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THE MARK OF RELIABILITY

Integrated Circuits

Vol. 1

DIGITAL INTERFACE CIRCUITS

- POWER DRIVERS
- DISPLAY DRIVERS
- TRANSISTOR ARRAYS
- DARLINGTON ARRAYS
- MOS AND BIMOS CIRCUITS
- SPECIALTY CIRCUITS

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Second Edition

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SPRAGUE ELECTRIC COMPANY

EXECUTIVE OFFICES: North Adams, Mass. 01247

INTEGRATED CIRCUIT OPERATIONS, SEMICONDUCTOR DIVISION

115 Northeast Cutoff • Worcester, Mass. 01606 • 617/853-5000

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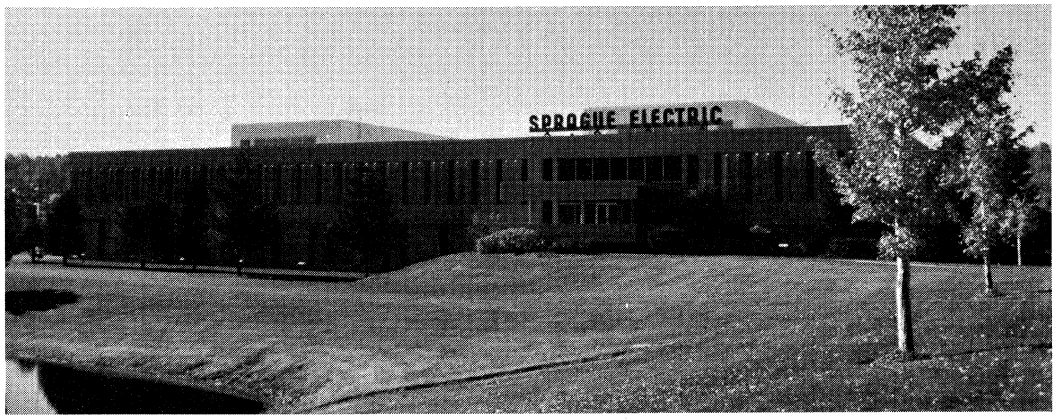
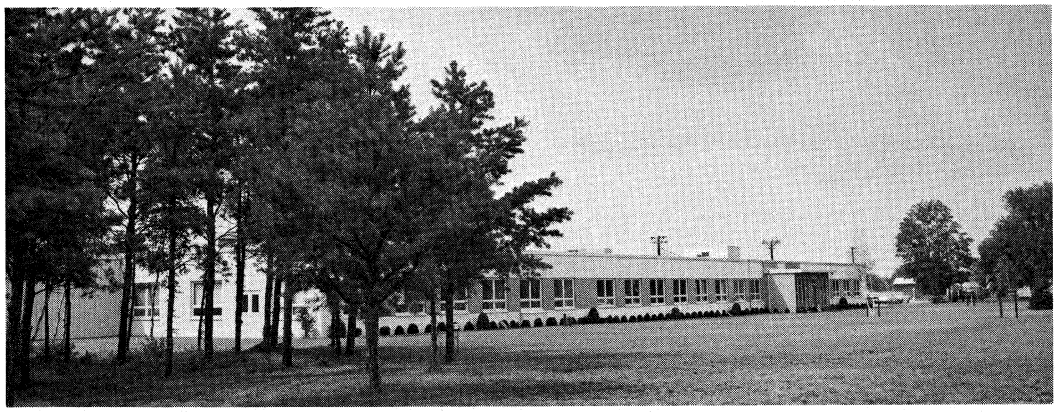
The Integrated Circuits Operations of the Sprague Electric Semiconductor Division is headquartered in a 140,000 square foot modern plant in Worcester, Mass. Discrete components, such as transistors and diodes and Hall Effect integrated circuits, are manufactured at the Division's Concord, N. H. plant, which occupies some 30,000 square feet of floor space.

Sprague Electric is a leading manufacturer of volume specialty circuits for the consumer, industrial controls, and peripherals markets. Production process technologies include P-Channel and complementary metal-gate MOS, high voltage and high-current bipolar and high-performance bipolar linear. This breadth of process technology makes it possible for Sprague Electric to manufacture optimum cost-performance integrated circuits.



INTEGRATED CIRCUIT OPERATIONS, Worcester, Massachusetts



TRANSISTOR OPERATIONS, Concord, New Hampshire

Sprague Facilities

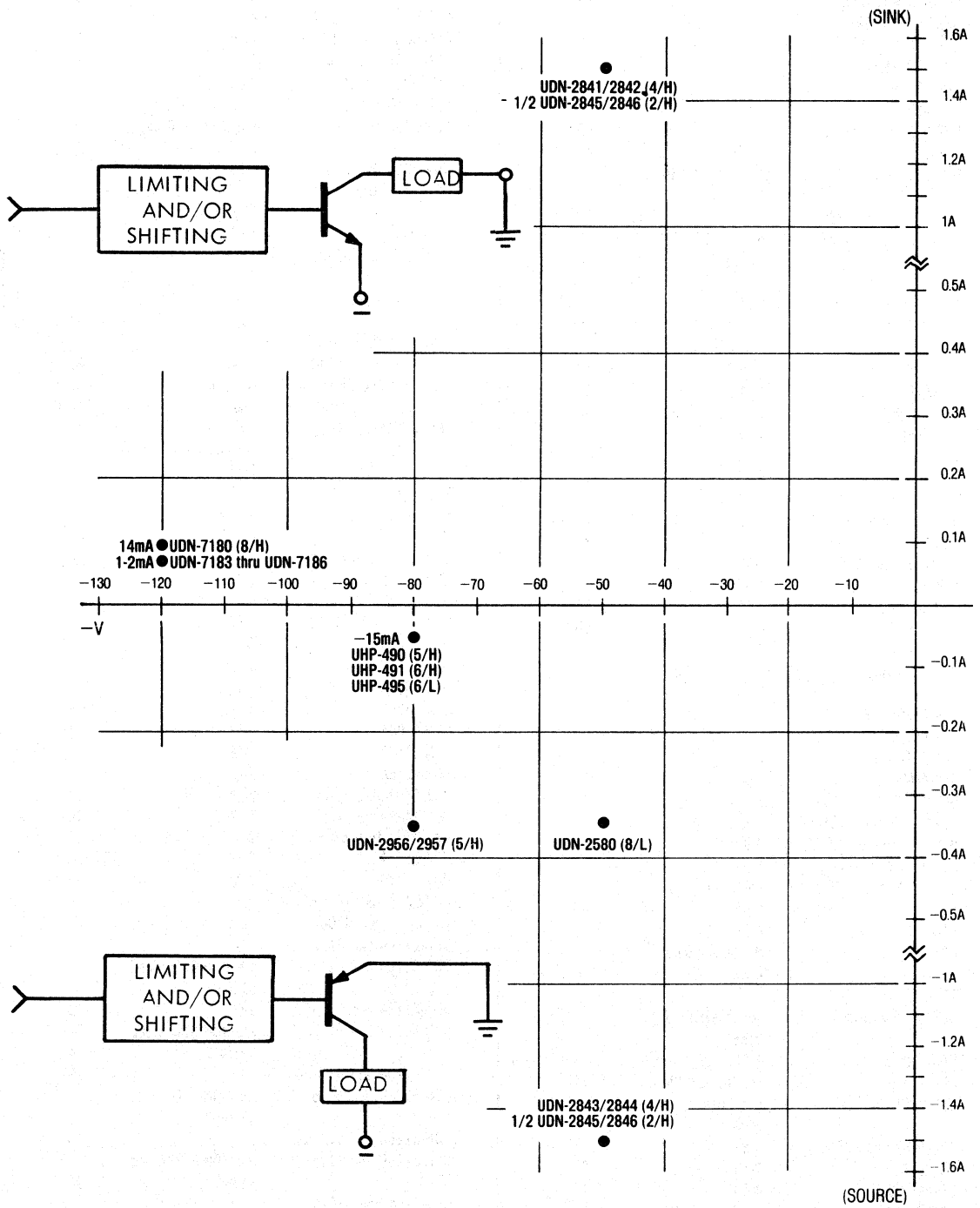
The Sprague Electric Company manufactures active and passive components in 17 locations in the United States and 5 countries in Europe and the Far East. Headquarters of the Semiconductor Division are located in the Worcester, Mass. plant shown in the photograph. All semiconductor wafer fabrication is in this plant as are all services integral to its support. Volume assembly operations are located both in Worcester and in Manila, Phillipines. Marketing and sales offices and sales representatives are located throughout the United States and Canada, Latin America, Europe, Japan, and other countries in Africa and the Far East.

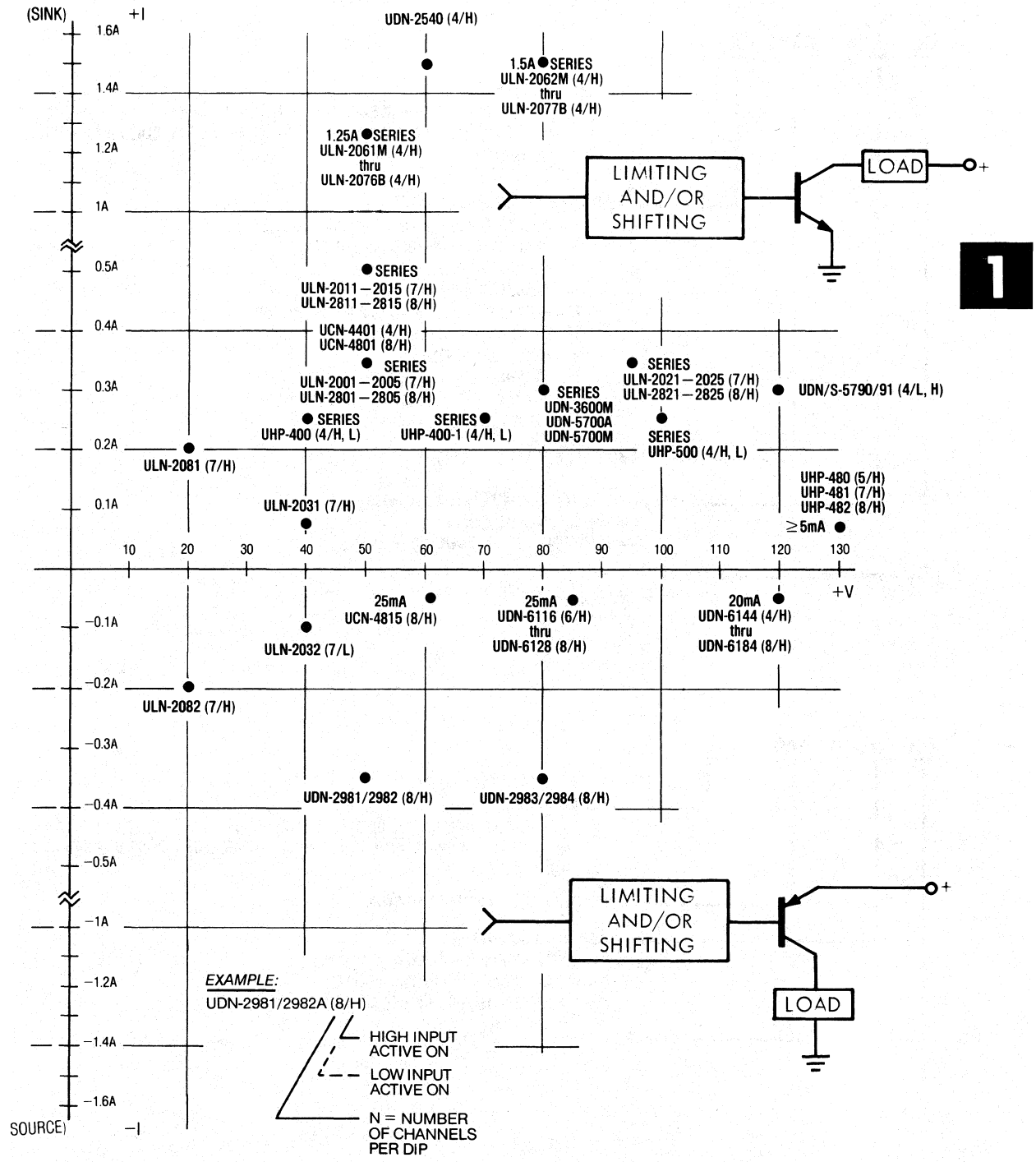
Index to All Devices (in numerical order)

Device Type	Data	Applications	Thermal*
UHC-400 thru 433-1	2-8		4D
UHD-400 thru 433-1	2-8		4B
UHP-400 thru 433-1	2-2	7-15	1B
UHP-480 and 481	3-2	7-4	1E
UHP-482	3-2		1D
UHD-490 and 491	3-5		4D
UHP-490 and 491	3-5	7-4	1E
UHP-495	3-7		1E
UHC-500 thru 533	2-8		4D
UHD-500 thru 533	2-8		4B
UHP-500 thru 533	2-2	7-7,16	1B
TPP-1000 and 2000	4-81		—
ULN-2001 thru 2025A	4-2	7-2,6,35,42	1B
ULN-2001 thru 2015R	see ULN-2001 thru 2015A		3B
ULS-2001 thru 2025H	4-11		4B
ULS-2001 thru 2015R	4-11		3A
ULN-2031 thru 2033A	4-22	7-6	1E
ULN-2031 thru 2033R	see ULN-2031 thru 2033A		3B
ULS-2045H	4-24		4B
ULS-2045R	see ULS-2045H		3B
ULN-2046A	4-24		1E
ULN-2046A-1	4-26		1E
ULN-2047A	4-27		1E
ULN-2054A	4-28		1E
ULN-2061 and 2062M	4-31	7-24	1C
ULN-2064 thru 2077B	4-31	7-5,32	2
ULN-2081 and 2082A	4-42	7-6,37	1E
ULN-2083A	4-43		1E
ULN-2083A-1	4-45		1E
ULS-2083H	4-43		4B
ULN-2086A	4-45		1E
ULN-2110 thru 2136A	see Linear Data Book		1E
ULN-2139D and 2139M	6-2		—
ULS-2139D and 2139M	6-2		—
ULN-2140A	6-4		1E
ULS-2140H	6-4		4B
ULN-2151D and 2151M	6-7		—
ULS-2151D and 2151M	6-7		—
ULN-2171D and 2171M	6-9		—
ULS-2171D and 2171M	6-9		—
ULN-2204 thru 2220A	see Linear Data Book		—
TPQ-2221	4-83		—
ULN-2221A	see Linear Data Book		1E
TPQ-2222	4-83		—
ULN-2224 thru 2298A	see Linear Data Book		—
ULN-2300M	6-11		1E
ULN-2301M	see ULN-2300M		1E
ULN-2401 thru 2430M	see Linear Data Book		—
TPQ-2483 and 2484	4-83		—
UDN-2540B	2-13		2
UDN-2580A	4-46		1A
UDN-2580R	see UDN-2580A		3A
ULN-2601A	see Linear Data Book		1E

*Thermal data is given in the curves on page 7-60.

Device Type	Data	Applications	Thermal*
ULN-2801 thru 2825A	4-50		1A
ULN-2801 thru 2815R	see ULN-2801 thru 2815A		3A
ULS-2801 thru 2825H	4-60		4A
ULS-2801 thru 2815R	4-60		3A
UDN-2841 thru 2846B	4-71	7-36	2
TPQ-2906 and 2907	4-83		—
UDN-2956 and 2957A	4-77	7-36	1B
UDN-2956 and 2957R	see UDN-2956 and 2957A		3B
UDN-2981 thru 2984A	4-79	7-6,39	1A
UDN-2981 thru 2984R	see UDN-2981 thru 2984A		3A
TPP-3000	4-81		—
ULN-3303 thru 3330Y	see Linear Data Book		—
UGN-3501M and 3501T	see Linear Data Book		—
UDN-3611 thru 3614M	2-19	7-21	1C
UDS-3611 thru 3614H	2-14		4C
ULN-3701 and 3702Z	see Linear Data Book		—
TPQ-3724 thru 3799	4-83		—
ULN-3801Q	see Linear Data Book		—
TPQ-3904 and 3906	4-83		—
UCN-4103A	5-3		—
UCN-4105A	5-4		—
UCN-4112A and 4112M	5-5		—
UCN-4116M	5—7		—
UCN-4123M	5-3		—
ULN-4136 thru 4336A	6-17		1E
UCN-4401A	5-9		1B
ULN-4436A	6-17		1E
UCN-4801A	5-9		—
UCN-4805A	5-12		1A
UCN-4806A	5-12		1A
UCN-4810A	5-16		1A
UCN-4815A	5-19		—
UDN-5703 thru 5707A	2-23	7-2,19	1B
UDS-5703 thru 5707H	2-27		4B
UDN-5711 thru 5714M	2-32	7-49	1C
UDN-5733A	2-26		1B
UDS-5733H	2-30		4B
UDS-5790 and 5791H	2-37		4B
TPQ-6001 thru 6100A	4-83		—
UDN-6116A and 6116A-2	3-9		1E
UDN-6116R and 6116R-2	see UDN-6116A and 6116A-2		3B
UDN-6118A and 6118A-2	3-9		1D
UDN-6118R and 6118R-2	see UDN-6118A and 6118A-2		3A
UDN-6126A and 6126A-2	3-9		1E
UDN-6126R and 6126R-2	see UDN-6126A and 6126A-2		3B
UDN-6128A and 6128A-2	3-9		1D
UDN-6128R and 6128R-2	see UDN-6128A and 6128A-2		3A
UDN-6144 and 6164A	3-13	7-4,27	1E
UDN-6184A	3-13		1D
TPQ-6501 thru 6700	4-83		—
UDN-7180 thru 7186A	3-17	7-3,27	1D


(SINK)
1.6A
1.4A
1.2A
1A
0.5A
0.4A
0.3A
0.2A
0.1A
UDN-2841/2842 (4/H)
1/2 UDN-2845/2846 (2/H)
LIMITING AND/OR SHIFTING
LOAD
14mA UDN-7180 (8/H)
1-2mA UDN-7183 thru UDN-7186
−130 −120 −110 −100 −90 −80 −70 −60 −50 −40 −30 −20 −10
−V
−15mA
UHP-490 (5/H)
UHP-491 (6/H)
UHP-495 (6/L)
−0.1A
−0.2A
−0.3A
−0.4A
−0.5A
−1A
−1.2A
−1.4A
−1.6A
UDN-2956/2957 (5/H)
UDN-2580 (8/L)
LIMITING AND/OR SHIFTING
LOAD
UDN-2843/2844 (4/H)
1/2 UDN-2845/2846 (2/H)
(SOURCE)


(SINK)
+I
1.6A
1.4A
1.2A
1A
0.5A
0.4A
0.3A
0.2A
0.1A
UDN-2540 (4/H)
1.5A SERIES
ULN-2062M (4/H)
thru
ULN-2077B (4/H)
1.25A SERIES
ULN-2061M (4/H)
thru
ULN-2076B (4/H)
LIMITING
AND/OR
SHIFTING
LOAD
+
SERIES
ULN-2011—2015 (7/H)
ULN-2811—2815 (8/H)
UCN-4401 (4/H)
UCN-4801 (8/H)
SERIES
ULN-2001—2005 (7/H)
ULN-2801—2805 (8/H)
SERIES
UHP-400 (4/H, L)
SERIES
UHP-400-1 (4/H, L)
SERIES
UDN-3600M
UDN-5700A
UDN-5700M
SERIES
ULN-2021—2025 (7/H)
ULN-2821—2825 (8/H)
SERIES
UHP-500 (4/H, L)
UDN/S-5790/91 (4/L, H)
ULN-2081 (7/H)
ULN-2031 (7/H)
UHP-480 (5/H)
UHP-481 (7/H)
UHP-482 (8/H)
≥5mA
10
20
30
40
50
60
70
80
90
100
110
120
130
+V
25mA
UCN-4815 (8/H)
25mA
UDN-6116 (6/H)
thru
UDN-6128 (8/H)
20mA
UDN-6144 (4/H)
thru
UDN-6184 (8/H)
ULN-2032 (7/L)
−0.1A
−0.2A
−0.3A
−0.4A
−0.5A
−1A
−1.2A
−1.4A
−1.6A
ULN-2082 (7/H)
UDN-2981/2982 (8/H)
UDN-2983/2984 (8/H)
LIMITING
AND/OR
SHIFTING
+
LOAD
EXAMPLE:
UDN-2981/2982A (8/H)
HIGH INPUT
ACTIVE ON
LOW INPUT
ACTIVE ON
N = NUMBER
OF CHANNELS
PER DIP
SOURCE)
−I

How to Place an Order

UL N - 2046 A - 1

INSTRUCTIONS.
1 = SELECTED VERSION, SEE DETAIL SPECIFICATIONS
MIL = MILITARY GRADE WITH SCREENING TO MIL-STD-883, CLASS B (HERMETIC PARTS ONLY).

PACKAGE DESIGNATION.
A = PLASTIC, 14-, 16-, 18-, or 22-PIN DUAL IN-LINE
B = PLASTIC, 16-PIN WEBBED DUAL IN-LINE
C = CHIPS OR WAFERS
D = METAL CAN, 8-PIN
H = HERMETIC, 8-, 14-, 16-, or 18-PIN DUAL IN-LINE
J = HERMETIC, 14-PIN FLAT PACK
K = METAL CAN, 10-PIN
M = PLASTIC, 8-PIN DUAL IN-LINE
R = HERMETIC, 14-, 16-, or 18-PIN DUAL IN-LINE
T = PLASTIC, 3-LEAD

DEVICE TYPE (ALWAYS FOUR DIGITS).

OPERATING AMBIENT TEMPERATURE RANGE.
N = COMMERCIAL/INDUSTRIAL
S = FULL MILITARY/EXTENDED INDUSTRIAL

FAMILY
UC = CMOS, BiMOS, AND I^2L
UD = DIGITAL DRIVERS
UG = HALL EFFECT DEVICES
UL = LINEAR DEVICES

UH D - 400 - 1

INSTRUCTIONS.
1 = SELECTED VERSION, SEE DETAIL SPECIFICATIONS
MIL = MILITARY GRADE WITH SCREENING TO MIL-STD-883, CLASS B (HERMETIC PARTS ONLY).

DEVICE TYPE (ALWAYS THREE DIGITS).

PACKAGE DESIGNATION
C = HERMETIC, 14-PIN FLAT PACK
D = HERMETIC, 14- or 16-PIN DUAL IN-LINE
P = PLASTIC, 14-, 16-, OR 18-PIN DUAL IN-LINE

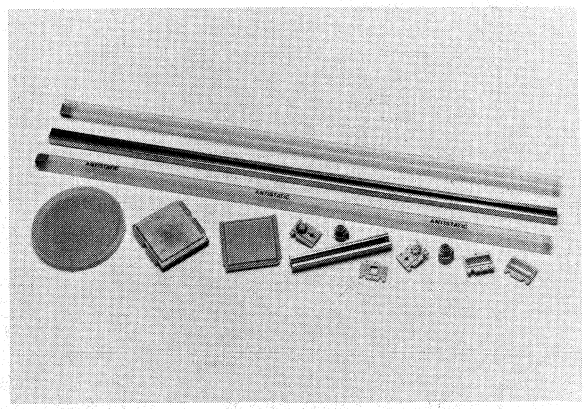
FAMILY

How Integrated Circuits are Shipped

Integrated circuits are shipped in one of these carriers:

Slide Magazine
A-Channel Plastic Tubing
A-Channel Metal Tubing
Barnes Carrier
Individual Plastic Box

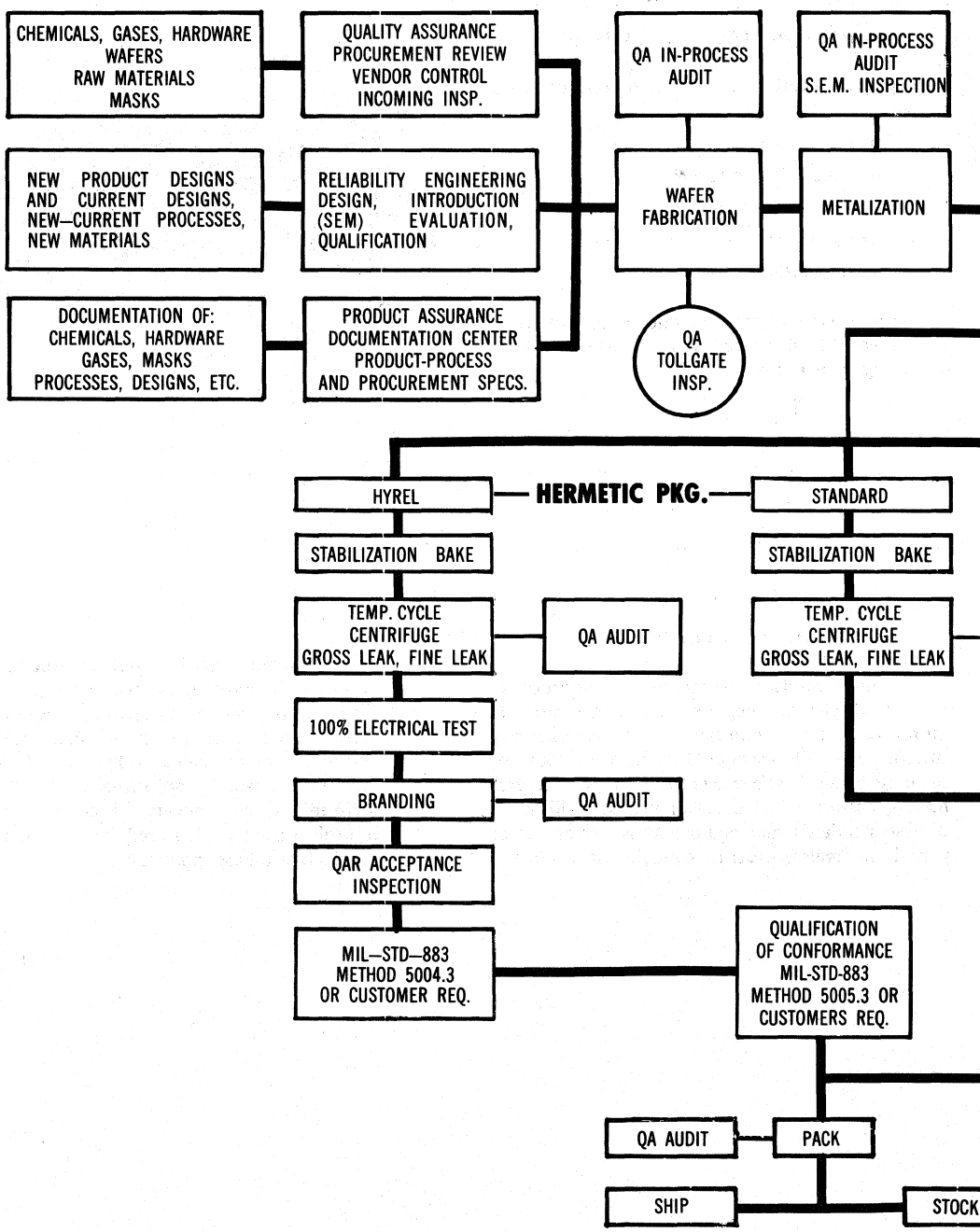
Integrated circuit chips are shipped in either unscribed wafer form or individually partitioned in a see-through plastic box.

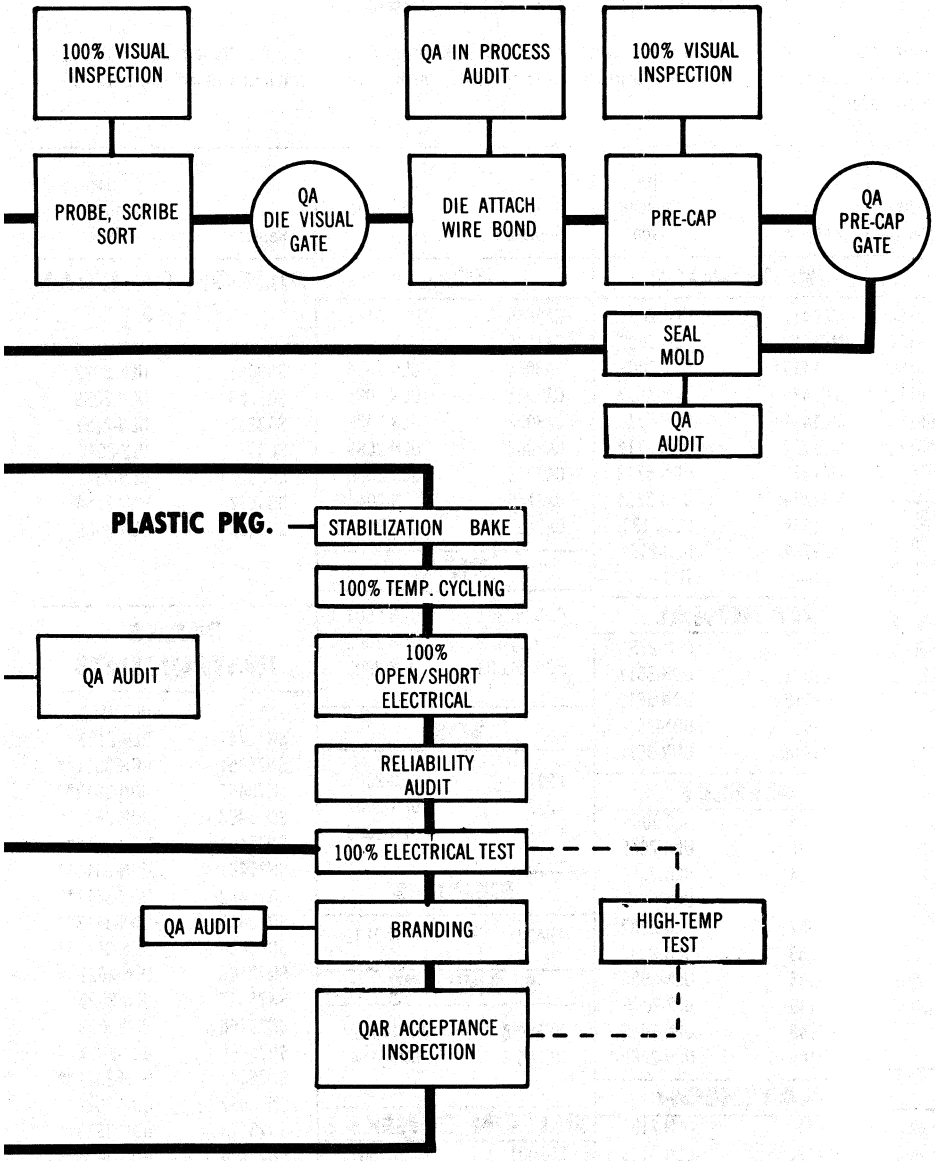


Quality Control and Reliability

All critical points in the manufacturing processes of Sprague Electric integrated circuits are carefully monitored for compliance to engineering specifications. Electrical tests are made on 100% of the parts by automatic testers. Lot sampling assures meeting customer A.Q.L. requirements. Calibration of test standards and equipment is performed at periodic intervals in order to maintain test accuracy.

The Sprague Electric Company conducts a continuing reliability assurance program to detect deviations in device characteristics. Test samples are taken at random from each lot and are subjected to testing for performance evaluation. Periodically, finished test samples are subjected to all electrical performance requirements. A copy of the quality control inspection plan used for specific integrated circuits is available upon request.


CHEMICALS, GASES, HARDWARE
WAFERS
RAW MATERIALS
MASKS
QUALITY ASSURANCE
PROCUREMENT REVIEW
VENDOR CONTROL
INCOMING INSP.
QA IN-PROCESS
AUDIT
QA IN-PROCESS
AUDIT
S.E.M. INSPECTION
NEW PRODUCT DESIGNS
AND CURRENT DESIGNS,
NEW–CURRENT PROCESSES,
NEW MATERIALS
RELIABILITY ENGINEERING
DESIGN, INTRODUCTION
(SEM) EVALUATION,
QUALIFICATION
WAFER
FABRICATION
METALIZATION
DOCUMENTATION OF:
CHEMICALS, HARDWARE
GASES, MASKS
PROCESSES, DESIGNS, ETC.
PRODUCT ASSURANCE
DOCUMENTATION CENTER
PRODUCT-PROCESS
AND PROCUREMENT SPECS.
QA
TOLLGATE
INSP.
HYREL
HERMETIC PKG.
STANDARD
STABILIZATION BAKE
STABILIZATION BAKE
TEMP. CYCLE
CENTRIFUGE
GROSS LEAK, FINE LEAK
QA AUDIT
TEMP. CYCLE
CENTRIFUGE
GROSS LEAK, FINE LEAK
100% ELECTRICAL TEST
BRANDING
QA AUDIT
QAR ACCEPTANCE
INSPECTION
MIL–STD–883
METHOD 5004.3
OR CUSTOMER REQ.
QUALIFICATION
OF CONFORMANCE
MIL-STD-883
METHOD 5005.3 OR
CUSTOMERS REQ.
QA AUDIT
PACK
SHIP
STOCK



PRODUCTION/QA FLOW CHART

INTERCHANGEABILITY GUIDE

The suggested Sprague replacement devices are based on similarity as shown in currently published data. Exact replacement in all applications is not guaranteed and the user should compare the specifications of the original and recommended equivalent.

To Replace	Use Sprague Type
DIONICS	
DI302	UDN-7184*
DI502	UDN-6144
DI507	UDN-6164
DI509	UDN-6116*
DI512	UDN-6184
DI514	UDN-6118*
EXAR	
XR2001	ULN-2001
XR2002	ULN-2002
XR2003	ULN-2003
XR2201	ULN-2001
XR2202	ULN-2002
XR2203	ULN-2003
XR2204	ULN-2004
FAIRCHILD	
FPQ—	TPQ—
μA741	ULN-2151
μA3045	ULS-2045
μA3046	ULN-2046
μA3054	ULN-2054
μA3086	ULN-2086
9665	ULN-2001
9666	ULN-2002
9667	ULN-2003
9668	ULN-2004
ITT	
512	UHP-491
552	ULN-2001
554	ULN-2002
556	ULN-2003
652	ULN-2001
654	ULN-2002
656	ULN-2003

To Replace	Use Sprague Type
MOTOROLA	
MC1411	ULN-2001
MC1412	ULN-2002
MC1413	ULN-2003
MC1439	ULN-2139
MC1471	UDN-5711
MC1472	UDN-5712
MC1473	UDN-5713
MC1474	UDN-5714
MC1539	ULS-2139
MC1741	ULN-2151
MPQ—	TPQ—
NATIONAL	
LM741	ULN-2151
LM3611	UDN-3611
LM3612	UDN-3612
LM3613	UDN-3613
LM3614	UDN-3614
PLESSEY	
SL3045	ULS-2045
SL3046	ULN-2046
SL3054	ULN-2054
SL3081	ULN-2081
SL3082	ULN-2082
SL3083	ULN-2083
SL3086	ULN-2086
SL3145	ULS-2045
SL3146	ULN-2046-1
SL3183	ULN-2083-1
RAYTHEON	
RC741	ULN-2151
RC4136	ULN-4136
RC4236	ULN-4236
RC4336	ULN-4336
RC4436	ULN-4436
RM741	ULS-2151

To Replace	Use Sprague Type
RCA	
CA3045	ULS-2045
CA3046	ULN-2046
CA3054	ULN-2054
CA3081	ULN-2081
CA3082	ULN-2082
CA3083	ULN-2083
CA3086	ULN-2086
CA3146	ULN-2046-1
CA3183	ULN-2083-1
RIFA	
PBD352301	ULN-2001
PBD352302	ULN-2002
PBD352303	ULN-2003
SGS	
L201	ULN-2001
L202	ULN-2002
L203	ULN-2003
SIEMENS	
TBA221	ULN-2151
SIGNETICS	
NE584-8	UDN-7180*
NE585-6	UDN-6164*
SILICON GENERAL	
SG2001	ULN-2001
SG2002	ULN-2002
SG2003	ULN-2003
SG2004	ULN-2004
SG3081	ULN-2081

To Replace	Use Sprague Type
SILICON GENERAL (Cont.)	
SG3082	ULN-2082
SG3086	ULN-2086
SG3217	ULN-2151
SG3821J	ULS-2045
SG3821N	ULN-2046
SG3822	ULN-2054
SG3886	ULN-2086
TEXAS INSTRUMENTS	
SN52741	ULS-2151
SN72741	ULN-2151
SN75451	UDN-3611**
SN75452	UDN-3612**
SN75453	UDN-3613**
SN75454	UDN-3614**
SN75461	UDN-3611**
SN75462	UDN-3612**
SN75463	UDN-3613**
SN75464	UDN-3614**
SN75466	ULN-2021
SN75467	ULN-2022
SN75468	ULN-2023
SN75469	ULN-2024
SN75471	UDN-3611**
SN75472	UDN-3612**
SN75473	UDN-3613**
SN75474	UDN-3614**
SN75476	UDN-5711
SN75477	UDN-5712
SN75478	UDN-5713
SN75479	UDN-5714

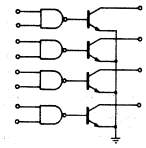
* Suggested replacement devices contain pull-down resistors or OFF-bias references. Other devices within the same Sprague series indicated may be more suitable for specific applications.

** Some differences in specified switching speed with the Sprague device being superior for use with inductive loads.

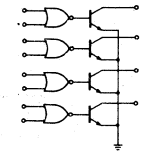
Device Type	Data	Applications	Thermal
UHC-400 thru 433-1	2-8		4D
UHD-400 thru 433-1	2-8		4B
UHP-400 thru 433-1	2-2	7-15	1B
UHC-500 thru 533	2-8		4D
UHD-500 thru 533	2-8		4B
UHP-500 thru 533	2-2	7-7, 16	1B
UDN-2540B	2-13		2
UDS-3611 thru 3614H	2-14		4C
UDN-3611 thru 3614M	2-19	7-21	1C
UDN-5703 thru 5707A	2-23	7-2, 19	1B
UDS-5703 thru 5707H	2-27		4B
UDN-5711 thru 5714M	2-32	7-19	1C
UDN-5733A	2-26		1B
UDS-5733H	2-30		4B
UDS-5790 and 5791H	2-37		4B

Device Type	I_{OUT}	V_{OUT}	Outputs
UH( )-400 thru 433	500 mA	40 V	Sink 4
UH( )-400-1 thru 433-1	500 mA	70 V	Sink 4
UH( )-500 thru 533	500 mA	100 V	Sink 4
UDN-2540B	1.5 A	60 V	Sink 4
UD( )-3611 thru 3614H/M	600 mA	80 V	Sink 2
UD( )-5703 thru 5707A/H	600 mA	80 V	Sink 4
UDN-5711 thru 5714M	600 mA	80 V	Sink 2
UD( )-5733A/H	600 mA	80 V	Sink 4
UDS-5790 and 5791H	500 mA	120 V	Sink 4

SERIES UHP-400, UHP-400-1, & UHP-500 POWER and RELAY DRIVERS — PLASTIC ENCASED



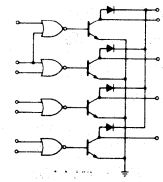
UHP-400/400-1/500
Quad 2 AND



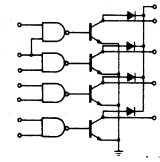
UHP-402/402-1/502
Quad 2 OR

FEATURES

- Inputs Compatible with DTL/TTL
- 500mA Output Sink Current Capability
- Pinning Compatible with 54/74 Logic Series
- Transient Protected Outputs on Relay Drivers
- High Voltage Output – 100V Series UHP-500, 70V Series UHP-400-1, 40V Series UHP-400



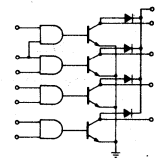
UHP-403/403-1/503
Quad OR



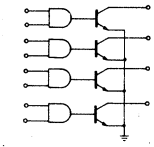
UHP-406/406-1/506
Quad AND

Description

These power and relay drivers are bi-polar monolithic circuits and incorporate logic gates and high-current switching transistors on the same chip. Each output transistor is capable of sinking 500mA in the ON state. In the OFF state, Series UHP-400 devices will sustain 40V, Series UHP-400-1 devices will sustain 70V, and Series UHP-500 devices will sustain 100V.



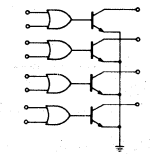
UHP-407/407-1/507
Quad NAND



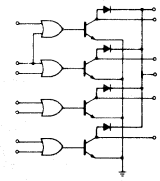
UHP-408/408-1/508
Quad 2 NAND

Applications

The UHP-400, UHP-400-1, and UHP-500 Series Power Drivers are ideally suited for driving incandescent lamps, relays, solenoids, and other interface devices with up to 1A output current per package.



UHP-432/432-1/532
Quad 2 NOR



UHP-433/433-1/533
Quad NOR

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} 7V
Input Voltage, V_{in}: 5.5V
Output Off-state Voltage, V_{off}:
  Series UHP-400 ..... 40V
  Series UHP-400-1 ..... 70V
  Series UHP-500 ..... 100V
Output On-State Sink Current, I_{on} 500mA
Suppression Diode Off-State Voltage, V_{off}.
  Series UHP-400 ..... 40V
  Series UHP-400-1 ..... 70V
  Series UHP-500 ..... 100V
Suppression Diode On-State Current, I_{on} 500mA
Operating Free-Air Temperature Range, T_A ..... 0°C to +70°C
Storage Temperature Range, T_S ..... −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC}):	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+70	°C
Current into any output (ON state)			250	mA

ELECTRICAL CHARACTERISTICS:
(over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current at all Inputs except Strobe	$I_{in(0)}$		MAX	0.4V	4.5V			−0.55	−0.8	mA	2
"0" Input Current at Strobe	$I_{in(0)}$		MAX	0.4V	4.5V			−1.1	−1.6	mA	
"1" Input Current at all Inputs except Strobe	$I_{in(1)}$		MAX	2.4V	0V				40	μA	2
			MAX	5.5V	0V				1	mA	
"1" Input Current at Strobe	$I_{in(1)}$		MAX	2.4V	0V				100	μA	2
			MAX	5.5V	0V				1	mA	

SWITCHING CHARACTERISTICS: V_{CC} = 5.0V, T_A = 25°C

Characteristic	Symbol	Test Conditions	Limits			Units	Notes
			Min.	Typ.	Max.		
Turn-on Delay Time Series UHP-400 Series UHP-400-1 Series UHP-500	t_{pd0}	V_S = 40V, R_L = 265Ω (6 Watts) V_S = 70V, R_L = 465Ω (10 Watts) V_S = 100V, R_L = 670Ω (15 Watts) C_L = 15pF		200	500	ns	3
Turn-off Delay Time Series UHP-400 Series UHP-400-1 Series UHP-500	t_{pd1}	V_S = 40V, R_L = 265Ω (6 Watts) V_S = 70V, R_L = 465Ω (10 Watts) V_S = 100V, R_L = 670Ω (15 Watts) C_L = 15pF		300	750	ns	3

INPUT PULSE CHARACTERISTICS

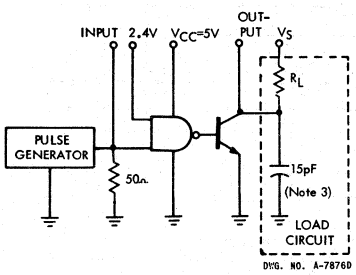
$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

Type UHP-400, UHP-400-1, and UHP-500 Quad 2-Input AND Power Drivers

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-400	I_{off}		MIN	2.0V	2.0V	40V			50	μA	
"1" Output Reverse Current Type UHP-400-1	I_{off}		MIN	2.0V	2.0V	70V			50	μA	
"1" Output Reverse Current Type UHP-500	I_{off}		MIN	2.0V	2.0V	100V			50	μA	
"0" Output Voltage	V_{on}		MIN	0.8V	V_{cc}	150mA			0.5	V	
			MIN	0.8V	V_{cc}	250mA			0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0V	5.0V			4	6	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0V	0V			17.5	24.5	mA	1, 2



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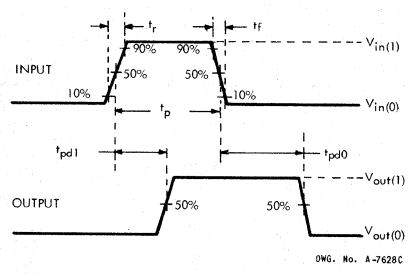

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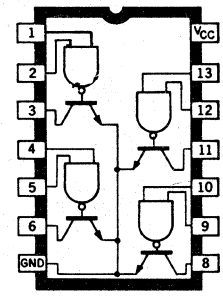
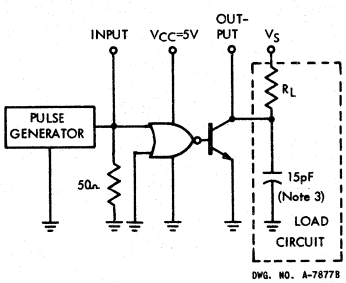


DWG. NO. A-7606

Type UHP-402, UHP-402-1, and UHP-502 Quad 2-Input OR Power Drivers

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-402	I_{off}		MIN	2.0V	0V	40V			50	μA	
"1" Output Reverse Current Type UHP-402-1	I_{off}		MIN	2.0V	0V	70V			50	μA	
"1" Output Reverse Current Type UHP-502	I_{off}		MIN	2.0V	0V	100V			50	μA	
"0" Output Voltage	V_{on}		MIN	0.8V	0.8V	150mA			0.5	V	
			MIN	0.8V	0.8V	250mA			0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0V	5.0V			4.1	6.3	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0V	0V			18	25	mA	1, 2



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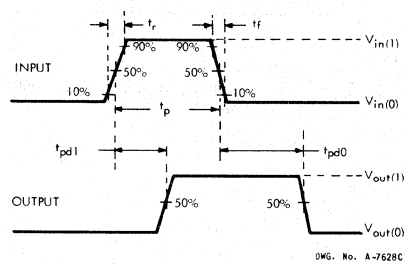

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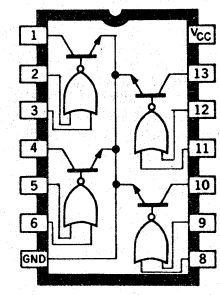


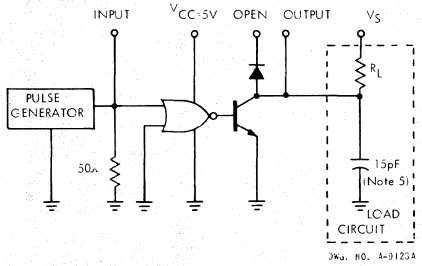
DWG. NO. A-7608

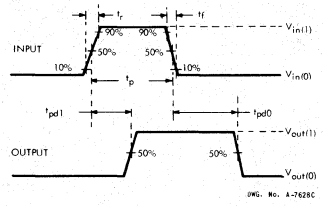
NOTES:
1. Typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.
2. Each gate.
3. Capacitance values specified include probe and test fixture capacitance.

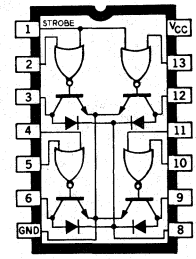
Type UHP-403, UHP-403-1, and UHP-503 Quad OR Relay Drivers

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-403	I_{off}		MIN	2.0V	0V	40V			100	μA	
"1" Output Reverse Current Type UHP-403-1	I_{off}		MIN	2.0V	0V	70V			100	μA	
"1" Output Reverse Current Type UHP-503	I_{off}		MIN	2.0V	0V	100V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8V	0.8V	150mA			0.5	V	
			MIN	0.8V	0.8V	250mA			0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0V	0V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0V	5.0V			4.1	6.3	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0V	0V			18	25	mA	1, 2





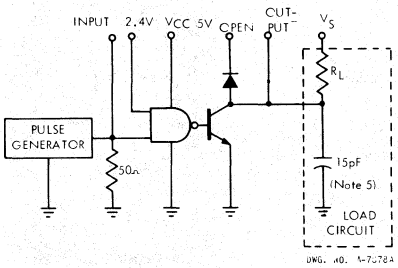


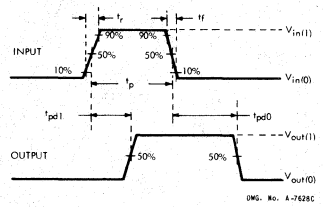
2

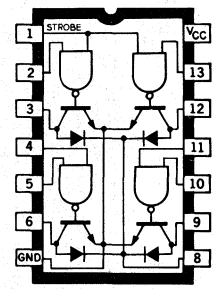
Type UHP-406, UHP-406-1, and UHP-506 Quad AND Relay Drivers

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-406	I_{off}		MIN	2.0V	2.0V	40V			100	μA	
"1" Output Reverse Current Type UHP-406-1	I_{off}		MIN	2.0V	2.0V	70V			100	μA	
"1" Output Reverse Current Type UHP-506	I_{off}		MIN	2.0V	2.0V	100V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8V	V_{CC}	150mA			0.5	V	
			MIN	0.8V	V_{CC}	250mA			0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0V	0V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0V	5.0V			4	6	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0V	0V			17.5	24.5	mA	1, 2







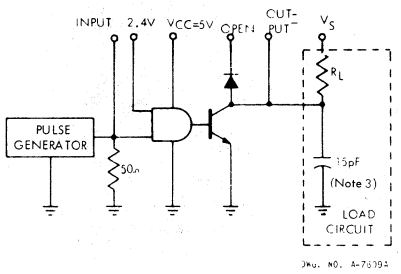
NOTES:

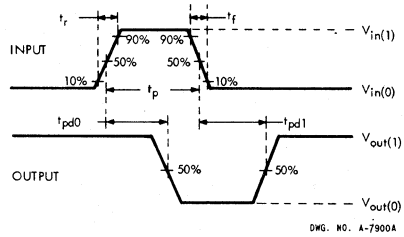
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each gate.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 200mA.
5. Capacitance values specified include probe and test fixture capacitance.

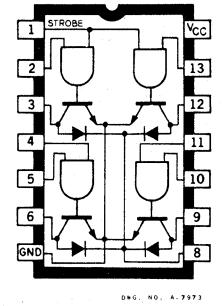
Type UHP-407, UHP-407-1, and UHP-507 Quad NAND Relay Drivers

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-407	I_{off}		MIN	0.8V	Vcc	50V			100	μA	
"1" Output Reverse Current; Type UHP-407-1	I_{off}		MIN	0.8V	Vcc	70V			100	μA	
"1" Output Reverse Current Type UHP-507	I_{off}		MIN	0.8V	Vcc	100V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0V	2.0V	150mA			0.5	V	
			MIN	2.0V	2.0V	250mA			0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	4
Diode Forward Voltage Drop	V_D	NOM	NOM	0V	0V			1.5	1.75	V	5
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0V	0V			6	7.5	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5V	5V			20	26.5	mA	1, 2



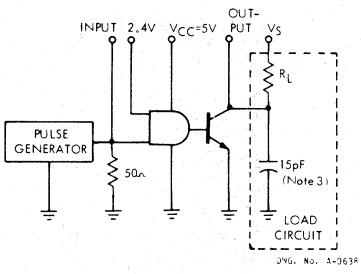


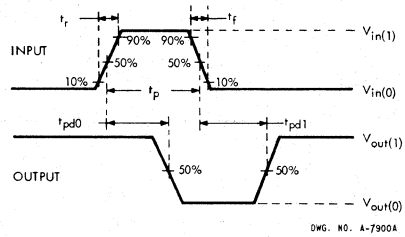


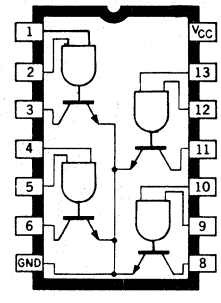
Type UHP-408, UHP-408-1, and UHP-508 Quad 2-Input NAND Power Drivers

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-408	I_{off}		MIN	0.8V	V_{CC}	40V			50	μA	
"1" Output Reverse Current Type UHP-408-1	I_{off}		MIN	0.8V	V_{CC}	70V			50	μA	
"1" Output Reverse Current Type UHP-508	I_{off}		MIN	0.8V	V_{CC}	100V			50	μA	
"0" Output Voltage	V_{on}		MIN	2.0V	2.0V	150mA			0.5	V	
			MIN	2.0V	2.0V	250mA			0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0V	0V			6	7.5	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0V	5.0V			20	26.5	mA	1, 2





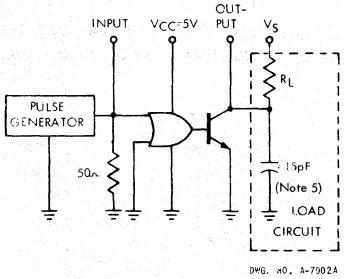


NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each gate.
3. Capacitance values specified include probe and test fixture capacitance.
4. Diode leakage current measured at $V_R = V_{off(min)}$.
5. Diode forward voltage drop measured at I_f = 200mA.

Type UHP-432, UHP-432-1, and UHP-532 Quad 2-Input NOR Power Drivers

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-432	I_{off}		MIN	0.8V	0.8V	40V			50	μA	
"1" Output Reverse Current Type UHP-432-1	I_{off}		MIN	0.8V	0.8V	70V			50	μA	
"1" Output Reverse Current Type UHP-532	I_{off}		MIN	0.8V	0.8V	100V			50	μA	
"0" Output Voltage	V_{on}		MIN	2.0V	0V	150mA			0.5	V	
			MIN	2.0V	0V	250mA			0.7	V	
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0V	5.0V			20	25	mA	1, 2
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0V	0V			6	7.5	mA	1, 2



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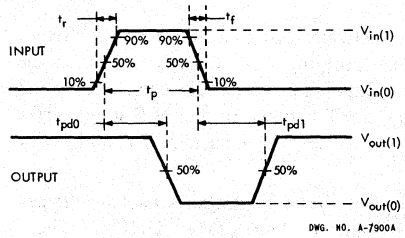

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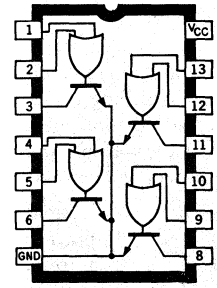

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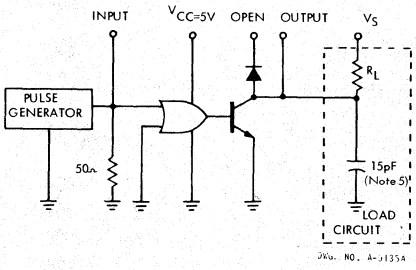
Type UHP-433, UHP-433-1, and UHP-533 Quad NOR Relay Drivers

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	Vcc	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-433	I_{off}		MIN	0.8V	0.8V	40V			100	μA	
"1" Output Reverse Current Type UHP-433-1	I_{off}		MIN	0.8V	0.8V	70V			100	μA	
"1" Output Reverse Current Type UHP-533	I_{off}		MIN	0.8V	0.8V	100V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0V	0V	150mA			0.5	V	
			MIN	2.0V	0V	250mA			0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0V	0V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0V	0V			6	7.5	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5V	5V			20	25	mA	1, 2



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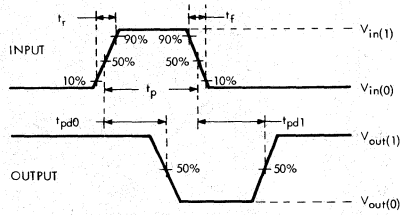

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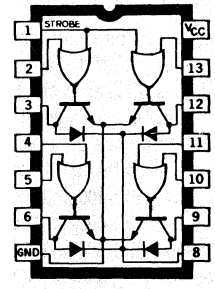
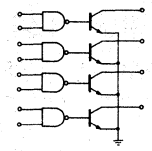


NOTES:
1. Typical values are at $V_{CC} = 5.0$, $T_A = 25°C$.
2. Each gate.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at $I_f = 200mA$.
5. Capacitance values specified include probe and test fixture capacitance.

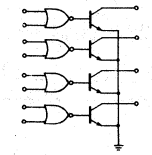
SERIES UHC- and UHD-400, 400-1, & 500 POWER and RELAY DRIVERS — HERMETICALLY-SEALED

FEATURES

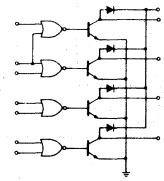
- 500mA Output Sink Current Capability
- DTL/TTL Compatible Inputs
- Transient Protected Outputs on Relay Drivers
- High Voltage Output – 100V Series 500, 70V Series 400-1, and 40V Series 400
- Hermetically-Sealed Packages to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B



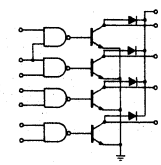
UHC-400/400-1/500
UHD-400/400-1/500



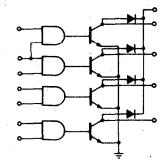
UHC-402/402-1/502
UHD-402/402-1/502



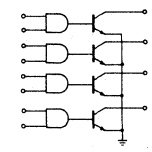
UHC-403/403-1/503
UHD-403/403-1/503



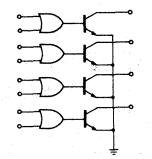
UHC-406/406-1/506
UHD-406/406-1/506



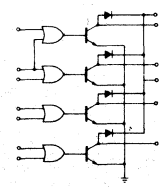
UHC-407/407-1/507
UHD-407/407-1/507



UHC-408/408-1/508
UHD-408/408-1/508



UHC-432/432-1/532
UHD-432/432-1/532



UHC-433/433-1/533
UHD-433/433-1/533

Description

These Series 400, 400-1, and 500 hermetically-sealed power and relay drivers are bi-polar monolithic circuits incorporating both logic gates and high-current switching transistors on the same chip. Each device contains four drivers capable of sinking 500mA in the ON state. In the OFF state, Series 400 devices will sustain 40V, Series 400-1 devices will sustain 70V, and Series 500 devices will sustain 100V.

All devices are available in either a 14-pin hermetic flat-pack package (Types UHC-) or a 14-pin hermetic dual in-line package (Types UHD-). These packages conform to the dimensional requirements of Military Specification MIL-M-38510 and meet all of the processing and environmental requirements of Military Standard MIL-STD-883, Method 5004 and 5005. These devices are also furnished in a plastic 14-pin dual in-line package (Types UHP-) for operation over a limited temperature range.

Applications

The UHC- and UHD- Series 400, 400-1, and 500 power and relay drivers are ideally suited for driving incandescent lamps, relays, solenoids, and other interface devices with up to 1A output current per package. Hermetic sealing and an operating temperature range of −55°C to +125°C recommend them for military and aerospace applications as well as commercial and industrial control applications where severe environments may be encountered.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} 7V
Input Voltage, V_{in}: 5.5V
Output Off-state Voltage, V_{off}:
  Series UHC-400 and UHD-400 ..... 40V
  Series UHC-400-1 and UHD-400-1 ..... 70V
  Series UHC-500 and UHD-500 ..... 100V
Output On-State Sink Current, I_{on} 500mA
Suppression Diode Off-State Voltage, V_{off}.
  Series UHC-400 and UHD-400 ..... 40V
  Series UHC-400-1 and UHD-400-1 ..... 70V
  Series UHC-500 and UHD-500 ..... 100V
Suppression Diode On-State Current, I_{on} 500mA
Operating Free-Air Temperature Range, T_A ..... −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC}):	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into any output (ON state)			250	mA

STATIC ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	Vcc	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current at all Inputs except Strobe	$I_{in(0)}$		MAX	0.4V	4.5V			−0.55	−0.8	mA	1, 2
"0" Input Current at Strobe	$I_{in(0)}$		MAX	0.4V	4.5V			−1.1	−1.6	mA	2
"1" Input Current at all Inputs except Strobe	$I_{in(1)}$		MAX	2.4V	0V				40	μA	1
			MAX	5.5V	0V				1	mA	1
"1" Input Current at Strobe	$I_{in(1)}$		MAX	2.4V	0V				100	μA	
			MAX	5.5V	0V				1	mA	
"1" Output Reverse Current	I_{off}										
Series 400			MIN			40V			100	μA	6
Series 400-1			MIN			70V			100	μA	6
Series 500			MIN			100V			100	μA	6
"0" Output Voltage	V_{on}	NOM	MIN			150mA			0.5	V	6
		NOM	MIN			250mA			0.7	V	6
		MAX	MIN			150mA			0.6	V	6
		MAX	MIN			250mA			0.8	V	6
Diode Leakage Current	I_{LK}	NOM	NOM			OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM					1.5	1.75	V	2, 4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX						7.5	mA	5, 6
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX						26.5	mA	5, 6

NOTES:
1. Each input.
2. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
3. Measured at $V_R = V_{off(min)}$.
4. Measured at I_f = 200mA.
5. Each gate.
6. Input test conditions are listed in Table IV.

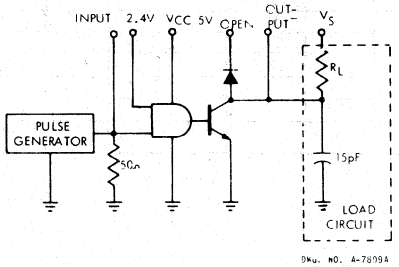
Table IV
INPUT CONDITIONS FOR OUTPUT CHARACTERISTIC MEASUREMENTS

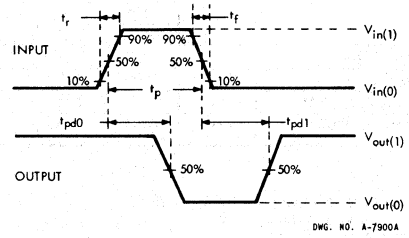
Type UHC- or UHD-	"1" Output Reverse Current (I_{off})		"0" Output Voltage (V_{on})		"1" Level Supply Current ($I_{CC(1)}$)		"0" Level Supply Current ($I_{CC(0)}$)	
	Driven Input	Other Input	Driven Input	Other Input	Driven Input	Other Input	Driven Input	Other Input
400, 400-1, 500	2.0V	2.0V	0.8V	V_{CC}	5.0V	5.0V	0V	0V
402, 402-1, 502	2.0V	2.0V	0.8V	0.8V	5.0V	5.0V	0V	0V
403, 403-1, 503	2.0V	0V	0.8V	0.8V	5.0V	5.0V	0V	0V
406, 406-1, 506	2.0V	2.0V	0.8V	V_{CC}	5.0V	5.0V	0V	0V
407, 407-1, 507	0.8V	V_{CC}	2.0V	2.0V	0V	0V	5.0V	5.0V
408, 408-1, 508	0.8V	V_{CC}	2.0V	2.0V	0V	0V	5.0V	5.0V
432, 432-1, 532	0.8V	0.8V	2.0V	0V	0V	0V	5.0V	5.0V
433, 433-1, 533	0.8V	0.8V	2.0V	0V	0V	0V	5.0V	5.0V

SWITCHING CHARACTERISTICS: V_{CC} = 5.0V, T_A = 25°C

Characteristic	Symbol	Test Conditions	Limits				Notes
			Min.	Typ.	Max.	Units	
Turn-on Delay Time Series 400 Series 400-1 Series 500	t_{pd0}	V_S = 40V, R_L = 265Ω (6 Watts) V_S = 70V, R_L = 465Ω (10 Watts) V_S = 100V, R_L = 670Ω (15 Watts)		200	500	ns	
Turn-off Delay Time Series 400 Series 400-1 Series 500	t_{pd1}	V_S = 40V, R_L = 265Ω (6 Watts) V_S = 70V, R_L = 465Ω (10 Watts) V_S = 100V, R_L = 670Ω (15 Watts)		300	750	ns	

Typical Switching Test Circuit



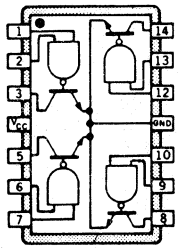


INPUT PULSE CHARACTERISTICS

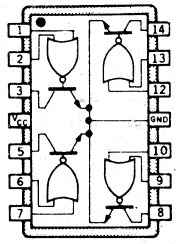
$V_{in(0)}$ = 0V	t_f = 7 ns	t_p = 1 µs
$V_{in(1)}$ = 3.5V	t_r = 14 ns	PRR = 500kHz

THERMAL DATA	UHC-	UHD-	Units
Thermal Resistance, Junction to Case, θ_{jc}	80	65	°C/Watt
Thermal Resistance, Junction to Free Air, θ_{ja}	140	90	°C/Watt

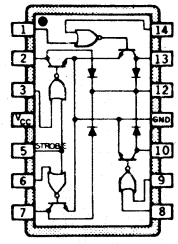
Device Pinning



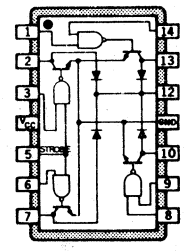
UHC-400
UHC-400-1
UHC-500



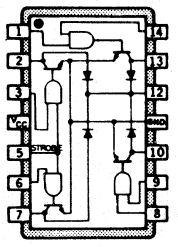
UHC-402
UHC-402-1
UHC-502



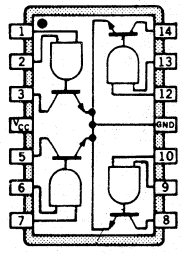
UHC-403
UHC-403-1
UHC-503



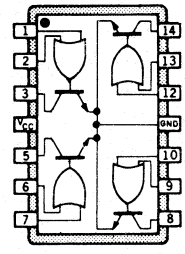
UHC-406
UHC-406-1
UHC-506



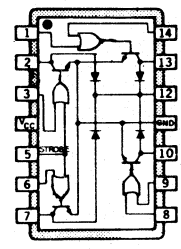
UHC-407
UHC-407-1
UHC-507



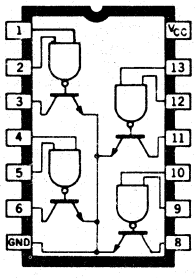
UHC-408
UHC-408-1
UHC-508



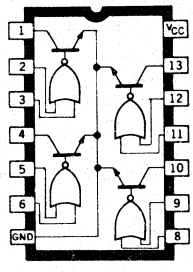
UHC-432
UHC-432-1
UHC-532



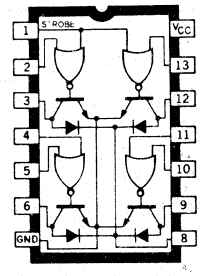
UHC-433
UHC-433-1
UHC-533



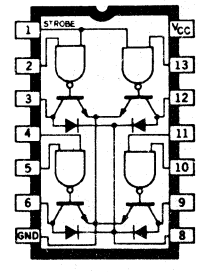
UHD-400
UHD-400-1
UHD-500



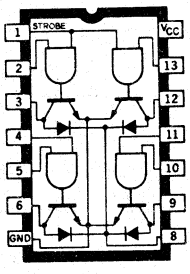
UHD-402
UHD-402-1
UHD-502



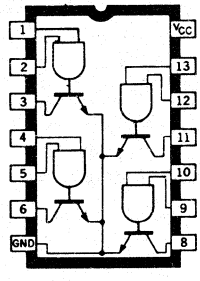
UHD-403
UHD-403-1
UHD-503



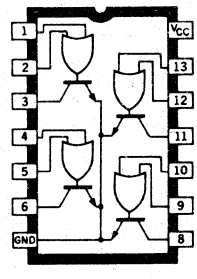
UHD-406
UHD-406-1
UHD-506



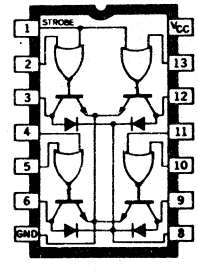
UHD-407
UHD-407-1
UHD-507



UHD-408
UHD-408-1
UHD-508



UHD-432
UHD-432-1
UHD-532



UHD-433
UHD-433-1
UHD-533

POWER DRIVERS WITH MIL-STD-883 HIGH-RELIABILITY SCREENING

Power drivers with high-reliability screening can be ordered by adding the suffix "MIL" to the part number, for example, UHD-400MIL. If marking with the customers part number is necessary in place of the Sprague Electric part number, this must be stated on the purchase order with the marking desired.

Table I — 100% Production Screen Tests (All Hermetic Parts)
MIL-STD-883, Method 5004, Class B, Paragraphs 3.1.1 thru 3.1.6

Screen	MIL-STD-883 Test Method	Conditions
Internal Visual	2010, Cond. B	—
Stabilization Bake	1008, Cond. C	150°C, 24 Hours
Thermal Shock	1011, Cond. A	0 to 100°C, 15 Cycles
Constant Acceleration	2001, Cond. E	30,000 G's, Y1 Plane
Fine Seal	1014, Cond. A	5 x 10^{-7} Maximum
Gross Seal	1014, Cond. C	—
Electrical	—	Per Eng. Bull. 29300.1
Marking	—	Sprague or customer part number, date code, lot identification, index point

Table II — 100% High-Reliability Screening ("MIL" Suffix Parts Only)
MIL-STD-883, Method 5004, Class B, Paragraphs 3.1.9 thru 3.1.15 and 3.1.18

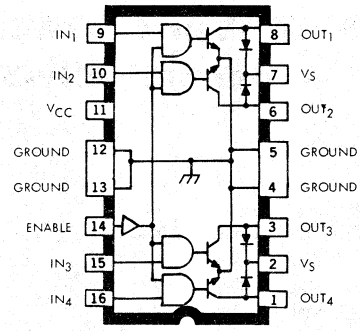
Screen	MIL-STD-883 Test Method	Conditions
Interim Electrical	5005, Gp A, Subgp 1	25°C per Eng. Bull. 29300.1
Burn-In	1015, Cond. A	125°C, 160 Hours
Static Electrical	5005, Gp A, Subgp 1	25°C per Eng. Bull. 29300.1
	5005, Gp A, Subgp 2 & 3	−55° & +125°C per Eng. Bull. 29300.1
Dynamic & Functional Electrical	5005, Gp A, Subgp 4, 7 & 9	25°C per Eng. Bull. 29300.1
Fine Seal	1014, Cond. A	5 x 10^{-7} Maximum
Gross Seal	1014, Cond. C	—
External Visual	2009	—

Table III — High-Reliability Qualification and Quality Conformance Inspection
MIL-STD-883, Method 5004, Class B, Paragraph 3.1.17

Test	MIL-STD-883 Test Method	Description
Group A Subgp. 1-4, 7 & 9	5005, Table I	Each production lot
Group B	5005, Table II	Each production lot
Group C	5005, Table III	End points, Gp. A, Subgp. 1, every 90 days
Group D	5005, Table IV	End points, Gp. A, Subgp. 1, every 6 months

UDN-2540B QUAD NAND POWER DRIVER

SPECIFICALLY DESIGNED for use in extremely harsh electrical environments, the UDN-2540B quad NAND driver interfaces between low-level signal processing circuits and medium-power inductive loads. The inputs are compatible with most TTL, DTL, LS TTL, 5 V to 15 V CMOS, and PMOS. The outputs include integral transient suppression diodes for inductive loads such as relays, solenoids, d-c and stepping motors. These devices can also be used to drive incandescent or heater loads.



ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Output Voltage, V_{OUT} ..... 60 V
Output Sustaining Voltage, $V_{CE(SUS)}$ ..... 35 V
Output Current, I_{OUT} ..... 1.5 A
Logic Supply Voltage, V_{CC} ..... 18 V
Input Voltage, V_{IN} ..... 30 V
Power Dissipation, P_D (each driver) ..... 2.5 W
(total package) 2.77W*
Operating Temperature Range, T_A ..... 0°C to +70°C
Storage Temperature Range, T_S ..... −55°C to +150°C

*Derate at the rate of 22.2 mW/°C above 25°C.

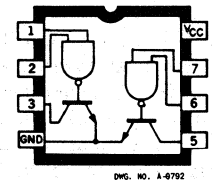
RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC} ..... +10.5 V to +17 V
Collector Current, I_C ..... $\leq$ 500 mA
High-Level Input Voltage, $V_{IN(1)}$ ..... $\geq$ 2.0V
Low-Level Input Voltage, $V_{IN(0)}$ ..... $\leq$ 0.4 V
Output Diode Reverse Voltage, V_S ..... $\leq$ 65 V

ELECTRICAL CHARACTERISTICS Over Operating Temperature Range And V_{CC} = 10 V to 15 V (Unless Otherwise Specified)

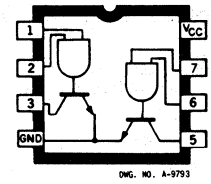
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
"1" Output Reverse Current	I_{OFF}	V_{OUT} = 50 V, V_{IN} = 0.4 V, V_{ENABLE} = 2.0 V	–	500	μA
		V_{OUT} = 50 V, V_{IN} = 2.0 V, V_{ENABLE} = 0.4 V	–	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 50 mA, V_{IN} = V_{ENABLE} = 0.4 V	35	–	V
"0" Output Voltage	V_{ON}	I_{OUT} = 500 mA, V_{IN} = V_{ENABLE} = 2.0 V	–	1.1	V
		I_{OUT} = 750 mA, V_{IN} = V_{ENABLE} = 2.0 V	–	1.25	V
		I_{OUT} = 1.0 A, V_{IN} = V_{ENABLE} = 2.0 V	–	1.4	V
		I_{OUT} = 1.25 A, V_{IN} = V_{ENABLE} = 2.0 V, V_{CC} = 12 V	–	1.6	V
"1" Input Voltage	$V_{IN(1)}$		2.0	–	V
"0" Input Voltage	$V_{IN(0)}$		–	0.5	V
"1" Input Current	$I_{IN(1)}$	V_{IN} = 15 V	–	20	μA
"0" Input Current	$I_{IN(0)}$	V_{IN} = 0.4 V	–	−200	μA
Input Clamp Voltage	V_{IK}	I_{IN} = −10 mA	–	−1.5	V
"1" Level Supply Current	$I_{CC(1)}$	I_{OUT} = 500 mA, V_{IN} = V_{ENABLE} = 2.0 V, V_{CC} = 15 V	–	33	mA
"0" Level Supply Current	$I_{CC(0)}$	V_{OUT} = 50 V, V_{IN} = V_{ENABLE} = 0.4 V, V_{CC} = 15 V	–	7.0	mA
Clamp Diode Forward Voltage	V_F	I_F = 1.0 A	–	2.1	V
		I_F = 1.25 A	–	2.5	V
Clamp Diode Leakage Current	I_R	V_R = 50 V, V_{IN} = V_{ENABLE} = 2.0 V, D_1 +D_2 or D_3 +D_4	–	1.0	mA

SERIES UDS-3600H DUAL 2-INPUT PERIPHERAL and POWER DRIVERS — Hermetically-Sealed



Type UDS-3611H
Dual AND Driver

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Sustaining Voltage of 80 V
- Hermetically Sealed Package
- High-Reliability Screening to MIL-STD-883, Class B



Type UDS-3612H
Dual NAND Driver

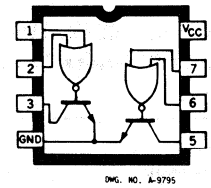
Description

These "mini-DIP" dual 2-input peripheral and power drivers are bi-polar monolithic integrated circuits incorporating AND, NAND, OR, or NOR logic gates, and high-current switching transistors on the same chip. The two output transistors are capable of simultaneously sinking 250 mA continuously at an ambient temperature of +75°C. In the OFF state, these drivers will sustain at least 80 V.

Applications

The Series UDS-3600H dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

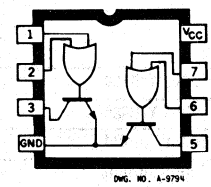
With appropriate external diode transient suppression, the Series UDS-3600H drivers can also be used with inductive loads such as relays, solenoids, and stepping motors. Similar devices with integral transient suppression are also available.



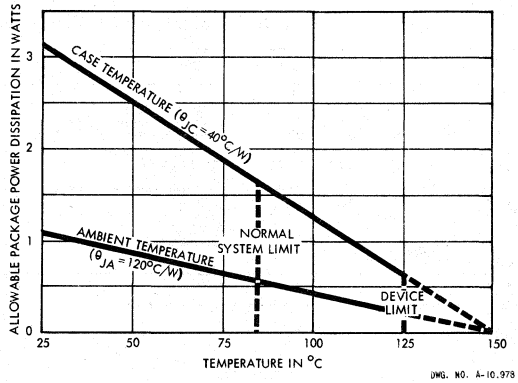
Type UDS-3613H
Dual OR Driver

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{in}	30 V
Output Off-State Voltage, V_{off}	80 V
Output On-State Sink Current, I_{on}	600 mA
Suppression Diode Off-State Voltage, V_{off}	80 V
Suppression Diode On-State Current, I_{on}	600 mA
Power Dissipation, P_D	1.0 W
Package Power Dissipation, P_D	See Graph
Ambient Temperature Range (operating), T_A	−55°C to +125°C
Storage Temperature Range, T_S	−65°C to +150°C



Type UDS-3614H
Dual NOR Driver



2

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into any output (ON state)	—	—	300	mA

ELECTRICAL CHARACTERISTICS (over operating temperature range unless otherwise noted)

			Test Conditions				Limits				
Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.7	V	
"0" Input Current	$I_{in(0)}$		MAX	0.4 V	30 V			50	100	μA	2
"1" Input Current	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS: V_{CC} = 5.0V, T_A = 25°C

			Limits				
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF	—	200	500	ns	3
Turn-off Delay Time	T_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF	—	300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

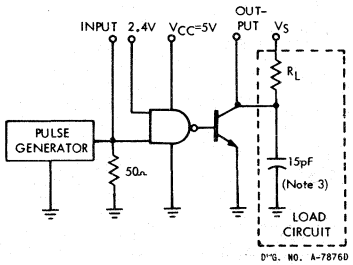
INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

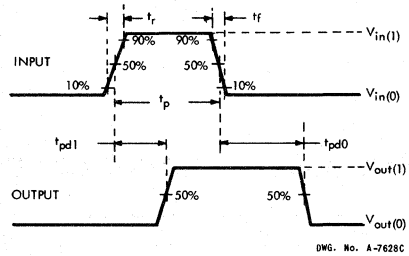
Type UDS-3611H Dual AND Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

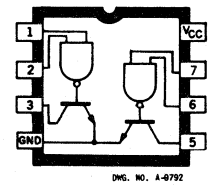
Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	150 mA		0.4	0.5	V	
			MIN	0.8 V	V_{CC}	300 mA		0.6	0.8	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			35	49	mA	1, 2



DWG. NO. A-7876D



DWG. No. A-7628C

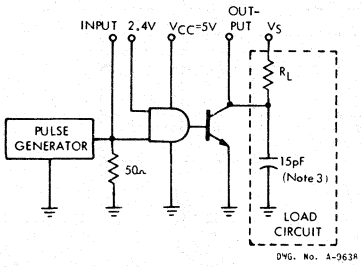


DWG. NO. A-9792

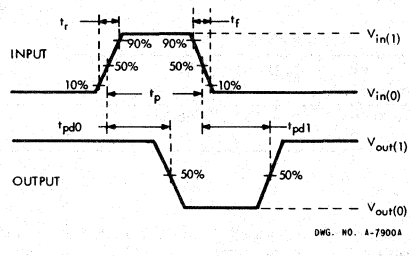
Type UDS-3612H Dual NAND Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	150 mA		0.4	0.5	V	
			MIN	2.0 V	2.0 V	300 mA		0.6	0.8	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	53	mA	1, 2



DWG. No. A-963R



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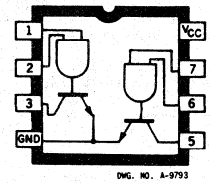


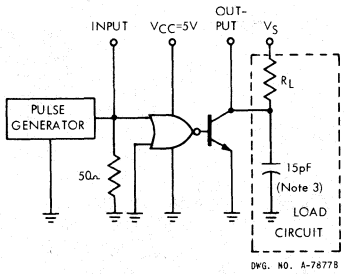
DWG. NO. A-9793

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

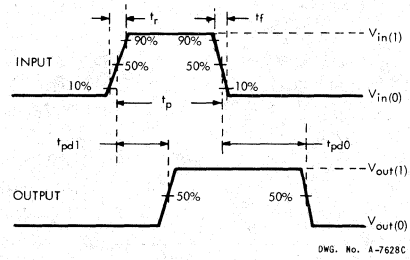
Type UDS-3613H Dual OR Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	150 mA		0.4	0.5	V	
			MIN	0.8 V	0.8 V	300 mA		0.6	0.8	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			36	50	mA	1, 2



DWG. NO. A-7877B



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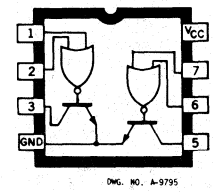


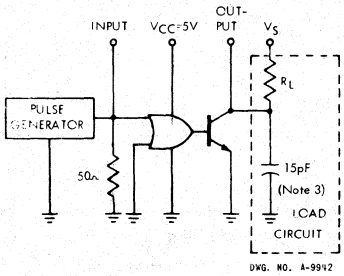
DWG. NO. A-9795

2

Type UDS-3614H Dual NOR Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	150 mA		0.4	0.5	V	
			MIN	2.0 V	0 V	300 mA		0.6	0.8	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	50	mA	1, 2



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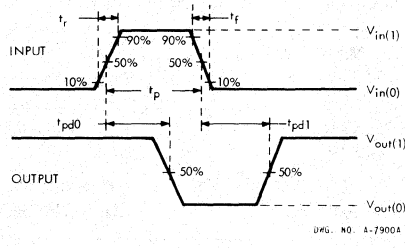

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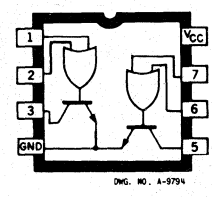


DWG. NO. A-9794

NOTES:
1. Typical values are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

POWER DRIVERS WITH MIL-STD-883 HIGH-RELIABILITY SCREENING

Power drivers with high-reliability screening can be ordered by adding the suffix 'MIL' to the part number, for example, UDS-3611H-MIL. If marking with the customer's part number is necessary in place of the Sprague Electric part number, this must be stated on the purchase order with the marking desired.

Table I — 100% Production Screen Tests (All Hermetic Parts)
MIL-STD-883, Method 5004, Class B, Paragraphs 3.1.1. thru 3.1.6

Screen	MIL-STD-883 Test Method	Conditions
Internal Visual	2010, Cond. B	—
Stabilization Bake	1008, Cond. C	150°C, 24 Hours
Thermal Shock	1011, Cond. A	0 to 100°C, 15 Cycles
Constant Acceleration	2001, Cond. E	30,000 G's, Y1 Plane
Fine Seal	1014, Cond. A	5×10^{-7} Maximum
Gross Seal	1014, Cond. C	—
Electrical	—	Per Specification
Marking	—	Sprague or customer part number, date code, lot identification, index point

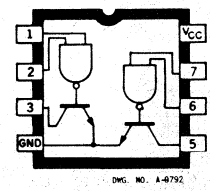
Table II — 100% High-Reliability Screening ("MIL" Suffix Parts Only)
MIL-STD-883, Method 5004, Class B, Paragraphs 3.1.9 thru 3.1.15 & 3.1.18

Screen	MIL-STD-883 Test Method	Conditions
Interim Electrical	5005, Gp A, Subgp 1	25°C per Specification
Burn-In	1015, Cond. A	125°C, 160 Hours
Static Electrical	5005, Gp A, Subgp 1	25°C per Specification
	5005, Gp A, Subgp 2 & 3	−55°C & +125°C per Specification
Dynamic & Functional Electrical	5005, Gp A, Subgp 4, 7 & 9	25°C per Specification
Fine Seal	1014, Cond. A	5×10^{-7} Maximum
Gross Seal	1014, Cond. C	—
External Visual	2009	—

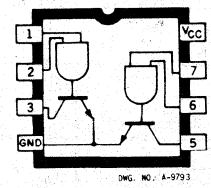
Table III — High-Reliability Qualification and Quality Conformance Inspection
MIL-STD-883, Method 5004, Class B, Paragraph 3.1.17

Test	MIL-STD-883 Test Method	Description
Group A Subgp. 1-4, 7 & 9	5005, Table I	Each production lot
Group B	5005, Table II	Each production lot
Group C	5005, Table III	End points, Gp. A, Subgp. 1, every 90 days
Group D	5005, Table IV	End points, Gp. A, Subgp. 1, every 6 months

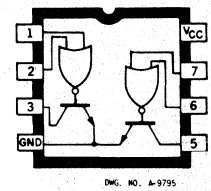
SERIES UDN-3600M DUAL 2-INPUT PERIPHERAL and POWER DRIVERS



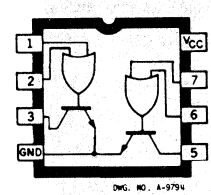
Type UDN-3611M
Dual AND Driver



Type UDN-3612M
Dual NAND Driver



Type UDN-3613M
Dual OR Driver



Type UDN-3614M
Dual NOR Driver

FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Sustaining Voltage of 80 V
- Pin-for-Pin Replacement for Series LM3600N
- Pin-for-Pin Replacement for SN75451BP thru SN75454BP and 75461 thru 75464

Description

These "mini-DIP" dual 2-input peripheral and power drivers are bi-polar monolithic integrated circuits incorporating AND, NAND, OR, or NOR logic gates, and high-current switching transistors on the same chip. The two output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, these drivers will sustain at least 80 V.

Applications

The Series UDN-3600M dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, heaters, and other non-inductive loads of up to 600 mA (both drivers in parallel).

With appropriate external diode transient suppression, the Series UDN-3600M drivers can also be used with inductive loads such as relays, solenoids, **and stepping motors. Similar devices with integral transient suppression are the series UDN-5700M.**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{in}	30 V
Output Off-State Voltage, V_{off}	80 V
Output On-State Sink Current, I_{on}	600 mA
Suppression Diode Off-State Voltage, V_{off}	80 V
Suppression Diode On-State Current, I_{on}	600 mA
Operating Free-Air Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_S	−55°C to +150°C
Power Dissipation, P_D	1.5 W
Each Driver	0.8 W
Derating Factor Above 25°C	12.5 mW/°C or 80°C/W

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC}):	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+70	°C
Current into any output (ON state)			300	mA

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current	$I_{in(0)}$		MAX	0.4 V	30 V			50	100	μA	2
"1" Input Current	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS: V_{CC} = 5.0V, T_A = 25°C

Characteristic	Symbol	Test Conditions	Limits				Notes
			Min.	Typ.	Max.	Units	
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

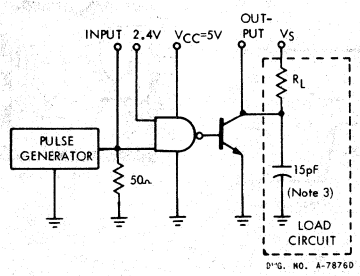
INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

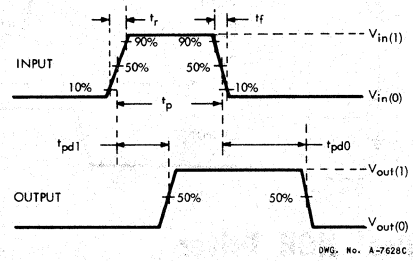
Type UDN-3611M Dual AND Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

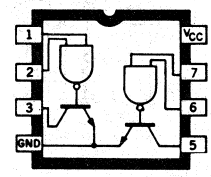
Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	150 mA		0.35	0.5	V	
			MIN	0.8 V	V_{CC}	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			35	49	mA	1, 2



DWG. NO. A-7876D



DWG. No. A-7628C

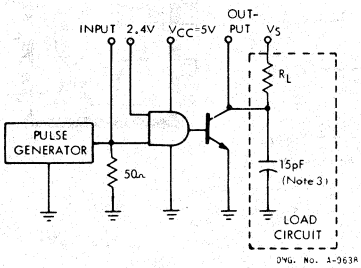


DWG. NO. A-6792

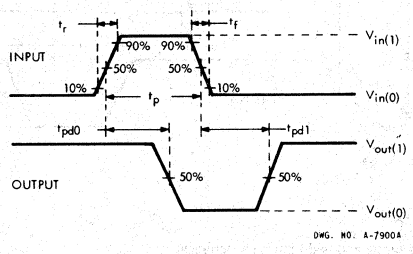
Type UDN-3612M Dual NAND Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	2.0 V	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	14	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	53	mA	1, 2



DWG. NO. A-9638



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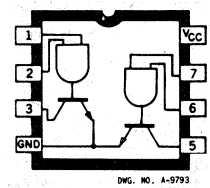


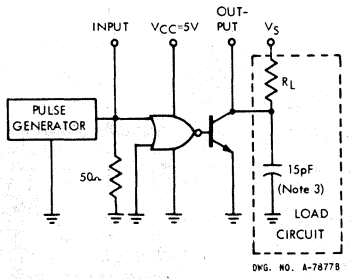
DWG. NO. A-9793

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

Type UDN-3613M Dual OR Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	150 mA		0.35	0.5	V	
			MIN	0.8 V	0.8 V	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			36	50	mA	1, 2



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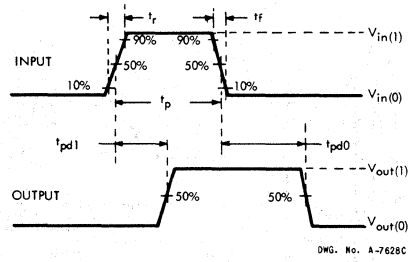

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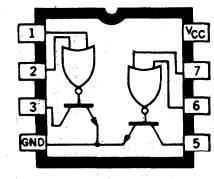
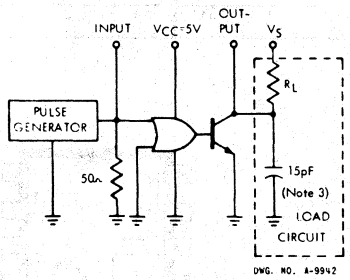


DWG. NO. A-9795

Type UDN-3614M Dual NOR Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	0 V	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	50	mA	1, 2



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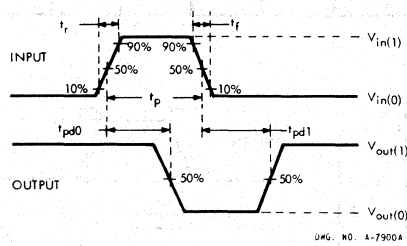

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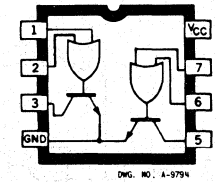
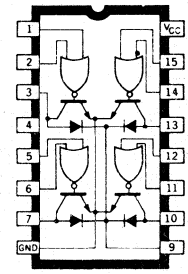


DWG. NO. A-9794

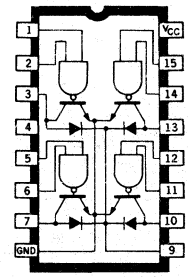
NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

SERIES UDN-5700A QUAD 2-INPUT PERIPHERAL and POWER DRIVERS

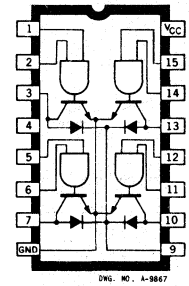
— TRANSIENT PROTECTED OUTPUTS



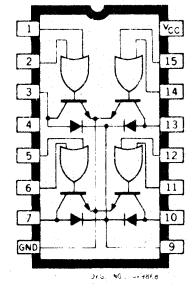
Type UDN-5703A
Quad OR Driver



Type UDN-5706A
Quad AND Driver



Type UDN-5707A
Quad NAND Driver



Type UDN-5733A
Quad NOR Driver

FEATURES:

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Sustaining Voltage of 80 V

Description

These 16-lead quad 2-input peripheral and power drivers are bi-polar monolithic integrated circuits incorporating AND, NAND, OR, and NOR logic gates, high-current switching transistors, and transient suppression diodes on the same chip. The four output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, these drivers will sustain at least 80 V.

Applications

The Series UDN-5700A quad drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

The integral transient suppression diodes allow their use with inductive loads such as relays, solenoids, or stepping motors without the need for discrete diodes. For non-inductive loads, the diode common buss can be used as a convenient lamp test.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{in}	30 V
Output Off-State Voltage, V_{off}	80 V
Output On-State Sink Current, I_{on}	600 mA
Suppression Diode Off-State Voltage, V_{off}	80 V
Suppression Diode On-State Current, I_{on}	600 mA
Operating Free-Air Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_S	−55°C to +150°C
Power Dissipation, P_D	2.0 W
Each Driver	0.8 W
Derating Factor Above 25°C	16.67 mW/°C or 60°C/W

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC}):	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+70	°C
Current into any output (ON state)			300	mA

ELECTRICAL CHARACTERISTICS (over operating temperature range unless otherwise noted)

		Test Conditions					Limits				
Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current	$I_{in(0)}$		MAX	0.4 V	30 V			50	100	μA	2
"1" Input Current	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS: V_{CC} = 5.0V, T_A = 25°C

			Limits				
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

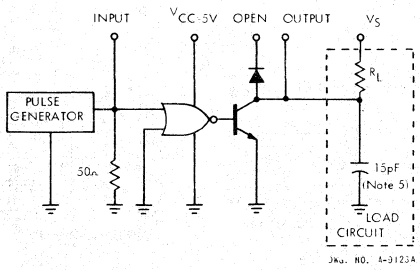
INPUT PULSE CHARACTERISTICS

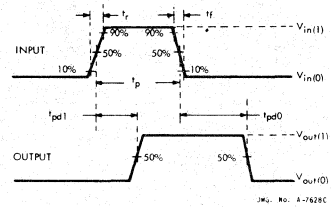
$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

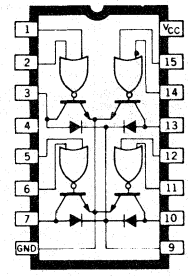
Type UDN-5703A Quad OR Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	150 mA		0.35	0.5	V	
			MIN	0.8 V	0.8 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			16	25	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			72	100	mA	1, 2



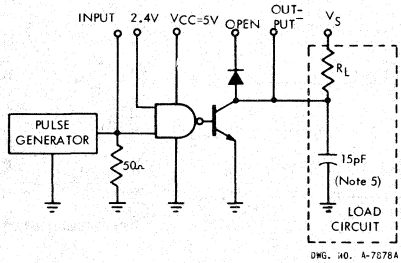


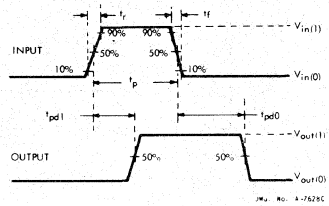


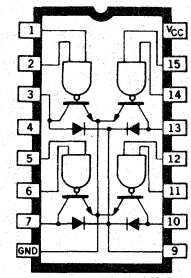
Type UDN-5706A Quad AND Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	150 mA		0.35	0.5	V	
			MIN	0.8 V	V_{CC}	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			16	24	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			70	98	mA	1, 2





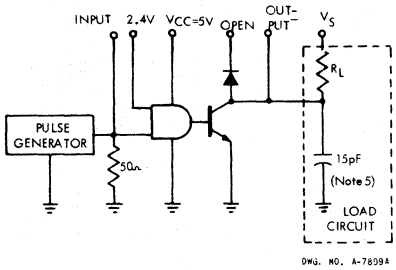


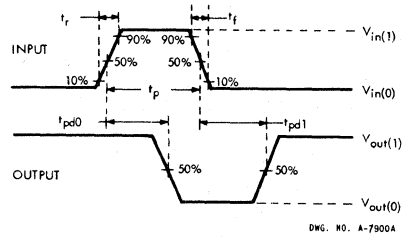
NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

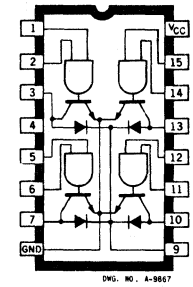
Type UDN-5707A Quad NAND Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	2.0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			80	106	mA	1, 2



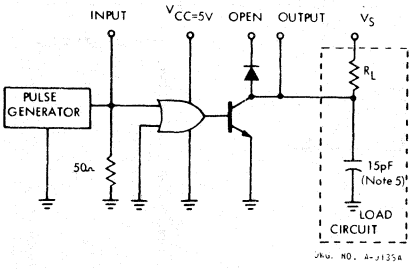


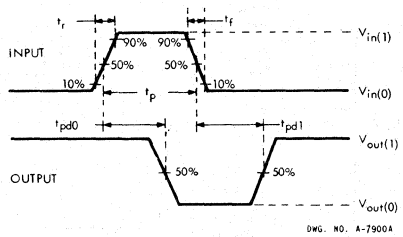


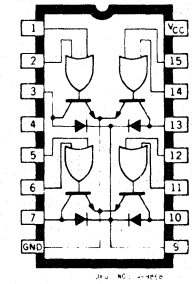
Type UDN-5733A Quad NOR Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			80	100	mA	1, 2



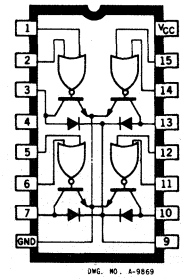




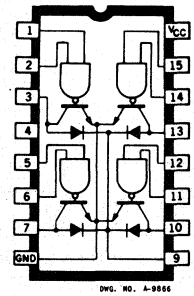
NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

SERIES UDS-5700H QUAD 2-INPUT PERIPHERAL and POWER DRIVERS -- Hermetically-Sealed

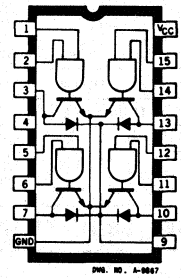
- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Sustaining Voltage of 80 V
- Hermetically Sealed Package to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B



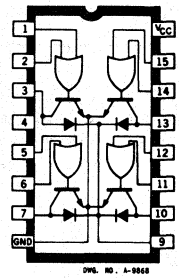
Type UDS-5703H
Quad OR Driver



Type UDS-5706H
Quad AND Driver



Type UDS-5707H
Quad NAND Driver



Type UDS-5733H
Quad NOR Driver

2

Description

These 16-Lead quad 2-input peripheral and power drivers are bi-polar monolithic integrated circuits incorporating AND, NAND, OR, and NOR logic gates, high-current switching transistors, and transient suppression diodes on the same chip. The four output transistors are capable of simultaneously sinking 150 mA continuously at an ambient temperature of +70°C. In the OFF state, these drivers will sustain at least 80 V.

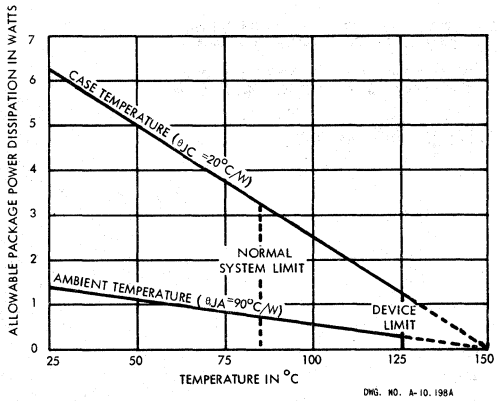
Applications

The Series UDS-5700H quad drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

The integral transient suppression diodes allow their use with inductive loads such as relays, solenoids, or stepping motors without the need for discrete diodes. For non-inductive loads, the diode common buss can be used as a convenient lamp test.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{in}	30 V
Output Off-State Voltage, V_{off}	80 V
Output On-State Sink Current, I_{on}	600 mA
Suppression Diode Off-State Voltage, V_{off}	80 V
Suppression Diode On-State Current, I_{on}	600 mA
Power Dissipation, P_D	1.0 W
Package Power Dissipation, P_D	See Graph
Ambient Temperature Range (operating), T_A	−55°C to +125°C
Storage Temperature Range, T_S	−65°C to +150°C



RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into any output (ON state)	—	—	300	mA

ELECTRICAL CHARACTERISTICS (over operating temperature range unless otherwise noted)

		Test Conditions					Limits				
Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.7	V	
"0" Input Current	$I_{in(0)}$		MAX	0.4 V	30 V			50	100	μA	2
"1" Input Current	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS: V_{CC} = 5.0V, T_A = 25°C

			Limits				
Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		300	750	ns	3

NOTES:

1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

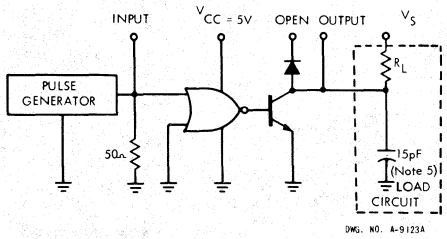
INPUT PULSE CHARACTERISTICS

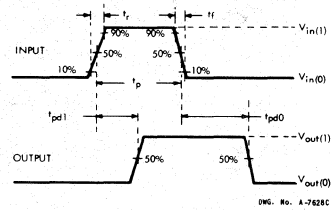
$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

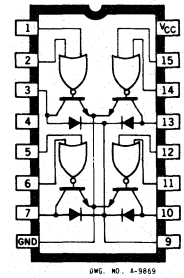
Type UDS-5703H Quad OR Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	150 mA		0.4	0.5	V	
			MIN	0.8 V	0.8 V	300 mA		0.6	0.8	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			16	25	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			72	100	mA	1, 2





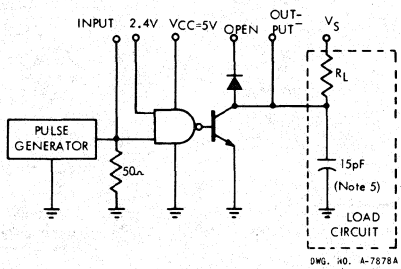


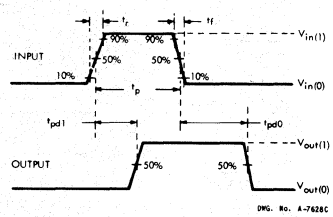
2

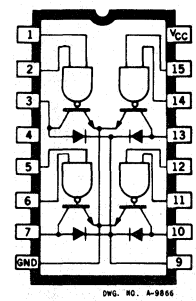
Type UDS-5706H Quad AND Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	150 mA		0.4	0.5	V	
			MIN	0.8 V	V_{CC}	300 mA		0.6	0.8	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			16	24	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			70	98	mA	1, 2





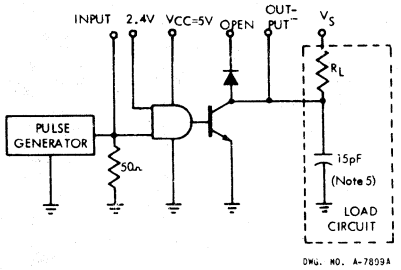


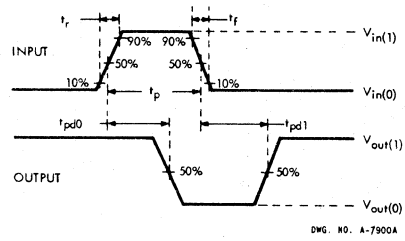
NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

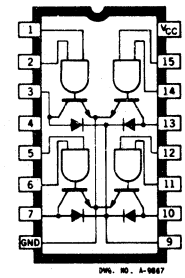
Type UDS-5707H Quad NAND Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	150 mA		0.4	0.5	V	
			MIN	2.0 V	2.0 V	300 mA		0.6	0.8	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			80	106	mA	1, 2



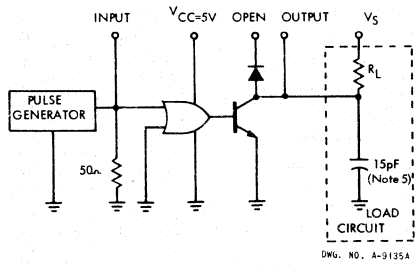


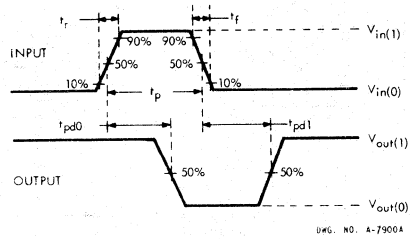


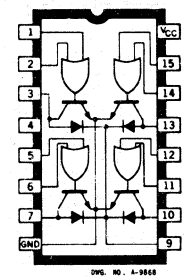
Type UDS-5733H Quad NOR Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	150 mA		0.4	0.5	V	
			MIN	2.0 V	0 V	300 mA		0.6	0.8	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			80	100	mA	1, 2







NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

POWER DRIVERS WITH MIL-STD-883 HIGH-RELIABILITY SCREENING

Power drivers with high-reliability screening can be ordered by adding the suffix 'MIL' to the part number, for example, UDS-5703H-MIL. If marking with the customer's part number is necessary in place of the Sprague Electric part number, this must be stated on the purchase order with the marking desired.

Table I - 100% Production Screen Tests (All Hermetic Parts) MIL-STD-883, Method 5004, Class B, Paragraphs 3.1.1 thru 3.1.6

Screen	MIL-STD-883 Test Method	Conditions
Internal Visual	2010, Cond. B	—
Stabilization Bake	1008, Cond. C	150°C, 24 Hours
Thermal Shock	1011, Cond. A	0 to 100°C, 15 Cycles
Constant Acceleration	2001, Cond. E	30,000 G's, Y1 Plane
Fine Seal	1014, Cond. A	5×10^{-7} Maximum
Gross Seal	1014, Cond. C	—
Electrical	—	Per Specification
Marking	—	Sprague or customer part number, date code, lot identification, index point

Table II - 100% High-Reliability Screening ("MIL" Suffix Parts Only) MIL-STD-883, Method 5004, Class B, Paragraphs 3.1.9 thru 3.1.15 & 3.1.18

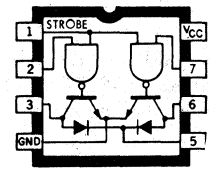
Screen	MIL-STD-883 Test Method	Conditions
Interim Electrical	5005, Gp A, Subgp 1	25°C per Specification
Burn-In	1015, Cond. A	125°C, 160 Hours
Static Electrical	5005, Gp A, Subgp 1	25°C per Specification
	5005, Gp A, Subgp 2 & 3	−55°C & +125°C per Specification
Dynamic & Functional Electrical	5005, Gp A, Subgp 4, 7 & 9	25°C per Specification
Fine Seal	1014, Cond. A	5×10^{-7} Maximum
Gross Seal	1014, Cond. C	—
External Visual	2009	—

Table III - High-Reliability Qualification and Quality Conformance Inspection MIL-STD-883, Method 5004, Class B, Paragraph 3.1.17

Test	MIL-STD-883 Test Method	Description
Group A Subgp. 1-4, 7 & 9	5005, Table I	Each production lot
Group B	5005, Table II	Each production lot
Group C	5005, Table III	End points, Gp. A, Subgp. 1, every 90 days
Group D	5005, Table IV	End points, Gp. A, Subgp. 1, every 6 months

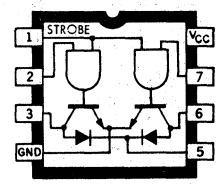
SERIES UDN-5700M DUAL PERIPHERAL and POWER DRIVERS

— TRANSIENT PROTECTED OUTPUTS



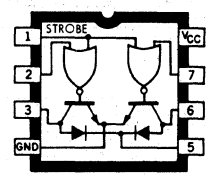
DWG. NO. A-9791

Type UDN-5711M
Dual AND Driver



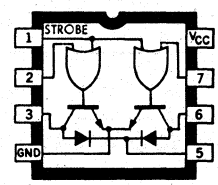
DWG. NO. A-9790

Type UDN-5712M
Dual NAND Driver



DWG. NO. A-9789

Type UDN-5713M
Dual OR Driver



DWG. NO. A-9788

Type UDN-5714M
Dual NOR Driver

FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Sustaining Voltage of 80 V

Description

These "mini-DIP" dual peripheral and power drivers are bi-polar monolithic integrated circuits incorporating AND, NAND, OR, or NOR logic gates, high-current switching transistors, and transient suppression diodes on the same chip. The two output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, these drivers will sustain at least 80 V.

Applications

The Series UDN-5700M dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters with a load current of up to 600 mA.

The integral transient suppression diodes allow the use of these drivers with inductive loads such as relays, solenoids, or stepping motors without the need for discrete diodes. When not required for transient suppression, the diode common bus can be used to perform the "lamp test" function. **Similar devices with four drivers per package are the Series UDN-5700A.**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	7.0 V
Input Voltage, V_{in}	30 V
Output Off-State Voltage, V_{off}	80 V
Output On-State Sink Current, I_{on}	600 mA
Suppression Diode Off-State Voltage, V_{off}	80 V
Suppression Diode On-State Current, I_{on}	600 mA
Operating Free-Air Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_S	−55°C to +150°C
Power Dissipation, P_D	1.5 W
Each Driver	0.8 W
Derating Factor Above 25°C	12.5 mW/°C or 80°C/W

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC}):	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+70	°C
Current into any output (ON state)			300	mA

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current at all Inputs except Strobe	$I_{in(0)}$		MAX	0.4 V	30 V			50	100	μA	2
"0" Input Current at Strobe	$I_{in(0)}$		MAX	0.4 V	30 V			100	200	μA	
"1" Input Current at all Inputs except Strobe	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
"1" Input Current at Strobe	$I_{in(1)}$		MAX	30 V	0 V				20	μA	2
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS: V_{CC} = 5.0V, T_A = 25°C

Characteristic	Symbol	Test Conditions	Limits				Notes
			Min.	Typ.	Max.	Units	
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

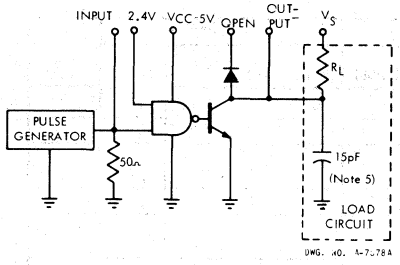
INPUT PULSE CHARACTERISTICS

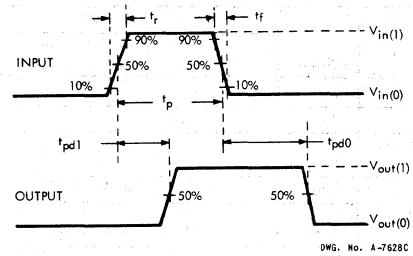
$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

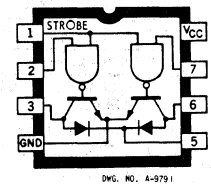
Type UDN-5711M Dual AND Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	150 mA		0.35	0.5	V	
			MIN	0.8 V	V_{CC}	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			35	49	mA	1, 2



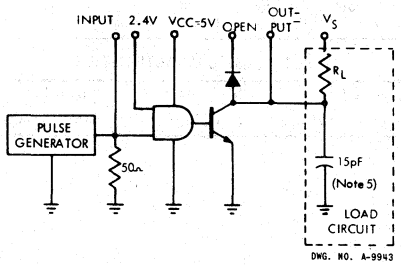


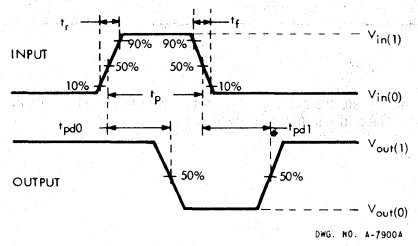


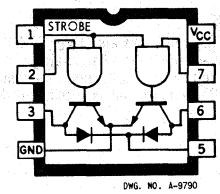
Type UDN-5712M Dual NAND Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	2.0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	4
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	5
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	53	mA	1, 2







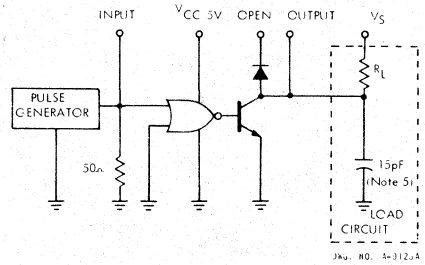
NOTES:

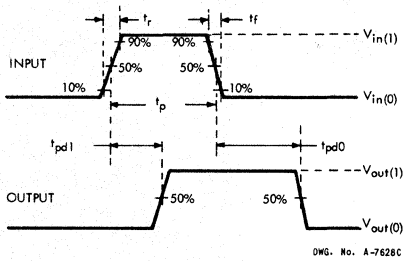
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA
5. Capacitance values specified include probe and test fixture capacitance.

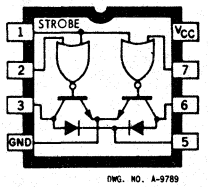
Type UDN-5713M Dual OR Driver

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	150 mA		0.35	0.5	V	
			MIN	0.8 V	0.8 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			36	50	mA	1, 2





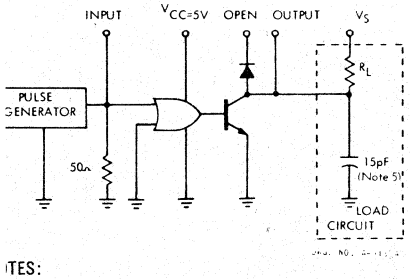


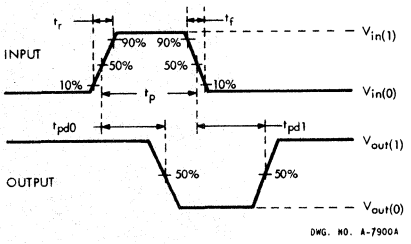
2

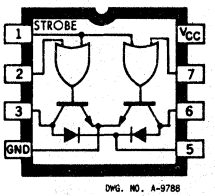
Type UDN-5714M Dual NOR Driver

LECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	50	mA	1, 2







NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

THE UDN-5733A QUAD 2-INPUT POWER DRIVER IS SHOWN ON PAGE 2-26.

THE UDS-5733H HERMETICALLY-SEALED POWER DRIVER IS SHOWN ON PAGE 2-30.

UDS-5790H and UDS-5791H QUAD PIN DIODE POWER DRIVERS

FEATURES

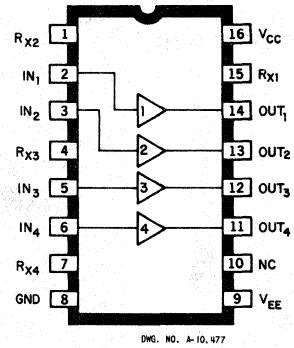
- Inverting or Non-Inverting
- Low Input Current
- TTL, DTL, MOS Compatible
- Wide Operating Voltage Range
- High Output Breakdown Voltage

CONSISTING of four high-voltage NPN output stages and associated logic and level shifting, these monolithic, planar integrated circuits offer an easy solution to many PIN diode driving applications.

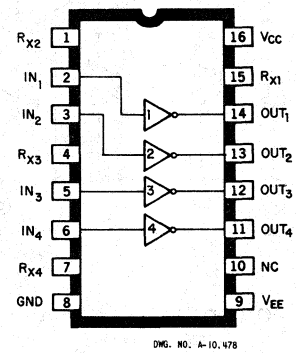
The UDS-5790H and UDS-5791H quad power drivers are designed to replace discrete or hybrid PIN diode drivers. They provide significant reductions in cost and space with improved reliability. The UDS-5790H driver uses a grounded-base input stage for non-inverting operation while the UDS-5791H driver uses a common-emitter input stage for inverting operation. Both devices are capable of sustaining OFF voltages of 120V and will switch currents to 500 mA.

The input buffer circuitry has been designed to utilize external discrete resistors. The one-resistor-per-driver effectively reduces total package power dissipation and junction temperature while allowing user selection of output base drive current, power supply voltages, and output current.

All devices are rated for operation over an extended temperature range of −55°C to +125°C. They are customarily supplied in 16-pin hermetic dual in-line packages. All units are subjected to the 100% production screen tests specified in MIL-STD-883, Method 5004, Class B, paragraphs 3.1.1 through 3.1.6. On special order, 160 hours of burn-in to Method 1015, Condition A, can also be performed.



UDS-5790H



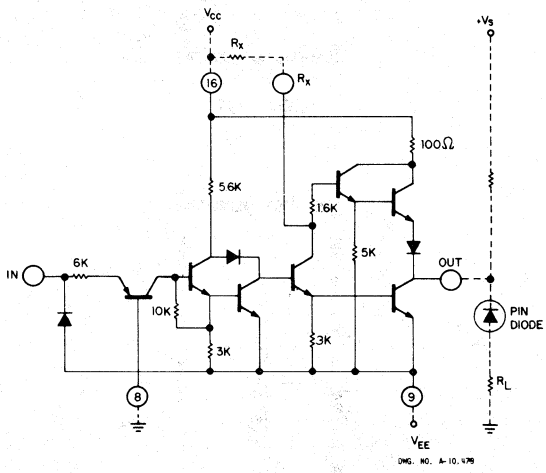
UDS-5791H

2

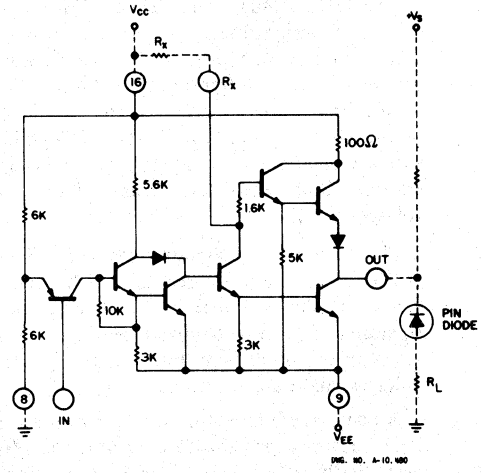
ABSOLUTE MAXIMUM RATINGS over free-air operating temperature range

Supply Voltage, V_{CC} ..... +6.0 V
Supply Voltage, V_{EE} ..... −6.0 V
Input Voltage, V_{IN} ..... V_{CC}
Output OFF-State Voltage, V_{OFF} (ref. V_{EE}) ..... +120 V
Output ON-State Current, I_{ON} ..... 500 mA
Package Power Dissipation, P_D ..... See Graph
Operating Ambient Temperature Range, T_A ..... −55°C to +125°C
Storage Temperature Range, T_S ..... −65°C to +150°C

PARTIAL SCHEMATICS



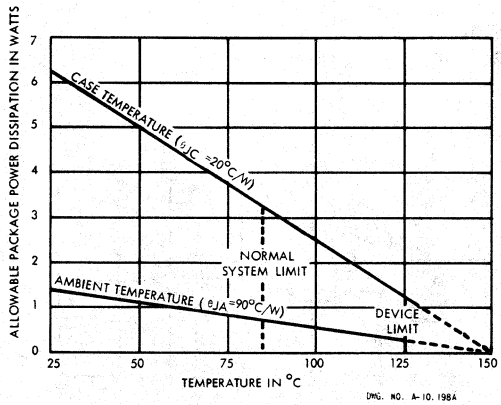
ONE OF FOUR DRIVERS
UDS-5790H



ONE OF FOUR DRIVERS
UDS-5791H

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	4.5	5.0	5.5	V
Supply Voltage, V_{EE}	−1.5	−3.0	−5.5	V
Output ON-State Current, I_{ON}			300	mA
Operating Ambient Temperature Range, T_A	−55	+85	+125	°C



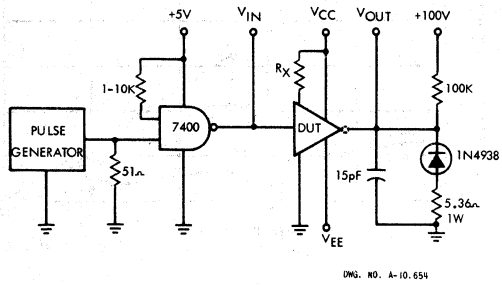
2

STATIC ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp. °C	V_{CC} +V	V_{EE} −V	V_{IN} +V	V_{OFF} or I_{ON} +V	mA	R_X Ω	Limits Min.	Max.	Units	Notes
"1" Input Voltage	$V_{IN(1)}$		4.5						2.0	4.0	V	
"0" Input Voltage	$V_{IN(0)}$		4.5						—	0.8	V	
"1" Input Current	$I_{IN(1)}$		5.5	3.0	5.0				—	1.0	mA	1
			5.5	3.0	5.0				—	50	μA	2
"0" Input Current	$I_{IN(0)}$		5.5	3.0	0.4				—	50	μA	1
			5.5	3.0	0.4				—	1.0	mA	2
OFF-State Reverse Current	I_{OFF}	+25	4.5	3.0		115			—	50	μA	3
		+125	4.5	3.0		115			—	100	μA	3
ON-State Output Voltage (ref. V_{EE})	V_{ON}	−55	4.5	1.5			150	720	—	400	mV	4, 5
							300	360	—	600	mV	4, 5
		+85	4.5	1.5			150	720	—	400	mV	4, 5
							300	360	—	700	mV	4, 5
		+125	4.5	1.5			150	720	—	500	mV	4, 5
							300	360	—	850	mV	4, 5
Predriver Collector Voltage (ref. V_{EE})	V_X		4.5	1.5			150	720	—	1.3	V	4, 5
							300	360	—	1.5	V	4, 5
Output Short-Circuit Current	I_{OS}		4.5	3.0		−2.3		510	20	50	mA	3, 5
OFF-State Supply Current	I_{CC}		5.5	5.5					—	3.4	mA	3
ON-State Supply Current	I_{CC}		5.5	5.5					—	4.1	mA	4
Turn-On Delay	t_{on}	—	5.0	3.0	—	—	—	510	—	500	nS	
Storage Delay	t_s	—	5.0	3.0	—	—	—	510	—	5.0	μS	
Fall Time	t_f	—	5.0	3.0	—	—	—	510	—	100	nS	

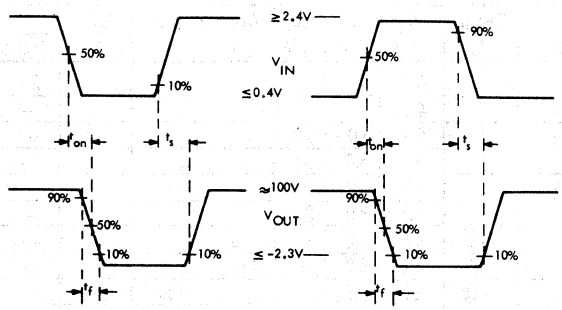
NOTES:
1. Type UDS-5790H only.
2. Type UDS-5791H only.
3. V_{IN} = 2.4 V for UDS-5790H or 0.4 V for UDS-5791H.
4. V_{IN} = 0.4 V for UDS-5790H or 2.4 V for UDS-5791H.
5. Each output tested separately.

SWITCHING TEST CIRCUIT AND WAVEFORMS



DWG. NO. A-10.654

UDS-5790H **UDS-5791H**



DWG. NO. A-10.655

GENERAL DESIGN NOTES

$$I_{RX} = \frac{I_{ON}}{B}$$

$$R_X = \frac{B\,(V_{CC} - V_{EE} - V_X)}{I_{ON}}$$

where

$B = 30$, the minimum output current gain over the operating temperature range

$V_X = 1.5$, the maximum predriver voltage

It is recommended that a minimum overdrive of 25% to be used ($1.25\ I_{RX}$ or 0.8_{RX}).

POWER DRIVERS WITH MIL-STD-883 HIGH-RELIABILITY SCREENING

Power drivers with high-reliability screening can be ordered by adding the suffix "MIL" to the part number, for example, UDS-5790H-MIL. If marking with the customers part number is necessary in place of the Sprague Electric part number, this must be stated on the purchase order with the marking desired.

Table I – 100% Production Screen Tests (All Hermetic Parts) MIL-STD-883, Method 5004, Class B, Paragraphs 3.1.1 thru 3.1.6

Screen	MIL-STD-883 Test Method	Conditions
Internal Visual	2010, Cond. B	—
Stabilization Bake	1008, Cond. C	150°C, 24 Hours
Thermal Shock	1011, Cond. A	0 to 100°C, 15 Cycles
Constant Acceleration	2001, Cond. E	30,000 G's, Y1 Plane
Fine Seal	1014, Cond. A	5 x 10^{-7} Maximum
Gross Seal	1014, Cond. C	—
Electrical	—	Per Specification
Marking	—	Sprague or customer part number, date code, lot identification, index point

Table II – 100% High-Reliability Screening ("MIL" Suffix Parts Only) MIL-STD-883, Method 5004, Class B, Paragraphs 3.1.9 thru 3.1.15 & 3.1.18

Screen	MIL-STD-883 Test Method	Conditions
Interim Electrical	5005, Gp A, Subgp 1	25°C per Specification
Burn-In	1015, Cond. A	125°C, 160 Hours
Static Electrical	5005, Gp A, Subgp 1	25°C per Specification
	5005, Gp A, Subgp 2 & 3	−55° & +125°C per Specification
Dynamic & Functional Electrical	5005, Gp A, Subgp 4, 7 & 9	25°C per Specification
Fine Seal	1014, Cond. A	5 x 10^{-7} Maximum
Gross Seal	1014, Cond. C	—
External Visual	2009	—

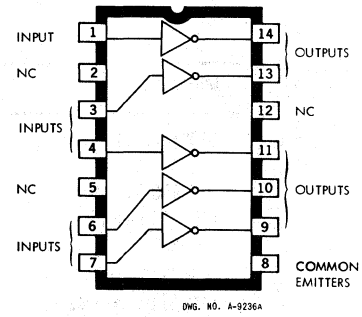
Table III – High-Reliability Qualification and Quality Conformance Inspection MIL-STD-883, Method 5004, Class B, Paragraph 3.1.17

Test	MIL-STD-883 Test Method	Description
Group A Subgp. 1-4, 7 & 9	5005, Table I	Each production lot
Group B	5005, Table II	Each production lot
Group C	5005, Table III	End points, Gp. A, Subgp. 1, every 90 days
Group D	5005, Table IV	End points, Gp. A, Subgp. 1, every 6 months

Device Type	Data	Applications	Thermal
UHP-480 and 481	3–2	7–4	1E
UHP-482	3–2		1D
UHD-490 and 491	3–5		4B
UHP-490 and 491	3–5	7–4	1E
UHP-495	3–7		1E
UDN-6116A and 6116A-2	3–9		1E
UDN-6116R and 6116R-2	3–9		3B
UDN-6118A and 6118A-2	3–9	7–10	1D
UDN-6118R and 6118R-2	3–9		3A
UDN-6126A and 6126A-2	3–9		1E
UDN-6126R and 6126R-2	3–9		3B
UDN-6128A and 6128A-2	3–9	7–10	1D
UDN-6128R and 6128R-2	3–9		3A
UDN-6144 and 6164A	3–13	7–4, 27	1E
UDN-6184A	3–13		1D
UDN-7180 thru 7186A	3–17	7–3, 27	1D

Device Type	I_{OUT}	V_{OUT}	Outputs
UHP-480	15 mA	130 V	Sink 5
UHP-481	15 mA	130 V	Sink 7
UHP-482	15 mA	130 V	Sink 8
UH( )-490	−30 mA	−80 V	Source 5
UH( )-491	−30 mA	−80 V	Source 6
UHP-495	−30 mA	−80 V	Source 6
UDN-6116 and 6126A/R	−40 mA	85 V	Source 6
UDN-6116 and 6126A/R-2	−40 mA	65 V	Source 6
UDN-6118 and 6128A/R	−40 mA	85 V	Source 8
UDN-6118 and 6128A/R-2	−40 mA	65 V	Source 8
UDN-6144A	−70 mA	120 V	Source 4
UDN-6164A	−70 mA	120 V	Source 6
UDN-6184A	−70 mA	120 V	Source 8
UDN-7180A	20 mA	−120 V	Sink 8
UDN-7183A	3.25 mA	−120 V	Sink 8
UDN-7184A	2.0 mA	−120 V	Sink 8
UDN-7186A	1.0 mA	−120 V	Sink 8

SERIES UHP-480
HIGH-VOLTAGE DISPLAY DRIVERS



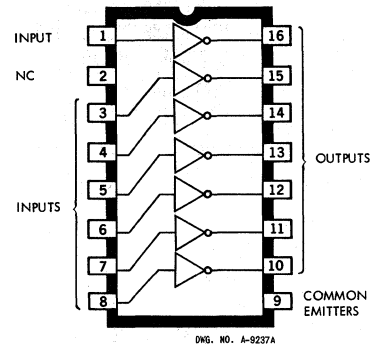
UHP-480
14-Lead Dual In-Line

FEATURES

- Reliable Monolithic Integrated Construction
- Low Output Leakage Current
- High-Voltage Output Capability
- Small Size
- 130 Volt Breakdown

Description

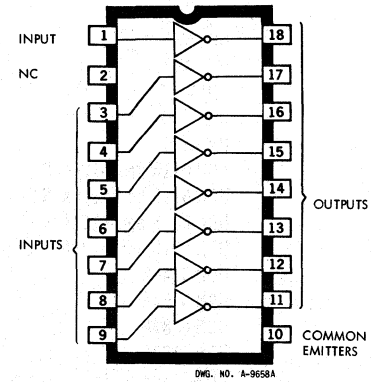
The Series UHP-480 high-voltage display drivers are bipolar monolithic integrated circuits designed for interface between MOS or open collector TTL logic and gas discharge displays such as the Burroughs Panaplex®, the Cherry Plasma-Lux and the Beckman SP Series. These drivers replace the major portion of discrete components typically required to interface between an MOS calculator or counter/decoder circuit and the gas discharge display. They are high-voltage switches intended for use in the cathode portion of the display and are available with either 5 (UHP-480), 7 (UHP-481), or 8 (UHP-482) switches per dual in-line package.



UHP-481
16-Lead Dual In-Line

Applications

The Series UHP-480 devices may be used in gas discharge applications which include calculators, DVM's, DMM's, DPM's, mini-computers, clocks, etc. Their high reliability coupled with small size make them an excellent choice for those applications where space is at a premium.



UHP-482
18-Lead Dual In-Line

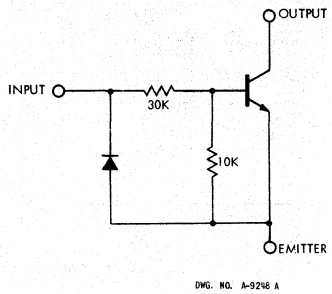
ABSOLUTE MAXIMUM RATINGS

Output Voltage	130V
Output Sink Current	15mA
Input Voltage	30V
Diode Forward Current	50mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS @ T_A = 25°C unless otherwise specified

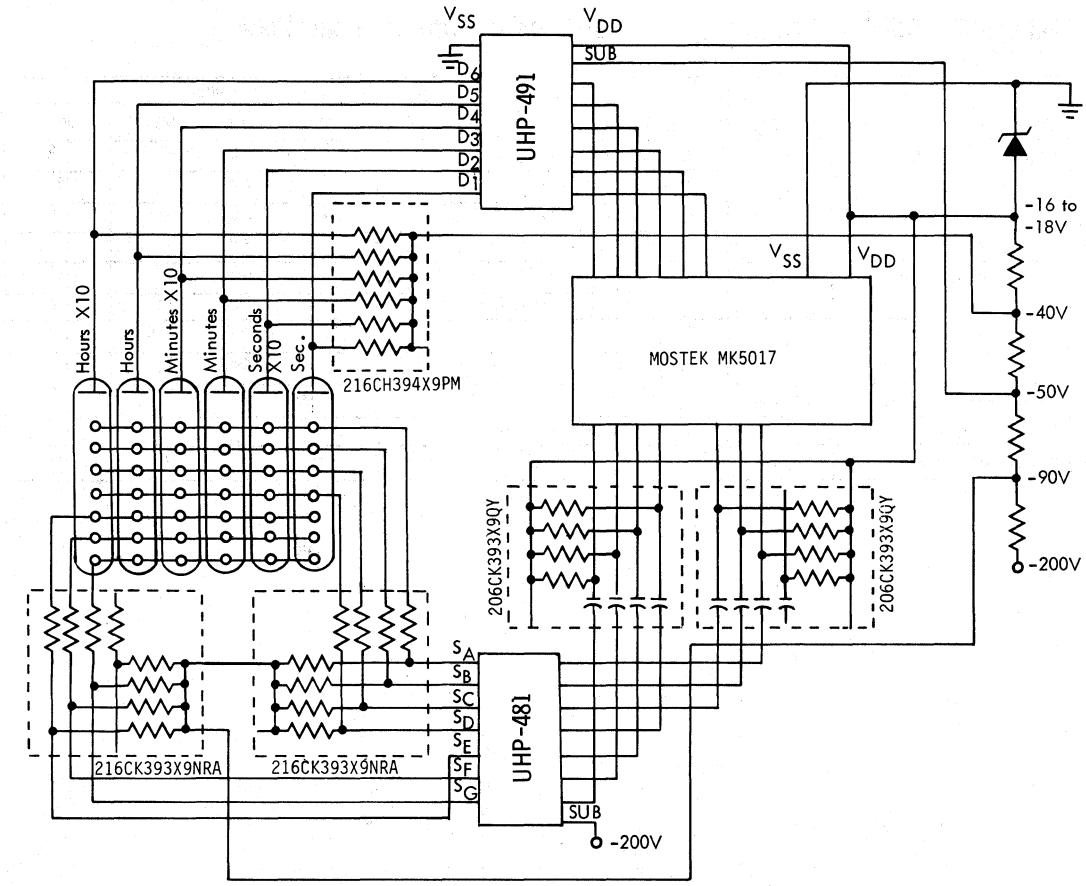
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Sink Current	I_{OUT}	V_{IN} = 4V, V_{CE} = 5V	2.0	5.5	—	mA
		V_{IN} = 5V, V_{CE} = 5V	3.0	7.0	—	mA
		V_{IN} = 6V, V_{CE} = 5V	4.0	8.0	—	mA
		V_{IN} = 7V, V_{CE} = 5V	5.0	9.0	—	mA
Output Leakage Current	I_{CEX}	V_{IN} = 0V, V_{CE} = 130V	—	0.2	1.5	μA
		V_{IN} = 0V, V_{CE} = 130V, T_A = 70°C	—	1.5	15	μA
Input Current	I_{IN}	V_{IN} = 7V	—	200	350	μA
		V_{IN} = 15V	—	490	700	mA
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 5.5mA, V_{IN} = 9V	—	1.3	2.5	V
Turn-on Delay Time	T_{PHL}	R_L = 56kΩ, V_{CC} = 130V	—	2	5	μs
Turn-off Delay Time	T_{PLH}	R_L = 56kΩ, V_{CC} = 130V	—	2	5	μs

3



UHP-480, 481, and 482 (1 Driver)

Due to the high input impedance of these devices, they are susceptable to static discharge damage sometimes associated with handling and testing. Therefore, techniques similar to those used for handling MOS devices should be employed. (See Page 5-2).



Type 206C and 216C are single in-line networks

DWG. NO. A-9413A

TYPICAL CLOCK APPLICATION

SERIES 490 and 491
HIGH-VOLTAGE DISPLAY DRIVERS

FEATURES

- Reliable Monolithic Integrated Construction
- Low Output Leakage Currents
- High Output Breakdown Voltages
- Small Size

Description

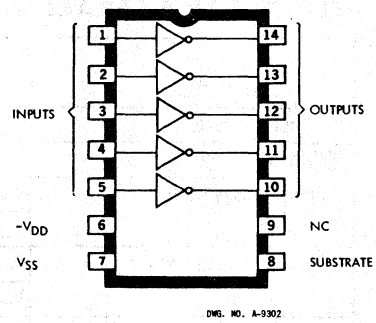
The Series 490 and 491 high-voltage display drivers are bipolar monolithic integrated circuits designed for interfacing MOS or other low-voltage circuitry with high-voltage gas discharge displays or loads. These drivers replace most of the discrete components normally required to drive multiplexed gas discharge displays from MOS calculator or clock circuits. The Series 490 and 491 high-voltage display drivers are intended for use in the anode portion of the display and are available with either 5 (Series 490) or 6 (Series 491) drivers per dual in-line package.

Applications

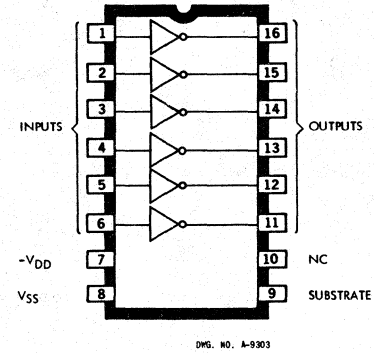
The Series 490 and 491 may be used in a variety of low-voltage to high-voltage interfacing applications such as are found in MOS calculators, digital clocks, etc. Their high reliability and small size make them an excellent choice for those applications where space is at a premium.

Packages

Package	Part Number	Drivers/ Package
14-Lead Hermetic Dual In-line	UHD-490	5
14-Lead Plastic Dual In-line	UHP-490	5
16-Lead Hermetic Dual In-line	UHD-491	6
16-Lead Plastic Dual In-line	UHP-491	6



UHD-490
UHP-490



UHD-491
UHP-491

3

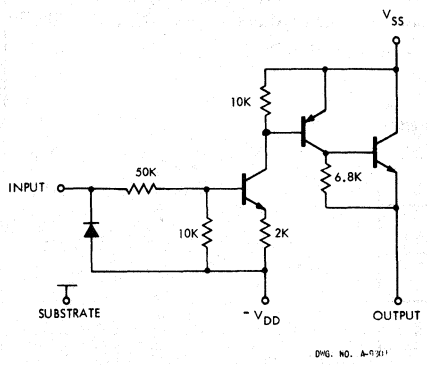
ABSOLUTE MAXIMUM RATINGS
(referenced to V_{SS})

Output Voltage ..... −80V
Output Source Current 30mA
V_{DD} Supply Voltage ..... −30V
Input Voltage ..... −30V
Input Diode Forward Current 20mA
Operating Temperature Range:
UHP-490, UHP-491 ..... 0°C to +70°C
UHD-490, UHD-491 ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C

Note: The substrate pin must be connected to a voltage potential equal to or greater than the most negative operating voltage applied to the device.

ELECTRICAL CHARACTERISTICS @ T_A = 25°C (unless otherwise specified)

Characteristic	Test Conditions	Limits		
		Min.	Max.	Units
"1" Input Voltage		—	V_{DD}+2.5	V
"0" Input Voltage		V_{DD}+6	—	V
Output Leakage Current	V_{IN} = V_{DD}+2.5V, V_{SS} = 80V	—	1.5	μA
	V_{IN} = V_{DD}+2.5V, V_{SS} = 80V, T_A = 70°C	—	15	μA
Output Saturation Voltage	V_{IN} = V_{DD}+6V, I_{OUT} = 5mA	—	2	V
	V_{IN} = V_{DD}+6V, I_{OUT} = 15mA	—	5	V
Input Current	V_{IN} = V_{SS}, I_{OUT} = 15mA	—	400	μA
I_{DD} Supply Current	V_{IN} = V_{SS}, I_{OUT} = 15mA	—	2	mA
Input Diode Forward Voltage	I_D = 20mA	—	2	V
Turn-on Delay Time	R_L = 4kΩ	—	3	μs
Turn-off Delay Time	R_L = 4kΩ	—	5	μs



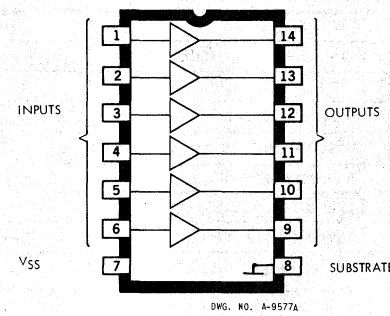
Series 490 and 491 (1 Driver)

Due to the high input impedance of these devices, they are susceptable to static discharge damage sometimes associated with handling and testing. Therefore, techniques similar to those used for handling MOS devices should be employed. (See Page 5-2).

TYPE UHP-495
HIGH-VOLTAGE DISPLAY DRIVERS

FEATURES

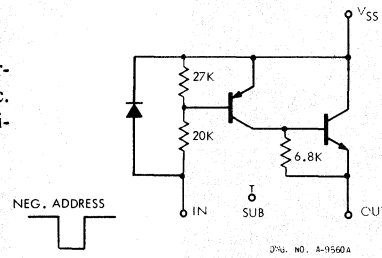
- Reliable Monolithic Integrated Construction
- Low Output Leakage Currents
- High Output Breakdown Voltages
- Small Size



THE TYPE UHP-495 High-Voltage Display Driver is a bipolar monolithic integrated circuit designed for interfacing MOS or other low-voltage circuitry with high-voltage gas discharge displays or loads. This driver replaces most of the discrete components normally required to drive multiplexed gas discharge displays from MOS calculator or clock circuits. The UHP-495 high voltage display driver is intended for use in the anode portion of the display and is available with 6 drivers per dual in-line package.

Applications

The UHP-495 may be used in a variety of low-voltage to high-voltage interfacing applications such as are found in MOS calculators, digital clocks, etc. Its high reliability and small size make it an excellent choice for those applications where space is at a premium.



Partial Schematic
One of Six Drivers

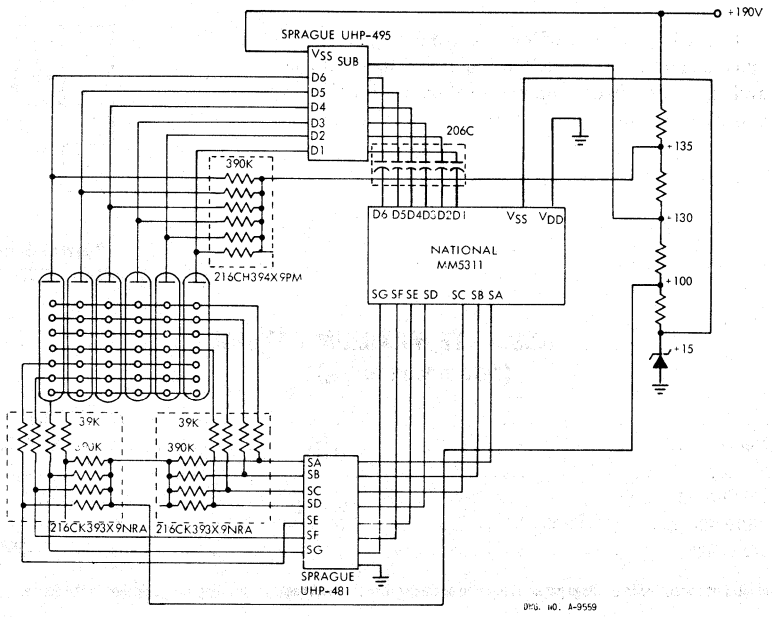
ABSOLUTE MAXIMUM RATINGS
(referenced to V_{SS})

Output Voltage	−80V
Output Source Current	30mA
Input Voltage	−30V
Input Diode Forward Current	20mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: The susbstrate pin must be connected to a voltage potential equal to or greater than the most negative operating voltage applied to the device.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{SS} = 0 V, V_{SUB} = −80 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Input Voltage	V_{IN}	I_{OUT} = 15 mA, $V_{OUT} \leqq -5$ V	—	−3.5	−6.0	V
Input Current	I_{IN}	V_{IN} = −12 V	400	600	850	μA
Output Saturation Voltage	$V_{CE(SAT)}$	V_{IN} = −6 V, I_{OUT} = 15 mA	—	2.0	5.0	V
Output Leakage Current	I_{CEX}	V_{OUT} = −80 V	—	—	1.5	μA
Substrate Current	I_{SUB}	V_{IN} = −6 V, I_{OUT} = 1 mA	—	—	1.5	mA
Substrate Leakage Current		V_{OUT} = 0 V, V_{SS} = open	—	0.4	1.5	μA
Diode Forward Voltage	V_F	I_F = 20 mA	—	1.6	2.0	V
Diode Breakdown Voltage	BV_R		30	50	—	V
Turn-on Delay Time	t_{PHL}	R_L = 6.8 kΩ	—	3.0	7.0	μs
Turn-off Delay Time	t_{PLH}	R_L = 6.8 kΩ	—	3.0	7.0	μs

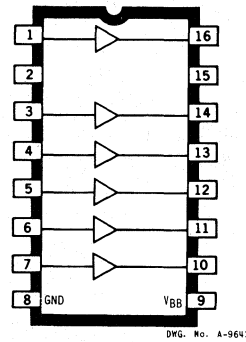


TYPICAL CLOCK APPLICATION

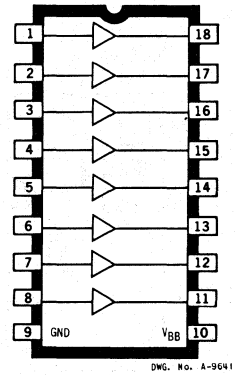
UDN-6116A, UDN-6118A, UDN-6126A, UDN-6128A
FLUORESCENT DISPLAY DRIVERS

FEATURES

- Digit or Segment Drivers
- Low Input Current
- Integral Output Pulldown Resistors
- Low Power
- Reliable Monolithic Construction
- High Output Breakdown Voltage



UDN-6116A
UDN-6126A



UDN-6118A
UDN-6128A

CONSISTING of six or eight NPN Darlington output stages and the associated common-emitter input stages, Type UDN-6116A, UDN-6118A, UDN-6126A and UDN-6128A display drivers are designed to interface between low-level digital logic and vacuum fluorescent displays. All devices are capable of driving the digits and/or segments of these displays and are designed to permit all outputs to be activated simultaneously. Pulldown resistors are incorporated into each output and no external components are required for most fluorescent display applications.

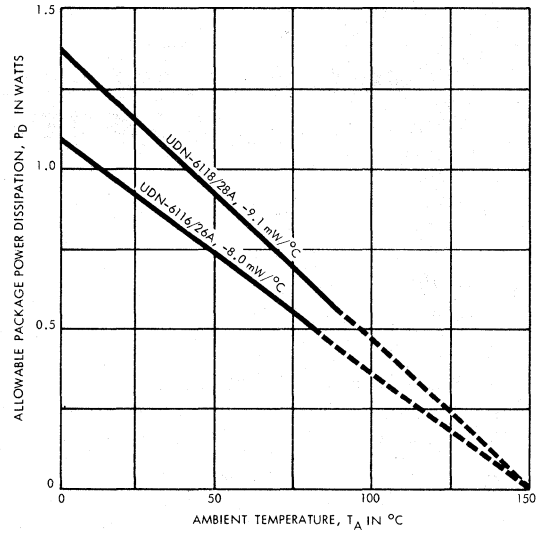
The Type UDN-6116A and UDN-6118A devices are compatible with TTL, Schottky TTL, DTL, and 5 volt CMOS. The Type UDN-6126A and UDN-6128A devices are intended for use with MOS (PMOS or CMOS) logic operating from supply voltages of 6 V to 15 V. With any device, the output load is activated when the input is pulled towards the positive supply (active 'high').

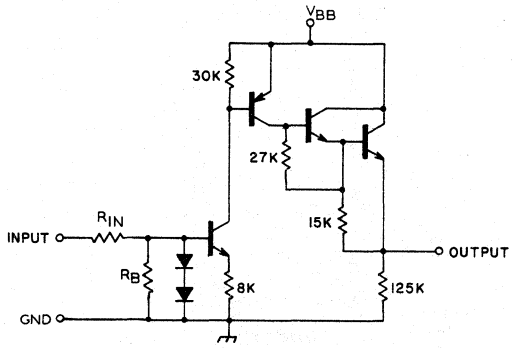
The standard UDN-6116A, UDN-6118A, UDN-6126A, and UDN-6128A display drivers are rated for continuous operation with supply voltages of up to 80 V. Lower-cost devices for operation at supply voltages of up to 60 V are specified by adding the suffix "−2" to the part number. All devices are normally supplied in dual in-line plastic packages. They can also be supplied, with reduced package power capability, in military-grade hermetic packages to the processing and environmental requirements of Military Standard MIL-STD-883, or industrial grade dual in-line hermetic packages. To order, change the last letter of the part number from "A" to "H" or "R", respectively.

ABSOLUTE MAXIMUM RATINGS at 25°C

Free-Air Temperature

Supply Voltage Range, V_{BB} (UDN-6116/18/26/28A) . . . . 5.0 V to 85 V
(UDN-6116/18/26/28A-2) . . . 5.0 V to 65 V
Output Voltage, V_{OUT} (UDN-6116/18/26/28A) . . . . . 85 V
(UDN-6116/18/26/28A-2) . . . . . 65 V
Input Voltage, V_{IN} . . . . . 20 V
Output Current, I_{OUT} . . . . . 40 mA
Power Dissipation, P_D . . . . . See Graph
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_S . . . . . −55°C to +150°C





DWG. NO. A-10,592A

TYPICAL STAGE

PARTIAL SCHEMATIC

ONE OF SIX DRIVERS (UDN-6116/26A)
ONE OF EIGHT DRIVERS (UDN-6118/28A)

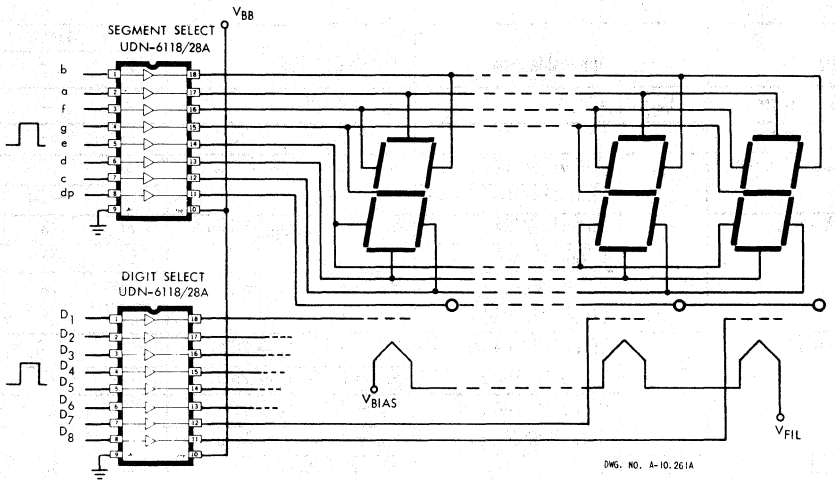
Type	R_{IN}	R_B
UDN-6116/18A	10 kΩ	30 kΩ
UDN-6126/28A	20 kΩ	20 kΩ

ELECTRICAL CHARACTERISTICS Over Operating Temperature Range; V_{BB} = 80 V For UDN-6116/18/26/28A, V_{BB} = 60 V For UDN-6116/18/26/28A-2 (Unless Otherwise Specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits			
				Min.	Typ.	Max.	Units
Output Leakage Current	I_{OUT}	All	V_{IN} = 0.4 V	–	–	15	μA
Output OFF Voltage	V_{OUT}	All	V_{IN} = 0.4 V, T_A = 25°C	–	–	1.0	V
Output Pulldown Current	I_{OUT}	UDN-6116/18/26/28A	Input Open, T_A = 25°C,	–500	–640	–900	μA
		UDN-6116/18/26/28A-2	V_{OUT} = V_{BB}	–375	–480	–675	μA
Output ON Voltage	V_{OUT}	UDN-6116/18A	V_{IN} = 2.4 V, I_{OUT} = 25mA	77	78	–	V
		UDN-6116/18A-2		57	58	–	V
		UDN-6126/28A	V_{IN} = 4.0 V, I_{OUT} = 25mA	77	78	–	V
		UDN-6126/28A-2		57	58	–	V
Input ON Current	I_{IN}	UDN-6116/18A and	V_{IN} = 2.4 V, T_A = 25°C	–	120	200	μA
		UDN-6116/18A-2	V_{IN} = 5.0 V, T_A = 25°C	–	375	600	μA
		UDN-6126/28A and	V_{IN} = 4.0 V, T_A = 25°C	–	130	200	μA
		UDN-6126/28A-2	V_{IN} = 15 V, T_A = 25°C	–	675	1000	μA
Supply Current	I_{BB}	All	All Inputs Open	–	10	100	μA
		UDN-6116A	All Inputs = 2.4 V	–	5.0	7.5	mA
		UDN-6116A-2		–	4.0	6.0	mA
		UDN-6118A	All Inputs = 2.4 V	–	6.0	9.0	mA
		UDN-6118A-2		–	5.5	8.0	mA
		UDN-6126A	All Inputs = 4.0 V	–	5.0	7.5	mA
		UDN-6126A-2		–	4.0	6.0	mA
		UDN-6128A	All Inputs = 4.0 V	–	6.0	9.0	mA
		UDN-6128A-2		–	5.5	8.0	mA

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	V_{BB}	UDN-6116/18/26/28A	5.0	–	70	V
		UDN-6116/18/26/28A-2	5.0	–	50	V
Input ON Voltage	V_{IN}	UDN-6116/18A, 6116/18A-2	2.4	–	15	V
		UDN-6126/28A, 6126/28A-2	4.0	–	15	V
Output ON Current	I_{OUT}	All	–	–	25	mA



TYPICAL MULTIPLEXED FLUORESCENT DISPLAY

TYPE UDN-6144A, UDN-6164A, AND UDN-6184A GAS DISCHARGE DISPLAY DIGIT DRIVERS

FEATURES

- Reliable Monolithic Construction
- High Output Breakdown Voltage
- High Output Current Capability
- Low Power
- Minimum Size

Description

Designed for interfacing between MOS, or other low-voltage circuitry, and the anode of gas discharge display panels, these monolithic high-voltage bipolar integrated circuits dramatically reduce the number of discrete components previously required. The Types UDN-6144A, UDN-6164A, and UDN-6184A are used with multiplexed gas discharge display panels, such as the Burroughs Panaplex®, the Cherry Plasma-Lux, and the Beckman SP Series in calculator, clock, or instrumentation applications. Each driver contains appropriate level shifting, signal amplification, output off state voltage bias, and 70mA output current sourcing for the sequential addressing of display panel anodes. The inputs include pull-down resistors for direct connection to open drain PMOS logic.

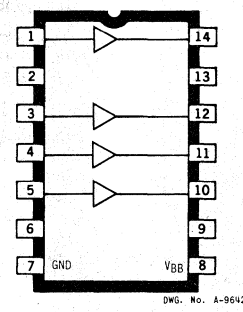
The Type UDN-6144A contains four complete drivers, while the Type UDN-6164A contains six drivers and the Type UDN-6184A contains eight drivers. Applications with a greater number of digits may use any combination of units for minimum package count.

Applications

The devices can be used in a wide variety of low-level to high-voltage applications. Their high reliability, minimum size, ease of installation, and low cost make them the ideal choice in many applications. A typical application showing the use of these devices, and their counterpart cathode drivers, is shown.

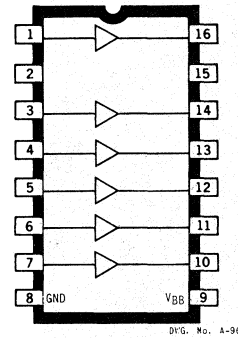
Due to the high input impedance of these devices, they are susceptable to static discharge damage sometimes associated with handling and testing. Therefore, techniques similar to those used for handling MOS devices should be employed. (See Page 5-2).

TYPE UDN-6144A
(FOUR DRIVERS)



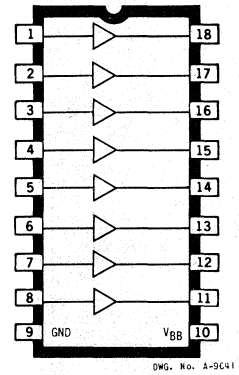
DWG. No. A-9642

TYPE UDN-6164A
(SIX DRIVERS)



DWG. No. A-9643

TYPE UDN-6184A
(EIGHT DRIVERS)



DWG. No. A-9641

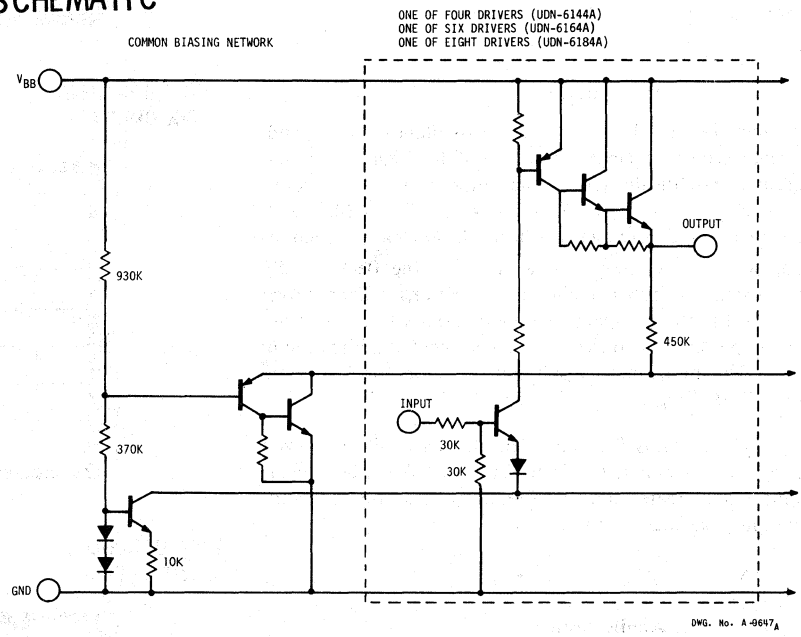
3

ABSOLUTE MAXIMUM RATINGS AT 25°C

Supply Voltage, V_{BB} . . . . . +120 V
Input Voltage, V_{IN} . . . . . +20 V
Output Current, I_{OUT} . . . . . 70 mA
Power Dissipation, P_D:
UDN-6144/64A . . . . . 1.0 W*
UDN-6184A . . . . . 1.13 W†
Operating Temperature Range, T_A . . . . . 0°C to +70°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C

*Derating Factor above 25°C: −8 mW/°C
†Derating Factor above 25°C: −9.1 mW/°C

PARTIAL SCHEMATIC



ELECTRICAL CHARACTERISTICS: $T_A = +25°C$, $V_{BB} = +110V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Test Fig.	Limits Min.	Typ.	Max.	Units
Output ON Voltage	V_{ON}	Test input at 4.5V Other inputs at 0.5V, I_{OUT} = 20mA	1	105	108	—	V
Output OFF Voltage	V_{OFF}	Test input at 0.5V, One input at 4.5V All other inputs open, Reference V_{BB}	2	−68	−73	—	V
Input High Current	I_{IH}	Test input at 15V, Other inputs at 0V	3	—	250	330	μA
Input Low Current	I_{IL}	Test input at 0V, One input at 15V, All other inputs at 0V	4	—	−1	−5	μA
Supply Current	I_{BB}	One input at 4.5V Other inputs at 0.5V, All outputs open, Repeat for all inputs	5A	—	450	750	μA
		All inputs at 0V, All outputs open	5B	—	85	125	μA

NOTES:
1. All voltage measurements are referenced to Ground terminal unless otherwise specified.
2. All voltage measurements are made with 10MΩ, DVM or VTVM.
3. Recommended V_{BB} operating range: +85V to 110V.

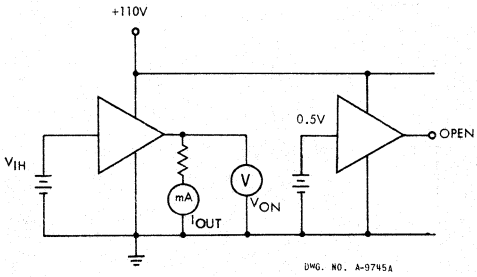


FIGURE 1

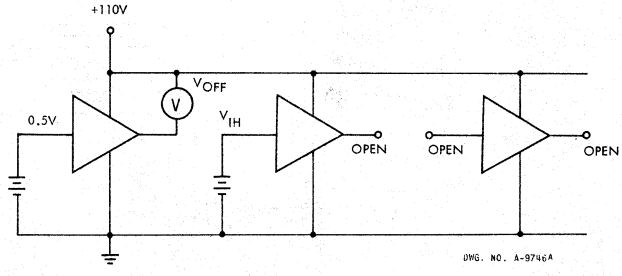


FIGURE 2

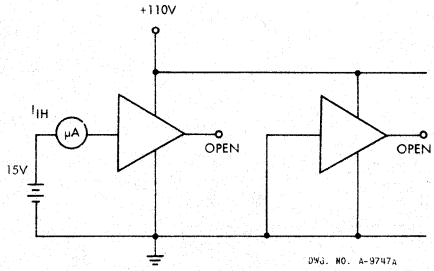


FIGURE 3

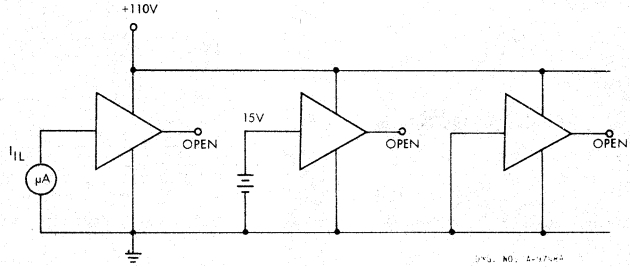


FIGURE 4

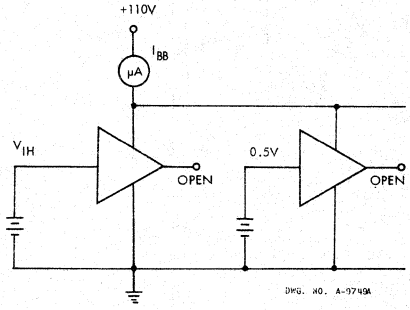


FIGURE 5A

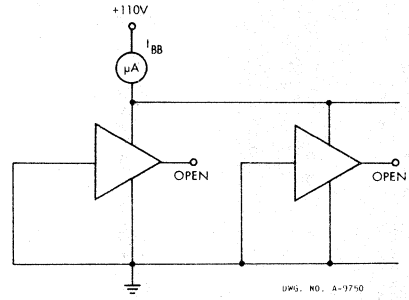
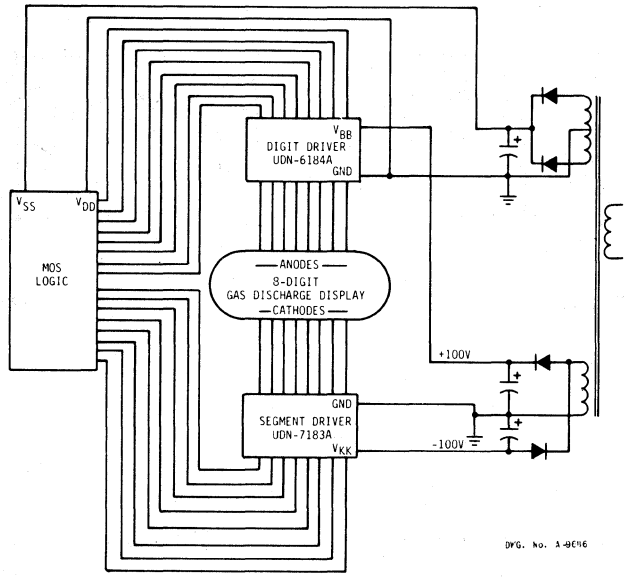
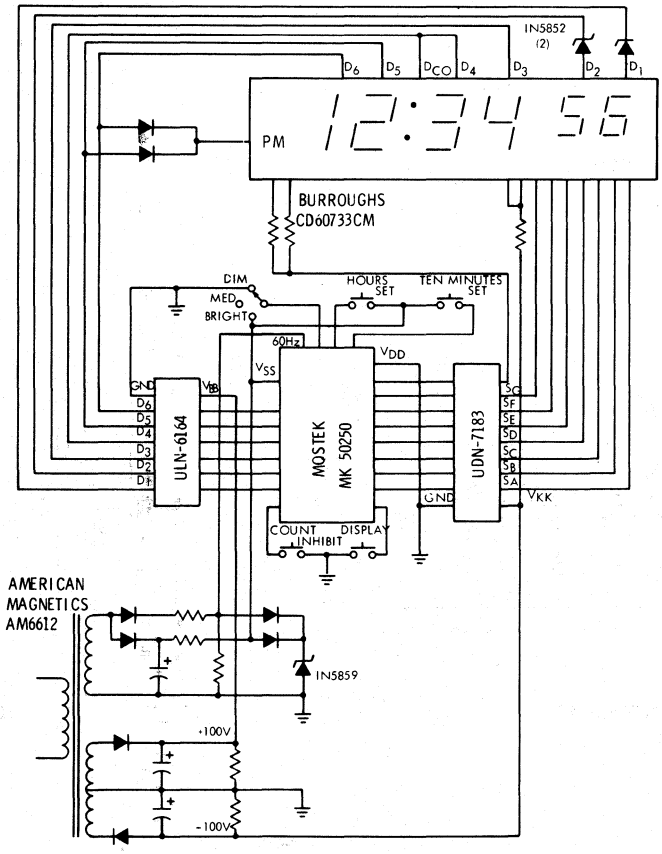


FIGURE 5B

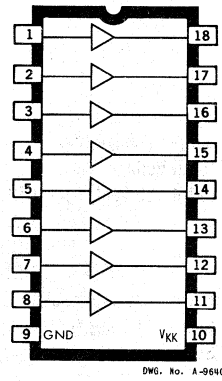
TYPICAL APPLICATION



TYPICAL SIX-DIGIT CLOCK



SERIES UDN-7180A GAS DISCHARGE DISPLAY SEGMENT DRIVERS



DWG. No. A-9640

FEATURES

- Reliable Monolithic Construction
- High Output Breakdown Voltage
- Low Power
- Minimum Size

Description

Series UDN-7180A segment drivers are monolithic high-voltage bipolar integrated circuits for interfacing between MOS or other low-voltage circuits and the cathode of gas-discharge display panels.

These drivers reduce substantially the number of discrete components required with panels (Beckman, Burroughs, Dale, Matsushita, NEC, Pantek, etc) in calculator, clock and instrumentation applications.

The UDN-7183A, UDN-7184A, and UDN-7186A drivers contain appropriate level shifting, signal amplification, current limiting, and output OFF-state voltage bias. The UDN-7180A driver requires external current limiting and is intended for higher-current applications or where individual outputs are operated at different current levels (i.e. with alpha-numeric displays). All inputs have pull-down resistors for direct connection to open-drain PMOS logic.

All devices are customarily furnished for use with 12 to 25 V PMOS, CMOS, or other high-level output logic devices.

These devices provide output currents suitable for display segments in a wide variety of display sizes and number of display digits. Either the fixed split supply operation or the feedback controlled scheme is allowed.

Applications

The series UDN-7180A drivers can be used in a wide variety of low-level to high-voltage applications utilizing gas discharge displays such as those found in calculators, clocks, point-of-sale terminals, and instruements. Their high reliability combined with minimum size, ease of installation, and the cost advantages of a complete monolithic interface make them the ideal choice in many applications. A typical application showing the use of these devices, and their counterpart anode drivers, is shown.

These devices were formerly known under the Developmental No. UDD-7183 and UDD-7186.

ABSOLUTE MAXIMUM RATINGS
(Referenced to Terminal 9)

Supply Voltage, V_{KK} ..... −120 V
Input Voltage, V_{IN} ..... +20 V
Output Current, I_{OUT}: UDN-7180A 20mA
UDN-7183A ..... 3.25 mA
UDN-7184A ..... 2.0 mA
UDN-7186A ..... 1.0 mA
Power Dissipation, at 70°C, P_D ..... 725 mW*
Operating Temperature Range, T_A ..... **0°C to +70°C**
Storage Temperature Range, T_S ..... −65°C to +150°C

*Derate at the rate of 9.1 mW/°C above 70°C.

ELECTRICAL CHARACTERISTICS: T_A = +25°C, V_{KK} = −110 V (unless otherwise specified)

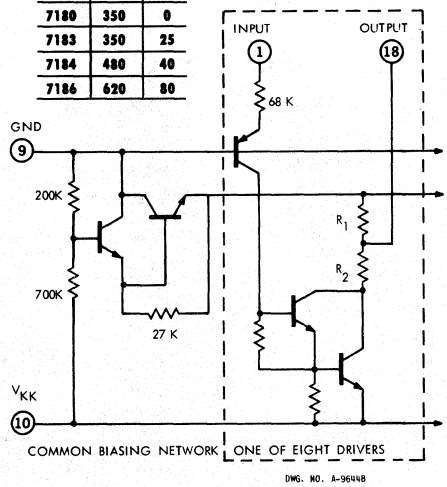
Characteristic	Symbol	Test Conditions	Test Fig.	UDN-7180/83A Min.	UDN-7180/83A Typ.	UDN-7180/83A Max.	UDN-7184A Min.	UDN-7184A Typ.	UDN-7184A Max.	UDN-7186A Min.	UDN-7186A Typ.	UDN-7186A Max.	Units
Output ON Voltage UDN-7183/84/86A	V_{ON}	All inputs at 4.5 V	1	−100	−104	—	−98	−102	—	−97	−100	—	V
		All inputs at 4.5 V, V_{KK} = −70 V	1	—	−66	—	—	−65	—	—	−63	—	V
Output ON Voltage UDN-7180A	V_{ON}	All inputs at 4.5 V, I_{ON} = 14 mA		−105	−108	—	—	—	—	—	—	—	V
Output OFF Voltage	V_{OFF}	All inputs at 0.5 V, Reference V_{KK}	2	76	84	—	76	84	—	76	84	—	V
Output Current ($I_{LIMITING}$)	I_{ON}	All inputs at 15 V, V_{KK} = −110 V, Test output held at −60 V	3A	UDN-7183A only 1475	1850	2450	910	1140	1520	440	550	725	μA
Output Current (I_{SENSE})	I_{ON}	All inputs at 0.5 V, V_{KK} = −110 V, Test output held at −66 V	3B	−95	−120	−155	−65	−85	−115	−50	−65	−90	μA
Input High Current	I_{IH}	Test input at 15 V, Other inputs at 0 V	4	—	200	275	—	200	275	—	200	275	μA
Input Low Current	I_{IL}	Test input at 0.5 V, One input at 4.5 V, Other inputs at 0.5 V	5	—	1	10	—	1	10	—	1	10	μA
Supply Current	I_{KK}	All inputs at 0 V	6	—	125	175	—	125	175	—	125	175	μA

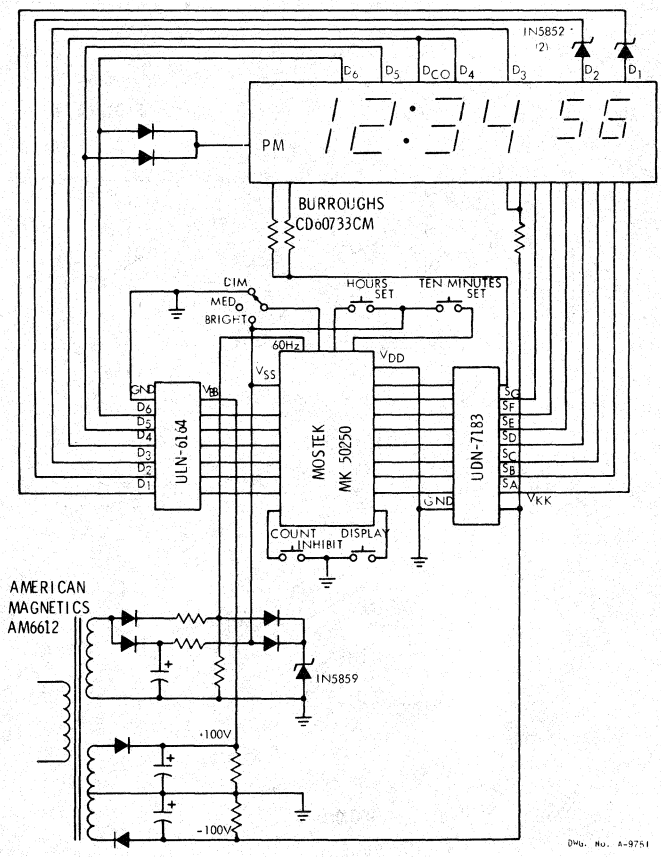
NOTES:
1. All voltage measurements are referenced to pin 9 unless otherwise specified.
2. All voltage measurements made with 10MΩ, DVM or VTVM.
3. Recommended V_{KK} operating range: −85 to −110 V.

Due to the high input impedance of these devices, they are susceptable to static discharge damage sometimes associated with handling and testing. Therefore, techniques similar to those used for handling MOS devices should be employed. (See Page 5-2).

PARTIAL SCHEMATIC

	R_1 (kΩ)	R_2 (kΩ)
7180	350	0
7183	350	25
7184	480	40
7186	620	80





TYPICAL SIX-DIGIT CLOCK USING TYPE UDN-7183A

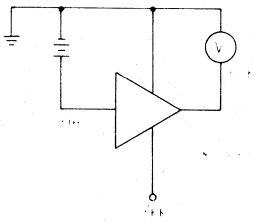


FIGURE 1

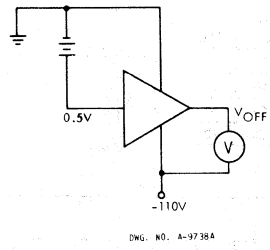


FIGURE 2

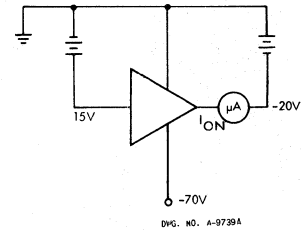


FIGURE 3A

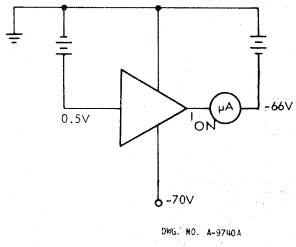


FIGURE 3B

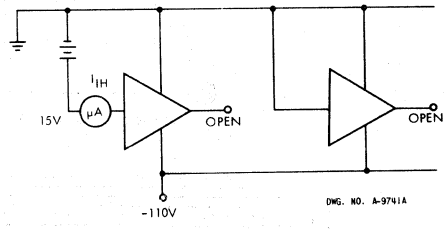


FIGURE 4

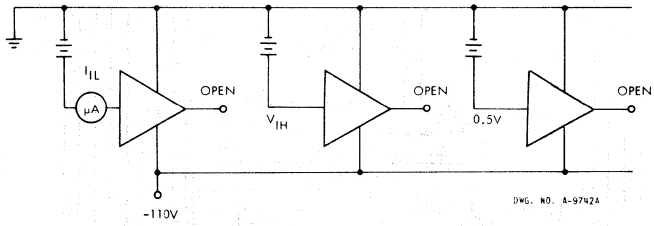


FIGURE 5

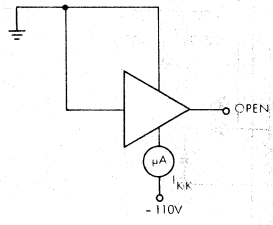


FIGURE 6

Device Type	Data	Applications	Thermal
TPP-1000 and 2000	4-81		—
ULN-2001 thru 2025A	4-2	7-2, 6, 35, 42	1B
ULN-2001 thru 2015R	4-2		3B
ULS-2001 thru 2025H	4-11		4B
ULS-2001 thru 2015R	4-11		3B
ULN-2031 thru 2033A	4-22	7-6	1E
ULN-2031 thru 2033R	4-22		3B
ULS-2045H	4-24		4B
ULS-2045R	4-24		3B
ULN-2046A	4-24		1E
ULN-2046A-1	4-26		1E
ULN-2047A	4-27		1E
ULN-2054A	4-28		1E
ULN-2061 and 2062M	4-31	7-24	1C
ULN-2064 thru 2077B	4-31	7-5, 32	2
ULN-2081 and 2082A	4-42	7-6, 37	1E
ULN-2083A	4-43		1E
ULN-2083A-1	4-45		1E
ULS-2083H	4-43		4B
ULN-2086A	4-45		1E
TPQ-2221 thru 2484	4-83		—
UDN-2580A	4-46		1A
UDN-2580R	4-46		3A
ULN-2801 thru 2825A	4-50		1A
ULN-2801 thru 2815R	4-50		3A
ULS-2801 thru 2815R	4-60		3A
UDN-2841 thru 2846B	4-71	7-36	2
TPQ-2906 and 2907	4-83		—
UDN-2956 and 2957A	4-77	7-36	1B
UDN-2956 and 2957R	4-77		3B
UDN-2981 thru 2984A	4-79	7-6, 39	1A
UDN-2981 thru 2984R	4-79		3A
TPP-3000	4-81		—
TPQ-3724 thru 3906	4-83		—
TPP-4000	4-81		—
TPQ-6001 thru 6700	4-83		—

4

Device Type	I_{OUT}	V_{OUT}	Outputs
UL( )-2001 thru 2005A/H/R	500 mA	50 V	Sink 7
UL( )-2011 thru 2015A/H/R	600 mA	50 V	Sink 7
UL( )-2021 thru 2025A/H	500 mA	95 V	Sink 7
UL( )-2031 thru 2054A/H/R		Transistor Arrays	
ULN-2061M	1.75 A	50 V	Source/Sink 2
ULN-2062M	1.75 A	80 V	Source/Sink 2
ULN-2064/68/70B	1.75 A	50 V	Sink 4
ULN-2067/69/71B	1.75 A	80 V	Sink 4
ULN-2074B	1.75 A	50 V	Source/Sink 4
ULN-2077B	1.75 A	80 V	Source/Sink 4
ULN-2081A	200 mA	16 V	Sink 7
ULN-2082A	200 mA	16 V	Source 7
UL( )-2083 thru 2086A/H		Transistor Arrays	
UDN-2580A/R	−500 mA	−50 V	Source 8
UL( )-2801 thru 2805A/H/R	500 mA	50 V	Sink 8
UL( )-2811 thru 2815A/H/R	600 mA	50 V	Sink 8
UL( )-2821 thru 2825A/H	500 mA	95 V	Sink 8
UDN-2841 and 2842B	−1.75 A	−50 V	Sink 4
UDN-2843 and 2844B	−1.75 A	−50 V	Source 4
UDN-2845 and 2846B	±1.75 A	−50 V	Source/Sink 4
UDN-2956 and 2957A/R	−500 mA	−80 V	Source 5
UDN-2981 and 2982A	500 mA	50 V	Source 8
UDN-2983 and 2984A	500 mA	80 V	Source 8
TPP—		Darlington Transistor Arrays	
TPQ—		Transistor Arrays	

SERIES ULN-2000A
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

THESE high-voltage, high-current Darlington arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral diodes for inductive load transient suppression. Peak inrush currents to 600 mA (Series ULN-2000A and ULN-2020A) or 750 mA (Series ULN-2010A) are permissable, making them ideal for driving tungsten filament lamp loads.

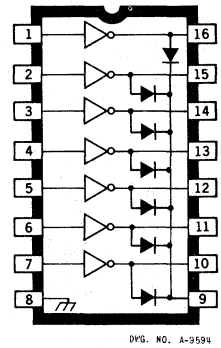
The Series ULN-2001A devices are general purpose arrays which may be used with standard bipolar digital logic using external current limiting, or with most PMOS or CMOS directly. All are pinned with outputs opposite inputs to facilitate ease of circuit board layout and are priced to compete directly with discrete transistor alternatives.

The Series ULN-2002A was specifically designed for use with 14 to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also means excellent noise immunity for these devices.

The Series ULN-2003A has a 2.7 kΩ series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs – particularly those beyond the capabilities of standard logic buffers.

The Series ULN-2004A features a 10.5 kΩ series input resistor to permit their operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of the Series ULN-2003A while the required input voltage is less than that required by the Series ULN-2002A.

The Series ULN-2005A is especially designed for use with standard and Schottky TTL where higher output currents are required and loading of the logic output is not a concern. These devices will sink a minimum of 350 mA when driven from a "totem pole" logic output. Typical voltage and current levels for both the Series ULN-2003A and ULN-2005A are shown in the graphs.



DWG. NO. A-9594

The Series ULN-2000A is the original high-voltage, high-current Darlington array. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Outputs may be paral-

Device Type Number Designation

$V_{CE(MAX)}$ = $I_{C(MAX)}$ =	50 V 500 mA	50 V 600 mA	95 V 500 mA
	Type Number		
General Purpose PMOS, CMOS	ULN-2001A	ULN-2011A	ULN-2021A
14 - 25 V PMOS	ULN-2002A	ULN-2012A	ULN-2022A
5 V TTL, CMOS	ULN-2003A	ULN-2013A	ULN-2023A
6 - 15 V CMOS, PMOS	ULN-2004A	ULN-2014A	ULN-2024A
High Output TTL	ULN-2005A	ULN-2015A	ULN-2025A

Series ULN-2000A and ULN-2010A devices are also available (with reduced package power capability) in industrial-grade hermetic packages. To order, change the last letter of the part number from 'A' to 'R'. Note that the high-voltage devices ($BV_{CE} \geq 95$ V) are not presently available with this packaging option.

leled for higher load current capability. The Series ULN-2010A devices are similar except that they will sink 600 mA. The Series ULN-2020A will sustain 95 V in the OFF state. A table showing the specific type numbers available for the various applications is given on page 4-2.

All Series ULN-2000A Darlington arrays are furnished in a 16-pin dual in-line plastic package. These devices can also be supplied in a hermetic dual in-line package for use in military and aerospace applications (with a slightly reduced power handling capacity).

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature for any one Darlington pair (unless otherwise noted)

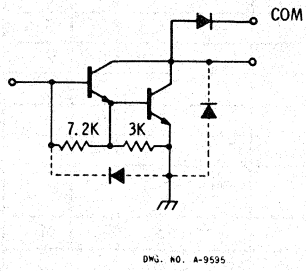
Output Voltage, V_{CE} (Series ULN-2000, 2010A)	50 V
(Series ULN-2020A)	95 V
Input Voltage, V_{IN} (Series ULN-2002, 2003, 2004A)	30 V
(Series ULN-2005A)	15 V
Continuous Collector Current, I_C (Series ULN-2000, 2020A)	500 mA
(Series ULN-2010A)	600 mA
Continuous Base Current, I_B	25 mA
Power Dissipation, P_D (one Darlington pair)	1.0 W
(total package)	2.0 W*
Operating Ambient Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 16.67 mW/°C above 25°C.

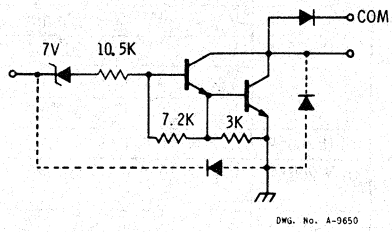
Under normal operating conditions, these devices will sustain 350 mA per output with $V_{CE(SAT)} = 1.6$ V at 70°C with a pulse width of 20 ms and a duty cycle of 34%. Other allowable combinations of output current, number of outputs conducting, and duty cycle are shown on page 4-8.

4

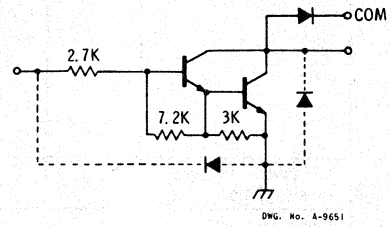
PARTIAL SCHEMATICS



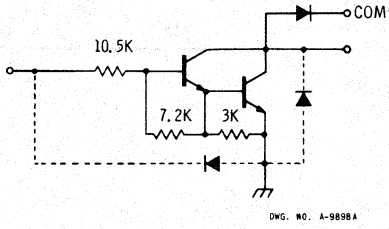
Series ULN-2001A (each driver)



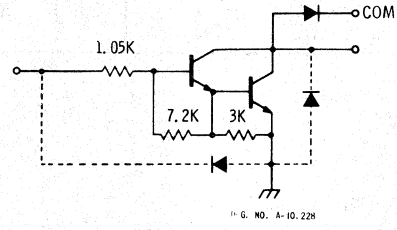
Series ULN-2002A (each driver)



Series ULN-2003A (each driver)



Series ULN-2004A (each driver)



Series ULN-2005A (each driver)

SERIES ULN-2000A

ELECTRICAL CHARACTERISTICS AT 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	–	–	50	μA
				V_{CE} = 50 V, T_A = 70°C	–	–	100	μA
		1B	ULN-2002A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	–	–	500	μA
			ULN-2004A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	–	–	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 μA	–	0.9	1.1	V
				I_C = 200 mA, I_B = 350 μA	–	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	–	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2002A	V_{IN} = 17 V	–	0.82	1.25	mA
			ULN-2003A	V_{IN} = 3.85 V	–	0.93	1.35	mA
			ULN-2004A	V_{IN} = 5.0 V	–	0.35	0.5	mA
				V_{IN} = 12 V	–	1.0	1.45	mA
			ULN-2005A	V_{IN} = 3.0 V	–	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	–	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2002A	V_{CE} = 2.0 V, I_C = 300 mA	–	–	13	V
			ULN-2003A	V_{CE} = 2.0 V, I_C = 200 mA	–	–	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	–	–	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	–	–	3.0	V
			ULN-2004A	V_{CE} = 2.0 V, I_C = 125 mA	–	–	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	–	–	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	–	–	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	–	–	8.0	V
			ULN-2005A	V_{CE} = 2.0 V, I_C = 350 mA	–	–	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2001A	V_{CE} = 2.0 V, I_C = 350 mA	1000	–	–	
Input Capacitance	C_{IN}	–	All		–	15	25	pF
Turn-On Delay	t_{PLH}	–	All	0.5 E_{in} to 0.5 E_{out}	–	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	–	All	0.5 E_{in} to 0.5 E_{out}	–	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 50 V, T_A = 25°C	–	–	50	μA
				V_R = 50 V, T_A = 70°C	–	–	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	–	1.7	2.0	V

SERIES ULN-2010A

ELECTRICAL CHARACTERISTICS AT 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 50 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2012A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2014A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
				I_C = 500 mA, I_B = 600 μA	—	1.7	1.9	V
Input Current	$I_{IN(ON)}$	3	ULN-2012A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2013A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2014A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2015A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2012A	V_{CE} = 2.0 V, I_C = 500 mA	—	—	17	V
			ULN-2013A	V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	—	—	3.5	V
			ULN-2014A	V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	—	—	9.5	V
			ULN-2015A	V_{CE} = 2.0 V, I_C = 500 mA	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2011A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
				V_{CE} = 2.0 V, I_C = 500 mA	900	—	—	
Input Capacitance	C_{IN}	–	All		—	15	25	pF
Turn-On Delay	t_{PLH}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	μA
				V_R = 50 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V
				I_F = 500 mA	—	2.1	2.5	V

SERIES ULN-2020A

ELECTRICAL CHARACTERISTICS AT 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 95 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 95 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2022A	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2024A	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 μA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2022A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2023A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2024A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2025A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2022A	V_{CE} = 2.0 V, I_C = 300 mA	—	—	13	V
			ULN-2023A	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN-2024A	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
			ULN-2025A	V_{CE} = 2.0 V, I_C = 350 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2021A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
Input Capacitance	C_{IN}	–	All		—	15	25	pF
Turn-On Delay	t_{PLH}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 95 V, T_A = 25°C	—	—	50	μA
				V_R = 95 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

TEST FIGURES

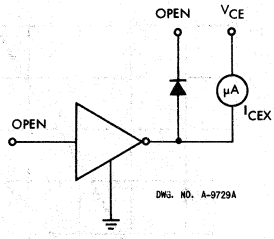


FIGURE 1A

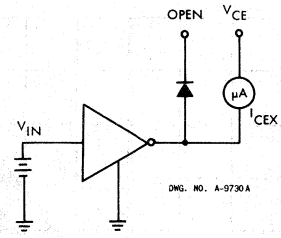


FIGURE 1B

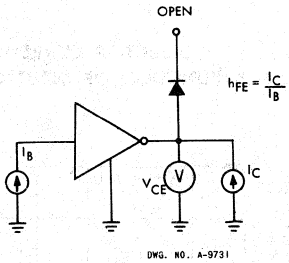


FIGURE 2

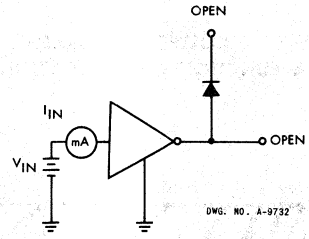


FIGURE 3

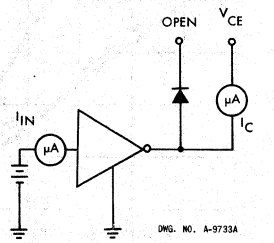


FIGURE 4

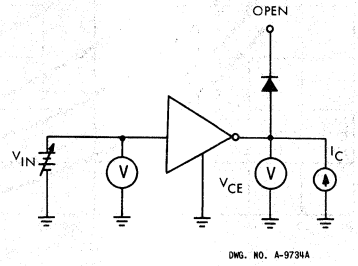


FIGURE 5

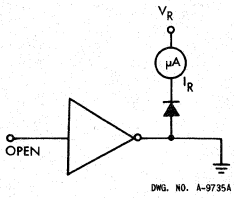


FIGURE 6

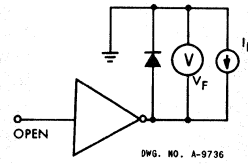
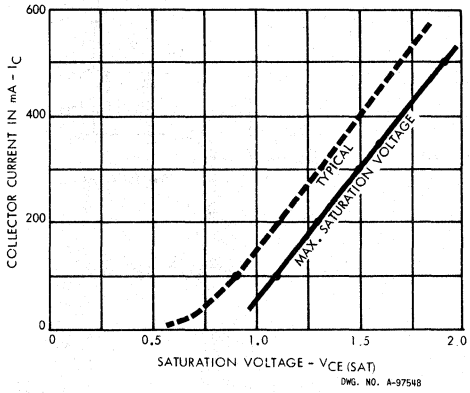
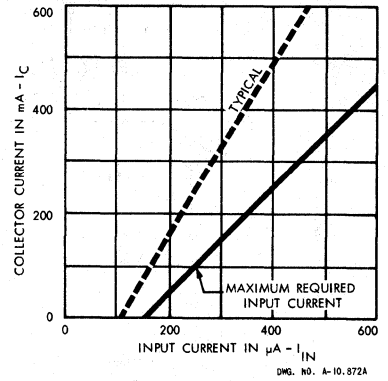


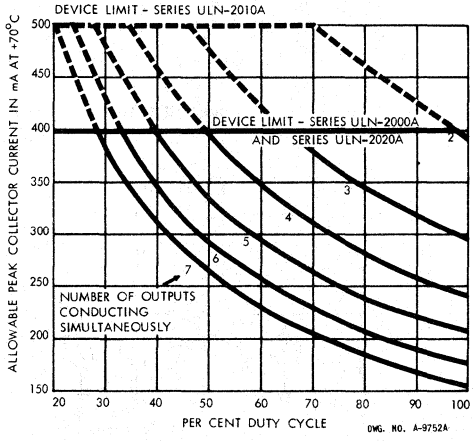
FIGURE 7



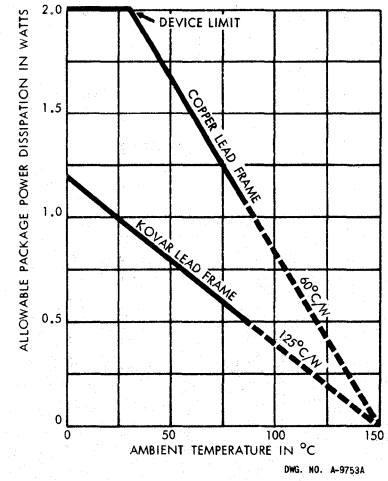
COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT

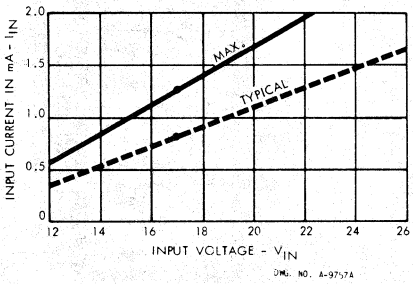


PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS

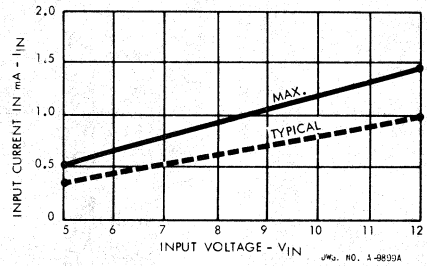


ALLOWABLE AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



SERIES ULN-2002A



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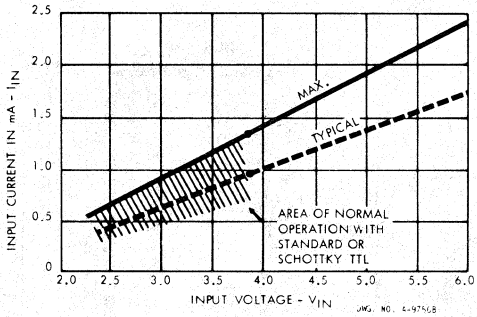
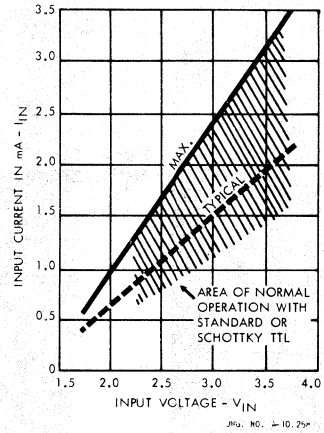


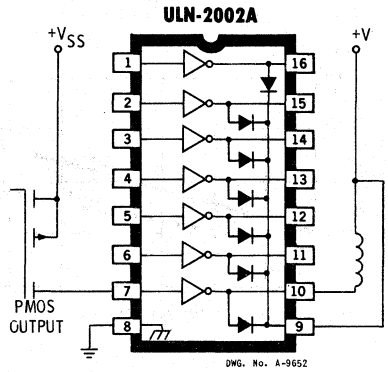
SERIES ULN-2003A



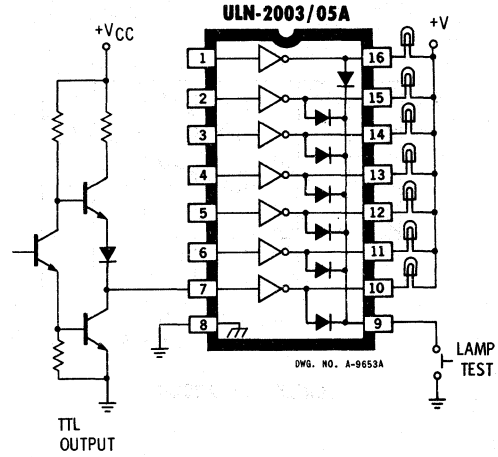
SERIES ULN-2005A

4

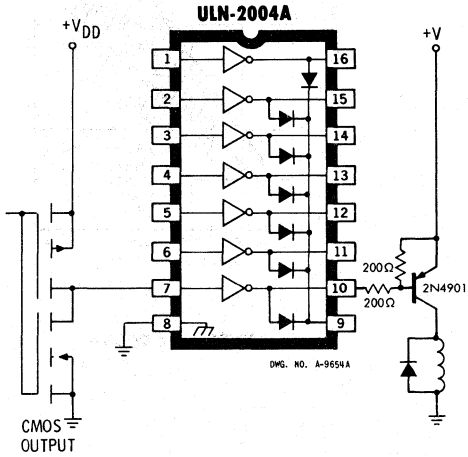
TYPICAL APPLICATIONS



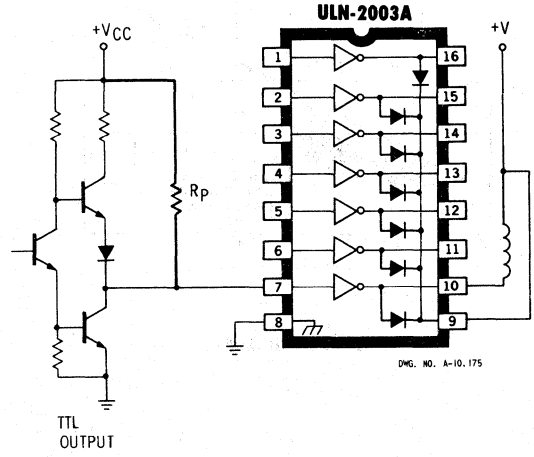
PMOS TO LOAD



TTL TO LOAD



BUFFER FOR HIGHER CURRENT LOADS

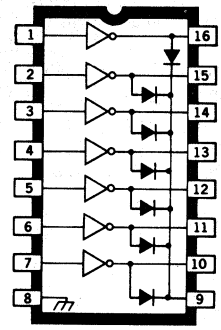


USE OF PULL-UP RESISTORS
TO INCREASE DRIVE CURRENT

SERIES ULS-2000H and ULS-2000R HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Peak Output Current to 600 mA
- Transient Protected Outputs
- Side-Brazed Hermetic Package, or
- Cer-DIP Package
- High-Reliability Screening Available
- Wide Operating Temperature Ranges



DWG. NO. A-9594

COMPRISED of seven silicon NPN Darlington power drivers on a common monolithic substrate, the Series ULS-2000H and ULS-2000R arrays are ideally suited for driving relays, solenoids, lamps, and other devices with up to 3.0 A output current per package. The side-brazed, hermetically-sealed Series ULS-2000H devices are rated for operation over the temperature range of −55°C to +125°C, recommending them for military and aerospace applications. The Cer-DIP, industrial grade hermetic Series ULS-2000R devices are rated for use over the operating temperature range of −40°C to +85°C, allowing their use in commercial and industrial applications where severe environments may be encountered.

The twenty-five integrated circuits listed in this engineering bulletin permit the circuit designer to select the optimum device for his application. There are 2 packages, 5 input characteristics, 2 output voltages, and 2 output currents covered by the listings. The appropriate part for use in specific applications can be determined from the Device Type Number Designation chart. Note that the high-voltage devices ($BV_{CE} \geqq 95$ V) are available in the Series ULS-2000H only. All units feature open collector outputs and integral diodes for inductive load transient suppression.

All Series ULS-2000H arrays are furnished in a 16-pin side-brazed dual in-line hermetic package which conforms to the dimensional requirements of Military Specification MIL-M-38510 and meets the processing and environmental requirements of Military Standard MIL-STD-883, Methods 5004 and 5005. Series ULS-2000H arrays with high-reliability screening are described on page 4-21.

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Device Type Number Designation

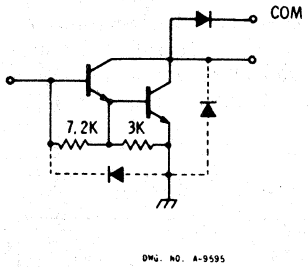
$V_{CE(MAX)}$ = / $I_{C(MAX)}$ =	50 V 500 mA	50 V 600 mA	95 V 500 mA
	Type Number		
General Purpose PMOS, CMOS	ULS-2001*	ULS-2011*	ULS-2021H
14 - 25 V PMOS	ULS-2002*	ULS-2012*	ULS-2022H
5 V TTL, CMOS	ULS-2003*	ULS-2013*	ULS-2023H
6 - 15 V CMOS, PMOS	ULS-2004*	ULS-2014*	ULS-2024H
High Output TTL	ULS-2005*	ULS-2015*	ULS-2025H

*Complete part number includes a final letter to indicate package. H = hermetic dual in-line, R = ceramic dual in-line.

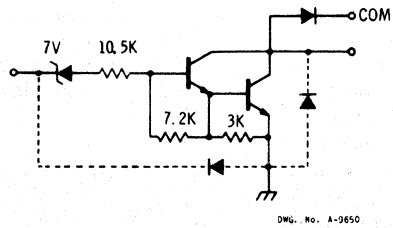
ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE} (Series ULS-2000, 10*) ..... 50 V
(Series ULS-2020H) ..... 95 V
Input Voltage, V_{IN} (Series ULS-2002, 03, 04*) ..... 30 V
(Series ULS-2005*) ..... 15 V
Peak Output Current, I_{OUT} (Series ULS-2000*, 20H) ..... 500 mA
(Series ULS-2010*) ..... 600 mA
Ground Terminal Current, I_{GND} ..... 3.0 A
Continuous Input Current, I_{IN} ..... 25 mA
Power Dissipation, P_D (one Darlington pair) ..... 1.0 W
(total package) ..... See Graph, p 4-18
Operating Temperature Range, T_A ('H' package) ..... −55°C to +125°C
('R' package) ..... −40°C to +85°C
Storage Temperature Range, T_S ..... −65°C to +150°C

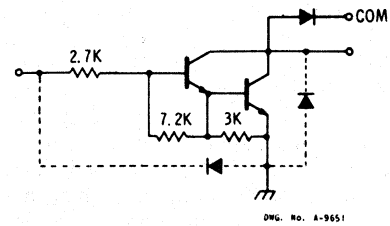
PARTIAL SCHEMATICS



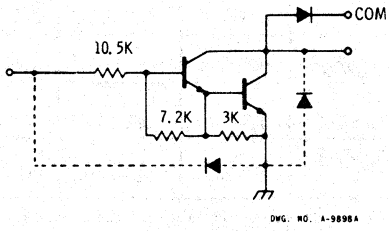
Series ULS-2001*
(each driver)



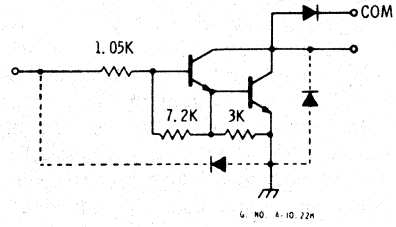
Series ULS-2002*
(each driver)



Series ULS-2003*
(each driver)



Series ULS-2004*
(each driver)



Series ULS-2005*
(each driver)

*Complete part number includes a final letter to indicate package. H = hermetic dual in-line, R = ceramic dual in-line.

SERIES ULS-2000H and ULS-2000R

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions			Limits			
			Temp.		Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	μA
		ULS-2002*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	μA
		ULS-2004*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	Min.	I_C = 350 mA, I_B = 850 μA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 μA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 μA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 μA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 μA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 μA	2	—	0.9	1.1	V
			Max.	I_C = 350 mA, I_B = 500 μA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 μA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 μA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS-2002*		V_{IN} = 17 V	3	575	850	1300	μA
		ULS-2003*		V_{IN} = 3.85 V	3	675	930	1350	μA
		ULS-2004*		V_{IN} = 5 V	3	250	350	500	μA
				V_{IN} = 12 V	3	750	1000	1450	μA
		ULS-2005*		V_{IN} =3 V	3	1150	1500	2400	μA
	$I_{IN(OFF)}$	All	Max.	I_C = 500 μA	4	25	50	—	μA
Input Voltage	$V_{IN(ON)}$	ULS-2002*	Min.	V_{CE} = 2 V, I_C = 300 mA	5	—	—	18	V
			Max.	V_{CE} = 2 V, I_C = 300 mA	5	—	—	13	V
		ULS-2003*	Min.	V_{CE} = 2 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2 V, I_C = 300 mA	5	—	—	3.9	V
			Max.	V_{CE} = 2 V, I_C = 200 mA	5	—	—	2.4	V
				V_{CE} = 2 V, I_C = 250 mA	5	—	—	2.7	V
				V_{CE} = 2 V, I_C = 300 mA	5	—	—	3.0	V
		ULS-2004*	Min.	V_{CE} = 2 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2 V, I_C = 350 mA	5	—	—	12	V
			Max.	V_{CE} = 2 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2 V, I_C = 200 mA	5	—	—	6.0	V
				V_{CE} = 2 V, I_C = 275 mA	5	—	—	7.0	V
				V_{CE} = 2 V, I_C = 350 mA	5	—	—	8.0	V
		ULS-2005*	Min.	V_{CE} = 2 V, I_C = 350 mA	5	—	—	3.0	V
			Max.	V_{CE} = 2 V, I_C = 350 mA	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS-2001*	Min.	V_{CE} = 2 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2 V, I_C = 350 mA	2	1000	—	—	—
Input Capacitance	C_{IN}	All	+25°C		—	—	15	25	pF
Turn-On Delay	t_{PLH}	All	+25°C	0.5 E_{in} to 0.5 E_{out}	—	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C	0.5 E_{in} to 0.5 E_{out}	—	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package. H = hermetic dual in-line, R = ceramic dual in-line.
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

SERIES ULS-2010H and ULS-2010R

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions: Temp.	Test Conditions	Fig.	Limits: Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	μA
		ULS-2012*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	μA
		ULS-2014*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	Min.	I_C = 500 mA, I_B = 1100 μA	2	—	1.8	2.1	V
				I_C = 350 mA, I_B = 850 μA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 μA	2	—	1.3	1.5	V
			+25°C	I_C = 500 mA, I_B = 600 μA	2	—	1.7	1.9	V
				I_C = 350 mA, I_B = 500 μA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 μA	2	—	1.1	1.3	V
			Max.	I_C = 500 mA, I_B = 600 μA	2	—	1.8	2.1	V
				I_C = 350 mA, I_B = 500 μA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 μA	2	—	1.3	1.5	V
Input Current	$I_{IN(ON)}$	ULS-2012*		V_{IN} = 17 V	3	575	850	1300	μA
		ULS-2013*		V_{IN} = 3.85 V	3	675	930	1350	μA
		ULS-2014*		V_{IN} = 5 V	3	250	350	500	μA
				V_{IN} = 12 V	3	750	1000	1450	μA
		ULS-2015*		V_{IN} = 3 V	3	1150	1500	2400	μA
	$I_{IN(OFF)}$	All	Max.	I_C = 500 μA	4	25	50	—	μA
Input Voltage	$V_{IN(ON)}$	ULS-2012*	Min.	V_{CE} = 2 V, I_C = 500 mA	5	—	—	23.5	V
			Max.	V_{CE} = 2 V, I_C = 500 mA	5	—	—	17	V
		ULS-2013*	Min.	V_{CE} = 2 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2 V, I_C = 300 mA	5	—	—	3.9	V
				V_{CE} = 2 V, I_C = 500 mA	5	—	—	6.0	V
			Max.	V_{CE} = 2 V, I_C = 250 mA	5	—	—	2.7	V
				V_{CE} = 2 V, I_C = 300 mA	5	—	—	3.0	V
				V_{CE} = 2 V, I_C = 500 mA	5	—	—	3.5	V
		ULS-2014*	Min.	V_{CE} = 2 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2 V, I_C = 350 mA	5	—	—	12	V
				V_{CE} = 2 V, I_C = 500 mA	5	—	—	17	V
			Max.	V_{CE} = 2 V, I_C = 275 mA	5	—	—	7.0	V
				V_{CE} = 2 V, I_C = 350 mA	5	—	—	8.0	V
				V_{CE} = 2 V, I_C = 500 mA	5	—	—	9.5	V
		ULS-2015*	Min.	V_{CE} = 2 V, I_C = 350 mA	5	—	—	3.0	V
				V_{CE} = 2 V, I_C = 500 mA	5	—	—	3.5	V
			Max.	V_{CE} = 2 V, I_C = 350 mA	5	—	—	2.4	V
				V_{CE} = 2 V, I_C = 500 mA	5	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS-2011*	Min.	V_{CE} = 2 V, I_C = 500 mA	2	450	—	—	—
			+25°C	V_{CE} = 2 V, I_C = 500 mA	2	900	—	—	—
Input Capacitance	C_{IN}	All	+25°C		—	—	15	25	pF
Turn-On Delay	t_{PLH}	All	+25°C	0.5 E_{in} to 0.5 E_{out}	—	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C	0.5 E_{in} to 0.5 E_{out}	—	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA	7	—	1.7	2.0	V
				I_F = 500 mA	7	—	—	2.5	V

*Complete part number includes a final letter to indicate package. H = hermetic dual in-line, R = ceramic dual in-line.

Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.

Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.

Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

SERIES ULS-2020H

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions Temp.		Fig.	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 95 V	1A	—	—	100	μA
		ULS-2022H		V_{CE} = 95 V, V_{IN} = 6 V	1B	—	—	500	μA
		ULS-2024H		V_{CE} = 95 V, V_{IN} = 1 V	1B	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	Min.	I_C = 350 mA, I_B = 850 μA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 μA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 μA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 μA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 μA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 μA	2	—	0.9	1.1	V
			Max.	I_C = 350 mA, I_B = 500 μA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 μA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 μA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS-2022H		V_{IN} = 17 V	3	575	850	1300	μA
		ULS-2023H		V_{IN} = 3.85 V	3	675	930	1350	μA
		ULS-2024H		V_{IN} = 5 V	3	250	350	500	μA
				V_{IN} = 12 V	3	750	1000	1450	μA
		ULS-2025H		V_{IN} = 3 V	3	1150	1500	2400	μA
	$I_{IN(OFF)}$	All	Max.	I_C = 500 μA	4	25	50	—	μA
Input Voltage	$V_{IN(ON)}$	ULS-2022H	Min.	V_{CE} = 2 V, I_C = 300 mA	5	—	—	18	V
			Max.	V_{CE} = 2 V, I_C = 300 mA	5	—	—	13	V
		ULS-2023H	Min.	V_{CE} = 2 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2 V, I_C = 300 mA	5	—	—	3.9	V
			Max.	V_{CE} = 2 V, I_C = 200 mA	5	—	—	2.4	V
				V_{CE} = 2 V, I_C = 250 mA	5	—	—	2.7	V
				V_{CE} = 2 V, I_C = 300 mA	5	—	—	3.0	V
		ULS-2024H	Min.	V_{CE} = 2 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2 V, I_C = 350 mA	5	—	—	12	V
			Max.	V_{CE} = 2 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2 V, I_C = 200 mA	5	—	—	6.0	V
				V_{CE} = 2 V, I_C = 275 mA	5	—	—	7.0	V
				V_{CE} = 2 V, I_C = 350 mA	5	—	—	8.0	V
		ULS-2025H	Min.	V_{CE} = 2 V, I_C = 350 mA	5	—	—	3.0	V
			Max.	V_{CE} = 2 V, I_C = 350 mA	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS-2021H	Min.	V_{CE} = 2 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2 V, I_C = 350 mA	2	1000	—	—	—
Input Capacitance	C_{IN}	All	+25°C		—	—	15	25	pF
Turn-On Delay	t_{PLH}	All	+25°C	0.5 E_{in} to 0.5 E_{out}	—	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C	0.5 E_{in} to 0.5 E_{out}	—	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 95 V	6	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA	7	—	1.7	2.0	V

Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

TEST FIGURES

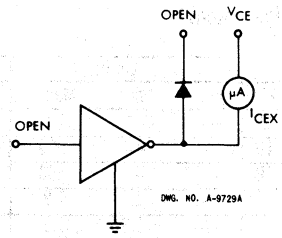


FIGURE 1A

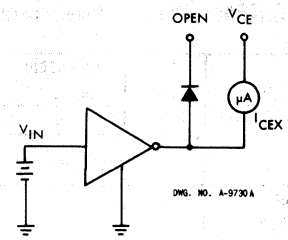


FIGURE 1B

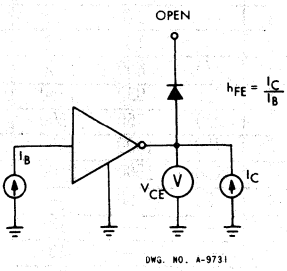


FIGURE 2

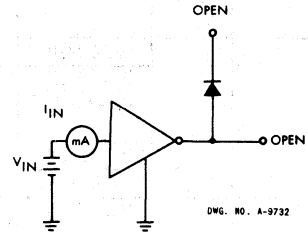


FIGURE 3

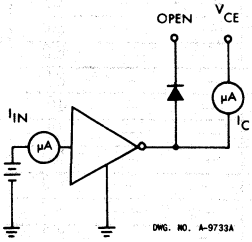


FIGURE 4

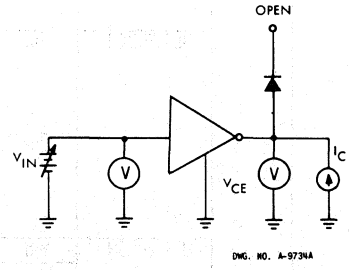


FIGURE 5

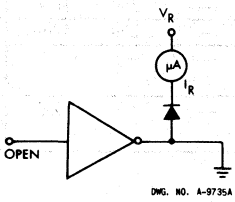


FIGURE 6

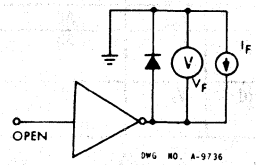
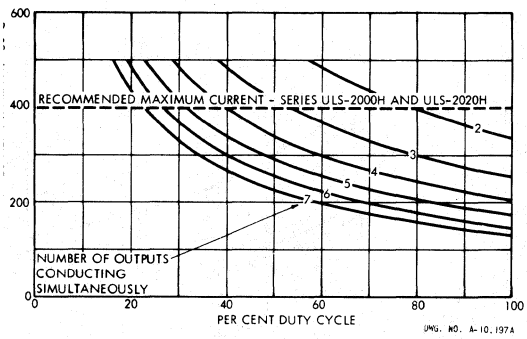
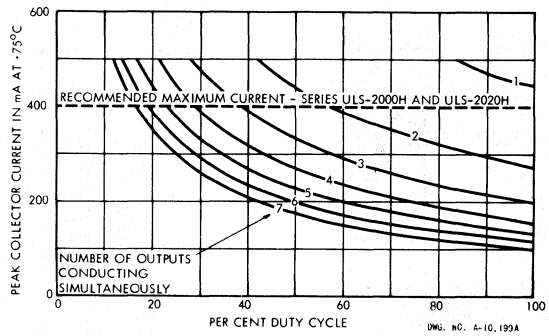


FIGURE 7

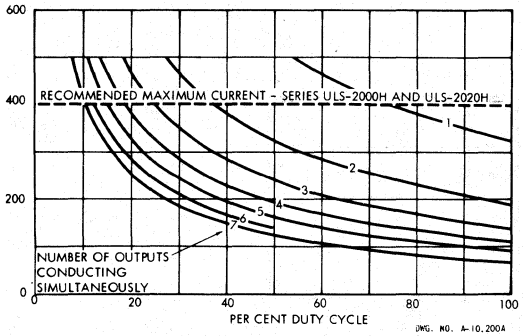
SERIES ULS-2000H



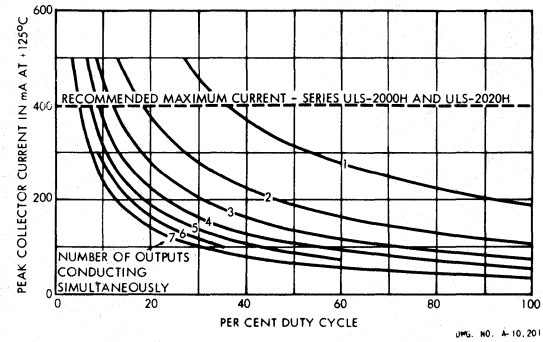
PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS AT +50°C



PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS AT +75°C

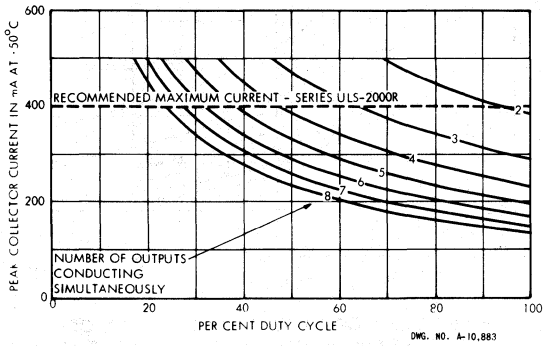


PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS AT +100°C

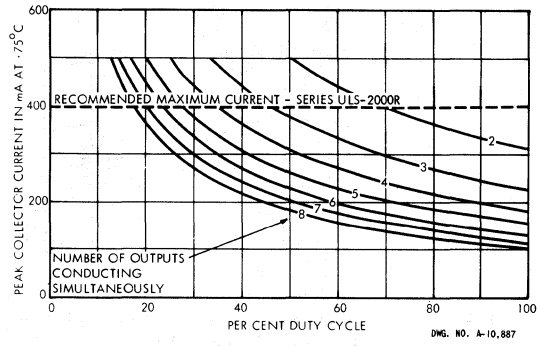


PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS AT +125°C

SERIES ULS-2000R

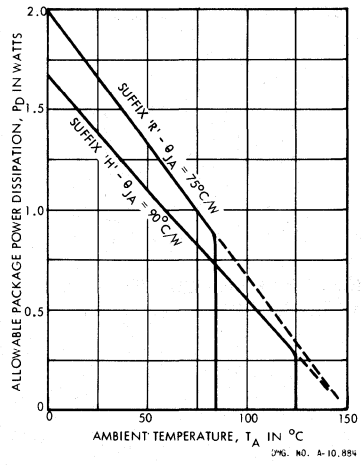


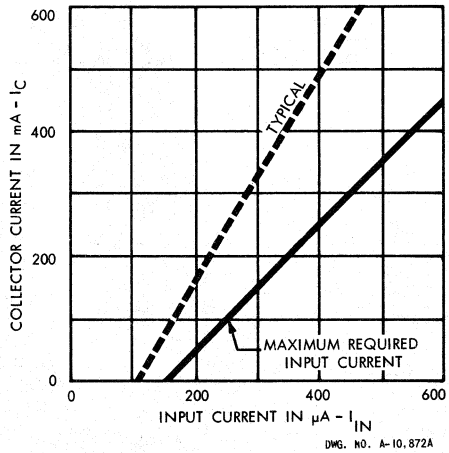
PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS AT +50°C



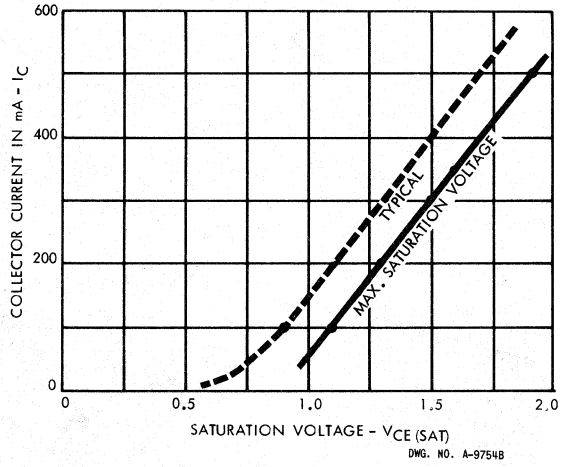
PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS AT +75°C

ALLOWABLE PACKAGE POWER DISSIPATION SERIES ULS-2000H and ULS-2000R





COLLECTOR CURRENT
AS A FUNCTION OF INPUT CURRENT

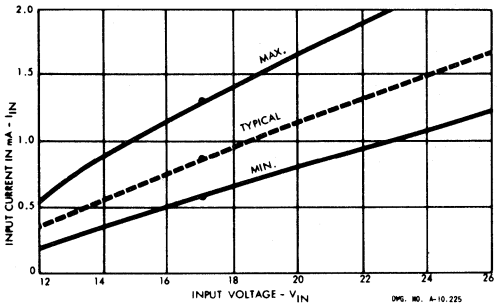


COLLECTOR CURRENT
AS A FUNCTION OF SATURATION VOLTAGE

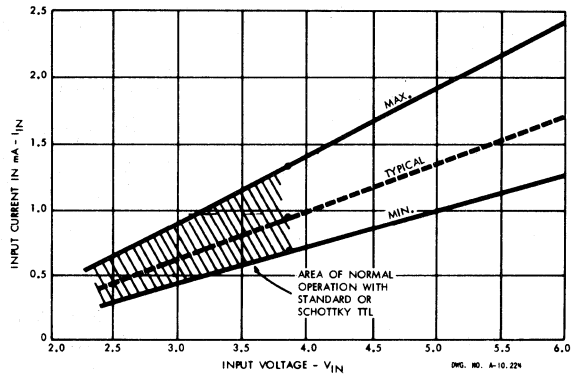
4

*Complete part number includes a final letter to indicate package. H = hermetic dual in-line, R = ceramic dual in-line.

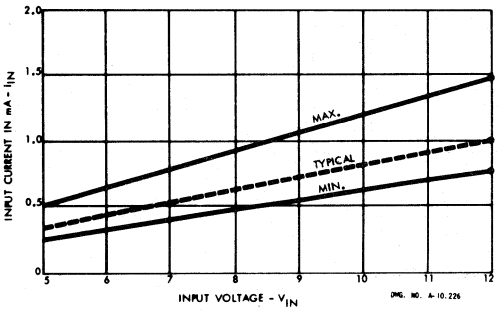
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



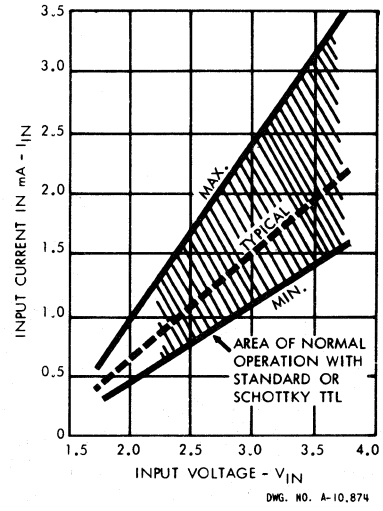
SERIES ULS-2002



SERIES ULS-2003



SERIES ULS-2004



SERIES ULS-2005

HERMETICALLY-SEALED DARLINGTON TRANSISTOR ARRAYS WITH MIL-STD-883 HIGH-RELIABILITY SCREENING

Hermetically-sealed Darlington arrays with high-reliability screening can be ordered by adding the suffix "MIL" to the part number, for example, ULS-2001H-MIL. If marking with the customers part number is necessary in place of the Sprague Electric part number, this must be stated on the purchase order with the marking desired.

Table I — 100% Production Screen Tests (All Hermetic Parts)
MIL-STD-883, Method 5004, Class B, Paragraphs 3.1.1 thru 3.1.6

Screen	MIL-STD-883 Test Method	Conditions
Internal Visual	2010, Cond. B	—
Stabilization Bake	1008, Cond. C	150°C, 24 Hours
Thermal Shock	1011, Cond. A	0 to 100°C, 15 Cycles
Constant Acceleration	2001, Cond. E	30,000 G's, Y1 Plane
Fine Seal	1014, Cond. A	5×10^{-7} Maximum
Gross Seal	1014, Cond. C	—
Electrical	—	Per specification
Marking	—	Sprague or customer part number, date code, lot identification, index point

Table II — 100% High-Reliability Screening ("MIL" Suffix Parts Only)
MIL-STD-883, Method 5004, Class B, Paragraphs 3.1.9 thru 3.1.15 and 3.1.18

Screen	MIL-STD-883 Test Method	Conditions
Interim Electrical	5005, Gp A, Subgp 1	25°C per specification
Burn-In	1015, Cond. A	125°C, 160 Hours
Static Electrical	5005, Gp A, Subgp 1	25°C per specification
	5005, Gp A, Subgp 2 & 3	−55°C & +125°C per specification
Dynamic & Functional Electrical	5005, Gp A, Subgp 4, 7 & 9	25°C per specification
Fine Seal	1014, Cond. A	5×10^{-7} Maximum
Gross Seal	1014, Cond. C	—
External Visual	2009	—

Table III — High-Reliability Qualification and Quality Conformance Inspection
MIL-STD-883, Method 5004, Class B, Paragraph 3.1.17

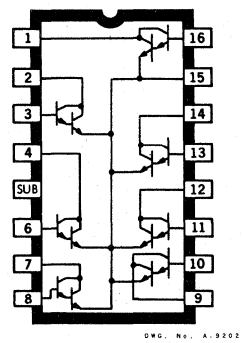
Test	MIL-STD-883 Test Method	Description
Group A Subgp. 1-4, 7 & 9	5005, Table I	Each production lot
Group B	5005, Table II	Each production lot
Group C	5005, Table III	End points, Gp. A, Subgp. 1, every 90 days
Group D	5005, Table IV	End points, Gp. A, Subgp. 1, every 6 months

TYPE ULN-2031A, ULN-2032A, AND ULN-2033A HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

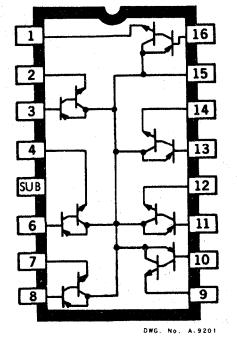
SPRAGUE TYPE ULN-2031A, ULN-2032A, and ULN-2033A High-Current Darlington Transistor Arrays are comprised of seven silicon Darlington pairs on a common monolithic substrate. The Type ULN-2031A consists of 14 NPN transistors connected to form seven Darlington pairs with NPN action. The Type ULN-2032A ($h_{FE} = 500$ min.) and the Type ULN-2033A ($h_{FE} = 50$ min.) consist of seven NPN and seven PNP transistors connected to form seven Darlington pairs with PNP action. All devices feature a common emitter configuration.

These devices are especially suited for interfacing between MOS, TTL, or DTL outputs and 7-segment LED or tungsten filament indicators. Peak inrush currents to 100mA are allowable. They are also ideal for a variety of other driver applications such as relay control and thyristor firing.

Type ULN-2031A, ULN-2032A, and ULN-2033A transistor arrays are housed in 16-lead DIP plastic packages which include a separate substrate connection for maximum circuit design flexibility.



ULN-2031A



ULN-2032A
ULN-2033A

ABSOLUTE MAXIMUM RATINGS at 25 C Free-Air Temperature (unless otherwise noted)

Power Dissipation (any one Darlington pair) 500mW
(total package) 750mW
Derating Factor Above 25 C ..... 6.67mW/°C
Ambient Temperature Range (operating), T_A ..... 0 C to +85 C
Storage Temperature Range, T_S ..... −55 C to +125 C
Individual Darlington Pair Ratings:
Collector-to-Emitter Voltage, V_{CEO} 16V
Collector-to-Base Voltage, V_{CBO} 40V
Collector-to-Substrate Voltage, V_{CIO} 40V
Emitter-to-Base Voltage, V_{EBO}
Type ULN-2031A 5V
Type ULN-2032A and ULN-2033A 40V
Continuous Collector Current, I_C 80mA
Continuous Base Current, I_B 5mA

NOTE:
The substrate must be connected to a voltage which is more negative than any collector or base voltage so as to maintain isolation between transistors, and to provide normal transistor action.

These devices are also available in industrial-grade hermetic packages with reduced package power capability. To order, change the last letter of the part number from 'A' to 'R'.

ELECTRICAL CHARACTERISTICS AT 25 C

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 500\mu A$	40	—	—	V
Collector-Substrate Breakdown Voltage	BV_{CIO}	$I_C = 500\mu A$	40	—	—	V
Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1mA$	16	—	—	V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 500\mu A$				
Type ULN-2031A			5	—	—	V
Type ULN-2032A and ULN-2033A			40	—	—	V
D-C Forward Current Transfer Ratio	h_{FE}	$V_{CE} = 2V$, $I_C = 20mA$				
Type ULN-2031A and ULN-2032A			500	—		—
Type ULN-2033A			50	—	500	—
Base-Emitter Saturation Voltage	$V_{BE(SAT)}$	$I_C = 20mA$, $I_B = 500\mu A$				
Type ULN-2031A			—	—	2	V
Type ULN-2032A and ULN-2033A			—	—	1	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$					
Type ULN-2031A and ULN-2032A		$I_C = 20mA$, $I_B = 40\mu A$	—	—	1.2	V
		$I_C = 80mA$, $I_B = 1mA$	—	—	1.5	V
Type ULN-2033A		$I_C = 20mA$, $I_B = 400\mu A$	—	—	1.2	V
		$I_C = 80mA$, $I_B = 2mA$	—	—	1.5	V
Collector Cutoff Current	I_{CEO}	$V_{CE} = 8V$	—	—	100	μA
	I_{CBO}	$V_{CB} = 10V$	—	—	10	μA

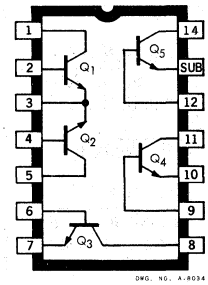
4

TYPE ULS-2045H AND ULN-2046A TRANSISTOR ARRAYS (Three Isolated Transistors and One Differential Amplifier)

THE ULS-2045H and ULN-2046A are general-purpose transistor arrays each consisting of five silicon N-P-N transistors on a single monolithic chip. Two transistors are internally connected to form a differential pair. Integrated circuit construction provides close electrical and thermal matching between each transistor.

These arrays are well-suited for a wide range of applications such as: d-c to VHF signal processing systems; temperature-compensated amplifiers; custom designed differential amplifiers and discrete transistors in conventional circuits.

Three package configurations are available. Type ULS-2045H is supplied in a hermetic 14-lead dual in-line ceramic package and is rated for operation over the military temperature range of −55°C to +125°C. Type ULN-2046A is electrically identical to the ULS-2045H but is supplied in a dual in-line plastic package rated for 0°C to +85°C ambients.



The ULS-2045H transistor array is also available in an industrial-grade hermetic package for operation over the temperature range of −40°C to +85°C. To order, change the 'H' in the part number to 'R'.

ABSOLUTE MAXIMUM RATINGS at 25 C Free-Air Temperature (unless otherwise noted)

	ULS-2045H		ULN-2046A		
	EACH TRANSISTOR	TOTAL PACKAGE	EACH TRANSISTOR	TOTAL PACKAGE	UNITS
Power Dissipation:					
T_A to +55°C			300	750	mW
T_A to +75°C	300	750	—	—	mW
Derating Factor:					
T_A > +55°C	—	—	—	6.67	mW/°C
T_A > +75°C	—	8	—	—	mW/°C

Collector-Base Voltage, $V_{(BR)CBO}$ 30V
Collector-Emitter Voltage, $V_{(BR)CEO}$ 20V
Collector-Substrate Voltage, $V_{(BR)CIO}$ (See note 2) 20V
Emitter-Base Voltage, $V_{(BR)EBO}$ 6V
Collector Current, I_C 50mA
Operating Temperature Range, T_A:
Type ULS-2045H ..... −55°C to +125°C
Type ULN-2046A ..... 0°C to +85°C
Storage Temperature Range, t_{sg} ..... −65°C to +150°C

Notes:

1. The maximum ratings are limiting absolute values above which the serviceability may be impaired from the viewpoint of life or satisfactory performance. The breakdown voltages may be far above the maximum voltage ratings. To avoid permanent damage to the transistor, do not attempt to measure these characteristics above the maximum ratings.
2. Pin 13 is connected to the substrate. This terminal must be tied to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25 C

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	20	60		V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	15	24		V
Collector-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_{CI} = 0$	20	60		V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$	5	7		V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$			40	nA
	I_{CEO}	$V_{CE} = 10V$, $I_B = 0$			0.5	μA
Static Forward Current Transfer Ratio	h_{FE}	$I_C = 10\mu A$, $V_{CE} = 3V$		54		—
		$I_C = 1mA$, $V_{CE} = 3V$	40	100		—
		$I_C = 10mA$, $V_{CE} = 3V$		100		—
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 10mA$, $I_B = 1mA$		0.23		V
Base-Emitter Voltage	V_{BE}	$I_E = 1mA$, $V_{CE} = 3V$		0.715		V
		$I_E = 10mA$, $V_{CE} = 3V$		0.800		V
Input Offset Current for Matched Pair Q_1 and Q_2	$\lvert I_{101} - I_{102} \rvert$	$I_C = 1mA$, $V_{CE} = 3V$		0.3	2	μA
Magnitude of Input Offset Voltage for Differential Pair	$\lvert V_{BE1} - V_{BE2} \rvert$	$I_C = 1mA$, $V_{CE} = 3V$		0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors	$\lvert V_{BE3} - V_{BE4} \rvert$	$I_C = 1mA$, $V_{CE} = 3V$		0.45	5	mV
	$\lvert V_{BE4} - V_{BE5} \rvert$	$I_C = 1mA$, $V_{CE} = 3V$		0.45	5	mV
	$\lvert V_{BE5} - V_{BE3} \rvert$	$I_C = 1mA$, $V_{CE} = 3V$		0.45	5	mV
Temperature Coefficient of Base-Emitter Voltage	$\frac{\triangle V_{BE}}{\triangle T}$	$I_C = 1mA$, $V_{CE} = 3V$		−1.9		mV/°C
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\triangle V_{IO}}{\triangle T}$	$I_C = 1mA$, $V_{CE} = 3V$		1.1		μV/°C

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DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25 C

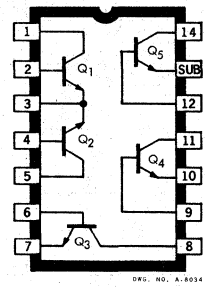
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Small-Signal Common-Emitter Forward Current Transfer Ratio	h_{fe}	$I_C = 1mA$, $V_{CE} = 3V$, $f = 1KHz$		110		—
Small-Signal Common-Emitter Short-Circuit Input Impedance	h_{ie}	$I_C = 1mA$, $V_{CE} = 3V$, $f = 1KHz$		3.5		KΩ
Small-Signal Common-Emitter Open-Circuit Output Impedance	h_{oe}	$I_C = 1mA$, $V_{CE} = 3V$, $f = 1KHz$		15.6		μmho
Small-Signal Common-Emitter Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}	$I_C = 1mA$, $V_{CE} = 3V$, $f = 1KHz$		1.8×10^{-4}		—
Gain-Bandwidth Product	f_T	$I_C = 3mA$, $V_{CE} = 3V$	300	550		MHz
Emitter-to-Base Capacitance	C_{EB}	$V_{EB} = 3V$, $I_E = 0$, $f = 1MHz$		0.6		pF
Collector-to-Base Capacitance	C_{CB}	$V_{CB} = 3V$, $I_C = 0$, $f = 1MHz$		0.6		pF
Collector-to-Substrate Capacitance	C_{CI}	$V_{CS} = 3V$, $I_C = 0$, $f = 1MHz$		2.8		pF
Noise Figure	N.F.	$I_C = 100\mu A$, $V_{CE} = 3V$, $R_g = 1K\Omega$ $f = 1KHz$, $BW = 15.7KHz$		3.25		dB

Note:
Characteristics apply for each transistor unless otherwise specified.

ULN-2046A-1 TRANSISTOR ARRAY

The ULN-2046A-1 general-purpose transistor array consists of five silicon NPN transistors, two of which are connected as a differential amplifier. The monolithic construction provides close electrical and thermal matching between all transistors.

Except as shown in the following electrical characteristics, the ULN-2046A-1 transistor array is identical to the ULN-2046A.



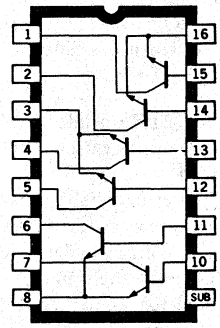
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 10\,\mu A$, $I_E = 0$	40	60	—	V
Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1$ mA, $I_B = 0$	30	—	—	V
Collector-Substrate Breakdown Voltage	BV_{CIO}	$I_C = 10\,\mu A$, $I_{CI} = 0$	40	60	—	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10$ V, $I_E = 0$	—	—	100	nA
	I_{CEO}	$V_{CE} = 10$ V, $I_B = 0$	—	—	5.0	μA
Static Forward Current Transfer Ratio	h_{FE}	$I_C = 1$ mA, $V_{CE} = 3$ V	30	100	—	

NOTE: Pin 13 is connected to the substrate. This terminal must be tied to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

TYPE ULN-2047A TRANSISTOR ARRAY
(Three Differential Amplifiers)

THE ULN-2047A is a silicon NPN multiple transistor array comprising three independent differential amplifiers. It is specifically intended for use in switching applications such as electronic organ keyboards. All base leads are brought out on one side of the 16-lead plastic dual in-line package to simplify printed wiring board layout. A separate substrate connection permits maximum circuit design flexibility.

The Type ULN-2047A Transistor Array is supplied in a 16-pin dual in-line plastic package.



DWG. NO. A-10,231

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

Power Dissipation, P_D (any one transistor) ..... 300 mW
(total package) ..... 750 mW*
Operating Temperature Range, T_A ..... 0°C to +85°C
Storage Temperature Range, T_S ..... −55°C to +150°C

*Derate at the rate of 6.67 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS at 25°C Free-Air Temperature

Collector-Emitter Breakdown Voltage, BV_{CEO} (note 1)
at I_C = 5 mA ..... 30 V Min.
Emitter Cutoff Current, I_{EBO} (note 2)
at V_{EB} = 5 V ..... 100 nA Max.
Collector Cutoff Current, I_{CES} (note 1)
at V_{CE} = 25 V ..... 100 nA Max.
D-C Forward Current Transfer Ratio, h_{FE} (note 1)
at V_{CE} = 2 V, I_C = 0.1 mA ..... 30 Min.
at V_{CE} = 2 V, I_C = 10 mA ..... 75 Min.
Differential Input Offset Voltage, V_{IO} (note 1)
at V_{CE} = 2 V, $I_{C1} = I_{C2}$ = 1 mA ..... 5 mV Max.

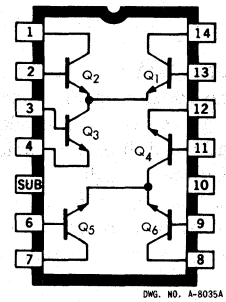
NOTES:
1. All other pins common to emitter of transistor under test.
2. Base and collector of associated transistor connected to emitter, all other pins common to base of transistor under test.

TYPE ULN-2054A TRANSISTOR ARRAY
(Dual Independent Differential Amplifiers)

THE ULN-2054A is a transistor array consisting of six silicon NPN transistors on a single monolithic chip. The transistors are internally interconnected to form two independent differential amplifiers.

The ULN-2054A is intended for a wide range of applications requiring extremely close electrical and thermal matching characteristics. Some applications are: cascade limiter circuits; balanced mixer circuits; balanced quadrature/synchronous detector circuits; balanced (push-pull) cascade/sense/IF amplifier circuits; or in almost any multifunction system requiring RF/Mixer/Oscillator, converter/IF functions.

Available in a 14-lead dual in-line plastic package the ULN-2054A is rated for operation over a 0°C to +85°C ambient temperature range.



DWG. NO. A-8035A

Other features are:

- Input Offset Voltage – 5mV max.
- Input Offset Current – 2 μA max.
- Voltage gain (single-stage double ended output) – 32 dB typ.
- Common-Mode Rejection Ratio (each amplifier) – 100 dB typ.

ABSOLUTE MAXIMUM RATINGS at 25 C Free-Air Temperature (unless otherwise noted)

Power Dissipation T_A to +55°C:
- Each Transistor 300mW
- Total Package 750mW

Derating Factor, Total Package, $T_A \geq 55°C$ ..... 6.67mW/°C
Collector-Base Voltage, $V_{(BR)CBO}$ 20V
Collector-Substrate Voltage, $V_{(BR)CIO}$ (See note 2) 20V
Collector-Emitter Voltage, $V_{(BR)CEO}$ 15V
Emitter-Base Voltage, $V_{(BR)EBO}$ 5V
Collector Current, I_C 50mA
Base Current I_B 5mA
Operating Temperature Range, T_A ..... 0°C to +85°C
Storage Temperature Range, t_{sq} ..... −65°C to +150°C

Notes:
1. The maximum ratings are limiting absolute values above which the serviceability may be impaired from the viewpoint of life or satisfactory performance. The breakdown voltages may be far above the maximum voltage ratings. To avoid permanent damage to the transistor, do not attempt to measure these characteristics above the maximum ratings.
2. Pin 5 is connected to the substrate. This terminal must be tied to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

STATIC ELECTRICAL CHARACTERISTICS: at $T_A = 25°C$

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A$, $I_E = 0$	20	60		V
Collector-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A$, $I_{C1} = 0$	20	60		V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA$, $I_B = 0$	15	24		V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A$, $I_C = 0$	5	7		V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10V$, $I_E = 0$			100	nA
Base-Emitter Voltage	V_{BE}	$I_C = 50\mu A$, $V_{CB} = 3V$		0.630	0.700	V
		$I_C = 1mA$, $V_{CB} = 3V$		0.715	0.800	V
		$I_C = 3mA$, $V_{CB} = 3V$		0.750	0.850	V
		$I_C = 10mA$, $V_{CB} = 3V$		0.800	0.900	V
Temperature Coefficient of Base-Emitter Voltage	$\frac{\triangle V_{BE}}{\triangle T}$	$I_C = 1mA$, $V_{CB} = 3V$		−1.9		mV/°C
Input Offset Voltage	V_{IO}	$I_{E(Q3)} = I_{E(Q4)} = 2mA$, $V_{CB} = 3V$		0.45	5	mV
Input Offset Current	O_{IO}	$I_{E(Q3)} = I_{E(Q4)} = 2mA$, $V_{CB} = 3V$		0.3	2	μA
Input Bias Current	I_I	$I_{E(Q3)} = I_{E(Q4)} = 2mA$, $V_{CB} = 3V$		10	24	μA
Quiescent Operating Current Ratio	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$	$I_{E(Q3)} = 2mA$, $V_{CB} = 3V$		0.98-1.02		—
	$\frac{I_{C(Q5)}}{I_{C(Q6)}}$	$I_{E(Q4)} = 2mA$, $V_{CB} = 3V$		0.98-1.02		—
Temperature Coefficient Magnitude of Input-Offset Voltage	$\left\lvert\frac{\triangle V_{IO}}{\triangle T}\right\rvert$	$I_{E(Q3)} = I_{E(Q4)} = 2mA$, $V_{CB} = 3V$		1.1		$\mu V/°C$

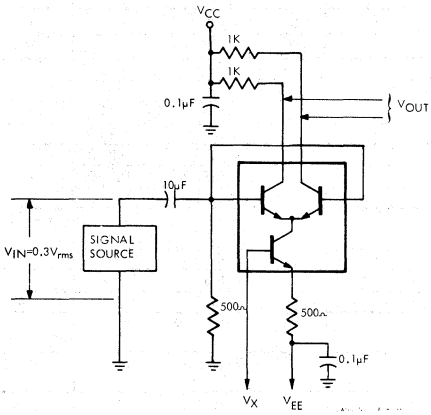
4

DYNAMIC ELECTRICAL CHARACTERISTICS: at $T_A = 25°C$

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Common-Mode Rejection Ratio For each Amplifier	CMR	$V_{CC} = 12V$, $V_{EE} = -6V$, $V_X = 3.3V$, $f = 1kHz$ (See figure 1)		100		dB
AGC Range, One Stage	AGC	$V_{CC} = 12V$, $V_{EE} = -6V$, $V_X = 3.3V$, $f = 1kHz$ (See figure 2)		75		dB
Voltage Gain, Single Stage Double-Ended Output	A	$V_{CC} = 12V$, $V_{EE} = -6V$, $V_X = 3.3V$, $f = 1kHz$ (See figure 2)		32		dB
AGC Range, Two Stage	AGC	$V_{CC} = 12V$, $V_{EE} = -6V$, $V_X = 3.3V$, $f = 1kHz$ (See figure 3)		105		dB
Voltage Gain, Two Stage Double-Ended Output	A	$V_{CC} = 12V$, $V_{EE} = -6V$, $V_X = 3.3V$, $f = 1kHz$ (See figure 3)		60		dB
Small-Signal Common-Emitter Forward Current Transfer Ratio	h_{fe}	$I_C = 1mA$, $V_{CE} = 3V$, $f = 1kHz$		110		—
Small-Signal Common-Emitter Short-Circuit Input Impedance	h_{ie}	$I_C = 1mA$, $V_{CE} = 3V$, $f = 1kHz$		3.5		KΩ
Small-Signal Common-Emitter Open-Circuit Output Impedance	h_{oe}	$I_C = 1mA$, $V_{CE} = 3V$, $f = 1kHz$		15.6		μmho
Small-Signal Common-Emitter Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}	$I_C = 1mA$, $V_{CE} = 3V$, $f = 1kHz$		1.8×10^{-4}		—
Gain-Bandwidth Product (for Single Transistor)	f_T	$I_C = 3mA$, $V_{CE} = 3V$		550		MHz
Noise Figure (for Single Transistor)	N.F.	$V_{CE} = 3V$, $f = 1kHz$, $I_C = 100\mu A$, $R_g = 1K\Omega$, $BW = 15.7$ kHz		3.25		dB
Noise Figure (for each Amplifier)	N.F.	$f = 100MHz$		8		dB

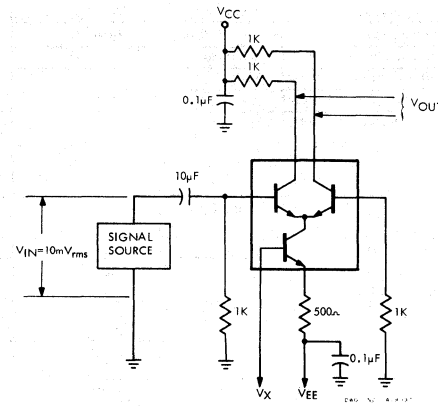
Note:
Characteristics apply for each transistor unless otherwise specified.

AMPLIFIER TEST CIRCUITS



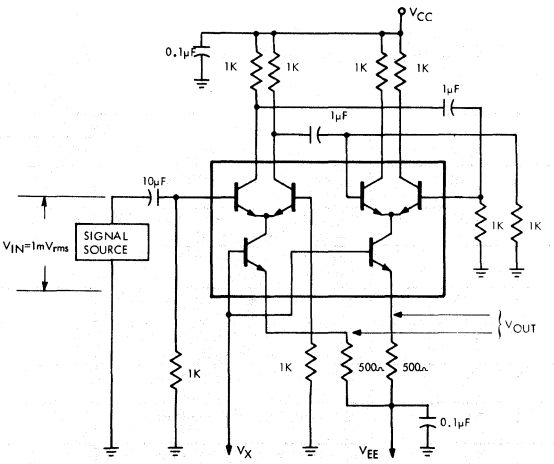
COMMON MODE REJECTION RATIO

Figure 1



SINGLE-STAGE VOLTAGE GAIN

Figure 2



TWO-STAGE VOLTAGE GAIN

Figure 3

TYPE ULN-2061M thru ULN-2077B
1.5 A DARLINGTON SWITCHES

THESE HIGH-VOLTAGE, HIGH-CURRENT Darlington arrays are monolithic bipolar devices especially designed for switching applications and may control loads of up to 480 watts (1.5 A per output, 80 V, 26% duty cycle).

The ULN-2061M thru ULN-2077B devices are intended for interfacing from low-level logic to peripheral loads such as relays, solenoids, d-c and stepping motors, multiplexed LED and incandescent displays, heaters, and similar high-voltage, high-current loads.

All standard types are specified with a guaranteed minimum output breakdown of 50 volts and a $V_{CE(SUS)}$ limit of 35 volts (min) measured at 100mA. In addition, all types are available with a minimum output breakdown of 80 volts; a guaranteed $V_{CE(SUS)}$ of 50 volts; and an output current specification of 1.5 A (saturated). Most types also include integral transient suppression diodes for inductive loads and inputs are compatible with TTL, DTL, LS TTL, 5 V to 15 V CMOS, and PMOS. Isolated Darlington types are available for emitter follower or similar uses which do not allow common emitter versions.

The dual driver Type ULN-2061/62M arrays are used for either common-emitter (externally connected) or emitter-follower applications. The ULN-2062M is the higher-voltage version of the ULN-2061M. Both of these devices are supplied in an 8-pin plastic mini-DIP package.

Quad driver Types ULN-2064/65B and ULN-2068/69B are intended for use with TTL, low-speed TTL, and 5 V MOS logic. For those applications requiring high gain (low input current loading), the ULN-2068/69B are most suitable. The ULN-2065/69B are selected for the 80 V minimum output breakdown voltage specification.

The Types ULN-2066/67B and ULN-2070/71B are similar to the preceding quad driver types except that they are recommended for use with PMOS and 12 V CMOS logic. The ULN-2070/71B devices are for use where input current is restricted by MOS output ratings.

Types ULN 2068/69B utilize a predriver stage requiring a 5 V supply rail; types ULN 2070/71B also incorporate the additional gain stage and utilize a 12 V supply (nominal). Use of these types reduces input drive requirements, while allowing the output to switch currents to 1.5 A.

Isolated Darlington arrays, Type ULN-2074B thru ULN-2077B, are identical to the Type 2064B thru ULN-2067B, respectively, except for the isolated Darlington pin-out and the deletion of suppression diodes. They are intended primarily for use in emitter-follower or similar isolated Darlington applications.

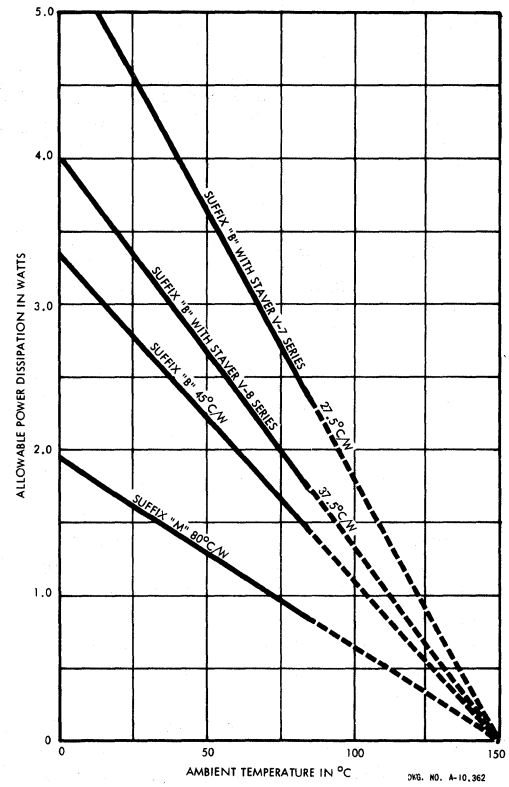
All of the quad Darlington arrays (suffix "B" devices) are supplied in an improved 16-lead plastic dual in-line package with heat-sink contact tabs. A copper alloy lead frame allows maximum power dissipation with standard cooling methods. Further increases in package power dissipation can be obtained by attaching an external heat sink to the webbed leads. This unique lead configuration, originated by Sprague Electric, allows easy attachment of the heat sink and yet permits the use of a standard IC socket or printed wiring board layout.

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature for any one driver (unless otherwise noted)

Output Voltage, V_{CEX} ..... see below
Output Sustaining Voltage, $V_{CE(SUS)}$ ..... see below
Output Current, I_{OUT} (note 1) ..... 1.75 A
Input Voltage, V_{IN} (note 2) ..... see below
Input Current, I_B (note 3) ..... 25 mA
Supply Voltage, V_S (ULN-2068/69B) ..... 10 V
(ULN-2070/71B) ..... 20 V
Total Package Power Dissipation (ULN-2061/62M) ... 1.56 W*
(all suffix 'B' devices) ..... 2.77 W*
Operating Ambient Temperature Range, T_A
..... 0°C to +70°C
Storage Temperature Range, T_S ..... −55°C to +150°C

*Derate linearly to 0 W at +150°C.

$R\phi_{JA}$	$G\phi_{JA}$
80°C/W	12.5 mW/°C
45°C/W	22.2 mW/°C
37.5°C/W	26.7 mW/°C
27.5°C/W	36.4 mW/°C



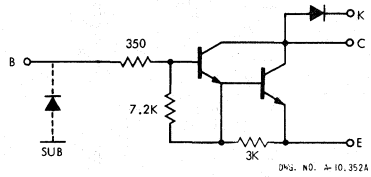
Type Number	V_{CEX} (Max.)	$V_{CE(SUS)}$ (Max.)	V_{IN} (Max.)	Application
ULN-2061M	50 V	35 V	30 V	TTL, DTL, Schottky TTL,
ULN-2062M	80 V	50 V	60 V	and 5 V CMOS
ULN-2064B	50 V	35 V	15 V	TTL, DTL, Schottky TTL,
ULN-2065B	80 V	50 V	15 V	and 5 V CMOS
ULN-2066B	50 V	35 V	30 V	6 to 15 V CMOS
ULN-2067B	80 V	50 V	30 V	and PMOS
ULN-2068B	50 V	35 V	15 V	TTL, DTL, Schottky TTL,
ULN-2069B	80 V	50 V	15 V	and 5 V CMOS
ULN-2070B	50 V	35 V	30 V	6 to 15 V CMOS
ULN-2071B	80 V	50 V	30 V	and PMOS
ULN-2074B	50 V	35 V	30 V	General Purpose
ULN-2075B	80 V	50 V	60 V	
ULN-2076B	50 V	35 V	30 V	6 to 15 V CMOS
ULN-2077B	80 V	50 V	60 V	and PMOS

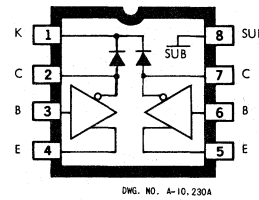
Notes:

1. Allowable combinations of output current, number of outputs conducting, and duty cycle are shown on pages 4-38 and 4-39.
2. Input voltage is with reference to the substrate (no connection to any other pins) for the ULN-2061/62M and ULN-2074/75/76/77B; reference is ground for all other types.
3. Input current may be limited by maximum allowable input voltage.

TYPE ULN-2061M & ULN-2062M

PARTIAL SCHEMATIC





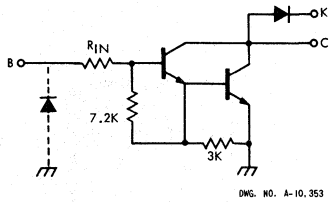
ELECTRICAL CHARACTERISTICS AT 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	1	ULN-2061M	V_{CE} = 50 V	—	100	μA
				V_{CE} = 50 V, T_A = 70°C	—	500	μA
			ULN-2062M	V_{CE} = 80 V	—	100	μA
				V_{CE} = 80 V, T_A = 70°C	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN-2061M	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
			ULN-2062M	I_C = 100 mA, V_{IN} = 0.4 V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	I_C = 500 mA, I_B = 625 μA	—	1.0	V
				I_C = 750 mA, I_B = 935 μA	—	1.13	V
				I_C = 1.0 A, I_B = 1.25 mA	—	1.25	V
			ULN-2061M	I_C = 1.25 A, I_B = 2.0 mA	—	1.4	V
			ULN-2062M	I_C = 1.5 A, I_B = 2.25 mA	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	V_{IN} = 2.4 V	2.0	4.3	mA
				V_{IN} = 3.75 V	4.5	9.6	mA
Input Voltage	$V_{IN(ON)}$	5	Both	V_{CE} = 2.0 V, I_C = 1.0 A	—	2.0	V
				V_{CE} = 2.0 V, I_C = 1.5 A	—	2.5	V
Turn-On Delay	t_{PLH}	–	Both	0.5 E_{in} to 0.5 E_{out}	—	1.0	μs
Turn-Off Delay	t_{PHL}	–	Both	0.5 E_{in} to 0.5 E_{out}	—	1.5	μs
Clamp Diode Leakage Current	I_R	6	ULN-2061M	V_R = 50 V	—	50	μA
				V_R = 50 V, T_A = 70°C	—	100	μA
			ULN-2062M	V_R = 80 V	—	50	μA
				V_R = 80 V, T_A = 70°C	—	100	μA
Clamp Diode Forward Voltage	V_F	7	Both	I_F = 1.0 A	—	1.75	V
				I_F = 1.5 A	—	2.0	V

4

TYPE ULN-2064B THRU ULN-2067B

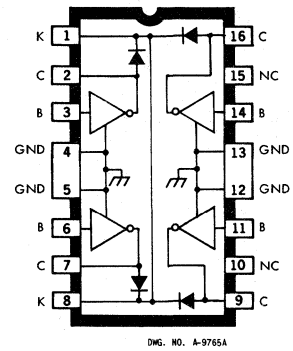
PARTIAL SCHEMATIC



ULN-2064B, ULN-2065B } R_{IN} = 350Ω

ULN-2066B, ULN-2067B } R_{IN} = 3kΩ

(SIMILAR TO ULN-2074B THRU ULN-2077B

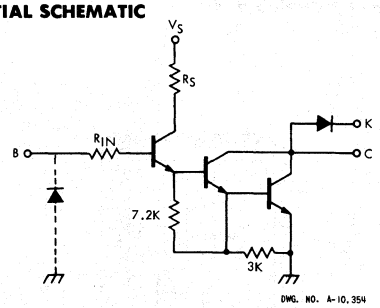


ELECTRICAL CHARACTERISTICS AT 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	1	ULN-2064/66B	V_{CE} = 50 V	—	100	μA
				V_{CE} = 50 V, T_A = 70°C	—	500	μA
			ULN-2065/67B	V_{CE} = 80 V	—	100	μA
				V_{CE} = 80 V, T_A = 70°C	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN-2064/66B	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
			ULN-2065/67B	I_C = 100 mA, V_{IN} = 0.4 V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	All	I_C = 500 mA, I_B = 625 μA	—	1.0	V
				I_C = 750 mA, I_B = 935 μA	—	1.13	V
				I_C = 1.0 A, I_B = 1.25 mA	—	1.25	V
			ULN-2064/66B	I_C = 1.25 A, I_B = 2.0 mA	—	1.4	V
			ULN-2065/67B	I_C = 1.5 A, I_B = 2.25 mA	—	1.5	V
Input Current	$I_{IN(ON)}$	4	ULN-2064/65B	V_{IN} = 2.4 V	2.0	4.3	mA
				V_{IN} = 3.75 V	4.5	9.6	mA
			ULN-2066/67B	V_{IN} = 5.0 V	0.9	1.8	mA
				V_{IN} = 12 V	2.75	5.2	mA
Input Voltage	$V_{IN(ON)}$	5	ULN-2064/65B	V_{CE} = 2.0 V, I_C = 1.0 A	—	2.0	V
				V_{CE} = 2.0 V, I_C = 1.5 A	—	2.5	V
			ULN-2066/67B	V_{CE} = 2.0 V, I_C = 1.0 A	—	6.5	V
				V_{CE} = 2.0 V, I_C = 1.5 A	—	10	V
Turn-On Delay	t_{PLH}	–	All	0.5 E_{in} to 0.5 E_{out}	—	1.0	μs
Turn-Off Delay	t_{PHL}	–	All	0.5 E_{in} to 0.5 E_{out}	—	1.5	μs
Clamp Diode Leakage Current	I_R	6	ULN-2064/66B	V_R = 50 V	—	50	μA
				V_R = 50 V, T_A = 70°C	—	100	μA
			ULN-2065/67B	V_R = 80 V	—	50	μA
				V_R = 80 V, T_A = 70°C	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 1.0 A	—	1.75	V
				I_F = 1.5 A	—	2.0	V

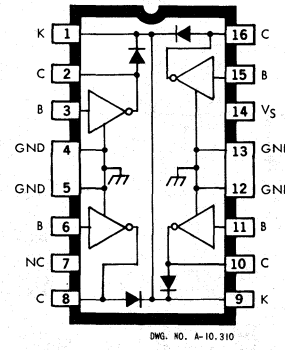
TYPE ULN-2068B THRU ULN-2071B

PARTIAL SCHEMATIC



ULN-2068B, ULN-2069B } R_{IN} = 2.5kΩ, R_S = 900Ω

ULN-2070B, ULN-2071B } R_{IN} = 11.6kΩ, R_S = 3.4kΩ

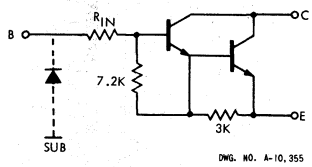


ELECTRICAL CHARACTERISTICS AT 25°C (unless otherwise noted)
Vs = 5.0 V (ULN-2068/69B) OR Vs=12 V (ULN-2070/71B)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	1	ULN-2068/70B	V_{CE} = 50 V	—	100	μA
				V_{CE} = 50 V, T_A = 70°C	—	500	μA
			ULN-2069/71B	V_{CE} = 80 V	—	100	μA
				V_{CE} = 80 V, T_A = 70°C	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN-2068/70B	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
			ULN-2069/71B	I_C = 100 mA, V_{IN} = 0.4 V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	ULN-2068/69B	I_C = 500 mA, V_{IN} = 2.4 V	—	1.0	V
				I_C = 750 mA, V_{IN} = 2.4 V	—	1.13	V
				I_C = 1.0 A, V_{IN} = 2.4 V	—	1.25	V
				I_C = 1.25 A, V_{IN} = 2.4 V	—	1.4	V
			ULN-2069B	I_C = 1.5 A, V_{IN} = 2.4 V	—	1.5	V
			ULN-2070/71B	I_C = 500 mA, V_{IN} = 5.0 V	—	1.0	V
				I_C = 750 mA, V_{IN} = 5.0 V	—	1.13	V
				I_C = 1.0 A, V_{IN} = 5.0 V	—	1.25	V
				I_C = 1.25 A, V_{IN} = 5.0 V	—	1.4	V
			ULN-2071B	I_C = 1.5 A, V_{IN} = 5.0 V	—	1.5	V
Input Current	$I_{IN(ON)}$	4	ULN-2068/69B	V_{IN} = 2.4 V	—	250	μA
				V_{IN} = 3.75 V	—	1000	μA
			ULN-2070/71B	V_{IN} = 5.0 V	—	400	μA
				V_{IN} = 12 V	—	1250	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2068/69B	V_{CE} = 2.0 V, I_C = 1.5 A	—	2.75	V
			ULN-2070/71B	V_{CE} = 2.0 V, I_C = 1.5 A	—	5.0	V
Supply Current	I_S	8	ULN-2068/69B	I_C = 500 mA, V_{IN} = 2.4 V	—	6.0	mA
			ULN-2070/71B	I_C = 500 mA, V_{IN} = 5.0 V	—	4.5	mA
Turn-On Delay	t_{PLH}	–	All	0.5 E_{in} to 0.5 E_{out}	—	1.0	μs
Turn-Off Delay	t_{PHL}	–	All	0.5 E_{in} to 0.5 E_{out}	—	1.5	μs
Clamp Diode Leakage Current	I_R	6	ULN-2068/70B	V_R = 50 V	—	50	μA
				V_R = 50 V, T_A = 70°C	—	100	μA
			ULN-2069/71B	V_R = 80 V	—	50	μA
				V_R = 80 V, T_A = 70°C	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 1.0 A	—	1.75	V
				I_F = 1.5 A	—	2.0	V

TYPE ULN-2074B THRU ULN-2077B

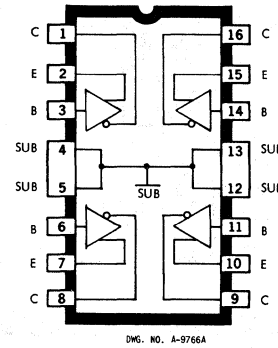
PARTIAL SCHEMATIC



ULN-2074B
ULN-2075B } R_{IN} = 350Ω

ULN-2076B
ULN-2077B } R_{IN} = 3kΩ

(SIMILAR TO ULN-2064B THRU ULN-2067B)



ELECTRICAL CHARACTERISTICS AT 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	1	ULN-2074/76B	V_{CE} = 50 V	—	100	μA
				V_{CE} = 50 V, T_A = 70°C	—	500	μA
			ULN-2075/77B	V_{CE} = 80 V	—	100	μA
				V_{CE} = 80 V, T_A = 70°C	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN-2074/76B	I_C = 100 mA, V_{IN} = 0.4 V	35	—	V
			ULN-2075/77B	I_C = 100 mA, V_{IN} = 0.4 V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	All	I_C = 500 mA, I_B = 625 μA	—	1.0	V
				I_C = 750 mA, I_B = 935 μA	—	1.13	V
				I_C = 1.0 A, I_B = 1.25 mA	—	1.25	V
			*ULN-2074/76B	I_C = 1.25 A, I_B = 2.0 mA	—	1.4	V
			ULN-2075/77B	I_C = 1.5 A, I_B = 2.25 mA	—	1.5	V
Input Current	$I_{IN(ON)}$	4	ULN-2074/75B	V_{IN} = 2.4 V	2.0	4.3	mA
				V_{IN} = 3.75 V	4.5	9.6	mA
			ULN-2076/77B	V_{IN} = 5.0 V	0.9	1.8	mA
				V_{IN} = 12 V	2.75	5.2	mA
Input Voltage	$V_{IN(ON)}$	5	ULN-2074/75B	V_{CE} = 2.0 V, I_C = 1.0 A	—	2.0	V
				V_{CE} = 2.0 V, I_C = 1.5 A	—	2.5	V
			ULN-2076/77B	V_{CE} = 2.0 V, I_C = 1.0 A	—	6.5	V
				V_{CE} = 2.0 V, I_C = 1.5 A	—	10	V
Turn-On Delay	t_{PLH}	–	All	0.5 E_{in} to 0.5 E_{out}	—	1.0	μs
Turn-Off Delay	t_{PHL}	–	All	0.5 E_{in} to 0.5 E_{out}	—	1.5	μs

TEST FIGURES

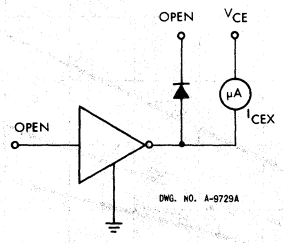


Figure 1

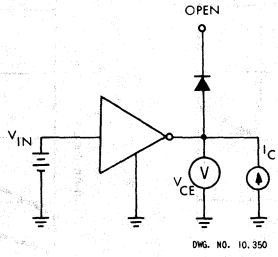


Figure 2

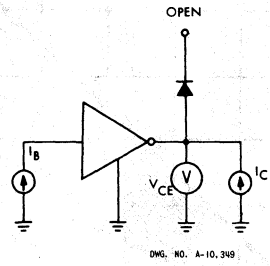


Figure 3

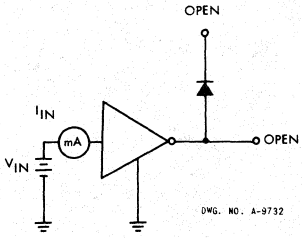


Figure 4

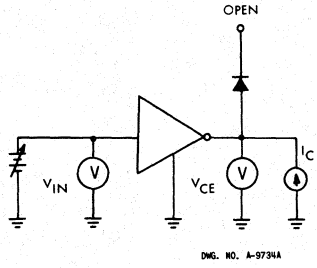


Figure 5

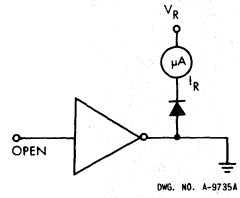


Figure 6

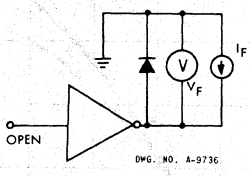


Figure 7

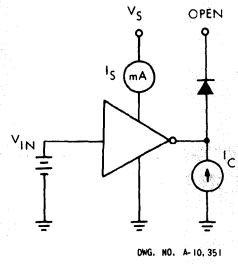
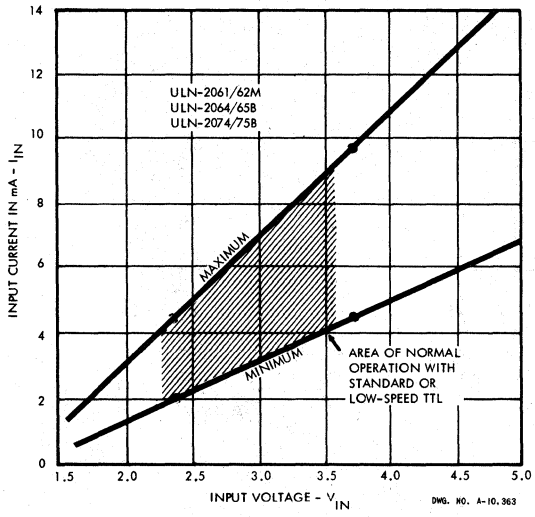
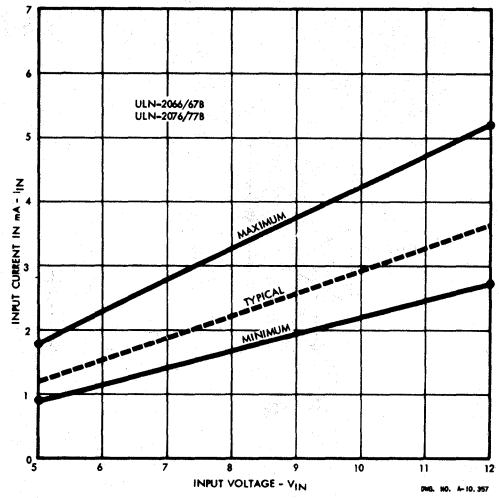


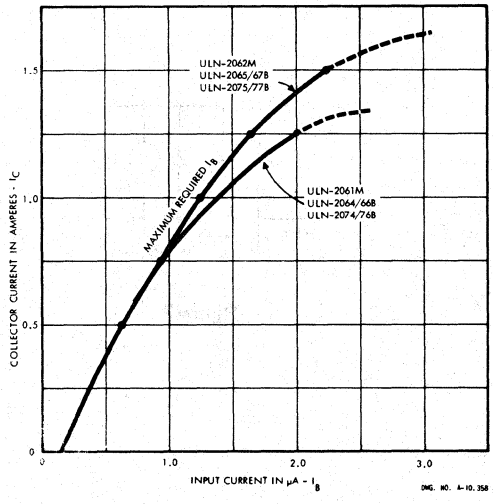
Figure 8



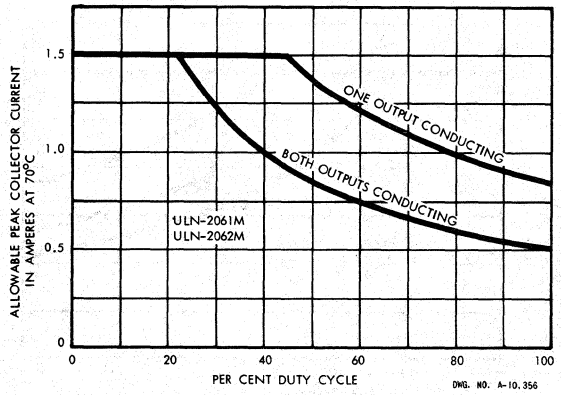


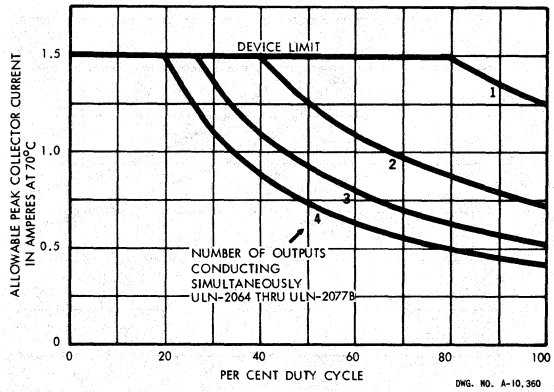
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

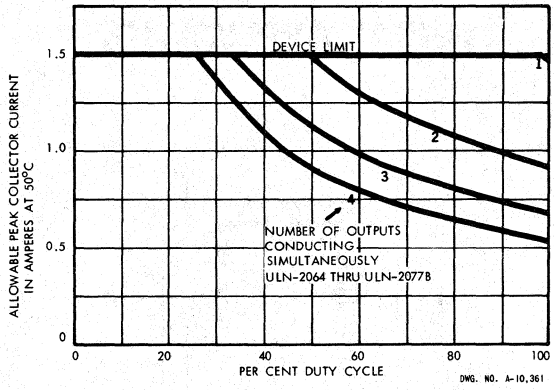
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT

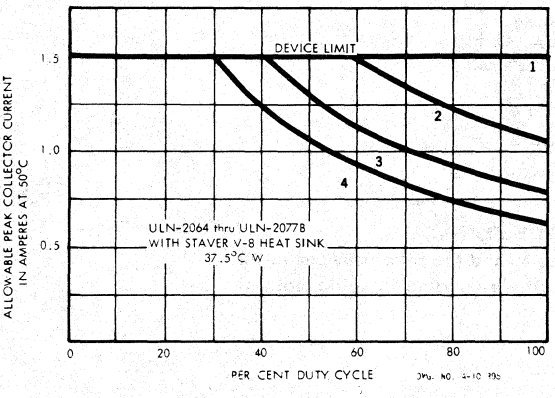


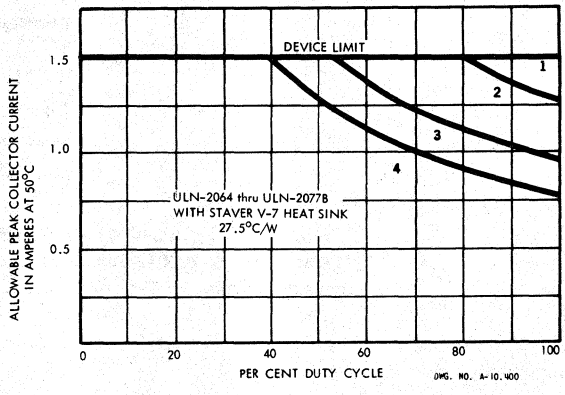
PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS



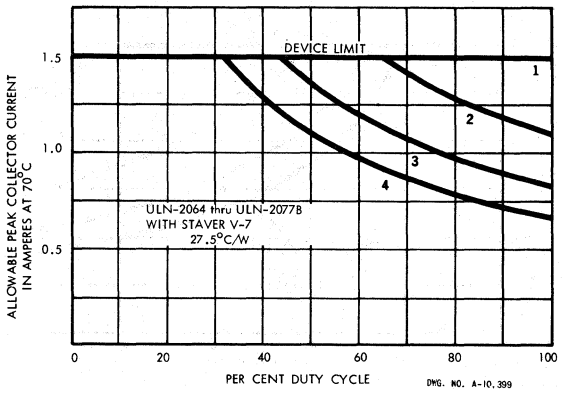


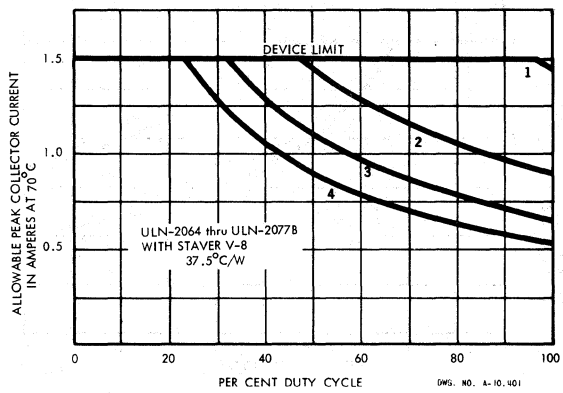




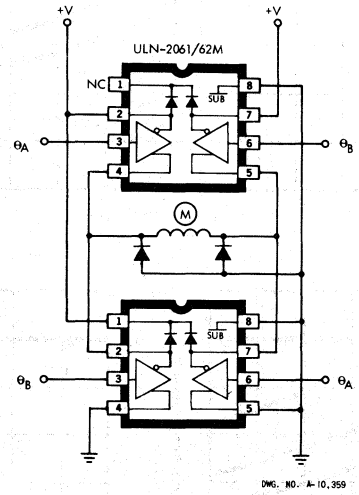


PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS





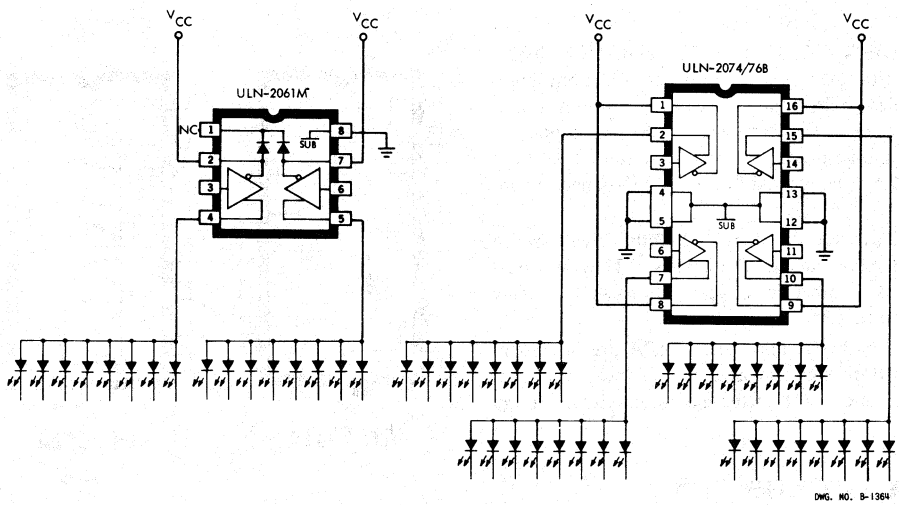
TYPICAL APPLICATION



BIDIRECTIONAL MOTOR CONTROL

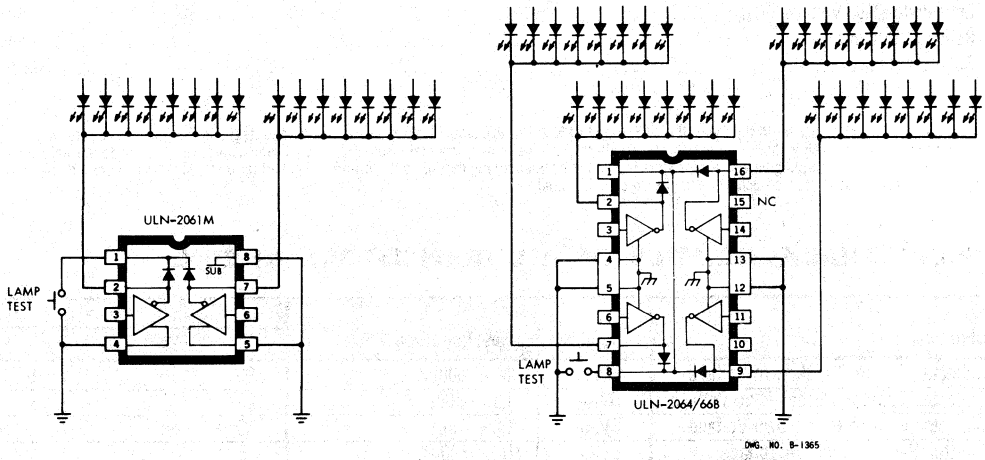
(The Series ULN-2000A, Series UDN-2980A, and the other devices in this series are recommended for use with multiple-winding stepping motors)

TYPICAL APPLICATIONS



COMMON-ANODE LED DRIVERS
(The Series UDN-2980A devices can also be used in similar applications for currents to 500 mA)

4



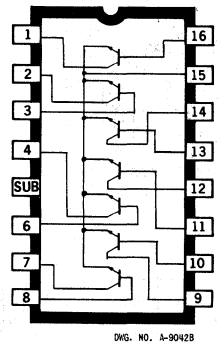
COMMON-CATHODE LED DRIVERS
(Types ULN-2068/70B are also applicable)

TYPE ULN-2081A AND ULN-2082A GENERAL PURPOSE HIGH CURRENT TRANSISTOR ARRAYS

SPRAGUE TYPE ULN-2081A and ULN-2082A Transistor Arrays are comprised of seven high-current silicon NPN transistors on a common monolithic substrate. The Type ULN-2081A is connected in a common-emitter configuration and the Type ULN-2082A is connected in a common-collector configuration.

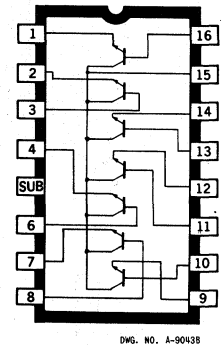
Both arrays are capable of directly driving seven segment displays and LED displays. They are ideal for a variety of other driver applications such as relay control and thyristor firing.

Type ULN-2081A and ULN-2082A are housed in 16-lead DIP plastic packages which include a separate substrate connection for maximum circuit design flexibility.



DWG. NO. A-9042B

ULN-2081A



DWG. NO. A-9043B

ULN-2082A

MAXIMUM RATINGS

Power Dissipation (any one transistor) 500mW
(total package) 750mW
Ambient Temperature Range (operating) ..... −40°C to +85°C
Individual Transistor Ratings:
Collector-to-Emitter Voltage, V_{CEO} 16V
Collector-to-Base Voltage, V_{CBO} 20V
Collector-to-Substrate Voltage, V_{CIO} 20V
Emitter-to-Base Voltage, V_{EBO} 5V
Collector Current, I_C 200mA
Base Current, I_B 20mA

NOTE:
The collector of each transistor in the Type ULN-2081A and ULN-2082A is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage so as to maintain isolation between transistors, and to provide normal transistor action. Undesired coupling between transistors is avoided by maintaining the substrate terminal (5) at either d-c or signal (a-c) ground. An appropriate bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS OF ALL TRANSISTORS at 25°C

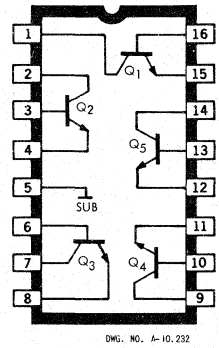
Characteristic	Symbol	Test Conditions	Limits Min.	Typ.	Max.	Units
Collector-Emitter Breakdown Voltage	BV_{CES}	I_C = 500μA	20	80		V
Collector-Substrate Breakdown Voltage	BV_{CIE}	I_{CI} = 500μA	20	80		V
Collector-Emitter Breakdown Voltage	BV_{CEO}	I_C = 1mA	16	40		V
Emitter-Base Breakdown Voltage	BV_{EBO}	I_C = 500μA	5	7		V
Forward Current Transfer Ratio	h_{FE}	V_{CE} = 0.5V, I_C = 30mA	30	80		
		V_{CE} = 0.8V, I_C = 50mA	40	85		
Base-Emitter Saturation Voltage	$V_{BE(SAT)}$	I_C = 30mA		0.75	1	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 30mA		0.13	0.5	V
		I_C = 50mA		0.2	0.7	V
Collector Cutoff Current	I_{CEO}	V_{CE} = 10V			10	μA
	I_{CBO}	V_{CB} = 10V			1	μA

TYPE ULN-2083A AND ULS-2083H TRANSISTOR ARRAYS (Five Independent NPN Transistors)

DESIGNED for use in general purpose, medium current (to 100 mA) switching and differential amplifier applications, the ULN-2083A and ULS-2083H transistor arrays each consist of five NPN transistors on a single monolithic chip. Two transistors are matched at low currents (1 mA) making them ideal for use in balanced mixer circuits, push-pull amplifiers, and other circuit functions requiring close thermal and offset matching.

A separate substrate connection permits maximum circuit design flexibility. In order to maintain isolation between transistors and provide normal transistor action, the substrate must be connected to a voltage which is more negative than any collector voltage. The substrate terminal (pin 5) should therefore be maintained at either d-c ground or suitably bypassed to a-c ground to avoid undesired coupling between transistors.

Two package configurations are available. The Type ULN-2083A is supplied in a 16-lead dual in-line plastic package for operation over the temperature range of 0°C to +85°C. This package is similar to JEDEC style MO-001AC. The Type ULS-2083H is electrically identical to the ULN-2083A but is supplied in a hermetic dual in-line package for operation over the temperature range of −55°C to +125°C. This package conforms to the dimensional requirements of Military Specification MIL-M-38510 and can meet all of the applicable environmental requirements of Military Standard MIL-STD-883.



DWG. NO. A-10,232

4

ELECTRICAL CHARACTERISTICS AT 25°C Free-Air Temperature

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Collector-Base Breakdown Voltage	BV_{CBO}	I_C = 100 μA	20	60	—	V
Collector-Emitter Breakdown Voltage	BV_{CEO}	I_C = 1 mA	15	24	—	V
Collector-Substrate Breakdown Voltage	BV_{CIO}	I_{CI} = 100 μA	20	60	—	V
Emitter-Base Breakdown Voltage	BV_{EBO}	I_E = 500 μA	5.0	6.9	—	V
Collector Cutoff Current	I_{CEO}	V_{CE} = 10 V	—	—	10	μA
	I_{CBO}	V_{CB} = 10 V	—	—	1.0	μA
Base-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_C = 10 mA	650	740	850	mV
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 50 mA, I_B = 5 mA	—	400	700	mV
D-C Forward Current Transfer Ratio	h_{FE}	V_{CE} = 3 V, I_C = 10 mA	40	76	—	
		V_{CE} = 3 V, I_C = 50 mA	40	75	—	
Differential Input Offset Voltage*	V_{IO}	V_{CE} = 3 V, I_C = 1 mA	—	1.2	5.0	mV
Differential Input Offset Current*	I_{IO}	V_{CE} = 3 V, I_C = 1 mA	—	0.7	2.5	μA

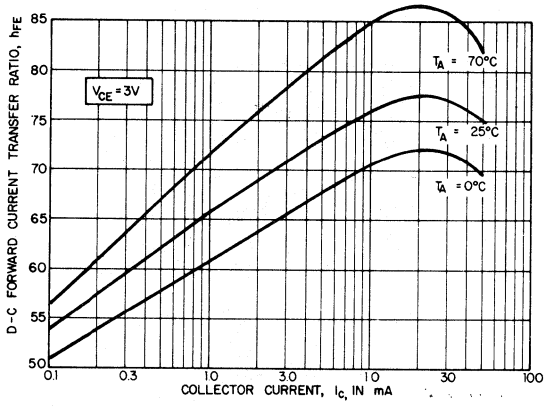
*Applies only to transistors Q_1 and Q_2 when connected as a differential pair.

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature

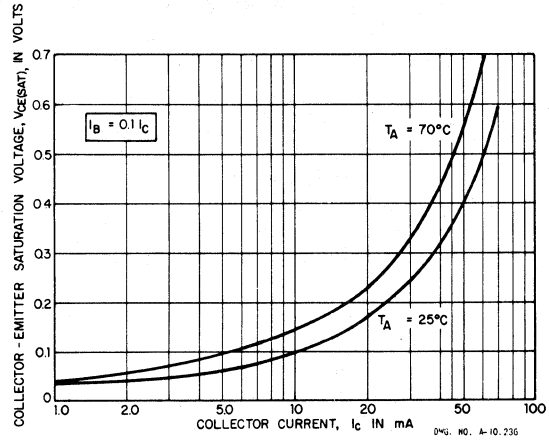
Power Dissipation, P_D (any one transistor) ..... 500 mW
(total package) ..... 750 mW*
Operating Temperature Range, T_A (ULN-2083A) ..... 0°C to +85°C
(ULS-2083H) ..... −55°C to +125°C
Storage Temperature Range, T_S ..... −55°C to +150°C

*Derate at the rate of 6.67 mW/°C above 25°C.

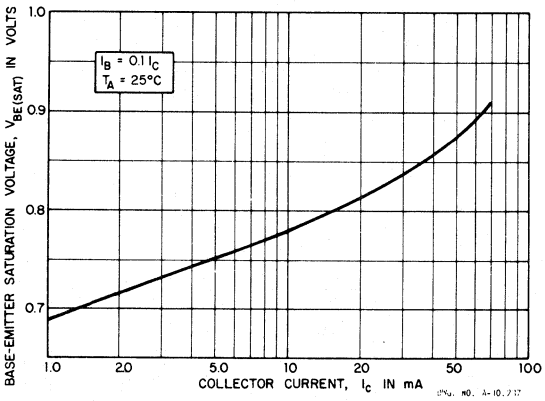
TYPICAL STATIC CHARACTERISTICS as a Function of Collector Current



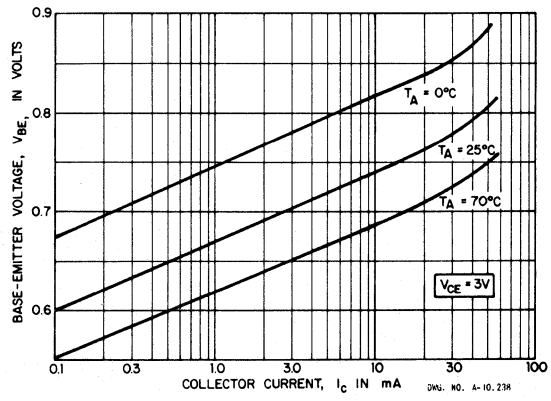
D-C FORWARD CURRENT TRANSFER RATIO



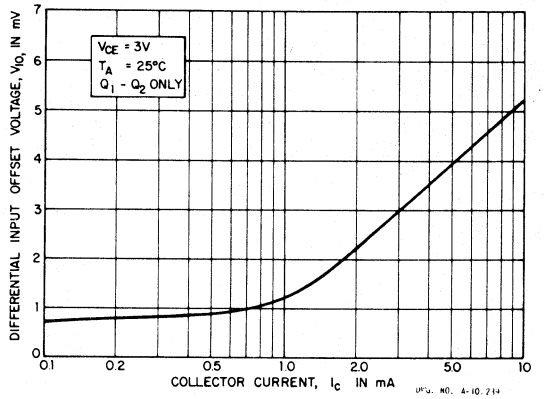
COLLECTOR-EMITTER SATURATION VOLTAGE



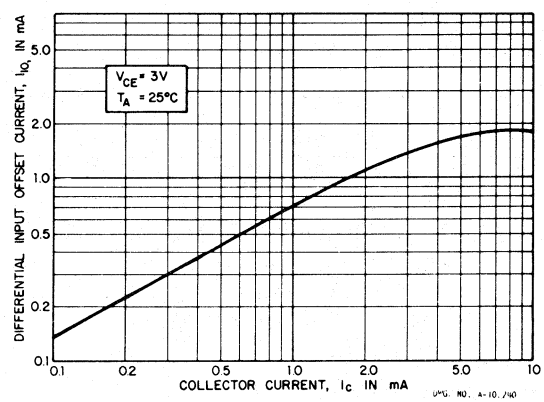
BASE-EMITTER SATURATION VOLTAGE



BASE-EMITTER VOLTAGE



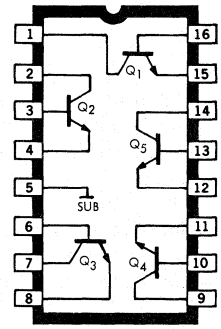
DIFFERENTIAL INPUT OFFSET VOLTAGE



DIFFERENTIAL INPUT OFFSET CURRENT

ULN-2083A-1
TRANSISTOR ARRAY

This device is a general-purpose transistor array for use in medium-current switching and differential amplifier applications. With the exception of the increased breakdown voltages shown below, the ULN-2083A-1 is identical to the ULN-2083A transistor array.



DWG. NO. A-10,232

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Collector-Base Breakdown Voltage	BV_{CBO}	I_C = 100 μA	40	60	—	V
Collector-Emitter Breakdown Voltage	BV_{CEO}	I_C = 1 mA	30	—	—	V

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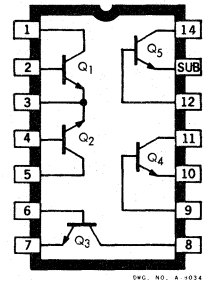
ULN-2086A
TRANSISTOR ARRAY

The ULN-2086A general-purpose transistor array consists of five silicon NPN transistors, two of which are connected as a differential amplifier. The monolithic construction provides close electrical and thermal matching between all transistors.

With the exception of the collector cutoff current specifications listed below and the omission of guaranteed limits on input offset voltage and input offset current, the ULN-2086A is identical to the ULN-2046A transistor array.



Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Collector Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	—	—	100	nA
	I_{CEO}	V_{CE} = 10 V, I_B = 0	—	—	5.0	μA

NOTE: The substrate terminal must be tied to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

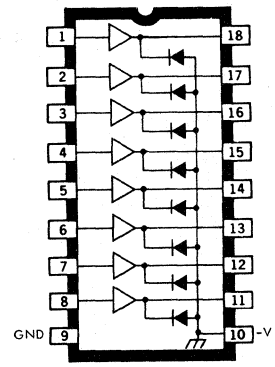
UDN-2580A 8-CHANNEL HIGH-CURRENT SOURCE DRIVER

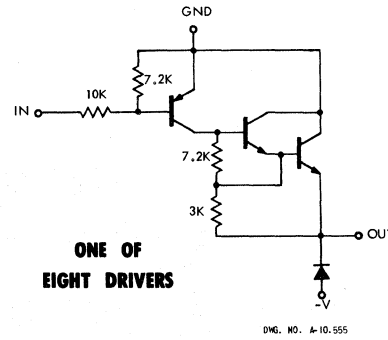
ORIGINATING from a need to provide an interface from NMOS to high-current inductive loads, the UDN-2580A 8-channel source driver is very versatile and has been used as an incandescent or LED driver and as a power predriver. The device functions like a PNP amplifier, but an NPN Darlington has been added to provide suitable current gain. By switching the input low (made more negative), the output is turned ON and the load current is sourced from the compound output.

Most NMOS logic includes depletion load and is capable of pulling the input of the UDN-2580A driver sufficiently high to turn OFF the device. For those few instances where open-drain NMOS is to be used, or the depletion load is excessively high, external pull-up resistors may be employed.

Although the UDN-2580A was chiefly intended for use with inductive loads, it will help solve many other design problems as well. When combined with the ULN-2068B quad 1.5 A driver, the UDN-2580A will effectively drive the segments of a common-cathode LED display. Alternatively, it may be employed as a digit driver with common-anode LEDs in combination with a ULN-2804A Darlington array. Typical applications are shown on the following pages.

The UDN-2580A 8-channel, high-current source driver is furnished in an 18-pin dual in-line plastic package with the outputs pinned opposite the inputs for ease in circuit layout. This device is also available in an industrial-grade hermetic package with reduced package power capability by changing the last letter of the part number from 'A' to 'R'.





Absolute Maximum Ratings at 25°C Free-Air Temperature for any Source Output (unless otherwise noted)

Circuit voltages are referenced to circuit ground (pin #9) unless otherwise noted:

Output Voltage, V_{CE}	−50 V
Input Voltage, V_{IN}	−30 V
Output Current, I_{OUT}	−500 mA
Ground Terminal Current, I_{GND}	3 A
Operating Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_S	−55°C to +150°C
Power Dissipation, P_D	
(Single Output)	1.0 W
(Total Package)	2.25 W
Derating Factor	18.18 mW/°C or 55°C/W

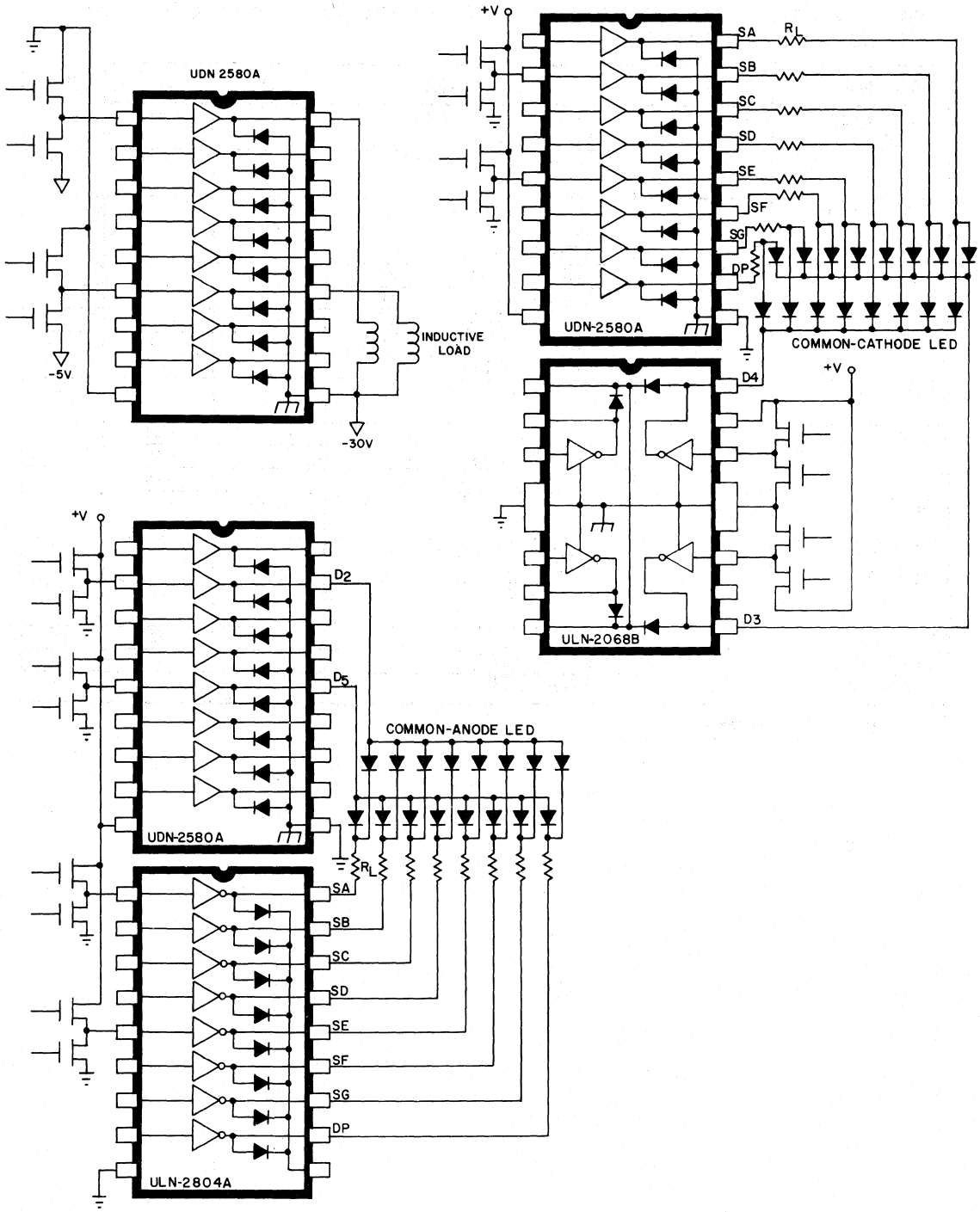
ELECTRICAL CHARACTERISTICS at 25°C (Unless Otherwise Noted)

Circuit voltages and currents are referenced to ground (pin #9) unless otherwise specified; V substrate is at −50V unless otherwise specified.

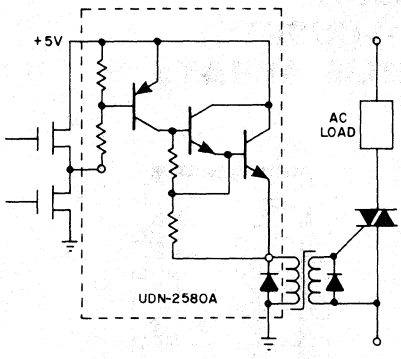
Characteristic	Symbol	Test Condition	Min.	Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = −50 V, T_A = 25°C V_{IN} = −0.5 V		50	μA
		V_{OUT} = −50 V, T_A = 70°C V_{IN} = −0.4 V		100	μA
Output Sustaining Voltage	$LV_{CE(SUS)}$	I_{OUT} = 25 mA (pulsed) V_{IN} = −0.4 V REFERENCE = −50 V	35*		V
Output Saturation Voltage	$V_{CE(ON)}$	I_{OUT} = −100 mA, V_{IN} = −2.4		1.7	V
		I_{OUT} = −225 mA, V_{IN} = −3.0		1.8	V
		I_{OUT} = −350 mA, V_{IN} = −3.6		1.9	V
Input Current	$I_{IN(ON)}$	V_{IN} = −3.6 V, I_{OUT} = −350 mA		500	μA
		V_{IN} = −15 V, I_{OUT} = −350 mA		2.1	mA
Input Current	$I_{IN(OFF)}$	I_C = 500 μA, V_{OUT} = −50 V T_A = 70°C	50		μA
Input Voltage	$V_{IN(ON)}$	I_C = 100 mA, $V_{OUT} \leq$ 1.7 V		−2.4	V
		I_C = 225 mA, $V_{OUT} \leq$ 1.8 V		−3.0	V
		I_C = 350 mA, V_{OUT} = 1.9 V		−3.6	V
Input Voltage	$V_{IN(OFF)}$	I_{OUT} = −500 μA, V_{OUT} = −50 V T_A = 70°C	−0.25		V
Clamp Diode Leakage Current	I_R	V_{SUB} = −50 V, V_{OUT} = −2.0 V T_A = +70°C		50	μA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA		2.0	V
Input Capacitance	C_{IN}			25	pF
Turn On Delay	T_{PHL}	0.5 E_{IN} to 0.5 E_{OUT}		5	μs
Turn Off Delay	T_{PLH}	0.5 E_{IN} to 0.5 E_{OUT}		5	μs

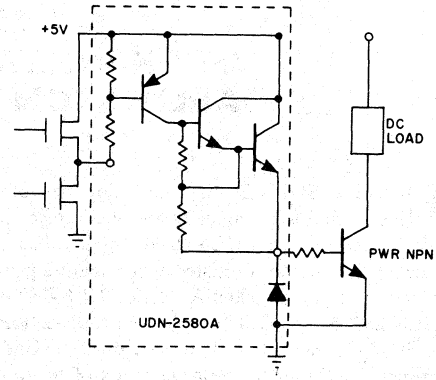
*Pulsed Test, $T_P \leq$ 300μs, Duty Cycle ≤ 2%.

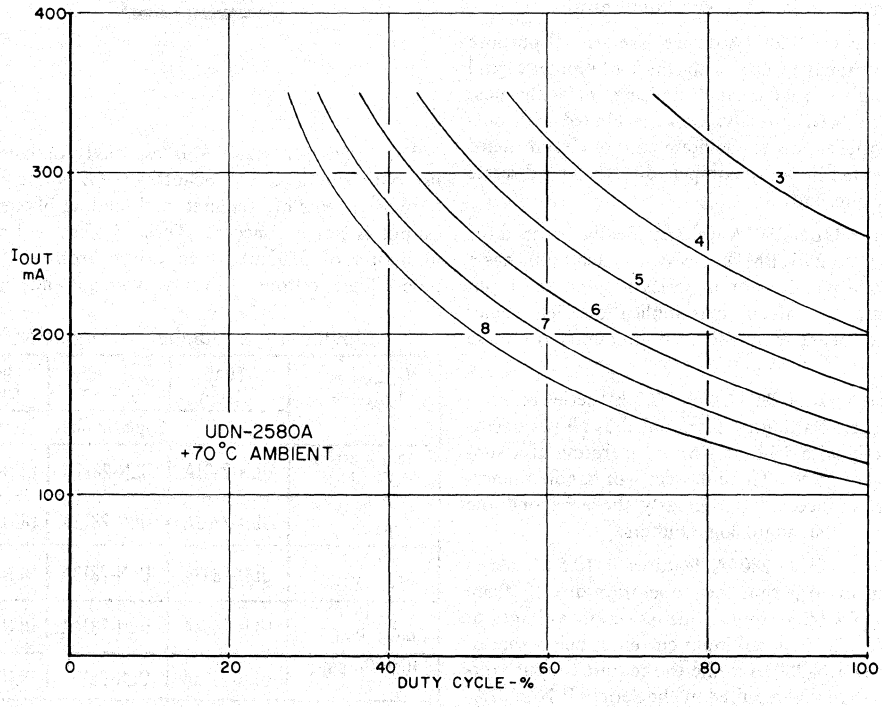
TYPICAL APPLICATIONS



TYPICAL APPLICATIONS (Cont.)







PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS AT +70°C

4

SERIES ULN-2800A
HIGH-VOLTAGE, HIGH-CURRENT
DARLINGTON TRANSISTOR ARRAYS

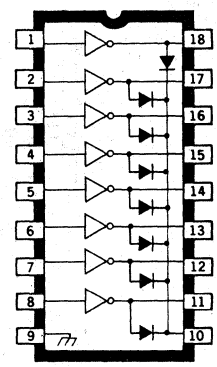
IDEALLY SUITED for interfacing between low-level digital logic circuitry and high-power peripheral loads, the Series ULN-2800A high-voltage, high-current Darlington transistor arrays feature peak load current ratings of 600 mA (Series ULN-2800A and ULN-2820A) or 750 mA (Series ULN-2810A) for each of the eight drivers in each device. Under the proper conditions, high-power loads of up to 4 A at 50V (200 W at 23% duty cycle) or 3.2 A at 95 V (304 W at 33% duty cycle) can be controlled. Typical loads include relays, solenoids, stepping motors, multiplexed LED and incandescent displays, and heaters. All devices feature open collector outputs and integral diodes for inductive load transient suppression.

The Series ULN-2801A devices are general purpose arrays which may be used with standard bipolar digital logic using external current limiting, or with most PMOS or CMOS directly. All are pinned with outputs opposite inputs to facilitate ease of circuit board layout and are priced to compete directly with discrete transistor alternatives.

The Series ULN-2802A was specifically designed for use with 14 to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also means excellent noise immunity for these devices.

The Series ULN-2803A has a 2.7 kΩ series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs – particularly those beyond the capabilities of standard logic buffers.

The Series ULN-2804A features a 10.5 kΩ series input resistor to permit their operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of the Series ULN-2803A while the required input voltage is less than that required by the Series ULN-2802A.



D-G. NO. A-10,322

The Series ULN-2805A is especially designed for use with standard and Schottky TTL where higher output currents are required and loading of the logic output is not a concern. These devices will sink a minimum of 350 mA when driven from a "totem pole" logic output. Typical voltage and current

Device Type Number Designation

$V_{CE(MAX)}$ = $I_{C(MAX)}$ =	50 V 500 mA	50 V 600 mA	95 V 500 mA
	Type Number		
General Purpose PMOS, CMOS	ULN-2801A	ULN-2811A	ULN-2821A
14 - 25 V PMOS	ULN-2802A	ULN-2812A	ULN-2822A
5 V TTL, CMOS	ULN-2803A	ULN-2813A	ULN-2823A
6 - 15 V CMOS, PMOS	ULN-2804A	ULN-2814A	ULN-2824A
High Output TTL	ULN-2805A	ULN-2815A	ULN-2825A

Series ULN-2800A and ULN-2810A devices are also available (with reduced package power capability) in industrial-grade hermetic packages. To order, change the last letter of the part number from 'A' to 'R'. Note that the high-voltage devices ($BV_{CE} \geq 95$ V) are not presently available with this packaging option.

levels for both the Series ULN-2803A and ULN-2805A are show in the graphs on page 4-57.

The Series ULN-2800A is the standard high-voltage, high-current Darlington array. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Outputs may be paralleled for higher load current capability. The Series ULN-2810A devices are similar except that they will sink 600 mA. The Series ULN-2820A will sustain 95 V in the OFF state. A table showing the specific type numbers available for the various applications is given on page 4-50.

All Series ULN-2800A Darlington arrays are furnished in an 18-pin dual in-line plastic package. Similar devices can also be supplied in a hermetic dual in-line package for use in military and aerospace applications (with a slightly reduced power handling capability).

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature for any one Darlington pair (unless otherwise noted)

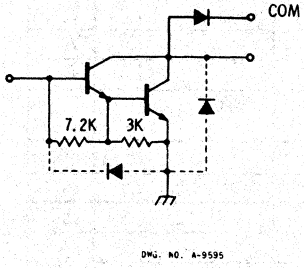
Output Voltage, V_{CE} (Series ULN-2800, 2810A)	50 V
(Series ULN-2820A)	95 V
Input Voltage, V_{IN} (Series ULN-2802, 2803, 2804A)	30 V
(Series ULN-2805A)	15 V
Continuous Collector Current, I_C (Series ULN-2800, 2820A)	500 mA
(Series ULN-2810A)	600 mA
Continuous Base Current, I_B	25 mA
Power Dissipation, P_D (one Darlington pair)	1.0 W
(total package)	2.25 W*
Operating Ambient Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_S	−55°C to +150°C

*Derate at the rate of 18.18 mW/°C above 25°C.

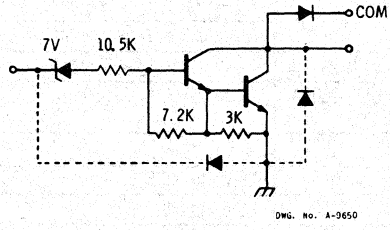
Under normal operating conditions, these devices will sustain 350 mA per output with $V_{CE(SAT)} = 1.6$ V at 70°C with a pulse width of 20 ms and a duty cycle of 40%. Other allowable combinations of output current, number of outputs conducting, and duty cycle are shown on page 4-56.

4

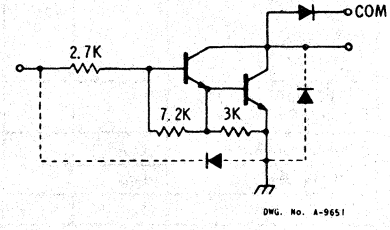
PARTIAL SCHEMATICS



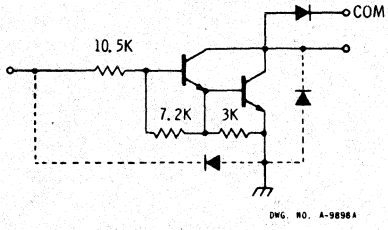
Series ULN-2801A
(each driver)



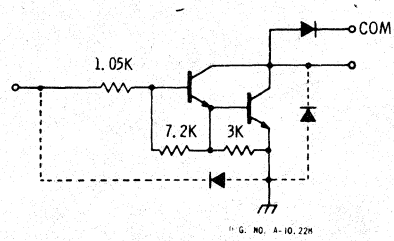
Series ULN-2802A
(each driver)



Series ULN-2803A
(each driver)



Series ULN-2804A
(each driver)



Series ULN-2805A
(each driver)

SERIES ULN-2800A

ELECTRICAL CHARACTERISTICS AT 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 50 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2802A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2804A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 μA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2802A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2803A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2804A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2805A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2802A	V_{CE} = 2.0 V, I_C = 300 mA	—	—	13	V
			ULN-2803A	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN-2804A	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
			ULN-2805A	V_{CE} = 2.0 V, I_C = 350 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2801A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
Input Capacitance	C_{IN}	–	All		—	15	25	pF
Turn-On Delay	t_{PLH}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	μA
				V_R = 50 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

SERIES ULN-2810A

ELECTRICAL CHARACTERISTICS AT 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 50 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 50 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2812A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2814A	V_{CE} = 50 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
				I_C = 500 mA, I_B = 600 μA	—	1.7	1.9	V
Input Current	$I_{IN(ON)}$	3	ULN-2812A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2813A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2814A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2815A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2812A	V_{CE} = 2.0 V, I_C = 500 mA	—	—	17	V
			ULN-2813A	V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	—	—	3.5	V
			ULN-2814A	V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
				V_{CE} = 2.0 V, I_C = 500 mA	—	—	9.5	V
			ULN-2815A	V_{CE} = 2.0 V, I_C = 500 mA	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2811A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
				V_{CE} = 2.0 V, I_C = 500 mA	900	—	—	
Input Capacitance	C_{IN}	–	All		—	15	25	pF
Turn-On Delay	t_{PLH}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 50 V, T_A = 25°C	—	—	50	μA
				V_R = 50 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V
				I_F = 500 mA	—	2.1	2.5	V

4

SERIES ULN-2820A

ELECTRICAL CHARACTERISTICS AT 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	1A	All	V_{CE} = 95 V, T_A = 25°C	—	—	50	μA
				V_{CE} = 95 V, T_A = 70°C	—	—	100	μA
		1B	ULN-2822A	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 6.0 V	—	—	500	μA
			ULN-2824A	V_{CE} = 95 V, T_A = 70°C, V_{IN} = 1.0 V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	I_C = 100 mA, I_B = 250 μA	—	0.9	1.1	V
				I_C = 200 mA, I_B = 350 μA	—	1.1	1.3	V
				I_C = 350 mA, I_B = 500 μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2822A	V_{IN} = 17 V	—	0.82	1.25	mA
			ULN-2823A	V_{IN} = 3.85 V	—	0.93	1.35	mA
			ULN-2824A	V_{IN} = 5.0 V	—	0.35	0.5	mA
				V_{IN} = 12 V	—	1.0	1.45	mA
			ULN-2825A	V_{IN} = 3.0 V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	I_C = 500 μA, T_A = 70°C	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2822A	V_{CE} = 2.0 V, I_C = 300 mA	—	—	13	V
			ULN-2823A	V_{CE} = 2.0 V, I_C = 200 mA	—	—	2.4	V
				V_{CE} = 2.0 V, I_C = 250 mA	—	—	2.7	V
				V_{CE} = 2.0 V, I_C = 300 mA	—	—	3.0	V
			ULN-2824A	V_{CE} = 2.0 V, I_C = 125 mA	—	—	5.0	V
				V_{CE} = 2.0 V, I_C = 200 mA	—	—	6.0	V
				V_{CE} = 2.0 V, I_C = 275 mA	—	—	7.0	V
				V_{CE} = 2.0 V, I_C = 350 mA	—	—	8.0	V
			ULN-2825A	V_{CE} = 2.0 V, I_C = 350 mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2821A	V_{CE} = 2.0 V, I_C = 350 mA	1000	—	—	
Input Capacitance	C_{IN}	–	All		—	15	25	pF
Turn-On Delay	t_{PLH}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	V_R = 95 V, T_A = 25°C	—	—	50	μA
				V_R = 95 V, T_A = 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	I_F = 350 mA	—	1.7	2.0	V

TEST FIGURES

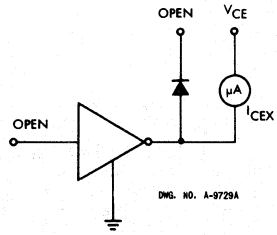


FIGURE 1A

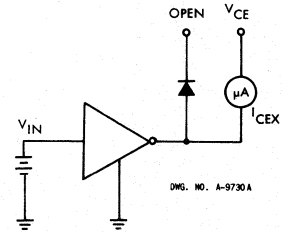


FIGURE 1B

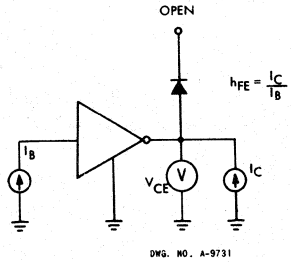


FIGURE 2

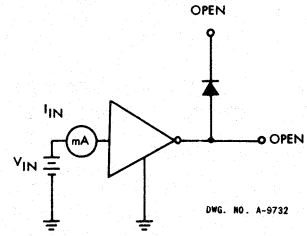


FIGURE 3

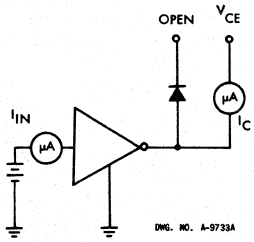


FIGURE 4

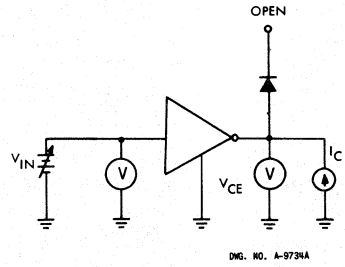


FIGURE 5

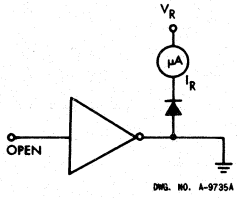


FIGURE 6

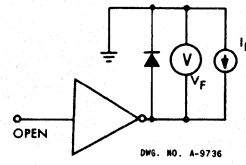
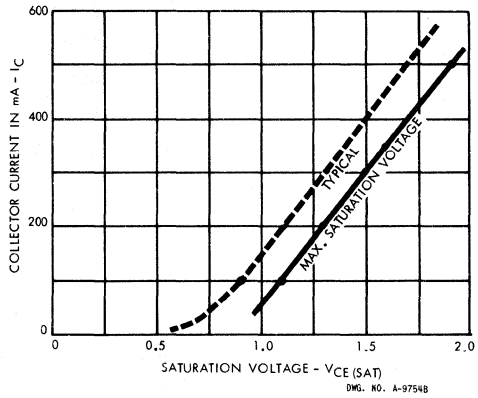
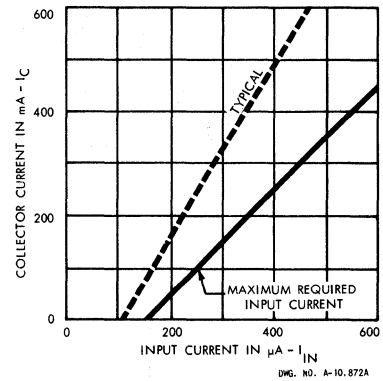


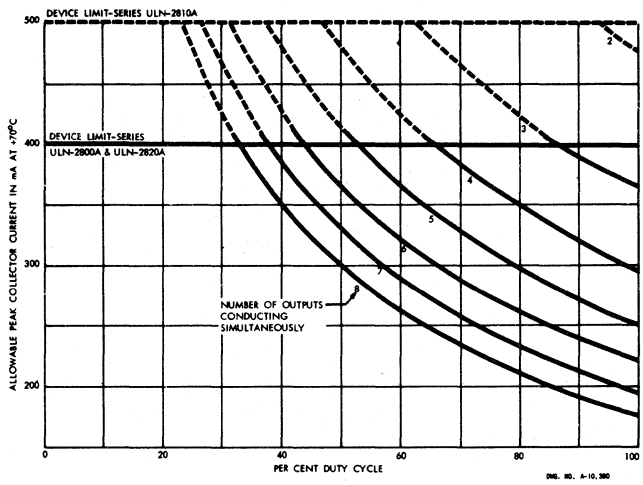
FIGURE 7



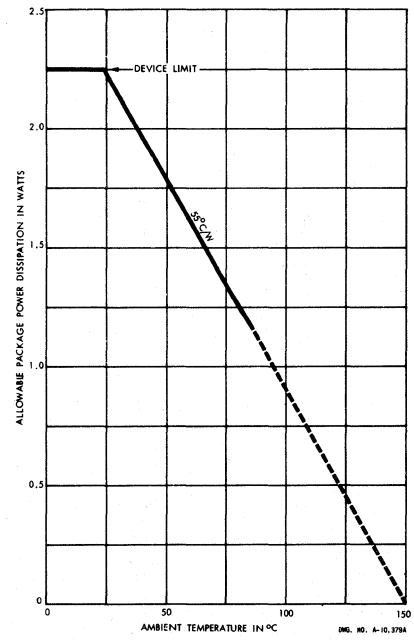
COLLECTOR CURRENT
AS A FUNCTION OF SATURATION VOLTAGE



COLLECTOR CURRENT
AS A FUNCTION OF INPUT CURRENT

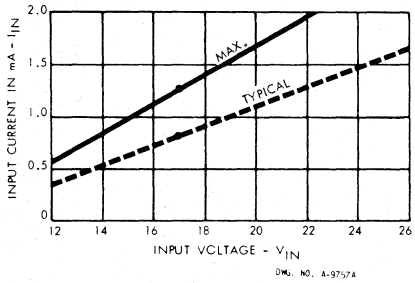


PEAK COLLECTOR CURRENT
AS A FUNCTION OF
DUTY CYCLE AND NUMBER OF OUTPUTS

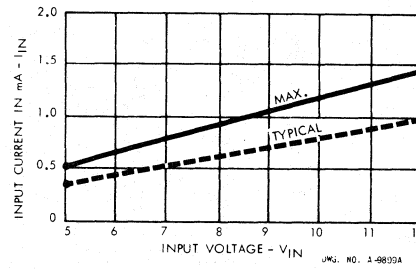


ALLOWABLE AVERAGE POWER DISSIPATION
AS A FUNCTION OF AMBIENT TEMPERATURE

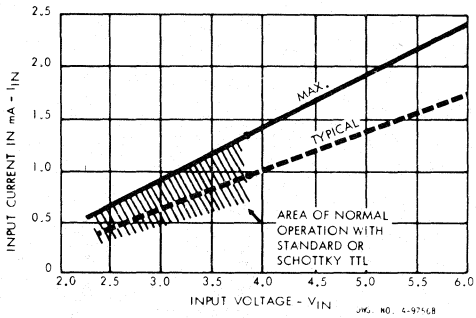
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



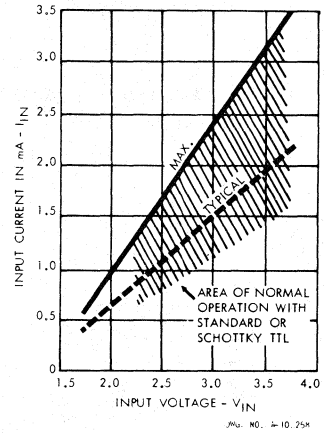
SERIES ULN-2802A



SERIES ULN-2804A

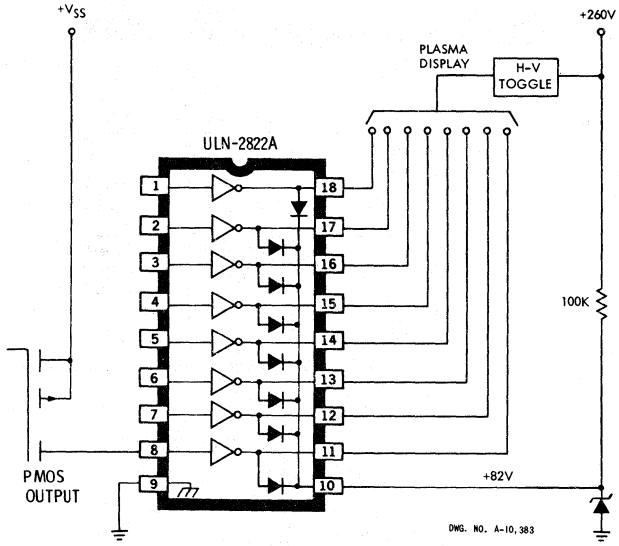


SERIES ULN-2803A

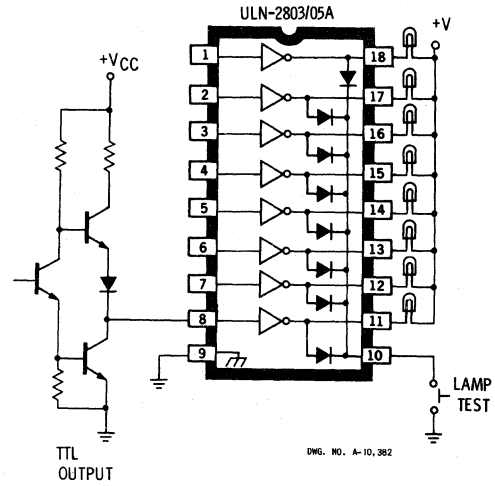


SERIES ULN-2805A

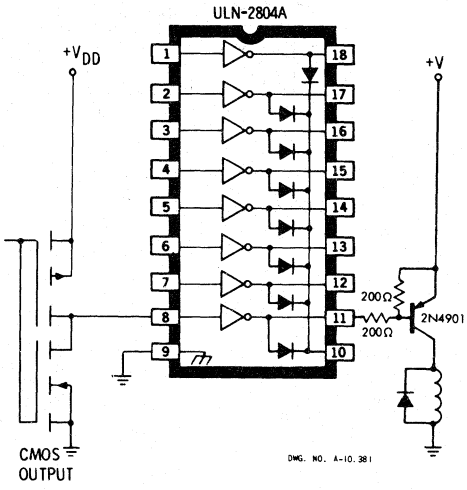
4



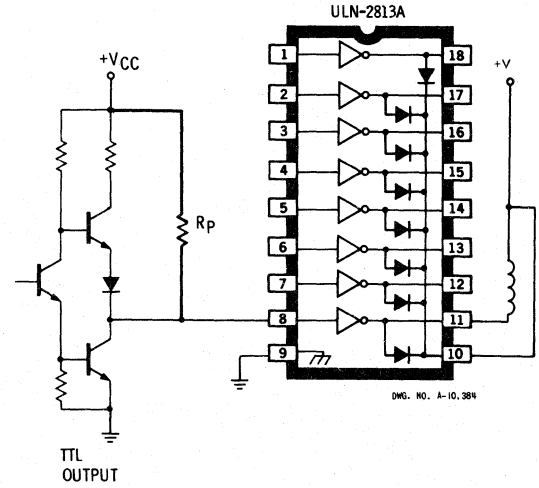
OFF VOLTAGE BIAS FOR HIGH-VOLTAGE LOADS



TTL TO LOAD

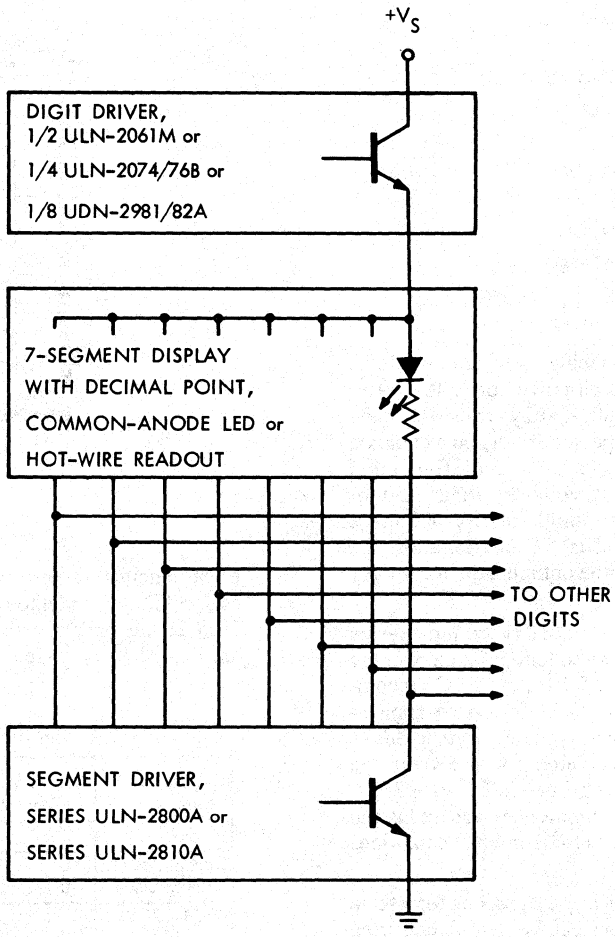


BUFFER FOR HIGHER CURRENT LOADS



USE OF PULL-UP RESISTORS TO INCREASE DRIVE CURRENT

TYPICAL DISPLAY INTERFACE

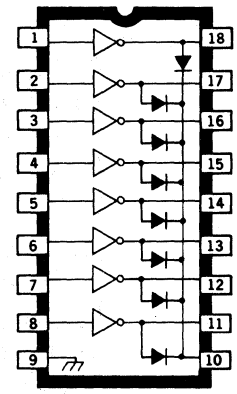


DWG. NO. A-10,378

SERIES ULS-2800H and ULS-2800R HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Peak Output Current to 600 mA
- Transient Protected Outputs
- Side-Brazed Hermetic Package, or
- Cer-DIP Package
- High-Reliability Screening Available
- Wide Operating Temperature Ranges



DWG. NO. A-10,322

DESIGNED for interfacing between low-level logic circuitry and high-power loads, the Series ULS-2800H and ULS-2800R arrays consist of eight silicon NPN Darlington power drivers on a common monolithic substrate. The choice of five input characteristics, 2 output voltage ratings (50 or 95 V), 2 output current ratings (500 or 600 mA), and 2 package styles (suffix 'H' or 'R') allow the circuit designer to select the optimum device for any specific application.

The side-brazed, hermetically-sealed Series ULS-2800H devices are rated for operation over the temperature range of −55°C to +125°C, recommending them for military and aerospace applications. The cer-DIP, industrial grade hermetic Series ULS-2800R devices are rated for use over the operating temperature range of −40°C to +85°C, permitting their use in commercial and industrial applications where severe environmental conditions may be encountered.

The appropriate specific part number for use in standard logic applications can be determined from the Device Type Number Designation chart. Note that the high-voltage devices ($BV_{CE} \geqq 95$ V) are available in the Series ULS-2800H only. All units feature open collector outputs and integral diodes for inductive load transient suppression.

All Series ULS-2800H Darlington power drivers are furnished in an 18-pin side-brazed dual in-line hermetic package which meets the processing and environmental requirements of Military Standard MIL-STD-883, Methods 5004 and 5005. Series ULS-2800H arrays with high-reliability screening are described on page 4-70.

Device Type Number Designation

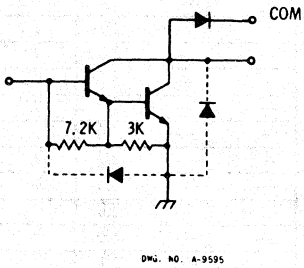
$V_{CE(MAX)}$ = $I_{C(MAX)}$ =	50 V 500 mA	50 V 600 mA	95 V 500 mA
		Type Number	
General Purpose PMOS, CMOS	ULS-2801*	ULS-2811*	ULS-2821H
14 - 25 V PMOS	ULS-2802*	ULS-2812*	ULS-2822H
5 V TTL, CMOS	ULS-2803*	ULS-2813*	ULS-2823H
6 - 15 V CMOS, PMOS	ULS-2804*	ULS-2814*	ULS-2824H
High Output TTL	ULS-2805*	ULS-2815*	ULS-2825H

*Complete part number includes a final letter to indicate package. H = hermetic dual in-line, R = ceramic dual in-line.

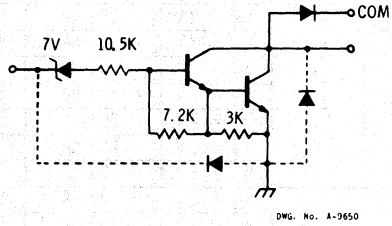
ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE} (Series ULS-2800, 10*) ..... 50 V
(Series ULS-2820H) ..... 95 V
Input Voltage, V_{IN} (Series ULS-2802, 03, 04*) ..... 30 V
(Series ULS-2805*) ..... 15 V
Peak Output Current, I_{OUT} (Series ULS-2800*, 20H) ..... 500 mA
(Series ULS-2810*) ..... 600 mA
Ground Terminal Current, I_{GND} ..... 3.0 A
Continuous Input Current, I_{IN} ..... 25 mA
Power Dissipation, P_D (one Darlington pair) ..... 1.0 W
(total package) ..... See Graph, p 4-67
Operating Temperature Range, T_A ('H' package) ..... −55°C to +125°C
('R' package) ..... −40°C to +85°C
Storage Temperature Range, T_S ..... −65°C to +150°C

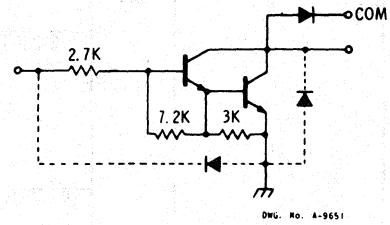
PARTIAL SCHEMATICS



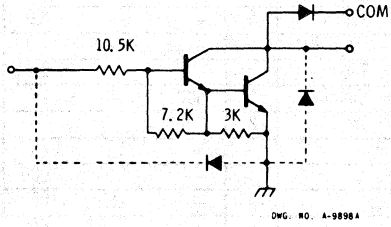
Series ULS-2801*
(each driver)



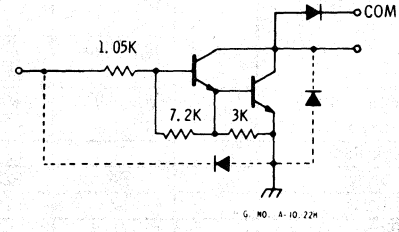
Series ULS-2802*
(each driver)



Series ULS-2803*
(each driver)



Series ULS-2804*
(each driver)



Series ULS-2805*
(each driver)

*Complete part number includes a final letter to indicate package. H = hermetic dual in-line, R = ceramic dual in-line.

SERIES ULS-2800H and ULS-2800R

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions: Temp	Test Conditions	Fig.	Limits: Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	μA
		ULS-2802*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	μA
		ULS-2804*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	Min.	I_C = 350 mA, I_B = 850 μA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 μA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 μA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 μA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 μA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 μA	2	—	0.9	1.1	V
			Max.	I_C = 350 mA, I_B = 500 μA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 μA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 μA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS-2802*		V_{IN} = 17 V	3	575	850	1300	μA
		ULS-2803*		V_{IN} = 3.85 V	3	675	930	1350	μA
		ULS-2804*		V_{IN} = 5 V	3	250	350	500	μA
				V_{IN} = 12 V	3	750	1000	1450	μA
		ULS-2805*		V_{IN} = 3 V	3	1150	1500	2400	μA
	$I_{IN(OFF)}$	All	Max.	I_C = 500 μA	4	25	50	—	μA
Input Voltage	$V_{IN(ON)}$	ULS-2802*	Min.	V_{CE} = 2 V, I_C = 300 mA	5	—	—	18	V
			Max.	V_{CE} = 2 V, I_C = 300 mA	5	—	—	13	V
		ULS-2803*	Min.	V_{CE} = 2 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2 V, I_C = 300 mA	5	—	—	3.9	V
			Max.	V_{CE} = 2 V, I_C = 200 mA	5	—	—	2.4	V
				V_{CE} = 2 V, I_C = 250 mA	5	—	—	2.7	V
				V_{CE} = 2 V, I_C = 300 mA	5	—	—	3.0	V
		ULS-2804*	Min.	V_{CE} = 2 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2 V, I_C = 350 mA	5	—	—	12	V
			Max.	V_{CE} = 2 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2 V, I_C = 200 mA	5	—	—	6.0	V
				V_{CE} = 2 V, I_C = 275 mA	5	—	—	7.0	V
				V_{CE} = 2 V, I_C = 350 mA	5	—	—	8.0	V
		ULS-2805*	Min.	V_{CE} = 2 V, I_c = 350 mA	5	—	—	3.0	V
			Max.	V_{CE} = 2 V, I_c = 350 mA	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS-2801*	Min.	V_{CE} = 2 V, I_c = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2 V, I_c = 350 mA	2	1000	—	—	—
Input Capacitance	C_{IN}	All	+25°C		—	—	15	25	pF
Turn-On Delay	t_{PLH}	All	+25°C	0.5 E_{in} to 0.5 E_{out}	—	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C	0.5 E_{in} to 0.5 E_{out}	—	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA	7	—	1.7	2.0	V

*Complete part number includes a final letter to indicate package. H = hermetic dual in-line, R = ceramic dual in-line.
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

SERIES ULS-2810H and ULS-2810R

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions: Temp	Test Conditions	Fig.	Limits: Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		V_{CE} = 50 V	1A	—	—	100	μA
		ULS-2812*		V_{CE} = 50 V, V_{IN} = 6 V	1B	—	—	500	μA
		ULS-2814*		V_{CE} = 50 V, V_{IN} = 1 V	1B	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	Min.	I_C = 500 mA, I_B = 1100 μA	2	—	1.8	2.1	V
				I_C = 350 mA, I_B = 850 μA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 μA	2	—	1.3	1.5	V
			+25°C	I_C = 500 mA, I_B = 600 μA	2	—	1.7	1.9	V
				I_C = 350 mA, I_B = 500 μA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 μA	2	—	1.1	1.3	V
			Max.	I_C = 500 mA, I_B = 600 μA	2	—	1.8	2.1	V
				I_C = 350 mA, I_B = 500 μA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 μA	2	—	1.3	1.5	V
Input Current	$I_{IN(ON)}$	ULS-2812*		V_{IN} = 17 V	3	575	850	1300	μA
		ULS-2813*		V_{IN} = 3.85 V	3	675	930	1350	μA
		ULS-2814*		V_{IN} = 5 V	3	250	350	500	μA
				V_{IN} = 12 V	3	750	1000	1450	μA
		ULS-2815*		V_{IN} = 3 V	3	1150	1500	2400	μA
	$I_{IN(OFF)}$	All	Max.	I_C = 500 μA	4	25	50	—	μA
Input Voltage	$V_{IN(ON)}$	ULS-2812*	Min.	V_{CE} = 2 V, I_C = 500 mA	5	—	—	23.5	V
			Max.	V_{CE} = 2 V, I_C = 500 mA	5	—	—	17	V
		ULS-2813*	Min.	V_{CE} = 2 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2 V, I_C = 300 mA	5	—	—	3.9	V
				V_{CE} = 2 V, I_C = 500 mA	5	—	—	6.0	V
			Max.	V_{CE} = 2 V, I_C = 250 mA	5	—	—	2.7	V
				V_{CE} = 2 V, I_C = 300 mA	5	—	—	3.0	V
				V_{CE} = 2 V, I_C = 500 mA	5	—	—	3.5	V
		ULS-2814*	Min.	V_{CE} = 2 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2 V, I_C = 350 mA	5	—	—	12	V
				V_{CE} = 2 V, I_C = 500 mA	5	—	—	17	V
			Max.	V_{CE} = 2 V, I_C = 275 mA	5	—	—	7.0	V
				V_{CE} = 2 V, I_C = 350 mA	5	—	—	8.0	V
				V_{CE} = 2 V, I_C = 500 mA	5	—	—	9.5	V
		ULS-2815*	Min.	V_{CE} = 2 V, I_C = 350 mA	5	—	—	3.0	V
				V_{CE} = 2 V, I_C = 500 mA	5	—	—	3.5	V
			Max.	V_{CE} = 2 V, I_C = 350 mA	5	—	—	2.4	V
				V_{CE} = 2 V, I_C = 500 mA	5	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS-2811*	Min.	V_{CE} = 2 V, I_C = 500 mA	2	450	—	—	—
			+25°C	V_{CE} = 2 V, I_C = 500 mA	2	900	—	—	—
Input Capacitance	C_{IN}	All	+25°C		—	—	15	25	pF
Turn-On Delay	t_{PLH}	All	+25°C	0.5 E_{in} to 0.5 E_{out}	—	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C	0.5 E_{in} to 0.5 E_{out}	—	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 50 V	6	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA	7	—	1.7	2.0	V
				I_F = 500 mA	7	—	—	2.5	V

*Complete part number includes a final letter to indicate package. H = hermetic dual in-line, R = ceramic dual in-line.
Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

SERIES ULS-2820H

ELECTRICAL CHARACTERISTICS: (over operating temperature range unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions		Fig.	Limits			Units
			Temp			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	All		V_{CE} = 95 V	1A	—	—	100	μA
		ULS-2822H		V_{CE} = 95 V, V_{IN} = 6 V	1B	—	—	500	μA
		ULS-2824H		V_{CE} = 95 V, V_{IN} = 1 V	1B	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	Min.	I_C = 350 mA, I_B = 850 μA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 550 μA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 350 μA	2	—	1.1	1.3	V
			+25°C	I_C = 350 mA, I_B = 500 μA	2	—	1.25	1.6	V
				I_C = 200 mA, I_B = 350 μA	2	—	1.1	1.3	V
				I_C = 100 mA, I_B = 250 μA	2	—	0.9	1.1	V
			Max.	I_C = 350 mA, I_B = 500 μA	2	—	1.6	1.8	V
				I_C = 200 mA, I_B = 350 μA	2	—	1.3	1.5	V
				I_C = 100 mA, I_B = 250 μA	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS-2822H		V_{IN} = 17 V	3	575	850	1300	μA
		ULS-2823H		V_{IN} = 3.85 V	3	675	930	1350	μA
		ULS-2824H		V_{IN} = 5 V	3	250	350	500	μA
				V_{IN} = 12 V	3	750	1000	1450	μA
		ULS-2825H		V_{IN} = 3 V	3	1150	1500	2400	μA
	$I_{IN(OFF)}$	All	Max.	I_C = 500 μA	4	25	50	—	μA
Input Voltage	$V_{IN(ON)}$	ULS-2822H	Min.	V_{CE} = 2 V, I_C = 300 mA	5	—	—	18	V
			Max.	V_{CE} = 2 V, I_C = 300 mA	5	—	—	13	V
		ULS-2823H	Min.	V_{CE} = 2 V, I_C = 200 mA	5	—	—	3.3	V
				V_{CE} = 2 V, I_C = 250 mA	5	—	—	3.6	V
				V_{CE} = 2 V, I_C = 300 mA	5	—	—	3.9	V
			Max.	V_{CE} = 2 V, I_C = 200 mA	5	—	—	2.4	V
				V_{CE} = 2 V, I_C = 250 mA	5	—	—	2.7	V
				V_{CE} = 2 V, I_C = 300 mA	5	—	—	3.0	V
		ULS-2824H	Min.	V_{CE} = 2 V, I_C = 125 mA	5	—	—	6.0	V
				V_{CE} = 2 V, I_C = 200 mA	5	—	—	8.0	V
				V_{CE} = 2 V, I_C = 275 mA	5	—	—	10	V
				V_{CE} = 2 V, I_C = 350 mA	5	—	—	12	V
			Max.	V_{CE} = 2 V, I_C = 125 mA	5	—	—	5.0	V
				V_{CE} = 2 V, I_C = 200 mA	5	—	—	6.0	V
				V_{CE} = 2 V, I_C = 275 mA	5	—	—	7.0	V
				V_{CE} = 2 V, I_C = 350 mA	5	—	—	8.0	V
		ULS-2825H	Min.	V_{CE} = 2 V, I_C = 350 mA	5	—	—	3.0	V
			Max.	V_{CE} = 2 V, I_C = 350 mA	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS-2821H	Min.	V_{CE} = 2 V, I_C = 350 mA	2	500	—	—	—
			+25°C	V_{CE} = 2 V, I_C = 350 mA	2	1000	—	—	—
Input Capacitance	C_{IN}	All	+25°C		—	—	15	25	pF
Turn-On Delay	t_{PLH}	All	+25°C	0.5 E_{in} to 0.5 E_{out}	—	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C	0.5 E_{in} to 0.5 E_{out}	—	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		V_R = 95 V	6	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All		I_F = 350 mA	7	—	1.7	2.0	V

Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

TEST FIGURES

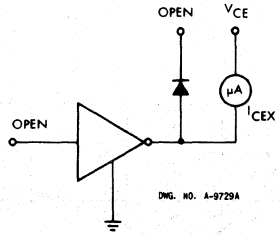


FIGURE 1A

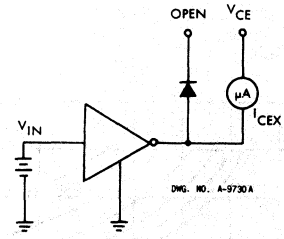


FIGURE 1B

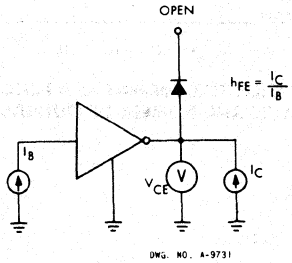


FIGURE 2

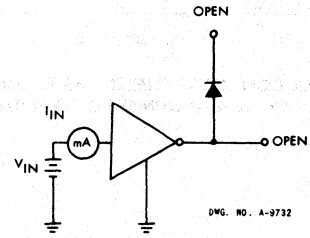


FIGURE 3

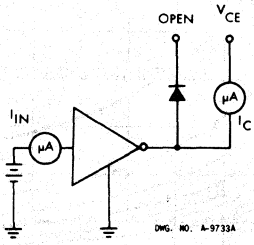


FIGURE 4

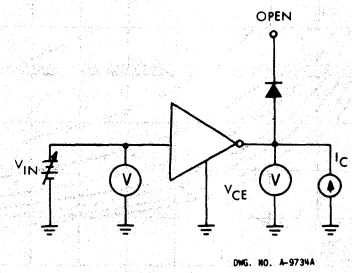


FIGURE 5

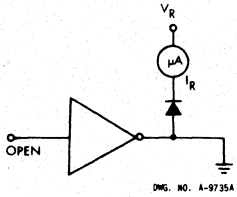


FIGURE 6

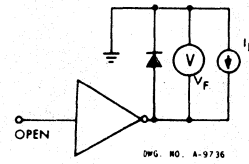
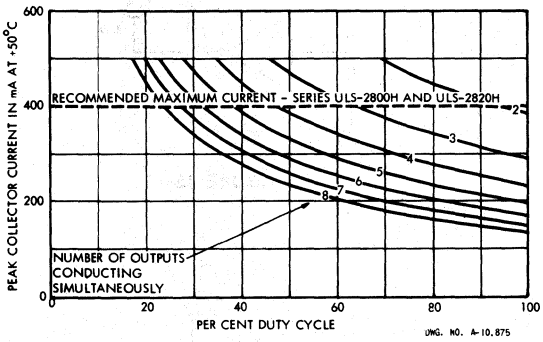
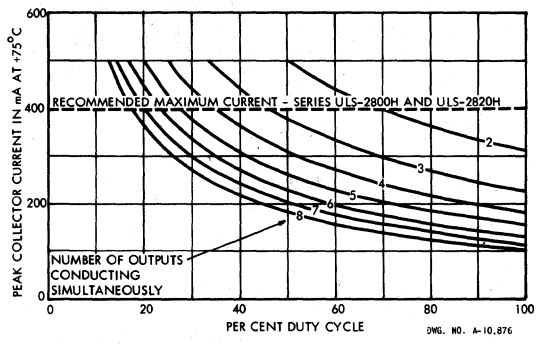


FIGURE 7

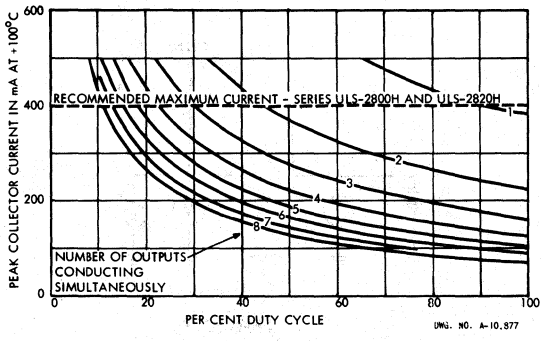
SERIES ULS-2800H



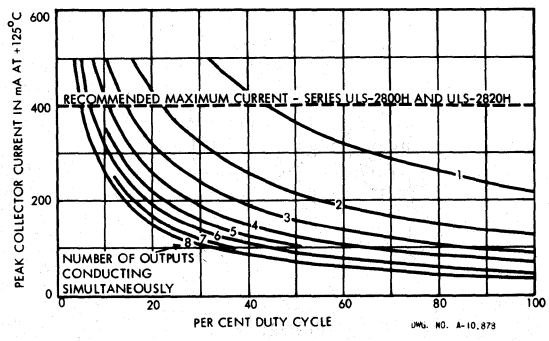
PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS AT +50°C



PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS AT +75°C

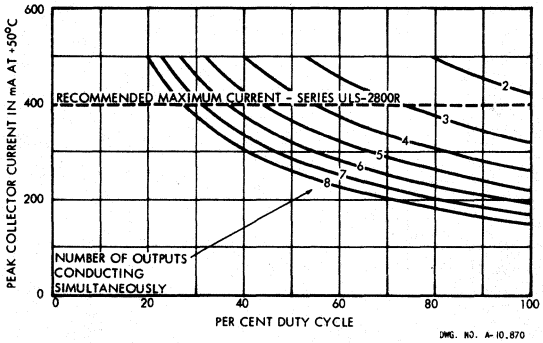


PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS AT +100°C

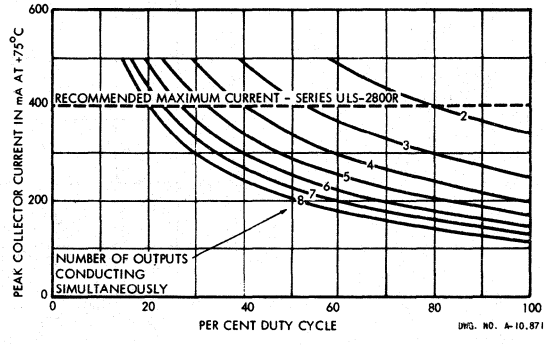


PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS AT +125°C

SERIES ULS-2800R

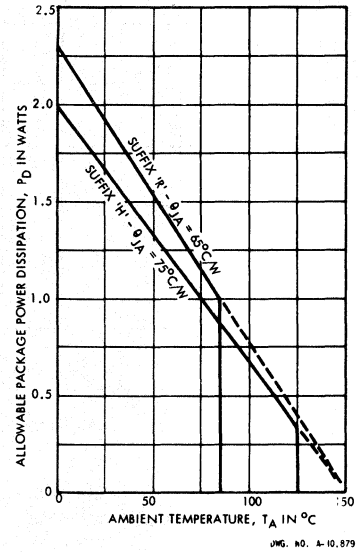


PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS AT +50°C



PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS AT +75°C

ALLOWABLE PACKAGE POWER DISSIPATION SERIES ULS-2800H and ULS-2800R



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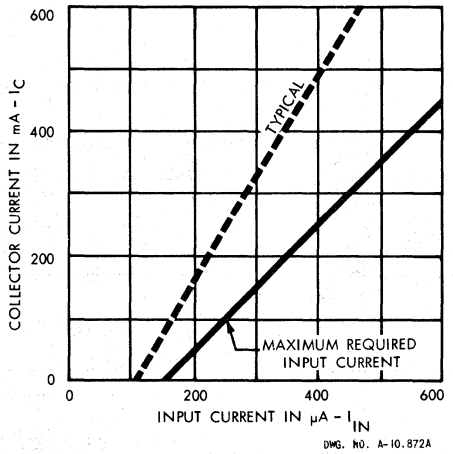
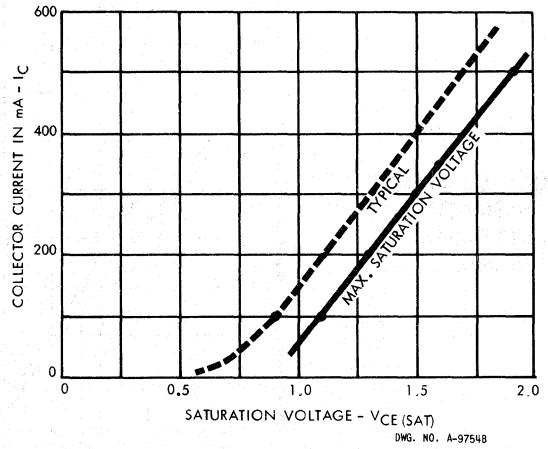


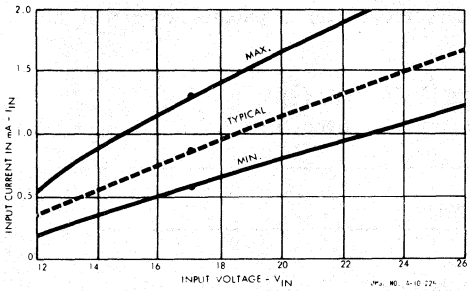
COLLECTOR CURRENT
AS A FUNCTION OF INPUT CURRENT



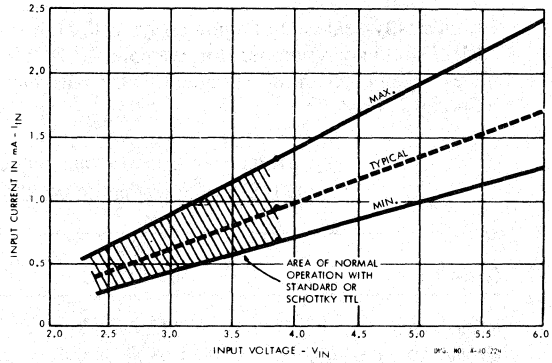
COLLECTOR CURRENT
AS A FUNCTION OF SATURATION VOLTAGE

*Complete part number includes a final letter to indicate package. H = hermetic dual in-line, R = ceramic dual in-line.

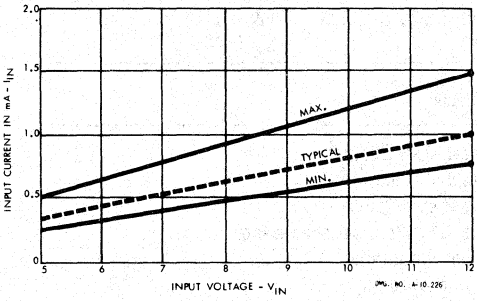
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



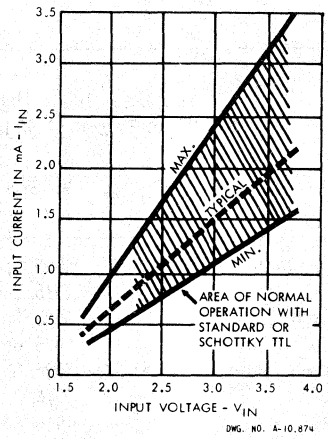
SERIES ULS-2802



SERIES ULS-2803



SERIES ULS-2804



SERIES ULS-2805

4

HERMETICALLY-SEALED DARLINGTON TRANSISTOR ARRAYS WITH MIL-STD-883 HIGH-RELIABILITY SCREENING

Hermetically-sealed Darlington arrays with high-reliability screening can be ordered by adding the suffix "MIL" to the part number, for example, ULS-2801H-MIL. If marking with the customers part number is necessary in place of the Sprague Electric part number, this must be stated on the purchase order with the marking desired.

Table I — 100% Production Screen Tests (All Hermetic Parts)
MIL-STD-883, Method 5004, Class B, Paragraphs 3.1.1 thru 3.1.6

Screen	MIL-STD-883 Test Method	Conditions
Internal Visual	2010, Cond. B	—
Stabilization Bake	1008, Cond. C	150°C, 24 Hours
Thermal Shock	1011, Cond. A	0 to 100°C, 15 Cycles
Constant Acceleration	2001, Cond. E	30,000 G's, Y1 Plane
Fine Seal	1014, Cond. A	5×10^{-7} Maximum
Gross Seal	1014, Cond. C	—
Electrical	—	Per specification
Marking	—	Sprague or customer part number, date code, lot identification, index point

Table II — 100% High-Reliability Screening ("MIL" Suffix Parts Only)
MIL-STD-883, Method 5004, Class B, Paragraphs 3.1.8, 3.1.9, 3.1.12 & 3.1.14

Screen	MIL-STD-883 Test Method	Conditions
Interim Electrical	5005, Gp A, Subgp 1	25°C per specification
Burn-In	1015, Cond. A	125°C, 160 Hours
Static Electrical	5005, Gp A, Subgp 1	25°C per specification
	5005, Gp A, Subgp 2 & 3	−55°C & +125°C per specification
Dynamic & Functional Electrical	5005, Gp A, Subgp 4, 7 & 9	25°C per specification
Fine Seal	1014, Cond. A	5×10^{-7} Maximum
Gross Seal	1014, Cond. C	—
External Visual	2009	—

Table III — High-Reliability Qualification and Quality Conformance Inspection
MIL-STD-883, Method 5004, Class B, Paragraph 3.1.17

Test	MIL-STD-883 Test Method	Description
Group A Subgp. 1-4, 7 & 9	5005, Table I	Each production lot
Group B	5005, Table II	Each production lot
Group C	5005, Table III	End points, Gp. A, Subgp. 1, every 90 days
Group D	5005, Table IV	End points, Gp. A, Subgp. 1, every 6 months

TYPE UDN-2841B thru UDN-2846B
QUAD 1.5 AMPERE DRIVERS

FEATURES

- Inputs Compatible with DTL/TTL/LS TTL/ CMOS/PMOS
- High Voltage Output: −50 V
- High Current Gain
- Sink from Negative Supply: UDN-2841B/UDN-2842B
- Source to Negative Supply: UDN-2843B/UDN-2844B
- Sink & Source Combination: UDN-2845B/UDN-2846B

THIS SERIES of quad Darlington based switches is especially designed for high-current, high-voltage peripheral driver applications. It is intended to provide solutions to interface problems involving electronic discharge printers, d-c motor drive (bipolar or unipolar), telephone relays, PIN diodes, LEDs, and other high-current loads operating from negative supplies.

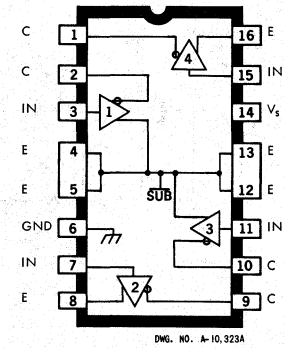
Types UDN-2841B and UDN-2842B are intended for sinking applications in which the load is connected **to ground and the I.C. device switches the negative supply. The input PNP transistor in each driver serves as a level translator and the first NPN stage provides sufficient current gain to drive the output Darlingtons.**

Type UDN-2843B and UDN-2844B quad drivers are primarily intended for switching the ground end of loads which utilize negative supply voltages. The NPN Darlington emitter follower outputs are operated as emitter followers in this application.

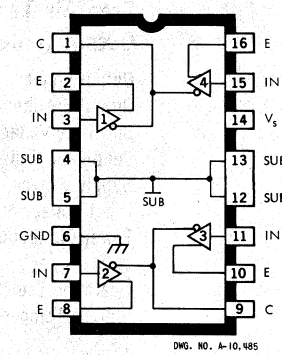
Type UDN-2845B and UDN-2846B devices are sink-and-source combinations in a single dual in-line package. Either device can be used for bipolar switching applications in which both ends of the load are floating.

The UDN-2841B, UDN-2843B, and UDN-2845B I.C.s are intended for use with 5 V TTL, Schottky TTL, DTL, and CMOS logic. The UDN-2842B, UDN-2844B, UDN-2845B, and UDN-2846B feature a higher input impedance and are intended for use with 8 V to 15 V PMOS and CMOS logic.

All types reduce component count, lower system cost, reduce circuit and board complexity, and provide solutions for many interface requirements.

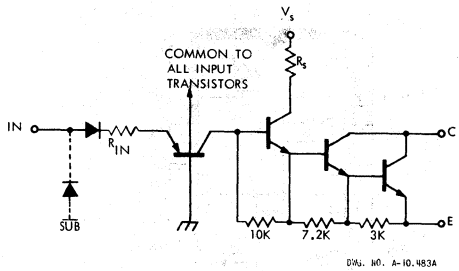


UDN-2841B, UDN-2842B, UDN-2845B, UDN-2846B



UDN-2843B, UDN-2844B

SCHEMATIC (each driver)



DWG. NO. A-10,483A

Type Number	Resistor Values in kΩ			
	Amplifier 1 & 3		Amplifier 2 & 4	
	R_{IN}	R_S	R_{IN}	R_S
UDN-2841B	3.3	15	3.3	15
UDN-2842B	10.5	15	10.5	15
UDN-2843B	3.3	1	3.3	1
UDN-2844B	10.5	1	10.5	1
UDN-2845B	3.3	15	3.3	1
UDN-2846B	10.5	15	10.5	1

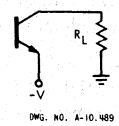
NOTE: The substrate terminals must be tied to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal device operation.

ABSOLUTE MAXIMUM RATINGS at +25°C Free-Air Temperature for any one Darlington Output (unless otherwise noted)

Output Voltage, $V_{CE(OFF)}$ ..... 50 V
Output Sustaining Voltage, $V_{CE(SUS)}$ ..... 35 V
Substrate Voltage, V_{SUB} ..... −50 V
Continuous Output Current, I_{OUT} ..... 1.75 A
Supply Voltage, V_S ..... See Table
Input Voltage, V_{IN} ..... See Table
Power Dissipation, P_D (one output) ..... 2.25 W*
(total package) ..... 2.77 W*
Operating Temperature Range, T_A ..... 0°C to +70°C
Storage Temperature Range, T_S ..... −55°C to +150°C

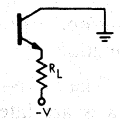
*Derate linearly to 0 W at +150°C.

Type Number	V_S (Max.)	V_{IN} (Max.)	Application
UDN-2841B	10 V	10 V	TTL, DTL, 5 V CMOS; current sink
UDN-2842B	15 V	15 V	8–15 V PMOS & CMOS; current sink
UDN-2843B	10 V	10 V	TTL, DTL, 5 V CMOS; current source
UDN-2844B	15 V	15 V	8–15 V PMOS & CMOS; current source
UDN-2845B	10 V	10 V	TTL, DTL, 5 V CMOS; source & sink
UDN-2846B	10 V	15 V	8–15 V PMOS & CMOS; source & sink



DWG. NO. A-10,489

Current Sink



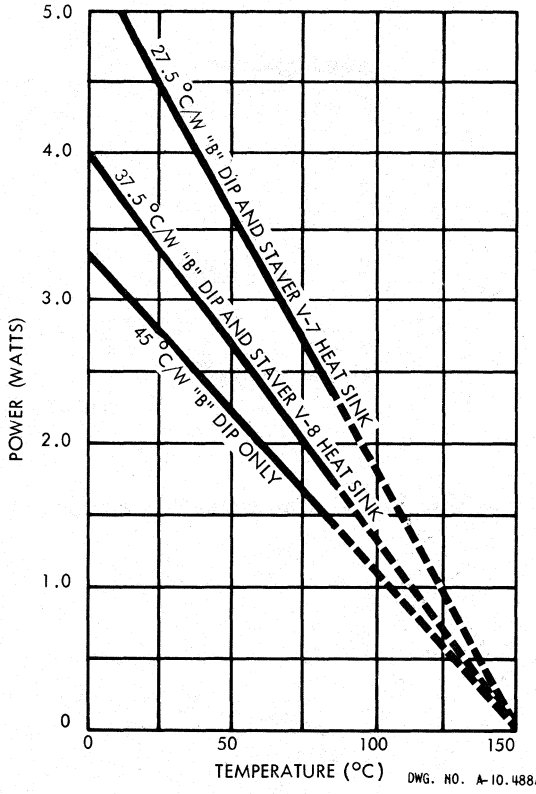
DWG. NO. A-10,490

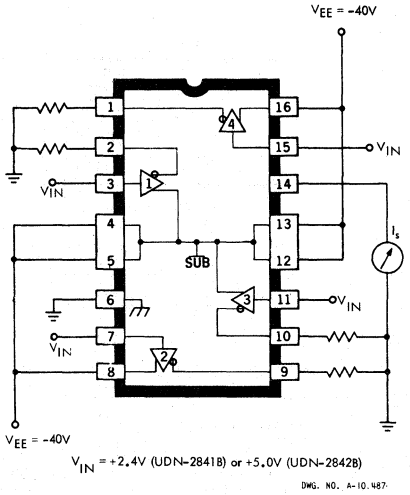
Current Source

ELECTRICAL CHARACTERISTICS at T_A = 25°C (unless otherwise noted), See Applicable Test Figure for Conditions not Specified

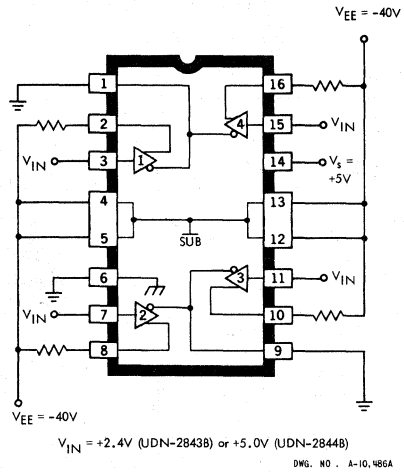
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{EE} = −50 V, V_{IN} = 0.4 V, T_A = 25°C	—	—	100	μA
		V_{EE} = −50 V, V_{IN} = 0.4 V, T_A = 70°C	—	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	V_{EE} = −50 V, V_{IN} = 0.4 V, I_{OUT} = 100 mA	35	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 500 mA	—	—	1.1	V
		I_{OUT} = 1.0 A (Note 1)	—	—	1.4	V
		I_{OUT} = 1.5 A (Note 1)	—	—	1.7	V
Input Current	$I_{IN(ON)}$	I_{OUT} = 500 mA, UDN-2841/43/45B	—	300	500	μA
		I_{OUT} = 500 mA, UDN-2842/44/46B	—	350	525	μA
Input Voltage (Note 1)	$V_{IN(ON)}$	I_{OUT} = 1.5 A, UDN-2841/43/45B	—	—	2.4	V
		I_{OUT} = 1.5 A, UDN-2842/44/46B	—	—	5.0	V
Supply Current (Note 1)	I_S	I_{OUT} = 500 mA, UDN-2841/42B, UDN-2845/46B (Note 2)	—	2.5	3.75	mA
		I_{OUT} = 500 mA, UDN-2843/44B, UDN-2845/46B (Note 3)	—	3.25	7.5	mA
Turn-On Delay	$t_{pd(ON)}$	R_L = 39Ω, 0.5 V_{IN} to 0.5 V_{OUT}	—	—	2.0	μs
Turn-Off Delay	$t_{pd(OFF)}$	R_L = 39Ω, 0.5 V_{IN} to 0.5 V_{OUT}	—	—	5.0	μs

NOTES:
1. Each driver tested separately.
2. Drivers 1 & 3 (sink drivers) only.
3. Drivers 2 & 4 (source drivers) only.

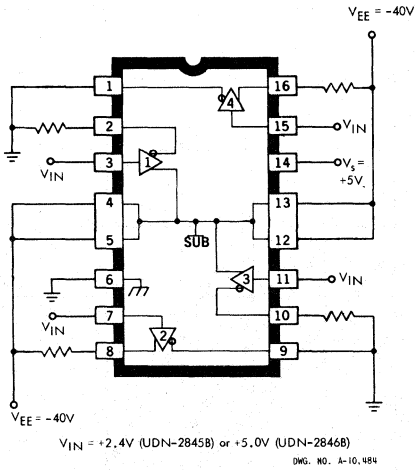




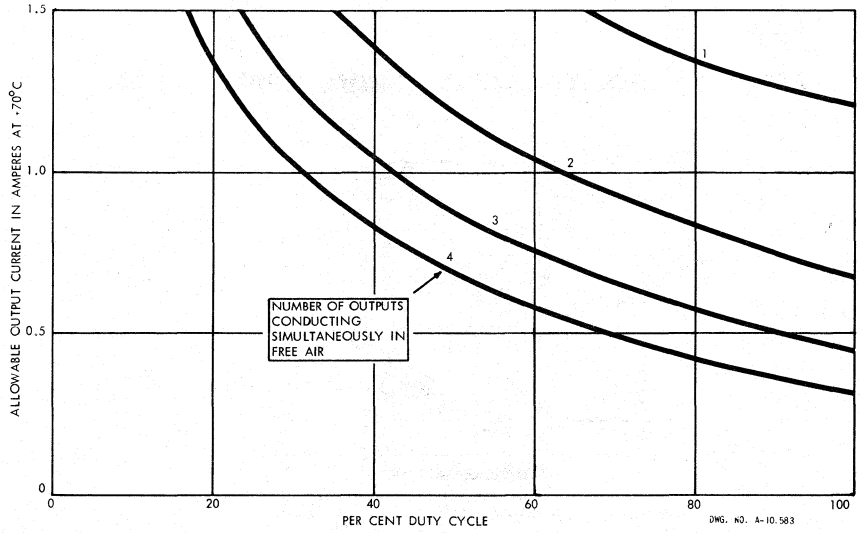
TYPE UDN-2841B and UDN-2842B TEST CIRCUIT

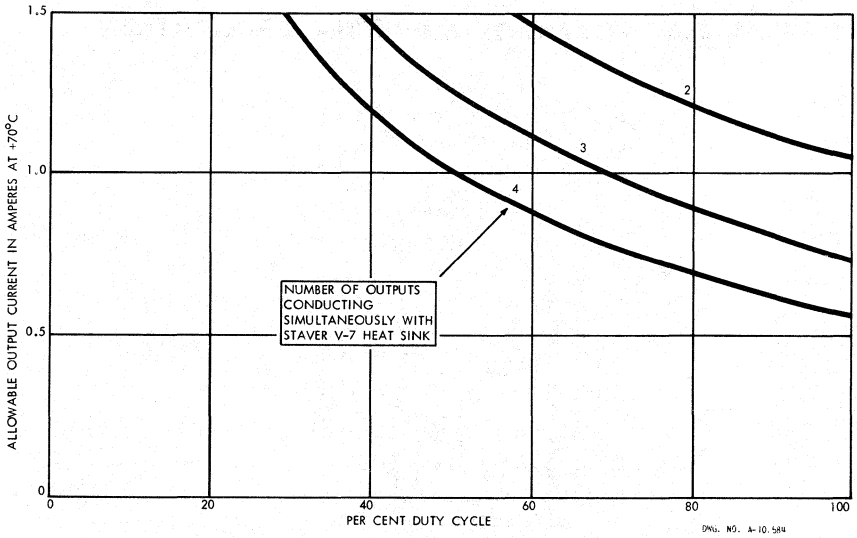


TYPE UDN-2843B and UDN-2844B TEST CIRCUIT



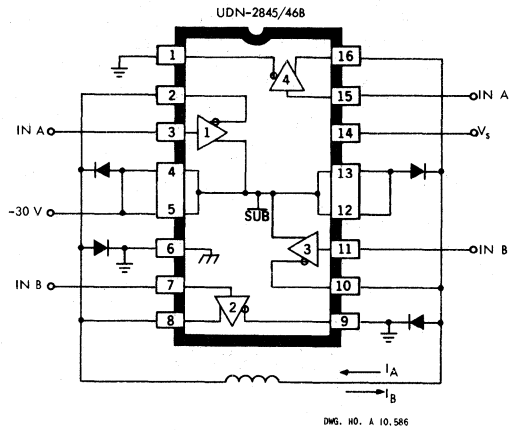
TYPE UDN-2845B and UDN-2846B TEST CIRCUIT


ALLOWABLE OUTPUT CURRENT IN AMPERES AT +70°C
1.5
1.0
0.5
0
0
20
40
60
80
100
PER CENT DUTY CYCLE
1
2
3
4
NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY IN FREE AIR
DWG. NO. A-10.583

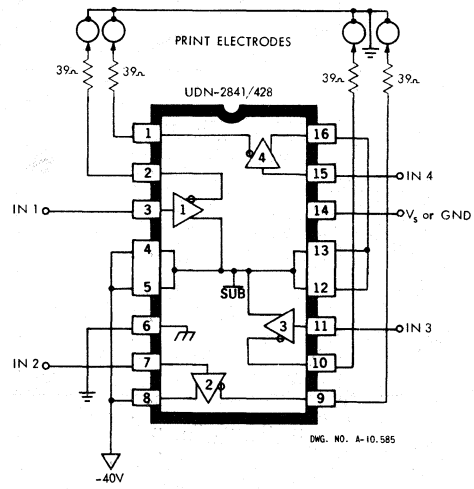

ALLOWABLE OUTPUT CURRENT IN AMPERES AT +70°C
1.5
1.0
0.5
0
0
20
40
60
80
100
PER CENT DUTY CYCLE
2
3
4
NUMBER OF OUTPUTS CONDUCTING SIMULTANEOUSLY WITH STAVER V-7 HEAT SINK
DWG. NO. A-10.584

4

TYPICAL BIPOLAR MOTOR DRIVE APPLICATION



TYPICAL ELECTROSENSITIVE PRINTER APPLICATION



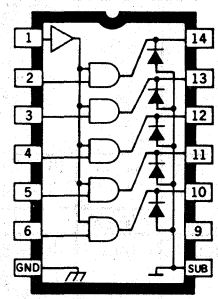
TYPE UDN-2956A and UDN-2957A HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

COMPRISED of five common collector NPN Darlington output stages, the associated common base PNP input stages, and a common "enable" stage, Type UDN-2956A and UDN-2957A high-voltage, high-current source drivers are used to switch the ground end of loads which are directly connected to a negative supply. Typical loads include telephone relays, PIN diodes, and LEDs. Both devices will sustain output OFF voltages of −80 V and will source currents to −500 mA per driver. Under normal operating conditions, these units will sustain load currents of −200 mA on each of the five drivers simultaneously at ambient temperatures up to +70°C.

The Type UDN-2956A driver is intended for use with MOS (PMOS or CMOS) logic input levels operating with supply voltages from 6 V to 16 V. The Type UDN-2957A driver has appropriate input current limiting resistors for operation from TTL, Schottky TTL, DTL, and 5 V CMOS. With either device, the input and enable levels must both be pulled towards the positive supply to activate the output load.

Integral transient suppression diodes allow these devices to be used with inductive loads without the need for discrete diodes. In order to maintain isolation between drivers, the substrate should be connected to the most negative supply in any event. All input connections are on one side of the dual in-line package, output connections on the other side to simplify printed wiring board layout.

The Type UDN-2956A and UDN-2957A high-voltage, high-current drivers are supplied in 14-lead dual in-line packages conforming to JEDEC outline TO-116 (MO-001AA). On special order, hermetically-sealed versions of these devices (with reduced package power dissipation capability) can also be furnished.



DWG. NO. A-10,229

4

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature (reference pin 7)

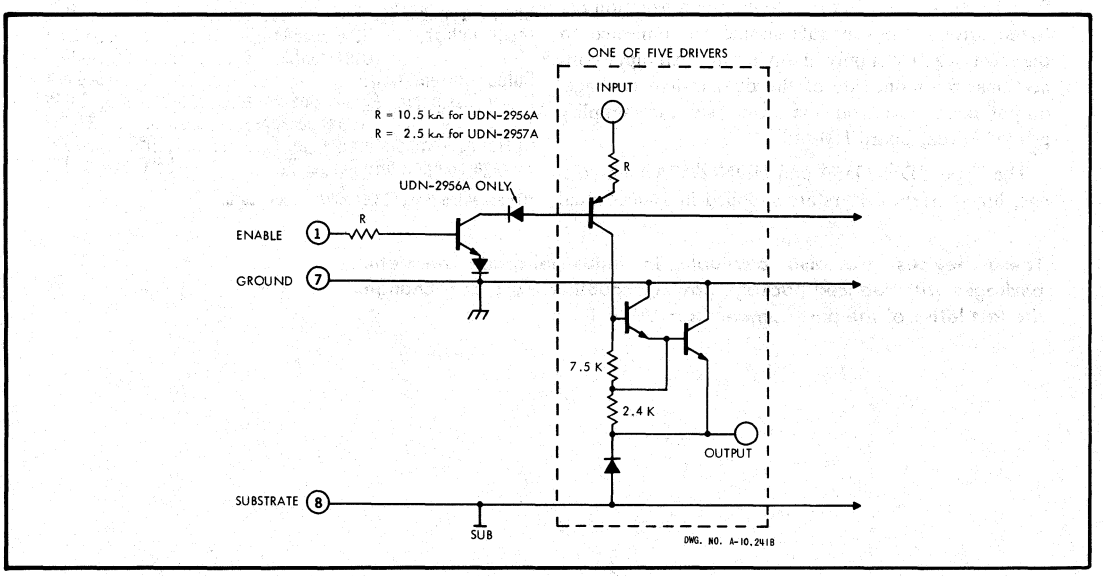
Supply Voltage, V_{EE} ..... −80 V
Input Voltage, V_{IN} (UDN-2956A) ..... +20 V
(UDN-2957A) ..... +10 V
Output Current, I_{OUT} ..... −500 mA
Power Dissipation, P_D any one driver ..... 1.0 W
(total package) ..... 2.0 W*
Operating Temperature Range, T_A ..... 0°C to +70°C
Storage Temperature Range, T_S ..... −55°C to +150°C

*Derate at the rate of 16.67 mW/°C above 25°C.

These devices are also available in industrial-grade hermetic packages with reduced package power capability. To order, change the last letter of the part number from 'A' to 'R'.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{ENABLE} = V_{IN}$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limit
Output Leakage Current	I_{CEX}	UDN-2956A	$V_{IN} = V_{ENABLE} = 0.8$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	−200 μA Max.
			$V_{IN} = 0.8$ V, $V_{ENABLE} = 15$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	−200 μA Max.
			$V_{IN} = 15$ V, $V_{ENABLE} = 0.8$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	−200 μA Max.
		UDN-2957A	$V_{IN} = V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = +70°$ C	−200 μA Max.
			$V_{IN} = 0.4$ V, $V_{ENABLE} = 3.85$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	−200 μA Max.
			$V_{IN} = 3.85$ V, $V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = 70°C$	−200 μA Max.
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	UDN-2956A	$V_{IN} = 6.0$ V, $I_{OUT} = 100$ mA	−1.10 V Max.
			$V_{IN} = 7.0$ V, $I_{OUT} = 175$ mA	−1.25 V Max.
			$V_{IN} = 10$ V, $I_{OUT} = -350$ mA	−1.60 V Max.
		UDN-2957A	$V_{IN} = 2.4$ V, $I_{OUT} = -100$ mA	−1.10 V Max.
			$V_{IN} = 2.7$ V, $I_{OUT} = -175$ mA	−1.25 V Max.
			$V_{IN} = 3.9$ V, $I_{OUT} = -350$ mA	−1.60 V Max.
Input Current	$I_{IN(ON)}$	UDN-2956A	$V_{IN} = 15$ V, $V_{OUT} = -2.0$ V	1.85 mA Max.
		UDN-2957A	$V_{IN} = 3.85$ V, $V_{OUT} = -2.0$ V	1.40 mA Max.
	$I_{IN(OFF)}$	ALL	$I_{OUT} = -500$ μA, $T_A = +70°C$	50 μA Min.
Output Source Current	I_{OUT}	UDN-2956A	$V_{IN} = 5.0$ V, $V_{OUT} = -2.0$ V	−125 mA Min.
			$V_{IN} = 6.0$ V, $V_{OUT} = -2.0$ V	−200 mA Min.
			$V_{IN} = 7.0$ V, $V_{OUT} = -2.0$ V	−250 mA Min.
			$V_{IN} = 8.0$ V, $V_{OUT} = -2.0$ V	−300 mA Min.
			$V_{IN} = 9.0$ V, $V_{OUT} = -2.0$ V	−350 mA Min.
		UDN-2957A	$V_{IN} = 2.4$ V, $V_{OUT} = -2.0$ V	−125 mA Min.
			$V_{IN} = 2.7$ V, $V_{OUT} = -2.0$ V	−200 mA Min.
			$V_{IN} = 3.0$ V, $V_{OUT} = -2.0$ V	−250 mA Min.
			$V_{IN} = 3.3$ V, $V_{OUT} = -2.0$ V	−300 mA Min.
			$V_{IN} = 3.6$ V, $V_{OUT} = -2.0$ V	−350 mA Min.
Clamp Diode Leakage Current	I_R	ALL	$V_R = 80$ V	50 μA Max.
Clamp Diode Forward Voltage	V_F	ALL	$I_F = 350$ mA	2.0 V Max.



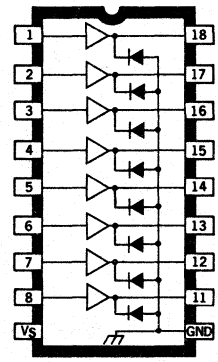
SERIES UDN-2980A
HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

RECOMMENDED for applications requiring separate logic and load grounds, load supply voltages to +80 V, and/or load currents to 500 mA, Series UDN-2980A source drivers are used to interface between standard low-power digital logic and relays, solenoids, stepping motors, LEDs, lamps, etc.

Under normal operating conditions, these devices will sustain 100 mA continuously on each of the eight outputs at an ambient temperature of +70°C and a supply of +15 V. All devices in this series incorporate input current limiting resistors and output transient suppression diodes.

The Type UDN-2981A and UDN-2983A drivers are for use with +5 V logic systems — TTL, Schottky TTL, DTL, and 5 V CMOS. The Type UDN-2982A and UDN-2984A drivers are intended for MOS interface (PMOS and CMOS) operating from supply voltages of 6 to 16 V. The UDN-2981A and UDN-2982A will sustain a maximum output OFF voltage of +50 V while the UDN-2983A and UDN-2984A will sustain an output voltage of +80 V. In all cases, the output is switched ON by an active high input level.

The Series UDN-2980A high-voltage, high-current source drivers are supplied in 18-lead dual in-line plastic packages. They can also be supplied, with reduced package power capability, in military-grade hermetic packages to the processing and environmental requirements of Military Standard MIL-STD-883, or industrial-grade dual in-line hermetic packages. To order, change the last letter of the part number from 'A' to 'H' or 'R', respectively.



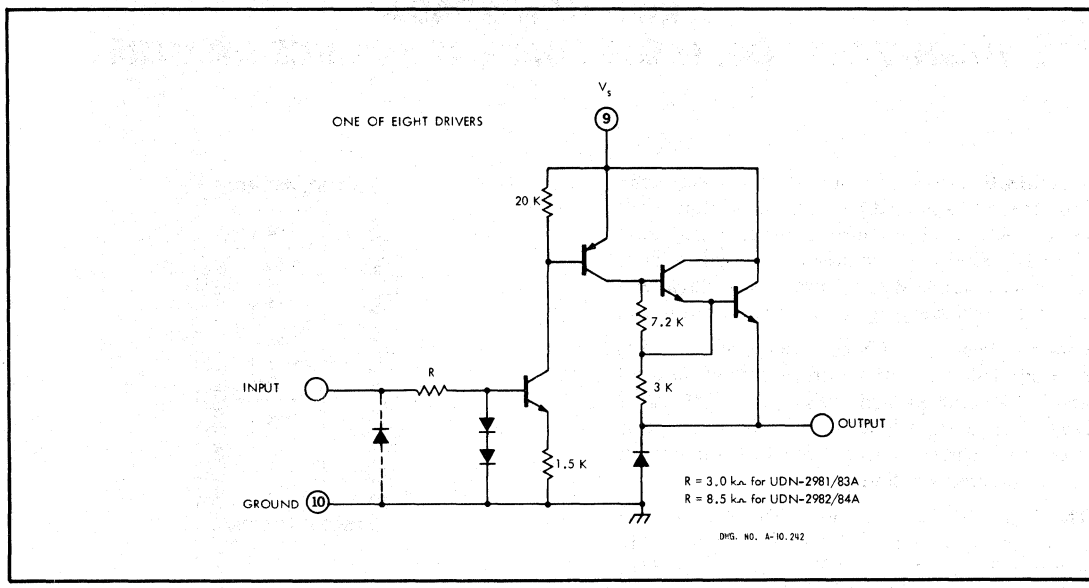
DWG. NO. A-10,243

4

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature

Output Voltage, V_{CE} (UDN-2981A & UDN-2982A) ..... +50 V
(UDN-2983A & UDN-2984A) ..... +80 V
Input Voltage, V_{IN} (UDN-2981A & UDN-2983A) ..... +15 V
(UDN-2982A & UDN-2984A) ..... +30 V
Output Current, I_{OUT} ..... −500 mA
Power Dissipation, P_D (any one driver) ..... 1.1 W
(total package) ..... 2.2 W*
Operating Temperature Range, T_A ..... 0°C to +70°C
Storage Temperature Range, T_S ..... −55°C to +150°C

*Derate at the rate of 18 mW/°C above 25°C.



ELECTRICAL CHARACTERISTICS at $T_A = +25°C$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limit
Output Leakage Current	I_{CEX}	UDN-2981/82A	V_{IN} = 0.4 V, V_S = 50 V, T_A = +70°C	200 μA Max.
		UDN-2983/84A	V_{IN} = 0.4 V, V_S = 80 V, T_A = +70°C	200 μA Max.
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	UDN-2981/83A	V_{IN} = 2.4 V, I_{OUT} = −100 mA	1.7 V Max.
			V_{IN} = 2.4 V, I_{OUT} = −225 mA	1.8 V Max.
			V_{IN} = 2.4 V, I_{OUT} = −350 mA	1.9 V Max.
		UDN-2982/84A	V_{IN} = 5.0 V, I_{OUT} = −100 mA	1.7 V Max.
			V_{IN} = 5.0 V, I_{OUT} = −225 mA	1.8 V Max.
			V_{IN} = 5.0 V, I_{OUT} = −350 mA	1.9 V Max.
Input Current	$I_{IN(ON)}$	UDN-2981/83A	V_{IN} = 2.4 V	575 μA Max.
			V_{IN} = 3.85 V	1.26 mA Max.
		UDN-2982/84A	V_{IN} = 5.0 V	680 μA Max.
			V_{IN} = 12 V	1.93 mA Max.
Output Source Current	I_{OUT}	UDN-2981/83A	V_{IN} = 2.4 V, V_{CE} = 2.0 V	−350 mA Min.
		UDN-2982/84A	V_{IN} = 5.0 V, V_{CE} = 2.0 V	−350 mA Min.
Supply Current (Outputs Open)	I_S	UDN-2981A	V_{IN} = 2.4 V (All Inputs), V_S = 50 V	10 mA Max.
		UDN-2982A	V_{IN} = 5.0 V (All Inputs), V_S = 50 V	10 mA Max.
		UDN-2983A	V_{IN} = 2.4 V (All Inputs), V_S = 80 V	10 mA Max.
		UDN-2984A	V_{IN} = 5.0 V (All Inputs), V_S = 80 V	10 mA Max.
Clamp Diode Leakage Current	I_R	UDN-2981/82A	V_R = 50 V, V_{IN} = 0 V	50 μA Max.
		UDN-2983/84A	V_R = 80 V, V_{IN} = 0 V	50 μA Max.
Clamp Diode Forward Voltage	V_F	ALL	I_F = 350 mA	2.0 V Max.

SERIES TPP
MEDIUM-POWER DARLINGTON ARRAYS
In Dual In-Line Plastic Packages

SPRAGUE Series TPP devices are medium-power Darlington arrays, consisting of 1, 2, 3 or 4 discrete Darlington chips in a single 14-pin package. These devices complement Sprague's Series TPQ quad transistor arrays.

All of these devices are furnished in the industry standard T0-116 (or M0-001AA) 14-lead dual in-line plastic package. The molded package is identical to that used in most consumer integrated circuits and offers superior mechanical protection during insertion into printed wiring boards.

TYPICAL RATINGS (Max.)

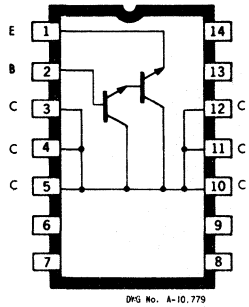
Power Dissipation, P_D (total package) . . . . . 2 W*
Operating Temperature Range, T_A . . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . . −65°C to +150°C
*Derate at the rate of 15 mW/°C above T_A = +25°C

STANDARD RATINGS

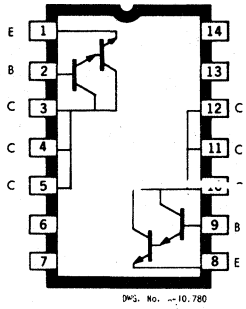
	Type Number			
	TPP-1000	TPP-2000	TPP-3000	TPP-4000
Devices/Package	1	2	3	4
Max. Total Power Dissipation, P_D @ 25°C	2 Watts			
BV_{CES} @ 100 μA	40 Volts			
BV_{CBO} @ 100 μA	50 Volts			
BV_{EBO} @ 100 μA	12 Volts			
I_{CBO} @ 30 V	100 nA			
I_{EBO} @ 10 V	100 nA			
V_{CE} @ 1A, 1mA	1.5 Volts Max. 1.0 Volts Typ.			
V_{BE} @ 1A, 1mA	2.0 Volts Max. 1.6 Volts Typ.			
H_{FE} @ 500 mA, 5V @ 1 A, 5V @ 2 A, 5V	2K Min.			
I_C Max	4 Amps			

Additional information on these devices is available from Sprague Electric Co., 70 Pembroke Road, Concord, New Hampshire 03301, Telephone 603-224-1961.

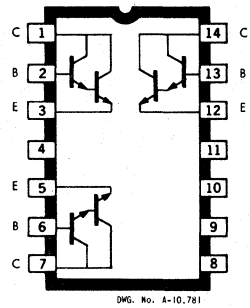
SERIES TPP (Cont'd)



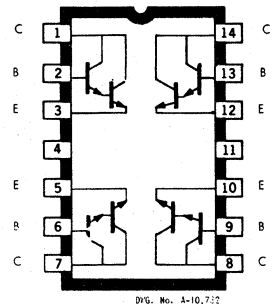
TPP-1000



TPP-2000



TPP-3000



TPP-4000

SERIES TPQ QUAD TRANSISTOR ARRAYS
In Dual In-Line Plastic Packages

THE SPRAGUE Series TPQ quad transistor arrays are general-purpose silicon transistor arrays consisting of four independent transistors. Shown are eight NPN types, five PNP types, and nine NPN/PNP dual complementary pairs.

All of these devices are furnished in the industry standard TO-116 (or MO-001AA) 14-lead dual in-line plastic package. The molded package is identical to that used in most consumer integrated circuits and offers superior mechanical protection during insertion into printed wiring boards.

TYPICAL RATINGS (Max.)

Power Dissipation, P_D
(each transistor).....500 mW
(total package).....1700 mW*

Operating Temperature
Range, T_A.....0°C to +85°C

Storage Temperature
Range, T_S.....−65°C to +150°C

*Derate at the rate of 1.79 mW/° C above T_A=+55° C

STANDARD RATINGS

Type No.	BV_{CBO} V Min.	BV_{CEO} V Min.	BV_{EBO} V Min.	I_{CBO} nA Max.	D-C Current Gain, h_{FE} Limits Min.	Max.	@ I_C mA	& V_{CE} V	f_T MHz Min.	C_{ob} pF Max.	$V_{CE(SAT)}$ mV Max.	@ I_C mA	Similar Discrete Devices
Four NPN Devices – Figure 1													
TPQ2221	60	40	5	50	40	—	150	10	200	8.0	400	150	2N2221
TPQ2222	60	40	5	50	100	—	150	10	200	8.0	400	150	2N2222
TPQ2483	60	40	6	20	100	—	0.1	5	50	6.0	350	1.0	2N2483
TPQ2484	60	40	6	20	200	—	0.1	5	50	6.0	350	1.0	2N2484
TPQ3724	50	30	5	500	35	—	100	1	250	8.0	450	500	2N3724
TPQ3725	60	40	5	500	35	200	100	1	250	10.0	450	500	2N3725
TPQ3725A	70	50	5	500	40	—	100	1	200	10.0	450	500	2N3725A
TPQ3904	60	40	6	50	75	—	10	1	250	4.0	200	10	2N3904
Four PNP Devices – Figure 2													
TPQ2906	60	40	5	50	40	—	150	10	200	8.0	400	150	2N2906
TPQ2907	60	40	5	50	100	—	150	10	200	8.0	400	150	2N2907
TPQ3798	60	40	5	10	150	—	0.1	5	60	4.0	250	1.0	2N3798
TPQ3799	60	60	5	10	300	—	0.1	5	60	4.0	250	1.0	2N3799
TPQ3906	40	40	5	50	75	—	10	1	200	4.5	250	10	2N3906
Two NPN/Two PNP Devices – Figure 3													
TPQ6001	60	30	5	30	40	—	150	10	200	8.0	400	150	2N2221/2N2906
TPQ6002	60	30	5	30	100	—	150	10	200	8.0	400	150	2N2222/2N2907
TPQ6100	60	40	5	10	75	—	1.0	5	50	4.0	250	1.0	2N2483/2N3798
TPQ6100A	60	45	5	10	150	—	1.0	5	50	4.0	250	1.0	2N2484/2N3799
Two NPN/Two PNP Devices – Figure 4													
TPQ6501	60	30	5	30	40	—	150	10	200	8.0	400	150	2N2221/2N2906
TPQ6502	60	30	5	30	100	—	150	10	200	8.0	400	150	2N2222/2N2907
TPQ6600	60	40	5	10	75	—	1.0	5	50	4.0	250	1.0	2N2483/2N3798
TPQ6600A	60	45	5	10	150	—	1.0	5	50	4.0	250	1.0	2N2484/2N3799
TPQ6700	40	40	5	50	70	—	10	1	200	4.5	250	10	2N3904/2N3906

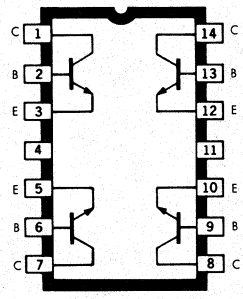


Figure 1

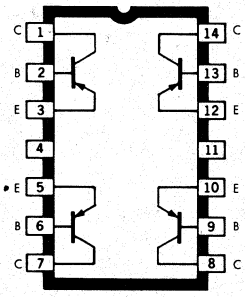


Figure 2

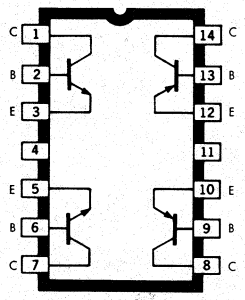


Figure 3

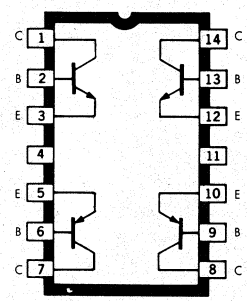
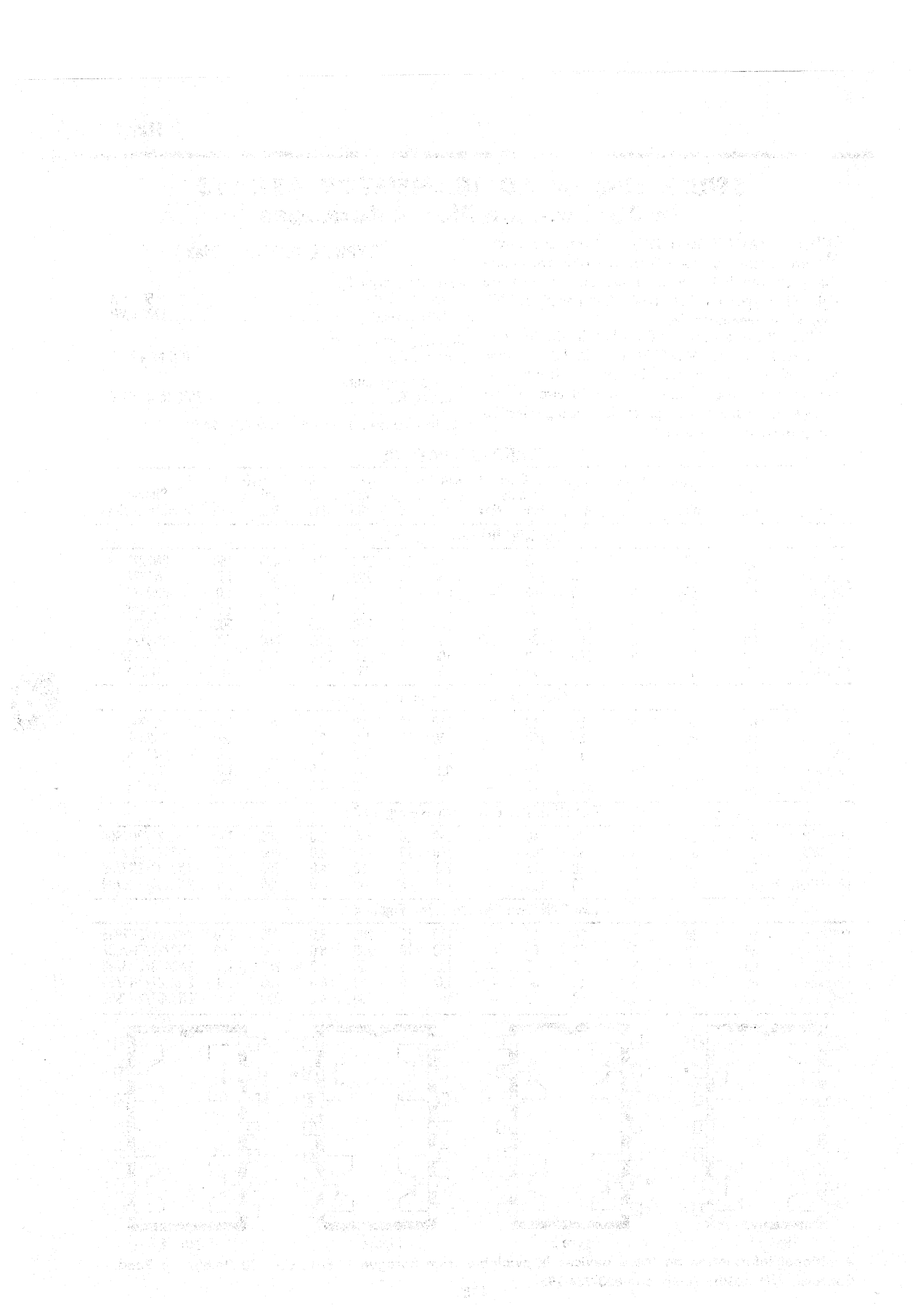


Figure 4

Additional information on these devices is available from Sprague Electric Co., 70 Pembroke Road, Concord, NH 03301, Telephone 603-224-1961.



Device Type	Description
UCN-4103A	Crystal Oscillator/Divider (3×2^{14})
UCN-4105A	RC Oscillator/Divider (2^{14} or 2^{15})
UCN-4112A/M	Crystal Oscillator/Divider (2^{16})
UCN-4116A/M	Crystal Oscillator/Divider (2^{16})
UCN-4123M	Crystal Oscillator/Divider (3×2^{14})
UCN-4401A	Latch/Driver (4 Sink Outputs at 500 mA & 50 V)
UCN-4801A	Latch/Driver (8 Sink Outputs at 500 mA & 50 V)
UCN-4805A	Latch Decoder/Driver (8 Source Outputs at 40 mA & 60 V)
UCN-4806A	Latch Decoder/Driver (8 Source Outputs at 40 mA & 60 V)
UCN-4810A	Serial-to-Parallel Latch/Driver (10 Source Outputs at 40 mA & 60 V)
UCN-4815A	Latched Driver (8 Source Outputs at 40 mA & 60 V)

Operating and Handling Practices for MOS Integrated Circuits

Handling Practices - Packaged Devices

Sprague Electric incorporates input protection diodes in all of its MOS/CMOS devices. Because of the very high input resistance in MOS devices, the following practices should be observed for protection against high static electrical charges:

1. Device leads should be in contact with a conductive material except when being tested or in actual operation.
2. Conductive parts of tools, fixtures, soldering irons and handling equipment should be grounded.
3. Devices should not be inserted into or removed from test stations unless the power is off.
4. Neither should signals be applied to the inputs while the device power supply is in an off condition.
5. Unused input leads should be committed to either V_{SS} or V_{DD}.

Handling Practices - Die

A conductive carrier should be used in order to avoid differences in voltage potential.

Automatic Handling Equipment

Grounding alone may not be sufficient and feed mechanisms should be insulated from the devices under test at the point where the devices are connected to the test equipment. Ionized air blowers can be of aide here and are available commercially. This method is very effective in eliminating static electricity problems.

Ambient Conditions

Dry weather with accompanying low humidity tends to intensify the accumulation of static charges on any surface. In this atmosphere, proper handling procedures take on added importance. If necessary, steam injectors can be procured commercially.

Alert Failure Modes

The common failure modes that appear when static energy exists and when proper handling practices are not used are:

1. Shorted input protection diodes.
2. Shorted or 'blown' open gates.
3. Open metal runs.

Simple diagnostic checks with curve tracers or similar equipment readily identifies the above failure modes.

UCN-4103A/23M OSCILLATOR/FREQUENCY DIVIDERS FOR AUTOMOTIVE CLOCK APPLICATIONS

FEATURES

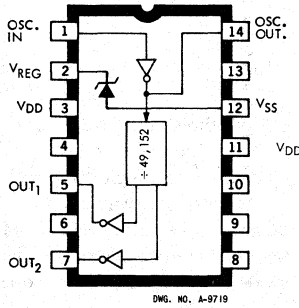
- Metal Gate Ion-Implanted CMOS
- Internal 12V Regulator
- Buffered Outputs
- Plastic Dual In-Line Package

SPECIFICALLY designed for use in automotive applications, the UCN-4103A/23M CMOS circuits consist of an oscillator inverter, a frequency divider, and buffer amplifiers. Only a minimum number of external components are needed for a complete clock.

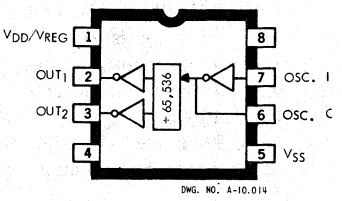
The buffered output of 60 or 64 Hz is suitable for directly driving most clock motor assemblies. The crystal frequency in these applications would be 2.949 MHz or 3.146 MHz, respectively.

On special order, the UCN-4123M Oscillator/Frequency Divider is also available with additional divider stages (÷65,536 total) to allow operation with crystal frequencies of 4.194 MHz or 3.932 MHz to produce the 64 Hz or 60 Hz outputs.

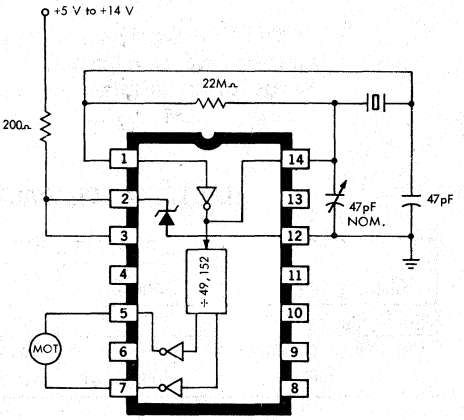
The Type UCN-4103A Oscillator/Frequency Divider is furnished in a standard 14-pin dual in-line plastic 'A' package. The Type UCN-4123M is furnished in a standard 8-pin dual in-line plastic 'M' package.



TYPE UCN-4103A



TYPE UCN-4123M



TYPICAL APPLICATION

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD} - V_{SS}$ (UCN-4103A) . . . . . +15 V
V_{REG} . . . . . See Note
Zener Current, I_{REG} . . . . . 15 mA
Operating Temperature Range, T_A . . . . . −30°C to +80°C
Storage Temperature Range, T_S . . . . . −55°C to +125°C

NOTE: The allowable V_{REG} is dependent on the value of an external current limiting resistor and is +10 V at 0 Ω.

ELECTRICAL CHARACTERISTICS: V_{SS} = 0 V, T_A = 25°C

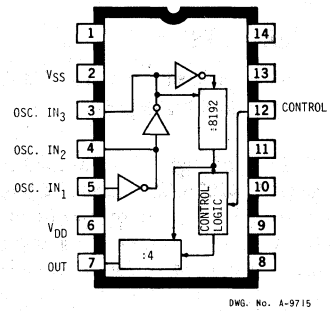
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Supply Current	I_{AVG}	V_{DD} = 10V, f_{IN} = 3, 145, 728Hz	—	1.8	mA
Zener Voltage	V_{REG}	I_{REG} = 100μA	10	13	V
Output Source Current	$I_{OUT\ (source)}$	V_{DD} = 4V, V_{OUT} = 3V	2	—	mA
Output Sink Current	$I_{OUT\ (sink)}$	V_{DD} = 4V, V_{OUT} = 1V	−2	—	mA
Upper Frequency Response	f_{IN}	V_{DD} = 4V	3.146	—	MHz

CAUTION: Sprague CMOS devices feature input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

TYPE UCN-4105A OSCILLATOR/FREQUENCY DIVIDER FOR TIMER APPLICATIONS

FEATURES

- Low Threshold, Metal Gate, Ion-Implanted CMOS
- 2V to 5V Operation
- Buffered Outputs
- Static Charge Protection



DWG. No. A-9715

THE TYPE UCN-4105A is a low-threshold CMOS circuit consisting of 3 oscillator inverters, a 15-stage ripple counter, and associated control logic. In normal operation, the 18.2Hz oscillator frequency is divided by 2^{14} or 2^{15} to provide an output pulse every 15 or 30 minutes. By adjustment of the three external components, other timing periods may be obtained.

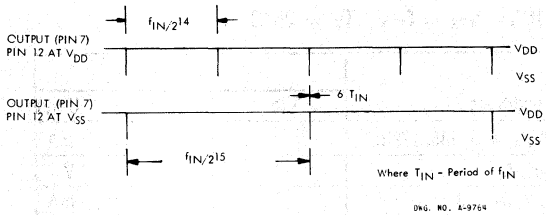
This device is available in a 14-pin dual in-line plastic 'A' package. On special order, devices for operation at higher supply voltages are obtainable.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD} - V_{SS}$ ..... +5V
Operating Temperature Range, T_A ..... −30°C to +80°C
Storage Temperature Range, T_S ..... −55°C to +125°C

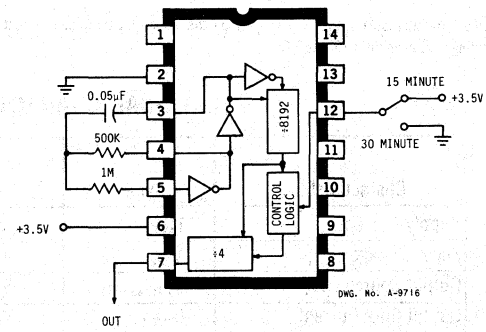
ELECTRICAL CHARACTERISTICS: V_{SS} = 0 V, T_A = +25°C

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Supply Current	I_{DD}	V_{DD} = 3.5V, No Load, f_{IN} = 18.2Hz	—	250	μA
Osc. Source Resistance	R_{OSC}	V_{DD} = 2V, V_5 = 2V, Pin 3 or Pin 4	—	10	kΩ
Output Current	$I_{OUT\ (source)}$	V_{DD} = 2V, V_{OUT} = 0.6V	1.0	—	mA



DWG. NO. A-9764

TYPICAL WAVEFORM



DWG. No. A-9716

TYPICAL APPLICATION ($f_{IN} \simeq$ 18.2Hz)

UCN-4112 OSCILLATOR/FREQUENCY DIVIDERS FOR AUTOMOTIVE CLOCK APPLICATIONS

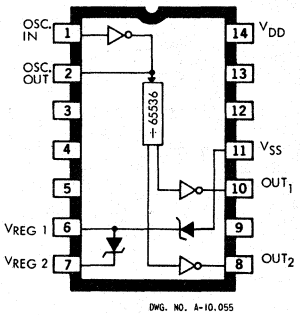
FEATURES

- Metal Gate Ion-Implanted CMOS
- Internal Zener Diode Regulator
- Buffered Outputs
- Plastic Dual In-Line Package

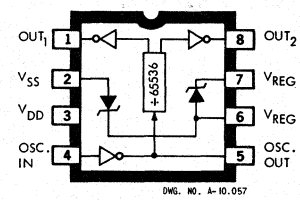
CONSISTING of an oscillator inverter, a frequency divider, buffer amplifiers, and two Zener diode regulators, the Series UCN-4112 low-threshold CMOS circuits are designed for synchronous motor applications. These devices are operable over a wide temperature range, over a wide supply voltage range, and feature very low power consumption. All of these features allow the Series UCN-4112 Oscillator/Frequency Dividers to be particularly suitable for use in automotive applications.

Complementary, low-impedance outputs of 48 Hz with a crystal frequency of 3.146 MHz or 30 Hz with a crystal frequency of 1.966 MHz can be used to directly drive most clock motor assemblies. Alternatively, crystal frequencies of 4.194 MHz or 3.932 MHz can be used to produce output frequencies of 64 or 60 Hz, respectively.

The Type UCN-4112A Oscillator/Frequency Divider is furnished in a standard 14-pin dual in-line plastic 'A' package. The Type UCN-4112M is furnished in a standard 8-pin dual in-line 'M' package. On special order, these devices are also available in a 16-pin dual in-line plastic package.



UCN-4112A



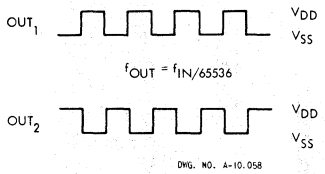
UCN-4112M

ABSOLUTE MAXIMUM RATINGS

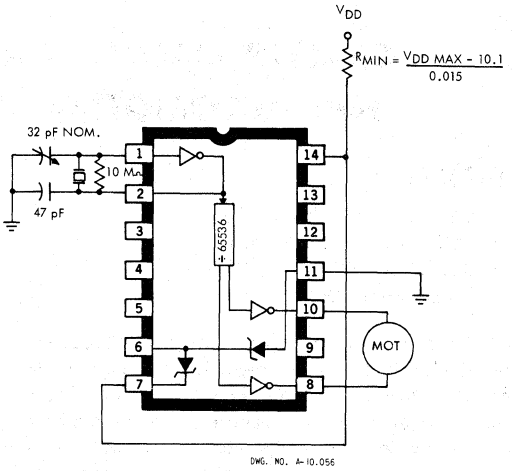
Supply Voltage, V_{DD}—V_{SS} ..... +15 V
Zener Current, $I_{REG\ 1}$ or $I_{REG\ 2}$ ..... 15 mA
Operating Temperature Range, T_A ..... −30°C to +80°C
Storage Temperature Range, T_S ..... −55°C to +125°C

ELECTRICAL CHARACTERISTICS: V_{SS} = 0 V, T_A = 25°C

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Supply Current	I_{AVG}	V_{DD} = 12 V, f_{IN} = 3,145, 728 Hz	—	2.6	mA
		V_{DD} = 6 V, f_{IN} = 3,145, 728 Hz	—	1.1	mA
		V_{DD} = 12 V, f_{IN} = 1,966, 080 Hz	—	1.8	mA
		V_{DD} = 6 V, f_{IN} = 1,966, 080 Hz	—	0.75	mA
Zener Voltage	$V_{REG\ 1}$	$I_{REG\ 1}$ = 250 μA	5.0	—	V
	$V_{REG\ 2}$	$I_{REG\ 2}$ = 2.5 mA, ref. $V_{REG\ 1}$	5.1	—	V
Output Resistance	R_{OUT}	V_{DD} = 4 V, I_{OUT} = 5.1 mA	—	170	Ω
Upper Freq. Response	f_{IN}	V_{DD} = 3.8 V	3.146	—	MHz
		V_{DD} = 3.5 V	1.966	—	MHz



TYPICAL WAVEFORMS



TYPICAL APPLICATION

UCN-4116M OSCILLATOR/FREQUENCY DIVIDER FOR AUTOMOTIVE CLOCK APPLICATIONS

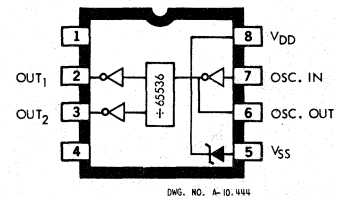
FEATURES

- Metal Gate Ion-Implanted CMOS
- Internal Zener Diode Regulator
- Buffered Outputs
- Plastic Dual In-Line Package

SPECIFICALLY DESIGNED for use in automotive applications, the Type UCN-4116M oscillator/frequency divider will drive synchronous clock motors in a push-pull configuration. The Zener diode regulator serves the dual function of voltage regulation and protection from automotive electrical system transients, spikes, and noise.

The buffered output of 60 or 64 Hz is suitable for directly driving most clock motor assemblies. The crystal frequency in these applications would be 3.932 MHz or 4.194 MHz, respectively. The oscillator/frequency divider will accommodate other quartz crystal frequencies in the 2 to 10 MHz range for use in other applications.

The Type UCN-4116M oscillator/frequency divider is supplied in a standard 8-pin "mini-DIP" dual in-line plastic package.



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD} - V_{SS}$ ..... Note 1
Zener Current, I_Z ..... 15 mA
Package Power Dissipation, P_D ..... 330 mW (Note 2)
Operating Temperature Range, T_A ..... −30°C to +80°C
Storage Temperature Range, T_S ..... −55°C to +125°C

Notes:
1. Dependent on value of external current limiting resistor and is 12 V at 0 Ω.
2. Derate at the rate of 3.3 mW/°C above T_A = +25°C.

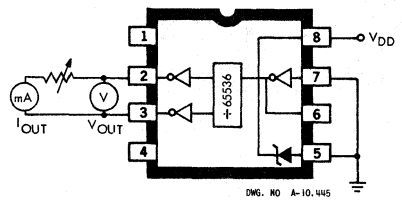
5

ELECTRICAL CHARACTERISTICS: V_{SS} = 0 V, T_A = +25°C

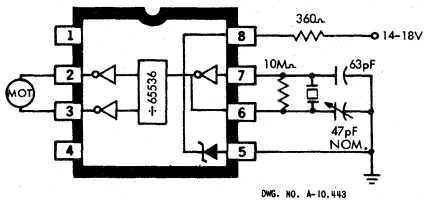
Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Supply Current	I_{AVG}	V_{DD} = 12 V, f_{IN} = 3,932,160 Hz, Outputs Open-Circuited	—	5	mA
Zener Voltage	V_Z	I_Z = 100 μA	12.5	15.5	V
Output Current	I_{OUT}	V_{DD} = 10 V, V_{OUT} = ±6.5 V	±20	—	mA
Upper Frequency Response	f_{IN}	V_{DD} = 5 V	3.932	—	MHz

• • •

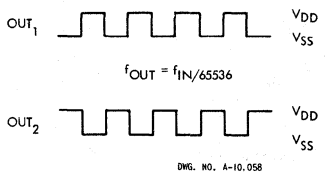
CAUTION: Sprague CMOS devices feature input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.



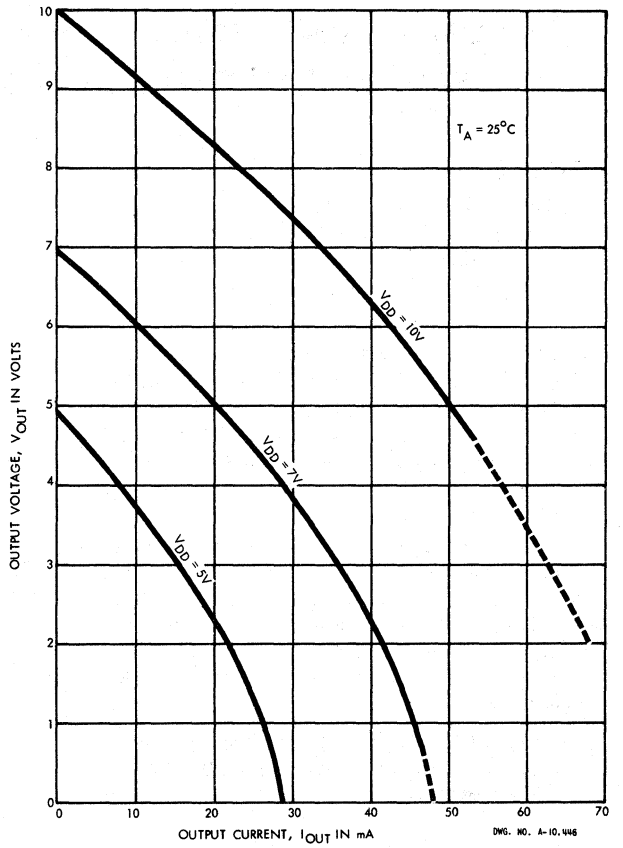
TEST CIRCUIT



TYPICAL APPLICATION



Typical Waveforms



THE UCN-4123M OSCILLATOR/FREQUENCY DIVIDER IS SHOWN ON PAGE 5—3.

UCN-4401A and UCN-4801A
BiMOS LATCH/DRIVERS

FEATURES

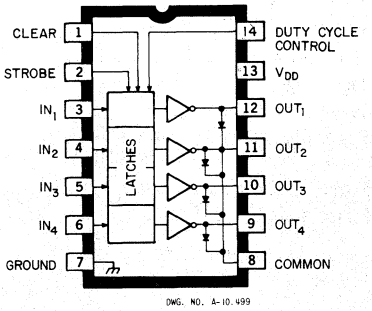
- High-Voltage, High-Current Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

THESE high-voltage, high-current latch/drivers are comprised of four or eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and DUTY CYCLE CONTROL functions. The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. The UCN-4401A contains four latch/drivers while the UCN-4801A contains eight latch/drivers.

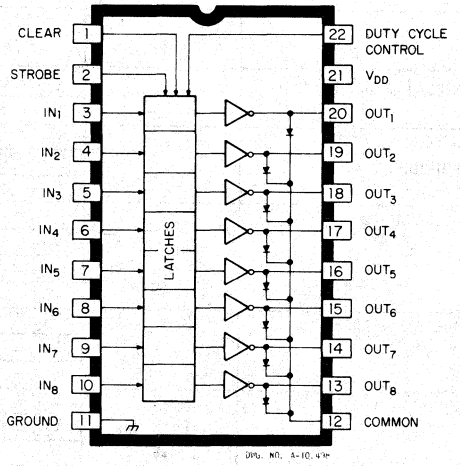
The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads.

Both units feature open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

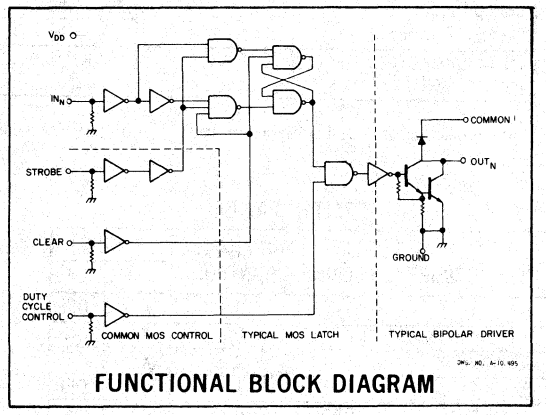
The UCN-4401A 4-latch device is furnished in a standard 14-pin dual in-line plastic package. The UCN-4801A 8-latch device is furnished in a 22-pin dual in-line plastic package with lead centers on 0.400" (10.16 mm) spacing. All outputs are pinned opposite their respective inputs to simplify circuit board layout.



TYPE UCN-4401A



TYPE UCN-4801A



FUNCTIONAL BLOCK DIAGRAM

5

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE} ..... 50 V
Supply Voltage, V_{DD} ..... 18 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Continuous Collector Current, I_C ..... 500 mA
Package Power Dissipation, P_D (UCN-4401A) ..... 1.67 W*
(UCN-4801A) ..... 2.0 W**
Operating Ambient Temperature Range, T_A ..... 0°C to +70°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*Derate at the rate of 16.7 mW/°C above T_A = 25°C.
**Derate at the rate of 20 mW/°C above T_A = 25°C.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{DD} = 5 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V, T_A = +25°C	—	—	50	μA
		V_{CE} = 50 V, T_A = +70°C			100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	0.9	1.1	V
		I_C = 200 mA		1.1	1.3	V
		I_C = 350 mA, V_{DD} = 7.0V	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	V_{DD} = 15 V	13.5	—	—	V
		V_{DD} = 10 V	8.5	—	—	V
		V_{DD} = 5.0 V (See note)	3.5	—	—	V
Input Resistance	R_{IN}	V_{DD} = 15 V	50	200	—	kΩ
		V_{DD} = 10 V	50	300	—	kΩ
		V_{DD} = 5.0 V	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each stage)	V_{DD} = 15 V	—	1.0	2.0	mA
		V_{DD} = 10 V	—	0.9	1.7	mA
		V_{DD} = 5.0 V	—	0.7	1.0	mA
	$I_{DD(OFF)}$	All Drivers OFF	—	50	100	μA
Clamp Diode Leakage Current	I_R	V_R = 50 V, T_A = +25°C	—	—	50	μA
		V_R = 50 V, T_A = +70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.7	2.0	V

*Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "1".

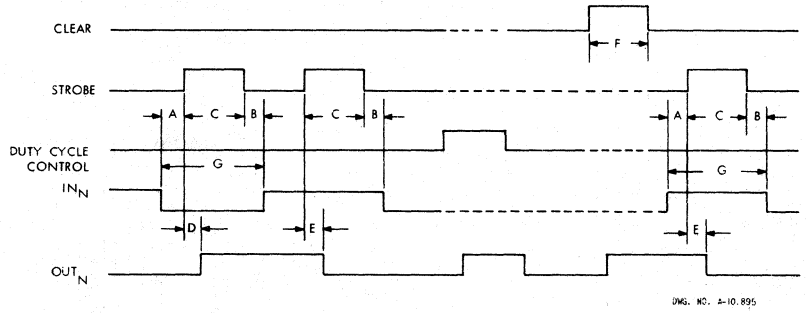
TRUTH TABLE

IN_N	STROBE	CLEAR	DUTY CYCLE CONTROL	OUT_N	
				t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

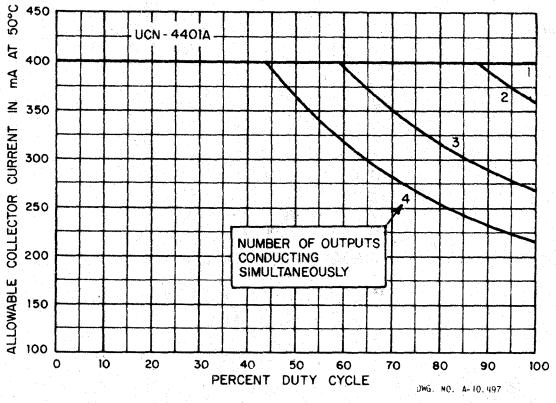
X = irrelevant
t-1 = previous output state
t = present output state

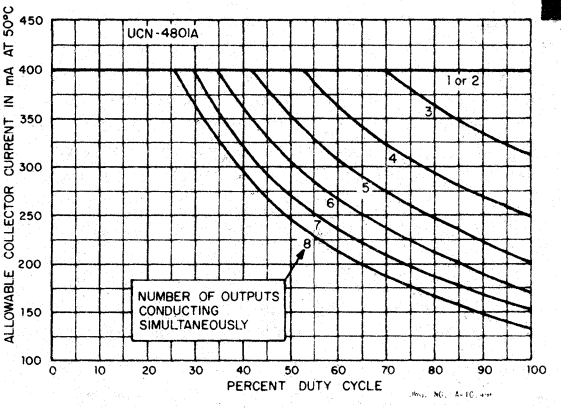
Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high DUTY CYCLE CONTROL will set all outputs to the OFF condition regardless of any other input conditions. When the DUTY CYCLE CONTROL is low, the outputs depend on the state of their respective latches.

TIMING CONDITIONS



A. Minimum data active time before strobe enabled (data set-up time) ..... 100 ns
B. Minimum data active time after strobe disabled (data hold time) ..... 100 ns
C. Minimum strobe pulse width ..... 300 ns
D. Typical time between strobe activation and output on to off transition ..... 250 ns
E. Typical time between strobe activation and output off to on transition ..... 250 ns
F. Minimum clear pulse width ..... 300 ns
G. Minimum data pulse width ..... 300 ns





CAUTION: Sprague CMOS devices feature input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

UCN-4805A and UCN-4806A
BiMOS LATCHED DECODER/DRIVERS

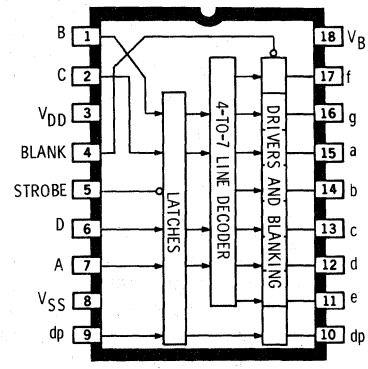
FEATURES

- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Hexadecimal Decoding
- Internal Pull-Up/Pull-Down Resistors
- Wide Supply Voltage Range

DESIGNED for use in high-voltage vacuum fluorescent display driver applications, the UCN-4805A and UCN-4806A latched decoder/drivers combine CMOS logic with bipolar source outputs. Both devices consist of eight high-voltage bipolar sourcing outputs with internal pull-down resistors and CMOS input latches, hexadecimal decoder, and control circuitry (strobe and blanking).

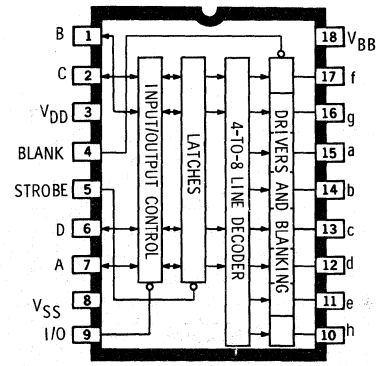
The UCN-4805A BiMOS latched decoder/driver is intended to serve as the segment driver with standard 7-segment displays incorporating a colon or decimal point. The UCN-4806A modification is designed for use with centered "1" (9-segment) displays. It has an I/O input to permit interrogating the input latches for error-checking purposes. Both ICs use hexadecimal decoding to display 0-9, A, b, C, d, E, and F.

Both BiMOS latched decoder/drivers have sufficient speed to permit operation with most microprocessor/LSI-based systems. The CMOS input latches provide operation over the supply voltage range of 5 to 15 volts with minimum logic loading. Internal output pull-down resistors eliminate the need for external components usually required for fluorescent display applications. When used with standard TTL or low speed TTL logic, both devices may require employment of input pull-up resistors to insure a proper input logic high.



Dwg. No. A-10,984

UCN-4805A



Dwg. No. A-10,983

UCN-4806A

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature and V_{SS} = 0 V

Output Voltage, V_{OUT} ..... 60 V
Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 18 V
Driver Supply Voltage Range, V_{BB} ..... 5.0 V to 60 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} ..... 40 mA
Package Power Dissipation, P_D ..... 1.82 W*
Operating Temperature Range, T_A ..... 0°C to +70°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*Derate at the rate of 18.18 mW/°C above T_A = 25°C.

Number of Outputs ON (I_{OUT} = 25 mA)	Max. Allowable Duty Cycle at Ambient Temperature of 50°C	60°C	70°C
8	100%	92%	78%
7	|	100%	89%
6	|	|	100%
1	100%	100%	100%

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{BB} = 60 V, V_{DD} = 4.75 V to 15.75 V, V_{SS} = 0 V (unless otherwise noted)

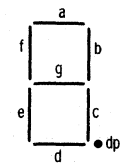
Characteristic	Symbol	Test Conditions	Limits Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = 25 mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	−400	−850	μA
Output Leakage Current		T_A = 70°C	—	15	μA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 15 V	13.5	15.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = 5.0 V	—	100	μA
		V_{DD} = 15 V	—	300	μA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Supply Current	I_{BB}	Display "8"	—	9.1	mA
		All outputs OFF	—	100	μA
	I_{DD}	V_{DD} = STROBE = 5.0 V, All other inputs = 0 V	—	200	μA
		V_{DD} = STROBE = 15 V, All other inputs = 0 V	—	500	μA
		V_{DD} = STROBE = BLANK = 5.0 V, Data latched, Display "8"	—	7.0	mA
		V_{DD} = STROBE = BLANK = 15 V, Data latched, Display "8"	—	21	mA

5

UCN-4805A TRUTH TABLE

Inputs								Outputs							
D	C	B	A	dp	BL	ST	Character	a	b	c	d	e	f	g	dp
0	0	0	0	0	1	0	Zero	1	1	1	1	1	1	0	0
0	0	0	1	0	1	0	One	0	1	1	0	0	0	0	0
0	0	1	0	0	1	0	Two	1	1	0	1	1	0	1	0
0	0	1	1	0	1	0	Three	1	1	1	1	0	0	1	0
0	1	0	0	0	1	0	Four	0	1	1	0	0	1	1	0
0	1	0	1	0	1	0	Five	1	0	1	1	0	1	1	0
0	1	1	0	0	1	0	Six	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	Seven	1	1	1	0	0	0	0	0
1	0	0	0	0	1	0	Eight	1	1	1	1	1	1	1	0
1	0	0	1	0	1	0	Nine	1	1	1	0	0	1	1	0
1	0	1	0	0	1	0	A	1	1	1	0	1	1	1	0
1	0	1	1	0	1	0	b	0	0	1	1	1	1	1	0
1	1	0	0	0	1	0	C	1	0	0	1	1	1	0	0
1	1	0	1	0	1	0	d	0	1	1	1	1	0	1	0
1	1	1	0	0	1	0	E	1	0	0	1	1	1	1	0
1	1	1	1	0	1	0	F	1	0	0	0	1	1	1	0
X	X	X	X	1	1	0	dp	X	X	X	X	X	X	X	1
X	X	X	X	X	0	X	blank	0	0	0	0	0	0	0	0

X = irrelevant

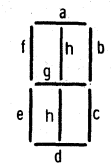


DWG. NO. A-10,985

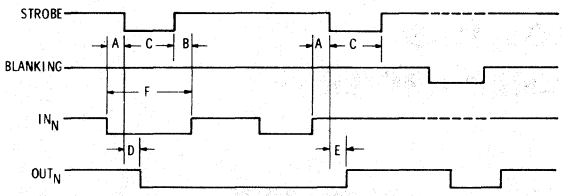
UCN-4806A TRUTH TABLE

Inputs								Outputs							
D	C	B	A	BL	ST	I/O	Character	a	b	c	d	e	f	g	h
0	0	0	0	1	0	1	Zero	1	1	1	1	1	1	0	0
0	0	0	1	1	0	1	One	0	0	0	0	0	0	0	1
0	0	1	0	1	0	1	Two	1	1	0	1	1	0	1	0
0	0	1	1	1	0	1	Three	1	1	1	1	0	0	1	0
0	1	0	0	1	0	1	Four	0	1	1	0	0	1	1	0
0	1	0	1	1	0	1	Five	1	0	1	1	0	1	1	0
0	1	1	0	1	0	1	Six	1	0	1	1	1	1	1	0
0	1	1	1	1	0	1	Seven	1	1	1	0	0	0	0	0
1	0	0	0	1	0	1	Eight	1	1	1	1	1	1	1	0
1	0	0	1	1	0	1	Nine	1	1	1	0	0	1	1	0
1	0	1	0	1	0	1	A	1	1	1	0	1	1	1	0
1	0	1	1	1	0	1	b	0	0	1	1	1	1	1	0
1	1	0	0	1	0	1	C	1	0	0	1	1	1	0	0
1	1	0	1	1	0	1	d	0	1	1	1	1	0	1	0
1	1	1	0	1	0	1	E	1	0	0	1	1	1	1	0
1	1	1	1	1	0	1	F	1	0	0	0	1	1	1	0
X	X	X	X	0	X	X	blank	0	0	0	0	0	0	0	0
X	X	X	X	X	1	0	interrogate latches	X	X	X	X	X	X	X	X

X = irrelevant



DWG. NO. A-10,986



Dwg. No. A-10,982

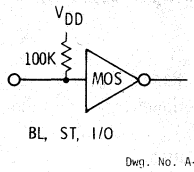
TIMING CONDITIONS

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) ..... 100 ns
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) ..... 100 ns
C. Minimum Strobe Pulse Width ..... 300 ns
D. Typical Time Between Strobe Activation and Output On to Off Transition ..... 1.0 μs
E. Typical Time Between Strobe Activation and Output Off to On Transition ..... 1.0 μs
F. Minimum Data Pulse Width ..... 300 ns

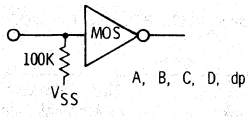
Information present at an input is transferred to its latch when the STROBE (ST) is low. The latches will continue to accept new data as long as the STROBE is held low. Applications where the latches are bypassed (STROBE tied low) ordinarily require that the BLANKING input be low between digit selection because of possible non-synchronous decoding.

When the BLANKING (BL) input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input high, the outputs are controlled by the latch/decoder circuitry.

With the I/O input control (UCN-4806A only) held high, the BCD data terminals function as inputs and allow information to be transferred to the latches. With the I/O input control held low, the BCD data terminals function as high-impedance latch outputs and allow the latches to be interrogated for error-checking purposes. While I/O is low, the STROBE line must be held high.

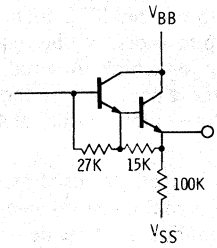


Dwg. No. A-10,979



Dwg. No. A-10,980

TYPICAL INPUT CIRCUITS



Dwg. No. A-10,981

TYPICAL OUTPUT DRIVER

5

UCN-4810A BiMOS 10-BIT SERIAL-INPUT, LATCHED DRIVER

FEATURES

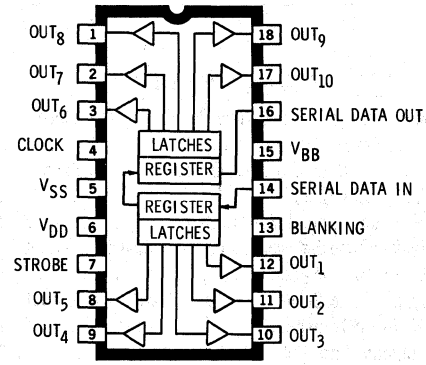
- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Logic & Latches
- Internal Pull-Down Resistors
- Wide Supply Voltage Range

COMBINING low-power CMOS logic with bipolar source drivers, the UCN-4810A BiMOS 10-bit serial-input, latched driver will simplify many display systems. Primarily designed for use with vacuum fluorescent displays, it can also be used with LED and incandescent displays within its output limitations of 60 V and 40 mA per driver.

The CMOS 10-bit shift register and associated latches are designed for operation over a supply voltage range of 5 V to 15 V. They also provide for minimum loading and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or low speed TTL logic the use of appropriate pull-up resistors may be required to insure a proper input logic high. A serial data output allows cascading these devices for interface requiring many drive lines (dot matrix, alphanumeric, bargraph, etc.).

The ten bipolar outputs are used as segment or digit drivers in vacuum fluorescent displays. Under normal operating conditions, these devices will sustain 25 mA per output at 50°C and a duty cycle of 85%. Other combinations of number of outputs conducting and duty cycle are shown in the specifications.

The UCN-4810A driver, combined with the UCN-4805A or UCN-4806A latched hexadecimal decoder/drivers or the UCN-4815A 8-bit latched source driver, comprises a minimum component display subsystem, requiring few, if any, discrete components.



Dwg. No. A-10,988

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature and V_{SS} = 0 V

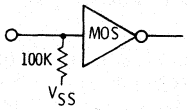
Output Voltage, V_{OUT} ..... 60 V
Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 18 V
Driver Supply Voltage Range, V_{BB} ..... 5.0 V to 60 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} ..... 40 mA
Package Power Dissipation, P_D ..... 1.82 W*
Operating Temperature Range, T_A ..... 0°C to +70°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*Derate at the rate of 18.18 mW/°C above T_A = 25°C.

Number of Outputs ON (I_{OUT} = 25 mA)	Max. Allowable Duty Cycle at Ambient Temperature of 25°C	40°C	50°C	60°C	70°C
10	100%	97%	85%	73%	62%
9	|	100%	94%	82%	69%
8	|	|	100%	92%	78%
7	|	|	|	100%	89%
6	|	|	|	|	100%
1	100%	100%	100%	100%	100%

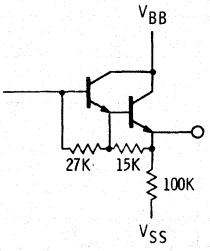
ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{BB} = 60 V, V_{DD} = 4.75 V to 15.75 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = 25 mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	−400	−850	μA
Output Leakage Current		T_A = 70°C	—	15	μA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 15 V	13.5	15.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = 5.0 V	—	100	μA
		V_{DD} = 15 V	—	300	μA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Output Resistance	R_{OUT}	V_{DD} = 5.0 V	—	20	kΩ
		V_{DD} = 15 V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON	—	13	mA
		All outputs OFF	—	1.3	mA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	μA
		V_{DD} = 15 V, All outputs OFF, All inputs = 0 V	—	200	μA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 15 V, One output ON, All inputs = 0 V	—	3.0	mA



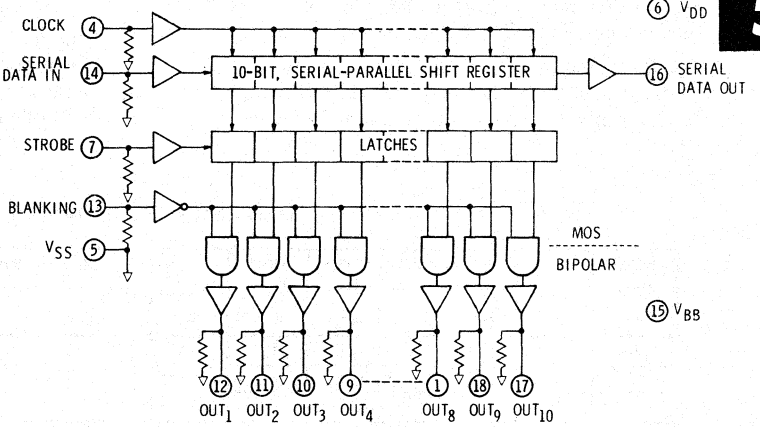
Dwg. No. A-10,980

TYPICAL INPUT CIRCUIT



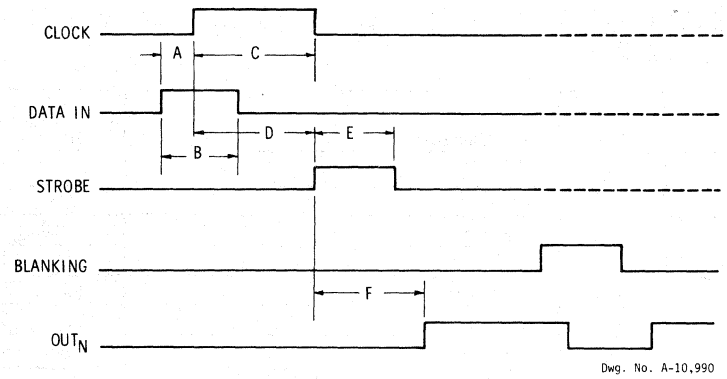
Dwg. No. A-10,981

TYPICAL OUTPUT DRIVER



Dwg. No. A-10,989

FUNCTIONAL BLOCK DIAGRAM



Dwg. No. A-10,990

TIMING CONDITIONS

		V_{DD} = 5.0 V	V_{DD} = 15 V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	250 ns	150 ns
B.	Minimum Data Pulse Width	500 ns	300 ns
C.	Minimum Clock Pulse Width	1.0 μs	250 ns
D.	Minimum Time Between Clock Activation and Strobe	1.0 μs	400 ns
E.	Minimum Strobe Pulse Width	500 ns	300 ns
F.	Typical Time Between Strobe Activation and Output Transition	1.0 μs	1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the BLANKING input low, the outputs are controlled by the state of the latches.

UCN-4810A TRUTH TABLES

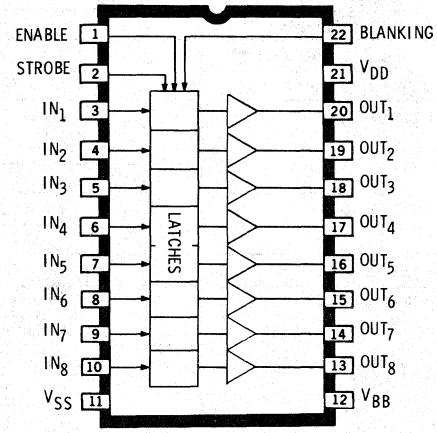
Serial Data Input	Clock Input	Shift Register Contents $I_1\ I_2\ I_3 \ldots I_8\ I_9\ I_{10}$	Serial Data Output	Strobe Input	Latch Contents $I_1\ I_2\ I_3 \ldots I_8\ I_9\ I_{10}$	Blanking Input	Output Contents $I_1\ I_2\ I_3 \ldots I_8\ I_9\ I_{10}$
H	⌐¬	H $R_1\ R_2 \ldots R_7\ R_8\ R_9$	R_9				
L	⌐¬	L $R_1\ R_2 \ldots R_7\ R_8\ R_9$	R_9				
X	¬⌐	$R_1\ R_2\ R_3 \ldots R_8\ R_9\ R_{10}$	R_{10}				
		X X X ..... X X X	X	L	$R_1\ R_2\ R_3 \ldots R_8\ R_9\ R_{10}$		
		$P_1\ P_2\ P_3 \ldots P_8\ P_9\ P_{10}$	P_{10}	H	$P_1\ P_2\ P_3 \ldots P_8\ P_9\ P_{10}$	L	$P_1\ P_2\ P_3 \ldots P_8\ P_9\ P_{10}$
					X X X ..... X X X	H	L L L ..... L L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCN-4815A BiMOS LATCH/SOURCE DRIVER

FEATURES

- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Internal Pull-Down Resistors
- Wide Supply Voltage Range



Dwg. No. A-10,987

DESIGNED primarily for use with high-voltage vacuum fluorescent displays, the UCN-4815A BiMOS latch/source driver consists of eight NPN Darlington source drivers with pull-down resistors, a CMOS latch for each driver, and common strobe, blanking, and enable functions.

The CMOS inputs provide for minimum loading and are compatible with standard CMOS, PMOS, and NMOS logic commonly found in microprocessor designs. The use of CMOS latches also allows operation over a supply voltage range of 5 V to 15 V. When employed with either standard TTL or low speed TTL logic, the UCN-4815A may require the use of appropriate pull up resistors.

The bipolar outputs may be used as segment, dot (matrix), bar, or digit drivers in vacuum fluorescent displays. All eight outputs can be activated simultaneously at ambient temperatures up to 60°C. To simplify circuit board layout, all outputs are pinned opposite their respective inputs.

A minimum component display subsystem, requiring few or no discrete components, may be realized by using the UCN-4815A BiMOS Latch/Source Driver with either a UCN-4805A or UCN-4806A latched hexadecimal decoder/drivers or a UCN-4810A serial-to-parallel latch/driver.

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature and V_{SS} = 0 V

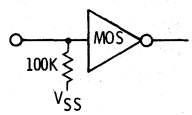
Output Voltage, V_{OUT} ..... 60 V
Logic Supply Voltage Range, V_{DD} ..... 4.5 V to 18 V
Driver Supply Voltage Range, V_{BB} ..... 5.0 V to 60 V
Input Voltage Range, V_{IN} ..... −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} ..... 40 mA
Package Power Dissipation, P_D ..... 2.0 W*
Operating Temperature Range, T_A ..... 0°C to +70°C
Storage Temperature Range, T_S ..... −55°C to +125°C

*Derate at the rate of 20 mW/°C above T_A = 25°C.

Number of Outputs ON (I_{OUT} = 25 mA)	Max. Allowable Duty Cycle at Ambient Temperature of 50°C	60°C	70°C
8	100%	100%	86%
7			98%
6			100%
1	100%	100%	100%

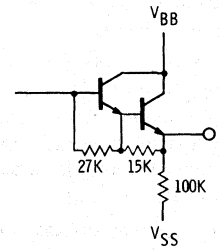
ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{BB} = 60 V, V_{DD} = 4.75 V to 15.75 V, V_{SS} = 0 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits		
			Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		I_{OUT} = 25 mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	V_{OUT} = V_{BB}	−400	−850	μA
Output Leakage Current		T_A = 70°C	—	15	μA
Input Voltage	$V_{IN(1)}$	V_{DD} = 5.0 V	3.5	5.3	V
		V_{DD} = 15 V	13.5	15.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	V_{DD} = 5.0 V	—	100	μA
		V_{DD} = 15 V	—	300	μA
Input Impedance	Z_{IN}	V_{DD} = 5.0 V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON	—	10.5	mA
		All outputs OFF	—	100	μA
	I_{DD}	V_{DD} = 5.0 V, All outputs OFF, All inputs = 0 V	—	100	μA
		V_{DD} = 15 V, All outputs OFF, All inputs = 0 V	—	200	μA
		V_{DD} = 5.0 V, One output ON, All inputs = 0 V	—	1.0	mA
		V_{DD} = 15 V, One output ON, All inputs = 0 V	—	3.0	mA



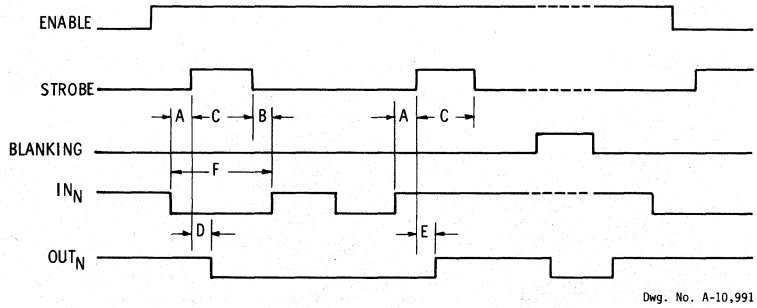
Dwg. No. A-10,980

TYPICAL INPUT CIRCUIT



Dwg. No. A-10,981

TYPICAL OUTPUT DRIVER



Dwg. No. A-10,991

TIMING CONDITIONS

A.	Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time)	100 ns
B.	Minimum Data Active Time After Strobe Disabled (Data Hold Time)	100 ns
C.	Typical Strobe Pulse Width For Power-Up Clear Disable	500 ns
	Minimum Strobe Pulse Width After Power-Up Clear Disabled	300 ns
D.	Typical Time Between Strobe Activation and Output On to Off Transition	1.0 μs
E.	Typical Time Between Strobe Activation and Output Off to On Transition	1.0 μs
F.	Minimum Data Pulse Width	300 ns

Information present at an input is transferred to its latch when the STROBE and ENABLE are high. The latches will continue to accept new data as long as both STROBE and ENABLE are held high. With either STROBE or ENABLE in the low state, no information can be loaded into the latches.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input low, the outputs are controlled by the state of the latches.

On first applying V_{DD} to the device, all latch outputs assume a low state (Power-Up Clear) resulting in all outputs being OFF. The latches will remain in the low condition until the Clear is disabled by a STROBE high input. Data may be entered into the latches during Power-Up Clear disable if the ENABLE input is also high.

UCN-4815A TRUTH TABLE

Inputs				OUT_N	
IN_N	STROBE	ENABLE	BLANK	T-1	T
0	1	1	0	X	0
1	1	1	0	X	1
X	X	X	1	X	0
X	0	X	0	1	1
X	0	X	0	0	0
X	X	0	0	1	1
X	X	0	0	0	0

X = irrelevant
T-1 = previous output state
T = present output state

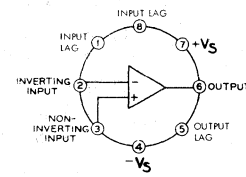
5

Device Type	Description
ULN/ULS-2139D/M	Op. Amp., Ext. Comp., 4.2 V/μs
ULN/ULS-2140A/H	Quad Current Switch
ULN/ULS-2151D/M	Op. Amp., Int. Comp., 0.6 V/μs
ULN/ULS-2171D/M	Op. Amp., Int. Comp., 1.5 V/μs
ULN-2300M	Amplifier/Detector/SCR
ULN-4136/4336A	Quad Op. Amp., 1.0 V/μs
ULN-4236/4436A	Quad Op. Amp., 0.6 V/μs

TYPE ULN-2139 and ULS-2139 HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIERS

FEATURES

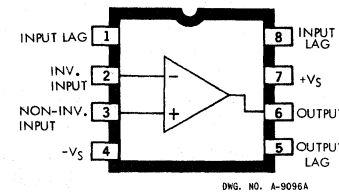
- Wide Operating Temperature Range, T_A:
  ULN-2139..... 0°C to +70°C
  ULS-2139.....−55°C to +125°C
- Fast Slew Rate: 4.2V/μs Typ. at Unity Gain
- Large Power Bandwidth: $20V_{P-P}$ at 20kHz Min.
- Low Offset Voltage: 1mV Typ.
- Low Offset Current: 20nA Typ.
- Input Overvoltage Protection
- Output Short-Circuit Protection



ULN-2139D
ULS-2139D

Description

SERIES 2139 Operational Amplifiers are monolithic integrated circuits designed as improved plug-in replacements for the MC-1439 and MC-1539. Features include large power-bandwidth, fast slew rate, low input offset voltage, and operation over wide temperature ranges. External compensation allows adjustment of frequency response and slew rate for specific applications. Unity gain compensation is accomplished with a 2200pF capacitor and a 390Ω resistor connected in series between pins 1 and 8.



ULN-2139M
ULS-2139M

Applications

Designed for general-purpose use, Series 2139 Operational Amplifiers are ideally suited for signal processing applications, voltage followers, summing amplifiers, amplifiers requiring specialized or general-purpose feedback networks, and applications where selective frequency response and fast slew rates are a requirement.

Packages

Package	Operating Temperature Range	
	0°C to +70°C	−55°C to +125°C
	Part Number	
TO-99	ULN-2139D	ULS-2139D
8-Lead DIP	ULN-2139M	ULS-2139M

ELECTRICAL CHARACTERISTICS @ $T_A = 25°C$, $V_S = \pm 15V$

(Compensation, 390Ω in series with 2200pF between pins 1 and 8)

Characteristic	Conditions	ULS-2139 Min.	ULS-2139 Typ.	ULS-2139 Max.	ULN-2139 Min.	ULN-2139 Typ.	ULN-2139 Max..	Units
Input Offset Voltage	$R_S \leq 10K\Omega$		±1	±3		±2	±7.5	mV
Input Offset Current			±20	±60		±20	±100	nA
Input Bias Current			150	500		250	1000	nA
Input Resistance		150	300		100	300		kΩ
Common Mode Input Voltage		±11	±12		±11	±12		V_P
Open Loop Voltage Gain	$V_O = \pm 10V$ ULS $R_L \geq 1K\Omega$, ULN $R_L \geq 2K\Omega$	94	106		86	100		dB
Output Voltage Swing	ULS $R_L = 1K\Omega$, ULN $R_L = 2K\Omega$	±10	±13		±10	±13		V_P
Power Dissipation	$V_O = 0V$		120	150		120	200	mW
Input Noise (equiv.)	$R_S = 10K\Omega$, f = 1kHz		20			20		nV/(Hz)½
Common Mode Rejection Ratio		80	100		80	100		dB
Power Supply Rejection Ratio		75	90		75	90		dB
Slew Rate	$V_O = \pm 10V$, ULS $R_L = 1K\Omega$, ULN $R_L = 2K\Omega$	1.0	4.2		0.8	4.2		V/μs
Power Bandwidth	$V_O = \pm 10V$, ULS $R_L = 1K\Omega$, ULN $R_L = 2K\Omega$	20	50		10	50		kHz
Output Resistance			2			2		kΩ
Unity Gain Bandwidth			1			1		MHz

GUARANTEED ELECTRICAL CHARACTERISTICS OVER TEMPERATURE @ $V_S = \pm 15V$

		ULS-2139		ULN-2139		Units
Operating Temperature Range		−55	125	0	+70	°C
Characteristic	Conditions	Min.	Max.	Min.	Max.	
Input Offset Voltage	$Rs \leq 10K\Omega$		±4.5		±9	mV
Input Offset Current			±80		±115	nA
Input Bias Current			800		1200	nA
Open Loop Voltage Gain	$V_O = \pm 10V$ ULS $R_L \geq 1K\Omega$, ULN $R_L \geq 2K\Omega$	86		82		dB

6

ABSOLUTE MAXIMUM RATINGS

Power Supply, $+V_S$ ..... +18V
$-V_S$ ..... −18V
Differential Input Voltage ..... $\pm V_S$
Common Mode Input Swing ..... $\pm V_S$
Load Current 15mA
Output Short Circuit Duration ..... Continuous
Storage Temperature Range, T_S ..... −65°C to +150°C

NOTES:
1. For V_S less than ±15V, the absolute maximum rating is equal to V_S.

SERIES 2140
HIGH PERFORMANCE
QUAD CURRENT SWITCHES

FEATURES

- Variable Reference: −3 to −10 Volts
- Low Temperature Coefficient: 5 ppm/°C
- Fast Settling: 300 ns to 0.01%
- TTL/CMOS Compatible Inputs

Description

SERIES 2140 quad current switches are high precision monolithic integrated circuits for use in digital-to-analog converters. Each device contains four logic-controlled current switches and a reference transistor. Continuously running current sources and superior thermal layout, maximize speed and accuracy by reducing transitional anomalies. Series 2140 switches accept a wide range of d-c references or an a-c reference for two-quadrant mutiplying D/A applications. Inputs may be driven from TTL, or similar sources and are independent of reference voltage level.

The ULN-2140A switches are rated for operation over the temperature range of −0°C to +70°C, the 'A' suffix indicating a 14-pin dual in-line plastic package. The ULS-2140H switches are rated for operation over the extended temperature range of −55°C to +125°C with the 'H' suffix indicating a dual in-line hermetic package to Military Specification MIL-M-38510. Devices in unpackaged, chip form, for use in hybrid circuit applications, are designated by changing the suffix letter from A or H to C.

On special order, hermetically-sealed quad current switches with high-reliability screening to MIL-STD-883 are available by adding the suffix 'MIL' to the part number, for example, ULS-2140H-MIL. Also, on special order, devices with improved linearity and drift can be supplied.

ABSOLUTE MAXIMUM RATINGS

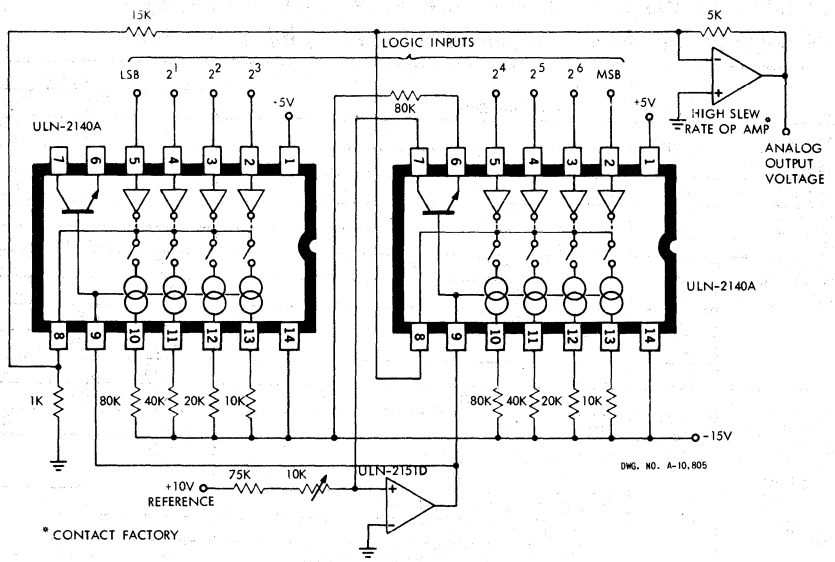
Supply Voltage, V_{CC}	+18 V
V_{EE}	−18 V
Input Voltage, V_{IN}	+6 V
Reference Voltage Range, V_{REF}	−3 V to V_{EE}
Operating Temperature Range, T_A (ULN-2140A)	−0°C to +70°C
(ULS-2140H)	−55°C to +125°C
Storage Temperature Range, T_S	−65°C to +150°C

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = +5$ to $+15$ V, $V_{EE} = -15$ V, $I_{MSB} = 1$ mA, Operational Amplifier Summing Junction Load (unless otherwise noted)

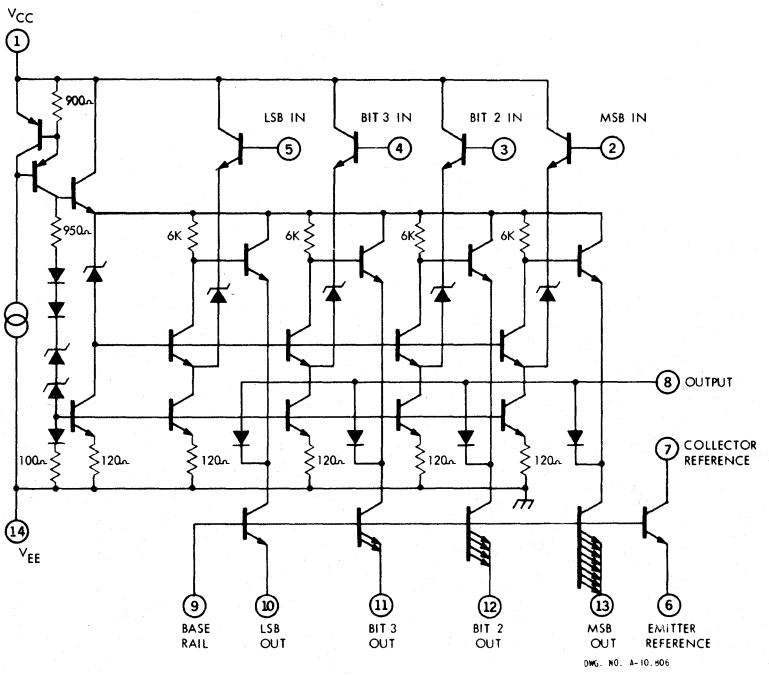
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
"0" Input Voltage	$V_{IN(0)}$		—	—	0.8	V
"1" Input Voltage	$V_{IN(1)}$		2.0	—	—	V
"0" Input Current	$I_{IN(0)}$	$V_{IN} = 0.8$ V	—	—	−1.0	μA
"1" Input Current	$I_{IN(1)}$	$V_{IN} = 2.4$ V	—	—	10	μA
Output Voltage	V_{OUT}	$R_L = 1$ kΩ		See Note		
Output Voltage Swing	ΔV_{OUT}	$R_L = 1$ kΩ, Logic = 0000 to 1111	−2.0	—	—	V
Output Current	I_{MSB}	Logic = 1000	2.0	1.0	—	mA
	$I_{BIT\ 2}$	Logic = 0100	1.0	0.5	—	mA
	$I_{BIT\ 3}$	Logic = 0010	0.5	0.25	—	mA
	I_{LSB}	Logic = 0001	0.25	0.125	—	mA
Settling Time		$R_L = 1$ kΩ, To 0.01%, Logic = 1000 to 0111	—	300	—	ns
Output Leakage Current	I_{OUT}	Logic = 0000	—	—	10	μA
Ref. Transistor Static Forward Current Gain	h_{FE}	$I_C = 125$ μA	100	—	—	—
Non-Linearity		Over Operating Temperature Range	—	—	0.5	%
TC of Non-Linearity		−0°C to +70°C (ULN-2140 Devices)	—	—	20	ppm/°C
		−55°C to +125°C (ULS-2140 Devices)	—	—	10	ppm/°C
Scale Factor Drift		Over Operating Temperature Range	—	5.0	—	ppm/°C
Supply Current	I_{CC}	$V_{CC} = +15$ V	—	8.0	—	mA
	I_{EE}		—	−8.0	—	mA

Note: Output voltage with a resistive load will be a negative voltage.

6



TYPICAL APPLICATION

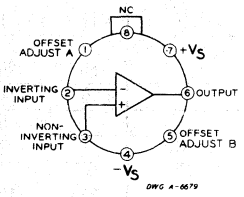


SCHEMATIC

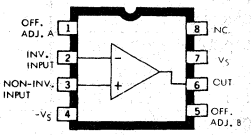
TYPE ULN-2151 and ULS-2151 HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIERS

FEATURES

- Wide Operating Temperature Range, T_A:
  ULN-2151.....0°C to +70°C
  ULS-2151.....−55°C to +125°C
- Input Offset Current: 2nA Typ.
- Input Bias Current: 35nA Typ.
- Input Offset Voltage: ±0.7mV Typ.
- Open Loop Voltage Gain: 250 V/mV Typ.
- Input Resistance: 3 MΩ Typ.
- Offset Null Capability
- Output Short-Circuit Protection
- Input Overvoltage Protection



ULN-2151D
ULS-2151D



ULN-2151M
ULS-2151M

Description

SERIES 2151 Operation Amplifiers are monolithic integrated circuits designed for high performance and ease of application. They feature high common mode input voltage range, low input offset and bias currents, low input offset voltage, input and output protection, offset voltage null capability, and high open loop voltage gain. The 2151 Series is a direct plug-in replacement for the μA741 and with improved electrical performance over a wider temperature range.

Applications

Designed for general-purpose use, Series 2151 Operational Amplifiers are ideally suited for signal processing applications, voltage followers, summing amplifiers, integrators, and amplifiers requiring specialized or general feedback networks.

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Packages

Package	Operating Temperature Range	
	0°C to +70°C	−55°C to +125°C
	Part Number	
TO-99	ULN-2151D	ULS-2151D
8-Lead DIP	ULN-2151M	ULS-2151M

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, $\pm V_S$: ULS-2151.....±22V
ULN-2151.....±20V
Differential Input Voltage.....±30V
Input Voltage (See Note 1), V_{CMI}.....±15V
Output Short Circuit Duration.....Continuous
Storage Temperature Range, T_S.....−65°C to +150°C

NOTES:
1. For V_S less than ±15V, the absolute maximum rating is equal to V_S.

ELECTRICAL CHARACTERISTICS @ T_A = 25°C V_s = ± 15V

Characteristic	Conditions	ULS-2151 Min.	ULS-2151 Typ.	ULS-2151 Max.	ULN-2151 Min.	ULN-2151 Typ.	ULN-2151 Max.	Units
Input Offset Voltage	$R_S \leq 50K\Omega$		±0.7	±2		±1	±5	mV
Input Offset Current			±2	±5		±5	±25	nA
Input Bias Current			35	50		70	250	nA
Input Resistance		1.5	3		0.4	1.5		MΩ
Common Mode Input Voltage		±12	±13		±11	±13		Vp
Open Loop Voltage Gain	$V_O = \pm 10V$ $R_L \geq 2K\Omega$	50	250		25	150		V/mV
Output Voltage Swing	$R_L = 2K\Omega$	±10	±13		±10	±13		Vp
Power Dissipation	$V_O = 0V$		51	85		51	85	mW
Input Noise (equiv.)	$R_S = 10K\Omega$, f = 1kHz		25	35		30	45	nV/(Hz)½
Common Mode Rejection Ratio		85	100		75	90		dB
Power Supply Rejection Ratio		85	100		75	95		dB
Slew Rate	$V_O = \pm 10V$, $R_L = 2K\Omega$	0.5	0.6		0.4	0.6		V/μs
Full Power Bandwidth	$V_O = \pm 10V$, $R_L = 2K\Omega$	8			6			kHz
Output Resistance			75			75		ohms

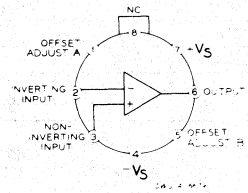
GUARANTEED ELECTRICAL CHARACTERISTICS OVER TEMPERATURE@ V_s = ±15V

		ULS-2151		ULN-2151		Units
Operating Temperature Range		−55	+125	0	+70	°C
Characteristic	Conditions	Min.	Max.	Min.	Max.	
Input Offset Voltage	$R_S \leq 10K\Omega$		±5		±6.5	mV
Input Offset Current			±15		±50	nA
Input Bias Current			75		350	nA
Open Loop Voltage Gain	$V_O = \pm 10V$ $R_L \geq 2K\Omega$	25		12.5		V/mV

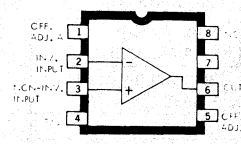
TYPE ULN-2171 and ULS-2171 HIGH PERFORMANCE MONOLITHIC OPERATIONAL AMPLIFIERS

FEATURES

- Wide Operating Temperature Range, T_A:
  ULN-2171..... **0°C to +70°C**
  ULS-2171.....−55°C to +125°C
- High Common Mode Input Impedance: 5000MΩ | 3pF Typ.
- High Input Impedance: 8MΩ | 3pF
- Slew Rate at Unity Gain: 1.5V/μs Typ.
- Input Offset Voltage: 0.7mV Typ.
- Input Offset Current: 4nA Typ.
- Input Bias Current: 8nA Typ.
- Offset Null Capability
- Output Short-Circuit Protection
- Operates from ±3V to ±22V Power Supplies
- Input Overvoltage Protection



ULN-2171D
ULS-2171D



ULN-2171M
ULS-2171M

Description

SERIES 2171 Operational Amplifiers are monolithic integrated circuits designed for high performance and stability. They employ a unique input current cancellation network which achieves high input impedance and low input current while maintaining fast slew rate. Features include high slew rate, high common mode impedance, low input offset and bias currents, low offset voltage, input and output protection, and input offset voltage null capability. In addition, no external components are required for frequency compensation.

Applications

Designed for general-purpose use, Series 2171 Operational Amplifiers are ideally suited for signal processing applications, voltage followers, integrators, and amplifiers requiring specialized or general-purpose feedback networks.

6

Packages

Package	Operating Temperature Range	
	0°C to +70°C	−55°C to +125°C
	PART NUMBER	
TO-99	ULN-2171D	ULS-2171D
8-Lead DIP	ULN-2171M	ULS-2171M

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, $\pm V_S$: ULS-2171.....±22V
ULN-2171.....±20V
Differential Input Voltage.....±30V
Input Voltage (See Note 1), V_{CMI}..... ±15V
Output Short Circuit Duration.....Continuous
Storage Temperature Range, T_S.....−65°C to +150°C

NOTES:
1. For V_S less than ±15V, the absolute maximum rating is equal to V_S.

ELECTRICAL CHARACTERISTICS @ T_A = 25°C, V_S = ±15V

Characteristic	Conditions	ULS-2171			ULN-2171			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	R_S = ≤ 10KΩ		±0.7	±2.0		±0.7	±5.0	mV
Input Offset Current			±4	±7		±8	±20	nA
Input Bias Current			8	15		30	50	nA
Input Resistance		8	13		2	5		MΩ
Common Mode Input Voltage		±12	±13		±12	±13		V_P
Open Loop Voltage Gain	V_O = ±10V, R_L ≥ 2KΩ	50	150		25	100		V/mV
Output Voltage Swing	R_L = 2KΩ	±10	±13		±10	±13		V_P
Power Dissipation	V_O = 0V		55	90		55	95	mW
Input Noise (equiv.)	R_S = 10KΩ, f = 1kHz		35			35		nV/(Hz)½
Common Mode Rejection Ratio		85	105		80	100		dB
Power Supply Rejection Ratio		85	105		80	100		dB
Slew Rate	V_O = ±10V, R_L = 2KΩ	1.0	1.5		0.8	1.5		V/μs
Power Bandwidth	V_O = ±10V, R_L = 2KΩ	15			10			kHz
Output Resistance			100			100		ohms

GUARANTEED ELECTRICAL CHARACTERISTICS OVER TEMPERATURE @ V_S = ±15V

		ULS-2171		ULN-2171		Units
Operating Temperature Range		−55	+125	0	+70	°C
Characteristic	Conditions	Min.	Max.	Min.	Max.	
Input Offset Voltage	R_S ≤ 10KΩ		±5		±6.5	mV
Input Offset Current			±17		±30	nA
Input Bias Current			40		75	nA
Open Loop Voltage Gain	V_O = ±10V, R_L = 2KΩ	25		12.5		V/mV

TYPE ULN-2300M UNICIRCUIT®
AMPLIFIER-SCR FIRING CIRCUIT

THE ULN-2300M combines a linear differential amplifier, a half-wave complementary detector, and a silicon-controlled rectifier on a single silicon die. This monolithic device is used for sensing small voltages and supplying large currents of up to 300 mA.

This amplifier-SCR firing circuit includes an internal zener diode voltage regulator which maintains the circuit supply at + 12 volts. This amplifier has a high input impedance and an internal bias network. The SCR trigger level is independent of temperature variations because the amplifier gain is matched to the SCR firing voltage over the operating temperature range.

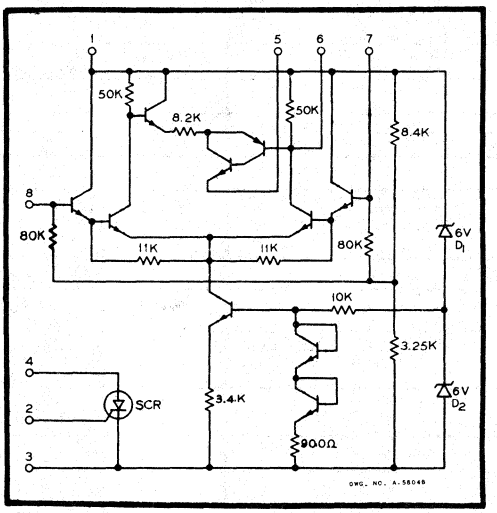
The ULN-2300M amplifier can be driven either single-ended or differentially. Its sensitivity can be adjusted by external a-c feedback from pin 6 to pin 7, or by the proper choice of gate resistor between pins 2 and 3 (R_{GK}). Frequency dependence of the trigger level is determined by the choice of appropriate passive networks.

The ULN-2300M features:

- **Input impedance: 80KΩ**
- **Trigger level: 12 mV (rms)**
- **Gain: 35 dB**
- **Frequency response: 150 kHz**
- **SCR pulse current (10 μs duration): 3 A**

This device, with the deletion of the SCR, was also available as the ULN-2301M. In all other respects they were identical.

The ULN-2300M amplifier SCR Firing Circuit is supplied in the space-saving 8-pin dual in-line 'M' plastic molded package.



PIN CONNECTIONS

Pin 1: I_{CC}
Pin 2: SCR gate
Pin 3: SCR cathode and ground
Pin 4: SCR anode
Pin 5: Detector output (control pin for SCR gate)
Pin 6: Amplifier output
Pin 7: Inverting input
Pin 8: Non-inverting input

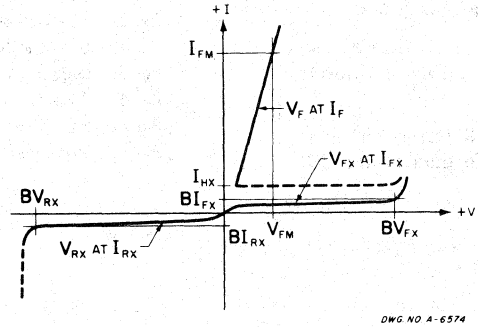
6

ELECTRICAL CHARACTERISTICS

at I_{CC} = 5mA (over operating temperature range unless otherwise specified)

Characteristics	Symbol	Test Conditions	Limits				Note	Figure (Note 4)
			Min.	Typ.	Max.	Units		
AMPLIFIER-DETECTOR (Note 1)								
Open Loop Voltage Gain (V_{OUT} at Pin 6)	A_V	V_8 = 10 mV rms, f = 1kHz	30	35		dB		1
Upper Frequency Response (V_{OUT} at Pin 6)	f_C	V_8 = 10 mV rms, T_A = 25 C	75	150		kHz		6
Input Impedance (Single Ended)	Z_{IN}	V_{IN} at Pin 8, f = 1kHz, T_A = 25 C	60	80		KΩ		3
Maximum Output Voltage Swing (V_{OUT} at Pin 6)	V_6	Open Loop, f = 1kHz		3.3		Vrms		
Detector Output Voltage (V_{OUT} at Pin 5)	V_5	R_L = 2kΩ (pin 5 to 3), V_8 = 20 mV rms, f = 1kHz, T_A = 25 C	0.3	0.8	1.3	V peak		7, 8
Output Impedance (V_{OUT} at Pin 6)	Z_{OUT}			50		KΩ		
Common Mode Rejection Ratio	C_{MRR}	V_{IN} = 1V p-p, f = 1kHz		80		dB		
Regulated Zener Voltage	V_1		10.5	12	13	VDC		
AMPLIFIER-SCR CIRCUIT								
Trigger Level (Open Loop)	V_T	V_{IN} at Pin 8 (pin 5 to 2) R_{GK} = 2KΩ, f = 1kHz T_A = 25 C		12		mV rms	1	9, 10
SILICON-CONTROLLED RECTIFIER (Note 2)								
Anode Reverse Blocking Current	I_{RXM}	V_{KA} = 50V, R_{GK} = ∞ T_A = +70 C			10	μA		
Anode Forward Blocking Current	I_{FXM}	V_{AA} = 50V, T_A = +70 C			10	μA		
Gate Trigger Voltage	$V_{GT(ON)}$	V_{AA} = 50V, R_L = 500Ω T_A = 0°C		0.5	0.8	Volts		12
Gate Trigger Current	I_{GT}	V_{AA} = 50V, R_L = 500Ω T_A = 0°C		30		μA		
Holding Current	I_{HX}	T_A = 0°C R_{GK} = 2KΩ	0.6	2.4	6.0	mA		14
Forward Voltage	V_F	I_F = 150 mA, T_A = +70 C		1.1	1.5	Volts	3	13

NOTES:
1. Inverting input (pin 7) returned to ground with a 0.1μF ceramic capacitor.
2. Unless otherwise noted, a 2KΩ resistor (R_{GK}) is connected between gate (pin 2) and cathode (pin 3) to prevent triggering by random noise.
3. Measured using pulse techniques, tp = 1mS, duty cycle ≤ 1%.
4. See applicable typical characteristic curve for further information.



SCR ANODE CHARACTERISTICS WITH GATE CONNECTED TO CATHODE THROUGH R_{GK}

ABSOLUTE MAXIMUM RATINGS

(over operating free-air temperature)

LINEAR DIFFERENTIAL AMPLIFIER

Supply Current, I_{CC} 10mA

SILICON-CONTROLLED RECTIFIER

Continuous Reverse Blocking Voltage, V_{ROM} 50V

Continuous Forward Blocking Voltage[2], V_{FXM} 50V

Continuous Anode Forward Current, $I_{FM\ (AV)}$ 300mA
(at or below 25 C free-air temperature)[3]

Peak Anode Current (10 μS duration)[4], $I_{FM\ (PULSE)}$ 3A

Average Forward Gate Power, $P_{GF\ (AV)}$ 0.01W

Peak Forward Gate Current[5], I_{GFM} 0.1A

Peak Reverse Gate Voltage, V_{GRM} 5V

AMPLIFIER-SCR CIRCUIT

Operating free-air temperature, T_A . . 0 C to +70 C

Storage Temperature, T_{STG} . . . . . −55 C to +125 C

Internal Power Dissipation, P_D 250mW

NOTES:

1. Maximum ratings are limiting values above which the serviceability may be impaired from the viewpoint of life or satisfactory performance. The forward or reverse blocking capabilities of the SCR should not be tested with a constant current source such that the voltage applied exceeds the maximum rated voltage.
2. Values apply when the gate-to-cathode resistance, R_{GK}, ≤ 16KΩ.
3. SCR maximum rated anode current, $I_{FM\ (AV)}$, applies for continuous d-c operation with resistive load. For operation above 25 C free-air temperature, refer to Anode Forward Current derating curve, Figure 11.
4. Peak surge current should not be repeated until thermal equilibrium is restored.
5. SCR peak forward gate current maximum rating at PW ≤ 300μS, f = 120pps.

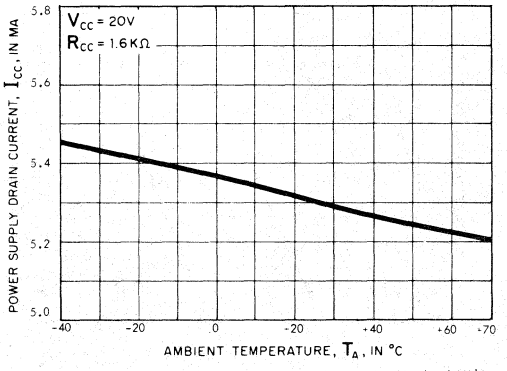


Figure 2
QUIESCENT POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF AMBIENT OPERATING TEMPERATURE

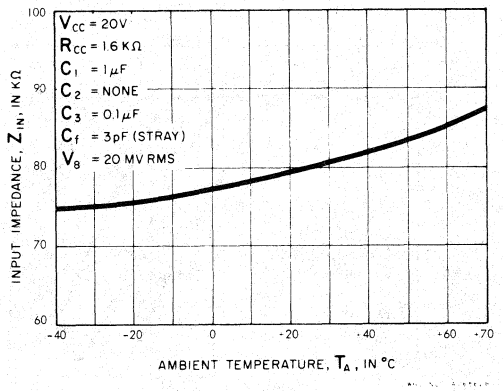


Figure 3
INPUT IMPEDANCE AS A FUNCTION OF AMBIENT OPERATING TEMPERATURE

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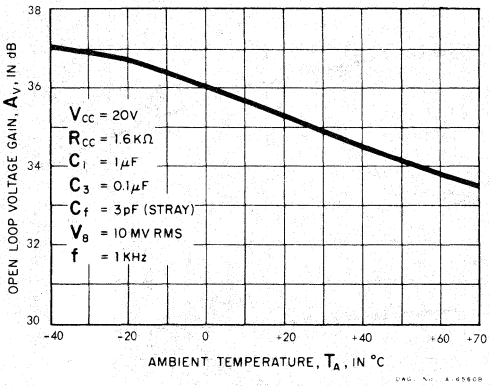


Figure 1
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT OPERATING TEMPERATURE

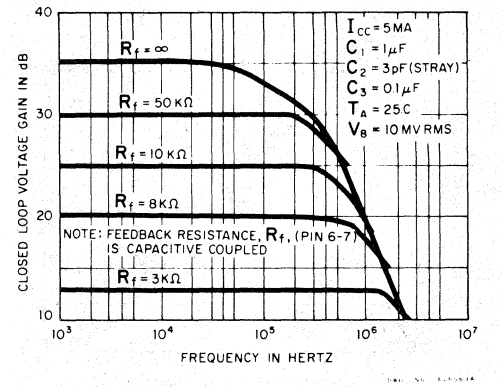


Figure 4
CLOSED LOOP VOLTAGE GAIN AS A FUNCTION OF OPERATING FREQUENCY

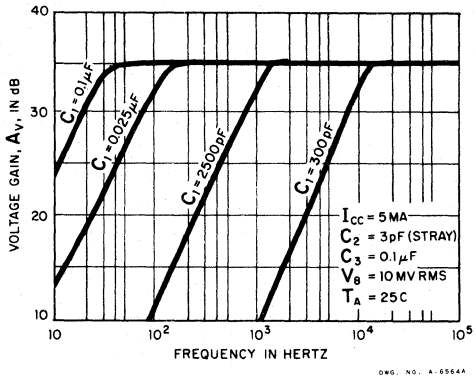


Figure 5
VOLTAGE GAIN FOR VARIOUS INPUT COUPLING CAPACITORS AS A FUNCTION OF FREQUENCY

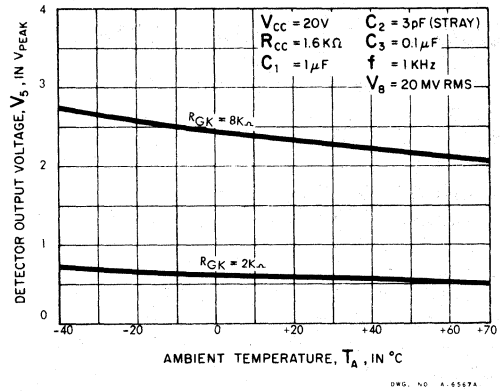


Figure 8
DETECTOR OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT OPERATING TEMPERATURE

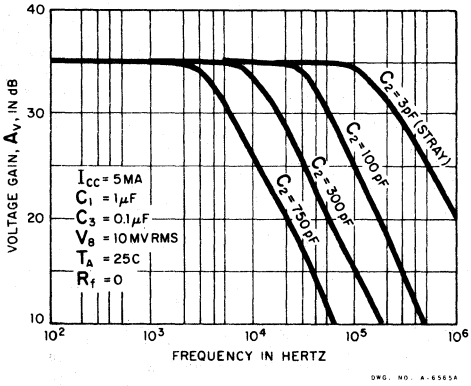


Figure 6
VOLTAGE GAIN FOR VARIOUS FEEDBACK CAPACITORS AS A FUNCTION OF FREQUENCY

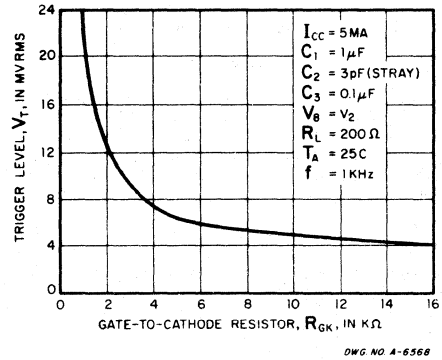


Figure 9
SCR TRIGGER LEVEL AS A FUNCTION OF GATE-TO-CATHODE RESISTANCE (R_{GK})

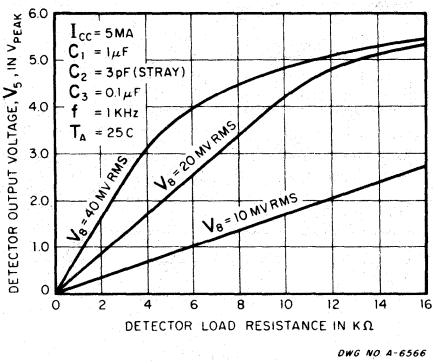


Figure 7
DETECTOR OUTPUT VOLTAGE AS A FUNCTION OF DETECTOR LOAD RESISTANCE

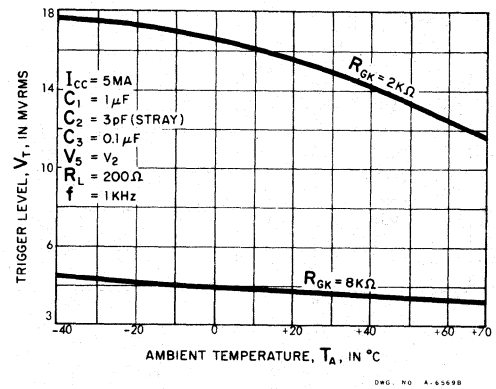


Figure 10
SCR TRIGGER LEVEL AS A FUNCTION OF AMBIENT OPERATING TEMPERATURE

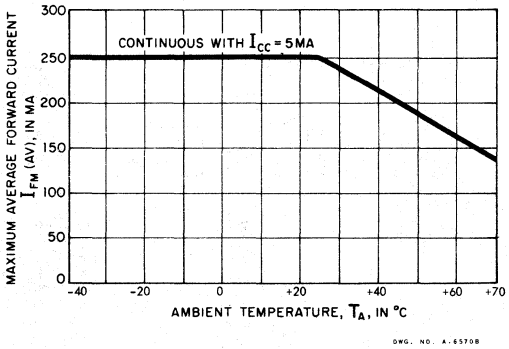


Figure 11
SCR ANODE FORWARD CURRENT DERATING CURVE

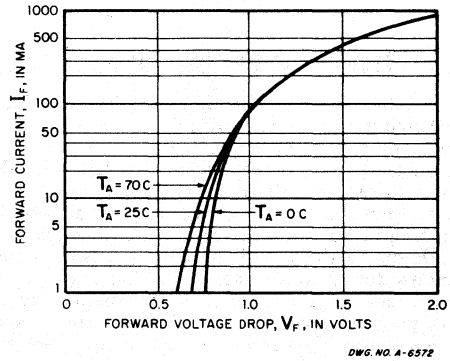


Figure 13
FORWARD VOLTAGE DROP AS A FUNCTION OF ANODE FORWARD CURRENT

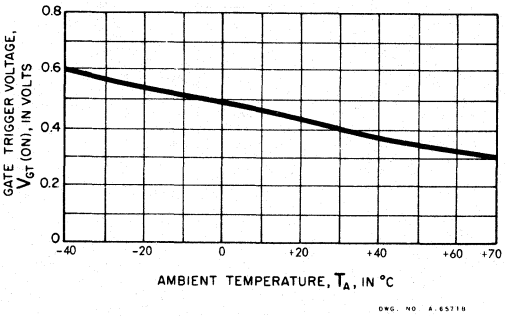


Figure 12
SCR GATE TRIGGER VOLTAGE AS A FUNCTION OF AMBIENT OPERATING TEMPERATURE

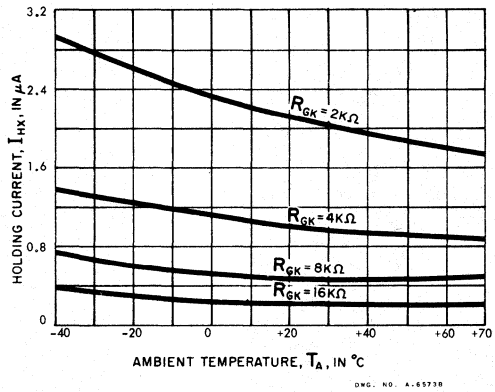


Figure 14
SCR HOLDING CURRENT AS A FUNCTION OF AMBIENT OPERATING TEMPERATURE

6

AMPLIFIER-DETECTOR OPERATION

The block diagram of the ULN-2300M Amplifier-SCR Firing Circuit is shown in Figure 15. The input and output waveforms are shown in Figure 16. Capacitors C_1 and C_3 are required because of the d-c voltages present at the input terminals.

The low-frequency response may be shaped by choosing an appropriate input coupling capacitor, C_1. Figure 5 shows voltage gain versus frequency response for various values of this capacitor. The high-frequency response may be shaped by an appropriate feedback capacitor, C_2. Figure 6 shows the effect that C_2 has on voltage gain versus frequency. For maximum sensitivity and frequency response, the unused input should be returned to ground with a 0.1 μF ceramic capacitor, C_3.

The system gain (trigger level) may be adjusted by varying the gate-to-cathode resistor, R_{GK} or by a-c feedback from pin 6 to pin 7 as shown in Figure 7. The output of the detector at pin 5 may be coupled directly into the gate of the SCR or may be filtered with an appropriate network to provide d-c to the gate of the SCR.

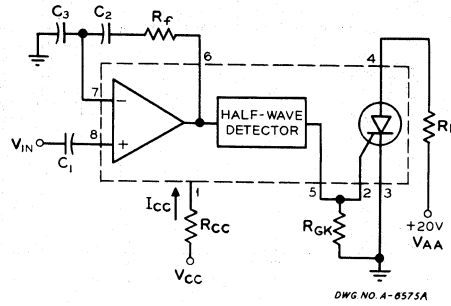


Figure 15

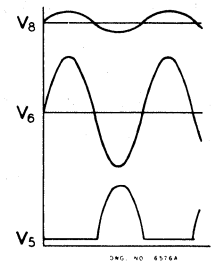
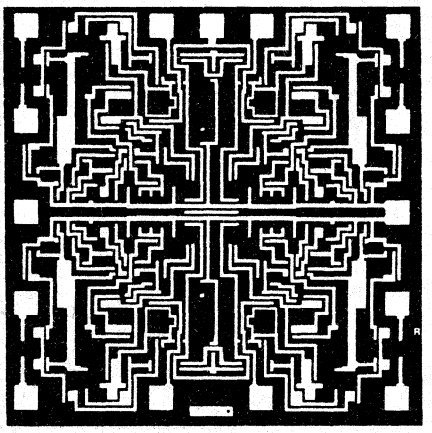


Figure 16

SERIES ULN-4036A
HIGH PERFORMANCE MONOLITHIC QUAD OPERATIONAL AMPLIFIERS

FEATURES

- Internal Frequency Compensation
- Output Short Circuit Protection
- Low Power Consumption
- Channel Separation: 120 dB Typ.
- Input Resistance: 2 MΩ Typ.
- Open Loop Voltage Gain: 300 V/mV Typ.
- High CMRR: 90 dB Typ.

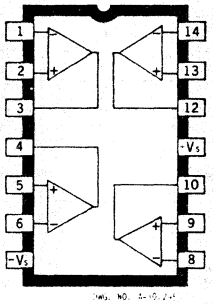


CONSISTING of four independent, internally compensated, high gain, operational amplifiers on a single silicon chip, the Series ULN-4036A devices are intended for use in active filters, multi-channel amplifiers, and similar applications.

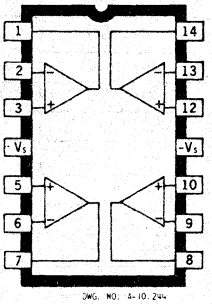
The Type ULN-4136A device will meet or exceed all specifications for industry standard μA741 amplifiers. It provides the highest possible packaging density and the monolithic construction allows very close thermal tracking. The Type ULN-4236A device is a low-power, pin-compatible version of the ULN-4136A.

The Type ULN-4336A quad operational amplifier is electrically identical to the Type ULN-4136A but is pin compatible with the LM124, LM148, and MC3403 series devices and can directly replace them in many applications. The Type ULN-4436A is the low-power, pin-compatible version of the ULN-4336A.

The Series ULN-4036A quad high-performance monolithic operational amplifiers are supplied in 14-lead dual in-line packages conforming to JEDEC outline TO-116 (MO-001AA) and are rated for continuous operation over the temperature range of 0°C to +70°C.



ULN-4136A
ULN-4236A



ULN-4336A
ULN-4436A

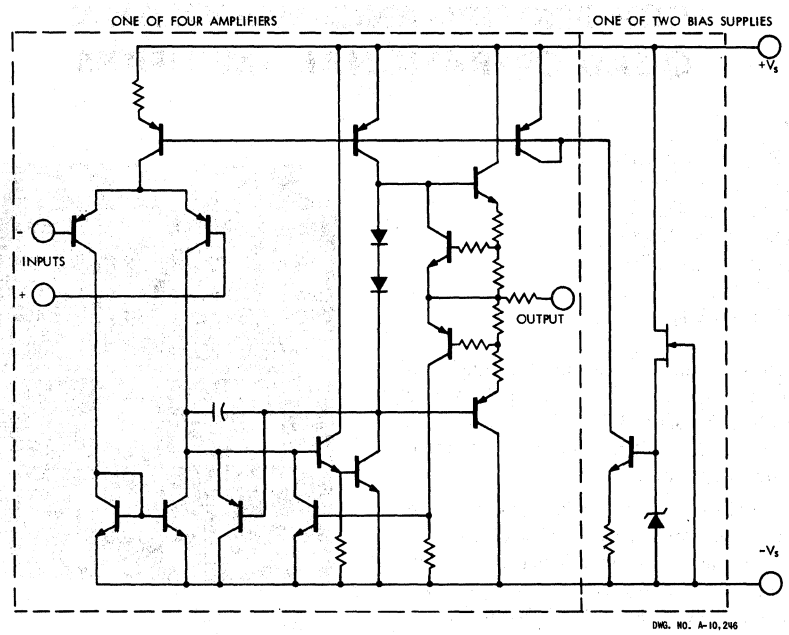
ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature

Supply Voltage, $\pm V_S$	±18 V
Common Mode Voltage Range	$\pm V_S$
Differential Input Voltage	±30 V
Output Short Circuit Duration	Continuous
Total Power Dissipation, P_D	625 mW*
Operating Temperature Range, T_A	0°C to +70°C
Storage Temperature Range, T_S	−65°C to +150°C

*Derate at the rate of 5 mW/°C above T_A = 25°C.

6

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_S = \pm 15\,V$, $R_L = 2\,k\Omega$, $R_S = 10\,k\Omega$ (unless otherwise specified)

Characteristic	Test Conditions	Limits						Units
		ULN-4136A & ULN-4336A			ULN-4236A & ULN-4436A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage		—	1.0	5.0	—	1.0	5.0	mV
Input Offset Current		—	30	50	—	20	50	nA
Input Bias Current		—	50	300	—	30	200	nA
Input Resistance		0.3	2.0	—	0.3	2.0	—	MΩ
Large Signal Voltage Gain	$V_{out} = \pm 10\,V$	25	300	—	25	300	—	V/mV
Output Voltage Swing	$R_L = 2\,k\Omega$	±10	±13	—	±10	±13	—	V
	$R_L = 10\,k\Omega$	±12	±14	—	±12	±14	—	V
Input Voltage Range		±13	±14	—	±13	±14	—	V
Common Mode Rejection Ratio		80	90	—	80	90	—	dB
Supply Voltage Rejection Ratio		30	150	—	30	150	—	μV/V
Total Power Dissipation		—	210	330	—	60	120	mW
Unity Gain Bandwidth		—	3.0	—	—	1.5	—	MHz
Slew Rate	$A_V = 1$	—	1.0	—	—	0.6	—	V/μs
Channel Separation	$f = 20\,kHz$, $R_S = 1\,k\Omega$	—	120	—	—	120	—	dB

CUSTOM CIRCUIT DESIGNS

Sprague is active in the design of both standard and custom high-volume integrated circuits and subassemblies for both linear and digital applications. A wide range of semiconductor technologies is available to optimize cost/performance. Often, new processes or innovative circuit designs are required.

The first concern of a custom device is generally one of cost, though performance, reliability, size, and process are also important considerations.

Production Volume: unit cost is very dependent on quantity such that volumes of 250,000 pieces per year are required after the initial design and development.

Chip size: unit cost is directly affected by chip size which is related to circuit complexity, output current, and output voltage ratings.

Test Requirements: digital, d-c, and static measurements are simple, fast, and inexpensive to perform while linear measurements such as distortion, phase, noise, etc. affect throughput and increase cost.

Specifications: well-defined specifications can expedite circuit design while excessive or arbitrarily tight specifications will reduce yields and increase cost.

Custom Design Schedule

Task	Time in Weeks
Define Specifications	—
Circuit Design	2 to 10
Breadboard Construction	2 to 8
Breadboard Approval	3 to 4
Circuit Layout	2 to 8
Prototype Construction	3 to 8
Production Pilot Run	8 to 12
Production Volume	12 to 16

Total 32 to 66 weeks at an engineering cost of between $20,000 and $50,000 but not including special test hardware or assembly tooling.

Integrated Component Capability

Transistors:
NPN — Beta to 300, BV_{CES} to 120 V, f_T to 500 MHz
PNP — Beta to 40, BV_{CES} to 100 V, f_T to 4 MHz
MOS — P channel or CMOS, V_{TH} 0.8 to 2.5 V, BV_{DS} to 18

Resistors:
Diffused — 5 Ω/□, to 100 Ω, 100 V
135 Ω/□, to 100 kΩ, 100 V
Ion Implant — 500 Ω/□ to 4 kΩ/□, to 4 MΩ, 20 V
Thin Film — 2 kΩ/□, to 2 MΩ, 250 V
Aluminum — 0.025 Ω/□, to 1.0 Ω, 150 V

Capacitors:
Junction — 0.1 pF/mil^2, to 30 pF, 100 V
0.3 pF/mil^2, to 100 pF, 12 V
0.9 pF/mil^2, to 300 pF, 6 V
MOS — 0.1 pF/mil^2, to 30 pF, 50 V
0.2 pF/mil^2, to 50 pF, 20 V

Diodes:
Zener — 5.7 or 7.0 V, ±0.3 V
Photo — 0.5 A/W or > 300 nA/fc at 800 nm
Schottky — 0.1-0.4 V at 1 μA to 0.3-0.6 V at 1 mA
Small Signal — BV = 7 V
Varactor — $C_0/C_5 \approx 2$

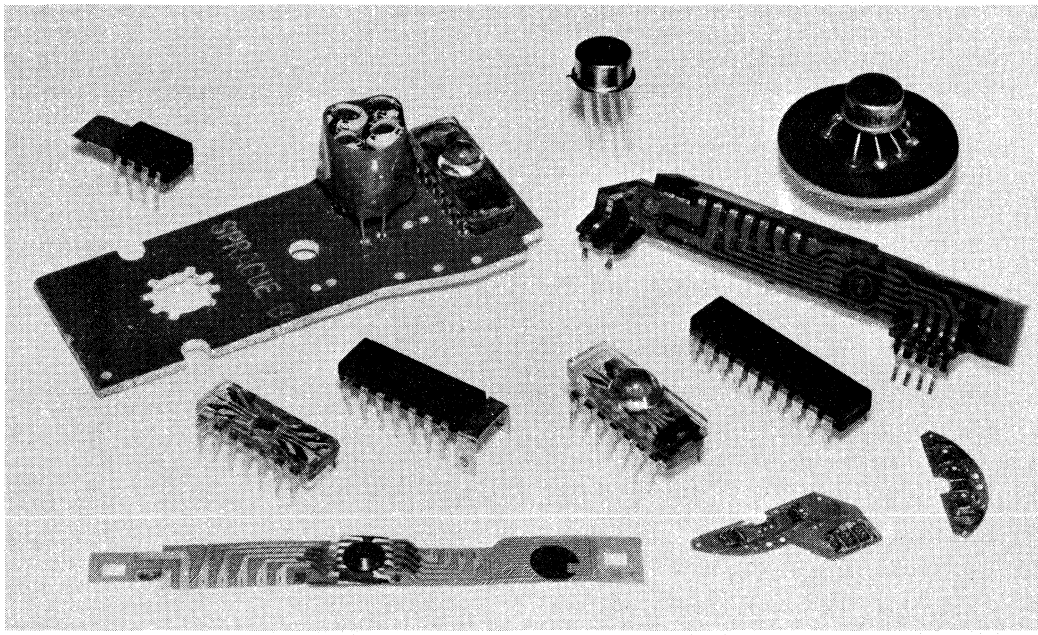
Other:
SCRs — to 1 A, to 60 V
PUTs — to 1 A, to 60 V
I^2L — propogation delay typically 100 ns
BiMOS — High-power bipolar plus low-power MOS
Hall Cells — 35 mV/kG

6

Application Areas of Sprague Expertise

TV — NTSC or PAL; video, chroma, sound, sync., IF
Toy — sound generators and amplifiers, optolinear, timers, controls
Camera — photodiodes, light integrators, timers, controls
Transistor Arrays — small signal, control, high current, SCR
Control — Schmitt triggers, timers, Hall cells
Radio — AM, FM, FM stereo, AM stereo
Safety — GFI, smoke detectors, burglar alarms
Audio — 250 mW to 10 W, mono and stereo
Automotive — controls, monitoring, safety, radio, clock
Interface — display drivers, Hall cells, optolinear
Military — communications, fuze, interface
Computer — interface to ± 120 V or 1.5 A

Optional Package Capabilities



Standard integrated circuits from the Sprague Electric Company are most often furnished in packages meeting industry or military standards (JEDEC TO-87, TO-91, TO-99, TO-100, or TO-116, or MIL-M-38510). However, on special order, other packages or assemblies of packaged devices may also be supplied. A few special order devices are illustrated above and include special heat sink tabs, subminiature plastic packages, printed wiring boards, flexible circuits, and complex assemblies. Devices incorporating photodiodes are furnished in clear plastic cases.

See Also:

Expanding the Frontiers of IC Interface For Electronic Displays

INTRODUCTION

The original monolithic high-voltage/high-current power drivers from Sprague were capable of sustaining 100 V and sinking load currents of 250 mA on each of four outputs. That 1970 peripheral driver capability has since been expanded and improved on to solve many of the most difficult display interfaces. Our newest devices are rated for operation to 130 V, sourcing or sinking to 1.5 A, and as many as eight drivers per package (not all together) with inputs for TTL, Schottky TTL, DTL, CMOS, and PMOS.

LAMP (INCANDESCENT) INTERFACE

Utilizing marketing inputs that related to existing hybrid interface circuits, a group at Sprague designed and manufactured monolithic ICs which initially were largely used for aircraft indicator lamp interface. Although not widely known, these quad driver units were developed quite independently (and simultaneously) to the ubiquitous 75451 series of high-speed, low-voltage peripheral drivers. A concentration upon circuit design factors, improvements in DIP packaging (copper alloy lead frames), and tighter, tougher control of diffusion-related parameters has allowed the manufacture of quad power drivers rather than the dual mini-DIPs offered by other sources.

An increased awareness for improvements in reliability and space and power reductions provided a rather successful military market for Sprague lamp and relay interface; early success was evident in military aircraft indicator lamp interface, a tough application for TTL type ICs due to severe inrush currents resulting in secondary breakdown during "turn on". The increased current sinking capability of the Sprague ICs offers a solution to lamp interface that usually obviates the need for "warming" resistors (across the output) which slightly warm the lamp filament and thus minimize problems associated with cold lamp filaments.

The relay driver types of Sprague IC drivers (and other similar transient-protected ICs) are somewhat more useful than the so-called general purpose types, since the diode common terminal may be switched for a system "lamp test". As shown in Figure 1, only a single connection to each DIP is required.

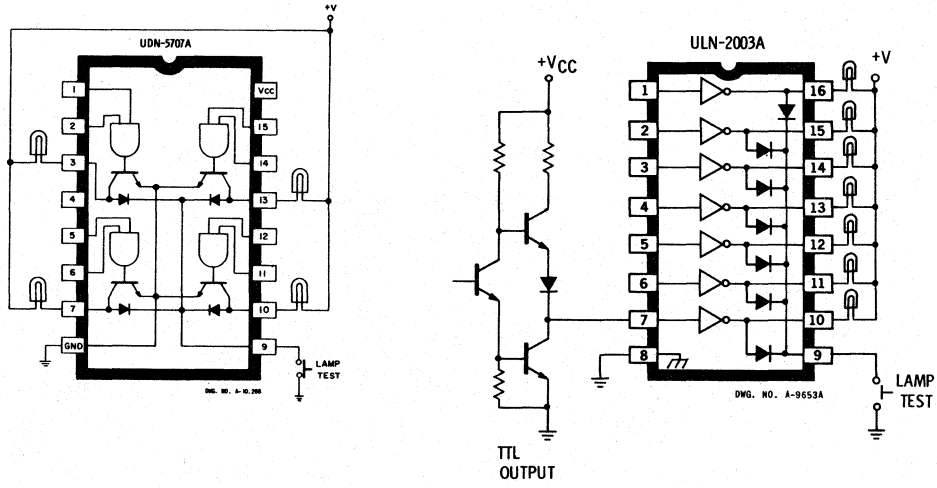


Figure 1

The high current-sinking capability of the Sprague ICs allows such loads as the #327 or #387 lamps (usually two in parallel - 28 V at 40 mA each) to be driven without difficulty of secondary breakdown. The device beta will usually not allow sinking of the 10 to 13 times (nominal value) inrush current of cold lamps; but the lamp rapidly reaches a current level within the device output limitations (Figure 2 shows current as a function of time for a single #327 lamp). Sustaining this instantaneous inrush current and its peak power has been a key element in the success of many lamp interface circuits.

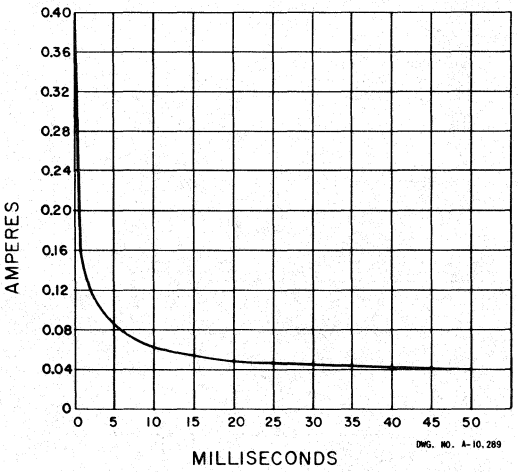


Figure 2

GAS DISCHARGE DISPLAY ICs

Early in 1972, Sprague successfully produced its first high-voltage IC designed for gas discharge displays - a five channel, 130 V unit for cathode (segment) interface. Subsequently, other circuits, both cathode and anode drivers, were produced; most of which were used in calculator applications with the Burroughs Panaplex® II. In Figure 3 is shown a display interface system utilizing the UHP-481 and UHP-491 display drivers, associated thick-film networks, and discretes. This was a step forward, but still required external discrete components.

Through a collaborative effort begun late in 1973 between Sprague Electric and Burroughs Corp. a newer, more efficient interface scheme evolved. Featured in "Electronic Displays '75", this series of monolithic IC interface devices for the high-voltage gas discharge panels has been one of the trailblazers in the world of display interface ICs. Intended for use in multiplexed display systems, these ICs present one of the easiest and least expensive solutions to a difficult interface problem. A combination of high-voltage bipolar techniques with thin-film resistor technology (circuit resistors sputtered over the IC dielectric) has provided both digit (anode) and segment (cathode) interface.

To facilitate a minimum component interface, a split supply ($\pm$ 100 V) is employed to allow d-c level-shifting (rather than capacitors or>200 V transistors) and both digit and segment drivers incorporate all pull-up, pull-down, current limiting, off-bias reference, etc. which were formerly required in discrete and/or hybrid systems. With the combination of the digit and segment drivers (each capable of withstanding 120 V), the split power supply approach affords PN diode IC technology suitable for driving a display usually requiring a 180 V minimum ionization voltage (equivalent to $\pm$ 90 V in the split system).

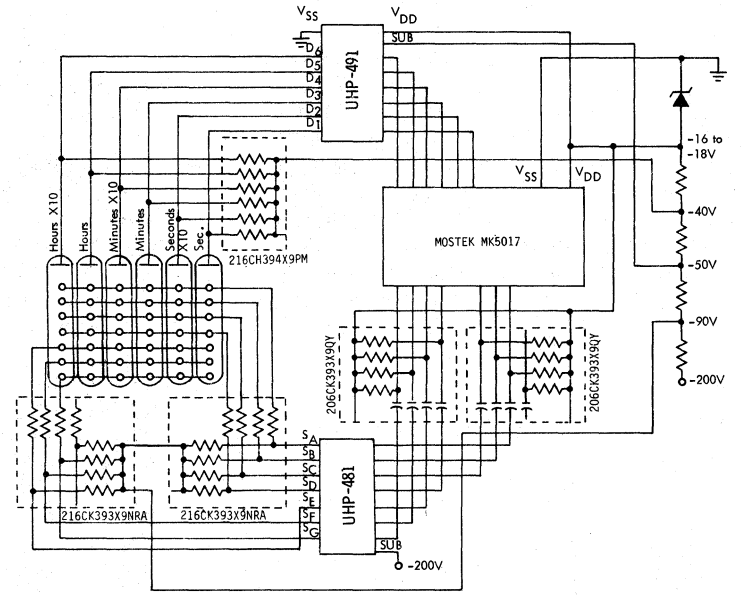
The use of the Series UDN-6100/7100A gas discharge display drivers shows the need for only two monolithic ICs for displays of up to eight digits and eight segments as shown in Figure 4. Systems requiring digit or segment counts greater than eight employ additional driver ICs, and with the exception of the Type UDN-7180A segment driver, the segment ICs all have outputs with internal current-limiting resistors for the display segments. The UDN-7180A device, for reasons of package power dissipation and/or dissimilar segment currents (certain 14 or 16 segment alphanumeric panels) can also be used, but must have external, discrete current-limiting resistors.

Higher current applications are difficult for both programmable current and switching type display drivers. Segment currents beyond 2.5 or 3 mA present package power dissipation limitations to most dual in-line packages. By using external resistors, the Type UDN-7180A driver allows segment currents of up to 14 mA.

The transistor switch with current-limiting resistor scheme used in Sprague gas discharge display drivers also minimizes problems associated with gas panel arcing which can destroy programmable current circuits. Some of the gas display manufacturers recommend the use of series resistors in each segment

APPLICATIONS INFORMATION (Cont'd)

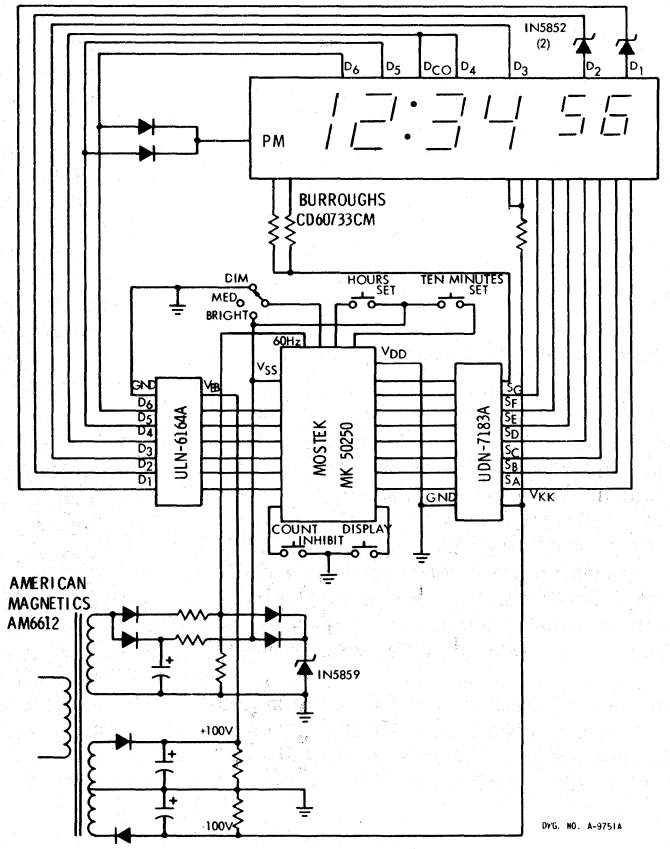
Figure 3



Type 206C and 216C are single in-line networks

DWG. NO. A-9413A

Figure 4



DWG. NO. A-9751A

line to prevent destruction to the semiconductor interface circuit should such a panel arc occur. Without these series resistors (internal thin-film resistors in Sprague devices) the IC can be destroyed by the high voltage and resulting high current should the panel voltage drop to a very-low level during an arc.

LED INTERFACE

With the obvious abundance and variety of LED interface integrated circuits it would seem unlikely that there are still systems in search of an IC hardware solution to further minimize cost, component count, space, etc.; but this is definitely the case. The deficiencies are chiefly related to the limited number of current-sourcing circuits and/or high-current drivers.

The efficiency of LED displays has improved, but with the larger digits (up to 1" presently) most of the IC drivers are unable to switch the higher currents required in multiplexed systems. The rule-of-thumb generally applied uses the suggested d-c current - multiplied by the number of digits in the display. For example, a multiplexed display of 160 mA peak current will give approximately the same light intensity output as a steady 20 mA in each of eight digits. Of particular difficulty is the switching of currents associated with the lower efficiency yellow and green LEDs. Sprague has provided monolithic integrated circuit solutions to applications requiring segment currents of 350 mA and digit currents of up to 1.5 amperes!

Many of the Sprague ICs used in high-current LED applications were originally designed for use with electro-mechanical loads (relays, solenoids, motors, etc.) although the high-voltage ratings of the drivers are obviously not a concern. A combination of high-current, high-voltage Darlington drivers is shown in Figure 5.

The ULN-2074B source driver is utilized as a modified emitter-follower. Through the use of discrete diodes in the common collector line, allowing the base to be switched to a potential higher than the collector, it is then possible to obtain a saturated output. This prevents the usual emitter-follower problems associated with gain, the MOS output impedance, and power. It is also possible to now better define the voltage at the emitter output and to then provide suitable segment current-limiting resistors for the LEDs.

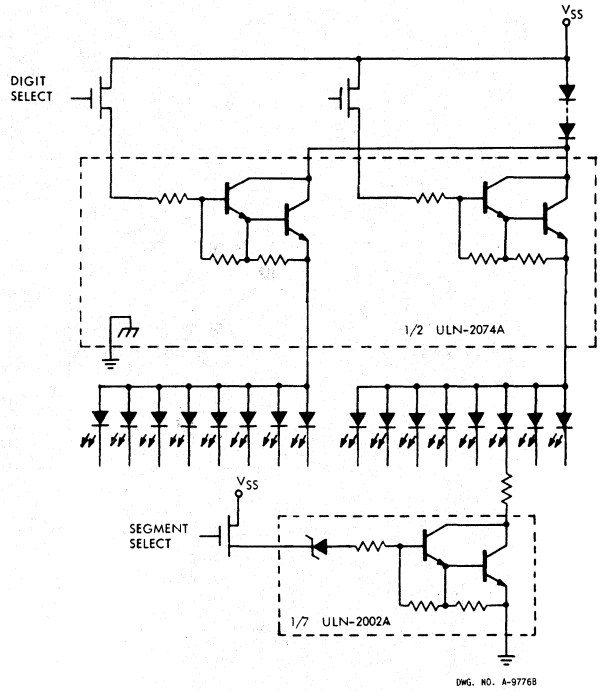


Figure 5

The ULN-2002A sink driver is a high-current Darlington array with the capability of switching multiplexed LEDs with an available limit of 155 mA for each of the seven drivers when used at a 100% duty cycle. Even the more inefficient yellow or green LEDs can be driven with higher output currents at lower duty cycles (400 mA at a 28% duty cycle).

A new eight-channel source driver is shown as a digit switch for common anode LEDs in Figure 6. The Series UDN-2980A drivers will handle output currents to a maximum of 500 mA. Two basic versions of the driver will allow interface from TTL, Schottky TTL, DTL, PMOS, and CMOS levels. Other versions of the ULN-2003A driver are also available for use with the various logic levels.

Of the three sink drivers shown, the ULN-2003A is probably the better choice from a standpoint of both pinout and component count. It also has straightforward in-out pinning. The ULN-2031A and ULN-2081A devices offer lower cost. They are also interchangeable from a pinning aspect although the output ON voltage will be dissimilar.

A common-cathode LED configuration is shown in Figure 7 for currents of up to 1.5 A per digit! A series UDN-2980A source driver is used to switch the segment side, the ULN-2064B or ULN-2074B to switch the digit side. As has been shown with Figure 5, the IC package power dissipation must be considered with high-current applications.

The three examples that have been shown for LED interface represent only a very-small portion of the total applications area. The high-current capabilities and high gain of the Sprague drivers represent potential solutions to many difficult LED display systems - alphanumeric, seven-segment, or matrix; common-cathode or common-anode; continuous or multiplexed.

A-C PLASMA DISPLAY INTERFACE

Plasma displays, such as those manufactured by National Electronics/NCR (USA) and NEC or Fujitsu (Japan), all have one common element with their gas discharge cousin - both types use a neon gas mixture. The plasma panels emit an orange glow when

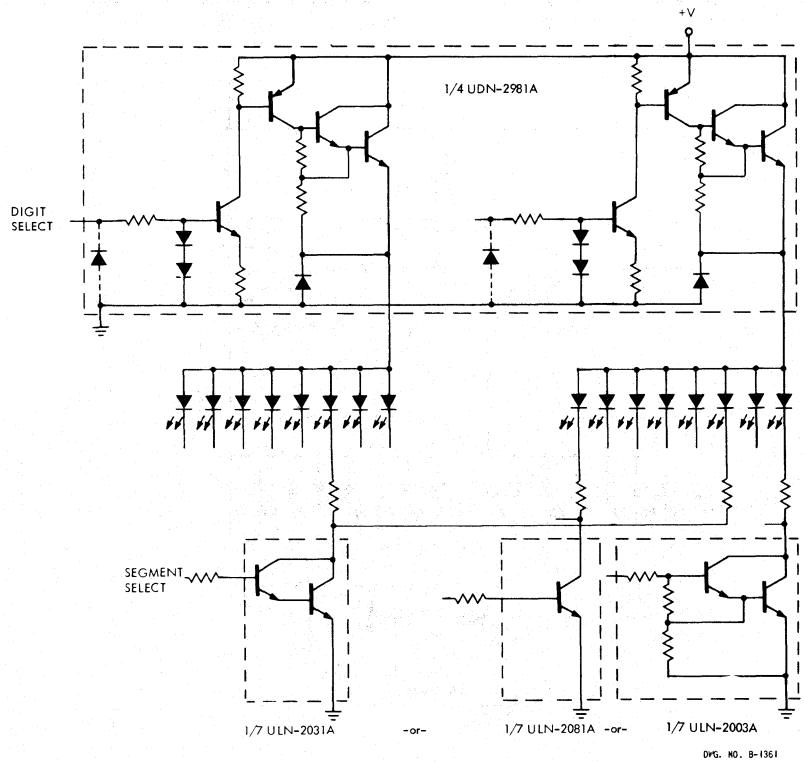


Figure 6

switched at rather high frequencies, and light output intensity is a function of frequency. The a-c term for the plasma display is something of a misnomer since these panels actually operate from a toggled d-c supply (usually in the area of 20 kHz).

The panel is basically a neon-filled capacitor, and has plates (electrodes) which are covered with the dielectric - between which is the neon mixture. Switching this capacitive load presents a problem with high peak currents in addition to the older problem of the high voltages which are associated with gas displays. Drive circuits use supply voltages of 150 to 260 V (depending on unipolar or bipolar drive), and the semiconductors used must switch instantaneous currents in the order of several hundred milliamperes for the larger displays.

Several high-voltage, high-current arrays made at Sprague Electric can provide an answer to one side of the a-c plasma display interface. The Series ULN-2020A Darlingtons are rated at 95 V while the Series UHP-500 power drivers are rated at 100 V. They are both able to handle the application shown in Figure 8 (a basic d-c, non-multiplexed clock interface rather than a more complex multiplexed system). The ULN-2022A is specifically designed for 14 to 25 V PMOS logic levels while the UHP-506 is intended for use with TTL.

The high-current diodes that are internal to the Sprague arrays are utilized in the unipolar drive scheme connected to a suitable OFF reference. In one POS application, a set of 14 ULN-2023A Darlington drivers replaced more than 400 discrete components. The cost and space savings in such a machine are considerable, and a very complex printed wiring board was greatly simplified.

Further improvements in interface and plasma displays will no doubt evolve, and thus benefit all concerned - display and interface vendor along with the end user. Plasma displays are well-suited to custom panels (particularly those with various sizes of characters) and with improvements in IC breakdown voltages some further simplification of interface should evolve.

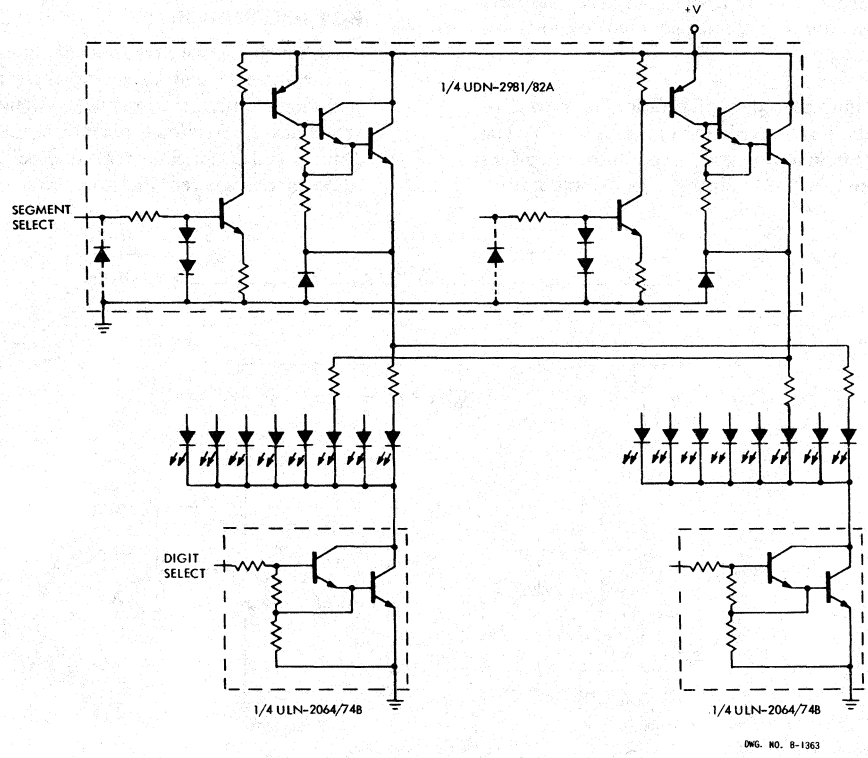


Figure 7

FLUORESCENT DISPLAY INTERFACE

Although the vast majority of fluorescent displays are directly driven from MOS logic (handheld and low-cost desk calculators), there is an emerging need for interface integrated circuits for use with the larger characters (higher currents) and the higher voltages coming into use. These blue-green display panels originated in Japan, and the manufacturers are quite aggressively pursuing markets such as POS systems, clocks, cash registers, appliances, automotive displays, etc. Larger and/or more complex styles are being made, including displays with alphanumeric capability (a starburst 14 or 16-segment pattern).

Modest voltage capability (60 or 70 volts) is all that is required of a semiconductor device to drive these panels, and the currents are in 20 to 30 mA region. These electrical requirements are well within the capability of many gas discharge digit drivers. In Figure 9, the UHP-491 is shown used with pull-down resistors connected to each output. When both the segment (equivalent to a vacuum tube anode) and the digit (controlled by the grid) are switched sufficiently positive with respect to the cathode (filament), the appropriate display digit/segment are energized.

Another multiplexed configuration is shown in Figure 10; the difference being that a push-pull type of MOS output is in use, and the pull-down rail does not allow the UHP-491 substrate, V_{DD}, and output potentials to be the same. The substrate and output are tied to the most-negative rail, while the V_{DD} terminal connects to the – 12 V line for the MOS.

Since these solutions using the older gas discharge digit driver circuits require the use of appropriate pull-down resistors, either in discrete or thick-film network form, a more suitable solution employs the circuit shown in Figure 11. The UDN-6118/28A devices are designed specifically for use with fluorescent displays and include internal pull-down resistors so that up to eight segments and eight digits will require only two packages and a greatly simplified power supply. The Type UDN-6118A driver is compatible with TTL, Schottky TTL, DTL, and 5 volt CMOS. The Type UDN-6128A driver is for use with 6 to 15 volt PMOS or CMOS logic.

The future of fluorescent displays looks rather strong, particularly if competition further reduces prices. For the moment at least, these displays will not seriously tax the capability of IC interface except, perhaps, from a price/cost standpoint.

HOT WIRE READOUTS

Although hot wire readouts could easily be placed in the incandescent category, their application in multidigit, multiplexed display systems more closely resembles LED circuit operation. Since hot wire displays will conduct current in either direction, isolation diodes are required to prevent "sneak" paths

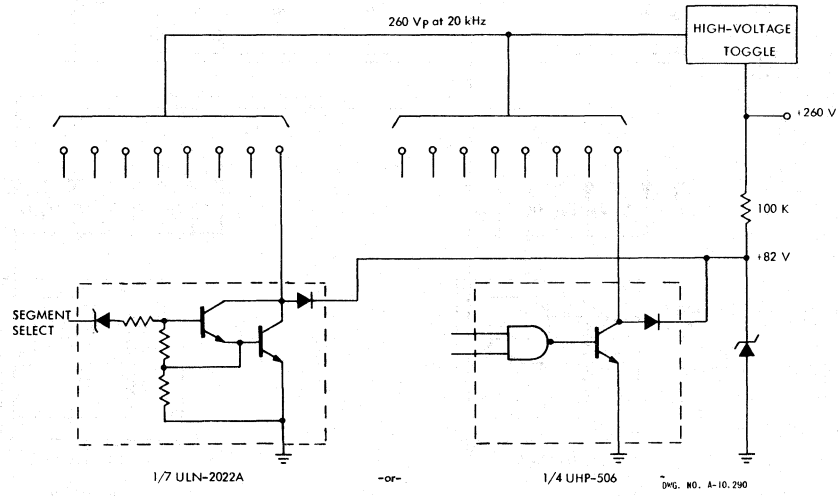


Figure 8

from partially turning ON unaddressed segments. Compare the typical hot wire display of Figure 12 with the LED display of Figure 6. The availability of a suitable, inexpensive diode array would be of considerable asset in multiplexed hot wire systems.

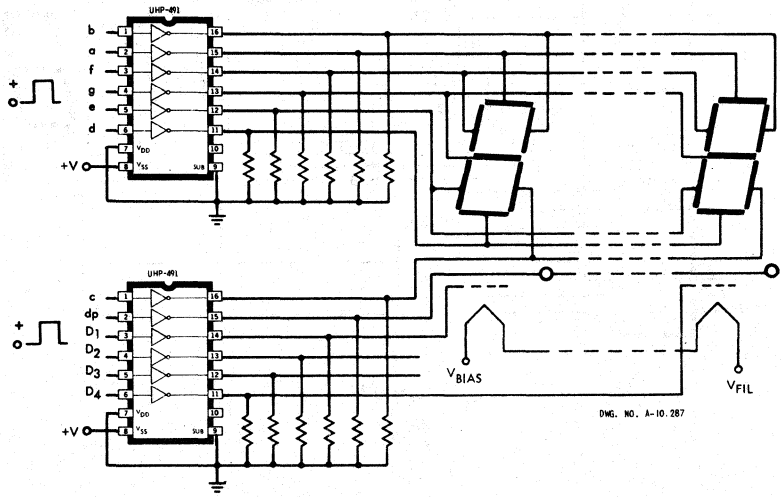


Figure 9

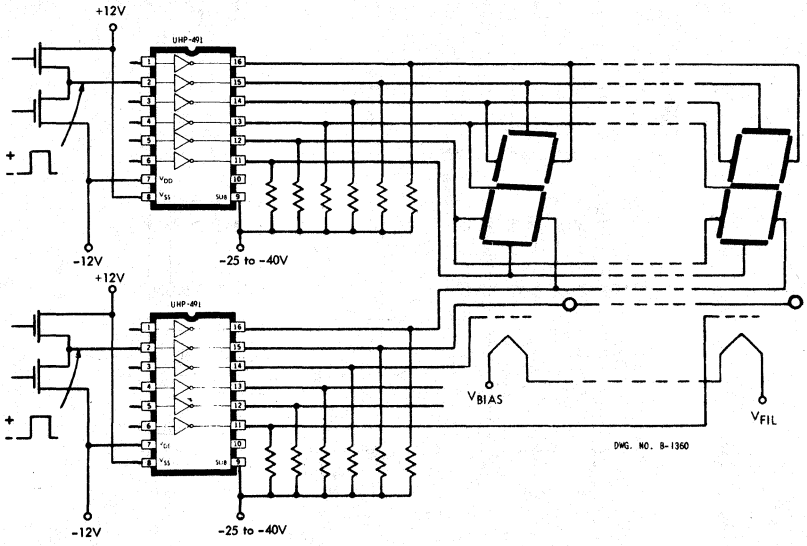


Figure 10

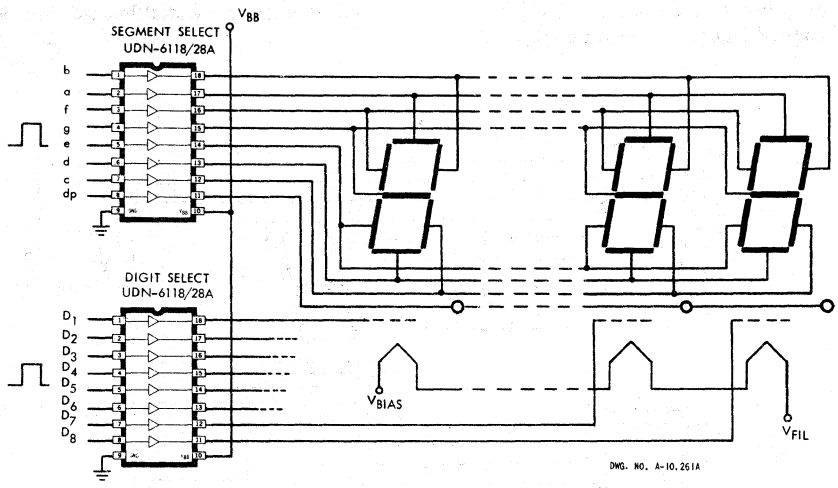


Figure 11

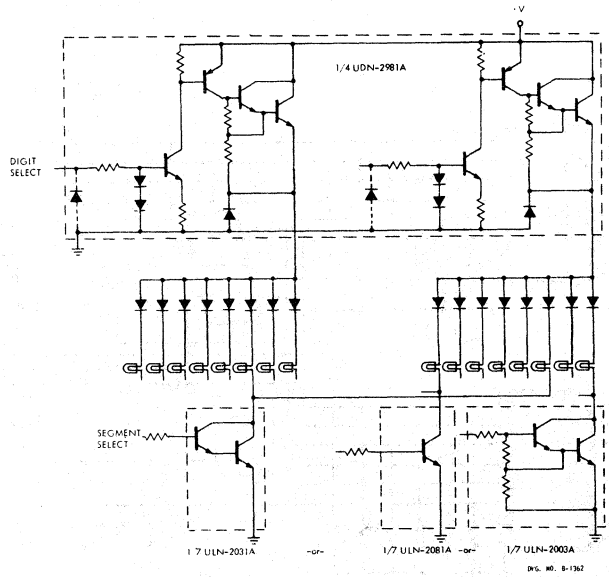


Figure 12

The hot wire readouts are available in both seven-segment and alphanumeric (16-segment) versions and are quite well-suited to high ambient light applications. They do not wash out in sunlight, although their reliability diminishes with the higher currents required in brightly lighted applications. As described, multiplexed schemes can be cumbersome because of the great number of discrete diodes required. One avionics system using a 16-character, 16-segment alphanumeric panel required 256 discrete diodes!

GLOW TRANSFER - BAR GRAPH & MATRIX PANELS

Neon-based display technology has shifted into many new market areas. The Burroughs Self-Scan® is a solution to many alphanumeric applications; the newer bar graph is a solid state replacement for analog instrumentation. Both use the glow transfer principle of the dot matrix Self-Scan display.

The nominal voltage for this type of panel is 250 V. High-voltage gas discharge drivers (Series UHP-480) or Darlington arrays (Series ULN-2020A) afford a cathode interface to the glow transfer panel. With a typical display current of 3 to 5 mA, the gas discharge drivers are perfectly adequate. For higher current applications, the Darlington arrays are a solution.

As illustrated in Figure 13, the bar graph cathode is easily driven with a Series UHP-480 driver. Signal level shifting is inexpensively accomplished with capacitors; the OFF reference, pull-up, and pull-down is done with a few discretes. The anodes are driven with two discrete transistors ($BV_{CES} \geq 120$ V). By utilizing a negative supply, the level shifting is easily done in the cathode side. If a positive supply were used, relatively complex d-c level shifting would be required in the anode side. The few discretes necessary in the circuit shown are generally a viable solution when faced with cost and space parameters for the system.

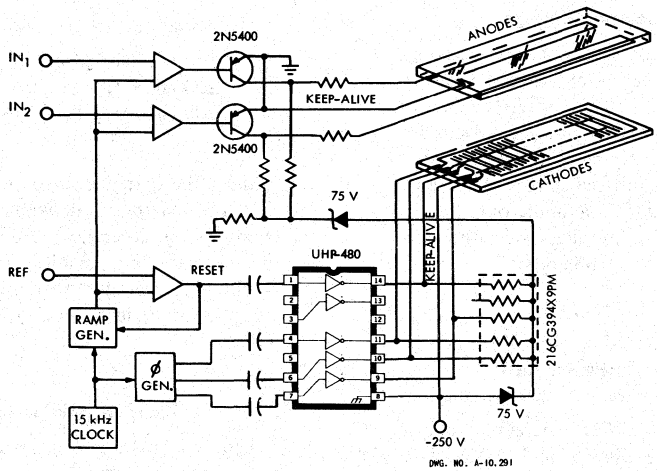


Figure 13

SUMMARY

The phenomenal growth in display technology has largely come as a result of the electronic calculator, and electronic displays will pervade all our lives in an ever-increasing number of products. The use of digital displays in appliances, gasoline pumps, electronic games (even pinball machines), etc., etc., etc., will also require that a continuing evolution of interface integrated circuits meet the challenges of higher brightness, increased currents, improved reliability, and lower system costs.

Both the display and semiconductor industries have demonstrated that they will meet the challenges of today, and these challenges then become routine with tomorrow.

Electrical Characteristics for Series ULN-2000A Darlington Arrays

Introduction

With the tremendous industry acceptance of the Series ULN-2000A high-performance Darlington arrays has also come a large number of inquiries relating to their application and specifications. A considerable amount of applications material has been, and will continue to be, generated as it can be identified, prepared, and published. It is now necessary to comment on and further explain the devices' electrical specifications.

Please note that much of this information is equally applicable to the Series ULN-2000A and the Series ULS-2000H; the major differences being the hermetic package, the lower package power dissipation, and the wider operating temperature range of the latter devices.

Absolute Maximum Ratings

Referring to the applicable data, under this heading are limits that indicate potential impairment of device performance and/or reliability if exceeded. The devices are very conservatively rated and it should therefore be noted that devices can often be specified (after factory concurrence) with improved limits. The most common variation is increased maximum output voltage (for example 95 V) as is described under the Output Leakage Current section of this report.

Power Dissipation, P_D

Still under the Absolute Maximum Ratings, the power dissipation ratings and derating factor are specfications which often require some further explanation.

At temperatures up to +25°C, the maximum allowable average package power dissipation is 2.0 W. This rather high limit is primarily as the result of going to a copper alloy lead frame instead of the previous standard iron-nickel-cobalt alloy (Kovar) lead frame. The total thermal resistance is only 60°C/W (thermal conductance of 16.67 mW/°C). As usual, the maximum allowable junction temperature is +150°C. The thermal equation is:

$$P_D = (T_J - T_A)/R\theta \text{ or}$$
$$P_D = G\theta\,(T_J - T_A)$$

where P_D = allowable average package power dissipation

T_J = allowable junction temperature (+150°C)
T_A = operating ambient temperature in °C
$R\theta$ = thermal resistance (60° C/W)
$G\theta$ = thermal conductance (0.01667 W/°C)

The actual package power dissipation is the sum of the individual Darlington pair dissipations, each of which is the product of the collector current, the output voltage, and the duty cycle.

A typical example is:

3 outputs at 350 mA at 35% duty cycle
3 outputs at 200 mA at 70% duty cycle
1 output at 100 mA at 100% duty cycle
ambient temperature of +70°C

From the above equation, the allowable average package power dissipation is

$$P_D = (150°C - 70° C)/(60° C/W)$$
$$P_D = (80° C)/(60° C/W)$$
$$P_D = 1.333 \text{ W}$$

The actual desired power dissipation is

350 mA x 1.6 V x 35% x 3 outputs = 0.588 W
200 mA x 1.3 V x 70% x 3 outputs = 0.546 W
100 mA x 1.1 V x 100% x 1 output = 0.110 W
Total = 1.244 W

Since the actual desired power dissipation is less than the maximum allowable, this set of operating conditions is acceptable. Additional information on the thermal characteristics of integrated circuits can be found in Sprague Technical Papers TP 74-1 and TP 74-4 and Microcircuit Application Report MAR 73-1.

Output Leakage Current, I_{CEX}

The first characteristic shown under the electrical characteristics is the Output Leakage Current. This characteristic is tested with the input open-circuited for all type numbers, and then with an applied input voltage for the ULN-2002A and the ULN-2004A. Each Darlington output is tested at the rated maximum output voltage (50 V). The limit shown is the total leakage current (collector-to-base, isolation, and substrate). Collector-base leakage current is shunted to the common emitter terminal through the 7.2 kΩ base-emitter resistor, and will not be amplified by the Darlington input stage. The power output stage also has a base-emitter resistor, but its effects are somewhat less.

The Type ULN-2002A and ULN-2004A are tested with an applied input voltage to assure a specified threshold level for each type.

The Output Leakage Current tests serve to guarantee the minimum output breakdown voltage. Any output which will not meet the leakage current limit either has a breakdown below the specified test voltage, or excessive leakage current, and is rejected. Customers ordering increased or decreased output breakdown voltage versions can also be served (Series ULN-2020A devices are guaranteed to a minimum 95 V output voltage).

Collector-Emitter Saturation Voltage, $V_{CE(SAT)}$

After the Output Breakdown Voltage, the Collector-Emitter Saturation Voltage is probably the most important device parameter. The limits shown should be used in determining the actual maximum device power dissipation at the specified collector current and ambient temperature.

The saturation voltage is also an indicator of the minimum overall Darlington gain with the output well into saturation (see also, the h_{FE} characteristic for the Type ULN-2001A). At 350 mA, the minimum "black box" gain is 700; at 200 mA, the gain is 570; and at 100 mA, the minimum gain is 400. The gain of the Darlington stage appears to fall off with lower input currents due to the effect of the input base-emitter shunt resistor.

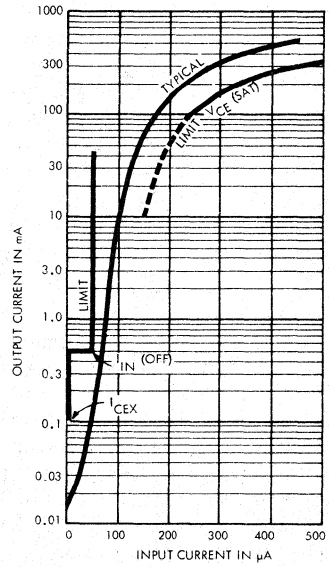
Input Current, $I_{IN(ON)}$

This test is performed on all Series ULN-2000A devices which contain input current limiting elements.

The input test voltages are not arbitrary specifications but are typical voltage levels as found in the recommended normal applications for each device. Generating the most inquiry has been the 3.85 volt level for the ULN-2003A. The test voltage represents an extrapolated maximum limit for TTL (high V_{CC} and maximum logic "1"). A standard TTL output is fully capable of sourcing currents well beyond the 400 μA test condition associated with its 2.4 V guaranteed minimum logic "1" output voltage. Unfortunately, this is not well defined by the suppliers. This same lack of specifications is also true for low-power Schottky TTL with a 2.7 volt minimum logic "1" output voltage.

If the logic output limits are still in doubt, either consult the factory or use appropriate pull-up resistors (input to V_{CC}) to increase input current to the Darlington as described in Sprague Application Note 29304.9.

All of the devices which employ input current limiting will safely withstand the continuous application of as much as +30 volts on any input.



Series ULN-2000A Darlington Arrays

Input vs. Output Current

Note: Since this application report was published an increased output current version (Series ULN-2010A) and the increased output voltage version (Series ULN-2020A) have been finalized. In addition, a new Type ULN-2005A has been designed for use where higher source loading is not a problem and high output currents are required.

Input Current, $I_{IN(OFF)}$

This test continues to be a topic of considerable discussion. Stated simply, it represents the level of input current which will NOT produce more than 500 μA output leakage current at the high temperature limit. The device will not turn "ON" with any input current up to the specified minimum guaranteed limit. Beyond the minimum, the circuit will gradually turn "ON"; the actual collector current being determined primarily by the value of the input base-emitter resistor for low values of input current.

The specified minimum input current corresponds to a maximum allowable logic output leakage current and is particularly useful when operating with open drain PMOS.

Input Voltage, $V_{IN(ON)}$

The Input Voltage tests again illustrate the "black box" approach to the application and testing of these high-voltage, high-current Darlington transistor arrays. Like the Input Current test, the Input Voltage specifications apply only to those devices which contain input current limiting elements.

With the specified maximum input voltage applied, there is a guarantee of at least the level of collector current listed, with a saturation voltage of not more than 2 V.

As shown, the maximum Input Voltage for each device determines the range of applications for that device. Using the Type ULN-2003A array as an example; the minimum logic "1" output level for 7400 type TTL (2.4 V) will result in at least 200 mA collector current, the minimum logic "1" output level for low-power Schottky TTL (2.7 V) will result in at least 250 mA collector current, a more realistic logic "1" output level for TTL and most 5 volt CMOS (3.0 V) will result in a typical minimum of 300 mA collector current at an ambient temperature of +25°C.

Variations in integrated circuit component values can and will happen. However, this particular test assures a minimum output current with a given input voltage level. Device characteristics may change, but this type of "black box" testing assures functionality while allowing design and process variations from the nominal circuit design.

Applications requiring the paralleling of Darlington inputs (either for higher output sink current or for multiple loads) can be accommodated, provided the logic current source is capable of furnishing enough drive current. Alternatively, the use of pull-up resistors, as described in Sprague Application Note 29304.9, may be employed.

D-C Forward Current Transfer Ratio, h_{FE}

The Type ULN-2001A Darlington transistor array is the basic device in this series. Although there is no input current limiting, a "black box" approach must still be taken because of the effect of the input base-emitter resistor. Input current is shunted in this resistor and the minimum individual transitor gains must be higher. The minimum gain of a device passing the ULN-2001A specifications might easily be 2000 without the input base-emitter resistor. Here again, the intent is to provide function rather than meaningless (although accurate) device specifications.

Customers accustomed to standard discrete device specifications frequently find our test methods somewhat unusual. Our intent is to describe a usable function without becoming bogged down in a conglomeration of trivial discrete device parameters.

Input Capacitance, C_{IN}

The Input Capacitance specification describes all capacitances associated with each individual input. It is a composite of lead and wire capacitance as well as the junction capacitance of the Darlington input. This specification was requested by an early customer and it was incorporated into the standard product.

Turn-On Delay, t_{PLH}

The Series ULN-2000A uses the industry-standard method of specifying Turn-On Delay time. This characteristic is measured from the 50% point of the positive-going input pulse to the 50% point of the output waveform when switching typical load currents.

Turn-Off Delay, t_{PHL}

Turn-Off Delay time is measured from the 50% point of the negative-going input pulse (trailing edge) to the 50% point of the output waveform as the Darlington switches "OFF."

Clamp Diode Leakage Current, I_R

The suppression diode at each Darlington output is tested at the rated maximum output voltage. This test at reverse bias, and the following forward voltage test, are equivalent to conventional tests on discrete diodes.

Clamp Diode Forward Voltage, V_F

Each output diode is tested for its forward voltage drop at a current level compatible with the Darlington output sink capability. An application utilizing these transient-suppression diode characteristics to perform the lamp test function is described in Application Note 29304.9 (Figure 6).

Summary

The intent of this applications material was to answer some common questions and to clarify some of the bulletin specifications for the Series ULN-2000A high-voltage, high-current Darlington transistor arrays. Specifications can often be difficult to interpret, especially when comparing discrete and monolithic devices. Because of this, the Series ULN-2000A arrays are specified as "black box" functions and tested accordingly.

DTL Peripheral/Power Drivers "A Giant Step Backward" Reverting to DTL Adds New Dimensions To Sprague Peripheral/Power Drivers

Introduction

Although not widely known in the industry, Sprague Electric was one of the pioneers with Peripheral/Power Driver ICs, with our Series UHP-400/500 Quad Drivers introduced in 1970.

The design and manufacture of a quad driver meant rather dramatic deviations from any standard bipolar processing/packaging/circuit design techniques in use at the time. To allow the use of four high-current outputs in the same dual in-line package necessitated the development of high Beta, high-current, high-voltage output NPNs; chiefly done to minimize package power dissipation when confronted with a quad 14-pin DIP rather than an 8-lead dual mini-DIP driver. Reducing the I_{CC} drive power for the output transistor by improvements in high current Beta significantly affected the overall package power.

Further it was necessary to utilize a copper alloy lead frame for the DIP if the units were to be used in systems requiring the four outputs to be energized continuously and simultaneously. The standard Kovar (iron alloy) in use definitely would not allow this, but the change to a copper alloy package frame reduced the DIP θja (junction to ambient rise) from +125°C/W (Kovar) to +60°C/W (copper). The combination of the high Beta process and dramatic improvement in package technology permitted our quad power drivers to simultaneously and continuously switch 250 mA in all four outputs in a +70°C ambient without exceeding a junction temperature of +150°C.

The Sprague Electric series UHP-400 and UHP-500 Quad Drivers have been an industry standard. The UHP-407/507 is shown in Figure 1. These ICs are available with NAND, NOR, AND, and OR logic gates and with three output breakdown minimums: the UHP-400-1 series at 40 volts, the UHP-400-1 series at 70 volts, and UHP-500 series with 100 volt output breakdown. Additionally, there are four basic relay driver types which incorporate internal transient suppression diodes for use with inductive loads. All types are guaranteed to sink a minimum of 250 mA with a $V_{CE(sat)}$ of less than 0.7 volts and are compatible with TTL and DTL logic families.

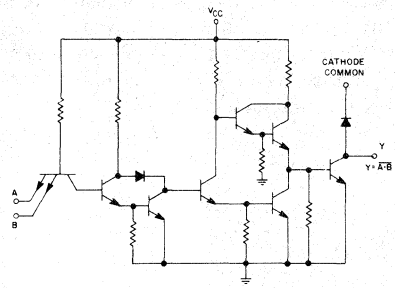


Figure 1

Electromechanical Loads

The Sprague Electric high-current, high-voltage drivers have been designed primarily for use with electromechanical loads. No attempt has been made to produce a high speed device; moderate switching speeds result in less noise generation during output transitions. Virtually all peripheral loads are much slower than any semiconductor switching device and it is neither necessary nor desirable to utilize high speed switching for interface to electromechanical loads. Needs for decoupling and/or critical printed wiring board layout are diminished with slower switching devices coupled with the serious attempts to minimize logic circuit power, $I_{CC}(0)$.

High-Voltage, High-Current ICs

Many design and process changes were imposed to create Sprague drivers. To obtain the high voltage output NPNs, it was necessary to modify the N doped epitaxial layer. The epi-layer has been increased in both thickness and resistivity to provide higher output breakdown. These changes caused these ICs to resemble linear circuit processing more than TTL digital process techniques.

Transistor design tolerances were quite dramatically changed to sustain the much higher OFF voltages required of these circuit applications. Much deeper junctions with greater curvature and rounded transistor diffusions (another element of the curvature) were

part of the design modifications for improving breakdown voltages. Through use of these techniques it became possible to achieve breakdowns of 100 volts very repeatably.

A combination design/process addition was also instituted to minimize the output NPN saturation voltage. The use of higher resistivity epitaxial layers would have adversely affected the collector-emitter $V_{CE(sat)}$ were it not for the use of a highly doped, low resistivity collector diffusion. A low resistivity N+ collector plug, which is driven sufficiently to contact the N+ buried (floating) collector diffusion beneath the NPN base was added.

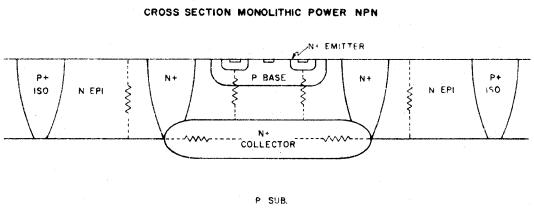


Figure 2

Figure 2 shows the series collector resistance associated with the buried N+ collector plug. Without the low resistance collector diffusion, the series resistance between the buried N+ collector and the metallization on the chip surface would be much higher. Through use of the N+ collector diffusion, which also serves as an N+ surface guard ring to prevent unwanted inversion of the epi, it is possible to achieve an R_{sat} of less than 1 ohm (very large, high-current circuits) to a more standard 2 to 3 ohms collector resistance.

Package Availability

The original Series UHP-400 and UHP-500 quad power drivers have been furnished to commercial/industrial users in plastic DIP using a copper lead frame, thus allowing use of all four outputs simultaneously and continuously at 250 mA each. Two types of fully hermetic packages have also been furnished to meet to MIL-STD-883: a 14-lead ceramic DIP and a 14-lead flat-pack.

Newer additions to this product family, the DTL UDN-3600M and UDN-5700M dual drivers, are furnished in a copper frame 8-lead mini-DIP. The Series UDN-3600M are interchangeable, pin-for-pin, with competitive devices.

The new DTL Series UDN-5700A are available in a new package: the 16-lead copper frame DIP. Use of this package was largely predicated upon the need for all gates to have separate inputs, rather than a pair connected (strobed) together, thus somewhat improving the versatility of the quads. All the newer plastic power drivers benefit greatly from the improved θja of the copper frame package.

The new DTL types with their improved electrical parameters will also be supplied in fully hermetic packages to MIL-STD-883 for use in adverse environments or military systems requiring a full temperature range unit and/or hermeticity. Some reduction in package dissipation potential results, but the ease of interface to logic families, such as CMOS, with the newer DTL circuits will benefit those unable to obtain standard TTL or CMOS logic with either sufficient output current and/or the high breakdown capability (80 volts) of these ICs.

Standard package power curves are shown in Figures 3A (plastic) and 3B (hermetic). The curves of Figure 3A compare the two copper lead frame DIPs with the capability of the Kovar frame packages used for standard lower power circuits. Any area beneath the appropriate package curve represents allowable average power and is plotted against ambient temperature to a +85°C limit. It is quite apparent that both the mini-DIP at +80°C/W and the 14- or 16-lead quad drivers at 60°C/W with copper frames are much superior to the Kovar DIP with a rating of +125°C/W.

The curves of Figure 3B apply to the hermetic packages used with the Series UHP-400 and UHP-500 quad drivers. Note that the materials used and the size of the package have a considerable bearing on the package dissipation limits. The flat-pack is the poorest of all and should not be used unless there is insufficient space (chiefly height) for the hermetic DIP. With either type, the average power is reduced, particularly if the ambient temperature is to reach +125°C.

These θja rating curves show the maximum junction temperature rise with a unit of power applied. The plastic packaged units are generally restricted to uses below +85°C, while the hermetic devices may be used up to +125°C. In either case, the upper junction limit will not exceed a +150°C level and is shown by the dashed lines extending to zero (0) power at +150°C. Operating within these ambient temperature/average power limits will insure that the junction temperature does not exceed +150°C, since variations in manufacturing and electrical parameters are guardbanded.

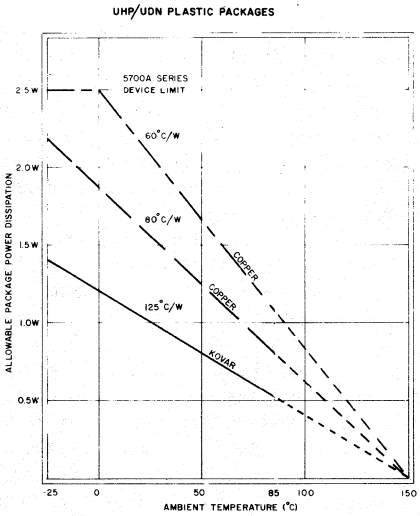


Figure 3A

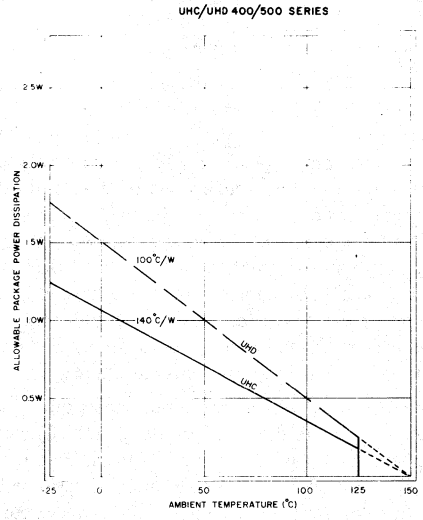


Figure 3B

DTL Logic – "A Giant Step Backward"

Through ongoing evolutionary improvements, the power drivers have seen a series of improvements; the most notable a conversion to a DTL logic gate in the Series UDN-3600 and UDN-5700. Other improvements have affected the high-current output NPN and a small reduction in the typical I_{CC} 0 power.

Converting the logic gate (Figure 4) to a diode input (DTL) has brought about new potential applications with CMOS and PMOS circuitry. Prime advantages are associated with the much higher input voltages allowed (up to 30V), and the extremely low logic "0" input current (100μA maximum vs 1.6mA for a standard TTL). This comparison is between the new, improved Sprague DTL types and competitive devices. The earlier Sprague UHP-400 family had an industry low of 800 μA (1/2 TTL load) and that has subsequently been reduced further to a 100 μA maximum (200 μA on strobe inputs) thus allowing use with CMOS and PMOS logic; while the competitive TTL types have the standard 1.6 mA TTL maximum.

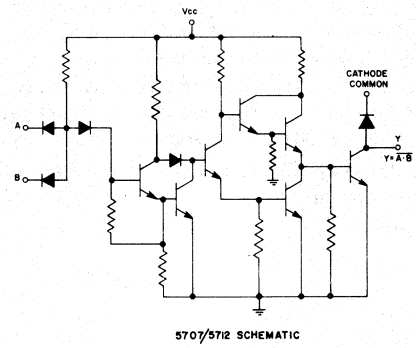


Figure 4

Lamp Interface – Inrush Current

These IC drivers are well-suited to the switching of incandescent lamps. Of great concern to those using semiconductor devices for switching lamp filaments is the high inrush (surge) current associated with cold lamp filaments. When switched with either mechanical or electromechanical switches, this inrush current may reach a value that is 1000% to 1200% of the nominal steady-state current. This 10-12X the nominal can be disastrous to lower current ICs, since they are unable to sustain the instantaneous currents of a cold filament and are prone to destruction; usually resulting from secondary breakdown during turn-on of the output.

A technique frequently employed to obviate this type of failure with lower current devices is the use of "warming" resistors across the switching output. Maintaining the filament partially warmed reduces the inrush (surge) current in the transistor, but it complicates designs considerably when a large number of lamps is used. The high current peripheral/

power drivers are able to sustain these momentary inrush currents; and, hence, it is *not* necessary to add one "warming" resistor for each lamp.

Sprague Electric power drivers have been widely used since 1970 in systems employing them as lamp drivers, and the most typical is a parallel pair of 28 volt, 40 mA lamps (#327 or #387) switched by each NPN output. Even though none of the standard IC peripheral/power drivers available will be in saturation under conditions of lamp inrush, they have been designed to sink currents of 300 mA (well saturated) and are able to sustain the momentary high power. The transistor design and process chosen precludes these drivers from failure due to secondary breakdown when used in a conventional manner.

The current at which the output comes out of saturation is related to the transistor design (chiefly emitter periphery) and process related variables: Beta of output NPN, diffused resistor tolerances (determine base current of output), etc. As the graph of inrush current shown in Figure 5 indicates, the time necessary to reach a current level within the device saturation level is less than 5 ms. Even assuming the use of two lamps in parallel, which is the typical case (current value is thus skewed by a factor of two), the outputs of these power drivers need only sustain an inrush period of approximately 2 to 3 ms (intersection at 0.12 A). The newer DTL units, with a guaranteed output saturation voltage at 300 mA are somewhat better than the earlier UHP-400/500 series, although neither has given trouble with inrush currents when used with #327 or #387 lamps.

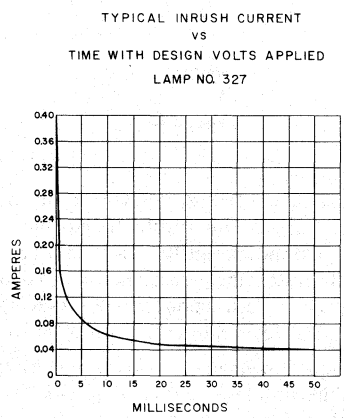


Figure 5

Lamp Interface – D-C

Perhaps the most frequent application of these ICs is the interface to aircraft type lamps such as the #327 and #387, both of which are rated at 28 volts and 40 mA (Figure 6A and 6B). Usually two are connected in parallel (reasons of redundancy) and run from a 28 volt d-c supply. As previously mentioned the full inrush is not likely to be reached due to the limitations of the device output sinking capability and its modest switching speeds (compared with TTL logic). Maximum inrush currents of 10-12X nominal are typically reduced to a value approximating half that level (5-6 times steady state).

Through the use of one of the relay driver versions with its integral suppression diodes, a simple lamp test may be accommodated without the need to use an input on the logic gate. Figure 6A shows the use of an input from each gate for lamp test purposes, but the same function may be achieved using the suppression diodes switched to ground as in Figure 6B. By switching the diode common cathode line with an electromechanical or transistor switch the need for the logic input is obviated; a scheme that requires only one connection per package rather than four (quads) or two (duals).

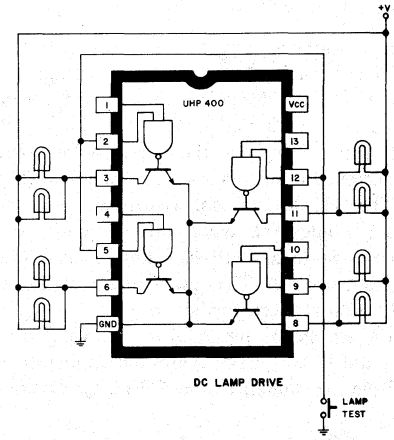


Figure 6A

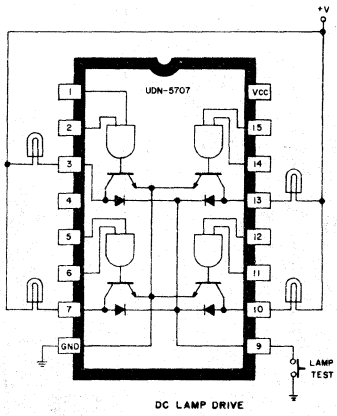


Figure 6B

Lamp Interface A-C (Half-Wave)

Two potential configurations for operating the lamp driver from an a-c source using only half wave rectification are given in Figure 7A and 7B. Either of the two diode configurations is permissable and choice largely depends upon whether a common ground exists in the system.

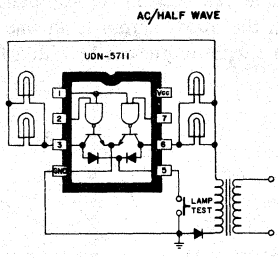


Figure 7A

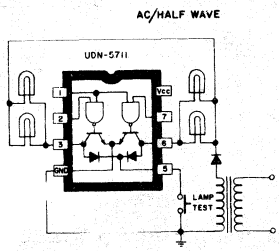


Figure 7B

Light output will be reduced somewhat when run in a half-wave mode, as will the filament temperature. It should still suffice for most ambient conditions excepting, specifically, sunlight.

An element of caution should be observed when operating from an a-c source rather than a d-c supply. The inductance of the transformer may produce voltage transients beyond the device breakdown level, particularly when all lamps are switched OFF simultaneously. Use of such items as back-to-back Zener diodes for clamping, a General Electric MOV*, or sufficient capacitance across the supply to prevent the transients will solve the problem. The capacitance required would be a function of the total lamp current, but it should not be necessary to achieve any appreciable degree of filtering.

Preventing these inductive transients through use of zero-crossing devices would be another more complex solution.

Lamp Interface A-C (Full-Wave)

Inexpensive bridge rectifiers allow the approach shown in Figure 8 and will provide greater lamp brightness than the half-wave counterpart. In either case, the simplicity of lamp drive without the need for well filtered regulated power supplies is apparent. Again, the same cautions pertaining to the transformer inductance mentioned in the half-wave a-c section apply for full-wave rectification.

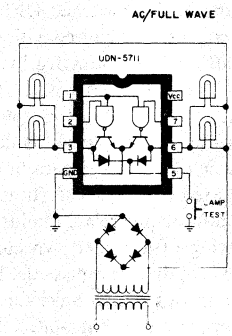


Figure 8

Solenoid/Relay Interface

The use of the integral suppression diodes originated in the Sprague Electric UHP-400/500 series of relay drivers is shown in Figure 9. The newer UDN-

*Trademark

5700M dual and UDN-5700A quad peripheral/power drivers all include high-current/high-voltage transient (flyback) diodes for use with inductive loads. The obvious advantage is the reduction in component count, board space, and assembly costs that result when choosing a Sprague Electric relay driver over a non-diode protected type.

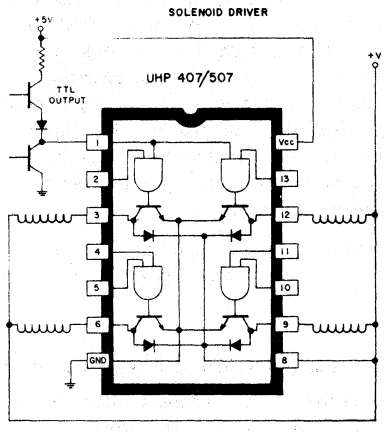


Figure 9

$V_{CEX(sus)}$ Curve

Operating inductive loads requires that any semiconductor sustain a combination of output voltage and current as the load is switched OFF; a combination of voltage/current not required with non-inductive loads. The collapse of the inductive load produces a very non-linear "looping" load line. It is desirable that it not intersect the device output breakdown curve. The phantom of secondary breakdown creates device failures when the voltage/current (power) combines with an excessive interval (time). Secondary breakdown is a power/time related failure mechanism, but the intersecting of a breakdown curve by an inductive load line is at times permissable. It is, however, definitely advantageous not to have such an intersection (crossing) occur during turn-off.

Figure 10 shows a typical $V_{CEX(sus)}$ curve obtained with the Series UDN-3600 or UDN-5700 IC drivers. In accordance with the V_{CC} notation, this curve is obtained with the supply equal to or greater than +4.75 volts. Inductive load lines vary greatly with load current and voltage and are difficult to include. The load line of a solenoid or relay may be obtained by properly connecting an oscilloscope to monitor load current and voltage while repetitively switching the coil. Use of a current probe to monitor load current (vertical input) while applying the voltage waveform to a calibrated horizontal input will display the load line.

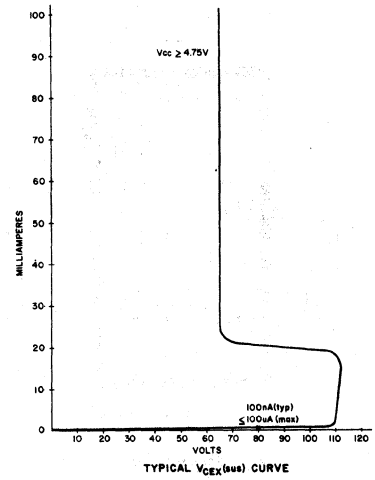


Figure 10

Paralleling Outputs

Due to the excellent matching provided by monolithic IC processing and identical output transistor designs, it is possible to parallel output/input combinations to allow higher current sinking as systems necessitate. All four outputs may be paralleled with results like those shown in Figure 11 for 2, 3, or 4 drivers in parallel. Current sharing is extremely well matched, and the best choice for pairing would be outputs on the quads across from one another (i.e., output pin 3 with output pin 11 with a UHP-400).

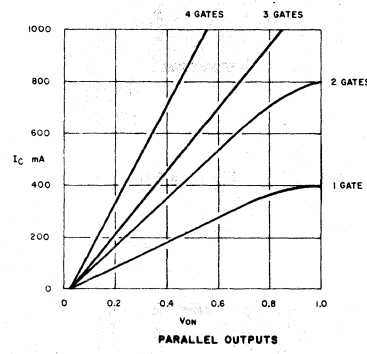


Figure 11

Logic Gate Power

The high gain transistor process used at Sprague Electric has resulted in a considerable decrease in the power dissipated in the logic gate which sources base current for the output NPN. The collector resistor in the TTL totem pole output is the determining component for the high current output. It is this resistor

in each of the gates which has a principal influence on the power when the output is switched on (supply current/output low). Figure 12A compares the Competitor A or B logic output (130 ohm resistor) to the Sprague types (228 ohm resistor). It is this 228 ohm resistor value in Figure 12B that decreases package power substantially.

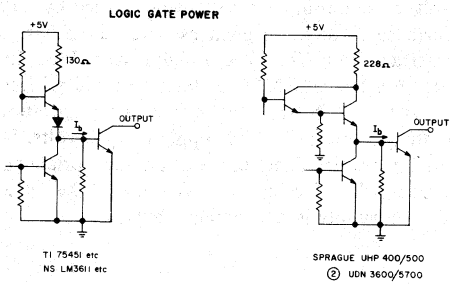


Figure 12A **Figure 12B**

The histograms of Figures 13A and 13B compare the dual drivers furnished by Sprague, Competitor A and Competitor B. Note that the output ON currents of Competitive A and B circuits are either identical or very similar but that both are considerably higher than the Sprague equivalents. A small discrepancy exists between the output OFF currents, but these are of much less consideration than the output ON supply current. The Sprague devices offer an obvious advantage of less heat and lower current supplies while providing the same functional capability for interface to peripheral loads. Reductions in power (heat) can appreciably affect some system considerations (largely power supplies) and/or improve reliability via lower operating temperatures.

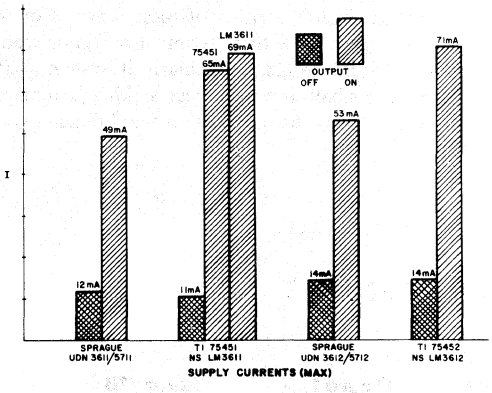


Figure 13A

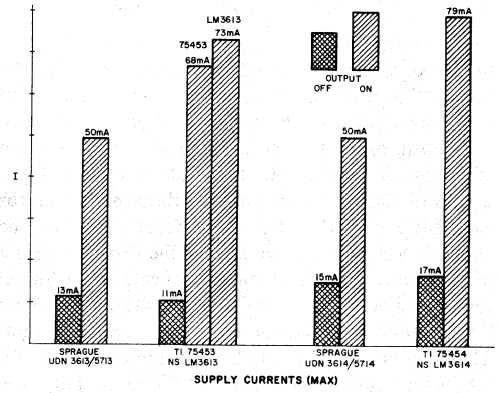


Figure 13B

Logic "0" Input Current – DTL Types

The reversion to a DTL logic gate with an allowable input logic level of up to 30 volts brings new dimensions to the applications for the newer dual and quad power drivers. TTL circuits are difficult to use in systems that have logic "1" input levels beyond the 5.5 volt TTL maximum specified; but even more difficult to handle with many MOS devices is the maximum logic "0" current of 1.6 mA for UDN-7400 TTL. Figure 14 compares the Sprague DTL 100 μA maximum types to the much higher (1.6 mA max) levels of the Competitor A and B types.

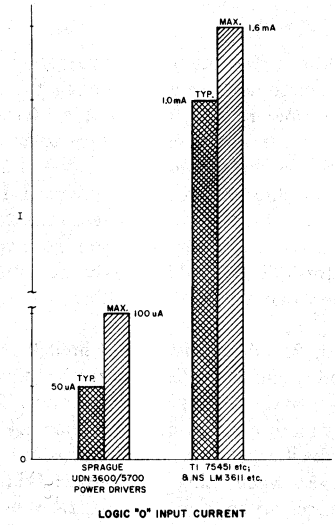


Figure 14

PMOS Interface – DTL Types

The combination of an allowable input voltage of up to 30 volts and the 100 μA input current for the logic "0" state opens up new areas of simple, minimum component interface with both PMOS and CMOS. The open drain PMOS of Figure 15A shows the technique for employing the UDN-5707 or UDN-5712 with only an appropriate pulldown resistor for each MOS output and a series Zener to obtain the +5 volt V_{CC} for the logic gate of the driver. The use of a high voltage input diode (collector/base diode) results in a vertical PNP to the substrate and accounts for the dramatic reduction in logic "0" input current. The input is actually a PNP, and the current (≤100 μA) being sunk in the driving device or pulldown resistor is the base current of the PNP shown in Figure 15B. The main element of the logic "0" input current (I_E) is shunted to the substrate (ground) as PNP collector current (I_C); – another Sprague first in peripheral/power drivers.

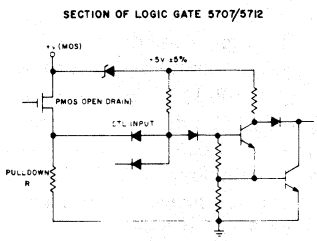


Figure 15A

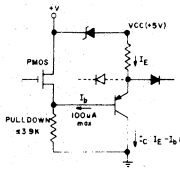


Figure 15B

Pulldown resistors for this type of application fall within reasonable values, although the same is not true of standard TTL inputs with a 1.6 mA input current limit. It would be necessary to use a 250 ohm pulldown with standard TTL (0.4 ÷ 1.6 mA = 250 ohm), but the 100 μA of the Sprague DTL units will allow up to 4 kΩ. Even if this need for a 250 ohm pulldown is overcome, the maximum input voltage of 5.5 volts for TTL precludes its easy use with most MOS circuitry operating above 5 volts.

Most PMOS circuits have a limited output source capability and a problem results when the PMOS output is turned on. To properly operate a TTL or DTL IC, its input must swing higher than 2.4 V; a serious difficulty if a 250 ohm pulldown resistor is used (TTL). However, when using the Sprague DTL types, it is only necessary to source 615 μA (2.4 V ÷ 3900 ohms), and should present little, if any, problem for most PMOS interface.

With the exception of the probable need for a pulldown resistor (may not be required with some depletion load PMOS), the same basic considerations apply to CMOS interface.

CMOS Interface – DTL Types

The much lower input logic "0" current and the 30 volt minimum input breakdown afforded by a collector/base diode are a great asset for those wishing to interface from CMOS to a high current load. In Figure 16 a typical CMOS to relay/solenoid scheme employs the UDN-5712 dual driver; a configuration operating from the CMOS supply of +12 volts. Use of a simple series Zener diode of an appropriate current rating will suffice for the V_{CC} line if the +12 volt CMOS supply is adequately regulated.

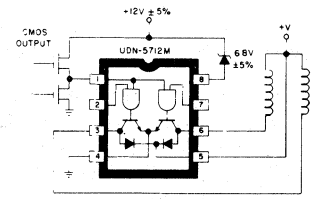


Figure 16

Systems with poor regulation may require a simple regulator such as those shown in Figure 17A (NPN power transistor) or Figure 17B (power Darlington) to obtain the +5 volt V_{CC} line. The choice is based upon the input current required for the series pass power device, and the effects upon the Zener power rating under minimum load conditions (obvious advantage to Darlington). For CMOS logic systems requiring relatively few peripheral/power drivers for high current interface either of these schemes or the use of an appropriate three terminal regulator would simplify system design, particularly if system +5 V currents are small and little heat sinking is required for the pass transistor or three terminal regulator.

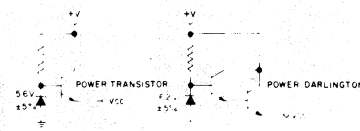


Figure 17A Figure 17B

Extending Output Sink Current – DTL Types

The high current output NPN of all the Sprague peripheral power drivers will operate beyond the 250 mA guaranteed level (Series UHP-400 and UHP-500) or the 300 mA rating of the newer DTL types (Series UDN-3600 and UDN-5700). The newer units are better suited to use above standard output current ratings, an improvement largely related to improvements in the output NPN design. Extending the 300 mA capability requires additional base current and consequently, the V_{CC} line must be raised above the nominal 5 volts. In Figure 18A, the increased minimum output current is plotted against the increased V_{CC}. Alternatively, it can be viewed as a maximum increase in V_{CC} to obtain additional sink current capability.

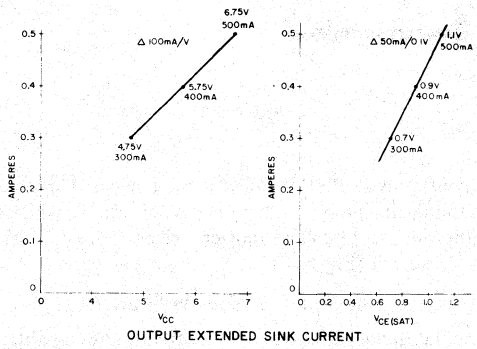


Figure 18A

Figure 18B

Figure 18B indicates the maximum $V_{CE(sat)}$ changes as the current is increased from 300 mA to 500 mA. This information is necessary for calculations of package power dissipation if the system duty cycle presents questions of average power.

Figure 19A and 19B present information relating to the increased logic gate supply currents as a function of the increased V_{CC} required for extending output currents. Figure 19A is for the dual types and presents the information on both a per package change (Δ 16 mA/V) and a per gate maximum. The maximum increase is presented for both I_{CC} "1" and I_{CC} "0" and the most significant is the I_{CC} "0" which is indicated in each figure on both a per package and per gate basis. The change in I_{CC} "1" is small (≤ 1.5 mA/gate) and, to prevent confusion, is shown per package for the dual only and per gate only in the quad graph. Increase in I_{CC} "1" in quad types is 4X the per gate maximum (4 X 1.5 mA, or 6 mA/package per volt).

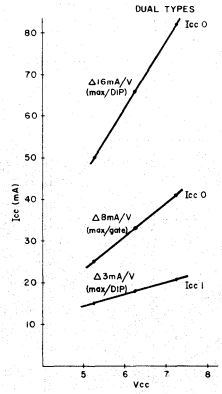


Figure 19A

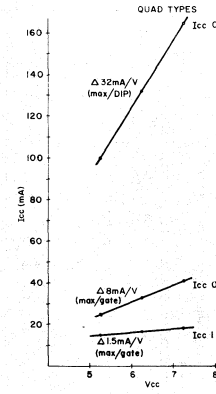


Figure 19B

Vcc vs Icc

Package Dissipation – Mini-DIPs

The θja rating of Sprague dual drivers in a mini-DIP is +80°C/W, while the Competitor B specifications list all dual mini-DIPs at +110°C/W. Similar ratings apply to other suppliers and the advantage is to any type using copper alloy lead frames.

The allowable average power, low at +70°C, is definitely in favor of the Sprague DIPs. Contrast this 1.0 W maximum from Figure 20 (+80°C/W curve intersects 1.0 W at +70°C) with a 727 mW limit calculated from the +100°C/W ratings listed by Competitor B (both limits are derived using max. junction limit of +150°C and manufacturers θja rating). A worst case analysis will reveal that the electrical specifications of competitive parts produce power levels for 100% duty cycle applications that may result in junction temperatures above the +150°C level if both outputs are simultaneously and continuously sinking 300 mA with V_{CC} at 5.25 V. The LM 3611 max. power (per spec) could reach 782 mW (LM 3612, etc, slightly higher) and the 75451 maximum is 761 mW (75452, etc. slightly higher).

The Sprague UDN-3611 or UDN-5711 will have a worst-case power (same conditions of V_{CC} and I_C) of only 677 mW and is also manufactured in a DIP package capable of sustaining 1.0 W rather than the 727 mW limit. A clear advantage for lower junction temperatures, less heat, and/or greater output capability in a system. Maximum junction temperatures obtained would be: LM 3611 with 782 mW ≃ 156°C; 75451 with 761 mW ≃ 153°C; and the Sprague UDN-3611/5711 with 677 mW ≃ 124°C.

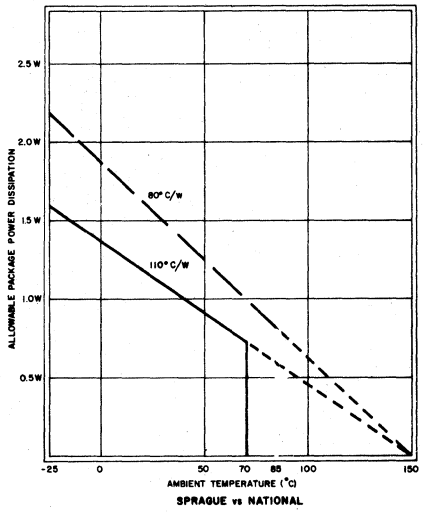


Figure 20

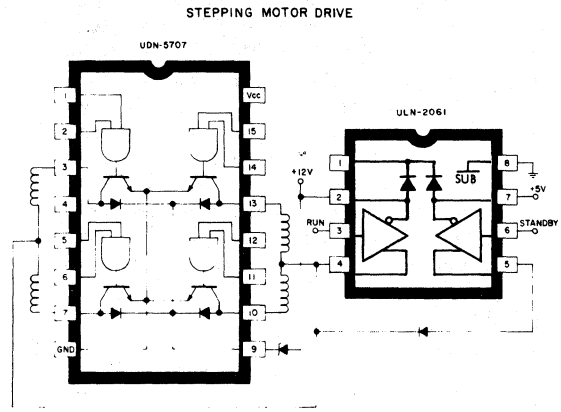


Figure 21

Stepping Motor Applications

Combining the use of a peripheral/power driver and a dual Darlington switch (Type ULN-2061) provides a capability of driving a 4-phase bifilar stepping motor. Motors designed to operate with voltages and currents compatible with these ICs may be driven with a minimum of components. In Figure 21, the signals from appropriate logic/sequencing circuitry operate a Sprague UHP-407 or UDN-5707 (may also be done with two UDN-5712 devices) for switching the motor coils selected. The transient suppression diodes are utilized in accordance with solenoid/relay applications, although here they are connected through a Zener diode to the supply voltage. The Zener will improve the speed of the switching, but should be chosen such that the maximum voltage across the output (+V added to V_Z) is below the device breakdown. Permitting voltage excursions of this sort produces improved high speed motor operation, but must be clamped to a safe value.

Application requiring a holding or detent current may employ a dual Darlington (ULN-2061). One Darlington switch is used for the RUN mode, while the second (lower) half of the ULN-2061 is used to provide a lower holding current to maintain the position of the motor. Use of two supplies is shown and diode D1 decouples the power supplies and prevents unwanted reverse bias from reaching the STANDBY Darlington. Similar schemes may be employed to obtain bipolar drive schemes for high-speed stepping motor applications. Current is sourced from the positive supply (a PNP switched by a gate capable of sustaining the supply voltage is one example), while an appropriate peripheral/power driver is used to sink coil current (Figure 21).

Control 100 Watts With an IC

The quad peripheral power drivers are capable of controlling or switching loads that total 100 W/package (50 watts for duals). Load currents beyond the standard 250 mA level (UHP-500) or 300 mA (UDN-5700A) would result in the capability of switching loads in excess of the 100 watt capability with standard specifications.

The UHP-500 series has a 100 volt/250 mA capability for each of four outputs: 100 V x .25 A x 4 outputs = 100 watts of control.

The UDN-3600 and UDN-5700 quad drivers offer an 80 volt/300 mA combination for each of four outputs: 80 volts x 0.3 A x 4 outputs = 96 watts.

All of these high-current/high-voltage peripheral/power drivers offer simple, inexpensive interface solutions to some tough load requirements. Those applitions beyond the output voltage and/or current handling limits of lower current, TTL type devices are easily handled with these devices. The newer DTL types provide solutions to interface problems associated with PMOS and CMOS that are quite often impossible with TTL type units. The "giant step backward" actually results in a "stride forward" with the newer DTL peripheral/power drivers.

Completely Monolithic IC Series for Gas Discharge Display Interface

Introduction

The switching of the high voltages necessary for display panels such as the Burroughs Panaplex® has long presented difficulties to the semiconductor industry – particularly to IC manufacturers. It is difficult to fabricate devices capable of sustaining 200 volts or greater with standard IC processes of today. Solutions to the high voltage gas discharge display interface also must be inexpensive as well as functional; this cost/simplicity factor prohibits most unusual or exotic circuit designs and/or IC processes.

The earliest (and a great many recent) gas discharge interface schemes used discrete components, but that has been an increasingly cumbersome and expensive solution. Competition at the system level has largely come from LEDs, and a great many standard ICs are available for the smaller LEDs. In most instances, the small displays have gone to LEDs. However, the larger display applications are still an opportunity for gas discharge since character size and cost are not directly related. The cost impact upon the potential for gas discharge displays in many systems is a function of interface complexity and cost, and it was to this end that a joint Sprague/Burroughs effort was launched.

Early Sprague/Burroughs meetings were held to define the relevant factors involved in such a program and provide the necessary insight for both parties into the capabilities of diode isolated ICs, the voltage and current requirements of the Panaplex displays, the need for minimization of power (battery systems), packaging of the circuits, component count and cost, etc. Add to this the potential for use with feedback controlled supplied, poorly regulated d-c supplies, the wide variety of numbers of display digits, the range of digit sizes (in use or contemplated), etc., and our task was not to be an easy one.

Our direction was determined by two factors: a history of fabricating 130-140 volt PN diode isolated display circuits, and a more recent effort to utilize compatible thin-film resistor technology. These factors, coupled with considerable expertise in designing and processing high voltage ICs, dictated an approach utilizing a split (± 100 V) supply. The split supply would provide the 200 volts needed to ionize the display and the resistor capability would greatly aid the incorporation of functions previously done by discrete components – including both input and output (segment) current limiting, pulldown (open drain PMOS), pullup and pulldown reference for IC outputs, and a high impedance voltage divider for the output OFF bias. All level shifting is accomplished via use of PNP or NPN transistors, and the capacitors previously required were negated.

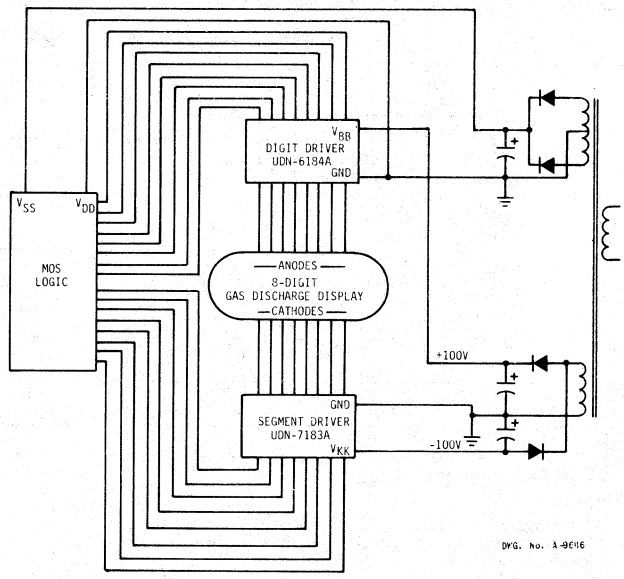


Figure 1

APPLICATIONS INFORMATION (Cont'd)

Basic Scheme

Replacing discrete components through incorporating their function into this IC series results in the block diagram of Figure 1 with its basic requirement for a single digit and single segment driver; a scheme capable of driving as many as eight digits and the eight segments. Additional digits or segments beyond the eight provided in an 18-lead DIP may be driven by combinations of packages beyond the minimum two necessary. Example: three ICs — two digit and one segment — will fulfill the needs of a 12 to 16 digit calculator.

Included in this series of high voltage interface are three digit driver packages: UDN-6144 (4-digit), UDN-6164 (6-digit), and UDN-6184 (8-digit). Segment drivers include the UDN-7180, UDN-7183, UDN-7184, and UDN-7186, and the four offer current ranges compatible with display sizes from 0.250″ to 1″ panels, and others will be made available as needs are defined.

Digit Interface

The digit driver is the more complex of the two and its schematic is shown in Figure 2. Input address polarity is positive (active high in TTL parlance) and the circuit is designed to interface from TTL (4.5 volts from open collector — or using pull-up to V_{CC}), CMOS, PMOS, etc. Input current-limiting and one-half of the pull-down for open drain PMOS is the function of R_5; R_6 adds the second half of the pull-down to the ground buss. The protective value of R_4 and R_5 must be noted; a junction failure in Q_1 has the two resistors as a current limiter to the MOS (or TTL) output and will minimize the likelihood of destroying the low level logic outputs.

Input transistor Q_4 is a high voltage inverter and sinks the base current of PNP Q_3. The current sink Q_5, R_8, D_2, and D_3 is common to all stages and serves to both minimize power (influence of battery applications) and to maintain PNP base current sufficient for saturating the output Darlington while being independent of power supply variations.

A positive input (4.5 to 20 V) will turn on Q_4 and this base current (65 μA typ.) for PNP Q_3 will turn on the output Darlington (Q_1 and Q_2) and source digit current. The typical current of 65 μA is defined by the current sink Q_5, D_2, and D_3, and R_8 is to enhance battery life in portable (hand held) designs.

Resistor R_7 is the output pull-down connected to the off voltage buss from the pull-down shunt Q_6 and Q_7. Q_6 and Q_7 are needed to shunt the current in a pull-down resistor to ground and prevent excessive shifts in the level developed by the voltage divider R_{10} and R_{11}. This voltage divider sets up an ON to

ELECTRICAL CHARACTERISTICS: T_A = +25°C, V_{KK} = −110 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Test Fig.	UDN-7180/83A Min.	Typ.	Max.	UDN-7184A Min.	Typ.	Max.	UDN-7186A Min.	Typ.	Max.	Units
Output ON Voltage	V_{ON}	All inputs at 6 V*	1	−100	−104	–	−98	−102	–	−97	−100	–	V
UDN-7183/84/86A		All inputs at 6 V*, V_{KK} = −70 V	1	–	−66	–	–	−65	–	–	−63	–	V
Output ON Voltage UDN-7180A	V_{ON}	All inputs at 6 V*, I_{ON} = 14 mA		−105	−108	–	–	–	–	–	–	–	V
Output OFF Voltage	V_{OFF}	All inputs at 0.5 V, Reference V_{KK}	2	76	84	–	76	84	–	76	84	–	V
Output Current ($I_{LIMITING}$)	I_{ON}	All inputs at 15 V, V_{KK} = −110 V, Test output held at −60 V	3A	UDN-7183A only 1475	1850	2450	910	1140	1520	440	550	725	μA
Output Current (I_{SENSE})	I_{ON}	All inputs at 0.5 V, V_{KK} = −110 V, Test output held at −66 V	3B	−95	−120	−155	−65	−85	−115	−50	−65	−90	μA
Input High Current	I_{IH}	Test input at 15 V, Other inputs at 0 V	4	–	200	275	–	200	275	–	200	275	μA
Input Low Current	I_{IL}	Test input at 0.5 V, One input at 6 V*, Other inputs at 0.5 V	5	–	1	10	–	1	10	–	1	10	μA
Supply Current	I_{KK}	All inputs at 0 V	6	–	125	175	–	125	175	–	125	175	μA

*Specify input voltage = 4.5 V for devices with "-5" suffix.

NOTES:

1. All voltage measurements are referenced to pin 9 unless otherwise specified.
2. All voltage measurements made with 10MΩ, DVM or VTVM.
3. Recommended V_{KK} operating range: −85 to −110 V.

PARTIAL SCHEMATIC

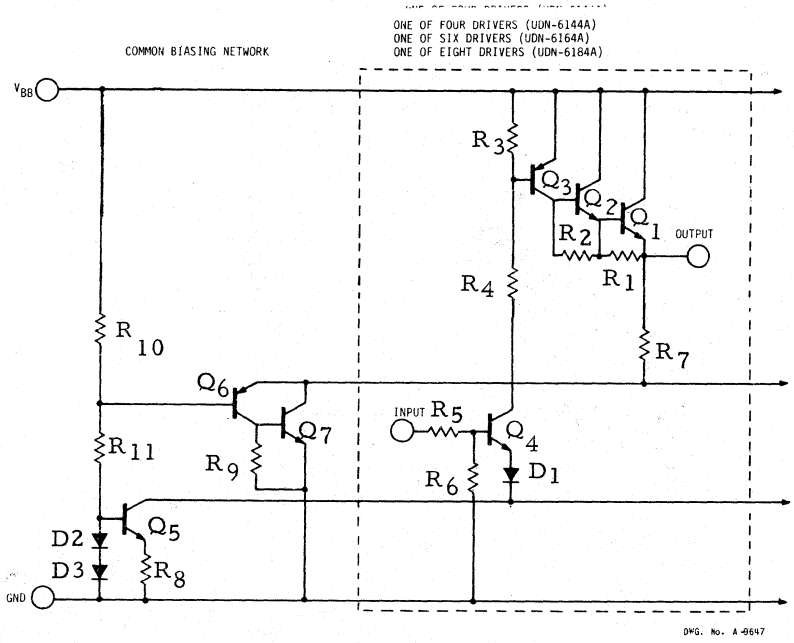


Figure 2

OFF voltage swing of approximately 2/3 the difference between V_{BB} and ground. This adequate swing prevents problems associated with past attempts at 'direct MOS drive' — problems quite frequently the result of inadequate voltage swings available from the PMOS LSI.

Consistent ionization and extinguishing of the display panel is the result of the 60-75 volt swings available from both digit and segment ICs. The conditions that previously created problems for the 'direct MOS drive' with minimal swings at the output have been very adequately handled with the increased output swings of the 6100/7100 series. Problems from leading zero blanking, low temperature, low ambient light, etc. which previously gave difficulty are well taken care of with this series of ICs.

The 'housekeeping' current resulting from the very high impedance voltage divider (typ. $R_9 + R_{10} = 1.3$ MΩ) is low, and aids the use of these ICs in battery or low power applications.

Segment Interface

The segment driver circuit is shown in Figure 3 and the value of R_2 (segment limiting) is determined via masking for the appropriate display current. Its counterpart pull-up resistor R_1 is also changed to some known ratio of R_2. The ground terminal (#9) is referenced near, or connected directly to ground, and the V_{KK} line is typically a -90 to -100 volts.

The input PNP (Q_1) serves as a level translator and provides d-c level shifting to the output Darlington (Q_2 and Q_3). Emitter resistor (R_3) both limits the input current and furnished pull-down for open drain PMOS. An added intent is the measure of protection furnished the MOS by the very high impedance of R_3.

The basic switching function is the combination of PNP Q_1, Darlington Q_2 and Q_3, and the associated resistors R_1, R_2, and R_3. Address polarity is again active high. The input may be raised a maximum of 20 volts above ground and will function with input levels obtained from CMOS and open collector TTL (4.5 V).

PARTIAL SCHEMATIC

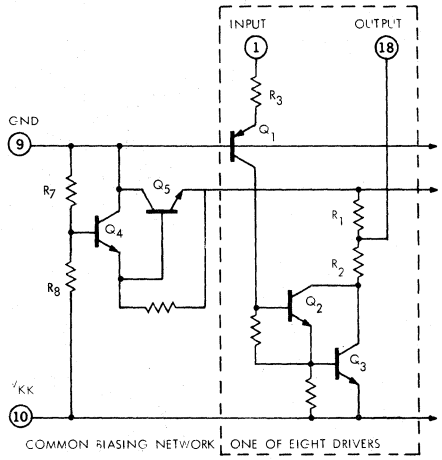


Figure 3

TYPICAL APPLICATION

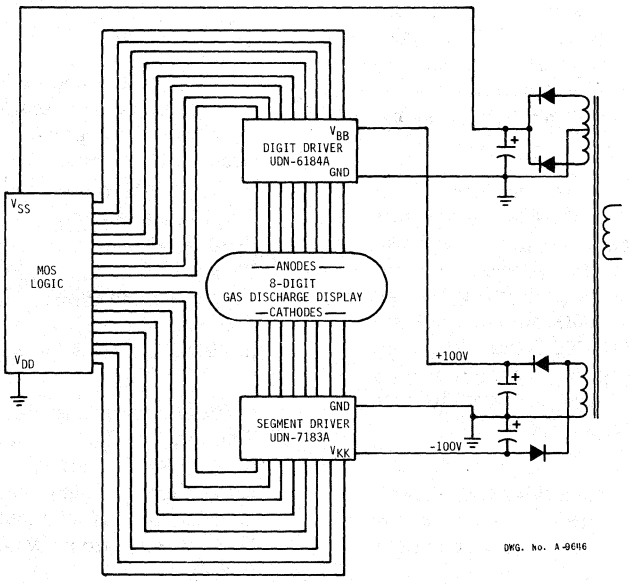


Figure 4

The OFF output biasing network is common to all the individual drivers with the level of bias determined by the ratio of R_7 to the total of R_7 and R_8. As in the digit driver, the value of output bias is ≈2/3 the voltage across V_{KK} and ground — thus insuring sufficient 'on to off' swings to properly fire, and effectively extinguish unaddressed segments during a scan. Emitter follower Q_4 and Q_5 sources current to the pull-up buss connected to the various outputs as they are turned on during the display scan.

Minimum Component Interface

The impact of this new product family may be seen in the typical digital clock of Figure 5. This a-c powered clock uses a Mostek 50250 clock IC, a UDN-6164 digit driver, and a UDN-7183 segment driver. Total component count is approximately 30 pieces, and the board layout is straightforward and uses single-sided board.

Many calculator interface schemes use considerable numbers of components (70 to 100 typically) to drive gas discharge panels. As one example: a twelve digit/eight segment machine uses 85-90 discretes while the new IC version uses only three packages, and results in less space along with considerable simplification. Other applications will benefit similarly with this series of circuits.

Summary

Display technology and usage has emerged at a mind boggling rate in the past several years — largely due to the fantastic growth rate of calculators. The planar gas panels have been an integral portion of this burgeoning market, but like all the other displays

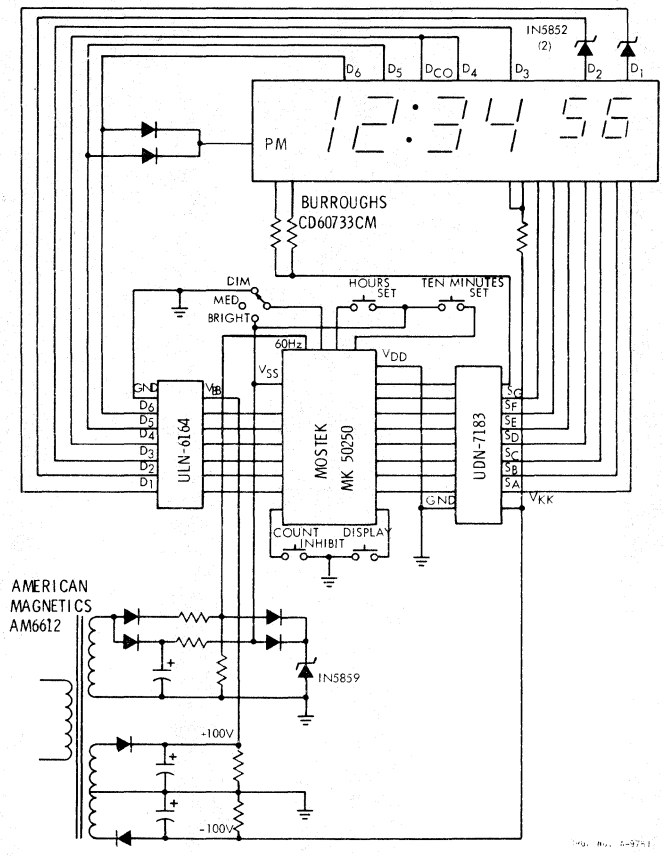


Figure 5

available does not meet the requirements for an ideal display.

Gas discharge panels are a fine combination of aesthetics, reliability, low cost, large character size, multiplexing capability, etc., but have been impacted to some degree by the lack of an available and inexpensive, totally monolithic interface. The move toward IC interface for displays has stifled some potential — largely in favor of LEDs; although many applications requiring large characters and/or in high ambient light turn toward gas panels. The planar gas discharge display is a long way from obscurity, and the availability of this family of ICs should open up new areas as well as satisfying existing systems.

The intent from the inception of this program has been to produce and provide a standard, inexpensive and easy to use interface for gas discharge displays. A great many potential applications exist for these circuits in consumer and commercial products. From the calculator and digital clock areas this product also will find use in automotive dashboards, point-of-sale systems, electronic cash registers and scales, and instrumentation. The market for displays is still very elastic, and many applications for gas discharge panels are continuing to appear. The Sprague contribution to this market is this series of state-of-the-art interface ICs.

Augmenting the μP LSI Revolution with New Power Interface for Peripheral Loads

Introduction

It is a foregone conclusion to now state that the microprocessor will have a profound effect upon the electronics world; we are already into another *revolutionary* era. Random logic LSI has had an enormous effect upon "component shrinkage" in computing and control systems, and even to "insiders" stretches the imagination. Although the μP is not yet a mature product, it has been and is being designed into a myriad of new products. In many instances, the systems have never previously utilized any semiconductors, while in a great many others the product (system) has never existed in any form. Functions which had previously been difficult or impossible to implement, particularly economically are rapidly surrendering to the onslaught of the μP, PLA, or custom LSI devices now available.

The revolution in control/calculation capability resulting from devices such as the μP and PLA is bringing about an increasing need for further evolution (with perhaps an occasional revolution) in many other areas. Systems are becoming smaller while also incorporating additional functions; becoming more reliable while becoming lower in price; more versatile while becoming more complex; and operating at higher speeds while also interfacing to electromechanical devices. Some of this represents a bit of a paradox (i.e. improved reliability at lower costs), but the dynamic nature of the semiconductor industry is continuing to bring about dissolution of old concepts of function, reliability, and cost.

At Sprague Electric an evolution of interface ICs is underway to provide answers for lower speed applications such as electromechanical peripheral loads and electronic displays. Few of the newer interface ICs at Sprague Electric are oriented toward "jellybean" IC markets, but rather are designed to displace discrete components in tough applications. Most of the activity is based upon high current or/and high voltage interface circuits and will extend our product leadership in these areas.

ULN-2064/2074 Quad Darlington

Originally this quad 1.5A (max.) Darlington was intended for interface to peripheral loads such as solenoids, relays, and small motors. By virtue of unsatisfied needs for high current buffers for LEDs, incandescent lamps, and other low voltage loads, additional systems applications continue to evolve. Multiplexed LED applications have arisen in which the strobed current was 1.0 to 1.4A, and the ULN-2064 or ULN-2074 has provided the only IC solution.

In Figures 1A, 1B and 1C, the basic Darlingtons are shown; a redesign effort has added other versions which will provide interface solutions for 5V CMOS with its very low current handling capability to 1.5A loads. The standard types in this series are guaranteed to sustain a 50 volt breakdown; although new part types are being added for breakdown selection to other limits, thus satisfying applications outside the normal 50V limit.

A version to allow interface directly from PMOS and 12V CMOS logic is being added; the ULN-2066 incorporates a higher input resistor than the ULN-2064 and limits the current from the MOS logic output to a value which allows use with many MOS ICs while simultaneously providing adequate input current for high current loads (Figure 1B).

The loading of the logic circuitry is of considerable concern and the V_{IN}/I_{IN} curves of Figure 2 and Figure 3 indicate the input limits over a range which corresponds to normal application. Figure 2 is for the ULN-2064/2074 versions with a nominal input resistor of 350Ω (increased from original value of 230Ω), and is designed to switch high currents when operated from "totem pole" TTL or LS TTL. For 5V CMOS ICs with limited source capability the ULN-2068 type (discussed later) should be a better choice, although the use of pull up resistors may be employed to satisfy the necessary input current for the load.

APPLICATIONS INFORMATION (Cont'd)

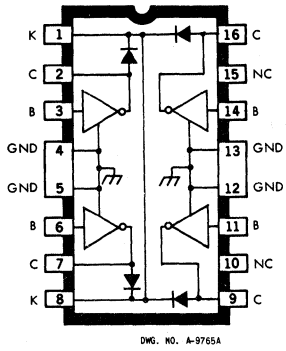
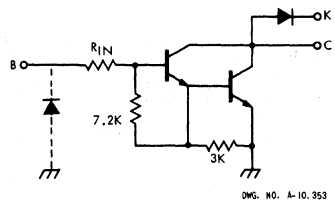


Figure 1A

PARTIAL SCHEMATIC



ULN-2064B, ULN-2065B } R_{IN} = 350Ω

ULN-2066B, ULN-2067B } R_{IN} = 3kΩ

Figure 1B

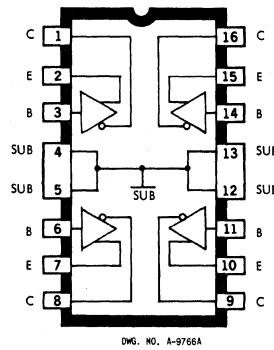


Figure 1C

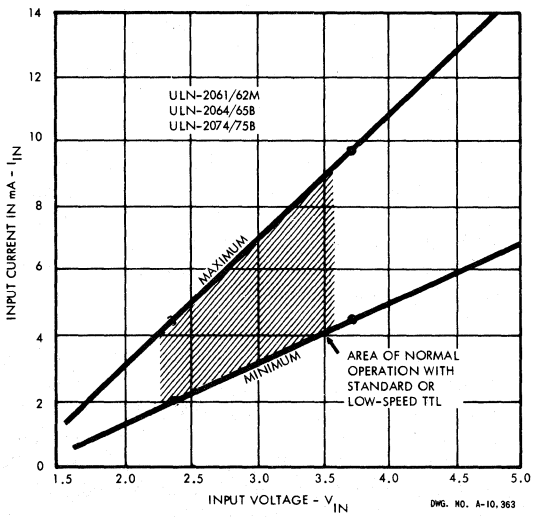


Figure 2

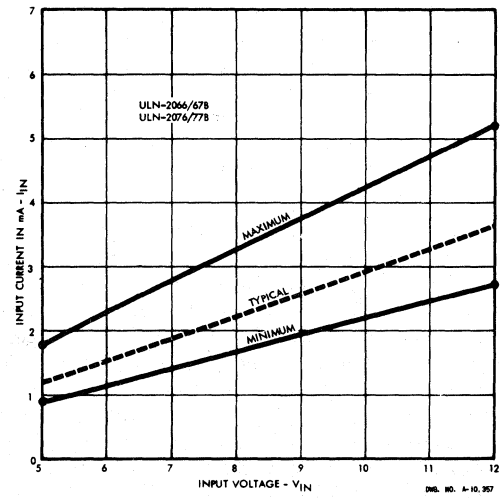
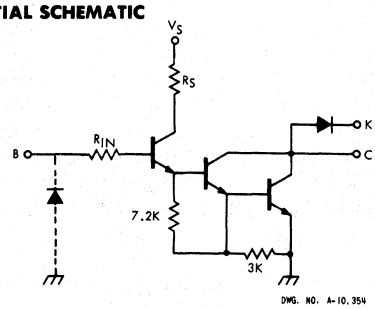


Figure 3

Figure 3 is the input current curve for the ULN-2066 and is intended for PMOS or CMOS applications. For MOS ICs which do not provide sufficient source output currents the use of the pull up resistors is required, or an alternative is the use of the ULN-2070 (another three stage buffer like the aforementioned ULN-2068 – shown in Figure 4).

The low current capabilities of many MOS devices necessitated further evolution which has resulted in adding a third NPN to these high current buffers. The intent is to provide a high current interface, which in some instances requires less than 100μA input current, while offering output capability to 1.5A. It is difficult to provide any graphical analysis of MOS interface,

PARTIAL SCHEMATIC



ULN-2068B, ULN-2069B } R_{IN} = 2.5kΩ, R_S = 900Ω

ULN-2070B, ULN-2071B } R_{IN} = 11.6kΩ, R_S = 3.4kΩ

Figure 4

particularly due to the vast range of MOS source capability, which ranges from less than 100μA to well above the milliamp level. While TTL specs are quite well defined, a useful approach to MOS applications is to use the worst case equivalent output Z for the particular device. Source outputs (CMOS and PMOS) are spec'd for given current and voltage conditions and a series circuit can be depicted much like Figure 5. Use the output voltage/current levels for the particular device to determine its suitability; $V_{ON} \div I_{OUT}$ = Output Z (max).

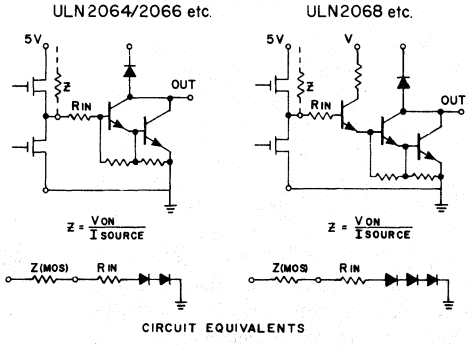


Figure 5

Determining the worst case (minimum) input current is necessary to assure that the output is well saturated. Although there is nonlinearity due chiefly to to beta rolloff, the graph of Figure 6 will insure the output sinking capability is matched to the input drive. The input current origin is skewed to compensate for the effects of the shunting resistors across the EB junction of the ULN-2064, ULN-2074, etc. types which do not incorporate the additional (third) NPN stage.

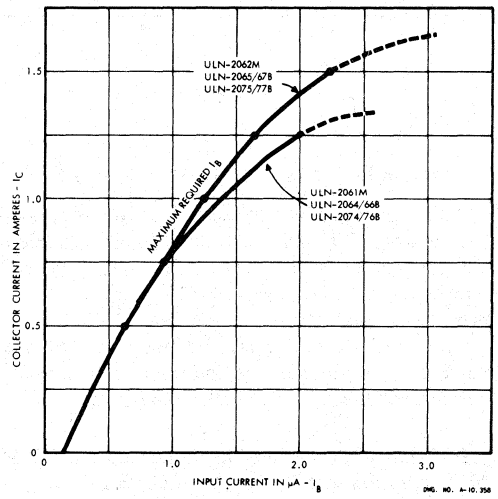


Figure 6

Allowable Power

An obvious concern with such high current ICs is the allowable combination of outputs ON, the output load current, and duty cycle. The "B" type of plastic DIP with its copper lead frame is used for this series and offers a thermal resistance (θja) adequate for many applications, and may be improved further through use of heat sinking.

In Figure 7, the plot of output current, number of outputs, and duty cycle for a +70°C ambient is shown. As in earlier, similar graphs it conveys:

(a) Allowable d-c current; intersection of the 100% duty cycle (i.e. ≃ 500 mA for 3 outputs simultaneously).
(b) Allowable duty cycle with a given output current.
(c) Allowable output current for a given duty cycle.

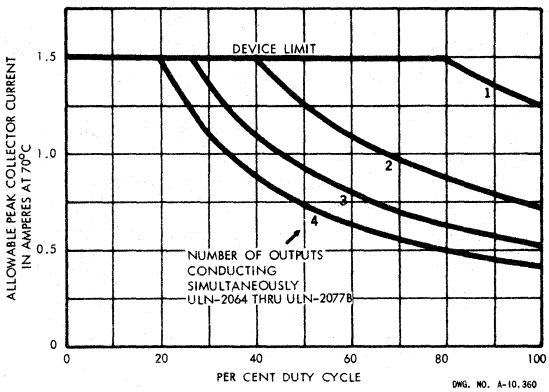


Figure 7

Input I – TTL and LS TTL (ULN-2064/74)

Although it is not well recognized, the outputs of "totem pole" TTL and Schottky TTL are capable of sourcing current well in excess of the 400μA (at 2.4V min logic "1") that is part of TTL specs. If it is not necessary to maintain the proper logic "1" level of 2.4 (or 2.7 volts) the output may be more heavily loaded via a lower impedance, and the result is higher input currents for the ULN-2064/2074 type of IC.

In Figure 8, the enclosed area indicates ULN-2064/2074 operation with TTL or LS TTL and the normal variations of Darlington input resistor value, logic

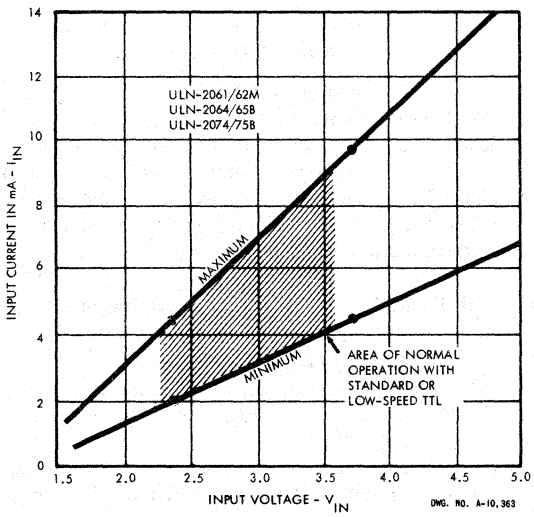


Figure 8

supply voltage, and TTL output level. This is useful information for designers operating with 7400 or 74LS families, but obviously cannot be guaranteed since we have no control over another vendor's devices. The minimum input current is extremely important for interface to high current loads, and the user can empirically corroborate the indicated I_{IN}/V_{IN} levels for TTL logic. I_{IN} corresponds to the I_{OUT} for the TTL; and V_{OUT} equates to the V_{OUT} logic "1," or V_{IN} for the Darlington.

Solenoid Drivers

A large portion of the ULN-2064 series ICs are for solenoid, relay, or motor interface. Use of the types with suppression diodes minimizes component count while allowing use with inductive loads as in Figure 9. The usual concern for power dissipation, input current, etc. should be exercised for these applications.

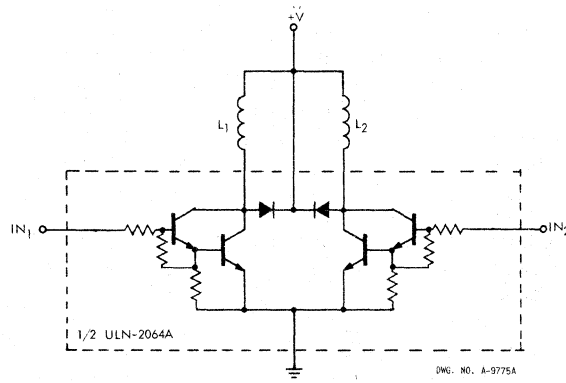


Figure 9

LED Interface

Figure 10 shows the ULN-2074 used as a source driver (digit driver) for common anode LEDS; this is a quasi-emitter-follower with the collector common being biased by the discrete diodes shown. Using such a scheme allows the base (input) to be pulled above the collector potential and provides a much better solution than a true emitter follower which is subject to the variables of gain, changes in load current, and the ranges of MOS output impedance.

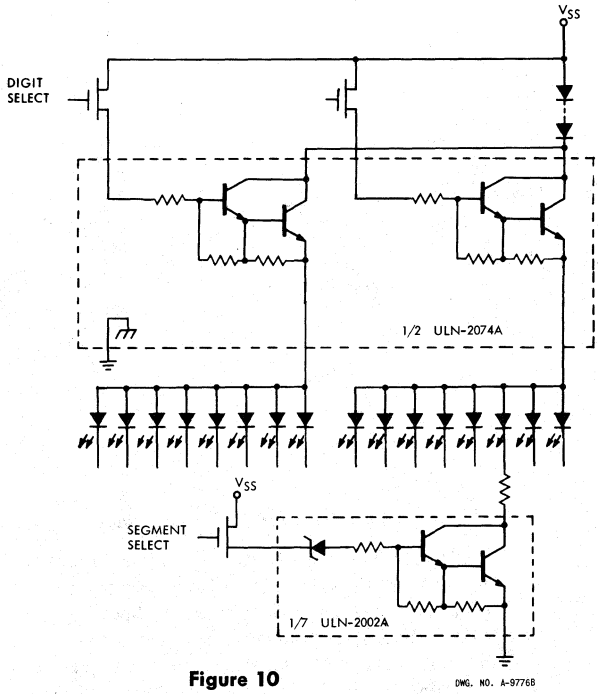


Figure 10

In Figure 11, the ULN-2064 series is again shown as a digit switch; here it is used as a sinking output with common cathode LEDs. Using such a combination allows an easy interface to high cursent, MUXed LED displays of large digit size, many digits, or low efficiency (green and amber types).

Sink/Source (Bridge) Circuit

The combination of a ULN-2068 high gain buffer and a ULN-2981 source driver offers a solution to bipolar (bridge) drive schemes. By paralleling inputs/outputs of the ULN-2981 IC driver it is possible to switch load currents of 1A with the basic configuration of Figure 12. While Figure 12 shows a 5V CMOS interface, the same prospects are available with PMOS, TTL, or DTL ICs.

Other potential solutions will be forthcoming with the introduction of the ULN-2840 series of drivers which may be used as source or sink drivers (a packaging configuration change).

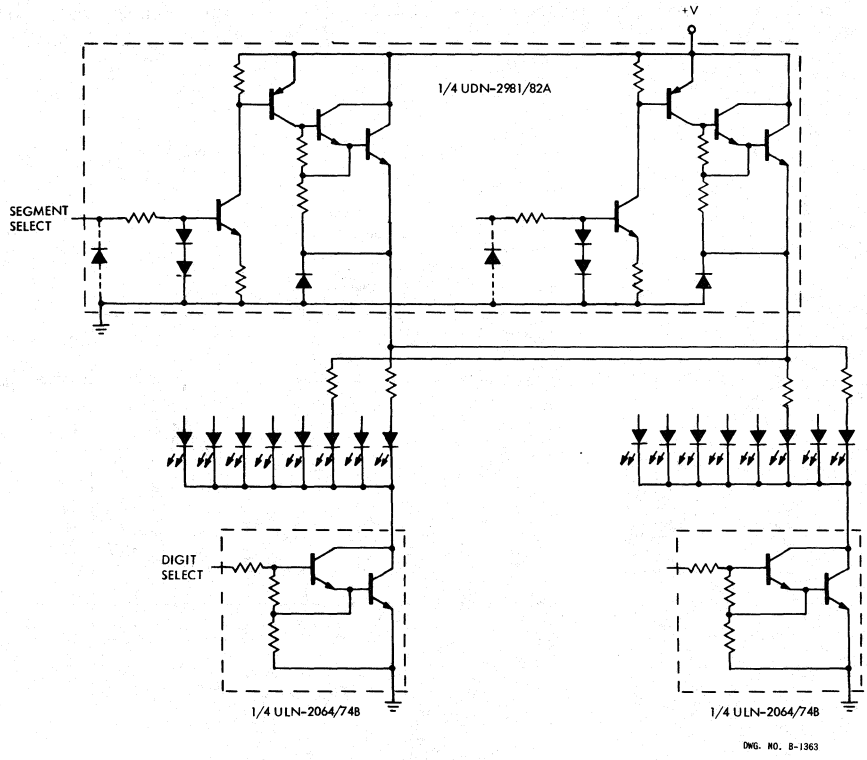


Figure 11

7

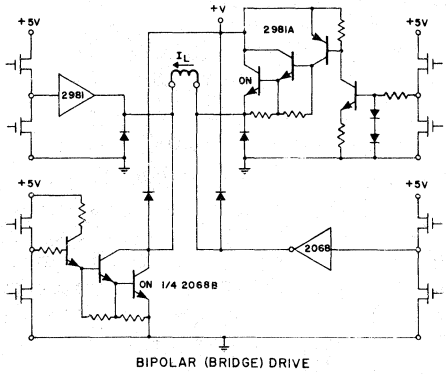


Figure 12

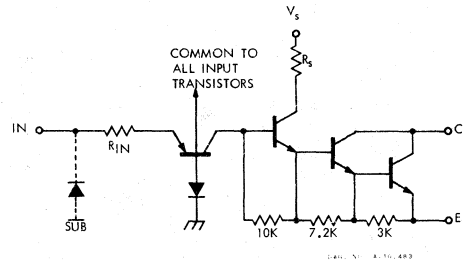


Figure 13

UDN-2840 Series (Figure 13)

The prospects for this circuit are not well defined as yet, but it will offer solutions to high current applications presently being done with discrete components. Through packaging options it will operate as either a source or sink driver, and will have the same basic electrical parameters (1.5A and 50V) as the ULN-2064 family.

UDN-2956/2957 Relay Drivers

Although chiefly intended as interface to telecommunications relays and similar loads, this source driver has additional areas of application. Shown (Figure 14) is the basic circuit which functions as a PNP driver, and utilizes the NPN stages to provide adequate current gain. The enable pin must be high ($\geq$5.0V for UDN-2956 and $\geq$2.4V for UDN-2957) for operation of the outputs; while a low or logic "0" on the enable pin inhibits all outputs.

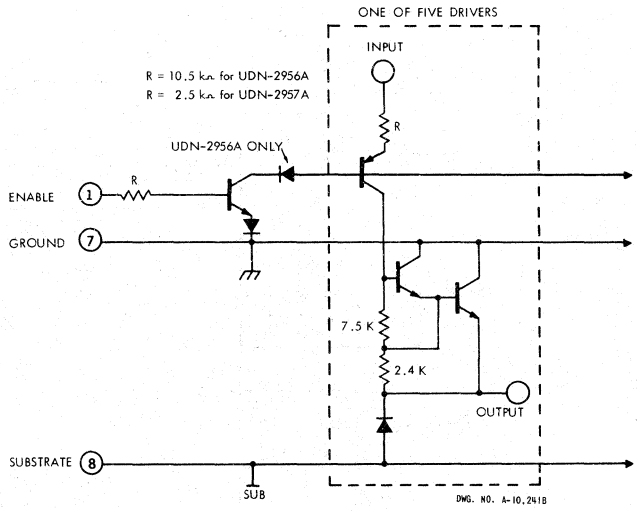


Figure 14

These source drivers are capable of switching currents to 500mA (max) and sustaining OFF voltages to a max of −80V. The UDN-2956 has input limiting designed for MOS applications, while the UDN-2957 is intended for TTL, LS TTL, and 5V CMOS applications.

The minimum TTL logic "1" level of 2.4V guarantees a source current of −100mA for the UDN-2957, and the output voltage will be less than −1.1V under these conditions. Similarly the UDN-2956 will source −100MA with an input potential of +6V and V_{ON} will not exceed −1.1V. Higher output currents are a function of increased input voltage and greater input currents.

An interface for common anode LEDs is shown in Figure 15; the UDN-2957 is shown as a digit driver operating with CMOS logic. In this configuration the DIP ground (pin 7) is connected to a positive supply to allow the IC to operate as a source to ground. A variety of Sprague Electric arrays are prospects for the segment side; these include the ULN-2031, ULN-2081, ULN-2003 or ULN-2004 types, all of which incorporate seven drivers per 16-lead DIP.

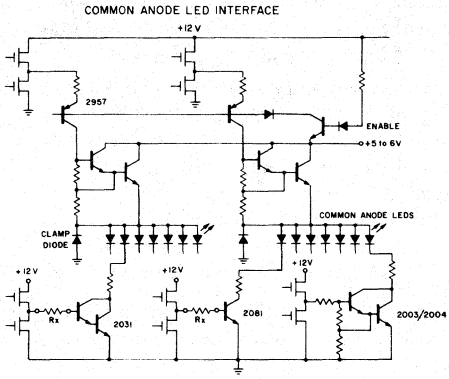


Figure 15

Another sourcing interface is shown in Figure 16; again the DIP ground pin is shifted to a positive supply for interface to a PIN diode. With open collector TTL or 12V CMOS the UDN-2957 will again serve as a source driver to ground. The output is pulled down in the OFF condition by R_P and the PIN diode forward current is limited by R_L.

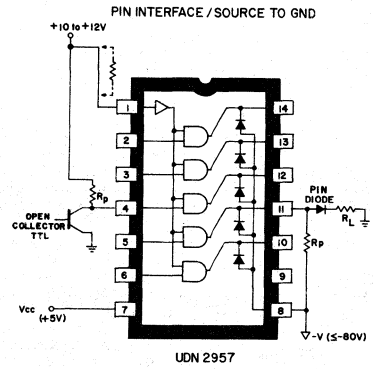


Figure 16

A similar prospect is the UDN-2957 sourcing from ground if the PIN diode supply is a proper negative voltage (−3 to −5 volts), the same pulldown to the −80 volt maximum applies. Military applications of the UDN-2956 or UDN-2957 drivers as PIN diode interface may be served by hermetic, 883 versions of these types.

Considerations for output current, duty cycle, and ambient temperature are shown in Figure 17. As is being done with other Sprague Electric power interface the allowable conditions of duty cycle, output current, and d-c operation are shown for various combinations of outputs activated. The curves of Figure 17 are for plastic DIPs (copper lead frame) for an ambient of +70°C.

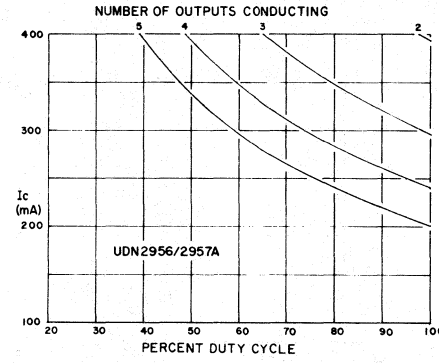


Figure 17

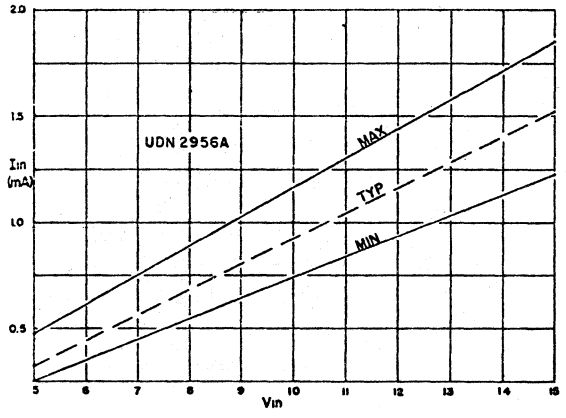


Figure 18

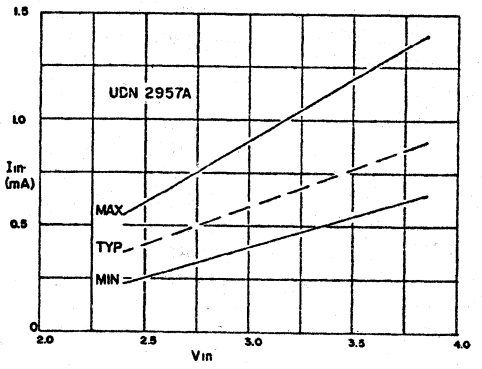


Figure 19

The loading of the logic outputs is shown in Figures 18 and 19. The UDN-2956 V_{IN}/I_{IN} curves are shown in Fig. 18; the same information for the UDN-2957A is indicated in Figure 19.

Use of the UDN-2957 with TTL or Schottky TTL (LS TTL) will produce input voltage (logic output "1") and input current (logic "1" output loading) limits as typified in Figure 20. It is not possible to guarantee other manufacturers' ICs, but the totem pole outputs of the 7400 and 74LS families will not be excessively loaded by the UDN-2957A. With the input Z of the UDN-2957 the minimum logic "1" level of 2.0 volts for TTL should be maintained without a need for additional pullup resistors.

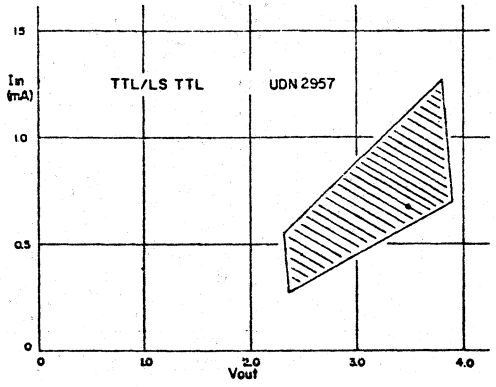


Figure 20

UDN-2980 Series Source Drivers

Customer inquiries for a source IC to complement our highly successful Series ULN-2000 Darlington Arrays have resulted in another high current device; the UDN-2980 series is an 8-channel array for general purpose high voltage/high current sourcing applications. Output loads range from LEDs, relays, solenoids, stepping motors, lamps, etc. which operate within the electrical limits of the device and the thermal limits of the package.

Two output voltage limits are available; +50V (min) for the UDN-2981 and UDN-2982, and +80V (min) for the UDN-2983 and UDN-2984. Outputs are spec'd for a recommended current of −350mA, while a maximum limit is −500mA per output. The UDN-2981 and UDN-2983 are intended for TTL, DTL, and 5V CMOS applications, and the UDN-2982 and UDN-2984 are for 12V CMOS or PMOS logic types.

Pin-out for the series is inputs opposite outputs, thus facilitating printed wiring board layouts and separating high voltage connections from lower levels wherever practical. As is the typical case with Sprague Electric interface the series incorporates transient protection diodes for inductive loads. Shown (Figure 21) is the pin-out of these 18-lead DIPs which utilize a copper alloy lead frame for improved thermal characteristics.

The schematic of Figure 22 shows the basic source circuit with an inductive load. To minimize power and allow use with a wide range of power supplies the high voltage input inverter uses a current sink. Of particular importance with such a device is power, since unwanted circuit power restricts output current and duty cycle combinations.

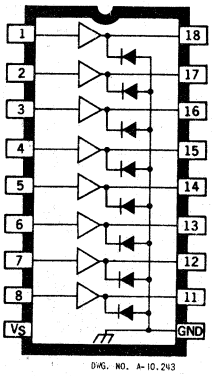


Figure 21

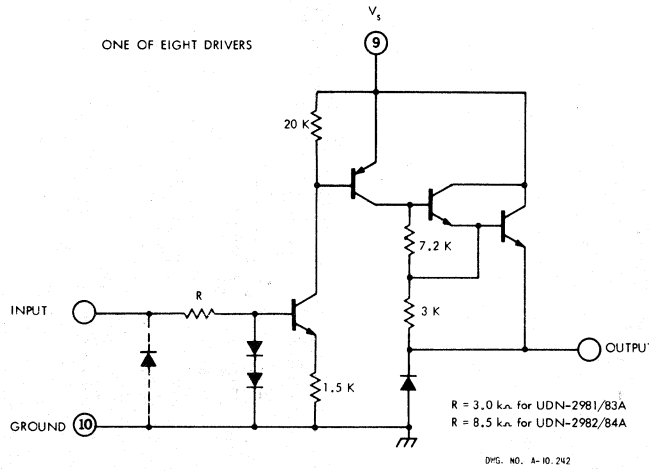


Figure 22

An advantage using the source driver for high current interface is a potential minimization of coupling of unwanted switching transients which affect circuit logic components. Poorly designed printed wiring boards or lengthy cabling may create difficulties with the high ground currents (and IR drops) when open collector circuits are used. Lamps are particularly strong offenders due to their severe inrush currents.

Separation of logic ground and load ground is possible with the UDN-2980 series, and IR drops or high transient currents are much less problemsome. IR drops in the wiring from the output will affect lamp intensity, and the ground side of the lamp may be well separated (physically) from the logic grounds. With open collector ICs high currents and microsecond switching speeds may combine to create "false" signals, but separating these at the power supply minimizes any potential difficulties (a UDN-2980 advantage).

In Figures 23 and 24 the UDN-2980 series is shown with MUXed LEDs; the configuration in Figure 23 is for common anode LEDs, and the UDN-2980 type is used as a digit driver. The arrays for the segment side of the display offer current sinking levels to a 350mA max (ULN-2003) with proper duty cycle and package power considerations. Since the 500mA maximum level of the UDN-2980 types is the digit current the **upper limit of source current is approximately 70mA without any duty cycle or V_s level concerns.**

Higher current applications may utilize the UDN-2980 series as a segment driver and the ULN-2064 type as a digit driver. With no duty cycle considerations the output current for all 8 channels is approximately —100mA at +70°C (assuming the +V supply is less than +15V). A 100mA segment current translates into 800mA digit current for the ULN-2064 driver. High currents are possible with duty cycles less than the d-c (100%) level which assumes all "eights" and no "blanking" intervals.

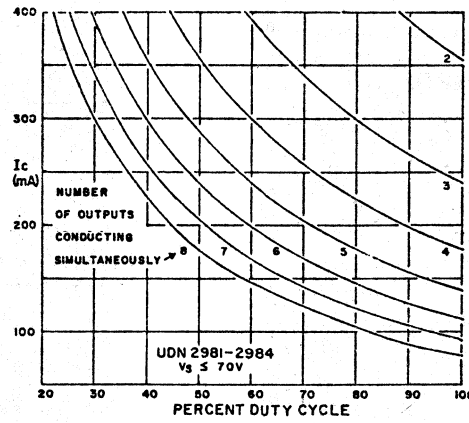


Figure 25

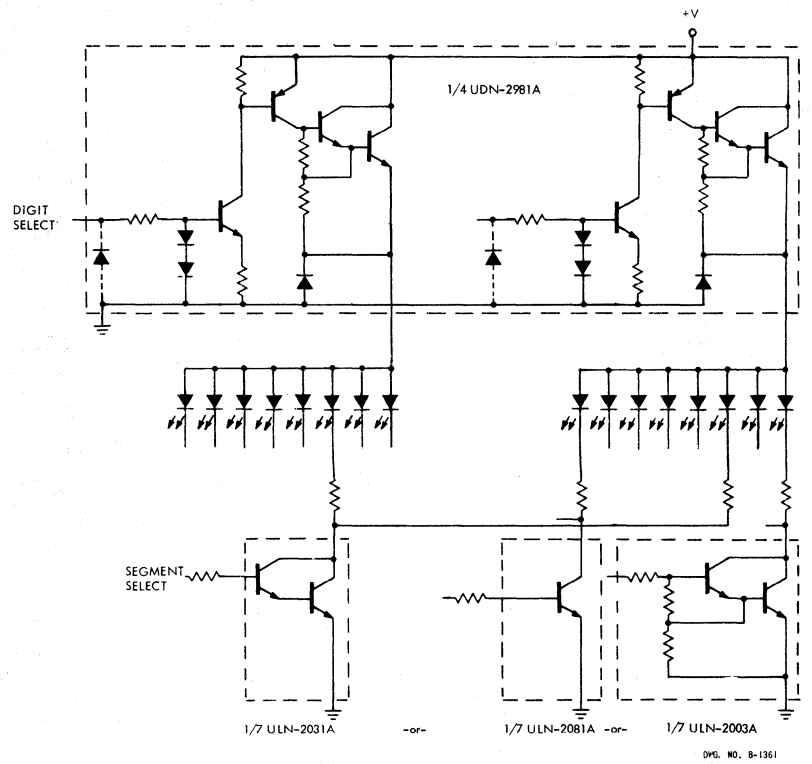


Figure 23

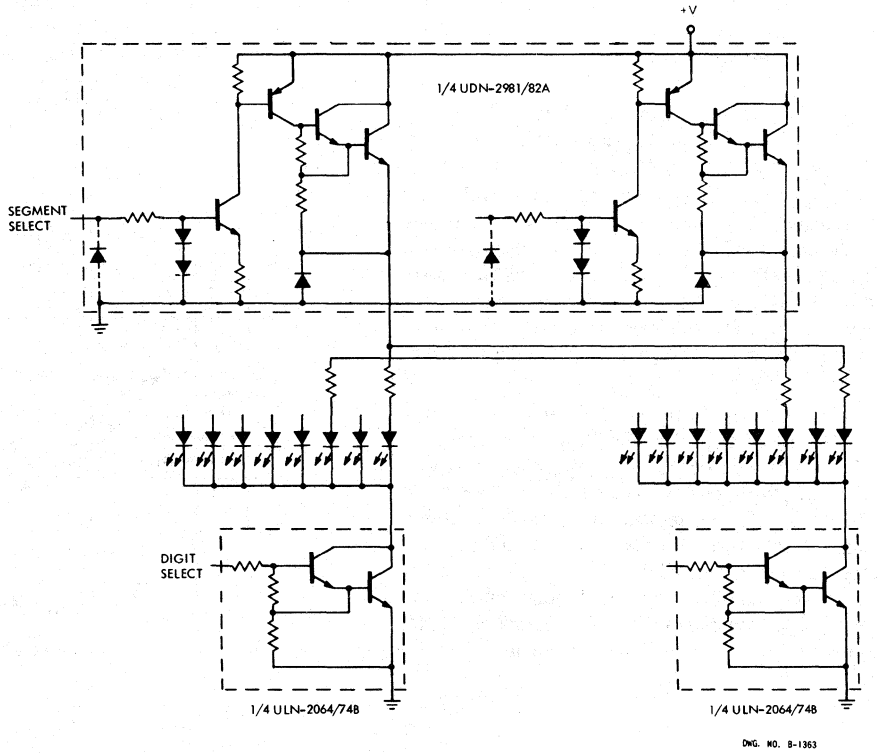


Figure 24

Power curves indicating allowable conditions for a +70°C ambient and $V_S \leq +70$ volts are shown in Figure 25. Operation at much lower supplies improves **the capability somewhat, since the max current from V_S affects the IC power. Lower voltages improve the allowable duty cycle or current limits somewhat, and if necessary should be included as a factor in calculating safe thermal operation.**

Hot wire (incandescent) readouts are driven in much the same manner as LEDs, except that MUXed (Figure 26) hot wire displays must incorporate diodes to prevent "sneak" series-parallel paths to unaddressed elements. It may be possible to use some transistor arrays (short collector to base) for the circuit diodes, but the maximum reverse voltage to the diode must not exceed 6 volts. Another consideration is current, and this limit (max base current) may have to be confirmed by the vendor.

Summary

With each new Sprague Electric interface IC has come an extension of the boundaries of simplifying many designs while also reducing component count and system cost. A great many complex MOS ICs must interface to the outside world and such designs are "self defeating" if they must incorporate large numbers of discrete components for peripheral loads and displays. Further evolution of Sprague Electric power and display interface will be keyed to the customer needs evolving from the growing μP revolution.

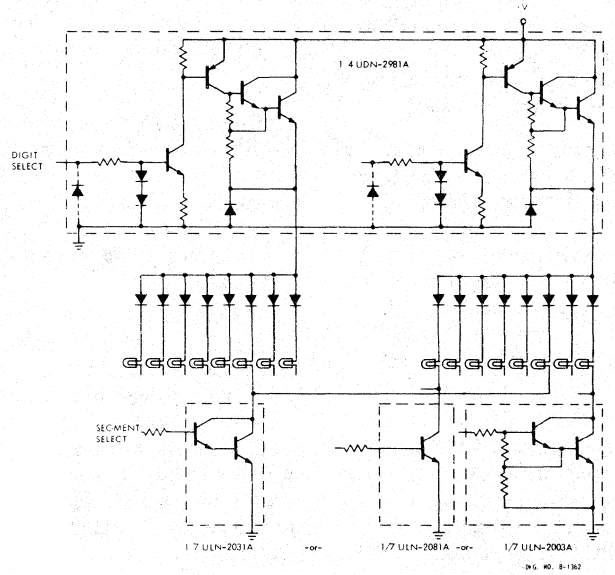


Figure 26

Series ULN-2000A Darlington Transistor Arrays — Description and Application

Introduction

The increased use of electronic circuits in systems formerly built with mechanical, electro-mechanical, or hydraulic components has resulted in systems becoming more precise, more reliable, generally less expensive, smaller, more efficient, and faster. Although the drive capabilities of monolithic integrated logic circuits are adequate for most information processing applications, there now exists a large and rapidly growing number of system applications where the current-carrying and/or voltage-sustaining capability of the integrated circuit logic is inadequate. Typically, these deficiencies arise when the logic must control such peripheral components as relays, solenoids, punches, stepping motors, and a variety of indicators (incandescent, LED, or gas discharge lamps and displays).

A very common solution to this output interface inadequacy has been the addition of discrete power transistors (or SCRs) and associated passive components to the logic output in order to obtain the necessary current and/or voltage capability. Although this provides a very satisfactory electrical solution, the large number of discrete components often required, high assembly labor costs, and space (packaging) limitations often mean additional problems and cost. A simple, and less expensive solution is the use of monolithic integrated circuits.

The Series ULN-2000A is comprised of five different high-voltage/high-current interface circuits. They are capable of controlling resistive, inductive, or tungsten filament loads of up to 125 watts and are compatible with all standard digital logic families (DTL, TTL, PMOS, and CMOS) without the need for additional discrete components.

High-Voltage and High-Current Capability

A large number of interface problems have been simplified by the Series ULN-2000A high-voltage, high-current Darlington transistor arrays. These devices are suitable for voltage, current, and gain levels beyond the limits of other monolithic buffers and arrays.

The five devices in the ULN-2000A series are all comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for use with inductive loads.

All devices have an output sink current capability of 500 mA although peak inrush currents to 600 mA are permissible, making them ideal for use with tungsten filament lamps. All of the outputs will sustain "OFF" voltages of at least 50 volts. Each individual Darlington circuit may therefore switch up to 25 watts (50 V at 500 mA).

A definite asset of monolithic device technology is the very fine match between adjacent outputs when used in parallel. Applications requiring a sink current beyond the capability of a single output can be accommodated by parallel outputs. Continuous operation of all outputs at the maximum rated current is not allowed because of power dissipation limitations imposed by the package. However, as illustrated in Figure 1, under certain conditions, the Series ULN-2000A Darlington arrays are capable of switching loads totaling more than 125 watts at an ambient temperature of +70°C.

High-Power Capability

A primary limitation of many interface circuits is the power dissipation of the device package. Until recently, very little concern was expressed for monolithic integrated circuit power dissipation. Improvements in silicon device technology have brought about a growing number of monolithic circuits capable of power considerably in excess of present package technology.

The Series ULN-2000A is supplied in a 16-pin dual in-line plastic package with a copper lead frame. Shown in Figure 2 is a comparison of the allowable package power dissipation for the industry standard iron-nickel alloy (Kovar) lead frame and the Sprague copper lead frame used on these devices. As shown, at an ambient temperature of +70°C, the Kovar lead frame allows only 0.64 watts while the copper lead frame allows 1.33 watts. At +25°C the copper lead frame permits a package power dissipation of 2.0 watts!

Actual power dissipation in any application for the Series ULN-2000A devices is the sum of the individual driver power dissipations. In turn, the individual driver dissipation is the product of the collector-emitter saturation voltage, the collector current, and the duty cycle. The collector-emitter saturation voltage is dependent on the collector current and, to a lesser extent, operating temperature.

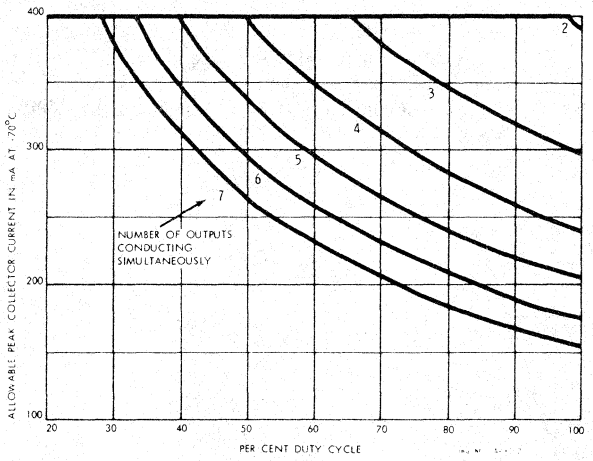


Figure 1

COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS

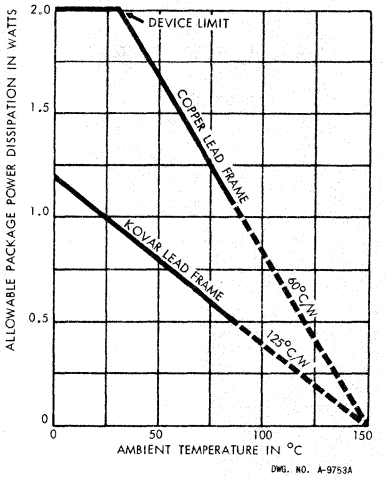


Figure 2

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

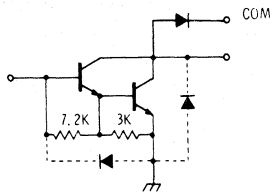
7

APPLICATIONS INFORMATION (Cont'd)

The Basic Darlington Array

The first, and basic array, in this series, is the Type ULN-2001A. This is a general-purpose version with input current limiting normally accomplished via the use of an appropriate discrete resistor connected in series with each input. It is also possible to utilize the intrinsic current limiting of many MOS outputs as shown in Figure 4; a typical P-channel characteristic.

The use of TTL in such a manner is not recommended due to the higher currents and resultant high level of package power dissipation. Outputs of most PMOS and CMOS circuits will not normally source currents of any significance due to their high source impedance.



(each driver)

Figure 3

TYPE ULN-2001A SCHEMATIC

14 to 25 Volts PMOS Applications

The Type ULN-2002A Darlington array was specifically designed for use with 14 to 25 volt PMOS devices. Each input has a 7 V Zener diode and a 10,500 ohm resistor (nominal values) to limit the input current to within the capability of most PMOS of the type specified. The basic circuit diagram is shown in Figure 5 with a typical application. Note that there are *no* pull-down resistors or other external discrete components necessary. The incorporation of the Zener diode also results in excellent noise immunity for this array.

TTL and CMOS INTERFACE

The ULN-2001A and ULN-2002A allow only a limited number of input options. Shown in Figure 6 is the basic circuit diagram of the Type ULN-2003A. This device has a series base input resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS logic operating at a supply voltage of 5 V (or 12 V CMOS using FET characteristics).

A guarantee of 200 mA output sink current capability (saturated) is provided with the worse case TTL logic *1* level of 2.4 volts. Low-power Schottky-clamped TTL logic is generally specified to have a minimum V_{OUT} of 2.7 volts. The ULN-2003A is guaranteed to sink 250 mA under this input condition. With the more typical input of 3 volts, the ULN-2003A Darlington pair will sink at least 300 mA in the "ON" state.

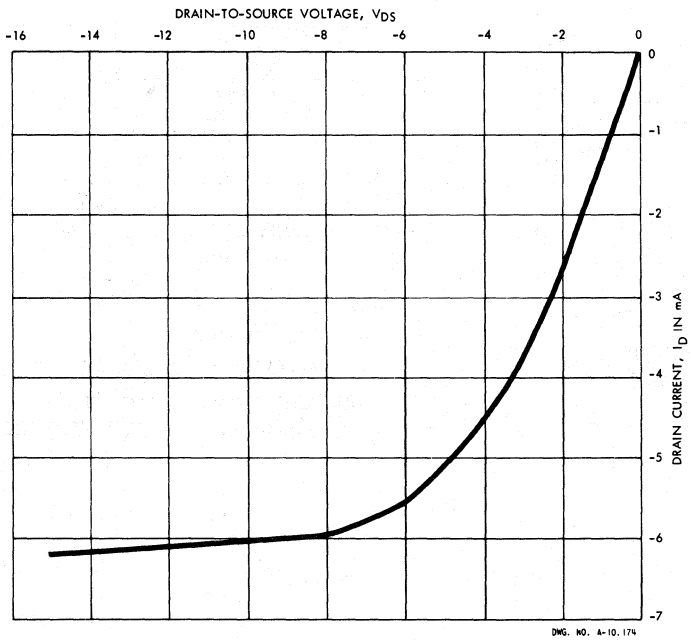


Figure 4

TYPICAL P-CHANNEL DRAIN CHARACTERISTIC

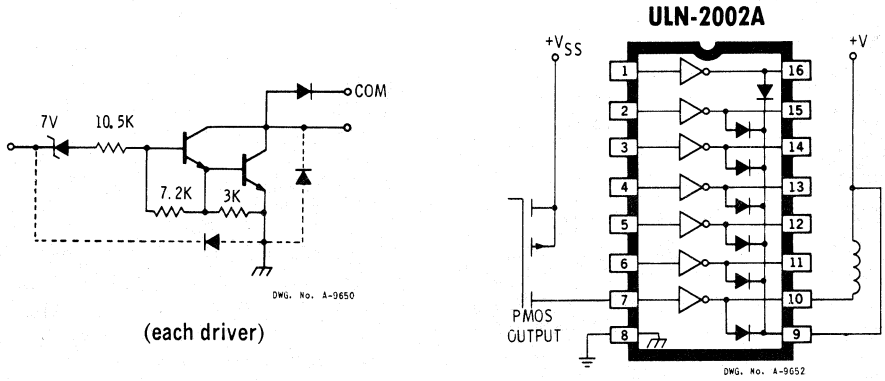


Figure 5

TYPE ULN-2002A SCHEMATIC AND APPLICATION

TTL totem pole outputs are not specified between the 400 μA logic *1* fanout condition and the maximum output short-circuit current (20 to 55 mA for the 7400 series). Between these rather wide limits lies the required ULN-2003A input current. The maximum Type ULN-2003A input current level is specified at 1.35 mA at the extrapolated TTL maximum logic *1* level of 3.85 V.

The ULN-2003A Darlington array will handle a great many interface needs – particularly those beyond the capabilities of TTL buffers. Also shown in Figure 6, is a typical application of the ULN-2003A Darlington array. Of particular interest in this application is an unusual use of the transient-suppression diodes for a non-inductive load. The lamp test feature can of course be used with any of the devices in this series.

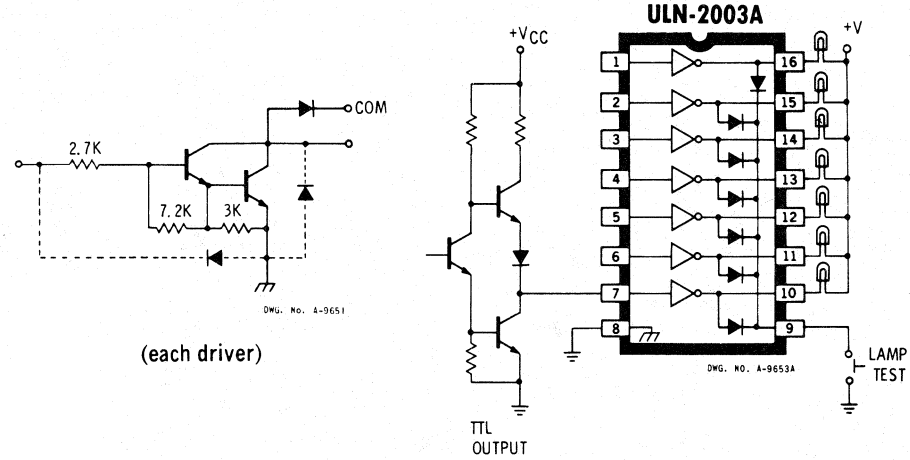


Figure 6

TYPE ULN-2003A SCHEMATIC AND APPLICATION

The diodes are designed to handle the same current and voltage as the output transistors. Switching can be accomplished through an ordinary switch or an appropriate power transistor. With the standard +70°C ambient and the most widely used lamps (2 No. 327 or 2 No. 387 lamps per output) there is no problem with continuous operation.

6 to 15 Volt CMOS or PMOS Applications

The Type ULN-2004A Darlington array has an appropriate series input resistor (nominally 10.5 k Ω) to allow its operation directly from CMOS or PMOS logic outputs utilizing supply voltages of between 6 and 15 V.

Shown in Figure 7 is a typical application of this array. Although the discrete output buffer could be used to increase the output capability of any of the devices in this series, this is most often done by paralleling outputs as was described earlier.

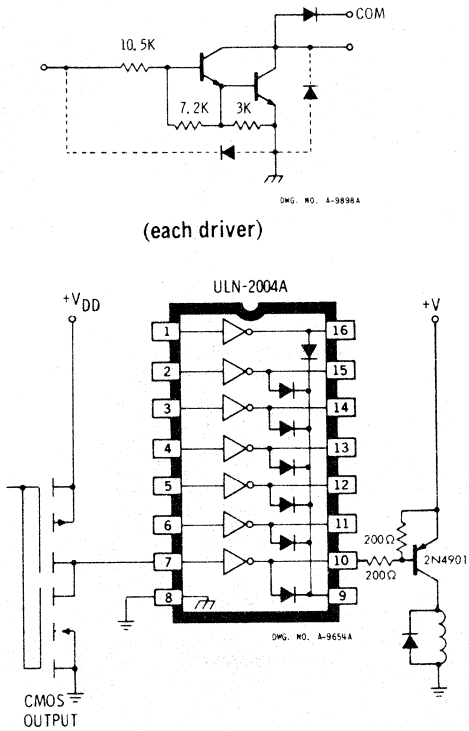


Figure 7
Type ULN-2004A SCHEMATIC AND APPLICATION

Input Current

The Darlington collector current (output in saturation) at an ambient temperature of +25°C, for any input current is the same for all four devices in this series and is shown in the graph of Figure 8. More accurately, the maximum input current for any collector current is described by the equation:

$$I_{IN(\mu A)} = I_{C(mA)} + 140\ \mu A$$

where I_{in} is the input current in microamperes, I_C is the collector current in milliamperes, and the figure 140 represents the maximum shunt current through the emitter-base resistors. The typical input current can be described as:

$$I_{IN(\mu A)} = 0.58\ I_{C(mA)} + 110\ \mu A$$

where the figure 0.58 is an adjustment for the typical Darlington current gain and the figure 110 represents the typical shunt current.

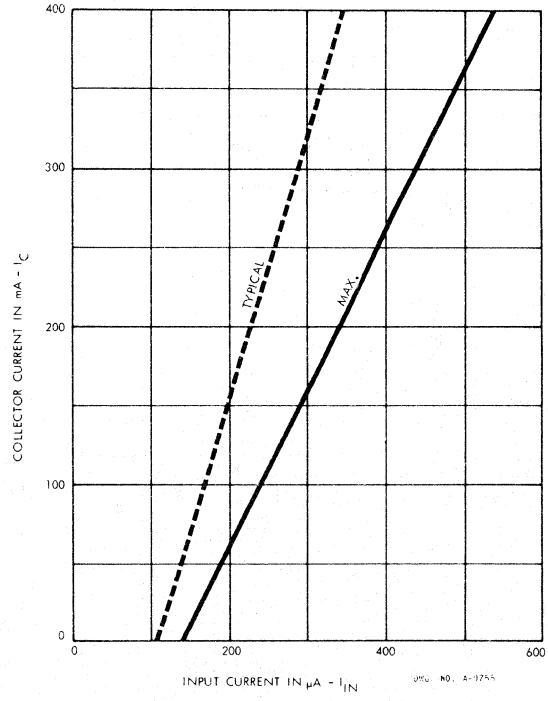


Figure 8
COLLECTOR CURRENT
AS A FUNCTION OF INPUT CURRENT

The input current as a function of input voltage is shown in Figure 9 for the ULN-2002A, ULN-2003A, and the ULN-2004A. The Type ULN-2001A Darlington array is not shown since input current is more a function of the external circuitry. Systems utilizing either CMOS or PMOS logic should be evaluated for intrinsic current limiting as was shown in Figure 4.

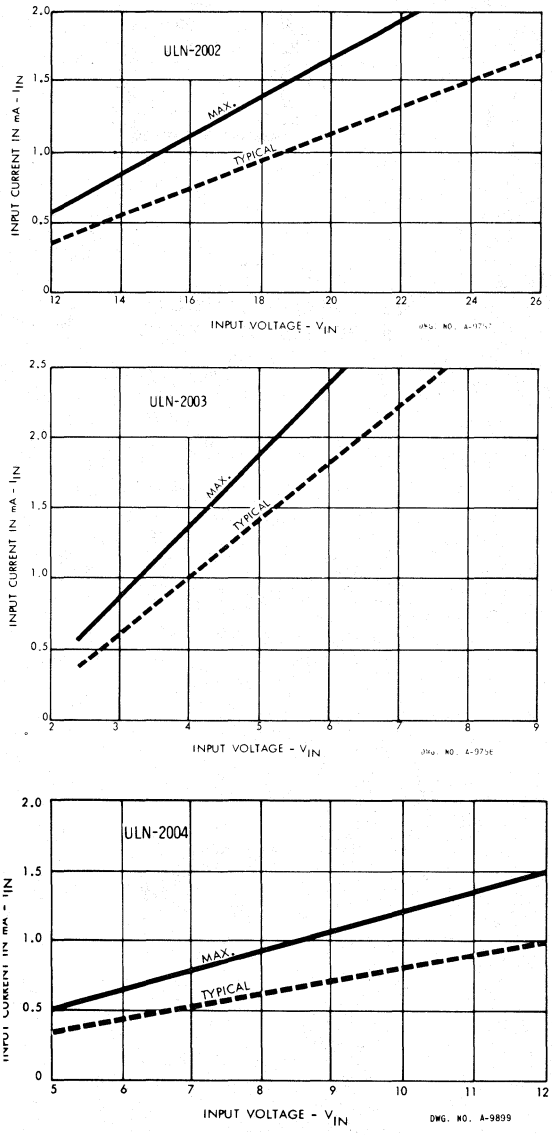


Figure 9
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

Low Available Drive Current Operation

Occasionally, applications featuring minimum available input drive current and a high output load current have shown the Type ULN-2003A and ULN-2004A Darlington arrays to be inadequate for the particular requirement under worst case conditions. This usually results from the restricted drive current available from a TTL or CMOS gate operating from a nominal supply of 5 volts.

Under worst case conditions with a low logic *1* voltage (2.4 V), and a high input resistor value (3.51 kΩ), the available load current is reduced to only 145 mA. Compounding this problem would be the effect that a high drive current requirement would have on the logic output voltage since that is normally specified at only 400 μA. If the gate output is connected to additional logic elements, a minimum logic *1* voltage of 2.0 V must be maintained and at that level the worst case Darlington load current would be reduced to only 31 mA!

A simple solution to this problem is through the use of inexpensive pull-up resistors as shown in Figure 10. The minimum resistor value is determined by the maximum allowable sink current (16 mA for TTL, 360μ A for CMOS), the minimum logic *0* output voltage, and the maximum supply voltage as per the following equation:

$$R_P \geq \frac{V_S - V_{OUT(0)}}{I_{OUT}}$$

For standard TTL, the minimum value for R_P is about 316 Ω with values between 3000 Ω and 5000 Ω being used customarily. Multiple pull-up resistors in a single in-line package are shown in Sprague Engineering Bulletin No. 7041; resistors in a dual in-line package are shown in Bulletin No. 7042.

Conclusion

Since the Series ULN-2000A high-voltage, high-current Darlington transistor arrays are quite conservatively designed, the basic product is fully capable of being ordered to higher voltages and/or higher currents than the standard specifications. Presently, parts are available to withstand up to 95 volts on the output. Parts with this higher voltage rating would create a potential for switching loads far in excess of 125 watts! Aside from the higher power handling capability, the higher voltage rating is required for driving plasma or gas-discharge displays.

APPLICATIONS INFORMATION (Cont'd)

Although not intended for high power applications, there is also available a Series ULS-2000H with hermetic sealing and an operating temperature range to +125°C. These parts are recommended for military and aerospace applications as well as commercial and industrial control applications where severe environments may be encountered.

All of these Darlington transistor arrays offer a common solution to a great many interface needs. The minimal component count and straightforward printed wiring board layout offer benefits in cost reduction, simplicity of board layout, and savings in space. Other benefits are a reduction in insertion costs, and lower handling and inventory costs than other alternatives. Cost benefits from some of these factors are not very tangible. However, fewer components, less complex boards, etc. usually result in lower system manufacturing costs.

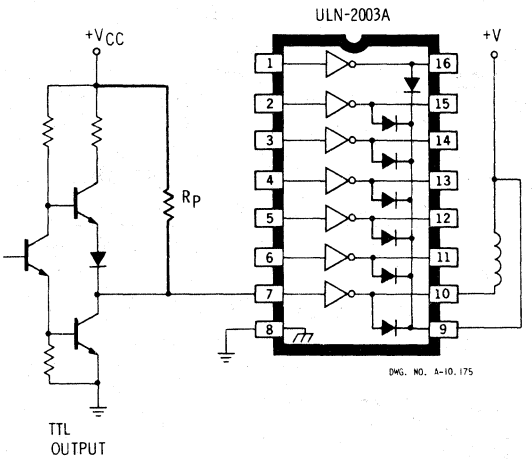


Figure 10
USE OF PULL-UP RESISTORS TO INCREASE DRIVE CURRENT

Computing IC Temperature Rise

Heat is the enemy of integrated circuits—particularly power devices. Here's how to use thermal ratings to determine safe IC operation.

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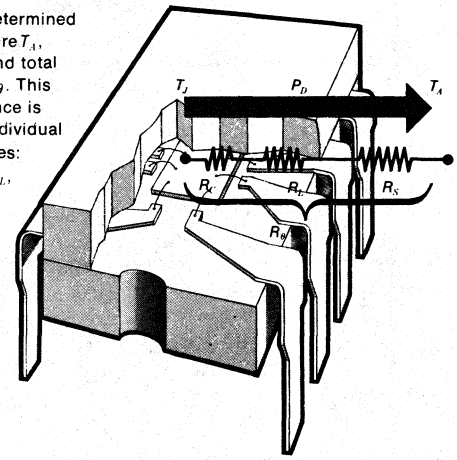
Why IC Temperatures Rise

IC temperature T_J is determined by ambient temperature T_A, heat dissipated P_D, and total thermal resistance R_θ. This total thermal resistance is comprised of three individual component resistances: chip R_C, lead frame R_L, and heat sink R_S.



EXCESSIVE heat shortens the life of an IC and reduces its operating capability. Until recently, ICs were capable of operating only in low-power applications requiring perhaps a few milliwatts of power. But now, new ICs handle several hundred milliamperes and drive devices such as relays, solenoids, stepping motors, and incandescent lamps. These high power levels may increase IC temperatures substantially and are capable of destroying devices unless appropriate precautions are taken.

Thermal Characteristics

The thermal characteristics of any IC are determined by four parameters. Maximum allowable IC chip junction temperature T_J and thermal resistance R_θ are specified by the IC manufacturer. Ambient temperature T_A and the power dissipation P_D are determined by the user. Equation 1 expresses the relation of these parameters.

$$T_J = T_A + P_D R_\theta \qquad (1)$$

Junction temperature T_J usually is limited to 150°C for silicon ICs. Devices may operate momentarily at slightly higher temperatures, but device life expectancy decreases exponentially for extended high-temperature operation. Usually, the lower the junction operating temperature, the greater the anticipated life of the IC.

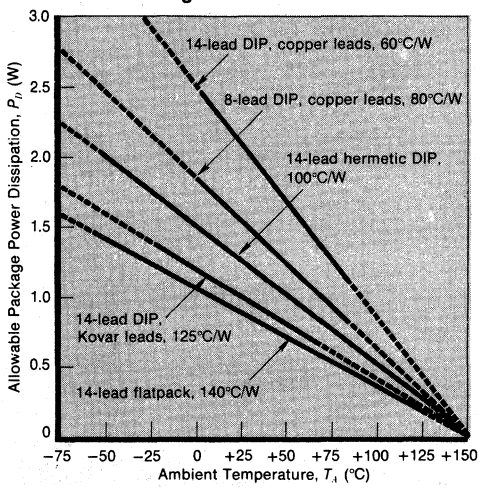
Ambient temperature T_A is traditionally limited either to 70°C or 85°C for plastic dual in-line packages (DIPs) or 125°C for hermetic devices. Again, the objective is to operate at as low a junction temperature as practical.

Thermal resistance R_θ is the basic thermal characteristic for ICs. It is usually expressed in terms of °C/W and represents the rise in junction temperature with a unit of power applied in still air. (The reciprocal of thermal resistance is thermal conductance, or derating factor,

What the Curves Show

The junction temperature of an IC depends on several factors, including the thermal resistance of the IC and the operating duty cycle. Graphs showing the relationship of these factors are often useful in specifying an IC.

Thermal Ratings

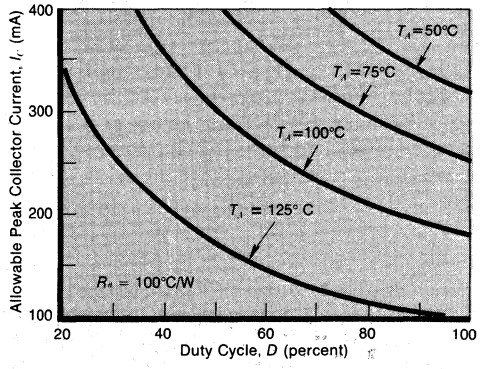


Typical thermal-resistance ratings for ICs in still air range from 60°C/W to 140°C/W. The slope of each curve on this graph is equal to the derating factor $G\theta$, which is the reciprocal of thermal resistance $R\theta$. For an ambient temperature of 50°C, a typical 14-lead flatpack with an $R\theta$ of 140°C/W can dissipate about 0.7 W. A typical DIP, however, with 14 copper-alloy leads can dissipate almost 1.7 W at 50°C.

The highest allowable package power dissipation shown here is 2.5 W. Other special-purpose DIP packages are available with power dissipation ratings as high as 3.3 W at 0°C ($R\theta$ = 45°C/W). If not for package limitations, IC chip dissipation might be greater than 9 W at an ambient temperature of up to 70°C.

Although the curve for plastic DIPs goes all the way to 150°C, they ordinarily are not used in ambients above 85°C because of traditional package limitations. Hermetic DIPs are specified to temperatures of 125°C, and at 150°C the device should be derated to 0 W. The higher specification limits for hermetic devices is the result of their design for use in rigorous, high-reliability military applications.

Duty Cycle



Duty cycle is important in calculating IC junction temperature because average power—not instantaneous power—is responsible for heating the IC. To convert from peak power to average power, multiply the peak power dissipation by the duty cycle. The average-power rating is then used with the thermal-resistance rating to calculate the IC junction temperature. Thus, short duty cycles allow peak power to be high without exceeding the 150°C junction-temperature limit. However, this consideration applies only to ON times of less than 0.5 sec.

$G\theta$ expressed as W/°C.) Thermal resistance of an IC consists of several distinct components, the sum of which is the specified thermal resistance. For a typical IC, these components of thermal resistance are 0.5°C/W per unit thickness of the silicon chip, 0.1 to 3°C/W per unit length of the lead frame, and up to 2,000°C/W per unit thickness of still air surrounding the IC. DIPs are used more than any other type of packaging for ICs and newer copper-alloy lead frames provide a superior thermal rating over the standard iron-nickel-cobalt alloy (Kovar) lead frames. However, power ICs are also available in other packages such as flatpacks and TO-type cans.

The power P_D that an IC can safely dissipate usually depends on the size of the IC chip and the type of packaging. Most common copper-frame DIPs can dissipate about 1.5 W, although some special-purpose types have ratings as high as 5 W.

Power Dissipation

Total IC power to be dissipated depends on input current, output current, voltage drop, and duty cycle. Thus, for many industrial digital-control ICs, logic-gate power P_l (typically less than 0.1 W) and output

power P_o must be determined to find the total power to be dissipated. Total power dissipation for these logic devices is the sum of P_l and P_o.

$$P_l = n(V_{CC}I_{CC}) \quad (2)$$

$$P_o = n(V_{CE(SAT)}I_C) \quad (3)$$

where V_{CC} = logic-gate supply voltage, I_{CC} = logic-gate ON current, $V_{CE(SAT)}$ = output saturation voltage, I_C = output load current, and n = number of logic gates. Manufacturers usually list typical and maximum values for these voltages and currents. For thermal considerations it is best to use the maximum values so that worst-case power dissipation is determined.

If the duty cycle of the device is longer than 0.5 sec, the peak power dissipation is the sum of the logic-gate power P_l and output power P_o for the logic ON state alone. If the ON time is less than 0.5 sec, however, average power dissipation must be calculated from instantaneous ON and OFF power P_{ON} and P_{OFF} from

$$P_D = DP_{ON} + (1 - D)P_{OFF} \quad (4)$$

Finding Safe Operating Limits

Here's how to calculate the safe operating limits for an IC. The first two examples are simple calculations involving maximum allowable power and are straightforward. The third and fourth examples are more complex and involve logic power, output power, and duty cycle.

Problem: Determine the maximum allowable power dissipation that can be handled safely by a 16-lead Kovar DIP with an R_θ of 125°C/W in an ambient temperature of 70°C.

Solution: From Equation 1, the maximum allowable power dissipation P_D for this IC is

$$P_D = \frac{150°C - 70°C}{125°C/W}$$

$$= 0.64\ W$$

Problem: Determine the maximum allowable power dissipation that can be handled by a 14-lead copper DIP with a derating factor G_θ of 16.67 mW/°C in an ambient of 70°C.

Solution: Since the derating factor G_θ is the reciprocal of thermal resistance R_θ, the maximum allowable power dissipation P_D from Equation 1 is

$$P_D = (150°C - 70°C) \times (16.67\ mW/°C)$$

$$= 1.33\ W$$

Problem: Calculate the maximum junction temperature for a quad power driver with a thermal resistance of 60°C/W in an ambient of 70°C and which is controlling a 250 mA load on each of the four outputs.

Solution: To determine the maximum (worst case) junction temperature for this IC, the maximum total power dissipation must be determined from the data listed on the IC data sheet. The specifications are usually listed as typical and minimum or maximum values. It is important to use maximum voltage and current limits to insure an adequate design. Common maximum values for an IC is calculated to be greater than the maximum values specified by the manufacturer, device reliability and operating characteristics possi-

Corrective Actions

If the junction temperature or the required power dissipation

Measuring IC Temperature

Sometimes IC junction temperature cannot be calculated readily and instead must be measured. Measurement should be made when there is insufficient data with which to calculate, when the effects of external variables such as forced-air cooling or enclosure size must be determined, or as a check on the manufacturer's specifications regarding package thermal resistance.

The most popular technique for measuring IC temperature uses the characteristic of a diode to reduce its forward voltage with temperature. Many IC chips have some sort of accessible diode—parasitic, input protection, base-emitter junction, or output clamp. With this technique, a "sense" diode is calibrated so that forward voltage is a direct indicator of diode junction temperature. Then, current is applied to some other component on the chip to simulate operating conditions and to produce a temperature rise. Since the thermal resistance of the silicon chip is low, the temperature of the sense diode is assumed to be the same as the rest of the monolithic chip.

The sense diode should be calibrated over at least the expected junction operating temperature chamber. Apply an accurately measured, low current of about 1 mA through the sense diode and measure the forward voltage in 25°C increments after stabilization at each temperature. This calibration provides enough data for at least six points to construct a diode-forward-voltage versus junction-temperature graph at the specified forward current. A typical 25°C forward voltage is between 600 and 750 mV and decreases 1.6 to 2.0 mV/°C.

For power levels above 2 W, it may be necessary to use more than a single transistor if only the device saturation voltage and sink current are used. When higher power is desired, keep the output out of saturation.

Measuring the sense-diode forward voltage may require a considerable waiting period (10 to 15 minutes) for thermal equilibrium. In any event, at the instant of measurement, the heating power may have to be disconnected since erroneous readings may result from IR drop in circuit common leads. Various circuit connections (such as four-point Kelvin) may be arranged to reduce or eliminate this source of error.

The IC junction temperature can be determined by comparing the voltage measurement with the internal power source against the voltage measurement with the temperature chamber.

APPLICATIONS INFORMATION (Cont'd)

industrial power driver are V_{CC} = 5.25 V, I_{CC} = 25 mA, and $V_{CE(SAT)}$ = 0.7V, and I_c = 250 mA. From Equations 2 and 3, worst case logic and output power dissipation are

$$P_l = 4(5.25\text{ V} \times 25\text{ mA}) = 525\text{ mW}$$

$$P_o = 4(0.7\text{ V} \times 250\text{ mA}) = 700\text{ mW}$$

Thus, the total worst case power dissipation P_D is 525 mW plus 700 mW, or 1.225 W. From Equation 1, maximum junction temperature T_J is

$$T_J = 70°\text{C} + (1.225\text{ W}) \div (16.67\text{ mW/°C}) = 143.5°\text{C}$$

Problem: Determine the acceptable duty cycle for a hermetic power driver with a thermal resistance of 100°C/W in an ambient of 85°C and which is controlling load currents of 250 mA on each of four outputs.

Solution: From Equation 1, the allowable average power dissipation P_D for this IC is

$$P_D = \frac{150°\text{C} - 85°\text{C}}{100°\text{C/W}} = 0.65\text{ W}$$

This means that there is 0.65 W limit on average power, but, not instantaneous power. If the duty cycle is low enough, and the ON time is not more than about 0.5 sec, the average power dissipation can be considerably lower than the peak power. The ON, or peak power, is determined from the data sheet maximum values of V_{CC}, I_{CC}, and $V_{CE(SAT)}$ at the specified load current of 250 mA. From Equations 2 and 3, logic-gate power P_l and output power P_o for the ON state are

$$P_l = 4(5.5\text{ V} \times 26.5\text{ mA}) = 583\text{ mW}$$

$$P_o = 4(0.7\text{ V} \times 250\text{ mA}) = 700\text{ mW}$$

Instantaneous ON power P_{ON} is the sum of P_l and P_o for the ON state, or 1.283 W. The OFF power is primarily the power dissipated by the logic in the OFF state, and is found by using the I_{CC} maximum rated current listed on the specification sheet. The power dissipated in the output stage can be calculated from the leakage current I_C and supply voltage V_{CE}. From Equations 2 and 3, logic-gate power P_l and output power P_o for the OFF state are

$$P_l = 4(5.5\text{ V} \times 7.5\text{ mA}) = 165\text{ mW}$$

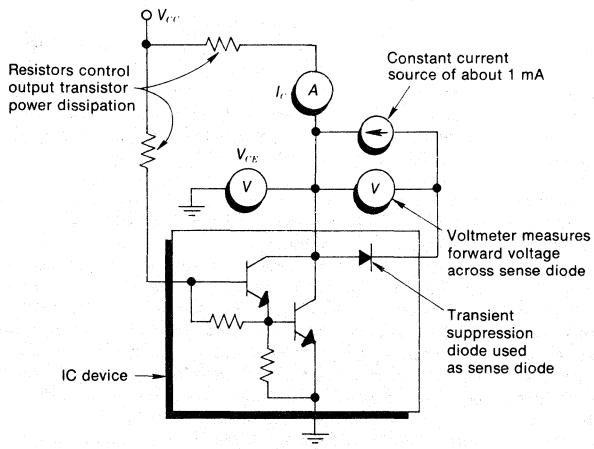
$$P_o = 4(100\text{ V} \times 0.1\text{ mA}) = 40\text{ mW}$$

Instantaneous OFF power P_{OFF} is the sum of P_l and P_o for the OFF state, or 205 mW. From Equation 4, acceptable duty cycle D is

$$D = \frac{P_D - P_{OFF}}{P_{ON} - P_{OFF}} = \frac{0.65\text{ W} - 0.205\text{ W}}{1.283\text{ W} - 0.205\text{ W}} = 41.3\%$$

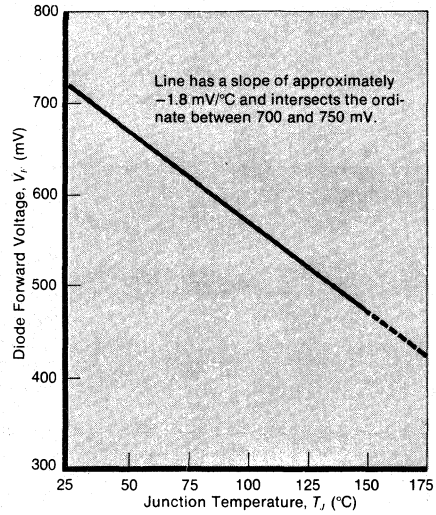
bly will be reduced. Possible solutions are: 1. Modify or partition the circuit design so the IC is not required to dissipate as much power. 2. Reduce the thermal resistance of the IC by using a heat sink or forced-air cooling. 3. Reduce the ambient temperature by moving heat-producing components such as transformers and resistors away from the IC. 4. Specify a different IC with improved thermal or electrical characteristics (if available). MD

Setting Up the Circuit

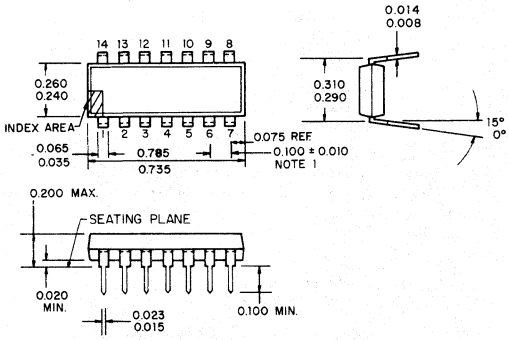


Input power is negligible compared to output power and is therefore not measured.

Calibrating the Sense Diode

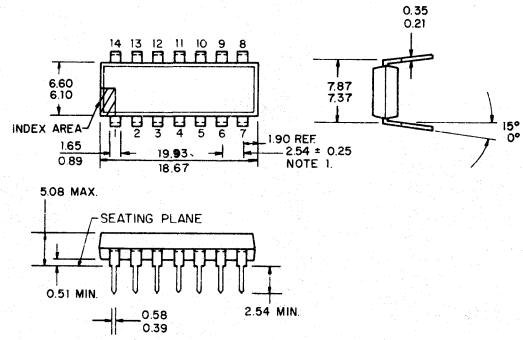


DIMENSIONS IN INCHES

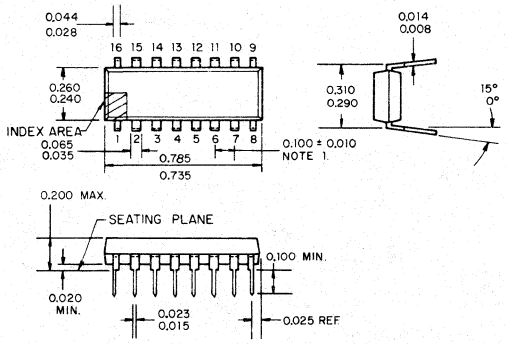


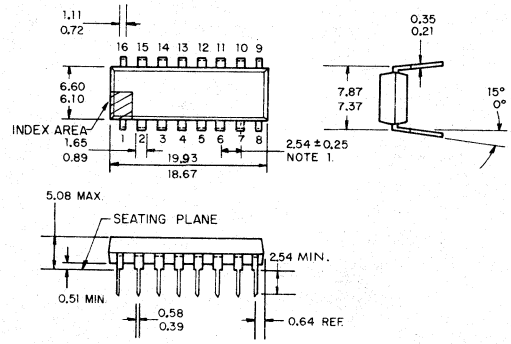
DIMENSIONS IN MILLIMETRES

METRIC DIMENSIONS ARE BASED ON 1" = 25.4 mm

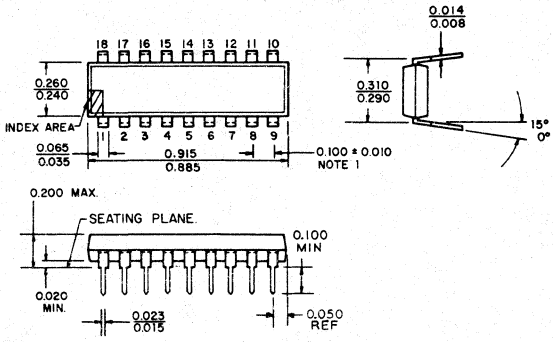


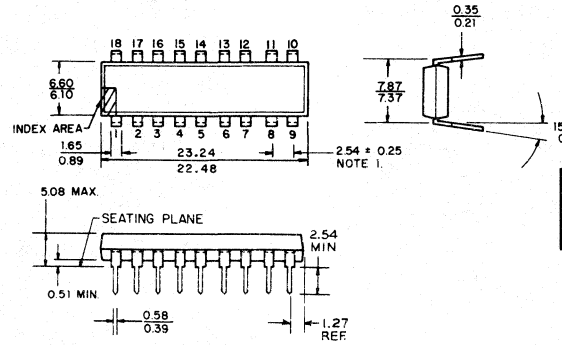
'A' PACKAGE: 14-Pin Plastic Dual In-Line





'A' PACKAGE: 16-Pin Plastic Dual In-Line





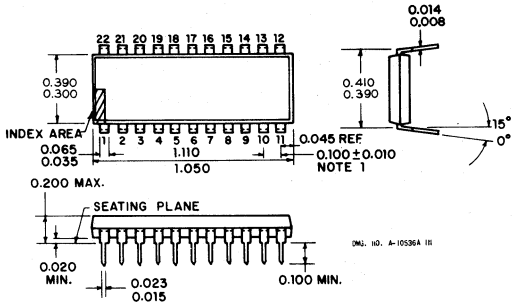
'A' PACKAGE: 18-Pin Plastic Dual In-Line

NOTES:

1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030" (0.76 mm) max. below seating plane.

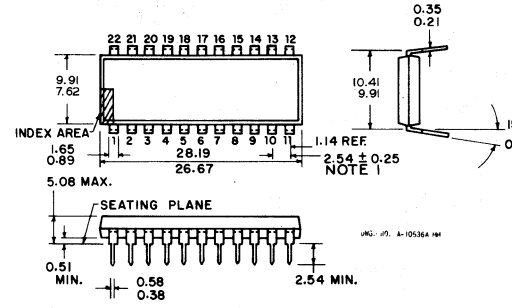
PACKAGE DRAWINGS (Cont'd)

DIMENSIONS IN INCHES

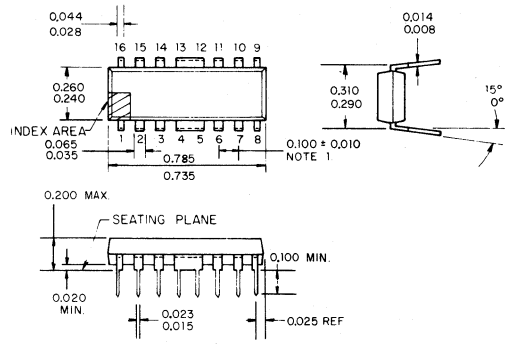


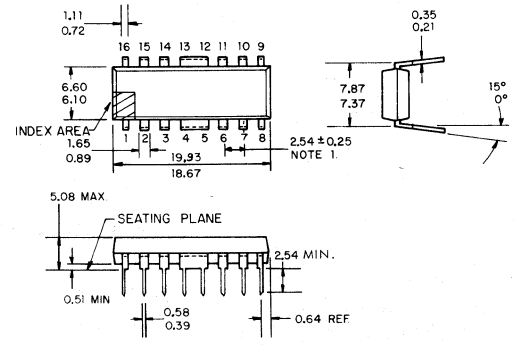
DIMENSIONS IN MILLIMETRES

METRIC DIMENSIONS ARE BASED ON 1" = 25.4 mm



'A' PACKAGE: 22-Pin Plastic Dual In-Line



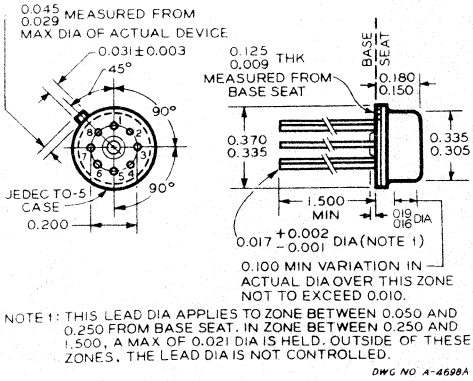


'B' PACKAGE: 16-Pin Plastic Dual In-Line

NOTES:

1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030" (0.76 mm) max. below seating plane.

DIMENSIONS IN INCHES

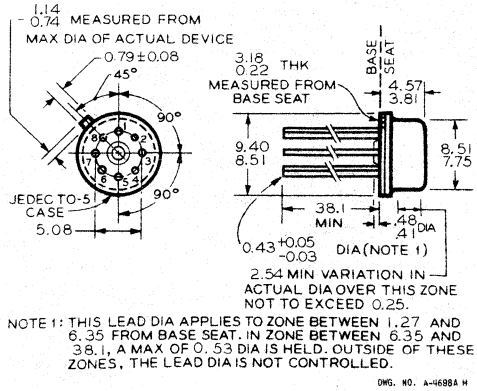


NOTE 1: THIS LEAD DIA APPLIES TO ZONE BETWEEN 0.050 AND 0.250 FROM BASE SEAT. IN ZONE BETWEEN 0.250 AND 1.500, A MAX OF 0.021 DIA IS HELD. OUTSIDE OF THESE ZONES, THE LEAD DIA IS NOT CONTROLLED.

DWG NO A-4698A

DIMENSIONS IN MILLIMETRES

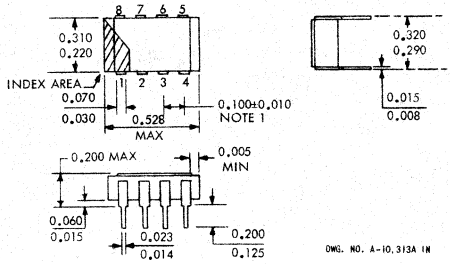
METRIC DIMENSIONS ARE BASED ON 1" = 25.4 mm



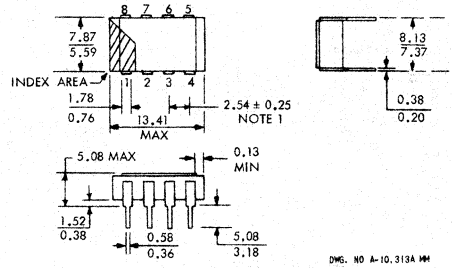
NOTE 1: THIS LEAD DIA APPLIES TO ZONE BETWEEN 1.27 AND 6.35 FROM BASE SEAT. IN ZONE BETWEEN 6.35 AND 38.1, A MAX OF 0.53 DIA IS HELD. OUTSIDE OF THESE ZONES, THE LEAD DIA IS NOT CONTROLLED.

DWG. NO. A-4698A M

'D' PACKAGE: 8-Pin Metal Can



DWG. NO. A-10.313A IN



DWG. NO A-10.313A MM

'H' PACKAGE: 8-Pin Hermetic Dual In-Line

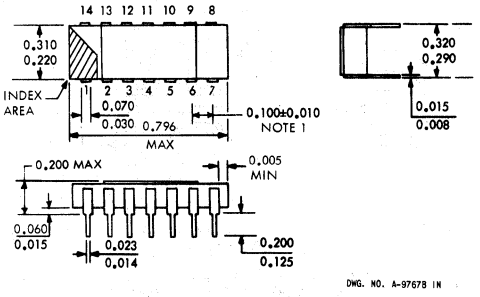
7

NOTES:

1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030" (0.76 mm) max. below seating plane.

PACKAGE DRAWINGS (Cont'd)

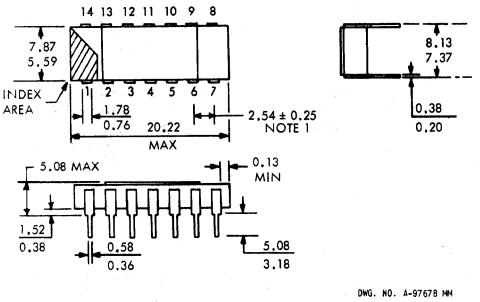
DIMENSIONS IN INCHES



DWG. NO. A-97678 IN

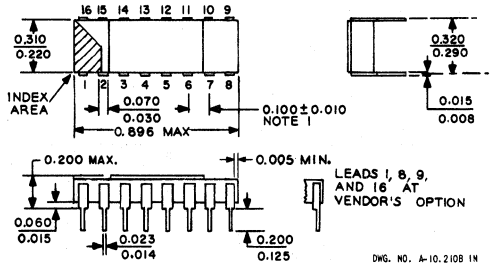
DIMENSIONS IN MILLIMETRES

METRIC DIMENSIONS ARE BASED ON 1″ = 25.4 mm

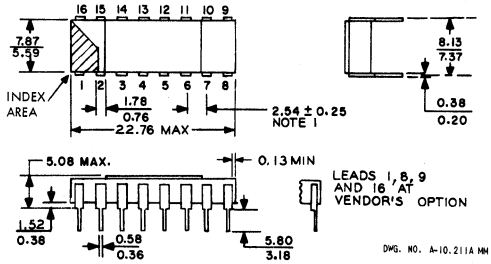


DWG. NO. A-97678 MM

'H' PACKAGE: 14-Pin Hermetic Dual In-Line

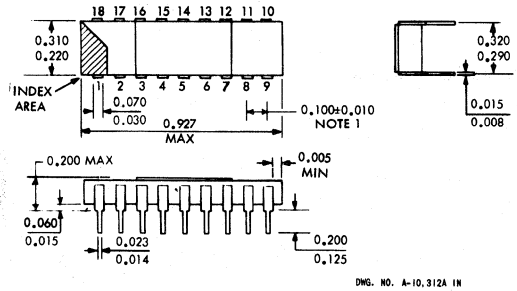


DWG. NO. A-10.210B IN

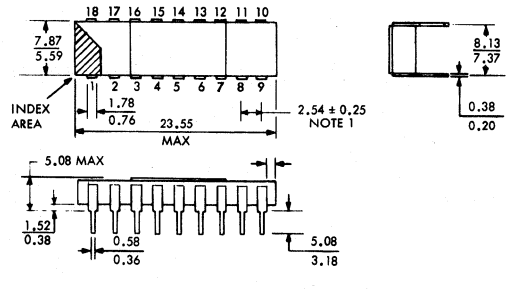


DWG. NO. A-10.211A MM

'H' PACKAGE: 16-Pin Hermetic Dual In-Line



DWG. NO. A-10.312A IN

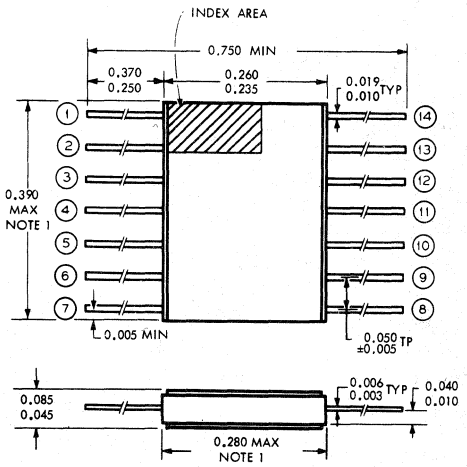


'H' PACKAGE: 18-Pin Hermetic Dual In-Line

NOTES:

1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030″ (0.76 mm) max. below seating plane.

DIMENSIONS IN INCHES

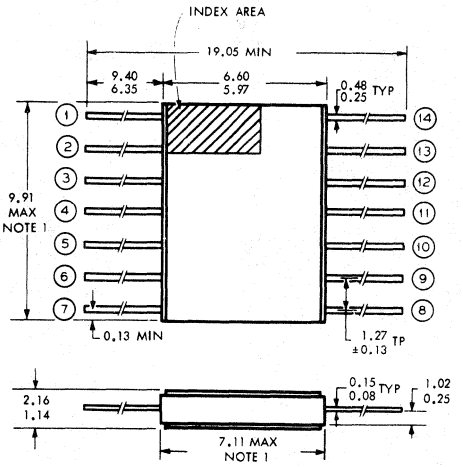


NOTES:
1 INCLUDES OFF-CENTER LID, MENISCUS, + GLASS OVERRUN
2 ALL LEADS WELDABLE AND SOLDERABLE

DWG. NO. A-10.252A IN

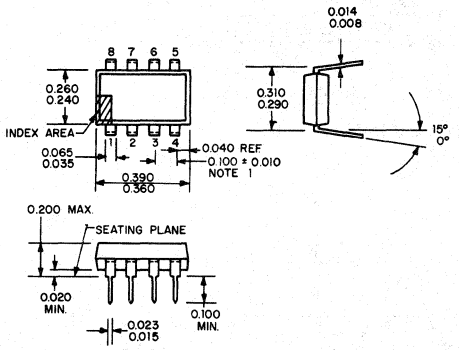
DIMENSIONS IN MILLIMETRES

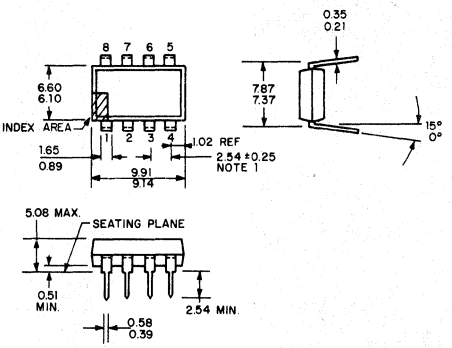
METRIC DIMENSIONS ARE BASED ON 1" = 25.4 mm



DWG. NO. A-10.252A MM

'J' PACKAGE: 14-Pin Hermetic Flat-Pack





NOTES:

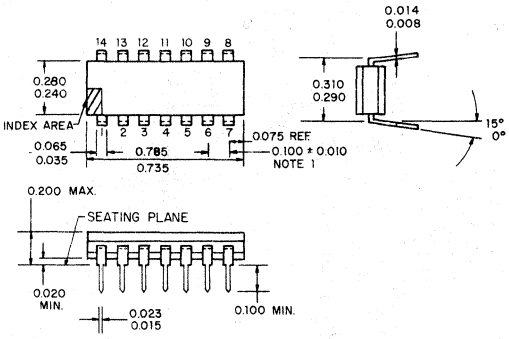
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030" (0.76 mm) max. below seating plane.

'M' PACKAGE: 8-Pin Plastic Dual In-Line

7

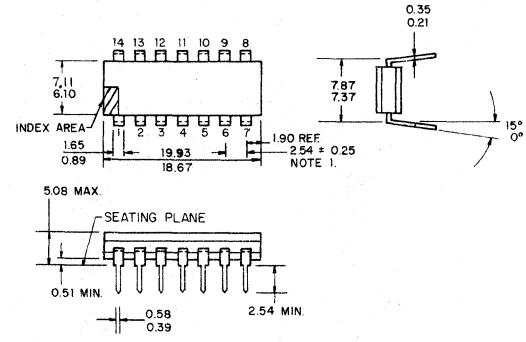
PACKAGE DRAWINGS (Cont'd)

DIMENSIONS IN INCHES

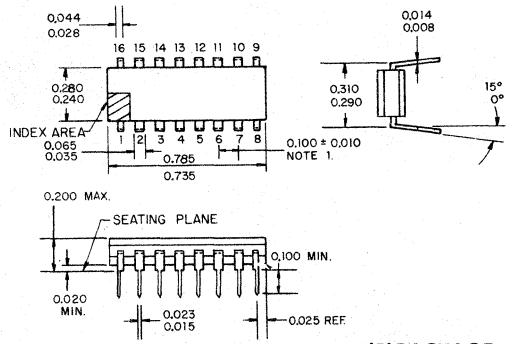


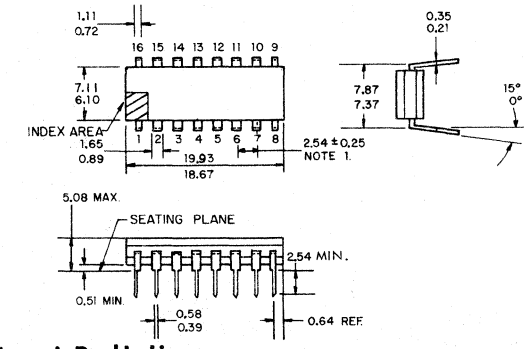
DIMENSIONS IN MILLIMETRES

METRIC DIMENSIONS ARE BASED ON 1" = 25.4 mm

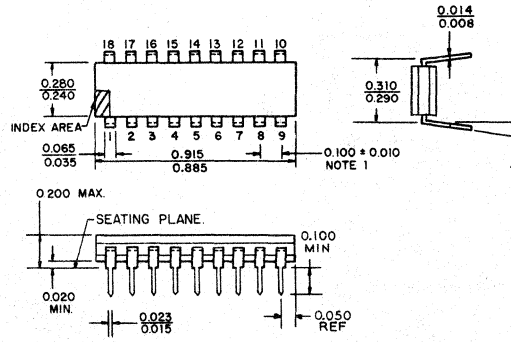


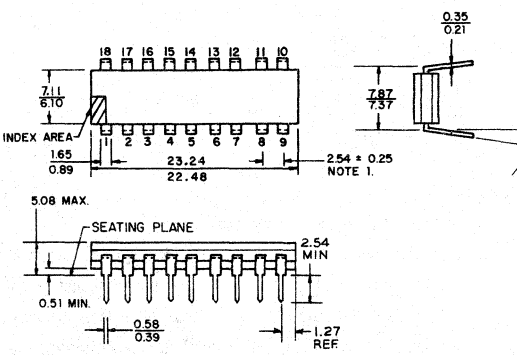
'R' PACKAGE: 14-Pin Ceramic Dual In-Line





'R' PACKAGE: 16-Pin Ceramic Dual In-Line





'R' PACKAGE: 18-Pin Ceramic Dual In-Line

NOTES:

1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030" (0.76 mm) max. below seating plane.

Package Thermal Characteristics

Package Type	Designator	Frame Mater	Applicable Curve	RΘja	GΘja
Plastic					
8 Lead Mini	M	Copper	Fig 1C	80°C/W	12.5mW/°C
14 Lead	A	Kovar	Fig 1E	125°C/W	8mW/°C
14 Lead	A	Copper	Fig 1B	60°C/W	16.67mW/°C
16 Lead	A	Kovar	Fig 1E	125°C/W	8mW/°C
16 Lead	A	Copper	Fig 1B	60°C/W	16.67mW/°C
16 Lead	B	Copper	Fig 2C	45°C/W	22.22mW/°C
16 Lead (V8 Heat Sink)	B	Copper	Fig 2B	37.5°C/W	26.67mW/°C
16 Lead (V7 Heat Sink)	B	Copper	Fig 2A	27.5°C/W	36.36mW/°C
18 Lead	A	Kovar	Fig 1D	110°C/W	9.1mW/°C
18 Lead	A	Copper	Fig 1A	55°C/W	18.18mW/°C
22 Lead	A	Copper	—	50°C/W	20mW/°C
Cer DIP					
14 Lead	R	Kovar	Fig 3B	75°C/W	13.33mW/°C
16 Lead	R	Kovar	Fig 3B	75°C/W	13.33mW/°C
18 Lead	R	Kovar	Fig 3A	65°C/W	15.4mW/°C
Hermetic					
8 Lead	H		Fig 4C	120°C/W	8.33mW/°C
14 Lead	H		Fig 4B	90°C/W	11.1mW/°C
16 Lead	H		Fig 4B	90°C/W	11.1mW/°C
18 Lead	H		Fig 4A	75°C/W	13.33mW/°C
14 Lead	J (flat pack)		Fig 4D	140°C/W	7.14mW/°C

NOTE: Further thermal information is contained in the Applications Section; reference pages 7–16, 7–23, 7–43, and 7–49 thru 52.

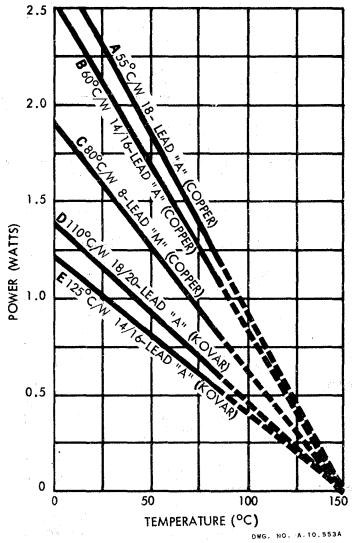


Figure 1

ALL 'A' and 'M' PACKAGES (Kovar and Copper)

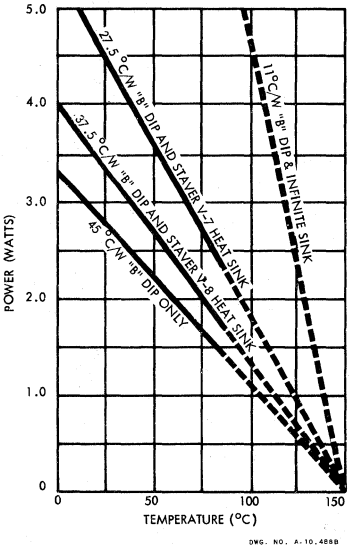


Figure 2

'B' PACKAGE (Copper Only)

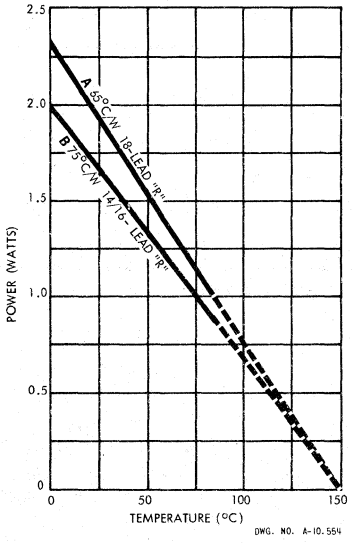


Figure 3

ALL 'R' PACKAGES (CER DIP)

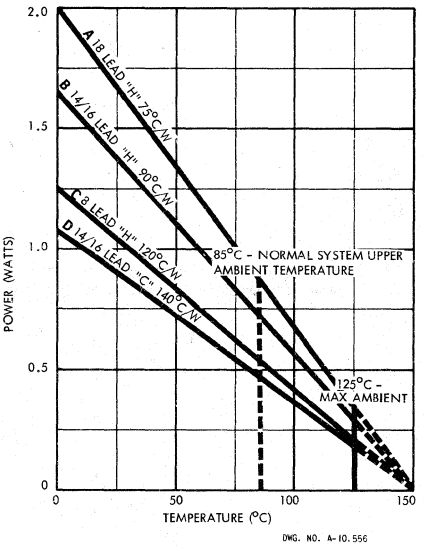


Figure 4

SIDE BRAZED CERAMIC AND FLAT PACK (Aerospace and Military)

NOTES

NOTES

NOTES

In the construction of the components described, the full intent of the specification will be met. The Sprague Electric Company, however, reserves the right to make, from time to time, such departures from the detail specification as may be required to permit improvements in the design of its products. Components made under military approvals will be in accordance with the approval requirements.

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