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INTEGRATED CIRCUITS

INTEGRATED CIRCUITS

DATA
BOOK
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Power
Interface • Linear • Hall-Effect • Transistor
Arrays

SPRAGUE®
THE MARK OF RELIABILITY
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INTEGRATED CIRCUITS

INTERFACE

- High Voltage
- High Current
- BiMOS and Complex Arrays

LINEAR

- Radio/Communications
- Video and Television
- Audio

HALL EFFECT DEVICES

TRANSISTOR ARRAYS

☐   ☐   ☐

SPRAGUE ELECTRIC COMPANY

INTERFACE AND LINEAR INTEGRATED CIRCUITS
115 Northeast Cutoff • Worcester, Mass. 01606 • 617/853-5000

DISCRETE SEMICONDUCTORS AND HALL EFFECT ICs
70 Pembroke Road • Concord, N.H. 03301 • 603/224-1961

Contents

SECTION 3—HIGH-CURRENT INTERFACE DRIVERS

*New product. Contact factory for detailed information.

SECTION 4—BiMOS AND COMPLEX ARRAY INTERFACE DRIVERS

SECTION 5—MILITARY AND AEROSPACE DEVICES

*New product. Contact factory for detailed information.

SECTION 6—RADIO/COMMUNICATIONS INTEGRATED CIRCUITS

SECTION 7—VIDEO AND TELEVISION INTEGRATED CIRCUITS

*New product. Contact factory for detailed information.

SECTION 8—AUDIO POWER AMPLIFIERS

SECTION 9—HALL EFFECT DEVICES

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New product. Contact factory for detailed information.

SECTION 10—TRANSISTOR ARRAYS AND MISCELLANEOUS DEVICES

*New product. Contact factory for detailed information.

SECTION 11—CUSTOM DEVICES

SECTION 12—PACKAGE INFORMATION

Product Index in Numerical Order

Product Index (Continued)

*New Product. Contact factory for detailed information.

Product Index (Continued)

*New product. Contact factory for detailed information.

Product Index (Continued)

*New product. Contact factory for detailed information.

1

SECTION 1—GENERAL INFORMATION

Sprague Part Numbering Systems

UL   N - 2046   A - 1

INSTRUCTIONS.
1 = SELECTED VERSION, SEE DETAIL SPECIFICATIONS
BU = BURNED-IN PARTS TO DOUBLE-DEUCE PROGRAM
MIL = MILITARY GRADE WITH SCREENING TO MIL-STD-883,
   CLASS B (PACKAGES H, J, AND R ONLY)

PACKAGE DESIGNATION.
A = PLASTIC, 14- THROUGH 40-PIN DUAL IN-LINE
B = PLASTIC, 8- THROUGH 22-PIN DUAL IN-LINE SEMI-TAB
C = UNPACKAGED CHIP
CW = PROBED WAFER
D = METAL CAN, 3-LEAD (TO-52)
E = LEADLESS CHIP CARRIER (CONTACT FACTORY)
H = GLASS/METAL HERMETIC, 8- THROUGH 40-PIN DUAL IN-LINE
J = GLASS/METAL HERMETIC, 14-LEAD FLAT PACK
L = PLASTIC SOIC (CONTACT FACTORY)
M = PLASTIC, 8-PIN DUAL IN-LINE
P = DIRECTLY REPLACED BY B PACKAGE
Q = PLASTIC, 16-PIN QUAD IN-LINE
R = CERAMIC/GLASS HERMETIC, 14- THROUGH 40-PIN DUAL IN-LINE
S = PLASTIC, 4-LEAD SINGLE IN-LINE
T = PLASTIC, 3-LEAD SINGLE IN-LINE
U = PLASTIC, 3-LEAD THIN SINGLE IN-LINE
V = METAL FLANGE MOUNT, 11-LEAD (TO-3)
W = PLASTIC, 12-LEAD SINGLE IN-LINE POWER TAB
Y = PLASTIC, 3-LEAD (TO-92)
Z = PLASTIC, 5-LEAD SINGLE IN-LINE POWER TAB (TO-220)
ZH = Z PACKAGE WITH FORMED LEADS FOR HORIZONTAL MOUNT
ZV = Z PACKAGE WITH FORMED LEADS FOR VERTICAL MOUNT

DEVICE TYPE (FOUR DIGITS).

OPERATING AMBIENT TEMPERATURE RANGE.
N = COMMERCIAL/INDUSTRIAL, SEE DETAIL SPECIFICATIONS
Q = EXTENDED (− 40°C TO + 85°C)
S = FULL MILITARY (− 55°C TO + 125°C)
X = SPECIAL SIGNIFIER FOR PRE-PRODUCTION DEVICES

FAMILY (UC, UD, UG, UL, OR UT).

Sprague Part Numbering Systems

UH   D - 400 - 1

INSTRUCTIONS.
1 = SELECTED VERSION, SEE DETAIL SPECIFICATIONS
MIL = MILITARY GRADE WITH SCREENING TO MIL-STD-883,
       CLASS B (PACKAGES C AND D ONLY)

DEVICE TYPE (THREE DIGITS).

PACKAGE DESIGNATION.
C = GLASS/METAL HERMETIC, 14-PIN FLAT PACK
D = GLASS/METAL HERMETIC, 14-PIN DUAL IN-LINE
K = UNPACKAGED CHIP OR PROBED WAFER
P = PLASTIC, 14-PIN DUAL IN-LINE
R = CERAMIC/GLASS HERMETIC, 14-PIN DUAL IN-LINE

FAMILY (UH ONLY).

TPP - 1000

DEVICE TYPE (FOUR DIGITS OR FOUR DIGITS AND LETTER).

FAMILY.
TPP = DARLINGTON ARRAY
TPQ = QUAD TRANSISTOR ARRAY

CROSS-REFERENCE in Numerical Order

The suggested Sprague replacement devices are based on similarity as shown in currently published data. Exact replacement in all applications is not guaranteed. The user should compare the specifications of the competitive and recommended Sprague replacement.

Manufacturers' Abbreviations:

AMI	American Microsystems
CS	Cherry Semiconductor
DI	Dionics, Inc.
EXR	Exar Integrated Systems
FER	Ferranti Limited
FSC	Fairchild Semiconductor
FUJ	Fujitsu
GE	General Electric*
HIT	Hitachi Ltd.
IR	International Rectifier*
ITT	ITT Semiconductors
MAL	P. R. Mallory*
MAT	Matsushita
MIT	Mitsubishi Electric Corp.
MOT	Motorola Semiconductor
NEC	Nippon Electric Co.
NS	National Semiconductor
OKI	Oki Semiconductor
PE	Pro-Electron‡
PLS	Plessey Semiconductor
RAY	Raytheon Co.*
RCA	RCA
RFA	Rifa
SANY	Sanyo
SG	Silicon General Inc.
SIG	Signetics Corp.
SIL	Siliconix
SGS	SGA/ATES
SPC	Sprague Products Co.*
SPR	Sprague Electric Co.
SYL	Sylvania
THM	Thomson-CSF
TI	Texas Instruments
TLF	AEG-Telefunken
TOKO	RCL Toko
TOS	Toshiba Corp.
UNI	Unitrode

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
AD741CH		ULN-2151D*
AD741CN		ULN-2151M*
AN206	MAT	ULN-2165A*
CA124E	RCA	ULN-4336A*
CA224E	RCA	ULN-4336A*
CA324E	RCA	ULN-4336A*
CA741CE	RCA	ULN-2151M*
CA741CT	RCA	ULN-2151D*
CA758E	RCA	ULN-3812A
CA1190E	RCA	ULN-2290B
CA1190Q	RCA	ULN-2290Q
CA1310E	RCA	ULN-3810A
CA1391E	RCA	ULN-2291M*
CA1394E	RCA	ULN-2294M*
CA1398E	RCA	ULN-2298A*
CA1724G	RCA	TPQ-3724
CA1725G	RCA	TPQ-3725
CA2002	RCA	ULN-3701Z
CA2002M	RCA	ULN-3701ZH
CA2004	RCA	ULN-3702Z
CA2004M	RCA	ULN-3702ZH
CA2111AE	RCA	ULN-2111A
CA2136AE	RCA	ULN-2136A*
CA3045	RCA	ULS-2045H

‡European registration; manufactured by various companies including ITT, Philips, SGS/ATES, Siemens, Thomson-CSF, AEG-Telefunken, and Valvo.
*No longer manufactured. Listed for reference only.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
CA3045F	RCA	ULS-2045R
CA3045L	RCA	ULS-2045H
CA3046	RCA	ULN-2046A
CA3054	RCA	ULN-2054A
CA3064E	RCA	ULN-2264A*
CA3065	RCA	ULN-2165A*
CA3066	RCA	ULN-2266A*
CA3067	RCA	ULN-2267A*
CA3070	RCA	ULN-2124A*
CA3071	RCA	ULN-2127A*
CA3072	RCA	ULN-2228A*
CA3075	RCA	ULN-2129A*
CA3081E	RCA	ULN-2081A
CA3082E	RCA	ULN-2082A
CA3083E	RCA	ULN-2083A
CA3086	RCA	ULN-2986A
CA3089E	RCA	ULN-2289A*
CA3120E	RCA	ULN-2125A*
CA3121E	RCA	ULN-2269A*
CA3123E	RCA	ULN-2137A*
CA3126Q	RCA	ULN-2262A*
CA3135G	RCA	ULN-2261A*
CA3146E	RCA	ULN-2046A-1
CA3153G	RCA	ULN-2297A*
CA3170E	RCA	ULN-2268A*
CA3172G	RCA	ULN-2229A*
CA3183AE	RCA	ULN-2083A-1
CA3183E	RCA	ULN-2083A-1
CA3189E	RCA	ULN-3889A*
CA3195	RCA	ULN-3812A*
CA3209E	RCA	ULX-3888A*
CA3217E	RCA	ULN-3914A
CA3219E	RCA	UDN-2541B
CA3724G	RCA	TPQ-3724
CA3725G	RCA	TPQ-3725
CA10806A	RCA	ULN-3914A
CS102	CS	ULN-3304M*
CS122	CS	ULN-3306M*
CS166	CS	ULN-2492A

Competitive Part Number	Manufacturer	Suggested Sprague Replacement
DH3724CN	NS	TPQ-3724
DH3725CN	NS	TPQ-3725
DI302	DI	UDN-7183A
DI502	DI	UDN-6144A*†
DI507	DI	UDN-6116A-1¶
DI509	DI	UDN-6116A-2¶
DI510	DI	UDN-6510A
DI512	DI	UDN-6514A
DI514	DI	UDN-6118A-2¶
DM3724CN	NS	TPQ-3724
DM3725CN	NS	TPQ-3725
DS3611N	NS	UDN-3611M
DS3612N	NS	UDN-3612M
DS3613N	NS	UDN-3613M
DS3614N	NS	UDN-3614M
DVR-01		UHP-480*
FPQ2222	FSC	TPQ-2222
FPQ2907	FSC	TPQ-2907
FPQ3724	FSC	TPQ-3724
FPQ3725	FSC	TPQ-3725
FSA2619P	FSC	TND-908
FSA2719P	FSC	TND-903
GEL2113	GE	ULN-2111A
HA1137W	HIT	ULN-2289A*
HA1156W	HIT	ULN-3810A-1
HA1199	HIT	ULN-2249A
HA1364	HIT	ULN-2290Q
HA1377A	HIT	ULX-3777W*
HA1388	HIT	ULX-3788W*
HA12402	HIT	ULN-2204A
ITT512	ITT	UHP-491*
ITT552	ITT	ULN-2001A

¶Sprague device includes internal pull-down resistors.
*No longer manufactured. Listed for reference only.
†Some differences in specified switching speed with the Sprague device being superior for use with inductive loads.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement	Competitive Part Number	Manufacturer	Suggested Sprague Replacement
ITT554	ITT	ULN-2002A	LM124N	NS	ULN-4336A*
ITT556	ITT	ULN-2003A	LM148N	NS	ULN-4336A*
ITT652	ITT	ULN-2001A	LM224N	NS	ULN-4336A*
ITT654	ITT	ULN-2002A	LM324N	NS	ULN-4336A*
ITT656	ITT	ULN-2003A	LM377N	NS	ULN-2274B*
ITT3064	ITT	ULN-2264A*	LM378N	NS	ULN-2278B-1*
ITT3065	ITT	ULN-2165A*	LM380N	NS	ULN-2280B
			LM383AT	NS	ULN-3702Z
KB4402	TOKO	ULN-2289A*	LM383T	NS	ULN-3701Z
KB4409	TOKO	ULN-3810A	LM384N	NS	ULN-3784B
			LM741CH	NS	ULN-2151D*
L119	SGS	ULX-3908Q*	LM741CN	NS	ULN-2151M*
L180	SGS	ULX-3801Q*	LM746N	NS	ULN-2228A*
L201	SGS	ULN-2001A	LM1304	NS	ULN-2120A*
L202	SGS	ULN-2002A	LM1305	NS	ULN-2122A*
L203	SGS	ULN-2003A	LM1307N	NS	ULN-2128A*
L204	SGS	ULN-2004A	LM1310N	NS	ULN-3810A-1
L601	SGS	ULN-2821A	LM1391N	NS	ULN-2291M*
L602	SGS	ULN-2822A	LM1394N	NS	ULN-2294M*
L603	SGS	ULN-2823A			
L604	SGS	ULN-2824A	LM1800N	NS	ULN-3812A
			LM1820N	NS	ULN-2137A*
LA705PC	SANY	ULN-3812A	LM1827N	NS	ULN-2224A*
LA758PC	SANY	ULN-3812A	LM1828N	NS	ULN-2228A*
LA1160	SANY	ULN-2243A	LM1829N	NS	ULN-2262A*
LA1230	SANY	ULN-2289A*	LM1841N	NS	ULN-2136A*
LA1364	SANY	ULN-2264A*	LM1848N	NS	ULN-2229A*
LA1368	SANY	ULN-2298A*	LM1877N	NS	ULN-2274B*
LA1369	SANY	ULN-2224A*	LM2002T	NS	ULN-3701Z
LA3045	SANY	ULS-2045H	LM2002AT	NS	ULN-3702Z
LA3046	SANY	ULN-2046A	LM2111N	NS	ULN-2111A
LA3086	SANY	ULN-2086A	LM2113N	NS	ULN-2111A
LA3089	SANY	ULN-2289A*	LM3045D	NS	ULS-2045H
LA3301	SANY	ULN-3810A-1	LM3046N	NS	ULN-2046A
LA3350	SANY	ULN-3810A	LM3053N	NS	ULN-2209M*
LB1231	SANY	ULN-2001A	LM3054N	NS	ULN-2054A
LB1232	SANY	ULN-2002A	LM3064N	NS	ULN-2264A*
LB1233	SANY	ULN-2003A	LM3065N	NS	ULN-2165A*
LB1234	SANY	ULN-2004A	LM3066N	NS	ULN-2266A*
LB1294	SANY	UHP-491*	LM3067N	NS	ULN-2267A*

*No longer manufactured. Listed for reference only.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement	Competitive Part Number	Manufacturer	Suggested Sprague Replacement
LM3070N	NS	ULN-2124A*	MC1356P	MOT	ULN-2136A*
LM3071N	NS	ULN-2127A*	MC1357P	MOT	ULN-2111A
LM3072N	NS	ULN-2228A*	MC1358P	MOT	ULN-2165A*
LM3075N	NS	ULN-2129A*	MC1364P	MOT	ULN-2264A*
LM3086N	NS	ULN-2086A	MC1370P	MOT	ULN-2124A*
LM3089N	NS	ULN-2289A*	MC1371P	MOT	ULN-2127A*
LM3611N	NS	UDN-3611M	MC1375P	MOT	ULN-2129A*
LM3612N	NS	UDN-3612M	MC1389P	MOT	ULN-2289A*
LM3613N	NS	UDN-3613M	MC1391P	MOT	ULN-2291M*
LM3614N	NS	UDN-3614M	MC1394P	MOT	ULN-2294M*
			MC1398P	MOT	ULN-2298A*
M54523	MIT	ULN-2003A			
M54524P	MIT	ULN-2001A	MC1411L	MOT	ULN-2001R
M54525P	MIT	ULN-2002A	MC1411P	MOT	ULN-2001A
M54526P	MIT	ULN-2004A	MC1412L	MOT	ULN-2002R
M54532P	MIT	ULN-2064B	MC1412P	MOT	ULN-2002A
M54562P	MIT	UDN-2982A	MC1413L	MOT	ULN-2003R
M5463P	MIT	UDN-2981A	MC1413P	MOT	ULN-2003A
			MC1413TP	MOT	ULQ-2003A
MB3759C	FUJ	ULQ-8194R§	MC1416L	MOT	ULN-2004R
MB3759P	FUJ	ULQ-8194A§	MC1416P	MOT	ULN-2004A
MB3760C	FUJ	ULQ-8195R§	MC1417P	MOT	UDN-2580A
MB3760P	FUJ	ULQ-8195A§	MC1439G	MOT	ULN-2139G*
			MC1439P1	MOT	ULN-2139M*
MC1304	MOT	ULN-2120A*	MC1471P1	MOT	UDN-5711M
MC1305	MOT	ULN-2122A*	MC1472P1	MOT	UDN-5712M
MC1307P	MOT	ULN-2128A*	MC1473P1	MOT	UDN-5713M
MC1309	MOT	ULN-3809A	MC1474P1	MOT	UDN-5714M
MC1310EP	MOT	ULN-3810A	MC1741CG	MOT	ULN-2151D*
MC1310P	MOT	ULN-3810A	MC1741CP1	MOT	ULN-2151M*
MC1311P	MOT	ULN-3812A	MC3346	MOT	ULN-2046A
MC1320P	MOT	ULN-2137A*	MC3357P	MOT	ULX-3857A*
MC1324P	MOT	ULN-2224A*	MC3386P	MOT	ULN-2086A
MC1326P	MOT	ULX-2226A*	MC3403P	MOT	ULN-4336A*
MC1327P	MOT	ULN-2217A*	MFC4050	MOT	ULN-2135E*
MC1328P	MOT	ULN-2228A*			
MC1329P	MOT	ULN-2229A*	ML3045		ULS-2045H
MC1339P	MOT	ULN-2126A*	ML3046		ULN-2046A
MC1344P	MOT	ULN-3812A	ML3086		ULN-2086A

*No longer manufactured. Listed for reference only.
§Sprague engineering bulletin in preparation.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement	Competitive Part Number	Manufacturer	Suggested Sprague Replacement
MPQ2221	MOT	TPQ-2221	NE594F	SIG	UDN-6118R-2
MPQ2222	MOT	TPQ-2222	NE594N	SIG	UDN-6118A-2
MPQ2369	MOT	TPQ-2369	NE5501N	SIG	ULN-2021A
MPQ2483	MOT	TPQ-2483	NE5502N	SIG	ULN-2022A
MPQ2484	MOT	TPQ-2484	NE5503N	SIG	ULN-2023A
MPQ2906	MOT	TPQ-2906	NE5504N	SIG	ULN-2024A
MPQ2907	MOT	TPQ-2907	NE5560F	SIG	ULN-8160R
MPQ3724	MOT	TPQ-3724	NE5560N	SIG	ULN-8160A
MPQ3725	MOT	TPQ-3725	NE5561N	SIG	ULN-8161M
MPQ3725A	MOT	TPQ-3725A	NE5562F	SIG	ULN-8162R§
MPQ3798	MOT	TPQ-3798	NE5562N	SIG	ULN-8162A§
MPQ3799	MOT	TPQ-3799	NE5563F	SIG	ULN-8163R§
MPQ3904	MOT	TPQ-3904	NE5563N	SIG	ULN-8163A§
MPQ3906	MOT	TPQ-3906	NE5601N	SIG	ULN-2001A
MPQ6001	MOT	TPQ-6001	NE5602N	SIG	ULN-2002A
MPQ6002	MOT	TPQ-6002	NE5603N	SIG	ULN-2003A
MPQ6100	MOT	TPQ-6100	NE5604N	SIG	ULN-2004A
MPQ6100A	MOT	TPQ-6100A			
MPQ6501	MOT	TPQ-6501	PA239	GE	ULN-2126A*
MPQ6502	MOT	TPQ-6502			
MPQ6600	MOT	TPQ-6600	PBD352301J	RFA	ULN-2001R
MPQ6600A	MOT	TPQ-6600A	PBD352301N	RFA	ULN-2001A
MPQ6700	MOT	TPQ-6700	PBD352302J	RFA	ULN-2004R
			PBD352302N	RFA	ULN-2004A
MSL912R	OKI	UDN-6118A-2	PBD352303J	RFA	ULN-2003R
			PBD352303N	RFA	ULN-2003A
N2211A	SIG	ULN-2211B*	PBD352304J	RFA	ULN-2002R
N2212A	SIG	ULN-2212B*	PBD352304N	RFA	ULN-2002A
N5065A	SIG	ULN-2165A*	PBD352311N	RFA	ULN-2021A
N5070B	SIG	ULN-2124A*	PBD352312N	RFA	ULN-2024A
N5071A	SIG	ULN-2127A*	PBD352313N	RFA	ULN-2023A
N5072A	SIG	ULN-2228A*	PBD352314N	RFA	ULN-2022A
N5111A	SIG	ULN-2111A	PBD353801J	RFA	ULN-2801R
N5741T	SIG	ULN-2151D*	PBD353802J	RFA	ULN-2804R
N5741V	SIG	ULN-2151M*	PBD353803J	RFA	ULN-2803R
			PBD353804J	RFA	ULN-2802R
NA3086		ULN-2086A			
			PWM25BK	SIL	ULQ-8125R§
			PWM25CK	SIL	ULN-8125R§
NE564F	SIG	ULN-8564R§	PWM27BK	SIL	ULQ-8127R§
NE564N	SIG	ULN-8564A§	PWM27CK	SIL	ULN-8127R§

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Competitive Part Number	Manufacturer	Suggested Sprague Replacement	Competitive Part Number	Manufacturer	Suggested Sprague Replacement
Q2T2222	TI	TPQ-2222	SG2002N	SG	ULN-2002A
Q2T3725	TI	TPQ-3725	SG2003J	SG	ULS-2003R
			SG2003N	SG	ULN-2003A
RC741DN	RAY	ULN-2151M*	SG2004J	SG	ULS-2004R
RC741TE	RAY	ULN-2151D*	SG2004N	SG	ULN-2004A
RC4136DP	RAY	ULN-4136A*	SG2524BJ	SG	ULQ-8124R§
RC4236DP	RAY	ULN-4236A*	SG2524BN	SG	ULQ-8124A§
RC4336DP	RAY	ULN-4336A*			
RC4436DP	RAY	ULN-4436A*	SG2524F	SIG	ULQ-8124R§
			SG2524N	SIG	ULQ-8124A§
S4534	AMI	UCN-4810A			
S4535	AMI	UCN-5818A	SG2525AJ	SG	ULQ-8125R§
			SG2525AN	SG	ULQ-8125A§
SA594N	SIG	UDQ-6118A-2§	SG2526J	SG	ULQ-8126R
SE5560F	SIG	ULS-8160R	SG2526N	SG	ULQ-8126A
SE5560N	SIG	ULS-8160A	SG2527AJ	SG	ULQ-8127R§
SE5561N	SIG	ULS-8161M	SG2527AN	SG	ULQ-8127A§
SE5562F	SIG	ULS-8162R§	SG2841N	SG	UDN-2841B
SE5562N	SIG	ULS-8162A§	SG3081N	SG	ULN-2081A
SE5563F	SIG	ULS-8163R§	SG3082N	SG	ULN-2082A
SE5563N	SIG	ULS-8163A§	SG3083N	SG	ULN-2083A
			SG3086N	SG	ULN-2086A
SFC2046E	THM	ULN-2046A	SG3146N	SG	ULN-2046A-1
SFC2054EC	THM	ULN-2054A	SG3183N	SG	ULN-2083A-1
SFC2086E	THM	ULN-2086A	SG3524BJ	SG	ULN-8124R§
			SG3524BN	SG	ULN-8124A§
SG741CT	SG	ULN-2151D*			
SG741CM	SG	ULN-2151M*	SG3524N	SIG	ULN-8124A§
SG1524BJ	SG	ULS-8124R§			
			SG3525AJ	SG	ULN-8125R§
SG1524F	SIG	ULS-8124R§	SG3525AN	SG	ULN-8125A§
			SG3526J	SG	ULN-8126R
			SG3526N	SG	ULN-8126A
SG1525AJ	SG	ULS-8125R§	SG3527AJ	SG	ULN-8127R§
SG1526J	SG	ULS-8162R	SG3527AN	SG	ULN-8127A§
SG1527AJ	SG	ULS-8127R§	SG3635P	SG	UDN-2935Z
SG2001J	SG	ULS-2001R	SG3821J	SG	ULS-2045H
SG2001N	SG	ULN-2001A	SG3821N	SG	ULN-2046A
SG2002J	SG	ULS-2002R	SG3822N	SG	ULN-2054A

*No longer manufactured. Listed for reference only.
§Sprague engineering bulletin in preparation.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement	Competitive Part Number	Manufacturer	Suggested Sprague Replacement
SG3851J	SG	ULS-2011R	SN75469J	TI	ULN-2024R
SG3851N	SG	ULN-2011A	SN75469N	TI	ULN-2024A
SG3852J	SG	ULS-2012R	SN75471P	TI	UDN-3611M†
SG3852N	SG	ULN-2012A	SN75472P	TI	UDN-3612M†
SG3853J	SG	ULS-2013R	SN75473P	TI	UDN-3613M†
SG3853N	SG	ULN-2013A	SN75474P	TI	UDN-3614M†
SG3854J	SG	ULS-2014R	SN75475P	TI	UDN-5712M†
SG3854N	SG	ULN-2014A	SN75476P	TI	UDN-5711M†
SG3886N	SG	ULN-2086A	SN75477P	TI	UDN-5722M†
SG6118N	SG	UDN-6118A	SN75478P	TI	UDN-5713M†
			SN75479P	TI	UDN-5714M†
SL3045C	PLS	ULS-2045R	SN75518N	TI	UCN-5818A§
SL3046C	PLS	ULN-2046A	SN75605	TI	UDN-2950Z
SL3054	PLS	ULN-2054A	SN76104N	TI	ULN-2120A*
SL3081D	PLS	ULN-2081A	SN76105N	TI	ULN-2122A*
SL3082D	PLS	ULN-2082A	SN76110N	TI	ULN-2128A*
SL3083E	PLS	ULN-2083A	SN76111N	TI	ULN-2121A*
SL3086	PLS	ULN-2086A	SN76113N	TI	ULN-2128A*
SL3145E	PLS	ULS-2045H	SN76115N	TI	ULN-3810A
SL3146E	PLS	ULN-2046A-1	SN76116N	TI	ULN-3812A
SL3183E	PLS	ULN-2083A-1	SN76130N	TI	ULN-2126A*
			SN76177ND	TI	ULN-2278B*
SN72741L	TI	ULN-2151D*	SN76226N	TI	ULN-2216A*
SN72741P	TI	ULN-2151M*	SN76227N	TI	ULN-2217A*
SN75064NE	TI	ULN-2064B	SN76228N	TI	ULN-2218A*
SN75065NE	TI	ULN-2065B	SN76242N	TI	ULN-2124A*
SN75066NE	TI	ULN-2066B	SN76243AN	TI	ULN-2127A*
SN75067NE	TI	ULN-2067B	SN76246N	TI	ULN-2228A*
SN75068NE	TI	ULN-2068B	SN76266N	TI	ULN-2266A*
SN75069NE	TI	ULN-2069B	SN76267N	TI	ULN-2267A*
SN75074NE	TI	ULN-2074B	SN76298N	TI	ULN-2298A*
SN75075NE	TI	ULN-2075B	SN76564N	TI	ULN-2264A*
SN75407P	TI	UDN-5732M	SN76565N	TI	ULN-2264A*
SN75437ND	TI	UDN-2541B	SN76591P	TI	ULN-2291M*
SN75466J	TI	ULN-2021R	SN76594P	TI	ULN-2294M*
SN75466N	TI	ULN-2021A	SN76635N	TI	ULN-2137A*
SN75467J	TI	ULN-2022R	SN76642N	TI	ULN-2111A
SN75467N	TI	ULN-2022A	SN76643N	TI	ULN-2111A
SN75468J	TI	ULN-2023R	SN76665N	TI	ULN-2165A*
SN75468N	TI	ULN-2023A			

*No longer manufactured. Listed for reference only.
†Some differences in specified switching speed with the Sprague device being superior for use with inductive loads.
§Sprague engineering bulletin in preparation.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement	Competitive Part Number	Manufacturer	Suggested Sprague Replacement
SN76669N	TI	ULN-2136A*	TD62104P	TOS	ULN-2004A
SN76675N	TI	ULN-2129A*	TD62479P	TOS	UDN-5714M
SN76678P	TI	ULN-2209M*	TD62703P	TOS	UHP-495*
SN76688ND	TI	ULN-2211B*	TD62705P	TOS	UHP-491*
SN76689N	TI	ULN-2289A*	TD62781AP	TOS	UDN-6118A-2
SN76883N	TI	ULX-2230A*	TD62782AP	TOS	UDN-6128A-2
SP3724QD	TI	TPQ-3724			
SP3725QD	TI	TPQ-3725	TDA1060	PE‡	ULN-8160A
			TDA1083	PE‡	ULN-2204A
TA7070P	TOS	ULN-2264A*	TDA1090	PE‡	ULN-2242A
TA7103P	TOS	ULN-2224A*	TDA1170	PE‡	ULN-2270Q
TA7141AP	TOS	ULN-2217A*	TDA1190	PE‡	ULX-3908Q*
TA7157P	TOS	ULN-3810A	TDA1190P	PE‡	ULN-2290B
TA7613P	TOS	ULN-2204A	TDA1190Z	PE‡	ULN-2290Q
			TDA1200	PE‡	ULN-2289A*
TAA930		ULN-2111A	TDA1230	PE‡	ULX-3801Q*
TBA395		ULN-2218A*	TDA1327	PE‡	ULN-2217A*
TBA396		ULN-2219A*	TDA2002	PE‡	ULN-3701Z
			TDA2002A	PE‡	ULN-3702Z
TCA3089	PE‡	ULN-2289A*	TDA2002H	PE‡	ULN-3701ZH
TCA3189	PE‡	ULN-3889A*	TDA2002V	PE‡	ULN-3701ZV
			TDA2003H	PE‡	ULN-3703ZH
TD62001AP	TOS	ULN-2001A	TDA2003V	PE‡	ULN-3703ZV
TD62001P	TOS	ULN-2001A	TDA2008V	PE‡	ULN-3702ZV
TD62002AP	TOS	ULN-2002A	TDA3189	PE‡	ULN-3889A*
TD62002P	TOS	ULN-2002A	TDA3190	PE‡	ULN-2290B
TD62003AP	TOS	ULN-2003A	TDA3190P	PE‡	ULN-2290B
TD62003P	TOS	ULN-2003A	TDA3950A	PE‡	ULN-2220A*
TD62004AP	TOS	ULN-2004A			
TD62004P	TOS	ULN-2004A	TID121	TI	TND-933
TD62064AP	TOS	ULN-2064B	TID122	TI	TND-940
TD62064P	TOS	ULN-2064B	TID123	TI	TND-938
TD62074AP	TOS	ULN-2074B	TID124	TI	TND-939
TD62074P	TOS	ULN-2074B	TL494CJ	TI	ULN-8194R§
TD62081AP	TOS	ULN-2801A	TL494CN	TI	ULN-8194A§
TD62082AP	TOS	ULN-2802A	TL494IJ	TI	ULQ-8194R§
TD62083	TOS	ULN-2803A	TL494IN	TI	ULQ-8194A§
TD62084AP	TOS	ULN-2804A	TL494MJ	TI	ULS-8194R§
TD62101P	TOS	ULN-2001A	TL495CJ	TI	ULN-8195R§
TD62103P	TOS	ULN-2003A	TL495CN	TI	ULN-8195A§

‡European registration; manufactured by various companies including ITT, Philips, SGS/ATES, Siemens, Thomson-CSF, AEG-Telefunken, and Valvo.
*No longer manufactured. Listed for reference only.
§Sprague engineering bulletin in preparation.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement	Competitive Part Number	Manufacturer	Suggested Sprague Replacement
TL495IJ	TI	ULQ-8195R§	TVCM-27	SPC	ULN-2298A*
TL495IN	TI	ULQ-8195A§	TVCM-28	SPC	ULN-2211B*
TL594CJ	TI	ULN-8194R§	TVCM-29	SPC	ULN-3812A
TL594CN	TI	ULN-8194A§	TVCM-30	SPC	ULN-2264A*
TL594IJ	TI	ULQ-8194R§	TVCM-33	SPC	ULN-2267A*
TL594IN	TI	ULQ-8194A§	TVCM-34	SPC	ULN-2269A*
TL594MJ	TI	ULS-8194R§	TVCM-35	SPC	ULN-2280B
TL595CJ	TI	ULN-8195R§	TVCM-36	SPC	ULN-3784B
TL595CN	TI	ULN-8195A§	TVCM-37	SPC	ULN-2285A*
TL595IJ	TI	ULQ-8195R§	TVCM-38	SPC	ULN-2285P*
TL595IN	TI	ULQ-8195A§	TVCM-39	SPC	ULN-2289A*
TL595MJ	TI	ULS-8195R§	TVCM-40	SPC	ULN-2298A*
			TVCM-62	SPC	ULN-3812A
TVCM-1	SPC	ULN-2114W*	TVCM-65	SPC	ULN-2278B*
TVCM-2	SPC	ULN-2114A*	TVCM-66	SPC	ULN-2046A
TVCM-3	SPC	ULN-2114K*	TVCM-67	SPC	ULN-2054A
TVCM-4	SPC	ULN-2111A	TVCM-68	SPC	ULN-2208M*
TVCM-5	SPC	ULN-2111A	TVCM-73	SPC	ULN-3810A
TVCM-6	SPC	ULN-2120A*			
TVCM-7	SPC	ULN-2122A*	U5E737394	FSC	ULN-2114W*
TVCM-8	SPC	ULN-2124A*	U5E7746394	FSC	ULN-2114W*
TVCM-9	SPC	ULN-2127A*	U6A758394	FSC	ULN-3812A
TVCM-10	SPC	ULN-2128A*	U6A7704394	FSC	ULN-2211B*
TVCM-11	SPC	ULN-2165A*	U6A7720394	FSC	ULN-2137A*
TVCM-12	SPC	ULN-2121A*	U6A7729394	FSC	ULN-2122A*
TVCM-13	SPC	ULN-2126A*	U6A7732394	FSC	ULN-2120A*
TVCM-14	SPC	ULN-2131M*	U6A7746394	FSC	ULN-2114A*
TVCM-15	SPC	ULN-2125A*	U6A7767394	FSC	ULN-2128A*
TVCM-16	SPC	ULN-2129A*	U6A7781394	FSC	ULN-2127A*
TVCM-17	SPC	ULN-2135E*	U6B7780394	FSC	ULN-2124A*
TVCM-18	SPC	ULN-2136A*	U6E7729394	FSC	ULN-2122A*
TVCM-19	SPC	ULN-2137A*	U7F7064394	FSC	ULN-2264A*
TVCM-20	SPC	ULN-2209M*	U7F7065354	FSC	ULN-2165A*
TVCM-21	SPC	ULN-2224A*	U7F7065394	FSC	ULN-2165A*
TVCM-22	SPC	ULN-2228A*	U7F7075394	FSC	ULN-2129A*
TVCM-23	SPC	ULN-2274B*	U7F7729394	FSC	ULN-2122A*
TVCM-24	SPC	ULN-2276P*	U7F7732394	FSC	ULN-2120A*
TVCM-25	SPC	ULN-2278B*	U7F7746394	FSC	ULN-2114A*
TVCM-26	SPC	ULN-2278B*	U7F7767394	FSC	ULN-2128A*

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§Sprague engineering bulletin in preparation.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement	Competitive Part Number	Manufacturer	Suggested Sprague Replacement
U7F7780394	FSC	ULN-2124A*	UA3089PC	FSC	ULN-2289A*
U7F7781394	FSC	ULN-2127A*	UA7327	FSC	ULN-2270B
U8F7746394	FSC	ULN-2114W*			
U9A7746394	FSC	ULN-2114A*	UC1524AJ	UNI	ULS-8124R§
U9A7781394	FSC	ULN-2127A*	UC1525AJ	UNI	ULS-8125R§
U9B7780394	FSC	ULN-2124A*	UC1526J	UNI	ULS-8126R
U9C7065354	FSC	ULN-2165A*	UC1527AJ	UNI	ULS-8127R§
			UC2524AJ	UNI	ULQ-8124R§
U417B	TLF	ULN-2204A	UC2524AN	UNI	ULQ-8124A§
			UC2525AJ	UNI	ULQ-8125R§
UA704PC	FSC	ULN-2211B*	UC2525AN	UNI	ULQ-8125A§
UA705PC	FSC	ULN-3812A	UC2526J	UNI	ULQ-8126R
UA720PC	FSC	ULN-2137A*	UC2526N	UNI	ULQ-8126A
UA729PC	FSC	ULN-2122A*	UC2527AJ	UNI	ULQ-8127R§
UA732PC	FSC	ULN-2120A*	UC2527AN	UNI	ULQ-8127A§
UA737EC	FSC	ULN-2114K*	UC3524AJ	UNI	ULN-8124R§
UA739PC	FSC	ULN-2126A*	UC3524AN	UNI	ULN-8124A§
UA741CT	FSC	ULN-2151D*	UC3525AJ	UNI	ULN-8125R§
UA741CV	FSC	ULN-2151M*	UC3525AN	UNI	ULN-8125A§
UA746PC	FSC	ULN-2228A*	UC3526J	UNI	ULN-8126R
UA753TC	FSC	ULN-2209M*	UC3526N	UNI	ULN-8126A
UA758PC	FSC	ULN-3812A	UC3527AJ	UNI	ULN-8127R§
UA767PC	FSC	ULN-2128A*	UC3527AN	UNI	ULN-8127A§
UA780PC	FSC	ULN-2124A*	UC494ACJ	UNI	ULN-8194R§
UA781PC	FSC	ULN-2127A*	UC494ACN	UNI	ULN-8194A§
UA787PC	FSC	ULN-2162A*	UC494AJ	UNI	ULS-8194R§
UA1391TC	FSC	ULN-2191M*	UC495ACJ	UNI	ULN-8195R§
UA1394TC	FSC	ULN-2294M*	UC495ACN	UNI	ULN-8195A§
UA2136PC	FSC	ULN-2136A*	UC495AJ	UNI	ULS-8195R§
UA3045DM	FSC	ULS-2045H			
UA3046PC	FSC	ULN-2046A	UCN4810N	TI	UCN-4810A
UA3054PC	FSC	ULN-2054A	UDN2841NE	TI	UDN-2841B
UA3064PC	FSC	ULN-2264A*	UDN2845NE	TI	UDN-2845B
UA3065PC	FSC	ULN-2165A*	UDN5711N	TI	UDN-5711M
UA3067PC	FSC	ULN-2267A*	UDN5712N	TI	UDN-5712M
UA3075PC	FSC	ULN-2129A*	UDN5713N	TI	UDN-5713M
UA3066PC	FSC	ULN-2266A*	UDN5714N	TI	UDN-5714M
UA3067PC	FSC	ULN-2267A*			
UA3086PC	FSC	ULN-2086A*	UDN-6164A	SPR	UDN-6116A-1

*No longer manufactured. Listed for reference only.
§Sprague engineering bulletin in preparation.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement	Competitive Part Number	Manufacturer	Suggested Sprague Replacement
UDN-6184A	SPR	UDN-6118A-1	ULN-2114A	SPR	ULN-2228A*
ULN2001AJ	TI	ULN-2001R	ULN-2209V		ULN-2209M*
ULN2001AN	TI	ULN-2001A			
ULN2002AJ	TI	ULN-2002R	ULN-2210A	SPR	ULN-3810A
ULN2002AN	TI	ULN-2002A	ULN-2225P	SPR	ULN-2211B*
ULN2003AJ	TI	ULN-2003R	ULN-2226A	SPR	ULN-2224A*
ULN2003AN	TI	ULN-2003A	ULN-2244A	SPR	ULN-3812A
ULN2004AJ	TI	ULN-2004R	ULN-2245A	SPR	ULN-3812A
ULN2004AN	TI	ULN-2004A	ULN-2275P	SPR	ULN-2274B*
ULN2005AJ	TI	ULN-2005R	ULN-2277P	SPR	ULN-2278B*
ULN2005AN	TI	ULN-2005A	ULN-2281B	SPR	ULN-3784B
			ULN-2287A	SPR	ULN-2289A*
ULN2064NE	TI	ULN-2064B	ULN-2301M	SPR	ULN-2300M*
ULN2065NE	TI	ULN-2065B			
ULN2066NE	TI	ULN-2066B	ULN-3006M	SPR	UGN-3201M
ULN2067NE	TI	ULN-2067B	ULN-3006T	SPR	UGN-3019T
			ULN-3007M	SPR	UGN-3203M
ULN2068	MOT	ULN-2068B	ULN-3008M	SPR	UGN-3501M
			ULN-3008T	SPR	UCN-3501T
ULN2068NE	TI	ULN-2068B	ULN-3100M	SPR	UGN-3600M
ULN2069NE	TI	ULN-2069B	ULN-3101M	SPR	UGN-3601M
ULN2074NE	TI	ULN-2074B	ULN-3330Y-2	SPR	ULN-3330Y
ULN2075NE	TI	ULN-2075B	ULN-3905A	SPR	ULN-3914A
			ULS-3006T	SPR	UGS-3019T
ULN-2110A	SPR	ULN-3810A			
ULN-2113A	SPR	ULN-2111A	UPA2001C	NEC	ULN-2001A

*No longer manufactured. Listed for reference only.

Competitive Part Number	Manufacturer	Suggested Sprague Replacement	Competitive Part Number	Manufacturer	Suggested Sprague Replacement
UPA2002C	NEC	ULN-2002A	XR2204CP	EXR	ULN-2004A
UPA2003C	NEC	ULN-2003A	XR2205CP	EXR	ULN-2005A
UPA2004C	NEC	ULN-2004A	XR6118P	EXR	UDN-6118A
UPC324	NEC	ULN-4336A*	XR6128P	EXR	UDN-6128A
XR1310CP	EXR	ULN-3810A	ZN1060	FER	ULN-8160A
XR1800P	EXR	ULN-3812A			
			512	ITT	UHP-491*
XR2001CN	EXR	ULN-2001R	552	ITT	ULN-2001A
XR2001P	EXR	ULQ-2001A	554	ITT	ULN-2002A
XR2002CN	EXR	ULN-2002R	556	ITT	ULN-2003A
XR2002P	EXR	ULQ-2002A	652	ITT	ULN-2001A
XR2003CN	EXR	ULN-2003R	654	ITT	ULN-2002A
XR2003P	EXR	ULQ-2003A	656	ITT	ULN-2003A
XR2004CN	EXR	ULN-2004R			
XR2004P	EXR	ULQ-2004A	9665DC	FSC	ULN-2001R
XR2011CN	EXR	ULN-2011R	9665DM	FSC	ULS-2001R
XR2011CP	EXR	ULN-2011A	9665PC	FSC	ULN-2001A
XR2012CN	EXR	ULN-2012R	9666DC	FSC	ULN-2002R
XR2012CP	EXR	ULN-2012A	9666DM	FSC	ULS-2002R
XR2013CN	EXR	ULN-2013R	9666PC	FSC	ULN-2002A
XR2013CP	EXR	ULN-2013A	9667DC	FSC	ULN-2003R
XR2014CN	EXR	ULN-2014R	9667DM	FSC	ULS-2003R
XR2014CP	EXR	ULN-2014A	9667PC	FSC	ULN-2003A
XR2201CP	EXR	ULN-2001A	9668DC	FSC	ULN-2004R
XR2202CP	EXR	ULN-2002A	9668DM	FSC	ULS-2004R
XR2203CP	EXR	ULN-2003A	9668PC	FSC	ULN-2004A

*No longer manufactured. Listed for reference only.

HOW TO ORDER

TO PLACE AN ORDER, obtain price and delivery, or request additional technical literature, call or write your local sales office (see inside back cover) or:

From U.S.A.	Sprague Electric Co.
	Marshall Street
	North Adams, MA 01247
	(413) 664-4411
	Telex: 710-369-1360
From Asia	Sprague World Trade Corp.
	Eastern Branch
	G.P.O. Box 4289
	Hong Kong
	3-7440010
	Telex: 780 433 95
From Europe	Sprague World Trade Corp.
	3 Chemin de Tavernay
	1218 Grand Saconex
	Geneva, Switzerland
	022-98-4021
	Telex: 23469

REQUESTS FOR additional technical information on standard or custom devices may be sent to the appropriate manufacturing facility:

For all monolithic integrated circuits except Hall effect devices,

> Sprague Electric Co.
> 115 Northeast Cutoff
> Worcester, MA 01606
> (617) 853-5000
> Telex: 710-340-6304

For discrete semiconductors and Hall Effect devices,

> Sprague Electric Co.
> 70 Pembroke Road
> Concord, NH 03301
> (603) 224-1961
> Telex: 710-361-1495

SPRAGUE FACILITIES

Sprague Electric Company manufactures active and passive components in 15 locations in the United States and in five countries in Europe and the Far East. Headquarters of the Semiconductor Division is in Worcester, Mass. All semiconductor wafer fabrication is done in the Worcester plant, as are all

services integral to its support. Volume assembly operations are located both in Worcester and in Manila, Republic of the Philippines. Sales offices and sales representatives are located throughout the United States and Canada, Latin America, Europe, Japan, Africa, and the Far East.
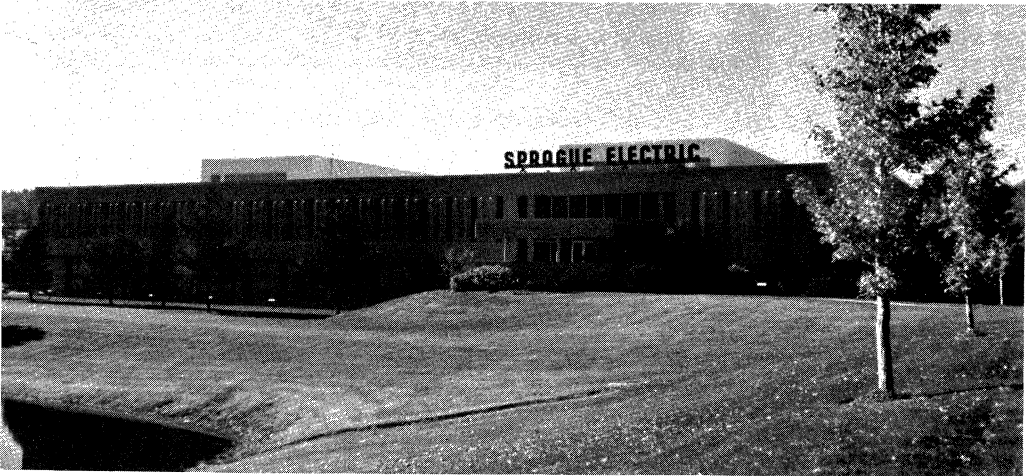
INTEGRATED CIRCUIT OPERATIONS, Worcester, Massachusetts

Semiconductor Operations

The integrated circuit operation of the Sprague Electric Semiconductor Division is located in a modern 115,000 square-foot plant in Worcester, Mass. Discrete components, such as transistors and diodes, and Hall Effect integrated circuits are manufactured at the division's Concord, N.H., plant, which occupies 30,000 square feet.

Sprague Electric is a leading manufacturer of volume integrated circuits serving the consumer, industrial controls, and peripherals markets. Production process technologies include complementary metal-gate MOS, high-voltage and high-current bipolar, and high-performance bipolar linear. This breadth of process technology enables Sprague Electric to manufacture optimal cost-performance integrated circuits.
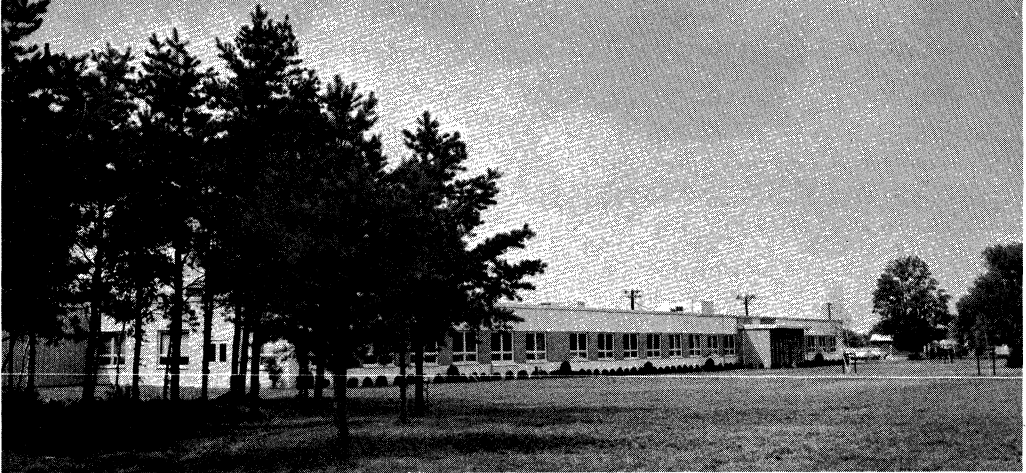
TRANSISTOR OPERATIONS, Concord, New Hampshire

How Integrated Circuits are Shipped

Integrated circuits are shipped in one of these carriers:

A-Channel Anti-Static Plastic Tubing
TO-220 Plastic Magazine
Individual Plastic Box

Integrated circuit chips are shipped in either un-scribed wafer form or individually partitioned in a plastic box.

Quality Control and Reliability

All critical points in the manufacturing processes of Sprague Electric integrated circuits are carefully monitored for compliance to engineering specifications. Electrical tests are made on 100% of the parts by automatic test systems. Lot sampling assures meeting customer A.Q.L. requirements. Calibration of test standards and equipment is performed at periodic intervals in order to maintain test accuracy.

Sprague Electric Company conducts a continuing reliability assurance program to detect deviations in device characteristics. Test samples are taken at random from each lot and are subjected to testing for performance evaluation and specification compliance. Routinely, finished samples are subjected to all electrical performance tests. A copy of the quality control inspection plan used for specific integrated circuits is available on request.

ENGINEERING BULLETINS

The information in this data book is equivalent to the Sprague Engineering Bulletins listed below. If an individual bulletin and this data book are compared, the latest revision takes precedence. For example, data on the UCN-4805A, described in Chapter 4, supersedes Bulletin 26181, which is presently in print. If that bulletin is revised to match this data book, it will carry the 'A' revision letter. If revisions beyond what appear here are later incorporated, the bulletin would then bear a 'B' revision letter.

Part Number	Bulletin Number		Part Number	Bulletin Number	
UHC/UHD-400 through 433-1	29300.1	3P	ULN-2249A	27121.10	
UHP-400 through 433-1	29300B	2P	ULN-2260A	27119.2	
UHC/UHD-500 through 533	29300.1	3P	ULN-2270B and 2270Q	27124.10	
UHP-500 through 533	29300B	2P	ULN-2280B	27117.11A	
TPP-1000 and 2000	29714A		ULN-2283B and 2283B-1	27117.21	2P
SG 1526J	27466.10		ULN-2290B and 2290Q	27110.32	2P
ULN-2001A through 2015A	29304C		ULN-2350C and 2351C	27405	
ULS-2001H through 2015H	29304.1B		ULN-2401A	27460	
ULS-2001R through 2015R	29034.1B		ULN-2429A	27461	
ULN-2021A through 2025A	29304C		ULN-2430M	27462	
ULS-2021H through 2025H	29304.1B		ULN-2435A and 2445A	27460.10	
ULN-2031A through 2033A	29710A	2P	ULN-2455A	27460.10	
ULS-2045H	29707	2P	TPQ-2483 and 2484	29711A	
ULN-2046A	29707	2P	SG 2526J	27466.10	
ULN-2046A-1	—		UDN-2541B/W and UDN-2542B/W	29317	
ULN-2047A	29712	2P	UDN-2580A through 2588A	29316	
ULN-2054A	29708A	2P	UDN-2595A	29320	
ULN-2061M and 2062M	29305C		ULN-2810A through 2815A	29304.3A	2P
ULN-2064B through 2077B	29305C		ULS-2801H through 2815H	29304.4A	
ULS-2064H through 2077H	29305.1		ULS-2801R through 2815R	29304.4A	
ULN-2081A and 2082A	29709		ULN-2821A through 2825A	29304.3A	2P
ULN-2083A	29713	2P	ULS-2821H through 2825H	29304.4A	
ULN-2083A-1	—		UDN-2841B and 2845B	29314A	
ULS-2083H	29713	2P	UDN-2878W and 2879W	29305.10	
ULN-2086A	—		UTN-2886B and 2888A	29401	2P
ULN-2111A	27102E	2P	TPQ-2906 and 2907	29711A	
ULN-2140A	29015.210A	2P	UDN-2935Z	29318.3	
ULS-2140H	29015.210A	2P	UDN-2949Z	29318A	
ULN-2204A	27121.50A		UDN-2950Z	29318.3	
TPQ-2221 and 2222	29711A		UDN-2952B and 2952W	29319	
ULN-2240A	27121.62		UDN-2956A and 2957A	29309A	2P
ULN-2241A	27121.61A		UDQ-2956R and 2957R	29309.1A	
ULN-2242A	27121.60A		UDN-2975W and 2976W	29319.10	
ULN-2243A	27105.1				

NOTE: 2P (2nd printing) indicates minor changes and/or corrections not normally affecting device performance.

ENGINEERING BULLETINS (Continued)

Part Number	Bulletin Number		Part Number	Bulletin Number	
UDN-2981A through 2984A	29310A		UCN-4401A	26180A	2P
UDS-2981H through 2984H	29310.1	2P	UCS-4401H	26180.1	
TPP-3000	29714A		UCN-4801A	26180A	2P
UGN-3013T	27603B		UCS-4801H	26180.1	
UGN/UGS-3019T/U	27601B		UCN-4805A	26181A	
UGN/UGS-3020T	27602A		UCN-4807A and 4808A	26186	
UGN/UGS-3030T/U	27606A		UCN-4810A	26182A	
UGN-3040T	27607		UCS-4810H	26182.1	
UGN/UGS-3075T/U	27608		UCN-4815A	26183	2P
UGN/UGS-3076T/U	27609		UCN-4815H	26183.1	
UGN-3201M and 3203M	27604		UCN-4821A through 4823A	26185	2P
UGN-3220S	27605		UCS-4821H through 4823H	26185.1	
ULN-3310D/T	27481		NE/SE 5560F and 5560N	27466A	
ULN-3330D/T/Y	27480B		NE 5561F	27466.1	
UGN-3501M	27500.1	2P	UDN-5703A through 5707A	29306	2P
UGN-3501T	27500	2P	UDS-5703H through 5707H	29306.1	2P
SG 3526J	27466.10		UDN-5711M through 5714M	29307A	2P
UGN-3600M and 3601M	27120B		UDS-5711H through 5714H	29307.1	
UDN-3611M through 3614M	29308	2P	UDN-5722M	29307.2	
UDS-3611H through 3614H	29308.1		UDN-5732M	29307.4	
ULN-3701Z	27117.31		UDN-5733M	29306	2P
ULN-3702Z	27117.33		UDS-5733H	29306.1	2P
ULN-3703Z	27117.34		UDN-5742M	29307.4	
ULN-3705M	27117.23		UDS-5791H	29315.1A	
TPQ-3724 through 3725A	29711A		TPQ-6001 through 6100A	29711A	
ULN-3784B	27117.12		UDN-6116A through 6128R-2	29313B	2P
TPQ-3798 and 3799	29711A		UDN-6138A through 6148A-2	29313B	2P
ULN-3804A	27121.52		TPQ-6501 and 6502	29711A	
ULN-3809A	27109.112		UDN-6510A/R and 6514A/R	29313.3	
ULN-3810A	27109.113		TPQ-6600 through 6700	29711A	
ULN-3812A	27109.114		UDN-7180A through 7186A	29311A	2P
ULN-3838A	27121.53		ULN-8126A and 8126R	27466.10	2P
ULN-3840A	27121.64		ULQ-8126A and 8126R	27466.10	2P
ULN-3859A	27105.10		ULS-8126R	27466.10	2P
TPQ-3904 and 3906	29711A		ULN-8160A and 8160R	27466A	
TPP-4000	29714A		ULS-8160R	27466A	
UCN-4202A and 4203A	26184A		ULN-8161M	27466.1	

NOTE: 2P (2nd printing) indicates minor changes and/or corrections not normally affecting device performance.

NOTES

2

SECTION 2 — HIGH-VOLTAGE INTERFACE DRIVERS

SELECTION GUIDE TO HIGH-VOLTAGE INTERFACE DRIVERS

| Device Type | Absolute Maximum Ratings | | Outputs |
	I_{OUT}	V_{OUT}	
UHP-500 through 533	500 mA	100 V	Sink 4
UCN-4823A	500 mA	100 V	Sink 8
UDN-6116A/R	−40 mA	85 V	Source 6
UDN-6116A-1	−40 mA	115 V	Source 6
UDN-6116A/R-2	−40 mA	65 V	Source 6
UDN-6118A/R	−40 mA	85 V	Source 8
UDN-6118A-1	−40 mA	115 V	Source 8
UDN-6118A/R-2	−40 mA	65 V	Source 8
UDN-6126A/R	−40 mA	85 V	Source 6
UDN-6126A-1	−40 mA	115 V	Source 6
UDN-6126A/R-2	−40 mA	65 V	Source 6
UDN-6128A/R	−40 mA	85 V	Source 8
UDN-6128A-1	−40 mA	115 V	Source 8
UDN-6128A/R-2	−40 mA	65 V	Source 8
UDN-6138A	−40 mA	±40 V	Source 8
UDN-6138A-2	−40 mA	±30 V	Source 8
UDN-6148A	−40 mA	±40 V	Source 8
UDN-6148A-2	−40 mA	±30 V	Source 8
UDN-6510A/R	−40 mA	200V	Source 8
UDN-6514A/R	−40 mA	140 V	Source 8
UDN-7180A	20 mA	−115 V	Sink 8
UDN-7180A	20 mA	−115 V	Sink 8
UDN-7183A	3.25 mA	−115 V	Sink 8
UDN-7184A	2.0 mA	−115 V	Sink 8
UDN-7186A	1.0 mA	−115 V	Sink 8

SERIES UDN-6100A AND UDN-6100R FLUORESCENT DISPLAY DRIVERS

2

FEATURES
- Digit or Segment Drivers
- Low Input Current
- Integral Output Pull-Down Resistors
- high Output Breakdown Voltage
- Single or Split Supply Operation

Dwg. No. A-9643A

UDN-6116*
UDN-6126*

CONSISTING of six or eight NPN Darlington output stages and the associated common-emitter input stages, these drivers are designed to interface between low-level digital logic and vacuum fluorescent displays. All devices are capable of driving the digits and/or segments of these displays and are designed to permit all outputs to be activated simultaneously. Pull-down resistors are incorporated into each output and no external components are required for most fluorescent display applications. The highest voltage parts (suffix A-1) are also used in gas-discharge display applications as anode (digit) drivers.

Twenty-four standard devices are listed, so that a circuit designer may select the optimum device for his application. Input characteristics, number of drivers, package style, and output voltage are tabulated for each device in the Device Type Number Designation chart. With any device, the output load is activated when the input is pulled towards the positive supply (active 'high'). All units operate over the temperature range of −20°C to +85°C.

Always specify complete part number, such as:

UD N − 6116 A − 2

— **INSTRUCTIONS:** SELECTED VERSION. SEE TYPE NUMBER DESIGNATION, NEXT PAGE.

— **PACKAGE:** A = PLASTIC DIP
R = CERAMIC DIP

— **DEVICE TYPE.**

— **OPERATING TEMPERATURE RANGE.** N = −20°C to +85°C

— **FAMILY.** UD = DIGITAL DRIVERS

Dwg. No. A-9641A

UDN-6118*
UDN-6128*
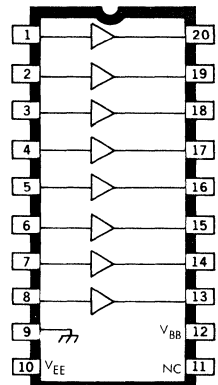
DWG. NO. A-11,222

UDN-6138*
UDN-6148*

DEVICE TYPE NUMBER DESIGNATION

Input Compatibility	No. of Drivers	V_{OUT}	No. of Pins	Type Number	
				Plastic DIP	Ceramic DIP
5V TTL, CMOS	6	60 V	16	UDN-6116A-2	UDN-6116R-2
		80 V	16	UDN-6116A	UDN-6116R
		110 V	16	UDN-6116A-1	—
	8	60 V	18	UDN-6118A-2	UDN-6118R-2
		80 V	18	UDN-6118A	UDN-6118R
		110 V	18	UDN-6118A-1	—
		±30 V	20	UDN-6138A-2	—
		±40 V	20	UDN-6138A	—
6—15V CMOS, PMOS	6	60 V	16	UDN-6126A-2	UDN-6126R-2
		80 V	16	UDN-6126A	UDN-6126R
		110 V	16	UDN-6126A-1	—
	8	60 V	18	UDN-6128A-2	UDN-6128R-2
		80 V	18	UDN-6128A	UDN-6128R
		110 V	18	UDN-6128A-1	—
		±30 V	20	UDN-6148A-2	—
		±40 V	20	UDN-6148A	—

ABSOLUTE MAXIMUM RATINGS at T_A = +25°C

(Voltages are with reference to ground unless otherwise shown)

Supply Voltage, V_{BB} (all devices, suffix A or R)..........................85 V
(UDN-6138/48A or R, ref. V_{EE})......................85 V
(all devices, suffix A-1)............................115 V
(all devices, suffix A-2 or R-2)......................65 V
(UDN-6138/48A-2 or R-2, ref. V_{EE})...................65 V
Supply Voltage, V_{EE} (UDN-6138/48 all suffixes).........................−40 V
Input Voltage, V_{IN} (all devices) ....20 V
(UDN-6138/48 all suffixes, ref. V_{EE})...................55 V
Output Current, I_{OUT}...−40 mA
Allowable Package Power Dissipation, P_D.........................See Graph
Operating Temperature Range, T_A.........................−20°C to +85°C
Storage Temperature Range, T_S.........................−55°C to +150°C

DWG. NO. A-11,224
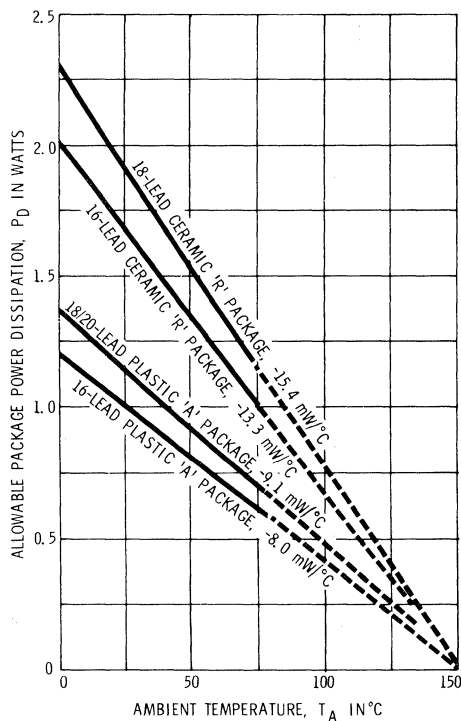
ELECTRICAL CHARACTERISTICS (over operating temperature range)

Note: All Values Specified At ——

Suffixes	A	R	A-1	A-2	R-2	
V_{BB} =	80	80	110	60	60	Volts
*V_{EE} =	0	0	NA	0	0	Volts

*UDN-6138 and UDN-6148

Characteristic	Symbol	Applicable Devices		Test Conditions	Limits			Units
		Basic Part No.	Suffix		Min.	Typ.	Max.	
Output Leakage Current	I_{OUT}	All	All	V_{IN} = 0.4 V	—	—	15	μA
Output OFF Voltage	V_{OUT}	All	All	V_{IN} = 0.4 V	—	—	1.0	V
Output Pull-Down Current	I_{OUT}	All	A or R	Input Open,	450	650	1100	μA
			A-1	V_{OUT} = V_{BB}	600	900	1500	μA
			A-2 or R-2		350	500	775	μA
Output ON Voltage	V_{OUT}	UDN-6116/18/38	A or R	V_{IN} = 2.4 V,	77	78	—	V
			A-1	I_{OUT} = —25 mA	107	108	—	V
			A-2 or R-2		57	58	—	V
		UDN-6126/28/48	A or R	V_{IN} = 4.0 V,	77	78	—	V
			A-1	I_{OUT} = —25 mA	107	108	—	V
			A-2 or R-2		57	58	—	V
Input ON Current	I_{IN}	UDN-6116/18/38	All	V_{IN} = 2.4 V	—	120	225	μA
				V_{IN} = 5.0 V	—	375	650	μA
		UDN-6126/28/48	All	V_{IN} = 4.0 V	—	130	250	μA
				V_{IN} = 15 V	—	675	1150	μA
Supply Current	I_{BB}	All	All	All Inputs Open	—	10	100	μA
		UDN-6116	A or R	All Inputs = 2.4 V	—	5.0	7.5	mA
			A-1	Two Inputs = 2.4 V	—	2.5	4.5	mA
			A-2 or R-2	All Inputs = 2.4 V	—	4.0	6.0	mA
		UDN-6118/38	A or R	All Inputs = 2.4 V	—	6.0	9.0	mA
			A-1	Two Inputs = 2.4 V	—	2.5	4.5	mA
			A-2 or R-2	All Inputs = 2.4 V	—	5.5	8.0	mA
		UDN-6126	A or R	All Inputs = 4.0 V	—	5.0	7.5	mA
			A-1	Two Inputs = 4.0 V	—	2.5	4.5	mA
			A-2 or R-2	All Inputs = 4.0 V	—	4.0	6.0	mA
		UDN-6128/48	A or R	All Inputs = 4.0 V	—	6.0	9.0	mA
			A-1	Two Inputs = 4.0 V	—	2.5	4.5	mA
			A-2 or R-2	All Inputs = 4.0 V	—	5.5	8.0	mA

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	V_{BB}	UDN-6116/18/26/28	A or R		5.0	—	70	V
			A-1		5.0	—	100	V
			A-2 or R-2		5.0	—	50	V
		UDN-6138/48	A		5.0	—	40	V
			A-2		5.0	—	30	V
	V_{EE}	UDN-6138/48	A		0	—	—40	V
			A-2		0	—	—30	V
Input ON Voltage	V_{IN}	UDN-6116/18/38	All		2.4	—	15	V
		UDN-6126/28/48	All		4.0	—	15	V
Output ON Current	I_{OUT}	All	All		—	—	—25	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

SERIES UDN-6100A AND UDN-6100R
FLUORESCENT DISPLAY DRIVERS

PARTIAL SCHEMATIC

**One Driver
(All Types)**

Type (All Suffixes)	R_{IN}	R_B
UDN-6116/18/38	10 kΩ	30 kΩ
UDN-6126/28/48	20 kΩ	20 kΩ
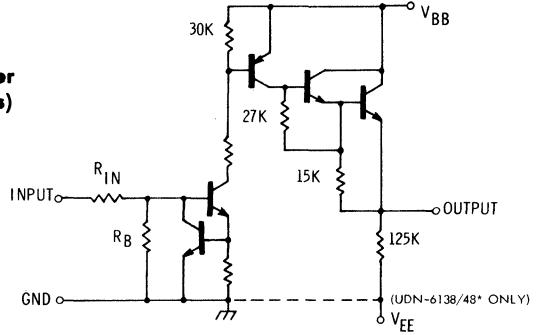
DWG.NO. A-10,592C

TYPICAL MULTIPLEXED FLUORESCENT DISPLAY
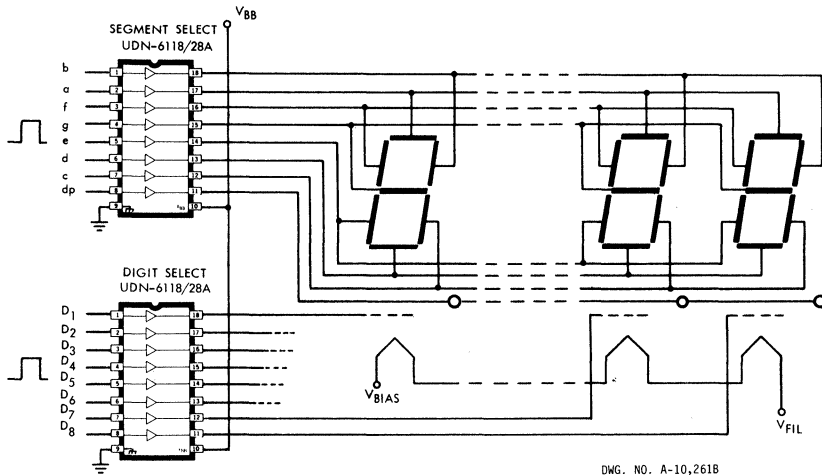
DWG. NO. A-10,261B

UDN-6510A/R AND UDN-6514A/R
HIGH-VOLTAGE SOURCE DRIVERS

FEATURES

- TTL/MOS-Compatible Inputs
- High Output-Breakdown Voltage
- 40 mA Output-Current Capability
- Low Power Dissipation
- Reliable Monolithic Construction

2

E ASY, EFFECTIVE INTERFACE for low-level TTL or MOS circuitry and high-voltage loads is available with Sprague UDN-6510A/R and UDN-6514A/R bipolar integrated circuits. These eight-channel devices drive the anodes of gas-discharge displays or the grids and anodes of large, multiplexed dot-matrix vacuum-fluorescent display panels.

Types UDN-6510A and UDN-6510R supply an output-voltage swing of up to 100 V with a maximum V_{BB} of 200 V. Typically, the output is switched between +100 V and +180 V.

Types UDN-6514A and UDN-6514R can switch output-voltage levels from ground to +135 V with appropriate pull-down circuitry and a maximum supply voltage of +140 V.

Each device in the series has eight independent drivers made up of switched constant-current level

Dwg. No. A-9641A
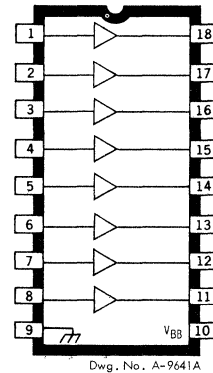
shifters and PNP/NPN driver stages. Driver inputs operate with open-drain PMOS or CMOS, or with open-collector or standard TTL.

Types UDN-6510R and UDN-6514R are furnished in 18-pin dual in-line industrial-grade, hermetically sealed ceramic packages. Types UDN-6510A and UDN-6514A are supplied in inexpensive 18-pin dual in-line plastic packages. To simplify applications designs, all units have input connections on one side of the package and output pins on the other. All devices are rated for operation over the temperature range of −20°C to +85°C.

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C
(V_{REF} = GROUND unless otherwise specified)

Supply Voltage, V_{BB} (UDN-6510A/R) .... 200 V

(UDN-6514A/R) .... 140 V

Output OFF Voltage (V_{REF} = V_{BB}), V_{OUT} (UDN-6510A/R) .... −100 V

Input Voltage, V_{IN} .... 20 V

Output Current, I_{OUT} .... −40 mA

Package Power Dissipation, P_D .... See Graph

Operating Temperature Range, T_A .... −20°C to +85°C

Storage Temperature Range, T_S .... −55°C to +150°C

PARTIAL SCHEMATIC
One Driver (All Types)

Dwg. No. A-11,657

PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE

Dwg. No. A-11,658

*Caution: The high input impedance of these devices makes them suscepti-
ble to static discharge damage associated with handling and testing.
Techniques similar to those used for handling MOS devices should be
employed.*

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{BB} = 200 V (UDN-6510A/R) or 140 V (UDN-6514A/R), all voltage measurements are referenced to ground (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Min.	Typ.	Max.	Units
Output Leakage Current	I_{OUT}	UDN-6510A/R	V_{OUT} = 100 V, V_{IN} = 0.4 V, T_A = +70°C	—	—	15	μA
		UDN-6514A/R	V_{OUT} = 0 V, V_{IN} = 0.4 V, T_A = +70°C	—	—	15	μA
Output ON Voltage	V_{OUT}	UDN-6510A/R	V_{IN} = 2.4 V, I_{OUT} = −25 mA	195	197	—	V
		UDN-6514A/R	V_{IN} = 2.4 V, I_{OUT} = −25 mA	135	137	—	V
Input ON Current	I_{IN}	All	V_{IN} = 2.4 V	—	120	225	μA
			V_{IN} = 5.0 V	—	375	650	μA
Supply Current	I_{BB}	All	All inputs open	—	10	100	μA
			One input = 3.5 V	—	—	500	μA

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	V_{BB}	UDN-6510A/R		55	—	180	V
		UDN-6514A/R		55	—	130	V
Output OFF Voltage	V_{OUT}	UDN-6510A/R	Reference V_{BB}	—	—	−80	V
Input ON Voltage	V_{IN}	All		2.4	—	15	V
Output ON Current	I_{OUT}	All		—	—	−25	mA

NOTE: Negative current is defined as coming out of the specified device pin.

TYPICAL PLASMA GAS-DISCHARGE DISPLAY APPLICATION
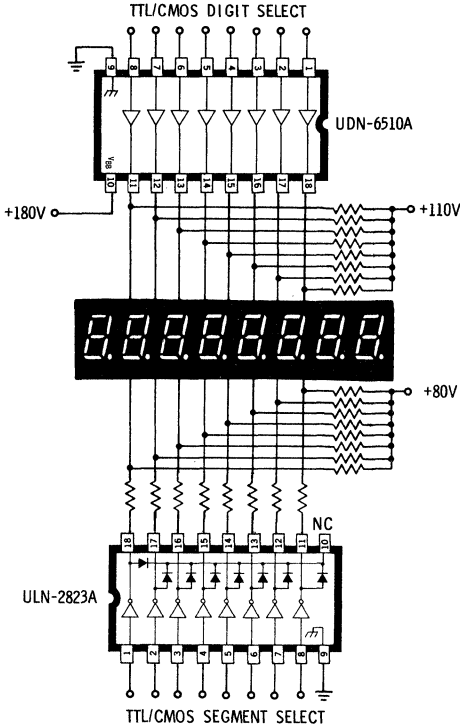
EQUIVALENT CIRCUIT

Dwg. No. A-11,655

Dwg. No. A-11,656

2

MULTIPLEXED DOT-MATRIX VACUUM-FLUORESCENT DISPLAY APPLICATION
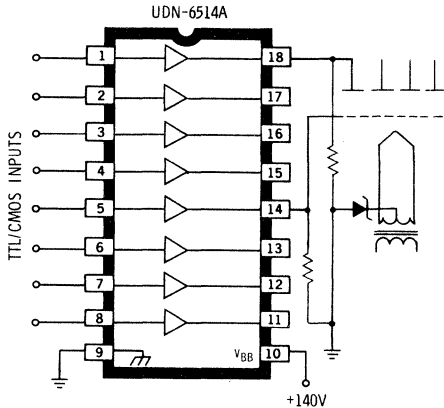
Dwg. No. A-11,659

2—9

SERIES UDN-7180A

GAS DISCHARGE DISPLAY SEGMENT DRIVERS

FEATURES

- Reliable Monolithic Construction
- High Output Breakdown Voltage
- Low Power
- TTL/MOS Compatible Inputs
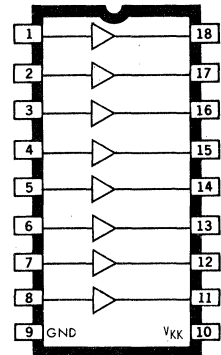
Dwg. No. A-9640A

Description

Series UDN-7180A segment drivers are monolithic high-voltage bipolar integrated circuits for interfacing between MOS or other low-voltage circuits and the cathode of gas-discharge display panels.

These drivers reduce substantially the number of discrete components required with panels (Beckman, Burroughs, Dale, Matsushita, NEC, Pantek, etc) in calculator, clock and instrumentation applications.

The UDN-7183A, UDN-7184A, and UDN-7186A drivers contain appropriate level shifting, signal amplification, current limiting, and output OFF-state voltage bias. The UDN-7180A driver requires external current limiting and is intended for higher-current applications or where individual outputs are operated at different current levels (i.e. with alpha-numeric displays). All inputs have pull-down resistors for direct connection to open-drain PMOS logic.

These devices provide output currents suitable for display segments in a wide variety of display sizes and number of display digits. Either a fixed split supply operation or a feedback-controlled scheme is allowed.

Applications

The Series UDN-7180A drivers can be used in a wide variety of low-level to high-voltage applications utilizing gas discharge displays such as those found in calculators, clocks, point-of-sale terminals, and instruments. Their high reliability combined with minimum size, ease of installation, and the cost advantages of a complete monolithic interface make them the ideal choice in many applications. A typical application showing the use of these devices, and their counterpart anode drivers, is shown.

ABSOLUTE MAXIMUM RATINGS at +25°C

Supply Voltage, V_{KK} . . . . −115 V

Input Voltage, V_{IN} . . . . +20 V

Output Current, I_{OUT}: UDN-7180A . . . . 20 mA

UDN-7183A . . . . 3.25 mA

UDN-7184A . . . . 2.0 mA

UDN-7186A . . . . 1.0 mA

Power Dissipation, P_D . . . . 1.13 W*

Operating Temperature Range, T_A . . . . −20°C to +85°C

Storage Temperature Range, T_S . . . . −65°C to +150°C

*Derate at the rate of 9.1 mW/°C above 25°C

Due to the high input impedance of these devices, they are susceptible to static discharge damage sometimes associated with handling and testing. Therefore, techniques similar to those used for handling MOS devices should be employed.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{KK} = 110 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Test Fig.	UDN-7180/83A Min.	Typ.	Max.	UDN-7184A Min.	Typ.	Max.	UDN-7186A Min.	Typ.	Max.	Units
Output ON Voltage UDN-7183/84/86A	V_{ON}	All inputs at 2.4 V	1	−100	−104	—	−98	−102	—	−97	−100	—	V
		All inputs at 2.4 V, V_{KK} = −70 V	1	—	−66	—	—	−65	—	—	−63	—	V
Output ON Voltage UDN-7180A	V_{ON}	All inputs at 2.4 V, I_{ON} = 14 mA		−105	−108	—	—	—	—	—	—	—	V
Output OFF Voltage	V_{OFF}	All inputs at 0.4 V, Reference V_{KK}	2	76	84	—	76	84	—	76	84	—	V
Output Current ($I_{LIMITING}$)	I_{ON}	All inputs at 2.4 V, V_{KK} = −110 V, Test output held at −60 V	3A	UDN-7183A only 1475	1850	2450	910	1140	1520	440	550	725	μA
Output Current (I_{SENSE})	I_{ON}	All inputs at 0.4 V, V_{KK} = −110 V, Test output held at −66 V	3B	−95	−120	−155	−65	−85	−115	−50	−65	−90	μA
Input High Current	I_{IH}	Test input at 2.4 V, Other inputs at 0 V	4	—	100	200	—	100	200	—	100	200	μA
Input Low Current	I_{IL}	Test input at 0.4 V, One input at 2.4 V, Other inputs at 0.4 V	5	—	1	10	—	1	10	—	1	10	μA
Supply Current	I_{KK}	All inputs at 0 V	6	—	−125	−175	—	−125	−175	—	−125	−175	μA

NOTES:
1. All voltage measurements are referenced to pin 9 unless otherwise specified.
2. All voltage measurements made with 10MΩ DVM or VTVM.
3. Recommended V_{KK} operating range: −85 to −110 V.
4. Positive (negative) current is defined as going into (coming out of) the specified device pin.

TEST CIRCUITS
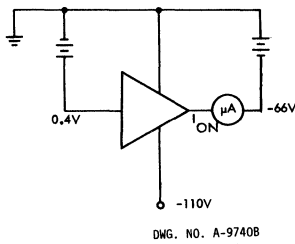
DWG. NO. A-9737A

FIGURE 1

DWG. NO. A-9738B

FIGURE 2

DWG. NO. A-9739B

FIGURE 3A

DWG. NO. A-9740B

FIGURE 3B

DWG. NO. A-9741A

FIGURE 4

DWG. NO. A-9742B

FIGURE 5

DWG. NO. A-9743

FIGURE 6

2—12

2

PARTIAL SCHEMATIC

	R_1 (kΩ)	R_2 (kΩ)
7180	350	0
7183	350	25
7184	480	40
7186	620	80

INPUT OUTPUT

① 18 K ⑱

GND ⑨

200K

700K

R_1

R_2

27 K

V_{KK} ⑩

COMMON BIASING NETWORK | ONE OF EIGHT DRIVERS

Dwg.No. A-9644C

TYPICAL APPLICATION

V_{BB}
DIGIT DRIVER
UDN-6118A-1
GND

V_{SS}

MOS
LOGIC

— ANODES —
8-DIGIT
GAS-DISCHARGE DISPLAY
— CATHODES —

V_{DD}

GND
SEGMENT DRIVER
UDN-7183A
V_{KK}

Dwg.No. A-9646A
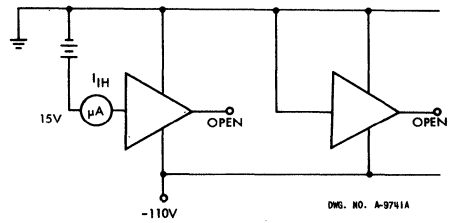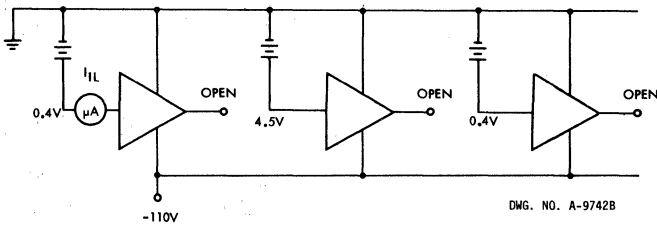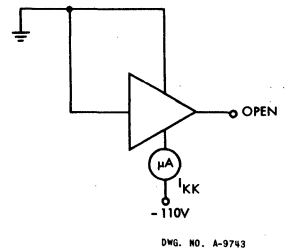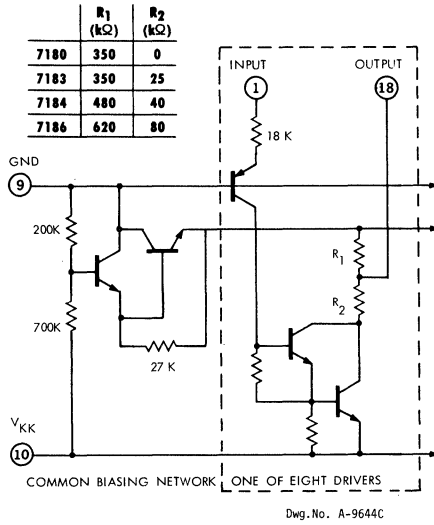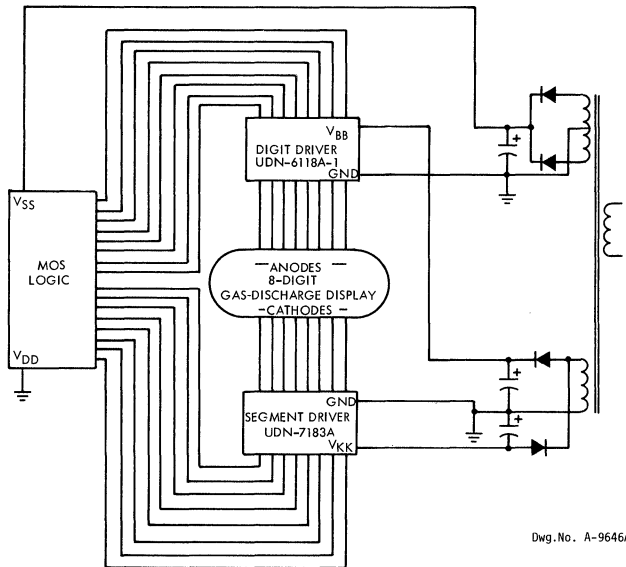
TYPICAL SIX-DIGIT CLOCK

DWG. NO. A-9751A

2

ONE SCAN CYCLE

DIGIT 1 — ON
DIGIT 2 — ON
DIGIT 3 — ON
DIGIT 4 — ON
SEG a
SEG b
SEG c
SEG d
SEG e
SEG f
SEG g

INTERDIGIT BLANKING INTERVAL

DWG. NO. A-11,096

ACTUAL OUTPUT CIRCUITS

V_{BB}

1/8 UDN-6118A-1

125 K

-V REF R_1 (-26V)

R_2

1/8 UDN-7183A

EQUIVALENT CIRCUITS

(+100V)

DIGIT SWITCH

125 K

350 K

25 K

SEGMENT SWITCH

(-100V)

Dwg.No. A-11,094B
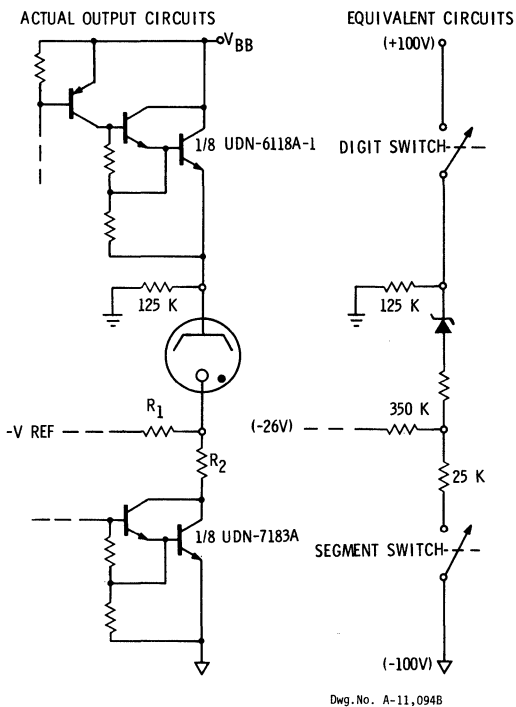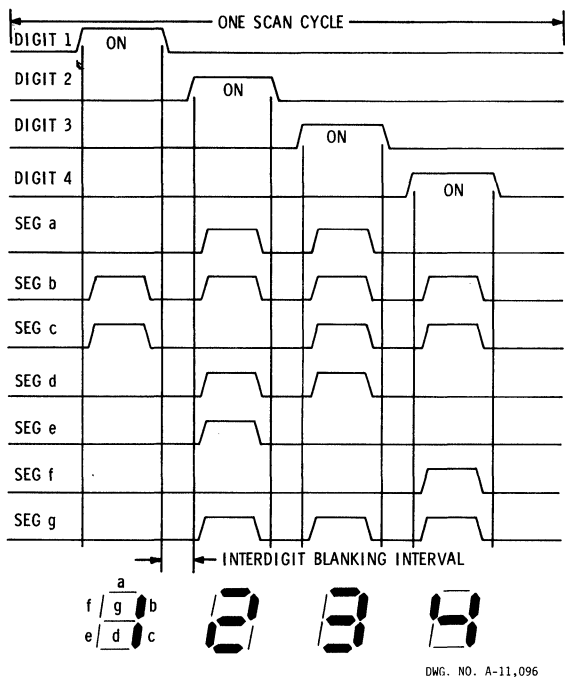
ANODE AND CATHODE WAVEFORMS

ANODE ON VOLTAGE

ANODE SELECT SIGNAL   50%   50%

OFF BIAS VOLTAGE

PANEL VOLTAGE DROP   CATHODE BLANKING OVERLAP

OFF BIAS VOLTAGE   50%

CATHODE SELECT SIGNAL   50%   50%

CATHODE ON VOLTAGE
REIONIZATION TIME

DIGIT PERIOD   CATHODE BLANKING INTERVAL

DWG. NO. A-11,095
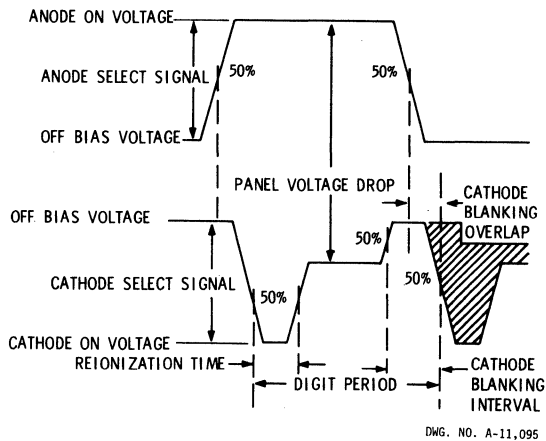
A MONOLITHIC IC SERIES
FOR GAS-DISCHARGE DISPLAY INTERFACE

Introduction

The switching of the high voltages necessary for display panels such as the Burroughs Panaplex® has long presented difficulties to the semiconductor industry – particularly to IC manufacturers. It is difficult to fabricate devices capable of sustaining 200 volts or greater with standard IC processes of today. Solutions to the high voltage gas discharge display interface also must be inexpensive as well as functional; this cost/simplicity factor prohibits most unusual or exotic circuit designs and/or IC processes.

The earliest (and a great many recent) gas discharge interface schemes used discrete components, but that has been an increasingly cumbersome and expensive solution. Competition at the system level has largely come from LEDs, and a great many standard ICs are available for the smaller LEDs. In most instances, the small displays have gone to LEDs. However, the larger display applications are still an opportunity for gas discharge since character size and cost are not directly related. The cost impact upon the potential for gas discharge displays in many systems is a function of interface complexity and cost, and it was to this end that a joint Sprague/Burroughs effort was launched.

Early Sprague/Burroughs meetings were held to define the relevant factors involved in such a program and provide the necessary insight for both parties into the capabilities of diode isolated ICs, the voltage and current requirements of the Panaplex displays, the need for minimization of power (battery systems), packaging of the circuits, component count and cost, etc. Add to this the potential for use with feedback controlled supplied, poorly regulated d-c supplies, the wide variety of numbers of display digits, the range of digit sizes (in use or contemplated), etc., and our task was not to be an easy one.

Our direction was determined by two factors: a history of fabricating 130-140 volt PN diode isolated display circuits, and a more recent effort to utilize compatible thin-film resistor technology. These factors, coupled with considerable expertise in designing and processing high voltage ICs, dictated an approach utilizing a split ($\pm$ 100 V) supply. The split supply would provide the 200 volts needed to ionize the display and the resistor capability would greatly aid the incorporation of functions previously done by discrete components – including both input and output (segment) current limiting, pulldown (open drain PMOS), pullup and pulldown reference for IC outputs, and a high impedance voltage divider for the output OFF bias. All level shifting is accomplished via use of PNP or NPN transistors, and the capacitors previously required were negated.

Figure 1

Dwg.No. A-9646A

2
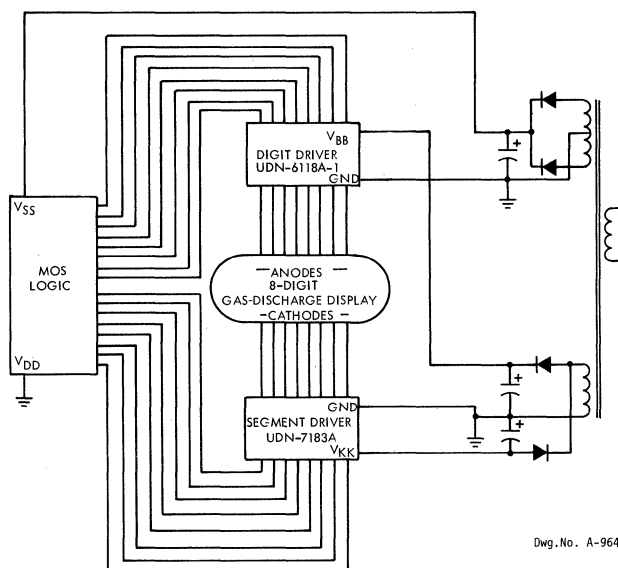
Basic Scheme

Replacing discrete components through incorporating their function into this IC series results in the block diagram of Figure 1 with its basic requirement for a single digit and single segment driver; a scheme capable of driving as many as eight digits and the eight segments. Additional digits or segments beyond the eight provided in an 18-lead DIP may be driven by combinations of packages beyond the minimum two necessary. Example: three ICs—two digit and one segment—will fulfill the needs of a 12 to 16 digit calculator.

Included in this series of high voltage interface are two digit driver packages: UDN-6116 (6-digit), and UDN-6118 (8-digit). Segment drivers include the UDN-7180, UDN-7183, UDN-7184, and UDN-7186, and the four offer current ranges compatible with display sizes from 0.250″ to 1″ panels, and others will be made available as needs are defined.

Digit Interface

The digit driver is the more complex of the two and its schematic is shown in Figure 2. Input address polarity is positive (active high in TTL parlance) and the circuit is designed to interface from TTL (4.5 volts from open collector—or using pull-up to V_{CC}), CMOS, PMOS, etc. Input current-limiting and one-half of the pull-down for open drain PMOS is the function of R_5; R_6 adds the second half of the pull-down to the ground bus. The protective value of R_4 and R_5 must be noted; a junction failure in Q_1 has the two resistors as a current limiter to the MOS (or TTL) output and will minimize the likelihood of destroying the low level logic outputs.

Input transistor Q_4 is a high voltage inverter and sinks the base current of PNP Q_3. A positive input (4.5 to 20 V) will turn on Q_4 and this base current (65 μA typ.) for PNO Q_3 will turn on the output Darlington (Q_1 and Q_2) and source digit current.

ELECTRICAL CHARACTERISTICS: $T_A = +25°C$, $V_{KK} = 110\,V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Test Fig.	UDN-7180/83A Min.	Typ.	Max.	UDN-7184A Min.	Typ.	Max.	UDN-7186A Min.	Typ.	Max.	Units
Output ON Voltage UDN-7183/84/86A	V_{ON}	All inputs at 2.4 V	1	−100	−104	—	−98	−102	—	−97	−100	—	V
		All inputs at 2.4 V, $V_{KK} = -70\,V$	1	—	−66	—	—	−65	—	—	−63	—	V
Output ON Voltage UDN-7180A	V_{ON}	All inputs at 2.4 V, $I_{ON} = 14\,mA$		−105	−108	—	—	—	—	—	—	—	V
Output OFF Voltage	V_{OFF}	All inputs at 0.4 V, Reference V_{KK}	2	76	84	—	76	84	—	76	84	—	V
Output Current ($I_{LIMITING}$)	I_{ON}	All inputs at 2.4 V, $V_{KK} = -110\,V$, Test output held at −60 V	3A	UDN-7183A only 1475	1850	2450	910	1140	1520	440	550	725	μA
Output Current (I_{SENSE})	I_{ON}	All inputs at 0.4 V, $V_{KK} = -110\,V$, Test output held at −66 V	3B	−95	−120	−155	−65	−85	−115	−50	−65	−90	μA
Input High Current	I_{IH}	Test input at 2.4 V, Other inputs at 0 V	4	—	100	200	—	100	200	—	100	200	μA
Input Low Current	I_{IL}	Test input at 0.4 V, One input at 2.4 V, Other inputs at 0.4 V	5	—	1	10	—	1	10	—	1	10	μA
Supply Current	I_{KK}	All inputs at 0 V	6	—	−125	−175	—	−125	−175	—	−125	−175	μA

NOTES:
1. All voltage measurements are referenced to pin 9 unless otherwise specified.
2. All voltage measurements made with 10MΩ DVM or VTVM.
3. Recommended V_{KK} operating range: −85 to −110 V.
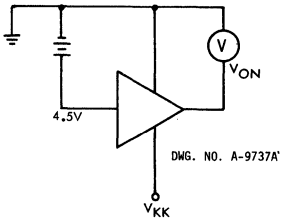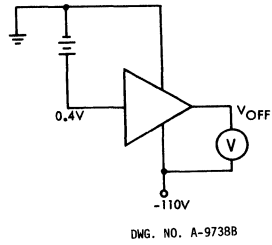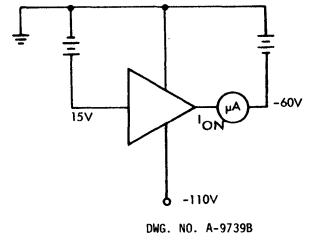4. Positive (negative) current is defined as going into (coming out of) the specified device pin.

PARTIAL SCHEMATIC
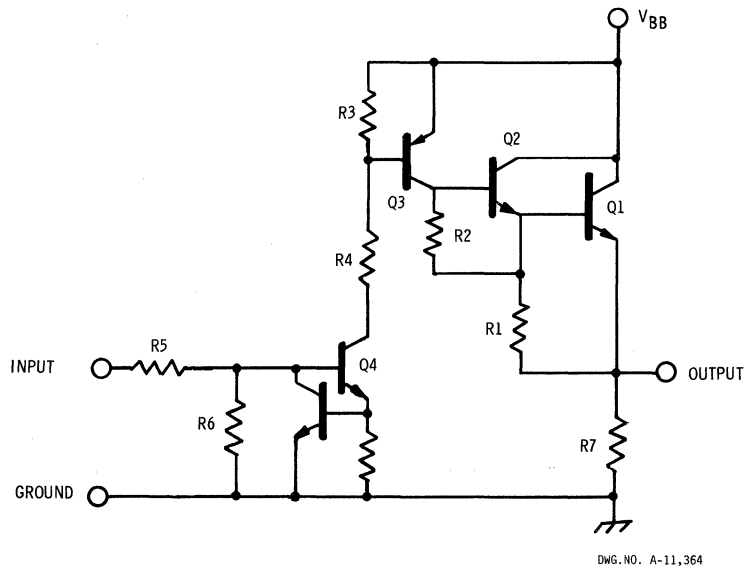
DWG. NO. A-11,364

Figure 2

Consistent ionization and extinguishing of the display panel is the result of the 60-75 volt swings available from both digit and segment ICs. The conditions that previously created problems for the direct MOS drive with minimal swings at the output have been very adequately handled with the increased output swings of the 6100/7100 series. Problems from leading zero blanking, low temperature, low ambient light, etc. which previously gave difficulty are well taken care of with this series of ICs.

Segment Interface

The segment driver circuit is shown in Figure 3 and the value of R_2 (segment limiting) is determined via masking for the appropriate display current. Its counterpart pull-up resistor R_1 is also changed to some known ratio of R_2. The ground terminal (#9) is referenced near, or connected directly to ground, and the V_{KK} line is typically a -90 to -100 volts.

The input PNP (Q_1) serves as a level translator and provides d-c level shifting to the output Darlington (Q_2 and Q_3). Emitter resistor (R_3) both limits the input current and furnished pull-down for open drain PMOS. An added intent is the measure of protection furnished the MOS by the very high impedance of R_3.

The basic switching function is the combination of PNP Q_1, Darlington Q_2 and Q_3, and the associated resistors R_1, R_2, and R_3. Address polarity is again active high. The input may be raised a maximum of 20 volts above ground and will function with input levels obtained from CMOS and open collector TTL (4.5 V).

PARTIAL SCHEMATIC
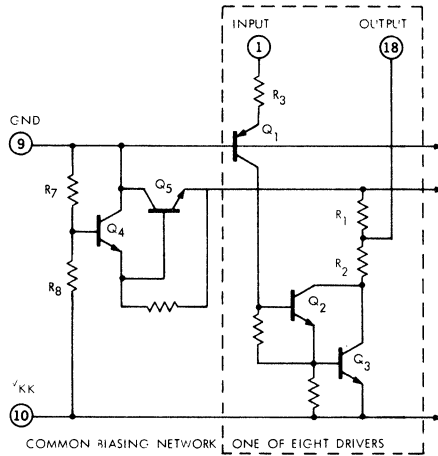
Figure 3

TYPICAL APPLICATION
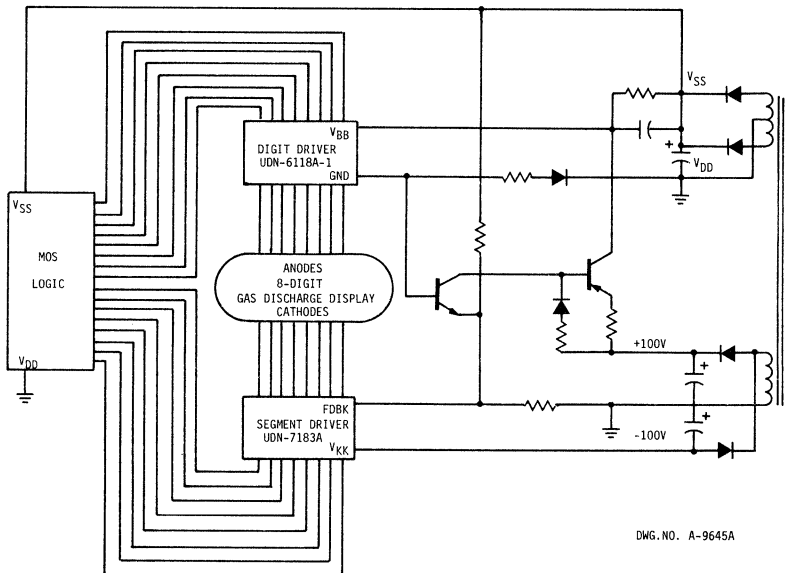
DWG. NO. A-9645A

Figure 4

The OFF output biasing network is common to all the individual drivers with the level of bias determined by the ratio of R_7 to the total of R_7 and R_8. As in the digit driver, the value of output bias is $\approx\frac{2}{3}$ the voltage across V_{KK} and ground—thus insuring sufficient 'on to off' swings to properly fire, and effectively extinguish unaddressed segments during a scan. Emitter follower Q_4 and Q_5 sources current to the pull-up bus connected to the various outputs as they are turned on during the display scan.

Minimum Component Interface

The impact of this new product family may be seen in the typical digital clock of Figure 5. This a-c powered clock uses a Mostek 50250 clock IC, a UDN-6116A-1 digit driver, and a UDN-7183 segment driver. Total component count is approximately 30 pieces, and the board layout is straightforward and uses single-sided board.

Many calculator interface schemes use considerable numbers of components (70 to 100 typically) to drive gas discharge panels. As one example: a twelve digit/eight segment machine uses 85-90 discretes while the new IC version uses only three packages, and results in less space along with considerable simplification. Other applications will benefit similarly with this series of circuits.

Summary

Display technology and usage has emerged at a mind boggling rate in the past several years—largely due to the fantastic growth rate of calculators. The planar gas panels have been an integral portion of this burgeoning market, but like all the other displays
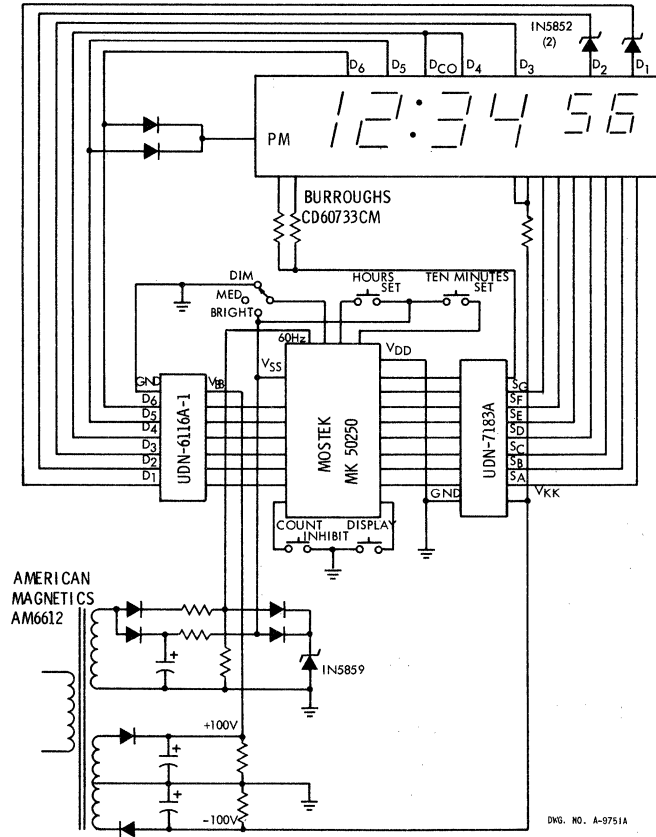
Figure 5

available does not meet the requirements for an ideal display.

Gas discharge panels are a fine combination of aesthetics, reliability, low cost, large character size, multiplexing capability, etc., but have been impacted to some degree by the lack of an available and inexpensive, totally monolithic interface. The move toward IC interface for displays has stifled some potential — largely in favor of LEDs; although many applications requiring large characters and/or in high ambient light turn toward gas panels. The planar gas discharge display is a long way from obscurity, and the availability of this family of ICs should open up new areas as well as satisfying existing systems.

The intent from the inception of this program has been to produce and provide a standard, inexpensive and easy to use interface for gas discharge displays. A great many potential applications exist for these circuits in consumer and commercial products. From the calculator and digital clock areas this product also will find use in automotive dashboards, point-of-sale systems, electronic cash registers and scales, and instrumentation. The market for displays is still very elastic, and many applications for gas discharge panels are continuing to appear. The Sprague contribution to this market is this series of state-of-the-art interface ICs.

2

TRENDS IN IC INTERFACE
FOR ELECTRONIC DISPLAYS

Introduction

Display technology was truly set into high gear by the explosion of the electronic calculator business. Expansion at a phenomenal pace continues, encompassing a multitude of products, particularly high-volume consumer products (calculators, clocks, games, and watches). Recently, further stimulated by the "microprocessor revolution," with its far-reaching effects, and the resulting changeover to solid state design from electromechanical, mechanical, fluidic, or electrical systems, the vistas for displays have expanded well beyond the horizon. Products have been and are being developed, using microprocessors and displays, that never previously existed.

To augment this microprocessor revolution, semiconductor manufacturers are developing many new interface circuits useful with displays, although some of these will not be exclusively for display systems. To accomplish this, the present boundaries of device design, process, packaging, and electrical parameters will require continual extension and expansion.

Display Buffers

A continuing evolution of standard interface ICs is needed to buffer low-level logic from high-voltage and /or high-current loads. Some of this buffer development will serve display systems. Since there already is a broad assortment of buffers (particularly for low- to medium-current LED applications), the ongoing development in simple or low-order interface will mainly concentrate upon further reduction in discrete component count, package improvement (particularly for high-current /high-power devices), improvements in device current, voltage, switching speed, and greater reliability.

Figures 1, 2, and 3 show some Sprague interface ICs that represent buffer circuits; other vendors supply similar, or identical, high-current or high-voltage buffers to allow operation of displays from low-level logic. Two basic changes have occurred relatively recently:

1. Greater use of 18-pin DIPs for eight driver channels (Source Driver, Figure 2).

2. Creation of sourcing functions (Figures 2 and 3; useful for LED, gas-discharge, vacuum fluorescent, incandescent, and electromagnetic displays, depending upon device ratings). While further buffer designs are needed (particularly in high-current (> 2 A) and high-voltage (> 100 V) circuits), the main emphasis will be toward the incorporation of logic and control circuitry with output buffers.

Complex Interface

Paralleling (though lagging) the microprocessor LSI revolution is the area of greatest future for IC display circuits: The need for complex, smart or high-order interface. This will be MSI to LSI logic (with perhaps some linear functions) combined with suitable output buffers.

UDN-6116A-1 GAS-DISCHARGE DRIVER
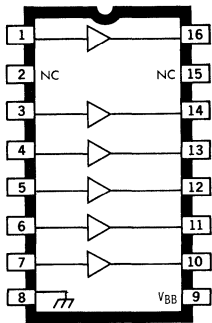
Dwg. No. A-9643A

Figure 1A
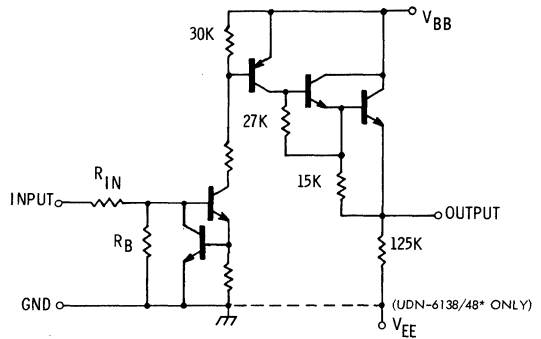
DWG. NO. A-10,592C

Figure 1B

SERIES UDN-2980 SOURCE DRIVER
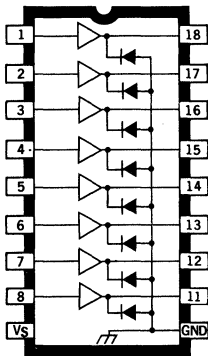
DWG. NO. A-10,243

Figure 2A

ONE OF EIGHT DRIVERS
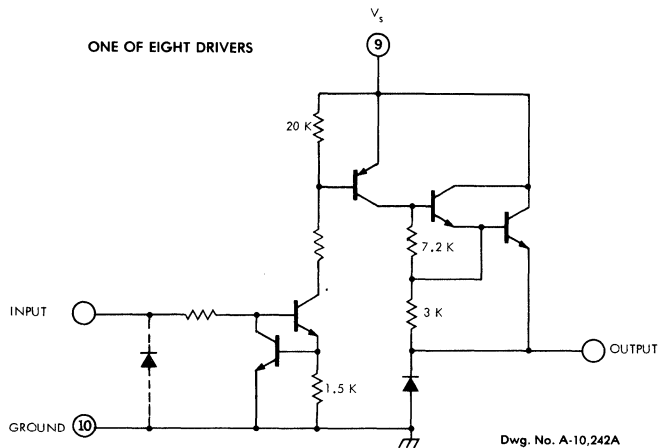
Dwg. No. A-10,242A

Figure 2B

Display interface ICs (similar to the MOS I/O control chips), both custom and standard product, are becoming available in this category. High-volume applications may justify custom ICs, but the more general trend will be toward standard, off-the-shelf designs — chiefly due to the high costs of developing custom ICs.

The higher voltage displays (gas-discharge, vacuum fluorescent, a-c plasma, and d-c electroluminescent) may share some circuits (if appropriately planned and designed), particularly in the area of matrix displays. It is difficult to imagine, however, much commonality between high-current LEDs, high-voltage gas-discharge or a-c plasma, and low-power LCDs,
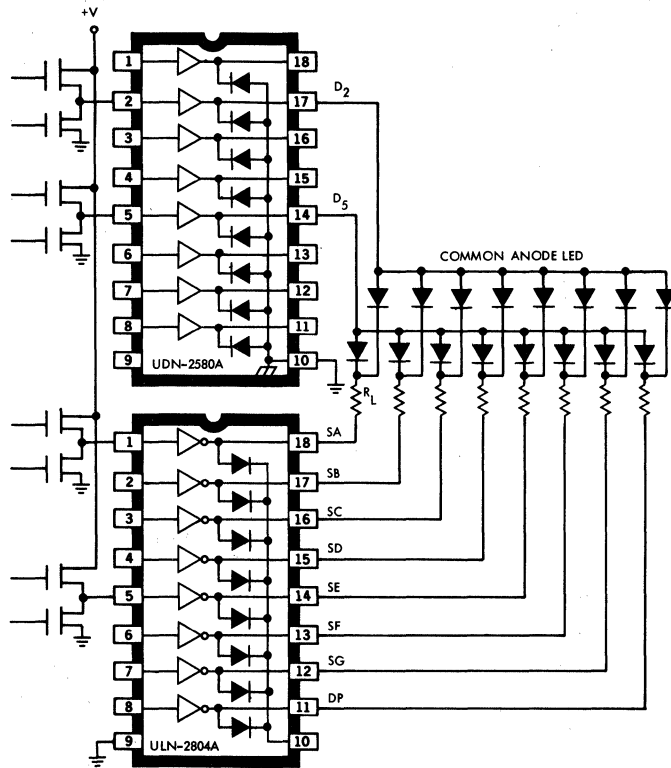
Figure 3

8-DIGIT/8-SEGMENT HIGH-CURRENT LED INTERFACE

although they should share considerably the development of cellular CAD circuit designs. Basic shift registers, latches and decoders do have considerable commonality.

In Figure 4 is a pinout and logic diagram of the first BiMOS Sprague IC combining logic and output drive. Although not expressly intended for display applications, this BiMOS (CMOS logic and bipolar outputs) IC has a great deal of utility to engineers working with lower voltages and high currents (LEDs, incandescent and electromagnetic displays). Type UCN-4801A is a parallel-in/parallel-out unit composed of eight 'D' latches and eight 350 mA /50 V bipolar Darlington outputs.
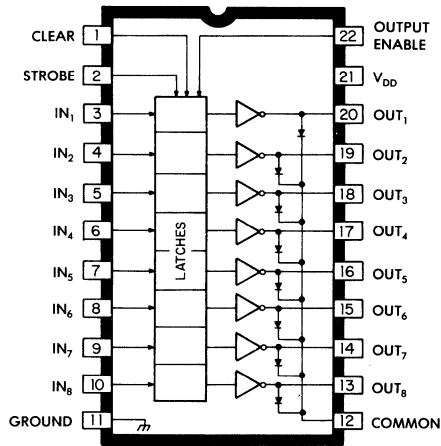
DWG.NO. A-10,498A

Figure 4A
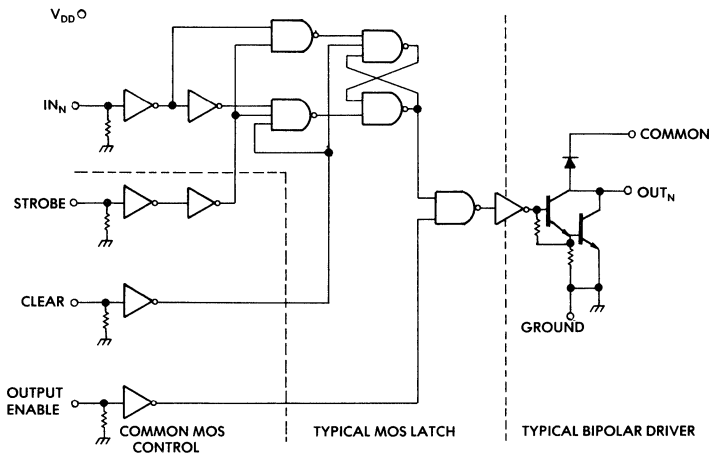
DWG.NO. A-10,495A

Figure 4B
UCN-4801A BIMOS LATCH/DRIVER

More recently, Sprague has designed a serial-in/parallel-out BiMOS interface IC expressly for use with vacuum fluorescent displays. Figure 5 shows the UCN-4810A 10-bit serial-in/parallel-out interface for use with VF displays; the use of serial data allows 10 output lines, data in and data out in a standard 18-lead DIP. It makes possible both fewer IC packages and simpler PC board wiring, although it is slower than a parallel data approach. It uses only a single pin of the I/O ports.
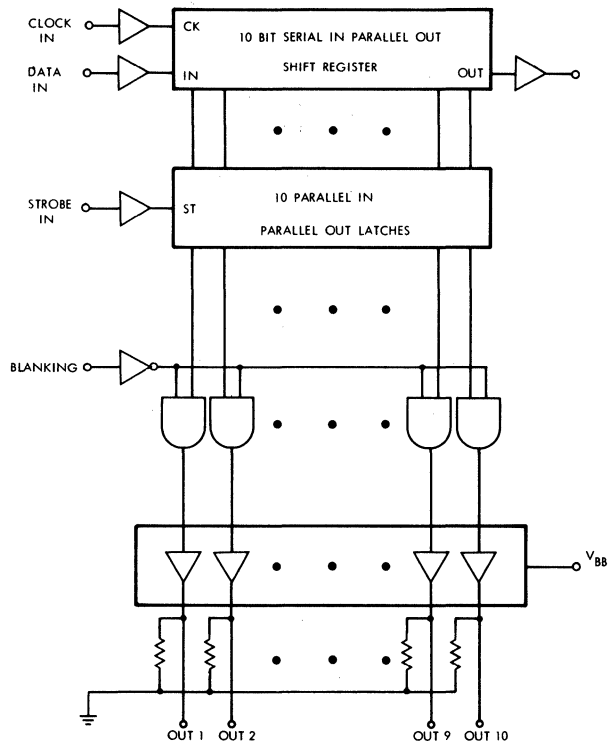
Figure 5B

UCN-4810A VF DRIVER BLOCK DIAGRAM
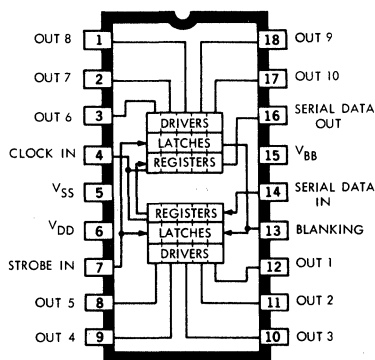
Figure 5A

UCN-4810A PINOUT

A slightly more recent design for vacuum fluorescent displays is the Sprague UCN-4815A. This is a 22-lead, 8-bit parallel-in /parallel-out BiMOS unit. The unit may have data inputs and a strobe bus (see Figure 6). The chip enable /blanking pin provides control of VF buffers. A power-on-clear is internally incorporated.

2
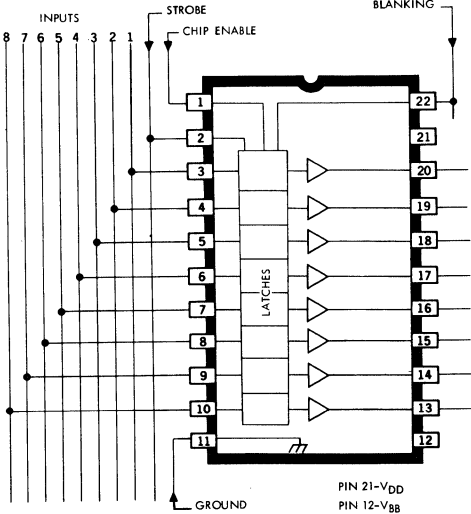
Figure 6
UCN-4815A PARALLEL 8-BIT VF INTERFACE

2—27

Device Technologies

With the exception of LCD displays (which at least until recently have been largely, if not entirely, driven by MOS) the display and interface technologies in high-volume use are mainly associated with bipolar semiconductors. Early display interface ICs (particularly devices such as the 7447 and 7448) were aimed at LED technology and represent MSI with modest output capability. The increasing use of higher voltage displays, multiplexed high-current applications, and the need for greater circuit complexity and low pin count will dictate other technologies, such as I^2L, BiMOS, CMOS/DMOS, and possibly DMOS.

Standard Bipolar

Standard bipolar technology, long associated with TTL or linears (early op amps), appears very limited in scope for the future. Circuit density and supply power requirements will dictate other processes for functions beyond the simple MSI level. The advantages of standard bipolar ICs appear to be in the areas of simple high-current, high-power or high-voltage interface. In particular, applications requiring the combination of high voltages (≥ 100 V) or multiple high-current outputs (≥ 2 A) will restrict the logic/control circuitry to a low level. Cost, chip size and package power dissipation will restrict this circuitry largely to versatile, simple buffers.

I^2L

Anticipated to increase significantly is the use of I^2L for systems of low to modest voltages (LEDs through VF). The present limits of I^2L appear to be limited to applications below the 50- to 60-volt level. I^2L, with its combination of circuit density, low power and reasonable switching speeds should make a fine match for LEDs or other low-voltage display applications. For higher voltages (> 25 or 30 V), prospects the penalty of reduced circuit density may diminish its cost effectiveness. Some increase in standoff voltage may be afforded by the uses of cascaded output transistors or process improvements, thus reducing the need to sacrifice logic density. Without a standard I^2L logic family, the main market penetration would appear to be custom designs although there is a definite opportunity for standard interface for lower voltage applications, particularly LEDs and vacuum fluorescent.

2

BiMOS

BiMOS, a combination of CMOS and bipolar for interface ICs, seems to fit a technology niche of higher breakdown voltages than I^2L, especially where logic power and supply voltage range (5 to 15 V) is important. BiMOS or BiFET ICs, which are presently on the market, are largely related to operational amplifiers, although other uses, such as the Sprague application of BiMOS to interface, are emerging.

Currently, it is feasible to design and manufacture BiMOS interface with breakdown voltages in the 80 to 100 V range. With additional time and greater concentration on increasing BV, it appears that higher voltages ($\ge$ 150 V) for output buffers could be obtained. By obtaining breakdowns in the 120 V to 160 V range, BiMOS then becomes a viable IC technology for interface for the higher voltage displays: d-c gas-discharge with ±100 to ±130 V; a-c plasma with 160 to 170 V, and glow transfer or d-c electroluminescent (DCEL) opportunities with a range of 120-150 volts.

Switching speeds and output configurations (active pull-down or resistive) are critical to matrix displays (particularly a-c plasma) with large numbers of drive lines. Adding active pull-down or pull-up will tend to increase chip size (and cost), thus adding to the potential overall difficulty of BiMOS with its greater process complexity and slightly longer manufacturing cycle. This does appear to be a very key technology for the near future. Its product niche will include for applications requiring 60 to 100 V (or more) breakdowns, low-power logic, wide supply range, modest speeds, and MSI to small LSI.

CMOS/DMOS

Chiefly being carried on by Texas Instruments, CMOS /DMOS display interface appears to be intended for much of the same display market as BiMOS. Product information now available indicates 60 to 100 V breakdown (DMOS outputs), CMOS logic, low to modest output currents ($\le$ 25 mA), and logic speeds to 4 MHz. Designs now being promoted are targeted toward a-c plasma and vacuum fluorescent panels.

Two apparent disadvantages now appear to exist:
1. Logic operates from 12 V ±10% (may be done to provide maximum speed).
2. Output drive current is insufficient for high-current displays (without 100 mA, or more, the larger matrix panels will use discretes or another technology).

These shortcomings may be modified with time, although it is doubtful if 500 mA to 1 A DMOS outputs are practical.

Dielectric Isolation

Affording the highest breakdown voltage capability of present technologies is dielectric isolation. Since there is no collector-to-substrate PN junction, nor a collector-to-isolation wall PN junction, considerable improvement in collector-to-base and collector-to-emitter voltage is possible. Additionally, transistor sizes are considerably smaller than their PN-isolated counterparts. The dielectrically isolated devices offered by Dionics span a spectrum of approximately 100 volts to 280 volts (a-c plasma driver). DI affords the maximum breakdown voltage capability currently available.

Opposing this great advantage in breakdown voltage, however, is the increased process complexity of dielectrically isolated ICs. Definite improvements are needed in the area of process simplification, cost reduction, and alternate sources. Large-volume use of DI circuits will be restrained until these problems (particularly alternate sources) can be overcome. DI interface, with its potential for 300 V transistors, has a great promise if the barriers can be overcome.

Packaging

Semiconductor design and process have greatly outstripped packaging currently in use, particularly in the area of power-handling capability. Greater concentration and resources are required to solve some of the following display interface related problems:

1. DIP power dissipation.

2. Greater number of leads (and smaller package sizes).

3. Improved plastic DIP resistance to moisture and corrosive environments.

4. Lower package manufacturing costs.

5. Smaller module or display subassemblies.

2

Power dissipation difficulties (strobed high currents) are most associated with LEDs. Use of very low duty-cycle and bright LEDs (particularly alphanumeric and matrix) dictates a need for multiplexing with peak currents as high as 3 A. Nothing currently on the market exceeds 1.75 A per output, and DIP ratings preclude d-c operation at such currents. However, many of the high-current applications are within the capability of standard bipolar ICs now offered.

For LSI ICs containing many I/O lines, the 24-, 28-, and 40-lead DIPs are standard. Since package size and cost increase together, it may be desirable to constrain many newer ICs to 18-, 20-, or 22-lead DIPs (with 0.300" spacing, 22 also in use with 0.450" width). Printed wiring board real estate is increasingly dictating smaller size. Solutions such as the quad in-line (Rockwell) or less than 0.100" centers are possible. There are problems associated with a non-standard configuration (lack of sockets and higher prices) and the smaller physical size will not aid the quest for higher power (LEDs).

Improvements in plastic DIP moisture resistance and reliability are already underway; uses of tri-metal schemes (such as RCA's), silicon nitride or quartz passivation will continue to improve resistance to moisture and corrosive fumes. For display applications, these reliability improvements are of greatest concern in high-voltage devices.

Lower package costs are necessary to further increase the use of ICs in areas such as flat panel matrix displays. Currently, much of the cost of such a system is related to drive electronics, and much of the cost of the interface is the assembly cost of the DIPs (or hybrids). Increased use of automated assembly, film-carrier techniques and solder bumps will enhance the choice of ICs over discretes, and flat panel over CRT.

Also of concern is the possible mating of IC chips, solder-bump chips, or film-strip chips into the display assembly. Candidates for such a treatment would include d-c and a-c plasma, LEDs (already being done to a degree), DCEL, ACEL, LCD, and VF. Panel technologies using thick or thin-film techniques could benefit from such an approach. The biggest barrier to such an integrated assembly is the market data needed to justify tooling and lead time. It will only require one manufacturer willing to be a pioneer to further swing display technology into integrated systems. Prospects for purchasing a display complete with all drive electronics, such as a flat panel a-c plasma matrix (chips mounted via hybrid techniques on the rear of the glass envelope), are improving with time.

Summary

A bright future exists for IC interface in display systems; the combination of logic (from MSI to small LSI) with suitable output buffers will further assist display designs. The following IC Technology-Display Interface matrix lists the key characteristics and primary display applications of various semiconductor technologies. Since many of these characteristics are changing, the table lists the device characteristics either now available or for the near future.

The most dynamic technologies for the immediate future appear to be BiMOS, I^2L, CMOS/DMOS, and, perhaps soon, DMOS. Sprague, Dionics, RCA, Texas Instruments, National Semiconductor, and others are using these device technologies to carve market niches where suitable. The dynamics of the IC market make for an uncertain future for any supplier of display circuitry unable or unwilling to continue the technological advancement necessary to meet the changing demands of the display market.

IC TECHNOLOGY — DISPLAY INTERFACE

Technology	Breakdown V	Output 1	Speed	LOGIC Complexity (max)	Range	Supply Power	Primary Display Suitability
Linear Process Bipolar	10 to ~170 V	<10 mA to 2 A	<1 MHz	MSI	5 V	High	LEDs, GD, VF, ACP, DCEL, EM
I^2L	20 to ~60 V	<10 mA to 2 A	3-6 MHz	LSI	5 V	Low-Modest	LED, VF, EM
BiMOS	50 to ~150 V	<10 MA to 500 mA	2-5 MHz	LSI	5 to 15 V	Low	LED, GD, VF, ACP, DCEL, EM
CMOS/DMOS	60 to ~100 V	~25 mA	2-4 MHz	LSI	12 V	Low	GD, VF, ACP, LCD
DI	~200 to ~300 V	<10 mA to 100 mA (est)	1 MHz (est)	MSI	5 V	High	GD, VF, ACP, DCEL

Code: GD = D-C Gas-Discharge & Glow Transfer   DCEL = D-C Electroluminescent
    ACP = A-C Plasma   EM = Electromagnetic
    VF = Vacuum Fluorescent

RELIABILITY OF SERIES UDN-6100A
HIGH-VOLTAGE DISPLAY DRIVERS

THIS REPORT SUMMARIZES accelerated-life tests that have been performed on Series UDN-6100A integrated circuits and provides information that can be used to calculate the failure rate at any junction operating temperature.

INTRODUCTION

Product-reliability improvement is a continuous and evolving process at Sprague Electric Company. Ongoing life tests, environmental tests, and stress tests are performed to establish failure rates and monitor established process-control procedures. Failures are analyzed to determine design changes or process improvements that can be implemented to improve device reliability.

The reliability of integrated circuits can be measured by qualification tests, accelerated tests, and burn-in:

1) Qualification testing is performed at +125°C for 1000 hours with an LTPD = 5 in accordance with MIL-STD-883B. This testing is normally conducted in response to a specific customer request or requirement. Qualification testing highlights design problems or gross processing problems, but does not provide sufficient data to generate accurate failure rates in a reasonable period of time.

2) Accelerated testing is performed at temperatures above +125°C and is used to generate failure-rate data.

3) Burn-in is intended to remove infant-mortality rejects and is conducted at +150°C for 96 hours or at +125°C for 168 hours. An analysis of test results from Sprague Electric's Double-Deuce™ burn-in program found 1.27% failures in more than 325,000 pieces tested in a recent time period. Most failures

were due to slight parametric shifts. Catastrophic failures, which would cause user-equipment failure, were less than 0.1%.

ACCELERATED-LIFE TESTS

Sprague Electric performs accelerated-life tests on integrated circuits at junction temperatures of +150°C or +175°C at the recommended operating voltages. The internal power dissipation on some high-power circuits requires the ambient temperature to be lower than +150°C to keep the junction temperature between +150°C and +175°C.

In these tests, failures are produced so that the statistical life distribution may be established. The distribution cannot be established without failures. High-temperature accelerated-life testing is necessary to accumulate data in reasonable time periods. It has been established that the failure mechanisms all temperatures in these tests are identical. Temperatures above +175°C are not generally used for the following reasons:

a) Industry-standard molding compounds degrade and release contaminants (halides) at approximately +200°C.

b) Life-test boards constructed with materials capable of withstanding exposure to temperatures greater than +175°C have been deemed to be cost prohibitive.

c) Increases in junction leakage currents may increase the power dissipation and device temperature to an indeterminant level.

Table I contains Series UDN-6100A data produced by life tests that were conducted at +150°C. The data includes the number of test samples, number of units in each sample, and the time periods during which failures occurred. The total time-on-test varies, with priority changes influencing allocation of oven and board space, as new products are introduced. The time intervals between test readings were chosen for ease of plotting on log-normal paper.

The acceleration factor calculated using the Arrhenius equation, and a 1 eV activation energy, is approximately 5× for each 25°C temperature rise in junction temperature and is multiplicative.[1] This allows the data to be compared to qualification life-test data by equating 200 hours at +150°C to 1000 hours at +125°C. If these tests had been qualification tests, they would have ended at 200 hours at +150°C or 40 hours at +175°C.

The data at the bottom of Table I is compiled by calculating the probability of success (P_s), the cumulative probability of success, the probability of failure (P_f) and the percentage of failed units in each time period.

The cumulative percent of failures is plotted on log-normal plotting paper in Figure 1. This paper has a logarithmic time-scale axis and a probability-scale axis. A log-normal distribution plots a straight line. A line of best fit is drawn through the plotted points and extended to determine the median lifetime at the 50% fail-point. The median life at a junction temperature of +150°C is 100,000 hours, in this case.

The log-normal distribution is commonly and widely used, because most semiconductor device data fits such a distribution.[2] When the median life has been found at the elevated temperature, it can be converted to the lower temperature of the actual application. The Arrhenius equation, which relates the reaction rate to temperature, is used to make this conversion.[1] The Arrhenius equation is:

$$V_r = V_r^\circ e^{-\varepsilon/kT}$$

where V_r° = a constant
ε = activation energy
k = Boltzmann's constant
T = absolute temperature in degrees Kelvin

An activation energy of 1.0 electron-volt was established by testing Series ULN-2000A, Series UDN-5700M, and Series UDN-2980A devices at multiple temperatures. Failure analysis of devices rejected during the testing also supports this activation energy, as failures were mainly due to increased leakages, reduced beta, and surface inversion.[3]

TABLE I
TEST RESULTS AT T_J = +150°C

TEST NUMBER	BIAS VOLTS	QTY.	90	150	300	600	1200	1800	2000	5000	6000
						HOURS ON TEST					
						NUMBER OF FAILURES					
1	80	24	0	0	2	—	—	—	—	—	—
2	80	24	0	0	0	0	0	0	1	0	—
3	80	12	0	0	0	0	0	—	—	—	—
4	80	12	0	0	0	0	2	1	1	0	0
5	110	24	0	0	0	0	0	0	1	—	—
6	80	12	0	0	0	—	—	—	—	—	—
TOTAL ON TEST			108	108	108	72	72	58	57	31	8
TOTAL FAILURES			0	0	2	0	2	1	3	0	0
TOTAL GOOD			108	108	106	72	70	57	54	31	8
P_s			1.00	1.00	0.981	1.00	0.972	0.983	0.947	1.00	1.00
Cumulative P_s			1.00	1.00	0.981	0.981	0.954	0.938	0.888	0.888	0.888
$P_f = 1 - P_s$			0	0	0.019	0.019	0.046	0.062	0.112	0.112	0.112
% Failures			0	0	1.9	1.9	4.6	6.2	11.2	11.2	11.2

Dwg. No. A-11,865
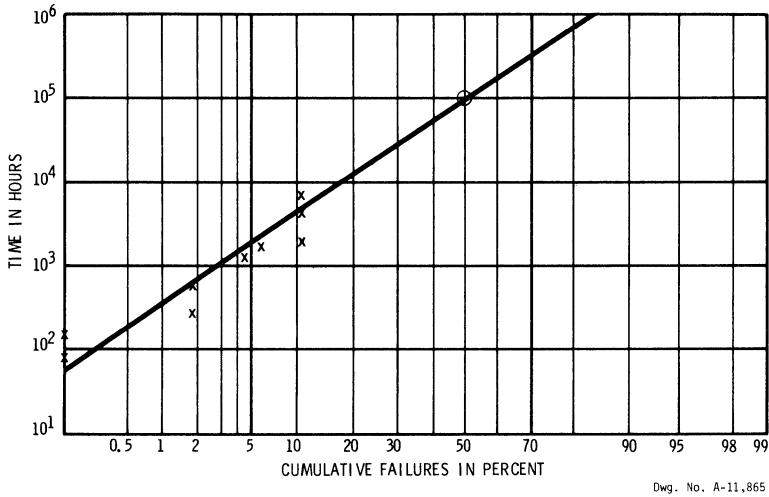
Figure 1
CUMULATIVE PERCENT OF FAILURES

The median life-point is drawn on Arrhenius graph paper in Figure 2. Arrhenius plotting paper gives a graphical solution, rather than a mathematical solution, to the problem of equivalent median lifetime at any junction temperature. A line is drawn through this point (or points when multiple temperatures are used) with a slope of $\varepsilon = 1.0$ eV.

Although not as statistically accurate as the median lifetime, the 5% fail-point can be read from Figure 1 and plotted parallel to the median-life line in Figure 2.

The median life with lower junction temperatures may now be determined using Figure 2. It must be emphasized that this is junction temperature and not ambient temperature. The temperature rise at the junction due to internal power dissipation must be taken into account using the formula:

$$T_J = P_D \Theta_{JA} + T_A$$
$$\text{or}$$
$$T_J = P_D \Theta_{JC} + T_C$$

The median lifetime, or 50% fail-point, as determined in Figure 2, is approximately 100 years at

+125°C or 1,000 years at +90°C junction temperature.

The approximate failure rate ($\overline{FR}$) may be determined from $\overline{FR} = 1/\text{Median Life}$, where Median Life is taken from Figure 2 at the intersection of the junction-temperature line and median-life plot. The actual instantaneous failure rate may be calculated using a Goldwaite plot.[4] However, this approximation is very close. At +100°C the failure rate would be:

$$\overline{FR} = 1/(4 \times 10^6 \text{ hours})$$
$$= 0.025\%/1000 \text{ hours}$$

Other failure rate values have been calculated in Table II.

TABLE II
SERIES UDN-6100A FAILURE RATES

T_J (°C)	Median Life (h)	Failure Rate (%/1000 h)
125	6×10^5	0.167
100	4×10^6	0.025
75	4×10^7	0.0025
50	5×10^8	0.0002
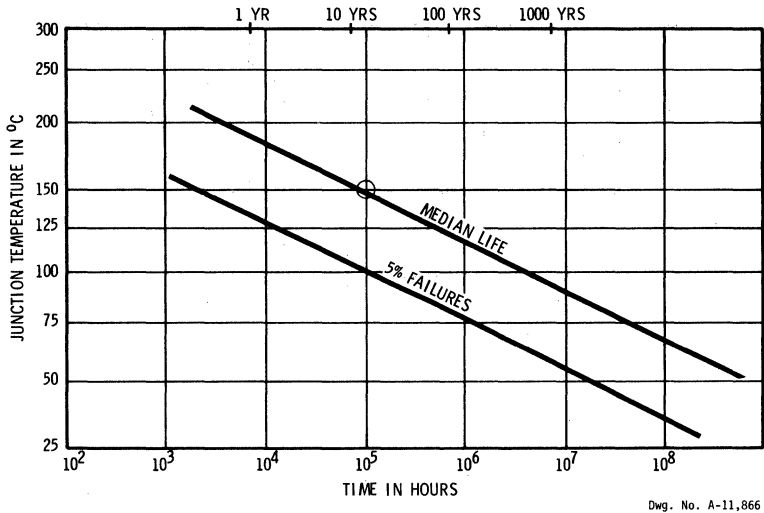
Figure 2

MEDIAN LIFE

CONCLUSION

The relationship between temperature and failure rate is well documented and is an important factor in all designs. Load currents, duty cycle, and ambient temperature must be considered by the design engineer to establish a junction-temperature limit that provides failure rates within design objectives.

Figure 2 shows that a design with a junction temperature of +100°C, calculated from internal power dissipation and external ambient temperature, reaches the 5% fail-point in 10 years. Lowering the junction temperature to +70°C increases the time to 100 years.

A complete sequence of environmental tests on Series UDN-6100A, including temperature cycle, pressure cooker, and biased humidity tests are also continuously monitored to ensure that assembly and package technology remain within established limits.

These environmental tests and accelerated-life tests establish a base line for comparisons of new processes and materials.

REFERENCES

1) Manchester, K. E., and Bird, D.W., "Thermal Resistance: A Reliability Consideration," *IEEE Transactions,* Vol. CHMT-3, No. 4, 1980, pp. 580-587 (Sprague Technical Paper TP 80-2).

2) Peck, D.S., and Trapp, O. D., *Accelerated Testing Handbook,* Technology Associates, 1978, pp. 2-1–2-6.

3) *ibid.,* p. 6-7.

4) Goldwaite, L. R., "Failure Rate Study for the Log-Normal Lifetime Model," *Proceedings of the 7th Symposium on Reliability and Quality Control,* 1961, pp. 208–213.

NOTES

SECTION 3—HIGH-CURRENT INTERFACE DRIVERS

*New product. Contact factory for detailed information.

SELECTION GUIDE TO HIGH-CURRENT INTERFACE DRIVERS

Device Type	Absolute Maximum Ratings		Outputs
	I_{OUT}	V_{OUT}	
UHP-400 through 433	500 mA	40 V	Sink 4
UHP-400 through 433-1	500 mA	70 V	Sink 4
UHP-500 through 533	500 mA	100 V	Sink 4
ULN-2001 through 2005A	500 mA	50 V	Sink 7
ULN-2011 through 2015A	600 mA	50 V	Sink 7
ULN-2021 through 2025A	500 mA	95 V	Sink 7
ULN-2061M	1.75 A	50 V	Source/Sink 2
ULN-2062M	1.75 A	80 V	Source/Sink 2
ULN-2064/66/68/70B	1.75 A	50 V	Sink 4
ULN-2065/67/69/71B	1.75 A	80 V	Sink 4
ULN-2074/76B	1.75 A	50 V	Source/Sink 4
ULN-2075/77B	1.75 A	80 V	Source/Sink 4
UDN-2541B/W	1.5 A	60 V	Sink 4
UDN-2542B/W	1.5 A	80 V	Sink 4
UDN-2580A	− 500 mA	50 V	Source 8
UDN-2580A-1	− 500 mA	80 V	Source 8
UDN-2585A	− 250 mA	20 V	Source 8
UDN-2588A	− 500 mA	50 V	Source 8
UDN-2588A-1	− 500 mA	80 V	Source 8
UDN-2595A	200 mA	20 V	Sink 8
ULN-2801 through 2805A	500 mA	50 V	Sink 8
ULN-2811 through 2815A	600 mA	50 V	Sink 8
ULN-2821 through 2825A	500 mA	95 V	Sink 8
UDN-2841B	1.75 A	− 50 V	Sink 4
UDN-2845B	1.75 A	− 50 V	Source/Sink 4
UDN-2878W	5.0 A	50 V	Sink 4
UDN-2879W	5.0 A	80 V	Sink 4
UTN-2886B	800/1600 mA	35 V	Sink 4 + 2
UTN-2888A	800 mA	35 V	Sink 8
UDN-2933/34B	± 800 mA	30 V	3 Half-Bridge
UDN-2935Z	± 2.0 A	35 V	Half-Bridge
UDN-2949Z	± 2.0 A	30 V	Half-Bridge
UDN-2950Z	± 2.0 A	35 V	Half-Bridge
UDN-2952B/W	+ 3.5 A	40 V	Full Bridge
UDN-2956/57A	− 500 mA	− 80 V	Source 5
UDN-2975W	5.0 A	50 V	Source/Sink 2
UDN-2976W	5.0 A	60 V	Source/Sink 2
UDN-2981/82A	− 500 mA	50 V	Source 8
UDN-2983/84A	− 500 mA	80 V	Source 8
UDN-3611 through 3614M	600 mA	80 V	Sink 2
UDN-5703 through 5707A	600 mA	80 V	Sink 4
UDN-5711 through 5714M	600 mA	80 V	Sink 2
UDN-5722M	600 mA	70 V	Sink 2
UDN-5732M	600 mA	70 V	Sink 2
UDN-5733A	600 mA	80 V	Sink 4
UDN-5742M	700 mA	70 V	Sink 2

SERIES UHP-400, UHP-400-1 AND UHP-500 POWER AND RELAY DRIVERS

FEATURES

- Inputs Compatible with DTL/TTL
- 500mA Output Sink Current Capability
- Pinning Compatible with 54/74 Logic Series
- Transient Protected Outputs on Relay Drivers
- High Voltage Output – 100V Series UHP-500, 70V Series UHP-400-1, 40V Series UHP-400

3

Description

These power and relay drivers are bi-polar monolithic circuits and incorporate logic gates and high-current switching transistors on the same chip. Each output transistor is capable of sinking 500mA in the ON state. In the OFF state, Series UHP-400 devices will sustain 40V, Series UHP-400-1 devices will sustain 70V, and Series UHP-500 devices will sustain 100V.

Applications

The UHP-400, UHP-400-1, and UHP-500 Series Power Drivers are ideally suited for driving incandescent lamps, relays, solenoids, and other interface devices with up to 1A output current per package.

| UHP-400/400-1/500 Quad 2 AND | UHP-402/402-1/502 Quad 2 OR | UHP-403/403-1/503 Quad OR | UHP-406/406-1/506 Quad AND |
| UHP-407/407-1/507 Quad NAND | UHP-408/408-1/508 Quad 2 NAND | UHP-432/432-1/532 Quad 2 NOR | UHP-433/433-1/533 Quad NOR |
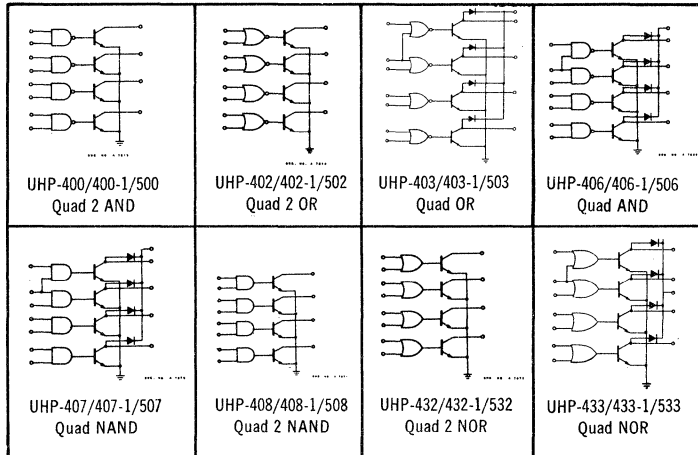
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} 7V
Input Voltage, V_{in} 5.5V
Output Off-state Voltage, V_{off}
   Series UHP-400 .... 40V
   Series UHP-400-1 .... 70V
   Series UHP-500 .... 100V
Output On-State Sink Current, I_{on} 500mA
Suppression Diode Off-State Voltage, V_{off}
   Series UHP-400 .... 40V
   Series UHP-400-1 .... 70V
   Series UHP-500 .... 100V
Suppression Diode On-State Current, I_{on} 500mA
Operating Free-Air Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+85°	°C
Current into any output (ON state)			250	mA

Series UHP 14-pin plastic dual in-line; copper lead frame and epoxy encapsulation standard for high power handling capability.*
Thermal Resistance:
   Junction to case, ϕ_{jc} .... 40°C/W
   Junction to still air, ϕ_{ja} .... 60°C/W

*ϕ_{ja} of 60°C/W permits operation of four outputs continuously and simultaneously at 250mA with a junction temperature which will not exceed +150°C (ϕ_j) at a +85°C ambient.

> At manufacturer's option, these devices may be marked with the original Series UHP-400, UHP-400-1, or UHP-500 part numbers and/or part numbers in the new Series UDN-0400A, UDN-0400A-1, or UDN-0500A, respectively. Similar devices using the original and new part numbering systems are identical in all respects. For example: UHP-408 is exactly the same as the UDN-0408A.

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
				Test Conditions				Limits			
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current at all Inputs except Strobe	$I_{in(0)}$		MAX	0.4V	4.5V			−0.55	−0.8	mA	2
"0" Input Current at Strobe	$I_{in(0)}$		MAX	0.4V	4.5V			−1.1	−1.6	mA	
"1" Input Current at all Inputs except Strobe	$I_{in(1)}$		MAX	2.4V	0V				40	μA	2
			MAX	5.5V	0V				1	mA	
"1" Input Current at Strobe	$I_{in(1)}$		MAX	2.4V	0V				100	μA	2
			MAX	5.5V ·	0V				1	mA	

SWITCHING CHARACTERISTICS at V_{CC} = 5.0V, T_A = 25°C

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
				Limits			
Turn-on Delay Time Series UHP-400 Series UHP-400-1 Series UHP-500	t_{pd0}	$C_L = 15pF$ $V_S = 40V, R_L = 265\,\Omega$ (6 Watts) $V_S = 70V, R_L = 465\,\Omega$ (10 Watts) $V_S = 100V, R_L = 670\,\Omega$ (15 Watts)		200	500	ns	3
Turn-off Delay Time Series UHP-400 Series UHP-400-1 Series UHP-500	t_{pd1}	$C_L = 15pF$ $V_S = 40V, R_L = 265\,\Omega$ (6 Watts) $V_S = 70V, R_L = 465\,\Omega$ (10 Watts) $V_S = 100V, R_L = 670\,\Omega$ (15 Watts)		300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

Type UHP-400, UHP-400-1, and UHP-500

Quad 2-Input AND Power Drivers

DWG. NO. A-7606

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-400	I_{off}		MIN	2.0V	2.0V	40V			50	μA	
"1" Output Reverse Current Type UHP-400-1	I_{off}		MIN	2.0V	2.0V	70V			50	μA	
"1" Output Reverse Current Type UHP-500	I_{off}		MIN	2.0V	2.0V	100V			50	μA	
"0" Output Voltage	V_{on}		MIN	0.8V	V_{cc}	150mA			0.5	V	
			MIN	0.8V	V_{cc}	250mA			0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0V	5.0V			4	6	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0V	0V			17.5	24.5	mA	1, 2

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each gate.
3. Capacitance values specified include probe and test fixture capacitance.

DWG. NO. A-7876D

DWG. No. A-7628C

Type UHP-402, UHP-402-1, and UHP-502

Quad 2-Input OR Power Drivers

3

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Output Reverse Current Type UHP-402	I_{off}		MIN	2.0V	0V	40V			50	μA	
"1" Output Reverse Current Type UHP-402-1	I_{off}		MIN	2.0V	0V	70V			50	μA	
"1" Output Reverse Current Type UHP-502	I_{off}		MIN	2.0V	0V	100V			50	μA	
"0" Output Voltage	V_{on}		MIN	0.8V	0.8V	150mA			0.5	V	
			MIN	0.8V	0.8V	250mA			0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM MAX	5.0V	5.0V			4.1	6.3	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM MAX	0V	0V			18	25	mA	1, 2

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each gate.
3. Capacitance values specified include probe and test fixture capacitance.

Type UHP-403, UHP-403-1, and UHP-503

Quad OR Relay Drivers

DWG. NO. A-9130

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-403	I_{off}		MIN	2.0V	0V	40V			100	μA	
"1" Output Reverse Current Type UHP-403-1	I_{off}		MIN	2.0V	0V	70V			100	μA	
"1" Output Reverse Current Type UHP-503	I_{off}		MIN	2.0V	0V	100V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8V	0.8V	150mA			0.5	V	
			MIN	0.8V	0.8V	250mA			0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0V	0V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0V	5.0V			4.1	6.3	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0V	0V			18	25	mA	1, 2

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each gate.
3. Diode leakage current measured at V_R = $V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 200mA.
5. Capacitance values specified include probe and test fixture capacitance.

DWG. NO. A-9123A

DWG. No. A-7628C

Type UHP-406, UHP-406-1, and UHP-506
Quad AND Relay Drivers
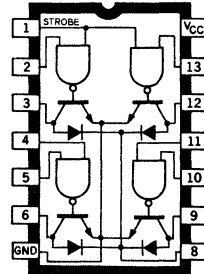
DWG. NO. A 7880

3

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-406	I_{off}		MIN	2.0V	2.0V	40V			100	μA	
"1" Output Reverse Current Type UHP-406-1	I_{off}		MIN	2.0V	2.0V	70V			100	μA	
"1" Output Reverse Current Type UHP-506	I_{off}		MIN	2.0V	2.0V	100V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8V	V_{CC}	150mA			0.5	V	
			MIN	0.8V	V_{CC}	250mA			0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0V	0V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0V	5.0V			4	6	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0V	0V			17.5	24.5	mA	1, 2

NOTES:
1. Typical values are at V_{CC} = 5.0, T_A = 25°C.
2. Each gate.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 200mA.
5. Capacitance values specified include probe and test fixture capacitance.

DWG. NO. A-7678A

DWG. No. A-7628C

Type UHP-407, UHP-407-1, and UHP-507

Quad NAND Relay Drivers

DWG. NO. A-7973

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Output Reverse Current Type UHP-407	I_{off}		MIN	0.8V	Vcc	40V			100	μA	
"1" Output Reverse Current; Type UHP-407-1	I_{off}		MIN	0.8V	Vcc	70V			100	μA	
"1" Output Reverse Current Type UHP-507	I_{off}		MIN	0.8V	Vcc	100V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0V	2.0V	150mA			0.5	V	
			MIN	2.0V	2.0V	250mA			0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	4
Diode Forward Voltage Drop	V_D	NOM	NOM	0V	0V			1.5	1.75	V	5
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0V	0V			6	7.5	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5V	5V			20	26.5	mA	1, 2

NOTES:
1. Typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.
2. Each gate.
3. Capacitance values specified include probe and test fixture capacitance.
4. Diode leakage current measured at $V_R = V_{off(min)}$.
5. Diode forward voltage drop measured at $I_f = 200mA$.

DWG. NO. A-7899A

DWG. NO. A-7900A
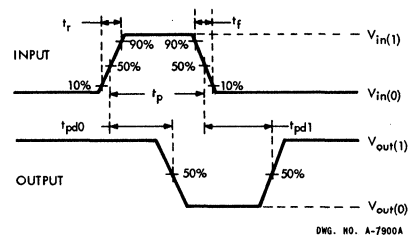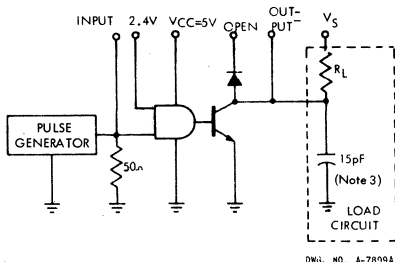
Type UHP-408, UHP-408-1, and UHP-508
Quad 2-Input NAND Power Drivers

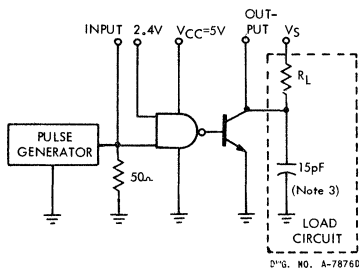**ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)**

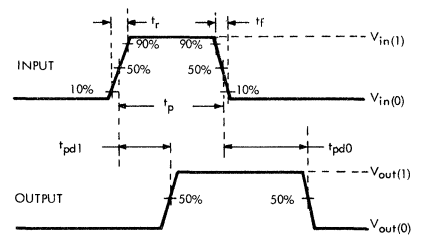| Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-408	I_{off}		MIN	0.8V	V_{CC}	40V			50	μA	
"1" Output Reverse Current Type UHP-408-1	I_{off}		MIN	0.8V	V_{CC}	70V			50	μA	
"1" Output Reverse Current Type UHP-508	I_{off}		MIN	0.8V	V_{CC}	100V			50	μA	
"0" Output Voltage	V_{on}		MIN	2.0V	2.0V	150mA			0.5	V	
			MIN	2.0V	2.0V	250mA			0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0V	0V		6		7.5	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0V	5.0V		20		26.5	mA	1, 2

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each gate.
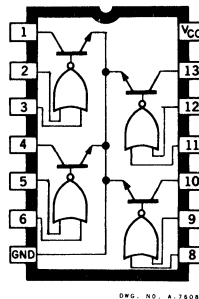3. Capacitance values specified include probe and test fixture capacitance.
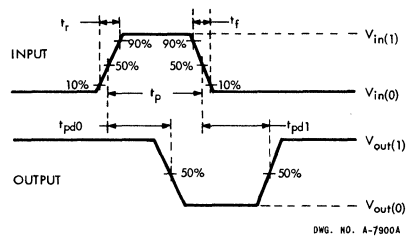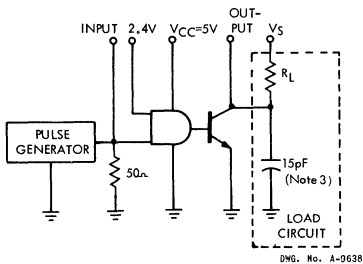
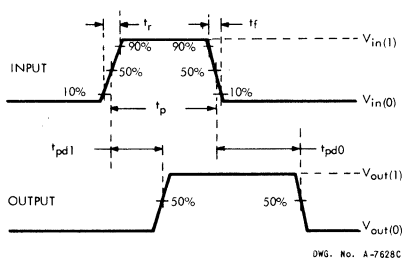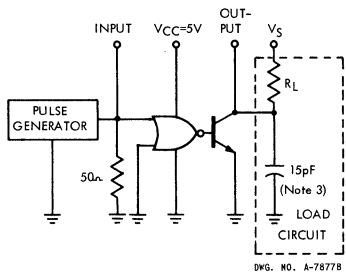# Type UHP-432, UHP-432-1, and UHP-532
Quad 2-Input NOR Power Drivers

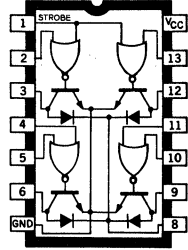## ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Output Reverse Current Type UHP-432	I_{off}		MIN	0.8V	0.8V	40V			50	μA	
"1" Output Reverse Current Type UHP-432-1	I_{off}		MIN	0.8V	0.8V	70V			50	μA	
"1" Output Reverse Current Type UHP-532	I_{off}		MIN	0.8V	0.8V	100V			50	μA	
"0" Output Voltage	V_{on}		MIN	2.0V	0V	150mA			0.5	V	
			MIN	2.0V	0V	250mA			0.7	V	
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0V	5.0V			20	25	mA	1, 2
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0V	0V			6	7.5	mA	1, 2

NOTES:
1. Typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.
2. Each gate.
3. Capacitance values specified include probe and test fixture capacitance.
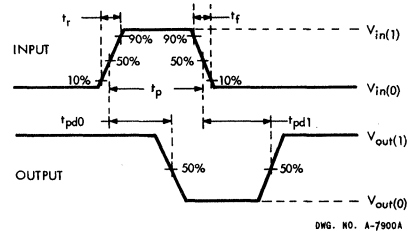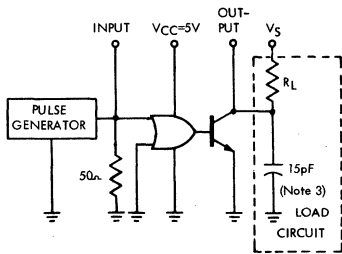
Type UHP-433, UHP-433-1, and UHP-533
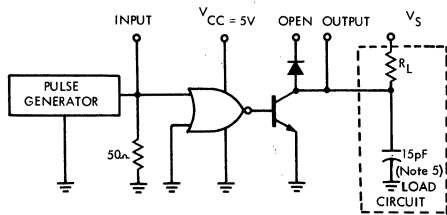## Quad NOR Relay Drivers

3

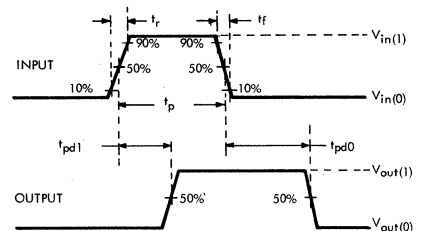## ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	Vcc	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current Type UHP-433	I$_{off}$		MIN	0.8V	0.8V	40V			100	μA	
"1" Output Reverse Current Type UHP-433-1	I$_{off}$		MIN	0.8V	0.8V	70V			100	μA	
"1" Output Reverse Current Type UHP-533	I$_{off}$		MIN	0.8V	0.8V	100V			100	μA	
"0" Output Voltage	V$_{on}$		MIN	2.0V	0V	150mA			0.5	V	
			MIN	2.0V	0V	250mA			0.7	V	
Diode Leakage Current	I$_{LK}$	NOM	NOM	V$_{CC}$	V$_{CC}$	OPEN			200	μA	3
Diode Forward Voltage Drop	V$_D$	NOM	NOM	0V	0V			1.5	1.75	V	4
"1" Level Supply Current	I$_{CC(1)}$	NOM	MAX	0V	0V			6	7.5	mA	1, 2
"0" Level Supply Current	K$_{CC(0)}$	NOM	MAX	5V	5V			20	25	mA	1, 2

NOTES:
1. Typical values are at V$_{CC}$ = 5.0, T$_A$ = 25°C.
2. Each gate.
3. Diode leakage current measured at V$_R$ = V$_{off(min)}$.
4. Diode forward voltage drop measured at I$_f$ = 200mA.
5. Capacitance values specified include probe and test fixture capacitance.
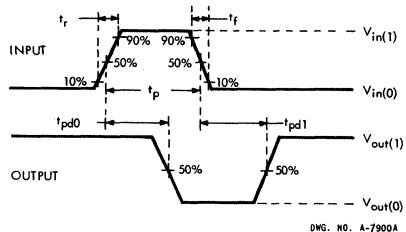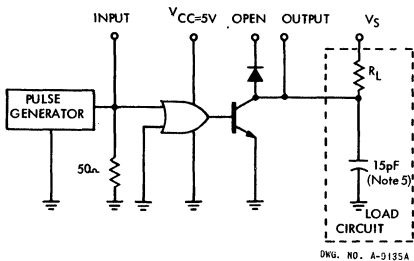
SERIES ULN-2000A
HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON ARRAYS

THESE HIGH-VOLTAGE, HIGH-CURRENT Darlington arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units have open-collector outputs and integral diodes for inductive load transient suppression.

Peak inrush currents to 600 mA (Series ULN-2000A and ULN-2020A) or 750 mA (Series ULN-2010A) are permissible, making them ideal for driving tungsten filament lamps.

Series ULN-2001A devices are general purpose arrays that may be used with standard bipolar digital logic using external current limiting, or with most PMOS or CMOS directly. All are pinned with outputs opposite inputs to facilitate printed wiring board layout and are priced to compete directly with discrete transistor alternatives.
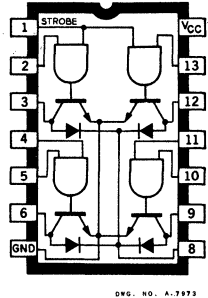
Series ULN-2002A is designed for use with 14 to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also gives these devices excellent noise immunity.

Series ULN-2003A has a 2.7 kΩ series base resistor for each Darlington pair, allowing operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs — particularly those beyond the capabilities of standard logic buffers.

Series ULN-2004A has a 10.5 kΩ series input resistor that permits operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of Series ULN-2003A, while the required input voltage is less than that required by Series ULN-2002A.

Series ULN-2005A is designed for use with standard TTL and Schottky TTL, with which higher output currents are required and loading of the logic
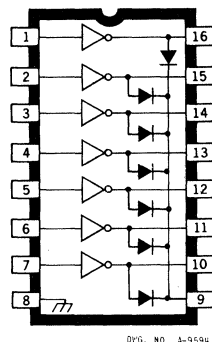
DWG. NO. A-9594

output is not a concern. These devices will sink a minimum of 350 mA when driven from a "totem pole" logic output.

Series ULN-2000A is the original high-voltage, high-current Darlington array. The output transistors are capable of sinking 500 mA and will sustain at

Device Number Designation

$V_{CE(MAX)}$	50 V	50 V	95 V
$I_{C(MAX)}$	500 mA	600 mA	500 mA
Logic	Type Number		
General Purpose PMOS, CMOS	ULN-2001A	ULN-2011A	ULN-2021A
14-25 V PMOS	ULN-2002A	ULN-2012A	ULN-2022A
5 V TTL, CMOS	ULN-2003A	ULN-2013A	ULN-2023A
6-15 V CMOS, PMOS	ULN-2004A	ULN-2014A	ULN-2024A
High-Output TTL	ULN-2005A	ULN-2015A	ULN-2025A

least 50 V in the OFF state. Outputs may be paralleled for higher load-current capability. Series ULN-2010A devices are similar, except that they will sink 600 mA. Series ULN-2020A will sustain 95 V in the OFF state.

All Series ULN-2000A Darlington arrays are furnished in a 16-pin dual in-line plastic package. These can also be supplied in a hermetic dual in-line package for use in military and aerospace applications.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
for any one Darlington pair
(unless otherwise noted)

Output Voltage, V_{CE} (Series ULN-2000, 2010A) .... 50 V
                   (Series ULN-2020A) .... 95 V
Input Voltage, V_{IN} (Series ULN-2002, 2003, 2004A) .... 30 V
               (Series ULN-2005A) .... 15 V
Continuous Collector Current, I_C (Series ULN-2000, 2020A) .... 500 mA
                      (Series ULN-2010A) .... 600 mA
Continuous Input Current, I_{IN} .... 25 mA
Power Dissipation, P_D (one Darlington pair) .... 1.0 W
              (total package) .... 2.0 W*
Operating Ambient Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −55°C to +150°C

*Derate at the rate of 16.67 mW/°C above +25°C.
Under normal operating conditions, these devices will sustain 350 mA per output with $V_{CE(SAT)}$ = 1.6 V at +70°C with a pulse width of 20 ms and a duty cycle of 34%.

ALLOWABLE AVERAGE POWER DISSIPATION
AS A FUNCTION OF AMBIENT TEMPERATURE
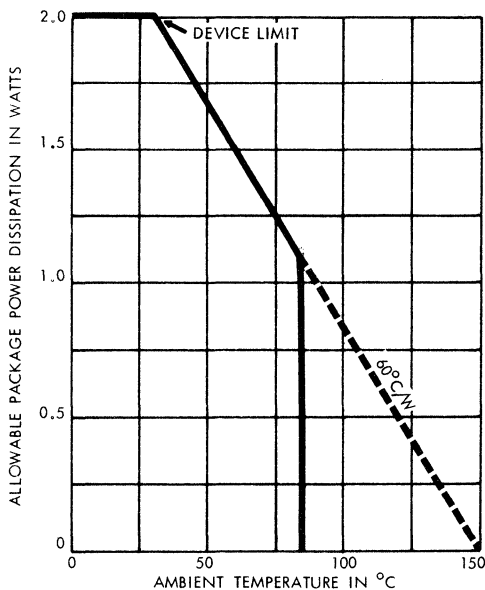
Dwg. No. A-9753C

PARTIAL SCHEMATICS

Series ULN-2001A
(each driver)
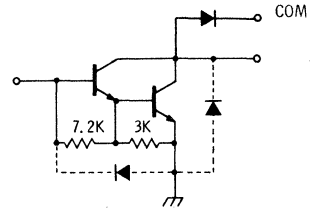
DWG. NO. A-9595

Series ULN-2002A
(each driver)
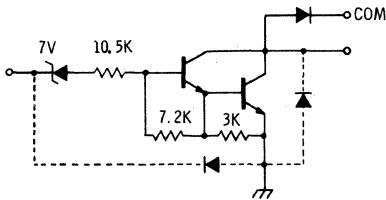
DWG. No. A-9650

Series ULN-2003A
(each driver)
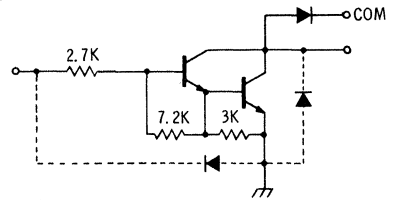
DWG. No. A-9651

Series ULN-2004A
(each driver)
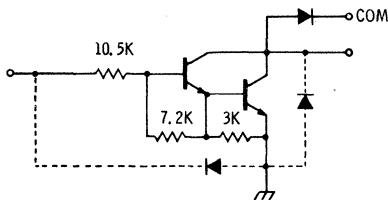
DWG. NO. A-9898A

Series ULN-2005A
(each driver)
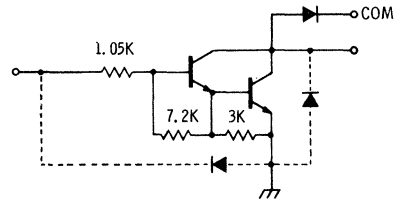
DWG. NO. A-10,228

SERIES ULN-2000A

ELECTRICAL CHARACTERISTICS AT +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			Units
					Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	1A	All	$V_{CE} = 50\,V$, $T_A = 25°C$	—	—	50	μA
				$V_{CE} = 50\,V$, $T_A = 70°C$	—	—	100	μA
		1B	ULN-2002A	$V_{CE} = 50\,V$, $T_A = 70°C$, $V_{IN} = 6.0\,V$	—	—	500	μA
			ULN-2004A	$V_{CE} = 50\,V$, $T_A = 70°C$, $V_{IN} = 1.0\,V$	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	$I_C = 100\,mA$, $I_B = 250\,\mu A$	—	0.9	1.1	V
				$I_C = 200\,mA$, $I_B = 350\,\mu A$	—	1.1	1.3	V
				$I_C = 350\,mA$, $I_B = 500\,\mu A$	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2002A	$V_{IN} = 17\,V$	—	0.82	1.25	mA
			ULN-2003A	$V_{IN} = 3.85\,V$	—	0.93	1.35	mA
			ULN-2004A	$V_{IN} = 5.0\,V$	—	0.35	0.5	mA
				$V_{IN} = 12\,V$	—	1.0	1.45	mA
			ULN-2005A	$V_{IN} = 3.0\,V$	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	$I_C = 500\,\mu A$, $T_A = 70°C$	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2002A	$V_{CE} = 2.0\,V$, $I_C = 300\,mA$	—	—	13	V
				$V_{CE} = 2.0\,V$, $I_C = 200\,mA$	—	—	2.4	V
			ULN-2003A	$V_{CE} = 2.0\,V$, $I_C = 250\,mA$	—	—	2.7	V
				$V_{CE} = 2.0\,V$, $I_C = 300\,mA$	—	—	3.0	V
			ULN-2004A	$V_{CE} = 2.0\,V$, $I_C = 125\,mA$	—	—	5.0	V
				$V_{CE} = 2.0\,V$, $I_C = 200\,mA$	—	—	6.0	V
				$V_{CE} = 2.0\,V$, $I_C = 275\,mA$	—	—	7.0	V
				$V_{CE} = 2.0\,V$, $I_C = 350\,mA$	—	—	8.0	V
			ULN-2005A	$V_{CE} = 2.0\,V$, $I_C = 350\,mA$	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2001A	$V_{CE} = 2.0\,V$, $I_C = 350\,mA$	1000	—	—	
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{PLH}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	$V_R = 50\,V$, $T_A = 25°C$	—	—	50	μA
				$V_R = 50\,V$, $T_A = 70°C$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	$I_F = 350\,mA$	—	1.7	2.0	V

3

SERIES ULN-2010A

ELECTRICAL CHARACTERISTICS AT +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			Units
					Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	1A	All	$V_{CE} = 50 \text{ V}, T_A = 25°C$	—	—	50	μA
				$V_{CE} = 50 \text{ V}, T_A = 70°C$	—	—	100	μA
		1B	ULN-2012A	$V_{CE} = 50 \text{ V}, T_A = 70°C, V_{IN} = 6.0 \text{ V}$	—	—	500	μA
			ULN-2014A	$V_{CE} = 50 \text{ V}, T_A = 70°C, V_{IN} = 1.0 \text{ V}$	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	$I_C = 200 \text{ mA}, I_B = 350 \mu\text{A}$	—	1.1	1.3	V
				$I_C = 350 \text{ mA}, I_B = 500 \mu\text{A}$	—	1.3	1.6	V
				$I_C = 500 \text{ mA}, I_B = 600 \mu\text{A}$	—	1.7	1.9	V
Input Current	$I_{IN(ON)}$	3	ULN-2012A	$V_{IN} = 17 \text{ V}$	—	0.82	1.25	mA
			ULN-2013A	$V_{IN} = 3.85 \text{ V}$	—	0.93	1.35	mA
			ULN-2014A	$V_{IN} = 5.0 \text{ V}$	—	0.35	0.5	mA
				$V_{IN} = 12 \text{ V}$	—	1.0	1.45	mA
			ULN-2015A	$V_{IN} = 3.0 \text{ V}$	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	$I_C = 500 \mu\text{A}, T_A = 70°C$	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2012A	$V_{CE} = 2.0 \text{ V}, I_C = 500 \text{ mA}$	—	—	17	V
			ULN-2013A	$V_{CE} = 2.0 \text{ V}, I_C = 250 \text{ mA}$	—	—	2.7	V
				$V_{CE} = 2.0 \text{ V}, I_C = 300 \text{ mA}$	—	—	3.0	V
				$V_{CE} = 2.0 \text{ V}, I_C = 500 \text{ mA}$	—	—	3.5	V
			ULN-2014A	$V_{CE} = 2.0 \text{ V}, I_C = 275 \text{ mA}$	—	—	7.0	V
				$V_{CE} = 2.0 \text{ V}, I_C = 350 \text{ mA}$	—	—	8.0	V
				$V_{CE} = 2.0 \text{ V}, I_C = 500 \text{ mA}$	—	—	9.5	V
			ULN-2015A	$V_{CE} = 2.0 \text{ V}, I_C = 500 \text{ mA}$	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2011A	$V_{CE} = 2.0 \text{ V}, I_C = 350 \text{ mA}$	1000	—	—	
				$V_{CE} = 2.0 \text{ V}, I_C = 500 \text{ mA}$	900	—	—	
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{PLH}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	$V_R = 50 \text{ V}, T_A = 25°C$	—	—	50	μA
				$V_R = 50 \text{ V}, T_A = 70°C$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	$I_F = 350 \text{ mA}$	—	1.7	2.0	V
				$I_F = 500 \text{ mA}$	—	2.1	2.5	V

SERIES ULN-2020A

ELECTRICAL CHARACTERISTICS AT +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			Units
					Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	1A	All	$V_{CE} = 95$ V, $T_A = 25°C$	—	—	50	μA
				$V_{CE} = 95$ V, $T_A = 70°C$	—	—	100	μA
		1B	ULN-2022A	$V_{CE} = 95$ V, $T_A = 70°C$, $V_{IN} = 6.0$ V	—	—	500	μA
			ULN-2024A	$V_{CE} = 95$ V, $T_A = 70°C$, $V_{IN} = 1.0$ V	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	$I_C = 100$ mA, $I_B = 250$ μA	—	0.9	1.1	V
				$I_C = 200$ mA, $I_B = 350$ μA	—	1.1	1.3	V
				$I_C = 350$ mA, $I_B = 500$ μA	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2022A	$V_{IN} = 17$ V	—	0.82	1.25	mA
			ULN-2023A	$V_{IN} = 3.85$ V	—	0.93	1.35	mA
			ULN-2024A	$V_{IN} = 5.0$ V	—	0.35	0.5	mA
				$V_{IN} = 12$ V	—	1.0	1.45	mA
			ULN-2025A	$V_{IN} = 3.0$ V	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	$I_C = 500$ μA, $T_A = 70°C$	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2022A	$V_{CE} = 2.0$ V, $I_C = 300$ mA	—	—	13	V
			ULN-2023A	$V_{CE} = 2.0$ V, $I_C = 200$ mA	—	—	2.4	V
				$V_{CE} = 2.0$ V, $I_C = 250$ mA	—	—	2.7	V
				$V_{CE} = 2.0$ V, $I_C = 300$ mA	—	—	3.0	V
			ULN-2024A	$V_{CE} = 2.0$ V, $I_C = 125$ mA	—	—	5.0	V
				$V_{CE} = 2.0$ V, $I_C = 200$ mA	—	—	6.0	V
				$V_{CE} = 2.0$ V, $I_C = 275$ mA	—	—	7.0	V
				$V_{CE} = 2.0$ V, $I_C = 350$ mA	—	—	8.0	V
			ULN-2025A	$V_{CE} = 2.0$ V, $I_C = 350$ mA	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2021A	$V_{CE} = 2.0$ V, $I_C = 350$ mA	1000	—	—	
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{PLH}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Turn-Off Delay	t_{PHL}	—	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μs
Clamp Diode Leakage Current	I_R	6	All	$V_R = 95$ V, $T_A = 25°C$	—	—	50	μA
				$V_R = 95$ V, $T_A = 70°C$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	$I_F = 350$ mA	—	1.7	2.0	V

3

TEST FIGURES

FIGURE 1A

FIGURE 1B

FIGURE 2

FIGURE 3

FIGURE 4

FIGURE 5

FIGURE 6

FIGURE 7

PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE
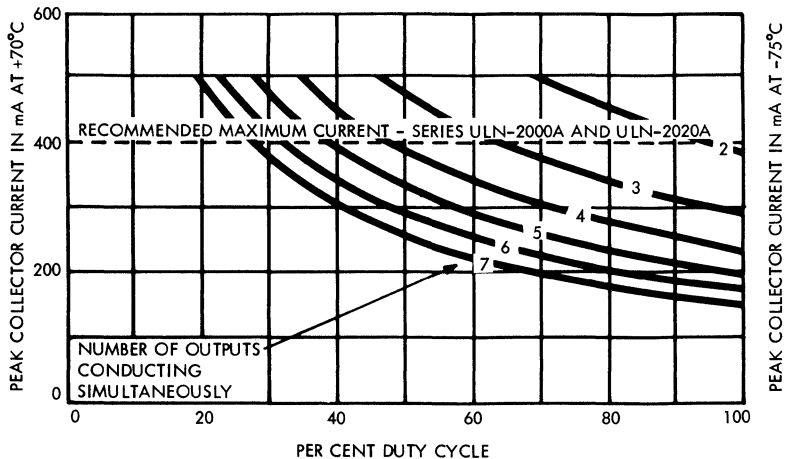
Dwg.No. A-9752B

3

COLLECTOR CURRENT
AS A FUNCTION OF SATURATION VOLTAGE

DWG. NO. A-9754B

COLLECTOR CURRENT
AS A FUNCTION OF INPUT CURRENT

DWG. NO. A-10,872A

INPUT CURRENT
AS A FUNCTION OF INPUT VOLTAGE

SERIES ULN-2002A

DWG. NO. A-9757A

SERIES ULN-2003A

DWG. NO. A-9756B

SERIES ULN-2005A

DWG. NO. A-10.258

SERIES ULN-2004A

DWG. NO. A-9899A
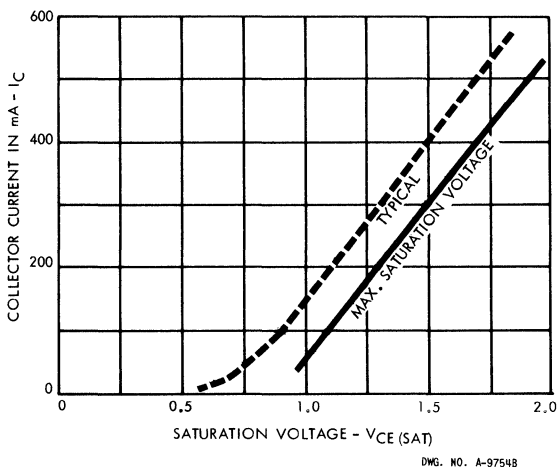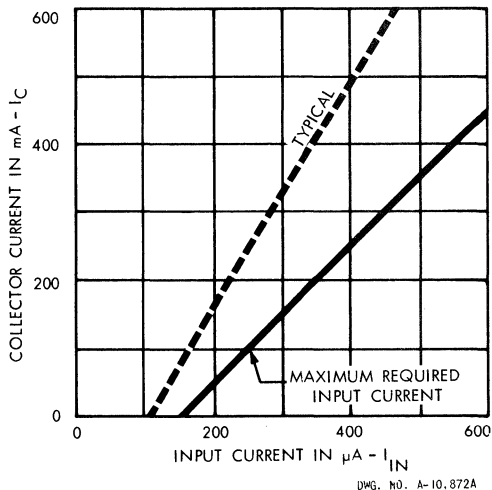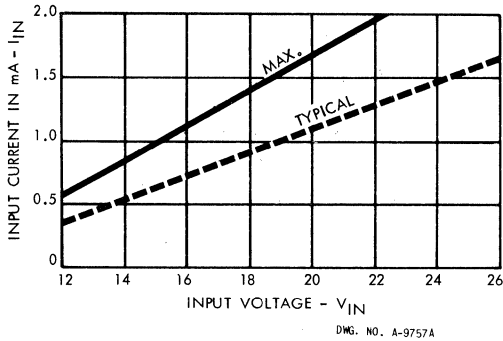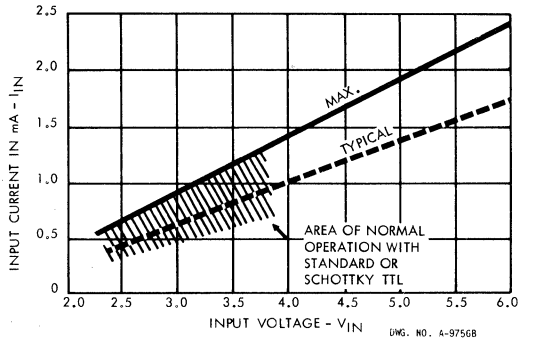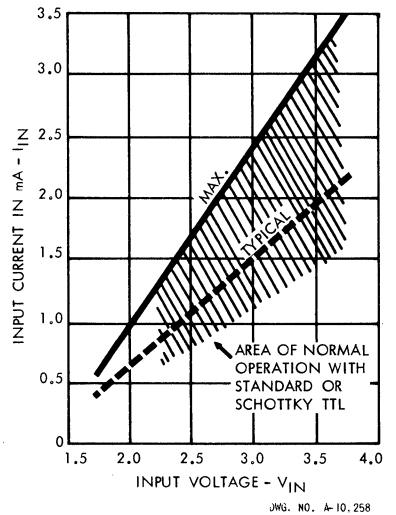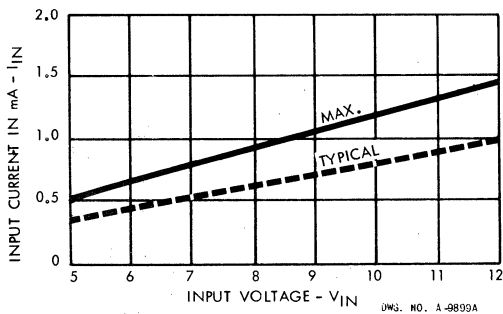
TYPICAL APPLICATIONS

PMOS TO LOAD

ULN-2002A

DWG. No. A-9652

TTL TO LOAD

ULN-2003/5A

DWG. NO. A-9653A
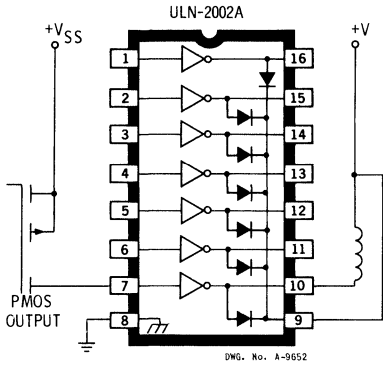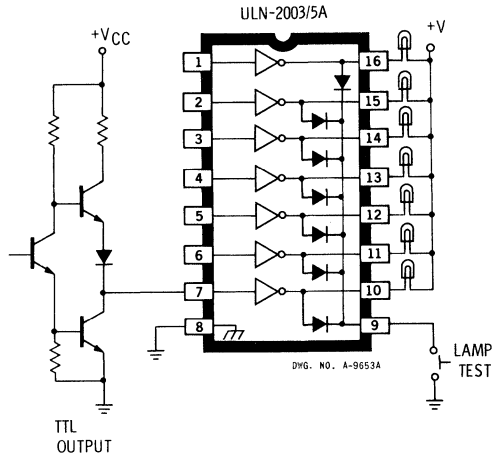
BUFFER FOR HIGH-CURRENT LOAD

ULN-2004A

DWG. NO. A-9654A
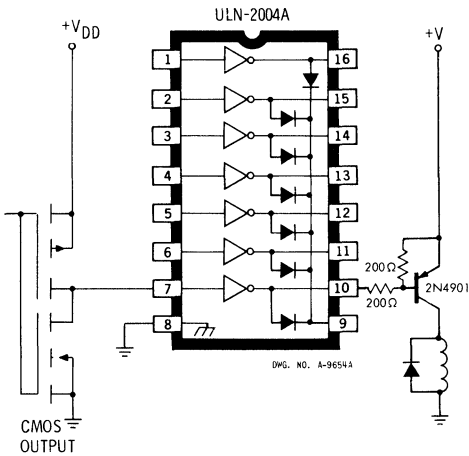
USE OF PULL-UP RESISTORS
TO INCREASE DRIVE CURRENT

ULN-2003A

DWG. NO. A-10,175
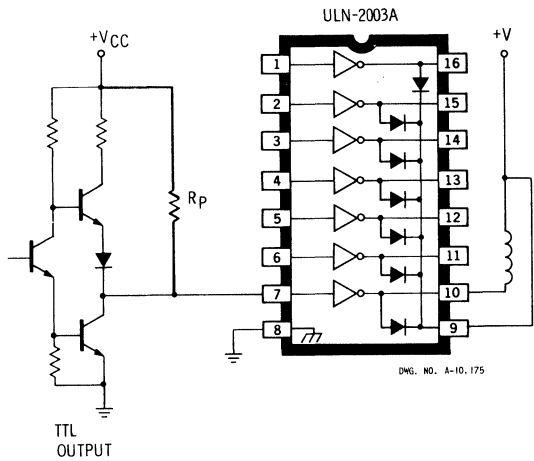
ULN-2061M THROUGH ULN-2077B
1.5A DARLINGTON SWITCHES

FEATURES

- TTL, DTL, PMOS, CMOS Compatible Inputs
- Transient-Protected Outputs
- Loads to 480 Watts
- Plastic Dual In-Line Packages
- Heat-Sink Contact Tabs on Quad Arrays

DWG. NO. A-10.230A

ULN-2061M
ULN-2062M

HIGH-VOLTAGE, HIGH-CURRENT Darlington arrays ULN-2061M through ULN-2077B are designed as interface between low-level logic and a variety of peripheral loads such as relays, solenoids, d-c and stepper motors, multiplexed LED and incandescent displays, heaters, and similar loads to 480 watts (1.5 A per output, 80 V, 26% duty cycle).

The devices have a minimum output breakdown of 50 V and a minimum $V_{CE(SUS)}$ of 35 V measured at 100 mA, or a minimum output breakdown of 80 V and a minimum $V_{CE(SUS)}$ of 50 V.

Dual-driver arrays ULN-2061M and ULN-2062M are used for common-emitter (externally connected), or emitter-follower applications. Both devices are supplied in miniature 8-pin dual in-line plastic packages.
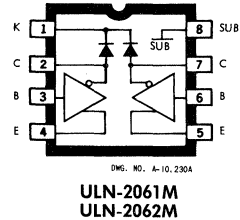
Quad drivers ULN-2064B, ULN-2065B, ULN-2068B and ULN-2069B are intended for use with TTL, low-speed TTL, and 5 V MOS logic. Types ULN-2065B and ULN-2069B are selected for the 80 V minimum output breakdown specification. Types ULN-2068B and ULN-2069B have pre-driver stages and are most suitable for applications requiring high gain (low input-current loading).

DWG. NO. A-9765A
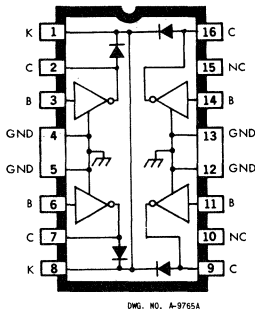
ULN-2064B
ULN-2065B
ULN-2066B
ULN-2067B

DWG. NO. A-10.310
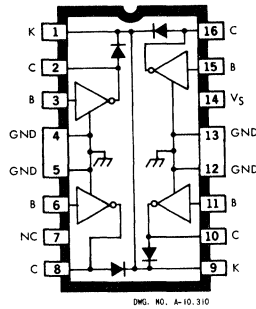
ULN-2068B
ULN-2069B
ULN-2070B
ULN-2071B

DWG. NO. A-9766A
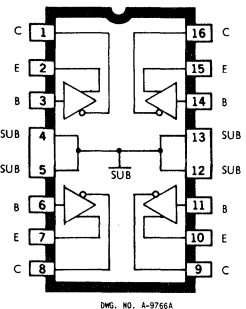
ULN-2074B
ULN-2075B
ULN-2076B
ULN-2077B

Types ULN-2066B, ULN-2067B, ULN-2070B and ULN-2071B are similar to the preceding quad drivers except that they are designed for use with PMOS and 12 V CMOS logic. The ULN-2070B and ULN-2071B both have a predriver stage and are best suited for use where input current is restricted by MOS output ratings.

Isolated Darlington arrays ULN-2074B through ULN-2077B are identical to Types ULN-2064B through ULN-2067B except for the isolated Darlington pin-out and the deletion of suppression diodes. These switches are for emitter-follower or similar isolated-Darlington applications.

All quad Darlington arrays (suffix "B" devices) are supplied in a 16-pin plastic dual in-line package with heat-sink contact tabs. A copper-alloy lead frame provides maximum power dissipation using standard cooling methods. This lead configuration facilitates attachment of external heat sinks for increased power dissipation with standard IC sockets and printed wiring boards.

SELECTION GUIDE

Part Number	MAX. V_{CEX}	MIN. $V_{CE(SUS)}$	MAX. V_{IN}	Application
ULN-2061M	50 V	35 V	30 V	TTL, DTL, Schottky TTL,
ULN-2062M	80 V	50 V	60 V	and 5 V CMOS
ULN-2064B	50 V	35 V	15 V	TTL, DTL, Schottky TTL
ULN-2065B	80 V	50 V	15 V	and 5 V CMOS
ULN-2066B	50 V	35 V	30 V	6 to 15 V CMOS
ULN-2067B	80 V	50 V	30 V	and PMOS
ULN-2068B	50 V	35 V	15 V	TTL, DTL, Schottky TTL,
ULN-2069B	80 V	50 V	15 V	and 5 V CMOS
ULN-2070B	50 V	35 V	30 V	6 to 15 V CMOS
ULN-2071B	80 V	50 V	30 V	and PMOS
ULN-2074B	50 V	35 V	30 V	General Purpose
ULN-2075B	80 V	50 V	60 V	
ULN-2076B	50 V	35 V	30 V	6 to 15 V CMOS
ULN-2077B	80 V	50 V	60 V	and PMOS

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
for Any One Driver
(unless otherwise noted)

Output Voltage, V_{CEX} . . . . See Guide
Output Sustaining Voltage, $V_{CE(SUS)}$ . . . . See Guide
Output Current, I_{OUT} (Note 1) . . . . 1.75 A
Input Voltage, V_{IN} (Note 2) . . . . See Guide
Input Current, I_B (Note 3) . . . . 25 mA
Supply Voltage, V_S (ULN-2068/69B) . . . . 10 V
(ULN-2070/71B) . . . . 20 V
Total Package Power Dissipation . . . . See Graph
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −55°C to −150°C

NOTES:
1. Allowable combinations of output current, number of outputs conducting, and duty cycle are shown on following pages.
2. Input voltage is referenced to the substrate (no connection to other pins) for Type ULN-2061/62M and ULN-2074/75/76/77B; reference is ground for all other types.
3. Input current may be limited by maximum allowable input voltage.

ALLOWABLE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE

Dwg. No. A-10,362A

ULN-2061M AND ULN-2062M

PARTIAL SCHEMATIC
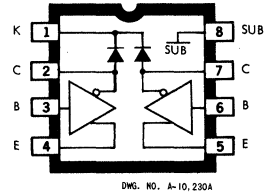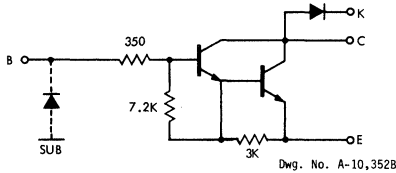
Dwg. No. A-10,352B

DWG. NO. A-10,230A

ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	1	ULN-2061M	$V_{CE} = 50\,V$	—	100	μA
				$V_{CE} = 50\,V, T_A = 70°C$	—	500	μA
			ULN-2062M	$V_{CE} = 80\,V$	—	100	μA
				$V_{CE} = 80\,V, T_A = 70°C$	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN-2061M	$I_C = 100\,mA, V_{IN} = 0.4\,V$	35	—	V
			ULN-2062M	$I_C = 100\,mA, V_{IN} = 0.4\,V$	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	Both	$I_C = 500\,mA, I_B = 625\,\mu A$	—	1.1	V
				$I_C = 750\,mA, I_B = 935\,\mu A$	—	1.2	V
				$I_C = 1.0\,A, I_B = 1.25\,mA$	—	1.3	V
				$I_C = 1.25\,A^*, I_B = 2.0\,mA$	—	1.4	V
			ULN-2062M	$I_C = 1.5\,A^*, I_B = 2.25\,mA$	—	1.5	V
Input Current	$I_{IN(ON)}$	4	Both	$V_{IN} = 2.4\,V$	1.4	4.3	mA
				$V_{IN} = 3.75\,V$	3.3	9.6	mA
Input Voltage	$V_{IN(ON)}$	5	Both	$V_{CE} = 2.0\,V, I_C = 1.0\,A$	—	2.0	V
			ULN-2061M	$V_{CE} = 2.0\,V, I_C = 1.25\,A^*$	—	2.5	V
			ULN-2062M	$V_{CE} = 2.0\,V, I_C = 1.5\,A^*$	—	2.5	V
Turn-On Delay	t_{PLH}	—	Both	$0.5\,E_{in}$ to $0.5\,E_{out}$	—	1.0	μs
Turn-Off Delay	t_{PHL}	—	Both	$0.5\,E_{in}$ to $0.5\,E_{out}$	—	1.5	μs
Clamp Diode Leakage Current	I_R	6	ULN-2061M	$V_R = 50\,V$	—	50	μA
				$V_R = 50\,V, T_A = 70°C$	—	100	μA
			ULN-2062M	$V_R = 80\,V$	—	50	μA
				$V_R = 80\,V, T_A = 70°C$	—	100	μA
Clamp Diode Forward Voltage	V_F	7	Both	$I_F = 1.0\,A$	—	1.75	V
				$I_F = 1.5\,A$	—	2.0	V

*Pulse-Test

ULN-2064B THROUGH ULN-2067B

PARTIAL SCHEMATIC

Dwg. No. A-10,353A

ULN-2064B }
ULN-2065B } $R_{IN} = 350\ \Omega$

ULN-2066B }
ULN-2067B } $R_{IN} = 3\ k\Omega$

(SIMILAR TO ULN-2074B THROUGH ULN-2077B)
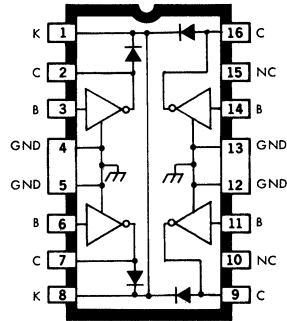
DWG. NO. A-9765A

3

ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Min.	Max.	Units
Output Leakage Current	I_{CEX}	1	ULN-2064/66B	$V_{CE} = 50\ V$	—	100	μA
				$V_{CE} = 50\ V, T_A = 70°C$	—	500	μA
			ULN-2065/67B	$V_{CE} = 80\ V$	—	100	μA
				$V_{CE} = 80\ V, T_A = 70°C$	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN-2064/66B	$I_C = 100\ mA, V_{IN} = 0.4\ V$	35	—	V
			ULN-2065/67B	$I_C = 100\ mA, V_{IN} = 0.4\ V$	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	All	$I_C = 500\ mA, I_B = 625\ \mu A$	—	1.1	V
				$I_C = 750\ mA, I_B = 935\ \mu A$	—	1.2	V
				$I_C = 1.0\ A, I_B = 1.25\ mA$	—	1.3	V
				$I_C = 1.25\ A, I_B = 2.0\ mA$	—	1.4	V
			ULN-2065/67B	$I_C = 1.5\ A, I_B = 2.25\ mA$	—	1.5	V
Input Current	$I_{IN(ON)}$	4	ULN-2064/65B	$V_{IN} = 2.4\ V$	1.4	4.3	mA
				$V_{IN} = 3.75\ V$	3.3	9.6	mA
			ULN-2066/67B	$V_{IN} = 5.0\ V$	0.6	1.8	mA
				$V_{IN} = 12\ V$	1.7	5.2	mA
Input Voltage	$V_{IN(ON)}$	5	ULN-2064/65B	$V_{CE} = 2.0\ V, I_C = 1.0\ A$	—	2.0	V
			ULN-2064B	$V_{CE} = 2.0\ V, I_C = 1.25\ A$	—	2.5	V
			ULN-2065B	$V_{CE} = 2.0\ V, I_C = 1.5\ A$	—	2.5	V
			ULN-2066/67B	$V_{CE} = 2.0\ V, I_C = 1.0\ A$	—	6.5	V
			ULN-2066B	$V_{CE} = 2.0\ V, I_C = 1.25\ A$	—	10	V
			ULN-2067B	$V_{CE} = 2.0\ V, I_C = 1.5\ A$	—	10	V
Turn-On Delay	t_{PLH}	—	All	$0.5\ E_{in}$ to $0.5\ E_{out}$	—	1.0	μs
Turn-Off Delay	t_{PHL}	—	All	$0.5\ E_{in}$ to $0.5\ E_{out}$	—	1.5	μs
Clamp Diode Leakage Current	I_R	6	ULN-2064/66B	$V_R = 50\ V$	—	50	μA
				$V_R = 50\ V, T_A = 70°C$	—	100	μA
			ULN-2065/67B	$V_R = 80\ V$	—	50	μA
				$V_R = 80\ V, T_A = 70°C$	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	$I_F = 1.0\ A$	—	1.75	V
				$I_F = 1.5\ A$	—	2.0	V

ULN-2068B THROUGH ULN-2071B

PARTIAL SCHEMATIC
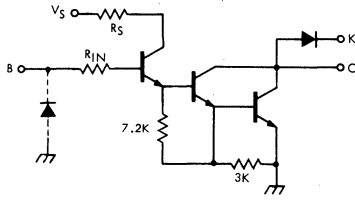
ULN-2068B
ULN-2069B $\}$ $R_{IN} = 2.5\ k\Omega,\ R_S = 900\ \Omega$

ULN-2070B
ULN-2071B $\}$ $R_{IN} = 11.6\ k\Omega,\ R_S = 3.4\ k\Omega$
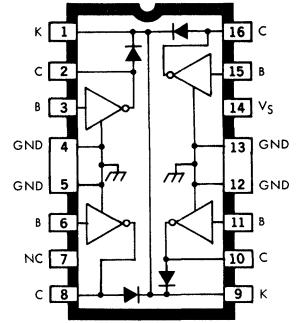
DWG.NO. A-10,354B

DWG. NO. A-10.310

ELECTRICAL CHARACTERISTICS at +25°C, $V_S = 5.0$ V (ULN-2068/69B) or $V_S = 12$ V (ULN-2070/71B) (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Min.	Max.	Units
Output Leakage Current	I_{CEX}	1	ULN-2068/70B	$V_{CE} = 50$ V	—	100	μA
				$V_{CE} = 50$ V, $T_A = 70°C$	—	500	μA
			ULN-2069/71B	$V_{CE} = 80$ V	—	100	μA
				$V_{CE} = 80$ V, $T_A = 70°C$	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN-2068/70B	$I_C = 100$ mA, $V_{IN} = 0.4$ V	35	—	V
			ULN-2069/71B	$I_C = 100$ mA, $V_{IN} = 0.4$ V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	ULN-2068/69B	$I_C = 500$ mA, $V_{IN} = 2.75$ V	—	1.1	V
				$I_C = .750$ mA, $V_{IN} = 2.75$ V	—	1.2	V
				$I_C = 1.0$ A, $V_{IN} = 2.75$ V	—	1.3	V
				$I_C = 1.25$ A, $V_{IN} = 2.75$ V	—	1.4	V
			ULN-2069B	$I_C = 1.5$ A, $V_{IN} = 2.75$ V	—	1.5	V
			ULN-2070/71B	$I_C = 500$ mA, $V_{IN} = 5.0$ V	—	1.1	V
				$i_C = 750$ mA, $V_{IN} = 5.0$ V	—	1.2	V
				$I_C = 1.0$ A, $V_{IN} = 5.0$ V	—	1.3	V
				$I_C = 1.25$ A, $V_{IN} = 5.0$ V	—	1.4	V
			ULN-2071B	$I_C = 1.5$ A, $V_{IN} = 5.0$ V	—	1.5	V
Input Current	$I_{IN(ON)}$	4	ULN-2068/69B	$V_{IN} = 2.75$ V	—	550	μA
				$V_{IN} = 3.75$ V	—	1000	μA
			ULN-2070/71B	$V_{IN} = 5.0$ V	—	400	μA
				$V_{IN} = 12$ V	—	1250	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2068B	$V_{CE} = 2.0$ V, $I_C = 1.25$ A	—	2.75	V
			ULN-2069B	$V_{CE} = 2.0$ V, $I_C = 1.5$ A	—	2.75	V
			ULN-2070B	$V_{CE} = 2.0$ V, $I_C = 1.25$ A	—	5.0	V
			ULN2071B	$V_{CE} = 2.0$ V, $I_C = 1.5$ A	—	5.0	V
Supply Current	I_S	8	ULN-2068/69B	$I_C = 500$ mA, $V_{IN} = 2.75$ V	—	6.0	mA
			ULN-2070/71B	$I_C = 500$ mA, $V_{IN} = 5.0$ V	—	4.5	mA
Turn-On Delay	t_{PLH}	—	All	0.5 E_{in} to 0.5 E_{out}	—	1.0	μs
Turn-Off Delay	t_{PHL}	—	All	0.5 E_{in} to 0.5 E_{out}, $I_C = 1.25$ A	—	1.5	μs
Clamp Diode Leakage Current	I_R	6	ULN-2068/70B	$V_R = 50$ V	—	50	μA
				$V_R = 50$ V, $T_A = 70°C$	—	100	μA
			ULN-2069/71B	$V_R = 80$ V	—	50	μA
				$V_R = 80$ V, $T_A = 70°C$	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	$I_F = 1.0$ A	—	1.75	V
				$I_F = 1.5$ A	—	2.0	V

ULN-2074B THROUGH ULN-2077B

PARTIAL SCHEMATIC
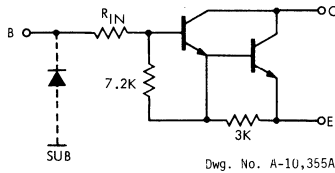
Dwg. No. A-10,355A

$\left.\begin{array}{c}\text{ULN-2074B}\\\text{ULN-2075B}\end{array}\right\}$ $R_{IN} = 350\,\Omega$

$\left.\begin{array}{c}\text{ULN-2076B}\\\text{ULN-2077B}\end{array}\right\}$ $R_{IN} = 3\,k\Omega$
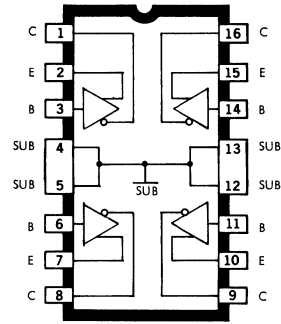
(SIMILAR TO ULN-2064B THROUGH ULN-2067B)

DWG. NO. A-9766A

ELECTRICAL CHARACTERISTICS at +25°C (unless otherwise noted)

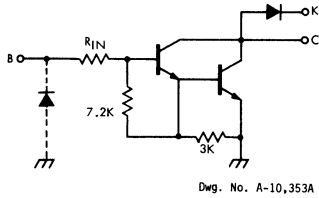| Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	1	ULN-2074/76B	$V_{CE} = 50\,V$	—	100	μA
				$V_{CE} = 50\,V,\ T_A = 70°C$	—	500	μA
			ULN-2075/77B	$V_{CE} = 80\,V$	—	100	μA
				$V_{CE} = 80\,V,\ T_A = 70°C$	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	ULN-2074/76B	$I_C = 100\,mA,\ V_{IN} = 0.4\,V$	35	—	V
			ULN-2075/77B	$I_C = 100\,mA,\ V_{IN} = 0.4\,V$	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	3	All	$I_C = 500\,mA,\ I_B = 625\,\mu A$	—	1.1	V
				$I_C = 750\,mA,\ I_B = 935\,\mu A$	—	1.2	V
				$I_C = 1.0\,A,\ I_B = 1.25\,mA$	—	1.3	V
				$I_C = 1.25\,A,\ I_B = 2.0\,mA$	—	1.4	V
			ULN-2075/77B	$I_C = 1.5\,A,\ I_B = 2.25\,mA$	—	1.5	V
Input Current	$I_{IN(ON)}$	4	ULN-2074/75B	$V_{IN} = 2.4\,V$	1.4	4.3	mA
				$V_{IN} = 3.75\,V$	3.3	9.6	mA
			ULN-2076/77B	$V_{IN} = 5.0\,V$	0.6	1.8	mA
				$V_{IN} = 12\,V$	1.7	5.2	mA
Input Voltage	$V_{IN(ON)}$	5	ULN-2074/75B	$V_{CE} = 2.0\,V,\ I_C = 1.0\,A$	—	2.0	V
			ULN-2074B	$V_{CE} = 2.0\,V,\ I_C = 1.25\,A$	—	2.5	V
			ULN-2075B	$V_{CE} = 2.0\,V,\ I_C = 1.5\,A$	—	2.5	V
			ULN-2076/77B	$V_{CE} = 2.0\,V,\ I_C = 1.0\,A$	—	6.5	V
			ULN-2076B	$V_{CE} = 2.0\,V,\ I_C = 1.25\,A$	—	10	V
			ULN-2077B	$V_{CE} = 2.0\,V,\ I_C = 1.5\,A$	—	10	V
Turn-On Delay	t_{PLH}	—	All	$0.5\,E_{in}$ to $0.5\,E_{out}$	—	1.0	μs
Turn-Off Delay	t_{PHL}	—	All	$0.5\,E_{in}$ to $0.5\,E_{out}$	—	1.5	μs

TEST FIGURES
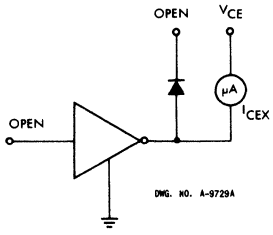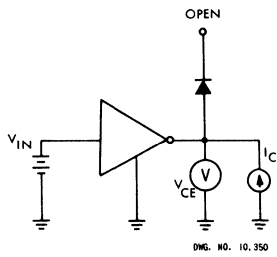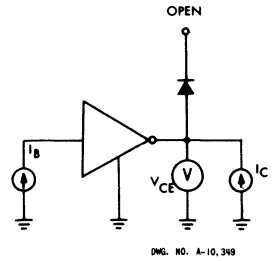
Figure 1
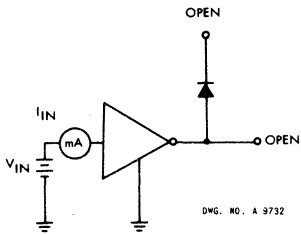
Figure 2

Figure 3

Figure 4
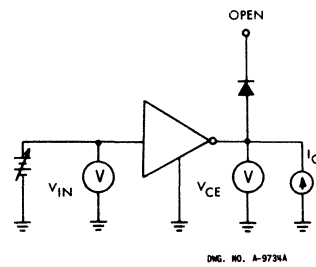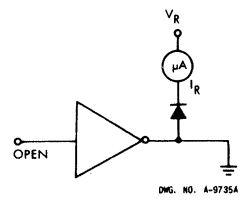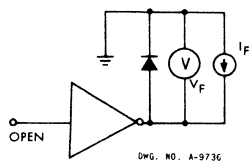
Figure 5
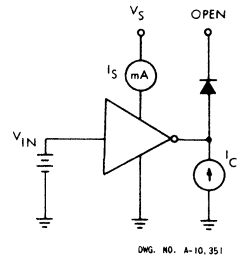
Figure 6

Figure 7

Figure 8

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

Dwg. No. A-10,356

Dwg. No. A-10,360A

Dwg. No. A-10,361

Dwg. No. A-10,398A

Dwg. No. A-10,400A
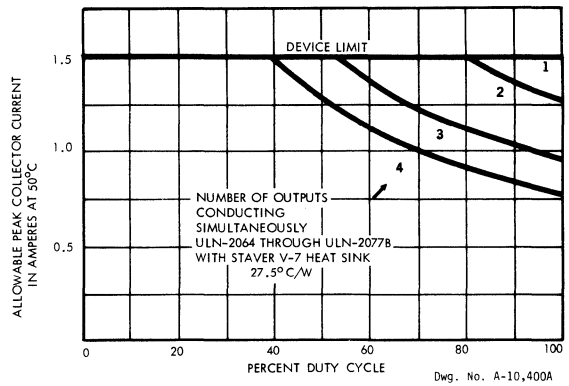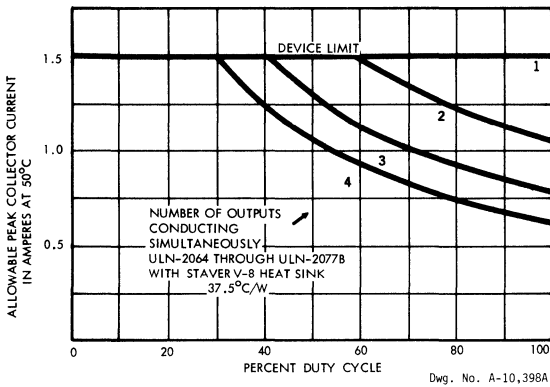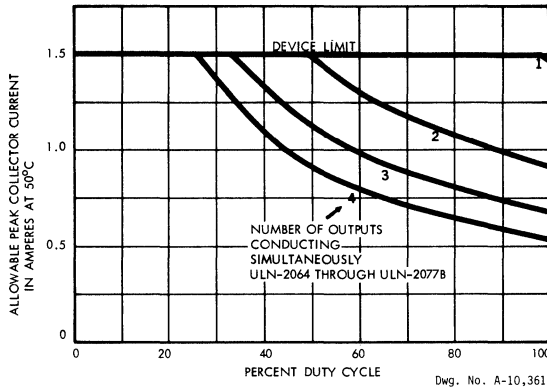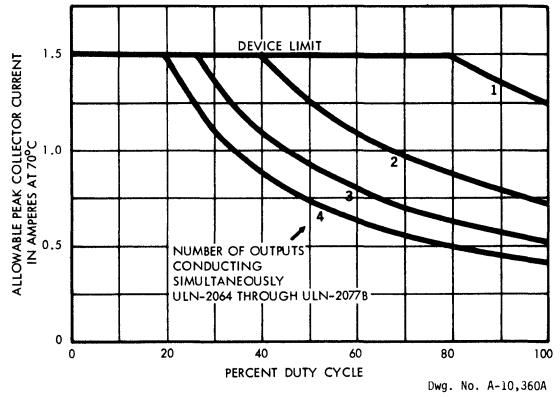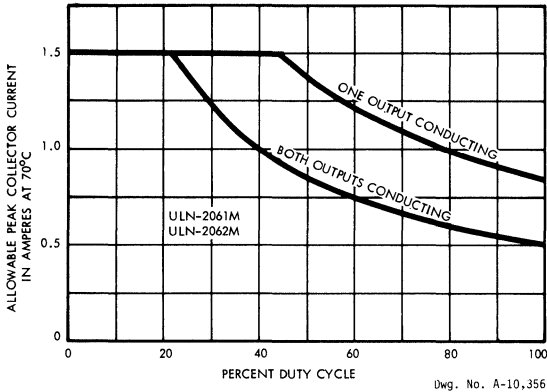
PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE (Continued)
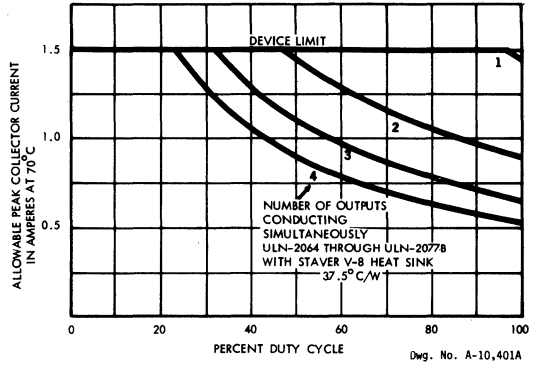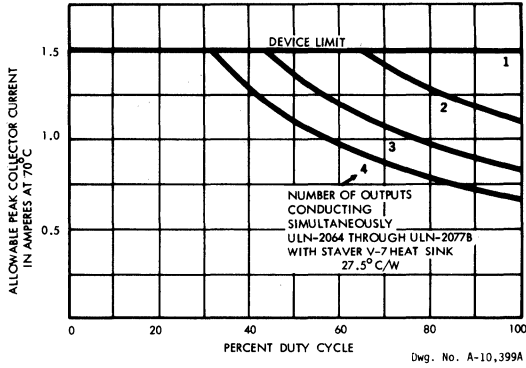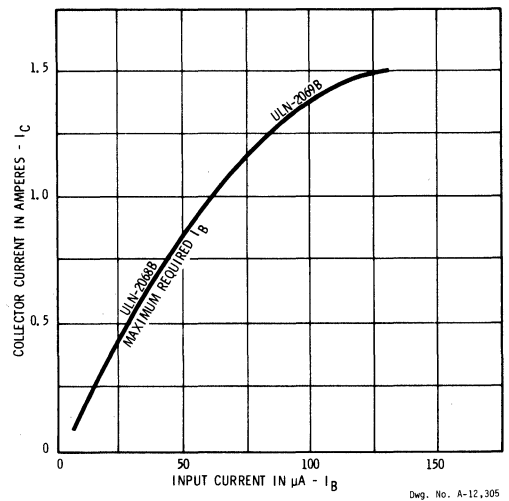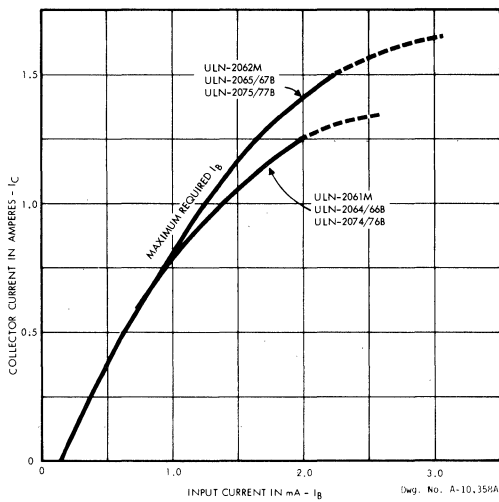
Dwg. No. A-10,399A

Dwg. No. A-10,401A

COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT AT +25°C

Dwg. No. A-10,35RA

Dwg. No. A-12,305

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE AT +25°C

ULN-2061/62M
ULN-2064/65B
ULN-2074/75B

MAXIMUM

MINIMUM

AREA OF NORMAL
OPERATION WITH
STANDARD OR
LOW-SPEED TTL

INPUT CURRENT IN mA - I_{IN}

INPUT VOLTAGE - V_{IN}

Dwg. No. A-10,363B

ULN-2066/67B
ULN-2076/77B

MAXIMUM

TYPICAL

MINIMUM

INPUT CURRENT IN mA - I_{IN}

INPUT VOLTAGE - V_{IN}

Dwg. No. A-10,357B

3

ULN-2068/69B

MAXIMUM

MINIMUM

INPUT CURRENT IN mA - I_{IN}

INPUT VOLTAGE - V_{IN}

Dwg. No. A-12,306

TYPICAL APPLICATION

+V   +V

ULN-2061/62M

NC

SUB

θ_A θ_B

M

SUB

θ_B θ_A

DWG. NO. A-10,959
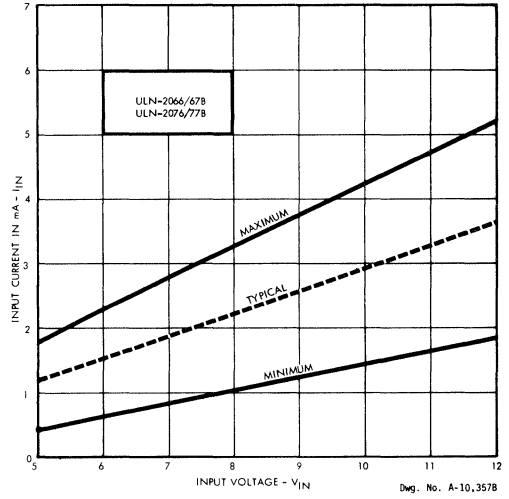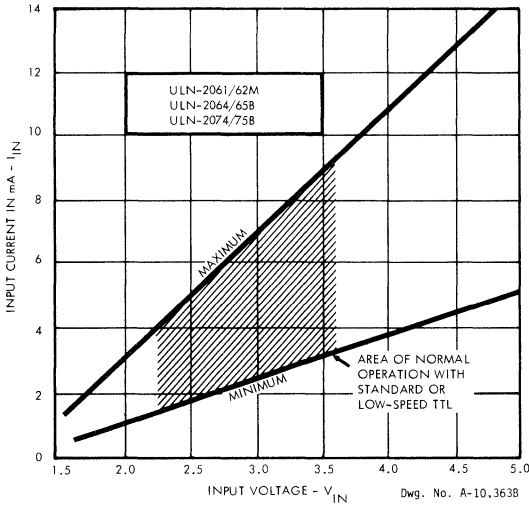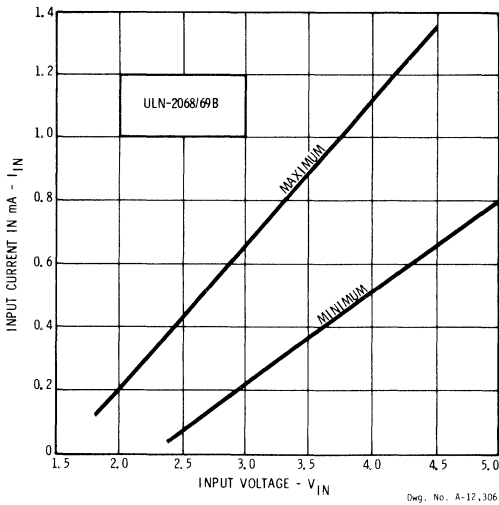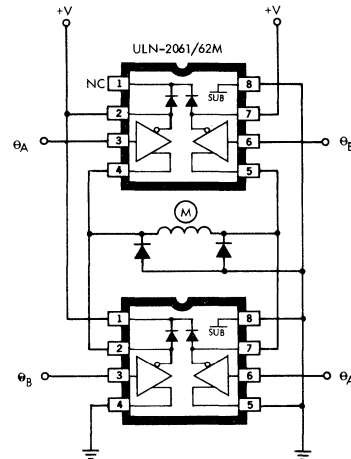
BIDIRECTIONAL MOTOR CONTROL

TYPICAL APPLICATIONS (Continued)
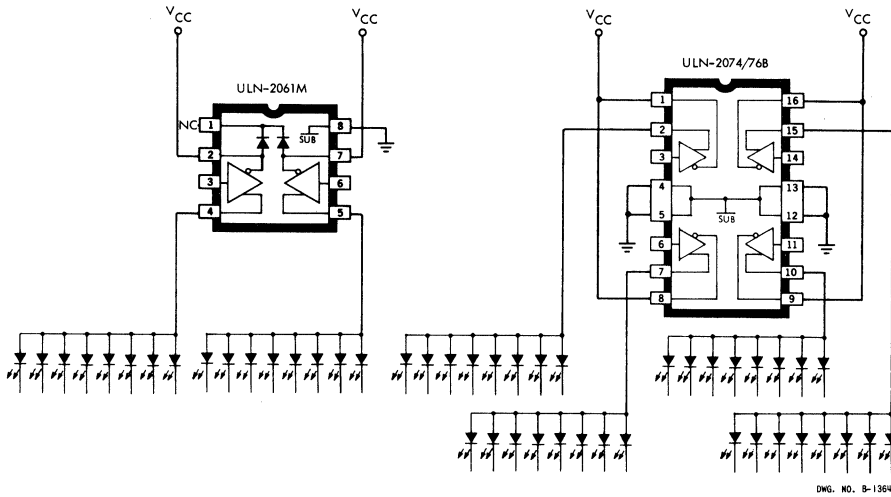
DWG. NO. B-1364

COMMON-ANODE LED DRIVERS
(Series UDN-2980A devices can be used in similar applications at currents of up to 500 mA)
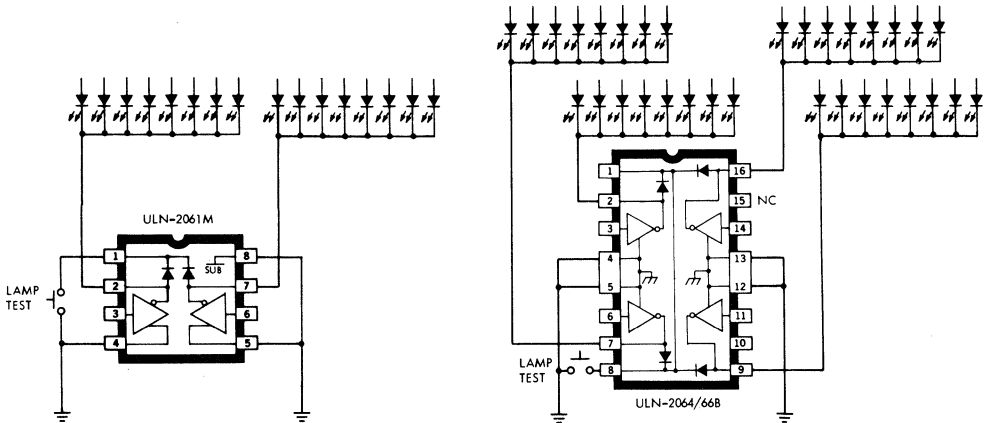
DWG. NO. B-1365

COMMON-CATHODE LED DRIVERS
(Types ULN-2068/70B are also applicable)

UDN-2541B/W AND UDN-2542B/W
QUAD NAND-GATE POWER DRIVERS

FEATURES

- TTL, CMOS, PMOS, NMOS Compatible
- 1.5 A Continuous Output Current
- Efficient Input/Output Pin Structure
- Low Output Saturation Voltage
- SN75437NE Equivalent

COMBINING NAND LOGIC GATES and high-current bipolar outputs, the four power and relay drivers in this series can provide interface between low-level signal-processing circuits and medium-power loads in extremely harsh environments. Each of the four independent outputs of these devices can sink up to 1.5 A in the ON state.

Type UDN-2541B/W and UDN-2542B/W integrated circuits differ only in output-voltage ratings and high-current saturation limits. Types UDN-2541B and UDN-2541W are rated at 60 V and 1.25 A. Types UDN-2542B and UDN-2542W are

Dwg. No. A-11,797

UDN-2541W
UDN-2542W

Dwg. No. A-11,561

UDN-2541B
UDN-2542B

rated at 1.0 A with a breakdown voltage of greater than 80 V. All devices have a minimum output sustaining voltage of 35 V. Inputs are compatible with most TTL, DTL, LSTTL, and 5 V to 15 V CMOS and PMOS logic.

Types UDN-2541B and UDN-2542B are supplied in 16-pin dual in-line packages with heat-sink contact tabs. This configuration enables easy attachment of an inexpensive heat sink and fits a standard integrated circuit socket or printed wiring board layout. The outputs include transient suppression diodes for inductive loads such as relays, solenoids, and d-c and stepping motors.

Types UDN-2541W and UDN-2542W, with higher power-dissipation ratings, are in 12-pin single in-line power-tab packages that allow efficient attachment of external heat sinks for maximum allowable package power dissipation. The tab is at ground potential and needs no insulation. These devices are used to drive high-current incandescent lamps, LEDs, heaters, and (with external transient suppression) high-voltage inductive loads.

ABSOLUTE MAXIMUM RATINGS
at + 25°C Free-Air Temperature

Output Voltage, V_{CE} (UDN-2541B/W) .... 60 V
(UDN-2542B/W) .... 80 V
Output Current, I_{OUT} .... 1.5 A
Supply Voltage, V_{CC} .... 18 V
Input Voltage, V_{IN} .... 18 V
Power Dissipation, P_D (Each Driver) .... 2.5 W
(Total Package) .... See Graph
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range, V_{CC} .... 4.5 V to 7 V
Input Voltage, $V_{IN(1)}$ .... 2 V to 7 V
$V_{IN(0)}$ .... <0.8 V

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE

UDN-2541B
UDN-2542B
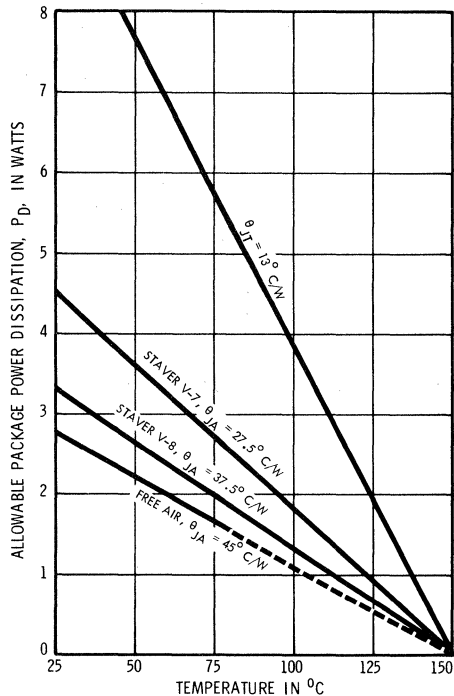
UDN-2541W
UDN-2542W
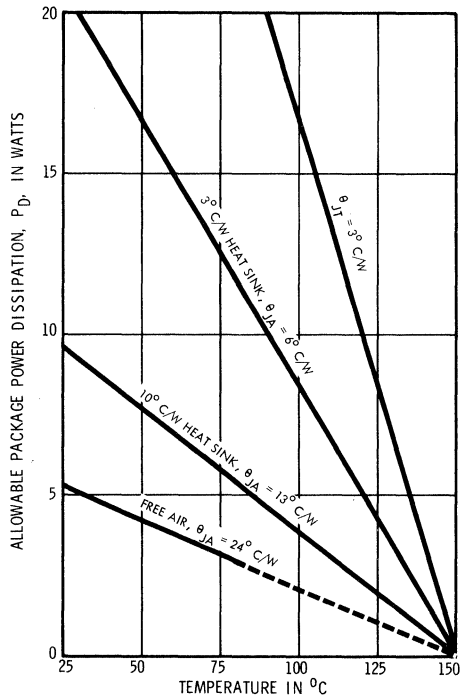
Dwg. No. A-11,793A

Dwg. No. A-11,794

ELECTRICAL CHARACTERISTICS at V_{cc} = 4.5 V to 5.5 V, T_A = +25°C (unless otherwise noted)

Characteristic	Symbol	Test Conditions	UDN-2541B/W Min.	UDN-2541B/W Max.	UDN-2542B/W Min.	UDN-2542B/W Max.	Units
Output Leakage Current	I_{CEX}	V_{OUT} = 60 V, V_{IN} = 0.8 V, V_{ENABLE} = 2.0 V	—	100	—	—	µA
		V_{OUT} = 60 V, V_{IN} = 2.0 V, V_{ENABLE} = 0.8 V	—	100	—	—	µA
		V_{OUT} = 80 V, V_{IN} = 0.8 V, V_{ENABLE} = 2.0 V	—	—	—	100	µA
		V_{OUT} = 80 V, V_{IN} = 2.0 V, V_{ENABLE} = 0.8 V	—	—	—	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_{OUT} = 100 mA, V_{IN} = V_{ENABLE} = 0.8 V	35	—	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	I_{OUT} = 250 mA, V_{IN} = V_{ENABLE} = 2.0 V	—	350	—	350	mV
		I_{OUT} = 500 mA, V_{IN} = V_{ENABLE} = 2.0 V	—	500	—	500	mV
		I_{OUT} = 750 mA, V_{IN} = V_{ENABLE} = 2.0 V	—	800	—	750	mV
		I_{OUT} = 1.0 A, V_{IN} = V_{ENABLE} = 2.0 V	—	1.1	—	1.0	V
		I_{OUT} = 1.25 A, V_{IN} = V_{ENABLE} = 2.0 V	—	1.4	—	—	V
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{ENABLE(1)}$	2.0	—	2.0	—	V
	Logic 0	$V_{IN(0)}$ or $V_{ENABLE(0)}$	—	0.8	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{ENABLE(1)}$ = 2.0 V	—	20	—	20	µA
	Logic 0	$V_{IN(0)}$ or $V_{ENABLE(0)}$ = 0.8 V	—	10	—	10	µA
Input Clamp Voltage	V_{IK}	I_{IN} or I_{ENABLE} = −10 mA	—	−1.5	—	−1.5	V
Total Supply Current	I_{CC}	I_{OUT} = 750 mA, V_{IN}* = V_{ENABLE} = 2.0 V	—	75	—	75	mA
		I_{OUT} = 1.25 A, V_{IN}* = V_{ENABLE} = 2.0 V	—	125	—	125	mA
		Outputs Open, V_{IN}* = V_{ENABLE} = 0.8 V	—	5.0	—	5.0	mA
Clamp Diode Forward Voltage†	V_F	I_F = 1.0 A	—	1.6	—	1.6	V
		I_F = 1.5 A	—	2.0	—	2.0	V
Clamp Diode Leakage Current†	I_R	V_R = 60 V, V_{IN} = V_{ENABLE} = 2.0 V, $D_1 + D_2$ or $D_3 + D_4$	—	50	—	—	µA
		V_R = 80 V, V_{IN} = V_{ENABLE} = 2.0 V, $D_1 + D_2$ or $D_3 + D_4$	—	—	—	50	µA

*All inputs simultaneously, all other tests are performed with each input tested separately.
†Test not applicable to SIP (suffix 'W') devices.

TYPICAL APPLICATION
UDN-2541B Driving A Stepper Motor

Input Waveforms

Dwg. No. A-11,795

Dwg. No. A-11,796
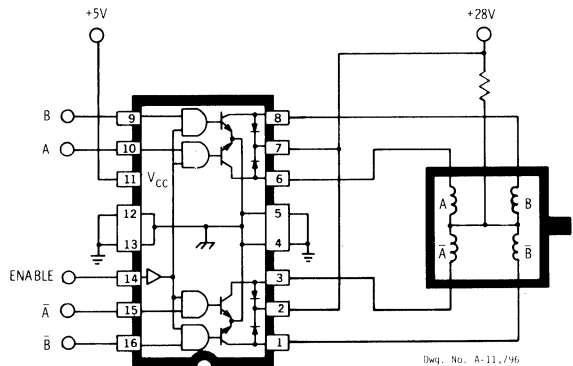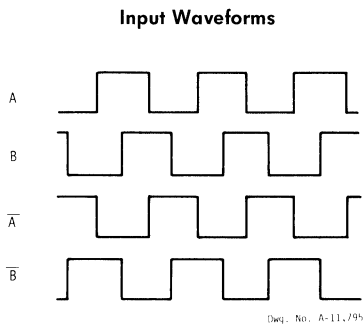
SERIES UDN-2580A
8-CHANNEL SOURCE DRIVERS

FEATURES

- TTL, CMOS, PMOS, NMOS Compatible
- High Output Current Ratings
- Internal Transient Suppression
- Efficient Input/Output Pin Structure

THIS versatile family of integrated circuits, originally designed to link NMOS logic with high-current inductive loads, will work with many combinations of logic- and load-voltage levels, meeting interface requirements beyond the capabilities of standard logic buffers.

Series UDN-2580A source drivers can drive incandescent, LED, or vacuum fluorescent displays. Internal transient-suppression diodes permit the drivers to be used with inductive loads.

Type UDN-2580A is a high-current source driver used to switch the ground ends of loads that are directly connected to a negative supply. Typical loads are telephone relays, PIN diodes, and LEDs.

Type UDN-2585A is a driver designed for applications requiring low output saturation voltages. Typical loads are low-voltage LEDs and incandescent displays. The eight non-Darlington outputs will simultaneously sustain continuous load currents of − 120 mA at ambient temperatures to + 70°C.

Type UDN-2588A, a high-current source driver similar to Type UDN-2580A, has separate logic and driver supply lines. Its eight drivers can serve as an interface between positive logic (TTL, CMOS, PMOS) or negative logic (NMOS) and either negative or split-load supplies.

Types UDN-2580A and UDN-2588A are rated for operation with output voltages of up to 50 V. Selected devices, carrying the suffix "-1" on the Sprague part number, have maximum ratings of 80 V.

Types UDN-2580A and UDN-2585A are furnished in 18-pin dual in-line plastic packages; Type UDN-2588A is supplied in a 20-pin dual in-line plastic package. All input connections are on one side of the packages, output pins on the other, to simplify printed wiring board layout.

DWG. NO. A-11,359
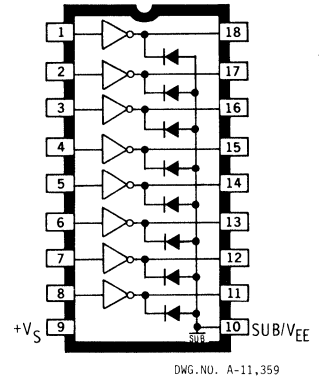
UDN-2580A
UDN-2585A

DWG. NO. A-11,357
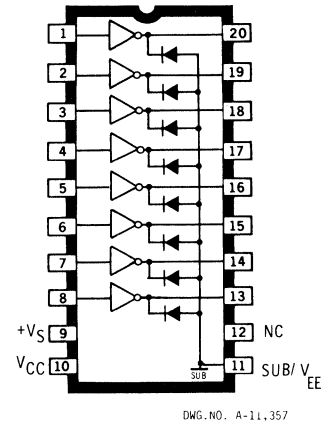
UDN-2588A

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature
for Any One Driver
(unless otherwise noted)

	UDN-2580A	UDN-2580A-1	UDN-2585A	UDN-2588A	UDN-2588A-1
Output Voltage, V_{CE}	50 V	80 V	25 V	50 V	80 V
Supply Voltage, V_S (ref. sub.)	50 V	80 V	25 V	50 V	80 V
Supply Voltage, V_{CC} (ref. sub.)	—	—	—	50 V	80 V
Input Voltage, V_{IN} (ref. V_S)	−30 V	−30 V	−20 V	−30 V	−30 V
Total Current, $I_{CC} + I_S$	−500 mA	−500 mA	−250 mA	−500 mA	−500 mA
Substrate Current, I_{SUB}	3.0 A	3.0 A	2.0 A	3.0 A	3.0 A

Allowable Power Dissipation, P_D (single output) . . . . 1.0 W
(total package) . . . . 2.2 W*
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −55°C to +150°C

*Derate at the rate of 18 mW/°C above 25°C

For simplification, these devices are characterized on the following pages with specific voltages for inputs, logic supply (V_S), load supply (V_{EE}), and collector supply (V_{CC}). Typical use of the UDN-2580A and UDN-2580A-1 is with negative referenced logic. The more common application of the UDN-2585A, UDN-2588A, and UDN-2588A-1 is with positive referenced logic supplies. In application, the devices are capable of operation over a wide range of logic and supply voltage levels:

TYPICAL OPERATING VOLTAGES

V_S	$V_{IN(ON)}$	$V_{IN(OFF)}$	V_{CC}	$V_{EE(MAX)}$	Device Type
0 V	−15 V to −3.6 V	−0.5 V to 0 V	NA	−25 V	UDN-2585A
				−50 V	UDN-2580A
				−80 V	UDN-2580A-1
+5 V	0 V to +1.4 V	+4.5 V to +5 V	NA	−20 V	UDN-2585A
				−45 V	UDN-2580A
				−75 V	UDN-2580A-1
			≤5 V	−45 V	UDN-2588A
				−75 V	UDN-2588A-1
+12 V	0 V to +8.4 V	+11.5 V to +12 V	NA	−13 V	UDN-2585A
				−38 V	UDN-2580A
				−68 V	UDN-2580A-1
			≤12 V	−38 V	UDN-2588A
				−68 V	UDN-2588A-1
+15 V	0 V to +11.4 V	+14.5 V to +15 V	NA	−10 V	UDN-2585A
				−35 V	UDN-2580A
				−65 V	UDN-2580A-1
			≤15 V	−35 V	UDN2588A
				−65 V	UDN-2588A-1

NOTE: The substrate must be tied to the most negative point in the external circuit to maintain isolation between drivers and to provide for normal circuit operation.

UDN-2580A
UDN-2580A-1

PARTIAL SCHEMATIC

DWG.NO. A-11,358

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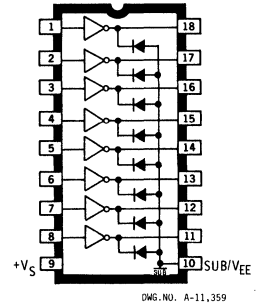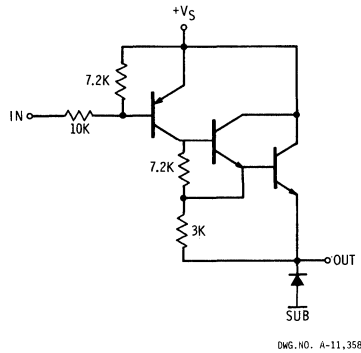
ELECTRICAL CHARACTERISTICS at $T_A = +25°C$,
$V_S = 0$ V, $V_{EE} = -45$ V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Min.	Max.	Units
Output Leakage Current	I_{CEX}	UDN-2580A	$V_{IN} = -0.5$ V, $V_{OUT} = V_{EE} = -50$ V	—	50	μA
			$V_{IN} = -0.4$ V, $V_{OUT} = V_{EE} = -50$ V, $T_A = 70°C$	—	100	μA
		UDN-2580A-1	$V_{IN} = -0.5$ V, $V_{OUT} = V_{EE} = -80$ V	—	50	μA
			$V_{IN} = -0.4$ V, $V_{OUT} = V_{EE} = -80$ V, $T_A = 70°C$	—	100	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	UDN-2580A	$V_{IN} = -0.4$ V, $I_{OUT} = -25$ mA, Note 1	35	—	V
		UDN-2580A-1	$V_{IN} = -0.4$ V, $V_{EE} = -75$ V, $I_{OUT} = -25$ mA, Note 1	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Both	$V_{IN} = -2.4$ V, $I_{OUT} = -100$ mA	—	1.8	V
			$V_{IN} = -3.0$ V, $I_{OUT} = -225$ mA	—	1.9	V
			$V_{IN} = -3.6$ V, $I_{OUT} = -350$ mA	—	2.0	V
Input Current	$I_{IN(ON)}$	Both	$V_{IN} = -3.6$ V, $I_{OUT} = -350$ mA	—	-500	μA
			$V_{IN} = -15$ V, $I_{OUT} = -350$ mA	—	-2.1	mA
	$I_{IN(OFF)}$	Both	$I_{OUT} = -500$ μA, $T_A = 70°C$, Note 3	-50	—	μA
Input Voltage	$V_{IN(ON)}$	Both	$I_{OUT} = -100$ mA, $V_{CE} \leq 1.8$ V, Note 4	—	-2.4	V
			$I_{OUT} = -225$ mA, $V_{CE} \leq 1.9$ V, Note 4	—	-3.0	V
			$I_{OUT} = -350$ mA, $V_{CE} \leq 2.0$ V, Note 4	—	-3.6	V
	$V_{IN(OFF)}$	Both	$I_{OUT} = -500$ μA, $T_A = 70°C$	-0.2	—	V
Clamp Diode Leakage Current	I_R	UDN-2580A	$V_R = 50$ V, $T_A = 70°C$	—	50	μA
		UDN-2580A-1	$V_R = 80$ V, $T_A = 70°C$	—	50	μA
Clamp Diode Forward Voltage	V_F	Both	$I_F = 350$ mA	—	2.0	V
Input Capacitance	C_{IN}	Both		—	25	pF
Turn-On Delay	t_{PHL}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs
Turn-Off Delay	t_{PLH}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs

NOTES: 1. Pulsed test, $t_p \leq 300$ μs, duty cycle $\leq 2\%$.
    2. Negative current is defined as coming out of the specified device pin.
    3. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
    4. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
    5. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.

UDN-2585A

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$,
$V_S = 0$ V, $V_{EE} = -20$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Max.	Units
			Limits		
Output Leakage Current	I_{CEX}	$V_{IN} = -0.5$ V, $V_{OUT} = V_{EE} = -25$ V	—	50	μA
		$V_{IN} = -0.4$ V, $V_{OUT} = V_{EE} = -25$ V, $T_A = 70°C$	—	100	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	$V_{IN} = -0.4$ V, $I_{OUT} = -25$ mA, Note 1	15	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	$V_{IN} = -4.6$ V, $I_{OUT} = -60$ mA	—	1.1	V
		$V_{IN} = -4.6$ V, $I_{OUT} = -120$ mA	—	1.2	V
Input Current	$I_{IN(ON)}$	$V_{IN} = -4.6$ V, $I_{OUT} = -120$ mA	—	−1.6	mA
		$V_{IN} = -14.6$ V, $I_{OUT} = -120$ mA	—	−5.0	mA
Input Voltage	$V_{IN(ON)}$	$I_{OUT} = -120$ mA, $V_{CE} \leq 1.2$ V, Note 3	—	−4.6	V
	$V_{IN(OFF)}$	$I_{OUT} = -100$ μA, $T_A = 70°C$	−0.4	—	V
Clamp Diode Leakage Current	I_R	$V_R = 25$ V, $T_A = 70°C$	—	50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 120$ mA	—	2.0	V
Input Capacitance	C_{IN}		—	25	pF
Turn-On Delay	t_{PHL}	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs
Turn-Off Delay	t_{PLH}	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs

NOTES: 1. Pulsed test, $t_p \leq 300$ μs, duty cycle $\leq 2\%$.
      2. Negative current is defined as coming out of the specified device pin.
      3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
      4. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.

3
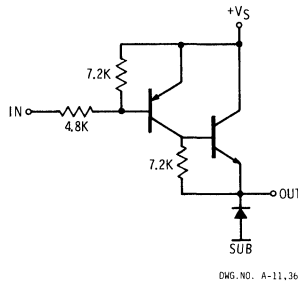
PARTIAL SCHEMATIC

DWG.NO. A-11,360
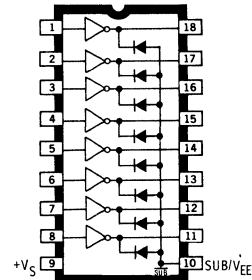
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UDN-2588A
UDN-2588A-1

PARTIAL SCHEMATIC
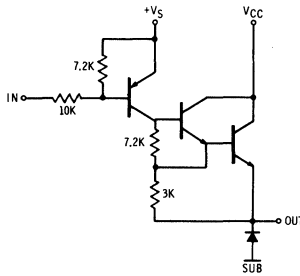
DWG.NO. A-11,361
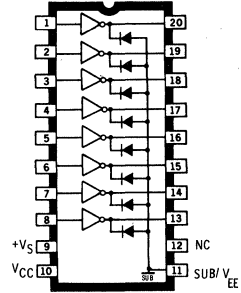
DWG.NO. A-11,357

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_S = 5.0$ V, $V_{CC} = 5.0$ V, $V_{EE} = -40$ V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Min.	Max.	Units
Output Leakage Current	I_{CEX}	UDN-2588A	$V_{IN} \geq 4.5$ V, $V_{OUT} = V_{EE} = -45$ V	—	50	μA
			$V_{IN} \geq 4.6$ V, $V_{OUT} = V_{EE} = -45$ V, $T_A = 70°C$	—	100	μA
		UDN-2588A-1	$V_{IN} \geq 4.5$ V, $V_{OUT} = V_{EE} = -75$ V	—	50	μA
			$V_{IN} \geq 4.6$ V, $V_{OUT} = V_{EE} = -75$ V, $T_A = 70°C$	—	100	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	UDN-2588A	$V_{IN} \geq 4.6$ V, $I_{OUT} = -25$ mA, Note 1	35	—	V
		UDN-2588A-1	$V_{IN} \geq 4.6$ V, $V_{EE} = -70$ V, $I_{OUT} = -25$ mA, Note 1	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	Both	$V_{IN} = 2.6$ V, $I_{OUT} = -100$ mA, Ref. V_{CC}	—	1.8	V
			$V_{IN} = 2.0$ V, $I_{OUT} = -225$ mA, Ref. V_{CC}	—	1.9	V
			$V_{IN} = 1.4$ V, $I_{OUT} = -350$ mA, Ref. V_{CC}	—	2.0	V
Input Current	$I_{IN(ON)}$	Both	$V_{IN} = 1.4$ V, $I_{OUT} = -350$ mA	—	-500	μA
			$V_S = 15$ V, $V_{EE} = -30$ V, $V_{IN} = 0$ V, $I_{OUT} = -350$ mA	—	-2.1	mA
	$I_{IN(OFF)}$	Both	$I_{OUT} = -500$ A, $T_A = 70°C$, Note 3	-50	—	μA
Input Voltage	$V_{IN(ON)}$	Both	$I_{OUT} = -100$ mA, $V_{CE} \leq 1.8$ V, Note 4	—	2.6	V
			$I_{OUT} = -225$ mA, $V_{CE} \leq 1.9$ V, Note 4	—	2.0	V
			$I_{OUT} = -350$ mA, $V_{CE} \leq 2.0$ V, Note 4	—	1.4	V
	$V_{IN(OFF)}$	Both	$I_{OUT} = -500$ μA, $T_A = 70°C$	4.8	—	V
Clamp Diode Leakage Current	I_R	UDN-2588A	$V_R = 50$ V, $T_A = 70°C$	—	50	μA
		UDN-2588A-1	$V_R = 80$ V, $T_A = 70°C$	—	50	μA
Clamp Diode Forward Voltage	V_F	Both	$I_F = 350$ mA	—	2.0	V
Input Capacitance	C_{IN}	Both		—	25	pF
Turn-On Delay	t_{PHL}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs
Turn-Off Delay	t_{PLH}	Both	0.5 E_{IN} to 0.5 E_{OUT}	—	5.0	μs

NOTES: 1. Pulsed test, $t_p \leq 300$ μs, duty cycle $\leq 2\%$.
      2. Negative current is defined as coming out of the specified device pin.
      3. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
      4. The $V_{IN(ON)}$ voltage limit guarantees a minimum output source current per the specified conditions.
      5. The substrate must always be tied to the most negative point and must be at least 4.0 V below V_S.
      6. V_{CC} must never be more positive than V_S.

ALLOWABLE PEAK COLLECTOR CURRENT AT 50°C AS A FUNCTION OF DUTY CYCLE

Dwg. No. A-11,107B
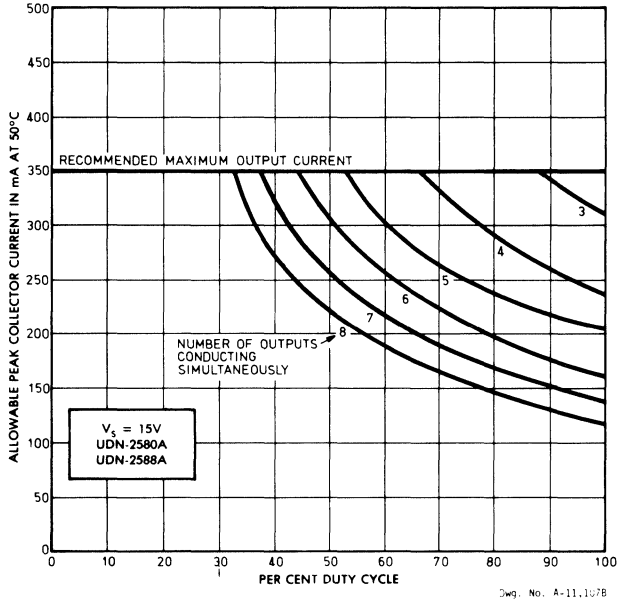
ALLOWABLE PEAK COLLECTOR CURRENT AT 70°C AS A FUNCTION OF DUTY CYCLE

Dwg. No. A-11,108B
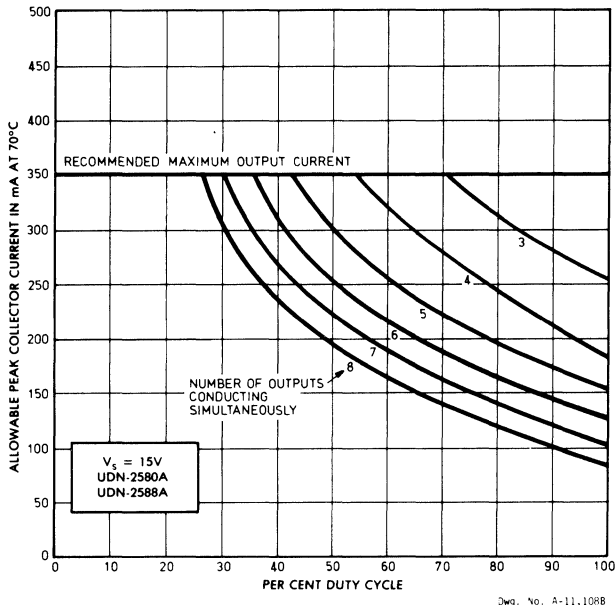
TYPICAL APPLICATIONS
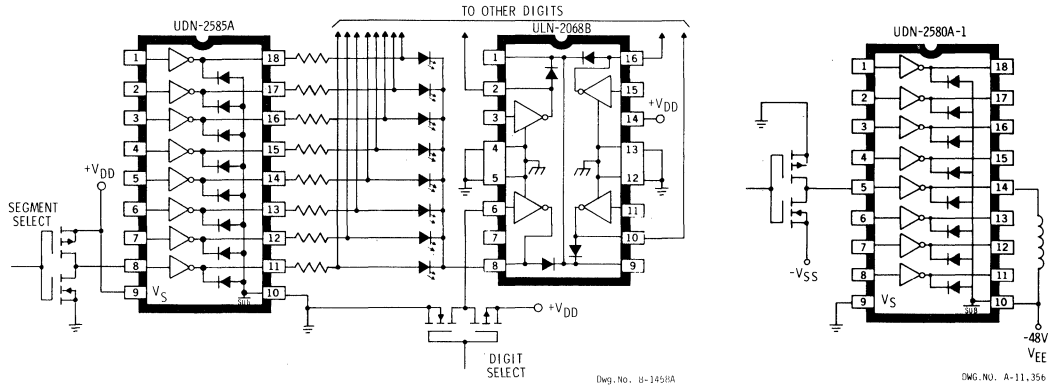
COMMON-CATHODE LED DRIVER

**TELECOMMUNICATIONS
RELAY DRIVER
(Negative Logic)**
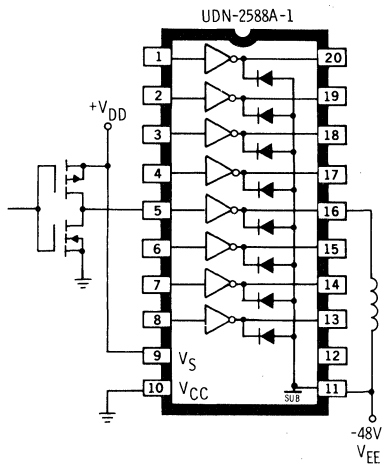
**TELECOMMUNICATIONS RELAY DRIVER
(Positive Logic)**
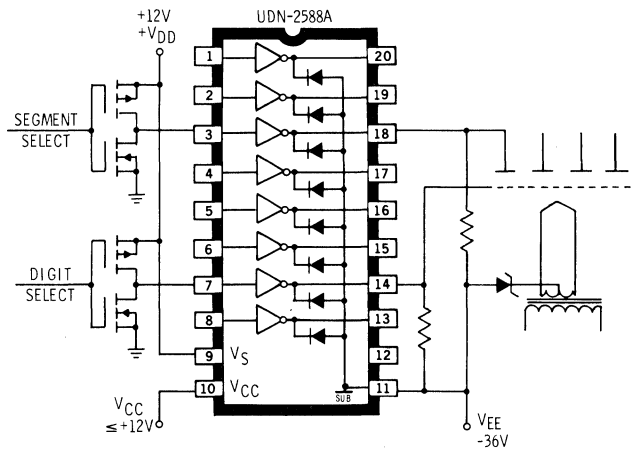
**VACUUM FLUORESCENT DISPLAY DRIVER
(Split Supply)**

UDN-2595A
8-CHANNEL CURRENT-SINK DRIVER

FEATURES
- 200 mA Current Rating
- Low Saturation Voltage
- TTL, CMOS, NMOS Compatible
- Efficient Input/Output Pin Format
- 18-Pin Dual In-Line Plastic Package

3

Dwg. No. A-11,407

DEVELOPED for use with low-voltage LED and incandescent displays requiring low output saturation voltage, Type UDN-2595A meets many other interface needs, including those exceeding the capabilities of standard logic buffers.

The eight non-Darlington outputs of this driver can simultaneously sink load currents of 200 mA at ambient temperatures of up to +85°C.

The eight-channel driver's active low inputs can be linked directly to TTL, Schottky TTL, DTL, 5 to 16 V CMOS, and NMOS logic. All input connections are on one side of the package, output connections on the other, for simplified layout of printed wiring boards.

Type UDN-2595A is supplied in an 18-pin dual-in-line plastic package with a copper lead frame that maximizes the driver's power-handling capabilities. A hermetically sealed version of Type UDN-2595A, with reduced package power dissipation ratings, is available on special order.

This device complements Sprague Type UDN-2585A, an eight-channel source driver.
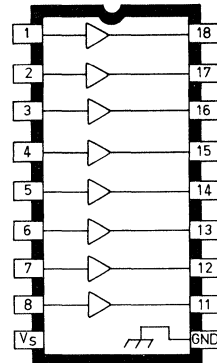
ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature
for any one driver
(unless otherwise noted)

Output Voltage, V_{CE} .... 20 V
Supply Voltage, V_S .... 20 V
Input Voltage, V_{IN} .... 20 V
Output Collector Current, I_C .... 200 mA
Ground Terminal Current, I_{GND} .... 1.6 A
Allowable Power Dissipation, P_D
    (single output) .... 1.0 W
    (total package) .... 2.2 W*
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −55°C to +150°C

*Derate at the rate of 18 mW/°C above +25°C.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_S = 5.0$ V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	$V_{IN} \geq 4.5$ V, $V_{OUT} = 20$ V, $T_A = 25°C$	—	50	μA
		$V_{IN} \geq 4.6$ V, $V_{OUT} = 20$ V, $T_A = 70°C$	—	100	μA
Output Saturation Voltage	$V_{CE(SAT)}$	$V_{IN} = 0.4$ V, $I_{OUT} = 50$ mA	—	0.5	V
		$V_{IN} = 0.4$ V, $I_{OUT} = 100$ mA	—	0.6	V
Input Current	$I_{IN(ON)}$	$V_{IN} = 0.4$ V, $I_{OUT} = 100$ mA	—	-1.6	mA
		$V_{IN} = 0.4$ V, $I_{OUT} = 100$ mA, $V_S = 15$ V	—	-5.0	mA
Input Voltage	$V_{IN(ON)}$	$I_{OUT} = 100$ mA, $V_{OUT} \leq 0.6$ V, $V_S = 5$ V	—	0.4	V
	$V_{IN(OFF)}$	$I_{OUT} = 100 \mu A$, $T_A = 70°C$	4.6	—	V
Input Capacitance	C_{IN}		—	25	pF
Supply Current	I_{SS}	$V_{IN} = 0.4$ V, $I_{OUT} = 100$ mA	—	6.0	mA
		$V_{IN} = 0.4$ V, $I_{OUT} = 100$ mA, $V_S = 15$ V	—	20	mA

NOTES:
1. Negative current is defined as coming out of the specified device pin.
2. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified conditions.
3. I_{SS} is measured with any one of eight drivers turned ON.

**UDN-2595A
ONE OF EIGHT DRIVERS**

Dwg. No. A-11,408
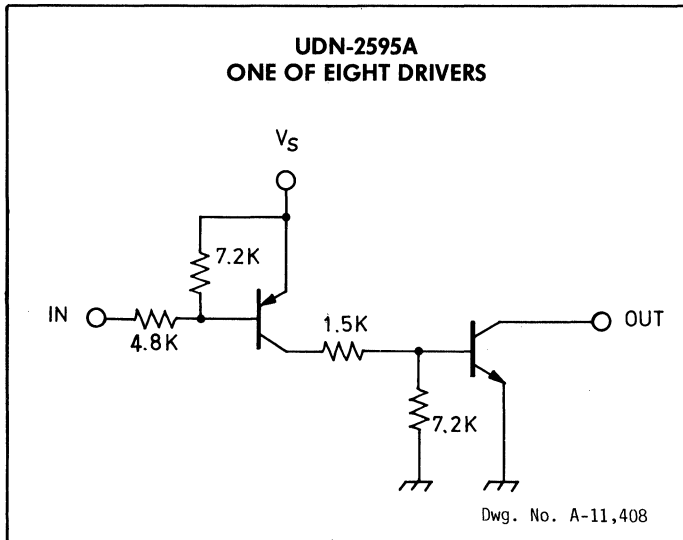
SERIES ULN-2800A
HIGH-VOLTAGE, HIGH-CURRENT
DARLINGTON TRANSISTOR ARRAYS

IDEALLY SUITED for interfacing between low-level digital logic circuitry and high-power peripheral loads, the Series ULN-2800A high-voltage, high-current Darlington transistor arrays feature peak load current ratings of 600 mA (Series ULN-2800A and ULN-2820A) or 750 mA (Series ULN-2810A) for each of the eight drivers in each device. Under the proper conditions, high-power loads of up to 4 A at 50V (200 W at 23% duty cycle) or 3.2 A at 95 V (304 W at 33% duty cycle) can be controlled. Typical loads include relays, solenoids, stepping motors, multiplexed LED and incandescent displays, and heaters. All devices feature open collector outputs and integral diodes for inductive load transient suppression.

The Series ULN-2801A devices are general purpose arrays which may be used with standard bipolar digital logic using external current limiting, or with most PMOS or CMOS directly. All are pinned with outputs opposite inputs to facilitate ease of circuit board layout and are priced to compete directly with discrete transistor alternatives.

The Series ULN-2802A was specifically designed for use with 14 to 25 V PMOS devices. Each input has a Zener diode and resistor in series to limit the input current to a safe value in that application. The Zener diode also means excellent noise immunity for these devices.

The Series ULN-2803A has a 2.7 kΩ series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5 V. These devices will handle numerous interface needs – particularly those beyond the capabilities of standard logic buffers.

The Series ULN-2804A features a 10.5 kΩ series input resistor to permit their operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15 V. The required input current is below that of the Series ULN-2803A while the required input voltage is less than that required by the Series ULN-2802A.

The Series ULN-2805A is especially designed for use with standard and Schottky TTL where higher output currents are required and loading of the logic
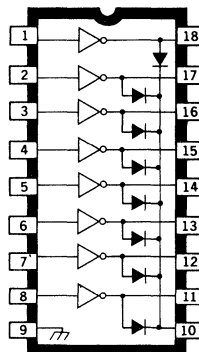
DWG. NO. A-10.322

output is not a concern. These devices will sink a minimum of 350 mA when driven from a "totem pole" logic output.

The Series ULN-2800A is the standard high-voltage, high-current Darlington array. The output transistors are capable of sinking 500mA and will withstand at least 50 V in the OFF state. Outputs may be paralleled for higher load current capability. The Series ULN-2810A devices are similar except that they will sink 600mA. The Series ULN-2820A will withstand 95 V in the OFF state.

All Series ULN-2800A Darlington arrays are furnished in an 18-pin dual in-line plastic package.

Device Type Number Designation

$V_{CE(MAX)} =$ $I_{C(MAX)} =$	50 V 500 mA	50 V 600 mA	95 V 500 mA
	Type Number		
General Purpose PMOS, CMOS	ULN-2801A	ULN-2811A	ULN-2821A
14 - 25 V PMOS	ULN-2802A	ULN-2812A	ULN-2822A
5 V TTL, CMOS	ULN-2803A	ULN-2813A	ULN-2823A
6 - 15 V CMOS, PMOS	ULN-2804A	ULN-2814A	ULN-2824A
High Output TTL	ULN-2805A	ULN-2815A	ULN-2825A

ABSOLUTE MAXIMUM RATINGS at 25°C Free-Air Temperature
for any one Darlington pair (unless otherwise noted)

Output Voltage, V_{CE} (Series ULN-2800, 2810A)..50 V

(Series ULN-2820A)..95 V

Input Voltage, V_{IN} (Series ULN-2802, 2803, 2804A)..30 V

(Series ULN-2805A)..15 V

Continuous Collector Current, I_C (Series ULN-2800, 2820A)..500 mA

(Series ULN-2810A)..600 mA

Continuous Base Current, I_B..25 mA

Power Dissipation, P_D (one Darlington pair)..1.0 W

(total package)..2.25 W*

Operating Ambient Temperature Range, T_A..−20°C to +85°C

Storage Temperature Range, T_S..−55°C to +150°C

*Derate at the rate of 18.18mW/°C above 25°C.

Under normal operating conditions, these devices will sustain 350 mA per output with $V_{CE(SAT)} = 1.6$ V at 50°C with a pulse width of 20 ms and a duty cycle of 40%.

PARTIAL SCHEMATICS
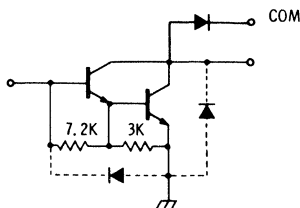
DWG. NO. A-9595

Series ULN-2801A
(each driver)
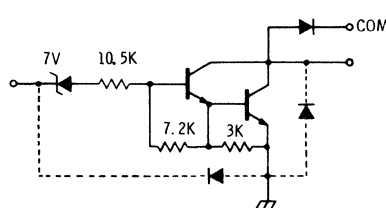
DWG. No. A-9650

Series ULN-2802A
(each driver)
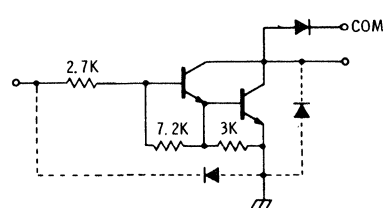
DWG. No. A-9651

Series ULN-2803A
(each driver)
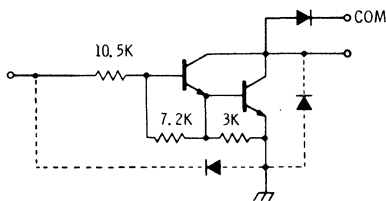
DWG. NO. A-9898A

Series ULN-2804A
(each driver)
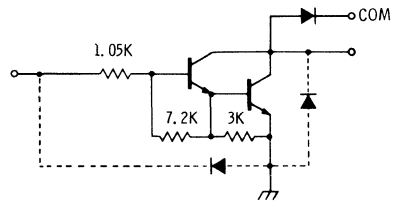
DWG. NO. A-10.228

Series ULN-2805A
(each driver)

SERIES ULN-2800A

ELECTRICAL CHARACTERISTICS at 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			Units
					Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	1A	All	$V_{CE} = 50\,V$, $T_A = 25°C$	—	—	50	μA
				$V_{CE} = 50\,V$, $T_A = 70°C$	—	—	100	μA
		1B	ULN-2802A	$V_{CE} = 50\,V$, $T_A = 70°C$, $V_{IN} = 6.0\,V$	—	—	500	μA
			ULN-2804A	$V_{CE} = 50\,V$, $T_A = 70°C$, $V_{IN} = 1.0\,V$	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2		$I_C = 100\,mA$, $I_B = 250\,\mu A$	—	0.9	1.1	V
			All	$I_C = 200\,mA$, $I_B = 350\,\mu A$	—	1.1	1.3	V
				$I_C = 350\,mA$, $I_B = 500\,\mu A$	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2802A	$V_{IN} = 17\,V$	—	0.82	1.25	mA
			ULN-2803A	$V_{IN} = 3.85\,V$	—	0.93	1.35	mA
			ULN-2804A	$V_{IN} = 5.0\,V$	—	0.35	0.5	mA
				$V_{IN} = 12\,V$	—	1.0	1.45	mA
			ULN-2805A	$V_{IN} = 3.0\,V$	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	$I_C = 500\,\mu A$, $T_A = 70°C$	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2802A	$V_{CE} = 2.0\,V$, $I_C = 300\,mA$	—	—	13	V
				$V_{CE} = 2.0\,V$, $I_C = 200\,mA$	—	—	2.4	V
			ULN-2803A	$V_{CE} = 2.0\,V$, $I_C = 250\,mA$	—	—	2.7	V
				$V_{CE} = 2.0\,V$, $I_C = 300\,mA$	—	—	3.0	V
				$V_{CE} = 2.0\,V$, $I_C = 125\,mA$	—	—	5.0	V
			ULN-2804A	$V_{CE} = 2.0\,V$, $I_C = 200\,mA$	—	—	6.0	V
				$V_{CE} = 2.0\,V$, $I_C = 275\,mA$	—	—	7.0	V
				$V_{CE} = 2.0\,V$, $I_C = 350\,mA$	—	—	8.0	V
			ULN-2805A	$V_{CE} = 2.0\,V$, $I_C = 350\,mA$	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2801A	$V_{CE} = 2.0\,V$, $I_C = 350\,mA$	1000	—	—	
Input Capacitance	C_{IN}	–	All		—	15	25	pF
Turn-On Delay	t_{ON}	–	All	$0.5\,E_{in}$ to $0.5\,E_{out}$	—	0.25	1.0	μS
Turn-Off Delay	t_{OFF}	–	All	$0.5\,E_{in}$ to $0.5\,E_{out}$	—	0.25	1.0	μS
Clamp Diode Leakage Current	I_R	6	All	$V_R = 50\,V$, $T_A = 25°C$	—	—	50	μA
				$V_R = 50\,V$, $T_A = 70°C$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	$I_F = 350\,mA$	—	1.7	2.0	V

Series ULN-2800A and ULN-2810A devices are also available (with reduced package power capability) in industrial-grade hermetic packages. To order, change the last letter of the part number from 'A' to 'R'. Note that the high-voltage devices ($BV_{CE} \geq 95\,V$) are not presently available with this packaging option.

SERIES ULN-2810A

ELECTRICAL CHARACTERISTICS at 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			Units
					Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	1A	All	$V_{CE} = 50\,V$, $T_A = 25°C$	—	—	50	μA
				$V_{CE} = 50\,V$, $T_A = 70°C$	—	—	100	μA
		1B	ULN-2812A	$V_{CE} = 50\,V$, $T_A = 70°C$, $V_{IN} = 6.0\,V$	—	—	500	μA
			ULN-2814A	$V_{CE} = 50\,V$, $T_A = 70°C$, $V_{IN} = 1.0\,V$	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	$I_C = 200\,mA$, $I_B = 350\,\mu A$	—	1.1	1.3	V
				$I_C = 350\,mA$, $I_B = 500\,\mu A$	—	1.3	1.6	V
				$I_C = 500\,mA$, $I_B = 600\,\mu A$	—	1.7	1.9	V
Input Current	$I_{IN(ON)}$	3	ULN-2812A	$V_{IN} = 17\,V$	—	0.82	1.25	mA
			ULN-2813A	$V_{IN} = 3.85\,V$	—	0.93	1.35	mA
			ULN-2814A	$V_{IN} = 5.0\,V$	—	0.35	0.5	mA
				$V_{IN} = 12\,V$	—	1.0	1.45	mA
			ULN-2815A	$V_{IN} = 3.0\,V$	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	$I_C = 500\,\mu A$, $T_A = 70°C$	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2812A	$V_{CE} = 2.0\,V$, $I_C = 500\,mA$	—	—	17	V
			ULN-2813A	$V_{CE} = 2.0\,V$, $I_C = 250\,mA$	—	—	2.7	V
				$V_{CE} = 2.0\,V$, $I_C = 300\,mA$	—	—	3.0	V
				$V_{CE} = 2.0\,V$, $I_C = 500\,mA$	—	—	3.5	V
			ULN-2814A	$V_{CE} = 2.0\,V$, $I_C = 275\,mA$	—	—	7.0	V
				$V_{CE} = 2.0\,V$, $I_C = 350\,mA$	—	—	8.0	V
				$V_{CE} = 2.0\,V$, $I_C = 500\,mA$	—	—	9.5	V
			ULN-2815A	$V_{CE} = 2.0\,V$, $I_C = 500\,mA$	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2811A	$V_{CE} = 2.0\,V$, $I_C = 350\,mA$	1000	—	—	
				$V_{CE} = 2.0\,V$, $I_C = 500\,mA$	900	—	—	
Input Capacitance	C_{IN}	–	All		—	15	25	pF
Turn-On Delay	t_{ON}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μS
Turn-Off Delay	t_{OFF}	–	All	0.5 E_{in} to 0.5 E_{out}	—	0.25	1.0	μS
Clamp Diode Leakage Current	I_R	6	All	$V_R = 50\,V$, $T_A = 25°C$	—	—	50	μA
				$V_R = 50\,V$, $T_A = 70°C$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	$I_F = 350\,mA$	—	1.7	2.0	V
				$I_F = 500\,mA$	—	2.1	2.5	V

Series ULN-2800A and ULN-2810A devices are also available (with reduced package power capability) in industrial-grade hermetic packages. To order, change the last letter of the part number from 'A' to 'R'. Note that the high-voltage devices ($BV_{CE} \geqq 95$ V) are not presently available with this packaging option.

SERIES ULN-2820A

ELECTRICAL CHARACTERISTICS at 25°C (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits			Units
					Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	1A	All	$V_{CE} = 95\text{ V}$, $T_A = 25°C$	—	—	50	μA
				$V_{CE} = 95\text{ V}$, $T_A = 70°C$	—	—	100	μA
		1B	ULN-2822A	$V_{CE} = 95\text{ V}$, $T_A = 70°C$, $V_{IN} = 6.0\text{ V}$	—	—	500	μA
			ULN-2824A	$V_{CE} = 95\text{ V}$, $T_A = 70°C$, $V_{IN} = 1.0\text{ V}$	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	$I_C = 100\text{ mA}$, $I_B = 250\,\mu A$	—	0.9	1.1	V
				$I_C = 200\text{ mA}$, $I_B = 350\,\mu A$	—	1.1	1.3	V
				$I_C = 350\text{ mA}$, $I_B = 500\,\mu A$	—	1.3	1.6	V
Input Current	$I_{IN(ON)}$	3	ULN-2822A	$V_{IN} = 17\text{ V}$	—	0.82	1.25	mA
			ULN-2823A	$V_{IN} = 3.85\text{ V}$	—	0.93	1.35	mA
			ULN-2824A	$V_{IN} = 5.0\text{ V}$	—	0.35	0.5	mA
				$V_{IN} = 12\text{ V}$	—	1.0	1.45	mA
			ULN-2825A	$V_{IN} = 3.0\text{ V}$	—	1.5	2.4	mA
	$I_{IN(OFF)}$	4	All	$I_C = 500\,\mu A$, $T_A = 70°C$	50	65	—	μA
Input Voltage	$V_{IN(ON)}$	5	ULN-2822A	$V_{CE} = 2.0\text{ V}$, $I_C = 300\text{ mA}$	—	—	13	V
			ULN-2823A	$V_{CE} = 2.0\text{ V}$, $I_C = 200\text{ mA}$	—	—	2.4	V
				$V_{CE} = 2.0\text{ V}$, $I_C = 250\text{ mA}$	—	—	2.7	V
				$V_{CE} = 2.0\text{ V}$, $I_C = 300\text{ mA}$	—	—	3.0	V
			ULN-2824A	$V_{CE} = 2.0\text{ V}$, $I_C = 125\text{ mA}$	—	—	5.0	V
				$V_{CE} = 2.0\text{ V}$, $I_C = 200\text{ mA}$	—	—	6.0	V
				$V_{CE} = 2.0\text{ V}$, $I_C = 275\text{ mA}$	—	—	7.0	V
				$V_{CE} = 2.0\text{ V}$, $I_C = 350\text{ mA}$	—	—	8.0	V
			ULN-2825A	$V_{CE} = 2.0\text{ V}$, $I_C = 350\text{ mA}$	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2	ULN-2821A	$V_{CE} = 2.0\text{ V}$, $I_C = 350\text{ mA}$	1000	—	—	
Input Capacitance	C_{IN}	—	All		—	15	25	pF
Turn-On Delay	t_{ON}	—	All	$0.5\ E_{in}$ to $0.5\ E_{out}$	—	0.25	1.0	μS
Turn-Off Delay	t_{OFF}	—	All	$0.5\ E_{in}$ to $0.5\ E_{out}$	—	0.25	1.0	μS
Clamp Diode Leakage Current	I_R	6	All	$V_R = 95\text{ V}$, $T_A = 25°C$	—	—	50	μA
				$V_R = 95\text{ V}$, $T_A = 70°C$	—	—	100	μA
Clamp Diode Forward Voltage	V_F	7	All	$I_F = 350\text{ mA}$	—	1.7	2.0	V

3

TEST FIGURES

FIGURE 1A

FIGURE 1B

FIGURE 2

FIGURE 3

FIGURE 4

FIGURE 5

FIGURE 6

FIGURE 7

COLLECTOR CURRENT
AS A FUNCTION OF SATURATION VOLTAGE
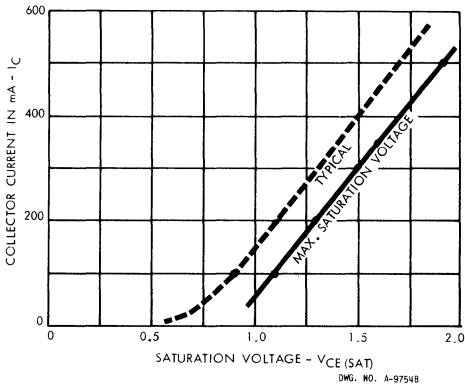
COLLECTOR CURRENT
AS A FUNCTION OF INPUT CURRENT
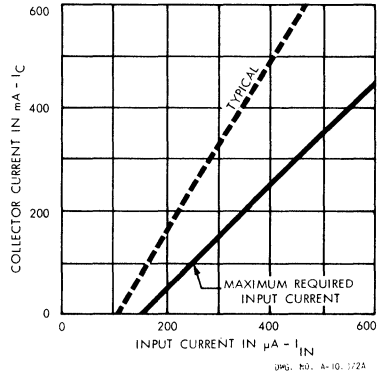
ALLOWABLE AVERAGE POWER DISSIPATION
AS A FUNCTION OF AMBIENT TEMPERATURE

PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE

Dwg. No. A-11,037

Dwg. No. A-10,380A

3—54
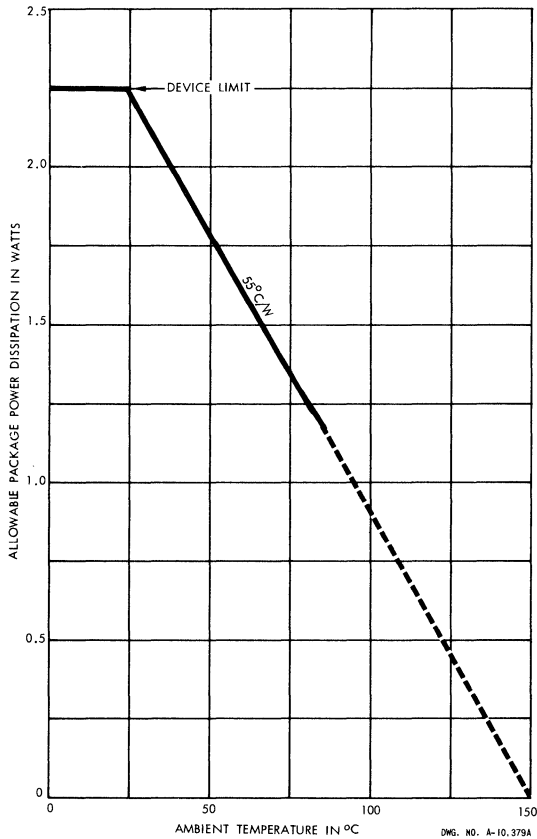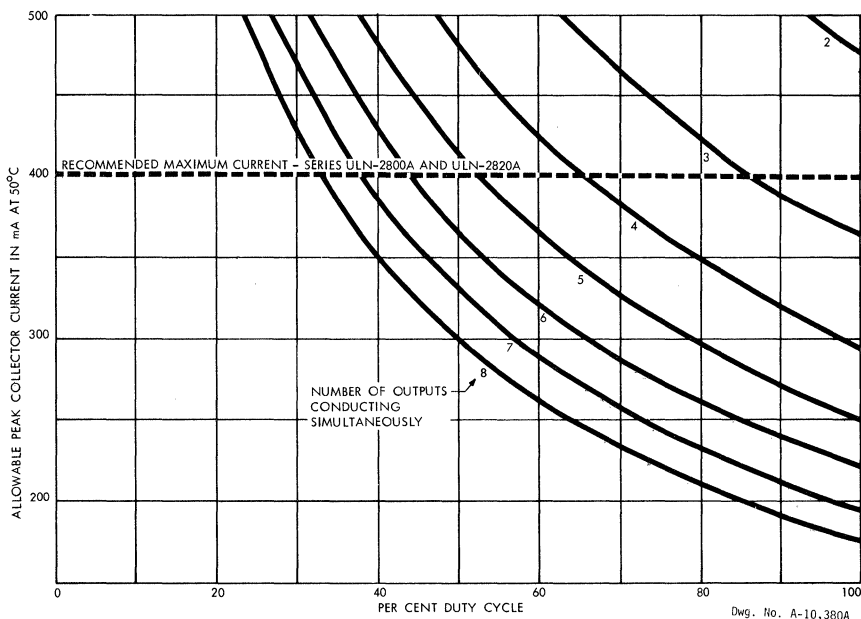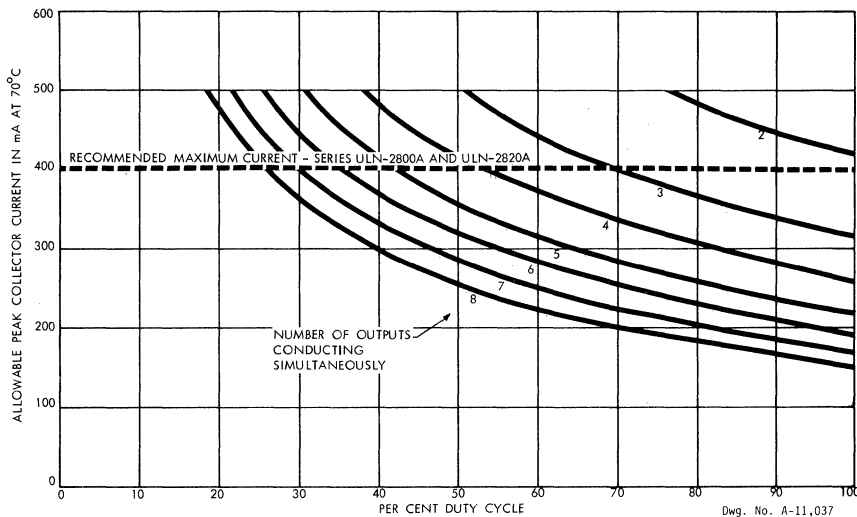
INPUT CURRENT
AS A FUNCTION OF INPUT VOLTAGE
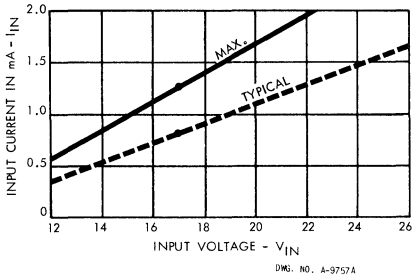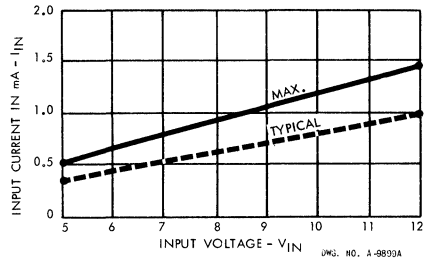
SERIES ULN-2802A

SERIES ULN-2804A
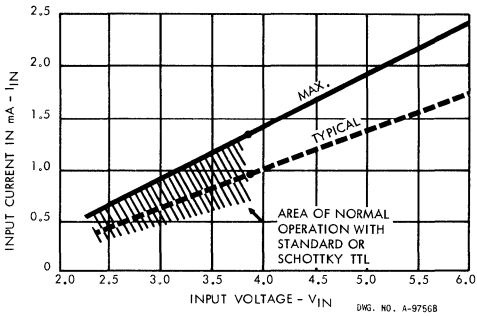
SERIES ULN-2803A
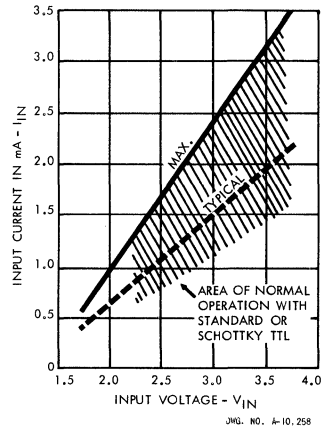
SERIES ULN-2805A

3

3—55
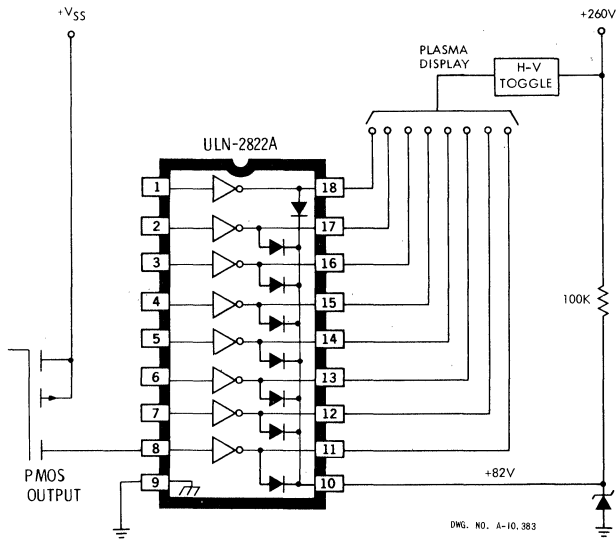
**OFF VOLTAGE BIAS FOR
HIGH-VOLTAGE LOADS**
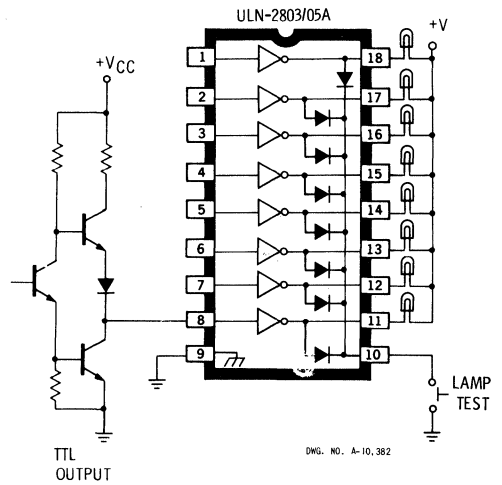
TTL TO LOAD
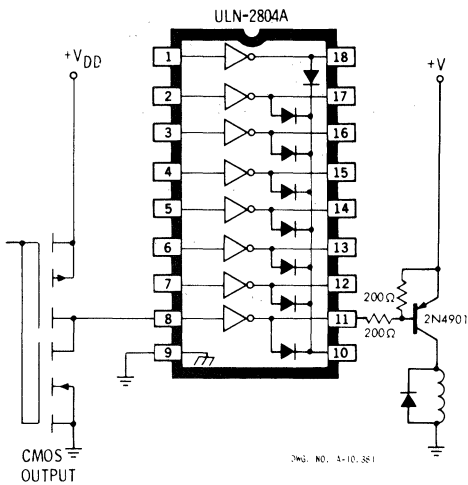
BUFFER FOR HIGHER CURRENT LOADS
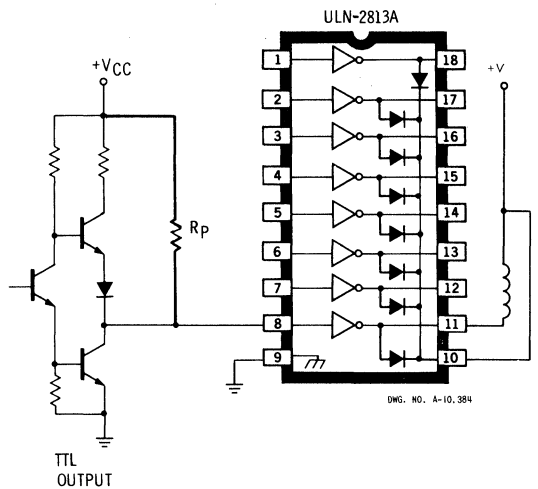
**USE OF PULL-UP RESISTORS
TO INCREASE DRIVE CURRENT**

TYPICAL DISPLAY INTERFACE

3

+V$_S$

DIGIT DRIVER,
1/2 ULN-2061M or
1/4 ULN-2074/76B or
1/8 UDN-2981/82A

7-SEGMENT DISPLAY
WITH DECIMAL POINT,
COMMON-ANODE LED or
HOT-WIRE READOUT

TO OTHER
DIGITS

SEGMENT DRIVER,
SERIES ULN-2800A or
SERIES ULN-2810A

DWG. NO. A-10,378
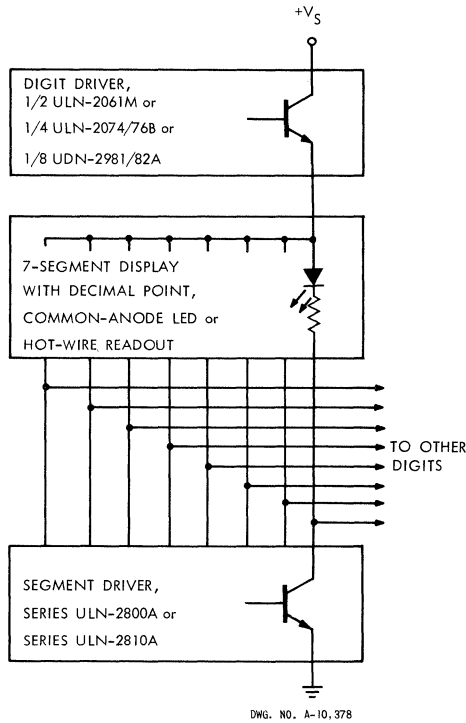
UDN-2841B AND UDN-2845B
QUAD DARLINGTON 1.5 A DRIVERS

FEATURES

- Inputs Compatible with DTL, TTL, LSTTL, CMOS
- −50 V Darlington Outputs
- Current-Sink or Sink-and-Source Combination
- 16-Pin Dual In-Line Plastic Package

THIS PAIR OF QUAD DARLINGTON switches is designed for high-current, high-voltage peripheral driver applications. They provide solutions to interface problems involving electronic discharge printers, d-c motor drive (bipolar or unipolar), telephone relays, PIN diodes, LEDs, and other high-current loads operating with negative voltage supplies.

Type UDN-2841B is for current-sink applications in which the load is connected to ground. The outputs switch the negative supply. The input PNP transistor in each driver serves as a level translator. The first NPN stage provides current gain to drive the Darlington-pair outputs.

Type UDN-2845B is a current-sink, current-source combination in a single dual in-line plastic package. It can be used in bipolar switching applications in which neither end of the load is at ground potential.

Types UDN-2841 and UDN-2845B are intended for use with 5 V TTL, Schottky TTL, DTL, and CMOS logic. Both drivers reduce component count, lower system costs, and reduce circuit and board complexity.

DWG. NO. A-10,323B

Current Sink

Dwg.No. A-10,489

Current Source
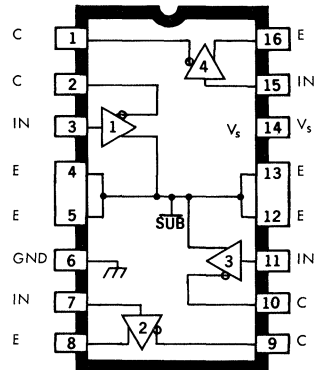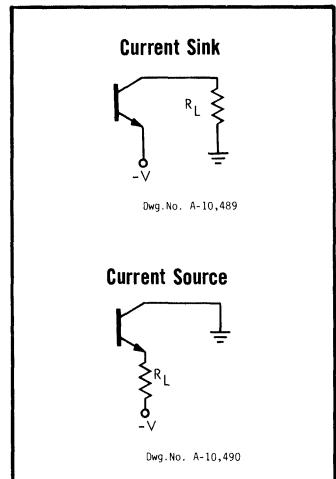
Dwg.No. A-10,490

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
For Single Darlington Output
(Unless Otherwise Noted)

Output Voltage, $V_{CE(OFF)}$ .... 50 V
Output Sustaining Voltage, $V_{CE(SUS)}$ .... 35 V
Substrate Voltage, V_{SUB} .... −50 V
Continuous Output Current, I_{OUT} .... 1.75 A
Supply Voltage, V_S .... 10 V
Input Voltage, V_{IN} .... 10 V
Power Dissipation, P_D (one output) .... See Graph
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −55°C to +150°C

3

SCHEMATIC
(Each Driver)

DWG. NO. A-10,483C

ALLOWABLE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE

DWG. NO. A-10,488C
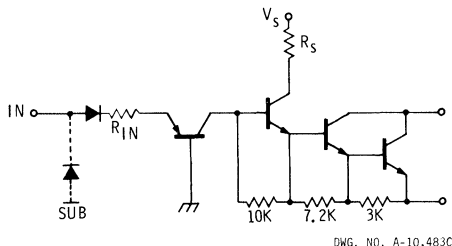
Type Number	Resistor Values in kΩ			
	Amplifier 1 & 3		Amplifier 2 & 4	
	R_{IN}	R_S	R_{IN}	R_S
UDN-2841B	3.3	15	3.3	15
UDN-2845B	3.3	15	3.3	1

NOTE: The substrate terminals must be tied to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal device operation.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{EE} = -50V$, $V_{IN} = 0.4V$, $T_A = 25°C$	—	—	100	μA
		$V_{EE} = -50V$, $V_{IN} = 0.4V$, $T_A = 70°C$	—	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	$V_{EE} = -50V$, $V_{IN} = 0.4V$, $I_{OUT} = 100$ mA	35	50	—	V
Output Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 500$ mA	—	—	1.1	V
		$I_{OUT} = 1.0A$ (Note 1)	—	—	1.4	V
		$I_{OUT} = 1.5A$ (Note 1)	—	—	1.6	V
Input Current	$I_{IN(ON)}$	$I_{OUT} = 500$ mA, $V_{IN} = 2.4V$	—	300	500	μA
Input Voltage (Note 1)	$V_{IN(ON)}$	$I_{OUT} = 1.5A$	—	—	2.4	V
Supply Current (Note 1)	I_S	$I_{OUT} = 500$ mA, UDN-2841B, UDN-2845B (Note 2)	—	2.5	3.75	mA
		$I_{OUT} = 500$ mA, UDN-2845B (Note 3)	—	3.3	7.5	mA
Turn-On Delay	$t_{pd(ON)}$	$R_L = 30Ω$, $0.5V_{IN}$ to $0.5V_{OUT}$	—	—	2.0	μs
Turn-Off Delay	$t_{pd(OFF)}$	$R_L = 39Ω$, $0.5V_{IN}$ to $0.5V_{OUT}$	—	—	5.0	μs

NOTES:
1. Each driver tested separately.
2. Drivers 1 & 3 (sink drivers) only, $V_S = 0V$, $V_{EE} = -40V$.
3. Drivers 2 & 4 (source drivers) only, $V_S = 5V$, $V_{EE} = -40V$.

TEST CIRCUITS
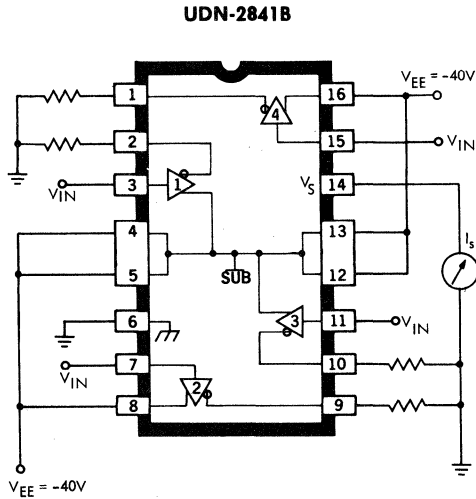
UDN-2841B

DWG. NO. A-10,487A
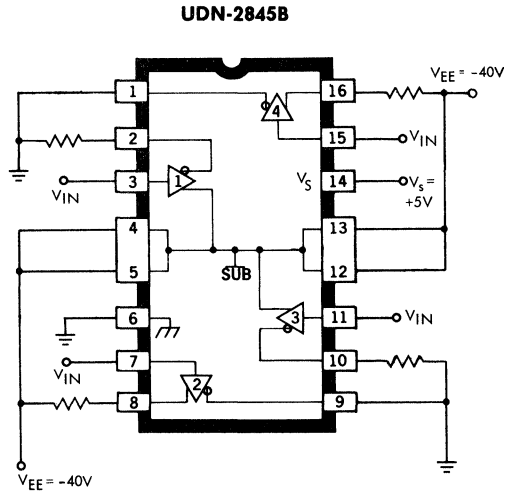
UDN-2845B

DWG. NO. A-10,484A

ALLOWABLE OUTPUT CURRENT
AS A FUNCTION OF DUTY CYCLE

WITHOUT HEAT SINK

DWG. NO. A-10,583

WITH STAVER V-7 HEAT SINK

DWG. NO. A-10,584
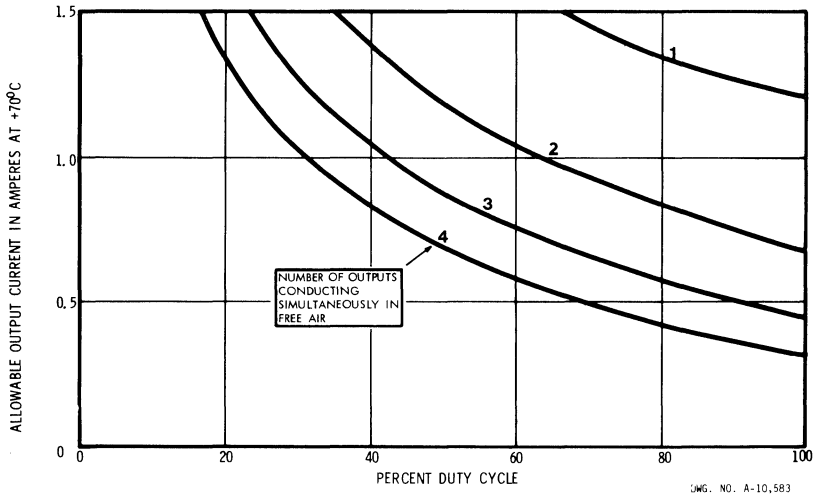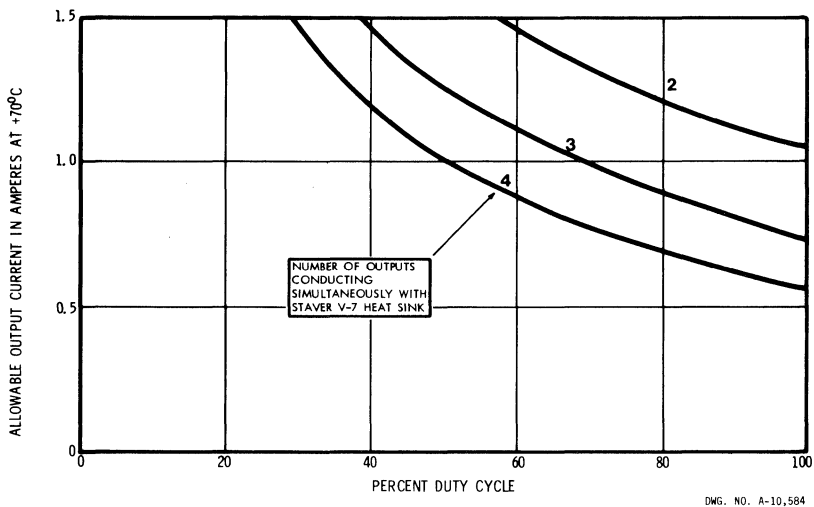
OUTPUT-STAGE TRANSIENT PROTECTION

When switching inductive loads, the output transistors of UDN-2841B and UDN-2845B drivers should be protected by a suitable clamping technique. The simplest approach is to clamp each output with a discrete diode, as shown in Figures 1 and 2.

DWG. NO. A-11,790A

Figure 1
UDN-2841B

DWG. NO. A-11,792A

Figure 2
UDN-2845B

DWG. NO. A-11,787A
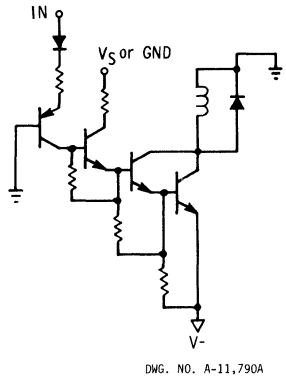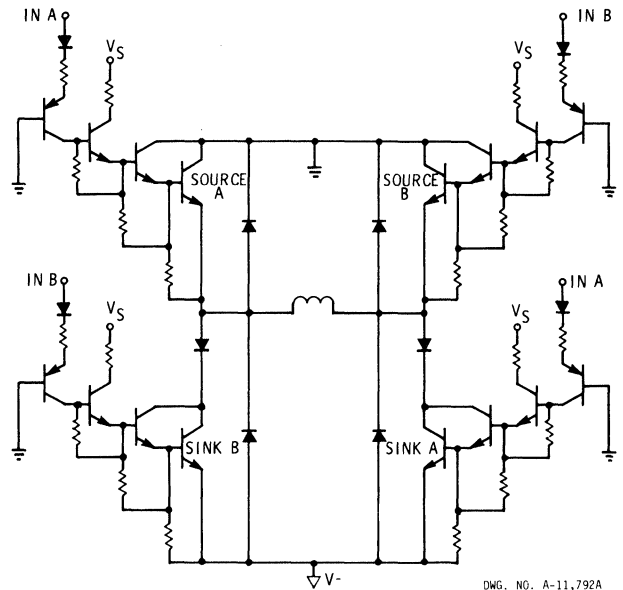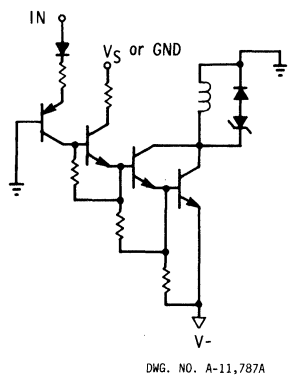
Figure 3
UDN-2841B

For improved turnoff, a combination diode/Zener diode scheme can be used. The Zener diode in the clamp circuit of Figure 3 allows the flyback voltage to rise above the supply voltage, speeding turnoff of the load. An appropriate resistor can be substituted for the Zener diode. With a 1A load, substitution of a 15Ω resistor results in operation similar to that of the Zener diode circuit.

TYPICAL APPLICATIONS

BIPOLAR MOTOR DRIVER

UDN-2845B
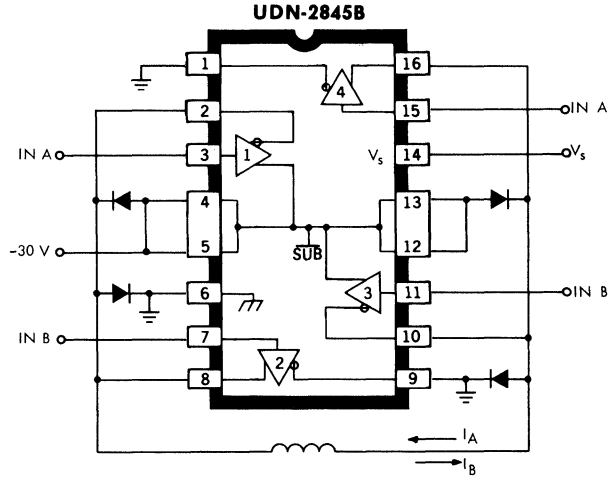
DWG. NO. A-10,586A

ELECTROSENSITIVE PRINTER INTERFACE
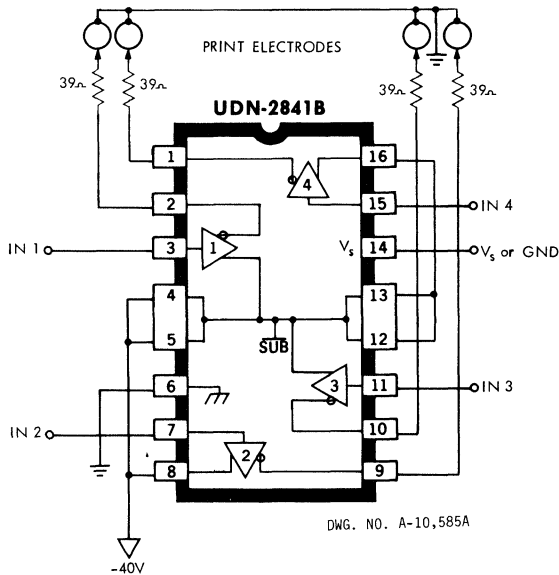
DWG. NO. A-10,585A

UDN-2878W AND UDN-2879W
QUAD HIGH-CURRENT DARLINGTON SWITCHES

FEATURES

- Output Currents to 4 A
- Output Voltages to 80 V
- Loads to 1280 W
- TTL, DTL, or CMOS Compatible Inputs
- Internal Clamp Diodes
- Plastic Single In-Line Package
- Heat-Sink Tab

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| B₁ | | C₁ | GND | C₂ | K₁₋₂ | B₂ | B₃ | V$_S$ | C₃ | K₃₋₄ | C₄ | B₄ |
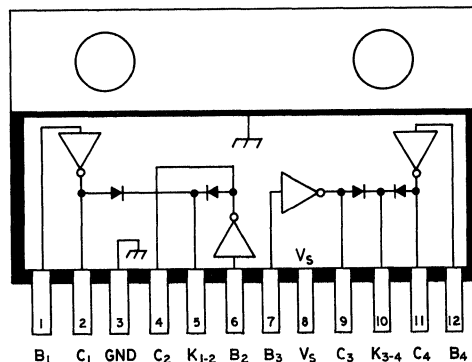
DWG. NO. A-11,974

THESE QUAD DARLINGTON ARRAYS are designed to serve as interface between low-level logic and peripheral power devices such as solenoids, motors, incandescent displays, heaters, and similar loads of up to 320 W per channel. Both integrated circuits include transient-suppression diodes that enable use with inductive loads. The input logic is compatible with most TTL, DTL, LS TTL, and 5 V CMOS logic.

Type UDN-2878W and UDN-2879W 4 A arrays are identical except for output-voltage ratings. The former is rated for operation to 50 V (35 V sustaining), while the latter has a minimum output breakdown rating of 80 V (50 V sustaining). The economical Type UDN-2878W-2 and Type UDN-2879W-2 are recommended for applications requiring load currents of 3 A or less. These less expensive devices are identical to the basic parts except for the maximum allowable load-current rating.

For maximum power-handling capability, all drivers are supplied in a 12-pin single in-line power-tab package. The tab is at ground potential and needs no insulation. External heat sinks are usually required for proper operation of these devices.

Device	Output Voltage	Sustaining Voltage	Output Current
UDN-2878W	50 V	35 V	4 A
UDN-2878W-2	50 V	35 V	3 A
UDN-2879W	80 V	50 V	4 A
UDN-2879W-2	80 V	50 V	3 A

ABSOLUTE MAXIMUM RATINGS
at + 25°C Free-Air Temperature
for any driver
(unless otherwise noted)

Output Voltage, V_{CEX} (UDN-2878W & UDN-2878W-2) . . . . 50 V
(UDN-2879W & UDN-2879W-2) . . . . 80 V
Output Current, I_C (UDN-2878W & UDN-2879W) . . . . 5.0 A
(UDN-2878W-2 & UDN-2979W-2) . . . . 4.0 A
Input Voltage, V_{IN} . . . . 15 V
Input Current, I_{IN} . . . . 25 mA
Supply Voltage, V_S . . . . 10 V
Total Package Power Dissipation, P_D . . . . See Graph
Operating Ambient Temperature Range, T_A . . . . − 20°C to + 85°C
Storage Temperature Range, T_S . . . . − 55°C to + 150°C

3

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE
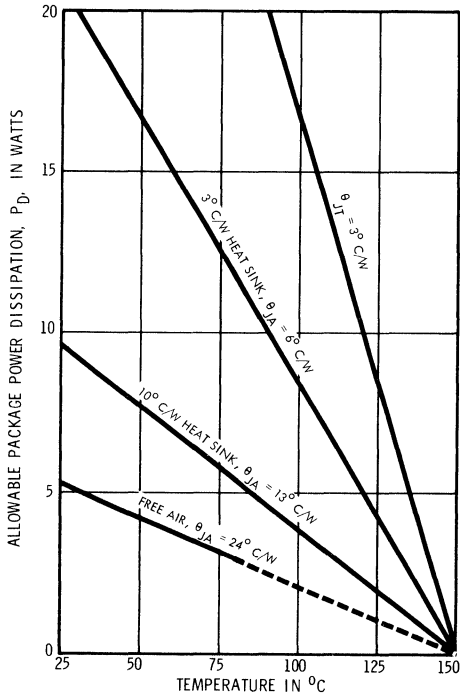
Dwg. No. A-11,794

PARTIAL SCHEMATIC
One of 4 Drivers

DWG. NO. A-12,037

ELECTRICAL CHARACTERISTICS at $V_S = 5.0$ V, $T_A = +25°C$ (unless otherwise noted)

Characteristic	Symbol	Test Fig.	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	1	UDN-2878W/W-2	$V_{CE} = 50$ V	—	100	μA
				$V_{CE} = 50$ V, $T_A = +70°C$	—	500	μA
			UDN-2879W/W-2	$V_{CE} = 80$ V	—	100	μA
				$V_{CE} = 80$ V, $T_A = +70°C$	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	2	UDN-2878W/W-2	$I_C = 100$ mA, $V_{IN} = 0.4$ V	35	—	V
			UDN-2879W/W-2	$I_C = 100$ mA, $V_{IN} = 0.4$ V	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	2	All	$I_C = 500$ mA, $V_{IN} = 2.75$ V	—	1.1	V
				$I_C = 1.0$ A, $V_{IN} = 2.75$ V	—	1.3	V
				$I_C = 2.0$ A, $V_{IN} = 2.75$ V	—	1.5	V
				$I_C = 3.0$ A, $V_{IN} = 2.75$ V	—	1.9	V
			UDN-2878/2879W	$I_C = 4.0$ A, $V_{IN} = 2.75$ V	—	2.2	V
Input Current	I_{IN}	3	All	$V_{IN} = 2.75$ V	—	550	μA
				$V_{IN} = 3.75$ V	—	1000	μA
Input Voltage	$V_{IN(ON)}$	4	All	$V_{CE} = 2.2$ V, $I_C = 3.0$ A	—	2.75	V
			UDN-2878/2879W	$V_{CE} = 2.2$ V, $I_C = 4.0$ A	—	2.75	V
Supply Current per Driver	I_S	7	All	$I_C = 500$ mA, $V_{IN} = 2.75$ V	—	6.0	mA
Turn-On Delay	t_{PLH}	—	All	0.5 E_{in} to 0.5 E_{out}	—	1.0	μs
Turn-Off Delay	t_{PHL}	—	All	0.5 E_{in} to 0.5 E_{out}, $I_C = 3.0$ A	—	1.5	μs
Clamp Diode Leakage Current	I_R	5	All	$V_R = 50$ V	—	50	μA
				$V_R = 50$ V, $T_A = +70°C$	—	100	μA
			UDN-2879W/W-2	$V_R = 80$ V	—	50	μA
				$V_R = 80$ V, $T_A = +70°C$	—	100	μA
Clamp Diode Forward Voltage	V_F	6	All	$I_F = 3.0$ A	—	2.5	V
			UDN-2878/2879W	$I_F = 4.0$ A	—	3.0	V

CAUTION: High-current tests are pulse tests or require heat sinking.

TEST FIGURES
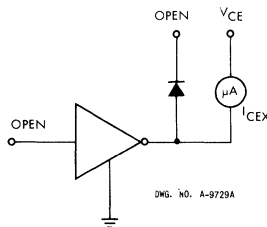
Figure 1
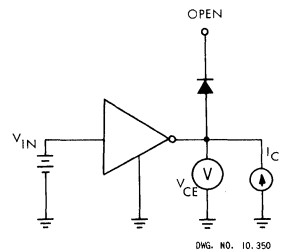
Figure 2

TEST FIGURES (Continued)
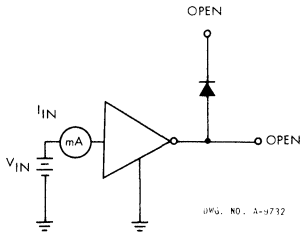
Figure 3
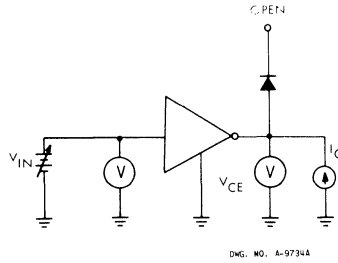
Figure 4
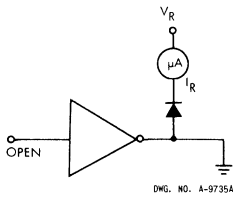
Figure 5
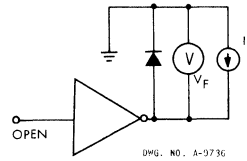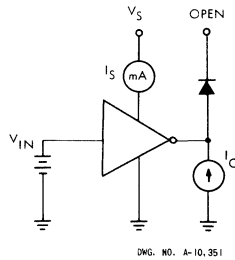
Figure 6

Figure 7

TYPICAL APPLICATIONS

STEPPER-MOTOR DRIVER

UDN-2878W
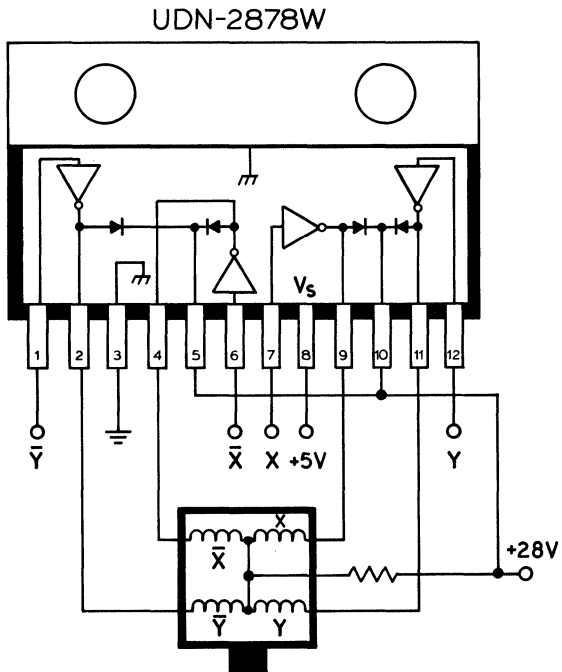
DWG. NO. A-11,975

INPUT WAVEFORMS
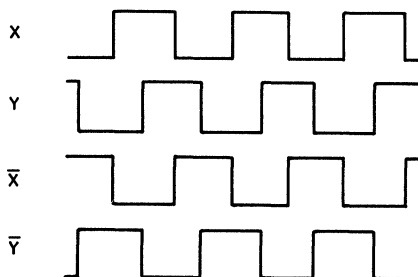
Dwg. No. A-11,795

TYPICAL APPLICATIONS (Continued)

UDN-2879W

PRINT-HAMMER DRIVER

DWG. NO. A-11,976

UDN-2879W
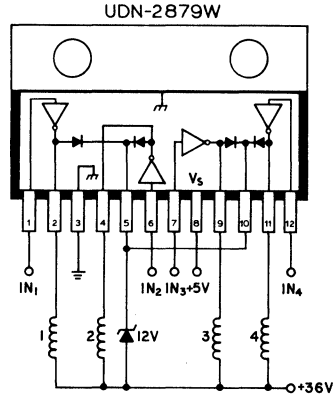
DIGIT DRIVER
FOR MULTIPLEXED INCANDESCENT LAMP DISPLAY
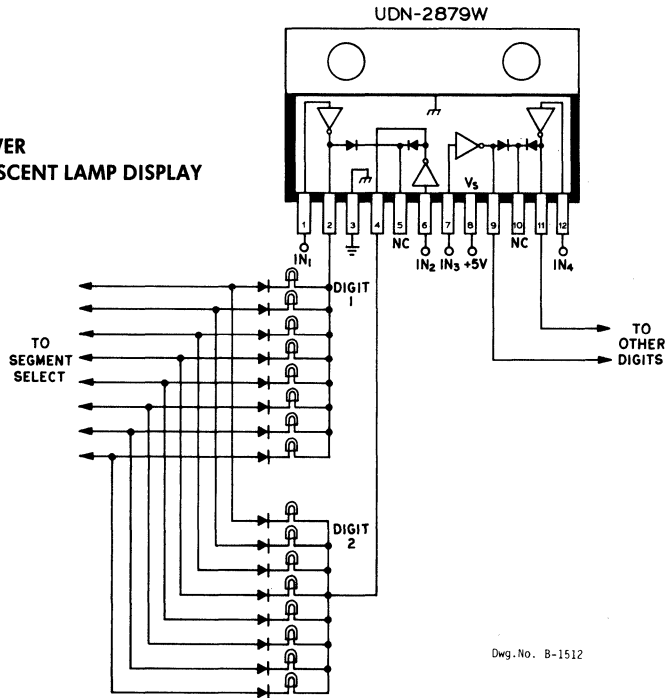
Dwg.No. B-1512

UTN-2886B AND UTN-2888A
MONOLITHIC SCR ARRAYS

FEATURES

- Low Input Current
- TTL, LSTTL and CMOS Compatible
- Momentary Inrush Current Capability to 2 A
- Minimum Forward Blocking Voltage 35 V
- Use with Full-Wave or Half-Wave Sources

INTENDED FOR USE with microprocessors that are strobing power loads, these monolithic SCR arrays will interface to high-current loads including lamps, relays, and solenoids. The use of multiple SCRs in a single package reduces component count, insertion costs, assembly time, and circuit space, while improving overall circuit reliability.

Each array contains multiple SCRs with integral current limiting and gate-to-cathode resistors. In all cases, the maximum allowable SCR current rating at +25°C is 800 mA continuous or 2 amperes non-recurring peak. Outputs may be paralleled for higher load current capability within the limits of the allowable package power dissipation rating.

The UTN-2886B array contains four individual SCRs and two pairs of paralleled SCRs (pins 8-9 and 1-16). Each SCR is capable of continuous and simultaneous operation at 250 mA (500 mA at pins 9 and 16) at an ambient temperature of +50°C. The 16-lead package with heat-sink contact tabs allows maximum power dissipation with standard cooling methods. Further increases in power dissipation can be obtained by attaching an external heat sink to the webbed leads.

The UTN-2888A SCR array contains eight isolated devices, each capable of continuous and simultaneous operation at 200 mA at an ambient temperature of +50°C.

These SCR arrays operate from an unfiltered half-wave (50 or 60 Hz) or full-wave (100 or 120 Hz) rectified source. They are not intended for use with a-c sources, and will not sustain commercial a-c line voltages (115 VAC).
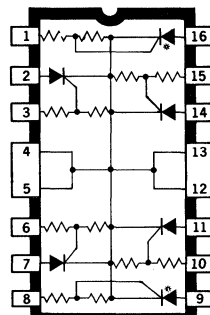
*Two Parallel SCRs
Dwg. No. A-11,092

UTN-2886B
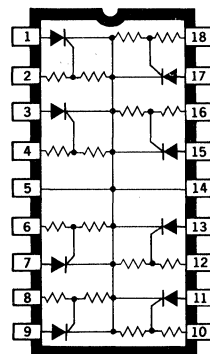
Dwg. No. A-11,093

UTN-2888A

ABSOLUTE MAXIMUM RATINGS
for any one individual SCR*

Forward Blocking Voltage (Input Open), V_{AK} . . . . 35 V
Reverse Blocking Voltage, V_{KA} . . . . 300 mV
Continuous Forward Current, I_A . . . . 800 mA
Peak Forward Surge Current, I_A . . . . 2.0 A
Gate Input Power, P_{IN} . . . . 10 mW
Peak Gate Input Power, P_{IN} . . . . 50 mW
Gate Input Current, I_{IN} . . . . 50 mA
Reverse Gate Input Voltage, V_{IN} . . . . 5.0 V
Total Package Power Dissipation, P_D . . . . See Graph
Operating Temperature Range, T_A . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . . $-55°C$ to $+150°C$

ALLOWABLE AVERAGE POWER DISSIPATION
AS A FUNCTION OF AMBIENT TEMPERATURE
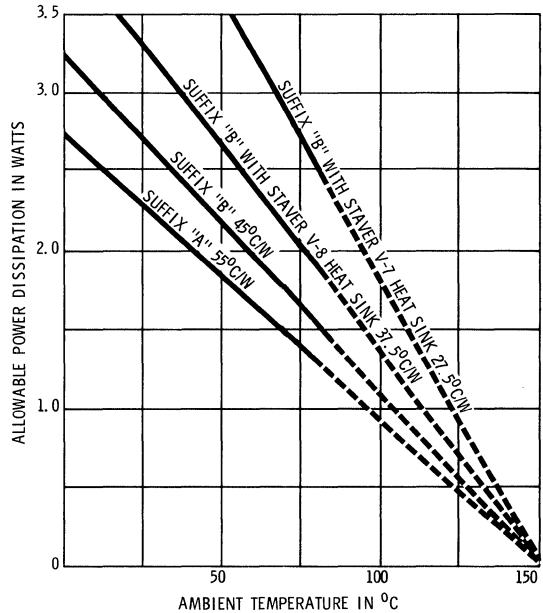
Dwg. No. A-11,090

3

ELECTRICAL CHARACTERISTICS for any one individual SCR*

Characteristic	Symbol	Test Temp.	Test Conditions	Limits Min.	Limits Max.	Units
Forward Blocking Current	I_A	+70°C	$V_{AK} = 35$ V, $V_{IN} = 100$ mV	—	50	μA
Gate-to-Anode Leakage Current	I_{IN}	+70°C	$V_{AK} = 0$ V, $V_{IN} = 5.0$ V	—	250	μA
Forward ON Voltage	$V_{AK(ON)}$	+25°C	$I_A = 275$ mA, $V_{IN} = 2.5$ V	—	1.2	V
		+55°C	$I_A = 275$ mA, $V_{IN} = 2.5$ V	—	1.15	V
Gate Trigger Current	$I_{IN(ON)}$	+25°C	$V_{AK} = 7.0$ V, $V_{IN} = 2.5$ V, $R_L = 50\Omega$	—	300	μA
Gate Trigger Voltage	$V_{IN(ON)}$	+25°C	$V_{AK} = 1.7$ V, $t_{gt} = 20$ μs, $R_L = 50\Omega$	—	2.5	V
Gate OFF Voltage	$V_{IN(OFF)}$	+70°C	$V_{AK} = 35$ V, $R_L = 50\Omega$	100	—	mV
Gate OFF Current	$I_{IN(OFF)}$	+70°C	$V_{AK} = 35$ V, $R_L = 50\Omega$	—	10	μA
Holding Current	I_H	0°C	$I_{IN(INIT.)} = 20$ mA	—	10	mA
		+55°C	$I_{IN(INIT.)} = 20$ mA	—	5.0	mA
Anode OFF Voltage	$V_{AK(OFF)}$	+55°C	$V_{IN} = 5.0$ V, $R_L = 50\Omega$	400	—	mV

*I_A, I_{IN}, and I_H test conditions and limits for the paralleled SCRs at pin 8-9 or pin 1-16 of the UTN-2886B are twice the value shown.
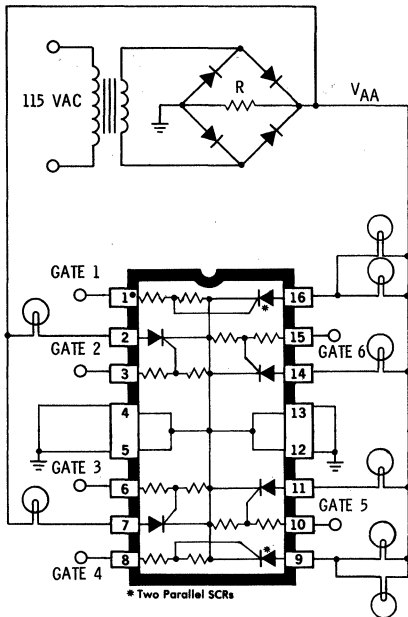
Dwg. No. A-11,091

TYPICAL LAMP APPLICATION
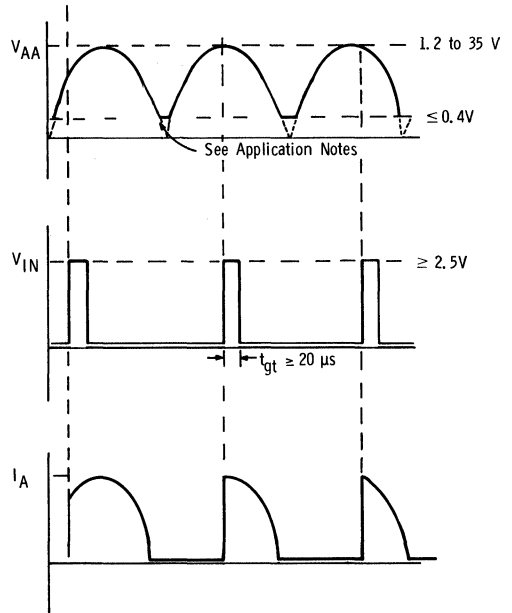
Dwg. No. A-11,089

TYPICAL WAVEFORMS

APPLICATION NOTES

1. These devices normally operate from an unfiltered half-wave or full-wave rectified source. They *cannot* be operated with a bidirectional (unrectified) a-c source.

2. During operation, the SCR is turned ON by application of a positive voltage to the input. The SCR will remain ON, even though the input voltage is removed or made slightly negative, until the anode-to-cathode voltage is reduced to below the anode OFF voltage.

3. When using multiple SCRs and a common supply, gate-to-anode leakage currents can hold the supply voltage above the anode OFF voltage and prevent proper turn-OFF. To insure proper operation, resistor R should be used as shown in the typical application. The maximum resistor value is determined from:

$$R = \frac{V_{AK(OFF)}}{(n-1)\, I_{GA}} = \frac{400\ mV}{(n-1)\, 250\,\mu A}$$

where n is the number of SCRs being used in the system. Note that n = 2 for pin 8-9 and pin 1-16 of the UTN-2886B.

4. Various combinations of number of outputs conducting, duty cycle, and ambient temperature must be held within the allowable package power dissipation limits shown.

UDN-2935Z AND UDN-2950Z
BIPOLAR HALF-BRIDGE MOTOR DRIVERS

FEATURES

- 3.5 A Peak Output
- 37 V Min. Output Breakdown
- Output Transient Protection
- Tri-State Outputs
- TTL, CMOS, PMOS, NMOS Compatible Inputs
- Internal Thermal Shutdown
- High-Speed Chopper (to 100 kHz)
- UDN-2935Z Replaces SG3635P
- UDN-2950Z Replaces UDN-2949Z, SN75605
- TO-220 Style Packages

Dwg.No. A-12,116

UDN-2935Z

DWG. NO. A-11,177

UDN-2950Z

3

BOTH Type UDN-2935Z and UDN-2950Z integrated circuits are designed for servo-motor applications using pulse-width modulation. These two high-current, monolithic half-bridge motor drivers combine a sink-and-source driver with diode transient protection, input gain, level shifting, logic stages, and a voltage regulator for single-supply operation.

The UDN-2935Z output goes high with an active low input at pin 2; it is especially desirable in NMOS microprocessor applications. The UDN-2950Z output goes high with an active high input at pin 2; its inputs can be tied together for single-wire control. The input circuitry of both devices is compatible with TTL and low-voltage CMOS, PMOS, and NMOS logic. Both ICs have logic lockout (tri-state output) that prevents source and sink drivers from turning ON simultaneously.

In typical applications, the chopper-drive mode is characterized by low power-dissipation levels, low saturation voltages, and short chopper-storage
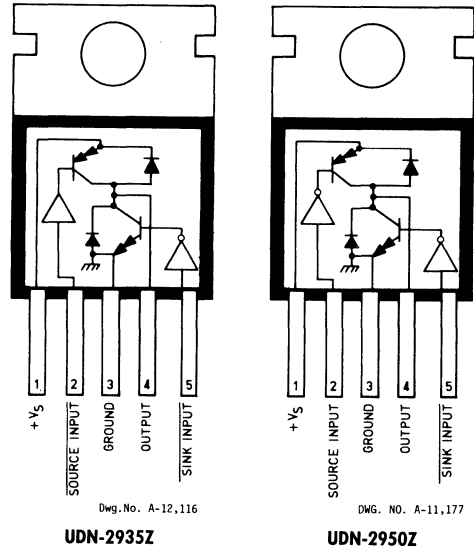
times for the sink drivers. The motor drivers can be used in pairs for full-bridge operation, or as triplets in three-phase brushless d-c motor-drive applications. They can also be teamed with the Sprague Electric UCN-4202A stepper motor translator/driver for bipolar d-c stepper motor control

The motor drivers' single-chip construction and power-tab TO-220 package enable cost-effective and reliable system designs supported by excellent power-dissipation ratings, minimum size, and ease of installation; because the package's heat tab is at ground potential, several devices can share a common heat sink without insulating hardware.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_S .... 8.0 V to 35 V
Output Voltage Range, V_{OUT} .... -2.0 V to $V_S + 2.0$ V
Input Voltage Range, V_{IN} .... -0.3 V to $+7.0$ V
Peak Output Current (100 ms, 10% d-c), I_{OP} .... ± 3.5 A
Continuous Output Current, I_{OUT} .... ± 2.0 A
Package Power Dissipation, P_D .... See Graph
Operating Temperature Range, T_A .... $-20°C$ to $+85°C$
Storage Temperature Range, T_S .... $-55°C$ to $+85°C$

ALLOWABLE POWER DISSIPATION
AS A FUNCTION OF AMBIENT TEMPERATURE

DWG. NO. A-12,000A
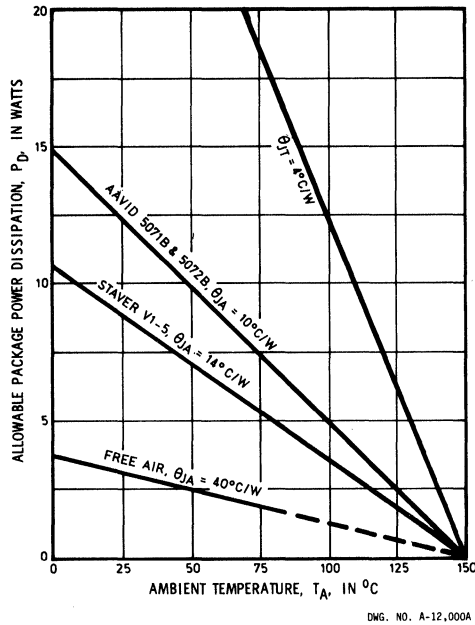
TRUTH TABLE

Source Driver, Pin 2	Sink Driver, Pin 5	Output, Pin 4	
		UDN-2935Z	UDN-2950Z
Low	Low	High	Low
Low	High	High	High Z
High	Low	Low	High
High	High	High Z	High

FUNCTIONAL BLOCK DIAGRAMS

UDN-2935Z
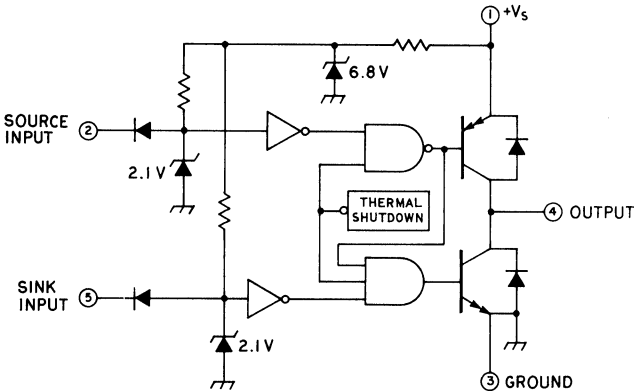
Dwg.No. A-12,113
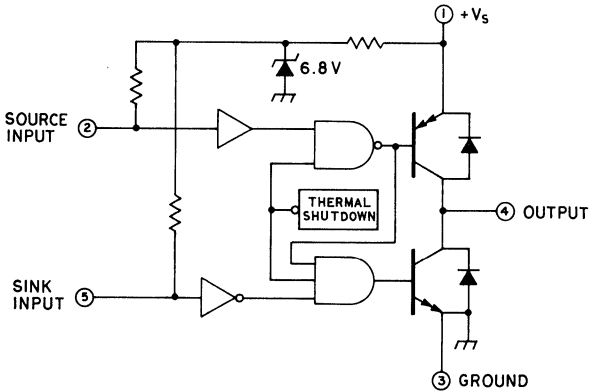
UDN-2950Z

Dwg.No. A-12,112

ELECTRICAL CHARACTERISTICS at T$_A$ = +25°C, T$_{TAB}$ = +70°C, V$_S$ = 35 V (unless otherwise noted)

Characteristic	Source Driver Input, Pin 2		Sink Driver Input, Pin 5	Output, Pin 4	Other	Limits		
	UDN-2935Z	UDN-2950Z				Min.	Max.	Units
Output Leakage Current	2.4 V	0.8 V	2.4 V	0 V	—	—	−500	μA
	2.4 V	0.8 V	2.4 V	35 V	—	—	500	μA
Output Sustaining Voltage	2.4 V	0.8 V	0.8 to 2.4 V	2.0 A	Fig. 1	35	—	V
Output Saturation Voltage	0.8 V	2.4 V	2.4 V	−2.0 A	—	33	—	V
	2.4 V	0.8 V	0.8 V	2.0 A	—	—	2.0	V
Output Source Current	0.8 V	2.4 V	2.4 V	—	—	−2.0	—	A
Output Sink Current	2.4 V	0.8 V	0.8 V	—	—	2.0	—	A
Input Open-Circuit Voltage	−250 μA	−250 μA	−250 μA	—	—	—	7.5	V
Input Current	—	2.4 V	2.4 V	NC	—	—	−700	μA
	2.4 V	—	2.4 V	NC	—	—	10	μA
	0.8 V	0.8 V	0.8 V	NC	—	—	−1.6	mA
Propagation Delay	2.4 V	0.8 V	0.8 to 2.4 V	2.0 A	—	—	750	ns
	0.8 to 2.4 V	2.4 to 0.8 V	2.4 V	2.0 A	—	—	2.0	μs
Clamp Diode Forward Voltage	NC	NC	NC	2.0 A	Fig. 2	—	2.2	V
Supply Current	0.8 V	2.4 V	NC	NC	—	—	35	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TEST FIGURE 1

Dwg.No. A-12,117

TEST FIGURE 2

Dwg.No. A-12,118
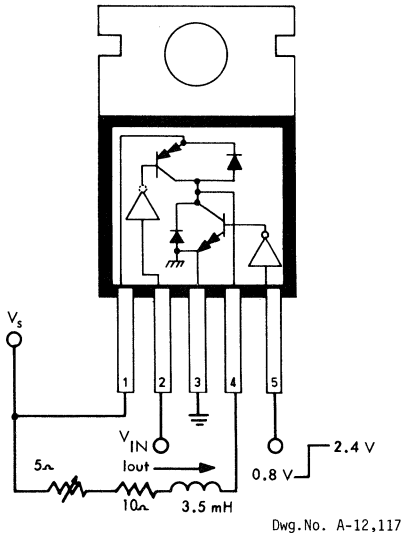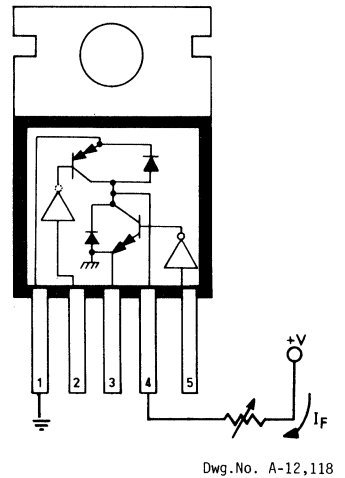
APPLICATION NOTES

It should be noted that an additional power dissipation component may arise from crossover currents flowing from supply to ground when current direction through the load is reversed. This is due to differences in the switching speeds between the source and sink drivers. Although the internal logic lockout protects these devices from catastrophic failure, the crossover power component can cause device operation at substantially higher junction temperatures.

If timing conditions are ignored, the magnitude of this power can be approximated as:

$$P_D = V_S \times I_C \times t \times f$$

where V_S = supply voltage
I_C = crossover current (≈ 3.5 A max.)
t = crossover current duration (≈ 1 µs)
f = frequency of direction change

In some applications (high switching speeds or high package power dissipation), it is recommended that the inputs be driven separately, and that the sink driver not be turned ON for at least 2 µs (maximum source t_{PD}) after the source driver input is turned OFF. The sink driver should be turned OFF at least 750 ns (maximum sink t_{PD}) before the source driver is turned ON.

RECOMMENDED TIMING CONDITIONS
(UDN-2950Z shown)

Dwg. No. A-12,120

Dwg. No. A-12,119
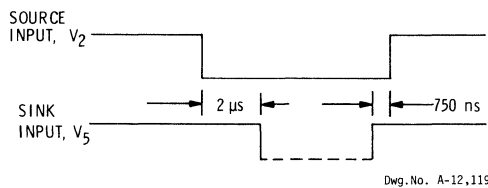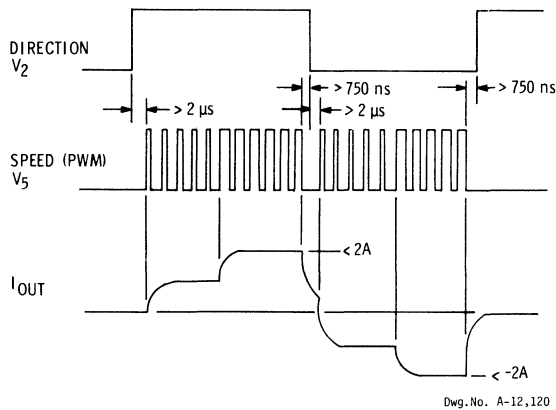
TYPICAL APPLICATIONS

3-PHASE BRUSHLESS D-C MOTOR DRIVE

Dwg. No. B-1523
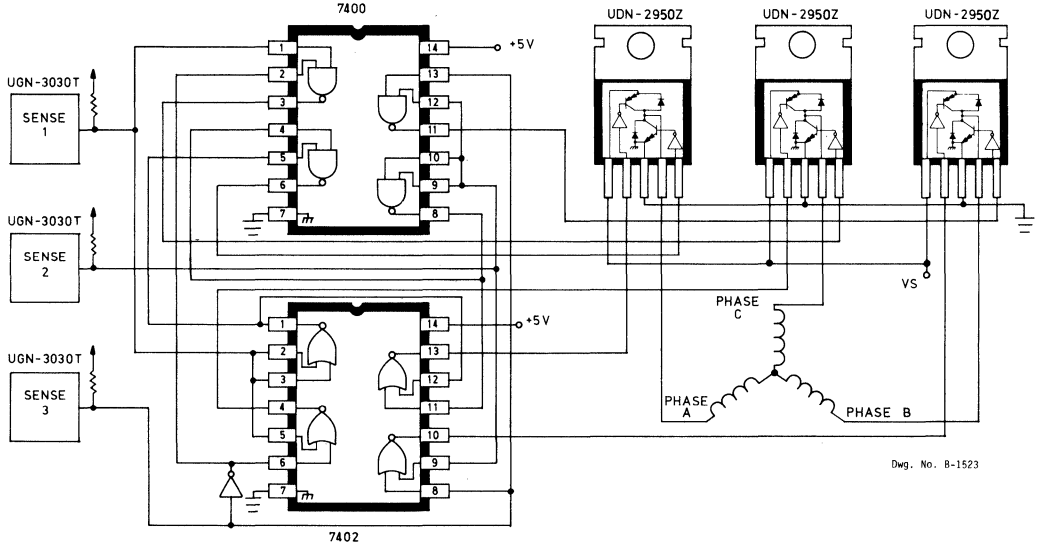
SINGLE-WINDING D-C OR STEPPER MOTOR DRIVE

Dwg. No. A-12,114
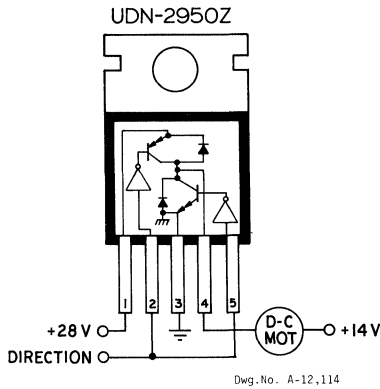
FULL-BRIDGE D-C SERVO MOTOR DRIVE

Dwg. No. A-12,115
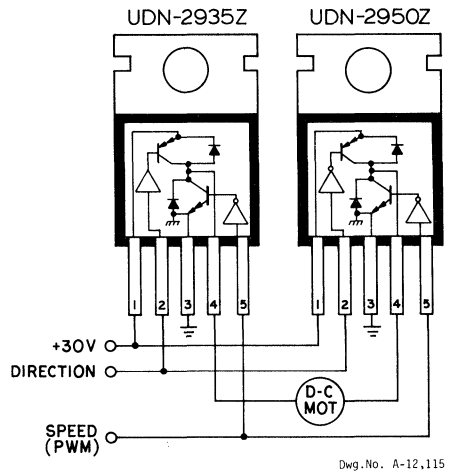
UDN-2949Z HIGH-CURRENT BIPOLAR HALF-BRIDGE MOTOR DRIVER

FEATURES

- 3.5 A Peak Output
- 30 V Output Breakdown
- Output Transient Suppression
- TTL, CMOS, PMOS, NMOS Compatible Inputs
- High-Speed Chopper (to 100 kHz)
- Low Standby Current (10 mA)
- TO-220 Style Package

THE UDN-2949Z is a monolithic half-bridge motor driver supplied in a power-tab TO-220 style package. The circuit combines sink and source drivers with diode protection, gain and level shifting systems, and a voltage regulator for single-supply operation. The unit is specifically designed for servomotor drive applications using pulse-width modulation (chopping).

The chopper drive mode is characterized by a minimum power dissipation requirement, low saturation voltages, and low chopper storage times for the NPN sink driver. Predriver stages reduce input drive requirements while allowing the output to switch currents of 2 amperes.

The PNP sourcing driver is turned ON by an active high input while the NPN sinking driver is activated with a low input. These inputs are completely compatible with TTL, low-voltage CMOS, PMOS, and NMOS.

The UDN-2949Z may be used in pairs (full-bridge) for d-c stepper motor or brushless a-c motor drive applications. Such applications may require an external ground clamp diode (1N4000) connected at the output of each device in order to minimize package power dissipation.
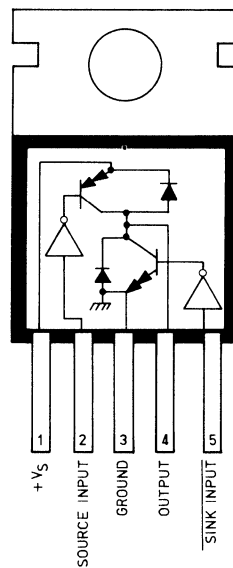
DWG. NO. A-11,177

Single-chip construction and the power-tab TO-220 style package provide improved cost effectiveness and reliability over discrete component motor drive systems with excellent power dissipation capability, minimum size, ease of installation, and heat sinking.

The package heat tab is at ground potential. Multiple devices may share a common heat sink without insulating hardware.

The UDN-2949Z power driver may be used in stepper-motor bipolar bridge-driver circuits, for example, with the Sprague UCN-4202A Stepper Motor Translator/Driver.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_S . . . . 15 V to 30 V

Input Voltage Range, V_{IN} . . . . −0.3 V to +7.0 V

Peak Output Current (100 ms, 10% d.c.), I_{OP} . . . . . ±3.5 A

Continuous Output Current, I_{OUT} . . . . ±2.0 A

Package Power Dissipation, P_D . . . . See Graph

Operating Temperature Range, T_A . . . . . −20°C to +85°C

Storage Temperature Range, T_S . . . . . −55°C to +150°C

LOGIC TRUTH TABLE

Source Driver Input, V_2	Sink Driver Input, V_5	Output, V_4
Low	Low	Low
Low	High	Open
High	High	High
High	Low	Disallowed

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_S = 24 V (unless otherwise noted).

Characteristic	Test Conditions				Limits		Units
	Source Driver Input, Pin 2	Sink Driver Input, Pin 5	Output Pin 4	Other	Min.	Max.	
Output Leakage Current	0.8 V	2.4 V	0 V	V_S = 28 V	—	−500	μA
	0.8 V	2.4 V	28 V	V_S = 28 V	—	500	μA
Output Sustaining Voltage	0.8 V	0.8 to 2.4 V	2.0 A	Test Fig. 1	30	—	V
Output Saturation Voltage	2.4 V	2.4 V	−2.0 A		22	—	V
	0.8 V	0.8 V	2.0 A		—	2.0	V
Output Source Current	2.4 V	2.4 V	—		−2.0	—	A
Output Sink Current	0.8 V	0.8 V	—		2.0	—	A
Input Open-Circuit Voltage	−250 μA	−250 μA	—		—	7.5	V
Input Current	2.4 V	2.4 V	NC		—	−700	μA
	0.8 V	0.8 V	NC		—	−5.0	mA
Propagation Delay	0.8 V	0.8 to 2.4 V	NC		—	750	ns
	0.8 to 2.4 V	2.4 V	NC		—	5.0	μs
Clamp Diode Forward Voltage	NC	NC	2.0 A	Test Fig. 2	—	2.2	V
Supply Current	NC	NC	NC		—	35	mA

Note: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TEST FIGURE 1

DWG. NO. A-11,178

DWG. NO. A-11,179
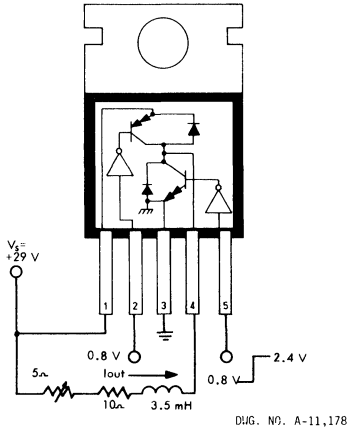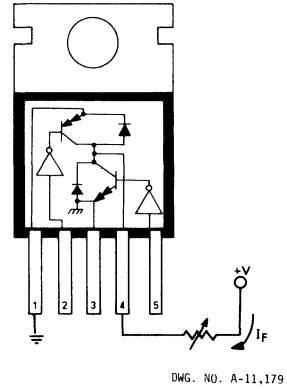
TEST FIGURE 2

APPLICATION NOTES

1. The source and sink outputs should not be ON simultaneously (V_2 High, V_5 Low). High "crossover" currents could degrade or destroy the device.

2. Do not assume from the Logic Truth Table that both inputs can be connected (V_4 High or Low only). The sink driver is considerably faster than the source driver. An input shift from high-to-low levels could produce a condition where both drivers are ON, and that condition could occur for as long as 5 μs.

3. It is recommended that the inputs be driven separately, and that the sink driver input

not be pulled low (turned ON) for at least 5 μs (max. source t_{PD}) after the source driver input is pulled low (turned OFF). The sink driver should be allowed to go high (turned OFF) at least 750 ns (max. sink t_{PD}) before the source driver goes high (turned ON).
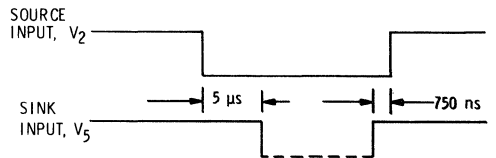
DWG. NO. A-11,242

Timing Conditions
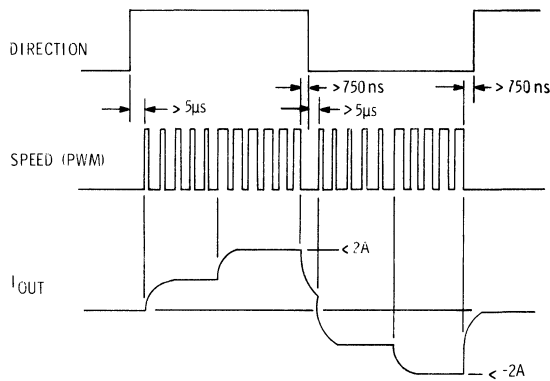
DWG. NO. A-11,241

**PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE**
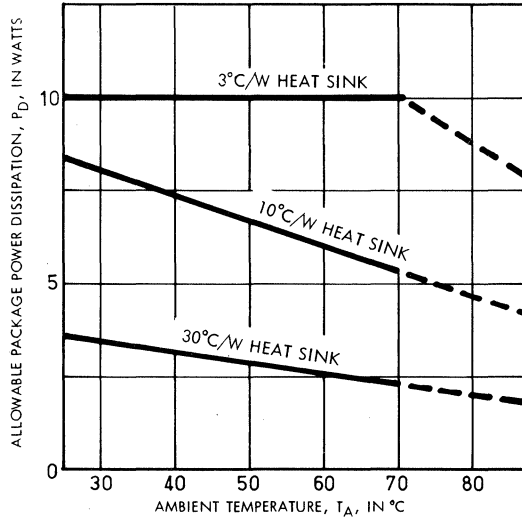
DWG. NO. A-11,183

SINGLE-WINDING D-C OR STEPPER MOTOR
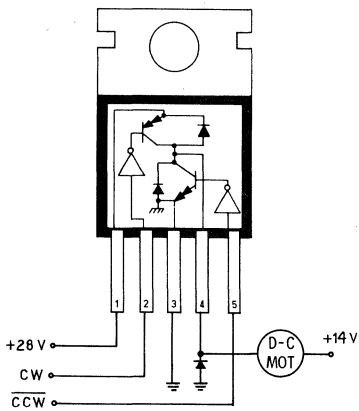
Dwg. No. A-11,181A

FULL-BRIDGE D-C SERVO MOTOR APPLICATION
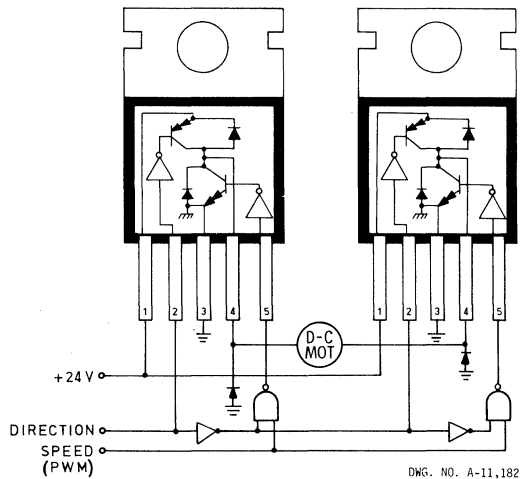
DWG. NO. A-11,182

UDN-2952B AND UDN-2952W
FULL-BRIDGE MOTOR DRIVERS

FEATURES

- High Output Current
- Adjustable Short-Circuit Protection
- Thermal Protection
- Internal Clamp Diodes
- TTL, DTL, PMOS, CMOS Compatible
- DIP or SIP Packaging

FULL-BRIDGE MOTOR-DRIVER integrated circuits, Types UDN-2952B and UDN-2952W combine low-level logic circuitry and Darlington output power drivers for bidirectional control of d-c motors or solenoids operating with continuous load currents of up to 2 A and peak start-up currents as high as 3.5 A.

For applications requiring load currents of 1 A or less (2 A peak), the economical Type UDN-2952B-2 and UDN-2952W-2 are recommended. The lower-
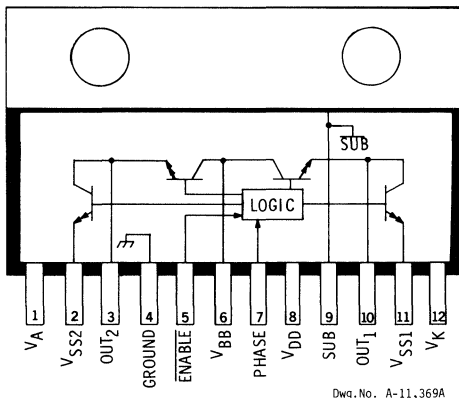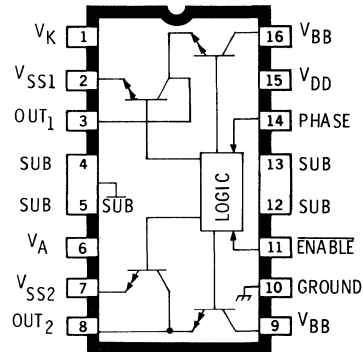
Dwg. No. A-11,368B

UDN-2952B

cost devices are identical to the basic parts, except for the maximum allowable load-current rating.

These monolithic integrated circuits have extensive circuit protection. Both drivers have thermal shutdown networks that disable motor drive if the package power dissipation ratings are exceeded. Internal diode transient suppression is provided on-chip. Output-current limiting is determined by the user's selection of a sensing resistor.

The Type UDN-2952B full-bridge power driver is supplied in a 16-pin dual in-line plastic package with copper heat-sink contact tabs. The lead configuration enables easy attachment of a heat sink while fitting a standard integrated circuit socket or printed wiring board layout. Type UDN-2952W, for higher power requirements, is in a 12-pin single in-line power tab package. The tab is at ground potential and needs no insulation. For output currents above 700 mA at normal ambient temperatures, both drivers require an external heat sink.

Dwg. No. A-11,369A

UDN-2952W

ABSOLUTE MAXIMUM RATINGS
at $T_{TAB} = +70°C$

Motor Supply Voltage Range, V_{BB} . . . . 4.5V to 40V
Logic Supply Voltage Range, V_{DD} . . . . 4.5V to 15V
Substrate Voltage Range, V_{SUB} . . . . 0V to −20V
Logic Input Voltage, V_{PHASE} or V_{ENABLE} 30V
Output Current, I_{OUT} (UDN-2952B and UDN-2952W) . . . . ±3.5A
        (UDN-2952B-2 and UDN-2952W-2) . . . ±2A
Package Power Dissipation, P_D . . . . See Graphs
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −55°C to +150°C

TRUTH TABLE

$\overline{ENABLE}$	PHASE	V_{SS}	V_{DD}	OUT_1	OUT_2
High	X	X	X	Open	Open
Low	High	<0.8 V	>4.5 V	High	Low
Low	Low	<0.8 V	>4.5 V	Low	High
X	X	>0.9 V	>4.5 V	Open	Open
X	X	X	0 V	Open	Open

X = Irrelevant.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 40V$, $V_{DD} = 5V$, $T_{TAB} \leq +70°C$,
Figure 1 (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Output Drivers (OUT₁ or OUT₂)						
Output Leakage Current	I_{CEX}	$V_{ENABLE} = 5V$, $V_{OUT} = V_{BB}$, Note 1	—	—	500	μA
		$V_{ENABLE} = 5V$, $V_{OUT} = 0V$, Note 1	—	—	−500	μA
Output Saturation Voltage	$V_{CE(SAT)}$	$V_{ENABLE} = 0V$, $I_{OUT} = 1A$, Notes 1 and 2	—	1.2	1.5	V
		$V_{ENABLE} = 0V$, $I_{OUT} = 2A$, Notes 1 and 3	—	1.5	2.0	V
Output Sustaining Voltage	$V_{CE(SUS)}$	$I_{OUT} = 1A$, Figure 2, Notes 1 and 2	40	—	—	V
		$I_{OUT} = 2A$, Figure 2, Notes 1 and 3	40	—	—	V
Motor Supply Current	$I_{BB(ON)}$	$V_{ENABLE} = 0.8V$, Outputs Open, Note 1	—	15	30	mA
	$I_{BB(OFF)}$	$V_{ENABLE} = 2.4V$, Outputs Open, Note 1	—	3.0	5.0	mA
Clamp Diode Forward Voltage	V_F	$I_F = 1A$, Note 2	—	1.0	1.5	V
		$I_F = 2A$, Note 3	—	1.8	2.2	V
Control Logic (PHASE or ENABLE)						
Logic Open-Circuit Voltage	V_{IN}	I_{PHASE} or $I_{ENABLE} = -250$ μA	—	—	7.5	V
Logic Input Current	$I_{IN(1)}$	V_{PHASE} or $V_{ENABLE} = 2.4V$	—	−50	−100	μA
	$I_{IN(0)}$	V_{PHASE} or $V_{ENABLE} = 0.8V$	—	−1.0	−1.6	mA
Logic Input Voltage	$V_{IN(1)}$		2.4	—	—	V
	$V_{IN(0)}$		—	—	0.8	V
Logic Supply Current	I_{DD}		—	15	30	mA
Sense Trigger Voltage	V_{SS}	$V_{ENABLE} = 0.8V$	—	850	—	mV
Turn-On Delay Time	t_{pd0}	Source Drivers	—	1.0	—	μs
		Sink Drivers	—	0.5	—	μs
Turn-Off Delay Time	t_{pd1}	Source Drivers	—	2.0	—	μs
		Sink Drivers	—	1.0	—	μs
Thermal Shutdown	T_J		—	175	—	°C

NOTES: 1. Test is performed with $V_{PHASE} = 0.8V$ and then repeated for $V_{PHASE} = 2.4V$.
     2. Output measurement at 1A are applicable to the UDN-2952B, UDN-2952B-2, UDN-2952W, and UDN-2952W-2.
     3. Output measurements at 2A are applicable only to the UDN-2952B and UDN-2952W.

FUNCTIONAL BLOCK DIAGRAM
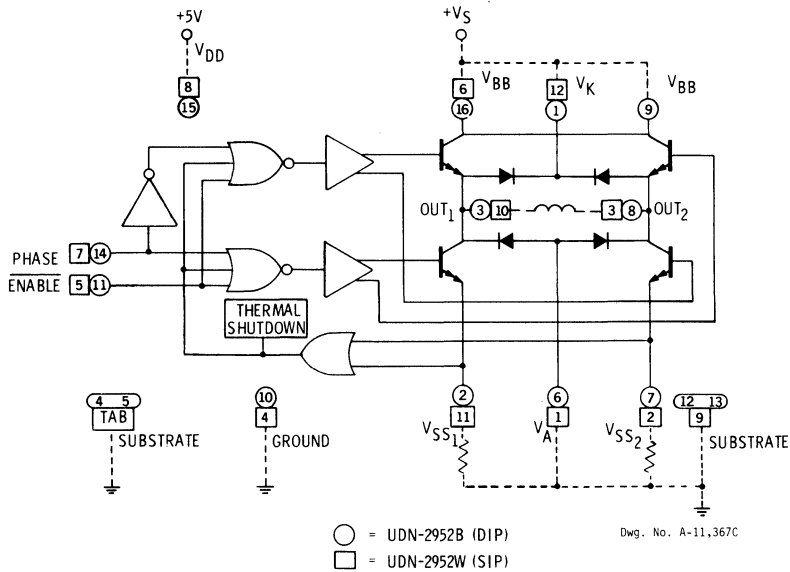
Dwg. No. A-11,367C

○ = UDN-2952B (DIP)
□ = UDN-2952W (SIP)

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE

UDN-2952B

Dwg. No. A-11,793A

UDN-2952W
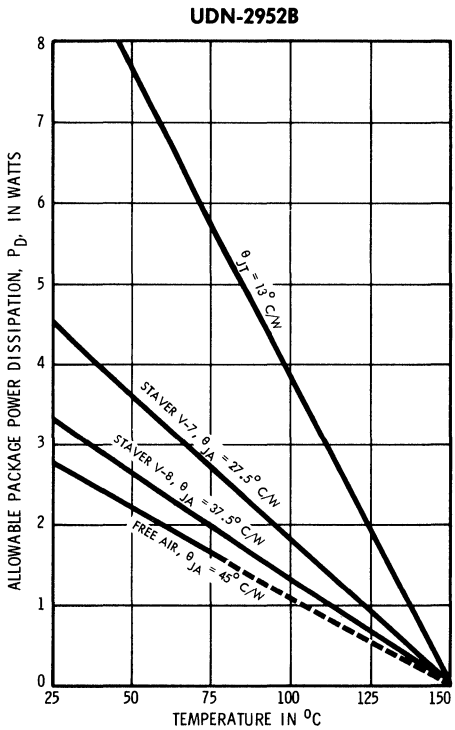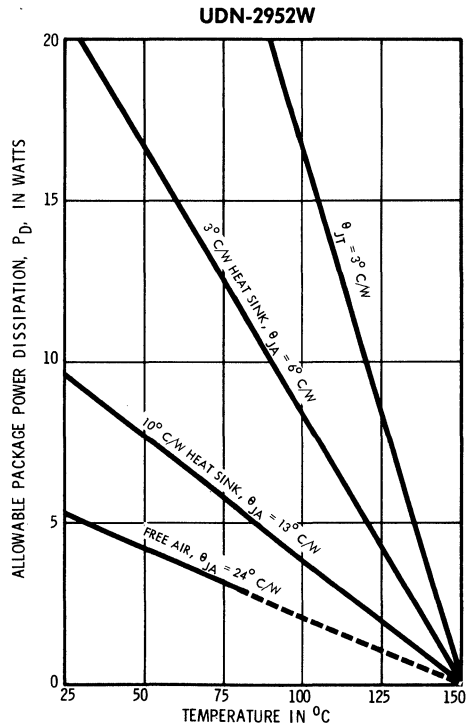
Dwg. No. A-11,794

TEST FIGURES
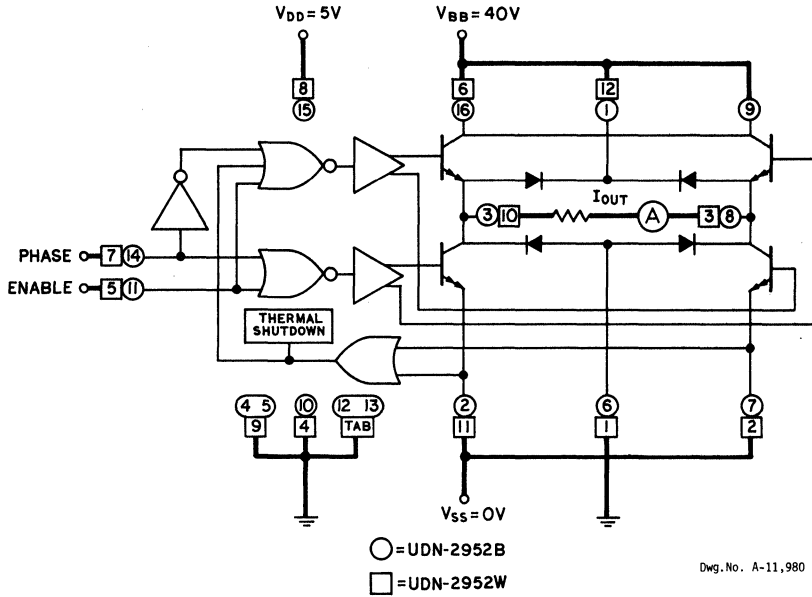
FIGURE 1
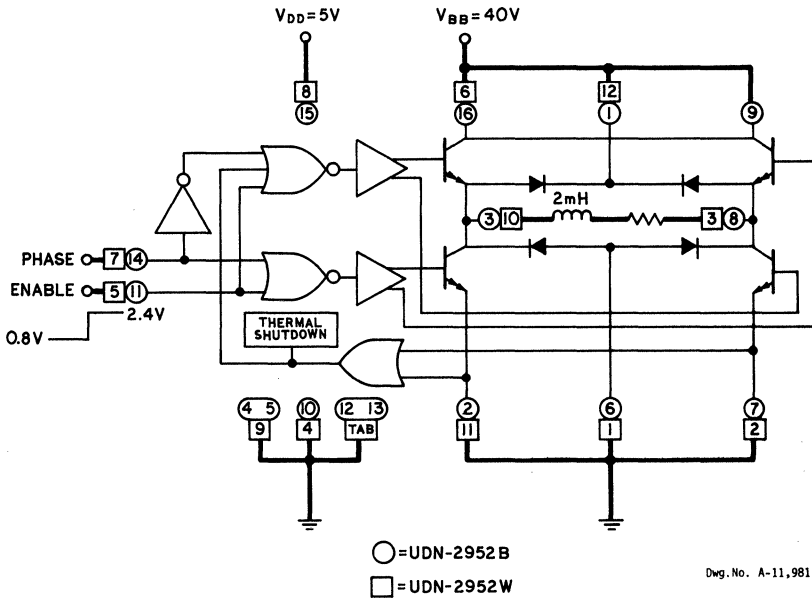
FIGURE 2

TYPICAL APPLICATIONS

Dwg.No. B-1511
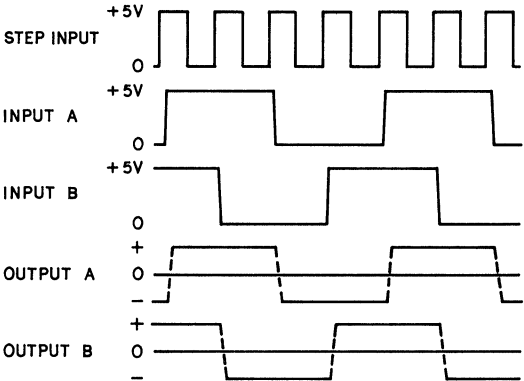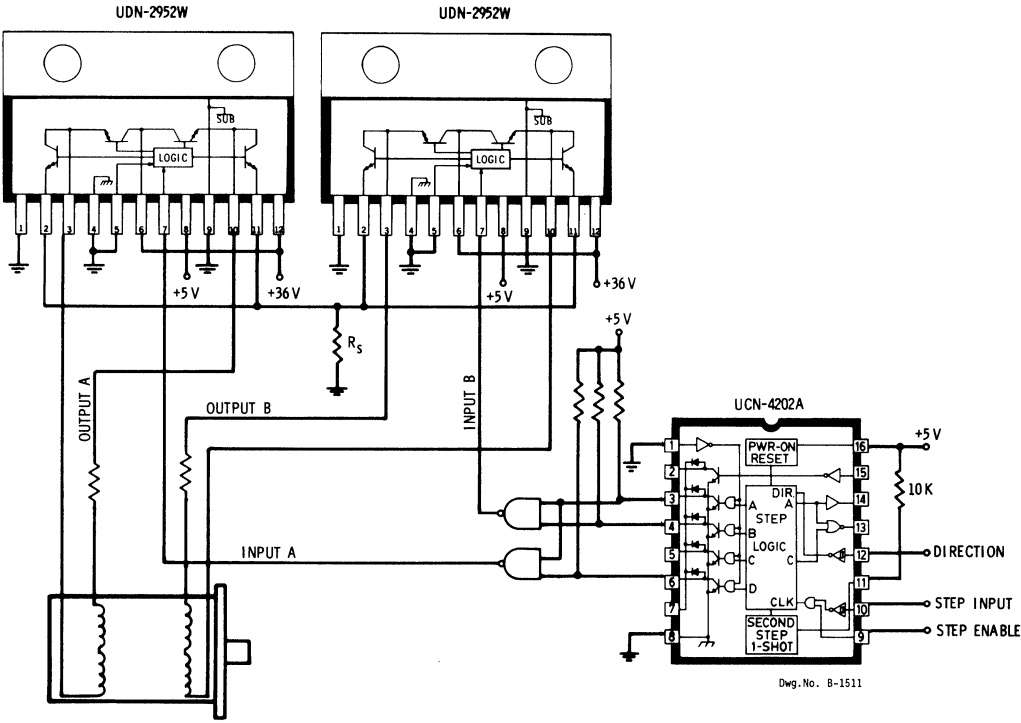
Dwg.No. A-11,982

NOTES:
  1. This is *not* a bipolar chopper application.
  2. Resistor R_S sets the maximum allowable output current for protection against crossover currents and short circuits. $R_S = 0.6/I_{LIMIT}$.

TYPICAL APPLICATIONS (Continued)

FULL-BRIDGE D-C SERVO MOTOR APPLICATION
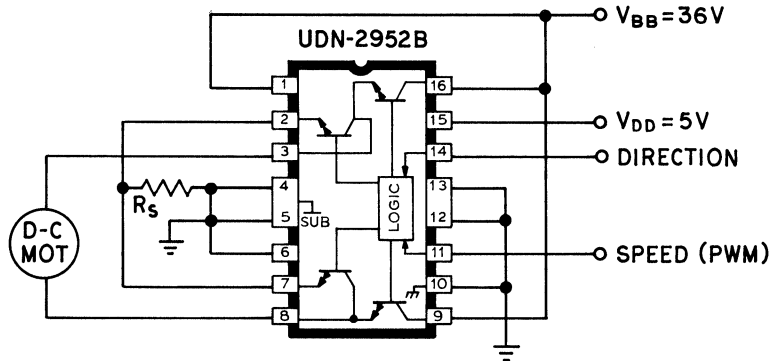
Dwg. No. A-11,984
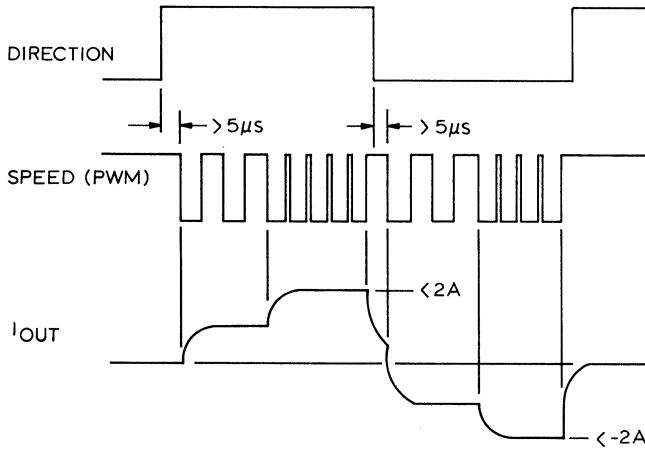
Dwg. No. A-11,983

UDN-2956A AND UDN-2957A
HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

COMPRISED of five common collector NPN Darlington output stages, the associated common base PNP input stages, and a common "enable" stage, the UDN-2956A and UDN-2957A high-voltage, high-current source drivers are used to switch the ground end of loads which are directly connected to a negative supply. Typical loads include telephone relays, PIN diodes, and LEDs. Both devices will sustain output OFF voltages of −80 V and will source currents to −500 mA per driver. Under normal operating conditions, these units will sustain load currents of −200 mA on each of the five drivers simultaneously at ambient temperatures up to +70°C.

The UDN-2956A driver is intended for use with MOS (PMOS or CMOS) logic input levels operating with supply voltages from 6 V to 16 V. The UDN-2957A driver has appropriate input current limiting resistors for operation from TTL, Schottky TTL, DTL, and 5 V CMOS. With either device, the input and enable levels must both be biased towards the positive supply to activate the output load.

Integral transient suppression diodes allow these devices to be used with inductive loads without the need for discrete diodes. In order to maintain isolation between drivers, the substrate should be connected to the most negative supply applied.

Input connections are on one side of the dual in-line package, output connections on the other side to simplify printed wiring board layout.

The UDN-2956A and UDN-2957A high-voltage, high-current drivers are supplied in 14-lead dual in-line packages conforming to JEDEC outline

DWG. NO. A-10,229
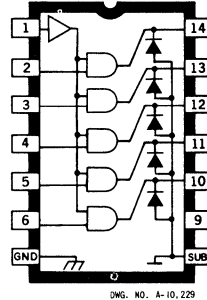
TO-116 (MO-001AA). Hermetically-sealed versions of these devices (with reduced package power dissipation capability) are available.

ABSOLUTE MAXIMUM RATINGS at 25°C
Free-Air Temperature (reference pin 7)

Supply Voltage, V_{EE} .... −80 V
Input Voltage, V_{IN} (UDN-2956A) .... +20 V
　　　　　　　　　 (UDN-2957A) .... +10 V
Output Current, I_{OUT} .... −500 mA
Power Dissipation, P_D (any one driver) .... 1.0 W
　　　　　　　　　 (total package) .... 2.0 W*
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −55°C to +150°C

*Derate at the rate of 16.67 mW/°C above 25°C.

UDN-2956A AND UDN-2957A
HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{ENABLE} = V_{IN}$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limit
Output Leakage Current	I_{CEX}	UDN-2956A	$V_{IN} = V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	$-200\,\mu$A Max.
			$V_{IN} = 0.4$ V, $V_{ENABLE} = 15$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	$-200\,\mu$A Max.
			$V_{IN} = 15$ V, $V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	$-200\,\mu$A Max.
		UDN-2957A	$V_{IN} = V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	$-200\,\mu$A Max.
			$V_{IN} = 0.4$ V, $V_{ENABLE} = 3.85$ V, $V_{OUT} = -80$ V, $T_A = +70°C$	$-200\,\mu$A Max.
			$V_{IN} = 3.85$ V, $V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V, $T_A = 70°C$	$-200\,\mu$A Max.
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	UDN-2956A	$V_{IN} = 6.0$ V, $I_{OUT} = -100$ mA	-1.20 V Max.
			$V_{IN} = 7.0$ V, $I_{OUT} = -175$ mA	-1.35 V Max.
			$V_{IN} = 10$ V, $I_{OUT} = -350$ mA	-1.70 V Max.
		UDN-2957A	$V_{IN} = 2.4$ V, $I_{OUT} = -100$ mA	-1.20 V Max.
			$V_{IN} = 2.7$ V, $I_{OUT} = -175$ mA	-1.35 V Max.
			$V_{IN} = 3.9$ V, $I_{OUT} = -350$ mA	-1.70 V Max.
Input Current	$I_{IN(ON)}$	UDN-2956A	$V_{IN} = 6.0$ V, $V_{OUT} = -2.0$ V	$650\,\mu$A Max.
			$V_{IN} = 15$ V, $V_{OUT} = -2.0$ V	1.85 mA Max.
		UDN-2957A	$V_{IN} = 2.4$ V, $V_{OUT} = -2.0$ V	$675\,\mu$A Max.
			$V_{IN} = 3.85$ V, $V_{OUT} = -2.0$ V	1.40 mA Max.
	$I_{IN(OFF)}$	ALL	$I_{OUT} = -500\,\mu$A, $T_A = +70°C$	$50\,\mu$A Min.
Output Source Current	I_{OUT}	UDN-2956A	$V_{IN} = 5.0$ V, $V_{OUT} = -2.0$ V	-125 mA Min.
			$V_{IN} = 6.0$ V, $V_{OUT} = -2.0$ V	-200 mA Min.
			$V_{IN} = 7.0$ V, $V_{OUT} = -2.0$ V	-250 mA Min.
			$V_{IN} = 8.0$ V, $V_{OUT} = -2.0$ V	-300 mA Min.
			$V_{IN} = 9.0$ V, $V_{OUT} = -2.0$ V	-350 mA Min.
		UDN-2957A	$V_{IN} = 2.4$ V, $V_{OUT} = -2.0$ V	-125 mA Min.
			$V_{IN} = 2.7$ V, $V_{OUT} = -2.0$ V	-200 mA Min.
			$V_{IN} = 3.0$ V, $V_{OUT} = -2.0$ V	-250 mA Min.
			$V_{IN} = 3.3$ V, $V_{OUT} = -2.0$ V	-300 mA Min.
			$V_{IN} = 3.6$ V, $V_{OUT} = -2.0$ V	-350 mA Min.
Output Sustaining Voltage	$V_{CE(SUS)}$	UDN-2956A	$V_{IN} = 0.4$ V, $I_{OUT} = -25$ mA	50 V Min.
		UDN-2957A	$V_{IN} = 0.4$ V, $I_{OUT} = -25$ mA	50 V Min.
Clamp Diode Leakage Current	I_R	ALL	$V_R = 80$ V	$50\,\mu$A Max.
Clamp Diode Forward Voltage	V_F	ALL	$I_F = 350$ mA	2.0 V Max.
Turn-On Delay	t_{ON}	ALL	0.5 E_{in} to 0.5 E_{out}, $R_L = 400\,\Omega$ $C_T = 25$ pF	$4.0\,\mu$s Max.
Turn-Off Delay	t_{OFF}	ALL	0.5 E_{in} to 0.5 E_{out}, $R_L = 400\,\Omega$ $C_T = 25$ pF	$10\,\mu$s Max.

INPUT CURRENT
AS A FUNCTION OF INPUT VOLTAGE

3

UDN-2956A

MAX

TYP

INPUT CURRENT IN AMPERES

INPUT VOLTAGE IN VOLTS   Dwg. No. A-11,060

UDN-2957A

MAX

TYP

INPUT CURRENT IN AMPERES

INPUT VOLTAGE IN VOLTS   Dwg. No. A-11,061

ALLOWABLE PEAK OUTPUT CURRENT
AS A FUNCTION OF DUTY CYCLE

ALLOWABLE PEAK OUTPUT CURRENT IN mA AT 50°C

ABSOLUTE MAXIMUM CURRENT

-500
-400
-300
-200
-100
0

NUMBER OF OUTPUTS
CONDUCTING SIMULTANEOUSLY

10   20   30   40   50   60   70   80   90   100
PER CENT DUTY CYCLE

Dwg. No. A-11,062

ALLOWABLE PEAK OUTPUT CURRENT IN mA AT 70°C

ABSOLUTE MAXIMUM CURRENT

-500
-400
-300
-200
-100
0

NUMBER OF OUTPUTS
CONDUCTING SIMULTANEOUSLY

10   20   30   40   50   60   70   80   90   100
PER CENT DUTY CYCLE

Dwg. No. A-11,063

ONE OF FIVE DRIVERS

INPUT

R = 10.5 kΩ for UDN-2956A
R = 2.5 kΩ for UDN-2957A

R

ENABLE ①—⋀⋀⋀—

GROUND ⑦

7.5 K

2.4 K

OUTPUT

SUBSTRATE ⑧

SUB

Dwg. No. A-10,241D

3—92

UDN-2975W AND UDN-2976W
DUAL 4A SOLENOID DRIVERS

FEATURES

- 5 A Peak Output
- TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Output Voltage to 60 V
- Single-Ended or Split Supply
- Adjustable Short-Circuit Protection
- Internal Clamp Diodes
- Plastic SIP With Heat-Sink Tab

Dwg. No. A-12,105

C URRENT CONTROL for operation of a pair of print solenoids is provided by both Type UDN-2975W and UDN-2976W. Each IC's dual driver sections operate directly from the printer control line. The two devices differ only in output-voltage ratings. They can be used at currents of up to 4 A.

Type UDN-2975W is rated at 50 V. Type UDN-2976W is rated at 60 V or ±30 V. Inputs are compatible with most TTL, DTL, LSTTL, and 5 V to 15 V CMOS and PMOS logic.

Current is controlled by a current-sensing latch method that uses only one external sensing resistor for each driver. The load current is compared with the reference voltage and, at the level fixed by the system designer ($V_{REF}/10 = I_{LOAD} \times R_{SENSE}$), a latch is set, shutting OFF one of the output transistors. The internal flyback diode then maintains the flux without further input from the power supply, resulting in maximum efficiency. The latch is reset by pulling the input high.

For the maximum in power-handling capability, the integrated circuits are supplied in 12-pin single in-line power tab packages. For proper operation, an external heat sink is required. The tab is at V_{EE} potential and must be insulated from ground when Type UDN-2976W is used with a split supply.
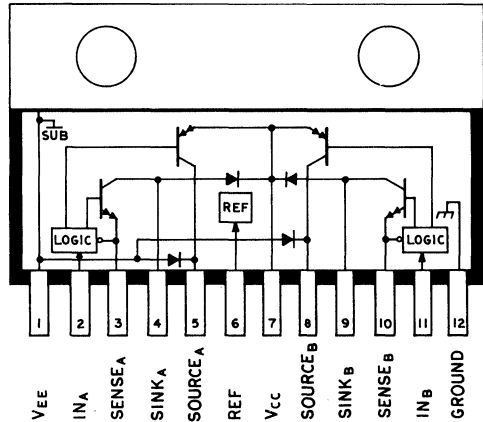
ABSOLUTE MAXIMUM RATINGS
at $T_{TAB} = +70°C$

Supply Voltage, V_{CC} (Ref. V_{EE}, UDN-2975W) . . . . 50 V

(Ref. V_{EE}, UDN-2976W) . . . . 60 V

V_{EE} (Ref. GND, UDN-2975W) . . . . 0 V

(Ref. GND, UDN-2976W) . . . . −30 V

Peak Output Current, I_{OUT} . . . . 5 A

Input Voltage, V_{IN} . . . . 7 V

Reference Voltage, V_{REF} . . . . 5 V

Package Power Dissipation, P_D . . . . See Graph

Operating Temperature Range, T_A . . . . −20°C to +85°C

Storage Temperature Range, T_S . . . . −55°C to +150°C

FUNCTIONAL BLOCK DIAGRAM
(ONE OF TWO DRIVERS)
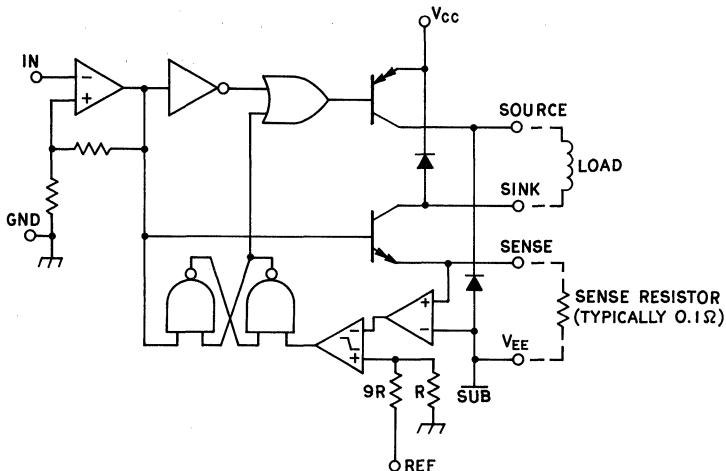
Dwg. No. A-12,106A

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF TEMPERATURE
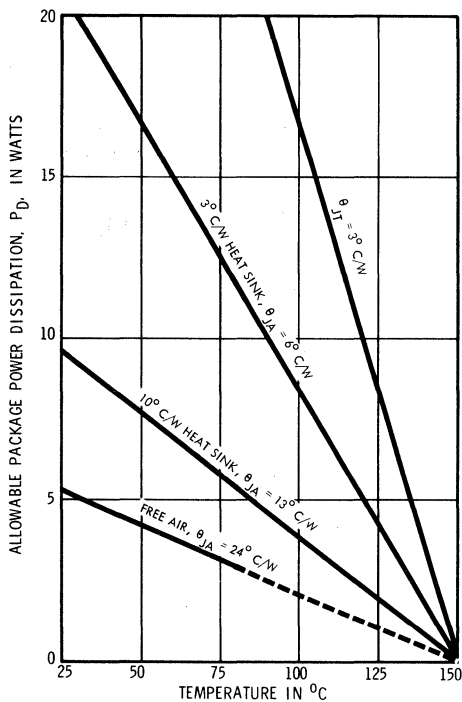
Dwg. No. A-11,794

To maintain isolation between integrated circuit components and to provide for normal transistor operation, the substrate (pin 1) must be connected to the most negative point in the external circuit.

TRUTH TABLE

V_{IN}	V_{SENSE}	Source Driver	Sink Driver	Function
High	NA	Off	Off	Off
Low	$<V_{REF}/10$	On	On	On
Low	$>V_{REF}/10$	Off	On	Flyback

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $T_{TAB} \leq +70°C$, $V_{CC} = 45\ V$ (UDN-2975W) or 55 V (UDN-2976W), $V_{EE} = V_{SENSE} = 0\ V$ (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Drivers						
Output Leakage Current	I_{CEX}	UDN-2975W	$V_{IN} = 2.4\ V$, $V_{CC} = 50\ V$, $V_{SOURCE} = 0\ V$	—	100	μA
			$V_{IN} = 2.4\ V$, $V_{SINK} = V_{CC} = 50\ V$	—	100	μA
		UDN-2976W	$V_{IN} = 2.4\ V$, $V_{CC} = 60\ V$, $V_{SOURCE} = 0\ V$	—	100	μA
			$V_{IN} = 2.4\ V$, $V_{SINK} = V_{CC} = 60\ V$	—	100	μA
Output Saturation Voltage	$V_{CE(SAT)}$	Both	Source Drivers, $I_{LOAD} = 4\ A$	—	3.5	V
			Sink Drivers, $I_{LOAD} = 4\ A$	—	2.5	V
Output Sustaining Voltage (Source drivers only)	$V_{CE(sus)}$	UDN-2975W	$I_{LOAD} = 4\ A$, $L = 3.5\ mH$	50	—	V
		UDN-2976W	$I_{LOAD} = 4\ A$, $L = 3.5\ mH$	60	—	V
Clamp Diode Forward Voltage	V_F	Both	$I_F = 4\ A$	—	2.0	V
Output Rise Time	t_r	Both	$I_{LOAD} = 4\ A$, 10% to 90%, Resistive Load	—	2.0	μs
Output Fall Time	t_f	Both	$I_{LOAD} = 4\ A$, 90% to 10%, Resistive Load	—	2.0	μs
Control Logic						
Logic Input Voltage	$V_{IN(1)}$	Both		2.0	—	V
	$V_{IN(0)}$	Both	See Notes	—	0.5	V
Logic Input Current	$I_{IN(1)}$	Both	$V_{IN} = 2.4\ V$	—	20	μA
	$I_{IN(0)}$	Both	$V_{IN} = 0.4\ V$	—	-20	μA
	$I_{REF(1)}$	Both	$V_{REF} = 6.0\ V$	—	20	μA
Reference/Sense Ratio	—	Both	$V_{REF} = 2.0$ to $5.0\ V$	9.5	10.5	—
Supply Current	I_{CC}	Both	Outputs Open	—	25	mA
	I_{EE}	Both	Outputs Open	—	-20	mA
Propagation Delay Time	t_{pd}	Both	50% V_{in} to 50% V_{out}, Resistive Load	—	3.0	μs
			100% V_{sense} to 50% V_{out}*, Resistive Load	—	3.0	μs
Minimum Reset Pulse Width	t_{in}	Both		—	1.0	μs

*Where $V_{sence} = V_{REF}/10.5$
NOTES: Negative current is defined as coming out of (sourcing) the specific device pin.
For improved noise immunity, hysteresis insures $V_{IN(0)}$ of 0.8 V max. after V_{IN} is 0.5 V or less.

3

SERIES UDN-2980A
HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- 500 mA Output Source Current Capability
- Transient-Protected Outputs
- Output Breakdown Voltage to 80 V

DWG. NO. A-10.243

R ECOMMENDED for applications requiring sep-
arate logic and load grounds, load supply volt-
age to +80 V, and load currents to 500 mA, Series
UDN-2980A source drivers are used as interfaces
between standard low-power digital logic and relays,
solenoids, stepping motors, and LEDs.

Under normal operating conditions, these devices
will sustain 120 mA continuously for each of the
eight outputs at an ambient temperature of +50°C
and a supply of +15 V. All devices in this series
incorporate input current limiting resistors and out-
put transient suppression diodes.

Type UDN-2981A and UDN-2983A drivers are
for use with +5 V logic systems — TTL, Schottky
TTL, DTL, and 5 V CMOS. Type UDN-2982A and
UDN-2984A drivers are intended for MOS interface
(PMOS and CMOS) operating from supply voltages

of 6 to 16 V. Types UDN-2981A and UDN-2982A
will sustain a maximum output OFF voltage of
+50 V, while Types UDN-2983A and UDN-2984A
will sustain an output voltage of +80 V. In all cases,
the output is switched ON by an active high input
level.

Series UDN-2980A high-voltage, high-current
source drivers are supplied in 18-lead dual in-line
packages. On special order, hermetically-sealed ver-
sions of these devices (with reduced package power
dissipation capability) can also be furnished.
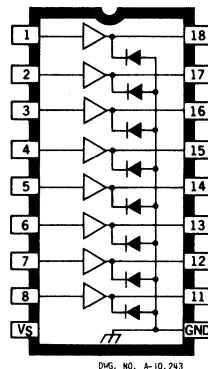
ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature

Output Voltage Range, V_{CE} (UDN-2981A & UDN-2982A) . . . . +5 V to +50 V

(UDN-2983A & UDN-2984A) . . . . +35 V to +80 V

Input Voltage, V_{IN} (UDN-2981A & UDN-2983A) . . . . +15 V

(UDN-2982A & UDN-2984A) . . . . +30 V

Output Current, I_{OUT} . . . . −500 mA

Power Dissipation, P_D (any one driver) . . . . 1.1 W

(total package) . . . . 2.2 W*

Operating Temperature Range, T_A . . . . −20°C to +85°C

Storage Temperature Range, T_S . . . . −55°C to +150°C

*Derate at the rate of 18 mW/°C above +25°C.

ONE OF EIGHT DRIVERS
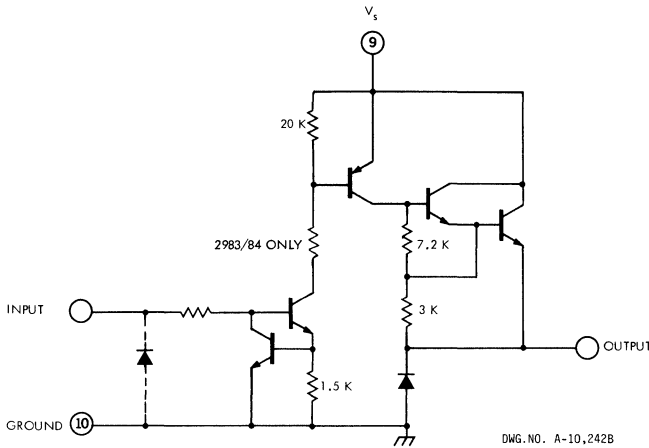
POWER DISSIPATION
AS A FUNCTION OF AMBIENT TEMPERATURE
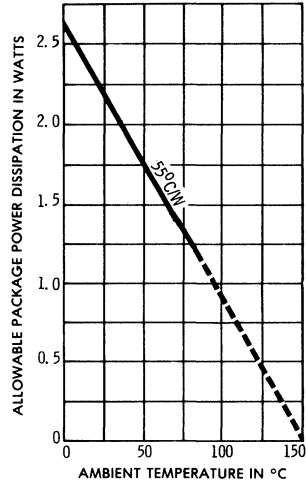
3

DWG.NO. A-10,242B

Dwg. No. A-11,112A

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Test Fig.	Limit Min.	Limit Typ.	Limit Max.	Units
Output Leakage Current	I_{CEX}	UDN-2981/82A	$V_{IN} = 0.4$ V*, $V_S = 50$ V, $T_A = +70°C$	1	—	—	200	μA
		UDN-2983/84A	$V_{IN} = 0.4$ V*, $V_S = 80$ V, $T_A = +70°C$	1	—	—	200	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	$V_{IN} = 2.4$ V, $I_{OUT} = -100$ mA	2	—	1.6	1.8	V
			$V_{IN} = 2.4$ V, $I_{OUT} = -225$ mA	2	—	1.7	1.9	V
			$V_{IN} = 2.4$ V, $I_{OUT} = -350$ mA	2	—	1.8	2.0	V
Input Current	$I_{IN(ON)}$	UDN-2981/83A	$V_{IN} = 2.4$ V	3	—	140	200	μA
			$V_{IN} = 3.85$ V	3	—	310	450	μA
		UDN-2982/84A	$V_{IN} = 2.4$ V	3	—	140	200	μA
			$V_{IN} = 12$ V	3	—	1.25	1.93	mA
Output Source Current	I_{OUT}	UDN-2981/83A	$V_{IN} = 2.4$ V, $V_{CE} = 2.0$ V	2	-350	—	—	mA
		UDN-2982/84A	$V_{IN} = 2.4$ V, $V_{CE} = 2.0$ V	2	-350	—	—	mA
Supply Current (Outputs Open)	I_S	UDN-2981/82A	$V_{IN} = 2.4$ V*, $V_S = 50$ V	4	—	—	10	mA
		UDN-2983/84A	$V_{IN} = 2.4$ V*, $V_S = 80$ V	4	—	—	10	mA
Clamp Diode Leakage Current	I_R	UDN-2981/82A	$V_R = 50$ V, $V_{IN} = 0.4$ V*	5	—	—	50	μA
		UDN-2983/84A	$V_R = 80$ V, $V_{IN} = 0.4$ V*	5	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All	$I_F = 350$ mA	6	—	1.5	2.0	V
Turn-On Delay	t_{ON}	All	0.5 E_{IN} to 0.5 E_{OUT}, $R_L = 100\Omega$, $V_S = 35$ V	—	—	1.0	2.0	μs
Turn-Off Delay	t_{OFF}	All	0.5 E_{IN} to 0.5 E_{OUT}, $R_L = 100\Omega$, $V_S = 35$ V	—	—	5.0	10	μs

*All Inputs Simultaneously

TEST FIGURES
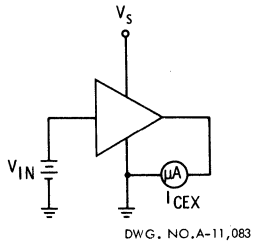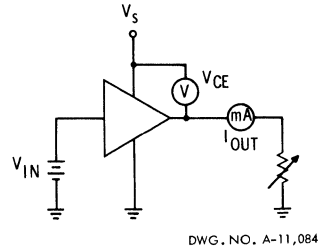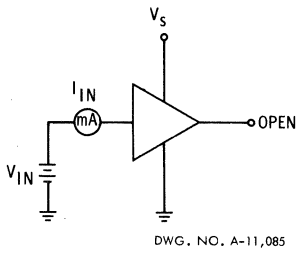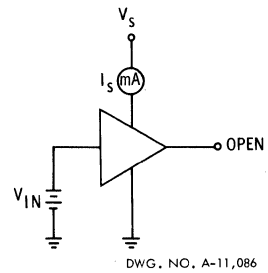
DWG. NO. A-11,083

Figure 1

DWG. NO. A-11,084

Figure 2

DWG. NO. A-11,085

Figure 3

DWG. NO. A-11,086

Figure 4

DWG. NO. A-11,087

Figure 5

DWG. NO. A-11,088
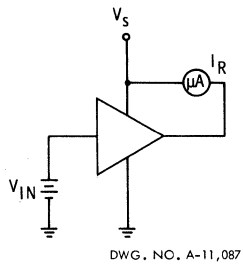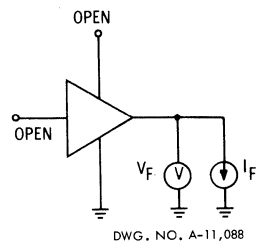
Figure 6

ALLOWABLE PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE
TYPE UDN-2981A/82A

Dwg. No. A-11,107B
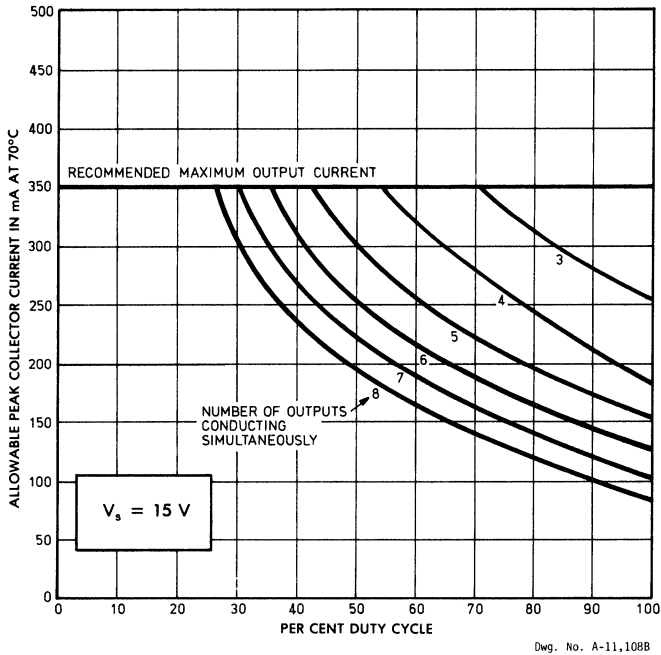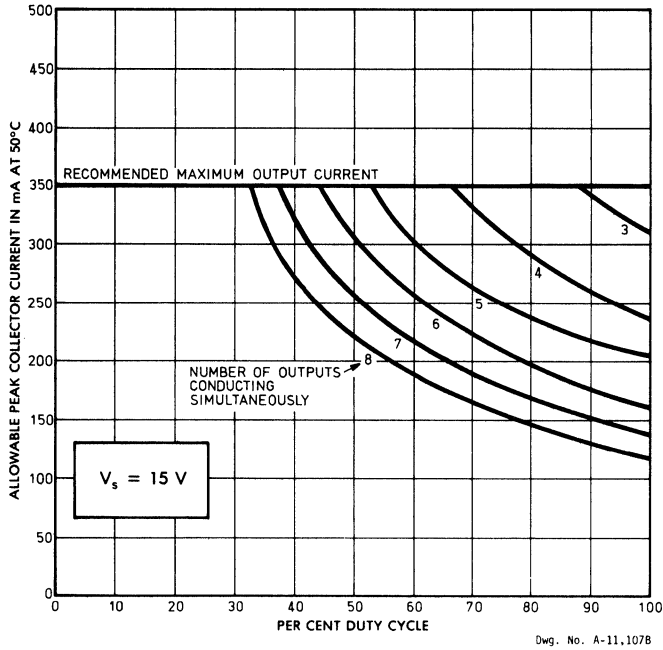
Dwg. No. A-11,108B

ALLOWABLE PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE
SERIES UDN-2980A

Dwg. No. A-11,106B
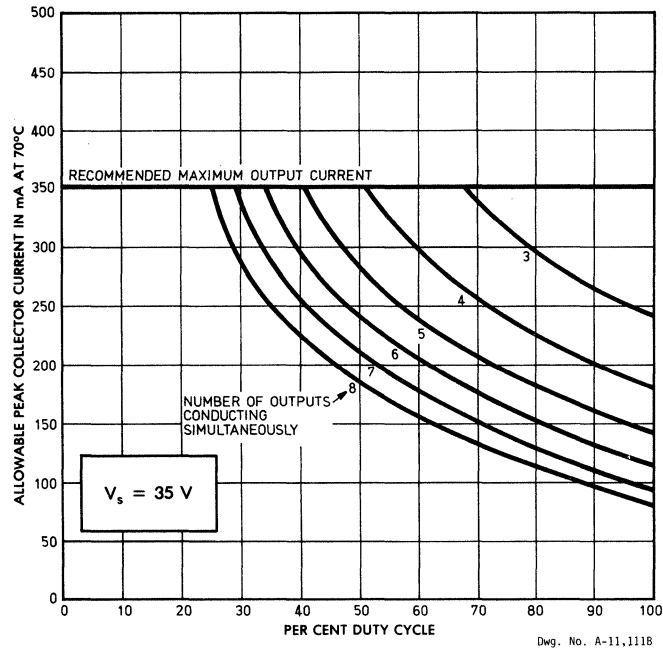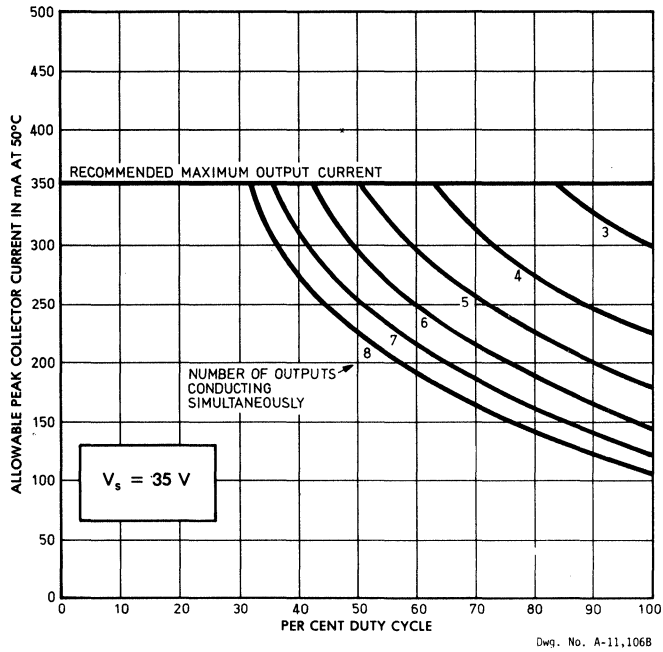
Dwg. No. A-11,111B

ALLOWABLE PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE
TYPES UDN-2983A/84A
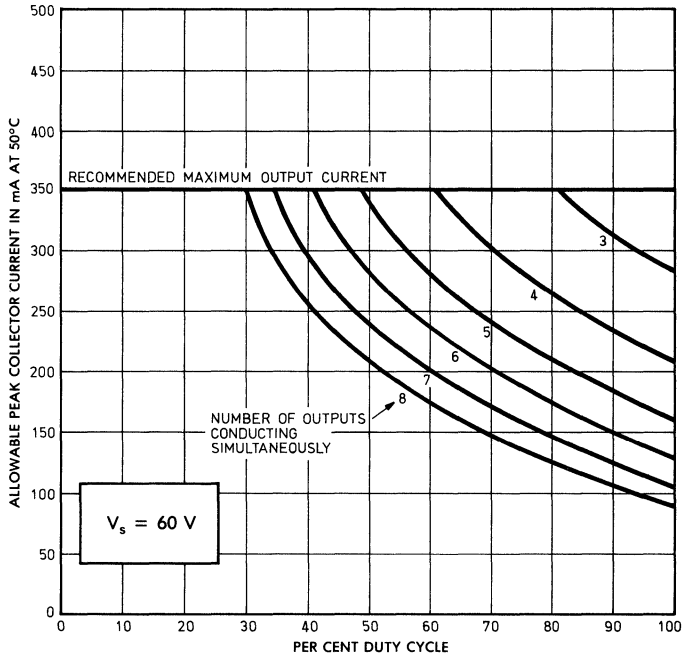
Dwg. No. A-11,109B
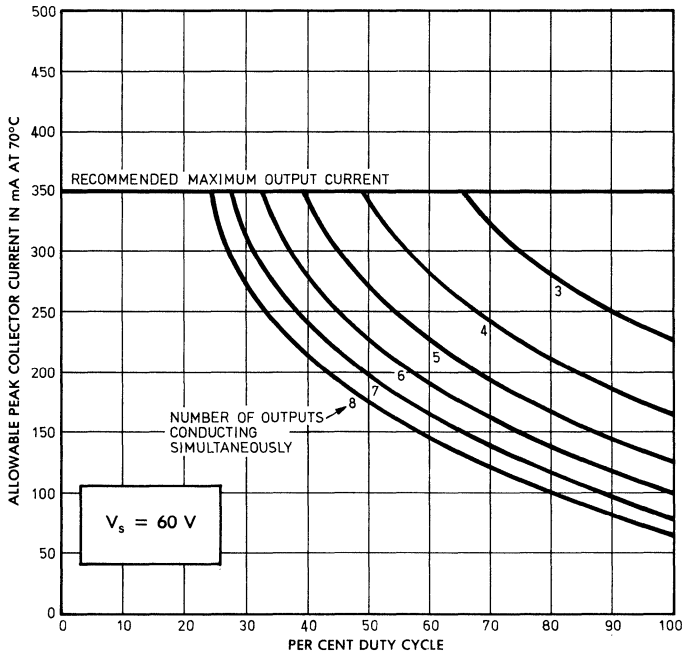
Dwg. No. A-11,110B

INPUT CURRENT
AS A FUNCTION OF INPUT VOLTAGE

Dwg.No. A-11,115A
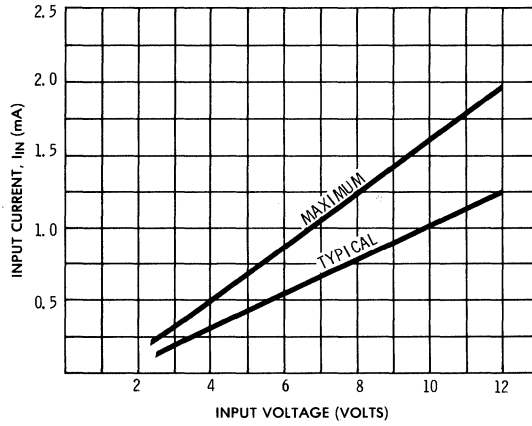
TYPICAL ELECTROSENSITIVE PRINTER APPLICATION

Dwg. No. A-11,113
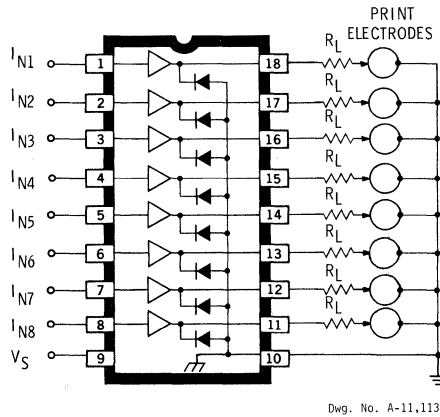
TYPICAL VALUES: V_S = 50 V
I_{OUT} = 200-300 mA

SERIES UDN-3600M
DUAL 2-INPUT PERIPHERAL AND POWER DRIVERS

FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Standoff Voltage of 80 V
- Pin-for-Pin Replacement for Series LM3600N
- Pin-for-Pin Replacement for SN75451BP through SN75454BP and 75461 through 75464

Description

THESE MINI-DIP dual 2-input peripheral power drivers are bipolar monolithic integrated circuits with AND, NAND, OR, or NOR logic gates and high-current switching transistors on the same chip. The two output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, these drivers will withstand at least 80 V.

Applications

Series UDN-3600M dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, heaters, and other non-inductive loads of up to 600 mA (both drivers in parallel).

With appropriate external-diode transient-suppression, Series UDN-3600M drivers can also be used with inductive loads such as relays, solenoids, and stepping motors.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 7.0 V
Input Voltage, V_{IN} .... 30 V
Output Off-State Voltage, V_{OFF} .... 80 V
Output On-State Sink Current, I_{ON} .... 600 mA
Power Dissipation, P_D .... 1.5 W
    Each Driver .... 0.8 W
    Derating Factor Above T_A = 25°C .... 12.5 mW/°C or 80°C/W
Operating Free-Air Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+85	°C
Current into any output (ON state)			300	mA

INPUT PULSE CHARACTERISTICS

$V_{in(0)} = 0V$	$t_f = 7ns$	$t_p = 1\mu s$
$V_{in(1)} = 3.5V$	$t_r = 14ns$	PRR = 500kHz

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions				Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current	$I_{in(0)}$		MAX	0.4 V	30 V			50	100	μA	2
"1" Input Current	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

(Test Conditions columns: Temp., V_{CC}, Driven Input, Other Input, Output; Limits columns: Min., Typ., Max.)

SWITCHING CHARACTERISTICS at $V_{CC} = 5.0$ V, $T_A = 25°C$

Characteristic	Symbol	Test Conditions	Limits			Units	Notes
			Min.	Typ.	Max.		
Turn-on Delay Time	t_{pdo}	$V_S = 70$ V, $R_L = 465\,\Omega$ (10 Watts) $C_L = 15$ pF		200	500	ns	3
Turn-off Delay Time	t_{pd1}	$V_S = 70$ V, $R_L = 465\,\Omega$ (10 Watts) $C_L = 15$ pF		300	750	ns	3

NOTES:
1. Typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

Type UDN-3611M Dual AND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	100 mA		0.25	0.4	V	
			MIN	0.8 V	V_{CC}	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			35	49	mA	1, 2

Type UDN-3612M Dual NAND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	100 mA		0.25	0.4	V	
			MIN	2.0 V	2.0 V	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	14	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	53	mA	1, 2
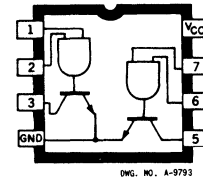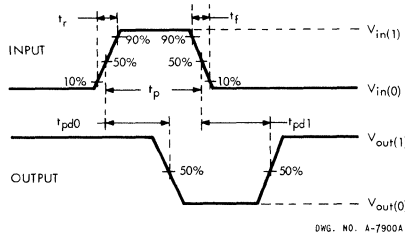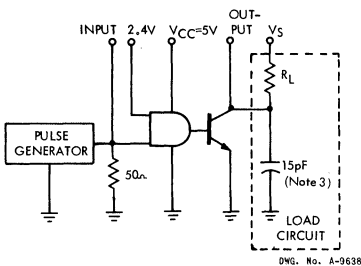
NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

Type UDN-3613M Dual OR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions				Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	100 mA		0.25	0.4	V	
			MIN	0.8 V	0.8 V	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			36	50	mA	1, 2

DWG. NO. A-7877B

DWG. No. A-7628C

DWG. NO. A-9795
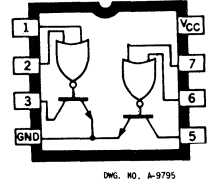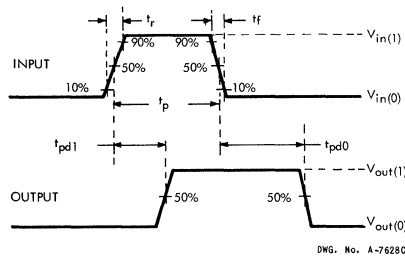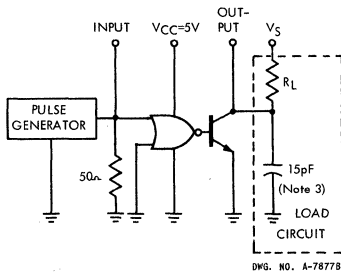
Type UDN-3614M Dual NOR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions				Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	100 mA		0.25	0.4	V	
			MIN	2.0 V	0 V	300 mA		0.5	0.7	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	50	mA	1, 2

DWG. NO. A-9942

DWG. NO. A-7900A

DWG. NO. A-9794
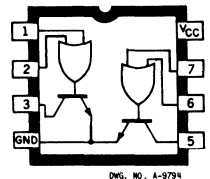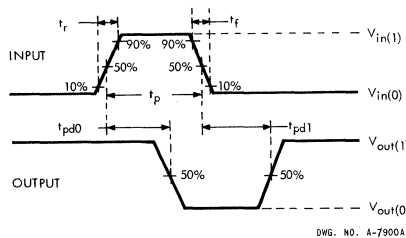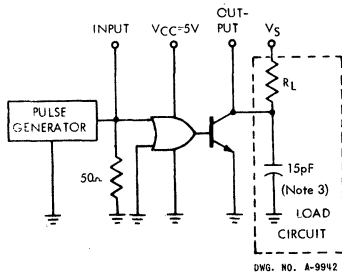
NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

SERIES UDN-5700A
QUAD 2-INPUT PERIPHERAL AND POWER DRIVERS
—Transient-Protected Outputs

3

FEATURES:

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Standoff Voltage of 80 V

Description

THESE 16-LEAD QUAD 2-input peripheral and power drivers are bipolar monolithic integrated circuits containing AND, NAND, OR, or NOR logic gates, high-current switching transistors, and transient-suppression diodes on the same chip. The four output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, these drivers will withstand at least 80 V.

Applications

Series UDN-5700A quad drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

The integral transient-suppression diodes allow their use with inductive loads such as relays, solenoids, or stepping motors without the need of discrete diodes. For non-inductive loads, the diode-common bus can be used for a convenient lamp test.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 7.0 V
Input Voltage, V_{IN} .... 30 V
Output Off-State Voltage, V_{OFF} .... 80 V
Output On-State Sink Current, I_{ON} .... 600 mA
Suppression Diode Off-State Voltage, V_{OFF} .... 80 V
Suppression Diode On-State Current, I_{ON} .... 600 mA
Power Dissipation, P_D .... 2.0 W
    Each Driver .... 0.8 W
    Derating Factor Above 25°C .... 16.7 mW/°C or 60°C/W
Operating Free-Air Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC}):	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+85	°C
Current into any output (ON state)			300	mA

INPUT PULSE CHARACTERISTICS

$V_{in(0)} = 0V$	$t_f = 7ns$	$t_p = 1\mu s$
$V_{in(1)} = 3.5V$	$t_r = 14ns$	PRR = 500kHz

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions				Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current	$I_{in(0)}$		MAX	0.4 V	30 V			−50	−100	μA	2
"1" Input Current	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS at $V_{CC} = 5.0$ V, $T_A = 25°C$

Characteristic	Symbol	Test Conditions	Limits				Notes
			Min.	Typ.	Max.	Units	Notes
Turn-on Delay Time	t_{pd0}	$V_S = 70$ V, $R_L = 465 \, \Omega$ (10 Watts) $C_L = 15$ pF		200	500	ns	3
Turn-off Delay Time	t_{pd1}	$V_S = 70$ V, $R_L = 465 \, \Omega$ (10 Watts) $C_L = 15$ pF		300	750	ns	3

NOTES:
1. Typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

Type UDN-5703A Quad OR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	150 mA		0.35	0.5	V	
			MIN	0.8 V	0.8 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			16	25	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			72	100	mA	1, 2

Type UDN-5706A Quad AND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	150 mA		0.35	0.5	V	
			MIN	0.8 V	V_{CC}	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			16	24	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			70	98	mA	1, 2

NOTES:
1. Typical values are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at $I_f = 300$ mA.
5. Capacitance values specified include probe and test fixture capacitance.

Type UDN-5707A Quad NAND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Output Reverse Current	I_{off}	MIN	0.8 V	V_{CC}	80 V			100	μA	
		OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}	MIN	2.0 V	2.0 V	150 mA		0.35	0.5	V	
		MIN	2.0 V	2.0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			80	106	mA	1, 2

DWG. NO. A-7899A

DWG. NO. A-7900A

DWG. NO. A-9867

Type UDN-5733A Quad NOR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Output Reverse Current	I_{off}	MIN	0.8 V	0.8 V	80 V			100	μA	
		OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}	MIN	2.0 V	0 V	150 mA		0.35	0.5	V	
		MIN	2.0 V	0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			80	100	mA	1, 2

DWG. NO. A-9135A

DWG. NO. A-7900A

DWG. NO. A-9868

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at V_R = $V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

SERIES UDN-5700M
DUAL PERIPHERAL AND POWER DRIVERS
—Transient-Protected Outputs

3

FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 300 mA Continuous Output Current
- Standoff Voltage of 80 V

Description

THESE MINI-DIP dual peripheral and power drivers are bipolar mono-lithic integrated circuits incorporating AND, NAND, OR, or NOR logic gates, high-current switching transistors, and transient-suppression diodes on the same chip. The two output transistors are capable of simultaneously sinking 300 mA continuously at ambient temperatures of up to +70°C. In the OFF state, these drivers will withstand at least 80 V.

Applications

Series UDN-5700M dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters with a load current of up to 600 mA.

The integral transientsuppression diodes allow the use of these drivers with inductive loads such as relays, solenoids, or stepping motors without the need for discrete diodes. When not required for transient suppression, the diode-common bus can be used for the "lamp test" function.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 7.0 V
Input Voltage, V_{IN} . . . . 30 V
Output Off-State Voltage, V_{OFF} . . . . 80 V
Output On-State Sink Current, I_{ON} . . . . 600 mA
Suppression Diode Off-State Voltage, V_{OFF} . . . . 80 V
Suppression Diode On-State Current, I_{ON} . . . . 600 mA
Power Dissipation at T_A = +25°C, P_D . . . . 1.5 W
    Each Driver . . . . 0.8 W
    Derating Factor . . . . 12.5 mW/°C or 80°C/W
Operating Free-Air Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −55°C to +150°C

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC}):	4.75	5.0	5.25	V
Operating Temperature Range	0	+25	+85	°C
Current into any output (ON state)			300	mA

INPUT PULSE CHARACTERISTICS

$V_{in(0)} = 0V$	$t_f = 7ns$	$t_p = 1\mu s$
$V_{in(1)} = 3.5V$	$t_r = 14ns$	$PRR = 500kHz$

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current at all Inputs except Strobe	$I_{in(0)}$		MAX	0.4 V	30 V			−50	−100	μA	2
"0" Input Current at Strobe	$I_{in(0)}$		MAX	0.4 V	30 V			−100	−200	μA	
"1" Input Current at all Inputs except Strobe	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
"1" Input Current at Strobe	$I_{in(1)}$		MAX	30 V	0 V				20	μA	
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS at $V_{CC} = 5.0 V$, $T_A = 25°C$

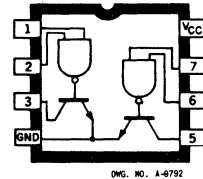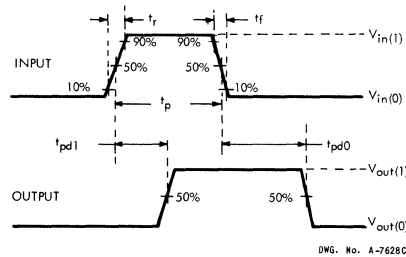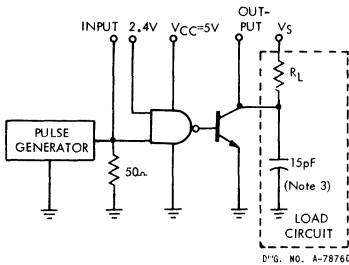| Characteristic	Symbol	Test Conditions	Limits			Units	Notes
			Min.	Typ.	Max.		
Turn-on Delay Time	t_{pd0}	$V_S = 70 V$, $R_L = 465\,\Omega$ (10 Watts) $C_L = 15\ pF$		200	500	ns	3
Turn-off Delay Time	t_{pd1}	$V_S = 70 V$, $R_L = 465\,\Omega$ (10 Watts) $C_L = 15\ pF$		300	750	ns	3

NOTES:
1. Typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

Type UDN-5711M Dual AND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	150 mA		0.35	0.5	V	
			MIN	0.8 V	V_{CC}	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			35	49	mA	1, 2

Type UDN-5712M Dual NAND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	150 mA		0.35	0.5	V	
			MIN	2.0 V	2.0 V	300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	53	mA	1, 2

NOTES:
1. Typical values are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at $I_f = 300$ mA.
5. Capacitance values specified include probe and test fixture capacitance.

Type UDN-5713M Dual OR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}	MIN	2.0 V	0 V		80 V			100	μA	
		OPEN	2.0 V	0 V		80 V			100	μA	
"0" Output Voltage	V_{on}	MIN	0.8 V	0.8 V		150 mA		0.35	0.5	V	
		MIN	0.8 V	0.8 V		300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			36	50	mA	1, 2

Type UDN-5714M Dual NOR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}	MIN	0.8 V	0.8 V		80 V			100	μA	
		OPEN	0.8 V	0.8 V		80 V			100	μA	
"0" Output Voltage	V_{on}	MIN	2.0 V	0 V		150 mA		0.35	0.5	V	
		MIN	2.0 V	0 V		300 mA		0.5	0.7	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	50	mA	1, 2

NOTES:
1. Typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at $I_f = 300$ mA.
5. Capacitance values specified include probe and test fixture capacitance.

UDN-5722M
DUAL PERIPHERAL AND POWER DRIVER
— Transient-Protected Outputs

FEATURES

- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- 350 mA Continuous Output Current
- 70 V Output Standoff Voltage
- Low Supply-Current Requirement
- Direct Replacement For SN75477

Dwg. No. A-9790A
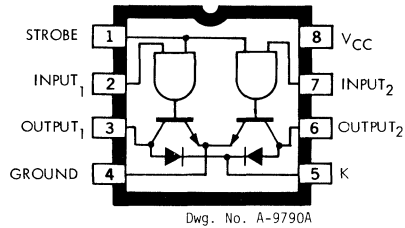
3

THIS PERIPHERAL AND POWER DRIVER combines dual AND logic gates, high-current switching transistors, and transient-suppression diodes in a bipolar monolithic integrated circuit that meets interface requirements beyond the capabilities of standard logic buffers.

The two output transistors are capable of simultaneously sinking 350mA continuously at ambient temperatures of up to +85°C. In the OFF state, the drivers will withstand at least 70 V.

Type UDN-5722M is supplied in a miniature 8-pin dual in-line plastic package with a copper lead frame for enhanced package power dissipation ratings.

The dual driver is ideally suited for interface between low-level logic and high-current inductive loads. Internal transient-suppression diodes allow the use of this driver with stepping motors, relays, or solenoids. Additional non-inductive applications include driving peripheral loads such as light-emitting diodes, memories, heaters, and incandescent lamps with peak load currents of up to 600 mA. When not required for transient suppression, the diode common bus can be used to perform the ''lamp test'' function. The outputs may be paralleled for higher load-current capability.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 15 V
Input Voltage, V_{IN} .... 30 V
Output Off-State Voltage, V_{OFF} .... 70 V
Output On-State Sink Current, I_{ON} .... 600 mA
Suppression Diode Off-State Voltage, V_{OFF} .... 70 V
Suppression Diode On-State Current, I_{ON} .... 600 mA
Power Dissipation at T_A = +25°C, P_D .... 1.5 W*
Operating Free-Air Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −55°C to +150°C

*Derate at the rate of 12.5 mW/°C above T_A = +25°C

RECOMMENDED OPERATING CONDITIONS

Operating Condition	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.75	—	12.6	V
Operating Temperature Range	0	+25	+85	°C
Current into any output (ON state)	—	—	350	mA

ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Input Voltage	$V_{IN(1)}$	—	Min.	—	—	—	2.0	—	—	V	—
"0" Input Voltage	$V_{IN(0)}$	—	Min.	—	—	—	—	—	0.8	V	—
"0" Input Current at All Inputs Except Strobe	$I_{IN(0)}$	—	Max.	0.4 V	30 V	—	—	−5.0	−10	μA	4
"0" Input Current at Strobe	$I_{IN(0)}$	—	Max.	0.4 V	30 V	—	—	−10	−20	μA	—
"1" Input Current at All Inputs Except Strobe	$I_{IN(1)}$	—	Max.	30 V	0 V	—	—	5.0	10	μA	4
"1" Input Current at Strobe	$I_{IN(1)}$	—	Max.	30 V	0 V	—	—	10	20	μA	—
Input Clamp Voltage	V_{CLAMP}	—	Min.	−12 mA	—	—	—	—	−1.5	V	—
"1" Output Reverse Current	I_{OFF}	—	Min.	0.8 V	V_{CC}	70 V	—	—	100	μA	—
		—	Open	0.8 V	V_{CC}	70 V	—	—	100	μA	—
"0" Output Voltage	V_{ON}	—	Min.	2.0 V	2.0 V	200 mA	—	0.4	0.6	V	—
		—	Min.	2.0 V	2.0 V	350 mA	—	0.6	0.8	V	—
Diode Leakage Current	I_R	Nom.	5.0	V_{CC}	V_{CC}	Open	—	—	200	μA	2
Diode Forward Voltage Drop	V_F	Nom.	5.0	0 V	0 V	—	—	1.5	1.75	V	3
"1" Level Supply Current	$I_{CC(1)}$	Nom.	5.25	0 V	0 V	—	—	1.0	3.0	mA	1
			12.6	0 V	0 V	—	—	2.6	5.0	mA	1
"0" Level Supply Current	$I_{CC(0)}$	Nom.	5.25	5.0 V	5.0 V	—	—	11	17	mA	1
			12.6	5.0 V	5.0 V	—	—	35	50	mA	1

NOTES:
1. Per package.
2. Diode leakage current measured at $V_R = V_{OFF(Min.)}$.
3. Diode forward voltage drop measured at $I_F = 300$ mA.
4. Each input tested separately.

SWITCHING TEST CIRCUIT

INPUT 2.4V V_{CC} OPEN OUT-PUT V_S

PULSE GENERATOR

50Ω

R_L

C_L

LOAD CIRCUIT

Dwg. No. A-11,746

3

SWITCHING CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 5.0$ V
Input-Pulse Characteristics

$V_{in(0)} = 0$ V	$t_f = 7$ ns	$t_p = 1\ \mu s$
$V_{in(1)} = 3.5$ V	$t_r = 14$ ns	PRR = 500kHz

Characteristic	Symbol	Test Conditions	Limits		Units	Notes
			Min.	Max.		
Turn-on Delay Time	$t_{pd(0)}$	$V_S = 30$ V, $R_L = 100\Omega$ (10 W) $C_L = 30$ pF	—	500	ns	1, 2
Turn-off Delay Time	$t_{pd(1)}$	$V_S = 30$ V, $R_L = 100\Omega$ (10 W) $C_L = 30$ pF	—	750	ns	1, 2

NOTES:
1. Capacitance values specified include probe and test fixture capacitance.
2. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.

INPUT/OUTPUT WAVEFORMS

t_r t_f

INPUT

90% 90%

50% 50%

10% 10%

t_P

$V_{in(1)}$

$V_{in(0)}$

t_{pd0} t_{pd1}

$V_{out(1)}$

OUTPUT

50% 50%

$V_{out(0)}$

DWG. NO. A-7900A
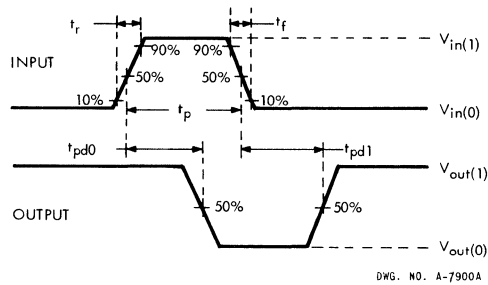
UDN-5732M AND UDN-5742M
DUAL PERIPHERAL AND POWER DRIVERS
—Transient-Protected Outputs

FEATURES

- DDL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Continuous Output Current to 600 mA
- 70 V Output Standoff Voltage

STROBE [1]   [8] V_{CC}
INPUT$_1$ [2]   [7] INPUT$_2$
OUTPUT$_1$ [3]   [6] OUTPUT$_2$
GROUND [4]   [5] K
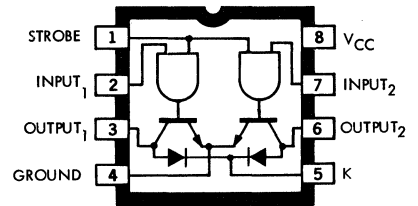
Dwg. No. A-9790A

INCORPORATING logic gates, high-current saturated output transistors, and transient-suppression diodes, Type UDN-5732M and UDN-5742M dual peripheral and power drivers meet interface requirements well beyond the capabilities of standard logic buffers.

The output transistors can each sink 425 mA continuously at ambient temperatures of up to +70°C. Reduced ambient temperatures or duty cycles permit increased load currents of up to 500 mA (UDN-5723M) or 600 mA (UDN-5742M) with miminum saturation voltages. In the OFF state, the drivers will withstand at least 70 V.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 7.0 V
Input Voltage, V_{IN} . . . . 30 V
Output OFF-State Voltage, V_{OFF} . . . . 70 V
Output ON-State Sink Current, I_{ON} (UDN-5732M) . . . . 600 mA
(UDN-5742M) . . . . 700 mA
Suppression Diode OFF-State Voltage, V_{OFF} . . . . 70 V
Suppression Diode ON-State Current, I_{ON} (UDN-5732M) . . . . 600 mA
(UDN-5742M) . . . . 700 mA
Allowable Package Power Dissipation, P_D . . . . 1.5 W*
Operating Free-Air Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −55°C to +150°C
*Derate at the rate of 12.5 mW/°C above T_A = +25°C.

RECOMMENDED OPERATING CONDITIONS

Operating Condition	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	4.75	5.00	5.25	V
Operating Temperature Range, T_A	0	+25	+85	°C
Output Sink Current, UDN-5732M	—	—	500	mA
Output Sink Current, UDN-5742M	—	—	600	mA

ELECTRICAL CHARACTERISTICS over recommended operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
"1" Input Voltage	$V_{IN(1)}$	—	Min.	—	—	—	2.0	—	—	V	—
"0" Input Voltage	$V_{IN(0)}$	—	Min.	—	—	—	—	—	0.8	V	—
"0" Input Current at All Inputs Except Strobe	$I_{IN(0)}$	—	Max.	0.4 V	30 V	—	—	−50	−100	μA	4
"0" Input Current at Strobe	$I_{IN(0)}$	—	Max.	0.4 V	30 V	—	—	−100	−200	μA	—
"1" Input Current at All Input Except Strobe	$I_{IN(1)}$	—	Max.	30 V	0 V	—	—	5.0	10	μA	4
"1" Input Current at Strobe	$I_{IN(1)}$	—	Max.	30 V	0 V	—	—	10	20	μA	
Input Clamp Voltage	V_{CLAMP}	—	Min.	−12 mA	—	—	—	—	−1.5	V	—
"1" Output Reverse Current	I_{OFF}	—	Min.	0.8 V	V_{CC}	70 V	—	—	100	μA	—
		—	Open	0.8 V	V_{CC}	70 V	—	—	100	μA	—
"0" Output Voltage	V_{ON}	—	Min.	2.0 V	2.0 V	300 mA	—	0.3	0.6	V	—
		—	Min.	2.0 V	2.0 V	500 mA	—	0.5	0.8	V	—
		—	Min.	2.0 V	2.0 V	600 mA	—	0.7	1.0	V	5
Diode Leakage Current	I_R	Nom.	5.0	V_{CC}	V_{CC}	Open	—	—	100	μA	2
Diode Forward Voltage Drop	V_F	Nom.	5.0	0 V	0 V	—	—	1.5	2.0	V	3
"1" Level Supply Current	$I_{CC(1)}$	Nom.	5.25	0 V	0 V	—	—	8.0	17	mA	1
"0" Level Supply Current	$I_{CC(0)}$	Nom.	5.25	5.0 V	5.0 V	—	—	50	75	mA	1

NOTES:
1. Per package.
2. Diode leakage current measured at $V_R = 70$ V.
3. Diode forward voltage drop measured at $I_F = 500$ mA (UDN-5732M) or 600 mA (UDN-5742M).
4. Each input tested separately.
5. Type UDN-5742M only.

SWITCHING TEST CIRCUIT

Dwg. No. A-11,746

SWITCHING CHARACTERISTICS at $T_A = +25°C$, $V_{cc} = 5.0$ V

Input-Pulse Characteristics

$V_{in(0)} = 0$ V	$t_f = 7$ ns	$t_p = 1$ μS
$V_{in(1)} = 3.5$ V	$t_r = 14$ ns	PRR $= 500$ kHz

Characteristic	Symbol	Test Conditions	Limits			Units	Notes
			Min.	Typ.	Max.		
Turn-on Delay Time	$t_{pd(0)}$	$V_S = 30$ V, $R_L = 100\Omega$ (10 W) $C_L = 15$ pF	—	200	500	ns	1, 2
Turn-off Delay Time	$t_{pd(1)}$	$V_S = 30$ V, $R_L = 100\Omega$ (10 W) $C_L = 15$ pF	—	300	750	ns	1, 2

NOTES:
  1. Capacitance values specified include probe and test fixture capacitance.
  2. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.

INPUT/OUTPUT WAVEFORMS

DWG. NO. A-7900A
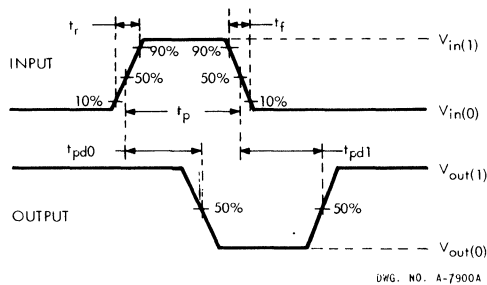
SERIES ULN-2000A
DARLINGTON TRANSISTOR ARRAYS*
—Description and Application

Introduction

The increased use of electronic circuits in systems formerly built with mechanical, electro-mechanical, or hydraulic components has resulted in systems becoming more precise, more reliable, generally less expensive, smaller, more efficient, and faster. Although the drive capabilities of monolithic integrated logic circuits are adequate for most information processing applications, there now exists a large and rapidly growing number of system applications where the current-carrying and/or voltage-sustaining capability of the integrated circuit logic is inadequate. Typically, these deficiencies arise when the logic must control such peripheral components as relays, solenoids, punches, stepping motors, and a variety of indicators (incandescent, LED, or gas discharge lamps and displays).

A very common solution to this output interface inadequacy has been the addition of discrete power transistors (or SCRs) and associated passive components to the logic output in order to obtain the necessary current and/or voltage capability. Although this provides a very satisfactory electrical solution, the large number of discrete components often required, high assembly labor costs, and space (packaging) limitations often mean additional problems and cost. A simple, and less expensive solution is the use of monolithic integrated circuits.

The Series ULN-2000A is comprised of four different high-voltage/high-current interface circuits. They are capable of controlling resistive, inductive, or tungsten filament loads of up to 125 watts and are compatible with all standard digital logic families (DTL, TTL, PMOS, and CMOS) without the need for additional discrete components.

High-Voltage and High-Current Capability

A large number of interface problems have been simplified by the Series ULN-2000A high-voltage, high-current Darlington transistor arrays. These devices are suitable for voltage, current, and gain levels beyond the limits of other monolithic buffers and arrays.

The four devices in the ULN-2000A series are all comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for use with inductive loads.

All devices have an output sink current capability of 500 mA although peak inrush currents to 600 mA are permissible, making them ideal for use with tungsten filament lamps. All of the outputs will sustain "OFF" voltages of at least 50 volts. Each individual Darlington circuit may therefore switch up to 25 watts (50 V at 500 mA).

A definite asset of monolithic device technology is the very fine match between adjacent outputs when used in parallel. Applications requiring a sink current beyond the capability of a single output can be accommodated by parallel outputs. Continuous operation of all outputs at the maximum rated current is not allowed because of power dissipation limitations imposed by the package. However, as illustrated in Figure 1, under certain conditions, the Series ULN-2000A Darlington arrays are capable of switching loads totaling more than 125 watts at an ambient temperature of +70°C.

*Examples and data in this application note applies equally to Series ULN-2800A Darlington arrays.

Figure 1

COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE AND NUMBER OF OUTPUTS
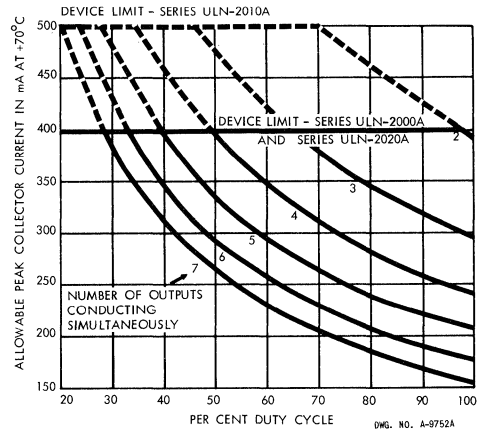
High-Power Capability

A primary limitation of many interface circuits is the power dissipation of the device package. Until recently, very little concern was expressed for monolithic integrated circuit power dissipation. Improvements in silicon device technology have brought about a growing number of monolithic circuits capable of power considerably in excess of present package technology.

The Series ULN-2000A is supplied in a 16-pin dual in-line plastic package with a copper lead frame. Shown in Figure 2 is a comparison of the allowable package power dissipation for the industry standard iron-nickel alloy (Kovar) lead frame and the Sprague copper lead frame used on these devices. As shown, at an ambient temperature of +70°C, the Kovar lead frame allows only 0.64 watts while the copper lead frame allows 1.33 watts. At +25°C the copper lead frame permits a package power dissipation of 2.0 watts!

Actual power dissipation in any application for the Series ULN-2000A devices is the sum of the individual driver power dissipations. In turn, the individual driver dissipation is the product of the collector-emitter saturation voltage, the collector current, and the duty cycle. The collector-emitter saturation voltage is dependent on the collector current and, to a lesser extent, operating temperature.
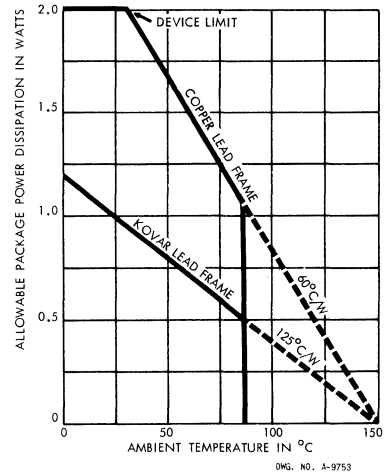
Figure 2

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

The Basic Darlington Array

The first, and basic array, in this series, is the Type ULN-2001A. This is a general-purpose version with input current limiting normally accomplished via the use of an appropriate discrete resistor connected in series with each input. It is also possible to utilize the intrinsic current limiting of many MOS outputs as shown in Figure 4; a typical P-channel characteristic.

The use of TTL in such a manner is not recommended due to the higher currents and resultant high level of package power dissipation. Outputs of most PMOS and CMOS circuits will not normally source currents of any significance due to their high source impedance.

COM

7.2K   3K

DWG. NO. A-9595
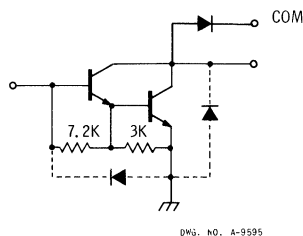
(each driver)

Figure 3

TYPE ULN-2001A SCHEMATIC

14 to 25 Volts PMOS Applications

The Type ULN-2002A Darlington array was specifically designed for use with 14 to 25 volt PMOS devices. Each input has a 7 V Zener diode and a 10,500 ohm resistor (nominal values) to limit the input current to within the capability of most PMOS of the type specified. The basic circuit diagram is shown in Figure 5 with a typical application. Note that there are *no* pull-down resistors or other external discrete components necessary. The incorporation of the Zener diode also results in excellent noise immunity for this array.

TTL and CMOS INTERFACE

The ULN-2001A and ULN-2002A allow only a limited number of input options. Shown in Figure 6 is the basic circuit diagram of the Type ULN-2003A. This device has a series base input resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS logic operating at a supply voltage of 5 V (or 12 V CMOS using FET characteristics).

A guarantee of 200 mA output sink current capability (saturated) is provided with the worse case TTL logic *1* level of 2.4 volts. Low-power Schottky-clamped TTL logic is generally specified to have a minimum V_{OUT} of 2.7 volts. The ULN-2003A is guaranteed to sink 250 mA under this input condition. With the more typical input of 3 volts, the ULN-2003A Darlington pair will sink at least 300 mA in the "ON" state.

DRAIN-TO-SOURCE VOLTAGE, V_{DS}
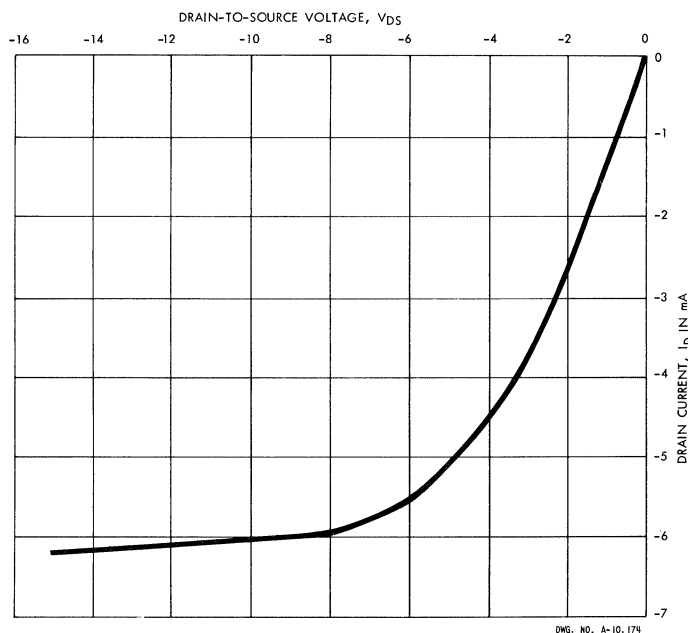
Figure 4

TYPICAL P-CHANNEL

DRAIN CHARACTERISTIC

DRAIN CURRENT, I_D IN mA

DWG. NO. A-10,174

ULN-2002A

(each driver)

DWG. No. A-9650

DWG. No. A-9652

+V_SS   PMOS OUTPUT   +V
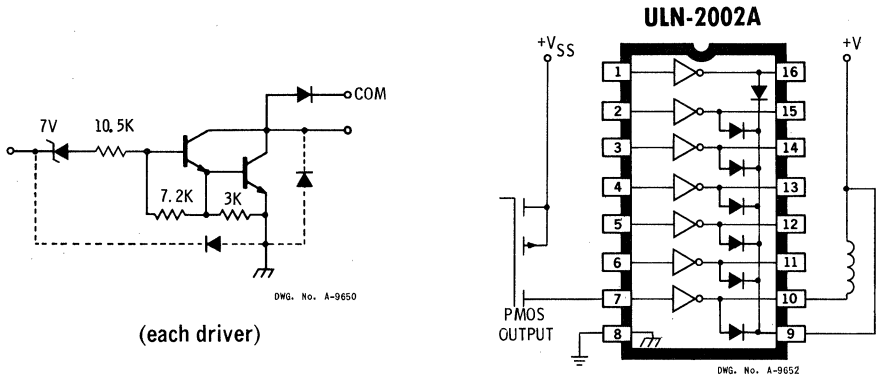
Figure 5

TYPE ULN-2002A SCHEMATIC AND APPLICATION

TTL totem pole outputs are not specified between the 400 μA logic 1 fanout condition and the maximum output short-circuit current (20 to 55 mA for the 7400 series). Between these rather wide limits lies the required ULN-2003A input current. The maximum Type ULN-2003A input current level is specified at 1.35 mA at the extrapolated TTL maximum logic 1 level of 3.85 V.

The ULN-2003A Darlington array will handle a great many interface needs – particularly those beyond the capabilities of TTL buffers. Also shown in Figure 6, is a typical application of the ULN-2003A Darlington array. Of particular interest in this application is an unusual use of the transient-suppression diodes for a non-inductive load. The lamp test feature can of course be used with any of the devices in this series.

ULN-2003A

(each driver)

DWG. No. A-9651

DWG. NO. A-9653A

+V_CC   TTL OUTPUT   +V   LAMP TEST
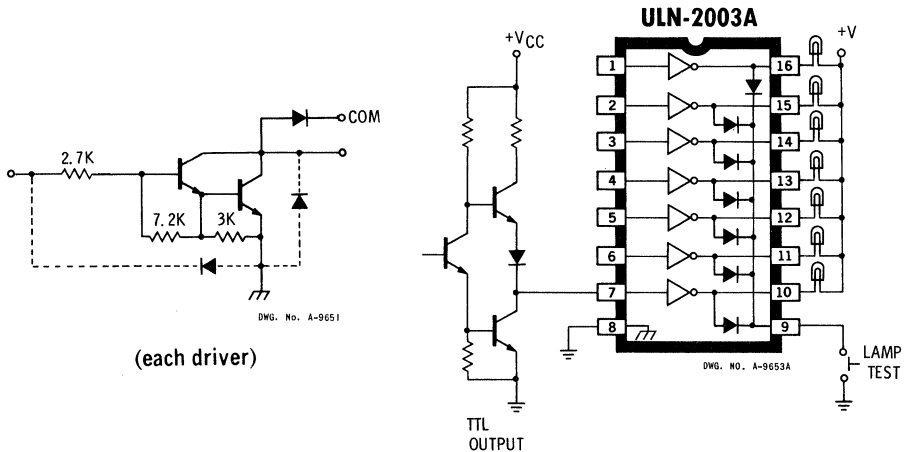
Figure 6

TYPE ULN-2003A SCHEMATIC AND APPLICATION

3—124

The diodes are designed to handle the same current and voltages as the output transistors. Switching can be accomplished through an ordinary switch or an appropriate power transistor. With the standard +70°C ambient and the most widely used lamps(No. 327 or No. 387 lamps) there is no problem with continuous operation.

6 to 15 Volt CMOS or PMOS Applications

The Type ULN-2004A Darlington array has an appropriate series input resistor (nominally 10.5 kΩ) to allow its operation directly from CMOS or PMOS logic outputs utilizing supply voltages of between 6 and 15 V.

Shown in Figure 7 is a typical application of this array. Although the discrete output buffer could be used to increase the output capability of any of the devices in this series, this is most often done by paralleling outputs as was described earlier.

Input Current

The Darlington collector current (output in saturation) at an ambient temperature of +25°C, for any input current is the same for all four devices in this series and is shown in the graph of Figure 8. More accurately, the maximum input current for any collector current is described by the equation:

$$I_{IN(\mu A)} = I_{C(mA)} + 140 \ \mu A$$

where I_{IN} is the input current in microamperes, I_C is the collector current in milliamperes, and the figure 140 represents the maximum shunt current through the emitter-base resistors. The typical input current can be described as:

$$I_{IN(\mu A)} = 0.58 \ I_{C(mA)} + 110 \ \mu A$$

where the figure 0.58 is an adjustment for the typical Darlington current gain and the figure 110 represents the typical shunt current.

DWG. NO. A-9898A

(each driver)

DWG. NO. A-9654A

Figure 7

Type ULN-2004A SCHEMATIC AND APPLICATION

DWG. NO. A-9755A
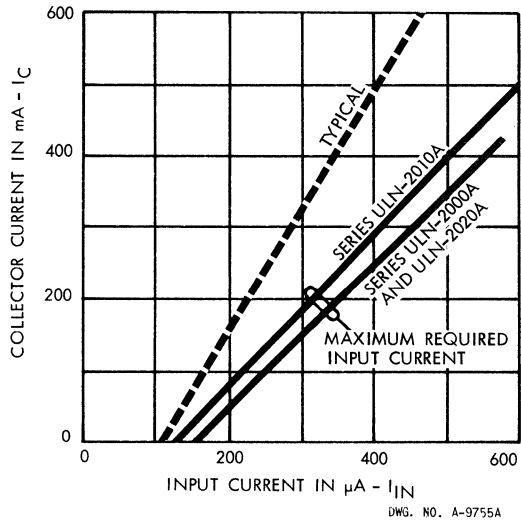
Figure 8

COLLECTOR CURRENT

AS A FUNCTION OF INPUT CURRENT

The input current as a function of input voltage is shown in Figure 9 for the ULN-2002A, ULN-2003A, and the ULN-2004A. The Type ULN-2001A Darlington array is not shown since input current is more a function of the external circuitry. Systems utilizing either CMOS or PMOS logic should be evaluated for intrinsic current limiting as was shown in Figure 4.

DWG. NO. A-9757A

DWG. NO. A-9756B

DWG. NO. A-9899A
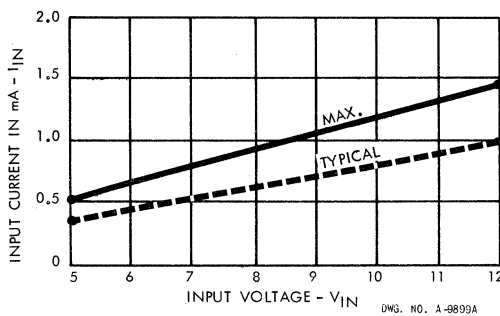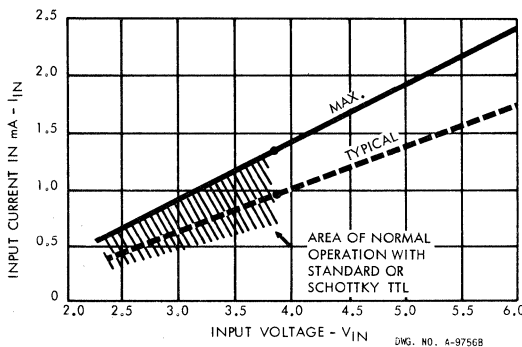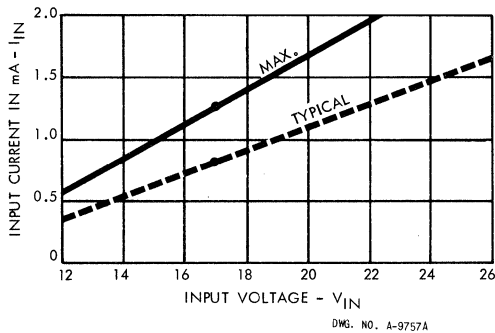
Figure 9
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

Low Available Drive Current Operation

Occasionally, applications featuring minimum available input drive current and a high output load current have shown the Type ULN-2003A and ULN-2004A Darlington arrays to be inadequate for the particular requirement under worst case conditions. This usually results from the restricted drive current available from a TTL or CMOS gate operating from a nominal supply of 5 volts.

Under worst case conditions with a low logic *1* voltage (2.4 V), and a high input resistor value (3.51 kΩ), the available load current is reduced to only 145 mA. Compounding this problem would be the effect that a high drive current requirement would have on the logic output voltage since that is normally specified at only 400 μA. If the gate output is connected to additional logic elements, a minimum logic *1* voltage of 2.0 V must be maintained and at that level the worst case Darlington load current would be reduced to only 31 mA!

A simple solution to this problem is through the use of inexpensive pull-up resistors as shown in Figure 10. The minimum resistor value is determined by the maximum allowable sink current (16 mA for TTL, 360μ A for CMOS), the minimum logic *0* output voltage, and the maximum supply voltage as per the following equation:

$$R_P \geq \frac{V_S - V_{OUT(0)}}{I_{OUT}}$$

For standard TTL, the minimum value for R_P is about 316 Ω with values between 3000 Ω and 5000 Ω being used customarily. Multiple pull-up resistors in a single in-line package are shown in Sprague Engineering Bulletin No. 7041; resistors in a dual in-line package are shown in Bulletin No. 7042.

Conclusion

Since the Series ULN-2000A high-voltage, high-current Darlington transistor arrays are quite conservatively designed, the basic product is fully capable of being ordered to higher voltages and/or higher currents than the standard specifications. Presently, parts are available to withstand up to 95 volts on the output. Parts with this higher voltage rating would create a potential for switching loads far in excess of 125 watts! Aside from the higher power handling capability, the higher voltage rating is required for driving plasma or gas-discharge displays.
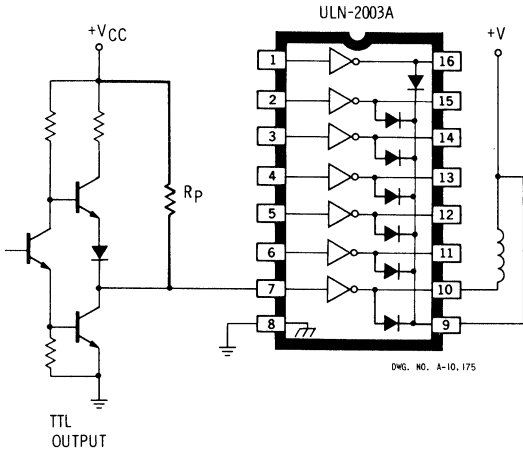
Figure 10

**USE OF PULL-UP RESISTORS
TO INCREASE DRIVE CURRENT**

Although not intended for high power applications, there is also available a Series ULS-2000H with hermetic sealing and an operating temperature range to +125°C. These parts are recommended for military and aerospace applications as well as commercial and industrial control applications where severe environments may be encountered.

Cer-DIP, industrial-grade hermetic devices, Series ULQ-2000R, are rated for use over the temperature range of −40°C to +85°C, permitting their use in commercial and industrial applications requiring a moderate package power dissipation (1 W at T_A = +85°C).

All of these Darlington transistor arrays offer a common solution to a great many interface needs. The minimal component count and straightforward printed wiring board layout offer benefits in cost reduction, simplicity of board layout, and savings in space. Other benefits are a reduction in insertion costs, and lower handling and inventory costs than other alternatives. Cost benefits from some of these factors are not very tangible. However, fewer components, less complex boards, etc. usually result in lower system manufacturing costs.

INTERFACE IC MOTOR DRIVE APPLICATIONS

THE INCORPORATION OF LOGIC systems and power drivers into a monolithic integrated circuit requires special skill and experience. Sprague Electric Company has developed such skill, and has long been a leader in solid-state interface technology and devices.

Improved systems reliability and performance, lower component counts, space savings and cost economy are some of the benefits to be derived from the use of Sprague Interface ICs. An increasing number of these Sprague devices are especially designed for or are easily adapted to motor drive applications. The availability of these devices is especially significant in view of the increasing use of microprocessor-based controls for servo and stepper motors.

UCN-4202A STEPPER MOTOR TRANSLATOR/DRIVER

THE UCN-4202A will drive permanent magnet (PM) stepper motors rated to 500 mA and 15 V with a minimum of external components required, or, the device may be used as a logic translator to drive discrete high-power transistors or the Sprague UDN-2949Z Half-Bridge Motor Driver.

With the MONOSTABLE RC timing pin (Pin 11) tied to V_{CC} (Pin 16) the circuit performs a full-step function. States B and D are stationary states and a separate input pulse is required to move through each of four output states.

The UCN-4202A internal step logic activates one of four output sink drivers to step the load from one position to the next. The logic is activated when the STEP INPUT (Pin 10) is pulled low for at least 1 μs and then allowed to return high. The sequence of states is determined by the DIRECTION CONTROL (Pin 12), either A-B-C-D, or A-D-C-B.

In the double-step mode states B and D are transition states with durations determined by the MONOSTABLE RC timing (Pin 11). Improved motor torque is obtained at double the nominal motor step angle, and motor stability is improved for high step rates.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage, V_{CE} .... 13.5 V
Output Current, I_{OUT} .... 500 mA
Supply Voltage, V_{CC} .... 5.5 V
Supply Voltage, V_K .... 13.5 V
Input Voltage, V_{IN} .... 5.5 V

FULL-STEP MODE
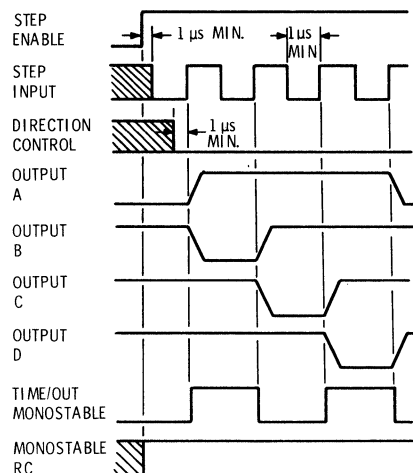
Dwg. No. A-12,353
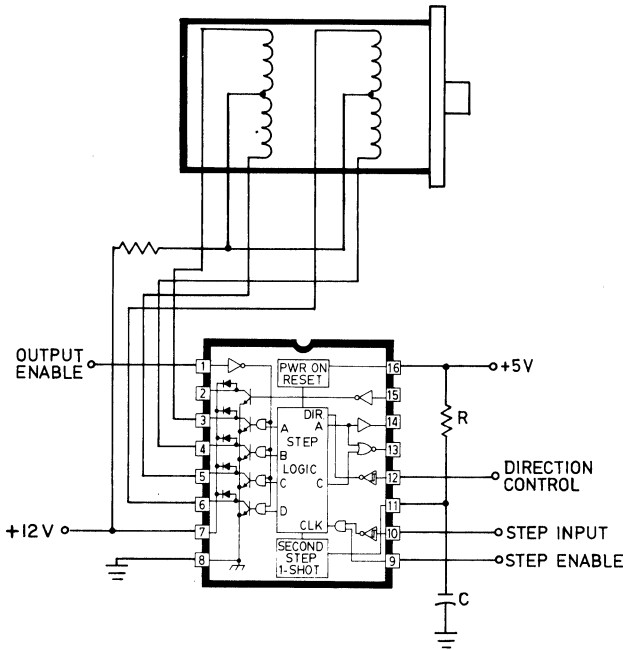
L/R DRIVE CIRCUIT

Used to Drive A 12-Volt
500 mA Unipolar Stepper Motor
(Double-Step Mode)

OUTPUT ENABLE

+5V

R

DIRECTION CONTROL

+12 V

STEP INPUT

STEP ENABLE

C

Dwg. No. A-11,187

TYPICAL A-C MOTOR APPLICATION

UDN-2949Z   UDN-2949Z

+5V   +5V   +5V

STOP

10K

GO

10K

UCN-4202A

PWR-ON RESET

DIR A
STEP
B
LOGIC
C C
D
CLK
SECOND STEP 1-SHOT

SPEED, ≈ 80 Hz

510 K

3.6 K

1 µF

5.1 K

CD4049AE

+24V

60 Hz MOT

80 pF

DEAD TIME, ≈ 50 µs

Dwg. No. B-1447

3—129
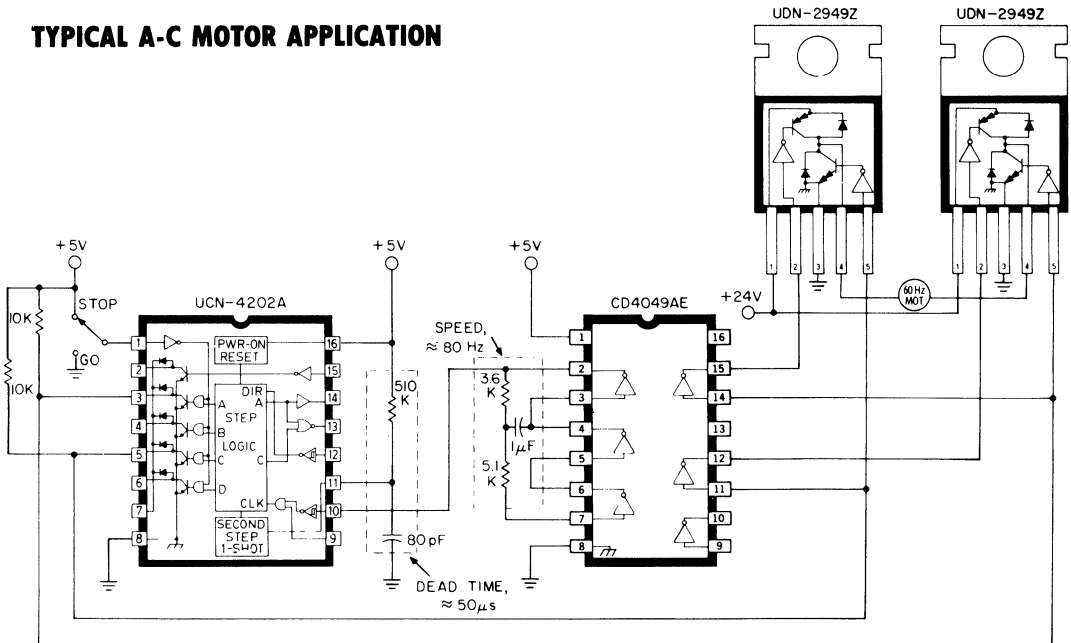
UDN-2949Z HIGH-CURRENT BIPOLAR HALF-BRIDGE MOTOR DRIVER

THE UDN-2949Z is a monolithic half-bridge motor driver supplied in a power tab TO-220 style package. The circuit combines sink and source drivers with diode protection, gain and level shifting systems, and a voltage regulator for single-supply operation. The unit is specifically designed for servo motor drive applications using pulse width modulation (chopping).

The chopper drive mode is characterized by a minimum power dissipation requirement while allowing the output to switch currents of 2 amperes. Output d-c current accuracies of better than 10% at 100 kHz can be obtained.

The UDN-2949Z may be used in pairs (full-bridge) for d-c stepper motor or brushless d-c motor drive applications. High load currents or step rates will usually require an external ground clamp diode (1N4000) connected at the output of each device.

The UDN-2949Z power driver may be also be used in stepper motor bipolar bridge drive circuits for example, with the Sprague UCN-4202A Stepper Motor Translator/Driver, as shown.

RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage Range, V_S . . . . 15 V to 28 V
Input Voltage, V_{IN} . . . . 5.5 V
Continuous Output Current, I_{OUT} . . . . ±2.0 A
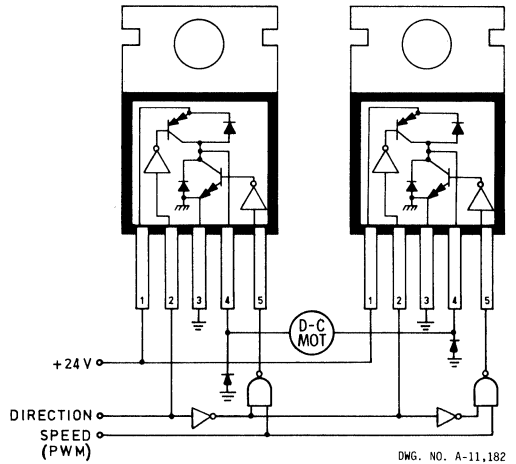
DWG. NO. A-11,182

FULL-BRIDGE D-C SERVO MOTOR APPLICATION

Dwg. No. A-11,181A

SINGLE-WINDING D-C OR STEPPER MOTOR

DWG.NO. A-11,241

Timing Conditions

3—130
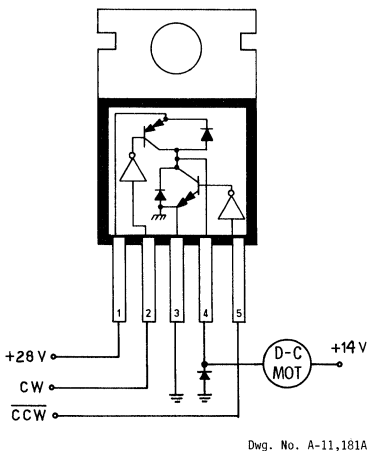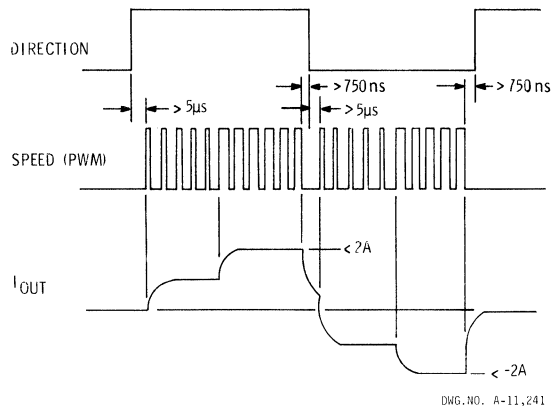
TYPICAL 3-PHASE BRUSHLESS D-C MOTOR DRIVE
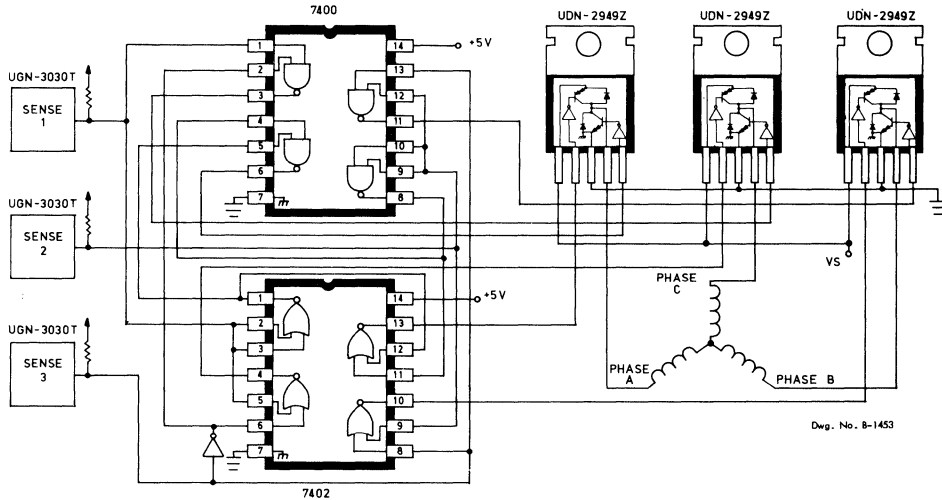
Dwg. No. B-1453

ULN-3701Z and ULN-3702Z HIGH-CURRENT DRIVERS

THESE HIGH-CURRENT drivers are suitable for driving d-c motors rated to ±2.5 A and 18 V with minimum external components. Internal voltage, current, and temperature shut-down circuitry protect these devices under the most severe operating conditions. The ULN-3702Z does not include the high-voltage shutdown, allowing operation with supply voltages up to 28 V. The high-gain, high-impedance operational amplifier configuration allows many specialized input, output, and feedback arrangements.
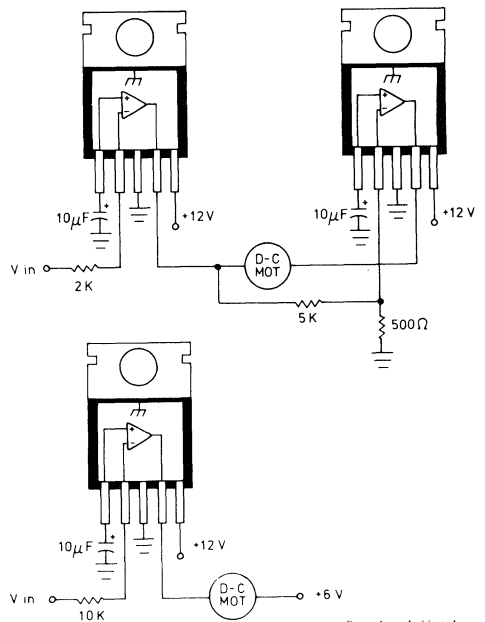
Dwg. No. A-11,314

SERIES ULN-2800A DARLINGTON ARRAYS and
SERIES UDN-2980A HIGH-CURRENT SOURCE DRIVERS

THE COMBINATION of separate 8-channel source and sink driver ICs provides a single or twin motor drive interface solution for "crossover" currents which may occur during switching transitions. No timing provisions are necessary provided the external resistance limits "crossover" currents to the maximum specified for the ICs (± 500 mA).

Flyback voltage should not exceed the recommended V_S level ($+35$ V or $+50$ V). With a UDN-2982A/ULN-2803A combination and a $+24$ V supply the flyback voltage should not exceed $+35$ V [V_S(max) + V_{Zener}(max) + V_{clamp}(max) ≤ 35 V].

Single motor drives may be accomodated by paralleling both inputs and outputs of each IC (max $I_{OUT} = \pm 1.0$ A; DIP rating allows ≈ 350 mA max).

Stepper motor bridge driver circuits using techniques such as that illustrated below should achieve greater reliability and space economy, cost reduction and improved performance.

RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage, V_s
    UDN-2982A and ULN-2803A . . . . 35 V
    UDN-2984A and ULN-2823A . . . . 50 V
Peak Output (100 ms), I_{OP} . . . . ± 350 mA
Continuous Output Current, I_{OUT}
    Single Motor . . . . ± 300 mA
    Independent Operation Twin Motors . . . . . . ± 300 mA
    Simultaneous Operation Twin Motors . . . . . ± 150 mA

UDN-2982A and ULN-2803A Twin Motor Combination

Dwg. No. A-11,192A
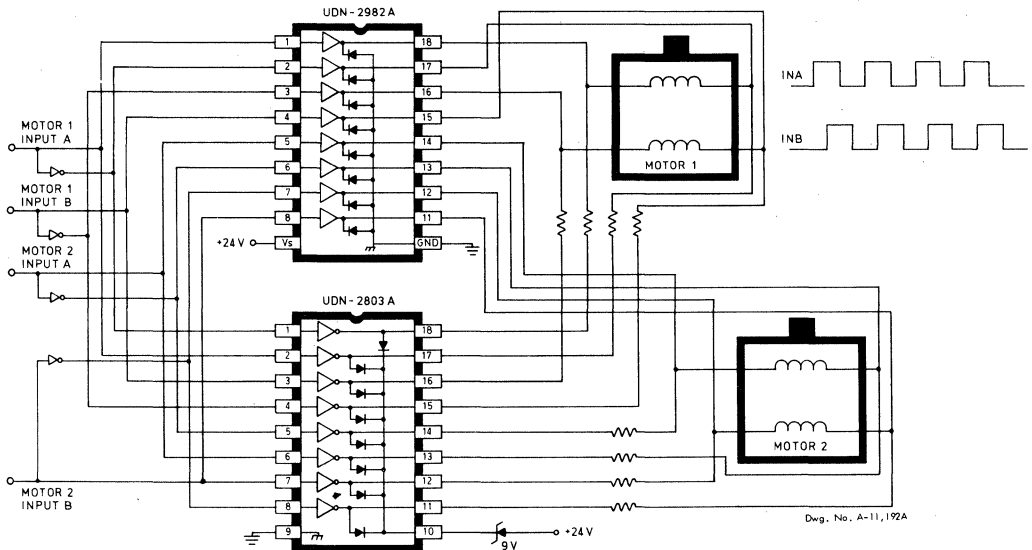
UDN-2580A SOURCE DRIVER

THE UDN-2580A SOURCE DRIVER serves as a direct interface from the Cybernetic Micro Systems CY500 Motor Controller, utilizing paralleled inputs and outputs. This IC is most useful with supplies of up to − 35 V. A selected version (UDN-2580A-1) is available for operation to − 50 V.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage, V_{CE} . . . . .35 V*
Output Current, I_{OUT} . . . . −350 mA

*Referenced to −V (+5 V and −30 V shown)
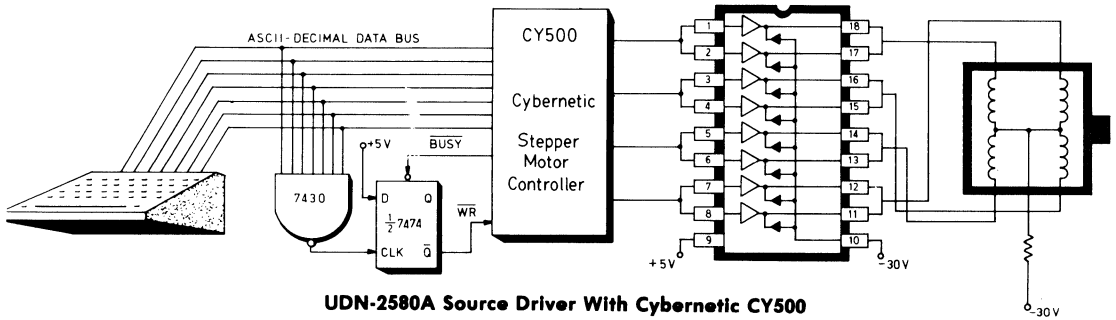
UDN-2580A Source Driver With Cybernetic CY500

DWG. NO. A-11,195

UDN-2845B and UDN-2846B QUAD DRIVERS

THESE QUAD DRIVERS are designed to handle high current loads operating from negative supplies. The d-c motor interface shown uses external diodes for clamping and commutation. A 10 μs interval between input transitions is recommended to prevent "crossover" current damage to the IC.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage, V_{CE} . . . . −35 V
Output Current, I_{OUT} . . . . −1.5 A
Supply Voltage, V_S . . . . .5.0 V
Input Voltage, V_{IN}
  UDN-2845B . . . . .5.0 V
  UDN-2846B . . . . .12 V
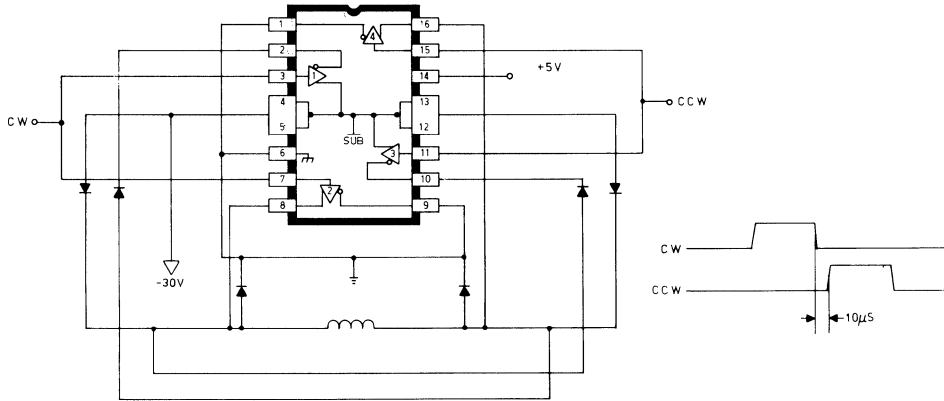
DC MOTOR INTERFACE

DWG. NO. A-11,193

UCN-4401A and UCN-4801A BiMOS LATCH/DRIVERS

THESE HIGH-VOLTAGE, high-current latch/drivers are comprised of four or eight CMOS data latches, a Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and DUTY CYCLE CONTROL functions. Data bits can be sent to the latch/drivers at rates from 500 kHz (V_{DD} = 5 V) to 1 MHz (V_{DD} = 12 V).

Microprocessor power can be utilized more effectively in motor drive systems incorporating UCN-4401A or UCN-4801A latch/drivers. The appropriate motor windings can be activated (usually at millisecond rates) while the microprocessor spends nearly 100% of its time performing other functions.

A full-step drive scheme implemented with the 4-latch UCN-4401A provides 350 mA for each output. The 8-latch UCN-4801A may be used for systems operating more than one motor, with 300 mA available for each output.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage, V_{CE} . . . . 35 V
Output Current, I_{OUT} . . . . 350 mA
Supply Voltage, V_{DD} . . . . 15 V
Input Voltage, V_{IN} . . . . V_{DD}
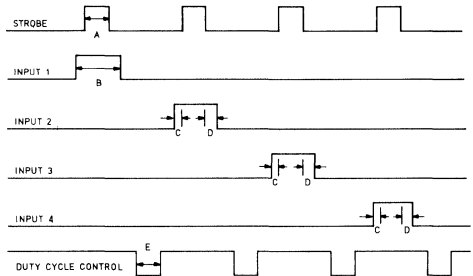
Dwg. No. A-11,194A

A. Minimum strobe pulse width _____ 300 ns
B. Minimum data pulse width _____ 300 ns
C. Minimum data set-up time _____ 100 ns
D. Minimum data hold time _____ 100 ns
E. Minimum duty cycle control pulse width ___ 300 ns

Timing Conditions (V_{DD} = 5.0 V)
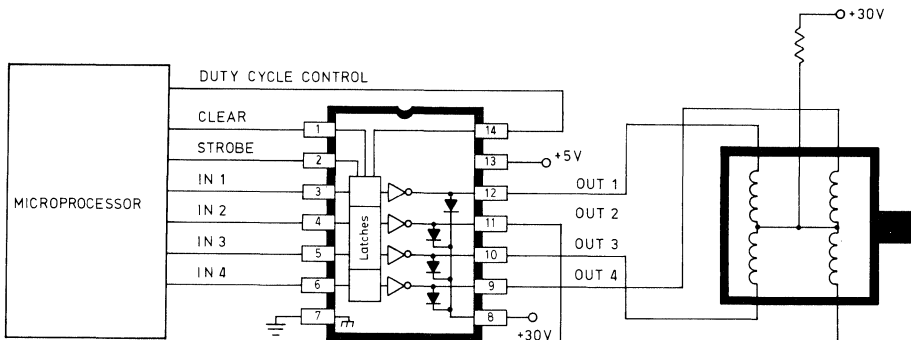
Dwg. No. A-11,191A

EXPANDING THE FRONTIERS OF IC INTERFACE FOR ELECTRONIC DISPLAYS

INTRODUCTION

The original monolithic high-voltage/high-current power drivers from Sprague were capable of sustaining 100 V and sinking load currents of 250 mA on each of four outputs. That 1970 peripheral driver capability has since been expanded and improved on to solve many of the most difficult display interfaces. Our newest devices are rated for operation to 130 V, sourcing or sinking to 1.5 A, and as many as eight drivers per package (not all together) with inputs for TTL, Schottky TTL, DTL, CMOS, and PMOS.

LAMP (INCANDESCENT) INTERFACE

Utilizing marketing inputs that related to existing hybrid interface circuits, a group at Sprague designed and manufactured monolithic ICs which initially were largely used for aircraft indicator lamp interface. Although not widely known, these quad driver units were developed quite independently (and simultaneously) to the ubiquitous TI 75451 series of high-speed, low-voltage peripheral drivers. A concentration upon circuit design factors, improvements in DIP packaging (copper alloy lead frames), and tighter, tougher control of diffusion-related parameters has allowed the manufacture of quad power drivers rather than the dual mini-DIPs offered by TI.

An increased awareness for improvements in reliability and space and power reductions provided a rather successful military market for Sprague lamp and relay interface; early success was evident in military aircraft indicator lamp interface, a tough application for TTL type ICs due to severe inrush currents resulting in secondary breakdown during "turn on". The increased current sinking capability of the Sprague ICs offers a solution to lamp interface that usually obviates the need for "warming" resistors (across the output) which slightly warm the lamp filament and thus minimize problems associated with cold lamp filaments.

The relay driver types of Sprague IC drivers (and other similar transient-protected ICs) are somewhat more useful than the so-called general purpose types, since the diode common terminal may be switched for a system lamp test. As shown in Figure 1, only a single connection to each DIP is required.
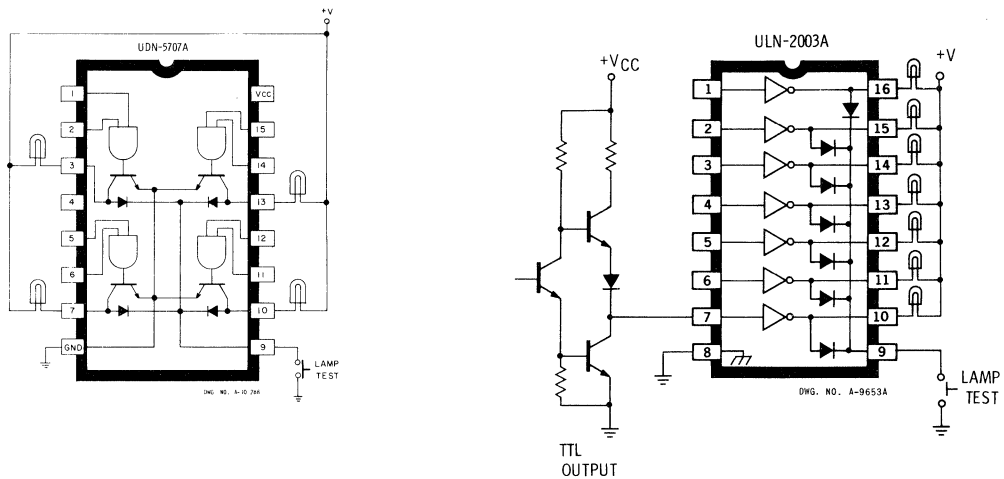
Figure 1

The high current-sinking capability of the Sprague ICs allow such loads as the #327 or #387 lamps to be driven without difficulty of secondary breakdown. The device beta will usually not allow sinking of the 10 to 13 times (nominal value) inrush current of cold lamps; but the lamp rapidly reaches a current level within the device output limitations (Figure 2 shows current as a function of time for a single #327 lamp). Sustaining this instantaneous inrush current and its peak power has been a key element in the success of many lamp interface circuits.

GAS DISCHARGE DISPLAY ICs

Early in 1972, Sprague successfully produced its first high-voltage IC designed for gas discharge displays—a five channel, 130 V unit for cathode (segment) interface. Subsequently, other circuits, both cathode and anode drivers, were produced; most of which were used in calculator applications with the Burroughs Panaplex® II. In Figure 3 is shown a display interface system utilizing the UHP-481 and UHP-491 display drivers, associated thick-film networks, and discretes. This was a step forward, but still required external discrete components.

Through a collaborative effort begun late in 1973 between Sprague Electric and Burroughs Corp. a newer, more efficient interface scheme evolved. Featured in "Electronic Displays '75," this series of monolithic IC interface devices for the high-voltage gas discharge panels has been one of the trailblazers in the world of display interface ICs. Intended for use in multiplexed display systems, these ICs present one of the easiest and least expensive solutions to a difficult interface problem. A combination of high-voltage bipolar techniques with thin-film resistor technology (circuit resistors sputtered over the IC dielectric) has provided both digit (anode) and segment (cathode) interface.
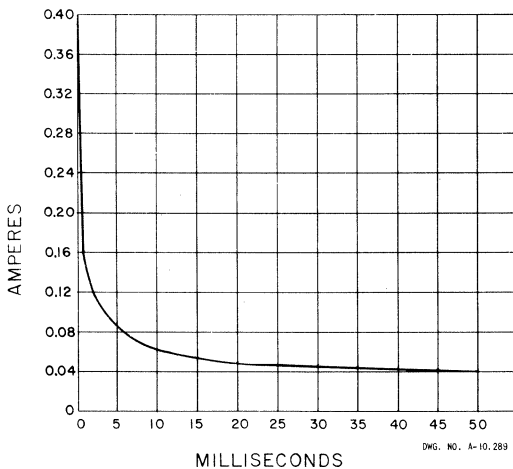
To facilitate a minimum component interface, a split supply (± 100 V) is employed to allow d-c level-shifting (rather than capacitors or >200 V transistors) and both digit and segment drivers incorporate all pull-up, pull-down, current limiting, off-bias reference, etc. which were formerly required in discrete and/or hybrid systems. With the combination of the digit and segment drivers (each capable of withstanding 120 V), the split power supply approach affords PN diode IC technology suitable for driving a display usually requiring a 180 V minimum ionization voltage (equivalent to ± 90 V in the split system).

The use of the Series UDN-6100/7100A gas discharge display drivers shows the need for only two monolithic ICs for displays of up to eight digits and eight segments as shown in Figure 4. Systems requiring digit or segment counts greater than eight employ additional driver ICs, and with the exception of the Type UDN-7180A segment driver, the segment ICs all have outputs with internal current-limiting resistors for the display segments. The UDN-7180A device, for reasons of package power dissipation and/or dissimilar segment currents (certain 14 or 16 segment alphanumeric panels) can also be used, but must have external, discrete current-limiting resistors.

MILLISECONDS

DWG. NO. A-10.289

Figure 2

Type 206C and 216C are single in-line networks

DWG. NO. A-9413A

Figure 3

3—136

Figure 4

Higher current applications are difficult for both programmable current and switching type display drivers. Segment currents beyond 2.5 or 3 mA present package power dissipation limitations to most dual in-line packages. By using external resistors, the Type UDN-7180A driver allows segment currents of up to 14 mA.

The transistor switch with current-limiting resistor scheme used in Sprague gas discharge display drivers

also minimizes problems associated with gas panel arcing which can destroy programmable current circuits. Some of the gas display manufacturers recommend the use of series resistors in each segment line to prevent destruction to the semiconductor interface circuit should such a panel arc occur. Without these series resistors (internal thin-film resistors in Sprague devices) the IC can be destroyed by the high voltage and resulting high current should the panel voltage drop to a very-low level during an arc.

LED INTERFACE

With the obvious abundance and variety of LED interface integrated circuits it would seem unlikely that there are still systems in search of an IC hardware solution to further minimize cost, component count, space, etc.; but this is definitely the case. The deficiencies are chiefly related to the limited number of current-sourcing circuits and/or high-current drivers.

The efficiency of LED displays has improved, but with the larger digits (up to 1″ presently) most of the IC drivers are unable to switch the higher currents required in multiplexed systems. The rule-of-thumb generally applied uses the suggested d-c current - multiplied by the number of digits in the display. For example, a multiplexed display of 160 mA peak current will give approximately the same light intensity output as a steady 20 mA in each of eight digits. Of particular difficulty is the switching of currents associated with the lower efficiency yellow and green LEDs. Sprague has provided monolithic integrated circuit solutions to applications requiring segment currents of 350 mA and digit currents of up to 1.5 amperes!

Many of the Sprague ICs used in high-current LED applications were originally designed for use with electro-mechanical loads (relays, solenoids, motors, etc.) although the high-voltage ratings of the drivers are obviously not a concern. A combination of high-current, high-voltage Darlington drivers is shown in Figure 5.

The ULN-2074B source driver is utilized as a modified emitter-follower. Through the use of discrete diodes in the common collector line, allowing the base to be switched to a potential higher than the collector, it is then possible to obtain a saturated output. This prevents the usual emitter-follower problems associated with gain, the MOS output impedance, and power. It is also possible to now better define the voltage at the emitter output and to then provide suitable segment current-limiting resistors for the LEDs.

The ULN-2002A sink driver is a high-current Darlington array with the capability of switching multiplexed LEDs with an available limit of 155 mA for each of the seven drivers when used at a 100% duty cycle. Even the more inefficient yellow or green LEDs can be driven with higher output currents at lower duty cycles (400 mA at a 28% duty cycle).

DWG. NO. A-9776B
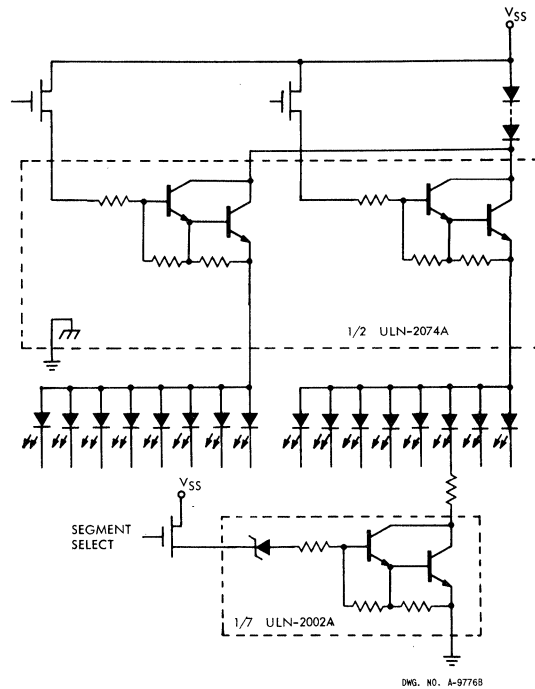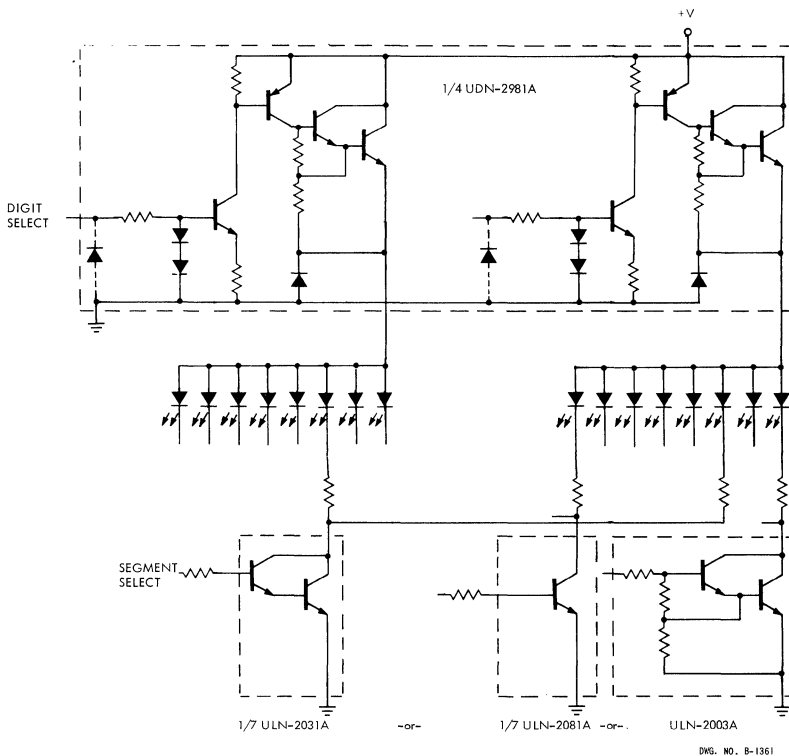
Figure 5

Figure 6

A new eight-channel source driver is shown as a digit switch for common anode LEDs in Figure 6. The Series UDN-2980A drivers will handle output currents to a maximum of 500 mA. Two basic versions of the driver will allow interface from TTL, Schottky TTL, DTL, PMOS, and CMOS levels. Other versions of the ULN-2003A driver are also available for use with the various logic levels.

Of the three sink drivers shown, the ULN-2003A is probably the better choice from a standpoint of both pinout and component count. It also has straightforward in-out pinning. The ULN-2031A and ULN-2081A devices offer lower cost. They are also interchangeable from a pinning aspect although the output ON voltage will be dissimilar.

A common-cathode LED configuration is shown in Figure 7 for currents of up to 1.5 A per digit! A series UDN-2980A source driver is used to switch the segment side, the ULN-2064B or ULN-2074B to switch the digit side. As has been shown with Figure 5, the IC package power dissipation must be considered with high-current applications.

The three examples that have been shown for LED interface represent only a very-small portion of the total applications area. The high-current capabilities and high gain of the Sprague drivers represent potential solutions to many difficult LED display systems - alphanumeric, seven-segment, or matrix; common-cathode or common-anode; continuous or multiplexed.

A-C PLASMA DISPLAY INTERFACE

Plasma displays, such as those manufactured by National Electronics/NCR (USA) and NEC or Fujitsu (Japan), all have one common element with their gas discharge cousin - both types use a neon gas mixture. The plasma panels emit an orange glow when switched at rather high frequencies, and light output intensity is a function of frequency. The a-c term for the plasma display is something of a misnomer since these panels actually operate from a toggled d-c supply (usually in the area of 20 kHz).

The panel is basically a neon-filled capacitor, and has plates (electrodes) which are covered with the dielectric - between which is the neon mixture. Switching this capacitive load presents a problem

with high peak currents in addition to the older problem of the high voltages which are associated with gas displays. Drive circuits use supply voltages of 150 to 260 V (depending on unipolar or bipolar drive), and the semiconductors used must switch instantaneous currents in the order of several hundred milliamperes for the larger displays.

Several high-voltage, high-current arrays made at Sprague Electric can provide an answer to one side of the a-c plasma display interface. The Series ULN-2020A Darlingtons are rated at 95 V while the Series UHP-500 power drivers are rated at 100 V. They are both able to handle the application shown in Figure 8 (a basic d-c, non-multiplexed clock interface rather than a more complex multiplexed system). The ULN-2022A is specifically designed for 14 to 25 V

PMOS logic levels while the UHP-506 is intended for use with TTL.

The high-current diodes that are internal to the Sprague arrays are utilized in the unipolar drive scheme connected to a suitable OFF reference. In one POS application, a set of 14 ULN-2023A Darlington drivers replaced more than 400 discrete components. The cost and space savings in such a machine are considerable, and a very complex printed wiring board was greatly simplified.

Further improvements in interface and plasma displays will no doubt evolve, and thus benefit all concerned - display and interface vendor along with the end user. Plasma displays are well-suited to custom panels (particularly those with various sizes of characters) and with improvements in IC breakdown voltages some further simplification of interface should evolve.
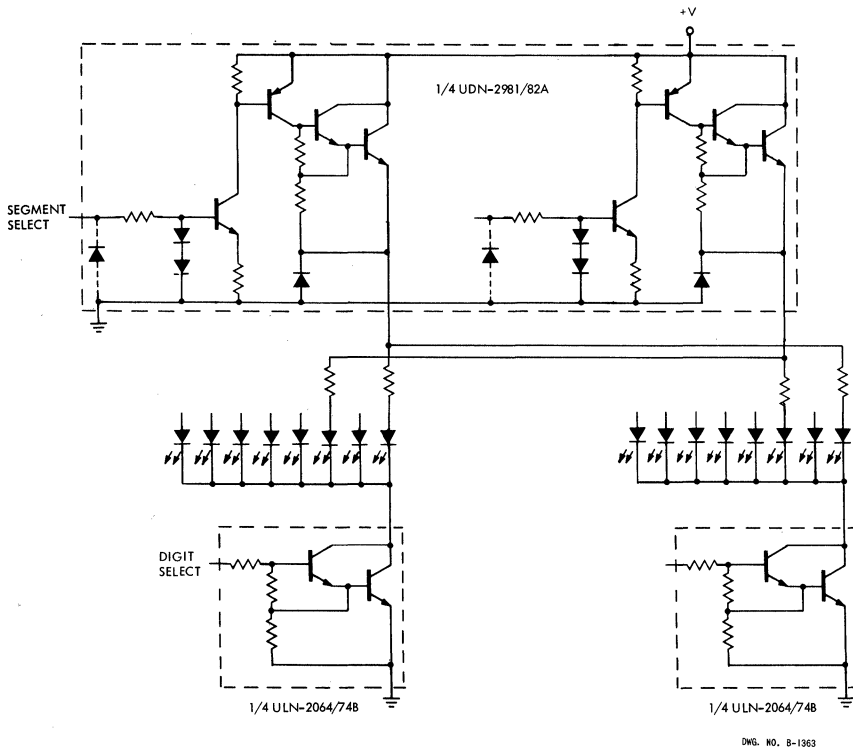
Figure 7
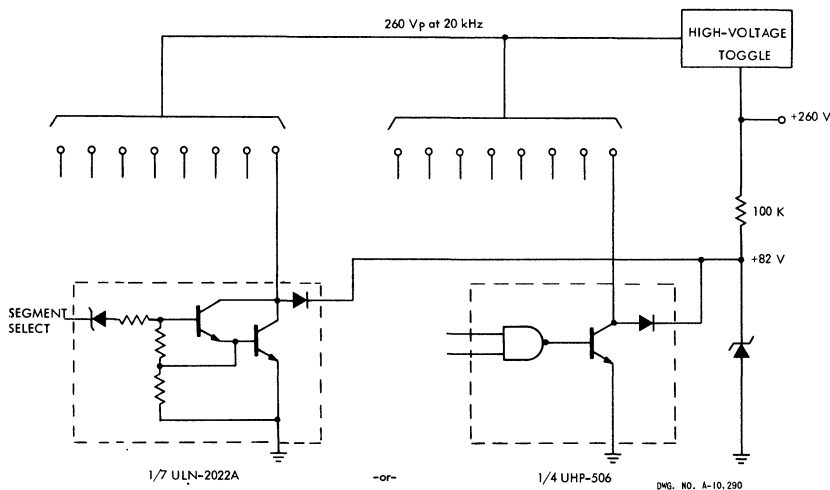
Figure 8

FLUORESCENT DISPLAY INTERFACE

Although the vast majority of fluorescent displays are directly driven from MOS logic (handheld and low-cost desk calculators), there is an emerging need for interface integrated circuits for use with the larger characters (higher currents) and the higher voltages coming into use. These blue-green display panels originated in Japan, and the manufacturers are quite aggressively pursuing markets such as POS systems, clocks, cash registers, appliances, automotive displays, etc. Larger and/or more complex styles are being made, including displays with alphanumeric capability (a starburst 14 or 16-segment pattern).

Modest voltage capability (60 or 70 volts) is all that is required of a semiconductor device to drive these panels, and the currents are in 20 to 30 mA region. These electrical requirements are well within the capability of many gas discharge digit drivers. In Figure 9, the UHP-491 is shown used with pull-down resistors connected to each output. When both the segment (equivalent to a vacuum tube anode) and the digit (controlled by the grid) are switched sufficiently positive with respect to the cathode (filament), the appropriate display digit/segment are energized.

Another multiplexed configuration is shown in Figure 10; the difference being that a push-pull type of MOS output is in use, and the pull-down rail does not allow the UHP-491 substrate, V_{DD}, and output potentials to be the same. The substrate and output are tied to the most-negative rail, while the V_{DD} terminal connects to the -12 V line for the MOS.

Since these solutions using the older gas discharge digit driver circuits require the use of appropriate pull-down resistors, either in discrete or thick-film network form, a more suitable solution employs the circuit shown in Figure 11. The UDN-6118/28A devices are designed specifically for use with fluorescent displays and include internal pull-down resistors so that up to eight segments and eight digits will require only two packages and a greatly simplified power supply. The Type UDN-6118A driver is compatible with TTL, Schottky TTL, DTL, and 5 volt CMOS. The Type UDN-6128A driver is for use with 6 to 15 volt PMOS or CMOS logic.

The future of fluorescent displays looks rather strong, particularly if competition further reduces prices. For the moment at least, these displays will not seriously tax the capability of IC interface except, perhaps, from a price/cost standpoint.
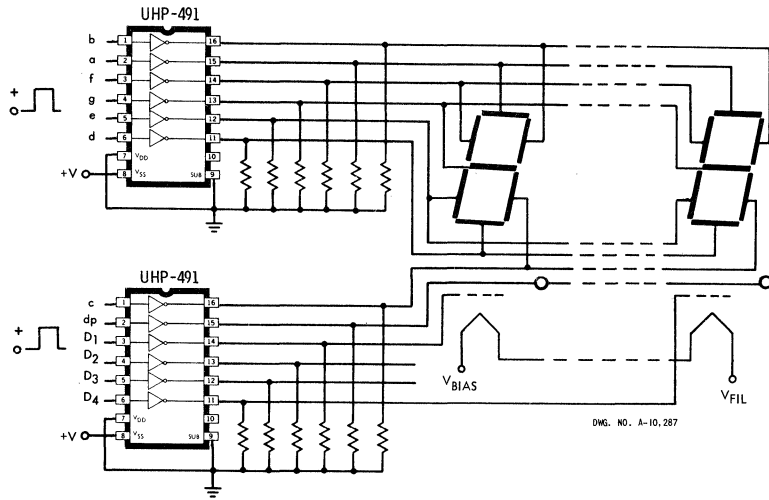
Figure 9
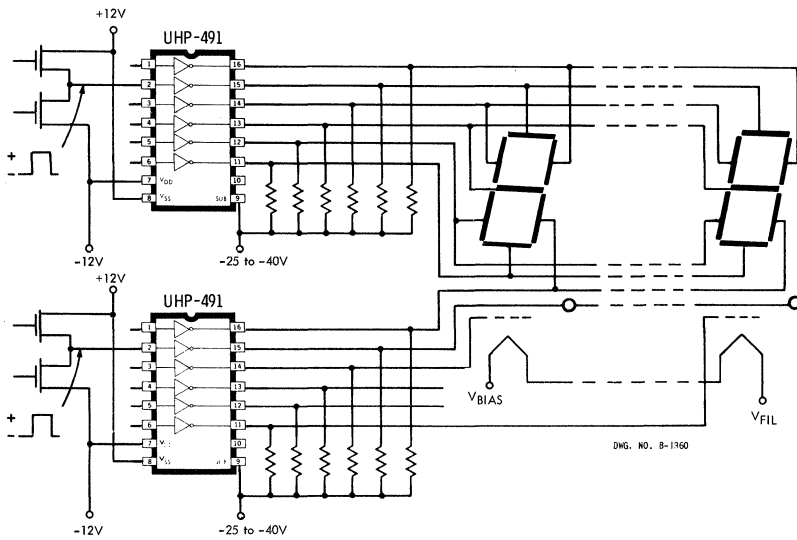
Figure 10

HOT WIRE READOUTS

Although hot wire readouts could easily be placed in the incandescent category, their application in multidigit, multiplexed display systems more closely resembles LED circuit operation. Since hot wire displays will conduct current in either direction, isolation diodes are required to prevent sneak paths from partially turning ON unaddressed segments. Compare the typical hot wire display of **Figure 12** with the LED display of Figure 6. The availability of a suitable, inexpensive diode array would be of considerable asset in multiplexed hot wire systems.

DWG. NO. A-10,261B

Figure 11

DWG. NO. B-1362
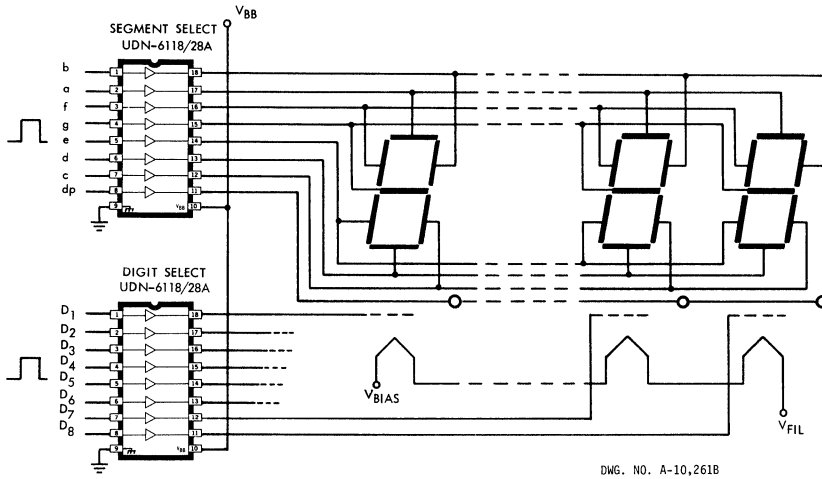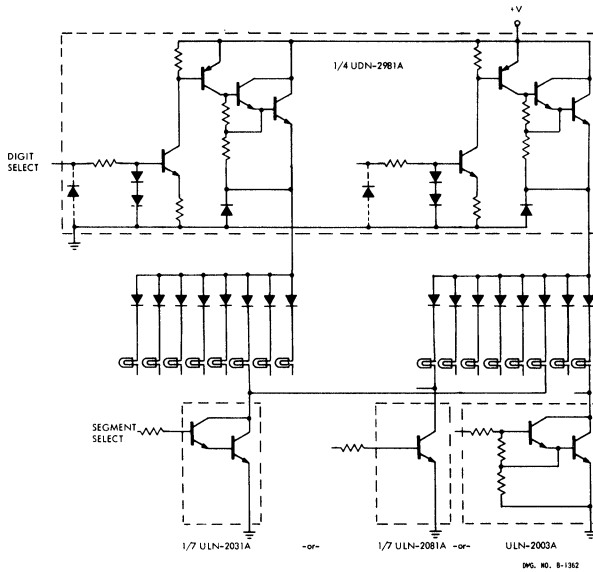
Figure 12

The hot wire readouts are available in both seven-segment and alphanumeric (16-segment) versions and are quite well-suited to high ambient light applications. They do not wash out in sunlight, although their reliability diminishes with the higher currents required in brightly lighted applications. As described, multiplexed schemes can be cumbersome because of the great number of discrete diodes required. One avionics system using a 16-character, 16-segment alphanumeric panel required 256 discrete diodes.
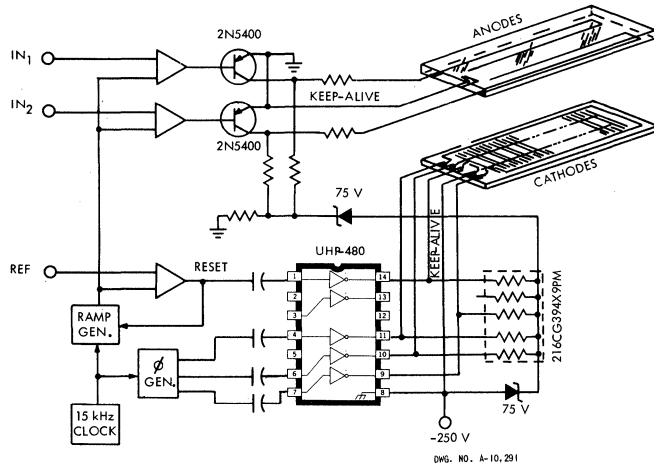
Figure 13

GLOW TRANSFER - BAR GRAPH & MATRIX PANELS

Neon-based display technology has shifted into many new market areas. The Burroughs Self-Scan® is a solution to many alphanumeric applications; the newer bar graph is a solid state replacement for analog instrumentation. Both use the glow transfer principle of the dot matrix Self-Scan display.

The nominal voltage for this type of panel is 250 V. High-voltage gas discharge drivers (Series UHP-480) or Darlington arrays (Series ULN-2020A) afford a cathode interface to the glow transfer panel. With a typical display current of 3 to 5 mA, the gas discharge drivers are perfectly adequate. For higher current applications, the Darlington arrays are a solution.

As illustrated in Figure 13, the bar graph cathode is easily driven with a Series UHP-480 driver. Signal level shifting is inexpensively accomplished with capacitors; the OFF reference, pull-up, and pull-down is done with a few discretes. The anodes are driven with two discrete transistors ($BV_{CES} \geq 120$ V). By utilizing a negative supply, the level shifting is easily done in the cathode side. If a positive supply were used, relatively complex d-c level shifting would be required in the anode side. The few discretes necessary in the circuit shown are generally a viable solution when faced with cost and space parameters for the system.

SUMMARY

The phenomenal growth in display technology has largely come as a result of the electronic calculator, and electronic displays will pervade all our lives in an ever-increasing number of products. The use of digital displays in appliances, gasoline pumps, electronic games (even pinball machines), etc., etc., etc., will also require that a continuing evolution of interface integrated circuits meet the challenges of higher brightness, increased currents, improved reliability, and lower system costs.

Both the display and semiconductor industries have demonstrated that they will meet the challenges of today, and these challenges then become routine with tomorrow.

INTEGRATED CIRCUITS FOR
CURRENT-SOURCING APPLICATIONS

DURING RECENT YEARS, the appearance of many new low-power monolithic devices (LSI and microprocessors) has created an increased need of peripheral power driver integrated circuits. Interface drivers are typically categorized in terms of their output-drive functions. When current flows out of the driver output terminal and into the load, the device is said to "source" current. Conversely, current flows from a load into a "sink" driver.

Sprague integrated source drivers usually consist of high-voltage PNP devices and high-power NPN Darlington outputs (which provide PNP-type action), with input-level shifting. These power ICs are useful for interfacing low-level logic (TTL, CMOS, NMOS, PMOS) and high-current or high-voltage relays, solenoids, lamps (incandescent, LED, neon), motors, and displays (gas-discharge, LED,

vacuum-fluorescent). They can also be used to provide multi-channel buffers for discrete power semiconductors.

The advantages of source drivers for display interface are quite evident. The X-Y addressing of most readouts requires both source and sink functions to minimize pin count, interconnections, and package count.

A more subtle advantage of source drivers is related to their use with inductive loads or incandescent lamps. Both types of load generate troublesome transients and noise currents on common logic/load ground lines. In addition, high ground currents can shift the ground rail, affecting logic input levels, thresholds, and noise immunity. The use of source drivers can minimize many of these concerns by separating the logic and power returns.

3

FLOATING LOGIC-GROUND LEVEL
(Sink Driver)

DWG.NO. A-11,532
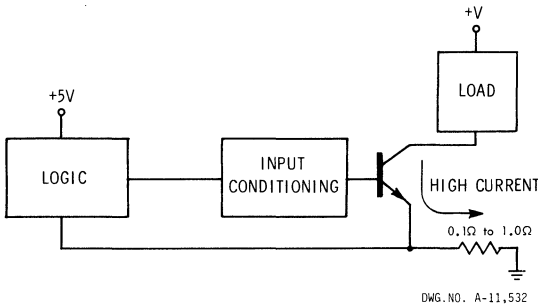
SEPARATE GROUND RETURNS
(Source Driver)

DWG.NO. A-11,531
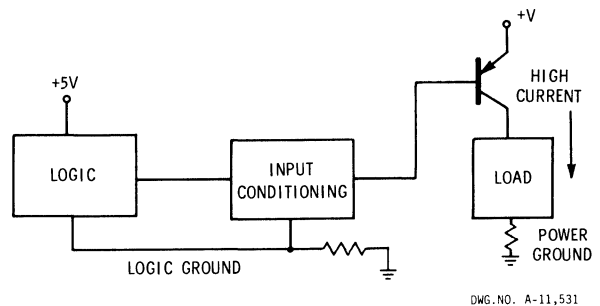
RELAY-DRIVER APPLICATIONS

SERIES UDN-2580A, eight-channel source drivers, and Types UDN-2956A and UDN-2957A, five-channel source drivers, provide current/voltage translation from TTL, positive CMOS, or negative CMOS logic to −48 V telecommunication relays requiring less than 350 mA. All devices have internal inductive-load transient-suppression diodes.

Type UDN-2580A-1 is best driven from negative-reference CMOS or NMOS logic (−5 V or −12 V swing) in order to provide a −48 V swing at the output. The active-low input Type UDN-2588A-1 can be driven from positive logic TTL

(+5 V swing) or CMOS (+12 V swing) levels. The active-high input Type UDN-2956A is similar to Type UDN-2588A-1, but it also has a chip-enable function that requires a minimum number of drive lines to control outputs from several packages in a simple multiplex scheme.

RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage, V_{EE} .... −50 V
Continuous Output Current, I_{OUT} (per output) ...... −350 mA

TELECOMMUNICATIONS RELAY DRIVER (Positive Logic)

UDN-2588A-1
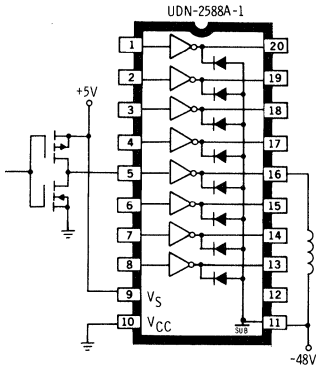
DWG. NO. A-11,524

TELECOMMUNICATIONS RELAY DRIVER (Negative Logic)
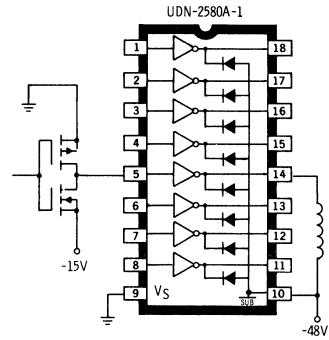
UDN-2580A-1

DWG. NO. A-11,538

MULTIPLEXED RELAY DRIVER

UDN-2956A
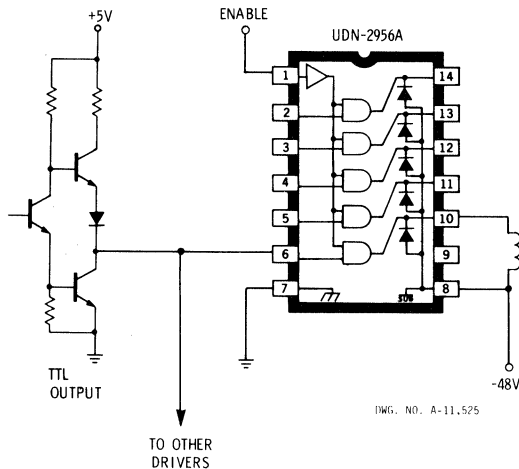
DWG. NO. A-11,525

PRINTER APPLICATIONS

S PRAGUE SOURCE DRIVERS have been used extensively in electrosensitive, thermal, and impact printer applications. Multi-channel devices in the Series UDN-2580A and UDN-2980A reduce parts count and provide up to 350 mA per output at voltages up to 75 V (resistive load). Copper lead frames make these devices capable of simultaneously delivering up to 125 mA continuously from all eight channels at an ambient temperature of +50°C.

RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage Range, V_S
  UDN-2588A-1 . . . . to 75 V
  UDN-2981A and UDN-2982A . . . . 5 V to 45 V
  UDN-2983A and UDN-2984A . . . . 35 V to 75 V
Logic Voltage, V_{IN} . . . . 12 V
Continuous Output Current, I_{OUT} (per output) . . . . . . −350 mA
Peak Output Current, I_{OP} . . . . −500 mA

3

THERMAL PRINTER APPLICATION
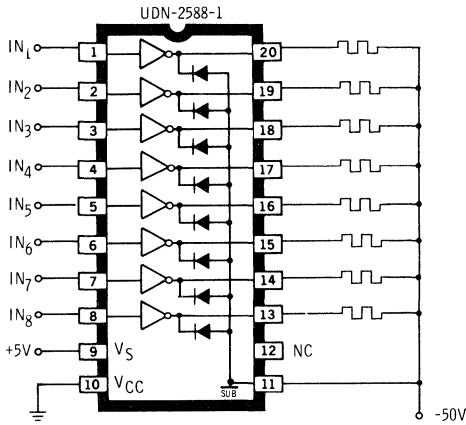
UDN-2588-1

DWG.NO. A-11,530

ELECTROSENSITIVE PRINTER APPLICATION

UDN-2983/84A

PRINT ELECTRODES
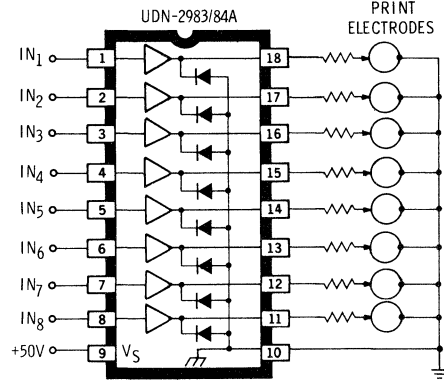
DWG.NO. A-11,529

ELECTRO-MECHANICAL DISPLAY APPLICATIONS

SOURCE DRIVERS in the Series UDN-2580A and UDN-2980A, when combined with the Type ULN-2804A sink driver, provide a simple interface between 12 V CMOS logic and a multiplexed electro-mechanical display. As shown, the need for additional inverter packages is eliminated since Type UDN-2580A is activated by a low input level and Type UDN-2982A is turned ON by a high input input level. All drivers have internal inductive-load transient-suppression diodes and copper lead frames for improved package power dissipation capability.

RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage, V_S .... 35 V
Continuous Output Current, I_{OUT} (per output) ...... −350 mA

MULTIPLEXED ELECTRO-MECHANICAL DISPLAY DRIVERS
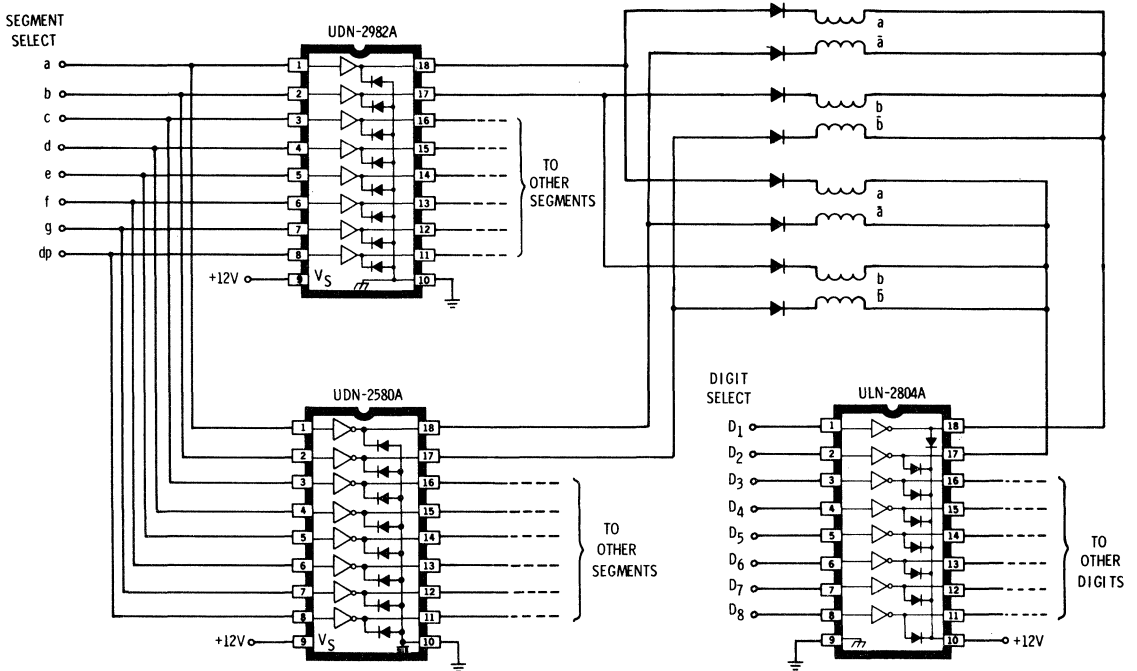
DWG.NO. B-1476

VACUUM-FLUORESCENT/GAS-DISCHARGE DISPLAY APPLICATIONS

S PRAGUE SERIES UDN-6100A and UDN-2580A source drivers provide solutions to problems encountered in driving higher-voltage vacuum-fluorescent and planar gas-discharge displays. Both series of parts provide TTL, CMOS, and NMOS input-logic compatibility. Series UDN-6100A devices are active high (non-inverting) drivers. Series UDN-2580A drivers are active low (inverting) devices.

At minimum cost, Series UDN-6100A-2 devices offer 60 V output breakdowns for vacuum-fluorescent displays typically utilizing less than 32 characters. Featuring a minimum 80 V output breakdown voltage, standard Series UDN-6100A drivers (no additional suffix) guarantee 25 mA per output. Suffix -1 devices provide for a 110 V breakdown, recommending them for 40 to 80-digit or dot-matrix V-F applications or gas-discharge anode-drive applications requiring the higher output voltage. All of these drivers include internal pull-

down resistors and provide operation from single-ended positive supplies.

Operation from a split-supply allows the user to bias the V-F filament at ground potential or to utilize a system-supply voltage above ground (± 40 V instead of $+80$ V). Either Type UDN-6138A or Type UDN-6148A source drivers are recommended.

For vacuum-fluorescent display applications requiring a higher current capability (operating several displays with common drive circuitry), Type UDN-2588A can be used with appropriate external output pull-down resistors to provide up to 350 mA per output.

3

MAXIMUM OPERATING VOLTAGES

V_S V_{BB}	$V_{IN(ON)}$	$V_{IN(OFF)}$	V_{CC}	$V_{EE(MAX)}$	Device Type
+5	<1.4	>4.5	0	−45	UDN-2588A
				−75	UDN-2588A-1
+12	<8.4	>11.5	0	−45	UDN-2588A
				−75	UDN-2588A-1
+30	2.4	<0.4	NA	−30	UDN-6138A-2
	4.0	<0.4	NA	−30	UDN-6148A-2
+40	2.4	<0.4	NA	−40	UDN-6138A
	4.0	<0.4	NA	−40	UDN-6148A
+60	TTL or CMOS		NA	0	Series UDN-6100A-2
+80	TTL or CMOS		NA	0	Series UDN-6100A
+110	TTL or CMOS		NA	0	Series UDN-6100A-1

GAS-DISCHARGE DISPLAY DRIVERS
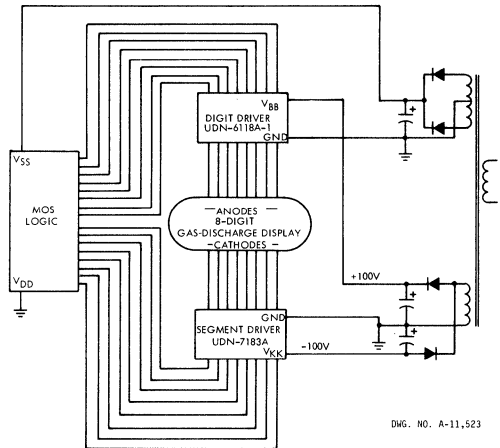
DWG. NO. A-11,523

MULTIPLEXED VACUUM-FLUORESCENT DISPLAY DRIVERS
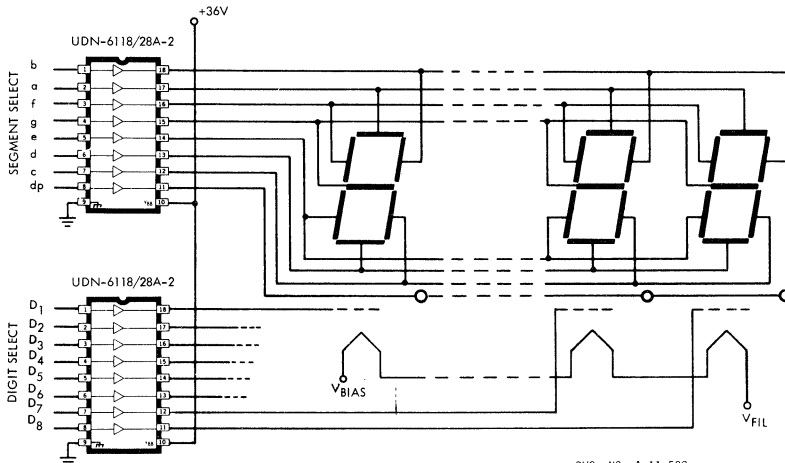
DWG. NO. A-11,522

VACUUM-FLUORESCENT/GAS-DISCHARGE DISPLAY APPLICATIONS
(Continued)

VACUUM-FLUORESCENT DISPLAY DRIVERS
(Split Supply)

DWG. NO. B-1472

*FOR ±36V SUPPLY,
USE UDN-6138A

DWG. NO. A-11,526

3—150
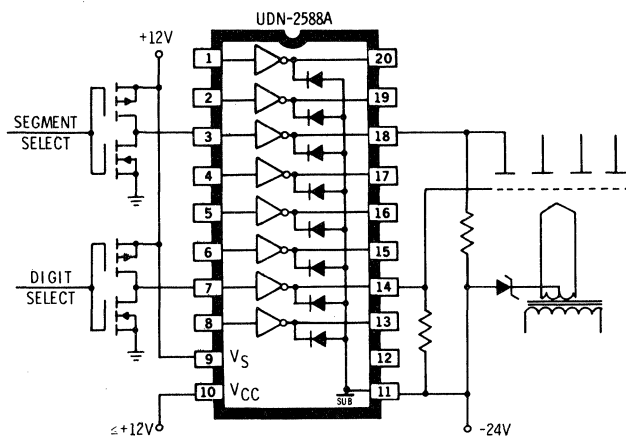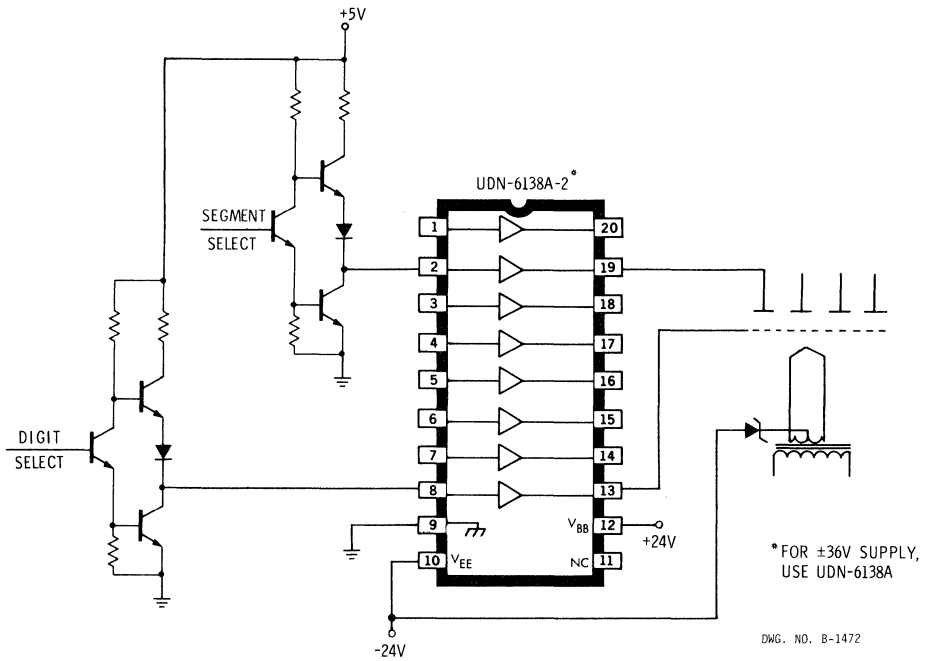
INCANDESCENT LAMP DRIVER APPLICATIONS

DRIVING MULTIPLEXED incandescent lamps at voltages up to 75 V with peak currents approaching 500 mA per segment, Series UDN-2980A eight-channel source drivers, when combined with Type ULN-2069B sink drivers, provide for a very cost-effective approach. Multiplexed lamps must typically be operated at a voltage $\sqrt{N}$ (N = the number of digits) times the nominal d-c voltage, to obtain sufficient brightness. For example, a four-digit, 28 V display requires 56 V to operate satisfactorily. In addition, care must be taken to select a proper driver to withstand the substantial inrush currents created by cold filaments. Peak currents of up to ten times the nominal operating currents have been observed. Multiplexed lamps must also incorporate diodes to prevent series/parallel paths to unaddressed elements.

RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage Range, V_S
  UDN-2981A and UDN-2982A . . . . 5 V to 45 V
  UDN-2983A and UDN-2984A . . . . 35 V to 75 V
Continuous Output Current, I_{OUT} (per output) . . . . . . −350 mA
Peak Output Current, I_{OP} . . . . −500 mA

3

MULTIPLEXED LAMP DRIVER, TTL- OR MOS-COMPATIBLE

DWG.NO. B-1475
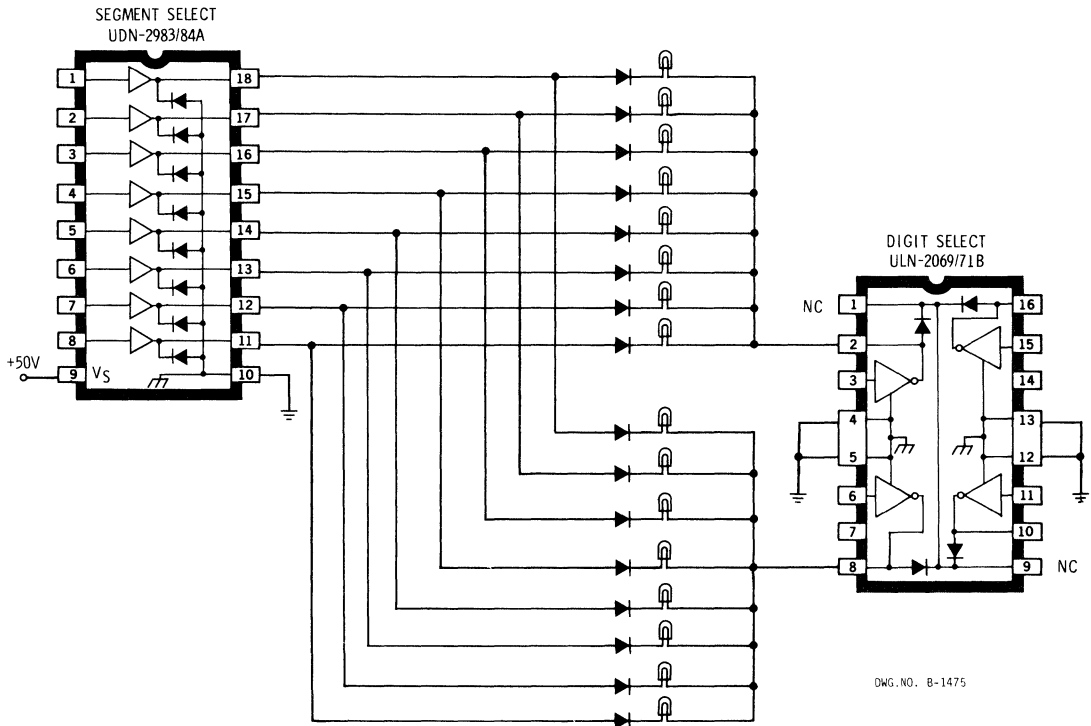
LIGHT-EMITTING DIODE APPLICATIONS

SERIES UDN-2580A and Series UDN-2980A 8-channel source drivers provide monolithic solutions to problems associated with driving multiplexed LED displays in common-cathode or common-anode configurations.

Type UDN-2585A is a non-Darlington inverting (input low = output high) source driver that is frequently used as a segment or dot driver in a common-cathode LED display where multiplexed segment or dot currents do not exceed 120 mA. This device features input logic-level compatibility with open-collector TTL, standard TTL, CMOS, and NMOS, as well as low output saturation voltages.

For common-cathode applications requiring higher segment currents, or for common-anode digit drive applications, Series UDN-2980A is recommended. This non-inverting (input high = output high) series features 350 mA per output continuous current ratings with peak currents reaching 500 mA per output. Outputs may be paralleled for higher current capability. Type UDN-2982A is logic-compatible with 2.4 V output levels of TTL and CMOS. Similar high output current ratings, for use in inverting applications, are offered by the Type UDN-2580A driver.

Combining Sprague source drivers with multichannel, high-current sink drivers (such as Type ULN-2068B, UDN-2595A, or ULN-2814A) provides simple, compact, and economical solutions to driving high-current multiplexed LED displays.

RECOMMENDED MAX. OPERATING CONDITIONS

Supply Voltage, V_S
UDN-2585A . . . . 15 V
UDN-2982A . . . . 45 V
Continuous Output Current, I_{OUT} (per output)
UDN-2585A . . . . −120 mA
UDN-2982A . . . . −350 mA
Input Voltage, V_{IN} . . . . 15 V

COMMON-CATHODE LED DISPLAY

COMMON-CATHODE LED DISPLAY

Dwg. No. B-1473A
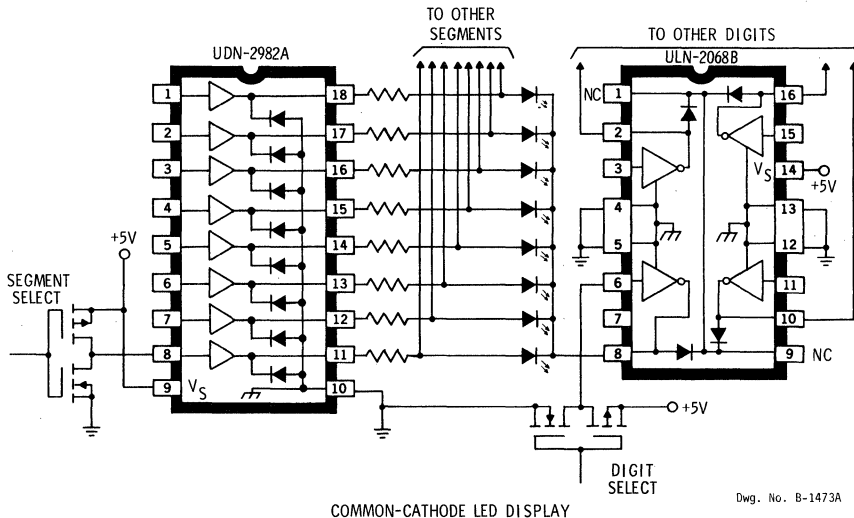
LIGHT-EMITTING DIODE APPLICATIONS
(Continued)

COMMON-CATHODE LED DISPLAY
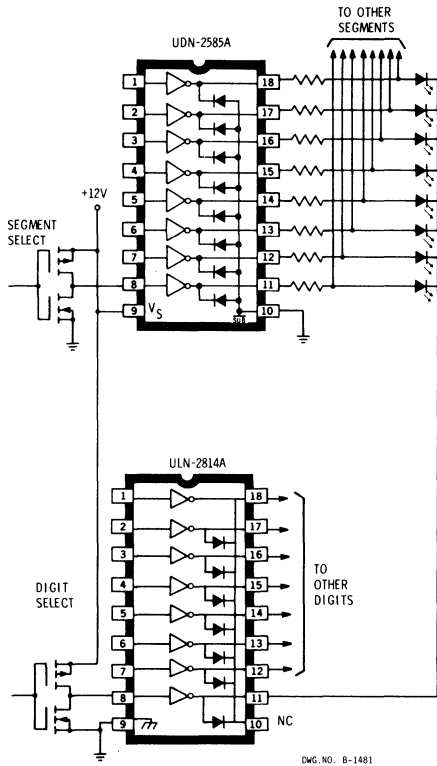
COMMON-ANODE LED DISPLAY

DWG.NO. B-1481

DWG. NO. B-1480
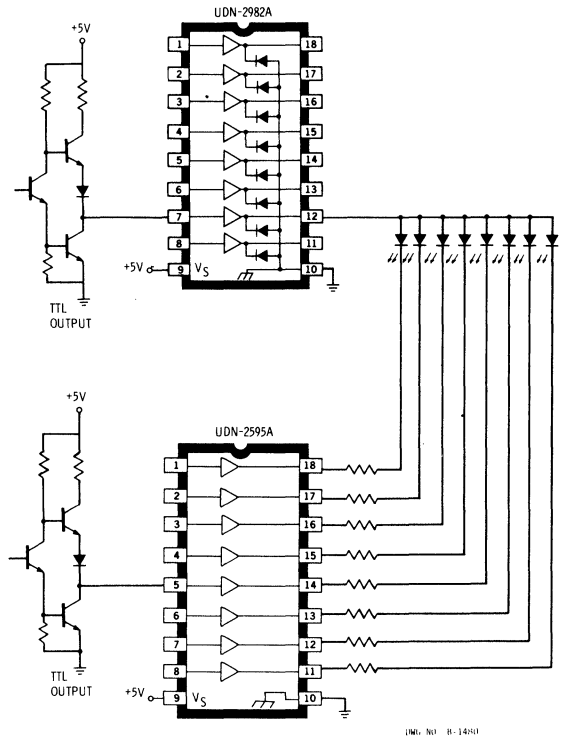
MULTI-CHANNEL INTERFACE TO HIGH-POWER LOADS

S PRAGUE SOURCE DRIVERS can be employed as multi-channel pre-drivers for discrete high-current or high-voltage semiconductors, thus reducing the need for many discrete components. For instance, a UDN-2580A 8-channel source driver can provide up to 350 mA of pre-drive current into the base of power NPN devices, making 5 A load currents readily available. Higher load currents can be obtained by using power NPN Darlington devices.

For a-c loads, it is possible to use any of the Sprague source drivers to provide gate current (with appropriate current-limiting) to a power SCR or triac. This scheme can provide an economical solution to many applications such as driving incandescent lamps or a-c motors at up to 20 A.

DRIVER FOR HIGH-POWER DISCRETE DEVICES
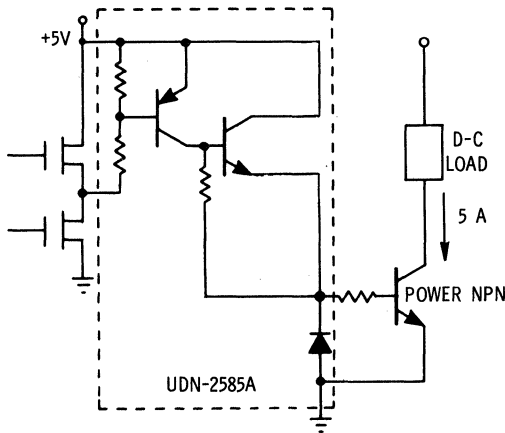
DWG.NO. A-11,533
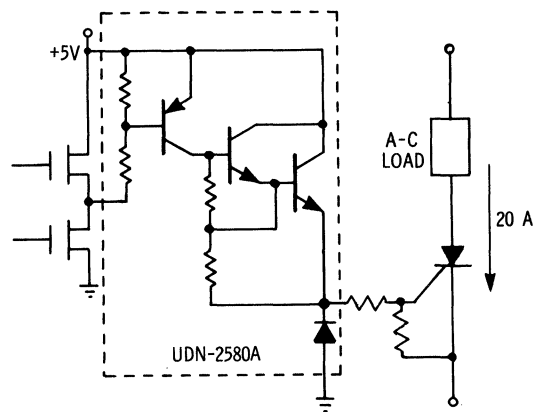
DWG.NO. A-11,534

NEW POWER-INTERFACE ICs

Introduction

In a continuing effort to maintain industry leadership as a producer of innovative power-interface chips, Sprague Electric Company recently introduced four new monolithic interface integrated circuits intended for medium-power switching applications. These power ICs provide integrated multi-channel interface between low-level TTL, CMOS, NMOS, and PMOS logic families, or microprocessor output ports, and medium-power peripheral loads such as relays, solenoids, displays, and motors at currents of up to 1.5 A and at voltages of up to 140 V.[1]

The four new integrated circuits are:

UDN-2585A Octal Source Driver (20 V, 120 mA per channel)
Primarily used as a segment/dot driver in common-cathode multiplexed LED display applications.

UDN-2595A Octal Sink Driver (20 V, 100 mA per channel)
Primarily a segment/dot driver in common-anode multiplexed LED display applications or as a medium-power buffer circuit to provide interface between various logic families and loads (voltage step-up, voltage step-down, current step-up).

UDN-6514A Octal Source Driver (140 V, 25 mA per channel)
Primarily for use in high-voltage display applications such as driving the grids or anodes of the newer large matrix vacuum-fluorescent display panels used for graphics.

UDN-2541B Quad NAND Sink Driver (60 V, 1.5 A per channel)
Primarily a general-purpose high-current, high-voltage interface between TTL, CMOS, PMOS, and NMOS logic and stepper motors, incandescent lamps, or relays.

All of these drivers add a level of system integration that offers these benefits:

Parts-Count Reduction
Printed Wiring Board Area Reduction
Insertion-Cost Reduction
System-Reliability Improvement
Performance Improvement
Overall System-Cost Reduction

The success of devices such as those described in this paper reaffirms customer needs to simplify designs, reduce costs, and improve overall system performance and reliability through the use of power integrated circuits.

[1]Simultaneous operation at these voltage and current limits is not available with a single device.

UDN-2585A
Octal Source Driver

The UDN-2585A evolved from a need to drive segments/dots of multiplexed (common-cathode) LED displays. Typical multiplexed LED segment/dot currents range from 50 mA to 100 mA, depending on LED digit size, number of multiplexed digits, and required display brightness. Frequently, these displays must operate with 5 V supplies. Moderate output-current requirements, combined with a need for low output-saturation voltage, suggest that a non-Darlington approach would provide an adequate solution for this application. It should be noted here that source functions are inherently more difficult to integrate.

A schematic for one of the eight UDN-2585A channels is shown in Figure 1. This source driver is an active-low, inverting device with input-drive requirements consistent with TTL, CMOS, and open-drain NMOS levels. The PNP input requires only 1.6 mA at 0.4 V (+5 V logic system, V_S = 5 V) to switch the output fully to the 120 mA output-current level. Input-limiting resistors as well as pull-up resistors are internal to the device.

DWG.NO. A-11,360
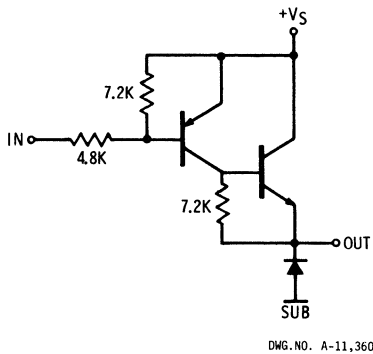
Figure 1
UDN-2585A PARTIAL SCHEMATIC

In the multiplexed mode, the supply voltage (+5 V) can be broken down into four components:

1. Source Driver Output ON voltage
2. Sink Driver Output ON Voltage
3. LED Forward Voltage
4. Current-Limiting Resistor Voltage Drop

A red LED running in saturation (for uniform display brightness) should be driven at approximately 2.0 V with the remaining voltage divided between the other three elements. Operating from a 5.0 V supply dictates that driver voltage drops be kept to a minimum so that adequate display brightness can be achieved and sufficient "headroom" voltage remains for the required current-limiting resistors.

A 4-digit, 7-segment plus decimal point LED display drive is shown in Figure 2 and requires only two IC drivers. Typical segment currents might be as high as 120 mA, with peak digit currents approaching 1 A (7-segment plus dp × 120 mA). The UDN-2585A source driver features a guaranteed 1.2 V maximum saturation voltage at 120 mA; the ULN-2068B sink driver has a guaranteed 1.3 V maximum at 1 A (see Sprague Electric Engineering Bulletins 29316 and 29305, respectively). With the LED operating at 2.0 V, this leaves 0.5 V across the 4.3Ω current-limiting resistor.

Dwg. No. B-1514
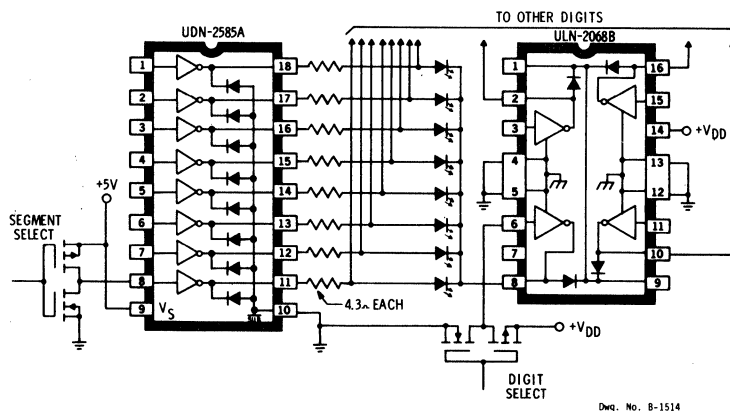
Figure 2
COMMON-CATHODE LED DRIVER

$$R_{LIMIT} = \frac{V_S - V_{SAT(SOURCE)} - V_{SAT(SINK)} - V_{F(DIODE)}}{I_{F(DIODE)}}$$

If source-sink drivers with higher saturation voltages are used, display brightness and uniformity will be somewhat reduced. The UDN-2585A is supplied in a plastic dual in-line package with copper lead frame that permits all eight output drivers to be ON simultaneously and continuously at 120 mA and a +70°C ambient.

This device can also be used to drive discrete semiconductors such as a power NPN or SCR (Figure 3). With a current-sourcing capability of 120 mA, load currents up to approximately 2.5 A can be handled with a vanilla-grade NPN and up to 20 A using a power SCR. These schemes provide economical solutions to many peripheral-power applications such as driving incandescent lamps or a-c motors, at 20 A or greater, with Darlingtons and sensitive-gate SCRs.

The UDN-2585A can be defined as an evolutionary device rather than revolutionary product. Although the device does not break any technological barriers (in terms of semiconductor processing or eiectrical capabilities), it does have merit in many applications where an economical current-source function is needed.

UDN-2595A
Octal Sink Driver

As with the UDN-2585A source driver, the UDN-2595A current-sink driver is intended for use as a segment/dot driver in multiplexed (common-cathode) LED display applications. A two-chip approach for driving an 8-digit, 8-segment red LED display is shown in Figure 4. Combining the UDN-2595A sink driver with the UDN-2982A source driver provides an interface between 5 V TTL, CMOS, or NMOS, and a 50 mA/segment, 400 mA/digit LED display. The UDN-2595A sink driver features a guaranteed 0.5 V saturation voltage at 50 mA; the UDN-2982A source driver has an approximate 2.0 V saturation rating at 400 mA (see Sprague Electric Engineering Bulletins 29320 and 29310, respectively). The 8Ω current-limiting resistor's value is determined from the same equation as used for the previous application.

Currents of up to 120 mA per segment or 1 A per digit can be obtained by paralleling outputs.

In addition to its LED display applications, the UDN-2595A can also be used as a logic translator (NMOS/CMOS, CMOS/TTL, or NMOS/TTL) or low-level current booster. These applications are shown in Figure 5.
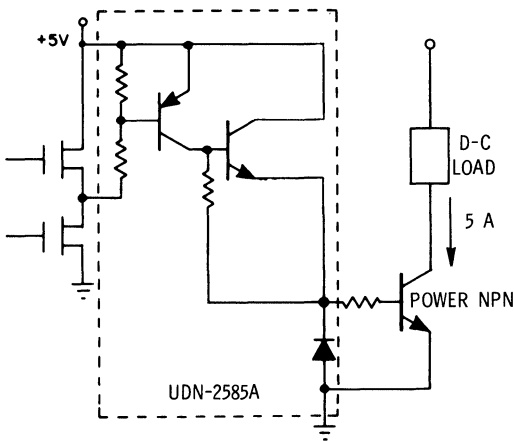
DWG.NO. A-11,533
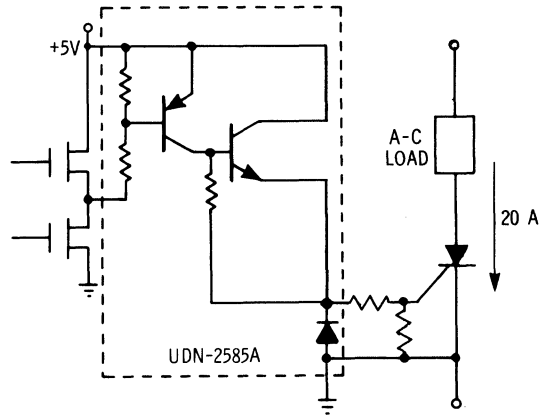
Dwg. No. A-12,064

Figure 3
DRIVER FOR HIGH-POWER APPLICATIONS
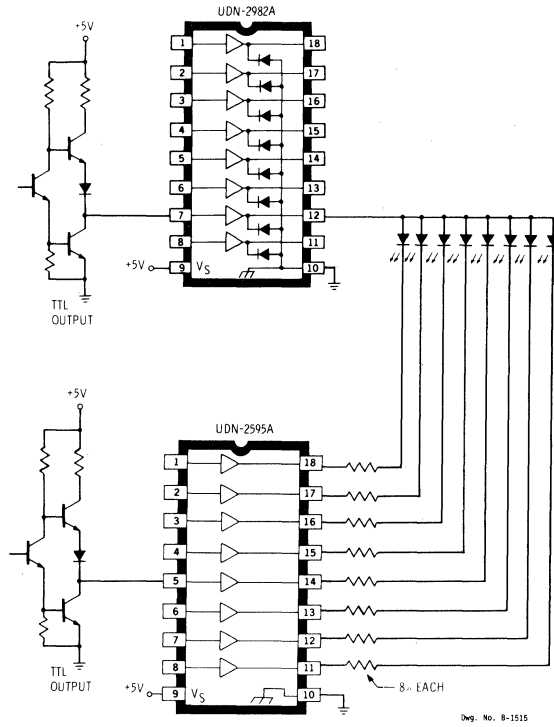
Figure 4
COMMON-ANODE LED DRIVER
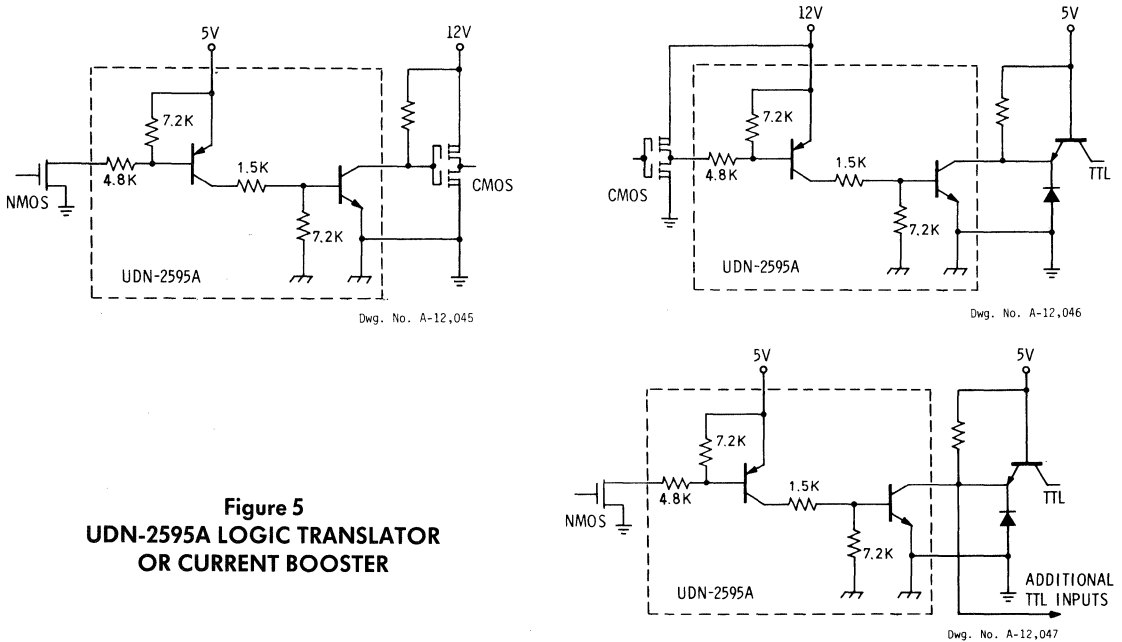
Figure 5
**UDN-2595A LOGIC TRANSLATOR
OR CURRENT BOOSTER**

Combining the UDN-2595A sink driver with the UDN-2585A source driver can also provide a low-voltage (15 V, maximum) bipolar stepper-motor drive circuit as shown in Figure 6. Paralleling the outputs of each device provides 200 mA to 400 mA of drive capability. The non-Darlington outputs of both devices enable low-voltage operation and maintain low power dissipation at reasonable current levels. For inductive load transient protection, external flyback diodes must be used for the UDN-2595A. Clamp diodes are internal to the UDN-2585A.

Input-drive requirements for the UDN-2595A are consistent with TTL, CMOS, and NMOS logic families. Only 1.6 mA (at 0.4 V) of logic sink current is required to turn the UDN-2595A output ON at the 100 mA level ($V_S = 5$ V). A schematic for one of the UDN-2595A sink-driver channels is shown in Figure 7. The UDN-2595A is supplied in a plastic dual in-line package with a copper lead frame providing package power dissipation capability of up to 2.2 W at +25°C. All eight output drivers are allowed ON

Dwg. No. A-11,408
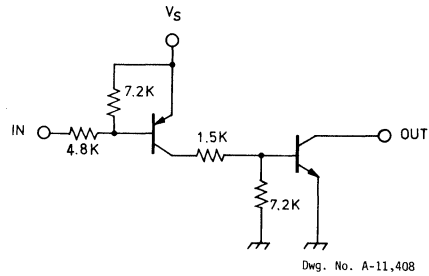
Figure 7
UDN-2595A PARTIAL SCHEMATIC

continuously and simultaneously with load currents of 200 mA at ambient temperatures up to +85°C.

The UDN-2595A octal sink driver provides a basic "nuts and bolts" building-block function for a variety of applications requiring the advantages of system integration.

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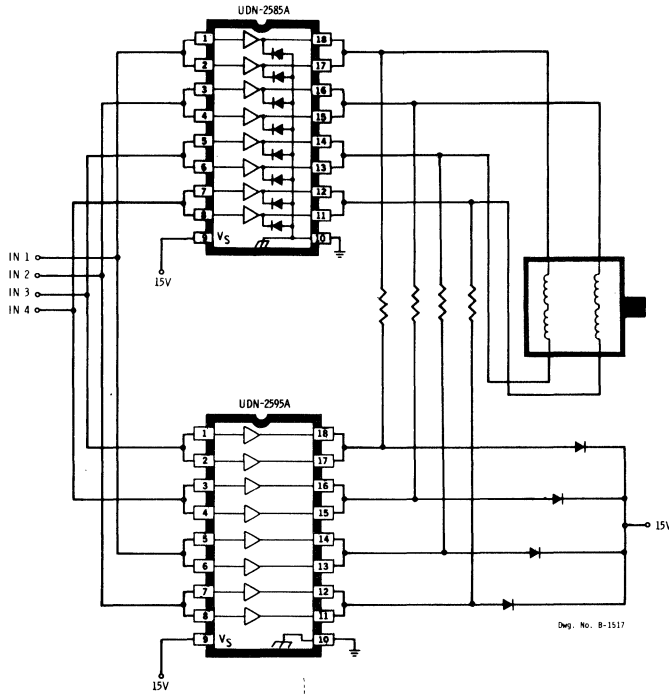
Figure 6
STEPPER-MOTOR DRIVER

UDN-6514A
Octal High-Voltage Source Driver

The UDN-6514A is an 8-channel non-inverting, active-high, current-source driver capable of switching 140 V supplies with output currents of up to 40 mA. Standard bipolar technology produces output-voltage breakdowns greater than 140 V in a monolithic integrated design while maintaining costs well below that of dielectrically-isolated devices. Typical applications for this device include driving anodes or grids of large vacuum-fluorescent matrix display panels (Figure 8). Note that external pull-down resistors must be included to provide the full 140 V output-voltage swing. In addition to VF display applications, the UDN-6514A has been used in ink-jet printer applications.

A simplified schematic for the UDN-6514A octal high-voltage source driver is shown in Figure 9. Input-drive requirements are compatible with TTL or CMOS operating at 5 V. A 10 kΩ input impedence ensures that the input current will not exceed 225 μA with 2.4 V applied. Complete electrical specifications are given in Sprague Electric Engineering Bulletin 29313.3.

Figure 9
UDN-6514 PARTIAL SCHEMATIC

As with all Sprague Electric plastic dual in-line packaged power integrated circuits, this device is supplied with a copper lead frame. This allows the maximum possible package power dissipation while ensuring the lowest possible junction temperature for maximum reliability. All eight outputs are allowed to source 25 mA continuously and simultaneously with ambient temperatures up to +64°C.

Sprague Electric Company has manufactured high-voltage, low-current, sink drivers since 1973. The 140 V, medium-current, UDN-6514A source driver represents another step forward in the ongoing pursuit of high-voltage capability in monolithic integrated designs. With the availability of high-voltage monolithic integrated circuits such as the UDN-6514A, many designs thought to be "discrete only" can now be made simpler and less expensive through integration.

UDN-2541B
Quad NAND High-Current Sink Driver

The UDN-2541B quad NAND high-current sink driver is a 60 V, 1.5 A per output device with non-Darlington saturated outputs. This driver is primarily intended as a general-purpose, high-power, four-channel driver for incandescent lamps, relays, and stepper motors. Its most important features are a non-Darlington saturated output driven by a variable current source operating from the logic-supply voltage. This provides a much more efficient approach to handling load-inrush currents associated with incandescent and inductive loads, and minimizes drive-current/power requirements.

Figure 8
MULTIPLEXED DOT-MATRIX
VACUUM-FLUORESCENT DISPLAY DRIVER

The typical Darlington driver, with a constant-current first stage, although capable of high output currents, tends to have high output-saturation voltage levels. It also usually requires approximately 6 mA of first stage drive supply current, regardless of output-current level.

The non-Darlington constant-current drive method features a relatively low output-saturation voltage, but requires approximately 20 mA of first stage drive supply current, regardless of output-current level.

The UDN-2541B uses a non-Darlington output and a variable-output base-drive current that is a function of output current. Therefore, operating at low output current requires minimum base-drive current (approximately 1 mA to 2 mA). At high output currents, the base-drive current will rise only to the level required to keep the output driver in saturation (less than 19 mA drive for 750 mA output). Complete specifications are given in Sprague Electric Engineering Bulletin 29317. This technique combines the high-current capability of a Darlington output with the low saturation voltage of a non-Darlington, and reduces the circuit power dissipation by limiting the base-drive current to what is required to drive the output into saturation.
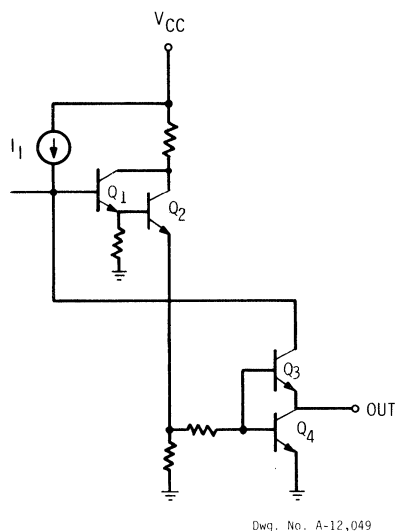
The output structure of the UDN-2541B sink driver is illustrated in Figure 10. Current source I1 supplies drive current to a Darlington drive circuit, Q1 and Q2, which drives output transistor Q4. With the collector voltage of Q4 equal to or less than 0.7 V, transistor Q3 is partially ON. Transistor Q3 bypasses a portion of the I1 current source from the first stage Darlington and steers it through Q4 to ground. Should the Q4 collector rise above approximately 0.7 V (indicating the need for more base drive), Q3 begins to turn OFF and a greater portion of the I1 current is driven through Q1 and Q2 and amplified to provide more base drive to output transistor Q4. Thus, supply current is optimized to the amount of base drive required to keep Q4 in saturation.

Input-drive requirements for the UDN-2541B are well below TTL, CMOS, PMOS, or NMOS drive capabilities (20 μA source at 2.0 V, 10 μA sink at 0.8 V). The modified bat-wing package allows all four drivers to be operated simultaneously and continuously at 750 mA output current at +25°C with a supply voltage of 5 V. Higher package power dissipation can be achieved through the use of a heat sink attached to the center webbed leads of the package. Typical applications for this device include driving incandescent lamps and d-c stepper motors. Incandescent lamps with steady-state current ratings up to 125 mA can be driven with no current-limiting or warming resistors (assumes 1.5 A peak inrush). The internal diodes can be used to perform a "lamp test" function as shown in Figure 11. Bifilar (unipolar) stepper motors running at up to 35 V, 1.5 A per phase, can be driven directly with the UDN-2541B device. Internal transient-suppression diodes prevent damage to the output transistor from positive high-voltage inductive spikes as the output switches OFF. Figure 12 depicts a typical drive circuit with input waveforms to control a 35 V, 1.5 A per phase unipolar stepper motor using the ENABLE pin of the UDN-2541B as a simple STOP/GO function.

The UDN-2541B quad NAND-gate power driver represents a continued effort to improve the performance of power interface integrated circuits by developing techniques to deal with problems associated with device and packaging power limitations. At the same time, these new techniques do not significantly add to overall device cost. The user is, therefore, offered a proposition not frequently encountered in today's marketplace: The opportunity to get more for less.

3

Dwg. No. A-12,049

Figure 10
UDN-2541B PARTIAL SCHEMATIC

Dwg. No. A-12,048
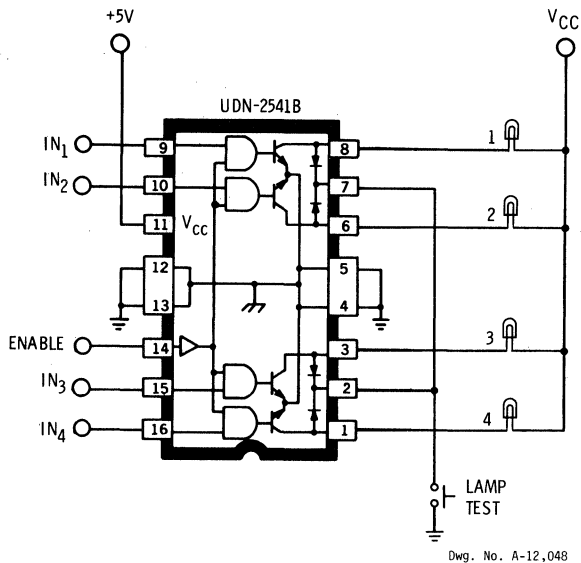
Figure 11
INCANDESCENT LAMP DRIVER

INPUT WAVEFORMS

Dwg. No. A-11,795

Dwg. No. A-11,796
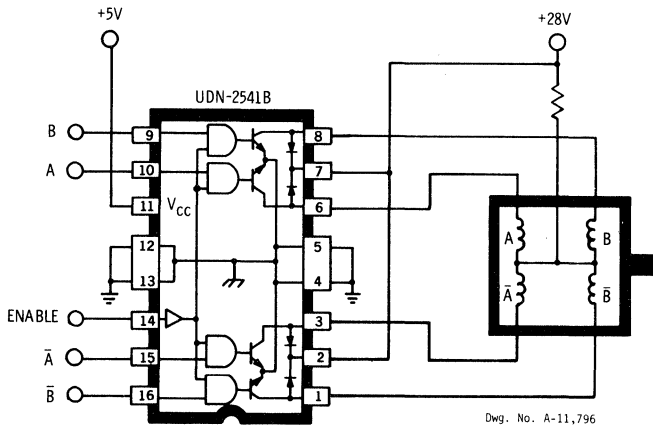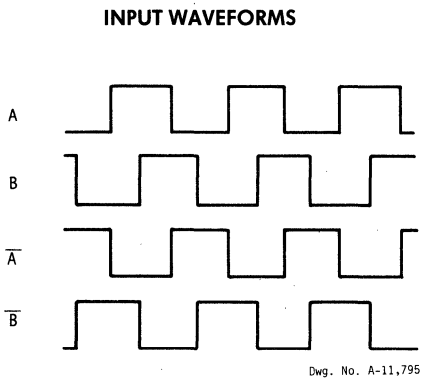
Figure 12
STEPPER-MOTOR DRIVER

SECTION 4 — BiMOS AND COMPLEX ARRAY INTERFACE DRIVERS

*New Product. Contact factory for detailed information.

4

UCN-4202A AND UCN-4203A
STEPPER-MOTOR TRANSLATORS AND DRIVERS

FEATURES

- 600 mA Output Current
- Full-Step or Double-Step Operation
- Single-Input Direction Control
- Power-On Reset
- Internal Transient Suppression
- Schmitt Trigger Inputs

DESIGNED TO DRIVE permanent-magnet step-per motors with current ratings of up to 500 mA, these integrated circuits employ a full-step, double-pulse drive scheme that allows use of up to 90 percent of available motor torque. The two devices differ only in output-voltage ratings: Type UCN-4202A has a 20 V breakdown-voltage rating and a 15 V sustaining voltage rating; Type UCN-4203A has a 50 V breakdown-voltage rating and a 35 V sustaining voltage rating.

Both drivers are bipolar I²L designs containing approximately 100 logic gates, TTL-compatible input/output circuitry, and 600 mA outputs with internal transient suppressors. The devices operate with a minimum of external components.

The four-phase stepper-motor load is controlled by step-logic functions. To step the load from one position to the next, STEP INPUT is pulled down to a logic low for at least 1 μs, then allowed to return to a logic high. The step logic is activated on the positive-going edge, which in turn activates one of the four current-sink outputs. DIRECTION CONTROL determines the sequence of states (A-B-C-D or A-D-C-B).

In the full-step mode, the MONOSTABLE RC timing pin is tied to V_{CC}, making states B and D stationary. A separate input pulse is required to move through each of the four output states.

In the double-step mode, states B and D are transition states with duration determined by MONOSTABLE RC timing. Improved motor torque is ob-
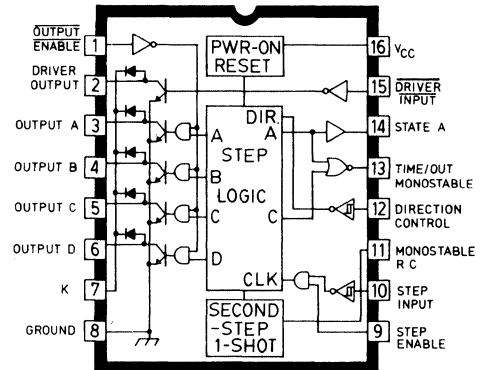
DWG. NO. A-11,184

tained at double the nominal motor step angle, and motor stability is improved for high step rates.

Higher current ratings, or bipolar operation, can be obtained by using Type UCN-4202A or UCN-4203A as a logic translator to drive integrated motor drivers (Sprague Type UDN-2949Z or UDN-2952B/W) or discrete high-power transistors.

ABSOLUTE MAXIMUM RATINGS
at $T_A = +25°C$

Supply Voltage, V_{CC} . . . . 7.0 V

V_K (UCN-4202A) . . . . 20 V

(UCN-4203A) . . . . 50 V

Output Voltage, V_{OUT} (UCN-4202A) . . . . 20 V

(UCN-4203A) . . . . 50 V

Input Voltage, V_{IN} . . . . 7.0 V

Output Sink Current, I_{OUT} . . . . 600 mA

Power Dissipation, P_D (One Driver) . . . . 0.8 W

(Total Package) . . . . 2.0 W*

Operating Temperature Range, T_A . . . . −20°C to +85°C

Storage Temperature Range, T_S . . . . −55°C to +150°C

Derate at the rate of 16.6 mW/°C above +25°C.

RECOMMENDED OPERATING CONDITIONS

Characteristic	UCN-4202A			UCN-4203A			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage, V_{CC}	4.5	5.0	5.5	4.5	5.0	5.5	V
V_K	—	12	13.5	—	30	35	V
Output Voltage, V_{CE}	—	—	13.5	—	—	35	V
Output Sink Current, I_{OUT}	—	—	500	—	—	500	mA
Operating Temperature, T_A	0	25	70	0	25	70	°C

MAXIMUM COLLECTOR CURRENT
AS A FUNCTION OF MOTOR TIME CONSTANT
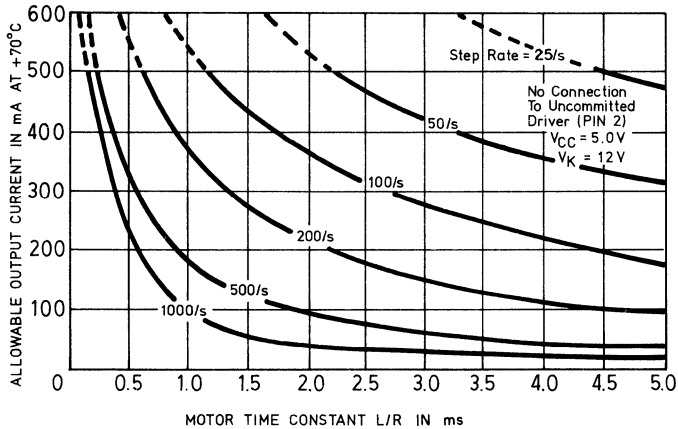
DWG. NO. A-11,185

Notes: 1. Values shown take into account static d-c losses ($V_{SAT}I_{OUT}$ and $V_{CC}I_{CC}$) as well as switching losses induced by inductive flyback through the clamp diodes at $V_K =$ 12 V. Maximum package power dissipation is assumed to be 1.33 W at +70°C. Higher package power dissipation may be obtained at lower operating temperatures.

2. Use of external discrete flyback diodes will eliminate power dissipation resulting from switching losses and will allow the full 500 mA output capability (Output A, B, C, or D and the Driver Output) under all conditions.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = +5.0$ V (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Supply Current	I_{CC}	All	2 Drivers ON	—	85	mA
TTL Inputs (Pins 1, 9, and 15), TTL Outputs (Pins 13 and 14)						
Input Voltage	$V_{IN(1)}$	All	$V_{CC} = 4.5$ V	2.0	—	V
	$V_{IN(0)}$	All	$V_{CC} = 5.5$ V	—	0.8	V
Input Current	$I_{IN(1)}$	All	$V_{CC} = 5.5$ V, $V_{IN} = 2.4$ V	—	40	μA
	$I_{IN(0)}$	All	$V_{CC} = 5.5$ V, $V_{IN} = 0.4$ V	—	−1.6	mA
Input Clamp Voltage	V_{IK}	All	$I_{IN} = -12$ mA	—	−1.5	V
Output Voltage	$V_{OUT(1)}$	All	$V_{CC} = 4.5$ V, $I_{OUT} = 80$ μA	2.4	—	V
	$V_{OUT(0)}$	UCN-4202A	$V_{CC} = 4.5$ V, $I_{OUT} = 3.2$ mA	—	0.4	V
		UCN-4203A	$V_{CC} = 4.5$ V, $I_{OUT} = 1.5$ mA	—	0.4	V
Output Current	$I_{OUT(SC)}$	All	$V_{CC} = 5.5$ V, $V_{OUT} = 0$	—	38	mA
Second-Step Monostable RC Input (Pin 11)						
Time Constant	t_{RC}	All		0.95	1.3	s/RC
Reset Voltage	V_{MR}	All	$R = 200$ kΩ, $I_{IN} = 25$ μA	—	50	mV
Reset Current	I_{MR}	All	$V_{IN} = 2.0$ V	40	—	μA
Schmitt Trigger Inputs (Pins 10 and 12)						
Threshold Voltage	V_{T+}	All		1.3	2.1	V
	V_{T-}	All		0.6	1.1	V
Hysteresis	ΔV_T	All		0.2	—	V
Input Current	$I_{IN(1)}$	All	$V_{CC} = 4.5$ V, $V_{IN} = 2.4$ V, $T_A = 25°C$	—	5.0	μA
		All	$V_{CC} = 4.5$ V, $V_{IN} = 2.4$ V, $T_A = 70°C$	—	40	μA
	$I_{IN(0)}$	All	$V_{CC} = 5.5$ V, $V_{IN} = 0.4$ V	—	−1.6	mA
Input Clamp Voltage	V_{IK}	All	$I_{IN} = -12$ mA	—	−1.5	V
Open Collector Outputs (Pins 2, 3, 4, 5, and 6)						
Output Leakage Current	I_{CEX}	UCN-4202A	$V_{CC} = 5.5$ V, K = Open, $V_{OUT} = 20$ V	—	500	μA
		UCN-4203A	$V_{CC} = 5.5$ V, K = Open, $V_{OUT} = 50$ V	—	500	μA
Output Saturation Voltage	$V_{CE(SAT)}$	UCN-4202A	$V_{CC} = 4.5$ V, $I_{OUT} = 300$ mA	—	500	mV
			$V_{CC} = 4.5$ V, $I_{OUT} = 400$ mA	—	750	mV
			$V_{CC} = 4.5$ V, $I_{OUT} = 500$ mA	—	900	mV
		UCN-4203A	$V_{CC} = 4.5$ V, $I_{OUT} = 300$ mA	—	850	mV
			$V_{CC} = 4.5$ V, $I_{OUT} = 400$ mA	—	1100	mV
			$V_{CC} = 4.5$ V, $I_{OUT} = 500$ mA	—	1350	mV
Output Sustaining Voltage	$V_{CE(SUS)}$	UCN-4202A	$I_{OUT} = 30$ mA, $t_p \leq 300$ μs, Duty Cycle $\leq 2\%$	15	—	V
		UCN-4203A	$I_{OUT} = 30$ mA, $t_p \leq 300$ μs, Duty Cycle $\leq 2\%$	35	—	V
Turn-On Delay	t_{pd0}	All	0.5 E_{in} (Pin 10) to 0.5 E_{out}	—	10	μs
Turn-Off Delay	t_{pd1}	All	0.5 E_{in} (Pin 10) to 0.5 E_{out}	—	10	μs
Clamp Diode Leakage Current	I_R	UCN-4202A	$V_R = 20$ V	—	50	μA
		UCN-4203A	$V_R = 50$ V	—	50	μA
Clamp Diode Forward Voltage	V_F	All	$I_F = 500$ mA	—	3.0	V

FUNCTIONAL DESCRIPTION

Power-On Reset

An internal RS flip-flop sets the Output A "ON" with the initial application of power. This state occurs approximately 30 μs after the logic supply voltage reaches 4 V with supply rise times of up to 10 ms/V. Once reset, the circuit functions according to the logic input conditions.

Step Enable

Pin 9 (STEP ENABLE) must be held high to enable the step pulses for advancing the motor to reach the translator logic clock circuits. Pulling this pin low inhibits the translator logic.

Step Input

Pin 10 (STEP INPUT) is normally high. The logic will advance one position on the positive transition after the input has been pulled low for at least 1 μs. The STEP INPUT current specification is compatible with NMOS and CMOS.

Direction Control

The direction of output rotation is determined by the logic level at pin 12. If the input is held high the rotation is A-D-C-B; if pulled low the rotation is A-B-C-D. This input is also NMOS and CMOS compatible.

Output Enable

Outputs A through D are inhibited (all outputs OFF) when pin 1 (OUTPUT ENABLE) is at high level. This condition creates a potential for wired-OR device outputs, or other potential control functions such as chopping or bi-level drive.

Transient Suppression

All five power outputs are diode protected against inductive transients. Zener diode or resistor "flyback" transient suppression is often used, provided the peak output voltage does not exceed the sustaining voltage rating of the device (15 V for Type UCN-4202A or 35 V for Type UCN-4203A).

Full-Step/Double-Step

Full-step operation is the most commonly used drive technique. The devices are capable of unipolar drive without external active devices, either in a full-step mode (pin 11, Monostable RC, tied high), or in a double-step mode (pin 11 connected to RC timing). The double-step mode provides improved torque characteristics, while the specified angular increment is doubled.

FULL-STEP MODE
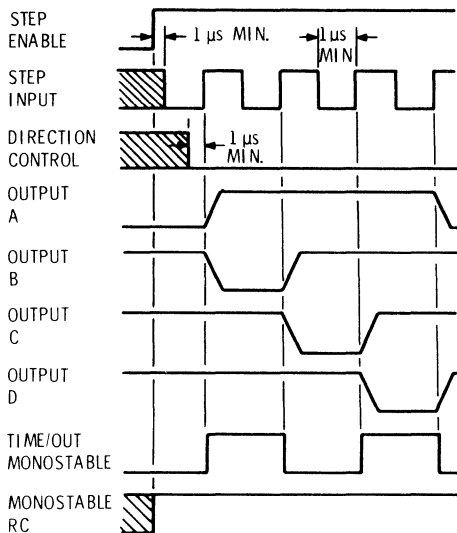
DOUBLE-STEP MODE
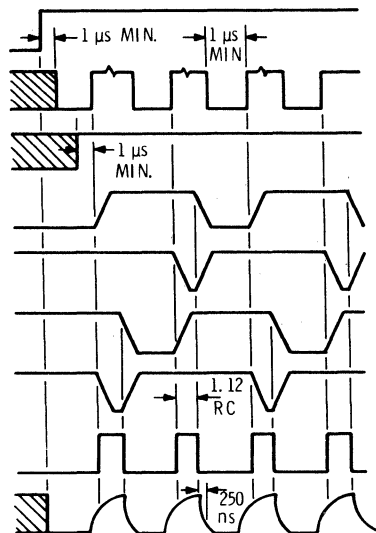
Dwg. No. A-11,844

STEPPER MOTORS
(Representative List)

Manufacturer	Model	L/R	Typ. Ratings	Step
Eastern Air	LA23ACK-2	1.4 ms	440 mA, 12 V	1.8°
Devices	LA23ACK-3	1.25 ms	220 mA, 24 V	1.8°
	LA23ACY-1	1.2 ms	440 mA, 12 V	7.5°
	LA34ADK-6	2.6 ms	530 mA, 14 V	1.8°
IMC	S-114	1.6 ms	340 mA, 12 V	7.5°
Hanson	S-115	1.9 ms	130 mA, 12 V	7.5°
	S-382	1.6 ms	171 mA, 24 V	7.5°
	S-406	4.3 ms	280 mA, 24 V	15°
	S-451	3.9 ms	280 mA, 24 V	7.5°
North American	K82701-P2	1.5 ms	330 mA, 12 V	7.5°
Phillips	K83701-P2	1.5 ms	330 mA, 12 V	15°
Septor	S-0912A	1.5 ms	340 mA, 12 V	9°
Superior	M061-FD-301	0.8 ms	440 mA, 12 V	1.8°
Electric	M061-FD-311	1.5 ms	220 mA, 20 V	1.8°

TYPICAL APPLICATIONS

CHOPPER DRIVE CIRCUIT
Used to Drive a 12 V, 500 mA
Unipolar Stepper Motor

Dwg. No. B-1498
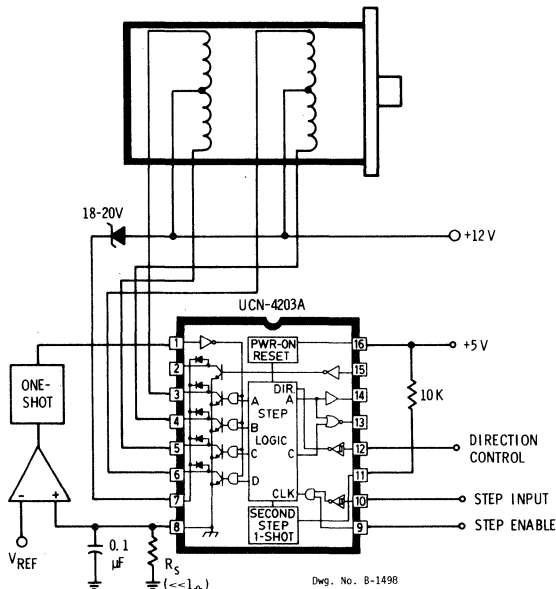
DISC DRIVE
APPLICATIONS

These stepper-motor translator/drivers provide additional special-purpose logic for use in disc drive applications. Pin 14 (STATE A) is high with OUTPUT A activated and is used with other drive logic in determining Track 0 Position on the disc. Pin 13 (TIME/OUT MONOSTABLE) in disc drive applications is called ON TRACK and is low with either OUTPUT A or OUTPUT C activated. It is used as a WRITE ENABLE condition with other drive logic.

An independent driver (pins 2 and 15) is used to control the head load solenoid.

TYPICAL APPLICATIONS (Continued)

BIPOLAR DRIVE CIRCUIT
Used to Drive a 500 mA Stepper Motor

Dwg. No. B-1496A

TWO-PHASE BIPOLAR DRIVE CIRCUIT
Used to Drive a 2A Stepper Motor

$$R_S = 0.6/I_{OUT(MAX.)}$$

Dwg. No. B-1497

4—7

TYPICAL APPLICATIONS (Continued)

A-C MOTOR DRIVE CIRCUIT
Used to Drive a 2 A Synchronous Motor

Dwg. No. B-1447

UNIPOLAR TWO-PHASE DRIVE CIRCUIT
Used to Drive a 500 mA
Unipolar Stepper Motor

Dwg. No. B-1499

UCN-4401A AND UCN-4801A BiMOS LATCH/DRIVERS

FEATURES

- High-Voltage, High-Current Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

THESE high-voltage, high-current latch/drivers are comprised of four or eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. The UCN-4401A contains four latch/drivers while the UCN-4801A contains eight latch/drivers.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads.

Both units feature open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.

The UCN-4401A 4-latch device is furnished in a standard 14-pin dual in-line plastic package. The UCN-4801A 8-latch device is furnished in a 22-pin dual in-line plastic package with lead centers on 0.400″ (10.16 mm) spacing. All outputs are pinned opposite their respective inputs to simplify circuit board layout.
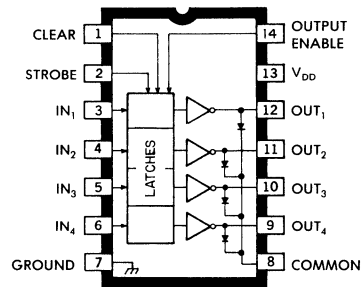
DWG. NO. A-10,499A

TYPE UCN-4401A
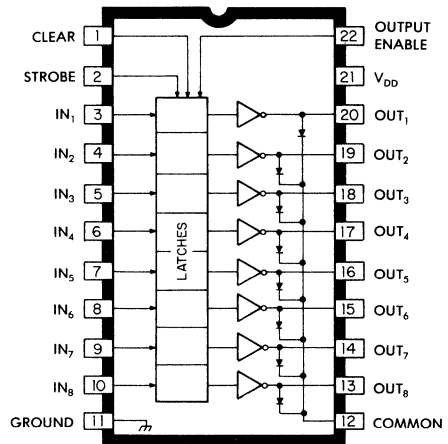
DWG. NO. A-10,498A

TYPE UCN-4801A
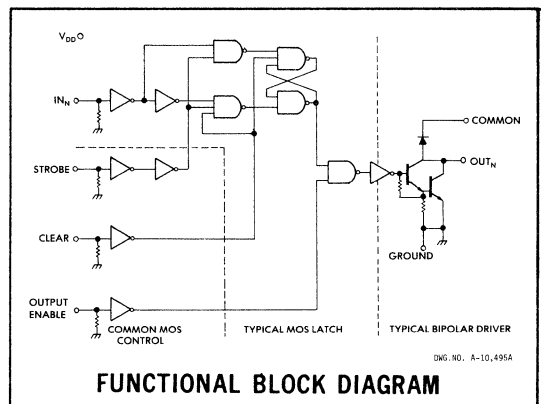
DWG. NO. A-10,495A

FUNCTIONAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE} . . . . 50 V
Supply Voltage, V_{DD} . . . . 18 V
Input Voltage Range, V_{IN} . . . . − 0.3 V to V_{DD} + 0.3 V
Continuous Collector Current, I_C . . . . 500 mA
Package Power Dissipation, P_D (UCN-4401A) . . . . 1.67 W*
(UCN-4801A) . . . . 2.0 W**
Operating Ambient Temperature Range, T_A . . . . − 20°C to + 85°C
Storage Temperature Range, T_S . . . . − 55°C to + 125°C

*Derate at the rate of 16.7 mW/°C above T_A = 25°C.
**Derate at the rate of 20 mW/°C above T_A = 25°C.

ELECTRICAL CHARACTERISTICS at T_A = + 25°C, V_{DD} = 5 V, V_{SS} = 0 V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	V_{CE} = 50 V, T_A = + 25°C	—	—	50	μA
		V_{CE} = 50 V, T_A = + 70°C	—	—	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100 mA	—	0.9	1.1	V
		I_C = 200 mA	—	1.1	1.3	V
		I_C = 350 mA, V_{DD} = 7.0 V	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	V_{DD} = 15 V	13.5	—	—	V
		V_{DD} = 10 V	8.5	—	—	V
		V_{DD} = 5.0 V (see note)	3.5	—	—	V
Input Resistance	R_{IN}	V_{DD} = 15 V	50	200	—	kΩ
		V_{DD} = 10 V	50	300	—	kΩ
		V_{DD} = 5.0 V	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each stage)	V_{DD} = 15 V	—	1.0	2.0	mA
		V_{DD} = 10 V	—	0.9	1.7	mA
		V_{DD} = 5.0 V	—	0.7	1.0	mA
	$I_{DD(OFF)}$	V_{DD} = 5.0 V, All Drivers OFF, All Inputs = 0 V	—	50	100	μA
		V_{DD} = 15 V, All Drivers OFF, All Inputs = 0 V	—	—	200	μA
Clamp Diode Leakage Current	I_R	V_R = 50 V, T_A = + 25°C	—	—	50	μA
		V_R = 50 V, T_A = + 70°C	—	—	100	μA
Clamp Diode Forward Voltage	V_F	I_F = 350 mA	—	1.7	2.0	V

*Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "1".

TRUTH TABLE

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant
t-1 = previous output state
t = present output state

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TIMING CONDITIONS

(Logic Levels are V_{DD} and V_{SS})

DWG.NO. A–10,895A

A. Minimum data active time before strobe enabled (data set-up time) . . . . .100 ns
B. Minimum data active time after strobe disabled (data hold time) . . . . .100 ns
C. Minimum strobe pulse width . . . . .300 ns
D. Typical time between strobe activation and output on to off transition . . . . .500 ns
E. Typical time between strobe activation and output off to on transition . . . . .500 ns
F. Minimum clear pulse width . . . . .300 ns
G. Minimum data pulse width . . . . .500 ns

CAUTION: Sprague CMOS devices feature input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

UCN-4805A BiMOS LATCHED DECODER/DRIVER

FEATURES

- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Hexadecimal Decoding
- Internal Pull-Up/Pull-Down Resistors
- Wide Supply Voltage Range

DESIGNED for use in high-voltage vacuum fluorescent display driver applications, the UCN-4805A latched decoder/driver combines CMOS logic with bipolar source outputs. The device consists of eight high-voltage bipolar sourcing outputs, with internal pull-down resistors and CMOS input latches, hexadecimal decoder, and control circuitry (strobe and blanking).

Type UCN-4805A is intended to serve as the segment driver with standard 7-segment displays incorporating a colon or decimal point. The integrated circuit uses hexadecimal decoding to display 0-9, A, b, C, d, E, and F.

This BiMOS latched decoder/driver has sufficient speed to permit operation with most microprocessor/LSI-based systems. The CMOS input latches provide operation over the supply voltage range of 5 to 15 V with minimum logic loading. Internal output pull-down resistors eliminate the need for external components usually required for fluorescent display applications. When used with standard TTL or low-speed TTL logic, the device may require employment of input pull-up resistors to insure a proper input logic high.
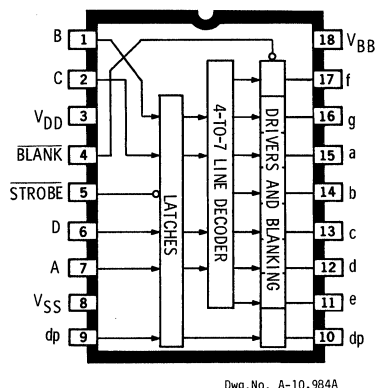
Dwg.No. A-10,984A

UCN-4805A

ABSOLUTE MAXIMUM RATINGS at +25°C
Free-Air Temperature and $V_{SS} = 0 V$

Output Voltage, V_{OUT} . . . . 60 V
Logic Supply Voltage Range, V_{DD} . . . . 4.5 V to 18 V
Driver Supply Voltage Range, V_{BB} . . . . 5.0 V to 60 V
Input Voltage Range, V_{IN} . . . . -0.3 V to $V_{DD} + 0.3$ V
Continuous Output Current, I_{OUT} . . . . -40 mA
Package Power Dissipation, P_D . . . . 1.82 W*
Operating Temperature Range, T_A . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . . $-55°C$ to $+125°C$
*Derate at the rate of 18.18 mW/°C above $T_A = 25°C$.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_{BB} = 60$ V, $V_{DD} = 4.75$ V to 15.75 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	850	μA
Output Leakage Current		$T_A = 70°C$	—	−15	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	5.3	V
		$V_{DD} = 15$ V	13.5	15.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = 5.0$ V	—	100	μA
		$V_{DD} = 15$ V	—	300	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	50	—	kΩ
Supply Current	I_{BB}	Display "8"	—	9.1	mA
		All outputs OFF	—	100	μA
	I_{DD}	$V_{DD} = I/O = $ STROBE $ = 5.0$ V, All other inputs $= 0$ V	—	200	μA
		$V_{DD} = I/O = $ STROBE $ = 15$ V, All other inputs $= 0$ V	—	500	μA
		$V_{DD} = $ STROBE $ = $ BLANK $ = 5.0$ V, Data latched, Display "8"	—	7.0	mA
		$V_{DD} = $ STROBE $ = $ BLANK $ = 15$ V, Data latched, Display "8"	—	21	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

Caution: Sprague CMOS devices feature input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

MAXIMUM ALLOWABLE DUTY CYCLE

Number of Outputs ON ($I_{OUT} = -25$ mA)	Max. Allowable Duty Cycle at Ambient Temperature of 50°C	60°C	70°C
8	100%	92%	78%
7	↑	100%	89%
6	↓	↕	100%
1	100%	100%	100%

UCN-4805A TRUTH TABLE

Inputs								Outputs							
D	C	B	A	dp	$\overline{BL}$	$\overline{ST}$	Character	a	b	c	d	e	f	g	dp
0	0	0	0	0	1	0	Zero	1	1	1	1	1	1	0	0
0	0	0	1	0	1	0	One	0	1	1	0	0	0	0	0
0	0	1	0	0	1	0	Two	1	1	0	1	1	0	1	0
0	0	1	1	0	1	0	Three	1	1	1	1	0	0	1	0
0	1	0	0	0	1	0	Four	0	1	1	0	0	1	1	0
0	1	0	1	0	1	0	Five	1	0	1	1	0	1	1	0
0	1	1	0	0	1	0	Six	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	Seven	1	1	1	0	0	0	0	0
1	0	0	0	0	1	0	Eight	1	1	1	1	1	1	1	0
1	0	0	1	0	1	0	Nine	1	1	1	0	0	1	1	0
1	0	1	0	0	1	0	A	1	1	1	0	1	1	1	0
1	0	1	1	0	1	0	b	0	0	1	1	1	1	1	0
1	1	0	0	0	1	0	C	1	0	0	1	1	1	0	0
1	1	0	1	0	1	0	d	0	1	1	1	1	0	1	0
1	1	1	0	0	1	0	E	1	0	0	1	1	1	1	0
1	1	1	1	0	1	0	F	1	0	0	0	1	1	1	0
X	X	X	X	1	1	0	dp	X	X	X	X	X	X	X	1
X	X	X	X	X	0	X	blank	0	0	0	0	0	0	0	0

X = irrelevant
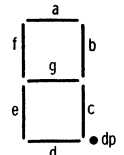
DWG. NO. A-10.985

TYPICAL INPUT CIRCUITS

$\overline{BL}$, $\overline{ST}$

Dwg. No. A-10,979A

A, B, C, D, dp

Dwg. No. A-10,980
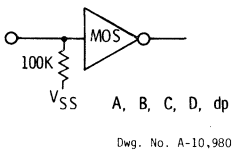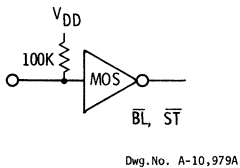
TYPICAL OUTPUT DRIVER
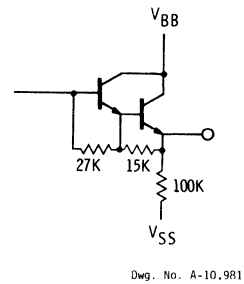
Dwg. No. A-10,981

TIMING CONDITIONS
(Logic Levels are V_{DD} and V_{SS})
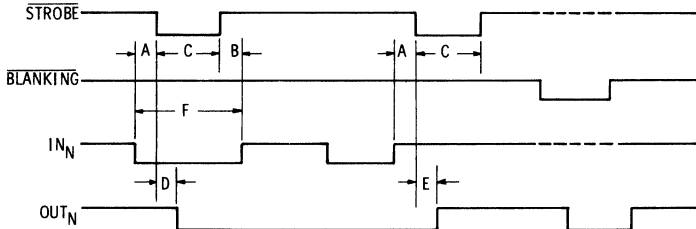
Dwg.No. A-10,982A

A. Minimum Data Active Time Before $\overline{\text{Strobe}}$ Enabled
   (Data Set-Up Time) .... 100 ns
B. Minimum Data Active Time After $\overline{\text{Strobe}}$ Disabled
   (Data Hold Time) .... 100 ns
C. Minimum $\overline{\text{Strobe}}$ Pulse Width .... 300 ns
D. Typical Time Between $\overline{\text{Strobe}}$ Activation and Output
   On to Off Transition .... 1.0 μs
E. Typical Time Between $\overline{\text{Strobe}}$ Activation and Output
   Off to On Transition .... 1.0 μs
F. Minimum Data Pulse Width .... 500 ns

Information present at an input is transferred to its latch when the $\overline{\text{STROBE}}$ ($\overline{\text{ST}}$) is low. The latches will continue to accept new data as long as the $\overline{\text{STROBE}}$ is held low. Applications where the latches are bypassed ($\overline{\text{STROBE}}$ tied low) ordinarily require that the $\overline{\text{BLANKING}}$ input be low between digit selection because of possible non-synchronous decoding.

When the $\overline{\text{BLANKING}}$ ($\overline{\text{BL}}$) input is low, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the $\overline{\text{BLANKING}}$ input high, the outputs are controlled by the latch/decoder circuitry.

UCN-4807A AND UCN-4808A
BiMOS ADDRESSABLE LATCHED DRIVERS

FEATURES

- Addressable Data Entry
- 50 V Current-Sink Outputs
- CMOS, PMOS, NMOS, TTL Compatible
- Low-Power CMOS Logic and Latches
- Wide Supply-Voltage Range

THESE 8-BIT, ADDRESSABLE, latched drivers are used in a wide variety of power demultiplexer applications. They can drive all types of common peripheral power loads, including lamps, relays, solenoids, LEDs, printer heads, heaters, and stepper motors. They can also be used as DMUX drivers for higher power loads requiring discrete power semiconductors.

Type UCN-4807A and UCN-4808A drivers are identical except for output current ratings. The former is rated for a maximum of 200 mA per output while the latter is capable of sinking up to 600 mA per output. The 50 V outputs are bipolar NPN saturated switches with first stage driver currents optimized for each version.

Each MSI array is comprised of a 3-bit to 8-line decoder, 8 type D latches, 8 open-collector output drivers, and MOS control circuitry for CHIP SELECT, CLEAR, and OUTPUT ENABLE functions. Any of the eight power loads can be addressed individually and can be turned ON or OFF independently of the other loads.

Dwg. No. A-11,783

Under normal operating conditions, all outputs of Type UCN-4807A can sustain 150 mA over the operating temperature range without derating. Type UCN-4808A will sustain 500 mA per output at 30°C and a duty cycle of 33%. Other combinations of number of outputs conducting and duty cycle are shown in the specifications.

These devices are supplied in 18-pin dual in-line plastic packages for operation over the temperature range of −20°C to +85°C. They are also available in industrial-grade ceramic packages (UCQ-4807R and UCQ-4808R) or in side-brazed, hermetically sealed packages to MIL-STD-883, Class B (UCS-4807H and UCS-4808H).

UCN-4808A DERATING

Number of Outputs ON (I_{OUT} = 500 mA)	Max. Duty Cycle (with V_{DD} = 5 V) at Ambient Temperature of				
	30°C	40°C	50°C	60°C	70°C
8	33%	29%	25%	21%	17%
7	37%	33%	29%	24%	20%
6	44%	39%	33%	28%	23%
5	52%	46%	40%	34%	28%
4	65%	58%	50%	42%	35%
3	87%	77%	67%	57%	46%
2	100%	100%	100%	85%	70%
1	100%	100%	100%	100%	100%

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature

Output Voltage, V_{OUT} . . . . 50 V
Logic Supply Voltage Range, V_{DD} . . . . 4.5 V to 18 V
Driver Supply Voltage Range, V_S . . . . 4.5 V to 5.5 V
Input Voltage Range, V_{IN} . . . . −0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} (UCN-4807A) . . . . . . 200 mA
                                (UCN-4808A) . . . . . . 600 mA
Package Power Dissipation, P_D . . . . 1.82 W*
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −55°C to +125°C

*Derate at the rate of 18.18 mW/°C above T_A = +25°C.

FUNCTIONAL BLOCK DIAGRAM

TYPICAL INPUT CIRCUITS

Dwg. No. A-11,913

UNUSED INPUTS SHOULD
BE TIED TO V_{DD} OR GROUND
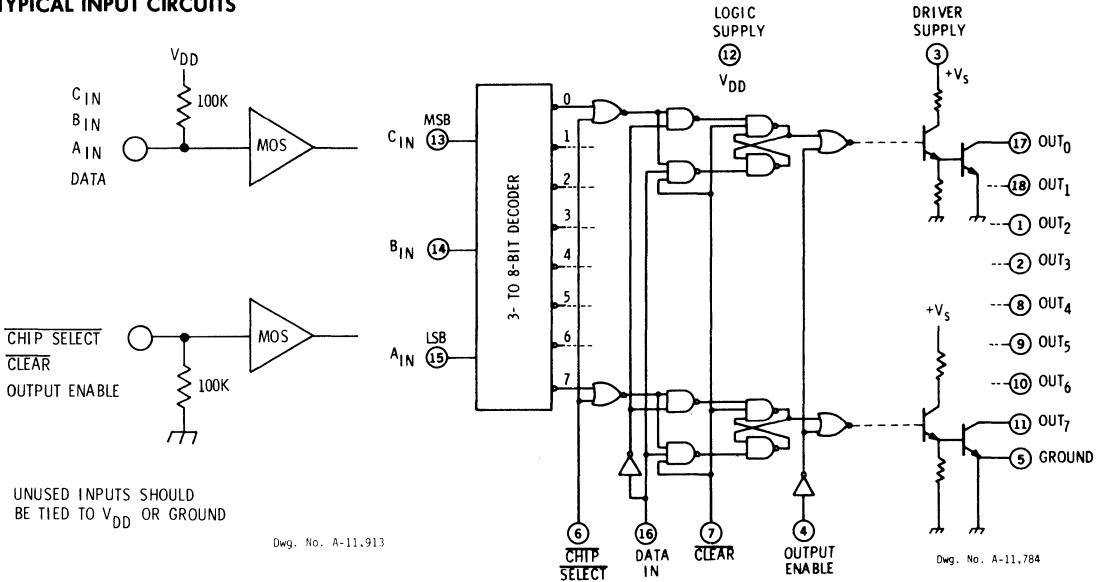
Dwg. No. A-11,784

Terminal Designation	Function
ADDRESS	A 3-bit binary address on these pins defines which one of the 8 latches is to receive the data. C_{IN} is the most-significant bit; A_{IN} is least significant.
$\overline{\text{CHIP SELECT}}$	When this input is low, the addressed output latch will accept data. When $\overline{\text{CHIP SELECT}}$ is high, the latches will retain their existing state, regardless of ADDRESS or DATA input conditions. This input should be held high while ADDRESS is being changed. $\overline{\text{CHIP SELECT}}$ also allows an additional level of address decoding.
DATA INPUT	When $\overline{\text{CHIP SELECT}}$ is low, the data bit present here is transferred to the addressed latch and output such that (when OUTPUT ENABLE is high) "1" turns the output ON and "0" turns the output OFF.
$\overline{\text{CLEAR}}$	When $\overline{\text{CLEAR}}$ goes from high to low, all latches are reset and outputs are turned OFF.
OUTPUT ENABLE	When this input is high, the outputs are controlled by their respective latches. When OUTPUT ENABLE is low, all outputs are OFF.
OUTPUTS	These are the 8 open-collector NPN outputs.
DRIVER SUPPLY	This is the supply voltage for the first stage of the bipolar output drivers. The nominal supply is 5.0 V.
LOGIC SUPPLY	This is the CMOS logic supply voltage input. Typically it is between 4.75 V and 15.75 V.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5$ V (unless otherwise specified)

Characteristic	Symbol	Test Conditions	UCN-4807A Min.	UCN-4807A Max.	UCN-4808A Min.	UCN-4808A Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 50$ V	—	50	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{OUT} = 50$ mA	—	0.2	—	—	V
		$I_{OUT} = 100$ mA	—	0.3	—	—	V
		$I_{OUT} = 150$ mA	—	0.4	—	—	V
		$I_{OUT} = 200$ mA	—	—	—	0.5	V
		$I_{OUT} = 350$ mA	—	—	—	0.7	V
		$I_{OUT} = 500$ mA	—	—	—	1.0	V
Input Voltage	$V_{IN(0)}$		—	0.8	—	0.8	V
	$V_{IN(1)}$	$V_{DD} = 15$ V	13.5	—	13.5	—	V
		$V_{DD} = 5$ V	3.5	—	3.5	—	V
Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD} = 15$ V	—	300	—	300	μA
		$V_{IN} = V_{DD} = 5$ V	—	100	—	100	μA
Input Resistance	R_{IN}		50	—	50	—	kΩ
Supply Current	$I_{DD(ON)}$	One Driver ON, $V_{DD} = 15$ V	—	5.0	—	5.0	mA
		One Driver ON, $V_{DD} = 5$ V	—	1.0	—	1.0	mA
	$I_{DD(OFF)}$	CLEAR = 0 V, SELECT = V_{DD} = 15 V	—	300	—	300	μA
		CLEAR = 0 V, SELECT = V_{DD} = 5 V	—	100	—	100	μA
	$I_{S(ON)}$	One Driver ON, $V_S = 5$ V	—	5.5	—	50	mA
		All Drivers ON, $V_S = 5$ V	—	45	—	160	mA
	$I_{S(OFF)}$	ENABLE = 0 V, $V_S = 5$ V	—	0.1	—	35	mA

Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure the minimum logic "I".
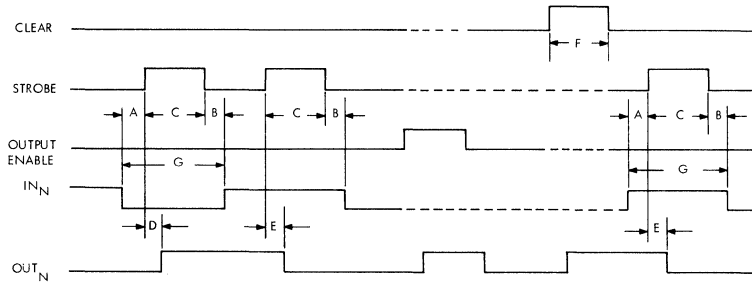
CAUTION: Sprague CMOS devices have input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

TRUTH TABLE

$\overline{CHIP}$ $\overline{SELECT}$	$\overline{CLEAR}$	DATA	C_{IN}	B_{IN}	A_{IN}	OUTPUT ENABLE	OUT_7	OUT_6	OUT_5	OUT_4	OUT_3	OUT_2	OUT_1	OUT_0	
X	L	X	X	X	X	X	H	H	H	H	H	H	H	H	Clear
H	H	X	X	X	X	H	R	R	R	R	R	R	R	R	Memory
L	H	D	L	L	L	H	R	R	R	R	R	R	R	$\overline{D}$	Address Latch 0
L	H	D	L	L	H	H	R	R	R	R	R	R	$\overline{D}$	R	Address Latch 1
L	H	D	L	H	L	H	R	R	R	R	R	$\overline{D}$	R	R	Address Latch 2
L	H	D	L	H	H	H	R	R	R	R	$\overline{D}$	R	R	R	Address Latch 3
L	H	D	H	L	L	H	R	R	R	$\overline{D}$	R	R	R	R	Address Latch 4
L	H	D	H	L	H	H	R	R	$\overline{D}$	R	R	R	R	R	Address Latch 5
L	H	D	H	H	L	H	R	$\overline{D}$	R	R	R	R	R	R	Address Latch 6
L	H	D	H	H	H	H	$\overline{D}$	R	R	R	R	R	R	R	Address Latch 7
X	X	X	X	X	X	L	H	H	H	H	H	H	H	H	Blanking
X	X	X	X	X	X	H	R	R	R	R	R	R	R	R	

L = Low Logic Level
H = High Logic Level
D = Data (High or Low)
X = Irrelevant
R = Previous State

I/O WAVEFORMS
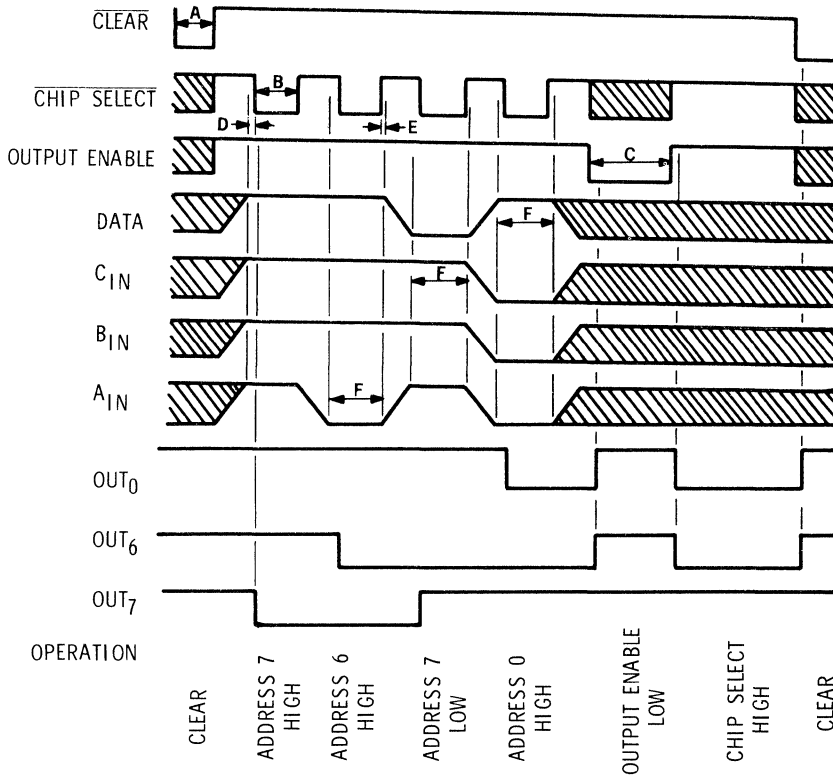
Dwg. No. A-11,785
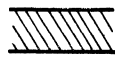
Logic Level
Irrelevant
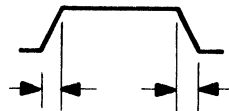
Allowable
Transition Time

TIMING CONDITIONS
(Logic Levels are V_{DD} and Ground)

A. Minimum CLEAR Pulse Width .... 300 ns
B. Minimum CHIP SELECT Pulse Width .... 500 ns
C. Typical OUTPUT ENABLE (Blanking) Pulse Width .... 5.0 μs
D. Minimum DATA or ADDRESS Setup Time .... 100 ns
E. Minimum DATA or ADDRESS Hold Time .... 100 ns
F. Minimum DATA or ADDRESS Pulse Width... 700 ns

4—19

TYPICAL APPLICATIONS

A typical application for Type UCN-4808A, driving a common-cathode LED display, is shown below. Many multi-character LED displays can make use of the high-current capability of this device. With the DATA input held high, the proper address code may be furnished by a 3-bit counter. Note that with DATA held constant and the ADDRESS sequenced through the binary code, setup and hold times associated with CHIP SELECT may be ignored.

The second application illustrates the use of Type UCN-4807A or UCN-4808A as a multiplexed power driver. A wide variety of peripheral loads including lamps, relays, solenoids, LEDs, and stepper motors can be accommodated. Inductive loads require external transient suppression.

These devices can also be employed as multi-channel drivers for discrete high-current or high-voltage semiconductors.

Common-Cathode LED Display Driver

Dwg. No. B-1494
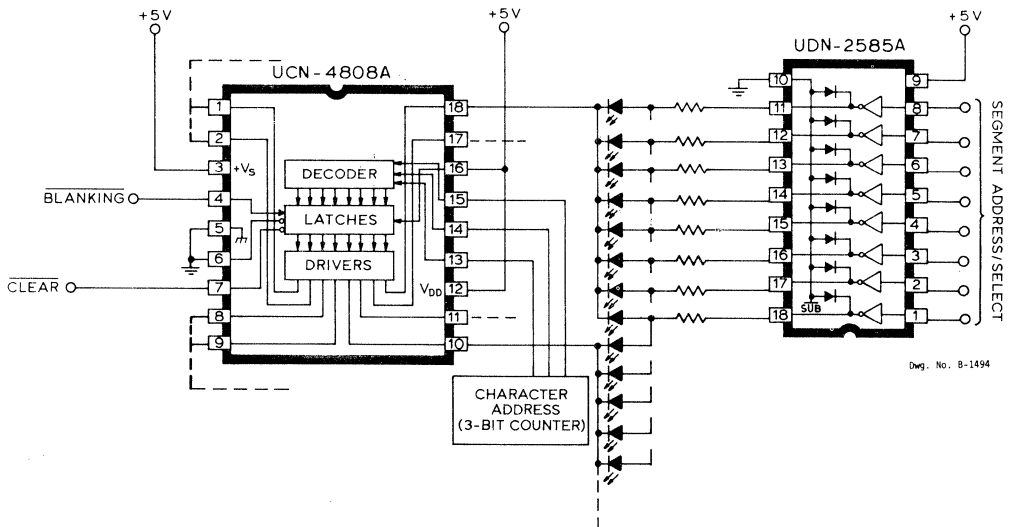
TYPICAL APPLICATIONS (Continued)

Multiplexed Power Driver

Dwg. No. B-1495
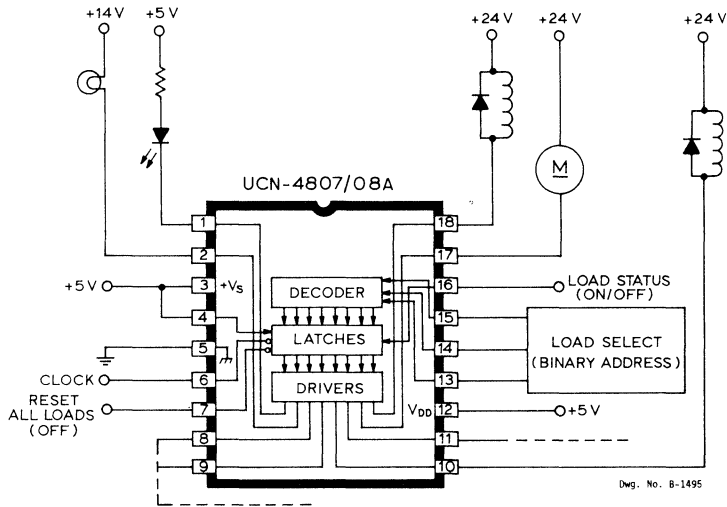
4

Multichannel Driver
for Discrete Power Semiconductors

Dwg. No. A-11,786
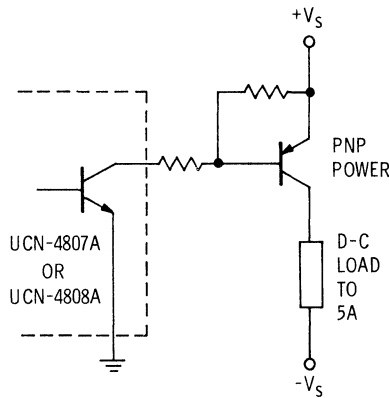
UCN-4810A
BiMOS 10-BIT SERIAL-INPUT, LATCHED DRIVER

FEATURES

- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Logic and Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range

COMBINING low-power CMOS logic with bipolar source drivers, the Type UCN-4810A integrated circuit simplifies many display systems. This BiMOS 10-bit serial-input, latched driver is primarily designed for use with vacuum-fluorescent displays, but can also be used with LED and incandescent displays within its output limitations of 60 V and 40 mA per driver.

Selected devices (UCN-4810A-1) have maximum output ratings of 80 V and 40 mA per driver. In all other respects, Type UCN-4810A-1 is identical to Type UCN-4810A.

The CMOS 10-bit shift register and associated latches are designed for operation over a supply-voltage range of 5 V to 15 V. They cause minimal loading and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or low-speed TTL, appropriate pull-up resistors may be required to ensure an input-logic high. A CMOS serial data output allows cascading these devices in multiple drive-line applications required by many dot matrix, alphanumeric, and bar graph displays.

The 10 bipolar outputs are used as segment or digit drivers in vacuum-fluorescent displays. Under normal operating conditions, the devices will source 25 mA per output at +50°C and a duty cycle of 85%. Other combinations of number of outputs conducting and duty cycle are shown in the specifications.
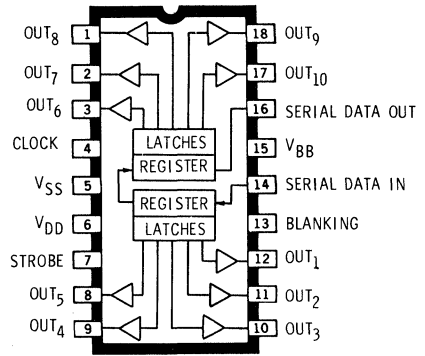
Dwg. No. A-10,988

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature and V_{ss} = 0 V

Output Voltage, V_{OUT} (UCN-4810A) . . . . 60 V
                 (UCN-4810A-1) . . . . 80 V
Logic Supply Voltage Range, V_{DD} . . . . 4.5 V to 18 V
Driver Supply Voltage Range, V_{BB}
                 (UCN-4810A) . . . . 5.0 V to 60 V
                 (UCN-4810A-1) . . . . 5.0 V to 80 V
Input Voltage Range, V_{IN} . . . . − 0.3 V to V_{DD} + 0.3 V
Continuous Output Current, I_{OUT} . . . . − 40 mA
Package Power Dissipation, P_D . . . . 1.82 W*
Operating Temperature Range, T_A . . . . − 20°C to + 85°C
Storage Temperature Range, T_S . . . . − 55°C to + 125°C

*Derate at the rate of 18.18 mW/°C above T_A = +25°C.

Number of Outputs ON (I_{OUT} = − 25 mA)	Max. Allowable Duty Cycle at Ambient Temperature of				
	+25°C	+40°C	+50°C	+60°C	+70°C
10	100%	97%	85%	73%	62%
9	100%	100%	94%	82%	69%
8	100%	100%	100%	92%	78%
7	100%	100%	100%	100%	89%
6	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

Caution: Sprague Electric CMOS devices have input static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 60\,V$, $V_{DD} = 4.75\,V$ to $15.75\,V$, $V_{SS} = 0\,V$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage	V_{OUT}	$I_{OUT} = -25\,mA$, $V_{BB} = 60\,V$	57.5	—	V
		$I_{OUT} = -25\,mA$, $V_{BB} = 80\,V$, UCN-4810A-1 only	77.5	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	850	μA
		$V_{OUT} = 80\,V$, UCN-4810A-1 only	550	1150	μA
Output Leakage Current	I_{OUT}	$T_A = +70°C$	—	-15	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0\,V$	3.5	5.3	V
		$V_{DD} = 15\,V$	13.5	15.3	V
	$V_{IN(0)}$		-0.3	$+0.8$	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0\,V$	—	100	μA
		$V_{DD} = V_{IN} = 15\,V$	—	300	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0\,V$	50	—	$k\Omega$
Serial Data Output Resistance	R_{OUT}	$V_{DD} = 5.0\,V$	—	20	$k\Omega$
		$V_{DD} = 15\,V$	—	6.0	$k\Omega$
Supply Current	I_{BB}	All outputs ON, All outputs open	—	13	mA
		All outputs OFF, All outputs open	—	200	μA
	I_{DD}	$V_{DD} = 5.0\,V$, All outputs OFF, All inputs $= 0\,V$	—	100	μA
		$V_{DD} = 15\,V$, One output ON, All inputs $= 0\,V$	—	200	μA
		$V_{DD} = 5.0\,V$, One output ON, All inputs $= 0\,V$	—	1.0	mA
		$V_{DD} = 15\,V$, One output ON, All inputs $= 0\,V$	—	3.0	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

TYPICAL INPUT CIRCUIT
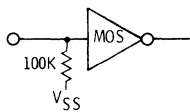
Dwg. No. A-10,980

TYPICAL OUTPUT DRIVER
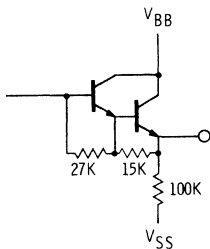
Dwg. No. A-10,981

FUNCTIONAL BLOCK DIAGRAM
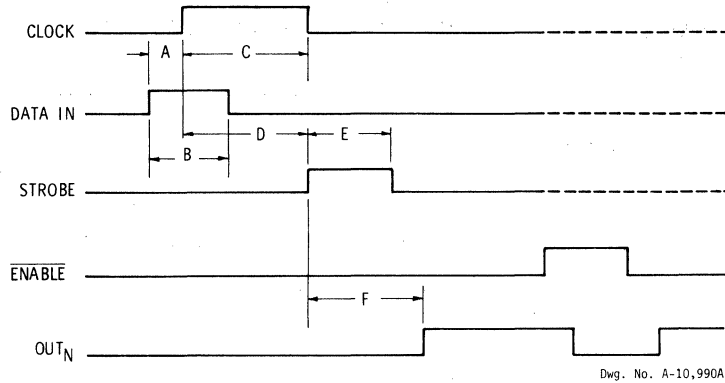
Dwg. No. A-10,989

Dwg. No. A-10,990A

TIMING CONDITIONS
(Logic Levels are V_{DD} and V_{SS})

		$V_{DD} = 5.0$ V	$V_{DD} = 15$ V
A.	Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	250 ns	150 ns
B.	Minimum Data Pulse Width	500 ns	300 ns
C.	Minimum Clock Pulse Width	600 ns	250 ns
D.	Minimum Time Between Clock Activation and Strobe	1.0 μs	400 ns
E.	Minimum Strobe Pulse Width	500 ns	300 ns
F.	Typical Time Between Strobe Activation and Output Transition	1.0 μs	1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SE-RIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will con-tinue to accept new data as long as the STROBE is held high. Applications where the latches are by-passed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, all of the out-put buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the BLANKING input low, the outputs are controlled by the state of the latches.

UCN-4810A TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents $I_1 I_2 I_3 \ldots \ldots I_8 I_9 I_{10}$	Serial Data Output	Strobe Input	Latch Contents $I_1 I_2 I_3 \ldots \ldots I_8 I_9 I_{10}$	Blanking Input	Output Contents $I_1 I_2 I_3 \ldots \ldots I_8 I_9 I_{10}$
H	⎍	$H\ R_1\ R_2 \ldots R_7\ R_8\ R_9$	R_9				
L	⎍	$L\ R_1\ R_2 \ldots R_7\ R_8\ R_9$	R_9				
X	⎍	$R_1\ R_2\ R_3 \ldots R_8\ R_9\ R_{10}$	R_{10}				
		$X X X \ldots \ldots X X X$	X	L	$R_1\ R_2\ R_3 \ldots R_8\ R_9\ R_{10}$		
		$P_1\ P_2\ P_3 \ldots P_8\ P_9\ P_{10}$	P_{10}	H	$P_1\ P_2\ P_3 \ldots P_8\ P_9\ P_{10}$	L	$P_1\ P_2\ P_3 \ldots P_8\ P_9\ P_{10}$
					$X X X \ldots \ldots X X X$	H	$L L L \ldots \ldots L L L$

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCN-4815A

BiMOS LATCH/SOURCE DRIVER

FEATURES
- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Internal Pull-Down Resistors
- Wide Supply Voltage Range

DESIGNED primarily for use with high-voltage vacuum fluorescent displays, the UCN-4815A BiMOS latch/source driver consists of eight NPN Darlington source drivers with pull-down resistors, a CMOS latch for each driver, and common strobe, blanking, and enable functions.

The CMOS inputs provide for minimum loading and are compatible with standard CMOS, PMOS, and NMOS logic commonly found in microprocessor designs. The use of CMOS latches also allows operation over a supply voltage range of 5 V to 15 V. When employed with either standard TTL or low speed TTL logic, the UCN-4815A may require the use of appropriate pull-up resistors.

The bipolar outputs may be used as segment, dot (matrix), bar, or digit drivers in vacuum fluorescent displays. All eight outputs can be activated simultaneously at ambient temperatures up to 60°C. To simplify circuit board layout, all outputs are pinned opposite their respective inputs.

A minimum component display subsystem, requiring few or no discrete components, may be realized by using the UCN-4815A BiMOS Latch/Source Driver with either a UCN-4805A or UCN-4806A latched hexadecimal decoder/drivers or a UCN-4810A serial-to-parallel latch/driver.
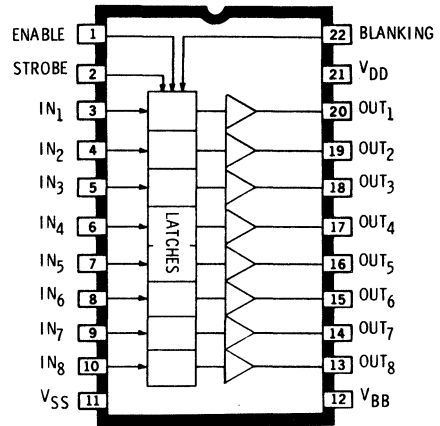
Dwg. No. A-10,987

ABSOLUTE MAXIMUM RATINGS at 25°C
Free-Air Temperature and $V_{SS} = 0$ V

Output Voltage, V_{OUT} .... 60 V
Logic Supply Voltage Range, V_{DD} .... 4.5 V to 18 V
Driver Supply Voltage Range, V_{BB} .... 5.0 V to 60 V
Input Voltage Range, V_{IN} .... −0.3 V to V_{DD} +0.3 V
Continuous Output Current, I_{OUT} .... −40 mA
Package Power Dissipation, P_D .... 2.0 W*
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −55°C to +125°C
*Derate at the rate of 20 mW/°C above T_A = 25°C.

| Number of Outputs ON ($I_{OUT} = -25$ mA)	Max. Allowable Duty Cycle at Ambient Temperature of		
	50°C	60°C	70°C
8	100%	100%	86%
7	↑	↑	98%
6			100%
1	100%	100%	100%

Caution: Sprague CMOS devices feature input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_{BB} = 60\,V$, $V_{DD} = 4.75\,V$ to $15.75\,V$, $V_{SS} = 0\,V$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25\,mA$	57.5	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	850	μA
Output Leakage Current		$T_A = 70°C$	—	−15	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0\,V$	3.5	5.3	V
		$V_{DD} = 15\,V$	13.5	15.3	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0\,V$	—	100	μA
		$V_{DD} = V_{IN} = 15\,V$	—	300	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0\,V$	50	—	$k\Omega$
Supply Current	I_{BB}	All outputs ON, All outputs open	—	10.5	mA
		All outputs OFF	—	100	μA
	I_{DD}	$V_{DD} = 5.0\,V$, All outputs OFF, All inputs = 0 V	—	100	μA
		$V_{DD} = 15\,V$, All outputs OFF, All inputs = 0 V	—	200	μA
		$V_{DD} = 5.0\,V$, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 15\,V$, One output ON, All inputs = 0 V	—	3.0	mA

NOTE: Positive (negative) current is defined as going into (coming out of) the specified device pin.

Dwg. No. A-10,980

TYPICAL INPUT CIRCUIT

UCN-4815A TRUTH TABLE

Inputs				OUT$_N$	
IN$_N$	STROBE	ENABLE	BLANK	T-1	T
0	1	1	0	X	0
1	1	1	0	X	1
X	X	X	1	X	0
X	0	X	0	1	1
X	0	X	0	0	0
X	X	0	0	1	1
X	X	0	0	0	0

X = irrelevant
T-1 = previous output state
T = present output state
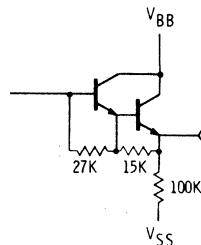
Dwg. No. A-10,981

TYPICAL OUTPUT DRIVER

TIMING CONDITIONS
(Logic Levels are V_{DD} and V_{SS})

Dwg. No. A-10,991

4

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) . . . . 100 ns
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) . . . . 100 ns
C. Typical Strobe Pulse Width For Power-Up Clear Disable . . . . 500 ns
    Minimum Strobe Pulse Width After Power-Up Clear Disabled . . . . 300 ns
D. Typical Time Between Strobe Activation and Output On to Off Transition . . . . 1.0 μs
E. Typical Time Between Strobe Activation and Output Off to On Transition . . . . 1.0 μs
F. Minimum Data Pulse Width . . . . 500 ns

Information present at an input is transferred to its latch when the STROBE and ENABLE are high. The latches will continue to accept new data as long as both STROBE and ENABLE are held high. With either STROBE or ENABLE in the low state, no information can be loaded into the latches.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input low, the outputs are controlled by the state of the latches.

On first applying V_{DD} to the device, all latch outputs assume a low state (Power-Up Clear) resulting in all outputs being OFF. The latches will remain in the low condition until the Clear is disabled by a STROBE high input. Data may be entered into the latches during Power-Up Clear disable if the ENABLE input is also high.

SERIES UCN-4820A
# BiMOS 8-BIT SERIAL-INPUT, LATCHED DRIVERS

FEATURES

- High-Voltage Current-Sink Outputs
- CMOS, PMOS, NMOS, TTL Compatible
- Low-Power CMOS Logic and Latches
- Internal Pull-Up/Pull-Down Resistors
- 16-Pin Dual In-Line Plastic Packages

A COMBINATION of bipolar and MOS technology gives Sprague's Series UCN-4820A an interface flexibility beyond the reach of standard logic buffers and power driver arrays.

The three devices in this series each have eight bipolar current-sink Darlington drivers, a CMOS data latch for each of the eight open-collector outputs, an eight-bit CMOS shift register and CMOS control circuitry. Except for maximum driver voltage ratings, Types UCN-4821A, UCN-4822A and UCN-4823A are identical.

The bipolar outputs can drive multiplexed LED displays, incandescent lamps, thermal print heads, and (with appropriate clamping techniques) relays, solenoids and other high-power inductive loads.

The CMOS shift register and latches, which operate over a 5- to 15-volt supply range, minimize loading and are compatible with CMOS, PMOS and NMOS logic. Use of the drivers with TTL and DTL may require a pull-up resistor to ensure an input logic high. By using the serial data output, the drivers can be cascaded for interface applications requiring additional drive lines.

These devices are also available in industrial-grade ceramic packages (Series UCQ-4820R) and in military side-brazed, hermetically sealed packages (Series UCS-4820H).

Dwg. No. A-11,388
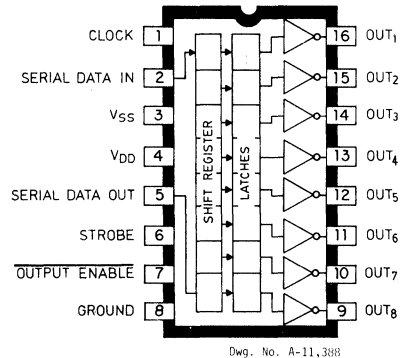
ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature
and $V_{SS} = 0$ V

Output Voltage, V_{OUT} (UCN-4821A) .... 50 V

(UCN-4822A) .... 80 V

(UCN-4823A) .... 100 V

Logic Supply Voltage, V_{DD} .... 18 V

Input Voltage Range, V_{IN} .... -0.3 V to V_{DD} $+0.3$ V

Continuous Output Current, I_{OUT} .... 500 mA

Package Power Dissipation, P_D .... 1.67 W*

Operating Temperature Range, T_A .... $-20°C$ to $+85°C$

Storage Temperature Range, T_S .... $-55°C$ to $+125°C$

*Derate at the rate of 16.7 mW/°C above $T_A = +25°C$

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5$ V, $V_{SS} = 0$ V (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Min.	Max.	Units
Output Leakage Current	I_{CEX}	UCN-4812A	$V_{OUT} = 50$ V	—	50	μA
			$V_{OUT} = 50$ V, $T_A = +70°C$	—	100	μA
		UCN-4822A	$V_{OUT} = 80$ V	—	50	μA
			$V_{OUT} = 80$ V, $T_A = +70°C$	—	100	μA
		UCN-4823A	$V_{OUT} = 100$ V	—	50	μA
			$V_{OUT} = 100$ V, $T_A = +70°C$	—	100	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_{OUT} = 100$ mA	—	1.1	V
			$I_{OUT} = 200$ mA	—	1.3	V
			$I_{OUT} = 350$ mA, $V_{DD} = 7.0$ V	—	1.6	V
Input Voltage	$V_{IN(0)}$	ALL		—	—	V
	$V_{IN(1)}$	ALL	$V_{DD} = 15$ V	13.5	—	V
			$V_{DD} = 10$ V	8.5	—	V
			$V_{DD} = 5.0$ V	3.5	—	V
Input Resistance	R_{IN}	ALL	$V_{DD} = 15$ V	50	—	kΩ
			$V_{DD} = 10V$ V	50	—	kΩ
			$V_{DD} = 5.0$ V	50	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	One Driver ON, $V_{DD} = 15$ V	—	2.0	mA
			One Driver ON, $V_{DD} = 10$ V	—	1.7	mA
			One Driver ON, $V_{DD} = 5.0$ V	—	1.0	mA
	$I_{DD(OFF)}$	ALL	$V_{DD} = 5.0$ V, All Drivers OFF, $V_{IN} = 0$ V	—	100	μA
			$V_{DD} = 15$ V, All Drivers OFF, $V_{IN} = 0$ V	—	200	μA

Number of Outputs ON ($I_{OUT} = 200$ mA)	Max. Allowable Duty Cycle at Ambient Temperature of				
	25°C	40°C	50°C	60°C	70°C
8	67%	56%	50%	43%	36%
7	76%	64%	57%	49%	41%
6	89%	74%	66%	57%	48%
5	100%	89%	80%	69%	58%
4	↑	100%	100%	75%	72%
3	↓	↑	↑	100%	95%
2	↓	↓	↓	↓	100%
1	100%	100%	100%	100%	100%

Caution: Sprague CMOS devices have input static protection but are still suscepti-
ble to damage when exposed to extremely high static electrical charges.
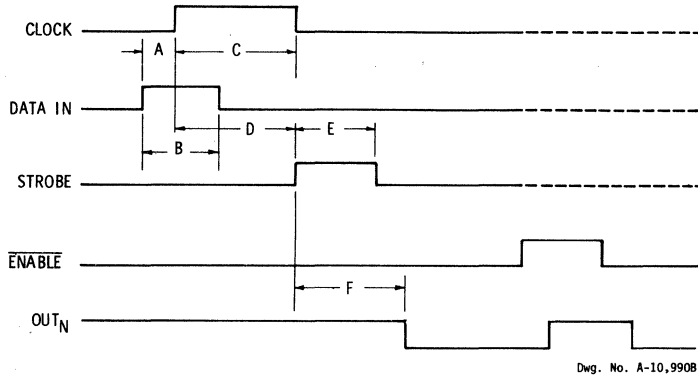
Dwg. No. A-10,990B

TIMING CONDITIONS
(Logic Levels are V_{DD} and V_{SS})

	$V_{DD} = 5.0$ V	$V_{DD} = 15$ V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	250 ns	150 ns
B. Minimum Data Pulse Width	500 ns	300 ns
C. Minimum Clock Pulse Width	1.0 μs	250 ns
D. Minimum Time Between Clock Activation and Strobe	1.0 μs	400 ns
E. Minimum Strobe Pulse Width	500 ns	300 ns
F. Typical Time Between Strobe Activation and Output Transition	1.0 μs	1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will con-

tinue to accept new data as long as the STROBE is held high. Applications where the latches are by-passed (STROBE tied high) will require that the ENABLE input be high during serial data entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

SERIES UCN-4820A TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents $I_1 I_2 I_3$ . . . . I_8	Serial Data Output	Strobe Input	Latch Contents $I_1 I_2 I_3$ . . . . I_8	Output Enable	Output Contents $I_1 I_2 I_3$ . . . . I_8
L	⌐	H R$_1$ R$_2$ . . . . R$_7$	R$_7$				
H	⌐	L R$_1$ R$_2$ . . . . R$_7$	R$_7$				
X	⌐	R$_1$ R$_2$ R$_3$ . . . . . . R$_8$	R$_8$				
		X X X X	X	L	R$_1$ R$_2$ R$_3$ . . . . . . R$_8$		
		P$_1$ P$_2$ P$_3$ . . . . P$_8$	P$_8$	H	P$_1$ P$_2$ P$_3$ . . . . P$_8$	L	P$_1$ P$_2$ P$_3$ . . . . P$_8$
					X X X X	H	H H H . . . . H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

FUNCTIONAL BLOCK DIAGRAM

Dwg. No. A-11,391B
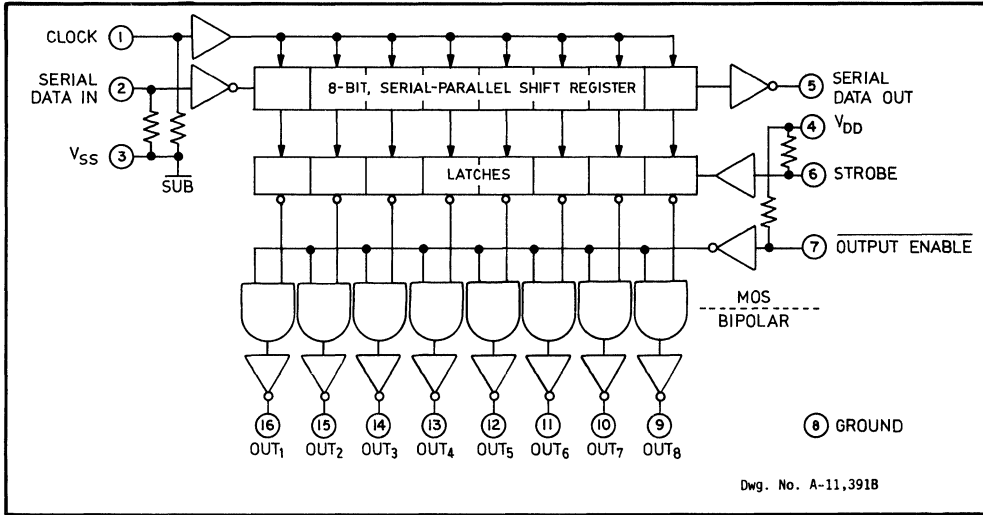
TYPICAL INPUT CIRCUITS

TYPICAL OUTPUT DRIVER

Dwg. No. A-11,389

Dwg. No. A-11,390
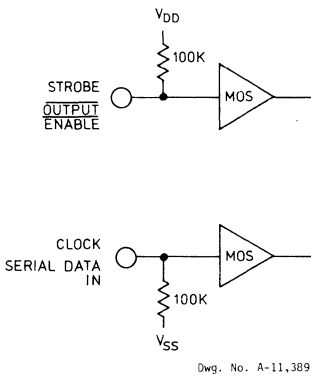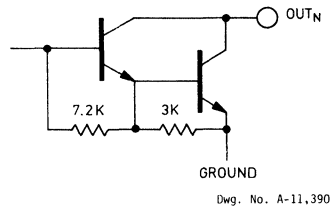
GROUP UCN-5800 BiMOS II
HIGH-SPEED INTERFACE DRIVERS

$\mathbf{S}$PRAGUE UCN-4400 and UCN-4800 BiMOS interface integrated circuits have evolved into new and improved designs. The CMOS sections of the original BiMOS devices have been reduced in size, resulting in faster switching speeds. Second-generation BiMOS devices also provide new and improved functions, as shown in the table below.

BiMOS II Type Number	Description*	Original BiMOS Type Number
UCN-5800A	Quad Latch, 350 mA/50 V Sink Driver	UCN-4401A
UCN-5801A	8-Bit Latch, 350 mA/50 V Sink Driver	UCN-4801A
UCN-5810A	10-Bit Serial/Parallel, − 25 mA/60 V Source Driver	UCN-4810A
UCN-5810A-1	10-Bit Serial/Parallel, − 25 mA/80 V Source Driver	UCN-4810A-1
UCN-5812A	20-Bit Serial/Parallel, − 25 mA/60 V Source Driver	None
UCN-5812A-1	20-Bit Serial/Parallel, − 25 mA/80 V Source Driver	None
UCN-5813B	Quad Latch, 1.5 A/50 V Sink Driver	None
UCN-5814B	Quad Latch, 1.5 A/50 V Sink Driver	None
UCN-5815A	8-Bit Latch, − 25 mA/60 V Source Driver	UCN-4815A
UCN-5815A-1	8-Bit Latch, − 25 mA/80 V Source Driver	UCN-4815A-1
UCN-5818A	32-Bit Serial/Parallel, − 25 mA/60 V Source Driver	None
UCN-5818A-1	32-Bit Serial Parallel, − 25 mA/80 V Source Driver	None
UCN-5821A	8-Bit Serial/Parallel, 350 mA/50 V Sink Driver	UCN-4812A
UCN-5822A	8-Bit Serial/Parallel, 350 mA/80 V Sink Driver	UCN-4822A
UCN-5823A	8-Bit Serial/Parallel, 350 mA/100 V Sink Driver	UCN-4823A
UCN-5825A	4-Bit Serial/Parallel, 1.5 A/50 V Driver	None
UCN-5826A	4-Bit Serial/Parallel, 1.5 A/60 V Driver	None
UCN-5832A	32-Bit Serial/Parallel, 100 mA/40 V Sink Driver	None
UCN-5890A	8-Bit Serial/Parallel, − 350 mA/50 V Source Driver	None
UCN-5895A	8-Bit Serial/Parallel, − 150 mA/50 V Source Driver	None

*Current ratings are maximum tested condition, voltage ratings are absolute maximum allowable.

These are new products. Detailed information, applications engineering assistance, samples, price, and delivery can be obtained directly from the factory in Worcester, Mass., Tel. (617) 853-5000.

SPRAGUE BiMOS —
MUSCLE FOR THE MICROPROCESSOR

Sprague Electric offers solutions to users' interface problems through a fusion of bipolar and CMOS technologies in BiMOS to create innovative interface devices.

The company's ability to shape technology to meet the specific needs of users is based on a commitment to provide versatile and practical interface products for systems design.

Sprague BiMOS devices are available with:
— Output breakdown voltage ratings of up to 100 V;
— Output current ratings as high as 600 mA;
— A logic voltage-supply range of 5 V to 15 V (±5%);
— Logic switching speeds of up to 1 MHz at 5 V and up to 2 MHz at 12 V;
— And up to 10 channels per dual in-line package.

Among advantages of BiMOS technology are microprocessor compatibility, low-power logic, a wide logic-supply range, component-count reduction, bipolar output capability, CMOS noise immunity, and space-saving integration.

APPLICATIONS

The following pages make up a sampler of applications for Sprague BiMOS interface devices. Performance specifications, truth tables and timing charts for these integrated circuits appear on previous pages. Additional applications are described in the Sprague brochure WR-185, "Interface ICs for Motor Drive Applications," and in Sprague engineering bulletins covering these BiMOS devices.

UCN-4401A and UCN-4801A

These four- and eight-bit BiMOS latch/drivers are the first Sprague IC's to incorporate CMOS logic (data latches) and bipolar drivers (NPN Darlington-pair outputs). Functionally, the eight-bit device is the equivalent of an octal latch and an octal NPN Darlington array.

Figure 1 depicts the use of the eight-bit latch/driver as an interface between a microprocessor and incandescent lamps. The device can also link a microprocessor with LEDs, high-power discrete semiconductors, relays or small stepper motors. Applications with inductive loads require connection of the internal transient-suppression diodes to the load's voltage supply, or use of discrete diodes. Inductive load applications should be limited to output voltages of +35 V.

Figure 2 shows use of Type UCN-4401A as an interface between a microprocessor and a stepper motor. Input signals to the four-bit device, for both unipolar wave drive and unipolar two-phase drive, are shown in Figures 3 and 4.

Type UCN-4401A can also be used to control discrete PNP transistors providing a high-power motor interface (Figure 5). Use of either single-ended or split supplies is possible with this approach.

The four-bit device can be paired with a quad PNP DIP to implement full-bridge drive for a stepper motor (Figure 6).

4

TYPE UCN-4801A

DWG.NO. A-11,444

Figure 1

UCN-4401A

DWG.NO. A-11,445

Figure 2

UNIPOLAR WAVE DRIVE

STROBE
IN 1
IN 2
IN 3
IN 4
OUT 1
OUT 2
OUT 3
OUT 4

DWG.NO. A-11,446

Figure 3

UNIPOLAR 2-PHASE DRIVE

STROBE
IN 1
IN 2
IN 3
IN 4
OUT 1
OUT 2
OUT 3
OUT 4

DWG.NO. A-11,447

Figure 4

4

C	1		14	OE
ST	2		13	V_{DD}
IN_1	3		12	
IN_2	4	LATCHES	11	
IN_3	5		10	
IN_4	6		9	
	7		8	+V

TYPE UCN-4401A

DWG.NO. A-11,448

Figure 5

4—35

Figure 6

DWG. NO. A-11,449
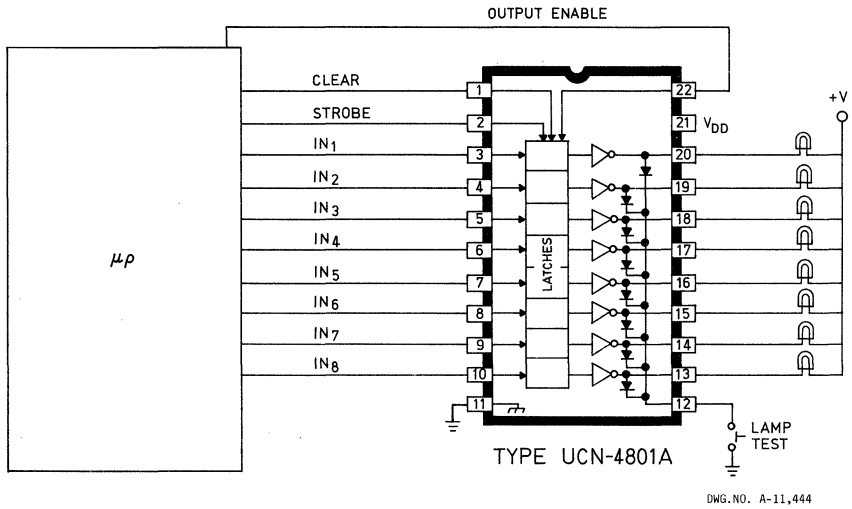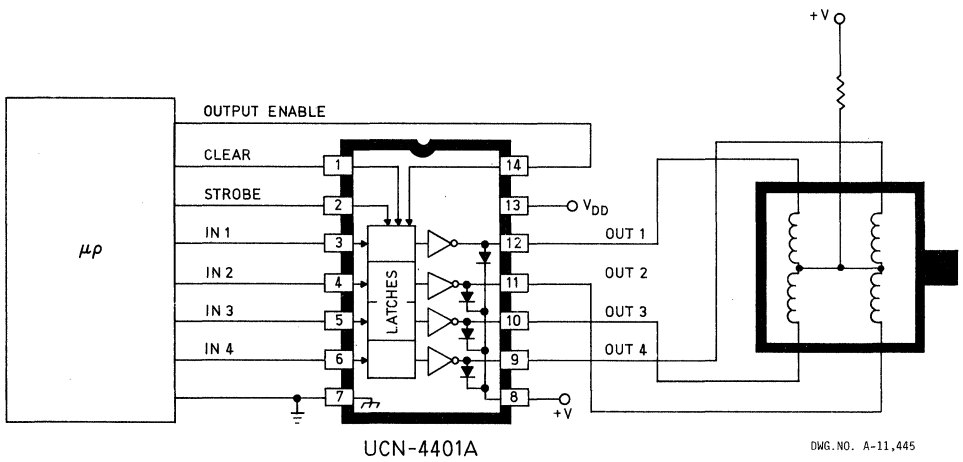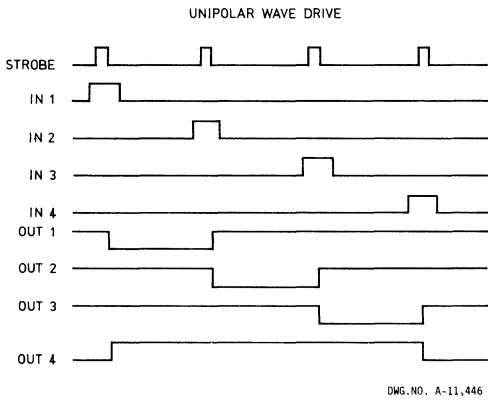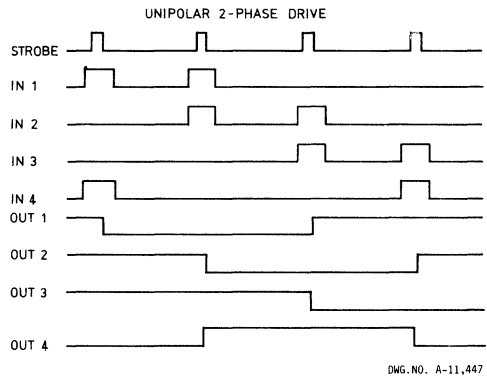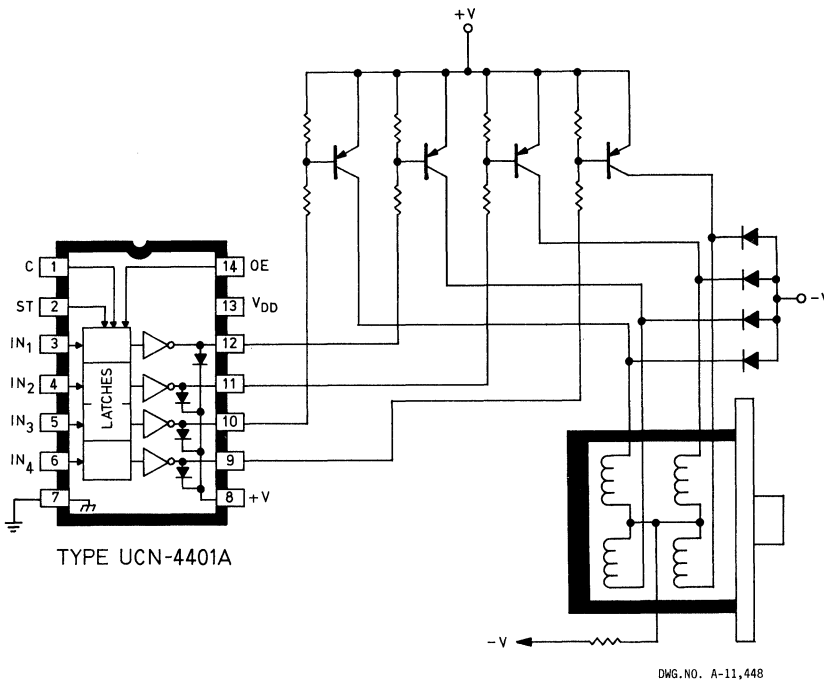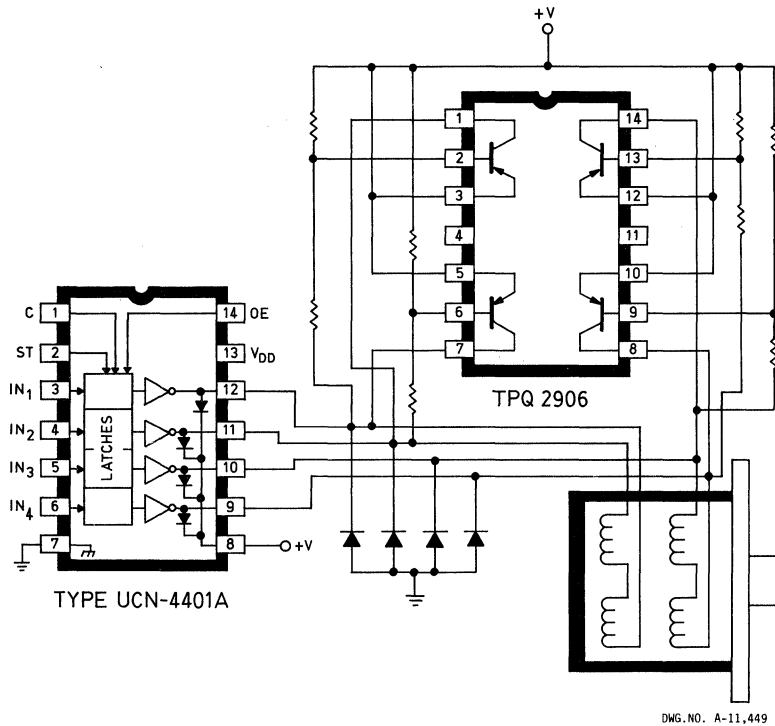
UCN-4810A

This integrated circuit functionally replaces a 10-bit serial-in, parallel-out shift register, a 10-bit data latch, and 10 high-voltage buffers (including output pull-down resistors). It is designed for use with vacuum fluorescent displays, but has been put to many other uses, including control of thermal print heads.

Connecting a data-out line from one device to a data-in pin of a second device minimizes the number of input/output lines required for a system. A 20-character 5 x 7 vacuum fluorescent dot matrix display, for instance, requires only six Type UCN-4810s (two as grid drivers and four as dot drivers). An example of cascaded data control is given in Figure 7. The arrangement cascades two devices for grid selection and four as dot drivers.

Data sent to the four dot drivers can be loaded in less than 80 μs using this configuration. The shift-rate limit of the dot drivers is 500 kHz at $V_{DD} = 5$ V.

The two units that function as grid drivers are loaded with a single "1" during each scan cycle. The minimum recommended scan frequency is 100 Hz per character (a clock frequency of 2 kHz for a 20-character display).

Since blanking (20 μs minimum) is required between characters, and since the minimum ON time for each digit or character is 100 μs, the maximum number of characters in a display is 80 (8 kHz clock, 125 μs ON and blanking time per character).

The typical ON time for vacuum fluorescent characters is 200 μs (40-character panel) to 500 μs (20-character display). Failure to provide proper blanking time can cause ghosting or flicker.

A faster method of loading matrix data, shown in Figure 8, requires more I/O lines. This technique loads shift registers during a blanking period (greater than 20 μs). Each dot driver has a separate data-input line, but uses common clock, strobe and blanking lines. A second clock is used with the grid drivers.

A typical data-input timing chart for this configuration is shown in Figure 9. With a 20-character vacuum fluorescent display having a 2 kHz scan frequency, 10 bits of data are loaded during the first blanking period; succeeding 10-bit data blocks are loaded during blanking periods at 400 μs intervals.

A more unusual application of Type UCN-4810A is shown in Figure 10: The device is used with a thermal printer. In production, the drivers (in chip form) were built into a hybrid assembly.

DWG.NO. A-11,450
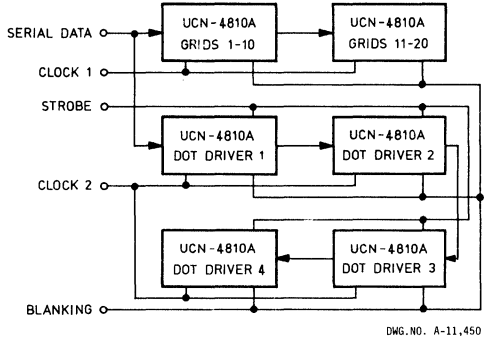
Figure 7
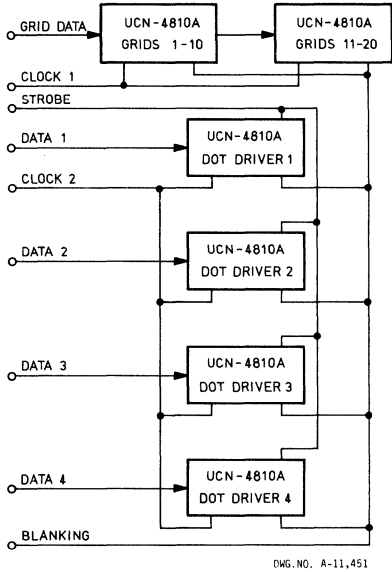
DWG.NO. A-11,451
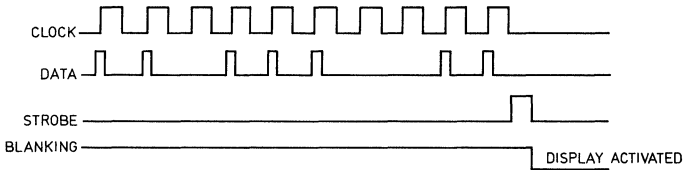
Figure 8

TIMING CONDITIONS UCN-4810A

DWG.NO. A-11,452

Figure 9

DWG. NO. A-11,453

Figure 10

DWG. NO. A-11,454

Figure 11

DWG.NO. A-11,455
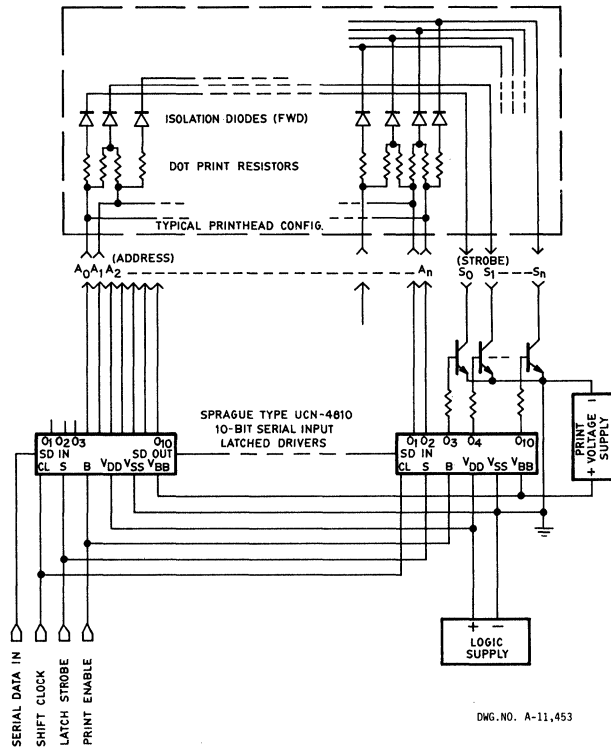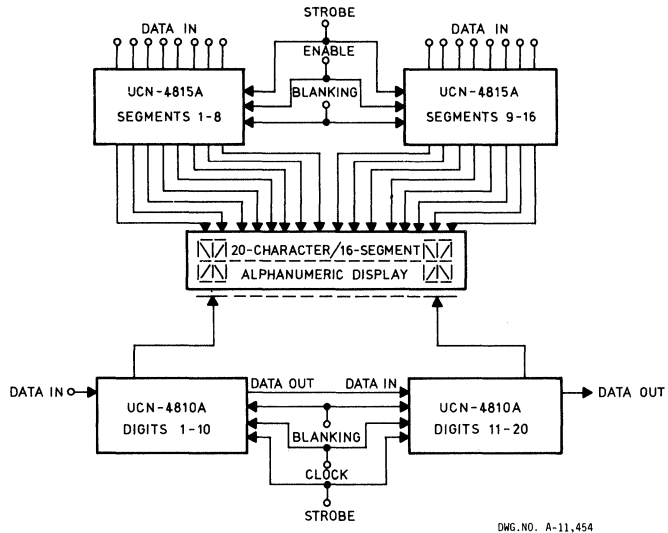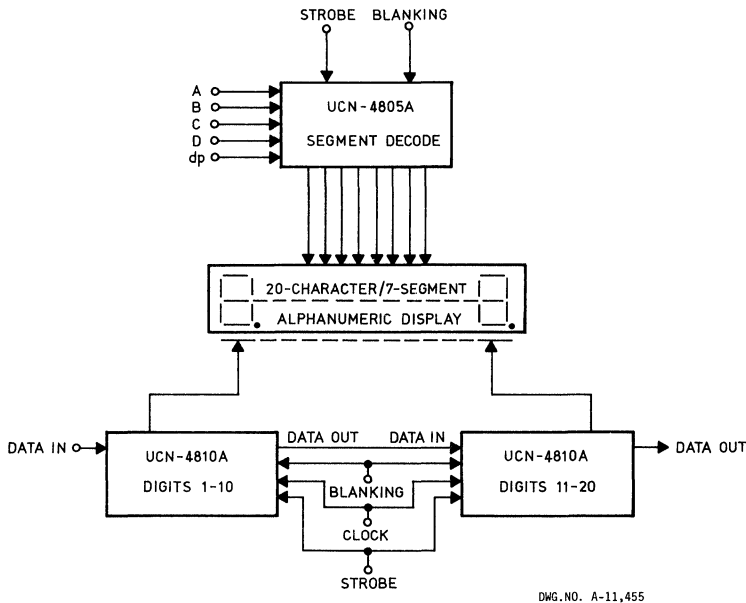
Figure 12

UCN-4815

Type UCN-4815A provides an eight-bit parallel-in, parallel-out interface for vacuum fluorescent displays. A typical application appears in Figure 11. A pair of Type ICN-4810As are used for grid control. The two Type UCN-4815As drive a 16-segment alphanumeric display.

UCN-4805A

Type UCN-4805A has eight high-voltage source outputs, latched inputs, and both the hexadecimal decoding and speed capabilities for microprocessor-based designs. The device is used to decode and drive seven-segment displays. Its eighth source output is used to generate a colon or decimal point.

A typical application with a 20-character vacuum fluorescent display is shown in Figure 12. Type UCN-4805A is used as a seven-segment decoder/driver. A pair of Type UCN-4810As is used for grid-select.

SERIES UCN-4820A

The drivers in this series were designed for use in printers. Each integrated circuit has an eight-bit serial-input shift register, an eight-bit data latch, and eight NPN Darlington-pair outputs. The data entry rate for this series is 500 kHz (minimum) at $V_{DD} = 5\,V$.

A typical application appears in Figure 13; although the drawing depicts use with an electrosensitive printer, the device can also control inductive loads such as print hammers and solenoids, or thermal print heads.

Use of Types ICN-4823A and UCN-4810A-1 is combined in the planar gas-discharge display application shown in Figure 14. Type UCN-4810A-1 signal inputs are level-shifted (floated to the V_{BB} supply level). The application requires external segment limiting and pull-up resistors and use of Zener diodes.

UCN-4820A

DWG.NO. A-11,456

Figure 13

DWG.NO. A-11,457

Figure 14

SECTION 5—MILITARY AND AEROSPACE DEVICES

NOTE: Most devices described in Sections 2, 3, and 4 can also be supplied in extended-temperature hermetic packages. Contact the local sales office or factory for additional information.

SERIES 400, 400-1, AND 500
HERMETICALLY SEALED POWER AND RELAY DRIVERS

FEATURES

- 500mA Output Sink Current Capability
- DTL/TTL Compatible Inputs
- Transient Protected Outputs on Relay Drivers
- High Voltage Output — 100V Series 500, 70V Series 400-1, and 40V Series 400
- Hermetically Sealed Packages to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B

Description

These Series 400, 400-1, and 500 hermetically sealed power and relay drivers are bipolar monolithic circuits incorporating both logic gates and high-current switching transistors on the same chip. Each device contains four drivers capable of sinking 500mA in the ON state. In the OFF state, Series 400 devices will sustain 40V, Series 400-1 devices will sustain 70V, and Series 500 devices will sustain 100V.

All devices are available in either a 14-pin hermetic flat-pack package (Types UHC-) or a 14-pin hermetic dual in-line package (Types UHD-). These packages conform to the dimensional requirements of Military Specification MIL-M-38510 and meet all of the processing and environmental requirements of Military Standard MIL-STD-883, Method 5004 and 5005. These devices are also furnished in a plastic 14-pin dual in-line package (Types UHP-) for operation over a limited temperature range.

Applications

The UHC- and UHD- Series 400, 400-1, and 500 power and relay drivers are ideally suited for driving incandescent lamps, relays, solenoids, and other interface devices with up to 1A output current per package. Hermetic sealing and an operating temperature range of −55°C to +125°C recommend them for military and aerospace applications as well as commercial and industrial control applications where severe environments may be encountered.

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into any output (ON state)			250	mA

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} 7V
Input Voltage, V_{in}: 5.5V
Output Off-state Voltage, V_{off}:
  Series UHC-400 and UHD-400 . . . . 40V
  Series UHC-400-1 and UHD-400-1 . . . . 70V
  Series UHC-500 and UHD-500 . . . . 100V
Output On-State Sink Current, I_{on} 500mA
Suppression Diode Off-State Voltage, V_{off}.
  Series UHC-400 and UHD-400 . . . . 40V
  Series UHC-400-1 and UHD-400-1 . . . . 70V
  Series UHC-500 and UHD-500 . . . . 100V
Suppression Diode On-State Current, I_{on} 500mA
Operating Free-Air Temperature Range, T_A . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

5

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	Vcc	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current at all Inputs except Strobe	$I_{in(0)}$		MAX	0.4V	4.5V			−0.55	−0.8	mA	1, 2
"0" Input Current at Strobe	$I_{in(0)}$		MAX	0.4V	4.5V			−1.1	−1.6	mA	2
"1" Input Current at all Inputs except Strobe	$I_{in(1)}$		MAX	2.4V	0V				40	μA	1
			MAX	5.5V	0V				1	mA	1
"1" Input Current at Strobe	$I_{in(1)}$		MAX	2.4V	0V				100	μA	
			MAX	5.5V	0V				1	mA	
"1" Output Reverse Current Series 400	I_{off}		MIN			40V			100	μA	6
Series 400-1			MIN			70V			100	μA	6
Series 500			MIN			100V			100	μA	6
"0" Output Voltage	V_{on}	NOM	MIN			150mA			0.5	V	6
		NOM	MIN			250mA			0.7	V	6
		MAX	MIN			150mA			0.6	V	6
		MAX	MIN			250mA			0.8	V	6
Diode Leakage Current	I_{LK}	NOM	NOM			OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM					1.5	1.75	V	2, 4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX						7.5	mA	5, 6
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX						26.5	mA	5, 6

NOTES:
1. Each input.
2. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
3. Measured at $V_R = V_{off(min)}$.
4. Measured at I_f = 200mA.
5. Each gate.
6. Input test conditions are listed in Table IV.

Table IV
INPUT CONDITIONS FOR OUTPUT CHARACTERISTIC MEASUREMENTS

Type UHC- or UHD-	"1" Output Reverse Current (I_{off})		"0" Output Voltage (V_{on})		"1" Level Supply Current ($I_{CC(1)}$)		"0" Level Supply Current ($I_{CC(0)}$)	
	Driven Input	Other Input	Driven Input	Other Input	Driven Input	Other Input	Driven Input	Other Input
400, 400-1, 500	2.0V	2.0V	0.8V	V_{CC}	5.0V	5.0V	0V	0V
402, 402-1, 502	2.0V	2.0V	0.8V	0.8V	5.0V	5.0V	0V	0V
403, 403-1, 503	2.0V	0V	0.8V	0.8V	5.0V	5.0V	0V	0V
406, 406-1, 506	2.0V	2.0V	0.8V	V_{CC}	5.0V	5.0V	0V	0V
407, 407-1, 507	0.8V	V_{CC}	2.0V	2.0V	0V	0V	5.0V	5.0V
408, 408-1, 508	0.8V	V_{CC}	2.0V	2.0V	0V	0V	5.0V	5.0V
432, 432-1, 532	0.8V	0.8V	2.0V	0V	0V	0V	5.0V	5.0V
433, 433-1, 533	0.8V	0.8V	2.0V	0V	0V	0V	5.0V	5.0V

SWITCHING CHARACTERISTICS at $V_{CC} = 5.0V$, $T_A = 25°C$

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Turn-on Delay Time	t_{pd0}					
Series 400		$V_S = 40V$, $R_L = 265 \ \Omega$ (6 Watts)			750	ns
Series 400-1		$V_S = 70V$, $R_L = 465 \ \Omega$ (10 Watts)			750	ns
Series 500		$V_S = 100V$, $R_L = 670 \ \Omega$ (15 Watts)			750	ns
Turn-off Delay Time	t_{pd1}					
Series 400		$V_S = 40V$, $R_L = 265 \ \Omega$ (6 Watts)			500	ns
Series 400-1		$V_S = 70V$, $R_L = 465 \ \Omega$ (10 Watts)			500	ns
Series 500		$V_S = 100V$, $R_L = 670 \ \Omega$ (15 Watts)			500	ns

Typical Switching Test Circuit

DWG. NO. A-7809A

DWG. NO. A-7900A
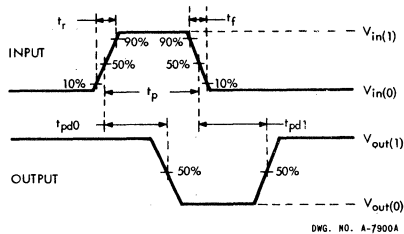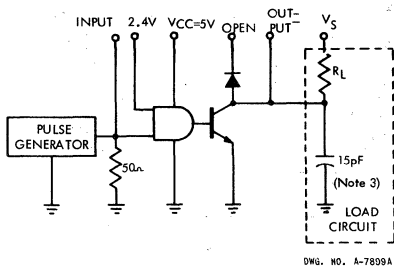
INPUT PULSE CHARACTERISTICS

$V_{in(0)} = 0V$	$t_f = 7.$ ns	$t_p = 1 \mu s$
$V_{in(1)} = 3.5V$	$t_r = 14$ ns	PRR = 500kHz

Device Pinning
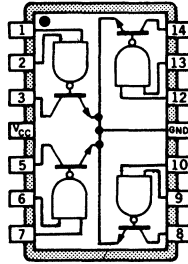
UHC-400
UHC-400-1
UHC-500
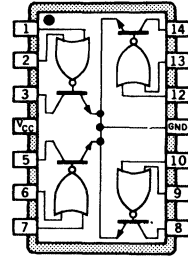
UHC-402
UHC-402-1
UHC-502
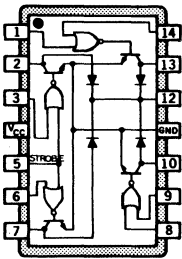
UHC-403
UHC-403-1
UHC-503
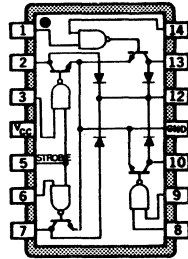
UHC-406
UHC-406-1
UHC-506
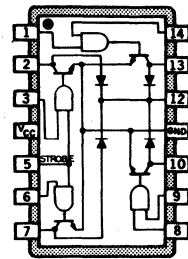
UHC-407
UHC-407-1
UHC-507
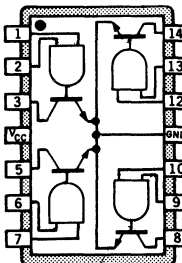
UHC-408
UHC-408-1
UHC-508
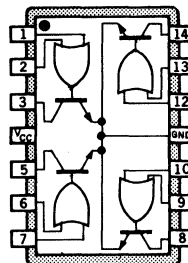
UHC-432
UHC-432-1
UHC-532
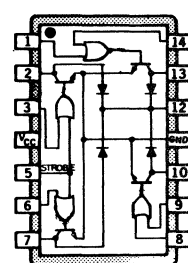
UHC-433
UHC-433-1
UHC-533

5

**Device Pinning
(Continued)**
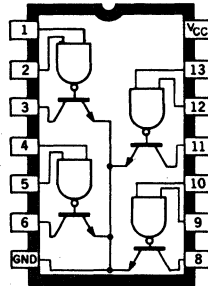
UHD-400
UHD-400-1
UHD-500
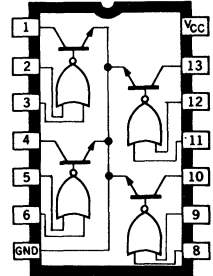
UHD-402
UHD-402-1
UHD-502
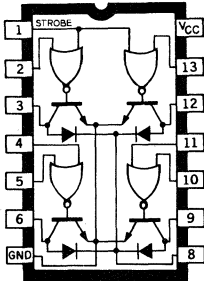
UHD-403
UHD-403-1
UHD-503
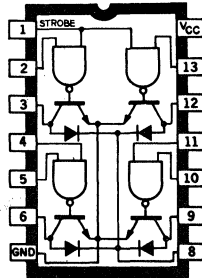
UHD-406
UHD-406-1
UHD-506
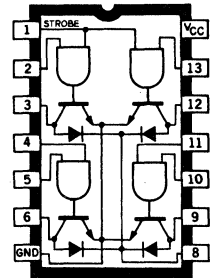
UHD-407
UHD-407-1
UHD-507
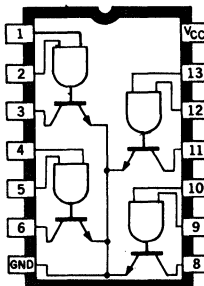
UHD-408
UHD-408-1
UHD-508
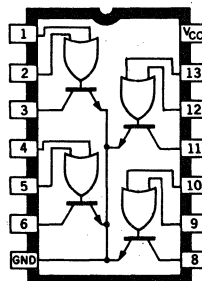
UHD-432
UHD-432-1
UHD-532
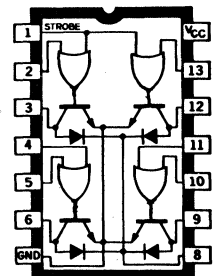
UHD-433
UHD-433-1
UHD-533

SERIES ULS-2000H AND ULS-2000R
HIGH-VOLTAGE, HIGH-CURRENT
DARLINGTON TRANSISTOR ARRAYS

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Peak Output Current to 600 mA
- Transient Protected Outputs
- Side-Brazed Hermetic Package, or
- Cer-DIP Package
- High-Reliability Screening Available
- Wide Operating Temperature Ranges

DWG. NO. A-9594

COMPRISED of seven silicon NPN Darlington power drivers on a common monolithic substrate, the Series ULS-2000H and ULS-2000R arrays are ideally suited for driving relays, solenoids, lamps, and other devices with up to 3.0 A output current per package. Both hermetically sealed package styles are rated for operation over the temperature range of −55°C to +125°C, recommending them for military and aerospace applications or in commercial and industrial applications where severe environments may be encountered.

The 25 integrated circuits permit the circuit designer to select the optimum device for any application. There are two packages, five input characteristics, two output voltages, and two output currents covered by the listings. The appropriate part for use in specific applications can be determined from the Device Type Number Designation chart. Note that the high-voltage devices (BV$_{CE}$ ≥ 95 V) are available in the Series ULS-2000H only. All units feature open collector outputs and integral diodes for inductive load transient suppression.
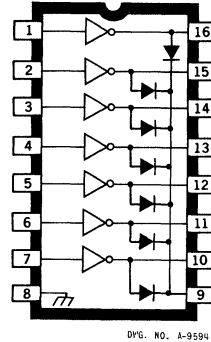
All series ULS-2000H arrays are furnished in a 16-pin side-brazed dual in-line hermetic package that conforms to the dimensional requirements of Military Specification MIL-M-38510 and meets the processing and environmental requirements of Military Standard MIL-STD.-883, Methods 5004 and 5005.

Device Type Number Designation

$V_{CE(MAX)}$ = $I_{C(MAX)}$ =	50 V 500 mA	50 V 600 mA	95 V 500 mA
		Type Number	
General-Purpose PMOS, CMOS	ULS-2001R ULS-2001H	ULS-2011R ULS-2001H	ULS-2021H
14-25 V PMOS	ULS-2002R ULS-2002H	ULS-2012R ULS-2012H	ULS-2022H
5 V TTL, CMOS	ULS-2003R ULS-2003H	ULS-2013R ULS-2013H	ULS-2023H
6-15 V CMOS, PMOS	ULS-2004R ULS-2004H	ULS-2014R ULS-2014H	ULS-2024H
High-Output TTL	ULS-2005R ULS-2005H	ULS-2015R ULS-2015H	ULS-2025H

5

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE} (Series 2000*, 2010*) . . . . 50 V
(Series ULS-2020H) . . . . 95 V
Input Voltage, V_{IN} (Series 2002*, 2003*, 2004*) . . . . 30 V
(Series 2005*) . . . . 15 V
Peak Output Current, I_{OUT} (Series 2000*, ULS-2020H) . . . . 500 mA
(Series 2010*) . . . . 600 mA
Ground Terminal Current, I_{GND}. . . . . 3.0 A
Continuous Input Current, I_{IN} . . . . 25 mA
Power Dissipation, P_D (one Darlington pair) . . . . 1.0 W
(total package) . . . . See Graphs
Operating Temperature Range, T_A. . . . . $-55°C$ to $+125°C$
Storage Temperature Range, T_S . . . . $-65°C$ to $+150°C$

PARTIAL SCHEMATICS

Series 2001*
(each driver)
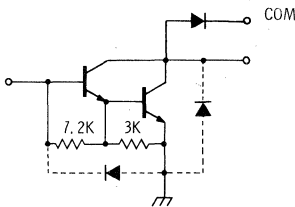
DWG. NO. A-9505

Series 2002*
(each driver)
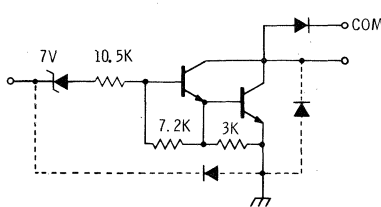
DWG. No. A-9650

Series 2003*
(each driver)
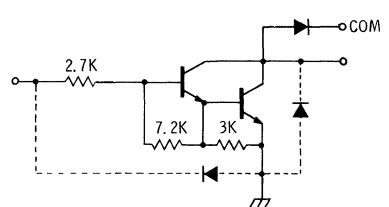
DWG. No. A-9651

Series 2004*
(each driver)
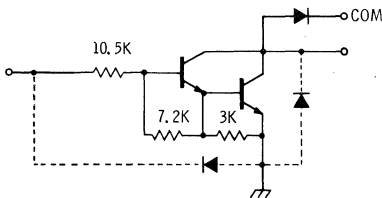
DWG. NO. A-9898A

Series 2005*
(each driver)
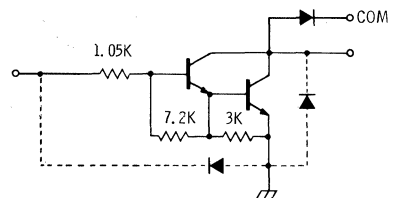
DWG. NO. A-10.228

*Complete part number includes a prefix to indicate temperature range and a suffix to indicate package style. See
following part number description.

SERIES ULS-2000H AND ULS-2000R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Temp.	Test Conditions		Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		$V_{CE} = 50\,V$		1A	—	—	100	μA
		2002*		$V_{CE} = 50\,V$, $V_{IN} = 6\,V$		1B	—	—	500	μA
		2004*		$V_{CE} = 50\,V$, $V_{IN} = 1\,V$		1B	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	Min.	$I_C = 350\,mA$, $I_B = 850\,\mu A$		2	—	1.6	1.8	V
				$I_C = 200\,mA$, $I_B = 550\,\mu A$		2	—	1.3	1.5	V
				$I_C = 100\,mA$, $I_B = 350\,\mu A$		2	—	1.1	1.3	V
				$I_C = 350\,mA$, $I_B = 500\,\mu A$		2	—	1.25	1.6	V
			+25°C	$I_C = 200\,mA$, $I_B = 350\,\mu A$		2	—	1.1	1.3	V
				$I_C = 100\,mA$, $I_B = 250\,\mu A$		2	—	0.9	1.1	V
			Max.	$I_C = 350\,mA$, $I_B = 500\,\mu A$		2	—	1.6	1.8	V
				$I_C = 200\,mA$, $I_B = 350\,\mu A$		2	—	1.3	1.5	V
				$I_C = 100\,mA$, $I_B = 250\,\mu A$		2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	2002*		$V_{IN} = 17\,V$		3	480	850	1300	μA
		2003*		$V_{IN} = 3.85\,V$		3	650	930	1350	μA
		2004*		$V_{IN} = 5\,V$		3	240	350	500	μA
				$V_{IN} = 12\,V$		3	650	1000	1450	μA
		2005*		$V_{IN} = 3\,V$		3	1180	1500	2400	μA
	$I_{IN(OFF)}$	All	Max.	$I_C = 500\,\mu A$		4	25	50	—	μA
Input Voltage	$V_{IN(ON)}$	2002*	Min.	$V_{CE} = 2\,V$, $I_C = 300\,mA$		5	—	—	18	V
			Max.	$V_{CE} = 2\,V$, $I_C = 300\,mA$		5	—	—	13	V
		2003*	Min.	$V_{CE} = 2\,V$, $I_C = 200\,mA$		5	—	—	3.3	V
				$V_{CE} = 2\,V$, $I_C = 250\,mA$		5	—	—	3.6	V
				$V_{CE} = 2\,V$, $I_C = 300\,mA$		5	—	—	3.9	V
			Max.	$V_{CE} = 2\,V$, $I_C = 200\,mA$		5	—	—	2.4	V
				$V_{CE} = 2\,V$, $I_C = 250\,mA$		5	—	—	2.7	V
				$V_{CE} = 2\,V$, $I_C = 300\,mA$		5	—	—	3.0	V
		2004*	Min.	$V_{CE} = 2\,V$, $I_C = 125\,mA$		5	—	—	6.0	V
				$V_{CE} = 2\,V$, $I_C = 200\,mA$		5	—	—	8.0	V
				$V_{CE} = 2\,V$, $I_C = 275\,mA$		5	—	—	10	V
				$V_{CE} = 2\,V$, $I_C = 350\,mA$		5	—	—	12	V
			Max.	$V_{CE} = 2\,V$, $I_C = 125\,mA$		5	—	—	5.0	V
				$V_{CE} = 2\,V$, $I_C = 200\,mA$		5	—	—	6.0	V
				$V_{CE} = 2\,V$, $I_C = 275\,mA$		5	—	—	7.0	V
				$V_{CE} = 2\,V$, $I_C = 350\,mA$		5	—	—	8.0	V
		2005*	Min.	$V_{CE} = 2\,V$, $I_C = 350\,mA$		5	—	—	3.0	V
			Max.	$V_{CE} = 2\,V$, $I_C = 350\,mA$		5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2001*	Min.	$V_{CE} = 2\,V$, $I_C = 350\,mA$		2	500	—	—	—
			+25°C	$V_{CE} = 2\,V$, $I_C = 350\,mA$		2	1000	—	—	—
Input Capacitance	C_{IN}	All	+25°C			—	—	15	25	pF
Turn-On Delay	t_{PLH}	All	+25°C	0.5 E_{in} to 0.5 E_{out}		—	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C	0.5 E_{in} to 0.5 E_{out}		—	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		$V_R = 50\,V$		6	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All		$I_F = 350\,mA$		7	—	1.7	2.0	V

*Complete part number includes a prefix to indicate temperature range and a suffix to indicate package style. See following part number description.

Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

5

SERIES ULS-2010H AND ULS-2010R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Temp.	Test Conditions	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		$V_{CE} = 50$ V	1A	—	—	100	μA
		2012*		$V_{CE} = 50$ V, $V_{IN} = 6$ V	1B	—	—	500	μA
		2014*		$V_{CE} = 50$ V, $V_{IN} = 1$ V	1B	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	Min.	$I_C = 500$ mA, $I_B = 1100\,\mu$A	2	—	1.8	2.1	V
				$I_C = 350$ mA, $I_B = 850\,\mu$A	2	—	1.6	1.8	V
				$I_C = 200$ mA, $I_B = 550\,\mu$A	2	—	1.3	1.5	V
			+25°C	$I_C = 500$ mA, $I_B = 600\,\mu$A	2	—	1.7	1.9	V
				$I_C = 350$ mA, $I_B = 500\,\mu$A	2	—	1.25	1.6	V
				$I_C = 200$ mA, $I_B = 350\,\mu$A	2	—	1.1	1.3	V
			Max.	$I_C = 500$ mA, $I_B = 600\,\mu$A	2	—	1.8	2.1	V
				$I_C = 350$ mA, $I_B = 500\,\mu$A	2	—	1.6	1.8	V
				$I_C = 200$ mA, $I_B = 350\,\mu$A	2	—	1.3	1.5	V
Input Current	$I_{IN(ON)}$	2012*		$V_{IN} = 17$ V	3	480	850	1300	μA
		2013*		$V_{IN} = 3.85$ V	3	650	930	1350	μA
		2014*		$V_{IN} = 5$ V	3	240	350	500	μA
				$V_{IN} = 12$ V	3	650	1000	1450	μA
		2015*		$V_{IN} = 3$ V	3	1180	1500	2400	μA
	$I_{IN(OFF)}$	All	Max.	$I_C = 500\,\mu$A	4	25	50	—	μA
Input Voltage	$V_{IN(ON)}$	2012*	Min.	$V_{CE} = 2$ V, $I_C = 500$ mA	5	—	—	23.5	V
			Max.	$V_{CE} = 2$ V, $I_C = 500$ mA	5	—	—	17	V
		2013*	Min.	$V_{CE} = 2$ V, $I_C = 250$ mA	5	—	—	3.6	V
				$V_{CE} = 2$ V, $I_C = 300$ mA	5	—	—	3.9	V
				$V_{CE} = 2$ V, $I_C = 500$ mA	5	—	—	6.0	V
			Max.	$V_{CE} = 2$ V, $I_C = 250$ mA	5	—	—	2.7	V
				$V_{CE} = 2$ V, $I_C = 300$ mA	5	—	—	3.0	V
				$V_{CE} = 2$ V, $I_C = 500$ mA	5	—	—	3.5	V
		2014*	Min.	$V_{CE} = 2$ V, $I_C = 275$ mA	5	—	—	10	V
				$V_{CE} = 2$ V, $I_C = 350$ mA	5	—	—	12	V
				$V_{CE} = 2$ V, $I_C = 500$ mA	5	—	—	17	V
			Max.	$V_{CE} = 2$ V, $I_C = 275$ mA	5	—	—	7.0	V
				$V_{CE} = 2$ V, $I_C = 350$ mA	5	—	—	8.0	V
				$V_{CE} = 2$ V, $I_C = 500$ mA	5	—	—	9.5	V
		2015*	Min.	$V_{CE} = 2$ V, $I_C = 350$ mA	5	—	—	3.0	V
				$V_{CE} = 2$ V, $I_C = 500$ mA	5	—	—	3.5	V
			Max.	$V_{CE} = 2$ V, $I_C = 350$ mA	5	—	—	2.4	V
				$V_{CE} = 2$ V, $I_C = 500$ mA	5	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	2011*	Min.	$V_{CE} = 2$ V, $I_C = 500$ mA	2	450	—	—	—
			+25°C	$V_{CE} = 2$ V, $I_C = 500$ mA	2	900	—	—	—
Input Capacitance	C_{IN}	All	+25°C		—	—	15	25	pF
Turn-On Delay	t_{PLH}	All	+25°C	0.5 E_{in} to 0.5 E_{out}	—	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C	0.5 E_{in} to 0.5 E_{out}	—	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		$V_R = 50$ V	6	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All		$I_F = 350$ mA	7	—	1.7	2.0	V
				$I_F = 500$ mA	7	—	—	2.5	V

*Complete part number includes a prefix to indicate temperature range and a suffix to indicate package style. See following part number description.

Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

SERIES ULS-2020H

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Temp.	Test Conditions	Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		$V_{CE} = 95\ V$	1A	—	—	100	μA
		ULS-2022H		$V_{CE} = 95\ V$, $V_{IN} = 6\ V$	1B	—	—	500	μA
		ULS-2024H		$V_{CE} = 95\ V$, $V_{IN} = 1\ V$	1B	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	Min.	$I_C = 350\ mA$, $I_B = 850\ \mu A$	2	—	1.6	1.8	V
				$I_C = 200\ mA$, $I_B = 550\ \mu A$	2	—	1.3	1.5	V
				$I_C = 100\ mA$, $I_B = 350\ \mu A$	2	—	1.1	1.3	V
			+25°C	$I_C = 350\ mA$, $I_B = 500\ \mu A$	2	—	1.25	1.6	V
				$I_C = 200\ mA$, $I_B = 350\ \mu A$	2	—	1.1	1.3	V
				$I_C = 100\ mA$, $I_B = 250\ \mu A$	2	—	0.9	1.1	V
			Max.	$I_C = 350\ mA$, $I_B = 500\ \mu A$	2	—	1.6	1.8	V
				$I_C = 200\ mA$, $I_B = 350\ \mu A$	2	—	1.3	1.5	V
				$I_C = 100\ mA$, $I_B = 250\ \mu A$	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	ULS-2022H		$V_{IN} = 17\ V$	3	480	850	1300	μA
		ULS-2023H		$V_{IN} = 3.85\ V$	3	650	930	1350	μA
		ULS-2024H		$V_{IN} = 5\ V$	3	240	350	500	μA
				$V_{IN} = 12\ V$	3	650	1000	1450	μA
		ULS-2025H		$V_{IN} = 3\ V$	3	1180	1500	2400	μA
	$I_{IN(OFF)}$	All	Max.	$I_C = 500\ \mu A$	4	25	50	—	μA
Input Voltage	$V_{IN(ON)}$	ULS-2022H	Min.	$V_{CE} = 2\ V$, $I_C = 300\ mA$	5	—	—	18	V
			Max.	$V_{CE} = 2\ V$, $I_C = 300\ mA$	5	—	—	13	V
		ULS-2023H	Min.	$V_{CE} = 2\ V$, $I_C = 200\ mA$	5	—	—	3.3	V
				$V_{CE} = 2\ V$, $I_C = 250\ mA$	5	—	—	3.6	V
				$V_{CE} = 2\ V$, $I_C = 300\ mA$	5	—	—	3.9	V
			Max.	$V_{CE} = 2\ V$, $I_C = 200\ mA$	5	—	—	2.4	V
				$V_{CE} = 2\ V$, $I_C = 250\ mA$	5	—	—	2.7	V
				$V_{CE} = 2\ V$, $I_C = 300\ mA$	5	—	—	3.0	V
		ULS-2024H	Min.	$V_{CE} = 2\ V$, $I_C = 125\ mA$	5	—	—	6.0	V
				$V_{CE} = 2\ V$, $I_C = 200\ mA$	5	—	—	8.0	V
				$V_{CE} = 2\ V$, $I_C = 275\ mA$	5	—	—	10	V
				$V_{CE} = 2\ V$, $I_C = 350\ mA$	5	—	—	12	V
			Max.	$V_{CE} = 2\ V$, $I_C = 125\ mA$	5	—	—	5.0	V
				$V_{CE} = 2\ V$, $I_C = 200\ mA$	5	—	—	6.0	V
				$V_{CE} = 2\ V$, $I_C = 275\ mA$	5	—	—	7.0	V
				$V_{CE} = 2\ V$, $I_C = 350\ mA$	5	—	—	8.0	V
		ULS-2025H	Min.	$V_{CE} = 2\ V$, $I_C = 350\ mA$	5	—	—	3.0	V
			Max.	$V_{CE} = 2\ V$, $I_C = 350\ mA$	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	ULS-2021H	Min.	$V_{CE} = 2\ V$, $I_C = 350\ mA$	2	500	—	—	—
			+25°C	$V_{CE} = 2\ V$, $I_C = 350\ mA$	2	1000	—	—	—
Input Capacitance	C_{IN}	All	+25°C		—	—	15	25	pF
Turn-On Delay	t_{PLH}	All	+25°C	$0.5\ E_{in}$ to $0.5\ E_{out}$	—	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C	$0.5\ E_{in}$ to $0.5\ E_{out}$	—	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		$V_R = 95\ V$	6	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All		$I_F = 350\ mA$	7	—	1.7	2.0	V

Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

TEST FIGURES

FIGURE 1A

FIGURE 1B

FIGURE 2

FIGURE 3

FIGURE 4

FIGURE 5

FIGURE 6

FIGURE 7

SERIES ULS-2000H

PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE
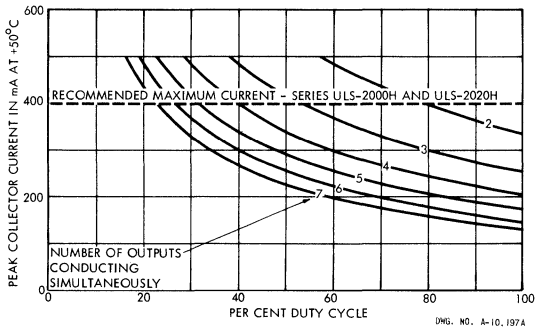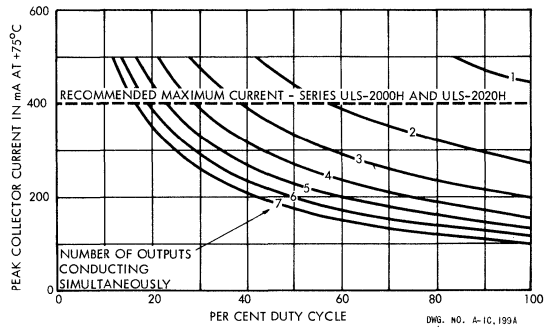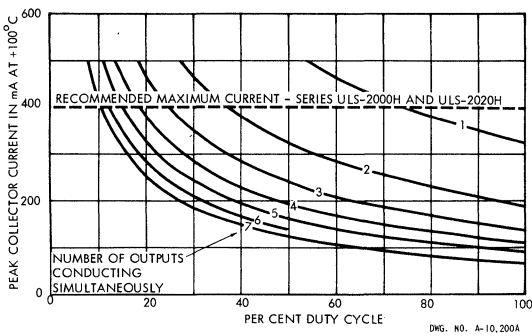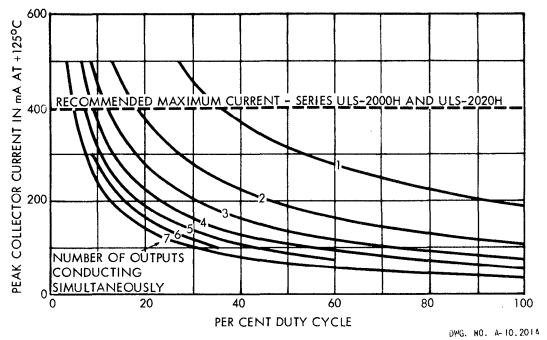
AT +50°C

DWG. NO. A-10,197A

AT +75°C

DWG. NO. A-10,199A

5

AT +100°C

DWG. NO. A-10,200A

AT +125°C

DWG. NO. A-10,201A

SERIES ULS-2000R

PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE

AT +50°C

AT +75°C

Dwg. No. A-10,883A
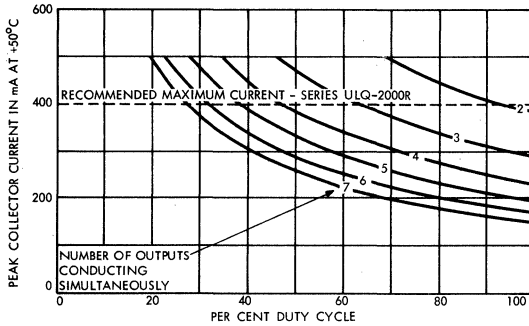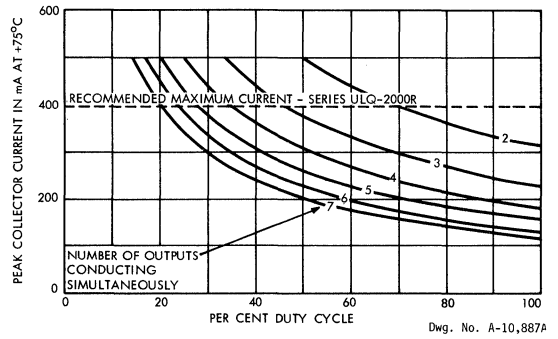
Dwg. No. A-10,887A

ALLOWABLE PACKAGE POWER DISSIPATION
SERIES ULS-2000H AND ULS-2000R
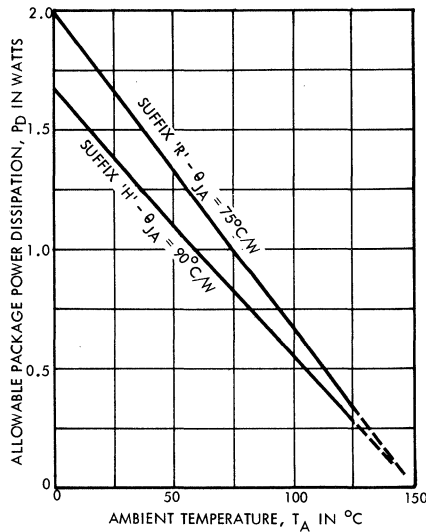
Dwg. No. A-10,884A

**COLLECTOR CURRENT
AS A FUNCTION OF INPUT CURRENT**
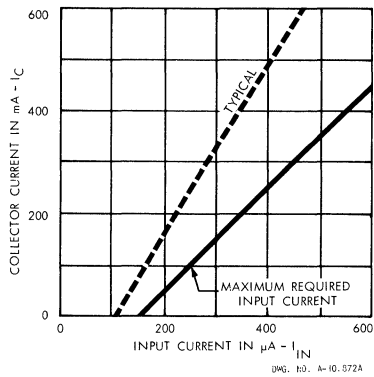
**COLLECTOR CURRENT
AS A FUNCTION OF SATURATION VOLTAGE**
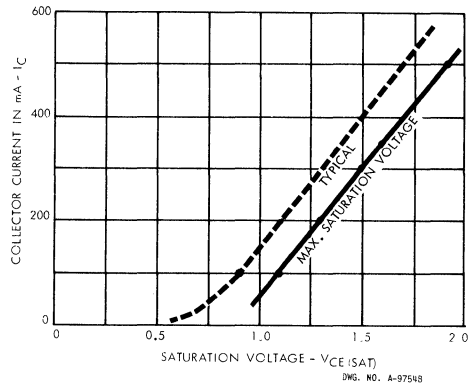
SERIES ULS-2000H AND ULS-2000R
PART NUMBERING SYSTEM

5

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UL  S - 20  1  3  H - MIL
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INSTRUCTIONS.
MIL = MILITARY GRADE WITH SCREENING TO
MIL-STD-883, CLASS B

PACKAGE DESIGNATION.
C = UNPACKAGED CHIP
H = GLASS/METAL HERMETIC, DUAL IN-LINE
A = PLASTIC, DUAL IN-LINE
R = CERAMIC/GLASS HERMETIC, DUAL IN-LINE

DEVICE INPUT CHARACTERISTICS
1 = GENERAL PURPOSE PMOS/CMOS
2 = 14-25 V PMOS
3 = 5 V TTL/CMOS
4 = 6-15 V CMOS/PMOS
5 = HIGH-OUTPUT TTL

DEVICE OUTPUT CHARACTERISTICS
0 = 50 V AND 500 mA MAXIMUM
1 = 50 V AND 600 mA MAXIMUM
2 = 95 V AND 500 mA MAXIMUM (PACKAGE H OR A ONLY)

DEVICE TYPE NUMBER (4 DIGITS IN 2000 SERIES)

OPERATING AMBIENT TEMPERATURE RANGE.
N = COMMERCIAL (−20°C TO +85°C)
Q = EXTENDED (−40°C TO +85°C)
S = FULL MILITARY (−55°C TO +125°C)

FAMILY.

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE
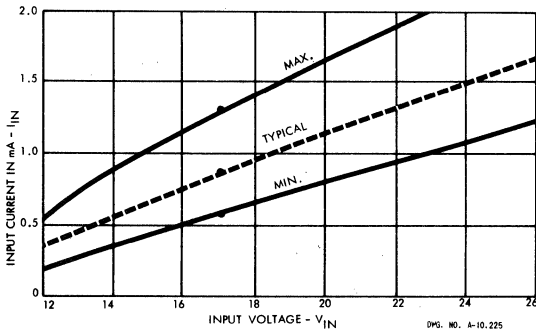
SERIES 2002*

SERIES 2003*
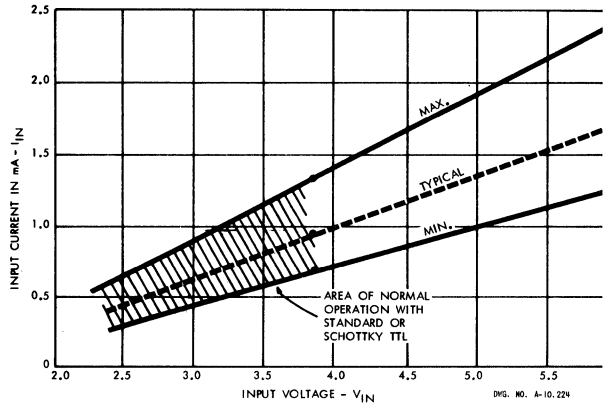
SERIES 2004*
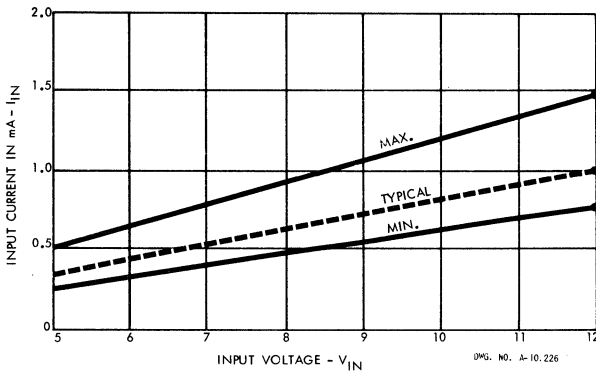
SERIES 2005*
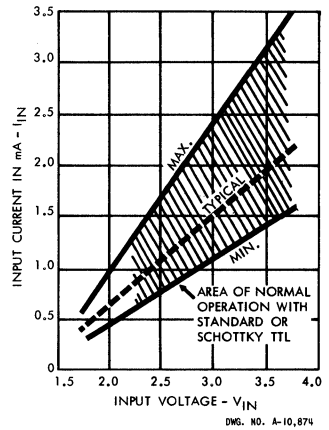
*Complete part number includes a prefix to indicate temperature range and a suffix to indicate package style. See previous part number description.

ULS-2064H THROUGH ULS-2077H
1.25 A QUAD DARLINGTON SWITCHES

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Transient-Protected Outputs
- Hermetically Sealed Package to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B

INTENDED FOR MILITARY, aerospace, and related applications, ULS-2064H through ULS-2077H high-voltage high-current integrated circuit switches will interface from low-level logic to a variety of peripheral loads such as relays, solenoids, d-c and stepping motors, multiplexed LED and incandescent displays, heaters, and similar loads up to 400 W (1.25 A per output, 80 V, 12.5% duty cycle, +50°C).

The devices are specified with a minimum output breakdown of 50 volts, and $V_{CE(SUS)}$ minimum of 35 volts measured at 100 mA, or a minimum output breakdown of 80 volts, $V_{CE(SUS)}$ minimum of 50 volts, and an output current specification of 1.25 A (saturated).

Types ULS-2064H, ULS-2065H, ULS-2068H and ULS-2069H are designed for use with TTL, DTL, Schottky TTL, and 5 V CMOS logic.

Types ULS-2066H, ULS-2067H, ULS-2070H and ULS-2071H are intended for use with 6 V to 15 V CMOS and PMOS input circuits.

All eight of these devices include integral transient suppression diodes for use with inductive loads.

Types ULS-2068H and ULS-2069H incorporate a pre-driver stage requiring a 5 V supply rail. Types ULS-2070H and ULS-2071H include an added gain stage requiring a 12 V (nominal) supply rail. The input drive requirements for these devices are reduced, while the output can switch currents up to 1.5 A.

Types ULS-2074H through ULS-2077H are intended for use in emitter-follower or similar isolated Darlington applications where common-emitter versions cannot be used. These circuits are identical with the ULS-2064H through ULS-2067H types except for the isolated Darlington pin-out and the omission of the suppression diodes.

All twelve Quad Darlington Switches are supplied in 16-pin hermetic dual-in-line packages. They meet the processing and environmental requirements of MIL-STD-883 Methods 5004 and 5005, and the dimensional requirements of MIL-M-38510.
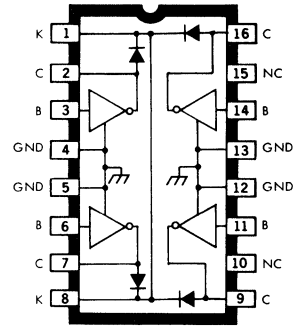
Dwg. No. A-11,025

**ULS-2064H
THROUGH ULS-2067H**
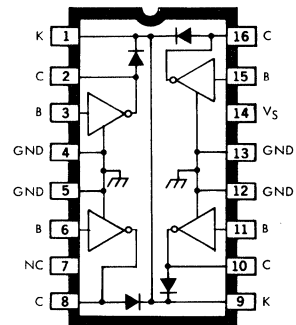
Dwg. No. A-11,026

**ULS-2068H
THROUGH ULS-2071H**
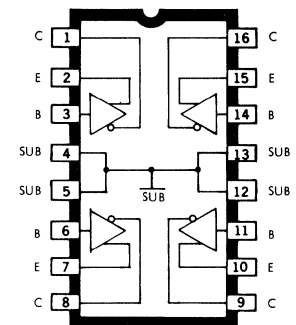
Dwg. No. A-11,027

**ULS-2074H
THROUGH ULS-2077H**

5

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature
for any one driver
(unless otherwise noted)

Output Voltage, V_{CEX} .... See Below
Output Sustaining Voltage, $V_{CE(SUS)}$ .... See Below
Output Current, I_{OUT} (Note 1) .... 1.5 A
Input Voltage, V_{IN} (Note 2) .... See Below
Input Current, I_B (Note 3) .... 25 mA
Supply Voltage, V_S (ULS-2068/69H) .... 10 V
                  (ULS-2070/71H) .... 20 V
Total Package Power Dissipation .... See Graph
Power Dissipation, P_D/Output .... 2.2 W
Operating Ambient Temperature Range, T_A −55°C to +125°C
Storage Temperature Range, T_S .... −65°C to +150°C

PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE

DWG. NO. A-10,198A
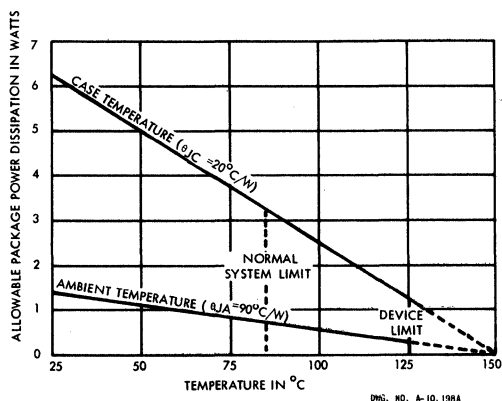
Type Number	V_{CEX} (max.)	$V_{CE(SUS)}$ (min.)	V_{IN} (max.)	Application
ULS-2064H	50 V	35 V	15 V	TTL, DTL, Schottky TTL,
ULS-2065H	80 V	50 V	15 V	and 5 V CMOS
ULS-2066H	50 V	35 V	30 V	6 to 15 V CMOS
ULS-2067H	80 V	50 V	30 V	and PMOS
ULS-2068H	50 V	35 V	15 V	TTL, DTL, Schottky TTL,
ULS-2069H	80 V	50 V	15 V	and 5 V CMOS
ULS-2070H	50 V	35 V	30 V	6 to 15 V CMOS
ULS-2071H	80 V	50 V	30 V	and PMOS
ULS-2074H	50 V	35 V	30 V	General Purpose
ULS-2075H	80 V	50 V	60 V	
ULS-2076H	50 V	35 V	30 V	6 to 15 V CMOS
ULS-2077H	80 V	50 V	60 V	and PMOS

Notes:
1. For allowable combinations of output current, number of outputs conducting, and duty cycle, see graphs following.
2. Input voltage is with reference to the substrate (no connection to any other pins) for the ULS-2074/75/76/77H, reference is ground for all other types.
3. Input current may be limited by maximum allowable input voltage.

ULS-2064H THROUGH ULS-2067H

PARTIAL SCHEMATIC
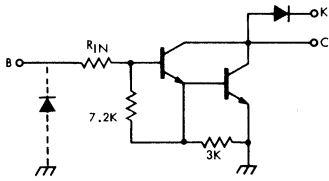
DWG. NO. A-10.353

| ULS-2064H
ULS-2065H | $R_{IN} = 350\ \Omega$ |
| ULS-2066H
ULS-2067H | $R_{IN} = 3\ k\Omega$ |
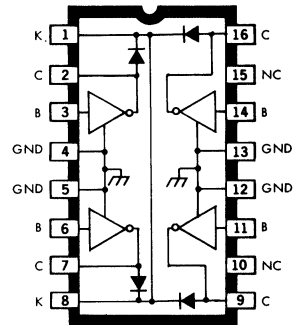
Dwg. No. A-11,025

ULS-2068H THROUGH ULS-2071H

PARTIAL SCHEMATIC
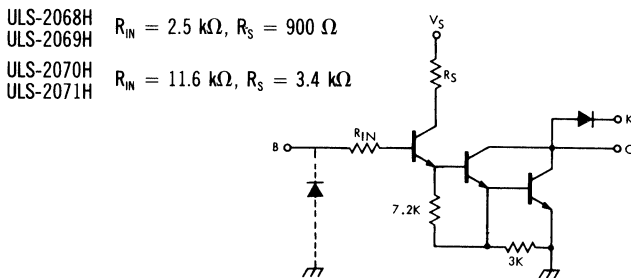
| ULS-2068H
ULS-2069H | $R_{IN} = 2.5\ k\Omega,\ R_S = 900\ \Omega$ |
| ULS-2070H
ULS-2071H | $R_{IN} = 11.6\ k\Omega,\ R_S = 3.4\ k\Omega$ |
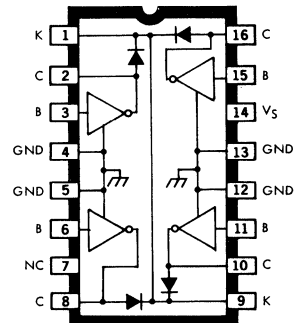
DWG. NO. A-10.354

Dwg. No. A-11,026

ULS-2074H THROUGH ULS-2077H

PARTIAL SCHEMATIC
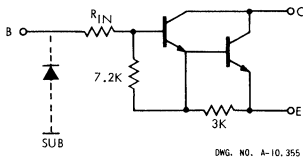
DWG. NO. A-10.355

| ULS-2074H
ULS-2075H | $R_{IN} = 350\ \Omega$ |
| ULS-2076H
ULS-2077H | $R_{IN} = 3\ k\Omega$ |

Dwg. No. A-11,027

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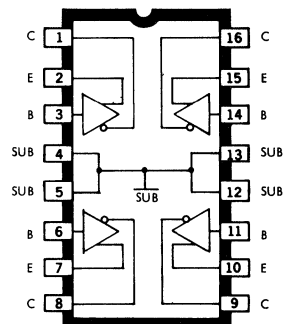
ULS-2064H THROUGH ULS-2067H

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Temp.	Test Conditions	Fig.	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	ULS-2064/66H		$V_{CE} = 50\ V$	1	—	500	μA
		ULS-2065/67H		$V_{CE} = 80\ V$	1	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	ULS-2064/66H		$I_C = 100\ mA,\ V_{IN} = 0.4\ V$	2	35	—	V
		ULS-2065/67H		$I_C = 100\ mA,\ V_{IN} = 0.4\ V$	2	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$		−55°C	$I_C = 500\ mA,\ I_B = 1.1\ mA$	3	—	1.35	V
				$I_C = 750\ mA,\ I_B = 1.7\ mA$	3	—	1.55	V
				$I_C = 1.0\ A,\ I_B = 2.25\ mA$	3	—	1.75	V
				$I_C = 1.25\ A,\ I_B = 3.75\ mA$	3	—	1.95	V
		All	+25°C	$I_C = 500\ mA,\ I_B = 625\ \mu A$	3	—	1.20	V
				$I_C = 750\ mA,\ I_B = 935\ \mu A$	3	—	1.35	V
				$I_C = 1.0\ A,\ I_B = 1.25\ mA$	3	—	1.55	V
				$I_C = 1.25\ A,\ I_B = 2.0\ mA$	3	—	1.75	V
			+125°	$I_C = 500\ mA,\ I_B = 625\ \mu A$	3	—	1.35	V
				$I_C = 750\ mA,\ I_B = 935\ \mu A$	3	—	1.55	V
				$I_C = 1.0\ A,\ I_B = 1.25\ mA$	3	—	1.75	V
				$I_C = 1.25\ A,\ I_B = 2.0\ mA$	3	—	1.95	V
Input Current	$I_{IN(ON)}$			$V_{IN} = 2.4\ V$	4	—	4.3	mA
		ULS-2064/65H		$V_{IN} = 3.75\ V$	4	—	9.6	mA
		ULS-2066/67H		$V_{IN} = 5.0\ V$	4	—	1.8	mA
				$V_{IN} = 12\ V$	4	—	5.2	mA
Input Voltage	$V_{IN(ON)}$		−55°C	$V_{CE} = 2.0\ V,\ I_C = 1.0\ A$	5	—	3.1	V
		ULS-2064/65H	+25°C	$V_{CE} = 2.0\ V,\ I_C = 1.0\ A$	5	—	2.0	V
		ULS-2066/67H	−55°C	$V_{CE} = 2.0\ V,\ I_C = 1.0\ A$	5	—	11.5	V
			+25°C	$V_{CE} = 2.0\ V,\ I_C = 1.0\ A$	5	—	6.5	V
Turn-On Delay	t_{ON}	All		$0.5\ E_{in}$ to $0.5\ E_{out}$	—	—	1.0	μs
Turn-Off Delay	t_{OFF}	All		$0.5\ E_{in}$ to $0.5\ E_{out}$	—	—	1.5	μs
Clamp Diode Leakage Current	I_R	ULS-2064/66H		$V_R = 50\ V$	6	—	100	μA
		ULS-2065/67H		$V_R = 80\ V$	6	—	100	μA
Clamp Diode Forward Voltage	V_F	All		$I_F = 1.25\ A$	7	—	2.1	V

ULS-2068H THROUGH ULS-2071H

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted),
$V_S = 5.0$ V (ULS-2068/69H) or $V_S = 12$ V (ULS-2070/71H)

Characteristic	Symbol	Applicable Devices	Temp.	Test Conditions	Fig.	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	ULS-2068/70H		$V_{CE} = 50$ V	1	—	500	μA
		ULS-2069/71H		$V_{CE} = 80$ V	1	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	ULS-2068/70H		$I_C = 100$ mA, $V_{IN} = 0.4$ V	2	35	—	V
		ULS-2069/71H		$I_C = 100$ mA, $V_{IN} = 0.4$ V	2	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ULS-2068/69H	−55°C	$I_C = 500$ mA, $V_{IN} = 3.2$ V	3	—	1.35	V
				$I_C = 750$ mA, $V_{IN} = 3.2$ V	3	—	1.55	V
				$I_C = 1.0$ A, $V_{IN} = 3.2$ V	3	—	1.75	V
				$I_C = 1.25$ A, $V_{IN} = 3.2$ V	3	—	1.95	V
			+25°C	$I_C = 500$ mA, $V_{IN} = 2.9$ V	3	—	1.20	V
				$I_C = 750$ mA, $V_{IN} = 2.9$ V	3	—	1.35	V
				$I_C = 1.0$ A, $V_{IN} = 2.9$ V	3	—	1.55	V
				$I_C = 1.25$ A, $V_{IN} = 2.9$ V	3	—	1.75	V
			+125°C	$I_C = 500$ mA, $V_{IN} = 2.8$ V	3	—	1.35	V
				$I_C = 750$ mA, $V_{IN} = 2.8$ V	3	—	1.55	V
				$I_C = 1.0$ A, $V_{IN} = 2.8$ V	3	—	1.75	V
				$I_C = 1.25$ A, $V_{IN} = 2.8$ V	3	—	1.95	V
		ULS-2070/71H	−55°C	$I_C = 500$ mA, $V_{IN} = 5.5$ V	3	—	1.35	V
				$I_C = 750$ mA, $V_{IN} = 5.5$ V	3	—	1.55	V
				$I_C = 1.0$ A, $V_{IN} = 5.5$ V	3	—	1.75	V
				$I_C = 1.25$ A, $V_{IN} = 5.5$ V	3	—	1.95	V
			+25°C	$I_C = 500$ mA, $V_{IN} = 5.1$ V	3	—	1.20	V
				$I_C = 750$ mA, $V_{IN} = 5.1$ V	3	—	1.35	V
				$I_C = 1.0$ A, $V_{IN} = 5.1$ V	3	—	1.55	V
				$I_C = 1.25$A, $V_{IN} = 5.1$ V	3	—	1.75	V
			+125°C	$I_C = 500$ mA, $V_{IN} = 5.0$ V	3	—	1.35	V
				$I_C = 750$ mA, $V_{IN} = 5.0$V	3	—	1.55	V
				$I_C = 1.0$ A, $V_{IN} = 5.0$ V	3	—	1.75	V
				$I_C = 1.25$ A, $V_{IN} = 5.0$ V	3	—	1.95	V
Input Current	$I_{IN(ON)}$	ULS-2068/69H	−55°C	$V_{IN} = 3.2$ V	4	—	600	μA
			+25°C	$V_{IN} = 2.75$ V	4	—	550	μA
			+125°C	$V_{IN} = 2.75$ V	4	—	850	μA
				$V_{IN} = 3.75$ V	4	—	1000	μA
		ULS-2070/71H		$V_{IN} = 5.0$ V	4	—	400	μA
				$V_{IN} = 12$ V	4	—	1250	μA
Input Voltage	$V_{IN(ON)}$	ULS-2068/69H	−55°C	$V_{CE} = 2.0$ V, $I_C = 1.0$ A	5	—	3.2	V
			+25°C	$V_{CE} = 2.0$ V, $I_C = 1.0$ A	5	—	2.75	V
		ULS-2070/71H	−55°C	$V_{CE} = 2.0$ V, $I_C = 1.0$ A	5	—	5.0	V
			+25°C	$V_{CE} = 2.0$ V, $I_C = 1.0$ A	5	—	5.0	V
Supply Current	I_S	ULS-2068/69H		$I_C = 500$ mA, $V_{IN} = 3.2$ V	8	—	6.0	mA
		ULS-2070/71H		$I_C = 500$ mA, $V_{IN} = 5.0$ V	8	—	4.5	mA
Turn-On Delay	t_{ON}	All		0.5 E_{in} to 0.5 E_{out}	—	—	1.0	μs
Turn-Off Delay	t_{OFF}	All		0.5 E_{in} to 0.5 E_{out}	—	—	1.5	μs
Clamp Diode Leakage Current	I_R	ULS-2068/70H		$V_R = 50$ V	6	—	100	μA
		ULS-2069/71H		$V_R = 80$ V	6	—	100	μA
Clamp Diode Forward Voltage	V_F	All		$I_F = 1.25$ A	7	—	2.1	V

5

ULS-2074H THROUGH ULS-2077H

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Temp.	Test Conditions	Fig.	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	ULS-2074/76H		$V_{CE} = 50$ V	1	—	500	μA
		ULS-2075/77H		$V_{CE} = 80$ V	1	—	500	μA
Output Sustaining Voltage	$V_{CE(SUS)}$	ULS-2074/76H		$I_C = 100$ mA, $V_{IN} = 0.4$ V	2	35	—	V
		ULS-2075/77H		$I_C = 100$ mA, $V_{IN} = 0.4$ V	2	50	—	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	−55°C	$I_C = 500$ mA, $I_B = 1.1$ mA	3	—	1.35	V
				$I_C = 750$ mA, $I_B = 1.7$ mA	3	—	1.55	V
				$I_C = 1.0$ A, $I_B = 2.25$ mA	3	—	1.75	V
				$I_C = 1.25$ A, $I_B = 3.75$ mA	3	—	1.95	V
			+25°C	$I_C = 500$ mA, $I_B = 625$ μA	3	—	1.20	V
				$I_C = 750$ mA, $I_B = 935$ μA	3	—	1.35	V
				$I_C = 1.0$ A, $I_B = 1.25$ mA	3	—	1.55	V
				$I_C = 1.25$ A, $I_B = 2.0$ mA	3	—	1.75	V
			+125°C	$I_C = 500$ mA, $I_B = 625$ μA	3	—	1.35	V
				$I_C = 750$ mA, $I_B = 935$ μA	3	—	1.55	V
				$I_C = 1.0$ A, $I_B = 1.25$ mA	3	—	1.75	V
				$I_C = 1.25$ A, $I_B = 2.0$ mA	3	—	1.95	V
Input Current	$I_{IN(ON)}$	ULS-2074/75H		$V_{IN} = 2.4$ V	4	—	4.3	mA
				$V_{IN} = 3.75$ V	4	—	9.6	mA
		ULS-2076/77H		$V_{IN} = 5.0$ V	4	—	1.8	mA
				$V_{IN} = 12$ V	4	—	5.2	mA
Input Voltage	$V_{IN(ON)}$	ULS-2074/75H	−55°C	$V_{CE} = 2.0$ V, $I_C = 1.0$ A	5	—	3.1	V
			+25°C	$V_{CE} = 2.0$ V, $I_C = 1.0$ A	5	—	2.0	V
		ULS-2076/77H	−55°C	$V_{CE} = 2.0$ V, $I_C = 1.0$ A	5	—	11.5	V
			+25°C	$V_{CE} = 2.0$ V, $I_C = 1.0$ A	5	—	6.5	V
Turn-On Delay	t_{ON}	All		0.5 E_{in} to 0.5 E_{out}	—	—	1.0	μs
Turn-Off Delay	t_{OFF}	All		0.5 E_{in} to 0.5 E_{out}	—	—	1.5	μs

TEST FIGURES

Figure 1

Figure 2

Figure 3

5
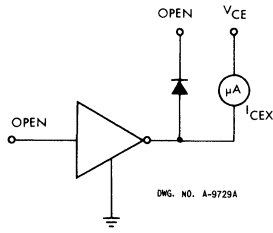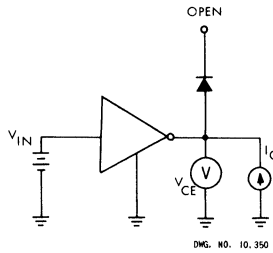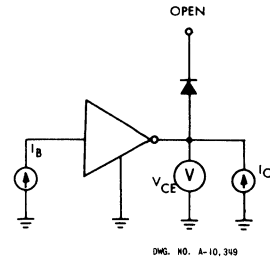
Figure 4

Figure 5

Figure 6

Figure 7

Figure 8

NOTE: Diodes not applicable to Type ULS-2074H through ULS-2077H.

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

ULS-2064/65H
ULS-2074/75H
(Emitters Grounded)

MAXIMUM

MINIMUM

AREA OF NORMAL
OPERATION WITH
STANDARD OR
LOW-SPEED TTL

INPUT CURRENT IN mA - I_{IN}

INPUT VOLTAGE - V_{IN}

DWG. NO. A-11,035

ULS-2066/67H
ULS-2076/77H

MAXIMUM

TYPICAL

MINIMUM

INPUT CURRENT IN mA - I_{IN}

INPUT VOLTAGE - V_{IN}

DWG. NO. A-11,034

COLLECTOR CURRENT AS A FUNCTION
OF INPUT CURRENT

ULS-2064H thru ULS-2067H
ULS-2074H thru ULS-2077H

$T_A = 25/125°C$

$T_A = -55°C$

COLLECTOR CURRENT IN AMPERES - I_c

INPUT CURRENT IN MILLIAMPERES - I_{IN}

Dwg. No. A-11,030
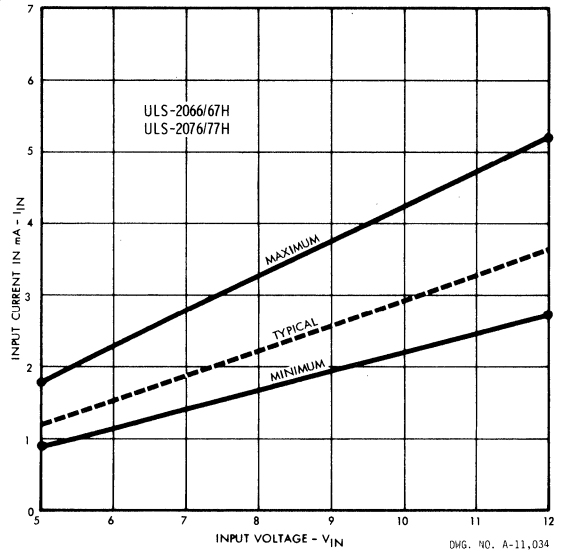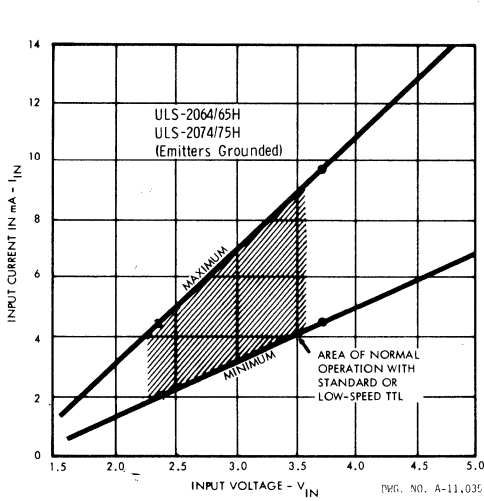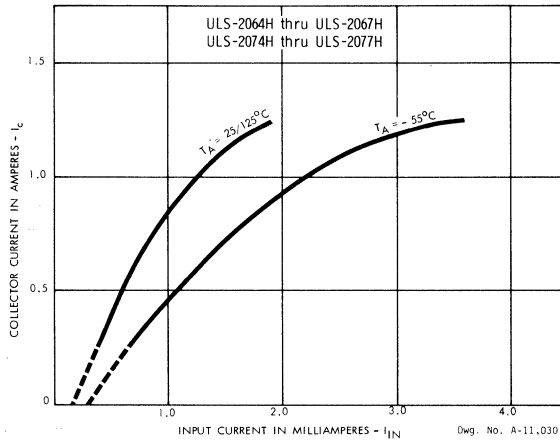
ALLOWABLE PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE

AT +50°C
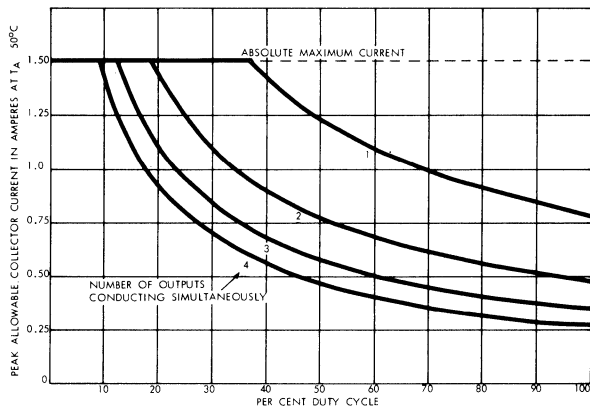
Dwg. No. A-11,031

AT +75°C
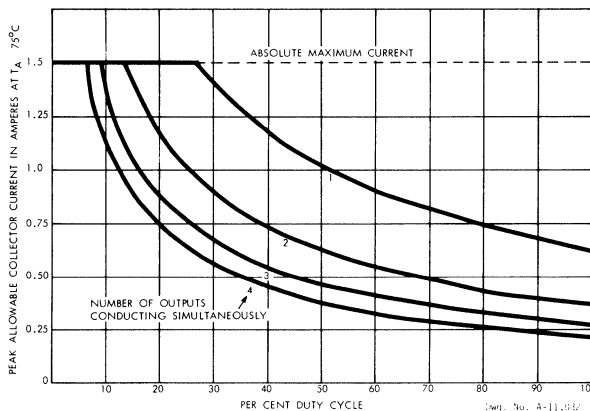
Dwg. No. A-11,032

AT +100°C
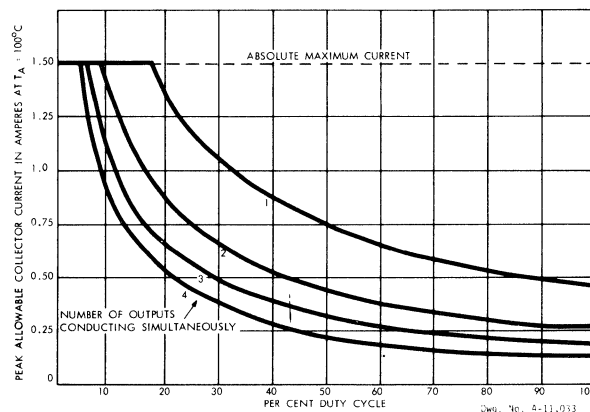
Dwg. No. A-11,033

SERIES ULS-2800H AND ULS-2800R
HIGH-VOLTAGE, HIGH-CURRENT
DARLINGTON TRANSISTOR ARRAYS

FEATURES

- TTL, DTL, PMOS, or CMOS Compatible Inputs
- Peak Output Current to 600 mA
- Transient Protected Outputs
- Side-Brazed Hermetic Package, or
- Cer-DIP Package
- High-Reliability Screening Available
- Wide Operating Temperature Ranges

D⁰G. NO. A-10.327

DESIGNED for interfacing between low-level logic circuitry and high-power loads, the Series ULS-2800H and ULS-2800R arrays consist of eight silicon NPN Darlington power drivers on a common monolithic substrate. The choice of five input characteristics, two output voltage ratings (50 or 95 V), two output current ratings (500 or 600 mA), and two package styles (suffix 'H' or 'R') allow the circuit designer to select the optimum device for any specific application.

Both hermetically sealed package styles are rated for operation over the temperature range of $-55°C$ to $+125°C$, recommending them for military and aerospace applications or commercial and industrial applications where severe environmental conditions may be encountered.

The appropriate specific part number for use in standard logic applications can be determined from the Device Type Number Designation chart. Note that the high-voltage devices ($BV_{CE} \geq 95$ V) are available in the Series ULS-2800H only. All units feature open collector outputs and integral diodes for inductive load transient suppression.
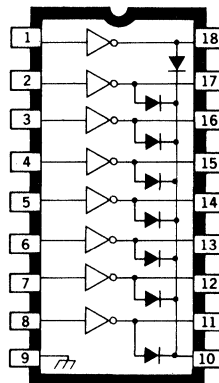
All Series ULS-2800H Darlington power drivers are furnished in an 18-pin side-brazed dual in-line hermetic package that meets the processing and environmental requirements of Military Standard MIL-STD-883, Methods 5004 and 5005.

Device Type Number Designation

$V_{CE(MAX)} =$ $I_{C(MAX)} =$	50 V 500 mA	50 V 600 mA	95 V 500 mA
	Type Number		
General-Purpose PMOS, CMOS	ULS-2801R ULS-2801H	ULS-2811R ULS-2811H	ULS-2821H
14-25 V PMOS	ULS-2802R ULS-2802H	ULS-2812R ULS-2812H	ULS-2822H
5 V TTL, CMOS	ULS-2803R ULS-2803H	ULS-2813R ULS-2813H	ULS-2823H
6-15 V CMOS, PMOS	ULS-2804R ULS-2804H	ULS-2814R ULS-2814H	ULS-2824H
High-Output TTL	ULS-2805R ULS-2805H	ULS-2815R ULS-2815H	ULS-2825H

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE} (Series 2800*, 2810*) .... 50 V

(Series ULS-2020H) .... 95 V

Input Voltage, V_{IN} (Series 2802*, 2803*, 2804*) .... 30 V

(Series 2805*) .... 15 V

Peak Output Current, I_{OUT} (Series 2800*, ULS-2820H) .... 500 mA

(Series 2810*) .... 600 mA

Ground Terminal Current, I_{GND} .... 3.0 A

Continuous Input Current, I_{IN} .... 25 mA

Power Dissipation, P_D (one Darlington pair) .... 1.0 W

(total package) .... See Graphs

Operating Temperature Range, T_A .... $-55°C$ to $+125°C$

Storage Temperature Range, T_S .... $-65°C$ to $+150°C$

PARTIAL SCHEMATICS

5

Series 2801*
(each driver)
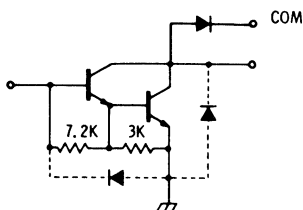
DWG. NO. A-9595

Series 2802*
(each driver)
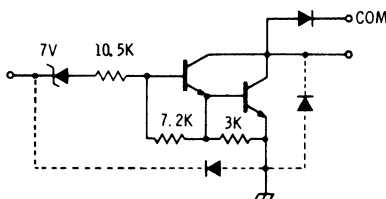
DWG. No. A-9650

Series 2803*
(each driver)
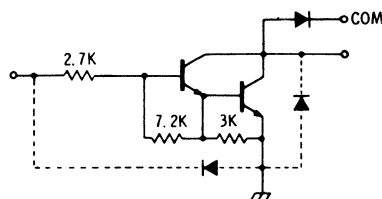
DWG. No. A-9651

Series 2804*
(each driver)
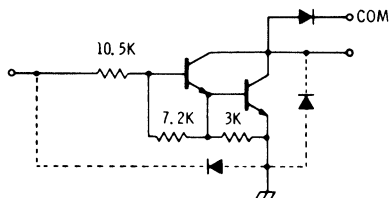
DWG. NO. A-9898A

Series 2805*
(each driver)

DWG. NO. A-10.22H

*Complete part number includes a prefix to indicate temperature range and a suffix to indicate package style. See following part number description.

SERIES ULS-2800H AND ULS-2800R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Temp	Test Conditions	Fig.	Limits Min.	Limits Typ.	Limits Max.	Units
Output Leakage Current	I_{CEX}	All		$V_{CE} = 50\,V$	1A	—	—	100	μA
		2802*		$V_{CE} = 50\,V$, $V_{IN} = 6\,V$	1B	—	—	500	μA
		2804*		$V_{CE} = 50\,V$, $V_{IN} = 1\,V$	1B	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	Min.	$I_C = 350\,mA$, $I_B = 850\,\mu A$	2	—	1.6	1.8	V
				$I_C = 200\,mA$, $I_B = 550\,\mu A$	2	—	1.3	1.5	V
				$I_C = 100\,mA$, $I_B = 350\,\mu A$	2	—	1.1	1.3	V
			+25°C	$I_C = 350\,mA$, $I_B = 500\,\mu A$	2	—	1.25	1.6	V
				$I_C = 200\,mA$, $I_B = 350\,\mu A$	2	—	1.1	1.3	V
				$I_C = 100\,mA$, $I_B = 250\,\mu A$	2	—	0.9	1.1	V
			Max.	$I_C = 350\,mA$, $I_B = 500\,\mu A$	2	—	1.6	1.8	V
				$I_C = 200\,mA$, $I_B = 350\,\mu A$	2	—	1.3	1.5	V
				$I_C = 100\,mA$, $I_B = 250\,\mu A$	2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	2802*		$V_{IN} = 17\,V$	3	480	850	1300	μA
		2803*		$V_{IN} = 3.85\,V$	3	650	930	1350	μA
		2804*		$V_{IN} = 5\,V$	3	240	350	500	μA
				$V_{IN} = 12\,V$	3	650	1000	1450	μA
		2805*		$V_{IN} = 3\,V$	3	1180	1500	2400	μA
	$I_{IN(OFF)}$	All	Max.	$I_C = 500\,\mu A$	4	25	50	—	μA
Input Voltage	$V_{IN(ON)}$	2802*	Min.	$V_{CE} = 2\,V$, $I_C = 300\,mA$	5	—	—	18	V
			Max.	$V_{CE} = 2\,V$, $I_C = 300\,mA$	5	—	—	13	V
		2803*	Min.	$V_{CE} = 2\,V$, $I_C = 200\,mA$	5	—	—	3.3	V
				$V_{CE} = 2\,V$, $I_C = 250\,mA$	5	—	—	3.6	V
				$V_{CE} = 2\,V$, $I_C = 300\,mA$	5	—	—	3.9	V
			Max.	$V_{CE} = 2\,V$, $I_C = 200\,mA$	5	—	—	2.4	V
				$V_{CE} = 2\,V$, $I_C = 250\,mA$	5	—	—	2.7	V
				$V_{CE} = 2\,V$, $I_C = 300\,mA$	5	—	—	3.0	V
		2804*	Min.	$V_{CE} = 2\,V$, $I_C = 125\,mA$	5	—	—	6.0	V
				$V_{CE} = 2\,V$, $I_C = 200\,mA$	5	—	—	8.0	V
				$V_{CE} = 2\,V$, $I_C = 275\,mA$	5	—	—	10	V
				$V_{CE} = 2\,V$, $I_C = 350\,mA$	5	—	—	12	V
			Max.	$V_{CE} = 2\,V$, $I_C = 125\,mA$	5	—	—	5.0	V
				$V_{CE} = 2\,V$, $I_C = 200\,mA$	5	—	—	6.0	V
				$V_{CE} = 2\,V$, $I_C = 275\,mA$	5	—	—	7.0	V
				$V_{CE} = 2\,V$, $I_C = 350\,mA$	5	—	—	8.0	V
		2805*	Min.	$V_{CE} = 2\,V$, $I_C = 350\,mA$	5	—	—	3.0	V
			Max.	$V_{CE} = 2\,V$, $I_C = 350\,mA$	5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2801*	Min.	$V_{CE} = 2\,V$, $I_C = 350\,mA$	2	500	—	—	—
			+25°C	$V_{CE} = 2\,V$, $I_C = 350\,mA$	2	1000	—	—	—
Input Capacitance	C_{IN}	All	+25°C		—	—	15	25	pF
Turn-On Delay	t_{PLH}	All	+25°C	$0.5\,E_{in}$ to $0.5\,E_{out}$	—	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C	$0.5\,E_{in}$ to $0.5\,E_{out}$	—	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		$V_R = 50\,V$	6	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All		$I_F = 350\,mA$	7	—	1.7	2.0	V

*Complete part number includes a prefix to indicate temperature range and a suffix to indicate package style. See following part number description.

Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

SERIES ULS-2810H AND ULS-2810R

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Temp	Test Conditions		Fig.	Limits			Units
							Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	All		$V_{CE} = 50$ V		1A	—	—	100	μA
		2812*		$V_{CE} = 50$ V, $V_{IN} = 6$ V		1B	—	—	500	μA
		2814*		$V_{CE} = 50$ V, $V_{IN} = 1$ V		1B	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	Min.	$I_C = 500$ mA, $I_B = 1100\,\mu$A		2	—	1.8	2.1	V
				$I_C = 350$ mA, $I_B = 850\,\mu$A		2	—	1.6	1.8	V
				$I_C = 200$ mA, $I_B = 550\,\mu$A		2	—	1.3	1.5	V
			+25°C	$I_C = 500$ mA, $I_B = 600\,\mu$A		2	—	1.7	1.9	V
				$I_C = 350$ mA, $I_B = 500\,\mu$A		2	—	1.25	1.6	V
				$I_C = 200$ mA, $I_B = 350\,\mu$A		2	—	1.1	1.3	V
			Max.	$I_C = 500$ mA, $I_B = 600\,\mu$A		2	—	1.8	2.1	V
				$I_C = 350$ mA, $I_B = 500\,\mu$A		2	—	1.6	1.8	V
				$I_C = 200$ mA, $I_B = 350\,\mu$A		2	—	1.3	1.5	V
Input Current	$I_{IN(ON)}$	2812*		$V_{IN} = 17$ V		3	480	850	1300	μA
		2813*		$V_{IN} = 3.85$ V		3	650	930	1350	μA
		2814*		$V_{IN} = 5$ V		3	240	350	500	μA
				$V_{IN} = 12$ V		3	650	1000	1450	μA
		2815*		$V_{IN} = 3$ V		3	1180	1500	2400	μA
	$I_{IN(OFF)}$	All	Max.	$I_C = 500\,\mu$A		4	25	50	—	μA
Input Voltage	$V_{IN(ON)}$	2812*	Min.	$V_{CE} = 2$ V, $I_C = 500$ mA		5	—	—	23.5	V
			Max.	$V_{CE} = 2$ V, $I_C = 500$ mA		5	—	—	17	V
		2813*	Min.	$V_{CE} = 2$ V, $I_C = 250$ mA		5	—	—	3.6	V
				$V_{CE} = 2$ V, $I_C = 300$ mA		5	—	—	3.9	V
				$V_{CE} = 2$ V, $I_C = 500$ mA		5	—	—	6.0	V
			Max.	$V_{CE} = 2$ V, $I_C = 250$ mA		5	—	—	2.7	V
				$V_{CE} = 2$ V, $I_C = 300$ mA		5	—	—	3.0	V
				$V_{CE} = 2$ V, $I_C = 500$ mA		5	—	—	3.5	V
		2814*	Min.	$V_{CE} = 2$ V, $I_C = 275$ mA		5	—	—	10	V
				$V_{CE} = 2$ V, $I_C = 350$ mA		5	—	—	12	V
				$V_{CE} = 2$ V, $I_C = 500$ mA		5	—	—	17	V
			Max.	$V_{CE} = 2$ V, $I_C = 275$ mA		5	—	—	7.0	V
				$V_{CE} = 2$ V, $I_C = 350$ mA		5	—	—	8.0	V
				$V_{CE} = 2$ V, $I_C = 500$ mA		5	—	—	9.5	V
		2815*	Min.	$V_{CE} = 2$ V, $I_C = 350$ mA		5	—	—	3.0	V
				$V_{CE} = 2$ V, $I_C = 500$ mA		5	—	—	3.5	V
			Max.	$V_{CE} = 2$ V, $I_C = 350$ mA		5	—	—	2.4	V
				$V_{CE} = 2$ V, $I_C = 500$ mA		5	—	—	2.6	V
D-C Forward Current Transfer Ratio	h_{FE}	2811*	Min.	$V_{CE} = 2$ V, $I_C = 500$ mA		2	450	—	—	—
			+25°C	$V_{CE} = 2$ V, $I_C = 500$ mA		2	900	—	—	—
Input Capacitance	C_{IN}	All	+25°C			—	—	15	25	pF
Turn-On Delay	t_{PLH}	All	+25°C	0.5 E_{in} to 0.5 E_{out}		—	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C	0.5 E_{in} to 0.5 E_{out}		—	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		$V_R = 50$ V		6	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All		$I_F = 350$ mA		7	—	1.7	2.0	V
				$I_F = 500$ mA		7	—	—	2.5	V

*Complete part number includes a prefix to indicate temperature range and a suffix to indicate package style. See following part number description.

Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

SERIES ULS-2820H

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Temp	Test Conditions		Fig.	Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	All		$V_{CE} = 95\,V$		1A	—	—	100	μA
		2822H		$V_{CE} = 95\,V$, $V_{IN} = 6\,V$		1B	—	—	500	μA
		2824H		$V_{CE} = 95\,V$, $V_{IN} = 1\,V$		1B	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	All	Min.	$I_C = 350\,mA$, $I_B = 850\,\mu A$		2	—	1.6	1.8	V
				$I_C = 200\,mA$, $I_B = 550\,\mu A$		2	—	1.3	1.5	V
				$I_C = 100\,mA$, $I_B = 350\,\mu A$		2	—	1.1	1.3	V
			+25°C	$I_C = 350\,mA$, $I_B = 500\,\mu A$		2	—	1.25	1.6	V
				$I_C = 200\,mA$, $I_B = 350\,\mu A$		2	—	1.1	1.3	V
				$I_C = 100\,mA$, $I_B = 250\,\mu A$		2	—	0.9	1.1	V
			Max.	$I_C = 350\,mA$, $I_B = 500\,\mu A$		2	—	1.6	1.8	V
				$I_C = 200\,mA$, $I_B = 350\,\mu A$		2	—	1.3	1.5	V
				$I_C = 100\,mA$, $I_B = 250\,\mu A$		2	—	1.1	1.3	V
Input Current	$I_{IN(ON)}$	2822H		$V_{IN} = 17\,V$		3	480	850	1300	μA
		2823H		$V_{IN} = 3.85\,V$		3	650	930	1350	μA
		2824H		$V_{IN} = 5\,V$		3	240	350	500	μA
				$V_{IN} = 12\,V$		3	650	1000	1450	μA
		2825H		$V_{IN} = 3\,V$		3	1180	1500	2400	μA
	$I_{IN(OFF)}$	All	Max.	$I_C = 500\,\mu A$		4	25	50	—	μA
Input Voltage	$V_{IN(ON)}$	2822H	Min.	$V_{CE} = 2\,V$, $I_C = 300\,mA$		5	—	—	18	V
			Max.	$V_{CE} = 2\,V$, $I_C = 300\,mA$		5	—	—	13	V
		2823H	Min.	$V_{CE} = 2\,V$, $I_C = 200\,mA$		5	—	—	3.3	V
				$V_{CE} = 2\,V$, $I_C = 250\,mA$		5	—	—	3.6	V
				$V_{CE} = 2\,V$, $I_C = 300\,mA$		5	—	—	3.9	V
			Max.	$V_{CE} = 2\,V$, $I_C = 200\,mA$		5	—	—	2.4	V
				$V_{CE} = 2\,V$, $I_C = 250\,mA$		5	—	—	2.7	V
				$V_{CE} = 2\,V$, $I_C = 300\,mA$		5	—	—	3.0	V
		2824H	Min.	$V_{CE} = 2\,V$, $I_C = 125\,mA$		5	—	—	6.0	V
				$V_{CE} = 2\,V$, $I_C = 200\,mA$		5	—	—	8.0	V
				$V_{CE} = 2\,V$, $I_C = 275\,mA$		5	—	—	10	V
				$V_{CE} = 2\,V$, $I_C = 350\,mA$		5	—	—	12	V
			Max.	$V_{CE} = 2\,V$, $I_C = 125\,mA$		5	—	—	5.0	V
				$V_{CE} = 2\,V$, $I_C = 200\,mA$		5	—	—	6.0	V
				$V_{CE} = 2\,V$, $I_C = 275\,mA$		5	—	—	7.0	V
				$V_{CE} = 2\,V$, $I_C = 350\,mA$		5	—	—	8.0	V
		2825H	Min.	$V_{CE} = 2\,V$, $I_C = 350\,mA$		5	—	—	3.0	V
			Max.	$V_{CE} = 2\,V$, $I_C = 350\,mA$		5	—	—	2.4	V
D-C Forward Current Transfer Ratio	h_{FE}	2821H	Min.	$V_{CE} = 2\,V$, $I_C = 350\,mA$		2	500	—	—	—
			+25°C	$V_{CE} = 2\,V$, $I_C = 350\,mA$		2	1000	—	—	—
Input Capacitance	C_{IN}	All	+25°C			—	—	15	25	pF
Turn-On Delay	t_{PLH}	All	+25°C	$0.5\,E_{in}$ to $0.5\,E_{out}$		—	—	250	1000	ns
Turn-Off Delay	t_{PHL}	All	+25°C	$0.5\,E_{in}$ to $0.5\,E_{out}$		—	—	250	1000	ns
Clamp Diode Leakage Current	I_R	All		$V_R = 95\,V$		6	—	—	50	μA
Clamp Diode Forward Voltage	V_F	All		$I_F = 350\,mA$		7	—	1.7	2.0	V

Note 1: All limits stated apply to the complete Darlington series except as specified for a single device type.
Note 2: The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
Note 3: The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

TEST FIGURES

FIGURE 1A

FIGURE 1B

$$h_{FE} = \frac{I_C}{I_B}$$

FIGURE 2

FIGURE 3

FIGURE 4

FIGURE 5

FIGURE 6

FIGURE 7

5

SERIES ULS-2800H

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE
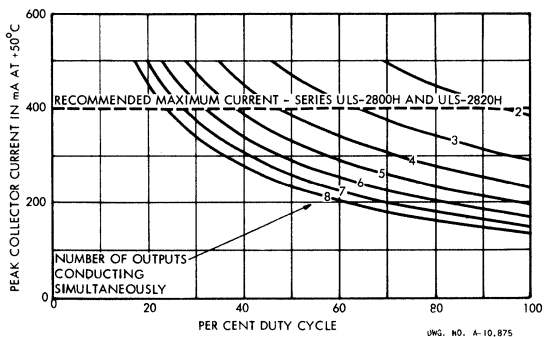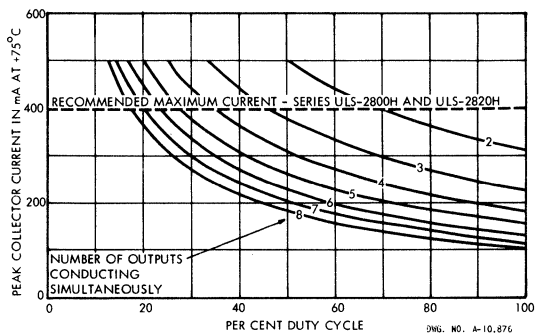
AT +50°C

AT +75°C

AT +100°C
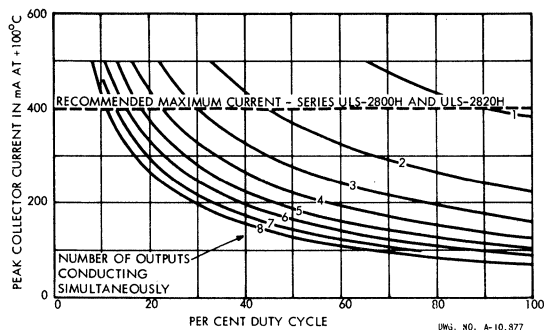
AT +125°C
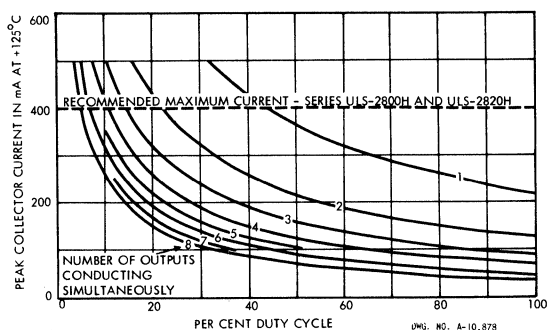
SERIES ULS-2800R

PEAK COLLECTOR CURRENT AS A FUNCTION OF DUTY CYCLE

AT +50°C

DWG. NO. A-10,870

AT +75°C
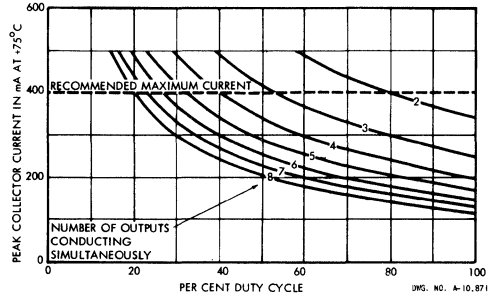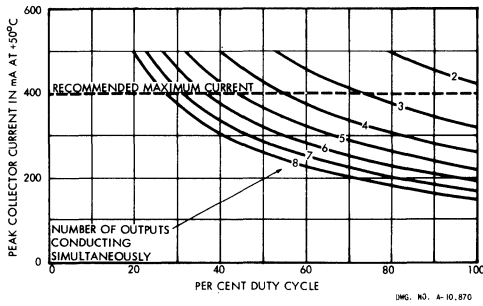
DWG. NO. A-10,871

ALLOWABLE PACKAGE POWER DISSIPATION
SERIES ULS-2800H AND ULS-2800R

Dwg. No. A-10,879A

5—33

COLLECTOR CURRENT
AS A FUNCTION OF INPUT CURRENT

COLLECTOR CURRENT
AS A FUNCTION OF SATURATION VOLTAGE

DWG. NO. A-10.872A

DWG. NO. A-9754B
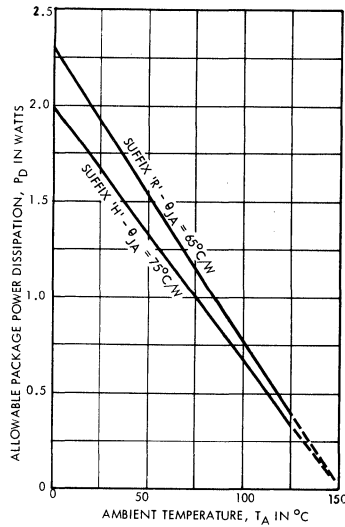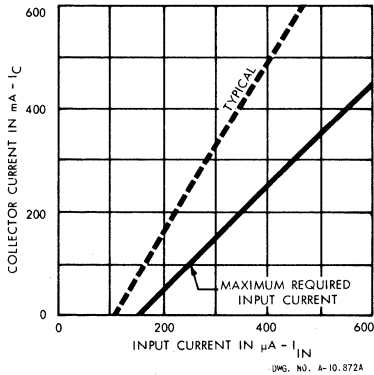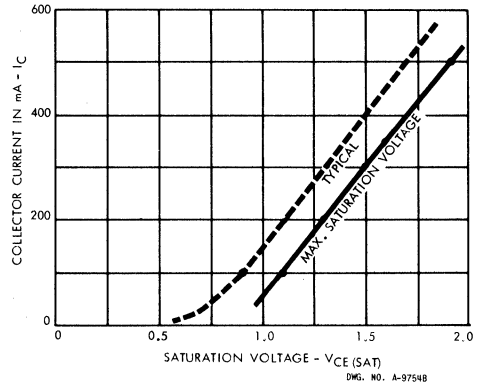
SERIES ULS-2800H AND ULS-2800R
PART NUMBERING SYSTEM

```
UL    S - 28  1  3    H - MIL
```

INSTRUCTIONS.
MIL = MILITARY GRADE WITH SCREENING TO
MIL-STD-883, CLASS B

PACKAGE DESIGNATION.
C = UNPACKAGED CHIP
H = GLASS/METAL HERMETIC, DUAL IN-LINE
A = PLASTIC, DUAL IN-LINE
R = CERAMIC/GLASS HERMETIC, DUAL IN-LINE

DEVICE INPUT CHARACTERISTICS
1 = GENERAL PURPOSE PMOS/CMOS
2 = 14-25 V PMOS
3 = 5 V TTL/CMOS
4 = 6-15 V CMOS/PMOS
5 = HIGH-OUTPUT TTL

DEVICE OUTPUT CHARACTERISTICS
0 = 50 V AND 500 mA MAXIMUM
1 = 50 V AND 600 mA MAXIMUM
2 = 95 V AND 500 mA MAXIMUM (PACKAGE H OR A ONLY)

DEVICE TYPE NUMBER (4 DIGITS IN 2800 SERIES)

OPERATING AMBIENT TEMPERATURE RANGE.
N = COMMERCIAL (−20°C TO +85°C)
Q = EXTENDED (−40°C TO +85°C)
S = FULL MILITARY (−55°C TO +125°C)

FAMILY.

5—34

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

SERIES 2802*

SERIES 2803*
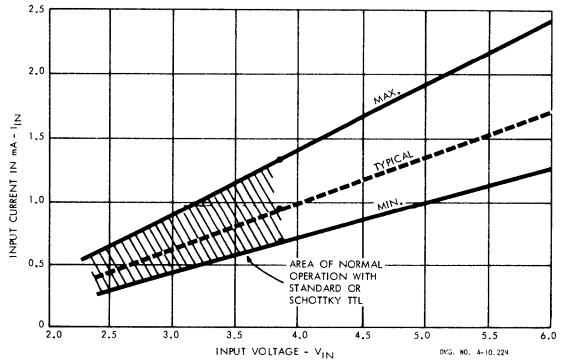
SERIES 2804*
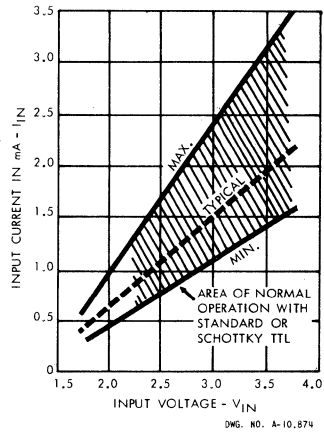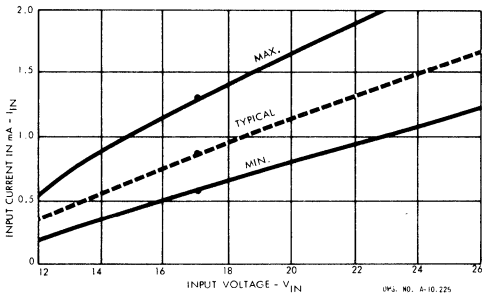
SERIES 2805*

*Complete part number includes a prefix to indicate temperature range and a suffix to indicate package style. See previous part number description.

UDQ-2956R AND UDQ-2957R
HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS

EACH OF THESE SOURCE-DRIVER arrays has five NPN Darlington-pair outputs and five PNP common-base inputs controlled by a single ENABLE stage.

Types UDQ-2956R and UDQ-2957R are typically used to switch the ground ends of loads such as telephone relays, PIN diodes, LEDs and similar devices directly connected to negative supplies. Internal transient-suppression diodes allow use of the drivers with inductive loads.

Each output stage of both integrated circuits will withstand output OFF voltages of − 80 V and load currents as high as − 500 mA. Under normal operating conditions, the five drivers will simultaneously handle load currents of − 170 mA at ambient temperatures of up to + 70°C.

Type UDQ-2956R is designed for use with PMOS or CMOS logic input levels operating with supply voltages of 6 V to 16 V. Type UDQ-2957R has input current-limiting resistors that permit its operation with TTL, Schottky TTL, DTL and 5 V CMOS.

Both devices are supplied in industrial-grade, hermetically sealed 14-pin dual in-line ceramic packages rated for use over the temperature range of − 40°C to + 85°C. Input connections are on one side of the packages, output connections on the other, to simplify applications designs.

The substrate of Type UDQ-2956R and Type UDQ-2957R should be tied to the most negative supply available in order to maintain isolation between drivers.
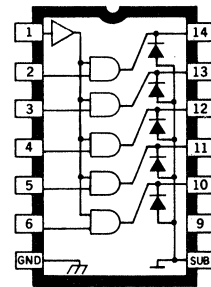
DWG. NO. A-10,229

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature
(reference pin 7)

Supply Voltage, V_{EE} .... −80 V
Input Voltage, V_{IN} (UDQ-2956R) .... +20 V
(UDQ-2957R) .... +10 V
Output Current, I_{OUT} .... −500 mA
Power Dissipation, P_D (any one driver) .... 1.0 W
(total package) .... 1.67 W*
Operating Temperature Range, T_A .... −40°C to +85°C
Storage Temperature Range, T_S .... −65°C to +150°C

*Derate at the rate of 13.3 mW/°C. above +25°C.

These devices can be ordered with an extended temperature range of − 55°C to + 125°C by changing the prefix from 'UDQ' to 'UDS'.

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Applicable Devices	Temp.	Test Conditions	Limit
Output Leakage Current	I_{CEX}	UDQ-2956R		$V_{IN} = V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V	$-200\,\mu$A Max.
				$V_{IN} = 0.4$ V, $V_{ENABLE} = 15$ V, $V_{OUT} = -80$ V	$-200\,\mu$A Max.
				$V_{IN} = 15$ V, $V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V	$-200\,\mu$A Max.
		UDQ-2957R		$V_{IN} = V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V	$-200\,\mu$A Max.
				$V_{IN} = 0.4$ V, $V_{ENABLE} = 3.85$ V, $V_{OUT} = -80$ V	$-200\,\mu$A Max.
				$V_{IN} = 3.85$ V, $V_{ENABLE} = 0.4$ V, $V_{OUT} = -80$ V	$-200\,\mu$A Max.
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	UDQ-2956R	$-40°$C	$V_{IN} = 6.0$ V, $I_{OUT} = -100$ mA	-1.40 V Max.
				$V_{IN} = 7.0$ V, $I_{OUT} = -175$ mA	-1.55 V Max.
				$V_{IN} = 10$ V, $I_{OUT} = -350$ mA	-1.90 V Max.
			$+25°$C	$V_{IN} = 6.0$ V, $I_{OUT} = -100$ mA	-1.20 V Max.
				$V_{IN} = 7.0$ V, $I_{OUT} = -175$ mA	-1.35 V Max.
				$V_{IN} = 10$ V, $I_{OUT} = -350$ mA	-1.70 V Max.
			$+85°$C	$V_{IN} = 6.0$ V, $I_{OUT} = -100$ mA	-1.40 V Max.
				$V_{IN} = 7.0$ V, $I_{OUT} = -175$ mA	-1.55 V Max.
				$V_{IN} = 10$ V, $I_{OUT} = -350$ mA	-1.90 V Max.
		UDQ-2957R	$-40°$C	$V_{IN} = 2.4$ V, $I_{OUT} = -100$ mA	-1.40 V Max.
				$V_{IN} = 2.7$ V, $I_{OUT} = -175$ mA	-1.55 V Max.
				$V_{IN} = 3.9$ V, $I_{OUT} = -350$ mA	-1.90 V Max.
			$+25°$C	$V_{IN} = 2.4$ V, $I_{OUT} = -100$ mA	-1.20 V Max.
				$V_{IN} = 2.7$ V, $I_{OUT} = -175$ mA	-1.35 V Max.
				$V_{IN} = 3.9$ V, $I_{OUT} = -350$ mA	-1.70 V Max.
			$+85°$C	$V_{IN} = 2.4$ V, $I_{OUT} = -100$ mA	-1.40 V Max.
				$V_{IN} = 2.7$ V, $I_{OUT} = -175$ mA	-1.55 V Max.
				$V_{IN} = 3.9$ V, $I_{OUT} = -350$ mA	-1.90 V Max.
Input Current	$I_{IN(ON)}$	UDQ-2956R		$V_{IN} = 6.0$ V, $V_{OUT} = -2.0$ V	0.8 mA Max.
				$V_{IN} = 15$ V, $V_{OUT} = -2.0$ V	2.25 mA Max.
		UDQ-2957R		$V_{IN} = 2.4$ V, $V_{OUT} = -2.0$ V	1.0 mA Max.
				$V_{IN} = 3.85$ V, $V_{OUT} = -2.0$ V	2.0 mA Max.
	$I_{IN(OFF)}$	ALL		$I_{OUT} = -500\,\mu$A	$50\,\mu$A Min.
Output Source Current	I_{OUT}	UDQ-2956R	$-40°$C	$V_{IN} = 5.0$ V, $V_{OUT} = -2.0$ V	-75 mA Min.
				$V_{IN} = 6.0$ V, $V_{OUT} = -2.0$ V	-125 mA Min.
				$V_{IN} = 7.0$ V, $V_{OUT} = -2.0$ V	-175 mA Min.
				$V_{IN} = 8.0$ V, $V_{OUT} = -2.0$ V	-250 mA Min.
				$V_{IN} = 9.0$ V, $V_{OUT} = -2.0$ V	-300 mA Min.
			$+85°$C	$V_{IN} = 5.0$ V, $V_{OUT} = -2.0$ V	-125 mA Min.
				$V_{IN} = 6.0$ V, $V_{OUT} = -2.0$ V	-200 mA Min.
				$V_{IN} = 7.0$ V, $V_{OUT} = -2.0$ V	-250 mA Min.
				$V_{IN} = 8.0$ V, $V_{OUT} = -2.0$ V	-300 mA Min.
				$V_{IN} = 9.0$ V, $V_{OUT} = -2.0$ V	-350 mA Min.
		UDQ-2957R	$-40°$C	$V_{IN} = 2.4$ V, $V_{OUT} = -2.0$ V	-50 mA Min.
				$V_{IN} = 2.7$ V, $V_{OUT} = -2.0$ V	-125 mA Min.
				$V_{IN} = 3.0$ V, $V_{OUT} = -2.0$ V	-200 mA Min.
				$V_{IN} = 3.3$ V, $V_{OUT} = -2.0$ V	-250 mA Min.
				$V_{IN} = 3.6$ V, $V_{OUT} = -2.0$ V	-300 mA Min.
			$+85°$C	$V_{IN} = 2.4$ V, $V_{OUT} = -2.0$ V	-125 mA Min.
				$V_{IN} = 2.7$ V, $V_{OUT} = -2.0$ V	-200 mA Min.
				$V_{IN} = 3.0$ V, $V_{OUT} = -2.0$ V	-250 mA Min.
				$V_{IN} = 3.3$ V, $V_{OUT} = -2.0$ V	-300 mA Min.
				$V_{IN} = 3.6$ V, $V_{OUT} = -2.0$ V	-350 mA Min.
Clamp Diode Leakage Current	I_R	ALL		$V_R = 80$ V	$50\,\mu$A Max.
Clamp Diode Forward Voltage	V_F	ALL		$I_F = 350$ mA	2.0 V Max.
Turn-On Delay	t_{ON}	ALL		$0.5\,E_{IN}$ to $0.5\,E_{OUT}$, $R_L = 400\,\Omega$ $C_T = 25$ pF	$4.0\,\mu$s Max.
Turn-Off Delay	t_{OFF}	ALL		$0.5\,E_{IN}$ to $0.5\,E_{OUT}$, $R_L = 400\,\Omega$ $C_T = 25$ pF	$10\,\mu$s Max.

5

PARTIAL SCHEMATIC

R = 10.5 kΩ for UDQ-2956R
R = 2.5 kΩ for UDQ-2957R

INPUT

ENABLE ①

GROUND ⑦

7.5 K

2.4 K

OUTPUT

SUBSTRATE ⑧

SUB

Dwg. No. A-11,047A

ALLOWABLE PEAK OUTPUT CURRENT
AS A FUNCTION OF DUTY CYCLE

ABSOLUTE MAXIMUM CURRENT

ALLOWABLE PEAK OUTPUT CURRENT IN mA AT 70°C

NUMBER OF OUTPUTS
CONDUCTING SIMULTANEOUSLY

PER CENT DUTY CYCLE

Dwg. No. A-11,046

INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE
at T_A = +25°C

UDQ-2956R

MAX

TYP

INPUT CURRENT IN mA

INPUT VOLTAGE IN VOLTS   Dwg. No. A-11,044A

UDQ-2957R

MAX

TYP

INPUT CURRENT IN mA

INPUT VOLTAGE IN VOLTS   Dwg. No. A-11,045A

SERIES UDS-2980H
HIGH-VOLTAGE, HIGH-CURRENT SOURCE DRIVERS
— Hermetically Sealed

FEATURES:
- TTL, DTL, PMOS or CMOS Compatible Inputs
- −500 mA Output Source Current Capability
- Transient-Protected Outputs
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature −55°C to +125°C

DWG. NO. A-10,243

S ERIES UDS-2980H HERMETICALLY SEALED source drivers interface between standard low-power digital logic, and relays, solenoids, stepping motors, LEDs, lamps, etc., in applications requiring separate logic and load grounds, load supply voltages to +80V, and/or load currents to 500 mA.

Under normal operating conditions these devices will sustain 50 mA continuously on each of the eight outputs, at an ambient temperature of +85°C, with a supply of +15 V. All four devices incorporate input current limiting resistors and output suppression diodes.

UDS-2981H and UDS-2983H drivers are intended for use with +5 V logic systems (TTL, Schottky TTL, DTL and 5 V CMOS). UDS-2982H and UDS-2984H drivers are intended for MOS interface (PMOS and CMOS) operating from supply voltages of from +6 to +16 V.

UDS-2981H and UDS-2982H drivers will sustain a maximum output OFF voltage of +50 V; UDS-2983H and UDS-2984H drivers a maximum output OFF voltage of +80 V.

In all cases the output is switched ON by an active high input level.

Note that the maximum current rating may not be obtained at −55°C because of beta fall-off, or at +125°C because of package power limitations.
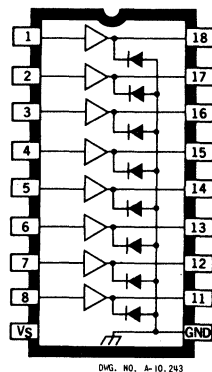
Series UDS-2980H drivers are furnished in 18-pin hermetic dual-in-line packages, and are processed to the requirements of MIL-STD-883, Methods 5004 and 5005.

ABSOLUTE MAXIMUM RATINGS
at $T_A = +25°C$

Output Voltage Range, V_{CE}
  (UDS-2981H & UDS-2982H) . . . . +5 to +50 V
  (UDS-2983H & UDS-2984H) . . . . +35 to +80 V
Input Voltage, V_{IN} (UDS-2981H & UDS-2983H) . . . . +15 V
              (UDS-2982H & UDS-2984H) . . . . +30 V
Output Current, I_{OUT} . . . . −500 mA
Power Dissipation, P_D (any one driver) . . . . 1.1 W
            (total package) 1.67W*
Operating Temperature Range, T_A . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

*Derate at 13.3 mW/°C above 25°C.

ONE OF EIGHT DRIVERS

DWG. NO. A-11,130B
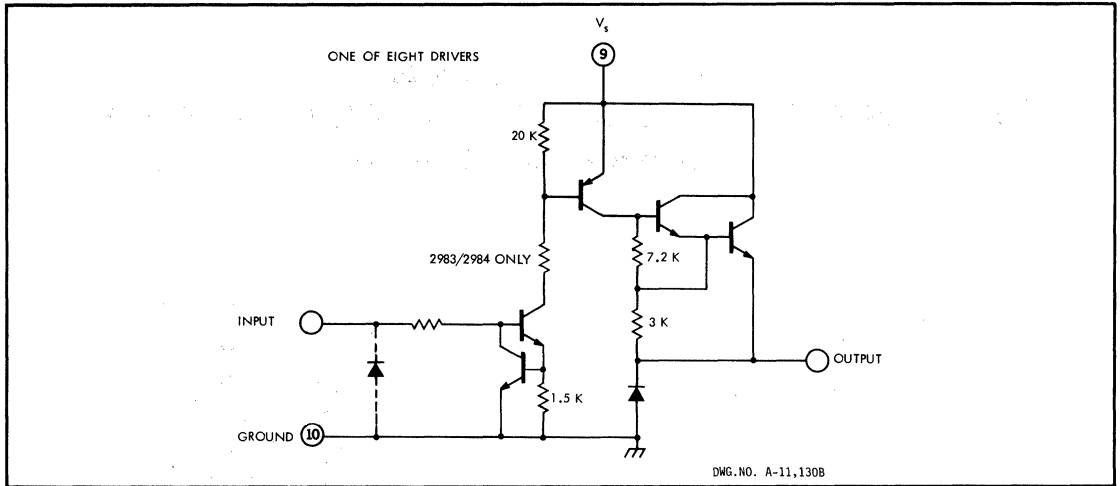
ELECTRICAL CHARACTERISTICS from −55°C to +125°C (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Temp.	Test Conditions	Fig.	Limit
Output Leakage Current	I_{CEX}	UDS-2981/82H		$V_{IN} = 0.25$ V*, $V_S = 50$ V	1	200 μA Max.
		UDS-2983/84H		$V_{IN} = 0.25$ V*, $V_S = 80$ V	1	200 μA Max.
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	UDS-2981/83H	−55°C	$V_{IN} = 2.4$ V, $I_{OUT} = -100$ mA	2	2.0 V Max.
				$V_{IN} = 2.4$ V, $I_{OUT} = -200$ mA	2	2.1 V Max.
			+25°C	$V_{IN} = 2.4$ V, $I_{OUT} = -350$ mA	2	2.0 V Max.
			+125°C	$V_{IN} = 2.4$ V, $I_{OUT} = -100$ mA	2	1.8 V Max.
				$V_{IN} = 2.4$ V, $I_{OUT} = -200$ mA**	2	1.9 V Max.
		UDS-2982/84H	−55°C	$V_{IN} = 5.0$ V, $I_{OUT} = -100$ mA	2	2.0 V Max.
				$V_{IN} = 5.0$ V, $I_{OUT} = -200$ mA	2	2.1 V Max.
			+25°C	$V_{IN} = 5.0$ V, $I_{OUT} = -350$ mA	2	2.0 V Max.
			+125°C	$V_{IN} = 5.0$ V, $I_{OUT} = -100$ mA	2	1.8 V Max.
				$V_{IN} = 5.0$ V, $I_{OUT} = -200$ mA**	2	1.9 V Max.
Input Current	$I_{IN(ON)}$	UDS-2981/83H		$V_{IN} = 2.4$ V	3	575 μA Max.
				$V_{IN} = 3.85$ V	3	1.26 mA Max.
		UDS-2982/84H		$V_{IN} = 5.0$ V	3	640 μA Max.
				$V_{IN} = 12$ V	3	1.8 mA Max.
	$I_{IN(OFF)}$	UDS-2981/82H		$V_{IN} = 0$ V, $V_S = 50$ V	3	10 μA Max.
		UDS-2983/84H		$V_{IN} = 0$ V, $V_S = 80$ V	3	10 μA Max.
Output Source Current	I_{OUT}	UDS-2981/83H		$V_{IN} = 2.4$ V, $V_{CE} = 2.2$ V	2	−200 mA Min.
		UDS-2982/84H		$V_{IN} = 5.0$ V, $V_{CE} = 2.2$ V	2	−200 mA Min.
Supply Current (Outputs Open)	I_S	UDS-2981H	+25°C	$V_{IN} = 2.4$ V*, $V_S = 50$ V	4	10 mA Max.
		UDS-2982H		$V_{IN} = 5.0$ V*, $V_S = 50$ V	4	10 mA Max.
		UDS-2983H		$V_{IN} = 2.4$ V*, $V_S = 80$ V	4	10 mA Max.
		UDS-2984H		$V_{IN} = 5.0$ V*, $V_S = 80$ V	4	10 mA Max.
Clamp Diode Leakage Current	I_R	UDS-2981/82H		$V_S = 50$ V (All Inputs $V_{IN} = 0.25$ V)	5	50 μA Max.
		UDS-2983/84H		$V_S = 80$ V (All Inputs $V_{IN} = 0.25$ V)	5	50 μA Max.
Clamp Diode Forward Voltage	V_F	ALL		$I_F = 200$ mA	6	1.75 V Max.

*All inputs simultaneously.
**Pulsed test.

TEST FIGURES
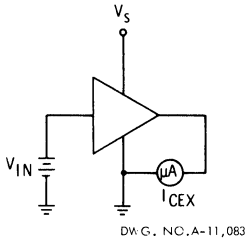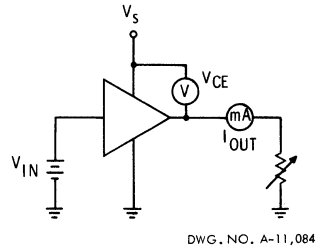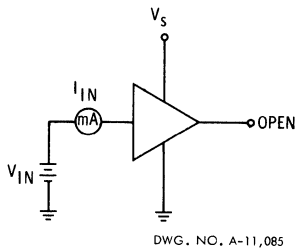
DWG. NO. A-11,083

Figure 1

DWG. NO. A-11,084

Figure 2

DWG. NO. A-11,085

Figure 3

DWG. NO. A-11,086

Figure 4
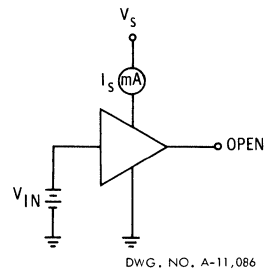
DWG. NO. A-11,087
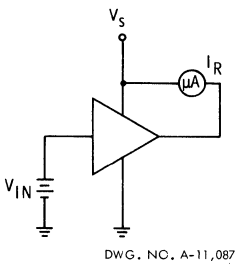
Figure 5
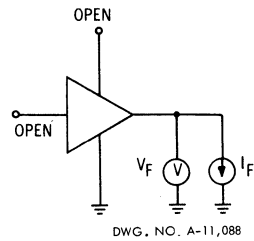
DWG. NO. A-11,088

Figure 6

ALLOWABLE PEAK COLLECTOR CURRENT
AS A FUNCTION OF DUTY CYCLE

UDS-2981/82H
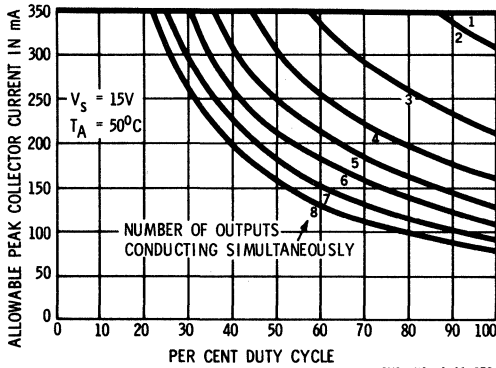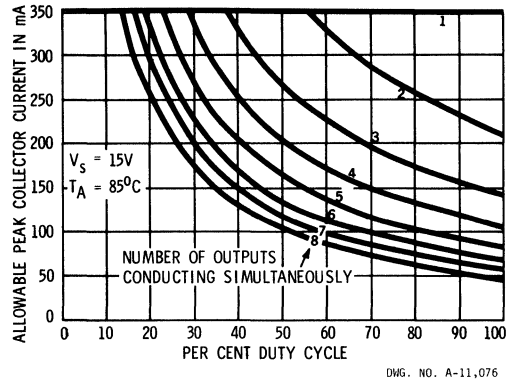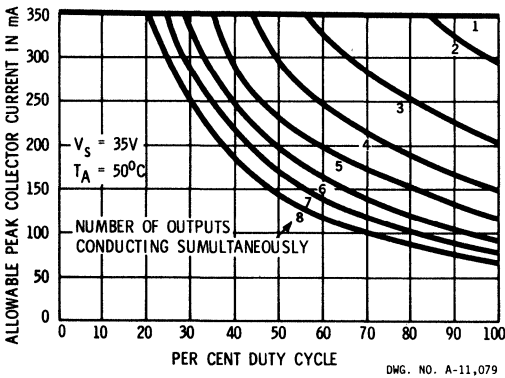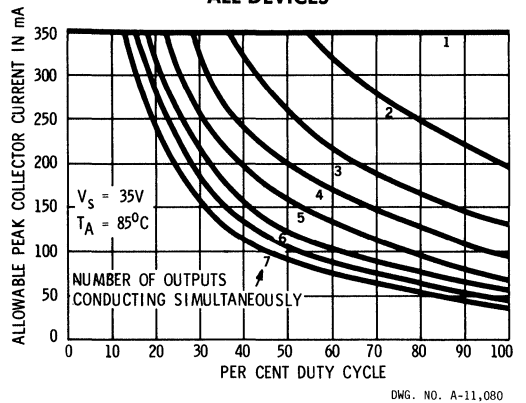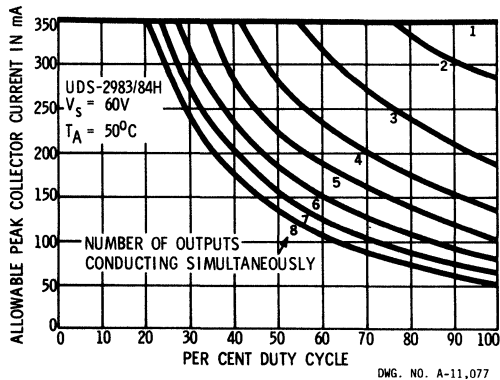
DWG. NO. A-11,078

UDS-2981/82H

DWG. NO. A-11,076

ALL DEVICES

DWG. NO. A-11,079

ALL DEVICES

DWG. NO. A-11,080

UDS-2983/84H

DWG. NO. A-11,077

UDS-2983/84H

DWG. NO. A-11,081

INPUT CURRENT AS A FUNCTION
OF INPUT VOLTAGE FOR TYPE UDS-2981/83H

UDS-2981/83H

MAX.

TYP.
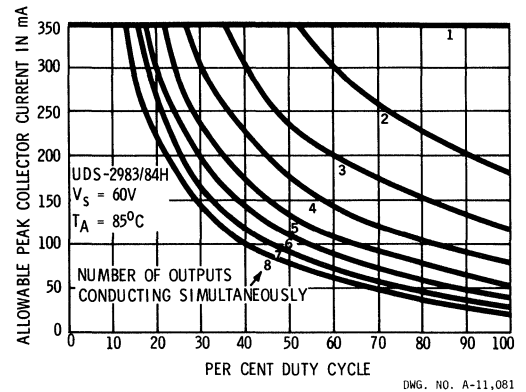
INPUT CURRENT I_{IN} (mA)

INPUT VOLTAGE (VOLTS)

DWG. NO. A-11,074

INPUT CURRENT AS A FUNCTION
OF INPUT VOLTAGE FOR TYPE UDS-2982/84H

UDS-2982/84H

MAX.

TYP.

INPUT CURRENT I_{IN} (mA)

INPUT VOLTAGE (VOLTS)

5

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE

ALLOWABLE PACKAGE POWER DISSIPATION IN WATTS

CASE TEMPERATURE ($\theta_{JC} = 20°C/W$)

AMBIENT TEMPERATURE ($\theta_{JA} = 75°C/W$)

NORMAL
SYSTEM LIMIT

DEVICE
LIMIT

TEMPERATURE IN °C

DWG. NO. A-11,082

SERIES UDS-3600H DUAL 2-INPUT PERIPHERAL AND POWER DRIVERS
— Hermetically Sealed

DWG. NO. A-9792

UDS-3611H

FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Sustaining Voltage of 80 V
- Hermetically Sealed Package
- High-Reliability Screening to MIL-STD-883, Class B

Description

These "mini-DIP" dual 2-input peripheral and power drivers are bi-polar monolithic integrated circuits incorporating AND, NAND, OR, or NOR logic gates, and high-current switching transistors on the same chip. The two output transistors are capable of simultaneously sinking 250 mA continuously at an ambient temperature of +75°C. In the OFF state, these drivers will sustain at least 80 V.

Applications

The Series UDS-3600H dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

With appropriate external diode transient suppression, the Series UDS-3600H drivers can also be used with inductive loads such as relays, solenoids, and stepping motors.

DWG. NO. A-9793

UDS-3612H

DWG. NO. A-9795

UDS-3613H

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 7.0 V
Input Voltage, V_{in} .... 30 V
Output Off-State Voltage, V_{off} .... 80 V
Output On-State Sink Current, I_{on} .... 600 mA
Power Dissipation, P_D (one output) .... 1.0 W
                    (total package) .... See Graph
Ambient Temperature Range (operating), T_A .... −55°C to +125°C
Storage Temperature Range, T_S .... −65°C to +150°C

DWG. NO. A-9794

UDS-3614H

PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE

DWG. NO. A-10,978

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into any output (ON state)	—	—	300	mA

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
				Test Conditions			Limits				
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.7	V	
"0" Input Current	$I_{in(0)}$		MAX	0.4 V	30 V			50	100	μA	2
"1" Input Current	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS at V_{CC} = 5.0V, T_A = 25°C

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
			Limits				
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF	—	200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF	—	300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

Type UDS-3611H Dual AND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	150 mA		0.4	0.5	V	
			MIN	0.8 V	V_{CC}	300 mA		0.6	0.8	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			35	49	mA	1, 2

Type UDS-3612H Dual NAND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	-2.0 V	150 mA		0.4	0.5	V	
			MIN	2.0 V	2.0 V	300 mA		0.6	0.8	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	53	mA	1, 2

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

Type UDS-3613H Dual OR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	150 mA		0.4	0.5	V	
			MIN	0.8 V	0.8 V	300 mA		0.6	0.8	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			36	50	mA	1, 2

DWG. NO. A-7877B

DWG. No. A-7628C

Type UDS-3614H Dual NOR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	150 mA		0.4	0.5	V	
			MIN	2.0 V	0 V	300 mA		0.6	0.8	V	
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	50	mA	1, 2

DWG. NO. A-9942

DWG. NO. A-7900A

NOTES:
1. Typical values are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
2. Per package.
3. Capacitance values specified include probe and test fixture capacitance.

UCS-4401H AND UCS-4801H
BiMOS LATCHED DRIVERS
— Hermetically Sealed

FEATURES

- High-Voltage, High-Current Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, TTL Compatible
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

HIGH-VOLTAGE, HIGH-CURRENT interface for military, aerospace and related applications is supplied by these latched drivers. Type UCS-4401H contains four pairs of latches and drivers; Type UCS-4801H has eight pairs of latches and drivers.

The integrated circuits' CMOS inputs work with standard CMOS, PMOS and NMOS logic levels and (with appropriate pull-up resistors) with TTL or DTL circuits. The bipolar open-collector outputs can be used with relays, solenoids, motors, LED or incandescent displays, and other high-power loads.

The output transistors can sink 500 mA and will withstand a V_{CE} of 50 V in the OFF state. Outputs can be paralleled for higher current capability. Because of limitations on package power dissipation, simultaneous operation of all drivers at maximum rated current can only be accomplished with a reduction of duty cycle.

Type UCS-4401H, the four-latch device, is furnished in a standard 14-pin side-brazed hermetic package. Type UCS-4801H, the eight-latch device, is furnished in a 22-pin side-brazed hermetic package with row centers 0.400-inch (10.16 mm) apart.

Both devices meet all processing and environmental requirements of Military Standard MIL-STD-883, Methods 5004 and 5005.
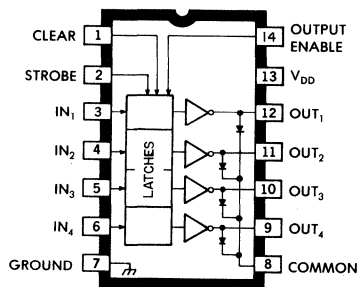
DWG.NO. A-10,499A

UCS-4401H
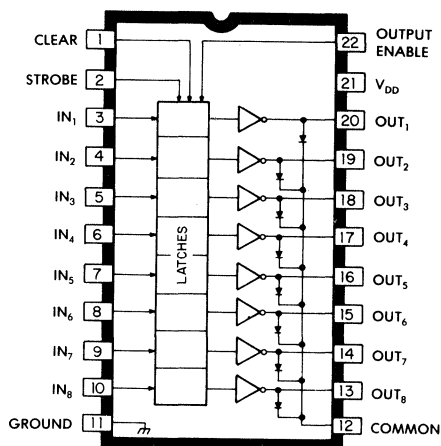
DWG.NO. A-10,498A

UCS-4801H

ABSOLUTE MAXIMUM RATINGS

Output Voltage, V_{CE} . . . . 50 V
Supply Voltage, V_{DD} . . . . 18 V
Input Voltage Range, V_{IN} . . . . −0.3 V to V_{DD} +0.3 V
Continuous Collector Current, I_C . . . . 500 mA
Package Power Dissipation, P_D . . . . See Graph
Operating Ambient Temperature Range, T_A . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

CAUTION: Sprague CMOS devices have input static protection but are still susceptible to damage when exposed to extremely high static electrical charges.

FUNCTIONAL BLOCK DIAGRAM

DWG.NO. A-10,495A
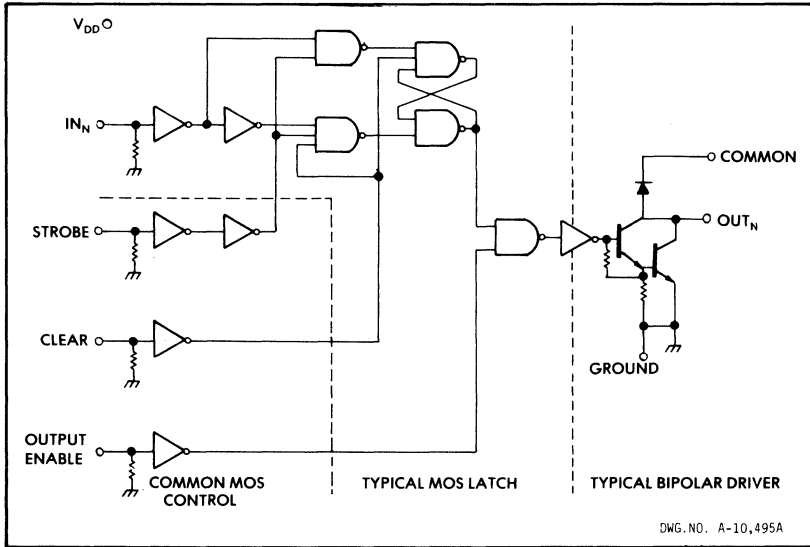
ALLOWABLE AVERAGE
PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE
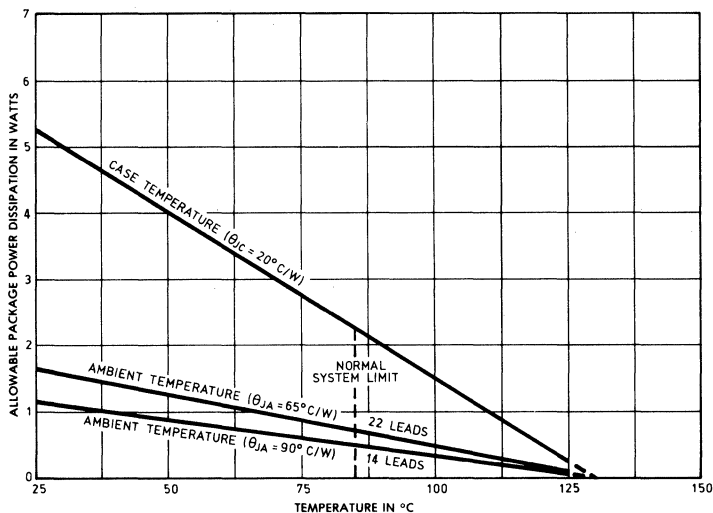
Dwg. No. A-11,464

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5\,V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
				Limits		
Output Leakage Current	I_{CEX}	$V_{CE} = 50\,V$	—	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\,mA$	—	0.9	1.1	V
		$I_C = 200\,mA$	—	1.1	1.3	V
		$I_C = 350\,mA$, $V_{DD} = 7.0\,V$	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 15\,V$	13.5	—	—	V
		$V_{DD} = 10\,V$	8.5	—	—	V
		$V_{DD} = 5.0\,V$ (See note)	3.5	—	—	V
Input Resistance	R_{IN}	$V_{DD} = 15\,V$	50	200	—	kΩ
		$V_{DD} = 10\,V$	50	300	—	kΩ
		$V_{DD} = 5.0\,V$	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 15\,V$, Outputs open	—	1.0	2.0	mA
		$V_{DD} = 10\,V$, Outputs open	—	0.9	1.7	mA
		$V_{DD} = 5.0\,V$, Outputs open	—	0.7	1.0	mA
	$I_{DD(OFF)}$	$V_{DD} = 5.0\,V$, All drivers OFF, All inputs $= 0\,V$	—	50	100	μA
		$V_{DD} = 15\,V$, All drivers OFF, All inputs $= 0\,V$	—	—	200	μA
Clamp Diode Leakage Current	I_R	$V_R = 50\,V$	—	—	50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350\,mA$	—	1.7	2.0	V

Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure the minimum logic "I".

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{DD} = 5 V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
					Limits	
Output Leakage Current	I_{CEX}	$V_{CE} = 50 V$	—	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100 mA$	—	—	1.3	V
		$I_C = 200 mA$	—	—	1.5	V
		$I_C = 350 mA$, $V_{DD} = 7.0 V$	—	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 15 V$	14	—	—	V
		$V_{DD} = 10 V$	9.0	—	—	V
		$V_{DD} = 5.0 V$ (See note)	3.6	—	—	V
Input Resistance	R_{IN}	$V_{DD} = 15 V$	35	—	—	$k\Omega$
		$V_{DD} = 10 V$	35	—	—	$k\Omega$
		$V_{DD} = 5.0 V$	35	—	—	$k\Omega$
Supply Current	$I_{DD(ON)}$	$V_{DD} = 15 V$, Ouputs open	—	1.0	2.5	mA
	(Each Stage)	$V_{DD} = 10 V$, Outputs open	—	0.9	1.7	mA
		$V_{DD} = 5.0 V$, Outputs open	—	0.7	1.0	mA
	$I_{DD(OFF)}$	$V_{DD} = 5.0 V$, All drivers OFF, All inputs = 0 V	—	50	100	μA
		$V_{DD} = 15 V$, All drivers OFF, All inputs = 0 V	—	—	200	μA
Clamp Diode Leakage Current	I_R	$V_R = 50 V$	—	—	50	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350 mA$	—	—	2.1	V

5

ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{DD} = 5 V$ (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
					Limits	
Output Leakage Current	I_{CEX}	$V_{CE} = 50 V$	—	—	500	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100 mA$*	—	—	1.3	V
		$I_C = 200 mA$*	—	—	1.5	V
		$I_C = 350 mA$, $V_{DD} = 7.0 V$*	—	—	1.8	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 15 V$	13.5	—	—	V
		$V_{DD} = 10 V$	8.5	—	—	V
		$V_{DD} = 5.0 V$ (See note)	3.5	—	—	V
Input Resistance	R_{IN}	$V_{DD} = 15 V$	50	—	—	$k\Omega$
		$V_{DD} = 10 V$	50	—	—	$k\Omega$
		$V_{DD} = 5.0 V$	50	—	—	$k\Omega$
Supply Current	$I_{DD(ON)}$	$V_{DD} = 15 V$, Outputs open	—	1.0	2.2	mA
	(Each Stage)	$V_{DD} = 10 V$, Outputs open	—	0.9	1.9	mA
		$V_{DD} = 5.0 V$, Outputs open	—	0.7	1.2	mA
	$I_{DD(OFF)}$	$V_{DD} = 5.0 V$, All drivers OFF, All inputs = 0 V	—	50	100	μA
		$V_{DD} = 15 V$, All drivers OFF, All inputs = 0 V	—	—	200	μA
Clamp Diode Leakage Current	I_R	$V_R = 50 V$	—	—	500	μA
Clamp Diode Forward Voltage	V_F	$I_F = 350 mA$*	—	—	2.0	V

Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure the minimum logic "1".
*Pulsed test.

TIMING CONDITIONS
$T_A = +25°C$; Logic Levels are V_{DD} and V_{SS}

DWG.NO. A-10,895A

A. Minimum data active time before strobe enabled (data set-up time) . . . . 100 ns
B. Minimum data active time after strobe disabled (data hold time) . . . . 100 ns
C. Minimum strobe pulse width . . . . 300 ns
D. Typical time between strobe activation and output on to off transition . . . . 500 ns
E. Typical time between strobe activation and output off to on transition . . . . 500 ns
F. Minimum clear pulse width . . . . 300 ns
G. Minimum data pulse width . . . . 500 ns

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

TRUTH TABLE

IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant
t-1 = previous output state
t = present output state

UCS-4810H
BiMOS 10-BIT, SERIAL-INPUT, LATCHED DRIVER
— Hermetically Sealed

FEATURES

- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Logic and Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature −55°C to +125°C

Pin connections:
- OUT_8 [1] — [18] OUT_9
- OUT_7 [2] — [17] OUT_{10}
- OUT_6 [3] — [16] SERIAL DATA OUT
- CLOCK [4] — LATCHES / REGISTER — [15] V_{BB}
- V_{SS} [5] — REGISTER — [14] SERIAL DATA IN
- V_{DD} [6] — LATCHES — [13] BLANKING
- STROBE [7] — [12] OUT_1
- OUT_5 [8] — [11] OUT_2
- OUT_4 [9] — [10] OUT_3

Dwg. No. A-10,988

5

COMBINING low-power CMOS logic with bipolar source drivers, Type UCS-4810H will simplify many display-system designs. Primarily intended for use with vacuum-fluorescent displays, this BiMOS 10-bit serial-input, latched driver can also be used with LED and incandescent displays within its output limitations of 60 V and 40 mA per driver.

The CMOS 10-bit shift register and associated latches are designed for operation over a 5 V to 15 V supply-voltage range. They cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or low-speed TTL logic, appropriate pull-up resistors may be required to ensure an input-logic high. A CMOS serial-data output allows cascading these devices for interface applications requiring many drive lines (dot matrix, alphanumeric, bargraph).

The 10 bipolar outputs are used as segment or digit drivers in vacuum-fluorescent displays. Under normal operating conditions, these devices will sustain
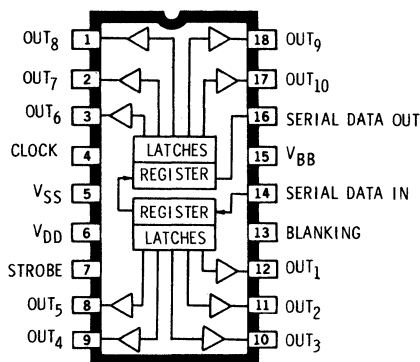
25 mA per output at 50°C at a duty cycle of 61%. Other combinations of number of conducting outputs and duty cycle are shown in the specifications in this bulletin.

Type UCS-4810H, when combined with Type UCS-4815H, an 8-bit latched source driver, comprises a minimum component display subsystem requiring few, if any, discrete components.

Type UCS-4810H is furnished in an 18-pin hermetic dual-in-line package and is processed to the requirements of MIL-STD-883, Methods 5004 and 5005.

The same circuit is also available, with increased allowable package power dissipation, in plastic or glass/ceramic (cer-DIP) hermetic packages for operation over the extended temperature range of −40°C to +85°C (Type UCQ-4810A or UCQ-4810R, respectively). Devices for use over a commercial/industrial temperature range are designated Type UCN-4810A or UCN-4810R, respectively.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
and $V_{SS} = 0 V$

Output Voltage, V_{OUT} .... 60 V

Logic Supply Voltage Range, V_{DD} .... 4.5 V to 18 V

Driver Supply Voltage Range, V_{BB} .... 5.0 V to 60 V

Input Voltage Range, V_{IN} .... -0.3 V to V_{DD} +0.3 V

Continuous Output Current, I_{OUT} .... -40 mA

Package Power Dissipation, P_D .... 1.4 W*

Operating Temperature Range, T_A .... $-55°C$ to $+125°C$

Storage Temperature Range, T_S .... $-65°C$ to $+150°C$

*Derate at 13.3 mW/°C above +25°C.

Number of Outputs ON ($I_{OUT} = -25$ mA)	Maximum Allowable Duty Cycle at $V_{DD} = 5$ V and T_A of:		
	+25°C	+50°C	+85°C
10	81%	61%	34%
9	90%	68%	38%
8	98%	76%	43%
7	100%	87%	49%
6		97%	57%
5		100%	69%
4			86%
3			100%

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

FUNCTIONAL BLOCK DIAGRAM
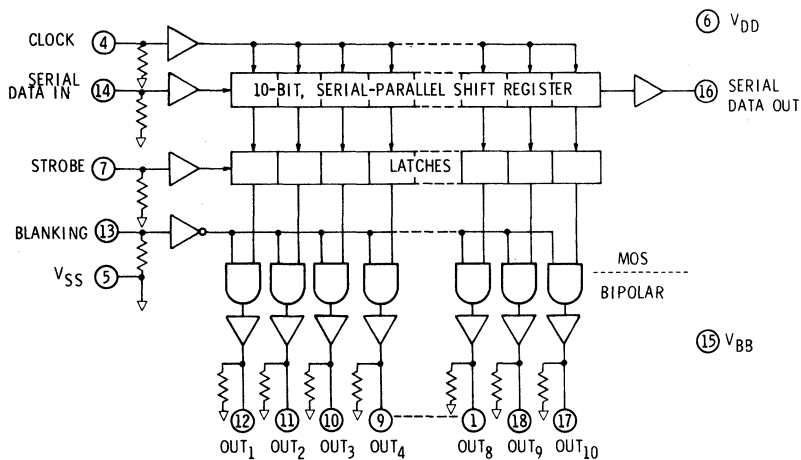
Dwg. No. A-10,989

TYPICAL INPUT CIRCUIT
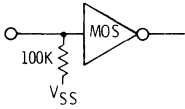
Dwg. No. A-10,980

TYPICAL OUTPUT DRIVER
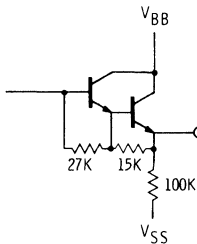
Dwg. No. A-10,981

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE
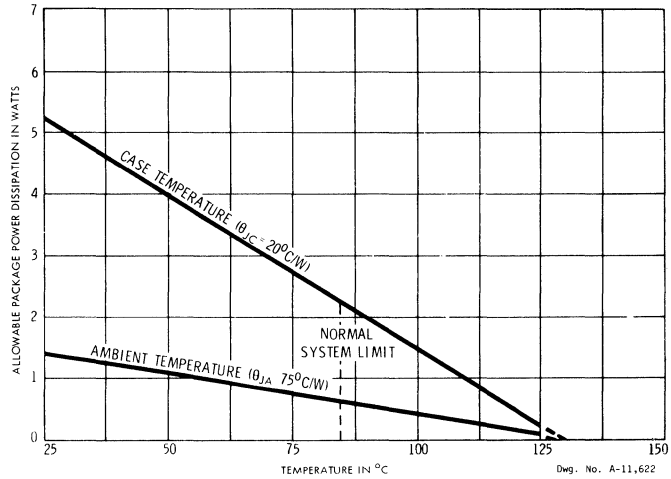
Dwg. No. A-11,622

5

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 60$ V, $V_{DD} = 4.75$ V to 15.75 V, $V_{SS} = 0$ V
(unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Max.	Units
				Limits	
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	850	μA
Output Leakage Current			—	−15	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	—	V
		$V_{DD} = 15$ V	13.5	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	100	μA
		$V_{DD} = V_{IN} = 15$ V	—	300	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	$V_{DD} = 5.0$ V	—	20	kΩ
		$V_{DD} = 15$ V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	13	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	μA
		$V_{DD} = 15$ V, All outputs OFF, All inputs = 0 V	—	200	μA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 15$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{BB} = 60$ V, $V_{DD} = 4.75$ V to 15.75 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	300	850	μA
Output Leakage Current			—	−15	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.6	—	V
		$V_{DD} = 15$ V	14	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	145	μA
		$V_{DD} = V_{IN} = 15$ V	—	430	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	35	—	kΩ
Serial Data Output Resistance	R_{OUT}	$V_{DD} = 5.0$ V	—	20	kΩ
		$V_{DD} = 15$ V	—	6.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	13	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	μA
		$V_{DD} = 15$ V, All outputs OFF, All inputs = 0 V	—	200	μA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 15$ V, One output ON, All inputs = 0 V	—	3.0	mA

ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{BB} = 60$ V, $V_{DD} = 4.75$ V to 15.75 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	1400	μA
Output Leakage Current			—	−30	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	—	V
		$V_{DD} = 15$ V	13.5	—	V
	$V_{IN(0)}$		−0.3	+0.8	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	100	μA
		$V_{DD} = V_{IN} = 15$ V	—	300	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	50	—	kΩ
Serial Data Output Resistance	R_{OUT}	$V_{DD} = 5.0$ V	—	27	kΩ
		$V_{DD} = 15$ V	—	8.0	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	15	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	μA
		$V_{DD} = 15$ V, All outputs OFF, All inputs = 0 V	—	200	μA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.5	mA
		$V_{DD} = 15$ V, One output ON, All inputs = 0 V	—	4.5	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

Dwg. No. A-10,990

TIMING CONDITIONS

$T_A = +25°C$; Logic Levels are V_{DD} and V_{SS}

	$V_{DD} = 5.0$ V	$V_{DD} = 15$ V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	250 ns	150 ns
B. Minimum Data Pulse Width	500 ns	300 ns
C. Minimum Clock Pulse Width	1.0 μs	250 ns
D. Minimum Time Between Clock Activation and Strobe	1.0 μs	400 ns
E. Minimum Strobe Pulse Width	500 ns	300 ns
F. Typical Time Between Strobe Activation and Output Transition	1.0 μs	1.0 μs

SERIAL DATA present at the input is transferred to the shift register on the logic ''0'' to logic ''1'' transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are by-passed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the BLANKING input low, the outputs are controlled by the state of the latches.

UCS-4810H TRUTH TABLES

Serial Data Input	Clock Input	Shift Register Contents I_1 I_2 I_3 . . . . . I_8 I_9 I_{10}	Serial Data Output	Strobe Input	Latch Contents I_1 I_2 I_3 . . . . . I_8 I_9 I_{10}	Blanking Input	Output Contents I_1 I_2 I_3 . . . . . I_8 I_9 I_{10}
H	⌐⌐	H R_1 R_2 . . . R_7 R_8 R_9	R_9				
L	⌐⌐	L R_1 R_2 . . . R_7 R_8 R_9	R_9				
X	⌐⌐	R_1 R_2 R_3 . . R_8 R_9 R_{10}	R_{10}				
		X X X . . . . . . X X X	X	L	R_1 R_2 R_3 . . R_8 R_9 R_{10}		
		P_1 P_2 P_3 . . P_8 P_9 P_{10}	P_{10}	H	P_1 P_2 P_3 . . P_8 P_9 P_{10}	L	P_1 P_2 P_3 . . P_8 P_9 P_{10}
					X X X . . . . . . X X X	H	L L L . . . . L L L

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

UCS-4815H
BiMOS LATCH/SOURCE DRIVER
— Hermetically Sealed

FEATURES

- High-Voltage Source Outputs
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Low-Power CMOS Latches
- Internal Pull-Down Resistors
- Wide Supply-Voltage Range
- High-Reliability Screening to MIL-STD-883, Class B
- Operating Temperature −55°C to +125°C

Dwg. No. A-10,987

DESIGNED primarily for use with high-voltage vacuum-fluorescent displays, the Type UCS-4815H BiMOS integrated circuit has eight NPN Darlington source drivers with pull-down resistors, a CMOS latch for each driver, and common strobe, blanking, and enable functions.

The CMOS inputs cause minimum loading and are compatible with standard CMOS, PMOS, and NMOS logic commonly found in microprocessor designs. The use of CMOS latches also allows operation over a supply-voltage range of 5 V to 15 V. When employed with either standard TTL or low-speed TTL, Type UCS-4815H may require the use of appropriate pull-up resistors.

The bipolar outputs may be used as segment, dot (matrix), bar, or digit drivers in vacuum-fluorescent displays. Under normal operating conditions, these devices will sustain 25 mA per output at 50°C and a duty cycle of 89%. Other combinations of numbers of conducting outputs and duty cycle are shown in the specifications in this bulletin.

A minimum component display subsystem, requiring few or no discrete components, may be as-

sembled by using a Type UCS-4815H BiMOS latch/source driver with a Type UCS-4810H serial-to-parallel latch/driver.
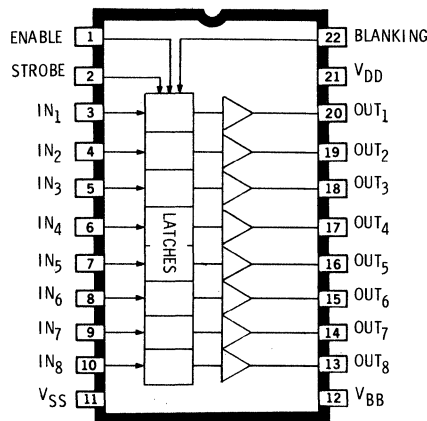
Type UCS-4815H is furnished in 22-pin hermetic dual-in-line packages, and is processed to the requirements of MIL-STD-883, Methods 5004 and 5005. To simplify printed wiring board layout, output pins on the package are opposite respective input pins.

The same circuit is also available, with increased allowable package power dissipation, in plastic or glass/ceramic (cer-DIP) hermetic packages for operation over the extended temperature range of −40°C to +85°C (Type UCQ-4815A or UCQ-4815R, respectively). Devices for use over a commercial/industrial temperature range are designated Type UCN-4815A or UCN-4815R, respectively.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
and V_{SS} = 0 V

Output Voltage, V_{OUT} .... 60 V

Logic Supply Voltage Range, V_{DD} .... 4.5 V to 18 V

Driver Supply Voltage Range, V_{BB} .... 5.0 V to 60 V

Input Voltage Range, V_{IN} .... −0.3 V to V_{DD} +0.3 V

Continuous Output Current, I_{OUT} .... −40 mA

Package Power Dissipation, P_D .... 1.6 W*

Operating Temperature Range, T_A .... −55°C to +125°C

Storage Temperature Range, T_S .... −65°C to +150°C

*Derate at 15.4 mW/°C above +25°C.

Number of Outputs ON (I_{OUT} = −25 mA)	Maximum Allowable Duty Cycle at V_{DD} = 5 V and T_A of:		
	+25°C	+50°C	+85°C
8	100%	89%	56%
7		98%	57%
6		100%	66%
5			80%
4			100%

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE
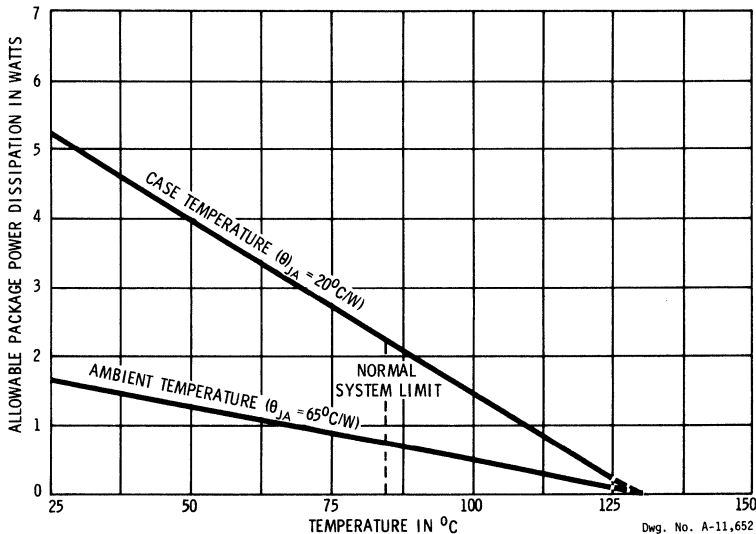
Dwg. No. A-11,652

TYPICAL INPUT CIRCUIT
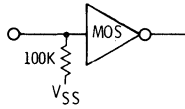
Dwg. No. A-10,980

TYPICAL OUTPUT DRIVER
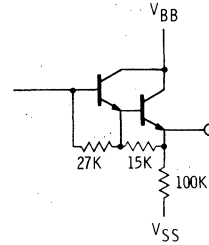
Dwg. No. A-10,981

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{BB} = 60$ V, $V_{DD} = 4.75$ V to 15.75 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Max.	Units
			Limits		
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57.5	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	850	μA
Output Leakage Current			—	-15	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	5.3	V
		$V_{DD} = 15$ V	13.5	15.3	V
	$V_{IN(0)}$		-0.3	$+0.8$	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	100	μA
		$V_{DD} = V_{IN} = 15$ V	—	300	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	10.5	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	μA
		$V_{DD} = 15$ V, All outputs OFF, All inputs = 0 V	—	200	μA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 15$ V, One output ON, All inputs = 0 V	—	3.0	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{BB} = 60$ V, $V_{DD} = 4.75$ V to 15.75 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	300	850	μA
Output Leakage Current			—	-15	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.6	—	V
		$V_{DD} = 15$ V	14	—	V
	$V_{IN(0)}$		-0.3	$+0.8$	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	145	μA
		$V_{DD} = V_{IN} = 15$ V	—	430	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	35	—	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	10.5	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	μA
		$V_{DD} = 15$ V, All outputs OFF, All inputs = 0 V	—	200	μA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.0	mA
		$V_{DD} = 15$ V, One output ON, All inputs = 0 V	—	3.0	mA

ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{BB} = 60$ V, $V_{DD} = 4.75$ V to 15.75 V, $V_{SS} = 0$ V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Max.	Units
Output OFF Voltage	V_{OUT}		—	1.0	V
Output ON Voltage		$I_{OUT} = -25$ mA	57	—	V
Output Pull-Down Current	I_{OUT}	$V_{OUT} = V_{BB}$	400	1400	μA
Output Leakage Current			—	-30	μA
Input Voltage	$V_{IN(1)}$	$V_{DD} = 5.0$ V	3.5	—	V
		$V_{DD} = 15$ V	13.5	—	V
	$V_{IN(0)}$		-0.3	$+0.8$	V
Input Current	$I_{IN(1)}$	$V_{DD} = V_{IN} = 5.0$ V	—	100	μA
		$V_{DD} = V_{IN} = 15$ V	—	300	μA
Input Impedance	Z_{IN}	$V_{DD} = 5.0$ V	50	—	kΩ
Supply Current	I_{BB}	All outputs ON, Outputs open	—	12	mA
		All outputs OFF, Outputs open	—	100	μA
	I_{DD}	$V_{DD} = 5.0$ V, All outputs OFF, All inputs = 0 V	—	100	μA
		$V_{DD} = 15$ V, All outputs OFF, All inputs = 0 V	—	200	μA
		$V_{DD} = 5.0$ V, One output ON, All inputs = 0 V	—	1.5	mA
		$V_{DD} = 15$ V, One output ON, All inputs = 0 V	—	4.5	mA

NOTES: Positive (negative) current is defined as going into (coming out of) the specified device pin.
Operation of this device with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

5

Dwg. No. A-10,991

TIMING CONDITIONS

$T_A = +25°C$; Logic Levels are V_{DD} and V_{SS}

A. Minimum Data Active Time Before Strobe Enabled (Data Set-Up Time) .... 100 ns
B. Minimum Data Active Time After Strobe Disabled (Data Hold Time) .... 100 ns
C. Typical Strobe Pulse Width For Power-Up Clear Disable .... 500 ns
    Minimum Strobe Pulse Width After Power-Up Clear Disabled .... 300 ns
D. Typical Time Between Strobe Activation and Output On to Off Transition .... 1.0 μs
E. Typical Time Between Strobe Activation and Output Off to On Transition .... 1.0 μs
F. Minimum Data Pulse Width .... 500 ns

Information present at an input is transferred to its latch when the STROBE and ENABLE are high. The latches will continue to accept new data as long as both STROBE and ENABLE are held high. With either STROBE or ENABLE in the low state, no information can be loaded into the latches.

When the BLANKING input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches. With the BLANKING input low, the outputs are controlled by the state of the latches.

On first applying V_{DD} to the device, all latch outputs assume a low state (Power-Up Clear) resulting in all outputs being OFF. The latches will remain in the low condition until the Clear is disabled by a STROBE high input. Data may be entered into the latches during Power-Up Clear disable if the ENABLE input is also high.

UCS-4815H TRUTH TABLE

Inputs				OUT$_N$	
IN$_N$	STROBE	ENABLE	BLANK	T-1	T
0	1	1	0	X	0
1	1	1	0	X	1
X	X	X	1	X	0
X	0	X	0	1	1
X	0	X	0	0	0
X	X	0	0	1	1
X	X	0	0	0	0

X = irrelevant
T-1 = previous output state
T = present output state

SERIES UCS-4820H
BiMOS 8-BIT, SERIAL-INPUT, LATCHED DRIVERS
— Hermetically Sealed

FEATURES

- High-Voltage Current-Sink Outputs
- CMOS, PMOS, NMOS, TTL Compatible
- Low-Power CMOS Logic and Latches
- Internal Pull-Up/Pull-Down Resistors
- Hermetically Sealed Packages to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B

INTENDED FOR MILITARY, aerospace, and related applications, Series UCS-4820H 8-bit, serial-input, latched drivers combine bipolar Darlington drivers with MOS logic circuitry (BiMOS) to provide an interface flexibility beyond the reach of standard logic buffers and power driver arrays. Except for the maximum allowable driver output-voltage ratings, Types UCS-4821H (50 V), UCS-4822H (80 V), and UCS-4823H (100 V) are identical.

Each driver contains a CMOS shift register and associated latches designed for operation over a 5 V to 15 V supply-voltage range. High-impedance inputs cause minimal loading of data lines and are compatible with standard CMOS, PMOS, and NMOS logic. When used with standard TTL or Schottky TTL, appropriate pull-up resistors may be required to ensure an input-logic high. The CMOS serial-data output allows cascading these devices for interface applications requiring additional drive lines.

The eight high-current bipolar outputs can drive multiplexed LED displays, incandescent lamps, thermal print heads, and (with appropriate clamping techniques) relays, solenoids and other high-power inductive loads. Under normal operating conditions,

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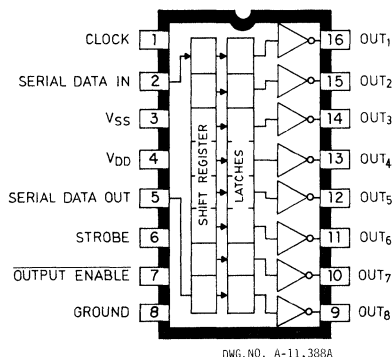
and without heat sinking, these devices can sustain 200 mA per output at 50°C at a 42% duty cycle. Other combinations of number of conducting outputs, temperature, and duty cycle are shown on the following page.

Series UCS-4820H is furnished in 16-pin side-brazed dual in-line hermetic packages that meet the processing and environmental requirements of Military Standard MIL-STD-883, Methods 5004 and 5005.

These same circuits are also available, with increased allowable package power dissipation, in glass/ceramic (cer-DIP) hermetic packages or plastic packages for operation over the extended temperature range of −40°C to +85°C (Series UCQ-4820R or UCQ-4820A, respectively). Devices for use over a commercial/industrial temperature range are designated Series UCN-4820R or UCN-4820A, respectively.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
and $V_{SS} = 0$ V

Output Voltage, V_{OUT} (UCS-4821H) .... 50 V

                 (UCS-4822H) .... 80 V

                 (UCS-4823H) .... 100 V

Logic Supply Voltage, V_{DD} .... 18 V

Input Voltage Range, V_{IN} .... -0.3 V to V_{DD} $+0.3$ V

Continuous Output Current, I_{OUT} .... 500 mA

Package Power Dissipation, P_D .... See Graph

Operating Temperature Range, T_A .... $-55°C$ to $+125°C$

Storage Temperature Range, T_S .... $-65°C$ to $+150°C$

Number of Outputs ON ($I_{OUT} = 200$ mA)	Maximum Allowable Duty Cycle at $V_{DD} = 5$ V and T_A of:		
	+25°C	+50°C	+85°C
8	50%	42%	18%
7	63%	48%	21%
6	74%	56%	25%
5	88%	67%	30%
4	100%	84%	37%
3		100%	50%
2			75%
1			100%

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

FUNCTIONAL BLOCK DIAGRAM

Dwg. No. A-11,391B

TYPICAL INPUT CIRCUITS

DWG. NO. A-11,389A

**ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE**

DWG. NO. A-11,677

TYPICAL OUTPUT DRIVER

Dwg. No. A-11,390

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5V$, $V_{SS} = 0V$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Min.	Max.	Units
Output Leakage Current	I_{CEX}	UCS-4821H	$V_{OUT} = 50 V$	—	50	μA
		UCS-4822H	$V_{OUT} = 80 V$	—	50	μA
		UCS-4823H	$V_{OUT} = 100 V$	—	50	μA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_{OUT} = 100 mA$	—	1.1	V
			$I_{OUT} = 200 mA$	—	1.3	V
			$I_{OUT} = 350 mA$, $V_{DD} = 7.0 V$	—	1.6	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	$V_{DD} = 15 V$	13.5	—	V
			$V_{DD} = 10 V$	8.5	—	V
			$V_{DD} = 5.0 V$ (See note)	3.5	—	V
Input Resistance	R_{IN}	ALL	$V_{DD} = 15 V$	50	—	$k\Omega$
			$V_{DD} = 10 V$	50	—	$k\Omega$
			$V_{DD} = 5.0 V$	50	—	$k\Omega$
Supply Current	$I_{DD(ON)}$	ALL	One driver ON, $V_{DD} = 15 V$	—	2.0	mA
			One driver ON, $V_{DD} = 10 V$	—	1.7	mA
			One driver ON, $V_{DD} = 5.0 V$	—	1.0	mA
	$I_{DD(OFF)}$	ALL	$V_{DD} = 5.0 V$, All drivers OFF, All inputs = 0 V	—	100	μA
			$V_{DD} = 15 V$, All drivers OFF, All inputs = 0 V	—	200	μA

Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.

ELECTRICAL CHARACTERISTICS at $T_A = -55°C$, $V_{DD} = 5\,V$, $V_{SS} = 0\,V$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UCS-4821H	$V_{OUT} = 50\,V$	—	50	μA
		UCS-4822H	$V_{OUT} = 80\,V$	—	50	μV
		UCS-4823H	$V_{OUT} = 100\,V$	—	50	μV
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_{OUT} = 100\,mA$	—	1.3	V
			$I_{OUT} = 200\,mA$	—	1.5	V
			$I_{OUT} = 350\,mA$, $V_{DD} = 7.0\,V$	—	1.8	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	$V_{DD} = 15\,V$	14	—	V
			$V_{DD} = 10\,V$	9.0	—	V
			$V_{DD} = 5.0\,V$ (See note)	3.6	—	V
Input Resistance	R_{IN}	ALL	$V_{DD} = 15\,V$	35	—	kΩ
			$V_{DD} = 10\,V$	35	—	kΩ
			$V_{DD} = 5.0\,V$	35	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	One driver ON, $V_{DD} = 15\,V$	—	2.5	mA
			One driver ON, $V_{DD} = 10\,V$	—	1.9	mA
			One driver ON, $V_{DD} = 5.0\,V$	—	1.2	mA
	$I_{DD(OFF)}$	ALL	$V_{DD} = 5.0\,V$, All drivers OFF, All inputs = 0 V	—	100	μA
			$V_{DD} = 5.0\,V$, All drivers OFF, All inputs = 0 V	—	200	μA

ELECTRICAL CHARACTERISTICS at $T_A = +125°C$, $V_{DD} = 5\,V$, $V_{SS} = 0\,V$ (unless otherwise specified)

Characteristic	Symbol	Applicable Devices	Test Conditions	Limits Min.	Limits Max.	Units
Output Leakage Current	I_{CEX}	UCS-4821H	$V_{OUT} = 50\,V$	—	500	μA
		UCS-4822H	$V_{OUT} = 80\,V$	—	500	μV
		UCS-4823H	$V_{OUT} = 100\,V$	—	500	μV
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	ALL	$I_{OUT} = 100\,mA*$	—	1.3	V
			$I_{OUT} = 200\,mA*$	—	1.5	V
			$I_{OUT} = 350\,mA*$, $V_{DD} = 7.0\,V$	—	1.8	V
Input Voltage	$V_{IN(0)}$	ALL		—	0.8	V
	$V_{IN(1)}$	ALL	$V_{DD} = 15\,V$	13.5	—	V
			$V_{DD} = 10\,V$	8.5	—	V
			$V_{DD} = 5.0\,V$ (See note)	3.5	—	V
Input Resistance	R_{IN}	ALL	$V_{DD} = 15\,V$	50	—	kΩ
			$V_{DD} = 10\,V$	50	—	kΩ
			$V_{DD} = 5.0\,V$	50	—	kΩ
Supply Current	$I_{DD(ON)}$	ALL	One driver ON, $V_{DD} = 15\,V$	—	2.0	mA
			One driver ON, $V_{DD} = 10\,V$	—	1.7	mA
			One driver ON, $V_{DD} = 5.0\,V$	—	1.0	mA
	$I_{DD(OFF)}$	ALL	$V_{DD} = 5.0\,V$, All drivers OFF, All inputs = 0 V	—	100	μA
			$V_{DD} = 5.0\,V$, All drivers OFF, All inputs = 0 V	—	200	μA

Note: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to ensure an input-logic high.
*Pulsed test.

CLOCK — A — C

DATA IN — D — E — B

STROBE

ENABLE — F

OUT$_N$

Dwg. No. A-10,990A

TIMING CONDITIONS

$T_A = +25°C$; Logic Levels are V_{DD} and V_{SS}

	$V_{DD} = 5.0$ V	$V_{DD} = 15$ V
A. Minimum Data Active Time Before Clock Pulse (Data Set-Up Time)	250 ns	150 ns
B. Minimum Data Pulse Width	500 ns	300 ns
C. Minimum Clock Pulse Width	1.0 μs	250 ns
D. Minimum Time Between Clock Activation and Strobe	1.0 μs	400 ns
E. Minimum Strobe Pulse Width	500 ns	300 ns
F. Typical Time Between Strobe Activation and Output Transition	1.0 μs	1.0 μs

5

SERIAL DATA present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to its respective latch when the STROBE is high (serial-to-parallel conversion). The latches will con-

tinue to accept new data as long as the STROBE is held high. Applications where the latches are by-passed (STROBE tied high) will require that the ENABLE input be high during serial entry.

When the ENABLE input is high, all of the output buffers are disabled (OFF) without affecting the information stored in the latches or shift register. With the ENABLE input low, the outputs are controlled by the state of the latches.

SERIES UCS-4820H TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents $I_1\,I_2\,I_3 \ldots \ldots \ldots I_8$	Serial Data Output	Strobe Input	Latch Contents $I_1\,I_2\,I_3 \ldots \ldots \ldots I_8$	Output Enable	Output Contents $I_1\,I_2\,I_3 \ldots \ldots \ldots I_8$
L	⌐	H R$_1$ R$_2$ .... R$_7$	R$_7$				
H	⌐	L R$_1$ R$_2$ .... R$_7$	R$_7$				
X	⌐	R$_1$ R$_2$ R$_3$ .... R$_8$	R$_8$				
		X X X X	X	L	R$_1$ R$_2$ R$_3$ .... R$_8$		
		P$_1$ P$_2$ P$_3$ .... P$_8$	P$_8$	H	P$_1$ P$_2$ P$_3$ .... P$_8$	L	P$_1$ P$_2$ P$_3$ .... P$_8$
					X X X X	H	H H H .... H

L = Low Logic Level
H = High Logic Level
X = Irrelevant
P = Present State
R = Previous State

SERIES UDS-5700H
QUAD 2-INPUT PERIPHERAL AND POWER DRIVERS
— Hermetically Sealed

FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Sustaining Voltage of 80 V
- Hermetically Sealed Package to MIL-M-38510
- High-Reliability Screening to MIL-STD-883, Class B

Description

These 16-Lead quad 2-input peripheral and power drivers are bi-polar monolithic integrated circuits incorporating AND, NAND, OR, and NOR logic gates, high-current switching transistors, and transient suppression diodes on the same chip. The four output transistors are capable of simultaneously sinking 150 mA continuously at an ambient temperature of +70°C. In the OFF state, these drivers will sustain at least 80 V.

Applications

The Series UDS-5700H quad drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters.

The integral transient suppression diodes allow their use with inductive loads such as relays, solenoids, or stepping motors without the need for discrete diodes. For non-inductive loads, the diode common bus can be used as a convenient lamp test.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . .7.0 V
Input Voltage, V_{in} . . . . 30 V
Output Off-State Voltage, V_{off} . . . . 80 V
Output On-State Sink Current, I_{on} . . . . 600 mA
Suppression Diode Off-State Voltage, V_{off} . . . . 80 V
Suppression Diode On-State Current, I_{on} . . . . 600 mA
Power Dissipation, P_D . . . . 1.0 W
Package Power Dissipation, P_D . . . . See Graph
Ambient Temperature Range (operating), T_A . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE

DWG. NO. A-10.198A

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into any output (ON state)	—	—	300	mA

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions				Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	
"1" Input Voltage	$V_{in(1)}$	MIN					2.0			V	
"0" Input Voltage	$V_{in(0)}$	MIN							0.7	V	
"0" Input Current	$I_{in(0)}$	MAX	0.4 V	30 V				−50	−100	μA	2
"1" Input Current	$I_{in(1)}$	MAX	30 V	0 V					10	μA	2
Input Clamp Voltage	V_I	MIN	−12 mA						−1.5	V	

SWITCHING CHARACTERISTICS at V_{CC} = 5.0V, T_A = 25°C

Characteristic	Symbol	Test Conditions	Limits			Units	Notes
			Min.	Typ.	Max.		
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		200	500	ns	3
Turn-off Delay Time	t_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
4. Capacitance values specified include probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

5

Type UDS-5703H Quad OR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	V_CC	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
				Test Conditions				Limits			
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	150 mA		0.4	0.5	V	
			MIN	0.8 V	0.8 V	300 mA		0.6	0.8	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			16	25	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			72	100	mA	1, 2

DWG. NO. A-9123A

DWG. No. A-7628C

DWG. NO. A-9869

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

Type UDS-5706H Quad AND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	150 mA	0.4	0.5		V	
			MIN	0.8 V	V_{CC}	300 mA	0.6	0.8		V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			16	24	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			70	98	mA	1, 2

(Header spanning: "Test Conditions" spans Temp., V_{CC}, Driven Input, Other Input, Output; "Limits" spans Min., Typ., Max.)

DWG. NO. A-7878A

DWG. No. A-7628C

DWG. NO. A-9866

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

Type UDS-5707H Quad NAND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits				Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	150 mA		0.4	0.5	V	
			MIN	2.0 V	2.0 V	300 mA		0.6	0.8	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			80	106	mA	1, 2

DWG. NO. A-7899A

DWG. NO. A-7900A

DWG. NO. A-9667

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at V_R = $V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

Type UDS-5733H Quad NOR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	150 mA	0.4	0.5		V	
			MIN	2.0 V	0 V	300 mA	0.6	0.8		V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			24	30	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			80	100	mA	1, 2

INPUT V_{CC}=5V   OPEN   OUTPUT V_S

PULSE GENERATOR

50Ω

R_L

15pF (Note 5)

LOAD CIRCUIT

DWG. NO. A-9135A

DWG. NO. A-7900A

DWG. NO. A-9868

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at V_R = $V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

SERIES UDS-5710H
DUAL PERIPHERAL AND POWER DRIVERS
— Hermetically Sealed

FEATURES

- Four Logic Types
- DTL/TTL/PMOS/CMOS Compatible Inputs
- Low Input Current
- Sustaining Voltage of 80 V
- Transient-Protected Outputs
- High-Reliability Screening to MIL-STD-883, Class B

Description

These dual peripheral and power drivers are bipolar monolithic integrated circuits incorporating AND, NAND, OR, or NOR logic gates, high-current switching transistors, and transient suppression diodes on the same chip. The two output transistors are capable of simultaneously sinking 200 mA continuously at ambient temperatures of up to +85°C. In the OFF state, these drivers will sustain at least 80 V. Units are supplied in 8-pin hermetically sealed mini-DIP packages.

Applications

The Series UDS-5710H dual drivers are ideally suited for interface between low-level or high-level logic and high-current/high-voltage loads. Typical applications include driving peripheral loads such as incandescent lamps, light-emitting diodes, memories, and heaters with a load current of up to a 500 mA peak value.

The integral transient suppression diodes allow the use of these drivers with inductive loads such as relays, solenoids, or stepping motors without the need for discrete diodes. When not required for transient suppression, the diode common bus can be used to perform the "lamp test" function.

DWG. NO. A-9791

Type UDS-5711H
Dual AND Driver
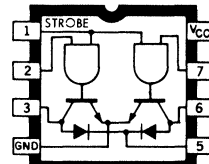
DWG. NO. A-9790

Type UDS-5712H
Dual NAND Driver
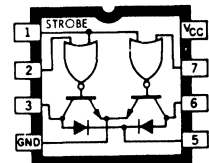
DWG. NO. A-9789

Type UDS-5713H
Dual OR Driver
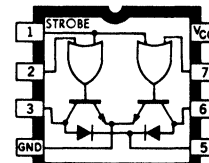
DWG. NO. A-9788

Type UDS-5714H
Dual NOR Driver
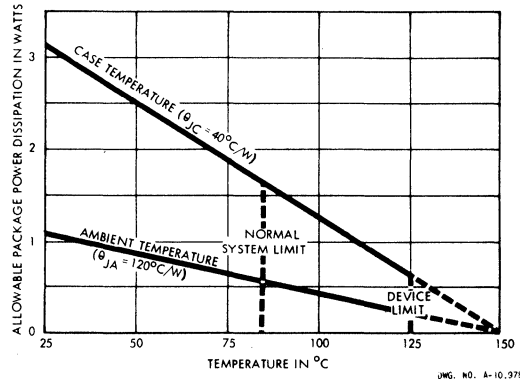
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 7.0 V
Input Voltage, V_{in} .... 30 V
Output Off-State Voltage, V_{off} .... 80 V
Output On-State Sink Current, I_{on} .... 500 mA
Suppression Diode Off-State Voltage, V_{off} .... 80 V
Suppression Diode On-State Current, I_{on} .... 500 mA
Power Dissipation, P_D (one output) .... 1.0 W
$\quad\quad\quad\quad\quad\quad\quad$ (total package) .... See Graph
Ambient Temperature Range (operating), T_A .... −55°C to +125°C
Storage Temperature Range, T_S .... −65°C to +150°C

POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE

RECOMMENDED OPERATING CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Temperature Range	−55	+25	+125	°C
Current into any output (ON state)	—	—	300	mA

5

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
				Test Conditions			Limits				
"1" Input Voltage	$V_{in(1)}$		MIN				2.0			V	
"0" Input Voltage	$V_{in(0)}$		MIN						0.8	V	
"0" Input Current at all Inputs except Strobe	$I_{in(0)}$		MAX	0.4 V	30 V			−50	−100	μA	2
"0" Input Current at Strobe	$I_{in(0)}$		MAX	0.4 V	30 V			−100	−200	μA	
"1" Input Current at all Inputs except Strobe	$I_{in(1)}$		MAX	30 V	0 V				10	μA	2
"1" Input Current at Strobe	$I_{in(1)}$		MAX	30 V	0 V				20	μA	2
Input Clamp Voltage	V_I		MIN	−12 mA					−1.5	V	

SWITCHING CHARACTERISTICS at V_{CC} = 5.0V, T_A = 25°C

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
			Limits				
Turn-on Delay Time	t_{pd0}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		200	500	ns	3
Turn-off Delay Time	T_{pd1}	V_S = 70 V, R_L = 465 Ω (10 Watts) C_L = 15 pF		300	750	ns	3

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Each input tested separately.
3. Voltage values shown in the test circuit waveforms are with respect to network ground terminal.
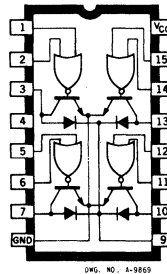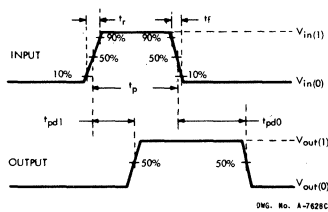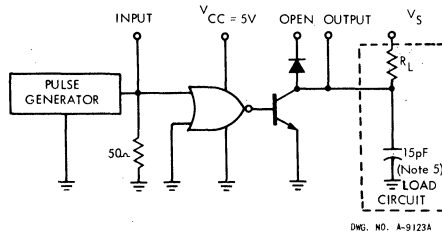4. Capacitance values specified include probe and test fixture capacitance.

INPUT PULSE CHARACTERISTICS

$V_{in(0)}$ = 0V	t_f = 7ns	t_p = 1μs
$V_{in(1)}$ = 3.5V	t_r = 14ns	PRR = 500kHz

UDS-5711H Dual AND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Output Reverse Current	I_{off}		MIN	2.0 V	2.0 V	80 V			100	μA	
			OPEN	2.0 V	2.0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	V_{CC}	150 mA		0.4	0.5	V	
			MIN	0.8 V	V_{CC}	300 mA		0.6	0.8	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	12	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			35	49	mA	1, 2

DWG. NO. A-7878A

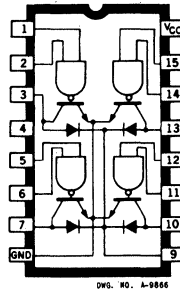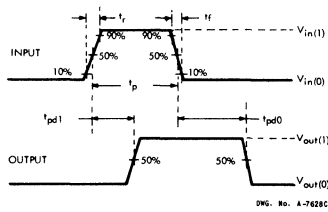DWG. No. A-7628C

DWG. NO. A-9791

NOTES:
1. Typical values are at $V_{CC} = 5.0$ V, $T_A = 25°C$.
2. Per package.
3. Diode leakage current measured at $V_R = V_{off(min)}$.
4. Diode forward voltage drop measured at $I_f = 300$ mA.
5. Capacitance values specified include probe and test fixture capacitance.

UDS-5712H Dual NAND Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Output Reverse Current	I_{off}		MIN	0.8 V	V_{CC}	80 V			100	μA	
			OPEN	0.8 V	V_{CC}	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	2.0 V	150 mA		0.4	0.5	V	
			MIN	2.0 V	2.0 V	300 mA		0.6	0.8	V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	53	mA	1, 2

DWG. NO. A-7809A
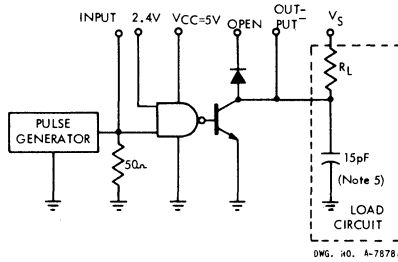

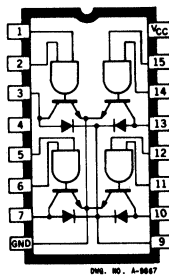DWG. NO. A-7900A

DWG. NO. A-9790

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at V_R = $V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

UDS-5713H Dual OR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.	Units	Notes
				Test Conditions				Limits			
"1" Output Reverse Current	I_{off}		MIN	2.0 V	0 V	80 V			100	μA	
			OPEN	2.0 V	0 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	0.8 V	0.8 V	150 mA	0.4		0.5	V	
			MIN	0.8 V	0.8 V	300 mA	0.6		0.8	V	
Diode Leakage Current	I_{LK}	NOM	NOM	0 V	0 V	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	V_{CC}	V_{CC}			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	5.0 V	5.0 V			8.0	13	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	0 V	0 V			36	50	mA	1, 2

DWG. NO. A-9123A

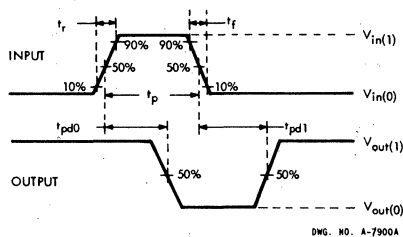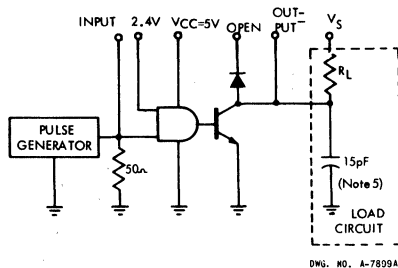
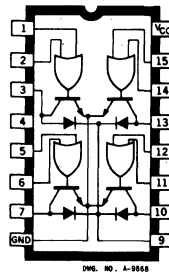DWG. No. A-7628C

DWG. NO. A-9789

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at V_R = $V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

UDS-5714H Dual NOR Driver

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Test Conditions					Limits			Units	Notes
		Temp.	V_{CC}	Driven Input	Other Input	Output	Min.	Typ.	Max.		
"1" Output Reverse Current	I_{off}		MIN	0.8 V	0.8 V	80 V			100	μA	
			OPEN	0.8 V	0.8 V	80 V			100	μA	
"0" Output Voltage	V_{on}		MIN	2.0 V	0 V	150 mA	0.4	0.5		V	
			MIN	2.0 V	0 V	300 mA	0.6	0.8		V	
Diode Leakage Current	I_{LK}	NOM	NOM	V_{CC}	V_{CC}	OPEN			200	μA	3
Diode Forward Voltage Drop	V_D	NOM	NOM	0 V	0 V			1.5	1.75	V	4
"1" Level Supply Current	$I_{CC(1)}$	NOM	MAX	0 V	0 V			12	15	mA	1, 2
"0" Level Supply Current	$I_{CC(0)}$	NOM	MAX	5.0 V	5.0 V			40	50	mA	1, 2

DWG. NO. A-9135A

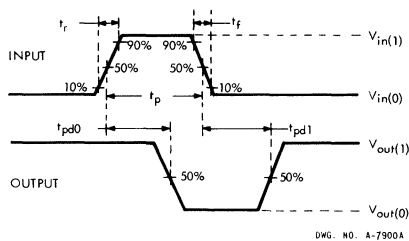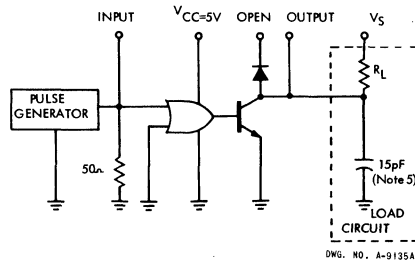DWG. NO. A-7900A

DWG. NO. A-9788

NOTES:
1. Typical values are at V_{CC} = 5.0 V, T_A = 25°C.
2. Per package.
3. Diode leakage current measured at V_R = $V_{off(min)}$.
4. Diode forward voltage drop measured at I_f = 300 mA.
5. Capacitance values specified include probe and test fixture capacitance.

UDS-5791H
QUAD PIN DIODE POWER DRIVER

FEATURES

- Low Input Current
- TTL, DTL, MOS Compatible
- Wide Operating Range
- High Output Breakdown Voltage

CONSISTING of four high-voltage NPN output stages and associated logic and level shifting, the Type UDS-5791H monolithic integrated circuit offers an easy solution to many problems associated with driving PIN diodes.

The UDS-5791H quad power driver is designed to replace discrete or hybrid PIN diode drivers. It provides significant reductions in cost and space with improved reliability. The driver uses a common-emitter input stage for inverting operation. It is capable of sustaining OFF voltages of 120 V and will switch currents to 500 mA.

The input buffer circuitry has been designed to utilize external discrete resistors. The one resistor per driver effectively reduces total package power dissipation and junction temperature while allowing user selection of output base drive current, power supply voltages, and output current.
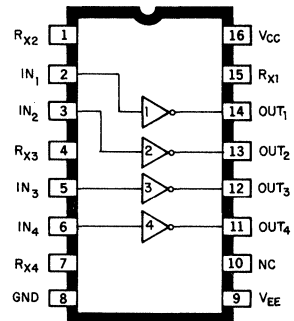
DWG. NO. A-10,478

UDS-5791H

The device is rated for operation over an extended temperature range of $-55°C$ to $+125°C$. It is customarily supplied in 16-pin hermetic dual in-line package. The unit is subjected to the 100% production screen tests specified in MIL-STD-883, Method 5004, Class B paragraphs 3.1.1 through 3.1.6. On special order, 160 hours of burn-in to Method 1015, Condition A, can also be performed.

ABSOLUTE MAXIMUM RATINGS
over free-air operating temperature range

Supply Voltage, V_{CC} . . . . +6.0 V
Supply Voltage, V_{EE} . . . . −6.0 V
Input Voltage, V_{IN} . . . . V_{CC}
Output OFF-State Voltage, V_{OFF} (ref. V_{EE}) . . . . +120 V
Output ON-State Current, I_{ON} . . . . 500 mA
Package Power Dissipation, P_D . . . . See Graph
Operating Ambient Temperature Range, T_A . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

PARTIAL SCHEMATIC

ONE OF FOUR DRIVERS
UDS-5791H

RECOMMENDED OPERATION CONDITIONS

	Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}	4.5	5.0	5.5	V
Supply Voltage, V_{EE}	−1.5	−3.0	−5.5	V
Output ON-State Current, I_{ON}			300	mA
Operating Ambient Temperature Range, T_A	−55	+85	+125	°C

POWER DISSIPATION AS A FUNCTION OF TEMPERATURE

ALLOWABLE PACKAGE POWER DISSIPATION IN WATTS

CASE TEMPERATURE ($\theta JC = 20°C/W$)

AMBIENT TEMPERATURE ($\theta JA = 90°C/W$)

NORMAL SYSTEM LIMIT

DEVICE LIMIT

TEMPERATURE IN °C

DWG. NO. A-10,198A

ELECTRICAL CHARACTERISTICS over operating temperature range (unless otherwise noted)

Characteristic	Symbol	Temp. (°C)	V_{CC} (+V)	V_{EE} (−V)	V_{IN} (+V)	V_{OFF} or I_{ON} (+V)	(mA)	R_X (Ω)	Limits Min.	Max.	Units
"1" Input Voltage	$V_{IN(1)}$		4.5						2.0	4.0	V
"0" Input Voltage	$V_{IN(0)}$		4.5						—	0.8	V
"1" Input Current	$I_{IN(1)}$		5.5	3.0	5.0				—	50	μA
"0" Input Current	$I_{IN(0)}$		5.5	3.0	0.4				—	1.0	mA
OFF-State Reverse Current	I_{OFF}	+25	4.5	3.0	0.4	115			—	50	μA
		+125	4.5	3.0	0.4	115			—	100	μA
ON-State Output Voltage (ref. V_{EE}) (See Note)	V_{ON}	−55	4.5	1.5	2.4		150	720	—	400	mV
							300	360	—	600	mV
		+85	4.5	1.5	2.4		150	720	—	400	mV
							300	360	—	700	mV
		+125	4.5	1.5	2.4		150	720	—	500	mV
							300	360	—	850	mV
Predriver Collector Voltage (ref. V_{EE}) (See Note)	V_X		4.5	1.5	2.4		150	720	—	1.3	V
							300	360	—	1.5	V
Output Short-Circuit Current (See Note)	I_{OS}		4.5	3.0	0.4	−2.3		510	20	50	mA
OFF-State Supply Current	I_{CC}		5.5	5.5	0.4				—	4.1	mA
ON-State Supply Current	I_{CC}		5.5	5.5	2.4				—	3.4	mA
Turn-On Delay	t_{on}	—	5.0	3.0	—	—	—	510	—	500	ns
Storage Delay	t_s	—	5.0	3.0	—	—	—	510	—	5.0	μs
Fall Time	t_f	—	5.0	3.0	—	—	—	510	—	100	ns

NOTE: Each output tested separately.

SWITCHING TEST CIRCUIT
AND WAVEFORMS
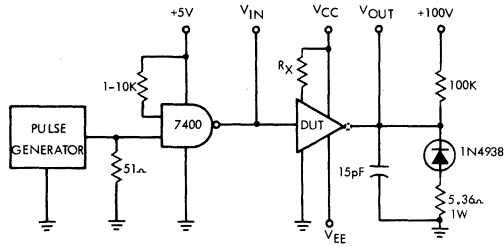
DWG. NO. A-10.654
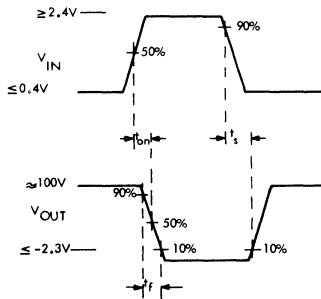
DWG. NO. A-10.655

GENERAL DESIGN NOTES

$$I_{RX} = \frac{I_{ON}}{B}$$

$$R_X = \frac{B(V_{CC} - V_{EE} - V_X)}{I_{ON}}$$

where

   $B = 30$, the minimum output current gain over the operating temperature range

   $V_X = 1.5$, the maximum predriver voltage

It is recommended that a minimum overdrive of 25% to be used ($1.25\ I_{RX}$ or 0.8_{RX}).

QUALITY ASSURANCE FLOW CHART

```
CHEMICALS, GASES, HARDWARE        QUALITY ASSURANCE
       WAFERS                    PROCUREMENT REVIEW        QA IN-PROCESS        QA IN-PROCESS
    RAW MATERIALS                  VENDOR CONTROL             AUDIT                AUDIT
       MASKS                       INCOMING INSP.                              S.E.M. INSPECTION

 NEW PRODUCT DESIGNS           RELIABILITY ENGINEERING
 AND CURRENT DESIGNS,          DESIGN  INTRODUCTION           WAFER                                 QA
 NEW-CURRENT PROCESSES,        (SEM) EVALUATION,           FABRICATION          METALLIZATION     TOLLGATE
 NEW MATERIALS                 QUALIFICATION                                                       INSP.

 DOCUMENTATION OF:             PRODUCT ASSURANCE
 CHEMICALS, HARDWARE           DOCUMENTATION CENTER
 GASES, MASKS                  PRODUCT-PROCESS
 PROCESSES, DESIGNS, ETC.      AND PROCUREMENT SPECS.
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          HYREL          —  HERMETIC PKG.  —        STANDARD

     STABILIZATION BAKE                         STABILIZATION BAKE

       TEMP. CYCLE                                TEMP. CYCLE
        CENTRIFUGE              QA AUDIT            CENTRIFUGE
   GROSS LEAK, FINE LEAK                      GROSS LEAK, FINE LEAK

   100% ELECTRICAL TEST

       BRANDING                 QA AUDIT

    QAR ACCEPTANCE
      INSPECTION
                                                QUALIFICATION
      MIL-STD-883                              OF CONFORMANCE
      METHOD 5004                                MIL-STD-883
    OR CUSTOMER REQ.                           METHOD 5005 OR
                                               CUSTOMERS REQ.

                                                    PACK

                                                     QA
                                                VISUAL/MECH
                                                 TOLLGATE

                   SHIP                                        STOCK
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┌─────────────┐              ┌─────────────┐
│ 100% VISUAL │              │ QA IN PROCESS│
│ INSPECTION  │              │    AUDIT    │
└─────────────┘              └─────────────┘
       │                            │
┌──────┐  ┌─────────┐   ╱QA╲   ┌─────────┐   ┌──────────┐   ╱QA╲
│PROBE │  │ SCRIBE  │  │DIE   │ │DIE ATTACH│  │100% VISUAL│ │PRE-CAP│
│      │  │  SORT   │  │VISUAL│ │WIRE BOND │  │  PRE-CAP  │ │TOLLGATE│
└──────┘  └─────────┘  │GATE  │ └─────────┘   │   INSP.   │  ╲    ╱
                        ╲   ╱                  └──────────┘
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PROBE — SCRIBE SORT — 100% VISUAL INSPECTION — QA DIE VISUAL GATE — DIE ATTACH WIRE BOND — QA IN PROCESS AUDIT — 100% VISUAL PRE-CAP INSP. — QA PRE-CAP TOLLGATE

SEAL MOLD

QA AUDIT

PLASTIC PKG. —

STABILIZATION BAKE

100% TEMP. CYCLING

100% OPEN/SHORT ELECTRICAL

QA AUDIT

RELIABILITY AUDIT

100% ELECTRICAL TEST

QA AUDIT — BRANDING ----- HIGH-TEMP TEST

QAR ACCEPTANCE INSPECTION

DWG. NO. B-1474

5—85

THE SPRAGUE ELECTRIC 'DOUBLE-DEUCE' BURN-IN PROGRAM FOR INTEGRATED CIRCUITS

THE EXPENSE OF DEVICE FAILURE is more than the time and money spent locating and replacing a defective integrated circuit. The total cost can include the price of assembly rework, system downtime, service calls, warranty claims and lost customer goodwill.

Costs of $25 for each in-house failure and $250 for each field failure are not uncommon. At a relatively low cost, Sprague Electric Company's "Double-Deuce" screening program removes marginal devices before shipment. Improved customer satisfaction with performance and reliability is an immeasurable but certain bonus of the program.

"Double-Deuce" screening is done during the last stage of production. Because Sprague does the screening, only qualified devices are received by the user.

QUALITY AND RELIABILITY

Quality and reliability are terms that are often used interchangeably. Quality implies reliability, but a product's merit should always be defined by both.

Quality is the extent to which a device conforms to specifications when it is shipped to the user. Quality is verified by testing. Inspections at every step of production of Sprague integrated circuits ensure the devices meet demanding standards for workmanship and materials.

Inspections of integrated circuits under the "Double-Deuce" program have been made even more stringent to secure a higher level of quality.

Reliability is the measure of an integrated circuit's ability to meet specifications over time. Reliability is a product of design and process control. Accelerated-life tests provide the manufacturer and user with an indication of the reliability of a device. Normally, a small number of integrated circuits exhibit signs of early failure or infant mortality. This statistic, taken from the steepest part of the IC

lifetime probability curve, is often used to project time-to-failure for integrated circuits. Because the "Double-Deuce" program eliminates early failures, Sprague integrated circuits delivered after the screening process have a higher degree of reliability.

**PROBABILITY OF FAILURE
AS A FUNCTION OF TIME**
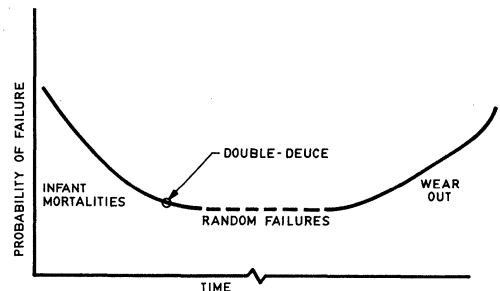
Dwg. No. A-11,417

OUTLINE OF THE 'DOUBLE-DEUCE' PROCESS

The "Double-Deuce" burn-in program uses high stress levels to accelerate the failure mechanisms associated with infant mortality. These normally occur within the first few hours of user application. Although typically less than 1 per cent of a lot will be rejected, user confidence in lot integrity is greatly improved. The screening program is designed to eliminate the following failure modes:

Stress	Failure Mode
High-Temp. Bake	Contamination
Temp. Cycling	Package-Related
Burn-In	Process-Related
High-Temp. Testing	Electrical Degradation

The majority of early integrated circuit failures (infant mortality or ionic contamination) can be attributed to manufacturing defects, package or assembly defects, or final test escapes. The "Double-Deuce" program is designed to eliminate weaker parts, reduce or eliminate user shipment inspection, assembly rework, system checkout, and warranty returns.

WAFER FABRICATION

WAFER FABRICATION → MILITARY PRODUCT PROCESSING

COMMERCIAL PRODUCT

100% PROBE

PACKAGE ASSEMBLY

DOUBLE-DEUCE PROGRAM

HIGH-TEMPERATURE BAKE | STANDARD PRODUCT PROCESSING

25° C D-C & FUNCTIONAL TESTS | 25° C D-C & FUNCTIONAL TESTS

BRAND ② ② | BRAND

TEMPERATURE CYCLE

BURN-IN

70° C D-C & FUNCTIONAL TESTS

TOLLGATE ACCEPTANCE INSP. | TOLLGATE ACCEPTANCE INSP.

SHIP | SHIP

DWG.NO. A-11,418A

TEST PROCEDURES

The "Double-Deuce" burn-in program includes five test procedures:

1. High-Temperature Bake

This is a process designed to stabilize electrical drift and to accelerate chemical degradation such as surface contamination. It is a four-hour bake at +175°C without electrical stress (similar to MIL-STD-883, Method 1008).

2. Temperature Cycling

This is a screening process designed to mechanically stress the integrated circuit by alternately heating and cooling it. Potential failures are seal or bond failure, cracked packages or chips.

The process has 10 cycles with 10 minutes of dwell at −65°C and 10 minutes of dwell at +150°C (air to air), with a maximum transfer time of five minutes (MIL-STD-883, Method 1010, Condition C). At Sprague's option, this process may be changed to thermal shock (liquid to liquid) for 10 cycles, five minutes at 0°C and five minutes at +100°C with a transfer time of 10 seconds (MIL-STD-883, Method 1011, Condition A).

TEST PROCEDURES

3. Burn-In

The burn-in, or accelerated-life test, is performed to screen out marginal devices, those with inherent defects, or defects resulting from manufacturing deviations that can cause time-dependent or stress-dependent failures. Without this conditioning, marginal circuits that initially meet all specifications could exhibit early lifetime failures under normal operating conditions. The test is conducted for 96 hours at a junction temperature of $+150\,°C$ under electrical stress conditions (similar to MIL-STD-883, Method 1015) such as:

Type of Device	Electrical Stress
Bipolar Interface	Steady-State Reverse Bias
Linear Devices	Steady-State Forward Bias
I²L and MOS Logic	Clocked

The burn-in conditions (96 hours at $T_J = +150\,°C$) are equivalent to 525 hours at $T_J = +125\,°C$ for ionic contamination ($E_A = 1.0$ eV) or for 192 hours at $T_J = +125\,°C$ for infant mortality defects ($E_A = 0.4$ eV).

4. High-Temperature Test

Every device is subjected to complete electrical tests at $+70\,°C$ for function and d-c parameters (similar to MIL-STD-883, Methods 3001 through 3014 and 4001 through 4007, as applicable). Relaxed $+25\,°C$ limits or published high-temperature limits, are used to remove devices with circuit anomalies such as beta mismatch, high leakage current, and intermittent bonds, which may only affect the circuit at higher temperatures.

5. Outgoing Quality Control Inspection

All "Double-Deuce" product is inspected to an outgoing sampling plan which guarantees that the product will meet an acceptable quality level of 0.25%.

HOW TO ORDER

All standard Sprague integrated circuits are branded with the Sprague registered trademark, ②.

Integrated circuits screened to the added requirements of the "Double-Deuce" program are marked:

② ②

The double "circle-deuce" identifies a part subjected to the screening program for extra reliability.

Devices processed in the "Double-Deuce" burn-in program are specified by adding the suffix "BU" to the end of the part number. For example, to order ULN-2023A with this processing, specify ULN-2023ABU; to order UDN-6116R-2, specify UDN-6116R-2BU.

INTERFACE DRIVERS WITH MIL-STD-883
HIGH-RELIABILITY SCREENING

Interface drivers with high-reliability screening can be ordered by adding the suffix "MIL" to the part number, for example, ULS-2064H-MIL. If marking with the customers part number is necessary in place of the Sprague Electric part number, this must be stated on the purchase order with the marking desired.

Table I — 100% Production Screen Tests (All Hermetic Parts)
MIL-STD-883, Method 5004, Class B, Paragraphs 3.1.1 through 3.1.6

Screen	MIL-STD-883 Test Method	Conditions
Internal Visual	2010, Cond. B	—
Stabilization Bake	1008, Cond. C	150°C, 24 Hours
Thermal Shock	1011, Cond. A	0 to 100°C, 15 Cycles
Constant Acceleration	2001, Cond. E	30,000 G's, Y1 Plane
Fine Seal	1014, Cond. A	5×10^{-7} atm•cm³/s Maximum
Gross Seal	1014, Cond. C	—
Electrical	—	Per Specification
Marking	—	Sprague or customer part number, date code, lot identification, index point

Table II — 100% High-Reliability Screening ("MIL" Suffix Parts Only)
MIL-STD-883, Method 5004, Class B, Paragraphs 3.1.9 through 3.1.15 & 3.1.18

Screen	MIL-STD-883 Test Method	Conditions
Interim Electrical	5005, Gp A, Subgp. 1	25°C per Specification
Burn-In	1015, Cond. A	125°C, 160 Hours
Static Electrical	5005, Gp A, Subgp. 1	25°C per Specification
	5005, Gp A, Subgp. 2 & 3	−55°C & +125°C per Specification
Dynamic & Functional Electrical	5005, Gp A, Subgp. 4, 7 & 9	25°C per Specification
Fine Seal	1014, Cond. A	5×10^{-7} atm•cm³/s Maximum
Gross Seal	1014, Cond. C	—
External Visual	2009	—

Table III — High-Reliability Qualification and Quality Conformance Inspection
MIL-STD-883, Method 5004, Class B, Paragraph 3.1.17

Test	MIL-STD-883 Test Method	Description
Group A Subgp. 1-4, 7 & 9	5005, Table I	Each production lot
Group B	5005, Table II	Each production lot
Group C	5005, Table III	End points, Gp. A, Subgp. 1, every 90 days
Group D	5005, Table IV	End points, Gp. A, Subgp. 1, every 6 months

Some of this material has been taken from Military Specification MIL-M-38510E and Military Standard MIL-STD-883B, Methods 1008.2, 1011.4, 1014.5, 1015.4, 2001.2, 2009.4, 2010.7, 5004.6, and 5005.8.
The above conditions may not comply with MIL-M-38510F and MIL-STD-883C.

5

BiMOS POWER DRIVERS TO MIL-STD-883

CONTINUING in its leadership role in inter-face integrated circuits, Sprague Electric Company has added hermetic BiMOS power drivers to its long list of innovations.

These high-current and high-voltage drivers with MIL-STD-883 screening provide a new level of interface flexibility and versatility for military, aerospace, avionics, and other applications requiring high reliability. They are supplied in either glass/metal side-brazed hermetic packages (suffix letter 'H') or ceramic/glass cer-DIP hermetic packages (suffix letter 'R').

BiMOS monolithic devices combine CMOS logic and control functions with four, seven, eight, or ten bipolar output, power-interface buffers. Reliable, single-chip solutions are now available for a wide variety of peripheral power interface problems. No longer are two or three devices required to link low-level (TTL, CMOS, NMOS, PMOS) LSI or microprocessor functions with power loads such as relays, LEDs, solenoids, lamps, gas-discharge or vacuum-fluorescent displays, and motors.

In addition to providing space-saving single-chip solutions to many peripheral power inter-face problems, Sprague BiMOS devices with an extended temperature range also improve system reliability and lower both component count and system cost.

Detailed engineering bulletins for the hermetic, extended temperature BiMOS integrated circuits described here are available from Sprague district sales offices, or from Technical Literature Service, Sprague Electric Company, Marshall Street, North Adams, Mass. 01247.

8-BIT SERIAL-INPUT/PARALLEL-OUTPUT LATCHED DRIVERS

SERIES UCS-4820H BiMOS 8-Bit Serial-In/Parallel-Out Latched Drivers augment the original Type UCS-4401H and UCS-4801H devices. All of the devices in this series contain an octal shift register, octal latch, and octal high-current, open-collector Darlington outputs. They improve systems designs through a reduced package count and a reduction in I/O line requirements. By using the serial data output, the drivers can be cascaded for interface applications requiring more than eight drive lines.

The three devices in this series are functionally identical, but differ in the maximum allowable output voltage ratings. The bipolar outputs are suitable for a variety of peripheral loads, including incandescent lamps, LEDs, thermal or electrosensitive printers, and (with appropriate clamping techniques) relays, solenoids, and other high-power inductive loads.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage (UCS-4821H) . . . . 45 V
               (UCS-4822H) . . . . 75 V
               (UCS-4823H) . . . . 95 V
Logic Supply Voltage . . . . 12 V
Continuous Output Current . . . . 350 mA

ELECTROSENSITIVE PRINTER APPLICATION
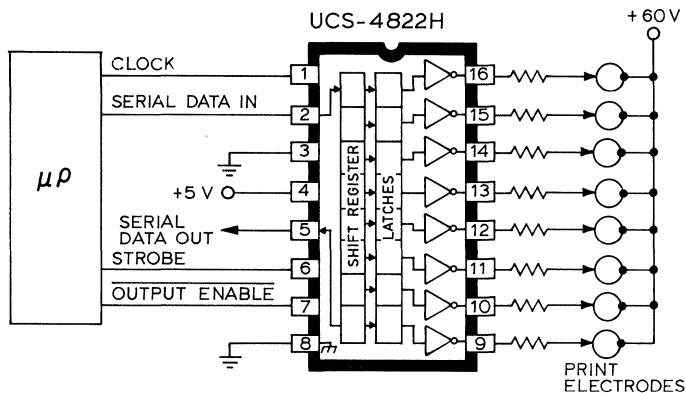
Dwg. No. A-11,742

10-BIT SERIAL-INPUT/PARALLEL-OUTPUT LATCHED SOURCE DRIVER

THE TYPE UCS-4810H BiMOS 10-Bit Serial-In/Parallel-Out Latched Source Driver is primarily designed as interface between logic circuitry and vacuum-fluorescent displays but may also be used with LED displays or thermal printers within its output limitations of 60 V and −40 mA per driver. A selected version, Type UCS-4810H-1, has a maximum operating-voltage rating of 80 V.

The CMOS shift register and latches will operate over a wide supply-voltage range and are compatible with standard MOS logic families. When used with TTL or low-speed TTL, pull-up resistors may be needed to ensure an input-logic high.

The 10 high-voltage outputs are used to switch the anodes (segments or dots) and/or grids (character or digit) of typical vacuum-fluorescent panels. The high-voltage version is often used with larger and more complex alphanumeric or graphics panels, or gas-discharge displays. With suitable signal-level shifting, it may also be used as an anode driver for planar gas-discharge applications.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage (UCS-4810H) .... 55 V
(UCS-4810H-1) .... 75 V
Logic Supply Voltage Range .... 5.0 V to 12 V
Continuous Output Current .... −25 mA

Dwg. No. C-1271
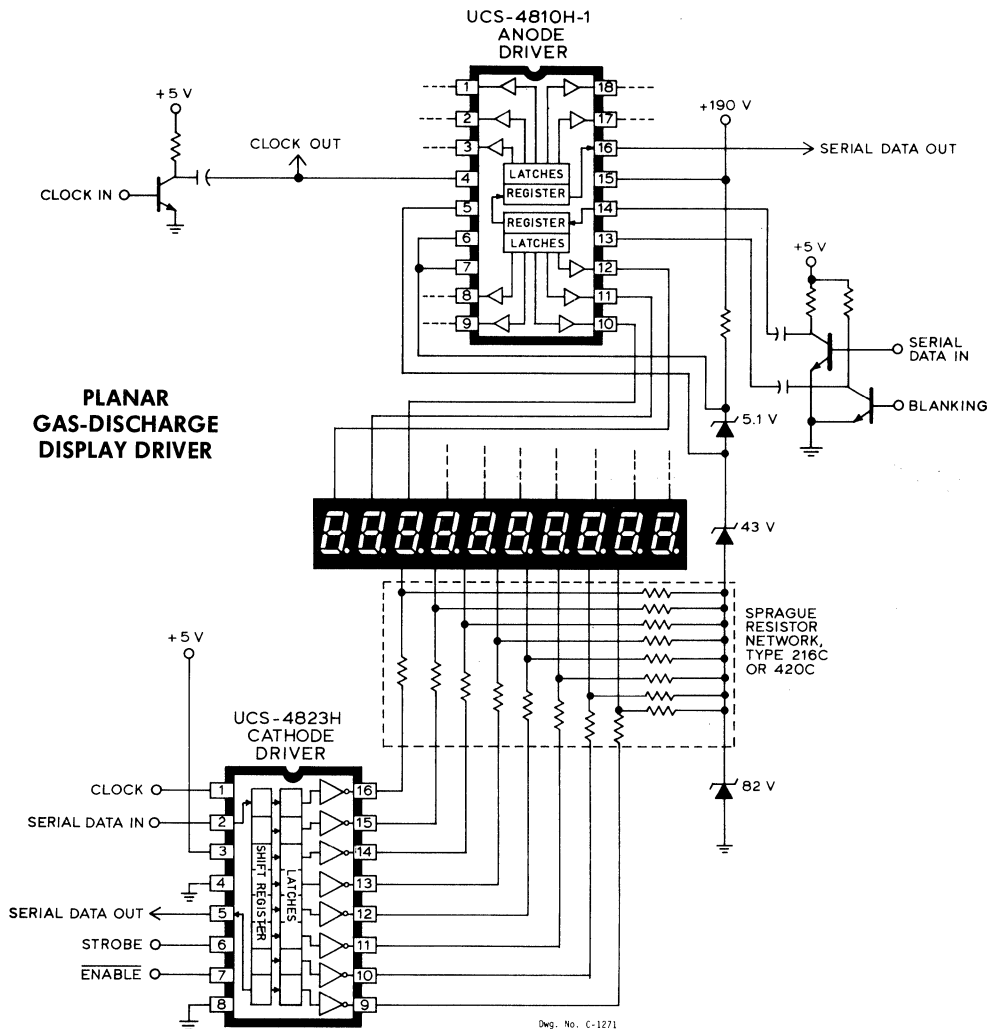
8-BIT LATCHED SOURCE DRIVER

THE TYPE UCS-4815H BiMOS 8-Bit Latched Source Driver is designed primarily for use with high-voltage vacuum-fluorescent displays. It contains an 8-bit type D latch and eight source outputs with pull-down resistors, a common strobe, blanking, and enable functions. The standard output voltage rating is 60 V, with a selected version (Type UCS-4815H-1) available for operation to 80 V.

The eight high-voltage outputs are generally used to drive the segments, dots (matrix panel), bars, or digits of vacuum-fluorescent displays. The high-voltage version is often used with larger and more complex gas-discharge alphanumeric or graphics panels.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage (UCS-4815H) .... 55 V
            (UCS-4815H-1) .... 75 V
Logic Supply Voltage Range .... 5.0 V to 12 V
Continuous Output Current .... −25 mA
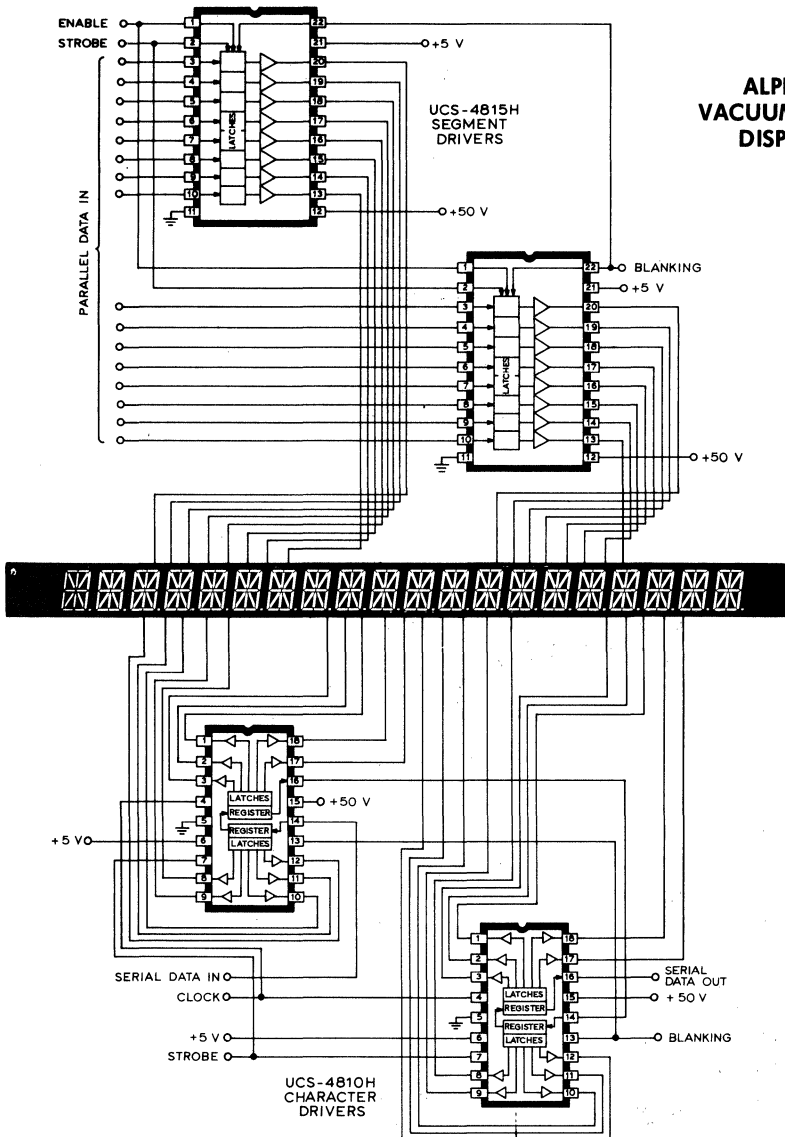
**ALPHANUMERIC
VACUUM-FLUORESCENT
DISPLAY DRIVERS**

Dwg. No. C-1272

4- AND 8-BIT LATCHED DRIVERS

TYPES UCS-4401H and UCS-4801H are the original BiMOS integrated circuits. They are used successfully in many applications. These high-voltage, high-current latched drivers have four or eight MOS data latches, a bipolar driver for each latch, and MOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions. Type UCS-4401H contains four latched drivers while Type UCS-4801H contains eight latched drivers.

Each of the open-collector Darlington outputs can sink up to 500 mA and will sustain at least 50 V in the OFF state. Internal diodes suppress transients and allow these devices to be used with inductive loads. Package power limitations normally disallow simultaneous and continuous operation of all outputs at the rated maximum current, and usually dictate either a reduction in output current or a suitable combination of duty cycle and number of active outputs.

Type UCS-4401H is supplied in a standard 14-lead side-brazed hermetic package. Type UCS-4801H is furnished in a 22-lead side-brazed hermetic package with lead centers on 0.400-inch spacing.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage . . . . 45 V
Logic Supply Voltage . . . . 12 V
Continuous Output Current . . . . 350 mA

UNIPOLAR BIFILAR MOTOR DRIVE

UCS-4401H

Dwg. No. B-1491

INCANDESCENT LAMP DRIVER
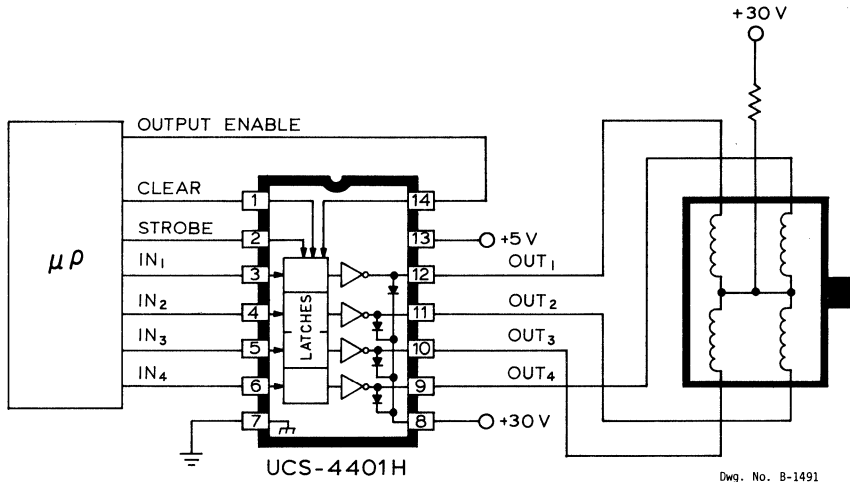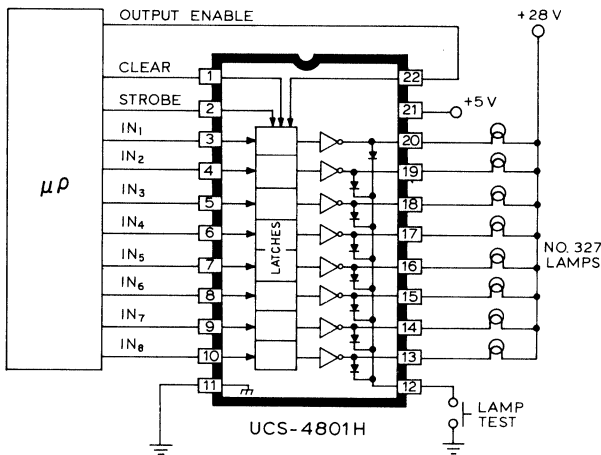
UCS-4801H

Dwg. No. A-11,743

8-BIT ADDRESSABLE LATCHED DRIVERS

TYPE UCS-4807H and UCS-4808H 8-Bit Addressable Latched Drivers are identical except for output current ratings. Type UCS-4807H is rated for a maximum of 200 mA per output while Type UCS-4808H is capable of sinking up to 600 mA per output. The outputs are NPN saturated switches; the drive currents are optimized for each version.

Both devices are comprised of a 3-bit to 8-line decoder, eight type D latches, eight open-collector NPN output drivers, and MOS control circuitry for CLEAR, input, output, and CHIP SELECT functions.

Both 8-bit addressable latched drivers are useful as demultiplexers. They are capable of driving a wide assortment of peripheral loads including lamps, relays, solenoids, LEDs, stepper motors, or may be used as DMUX/predrivers for higher power loads requiring discrete power semiconductors.

A typical application for Type UCS-4808H, driving a common-cathode LED display, is shown. Many of today's multi-character LED displays can make use of the high-current capability of this device. With the DATA input held high, the proper address code may be furnished by a 3-bit counter.

RECOMMENDED MAX. OPERATING CONDITIONS

Output Voltage .... 45 V
Logic Supply Voltage Range .... 5.0 V to 12 V
Continuous Output Current (UCS-4807H) .... 150 mA
(UCS-4808H) .... 350 mA

MULTIPLEXED COMMON-CATHODE LED DISPLAY DRIVER
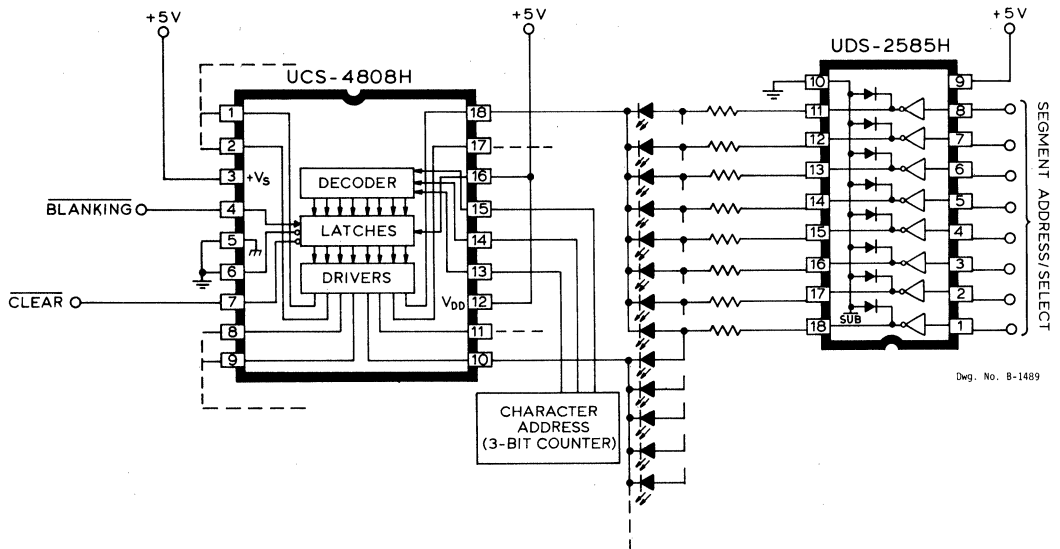
Dwg. No. B-1489

MULTIPLEXED POWER DRIVER

UCS-4807/08H
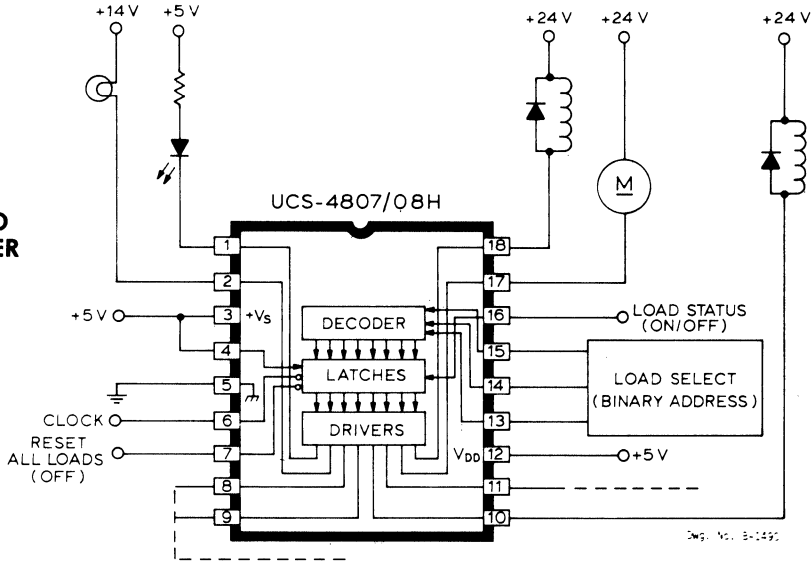
MULTI-CHANNEL INTERFACE TO HIGH-POWER LOADS

SPRAGUE BiMOS power drivers can be employed as multi-channel pre-drivers for discrete high-current or high-voltage semiconductors, thus reducing the need for many discrete components. For instance, any of the BiMOS sink drivers (Types UCS-4401/4801/4808/4821/4822/4823H) can provide enough current to the bases of discrete PNP power transistors to make 5 A load currents possible. Higher load currents can be obtained by using power Darlington devices. BiMOS source drivers (Types UCS-4810/4815H) will require discrete Darlington power drivers for any significant load currents, but have the added advantage of allowing rather wide load-voltage swings.

For a-c loads, it is possible to use a source driver to provide gate current (with appropriate current limiting) to a power SCR or triac. This scheme can provide an economical solution to many applications such as driving incandescent lamps or a-c motors with current levels of up to 20 A.

DISCRETE POWER DRIVERS FOR HIGH-POWER LOADS
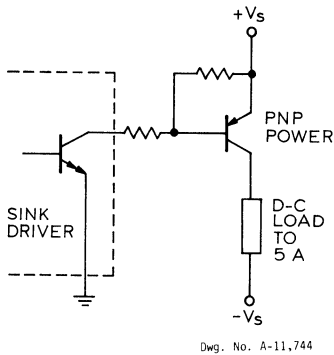
Dwg. No. A-11,744
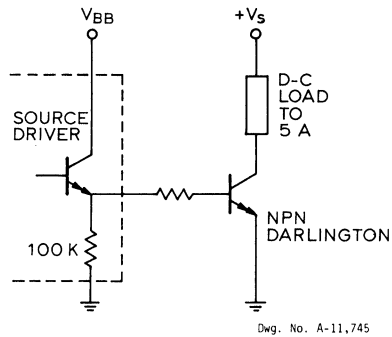
Dwg. No. A-11,745

BiMOS POWER DRIVERS TO MIL-STD-883, METHOD 5004

THE QUALITY ASSURANCE and Reliability department of Sprague Electric Company strives to assure that products delivered to customers are of the highest possible quality and reliability level and consistent with customer requirements. During product processing, there are several independent visual and electrical inspections performed by Quality Assurance personnel.

All full-temperature hermetic products are processed to stringent production screen inspec-tions and tests in accordance with MIL-STD-883, Method 5004, paragraphs 3.1.1 through 3.1.6. BiMOS power drivers subjected to burn-in and additional high-reliability screening (Method 5004, Class B) can be ordered by adding the suffix "-MIL" to the part number, for example UCS-4815H-MIL (side-brazed hermetic) or UCS-4815R-MIL (cer-DIP hermetic). This additional processing incorporates paragraphs 3.1.9 through 3.1.15, and 3.1.18 of the military standard.

```
WAFER                CONSTANT
FABRICATION          ACCELERATION
                     METHOD 2001
    │                    │
100%                 FINE & GROSS
PROBE                SEAL
                     METHOD 1014
    │                    │
SCRIBE               100%                    "-MIL" HIGH-RELIABILITY
&                    ELECTRICAL                    SCREENING
SORT                 PER SPECIFICATION
    │                    │                      BURN-IN
VISUAL                                          METHOD 1015
INSPECTION           MARKING
                                                    │
    │                    │                      100%
DIE ATTACH           QUALIFICATION             ELECTRICAL
AND                  OF CONFORMANCE
WIRE BOND            METHOD 5005                     │
    │                    │                      FINE & GROSS
INTERNAL             EXTERNAL                   SEAL
VISUAL               VISUAL                     METHOD 1014
METHOD 2010          METHOD 2009
    │                    │
STABILIZATION        PACK
BAKE
METHOD 1008
    │                    │
THERMAL              SHIP
SHOCK
METHOD 1011
```

Dwg. No. B-1492

SECTION 6—RADIO/COMMUNICATIONS INTEGRATED CIRCUITS

*New Product . . . Contact factory for detailed information.

SELECTION GUIDE TO RADIO/COMMUNICATIONS INTEGRATED CIRCUITS

Device Type	F-M R-F Mixer	F-M I-F	F-M Det.	Mute/ Squelch	Δ f Mute	Stereo Decoder	A-M Radio	Audio Amp
ULN-2111A	—	X	X	—	—	—	—	—
ULN-2204A	—	X	X	—	—	—	X	X
ULN-2240A	—	X	X	X	X	—	X	—
ULN-2241A	—	X	X	—	—	—	X	—
ULN-2242A	—	X	X	X	—	—	X	—
ULN-2243A	X	X	—	—	—	—	—	—
ULN-2249A	—	—	—	—	—	—	X	—
ULX-3803A*	—	X	X	—	—	—	X	—
ULN-3804A	—	X	X	—	—	—	X	—
ULN-3809A	—	—	—	—	—	X	—	—
ULN-3810A	—	—	—	—	—	X	—	—
ULN-3812A	—	—	—	—	—	X	—	—
ULN-3838A	—	—	—	—	—	—	X	X
ULN-3840A	—	X	X	X	X	—	X	—
ULN-3859A	X	X	X	X	—	—	—	—

NOTE: Additional devices for use as F-M radios can be found in Section 7; audio amplifiers appear in Section 8.
*New device. Contact factory for information.

ULN-2111A F-M I-F AMPLIFIER/LIMITER AND QUADRATURE DETECTOR

FEATURES

- Good Sensitivity
- Excellent A-M Rejection
- Low Harmonic Distortion
- Single-Adjustment Tuning
- High Gain to 50 MHz
- 500 mV Recovered Audio at 10.7 MHz
- Wide Operating Voltage Range
- Direct Replacement for ULN-2113A, MC1357, SN76643
- 14-Pin Dual In-Line Plastic Package
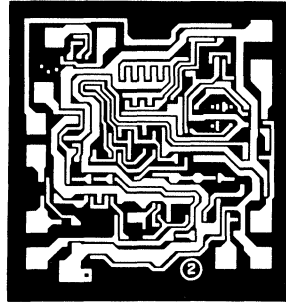
PROVIDING a multistage wideband amplifier/ limiter, an F-M quadrature detector, and an emitter-follower audio output stage, the Type ULN-2111A is designed for use in F-M receivers or in the sound I-F of TV receivers.

The Type ULN-2111A amplifier/limiter and quadrature detector is a Sprague-originated design. This circuit was the original monolithic integrated circuit F-M detector and was the first integrated circuit to be used in entertainment electronics. Its outstanding feature is that only a single low-cost tuned circuit is required instead of the previous triple-winding transformer.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 15 V
Package Power Dissipation, P_D . . . . 670 mW*
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

*Derate at the rate of 8.3 mW/°C above T_A = +70°C.

6
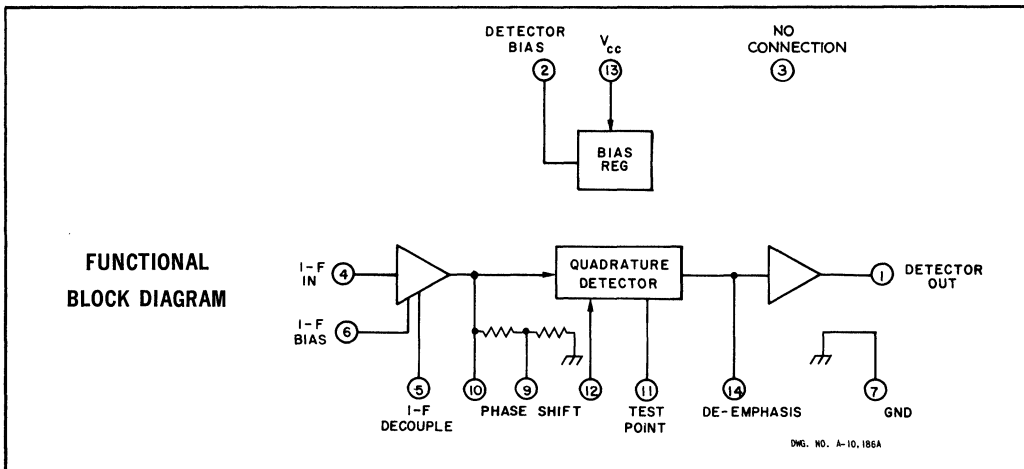
FUNCTIONAL BLOCK DIAGRAM

DWG. NO. A-10.186A

STATIC ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{cc} = +12\,V$

Characteristic	Symbol	Test Pin	Test Conditions	Min.	Typ.	Max.	Units
Supply Current	I_{cc}	13		12	17	27	mA
Terminal Voltage	V_1	1		4.3	5.7	7.2	V
	V_2	2		—	3.65	—	V
	V_6	6		—	1.45	—	V
	V_9	9		—	150	—	mV
	V_{10}	10		—	1.45	—	V
Resistance, Detector Output	R_1	1		—	200	—	Ω
I-F Input	R_4	4		—	5.0	—	kΩ
I-F Output	R_{10}	10		—	60	—	Ω
Detector Input	R_{12}	12		—	70	—	kΩ
De-Emphasis	R_{14}	14		6.0	9.0	12	kΩ
Capacitance, I-F Input	C_4	4		—	11	—	pF
Detector Input	C_{12}	12		—	2.7	—	pF

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{cc} = +12\,V$, $f_o = 10.7\,MHz$, $f_m = 400\,Hz$, $\Delta f = \pm 75\,kHz$, Peak Separation = 550 kHz

Characteristic	Symbol	Test Pin	Test Figure	Test Conditions	Min.	Typ.	Max.	Units	Notes
Amplifier Voltage Gain	A_e	10	1	$V_{in} \leq 300\,\mu V_{rms}$	—	53	—	dB	
Amplifier Output Voltage	V_{out}	10	1	$V_{in} = 10\,mV_{rms}$	—	1.45	—	V_{pp}	
Input Limiting Threshold	V_{th}	4	2		—	400	800	μV_{rms}	1, 3
Recovered Audio Output	V_{out}	1	2	$V_{12} = 60\,mV_{rms}$	—	500	—	mV_{rms}	3
Output Distortion	THD	1	2	100% F-M Modulation	—	1.0	—	%	3
A-M Rejection	AMR	1	3	$V_{in} = 10\,mV_{rms}$	—	40	—	dB	2

NOTES:
1. The input limiting threshold is the F-M input voltage for a recovered audio output which is 3 dB less than the recovered audio output for an F-M input voltage of 200 mV_{rms}.

2. The amplitude modulation rejection is determined by: $AMR_{db} = 20 \log \dfrac{V_{out} \text{ for 100\% F-M } V_{in}}{V_{out} \text{ for 30\% A-M } V_{in}}$

3. See also, General Design Note No. 9.

COMPONENT CHART

	Component Value	
	TV (4.5 MHz)	F-M (10.7 MHz)
L—Inductance	7.0 - 14 μH	1.5 - 3.0 μH
Unloaded Q	50	50
D-C Resistance	<50Ω	<50Ω
Type	Miller #9052	Miller #9050
C_1—Capacitance	120 pF	120 pF
TCC	NPO	NPO
C_2—Capacitance	3.0 pF	4.7 pF
R—Resistance	20 kΩ	3.9 kΩ
Loaded Network Q	30	20
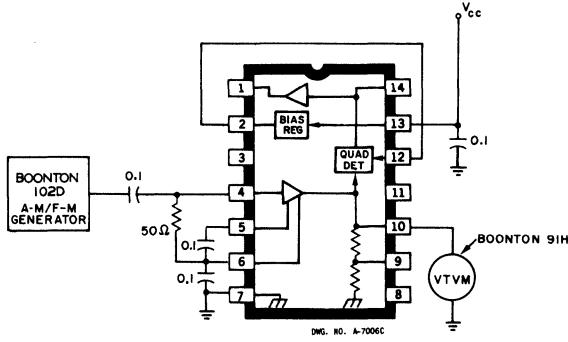
TEST FIGURE 1
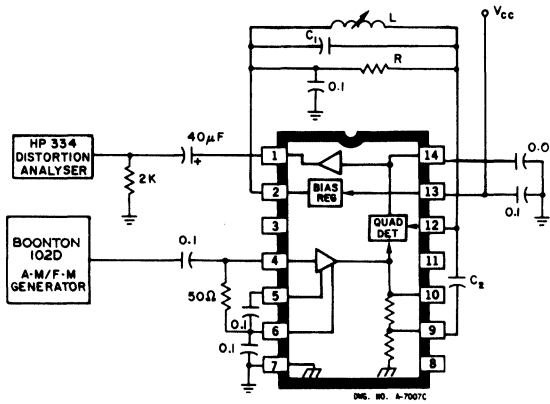
TEST FIGURE 2
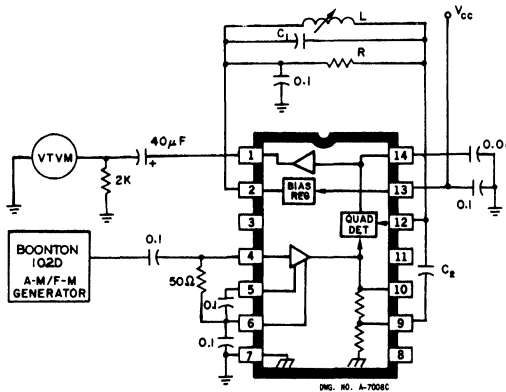
TEST FIGURE 3

6

TYPICAL APPLICATION

DWG. NO. A-6386D

TRANSFER CHARACTERISTICS

LINEAR DETECTION MODE ($V_{12} \leq 60mv_{rms}$) ————————

SWITCHING DETECTION MODE ($V_{12} \approx 600mV_{rms}$) — — — — — —
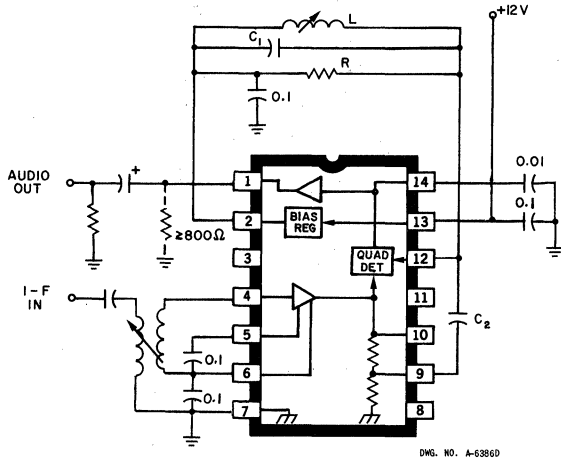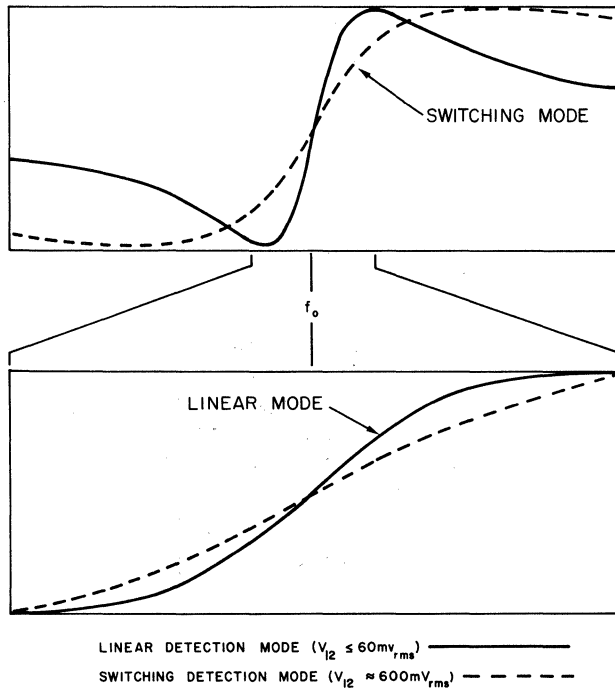
DWG. NO. A-10,180

GENERAL DESIGN NOTES

1. Phase shift network is aligned by applying F-M signal through decoupling network to pin 4 ($V_4 = 5\,mV_{rms}$). Tune for maximum recovered audio at pin 1 or maximum I-F voltage at pin 11.
2. A d-c path of less than $100\,\Omega$ must be provided between pins 2 and 12. No other biasing provisions are required.
3. A d-c path of less than $300\,\Omega$ must be provided between pins 4 and 6. No other biasing provisions are required.
4. The maximum a-c load current can be increased by adding an external resistor between pin 1 and ground. The minimum value for this resistor is $800\,\Omega$, giving a maximum load current of $4\,mA_{rms}$.

5. All decoupling capacitors should be of the ceramic type with minimum inductance at the operating frequency.

6. Decoupling capacitor leads at pins 2, 5, and 6 should be as short as possible.

7. Keep appropriate distance between the input (pin 4 and the input network) and the phase shift network (pins 9, 10, and 12, and the phase shift inductor).

8. If a high impedance power supply is used (voltage dropping resistor), decouple pin 13 for the lowest audio frequency.

9. The linear detection mode (low signal level at pin 12), as shown, is preferred for communications and other commercial applications, due to the preservation of the tuned circuit bandwidth and better rejection of Gaussian noise. The combination of coupling capacitor (C_2) and I-F amplifier output (pin 9) was chosen for optimum quieting. The bandwidth of the phase shift network (peak separation) is primarily defined by the Damping resistor (R). A higher value resistor will decrease bandwidth, increase the recovered audio output, reduce the capture ratio, and increase harmonic distortion.

10. The switching detection mode (high signal level at pin 12) features a greater linear range, increased insensitivity to amplitude variations, and is recommended for AFC applications or where side responses must be avoided. Limiting in the quadrature detector will produce slightly more audio output, but will increase the noise bandwidth and degrade quieting.

6

I-F AMPLIFIER GAIN
AS A FUNCTION OF FREQUENCY

DWG. NO. A-10.181
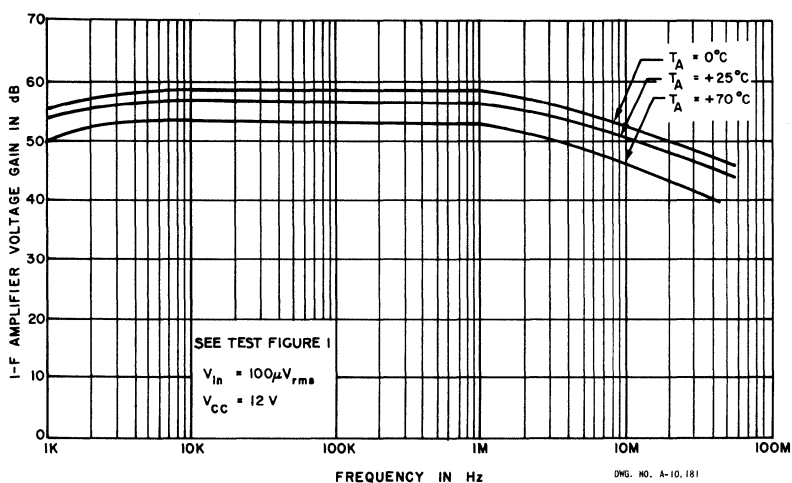
ULN-2204A A-M/F-M RADIO SYSTEM

FEATURES

- Low Harmonic Distortion
- Wide Operating Voltage Range
- Low Power Drain
- D-C A-M/F-M Switching
- 30 μV Limiting Threshold
- Excellent A-M Rejection
- Interchangeable With HA12402, TA7613, TDA1083, U417B
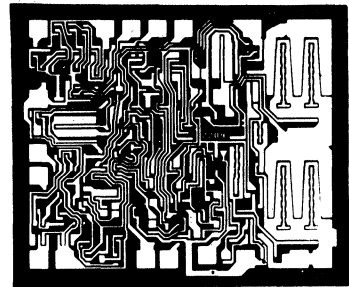
PROVIDING ALL radio functions except VHF tuning, Type ULN-2204A A-M/F-M radio system excels in low-cost applications requiring a minimal parts count and high performance.

In the A-M mode of operation, the device is a complete single-conversion superheterodyne broadcast or shortwave receiver with AGC and peak envelope detection. In the F-M mode, Type ULN-2204A operates as a high-gain I-F amplifier/limiter and phase-shift detector. A simple d-c switch is used to change mode of operation.

A single external capacitor at pin 16 provides the A-M AGC time constant, the F-M AFC time constant, and R-F decoupling. A single resistor at the same pin will adjust the A-M gain for optimal system performance.

The audio power amplifier will work into any speaker load of 8Ω or greater. Class B operation of the audio power amplifier yields high efficiency at rated output with very low quiescent power drain. The amplifier exhibits little crossover distortion. Its output impedance is significantly less than one ohm.

Type ULN-2204A will work with a wide range of supply voltages, and is suitable for use in a-c powered table radios and in battery-powered (6 or 9 V) portable radios.

This system will operate at supply voltages as low as 2 V at reduced volume without significant increase in distortion. Brown-outs or weak batteries need no longer be a major concern.

Type ULN-2204A is housed in a 16-pin dual in-line plastic package with a copper lead frame that eliminates many decoupling problems and allows maximum power dissipation.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . (Note 1)
Zener Current, I_{REG} . . . . 60 mA
Package Power Dissipation, P_D (Note 2) . . . . 1.0 W
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

NOTES:
1. Dependent on value of external current limiting resistor, 13 V at 0Ω.
2. Derate at the rate of 15 mW/°C above T_A = +70°C.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 6.0$ V, $R_8 = \infty$, $R_{16} = 1.2$ kΩ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
F-M MODE: $f_o = 10.7$ MHz, $f_m = 400$ Hz, $f_d = \pm 75$ kHz, Peak Separation = 550 kHz						
Input Limiting Threshold	V_{th}		—	30	60	μV
Detector Recovered Audio	V_o		—	250	—	mV
Detector Output Distortion	THD_D	$V_{in} = 10$ mV$_{rms}$	—	1.0	—	%
A-M Rejection	AMR	$V_{in} = 10$ mV$_{rms}$, 30% A-M, $f_{a-m} = 400$ Hz	35	50	—	dB
I-F Input Impedance	Z_2		—	40	—	kΩ
I-F Input Capacitance	C_2		—	4.0	—	pF
Quiescent Terminal Voltage	V_1		—	2.1	—	V
	V_8		—	1.7	—	V
Quiescent Supply Current	I_{CC}	$V_{CC} = 6.0$ V	—	14	20	mA
		$V_{CC} = 9.0$ V	—	18	—	mA
A-M MODE: $f_o = 1$ MHz, $f_{if} = 455$ kHz, $f_m = 400$ Hz, 30% A-M						
Sensitivity		$V_{out(8)} = 20$ mV$_{rms}$	—	5.0	10	μV
Detector Recovered Audio	V_o		—	150	—	mV
Overload Distortion		80% A-M, also see "ULN-2204A Variations"	—	10	—	mV
Usable Sensitivity		20 dB S+N/N	—	25	35	μV
Mixer Input Impedance	Z_6	See Note	—	4.5	—	kΩ
Mixer Input Capacitance	C_6		—	5.5	—	pF
Mixer Output Impedance	Z_4		—	25	—	kΩ
Mixer Output Capacitance	C_4		—	3.0	—	pF
I-F Input Impedance	Z_2		—	100	—	kΩ
I-F Input Capacitance	C_2		—	3.0	—	pF
Quiescent Terminal Voltage	V_1		—	1.3	—	V
	V_8		—	1.7	—	V
Quiescent Supply Current	I_{CC}	$V_{CC} = 6.0$ V	—	10	—	mA
		$V_{CC} = 9.0$ V	—	13	—	mA
AUDIO AMPLIFIER: $f_o = 400$ Hz, $R_L = 8Ω$						
Audio Gain	A_e		36	40	44	dB
Output Power	P_0	$V_{CC} = 3.0$ V, 10% THD	—	50	—	mW
		$V_{CC} = 6.0$ V, 10% THD	250	350	—	mW
		$V_{CC} = 9.0$ V, 10% THD	500	650	—	mW
Output Distortion	THD	$P_o = 50$ mW	—	2.0	—	%
A-F Input Impedance	Z_9		—	250	—	kΩ
Quiescent Terminal Voltage	V_{10}		—	1.1	—	V
	V_{12}		—	2.6	—	V

NOTE: For optimum noise match, source impedance should be 2.5 kΩ.

TEST CIRCUIT

DWG. NO. A-10,328B

*See "ULN-2204A Variations"

COIL WINDING INFORMATION

DWG. NO. A-10,370

T1 A-M First I-F 455 kHz	Qu = 120 N1:N2:N3 = 15.5:2.8:1 Ct = 180 pF	General Instrument Part No. EX 27835	Toko Part No. RMC-2A7641A
T2 A-M Second I-F 455 kHz	Qu = 70 N1:N2 = 2:1 Ct = 430 pF	General Instrument Part No. EX 27836	Toko Part No. RLE-4A7642G0
T3 F-M Detector 10.7 MHz	Qu = 50 Ct = 100 pF	General Instrument Part No. EX 27640	Toko Part No. BKAC-K3651HM
T4 F-M Detector 10.7 MHz	Qu = 50 Ct = 100 pF	General Instrument Part No. EX 27640	Toko Part No. BKAC-K3651HM
L1 A-M Oscillator 1455 kHz	Qu = 50 N1:N3 = 10.7:1 Ct = 39 pF	General Instrument Part No. EX 27641	Toko Part No. RWO-6A7640BM

FUNCTIONAL BLOCK DIAGRAM
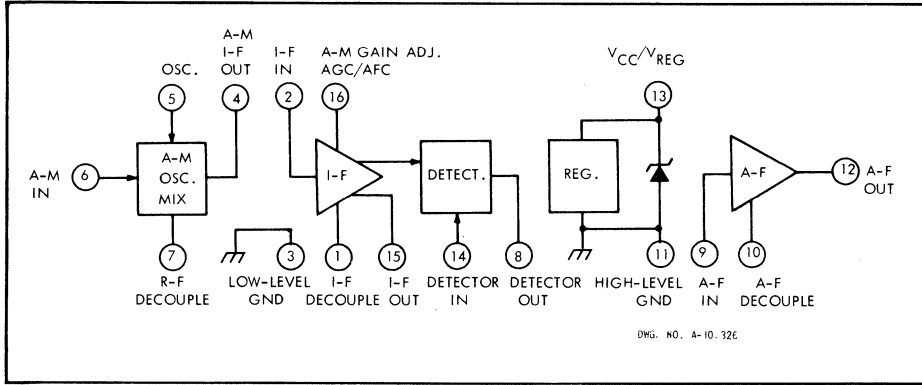
DWG. NO. A-10.326

PIN 16 OUTPUT VOLTAGE, V_{16}

A-M Operation	Complete Part Number Including Suffix		
	F-M Operation		
	2.20—2.65 V	2.55—3.05 V	2.95—3.40 V
1.40—1.75 V	ULN-2204A-11	ULN-2204A-21	ULN-2204A-31
1.65—2.00 V	ULN-2204A-12	ULN-2204A-22	ULN-2204A-32
1.90—2.25 V	ULN-2204A-13	ULN-2204A-23	ULN-2204A-33

6

TYPICAL QUIESCENT SUPPLY CURRENT

DWG. NO. A-10.325A

TYPICAL AUDIO POWER OUTPUT

DWG. NO. A-10.327

6—11
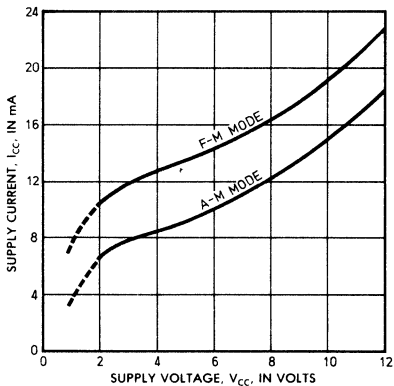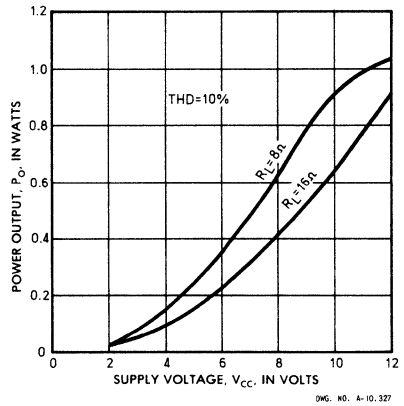
ULN-2204A VARIATIONS
FOR OPTIMAL SYSTEM PERFORMANCE

The receiver system's performance can be kept within tighter performance limits by matching bias groupings and appropriate external resistors (R_8 and R_{16}). With proper matching of parts and lots, consistent device performance can be obtained. Bias groups for Type ULN-2204A are shown in the table below. There are three selections for each mode of operation and nine possible combinations.

Sprague Electric Company recommends that customers do not specify particular selections except in unusual circumstances. All parts manufactured with Sprague part numbers are branded with appropriate part-number suffixes. Any shipment to a customer will consist of parts from a single selection (single suffix).

The first digit of the suffix (the "3" in ULN-2204A-31) refers to F-M performance. It indicates F-M gain and pin 16 output voltage as functions of the pin 16 load resistance. (See graph on next page.)

F-M circuit stability is inversely related to gain or sensitivity and is affected by source and load impedances, decoupling, and printed wiring board layout. After an optimal F-M I-F gain is determined for a particular circuit design, that gain can be attained by matching the part-number suffix and the pin 16 load.

In addition, some system designs derive the F-M tuner supply, tuner bias, or AFC voltage from pin 16 output of Type ULN-2204A. For example, if the tuner design requires 2.4 V at 2.0 mA (an equivalent R_{16} of 1200Ω), the graph below indicates a Type ULN-2204A-1X is required. A -2X or -3X device could also be used by paralleling the equivalent 1200Ω tuner load with a fixed resistance for an 830Ω load or a 520Ω load, respectively. For AFC applications, note that as frequency increases, V_{16} voltage decreases. The amount of change is a factor of load impedance, detector coil characteristics, and part grouping.

In A-M operation, stability is seldom a problem. However, large-signal overload can be optimized (to typically 30 mV) by matching the particular part group with an appropriate load resistor at pin 8. The A-M grouping of a device is identified by the second digit of the part-number suffix (the "1" in ULN-2204A-31).

For -X1, R_8 should be ∞.
For -X2, R_8 should be 47 kΩ.
For -X3, R_8 should be 33 kΩ.

Additional loading may raise the overload point slightly, but AGC and sensitivity will be compromised. For any fixed value of R_8, -X3 parts will exhibit slightly higher A-M gain, while -X1 parts will have slightly lower A-M gain.

TYPICAL F-M I-F GAIN CHARACTERISTIC
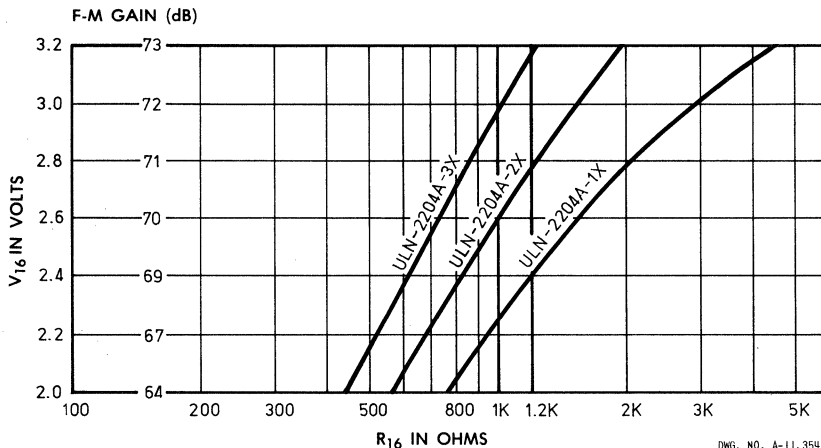
DWG. NO. A-11,354

TYPICAL APPLICATION

An A-M/F-M radio using the ULN-2204A receiver system, designed for a usable F-M sensitivity of about 4 μV and an A-M sensitivity of 350 μV/m, appears on the next page.

The two-stage F-M tuner is operated at about 4 V. Reducing the pin 16 voltage to 1.8 V (by changing R_{16}) reduces interstation noise and the F-M I-F gain. An inductor at pin 12 (L6) prevents the wide-band audio amplifier from

radiating R-F noise in the A-M spectrum.

The tuning indicator below may be added to the radio circuit to provide an LED indication when the received signal strength exceeds 7 μV in the F-M mode or 700 μV/m in the A-M mode. The tuning indicator circuit reduces the I-F gain by about 2 dB. The sensitivity may be adjusted by changing the value of C1 or C2.

TUNING INDICATOR
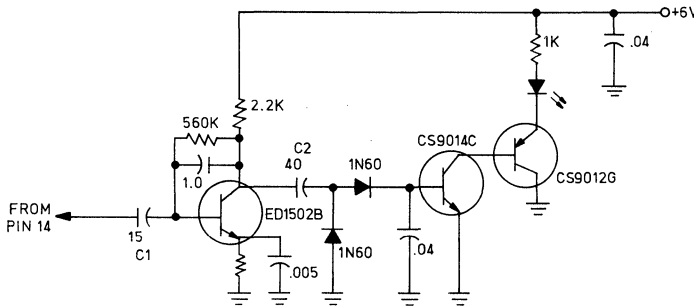
DWG. NO. A-11,355

COIL AND TRANSFORMER INFORMATION
FOR TYPICAL APPLICATION

L1	F-M Antenna Coil	4½ turns, #20 AWG (0.8 mm), 0.216″ (5.5 mm) 0
L2	F-M R-F Coil	3½ turns, #20 AWG (0.8 mm), 0.177″ (4.5 mm) 0
L3	F-M I-F Trap	16½ turns, #24 AWG (0.5 mm), 0.177″ (4.5 mm) 0
L4	F-M Oscillator Coil	2½ turns, #20 AWG (0.8 mm), 0.177″ (4.5 mm) 0
L5	F-M Detector Coil	15 μH, Qu = 120 @ 2.52 MHz
L6	Audio Choke	10 μH, Qu = 2 @ 2.52 MHz; 3 turns through ferrite bead
L7	A-M Antenna Coil	Qu = 250, 110:10 turns ratio; Q2B core, 3.5″ (90 mm) × 0.394″ (10 mm) 0
T1	F-M I-F Transformer	82 pF, Qu = 90 @ 10.7 MHz, 11:3 turns ratio
T2	F-M I-F Transformer	390 pF, Qu = 75 @ 10.7 MHz, 5:2 turns ratio
T3	A-M Detector Coil	390 pF, Qu = 130 @ 455 kHz, 100 turns center-tapped
T4	F-M Detector Coil	150 pF, Qu = 90 @ 10.7 MHz
T5	A-M Oscillator	460 μH, Qu = 120 @ 796 kHz, 110:11 turns ratio
T6	A-M I-F Transformer	180 pF, Qu = 145 @ 455 kHz, 155:10 turns ratio; primary tapped at 127 turns

Dwg. No. D-1107

*Required only for $V_{CC} \geq 9V$.

**I-F gain-dependent: See "ULN-2204A Variations".

TYPICAL APPLICATION

ULN-2240A A-M/F-M SIGNAL PROCESSOR

FEATURES

- 12 μV Limiting Threshold
- Tuning-Error and Signal-Level Muting
- Zero-Tune Meter Drive
- Balanced A-M Mixer
- 5 μV A-M Sensitivity
- D-C Mode Switching
- Internal Voltage Regulator
- Meets Dolby® Noise Requirements
- 20-Pin Dual In-Line Plastic Package
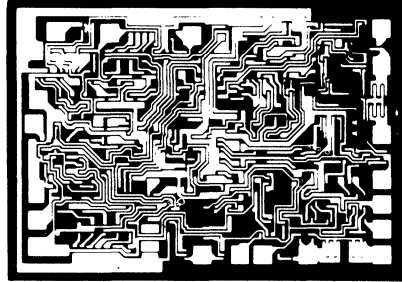
PREMIUM PERFORMANCE features such as delayed AGC for the R-F stage, an AFC drive circuit, interstation (signal level) muting, and off-channel (tuning error) muting, are offered by Type ULN-2240A.

®Registered Trademark, Dolby Laboratories, Inc.

The signal processor combines F-M I-F receiver functions and all A-M radio functions in a single monolithic integrated circuit. The system's audio output stage uses low-noise biasing that meets Dolby® receiver noise requirements.
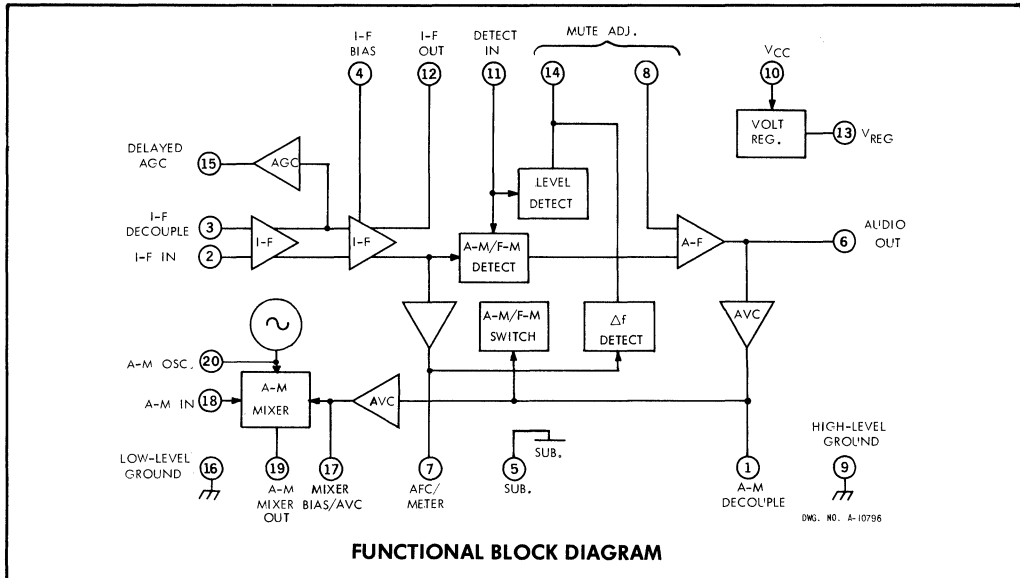
6

FUNCTIONAL BLOCK DIAGRAM

DWG. NO. A-10796

The A-M mixer is a balanced low-current analog multiplier with very low local oscillator feed-through, high I-F rejection and freedom from spurious responses. It can be used in the long, medium, and shortwave bands.

A balanced four-stage differential I-F amplifier is used in both A-M and F-M modes. It gives maximum gain without common-mode interference and noise. The delayed AGC output (pin 15) can be used for a discrete R-F stage or for stereo switching logic.

In the F-M mode of operation, the detector is a high-level, four-quadrant analog multiplier. In the A-M mode, the detector is operated as a balanced peak detector.

The low-level audio output is common to both operating modes and can be used to drive an audio power amplifier (ULN-3701Z) or stereo decoder (ULN-3810A).

A-M gain is controlled with AVC to the I-F and delayed AVC to the mixer. Switching between modes is done with a single-pole d-c switch.

Type ULN-2240A signal processor excels in signal-seeking or scanning applications. False triggers on adjacent channels or strong mistuned signals are eliminated since off-tune mute voltage changes are more pronounced than the usual signal-level voltage changes. In standard F-M radio applications, tuning-error muting eliminates the low-frequency "thump" and noise-tail associated with tuning through a strong signal.

Internal voltage regulators assure consistent performance with wide variations in supply voltage (8.5 to 16 V) and temperature.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 18 V
Mute Input Voltage, V_8 .... 5.0 V
Regulator Current, I_{REG} .... 5.0 mA
Package Power Dissipation, P_D (see note) .... 750 mW
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −65°C to +150°C

Note: P_D is derated at the rate of 9.4 mW/°C above $T_A = +70$°C.

TYPICAL A-M/F-M STEREO RECEIVER
FOR AUTOMOTIVE APPLICATIONS
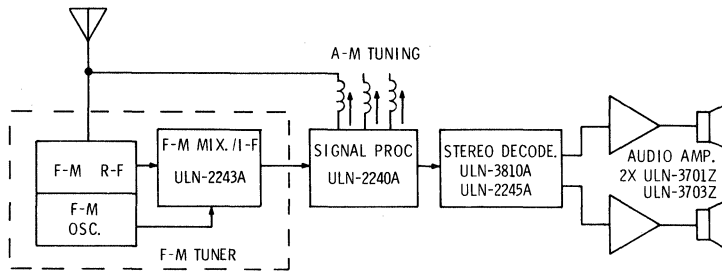
Dwg. No. A-11,020

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 12.8$ V

Characteristic	Symbol	Test Pin	Test Conditions	Min.	Typ.	Max.	Units
Operating Voltage Range	V_{CC}	10		8.5	12.8	16	V
Audio Output Voltage	V_6	6	No Signal	—	5.8	—	V
Regulator Output Voltage	V_{REG}	13	No Signal	—	6.4	—	V
Avail. Reg. Output Current	I_{REG}	13		2.0	—	—	mA

F-M MODE: $f_o = 10.7$ MHz, $f_m = 400$ Hz, $f_d = ±75$ kHz, $V_{in} = 10$ mVrms, Non-Muted (unless otherwise specified)

Characteristic	Symbol	Test Pin	Test Conditions	Min.	Typ.	Max.	Units
Input Limiting Threshold	V_{TH}	2		—	12	25	μV
Recovered Audio	V_{out}	6		350	425	600	mV
Output Distortion	THD	6		—	0.3	0.7	%
Output Noise	S + N/N	6		74	80	—	dB
A-M Rejection	AMR	6	See Note	40	> 55	—	dB
Mute	ΔV_{out}	6	$V_{in} = 100$ μV, max. mute	—	—	−1.0	dB
			$V_{in} = 5.0$ μV, max. mute	−45	—	—	dB
Mute Bandwidth	Δf_w	6	Max. mute	—	100	—	kHz
I-F Input Voltage	V_2	2	No Signal	—	3.5	—	V
Mute Output Voltage	V_{14}	14	No Signal	3.6	4.2	—	V
AGC Output Voltage	V_{15}	15	No Signal	4.2	4.8	5.5	V
			$V_{in} = 10$ mVrms	—	—	0.5	V
Mute Output Current	I_{14}	14	No Signal	0.5	—	—	mA
Avail. AGC Output Current	I_{15}	15	No Signal	1.0	—	—	mA
Supply Current	I_{CC}		No Signal	—	26	40	mA

A-M MODE: $f_o = 1$ MHz, $f_{if} = 455$ kHz, $f_m = 400$ Hz, 30% A-M, $V_{in} = 1.0$ mVrms (unless otherwise specified)

Characteristic	Symbol	Test Pin	Test Conditions	Min.	Typ.	Max.	Units
Sensitivity	V_{in}	18	$V_{out} = 50$ mVrms	—	5.0	8.5	μV
Usable Sensitivity		18	20 dB S+N/N	—	6.0	—	μV
Recovered Audio	V_{out}	6	80% A-M	250	325	600	mV
Input Overload	V_{in}	18	80% A-M, THD = 10%	25	50	—	mV
A-M Decoupling Voltage	V_1	1	No Signal	—	1.0	—	V
I-F Input Voltage	V_2	2	No Signal	—	3.7	—	V
Mute Output Voltage	V_{14}	14	No Signal	—	—	0.5	V
AGC Output Voltage	V_{15}	15	No Signal	—	—	0.5	V
A-M Bias Voltage	V_{17}	17	No Signal	1.6	1.8	2.1	V
Supply Current	I_{CC}		No Signal	—	16	30	mA

Note:

Amplitude Modulation Rejection is specified as $20 \log \dfrac{V_{out} \text{ for 100\% F-M } V_{in}}{V_{out} \text{ for 30\% A-M } V_{in}}$

COIL WINDING INFORMATION

T1	A-M I-F 455 kHz	Qu = 45 Ct = 1000 pF	General Instrument Part No. EX 27765	Toko Part No. RXN-6A6909HM
T2	F-M Detector 10.7 MHz	Qu = 60 Ct = 82 pF	General Instrument Part No. EX 27975	Toko Part No. TKAC-17044Z
L1	A-M Oscillator 1455 kHz	Qu = 50 N1:N2 = 11:1 Ct = 39 pF	General Instrument Part No. EX 27641	Toko Part No. RWO-6A7640BM
L2	F-M Detector 10.7 MHz	L = 18 μH Qu = 55	Coilcraft Type V	

DWG. NO. A-10,1128

SMALL-SIGNAL A-C CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Pin	Test Conditions	Limits			Units
				Min.	Typ.	Max.	
I-F Input Capacitance	C_2	2		—	6.0	—	pF
I-F Output Resistance	R_{12}	12		—	250	—	kΩ
I-F Output Capacitance	C_{12}	12		—	2.5	—	pF
Audio Output Impedance	Z_6	6		—	6.2	—	kΩ
F-M MODE: $f_o = 10.7$ MHz							
I-F Input Resistance	R_2	2		—	10	—	kΩ
I-F Transconductance	g_m	2-12		—	8.0	—	mho*
Detector Input Resistance	R_{11}	11		—	100	—	kΩ
Detector Input Capacitance	C_{11}	11		—	1.5	—	pF
A-M MODE: $f_o = 1$ MHz, $f_{if} = 455$ kHz							
A-M Input Resistance	R_{18}	18		—	5.0	—	kΩ
A-M Input Capacitance	C_{18}	18		—	20	—	pF
Mixer Transconductance	g_m	18-19		—	15	—	mmho*
Mixer Output Resistance	R_{19}	19		—	500	—	kΩ
Mixer Output Capacitance	C_{19}	19		—	5.0	—	pF
I-F Input Resistance	R_2	2		—	15	—	kΩ
I-F Transconductance	g_m	2-12		—	160	—	mmho*
Detector Input Resistance	R_{11}	11		—	250	—	kΩ
Detector Input Capacitance	C_{11}	11		—	1.0	—	pF

*The International Electrotechnical Commission recommends the use of siemens (S) as the standard international unit of conductance, admittance and susceptance.

TEST CIRCUIT

DWG. NO. A-10,796

DWG. NO. A-10,429

Filter Assembly:
Toko Part No. CFU455C-82BR

A-M CHARACTERISTICS
AS FUNCTIONS OF INPUT VOLTAGE
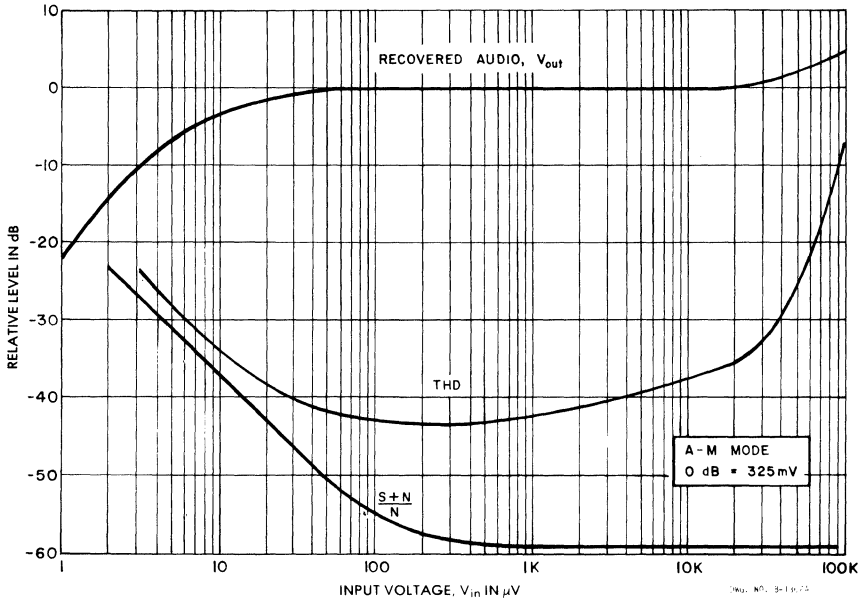
RECOVERED AUDIO, V_{out}

THD

A-M MODE
0 dB = 325 mV

$\frac{S+N}{N}$

RELATIVE LEVEL IN dB

INPUT VOLTAGE, V_{in} IN μV

DWG. NO. B-1367A

F-M CHARACTERISTICS
AS FUNCTIONS OF INPUT VOLTAGE

RECOVERED AUDIO, V_{out}

F-M MODE
0 dB = 425 mV

OUTPUT NOISE

A-M REJECTION

TO -80 dB

RELATIVE LEVEL IN dB

INPUT VOLTAGE, V_{in} IN μV

DWG. NO. B-1368A

6

6—19
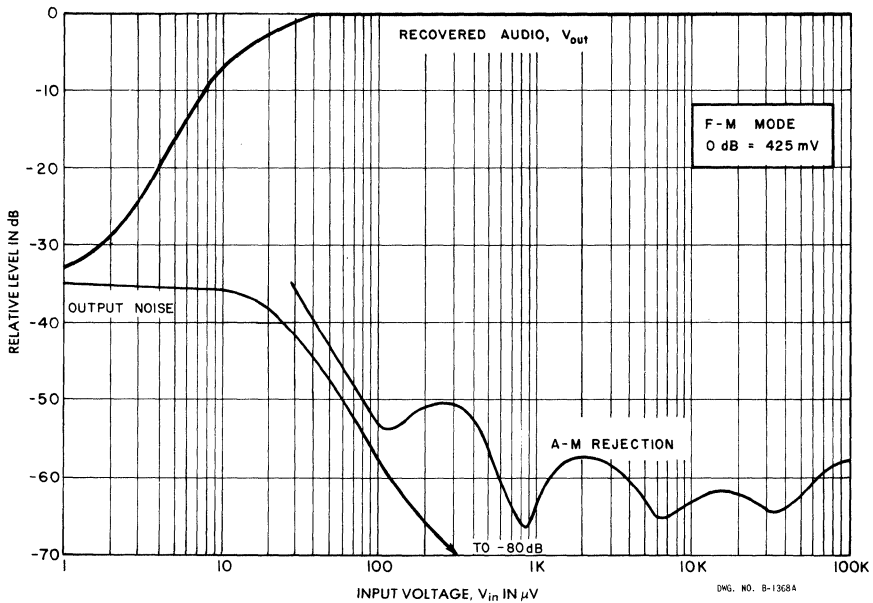
A-M CONTROL VOLTAGES
AS FUNCTIONS OF INPUT VOLTAGE
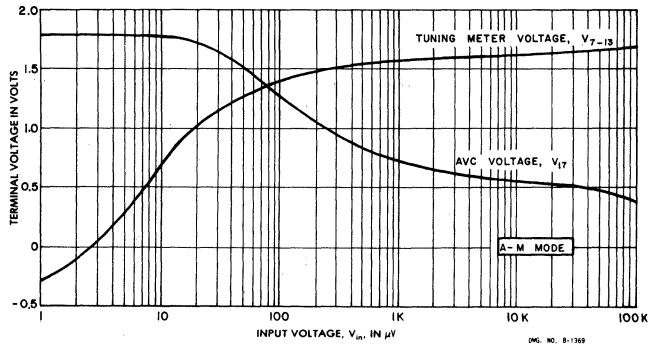
F-M CONTROL VOLTAGES
AS FUNCTIONS OF INPUT VOLTAGE
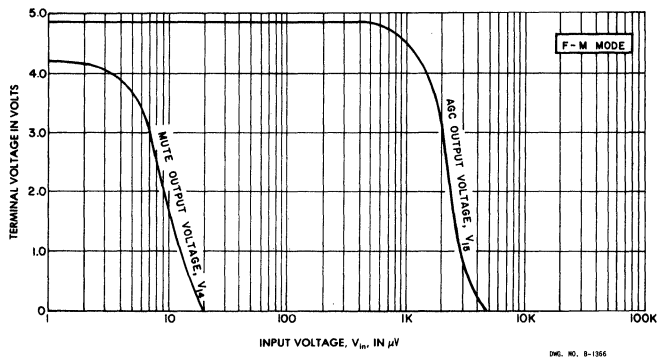
F-M TUNING-ERROR DETECTOR RESPONSE
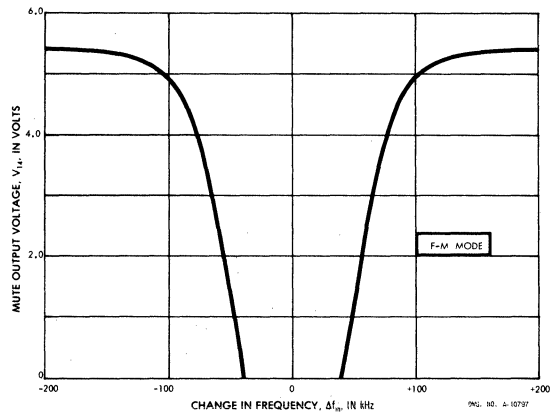
ULN-2241A
A-M/F-M SIGNAL PROCESSING SYSTEM

FEATURES

- Low External Parts Count
- D-C A-M/F-M Switching
- 12 μV Limiting Threshold
- 5 μV A-M Sensitivity
- Low Harmonic Distortion
- Balanced A-M Mixer
- Internal Regulator
- 16-Pin Dual In-Line Plastic Package
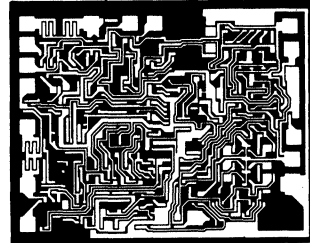
THIS SIGNAL PROCESSING SYSTEM was designed with careful attention to the total system costs and performance requirements of modern automotive and high-quality home entertainment broadcast receivers. All F-M I-F functions and all A-M functions are provided by Sprague Type ULN-2241A with a minimal external parts count.

The use of an analog multiplier as a balanced low-current mixer results in freedom from spurious responses and gives the system high tweet rejection, low feedthrough (I-F rejection), and low noise, as well as very low local oscillator feedthrough.

6
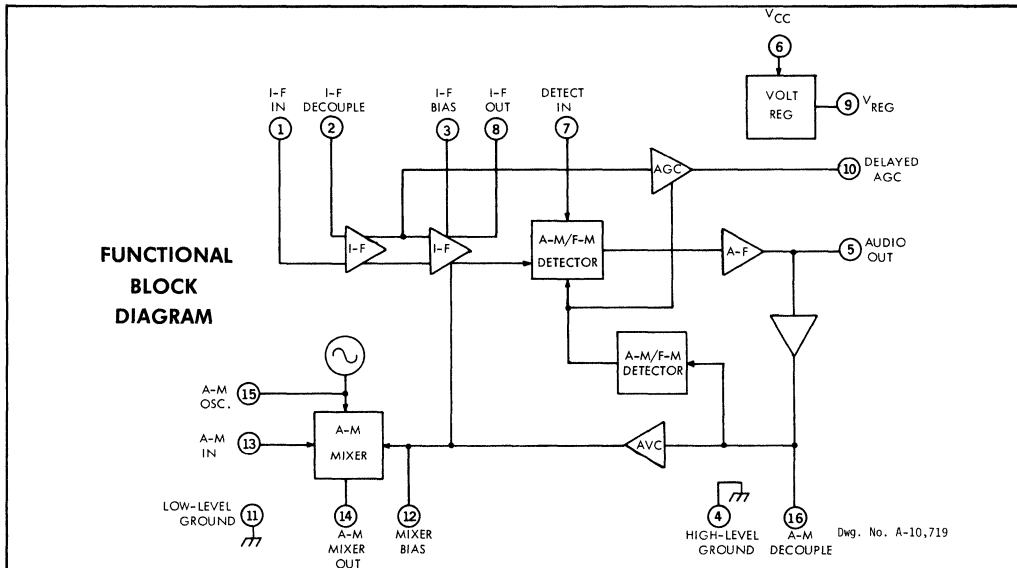
FUNCTIONAL
BLOCK
DIAGRAM

Dwg. No. A-10,719

Although primarily intended for use in A-M broadcast reception, the A-M mixer is also suitable for use at long-wave or shortwave frequencies. Delayed AGC is available for use with an optional discrete R-F stage.

A fully-balanced, four stage differential I-F amplifier gives maximum gain with freedom from interference and noise. It is used in both the A-M and F-M modes of operation with approximately 82 dB gain in the F-M mode and controlled AGC gain of 26 dB in the A-M mode.

The detector in the F-M mode is a four-quadrant analog multiplier operating in the high-level injection mode. Again, interference and noise are rejected through the use of balanced current-mirror outputs.

The delayed AGC output provides a d-c voltage for control of signal level-related functions. The detector is biased to a no-signal value of 4.7 V, that approaches 0 V with increasing signal input.

In the A-M mode of operation, the detector is configured as a balanced peak detector resulting in low audio distortion. A-M gain control is achieved with AVC applied to the I-F and with delayed AVC applied to the mixer.

Switching between modes can be accomplished with a simple single-pole d-c switch. The common low-level audio output can be used to drive any suitable audio power amplifier or stereo decoder (e.g. Sprague Types ULN-3701Z and ULN-3810A, respectively).

Internal voltage regulators and bias supplies assure premium performance despite variations in external supply voltage (8.5 to 16 V) or temperature ($-20°C$ to $+85°C$). Separate ground leads minimize possible decoupling problems.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 18 V
Regulator Current, I_{REG} . . . . 5.0 mA
Package Power Dissipation, P_D (see note) . . . . 640 mW
Operating Temperature Range, T_A . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . . $-65°C$ to $+150°C$

NOTE: P_D is derated at the rate of 8.0 mW/°C above $T_A = +70°C$.

TYPICAL APPLICATION
(High-Performance Table Radio)
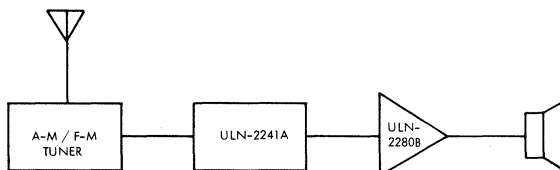
DWG. NO. A-10.974

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 12.8$ V

Characteristic	Symbol	Test Pin	Test Conditions	Min.	Typ.	Max.	Units
Operating Voltage Range	V_{CC}	6		10	12.8	16	V
Differential Audio Output	V_{out}	5	See Note 1	—	—	±3.0	dB
Audio Ouput Voltage	V_5	5	No Signal	—	5.8	—	V
Avail. Reg. Output Voltage	V_{REG}	9	No Signal	—	6.4	—	V
Avail. Reg. Output Current	I_{REG}	9		2.0	—	—	mA

F-M MODE: $f_o = 10.7$ MHz, $f_m = 400$ Hz, $f_d = ±75$ kHz, $V_{in} = 10$ mV$_{rms}$, Non-Muted (unless otherwise specified)

Characteristic	Symbol	Test Pin	Test Conditions	Min.	Typ.	Max.	Units
Input Limiting Threshold	V_{TH}	1		—	12	25	μV
Recovered Audio	V_{out}	5		350	425	600	mV
Output Distortion	THD	5		—	0.3	0.7	%
A-M Rejection	AMR	5	See Note 2	40	>55	—	dB
I-F Input Voltage	V_1	1	No Signal	—	3.5	—	V
AGC Output Voltage	V_{10}	10	No Signal	4.2	4.8	5.5	V
			$V_{in} = 10$ mV$_{rms}$	—	—	0.5	V
Avail. AGC Output Current	I_{10}	10	No Signal	1.0	—	—	mA
Supply Current	I_{CC}		No Signal	—	23	35	mA

A-M MODE: $f_o = 1$ MHz, $f_{if} = 455$ kHz, $f_m = 400$ Hz, 30% A-M, $V_{in} = 1.0$ mV$_{rms}$ (unless otherwise specified)

Characteristic	Symbol	Test Pin	Test Conditions	Min.	Typ.	Max.	Units
Sensitivity	V_{in}	13	$V_{out} = 50$ mV$_{rms}$	—	5.0	8.5	μV
Useable Sensitivity		13	20 dB S + N/N	—	6.0	—	μV
Recovered Audio	V_{out}	5	80% A-M	250	325	550	mV
Input Overload	V_{in}	13	80% A-M, THD = 10%	25	50	—	mV
A-M Decoupling Voltage	V_{16}	16	No Signal	—	1.0	—	V
I-F Input Voltage	V_1	1	No Signal	—	3.7	—	V
AGC Output Voltage	V_{10}	10	No Signal	—	—	0.5	V
A-M Input Voltage	V_{12}	12	No Signal	1.6	1.8	2.1	V
Supply Current	I_{CC}		No Signal	—	16	30	mA

Notes: 1. Differential Audio Output is specified as $20 \log \dfrac{V_{out} \text{ for 10 mV F-M } V_{in}}{V_{out} \text{ for 1.0 mV A-M } V_{in}}$

2. Amplitude Modulation Rejection is specified as $20 \log \dfrac{V_{out} \text{ for 100\% F-M } V_{in}}{V_{out} \text{ for 30\% A-M } V_{in}}$

COIL WINDING INFORMATION

T1 A-M I-F 455 kHz	Qu = 45 Ct = 1000 pF	General Instrument Part No. EX 27765	Toko Part No. RXN-6A6909HM
T2 F-M Detector 10.7 MHz	Qu = 60 Ct = 82 pF	General Instrument Part No. EX 27975	Toko Part No. TKAC-17044Z
L1 A-M Oscillator 1455 kHz	Qu = 50 N1:N2 = 11:1 Ct = 39 pF	General Instrument Part No. EX 27641	Toko Part No. RWO-6A7640BM
L2 F-M Detector 10.7 MHz	L = 27 μH Qu = 55 @ 2.5 MHz	General Instrument Part No. EX 27764	Toko Part No. 154A0-7A6115HM
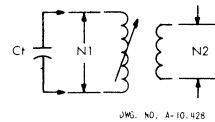
SMALL-SIGNAL A-C CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Pin	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
I-F Input Capacitance	C_1	1		—	6.0	—	pF
I-F Output Resistance	R_8	8		—	250	—	kΩ
I-F Output Capacitance	C_8	8		—	2.5	—	pF
Audio Output Impedance	Z_5	5		—	860	—	Ω
F-M MODE: $f_o = 10.7$ MHz							
I-F Input Resistance	R_1	1		—	10	—	kΩ
I-F Transconductance	g_m	1-8		—	8.0	—	mho*
Detector Input Resistance	R_7	7		—	100	—	kΩ
Detector Input Capacitance	C_7	7		—	1.5	—	pF
A-M MODE: $f_o = 1$ MHz, $f_{If} = 455$ kHz							
A-M Input Resistance	R_{13}	13		—	5.0	—	kΩ
A-M Input Capacitance	C_{13}	13		—	20	—	pF
Mixer Transconductance	g_m	13-14		—	15	—	mmho*
Mixer Output Resistance	R_{14}	14		—	500	—	kΩ
Mixer Output Capacitance	C_{14}	14		—	5.0	—	pF
I-F Input Resistance	R_1	1		—	15	—	kΩ
I-F Transconductance	g_m	1-8		—	160	—	mmho*
Detector Input Resistance	R_7	7		—	250	—	kΩ
Detector Input Capacitance	C_7	7		—	1.0	—	pF

*The International Electrotechnical Commission recommends the use of siemens (S) as the standard international unit of conductance, admittance and susceptance.

TEST CIRCUIT
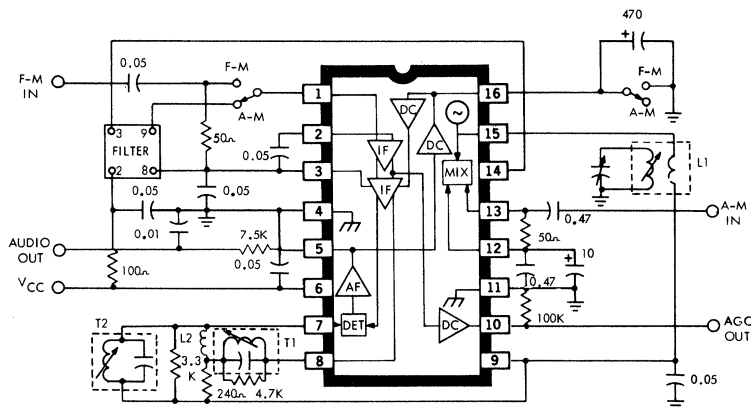
DWG. NO. A-10.718

Filter Assembly:
Toko Part No. CFU455C-82BR
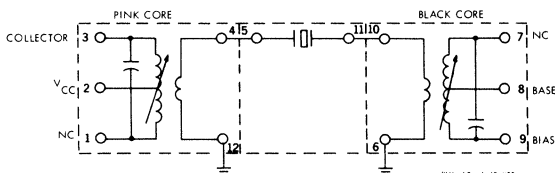
DWG. NO. A-10.429

F-M CHARACTERISTICS
AS FUNCTIONS OF INPUT VOLTAGE

RECOVERED AUDIO, V_{out}

F-M MODE
0 dB = 425 mV

OUTPUT NOISE

A-M REJECTION

TO -80 dB

RELATIVE LEVEL IN dB

INPUT VOLTAGE, V_{in}, IN μV

DWG. NO. B-1368A

A-M CHARACTERISTICS
AS FUNCTIONS OF INPUT VOLTAGE

RECOVERED AUDIO, V_{out}

THD

A-M MODE
0 dB = 325 mV

$\dfrac{S+N}{N}$

RELATIVE LEVEL IN dB

INPUT VOLTAGE, V_{in}, IN μV

DWG. NO. B-1367A
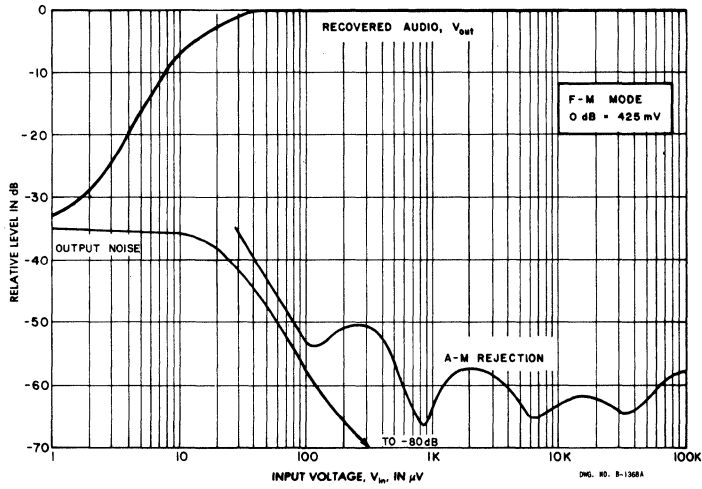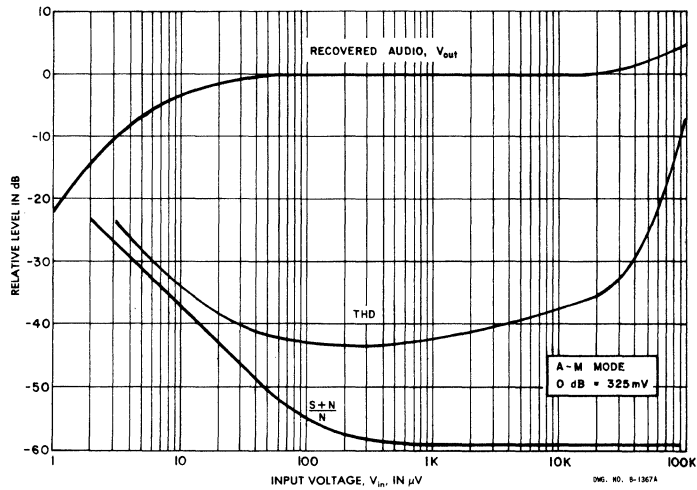
AGC OUTPUT VOLTAGE
AS A FUNCTION OF INPUT VOLTAGE
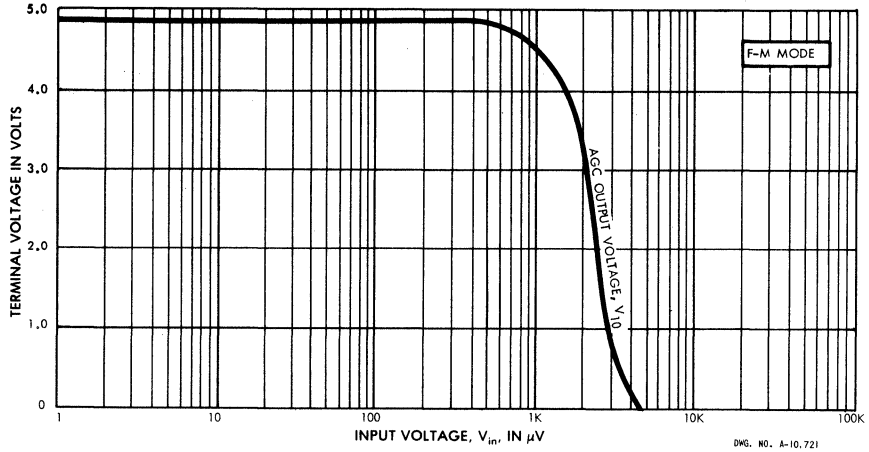
AVC VOLTAGE
AS A FUNCTION OF INPUT VOLTAGE
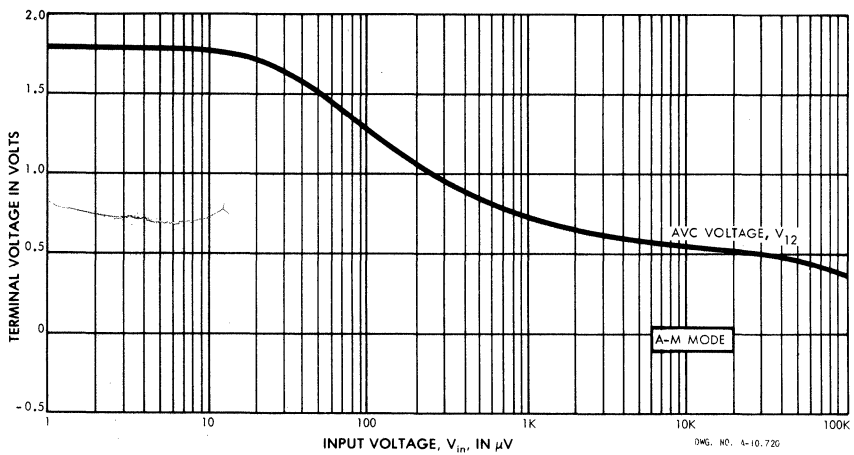
ULN-2242A/TDA1090
A-M/F-M SIGNAL PROCESSING SYSTEM

FEATURES

- Low External Parts Count
- D-C A-M/F-M Switching
- 12 μV Limiting Threshold
- 5 μV A-M Sensitivity
- Low Harmonic Distortion
- Balanced A-M Mixer
- Meter Drive
- Internal Regulator
- Self-Contained Muting (Squelch)
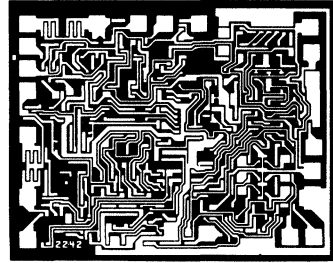
SUBSTANTIAL SIMPLIFICATION of A-M/F-M receiver design is possible with Type ULN-2242A signal processing system with improved system performance and a minimal external parts count. All F-M I-F functions and all A-M functions are provided by this monolithic integrated circuit.

The use of an analog multiplier as a balanced low-current mixer results in freedom from spurious responses, high tweet rejection, low feedthrough (I-F rejection), and low noise, as well as very low local oscillator radiation.

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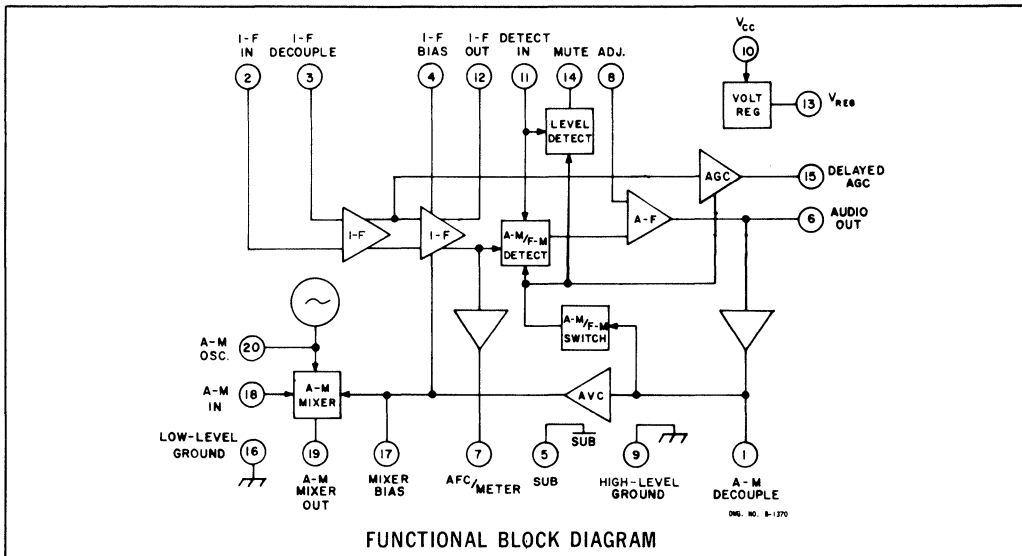
FUNCTIONAL BLOCK DIAGRAM

Although primarily intended for use in A-M broadcast reception, the A-M mixer is also suitable for use at long-wave or short-wave frequencies. Delayed AGC is available for use with an optional, discrete R-F stage.

A fully-balanced, four-stage differential I-F amplifier gives maximum gain with freedom from common-mode signals. It is used in both the A-M and F-M modes of operation with approximately 82 dB gain in the F-M mode and controlled AGC gain of 26 to 82 dB in the A-M mode.

The detector in the F-M mode is a four-quadrant analog multiplier operating in the high-level injection mode. Interference and noise are rejected. AFC and meter-drive signals (pin 7) are generated for use with any reference voltage between V_{CC} and ground, with AFC gain determined by the choice of load resistor.

The mute and delayed AGC outputs provide d-c voltages for control of signal-level-related functions. Both detectors are biased to a no-signal value of 4.7 V and approach zero with increasing signal input.

In the A-M mode of operation, the detector is configured as a balanced peak detector for low audio distortion. A-M gain control is achieved with AVC applied to the I-F and delayed AVC applied to the mixer.

Switching between modes can be accomplished with a simple single-pole d-c switch. The common low-level audio output can be used to drive any suitable audio power amplifier or stereo decoder (Sprague Type ULN-3703Z and ULN-3810A, respectively).

Internal voltage regulators and bias supplies assure premium performance despite variations in external supply voltage (8.5 to 16 V) or temperature ($-20°C$ to $+85°C$). Separate ground leads minimize possible decoupling problems.

Type ULN-2242A A-M/F-M signal processing system is housed in a 20-pin dual in-line plastic package. Parts are marked with the Sprague Electric part number (ULN-2242A) unless the Pro-Electron marking (TDA1090) is requested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 18 V
Mute Input Voltage, V_8 . . . . 5.0 V
Package Power Dissipation, P_D (see note) . . . . 750 mW
Operating Temperature Range, T_A . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . . $-65°C$ to $+150°C$

Note: P_D is derated at the rate of 9.4 mW/°C above $T_A = +70°C$.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 12.8$ V

Characteristic	Symbol	Test Pin	Test Conditions	Min.	Typ.	Max.	Units
Operating Voltage Range	V_{CC}	10		8.5	12.8	16	V
Audio Output Voltage	V_6	6	No Signal	—	5.8	—	V
Regulator Output Voltage	V_{REG}	13	No Signal	—	6.4	—	V
Regulator Output Current	I_{REG}	13		2.0	—	—	mA

F-M MODE: $f_o = 10.7$ MHz, $f_m = 400$ Hz, $f_d = \pm75$ kHz, $V_{in} = 10$ mVrms, Non-Muted (unless otherwise specified)

Input Limiting Threshold	V_{TH}	2		—	12	25	μV
Recovered Audio	V_{out}	6		350	425	600	mV
Output Distortion	THD	6		—	0.3	0.7	%
A-M Rejection	AMR	6	See Note	40	>55	—	dB
Mute	ΔV_{out}	6	$V_{in} = 100\ \mu$V, max. mute	—	—	−1.0	dB
			$V_{in} = 5\ \mu$V, max. mute	−45	—	—	dB
AFC Output Voltage	V_{afc}	7		220	—	600	mV
I-F Input Voltage	V_2	2	No Signal	—	3.5	—	V
Mute Output Voltage	V_{14}	14	No Signal	3.6	4.2	—	V
AGC Output Voltage	V_{15}	15	No Signal	4.2	4.8	5.5	V
			$V_{in} = 10$ mVrms	—	—	0.5	V
Mute Output Current	I_{14}	14	No Signal	0.5	—	—	mA
AGC Output Current	I_{15}	15	No Signal	1.0	—	—	mA
Supply Current	I_{CC}		No Signal	—	23	35	mA

A-M MODE: $f_o = 1$ MHz, $f_{if} = 455$ kHz, $f_m = 400$ Hz, 30% A-M, $V_{in} = 1.0$ mVrms (unless otherwise specified)

Sensitivity	V_{in}	18	$V_{out} = 50$ mVrms	—	5.0	8.5	μV
Usable Sensitivity		18	20 dB S+N/N	—	6.0	—	μV
Recovered Audio	V_{out}	6	80% A-M	250	325	600	mV
Input Overload	V_{in}	18	80% A-M, THD = 10%	25	50	—	mV
A-M Decoupling Voltage	V_1	1	No Signal	—	1.0	—	V
I-F Input Voltage	V_2	2	No Signal	—	3.7	—	V
Mute Output Voltage	V_{14}	14	No Signal	—	—	0.5	V
AGC Output Voltage	V_{15}	15	No Signal	—	—	0.5	V
A-M Input Voltage	V_{17}	17	No Signal	1.6	1.8	2.1	V
Supply Current	I_{CC}		No Signal	—	16	30	mA

Note:
Amplitude Modulation Rejection is specified as $20 \log \dfrac{V_{out} \text{ for } 100\% \text{ F-M } V_{in}}{V_{out} \text{ for } 30\% \text{ A-M } V_{in}}$

6

SMALL-SIGNAL A-C CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Pin	Test Conditions	Min.	Typ.	Max.	Units
I-F Input Capacitance	C_2	2		—	6.0	—	pF
I-F Output Resistance	R_{12}	12		—	250	—	kΩ
I-F Output Capacitance	C_{12}	12		—	2.5	—	pF
Audio Output Impedance	Z_6	6		—	860	—	Ω
F-M MODE: $f_o = 10.7$ MHz							
I-F Input Resistance	R_2	2		—	10	—	kΩ
I-F Transconductance	g_m	2-12		—	18	—	mho*
Detector Input Resistance	R_{11}	11		—	100	—	kΩ
Detector Input Capacitance	C_{11}	11		—	1.5	—	pF
A-M MODE: $f_o = 1$ MHz, $f_{if} = 455$ kHz							
A-M Input Resistance	R_{18}	18		—	5.0	—	kΩ
A-M Input Capacitance	C_{18}	18		—	20	—	pF
Mixer Transconductance	g_m	18-19		—	15	—	mmho*
Mixer Output Resistance	R_{19}	19		—	500	—	kΩ
Mixer Output Capacitance	C_{19}	19		—	5.0	—	pF
I-F Input Resistance	R_2	2		—	15	—	kΩ
I-F Transconductance	g_m	2-12		—	300	—	mmho*
Detector Input Resistance	R_{11}	11		—	250	—	kΩ
Detector Input Capacitance	C_{11}	11		—	1.0	—	pF

*The International Electrotechnical Commission recommends the use of siemens (S) as the standard international unit of conductance, admittance and susceptance.

TEST CIRCUIT
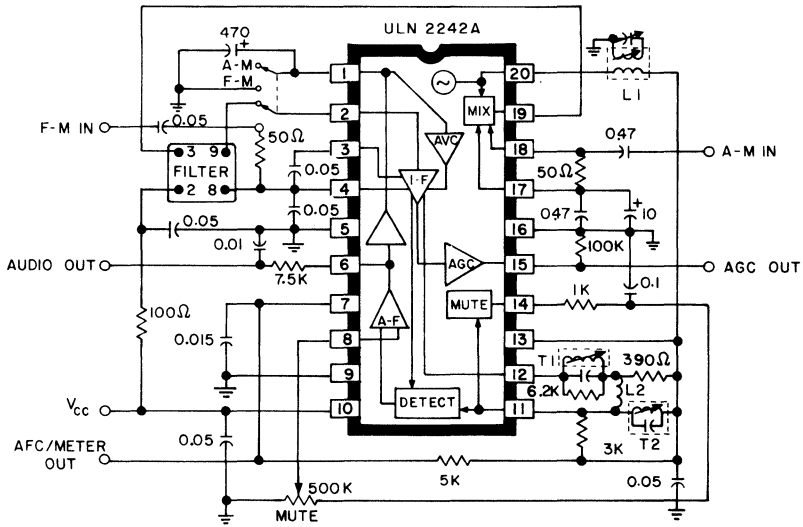
Dwg. No. A-10,427A

COIL WINDING INFORMATION

DWG. NO. A-10.428

T1	A-M I-F 455 kHz	Qu = 45 Ct = 1000 pF	General Instrument Part No. EX 27765	Toko Part No. RXN-6A6909HM
T2	F-M Detector 10.7 MHz	Qu = 60 Ct = 82 pF	General Instrument Part No. EX 27975	Toko Part No. TKAC-17044Z
L1	A-M Oscillator 1455 kHz	Qu = 50 N1:N2 = 11:1 Ct = 39 pF	General Instrument Part No. EX 27641	Toko Part No. RWO-6A7640BM
L2	F-M Detector 10.7 MHz	L = 18 μH Qu = 55		Coilcraft Type V

Filter Assembly:
Toko Part No. CFU455C-82BR
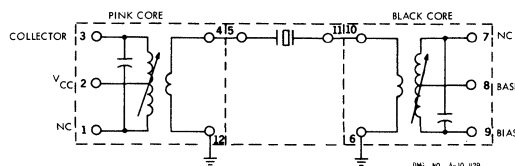
DWG. NO. A-10.429

A-M CHARACTERISTICS
AS FUNCTIONS OF INPUT VOLTAGE
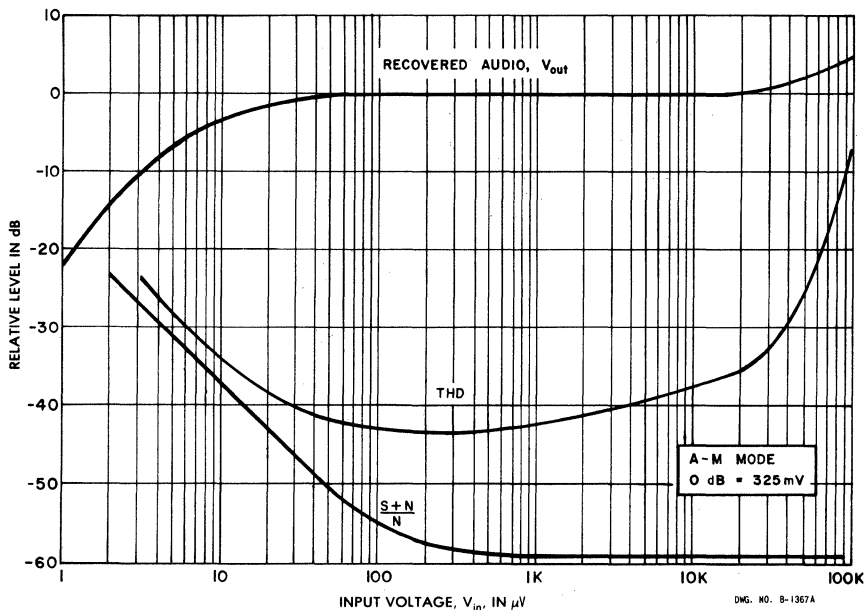
F-M CHARACTERISTICS
AS FUNCTIONS OF INPUT VOLTAGE
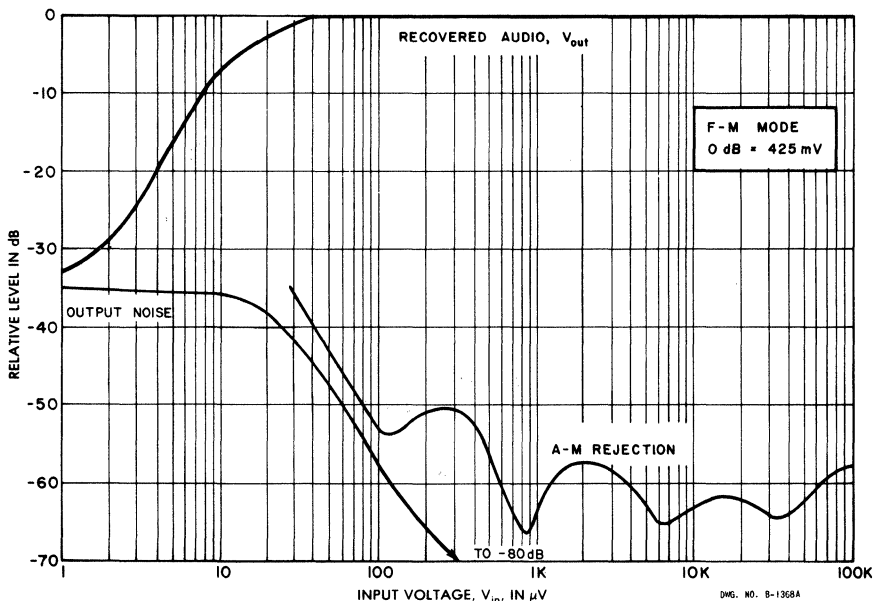
A-M CONTROL VOLTAGES
AS FUNCTIONS OF INPUT VOLTAGE

DWG. NO. B-1369

F-M CONTROL VOLTAGES
AS FUNCTIONS OF INPUT VOLTAGE

DWG. NO. B-1366

6

6—33
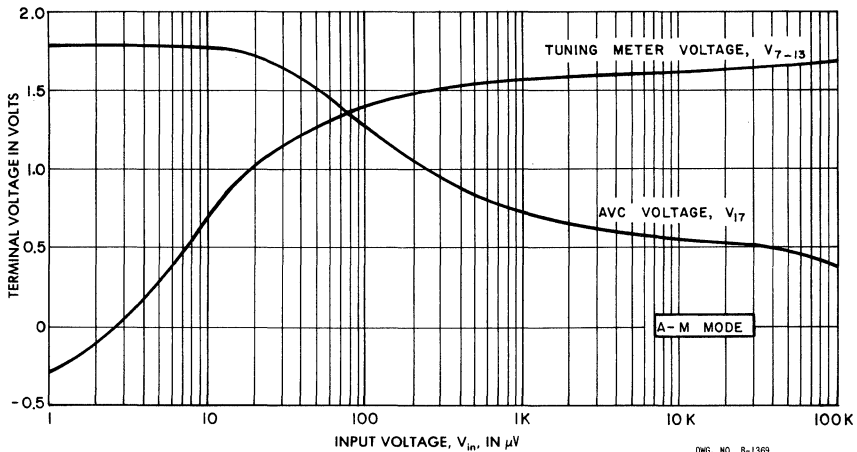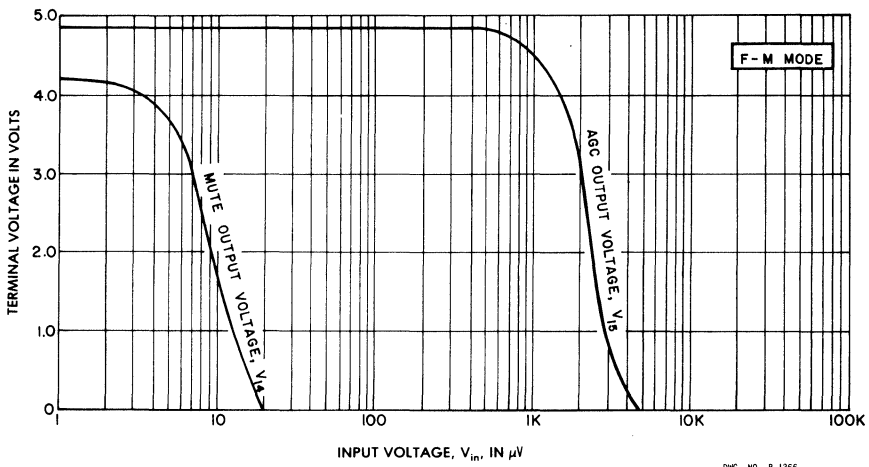
ULN-2243A

MIXER/I-F FOR F-M RADIO APPLICATIONS

FEATURES

- Doubly-Balanced Linear Mixer
- Very-High I-F Rejection
- 32 mmho (millisiemens) Conversion Gain at 100 MHz
- 330 Ω I-F Input/Output Impedance
- 46 dB I-F Gain at 10.7 MHz
- AGC Detector for MOSFET R-F Stage
- Low External Component Count
- 16-Pin Dual In-Line Plastic Package
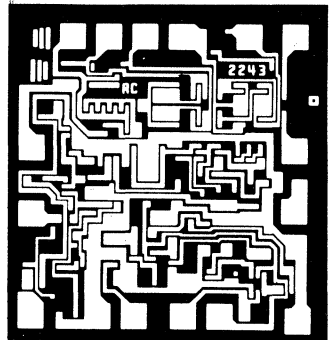
PROVIDING AN IMPORTANT basic building block for use in F-M radio applications, the ULN-2243A mixer/I-F minimizes spurious responses from strong off-channel signals while providing an excellent noise figure, maximum desired signal gain and very-high I-F rejection.

The linear fully-balanced mixer is an analog multiplier which will outperform discrete mixers. The low local oscillator and received frequency feed-through greatly reduces the outband rejection requirements.

I-F gain is furnished by a 2-stage amplifier with the gain set at typically 46 dB. Input and output impedances are 330Ω to allow the use of inexpensive ceramic filter coupling.

Both bias and AGC voltages, for use with a dual-gate MOSFET R-F stage, are provided by the wide-band AGC detector. An inhibit connection (pin 14) allows for maximum wide-band R-F gain up to the signal level at which the AGC action of the following narrow-band I-F amplifier/limiter and detector (ULN-3840A or ULN-3889A) starts operating. For strong on-channel signal levels, the wide-band R-F gain is determined by the strongest in-band signal.
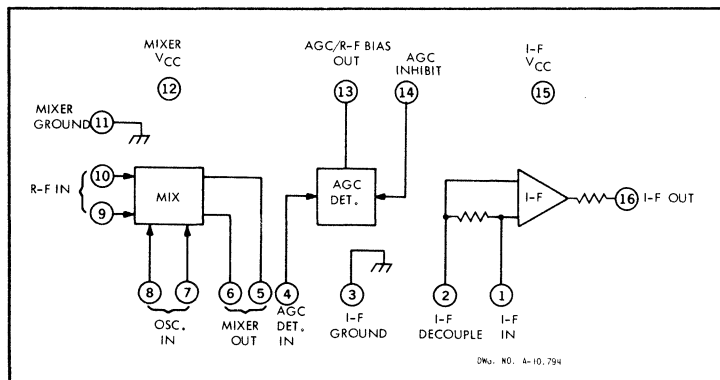
FUNCTIONAL BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Fig.	Test Pin	Test Conditions	Min.	Typ.	Max.	Units
Quiescent Supply Current	I_{CC}		5 + 6	$V_{CC} = +12$ V	5.0	—	11	mA
			12 + 15	$V_{CC} = +8$ V	18	—	38	mA
MIXER: $f_{in} = 100$ MHz, $V_{osc} = 200$ mV, $f_{osc} = 110.7$ MHz, $f_{out} = 10.7$ MHz								
Input Impedance	Z_{in}	1	9 or 10	$V_{in} = 25$ mV	—	525	—	Ω
Input Capacitance	C_{in}	1	9 or 10	$V_{in} = 25$ mV	—	9.0	—	pF
Osc. Impedance	Z_{osc}	1	7 or 8	$V_{in} = 0$	—	170	—	Ω
Osc. Capacitance	C_{osc}	1	7 or 8	$V_{in} = 0$	—	10	—	pF
Output Impedance	Z_{out}	2	5 or 6	$V_{in} = 0$	—	120	—	kΩ
Output Capacitance	C_{out}	2	5 or 6	$V_{in} = 0$	—	3.2	—	pF
Conversion Gain	g_m	3		$V_{in} = 1.0$ mV	—	32	—	mmho
I-F AMPLIFIER: $V_{in} = 100$ μV, $f_{in} = 10.7$ MHz								
Input Resistance	R_{IN}		1		—	330	—	Ω
Output Resistance	R_{OUT}		16		—	280	—	Ω
I-F Gain	A_e		16		—	46	—	dB
AGC DETECTOR: $f_{in} = 10.7$ MHz, $V_{in} = $ Pin 4, $V_{IN} = $ Pin 14								
Detector Threshold	V_{in}		4	$V_{IN} = 3.5$ V	—	150	—	mV
Inhibit Threshold	V_{IN}		14	$V_{in} = 350$ mV, $V_{OUT} = 2.0$ V	0.8	—	2.0	V
Quiescent Output Voltage	V_{OUT}		13	$V_{in} = 0$ and/or $V_{IN} = 0$	—	7.7	—	V
Output Voltage	V_{OUT}		13	$V_{in} = 350$ mV, $V_{IN} = 3.5$ V	—	0.7	—	V

Figure 1

Figure 2

Figure 3

APPLICATION INFORMATION

The ULN-2243A mixer/I-F performs a variety of functions especially suitable for automobile radios and other receivers required to handle an extremely wide range of input signal levels. It has been designed to use some of the inherent advantages of an integrated circuit to improve F-M front en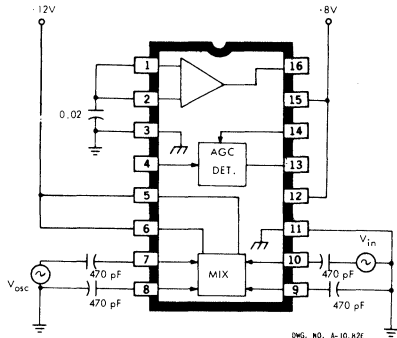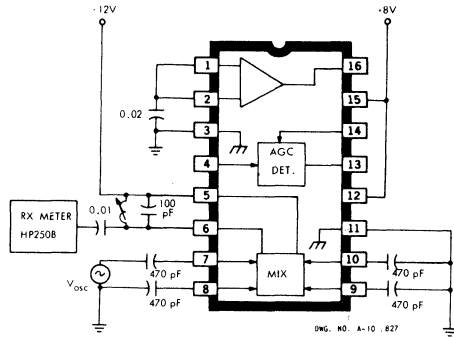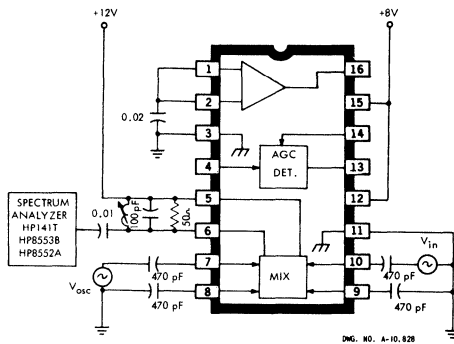d designs instead of simply attempting to replace discrete devices with integrated ones. This allows the tuner designer to select an R-F amplifier and oscillator circuit best-suited to the particular application.

The double-balanced mixer is internally biased so that all inputs can be capacitively coupled. This mixer possesses several advantages over discrete devices:

1. High inherent I-F rejection,
2. Good I-F/2 rejection,
3. Less oscillator drive required than with FET mixers,
4. Low oscillator feed through,
5. Less oscillator modulation with large signals, and
6. Balanced inputs eliminate ground loops which can cause stray coupling paths in discrete mixers.

Note that the oscillator input can be to either pin 7 or pin 8, the R-F input to either pin 9 or pin 10, to suit the circuit board layout.

The I-F transformer used with the ULN-2243A has been made to utilize both outputs of the mixer and was wound on a bobbin type coil form (Toko Type 10EZ) to maintain close couplings between windings. This eliminates the high cost of a bifilar-wound transformer. A conventional tuner with two R-F tuned circuits will typically have an I-F/2 rejection of at least 100 dB and a low noise figure. A single-ended output from either pin 5 or 6 could have been used (with degradation in rejection and noise figure) with the remaining output connected directly to V_{cc}.

The limiting amplifier has about 46 dB of gain at 10.7 MHz. The input and output impedances are 330 Ω for easy ceramic filter connection. The differential input again avoids the low-impedance ground loops associated with discrete common emitter I-F input stages. This makes the construction of a stable amplifier much easier. Since the I-F amplifier is an independent element, various combinations of filters before and after the amplifier are possible.

The relatively high gain of the ULN-2243A I-F amplifier allows the circuit designer to use surface wave or cascaded ceramic filters between it and the amplifier/detector integrated circuit. The resistive matching pad between ceramic filter elements prevents interactions which can cause undesirable group delay variations.

The AGC detector between pins 4, 13, and 14 has some unique properties which can be used in different ways. If the R-F amplifier is a dual-gate MOSFET (Figure 4), only the minimum in external discrete components is required.

The AGC detector input (pin 4) is connected through a small coupling capacitor to the mixer output. Internally is an R-F peak detector and d-c amplifier. If the AGC inhibit voltage (pin 14) is greater than approximately 1 volt, the AGC output voltage (pin 13) will change from typically 7.7 V with no applied signal to 0.5 V if an R-F signal of more than 150 mV is present at the input. This allows the tuner designer several design possibilities:

1. Connecting the AGC inhibit to the meter drive output of the limiter/detector (pin 15, ULN-3840A), the R-F stage will be AGC'd when tuned to a strong signal or when tuned to a weak signal with a strong adjacent channel signal, or
2. Pin 14 can be connected to a fixed bias voltage (typically +5 V). The R-F stage would then be AGC'd by any signal falling within the mixer coil bandpass, or
3. Combinations of fixed bias and signal-dependent levels (AFC, deviation mute, or delayed AGC) will then allow almost an unlimited number of AGC possibilities.

The AGC characteristics of the ULN-2243A mixer/I-F can be used with many other types of R-F amplifier. By adding a discrete transistor amplifier at pin 13, the AGC signal can be inverted and/or amplified to drive a bipolar R-F stage into forward AGC or to drive a PIN diode attenuator. A simplified graphical illustration of the most common AGC characteristic is shown in Figure 5.

A typical application of the ULN-2243A mixer/I-F in an F-M tuner was shown in Figure 4. Note that an output from the high-frequency oscillator has been provided with no increase in cost. This is one advantage to having the oscillator external to the integrated circuit. Also, by not including the R-F amplifier within the device, a wide variety of R-F amplifiers can be used depending on the wishes of the designer or the particular constraints of the application.
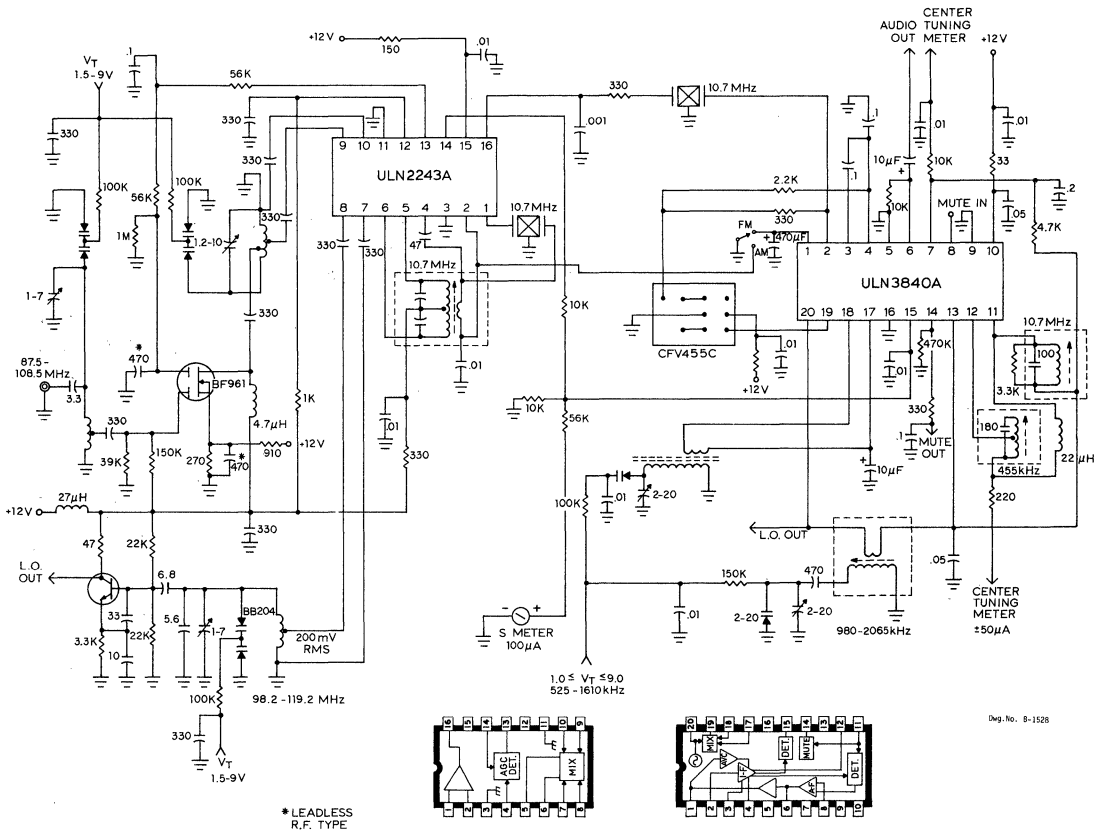
Figure 4
TYPICAL APPLICATION
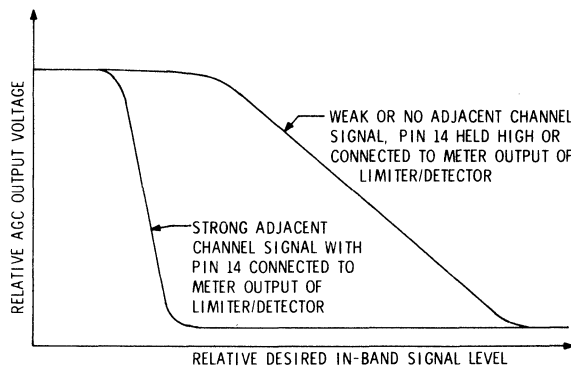
Figure 5
AGC CHARACTERISTICS

ULN-2249A A-M RADIO SYSTEM

FOR AUTOMOTIVE APPLICATIONS

FEATURES

- Low External Parts Count
- Internal Bias Regulator
- High AGC Ratio
- Low Distortion
- Good Sensitivity
- Direct Replacement for HA1199
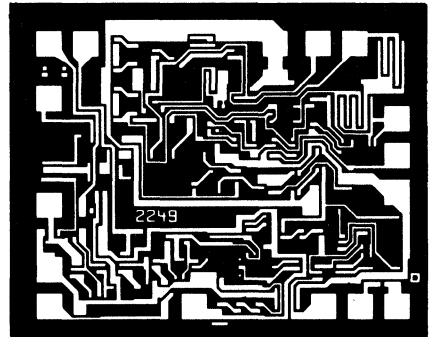
S PECIFICALLY DESIGNED for automotive A-M radio applications, the ULN-2249A A-M radio system consists of an R-F amplifier, converter, I-F amplifier, A-M detector, AGC amplifier, and bias voltage regulator. The low-level audio output can be used to drive a standard audio power amplifier, such as the Sprague Type ULN-3701Z.

Of particular significance in automotive applications is the ability of this integrated circuit to perform satisfactorily under wide variations in signal level. A typical AGC ratio of 63 dB, a usable sensitivity of approximately 8 μV, and an overload point in excess of 3 V, all contribute to the excellent performance of these devices under real conditions. Moreover, the ULN-2249A A-M radio system is rated for operation over the broad supply voltage range of 10.8 V to 15.6 V although the self-contained local oscillator will continue to function at much lower voltages.

FUNCTIONAL BLOCK DIAGRAM

DWG. NO. A-10.440
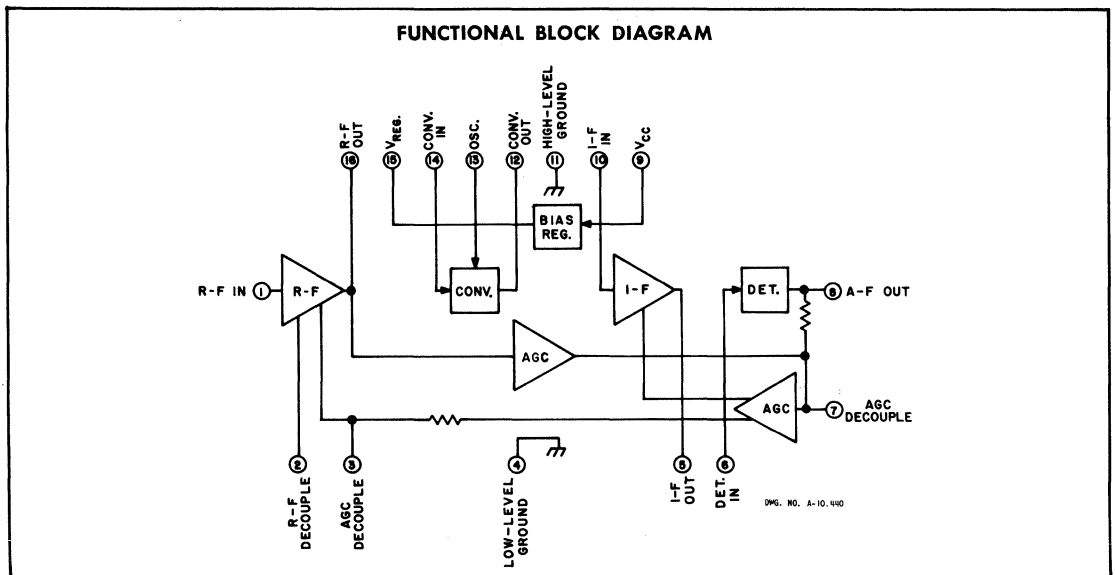
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 18 V
Package Power Dissipation, P_D . . . . 670 mW*
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

*Derate at the rate of 8.3 mW/°C above T_A = +70°C.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 13.5 V, f_o = 1 MHz, f_{if} = 262.5 kHz, f_m = 400 Hz, 30% A-M, Figure 2 (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Quiescent Supply Current	I_{CC}	Figure 1	—	15	—	mA
Sensitivity	V_{in}	V_{out} = 20 mV	—	3.0	6.0	μV
Detector Output Voltage	V_8	V_{in} = 5.0 mV	50	—	—	mV
Output Distortion	THD	V_{in} = 500 mV	—	0.4	5.0	%
Signal-to-Noise Ratio	S+N/N	V_{in} = 50 μV	26	30	—	dB
AGC Ratio*		V_{in} = 20 mV	60	63	—	dB

*AGC Ratio is defined as the ratio of the input voltages for a reduction in output voltage of 10 dB with the high level input as specified.

SMALL-SIGNAL A-C CHARACTERISTICS at T_A = +25°C, V_{CC} = 13.5 V, f_o = 1 MHz, f_{if} = 262.5 kHz, f_m = 400 Hz, 30% A-M, V_{in} ≤ 27 mVrms

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
R-F Input Impedance	Z_1	Also, see note	—	6.0	—	kΩ
R-F Output Impedance	Z_{16}		—	100	—	kΩ
R-F Transconductance	g_m		—	16	—	mmho
Conv. Input Impedance	Z_{14}		—	12	—	kΩ
Osc. Input Impedance	Z_{13}	f_{osc} = 1.262 MHz	—	3.6	—	kΩ
Conv. Output Impedance	Z_{12}		—	100	—	kΩ
Conv. Transconductance	g_m	Pin 14-12, V_{13} = 300 mVrms	—	0.2	—	mmho
		Pin 13-12, V_{13} ≤ 27 mVrms	—	1.4	—	mmho
Osc. Input Voltage	V_{13}	For optimum conv. performance	300	—	—	mVrms
I-F Input Impedance	Z_{10}		—	2.8	—	kΩ
I-F Output Impedance	Z_5		—	50	—	Ω
I-F Gain	Ae		—	24	—	dB
Det. Input Impedance	Z_6		—	310	—	Ω
Det. Output Impedance	Z_8		—	100	—	Ω
Det. Gain	Ae		—	25	—	dB

NOTE: For optimum noise match, source impedance should be 1.2 kΩ.

6

TEST CIRCUITS

FIGURE 1

DWG. NO. A-10.439

DWG. NO. A-10.441B

FIGURE 2

COIL WINDING INFORMATION

DWG. NO. A-10.442

T1 First I-F	$Q_{up} = 80$, $Q_{us} = 75$	Toko Part No.
262.5 kHz	Nt:Np:Ns = 13:2.3:1	B124FCS-1013PYG/
	Ct = 150 pF	B124FCS-1014STB
T2 Second I-F	$Q_{up} = 80$, $Q_{us} = 75$	Toko Part No.
262.5 kHz	Nt:Np:Ns = 13:5.6:1	B124FCS-60001PYG/
	Ct = 150 pF	B124FCS-1014STB

RECOVERED AUDIO, NOISE, AND DISTORTION
AS FUNCTIONS OF SIGNAL INPUT
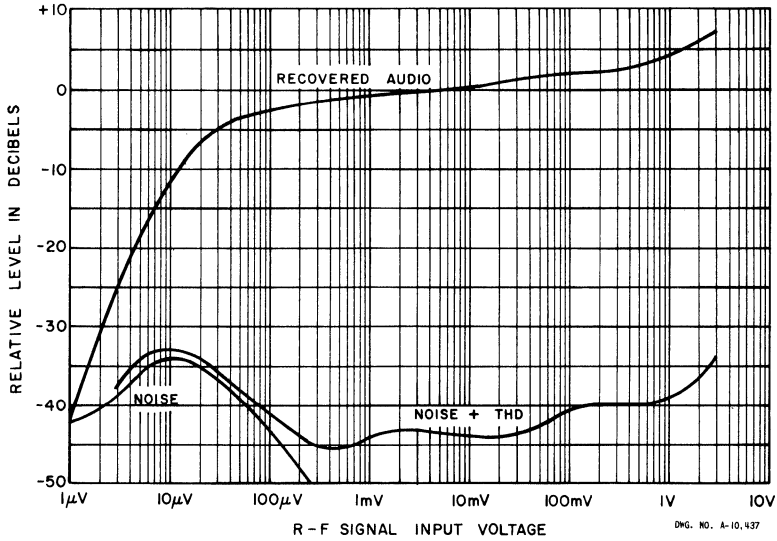
OUTPUT VOLTAGE
AS A FUNCTION OF INTERFERENCE FREQUENCY
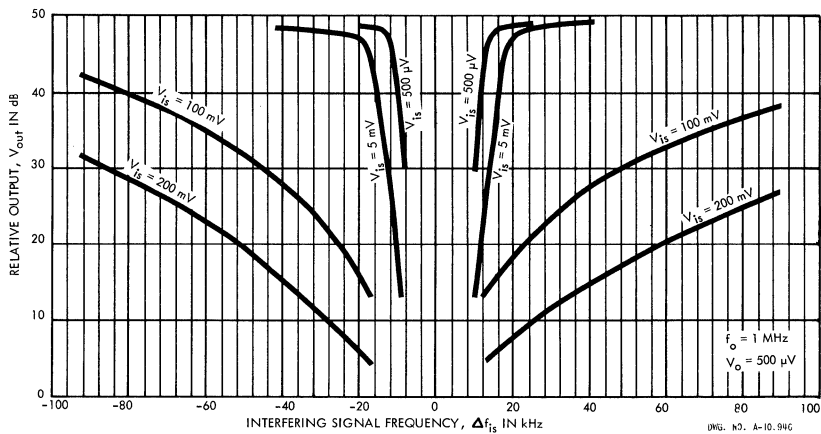
ULN-3804A

A-M/F-M SIGNAL PROCESSOR

FEATURES

- Good Sensitivity
- Low Harmonic Distortion
- Wide Operating Voltage Range
- Excellent A-M Rejection
- Low Power Drain
- D-C A-M/F-M Switching
- 30 μV Limiting Threshold
- 16-Pin Dual In-Line Plastic Package
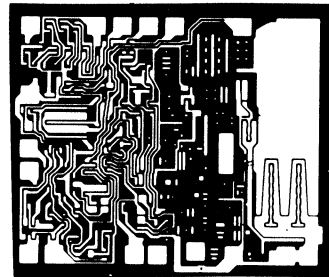
D ESIGNED for use in battery-powered portable radios or line-driven table radios. Type ULN-3804A works well in low-cost applications requiring high performance with few external parts. An entire A-M/F-M stereo receiver can be built with a Type ULN-3804A, a Type ULN-3809A stereo decoder, and two Type ULN-2283B audio amplifiers, for operation over a supply range of 4.5 to 12 V.

The signal processor includes the A-M oscillator and mixer and the A-M/F-M I-F amplifier and detector from the popular radio system, Sprague Type ULN-2204A. Radio designs using Type ULN-2204A can be revised for greater power output or for stereo operation (without reworking the printed wiring board layout) by replacement of Type ULN-2204A with Type ULN-3804A and addition of appropriate stereo decoders and audio power amplifiers.

In the A-M mode of operation, Type ULN-3804A provides all high-frequency circuitry, including AGC and envelope peak detection, for a single-conversion superheterodyne broadcast or shortwave receiver. In the F-M mode, the signal processor operates as a high-gain amplifier/limiter and phase-shift detector. A d-c switch is used to change modes.

A single external capacitor at pin 16 provides the A-M AGC time constant, the F-M AFC time constant, and R-F decoupling.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 16 V
Package Power Dissipation, P_D . . . . 640 mW*
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −65°C to +150°C
*Derate at the rate of 8.0 mW/°C above T_A = +70°C.

FUNCTIONAL BLOCK DIAGRAM

Dwg. No. A-11,068
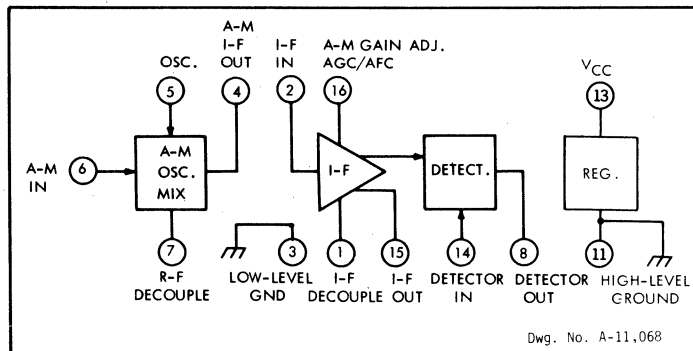
ELECTRICAL CHARACTERISTICS at $T_A = +25°C$
$V_{cc} = 6.0\,V$, $R_8 = \infty$, $R_{16} = 1.2\,k\Omega$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
F-M MODE: $f_0 = 10.7$ MHz, $f_m = 400$ Hz, $f_d = \pm 75$ kHz, Peak Separation $= 550$ kHz						
Input Limiting Threshold	V_{th}		—	30	60	μV
Detector Recovered Audio	V_o		—	250	—	mV
Detector Output Distortion	THD	$V_{in} = 10$ mV$_{rms}$	—	1.0	—	%
A-M Rejection	AMR	$V_{in} = 10$ mV$_{rms}$, 30% A-M, $f_{am} = 400$ Hz	35	50	—	dB
I-F Input Impedance	Z_2		—	40	—	$k\Omega$
I-F Input Capacitance	C_2		—	4.0	—	pF
Quiescent Terminal Voltage	V_1		—	2.1	—	V
	V_8		—	1.7	—	V
Quiescent Supply Current	I_{cc}		—	10	15	mA
A-M MODE: $f_0 = 1$ MHz, $f_{if} = 455$ kHz, $f_m = 400$ Hz, 30% A-M						
Sensitivity		Maximum Volume	—	5.0	10	μV
Detector Recovered Audio	V_o		—	150	—	mV
Overload Distortion		80% A-M	—	10	—	mV
Usable Sensitivity			—	25	35	μV
Mixer Input Impedence	Z_6	See Note	—	4.5	—	$k\Omega$
Mixer Input Capacitance	C_6		—	5.5	—	pF
Mixer Output Impedance	Z_4		—	25	—	$k\Omega$
Mixer Output Capacitance	C_4		—	3.0	—	pF
I-F Input Impedance	Z_2		—	100	—	$k\Omega$
I-F Input Capacitance	C_2		—	3.0	—	pF
Quiescent Terminal Voltage	V_1		—	1.3	—	V
	V_8		—	1.7	—	V
Quiescent Supply Current	I_{cc}		—	3.8	—	mA

NOTE: For optimum noise match, source impedance should be 2.5 kΩ.

6

TEST CIRCUIT

DWG. NO. A-11,067A

COIL WINDING INFORMATION

DWG. NO. A-10,330

T1 A-M First I-F 455 kHz	Qu = 120 N1:N2:N3 = 15.5:2.8:1 Ct = 180 pF	General Instrument Part No. EX 27835	Toko Park No. RMC-2A7641A
T2 A-M Second I-F 455 kHz	Qu = 70 N1:N2 = 2:1 Ct = 430 pF	General Instrument Part No. EX 27836	Toko Part No. RLE-4A7642G0
T3 F-M Detector 10.7 MHz	Qu = 50 Ct = 100 pF	General Instrument Part No. EX 27640	Toko Part No. BKAC-K3651HM
T4 F-M Detector 10.7 MHz	Qu = 50 Ct = 100 pF	General Instrument Part No. EX 27640	Toko Part No. BKAC-K3651HM
L1 A-M Oscillator 1455 kHz	Qu = 50 N1:N3 = 10.7:1 Ct = 39 pF	General Instrument Part No. EX 27641	Toko Part No. RWO-6A7640BM

Device Classification
and Design Considerations

The A-M/F-M receiver system's operation can be kept within tighter performance limits by matching bias groupings and appropriate external resistors (R8 and R16). With proper matching of parts and lots, consistent device performance can be obtained. The groupings, shown in the table below, are based on A-M and F-M operation. There are three selections for each mode and nine possible combinations:

PIN 16 OUTPUT VOLTAGE, V_{16}

A-M Operation	Complete Part Number Including Suffix		
	F-M Operation		
	2.20—2.65 V	2.55—3.05 V	2.95—3.40 V
1.40—1.75 V	ULN-3804A-11	ULN-3804A-21	ULN-3804A-31
1.65—2.00 V	ULN-3804A-12	ULN-3804A-22	ULN-3804A-32
1.90—2.25 V	ULN-3804A-13	ULN-3804A-23	ULN-3804A-33

6

Sprague recommends that customers not specify particular selections except in unusual circumstances. All parts manufactured with the Sprague part number will be marked with the complete number, including the appropriate suffix. In addition, any one shipment to a customer will consist of a single selection (single suffix).

The first digit of the suffix (such as the "3" in " – 31") applies to F-M performance. It indicates the F-M gain and pin 16 output voltage as functions of the pin 16 load resistance, as shown in the graph on the next page.

F-M circuit stability is inversely related to gain or sensitivity and is also affected by source and loan impedances, decoupling, and printed wiring board layout. After an optimal F-M I-F gain is determined for a particular circuit design, the gain can be controlled with proper matching of the suffix and the pin 16 load.

Design Considerations (Continued)

In addition, certain system designs derive the F-M tuner supply, tuner bias, or AFC voltage at pin 16 of Type ULN-3804A. As an example, if the tuner design requires 2.4 V at 2.0 mA (an equivalent R16 of 1200 Ω), Type ULN-3804A-1X is required. A $-2X$ or $-3X$ device can also be used by paralleling the equivalent 1200 Ω tuner load with a fixed resistor to present an 830 Ω load or a 520 Ω load.

For AFC applications, note that as the frequency is increased, the V_{16} voltage will decrease. The amount of change is a function of load impedance, detector coil characteristics, and part grouping.

TYPICAL F-M I-F GAIN CHARACTERISTICS

Dwg. No. A-11,458
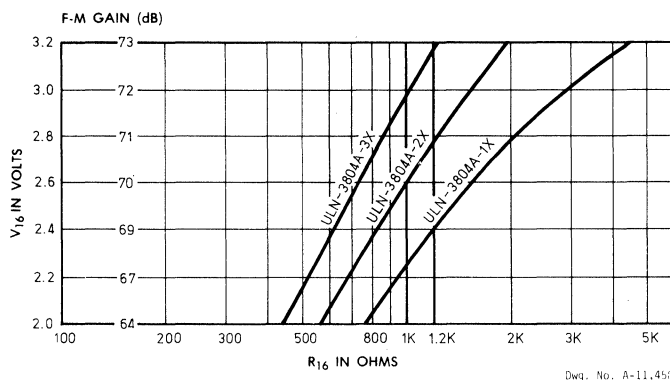
Stability is seldom a problem with A-M operation. However, large-signal overload can be held to typically 30 mV by matching the particular part group with an appropriate load resistor at pin 8. The A-M grouping is identified by the second digit of the part number suffix (such as the "2" in "-32").

> For $-X1$, R8 should be an open circuit;
> for $-X2$, R8 should be 47 kΩ;
> for $-X3$, R8 should be 33 kΩ.

Additional loading may raise the overload point slightly, but AGC and sensitivity will be compromised. For any fixed value of R8, the $-X3$ parts will exhibit slightly higher A-M gain, the $-X1$ parts slightly lower A-M gain.

ULN-3809A PHASE-LOCKED LOOP STEREO DECODER

FEATURES

- Unity Voltage Gain
- I^{2}L and Ion Implant Technology
- Wide Dynamic Range
- Low Distortion
- Excellent Channel Separation
- No Tuning Coils
- Automatic Stereo/Mono Switching
- Stereo Indicator Lamp Driver
- Direct Replacement for MC1309
- 14-Pin Dual In-Line Plastic Package
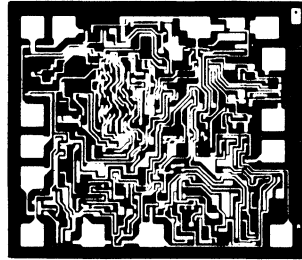
S PRAGUE Type ULN-3809A phase-locked loop decoder demodulates standard composite F-M stereo input signals within the range of 0.25 to 1.7 Vpp without the use of tuning coils.

Integrated circuit design allows tuning with a single resistive adjustment. The decoder automatically switches between stereo and monaural operation by detection and evaluation of the 19-kHz pilot carrier signal.

Type ULN-3809A exhibits 35 dB suppression of the 19-kHz pilot and 45 dB rejection of the regenerated 38-kHz subcarrier at demodulator output terminals. Stereo channel separation is typically 47 dB. With a composite input signal of 850 mV, total harmonic distortion for the unit is typically 0.06%.

Type ULN-3809A is designed to work within a range of supply voltages from 4.5 to 16 V.

6

FUNCTIONAL
BLOCK DIAGRAM

DWG. NO. A-9441B
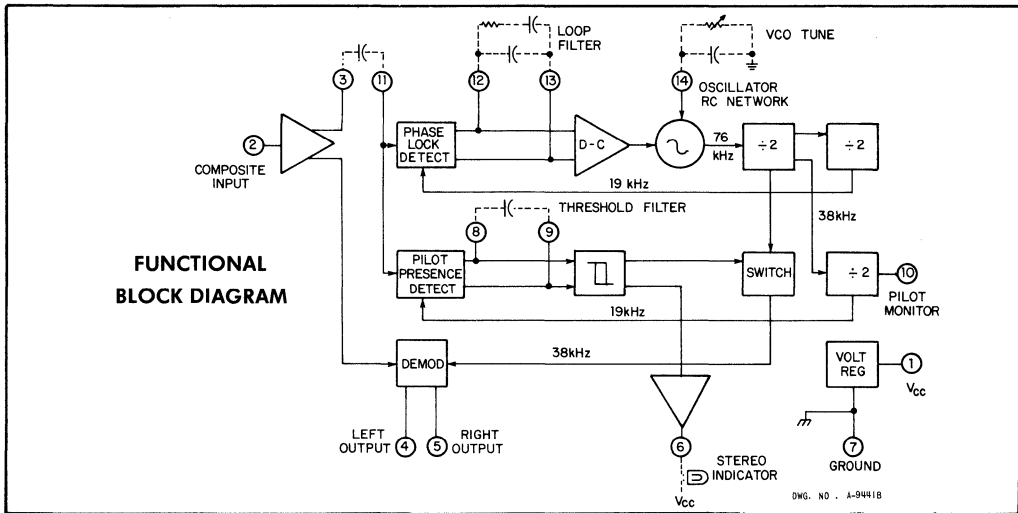
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 16 V
Nominal Lamp Current, I_{LAMP} . . . . 50 mA
Package Power Dissipation, P_D . . . . 670 mW*
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage, Temperature Range, T_S . . . . −65°C to +150°C

*Derate at the rate of 8.3 mW/C above T_A = +70°C.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 9.0 V, V_{in} = 1.7 Vpp, f_m = 1.0 kHz (L or R only), Pilot Level = 10% unless otherwise specified

Characteristic	Test Conditions	Limits			Units
		Min.	Typ.	Max.	
Max. Standard Composite Input Signal	V_{CC} = 6.0 V, 0.5% THD	0.85	1.7	—	Vpp
	V_{CC} = 9.0 V, 0.5% THD	1.7	2.1	—	Vpp
Max. Monaural Input Signal	V_{CC} = 6.0 V, 1.0% THD	0.85	1.7	—	Vpp
	V_{CC} = 9.0 V, 1.0% THD	1.7	2.2	—	Vpp
Input Impedance		15	30	—	kΩ
Stereo Channel Separation	f = 100 Hz	—	45	—	dB
	f = 1.0 kHz	30	47	—	dB
	f = 10 kHz	—	40	—	dB
Monaural Gain		0.6	0.9	—	V/V
Channel Balance		—	0	1.0	dB
Total Harmonic Distortion	Stereo, V_{in} = 850 mVpp	—	0.06	—	%
	Mono, V_{in} = 850 mVpp	—	0.08	—	%
Ultrasonic Frequency Rejection	19 kHz	—	35	—	dB
	38 kHz	—	45	—	dB
SCA Rejection		—	75	—	dB
Stereo Switch Level	Lamp ON	—	9.0	12	mV
	Lamp OFF	2.0	4.5	—	mV
Mono/Stereo Switch Transient	No Lamp	—	0	—	mV
Capture Range	Pilot = 60 mVrms	—	7.0	—	%
Supply Current		—	11	—	mA

NOTE: THD and channel separation are measured after a bandpass filter (200 Hz to 10 kHz).

APPLICATIONS INFORMATION

Dwg. No. A-11,460

TEST CIRCUIT AND TYPICAL APPLICATION

1. If relaxed performance is acceptable, the external circuit can be simplified by decreasing the value of C_1 (reduces separation at low frequencies), decreasing the values of C_4 and R_3 while eliminat-

ing C_5, and decreasing the value of C_6 while increasing the values of R_4 and R_5 (increases capture-range and beat-note distortion).

2. Typical I-F amplifier frequency response restricts channel separation to about 32 dB. This restriction can be counteracted by the network shown below. Exact circuit values will be determined by the I-F amplifier design.

DWG. NO. A-10.656

3. To manually disable the stereo decoder, ground pin 8 and connect pin 14 to ground through a resistance of 3.3 kΩ.

4. Capacitor C_6 should be temperature-stable (NPO).

MINIMUM-COST APPLICATION

IN A-M/F-M STEREO RADIO

Dwg. No. A-1457A
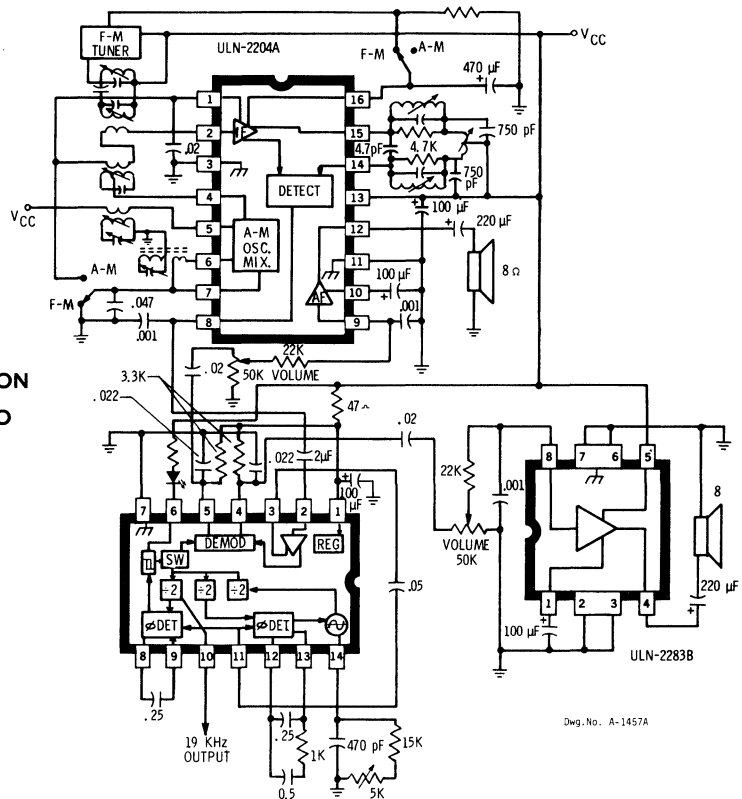
ULN-3810A
PHASE-LOCKED LOOP STEREO DECODER

FEATURES

- No Tuning Coils Required
- I^2L and Ion Implant Technology
- Single-Adjustment Tuning
- Automatic Stereo/Mono Switching
- Stereo Indicator Lamp Driver
- Excellent SCA Rejection
- Direct Replacement for TA7157, KB4409, CA1310, XR1310, LM1310, SN76115, MC1310 & ULN-2110A
- 14-Pin Dual In-Line Plastic Package
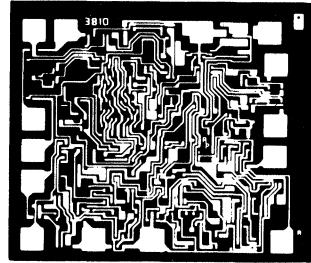
R ECOVERY of left- and right-channel audio from the standard F-M composite signal by this phase-locked loop decoder yields stereo channel separation of 40 dB and total harmonic distortion of less than 0.3%.

Type ULN-3810A is designed to operate over a supply voltage range of 6 to 16 V.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 16 V
Nominal Lamp Current, I_{LAMP} .... 75 mA
Package Power Dissipation, P_D .... 670 mW*
Operating Temperature Range, T_A .... $-20°C$ to $+85°C$
Storage, Temperature Range, T_S .... $-65°C$ to $+150°C$

*Derate at the rate of 8.3 mW/C above $T_A = +70°C$.

FUNCTIONAL BLOCK DIAGRAM

DWG. NO. A-9441B
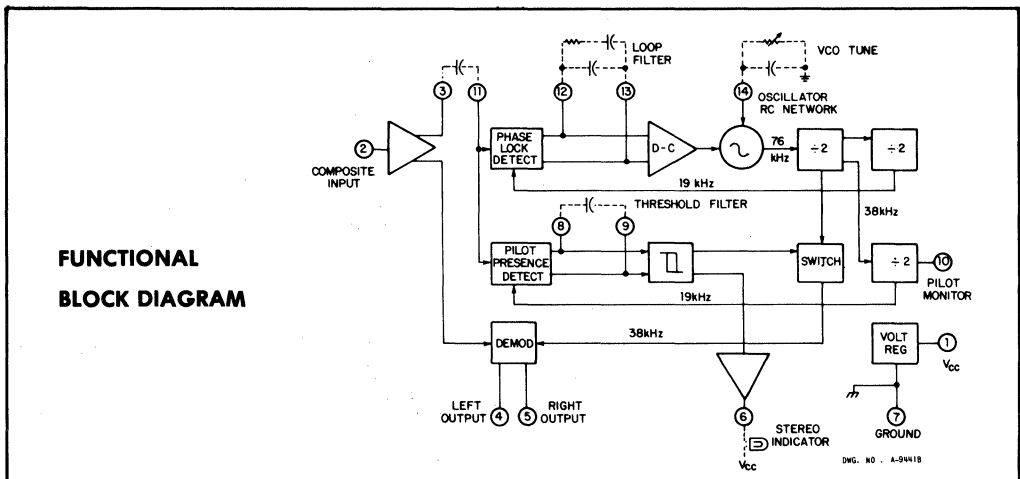
ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = +12V$, $V_{in} = 560mVrms$ (2.8V_{pp}), $f_m = 1.0$ kHz (L or R only), Pilot Level = 100 mVrms (10%) unless otherwise specified

Characteristic	Test Conditions	Min.	Typ.	Max.	Units
			Limits		
Max. Standard Composite Input Signal	THD = 0.5%	2.8	—	—	V_{pp}
Max. Monaural Input Signal	THD = 1.0%	2.8	—	—	V_{pp}
Input Impedance	Pin 2	20	25	—	kΩ
Stereo Channel Separation		30	40	—	dB
Audio Output Voltage	Desired Channel	—	485	—	mVrms
Monaural Channel Balance	Pilot Level = 0 V	—	—	1.5	dB
Total Harmonic Distortion		—	<0.3	—	%
Ultrasonic Freqency	19 kHz	—	34.4	—	dB
Rejection	38 kHz	—	45	—	dB
SCA Rejection	67 kHz, No Modulation, Measure 9 kHz Beat	—	75	—	dB
Stereo Switch Level	Pilot Only, Lamp ON	—	18	25	mVrms
	Pilot Only, Lamp OFF	5.0	9.0	—	mVrms
Capture Range	Permissible Tuning Error	—	3.5	—	%
Supply Current	Lamp OFF	—	12	22	mA

6

APPLICATION INFORMATION

DWG. NO. A-9442C

TEST CIRCUIT AND TYPICAL APPLICATION

1. If relaxed performance is acceptable, the external circuit can be simplified by decreasing the value of C_1 (reduces separation at low frequencies), decreasing the values of C_4 and R_3 while eliminating C_5, and decreasing the value of C_6 while increasing the values of R_4 and R_5 (increases capture-range and beat-note distortion).

2. Typical I-F amplifier frequency response restricts channel separation to about 32 dB. This restriction can be counteracted by the network shown below. Exact circuit values will be determined by the I-F amplifier design.


DWG. NO. A-10.656

3. To manually disable the stereo decoder, ground pin 8 and connect pin 14 to ground through a resistance of 3.3 kΩ.

4. Capacitor C_6 should be temperature stable (NPO).

ULN-3812A PHASE-LOCKED LOOP STEREO DECODER

FEATURES

- Internal Temperature Compensation
- Single-Adjustment Tuning
- Automatic Stereo/Mono Switching
- Stereo Indicator Lamp Driver
- 70 dB SCA Rejection
- Operating Voltage — 9 to 16 V
- Low Harmonic Distortion
- Replaces ULN-2245A, CA3145, ULN-2244A, μA758, LM1800, and MC1311
- 16-Pin Dual In-Line Plastic Package
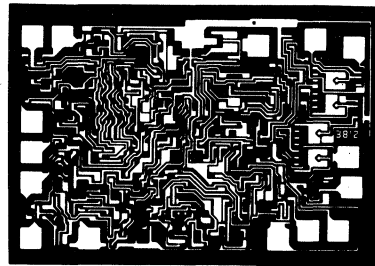
R EQUIRING only a single, non-critical resistive tuning adjustment, the Type ULN-3812A integrated circuit derives left and right audio channels from the standard composite stereo signal. This phase-locked loop stereo decoder can also be used in a number of subscription TV decoder schemes or in various proposed TV stereo systems.

Using phase-lock techniques, the subcarrier (38 kHz for F-M stereo) is regenerated in phase with and at exactly twice the frequency of the transmitted pilot signal. Switching between monaural and stereo op-

eration is accomplished automatically by the presence of the pilot signal.

Low-impedance emitter-follower outputs and an internal voltage regulator for increased stability make Type ULN-3812A suitable for both line-operated and automotive applications. It is designed to operate over a wide supply-voltage range and will function with supplies as low as 9 V.

Type ULN-3812A is functionally and pin compatible with the Type ULN-2245A decoder and, except for a reduced audio-output impedance, is also interchangeable with Type ULN-2244A.

FUNCTIONAL BLOCK DIAGRAM

Dwg. No. A-9085E
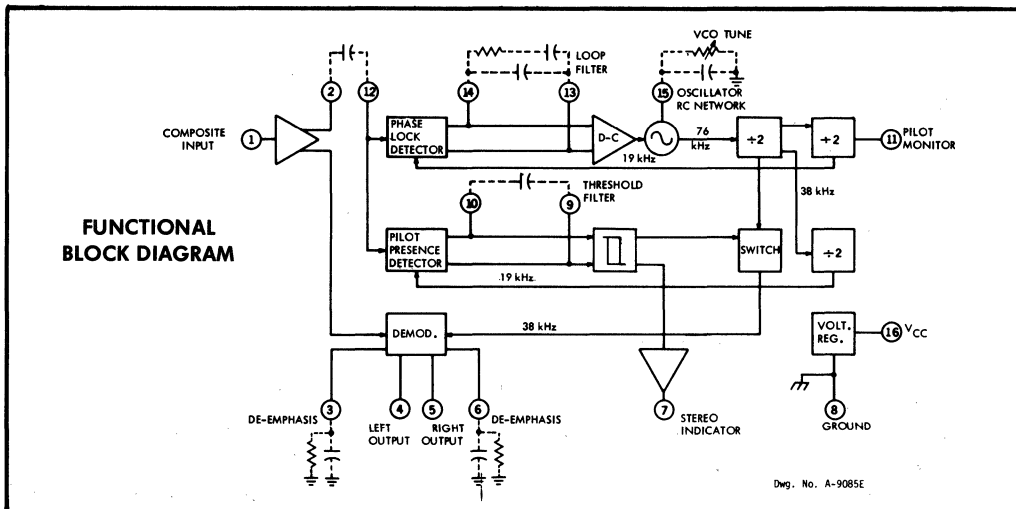
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} (Continuous) .... +16 V

(<15s) .... +22 V

Lamp Supply Voltage, V_{LAMP} .... +22 V

Lamp Current, I_{LAMP} .... 150 mA

Output Current, I_4 or I_5 .... 10 mA

Package Power Dissipation, P_D .... 670 mW*

Operating Temperature Range, T_A .... −20°C to +85°C

Storage Temperature Range, T_S .... −65°C to +150°C

*Derate at the rate of 8.3 mW/°C above $T_A = +70°C$.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = +12V$, Composite Input = 300 mV$_{rms}$ (L = R, Pilot OFF), Pilot Level = 30 mV$_{rms}$, f_m = 400 Hz or 1 kHz, unless otherwise specified.

Characteristic	Test Conditions	Min.	Typ.	Max.	Units	Notes
Input Impedance	Pin 2	20	35	—	kΩ	
Output Impedance	Pin 4 or 5	—	50	—	Ω	
Audio Voltage Gain	Desired Channel	0.7	1.0	1.4	V/V	
Stereo Channel Separation	f_m = 100 Hz	—	30	—	dB	
	f_m = 400 Hz	30	40	—	dB	3
	f_m = 10 kHz	—	30	—	dB	
Monaural Channel Balance	Pilot Level = 0 V	—	0.1	1.5	dB	
Total Harmonic Distortion	Multiplex Level = 600 mV	—	0.4	1.5	%	3
Ultrasonic Frequency Rejection	19 kHz	25	35	—	dB	
	38 kHz	25	40	—	dB	
SCA Rejection	67 kHz	—	70	—	dB	1
Stereo Switch Level	Pilot Only, Lamp ON	—	14	25	mVrms	
	Pilot Only, Lamp OFF	2.0	7.0	—	mVrms	
VCO Tuning Resistance	Pin 15	20	23	26	kΩ	2
VCO Frequency Drift	−20°C <T_A <+25°C	—	±0.5	±2.0	%	
	+25°C <T_A <+70°C	—	±0.5	±2.0	%	
Stereo Lamp Hysteresis	Lamp OFF to Lamp ON	3.0	6.0	—	dB	
Capture Range	Permissable Tuning Error	—	4.0	—	%	
Output Voltage Shift	Stereo to Mono Operation	—	±30	—	mV	
Lamp Output Current	Short Circuit, Lamp ON	50	100	—	mA	
	Lamp OFF	—	1.0	100	μA	
Lamp Driver Terminal Voltage	I_{LAMP} = 50 mA	—	1.3	2.0	V	
Supply Current	Lamp OFF	—	20	40	mA	
Power Supply Rejection	200 Hz, 200 mVrms	—	40	—	dB	

NOTES: 1. Measured with a stereo composite signal of 80% stereo, 10% pilot, and 10% SCA.
2. Total resistance from pin 15 to ground, to set reference frequency at pin 11 to 19 kHz ±10 Hz.
3. Measured with a Toko 208BLR-3152N filter, or equivalent.

APPLICATION INFORMATION
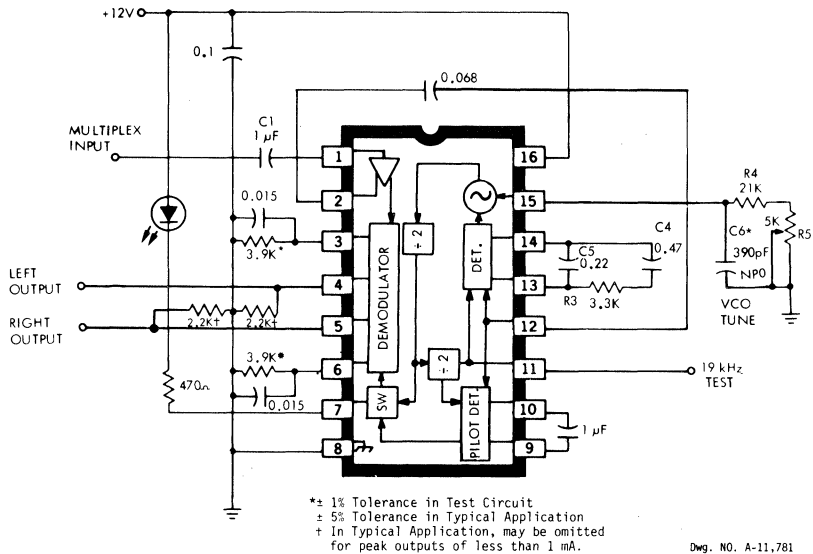
Dwg. NO. A-11,781

*± 1% Tolerance in Test Circuit
± 5% Tolerance in Typical Application
+ In Typical Application, may be omitted
for peak outputs of less than 1 mA.

TEST CIRCUIT AND TYPICAL APPLICATION

1. If relaxed performance is acceptable, the external circuit can be simplified by decreasing the value of C_1 (reduces separation at low frequencies), decreasing the values of C_4 and R_3 while eliminating C_5, and decreasing the value of C_6 while increasing the values of R_4 and R_5 (increases capture-range and beat-note distortion).

2. Typical I-F amplifier frequency response restricts channel separation to about 32 dB. This restriction can be countered by the network shown below. Exact circuit values will be determined by the I-F amplifier design.

3. The network at pin 15 should be temperature stable (NP0).

4. To manually disable the stereo decoder, ground pin 9 and connect pin 15 to ground through a resistance of 3.3 kΩ.
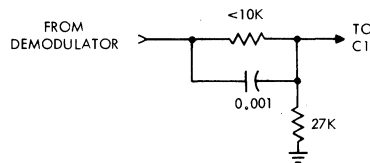
DWG. NO. A-10,656

ULN-3838A A-M RADIO SYSTEM

FEATURES

- 3, 6, or 9 V Operation
- Low Power Drain
- Low Harmonic Distortion
- 16-Pin Dual In-Line Plastic Package

OUTSTANDING for use in low-cost applications that require a minimum parts count and high performance, the Type ULN-3838A integrated circuit provides all standard A-M radio functions. It is a complete single-conversion superheterodyne broadcast or shortwave receiver with AGC and peak envelope detection.

Its ability to operate with a wide range of supply voltages makes the Type ULN-3838A receiver system suitable for use in battery-powered portable radios and in a-c table radios. This system will operate at supply voltages as low as 2 V at reduced volume without significant increase in distortion. Weak batteries need no longer be a major design concern.

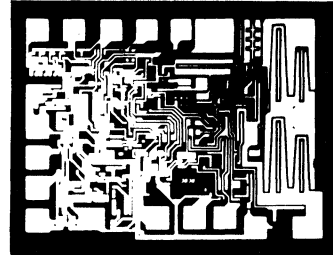A single external capacitor at pin 16 provides the AGC time constant and R-F decoupling. A single resistor at the same pin will adjust the A-M gain for optimum performance.

Class B operation of the audio power amplifier yields high efficiency at rated output power with very low quiescent current drain. The amplifier exhibits little crossover distortion. Its output impedance is significantly less than one ohm, allowing it to be used with a wide variety of speaker and headphone impedances.

Type ULN-3838A A-M radio system is supplied in a 16-pin dual in-line plastic package with a copper lead frame that eliminates many decoupling problems and gives the package an enhanced power dissipation rating.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 10 V
Package Power Dissipation, P_D (Note) .... 1.0 W
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −65°C to +150°C

NOTE: Derate at the rate of 15 mW/°C above T_A = +70°C.

6

FUNCTIONAL BLOCK DIAGRAM

Dwg. No. A-11,660
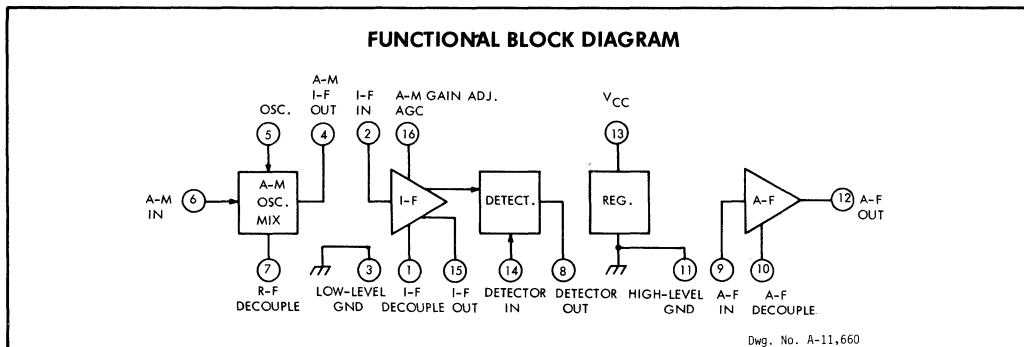
ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 6.0 V$, $R_8 = \infty$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
				Limits		
A-M MODE: f_o = 1 MHz, f_{if} = 455 kHz, f_m = 400 Hz, 30% A-M						
Sensitivity		$V_{OUT(8)}$ = 20 mV$_{rms}$	—	5.0	10	μV
Detector Recovered Audio	V_o		—	150	—	mV
Overload Distortion		80% A-M, also see "Optimizing System Performance"	—	10	—	mV
Usable Sensitivity		20 dB S+N/N	—	18	30	μV
Mixer Input Impedance	Z_6	See Note	—	4.5	—	kΩ
Mixer Input Capacitance	C_6		—	5.5	—	pF
Mixer Output Impedance	Z_4		—	25	—	kΩ
Mixer Output Capacitance	C_4		—	3.0	—	pF
I-F Input Impedance	Z_2		—	100	—	kΩ
I-F Input Capacitance	C_2		—	3.0	—	pF
Quiescent Terminal Voltage	V_1		—	1.3	—	V
	V_8		—	1.7	—	V
Quiescent Supply Current	I_{CC}	V_{CC} = 3.0 V	—	8.0	—	mA
		V_{CC} = 6.0 V	—	10	17	mA
		V_{CC} = 9.0 V	—	13	—	mA
AUDIO AMPLIFIER: f_o = 400 Hz, R_L = 8Ω						
Audio Gain	A_e		36	40	44	dB
Output Power	P_o	V_{CC} = 3.0 V, 10% THD	—	50	—	mW
		V_{CC} = 6.0 V, 10% THD	250	350	—	mW
		V_{CC} = 9.0 V, 10% THD	500	650	—	mW
Output Distortion	THD	P_o = 50 mW	—	2.0	—	%
A-F Input Impedance	Z_9		—	250	—	kΩ
Quiescent Terminal Voltage	V_{10}		—	1.1	—	V
	V_{12}		—	2.6	—	V

NOTE: For optimum noise match, source impedance should be 2.5 kΩ.

Device Classification and Design Considerations

Type ULN-3838A integrated circuits are sorted into three groups defined by the pin 16 voltage in the following test circuit. Applications information for this grouping is given in the text entitled "Optimizing System Performance."

V_{16}	Complete Part Number
1.40 - 1.75 V	ULN-3838A-1
1.65 - 2.00 V	ULN-3838A-2
1.90 - 2.25 V	ULN-3838A-3

TEST CIRCUIT
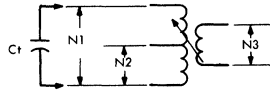
Dwg. No. A-11,521

*See "Optimizing System Performance."

COIL WINDING INFORMATION

DWG. NO. A-10.330

T1 A-M First I-F 455 kHz	Qu = 120 N1:N2:N3 = 15.5:2.8:1 Ct = 180 pF	General Instrument Part No. EX 27835	Toko Part No. RMC-2A7641A
T2 A-M Second I-F 455 kHz	Qu = 70 N1:N2 = 2:1 Ct = 430 pF	General Instrument Part No. EX 27836	Toko Part No. RLE-4A7642G0
L1 A-M Oscillator 1455 kHz	Qu = 50 N1:N3 = 10.7:1 Ct = 39 pF	General Instrument Part No. EX 27641	Toko Part No. RWO-6A7640BM

OPTIMIZING SYSTEM PERFORMANCE

Type ULN-3838A receiver system's performance can be kept within tighter limits by matching the bias group with an appropriate external resistor (R8). With proper matching, consistent device performance between parts and lots can be obtained. The bias groups, shown in the table are based on A-M operation; three selections are possible.

V_{16}	Complete Part Number
1.40 - 1.75 V	ULN-3838A-1
1.65 - 2.00 V	ULN-3838A-2
1.90 - 2.25 V	ULN-3838A-3

Sprague recommends that customers not specify particular selections except in unusual circumstances. All parts manufactured with Sprague part number marking will be branded with the appropriate suffix. Any one customer shipment will consist of a single selection (single suffix).

In A-M operation, large-signal overload can be optimized (to typically 30 mV) by matching the particular part group with an appropriate load resistor at pin 8. The group is identified by the part number suffix (ULN-3838A-1).

For -1, R8 should be ∞;
for -2, R8 should be 47 kΩ;
for -3, R8 should be 33 kΩ.

Additional loading may raise the overload point slightly, but AGC and sensitivity will be compromised. For any fixed value of R8, the -3 parts will exhibit slightly higher A-M gain, while the -1 parts will have slightly lower A-M gain.

**TYPICAL QUIESCENT SUPPLY CURRENT
AS A FUNCTION OF SUPPLY VOLTAGE**
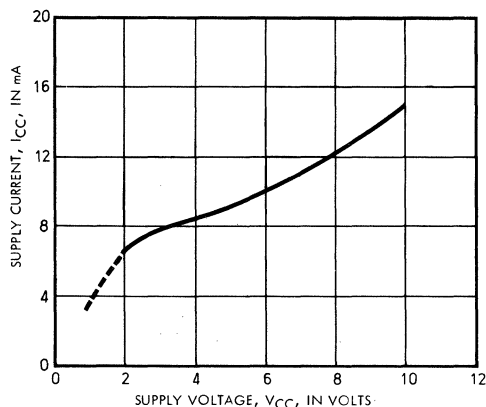
Dwg. No. A-11,517

**TYPICAL AUDIO POWER OUTPUT
AS A FUNCTION OF SUPPLY VOLTAGE**
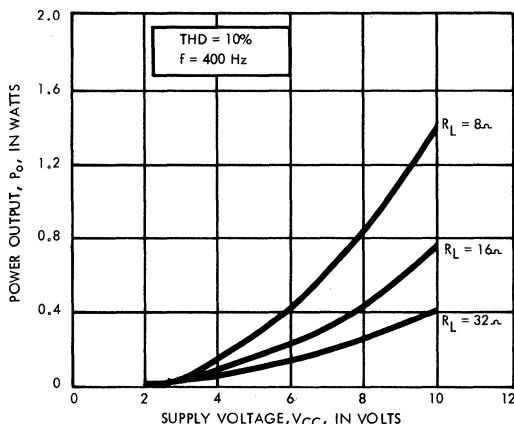
Dwg. No. A-11,518

AUDIO AMPLIFIER
TOTAL HARMONIC DISTORTION
AS A FUNCTION OF OUTPUT POWER

AUDIO AMPLIFIER
WITH 8Ω LOAD
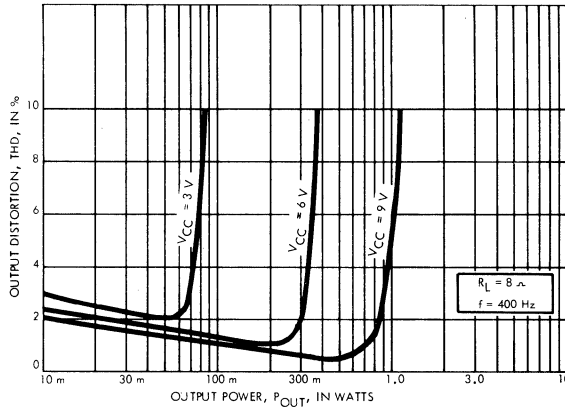
Dwg. No. A-11,519

AUDIO AMPLIFIER
WITH 16Ω LOAD
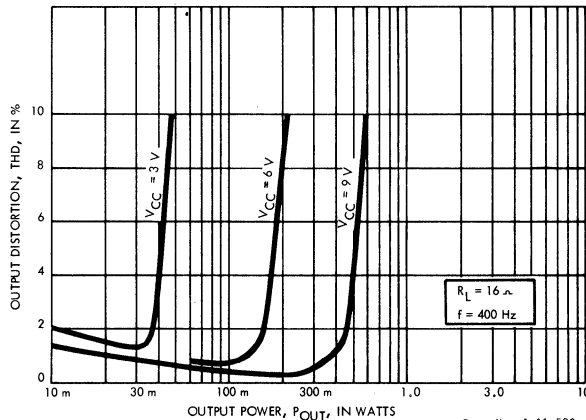
Dwg. No. A-11,520

6

TYPICAL APPLICATION

DWG. NO. B-1471

*Required only for V_{CC} = 9 V.

**I-F gain-dependent; see
"Optimizing System Performance."
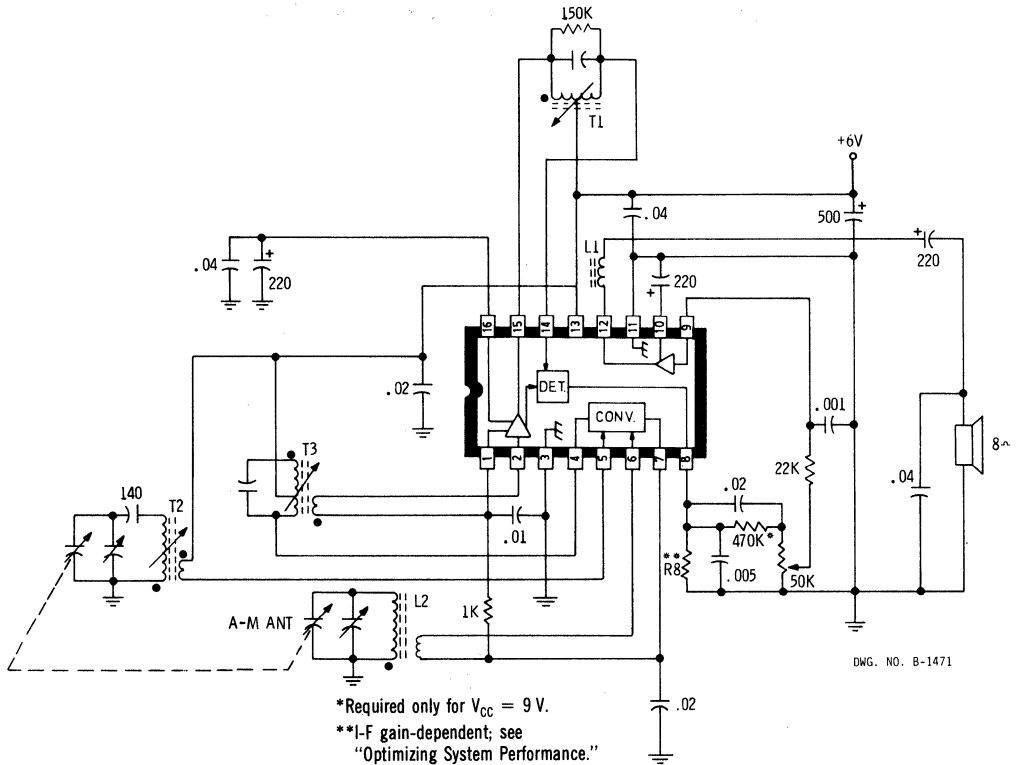
NOTE: Dress speaker wires as far as possible from antenna. L1 and 0.04 μF speaker bypass capacitor may be deleted, depending on speaker location.

COIL AND TRANSFORMER INFORMATION

L1	Audio Choke	10 μH, Qu = 2 @ 2.52 MHz, 3 turns through ferrite bead
L2	A-M Antenna Coil	Qu = 250, 110:10 turns ratio, Q2B core, 3.5'' (90 mm) × 0.394'' (10 mm) ϕ
T1	A-M Detector Coil	390 pF, Qu = 130 @ 455 kHz, 100 turns, center-tapped
T2	A-M Oscillator	460 μH, Qu = 120 @ 796 kHz, 110:11 turns ratio
T3	A-M I-F Transformer	180 pF, Qu = 145 @ 455 kHz, 155:10 turns ratio, primary tapped at 127 turns

ULN-3840A HIGH-PERFORMANCE A-M/F-M SIGNAL PROCESSING SYSTEM

FEATURES

- 12 μV Limiting Threshold
- Tuning-Error/Level Muting
- Meter Drive
- Balanced A-M Mixer
- 5 μV A-M Sensitivity
- D-C Mode Switching
- Internal Voltage Regulator
- Meets Dolby® Noise Requirements
- 20-Pin Dual In-Line Plastic Package

Dwg. No. A-11,462

6
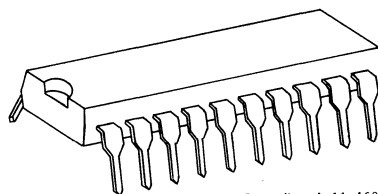
IDEALLY SUITED FOR TOP-NOTCH A-M/F-M radios, Type ULN-3840A provides sophisticated operating features highly desired by the modern consumer at a price that allows it to be used in budget receivers.

A combination of inter-station (signal-level) muting and off-channel (tuning-error) muting is useful in signal-seeking or scanning applications. The circuit design eliminates annoying low-frequency thump and noise tail when the system is manually tuned through a strong signal.

Outputs are available for directly driving a peak reading meter and a zero-tune meter. The peak meter output also is useful in controlling external system functions, such as blending multiplexers, stereo decoders, noise blankers, or in providing positive-going AGC for the tuner.

All standard F-M I-F functions and all A-M functions are provided by this single monolithic integrated circuit. The low-level audio output stages have been designed to meet stringent Dolby® noise requirements.

®Registered Trademark, Dolby Laboratories, Inc.

The A-M mixer is a balanced low-current analog multiplier with very low local oscillator feedthrough, high I-F rejection, and freedom from spurious responses. This mixer can be used in the long-wave, medium-wave, and shortwave bands.

A fully-balanced, four-stage differential I-F amplifier gives maximum gain with freedom from common-mode signals. It is used in both the A-M and F-M modes of operation with approximately 82 dB of gain in the F-M mode and controlled AGC gain of 26 dB in the A-M mode.

The detector in the F-M mode is a four-quadrant analog multiplier operating in the high-level injection mode. Common-mode signals are rejected through the use of balanced current-mirror outputs.

In the A-M mode of operation, the detector is configured as a balanced peak detector for low audio distortion. A-M gain control is achieved with AVC applied to the I-F and delayed AVC applied to the mixer.

Switching between modes can be accomplished with a simple single-pole d-c switch. The common low-level audio output can be used to drive an audio power amplifier (Type ULN-3703Z) or stereo decoder (Type ULN-3810A).

Internal voltage regulators and bias supplies assure premium performance despite variations in external supply voltage (8.5 to 16 V) or temperature ($-20°C$ to $+85°C$). Separate ground leads minimize decoupling problems.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 18 V
Mute Input Voltage, V_8 . . . . 5.0 V
Regulator Current, I_{REG} . . . . 5.0 mA
Package Power Dissipation, P_D . . . . 750 mW*
Operating Temperature Range, T_A . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . . $-65°C$ to $150°C$

*Derated at 9.4 mW/°C above $T_A = +70°C$.

FUNCTIONAL BLOCK DIAGRAM

DWG.NO. A-11,261

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 12.8 V$

Characteristic	Symbol	Test Pin	Test Conditions	Limits			Units
				Min.	Typ.	Max.	
Operating Voltage Range	V_{CC}	10		8.5	12.8	16	V
Audio Output Voltage	V_6	6	No Signal	—	5.8	—	V
Regulator Output Voltage	V_{REG}	13	No Signal	—	6.4	—	V
Avail. Reg. Output Current	I_{REG}	13		2.0	—	—	mA
F-M MODE: $f_0 = 10.7$ MHz, $f_m = 400$ Hz, $f_d = ±75$ kHz, $V_{in} = 10$ mVrms, Non-Muted (unless otherwise specified)							
Input Limiting Threshold	V_{TH}	2		—	12	25	μV
Recovered Audio	V_{OUT}	6		350	425	600	mV
Output Distortion	THD	6		—	0.3	0.7	%
Output Noise	S + N/N	6		74	80	—	dB
A-M Rejection	AMR	12	See Note	40	>55	—	dB
Mute	ΔV_{out}	6	$V_{in} = 100$ μV, Max. Mute	—	—	−1.0	dB
			$V_{in} = 5.0$ μV, Max. Mute	−45	—	—	dB
AFC Output Voltage	V_{afc}	7		220	—	600	mV
I-F Input Voltage	V_2	2	No Signal	—	3.5	—	V
Mute Output Voltage	V_{14}	14	No Signal	3.6	4.2	—	V
Mute Output Current	I_{14}	14	No Signal	0.5	—	—	mA
Supply Current	I_{CC}		No Signal	—	23	35	mA
A-M MODE: $f_0 = 1$ MHz, $f_{if} = 455$ kHz, $f_m = 400$ Hz, 30% A-M, $V_{in} = 1.0$ mVrms (unless otherwise specified)							
Sensitivity	V_{in}	18	$V_{out} = 50$ mVrms	—	5.0	8.5	μV
Usable Sensitivity		18	20 dB S + N/N	—	6.0	—	μV
Recovered Audio	V_{out}	6	80% A-M	250	325	600	mV
Input Overload	V_{in}	18	80% A-M, THD = 10%	25	50	—	mV
A-M Decoupling Voltage	V_1	1	No Signal	—	1.0	—	V
I-F Input Voltage	V_2	2	No Signal	—	3.7	—	V
Mute Output Voltage	V_{14}	14	No Signal	—	—	0.5	V
Peak Meter	V_{15}	15	No Signal	—	<0.5	—	V
			$V_{in} = 10$ mV	—	3.0	—	V
A-M Input Voltage	V_{17}	17	No Signal	1.6	1.8	2.1	V
Supply Current	I_{CC}		No Signal	—	16	30	mA

Note: Amplitude Modulation Rejection is specified as $20 \log \dfrac{V_{out} \text{ for } 100\% \text{ F-M } V_{in}}{V_{out} \text{ for } 30\% \text{ A-M } V_{in}}$

6

SMALL-SIGNAL A-C CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Pin	Test Conditions	Limits Min.	Typ.	Max.	Units
I-F Input Capacitance	C_2	2		—	6.0	—	pF
I-F Output Resistance	R_{12}	12		—	250	—	kΩ
I-F Output Capacitance	C_{12}	12		—	2.5	—	pF
Audio Output Impedance	Z_6	6		—	350	—	kΩ
F-M MODE: $f_0 = 10.7$ MHz							
I-F Input Resistance	R_2	2		—	10	—	kΩ
I-F Transconductance	g_m	2-12		—	8.0	—	mho*
Detector Input Resistance	R_{11}	11		—	100	—	kΩ
Detector Input Capacitance	C_{11}	11		—	1.5	—	pF
A-M MODE: $f_0 = 1$ MHz, $f_{if} = 455$ kHz							
A-M Input Resistance	R_{18}	18		—	5.0	—	kΩ
A-M Input Capacitance	C_{18}	18		—	20	—	pF
Mixer Transconductance	g_m	18-19		—	15	—	mmho*
Mixer Output Resistance	R_{19}	19		—	500	—	kΩ
Mixer Output Capacitance	C_{19}	19		—	5.0	—	pF
I-F Input Resistance	R_2	2		—	15	—	kΩ
I-F Transconductance	g_m	2-12		—	160	—	mmho*
Detector Input Resistance	R_{11}	11		—	250	—	kΩ
Detector Input Capacitance	C_{11}	11		—	1.0	—	pF

*The International Electrotechnical Commission recommends the use of siemens (S) as the standard international unit of conductance, admittance and susceptance.

F-M TUNING-ERROR DETECTOR RESPONSE
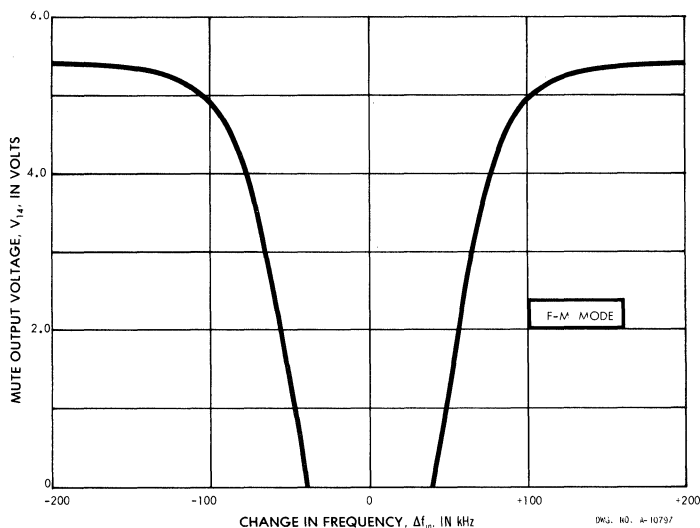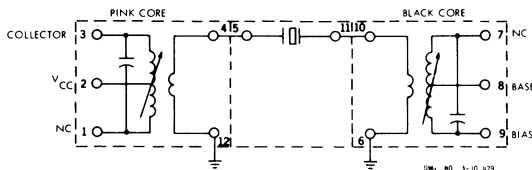

DWG. NO. A-10797
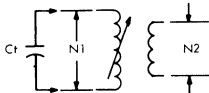
TEST CIRCUIT
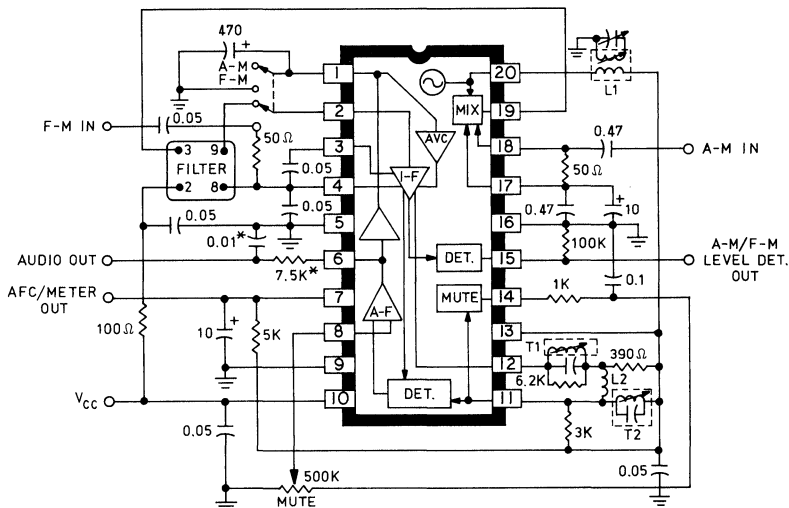
Dwg. No. A-11,262

*In application, R = 0 Ω, C = 0.008 μF for 50 μs de-emphasis (Europe) or 0.012 μF for 75 μS de-emphasis (U.S.A.)

Filter Assembly:
Toko Part No. CFU455C-82BR
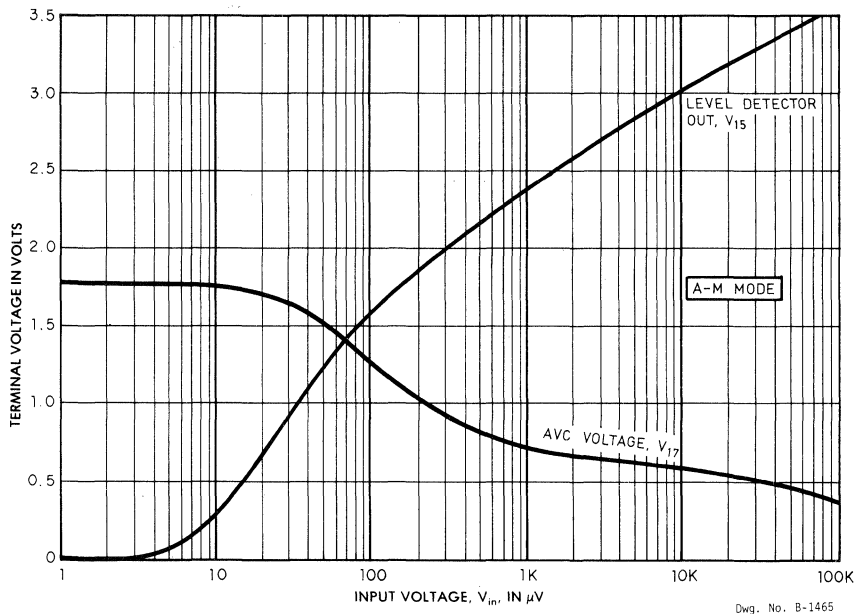

DWG. NO. A-10,479

COIL WINDING INFORMATION

DWG. NO. A-10,428

T1 A-M I-F 455 kHz	Qu = 45 Ct = 1000 pF	General Instrument Part No. EX 27765	Toko Part No. RXN-6A6909HM
T2 F-M Detector 10.7 MHz	Qu = 60 Ct = 82 pF	General Instrument Part No. EX 27975	Toko Part No. TKAC-17044Z
L1 A-M Oscillator 1455 kHz	Qu = 50 N1:N2 = 11:1 Ct = 39 pF	General Instrument Part No. EX 27641	Toko Part No. RWO-6A7640BM
L2 F-M Detector 10.7 MHz	L = 18 μH Qu = 55 @ 2.5 MHz	Coilcraft Type V	

A-M CONTROL VOLTAGES AS FUNCTIONS OF INPUT SIGNAL

LEVEL DETECTOR OUT, V$_{15}$

A–M MODE

AVC VOLTAGE, V$_{17}$

TERMINAL VOLTAGE IN VOLTS

INPUT VOLTAGE, V$_{in}$, IN μV

Dwg. No. B-1465

F-M CONTROL VOLTAGES AS FUNCTIONS OF INPUT SIGNAL

V$_{CC}$ = 12.8V
T$_{A}$ = +25°C

MUTE OUT, V$_{14}$

LEVEL DETECTOR OUT, V$_{15}$

TERMINAL VOLTAGE IN VOLTS

INPUT VOLTAGE, V$_{in}$, IN μV

Dwg. No. A-11,263A

A-M CHARACTERISTICS AS FUNCTIONS OF INPUT SIGNAL

RECOVERED AUDIO, V_{out}

THD

A-M MODE
0 dB = 325 mV

$\frac{S+N}{N}$

RELATIVE LEVEL IN dB

INPUT VOLTAGE, V_{in}, IN μV

DWG. NO. B-1367A

F-M CHARACTERISTICS AS FUNCTIONS OF INPUT SIGNAL

RECOVERED AUDIO, V_{out}

F-M MODE
0 dB = 425 mV

OUTPUT NOISE

A-M REJECTION

TO -80 dB

RELATIVE LEVEL IN dB

INPUT VOLTAGE, V_{in}, IN μV
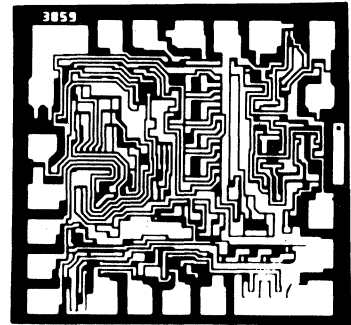
DWG. NO. B-1368A
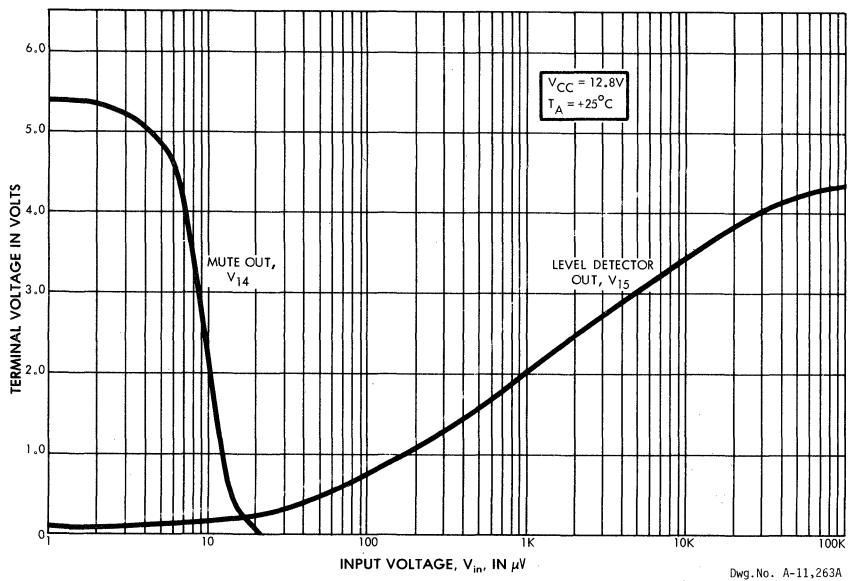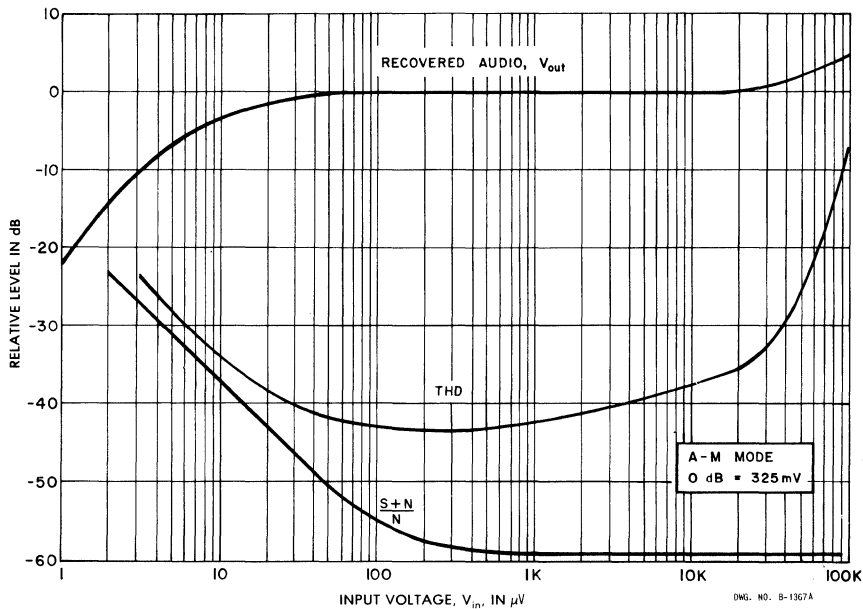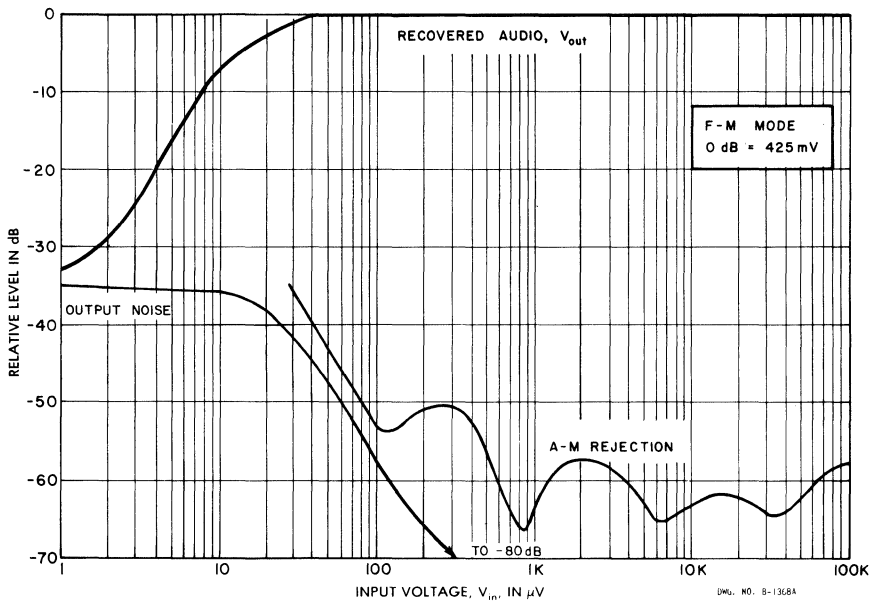
6

ULN-3859A
F-M COMMUNICATIONS I-F SYSTEM

FEATURES

- Dual Conversion
- Low Current Drain
- Wide Operating Voltage Range
- High Sensitivity
- Replaces MC3359P
- 18-Pin Dual In-Line Plastic Package

THIS low-power, narrow-band F-M I-F system provides the second converter, second I-F, demodulator and squelch circuitry for communications and scanning receivers.

Type ULN-3859A's double-balanced mixer permits low-noise operation while eliminating spurious responses, effectively rejecting tweet and I-F feedthrough, and reducing local oscillator radiation. The mixer's high input impedance matches popular 10.7 MHz crystal filters while its output impedance matches most 455 kHz ceramic filters. Although designed for use with a 10.7 MHz first I-F and a 455 kHz second I-F, the mixer operates at other R-F or I-F input frequencies through 30 MHz.

A multi-stage 1 MHz differential amplifier/limiter following the second I-F filter operates as a high gain stage with excellent common-mode rejection.

Audio is recovered by a quadrature F-M detector that requires only a single low-cost tuned circuit.

Type ULN-3859A has both a low-impedance emitter-follower audio output and an AFC output. Few external components are needed for operation with noise-activated or tone squelch.

This communications I-F system meets the stability requirements of many automotive applications, and also meets the low-power demands of portable radio design. Internal voltage regulators and bias supplies ensure stable performance despite variations in external supply voltage (4 to 9 V) or temperature (−20°C to +85°C).

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 12 V
Mixer Terminal Voltage, V_{in} . . . . 1.0 Vrms
Mute Terminal Voltage Range, V_{16} . . . . -0.5 V to $+12$ V
Operating Temperature Range, T_A . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_s . . . . $-65°C$ to $+150°C$

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 8.0$ V, $f_o = 10.7$ MHz, $f_m = 1.0$ kHz, $f_d = \pm3.0$ kHz (unless otherwise noted)

Characteristic	Test Pin	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Operating Voltage Range	4		4.0	8.0	9.0	V
Quiescent Supply Current	4	$V_{14} = 0$, Mute OFF	—	3.0	6.0	mA
		$V_{14} \geq 0.7$ V, Mute ON	—	4.0	7.0	mA
Input Limiting Threshold	18	-3 dB Limiting	—	2.0	6.0	μV
Mixer Conversion Gain	3	See Note 1, Next Page	—	24	—	dB
Mixer Input Resistance	18		—	3.6	—	kΩ
Mixer Input Capacitance	18	See Note 2, Next Page	—	2.2	—	pF
Mixer Output Impedance	3		—	1.8	—	kΩ
Limiter Input Impedance	5		—	1.8	—	kΩ
Quiescent D-C Output Voltage	10	$V_{in} = 0$	2.4	3.6	4.4	V
Audio Output Impedance	10		—	500	—	Ω
Recovered Audio Output	10	$V_{in} = 3.0$ mV	450	700	—	mV$_{rms}$
Amplifier Gain	13	$f = 4.0$ kHz, $V_{in} = 5.0$ mV	40	53	—	dB
Quiescent D-C Output Voltage	13	$V_{in} = 0$	—	1.7	—	V
Mute Switch Resistance	16	$I_{16} = 2.5$ mA, $V_{14} \geq 0.7$ V	—	4.0	10	Ω
Scan Source Current	15	$V_{14} = V_{15} = 0$, Mute OFF	2.0	4.0	—	mA

6

TEST CIRCUIT
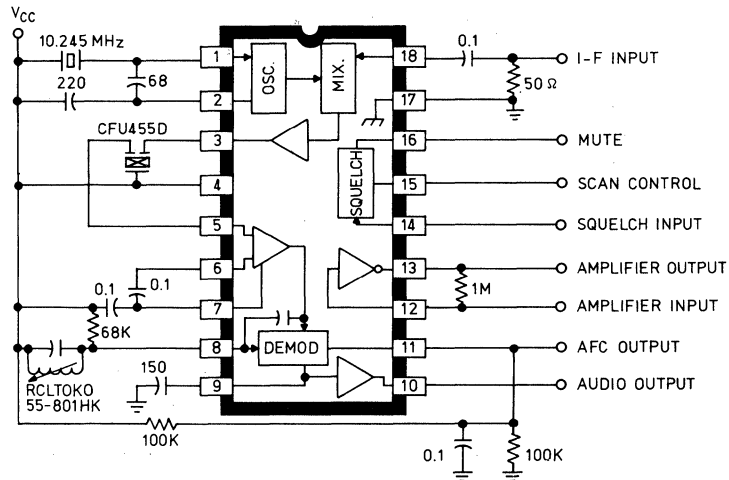
Dwg. No. A-11,372

APPLICATION INFORMATION

1. In a typical application, with a 3.6 kΩ crystal filter source, Type ULN-3859A will give 23 dB conversion gain.

2. Because crystal filters are extremely sensitive to reactive loading, radio designers frequently have added a coil and/or capacitor at pin 18 to cancel the input reactance component. This practice is not required with Type ULN-3859A, since its input is designed to match typical 10.7 MHz crystal filters. However, if an external reactive component is used, it is important to adjust it for optimal passband shape and not simply to peak it for maximum sensitivity.

3. Pin 11 provides AFC. If AFC is not required, pin 11 should be grounded, or tied to pin 9 to double the available recovered audio.

4. Pin 10 may require an external resistor (2 kΩ minimum) to ground to prevent audio rectification with some capacitive loads.

ULN-2204A A-M/F-M RECEIVER SYSTEM
—TYPICAL APPLICATIONS AND OPERATION

Introduction

Through the relatively short history of bipolar monolithic circuits, several revolutionary new circuits have been developed for a-m/f-m receiver design. A. Bilotti pioneered the original monolithic f-m quadrature detector/I-F gainblock in the form of the Sprague ULN-2111A.

Subsequent devices have included gain-control stages, output drivers, and voltage regulators. During this same period a-m integrated circuitry showed far less inspiration. Numerous a-m circuits were developed which in essence attempted to combine the active elements of a discrete bipolar a-m receiver in a monolithic circuit. To no surprise, the resulting chips were *at best* capable of performance no better than the parent discrete design, and with the uneconomical displacement of three discrete transistors with one integrated circuit. In addition to the a-m-only circuits and f-m-only circuits, a-m/f-m circuits were also attempted using the same design approaches used for the a-m only circuit, that of combining an existing discrete receiver circuitry in a monolithic device. The results were much like the a-m only efforts, a bewildering collection of economically unattractive circuits of modest performance.

To achieve useful cost and performance objectives, the ULN-2204A was designed with careful attention to the cost and performance objectives of the modern portable and table model broadcast receiver. Concern for low external component count, low power consumption, wide supply voltage range, and versatility remained foremost as design objectives.

Power Amplifier

To achieve the desired performance objectives of high power output and efficiency from a 2 to 12 V supply requires that the power amplifier be capable of peak-to-peak voltage swings approaching the available supply. To meet these performance objectives a new power amplifier design was required having no more than one V_{BE} of swing restriction.

As shown in Figure 1, the output stage is comprised of 2 NPN transistors (Q42 and Q49) plus a phase inverter (Q54). Quiescent operating current is set up by the current source (I).
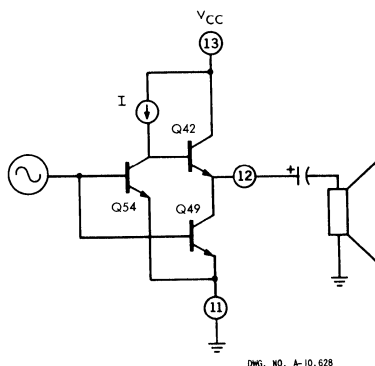

DWG. NO. A-10.628

Figure 1

Assuming $V_{oq} = V_{CC/2}$ then the collector current of Q54 = I, ignoring base currents, and if Q54 is matched to Q49 as is possible in a monolithic circuit, then the collector current of Q49 equals the collector current of Q54. The circuit in Figure 1 achieves an excellent voltage swing capability of $V_{CC} - V_{Be} - 2V_{CE(SAT)}$. This totally NPN configuration also has good freedom from the high-frequency problems that often occur with quasi-complementary composite NPN-PNP configurations.

Although the circuit in Figure 1 has been incorporated in production monolithic circuits in essentially the form shown, in practice it has unacceptable design restrictions. Since I is also the base drive current for Q42, the ratio of available base drive current I to idling current is proportional to the ratio of the emitter areas of Q49 to Q54. For practical values of IQ54/IQ49, i.e. one, the circuit has a serious implementation problem; it requires three output transistors (Q42, Q49, and Q54).

To reduce the size of Q54, an additional transistor (Q48) is added to the circuit as shown in Figure 2. Transistor Q48 divides I by its beta + 1 allowing Q54 to be reduced in area by a similar value. In the practical realization of the ULN-2204A, Q54 is chosen as 1/5 the emitter area of Q49 with a typical beta for Q48 of 6.
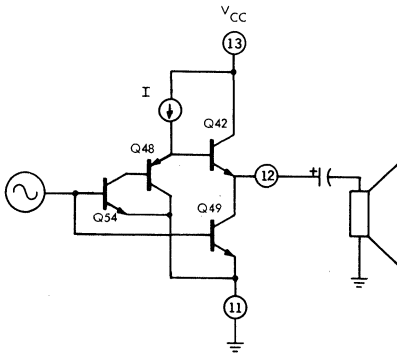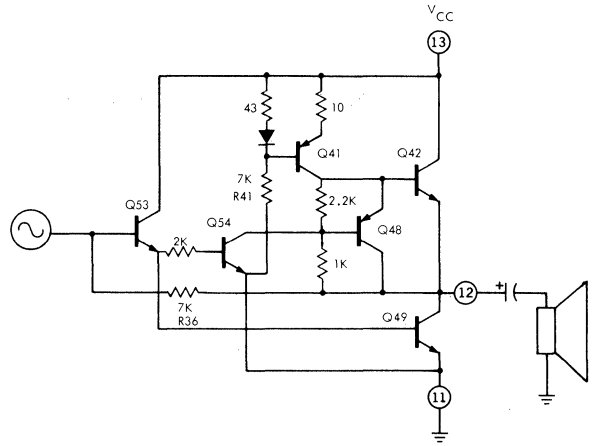

Figure 3

capacitor. Overall negative feedback, set by the ratio of R33 to R32, is applied to the inverting input Q45 through an NPN emitter follower (Q46) which also provides d-c level shifting.

Figure 2

Figure 3 illustrates other refinements in the practical realization of the output circuit. The drive and idling current I is derived from a V_{CC} dependent source allowing maximum drive under maximum supply conditions while affording reduced drive and associated current conservation under minimum supply conditions. In addition, the Q48 divider circuit is refined to reduce PNP beta dependence. Finally with the addition of an input emitter follower (Q53) and a local negative feedback loop (R36), the output is completed as it appears in the ULN-2204A.
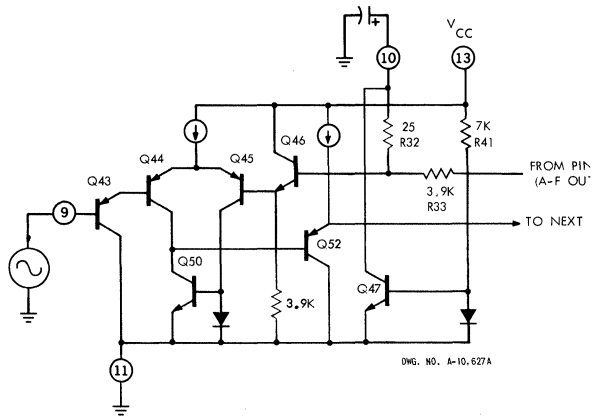
The input stage of the power amplifier (Figure 4) is comprised of a PNP differential pair (Q44 and Q45) preceded by a PNP emitter follower (Q43) which allows d-c referencing the source signal to ground. This eliminates the need for an input coupling

Figure 4

The $V_{CC}/2$ output tracking is achieved by summing the current flow through R33 and R32, with the current through R41 "reflected off of ground". Thus $V_{CC}/2$ tracking is maintained by the voltage drop across 2 resistors. This allows the current from R41 to be bypassed at Pin 10, thereby combining the ripple bypass capacitor with the audio feedback capacitor.

Figure 5 illustrates the complete power amplifier as realized in the ULN-2204A, including the external components. The remarkably-low external component count, (only two capacitors including the output coupling) reflects concern for simplicity in implementation, yet the device achieves excellent performance. Typical output power can be as high as 850 mW from a 9 volt supply and useful output power at supply voltages of as low as 2 volts, with minimum of distortion as the curves in Figure 6 illustrate.
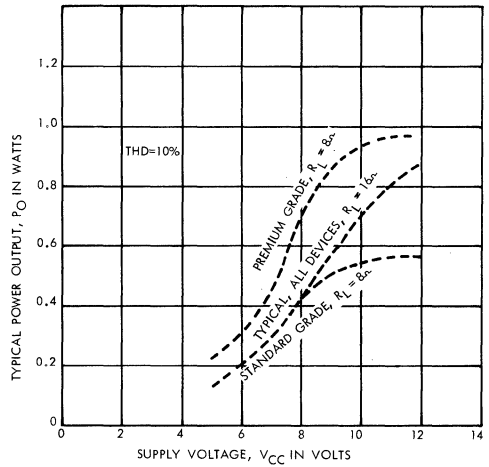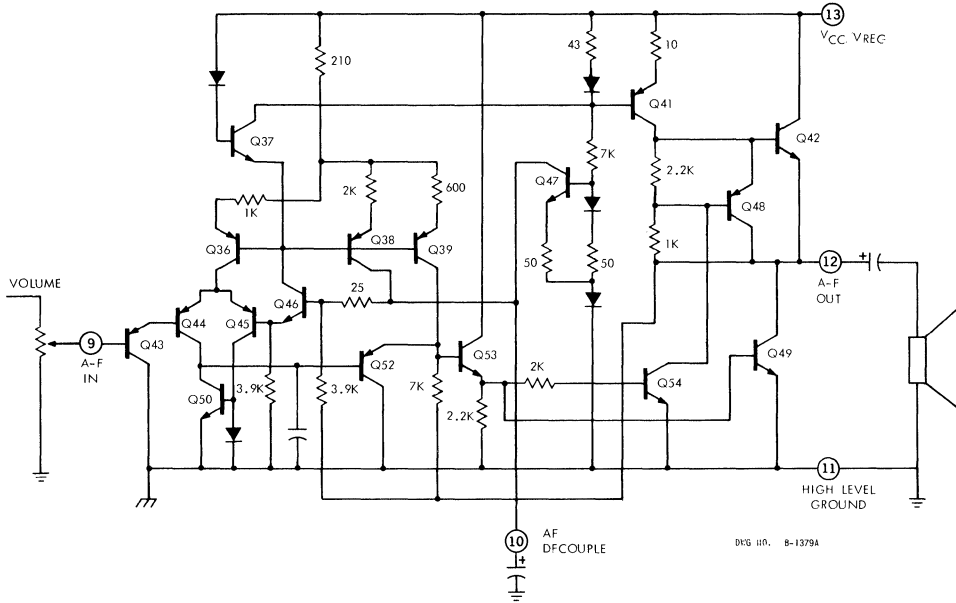
Figure 6

Figure 5

Receiver

The a-m signal is processed from the antenna to the detector output via the traditional blocks of mixer, I-F, and detector enclosed in a reverse A-G-C loop. However, closer examination reveals certain very important advantages that can be afforded only by the monolithic design.

The a-m mixer is a fully-balanced mixer based on a four-quadrant multiplier as shown in Figure 7. This affords rejection of both the oscillator and input signal as observed at the output. In addition, an analog multiplier is (as the name implies) a true linear device. Balanced operation of the mixer provides typically 25 dB of I-F rejection at the input, with a similar rejection of the associated noise passband. Also, the linear operation of the circuit affords good freedom from intermodulation product responses.

I-F gain is provided for both a-m and f-m by a common I-F amplifier (Figure 8) using "stacked" selectivity. In f-m operation the gain of stages 1, 2, 3, and 4 (Q1 thru Q8) is set at typically 76 dB providing a typical limiting threshold of 40 μV.

For a-m the gain is lowered by reducing stage current. This is accomplished by reducing the current applied to the I-F amplifier by the current source Q17. The fifth I-F stage (Q9 and Q10) is operated at maximum gain and current to provide full signal to the a-m and f-m detector.

A-M/F-M Detector

The detector is also a combination circuit. It recovers a-m audio by peak detection and f-m audio by phase discrimination.

The a-m signal from the I-F output appears at Pin 15 across T_2 as shown in Figure 9. The signal is applied to the base of Q18 and after phase inversion by T_2 is applied also to the base of Q19. Full wave detection occurs at the emitter of Q18 and Q19, utilizing the on-chip junction capacity for integration. This requires only that the stage current be chosen at a low value (typically 1 μA) to produce the desired integration.

The f-m detection process relies on the phase/frequency relationship of a tuned external circuit for demodulation. The device converts phase
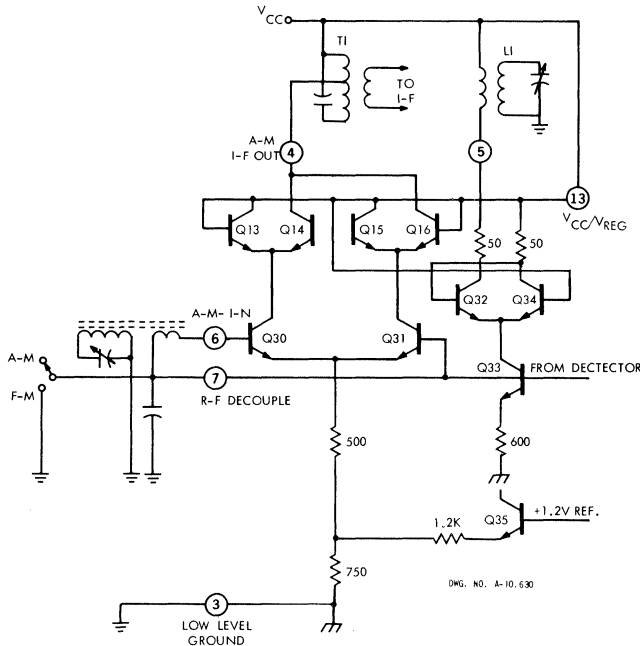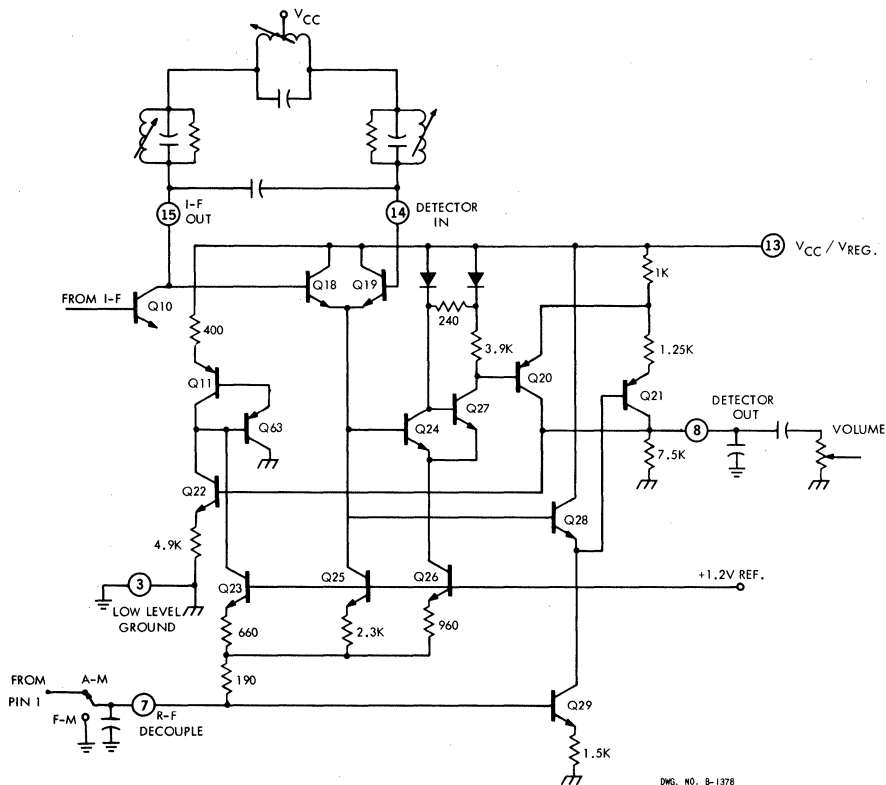

Figure 7

variation, as observed across the tuned network, to a proportional voltage. The basic phase detection process combines the positive-going portions of the quadrature and reference signals (Pin 14 and 15, respectively), and evaluating the duty cycle of the resulting waveform as shown in Figure 10. The combining action occurs at the emitters of Q18 and Q19 resulting in the waveform shown. Subsequent processing involves squaring up the signal in a limiter, comprised of Q24 and Q27, resulting in the constant-amplitude plus train which is also shown. This pulse train is then applied to a PNP gain stage which, owing to the PNP's low f_T of typically 1 MHz, integrates the pulse train into an average d-c

voltage which appears at Pin 8, the detector audio output. Figure 11 illustrates the complete a-m/f-m detector of the ULN-2204A, including the external components.

To complete the circuit, the a-m stages also require A-G-C. This is implemented in the ULN-2204A by internally setting the I-F supply voltage (Pin 16) equal to the voltage at the detector audio output. As carrier appears, a corresponding reduction in the d-c voltage occurs at the audio output terminal and at Pin 16, where an external bypass capacitor removes audio from the A-G-C line and sets the time constant.

Figure 8

6

Figure 9

Figure 10

Figure 11

Application

The primary application, but certainly not the only application, for the ULN-2204A is the broadcast band a-m/f-m table or portable radio as illustrated in Figure 12.

Power Amplifier

Selection of power supply voltage and speaker impedance allow the designer to choose audio power levels up to almost 1 watt as the curves in Figure 6 illustrated. No unique precautions are necessary when designing with the ULN-2204A power amplifier. The device is stable and short-circuit immune.

External component choice for the power amplifier involves only two capacitors; one for the speaker coupling and one for the feedback and ripple by-passing. The coupling capacitor value should be selected to provide the desired low-frequency cutoff with the chosen speaker impedance. The feedback and ripple bypass capacitor at Pin 10 should be chosen for both low-frequency audio rolloff and supply ripple rejection.

Ripple rejection is not practical to calculate due to the large number of mechanisms involved. The 220 μF capacitor indicated in Figure 12 achieves typically 35 dB rejection.

The high gain of typically 43 dB and the high input impedance (200 kΩ) of the power amplifier allow utilization of this stage for other applications such as ceramic cartridge phono amplifiers.

Typical ceramic phono cartridges develop approximately 400 mV. However, the recommended

load impedance for the most economical cartridges is usually 1 MΩ. This poses no problem with the 200 kΩ input impedance of the ULN-2204A since the cartridge manufacturer specifies the load impedance for full low-frequency response to less than 40 Hz. Decreasing the load impedance produces an increased low end cutoff frequency.

In a ULN-2204A based application employing a cost and space conscious loudspeaker, 40 Hz program material capability is not only unnecessary but undesirable, and therefore a mismatch of the cartridge to increase the lower cutoff frequency to a value more in keeping with the other components of the system is recommended.

The ULN-2204A audio amplifier stage has other input considerations to be taken into account for best results. The input is referenced to ground for internal biasing and must be provided with a d-c path to ground. A current of typically 0.1 μA flows from Pin 9 through the volume control producing an IR drop which is multiplied by the closed loop d-c gain of the amplifier (1), and appears as an error in output centering at Pin 12. This recommends a value of 200 kΩ or less for the volume control, with values of less than 100 kΩ preferred.

The selection of power amplifier load impedance involves more consideration than just the desired power output. Ideally an 8Ω speaker impedance would produce the highest power outputs for any one supply voltage as the curves in Figure 6 illustrated. However, operation with a 16Ω load can produce as much power as with an 8Ω load as is also shown in Figure 6. The higher impedance load will also furnish a significant reduction in harmonic distortion and improvement in overall repeatability in power output capacity. In applications which allow the selection of the power supply voltage it is therefore recommended that a 16Ω load impedance be utilized in applications up to 0.75 watt. For applications having fixed power supply values, i.e. batteries, device selections can be had that produce the maximum power level into 8Ω.

Receiver Section — F-M

The f-m intermediate frequency input transformer, comprised of T_5 and T_6, provides both selectivity and coupling. T_5 should present a source impedance to the device of approximately 500Ω for optimal stability. T_6, the primary, is governed primarily by the characteristics of the tuner head feeding it, and should be selected for those considerations. T_5 and T_6 comprise a double tuned section which for monaural f-m should have a bandwidth of 150 kHz.

The ULN-2204A also provides a regulated and decoupled d-c bias voltage to be used as the V_{CC} supply for the tuner head. This bias voltage is obtained at Pin 16 and provides typically 2.5 mA. The current drain loads Pin 16 significantly and must appear for Pin 16 to operate at the correct voltage of 2.2 V. The voltage at Pin 16 determines the gain of the f-m intermediate frequency with higher values producing increased gain. The voltage at Pin 16 also varies with the voltage at Pin 8 (the detector output voltage), and therefore applies some A-F-C to the tuner head through the oscillators' V_{CC} supply.

As described earlier, the f-m detector is a phase detector which detects the phase shift of an external network appearing between Pin 14 and Pin 15. The preferred network is a double-tuned transformer as shown in Figure 10. This network is selected to provide the correct recovered audio and minimum distortion by choosing the loaded and coupled "Q"s. In Figure 12, T_3 (the primary) and T_4 (the secondary) are loaded by resistors of 2.2 kΩ and 4.7 kΩ, respectively, and top coupled by a 4.7 pF capacitor giving an S curve peak to peak separation of 400 kHz. Coupling factor (Qk) is slightly greater than 1 to improve harmonic distortion. The bandwidth has been selected to place the carrier of an adjacent channel interfering station (standard f-m broadcasting) on the peaks of the S curve, thereby improving selectivity. Using the circuitry shown, a typical recovered audio value of 250 millivolts at Pin 8 and total harmonic distortion value of 0.7 percent are achieved with 75 kHz deviation. It should be noted that the network, particularly the coupling capacitor value, is affected by layout and may require optimization for a particular application. Extremely high values of coupling factor should be avoided as this produces an undesirable voltage gain from Pin 15 to Pin 14 which manifests itself as S curve inbalance at low signal levels.

The f-m de-emphasis is formed by the 0.01 μF capacitor connected at Pin 8 with an internal 7.5 kΩ resistor.

Receiver Section — A-M

The a-m section requires two external coils for I-F matching and selectivity, plus the local oscillator coil. The a-m detector transformer (T_2) and mixer load coil (T_1) are stacked with the corresponding f-m components to form the composite. The selection of bandwidth for the two-coil system shown in Figure 12 is restricted primarily by the practical coil Qs available. The unloaded Q of the first transformer (T_1) being selected as 120 and loaded to ap-
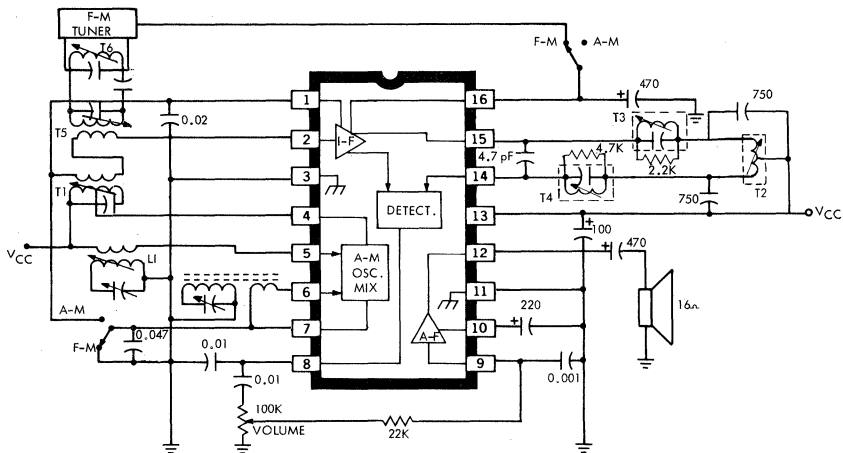
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COIL WINDING INFORMATION

T1	A-M First I-F 455 kHz	Qu = 120 N1:N2:N3 = 15.5:2.8:1 Ct = 180 pF	General Instrument Part No. 27835	Toko 7MC-A4018A or RMC2A7641A
T2	A-M Second I-F 455 kHz	Qu = 70 N1:N2 = 2:1 Ct = 430 pF	General Instrument Part No. 27836	Toko 7BO-A4017BM or RLE4A7642GO
T3	F-M Detector 10.7 MHz	Qu = 50 Ct = 100 pF	General Instrument Part No. EX 27639	Toko BKAC-K3651HM
T4	F-M Detector 10.7 MHz	Qu = 50 Ct = 100 pF	General Instrument Part No. EX 27640	Toko BKAC-K3651HM
L1	A-M Oscillator 1455 kHz	Qu = 50 N1:N3 = 10.7:1 Ct = 39 pF	General Instrument Part No. EX 27641	Toko 7BO-A4017BM or RWO-6A7640BM
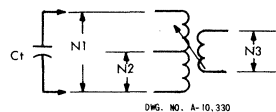
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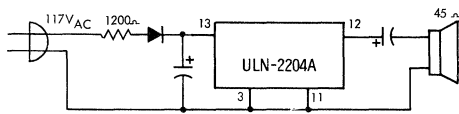
150 mW OUTPUT

DWG. NO. A-10.324
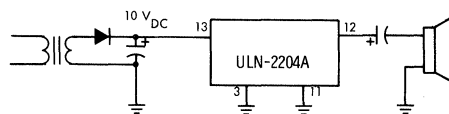
8 Ω SPEAKER – 1.0 W OUTPUT
16 Ω SPEAKER – 0.7 W OUTPUT
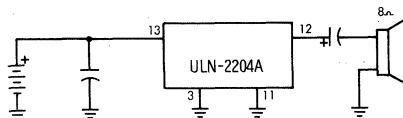
6V BATTERY (4 'AA' CELLS) – 250 mW OUTPUT
9V BATTERY (NEDA 1604) – 750 mW OUTPUT

Figure 12

proximately 90 in the circuit, and the second transformer T_2 as 70 with virtually no load presented by the circuit. Impedances are selected based on two constraints: a-m gain and overload. One additional point to consider is the behavior of the a-m component when the receiver is in the f-m mode.

The available I-F current at Pin 15 is 200 μA peak, 100 μA at its quiescent point. (See Figure 9). Maximum permissable swing at Pins 14 and 15 is limited to 0.5 volt positive with respect to Pin 13. This restricts peak voltage swing at Pin 15 to 1 V_{pp}, considering the inverting action of T_2. This restricts impedance of T_2, as seen by the I-F output, to values greater than 15 kΩ to permit maximum dynamic range. Including all worst case conditions, a value of 18kΩ is chosen for T_2 in the example. Considered were temperature variations and internal device tolerances. In addition, a 470 pF capacitor has been added to assure an adequate a-c return for the f-m coil.

Transformer T_1 (Figure 7) is chosen for the correct overload characteristics of the mixer. It also features a 100 μA quiescent state and a 0.5 volt peak swing restriction for primary impedance considerations, and the secondary winding chosen as the lowest practical impedance for desired system gain. Unlike T_2 which is not loaded to any degree by the circuit, T_1 is loaded by both the mixer output impedance of approximately 50 kΩ and the I-F input impedance of approximately 30 kΩ. Both must be taken into consideration in calculating the loaded Q of the transformer. In addition, the effect of the a-m components on the f-m I-F stability must be considered — the device must be stable at both the intermediate frequencies in both modes of operation. Although no practical method exists for evaluating stability criteria for an integrated circuit as is commonly done for discrete circuits, the practical ground rules are much the same — mismatching of the input at the first transformer to achieve stability.

The oscillator coil (L_1) has a secondary impedance selected to be approximately 800Ω at resonance. This provides typically 150 millivolts of injection voltage to the mixer driving the upper differential pairs of the four-quadrant multiplier into hard limiting. The oscillator is also restricted to a 1 V_{pp} swing and operates with a quiescent current of 0.5 mA.

Printed Wiring Board Layout and Special Considerations

Special on-chip considerations for minimizing tendencies towards instabilities of all types were taken in the design of the ULN-2204A. However, like all complex high-gain circuits, considerable care and forethought should still be given to a printed wiring board layout to avoid undesirable effects. Inputs and outputs should be well separated and should avoid common mode impedances wherever possible. Much of the signal-processing circuitry is referenced off of the supply line, and this should avoid being in a common mode loop caused by current drain of the power amplifier through Pin 13. Reference points for the local oscillator, a-m mixer, and the detector coils should be connected to Pin 13 very close to the device and away from the V_{CC} connection to the power supply bypass capacitor.

The Pin 13 common mode resistance will also interfere with device operation in a socket. In the f-m mode of operation, current drawn by the power amplifier will cause the Pin 13 voltage to drop slightly with respect to the reference for Pin 14 and 15. This will cause a variation in gain of the f-m detector. The effect also causes an apparent increase in distortion when the power amplifier is loaded, with distortion figures approaching several percent under worst case conditions. The effect is negligible, however, when the device is soldered into a printed wiring board.

Connections between Pins 14, 15, and transformers T_2, T_3, and T_4 should be kept as short as possible as should connections for Pins 1 and 2, those associated with the transformers. The ground return for the audio bypass at Pin 10 should be kept reasonably close to the volume control ground as Pin 9 and 10 represent the inverting and non-inverting inputs to the amplifier and enjoy about 40 dB of common mode rejection.

Other Applications — TV Sound Channel

Beyond the obvious applications of the ULN-2204A as an a-m/f-m receiver it has much to offer as a sound system for television. The device offers exceptionally-low current consumption and a wide operating supply voltage range. Its high a-m rejection and low external component count will make it practical for use in many power conscious applications. Most of the comments which apply to the f-m application of the ULN-2204A also apply to its application at 4.5 MHz or 5.5 MHz with suitable adaptations of the external selectivity components. (See Figure 13)

Multiband Receiver

The ULN-2204A A-M circuitry is not restricted to conventional broadcast band applications. The

6

Figure 13

ULN-2204A mixer and oscillator are both capable of operation from the very-long wave band to well above the medium wave bands. Only the antenna and oscillator coils need to be switched or adapted

for use at other frequencies. The useful limits of the mixer-oscillator combination extend to approximately 50 MHz with excellent performance up through and including the citizens' band at 28 MHz.

A-M/F-M RECEIVER DESIGNS USING ULN-2240A, ULN-2241A, and ULN-2242A INTEGRATED CIRCUITS

THREE MONOLITHIC INTEGRATED circuits, Types ULN-2240A, ULN-2241A and ULN-2242A, each contain all the active circuit elements required for the A-M tuner, F-M I-F amplifier and detector functions. Only an F-M tuner, filter elements, and a minimum of additional external components are necessary for a complete A-M/F-M receiver.

This Application Note discusses several circuits and options for a number of A-M/F-M receiver applications. Each of the three Sprague integrated circuits used provides performance characteristics equivalent to or better than systems using discrete components for A-M and F-M functions.

The circuits are ideal for special receivers such as scanners which must be able to detect A-M and F-M signals at one I-F frequency. Also, the three devices lend themselves to shortwave receiver designs because of the simplicity of their A-M oscillator systems.

The various receiver designs covered here include an A-M tuner using a ferrite antenna, and a permeability-tuned automobile radio. Enhanced sensitivity and overload performance is obtained with the addition of an R-F amplifier, easily accomplished using the AGC voltage for the A-M mixer to control an R-F amplifier stage. The discussion covers a table model receiver with a ferrite antenna and R-F stage, and an R-F stage for an automobile receiver. The concept is extended to varactor-tuned automobile radios with the addition of an FET-bipolar cascode R-F stage and an AGC driver.
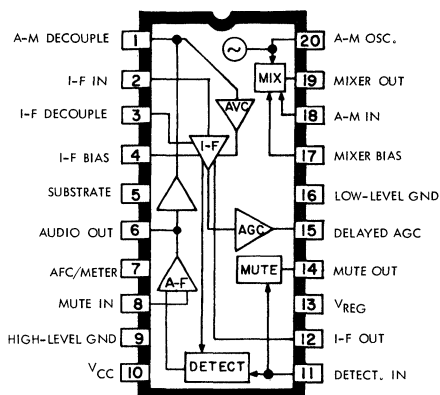
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ULN-2240A
ULN-2242A
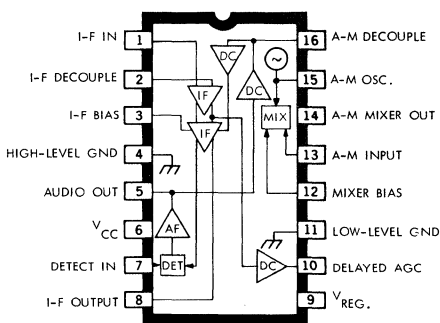
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ULN-2241A

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General Performance Considerations

Internal voltage regulators and bias supplies assure consistent performance despite variations in external supply voltage (8.5 to 16 V) or operating temperature ($-40°C$ to $+85°C$). Separate ground leads minimize decoupling problems.

The A-M sections of all three devices are the same. Use of an analog multiplier as a balanced low-current mixer results in freedom from spurious responses, high tweet rejection, low feedthrough, and low noise and very low local oscillator feedthrough. A fully-balanced four-stage differential amplifier gives maximum gain with freedom from common-mode interference

and noise. A-M gain control is achieved with AVC applied to the I-F and delayed AVC applied to the mixer.

The differences in these three circuits are found in the F-M sections, with packaging variations to accomodate the different features. Type ULN-2241A is supplied in a 16-pin plastic dual in-line package. This circuit has no mute, and no AFC/tuning meter output (the audio output can be used for AFC). Type ULN-2242A, in a 20-pin package, incorporates the F-M mute and AFC/tuning meter output. Type ULN-2240A, also in a 20-pin package, adds tuning-error mute, and higher F-M S/N.

Input-Filter Coupling

The common A-M and F-M I-F inputs for all three devices are basically the same. Note that terminals 1, 2 and 3 for Type ULN-2241A correspond to terminals 2, 3 and 4 respectively for Types ULN-2240A and ULN-2242A.

The method of arranging the I-F filters

depends entirely on the type of filters used. For example, coils placed in series may be used for A-M and F-M connected as shown in Figure 1.

A ceramic filter may be used for F-M with an A-M filter incorporating a tuned coil in its output. This arrangement is illustrated in Figure 2.
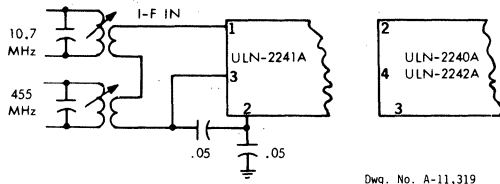

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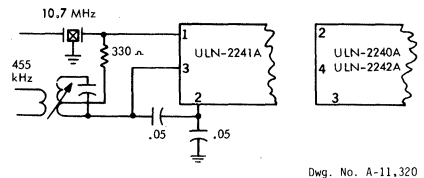**Figure 1**

Dwg. No. A-11,320

Figure 2

The I-F input impedance is very high (10 kΩ @ 10.7 MHz; 15 kΩ at 455 kHz) and can be ignored when selecting loading resistors for different types of I-F filters. Additionally, the input stage bias currents are very low, therefore a relatively high-value resistor can be connected between pins 1 and 3 of Type ULN-2241A, or pins 2 and 4 of Type ULN-2240A or ULN-2242A, without significantly affecting the limiter balance.

These characteristics simplify the input filter coupling to accomodate ceramic filters used for both A-M and F-M I-Fs as shown in Figure 3.

Most 455 kHz filters are terminated by a 1 to 3 kΩ resistor in parallel with a capacitor of less than 50 pF. The 10.7 MHz filter requires a 330 Ω termination. If the capacitance of the 455 kHz filter is high at 10.7 MHz, the circuit will work properly as shown. However, if the capacitance of the 455 kHz filter is low, it would be advantageous to add an inductance in series with the 330 Ω resistor to form a series resonant circuit with the output capacitance of the 455 kHz filter. Such a modification is shown in Figure 4.

If the inductance required is very small, it might be possible to incorporate it as an integral part of the printed wiring board.
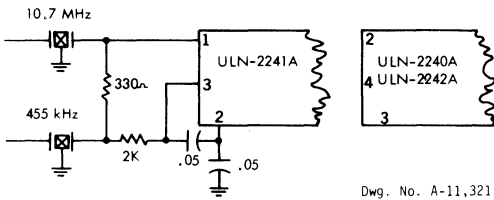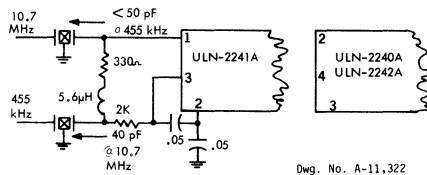

Figure 3

Figure 4

A-M Detector Considerations

Passive diode detectors are still used in many low-cost receiver designs. The A-M detector functions of Types ULN-2240A, ULN-2241A and ULN-2242A, however, are entirely self-contained. Several drawbacks to the passive diode detector design are overcome; the load presented to the detector coil does not change with signal level, the detected output is not distorted at low signal levels, and the detector coil is not loaded down, so overall receiver selectivity is unaffected.

The self-contained detector design produces excellent A-M performance without external filtering elements. There is virtually no 910 kHz and 1365 kHz tweet. Distortion at 30% modula-

tion is only 0.3%, and at 80% modulation the distortion is still under 1%.

The design of the detector coil is strictly dependent on the type of receiver desired. The detector input impedance is about 250 kΩ. For optimum detector operation, the coil should present an impedance of 4.7 kΩ. An inexpensive detector coil can be loaded with an external resistor or tapped to obtain the 4.7 kΩ impedance.

It should be noted that the A-M detector works very well at 455 kHz and also at 10.7 MHz. Switching from A-M to F-M is as simple as grounding one pin of the integrated circuit.

F-M Detector Options

The F-M detector functions in these three integrated circuits are very similar to those of Type ULN-3889A and the same type of circuit arrangements may be used. For low-cost receivers where distortion up to 0.4% at 100% modulation can be tolerated, the single-tuned coil detector illustrated in Figure 5 is most appropriate.
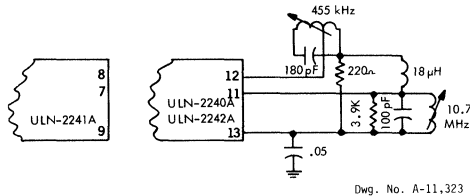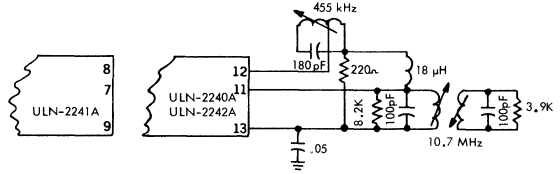

Dwg. No. A-11,323

Figure 5

Note that terminals 7, 8 and 9 of Type ULN-2241A correspond respectively to terminals 11, 12 and 13 for both Type ULN-2240A and Type ULN-2242A.

Types ULN-2240A and ULN-2242A require 165 mV injection level at pin 11 to insure proper mute detector operation.

Lower interstation noise levels can be obtained in applications using Type ULN-2241A by using a lower value resistor than the 220 Ω I-F load resistor shown (typically 82 Ω) and thus reducing the injection level.

The double-tuned detector shown in Figure 6 provides signal distortion levels as low as 0.1%. In addition, the double-tuned detector minimizes distortion as a function of tuning, when the receiver is tuned away from a strong signal.

Dwg. No. A-11,324

Figure 6

Usually the primary coil is adjusted for the maximum audio output while the secondary coil is adjusted for minimum distortion. Perfect detector balance at minimum distortion is desirable; however, a signal lag caused by excess parasitic capacitance from the I-F output to ground could prevent this.

The parasitic capacitance of the A-M detector coil may effectively compensate for this signal lag or it can be eliminated by placing a small inductance (0.1 to 1.0 μH) in series with the 220 Ω load resistor.

Any of the three signal processing systems can be used as phase-locked F-M detectors. An external, voltage-controlled oscillator signal must be applied to the F-M detector. If the audio output is used, the phase detector constant $K_D = 4.8$ volts/radian. If the AFC output is used, then:

$$K_D = 785 \times 10^{-6} \times R_L.$$

R_L is the value of the resistor connected to V_{REG}.

The AFC output is preferred because the audio can then still be muted without affecting the loop operation. More detailed information can be found in a paper published by Jon P. GrosJean. See Reference 2.

High-Performance A-M/F-M Tuner

A high-performance A-M/F-M tuner illustrated in Figure 7 uses an R-F stage controlled by the mixer bias on pin 17. This is 1.7 V with no input signal and 0.6 V with large input signals. The circuit also includes mute, a tuning meter, and an AFC output to the F-M tuner.

Dwg. No. B-1451

Figure 7

6

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┌─────────────────────────────────────────────────────────────┐
│                  PARTS LIST FOR FIGURE 7                       │
│                                                                │
│   F1    SFE10.7MA, F-M I-F Filter                              │
│   F2    CFZ455C, A-M I-F Filter                                │
│   Q1    MPS3563, F-M Converter                                 │
│   Q2    MPSH-04, A-M R-F Amplifier                             │
│   T1    Ferrite Loop, 571 μH, Qu = 150, 17:1 turns ratio       │
│   T2    RWO-6A7640BM, A-M Osc., Qu = 50, 11:1 turns ratio      │
│   T3    RLCS-4A7893GO, A-M Det., 256 μH, Qu = 75, 5.4:1 turns ratio │
│   T4    BKAC-K3651HM, F-M Det., Qu = 65                        │
│   T5    BKACS-K4551AO, F-M Input, Qu = 90, 7:1 turns ratio     │
└─────────────────────────────────────────────────────────────┘
```

Low-Cost Receiver Design

A simplified receiver design illustrated in Figure 8 can produce excellent performance at very low cost using Type ULN-2241A. This simple A-M/F-M system uses a Type ULN-2283B audio amplifier and a Toko CY2-22124 PT Polyvaricon type of tuning capacitor.

The A-M section tunes from 540 to 1610 kHz. The ferrite antenna T1 has an inductance of 571 μH, and 6 turns on the secondary. Twenty dB quieting sensitivity is 180 μV/m and the maximum signal is about 1.0 V/m. The A-M oscillator is a negative resistance type needing only an impedance greater than 1.5 kΩ across pins 9 and 15 to oscillate. The oscillator coil T2 has been designed for a secondary impedance of about 5 kΩ.

In order to obtain good A-M selectivity, a low-cost ceramic I-F filter F2 and a relatively high-Q detector coil T3 are used. The tap impedance T3 is 4.7 kΩ.

The CFZ455C filter F2 contains a tuned circuit and ceramic resonator and has sufficient input impedance for a good mixer gain. It must be loaded with 2 kΩ. The output capacitance of 250 pF at 10.7 MHz is large enough to terminate the F-M I-F filter F1 through 330 Ω. A slightly better termination for F1 can be produced using a small inductance (0.88 μH) placed in series with the output of F2, the 455 kHz filter. At 10.7 MHz, this inductance will form a series resonant circuit with the F2 output capacitance.

The single-tuned detector coil T4 is easily aligned by simply tuning for maximum audio output. Note that AFC has been included even though Type ULN-2241A has no AFC output pin. It is only necessary to filter the audio output at pin 5 with a 1 MΩ resistor and a 0.05 μF capacitor for AFC.

The F-M tuner design is relatively straightforward, except: the autodyne converter is designed so that the F-M oscillator signal does not appear across the primary of the mixer coil T5, and the oscillator coil is grounded. This circuit configuration prevents the F-M oscillator signal from coupling across T5 through F1 into the ULN-2241A (pin 1). Excessive oscillator input would cause the limiters to be driven by the oscillator producing undesirable offsets with weak signals.

Note the AGC output of Type ULN-2241A is used to drive the R-F amplifier Q1. This eliminates any problems with large signals overdriving the converter Q2. Consequently, the oscillator frequency in this tuner will not change even when the input voltage rises as high as 300,000 μV.

LOW-COST TUNER PERFORMANCE CHARACTERISTICS
(Figure 8)

F-M
20 dB (S + N)/N = 5 μV
f_0 + I-F/2 = 64 dB
Image = 27 dB
1 dB Limiting = 10 μV
Interstation Noise = 20 dB below 30%
A-M
20 dB (S + N)/N = 180 μV/m

Figure 8

6

PARTS LIST FOR FIGURE 8

D1	Siemens TA314, F-M Varactor Diode
F1	SFE10.7MA, F-M I-F Filter
F2	CFZ455C, A-M I-F Filter
Q1	MPS3563, F-M R-F Amplifier
Q2	MPS3563, F-M Converter
T1	Ferrite Loop, 571 μH, Qu = 150, 17:1 turns ratio
T2	RWO-6A7640BM, A-M Osc., Qu = 50, 11:1 turns ratio
T3	RLCS-4A7893GO, A-M Det., 256 μH, Qu = 75, 5.4:1 turns ratio
T4	BKAC-K3651HM, F-M Det., Qu = 65
T5	BKACS-K4551AO, F-M Input, Qu = 90, 7:1 turns ratio

Low-Cost Automobile Radio

Automobile radios usually have two tuned R-F circuits in addition to the local oscillator. In this case Type ULN-2242A can be used in an A-M/F-M automobile radio without an A-M R-F amplifier. The R-F circuit can be double-tuned with minimal loss in sensitivity. The inductive tuning circuit is easily connected to the mixer of Type ULN-2242A as shown in Figure 9.

Note that L51 and L53 are not tapped and only the oscillator coil L55 needs a secondary winding. The 150 μH coil L54 forms an inductive tap with L53 to provide a desired sensitivity and

overload level. The A-M sensitivity of the tuner with the 30 pF/30 pF dummy antenna shown is 10 μV for 10 dB (S + N)/N, and the maximum input at 80% modulation is 300 mV.

The I-F uses a ceramic filter and a single-tuned high-Q detector coil. The I-F collector load resistor of 150 Ω on pin 13 has been reduced from the usual 220 Ω (pin 9, Figure 8) to reduce the interstation noise and to increase the limiting level for better tuning feel. An F-M tuner of the designer's choice can be added to this circuit to form a complete A-M/F-M tuner.
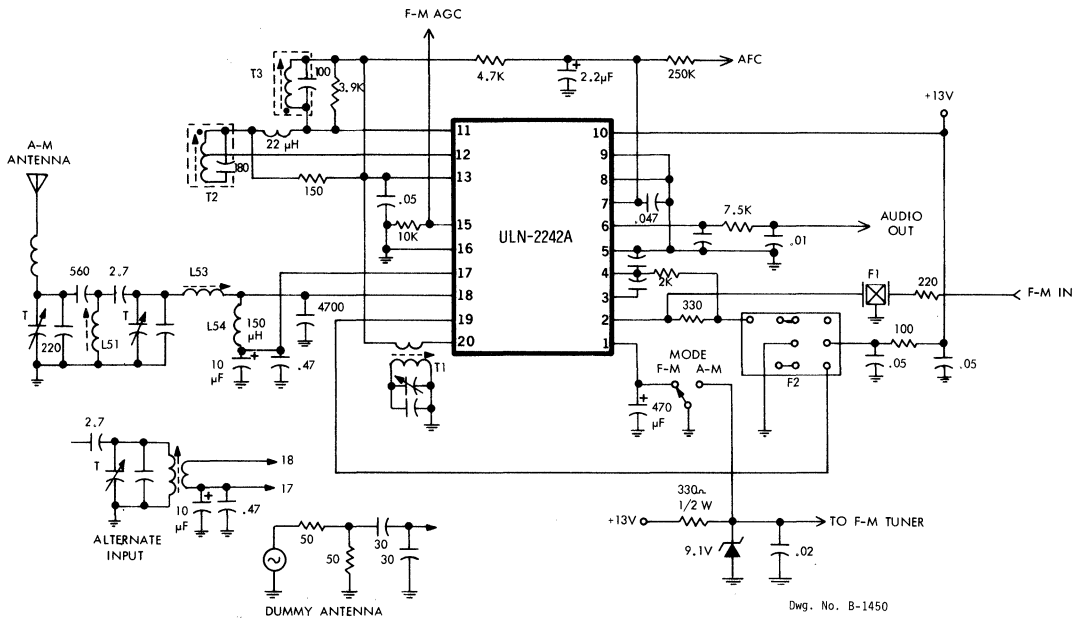
Figure 9

PARTS LIST FOR FIGURE 9

F1	SFE10.7MA, F-M I-F Filter
F2	CFZ455C, A-M I-F Filter
T1	RWO-6A7640BM, A-M Osc., Qu = 50, 11:1 turns ratio
T2	RLCS-4A7893GO, A-M Det., 256 μH, Qu = 75, 5.4:1 turns ratio
T3	BKAC-K3651HM, F-M Det., Qu = 65

LOW-COST AUTO RADIO PERFORMANCE CHARACTERISTICS (Figure 9)

A-M   10 dB (S + N)/N = 10 μV with 30% modulation
Maximum Signal = 300 mV with 80% modulation

6

Automobile Tuner With A-M R-F Stage

Improved sensitivity and excellent overload performance with the radio tuner illustrated in Figure 9 may be obtained by adding the R-F stage of Figure 10. A secondary winding has been added to L53 to couple it to the mixer of Type ULN-2241A. The emitter of the R-F stage is biased up to 0.5 V when it is turned OFF to im-prove the overload. This condition causes the R-F stage to be turned OFF at a lower R-F level. Large signals are not rectified in the R-F stage.

This circuit will handle input signals to 1 volt into the 30 pF/30 pF dummy antenna.
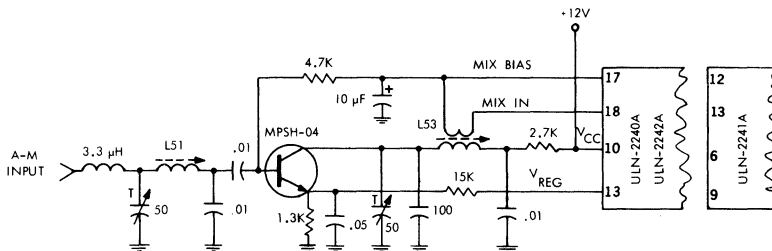
Dwg. No. A-11,325

Figure 10

Varactor-Tuned Automobile Radio

The tuner in Figure 11 was specifically designed for a digital synthesized A-M/F-M automobile radio. A large area, low-noise JFET, Q1, provides a reasonable broad-band match to the antenna. Tuning the antenna with a varactor diode would require a capacitance change of 9 times the total of antenna, input cable, minimum diode and stray capacitance. Because Q1 has about 5 pF feedback capacitance, Q3 is added to form a cascode input.

Q2 provides the interface between the AGC of Type ULN-2242A and Q1, reducing the g_m of Q1 by dropping the drain current as the signal level increases. This arrangement produces excellent large-signal and cross-modulation characteristics. L1 and R1 provide a static current discharge path for the antenna while L2 reduces interference from VHF signals.

T1, T2 and L4 form a double-tuned R-F circuit, an arrangement with several advantages over single-tuned circuits. The bandwidth is greater, especially at the low end of the band, so that receiver bandwidth is not determined by the R-F stages and image rejection is maintained. Mistracking caused by the matched tuning diodes is much less of a problem with the wider R-F bandwidth. The primary voltage of T1 increases as the receiver is tuned off a station, producing better local AGC action.

As the receiver is tuned off a strong station, the AGC supplied by Q2 is normally removed from the R-F stage Q1. Large signals applied to the diodes will cause oscillations heard as whistles when the receiver is tuned in and out of a strong station. Local AGC is therefore required, and is provided by Q4 and associated components.

Q4 is coupled to T1 by C2 and C3 so minimum additional capacitance is added to T1. The output of Q4 is rectified by a voltage doubler and filtered to remove audio frequencies produced by the voltage doubler. This arrangement coupled with the very good AGC characteristics of Type ULN-2242A, results in a receiver with large-signal capabilities better than most conventional automobile radios.

An A-M oscillator signal of about 200 mV at pin 20 can be used to drive a synthesizer if desired. Most synthesized radios mute the audio when changing stations. Since A-M and F-M are common in Type ULN-2242A, the mute works for both. A 3 to 4-volt signal applied to pin 8 will mute either A-M or F-M.

The A-M AGC and F-M mute signals applied to Q5 provide a stop signal for use with signal-seeking receivers. The collector of Q5 goes high when a signal is reached and is limited to 6.5 V to interface with 5 V digital logic circuits.

REFERENCES

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2. GrosJean, Jon P. "Phase-Locked Loops Using Quadrature Detector Integrated Circuits," *IEEE Transactions on Consumer Electronics,* February 1976, pp. 94-100.

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4. Richards, Oliver. "A Complete A-M/F-M Signal Processing System," *Sprague Technical Paper TP77-6.*

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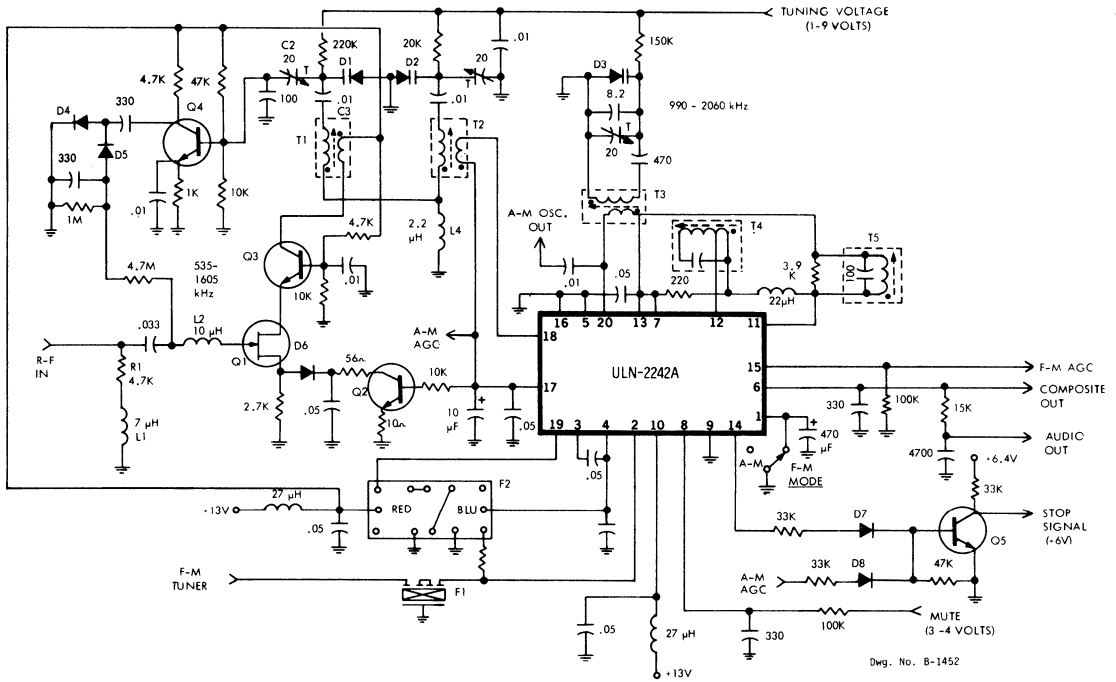
Figure 11

6

PARTS LIST FOR FIGURE 11

D1-3	Toko KV1215 or Sanyo SVC311 A-M Varactor Diode (3)
D4-7	1N914 or 1N4148 General Purpose Diode (4)
F1	SFJ10.7MA, F-M I-F Filter
F2	CFU455C, A-M I-F Filter
T1	RWOS-6A7894AO, A-M R-F, 178 μH, Qu = 120, 10:1 turns ratio
T2	RWOS-6A7894AO, A-M R-F, 178 μH, Qu = 120, 10:1 turns ratio
T3	RWOS-6A7892AO, A-M Osc., Qu = 120, Q1 = 80, 5:1 turns ratio
T4	RLCS-4A7893GO, A-M Det., 256 μH, Qu = 75, 5.4:1 turns ratio
T5	BKAC-K3651HM, F-M Det., Qu = 65
Q1	MPF820 A-M R-F Amplifier
Q2-5	2N4124 General Purpose Amplifier

THE ULN-2242A,
A COMPLETE AM/FM
SIGNAL PROCESSING SYSTEM

Introduction

This paper describes a monolithic integrated circuit which makes possible substantial simplification of AM/FM receiver design, while at the same time improving system performance.

Prior attempts at monolithic implementation started with the quadrature detector/IF gain block which was first described by A. Bilotti in 1967.[1] Other devices were developed for AM circuits which in essence attempted to combine the active elements of a descrete bipolar AM receiver. The resulting monolithic devices were capable of performance no better than the original discrete design, and with the very uneconomical displacement of three discrete transistors with one integrated circuit.

To achieve useful cost and performance objectives, a new monolithic AM/FM signal processing system[2] was designed with careful attention to the total system costs and performance objectives of modern automotive and high quality home entertainment broadcast receivers. In addition to providing state-of-the-art receiver performance, this "one-chip" receiver also provides for meter drive, interstation muting, delayed AGC (for control of external AM and FM RF stages), and simple AM/FM switching.

Circuit Description-AM Mixer

An analog multiplier is used for the AM mixer. It substantially outperforms discrete mixers in the areas of noise and spurious response rejection. As an AM mixer this circuit provides both local oscillator and received frequency rejection. The local oscillator is suppressed by approximately 40 dB and the intermediate frequency feedthrough is down by 26 dB. Spurious response suppression is important as a receiver performance objective, and also the receiver's ability to reject undesired noise passbands. The mixer's freedom from oscillator signal in
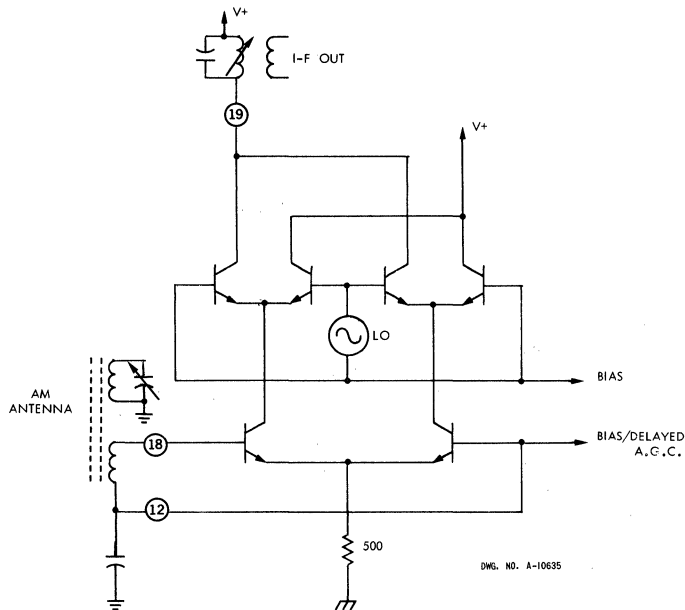
Figure 1

NOTE: This paper was originally presented at the IEEE Fall Conference on Broadcast and Television Receivers in Chicago, December 1977.

the IF also reduces the outband rejection requirement for the IF selectivity elements, simplifying the use of low-cost ceramic filters. The mixer current is chosen to provide 20 mmho of gain with an acceptable output overload capability.

The AM Detector

The AM signal is peak detected, recovering audio and a d-c voltage to control AGC. Low audio distortion of 1% is achieved by maintaining a relatively constant current and resistance load, presented by the emitter-base junction of Q82 as shown in Figure 2. The recovered audio is taken off in a balanced configuration and summed at a node to cancel stage current.

AM AGC

AM gain control is achieved by reverse AGC of the first IF by cutting off stage current to the first IF stage. AGC to the mixer is by the same method, but with a 14 dB delay to optimize gain distribution for noise considerations, and allow a better match to the input to the mixer. Gain reduction as a function of signal level is shown in the graph of Figure 3.

Combined AM/FM IF

Stacking of the AM and FM selectivity components allows the use of a common IF amplifier.

The IF (Figure 5) is a fully-balanced amplifier having each stage differentially coupled to the succeeding stage. In addition to providing a 6 dB per stage increase in gain over single-ended coupling, this maintains constant stage and emitter follower currents to prevent signal current from appearing in on-chip grounds or supplies. Attendant signals or noise appearing on ground or supplies will be rejected as common mode by the balanced stages.

The differential coupling approach also balances capacitive effects to minimize phase delay modulation with various signal levels. To further control AC effects and reduce device input capacitance, the first IF stage is a cascode configuration to reduce Miller effect.

In the FM configuration, the IF stages are operated as limiters and provide 76 dB of gain with a corner frequency of 36 MHz. Coupled with the detector section, the combination achieves a 3 dB limiting threshold of 15 μV.
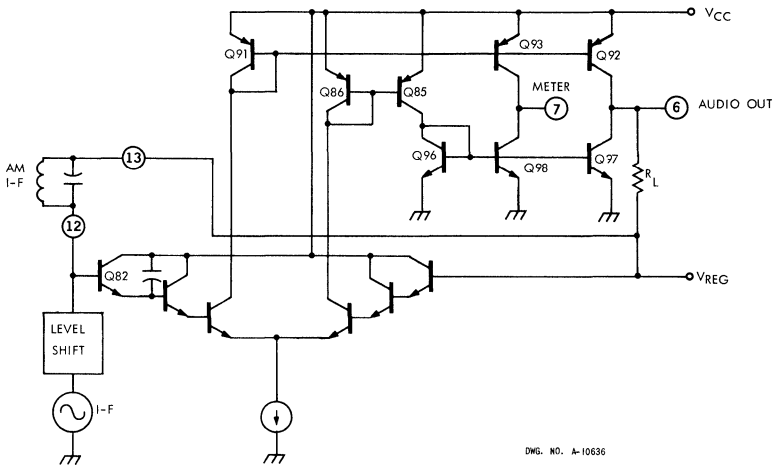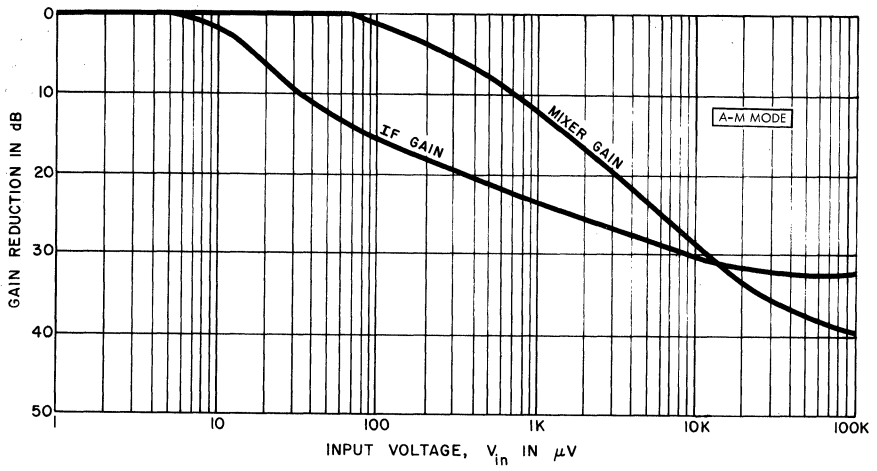
Figure 2

DWG. NO. A-10637

Figure 3

DWG. NO. 8-1369

Figure 4

DWG. NO. A-10638

Figure 5

6
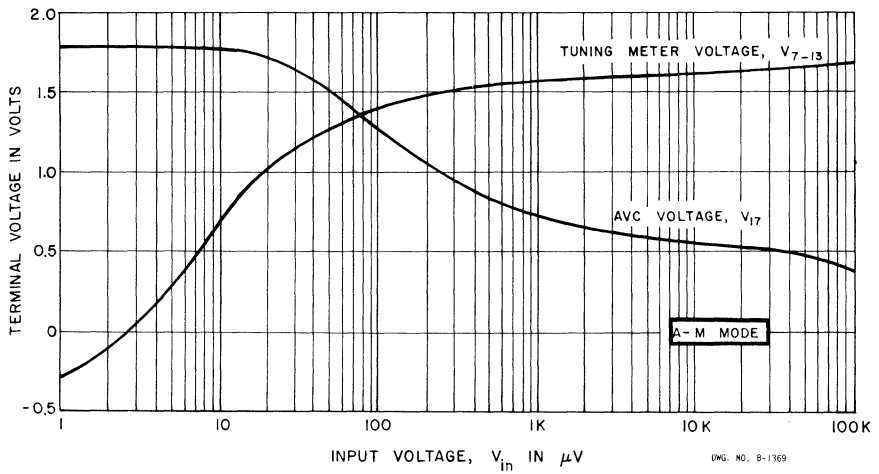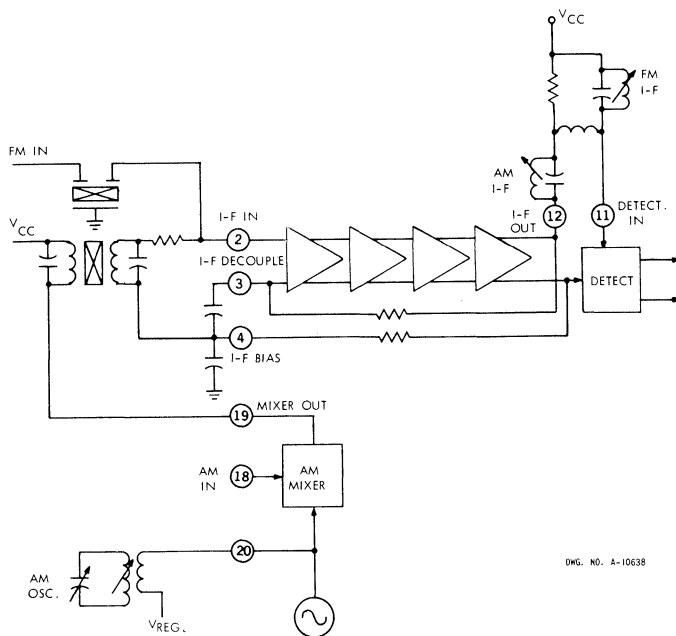
AM operation utilizes the same IF section as used for FM with a gain reduction and redistribution. To accomplish this, stage current is reduced in the second, third, and fourth IF stages. This puts 20 dB of gain in the first, and only 6 dB total in the remaining three stages, and also maintains a reasonably low input impedance to the IF.

The FM Detector

The FM detector (Figure 6) is an analog multiplier operating in the high-level injection mode. In this mode, a multiplier provides high recovered audio with low audio distortion. Like the IF, the detector is also driven differentially. In addition, the inphase and quadrature signals are passed through the same number of stages. This assures good freedom from a-c offset, i.e. detector d-c offset caused by unequal phase delay in the two applied signals.

Recovered audio is processed through the same current mirrors, summing resistor, and output pin as was used for AM. AFC and meter information is provided open collector for use with an external load. This allows the AFC to be used with any reference voltage between V+ and ground, and also permits adjustment of AFC gain by the choice of load resistor value.

FM Mute and AGC Detectors

The mute and AGC provide d-c voltages for control of signal level related functions. The basic detector (Figure 7) is biased as a triple Darlington current source, with a quiescent state value of 10 μA. Detector operation is accomplished by applying an a-c signal to C3 which forms a voltage doubler with the emitter-base junctions of Q61 and Q62 plus the smoothing Miller capacitors of convenient size for integration.
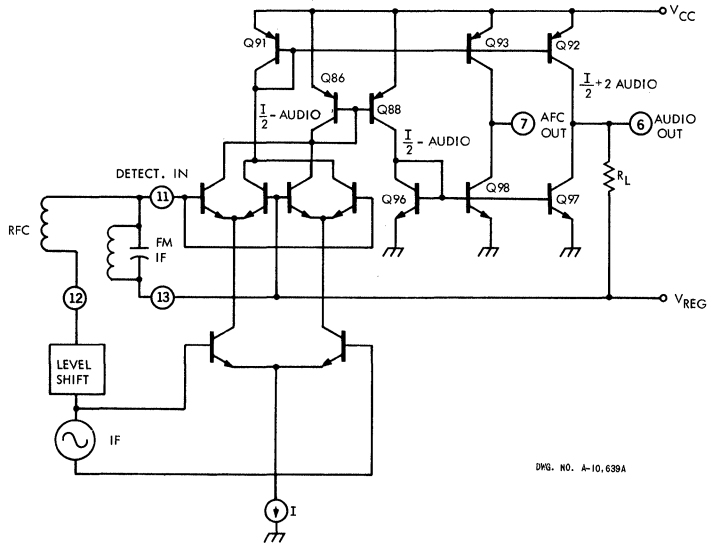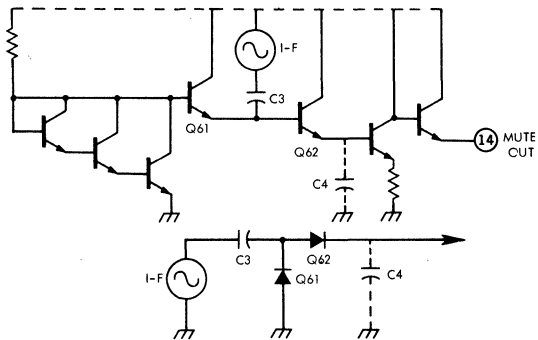
Figure 6

Figure 7

Signal for the mute detector is taken out of the quadrature coil to limit bandwidth and allow mute detector operation at the approximate limiting threshold of the device. The mute attenuation is obtained by cutting off the current mirrors to the audio. This achieves greater than 60 dB of attenuation with a minimum disturbance in d-c levels.

The AGC detector is basically the same as the mute detector, with the exception of the source of the a-c signal. This detector responds with a 2 mV signal input. Both detectors are biased to a no-signal value of 4.7 volts, and approach zero with increasing signal input as shown in Figure 8.

Typical Application

Figure 9 illustrates a typical home entertainment receiver application for this new AM/FM signal processing system.

Sufficient FM IF gain is provided by the device to eliminate the need for any additional external gain besides that of the tuner. A 3 dB limiting sensitivity of about 2 μV is easily achieved.

All AM signal processing is performed within the device. The gain AGC and noise performance of the device in the AM mode is sufficient to achieve a useable sensitivity of 150 μV/m while featuring an overload capability of 2 V/m with a 15 cm ferrite antenna.

Conclusion

Much of the original design for this new device was to define its operation as a system rather than as a simple component. To achieve the same revolutionary impact in AM/FM radio receivers as the design by A. Bilotti did for FM only, the new device required more than simple assembly of discrete components into an integrated circuit. Despite the integrated circuit's limitations on pin count and component values, the monolithic process with ion implantation is capable of fabricating superior circuit implementations such as fully-balanced mixers, multi-rate AGC systems, linear AM detectors, etc. at costs comparable to inferior circuits constructed with discrete components.
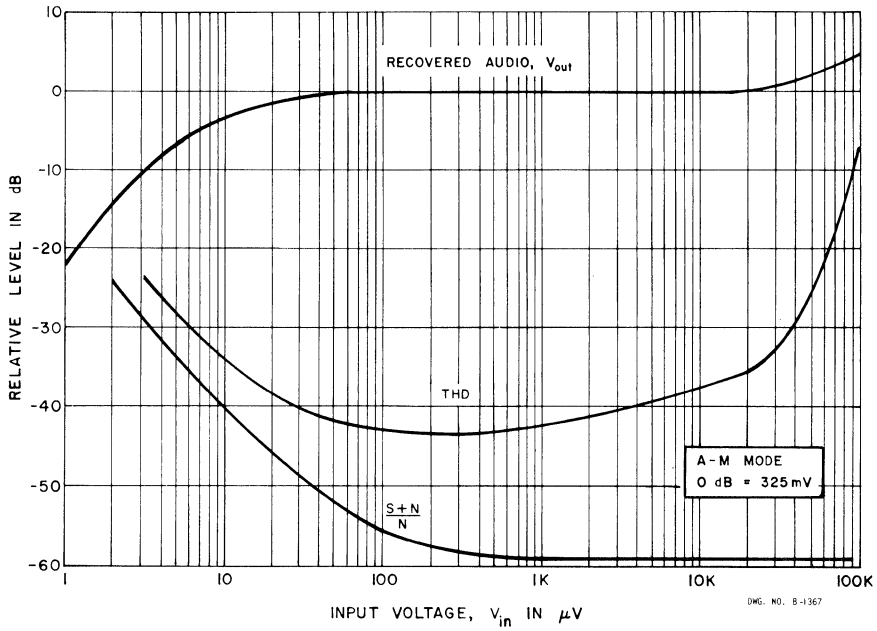

Figure 8

Figure 9

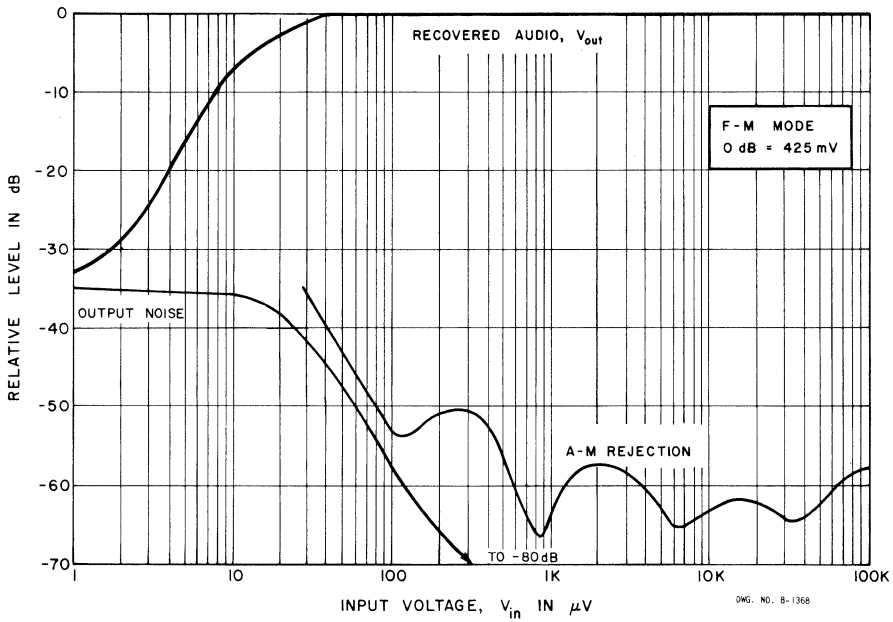The device is most often specified in a standardized test fixture, eliminating as many variables as possible including AM antenna and FM tuner characteristics. Typical overall performance in such a fixture is illustrated in the following curves.

This new monolithic AM/FM signal processing system which has been described, provides the radio designer with a modern cost-effective approach to

the "one-chip" radio receiver without the performance tradeoffs so common with previous AM/FM integrated circuits.

(1) A. Bilotti and R. S. Pepper, *A Monolithic Limiter and Balanced Discriminator for FM AND TV Receivers,* National Electronics Conference, October (1967).

(2) Sprague Electric part number ULN-2242A.

Figure 10

Figure 11

DEVELOPMENT OF HIGH-QUALITY RECEIVERS
FOR A-M STEREO

Introduction

Almost all current designs for A-M receivers or tuners use a ferrite antenna and/or a tuned R-F stage with one or two separate tuned R-F circuits. These are basically just slight modifications of the old five-tube radio. Because of this, almost all literature written on the subject of A-M receiver design was written when large tube-type receivers were popular.

When a receiver must have an audio-frequency response greater than about 4 kHz, this arrangement is not satisfactory and a new approach is required. This does not, however, necessitate the design of new integrated circuits for the R-F and I-F portions of high-quality A-M stereo tuners. Presently available integrated circuits can be used (with minor circuit variations) to produce A-M tuners with performance that compete with that of the receiver's F-M section.

Design Parameters

A-M stereo testing of many different types of A-M receivers indicates that receivers performing well with monophonic signals also perform well with stereophonic signals. A good criterion appears to be total harmonic distortion and audio frequency response. In addition to the usual requirements of good sensitivity, selectivity, image rejection, and the ability to handle large signals, distortion, signal-to-noise ratio, and audio fidelity are important parameters when designing A-M receivers for stereo or mono. Fortunately, if the I-F filter response can be kept symmetrical, current A-M integrated circuits will give very low distortion for a large range of signal levels. In addition, most of them have also had their gains apportioned properly so that under AGC conditions, signal-to-noise ratios are not degraded and high ultimate S+N/N ratios can be reached. This eliminates some problems for the designer, but does not solve all of the possible problems.

As a guide, the following receiver parameters have been chosen: (The modulation is 30% at 1 kHz unless otherwise noted.)

1. 20 dB S+N/N ≤ 200 μV/M
2. Adjacent Channel Attenuation ≥ 35 dB
3. Image Rejection ≥ 50 dB
4. Maximum Input Signal 1 V/M
5. THD < 0.5% and 1% at 80% Modulation
6. Maximum S/N ≥ 50 dB
7. Audio Response: 20 Hz - 15 kHz

Unfortunately, items 2 and 7 are incompatible with channel spacings of 10 kHz, so either a dual-bandwidth I-F or poorer frequency response must be accepted.

I-F Filters

The audio distortion and receiver selectivity are essentially determined by the I-F filter of a receiver. (Some other factors degrading the audio frequency response will be discussed under R-F circuits.) The traditional approach of using LC networks in a good quality receiver becomes very difficult because of Q limitations.

As an example, consider a transitional filter with a 40 dB bandwidth of 20 kHz and center frequency of 455 kHz.

Number of Sections	Max. 3 dB BW	Min. Coil Q
3	3.2 kHz	211
4	5.0 kHz	180
5	6.7 kHz	238
6	8.0 kHz	322
7	9.1 kHz	411
8	10.5 kHz	483

The maximum available coil Q is only about 140, so it is almost imperative that the I-F filter be a ceramic filter designed specifically for that purpose. Suitable communications ceramic filters are available, but at a cost 3 to 10 times greater than that of standard I-F transformers. There is, however, a good compromise available. Reasonably priced ceramic ladder filters with zeros in their transfer function are available with the following response (Figure 1):
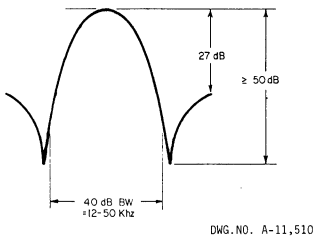

27 dB

≥ 50 dB

40 dB BW
≃12-50 Khz

DWG. NO. A-11,510

Figure 1

The zeros can be selected to fall at ±10 kHz for narrow-band I-Fs, and at ±20 kHz for wide-band I-Fs. The minimum attenuation beyond the zeros of only 27 dB is too small, but this falls within a range where supplemental inductive filters can be used. This requires buffers between the coil and ceramic filters, but, as we shall see later, some integrated circuit designs easily accommodate this arrangement.

It has been found by experiment that a full 20 kHz or even 15 kHz audio response is not necessarily desirable in a high quality A-M tuner, and might even be undesirable. So much background noise and interference from other stations is present even during local daytime listening that a narrower bandwidth is more acceptable. A good compromise appears to be about 20 kHz for 3 dB bandwidth. This is degraded by other filtering in the set plus the necessary 10 kHz notch filter in the audio output to give an overall audio frequency response of about 7 to 8 kHz. In the narrow bandwidth mode for nighttime listening, the ±10 kHz attenuation must be greater than 40 dB, restricting the audio response to about 4 kHz. It should be noted that this is considerably better than the 1.6 kHz to 3 kHz audio response of current receivers.

R-F Circuits

The R-F circuits of a high-quality A-M tuner present difficult challenges. The first occurs because the R-F stage bandwidth should not degrade the audio

frequency response. A few calculations will demonstrate the problem:

If the R-F circuit loaded Q is 60:
1400 kHz — 3 dB BW = 23 kHz, Audio = 12 kHz
At 600 kHz — 3 dB BW = 10 kHz, Audio = 5 kHz
600 kHz Image rejection = 48 dB

If the Q of the ferrite antenna or R-F tuned circuit is reduced to improve the audio response, the image rejection suffers. In the case of the ferrite antenna, the sensitivity also suffers:

$$E_g = \frac{n\mu Af}{60} E \qquad V = QE_g$$

V = Voltage Across Antenna Circuit
n = Number of Turns
μ = Antenna Permeability
A = Antenna Cross Sectional Area
f = Received Frequency
Q = Antenna Q
E = Electric Field Strength
E_g = Induced Voltage

This situation can be improved by using a large loop of a few turns of wire. In this case, the formula is the same with μ being replaced with μ_o. This antenna must, however, be very large in cross-sectional area (typically 1 m^2) before it is effective. It is also directional.

The only other alternative is the old-fashioned wire antenna which turns out to be much better in terms of signal reception. For this type:

$$E_g = \frac{\ell}{2} E \qquad V = Q E_g$$

ℓ = Antenna Length

Now, the received signal can be increased to offset reduced Q simply by making the wire longer.

This still leaves the problem of how to deal with the loss in image rejection when the R-F circuit Q is reduced. The most obvious solution is to use a double-tuned R-F circuit. This can be manipulated to have constant bandwidth with different center frequencies so almost any desired result (without severe loss in image rejection) can be obtained. Additionally, the wider R-F bandwidth reduces tracking problems which are not usually serious for A-M mono signals, but which will cause problems with A-M stereo signals because of the group delay variations they produce.

6

This leaves two possibilities for antenna input circuits:

1. Couple the antenna directly to the double-tuned circuit and suffer a 6 dB insertion loss.
2. Use an untuned FET input and put the double-tuned circuit between the FET and the mixer.

Option 2 also eliminates the need for an antenna trimming capacitor. This can be a significant cost savings in automobile receivers. In both cases, however, the Q of the antenna circuit will be quite low at the low end of the A-M band, and the receiver will have somewhat poor I-F rejection. This can easily be solved by using an integrated circuit with a double-balanced mixer.

Receiver Designs

Illustrations of two high quality A-M tuned designs which use currently available parts are shown in Figures 2 and 3.

Both achieve the following performance levels.

$$20 \text{ dB} \quad \frac{S+N}{N} \quad 100 \ \mu V/m$$

(depends on antenna length)

Image Rejection = 55 dB
— 3 dB audio frequency response from 550 to 1600 kHz:
   wide — 7.5 kHz
   narrow — 4 kHz
THD < 0.5% at 30% modulation
Maximum signal level > 1V/m
Max signal-to-noise at 30% modulation = 47 to 50 dB

The first design shown in Figure 2 uses a combination A-M/F-M integrated circuit (1) with a balanced mixer for A-M. A junction FET must be used for the R-F stage to obtain a reasonable sensitivity (MOSFETs are very noisy at these low frequencies), but since it has a high feedback capacitance, a transistor is also used to form a cascode stage. AGC is derived from the IC and is used to reduce the current of the R-F stage. Since the IC has enough gain, the R-F stage gain can be kept low to reduce overloading. The ceramic filters in the IF stage are separated by low-cost buffer transistor stages which also perform the bandwidth switching. Added to the ceramic filters are double-tuned input (pin 14) and output coils (pin 1) to suppress the spurious responses of the filters.

The audio output terminal (pin 4) includes a 10 kHz notch filter and a 15 kHz low-pass filter to reduce unwanted noise in wideband operation. Note the simplicity of the double-tuned R-F filter. The two coils are identical and a mutual coupling capacitor is used to give greater coupling at low frequencies.

The second tuner shown in Figure 3 uses a very popular A-M-only integrated circuit (2). This IC, while not having a balanced mixer, has a separate I-F stage perfectly suited to driving the ceramic I-F filter. The R-F stage is slightly different here but retains the double-tuned interstage filter. The required R-F gain is higher because of the lower overall gain of the IC.

Instead of two double-tuned I-F filters, a 3-section filter is used and transistors are again used for bandwidth switching. The lowpass and notch filters are also retained in the audio output.

Conclusion

It has been shown that high-quality A-M tuners using existing monolithic integrated circuits can be designed and their cost is reasonable. They are suitable for driving A-M stereo decoders and should produce very good A-M mono or stereo results. In the case of the first tuner, the 455 kHz signal to the decoder can be taken from the last I-F collector, or from a secondary winding on the detector coil. A 455 kHz signal of high-enough level is somewhat harder to obtain from the second tuner. The easiest approach appears to be to amplify the approximately 5 mV detector input signal. The internal detector then serves to generate AGC signals.

The advent of A-M stereo may hopefully serve as a catalyst for the re-development of good A-M tuners which died out when the "all-American" five-tube table radio was first introduced.

References

(1) Sprague Type ULN2240,41,42A, or TDA-1090.
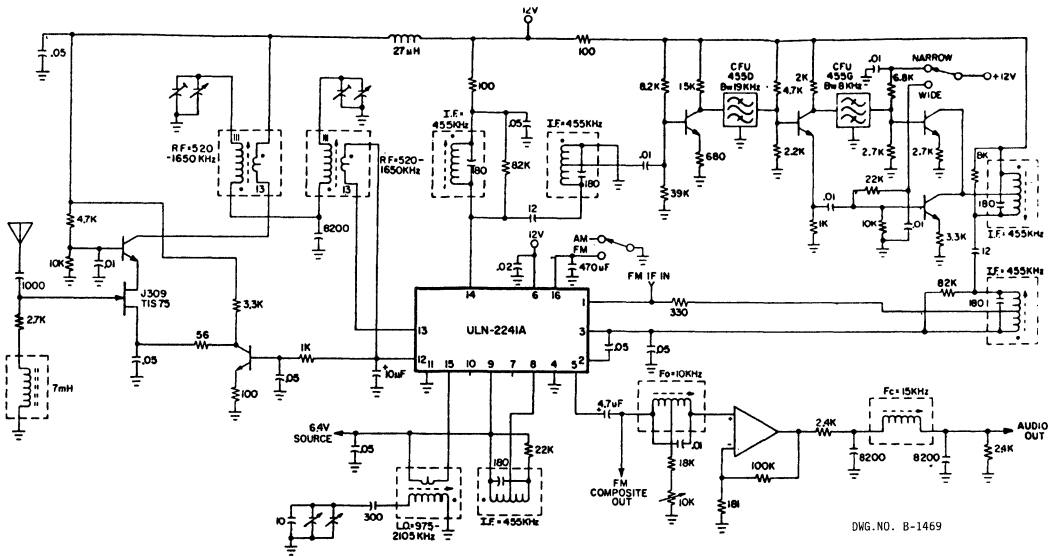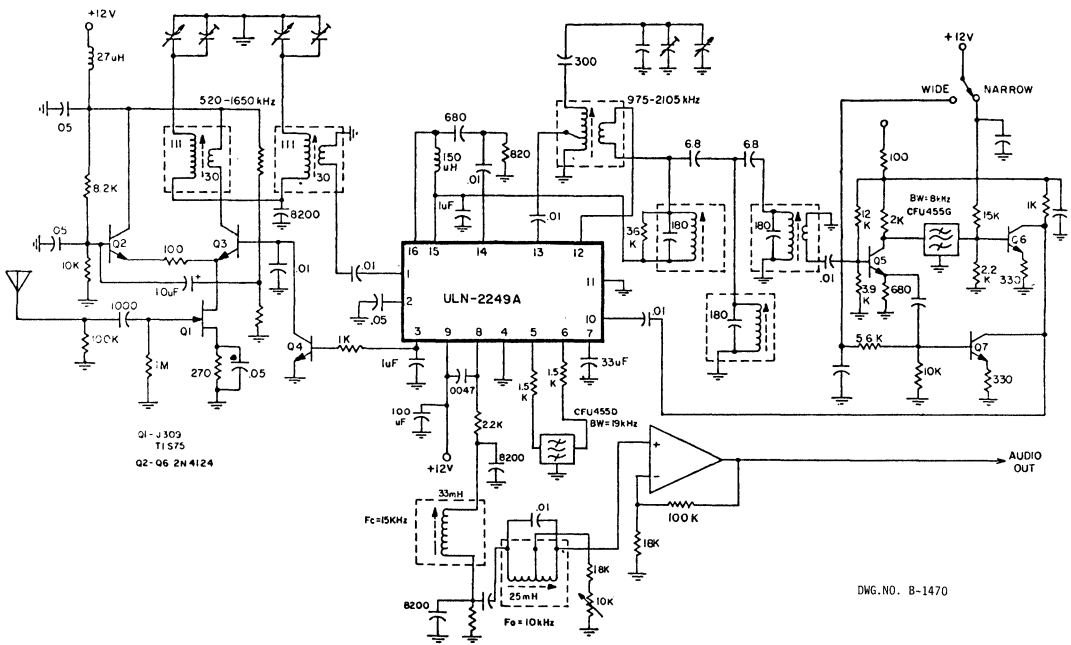(2) Sprague Type ULN2249A or HA1199

Figure 2

DWG.NO. B-1469

Figure 3

DWG.NO. B-1470

6—103

SECTION 7—VIDEO AND TELEVISION INTEGRATED CIRCUITS

7

SELECTION GUIDE TO VIDEO AND TELEVISION INTEGRATED CIRCUITS

Device Type	Chroma	Luma	Sound	Sync	Defl.
ULN-2260A	—	—	—	X	—
ULN-2270B/Q	—	—	—	—	X
ULN-2290B/Q	—	—	X	—	—
ULN-3702Z*	—	—	X	—	X

NOTE: Additional devices for use as sound channels may be found in Section 6. Audio amplifiers are described in Section 8.

*See page 8-22.

ULN-2260A AGC CONTROL,
SYNC SEPARATOR, AND SCAN PROCESSOR

FEATURES

- Excellent AGC Noise Immunity
- High Output Sync Level
- Balanced Phase Detector
- Stable Master Oscillator
- 16-Pin Dual-In-Line Plastic Package
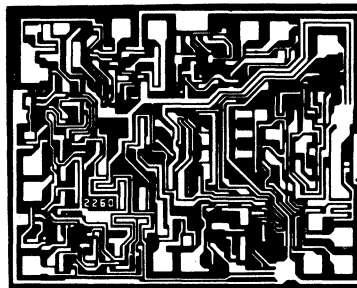
TELEVISION-CIRCUIT SIMPLIFICATION and high performance are primary advantages of designs using Type ULN-2260A. NTSC or PAL television receivers, color or monochrome, with countdown or conventional synchronization, can be flexibly and efficiently partitioned through use of this device.

The AGC detector of Type ULN-2260A employs a coincidence gate approach that minimizes noise effects. The circuit maintains constant AGC levels despite temporary losses of synchronization and temporary horizontal timing disturbances. The AGC-synchronization loop has both the high gain and high slew rate needed for fast channel-to-channel gain equalization and reduction of airplane flutter. Both forward and reverse delayed AGC currents are developed.

The sync separator uses an external passive network. The designer chooses the sampling level and time constants. The 10 Vpp output is short-circuit limited at approximately 25 mA.

The phase detector of Type ULN-2260A compares the sync separator's output to the integrated horizontal flyback pulse. Its output is a voltage proportional to the phasing error. Static phase error attributable to detector imbalance is minimized.

The designer is able to define the free-running frequency, control sensitivity and temperature compensation of the integrated circuit's oscillator. A wide range of frequencies can be generated, accomodating any of several TV or video display terminal deflection systems.

7

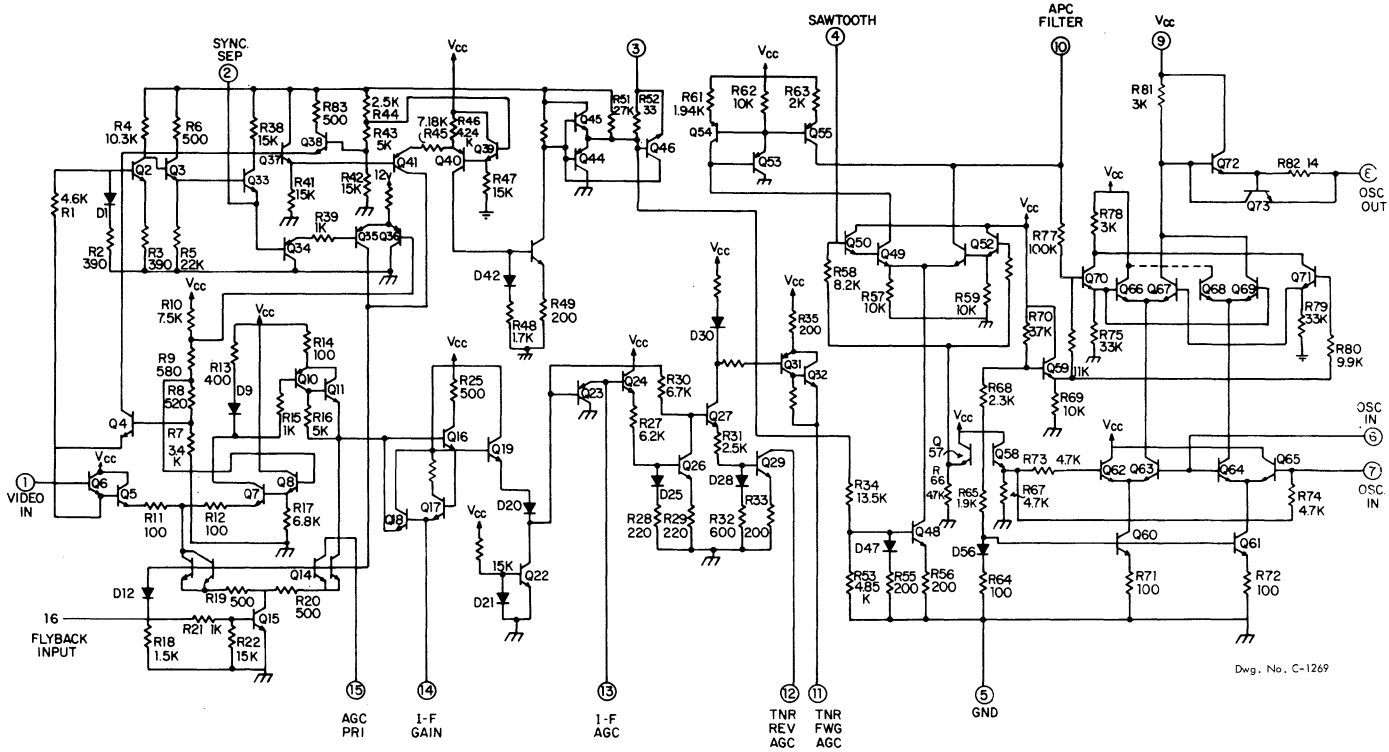# TYPICAL APPLICATION
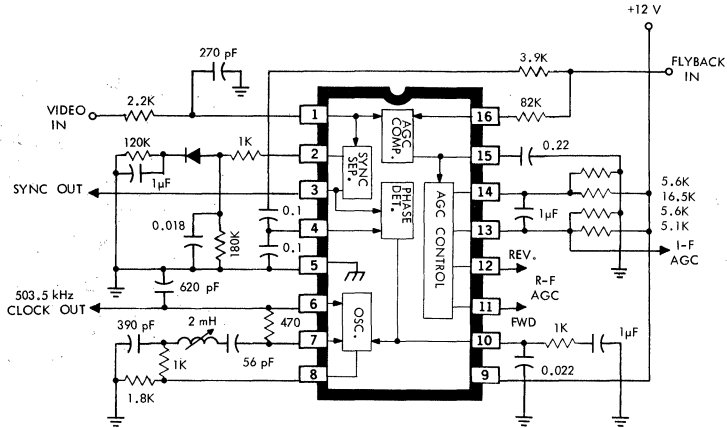
Dwg.No. A-11,225A

TYPICAL VCO CHARACTERISTIC
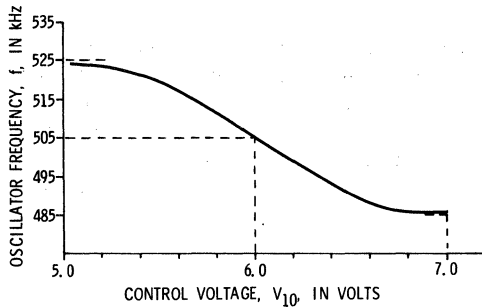
DWG. NO. A-11,221
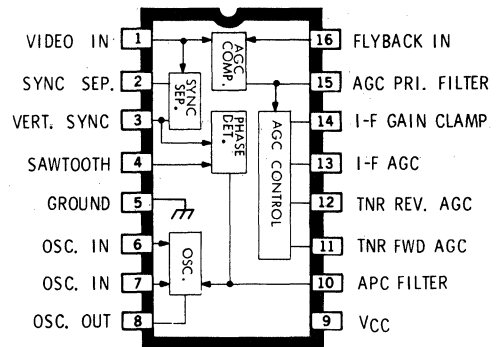
Pin	Label	Pin	Label
1	VIDEO IN	16	FLYBACK IN
2	SYNC SEP.	15	AGC PRI. FILTER
3	VERT. SYNC	14	I-F GAIN CLAMP
4	SAWTOOTH	13	I-F AGC
5	GROUND	12	TNR REV. AGC
6	OSC. IN	11	TNR FWD AGC
7	OSC. IN	10	APC FILTER
8	OSC. OUT	9	VCC

DWG. NO. A-11,223

SCHEMATIC

Dwg. No. C-1269

ULN-2270B AND ULN-2270Q/TDA1170
VERTICAL DEFLECTION SYSTEMS

FEATURES

- Internal Reference
- Positive or Negative Sync Input
- Vertical Ramp Generator
- Vertical Driver
- Flyback Generator
- Single-Supply Operation
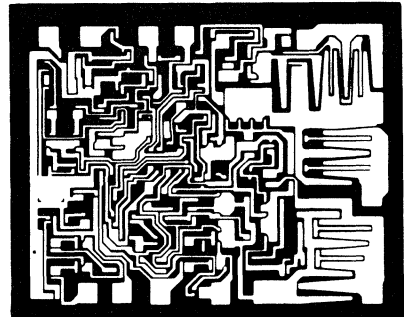
A S A SINGLE DEVICE containing a vertical oscillator, a flyback generator and a power amplifier, this vertical deflection system can greatly simplify design of black-and-white and small-screen color television receivers.

The oscillator of Types ULN-2270B and ULN-2270Q is directly synchronized by positive or negative sync pulses. A current feedback loop makes yoke current independent of yoke resistance changes caused by operating temperature variations. The flyback generator develops the high voltage required by the yoke for short flyback time and high efficiency.

Type ULN-2270B is supplied in a 16-pin dual in-line plastic package with heat sink contact tabs. Its copper alloy lead frame gives enhanced power dissipation ratings with standard cooling methods. Greater package power dissipation is available with attachment of an external heat sink to the webbed center leads of the device. The lead configuration makes possible easy attachment of a heat sink and use of a standard integrated circuit socket or printed wiring board layout.

Type ULN-2270Q/TDA1170 is supplied in a 16-pin quad in-line plastic package. It uses the printed wiring board on which it is mounted as a heat sink. Small heat sinks can also be attached to the center tabs of the device. The device carries the Sprague Electric Company part number (ULN-2270Q) unless the Pro-Electron marking (TDA1170) is requested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 27 V
Peak Flyback Voltage, V_6-V_7 .... 58 V
Sync Input Voltage, V_{10} .... ±12 V
Amp. Input Voltage Range, V_{14} .... −0.5 V to +10 V
Peak Output Current, I_6 (50 Hz, ≤10 μs) .... 2.5 A
            (50 Hz, >10 μs) .... 1.5 A
            (non-repetitive, 2 ms) .... 2.0 A
Package Power Dissipation, P_D .... See Graph
Junction Temperature Range, T_J .... −40°C to +150°C

For increased power-handling capability, these devices can be ordered in a 12-lead single in-line power-tab package by changing the part-number suffix from 'B' or 'Q' to 'W'.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_{CC} = 25\,V$, $f = 50\,Hz$ (unless otherwise specified)

Characteristic	Test Pin	Test Fig.	Test Conditions	Min.	Typ.	Max.	Units
Operating Supply Voltage Range	2			10	—	27	V
Sync Input Voltage	10	3	Positive or negative	1.0	—	—	V_p
Sync Input Resistance	10	3	$V_{10} = 1.0\,V$	—	3.5	—	$k\Omega$
Oscillator Bias Current	11	1		—	0.2	1.0	μA
Oscillator Voltage	11	3		—	2.4	—	V_{pp}
Oscillator Pull-In Range	10-11	3	Below 50 Hz	—	7.0	—	Hz
Oscillator Frequency Drift	11	3	$V_{CC} = 10\,V$ to $27\,V$	—	0.01	—	Hz/V
			$T_{TAB} = 40°C$ to $120°C$	—	0.015	—	Hz/°C
Ramp Generator Bias Current	16	1		—	50	500	nA
Amplifier Input Current	14	2		—	0.15	1.0	μA
Quiescent Output Voltage	6	1	$V_{CC} = 10\,V$, $R_2 = 10\,k\Omega$	4.0	4.4	4.8	V
			$V_{CC} = 25\,V$, $R_2 = 30\,k\Omega$	8.0	8.8	9.6	V
Flyback Voltage		3	$I_{YOKE} = 1.0\,A$	—	51	—	V
Flyback Time		3	$I_{YOKE} = 1.0\,A$	—	0.6	0.8	ms
Yoke Current		3		—	—	1.6	A_{pp}
Regulator Voltage	8 or 9	2		6.0	6.5	7.0	V
Line Regulation	8 or 9	2	$V_{CC} = 10\,V$ to $27\,V$	—	1.5	—	mV/V
Supply Current			$I_{YOKE} = 1.0\,A$	—	140	—	mA

NOTE: Pin numbering shown is in accordance with U.S. (JEDEC) practice where all positions are numbered (1 thru 16). European (Pro-Electron) practice is to skip the tab positions.

```
JEDEC        1  2  3  4    5    6  7  8  9 10 11  12   13  14 15 16
Pro-Electron 1  2  3  TAB  TAB  4  5  6  7  8  9  TAB  TAB 10 11 12
```

ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE
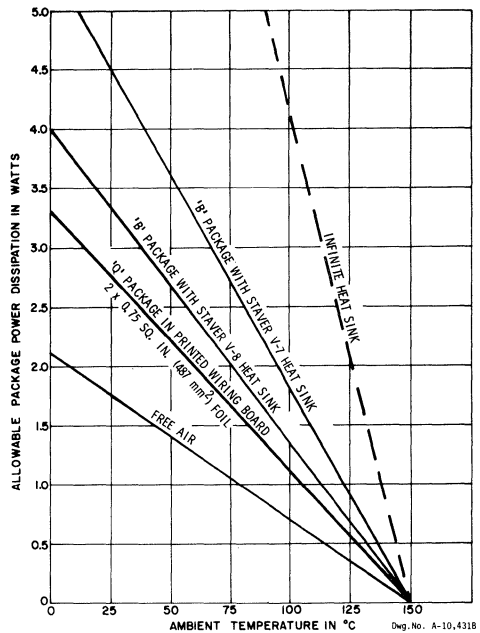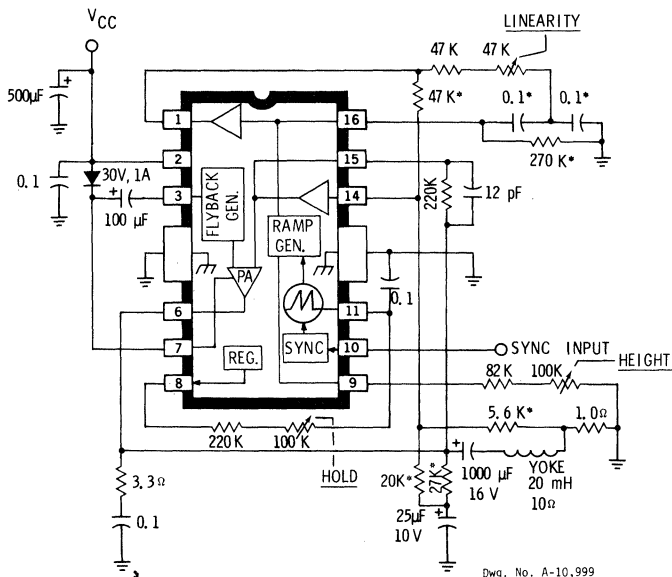
TEST FIGURES
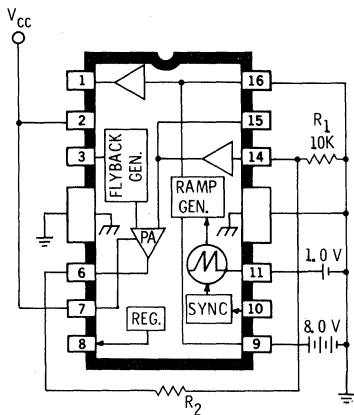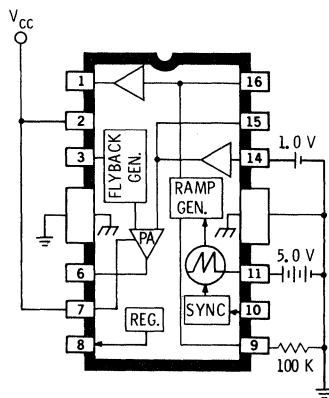
Figure 1

Figure 2

Figure 3

TYPICAL APPLICATION IN
LARGE-SCREEN BLACK-AND-WHITE TV

Supply Current, I_{CC} .... 140 mA
Flyback Time .... 0.75 ms
Yoke Current, I_{YOKE} .... 1.2 A_{pp}
Operating Supply Voltage Range, V_{CC} .... 20 V to 24 V
Package Power Dissipation, P_D .... 2.2 W
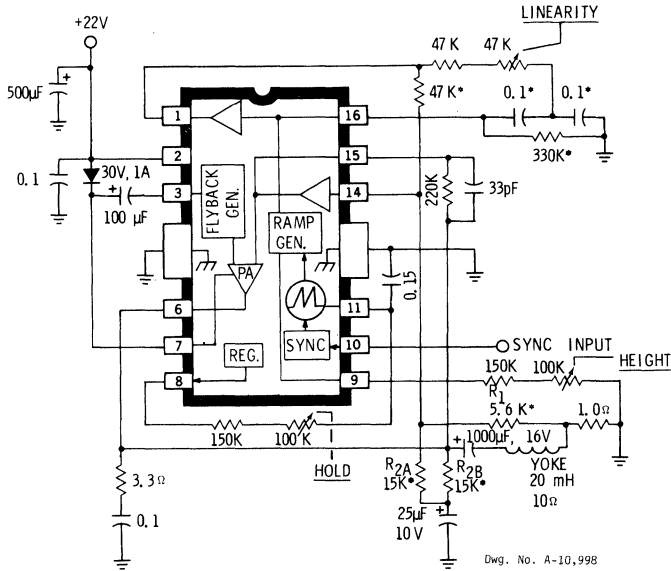
Dwg. No. A-10,998

*TOLERANCE ±5%

$$\text{Flyback Time} \approx \frac{2\, L_{YOKE}\, I_{YOKE}}{3\, V_{CC}}$$

$$I_{CC} \approx \frac{I_{YOKE}}{8} + 0.02$$

$$V_6 \approx V_{14}\, \frac{R_1 + R_2}{R_1}$$

Where:

Flyback Time is in seconds;

L_{YOKE} is in henries;

I_{YOKE} is the peak-to-peak current in amperes;

V_{CC} and V_6 are in volts;

I_{CC} is in amperes;

V_{14} is approximately 2.0 V.

TYPICAL APPLICATION IN
SMALL-SCREEN BLACK-AND-WHITE TV

Supply Current, I_{CC} .... 150 mA
Flyback Time .... 0.7 ms
Yoke Current, I_{YOKE} .... 1.15 A_{pp}
Package Power Dissipation, P_D .... 1.3 W

Dwg. No. A-11,000

*TOLERANCE ±5%

$$\text{Flyback Time} \approx \frac{2\ L_{YOKE}\ I_{YOKE}}{3\ V_{CC}}$$

$$I_{CC} \approx \frac{I_{YOKE}}{8} + 0.02$$

$$V_6 \approx V_{14}\ \frac{R_1 + R_2}{R_1}$$

Where:
      Flyback Time is in seconds;
      L_{YOKE} is in henries;
      I_{YOKE} is the peak-to-peak current in amperes;
      V_{CC} and V_6 are in volts;
      I_{CC} is in amperes;
      V_{14} is approximately 2.0 V.

CIRCUIT SCHEMATIC

Dwg. No. B-1437

FUNCTIONAL BLOCK DIAGRAM

Dwg. No. A-10,997
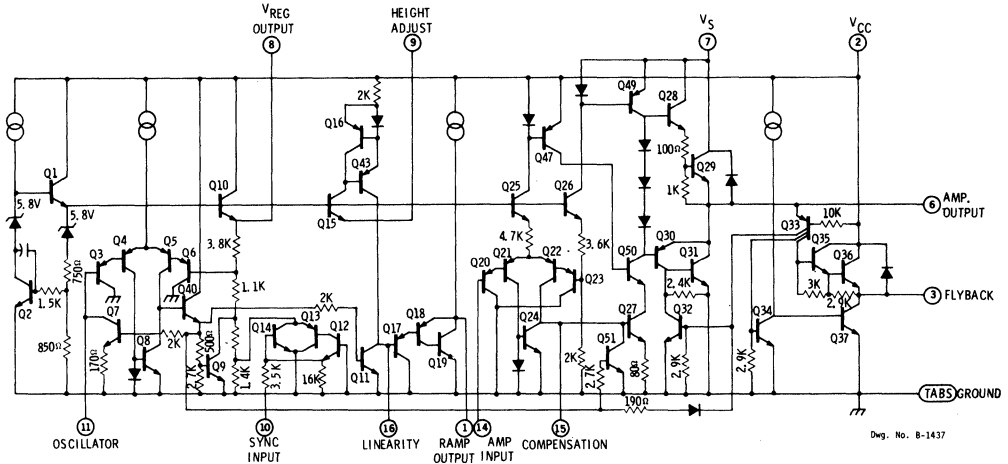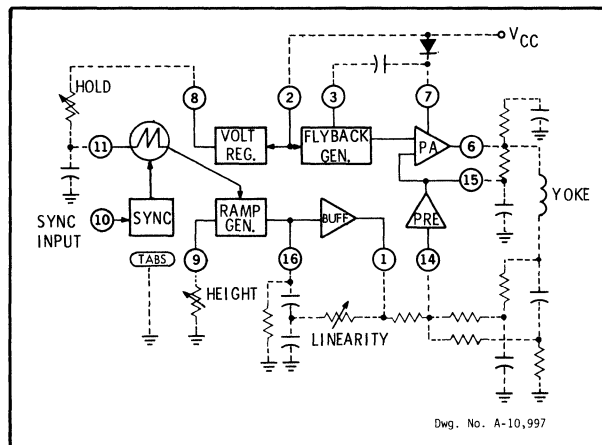
7

ULN-2290B AND ULN-2290Q
(TDA3190 AND TDA1190Z)
4-WATT TV SOUND CHANNELS

FEATURES

- High Sensitivity
- High A-M Rejection
- D-C Volume Control
- High Power Output
- Low Distortion
- Wide Operating Voltage Range (9 to 28 V)
- Low Quiescent Current Drain

CAPABLE OF CARRYING OUT all of the functions of a TV sound channel, the ULN-2290 silicon monolithic integrated circuit consists of a six-stage I-F amplifier/limiter, low-pass filter, differential peak detector, d-c volume control, regulated power supply, audio preamplifier and output stage.

The audio power amplifier will deliver 4 W of low-distortion audio to a 16Ω load with a supply of 24 V. When used with a 12 V supply, such as is found in many portable TV sets, these ICs will furnish 1.5 W to an 8Ω loud speaker.

This TV sound channel is available in either of two package configurations. Type ULN-2290Q is supplied in a quad in-line plastic package with a copper lead frame. This device is designed to use the printed wiring board on which it is mounted for heat dissipation and is identical to European Type TDA1190Z. It is marked with its Pro-Electron registration unless otherwise specified on production orders.
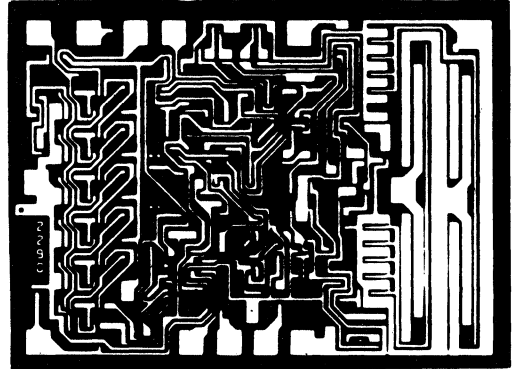
Type ULN-2290B is furnished in an improved 16-lead plastic dual in-line package with heat-sink contact tabs. The webbed lead configuration, originated by Sprague Electric, allows an inexpensive heat sink to be easily attached for increased power dissipation capability and yet permits the use of a standard IC socket or printed wiring board hole layout. This device is identical to European Type TDA3190.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}.................................+28 V
Repetitive Peak Output Current, I_{OUT}.................1.5 A
Package Power Dissipation, P_D..................See Graph
Junction Temperature Range, T_J..........—40°C to +150°C

FUNCTIONAL BLOCK DIAGRAM
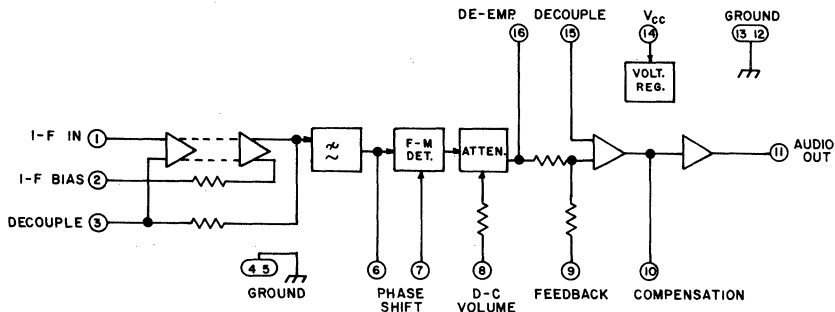
DWG. NO. A-10,433

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $f_o = 4.5$ MHz, $f_m = 400$ Hz, $f_d = \pm7.5$ kHz, $V_{CC} = 12$ V, $R_L = 8\Omega$, $V_{in} = 1$ mV (unless otherwise specified)

Characteristic	Symbol	Test Pin	Test Conditions	Limits			Units
				Min.	Typ.	Max.	
Quiescent Output Voltage	V_{OUT}	11	$V_{in} = 0$	5.1	6.0	6.9	V
Quiescent Supply Current	I_{CC}	14	$R_x = 22$ kΩ, $V_{in} = 0$	—	19	33	mA
Input Limiting Threshold	V_{TH}	1	$R_x = 0$	—	40	100	μV
A-M Rejection	AMR		$f_d = \pm25$ kHz, m = 0.3	40	55	—	dB
Signal-to-Noise Ratio	S+N/N		$P_{OUT} = 0.5$ W, $f_d = \pm25$ kHz	50	65	—	dB
Recovered Audio	V_{out}	16	$R_x = 0$	—	120	—	mV
Output Distortion	THD	11	$P_{OUT} = 50$ mW	—	1.0	—	%
Output Power	P_{OUT}	11	THD = 2%, $f_d = \pm25$ kHz	—	1.4	—	W
			THD = 10%, $f_d = \pm25$ kHz	—	1.5	—	W
Power Supply Rejection	PSR		f = 120 Hz, $R_x = 22$ kΩ, $R_L = 4\Omega$	—	46	—	dB
Input Resistance	R_{in}	1		—	30	—	kΩ
Input Capacitance	C_{in}	1		—	5.0	—	pF

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $f_o = 4.5$ MHz, $f_m = 400$ Hz, $f_d = \pm7.5$ kHz, $V_{CC} = 24$ V, $R_L = 16\Omega$, $V_{in} = 1$ mV (unless otherwise specified). **Heat Sinking is Required**

Characteristic	Symbol	Test Pin	Test Conditions	Limits			Units
				Min.	Typ.	Max.	
Quiescent Output Voltage	V_{OUT}	11	$V_{in} = 0$	11	12	13	V
Quiescent Supply Current	I_{CC}	14	$R_x = 22$ kΩ, $V_{in} = 0$	11	22	35	mA
Input Limiting Threshold	V_{TH}	1	$R_x = 0$	—	40	100	μV
A-M Rejection	AMR		$f_d = \pm25$ kHz, m = 0.3	40	55	—	dB
Signal-to-Noise Ratio	S+N/N		$P_{OUT} = 1.0$ W, $f_d = \pm25$ kHz	50	65	—	dB
Recovered Audio	V_{out}	16	$R_x = 0$	—	120	—	mV
Output Distortion	THD	11	$P_{OUT} = 50$ mW	—	0.75	—	%
Output Power	P_{OUT}	11	THD = 2%, $f_d = \pm25$ kHz	—	3.5	—	W
			THD = 10%, $f_d = \pm25$ kHz	—	4.2	—	W
Power Supply Rejection	PSR		f = 120 Hz, $R_x = 22$ kΩ, $R_L = 4\Omega$	—	46	—	dB
Input Resistance	R_{in}	1		—	30	—	kΩ
Input Capacitance	C_{in}	1		—	5.0	—	pF

7

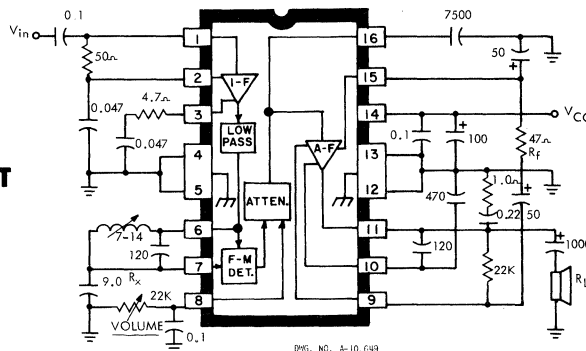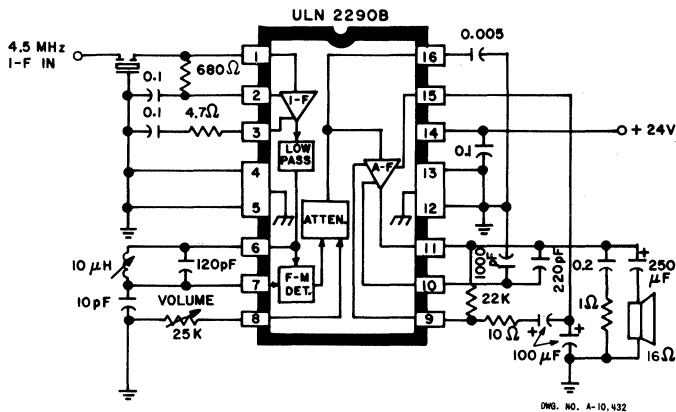**TEST CIRCUIT**

DWG. NO. A-10.049

TYPICAL APPLICATION
### (Heat Sink Required)

DWG. NO. A-10,432

NOTE: Pin numbering shown is in accordance with U.S. (JEDEC) practice where all positions are numbered (1 thru 16). European (Pro-Electron) practice is to skip the tab positions.

JEDEC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pro-Electron	1	2	3	TAB	TAB	4	5	6	7	8	9	TAB	TAB	10	11	12

Applications Information

1. Types ULN-2290B and ULN-2290Q have high input imped-ances, allowing them to be used with a ceramic filter or tuned circuit to provide the necessary input selectivity.

2. The electrical characteristics of these devices will remain relatively constant over the I-F frequency range of 4.5 MHz to 6 MHz. They can therefore be used with all common television standards.

3. The a-c gain of the audio amplifier is determined by the resistor ratio at pin 9. The gain should be defined in relation to the frequency deviation at which the output stage of the audio amplifier begins clipping.

4. The resistor between pins 9 and 11 can be replaced with various combinations of resistance and capacitance to provide bass boost or treble attenuation.

5. De-emphasis is determined by the capacitor connected at pin 16 and an internal 10 kΩ resistor. This pin can also be used to provide a treble-cut type of tone control.

6. The high-frequency audio cutoff is determined by the capac-itors connected at pin 10. To increase the audio bandwidth, reduce the values of these capacitors, keeping their ratio constant.

ALLOWABLE POWER DISSIPATION
AS A FUNCTION OF AMBIENT TEMPERATURE

ALLOWABLE PACKAGE POWER DISSIPATION IN WATTS

AMBIENT TEMPERATURE IN °C   Dwg. No. A-10,431B
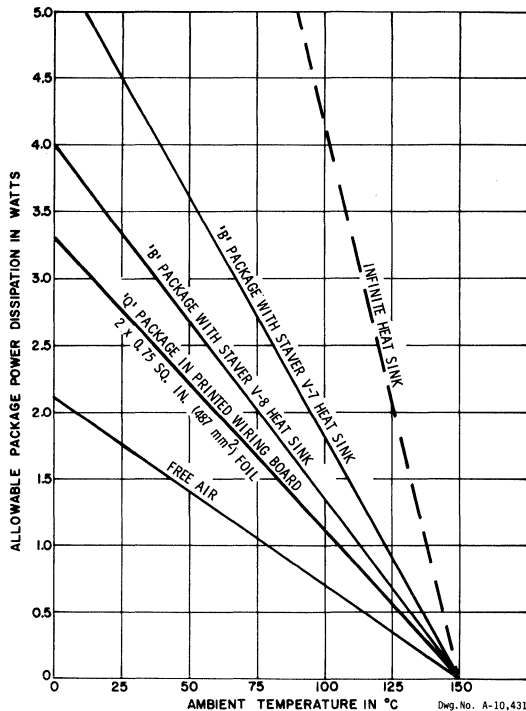
TYPICAL CHARACTERISTICS
at $T_A = 25°C$, $f_o = 4.5$ MHz, $f_m = 400$ Hz, $f_d = \pm25$ kHz, $V_{in} = 1$ mV
(unless otherwise shown)

AUDIO OUTPUT and NOISE
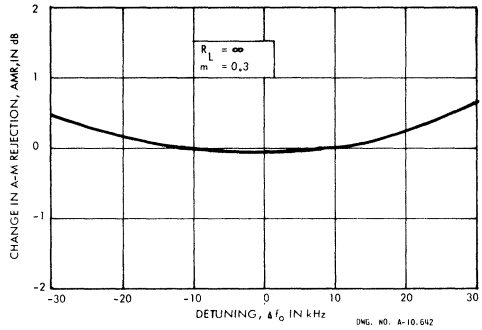### AS A FUNCTION OF INPUT VOLTAGE
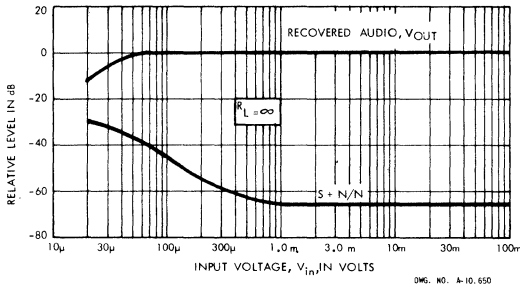
A-M REJECTION
AS A FUNCTION OF INPUT VOLTAGE
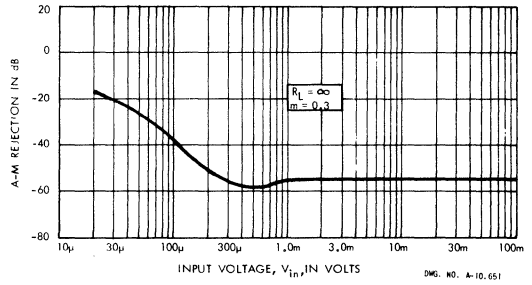
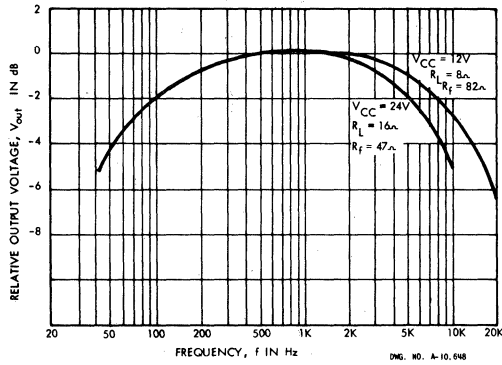## SOUND CHANNEL OUTPUT
AS A FUNCTION OF MODULATING FREQUENCY
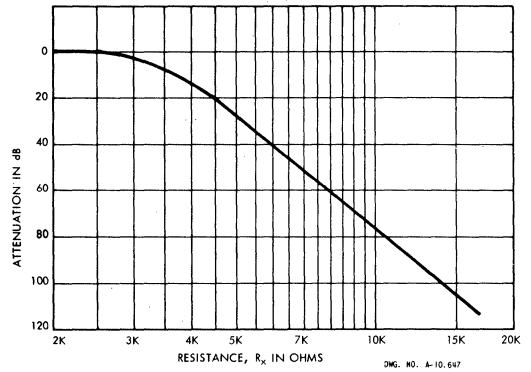

A-M REJECTION
AS A FUNCTION OF TUNING ERROR
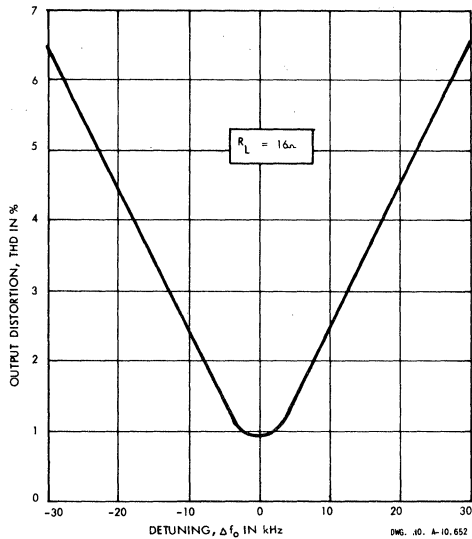

7
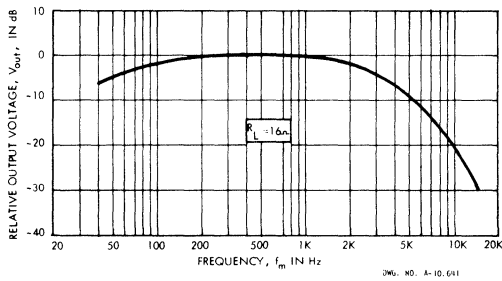
TYPICAL CHARACTERISTICS (Continued)
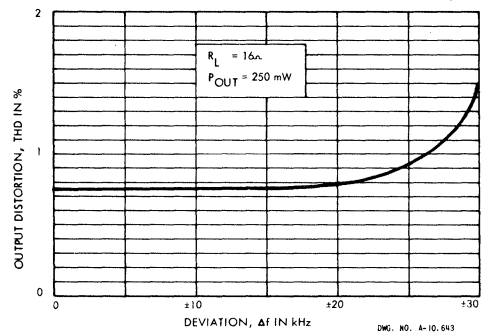
AUDIO AMPLIFIER OUTPUT
AS A FUNCTION OF FREQUENCY

ATTENUATION
AS FUNCTION OF RESISTANCE

DISTORTION
AS A FUNCTION OF TUNING ERROR

DISTORTION AS A FUNCTION
OF FREQUENCY DEVIATION

7—16

TYPICAL CHARACTERISTICS (Continued)
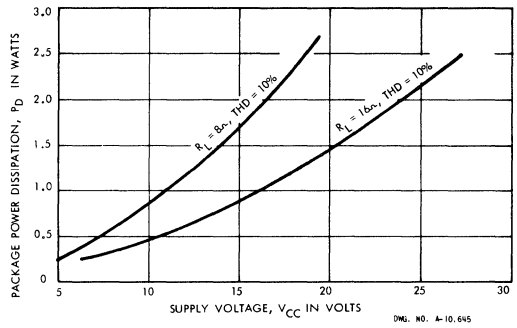
DISTORTION
AS A FUNCTION OF OUTPUT POWER
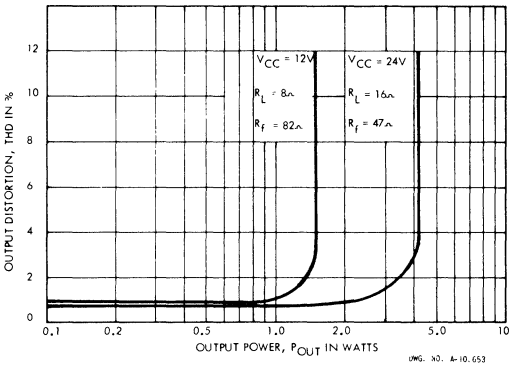
DISSIPATION and EFFICIENCY
AS FUNCTIONS OF OUTPUT POWER
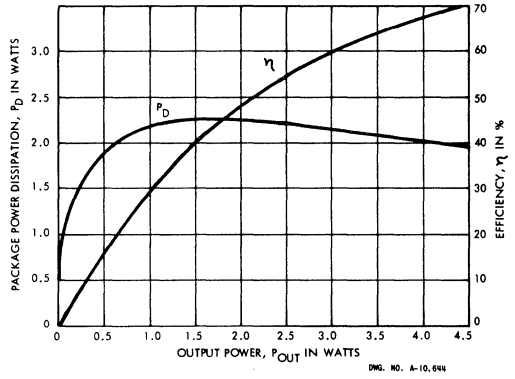
OUTPUT POWER
AS A FUNCTION OF SUPPLY VOLTAGE
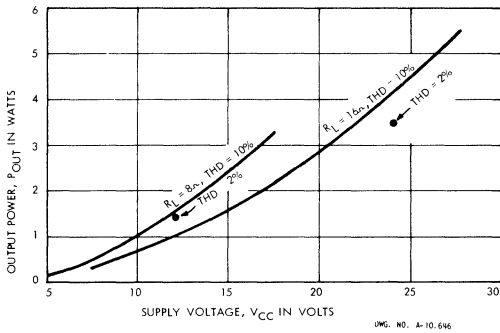
DISSIPATION
AS A FUNCTION OF SUPPLY VOLTAGE

DWG. NO. B-1381A

SCHEMATIC

THE ULN-2260A
SIGNAL, SYNC, AND SCAN PROCESSOR

Introduction

The monolithic integrated circuit provides high performance by careful selection of circuit techniques, and efficient partitioning of the AGC, sync separator, and master-scan phase-locked loop.

This grouping of circuit functions is particularly efficient. Since the video input is common to both AGC and sync separator, the separated sync can be internally coupled to the phase detector of the scan phase-locked loop; the flyback waveform is required for AGC gating and the phase detector.
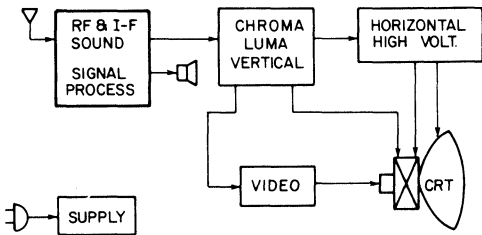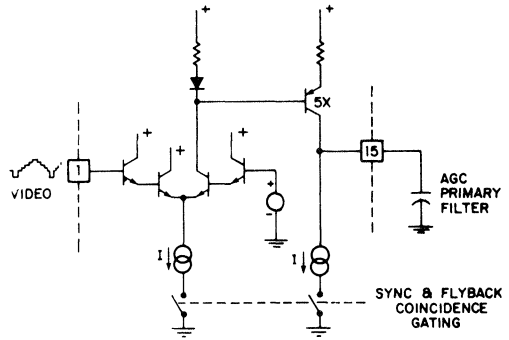

DWG.NO. A-11,484

Figure 1
RECEIVER PARTITIONING
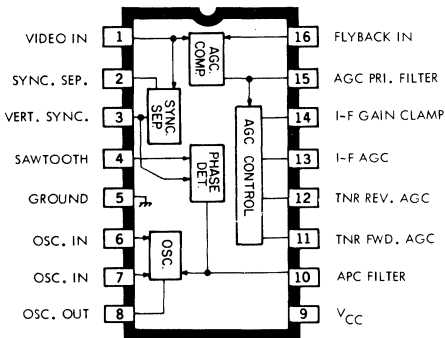

DWG.NO. A-11,485

Figure 2

AGC

When the scan is synchronized, current is supplied to the AGC detector (comparator) during the separated sync. The negative-going sync video waveform at pin 1 is compared with a 4.0 V level during this time. As a result of the AGC loop, the tip of the sync is clamped to 4.0 V.
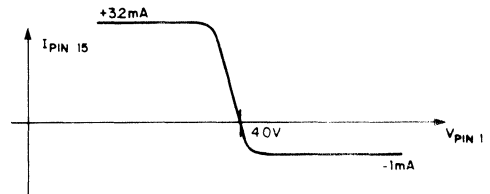

DWG.NO. A-11,486

Figure 3
AGC DETECTOR

The AGC detector is a high gain comparator with an asymmetrical active load (Figures 3 and 4). The active load provides approximately 3.2 mA of primary filter capacitor charge current and 1.0 mA of discharge current.

DWG.NO. A-11,487

Figure 4
AGC DETECTOR CHARACTERISTICS

The high AGC-loop gain provides the high slew rate necessary for fast channel-to-channel gain equalization and response to airplane flutter variations.

The AGC detector is gated ON by a pulse defined by coincidence of horizontal flyback and sync. Coincidence-gating provides improved AGC noise immunity over systems only are flyback-gated. Coincidence-gating maintains AGC levels in the event of temporary loss of horizontal sync or disturbance of horizontal timing.

Coincidence-gating demands the use of two additional internal circuits to compensate for two extremes of video input level at pin 1. The first is a sync recovery system (Figure 5).
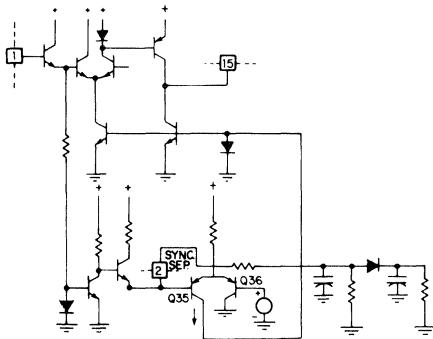

DWG.NO. A-11,488

Figure 5
SYNC RECOVERY SYSTEM

Extremes occur in the transition from a strong to a weak signal. The AGC loop requires time to respond to new signal level. In the meantime, system gain is too low, and the video amplitude at pin 1 is too low for the sync separator to provide sync pulses for coincidence-gating. The resulting condition would be lockout of the signal. However, a threshold detector composed of Q_{35} and Q_{36} senses sync-separator (pin 2) voltages less than 3.8 V. When this occurs, the AGC detector is gated by flyback only, allowing the AGC system to respond to the new signal level. As the video amplitude at pin 1 increases to its nominal value, the AGC detector returns to the coincidence-gating mode.

The second extreme of video input level occurs in the transition from a weak to a strong signal. In the transition, the I-F amplifier overloads, resulting in a low d-c level at pin 1, Figure 6. The sync separator at pin 2 charges to a higher d-c level, and no sync pulses are generated for coincidence-gating. Lockout of the signal is again possible, being dependent on both AGC-loop response and sync-separator time constants.
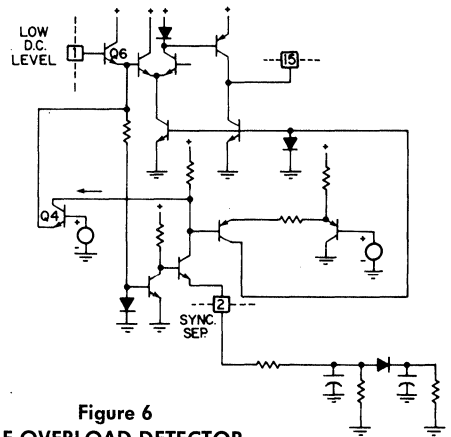

Figure 6
I-F OVERLOAD DETECTOR

DWG.NO. A-11,489

The threshold detector, Q_6 and Q_4, senses when the d-c level at pin 1 is below 3.4 V. When this occurs, the AGC detector is gated by flyback only, allowing the AGC system to respond to the new signal level. As the video level at pin 1 decreases to its nominal value, the AGC detector returns to the coincidence-gating mode.

The AGC primary filter at pin 15 integrates the AGC-detector output into a d-c voltage, which drives the AGC control circuit. A low d-c level at pin 15 corresponds to a low received-signal level. Conversely, a high d-c level at pin 15 corresponds to a high received-signal level.

Figure 7 is a simplification of the I-F portion of the AGC control circuit. As is common practice, the I-F amplifier is gain-reduced prior to the tuner under increasing signal levels.
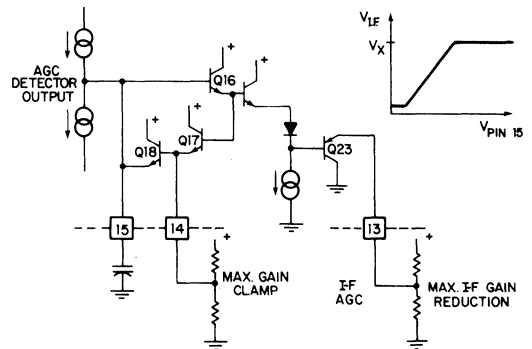

DWG.NO. A-11,490

Figure 7
I-F AGC CONTROL CIRCUIT

The maximum-gain voltage of the AGC primary filter is defined by the circuit designer as

$$V_{14} - 0.7 \text{ V}$$

since this level is internally clamped by Q_{18}. Under gain reduction, Q_{16} and Q_{17} force the voltage at pin 14 to follow 1.4 V below the primary filter voltage.

Produced by a series of emitter-followers, the I-F AGC output has a gain of 1, referenced to the AGC primary filter.

Choice of the external voltage-divider level, V_X, at pin 13 (I-F AGC output) defines the maximum I-F gain-reduction level, or AGC delay point, at which the tuner is called upon for further gain reduction. As there is a finite dead zone in the cross-over between I-F AGC and tuner AGC, a capacitor between pin 14 (a buffered primary AGC filter a-c voltage source) and pin 13 will decrease AGC recovery time in the transition between I-F and tuner AGC.

At the maximum I-F AGC level, V_X, the values of resistors R_{27} and R_{30} are such that the voltage at the base of Q_{27} is 1.4 V (Figure 8). This defines the point at which tuner AGC action is initiated. The collector current of Q_{27} is mirrored to provide forward-tuner AGC with a trans-conductance gain of 2.1 mA/V, referenced to the AGC primary filter. The emitter current of Q_{27} is mirrored to provide reverse-tuner AGC with a gain of 3.1 mA/V.
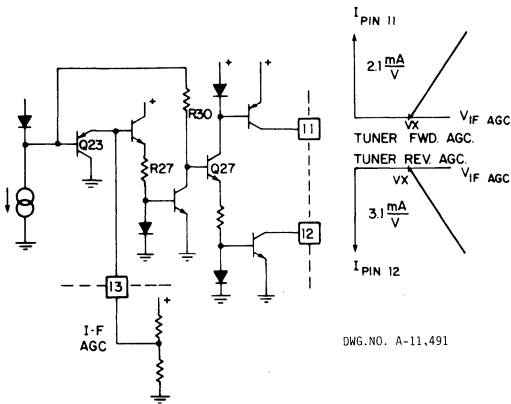

Figure 8
TUNER CONTROL CIRCUIT

Sync Separator

Since Q_4, (Figure 6), clamps the video waveform to 0.5 V below the level of the sync tip, noise accompanying the incoming video is prevented from severely altering the sampling level of the sync separator.

The negative-going sync video waveform at pin 1 is inverted and amplified by 6 dB. This waveform is

buffered and applied to the base of Q_{33}, which has as its emitter load a dual time-constant sync-separator network (Figure 9). Since this network is external to the device, the circuit designer has freedom to choose the sampling level and sync-separator time constants.
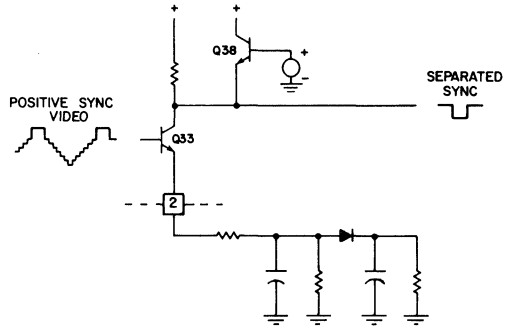

Figure 9
SINGLE PIN SYNC SEPARATOR

The separated sync-voltage waveform at the collector of Q_{33} is clamped to 7.3 V by Q_{38}, and is amplified by approximately 20 dB (Figure 10). Complementary emitter-followers buffering the sync waveform have an amplitude of 10 V_{PP}. The sync output is provided at pin 3, protected by short-circuit current-limiting of approximately 25 mA. It is internally coupled to the scan-phase detector. In addition to protecting the device against accidental shorts, grounding pin 3 also provides a convenient method of adjusting the oscillator's free-run frequency.
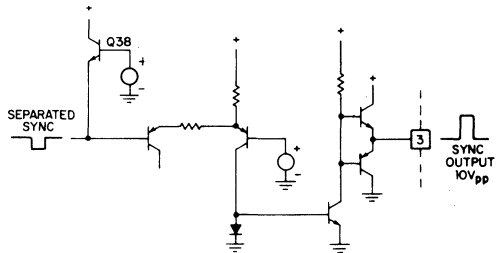

Figure 10
SYNC OUTPUT CIRCUIT

Scan Processing

The scan-phase detector consists of a differential amplifier that is gated ON by separated sync. An integrated flyback waveform is applied to the input of the differential amplifier (Figure 11). The differential amplifier has an active load, providing single-ended output of the phase-detector currents.
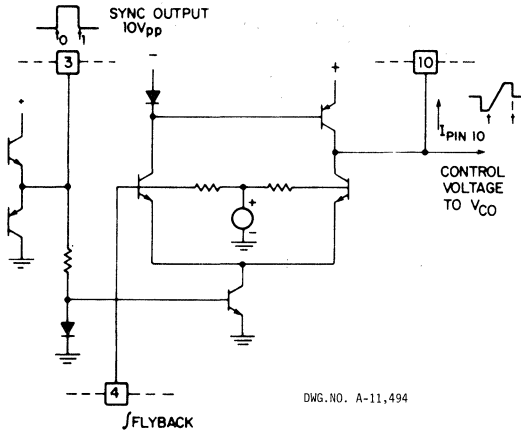
SYNC OUTPUT
10Vpp

DWG.NO. A-11,494

∫FLYBACK

Figure 11
PHASE DETECTOR CIRCUIT

The positive and negative-output currents (500 μA) of the phase detector are internally balanced to within approximately 5% of the absolute value of these currents. This limits the static phase-error attributable to phase-detector imbalance. Since the phase-detector output filter is external to the device, pull-in characteristics can be defined by the choice of external filter components at pin 10.

A simplification of the master-scan VCO of Type ULN-2260A is shown in Figure 12. The VCO is designed to minimize the effects of device parameter variations on free-run frequency and VCO characteristics. Components defining phase-shift and filter
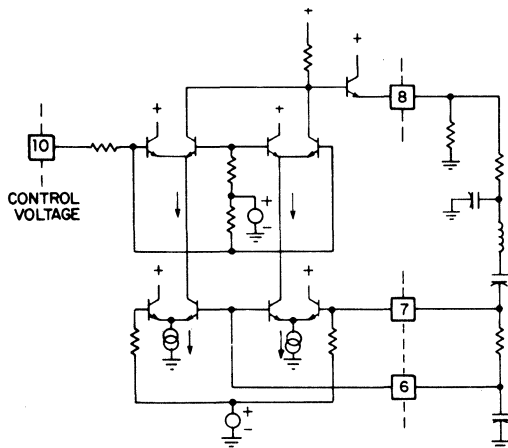
CONTROL
VOLTAGE

DWG.NO. A-11,495

Figure 12
MASTER SCAN VCO

functions are external to the device. This provides the circuit designer with freedom to define the characteristics of the oscillator: Free-run frequency, control sensitivity and temperature compensation. Control of free-run frequency allows operation of the circuit in both countdown-synchronized and conventionally synchronized receivers.

The oscillator is controlled by weighted summing of quadrature components of feedback-signal current. The quadrature is inherently defined by the external resistor and capacitor of the tank circuit at the input of each of the two differential amplifiers. These external components are series connected. Therefore, the capacitor voltage waveform lags that of the resistor by 90°. VCO characteristics for a 503.5-KHz L-C oscillator, vertical countdown receiver, are shown in Figure 13.
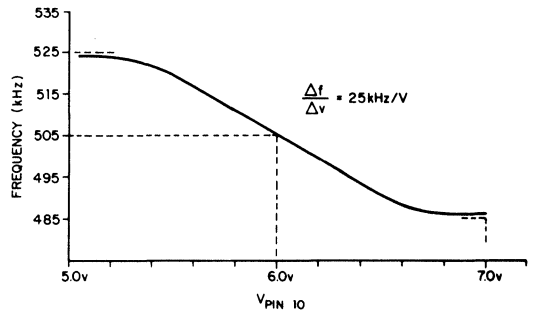
FREQUENCY (kHz)

$\frac{\Delta f}{\Delta v}$ = 25kHz/V

$V_{PIN\ 10}$

DWG.NO. A-11,496

Figure 13
VCO CHARACTERISTICS

Because it is a low-impedance source-point, pin 8 is internally short-circuit current-limited to approximately 70 mA.

Conclusions

The device presented above was designed to provide, with as much flexibility as possible, efficient partitioning of AGC, sync, and scan-control functions. Coincidence AGC-gating was utilized to improve AGC noise immunity. The circuit provides a high-level separated-sync output for sync integrators. The scan-phase detector is accurately balanced internally. The scan VCO was chosen to minimize the effects of device-parameter variations on oscillator characteristics, and is adaptable to both countdown-synchronized and conventionally synchronized receivers.

SECTION 8—AUDIO POWER AMPLIFIERS

*New product. Contact factory for detailed information.

8

SELECTION GUIDE TO AUDIO POWER AMPLIFIERS

Device Type	Monophonic	Stereo	P_{OUT}	V_{CC}
ULN-2280B	X	—	2.5 W	8.0-26 V
ULN-2283B	X	—	1.2 W	3.0-18 V
ULN-3701Z	X	—	10 W	8.0-18 V
ULN-3702Z	X	—	12 W	8.0-26 V
ULN-3703Z	X	—	10 W	8.0-18 V
ULN-3705M	X	—	600 mW	1.8-9.0 V
ULN-3783M*	—	X	520 mW	2.4-9.0 V
ULN-3784B	X	—	4.0 W	9.0-28 V
ULN-3793W*	X	—	20 W	8.0-18 V

*New product. Consult factory for information.

ULN-2280B AUDIO POWER AMPLIFIER

FEATURES

- Low Distortion
- Low Quiescent Current
- A-C Short-Circuit Protection
- 34 dB Internally Fixed Gain
- High Input Impedance
- Thermal Overload Protection
- Replaces LM380N
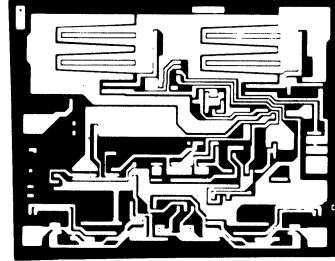
FEW SUPPLEMENTAL discrete components are needed to use Sprague Type ULN-2280B audio power amplifier in automotive, communication and consumer designs.

With an 18 V supply, the amplifier delivers 2.5 W of low-distortion audio into an 8Ω load. Output power with a 24 V supply is 2.5 W into a 16Ω load.

The audio amplifier is supplied in an improved 14-pin dual in-line plastic package with heat sink contact tabs. The webbed lead configuration, originated by Sprague Electric, permits attachment of an inexpensive heat sink for increased power dissipation capability and use of a standard integrated circuit socket or printed wiring board layout.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 26 V
Peak Output Current, I_{OUT} .... 1.2 A
Package Power Dissipation, P_D .... See Graph
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −65°C to +150°C

Dwg. No. A-9777A

SCHEMATIC
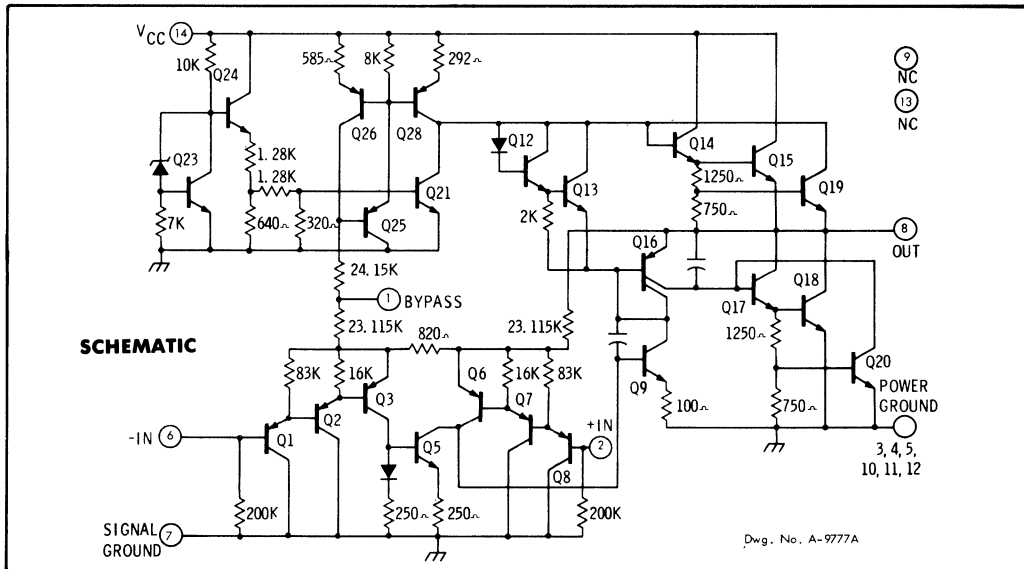
ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 18$ V, $R_L = 8\Omega$, $f_{in} = 1$ kHz (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Supply Voltage Range	V_{CC}		8.0	18	26	V
Quiescent Supply Current	I_{CC}	$V_{in} = 0$ V	—	15	—	mA
Quiescent Output Voltage	V_{OQ}	$V_{in} = 0$ V, See Note 1	—	9.0	—	V
Output Voltage Swing	V_{out}	$P_{out} = 2$ W	—	12	—	Vpp
Voltage Gain	A_v	$P_{out} = 0$ W	31	34	37	dB
Total Harmonic Distortion	THD	$P_{out} = 50$ mW, $R_L = 8\Omega$, $V_{CC} = 18$ V	—	<0.2	1.0	%
		$P_{out} = 50$ mW, $R_L = 16\Omega$, $V_{CC} = 24$ V	—	—	0.5	%
		$P_{out} = 2$ W, $R_L = 8\Omega$, $V_{CC} = 18$ V	—	<1.0	2.0	%
Audio Power Output	P_{out}	$R_L = 8\,\Omega$, $V_{CC} = 18$ V, THD = 2%	2.0	2.5	—	W
		$R_L = 16\,\Omega$, $V_{CC} = 24$ V, THD = 2%	2.0	2.5	—	W
Input Impedance	Z_{in}	Each Input	140	170	—	$k\Omega$
Power Supply Rejection	PSRR	$P_{out} = 0$ W, f = 120 Hz	—	35	—	dB
Equiv. Input Noise		f = 20 Hz to 20 kHz	—	60	—	μV_{rms}
Bandwidth (−3 dB)	BW	$P_{out} = 1$ W, See Note 2	—	100	—	kHz

NOTES: 1. The quiescent output voltage typically equals ½ the supply voltage.
2. Unity gain typically occurs between 10 MHz and 100 MHz.

TEST CIRCUIT

Dwg. No. A-11,396A

TYPICAL CHARACTERISTICS

DISTORTION AS A FUNCTION OF OUTPUT POWER

Dwg. No. A-11,397

DISTORTION AS A FUNCTION OF FREQUENCY

Dwg. No. A-11,398

PSRR AS A FUNCTION OF FREQUENCY

Dwg. No. A-11,399

VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

Dwg. No. A-11,400

8
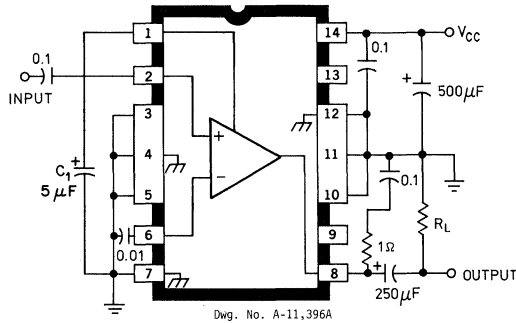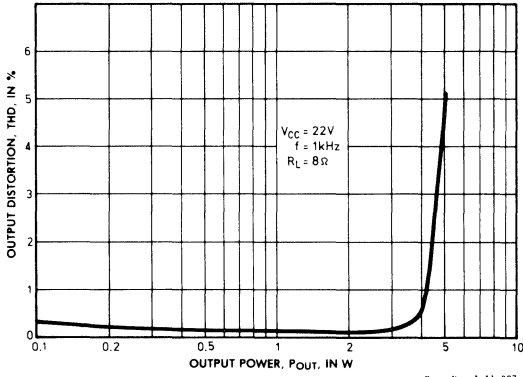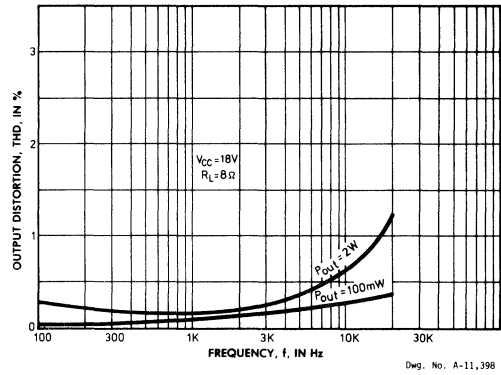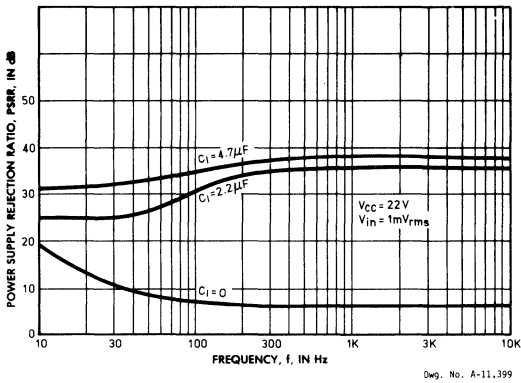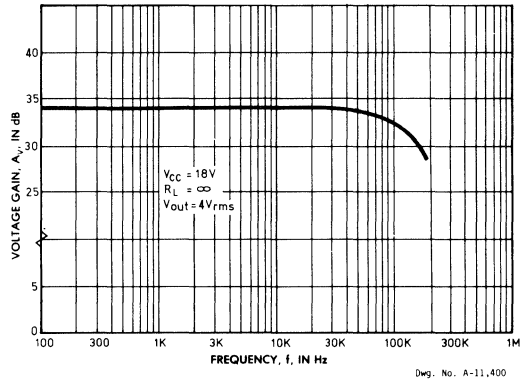
THERMAL FACTORS
AND ULN-2280B OPERATION

Thermal factors must be considered in achieving reliable operation of Type ULN-2280B. Guidelines given here provide the circuit design engineer with information on maintaining IC junction temperature below safe limits when the audio power amplifier is operated at maximum ambient temperature and power dissipation.

The graphs below show package power dissipation as a function of output power over a wide range of supply voltage with a load resistance of 8Ω or 16Ω. Lines indicating 3% distortion and 10% distortion are shown as guides to trade-offs between supply voltages, package power dissipation and upper-limit distortion.

As the power supply voltage increases for any output power requirement, distortion decreases and package power dissipation increases. Package power dissipation figures must be taken from the highest point on the supply voltage curve.

DISSIPATION AS A FUNCTION OF OUTPUT POWER (8Ω LOAD)
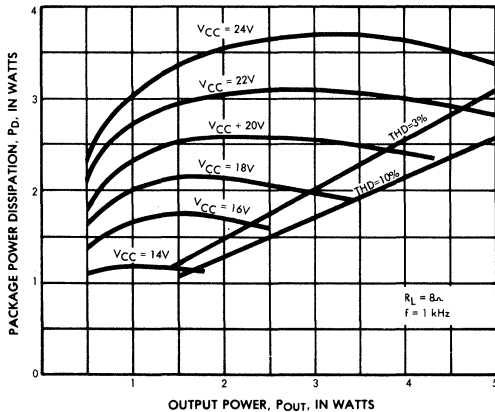
Dwg. No. A-9839A

DISSIPATION AS A FUNCTION OF OUTPUT POWER (16Ω LOAD)
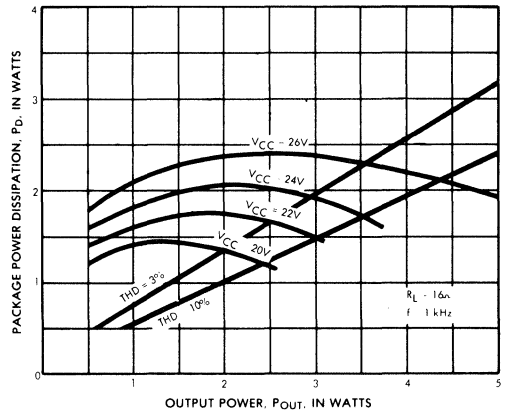
8—6

CIRCUIT DESIGN

If design values of audio output power, distortion and maximum ambient temperature have been selected, optimal speaker impedance and supply voltage, as well as heat-sink requirements, can be determined from curves below and on page 4.

For an output of 2.5 W with 3% distortion and a maximum ambient temperature of +50°C:

R_l	8Ω	16Ω
THD	3%	3%
P_{OUT}	2.5 W	2.5 W
V_{CC}	16.7 V	22 V
P_D (max)	1.9 W	1.75 W
$P_D + P_{OUT}$	4.4 W	4.25 W
I_{CC}	263 mA	193 mA

The preceding appears to indicate the best choice is an output impedance of 16Ω with a 22 V supply. However, if an unregulated supply is used, the designer may prefer an 8Ω load with a 16 V supply, since the absolute maximum V_{CC} rating of Type ULN-2280B is 26 V and since maximum package dissipation must be calculated using the no-load voltage level.

The graph below (left) shows that the Staver V-8 heat sink would be just adequate for design conditions outlined above at an ambient temperature of 50°C. The Staver V-7 heat sink would provide a wider margin of safety.

ALLOWABLE POWER DISSIPATION
AS A FUNCTION OF AMBIENT TEMPERATURE
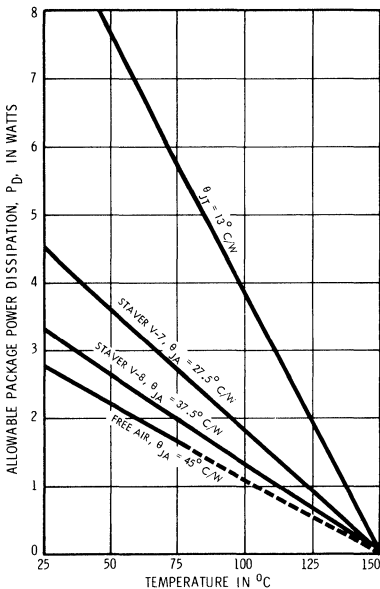
Dwg. No. A-11,793A

SUPPLY CURRENT AS A FUNCTION
OF SUPPLY VOLTAGE
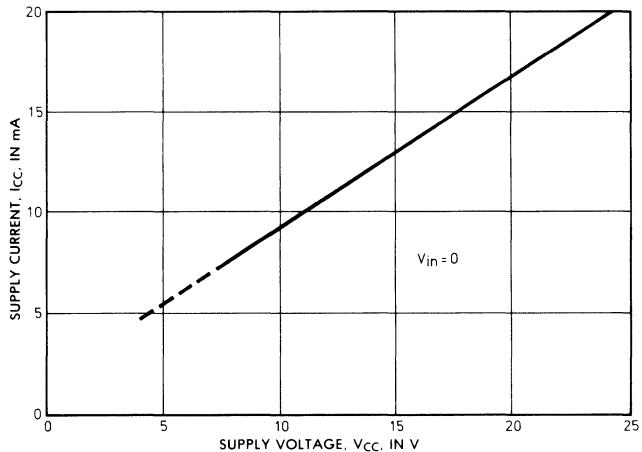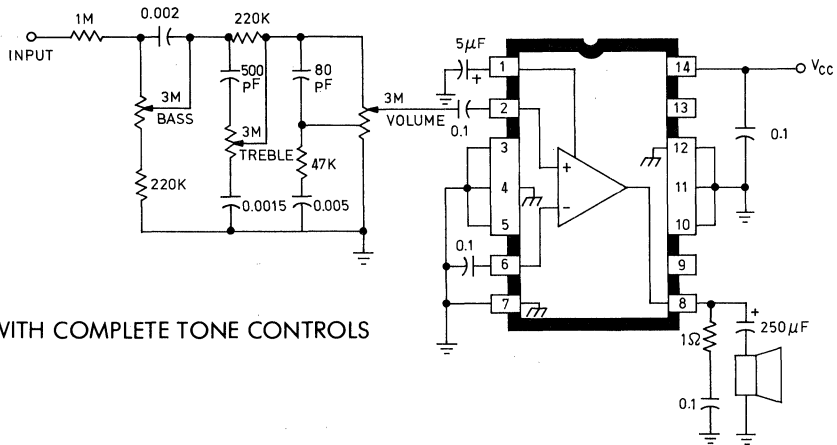
TYPICAL APPLICATIONS

AMPLIFIER WITH COMPLETE TONE CONTROLS
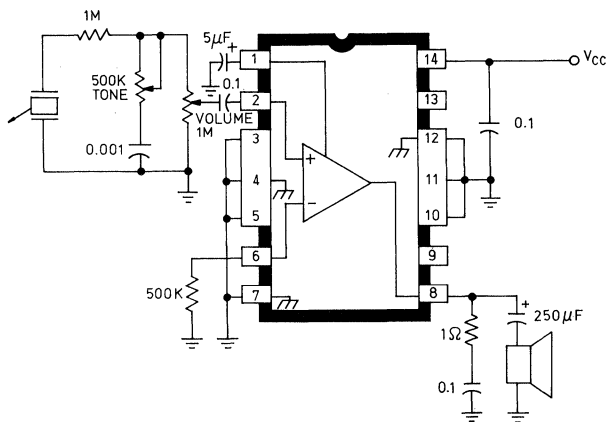
Dwg. No. A-11,403B

LOW-COST PHONOGRAPH
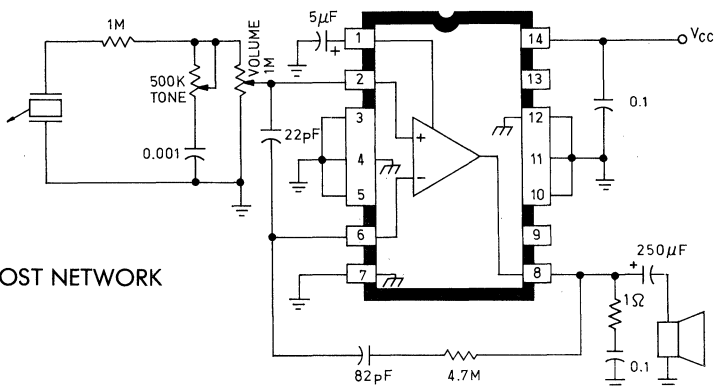
Dwg. No. A-11,404B

AMPLIFIER WITH BASS BOOST NETWORK

Dwg. No. A-11,405B

ULN-2283B LOW POWER AUDIO AMPLIFIER

FEATURES

- Wide Operating Voltage Range (3 to 18 V)
- Low Quiescent Current Drain
- A-C Short Circuit Protected
- Low External Parts Count
- Low Distortion
- 42 dB Voltage Gain

DESIGNED primarily for use in low-cost phonographs and radio receivers, the ULN-2283B audio power amplifier is well-suited for use in battery-operated portable equipment. It will function with supply voltages as low as 2 volts (at reduced volume) without any significant increase in distortion. Weak batteries need no longer be a major concern for users in sets with this device. The class AB audio amplifier also features low quiescent current drain for maximum battery life.

The ULN-2283B is rated for operation over the supply voltage range of 3.0 to 15 volts. Selected devices, for operation with supply voltages of up to 18 volts, are available as ULN-2283B-1. Except for the maximum allowable supply voltage specification, the ULN-2283B and the ULN-2283B-1 are identical.

The ULN-2283B audio power amplifier is supplied in an improved 8-lead dual in-line plastic-package with two webbed tabs. A copper alloy lead frame results in maximum power dissipation without need for an external heat sink. Lead configuration is compatible with standard IC sockets or printed wiring board hole layouts.

DECOUPLE	1	8 INPUT
GROUND	2	7 GROUND
GROUND	3	6 GROUND
OUTPUT	4	5 V_{CC}

DWG. NO. A-10,473
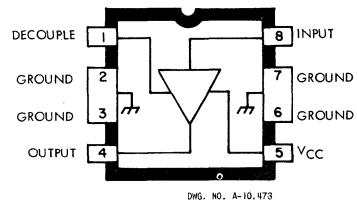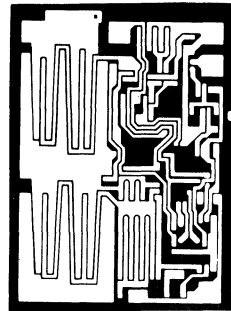
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} (ULN-2283B) .... 15 V
(ULN-2283B-1) .... 18 V
Package Power Dissipation, P_D .... See Graph
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −65°C to +150°C

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $f_{in} = 400$ Hz

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
			Limits	
Supply Voltage Range	V_{CC}	ULN-2283B	3.0	—	15	V
		ULN-2283B-1	3.0	—	18	V
Quiescent Supply Current	I_{CC}	$V_{CC} = 6.0$ V	—	12	16	mA
		$V_{CC} = 12$ V	—	24	28	mA
Voltage Gain	A_e	$P_{OUT} = 0$ W	39	42	46	dB
Audio Power Output	P_{OUT}	$V_{CC} = 6.0$ V, $R_L = 8\,\Omega$, THD = 10%	0.25	0.35	—	W
		$V_{CC} = 9.0$ V, $R_L = 8\,\Omega$, THD = 10%	0.80	1.1	—	W
		$V_{CC} = 12$ V, $R_L = 16\,\Omega$, THD = 10%	0.80	1.2	—	W
Input Resistance	R_{IN}	Pin 8	—	250	—	$k\Omega$
Power Supply Rejection	PSRR	$C_D = 500\,\mu F$, $f_{ripple} = 120$ Hz	28	34	—	dB

TEST CIRCUIT

DWG. NO. A-10.470A

TYPICAL FREQUENCY RESPONSE

V_{CC} = 3 to 12V
R_L = 8Ω
C_D = 100 to 250µF

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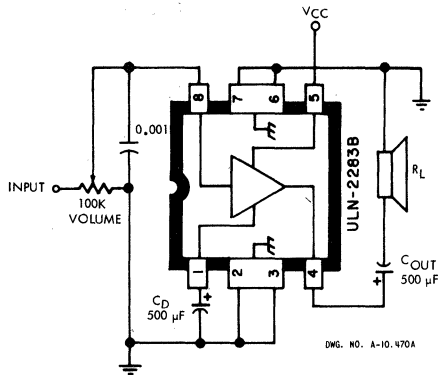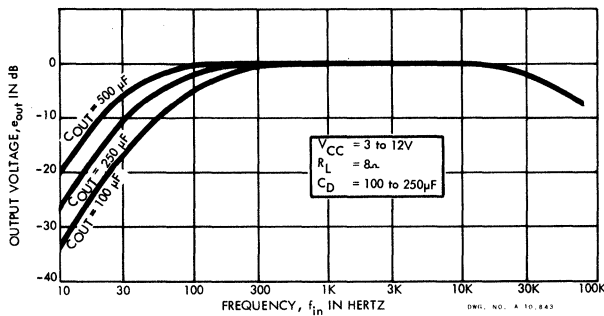
ALLOWABLE PACKAGE POWER DISSIPATION
Printed Wiring Board Copper
is 2 oz./ft², 2.5 sq. in.
(610 g/m², 16.1 cm²)
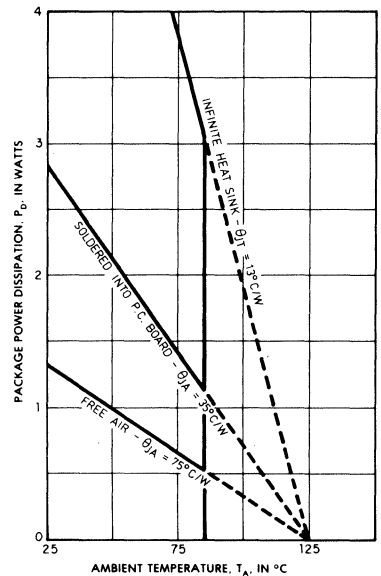
Dwg. No. A-11,422

TYPICAL CHARACTERISTICS

QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE
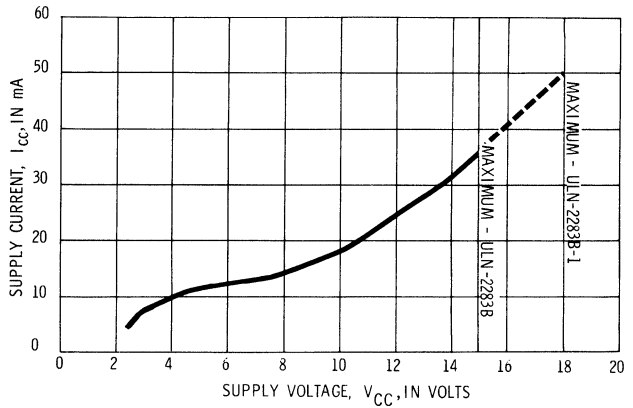
DWG.NO. A-11,238

OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE

DWG.NO. A-10,839A

8
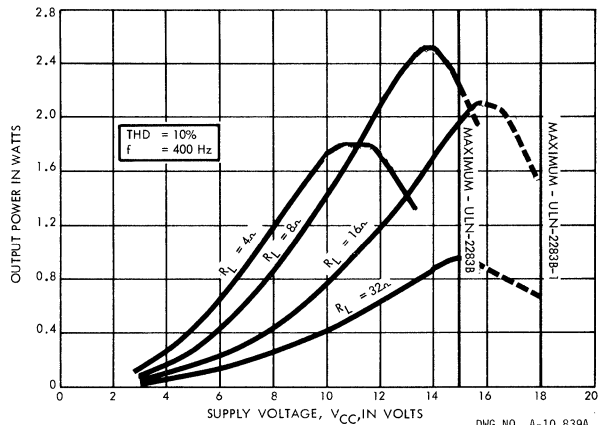
POWER SUPPLY REJECTION AS A FUNCTION OF FREQUENCY
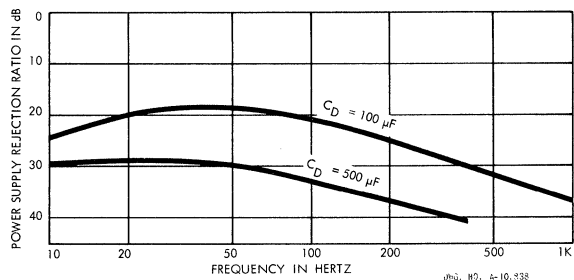
8—11

PACKAGE POWER DISSIPATION
AS A FUNCTION OF OUTPUT POWER

AT 4Ω LOAD

AT 8Ω LOAD

AT 16Ω LOAD

TOTAL HARMONIC DISTORTION
AS A FUNCTION OF OUTPUT POWER

OUTPUT DISTORTION, THD, IN %

$V_{CC} = 3 V$ $V_{CC} = 6 V$ $V_{CC} = 9 V$ $V_{CC} = 12 V$

$R_L = 8 \Omega$
$f = 400 Hz$

10 m   30 m   100 m   300 m   1.0   3.0   10

OUTPUT POWER IN WATTS

DWG. NO. A-10.840

AT 8Ω LOAD

OUTPUT DISTORTION, THD, IN %

$V_{CC} = 3 V$ $V_{CC} = 6 V$ $V_{CC} = 9 V$ $V_{CC} = 12 V$

$R_L = 16 \Omega$
$f = 400 Hz$

10 m   30 m   100 m   300 m   1.0   3.0   10

OUTPUT POWER IN WATTS

DWG. NO. A-10.841
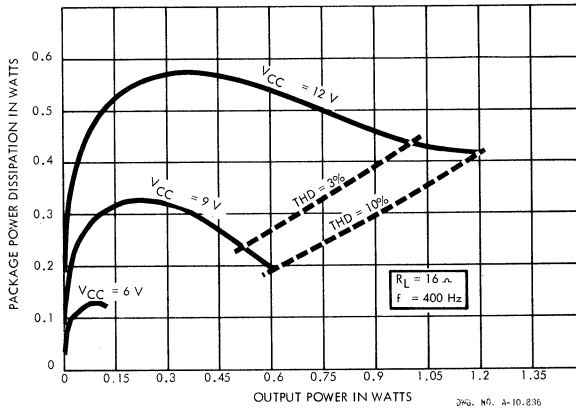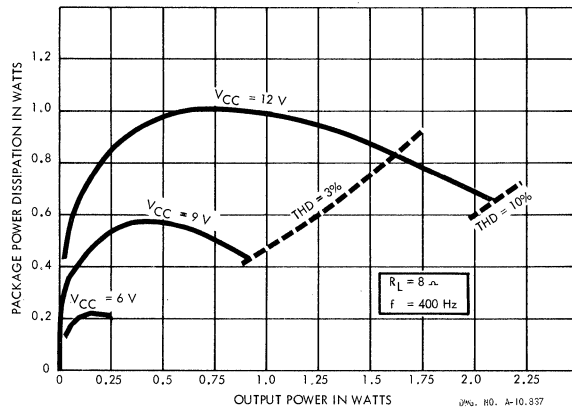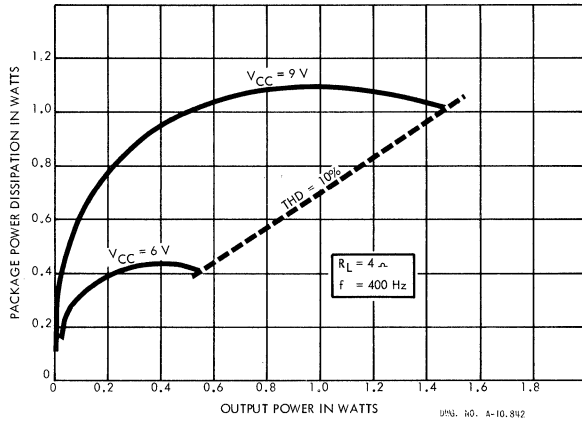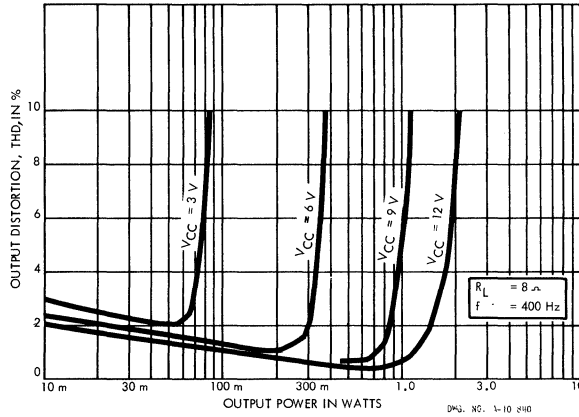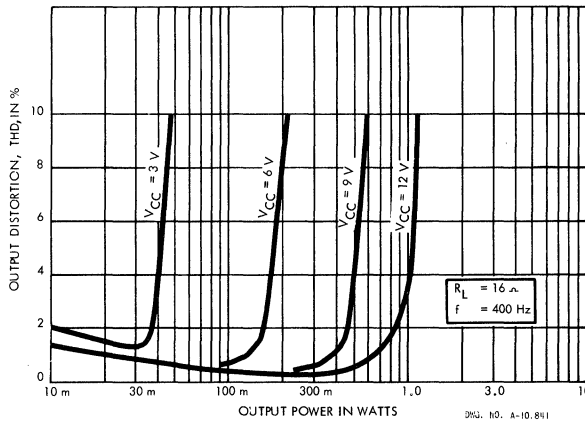
AT 16Ω LOAD

8

CIRCUIT DESCRIPTION

To achieve the desired performance objectives of high power output and efficiency from a 2 to 18 V supply requires that the amplifier be capable of peak-to-peak voltage swings approaching the available supply. To meet these performance objectives, a power amplifier design is required having no more than one V_{BE} of swing restriction.

As shown in Figure 1, the output stage is comprised of 2 NPN transistors (Q17 and Q18) plus a phase inverter (Q15). Quiescent operating current is set up by the current source (I).

Assuming $V_{oq} = V_{CC}/2$ then the collector current of Q15 = I, ignoring base currents, and if Q15 is matched to Q18 as is possible in a monolithic circuit, then the collector current of Q18 equals the collector current of Q15.

The circuit in Figure 1 achieves an excellent voltage swing capability of $V_{CC} - V_{BE} - 2V_{CE(SAT)}$. This totally NPN configuration also has good freedom from the high-frequency problems that often occur with quasi-complementary composite NPN-PNP configurations.

Figure 2

To reduce the size of Q15, an additional transistor (Q16) is added to the circuit as shown in Figure 2. Transistor Q16 divides I by its beta + 1 allowing Q15 to be reduced in area by a similar value. In the practical realization of the ULN-2283B, Q15 is chosen as $1/5$ the emitter area of Q18 with a typical beta for Q16 of 6.
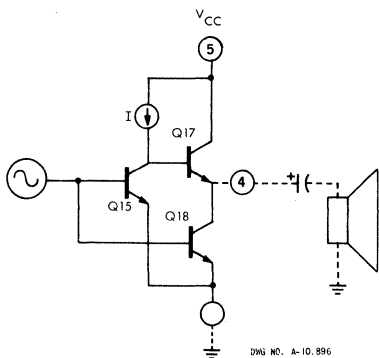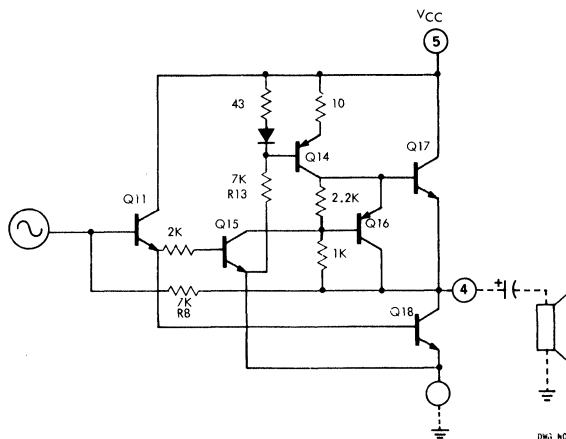
Figure 1

Figure 3

Although the circuit in Figure 1 has been incorporated in production monolithic circuits in essentially the form shown, in practice it has unacceptable design restrictions. Since I is also the base drive current for Q17, the ratio of available base drive current I to idling current is proportional to the ratio of the emitter areas of Q18 to Q15. For practical values of I_{Q15}/I_{Q18}, i.e. one, the circuit has a serious implementation problem; it requires three output transistors (Q15, Q17, and Q18).

Figure 3 illustrates other refinements in the practical realization of the output circuit. The drive and idling current I is derived from a V_{CC} dependent source allowing maximum drive under maximum supply conditions while affording reduced drive and associated current conservation under minimum supply conditions. In addition, the Q16 divider circuit is refined to reduce PNP beta dependence. Finally with the addition of an input emitter follower (Q11) and a local negative feedback loop (R8), the output is completed as it appears in the ULN-2283B.
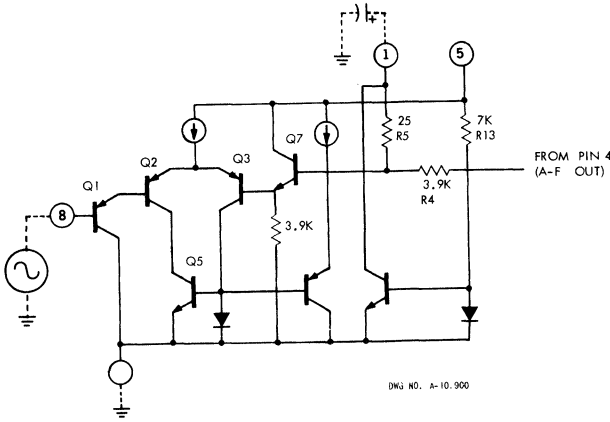
Figure 4

The input stage of the power amplifier (Figure 4) is comprised of a PNP differential pair (Q2 and Q3) preceded by a PNP emitter follower (Q1) which allows d-c referencing of the source signal to ground. This eliminates the need for an input coupling capacitor. Overall negative feedback, set by the ratio of R4 to R5, is applied to the inverting input Q3 through an NPN emitter follower (Q7) which also provides d-c level shifting.

The $V_{CC}/2$ output tracking is achieved by summing the current flow through R4 and R5, with the current through R13 "reflected off of ground." Thus $V_{CC}/2$ tracking is maintained by the voltage drop across 2 resistors. This allows the current from R13 to be bypassed at Pin 1, thereby combining the ripple bypass capacitor with the audio feedback capacitor.

Figure 5 illustrates the complete power amplifier as realized in the ULN-2283B, including the external components. The remarkably-low external component count, (only two capacitors including the output coupling) reflects concern for simplicity in implementation, yet the device achieves excellent performance. Typical output power can be as high as 2.1 W from a 12 volt supply and useful output power at supply voltages of as low as 2 volts.

APPLICATIONS

Selection of power supply voltage and speaker impedance allow the designer to choose audio power levels. No unique precautions are necessary when designing with the ULN-2283B power amplifier. The device is stable and a-c short-circuit immune.
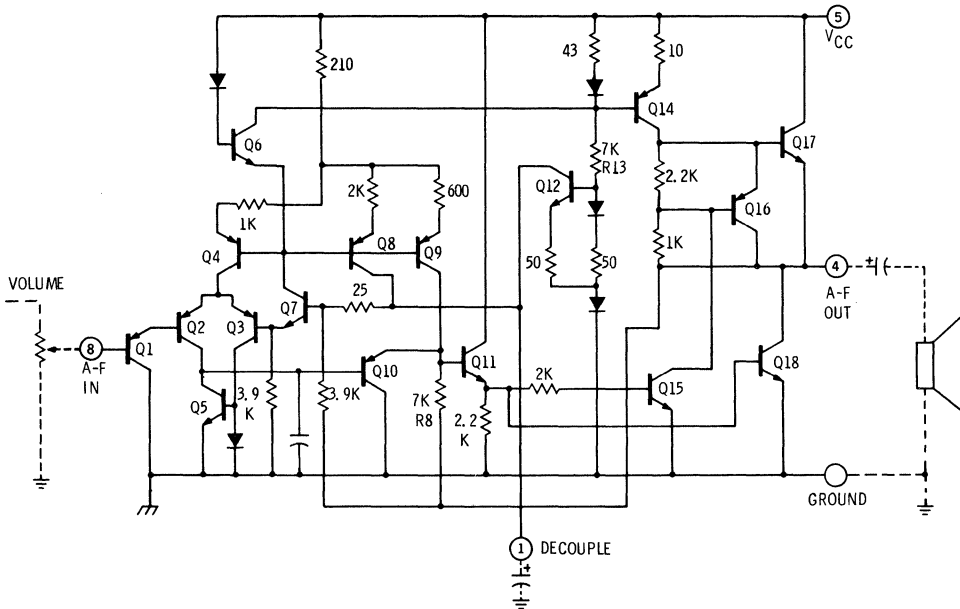
Figure 5

External component choice for the power amplifier involves only two capacitors; one for the speaker coupling and one for the feedback and ripple by-passing. The coupling capacitor value should be selected to provide the desired low-frequency cutoff with the chosen speaker impedance. The feedback and ripple bypass capacitor at Pin 1 should be chosen for both low-frequency audio rolloff and supply ripple rejection.

Ripple rejection is not practical to calculate due to the large number of mechanisms involved. A 500 μF capacitor at Pin 1 achieves typically 34 dB rejection.

The high gain of typically 42 dB and the high input impedance (250 kΩ) of the power amplifier allow utilization of this device for applications such as ceramic cartridge phono amplifiers.

Typical ceramic phono cartridges develop approximately 400 mV. However, the recommended load impedance for the most economical cartridges is usually 1 MΩ. This poses no problem with the 250 kΩ input impedance of the ULN-2283B since the cartridge manufacturer specifies the load impedance for full low-frequency response to less than 40 Hz. Decreasing the load impedance produces an increased low end cutoff frequency.

In a ULN-2283B based application employing a cost and space conscious loudspeaker, 40 Hz program material capability is not only unnecessary but undesirable, and therefore a mismatch of the cartridge to increase the lower cutoff frequency to a value more in keeping with the other components of the system is recommended.

The ULN-2283B audio amplifier stage has other input considerations to be taken into account for best results. The input is referenced to ground for internal biasing and must be provided with a d-c path to ground. A current of typically 0.1 μA flows from Pin 8 through the volume control producing an IR drop which is multiplied by the closed loop d-c gain of the amplifier (1), and appears as an error in output centering at Pin 4. This recommends a value of 200 kΩ or less for the volume control, with values of less than 100 kΩ preferred.

The selection of amplifier load impedance involves more consideration than just the desired power output. Ideally a low speaker impedance would produce the highest power outputs for any one supply voltage as the curves illustrated. However, operation with a 16Ω load can produce as much power as with an 8Ω load. The higher impedance load will also furnish a significant reduction in harmonic distortion and improvement in overall repeatability in power output capacity. In applications which allow the selection of the power supply voltage it is therefore recommended that a 16Ω load impedance be utilized in applications up to 1.2 watt.

PRINTED WIRING BOARD LAYOUT & SPECIAL CONSIDERATIONS

Special on-chip considerations for minimizing tendencies towards instabilities of all types were taken in the design of the ULN-2283B. However, like all high-gain circuits, care and forethought should still be given to a printed wiring board layout to avoid undesirable effects. Input and output should be well separated and should avoid common mode impedances wherever possible. The ground return for the audio bypass at Pin 1 should be kept reasonably close to the volume control ground as Pins 1 and 8 represent the inverting and non-inverting inputs to the amplifier and enjoy about 40 dB of common mode rejection.

Device dissipation vs. output power and supply voltage for 4, 8, and 16 ohm loads is shown in the curves on page 4. With no heat sinking (free air), the ULN-2283B audio power amplifier will withstand the worst case conditions (4 Ω at 9 V) for ambient temperatures to +42.5°C. For conditions not shown, for higher ambient temperatures, or for improved device reliability, a minimum heat sink is recommended. As illustrated in the allowable package power dissipation curves, with the heat sink tabs (Pins 2, 3, 6, and 7) soldered into a 2.5 square inch (16.13 cm^2) copper area of a printed circuit board, adequate heat sinking is easily obtained.

ULN-3701Z / TDA2002
5 TO 10-WATT AUDIO POWER AMPLIFIER

FEATURES

- Low External Parts Count
- Low Distortion
- Class B Operation
- Short-Circuit Protected
- Thermal Overload Protected
- Low Noise
- High Output-Voltage Swing
- TO-220 Style Package
- Direct Replacement for LM383 and CA2002
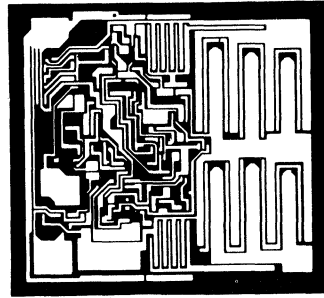
DESIGNED specifically to drive low-impedance loads down to 1.6 Ω, the Type ULN-3701Z / TDA2002 audio power amplifier is ideal for automotive radio, tape player, and CB applications.

It can deliver 5 W to 10 W of audio in the single-ended mode. Operating in the extremely harsh au-

NON-INVERTING INPUT 1
INVERTING INPUT 2
GROUND 3
OUTPUT 4
V_{CC} 5

Dwg. No. A-10,464

tomotive environment, this device is capable of withstanding high ambient temperatures, output overloads, and repeated power supply transient voltages without damage.

The Type ULN-3701Z/TDA2002 amplifier is rated for continuous operation with supply voltages of up to 18 V. With the application of increased voltages (to 28 V, maximum), a high-voltage protective circuit becomes operative, disabling the device. Devices without this internal high-voltage shutdown are available as Type ULN-3702Z/TDA2008 and are recommended for use where more than 10 W of audio power is required with higher impedance loads and supply voltages to 28 V. In all other respects, Types ULN-3701Z and ULN-3702Z are identical.

Type ULN-3701Z/TDA2002 is supplied in a modified 5-lead JEDEC Style TO-220 plastic package. The heat-sink tab is at ground potential; no insulation is required.

Lead configurations for vertical mounting (ULN-3701V) and for horizontal mounting (ULN-3701H) are available. Parts are branded with a partial Sprague Electric part number (ULN3701) and the basic Pro-Electron marking (TDA2002)
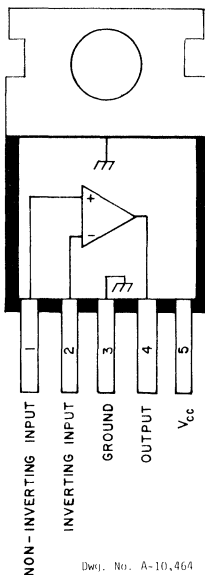
8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 28 V*
Peak Supply Voltage (50 ms) . . . . 40 V*
Peak Output Current, I_{OUT} . . . . 3.5 A
Non-Repetitive Peak Output Current . . . . 4.5 A
Package Power Dissipation, P_D . . . . See Graph
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −40°C to +150°C

*Internal high-voltage shutdown above 18 V.

ALLOWABLE POWER DISSIPATION
AS A FUNCTION OF AMBIENT TEMPERATURE
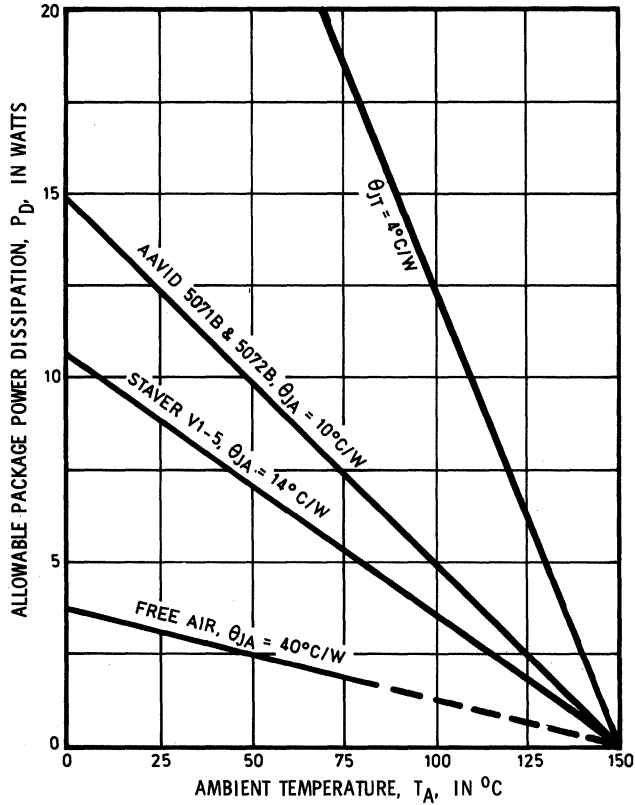
DWG. NO. A-12,000A

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{cc} = 14.4V$, $R_L = 4\Omega$, $f = 1$ kHz, $R_{fb} = \infty$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Supply Voltage Range	V_{CC}		8.0	14.4	18	V
Quiescent Supply Current	I_{CC}	No signal applied	—	45	80	mA
Quiescent Output Voltage	V_4	No signal applied	6.4	7.2	8.0	V
Open Loop Gain	A_v		—	80	—	dB
Closed Loop Gain	A_v		39.5	40	40.5	dB
Total Harmonic Distortion	THD	$P_{OUT} = 0.05$ to 3.5W	—	0.2	—	%
		$P_{OUT} = 0.05$ to 5.0W, $R_L = 2\Omega$	—	0.2	—	%
Audio Power Output	P_{OUT}	THD = 10%	4.8	5.2	—	W
		THD = 10%, $R_L = 2\Omega$	7.0	8.0	—	W
		THD = 10%, $V_{CC} = 16V$	—	6.5	—	W
		THD = 10%, $R_L = 2\Omega$, $V_{CC} = 16V$	—	10	—	W
Efficiency	η	$P_{OUT} = 5.2W$	—	68	—	%
		$P_{OUT} = 8.0W$, $R_L = 2\Omega$	—	58	—	%
Input Impedance	Z_1		70	150	—	kΩ
Power Supply Rejection	PSR	$f_{ripple} = 120$Hz, $V_{ripple} = 0.5V$	30	35	—	dB
Equiv. Input Noise Voltage	v_N	$f = 40$Hz to 15kHz	—	4.0	—	μV
Equiv. Input Noise Current	i_N	$f = 40$Hz to 15kHz	—	60	—	pA
Input Sensitivity	v_{in}	$P_{OUT} = 0.5W$	—	15	—	mV
		$P_{OUT} = 0.5W$, $R_L = 2\Omega$	—	11	—	mV
		$P_{OUT} = 5.2W$	—	55	—	mV
		$P_{OUT} = 8.0W$, $R_L = 2\Omega$	—	50	—	mV
Input Saturation Voltage	v_{in}		—	600	—	mV
Frequency Response (-3dB)		$C_{fb} = 0.039\mu F$, $R_{fb} = 39\Omega$	40	—	15k	Hz
Thermal Resistance	$R_{\Theta JT}$		—	—	4.0	°C/W

TEST CIRCUIT
All Capacitor
Values in μF
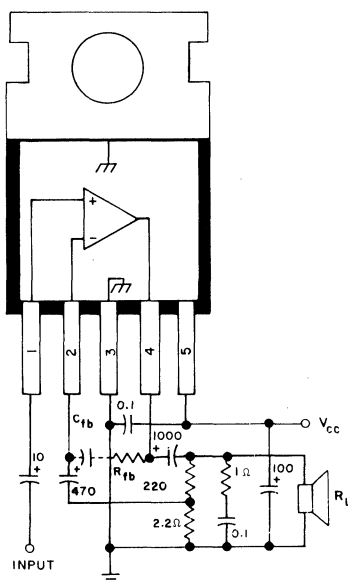
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APPLICATIONS INFORMATION
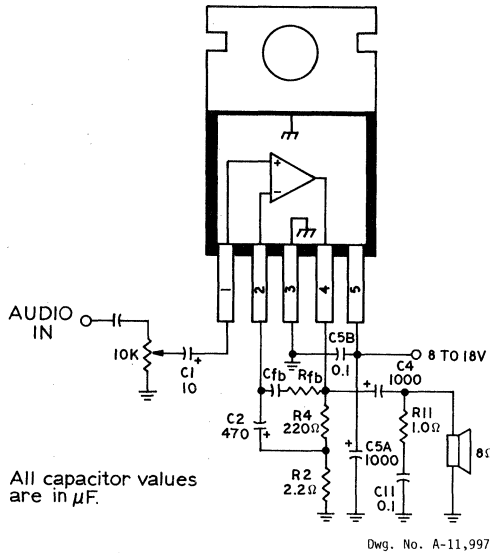
FIGURE 1

A typical application using Type ULN-3701Z / TDA2002 is shown in Figure 1. Component values other than those shown will affect circuit performance as follows:

C_1—The value of the input capacitor may be reduced with the lower limit determined by the device's input impedance and the required low-frequency performance. For a 20 Hz low-frequency cutoff, and a minimum input impedance of 70 kΩ, the minimum recommended value is 0.1 μF. This capacitor's value is normally very large so that transients (turn-on, turn-off) are inaudible. Common 1 μF to 2 μF electrolytic capacitors will work quite well.

C_2—The negative feedback capacitor affects the power supply rejection ratio; the capacitive value is therefore usually very large. If the power supply has low ripple, the feedback capacitor value can be reduced. Increasing the value of this capacitor above the recommended 470 μF will *not* have a large effect on PSRR, due to the terminating impedance of the output resistive divider.

C_4—The output capacitor is chosen to provide the desired low-frequency cutoff with the lower limit determined by the load impedance. The values shown provide for a 20 Hz cutoff.

C_5—The large electrolytic can be considered to be part of the power supply and may be reduced in capacitive value or eliminated, depending on the particular supply. The low-value capacitor is usually a monolithic ceramic capacitor. It provides for high-frequency bypass and should have a low series resistance and a high self-resonant frequency.

R_2, R_4—The output resistive divider sets the closed-loop gain of the amplifier according to $A_v = (R_2 + R_4)/R_2$. The values shown provide for a gain of 100 and a typical PSRR of 35 dB. Connecting this divider to the d-c side of the output capacitor increases the supply current drain (by 32 mA for a supply of 14.4 V and $R_2 + R_4 = 222$ Ω) but will reduce any tendency toward crossover distortion.

R_{fb}, C_{fb}—High-frequency roll-off can be controlled with the addition of this series RC combination. Values are approximately $R_{fb} = 20 \times R_2$ and $C_{fb} = 1/(2\pi R_4 f_H)$.

R_{11}, C_{11}—This network is chosen to suppress spurious oscillation. The values shown should work for loads between 2Ω and 16Ω. Some changes may be required depending on factors such as circuit layout, load reactances, and lead length. A factor of 2× should be worst-case variation.

CIRCUIT MUTING

A simple muting circuit is shown in Figure 2. In this circuit, the a-c input signal is attenuated without affecting any d-c levels. The 47 μF capacitor and the 18 kΩ resistor can be eliminated if signal-level ramping is not desired.
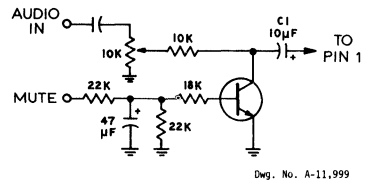
FIGURE 2

**TYPICAL OUTPUT POWER
AS A FUNCTION OF SUPPLY VOLTAGE**
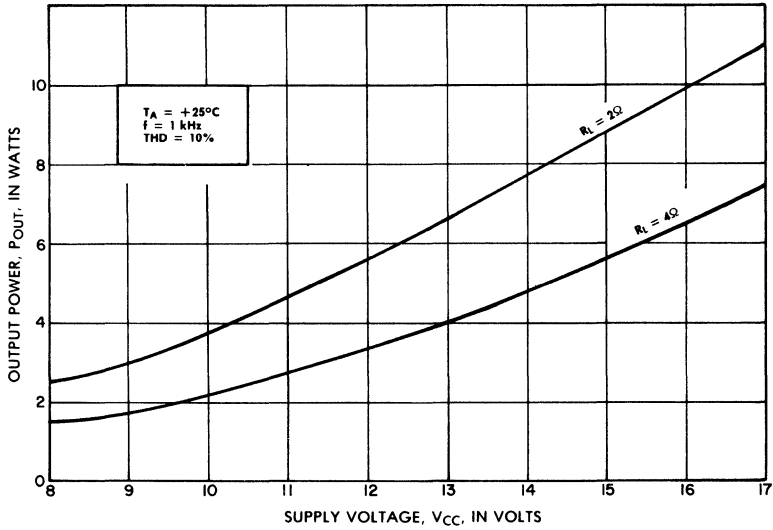
Dwg. No. A-10,463

**TYPICAL OUTPUT DISTORTION
AS A FUNCTION OF OUTPUT POWER**
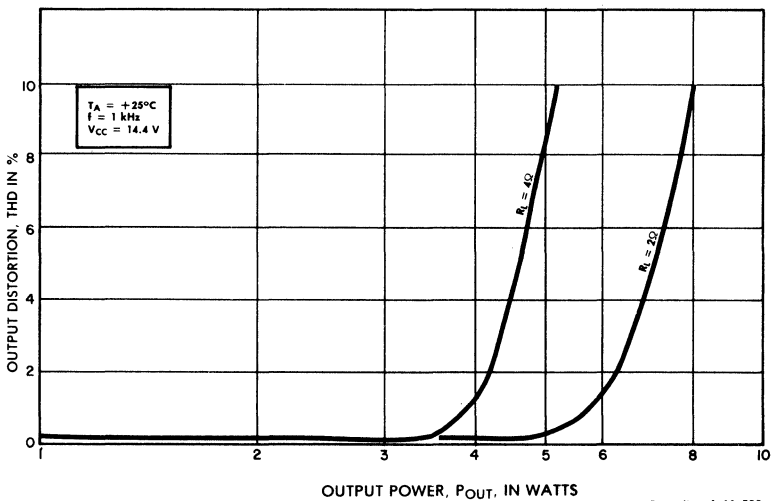
Dwg. No. A-11,782

ULN-3702Z/TDA2008
12-WATT AUDIO POWER AMPLIFIER

FEATURES

- Low External Parts Count
- Low Distortion
- Class B Operation
- Short-Circuit Protected
- Thermal Overload Protected
- Low Noise
- TO-220 Style Package

THE ABILITY TO DRIVE high-power loads in consumer and industrial electronics expands the field of application for Type ULN-3702Z/TDA2008.

The high-gain power amplifier can be used as a vertical output driver in television receivers and video terminals or as a linear d-c motor driver. Its operational-amplifier configuration, with high input impedance and low output impedance, makes it adaptable to many input, output and feedback arrangements.

One modification sets this audio power amplifier apart from Sprague Type ULN-3701Z/TDA2002: The integrated circuit's internal high-voltage shutdown has been disabled. The change allows continuous operation with supply voltages of up to 26 V. With a d-c load current rating of 2.5 A, Type ULN-3702Z/TDA2008 can handle up to 60 watts of power with an appropriate heat sink. It is able to withstand high ambient temperatures, output overloads, and repeated power supply transients without damage.

The amplifier is supplied in a modified five-lead JEDEC Style TO-220 plastic package. The heat sink tab is at ground potential; no insulation is required.

Lead configurations for vertical mounting (ULN-3702V) and for horizontal mounting (ULN-3702ZH) are available. Parts are branded with a partial Sprague Electric part number (ULN3702) and the basic Pro-Electron marking (TDA2008).
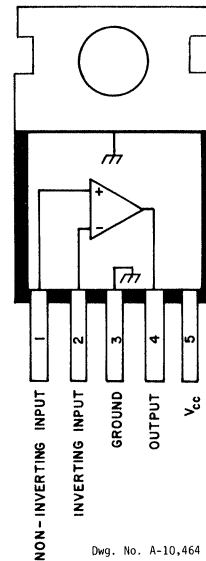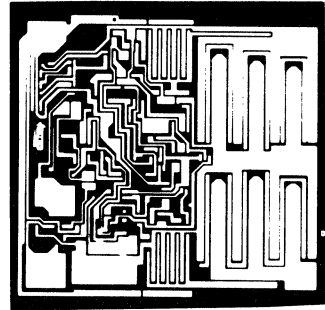
Dwg. No. A-10,464

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 28 V
Peak Supply Voltage (50 ms) .... 40 V
Peak Output Current, I_{OUT} .... 3.5 A
Non-Repetitive Peak Output Current .... 4.5 A
Package Power Dissipation, P_D .... 15 W*
Storage Temperature Range, T_S .... −40°C to +150°C

*Derate at the rate of 0.25 W/°C above T_{TAB} = 90°C

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$,
$V_{CC} = +24$ V, $R_L = 8\Omega$, f = 1 kHz (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
				Limits		
Supply Voltage Range	V_{CC}		8.0	24	26	V
Quiescent Supply Current	I_{CC}	No signal applied	—	80	120	mA
Quiescent Output Voltage	V_4	No signal applied	—	12	—	V
Open Loop Gain	A_e		—	80	—	dB
Closed Loop Gain	A_e		39.5	40	40.5	dB
Total Harmonic Distortion	THD	$P_{OUT} = 0.05$ to 3.5 W, $R_L = 8\Omega$	—	0.2	—	%
		$P_{OUT} = 0.05$ to 5.0 W, $R_L = 4\Omega$	—	0.2	—	%
Audio Power Output	P_{OUT}	THD = 10%, $R_L = 8\Omega$	—	8.0	—	W
		THD = 10%, $R_L = 4\Omega$	10	12	—	W
Input Impedance	Z_1		70	150	—	$k\Omega$
Power Supply Rejection	PSRR	$f_{ripple} = 120$ Hz, $V_{ripple} = 0.5$ V	30	35	—	dB
Equiv. Input Noise Voltage	e_N	f = 40 Hz to 15 kHz	—	4.0	—	μV
Equiv. Input Noise Current	i_N	f = 40 Hz to 15 kHz	—	60	—	pA
Input Sensitivity	e_{in}	$P_{OUT} = 0.5$ W, $R_L = 4\Omega$	—	15	—	mV
		$P_{OUT} = 0.5$ W, $R_L = 8\Omega$	—	21	—	mV
		$P_{OUT} = 8.0$ W, $R_L = 4\Omega$	—	71	—	mV
Input Saturation Voltage	e_{in}		400	600	—	mV_{rms}
Frequency Response (−3 dB)		$C_{fb} = 0.039\mu F$, $R_{fb} = 39\Omega$	40	—	15 k	Hz
Thermal Resistance	$R_{\Theta JT}$		—	—	4.0	°C/W

**TEST CIRCUIT AND
TYPICAL APPLICATION**

Dwg. No. A-10,465A

TYPICAL LOW-COST APPLICATION

Dwg. No. A-10,466A

8

OUTPUT POWER
AS A FUNCTION OF SUPPLY VOLTAGE

$T_A = 25°C$
$f = 1 kHz$
$THD = 10\%$

$R_L = 4\Omega$

$R_L = 8\Omega$

OUTPUT POWER, P_{OUT}, IN WATTS

SUPPLY VOLTAGE, V_{CC}, IN VOLTS
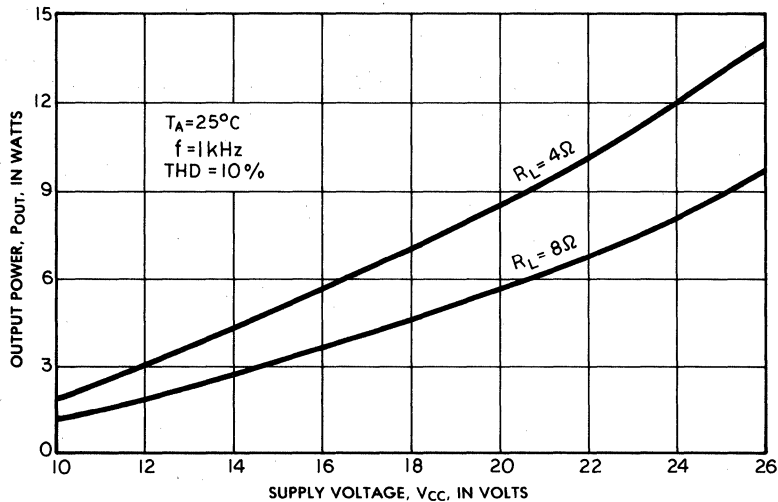
Dwg. No. A-11,409

POWER DISSIPATION
AS A FUNCTION OF OUTPUT POWER

$R_L = 4\Omega$

$R_L = 8\Omega$

$T_A = 25°C$
$f = 1 kHz$
$V_{CC} = 24 V$

PACKAGE POWER DISSIPATION, P_D, IN WATTS

OUTPUT POWER, P_{OUT}, IN WATTS
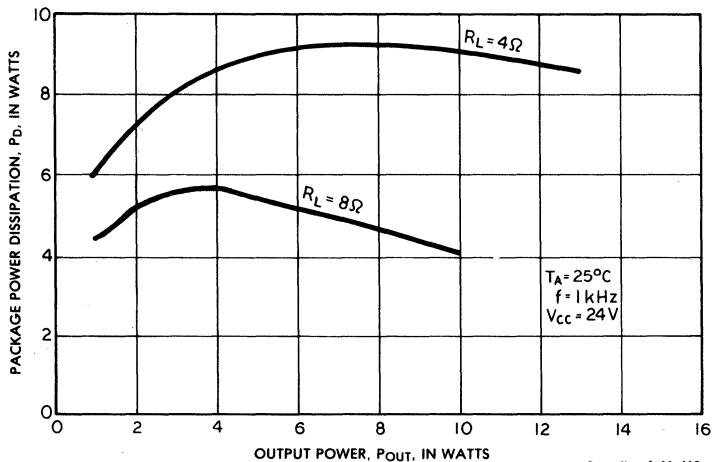
Dwg. No. A-11,410

TYPICAL D-C MOTOR DRIVE APPLICATIONS

10 µF   +24 V   10 µF   +24 V   10 µF   +24 V

V_{IN}
2 kΩ

5 kΩ

500Ω

V_{IN}
10 kΩ   0.001*

1.5 kΩ*

+12 V

*Required for a-c stability
with some loads.

Dwg. No. A-11,334A
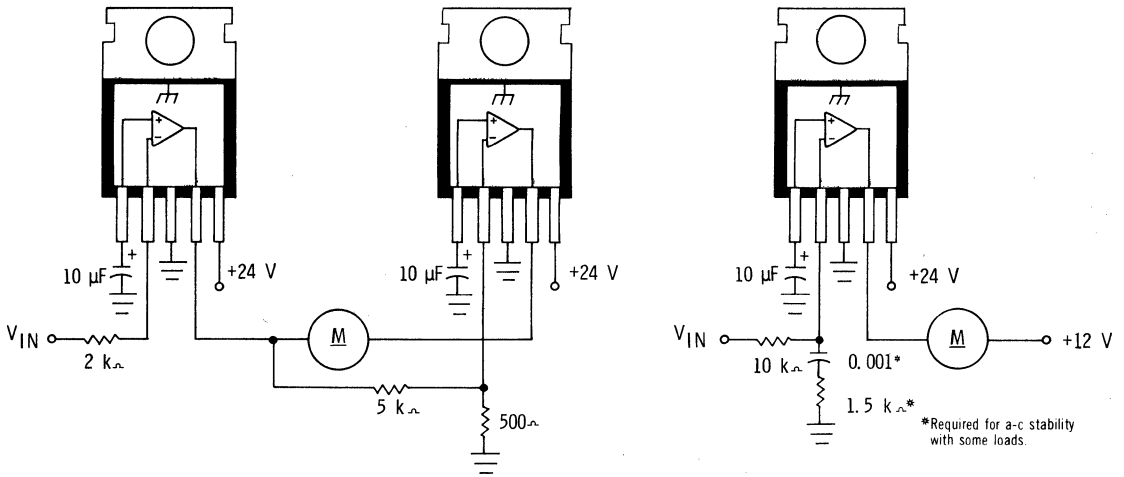
TYPICAL MOTOR CONTROL CURVE

CW

O

CCW

MOTOR SPEED

INPUT VOLTAGE, V_{IN}

Dwg. No. A-11,411

8
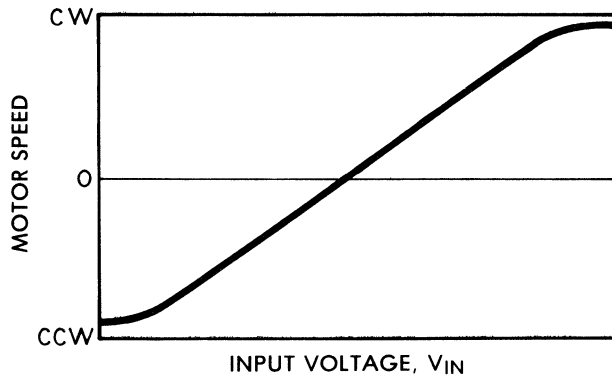
ULN-3703Z / TDA2003
10-WATT AUDIO POWER AMPLIFIER

FEATURES

- Low External Parts Count
- Low Distortion
- Class B Operation
- Short-Circuit Protected
- Thermal Overload Protected
- Low Noise
- High Output-Voltage Swing
- TO-220 Style Package

DESIGNED to drive low-impedance loads down to 1.6 Ω, Type ULN-3703Z/TDA2003 audio power amplifier is ideal for automotive radio, tape player, and CB applications and can deliver 15 W of audio in the bridge configuration or 5 W to 10 W single-ended.

Operating in the harsh automotive environment, this device is capable of withstanding high ambient temperatures, output overloads, and repeated power supply transient voltages without damage. It is protected against a-c/d-c short-circuits, polarity inversions, or open grounds.

Type ULN-3703Z/TDA2003 is supplied in a modified five-lead JEDEC Style TO-220 plastic package. The heat sink tab is at ground potential; no insulation is required. Lead forming for either vertical or horizontal mounting (suffix letter "V" or "H," respectively) is standard.

Parts are branded with both a partial Sprague Electric part number (ULN3703) and the basic Pro-Electron marking (TDA2003).
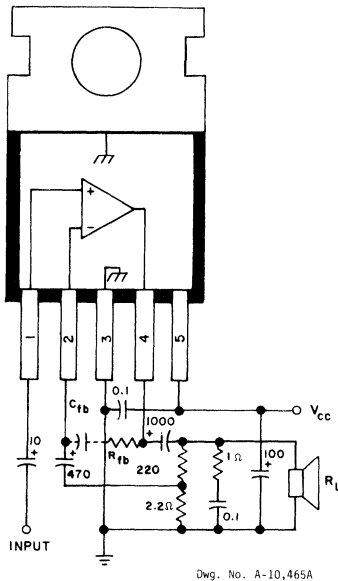
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 28 V
Peak Supply Voltage (50 ms) .... 40 V
Peak Output Current, I_{OUT} .... 3.5 A
Non-Repetitive Peak Output Current .... 4.5 A
Package Power Dissipation, P_D .... 20 W*
Storage Temperature Range, T_S .... −40°C to +150°C

*Derate at the rate of 0.33 W/°C above T_{TAB} = +90°C

NON–INVERTING INPUT 1
INVERTING INPUT 2
GROUND 3
OUTPUT 4
V_{CC} 5
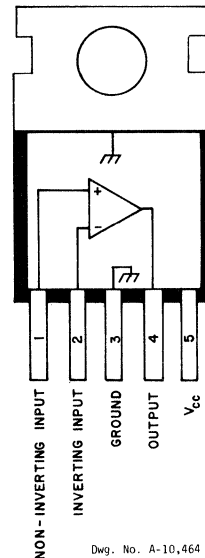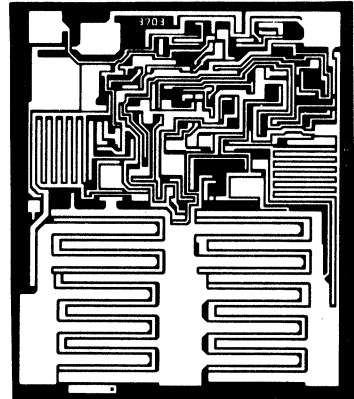
Dwg. No. A-10,464
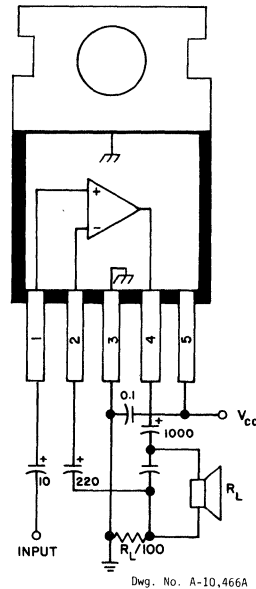
ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = +14.4\,V$, $R_L = 4\Omega$, $f = 1\,kHz$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
			Limits			
Supply Voltage Range	V_{CC}		8.0	—	18	V
Quiescent Supply Current	I_{CC}	No signal applied	—	44	—	mA
Quiescent Output Voltage	V_4	No signal applied	6.1	6.9	7.7	V
Open Loop Gain	A_e		—	80	—	dB
Closed Loop Gain	A_e		39.5	40	40.5	dB
Total Harmonic Distortion	THD	$P_{OUT} = 0.05$ to $4.5\,W$	—	0.15	—	%
		$P_{OUT} = 0.05$ to $7.0\,W$, $R_L = 2\Omega$	—	0.15	—	%
Audio Power Output	P_{OUT}	THD = 10%	5.5	6.0	—	W
		THD = 10%, $R_L = 3.2\Omega$	—	7.5	—	W
		THD = 10%, $R_L = 2\Omega$	8.0	10	—	W
		THD = 10%, $R_L = 1.6\Omega$	—	12	—	W
Efficiency	η	$P_{OUT} = 6.0\,W$	—	69	—	%
		$P_{OUT} = 10\,W$, $R_L = 2\Omega$	—	65	—	%
Input Impedance	Z_1		70	150	—	kΩ
Power Supply Rejection	PSR	$f_{ripple} = 120\,Hz$, $V_{ripple} = 0.5\,V$	30	36	—	dB
Equiv. Input Noise Voltage	e_N	$f = 22\,Hz$ to $22\,kHz$	—	1.0	5.0	μV
Equiv. Input Noise Current	i_N	$f = 22\,Hz$ to $22\,kHz$	—	60	200	pA
Input Sensitivity	e_{in}	$P_{OUT} = 0.5\,W$	—	14	—	mV
		$P_{OUT} = 0.5\,W$, $R_L = 2\Omega$	—	10	—	mV
		$P_{OUT} = 6.0\,W$	—	55	—	mV
		$P_{OUT} = 10\,W$, $R_L = 2\Omega$	—	50	—	mV
Input Saturation Voltage	e_{in}		300	—	—	mV
Frequency Response ($-3\,dB$)		$C_{fb} = 0.039\,\mu F$, $R_{fb} = 39\Omega$, $P_{OUT} = 1.0\,W$	40	—	15 k	Hz
Thermal Resistance	$R_{\Theta JT}$		—	—	3.0	°C/W

TEST CIRCUIT AND TYPICAL APPLICATION
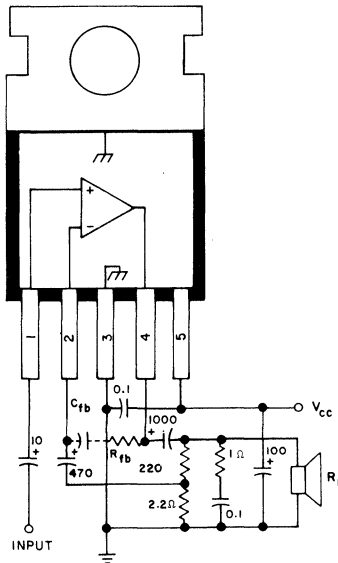
Dwg. No. A-10,465A

ULN-3705M
LOW-VOLTAGE AUDIO POWER AMPLIFIER

FEATURES

- Wide Operating Voltage Range
- Low Quiescent Current
- A-C Short-Circuit Protection
- Low External Parts Count
- Low Distortion
- 42 dB Voltage Gain
- Low Noise

PROVIDING a low-cost, compact alternative to discrete transistor amplifiers, the Type ULN-3705M integrated circuit is ideal for application as a headphone driver in portable radios, tape players, and other battery-operated equipment. The low-power audio amplifier's wide frequency response and low noise ensure premium performance.

The amplifier will operate (at reduced volume) with supply voltages as low as 1.8 V without a significant increase in distortion. This feature allows operation with a 3 V battery supply and minimizes concern about weak batteries. The class AB audio amplifier has low quiescent current drain for maximum battery life.

This device is rated for operation with supply voltages up to 12 V. Similar devices for operation up to 18 V (ULN-2283B) are described in Sprague Engineering Bulletin 27117.21.

The Type ULN-3705M audio amplifier is supplied in an 8-pin mini-DIP plastic package. A copper alloy lead frame gives the amplifier enhanced power dissipation ratings.

DECOUPLE 1		8 INPUT
POWER GROUND 2		7 NC
SIGNAL GROUND 3		6 NC
OUTPUT 4		V_{CC} 5 SUPPLY
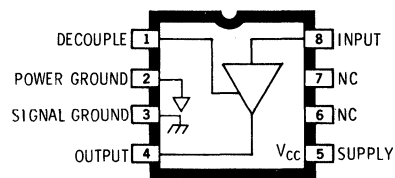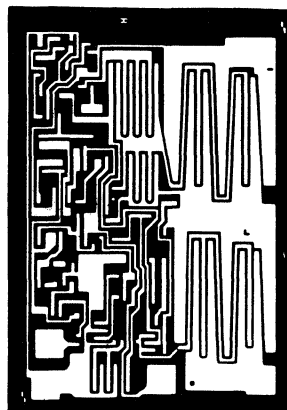
Dwg. No. A-11,715

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 12 V
Package Power Dissipation, P_D .... See Graph
Operating Temperature Range, T_A .... −20°C to +85°C
Storage Temperature Range, T_S .... −65°C to +150°C

ELECTRICAL CHARACTERISTICS at T_A = +25°C,
V_{CC} = 6 V, R_L = 32Ω, f_{in} = 400 Hz (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
				Limits		
Supply Voltage Range	V_{CC}		1.8	6.0	9.0	V
Quiescent Supply Current	I_{CC}	V_{CC} = 4.5 V	—	6.0	—	mA
		V_{CC} = 6.0 V	—	7.0	15	mA
		V_{CC} = 9.0 V	—	10	20	mA
Voltage Gain	A_V		—	42	—	dB
Audio Power Output	P_{OUT}	R_l = 8Ω, V_{CC} = 4.5 V, THD = 10%	—	220	—	mW
		R_l = 8Ω, V_{CC} = 6.0 V, THD = 10%	250	430	—	mW
		R_l = 16Ω, V_{CC} = 4.5 V, THD = 10%	—	125	—	mW
		R_l = 16Ω, V_{CC} = 6.0 V, THD = 10%	150	240	—	mW
		R_l = 16Ω, V_{CC} = 9.0 V, THD = 10%	—	600	—	mW
		R_l = 32Ω, V_{CC} = 4.5 V, THD = 10%	—	60	—	mW
		R_l = 32Ω, V_{CC} = 6.0 V, THD = 10%	85	110	—	mW
		R_l = 32Ω, V_{CC} = 9.0 V, THD = 10%	—	310	—	mW
Distortion	THD	P_{OUT} = 50 mW, R_l = 32Ω	—	0.4	1.0	%
		P_{OUT} = 50 mW, R_l = 16Ω	—	0.5	—	%
Output Noise	V_{out}	Input Shorted, BW = 80 kHz	—	225	—	μV
Input Resistance	R_{IN}	Pin 8	—	250	—	kΩ
Power Supply Rejection	PSRR	C_D (Pin 1) = 500 μF, f = 120 Hz	—	34	—	dB

TEST CIRCUIT
AND TYPICAL APPLICATION
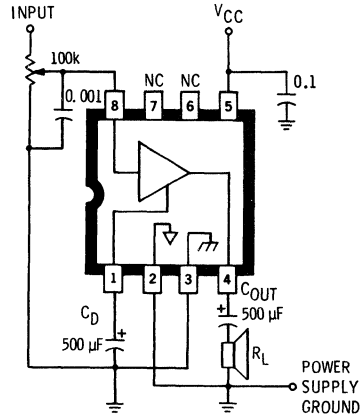
Dwg. No. A-11,716A

8

**ALLOWABLE AVERAGE
PACKAGE POWER DISSIPATION
AS A FUNCTION OF TEMPERATURE**

Allowable Package Power Dissipation, P_D, in Watts vs Temperature in °C

CASE TEMPERATURE, $\theta_{JC} = 55°C/W$

AMBIENT TEMPERATURE, $\theta_{JA} = 80°C/W$
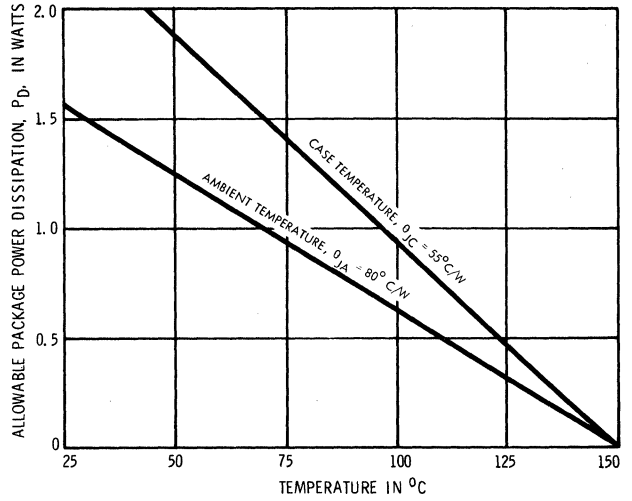
Dwg. No. A-11,727

**TYPICAL OUTPUT POWER
AS A FUNCTION OF SUPPLY VOLTAGE**

Output Power, P_{OUT}, in Watts vs Supply Voltage, V_{CC}, in Volts

THD = 10%
f_{in} = 400 Hz

$R_L = 8\,\Omega$
$R_L = 16\,\Omega$
$R_L = 32\,\Omega$
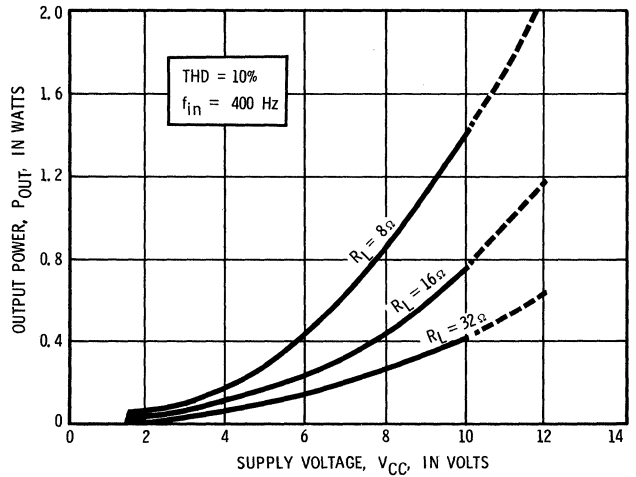
Dwg. No. A-11,720A

TYPICAL FREQUENCY RESPONSE

Voltage Gain, A_V, in dB vs Frequency, f_{in}, in Hz

C_{OUT} = 500 µF
C_{OUT} = 250 µF
C_{OUT} = 100 µF

V_{CC} = 3 to 9 V
R_L = 8 Ω
C_D = 100 to 250 µF

Dwg. No. A-11,717

8—30
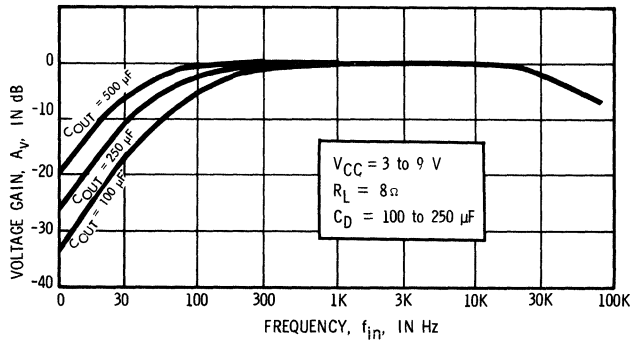
TYPICAL CHARACTERISTICS

**TOTAL HARMONIC DISTORTION
AT 8Ω LOAD**

$R_L = 8 \wedge$
$f_{in} = 400$ Hz

OUTPUT DISTORTION, THD, IN %

OUTPUT POWER, P_{OUT}, IN mW

$V_{CC} = 4.5$ V

$V_{CC} = 6$ V
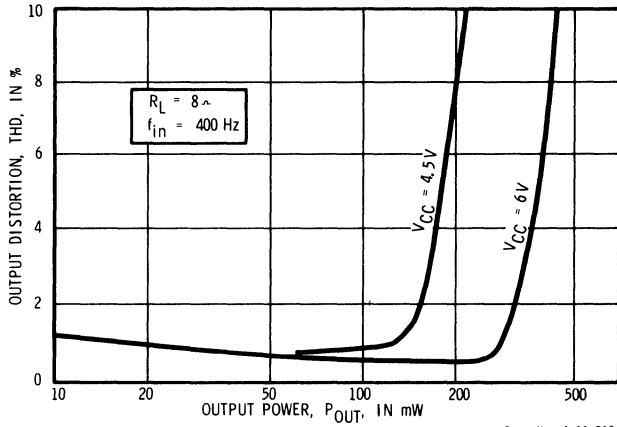
Dwg. No. A-11,718

**TOTAL HARMONIC DISTORTION
AT 16Ω LOAD**

$R_L = 16 \wedge$
$f_{in} = 400$ Hz

OUTPUT DISTORTION, THD, IN %

OUTPUT POWER, P_{OUT}, IN mW

$V_{CC} = 4.5$ V

$V_{CC} = 6$ V

$V_{CC} = 9$ V
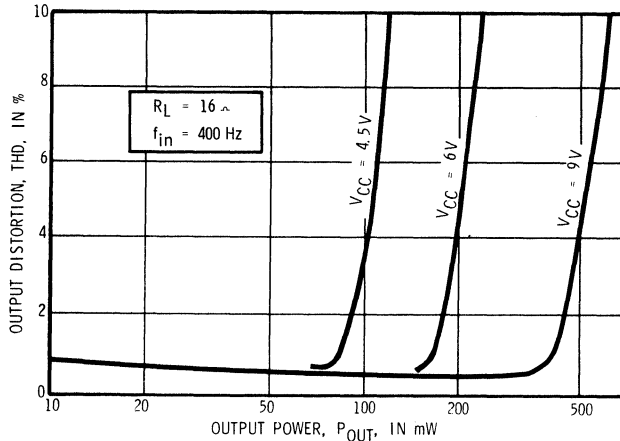
Dwg. No. A-11,719

**TOTAL HARMONIC DISTORTION
AT 32Ω LOAD**

$R_L = 32 \wedge$
$f_{in} = 400$ Hz

OUTPUT DISTORTION, THD, IN %

OUTPUT POWER, P_{OUT}, IN mW

$V_{CC} = 4.5$ V

$V_{CC} = 6$ V

$V_{CC} = 9$ V

Dwg. No. A-11,990

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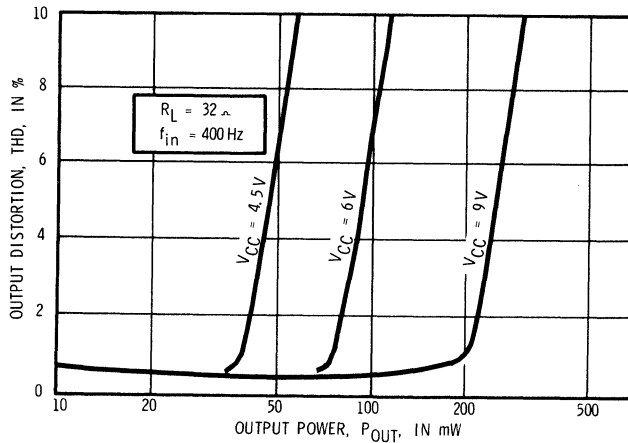
TYPICAL CHARACTERISTICS (Continued)

PACKAGE POWER DISSIPATION AT 8Ω LOAD
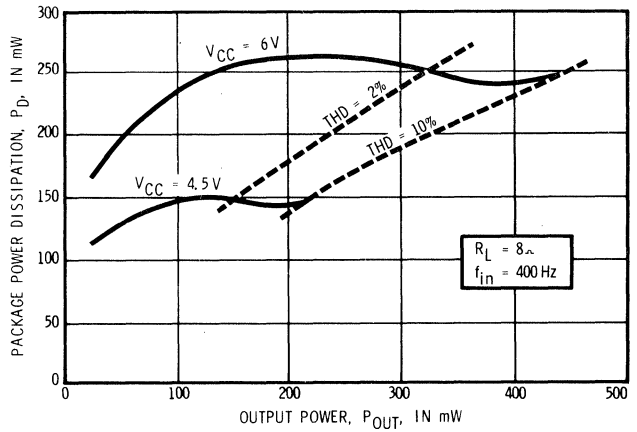
Dwg. No. A-11,721

PACKAGE POWER DISSIPATION AT 16Ω LOAD
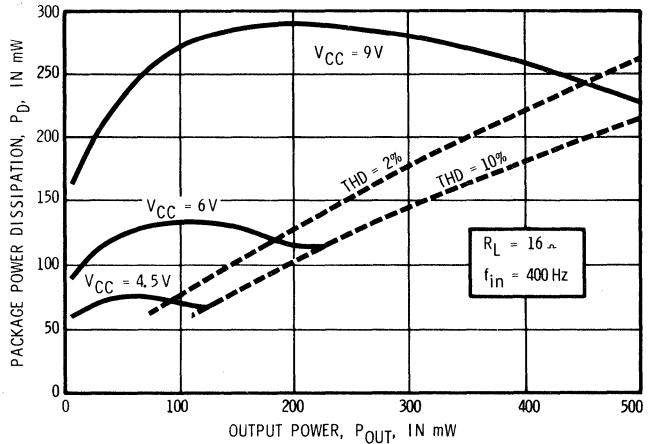
Dwg. No. A-11,722A

PACKAGE POWER DISSIPATION AT 32Ω LOAD
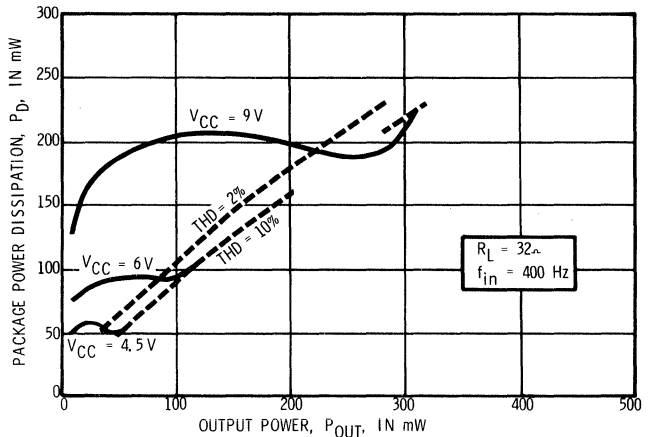
Dwg. No. A-12,025A

TYPICAL CHARACTERISTICS (Continued)

QUIESCENT SUPPLY CURRENT
AS A FUNCTION OF SUPPLY VOLTAGE

Dwg. No. A-11,728
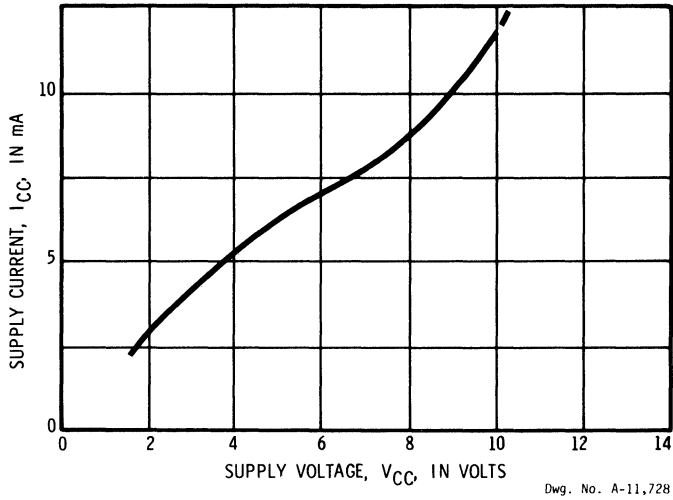
POWER SUPPLY REJECTION RATIO
AS A FUNCTION OF FREQUENCY

Dwg. No. A-10,838
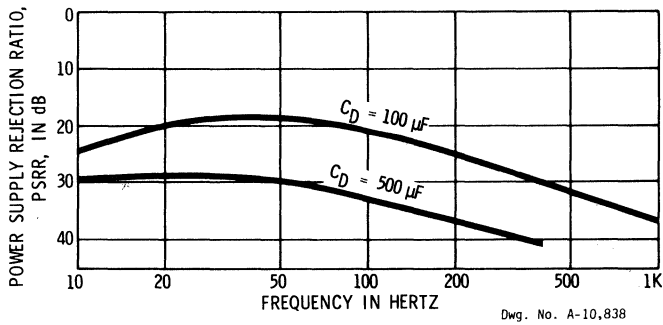
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APPLICATIONS INFORMATION

Selection of power-supply voltage and speaker impedance allows a designer to choose audio power levels within the allowable package power dissipation rating for any maximum operating temperature. No unique precautions are necessary when designing with this device. It is stable and a-c short-circuit immune.

External component selection for this low-power amplifier involves only two capacitors — one for output coupling and one for feedback and ripple decoupling. The coupling capacitor value should be selected to provide the desired low-frequency cutoff with the chosen load impedance. The decoupling capacitor should be chosen for both low-frequency audio rolloff and supply-ripple rejection.

Ripple rejection is not practical to calculate due to the large number of mechanisms involved. A 500 μF capacitor achieves typically 34 dB rejection at 120 Hz.

The high gain and the high input impedance of the power amplifier recommend use of this device in many diverse applications. However, the input stage does have other characteristics that should be taken into account for best results. The input is referenced to ground for internal biasing and must be provided with a d-c path to ground. A current of typically 1 μA flows from the input through the volume con-

trol. This produces an IR drop that is multiplied by the closed loop d-c gain of the amplifier and appears as an error in output centering. This recommends a value of 200 kΩ or less for the volume control; values of less than 100 kΩ are preferred.

The selection of amplifier load impedance involves more than just consideration of the desired power output. A low load impedance will produce the highest power output for any given supply voltage. Higher impedances will furnish significant reduction in harmonic distortion and improvement in overall repeatability in power output capacity.

Special steps toward minimizing tendencies towards instabilities of all types were taken in the design of this device. However, as with all high-gain circuits, care should be given to printed wiring board layout to avoid undesirable effects. Inputs and outputs should be well separated and should avoid common-mode impedances wherever possible. For best performance, connect low-level input-signal ground terminals and the decoupling capacitor ground terminal together at pin 3 (signal ground); connect the high-level speaker ground terminal and the power supply ground terminal together at pin 2 (power ground). The signal ground and the power ground should be interconnected at only one point.

ULN-3784B
4-WATT AUDIO POWER AMPLIFIER

FEATURES

- Low External Parts Count
- Wide Supply-Voltage Range (To 32 V)
- Single Power Supply
- 34 dB Internally Fixed Gain
- High Input Impedance
- Bandwidth Limited
- A-C Short-Circuit Protection
- Thermal Overload Protection
- Directly Replaces LM384N
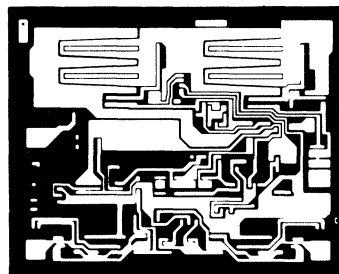
A MINIMUM of external components is needed to obtain high-quality audio from the Type ULN-3784B integrated circuit in communications, automotive, and consumer applications.

The audio power amplifier is supplied in a 14-pin dual in-line plastic package with heat-sink contact tabs. The lead configuration enables attachment of an inexpensive heat sink for increased power dissipation capability, and use of a standard integrated circuit socket or printed wiring board layout.

With a 24 V supply, Type ULN-3784B delivers a minimum of 4 W of audio into an 8Ω load. Output power with a 28 V supply is typically 4.8 W of low-distortion audio into a 16Ω load.

Type ULN-3784B is pin-compatible with, and significantly improves upon, several older designs. Its higher supply-voltage rating allows it to replace the LM380N, LM384N, and Sprague Types ULN-2280B and ULN-2281B with a wider margin of protection against supply transients. Internal bandwidth limiting provides a significant immunity to r-f not found in many other integrated amplifiers.
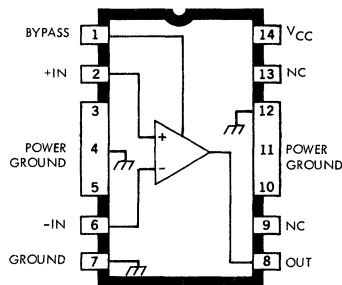
Dwg. No. A-11,681A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 32 V
Peak Output Current, I_{OUT} . . . . 1.2 A
Package Power Dissipation, P_D . . . . See Graph
Operating Temperature Range, T_A . . . . −20°C to +85°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 24\,V$, $R_L = 8\,\Omega$, $f_{in} = 1\,kHz$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
			Limits			
Supply Voltage Range	V_{CC}		9.0	24	28	V
Quiescent Supply Current	I_{CC}	$V_{in} = 0\,V$	—	20	—	mA
Quiescent Output Voltage	V_{OQ}	$V_{in} = 0\,V$, See Note 1	—	12	—	V
Voltage Gain	A_v	$P_{out} = 0\,W$	31	34	37	dB
Total Harmonic Distortion	THD	$P_{out} = 50\,mW$, $R_L = 8\,\Omega$, $V_{CC} = 24\,V$	—	0.2	—	%
		$P_{out} = 50\,mW$, $R_L = 16\,\Omega$, $V_{CC} = 28\,V$	—	<0.2	—	%
		$P_{out} = 4\,W$, $R_L = 8\,\Omega$, $V_{CC} = 24\,V$	—	<0.3	5.0	%
Audio Output Power	P_{out}	$R_L = 8\,\Omega$, $V_{CC} = 24\,V$, THD = 5%	4.0	5.0	—	W
		$R_L = 16\,\Omega$, $V_{CC} = 28\,V$, THD = 5%	4.0	4.8	—	W
Input Impedance	Z_{in}	Each Input	140	170	—	$k\Omega$
Power Supply Rejection	PSRR	$P_{out} = 0\,W$, f = 120 Hz	—	30	—	dB
Equiv. Input Noise Voltage		f = 20 Hz to 20 kHz	—	60	—	μV_{rms}
Bandwidth ($-3\,dB$)	BW	$P_{out} = 1\,W$, See Note 2	—	100	—	kHz

NOTES: 1. The quiescent output voltage typically equals ½ the supply voltage.
2. Unity gain typically occurs between 10 MHz and 100 MHz.

TEST CIRCUIT

Dwg. No. A-11,396A
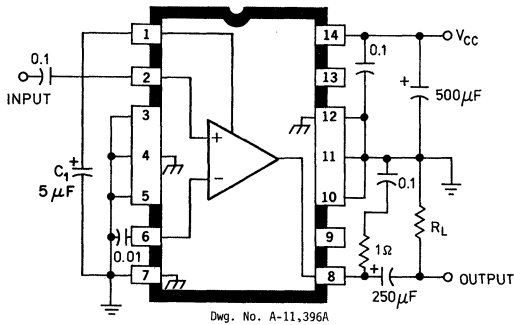
ALLOWABLE POWER DISSIPATION
AS A FUNCTION OF AMBIENT TEMPERATURE
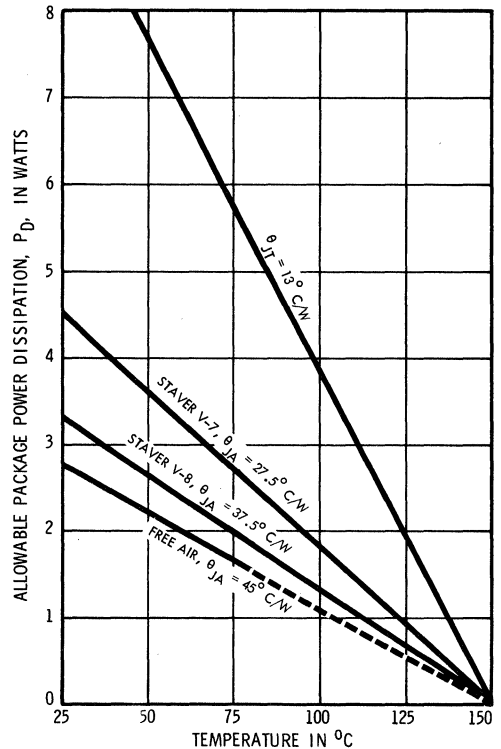
Dwg. No. A-11,793A

TYPICAL CHARACTERISTICS
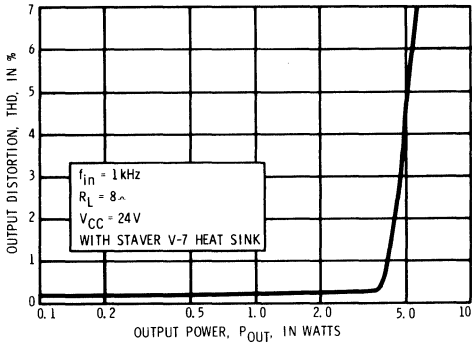
DISTORTION AS A FUNCTION OF OUTPUT POWER

$f_{in} = 1\,kHz$
$R_L = 8\,\Omega$
$V_{CC} = 24\,V$
WITH STAVER V-7 HEAT SINK

OUTPUT DISTORTION, THD, IN %

OUTPUT POWER, P_{OUT}, IN WATTS

Dwg. No. A-11,683A

DISTORTION AS A FUNCTION OF FREQUENCY

$V_{CC} = 24\,V$
$R_L = 8\,\Omega$

$P_{out} = 2\,W$
$P_{out} = 100\,mW$

OUTPUT DISTORTION, THD, IN %

FREQUENCY, f, IN Hz

Dwg. No. A-12,354

PSRR AS A FUNCTION OF FREQUENCY

$C_1 = 4.7\,\mu F$
$C_1 = 2.2\,\mu F$
$V_{CC} = 24\,V$
$V_{in} = 1\,mV_{rms}$
$C_1 = 0$

POWER SUPPLY REJECTION RATIO, PSRR, IN dB

FREQUENCY, f, IN Hz

Dwg. No. A-12,355

VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

$V_{CC} = 24\,V$
$R_L = \infty$
$V_{OUT} = 4\,V_{rms}$

VOLTAGE GAIN, A_V, IN dB

FREQUENCY, f, IN Hz

Dwg. No. A-11,400A

8
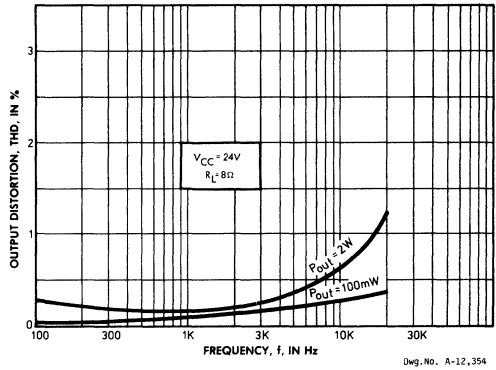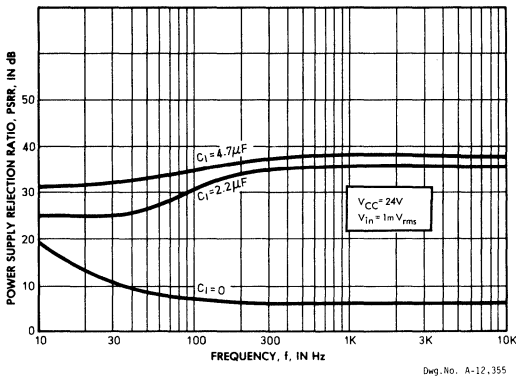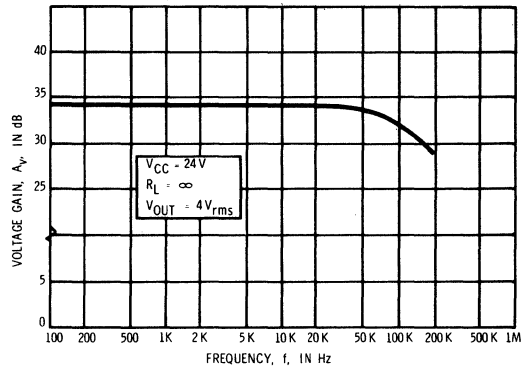
THERMAL FACTORS
AND ULN-3784B OPERATION

Thermal factors must be considered in achieving reliable operation of Type ULN-3784B. Guidelines given here provide the circuit-design engineer with information on maintaining IC junction temperature below safe limits.

The graphs below show package power dissipation as a function of output power over a wide range of supply voltage with a load resistance of 8Ω or 16Ω. Lines indicating 3% distortion and 5% distortion are shown as guides to trade-offs between supply voltages, package power dissipation, and upper-limit distortion. As the power supply voltage increases for any output power requirement, distortion decreases and package power dissipation increases.

Package power dissipation figures must be taken from the highest point on the supply voltage curve. Note that although supply voltage is normally specified at the rated audio-output power, it will usually increase for reduced audio-output levels.
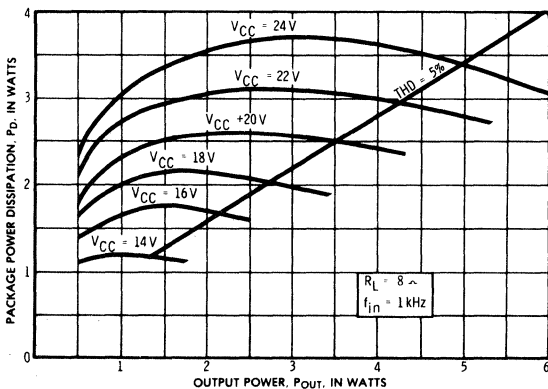
Dwg. No. A-12,016

POWER DISSIPATION AS A FUNCTION OF OUTPUT POWER (8Ω LOAD)

POWER DISSIPATION AS A FUNCTION OF OUTPUT POWER (16Ω LOAD)
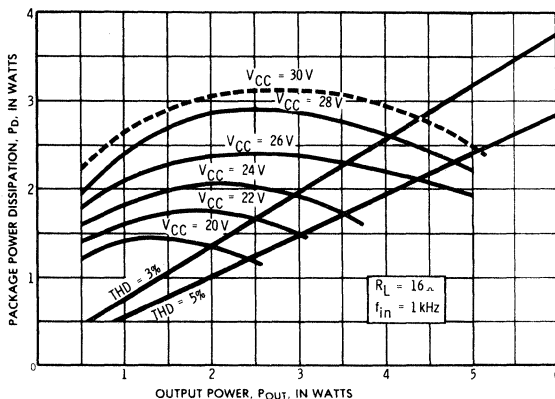
Dwg. No. A-12,015

CIRCUIT DESIGN

If design values of audio output power, distortion, and maximum ambient temperature have been selected, optimal speaker impedance, supply voltage, as well as heat-sink requirements can be determined from the curves below and on the previous page.

For an output of 4.5 W at 5% distortion and a maximum ambient temperature of +50°C:

R_L	8Ω	16Ω	Specified
V_{CC}	22.5 V	26.5 V	From Graph
$P_{D(max)}$	3.2 W	2.6 W	From Graph (determines heat sink)
P_D	3.1 W	2.2 W	From Graph at V_{CC} and P_{OUT}
$P_D + P_{OUT}$	7.6 W	6.7 W	Calculated
I_{CC}	338 mA	253 mA	Calculated (determines supply current)

The Allowable Package Power Dissipation graph shows that the Staver V-7 heat sink is required for the 8Ω, 22.5 V design, while the smaller Staver V-8 heat sink is just adequate for the 16Ω, 26.5 V design.

The preceding appears to indicate that the best choice is an output impedance of 16Ω with its higher efficiency and smaller heat sink requirements. If lower distortion is required, the higher impedence load with the higher supply voltage becomes even better. However, if an unregulated supply is used, the designer may prefer the 8Ω load, since the absolute maximum supply voltage rating is 32 V.

**QUIESCENT SUPPLY CURRENT
AS A FUNCTION OF SUPPLY VOLTAGE**
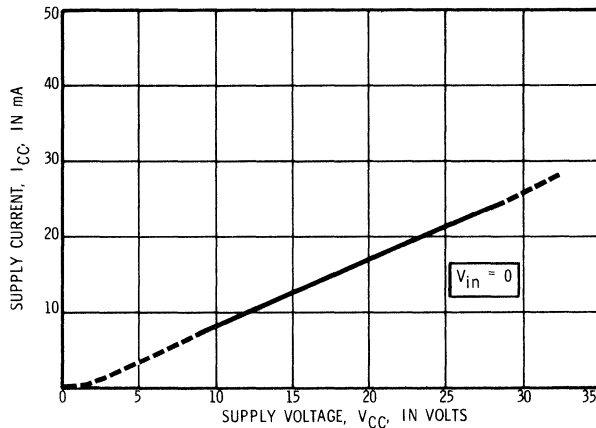
Dwg. No. A-11,682

TYPICAL APPLICATIONS

AMPLIFIER WITH COMPLETE TONE CONTROLS

Dwg. No. A-11,403B

LOW-COST PHONOGRAPH

Dwg. No. A-11,404B

AMPLIFIER WITH BASS-BOOST NETWORK

Dwg. No. A-11,405B

SECTION 9—HALL EFFECT DEVICES

*New Product. Contact factory in Concord, N.H., for information.

9

SELECTION GUIDE TO HALL EFFECT DEVICES

Device Type	Switch Points (Gauss)		Outputs
UGN-3013T/U	225	300	1
UGN/UGS-3019T/U	300	420	1
UGN/UGS-3020T/U	165	220	1
UGN/UGS-3030T/U	110	160	1
UGN-3035U	− 25	+ 25	1
UGN-3040T/U	100	150	1
UGN/UGS-3075T/U	− 100	+ 100	1
UGN/UGS-3076T/U	− 100	+ 100	1
UGN-3201M	300	450	2
UGN-3203M	100	235	2
UGN-3220S	160	220	2
UGN-3501M	Linear		Push-Pull
UGN-3501T/U	Linear		1
UGN-3503U	Linear		1
UGN-3604M	Linear		Push-Pull
UGN-3605M	Linear		Push-Pull

Additional information on all
Hall Effect devices is available from:

Sprague Electric Company
Hall Effect IC Marketing
70 Pembroke Road
Concord, New Hampshire 03301
(603) 224-1961

UGN-3013T SOLID-STATE
LOW-COST HALL EFFECT DIGITAL SWITCH

FEATURES

- Operate from 4.5 V to 16 V D-C Power Source
- Activates With Small, Commercially Available Permanent Magnets
- Solid-State Reliability — No Moving Parts
- Small Size
- Constant Amplitude Output
- Output Compatible With All Digital Logic Families

THE SPRAGUE TYPE UGN-3013T is a low-cost magnetically-activated electronic switch. Each device consists of a voltage regulator, a Hall voltage generator, amplifier, Schmitt trigger, and an open collector output stage integrated in a single monolithic silicon chip.

The on-board regulator permits operation over a wide variation of supply voltages. The circuit output can be interfaced directly with bipolar or MOS logic circuits.

UGN-3013T integrated circuits are packaged in the miniature 3-pin single output plastic "T" pack.

Dwg. NO. A-11,002
FUNCTIONAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC} . . . . 17 V
Magnetic Flux Density, B . . . . Unlimited
Output OFF Voltage, $V_{OUT(OFF)}$ . . . . 17 V
Output ON Current, I_{SINK} . . . . 25 mA
Operating Temperature Range, T_A . . . . 0°C to +70°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS at V_{CC} = 4.5 V to 16 VDC, T_A = +25°C

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Operate Point	B_{OP}		—	300	450	Gauss
Release Point	B_{RP}		25	225	—	Gauss
Hysteresis	B_H		30	75	—	Gauss
Output Saturation Voltage	V_{SAT}	B ≥ 450 Gauss, I_{SINK} = 15 mA	—	120	400	mV
Output Leakage Current	I_{OFF}	B ≤ 25 Gauss, V_{OUT} = 16 V	—	0.1	20	μA
Supply Current	I_{CC}	V_{CC} = 5 V, Output open	—	7.0	9.0	mA
		V_{CC} = 12 V, Output open	—	12	16	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	15	—	ns
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	100	—	ns

9

OPERATION

The output transistor is normally "off" when the magnetic field perpendicular to the surface of the chip is below the threshold or "operate point." When the field exceeds the "operate point," the output transistor switches "on" and is capable of sinking 25 mA of current.

The output transistor switches "off" when the magnetic field is reduced below the "release point" which is less than the "operate point." This is illustrated graphically in the transfer characteristics curve. The hysteresis characteristic provides for unambiguous or non-oscillatory switching.

The magnetic flux density is indicated for the most sensitive area of the device. This area is centrally located and 0.032'' ±0.002'' (0.81 ±0.05 mm) below the branded surface of the T package and 0.012'' ±0.002'' (0.30 ±0.05 mm) below the branded surface of the U package.

For reference purposes, both an Alnico VIII magnet, 0.212'' (5.38 mm) in diameter and 0.187'' (4.75 mm) long and a samarium cobalt magnet, 0.100'' (2.54 mm) square and 0.040'' (1.02 mm) thick, are approximately 1200 gauss at its surface.

The flux density decays at a high rate as the distance from a pole increases.

As an example, using the Alnico VIII magnet referenced above in good alignment and the pole surface in contact with the branded surface of the package, the flux density at the active Hall sensing area of the device would be approximately 850 gauss.

The flux density would drop to approximately 600 gauss with an air-gap between the package and the magnet of 0.031'' (0.79 mm).

TRANSFER CHARACTERISTICS SHOWING HYSTERESIS

Dwg. No. A-11,003

These Hall effect devices are also available in a miniature 3-pin plastic "U" package. The "T" package is 0.080'' (2.03 mm) thick; the "U" package is 0.061'' (1.54 mm) thick. All other dimensions are identical.

UGN-3019T/U AND UGS-3019T/U
LOW-COST HALL EFFECT DIGITAL SWITCHES

FEATURES

- D-C Operation from 4.5 V to 24 V
- Operable with a Small Permanent Magnet
- High Reliability — No Moving Parts
- Small Size
- Constant Amplitude Output
- Output Compatible with All Digital Logic Families

THESE low-cost, magnetically-activated electronic switches use the Hall Effect to sense a magnetic field. Each circuit consists of a voltage regulator, Hall cell, signal amplifier, Schmitt trigger, and current-sinking output stage on a monolithic silicon chip.

The switches' outputs can be used directly with bipolar or MOS logic circuits. The on-board regulator ensures stable operation over a wide range of supply voltages. Operation over an extended temperature range is made possible by carefully matching integrated circuit components.

Dwg. NO. A-11,002

FUNCTIONAL BLOCK DIAGRAM
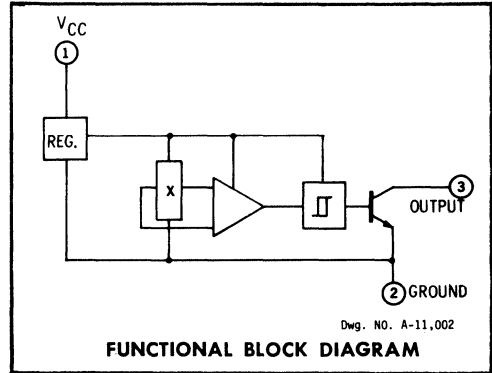
Type UGN-3019T/U and UGS-3019T/U digital switches are available in two three-pin single-output plastic packages: The "T" package is 80 mils (2.03 mm) thick; the "U" package is 60.5 mils (1.54 mm) thick.

ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC} . . . . 25 V
Magnetic Flux Density, B . . . . Unlimited
Output OFF Voltage, V_{OUT} . . . . 25 V
Output ON Current, I_{SINK} . . . . 25 mA
Storage Temperature Range, T_S . . . . −65°C to +150°C
Operating Temperature Range, T_A
    UGS-3019T/U . . . . −55°C to +150°C
    UGN-3019T/U . . . . −20°C to +85°C

ELECTRICAL CHARACTERISTICS at V_{CC} = 4.5 V to 24 V, T_A = +25°C (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
				Limits		
Operate Point*	B_{OP}		—	420	500	Gauss
Release Point*	B_{RP}		125	300	—	Gauss
Hysteresis	B_H		50	120	—	Gauss
Output Saturation Voltage	V_{SAT}	B ≥ 500 Gauss, I_{SINK} = 20 mA	—	100	400	mV
Output Leakage Current	I_{OFF}	B ≤ 125 Gauss, V_{OUT} = 24 V	—	0.1	1.0	μA
Supply Current	I_{CC}	V_{CC} = 4.5 V, Output Open	—	2.5	5.0	mA
		V_{CC} = 24 V, Output Open	—	3.5	7.0	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 820Ω, C_L = 20 pF	—	100	—	ns
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 820Ω, C_L = 20 pF	—	500	—	ns

*Magnetic flux density is measured at most sensitive area of device, located 0.032'' ±0.002 (0.81 ±0.05 mm) below the branded face of the "T" package and 0.012'' ±0.002'' (0.305 ±0.05 mm) below the branded face of the "U" package.

OPERATION

The output transistor is normally OFF when the magnetic field perpendicular to the surface of the chip is below the threshold or Operate Point. When the field exceeds the Operate Point, the output transistor switches ON and is capable of sinking 25 mA of current. Selections to 30 mA are available.

The output transistor switches OFF when the magnetic field is reduced below the Release Point (which is less than the Operate Point). This is illustrated in the transfer characteristics graph. The hysteresis characteristic provides for unambiguous or non-oscillatory switching.

The simplest form of magnet that will operate the Hall Effect digital switch is a bar magnet as shown. Other methods are possible.

In the illustration, the magnet's axis is on the centerline of the packaged device and the magnet is moved toward and away from the device. Also, note the orientation of the magnet's south pole in relation to the branded surface of the package.

The magnetic flux density is indicated for the most sensitive area of the device. This area is 0.032″ ±0.002″ (0.81 ±0.05 mm) below the branded surface of the "T" package, 0.012″ ±0.002″ (0.305 ±0.05 mm) below the branded surface of the "U" package.
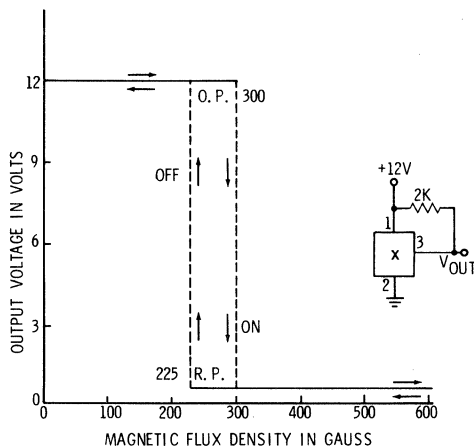
For reference purposes, both an Alnico VIII magnet, 0.212″ (5.38 mm) in diameter and 0.187″ (4.75 mm) long and a samarium cobalt magnet, 0.100″ (2.54 mm) square and 0.040″ (1.02 mm) thick, are approximately 1200 gauss at their surfaces.

The flux density decays at a high rate as the distance from a pole increases. As an example, using the Alnico VIII magnet referenced above in good alignment and with the pole surface in contact with the branded surface of the package, the flux density
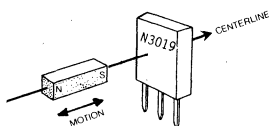
TRANSFER CHARACTERISTICS SHOWING HYSTERESIS
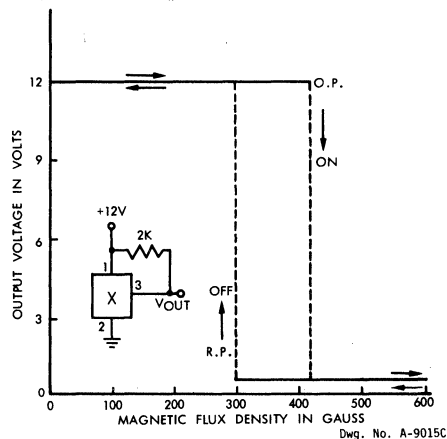
Dwg. No. A-9015C

at the active Hall-sensing area of the device would be approximately 850 gauss (0.032″ (0.81 mm) below the package surface).

The flux density would drop to approximately 600 gauss with an air gap between the package and the magnet of 0.031″ (0.79 mm).

Switching-point variations with temperature should be considered in applications covering a wide temperature range.

SWITCHING POINT VARIATION WITH TEMPERATURE

Dwg. No. A-11,004

BASIC 'HEAD-ON' MODE OF OPERATION

DWG. NO. A-9762

Guide to Installation

1. All Hall Effect integrated circuits are susceptible to mechanical stress effects. Caution should be exercised to minimize the application of stress to the leads or the epoxy package.

2. To prevent permanent damage to the Hall cell integrated circuit, heat-sink the leads during hand-soldering. For wave soldering, the part should not experience more than 260°C for more than five seconds. Solder flow should be no closer than 0.125″ (3.18 mm) to the epoxy package.

UGN-3020T AND UGS-3020T
LOW-COST HALL EFFECT DIGITAL SWITCHES

FEATURES

- Operate from 4.5 V to 24 V D-C Power Source
- Operable With a Small Permanent Magnet
- High Reliability—Eliminates Contact Wear, Contact Bounce
- No Moving Parts
- Small Size
- Constant Amplitude Output
- Output Compatible With All Logic Families

T HE TYPE UGN-3020T and UGS-3020T are low-cost magnetically-activated electronic switches utilizing the Hall effect for sensing a magnetic field. Each circuit consists of a voltage regulator, Hall cell, signal amplifier, Schmitt trigger, and current sinking output stage integrated in a single monolithic silicon chip.

The on-board regulator permits stable operation over a wide variation of supply voltages. Operation over an extended temperature range is made possible by the careful matching of components which can be done economically only on a monolithic circuit.

Both devices will typically operate up to a 100 kHz repetition rate.

The circuit output can be interfaced directly with bipolar or MOS logic circuits.

Dwg. NO. A-11,002
FUNCTIONAL BLOCK DIAGRAM
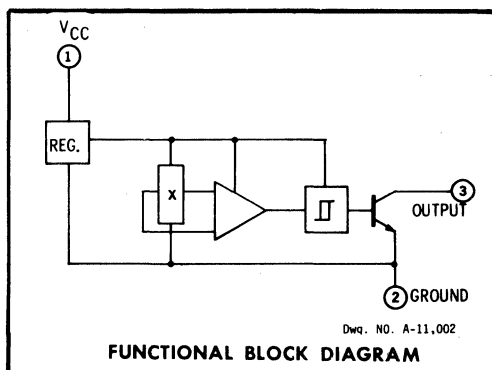
These devices are packaged in the 3-pin single output plastic "T" pack.

These devices were originally introduced with ULN and ULS prefixes.

ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC} . . . . 25 V
Magnetic Flux Density, B . . . . Unlimited
Output OFF Voltage, $V_{OUT(OFF)}$ . . . . 25 V
Output ON Current, I_{SINK} . . . . 25 mA
Operating Temperature Range, T_A
  UGS-3020T . . . . −40°C to +125°C
  UGN-3020T . . . . 0°C to +70°C
Storage Temperature, Range, T_S . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS at V_{CC} = 4.5 V to 24 VDC, T_A = +25°C

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Operate Point	B_{OP}		—	220	350	Gauss
Release Point	B_{RP}		50	165	—	Gauss
Hysteresis	B_H		20	55	—	Gauss
Output Saturation Voltage	V_{SAT}	B≥ 350 Gauss, I_{SINK} = 15 mA	—	85	400	mV
Output Leakage Current	I_{OFF}	B≤ 50 Gauss, V_{OUT} = 24 V	—	0.1	20	μA
Supply Current	I_{CC}	V_{CC} = 4.5 V, Output open	—	5.0	9.0	mA
		V_{CC} = 24 V, Output open	—	6.0	14	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	15	—	ns
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	100	—	ns

9

OPERATION

The output transistor is normally "off" when the magnetic field perpendicular to the surface of the chip is below the threshold or "operate point." When the field exceeds the "operate point," the output transistor switches "on" and is capable of sinking 25 mA of current. Selections to 50 mA are available.

The output transistor switches "off" when the magnetic field is reduced below the "release point" which is less than the "operate point." This is illustrated graphically in the transfer characteristics curve. The hysteresis characteristic provides for unambiguous or non-oscillatory switching.

The magnetic flux density is indicated for the most sensitive area of the device. This area is centrally located and 0.032″ ±0.002″ (0.81 ±0.05 mm) below the branded surface of the T package and 0.012″ ±0.002″ (0.30 ±0.05 mm) below the branded surface of the U package.

For reference purposes, both an Alnico VIII magnet, 0.212″ (5.38 mm) in diameter and 0.187″

(4.75 mm) long and a samarium cobalt magnet, 0.100″ (2.54 mm) square and 0.040″ (1.02 mm) thick, are approximately 1200 gauss at the pole surfaces.

The flux density decays at a high rate as the distance from a pole increases.

As an example, using the Alnico VIII magnet referenced above in good alignment and the pole surface in contact with the branded surface of the package, the flux density at the active Hall sensing area of the device would be approximately 850 gauss.

The flux density would drop to approximately 600 gauss with an air-gap between the package and the magnet of 0.031″ (0.79 mm).

Note: Switching point variations with temperature should be considered in applications covering a wide temperature range.

SWITCHING POINT VARIATION WITH TEMPERATURE

Dwg. No. A-11,011

TRANSFER CHARACTERISTICS SHOWING HYSTERESIS

Dwg. No. A-11,010
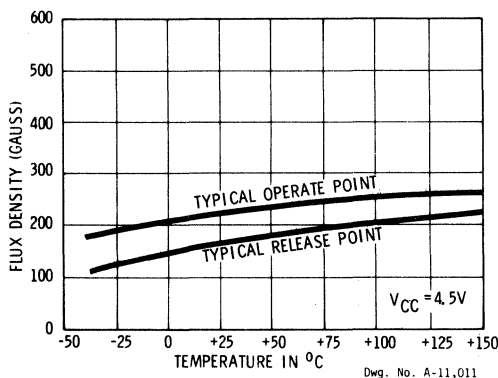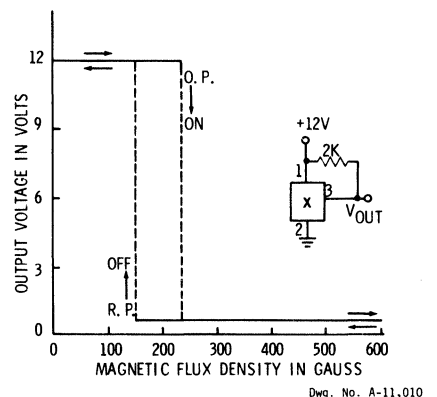
These Hall effect devices are also available in a miniature 3-pin plastic "U" package. The "T" package is 0.080″ (2.03 mm) thick; the "U" package is 0.061″ (1.54 mm) thick. All other dimensions are identical.

UGN-3030T/U AND UGS-3030T/U
BIPOLAR HALL EFFECT DIGITAL SWITCHES

FEATURES

- Operable with Inexpensive Multipole Ring Magnets
- High Reliability — No Moving Parts
- Small Size
- Compatible with All Digital Logic Families

THESE LOW-COST HALL EFFECT switches are designed for use with inexpensive multipole ring magnets. Both devices operate with supply voltages of 4.5 V to 24 V.

Type UGN-3030T/U operates over the temperature range of $-20°C$ to $+85°C$. Type UGS-3030T/U, intended for use in more severe automotive environments, operates over the temperature range of $-55°C$ to $+125°C$.

Circuit output of both Hall Effect ICs can be directly linked to bipolar or MOS logic circuitry. The switches provide a constant amplitude output at switching frequencies of up to 100 kHz.

Dwg. No. A–11,002A

FUNCTIONAL BLOCK DIAGRAM
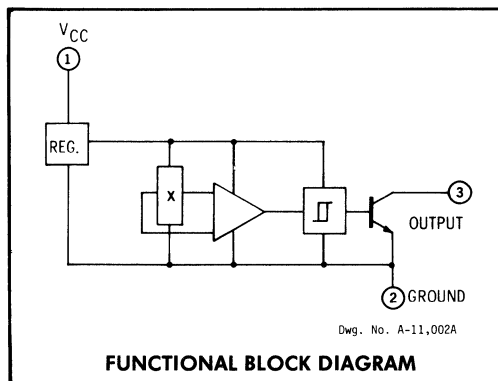
Types UGN-3030T and UGS-3030T are supplied in a three-pin plastic package 80 mils (2.03 mm) thick. Types UGN-3030U and UGS-3030U are furnished in a magnetically optimized 60.5-mil (1.54 mm) plastic 3-pin package.

ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC} .... 25 V
Magnetic Flux Density, B .... Unlimited
Output OFF Voltage, V_{OUT} .... 25 V
Output ON Current, I_{SINK} .... 25 mA
Storage Temperature Range, T_S .... $-65°C$ to $+150°C$
Operating Temperature Range, T_A
   UGS-3030T/U .... $-55°C$ to $+125°C$
   UGN-3030T/U .... $-20°C$ to $+85°C$

ELECTRICAL CHARACTERISTICS at $V_{CC} = 4.5$ V to 24 V, $T_A = +25°C$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Operate Point*	B_{OP}		—	160	250	Gauss
Release Point*	B_{RP}		−250	110	—	Gauss
Hysteresis	B_H		20	50	—	Gauss
Output Saturation Voltage	V_{SAT}	B ≥ 250 Gauss, I_{SINK} = 20 mA	—	100	400	mV
Output Leakage Current	I_{OFF}	B ≤ −250 Gauss, V_{OUT} = 24 V	—	0.1	1.0	μA
Supply Current	I_{CC}	V_{CC} = 4.5 V, Output Open	—	2.5	5.0	mA
		V_{CC} = 24 V, Output Open	—	3.5	7.0	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	100	—	ns
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	500	—	ns

*Magnetic flux density is measured at most sensitive area of device, located 0.032″ ±0.002 (0.81 ±0.05 mm) below the branded face of the "T" package and 0.012″ ±0.002″ (0.305 ±0.05 mm) below the branded face of the "U" package.

9

OPERATION

The output transistor is normally OFF when the magnetic field perpendicular to the surface of the chip is below the threshold or Operate Point. When the field exceeds the Operate Point, the output transistor switches ON and is capable of current-sinking 25 mA.

The output transistor switches OFF when the magnetic field is reduced below the "release point" which is less than the "operate point." This is illustrated graphically in the transfer characteristics curve. The hysteresis characteristic provides for unambiguous or non-oscillatory switching.

The magnetic flux density is indicated for the most sensitive area of the device. This area is centrally located and 0.032″ ±0.002″ (0.81 ±0.05 mm) below the branded surface of the ''T'' package, 0.012″ ±0.002″ (0.305 ±0.05 mm) below the branded surface of the ''U'' package.

The magnetic circuit must provide a +250 gauss to −250 gauss magnetic flux density range at this point for all conditions to ensure reliable operation; + gauss indicates a South pole is toward the branded face of the package; − gauss indicates a North pole is toward the branded package face.

The simplest form of magnet that will operate the Hall Effect bipolar digital switch is a multipole ring magnet as shown. Such magnets are commercially available and inexpensive.

SENSOR-CENTER LOCATION
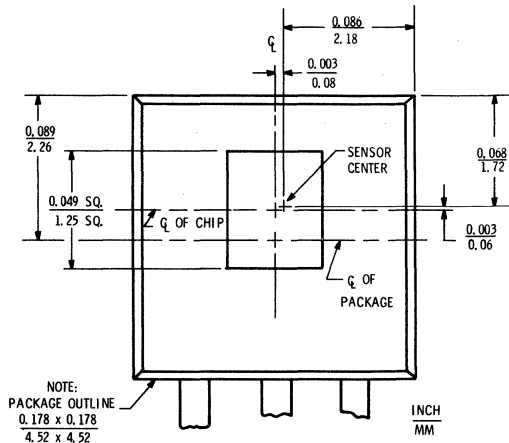
Dwg.No. A-11,912A

SWITCH ACTIVATION WITH MULTIPOLE RING MAGNET
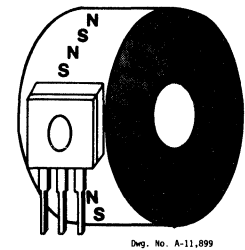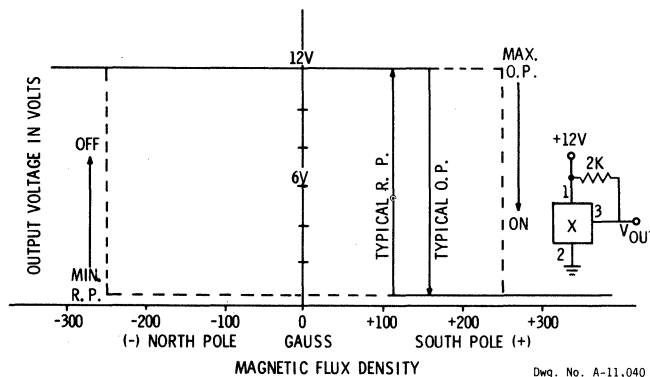
Dwg. No. A-11,899

TRANSFER CHARACTERISTICS SHOWING HYSTERESIS

Dwg. No. A-11,040

GUIDE TO INSTALLATION

1. All Hall Effect integrated circuits are susceptible to mechanical stress effects. Caution should be exercised to minimize the application of stress to the leads or the epoxy package.

2. To prevent permanent damage to the Hall cell integrated circuit, heat-sink the leads during hand-soldering. For wave soldering, the part should not experience more than 260°C for more than five seconds. Solder flow should be no closer than 0.125″ (3.18 mm) to the epoxy package.

UGN-3040T
ULTRA-SENSITIVE HALL EFFECT DIGITAL SWITCH

FEATURES

- Operate from 4.5 V to 24 V D-C Power Source
- Operable With Small Permanent Magnets
- Solid-State Reliability — No Moving Parts
- Small Size
- Constant Amplitude Output
- Output Compatible With All Digital Logic Families

THE SPRAGUE TYPE UGN-3040T is a magnetically-activated electronic switch with extreme sensitivity for use with small, inexpensive magnets, or with relatively large magnet-to-switch distances.

Each circuit consists of a voltage regulator, Hall voltage generator, signal amplifier, Schmitt trigger circuit, and an open collector output driver integrated in a single silicon chip.

The on-board regulator permits operation over a wide range of supply voltages. Circuit output can be interfaced directly with bipolar or MOS logic circuits, and will typically operate up to a 100 kHz repetition rate.

The UGN-3040T is packaged in a miniature 3-pin single-output plastic "T" pack.
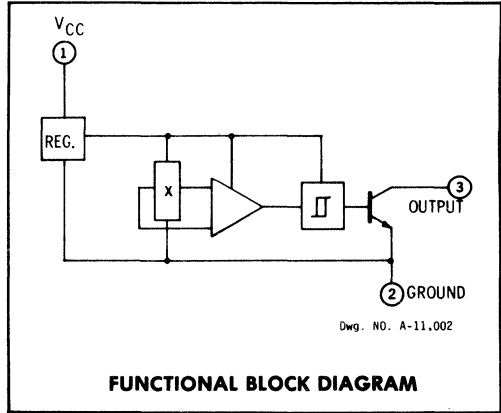
Dwg. NO. A-11,002

FUNCTIONAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC} . . . . 25 V
Magnetic Flux Density, B . . . . Unlimited
Output "OFF" Voltage, $V_{OUT(OFF)}$ . . . . 25 V
Output "ON" Current, I_{SINK} . . . . 25 mA
Storage Temperature Range, T_S . . . . −65°C to +150°C
Operating Temperature Range, T_A . . . . 0°C to +70°C

ELECTRICAL CHARACTERISTICS at V_{cc} = 4.5 V to 24 VDC, T_A = +25°C

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Operate Point	B_{OP}		—	150	200	Gauss
Release Point	B_{RP}		50	100	—	Gauss
Hysteresis	B_H		20	50	—	Gauss
Output Saturation Voltage	V_{SAT}	B ≥ 200 Gauss, I_{SINK} = 20 mA	—	85	400	mV
Output Leakage Current	I_{OFF}	B ≤ 50 Gauss, V_{OUT} = 24 V	—	0.1	20	μA
Supply Current	I_{CC}	V_{cc} = 4.5 V, Output open	—	5.0	9.0	mA
		V_{cc} = 24 V, Output open	—	6.0	14	mA
Output Rise Time	t_r	V_{cc} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	15	—	ns
Output Fall Time	t_f	V_{cc} = 12 V, R_L = 820 Ω, C_L = 20 pF	—	100	—	ns

9

Guide to Installation

1. All Hall Effect integrated circuits are susceptible to mechanical stress effects. Caution should be exercised to minimize the application of stress to the leads or the epoxy package.

2. To prevent permanent damage to the Hall cell integrated circuit, heat-sink the leads during hand-soldering. For wave soldering, the part should not experience more than 260°C for more than five seconds. Solder flow should be no closer than 0.125'' (3.18 mm) to the epoxy package.

**SWITCHING POINT
AS A FUNCTION OF TEMPERATURE**
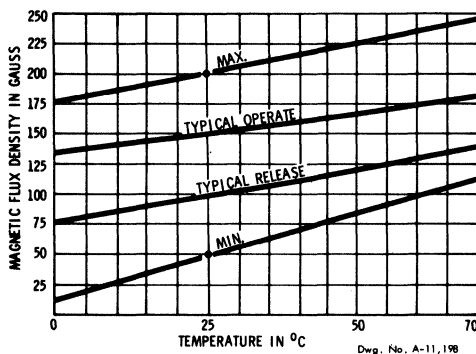
Dwg. No. A-11,198

These Hall effect devices are also available in a miniature 3-pin plastic "U" package. The "T" package is 0.080'' (2.03 mm) thick; the "U" package is 0.061'' (1.54 mm) thick. All other dimensions are identical.

OPERATION

The simplest form of magnet which will operate the Hall Effect digital sensor is a bar magnet as shown. Other methods are possible.

In the illustration, the magnet's axis is on the center line of the packaged device and the magnet is moved toward and away from the device. Also, note the orientation of the magnet's south pole in relation to the branded face of the package.

Dwg. No. A-11,200
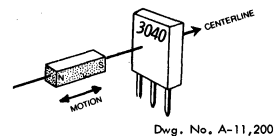
BASIC 'HEAD-ON' MODE OF OPERATION

SENSOR CENTER LOCATION

Dwg.No. A-11,896A

TRANSFER CHARACTERISTICS SHOWING HYSTERESIS

Dwg. No. A-11,199
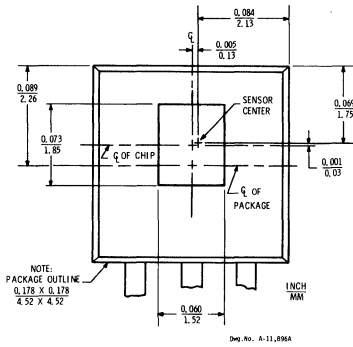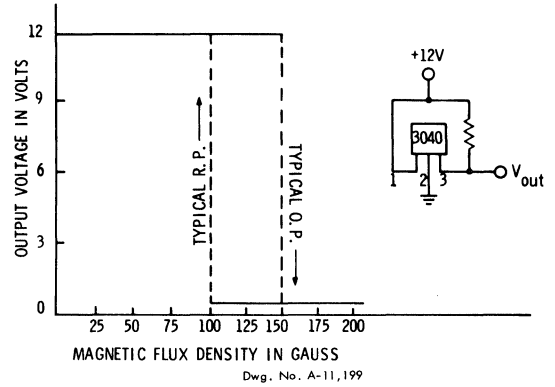
OPERATION (Continued)

The output transistor is normally "off" when the magnetic field perpendicular to the surface of the chip is below the threshold or "operate point." When the field exceeds the "operate point," the output transistor switches "on" and is capable of sinking 25 mA of current. A 50 mA unit is available upon special order.

The output transistor switches "off" when the magnetic field is reduced below the "release point" which is less than the "operate point." This is illustrated graphically in the transfer characteristics curve. The hysteresis characteristic provides for unambiguous or non-oscillatory switching.

The magnetic flux density is indicated for the most sensitive area of the device. This area is centrally located 0.032″ ±0.005″ (0.81 ±0.127mm) below the branded surface of the T package and 0.012 ±0.005″ (0.30 ±0.127 mm) below the branded surface of the U package.

A variety of magnets are commercially available, each exhibiting unique field characteristics. The curves presented below are flux density values for the magnets measured for switch activation in a head-on mode (along the magnet axis). The curves are also pertinent for peak flux density for a given clearance in the slide-by mode of actuation.

FLUX DENSITY AS A FUNCTION OF AIR GAP

(1) .250″ CUBE, RUBBER
(2) .1″ x .1″ x .125″, SAMARIUM COBALT
(3) .212″D x .187″ L, ALNICO 8
(4) .240″ D x .400″ L, CERAMIC
(5) .188″ CUBE, SAMARIUM COBALT
(6) .250″ CUBE, SAMARIUM COBALT

Dwg. No. B-1446

UGN-3075T/U AND UGS-3075T/U
BIPOLAR HALL EFFECT DIGITAL LATCHES

FEATURES

- Operable with Inexpensive Multipole Ring Magnets
- High Reliability — No Moving Parts
- Small Size
- Output Compatible with All Digital Logic Families
- Symmetrical Output
- High Hysteresis Level Minimizes Stray-Field Problems

THESE MAGNETICALLY-ACTIVATED, solid-state latches are designed for use with in-expensive multipole ring magnets and brushless d-c motors. They provide effective, reliable interface between electromechanical equipment and bipolar or MOS logic circuits at switching frequencies of up to 100 kHz.

The bipolar output of these devices saturates when the Hall cell is exposed to a magnetic flux density greater than the ON threshold (100 G typical, 250 G maximum). The output transistor remains in the ON state until magnetic field reversal exposes the Hall cell to a magnetic flux density below the OFF threshold (−100 G typical, −250 G minimum). Because the operating state switches only with magnetic field reversal, and not merely with a change in its strength, these integrated circuits qualify as true Hall Effect latches.

FUNCTIONAL BLOCK DIAGRAM

Dwg. No. A-11,002A
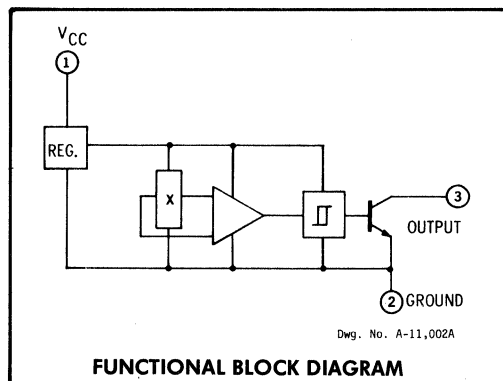
Type UGN-3075T/U is rated for operation over the temperature range of −20°C to +85°C. For applications in more severe environments, Type UGS-3075T/U has an operating temperature range of −55°C to +125°C. Both types work with supply voltages of 4.5 to 24 V.

Both Hall Effect latches are supplied in either the 80-mil (2.03 mm) three-pin plastic "T" package or the magnetically optimized 60.5-mil (1.54 mm) three-pin plastic "U" package.

ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC} .... 25 V
Magnetic Flux Density, B .... Unlimited
Output OFF Voltage .... 25 V
Output ON Current, I_{SINK} .... 50 mA
Operating Temperature Range, T_A
   UGS-3075T/U* .... −55°C to +125°C
   UGN-3075T/U .... −20°C to +85°C
Storage Temperature Range, T_S .... −65°C to +150°C

*Selected devices are available with a maximum T_A rating of +150°C.

Catalog Numbering System
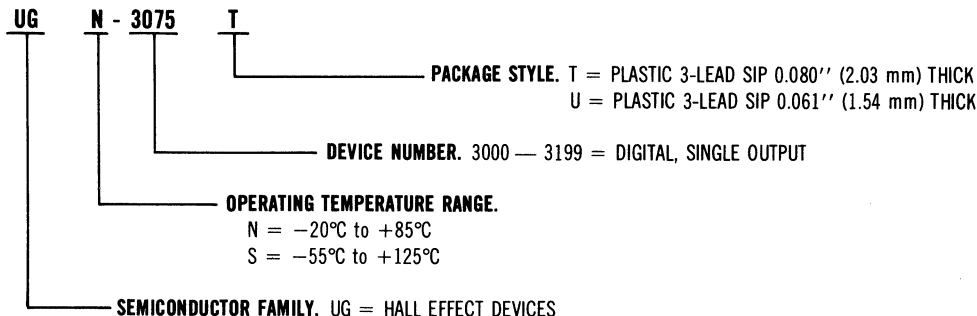
UG N - 3075 T

PACKAGE STYLE. T = PLASTIC 3-LEAD SIP 0.080'' (2.03 mm) THICK
U = PLASTIC 3-LEAD SIP 0.061'' (1.54 mm) THICK

DEVICE NUMBER. 3000 — 3199 = DIGITAL, SINGLE OUTPUT

OPERATING TEMPERATURE RANGE.
N = −20°C to +85°C
S = −55°C to +125°C

SEMICONDUCTOR FAMILY. UG = HALL EFFECT DEVICES

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 4.5 V to 24 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Operate Point*	B_{OP}		50	100	250	Gauss
Release Point*	B_{RP}		−250	−100	−50	Gauss
Hysteresis*	B_H		100	200	—	Gauss
Output Saturation Voltage	V_{SAT}	B ≥ 250 Gauss, I_{SINK} = 20 mA	—	85	400	mV
Output Leakage Current	I_{OFF}	B ≤ −250 Gauss, V_{OUT} = 24 V	—	0.2	1.0	μA
Supply Current	I_{CC}	B ≤ −250 Gauss, V_{CC} = 24 V, Output Open	—	3.0	7.0	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 820Ω, C_L = 20 pF	—	100	—	ns
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 820Ω, C_L = 20 pF	—	200	—	ns

*Magnetic flux density is measured at most sensitive area of device located 0.032'' ±0.002'' (0.81 mm ±0.05 mm) below the branded face of the 'T' package and 0.012'' ±0.002'' (0.31 mm ±0.05 mm) below the branded face of the 'U' package.

SENSOR-CENTER LOCATION

0.084 / 2.13

0.005 / 0.13

0.089 / 2.26

0.073 / 1.85

₵ OF CHIP

SENSOR CENTER

0.069 / 1.75

0.001 / 0.03

₵ OF PACKAGE

NOTE:
PACKAGE OUTLINE
0.178 X 0.178 / 4.52 X 4.52

0.060 / 1.52

INCH / MM

DWG. NO. A-11,896

GUIDE TO INSTALLATION

1. All Hall Effect integrated circuits are susceptible to mechanical stress effects. Caution should be exercised to minimize the application of stress to the leads or the epoxy package.

2. To prevent permanent damage to the Hall cell, heat sink the leads during hand soldering. For wave soldering, the part should not experience more than 260°C for more than five seconds. Solder flow should be no closer than 0.125'' (3.18 mm) to the epoxy package.

9

OPERATION

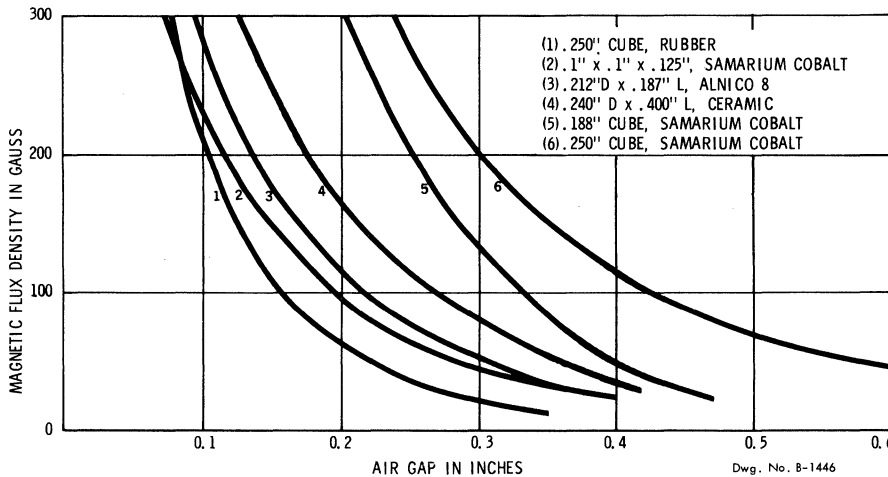The output transistor is normally OFF when the strength of the magnetic field perpendicular to the surface of the chip is below threshold or the Operate Point. When the field strength exceeds the Operate Point, the output transistor switches ON and is capable of current sinking 50 mA of current.

The output transistor switches OFF when magnetic field reversal results in a magnetic flux density below the OFF threshold. This is illustrated in the transfer characteristics graph.

The simplest form of magnet that will operate Types UGN-3075T/U and UGS-3075T/U is a ring magnet, as shown in Figure 1. Other methods of operation are possible.

Dwg. No. A-11,899

Figure 1

Note that the device latches; that is, a south pole of sufficient strength will turn the device ON. Removal of the south pole will leave the device ON. The presence of a north pole of sufficient strength is required to turn the device OFF.

ACTIVE AREA DEPTH (AAD)

The magnetic flux density is indicated in the operating-points graph for the active area of the device, which is located 0.032″ (0.81 mm) below the branded surface of the "T" package and 0.012″ (0.31 mm) below the branded surface of the "U" package. Note that, as shown in the plot of magnetic flux density as a function of total effective air gap, the "U" package offers a significant advantage in marginal flux density conditions for certain magnetic configurations.

TYPICAL TRANSFER CHARACTERISTICS

Dwg. No. A-11,739

PEAK FLUX DENSITY AS A FUNCTION OF TOTAL EFFECTIVE AIR GAP
Plastic 20-Pole Pair Ring (Radial Poles)
1″ (25.4 mm) in diameter
and 0.2″ (5.1 mm) long
with 0.01″ (0.25 mm) clearance

Dwg. No. A-11,738

UGN-3076T/U AND UGS-3076T/U
BIPOLAR HALL EFFECT DIGITAL LATCHES

FEATURES

- Operable with Inexpensive Multipole Ring Magnets
- High Reliability — No Moving Parts
- Small Size
- Output Compatible with All Digital Logic Families
- Symmetrical Output
- High Hysteresis Level Minimizes Stray-Field Problems

THESE SOLID-STATE, magnetically-activated latches, designed for use with brushless d-c motors and inexpensive multipole ring magnets, operate as effective, reliable interface between electromechanical equipment and bipolar or MOS logic circuits at switching frequencies of up to 100 kHz.

The bipolar output of these devices saturates when the Hall cell is exposed to a magnetic flux density greater than the ON threshold (100 G typical, 350 G maximum). The output transistor remains in the ON state until magnetic field reversal exposes the Hall cell to a magnetic flux density below the OFF threshold (-100 G typical, -350 G minimum). Because the operating state switches only with magnetic field reversal, and not merely with a change in its strength, these integrated circuits qualify as true Hall Effect latches.

Dwg. No. A-11,002A

FUNCTIONAL BLOCK DIAGRAM
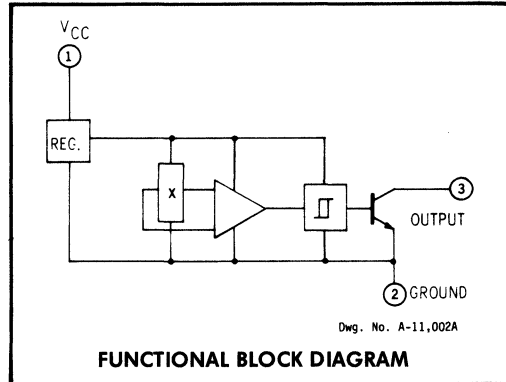
Type UGN-3076T/U is rated for operation over the temperature range of $-20°C$ to $+85°C$. For applications in more severe environments, Type UGS-3076T/U has an operating temperature range of $-55°C$ to $+125°C$. Both types work with supply voltages of 4.5 to 24 V.

Both Hall Effect latches are supplied in either the 80-mil (2.03 mm) three-pin plastic "T" package or the magnetically optimized 60.5-mil (1.54 mm) three-pin plastic "U" package.

ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC} . . . . 25 V
Magnetic Flux Density, B . . . . Unlimited
Output OFF Voltage . . . . 25 V
Output ON Current, I_{SINK} . . . . 50 mA
Operating Temperature Range, T_A
   UGS-3076T/U* . . . . $-55°C$ to $+125°C$
   UGN-3076T/U . . . . $-20°C$ to $+85°C$
Storage Temperature Range, T_S . . . . $-65°C$ to $+150°C$

*Selected devices are available with a maximum T_A rating of $+150°C$.

Additional information on all
Hall Effect devices is available from:

Sprague Electric Company
Hall Effect IC Marketing
70 Pembroke Road
Concord, New Hampshire 03301
(603) 224-1961

9

Catalog Numbering System

UG   N - 3076   T

PACKAGE STYLE. T = PLASTIC 3-LEAD SIP 0.080'' (2.03 mm) THICK
U = PLASTIC 3-LEAD SIP 0.061'' (1.54 mm) THICK

DEVICE NUMBER. 3000 — 3199 = DIGITAL, SINGLE OUTPUT

OPERATING TEMPERATURE RANGE. N = −20°C to +85°C
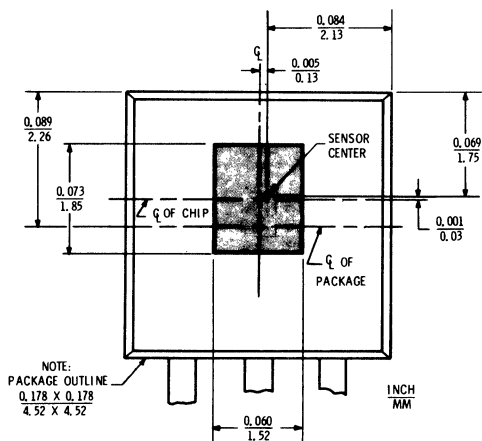S = −55°C to +125°C

SEMICONDUCTOR FAMILY. UG = HALL EFFECT DEVICES
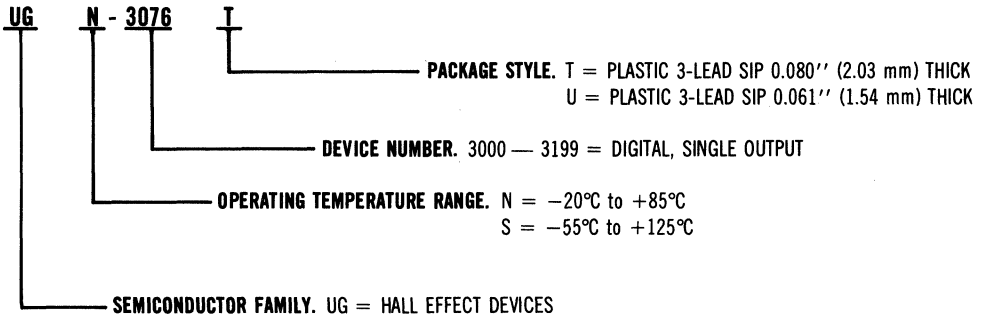
ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = 4.5 V to 24 V (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Operate Point*	B_{OP}		50	100	350	Gauss
Release Point*	B_{RP}		−350	−100	−50	Gauss
Hysteresis*	B_H		100	200	—	Gauss
Output Saturation Voltage	V_{SAT}	B ≥ 350 Gauss, I_{SINK} = 20 mA	—	85	400	mV
Output Leakage Current	I_{OFF}	B ≤ −350 Gauss, V_{OUT} = 24 V	—	0.2	1.0	μA
Supply Current	I_{CC}	V_{CC} = 24 V, Output Open, B ≤ −350 Gauss	—	3.0	7.0	mA
Output Rise Time	t_r	V_{CC} = 12 V, R_L = 820Ω, C_L = 20 pF	—	100	—	ns
Output Fall Time	t_f	V_{CC} = 12 V, R_L = 820Ω, C_L = 20 pF	—	200	—	ns

*Magnetic flux density is measured at most sensitive area of device located 0.032'' ±0.002'' (0.81 mm ±0.05 mm) below the branded face of the 'T'
package and 0.012'' ±0.002'' (0.31 mm ±0.05 mm) below the branded face of the 'U' package.

SENSOR-CENTER LOCATION

0.084 / 2.13
0.005 / 0.13
0.089 / 2.26
0.073 / 1.85
C̸ OF CHIP
SENSOR CENTER
0.069 / 1.75
0.001 / 0.03
C̸ OF PACKAGE

NOTE:
PACKAGE OUTLINE
0.178 X 0.178 / 4.52 X 4.52
0.060 / 1.52
INCH / MM

DWG. NO. A-11,896

GUIDE TO INSTALLATION

1. All Hall Effect integrated circuits are susceptible to mechanical stress effects. Caution should be exercised to minimize the application of stress to the leads or the epoxy package.

2. To prevent permanent damage to the Hall cell, heat sink the leads during hand soldering. For wave soldering, the part should not experience more than 260°C for more than five seconds. Solder flow should be no closer than 0.125'' (3.18 mm) to the epoxy package.

OPERATION

The output transistor is normally OFF when the strength of the magnetic field perpendicular to the surface of the chip is below threshold or the Operate Point. When the field strength exceeds the Operate Point, the output transistor switches ON and is capable of sinking 50 mA of current.

The output transistor switches OFF when magnetic field reversal results in a magnetic flux density below the OFF Threshold. This is illustrated in the transfer characteristics graph.

The simplest form of magnet that will operate Types UGN-3076T/U and UGS-3076T/U is a ring magnet, as shown in Figure 1. Other methods of operation are possible.

Figure 1

Note that the device latches; that is, a south pole of sufficient strength will turn the device ON. Removal of the south pole will leave the device ON. The presence of a north pole of sufficient strength is required to turn the device OFF.

ACTIVE AREA DEPTH (AAD)

The magnetic flux density is indicated in the operating-points graph for the active area of the device, which is located 0.032'' (0.81 mm) below the branded surface of the "T" package and 0.012'' (0.31 mm) below the branded surface of the "U" package. Note that, as shown in the plot of magnetic flux density as a function of total effective air gap, the "U" package offers a significant advantage in marginal flux density conditions for certain magnetic configurations.

TYPICAL TRANSFER CHARACTERISTICS

Dwg. No. A-11,739

**PEAK FLUX DENSITY AS A FUNCTION
OF TOTAL EFFECTIVE AIR GAP**
Plastic 20-Pole Pair Ring (Radial Poles)
1'' (25.4 mm) in diameter
and 0.2'' (5.1 mm) long
with 0.01'' (0.25 mm) clearance

Dwg. No. A-11,741

9

UGN-3201M AND UGN-3203M
DUAL OUTPUT HALL EFFECT DIGITAL SWITCHES

FEATURES

- Operate from 5 V to 16 V D-C Power Supply
- Operate With a Small Permanent Magnet
- High Reliability — No Contact Wear or Bounce
- Small Size — 8-Pin DIP
- Constant Amplitude Output
- Dual Open-Collector Outputs

INTENDED for use in position sensing and contactless switching applications, the Types UGN-3201M and UGN-3203M switches utilize the Hall Effect for detecting a magnetic field.

Both devices feature identical electrical and environmental characteristics. However, the UGN-3201M has a typical Operate Point of 450 gauss and Release Point of 300 gauss; the UGN-3203M is more sensitive, with a typical Operate Point of 235 gauss and Release Point of 100 gauss. The UGN-3203M may be activated by smaller magnets, or at a greater magnet-device spacing.

The UGN-3201M and UGN-3203M Hall Effect digital switches are supplied in 8-pin dual in-line plastic packages. These switches were originally introduced as device numbers ULN-3006M and ULN-3007M, respectively.

Dwg. No. A-11,013

FUNCTIONAL BLOCK DIAGRAM
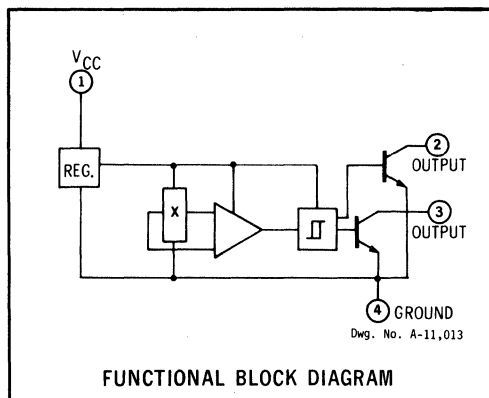
ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC} . . . . 20 V
Magnetic Flux Density, B . . . . Unlimited
Output OFF Voltage, $V_{OUT(OFF)}$ . . . . 20 V
Output ON Current, I_{SINK} . . . . 25 mA
Operating Temperature Range, T_A . . . . 0°C to +70°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS at V_{CC} = 12 VDC, T_A = +25°C

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Operate Point	B_{OP}	UGN-3201M	—	450	750	Gauss
		UGN-3203M	—	235	350	Gauss
Release Point	B_{RP}	UGN-3201M	100	300	—	Gauss
		UGN-3203M	25	100	—	Gauss
Hysteresis	B_H	UGN-3201M	—	150	—	Gauss
		UGN-3203M	—	135	—	Gauss
Output Saturation Voltage	V_{SAT}	B ≥ 350 Gauss, I_{SINK} = 20 mA	—	—	400	mV
Output Leakage Current	I_{OFF}	B ≤ 25 Gauss, V_{OUT} = 12 V	—	—	100	μA
Supply Current	$I_{CC(1)}$	B ≤ 25 Gauss, Outputs open	—	20	25	mA
	$I_{CC(0)}$	B ≥ 350 Gauss, Outputs open	—	20	25	mA

Guide to Installation

1. All Hall Effect integrated circuits are susceptible to mechanical stress effects. Caution should be exercised to minimize the application of stress to the leads or the epoxy package.

2. To prevent permanent damage to the Hall cell integrated circuit, heat-sink the leads during hand-soldering. For wave soldering, the part should not experience more than 260°C for more than five seconds. Solder flow should be no closer than 0.125'' (3.18 mm) to the epoxy package.

'M' PACKAGE

DIMENSIONS IN INCHES
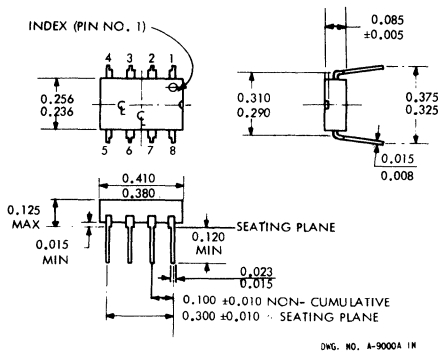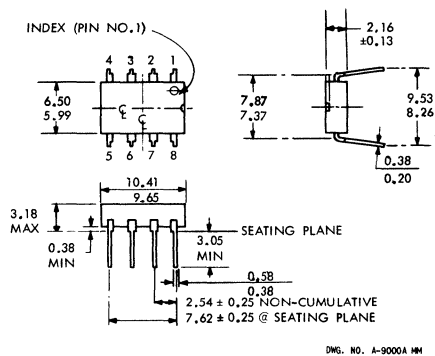
DIMENSIONS IN MILLIMETRES
Based on 1 in. = 25.4 mm

DWG. NO. A-9000A IN

DWG. NO. A-9000A MM

Additional information on all
Hall Effect devices is available from:

Sprague Electric Company
Hall Effect IC Marketing
70 Pembroke Road
Concord, New Hampshire 03301
(603) 224-1961

OPERATION

The output transistors are normally "off" when the magnetic field perpendicular to the surface of the chip is below the threshold or "operate point." When the field exceeds the "operate point," the output transistors switch "on" and will each typically sink 20mA.

The output transistors switch "off" when the magnetic field is reduced below the "release point" which is less than the "operate point." This is illustrated graphically in the transfer characteristic curves. The hysteresis characteristic provides for unambiguous or non-oscillatory switching regardless of the rate of change of the magnetic field.

The magnetic flux density is indicated for the most sensitive area of the device. This area is centrally located and 0.037" ±0.001" (0.94 ±0.05 mm) below the top surface of the package.

For reference purposes, both an Alnico VIII magnet, 0.212" (5.38 mm) in diameter and 0.187" (4.75 mm) long and a samarium cobalt magnet, 0.100" (2.54 mm) square and 0.040" (1.02 mm) thick, are approximately 1200 gauss at its surface.

The flux density decays at a high rate as the distance from a pole increases.

As an example, using the Alnico VIII magnet referenced above in good alignment and the pole surface in contact with the branded surface of the package, the flux density at the active Hall sensing area of the device would be approximately 850 gauss (0.032" below the package surface).

The flux density would drop to approximately 600 gauss with an air-gap between the package and the magnet of 0.031" (0.79 mm).

TYPICAL TRANSFER CHARACTERISTICS SHOWING HYSTERESIS
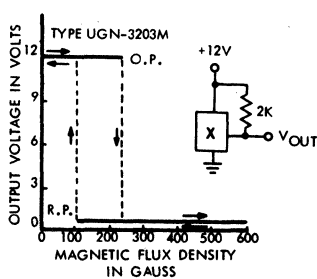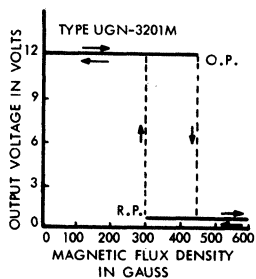
BASIC 'HEAD-ON' MODE OF OPERATION
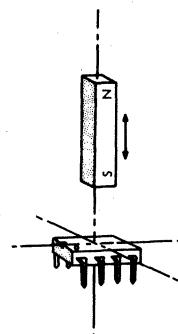
DWG. NO. A-10.307

DWG. NO. A-10.308

# UGN-3220S
LOW-COST DUAL OUTPUT HALL EFFECT DIGITAL SWITCH

FEATURES

- Operate from 4.5 V to 16 V D-C Power Source
- Operable With a Small Permanent Magnet
- High Reliability — Eliminates Contact Wear, Contact Bounce
- No Moving Parts
- Small Size
- Outputs Compatible With All Logic Families
- Operation to 100 kHz
- Dual Output Transistors Can Drive Independent Loads

TYPE UGN-3220S INTEGRATED CIRCUITS are low-cost magnetically-activated electronic switches which utilize the Hall Effect for sensing a magnetic field.

Each circuit consists of a voltage regulator, Hall sensor, signal amplifier, Schmitt trigger, and current sinking output stage, integrated onto a single monolithic silicon chip.

The on-board regulator permits operation over a wide variation of supply voltages. Operation over an extended temperature range is made possible by the careful matching of circuit components — something which can be done economically only on a monolithic circuit.

The circuit output can be interfaced directly with bipolar or MOS logic circuits.

Dwg. No. A-11,007

FUNCTIONAL BLOCK DIAGRAM
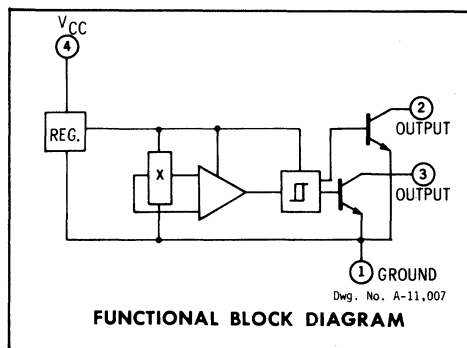
These devices are supplied in a 4-pin single in-line molded package.

ABSOLUTE MAXIMUM RATINGS

Power Supply, V_{CC} . . . . 17 V

Magnetic Flux Density, B . . . . Unlimited

Output OFF Voltage, $V_{OUT(OFF)}$ . . . . 17 V

Output ON Current, I_{SINK} . . . . 25 mA

Operating Temperature Range, T_A . . . . 0°C to +70°C

Storage Temperature Range, T_S . . . . −65°C to +125°C

9

ELECTRICAL CHARACTERISTICS at V_{CC} = 4.5 V to 16 VDC, T_A = +25°C

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Operate Point	B_{OP}		—	220	350	Gauss
Release Point	B_{RP}		50	160	—	Gauss
Hysteresis	B_H		20	60	—	Gauss
Output Saturation Voltage	V_{SAT}	B ≥ 350 Gauss, I_{SINK} = 15 mA	—	110	400	mV
Output Leakage Current	I_{OFF}	B ≤ 50 Gauss, V_{OUT} = 16 V	—	0.1	20	μA
Supply Current	I_{CC}	V_{CC} = 5 V, B ≤ 50 Gauss	—	3.5	9.0	mA

OPERATION

The output transistors are normally "off" when the magnetic field perpendicular to the surface of the chip is below the threshold or "operate point." When the field exceeds the "operate point," each output transistor switches "on" and is capable of sinking 25 mA of current. Selections to 30 mA are available.

The output transistors switch "off" when the magnetic field is reduced below the "release point" (which is less than the "operate point"). This is illustrated graphically in the transfer characteristics curve. The hysteresis characteristic provides for un-ambiguous or non-oscillatory switching.

The magnetic flux density is indicated for the most sensitive area of the device. This area is centrally located and 0.032" ±0.002" (0.81 ±0.05 mm) below the branded surface of the package.

For reference purposes, both an Alnico VIII magnet, 0.212" (5.38 mm) in diameter and 0.187" (4.75 mm) long and a samarium cobalt magnet, 0.100" (2.54 mm) square and 0.040" (1.02 mm) thick, are approximately 1200 gauss at its surface.

The flux density decays at a high rate as the distance from a pole increases.

As an example, using the Alnico VIII magnet referenced above in good alignment and the pole surface in contact with the branded surface of the package, the flux density at the active Hall sensing area of the device would be approximately 850 gauss (0.032" below the package surface).

The flux density would drop to approximately 600 gauss with an air-gap between the package and the magnet of 0.031" (0.79 mm).

TRANSFER CHARACTERISTICS SHOWING HYSTERESIS

Dwg. No. A-11,006

BASIC 'HEAD-ON' MODE OF OPERATION

Dwg. No. A-11,008

Additional information on all
Hall Effect devices is available from:

Sprague Electric Company
Hall Effect IC Marketing
70 Pembroke Road
Concord, New Hampshire 03301
(603) 224-1961

UGN-3501M
SOLID-STATE LINEAR OUTPUT HALL EFFECT SENSOR

FEATURES
- Excellent Sensitivity
- Flat Response to 25 kHz (typ.)
- Internal Voltage Regulation
- Excellent Temperature Stability

UTILIZING THE HALL EFFECT for sensing a magnetic field, Type UGN-3501M ICs provide a linear differential output which is a function of magnetic field intensity.

These devices are intended for applications requiring accurate measurement and/or control of position, weight, thickness, velocity, etc.

The Type UGN-3501M Hall Effect IC includes a monolithic Hall cell, linear differential amplifier, differential emitter follower output, and a voltage regulator. Integrating the Hall cell and the amplifier into one monolithic device minimizes problems related to the handling of millivolt analog signals.

Provisions are included for output offset null. This sensor is supplied as a 8-pin dual in-line plastic package and is rated for continuous operation over the temperature range of 0°C to +70°C and a voltage range of 8 to 16 volts d-c.

FUNCTIONAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . +16 V
Output Current, I_{OUT} . . . . 2 mA
Magnetic Flux Density, B . . . . Unlimited
Operating Temperature Range, T_A . . . . 0°C to +70°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

ELECTRICAL CHARACTERISTICS at V_{CC} = 12 VDC, T_A = +25°C (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Operating Voltage	V_{CC}		8.0	—	16	V
Supply Current	I_{CC}	V_{CC} = 16 V	—	10	18	mA
Output Offset Voltage	V_{OFF}	B = 0 Gauss, R-5-6-7 = 0 Ω, Note 1	—	100	400	mV
Output Common Mode Voltage	V_{CM}	B = 0 Gauss, Note 1	—	3.6	—	V
Sensitivity	ΔV_{OUT}	B = 1000 Gauss, R5-6-7 = 0 Ω, Notes 1,2	700	1400	—	mV
Sensitivity	ΔV_{OUT}	B = 1000 Gauss, R5-6 = 15 Ω, Notes 1, 2	650	1300	—	mV
Frequency Response	BW	R5-6-7 = 0 Ω, f_H − f_L at −3 dB	—	25	—	kHz
Broadband Output Noise	e_n	f = 10 Hz to 10 kHz, R5-6-7 = 0 Ω	—	0.15	—	mV
Output Offset Voltage vs. Temperature	$\Delta V_{OFF}/\Delta T$	R5-6-7 = 0 Ω	—	0.20	—	mV/°C

NOTE 1. All output voltage measurements are made with a voltmeter having an input impedance of 10 kΩ or greater and a common-mode rejection ratio greater than 60 dB.
    2. Magnetic flux density is measured at the most sensitive area of the device, which is on the top center, 0.037 ±0.001" (0.94 ±0.03mm) below the surface.

NORMALIZED SENSITIVITY AS A FUNCTION OF V_{CC}

Normalized Output Voltage vs V_{CC} (Volts)
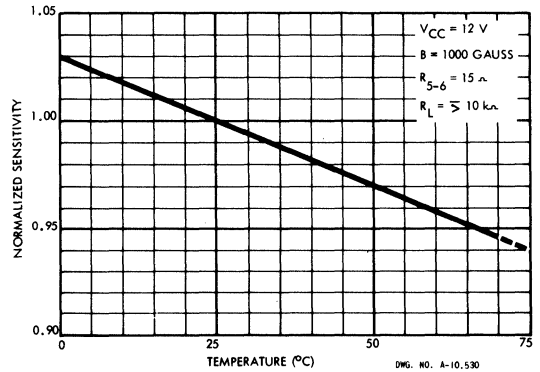
B = 1000 GAUSS
T_A = 25°C
R 5-6-7 = 0
R_L = ≥ 10 kΩ

DWG. NO. A-10,529

NORMALIZED SENSITIVITY AS A FUNCTION OF TEMPERATURE

Normalized Sensitivity vs Temperature (°C)

V_{CC} = 12 V
B = 1000 GAUSS
R_{5-6} = 15 Ω
R_L = ≥ 10 kΩ

DWG. NO. A-10,530

RELATIVE OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE

Relative Differential Output Voltage vs Load Resistance (Ohms)

V_{CC} = 12V
B = 1000 GAUSS
T_A = 25°C
R_{5-6} = 15 Ω

Alternative Output Circuit For Low Impedance Loads

DWG. NO. A-10,533

OUTPUT VOLTAGE AS A FUNCTION OF MAGNETIC FLUX DENSITY

Differential Output Voltage vs Flux Density (Gauss)

V_{CC} = 12V
T_A = 25°C
R_L = 10 kΩ

R_{5-6} = 0 Ω
R_{5-6} = 15 Ω
R_{5-6} = 100 Ω

DWG. NO. A-10,523
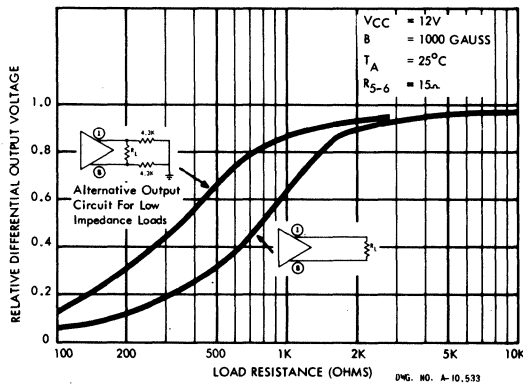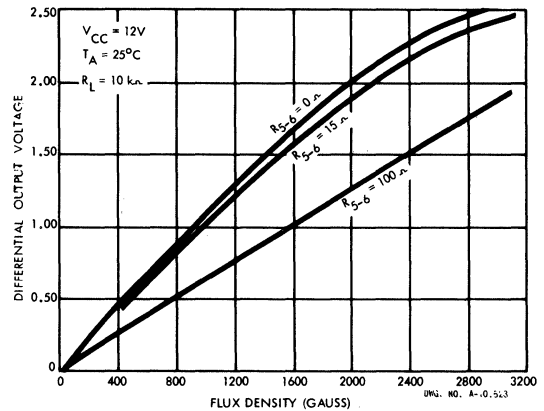
Additional information on all
Hall Effect devices is available from:

Sprague Electric Company
Hall Effect IC Marketing
70 Pembroke Road
Concord, New Hampshire 03301
(603) 224-1961

OUTPUT VOLTAGE AS A FUNCTION OF AIR GAP
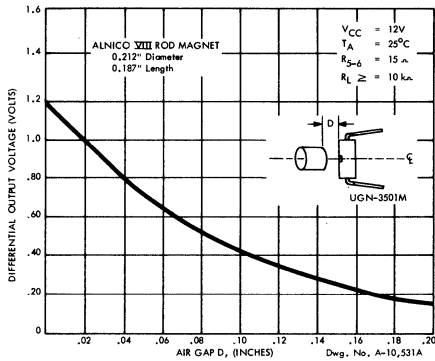
NOISE SPECTRAL DENSITY
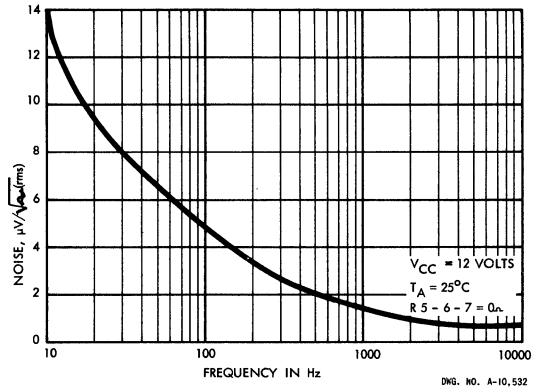
Guide to Installation

1. All Hall Effect integrated circuits are susceptible to mechanical stress effects. Caution should be exercised to minimize the application of stress to the leads or the epoxy package.

2. To prevent permanent damage to the Hall cell integrated circuit, heat-sink the leads during hand-soldering. For wave soldering, the part should not experience more than 260°C for more than five seconds. Solder flow should be no closer than 0.125" (3.18 mm) to the epoxy package.

3. If a zeroing potentiometer is used, minimize lead lengths from it and isolate these leads from output leads if possible. In some cases, it may be more practical to limit the frequency response with an output RC network to prevent oscillation.
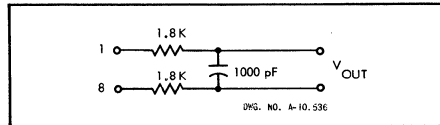
DIMENSIONS IN INCHES
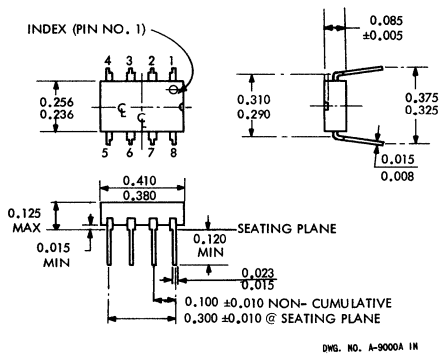
DIMENSIONS IN MILLIMETRES
Based on 1 in. = 25.4 mm
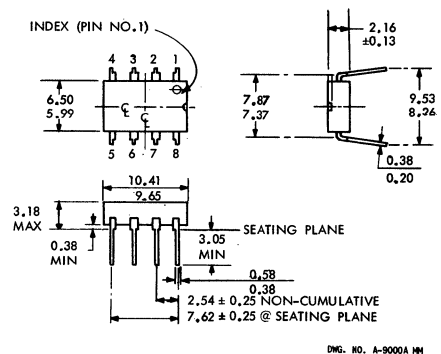
UGN-3501T
SOLID-STATE LINEAR OUTPUT HALL EFFECT SENSOR

FEATURES
- Excellent Sensitivity
- Flat Response to 25 kHz (typ.)
- Internal Voltage Regulation
- Excellent Temperature Stability

UTILIZING THE HALL EFFECT for sensing a magnetic field, Type UGN-3501T integrated circuits provide a linear single-ended output which is a function of magnetic field intensity.

These devices are used principally to sense relatively small changes in a magnetic field — changes which are too small to operate a Hall effect switching device. They are customarily capacitively coupled to an amplifier, which boosts the output to a higher level.

The Type UGN-3501T Hall Effect IC includes a monolithic Hall cell, linear amplifier, emitter follower output, and a voltage regulator. Integrating the Hall cell and the amplifier into one monolithic device minimizes problems related to the handling of millivolt analog signals.

This sensor is supplied a a 3-pin plastic package and is rated for continuous operation over the temperature range of 0°C to +70°C and a voltage range of 8 to 12 volts d-c.
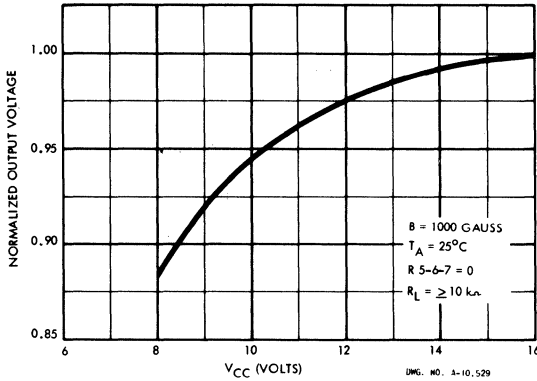

FUNCTIONAL BLOCK DIAGRAM
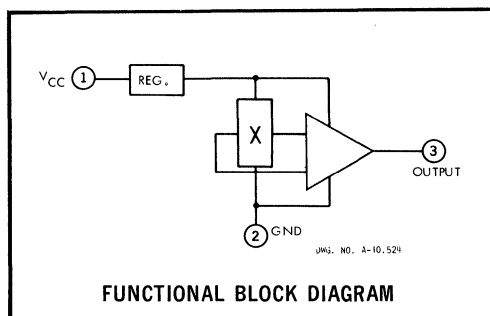
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . +16 V
Output Current, I_{OUT} . . . . 4 mA
Magnetic Flux Density, B . . . . Unlimited
Operating Temperature Range, T_A . . . . 0°C to +70°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

These Hall effect devices are also available in a miniature 3-pin plastic "U" package. The "T" package is 0.080" (2.03 mm) thick; the "U" package is 0.061" (1.54 mm) thick. All other dimensions are identical.

ELECTRICAL CHARACTERISTICS at V_{CC} = 12 VDC, T_A = +25°C

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Operating Voltage	V_{CC}		8.0	—	12	V
Supply Current	I_{CC}	V_{CC} = 12 V	—	10	20	mA
Quiescent Output Voltage	V_{OUT}	B = 0 Gauss, Note 1	2.5	3.6	5.0	V
Sensitivity	ΔV_{OUT}	B = 1000 Gauss, Notes 1, 2	350	700	—	mV
Frequency Response	BW	$f_H - f_L$ at −3 dB	—	25	—	kHz
Broadband Output Noise	e_n	f = 10 Hz to 10 kHz	—	0.1	—	mV
Output Resistance	R_0		—	100	—	Ω

NOTE 1. All output voltage measurements are made with a voltmeter having an input impedance of 10 kΩ or greater.
NOTE 2. Magnetic flux density is measured at the most sensitive area of the device, which is centered on the branded side of the T package, 0.042 ±0.001" (1.07 ±0.03mm) below the surface and 0.022" ±0.001" (0.56 ±0.03mm) below the branded side of the U package.

NORMALIZED SENSITIVITY AS A FUNCTION OF V_{CC}
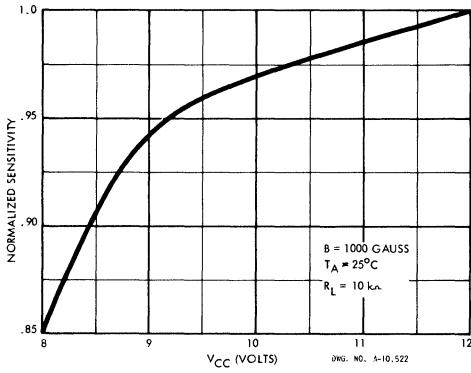
B = 1000 GAUSS
$T_A = 25°C$
$R_L = 10$ kΩ

NORMALIZED SENSITIVITY AS A FUNCTION OF TEMPERATURE

V_{CC} = 12 V
B = 1000 GAUSS
$R_L = 10$ kΩ

OUTPUT VOLTAGE AS A FUNCTION OF MAGNETIC FLUX DENSITY

V_{CC} = 12V
$T_A = 25°C$
$R_L = 10$ kΩ

OUTPUT VOLTAGE AS A FUNCTION OF AIR GAP

ALNICO VIII ROD MAGNET
0.212" Diameter
0.187" Length

V_{CC} = 12V
T_A = 25°C
R_L = 10 kΩ

UGN-3501T

NOISE SPECTRAL DENSITY

V_{CC} = 12 VOLTS
$T_A = 25°C$

9
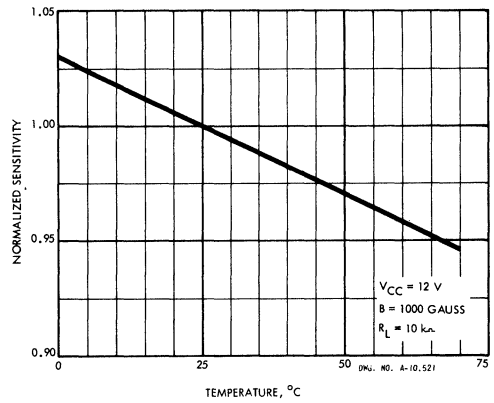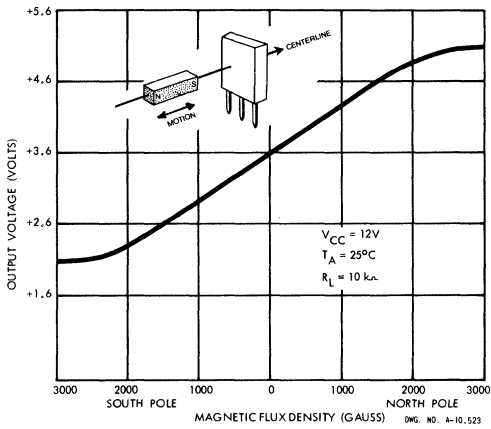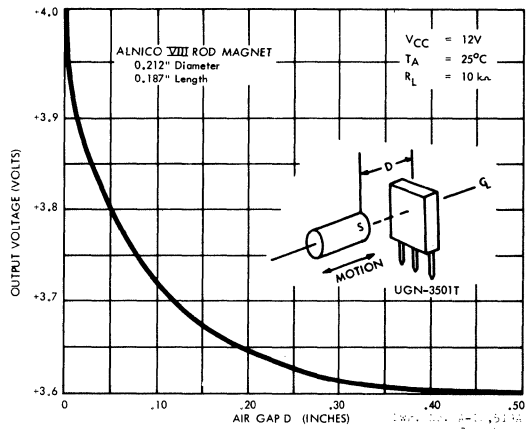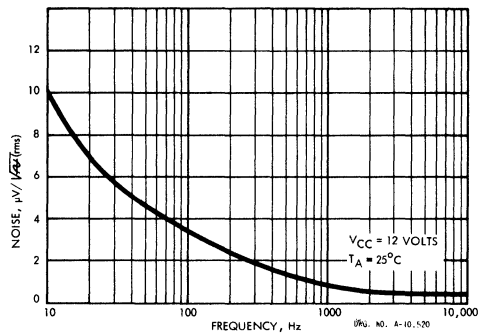
Typical Applications
of Hall Effect Linear Sensors

SENSITIVE PROXIMITY DETECTOR

$\Delta V_0 \simeq 10$ mV
D = 0.250"
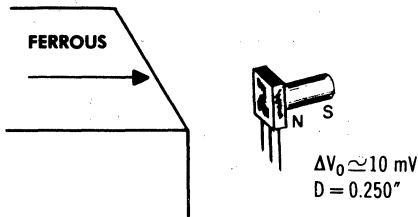
FERROUS METAL SENSOR
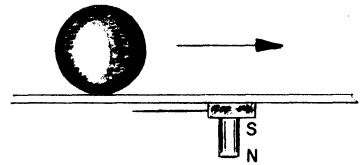
LOBE OR COG SENSOR
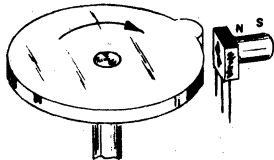
NOTCH OR HOLE SENSOR
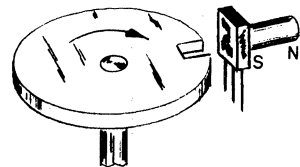
For reference only – an Alnico VIII permanent magnet, 0.212" (5.38 mm) in diameter and 0.187" (4.75 mm) long is approximately 800 gauss at the surface. A samarium cobalt permanent magnet, 0.100" (2.54 mm) square and 0.040" (1.02 mm) thick is approximately 1200 gauss at its surface.

Guide to Installation

1. All Hall Effect integrated circuits are susceptible to mechanical stress effects. Caution should be exercised to minimize the application of stress to the leads or the epoxy package.

2. To prevent permanent damage to the Hall cell integrated circuit, heat-sink the leads during hand-soldering. For wave soldering, the part should not experience more than 260°C for more than five seconds. Solder flow should be no closer than 0.125" (3.18 mm) to the epoxy package.

UGN-3604M AND UGN-3605M
HALL EFFECT SENSORS

THE MOST BASIC Hall Effect magnetic field sensors are the Type UGN-3604M and UGN-3605M. The differential output of the devices is a function of the magnetic flux density present at the sensor. Sensitivity is a function of the control current: sensitivity increases as the control current increases.

The UGN-3604M and UGN-3605M are most often used for magnetic circuit design, analysis, testing and alignment, and for calibrating magnetic sensing devices.

The UGN-3604M is supplied in an 8-pin DIP package, with a calibration chart. The UGN-3605M is the same device without the calibration chart.

Each Type UGN-3604M Hall Effect sensor is individually calibrated at a temperature of $+25°C$ using a supply voltage of 5-volts. The calibration chart supplied indicates differential output values for a magnetic flux density range from 0 gauss to 1000 gauss. Sensitivity at this supply voltage level is typically 40 mV per 1000 gauss.

Since the differential output voltage is a linear function of the magnetic flux density, other readings are easily interpolated.
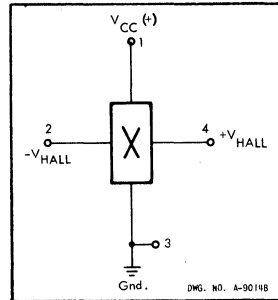
The UGN-3605M is intended to be used primarily as a sensing device. When operated from a constant current source of 3 mA the device provides a typical sensitivity of 60 mV per 1000 gauss. This is the preferred biasing method, to achieve the most stable output voltage vs. temperature.

ABSOLUTE MAXIMUM RATING

Supply Voltage, V_{CC} . . . . 7 V
Supply Current, I_{CC} . . . . 10 mA
Magnetic Flux Density, B . . . . Unlimited
Operating Temperature Range, T_A . . . . 0°C to $+70°C$
Storage Temperature Range, T_S . . . . $-65°C$ to $+150°C$

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
				Limits		
Control Current	I_{CC}	Notes 1, 2	—	3.0	7.0	mA
Control Resistance	R_{1-3}	—	1.0	2.2	4.5	kΩ
Control Resistance vs. Temperature	$\Delta R_{1-3}/\Delta T$	—	—	$+0.8$	—	%/°C
Differential Output Resistance	R_{2-4}	—	2.0	4.4	9.0	kΩ
Output Offset Voltage	V_{OFF}	B = 0 Gauss	—	5.0	—	mV
Output Offset Voltage vs. Temperature	$\Delta V_{OFF}/\Delta T$	B = 0 Gauss	—	30	—	μV/°C
Sensitivity	$\Delta V_{OUT}/\Delta B$	Note 1	—	0.06	—	mV/G
Sensitivity vs. Temperature	$\dfrac{\Delta V_{OUT}/\Delta B}{\Delta T}$	I_{CC} = 1.5 mA	—	$+0.1$	—	%/°C
Product Sensitivity	V/A × kG	Note 1	—	20	—	—

1. I_{CC} is limited to a maximum value which produces a 7 V drop across the control resistance, R_{1-3}.
2. Terminal 1 must always be positive in relation to terminal 3.

9

Guide to Installation

1. All Hall Effect integrated circuits are susceptible to mechanical stress effects. Caution should be exercised to minimize the application of stress to the leads or the epoxy package.

2. To prevent permanent damage to the Hall cell integrated circuit, heat-sink the leads during hand-soldering. For wave soldering, the part should not experience more than 260°C for more than five seconds. Solder flow should be no closer than 0.125'' (3.18 mm) to the epoxy package.

3. The magnetic flux density is indicated for the most sensitive area of the device. This area is centrally located and 0.037'' ±0.001'' (0.94 ±0.03 mm) below the top surface of the package.

4. For reference purposes, an Alnico VIII magnet, 0.212'' (5.38 mm) in diameter and 0.187'' (4.75 mm) long or a samarium cobalt magnet, 0.100'' (2.54 mm) square and 0.040'' (1.02 mm) thick, is approximately 1200 gauss at its surface.

Note that the flux density decays at a high rate as the distance from a pole increases. In most cases, this is a relatively linear decrease in the region of interest, and it may range from 5 to 20 gauss/mil.

DIMENSIONS IN INCHES
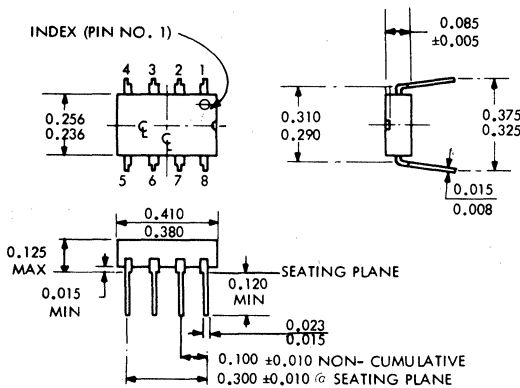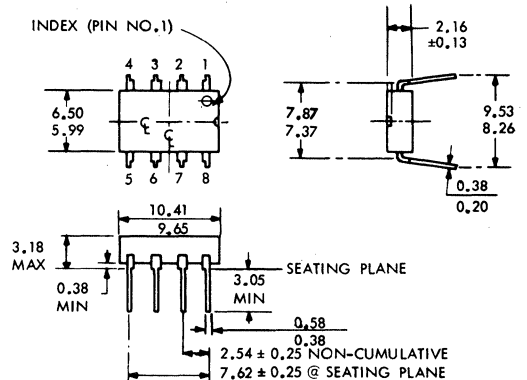
DWG. NO. A-9000A IN

DIMENSIONS IN MILLIMETRES
Based on 1 in. = 25.4 mm

DWG. NO. A-9000A MM

Additional information on all
Hall Effect devices is available from:

Sprague Electric Company
Hall Effect IC Marketing
70 Pembroke Road
Concord, New Hampshire 03301
(603) 224-1961

Hall Effect IC Application Guide

SPRAGUE ELECTRIC uses the latest linear integrated circuit technology in combination with the 100[+] year old Hall Effect to produce Hall Effect ICs. These are magnetically activated switches and sensors with the potential to simplify and improve systems designed for switch and sensor applications.

Simplified Switching At Low Cost

Simplified switching is a Hall switch feature. Sprague Hall Effect ICs combine Hall voltage generators, signal amplifiers, Schmitt trigger circuits and transistor output circuits on an IC chip. Output is clean, fast, and switched with no bounce, an inherent problem in mechanical contact switches. A Sprague Hall Effect IC switch costs less than many common electromechanical switches.

Efficient, Effective Low-Cost Sensors

A Hall Effect sensor detects the motion, position, or change in field strength of an electromagnet, a permanent magnet, or a ferromagnetic material with an applied magnetic bias. Output is linear and temperature stable. Energy consumption is significantly low. Response is independent of the velocity of the field being sensed.

A Sprague Hall Effect IC sensor can be more efficient and effective than inductive or optoelectronic sensors and at lower cost.

Sensitive Circuits For Rugged Service

The Hall Effect IC is virtually immune to environmental contaminants, is particularly rugged, and is suitable for use under severe service conditions. These circuits are very sensitive, providing reliable, repetitive operations in close tolerance applications. The Hall Effect IC can "see" precisely through dirt and darkness.

Sprague Hall Effect IC switches and sensing systems cost less than most optoelectronic switch and sensor circuits.

HALL EFFECT SWITCH OUTPUT WAVEFORM
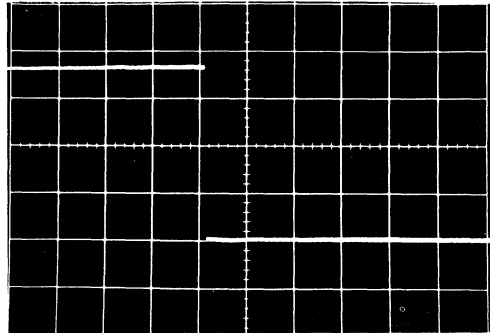
REED RELAY OUTPUT WAVEFORM
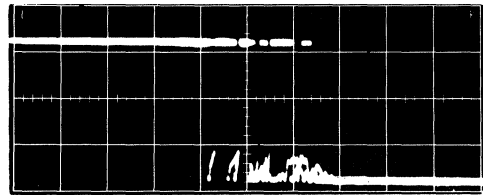
HALL EFFECT SENSOR LINEAR OUTPUT

$V_{CC} = 12V$
$T_A = 25°C$
$R_L = 10 k\Omega$

NOTE: NORTH POLE IS WITH THE NORTH POLE FACING THE BRANDED SIDE OF THE PACKAGE.

OUTPUT VOLTAGE (VOLTS)

SOUTH POLE   NORTH POLE

MAGNETIC FLUX DENSITY (GAUSS)   DWG. NO. A-10,523

9
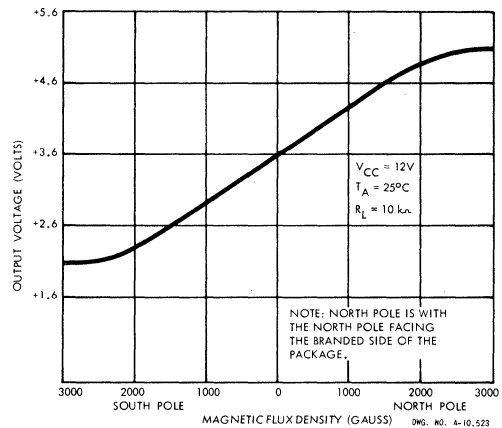
HISTORY AND THE HALL EFFECT

E. H. Hall, at Johns Hopkins University in 1879, first noted the effect that bears his name. A magnetic field applied to a conductor carrying current produces a voltage across the conductor as shown in Figure 6.

The effect is caused by electron deflection within the solid, concentrating the negative charges to one side or the other depending on the influence of the magnetic lines of force. The difference in potential is called the Hall voltage.

The ratio Vt/IH is the Hall Coefficient. (V is the Hall voltage, t the material thickness, I the primary current flow, and H the magnetic field.) This ratio is a constant for a given material.

H. A. Lorentz and Paul Drude developed theories of conduction which apparently accounted for the Hall Effect early in this century. Subsequently the Hall Effect was widely used to study conductivity of materials, with a Hall Coefficient assigned as a means of classification.

Attempts to classify some specific materials such as lead sulphide and silicon produced baffling, contradictory data. The introduction of quantum mechanics in 1926 provided a means for clarification of these problems and other difficulties associated with semiconductor materials.

A proper understanding of semiconductor theory, impurity conduction, junction theory and the fundamental approaches to semiconductor device design did evolve out of studies using the Hall Effect.

The Hall voltage is proportional to the cross-product $I \times H$ (Current x Field). A device that exhibits the Hall Effect is a multiplier: if current flow is constant, the Hall voltage will be proportional to the magnetic field applied; if the magnetic field is constant, the Hall voltage will be proportional to the current flow.

Early Hall Effect devices found limited application as wattmeters or gaussmeters. Such devices were complex, expensive, and susceptible to noise and temperature variations. It was difficult to achieve useful Hall voltage levels.

Production of Hall Effect integrated circuits have eliminated the problems associated with discrete component circuit designs. The Hall Effect ICs are simple, inexpensive, virtually immune to noise, and are temperature stable. Amplifier circuits integral to the devices produce useful electrical output levels.

DWG. NO. A-10.9C7
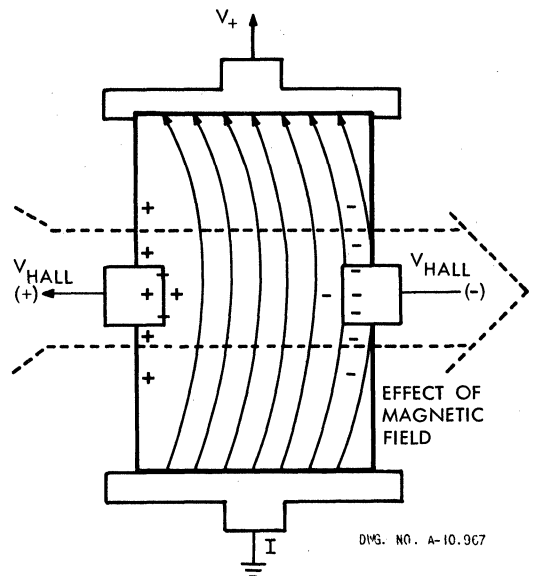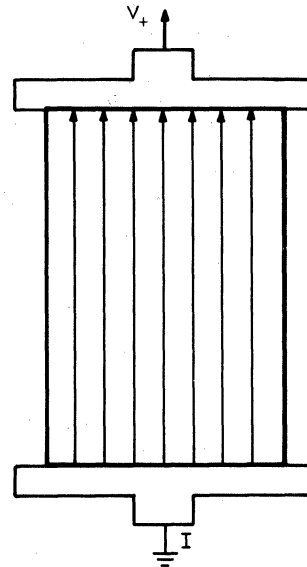
A MAGNETIC FIELD IS APPLIED TO THE CONDUCTOR CARRYING CURRENT. THE NEGATIVE CHARGES ARE DEFLECTED BY THE MAGNETIC FIELD PRODUCING A DIFFERENCE IN POTENTIAL CALLED THE HALL VOLTAGE (V_{HALL}). THIS PRINCIPLE IS APPLIED IN HALL EFFECT IC'S TO PRODUCE MAGNETICALLY ACTIVATED SWITCHES AND SENSORS.

SOME CURRENT HALL EFFECT IC APPLICATIONS —

Ignition Systems
Speed Controls
Speedometer Pickups
Security Systems
Alignment Controls

Mechanical Limit Switches
  (computers)
  (printers)
  (floppy discs)
  (sewing machines)
  (record players)
  (machine tools)

Current Sensors
Current Limit Switches
Linear Potentiometers
Position Detectors
Keyboard/Keyswitch
Selector Switches
Pushbutton Switches
Micrometers

HALL EFFECT SWITCH and SENSOR APPLICATIONS AREAS —

Appliances
Automotive OEM
Automotive Aftermarket
Business Machines
Communications
Computers/Peripherals
Controls
Entertainment Products
Industrial and Commercial Switches
Instrumentation
Keyboard/Keyswitch
Machinery
Machine Tools
Military Systems and Equipment
Power Supplies
Test Equipment

TYPICAL APPLICATIONS

| VANE INTERRUPTER (ignition switch, etc.) | LIMIT SWITCH (pressure monitor, etc.) | ANGLE SENSING (tilt switch, etc.) | CHANGE IN FLUX PATH (notch sensor, etc.) | FERROUS METAL SENSOR (pinball detector, etc.) | ANGLE OF ROTATION (antenna position, etc.) |
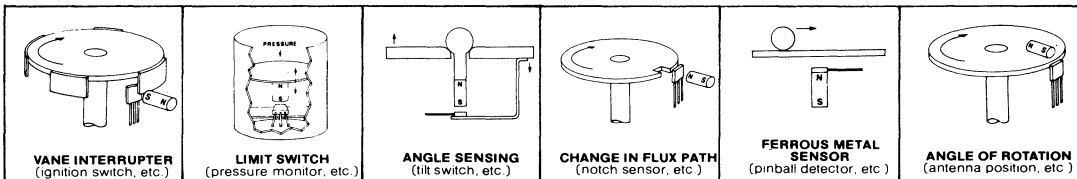
What Does A Hall Effect Switch Do?

Switch designers have obtained high performance switching characteristics with the use of photoelectric switching, capacitive circuits, mercury wetting switches, proximity devices and magnetic pickup techniques. Such designs have unique characteristics suitable for one or more specific applications. In general these designs are usually more complex and more expensive than Hall Effect IC switches performing similar functions.

Snap-action or reed switches have been used wherever the switch life, speed and reliability permitted, primarily because of their low cost. Some applications require performance standards not available in electro-mechanical switches.

Sprague Electric Hall Effect IC switches provide high-performance switching characteristics at costs comparable with snap-action or reed switches.

The devices are very small. The 3-lead "T" pack units are 0.18" x 0.18" x 0.08". The cost is as low as the devices are small.

9

Whatever Turns Them On . . .

The application of Hall Effect switches is not very different from other switching methods. A means for mounting and making electrical connections must be provided. Supply voltage, load, environment and ambient temperature range must fall within limits specified in the applicable engineering bulletin.

Hall Effect switches incorporate a voltage regulator, a Hall voltage generator, a signal amplifier, trigger circuits and output drivers on a single silicon chip.

The magnetic characteristics of the Hall Effect switch are specified in terms of magnetic flux density (in gauss). Typical, maximum, and minimum operate and release points and hysteresis factors are specified.

A built-in hysteresis feature insures that stray magnetic fields from transformers, solenoids, or other associated circuitry will not cause unwanted switch operation. The graph below shows typical hysteresis characteristics for the UGN-3019T switch.

FUNCTIONAL BLOCK DIAGRAM

Dwg. No. A-11,007

**TRANSFER CHARACTERISTICS
SHOWING HYSTERESIS**

Dwg. No. A-9015C

Switching is dependent on the proximity of an external magnet whose field passes perpendicularly through the Hall voltage generator on the chip face. The Hall generator produces an analog voltage amplified and converted by the trigger circuit to a digital output.

Hall Effect IC switches feature such characteristics as high-speed response and very high cycle rates. Typical rise time (turn-on) is 15 nanoseconds, fall time (turn-off) 100 nanoseconds. These units have the capability for cycling at 100,000 Hz (cycles-per-second).

Hall Effect IC switches feature constant amplitude output without the bounce characteristics of electromechanical switches. Hall Effect ICs also feature low power consumption: 7 mA is typical.

The maximum operate point for the UGN-3019T switch is specified at 500 gauss and the minimum release point at 100 gauss. The maximum hysteresis factor for this switch, however, is 275 gauss. Should the operate point fall near the maximum, the release point will move up as well. Similarly, if the release point falls near the minimum, the operate point will have a correspondingly lower value. The hysteresis factor will remain close to a typical value.

Basic fixed element switch designs will take the maximum and minimum operate and release points into account. However, a configuration which permits adjustment of switch and magnet elements in assembly or operation can take advantage of the closer tolerance hysteresis limits to achieve even more precise switching characteristics.

Head-On Mode of Operation

The simplest form of magnet which will operate the Hall Effect switch is a rod or bar. The curves below illustrate typical flux density (in gauss) as a function of air gap distance for two rod magnets.

In each case, the magnet is oriented with its axis perpendicular to, and on the center line of, a Hall Effect IC switch. Flux density and air gap distance are measured along the magnet axis and switch centerline.
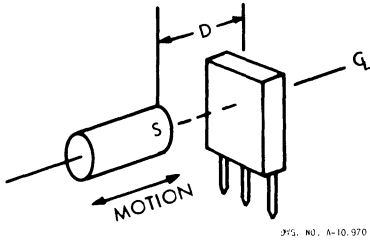
DWG. NO. A-10.970

The magnet is moved toward the switch to activate it and away to release it. This method of operation is commonly referred to as the head-on mode.

The switch used is the Sprague UGN-3019T. The typical operate and typical release points are 420 and 300 gauss, respectively.

An ALNICO V rod magnet 0.25'' in diameter by 1.25'' in length must be 0.18'' or less from the switch to insure operation at the 420 gauss typical operate point. The magnet must be moved to a distance 0.25'' from the switch to insure release, an "operate-release" distance of $1/16''$.

The UGN-3019T can be switched with a larger or stronger magnet over greater distances. Or, the device can be switched with a smaller or weaker magnet provided the air gap between the magnet and the switch is properly decreased.

An ALNICO VIII rod magnet 0.212'' in diameter by 0.187'' in length must be 0.05'' or less from the switch to insure operation at the 420 gauss typical operate point. The magnet must be moved to a distance 0.085'' from the switch to insure release at the 300 gauss typical release point.

Use of the smaller ALNICO VIII rod magnet reduced the on-to-off motion from approx. $1/16''$ to $1/32''$.

MAGNETIC FLUX DENSITY AS A FUNCTION OF AIR GAP
Head-On Mode of Operation

DWG. NO. A-10.968

DWG. NO. A-10.969

9
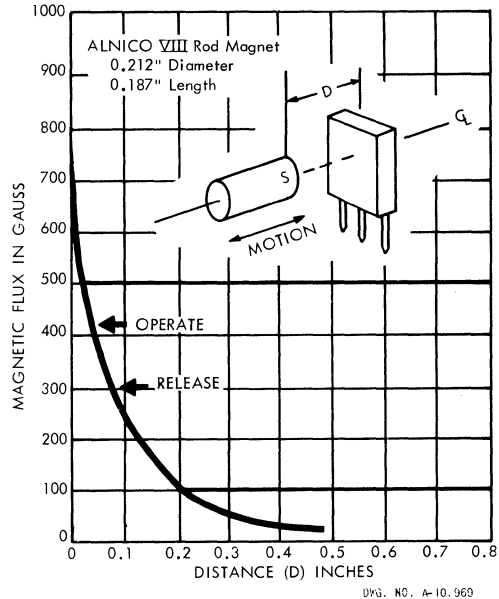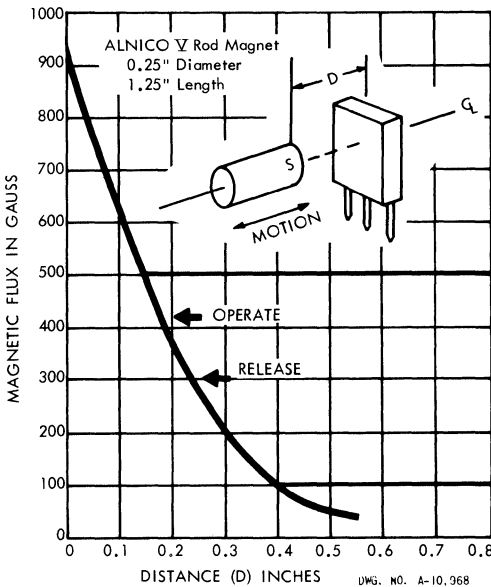
Slide-By Mode of Operation

Hall Effect switches are often activated by means of a slide-by movement of the magnet past the switch as illustrated below.

The axis of the magnet remains perpendicular to the face of the switch, the air gap remains constant, and the magnet passes close enough to the switch to activate it. The maximum flux density is obtained when the magnet axis is on the switch centerline.

The graph at bottom left shows slide-by characteristics for the same magnet used in the previous head-on mode example. The air gap is 0.01″. Flux density at the switch is a function of the distance between the magnet axis and the switch centerline.

Movement from the operate point to the release point covers only 0.018″. Movement continuing past the switch covers an "operate-release" distance of 0.24″, but no change in direction is required.
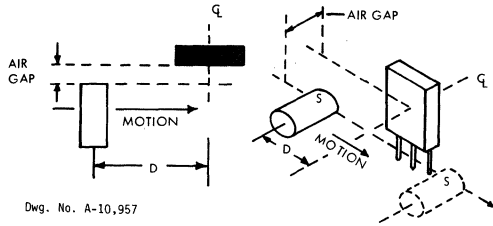
Slide-By With Actuator

Magnetic fields may be distorted, interrupted, squeezed, squashed, or focused by various ferromagnetic concentrators, shunts, vanes, flux returns, and actuators. The magnetic circuit improves the efficiency of the magnet by concentrating the magnetic field.

The extent of field distortion can be seen in a comparison of flux density at the switch for a magnet with and without the actuator. Flux density is plotted in a slide-by mode, with a 0.05″ air gap for an ALNICO VIII rod magnet 0.188″ in diameter by 0.938″ in length.

Without the actuator, the flux density across the 0.05″ air gap is not sufficient to activate a UGN-3019T, as illustrated in the graph at bottom right. With the actuator, the 420 gauss operate point is obtained with the magnet axis 0.15″ from the switch centerline.

Dwg. No. A-10,957

DWG. NO. 11,117-A
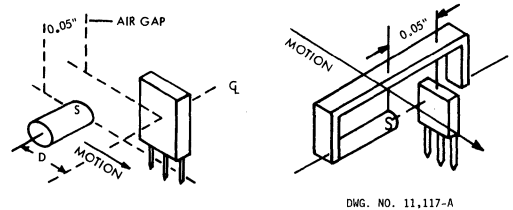
MAGNETIC FLUX DENSITY AS A FUNCTION OF MAGNET AXIS-TO-CENTERLINE DISTANCE
Slide-By Mode of Operation

ALNICO VIII Rod Magnet
0.212″ Diameter
0.187″ Length
Air Gap = 0.01″

DISTANCE (D) OF MAGNET FROM CENTERLINE (₵) INCHES

Dwg. No. A-10,956

ALNICO VIII MAGNET
0.188 Diameter
0.938 Length
Air Gap = 0.05″

SLIDE-BY MODE
WITH ACTUATOR ━━━━
WITHOUT ACTUATOR ━ ━ ━

DISTANCE (D) OF MAGNET FROM CENTERLINE (₵) INCHES

Dwg. No. A-9011C
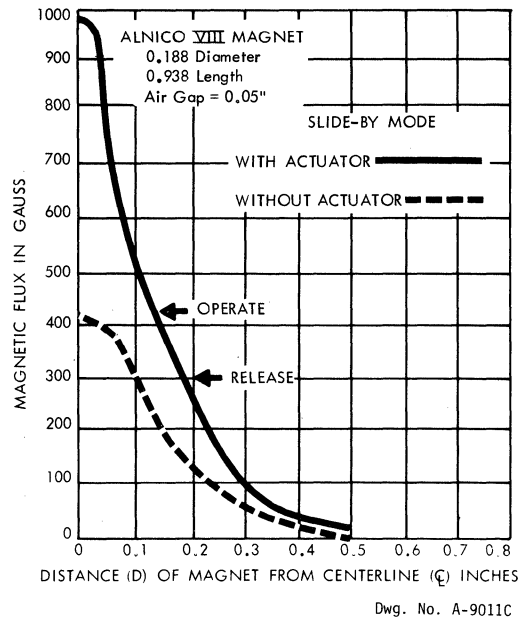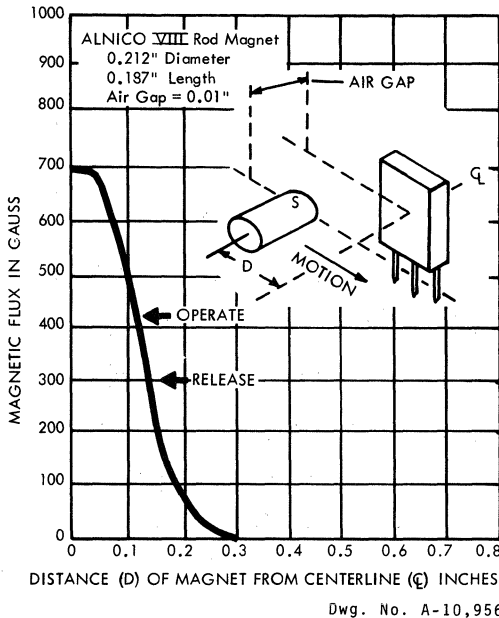
Vane Activation

A ferromagnetic plate or vane moved between the magnet and switch will shunt the field, shielding the switch from the magnet. A movable vane, as shown below, is a most practical device for switching a Hall Effect IC.

Vane activation is often accomplished in a fixed assembly incorporating a magnetic conductor to concentrate and focus the magnetic field through the switch. A ferrous vane is used to shunt the flux, turning the switch off. The magnet, switch and magnetic conductor may be molded in place, eliminating alignment problems, and often producing an extremely rugged completed switch.

A fixed assembly designed for vane activation lends itself to a wide variety of possible switch configurations.

Note the curve at bottom left is an approximation. Several factors influence the switching characteristics of a vane activated Hall Effect switch. The relative position of the vane leading and trailing edges and the strength of the magnet used are of primary importance.

The flux density, vane dimensions, and material all affect the slope of the flux density curve. *A steeper curve will minimize the effect of switching point tolerance and temperature and voltage variation.* A stronger magnet reduces the vane travel required to switch the Hall Effect switch.
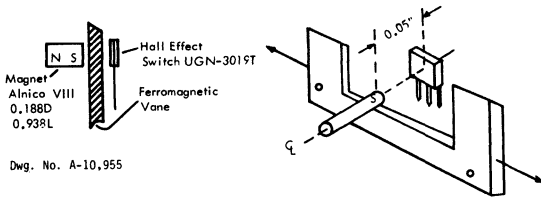
Switch designers have utilized strong magnets with efficient magnetic circuit design in a fixed element molded assembly to provide a very high flux density and a steep curve. This approach minimizes operate-release point variations with changes in temperature.

A different design approach has used an adjustable air gap, permitting use of a smaller magnet in the magnetic circuit design. This design approach produces a shallow flux density curve, and places severe operate-release point restrictions on the Hall switch required. Vane material is typically greater than $1/32''$ thick to result in a minimum flux density. This leaves little clearance.

Generally, the physical position of the vane leading and trailing edges, (which determine switch points), the switch characteristics, and the magnet specifications should all be considered as part of an overall switch design. Independent selection of any element can severely restrict the possibilities for designing an effective switch.

The graph at bottom right is a generalization of the principle involved in reducing switching distances and tolerances for vane activated switches. A stronger magnet produces a higher initial flux density and a steeper curve. Note that a steep slope minimizes the effect of temperature changes on the operate point.

Dwg. No. A-10,955

FLUX DENSITY AS A FUNCTION OF VANE POSITION
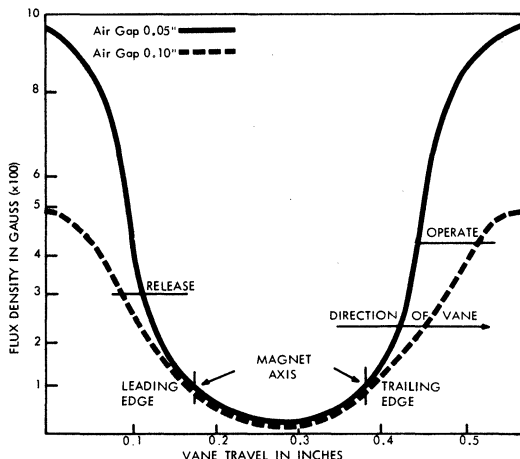
(D) is measured from the point where the vane first effects the flux density at the switch.

9
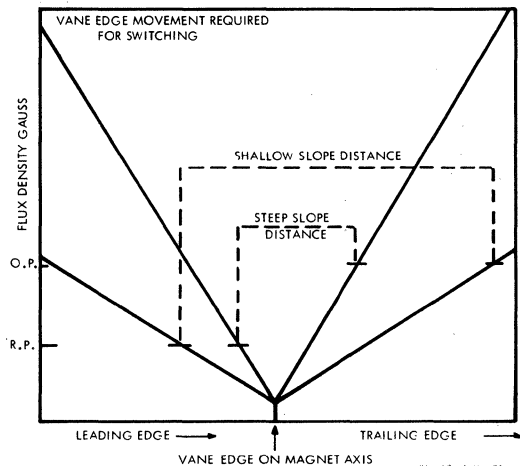
Ring Magnets and Bipolar Switches

Multiple-pole ring magnets and Hall Effect bi-polar switches are used to monitor or measure rotary motion and are especially useful in high-speed applications: speedometer pickups, rpm indicators, angle indicators, etc.

Rugged inexpensive ceramic or plastic ring magnets incorporate up to 20 magnetic pole pairs per inch of ring diameter. The useful field strength available in this type of magnet construction is approximately 250 gauss to 1000 gauss.

Sprague UGN-3030T and UGS-3030T bipolar digital switches operate in the magnetic field range of 250 gauss (South) to -250 gauss (North) and are intended specifically for operation with multiple-pole ring magnets.

Note below that exposure to a single pair of opposite magnetic poles accomplishes a single switching cycle.

The curves shown are approximations. Actual magnetic field exposure at the switch depends on the field strength available and the magnet-to-switch spacing.

Ring magnets are available with radially-oriented poles or with axially-oriented poles.

The output voltage wave form will be determined by the specific distribution of the operate and release points within the switching range. As with other Hall Effect switches, both points move together within the switching range so that the hysteresis factor remains close to the typical value in all cases, as illustrated in the graph at bottom.

A SINGLE SWITCHING CYCLE FOR A MULTIPLE POLE RING MAGNET USING A UGN-3030T SWITCH

DWG. NO. A-11042

RADIAL OR AXIAL ORIENTED POLES FOR SWITCH ACTUATION WITH A RING MAGNET

DWG. NO. A-11,041

TRANSFER CHARACTERISTICS SHOWING HYSTERESIS

Dwg. No. A-11,040
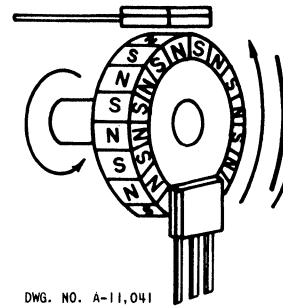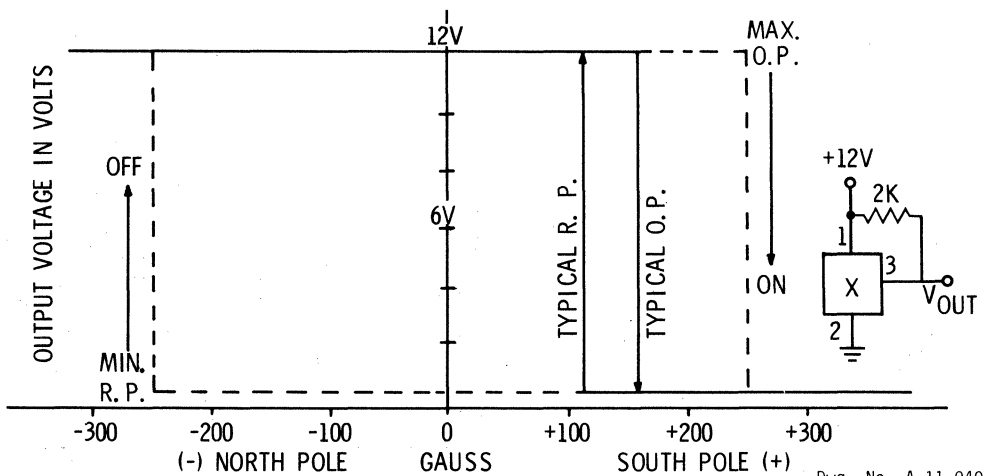
MODEL OF A MAGNET

An inexpensive commercially available standard ALNICO VIII magnet* is shown in the scale drawing. The solid lines are maximum operate and minimum release points for a Sprague UGN-3019T switch. The field strength levels indicated by dotted lines are maximum operate and minimum release points for other Sprague Hall Effect IC switches.

The field is unique to this magnet, and is a function of the material used and the geometry and dimensions of the magnet. Increasing the diameter would tend to spread the field. Extending the length of the magnet would strengthen the field.

A variety of magnet materials are commercially available, each exhibiting unique field characteristics. A samarium-cobalt magnet only 0.085″ square by 0.04″ long will produce up to 1200 gauss at its pole surface, more than adequate field strength to operate all Sprague Hall Effect IC switches. The strongest known field available in a permanent magnet is that generated by an ALNICO V magnet capped with a samarium-cobalt rare earth magnet.

The curves below left are flux density values for the magnet measured for switch activation in a head-on mode (along the magnet axis), and for slide-by modes with air gaps of 0.01″ and 0.025″.

FLUX DENSITY CURVES

Dwg. No. A-11,065

*Indiana General Magnet Products Co. SR8522.

MAGNETIC FIELD MODEL OF AN ALNICO VIII SINTERED ROD MAGNET

Dwg. No. A-11,064

The slide-by curves cross each other, reflecting the fact that the field strength contours are not concentric circles.

The magnetic flux density is indicated for the most sensitive area of the device. This area is centrally located and 0.032″ ±0.002″ below the branded surface of the T package and 0.012″ ±0.002″ below the branded face of the U package.

Note that Sprague Hall Effect ICs are designed to be activated by the field generated by a magnetic South pole, applied to the face or branded side of the switch package. The Hall Effect switches will operate with a magnetic North pole of sufficient strength applied to the back of the switch.

A magnetic South pole at the face, and a magnetic North pole at the back of the switch at the same time produce a concentrated field through the switch. A magnetic South pole applied to the reverse side of the switch will offset the effects of a South pole applied to the switch face. Conversely, a North pole may be applied to the back side of the switch so the device is normally on, and a North pole approaching the switch face will turn it off.

9

LOW-COST HALL EFFECT DIGITAL SWITCHES

Sprague offers 10 different Hall Effect switches from its automated high-volume production, packaging and test facilities in Concord, N.H. These rugged solid-state switches operate with small low-cost commercially available permanent magnets.

The devices feature "no-bounce" contactless switching to 100,000 Hz, circuit operation over a wide range of specified supply voltages (4.5 to 25 V), and constant amplitude output. Output stages are easily interfaced with a variety of output loads.

Each Hall Effect switch is a plastic-packaged monolithic integrated circuit: a voltage regulator, Hall voltage generator, signal amplifier, trigger circuit and output transistors on a single silicon chip.

Output transistors are normally OFF until a magnetic activating field exceeds a specified operate point. Switched ON the transistors will sink up to 25 mA. See Electrical Characteristics below.

The output transistors switch OFF when the activating field drops below a specified release point that is a lower value than the operate point. This switching hysteresis characteristic insures unambiguous, non-oscillatory switching.

FUNCTIONAL BLOCK DIAGRAM
TYPE UGN-3013, UGN-3019, UGN-3020, and UGN-3030 "T" Pack

DWG. NO. A-10.319
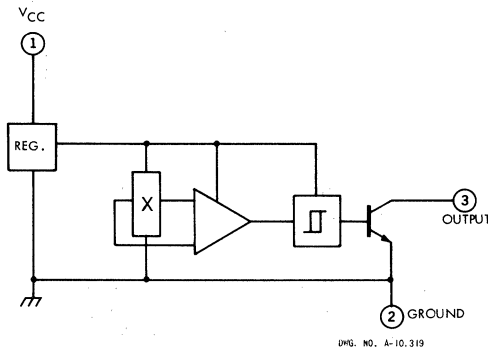
FUNCTIONAL BLOCK DIAGRAM
TYPE UGN-3201 and UGN-3203 8-Pin DIP and UGN-3220 "S" Pack

DWG. NO. A-10.898
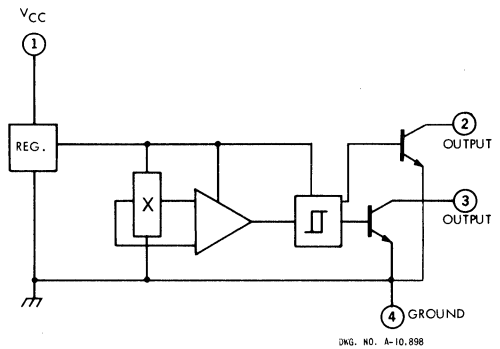
ELECTRICAL CHARACTERISTICS

Characteristics	UGN-3013T/U	UGN-3019T/U UGS-3019T/U	UGN-3201M	UGN-3203M	UGN-3020T/U UGS-3020T/U	UGN-3030T/U UGS-3030T/U	UGN-3040T/U	UGN-3220S
V_{CC} Max. V_{OUT} Max. (Logical 1)	17V	25V	20V		25V			17V
I_{SINK} Max. (Logical 0)	25 mA		2(25) mA*		25 mA			2(25) mA*
Operate Point in Gauss — Max.	450	500	750	350	350	250	200	350
Operate Point in Gauss — Typ.	300	420	450	235	220	160	150	220
Release Point in Gauss — Typ.	225	300	300	100	165	110	100	160
Release Point in Gauss — Min.	25	100	100	25	50	−250	50	50
Package	3-Pin "T" or "U" Pack		8-Pin DIP		3-Pin "T" or "U" Pack			4-Pin "S" Pack

T_A Max. Operating Temperature for UGN prefix devices is 0°C to +70°C.
T_A Max. Operating Temperature for UGS prefix devices is −40°C to +125°C.
*Dual Outputs

SUGGESTED OUTPUT LOADS FOR HALL EFFECT SWITCHES

The output of each Sprague Hall Effect switch is a grounded-emitter, open-collector structure. In the absence of a magnetic field the output transistor is OFF and switches ON when the proper field is applied to the associated Hall voltage generator.

The graph at bottom left illustrates the typical output ON voltage level as a function of temperature for the UGN-3019T.

Below are some suggested interfacing approaches. Many techniques can be used and are discussed in the following pages.
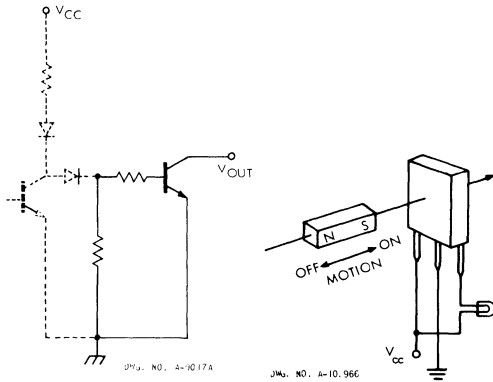
With a simple external resistor network the output can be interfaced with transistors, triacs, SCRs or common DTL, TTL, RTL and MOS logic circuits. Any type of load within specified current and voltage limitations is possible. Transient suppression may be required on all inductive loads.

Output is specified in the engineering bulletins in terms of positive logic: low or ON voltage level = 0; high or OFF voltage level = 1. In the logic "1" state, the output is guaranteed to sustain a specified voltage level. The UGN-3019T is capable of sinking up to 15 mA with a voltage drop of less than 400 mV.

Specific device type numbers are referenced in this section in discussion of applications, loads and interfacing techniques. However, all Sprague Hall Effect switches may be used in the same way provided the total sink current and maximum OFF voltage levels do not exceed values specified for each device.

Switching Common Loads With The UGN-3020T

The UGN-3020T is supplied in a 3-pin plastic "T" Pack. The branded side of the package is the face. Terminals are, from left-to-right facing the package, the input (V_{CC}) terminal, common ground and output terminals.

Supply voltage is any value between +4.5 and +24 volts applied between the V_{CC} terminal and common ground. The absolute maximum output terminal sink current is 25 mA. Voltage drop at 25 mA is typically 0.2 volts.

Note that the voltage on the output terminal must always be positive (+).

The South pole of the magnet shown below will activate the UGN-3020T in a head-on mode, at a typical distance of 0.12″ from the switch face (typical operate point is 220 gauss). The switch is turned OFF by removing the magnet to a distance of 0.16″ from the switch (typical release point is 165 gauss).

Light-Emitting-Diode

Let's connect a load, a light-emitting-diode. We have a +12 volt supply. We must connect a current-limiting resistor in series with the diode to keep the ON current under 50 mA maximum, as illustrated below.

If the LED drops 1.4 volt, we need a resistor of $\frac{12 \text{ V} - 1.4 \text{ V}}{.05 \text{ A}} = 212$ ohms. The closest standard value is 220 ohms.

DWG. NO. A-10.962
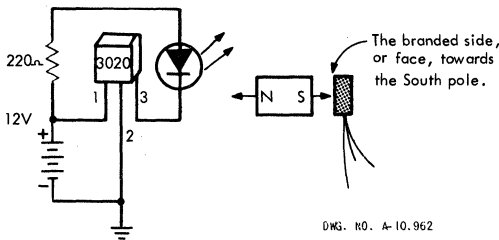
40669 Triac

The RCA 40669 triac is often used to control a-c loads up to 8 amperes rms maximum. We must add a current gain stage between the UGN-3020T and the 40669 triac.

When the Hall switch is turned on, it supplies 9 mA of base current to the 2N5811 which turns on and supplies 80 mA of drive to the triac. Note that the +12 volt supply common ground is connected to the low side of the a-c line. Be careful. If the high and low are mixed up the Hall switch could be hot!

DWG. NO. A-10.963
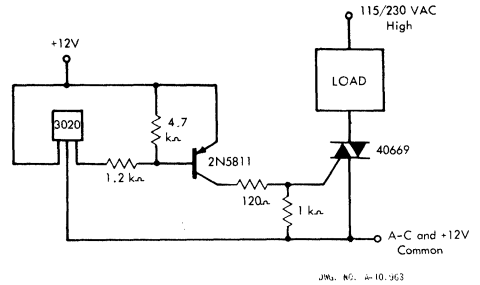
D-C Load 4 Amperes

When the UGN-3030T is activated, base drive is pulled away from the 2N5812. Collector current then flows to the base of the 2N3055. A 4 ampere load can be activated.

DWG. NO. A-10.964
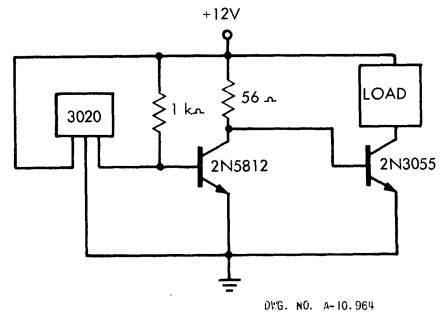
TTL/DTL

The popular TTL 7400 series is quite simple to drive. The UGN-3020T, switched ON, will sink the 1.6 mA maximum to operate the 7400.

DWG. NO. A-10.965
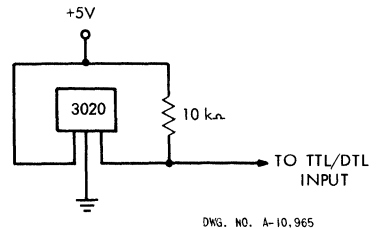
Isolating The Switch From The A-C Line

It is desirable to isolate the Hall Effect switch from the a-c line for many control applications driving line-operated loads. A Fairchild MC-232 photo-isolator may be used to accomplish this design.

The activated UGN-3020T will draw current through the LED. The current must be limited to 50 mA. A 5-volt supply is used. The calculation is

$$R = \frac{V_{CC} - V_F (LED)}{I} = \frac{5\ V - 1.4\ V}{.05\ A} = 72\ ohms.$$

The resistor selected is the closest standard value — 68 ohms. The LED drives the detector which supplies 70 mA to drive the triac. Note that the 10 volt power supply, consisting of the 6.3-volt transformer, diode and capacitor, can supply detector bias for several of these control circuits.
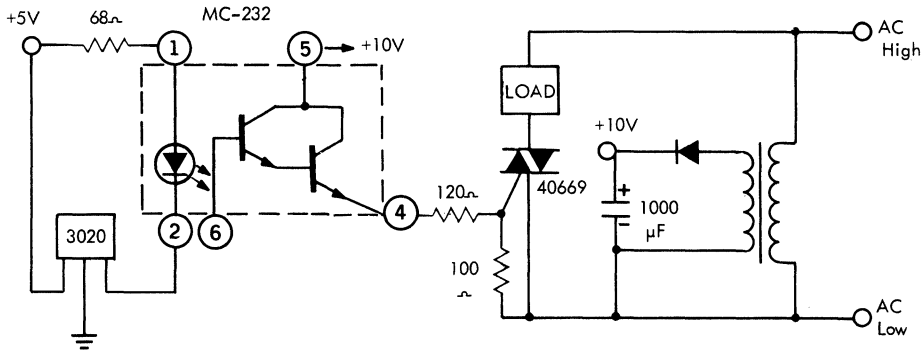
DWG. NO. A-10,961

Types UGN-3013T, UGN-3019T, UGS-3019T, UGN-3020T, UGS-3020T, UGN-3030T, UGS-3030T, UGN-3040T, and UGN-3501T are supplied in 3-pin plastic "T" packages 0.080" (2.03 mm) thick. These Hall effect devices are also available in 3-pin plastic "U" packages 0.061" (1.54 mm) thick. The "U" package is specified by replacing the "T" suffix to the part number with a "U" (UGN-3013U).

9

LINEAR OUTPUT HALL EFFECT SENSORS

TYPE UGN-3501T

Utilizing the Hall Effect for sensing a magnetic field, Type UGN-3501T integrated circuits provide a linear single-ended output which is a function of magnetic field intensity. Integrating the Hall cell and the amplifier into one monolithic device minimizes problems related to the handling of millivolt analog signals.

This sensor, supplied in a 3-pin plastic package, is rated for continuous operation over the temperature range of 0°C to +70°C and a voltage range of 8 to 12 volts d-c.

The functional block diagram for the UGN-3501T is shown below.

FUNCTIONAL BLOCK DIAGRAM

DWG. NO. A-10.524
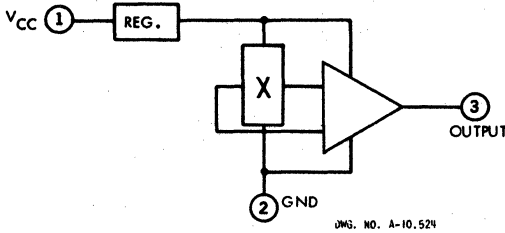
TYPE UGN-3501M

The Type UGN-3501M Hall Effect IC includes a monolithic Hall cell, linear differential amplifier, differential emitter follower output, and a voltage regulator.

Provisions are included for output offset null. This sensor is supplied in an 8-pin dual in-line plastic package and is rated for continuous operation over the temperature range of 0°C to +70°C and a voltage range of 8 to 16 volts d-c.

The figure below shows the functional block diagram for the UGN-3501M Hall Effect Sensor.

FUNCTIONAL BLOCK DIAGRAM

Dwg. No. A-11,119
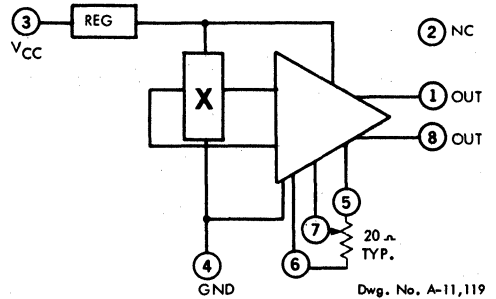
OUTPUT VOLTAGE AS A FUNCTION OF AIR GAP FOR HEAD-ON MODE OF OPERATION

Dwg. No. A-10,519A

DWG. NO. A-10,531B
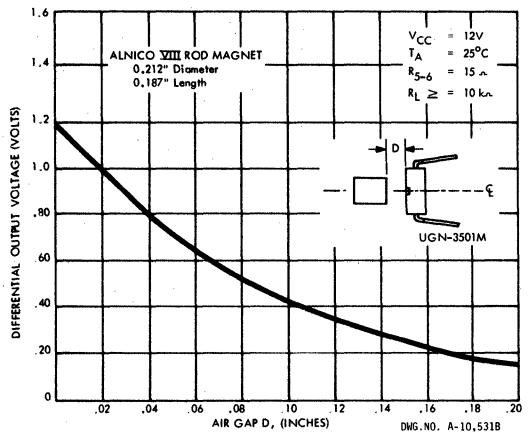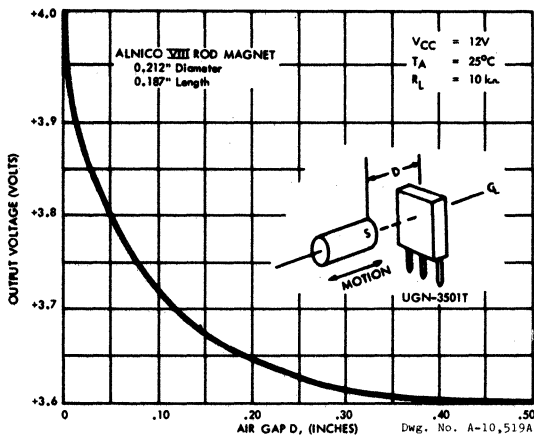
APPLICATIONS FOR TYPE UGN-3501T SENSORS

These devices are used principally to sense relatively small changes in a magnetic field — changes which are too small to operate a 'Hall Effect' switching device. They are customarily capacitively coupled to an amplifier, which boosts the output to a higher level.

The UGN-3501T is a single output linear device having a sensitivity of 700 mV/1000 gauss, and output offset which is typically +3.6 volts, at a V_{CC} of +12 volts.

The device will respond to magnetic North and South poles directed to the face or reverse side of the 3-pin ''T'' package, as illustrated below.
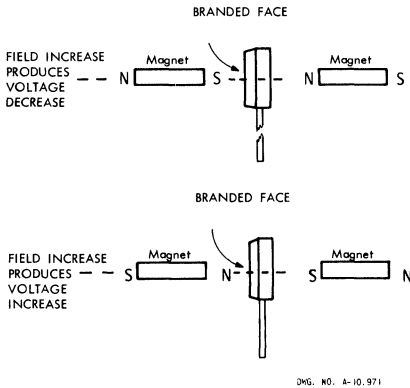
OUTPUT VOLTAGE AS A FUNCTION OF MAGNETIC FLUX DENSITY

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... +16V
Output Current, I_{OUT} 4mA
Magnetic Flux Density, B .... No Limit
Operating Temperature Range, T_A .... 0°C to +70°C
Storage Temperature Range, T_S .... -65°C to +150°C

ELECTRICAL CHARACTERISTICS at V_{CC} = 12 VDC, T_A = +25°C

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Operating Voltage	V_{CC}		8.0	—	12	V	—
Supply Current	I_{CC}	V_{CC} = 12V	—	10	20	mA	—
Quiescent Output Voltage	V_{OUT}	B = 0 Gauss	2.5	3.6	5.0	V	1
Sensitivity	ΔV_{OUT}	B = 1000 Gauss	350	700	—	mV	1, 2
Frequency Response	f(-3dB)		—	25	—	kHz	—
Broadband Output Noise	e_n	3dB B.W. 10 Hz to 10 kHz	—	0.10	—	mV	—
Output Resistance	R_O		—	100	—	Ω	—

NOTE 1. All output voltage measurements are made with a voltmeter having an input impedance of 10 kΩ or greater.
NOTE 2. Magnetic flux density is measured at the most sensitive area of the device, which is centered on the branded side of the package 0.042 ±0.001'' (1.07 ±0.03 mm) below the surface of the T package or 0.022'' ±0.001'' (0.56 ±0.03 mm) below the surface of the U package.

Ferrous Metal Detector

Two similar detector designs are illustrated below. One senses the *presence* of a ferrous metal, the other senses an *absence* of the metal. The two sensing modes are accomplished simply by reversing the magnet poles relative to the UGN-3501T. The pole of the magnet is fixed in contact with the reverse side of the UGN-3501T in both cases.

Frequency response characteristics of this circuit are easily controlled by changing the input decoupling capacitor value for the low-frequency breakpoint. If high-frequency attenuation is desired a capacitor may be used to shunt the feedback resistor.
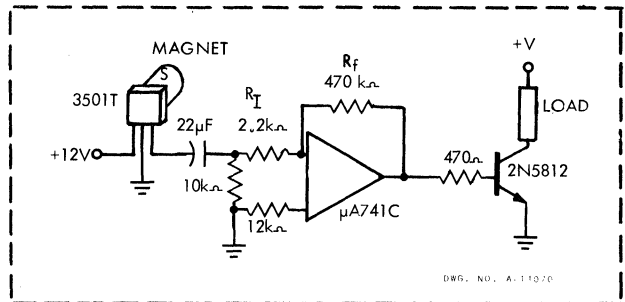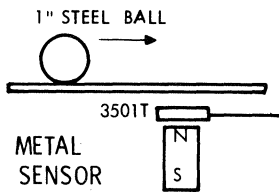
Metal Sensor

The North pole of the magnet is fixed to the reverse side of the UGN-3501T. The sensor is in contact with the bottom of a $3/32''$ epoxy board. A 20 mV peak output change (decrease) is produced as the 1'' steel ball rolls over the sensor. This signal is amplified by the μA741C to drive the 2N8512 ON to carry a 0.5 A collector current.
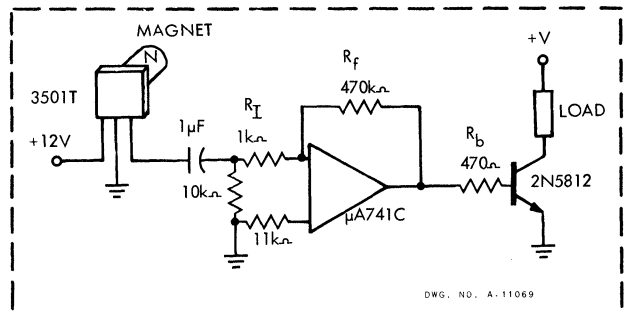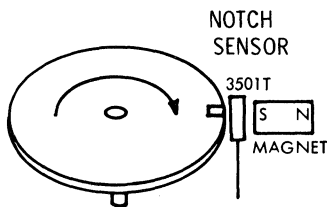
Notch Sensor

The South pole of the magnet is fixed to the reverse side of the UGN-3501T. The sensor is $1/32''$ from the edge of the steel rotor. A $1/16''$ wide by $1/8''$ deep slot in the rotor edge passing the sensor causes a 10 mV peak output change (decrease). This signal is amplified by the μA 741C to drive the 2N5812 ON, carrying a 0.5 A collector current.

Note that in both examples the branded side of the UGN-3501T faces the material (or lack of material) to be sensed. In both cases the presence (or absence) of the ferrous metal changes the flux density at the Hall Effect sensor so as to produce a negative going output pulse. This pulse is inverted by the amplifier to drive the transistor ON.

Printer Application For The UGN-3501T

The application below is for a sensor that will sense lobes on the character drum. Lobes are spaced $\approx {}^3/_{16}''$ apart around the circumference, are $\approx \frac{1}{4}''$ long and rise 10 to 15 mils from the surface of the drum.

DWG. NO. A-11072
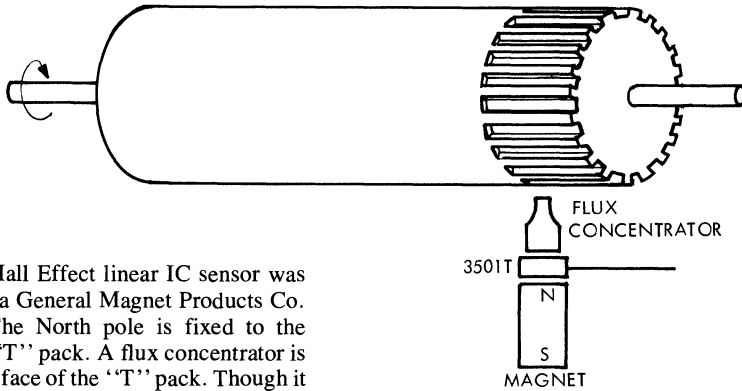
A UGN-3501T Hall Effect linear IC sensor was used with an Indiana General Magnet Products Co. SR8522 magnet. The North pole is fixed to the reverse side of the "T" pack. A flux concentrator is fixed to the branded face of the "T" pack. Though it does not provide a flux return path, a concentrator will "focus" the magnetic field through the switch.

The concentrator "blade" at right is aligned with the drum lobe at an air gap distance of 0.01''. The output change is 10 mV peak, amplified as shown to develop a +3 volt output from the operational amplifier, driving the transistor ON.

Sensitivity is so great in this configuration the UGN-3501T output signal base line tracked the eccentricities in the drum quite closely. This affected the lobe resolution, but the lobe position may still be measured.

DWG. NO. A-11.071

9
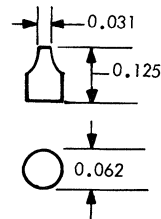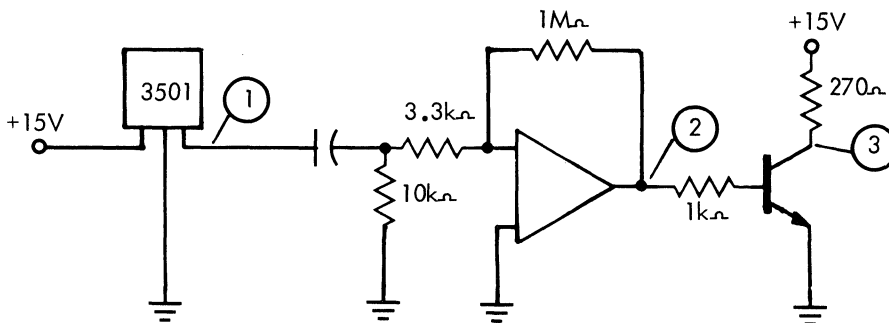
DWG. NO. A-11073

APPLICATIONS FOR TYPE UGN-3501M SENSORS

Type UGN-3501M sensors are well-suited for accurate measurement and/or control of position, weight, thickness, velocity, current, etc. The device provides a linear differential output which is a function of magnetic field intensity, with a typical sensitivity of 1.4 volts/1000 gauss.

Either magnetic pole can be used. Pins 1 and 8 are sinking and sourcing terminals for the differential output. Changing poles inverts the output. Connections may be reversed to account for this change.

The figure below shows a 20Ω trimmer potentiometer being used for output offset nulling. Pins 5, 6, and 7 may be shorted if an output offset voltage of up to ±400 mV can be tolerated.

OUTPUT VOLTAGE
AS A FUNCTION OF MAGNETIC FLUX DENSITY

DWG. NO. A-10.972

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... +16V
Output Current, I_{OUT} 2mA
Magnetic Flux Density, B .... No Limit
Operating Temperature Range, T_A .... 0°C to +70°C
Storage Temperature Range, T_S .... -65°C to +150°C

ELECTRICAL CHARACTERISTICS at V_{CC} = 12 VDC, T_A = +25°C (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units	Notes
Operating Voltage	V_{CC}		8.0	—	16	V	—
Supply Current	I_{CC}	V_{CC} = 16V	—	10	18	mA	—
Output Offset Voltage	V_{OFF}	B = 0 Gauss, R-5-6-7 = 0Ω	—	100	400	mV	1
Output Common Mode Voltage	V_{CM}	B = 0 Gauss	—	3.6	—	V	1
Sensitivity	ΔV_{OUT}	B = 1000 Gauss, R5-6-7 = 0Ω	700	1400	—	mV	1, 2
Sensitivity	ΔV_{OUT}	B = 1000 Gauss, R5-6 = 15Ω	650	1300	—	mV	1, 2
Frequency Response	f(-3dB)	R5-6-7 = 0Ω	—	25	—	kHz	—
Broadband Output Noise	e_n	3dB B.W. 10 Hz to 10kHz R5-6-7 = 0Ω	—	0.15	—	mV	—
Output Offset Voltage vs T (°C)	$\Delta V_{OFF}/\Delta T$	R5-6-7 = 0Ω	—	0.2	—	mV/°C	—

NOTE 1. All output voltage measurements are made with a voltmeter having an input impedance of 10 kΩ or greater and a common mode rejection ratio greater than 60 dB.
2. Magnetic flux density is measured at the most sensitive area of the device, which is on the top center, 0.037 ±0.001″ (0.94 ±0.03mm) below the surface.

Motion Measurement With Permanent Magnets

The UGN-3501M, properly biased, will produce the output voltage values shown below when activated in a head-on mode of operation.

Note the output voltage curve is almost linear over the first 0.04'' of travel. The change rate here is 10 mV/0.001'' air gap change.

The same magnet used in a "slide-by" mode of operation will produce the three curves presented at bottom.

Movement measurements would generate the largest outputs and most accurate readings where they are centered on the steepest portion of each curve, and are confined to the linear segment of that curve. This is the case for the head-on and the slide-by curves.

For example, in a slide-by mode of operation with an 0.03'' air gap, movement to be measured could be centered at a "zero" of 0.1'' from the centerline. The voltage rate of change would be linear at 5 mV/0.001'' movement, for a movement distance of ±0.02''.

The rate of change is, of course, a function of the flux density gradient across the magnetic field for the particular magnet used. A samarium-cobalt magnet, with its relatively compact field, can produce voltage change rates to 30 mV/0.001'' movement.
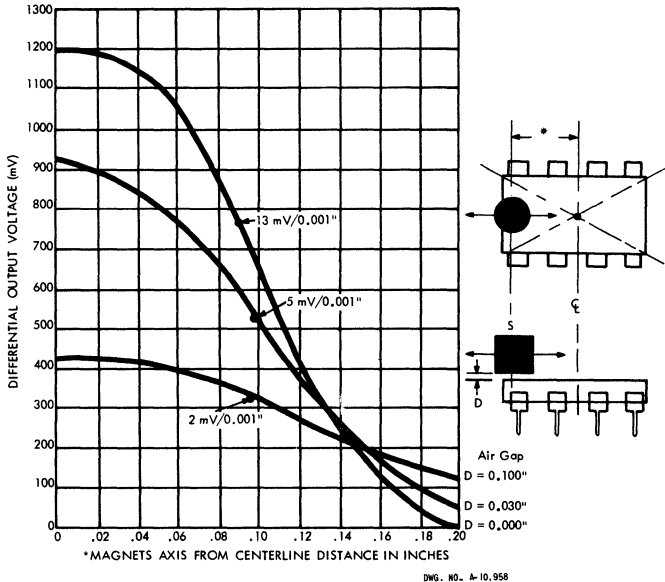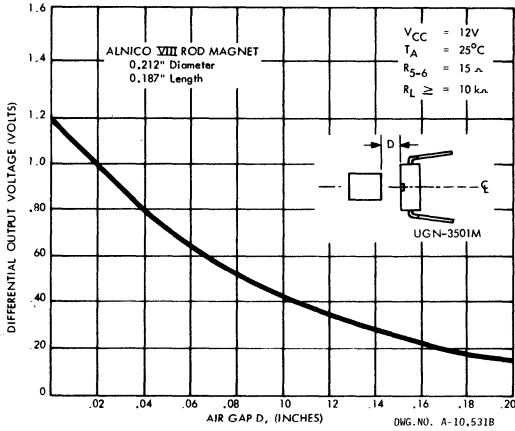
UGN-3501M Output Circuit Design

The output current handling capability of the UGN-3501M is 0.5 mA. In the differential connection one output pin sources load current, the other must sink it. A simple method for increasing drive capability is illustrated below.

DWG. NO. A-10.959
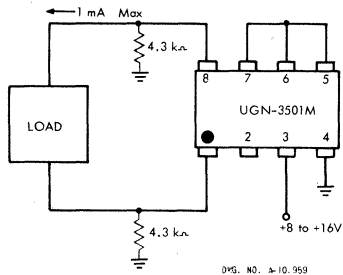
A 4.3 kΩ resistor is connected from each output pin to ground. The quiescent bias current of the output stage is increased, and the sinking capability is increased to 1 mA.

If even higher current drive capability is required, the simplest solution is the addition of a pair of emitter-followers:

DWG. NO. A-10.960
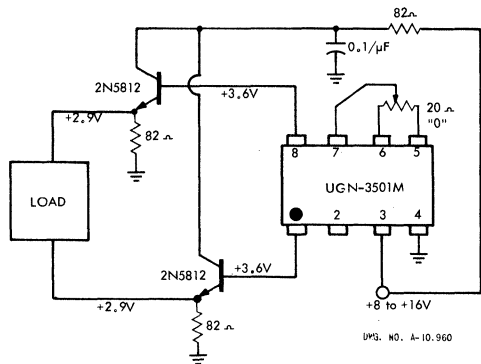
Up to 30 mA of load current can be sourced by the circuit as shown, and this can be increased considerably by using Darlington power transistors and lower resistance in the emitter circuits.

Note that the emitter-followers have no voltage gain. The output voltage differential is essentially the same as that of the UGN-3501M.

An operational amplifier will supply a voltage gain and a current gain, and transform the differential output of the UGN-3501M to a single-ended output. (The circuit will drive a load which has one side grounded.)

DWG. NO. A-10.950
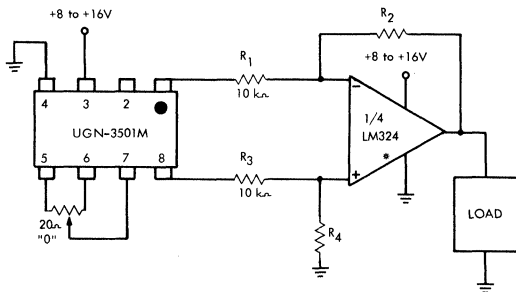
The LM-324 quad operational amplifier will operate from a single power supply if the output does not swing in the negative direction. Pin 1 of the UGN-3501M does swing negative when a magnetic South pole approaches the device surface. Pin 1, therefore, is connected to the negative or inverting input of the LM-324, and its output swings in the positive direction. Reversing connections to pins 1 and 8 allows the output to respond to a magnetic North pole. If the application requires the output be capable of swing both negative and positive, then a dual ± power supply would have to be used.

$$Voltage\ amplification \approx \frac{R_2}{R_1}$$

with
$$R_1 = R_3$$
$$R_2 = R_4$$

The LM-324 can source 40 mA. Other operational amplifiers suitable for single supply operation are MC-3403P, MC-3458P1, CA-3160E.

Current Sensing Applications

The UGN-3501M is ideally suited for current measurement applications. Typical applications are overload detectors for electric motors, current limiters for high-current power supplies, clamp-on current probes for high-current d-c loads, etc.

The standard toroid is typical of small commercially-available electromagnetic devices which can be used with the UGN-3501M:

1" O.D.,5/8" I.D.
1/4" H., 0.08" GAP

UGN3501M

DWG. NO. A-10.951A
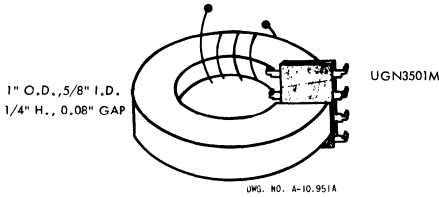
With this toroid, the UGN-3501M, fixed in the gap, would "see" 5.6 gauss per ampere-turn. To "read" from zero to 20 amperes, 9 turns would develop 9 x 20 x 5.6 = 1008 gauss. The UGN-3501M would have a 1.4 volt output with a 20 ampere activating current.

Gaussmeter Applications

A typical UGN-3501M has a differential output of 1400 mV in a 1000 gauss field. Using a 100 μA movement, with a series calibrating trimmer potentiometer, a simple gaussmeter suitable for many applications can be easily produced:

"CAL"
10 k$\wedge$
"0" 20$\wedge$
Voltmeter 10 k$\wedge$/V Min.
8 7 6 5
UGN-3501M
2 3 4
+8 to +16V
DWG. NO. A-10.952
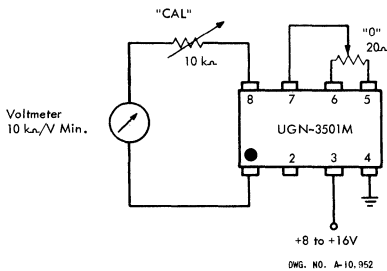
The UGN-3501M is quite linear to $\approx$ 1000 gauss. The input differential stage gain must be reduced to maintain linearity beyond this range.

A 47Ω $\pm$5% resistor in series with pins 5 and 6 extends the useful linear range to 3000 gauss:

"0" 20$\wedge$
"CAL" 10 k$\wedge$
47$\wedge$ 47$\wedge$
Voltmeter 10 k$\wedge$/V Min.
8 7 6 5
UGN-3501M
2 3 4
DWG. NO. A-10.953
+8 to +16V
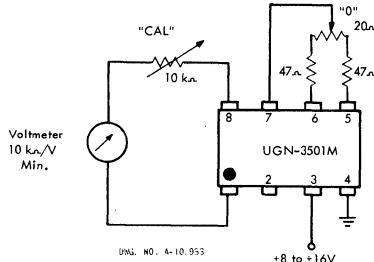
Calibrating The UGN-3501M Gaussmeter

Where applications require the differential output voltage at pins 1 and 8 be calibrated, dual precision 100 ohm variable resistors may be used:

"0" 20$\wedge$
100$\wedge$ PRECISION CONCENTRIC
VOLTMETER 10k$\wedge$/V Min.
8 7 6 5
UGN - 3501M
2 3 4
DWG. NO. A-10.949
+V$_{CC}$
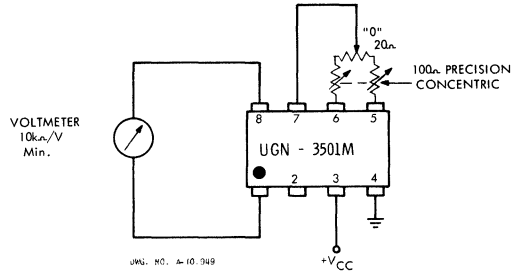
A calibration field can be constructed using standard Stancor C-2709 filter chokes, with the pole pieces removed and the center magnetic path completed with a section of the pole piece removed. Brass stock $1/16''$ x $1/2''$ x $4 3/8''$ was used for mechanical support, 2 pieces in the front and 2 pieces in the rear, plus $4 1/4''$ x $1''$ No. 6-32 threaded standoffs. The air gap was set at $3/8''$ as depicted below.

BRASS STOCK
N S
THREADED STANDOFFS
3/8"
AIR-GAP
BASE
DWG. NO. A-10.948

9
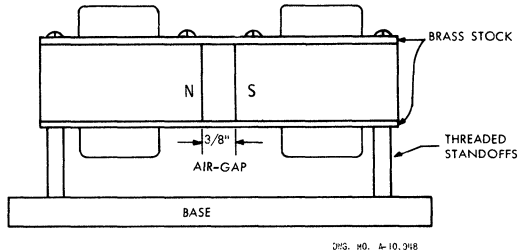
The chokes are wired in series opposing, and are driven from a constant current source. Initial calibration may be accomplished with a UGN-3600 Hall generator supplied with a calibration curve. The current is fixed at the value which produces 1000 gauss.

The UGN-3501M to be calibrated is "zeroed" and placed in the 1000 gauss field. The dual precision variable resistor is adjusted until the output is 1 volt. The UGN-3501M circuit is re-zeroed out of the field and the calibration rechecked.

The value of the precision variable resistor is then measured. Two 1% resistors of the closest standard value replace these in the final circuit configuration.

Check Oscillation Problems

The UGN-3501M has a relatively wide band width. Oscillation is the most common problem encountered in applications for the device, caused by excessive lead lengths (2") on the zero control, and coupling between the zero control leads and the output leads from pins 1 and 8. (If moving your hand near the zero control changes the output voltage — there are oscillation problems.)

Solutions to oscillation problems are: 1) cut the zero control lead lengths; 2) separate the zero control and output leads; and 3) (in extreme cases) use a low-pass filter on the output:
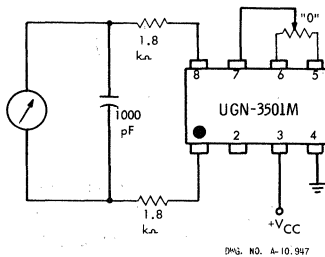
Sensitivity Variations

Note that the UGN-3501M is specified with a typical sensitivity of 1.4 mV/gauss and a minimum sensitivity of .7 mV/gauss. Unless a special "sort" is ordered, plan on this variation.

Note also that the "0" output varies typically 1 mV/°C, a major factor in determining a minimum detectable long term signal.

The sensitivity varies with temperature and V_{CE}. The output voltage is a function of the load resistance. These factors are illustrated in the graphs at right.

NORMALIZED SENSITIVITY AS A FUNCTION OF TEMPERATURE
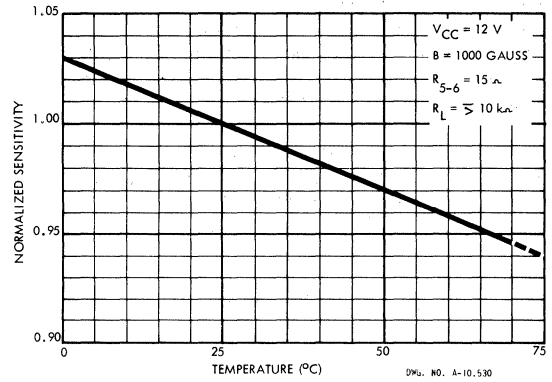
NORMALIZED SENSITIVITY AS A FUNCTION OF V_{CC}

RELATIVE OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE

9—54
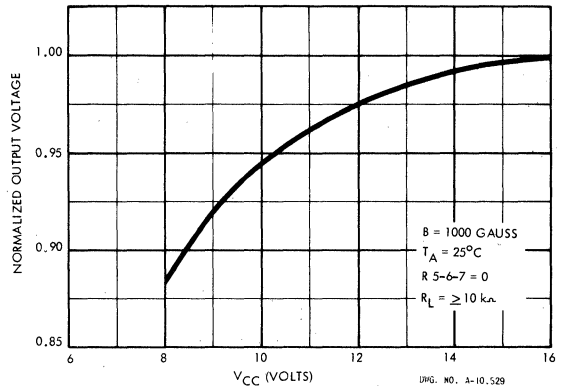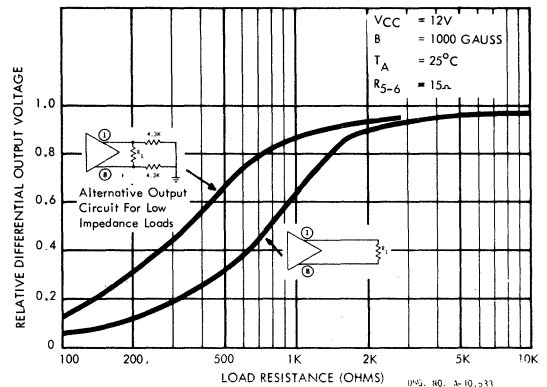
Type UGN-3604M/UGN-3605M Hall Cells

The UGN-3604M is a basic Hall voltage generator in an 8-pin DIP package, supplied with a calibration chart. Intended for use as a design or production test aid, the UGN-3604M permits accurate measurement of magnetic field inlensity as a means of aligning magnet/Hall switch positions, and for calibrating Hall Effect sensor circuits.

A UGN-3605M is the same Hall voltage generator without a calibration chart. Supply voltage for these units is 5 volts. Below is the terminal pinning diagram for UGN-3605M.

```
Vcc  1        8  NC
-VH  2        7  NC
GND  3        6  NC
+VH  4        5  NC
```
Dwg. No. A-11,122

PACKAGE INFORMATION

Sprague's Hall Effect IC's are packaged in a special epoxy material formulated to handle severe service environments. It is impervious to all commercially available consumer and industrial solvents and degreasing compounds, oils and alkaline chemicals. It is susceptible only to hot (+150°C) concentrated fuming red nitric acid applied under pressure.

The material has a continuous thermal rating of +150°C, and a hot-spot rating (100 hours) of +170°C. It is classed by Underwriters' Laboratories, Inc. as a self-extinguishing material. Its resistivity is 10^{15} ohms. Thermal coefficient of expansion (T_G) is 30 x 10^{-6}ppm/°C.

Device leads will meet solderability requirements of Military Standard MIL-STD-202 (95% or better solder-wetting without special preparation).

Applications at Sprague Electric Co.
(We use them . . . and love them)

Hall Effect ICs are designed into Sprague's own production and test equipment. Position-sensing digital switches control and monitor high-speed automatic machine operations. Hall Effect switch output provides direct input to a microprocessor-based control unit.

Data is compiled continuously from critical points in the production process. The control informs the machine operator, makes automatic adjustments, indicates manual adjustments which may be necessary, and reports on production.

Hall Effect ICs perform simultaneous control and reporting functions. Extremely reliable precise repetitive operation of these switches helps to achieve and maintain very high levels of process control and product quality.

Catalog Numbering System

UG N - 3501 M

Package Style
C = Chip
H = Hermetic DIP
M = Plastic DIP
S = Plastic 4-Pin SIP
T = Plastic 3-Pin SIP
U = Plastic 3-Pin SIP
Device Number

Temperature Range
N = 0°C to +70°C
S = -40°C to +125°C

Semiconductor Family
UG = Hall Effect Device

3-Pin "T" Pack or "U" Pack*

TERMINAL LEAD DESIGNATION
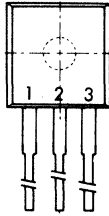
LOCATION OF SENSOR CIRCUIT

UGN-3013T/U
UGN-3019T/U
UGS-3019T/U
UGN-3020T/U
UGS-3020T/U
UGN-3030T/U
UGS-3030T/U
UGN-3501T/U
UGN-3075T/U
UGS-3075T/U
UGN-3076T/U
UGS-3076T/U
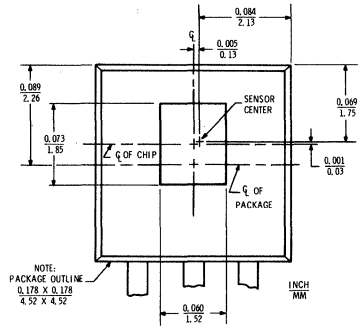
1 = V_{CC}
2 = GND
3 = V_{OUT}

NOTE:
PACKAGE OUTLINE
0.178 X 0.178
4.52 X 4.52

$\frac{INCH}{MM}$

Dwg. No. A-11,896A

*The "T" package is 0.080'' (2.03 mm) thick; the "U" package is 0.061'' (1.54 mm) thick; All other dimensions are identical.

4-Pin "S" Pack

TERMINAL LEAD DESIGNATION

LOCATION OF SENSOR CIRCUIT

UGN-3220S

SENSOR
CENTER

.0045
.11
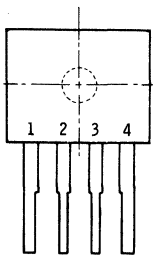
1 = GND
2 = V_{OUT_1}
3 = V_{OUT_2}
4 = V_{CC}

Dwg. No. A-11,105

.002
.05

$\frac{IN}{MM}$

Dwg. No. A-11,009
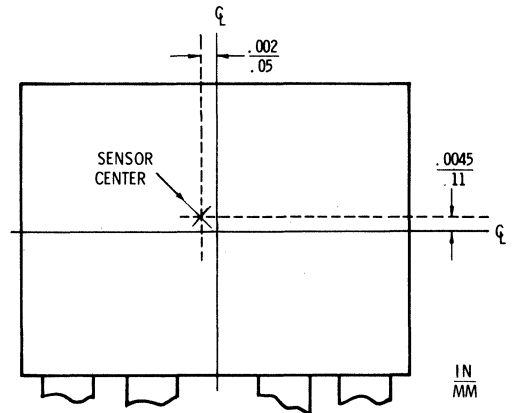
8-Pin "M" Package

TERMINAL LEAD DESIGNATION

Dwg. No. A-11,120

UGN-3201M
UGN-3203M

Dwg. No. A-11,121
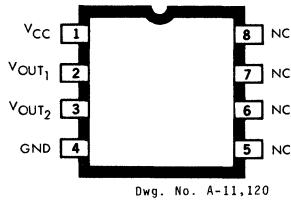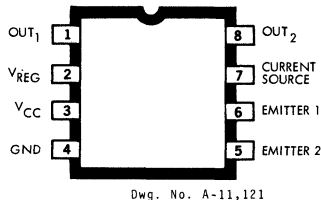
UGN-3501M

SENSOR CIRCUIT LOCATION

Dwg. No. A-11,012
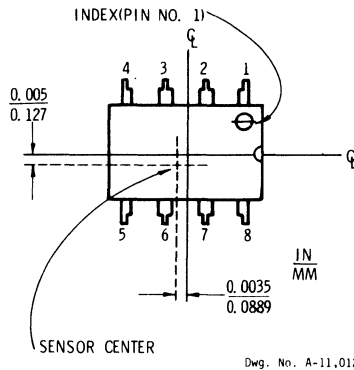
Magnet Marketplace

A strong field of magnetic components manufactur-ers can supply parts suitable for use in virtually any conceivable Hall Effect IC application. Comprehensive listings of these suppliers are presented in reference documents such as the Thomas Register.

Many of these firms are familiar with Hall Effect ICs application.

Magnetic components available from these manufacturers include ALNICO, rare-earth, ceramic, and plastic permanent magnets in a variety of form factors such as rods, bars, rings, sheets, etc. Ferromagnetic components for use as electro-magnets, concentrators, actuators, etc. are also available.

Additional information on all
Hall Effect devices is available from:

Sprague Electric Company
Hall Effect IC Marketing
70 Pembroke Road
Concord, New Hampshire 03301
(603) 224-1961

A representative listing:

Indiana General Magnet Products Co.
405 Elm St.
Valparaiso, Indiana 46383
(219) 462-3131

Hitachi Magnetics Corporation
Edmore, Michigan 48829
(517) 427-5151

Xolox Corporation
3111 Covington Rd.
Ft. Wayne, Indiana 46804
(219) 432-4532

The Electrodyne Company, Inc.
4188 Taylor Rd.
Ontavia, Ohio 45103
(513) 732-2822

Stackpole Carbon Company
Magnet Division
Kane, Pennsylvania 16735
(814) 837-7000

Spectra-Flux, Inc.
124 Manfre Rd.
Watsonville, California 95076
(408) 722-8133

The Arnold Engineering Co.
Railroad Ave. & West, Box G
Marengo, Illinois 60152
(815) 568-2000

9

SECTION 10—TRANSISTOR ARRAYS AND MISCELLANEOUS DEVICES

*New Product—Contact Factory for Information.

10

ULN-2031A, ULN-2032A, AND ULN-2033A
HIGH-CURRENT DARLINGTON TRANSISTORS ARRAYS

SPRAGUE TYPE ULN-2031A, ULN-2032A, and ULN-2033A High-Current Darlington Transistor Arrays are comprised of seven silicon Darlington pairs on a common monolithic substrate. The Type ULN-2031A consists of 14 NPN transistors connected to form seven Darlington pairs with NPN action. The Type ULN-2032A ($h_{FE} = 500$ min.) and the Type ULN-2033A ($h_{FE} = 50$ min.) consist of seven NPN and seven PNP transistors connected to form seven Darlington pairs with PNP action. All devices feature a common emitter configuration.

These devices are especially suited for interfacing between MOS, TTL, or DTL outputs and 7-segment LED or tungsten filament indicators. Peak inrush currents to 100mA are allowable. They are also ideal for a variety of other driver applications such as relay control and thyristor firing.

Type ULN-2031A, ULN-2032A, and ULN-2033A transistor arrays are housed in 16-lead DIP plastic packages which include a separate substrate connection for maximum circuit design flexibility.

DWG. No. A.9202

ULN-2031A

DWG. No. A.9201
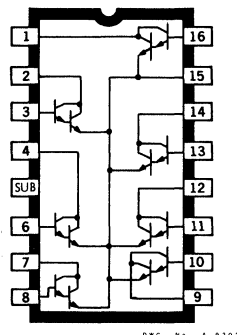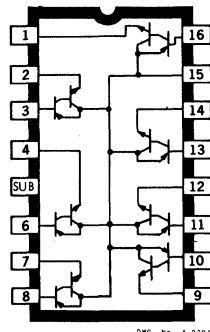
ULN-2032A
ULN-2033A

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
(unless otherwise noted)

Power Dissipation (any one Darlington pair)..500mW
                (total package)..750mW
Derating Factor Above +25°C..6.67mW/°C
Ambient Temperature Range (operating), T_A..−20°C to +85°C
Storage Temperature Range, T_S..−55°C to +125°C
Individual Darlington Pair Ratings:
  Collector-to-Emitter Voltage, V_{CEO}..16V
  Collector-to-Base Voltage, V_{CBO}..40V
  Collector-to-Substrate Voltage, V_{CIO}...40V
  Emitter-to-Base Voltage, V_{EBO}
    Type ULN-2031A...5V
    Type ULN-2032A and ULN-2033A...40V
  Continuous Collector Current, I_C..80mA
  Continuous Base Current, I_B..5mA

NOTE:
    The substrate must be connected to a voltage which is more negative than any collector or base voltage so as to maintain isolation between transistors, and to provide normal transistor action.

ELECTRICAL CHARACTERISTICS at T_A = +25°C

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 500\mu A$	40	—	—	V
Collector-Substrate Breakdown Voltage	BV_{CIO}	$I_C = 500\mu A$	40	—	—	V
Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1mA$	16	—	—	V

Emitter-Base Breakdown Voltage
  Type ULN-2031A
  Type ULN-2032A and ULN-2033A
	BV_{EBO}	$I_E = 500\mu A$	
			5
			40
				
				—
				—
					
					—
					—
						
						V
						V

D-C Forward Current Transfer Ratio
  Type ULN-2031A and ULN-2032A
  Type ULN-2033A
	h_{FE}	$V_{CE} = 2V, I_C = 20mA$	
			500
			50
				
				—
				—
					
					500
						
						—
						—

Base-Emitter Saturation Voltage
  Type ULN-2031A
  Type ULN-2032A and ULN-2033A
	$V_{BE(SAT)}$	$I_C = 20mA, I_B = 500\mu A$	
			—
			—
				
				—
				—
					
					2
					1
						
						V
						V

Collector-Emitter Saturation Voltage
  Type ULN-2031A and ULN-2032A
 	
  Type ULN-2033A
	$V_{CE(SAT)}$	$I_C = 20mA, I_B = 40\mu A$
		$I_C = 80mA, I_B = 1mA$
		$I_C = 20mA, I_B = 400\mu A$
		$I_C = 80mA, I_B = 2mA$
			—
			—
			—
			—
				—
				—
				—
				—
					1.2
					1.5
					1.2
					1.5
						V
						V
						V
						V

Collector Cutoff Current	I_{CEO} I_{CBO}	$V_{CE} = 8V$ $V_{CB} = 10V$	— —	— —	100 10	μA μA

10

ULS-2045H AND ULN-2046A TRANSISTOR ARRAYS
(Three Isolated Transistors
and One Differential Amplifier)

THE ULS-2045H and ULN-2046A are general-pur-
pose transistor arrays each consisting of five sili-
con N-P-N transistors on a single monolithic chip.
Two transistors are internally connected to form a dif-
ferential pair. Integrated circuit construction pro-
vides close electrical and thermal matching between
each transistor.

These arrays are well-suited for a wide range of ap-
plications such as: DC to VHF signal processing
systems; temperature-compensated amplifiers; custom
designed differential amplifiers and discrete transistors
in conventional circuits.

Two package configurations are available. Type
ULS-2045H is supplied in a hermetic 14-lead dual in-
line ceramic package and is rated for operation over
the military temperature range of −55°C to +125°C.

DWG. NO. A-8034
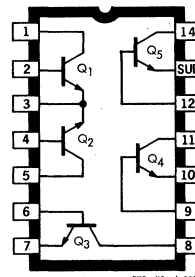
Type ULN-2046A is electrically identical to the ULS-
2045H but is supplied in a dual in-line plastic package
rated for −20°C to +85°C ambients.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
(unless otherwise noted)

	ULS-2045H		ULN-2046A		
	EACH TRANSISTOR	TOTAL PACKAGE	EACH TRANSISTOR	TOTAL PACKAGE	UNITS
Power Dissipation:					
T_A to +55°C			300	750	mW
T_A to +75°C	300	750	−	−	mW
Derating Factor:					
$T_A > +55$°C	−	−	−	6.67	mW/°C
$T_A > +75$°C	−	8	−	−	mW/°C

Collector-Base Voltage, $V_{(BR)CBO}$ 30V
Collector-Emitter Voltage, $V_{(BR)CEO}$ 20V
Collector-Substrate Voltage, $V_{(BR)CIO}$ (See note 2) 20V
Emitter-Base Voltage, $V_{(BR)EBO}$ 6V
Collector Current, I_C 50mA
Operating Temperature Range, T_A:
    Type ULS-2045H . . . . −55°C to +125°C
    Type ULN-2046A . . . . −20°C to +85°C
Storage Temperature Range, T_S: . . . . −65°C to +150°C

Notes:
1. The maximum ratings are limiting absolute values above which the serviceability may be impaired from the viewpoint of life or satisfactory per-
formance. The breakdown voltages may be far above the maximum voltage ratings. To avoid permanent damage to the transistor, do not
attempt to measure these characteristics above the maximum ratings.
2. Pin 13 is connected to the substrate. This terminal must be tied to the most negative point in the external circuit to maintain isolation between
transistors and to provide for normal transistor action.

STATIC ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\mu A, I_E = 0$	20	60		V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1mA, I_B = 0$	15	24		V
Collector-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\mu A, I_{CI} = 0$	20	60		V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\mu A, I_C = 0$	5	7		V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10V, I_E = 0$			40	nA
	I_{CEO}	$V_{CE} = 10V, I_B = 0$			0.5	μA
Static Forward Current Transfer Ratio	h_{FE}	$I_C = 10\mu A, V_{CE} = 3V$		54		—
		$I_C = 1mA, V_{CE} = 3V$	40	100		—
		$I_C = 10mA, V_{CE} = 3V$		100		—
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 10mA, I_B = 1mA$		0.23		V
Base-Emitter Voltage	V_{BE}	$I_E = 1mA, V_{CE} = 3V$		0.715		V
		$I_E = 10mA, V_{CE} = 3V$		0.800		V
Input Offset Current for Matched Pair Q_1 and Q_2	$I_{101}-I_{102}$	$I_C = 1mA, V_{CE} = 3V$		0.3	2	μA
Magnitude of Input Offset Voltage for Differential Pair	$V_{BE1}-V_{BE2}$	$I_C = 1mA, V_{CE} = 3V$		0.45	5	mV
Magnitude of Input Offset Voltage for Isolated Transistors	$V_{BE3}-V_{BE4}$	$I_C = 1mA, V_{CE} = 3V$		0.45	5	mV
	$V_{BE4}-V_{BE5}$	$I_C = 1mA, V_{CE} = 3V$		0.45	5	mV
	$V_{BE5}-V_{BE3}$	$I_C = 1mA, V_{CE} = 3V$		0.45	5	mV
Temperature Coefficient of Base-Emitter Voltage	$\dfrac{\Delta V_{BE}}{\Delta T}$	$I_C = 1mA, V_{CE} = 3V$		-1.9		mV/°C
Temperature Coefficient Magnitude of Input-Offset Voltage	$\dfrac{\Delta V_{10}}{\Delta T}$	$I_C = 1mA, V_{CE} = 3V$		1.1		$\mu V/°C$

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
Small-Signal Common-Emitter Forward Current Transfer Ratio	h_{fe}	$I_C = 1mA, V_{CE} = 3V, f = 1kHz$		110		—
Small-Signal Common-Emitter Short-Circuit Input Impedance	h_{ie}	$I_C = 1mA, V_{CE} = 3V, f = 1kHz$		3.5		$k\Omega$
Small-Signal Common-Emitter Open-Circuit Output Impedance	h_{oe}	$I_C = 1mA, V_{CE} = 3V, f = 1kHz$		15.6		μmho
Small-Signal Common-Emitter Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}	$I_C = 1mA, V_{CE} = 3V, f = 1kHz$		1.8×10^{-4}		—
Gain-Bandwidth Product	f_T	$I_C = 3mA, V_{CE} = 3V$	300	550		MHz
Emitter-to-Base Capacitance	C_{EB}	$V_{EB} = 3V, I_E = 0, f = 1MHz$		0.6		pF
Collector-to-Base Capacitance	C_{CB}	$V_{CB} = 3V, I_C = 0, f = 1MHz$		0.6		pF
Collector-to-Substrate Capacitance	C_{CI}	$V_{CS} = 3V, I_C = 0, f = 1MHz$		2.8		pF
Noise Figure	N.F.	$I_C = 100\mu A, V_{CE} = 3V, R_g = 1k\Omega$ $f = 1kHz, BW = 15.7kHz$		3.25		dB

NOTE:
   Characteristics apply for each transistor unless otherwise specified.

10

ULN-2046A-1

TRANSISTOR ARRAY

TYPE ULN-2046A-1 general-purpose transistor array consists of five silicon NPN transistors, two of which are connected as a differential amplifier. The monolithic construction provides close electrical and thermal matching between all transistors.

Except as shown in the following electrical characteristics, Type ULN-2046A-1 transistor array is identical to Type ULN-2046A.
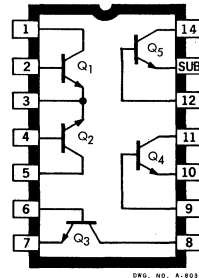
DWG. NO. A-8034

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 10\ \mu A,\ I_E = 0$	40	60	—	V
Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1\ mA,\ I_B = 0$	30	—	—	V
Collector-Substrate Breakdown Voltage	BV_{CIO}	$I_C = 10\ \mu A,\ I_{CI} = 0$	40	60	—	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10\ V,\ I_E = 0$	—	—	100	nA
	I_{CEO}	$V_{CE} = 10\ V,\ I_B = 0$	—	—	5.0	μA
Static Forward Current Transfer Ratio	h_{FE}	$I_C = 1\ mA,\ V_{CE} = 3\ V$	30	100	—	

NOTE:
   Pin 13 is connected to the substrate. This terminal must be tied to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

ULN-2047A TRANSISTOR ARRAY
(Three Differential Amplifiers)

TYPE ULN-2047A is a silicon NPN multiple transistor array comprising three independent differential amplifiers. It is specifically intended for use in switching applications such as electronic organ keyboards. All base leads are brought out on one side of the 16-lead plastic dual in-line package to simplify printed wiring board layout. A separate substrate connection permits maximum circuit design flexibility.

Type ULN-2047A is supplied in a 16-pin dual in-line plastic package.
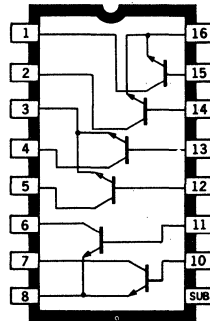
DWG. NO. A-10,231

ABSOLUTE MAXIMUM RATINGS
at 25°C Free-Air Temperature

Power Dissipation, P_D (any one transistor)............................300 mW
(total package)...............................750 mW*
Operating Temperature Range, T_A...........................−20°C to +85°C
Storage Temperature Range, T_S............................−55°C to +150°C

*Derate at the rate of 6.67 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS at 25°C Free-Air Temperature

Collector-Emitter Breakdown Voltage, BV_{CEO} (note 1)
at $I_C = 5$ mA...30 V Min.
Emitter Cutoff Current, I_{EBO} (note 2)
at $V_{EB} = 5$ V...100 nA Max.
Collector Cutoff Current, I_{CES} (note 1)
at $V_{CE} = 25$ V..100 nA Max.
D-C Forward Current Transfer Ratio, h_{FE} (note 1)
at $V_{CE} = 2$ V, $I_C = 0.1$ mA..30 Min.
at $V_{CE} = 2$ V, $I_C = 10$ mA..75 Min.
Differential Input Offset Voltage, V_{IO} (note 1)
at $V_{CE} = 2$ V, $I_{C1} = I_{C2} = 1$ mA.................................5 mV Max.

NOTES:
1. All other pins common to emitter of transistor under test.
2. Base and collector of associated transistor connected to emitter, all other pins common to base of transistor under test.

ULN-2054A TRANSISTOR ARRAY
(Dual Independent Differential Amplifiers)

THE ULN-2054A is a transistor array consisting of six silicon NPN transistors on a single monolithic chip. The transistors are internally interconnected to form two independent differential amplifiers.

The ULN-2054A is intended for a wide range of applications requiring extremely close electrical and thermal matching characteristics. Some applications are: cascade limiter circuits; balanced mixer circuits; balanced quadrature/synchronous detector circuits; balanced (push-pull) cascade/sense/IF amplifier circuits; or in almost any multifunction system requiring RF/Mixer/Oscillator, converter/IF functions.

Available in a 14-lead dual in-line plastic package the ULN-2054A is rated for operation over a −20°C to +85°C ambient temperature range.
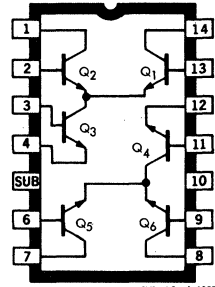
DWG. NO. A-8035A

Other features are:

● Input Offset Voltage − 5mV max.

● Input Offset Current − 2 μA max.

● Voltage gain (single-stage double ended output) − 32 dB typ.

● Common-Mode Rejection Ratio (each amplifier) − 100 dB typ.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature
(unless otherwise noted)

Power Dissipation T_A to +55°C:

    Each Transistor 300mW

    Total Package 750mW

Derating Factor, Total Package, $T_A \geq 55$°C . . . . .6.67mW/°C

Collector-Base Voltage, $V_{(BR)CBO}$ 20V

Collector-Substrate Voltage, $V_{(BR)CIO}$ (See note 2) 20V

Collector-Emitter Voltage, $V_{(BR)CEO}$ 15V

Emitter-Base Voltage, $V_{(BR)EBO}$ 5V

Collector Current, I_C 50mA

Base Current I_B 5mA

Operating Temperature Range, T_A . . . .−20°C to +85°C

Storage Temperature Range, T_S . . . .−65°C to +150°C

Notes:
  1. The maximum ratings are limiting absolute values above which the serviceability may be impaired from the viewpoint of life or satisfactory performance. The breakdown voltages may be far above the maximum voltage ratings. To avoid permanent damage to the transistor, do not attempt to measure these characteristics above the maximum ratings.
  2. Pin 5 is connected to the substrate. This terminal must be tied to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

STATIC ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 10\ \mu A,\ I_E = 0$	20	60		V
Collector-Substrate Breakdown Voltage	$V_{(BR)CIO}$	$I_C = 10\ \mu A,\ I_{C1} = 0$	20	60		V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = 1\ mA,\ I_B = 0$	15	24		V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 10\ \mu A,\ I_C = 0$	5	7		V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10\ V,\ I_E = 0$			100	nA
Base-Emitter Voltage	V_{BE}	$I_C = 50\ \mu A,\ V_{CB} = 3\ V$		0.630	0.700	V
		$I_C = 1\ mA,\ V_{CB} = 3\ V$		0.715	0.800	V
		$I_C = 3\ mA,\ V_{CB} = 3\ V$		0.750	0.850	V
		$I_C = 10\ mA,\ V_{CB} = 3\ V$		0.800	0.900	V
Temperature Coefficient of Base-Emitter Voltage	$\dfrac{\Delta V_{BE}}{\Delta T}$	$I_C = 1\ mA,\ V_{CB} = 3\ V$		−1.9		mV/°C
Input Offset Voltage	V_{IO}	$I_{E(Q3)} = I_{E(Q4)} = 2\ mA,\ V_{CB} = 3\ V$		0.45	5	mV
Input Offset Current	O_{IO}	$I_{E(Q3)} = I_{E(Q4)} = 2\ mA,\ V_{CB} = 3\ V$		0.3	2	μA
Input Bias Current	I_I	$I_{E(Q3)} = I_{E(Q4)} = 2\ mA,\ V_{CB} = 3\ V$		10	24	μA
Quiescent Operating Current Ratio	$\dfrac{I_{C(Q1)}}{I_{C(Q2)}}$	$I_{E(Q3)} = 2\ mA,\ V_{CB} = 3\ V$		0.98-1.02		—
	$\dfrac{I_{C(Q5)}}{I_{C(Q6)}}$	$I_{E(Q4)} = 2\ mA,\ V_{CB} = 3\ V$		0.98-1.02		—
Temperature Coefficient Magnitude of Input-Offset Voltage	$\dfrac{\Delta V_{IO}}{\Delta T}$	$I_{E(Q3)} = I_{E(Q4)} = 2\ mA,\ V_{CB} = 3\ V$		1.1		$\mu V/°C$

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Common-Mode Rejection Ratio For Each Amplifier	CMR	$V_{CC} = 12\ V,\ V_{EE} = -6\ V,\ V_X = 3.3\ V,$ $f = 1kHz$ (See figure 1)		100		dB
AGC Range, One Stage	AGC	$V_{CC} = 12\ V,\ V_{EE} = -6\ V,\ V_X = 3.3\ V,$ $f = 1kHz$ (See figure 2)		75		dB
Voltage Gain, Single Stage Double-Ended Output	A_v	$V_{CC} = 12\ V,\ V_{EE} = -6\ V,\ V_X = 3.3\ V,$ $f = 1kHz$ (See figure 2)		32		dB
AGC Range, Two Stage	AGC	$V_{CC} = 12\ V,\ V_{EE} = -6\ V,\ V_X = 3.3V,$ $f = 1kHz$ (See figure 3)		105		dB
Voltage Gain, Two Stage Double-Ended Output	A_v	$V_{CC} = 12\ V,\ V_{EE} = -6\ V,\ V_X = 3.3\ V,$ $f = 1kHz$ (See figure 3)		60		dB
Small-Signal Common-Emitter Forward Current Transfer Ratio	h_{fe}	$I_C = 1\ mA,\ V_{CE} = 3\ V,\ f = 1kHz$		110		—
Small-Signal Common-Emitter Short-Circuit Input Impedance	h_{ie}	$I_C = 1\ mA,\ V_{CE} = 3\ V,\ f = 1kHz$		3.5		$k\Omega$
Small-Signal Common-Emitter Open-Circuit Output Impedance	h_{oe}	$I_C = 1\ mA,\ V_{CE} = 3\ V,\ f = 1kHz$		15.6		μmho
Small-Signal Common-Emitter Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}	$I_C = 1\ mA,\ V_{CE} = 3\ V,\ f = 1kHz$		1.8×10^{-4}		—
Gain-Bandwidth Product (for Single Transistor)	f_T	$I_C = 3\ mA,\ V_{CE} = 3\ V$		550		MHz
Noise Figure (for Single Transistor)	N.F.	$V_{CE} = 3\ V,\ f = 1kHz,\ I_C = 100\ \mu A,$ $R_g = 1k\Omega,\ BW = 15.7\ kHz$		3.25		dB
Noise Figure (for each Amplifier)	N.F.	$f = 100\ MHz$		8		dB

NOTE:
Characteristics apply for each transistor unless otherwise specified.

10

AMPLIFIER TEST CIRCUITS
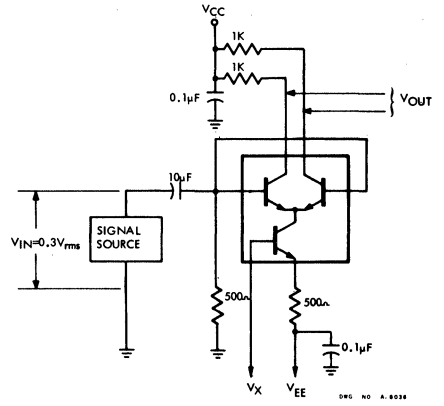
COMMON MODE REJECTION RATIO

Figure 1
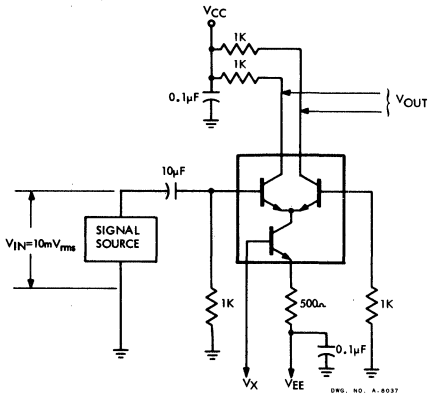
SINGLE-STAGE VOLTAGE GAIN

Figure 2
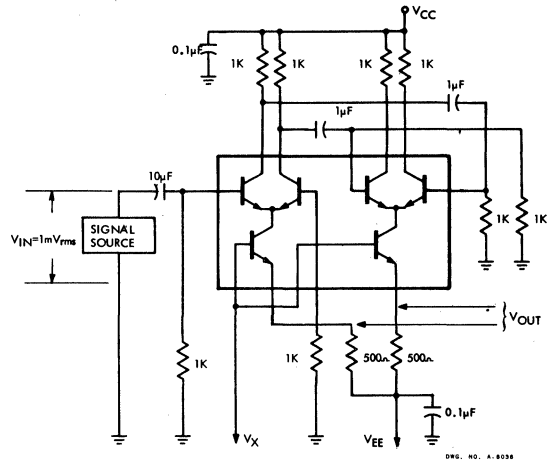
TWO-STAGE VOLTAGE GAIN

Figure 3

ULN-2081A AND ULN-2082A
GENERAL-PURPOSE HIGH-CURRENT TRANSISTOR ARRAYS

SPRAGUE TYPE ULN-2081A and ULN-2082A Transistor Arrays are comprised of seven high-current silicon NPN transistors on a common monolithic substrate. The Type ULN-2081A is connected in a common-emitter configuration and the Type ULN-2082A is connected in a common-collector configuration.

Both arrays are capable of directly driving seven segment displays and LED displays. They are ideal for a variety of other driver applications such as relay control and thyristor firing.

Type ULN-2081A and ULN-2082A are housed in 16-lead DIP plastic packages which include a separate substrate connection for maximum circuit design flexibility.

DWG. NO. A-9042B

DWG. NO. A-9043B
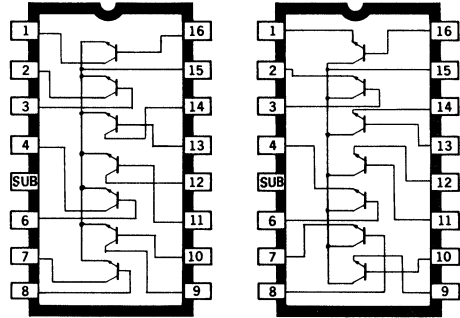
ULN-2081A   **ULN-2082A**

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (any one transistor)..500mW

(total package)..750mW

Ambient Temperature Range (operating)..$-20°C$ to $+85°C$

Individual Transistor Ratings:

Collector-to-Emitter Voltage, V_{CEO}..16V

Collector-to-Base Voltage, V_{CBO}..20V

Collector-to-Substrate Voltage, V_{CIO}..20V

Emitter-to-Base Voltage, V_{EBO}..5V

Collector Current, I_C..200mA

Base Current, I_B..20mA

NOTE:

The collector of each transistor in the Type ULN-2081A and ULN-2082A is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage so as to maintain isolation between transistors, and to provide normal transistor action. Undesired coupling between transistors is avoided by maintaining the substrate terminal (5) at either d-c or signal (a-c) ground. An appropriate bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 500\mu A$	20	80		V
Collector-Substrate Breakdown Voltage	BV_{CIE}	$I_{CI} = 500\mu A$	20	80		V
Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1mA$	16	40		V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_C = 500\mu A$	5	7		V
Forward Current Transfer Ratio	h_{FE}	$V_{CE} = 0.5V, I_C = 30mA$	30	80		
		$V_{CE} = 0.8V, I_C = 50mA$	40	85		
Base-Emitter Saturation Voltage	$V_{BE(SAT)}$	$I_C = 30mA$		0.75	1	V
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 30mA$		0.13	0.5	V
		$I_C = 50mA$		0.2	0.7	V
Collector Cutoff Current	I_{CEO}	$V_{CE} = 10V$			10	μA
	I_{CBO}	$V_{CB} = 10V$			1	μA

ULN-2083A AND ULS-2083H TRANSISTOR ARRAYS
(Five Independent NPN Transistors)

D ESIGNED for use in general purpose, medium current (to 100 mA) switching and differential amplifier applications, the ULN-2083A and ULS-2083H transistor arrays each consist of five NPN transistors on a single monolithic chip. Two transistors are matched at low currents (1 mA) making them ideal for use in balanced mixer circuits, push-pull amplifiers, and other circuit functions requiring close thermal and offset matching.

A separate substrate connection permits maximum circuit design flexibility. In order to maintain isolation between transistors and provide normal transistor action, the substrate must be connected to a voltage which is more negative than any collector voltage. The substrate terminal (pin 5) should therefore be maintained at either d-c ground or suitably bypassed to a-c ground to avoid undesired coupling between transistors.

Two package configurations are available. The Type ULN-2083A is supplied in a 16-lead dual in-line plastic package for operation over the temperature range of $-20°C$ to $+85°C$. This package is similar to
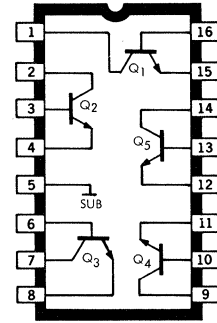
DWG. NO. A-10.232

JEDEC style MO-001AC. The Type ULS-2083H is electrically identical to the ULN-2083A but is supplied in a hermetic dual in-line package for operation over the temperature range of $-55°C$ to $+125°C$. This package conforms to the dimensional requirements of Military Specification MIL-M-38510 and can meet all of the applicable environmental requirements of Military Standard MIL-STD-883.

ABSOLUTE MAXIMUM RATINGS
at $+25°C$ Free-Air Temperature

Power Dissipation, P_D (any one transistor)...500 mW

(total package)...750 mW*

Operating Temperature Range, T_A (ULN-2083A)......................................$-20°C$ to $+85°C$

(ULS-2083H).......................................$-55°C$ to $+125°C$

Storage Temperature Range, T_S...$-55°C$ to $+150°C$

*Derate at the rate of 6.67 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS at $+25°C$ Free-Air Temperature

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 100\,\mu A$	20	60	—	V
Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_C = 1\,mA$	15	24	—	V
Collector-Substrate Breakdown Voltage	BV_{CIO}	$I_{CI} = 100\,\mu A$	20	60	—	V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 500\,\mu A$	5.0	6.9	—	V
Collector Cutoff Current	I_{CEO}	$V_{CE} = 10\,V$	—	—	10	μA
	I_{CBO}	$V_{CB} = 10\,V$	—	—	1.0	μA
Base-Emitter Voltage	V_{BE}	$V_{CE} = 3\,V, I_C = 10\,mA$	650	740	850	mV
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 50\,mA, I_B = 5\,mA$	—	400	700	mV
D-C Forward Current Transfer Ratio	h_{FE}	$V_{CE} = 3\,V, I_C = 10\,mA$	40	76	—	
		$V_{CE} = 3\,V, I_C = 50\,mA$	40	75	—	
Differential Input Offset Voltage*	V_{IO}	$V_{CE} = 3\,V, I_C = 1\,mA$	—	1.2	5.0	mV
Differential Input Offset Current*	I_{IO}	$V_{CE} = 3\,V, I_C = 1\,mA$	—	0.7	2.5	μA

*Applies only to transistors Q_1 and Q_2 when connected as a differential pair.

D-C FORWARD CURRENT TRANSFER RATIO AS A FUNCTION OF COLLECTOR CURRENT
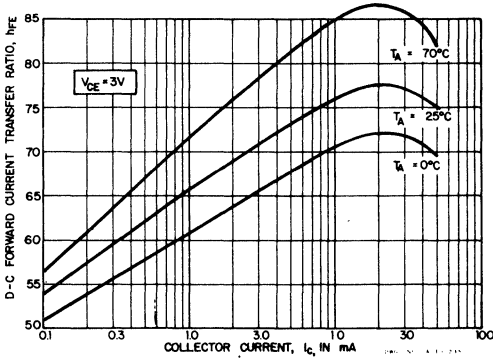
COLLECTOR-EMITTER SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT
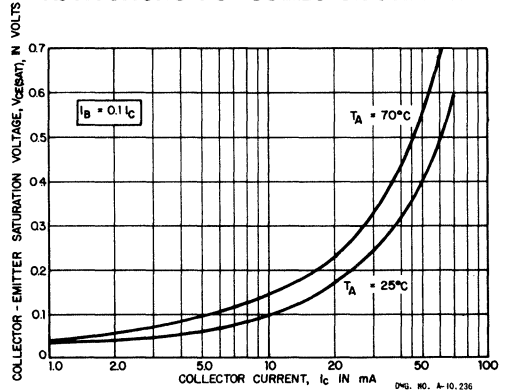
BASE-EMITTER SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT
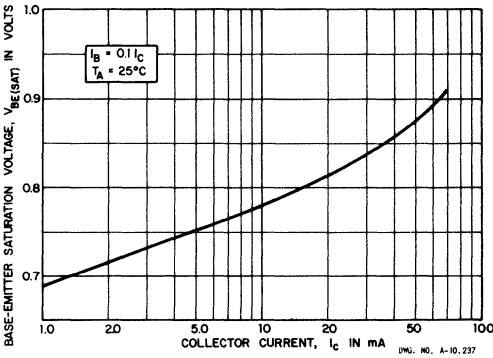
BASE-EMITTER VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT
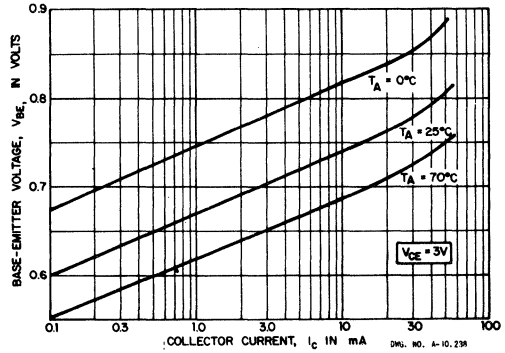
DIFFERENTIAL INPUT OFFSET VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT
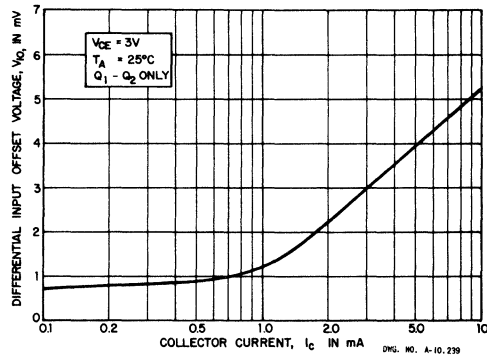
DIFFERENTIAL INPUT OFFSET CURRENT AS A FUNCTION OF COLLECTOR CURRENT

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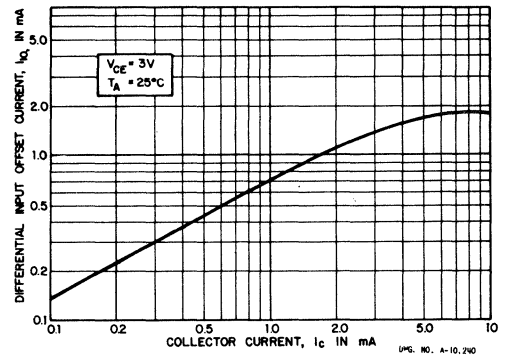
ULN-2083A-1 TRANSISTOR ARRAY

This device is a general-purpose transistor array for use in medium-current switching and differential amplifier applications. With the exception of the increased breakdown voltages shown below, Type ULN-2083A-1 is identical to Type ULN-2083A transistor array.
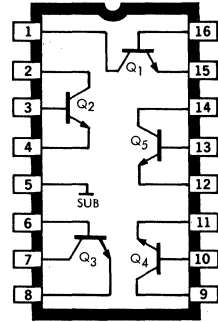
DWG. NO. A-10,232

ELECTRICAL CHARACTERISTICS at +25°C Free-Air Temperature

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Collector-Base Breakdown Voltage	BV_{CBO}	$I_c = 100 \ \mu A$	40	60	—	V
Collector-Emitter Breakdown Voltage	BV_{CEO}	$I_c = 1 \ mA$	30	—	—	V

ULN-2086A TRANSISTOR ARRAY

Type ULN-2086A general-purpose transistor array consists of five silicon NPN transistors, two of which are connected as a differential amplifier. The monolithic construction provides close electrical and thermal matching between all transistors.

With the exception of the collector cutoff current specifications listed below and the omission of guaranteed limits on input offset voltage and input offset current, Type ULN-2086A is identical to Type ULN-2046A transistor array.
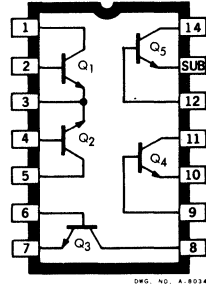
DWG. NO. A-8034

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Collector Cutoff Current	I_{CBO}	$V_{CB} = 10\,V, I_E = 0$	—	—	100	nA
	I_{CEO}	$V_{CE} = 10\,V, I_B = 0$	—	—	5.0	μA

NOTE: The substrate terminal must be tied to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

10

SERIES 2140
HIGH-PERFORMANCE QUAD CURRENT SWITCHES

FEATURES

- Variable Reference: −3 to −10 Volts
- Low Temperature Coefficient: 5 ppm/°C
- Fast Settling: 300 ns to 0.01%
- TTL/CMOS Compatible Inputs

SERIES 2140 quad current switches are high precision monolithic integrated circuits for use in digital-to-analog converters. Each device contains four logic-controlled current switches and a reference transistor. Continuously running current sources and superior thermal layout, maximize speed and accuracy by reducing transitional anomalies. Series 2140 switches accept a wide range of d-c references or an a-c reference for two-quadrant mutiplying D/A applications. Inputs may be driven from TTL, or similar sources and are independent of reference voltage level.

Type ULN-2140A switches are rated for operation over the temperature range of −20°C to +85°C; the 'A' suffix indicates a 14-pin dual in-line plastic package. Type ULS-2140H switches are rated for operation over the extended temperature range of −55°C to +125°C; the 'H' suffix indicates a dual in-line hermetic package to Military Specification MIL-M-38510. Devices in unpackaged, chip form, for use in hybrid circuit applications, are designated by changing the suffix letter from A or H to C.

On special order, hermetically sealed quad current switches with high-reliability screening to MIL-STD-883 are available by adding the suffix 'MIL' to the part number, for example, ULS-2140H-MIL. Also, on special order, devices with improved linearity and drift can be supplied.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... +18 V
              V_{EE} .... −18 V
Input Voltage, V_{IN} .... +6 V
Reference Voltage Range, V_{REF} .... −3 V to V_{EE}
Operating Temperature Range, T_A (ULN-2140A) .... −20°C to +85°C
                          (ULS-2140H) .... −55°C to +125°C
Storage Temperature Range, T_S .... −65°C to +150°C

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = +5$ to $+15$ V, $V_{EE} = -15$ V, $I_{MSB} = 1$ mA, Operational Amplifier Summing Junction Load (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits Min.	Limits Typ.	Limits Max.	Units
"0" Input Voltage	$V_{IN(0)}$		—	—	0.8	V
"1" Input Voltage	$V_{IN(1)}$		2.0	—	—	V
"0" Input Current	$I_{IN(0)}$	$V_{IN} = 0.8$ V	—	—	−1.0	μA
"1" Input Current	$I_{IN(1)}$	$V_{IN} = 2.4$ V	—	—	10	μA
Output Voltage	V_{OUT}	$R_L = 1$ kΩ		See Note		
Output Voltage Swing	ΔV_{OUT}	$R_L = 1$ kΩ, Logic = 0000 to 1111	−2.0	—		V
Output Current	I_{MSB}	Logic = 0111	2.0	1.0	—	mA
	$I_{BIT\ 2}$	Logic = 1011	1.0	0.5	—	mA
	$I_{BIT\ 3}$	Logic = 1101	0.5	0.25	—	mA
	I_{LSB}	Logic = 1110	0.25	0.125	—	mA
Settling Time		$R_L = 1$ kΩ, To 0.01%, Logic = 1000 to 0111	—	300	—	ns
Output Leakage Current	I_{OUT}	Logic = 1111	—	—	10	μA
Ref. Transistor Static Forward Current Gain	h_{FE}	$I_C = 125$ μA	100	—	—	—
Non-Linearity		Over Operating Temperature Range	—	—	0.5	%
TC of Non-Linearity		0°C to +70°C (ULN-2140 Devices)	—	—	20	ppm/°C
		−55°C to +125°C (ULS-2140 Devices)	—	—	10	ppm/°C
Scale Factor Drift		Over Operating Temperature Range	—	5.0	—	ppm/°C
Supply Current	I_{CC}	$V_{CC} = +15$ V	—	8.0	—	mA
	I_{EE}		—	−8.0	—	mA

Note: Output voltage with a resistive load will be a negative voltage.

TYPICAL APPLICATION

DWG. NO. A-10,805

* CONTACT FACTORY
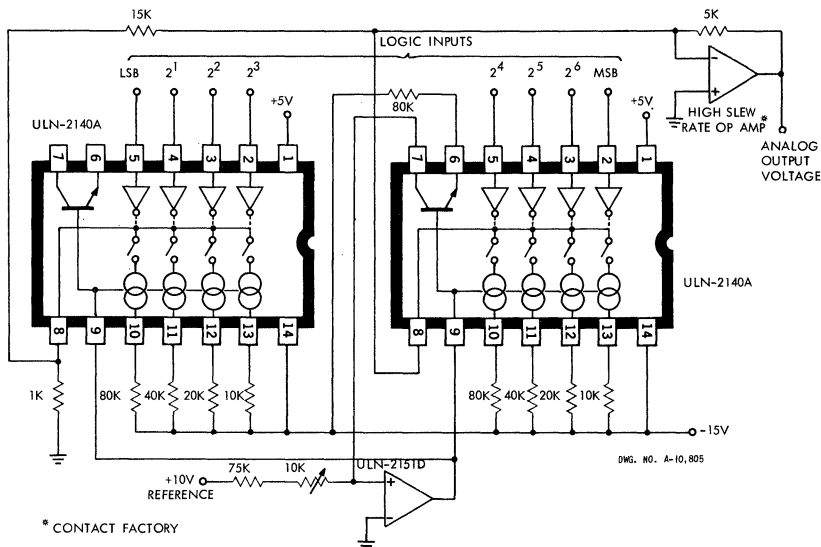
ULN-2401A AUTOMOTIVE LAMP MONITOR

FEATURES

- No Standby Power
- Completely Integral to Wiring Assembly
- Monitor 1 to 8 Lamps per Channel
- Fail-Safe
- Reverse Voltage Protected
- 14-Pin Dual In-Line Plastic Package

OFFERING SEVERAL ADVANTAGES for a lamp monitoring system, the ULN-2401A monolithic integrated circuit is versatile, easily connected, and does not affect normal lamp operation. Little additional wiring is required for installation since the system is completely integral to the wiring assembly.

The ULN-2401A electronic lamp monitor was specifically designed for application in the severe automotive environment. Lateral PNP transistors provide high-frequency noise immunity and differential transient voltage protection. Reverse voltage protection, internal voltage regulators, and temperature compensation are all incorporated in the design. A failure within the device will not affect lamp operation. As a quad comparator, the ULN-2401A can also be used to monitor multiple low-voltage power supplies or, with appropriate sensors, industrial processes.

This lamp monitor operates by sensing the voltage drop in the wiring (50 to 100 mV) for each lamp circuit. If any of the four comparators sees a differential input voltage of greater than 26 mV, a failure lamp is turned on. Lamp and wiring tolerances causing differential input voltages of up to 7 mV are permitted. Each comparator is capable of monitoring a mixture of one to eight similar lamps. No standby power is required because the operating voltage is obtained from the sense leads and is energized only when the lamps are turned on.
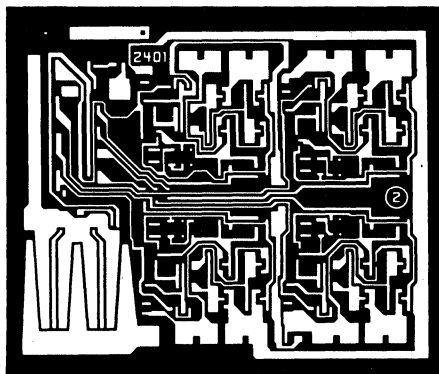
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .... 16 V
Peak Reverse Voltage (30 s) .... 6.0 V
                 (0.1 s) .... 30 V
Output Current, I_{OUT} .... 500 mA
Operating Temperature Range, T_A .... −35°C to +70°C
Storage Temperature Range, T_S .... −65°C to +150°C

EQUIVALENT LOGIC CIRCUITRY
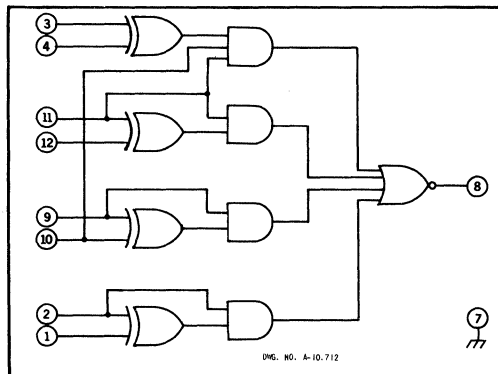
DWG. NO. A-10.712

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Operating Voltage Range	V_{CC}		10	13	16	V
Output Saturation Voltage	$V_{OUT(ON)}$	$V_{CC} = 10$ V, $\Delta V_{IN} = 26$ mV	—	—	2.2	V
		$V_{CC} = 13$ V, $\Delta V_{IN} = 26$ mV	—	—	2.4	V
		$V_{CC} = 16$ V, $\Delta V_{IN} = 26$ mV	—	—	2.6	V
Output Leakage Current	$I_{OUT(OFF)}$	$V_{CC} = 16$ V, $\Delta V_{IN} = 0$ mV	—	—	6.0	mA
		$V_{CC} = 16$ V, $\Delta V_{IN} = 7$ mV	—	—	10	mA
		$V_{CC} = 16$ V, $\Delta V_{IN} = 0$ mV (all inputs)	—	—	15	mA

NOTE: Electrical characteristics (unless otherwise specified) apply to any one pair of comparator inputs (pins 1 & 2, or 9 & 10, or 11 & 12) with all remaining comparator inputs (including pins 3 & 4) open-circuited. To test the comparator at pins 3 & 4, pins 9, 10, 11 & 12 must be connected to V_{CC}. In application, pins 10 and 11 must both be at or near V_{CC} for the comparator at pins 3 & 4 to be operative.

TEST CIRCUIT
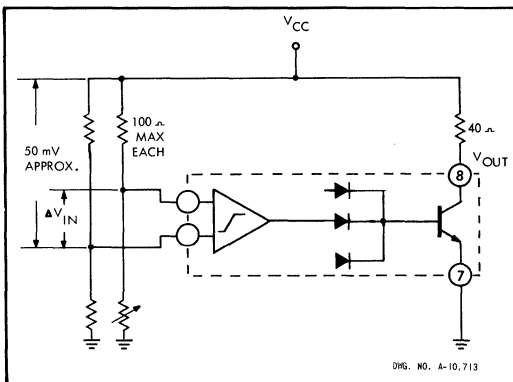
DWG. NO. A-10,713

SCHEMATIC

DWG.NO. B-1384

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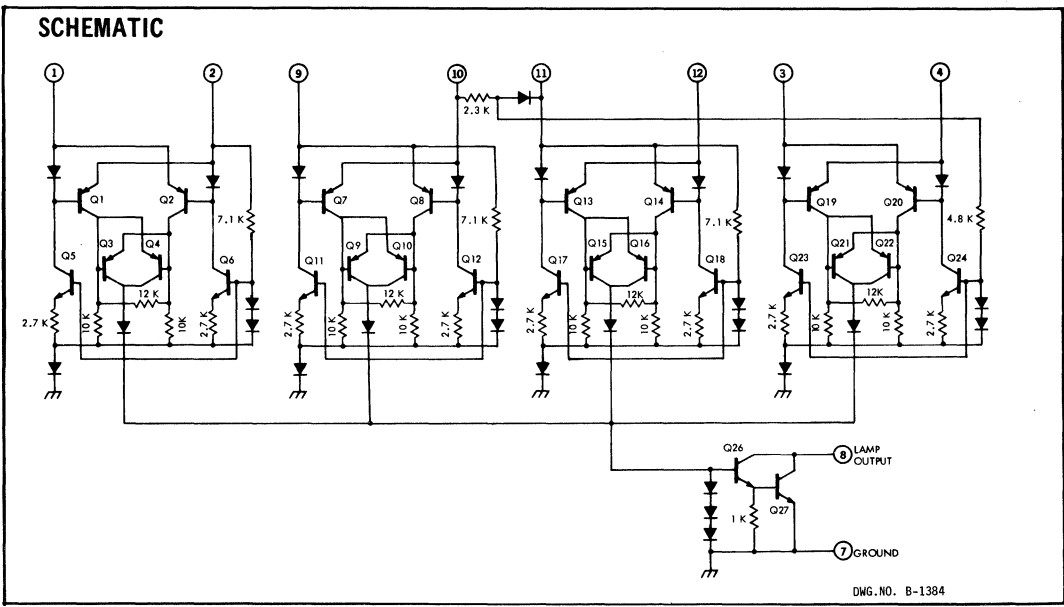
ULN-2429A FLUID DETECTOR

FEATURES

- High Output Current
- A-C or D-C Output
- Single-Wire Probe
- Low External Parts Count
- Internal Voltage Regulator
- Reverse Voltage Protection
- 14-Pin Dual In-Line Plastic Package

PRIMARILY DESIGNED for use as an auto-motive low coolant detector, the ULN-2429A monolithic bipolar integrated circuit is ideal for detecting the presence or absence of many different types of liquids in automotive, home, or industrial applictions. Especially useful in harsh environments, reverse voltage protection, internal voltage regulation, temperature compensation, and high-frequency noise immunity are all incorporated in the design.

A simple probe, immersed in the fluid being monitored, is driven with an a-c signal to prevent plating problems. The presence, absence, or condition of the fluid is determined by comparing the loaded probe resistance with an internal (pin 8) or external (pin 6) resistance. Typical conductive fluids which can be sensed are tap water, sea water, weak acids and bases, wet soil, wine, beer, and coffee. Non-conductive fluids include most petroleum products, distilled water, dry soil, and vodka. The probe can be replaced with any variable-resistance element such as a photodiode or photoconductive cell, rotary or linear position sensor, or thermistor for detecting solids, non-conducting liquids, gases, etc.

The high-current output is typically a square wave signal for use with an LED, incandescent lamp, or loudspeaker. A capacitor can be connected (pin 12) to provide a d-c output for use with inductive loads such as relays and solenoids.
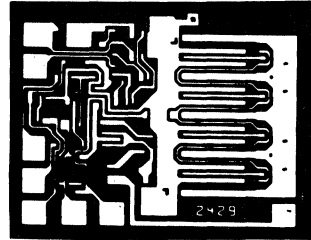
The ULN-2429A is rated for operation with a load voltage of up to 30 volts. Selected devices, for operation up to 50 V are available as the ULN-2429A-1. In all other respects, the ULN-2429A and the ULN-2429A-1 fluid detectors are identical.

These devices are furnished in an improved 14-lead dual in-line plastic package with a copper alloy lead frame for superior thermal characteristics. However, in order to realize the maximum current-handling capability of these devices, both of the output pins (1 and 14) and both ground pins (3 and 4) should be used.
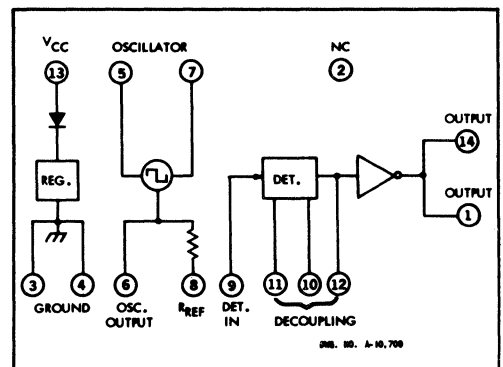
FUNCTIONAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} (continuous) . . . . +16 V, −50 V

(1 hr. at +25°C) . . . . +24 V

(10 μs) . . . . +50 V

Output Voltage, V_{OUT} (ULN-2429A) . . . . +30 V

(ULN-2429A-1) . . . . +50 V

Output Current, I_{OUT} (continuous) . . . . 700 mA

(1 hr. at +25°C) . . . . 1.0 A

Package Power Dissipation, P_D . . . . 1.33 W*

Operating Temperature Range, T_A . . . . −40°C to +85°C

Storage Temperature Range, T_S . . . . −65°C to +150°C

*Derate at the rate of 16.67 mW/°C above T_A = +70°C.

ELECTRICAL CHARACTERISTICS at $T_A = -25°C$, $V_{CC} = V_{OUT} = +12$ V
(unless otherwise specified)

Characteristic	Symbol	Test Pin	Test Conditions	Limits			
				Min.	Typ.	Max.	Units
Supply Voltage Range	V_{CC}	13	—	10	—	16	V
Supply Current	I_{CC}	13	$V_{CC} = +16V$	—	—	10	mA
Oscillator Output Voltage	V_{osc}	6	$R_L = 18$ kΩ	—	3.0	—	V_{PP}
Output ON Voltage	V_{OUT}	1,14	$R_L \geq 30$ kΩ, $I_{OUT} = 500$ mA	—	0.9	1.5	V
Output OFF Current	I_{OUT}	1,14	$R_L \leq 10$ kΩ, $V_{OUT} = V_{OUT}$(max)	—	—	100	μA
Oscillator Frequency	f_{osc}	6	$R_L = 18$ kΩ	—	2.4	—	kHz

TEST CIRCUIT
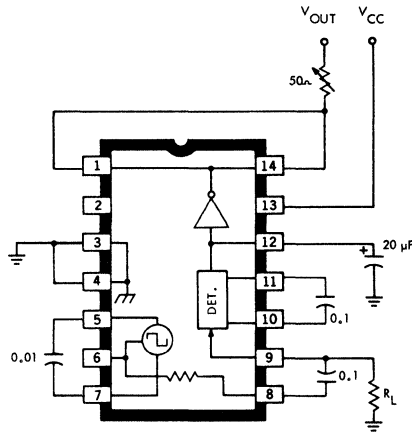
DWG. NO. A-10.707

10

CIRCUIT SCHEMATIC

DWG. NO. A-10,825

TYPICAL APPLICATIONS

HIGH-RESISTANCE (AIR)
TURNS OUTPUT LAMP ON.

DWG. NO. A-10.708

HIGH-RESISTANCE (AIR)
TURNS OUTPUT LAMP OFF.

DWG. NO. A-10.711

10—22
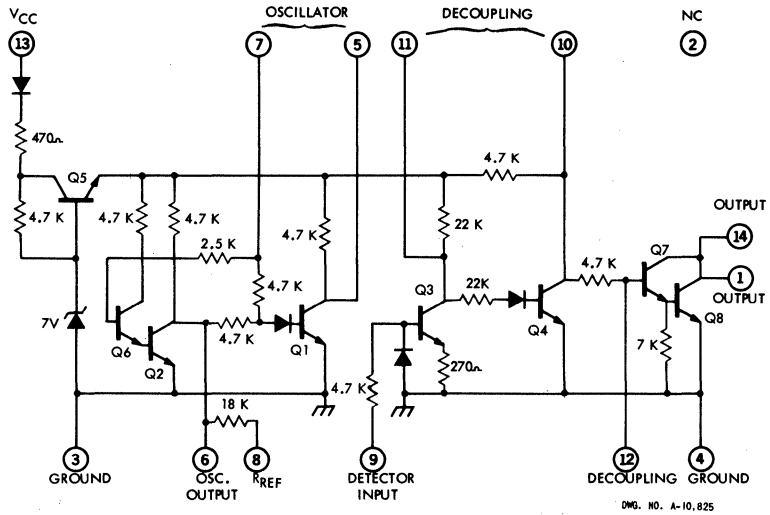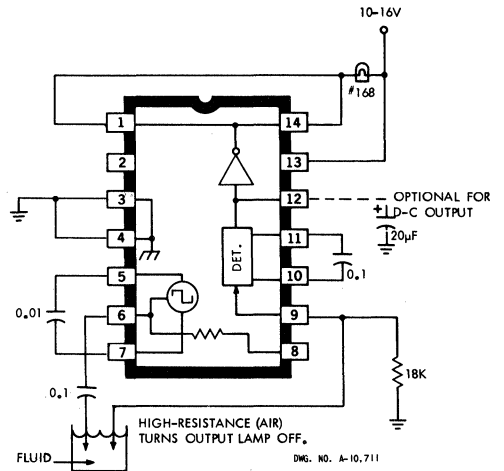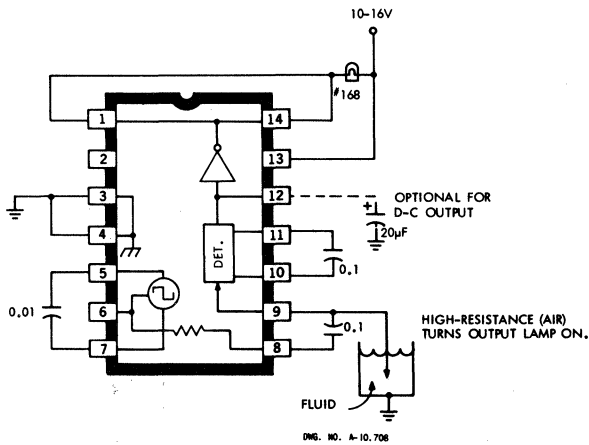
ULN-2430M TIMER

FEATURES

- Microseconds to Minutes
- Temperature Compensated
- 400 mA Output
- 8-Pin Dual In-Line Plastic Package
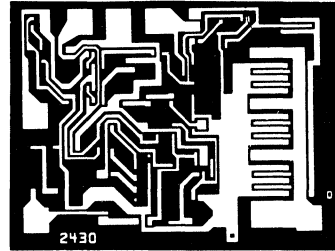
PROVIDING time delays from several microseconds to approximately 10 minutes, the ULN-2430M timer was originally designed for use as a rear window heater timer in automotive applications. In typical system designs, this device will meet all of the stringent automotive environmental and transient requirements, including "load dump". The rugged design, the high output current rating, and an internal voltage regulator and reference allow the ULN-2430M timer to be used in many industrial applications.

ABSOLUTE MAXIMUM RATINGS

Regulator Current, I_{REG} . . . . 15 mA
Latch Current, I_4 . . . . 3 mA
Output Current, I_{OUT} . . . . 400 mA
Package Power Dissipation, P_D . . . . 330 mW*
Operating Temperature Range, T_A . . . . −40°C to +85°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

*Derate at the rate of 4.2 mW/°C above T_A = +70°C.
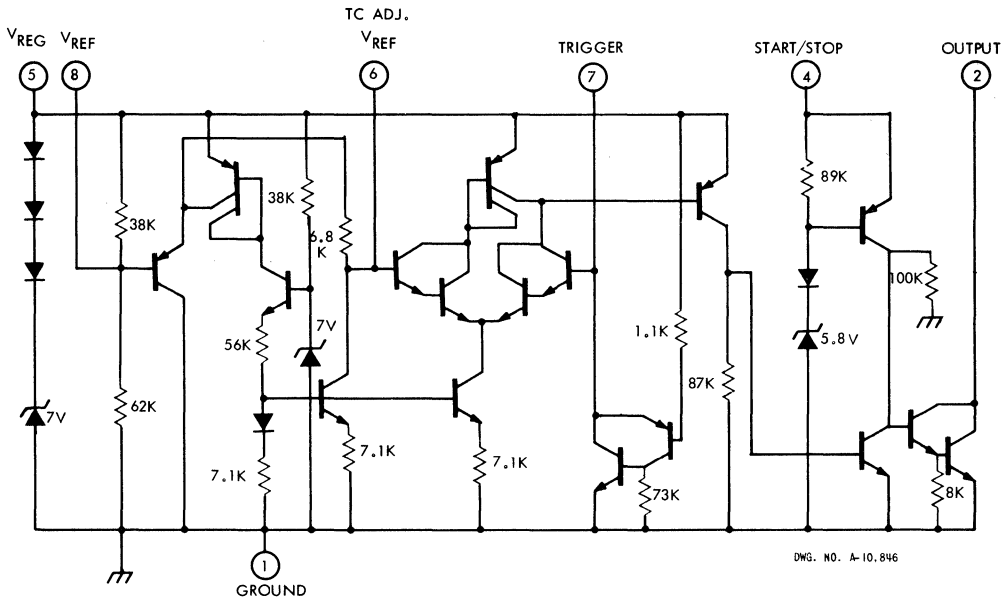
DWG. NO. A-10,846

10

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$ (unless otherwise noted), Fig. 1

Characteristic	Test Pin	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Operating Voltage Range			10	—	16	V
Regulator Voltage	5		8.4	9.0	10.1	V
Output Breakdown Voltage	2	$I_{LEAK} = 100\ \mu A$	30	—	—	V
Output Saturation Voltage	2	$I_{OUT} = 400\ mA$	—	—	2.5	V
		$I_{OUT} = 250\ mA$	—	—	1.3	V
Latch Voltage	4	Over Op. Temp. Range	5.5	7.0	8.0	V
Trigger Threshold	7	V_7/V_5	0.60	0.63	0.67	
Reference	8	V_8/V_5	0.58	0.63	0.68	
Temp. Coeff. of Trigger Threshold	7		−2.0	—	−4.0	mV/°C
Trigger Input Current	7		—	20	200	nA
Capacitor Discharge Time	7	$C_1 = 220\ \mu F,\ \pm 10\%$	—	—	2.0	s
Supply Current	5	$V_{CC} = 16\ V$	—	—	10	mA

CIRCUIT OPERATION

The basic system shown in Figure 1 provides power for the timer after the momentary closure of the "rear window heater switch" S_1. Momentary closure provides an input to pin 4 which turns ON the output driver, energizes the relay, and (through the relay contacts) provides power to the timer and the heater element. Waveforms are shown in Figure 2.

The output remains ON, supplying power to the heater until $V_7 = 62\%\ V_5$, which occurs at time $t = R_1 \times C_1$. The time delay can be adjusted from several microseconds to approximately 10 minutes by the choice of R_1 and C_1. When $t = R_1 \times C_1$, the comparator changes state and the relay de-energizes, returning the circuit to the quiescent condition.

Timing accuracy is primarily a function of capacitor leakage for long time delays. Hard switching of the comparator necessitates low input bias currents on the comparator and low capacitor leakage current. The worst case comparator input is 200 nA and the charge current at $V_7 = 62\%\ V_5$ is approximately $1.7\ \mu A$ for $R_1 = 2\ M\Omega$. For these reasons, it is recommended that R_1 not exceed 2 MΩ and C_1 leakage be less than 500 nA.

Diode D_1 and the circuitry associated with pin 4 provide start-stop capability for the timer. When the voltage at pin 4 is larger than 8 V timing is initiated. When less than 5.5 V, timing is stopped. Transient protection against load dump and other automotive environmental hazards is provided by the integrated circuit design and discrete components Z_1, C_2, R_3, R_4, and D_1.

TYPICAL APPLICATION
(Figure 1)

HEATER
SW
S_1
IGN
SW.
1K
D_1
R_2
75Ω
BALLAST RESISTOR
BATTERY

REAR
WINDOW
HEATER
R_3
1K
R_4
4.7K
65Ω
±5Ω

C_2
40 μF
10 V.
5
4
2
Z_1
24 VOLT
1 WATT

9V
62%
VCC
5V 8V

R_1
2M

7
C_1
220 μF
16 V
1

DWG. NO. A-10.845

TIMER WAVEFORMS

V_4
11.7 V
0

V_5
9.0 V
0

V_7
5.7V
0

I_2
0

$t = R_1 \times C_1$

DWG. NO. A-10.844

ULN-2435A, ULN-2445A, AND ULN-2455A AUTOMOTIVE LAMP MONITORS

FEATURES

- No Standby Power
- Integral to Wiring Assembly
- Fail-Safe
- Reverse Voltage Protected
- Internal Transient Protection
- Dual In-Line Plastic Packages

CAPABLE of monitoring all types of automotive lamps, Type ULN-2435A, ULN-2445A, and ULN-2455A lamp monitors provide multiple LED outputs to pinpoint the area in which a lamp has failed. Types ULN-2435A and ULN-2445A feature an additional output that triggers an alarm if any of the comparators detects a lamp failure. This output can be used to drive an audible signaling device or centrally located warning indicator.

The Type ULN-2435A lamp monitor has interconnected comparator ouputs and logic to monitor the ignition circuit and fuses, making it uniquely applicable to automotive applications. Type ULN-2445A is similar, but has no interconnected comparators. Type ULN-2455A is a general-purpose quad comparator that can be used to monitor automotive lamps, multiple low-voltage power supplies, or, with appropriate sensors, industrial processes.

Installation and operation of these quad lamp monitors has no effect on normal lamp operation. Comparators sense the normal voltage drop in the lamp wiring (approximately 20 mV) for each of the monitored lamp circuits. Little additional wiring is necessary for installation because the system can be completely integral to the wiring assembly. No standby power is required: The operating voltage is obtained from the sense leads; the system is energized only when the lamps are turned ON.

All three integrated circuits are designed for use in the severe automotive environment. Lateral PNP transistors provide high-frequency noise immunity and differential transient-voltage protection. Reverse voltage protection, internal regulators, and temperature compensation are all embodied in the circuit design. A failure within the device will not affect lamp operation.

Types ULN-2435A and ULN-2445A are supplied in 18-pin dual in-line plastic packages. The Type ULN-2455A lamp monitor is supplied in a 14-pin dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Supply Voltage, V_{CC} . . . . 30 V
Peak Supply Voltage, V_{CC} (0.1 s) . . . . 80 V
Peak Reverse Voltage, V_R . . . . 30 V
Output Current, I_{OUT} . . . . 35 mA
Package Power Dissipation, P_D (ULN-2435/45A) . . . . . . 2.3 W*
(ULN-2455A) . . . . 2.0 W**
Operating Temperature Range, T_A . . . . −40°C to +85°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

*Derate at the rate of 18.18 mW/°C above T_A = +25°C.
**Derate at the rate of 16.67 mW/°C above T_A = +25°C.

PRINCIPLE OF OPERATION

Operation of these lamp monitors is similar to that of a simple bridge circuit in which the top two legs of the bridge are formed by the wiring assembly resistance or discrete low-value resistors. The bottom legs of the bridge are the monitored lamps. Four differential amplifier circuits sense the voltage drops in the wiring assemblies (approximately 20 mV) for each of the lamp circuits. When the system detects a difference in voltage due to an open filament, the appropriate output driver is turned ON.

Sprague Electric Technical Paper TP 81-7 discusses the requirements of automotive lamp monitoring systems and presents a more detailed description of the operation of these differential sense amplifiers (page 10-56).

BASIC BRIDGE MONITORING SYSTEM
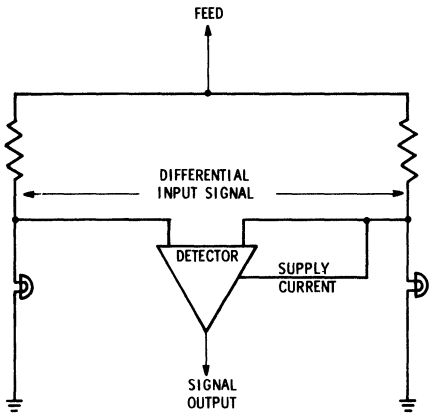
Dwg. No. A-11,473A

TYPICAL SWITCH CHARACTERISTICS
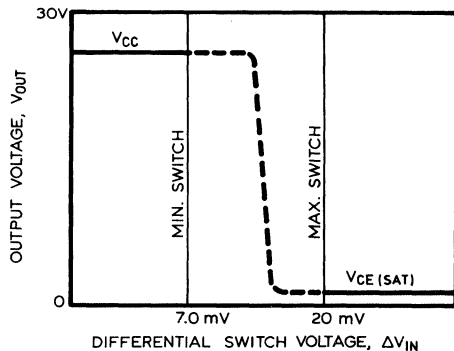
Dwg. No. A-12,187

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{CC} = V_{IN} = 10 to 16 V (unless otherwise shown)

Characteristic	Test Pins		Test Conditions	Limits			Units
	ULN-2435/45A	ULN-2455A		Min.	Typ.	Max.	
Output Leakage Current	1, 7, 10, 13, 15, 16	1, 4, 8, 11	V_{OUT} = 80 V, $\triangle V_{IN}$ < 7 mV	—	—	100	µA
Output Saturation Voltage	1, 7, 10, 13, 15, 16	1, 4, 8, 11	I_{OUT} = 5 mA, $\triangle V_{IN}$ > 20 mV	—	0.8	1.0	V
			I_{OUT} = 30 mA, $\triangle V_{IN}$ > 20 mV	—	1.4	2.0	V
Differential Switch Voltage	2-3, 8-9, 11-12, 17-18	2-3, 5-6, 9-10, 12-13	Absolute Value $V_{(2)} - V_{(3)}$	7.0	13	20	mV
Input Current	4	NA	V_{IN} = V_{CC} = 16 V	—	—	500	µA
	5	NA	V_{IN} = V_{CC} = 16 V	—	—	15	mA
	6	NA	V_{IN} = 0 V, V_{CC} = 16 V	—	—	− 1.0	mA
	2, 8, 11, 17	2, 5, 9, 12	$\triangle V_{IN}$ = $V_{(2)} - V_{(3)}$ = + 30 mV	150	300	800	µA
	3, 9, 12, 18	3, 6, 10, 1 3	$\triangle V_{IN}$ = $V_{(2)} - V_{(3)}$ = − 30 mV	1.0	2.5	4.0	mA

10

ULN-2435A
FUNCTIONAL BLOCK DIAGRAM
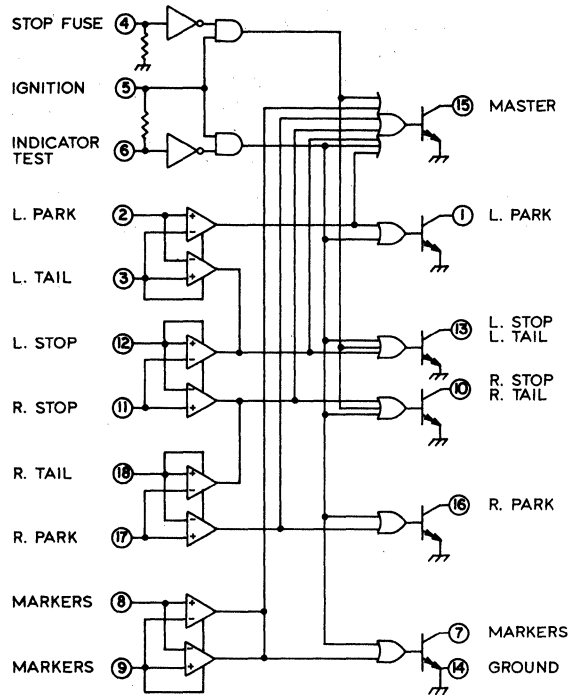
Dwg. No. A-12,031A

ULN-2435A and ULN-2445A TRUTH TABLES

CONDITIONS	INPUT PINS							OUTPUT PINS											
								ULN-2435A						ULN-2445A					
	2/3	8/9	11/12	17/18	6	4	5	1	7	10	13	15	16	1	7	10	13	15	16
Normal	=	=	=	=	0	H	X	H	H	H	H	H	H	H	H	H	H	H	H
L. Park Lamp Failure	>	=	=	=	0	H	X	L	H	H	H	L	H	L	H	H	H	L	H
L. Tail Lamp Failure	<	=	=	=	0	H	X	H	H	H	L	L	H	H	H	H	H	L	H
Marker Lamp Failure	=	>	=	=	0	H	X	H	L	H	H	L	H	H	L	H	H	L	H
Marker Lamp Failure	=	<	=	=	0	H	X	H	L	H	H	L	H	H	L	H	H	L	H
R. Stop Lamp Failure	=	=	>	=	0	H	X	H	H	L	H	L	H	H	H	L	H	L	H
L. Stop Lamp Failure	=	=	<	=	0	H	X	H	H	H	L	L	H	H	H	H	L	L	H
R. Park Lamp Failure	=	=	=	>	0	H	X	H	H	H	H	L	L	H	H	H	H	L	L
R. Tail Lamp Failure	=	=	=	<	0	H	X	H	H	L	H	L	H	H	H	H	H	L	H
Stop Lamp Fuse Failure	=	=	=	=	0	L	H	H	H	L	L	L	H	H	H	L	L	L	H
Indicator Lamp Test	X	X	X	X	L	X	H	L	L	L	L	L	L	L	L	L	L	L	L

= — Less than 7 mV offset between a pair of input pins
> — Greater than +20 mV differential between a pair of input pins [$V_{(2)} - V_{(3)}$]
< — Greater than −20 mV differential between a pair of input pins [$V_{(2)} - V_{(3)}$]
H — V_{CC}
L — V_{SAT} (outputs) or GROUND (inputs)
0 — Open or V_{CC}
X — Irrelevant

ULN-2445A FUNCTIONAL BLOCK DIAGRAM

Dwg. No. A-12,032A
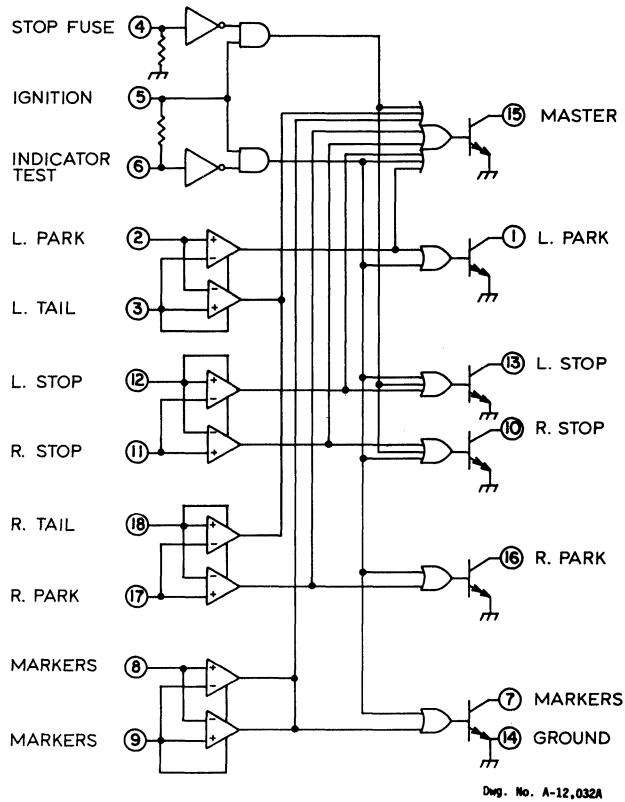
ULN-2455A
FUNCTIONAL BLOCK DIAGRAM

Dwg. No. A-12,033A

10
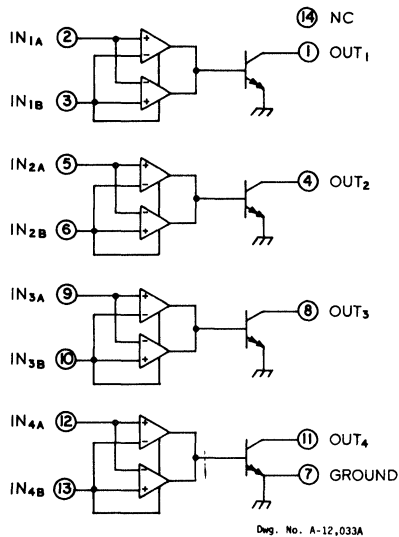
TYPICAL APPLICATIONS

AUTOMOTIVE LAMP MONITOR

Dwg. No. B-1513A

$$R \geq \frac{0.020}{I_{LAMP}}$$

QUAD LAMP MONITOR

$$R \geq \frac{0.020}{I_{LAMP}}$$

Dwg. No. A-12,035A
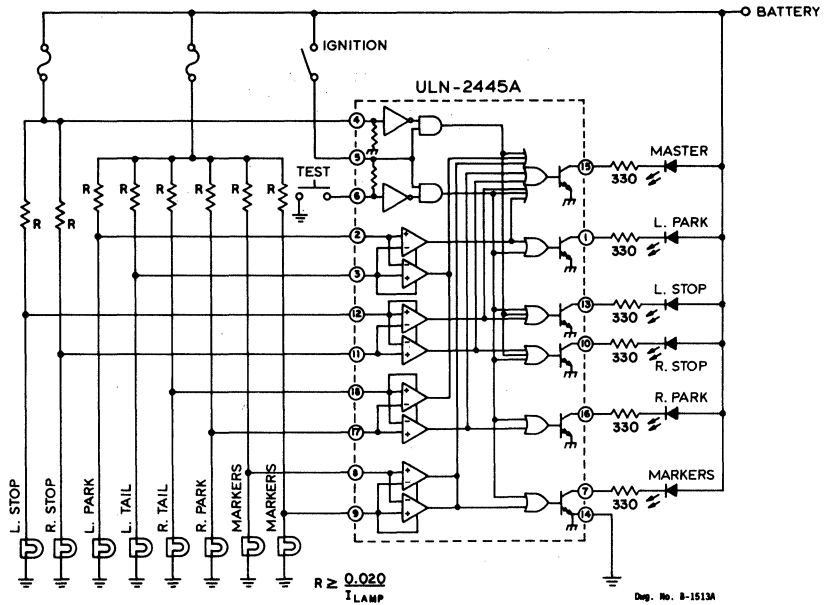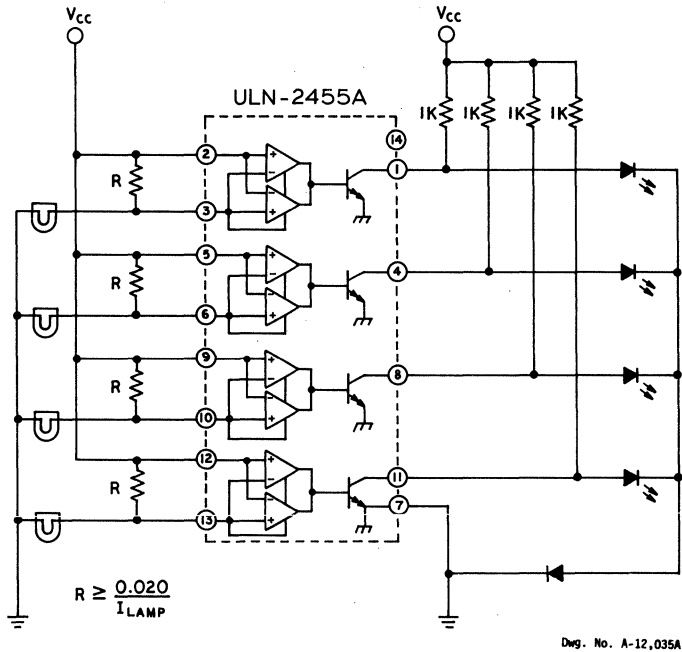
TYPICAL APPLICATIONS (Continued)

POWER SUPPLY SUPERVISORY CIRCUIT

VOLTAGE FOLLOWER SUPPLIES
DETECTOR OPERATING CURRENT
$V_{OFFSET} \ll V_{SWITCH}$

$$R_1 = \frac{R_2 \, (V_{IN} - V_{REF})}{V_{REF}}$$

$$R_S = \frac{V_{SWITCH} \, (R_1 \| R_2)(R_1 + R_2)}{(\Delta V_{IN} \cdot R_2) - V_{SWITCH} \, (R_1 + R_2)}$$

IF $V_{REF} = 10$ V
       $V_{IN} = 15$ V
       $R_2 = 15$ kΩ

THEN $R_1 = 7.5$ kΩ

IF $\Delta V_{IN} = 250$ mV
    $V_{SWITCH} = 13$ mV

THEN $R_S = 423\,\Omega$

Dwg. No. B-1524
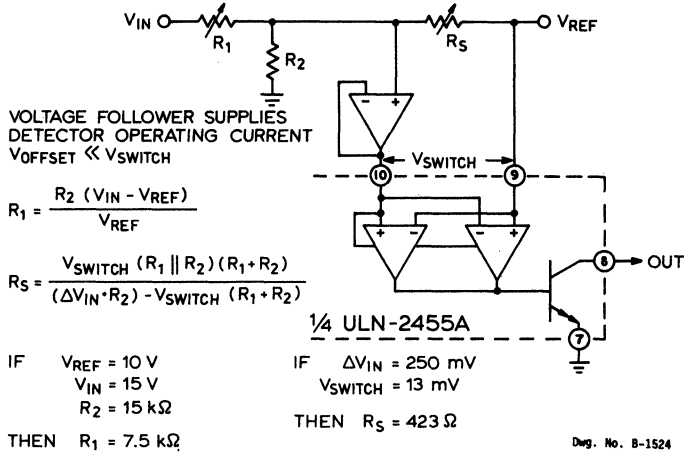
SIMPLIFIED SCHEMATIC
(One of 4 differential
sense amplifiers)

TO MASTER INDICATOR DRIVER

Dwg.No. A-12,036

10
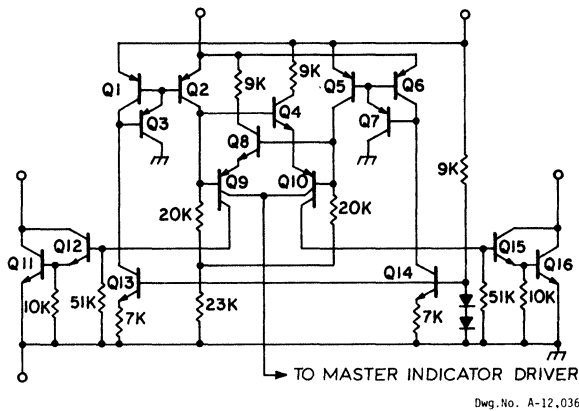
ULN-3310D AND ULN-3310T PRECISION LIGHT SENSORS

FEATURES

- Two-Terminal Operation
- Linear Over a Wide Range
- Precalibrated
- Wide Operating-Voltage Range
- High Output

DIRECT REPLACEMENTS for photocells and phototransistors, Type ULN-3310D and ULN-3310T Precision Light Sensors are two-terminal monolithic integrated circuits that linearly convert light level into electrical current. The light-controlled current sources are linear over a wide range of supply voltages and light levels and require no external calibration.

Each Precision Light Sensor (PLS) consists of a photodiode and a calibrated current amplifier. The design of the amplifier allows derivation of its supply current from the same terminal as the photodiode cathode and the amplifier output. Since this supply current is a linear function of the photodiode current, it acts as part of the signal current. Each PLS is calibrated during manufacture for an output current of 40 μA at 100 μW/cm² at 880 nm.
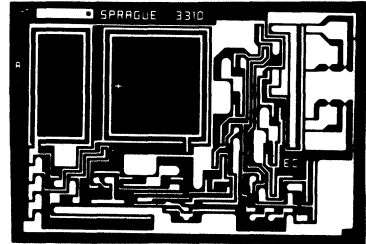
Type ULN-3310D is furnished in a hermetically sealed metal package with glass end cap conforming to JEDEC outline TO-52 (TO-206AC). Type ULN-3310T is supplied in an inexpensive clear plastic package. Both devices are rated for operation over the temperature range of −40°C to +70°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... 24 V
Operating Temperature Range .... −40°C to +70°C
Storage Temperature Range
        (ULN-3310D) .... −55°C to +150°C
        (ULN-3310T) .... −55°C to +110°C

FUNCTIONAL BLOCK DIAGRAM
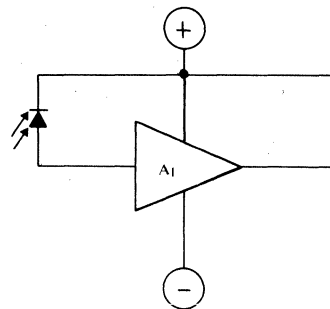
Dwg. No. A-11,991

APPLICATIONS INFORMATION

Type ULN-3310D and ULN-3310T precision light sensors can be used to replace several types of light sensors:

Photocells exhibit a change in resistance proportional to light intensity. However, they are highly inaccurate. They exhibit light memory, which makes their response dependent on the previous light level.

Phototransistors exhibit no light memory, but show as much as 50% variation in sensitivity among parts of the same type due to process and beta variations. Output current as a function of light level is linear only over a very small range.

Photodiodes have an output current that is a linear function of illumination, but the output is very small. The output current is typically in the range of tens of nanoamperes. These devices also show wide unit-to-unit sensitivity variations.

Sprague Electric precision light sensors are two-terminal replacements for photocells, phototransistors, and photodiodes. They are internally calibrated, have relatively high output currents, and are linear over a very wide range of light levels. Low-level amplifiers and adjustable controls can be eliminated. The ULN-3310D/T Precision Light Sensors are also ideal for use in arrays where matched characteristics are often required. Unpackaged chips are available on special order.

Both the hermetically sealed Type ULN-3310D sensor, and the low-cost Type ULN-3310T plastic-encapsulated sensor, are cost-effective solutions to precise light-sensing or light-measurement applications.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, V_{cc} = 12 V

Characteristic	Limits			
	Min.	Typ.	Max.	Units
Initial Accuracy at 100 μW/cm^2	—	—	±5.0	%
Sensitivity	380	400	420	nA/μW/cm^2
Operating Voltage Range	2.7	12	24	V
Output Linearity, 10 to 10k μW/cm^2	—	—	±5.0	%
Dark Current	—	—	100	nA
Power Supply Rejection, $(\Delta I_0/I_0)/\Delta V$	40	50	—	dB
Temperature Coefficient of Sensitivity	—	3500	—	ppM/°C

NOTE: Light source is an infrared LED with a peak output wavelength of 880 nm.

10

TYPICAL CHARACTERISTICS

RELATIVE SPECTRAL RESPONSE
AS A FUNCTION OF WAVELENGTH OF LIGHT

Dwg. No. A-12,135A
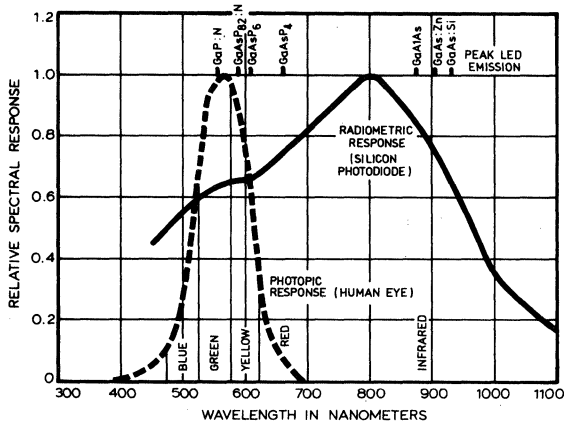
OUTPUT CURRENT
AS A FUNCTION OF ILLUMINANCE

Dwg. No. A-12,136A
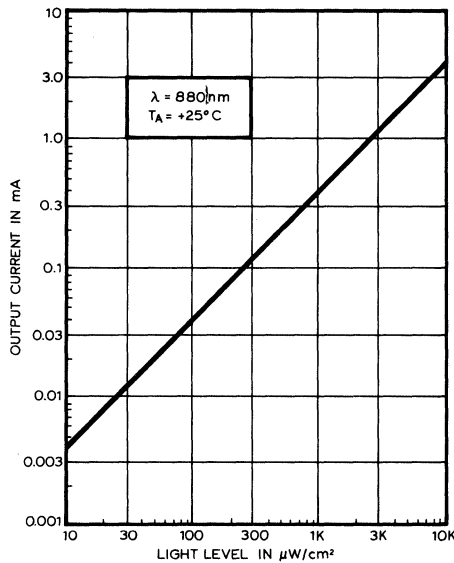
PROPAGATION DELAY
AS A FUNCTION OF ILLUMINANCE

Dwg. No. A-12,138A

OUTPUT CURRENT
AS A FUNCTION OF SUPPLY VOLTAGE

Dwg. No. A-12,137A
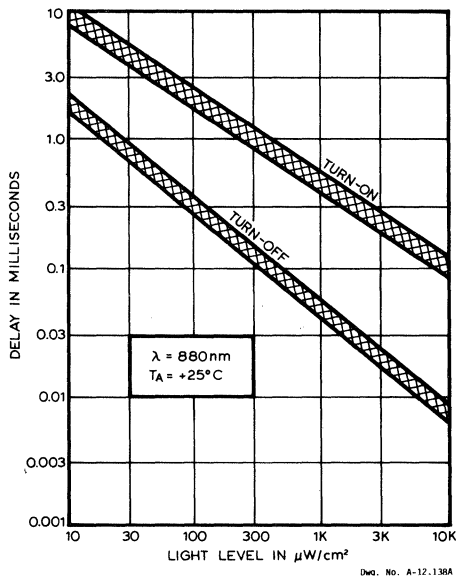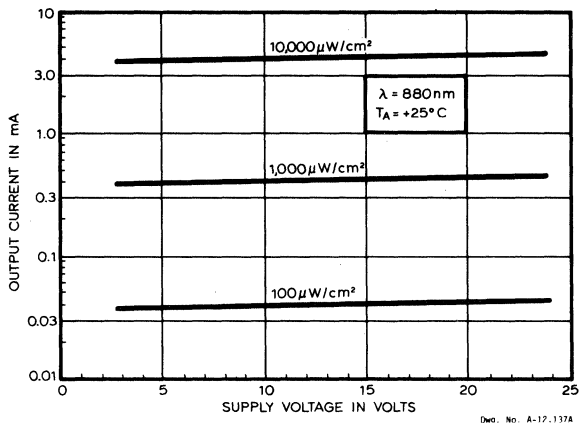
TYPICAL APPLICATIONS

Figure 1 shows a Type ULN-3310D or ULN-3310T integrated circuit replacing a photocell or phototransistor for the precise detection of a light level. Use of the precision light sensor eliminates the need for external calibration because it is calibrated to an initial accuracy of better than 5% during manufacture.
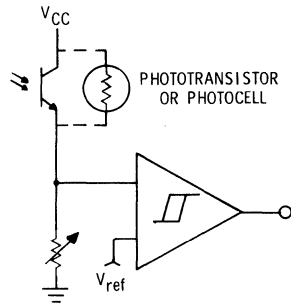
DWG. NO. A-11,808

Figure 1A
LIGHT-LEVEL DETECTOR
REQUIRING EXTERNAL CALIBRATION
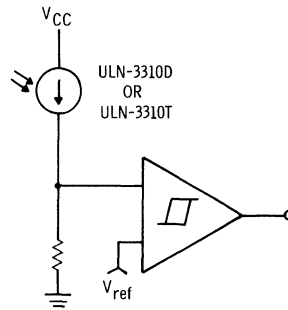
DWG. NO. A-11,809

Figure 1B
LIGHT-LEVEL DETECTOR USING PLS

In Figure 2, two precision light sensors are used in a differential config-uration to detect the edge of an object. When the light level on the first sensor is half of that on the second, the circuit switches. This circuit operates over a wide range of ambient light levels. No external calibration is required.

10

Dwg. No. A-11,995

Figure 2
DIFFERENTIAL EDGE DETECTOR

SCHEMATIC

Dwg. No. A-11,996

ULN-3310D

SENSOR-CENTER LOCATION

0.008" ± 0.010"
(0.20 mm ± 0.25 mm)

PHOTO-SENSITIVE AREA,
0.041" Dia. (1.04 mm)

0.009" ± 0.010"
(0.23 mm ± 0.25 mm)
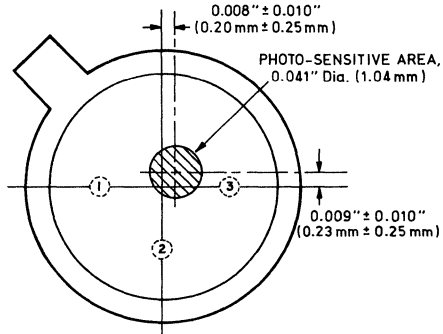
Dwg. No. A-11,993A

ULN-3310T

RELATIVE RESPONSE
AS A FUNCTION OF THE ANGLE OF INCIDENCE

RELATIVE RESPONSE

1.0
0.9
0.8
0.7
0.6

100 80 60 40 20 0 20 40 60 80 100

INCIDENT ANGLE, θ IN DEGREES

$\theta = 0^{\circ}$
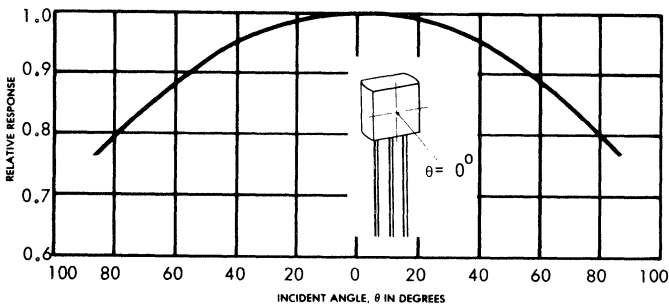
Dwg. No. A-12,134

SENSOR-CENTER LOCATION

PHOTO-SENSITIVE AREA,
0.041" Dia. (1.04 mm)

Center on PIN 2 within
±0.010" (0.254mm)

0.130" (3.30 mm)
0.110" (2.79 mm)

1   2   3

Dwg. No. A-11,994B

10
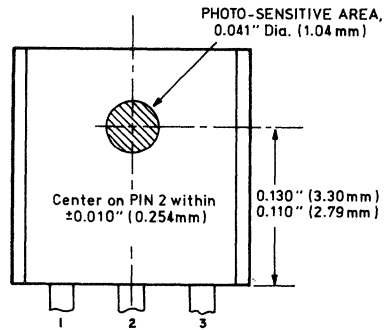
ULN-3330D, ULN-3330T, AND ULN-3330Y OPTOELECTRONIC SWITCHES

FEATURES

- Photodiode with:
  On-Chip Amplifier
  On-Chip Level Detector
  On-Chip Power Driver
  On-Chip Regulator
- Operation to 30 kHz
- Plastic or Hermetic Package
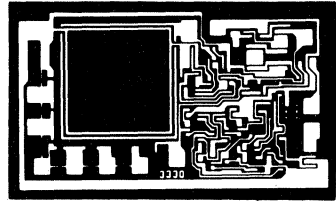
PROVIDING complete light detection and low-level signal-processing circuitry in a single 3-lead package, Type ULN-3330D, ULN-3330T, and ULN-3330Y optoelectronic switches are monolithic integrated circuits containing a photodiode, low-level amplifier, level detector, output power driver, and voltage regulator. The three devices are cost-effective solutions to light-sensing consumer or industrial applications. They require no external components for operation.

The optoelectronic switches typically turn ON as illumination of the photodiode falls below 55 μW/cm² at 880 nm. An internal latch provides hysteresis: The output will not turn OFF until the illumina-

tion increases by approximately 12%. Typical loads include an incandescent lamp, LED, sensitive relay, or d-c motor. For applications requiring interface to TTL or CMOS, Series ULN-3360 integrated circuits are similar devices that include an internal pull-up resistor.

Type ULN-3330D is furnished in a hermetically sealed metal package with a glass end cap. The 'D' package conforms to JEDEC outline TO-52 (TO-206AC). The miniature Type ULN-3330T is supplied in a clear plastic package only 0.080″ (2.0 mm) thick. Type ULN-3330Y is furnished in an inexpensive clear plastic package meeting the JEDEC TO-92 (TO-226AA) outline.

FUNCTIONAL BLOCK DIAGRAM

Dwg. No. A-11,127A
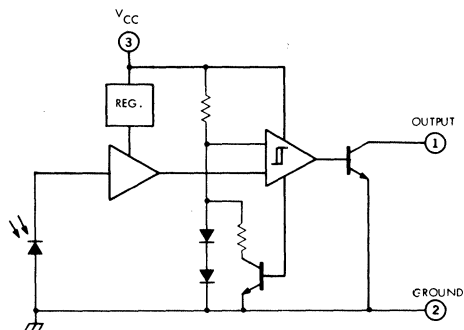
ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} . . . . 15 V
Output Voltage, V_{OUT} . . . . 15 V
Output Current, I_{OUT} . . . . 50 mA
Package Power Dissipation, P_D . . . . See Graph
Operating Temperature Range, T_A . . . . $-40°C$ to $+70°C$
Storage Temperature Range, T_S
      ULN-3330D . . . . $-55°C$ to $+150°C$
      ULN-3330T . . . . $-55°C$ to $+110°C$
      ULN-3330Y . . . . $-55°C$ to $+110°C$

TYPICAL TRANSFER CHARACTERISTICS
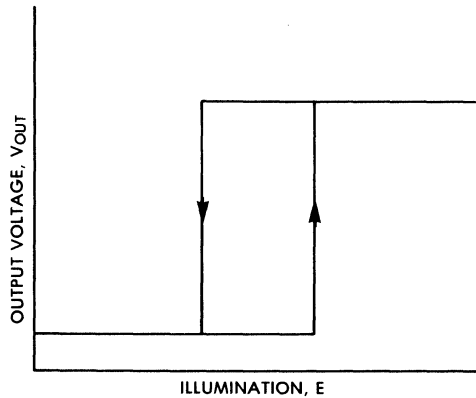
Dwg. No. A-11,128

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{CC} = 6.0$ V, $\lambda = 880$ nm

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Supply Voltage Range	V_{CC}		4.0	6.0	15	V
Supply Current	I_{CC}		—	4.0	8.0	mA
Light Threshold Level	E_{ON}	Output ON	45	55	65	$\mu W/cm^2$
	E_{OFF}	Output OFF	—	62	—	$\mu W/cm^2$
Hysteresis	ΔE	$(E_{OFF} - E_{ON})/E_{OFF}$	10	12	14	%
Output ON Voltage	V_{OUT}	$I_{OUT} = 15$ mA	—	300	500	mV
		$I_{OUT} = 25$ mA	—	500	800	mV
Output OFF Current	I_{OUT}	$V_{OUT} = 15$ V	—	—	1.0	μA
Output Fall Time	t_f	90% to 10%	—	200	500	ns
Output Rise Time	t_r	10% to 90%	—	200	500	ns

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RELATIVE SPECTRAL RESPONSE
AS A FUNCTION OF WAVELENGTH OF LIGHT
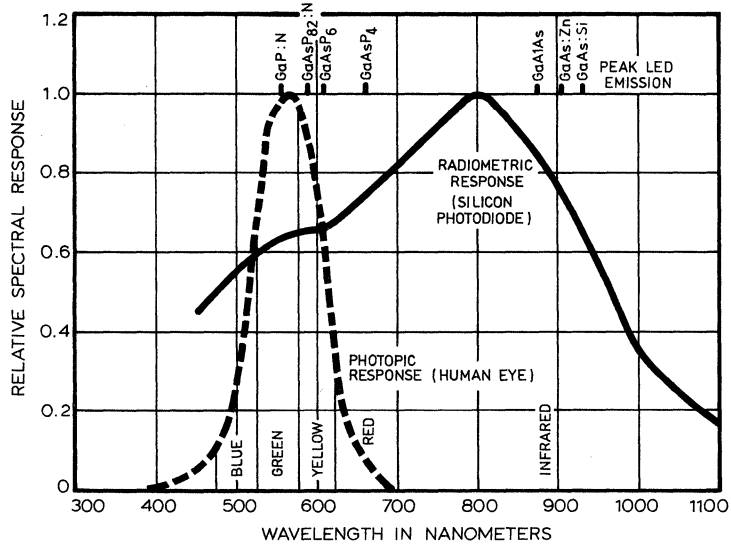
Dwg. No. A-12,135A

RELATIVE SWITCH RESPONSE
AS A FUNCTION OF THE ANGLE OF INCIDENCE
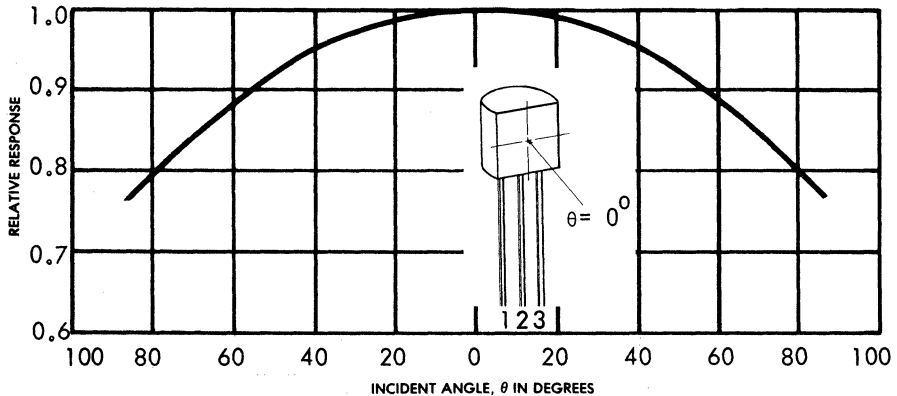
Dwg.No. A-10,853A

SERIES 8126
(SG3526J, SG2526J AND SG1526J)
SWITCHED-MODE POWER SUPPLY CONTROL CIRCUITS

FEATURES

- 8 V to 35 V Operation
- Dual 100 mA Source/Sink Outputs
- Internal Regulator
- Current Limiting
- Temperature-Compensated
  Reference Source
- Sawtooth Generator
- Low Supply-Voltage Protection
- External Synchronization
- Double-Pulse Suppression
- Programmable Dead-Time
- Programmable Soft-Start

THESE INTEGRATED CONTROLLERS of fixed-frequency switching regulators and similar power devices can be used with transformerless or transformer-coupled supplies with single-ended or push-pull, positive or negative output.

Types ULN-8126A/R, ULQ-8126A/R, and ULS-8126R have a temperature-compensated voltage reference, a sawtooth waveform generator, an error amplifier, a pulse-width modulator, pulse metering and steering logic and two 100 mA source/sink drivers. The devices perform housekeeping functions such as soft-start, low-voltage lockout, digital current limiting and double-pulse suppression. Other features include a data latch for single pulse metering, adjustable dead time and provision for symmetry correction.

(Continued on next page)

Dwg. No. A-11,425

ULN-8126A
ULQ-8126A

Dwg. No. A-11,426

ULN-8126R/SG3526J
ULQ-8126R/SG2526J
ULS-8126R/SG1526J

ABSOLUTE MAXIMUM RATINGS
at $T_A = +25°C$

Supply Voltage, V_S . . . . 40 V
Collector Supply Voltage, V_C . . . . 40 V
Logic Input Voltage Range, V_{IN} . . . . −0.3 V to +5.5 V
Analog Input Voltage Range, V_{IN} . . . . −0.3 V to V_S
Output Current, I_O . . . . ±200 mA
Reference Load Current, I_{REF} . . . . 50 mA
Logic Sink Current, I_{IN} . . . . 15 mA
Package Power Dissipation, P_D (Plastic DIP) . . . . 2.3 W*
(Cer-DIP) . . . . 1.9 W*
Operating Temperature Range, T_A . . . . . . See Ordering Data
Storage Temperature Range, T_S . . . . −65°C to +150°C

*Derate linearly to 0 watts at $T_A = +150°C$.

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All digital inputs are TTL and CMOS compatible. Active-low logic allows use of wired-OR connections.

Type ULS-8126R is supplied in an 18-pin glass/ceramic hermetically sealed (cer-DIP) package. It is rated for operation over a temperature range that recommends its use in military and aerospace applications ($-55°C$ to $+125°C$).

Types ULQ-8126A and ULQ-8126R operate over an extended temperature range of $-40°C$ to $+85°C$ that meets the demands of many industrial applications.

Low-cost Types ULN-8126A and ULN-8126R are rated for continuous operation over a temperature range that recommends them for commercial use ($0°C$ to $+70°C$).

Control circuits with commercial and extended temperature ranges are available in both the hermetically sealed cer-DIP package (suffix "R") and a dual in-line plastic package (suffix "A") with a copper alloy lead frame that gives them enhanced power dissipation ratings.

Cer-DIP packaged parts normally are marked with original source part numbers shown below. Sprague part numbers appear on plastic packages. Sprague part numbers should be used on orders and correspondence concerning all Series 8126 devices.

ORDERING INFORMATION

Operating Temperature Range	Package	Original Source Part Number	Sprague Part Number
Commercial 0°C to +70°C	Cer-DIP	SG3526J	ULN-8126R
	Plastic	—	ULN-8126A
Extended −40°C to +85°C	Cer-DIP	SG2526J	ULQ-8126R
	Plastic	—	ULQ-8126A
Full −55°C to +125°C	Cer-DIP	SG1526J	ULS-8126R

RECOMMENDED OPERATING CONDITIONS

Logic Supply Voltage, V_S . . . . 8 V to 35 V

Collector Voltage, V_C . . . . 4.5 V to 35 V

Output Load Current, I_0 . . . . 0 to ±100 mA

Reference Load Current, I_L . . . . 0 to 20 mA

Oscillator Frequency, f . . . . 1 Hz to 400 kHz

Oscillator Timing Resistance, R_T . . . . 2 kΩ to 150 kΩ

Oscillator Timing Capacitance, C_T . . . . 0.001 µF to 20 µF

Programmed Deadtime . . . . 3% to 50%

Operating Temperature Range, T_A . . . . See Ordering Data

FUNCTIONAL BLOCK DIAGRAM
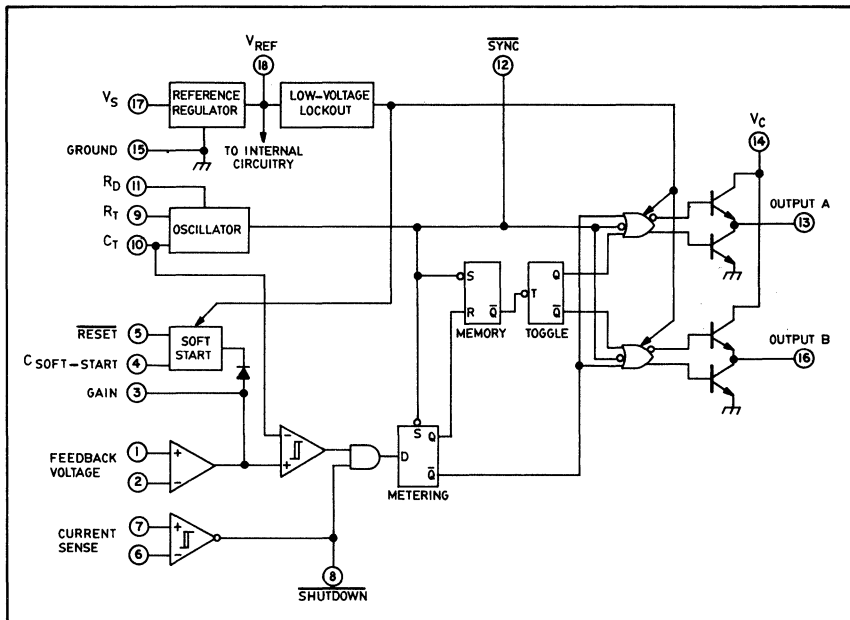
Dwg. No. A-11,427

ELECTRICAL CHARACTERISTICS over operating temperature range, $V_S = 15$ V (unless otherwise noted)

Characteristic	Test Pins	Test Conditions	Extended & Full Temperature Devices*			Commercial Temperature Devices*			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
REFERENCE SECTION ($I_L = 0$ mA)									
Reference Voltage	18	$T_A = +25°C$	4.95	5.00	5.05	4.90	5.00	5.10	V
		Over recommended conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Reference Voltage Regulation	18	$V_S = 8$ to 35 V	—	10	20	—	10	30	mV
		$I_L = 0$ to 20 mA	—	10	30	—	10	50	mV
		Over operating temperature range	—	15	50	—	15	50	mV
Short Circuit Current	18	$V_{REF} = 0$ V	25	50	100	25	50	100	mA
Standby Current	17	$V_S = 35$ V, $R_T = 4.22$ kΩ, $V_8 = 0.4$ V	—	18	—	—	18	—	mA
OSCILLATOR SECTION ($f = 40$ kHz, $R_T = 4.22$ kΩ, $C_T = 0.01$ μF, $R_D = 0\Omega$)									
Oscillator Frequency	9,10	$R_T = 150$kΩ, $C_T = 20$ μF	—	—	1.0	—	—	1.0	Hz
		$R_T = 2$ kΩ, $C_T = 0.001$ μF	400	—	—	400	—	—	kHz
Initial Oscillator Accuracy	9,10	$T_A = +25°C$	—	3.0	—	—	3.0	—	%
Oscillator Stability	9,10	$V_S = 8$ to 35 V	—	0.5	—	—	0.5	—	%
		Over operating temperature range	—	1.0	—	—	1.0	—	%
		Over recommended conditions	—	2.0	—	—	2.0	—	%
Sawtooth Peak Voltage	10	$V_S = 35$ V	—	3.0	3.5	—	3.0	3.5	V
Sawtooth Valley Voltage	10	$V_S = 8.0$ V	0.5	1.0	—	0.5	1.0	—	V
Sync Pulse Width	12	$C_L = 15$ pF	—	500	—	—	500	—	ns
HOUSEKEEPING FUNCTIONS									
Logic Voltage Levels	5,8,12	Logic HIGH, $I_{SOURCE} = -40$ μA	2.4	4.0	—	2.4	4.0	—	V
		Logic LOW, $I_{SINK} = 3.6$ mA	—	0.2	0.4	—	0.2	0.4	V
Input Current	5,8,12	$V_{IN} = 2.4$ V	—	-125	-200	—	-125	-200	μA
		$V_{IN} = 0.4$ V	—	-225	-360	—	-225	-360	μA
Shutdown Delay	8-13, 16	100 mV step, 5mv overdrive, $R_S = 50\Omega$	—	300	—	—	300	—	ns

NOTES: Negative current is defined as coming out of (sourcing) the specified device pin.

*Commercial, extended, and full temperature-range devices are defined in preceding text and "Ordering Information" table.

ELECTRICAL CHARACTERISTICS (Continued)

| Characteristic	Test Pins	Test Conditions	Extended & Full Temperature Devices*			Commercial Temperature Devices*			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
ERROR AMPLIFIER (V_{CM} = 0 to 5.2 V)									
Input Offset Voltage	1,2	R_S = 2 kΩ	—	2.0	5.0	—	2.0	5.0	mV
Input Bias Current	1,2		—	−350	−1000	—	−350	−2000	nA
Input Offset Current	1,2		—	35	100	—	35	200	nA
Error Amplifier Gain	1-3	Open loop, R_L = 10 MΩ	64	72	—	60	72	—	dB
Small Signal Bandwidth	1-3	C_L = 30 pF	0.7	1.0	—	0.7	1.0	—	MHz
Output Voltage Swing	3	Positive limit, R_L = 50 kΩ	3.6	4.2	—	3.6	4.2	—	V
		Negative limit, R_L = 50 kΩ	—	0.2	0.4	—	0.2	0.4	V
Common Mode Range	1,2	V_S = 8.0 V	0	—	5.2	0	—	5.2	V
Common Mode Rejection	1,2	R_S = 10 kΩ	70	94	—	70	94	—	dB
Error Amplifier V_S Rejection	3	f = 120 Hz, ΔV_S = 1.0 V_{rms}	66	80	—	66	80	—	dB
CURRENT LIMITING									
Common Mode Range	6,7	V_S = 18 V	0	—	15	0	—	15	V
Sense Voltage	6,7	V_{CM} = 0 to 15 V	—	100	—	—	100	—	mV
Input Current	6,7	V_{CM} = 0 to 15 V	—	−3.0	—	—	−3.0	—	μA
Voltage Gain	7-8	I_8 = 360 μA	—	68	—	—	68	—	dB
SOFT-START SECTION									
Error Clamp Voltage	—	V_5 = 0.4 V	—	100	400	—	100	400	mV
C_S Charging Current	4	V_5 = 2.4 V	—	100	—	—	100	—	μA
OUTPUT DRIVERS (V_C = 15 V)									
Output Voltage	13,16	I_{OUT} = −20 mA	12.5	13.5	—	12.5	13.5	—	V
		I_{OUT} = −100 mA	—	13	—	—	13	—	V
		I_{OUT} = 20 mA	—	0.2	0.3	—	0.2	0.3	V
		I_{OUT} = 100 mA	—	1.2	—	—	1.2	—	V
Leakage Current	13,16	V_C = 40 V	—	0.1	100	—	0.1	100	μA
Rise Time	13,16	C_L = 1000 pF	—	300	—	—	300	—	ns
Fall Time	13,16	C_L = 1000 pF	—	200	—	—	200	—	ns

NOTES: Negative current is defined as coming out of (sourcing) the specified device pin.

*Commercial, extended, and full temperature-range devices are defined in preceding text and "Ordering Information" table.

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SERIES 8160

(NE5560N, NE5560F AND SE5560F)

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUITS

FEATURES

- Internal Voltage Regulator
- Current Limiting
- Temperature-Compensated Reference Source
- Sawtooth Generator
- Pulse-Width Modulator
- Remote ON/OFF Switching
- Low Supply-Voltage Protection
- Loop-Fault Protection
- Demagnetization/High-Voltage Protection
- Maximum Duty-Cycle Adjustment
- Feed-Forward Control
- External Synchronization

FUNCTIONAL BLOCK DIAGRAM

Dwg. No. B-1463A
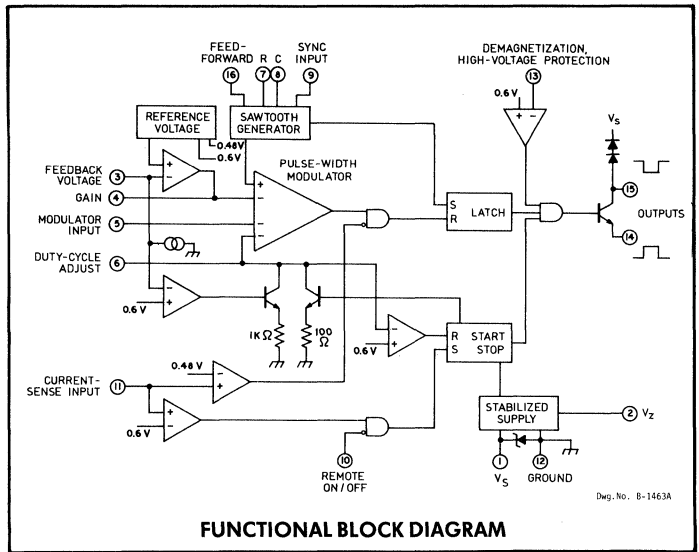
COMPREHENSIVE CONTROL of state-of-the-art power supplies is offered by Sprague Type ULN-8160A, ULN-8160R, and ULS-8160R integrated circuits. Each control circuit has its own temperature-compensated reference source, an internal error amplifier, a sawtooth waveform generator, a pulse-width modulator, an output driver, and a variety of protection circuitry.

Type ULN-8160A is supplied in a 16-pin dual in-line plastic package with a copper lead frame that gives the device enhanced power dissipation ratings. It is rated for operation over a temperature range of 0°C to +70°C.

Types ULN-8160R and ULS-8160R are furnished in 16-pin hermetically sealed glass/ceramic packages. These devices will withstand severe environmental contamination.

In addition, the extended temperature range of Type ULS-8160R (−55°C to +125°C) recommends it for use in military and aerospace applications.

These devices are normally branded with both the original source part number and the Sprague part numbers; however, the Sprague part number should be used on orders and in correspondence.

ABSOLUTE MAXIMUM RATINGS
AT $T_A = +25°C$

Supply Voltage, V_S . . . . (See Note)
Supply Current, I_{REG} . . . . 30 mA
Output Current, I_0 . . . . 40 mA
Package Power Dissipation, P_D (ULN-8160A) . . . . 2.1 W*
        (ULN-8160R/ULS-8160R) . . . . 1.7 W*
Operating Temperature Range, T_A (ULN-8160A/R) . . . . 0°C to +70°C
        (ULS-8160R) . . . . −55°C to +125°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

*Derate linearly to 0 W at $T_A = +150°C$.
Note: Maximum allowable supply voltage is dependent on value of external current limiting resistor;
18 V @ 0Ω.

ORDERING INFORMATION

Original Source* Part Number	Sprague Part Number	Operating Temperature Range	Package
NE5560N	ULN-8160A	0°C to +70°C	Plastic
NE5560F	ULN-8160R	0°C to +70°C	Cer-DIP
SE5560F	ULS-8160R	−55°C to +125°C	Cer-DIP

*These devices are manufactured under a cross-license with Signetics Corp. (a subsidiary of U.S. Philips Corp.)

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_S = 12$ V (unless otherwise noted)

Characteristic	Test Pin	Test Conditions	ULS-8160R Min.	ULS-8160R Typ.	ULS-8160R Max.	ULN-8160A/R Min.	ULN-8160A/R Typ.	ULN-8160A/R Max.	Units
Supply Clamp Voltage	1	$I_S = 10$ mA	20	—	23	19	—	24	V
		$I_S = 30$ mA	20	—	30	20	—	30	V
Supply Current	1	$V_S = 12$ V, $I_Z = 0$	—	—	10	—	—	10	mA
REFERENCE SECTIONS									
Internal Reference, V_{REF}	—	$T_A = +25°C$	3.69	3.72	3.81	3.57	3.72	3.95	V
		Over operating temperature range	3.65	—	3.85	3.53	—	4.00	V
Temperature Coefficient of V_{REF}	—		—	±100	—	—	±100	—	ppm/°C
Zener Reference, V_Z	2	$I_Z = -7.0$ mA	7.8	8.4	9.0	7.8	8.4	9.0	V
Temperature Coefficient of V_Z	2		—	−200	—	—	−200	—	ppm/°C
OSCILLATOR SECTION									
Oscillator Frequency Range	7, 8		50	—	100k	50	—	100k	Hz
Initial Oscillator Accuracy	7, 8	$R_7 = 5$ kΩ	—	5.0	—	—	5.0	—	%
Duty-Cycle Range	7, 8	$f_0 = 20$ kHz	0	—	98	0	—	98	%
MODULATOR									
Modulator Input Current	5	$V_5 = 1.0$ V	—	0.2	20	—	0.2	20	μA

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ELECTRICAL CHARACTERISTICS (Continued)

| Characteristic	Test Pin	Test Conditions	ULS-8160R Min.	ULS-8160R Typ.	ULS-8160R Max.	ULN-8160A/R Min.	ULN-8160A/R Typ.	ULN-8160A/R Max.	Units
HOUSEKEEPING FUNCTIONS									
Duty-Cycle Control	6	$V_6 = 0.41 V_z$	40	50	60	40	50	60	%
Duty-Cycle Control Current	6	Over operating temperature range	—	0.2	20	—	0.2	20	μA
Protection Thresholds	1	Low supply-voltage protection	8.0	9.0	10.5	8.0	9.0	10.5	V
	3	Feedback-loop protection ON	400	600	720	400	600	720	mV
	13	Demagnetization/high-voltage protection	470	600	720	470	600	720	mV
Sense-Input Current	3	Over operating temperature range	−7.0	−15	−35	−7.0	−15	−35	μA
Input Current	13	$T_A = +25°C$	—	−3.0	−20	—	−3.0	−20	μA
		Over operating temperature range	—	—	−40	—	—	−40	μA
Duty-Cycle Control	16	$V_{16} = 2V_z$, Percent of original duty cycle	30	40	50	30	40	50	%
Input Current	16	$T_A = +25°C$	—	0.2	5.0	—	0.2	5.0	μA
		Over operating temperature range	—	—	10	—	—	10	μA
EXTERNAL SYNCHRONIZATION									
Sync Input OFF Voltage	9		0	—	0.8	0	—	0.8	V
Sync Input ON Voltage	9		2.0	—	V_z	2.0	—	V_z	V
Sync Input Current	9	$V_9 = 0 V, T_A = +25°C$	—	−65	−100	—	−65	−125	μA
		$V_9 = 0 V$, over operating temp. range	—	—	−125	—	—	−125	μA
REMOTE									
Remote OFF Voltage	10		0	—	0.8	0	—	0.8	V
Remote ON Voltage	10		2.0	—	V_z	2.0	—	V_z	V
Remote Input Current	10	$T_A = +25°C$	—	−85	−100	—	−85	−125	μA
		Over operating temperature range	—	—	−125	—	—	−125	μA
CURRENT LIMITING									
Input Current	11	$V_{11} = 250$ mV, $T_A = +25°C$	—	−6.0	−40	—	−6.0	−40	μA
		$V_{11} = 250$ mV, Over operating temp. range	—	—	−80	—	—	−80	μA
Inhibit Delay	11	One pulse, 20% overdrive @ $I_0 = 40$ mA	—	700	800	—	700	800	ns
Trip Levels	11	Shutdown/slow start	560	600	700	560	600	700	mV
		Current limit	400	480	560	400	480	560	mV
ERROR AMPLIFIER									
Error-Amplifier Gain	3-4	Open loop	54	60	—	54	60	—	dB
Error-Amplifier Feedback Resistance	4		10	—	—	10	—	—	kΩ
Small-Signal Bandwidth	3-4		—	3.0	—	—	3.0	—	MHz
Output-Voltage Swing	4	Positive limits	6.2	—	9.5	6.2	—	9.5	V
		Negative limits	—	—	0.7	—	—	0.7	V
OUTPUT STAGE									
Output Current	15		40	—	—	40	—	—	mA
Output-Saturation Voltage	15	$V_{CE(SAT)}$ @ $I_C = 40$ mA	—	—	500	—	—	500	mV
Output Voltage	14		5.0	6.0	—	5.0	6.0	—	V

NOTE: Negative current is defined as coming out of (sourcing) the specified device pin.

ULN-8161M (NE5561N)
SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT

FEATURES

- Stabilized Power Supply
- Current Limiting
- Temperature-Compensated Reference Source
- Sawtooth Generator
- Pulse-Width Modulator
- Double-Pulse Protection
- Applications in
  —Switched-Mode Power Supplies
  —Motor Controller-Inverters
  —D-C/D-C Converters
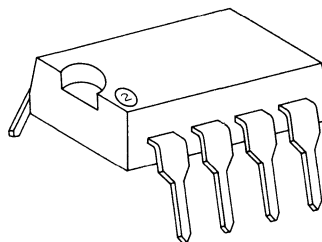
Dwg. No. A-11,423

ULN-8161M/NE5561N

DESIGNED AS A CONTROLLER for low-cost switched-mode power supplies, Sprague Type ULN-8161M excels in applications requiring only limited housekeeping functions.

The integrated circuit has its own temperature-compensated reference source, an internal Zener reference, a sawtooth waveform generator, an error amplifier, pulse-width modulator, output driver, current-sensing and low-voltage protection.

Type ULN-8161M is supplied in an 8-pin dual in-line plastic package with a copper lead frame that gives it enhanced power dissipation ratings. It is rated for continuous operation over the temperature range of 0°C to +70°C. Similar devices are available for operation over extended temperature ranges.

This device is normally branded with both the original source part number and the Sprague part number; however, the Sprague part number should be used on orders and in correspondence.

ABSOLUTE MAXIMUM RATINGS
at T_A = +25°C

Supply Voltage, V_S (Voltage Sourced) . . . . 18 V
Output Current, I_0 . . . . 40 mA
Output Duty Cycle 98%
Package Power Dissipation, P_D . . . . 1.5 W*
Operating Temperature Range, T_A . . . . 0°C to +70°C
Storage Temperature Range, T_S . . . . −65°C to +150°C
*Derate at the rate of 12.5 mW/°C above T_A = +25°C.

ORDERING INFORMATION

Original Source* Part Number	Sprague Part Number	Operating Temperature Range	Package
NE5561N	ULN-8161M	0°C to +70°C	Plastic

*This device is manufactured in accordance with a cross-license with Signetics Corp. (a subsidary of U.S. Philips Corp.)

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ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_S = 12$ V (unless otherwise noted)

Characteristic	Test Pin	Test Conditions	Min.	Typ.	Max.	Units
				Limits		
Supply Voltage Range	1	$I_S = 10$ mA, current-fed	19	—	24	V
Internal Reference, V_{REF}	—	Over operating temperature range	3.55	—	3.98	V
		$T_A = +25°C$	3.57	3.76	3.96	V
Temperature Coefficient of V_{REF}	—		—	±100	—	ppm/°C
Zener Reference, V_Z	2	$I_2 = -7.0$ mA	7.8	8.4	9.0	V
Temperature Coefficient of V_Z	2		—	±150	—	ppm/°C
Oscillator Frequency Range	5	Over operating temperature range	50	—	100k	Hz
Initial Oscillator Accuracy	5		—	5.0	—	%
Duty-Cycle Range	5	$f_0 = 20$ kHz	0	—	98	%
Protection Threshold	1	Low supply-voltage protection	8.5	9.1	10.5	V
Input Current	6	$V_6 = 250$ mV, over operating temperature range	—	—	—20	μA
		$V_6 = 250$ mV, $T_A = +25°C$	—	—2.0	—10	μA
Inhibit Delay	6	Single pulse, 20% overdrive at $I_0 = 20$ mA	—	700	800	ns
Trip Level	6	Current limit	400	520	600	mV
Error Amplifier Gain	3-4	Open loop	—	60	—	dB
Error Amplifier Feedback Resistance	4		10	—	—	kΩ
Small-Signal Bandwidth	3-4		—	3.0	—	MHz
Output-Voltage Swing	4	Positive limit	6.2	—	—	V
		Negative limit	—	—	0.6	V
Output Current	7	Over operating temperature range	20	—	—	mA
Output Saturation Voltage	7	$V_{CE(SAT)}$ @ $I_C = 20$ mA	—	—	0.5	V
Supply Current	1	$I_Z = 0$, over operating temp. range, voltage-fed	—	—	15	mA
		$I_Z = 0$, $T_A = +25°C$, voltage-fed	—	—	9.0	mA

FUNCTIONAL BLOCK DIAGRAM

Dwg. No. A-11,424
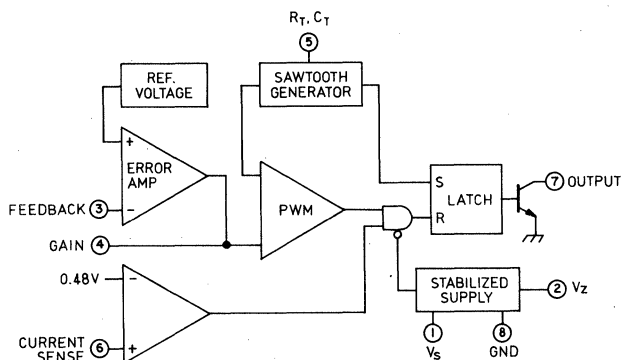
SERIES TPP
MEDIUM-POWER DARLINGTON ARRAYS
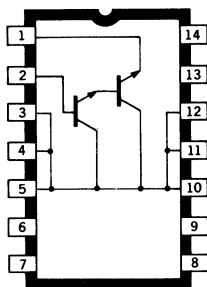
DWG.NO. A-10,779A

TPP-1000
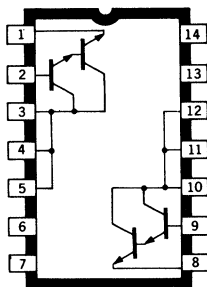
DWG.NO. A-10,780A

TPP-2000
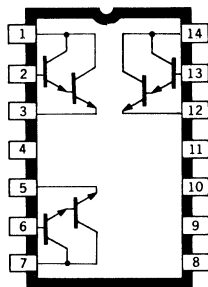
DWG.NO. A-10,781A

TPP-3000
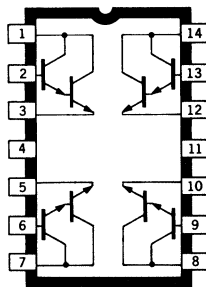
DWG.NO. A-10,782A

TPP-4000

THESE SPRAGUE MEDIUM-POWER arrays consist of one, two, three, or four Darlington-pairs in a single 14-pin dual in-line plastic package.

Features of Series TPP, which complements the Sprague TPQ Series of quad transistor arrays, includes a collector-current rating of 4 A, a minimum h_{FE} of 2,000, and a 2 W package power dissipation rating.

The standard molded dual in-line package for Series TPP is identical to the type used for many integrated circuits. It offers superior mechanical protection for circuit elements during automatic insertion into printed wiring boards.

ABSOLUTE MAXIMUM RATINGS

Collector Current, I_C . . . . 4.0 A
Power Dissipation, P_D (total package) . . . . 2 W*
Operating Temperature Range, T_A . . . . −55°C to +150°C
Storage Temperature Range, T_S . . . . −65°C to +150°C
*Derate at the rate of 16 mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS at T_A = +25°C

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Collector-Emitter Breakdown Voltage	BV_{CES}	$I_C = 100\ \mu A$	40	50	—	V
Collector-Base Breakdown Voltage	BV_{CBO}	$I_C = 100\ \mu A$	50	60	—	V
Emitter-Base Breakdown Voltage	BV_{EBO}	$I_E = 100\ \mu A$	12	14	—	V
Collector-Cutoff Current	I_{CBO}	$V_{CB} = 30\ V$	—	10	100	nA
Emitter-Cutoff Current	I_{EBO}	$V_{EB} = 10\ V$	—	10	100	nA
Collector-Emitter Saturation Voltage	$V_{CE\ (sat)}$	$I_B = 1.0\ mA,\ I_C = 1.0\ A$	—	1.0	1:5	V
Base-Emitter Saturation Voltage	$V_{BE\ (sat)}$	$I_B = 1.0\ mA,\ I_C = 1.0\ A$	—	1.6	2.0	V
Static Forward	h_{FE}	$V_{CE} = 5.0\ V,\ I_C = 500\ mA$	2000	—	—	—
Current-Transfer		$V_{CE} = 5.0\ V,\ I_C = 1.0\ A$	2000	—	—	—
Ratio		$V_{CE} = 5.0\ V,\ I_C = 2.0\ A$	2000	—	—	—

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SERIES TPQ

QUAD TRANSISTOR ARRAYS

SPRAGUE SERIES TPQ quad transistor arrays are general-purpose silicon transistor arrays consisting of four independent devices. Shown are 12 NPN types, 12 PNP types, and nine NPN/PNP complementary pairs.

All of these devices are furnished in a 14-pin dual in-line plastic package. The molded package is identical to that used in most consumer integrated circuits and offers superior mechanical protection during insertion into printed wiring boards.
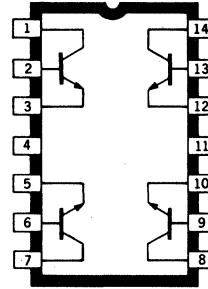
DWG. NO. A-10,050A

TPQ2221	TPQ3725A
TPQ2222	TPQ3904
TPQ2483	TPQ5550
TPQ2484	TPQ5551
TPQ3724	TPQA05
TPQ3725	TPQA06
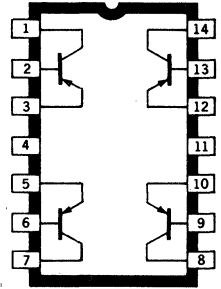
DWG. NO. A-10,051A

TPQ2906	TPQ4258
TPQ2907	TPQ4354
TPQ2907A	TPQ5400
TPQ3798	TPQ5401
TPQ3799	TPQA55
TPQ3906	TPQA56

ABSOLUTE MAXIUMUM RATINGS

Power Dissipation, P_D (Each Transistor) . . . . 500 mW
(Total Package) . . . . 2.0 W*
Operating Temperature Range, T_A . . . . −55°C to +150°C
Storage Temperature Range, T_S . . . . −65°C to +150°C

*Derate at the rate of 16 mW/°C above T_A = +25°C
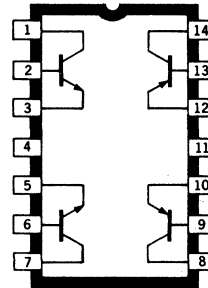
DWG. NO. A-10,052A

TPQ6001
TPQ6002
TPQ6100
TPQ6100A
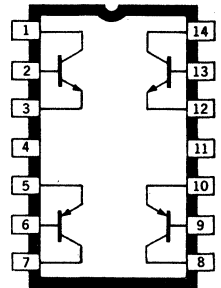
DWG. NO. A-10,053A

TPQ6501
TPQ6502
TPQ6600
TPQ6600A
TPQ6700

Additional information on
TPP and TPQ Transistor arrays is available from:

Sprague Electric Company
Discrete Semiconductor Operation
70 Pembroke Road
Concord, New Hampshire 03301
(603) 224-1961

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

Part Number	Min. BV_{CBO} (V)	Min. BV_{CEO} (V)	Min. BV_{EBO} (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	D-C Current Gain Min. h_{FE}	Conditions I_C (mA)	Conditions V_{CE} (V)	Saturation Voltage Max. V_{CE} (V)	Saturation Voltage Max. V_{BE} (V)	@ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	Max. C_{ob} (pF)	Similar Discrete Devices
								Four NPN Devices							
TPQ2221	60	40	5.0	50	50	35 40 20	10 150 300	10 10 10	0.40 1.60	1.30 2.60	150 300	200	20	8.0	2N2221
TPQ2222	60	50	5.0	50	50	75 100 30	10 150 300	10 10 10	0.40 1.60	1.30 2.60	150 300	200	20	8.0	2N2222
TPQ2483	60	40	6.0	20	45	100 150 150	0.1 1.0 10	5.0 5.0 5.0	0.35 0.50 (See Note 1)	0.70 0.80	1.0 10	50	0.5	6.0	2N2483
TPQ2484	60	40	6.0	20	45	200 300 300	0.1 1.0 10	5.0 5.0 5.0	0.35 0.50 (See Note 1)	0.70 0.80	1.0 10	50	0.5	6.0	2N2484
TPQ3724	60 (Note 2)	30	5.0	500	40	35 25	100 500	1.0 2.0	0.45	1.00	500	250	50	10	2N3724
TPQ3725	60	40	5.0	500	40	35 25	100 500	1.0 2.0	0.45	1.00	500	250	50	10	2N3725
TPQ3725A	70 (Note 2)	50	5.0	500	40	40 30	100 500	1.0 2.0	0.45	1.00	500	200	50	10	2N3725A
TPQ3904	60	40	6.0	50	40	30 50 75	0.1 1.0 10	1.0 1.0 1.0	0.20	0.85	10	250	10	4.0	2N3904
TPQ5550	160	140	6.0	100	100	60 60 20	1.0 10 50	5.0 5.0 5.0	0.15 0.25	1.00 1.20	10 50	100	10	6.0	2N5550
TPQ5551	180	160	6.0	50	120	80 80 30	1.0 10 50	5.0 5.0 5.0	0.15 0.25	1.00 1.20	10 50	100	10	6.0	2N5551
TPQA05	60	60	4.0	100	(Note 3)	50 50	10 100	1.0 2.0	0.25	—	100	—	—	10	MPSA05
TPQA06	80	80	4.0	100	(Note 4)	50 50	10 100	1.0 2.0	0.25	—	100	—	—	10	MPSA06

NOTES:
1. Base-emitter voltage shown is $V_{BE(ON)}$ at indicated I_C, $V_{CE} = 5.0$ V.
2. BV_{CES}
3. I_{CES} at $V_{CE} = 50$ V, $V_{BE} = 0$.
4. I_{CES} at $V_{CE} = 60$ V, $V_{BE} = 0$.

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ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

Part Number	Min. BV_{CBO} (V)	Min. BV_{CEO} (V)	Min. BV_{EBO} (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	D-C Current Gain Min. h_{FE}	Conditions I_C (mA)	Conditions V_{CE} (V)	Saturation Voltage Max. V_{CE} (V)	Saturation Voltage Max. V_{BE} (V)	@ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	Max. C_{ob} (pF)	Similar Discrete Devices
Four PNP Devices															
TPQ2906	−60	−40	−5.0	50	−30	35	10	−10	−0.40	−1.30	150	200	50	8.0	2N2906
						40	150	−10	−1.60	−2.60	300				
						30	300	−10							
TPQ2907	−60	−40	−5.0	50	−30	75	10	−10	−0.40	−1.30	150	200	50	8.0	2N2907
						100	150	−10	−1.60	−2.60	300				
						50	300	−10							
TPQ2907A	−60	−60	−5.0	50	−30	75	10	−10	−0.40	−1.30	150	200	50	8.0	2N2907A
						100	150	−10	−1.60	−2.60	300				
						50	300	−10							
TPQ3798	−60	−40	−5.0	10	−50	100	0.01	−5.0	−0.20	−0.70	0.1	60	1.0	4.0	2N3798
						150	0.1	−5.0	−0.25	−0.80	1.0				
						150	0.5	−5.0							
						125	10	−5.0							
TPQ3799	−60	−60	−5.0	10	−50	225	0.01	−5.0	−0.20	−0.70	0.1	60	1.0	4.0	2N3799
						300	0.1	−5.0	−0.25	−0.80	1.0				
						300	0.5	−5.0							
						250	10	−5.0							
TPQ3906	−40	−40	−5.0	50	−30	40	0.1	−1.0	−0.25	−0.85	10	200	10	4.5	2N3906
						60	1.0	−1.0							
						75	10	−1.0							
TPQ4258	−12	−12	−4.5	10	−6.0	30	10	−3.0	−0.15	−0.95	10	700	10	3.0	2N4258
TPQ4354	−60	−60	−5.0	50	−50	25	0.1	−10	−0.15	−0.90	150	100	50	30 (Note 1)	2N4354
						40	1.0	−10							
						50	10	−10							
						40	100	−10							
TPQ5400	−130	−120	−5.0	100	(Note 2)	30	1.0	−5.0	−0.20	−1.00	10	100	10	6.0	2N5400
						40	10	−5.0	−0.50	−1.00	50				
						40	50	−5.0							
TPQ5401	−160	−150	−5.0	100	(Note 3)	50	1.0	−5.0	−0.20	1.00	10	100	10	6.0	2N5401
						60	10	−5.0	−0.50	1.00	50				
						50	50	−5.0							
TPQA55	−60	−60	−4.0	100	(Note 4)	50	10	−1.0	−0.25	—	100	—	—	15	MPSA55
						50	100	−2.0							
TPQA56	−80	−80	−4.0	100	(Note 5)	50	10	−1.0	−0.25	—	100	—	—	15	MPSA56
						50	100	−2.0							

NOTES:
1. C_{cb}
2. I_{CES} at $V_{CE} = 100$ V, $V_{BE} = 0$.
3. I_{CES} at $V_{CE} = 120$ V, $V_{BE} = 0$.
4. I_{CES} at $V_{CE} = 50$ V, $V_{BE} = 0$.
5. I_{CES} at $V_{CE} = 60$ V, $V_{BE} = 0$.

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$

Part Number (See Note)	Min. BV_{CBO} (V)	Min. BV_{CEO} (V)	Min. BV_{EBO} (V)	I_{CBO} Max. (nA)	I_{CBO} @ V_{CB} (V)	D-C Current Gain Min. h_{FE}	Conditions I_C (mA)	Conditions V_{CE} (V)	Saturation Voltage Max. V_{CE} (V)	Max. V_{BE} (V)	@ I_C (mA)	f_T Min. (MHz)	f_T @ I_C (mA)	Max. C_{ob} (pF)	Similar Discrete Devices
Two NPN/Two PNP Devices															
TPQ6001	60	30	5.0	30	50	25 35 40 20	1.0 10 150 300	10 10 10 10	0.40 1.40	1.30 2.00	150 300	200	50	8.0	2N2221 and 2N2906
TPQ6002 (Note 1)	60	30	5.0	30	50	50 75 100 30	1.0 10 150 300	10 10 10 10	0.40 1.40	1.30 2.00	150 300	200	50	8.0	2N2222 and 2N2907
TPQ6100	60	40	5.0	10	50	50 75 75 60	0.1 0.5 1.0 10	5.0 5.0 5.0 5.0	0.25	0.80	1.0	100	0.5	4.0	2N2483 and 2N3798
TPQ6100A	60	45	5.0	10	50	100 150 150 60	0.1 0.5 1.0 10	5.0 5.0 5.0 5.0	0.25	0.80	1.0	100	0.5	4.0	2N2484 and 2N3799
TPQ6501	60	30	5.0	30	50	25 35 40 20	1.0 10 150 300	10 10 10 10	0.40 1.40	1.30 2.00	150 300	200	50	8.0	2N2221 and 2N2906
TPQ6502	60	30	5.0	30	50	50 75 100 30	1.0 10 150 300	10 10 10 10	0.40 1.40	1.30 2.00	150 300	200	50	8.0	2N2222 and 2N2907
TPQ6600	60	40	5.0	10	50	50 75 75 60	0.1 0.5 1.0 10	5.0 5.0 5.0 5.0	0.25	0.80	1.0	100	0.5	4.0	2N2483 and 2N3798
TPQ6600A	60	45	5.0	10	50	100 150 150 60	0.1 0.5 1.0 10	5.0 5.0 5.0 5.0	0.25	0.80	1.0	100	0.5	4.0	2N2484 and 2N3799
TPQ6700	40	40	5.0	50	30	30 50 70	0.1 1.0 10	1.0 1.0 1.0	0.25	0.90	10	200	10	4.5	2N3904 and 2N3906

NOTE:
NPN/PNP complementary pairs. Polarity shown is for NPN devices.

10

AN ELECTRONIC LAMP MONITOR

REQUIREMENTS

There are several requirements for a lamp monitoring system. The system should be able to monitor all types of exterior lamps on the automobile; the number of lamps must not be critical to the design. The system must be easy to assemble; it should be simple in design so that it can be repaired in the field with minimal training of personnel; it must be reliable and must be able to withstand the electrical and environmental conditions to which the vehicle is subjected. There should be minimal change from one car line to another, and from one model year to another. Most importantly, the unit cost should be reasonable.

LAMP MONITORING METHODS

Several methods of detecting lamp failure have been examined by the automotive industry. In one, reed relays mounted close to the wiring harness are closed by the electromagnetic force produced by the lamp current. If a lamp fails, the relay opens, resulting in an indication on the dashboard. The system has inherent problems, including a lack of uniformity of the relays, tight tolerances on the proximity of the relays to the wiring assemblies, and the effects of vibration in the automobile.

Another method of monitoring lamps involves the use of phototransistors (Figure 1). These light-sensitive solid-state devices detect the presence of light at each monitored lamp. The signals from each

Dwg. No. A-11,471
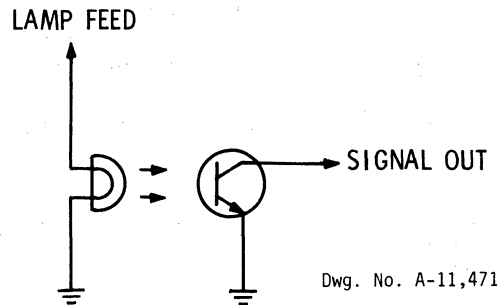
Figure 1
PHOTOTRANSISTOR SYSTEM

lamp are brought to a common switch, which controls the operation of an indicator on the dash. This monitoring system is unattractive to the user because of cost, difficulty in placement of the sensing devices, inability to detect a single failure in a dual filament lamp, and the need for calibration of devices for various types of lamps.

One of the more frequently used systems employs fiber optics (Figure 2). The fiber-optic system uses a plastic or glass fiber that transmits light and gives a positive-function indication for each of the lamps monitored. However, this system is used only in applications requiring the monitoring of a small number of lamps, since the cost of materials and of routing fiber optics is prohibitively expensive.

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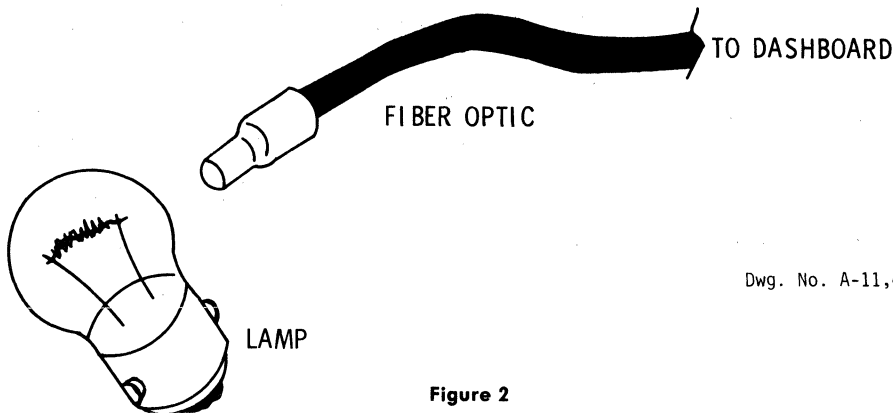
Figure 2
FIBER-OPTIC SYSTEM

SOLUTION

The Sprague Type ULN-2435A electronic lamp monitor overcomes technical problems discussed above while taking advantage of the low cost of integrated circuits. This integrated circuit monitors all types of exterior lamps and provides five outputs capable of driving light-emitting diodes that indicate the location of automotive lamp failure.
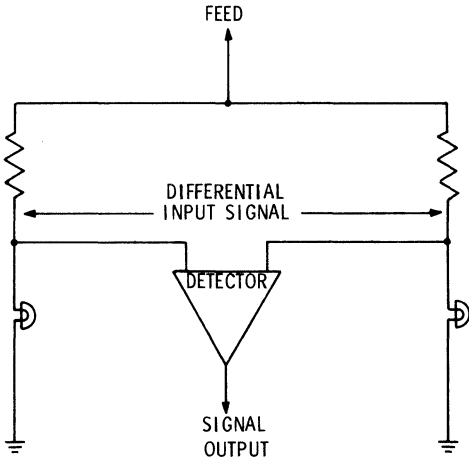
Dwg. No. A-11,473

Figure 3
BRIDGE MONITORING SYSTEM

The principle of operation is that of a simple bridge circuit (Figure 3) in which the top two legs of the bridge are the wiring-assembly resistance or discrete resistors. The bottom legs of the bridge circuit are the monitored lamps. Four differential amplifiers sense the voltage drops in the wiring assemblies (approximately 20 mV) for each of the various lamp circuits. When the system detects a difference in voltage due to an open filament, the appropriate output driver is turned ON.

A sixth output driver gives an indication if any of the monitored lamps fail. This output can be used to drive an audible signaling device or a centrally-located warning lamp.

CIRCUIT DESCRIPTION

A simplified detector is shown in Figure 4. Q1 and Q2 form a differential amplifier. The amplified differential signal is applied at Point A-B to threshold
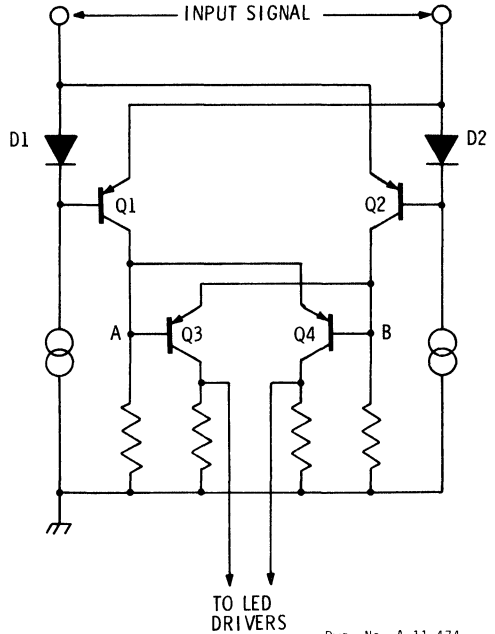
Dwg. No. A-11,474

Figure 4
SIMPLIFIED DETECTOR

detectors Q3 and Q4, which drive the LED driver transistors. D1 and D2 perform the dual function of level-shifting the input signal and establishing required bias currents for Q1 and Q2. Since the supply current is derived from the lamp lines, standby current is reduced to zero when the lamps are turned off.

The use of PNPs in the detectors reduces the system's susceptibility to high-frequency noise. Figure 5 shows a comparison of frequency response for a monolithic NPN transistor and a monolithic PNP transistor.
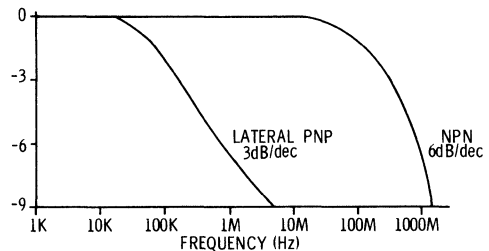
Dwg. No. A-11,475

Figure 5
FREQUENCY RESPONSE

10

A block diagram of a typical application of Type ULN-2435A is depicted in Figure 6. In this application, eight lamps and three fuses are monitored. The stop-lamp fuse (A) is monitored by the circuitry at Pin 4. If the fuse blows, the LEDs connected to pins 10 and 13 turn ON. By using separate fuses for the park lamps and tail /marker-lamp circuits, detectors 1 and 2 can double as fuse monitors. If, for example, fuse B blows, detectors 1 and 2 turn on the LEDs connected to pins 1 and 16. An additional input, pin 6, is used to test the LEDs and the master indicator during cranking.

The simplistic design of this system enables easy installation in an automobile. No external components are required, other than the LED indicators and the voltage-dropping resistors, to complete the system. The integrated circuit may be mounted on a printed wiring board. Depending on lamp current, the copper runs of a printed wiring board might be used as the top legs of the bridge circuit. A failure within the integrated circuit will not affect lamp operation or other automotive functions.

TRANSIENT PROTECTION

In laying out the integrated circuit, careful consideration was given to providing on-chip voltage-transient protection. The LED driver transistors, for example, were designed to withstand an 80-volt load-dump transient. The detector inputs are also designed to withstand 80 volts. In addition, the inputs to the detectors are essentially grounded through the low-resistance lamps being monitored, which further protects the integrated circuit from transients. Reverse-battery protection is included on the chip. In the event of a battery reversal, the PNPs provide inherent protection, while the dielectrically-isolated resistors provide additional safeguards.

Dwg. No. A-11,477
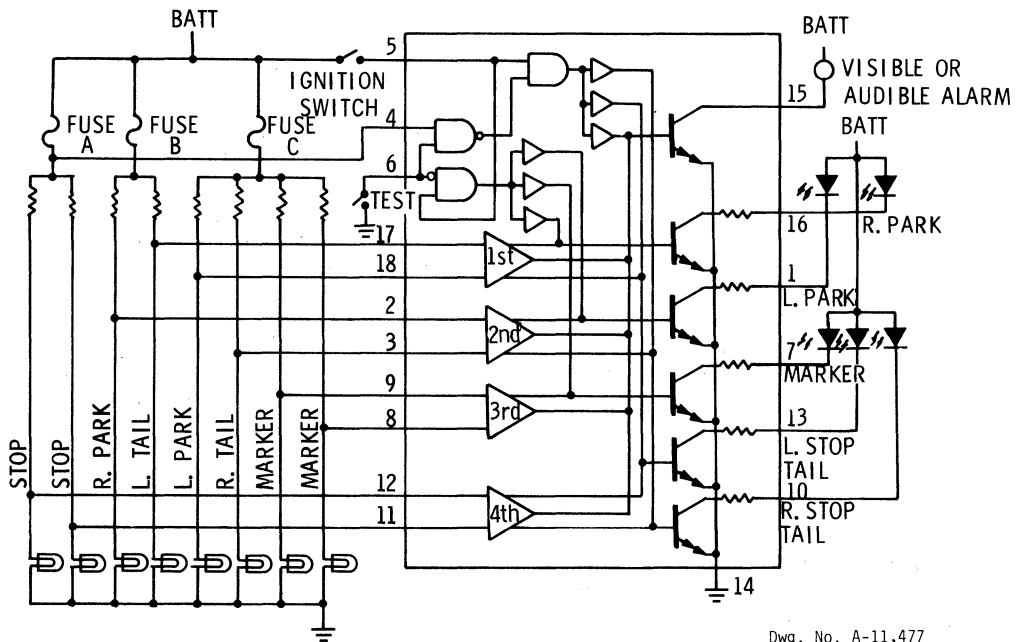
Figure 6

TYPICAL APPLICATION

SECTION 11 — CUSTOM DEVICES

11

ULN-2350C AND ULN-2351C
TUFF CHIP® SEMI-CUSTOM INTEGRATED CIRCUITS

FEATURES

- BV_{CES} = 80 V Min.
- 250 mA Outputs
- 500 Volt Resistors
- High-Gain PNP Transistors
- 80 pF Capacitors
- Time and Cost Savings

TUFF CHIP SEMI-CUSTOM integrated circuits offer substantial time and cost savings for custom circuit applications requiring from 2,000 to 100,000 pieces. This is an area that previously was met by hybrid circuits and, in some cases, by printed wiring boards.

The TUFF CHIP semi-custom approach utilizes a standard array of components fabricated on a single silicon chip: the ULN-2350C contains 460 separate elements; the ULN-2351C provides 261. Besides the traditional complement of NPN and lateral PNP transistors, high-gain vertical PNP transistors are included.

The user lays out the interconnecting circuit, similar to a printed wiring board layout, on sheets provided by Sprague Electric. The artwork is checked by Sprague engineers, and used to generate the customer's proprietary metal mask. Finished circuits are electrically probed and visually inspected. Chips are tray-packed for hybrid circuit manufacturers or are mounted in plastic, ceramic, or hermetic dual in-line packages with from eight to 28 pins.

TUFF CHIP components are optimized for a minimum BV_{CES} of 80 volts. Two or four 250 mA power transistors are provided, and these may be paralleled for high current requirements. On-chip transient protection of sensitive circuit components utilizes deposited film resistors with breakdown voltages higher than 500 volts. On-chip

89 × 104 mils
2.26 × 2.64 mm
ULN-2351C
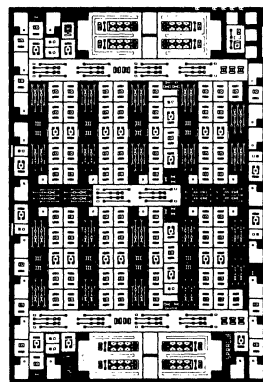
104 × 150 mils
2.64 × 3.81 mm
ULN-2350C

capacitors may be used for noise suppression or filtering.

Circuit users can expect prototypes six to 10 weeks after submitting initial artwork; production quantities can be shipped eight to 10 weeks after prototype approval.

ELECTRICAL CHARACTERISTICS at $T_J = +25°C$

Characteristic	Limits			Units
	Min.	Typ.	Max.	
Small-Signal NPN Transistors				
h_{FE} at $I_C = 1.0$ mA	50	150	200	—
Matching of h_{FE}	—	10	20	± %
BV_{CEO} at $I_C = 100$ μA	30	40	—	V
BV_{CES} at $I_C = 100$ μA	80	100	—	V
BV_{EBO} at $I_E = 100$ μA	6.9	—	7.7	V
R_{SAT} at $I_B = 100$ μA (with plug)	—	300	—	Ω
Cutoff Frequency	—	500	—	MHz
Useful Current Range	0.1	—	10k	μA
NPN Power Transistors				
h_{FE} at $I_C = 200$ mA	50	150	200	—
BV_{CEO} at $I_C = 100$ μA	30	40	—	V
BV_{CES} at $I_C = 100$ μA	80	100	—	V
$V_{CE(SAT)}$ at $I_C = 250$ mA	—	—	1.4	V
Useful Current Range	2.0	—	250	mA
Lateral PNP Transistors				
h_{FE} at $I_C = 100$ μA	15	30	—	—
BV_{CEO} at $I_C = 10$ μA	60	80	—	V
Cutoff Frequency	—	3.0	—	MHz
Vertical PNP Transistors				
h_{FE} at $I_C = 100$ μA	30	60	—	—
BV_{CEO} at $I_C = 10$ μA	50	—	—	V
Passive Components				
Resistor Tolerance	—	—	30	± %
Resistor Matching (1:1) Tol.	—	1.0	3.0	± %
BV—Base Resistor to Substrate	—	80	—	V
BV—Deposited Film Resistor to Substrate	500	—	—	V
Capacitance Tolerance	—	40	—	± %
BV—Capacitors	12	—	—	V

COMPONENT LIST

Component	Number of Devices	
	ULN-2350C	ULN-2351C
Small-Signal NPN Transistors	70	38
NPN Power Transistors	4	2
Lateral PNP Transistors	27	14
Vertical PNP Transistors	10	7
5.8 V Zener Diodes	5	2
Base Resistors:		
200 Ω	10	5
450 Ω	20	12
900 Ω	20	12
1.8 kΩ	20	12
3.6 kΩ	20	12
Deposited Film Resistors:		
2.0 kΩ	16	8
4.5 kΩ	58	33
9.0 kΩ	48	28
18 kΩ	50	29
36 kΩ	72	42
80 pF Capacitors	10	5
Bonding Pads	28	19

11

HIGH-VOLTAGE, SEMI-CUSTOM COMPONENT ARRAYS

INTRODUCTION

Semi-custom integrated circuits have been produced for several years for the low-volume integrated circuit market.

The semi-custom approach uses wafers that are completely fabricated except for the interconnecting metal. The user designs the interconnecting metal mask to convert the uncommitted circuit components into a unique integrated circuit based on his original pattern.

Traditionally, component arrays have been limited in voltage-handling capability to less than 30 volts. The ULN-2350C and ULN-2351C component arrays overcome this limitation, and provide features not found in other arrays.

CHIP FEATURES

One of the goals of laying out the arrays was to enable the user to design a semi-custom integrated circuit without concern over how to protect the circuit from destructive transient voltages. For example, the arrays' power transistors were designed to meet present automotive "load dump" requirements without the usual Zener clamp diode. Design rules for layout and the manufacturing process were developed for a BV_{CES} of greater than 80 volts.

Dielectrically isolated thin-film polysilicon resistors were chosen for the major portion of the resistive element, along with a complement of diffused resistors. Among advantages of thin-film resistors are an inherent ability to withstand voltage transients of up to 500 volts, and high resistance per unit area. These two properties can be utilized to protect sensitive circuit elements from damage by limiting the peak transient current.

Since thin-film resistors do not form a PN junction during their manufacture and are not polarity-sensitive, protection from inadvertent power supply reversal is achieved without external components.

The total available resistance for the ULN-2350C is 4 MΩ . Previous component arrays of similar chip size, using only diffused resistors, offered a total resistance of approximately 400 kΩ .

The availability of high-value resistors is important in applications requiring low standby current and/or low power dissipation.

Capacitors formed by buried-layer and isolation diffusions, with typical values of 80 pF, were included in the arrays for applications requiring noise suppression and stabilization. The capacitors in the ULN-2350C and ULN-2351C may be paralleled for totals of up to 800 pF and 400 pF, respectively.

In addition to the standard complement of NPN and lateral PNP transistors, vertical PNP transistors were built into the arrays to take advantage of their characteristically high current gain, which can be two to three times greater than that of standard lateral PNP transistors.

Figure 1 shows an example of the utilization of a vertical PNP in a current mirror to decrease the error introduced by base current from 20% to less than 1%.

$$I_0 = I_{REF} - \left(I_{B1} + I_{B2}\right) \qquad I_0 = I_{REF} - \left(\frac{I_{B1} + I_{B2}}{\beta}\right)$$
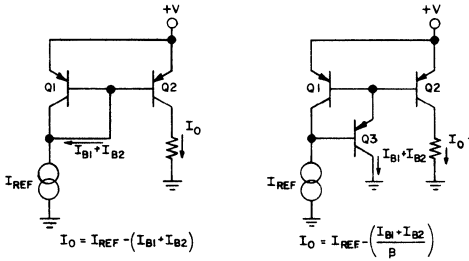
Figure 1

Figure 2 shows application of vertical PNP in a differential amplifier to decrease base drive current requirements.

$$I_B = \frac{I_{C2}}{\beta_1 \beta_2}$$
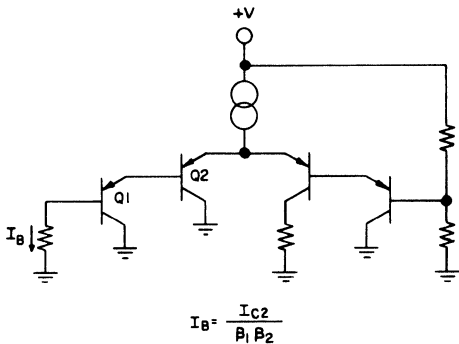
Figure 2

As an aid in designing voltage regulators, emitter-isolation zener diodes with a nominal breakdown voltage of 5.8V are incorporated in the arrays. They are particularly useful with low supply voltage circuits.

APPLICATION

Figure 3 depicts a hypothetical automotive application of a low-voltage integrated circuit that turns on an indicator if the ignition is turned on and the alternator voltage is below some predetermined value.
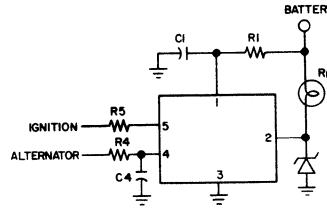
Figure 3

External components protect this circuit from damage by transient voltages encountered in the automotive environment.

AUTOMOTIVE TRANSIENTS

SOURCE	SOURCE IMPEDANCE	AMPLITUDE	DURATION
Air-Conditioning Compressor/ Clutch Coil	250 Ω	± 250 V	1.0 µs
Service Motors	60 Ω	± 32 V	40 µs
Anti-Dieseling Solenoid	200 Ω	± 450 V	22 µs
Alternator Load Disconnect "Load Dump"	0.1 Ω	80 V	200 ms

To protect the supply pin, a low-value resistor ($R_1 = 500\,\Omega$ to $1\,k\Omega$), and a large value capacitor ($C_1 = 1\ \mu F$ to $500\ \mu F$) are used to supress the

transients. The power transistor driving R_L is normally protected with a Zener diode. Pins 4 and 5 are protected from transients by current-limiting resistors R_4 and R_5. In addition, the sense input, pin 4, requires a capacitor, C_4, to form a low-pass filter to ensure rejection of noise pulses.
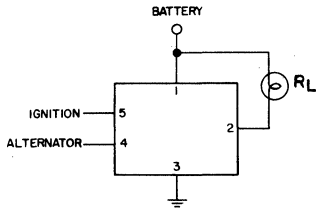
Figure 4

Figure 4 shows the high-voltage array performing the same function; all external protection components have been eliminated.

The actual circuit, shown in Figure 5, demonstrates the design's self-protective properties.
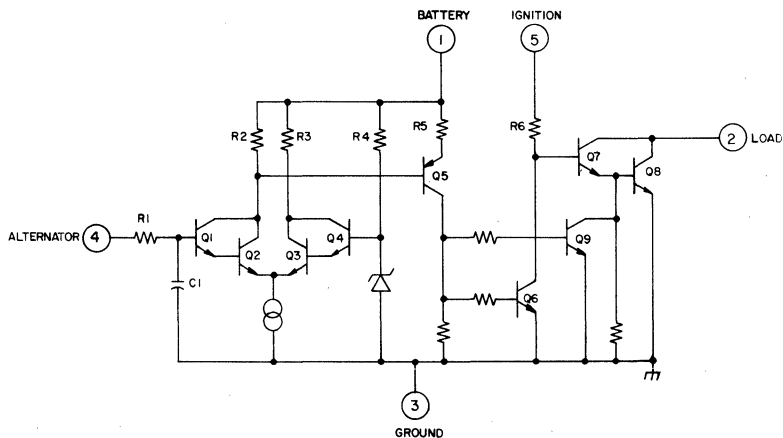
Resistors R_1 - R_6 limit the current through transistors Q_1 - Q_5 during a transient. This protection cannot be achieved with diffused resistors because of their low breakdown voltage ratings.

The output driver Q_7, Q_8, with a BV_{CES} of greater than 80 volts, is capable of withstanding the load dump transient. Voltage transients of greater magnitude are usually accompanied by high source impedance that limits the current.

The load connected to pin 2 limits the current in the event of battery reversal.

Capacitor C_1 supresses noise at pin 4 that could cause the lamp, such as R_L of Figure 4, to turn on erroneously.

CONCLUSION

Although an automotive application is presented above, the arrays' high-voltage capabilities can be used in other noisy environments and in interface circuits such as motor drivers and display drivers.

Figure 5

CUSTOM BIPOLAR INTEGRATED CIRCUITS

FOR AUTOMOTIVE APPLICATION

Here is a manager's overview of how to use bipolar integrated circuits (ICs) for a custom approach to an automotive system application. After selecting the IC technology and establishing the application specifications, the project will follow a basic development cycle. The schedule of events that take place is basic to all custom bipolar ICs for automotive applications. The cycle starts with selection of semiconductor supplier and ends with a reliable cost effective, custom bipolar IC in production several months later. Reaching a successful conclusion requires considerable positive interaction between systems manager and semiconductor supplier.

The first step is to determine that customizing a system is cost effective versus using standard "off-the-shelf" components. In conjunction with this, the manager will determine the extent of system integration desired, the type of interconnect needed and, to a broad extent, the semiconductor packaging.

The reliability level that must be met should be established at the beginning of the program. The reliability specifications have a <u>direct</u> <u>effect</u> on the cost of a device. This must be taken into consideration at the very beginning of the design. The phrase "reliability is designed in -- not tested in" is as true in the semiconductor as the vehicle brake system.

From a system point of view, is there any advantage to having one "large" custom device, versus having two or more "building block" devices which could be used in other or future systems? The "building block" approach will <u>usually</u> cost more (on stand alone

basis) at the system level. Application in other systems has the added advantage of lower overall tooling costs, development times, and economics of higher run rates.

The manager needs to determine the amount of lead time his project has available. The development of a custom IC takes 7 to 9 months, and another 3 months to achieve production buildup. This lead time alone may force the project to use available standard circuits.

Other questions which must be addressed are how many sources will be required and, with this, what is the risk of the parts <u>not</u> being interchangeable? Interchangeability can be a problem, especially with custom circuits where differing semiconductor technologies provide substantially different performance characteristics. Linear circuits, even when the technologies are "identical", can behave entirely different in an application. It is highly desirable to stay with "identical" technologies for all

	CMOS	PMOS	BIMOS	BIPOLAR	BIPOLAR I²L
Power per Gate	1 uW – 10 mW	200 uW – 10 mW	1 uW – 10 mW	2.5 uW – 10 mW	0.5 uW – 2.5 mW
Output Drive	5 mA	10 mA	1A	1A – 4A	1A – 4A
Timing Accuracy	Fair	Poor	Fair	Excellent	Excellent
DC Noise Immunity	Excellent	Fair–Good	Excellent	*	*
Device Diversity	Fair	Poor	Excellent	Excellent	Excellent
Supply (Max. Typ)	20V	30V	Logic 15 V Output 85 V	35V – 100V	Logic 10 V Output 85 V
Logic Density	Med–High	High	Medium	Medium	High
Process Complexity	6 Masks	4 Masks	11-12 Masks	6-8 Masks	6-7 Masks

* = Design dependent, normally excellent but requires additional circuitry

Figure 1

TECHNOLOGY COMPARISONS FOR AUTOMOTIVE ELECTRONIC SYSTEMS

suppliers of a given circuit. Almost all suppliers have their own process variation within a given technology so the term "identical" must be used with caution. Concentrate on defining the system's electrical, environmental, and mechanical limits, and establish a broad specification to achieve this end.

Once the decision has been made to customize, the next problem is getting the desired function within an acceptable schedule. At this stage the systems manager loses some control over the program's success, since there is a "new member" in the design and development team – the semiconductor supplier. The supplier can be another department or division within a vertically integrated company, however, most of the time this will be an "outside" supplier.

The larger or older semiconductor companies doing custom work will have several semiconductor technologies in production;the medium sized companies,

two or more; and the smaller suppliers generally concentrate on one technology. Today there are two popular technologies available (each having wide variations) – MOS and bipolar. MOS is suited for digital only applications (see Fig. 1), and bipolar for digital or analog (linear) amplification, I²L (analog/ digital) and power handling capability. MOS usually requires external (to the package) buffers and drivers. Bipolar devices normally interface directly with lamps, solenoids, motors, relays etc., and will have the drivers "on chip" requiring fewer external components. An alternate choice for certain applications is BiMOS which is the combination of MOS and bipolar on the same chip.

The biggest feature of MOS is its ability to perform many functions using a very small device. One of the main advantages to using a bipolar technology (without sacrificing performance) is its power

handling capability and high voltage tolerance. In reality, future vehicles will probably have both technologies on board since most microprocessors under consideration use a MOS technology with the interfaces to the microprocessor being bipolar.

Circuits can be designed to handle all present transient conditions, load dump, reverse battery, etc. However, most "off-the-shelf" standard ICs were not designed to handle these conditions, and require added discrete (diode and resistor) protection. Fortunately there are bipolar circuits, designed specifically for automotive use, that have the required "bullet proof process". These devices have established a bench mark from which future design and reliability levels can be accurately predicted.

Ideally a new project will be one of a series of previous custom circuits with the selected supplier(s). If the custom project is the first, then it will be necessary to seek out and establish a positive working relationship with a supplier(s) having the required expertise. The emphasis is on a positive relationship - for the semiconductor supplier is, as mentioned previously, a member of the design team. The success of the project is directly related to the relationship of the two organizations. Each team member knows their own disciplines best, and when brought together always require tradeoffs and compromise in order to get the best possible circuit design at the lowest possible cost. System cost effectiveness will be determined by the producibility of the IC, long term reliability, and system design. The unit cost for any custom IC

can, at best, only be estimated at the beginning of a project. This cost is based on the system requirements specified at the start of the project. Tightening of limits, addition (or deletion) of functions, and changes in electrical or mechanical specifications will have a very direct bearing on unit cost. The entire design team (systems manager and semiconductor supplier) must try to make all system trade-offs during the system design phase, and minimize any changes to the IC once started. If changes must be made, they should be during the IC design phase, for once beyond this there is a heavy penalty to schedule (and cost). This will be discussed to a greater extent later.

If the systems manager has selected an IC supplier from previous projects, then some of the unknowns will be eliminated. Also, previous program successes will give a guide as to how long the project realistically will take. In any event, several key steps will take place in the
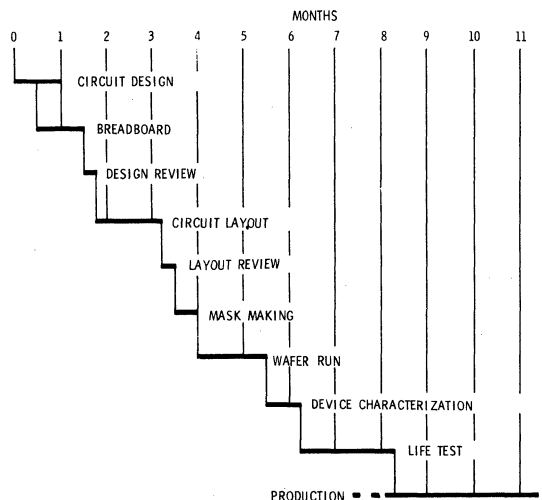
Figure 2
TYPICAL BIPOLAR IC DEVELOPMENT CYCLE

development of the custom bipolar IC, each with its own cycle and problems.

CUSTOM BIPOLAR IC DEVELOPMENT
(See Fig. 2)

All of the following development steps would apply to MOS technology with variations only in device character- istics.

1. Selection of Semiconductor
   Supplier
will be performed on many variables, and is beyond the scope of this paper. However, previous comments on working relationship and supplier expertise in automotive circuits should be key elements in the selection process. Some other points that need to be determined of any potential supplier:

   a. Stability - Financial and
      Workforce
   b. Volume Capability - for
      Present and Anticipated
      Quantities
   c. Basic Packaging Capability -
      IC, Module, etc.
   d. Test Capability - IC
      Module, etc.

A full and complete review of system, electrical and mechan- ical specifications along with quality requirements should be performed by both parties before contract finalization.

An IC supplier unfamiliar with automotive requirements may unknowingly accept a contract that has "hidden" costs which could result in the develop- ment of an unprofitable part. The prudent systems manager will make certain the IC supplier fully understands the system and contract requirements.

3. Circuit Design will ultimately determine the perfor- mance of the IC, the cost and long-term reliability. It is during this phase of the devel- opment that the greatest inter- action should take place. When this stage is reached, the system (custom IC) specification should be "frozen". Once the IC design is finalized and com- mitted to "lay-out" (step 6) only minor changes can be made without impacting the entire schedule and cost.

Trade-offs may be required in the system due to findings during the IC design. They will be verified during the simu- lation or breadboard phase. Most automotive electronic systems can be "breadboarded" (step 4) with discrete semi- conductors ("kit parts" from the bipolar process to be used on final circuits). If major trade-offs are required they must be made here.

The systems manager could breadboard his own IC with the same discretes (supplied by supplier to do final design analysis - do not use another supplier's breadboard components as the process can be different). This breadboarding can be very useful during system definition and development. The systems manager can optimize the system prior to committing the project. Here again is an example of having a positive working relationship with the selected supplier(s), as these components are not com- mercially available. A review of the IC design should be made at this point, and any system of IC modification implemented.

4. Breadboard layout is actually performed during, and in conjunction with the IC design (step 3). Some suppliers may use computer simulation from component models in conjunction with CAD (Computer Aided Design). If the CAD method is used, it is more difficult for the systems manager to review the customized design. The cell (component models) library is useful only when using the same CAD. In addition, (unlike some MOS technologies) the cells will be designed for the supplier's bipolar process, and therefore possibly proprietary to the semiconductor supplier.

A good breadboard is a very powerful tool and has often brought out unknown system problems during circuit design evaluation.

5. Design Review is the last convenient point in the design process to make modifications. At this step the design is reviewed in detail. The performance of the circuit is compared, via the breadboard, to the design objectives. The systems manager should make it a point to attend this session.

The circuit designer will have selected a particular bipolar process to best meet the system requirement. The interface (input or output) component from transients, accidental grounding, load dump, etc. Because of these requirements the designer will configure the component layout to handle these conditions. Few standard bipolar parts can meet all of these conditions, and will require external discrete protective circuitry.

Therefore, the systems manager, should determine the semiconductor suppliers' capabilities in this area during supplier selection. The inherent reliability of the system is improved with the fewest possible discrete components per system.

Most standard "off-the-shelf" ICs have breakdown voltages in the 20V DC range, while a bullet-proof automotive IC should be at least 50V DC. Note that this applies to the interface components within the IC. The signal processing section of the IC need not have high breakdown capability. This allows the most efficient use of area on the layout as high-voltage breakdown components and output drivers tend to be very large in comparison.

Design reviews are normally attended by engineers from all key facets of the semiconductor operation; production, mask making, wafer processing, packaging, test, reliability, etc. The design engineer(s) responsible for the custom IC(s) present the design to a critical review by all of these departments. Each of these departments must agree that the design is sound, does not violate any rules, and is manufacturable. At this point the designer will commit the custom design to layout.

6. Circuit Layout can be performed by either hand drafting or through the use of computer aided design. The use of either method generates "artwork" (every designer considers his work a masterpiece), which is a composite drawing of each "mask level". The layout artwork will be drawn

11

at several hundred times (typically 254X or 508X) the final IC's size. The actual magnification is dependent on the "die" size (once produced, the unpackaged individual circuit is referred to as a die or chip) or capability of photo reduction equipment. The CAD circuit layout method closely parallels the manual method but is usually completed faster.

In order to efficiently use CAD there first must be a library of devices (transistors, diodes, etc.) compatible with the bullet-proof process. This library can have standard "cells" of differing functions such as; drivers, gates, flip flops, etc. These will be used, as needed, by the CAD operator to integrate the required function. A CAD circuit design is better suited for digital than linear, especially where both are part of the circuit.

Caution: If a cell library is not already established, it must be created and this is very time consuming. If done properly, the cells will have been life tested (usually in IC form), and will have been interconnected previously to make certain that they are compatible. If the cells do not already exist, use the more familiar hand layout method. If used properly, CAD can be a very powerful tool, or a very expensive draftsperson.

7. Layout Review is attended by basically the same group as Design Review. At this juncture the layout is subjected to a careful examination of layout rules, component placement, test points (for wafer probe and evaluation prior to packaging) and conformity to the circuit design.

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The application of ICs to the automotive electrical system dictates special test requirements. Therefore, special wafer and package test requirements will be "finalized" at this point. This will mean building and fixturing the specialized interface hardware for the automatic testers. Since most of the general IC testers do not have high-voltage capability, special interface boxes must be created to do the required tests. This can cause incoming inspection problems for systems managers, as it is highly unlikely that the test systems will be exactly the same. For this reason the special interface boxes created by the IC supplier will not be usable by the systems manager. Therefore, it is vital that there be a "good" specification established so that differing test equipments will be able to do the same tests and obtain correlatable results.

8. Mask Making is performed next through one of several methods. If a CAD system was used, then the mask levels will be generated directly or by cutting Rubylith.® (same as doing a printed circuit board), which will be peeled by hand. These systems are fast, compared to hand cutting, but are not always available to the designer (especially. if the CAD was not used). A common approach is to use a digitizer, with hand-drawn artwork, which normally feeds an X-Y plotter that cuts the Rubylith. The Rubylith is then peeled by hand. In addition, the digitized artwork can be fed to a "reticle" generator which eliminates the Rubylith and required photo-reduction steps. A reticle is the mask (one level master

and is 10X the finished die size). The reticle will be "step-and-repeated" on the final working "plates" for the individual wafer masking steps.

9. Pilot Wafer Run will be made following the mask-making operation. The systems manager should follow this run with tempered enthusiasm.

The first run is actually a circuit "debug" step. For when it is checked out there are usually changes or error corrections to be made in the circuit, masks, and/or process. Therefore a second wafer run will be made following any changes. This second run is very important, since it will provide working parts for both the systems manager and semiconductor partner. The supplier will get the first "hard" yield information against the target specification. Up to this point the supplier has used experience to project yields which determine cost (this will be covered in later sections).

The final pilot run will be packaged, usually on an engineering assembly line, and submitted to initial electrical evaluation. Depending on the relationship between the partners, advance parts may be obtained by the systems manager. The semiconductor supplier will want to perform a complete device (IC) evaluation, and will be reluctant to provide parts until the evaluation and characterization is complete.

10. Device Characterization will be performed to ensure the custom bipolar IC meets the initial target specification. Depending on the circuit complexity, the characterization

can be very time consuming. However, it is essential to both the systems manager and semiconductor partner for slightly different reasons.

The semiconductor manufacturer is looking to make certain the custom IC meets the target specification, or to what extent it does not meet the specification. In the first case, the overall yeild can be projected with a much higher degree of accuracy. In the second case (some parameter is out of specification) corrective action is required. This may entail a simple mask or process change, or a major redesign. However, before this is initiated the partners should get together to determine if the part will work satisfactorily within the system. If it will meet system objectives, the specifications may be relaxed (step 11), then it's possible to derive the needed yield information.

The systems manager is concerned with the custom IC's performance within the system. Therefore it is essential that the custom IC be evaluated within the system during the system characterization. Differences may appear between the breadboard's operation and the "equivalent" IC due to capacitance, layout, and discrete versus integrated components (parasitics). If a careful system evaluation and design was performed at the start of the program, few surprises will develop.

Following system and IC charactertization it is essential to review and finalize any differences in specifications and parametrics. Remember that this is a partnership with a

11

common objective of selling systems, so approach the next phase with compromise in mind.

11. <u>Specification Review</u> takes place following successful pilot run(s) and product characterization. It is very important that the systems manager approach this as an opportunity to improve performance, manufacturability, reliability, and yield. As with any system the ultimate in performance and cost is a result of a series of tradeoffs. This stage in the system's development is no different.

The IC characterization provided a baseline with respect to the parametric distribution. Hopefully the IC comes into the center of the specification limits so that 100% of the product will be usable. In reality this seldom happens. There are so many variables in process that any given lot of parts will have a slightly different distribution. This results in throwing away product that does not meet the desired specification (yield loss), and shipping that which meets the limits (shippable yield).

At the beginning of the program the systems manager selected a partner who projected a satisfactory unit based on a specification and anticipated shippable yields. A product was developed and resulted in an IC that has a certain character. The semiconductor manufacturer will be able to make recommendations, based on the characterization data, for ways to improve performance and yield. Every percentage point of yield loss affects shipments and cost. Therefore, it is definitely to the systems manager's benefit to work towards the highest practical shippable yield.

Every engineer uses guard bands. Realistic guard bands are prudent and necessary to take care of a product's manufacturing variation. However, every guard band affects yield and is reelected in unit and system cost.

It is not possible to give exact comparisons of the inter-relationship of parameters to yield. However, it is to the systems manager's benefit to be flexible on "non-critical" parameters as the final IC will likely differ from the target specification following characterization. This happens because of the layout and interaction of active and passive components on the custom IC. It is not possible to predict with 100% confidence the behavior of an integrated system versus the discrete version. This is where the systems manager must rely on the semiconductor partner's experience and recommendations.

12. <u>Life Test</u> is essential for any new IC to determine circuit integrity and establish failure rates, etc. Normal accelerated life test procedures are adequate for bipolar ICs. The testing should be run only on parts produced with production tooling and assembly lines. Test samples should come from the same assembly line as will be used for the volume production, and the parts should be as representative of future production as is possible. If a common failure analysis should be performed to determine cause. Corrective action will be determined following the analysis.

If a major change is made (as a result of the life test) to the mask set, the part should be put through a new operating life test. Changes in test

procedures or limits will not normally require a new life test. The systems manager must keep in mind that a normal life test is 1000 hours, and takes six weeks of oven time with two weeks on each end to take data. This time should be factored into the development schedule as a normal part of any custom program.

Historical data on the bipolar process used for the custom IC is very useful in predicting long-term failure rates. This also will provide guidance in supplier selection. An established supplier of automotive ICs will have a history on similar devices which can be used to predict system life.

13. Release to Production of the custom IC can be achieved following, or even prior to completion (dotted area Fig. 2) of successful life testing. However, release prior to completion of life testing is very risky before 500 hours. Once released, it will take about sixteen weeks to achieve full production. Since the production cycle is so long, the system manager should consider that any change to the IC may affect a considerable quantity of product. Therefore, such changes can be very costly.

1. Selection of Semiconductor Supplier
2. Contract Definition and Negotiation
3. Circuit Design
4. Breadboard
5. Design Review
6. Circuit Layout
7. Layout Review
8. Mask Making
9. Pilot Wafer Run
10. Device Characterization
11. Specification Review
12. Life Test
13. Release to Production

SUMMARY

An overview of how to use a custom bipolar approach to a system requirement. The systems manager needs to determine when it is cost effective to either customize or use standard "off-the shelf" components. The manager needs to decide how much of the system to integrate. Should it be in one package, or broken up into several packages? What lead time is available and when will the electrical, environmental, and mechanical specification limits have to be frozen? How many sources will be required, and what is

the risk that parts will not be interchangeable? The preceding is a partial list of questions that have to be answered for any tentative "custom" project. The answers will affect the choice of technology, device development time, system development time, etc., all of which affect cost and have a direct bearing on reliability and program success.

Once the decision has been made to go "custom" the next problem is getting the desired function, within an acceptable schedule. At this stage the systems manager loses some control over his program's success, because at this point of the program there is a "new" member in his design team - the semiconductor supplier.

Ideally the program will be one of a series of customizations, and will have had a positive relationship with one or more of the suppliers that have the required expertise. Previous program successes will give a guide as to how long the project will take. In any event, the following major steps will take place, each with its own cycle and problems:

CONCLUSION

As previously indicated, the semiconductor supplier should be considered as a member of the project team. As such it is highly desirable to work closely with him on an open and frank basis. Remember, the circuit is a result of the designer's interpretation of the specification's basic system needs.

Assuming the systems manager has chosen the correct supplier; defined and brought to production a system that the final customer will buy; overcome all the major and minor problems during the development period; the systems manager may find it cannot be made for the desired price (because of low yield) and in the required quantities. Therefore, temper enthusiasm for all the latest technologies. Determine at the outset which approach is the best - a custom IC or "discrete" off-the-shelf design, and be flexible on specifications that affect yields. The advertising department will be able to live with either, because after all, it is SOLID STATE ELECTRONICS!!

CUSTOM CIRCUIT DESIGNS

Sprague is active in the design of standard and custom high-volume integrated circuits and subassemblies for both linear and digital applications. A wide range of semiconductor technologies is available to optimize cost and performance. Often, new processes or innovative circuit designs are involved.

Generally, the first concern of a designer of a custom device is one of cost, though performance, reliability, size, and process are also important considerations. Cost is determined by the following factors:

Production Volume: Unit cost is dependent on quantity. A minimum volume of $250,000 per year is required after the initial design and development.

Chip Size: Unit cost is directly affected by chip size, which is related to circuit complexity, output-current and output-voltage ratings.

Test Requirements: Logic, d-c, and static measurements are simple, fast, and inexpensive to perform, while linear measurements such as those for distortion, phase, and noise, may affect production rates and increase cost.

Typical Custom Design Schedule

Task	Time in Weeks
Define Specifications	—
Circuit Design	2 to 20
Breadboard Construction and Analysis	4 to 12
Circuit Layout and Maskmaking	4 to 12
Prototype Processing	3 to 10
Prototype Evaluation	4 to 8
Production Pilot Run	8 to 16
Production Volume	12 to 20

Total 37 to 98 weeks at an engineering cost of between $20,000 and $100,000, not including special test hardware or assembly tooling.

Package: Plastic packages are the least expensive. Cer-DIP packages are less expensive than side-brazed hermetic packages, which are the most costly. Cost also increases with pin count.

Specifications: Well-defined specifications can expedite circuit design. Excessive or arbitrarily tight specifications will reduce yields and increase cost.

Integrated Component Capability

Transistors: NPN—Beta to 300, BV_{CES} to 200 V, f_T to 500 MHz
PNP—Beta to 60, BV_{CES} to 150 V, f_T to 5 MHz
CMOS—V_{TH} 0.8 to 2.5 V, BV_{DS} to 18 V

Resistors: Diffused—5Ω/□, to 100Ω, to 100 V
175Ω/□, to 100 kΩ, to 100 V
Ion Implant—1 kΩ/□ to 4 kΩ/□, to 1 MΩ, 20 V
Thin Film—2 kΩ/□, to 2 MΩ, 250 V
Aluminum—0.025Ω/□, to 1.0Ω, 150 V

Capacitors: Junction—0.1 pF/mil², to 30 pF, 100 V
0.3 pF/mil², to 100 pF, 12 V
0.9 pF/mil², to 300 pF, 6 V
MOS—0.1 pF/mil², to 30 pF, 50 V
0.2 pF/mil², to 50 pF, 20 V

Diodes: Zener—5.7 or 7.0 V, ±0.3 V
Photo—0.5 A/W or >300 nA/fc at 800 nm
Schottky—0.1 to 0.4 V at 1 µA, 0.3 to 0.6 V at 1 mA
Small Signal—BV = 7.0 V

Other: SCRs—to 1 A, to 60 V
PUTs—to 1 A, to 60 V
I²L—Propagation delay typically 100 ns
BiMOS—High-power bipolar plus low-power MOS
Hall Cells—35 mV/kG

Application Areas of Sprague Expertise

Interface—Display drivers, motor/relay/solenoid drivers, Hall cells, opto-sensors

Computer—Peripheral power interface to 200 V or 5 A, video display drivers, SMPS

Radio—A-M, F-M, F-M stereo, communications, A-M stereo

Audio—250 mW to 20 W, mono and stereo

Control—Timers, Hall cells, opto-sensors, switching regulators, motor drivers, PWM

Military—Communications, fuze, interface

Camera—Light integrators, timers, controls

Telecommunications—SLIC, electronic telephones, wireless telephones

Automotive—Controls, monitoring, safety, radio

Transistor Arrays—Small-signal, high-current, SCR, control

General—Sound generators and amplifiers, timers, controls

11

OPTIONAL PACKAGE CAPABILITIES
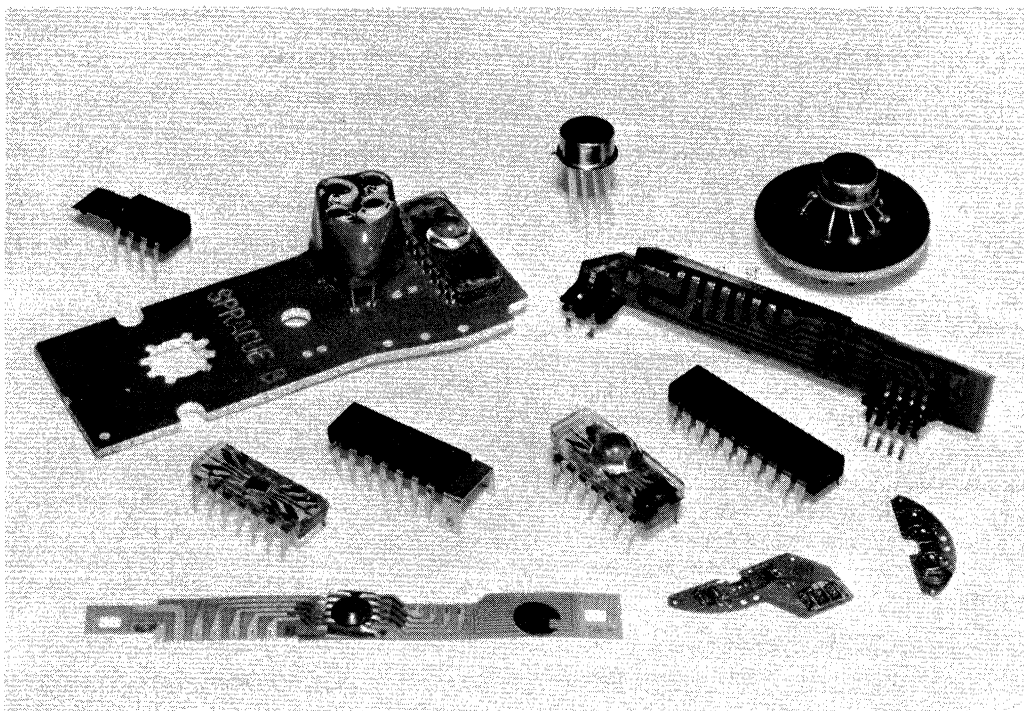
Standard integrated circuits from Sprague Electric Company are most often furnished in packages meeting industry or military standards (JEDEC TO-87, TO-91, TO-99, TO-100, or TO-116, or MIL-M-38510). However, on special order, other packages or assemblies of packaged devices can also be supplied. A few special order devices are illustrated above, including special heat sink tabs, subminiature plastic packages, printed wiring boards, flexible circuits, and complex assemblies. Devices with photodiodes are furnished in clear plastic cases.

SECTION 12—PACKAGE INFORMATION

12

Package Thermal Characteristics

Package Designator	Package Type	Frame Material	$R\Theta_{JA}$† (°C/W)	$R\Theta_{JC}$† (°C/W)
A	14-Lead Plastic DIP	Copper	60	38
A	16-Lead Plastic DIP	Copper	60	38
A	18-Lead Plastic DIP	Copper	55	25
A	20-Lead Plastic DIP	Copper	55	25
A	22-Lead Plastic DIP	Copper	50	21
A	28-Lead Plastic DIP	Copper	40	16
B	8-Lead Semi-Tab Plastic DIP	Copper	75	13*
B	14-Lead Semi-Tab Plastic DIP	Copper	45	13*
B	16-Lead Semi-Tab Plastic DIP	Copper	45	13*
D	3-Lead Transistor	Kovar	300	150
H	8-Lead Hermetic DIP	Kovar	120	40
H	14-Lead Hermetic DIP	Kovar	90	20
H	16-Lead Hermetic DIP	Kovar	90	20
H	18-Lead Hermetic DIP	Kovar	75	20
J	14-Lead Flat Pack	Kovar	140	80
M	8-Lead Mini DIP	Copper	80	55
Q	16-Lead Quad In-Line	Copper	45	13*
R	14-Lead CerDIP	Kovar	75	—
R	16-Lead CerDIP	Kovar	75	—
R	18-Lead CerDIP	Kovar	65	—
W	12-Lead Power Tab SIP	Copper	24	3.0*
Y	3-Lead Transistor	Copper	310	170
Z	5-Lead Power Tab SIP	Copper	40	4.5*

The data given is intended as a general reference only and is based on certain simplifications such as constant chip size, standard bonding methods, and an allowable +150°C junction temperature. Where differences exist, the detail specification takes precedence.
†$G\Theta_{JA} = 1/R\Theta_{JA}$ and $G\Theta_{JC} = 1/R\Theta_{JC}$
*$R\Theta_{JT}$

THERMAL DESIGN FOR
PLASTIC INTEGRATED CIRCUITS

PROPER THERMAL DESIGN is essential for reliable operation of many electronic circuits. Under severe thermal stress, leakage currents increase, materials decompose, and components drift in value or fail. Present-day linear integrated circuits are capable of delivering 5 to 10 watts of continuous power. Previously, such power levels came only with discrete metal can power transistors. It was relatively easy to determine the thermal resistance of these devices and attach a massive heat sink. However, in many markets, economic factors now dictate the use of molded dual in-line plastic packaged monolithic circuits. The guidelines to be discussed will provide the circuit design engineer with information on maintaining junction temperature below a safe limit under worst case conditions.

Design Considerations

Four factors must be considered before the required heat-sinking can be determined. These are:
1. Maximum ambient temperature
2. Maximum allowable chip temperature
3. Junction-to-ambient thermal resistance
4. Continuous chip power dissipation

Maximum ambient temperature for the integrated circuit is normally between +70°C and +85°C and is usually dependent on the case material. In most applications, however, the limiting factor is the associated discrete components and a limit of about +50°C is specified. The maximum allowable chip temperature is usually +150°C for silicon.

Thermal resistance is the all-important design factor. It is composed of several individual elements, some of which are determined by the integrated circuits manufacturer, and some by the user.

Chip Power Dissipation

The chip power dissipation should be obtainable from the manufacturer's specifications. In most applications it is a variable and determined by the user when he specifies the circuit variables.

A typical example is a dual 2-watt audio power amplifier. Power dissipation is determined by the load impedance, the required peak output power, the acceptable amount of total harmonic distortion (THD), and the supply voltage (V_{CC}). This is illustrated in Figures 1-3. Note that for a given supply voltage, the chip dissipation may be greatest at some point below the peak output power rating and must be considered.

As shown in the figures, a peak output power of 2 watts per channel with 3% maximum THD would mean a chip power dissipation of about 2.7 W and a V_{CC} of 15 V with a load impedance of 4Ω, or 1.8 W and 15 V at 8Ω, or 1.4 W and 19 V at 16Ω. In general, the highest load impedance for a given output power is the most desirable (within the output voltage capability of the device).

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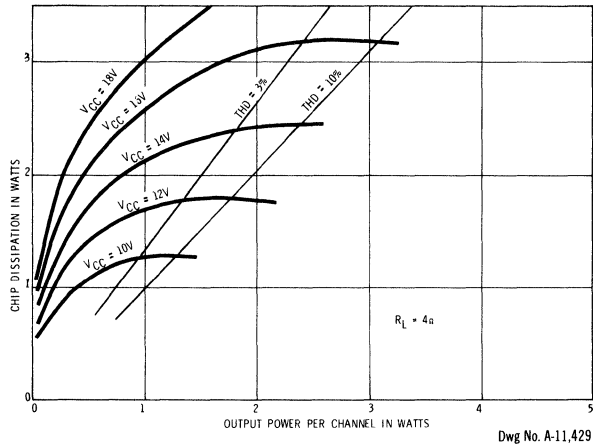
Figure 1
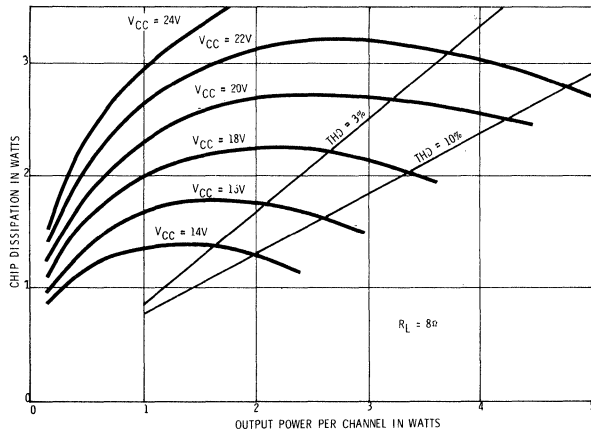
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Figure 2

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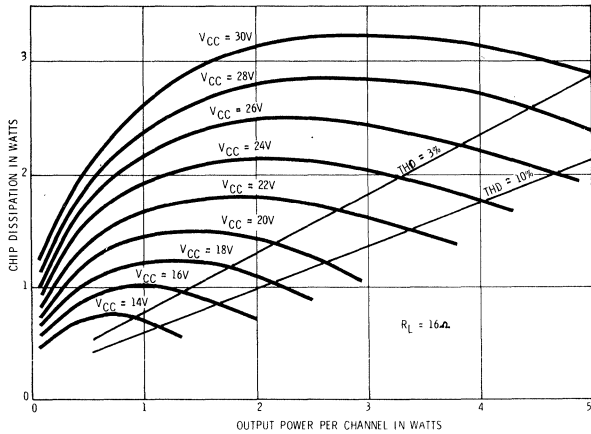
Figure 3

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Heat Dissipation

In any circuit involving power, a major design objective is to reduce the temperature of the components in order to improve reliability, reduce cost, or improve operation. The logical place to start is with the heat-producing component itself. First, keep the amount of heat generated to a minimum. Second, get rid of the heat that must be generated.

Heat generation can be minimized through proper circuit design. Heat dissipation is a function of thermal resistance.

With the typical discrete component, heat dissipation can be accomplished by fastening it directly to the chassis. Dual in-line plastic packaged integrated circuits, however, are quite a bit different. Their shape is not conducive to fastening directly to the chassis, they are normally installed in a plastic socket or on a printed wiring board, and the heat producing chip is not readily accessible.

Some users specify unusual packages so as to get the heat sink as close as possible to the chip and/or provide an attachment point for an external heat sink. A common factor in many of these special designs is that the lead frame is an integral part of the heat sink.

Since the plastic package may have a thermal resistance of between 50 and 100°C/W and the lead frame a thermal resistance of only 10 to 20°C/W, this would seem like the best route to go.

Standard Packages

The most common lead frame material has been Kovar (an iron-nickel-cobalt alloy). Its coefficient of expansion is close to that of silicon thereby minimizing mechanical stresses. However, Kovar has a relatively high thermal resistance and consequently is not suitable for standard lead frames in high power dissipation circuits. For these applications, copper or copper-alloy lead frames should be used. Additionally, some type of added heat sinking may be necessary. Thus lead frame configurations are being altered from the standard 14-pin or 16-pin designs.

Rapidly becoming an industry standard is the "bat-wing" package. This package is the same size as a 14-pin dual in-line package, but the center portion of the frame is left as tabs, measuring about ¼" square. These tabs can be soldered, welded, or bolted to a heat sink, or inserted directly into some sockets. The worst case thermal resistance of various lead frames (Θ_{JC}) is given below.

Lead Frame	Thermal Resistance
14-pin Kovar	47°C/W
14-pin copper	19°C/W
"Bat-wing"	11°C/W

Which Heat Sink?

If the integrated circuit manufacturer has done his job well, the chip-to-ambient thermal resistance will be minimized for maximum chip power dissipation. It would appear that even the Kovar lead frame would be adequate for most applications. However, the total thermal resistance (Θ_{JA}) is also dependent on a stagnant layer of air at the lead frame-ambient interface which will support a temperature gradient. The total thermal resistance of a non-heat sinked dual in-line plastic package is therefore much higher. Since air is a natural thermal insulator, maximum heat transfer is through convection and the total thermal resistance will decrease some at high power levels.

Lead Frame	Total Thermal Resistance	Max. Power Diss. (W) at 50°C T_A, 150°C T_J
14-Pin Kovar	120°C/W	0.83
14-Pin Copper	72°C/W	1.39
"Bat-Wing"	50°C/W	2.0

Ignoring any safety margin and device performance, even the "bat-wing" is now only barely adequate for most applications. The obvious solution is the use of an external heat sink.

12

Referring to Figures 4 and 5, the thermal resistance requirement of the heat sink is found at the junction of the specified chip power dissipation and maximum ambient temperature. These curves are typical of those furnished in many monolithic integrated circuit data sheets. Actual performance in a specific situation depends on factors such as the proximity of objects interfering with air flow, heat radiated or convected from other components, atmospheric pressure, and humidity. A good safety factor is therefore in order.
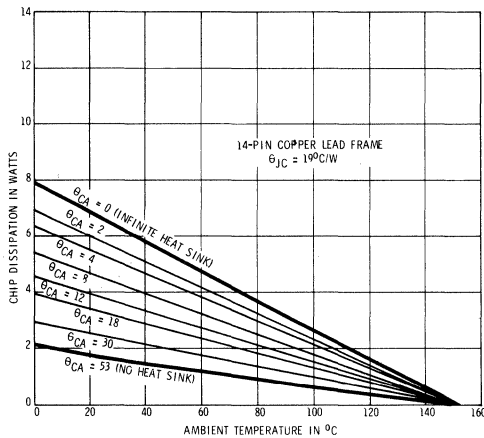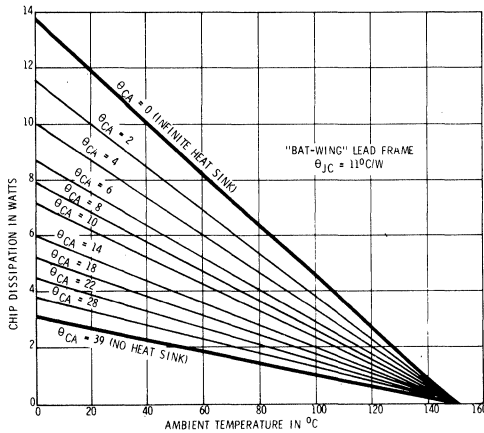
Heat sinks for plastic dual in-line packages can be of almost unlimited variety in design, material, and finish. Economics will normally play a very important role in the selection of any heat sink.

The least expensive and easiest to fabricate heat sink is the plain copper sheet. It is also very effective in reducing the total thermal resistance. The necessary dimensions can be obtained from Figure 6. These heat sinks are square in geometry, 0.015 inches thick, mounted vertically on each side of the lead frame, and with a dull or painted surface (Figure 7). The heat sinks should be soldered directly to the lead frame (approximately 0.3°C/W interface thermal resistance).

The plain copper sheet heat sink is also available commercially and may be less expensive than in-house manufacture. Two standard types are the Staver V7 and V8.

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Figure 4

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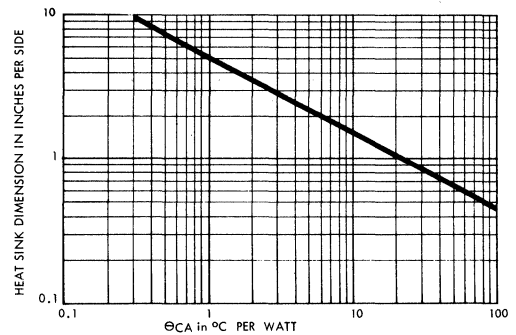
Figure 5

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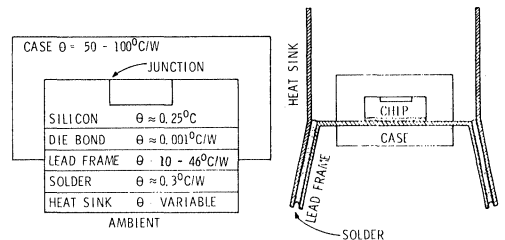
Figure 6

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Figure 7

12—6

Heat Sink Finishes

Although plain copper is an effective heat sink, it is sometimes desirable to have something that is more appealing to the eye. For this reason, and others, many heat sinks are either painted or anodized.

The most common finish is probably black anodizing. It is economical and offers a good appearance. The black finish will also increase the performance of the heat sink, due to radiation, by as much as 25%. However, since anodizing is an electrical and thermal insulator, the heat sink should have an area free of anodize where the heat-generating device is attached.

Other popular finishes for heat sinks are irridite and chromic acid dips. They are economical and have negligible thermal and electrical resistances. These finishes, however, do not enjoy the 25% increase in performance that a dull black finish has.

Forced Air Cooling

The performance of many heat sinks can be increased by as much as 100% by forcing air over the fins. Where space is a problem, the cost of a small fan can often be justified. If a fan is required for other purposes, it is advantageous to place the semiconductor heat source in the air flow. A rule-of-thumb is that semiconductor failure rate is halved for each 10°C reduction in junction operating temperature.

Chip Design

Proper thermal design by the integrated circuit user can reduce the operating temperature of the semiconductor junction. However, the minimum chip temperature at any power level is determined solely by the device manufacturer. For this reason, care must be taken in choosing the manufacturer. "Exact equivalent" integrated circuits are not necessarily identical. Electrically and mechanically they may be the same, but thermal differences can mean that "identical" audio power amplifiers will not put out the same power without exceeding the rated junction temperature.

The circuit manufacturer must optimize his chip design so that component drift is minimized and/or equalized so that rated performance can actually be obtained under maximum thermal stress.

Note in Figures 8 and 9 that the Darlington input differential pairs are cross-connected so as to minimize differences in gain as a function of output transistor power dissipation. Transistor Q_4, being closest to the output power transistors, is naturally the hottest; Q_3 is a degree or two cooler; Q_1 and Q_2 are about equal and midway between Q_3 and Q_4. The gain of the Q_1-Q_2 Darlington pair is about equal to the gain of Q_3-Q_4 at all output power levels because of careful thermal design.
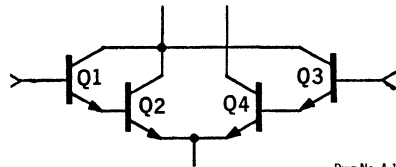
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Figure 8

Figure 9

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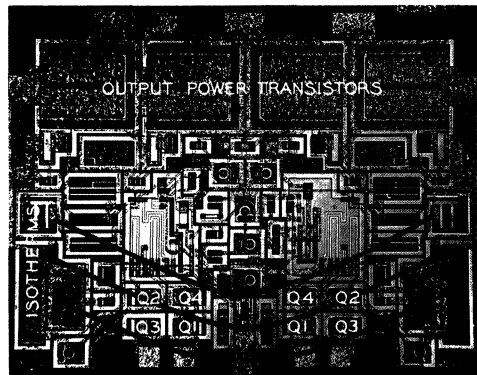
In certain specialized applications, thermal coupling can be used to a distinct advantage. Experimentally, thermal coupling has been used to provide a low-pass feedback network which otherwise could be obtained only with very large values of capacitance.

The foregoing discussion has covered the average thermal characteristics of today's dual in-line plastic integrated circuits. The specific devices will vary with the different packages and bonding techniques employed, but the concepts will remain the same.

APPENDIX

The following is intended to review terminology and compare thermal circuits with the more familiar electrical quantities.

The first law of thermodynamics states that energy cannot be created or destroyed but can be converted from one form to another. The second law of thermodynamics states that energy transfer will occur only in the direction of lower energy. In the semiconductor junction, the electrical energy is converted to thermal energy. Since no heat will be stored at the junction, the heat will flow to a lower temperature medium, air. The rate of heat flow is dependent on the resistance to that flow and the temperature difference between the source and the sink.
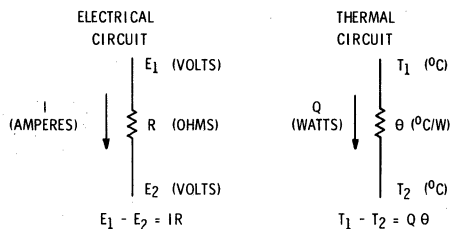
Figure 10

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This thermal electrical analogy is convenient only for conduction problems where heat flow and temperature obey linear equations. The analogy becomes much more complex for situations involving heat flow by convection and radiation. Where these two modes are not negligible, they can be approximated by an equivalent thermal resistance. If ignored, the error introduced will only improve the device reliability.

A simplified thermal flow diagram of a molded dual in-line package and heat sink is shown. The

thermal resistance of the lead frame-heat sink-ambient is shown as a variable resistor, because this is under the control of the user and may be varied over a considerable range.

$$T_J \approx T_A + Q \, (\theta_{JC} + \theta_{CS} + \theta_{SA})$$
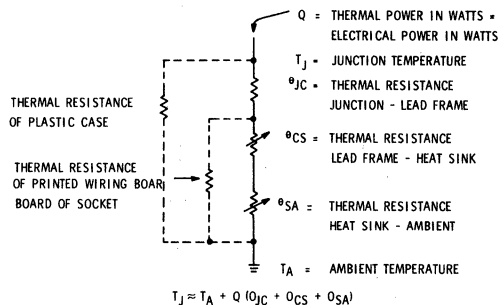
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Figure 11

Material	Thermal Resistance in °C/W for Unit Area/Unit Length
Silver	0.09
Copper, Annealed	0.10
Gold	0.12
Beryllia Ceramic	0.20
Aluminum	0.20
Brass (66 Cu, 34 Zn)	0.40
Silicon	0.50
Germanium	0.70
Steel, SAE 1045	0.80
Solder (60 Sn, 40 Pb)	1.5
Alumina Ceramic	2.0
Kovar (54 Fe, 29 Ni, 17 Co)	3.0
Glass	40
Epoxy	40
Mica	50
Teflon PTFE	200
Air	2000

Computing IC Temperature Rise

Heat is the enemy of integrated circuits—particularly power devices. Here's how to use thermal ratings to determine safe IC operation.

Why IC Temperatures Rise

IC temperature T_J is determined by ambient temperature T_A, heat dissipated P_D, and total thermal resistance R_θ. This total thermal resistance is comprised of three individual component resistances: chip R_C, lead frame R_L, and heat sink R_S.

EXCESSIVE heat shortens the life of an IC and reduces its operating capability. Until recently, ICs were capable of operating only in low-power applications requiring perhaps a few milliwatts of power. But now, new ICs handle several hundred milliamperes and drive devices such as relays, solenoids, stepping motors, and incandescent lamps. These high power levels may increase IC temperatures substantially and are capable of destroying devices unless appropriate precautions are taken.

Thermal Characteristics

The thermal characteristics of any IC are determined by four parameters. Maximum allowable IC chip junction temperature T_J and thermal resistance R_θ are specified by the IC manufacturer. Ambient temperature T_A and the power dissipation P_D are determined by the user. Equation 1 expresses the rela-

tion of these parameters.

$$T_J = T_A + P_D R_\theta \qquad (1)$$

Junction temperature T_J usually is limited to 150°C for silicon ICs. Devices may operate momentarily at slightly higher temperatures, but device life expectancy decreases exponentially for extended high-temperature operation. Usually, the lower the junction operating temperature, the greater the anticipated life of the IC.

Ambient temperature T_A is traditionally limited either to 70°C or 85°C for plastic dual in-line packages (DIPs) or 125°C for hermetic devices. Again, the objective is to operate at as low a junction temperature as practical.

Thermal resistance R_θ is the basic thermal characteristic for ICs. It is usually expressed in terms of °C/W and represents the rise in junction temperature with a unit of power applied in still air. (The reciprocal of thermal resistance is thermal conductance, or derating factor,

12

G_θ expressed as W/°C.) Thermal resistance of an IC consists of several distinct components, the sum of which is the specified thermal resistance. For a typical IC, these components of thermal resistance are 0.5°C/W per unit thickness of the silicon chip, 0.1 to 3°C/W per unit length of the lead frame, and up to 2,000°C/W per unit thickness of still air surrounding the IC. DIPs are used more than any other type of packaging for ICs and newer copper-alloy lead frames provide a superior thermal rating over the standard iron-nickel-cobalt alloy (Kovar) lead frames. However, power ICs are also available in other packages such as flat-packs and TO-type cans.

The power P_D that an IC can safely dissipate usually depends on the size of the IC chip and the type of packaging. Most common copper-frame DIPs can dissipate about 1.5 W, although some special-purpose types have ratings as high as 5 W.

Total IC power to be dissipated depends on input current, output current, voltage drop,

Finding Safe Operating Limits

Here's how to calculate the safe operating limits for an IC. The first two examples are simple calculations involving maximum allowable power and are straightforward. The third and fourth examples are more complex and involve logic power, output power, and duty cycle.

Problem: Determine the maximum allowable power dissipation that can be handled safely by a 16-lead Kovar DIP with an R_θ of 125°C/W in an ambient temperature of 70°C.

Solution: From Equation 1, the maximum allowable power dissipation P_D for this IC is

$$P_D = \frac{150°C - 70°C}{125°C/W}$$

$$= 0.64\ W$$

Problem: Determine the maximum allowable power dissipation that can be handled by a 14-lead copper DIP

with a derating factor G_θ of 16.67 mW/°C in an ambient of 70°C.

Solution: Since the derating factor G_θ is the reciprocal of thermal resistance R_θ, the maximum allowable power dissipation P_D from Equation 1 is

$$P_D = (150°C - 70°C)$$
$$\times (16.67\ mW/°C)$$
$$= 1.33\ W$$

Problem: Calculate the maximum junction temperature for a quad power driver with a thermal resistance of 60°C/W in an ambient of 70°C and which is controlling a 250 mA load on each of the four outputs.

Solution: To determine the maximum (worst case) junction temperature for this IC, the maximum total power dissipation must be determined from the data listed on the IC data sheet. The specifications are usually listed as typical and minimum or maximum values. It is important to use maximum voltage and current limits to insure an adequate design. Common maximum values for an

and duty cycle. Thus, for many industrial digital-control ICs, logic-gate power P_l (typically less than 0.1 W) and output power P_o must be determined to find the total power to be dissipated. Total power dissipation for these logic devices is the sum of P_l and P_o.

$$P_l = n(V_{CC}I_{CC}) \tag{2}$$

$$P_o = n(V_{CE(SAT)}I_C) \tag{3}$$

where V_{CC} = logic-gate supply voltage, I_{CC} = logic-gate ON current, $V_{CE(SAT)}$ = output saturation voltage, I_C = output

Measuring IC Temperature

Sometimes IC junction temperature cannot be calculated readily and instead must be measured. Measurement should be made when there is insufficient data with which to calculate, when the effects of external variables such as forced-air cooling or enclosure size must be determined, or as a check on the manufacturer's specifications regarding package thermal resistance.

The most popular technique for measuring IC temperature uses the characteristic of a diode to reduce its forward voltage with temperature. Many IC chips have some sort of accessible diode—parasitic, input protection, base-emitter junction, or output clamp. With this technique, a "sense" diode is calibrated so that forward voltage is a direct indicator of diode junction temperature. Then, current is applied to some other component on the chip to simulate operating conditions and to produce a temperature rise. Since the thermal resistance of the silicon chip is low, the temperature of the sense diode is assumed to be the same as the rest of the monolithic chip.

The sense diode should be calibrated over at least the expected junction operating temperature chamber. Apply an accurately measured, low current of about 1 mA through the

sense diode and measure the forward voltage in 25°C increments after stabilization at each temperature. This calibration provides enough data for at least six points to construct a diode-forward-voltage versus junction-temperature graph at the specified forward current. A typical 25°C forward voltage is between 600 and 750 mV and decreases 1.6 to 2.0 mV/°C.

For power levels above 2 W, it may be necessary to use more than a single transistor if only the device saturation voltage and sink current are used. When higher power is desired, keep the output out of saturation.

Measuring the sense-diode forward voltage may require a considerable waiting period (10 to 15 minutes) for thermal equilibrium. In any event, at the instant of measurement, the heating power may have to be disconnected since erroneous readings may result from IR drop in circuit common leads. Various circuit connections (such as four-point Kelvin) may be arranged to reduce or eliminate this source of error.

The IC junction temperature can be determined by comparing the voltage measurement against the internal power source with the voltage measurement with the temperature chamber.

industrial power driver are $V_{CC} = 5.25$ V, $I_{CC} = 25$ mA, and $V_{CE(SAT)} = 0.7$V, and $I_c = 250$ mA. From Equations 2 and 3, worst case logic and output power dissipation are

$$P_l = 4 (5.25 \text{ V} \times 25 \text{ mA})$$
$$= 525 \text{ mW}$$

$$P_o = 4 (0.7 \text{ V} \times 250 \text{ mA})$$
$$= 700 \text{ mW}$$

Thus, the total worst case power dissipation P_D is 525 mW plus 700 mW, or 1.225 W. From Equation 1, maximum junction temperature T_J is

$$T_J = 70°\text{C} + (1.225 \text{ W})$$
$$\times (16.67 \text{ mW/°C})$$
$$= 143.5°\text{C}$$

Problem: Determine the acceptable duty cycle for a hermetic power driver with a thermal resistance of 100°C/W in an ambient of 85°C and which is controlling load currents of 250 mA on each of four outputs.

Solution: From Equation 1, the allowable average power dissipation

P_D for this IC is

$$P_D = \frac{150°\text{C} - 85°\text{C}}{100°\text{C/W}}$$
$$= 0.65 \text{ W}$$

This means that there is 0.65 W limit on average power, but, not instantaneous power. If the duty cycle is low enough, and the ON time is not more than about 0.5 sec, the average power dissipation can be considerably lower than the peak power. The ON, or peak power, is determined from the data sheet maximum values of V_{CC}, I_{CC}, and $V_{CE(SAT)}$ at the specified load current of 250 mA. From Equations 2 and 3, logic-gate power P_l and output power P_o for the ON state are

$$P_l = 4 (5.5 \text{ V} \times 26.5 \text{ mA})$$
$$= 583 \text{ mW}$$

$$P_o = 4 (0.7 \text{ V} \times 250 \text{ mA})$$
$$= 700 \text{ mW}$$

Instantaneous ON power P_{ON} is the sum of P_l and P_o for the ON state, or 1.283 W. The OFF power is primarily the

power dissipated by the logic in the OFF state, and is found by using the I_{CC} maximum rated current listed on the specification sheet. The power dissipated in the output stage can be calculated from the leakage current I_c and supply voltage V_{CE}. From Equations 2 and 3, logic-gate power P_l and output power P_o for the OFF state are

$$P_l = 4 (5.5 \text{ V} \times 7.5 \text{ mA})$$
$$= 165 \text{ mW}$$

$$P_o = 4 (100 \text{ V} \times 0.1 \text{ mA})$$
$$= 40 \text{ mW}$$

Instantaneous OFF power P_{OFF} is the sum of P_l and P_o for the OFF state, or 205 mW. From Equation 4, acceptable duty cycle D is

$$D = \frac{P_D - P_{OFF}}{P_{ON} - P_{OFF}}$$
$$= \frac{0.65 \text{ W} - 0.205 \text{ W}}{1.283 \text{ W} - 0.205 \text{ W}}$$

load current, and n = number of logic gates. Manufacturers usually list typical and maximum values for these voltages and currents. For thermal considerations it is best to use the maximum values so that worst-case power dissipation is determined.

If the duty cycle of the device is longer than 0.5 sec, the peak power dissipation is the sum of the logic-gate power P_l and output power P_o for the logic ON state alone. If the ON time is less than 0.5 sec, however, average power dissipation must be calculated from instantaneous

Setting Up the Circuit

Resistors control output transistor power dissipation

Constant current source of about 1 mA

I_c A

V_{CE} V V

Voltmeter measures forward voltage across sense diode

Transient suppression diode used as sense diode

IC device
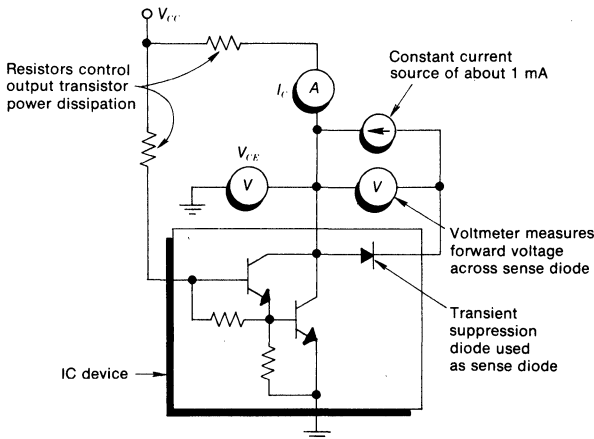
Input power is negligible compared to output power and is therefore not measured.

Calibrating the Sense Diode

Line has a slope of approximately −1.8 mV/°C and intersects the ordinate between 700 and 750 mV.

Diode Forward Voltage, V_F (mV)

Junction Temperature, T_J (°C)

12
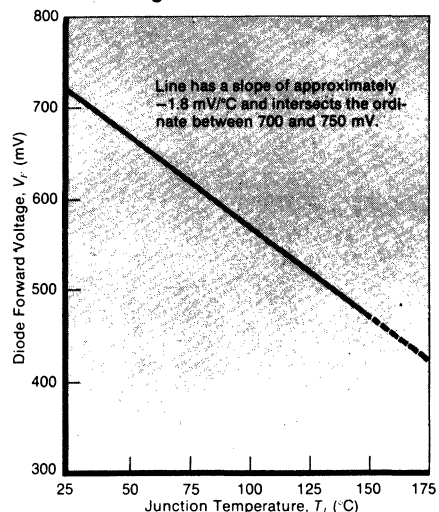
What the Curves Show

The junction temperature of an IC depends on several factors, including the thermal resistance of the IC and the operating duty cycle. Graphs showing the relationship of these factors are often useful in specifying an IC.
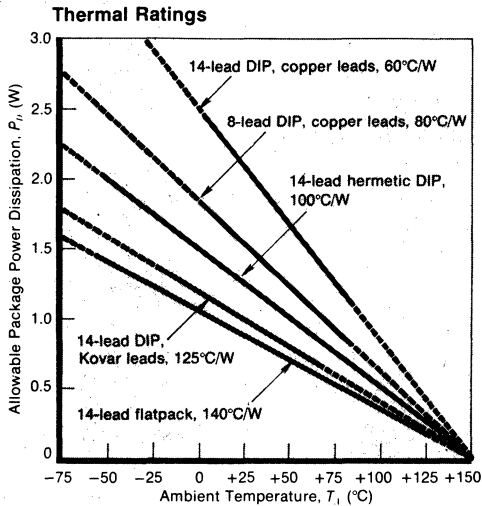
Thermal Ratings

Typical thermal-resistance ratings for ICs in still air range from 60°C/W to 140°C/W. The slope of each curve on this graph is equal to the derating factor $G\theta$, which is the reciprocal of thermal resistance $R\theta$. For an ambient temperature of 50°C, a typical 14-lead flatpack with an $R\theta$ of 140°C/W can dissipate about 0.7 W. A typical DIP, however, with 14 copper-alloy leads can dissipate almost 1.7 W at 50°C.

The highest allowable package power dissipation shown here is 2.5 W. Other special-purpose DIP packages are available with power dissipation ratings as high as 3.3 W at 0°C ($R\theta = 45$°C/W). If not for package limitations, IC chip dissipation might be greater than 9 W at an ambient temperature of up to 70°C.

Although the curve for plastic DIPs goes all the way to 150°C, they ordinarily are not used in ambients above 85°C because of traditional package limitations. Hermetic DIPs are specified to temperatures of 125°C, and at 150°C the device should be derated to 0 W. The higher specification limits for hermetic devices is the result of their design for use in rigorous, high-reliability military applications.
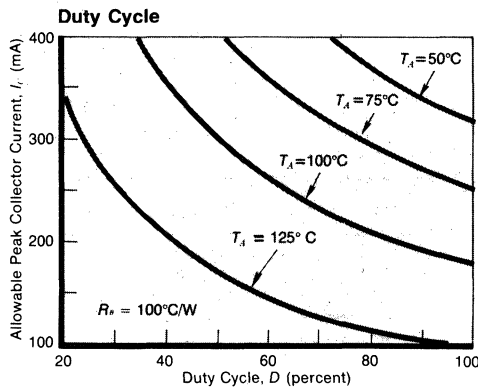
Duty Cycle

Duty cycle is important in calculating IC junction temperature because average power—not instantaneous power—is responsible for heating the IC. To convert from peak power to average power, multiply the peak power dissipation by the duty cycle. The average-power rating is then used with the thermal-resistance rating to calculate the IC junction temperature. Thus, short duty cycles allow peak power to be high without exceeding the 150°C junction-temperature limit. However, this consideration applies only to ON times of less than 0.5 sec.

ON and OFF power P_{ON} and P_{OFF} from

$$P_D = DP_{ON} + (1 - D)P_{OFF} \qquad (4)$$

Corrective Actions

If the junction temperature or the required power dissipation of the IC is calculated to be greater than the maximum values specified by the manufacturer, device reliability and operating characteristics possibly will be reduced. Possible solutions are: 1. Modify or partition the circuit design so the IC is not required to dissipate as much power. 2. Reduce the thermal resistance of the IC by using a heat sink or forced-air cooling. 3. Reduce the ambient temperature by moving heat-producing components such as transformers and resistors away from the IC. 4. Specify a different IC with improved thermal or electrical characteristics (if available).

THERMAL RESISTANCE—
A RELIABILITY CONSIDERATION

More and more the semiconductor component supplier and the ultimate system user are becoming aware of the need for reliable components. Most failure mechanisms responsible for reliability failures are temperature dependent and the kinetics of the failure reaction are normally described by an Arrhenius function. This dependence, therefore, demands the capability of measuring the mean temperature which an integrated circuit die will attain during operation to realistically assess the reliability of the part.

The problem addressed by this paper is the inconsistency of the measurement techniques and the results used by manufacturers and users to determine the thermal characteristics of packaged semiconductor components. Our objective is to provide insight into the considerations which must be applied when evaluating these thermal properties of the packaged component. These considerations are materials, geometry and environment.

Furthermore, we wish to instill uniformity in the method of determining thermal properties of packaged semiconductors through understanding of the variables involved which can lead to a useable industry standard.

Reliability—The Temperature Function

The recognition of the problems one encounters in measuring the mean temperature of a die has been directly related to our experiences at the Sprague Electric Co. in our Reliability Assurance Programs. The large number of device types manufactured require an equally large number of burn-in boards having different functions and geometry for the individual reliability studies. The variations in board density and thermal environment for a device under test have provided considerable junction temperature data from which we conclude that a "thermal resistance" measured in one oven with its set of conditions is not transferable to another oven with different boards, loading, etc. when the reference temperature for the measurement is the oven control temperature. Furthermore, it has become obvious that these same problems in measuring a mean die temperature exist in a system environment.

Most reactions which can cause a failure in an electrical parameter of an integrated circuit are chemical in nature and are influenced by temperature. The temperature dependence of these reactions has been described very well by S. Arrhenius in his treatment of reaction kinetics.[1] In his treatment, the reaction velocity or rate is given by the equation.

$$d\ln V_r/dT = E/RT^2$$

here V_r is the specific reaction rate, T is the absolute temperature, R is the Molar Gas Constant, and E is the energy difference between a mole of active molecules and a mole of normal molecules.

This equation integrates to

$$\ln V_r = E/RT + A$$

where A is a constant which is the value of $\ln V_r$ at $1/T = 0$, $(\ln V_r)$. A more familiar expression is

$$\ln V_r = \ln V_r^0 - \epsilon/kT$$

or

$$V_r = V_r^0 e - \epsilon/kT$$

where ϵ is the activation energy per molecule ($= E/N$), N = Avagado's number and k is the gas constant per molecule ($=R/N$), which is generally known as the Boltzmann constant. It has the value 8.6×10^{-5} eV/°K.

V_E, the time rate of change of the electrical parameter is proportional to V_r, i.e., $V_E = BV_r$. The amount of change in the electrical parameter necessary to cause a normal device to fail, ΔP_f, is $V_E t_f$ where t_f is the time of failure.

Recalling that $V_E = BV_r$, then

$$\Delta P_f = BV_r t_f$$

For a given device ΔP_F is a constant, therefore,

$$t_f = \Delta P_f B^{-1}/V_r$$

but

$$V_r = V_r^0 e \ \epsilon/kT$$

therefore

$$t_f = (B^{-1} \Delta P_f/V_r^0 e^{\ \epsilon/kT} = \delta e^{\ \epsilon/kT}$$

where

$$\delta = B^{-1} \Delta P_f/V_r^0$$

12

The acceleration factor ($\overline{\text{AF}}$) between any two temperatures is derived from this equation, when the activation energy for the failure reaction is known:

$$\overline{\text{AF}} = t_{f_1}/t_{f_2} = e^{e/k(1/T_1 - 1/T_2)}$$

Activation energies of most reactions responsible for random failures in a normal operating period (beyond infant mortality) are nominally

$$(0.4 - 1.0) \text{ eV}.$$

The importance of accurately determining the die temperature is now clear if one considers a not unrealistic situation where a device is thought to be operating with a die temperature of 120° and the actual temperature is 150°C. If the failure reaction has an activation energy of 0.7 eV, then the acceleration factor is 4.3 which means the device would fail in less than one quarter of the time it would have taken if the device actually operated at 120°C.

Thermal Resistance — θ_{JA}

Quite frequently applications engineers have made attempts to identify the temperature attained by a die when a steady state rate of heat is being generated by the die by applying the term called "Thermal Resistance." This "constant," designated $R\theta_{JA}$ or simply θ_{JA}, relates the temperature rise of a packaged integrated circuit die above an ambient temperature when a known constant power is generated in the die. This term is normally defined as

$$\theta_{JA} = (T_J - T_A)/P_D$$

where T_J is the mean junction or die temperature, T_A is an ambient temperature, and P_D is the power generated within the die which must be conducted from the die to the ambient. This is occasionally designated Q_T, the time rate of heat generation in the die. Thermal resistance data supplied by manufacturers may be referenced to a cubic foot of free or still air, flowing air at some velocity, or simply no reference. These are some of the definitions of "ambient" from which one must determine where to measure T_A.

Thermal resistance as defined by θ_{JA} is not constant. It is made up of a constant term (or terms) in series with a number of variable terms. The constant terms relate to the package materials and geometry, which we will designate θ_{JC_i} and the variable terms relate to the heat paths from the package boundary to some isothermal envelope in the system which has the temperature T_A. Even if the system for measuring θ_{JA} is defined, it is virtually impossible to re-

produce that system in an application since the external thermal paths are determined by the method of mounting, the printed wiring board if used, other heat generating components on the board or in the vicinity, air flow patterns, etc. These are all variable for each application. We have measured values of θ_{JA} for the same device which vary by a factor of two when the mounting and environmental conditions are changed. The values in the θ_{JA} column in Tables 2 and 3 are indicative of the variation.

One is tempted to partition θ_{JA} into two thermal terms,

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

where θ_{JC} is defined as the thermal resistance from the source of power at T_J to the boundary of the package not including the external legs, and θ_{CA} is the thermal resistance from the package boundary to that isothermal envelope at T_A. However, when one examines the thermal profile along the surface of a plastic dual-in-line package such as shown in Figure 1, it is immediately obvious that a definition of θ_{JC}

$$\theta_{JC} = (T_J - T_C)/P_D$$

cannot be applied because T_C varies with position. Similarly, the term θ_{CA} defined by

$$\theta_{CA} = (T_C - T_A)/P_D$$

suffers from the same variability in T_C. This being the case it is invalid to partition θ_{JA} when operating on the *total* power to be dissipated, P_D.
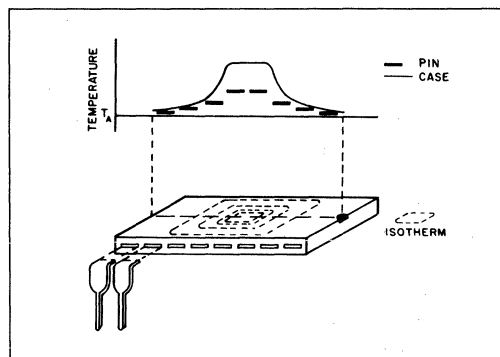
Figure 1

The Thermal Model

When one examines a plastic package supplied by an individual manufacturer it is found that the geometry of the lead frame, its position within the package boundary, its composition, the composition of the plastic and its filler, the internal wire bonding are very carefully controlled and constant in time. This being the case one can readily build a model of the package which can be as invariant as the package material properties. If one considers all possible heat flows, a very complex model emerges. However, if the thermal conductivities of the package materials and the orders of magnitude difference in the values of these conductivities are considered, a simplified workable model can be generated by neglecting heat paths where heat flows are minimal. The simplified model shown in Figure 2 has ignored the heat flow between leads and assumes that the large difference between the thermal conductivity of the loaded plastic and the metals in the package define the specified heat paths. For example, the heat flow between leads would be a shunting resistor between heat paths in the model. The thermal conductivity of most plastics range between 1.5 and 3 $\times$ 10^{-3} calories/cm $-$ °C while copper based materials range between 0.5 and 0.82 calories/cm $-$ °C and nickel based alloys are about 0.03 calories/cm $-$ °C.
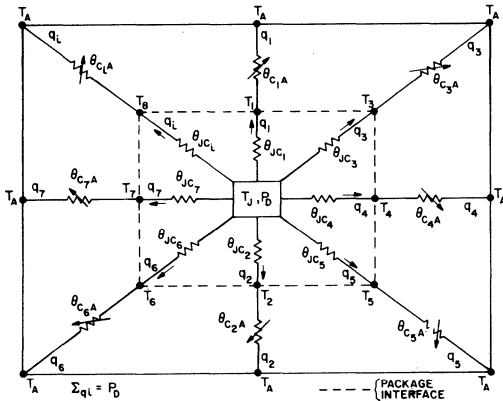
Figure 2

The heat paths defined by θ_{JC_i}, where i refers to a particular path, radiate from the chip to an area on the package periphery defined by the projected chip or pad area as well as the mean cross-sectional area of each of the leads within the plastic package boundary (see Figure 1). Because of package symmetry, a 16 lead isolated pad package may have seven different heat paths which can be characterized. The thermal resistance, θ_{JC_i}, can be calculated

for each path from the geometry and material properties. For example θ_{JC_1} is the resistance from the top of the chip to the projected area on the package surface. The value of θ_{JC_1} is given by

$$\theta_{JC_1} = (T_J - T_{C_1})/q_1 = L/K_pA$$

where L is the length of the heat path (thickness of the plastic above the die), A is the cross-sectional area of the heat path (are of the die or the pad), K_p is the thermal conductivity of the loaded plastic and q_1 is the heat/second flowing in the path defined by A and L.

θ_{JC_2} is the thermal resistance from the top of the die through the silicon, through the pad and through the plastic to the bottom surface. The value of θ_{JC_2} is given by

$$\theta_{JC_2} = (T_J - T_{C_2})/q_2 =$$
$$[1/A] \sum L_n/K_n$$
$$n = Si, Metal, Plastic$$

Similar expressions can be derived for each of the leads and they have the form

$$\theta_{JC_i} = (T_J - T_{C_i})/q_i =$$
$$[1/t] [(L/K_PW_P) + (1/K_M) \sum L_n/W_n]$$
$$n = 1, 2 \ldots \ldots$$

where t is the thickness of the lead frame, K_p is the thermal conductivity of the loaded plastic, K_M is the thermal conductivity of the frame metal, L_n is the mean length of each connected portion of a leg segment having a mean width, W_n. In accord with the model, each internal path characterized by a thermal resistance, θ_{JC_i}, is in series with an external thermal resistance, θ_{C_iA}, which completes the path to T_A. The value of θ_{C_iA} can be calculated from the amount of heat, q_i, flowing through the internal package path and the temperature difference, $(T_{C_i} - T_A)$, with the equation

$$\theta_{C_iA} = (T_{C_i} - T_A) / q_i.$$

Values of θ_{C_iA} are variable and depend upon the specific environment.

We at Sprague Electric Company identify the heat paths in our calculations and data as follows: a) when i = 1 the path is from die to case surface directly above, b) when i = 2 the path is from die to the case surface directly below and c) when i = 3, 4, 5 . . . the path is from die through an identified metal lead to the intersection with the plastic surface.

12

Verification of Model

From the model one can derive the minimum thermal resistance which is characteristic of the package. This can be calculated for the condition when all case temperatures are equal and at T_A. This is equivalent to shorting all external thermal resistances so that $T_{C_i} = T_A$. When all T_{C_i} are equal, the reciprocal of the sum of the reciprocals of all θ_{JC_i} is the minimum thermal resistance for the package. This is realized experimentally by placing the unit in an infinite heat sink such as a rapidly stirred, low-viscosity controlled temperature bath. The case temperature is now forced to be the same over all surfaces and by definition it is T_A. θ_{JC} is the minimum limit of θ_{JA}. Table 1 shows the agreement between the values of θ_{JC} calculated from the model when the case temperatures are shorted together and the values experimentally measured in a controlled temperature liquid bath. The agreement between calculated and experimental values for packages constructed from different materials enhance the validity of the model.

Applying The Model To Measure T_J

Having verified the model, any one of the identified heat paths, which has a constant thermal resistance, o_{JC_i}, can now be used to determine quite accurately the die temperature, T_J. If one chooses to measure the case temperature directly above the die, the difference between die temperature and case temperature is related to the heat flow, q_i, through that path by the thermal conductivity equation:

$$q_i = K_p A (T_J - T_{C_1})/L_1.$$

Rearranging this equation to

$$(T_J - T_{C_1})/q_1 = L_1/k_p A_1 = \theta_{JC_1}$$

Then

$$T_J = T_{C_1} + q_1 \theta_{JC_1}$$

If the fraction of total heat, P_D generated by the die which passes through path 1 is defined as k, then

$$q_1 = k_1 P_D$$

Substituting into the previous equation, T_J is now referenced to T_{C_1} by

$$T_J = T_{C_1} + k_1 \theta_{JC_1} P_D$$

where T_J, T_{C_1}, and P_D are experimentally measureable quantities. Values of $k_1 \theta_{JC_1}$ can be determined. This term can be used to determine T_J in any environment by measuring T_{C1} and the total heat generated by the die. This equation applies for any path, i., i, e.

$$T_J = T_{C_1} + k_i \theta_{JC_i} P_D$$

Experimental results are presented in Table 2 which establish that $k_i \theta_{JC_i}$ is a constant, the magnitude of which is determined by the heat path chosen.

In our notation, $k_4 \theta_{JC_4}$ is the thermal resistance of the path determined by measuring the temperature of pin 4 at the point of intersection with the case body. Further data are presented in Table 3 for a copper tab package where the pad on which the die is mounted extends to the outside of the package. The values of $k_5 \theta_{JC_5}$ remain constant over a large change in environment. When $i = 5$, the heat path is from the die through the heat tab to the intersection with the case surface.

Figure 3 shows the outline of the frame in the 16 pin isolated pad package which is designated the ''A'' package. The ''B'' package or tab package frame outline is also shown.

Measurement of $k_i \theta_{JC_i}$

Although the derived equations indicate that $k_i \theta_{JC_i}$ are determined by two temperature measurements at one power level, the values are more accurately determined from temperature versus power plots.

TABLE 1
COMPARISON OF CALCULATED AND EXPERIMENTAL VALUES
OF $[\theta_{JC}]$ $T_{C_i} = T_A$
(All measurements in °C/W)

Package Type	Frame Material	$[\theta_{JC}]$ $T_{C_i} = T_A$	
		Experimental	Calculated
16 pin, isolated pad, Epoxy I	copper	41 ± 3	43
16 pin, isolated pad, Epoxy I	Kovar	100 ± 4	93
16 Pin Tab	copper	$8.6 \pm .7$	8.5

TABLE 2
THERMAL RESISTANCE VALUES—ISOLATED PAD—EPOXY PACKAGE
(All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$k_4\theta_{C_4A}$	$k_1\theta_{C1A}$	$k_1\theta_{JC_1}$	$k_4\theta_{JC_4}$
ULN-2003A 16-Pin Copper Frame. "A" Package	1 ft.³ still air, socket mount	84.7	39.1	48.1	36.6	45.6
ULN-2003A 16-Pin Copper Frame. "A" Package	Oven #1 60 CFM, pin connectors	60.0	17.0	25.2	34.8	42.3
ULN-2003A 16-Pin Copper Frame. "A" Package	AAVID E type 5010 heat sink Oven #1 60 CFM	50.4	11.4	15.2	35.2	39
ULN-2003A 16-Pin Copper Frame. "A" Package	Fluorocarbon Bath, pin connectors	41.3	3.3	2.9	38.4	38
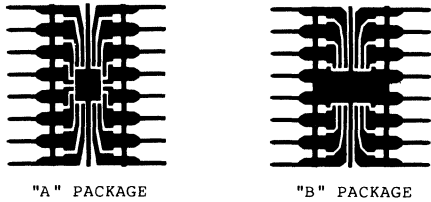
"A" PACKAGE   "B" PACKAGE

Figure 3
Plastic Package Frame Geometry

If one considers any one path, i, in the model, that path is described by:

$$T_J - T_A = q_i (\theta_{JC_i} + \theta_{C_iA})$$

Here again if k_i is the fraction of the total heat (P_D) which traverses path i then the previous equation can be written

$$T_J - T_A = k_iP_D (\theta_{JC_i} + \theta_{C_iA})$$

or rearranging terms

$$(T_J - T_A)/P_D = k_i\theta_{JC_i} + k_i\theta_{C_iA}$$

TABLE 3
THERMAL RESISTANCE VALUES—TAB PAD—EPOXY PACKAGE
(All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$K_5\theta_{C_5}A$	K_5J_{C5}
Test Chip "B" Package	oven #1, $T_A = 50°$, 60 CFM	32.8	25.0	7.8
ULN-2068 "B" Package	oven #1, $T_A = 50°$, 60 CFM	34.9	26.4	8.5
ULN-2068 "B" Package	Socket mount, FC-40 Bath	23.2	13.5	9.7
ULN-2068 "B" Package	Socket mounted on board, FC-40 Bath	26.8	17.4	9.4
Test Die "B" Package	oven #1, soldered on test board, 60 CFM	31.2	22.8	8.4
Test Die "B" Package	oven #1, soldered in test board w/Staver heat sink	22.3	14.2	8.1

12

By definition $(T_J - T_A)/P_D = \theta_{JA}$, therefore by substitution and rearrangement

$$k_i\theta_{JC_i} = \theta_{JA} - k_i\theta_{C_iA}$$

where experimentally θ_{JA} is the slope of a plot of T_J versus P_D and $K_i\theta_{C_iA}$ is the slope of the plot of T_{C_i}, versus P_D. Figures 4, 5, and 6 are representative of the experimental plots for evaluation of $k_i\theta_{JC_i}$.
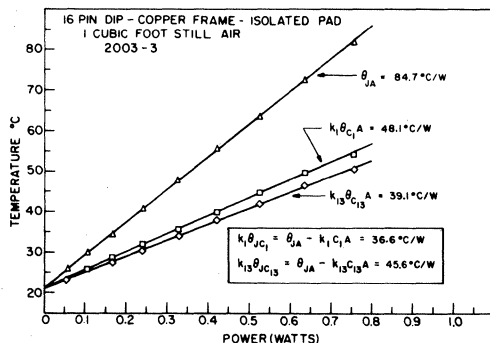
Figure 4
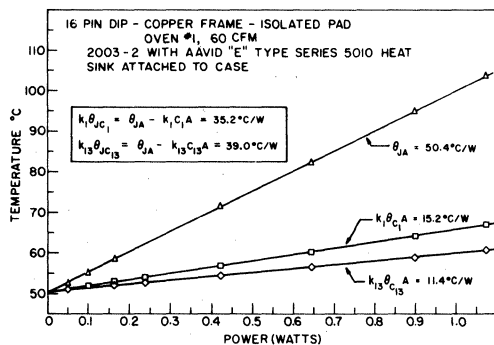
Figure 5
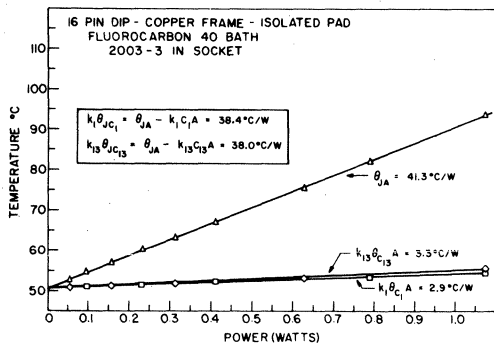
Figure 6

T_{C_i} Measurement

The numerical values of $k_i\theta_{JC_i}$ which we have shown experimentally to be constant over a large variation in environmental conditions are functions of the measuring system for determining the case or leg temperature, T_{C_i}. This can be shown by considering heat path 1 in the Model shown in Figure 2. In this case $q_1 = (T_J - T_A)/(\theta_{C_1} + \theta_{C_1A})$. θ_{JC_1} is defined as L_1/k_pA_1 where A_1 is determined by the die area. When a thermocouple is attached to the surface directly over the die it also functions as a heat sink. This changes the effective area A of the internal heat path and also changes the external thermal resistance, θ_{C_1A}. The changes are functions of the thermocouple composition and size. The value of θ_{JC_1} is now determined by the effective area of contact of the thermocouple and its value remains constant when the attached thermocouple's size is held constant. k_1, ($= q_1/Q_t$), also changes because q_1 is determined by the sum of θ_{JC_1} and θ_{C_1A}. The term $(T_J - T_A)$ is essentially constant within experimental error because q_1 is small compared to Q_t and the variations in q_1 do not measureably change the die temperature.

θ_{C_1A} decreases as the wire size of a copper-constantan thermocouple increases and it increases as the composition is changed from copper-constantan to iron constantan. The thermal conductivities of copper, iron, and constantan are respectively 0.9, 0.16, and 0.054 cal/°C-cm.

Data in Table 4 confirm the direction and change in $k_1\theta_{JC_1}$ with change in measuring system. Data were taken in the same oven ambient.

When the physical system for T_C measurement and the conditions for measurement are specified and held constant, values for $k_1\theta_{JC_1}$ are constants.

T_J Measurement For $k_i\theta_{JC_i}$ Determination

An accurate measurement of the value of $k_i\theta_{JC_i}$ requires a method of measuring the mean temperature of the die, T_J. Techniques to make this measurement have been discussed elsewhere. (See Ref. 2, 3, 4) They involve measurement of a temperature sensitive parameter of an element on the die. The forward voltage drop across a diode measured at constant current is a commonly used parameter. One must observe caution when applying the cali-

TABLE 4
VARIATIONS IN $k_i\theta_{JC_1}$ WITH MEASUREMENT SYSTEM
(All measurements in °C/W)

Device	Condition of Measurement	θ_{JA}	$k_i\theta_{C_1A}$	$k_i\theta_{JC_1}$
Test device	.005" Type "J" thermocouple	127.6	52.2	75.4
Test device	.012" Type "J" thermocouple	123.5	31.5	92.0
2125-Linear TV Circuit	.005" Type "T" thermocouple	123.3	75.0	48.3

bration data for an element in an unpowered die to the measured values of that element when the die is powered. It is rather unique if a parasitic voltage or current from the powered portion of the die does not interact with the temperature measuring element. This interaction leads to an inaccurate indication of the true temperature.

A test chip with a number of temperature sensitive elements is valuable. Figure 7 is a photo micrograph of a test chip designed by personnel at the Sprague Electric Company to evaluate thermal resistance values for various packages as well as package-surface interactions. The die contains 3 heat generators, and 6 primary temperature sensors, which are either diodes or special resistors. Parasitics normally interact differently with different elements because of location or structure variations. Agreement in the value of temperatures measured simultaneously for different elements on the chip normally indicates a correct measurement.
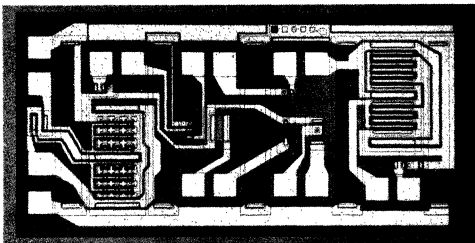
Figure 7

Figure 8 illustrates errors which can be introduced when making static steady state measurements of temperature during power application. Observe the plots of T_j (from V_{eb} calibration) versus P_D for three different diodes on the chip. Although the slopes of the plots after initial power agree within 10%, the initial portion of the curve indicates a negative ther-

mal resistance and the offsets of the curves indicate a varying interaction at different power levels. Although calculation of thermal resistance by the slope method would introduce a similar error for all three diodes, the single power point method for calculating $k_i\theta_{JC_i}$, where $k_i\theta_{JC_i} = (T_J - T_{C_i})/P_D$, would introduce considerable and different levels of error in the calculated values for each diode measurement.
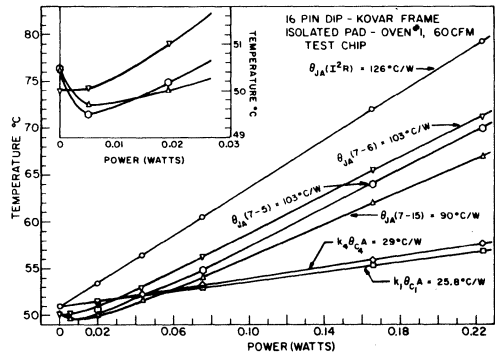
Figure 8

For example, if temperature measurements were made at a power level of 0.22 Watts, one would calculate a value of 44.6°C/W for $k_i\theta_{JC_1}$ using T_J from diode 7-15. 57.1°C/W using T_J from diode 7-5, and 63.8°C/W using T_J from diode 7-6. The true value which was verified by pulsed measurements was 97°C/W.

To eliminate interactions between the powered portion of a circuit and the temperature sensing element during measurement, the circuit shown in Figure 9 was developed. This circuit was designed for thermal evaluation of packages in which the function could be a linear circuit, a digital circuit, or the standard test chip which has a number of different power sources and temperature sensing elements.

12
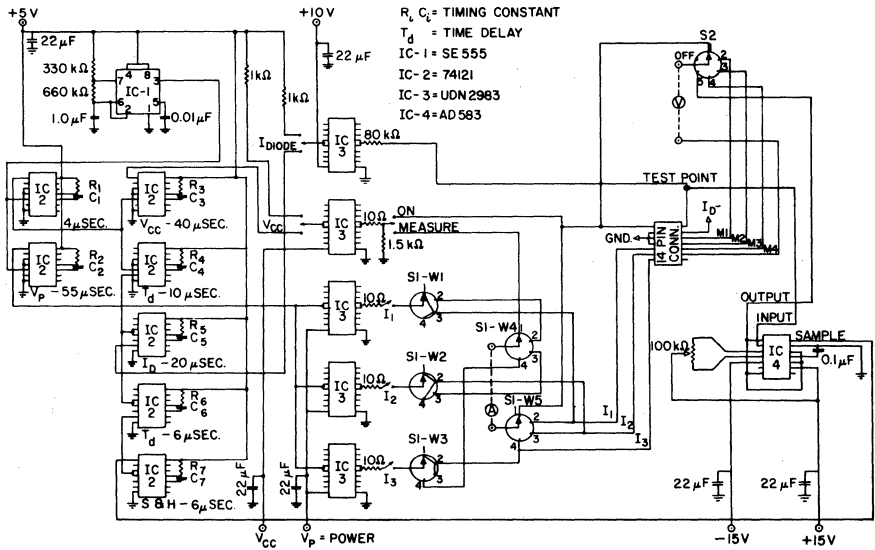
Figure 9

In operation, the circuit applies power at a measured level to the device under test for approximately one second, interrupts power for 40 microseconds, and continues this cycle throughout the test period. At the beginning of the 40-microsecond power off interval, a 10-microsecond delay allows circuit transients to decay before the diode current is activated. A 6-microsecond delay allows the current to settle before a sample and hold circuit

samples the diode voltage to determine the chip temperature. This sequence allows the package under test to come to thermal equilibrium with the environment which approaches that for continuous power input. The power down sequence and temperature measurement interval are short enough to insure that the actual temperature drop when power is removed is less than the sensitivity of the temperature sensitive element.

The case temperature measurements, T_{C_i}, can be made by thermocouple or by infra-red measurements.[4] In theory the infra-red measurements would be preferred since a conductive contact is not made to the surface which is to be measured. In practice a number of difficulties with I.R. measurements are encountered. The emissivity of the surface to be measured must be controlled to give accurate measurements. This normally requires painting the surface with a "proprietary" film. When the emissivity is mastered, two larger difficulties must be overcome; a) physically placing the infra-red measuring instrument into the system to view a package surface when the unit may be buried in a maze of printed wiring boards and circuitry and b) the cost of available instrumentation.

The thermocouple technique to measure case temperature is a practical and reliable method when the composition of the thermocouples, its physical size, its location on the package, and the method of its attachment are defined. The method of measurement can be standardized and provides an accurate, inexpensive method for the applications engineer or the reliability engineer to determine a reference temperature to which the temperature rise across the package path, $(k_i\theta_{JC_i})P_D$, can be applied in order to determine a true T_J.

REFERENCES

1. S. Glasstone, *Textbook of Physical Chemistry,* 2nd Edition, D. Van Nostrand Co. Inc., New York, 1946

2. P. E. Roughan, *Thermal Resistance of Integrated Circuit Packages,* Technical Paper TP72-7, Sprague Electric Co., 1972

3. F. R. Dewey and P. R. Emerald, *Computing IC Temperature Rise,* Machine Design, pp 98-101, June 1977

4. C. A. Lidback, *Scanning I. R. Microscopy Techniques for Semiconductor Thermal Analysis.* 17th Annual Proceedings Reliability Physics 1979 IEEE Catalog No. 79CH1425-8 Phy.

12

Operating and Handling Practices
for MOS Integrated Circuits

Handling Practices - Packaged Devices

Sprague Electric incorporates input protection diodes in all of its MOS/CMOS devices. Because of the very high input resistance in MOS devices, the following practices should be observed for protection against high static electrical charges:

1. Device leads should be in contact with a conductive material except when being tested or in actual operation.

2. Conductive parts of tools, fixtures, soldering irons and handling equipment should be grounded.

3. Devices should not be inserted into or removed from test stations unless the power is off.

4. Neither should signals be applied to the inputs while the device power supply is in an off condition.

5. Unused input leads should be committed to either V_{SS} or V_{DD}.

Handling Practices - Die

A conductive carrier should be used in order to avoid differences in voltage potential.

Automatic Handling Equipment

Grounding alone may not be sufficient and feed mechanisms should be insulated from the devices under test at the point where the devices are connected to the test equipment. Ionized air blowers can be of aide here and are available commercially. This method is very effective in eliminating static electricity problems.

Ambient Conditions

Dry weather with accompanying low humidity tends to intensify the accumulation of static charges on any surface. In this atmosphere, proper handling procedures take on added importance. If necessary, steam injectors can be procured commercially.

Alert Failure Modes

The common failure modes that appear when static energy exists and when proper handling practices are not used are:

1. Shorted input protection diodes.

2. Shorted or 'blown' open gates.

3. Open metal runs.

Simple diagnostic checks with curve tracers or similar equipment readily identifies the above failure modes.

'A' PACKAGE: 14-Pin Plastic Dual In-Line
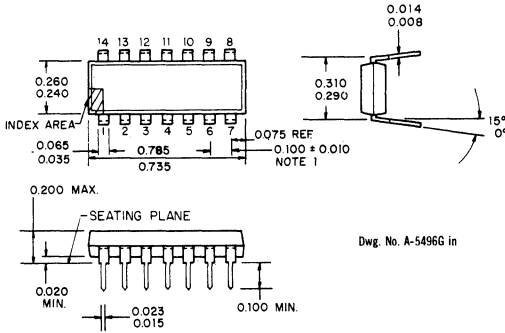
DIMENSIONS IN INCHES

DIMENSIONS IN MILLIMETRES
Based on 1″ = 25.4 mm

Dwg. No. A-5496G in

Dwg. No. A-5496G mm

'A' PACKAGE: 16-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES

DIMENSIONS IN MILLIMETRES
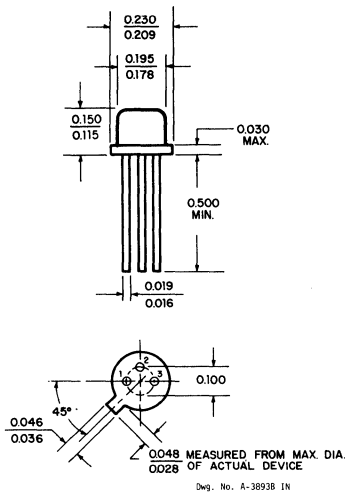Based on 1″ = 25.4 mm

Dwg. No. A-6402C in

Dwg. No. A-6402C mm

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030″ (0.76 mm) max. below seating plane.

12

'A' PACKAGE: 18-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES

Dwg. No. A-9649 in
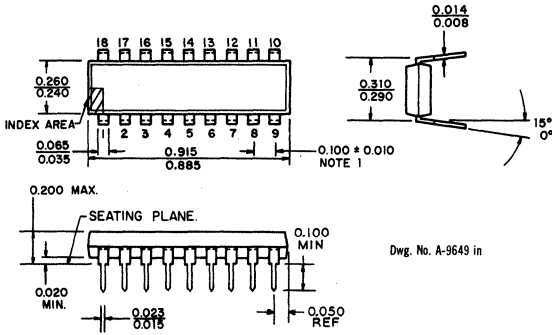
DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm

Dwg. No. A-9649 mm
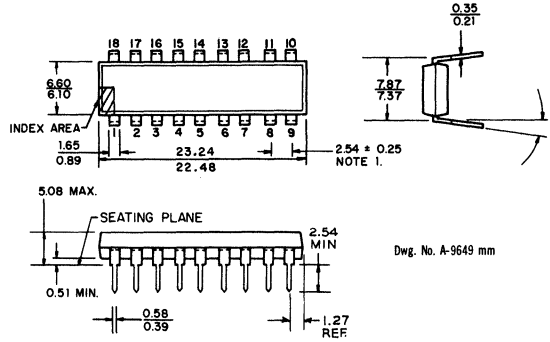
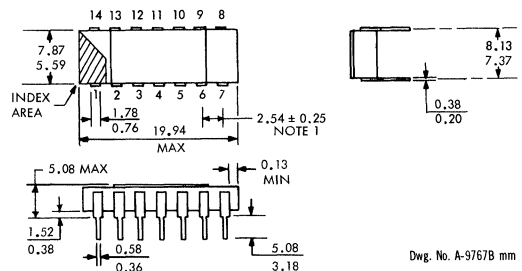## 'A' PACKAGE: 20-Pin Plastic Dual In-Line
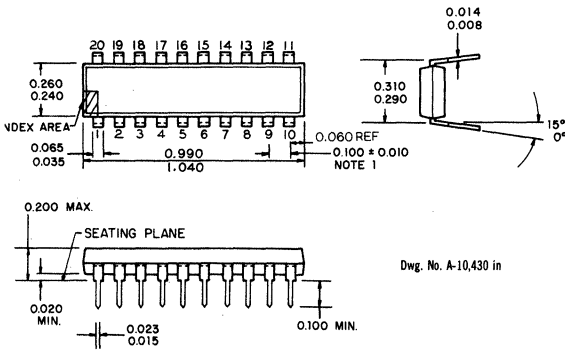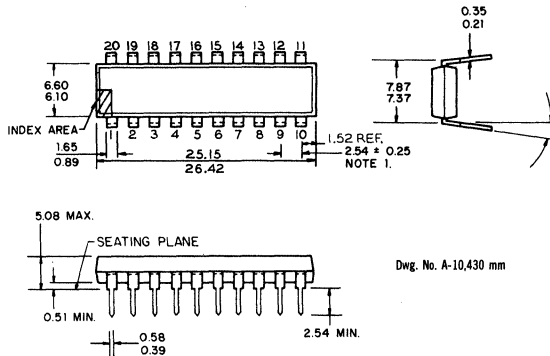
DIMENSIONS IN INCHES

Dwg. No. A-10,430 in

DIMENSIONS IN MILLIMETRES
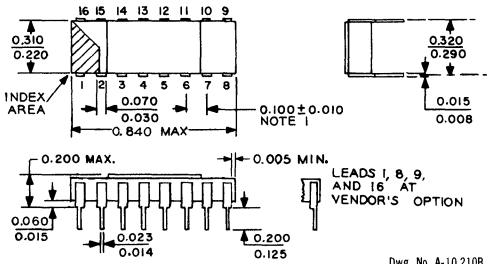Based on 1'' = 25.4 mm

Dwg. No. A-10,430 mm

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
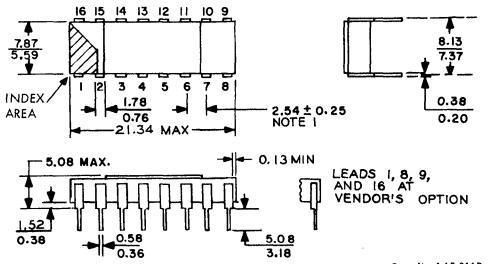5. Lead gauge plane is 0.030'' (0.76 mm) max. below seating plane.

## 'A' PACKAGE: 22-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES

Dwg. No. A-10,536B IN
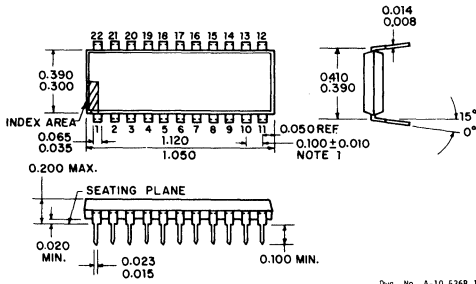
DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm

Dwg. No. A-10,536B MM
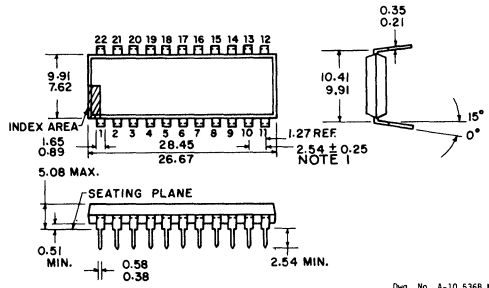
'A' PACKAGE: 28-Pin Plastic Dual In-Line
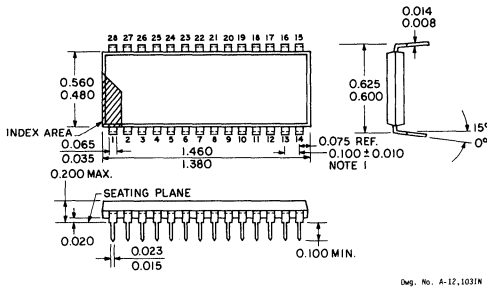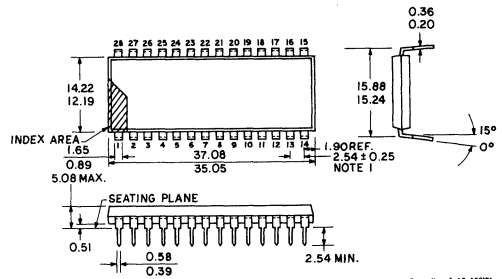
DIMENSIONS IN INCHES

Dwg. No. A-12,103IN

DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm

Dwg. No. A-12,103MM

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030'' (0.76 mm) max. below seating plane.

12

'B' PACKAGE: 8-Pin Plastic Dual In-Line

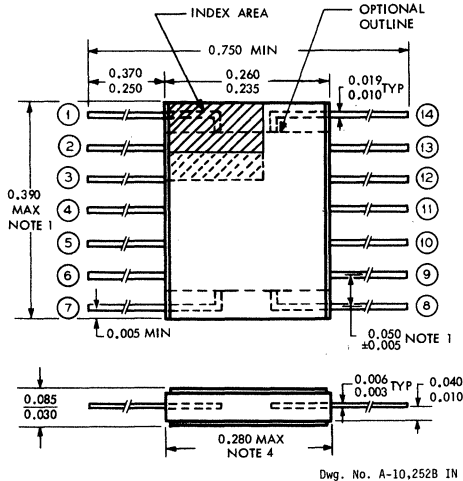**DIMENSIONS IN INCHES**

DIMENSIONS IN MILLIMETRES
(Based on 1 in. = 25.4 mm)

DWG.NO. A-10,474A IN

DWG.NO. A-10,474A MM

'B' PACKAGE: 14-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES

DIMENSIONS IN MILLIMETRES
(Based on 1 in. = 25.4 mm)

DWG.NO. A-9843C IN

DWG.NO. A-9843C MM

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030'' (0.76 mm) max. below seating plane.

'B' PACKAGE: 16-Pin Plastic Dual In-Line
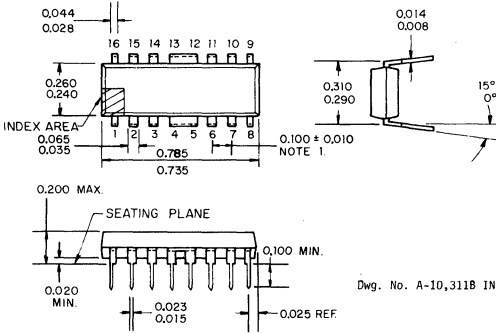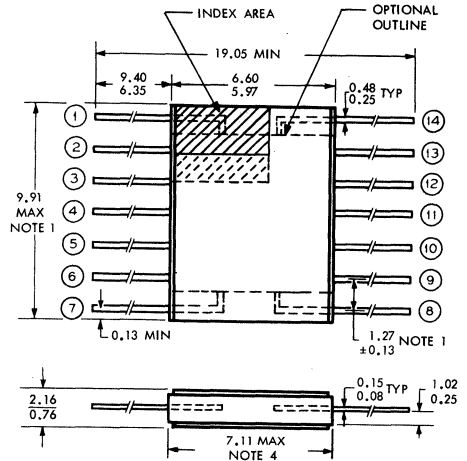
DIMENSIONS IN INCHES

DIMENSIONS IN MILLIMETRES
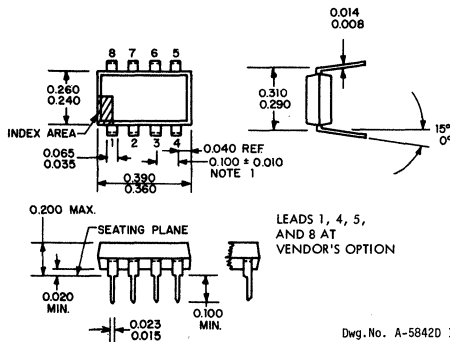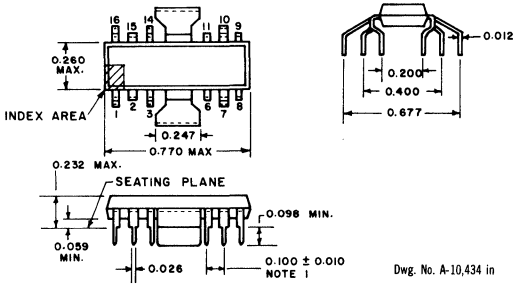Based on 1″ = 25.4 mm

Dwg. No. A-10,311B IN

Dwg. No. A-10,311B MM
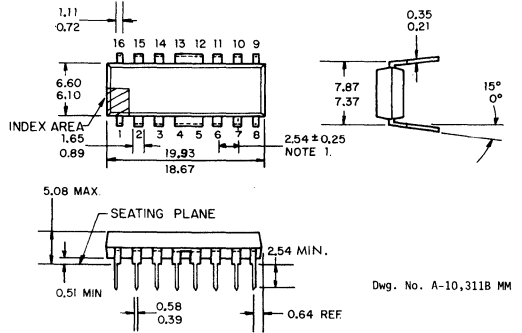
NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030″ (0.76 mm) max. below seating plane.

'D' PACKAGE: 3-Pin Metal TO-52/TO-206AC

DIMENSIONS IN INCHES
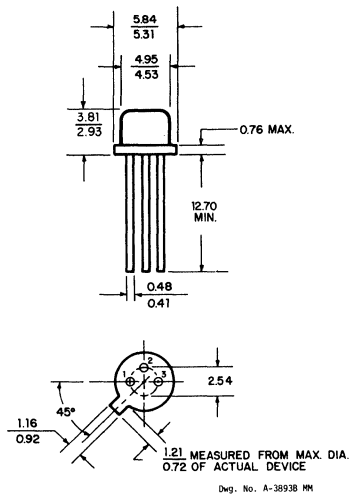
DIMENSIONS IN MILLIMETRES
Based on 1″ = 25.4 mm

Dwg. No. A-3893B IN

Dwg. No. A-3893B MM

NOTE: Lead diameter is controlled in the zone between 0.050″ (0.13 mm) and 0.250″ (6.35 mm) from the seating plane. Between 0.250″ (6.35 mm) and 0.500″ (12.7 mm) from the seating plane, a maximum lead diameter of 0.021″ (0.53 mm) is specified. Outside of these zones the lead diameter is not controlled.

12

'H' PACKAGE: 8-Pin Hermetic Dual In-Line
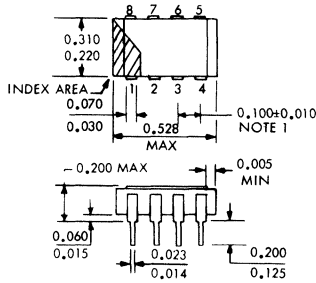
DIMENSIONS IN INCHES

DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm
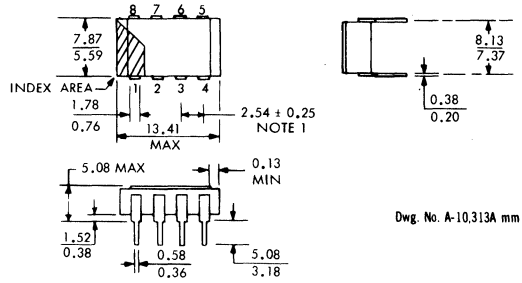
Dwg. No. A-10,313A in

Dwg. No. A-10,313A mm

'H' PACKAGE: 14-Pin Hermetic Dual In-Line
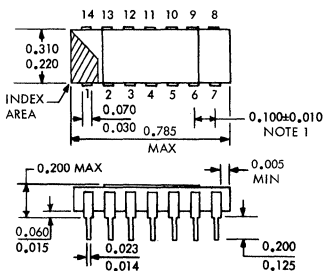
DIMENSIONS IN INCHES

DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm

Dwg. No. A-9767B in

Dwg. No. A-9767B mm

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
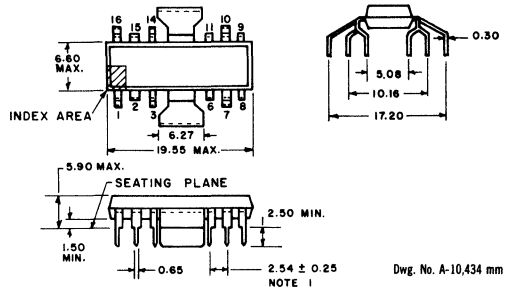5. Lead gauge plane is 0.030'' (0.76 mm) max. below seating plane.

## 'H' PACKAGE: 16-Pin Hermetic Dual In-Line

DIMENSIONS IN INCHES

Dwg. No. A-10,210B in

DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm

Dwg. No. A-10,211B mm

'H' PACKAGE: 18-Pin Hermetic Dual In-Line
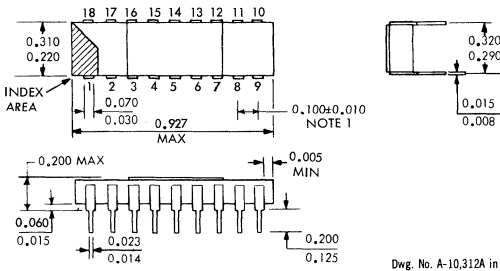
DIMENSIONS IN INCHES

Dwg. No. A-10,312A in

DIMENSIONS IN MILLIMETRES
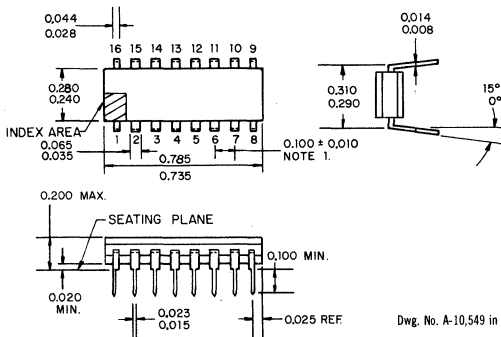#### Based on 1'' = 25.4 mm

Dwg. No. A-10,312A mm

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
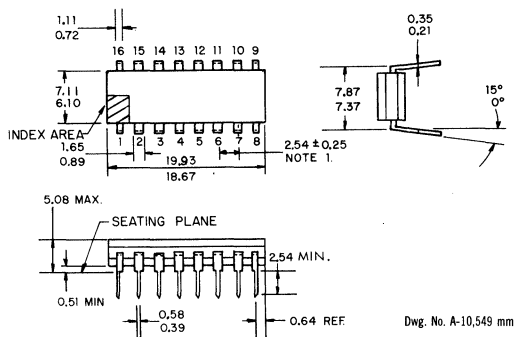5. Lead gauge plane is 0.030'' (0.76 mm) max. below seating plane.

12
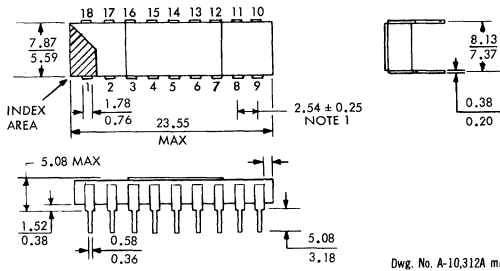
'J' PACKAGE: 14-Pin Hermetic Flat-Pack

DIMENSIONS IN INCHES

INDEX AREA
OPTIONAL OUTLINE

0.750 MIN

0.370
0.250

0.260
0.235

0.019
0.010 TYP

0.390 MAX NOTE 1

0.005 MIN

0.050 ±0.005 NOTE 1

0.085
0.030

0.006
0.003 TYP

0.040
0.010

0.280 MAX
NOTE 4

Dwg. No. A-10,252B IN

DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm

INDEX AREA
OPTIONAL OUTLINE

19.05 MIN

9.40
6.35

6.60
5.97

0.48
0.25 TYP

9.91 MAX NOTE 1

0.13 MIN

1.27 ±0.13 NOTE 1

2.16
0.76

0.15
0.08 TYP

1.02
0.25

7.11 MAX
NOTE 4

Dwg. No. A-10,252B MM

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Includes off-center lid, meniscus, and glass overrun.
5. All leads weldable and solderable.

'M' PACKAGE: 8-Pin Plastic Dual In-Line

DIMENSIONS IN INCHES

0.014
0.008

0.260
0.240

0.310
0.290

15°
0°

INDEX AREA

0.065
0.035

0.040 REF
0.100 ± 0.010
NOTE 1

0.390
0.360

0.200 MAX.

SEATING PLANE

LEADS 1, 4, 5, AND 8 AT VENDOR'S OPTION

0.020
MIN.

0.023
0.015

0.100
MIN.

Dwg. No. A-5842D IN

DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm

0.35
0.21

6.60
6.10

7.87
7.37

15°
0°

INDEX AREA

1.65
0.89

1.02 REF
2.54 ± 0.25
NOTE 1

9.91
9.14

5.08 MAX.

SEATING PLANE

LEADS 1, 4, 5, AND 8 AT VENDOR'S OPTION

0.51
MIN.

0.58
0.39

2.54 MIN.
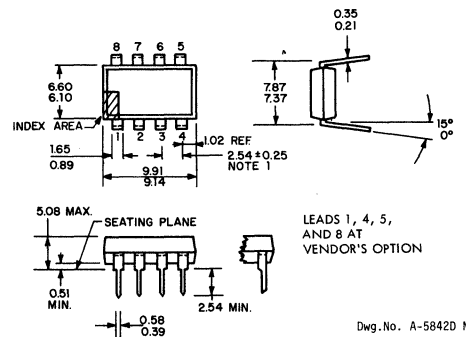
Dwg. No. A-5842D MM

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030'' (0.76 mm) max. below seating plane.

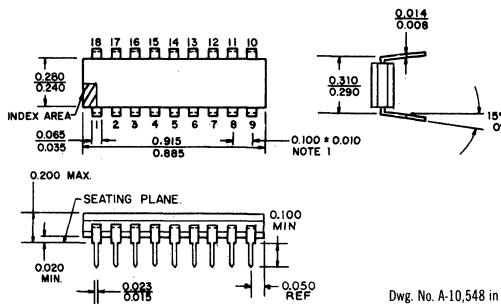## 'Q' PACKAGE: 16-Pin Plastic Quad In-Line

DIMENSIONS IN INCHES

Dwg. No. A-10,434 in

DIMENSIONS IN MILLIMETRES
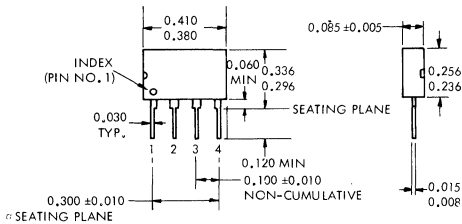Based on 1'' = 25.4 mm

Dwg. No. A-10,434 mm

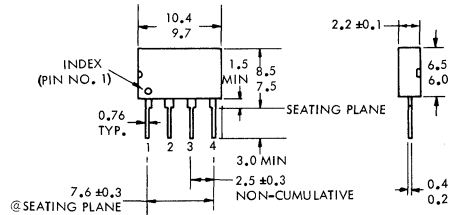## 'R' PACKAGE: 14-Pin Ceramic Dual In-Line
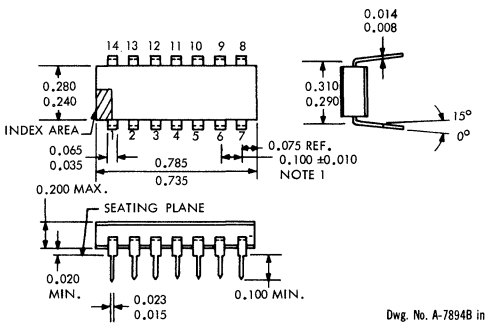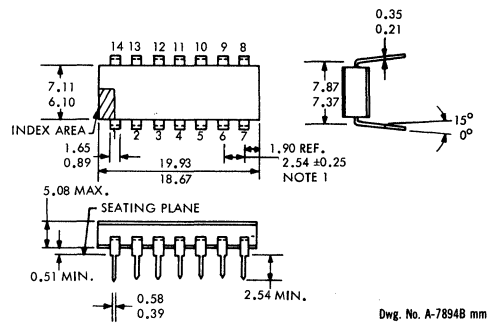
DIMENSIONS IN INCHES

Dwg. No. A-7894B in

DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm

Dwg. No. A-7894B mm

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030'' (0.76 mm) max. below seating plane.

12

'R' PACKAGE: 16-Pin Ceramic Dual In-Line

DIMENSIONS IN INCHES

0,044
0,028

16 15 14 13 12 11 10 9

0.280
0.240

INDEX AREA
0.065
0.035

1 2 3 4 5 6 7 8

0.785
0.735

0.014
0.008

0.310
0.290

15°
0°

0.100 ± 0.010
NOTE 1.

0.200 MAX.

SEATING PLANE

0.100 MIN.

0.020
MIN.

0.023
0.015

0.025 REF

Dwg. No. A-10,549 in

DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm

1.11
0.72

16 15 14 13 12 11 10 9

7.11
6.10

INDEX AREA
1.65
0.89

1 2 3 4 5 6 7 8

19,93
18.67

0.35
0.21

7.87
7.37

15°
0°

2.54 ± 0.25
NOTE 1.

5.08 MAX.

SEATING PLANE

2,54 MIN.

0.51 MIN

0.58
0.39

0.64 REF

Dwg. No. A-10,549 mm

'R' PACKAGE: 18-Pin Ceramic Dual In-Line
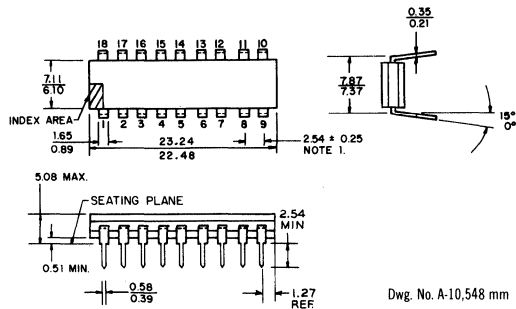
DIMENSIONS IN INCHES

18 17 16 15 14 13 12 11 10

0.280
0.240

INDEX AREA
0.065
0.035

1 2 3 4 5 6 7 8 9

0.915
0.885

0.014
0.008

0.310
0.290

15°
0°

0.100 ± 0.010
NOTE 1

0.200 MAX.

SEATING PLANE

0.100
MIN

0.020
MIN.

0.023
0.015

0.050
REF

Dwg. No. A-10,548 in

DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm

18 17 16 15 14 13 12 11 10

7.11
6.10

INDEX AREA
1.65
0.89

1 2 3 4 5 6 7 8 9

23.24
22.48

0.35
0.21

7.87
7.37

15°
0°

2.54 ± 0.25
NOTE 1.

5.08 MAX.

SEATING PLANE

2.54
MIN

0.51 MIN.

0.58
0.39

1.27
REF

Dwg. No. A-10,548 mm

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030'' (0.76 mm) max. below seating plane.

'S' PACKAGE: 4-Pin Molded Single In-Line

DIMENSIONS IN INCHES

Dwg. No. A-9002C in
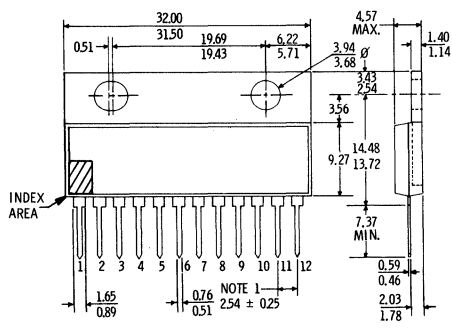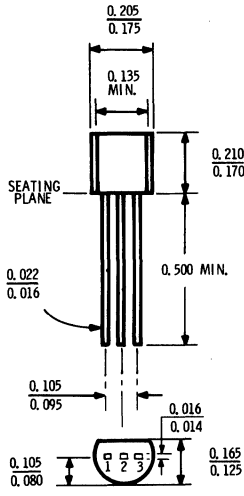
DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm

Dwg. No. A-9002C mm

NOTES:
1. Lead spacing tolerance is non-cumulative
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030'' (0.76 mm) max. below seating plane.
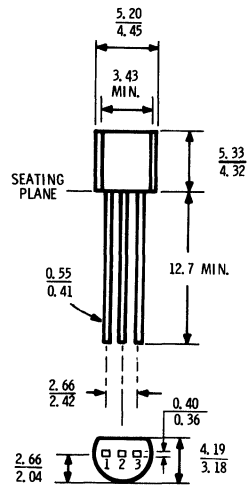
'T' PACKAGE: 3-Pin Plastic Single In-Line

DIMENSIONS IN INCHES
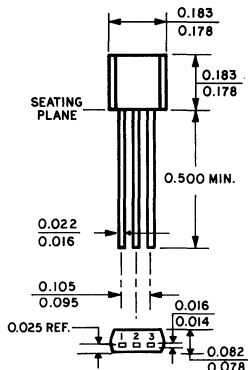
Dwg.No. A-12,139 IN

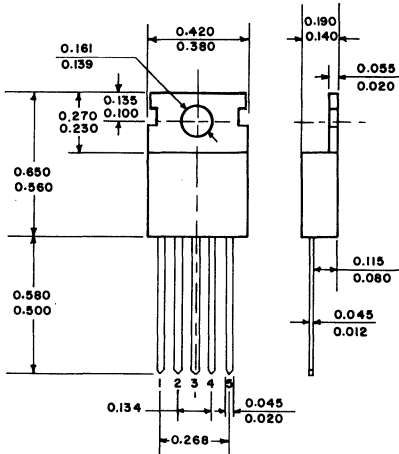### DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm
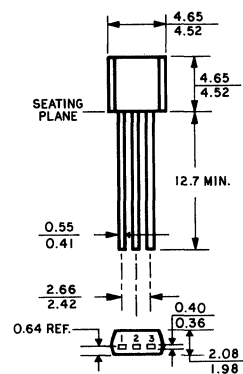
Dwg.No. A-12,139 MM

NOTE: Lead diameter is controlled in the zone between 0.050" (0.13 mm) and 0.250" (6.35 mm) from the seating plane. Between 0.250" (6.35 mm) and 0.500" (12.7 mm) from the seating plane, a maximum lead diameter of 0.021" (0.53 mm) is specified. Outside of these zones the lead diameter is not controlled.

12

'U' PACKAGE: 3-Pin Plastic Single In-Line
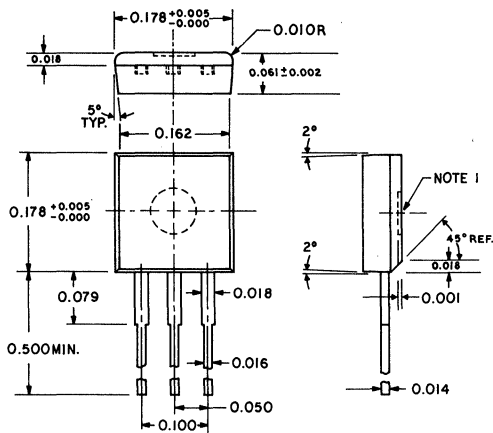
DIMENSIONS IN INCHES

DIMENSIONS IN MILLIMETRES
Based on 1″ = 25.4 mm
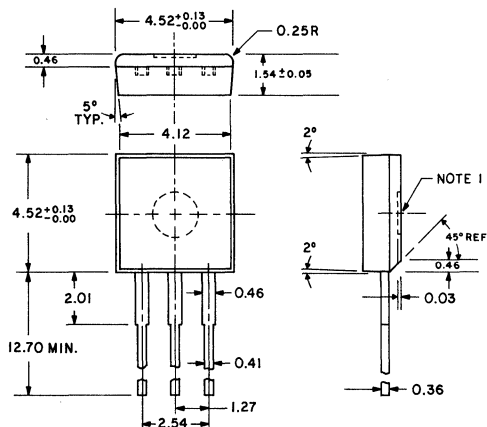
Dwg. No. A-11,901 IN

Dwg. No. A-11,901 MM

NOTE: Lead diameter is controlled in the zone between 0.050″ (0.13 mm) and 0.250″ (6.35 mm) from the seating plane. Between 0.250″ (6.35 mm) and 0.500″ (12.7 mm) from the seating plane, a maximum lead diameter of 0.021″ (0.53 mm) is specified. Outside of these zones the lead diameter is not controlled.

'W' PACKAGE: 12-Pin Plastic Single In-Line
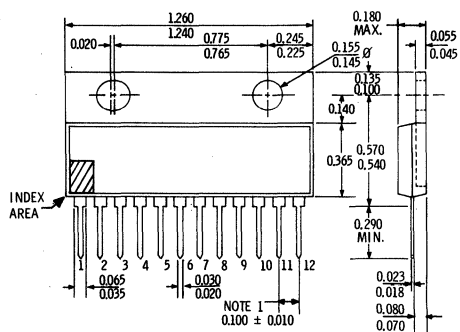
DIMENSIONS IN INCHES

DIMENSIONS IN MILLIMETRES
Based on 1″ = 25.4 mm
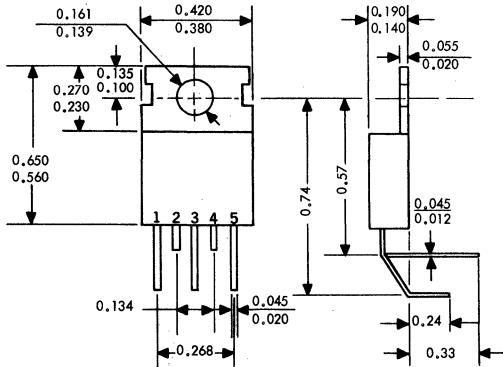

Dwg. No. A-11,138B IN

Dwg. No. A-11,138B MM

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030″ (0.76 mm) max. below seating plane.

'Y' PACKAGE: 3-Pin TO-92/TO-226AA

DIMENSIONS IN INCHES

DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm

Dwg. No. A-10,852A IN

Dwg. No. A-10,852A MM

NOTE: Lead diameter is controlled in the zone between 0.050" (0.13 mm) and 0.250" (6.35 mm) from the seating plane. Between 0.250" (6.35 mm) and 0.500" (12.7 mm) from the seating plane, a maximum lead diameter of 0.021" (0.53 mm) is specified. Outside of these zones the lead diameter is not controlled.

'Z' PACKAGE: 5-Lead TO-220

DIMENSIONS IN INCHES

DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm
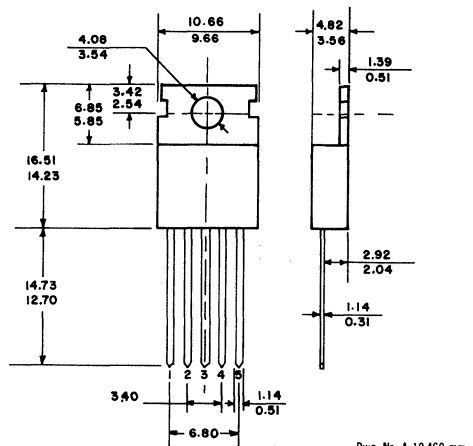
Dwg. No. A-10,460 in

Dwg. No. A-10,460 mm

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030'' (0.76 mm) max. below seating plane.

'ZH' PACKAGE: 5-Lead TO-220
(Horizontal Mount)

DIMENSIONS IN INCHES
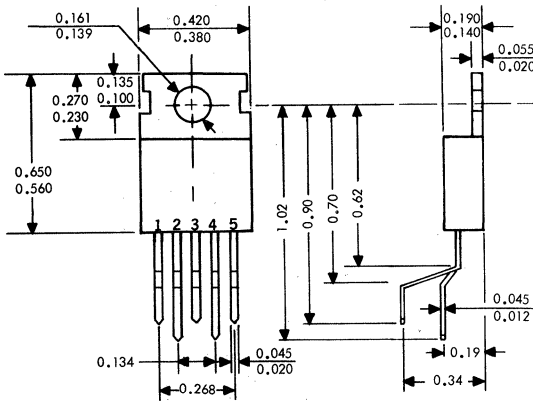

Dwg. No. A-10,462B IN

DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm
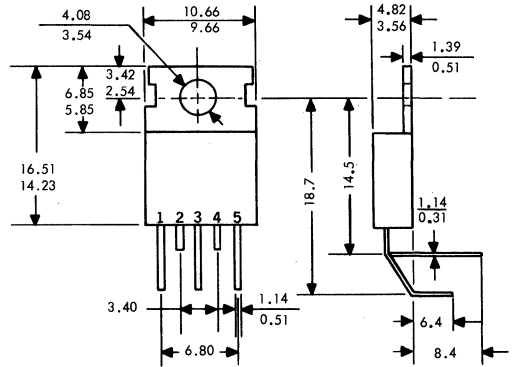
Dwg. No. A-10,462B MM

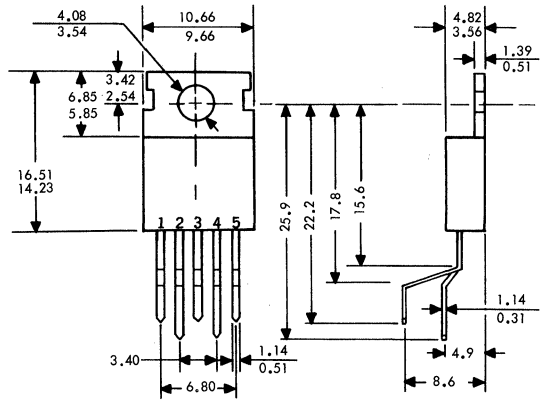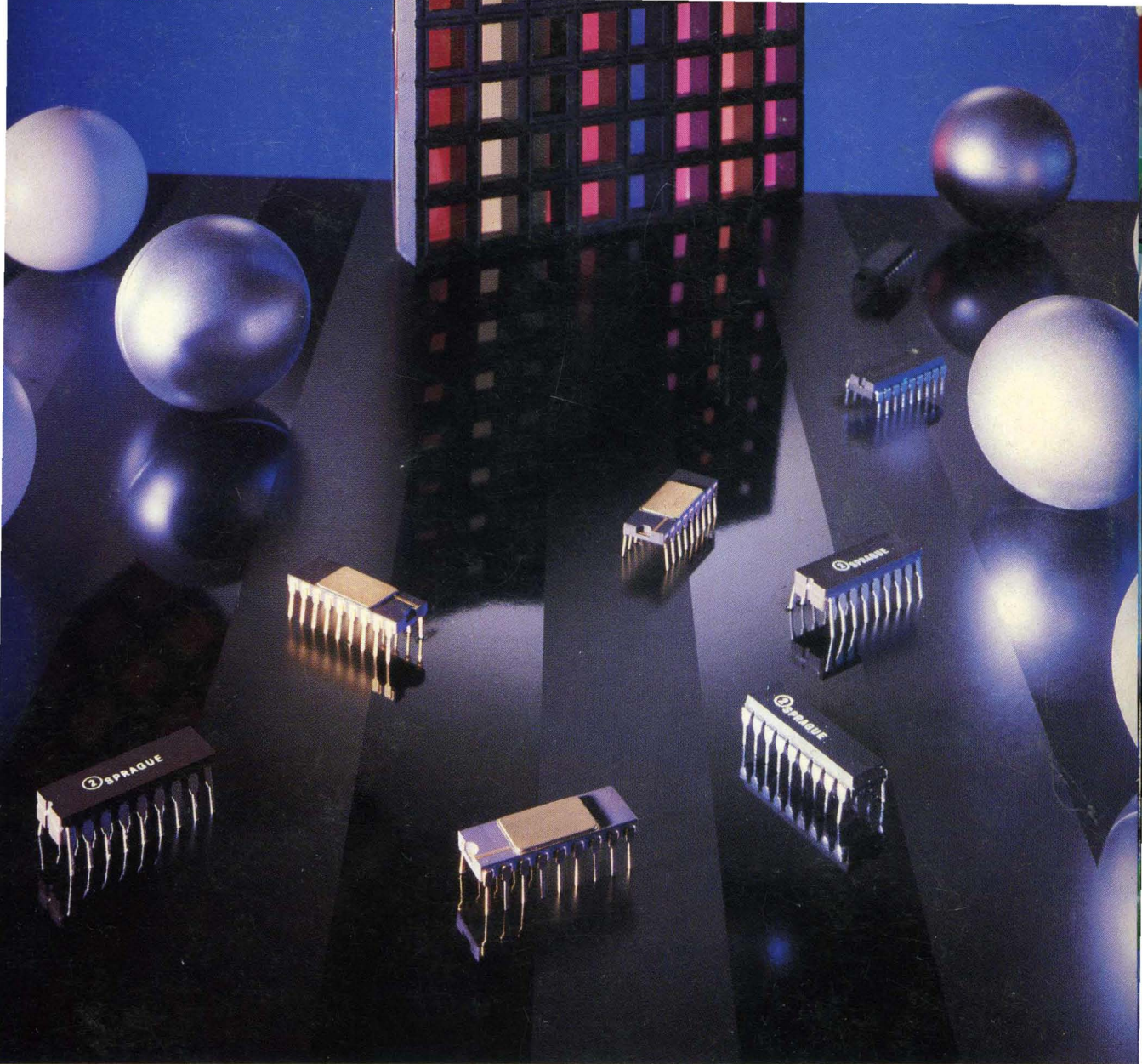## 'ZV' PACKAGE: 5-Lead TO-220
(Vertical Mount)

DIMENSIONS IN INCHES

Dwg. No. A-10,461B IN

DIMENSIONS IN MILLIMETRES
Based on 1'' = 25.4 mm

Dwg. No. A-10,461B MM

NOTES:
1. Lead spacing tolerance is non-cumulative.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Leads missing from their designated positions shall also be counted when numbering leads.
4. Terminal lead standoffs may be omitted and replaced by body standoffs.
5. Lead gauge plane is 0.030'' (0.76 mm) max. below seating plane.

NOTES

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