

High-Performance TTL and FAST Delay Modules

High Performance 5-Tap TTL Delay Modules

Part No.	Tap Delays (ns)					All Taps	
	T _{D1}	T _{D2}	T _{D3}	T _{D4}	T _{D5}	T _{RO}	T _{FO}
TTLDL025	5.0	10.0	15.0	20.0	25.0	2.0	2.0
TTLDL050	10.0	20.0	30.0	40.0	50.0	2.0	2.0
TTLDL075	15.0	30.0	45.0	60.0	75.0	2.0	2.0
TTLDL100	20.0	40.0	60.0	80.0	100.0	2.0	2.0
TTLDL125	25.0	50.0	75.0	100.0	125.0	2.0	2.0
TTLDL150	30.0	60.0	90.0	120.0	150.0	2.0	5.0
TTLDL200	40.0	80.0	120.0	160.0	200.0	2.0	5.0
TTLDL250	50.0	100.0	150.0	200.0	250.0	2.0	5.0
TTLDL500	100.0	200.0	300.0	400.0	500.0	2.0	9.0

Delay Characteristics measured at V_{CC} = 5.0V, 25°C, with 15 pf load per tap @ 1.5V level.

Delay Tolerance ± 1.5 ns or 5% whichever is greater.

Rise time measured @ 0.8V to 2.0V levels.

For minimum input pulse width—contact factory. Designs with pulse widths of less than 15% of delay are available.

High-Performance 5-Tap FAST Delay Modules

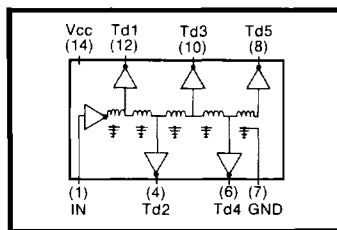
Part No.	Tap Delays (ns)					All Taps	
	T _{D1}	T _{D2}	T _{D3}	T _{D4}	T _{D5}	T _{RO}	T _{FO}
FSTDLO25	5.0	10.0	15.0	20.0	25.0	2.0	2.0
FSTDLO50	10.0	20.0	30.0	40.0	50.0	2.0	2.0
FSTDLO75	15.0	30.0	45.0	60.0	75.0	2.0	2.0
FSTDLO100	20.0	40.0	60.0	80.0	100.0	2.0	2.0
FSTDLO125	25.0	50.0	75.0	100.0	125.0	2.0	2.0
FSTDLO150	30.0	60.0	90.0	120.0	150.0	2.0	5.0
FSTDLO200	40.0	80.0	120.0	160.0	200.0	2.0	5.0
FSTDLO250	50.0	100.0	150.0	200.0	250.0	2.0	5.0
FSTDLO500	100.0	200.0	300.0	400.0	500.0	2.0	9.0

Delay Characteristics measured at V_{CC} = 5.0V, 25°C, with 15 pf load per tap @ 1.5V level.

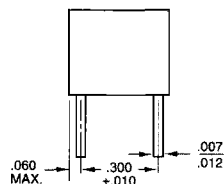
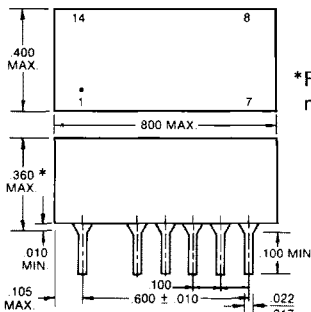
Delay Tolerance ± 1.5 ns or 5% whichever is greater.

Rise time measured @ 0.8V to 2.0V levels.

For minimum input pulse width—contact factory. Designs with pulse widths of less than 15% of delay are available.



*For delay values of 100 ns or greater, max. height is 0.380 in.



High-performance TTLDL delay modules are designed for slightly less stringent requirements than those satisfied by our STTLDL modules (previously described). Note differences in delay variance over temperature.

- ▶ Five tap, lumped constant, active series.
- ▶ Available in low profile, .250 inch high military (MX) series for delays up to 100 ns—contact factory.
- ▶ Temperature coefficient ± 2 ns or ± 2% (whichever is greater) at maximum delay, 0 to 70°C.
- ▶ Designed for leading edge timing. Trailing edge timing available.
- ▶ Compatible with Schottky TTL, FAST, low-power Schottky TTL, FACT, ALS, and AS circuits.
- ▶ Transfer-molded packaging for highest reliability.
- ▶ Military models with temperature range – 55 to + 125°C and ceramic package IC. Add suffix “M” to part number.
- ▶ Military models as above, but with ceramic package IC screened to Mil-Std 883C. Add suffix “MX” to part number.
- ▶ Military models as “MX” above, but with in-house burn-in and thermal shock, add suffix “MY”.
- ▶ For delay lines qualified to Mil-D-83532, see page 4.
- ▶ 10-tap models available, contact factory for details.

Notes

Only the pins specified in the schematics are provided with each package.

Pin numbers shown are for reference only and are not necessarily marked on unit.

Lead material is electro tin plated (alloy 42) or solder dipped.

All specifications are subject to change without notice.

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