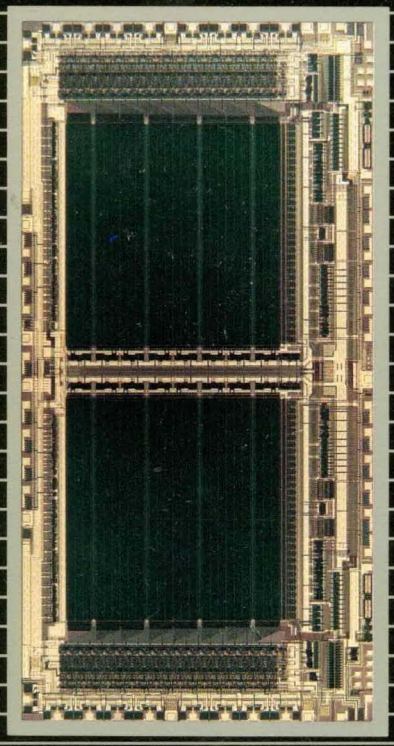
TOSHIBA



STATIC RAM 1990

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.

TOSHIBA STATIC RAM 1990 TAEC

TOSHIBA

STATIC RAM
1990

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CMOS PSEUDO STATIC RAM

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CMOS HIGH SPEED STATIC RAM

BiCMOS HIGH SPEED STATIC RAM

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Static RAM Product Guide

1. CMOS Pseudo Static RAM

CAPACITY	PART NUMBER	ORGANIZATION	ADDRESS ACCESS TIME Max(ns)	OUTPUT ENABLE ACCESS TIME Max(ns)	POWER SUPPLY (V)	POWER DISSIPATION Max (mW)		PIN COUNT	PACKAGE			PACKAGE WIDTH (inch)
						ACTIVE	STANDBY		P	SP	F	
256K Bit	TC51832P/SP/F-85	32Kx8	85	35	5V±10%	303	5.5	28	■	■	■	0.600 (P) 0.300 (SP) 0.450 (F)
	TP51832P/SP/F-10		100	40		248			■	■	■	
	TC51832P/SP/F-12		120	50		220			■	■	■	
	TC51832PL/SPL/FL-85		85	35		303	0.55		■	■	■	
	TC51832PL/SPL/FL-10		100	40		248			■	■	■	
	TC51832PL/SPL/FL-12		120	50		220			■	■	■	
1M Bit	TC518128AP/ASP/AF-80	128Kx8 ($\overline{CE}$1 CE2)	80	35		385	5.5	32	■	■	■	0.600 (P) 0.300 (SP) 0.450 (F)
	TC518128AP/ASP/AF-10		100	40		330			■	■	■	
	TC518128AP/ASP/AF-12		120	50		275			■	■	■	
	TC518128APL/ASPL/AFL-80		80	35		385	1.1		■	■	■	
	TC518128APL/ASPL/AFL-10		100	40		330			■	■	■	
	TC518128APL/ASPL/AFL-12		120	50		275			■	■	■	
	TC518128APL/AFL-80LV		80	35		385	1.1		■		■	
	TC518128APL/AFL-10LV		100	40		330			■		■	
	TC518128APL/AFL-12LV		120	50		275			■		■	
	TC518128AFW/AFWL-80		80	35		385	1.1				■	0.525 (FW)
	TC518128AFW/AFWL-10		100	40		330					■	
	TC518128AFW/AFWL-12		120	50		275					■	
	TC518129AP/ASP/AF-80	128Kx8 ($\overline{CE}$ CS)	80	35		385	5.5		■	■	■	0.600 (P) 0.300 (SP) 0.450 (F)
	TC518129AP/ASP/AF-10		100	40		330			■	■	■	
	TC518129AP/ASP/AF-12		120	50		275			■	■	■	
	TC518129APL/ASPL/AFL-80		80	35		385	1.1		■	■	■	
	TC518129APL/ASPL/AFL-10		100	40		330			■	■	■	
	TC518129APL/ASPL/AFL-12		120	50		275			■	■	■	
	TC518129APL/AFL-80LV		80	35		385	1.1		■		■	
	TC518129APL/AFL-10LV		100	40		330			■		■	
	TC518129APL/AFL-12LV		120	50		275			■		■	
	TC518129AFW/AFWL-80		80	35		385	1.1				■	0.525 (FW)
	TC518129AFW/AFWL-10		100	40		330					■	
	TC518129AFW/AFWL-12		120	50		275					■	

P = PLASTIC DIP, SP = PLASTIC SKINNY DIP, F = PLASTIC FLAT PACKAGE(SOP) , FW = PLASTIC FLAT WIDE PACKAGE(SOP)

2. CMOS Static RAM

CAPACITY	PART NUMBER	ORGANIZATION	ADDRESS ACCESS TIME Max (ns)	OUTPUT ENABLE ACCESS TIME Max (ns)	POWER SUPPLY (V)	POWER DISSIPATION Max (mW)		PIN COUNT	PACKAGE			PACKAGE WIDTH (inch)
						ACTIVE	STANDBY		P	SP	F	
64K Bit	TC5563APL-10	8Kx8	100	50	5V±10%	220	0.550	28	■			0.300
	TC5563APL-12		120	60					■			
	TC5563APL-15		150	70					■			
	TC5563APL-10L		100	50			0.165		■			0.300
	TC5563APL-12L		120	60					■			
	TC5563APL-15L		150	70					■			
	TC5565APL/AFL-10		100	50			0.550		■		■	0.600 (P) 0.300 (SP) 0.450 (F)
	TC5565APL/AFL-12		120	60					■		■	
	TC5565APL/AFL-15		150	70					■		■	
	TC5565APL/AFL-10L		100	50			0.165		■		■	
	TC5565APL/AFL-12L		120	60					■		■	
	TC5565APL/AFL-15L		150	70					■		■	
256K Bit	TC55257BPL/BFL-85	32Kx8	85	45		330	0.550	28	■		■	
	TC55257BSPL-85		85	45						■		
	TC55257BPL/BFL-10		100	50					■		■	
	TC55257BSPL-10		100	50						■		
	TC55257BPL/BFL-85L		85	45			0.165		■		■	
	TC55257BSPL-85L		85	45						■		
	TC55257BPL/BFL-10L		100	50					■		■	
	TC55257BSPL-10L		100	50						■		
	TC55257BPI/BFI-10L		100	50	5V±5%				■		■	
	TC55257BSPI-10L		100	50						■		
1M Bit	TC551001PL/FL-85	128Kx8	85	45	5V±10%	385	0.550	32	■		■	0.600 (P) 0.525 (F)
	TC551001PL/FL-10		100	50					■		■	

P = PLASTIC DIP, SP = PLASTIC SKINNY DIP, F = PLASTIC FLAT PACKAGE(SOP)

3. CMOS High Speed Static RAM (I)

CAPACITY	PART NUMBER	ORGANIZATION	ADDRESS ACCESS TIME Max (ns)	OUTPUT ENABLE ACCESS TIME Max (ns)	POWER SUPPLY (V)	POWER DISSIPATION Max(mW) ACTIVE	POWER DISSIPATION Max(mW) STANDBY	PIN COUNT	PACKAGE P	PACKAGE J	PACKAGE WIDTH (inch)
64K	TC5561P/J-45	64Kx1	45		5V±10%	550	0.550	22(P) 24(J)	■	■	0.300
	TC5561P/J-55		55				0.550		■	■	
	TC5561P/J-70		70				0.550		■	■	
	TC5562P/J-35		35				11.0		■	■	
	TC5562P/J-45		45						■	■	
	TC55416P-15H	16Kx4	15			660	5.5	22	■		
	TC55416P-20H		20			550	5.5		■		
	TC55416P-25H		25			550			■		
	TC55416P-35H		35			440			■		
	TC55417P/J-15H		15	9		660	5.5	24	■	■	
	TC55417P/J-20H		20	10		550			■	■	
	TC55417P/J-25H		25	10		550			■	■	
	TC55417P/J-35H		35	10		440			■	■	
	TC5588P/J-15	8Kx8	15	9		743	5.5	28	■	■	
	TC5588P/J-20		20	10		633			■	■	
	TC5588P/J-25		25	12		633			■	■	
	TC5588P/J-35		35	12		633			■	■	
72K	TC5589P/J-15	8Kx9	15	9		743	5.5		■	■	
	TC5589P/J-20		20	10		633			■	■	
	TC5589P/J-25		25	12		633			■	■	
	TC5589P/J-35		35	12		633			■	■	
256K	TC55328P/J-17	32Kx8	17	9	5V±5%	770	5.5	28	■	■	
	TC55328P/J-20		20	10	5V±10%	770	5.5		■	■	
	TC55328P/J-25		25	12		770			■	■	
	TC55328P/J-35		35	15		660			■	■	
	TC55464P/J-17	64Kx4	17		5V±5%	660	5.5	24	■	■	
	TC55464P/J-20		20		5V±10%	660	5.5		■	■	
	TC55464P/J-25		25			660			■	■	
	TC55464P/J-35		35			550			■	■	
	TC55465P/J-17		17	9	5V±5%	660	5.5	28	■	■	
	TC55465P/J-20		20	10	5V±10%	660	5.5		■	■	
	TC55465P/J-25		25	12		660			■	■	
	TC55465P/J-35		35	15		550			■	■	
288K	TC55329P/J-17	32Kx9	17	9	5V±5%	770	5.5	32	■	■	
	TC55329P/J-20		20	10	5V±10%	770	5.5		■	■	
	TC55329P/J-25		25	12		770			■	■	
	TC55329P/J-35		35	15		550			■	■	

P = PLASTIC DIP, J = PLASTIC SOJ

3. CMOS High Speed Static RAM (II)

CAPACITY	PART NUMBER	ORGANIZATION	ADDRESS ACCESS TIME Max(ns)	OUTPUT ENABLE ACCESS TIME Max(ns)	POWER SUPPLY (V)	POWER DISSIPATION MAX (mW) ACTIVE	POWER DISSIPATION MAX (mW) STANDBY	PIN COUNT	PACKAGE P J PLCC	PACKAGE WIDTH (inch)
144K	TC55187T-20	8Kx18 / 4Kx18 X2 Way	20	10	5V±10%	1265	220	52	■	0.800
	TC55187T-25		25	10		1210			■	
	TC55187T-30		30	12		1100			■	
	TC55188T-20		20	10		1265			■	
	TC55188T-25		25	10		1210			■	
	TC55188T-30		30	12		1100			■	

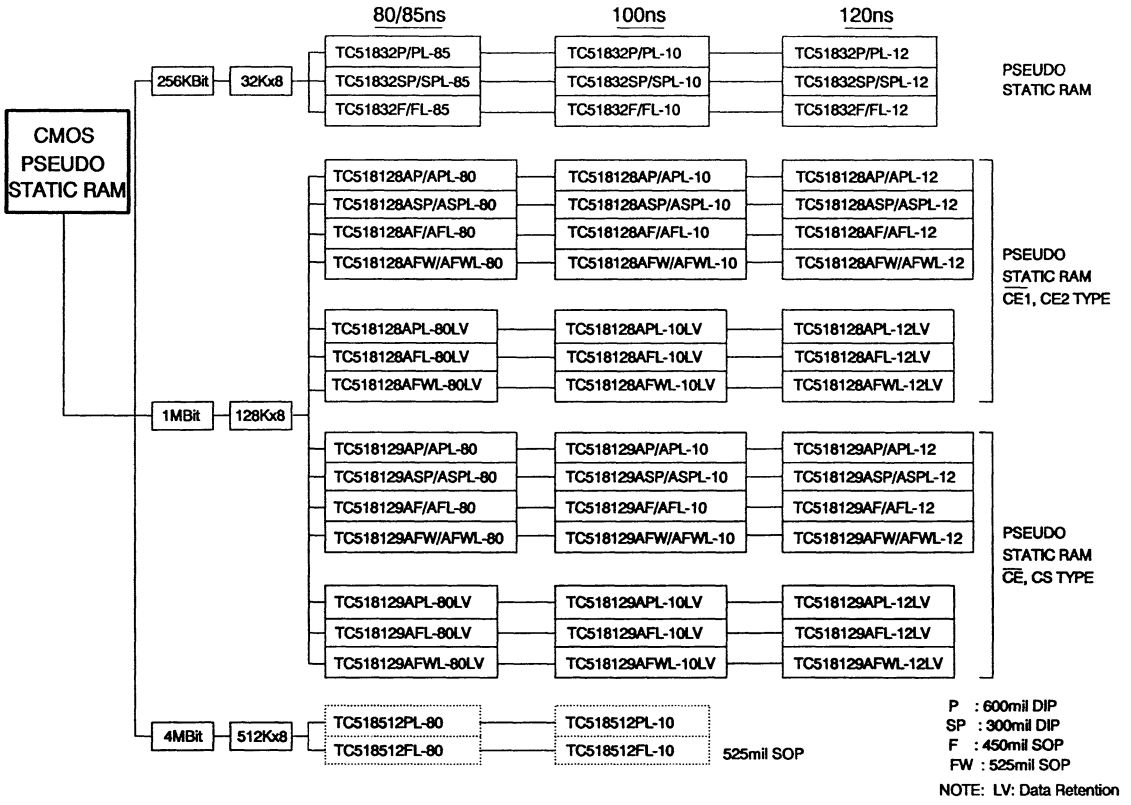
T = PLASTIC LEADLESS CHIP CARRIER(PLCC)

4. BiCMOS High Speed Static RAM

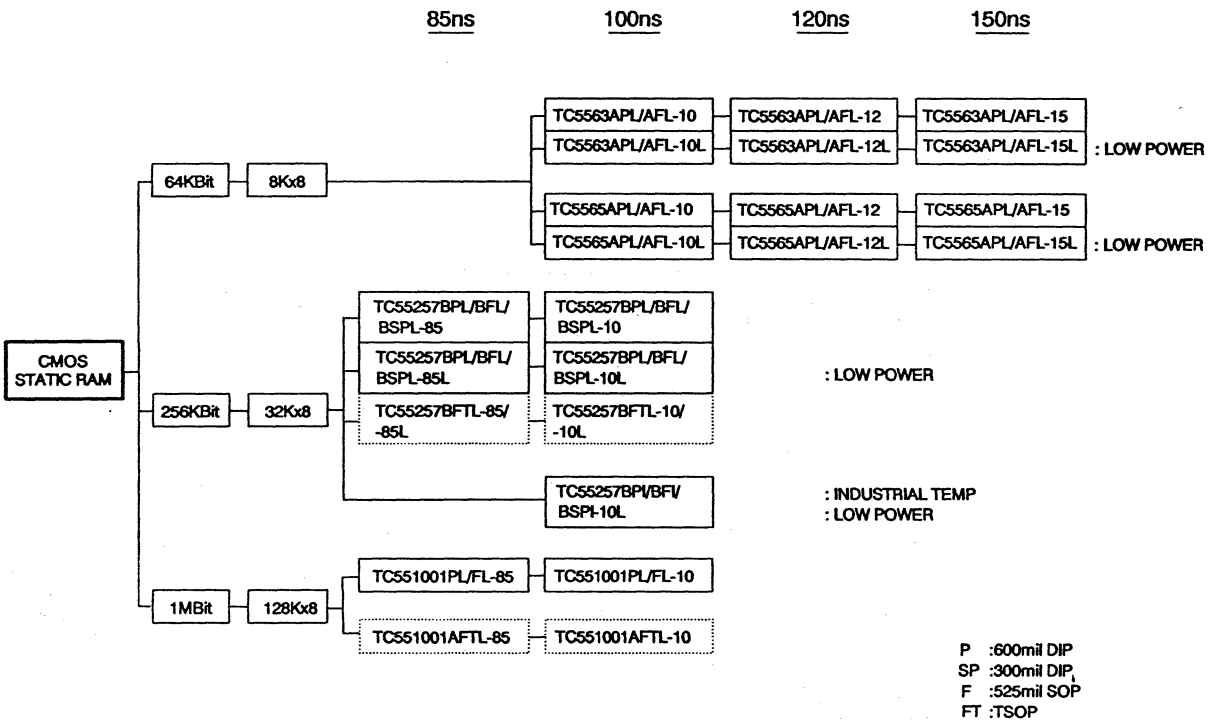
CAPACITY	PART NUMBER	ORGANIZATION	ADDRESS ACCESS TIME Max(ns)	OUTPUT ENABLE ACCESS TIME Max(ns)	POWER SUPPLY (V)	POWER DISSIPATION Max(mW)		PIN COUNT	PACKAGE		PACKAGE WIDTH (inch)
						ACTIVE	STANDBY		P	J	
64K	TC55B417P/J-10	16Kx4	10	5	5V±10%	742.5	55	24	■	■	0.300
	TC55B417P/J-12		12	6					■	■	
	TC55B88P/J-10	8Kx8	10	5		660		28	■	■	
	TC55B88P/J-12		12	6					■	■	

P = PLASTIC DIP, J = PLASTIC SOJ

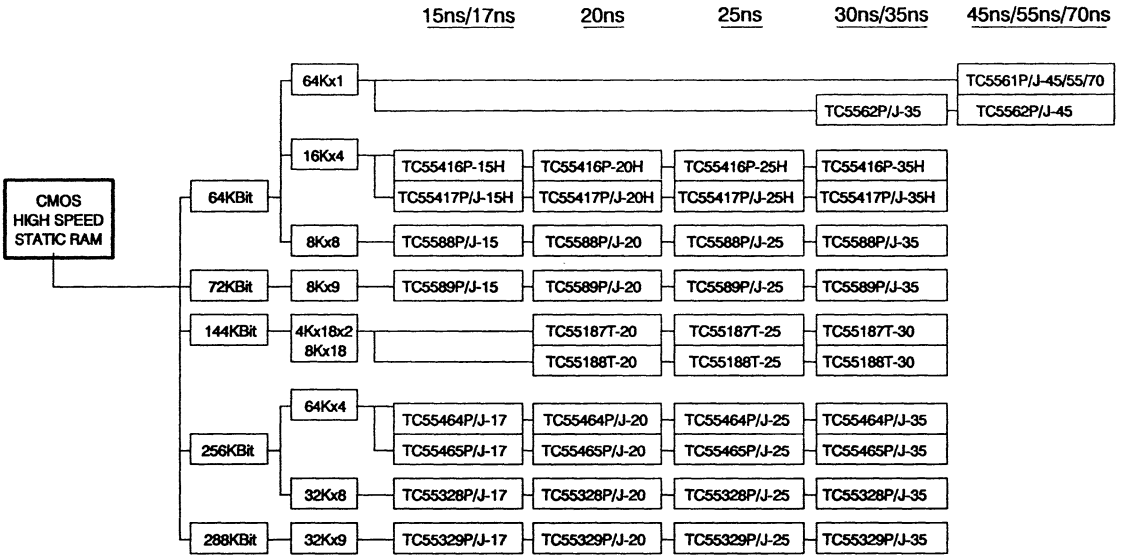
TOSHIBA CMOS PSEUDO STATIC RAM



TOSHIBA CMOS STATIC RAM

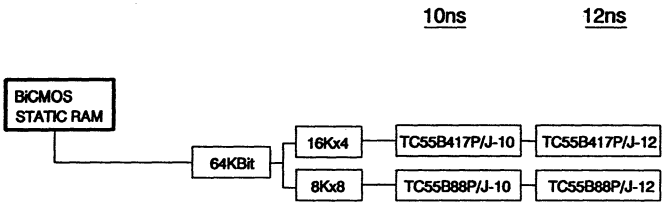


TOSHIBA CMOS HIGH SPEED STATIC RAM



P :300mil DIP
J :300mil SOJ
T :800mil PLCC

TOSHIBA BiCMOS HIGH SPEED STATIC RAM



P :300mil DIP
J :300mil SOJ

Cross Reference

1. CMOS Pseudo Static RAM

Organization	32K x 8			128K x 8			
Package Width	0.6in DIP	0.3in DIP	0.450in SOP	0.6in DIP	0.3in DIP	0.450in SOP	0.525in SOP
TOSHIBA	TC51832P	TC51832SP	TC51832F	TC518128AP	TC518128ASP	TC518128AF	TC518128AFW
HITACHI	HM65256BP	HM65256BSP	HM65256BFP				
NEC	uPD42832C		uPD42832GU				
MOTOROLA				MCM518128		MCM518128	

Organization	128K x 8			
Package Width	0.6in DIP	0.3in DIP	0.450in SOP	0.525 SOP
TOSHIBA	TC518129AP	TC518129ASP	TC518129AF	TC518129AFW
HITACHI	HM658128P			HM658128FP
NEC	uPD428128CZ			uPD428128GW
MOTOROLA	MCM518129		MCM518129	

2. CMOS Static RAM

Organization	8K x 8			32K x 8			128K x 8		
Package Width	0.6in DIP	0.450in SOP	0.3in DIP	0.6in DIP	0.450in SOP	TSOP	0.6in DIP	0.525in SOP	TSOP
TOSHIBA	TC5565APL	TC5565AFL	TC5563APL	TC55257BPL	TC55257BFL	TC55257BFTL	TC551001PL	TC551001FL	TC551001AFTL
FUJITSU	MB8464AP	MB8464APF	MB8464APSK	MB84256	MB8464		MB841000P		
HITACHI	HM6264AP	HM6264AFP	HM6264ASP	HM62256P	HM62256FP	HM62256	HM628128P	HM628128FP	HM628128
MITSUBISHI	M5M5165P	M5M5165FP		M5M256BP	M5M256BFP	M5M256B	M5M1008		M5M1008
NEC	uPD4364C	uPD4364G	uPD4364CX	uPD43256C					
OKI	MSM5165AL	MSM5165AL		MSM51257	MSM51257				
MOTOROLA	MCM6264WP		MCM6264P	MCM6206P			MCM6226P		
IDT	IDT7164LP	IDT7164LSO	IDT7164LTP	IDT71256LP	IDT71256LSO				
VITELIC	V62C64P	V62C64F		V62C256P	V62C256F				
SMOS	SRM2264LC	SRM2264LM		SRM20256LC	SRM20256LM		SRM201000	SRM201000	
SONY	CXK5864BP	CXK5864BM	CXK58257BSP	CXK58257P	CXK58257M		CXK581000P	CXK581000M	
SGS/THOMSON	MK48Z08			MK48Z30					
SHARP	LH5160	LH5160	LH5160	LH52256	LH52256				
SAMSUNG	KM6264			KM62256AP			KM681000		
PERFORMANCE	P4C164								
LATTICE	SR64K8								
CYPRESS	CY7C185		CY7C186						
PANASONIC	MN4464	MN4464S		MN44256	MN44256S				
INMOS	1MS1630								
AMD									
GE/RCA	CDM6264			CDM62256					

3. CMOS High Speed Static RAM - Common I/O (I)

Organization	8K x 8		8K x 9		64K x 1	
Package Width	0.3in DIP	0.3in SOJ	0.3in DIP	0.3in SOJ	0.3in DIP	0.3in SOJ
TOSHIBA	TC5588P	TC5588J	TC5589P	TC5589J	TC5561/2P	TC5561/2J
FUJITSU	MB81C78AP		MB81C79AP	MB81C79APJ	MB81C71AP	MB81C71APJ
HITACHI					HM6287H	
MITSUBISHI	M5M5178P		M5M5179P		M5M5187P	
NEC					uPD4361	
OKI	MSM5178				MSM5187	
MOTOROLA	MCM6264P	MCM6264NJ	MCM6265P	MCM6265NJ	MCM6287P	MCM6287NJ
IDT	IDT7164SP		IDT7169SP		IDT7187SP	IDT7187SY
VITELIC	V63C64S	V63C64K				
SMOS						
SONY	CXK5863AP	CXK5863AJ	CXK5971J	CXK5971J	CXK5164P	CXK5164J
SARATOGA	SSM7164					
SHARP	LH5165/64				LH5261	LH5261
SAMSUNG	KM6865P				KM6165P	
PERFORMANCE	P4C164		P4C163		P4C187	
TI	SMJ68CE64		SMJ69CE72		SMJ61CD64	
CYPRESS	CY7C185P				CY7C187P	CY7C187VC
PANASONIC						
SGS/THOMSON	IMS1630/35LP	IMS1635L	IMS1695P	IMS1695E	IMS1600/5P	IMS1600/5E
AMD	AM99C88H				AM99C641	
LATTICE	SR64K8				SR64K1	
MICRON	MT5C6408				MT5C6401C	

3. CMOS High Speed Static RAM - Common I/O (II)

Organization	16K x 4(w/o OE)	16K x 4 (w/OE)		64K x 4 (w/o OE)	
Package Width	0.3in DIP	0.3in DIP	0.3in SOJ	0.3in DIP	0.3in SOJ
TOSHIBA	**TC55416P**	**TC55417P**	**TC55417J**	**TC55464P**	**TC55464J**
FUJITSU	MB81C74	MB81C75P	MB81C75PJ	MB81C84P	MB81C84PJ
HITACHI	HM6788HP	HM6789P	HM6789JP	HM6708P	HM6708JP
MITSUBISHI	M5M5188P	M5M5189BP	M5M5189BJ	M5M5258P	M5M5258J
NEC	uPD4362	uPD4363		uPD43254	
OKI	MSM5188A				
MOTOROLA	MCM6288P	MCM6290P	MCM6290J	MCM6208P	MCM6208J
IDT	IDT7188SP	IDT7198		IDT71258SP	IDT71258SY
VITELIC	V61C62				
SMOS				SRM21256	
SONY	CXK5464AP	CXK5465P	CXK5465J	CXK54256P	
SHARP	LH5262A		LH5267A	LH52252AD	LH52252AK
SAMSUNG	KM6465P			KM64257P	KM64257J
PERFORMANCE	P4C188	P4C198		P4C1258	P4C1258
TI	SMJ64C64			SMJ64C256	
CYPRESS	CY7C164P	CY7C166P	CY7C166V	CY7C194P	
PANASONIC				MN44252	MN44252
SGS/THOMSON	IMS1620/5P	IMS1624/29P	IMS1624/29J	IMS1820P	IMS1820J
AMD	AM99C164	AM99C166		AM99C644	
GE/RCA					
MICRON	MT5C6404	MT5C6405	MT5C6405DJ	MT5C2564	MT5C2564DJ
SARATOGA	SSM7188	SSM7198			
LATTICE	SR64K4	SR64E4		SR256K4	

3. CMOS High Speed Static RAM - Common I/O (III)

Organization	64K x 4(w/OE)		32K x 8		32K x 9	
Package Width	0.3in DIP	0.3in SOJ	0.3in DIP	0.3in SOJ	0.3in DIP	0.3in SOJ
TOSHIBA	**TC55465P**	**TC55465J**	**TC55328P**	**TC55328J**	**TC55329P**	**TC55329J**
FUJITSU			MB8287		MB8289	
HITACHI						
MITSUBISHI						
NEC						
OKI						
MOTOROLA	MCM6209P	MCM6209J	MCM6206P	MCM6206J	MCM6205P	MCM6205J
IDT	IDT61298SP	IDT61298SY	IDT71256SP	IDT71256SY	IDT71259SP	
VITELIC						
SMOS						
SONY			CXK58255AP	CXK58255AJ		
SARATOGA						
SHARP			LH52257		LH52259	
SAMSUNG			KM68257P			
PERFORMANCE			P4C1256	P4C1256		
TI			SMJ68CE256		SMJ68CE288	
CYPRESS	CY7C196P		CY7C198P			
PANASONIC						
SGS/THOMSON	IMS1824P	IMS1824J	IMS1835P	IMS1835J		
AMD			AMD99C328			
GE/RCA						
MICRON	MT5C2565	MT5C2565DJ	MT5C2568	MT5C2568DJ		

3. CMOS High Speed Static RAM - Common I/O (IV)

Organization	4K x 18 x 2 / 8K x 18	4K x 18 x 2 / 8K x 18
Mode	CE/A12 UNLATCHED	CE/A12 LATCHED
TOSHIBA	**TC55187T**	**TC55188T**
VITELIC	V6C330J	V6C328J
TI	SN74AC210	
SONY	CXK7701J	
CYPRESS	CYC183	CYC184
MICRON	MT56C0816	

T: 52 Pin PLCC Package JEDEC Standard

4. BiCMOS High Speed Static RAM

Organization	8K x 8		16K x 4 (w/OE)	
Package Width	0.3in DIP	0.3in SOJ	0.3in DIP	0.3in SOJ
TOSHIBA	**TC55B88P**	**TC55B88J**	**TC55B417P**	**TC55B417J**
FUJITSU			MB82B75P	MB82B75PJ
HITACHI			HM6789SP	HM6708P
CYPRESS	CY7B185P	CY7B185V	CY7B166P	CY7B166P
SARATOGA	SSM7164P		SSM7166P	

CMOS Pseudo Static RAM

32,768 WORD x 8 BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC51832 Family is a 256K bit high-speed CMOS Pseudo-Static RAM organized as 32,768 words by 8 bits. The TC51832 Family utilizes one transistor dynamic memory cell array with CMOS peripheral circuitry to achieve large capacity, high speed accesses, and low power requirements, using a single 5V power supply. The $\overline{OE}/\overline{RFSH}$ input allows two types of refresh operations: Auto Refresh and Self Refresh. The TC51832 Family has a static RAM-like read/write functionality, which allows easy interfacing to a microprocessor. The TC51832 Family is pin-compatable with the 256K bit static RAM. The TC51832P is offered in a standard 28 pin 0.6 inch and 0.3 inch width plastic DIP. The TC51832F is offered in a standard 28 pin 0.450 inch width small out-line plastic flat package.

FEATURES

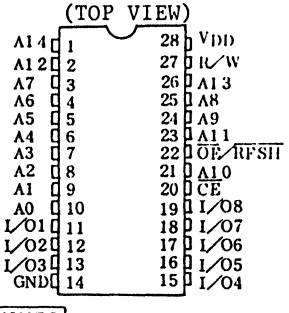
- Organization: 256K bit(32,768 word × 8 bit)
- Fast Access Time and Low Power Dissipation

	TC51832P Family		
	-85	-10	-12
t_{CEA} $\overline{CE}$ Access Time	85ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	135ns	160ns	190ns
P_D -Operating- Max.	303mW	248mW	220mW
Self Refresh Current	1mA/100μA (-L)		

- Single Power Supply: 5V±10%
- Auto refresh uses an internal counter.
- Self refresh uses an internal timer.
- All inputs and outputs: TTL compatible
- 256 refresh cycle/4ms
- Pin Compatible: 256K SRAM TC55257
- Logic Compatible: SRAM R/W Pin
- 28 pin Standard Plastic PKG
  P/PL : 600 mil DIP
  SP/SPL: 300 mil DIP
  F/FL : 450 mil SOP

PIN CONNECTION

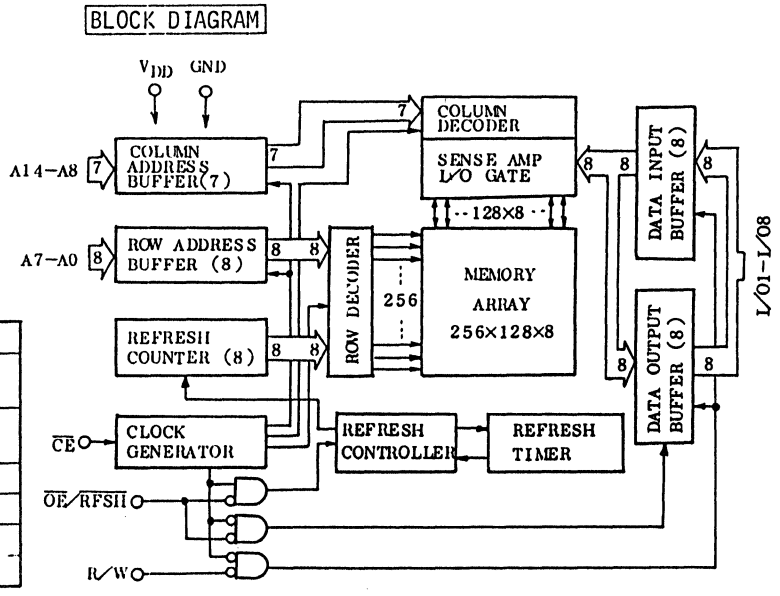
(TOP VIEW)



PIN NAMES

A0 ∿ A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/\overline{RFSH}$	Output Enable/ Refresh Input
$\overline{CE}$	Chip Enable Input
I/O1 ∿ I/O8	Data Inputs/Outputs
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	-1.0 ∿ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ∿ 7.0	V	1
V_{DD}	Power Supply Voltage	-1.0 ∿ 7.0	V	1
T_{OPR}	Operating Temperature	0 ∿ 70	°C	1
T_{STG}	Storage Temperature	-55 ∿ 150	°C	1
T_{SOLDER}	Soldering Temperature·Time	260 • 10	°C•sec	1
P_D	Power Dissipation	600	mW	1
I_{OUT}	Short Circuit Output Current	50	mA	1

DC RECOMMENDED OPERATING CONDITIONS (Ta=0 ∿ 70°C)

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNIT	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{DD}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		PERIOD	MIN.	MAX.	UNITS	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE}$, Address Cycling: t_{RC}=t_{RC} MIN.		135ns	-	55	mA	3,4
			160ns	-	45		
			190ns	-	40		
I_{DDS1}	Standby Current 1 $\overline{CE}$=$\overline{OE}$/$\overline{RFSH}$=V_{IH}	TC51832P/SP/F		-	2	mA	
		TC51832PL/SPL/FL		-	1		
I_{DDS2}	Standby Current 2 $\overline{CE}$=$\overline{OE}$/$\overline{RFSH}$=V_{DD}-0.2V	TC51832P/SP/F		-	1	mA	
		TC51832PL/SPL/FL		-	100	µA	
I_{DDF}	Self Refresh Current $\overline{CE}$=V_{DD}-0.2V, $\overline{OE}$/$\overline{RFSH}$=0.2V	TC51832P/SP/F		-	1	mA	
		TC51832PL/SPL/FL		-	100	µA	
$I_{I(L)}$	Input Leakage Current 0V≦V_{IN}≦V_{DD}, All other inputs not under test=0V			-10	10	µA	
$I_{O(L)}$	Output Leakage Current Output Disable, 0V≦V_{OUT}≦V_{DD}			-10	10	µA	
V_{OH}	Output High Level I_{OUT}=-5mA			2.4	-	V	
V_{OL}	Output Low Level I_{OUT}=4.2mA			-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD}=5V±10%, Ta=0~70°C) (NOTES:5,6,7,8,9)

SYMBOL	PARAMETER	-85		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	135	-	160	-	190	-	ns	
t_{RMW}	Read Modify Write Cycle Time	200	-	240	-	280	-	ns	
t_{CE}	$\overline{CE}$ Pulse Width	85	10,000	100	10,000	120	10,000	ns	
t_{P}	$\overline{CE}$ Precharge Time	40	-	50	-	60	-	ns	
t_{CEA}	$\overline{CE}$ Access Time	-	85	-	100	-	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	10	-	10	-	10	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{WLZ}	Output Active from End of Write Enable	0	-	0	-	0	-	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	10
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	10
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	10
t_{OHC}	$\overline{OE}$ Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	
t_{OSC}	$\overline{OE}$ Set-Up Time Referenced to $\overline{CE}$	10	-	10	-	10	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	
t_{WP}	Write Pulse Width	60	-	70	-	85	-	ns	
t_{WCH}	Write Command Hold Time	60	-	70	-	85	-	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	60	-	70	-	85	-	ns	
t_{DSW}	Data Set-Up Time Referenced to R/W	35	-	40	-	50	-	ns	11
t_{DSC}	Data Set-Up Time Referenced to $\overline{CE}$	35	-	40	-	50	-	ns	11
t_{DHW}	Data Hold Time Referenced to R/W	0	-	0	-	0	-	ns	11
t_{DHC}	Data Hold Time Referenced to $\overline{CE}$	0	-	0	-	0	-	ns	11
t_{ASC}	Address Set-Up Time	0	-	0	-	0	-	ns	12
t_{AHC}	Address Hold Time	20	-	25	-	30	-	ns	12
t_{FC}	Auto Refresh Cycle Time	135	-	160	-	190	-	ns	
t_{RFD}	$\overline{CE}$ to $\overline{RFSH}$ Delay Time	40	-	50	-	60	-	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	80	8,000	80	8,000	80	8,000	ns	13
t_{FP}	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	13
t_{FCE}	$\overline{RFSH}$ to $\overline{CE}$ Active Delay Time	160	-	190	-	225	-	ns	13
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	-	8,000	-	8,000	-	ns	13
t_{FRS}	$\overline{CE}$ Delay Time from $\overline{RFSH}$ (Self Refresh)	160	-	190	-	225	-	ns	13

(Continued)

SYMBOL	PARAMETER	-85		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{FST}	$\overline{RFSH}$ Set-Up Time (Refresh Counter Test)	10	30	10	30	10	30	ns	
t_{FHT}	$\overline{RFSH}$ Hold Time (Refresh Counter Test)	65	8,000	65	8,000	65	8,000	ns	
t_{REF}	Refresh Period	-	4	-	4	-	4	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

CAPACITANCE (V_{DD}=5V, f=1MHz, Ta=25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
C_{I1}	Input Capacitance (A0 ∿ A14)	-	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, $\overline{OE}$/$\overline{RFSH}$, R/W)	-	7	pF
C_{IO}	Input/Output Capacitance (I/O1 ∿ I/O8)	-	7	pF

NOTE) This parameter is periodically sampled and is not 100% tested.

NOTES:

1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2) All voltages are referenced to GND.

3) IDDO depends on cycle rate.

4) IDDO depends on output loading. Specified values are obtained with the output open.

5) An initial pause of 1ms with high $\overline{CE}$ and high $\overline{OE}/\overline{RFSH}$ are required after power-up, before proper device operation is achieved.

6) AC measurements assume t_T=5ns.

7) V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

8) Measured with a load equivalent to 2 TTL loads and 100pF.

9) The $\overline{OE}/\overline{RFSH}$ input operates as the output enable input ($\overline{OE}$) and refresh control input ($\overline{RFSH}$) under the condition of that $\overline{CE}$=V_{IL} and $\overline{CE}$=V_{IH}, respectively.

10) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

11) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW}, t_{DSC}) and hold time (t_{DHW}, t_{DHC}).

12) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore all the address inputs must be valid during t_{ASC} and t_{AHC}.

13) Two refresh operation - auto refresh and self refresh are defined by the $\overline{OE}/\overline{RFSH}$ pulse width under the condition of $\overline{CE}$=V_{IH}.

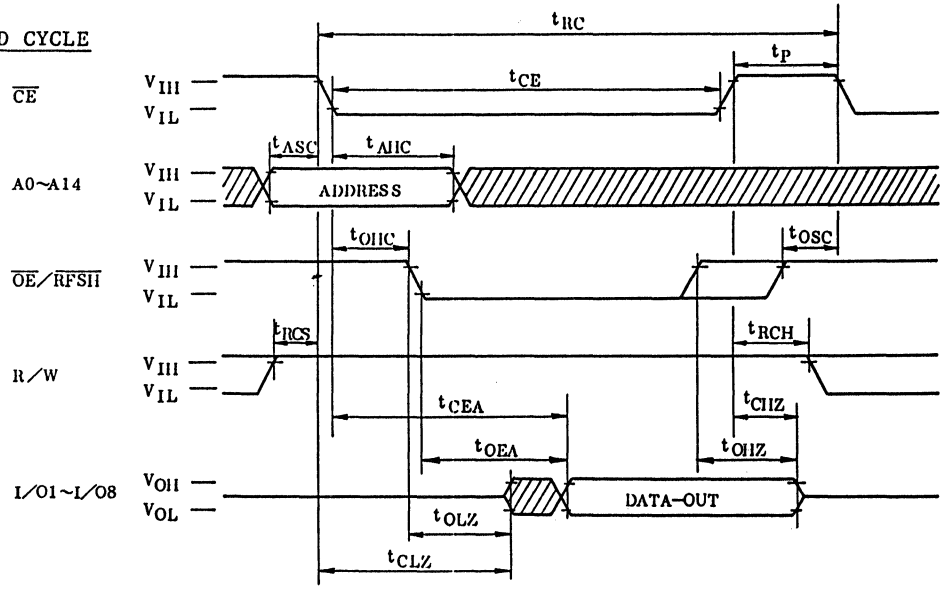
Auto refresh:$\overline{OE}/\overline{RFSH}$ pulse width$\leqq$tFAP (max.)
Self refresh:$\overline{OE}/\overline{RFSH}$ pulse width$\geqq$tFAS (min.)

The following timing parameter must be kept for proper device operation after refresh

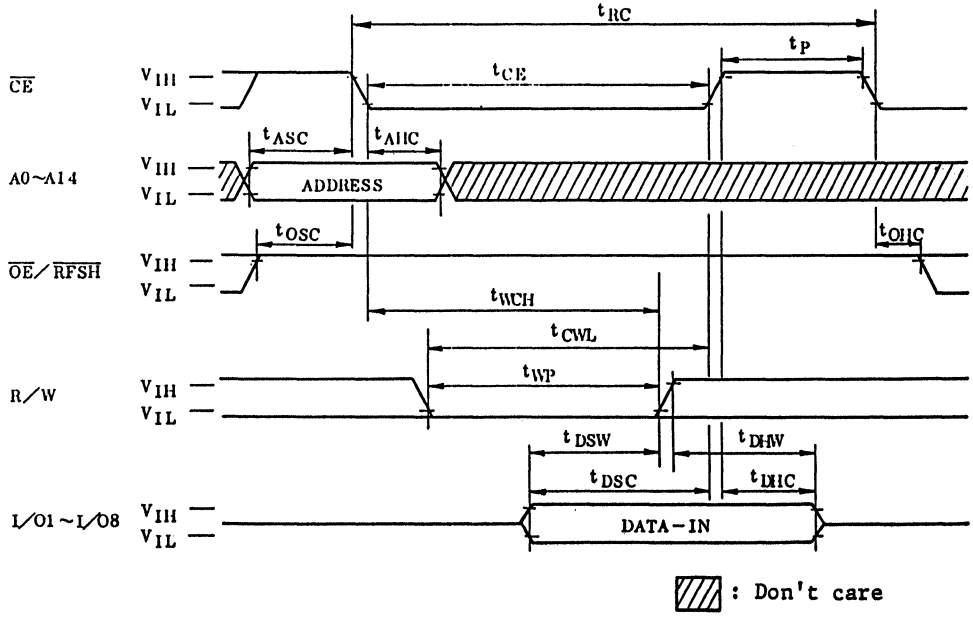
Auto refresh:tFCE
Self refresh:tFRS

TIMING CHART

READ CYCLE

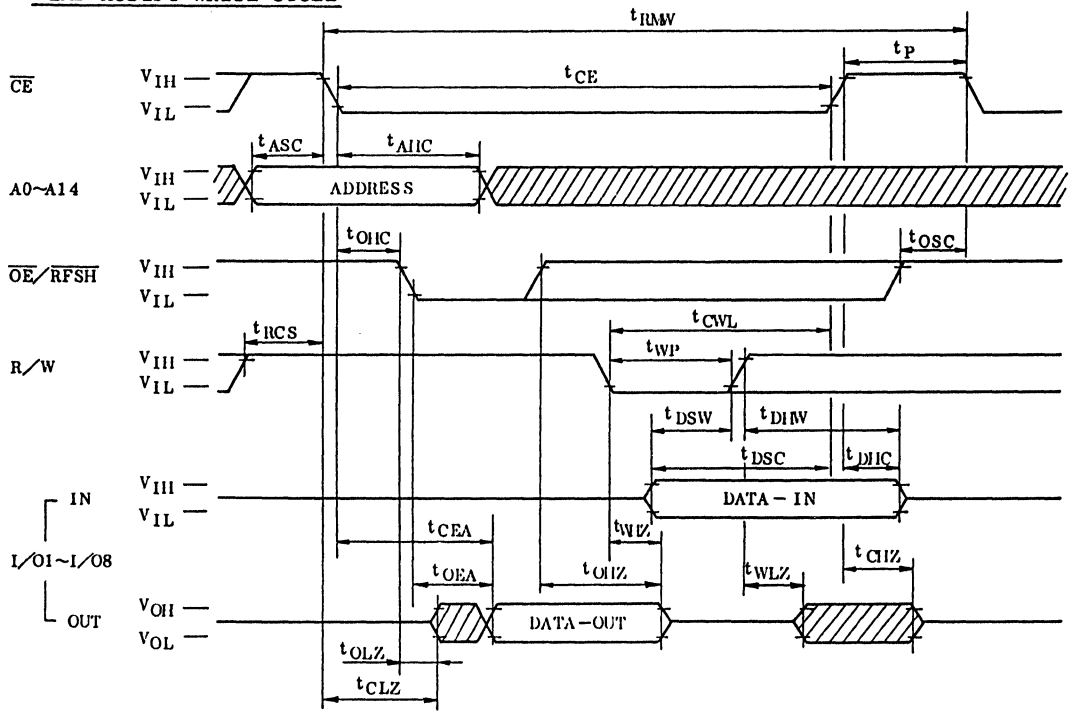


WRITE CYCLE

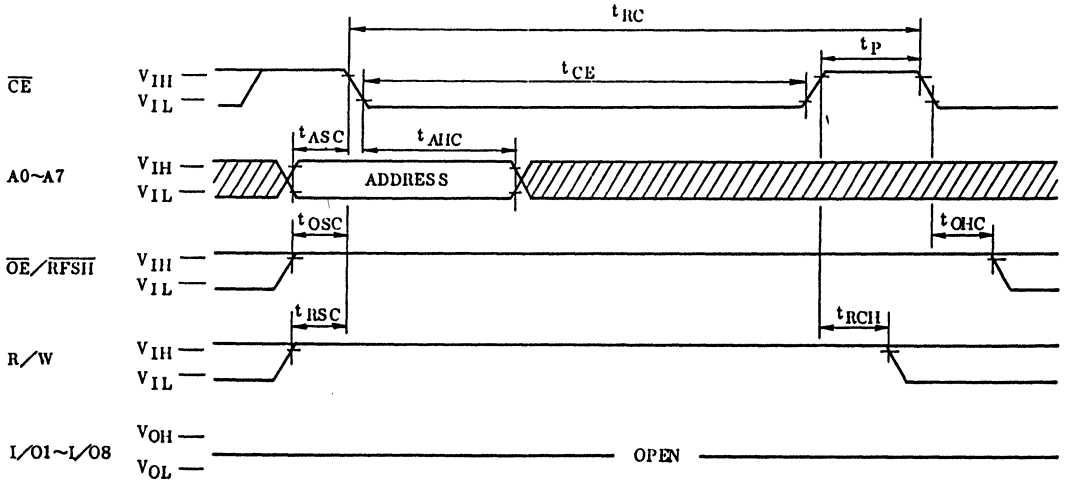


: Don't care

READ MODIFY WRITE CYCLE

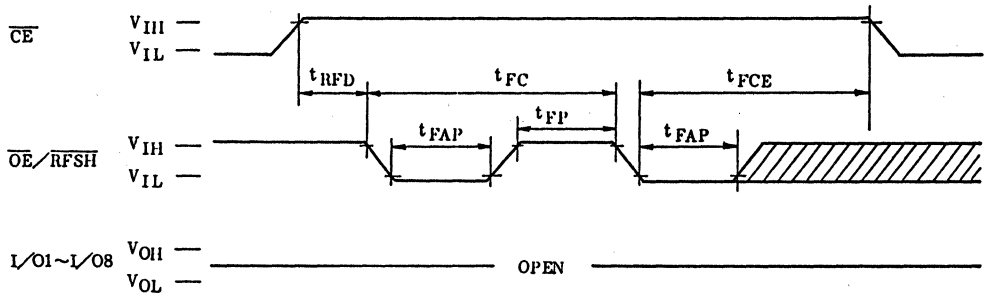


CE ONLY REFRESH CYCLE



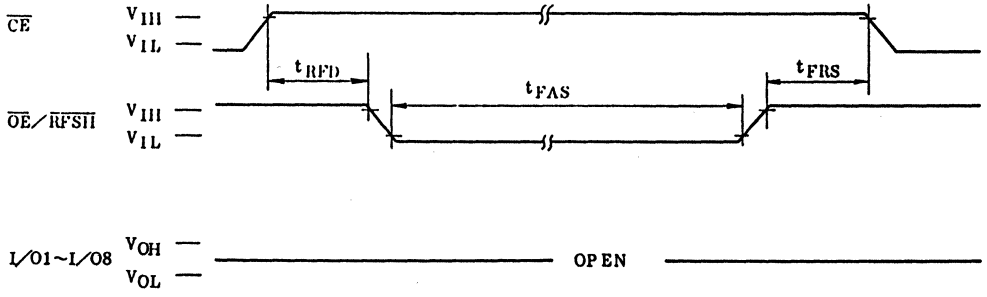
: Don't care

AUTO REFRESH CYCLE



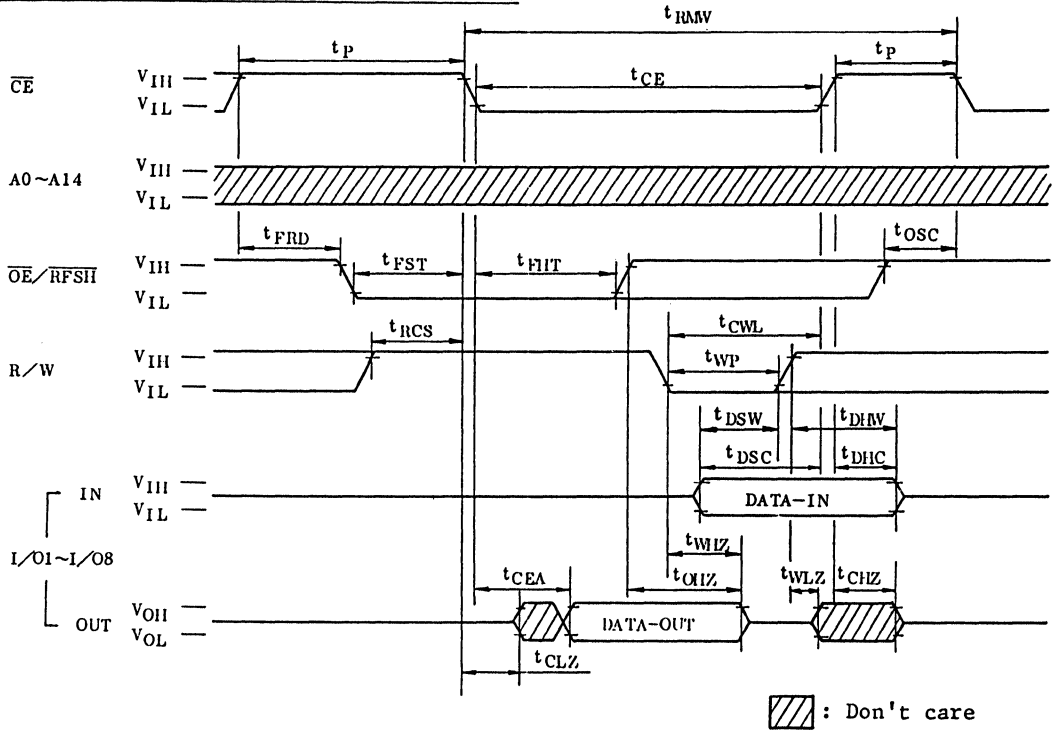
Note) A0 ∿ A14, R/W=Don't care ▨: Don't care

SELF REFRESH CYCLE



Note) A0 ∿ A14, R/W=Don't care

REFRESH COUNTER TEST CYCLE (READ WRITE)



REFRESH COUNTER TEST

The internal refresh operation of TC51832P family can be tested by REFRESH COUNTER TEST. This cycle performs READ/WRITE operation taking the internal counter address as row address and fixed zero as column address.

The test procedure is as follows.

① Write "0" into all the memory cells at normal write mode.

② Read "0" out and write "1" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.

③ Check "1" out of 256 bits at normal read mode, which was written at ②.

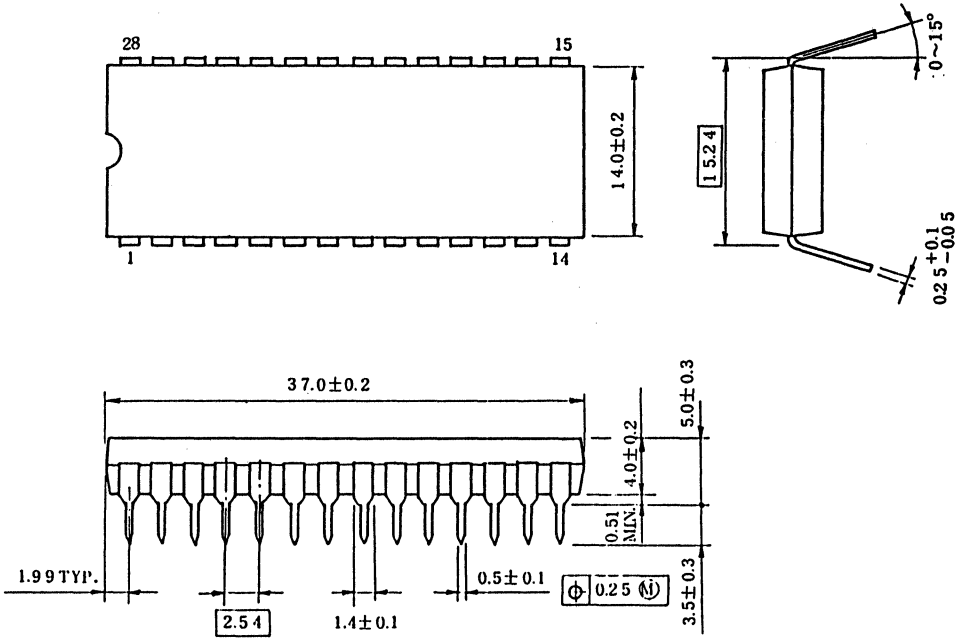
④ Read "1" out and write "0" in each cell by performing REFRESH COUNTER TEST. Repeat this operation 256 times.

⑤ Check "0" out of 256 bits at normal read mode, which was written at ④.

⑥ Perform the above ① to ⑤ the complement data.

OUTLINE DRAWINGS (DIP28-P-600)

Unit in mm



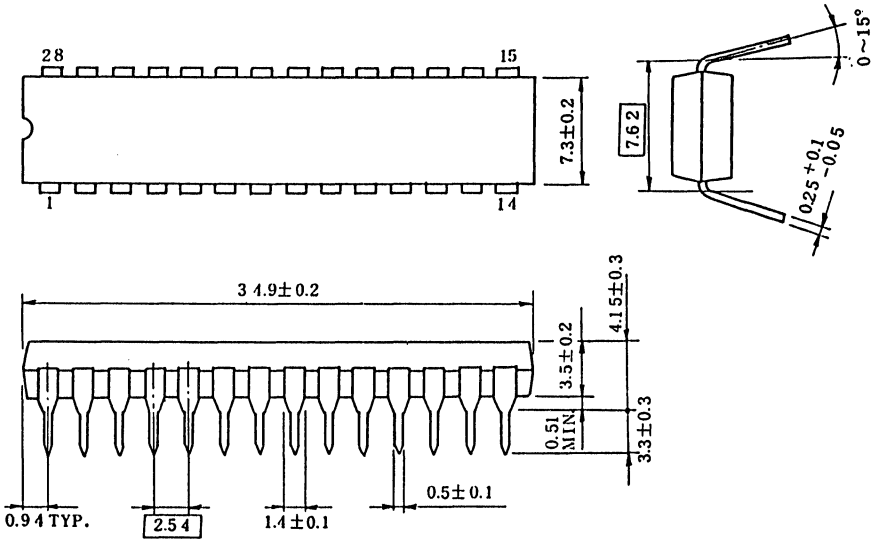
NOTES: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

These outline drawings apply to:

TC51832P-85, TC51832PL-85
TC51832P-10, TC51832PL-10
TC51832P-12, TC51832PL-12

OUTLINE DRAWINGS (DIP28-P-300)

Unit in mm



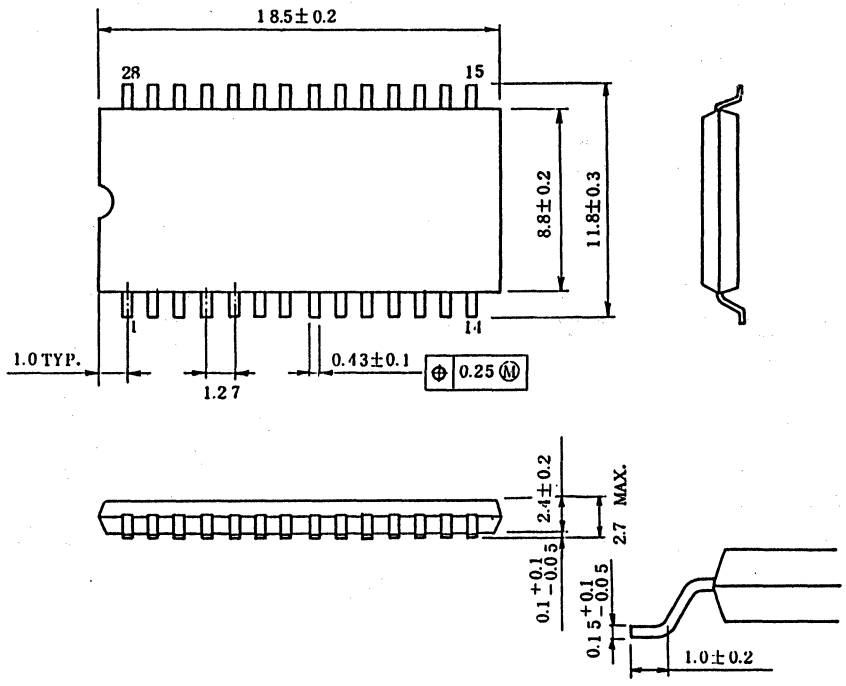
Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

These outline drawings apply to:

TC51832SP-85, TC51832SPL-85
TC51832SP-10, TC51832SPL-10
TC51832SP-12, TC51832SPL-12

OUTLINE DRAWINGS (SOP28-P-450)

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

These outline drawings apply to:

TC51832F-85, TC51832FL-85
TC51832F-10, TC51832FL-10
TC51832F-12, TC51832FL-12

131,072 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC518128A Family is a 1M bit high-speed CMOS Pseudo-Static RAM organized as 131,072 words by 8 bits. The TC518128A Family utilizes one transistor dynamic memory cell array with CMOS peripheral circuitry to achieve large capacity, high speed accesses, and low power requirements, using a single 5V power supply. The $\overline{RFSH}$ input allows two types of refresh operations: Auto Refresh and Self Refresh. The TC518128A Family has a static RAM-like write functionality, which allows easy interfacing to a microprocessor. The TC518128A Family is pin-compatable with the 1M bit static RAM. The TC518128AP is offered in a standard 28 pin 0.6 inch and 0.3 inch width plastic DIP. The TC518128AF is offered in a standard 28 pin 0.450 inch width small out-line plastic flat package.

FEATURES

- Organization: 1M bit (131,072 word × 8bit)
- Fast Access Time and Low Power Dissipation

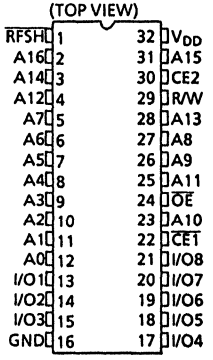
	TC518128AP Family		
	-80	-10	-12
t_{CEA} $\overline{CE}$ Access Time	80ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	1mA/200μA (-L)		

- Single Power Supply: 5V±10%
- Auto refresh uses an internal counter.
- Self refresh uses an internal timer.
- All inputs and outputs : TTL compatible
- 512 refresh cycle / 8ms
- Pin Compatible: 1M SRAM (JEDEC)
- Logic Compatible: SRAM R/W Pin
- 32 Pin Standard Plastic PKG

AP/APL	600 mil DIP
ASP/ASPL	300 mil DIP
AF/AFL	450 mil SOP

PIN CONNECTION

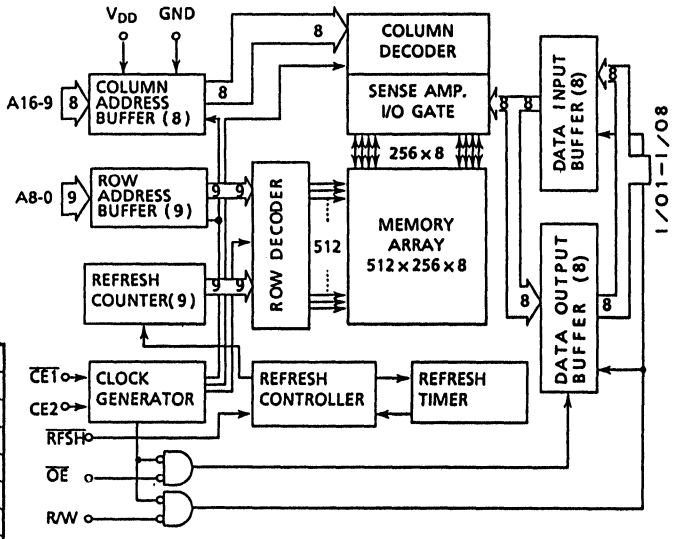
(TOP VIEW)



PIN NAMES

A0 ~ A16	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs / Outputs
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



FUNCTION LOGIC

$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8	CONDITION
L	H	L	H	H	V*	OUT	Read
L	H	*	L	H	V*	IN	Write
L	H	H	H	H	V*	HZ	CE only Refresh
H	*	*	*	L	*	HZ	Auto/Self Refresh
*	L	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by
*	L	*	*	H	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ −1.0V)
* ··· Don't care (6.5V ~ −1.0V)
V* ··· At $\overline{CE1}$ falling edge (CE2 = H) or CE2 rising edge ($\overline{CE1}$ = L), all address inputs are "IN", and at the other condition, the address input are "*"
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	−1.0~7.0	V	1
V_{OUT}	Output Voltage	−1.0~7.0	V	
V_{DD}	Power Supply Voltage	−1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	−55~150	°C	
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		PERIOD	MIN.	TYP.	MAX.	UNITS	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE1}$, CE2, Address cycling: $t_{RC} = t_{RC}$ min.		130ns	–	50	70	mA	3, 4
			160ns	–	40	60		
			190ns	–	35	50		
I_{DDS1}	Standby Current $\overline{CE1} = V_{IH}$ or CE2 = V_{IL} $\overline{RFSH} = V_{IH}$	TC518128AP/ASP/AF		–	–	2	mA	
		TC518128APL/ASPL/AFL		–	–	1		
*I_{DDS2}	Standby Current $\overline{CE1} = V_{DD} - 0.2V$ or CE2 = 0.2V, $\overline{RFSH} = V_{DD} - 0.2V$	TC518128AP/ASP/AF		–	–	1	mA	
		TC518128APL/ASPL/AFL		–	100	200	µA	
I_{DDF1}	Self Refresh Current $\overline{CE1} = V_{IH}$ or CE2 = V_{IL}, $\overline{RFSH} = V_{IL}$	TC518128AP/ASP/AF		–	–	2	mA	
		TC518128APL/ASPL/AFL		–	–	1		
*I_{DDF2}	Self Refresh Current $\overline{CE1} = V_{DD} - 0.2V$ or CE2 = 0.2V, $\overline{RFSH}$ = 0.2V	TC518128AP/ASP/AF		–	–	1	mA	
		TC518128APL/ASPL/AFL		–	100	200	µA	
$I_{I(L)}$	Input Leakage Current 0V ≦ V_{IN} ≦ V_{DD}, All other Inputs not under test = 0V			– 10	–	10	µA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or R/W = V_{IL}), 0V ≦ V_{OUT} ≦ V_{DD}			– 10	–	10	µA	
V_{OH}	Output High Level I_{OH} = – 5mA			2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 4.2mA			–	–	0.4	V	

Note*) In standby mode and self refresh with $\overline{CE1} \geqq V_{DD} - 0.2V$, these specification limits are guaranteed under the condition of CE2 ≧ V_{DD} – 0.2V, or CE2 ≦ 0.2V.

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25 °C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE1}$, CE2, $\overline{OE}$, R/W, $\overline{RFSH}$)	–	7	pF
C_{IO}	Input/Output Capacitance	–	7	pF

Note) This parameter is periodically sampled and is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD} = 5V ± 10%, Ta = 0~70 °C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	–80		–10		–12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	–	160	–	190	–	ns	
t_{RMW}	Read Modify Write Cycle Time	195	–	235	–	280	–	ns	
t_{CE}	CE Pulse Width	80	10,000	100	10,000	120	10,000	ns	13
t_P	CE Precharge Time	40	–	50	–	60	–	ns	
t_{CEA}	CE Access Time	–	80	–	100	–	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	35	–	40	–	50	ns	
t_{CLZ}	CE to Output in Low-Z	30	–	30	–	30	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	0	–	ns	
t_{WLZ}	Output Active from End of Write	0	–	0	–	0	–	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	–	0	–	0	–	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	–	10	–	10	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	
t_{WP}	Write Pulse Width	60	–	70	–	85	–	ns	
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000	ns	
t_{CWL}	Write Command to CE Lead Time	60	10,000	70	10,000	85	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	30	–	35	–	45	–	ns	10
t_{DSC}	Data Set-Up Time from CE	30	–	35	–	45	–	ns	10
t_{DHW}	Data Hold Time from R/W	0	–	0	–	0	–	ns	10
t_{DHC}	Data Hold Time from CE	0	–	0	–	0	–	ns	10
t_{ASC}	Address Set-Up Time	0	–	0	–	0	–	ns	11
t_{AHC}	Address Hold Time	20	–	25	–	30	–	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	–	15	–	15	–	ns	
t_{FC}	Auto Refresh Cycle Time	130	–	160	–	190	–	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from CE	40	–	50	–	60	–	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–	ns	12
t_{FRS}	CE Delay Time from $\overline{RFSH}$ (Self Refresh)	160	–	190	–	225	–	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	–	8	–	8	–	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

NOTES:

1) Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2) All voltages are referenced to GND.

3) I_{DDO} depends on cycle rate.

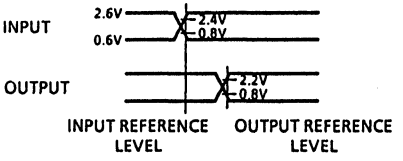
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.

5) An initial pause of 100μs with high $\overline{CE1}$ or low CE2 is required after power-up, before proper device operation is achieved.

6) AC measurements assume $t_T = 5ns$.

7) Timing reference level

Input Level	:	V_{IH} = 2.6V
		V_{IL} = 0.6V
Input Reference Level	:	V_{IH} = 2.4V
		V_{IL} = 0.8V
Output Reference Level	:	V_{OH} = 2.2V
		V_{OL} = 0.8V



8) Measured with a load equivalent to 2 TTL loads and 100pF.

9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE1}$ rising edge and CE2 falling edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).

11) All address inputs are latched at the falling edge of $\overline{CE1}$ and the rising edge of CE2. Therefore the all address inputs must be valid during t_{ASC} and t_{AHC}.

12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$.

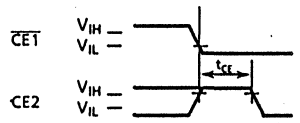
Auto refresh: $\overline{RFSH}$ pulse width $\leqq t_{FAP}$ (max.)

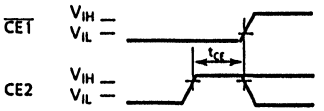
Self refresh: $\overline{RFSH}$ pulse width $\geqq t_{FAS}$ (min.)

The timing parameter (t_{FRS}) must be kept for proper device operation in the following conditions.

- after self refresh
- in case of "$\overline{RFSH}$" = "L" after power-up

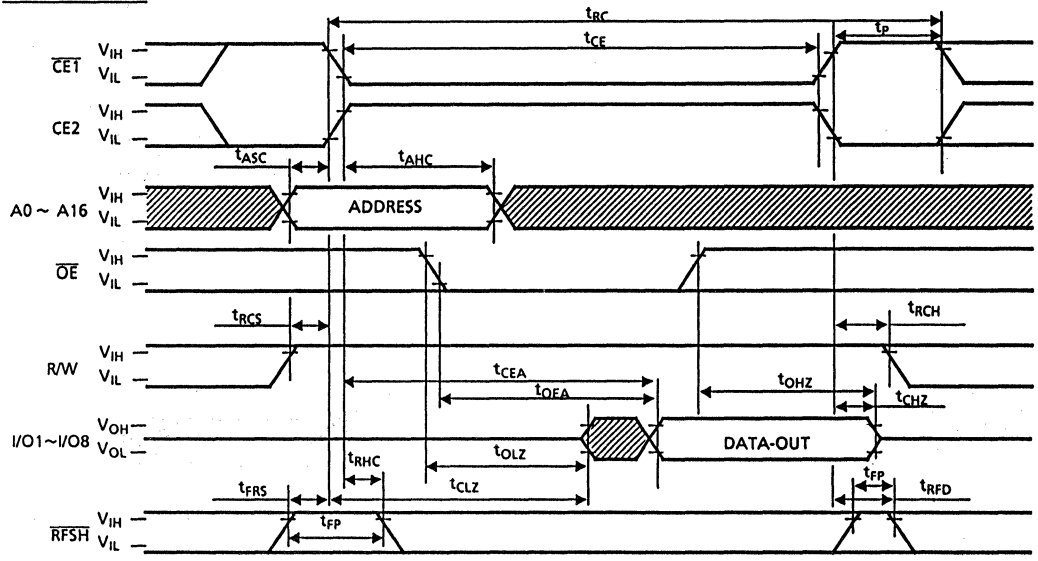
13) The timings, t_{CE} (min.) and T_{CE} (max.), must be kept for proper device operation as follows.



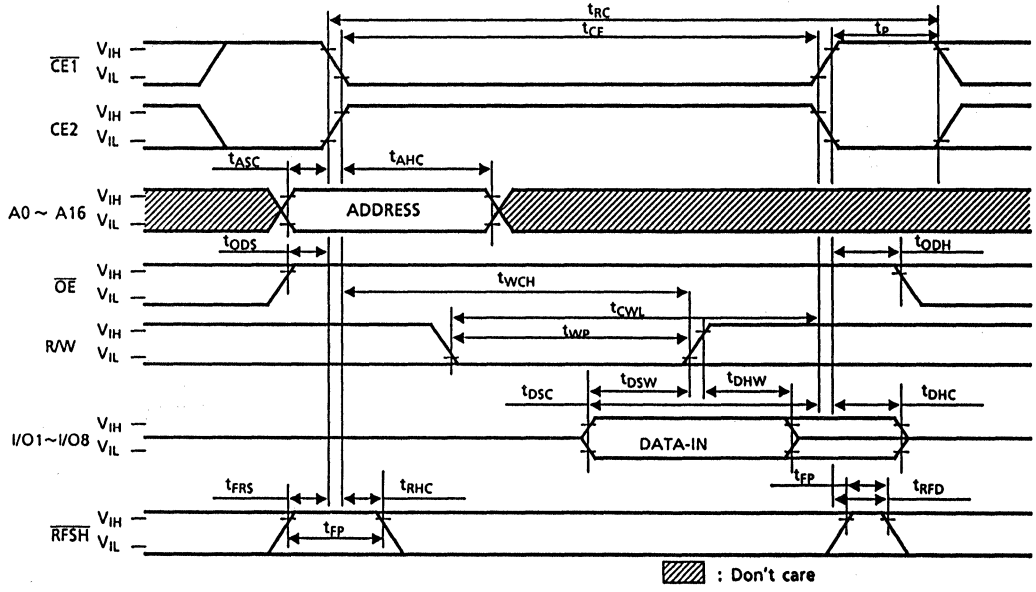


TIMING WAVEFORMS

READ CYCLE

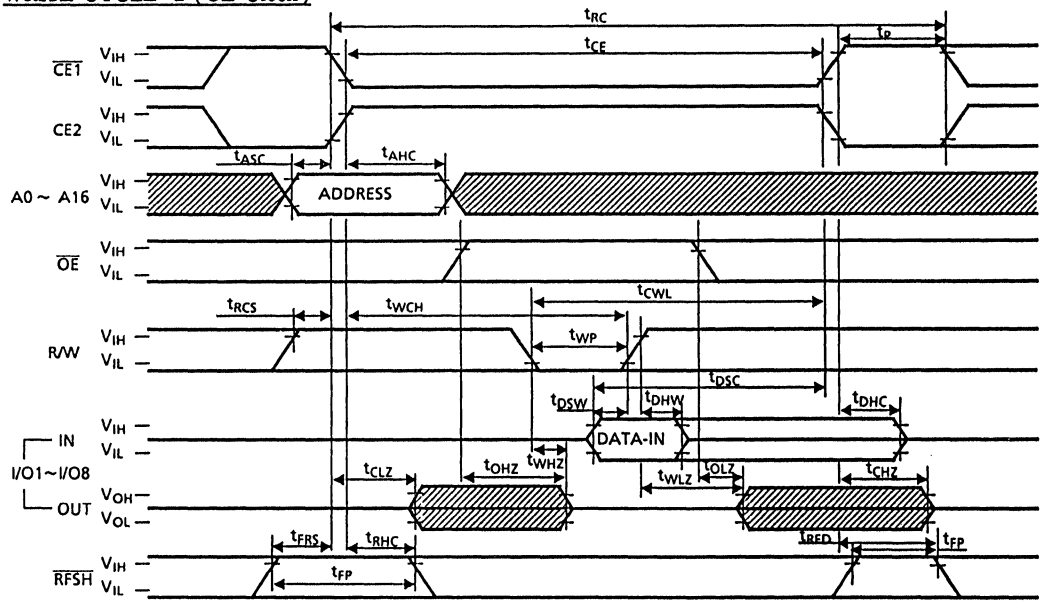


WRITE CYCLE-1 ($\overline{OE}$ Fix High)

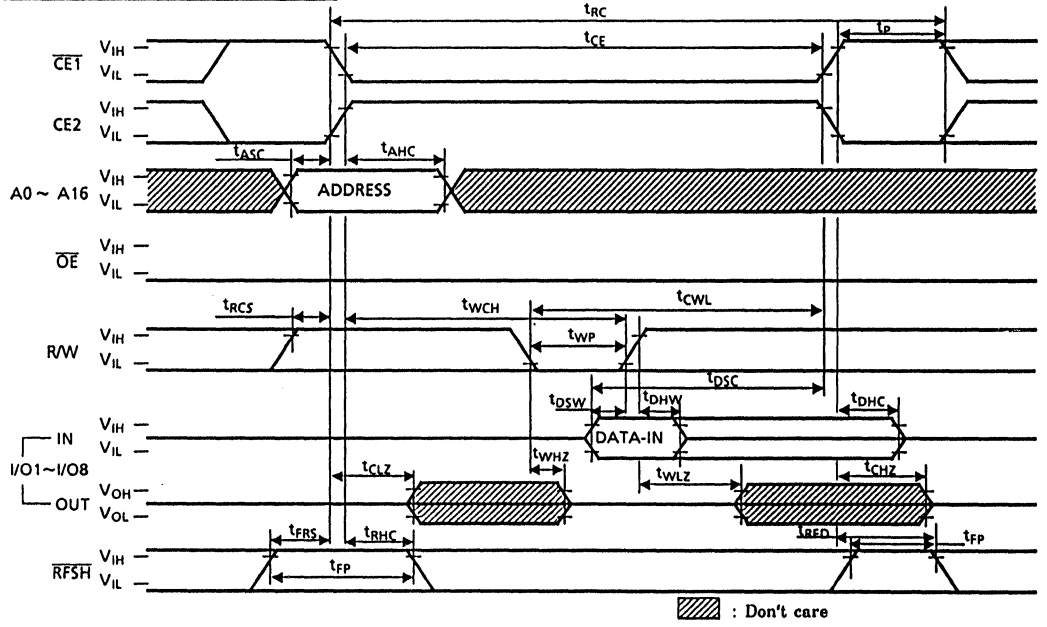


Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

WRITE CYCLE - 2 ($\overline{OE}$ Clock)

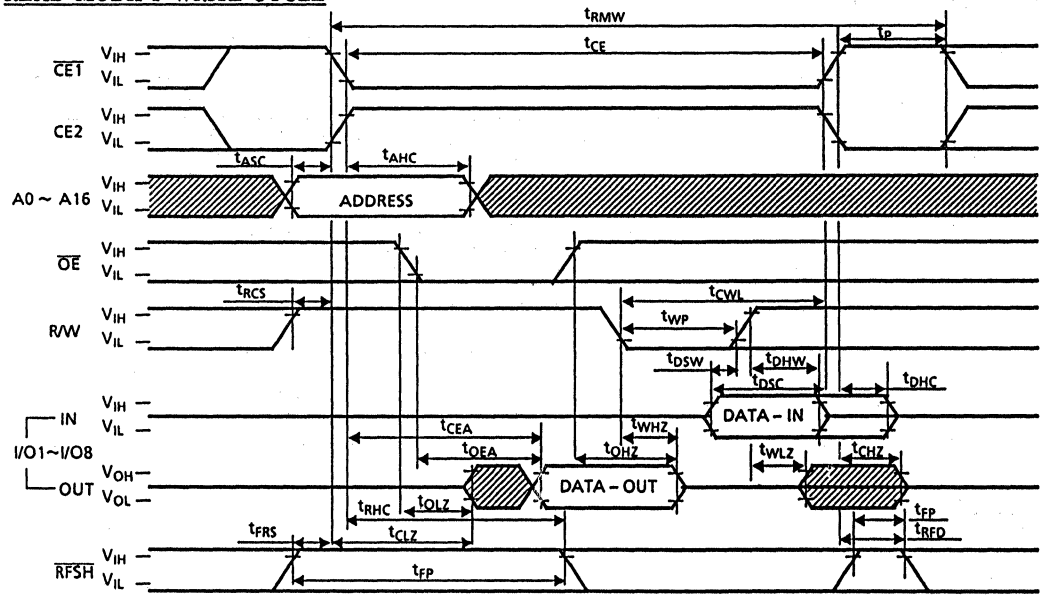


WRITE CYCLE - 3 ($\overline{OE}$ Fix Low)

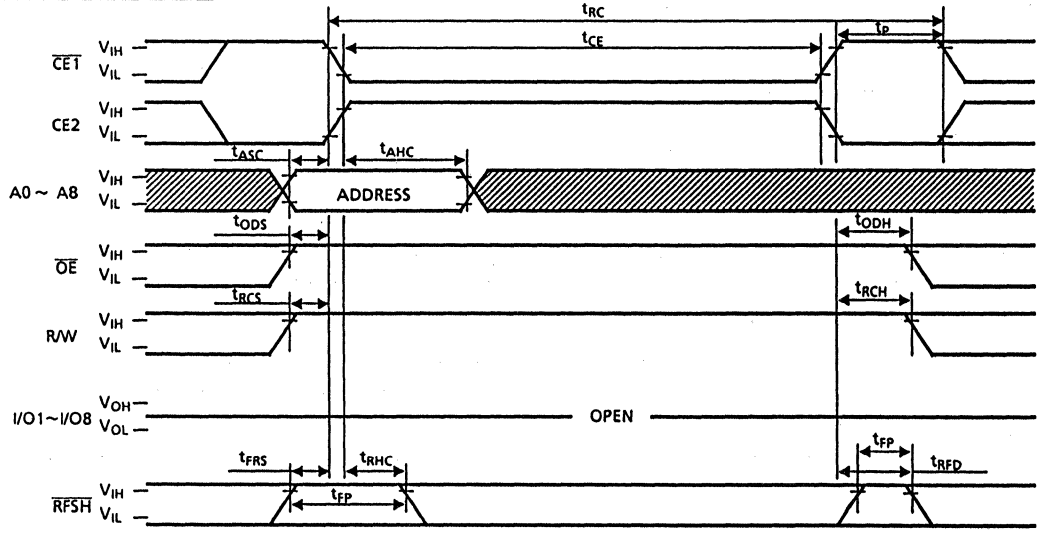


Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

READ MODIFY WRITE CYCLE



CE ONLY REFRESH

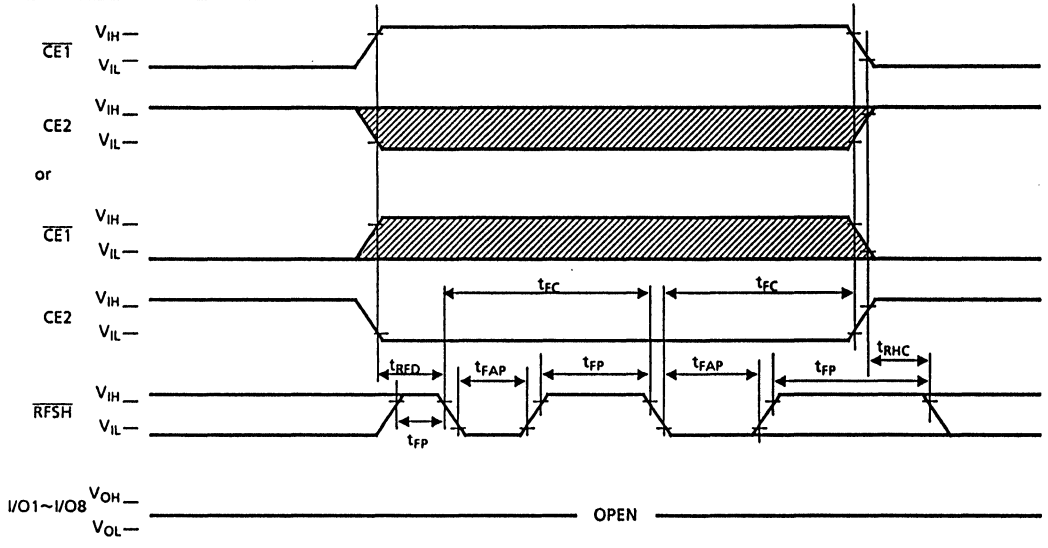


Note : A9 ~ A16 = Don't care

▨: Don't care

Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

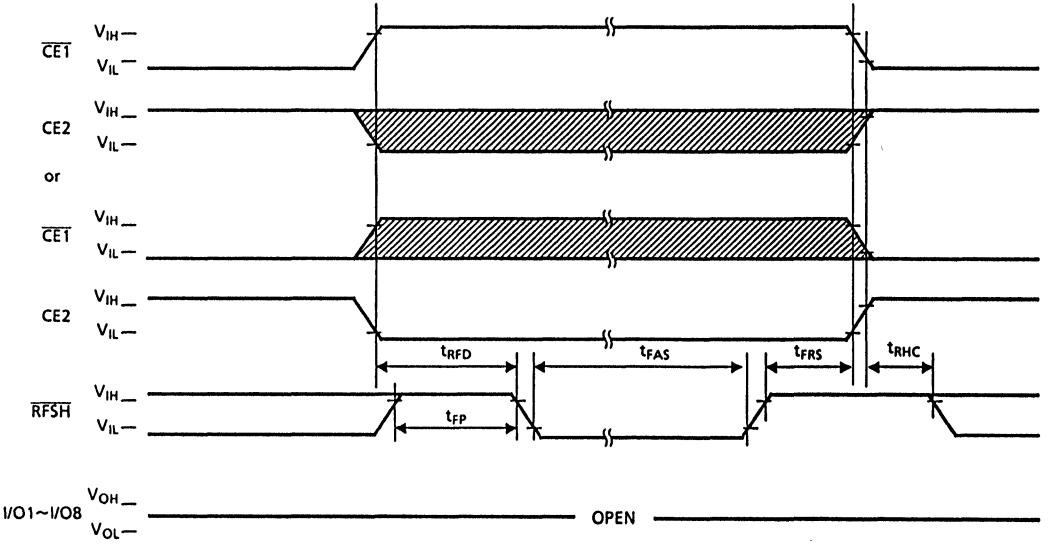
$\overline{RFSH}$ AUTO REFRESH



NOTE : $\overline{OE}$, R/W, A0~A16 = Don't care

▨: Don't care

SELF REFRESH



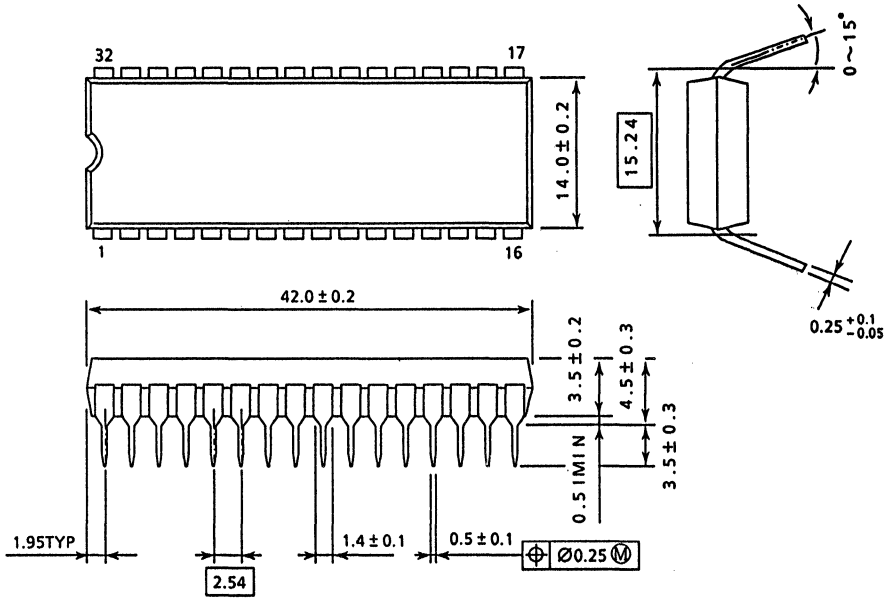
NOTE : $\overline{OE}$, R/W, A0~A16 = Don't care

▨: Don't care

OUTLINE DRAWINGS

(DIP32-P-600)

UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

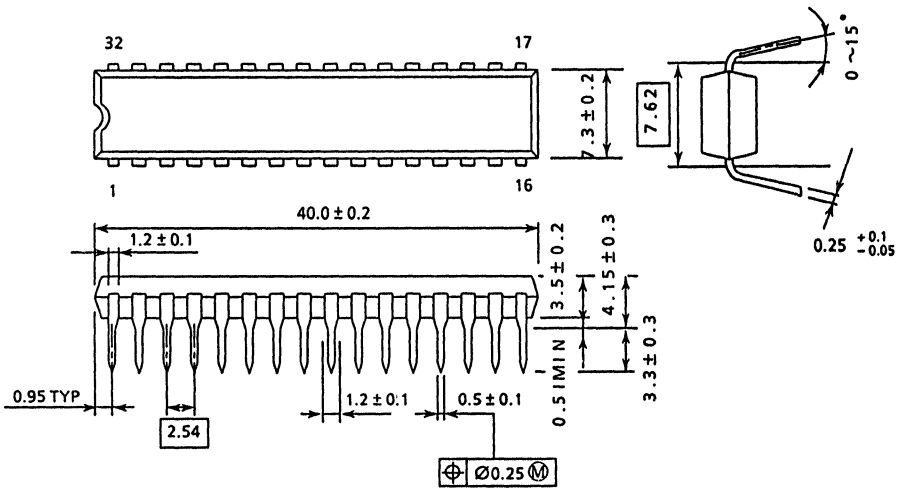
These outline drawings apply to:

TC518128AP-80, TC518128APL-80
TC518128AP-10, TC518128APL-10
TC518128AP-12, TC518128APL-12

OUTLINE DRAWINGS

(DIP32-P-300)

UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

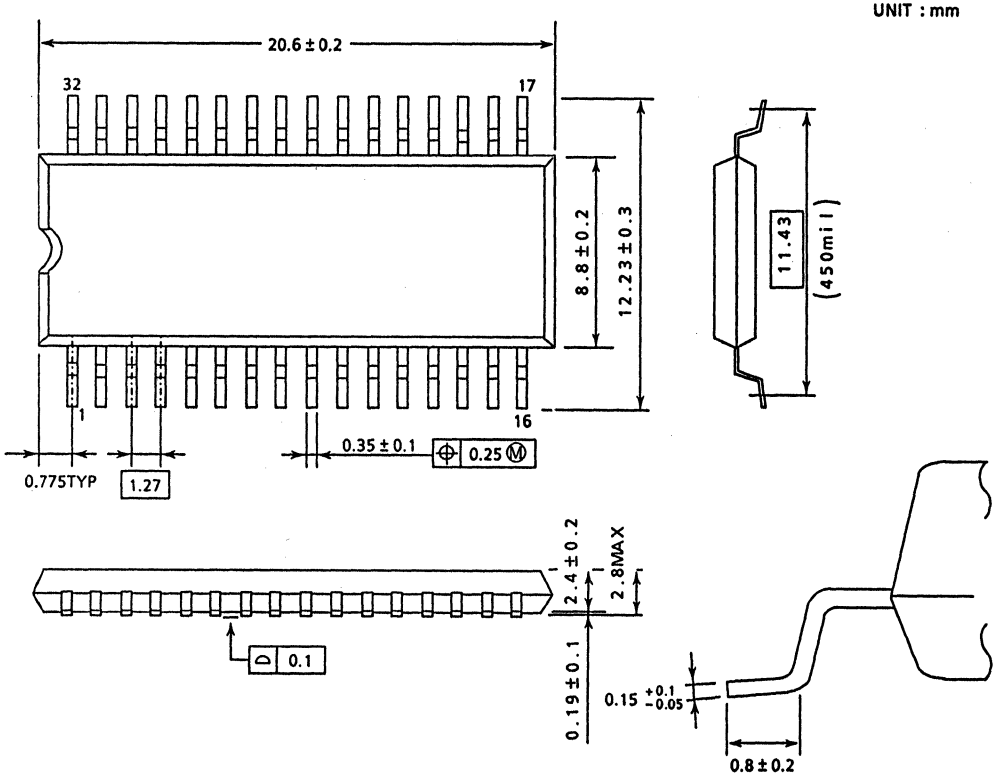
These outline drawings apply to:

TC518128ASP-80, TC518128ASPL-80
TC518128ASP-10, TC518128ASPL-10
TC518128ASP-12, TC518128ASPL-12

OUTLINE DRAWINGS

(SOP32-P-450)

UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

These outline drawings apply to:

TC518128AF-80, TC518128AFL-80
TC518128AF-10, TC518128AFL-10
TC518128AF-12, TC518128AFL-12

131,072 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC518128A-LV Family is a 1M bit high-speed CMOS Pseudo-Static RAM organized as 131,072 words by 8 bits. The TC518128A-LV Family utilizes one transistor dynamic memory cell array with CMOS peripheral circuitry to achieve large capacity, high speed accesses, and low power requirements, using a single 5V power supply. The TC518128A-LV Family offers 3V data retention capability for battery back-up applications. The $\overline{RFSH}$ input allows two types of refresh operations: Auto Refresh and Self Refresh. The TC518128A-LV Family has a static RAM-like read/write functionality, which allows easy interfacing to a microprocessor. The TC518128A-LV Family is pin-compatable with the 1M bit static RAM. The TC518128APL-LV is offered in a standard 28 pin 0.6 inch and 0.3 inch width plastic DIP. The TC518128AFL-LV is offered in a standard 28 pin 0.450 inch width small out-line plastic flat package.

FEATURES

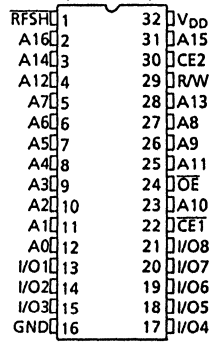
- Organization: 1M bit (131,072 word × 8bit)
- Fast Access Time and Low Power Dissipation

		TC518128APL Family		
		-85	-10	-12
t_{CEA} $\overline{CE}$ Access Time		80ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time		35ns	40ns	50ns
t_{RC} Cycle Time		130ns	160ns	190ns
Power Dissipation		385mW	330mW	275mW
Self Refresh Current	5.5V	200μA		
	3.0V	100μA		

- Single Power Supply: 5V±10%
- Data Retention Supply Voltage: 3.0V ~ 5.5V
- Auto refresh uses an internal counter.
- Self refresh uses an internal timer.
- All inputs and outputs : TTL compatible
- 512 refresh cycle/8ms
- Pin Compatible: 1M SRAM (JEDEC)
- Logic Compatible: SRAM R/W Pin
- 32 Pin Standard Plastic PKG
  - APL 600 mil DIP
  - AFL 450 mil SOP

PIN CONNECTION

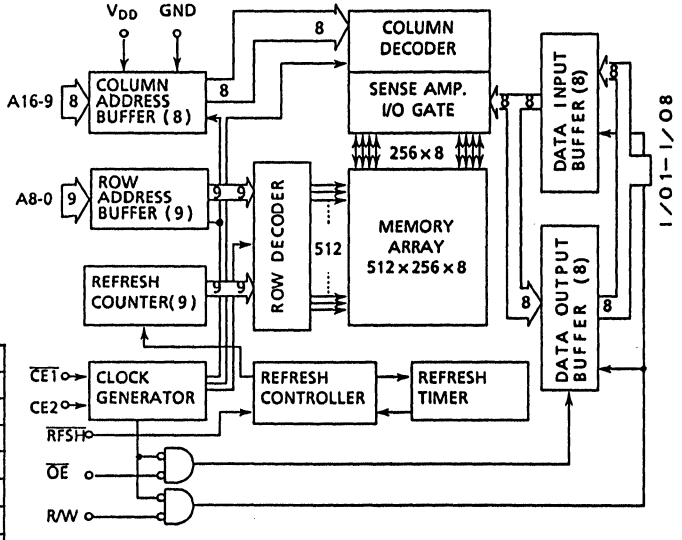
(TOP VIEW)



PIN NAMES

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



FUNCTION LOGIC

$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8	CONDITION
L	H	L	H	H	V*	OUT	Read
L	H	*	L	H	V*	IN	Write
L	H	H	H	H	V*	HZ	CE only Refresh
H	*	*	*	L	*	HZ	Auto/Self Refresh
*	L	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by
*	L	*	*	H	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ −1.0V)
* ··· Don't care (6.5V ~ −1.0V)
V* ··· At $\overline{CE1}$ falling edge (CE2 = H) or CE2 rising edge ($\overline{CE1}$ = L), all address inputs are "IN", and at the other condition, the address input are "*"
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	− 1.0~7.0	V	1
V_{OUT}	Output Voltage	− 1.0~7.0	V	
V_{DD}	Power Supply Voltage	− 1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	− 55~150	°C	
T_{SOLDER}	Soldering Temperature Time	260 · 10	°C · sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	
V_{IL}	Input Low Voltage	− 1.0	−	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER	PERIOD	MIN.	TYP.	MAX.	UNITS	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE1}$, CE2, Address cycling: t_{RC} = t_{RC} min.	130ns	–	50	70	mA	3, 4
		160ns	–	40	60		
		190ns	–	35	50		
I_{DDS1}	Standby Current, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} $\overline{RFSH}$ = V_{IH}		–	–	1	mA	
*I_{DDS2}	Standby Current, $\overline{CE1}$ = V_{DD} – 0.2V or CE2 = 0.2V $\overline{RFSH}$ = V_{DD} – 0.2V		–	100	200	µA	
I_{DDF1}	Self Refresh Current, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} $\overline{RFSH}$ = V_{IL}		–	–	1	mA	
*I_{DDF2}	Self Refresh Current, $\overline{CE1}$ = V_{DD} – 0.2V or CE2 = 0.2V $\overline{RFSH}$ = 0.2V		–	100	200	µA	
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ V_{DD}, All other Inputs not under test = 0V		– 10	–	10	µA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or R/W = V_{IL}), 0V ≤ V_{OUT} ≤ V_{DD}		– 10	–	10	µA	
V_{OH}	Output High Level (I_{OH} = – 5mA)		2.4	–	–	V	
V_{OL}	Output Low Level (I_{OL} = 4.2mA)		–	–	0.4	V	

Note*) In standby mode and self refresh with $\overline{CE1}$ ≧ V_{DD} – 0.2V, these specification limits are guaranteed under the condition of CE2 ≧ V_{DD} – 0.2V, or CE2 ≦ 0.2V.

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25 °C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE1}$, CE2, $\overline{OE}$, R/W, $\overline{RFSH}$)	–	7	pF
C_{IO}	Input / Output Capacitance	–	7	pF

Note) This parameter is periodically sampled and is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

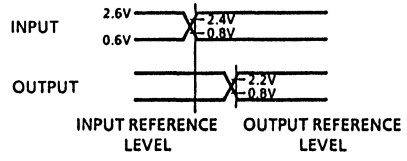
(V_{DD} = 5V ± 10%, Ta = 0~70 °C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	-	160	-	190	-	ns	
t_{RMW}	Read Modify Write Cycle Time	195	-	235	-	280	-	ns	
t_{CE}	CE Pulse Width	80	10,000	100	10,000	120	10,000	ns	13
t_P	CE Precharge Time	40	-	50	-	60	-	ns	
t_{CEA}	CE Access Time	-	80	-	100	-	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
t_{CLZ}	CE to Output in Low-Z	30	-	30	-	30	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{WLZ}	Output Active from End of Write	0	-	0	-	0	-	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	-	0	-	0	-	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	-	10	-	10	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	
t_{WP}	Write Pulse Width	60	-	70	-	85	-	ns	
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000	ns	
t_{CWL}	Write Command to CE Lead Time	60	10,000	70	10,000	85	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	30	-	35	-	45	-	ns	10
t_{DSC}	Data Set-Up Time from CE	30	-	35	-	45	-	ns	10
t_{DHW}	Data Hold Time from R/W	0	-	0	-	0	-	ns	10
t_{DHC}	Data Hold Time from CE	0	-	0	-	0	-	ns	10
t_{ASC}	Address Set-Up Time	0	-	0	-	0	-	ns	11
t_{AHC}	Address Hold Time	20	-	25	-	30	-	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	-	15	-	15	-	ns	
t_{FC}	Auto Refresh Cycle Time	130	-	160	-	190	-	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from CE	40	-	50	-	60	-	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	-	8,000	-	8,000	-	ns	12
t_{FRS}	CE Delay Time from $\overline{RFSH}$ (Self Refresh)	160	-	190	-	225	-	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	-	8	-	8	-	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

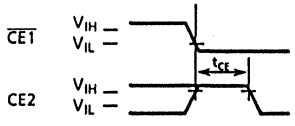
NOTES:

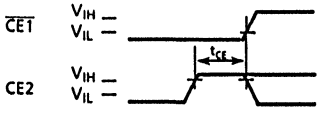
1) Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO} depends on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100μs with high $\overline{CE1}$ or low CE2 is required after power-up, before proper device operation is achieved.
6) AC measurements assume $t_T = 5ns$.
7) Timing reference level

Input Level	:	V_{IH} = 2.6V
		V_{IL} = 0.6V
Input Reference Level	:	V_{IH} = 2.4V
		V_{IL} = 0.8V
Output Reference Level	:	V_{OH} = 2.2V
		V_{OL} = 0.8V



8) Measured with a load equivalent to 2 TTL loads and 100pF.
9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE1}$ rising edge and CE2 falling edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched at the falling edge of $\overline{CE1}$ and the rising edge of CE2. Therefore the all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$.
    Auto refresh: $\overline{RFSH}$ pulse width $\leqq t_{FAP}$ (max.)
    Self refresh: $\overline{RFSH}$ pulse width $\geqq t_{FAS}$ (min.)
    The timing parameter (t_{FRS}) must be kept for proper device operation in the following conditions.
    - after self refresh
    - in case of "$\overline{RFSH}$" = "L" after power-up
13) The timings, t_{CE} (min.) and t_{CE} (max.), must be kept for proper device operation as follows.

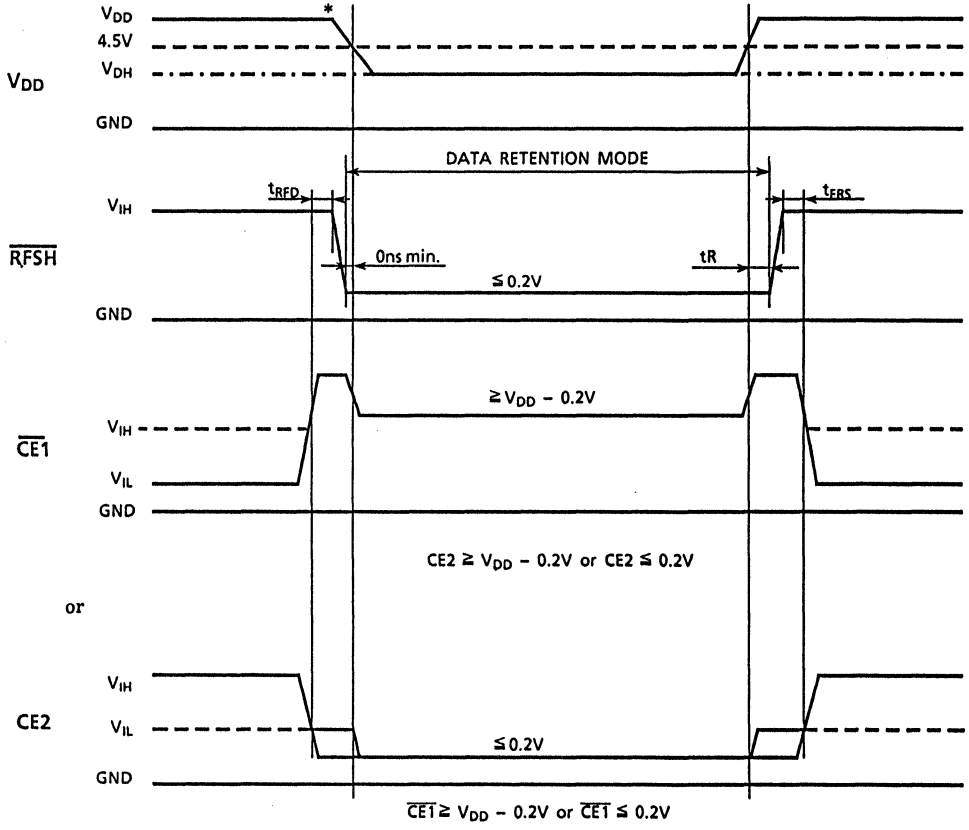




DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		3.0	-	5.5	V
I_{DDF2}	Self Refresh Current	V_{DH} = 3.0V	-	40	100	μA
		V_{DH} = 5.5V	-	100	200	μA
t_R	Recovery Time		5	-	-	mS

*The falling slope of V_{DD} must be more than 50ms in order to operate the device safely. (20ms/V)



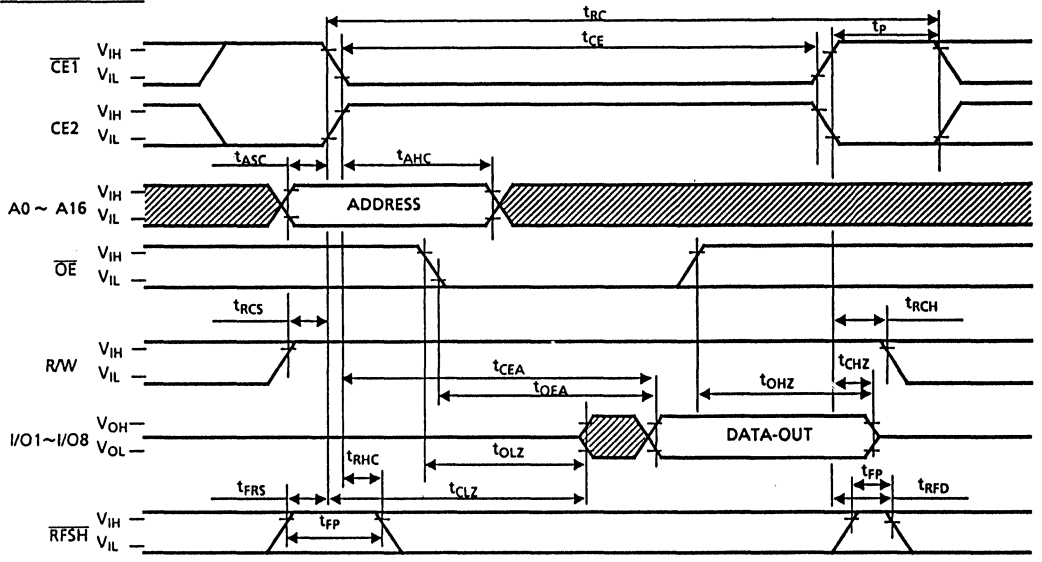
(Note)◦ $\overline{OE}$, R/W, A0~A16 = Don't care

◦ I_{DDF1} is applied in $\overline{RFSH} = V_{IL\ max.}$, $\overline{CE1} = V_{III\ min.}$, $CE2 = V_{IL\ max.}$

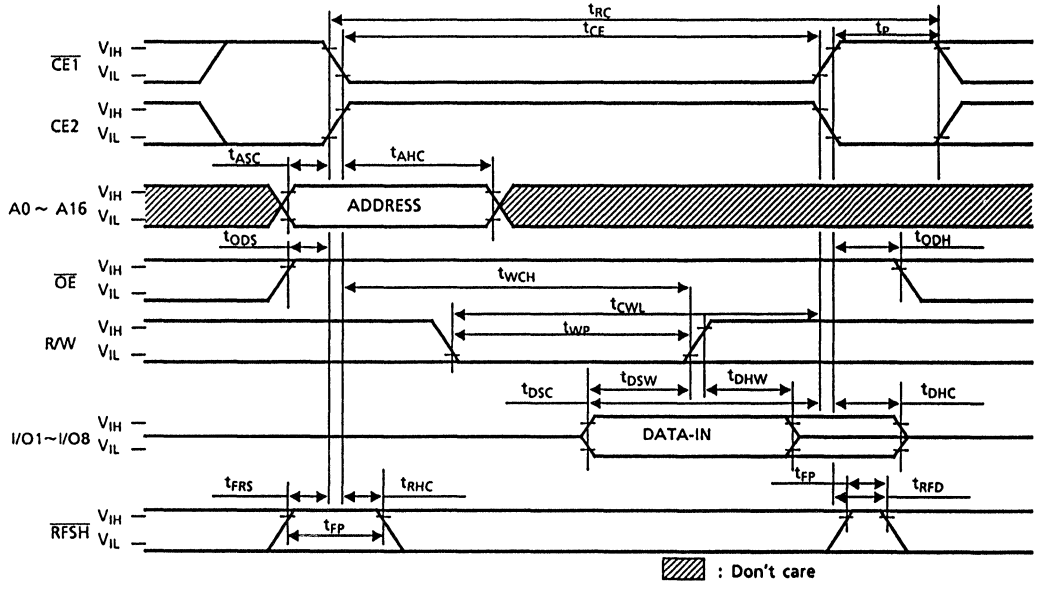
◦ At any state but Data Retention Mode, Auto Refresh or CE Only Refresh with 512cycle/8ms is required.

TIMING WAVEFORMS

READ CYCLE

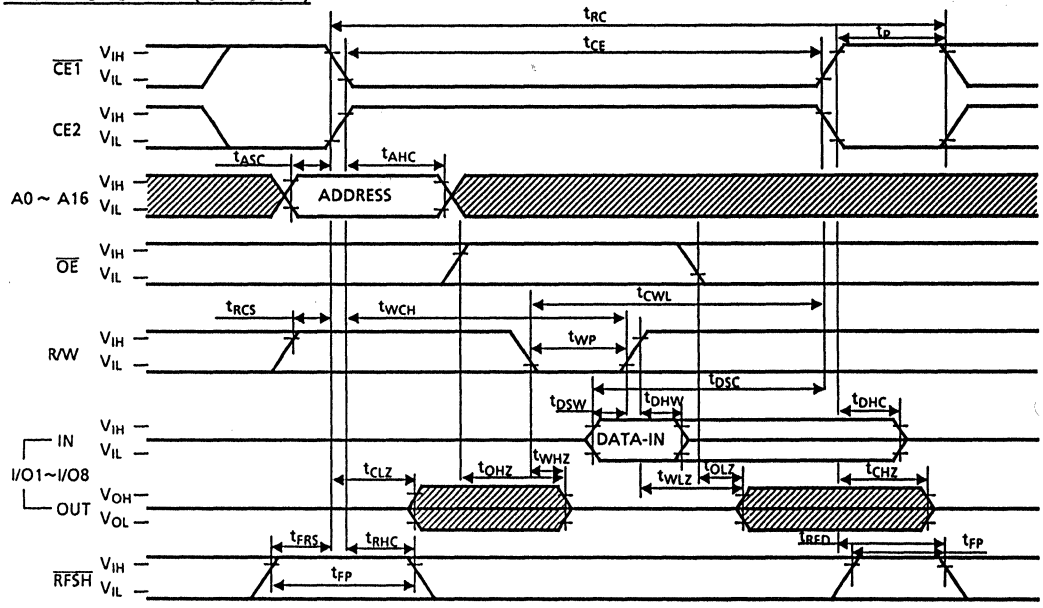


WRITE CYCLE-1 ($\overline{OE}$ Fix High)

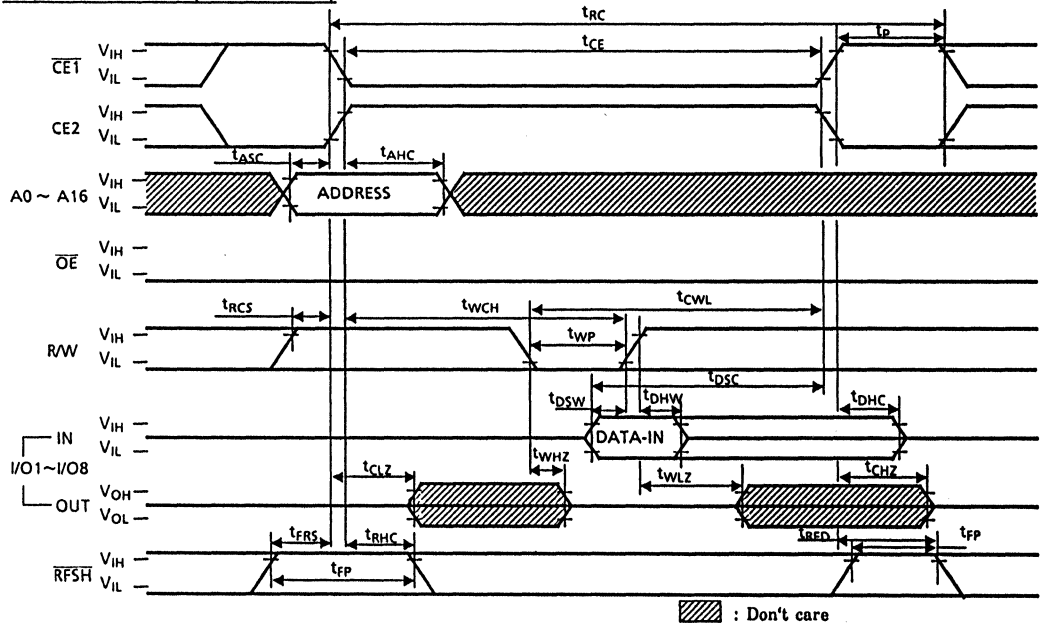


Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

WRITE CYCLE - 2 ($\overline{OE}$ Clock)

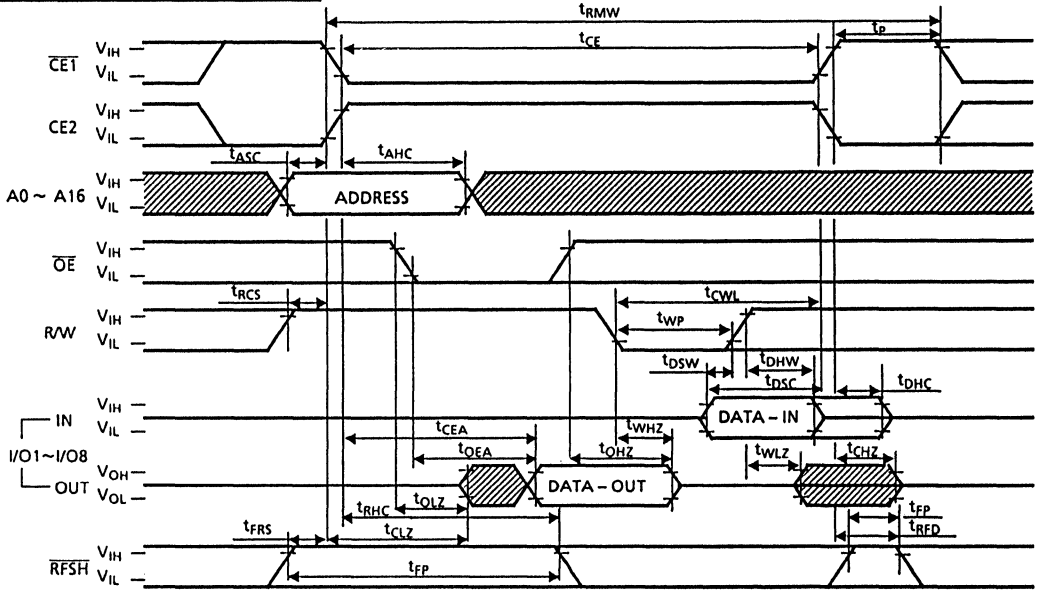


WRITE CYCLE - 3 ($\overline{OE}$ Fix Low)

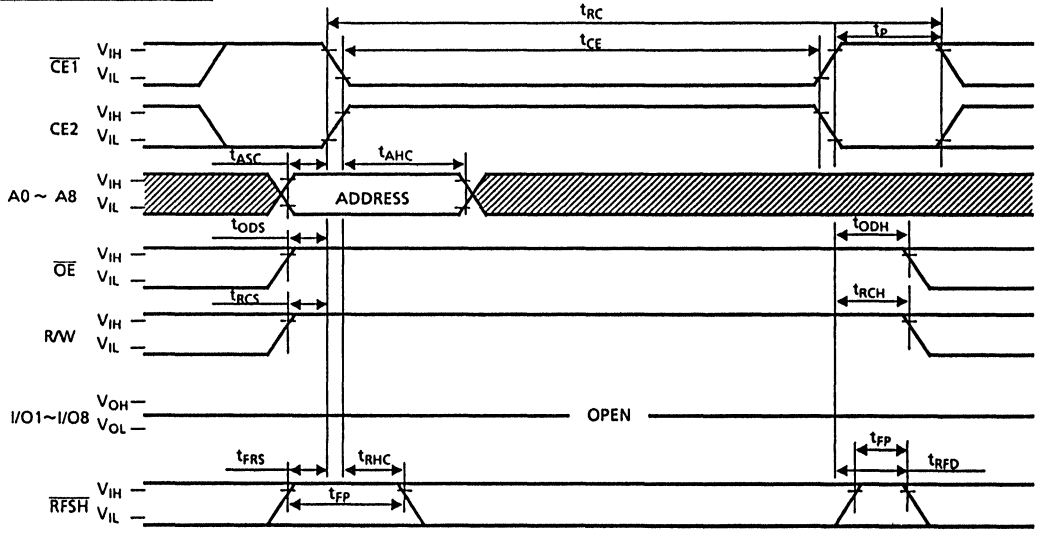


Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that " CE2 "(or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

READ MODIFY WRITE CYCLE



CE ONLY REFRESH

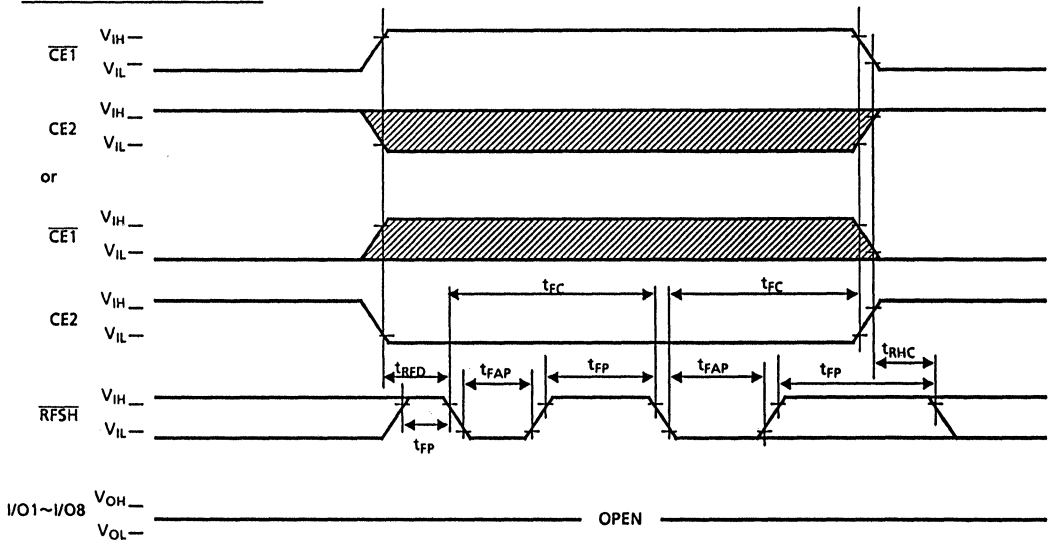


Note : A9~A16 = Don't care

▨: Don't care

Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

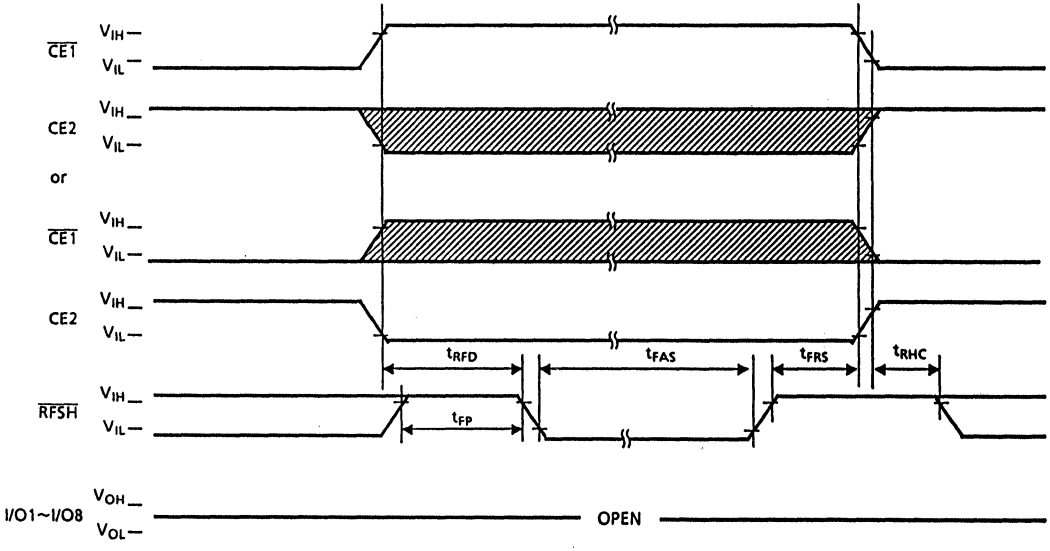
$\overline{RFSH}$ AUTO REFRESH



NOTE : $\overline{OE}$, R/W, A0~A16 = Don't care

: Don't care

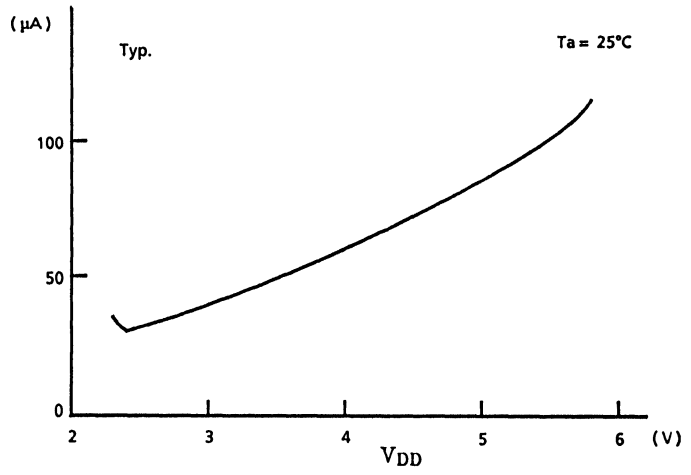
SELF REFRESH



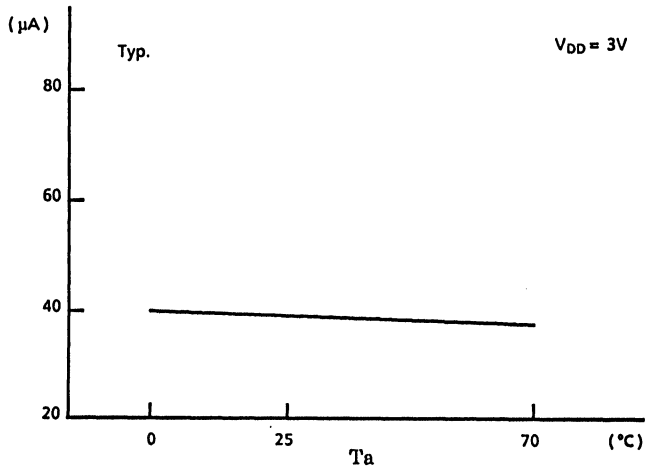
NOTE : $\overline{OE}$, R/W, A0~A16 = Don't care

: Don't care

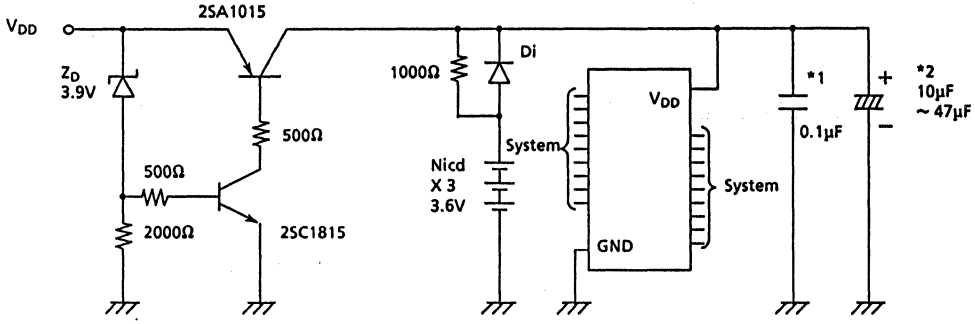
I_{DDF2} V_{DD} Characteristics



I_{DDF2} Temp. Characteristics



Battery Back Up applicable example



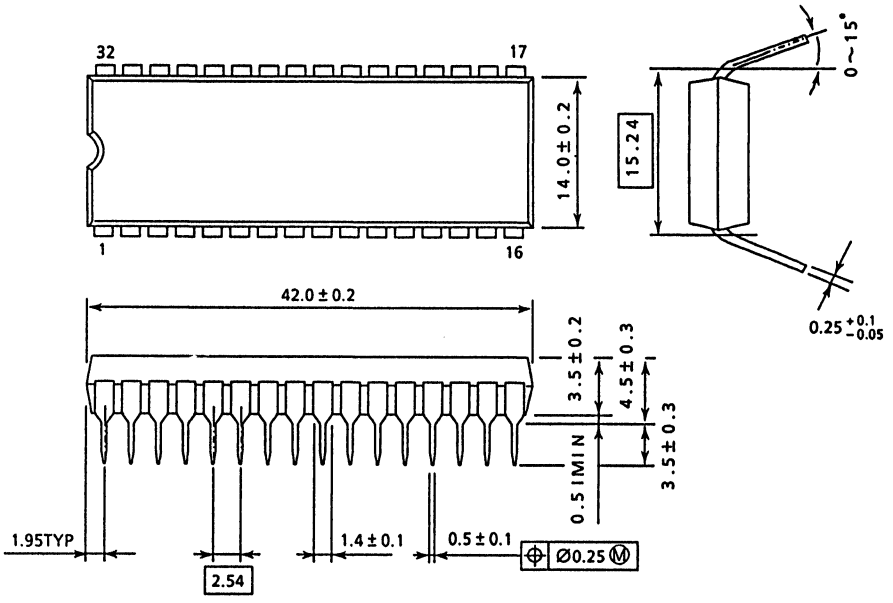
*1 : Ceramic condenser
*2 : Tantalum condenser
(The large Bypass condenser is preferable, as the noise is absorbed when the power supply is switched.)

This circuit does not have memory protection. Therefore, rapid turn-off of the power supply must be avoided. Enter the Self Refresh Mode before changing to Battery Back Up Power Supply.

OUTLINE DRAWINGS

(DIP32-P-600)

UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

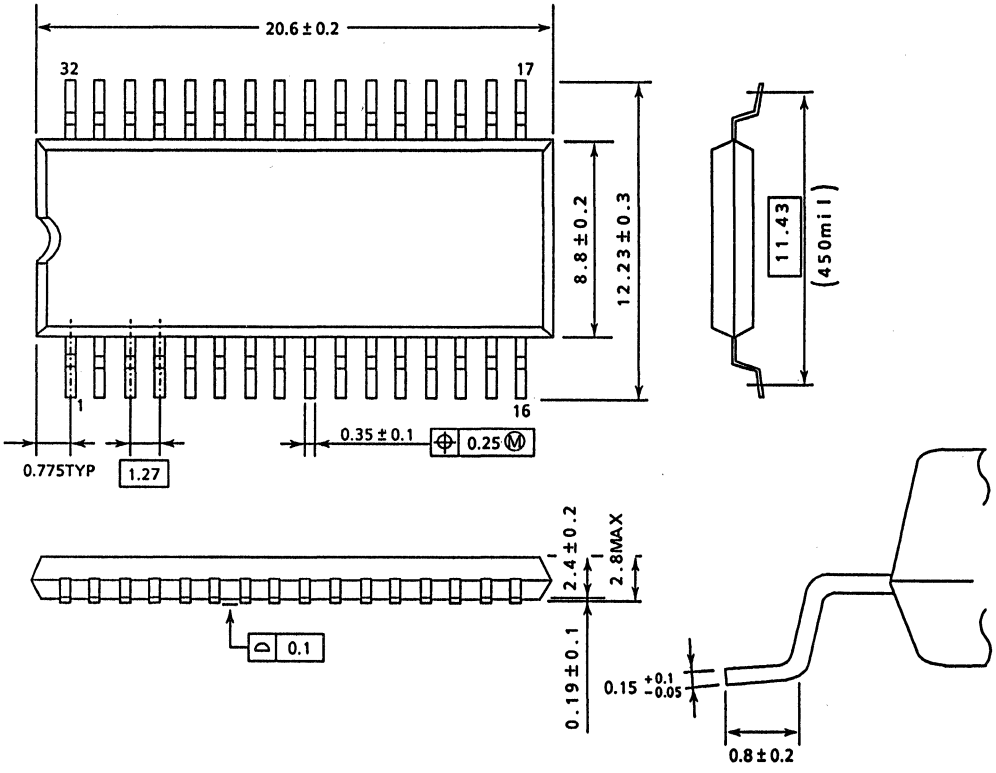
These outline drawings apply to:

TC518128APL-80LV
TC518128APL-10LV
TC518128APL-12LV

OUTLINE DRAWINGS

(SOP32-P-450)

UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

These outline drawings apply to:

TC518128AFL-80LV
TC518128AFL-10LV
TC518128AFL-12LV

131,072 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC518128A Family is a 1M bit high-speed CMOS Pseudo-Static RAM organized as 131,072 words by 8 bits. The TC518128A Family utilizes one transistor dynamic memory cell array with CMOS peripheral circuitry to achieve large capacity, high speed accesses, and low power requirements, using a single 5V power supply. The $\overline{RFSH}$ input allows two types of refresh operations: Auto Refresh and Self Refresh. The TC518128A Family has a static RAM-like read/write functionality, which allows easy interfacing to a microprocessor. The TC518128A Family is pin-compatable with the 1M bit static RAM. The TC518128AFWL is offered in a standard 28 pin 0.525 inch width small out-line plastic flat package.

FEATURES

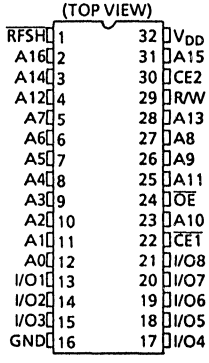
- Organization: 1M bit (131,072 word × 8bit)
- Fast Access Time and Low Power Dissipation

	TC518128AFW Family		
	-85	-10	-12
t_{CEA} $\overline{CE}$ Access Time	80ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	1mA/200μA (-L)		

- Single Power Supply: 5V±10%
- Auto refresh uses an internal counter.
- Self refresh uses an internal timer.
- All inputs and outputs : TTL compatible
- 512 refresh cycle / 8ms
- Pin Compatible: 1M SRAM (JEDEC)
- Logic Compatible: SRAM R/W Pin
- 32 Pin Standard Plastic PKG
  525 mil SOP

PIN CONNECTION

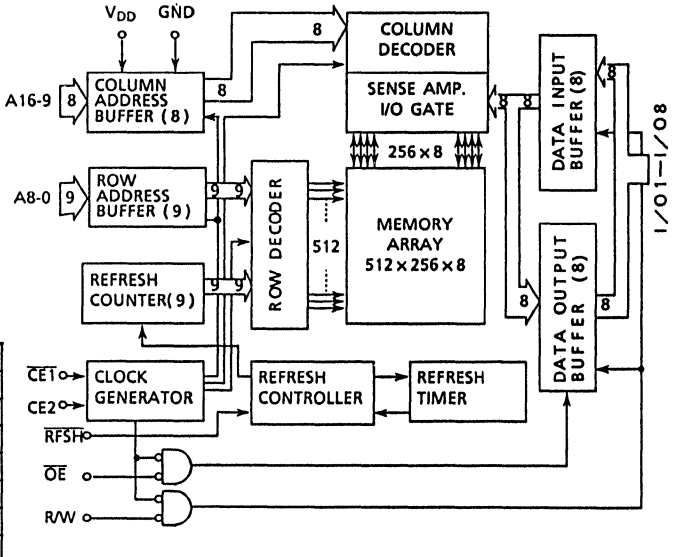
(TOP VIEW)



PIN NAMES

A0 ~ A16	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs / Outputs
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



FUNCTION LOGIC

$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8	CONDITION
L	H	L	H	H	V*	OUT	Read
L	H	*	L	H	V*	IN	Write
L	H	H	H	H	V*	HZ	CE only Refresh
H	*	*	*	L	*	HZ	Auto/Self Refresh
*	L	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by
*	L	*	*	H	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ −1.0V)
* ··· Don't care (6.5V ~ −1.0V)
V* ··· At $\overline{CE1}$ falling edge (CE2 = H) or CE2 rising edge ($\overline{CE1}$ = L), all address inputs are "IN", and at the other condition, the address input are "*".
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	−1.0~7.0	V	1
V_{OUT}	Output Voltage	−1.0~7.0	V	
V_{DD}	Power Supply Voltage	−1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	−55~150	°C	
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		PERIOD	MIN.	TYP.	MAX.	UNITS	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE1}$, CE2, Address cycling: $t_{RC} = t_{RC}$ min.		130ns	-	50	70	mA	3, 4
			160ns	-	40	60		
			190ns	-	35	50		
I_{DDS1}	Standby Current $\overline{CE1} = V_{IH}$ or CE2 = V_{IL} $\overline{RFSH} = V_{IH}$	TC518128AFW		-	-	2	mA	
		TC518128AFWL		-	-	1		
*I_{DDS2}	Standby Current $\overline{CE1} = V_{DD} - 0.2V$ or CE2 = 0.2V, $\overline{RFSH} = V_{DD} - 0.2V$	TC518128AFW		-	-	1	mA	
		TC518128AFWL		-	100	200	µA	
I_{DDF1}	Self Refresh Current $\overline{CE1} = V_{IH}$ or CE2 = V_{IL}, $\overline{RFSH} = V_{IL}$	TC518128AFW		-	-	2	mA	
		TC518128AFWL		-	-	1		
*I_{DDF2}	Self Refresh Current $\overline{CE1} = V_{DD} - 0.2V$ or CE2 = 0.2V, $\overline{RFSH}$ = 0.2V	TC518128AFW		-	-	1	mA	
		TC518128AFWL		-	100	200	µA	
$I_{I(L)}$	Input Leakage Current 0V ≦ V_{IN} ≦ V_{DD}, All other Inputs not under test = 0V			- 10	-	10	µA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE1} = V_{IH}$ or CE2 = V_{IL} or $\overline{OE} = V_{IH}$ or R/W = V_{IL}), 0V ≦ V_{OUT} ≦ V_{DD}			- 10	-	10	µA	
V_{OH}	Output High Level I_{OH} = - 5mA			2.4	-	-	V	
V_{OL}	Output Low Level I_{OL} = 4.2mA			-	-	0.4	V	

Note*) In standby mode and self refresh with $\overline{CE1} \geqq V_{DD} - 0.2V$, these specification limits are guaranteed under the condition of CE2 ≧ V_{DD} − 0.2V, or CE2 ≦ 0.2V.

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25 °C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	-	5	pF
C_{I2}	Input Capacitance ($\overline{CE1}$, CE2, $\overline{OE}$, R/W, $\overline{RFSH}$)	-	7	pF
C_{IO}	Input / Output Capacitance	-	7	pF

Note) This parameter is periodically sampled and is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{DD} = 5V ± 10%, Ta = 0~70 °C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	–	160	–	190	–	ns	
t_{RMW}	Read Modify Write Cycle Time	195	–	235	–	280	–	ns	
t_{CE}	CE Pulse Width	80	10,000	100	10,000	120	10,000	ns	13
t_P	CE Precharge Time	40	–	50	–	60	–	ns	
t_{CEA}	CE Access Time	–	80	–	100	–	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	35	–	40	–	50	ns	
t_{CLZ}	CE to Output in Low-Z	30	–	30	–	30	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	0	–	ns	
t_{WLZ}	Output Active from End of Write	0	–	0	–	0	–	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	–	0	–	0	–	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	–	10	–	10	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	
t_{WP}	Write Pulse Width	60	–	70	–	85	–	ns	
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000	ns	
t_{CWL}	Write Command to CE Lead Time	60	10,000	70	10,000	85	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	30	–	35	–	45	–	ns	10
t_{DSC}	Data Set-Up Time from CE	30	–	35	–	45	–	ns	10
t_{DHW}	Data Hold Time from R/W	0	–	0	–	0	–	ns	10
t_{DHC}	Data Hold Time from CE	0	–	0	–	0	–	ns	10
t_{ASC}	Address Set-Up Time	0	–	0	–	0	–	ns	11
t_{AHC}	Address Hold Time	20	–	25	–	30	–	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	–	15	–	15	–	ns	
t_{FC}	Auto Refresh Cycle Time	130	–	160	–	190	–	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from CE	40	–	50	–	60	–	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–	ns	12
t_{FRS}	CE Delay Time from $\overline{RFSH}$ (Self Refresh)	160	–	190	–	225	–	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	–	8	–	8	–	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

NOTES:

1) Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

2) All voltage are referenced to GND.

3) I_{DDO} depends on cycle rate.

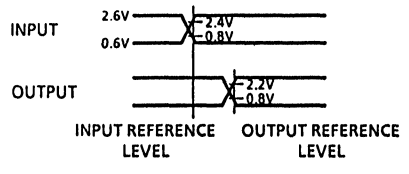
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.

5) An initial pause of 100μs with high $\overline{CE1}$ or low CE2 is required after power-up, before proper device operation is achieved.

6) AC measurements asuume t_T = 5ns.

7) Timing reference level

Input Level	:	V_{IH} = 2.6V
		V_{IL} = 0.6V
Input Reference Level	:	V_{IH} = 2.4V
		V_{IL} = 0.8V
Output Reference Level	:	V_{OH} = 2.2V
		V_{OL} = 0.8V



8) Measured with a load equivalent to 2 TTL loads and 100pF.

9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE1}$ rising edge and CE2 falling edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).

11) All address inputs are latched at the falling edge of $\overline{CE1}$ and the rising edge of CE2. Therefore all address inputs must be valid during t_{ASC} and t_{AHC}.

12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}.

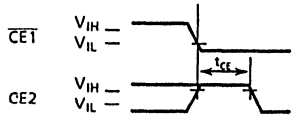
Auto refresh : $\overline{RFSH}$ pulse width $\leqq$ t_{FAP} (max.)

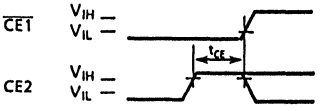
Self refresh : $\overline{RFSH}$ pulse width $\geqq$ t_{FAS} (min.)

The timing parameter (t_{FRS}) must be kept for proper device operation in the following conditions.

- after self refresh
- in case of "$\overline{RFSH}$" = "L" after power-up

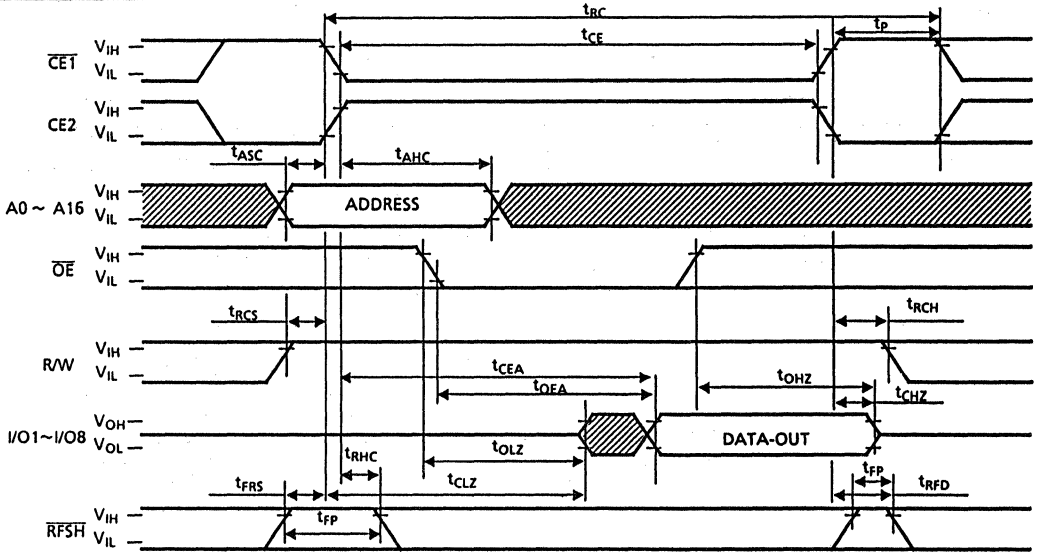
13) The timings, t_{CE} (min.) and t_{CE} (max.), must be kept for proper device operation as follows.



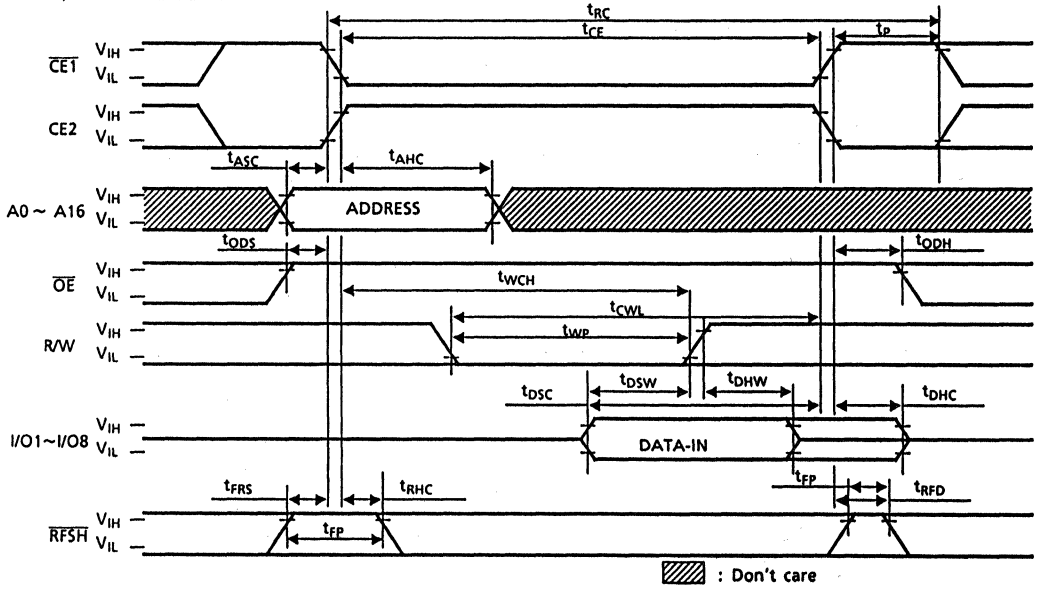


TIMING WAVEFORMS

READ CYCLE

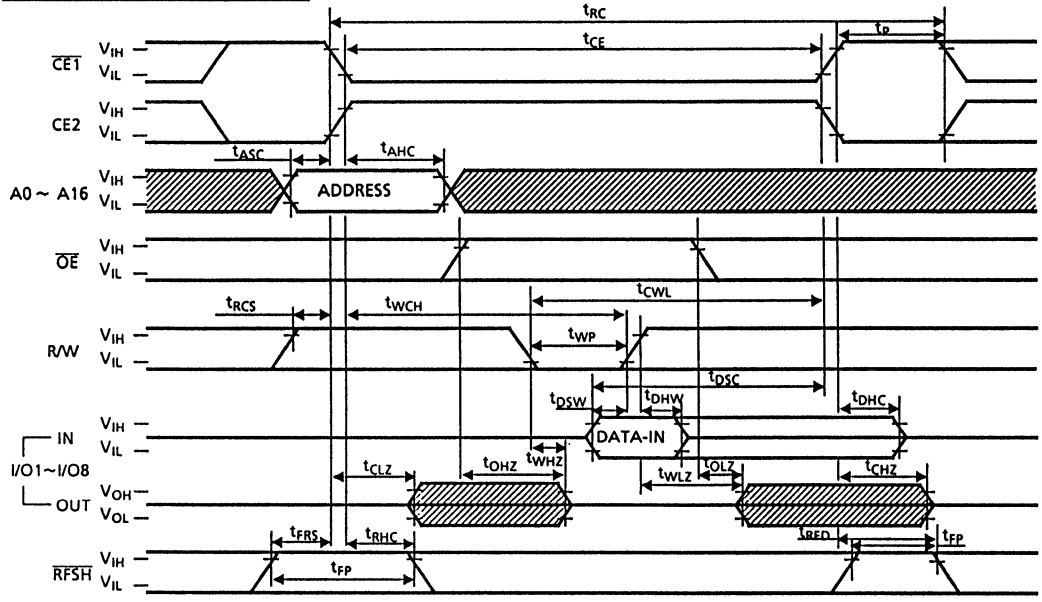


WRITE CYCLE-1 ($\overline{OE}$ Fix High)

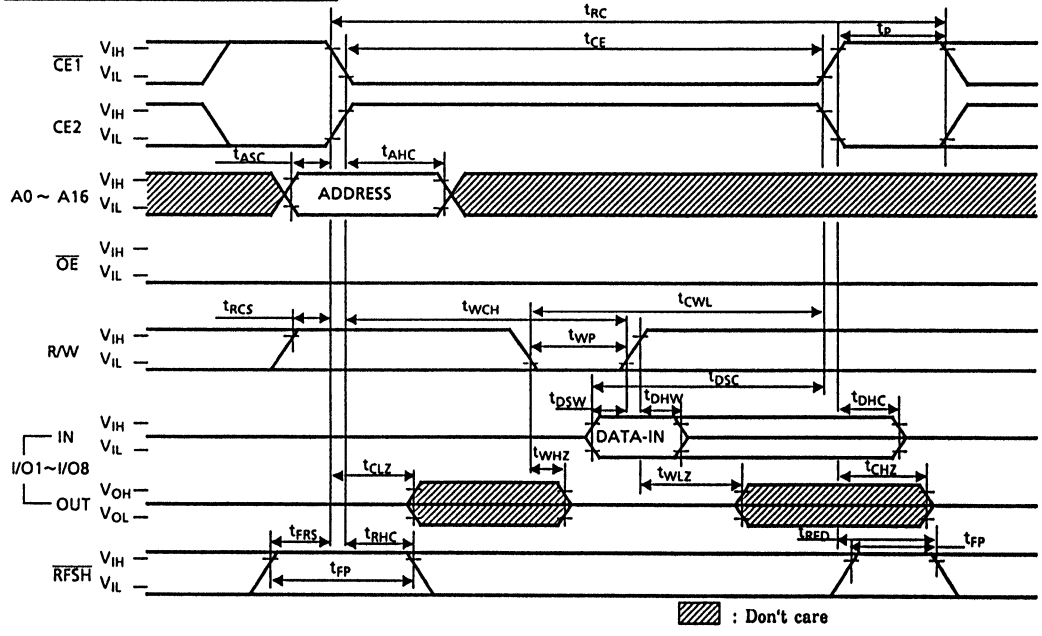


Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

WRITE CYCLE - 2 ($\overline{OE}$ Clock)

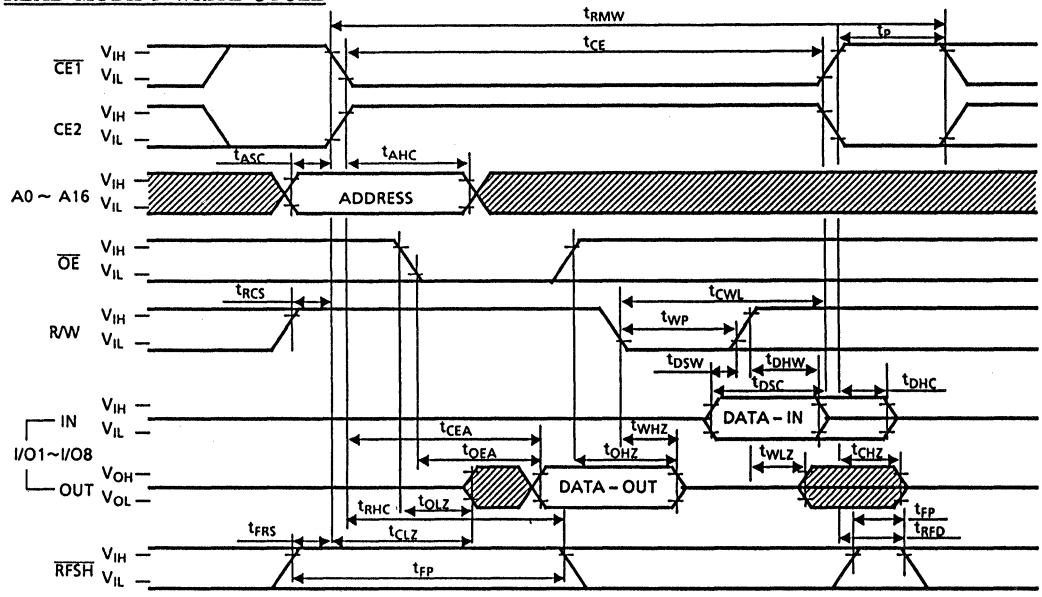


WRITE CYCLE - 3 ($\overline{OE}$ Fix Low)

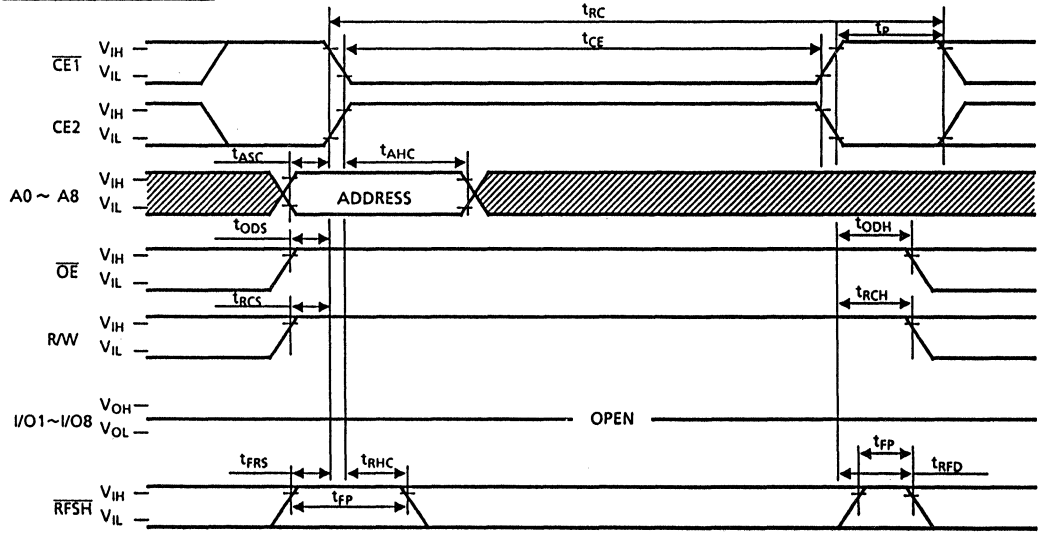


Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

READ MODIFY WRITE CYCLE



CE ONLY REFRESH

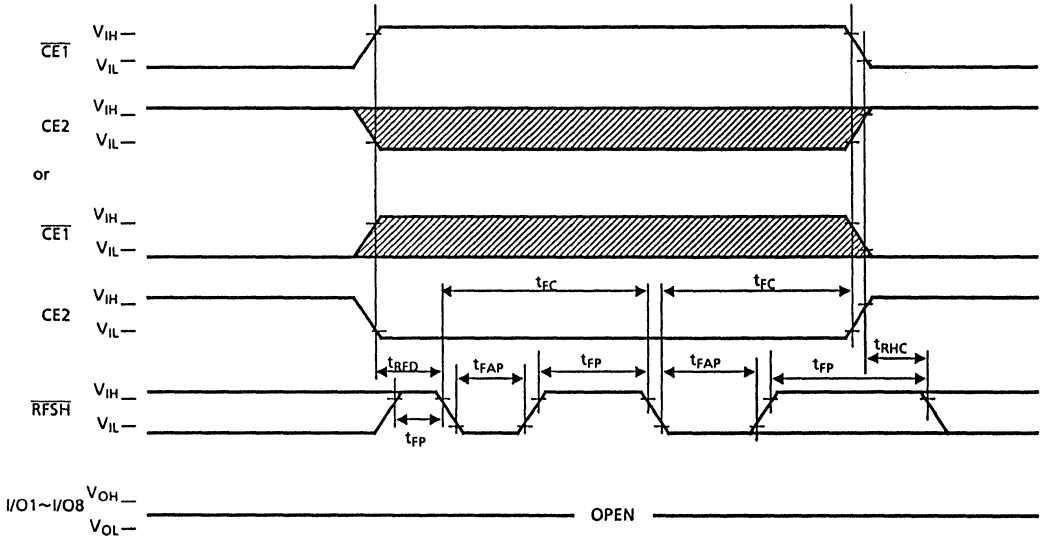


Note.: A9 ~ A16 = Don't care

▨: Don't care

Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

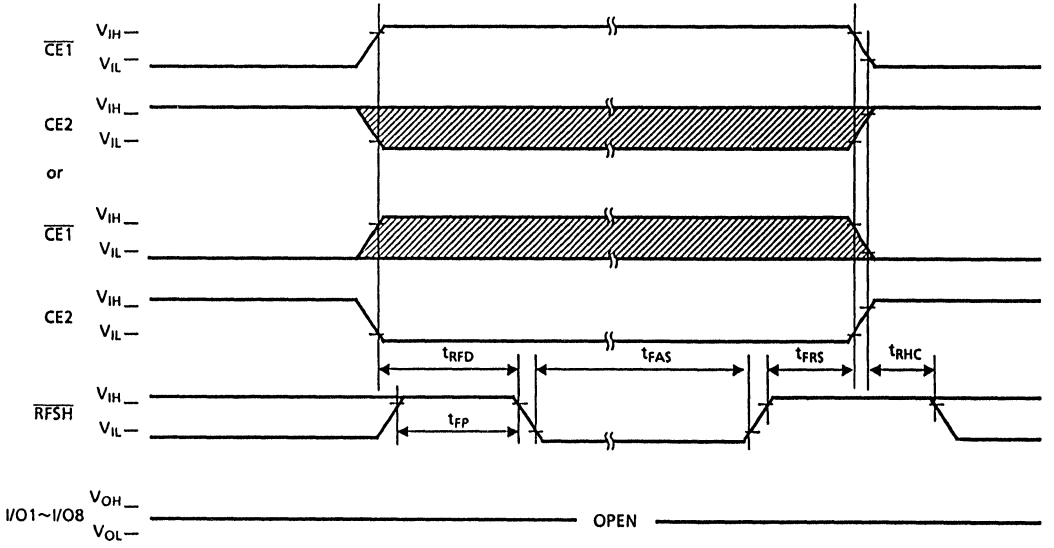
$\overline{RFSH}$ AUTO REFRESH



NOTE : $\overline{OE}$, R/W, A0~A16 = Don't care

▨: Don't care

SELF REFRESH



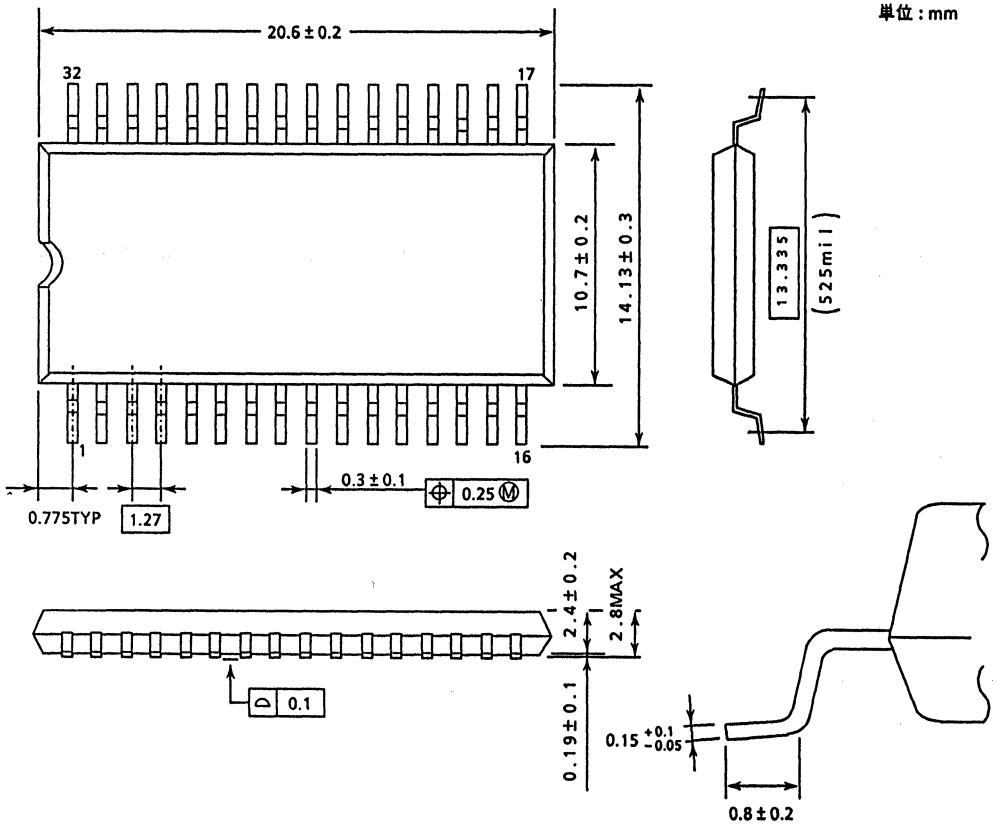
NOTE : $\overline{OE}$, R/W, A0~A16 = Don't care

▨: Don't care

OUTLINE DRAWINGS

(SOP32-P-525)

単位 : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

131,072 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC518128A-LV Family is a 1M bit high-speed CMOS Pseudo-Static RAM organized as 131,072 words by 8 bits. The TC518128A-LV Family utilizes one transistor dynamic memory cell array with CMOS peripheral circuitry to achieve large capacity, high speed accesses, and low power requirements, using a single 5V power supply. The TC518128A-LV Family offers 3V data retention capability for battery back-up applications. The $\overline{RFSH}$ input allows two types of refresh operations: Auto Refresh and Self Refresh. The TC518128A-LV Family has a static RAM-like read/write functionality, which allows easy interfacing to a microprocessor. The TC518128AFWL-LV Family is pin-compatable with the 1M bit static RAM. The TC518128AFWL-LV is offered in a standard 28 pin 0.525 inch width small out-line plastic flat package.

FEATURES

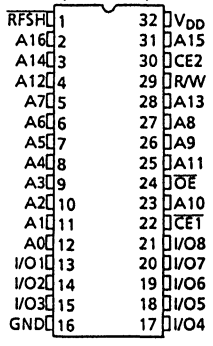
- Organization: 1M bit (131,072 word × 8bit)
- Fast Access Time and Low Power Dissipation

		TC518128AFW Family		
		-80	-10	-12
t_{CEA} $\overline{CE}$ Access Time		80ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time		35ns	40ns	50ns
t_{RC} Cycle Time		130ns	160ns	190ns
Power Dissipation		385mW	330mW	275mW
Self Refresh Current	5.5V	200μA		
	3.0V	100μA		

- Single Power Supply: 5V±10%
- Data Retention Supply Voltage: 3.0V ~ 5.5V
- Auto refresh uses an internal counter.
- Self refresh uses an internal timer.
- All inputs and outputs : TTL compatible
- 512 refresh cycle/8ms
- Pin Compatible: 1M SRAM (JEDEC)
- Logic Compatible: SRAM R/W Pin
- 32 Pin Standard Plastic 525 mil SOP

PIN CONNECTION

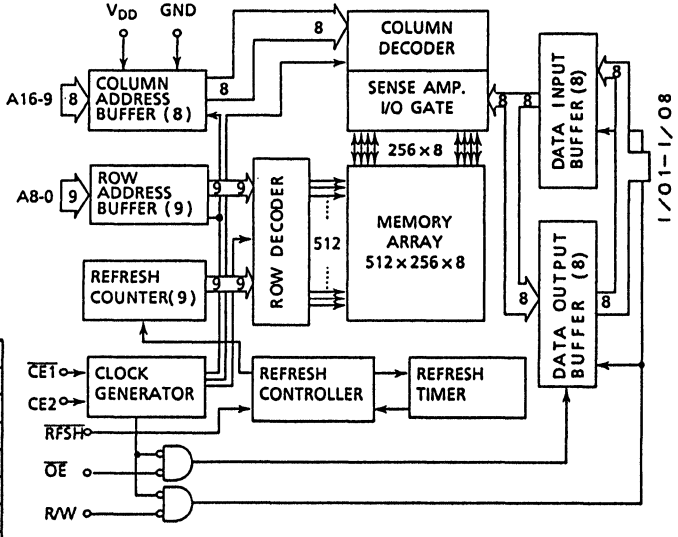
(TOP VIEW)



PIN NAMES

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



FUNCTION LOGIC

$\overline{CE1}$	CE2	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8	CONDITION
L	H	L	H	H	V*	OUT	Read
L	H	*	L	H	V*	IN	Write
L	H	H	H	H	V*	HZ	CE only Refresh
H	*	*	*	L	*	HZ	Auto/Self Refresh
*	L	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by
*	L	*	*	H	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ −1.0V)
* ··· Don't care (6.5V ~ −1.0V)
V* ··· At $\overline{CE1}$ falling edge (CE2 = H) or CE2 rising edge ($\overline{CE1}$ = L), all address inputs are "IN", and at the other condition, the address input are "*".
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	−1.0~7.0	V	1
V_{OUT}	Output Voltage	−1.0~7.0	V	
V_{DD}	Power Supply Voltage	−1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	−55~150	°C	
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER	PERIOD	MIN.	TYP.	MAX.	UNITS	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE1}$, CE2, Address cycling: t_{RC} = t_{RC} min.	130ns	-	50	70	mA	3, 4
		160ns	-	40	60		
		190ns	-	35	50		
I_{DDS1}	Standby Current, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} $\overline{RFSH}$ = V_{IH}		-	-	1	mA	
*I_{DDS2}	Standby Current, $\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V $\overline{RFSH}$ = V_{DD} - 0.2V		-	100	200	μA	
I_{DDF1}	Self Refresh Current, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} $\overline{RFSH}$ = V_{IL}		-	-	1	mA	
*I_{DDF2}	Self Refresh Current, $\overline{CE1}$ = V_{DD} - 0.2V or CE2 = 0.2V $\overline{RFSH}$ = 0.2V		-	100	200	μA	
$I_{I(L)}$	Input Leakage Current 0V ≦ V_{IN} ≦ V_{DD}, All other Inputs not under test = 0V		- 10	-	10	μA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or R/W = V_{IL}), 0V ≦ V_{OUT} ≦ V_{DD}		- 10	-	10	μA	
V_{OH}	Output High Level (I_{OH} = - 5mA)		2.4	-	-	V	
V_{OL}	Output Low Level (I_{OL} = 4.2mA)		-	-	0.4	V	

Note*) In standby mode and self refresh with $\overline{CE1}$ ≧ V_{DD} - 0.2V, these specification limits are guaranteed under the condition of CE2 ≧ V_{DD} - 0.2V, or CE2 ≦ 0.2V.

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	-	5	pF
C_{I2}	Input Capacitance ($\overline{CE1}$, CE2, $\overline{OE}$, R/W, $\overline{RFSH}$)	-	7	pF
C_{IO}	Input/Output Capacitance	-	7	pF

Note) This parameter is periodically sampled and is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

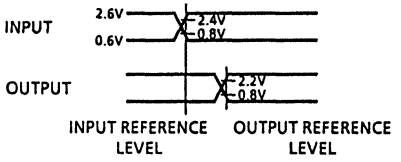
(V_{DD} = 5V ± 10%, Ta = 0~70 °C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	-	160	-	190	-	ns	
t_{RMW}	Read Modify Write Cycle Time	195	-	235	-	280	-	ns	
t_{CE}	CE Pulse Width	80	10,000	100	10,000	120	10,000	ns	13
t_P	CE Precharge Time	40	-	50	-	60	-	ns	
t_{CEA}	CE Access Time	-	80	-	100	-	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
t_{CLZ}	CE to Output in Low-Z	30	-	30	-	30	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{WLZ}	Output Active from End of Write	0	-	0	-	0	-	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	-	0	-	0	-	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	-	10	-	10	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	
t_{WP}	Write Pulse Width	60	-	70	-	85	-	ns	
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000	ns	
t_{CWL}	Write Command to CE Lead Time	60	10,000	70	10,000	85	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	30	-	35	-	45	-	ns	10
t_{DSC}	Data Set-Up Time from CE	30	-	35	-	45	-	ns	10
t_{DHW}	Data Hold Time from R/W	0	-	0	-	0	-	ns	10
t_{DHC}	Data Hold Time from CE	0	-	0	-	0	-	ns	10
t_{ASC}	Address Set-Up Time	0	-	0	-	0	-	ns	11
t_{AHC}	Address Hold Time	20	-	25	-	30	-	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	-	15	-	15	-	ns	
t_{FC}	Auto Refresh Cycle Time	130	-	160	-	190	-	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from CE	40	-	50	-	60	-	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	-	8,000	-	8,000	-	ns	12
t_{FRS}	CE Delay Time from $\overline{RFSH}$ (Self Refresh)	160	-	190	-	225	-	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	-	8	-	8	-	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

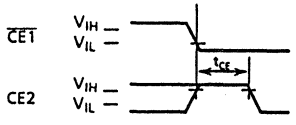
NOTES:

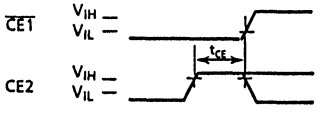
1) Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO} depends on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100μs with high $\overline{CE1}$ or low CE2 is required after power-up, before proper device operation is achieved.
6) AC measurements assume $t_T = 5ns$.
7) Timing reference level

Input Level	:	$V_{IH} = 2.6V$
		$V_{IL} = 0.6V$
Input Reference Level	:	$V_{IH} = 2.4V$
		$V_{IL} = 0.8V$
Output Reference Level	:	$V_{OH} = 2.2V$
		$V_{OL} = 0.8V$



8) Measured with a load equivalent to 2 TTL loads and 100pF.
9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE1}$ rising edge and CE2 falling edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched at the falling edge of $\overline{CE1}$ and the rising edge of CE2. Therefore all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$.
    Auto refresh: $\overline{RFSH}$ pulse width $\leqq t_{FAP}$ (max.)
    Self refresh : $\overline{RFSH}$ pulse width $\geqq t_{FAS}$ (min.)
    The timing parameter (t_{FRS}) must be kept for proper device operation in the following conditions.
    - after self refresh
    - in case of "$\overline{RFSH}$" = "L" after power-up
13) The timings, t_{CE} (min.) and T_{CE} (max.), must be kept for proper device operation as follows.

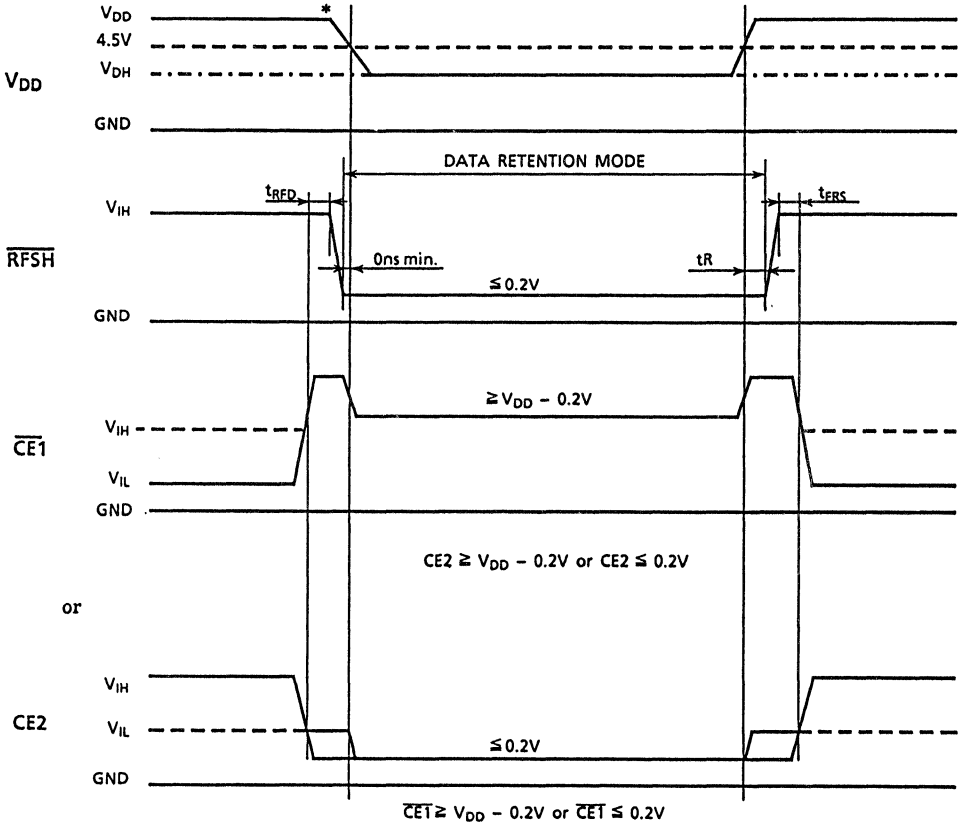




DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		3.0	-	5.5	V
I_{DDF2}	Self Refresh Current	V_{DH} = 3.0V	-	40	100	μA
		V_{DH} = 5.5V	-	100	200	μA
t_R	Recovery Time		5	-	-	mS

*The falling slope of V_{DD} must be more than 50ms in order to operate the device safely. (20ms/V)



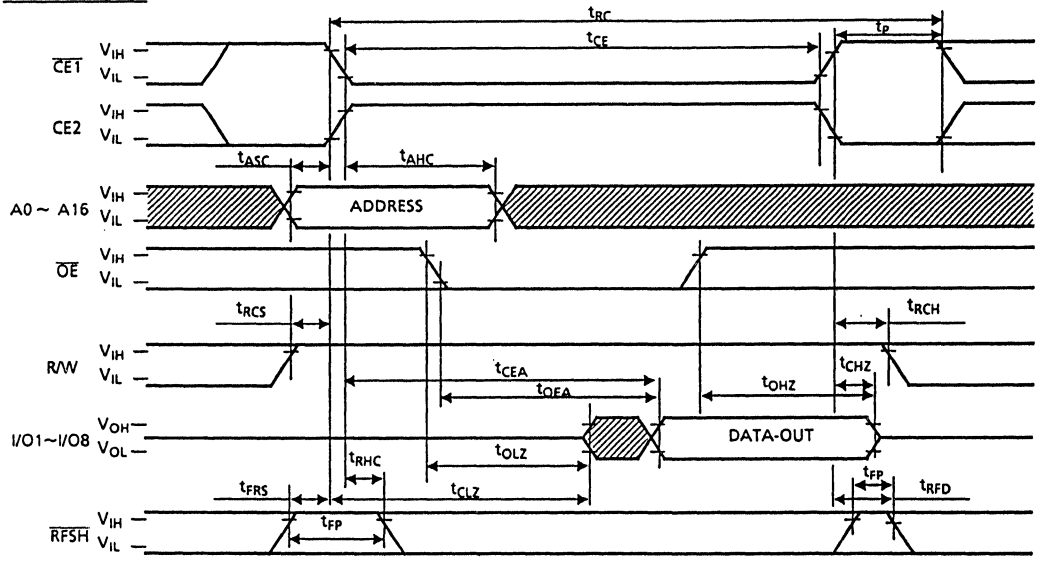
(Note) ∘ $\overline{OE}$, R/W, A0~A16 = Don't care

∘ I_{DDF1} is applied in $\overline{RFSH} = V_{IL\ max.}$, $\overline{CE1} = V_{IH\ min.}$, $CE2 = V_{IL\ max.}$

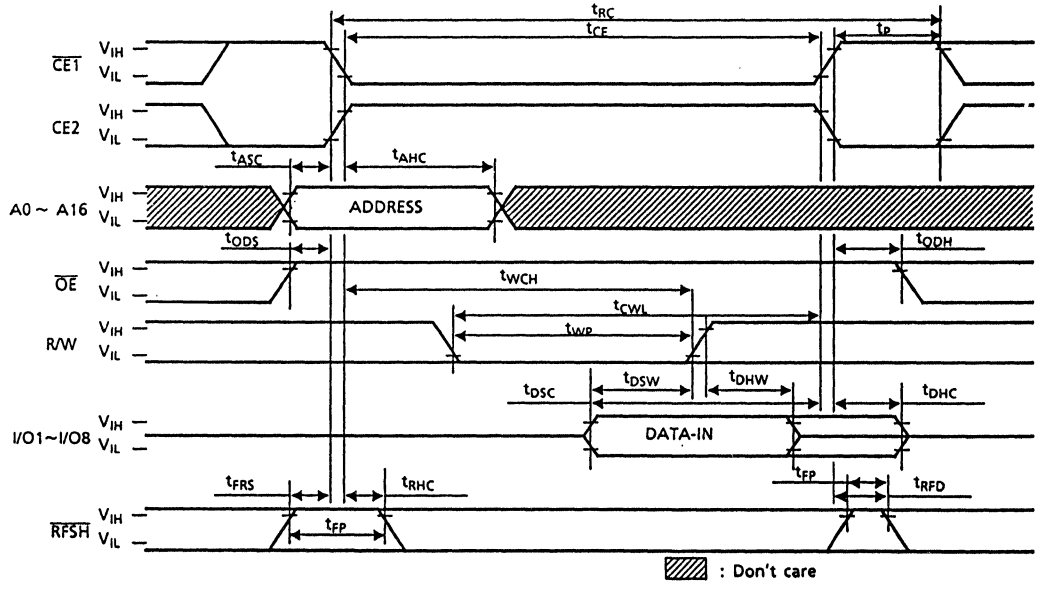
∘ At any state but Data Retention Mode, Auto Refresh or CE Only Refresh with 512cycle/8ms is required.

TIMING WAVEFORMS

READ CYCLE

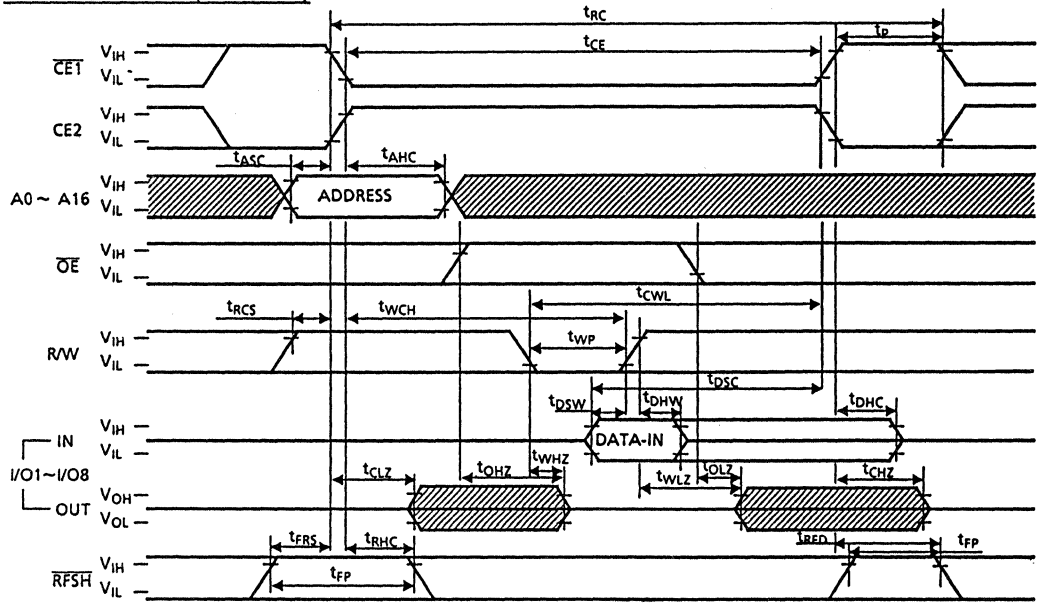


WRITE CYCLE-1 ($\overline{OE}$ Fix High)

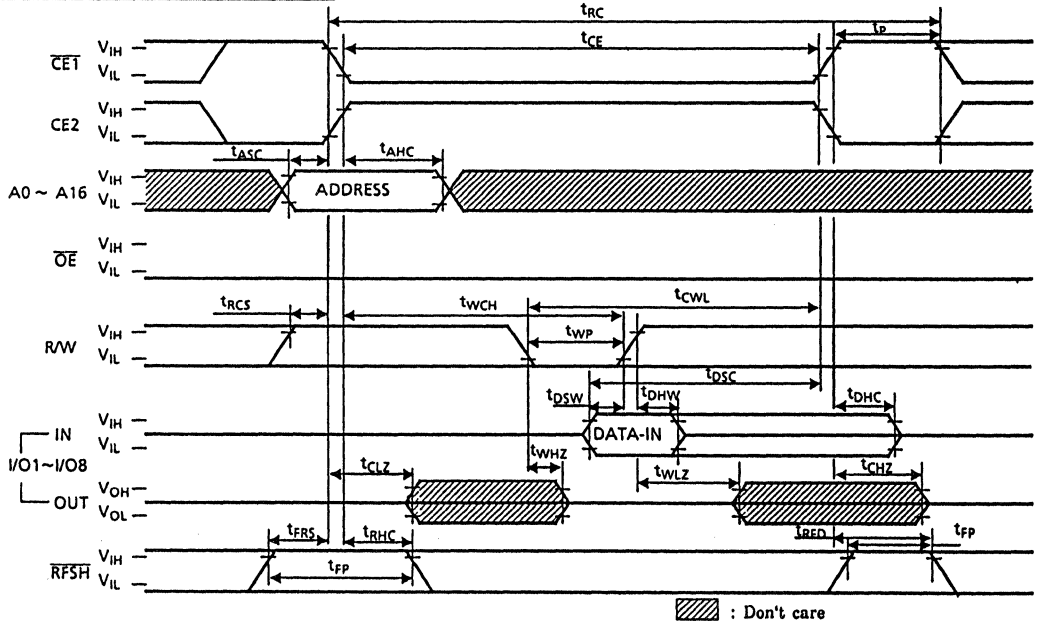


Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

WRITE CYCLE - 2 ($\overline{OE}$ Clock)

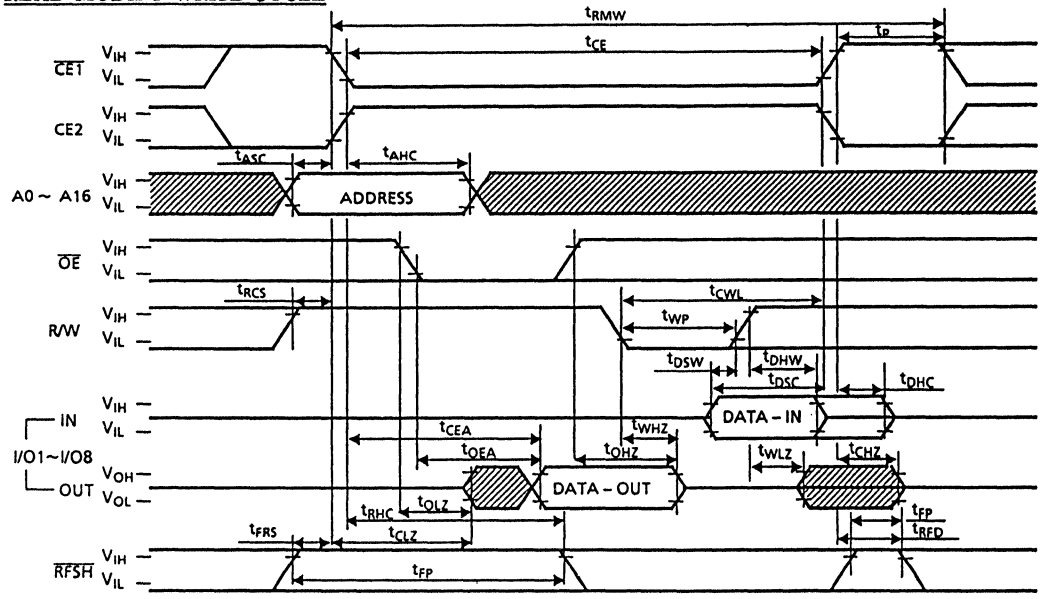


WRITE CYCLE - 3 ($\overline{OE}$ Fix Low)

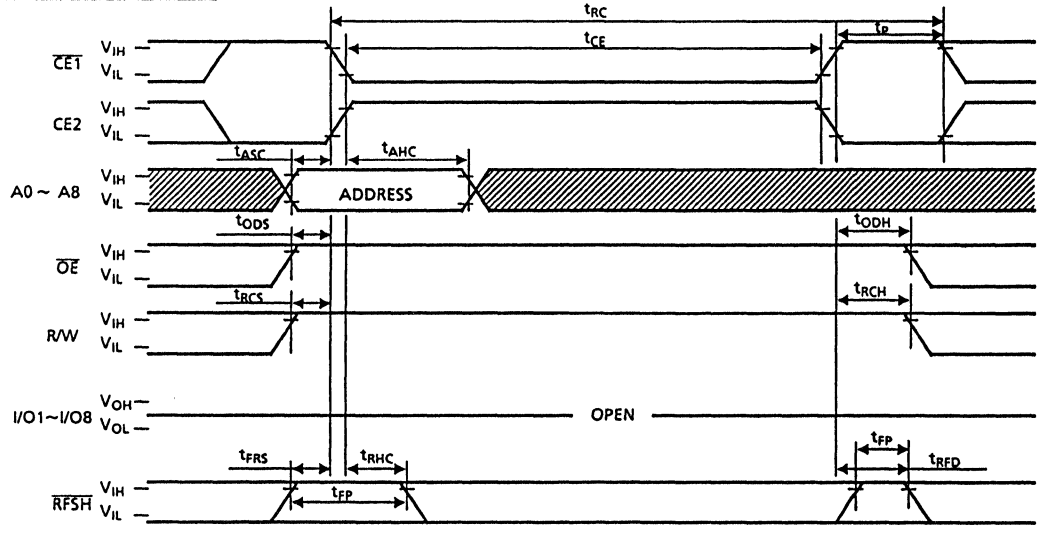


Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that " CE2 "(or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

READ MODIFY WRITE CYCLE



CE ONLY REFRESH

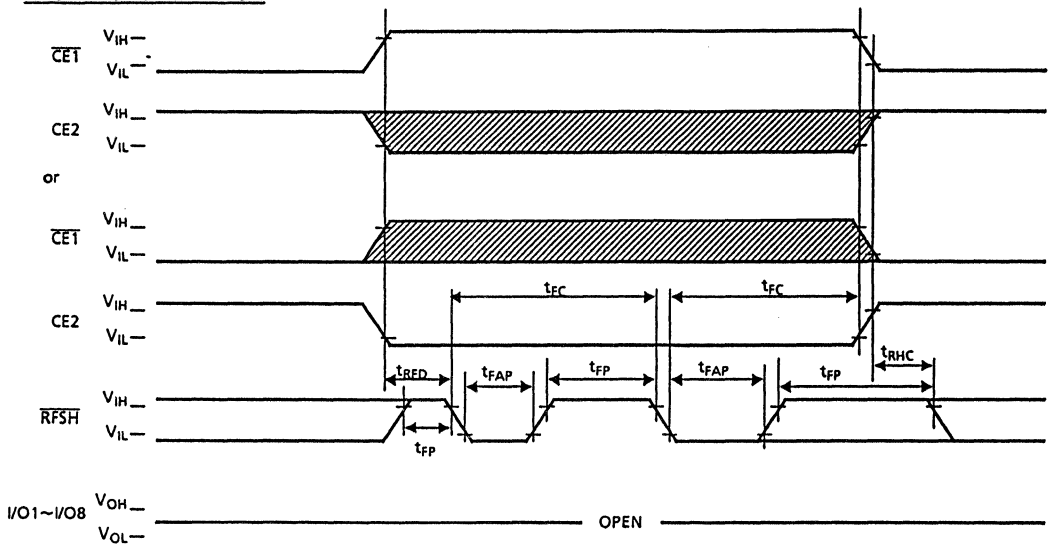


Note : A9~A16 = Don't care

▨: Don't care

Note: The device can be operated with cycling "$\overline{CE1}$" (or CE2) pin only, provided that "CE2" (or "$\overline{CE1}$") is connected to V_{IH} (or V_{IL}) level.

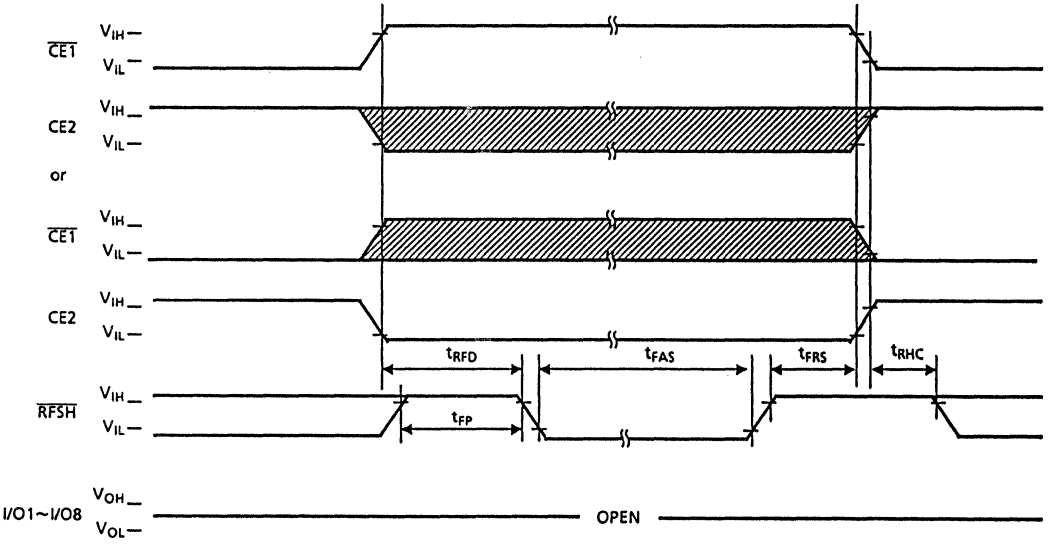
$\overline{RFSH}$ AUTO REFRESH



NOTE : $\overline{OE}$, R/W, A0~A16 = Don't care

▨: Don't care

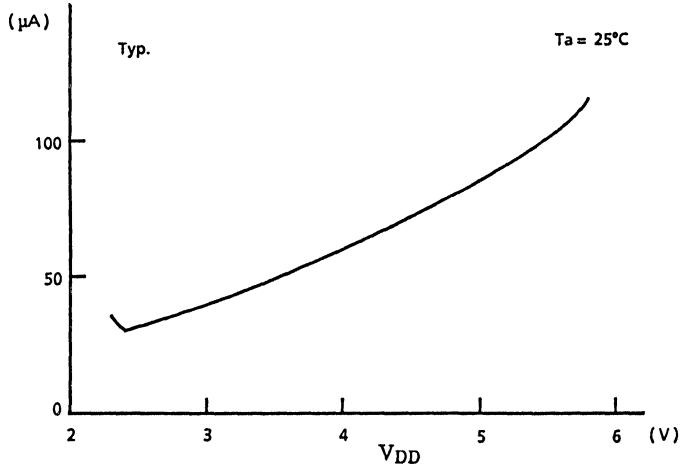
SELF REFRESH



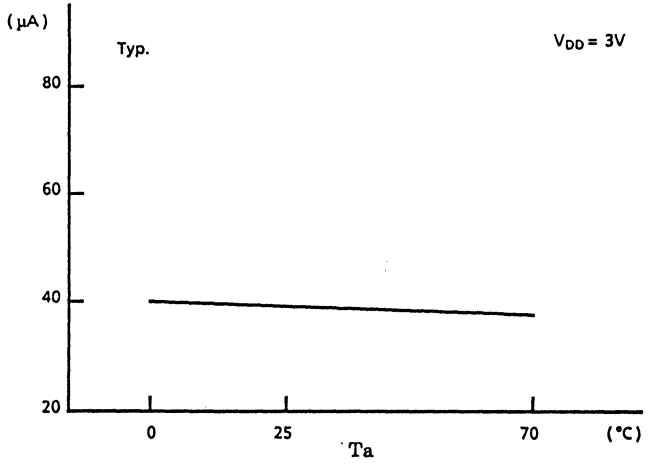
NOTE : $\overline{OE}$, R/W, A0~A16 = Don't care

▨: Don't care

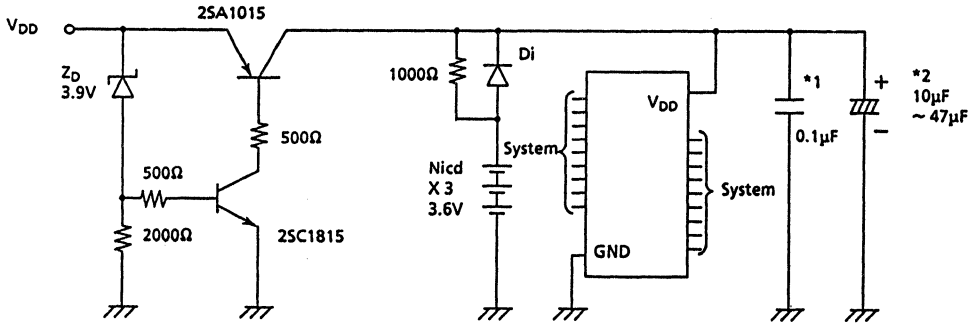
I_{DDF2} V_{DD} Characteristics



I_{DDF2} Temp. Characteristics



Battery Back Up applicable example



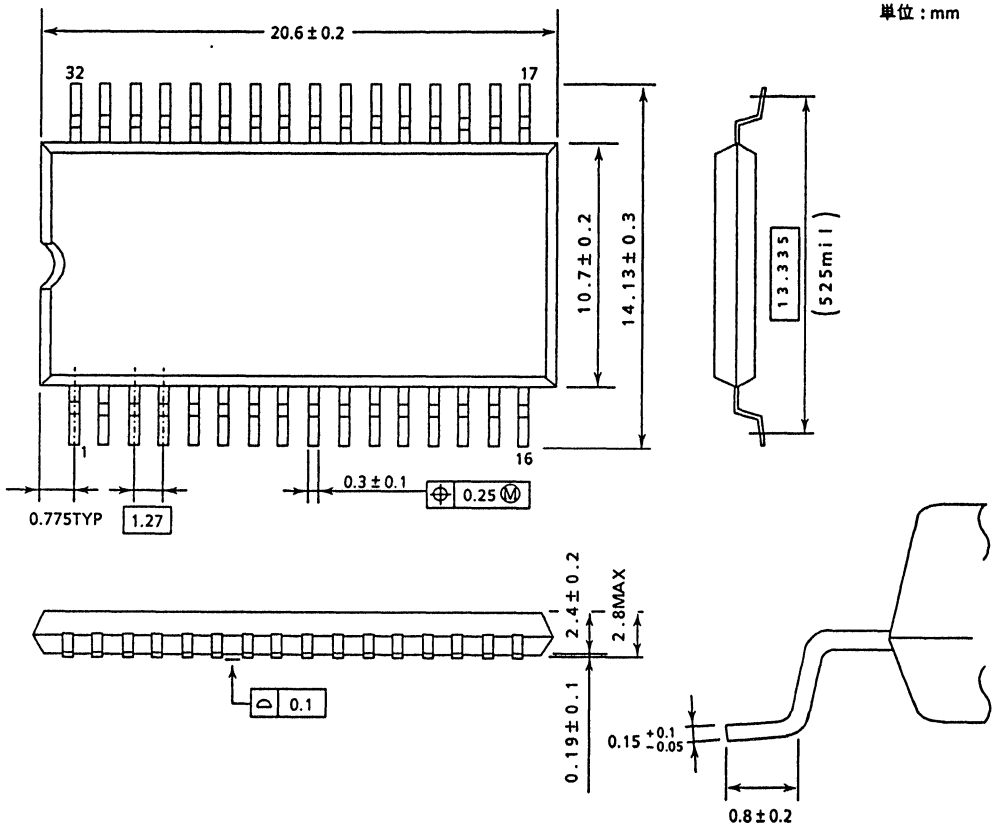
*1 : Ceramic condenser
*2 : Tantalum condenser
(The large Bypass condenser is preferable, as the noise is absorbed when the power supply is switched.)

This circuit does not have memory protection. Therefore, rapid turn off of the power supply must be avoided. Enter the Self Refresh Mode before changing to Battery Back Up Power Supply.

OUTLINE DRAWINGS

(SOP32-P-525)

単位：mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

131,072 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC518129A Family is a 1M bit high-speed CMOS Pseudo-Static RAM organized as 131,072 words by 8 bits. The TC518129A Family utilizes one transistor dynamic memory cell array with CMOS peripheral circuitry to achieve large capacity, high speed accesses, and low power requirements, using a single 5V power supply. The $\overline{RFSH}$ input allows two types of refresh operations: Auto Refresh and Self Refresh. The TC518129A Family has a static RAM-like write functionality, which allows easy interfacing to a microprocessor. The TC518129A Family is pin-compatable with the 1M bit static RAM. The TC518129AP is offered in a standard 28 pin 0.6 inch and 0.3 inch width plastic DIP. The TC518129AF is offered in a standard 28 pin 0.450 inch width small out-line plastic flat package.

FEATURES

- Organization: 1M bit (131,072 word × 8bit)
- Fast Access Time and Low Power Dissipation

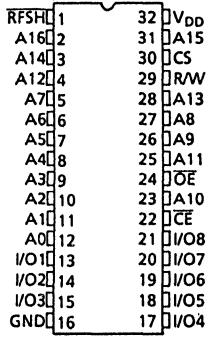
	TC518129AP Family		
	-80	-10	-12
t_{CEA} $\overline{CE}$ Access Time	80ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	1mA/200μA (-L)		

- Single Power Supply: 5V±10%
- Auto refresh uses an internal counter.
- Self refresh uses an internal timer.
- All inputs and outputs : TTL compatible
- CS standby cycle is available
- 512 refresh cycle / 8ms
- Pin Compatible: 1M SRAM (JEDEC)
- Logic Compatible: SRAM R/W Pin
- 32 Pin Standard Plastic PKG

AP/APL	600 mil DIP
ASP/ASPL	300 mil DIP
AF/AFL	450 mil SOP

PIN CONNECTION

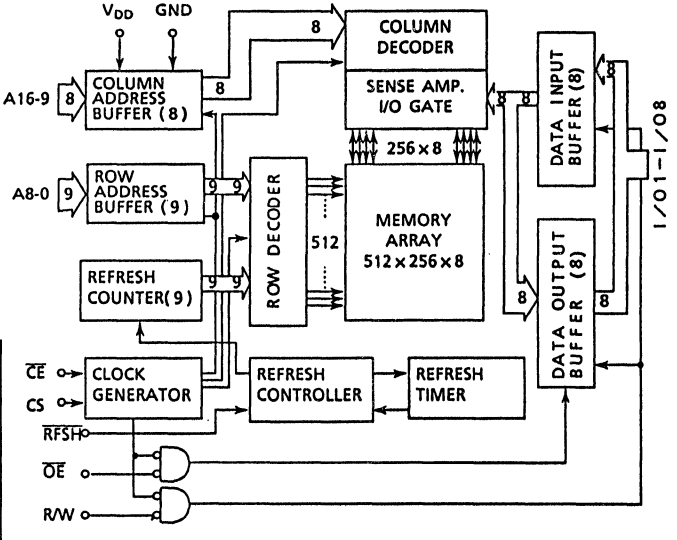
(TOP VIEW)



PIN NAMES

A0 ~ A16	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CS}$	Chip select Input
I/O1 ~ I/O8	Data Inputs / Outputs
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



FUNCTION LOGIC

$\overline{CE}$	CS	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8	CONDITION
↓	H	L	H	H	V*	OUT	Read
↓	H	*	L	H	V*	IN	Write
↓	H	H	H	H	V*	HZ	$\overline{CE}$ only Refresh
L	L	*	*	*	*	HZ	CS standby
H	*	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ −1.0V)
* ··· Don't care (6.5V ~ −1.0V)
V* ··· At $\overline{CE}$ falling edge, all address inputs are "IN", and at the other condition, the address input are "*".
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	−1.0~7.0	V	1
V_{OUT}	Output Voltage	−1.0~7.0	V	
V_{DD}	Power Supply Voltage	−1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	−55~150	°C	
T_{SOLDER}	Soldering Temperature · Time	260·10	°C·sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		PERIOD	MIN.	TYP.	MAX.	UNITS	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE}$, Address cycling: t_{RC} = t_{RC} min.		130ns	-	50	70	mA	3, 4
			160ns	-	40	60		
			190ns	-	35	50		
I_{DDS1}	Standby Current $\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IH}	TC518129AP/ASP/AF		-	-	2	mA	
		TC518129APL/ASPL/AFL		-	-	1		
I_{DDS2}	Standby Current $\overline{CE}$ = V_{DD} - 0.2V $\overline{RFSH}$ = V_{DD} - 0.2V	TC518129AP/ASP/AF		-	-	1	mA	
		TC518129APL/ASPL/AFL		-	100	200	µA	
I_{DDF1}	Self Refresh Current $\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IL}	TC518129AP/ASP/AF		-	-	2	mA	
		TC518129APL/ASPL/AFL		-	-	1		
I_{DDF2}	Self Refresh Current $\overline{CE}$ = V_{DD} - 0.2V $\overline{RFSH}$ = 0.2V	TC518129AP/ASP/AF		-	-	1	mA	
		TC518129APL/ASPL/AFL		-	100	200	µA	
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ V_{DD}, All other Inputs not under test = 0V			-10	-	10	µA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or R/W = V_{IL}), 0V ≤ V_{OUT} ≤ V_{DD}			-10	-	10	µA	
V_{OH}	Output High Level I_{OH} = -5mA			2.4	-	-	V	
V_{OL}	Output Low Level I_{OL} = 4.2mA			-	-	0.4	V	

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	-	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, CS, $\overline{OE}$, R/W, $\overline{RFSH}$)	-	7	pF
C_{IO}	Input/Output Capacitance	-	7	pF

Note) This parameter is periodically sampled and is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

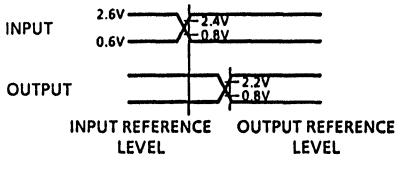
(V_{DD} = 5V ± 10%, Ta = 0~70 °C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	–80		–10		–12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	–	160	–	190	–	ns	
t_{RMW}	Read Modify Write Cycle Time	195	–	235	–	280	–	ns	
t_{CE}	CE Pulse Width	80	10,000	100	10,000	120	10,000	ns	13
t_P	CE Precharge Time	40	–	50	–	60	–	ns	
t_{CEA}	CE Access Time	–	80	–	100	–	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	35	–	40	–	50	ns	
t_{CLZ}	CE to Output in Low-Z	30	–	30	–	30	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	0	–	ns	
t_{WLZ}	Output Active from End of Write	0	–	0	–	0	–	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	–	0	–	0	–	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	–	10	–	10	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	
t_{CSS}	Chip Select Set-Up Time	0	–	0	–	–	0	ns	
t_{CSH}	Chip Select Hold Time	20	–	25	–	30	–	ns	
t_{WP}	Write Pulse Width	60	–	70	–	85	–	ns	
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000	ns	
t_{CWL}	Write Command to CE Lead Time	60	10,000	70	10,000	85	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	30	–	35	–	45	–	ns	10
t_{DSC}	Data Set-Up Time from CE	30	–	35	–	45	–	ns	10
t_{DHW}	Data Hold Time from R/W	0	–	0	–	0	–	ns	10
t_{DHC}	Data Hold Time from CE	0	–	0	–	0	–	ns	10
t_{ASC}	Address Set-Up Time	0	–	0	–	0	–	ns	11
t_{AHC}	Address Hold Time	20	–	25	–	30	–	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	–	15	–	15	–	ns	
t_{FC}	Auto Refresh Cycle Time	130	–	160	–	190	–	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from CE	40	–	50	–	60	–	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–	ns	12
t_{FRS}	CE Delay Time from $\overline{RFSH}$ (Self Refresh)	160	–	190	–	225	–	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	–	8	–	8	–	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

NOTES:

1) Stress greater than those listed under " Absolute Maximum Ratings " may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO} depends on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100μs with high $\overline{CE}$ is required after power-up, before proper device operation is achieved.
6) AC measurements assume t_T = 5ns.
7) Timing reference level

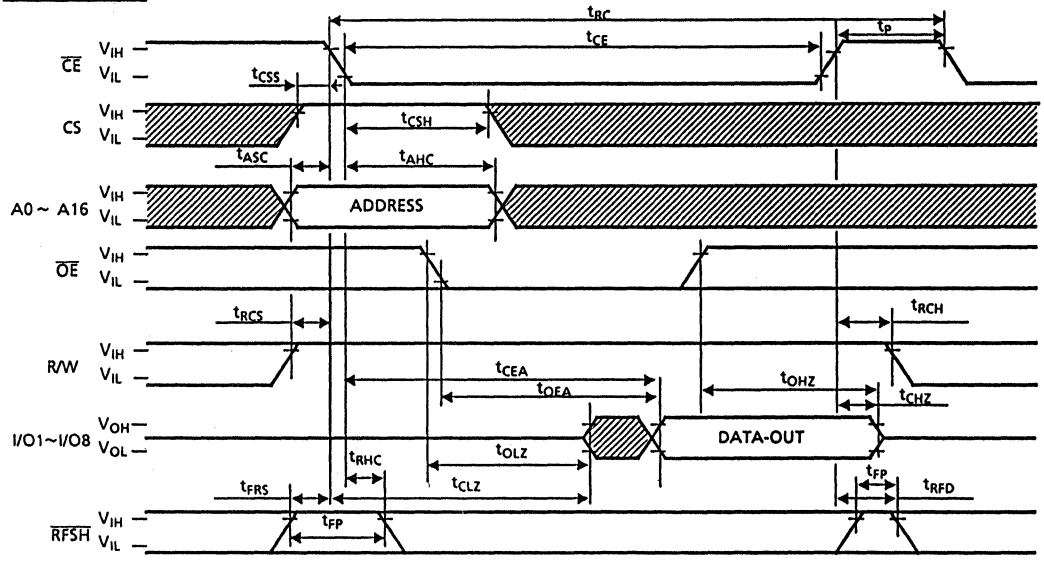
Input Level	:	V_{IH} = 2.6V
		V_{IL} = 0.6V
Input Reference Level	:	V_{IH} = 2.4V
		V_{IL} = 0.8V
Output Reference Level	:	V_{OH} = 2.2V
		V_{OL} = 0.8V



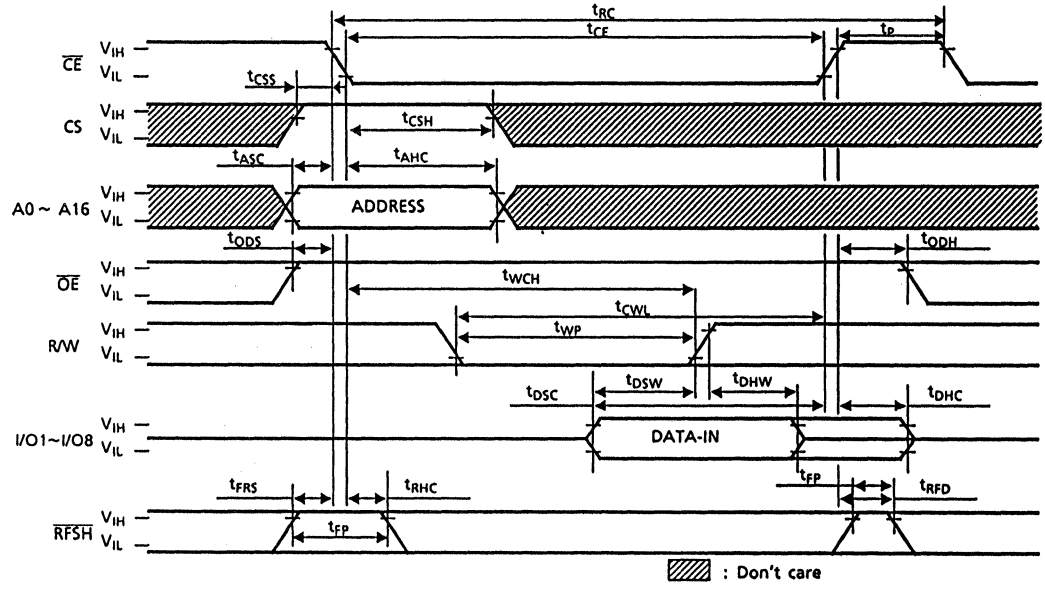
8) Measured with a load equivalent to 2 TTL loads and 100pF.
9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE}$ = V_{IH}.
    Auto refresh: $\overline{RFSH}$ pulse width $\leqq$ t_{FAP} (max.)
    Self refresh : $\overline{RFSH}$ pulse width $\geqq$ t_{FAS} (min.)
    The timing parameter (t_{FRS}) must be kept for proper device operation in the following conditions.
    - after self refresh
    - in case of "$\overline{RFSH}$" = "L" after power-up

TIMING WAVEFORMS

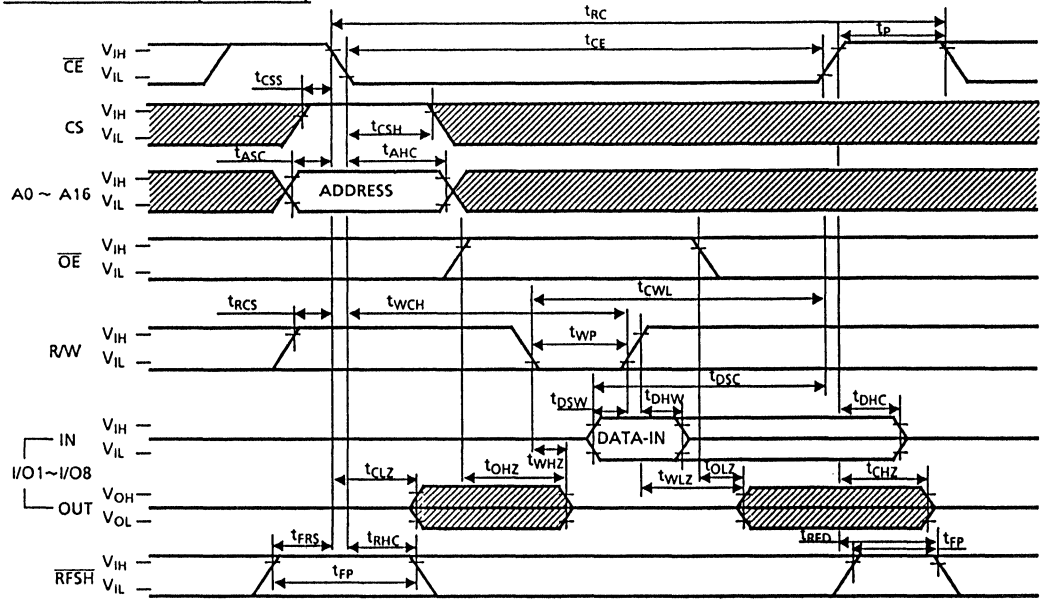
READ CYCLE



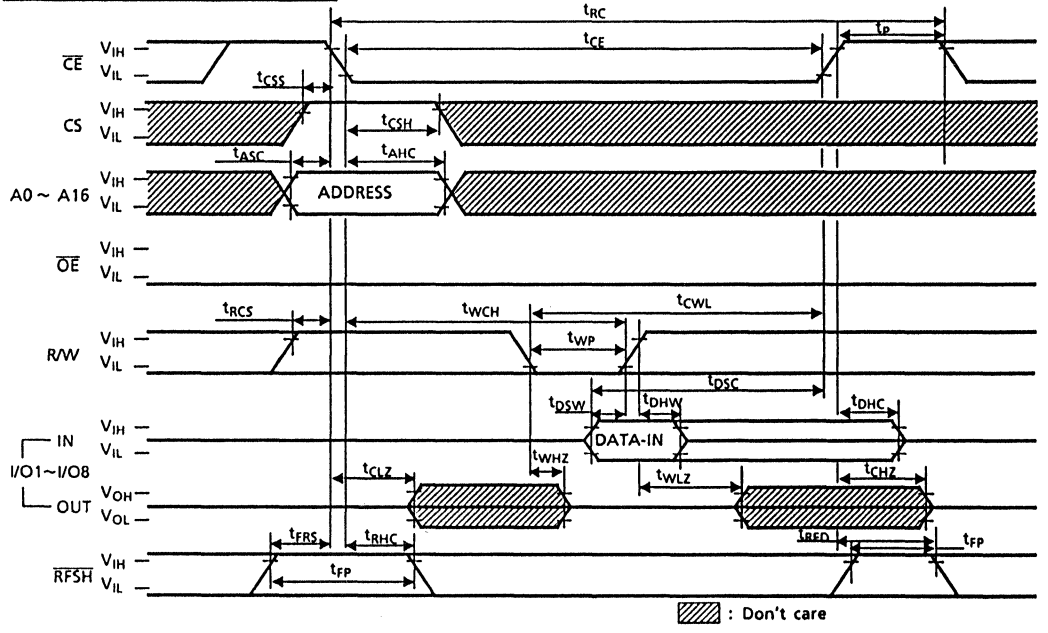
WRITE CYCLE-1 ($\overline{OE}$ Fix High)



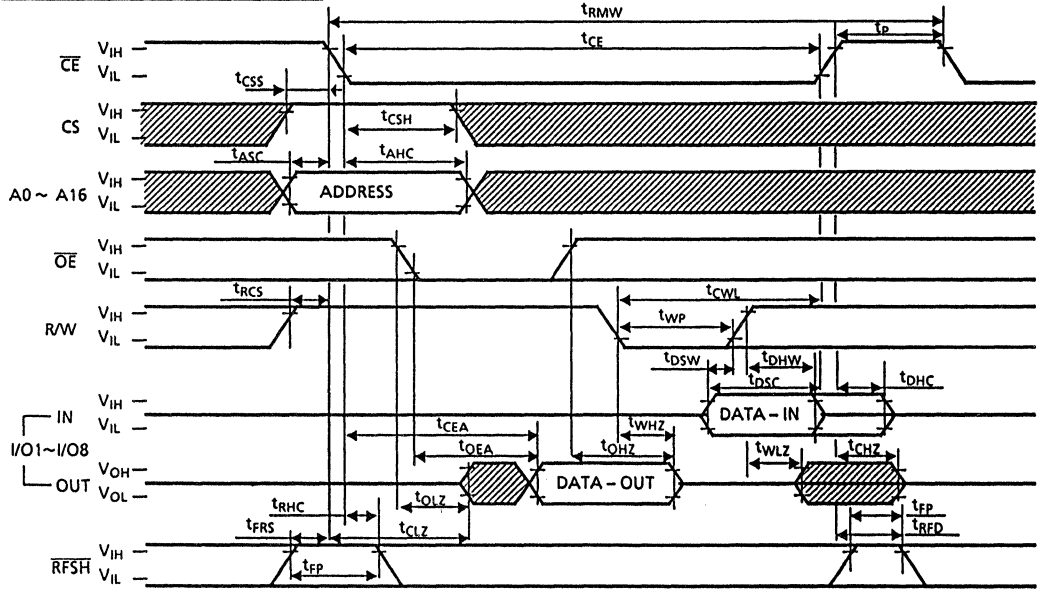
WRITE CYCLE - 2 ($\overline{OE}$ Clock)



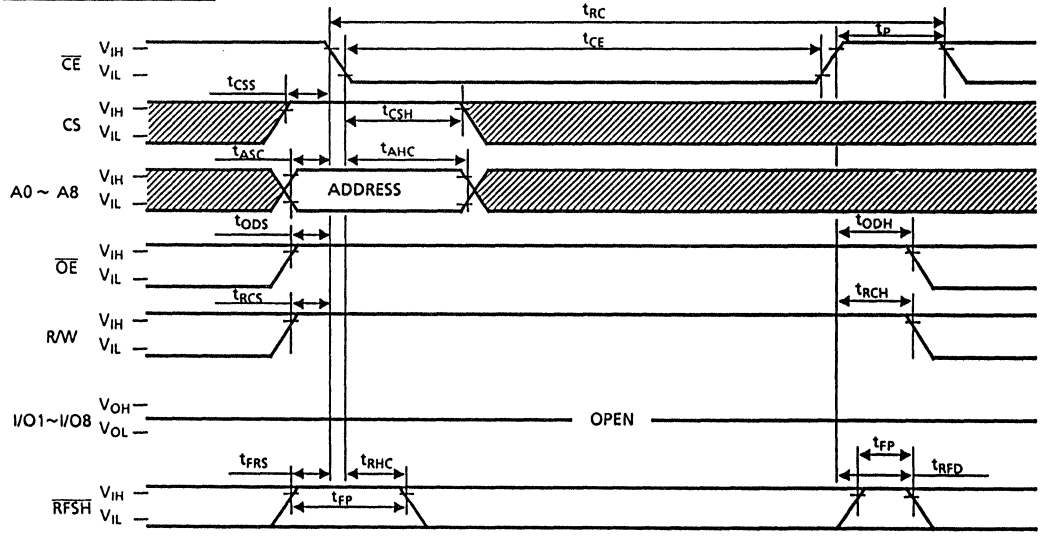
WRITE CYCLE - 3 ($\overline{OE}$ Fix Low)



READ MODIFY WRITE CYCLE

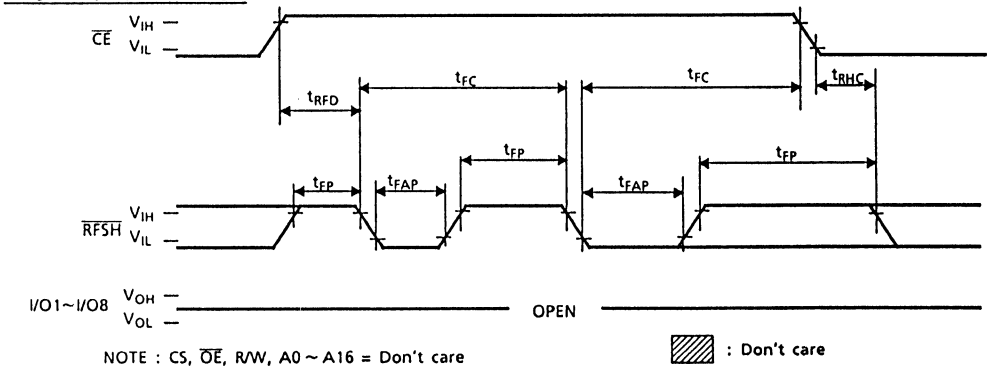


$\overline{CE}$ ONLY REFRESH



NOTE : A9 ~ A16 = Don't care, ▨ : Don't care

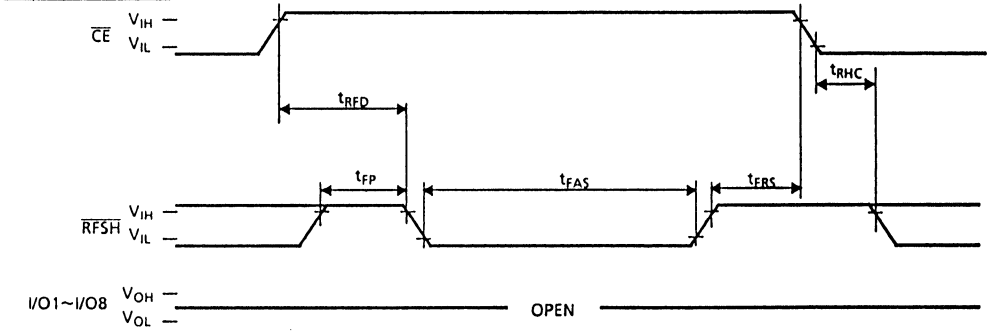
$\overline{RFSH}$ AUTO REFRESH



NOTE : CS, $\overline{OE}$, R/W, A0 ~ A16 = Don't care

: Don't care

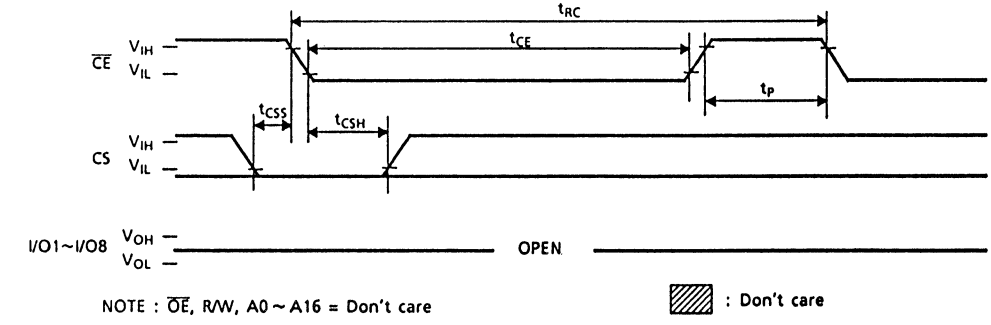
SELF REFRESH



NOTE : CS, $\overline{OE}$, R/W, A0 ~ A16 = Don't care

: Don't care

CS STANDBY MODE



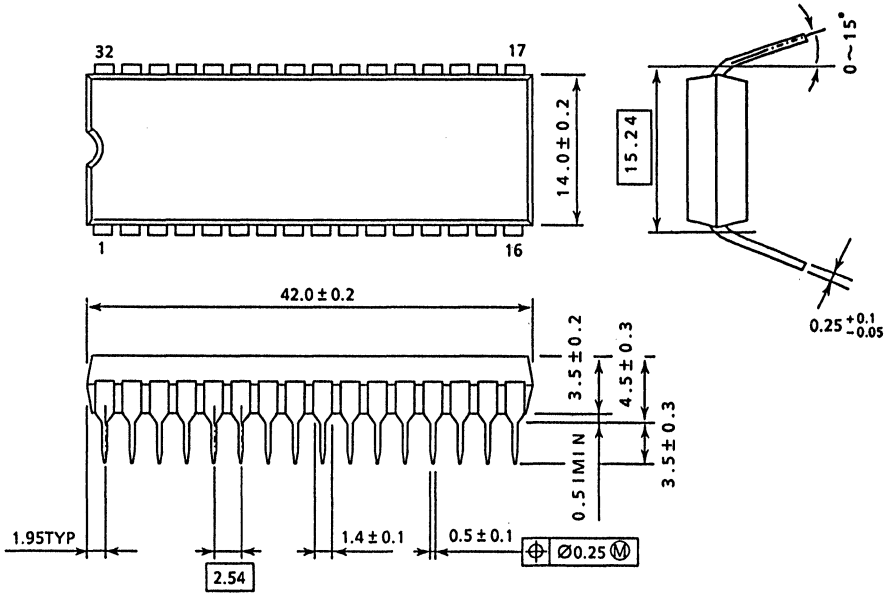
NOTE : $\overline{OE}$, R/W, A0 ~ A16 = Don't care

: Don't care

OUTLINE DRAWINGS

(DIP32-P-600)

UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

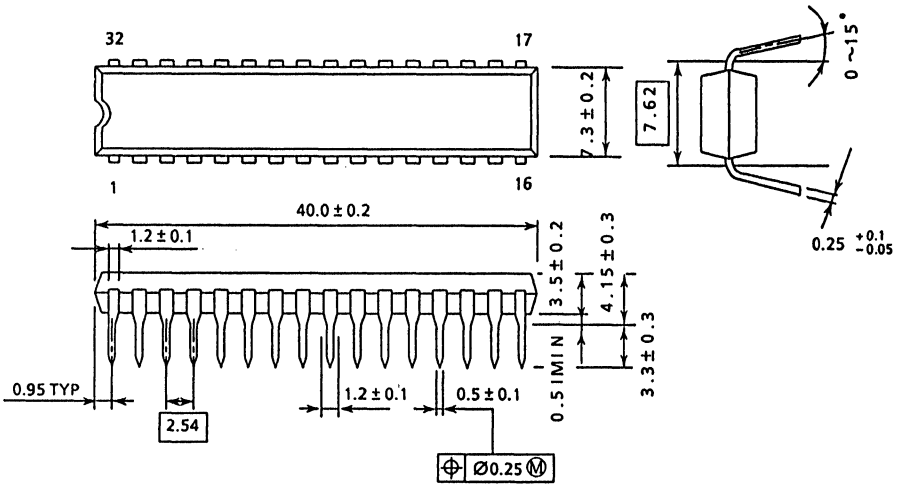
These outline drawings apply to:

TC518129AP-80, TC518129APL-80
TC518129AP-10, TC518129APL-10
TC518129AP-12, TC518129APL-12

OUTLINE DRAWINGS

(DIP32-P-300)

UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

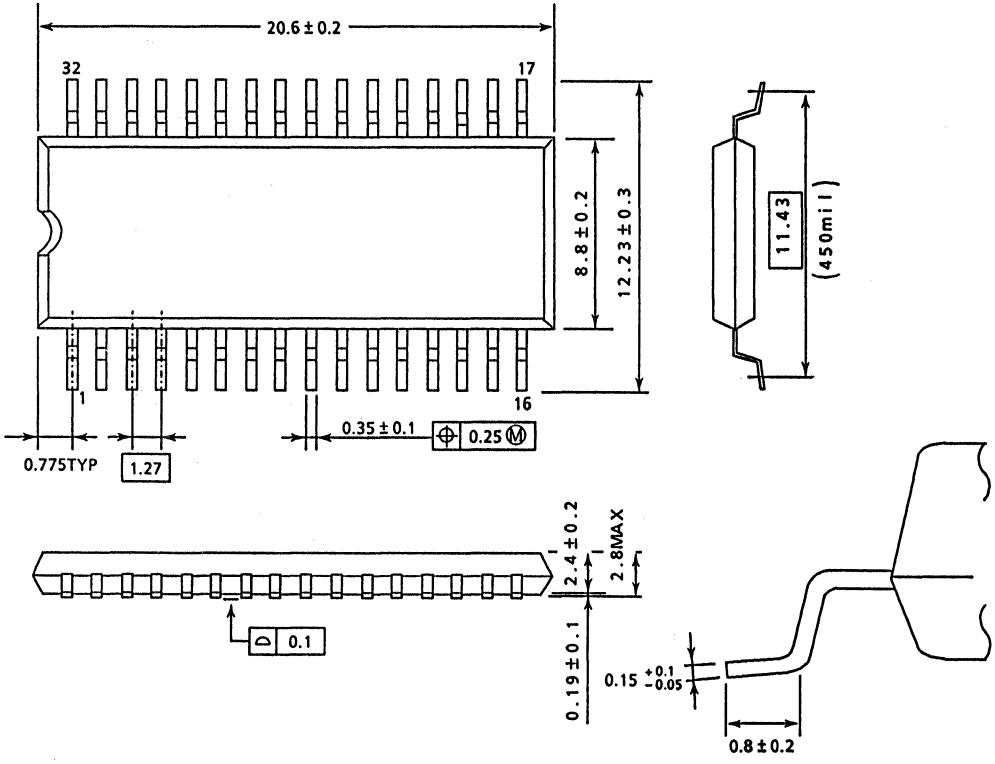
These outline drawings apply to:

TC518129ASP-80, TC518129ASPL-80
TC518129ASP-10, TC518129ASPL-10
TC518129ASP-12, TC518129ASPL-12

OUTLINE DRAWINGS

(SOP32-P-450)

UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

These outline drawings apply to:

TC518129AF-80, TC518129AFL-80
TC518129AF-10, TC518129AFL-10
TC518129AF-12, TC518129AFL-12

131,072 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC518129A-LV Family is a 1M bit high-speed CMOS Pseudo-Static RAM organized as 131,072 words by 8 bits. The TC518129A-LV Family utilizes one transistor dynamic memory cell array with CMOS peripheral circuitry to achieve large capacity, high speed accesses, and low power requirements, using a single 5V power supply. The TC518129A-LV Family offers 3V data retention capability for battery back-up applications. The $\overline{RFSH}$ input allows two types of refresh operations: Auto Refresh and Self Refresh. The TC518129A-LV Family has a static RAM-like read/write functionality, which allows easy interfacing to a microprocessor. The TC518129A-LV Family is pin-compatable with the 1M bit static RAM. The TC518129APL-LV is offered in a standard 28 pin 0.6 inch and 0.3 inch width plastic DIP. The TC518129AFL-LV is offered in a standard 28 pin 0.450 inch width small out-line plastic flat package.

FEATURES

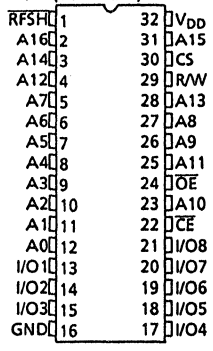
- Organization: 1M bit (131,072 word × 8bit)
- Fast Access Time and Low Power Dissipation

		TC518129APL Family		
		-80	-10	-12
t_{CEA} $\overline{CE}$ Access Time		80ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time		35ns	40ns	50ns
t_{RC} Cycle Time		130ns	160ns	190ns
Power Dissipation		385mW	330mW	275mW
Self Refresh Current	5.5V	200μA		
	3.0V	100μA		

- Single Power Supply: 5V±10%
- Data Retention Supply Voltage: 3.0V ~ 5.5V
- Auto refresh is capable by internal counter.
- Self refresh is capable by internal timer.
- Auto refresh uses an internal counter.
- Self refresh uses an internal timer.
- 512 refresh cycle / 8ms
- Logic Compatible: SRAM R/W Pin
- 32 Pin Standard Plastic PKG
  - APL 600 mil DIP
  - AFL 450 mil SOP

PIN CONNECTION

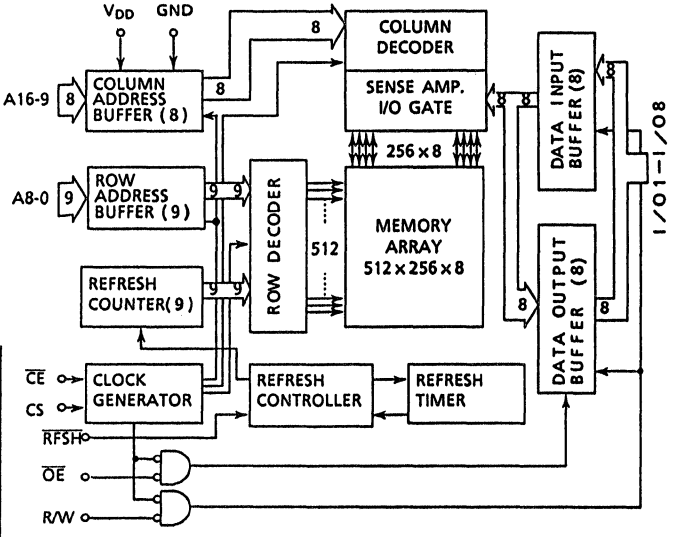
(TOP VIEW)



PIN NAMES

A0 ~ A16	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE}$	Chip Enable Input
CS	Chip select Input
I/O1 ~ I/O8	Data Inputs / Outputs
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



FUNCTION LOGIC

$\overline{CE}$	CS	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8	CONDITION
↓	H	L	H	H	V*	OUT	Read
↓	H	*	L	H	V*	IN	Write
↓	H	H	H	H	V*	HZ	$\overline{CE}$ only Refresh
L	L	*	*	*	*	HZ	CS standby
H	*	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ −1.0V)
* ··· Don't care (6.5V ~ −1.0V)
V* ··· At $\overline{CE}$ falling edge, all address inputs are "IN", and at the other condition, the address input are "*".
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	−1.0~7.0	V	1
V_{OUT}	Output Voltage	−1.0~7.0	V	
V_{DD}	Power Supply Voltage	−1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	−55~150	°C	
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER	PERIOD	MIN.	TYP.	MAX.	UNITS	NOTE
I_{DDO}	Operating Current	130ns	–	50	70	mA	3, 4
	(Average Power Supply Operating Current)	160ns	–	40	60		
	$\overline{CE}$, Address cycling: $t_{RC} = t_{RC}$ min.	190ns	–	35	50		
I_{DDS1}	Standby Current $\overline{CE} = V_{IH}$, $\overline{RFSH} = V_{IH}$		–	–	1	mA	
I_{DDS2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$, $\overline{RFSH} = V_{DD} - 0.2V$		–	100	200	µA	
I_{DDF1}	Self Refresh Current $\overline{CE} = V_{IH}$, $\overline{RFSH} = V_{IL}$		–	–	1	mA	
I_{DDF2}	Self Refresh Current $\overline{CE} = V_{DD} - 0.2V$, $\overline{RFSH} = 0.2V$		–	100	200	µA	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = 0V		– 10	–	10	µA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or R/W = V_{IL}), $0V \leq V_{OUT} \leq V_{DD}$		– 10	–	10	µA	
V_{OH}	Output High Level I_{OH} = – 5mA		2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 4.2mA		–	–	0.4	V	

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, CS, $\overline{OE}$, R/W, $\overline{RFSH}$)	–	7	pF
C_{I0}	Input / Output Capacitance	–	7	pF

Note) This parameter is periodically sampled and is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

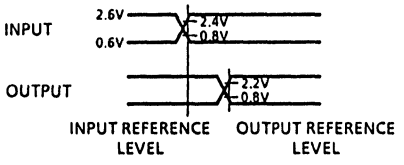
(V_{DD} = 5V ± 10%, Ta = 0~70 °C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	-	160	-	190	-	ns	
t_{RMW}	Read Modify Write Cycle Time	195	-	235	-	280	-	ns	
t_{CE}	$\overline{CE}$ Pulse Width	80	10,000	100	10,000	120	10,000	ns	
t_P	$\overline{CE}$ Precharge Time	40	-	50	-	60	-	ns	
t_{CEA}	$\overline{CE}$ Access Time	-	80	-	100	-	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	30	-	30	-	30	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{WLZ}	Output Active from End of Write	0	-	0	-	0	-	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	-	0	-	0	-	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	-	10	-	10	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	
t_{CSS}	Chip Select Set-Up Time	0	-	0	-	0	-	ns	
t_{CSH}	Chip Select Hold Time	20	-	25	-	30	-	ns	
t_{WP}	Write Pulse Width	60	-	70	-	85	-	ns	
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	60	10,000	70	10,000	85	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	30	-	35	-	45	-	ns	10
t_{DSC}	Data Set-Up Time from $\overline{CE}$	30	-	35	-	45	-	ns	10
t_{DHW}	Data Hold Time from R/W	0	-	0	-	0	-	ns	10
t_{DHC}	Data Hold Time from $\overline{CE}$	0	-	0	-	0	-	ns	10
t_{ASC}	Address Set-Up Time	0	-	0	-	0	-	ns	11
t_{AHC}	Address Hold Time	20	-	25	-	30	-	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	-	15	-	15	-	ns	
t_{FC}	Auto Refresh Cycle Time	130	-	160	-	190	-	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from $\overline{CE}$	40	-	50	-	60	-	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	-	8,000	-	8,000	-	ns	12
t_{FRS}	$\overline{CE}$ Delay Time from $\overline{RFSH}$ (Self Refresh)	160	-	190	-	225	-	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	-	8	-	8	-	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

NOTES:

1) Stress greater than those listed under " Absolute Maximum Ratings " may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO} depends on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100μs with high $\overline{CE}$ is required after power-up, before proper device operation is achieved.
6) AC measurements assume $t_T = 5ns$.
7) Timing reference level

Input Level	:	$V_{IH} = 2.6V$
		$V_{IL} = 0.6V$
Input Reference Level	:	$V_{IH} = 2.4V$
		$V_{IL} = 0.8V$
Output Reference Level	:	$V_{OH} = 2.2V$
		$V_{OL} = 0.8V$

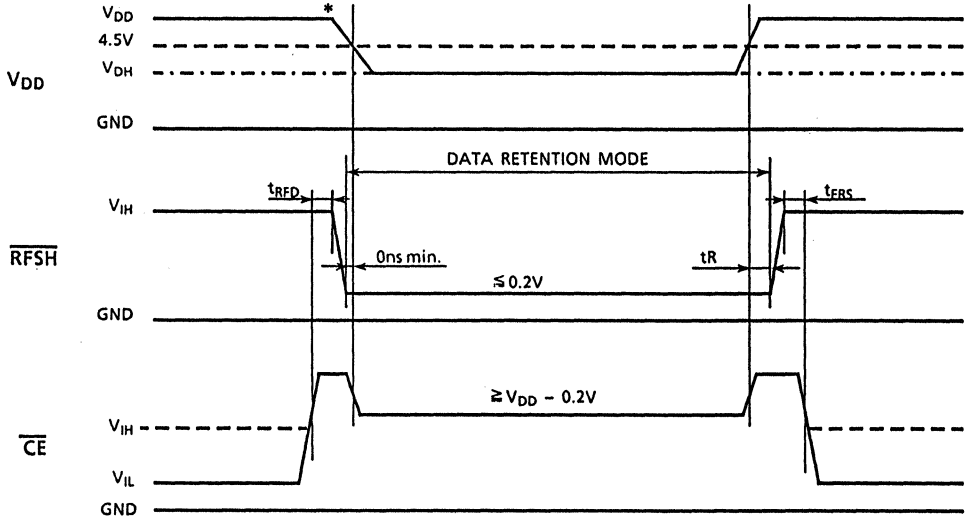


8) Measured with a load equivalent to 2 TTL loads and 100pF.
9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE} = V_{IH}$.
    Auto refresh : $\overline{RFSH}$ pulse width $\leqq t_{FAP}$ (max.)
    Self refresh : $\overline{RFSH}$ pulse width $\geqq t_{FAS}$ (min.)
    The timing parameter (t_{FRS}) must be kept for proper device operation in the following conditions.
    - after self refresh
    - in case of "$\overline{RFSH}$" = "L" after power-up

DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		3.0	-	5.5	V
I_{DDF2}	Self Refresh Current	V_{DH} = 3.0V	-	40	100	μA
		V_{DH} = 5.5V	-	100	200	μA
t_R	Recovery Time		5	-	-	mS

*The falling slope of V_{DD} must be more than 50ms in order to operate the device safely. (20ms/V)



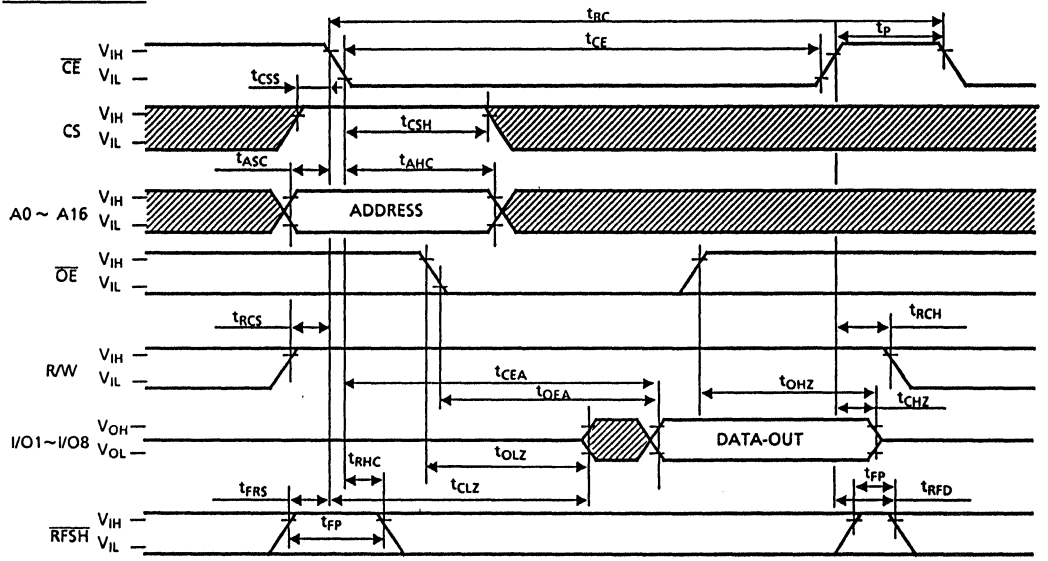
(Note)◦ CS, $\overline{OE}$, R/W, A0~A16 = Don't care

◦ I_{DDF1} is applied in $\overline{RFSH} = V_{IL\ max.}$, $\overline{CE} = V_{IH\ min.}$

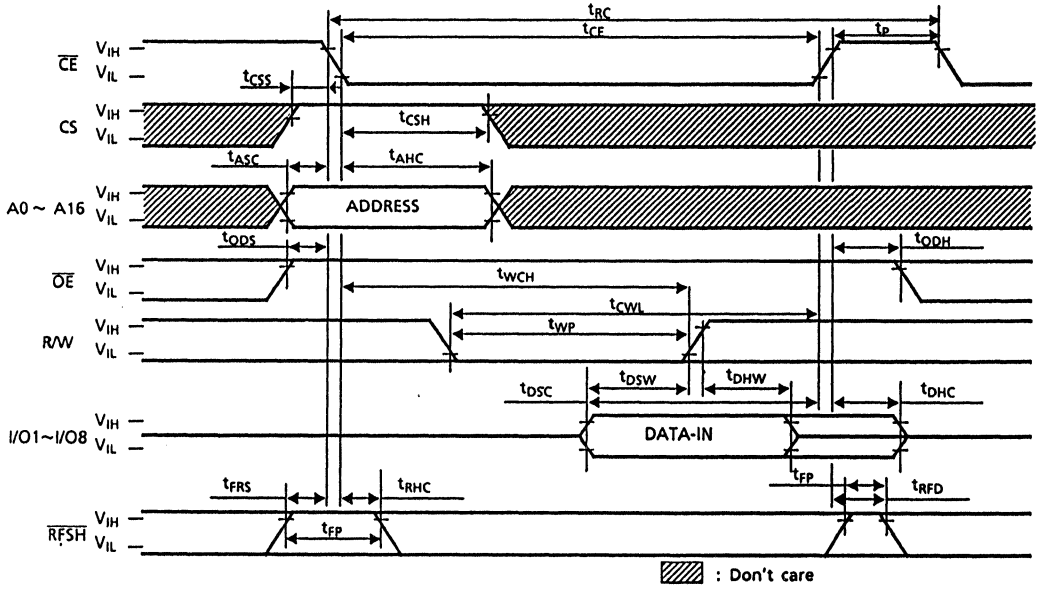
◦ At any state but Data Retention Mode, Auto Refresh or CE Only Refresh with 512cycle/8ms is required.

TIMING WAVEFORMS

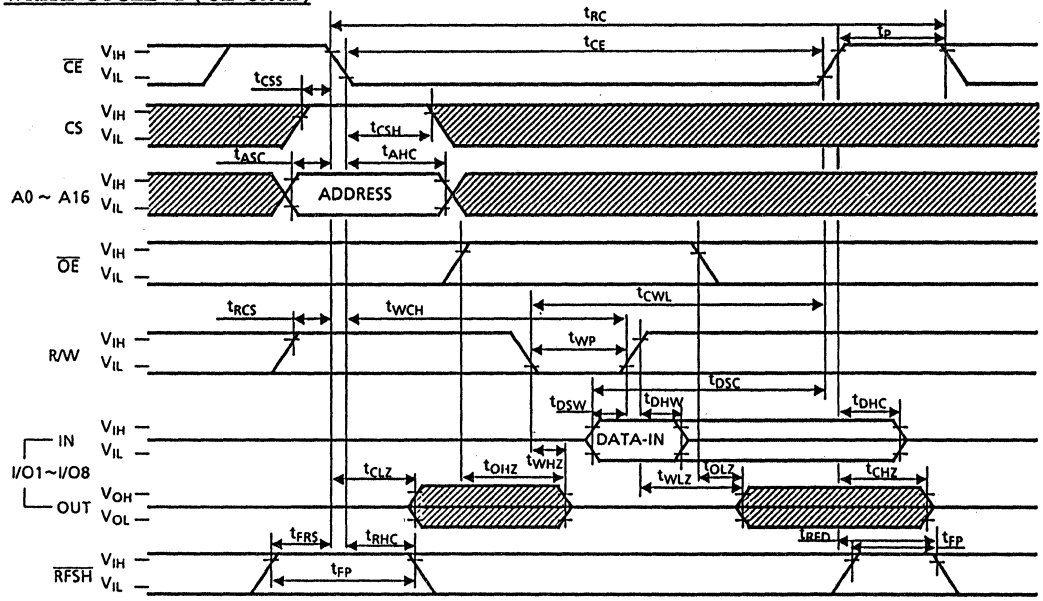
READ CYCLE



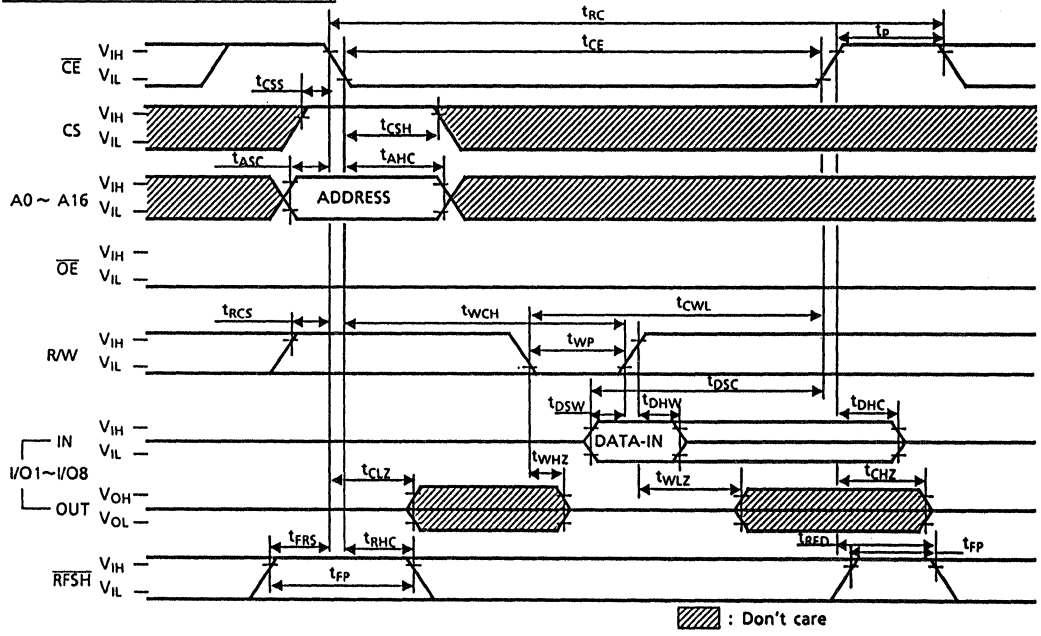
WRITE CYCLE-1 ($\overline{OE}$ Fix High)



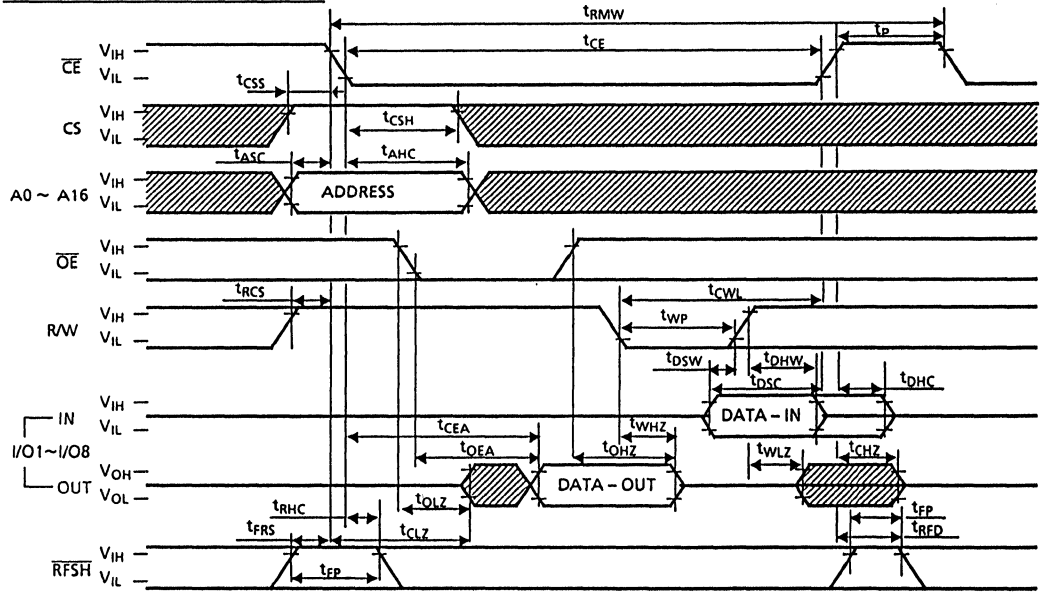
WRITE CYCLE - 2 ($\overline{OE}$ Clock)



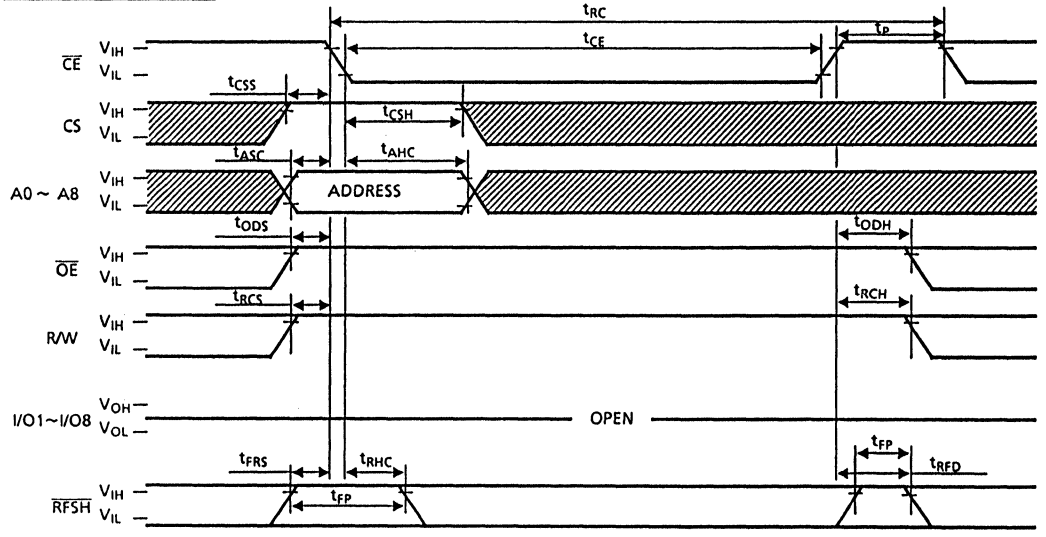
WRITE CYCLE - 3 ($\overline{OE}$ Fix Low)



READ MODIFY WRITE CYCLE

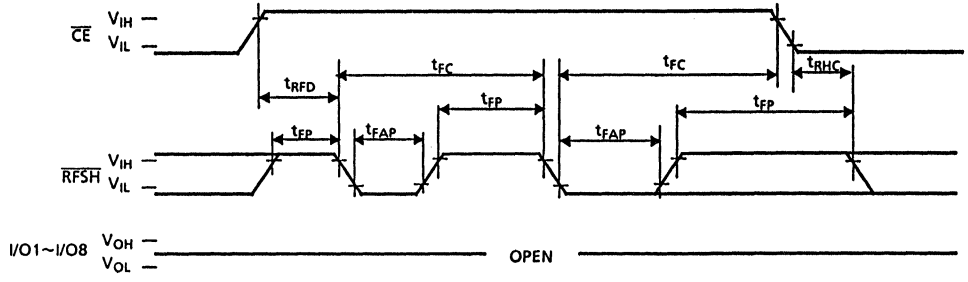


CE ONLY REFRESH



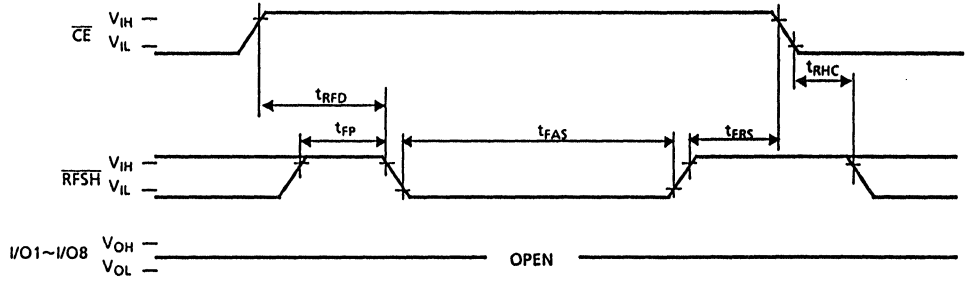
NOTE : A9 ~ A16 = Don't care, ▨ : Don't care

$\overline{RFSH}$ AUTO REFRESH



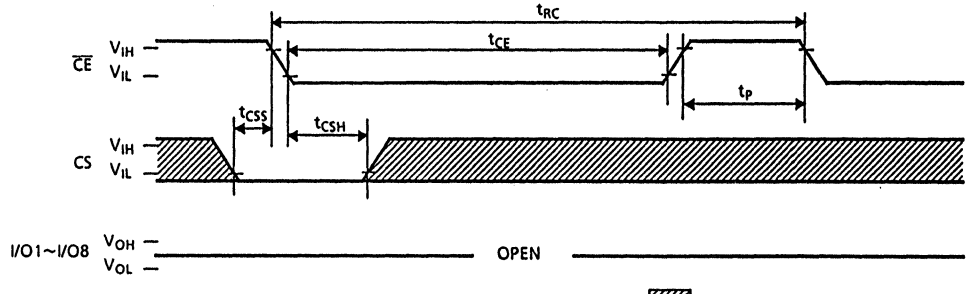
NOTE : CS, $\overline{OE}$, R/W, A0 ~ A16 = Don't care

SELF REFRESH



NOTE : CS, $\overline{OE}$, R/W, A0 ~ A16 = Don't care

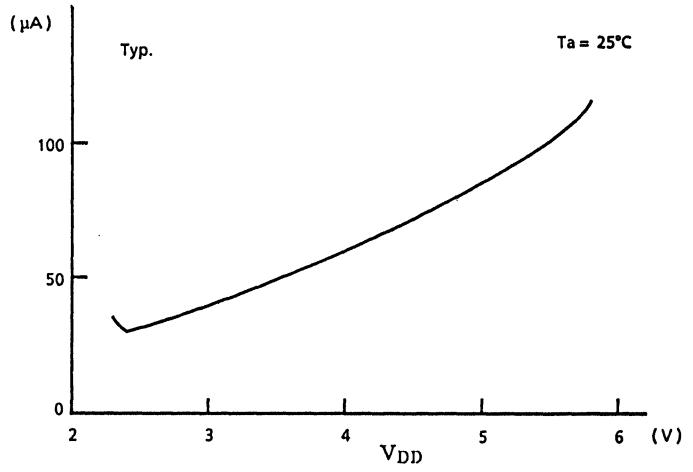
CS STANDBY MODE



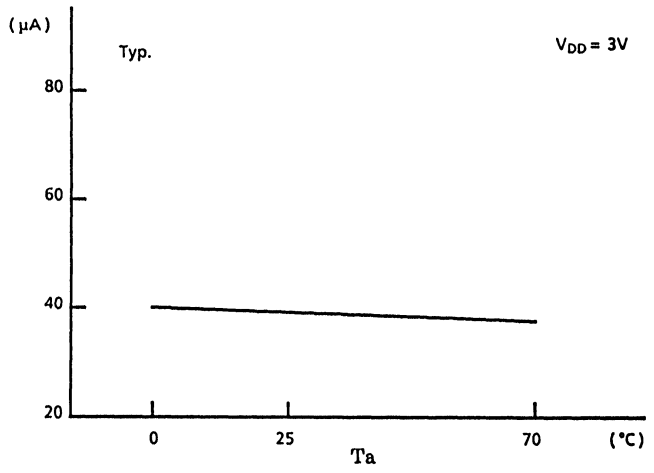
NOTE : $\overline{OE}$, R/W, A0 ~ A16 = Don't care

: Don't care

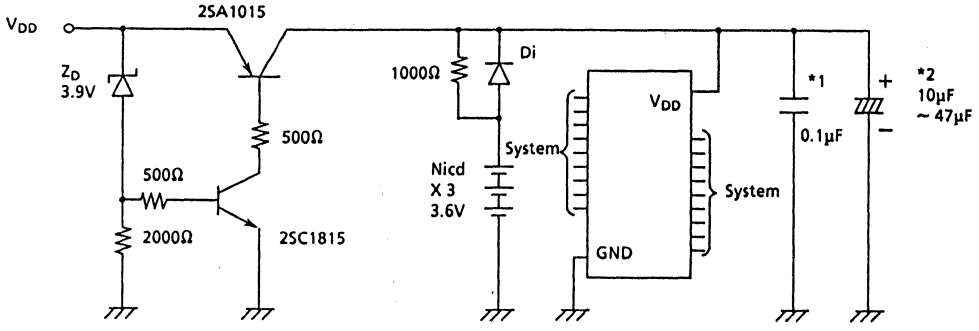
I_{DDF2} V_{DD} Characteristics



I_{DDF2} Temp. Characteristics



Battery Back Up applicable example



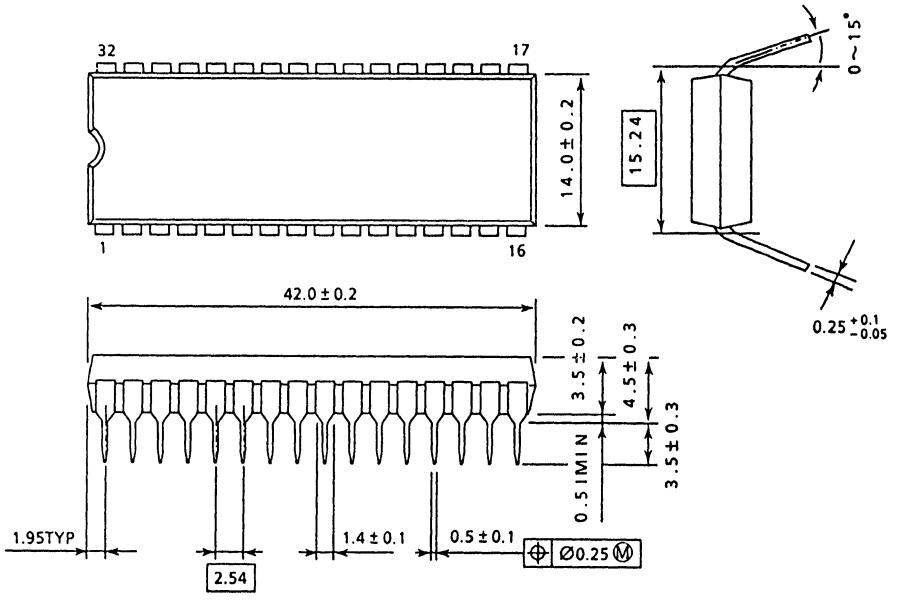
*1 : Ceramic condenser
*2 : Tantalum condenser
(The large Bypass condenser is preferable, as the noise is absorbed when the power supply is switched.)

This circuit does not have memory protection. Therefore, rapid turn-off of the power supply must be avoided. Enter the Self Refresh Mode before changing to Battery Back Up Power Supply.

OUTLINE DRAWINGS

(DIP32-P-600)

UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

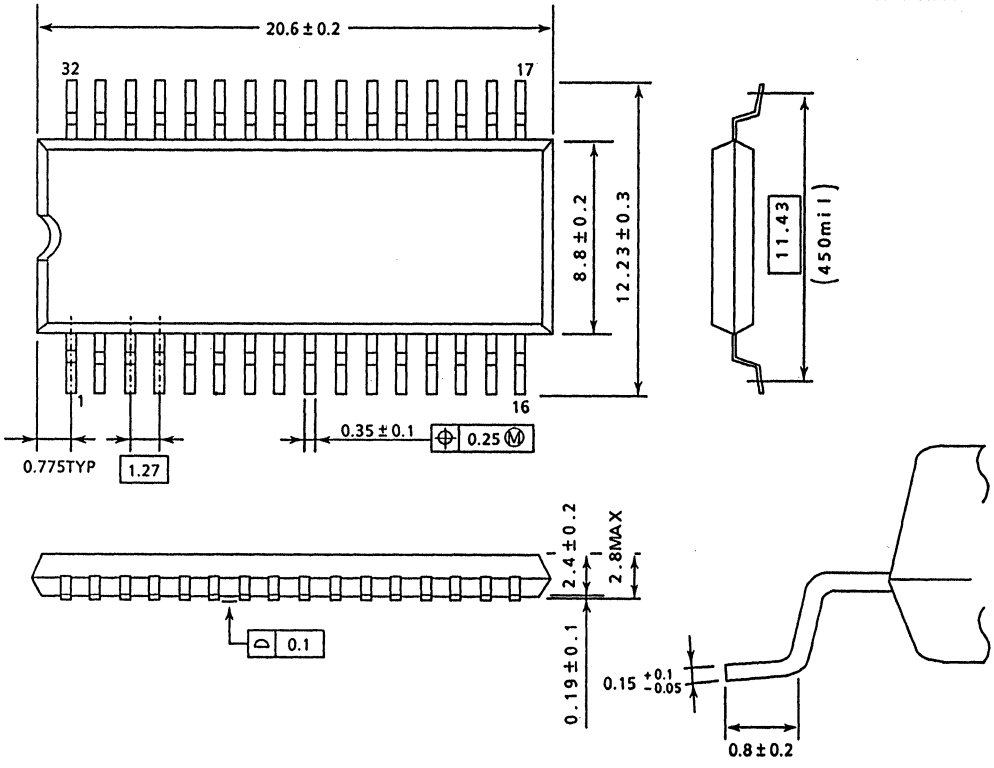
These outline drawings apply to:

TC518129APL-80LV
TC518129APL-10LV
TC518129APL-12LV,

OUTLINE DRAWINGS

(SOP32-P-450)

UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

These outline drawings apply to:

TC518129AF-80, TC518129AFL-80
TC518129AF-10, TC518129AFL-10
TC518129AF-12, TC518129AFL-12

131,072 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC518129A Family is a 1M bit high-speed CMOS Pseudo-Static RAM organized as 131,072 words by 8 bits. The TC518129A Family utilizes one transistor dynamic memory cell array with CMOS peripheral circuitry to achieve large capacity, high speed accesses, and low power requirements, using a single 5V power supply. The $\overline{RFSH}$ input allows two types of refresh operations: Auto Refresh and Self Refresh. The TC518129A Family has a static RAM-like read/write functionality, which allows easy interfacing to a microprocessor. The TC518129A Family is pin-compatable with the 1M bit static RAM. The TC518129AFWL is offered in a standard 28 pin 0.525 inch width small out-line plastic flat package.

FEATURES

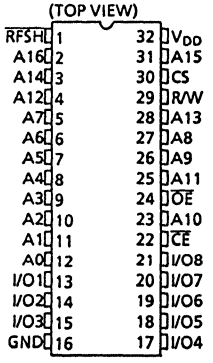
- Organization: 1M bit (131,072 word × 8bit)
- Fast Access Time and Low Power Dissipation

	TC518129AFW Family		
	-80	-10	-12
t_{CEA} $\overline{CE}$ Access Time	80ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time	35ns	40ns	50ns
t_{RC} Cycle Time	130ns	160ns	190ns
Power Dissipation	385mW	330mW	275mW
Self Refresh Current	1mA/200μA (-L)		

- Single Power Supply: 5V±10%
- Auto refresh uses an internal counter.
- Self refresh uses an internal timer.
- All inputs and outputs : TTL compatible
- CS standby cycle is capable
- 512 refresh cycle/8ms
- Logic Compatible: SRAM R/W Pin
- 32 Pin Standard Plastic PKG
  525 mil SOP

PIN CONNECTION

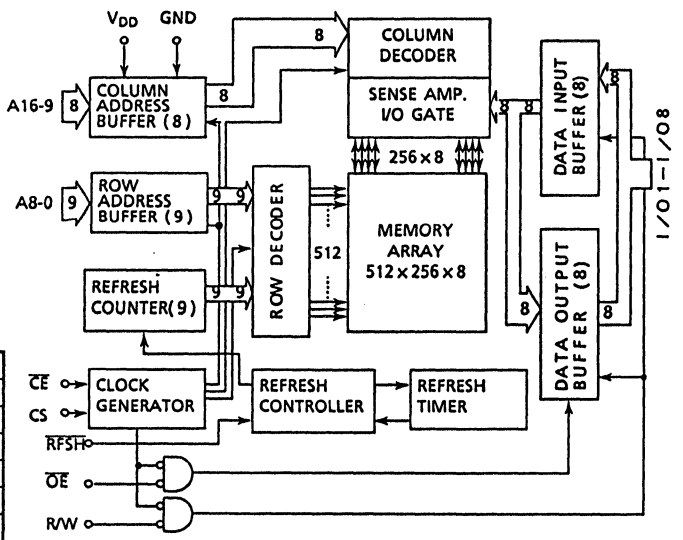
(TOP VIEW)



PIN NAMES

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE}$	Chip Enable Input
CS	Chip select Input
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



FUNCTION LOGIC

$\overline{CE}$	CS	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8	CONDITION
L	H	L	H	H	V*	OUT	Read
L	H	*	L	H	V*	IN	Write
L	H	H	H	H	V*	HZ	$\overline{CE}$ only Refresh
L	L	*	*	*	*	HZ	CS standby
H	*	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ −1.0V)
* ··· Don't care (6.5V ~ −1.0V)
V* ··· At $\overline{CE}$ falling edge, all address inputs are "IN", and at the other condition, the address input are "*".
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	−1.0~7.0	V	1
V_{OUT}	Output Voltage	−1.0~7.0	V	
V_{DD}	Power Supply Voltage	−1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	−55~150	°C	
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	
V_{IL}	Input Low Voltage	−1.0	−	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER		PERIOD	MIN.	TYP.	MAX.	UNITS	NOTES
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE}$, Address cycling: $t_{RC} = t_{RC}$ min.		130ns	-	50	70	mA	3, 4
			160ns	-	40	60		
			190ns	-	35	50		
I_{DDS1}	Standby Current $\overline{CE} = V_{IH}$ $\overline{RFSH} = V_{IH}$	TC518129AFW		-	-	2	mA	
		TC518129AFWL		-	-	1		
I_{DDS2}	Standby Current $\overline{CE} = V_{DD} - 0.2V$ $\overline{RFSH} = V_{DD} - 0.2V$	TC518129AFW		-	-	1	mA	
		TC518129AFWL		-	100	200	µA	
I_{DDF1}	Self Refresh Current $\overline{CE} = V_{IH}$ $\overline{RFSH} = V_{IL}$	TC518129AFW		-	-	2	mA	
		TC518129AFWL		-	-	1		
I_{DDF2}	Self Refresh Current $\overline{CE} = V_{DD} - 0.2V$ $\overline{RFSH} = 0.2V$	TC518129AFW		-	-	1	mA	
		TC518129AFWL		-	100	200	µA	
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = 0V			-10	-	10	µA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or R/W = V_{IL}), $0V \leq V_{OUT} \leq V_{DD}$			-10	-	10	µA	
V_{OH}	Output High Level I_{OH} = -5mA			2.4	-	-	V	
V_{OL}	Output Low Level I_{OL} = 4.2mA			-	-	0.4	V	

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	-	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, CS, $\overline{OE}$, R/W, $\overline{RFSH}$)	-	7	pF
C_{IO}	Input/Output Capacitance	-	7	pF

Note) This parameter is periodically sampled and is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

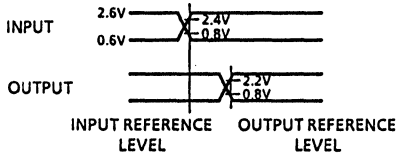
(V_{DD} = 5V ± 10%, Ta = 0~70 °C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	-	160	-	190	-	ns	
t_{RMW}	Read Modify Write Cycle Time	195	-	235	-	280	-	ns	
t_{CE}	$\overline{CE}$ Pulse Width	80	10,000	100	10,000	120	10,000	ns	
t_P	$\overline{CE}$ Precharge Time	40	-	50	-	60	-	ns	
t_{CEA}	$\overline{CE}$ Access Time	-	80	-	100	-	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	-	35	-	40	-	50	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	30	-	30	-	30	-	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns	
t_{WLZ}	Output Active from End of Write	0	-	0	-	0	-	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	-	0	-	0	-	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	-	10	-	10	-	ns	
t_{RCS}	Read Command Set-Up Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time	0	-	0	-	0	-	ns	
t_{CSS}	Chip Select Set-Up Time	0	-	0	-	0	-	ns	
t_{CSH}	Chip Select Hold Time	20	-	25	-	30	-	ns	
t_{WP}	Write Pulse Width	60	-	70	-	85	-	ns	
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	60	10,000	70	10,000	85	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	30	-	35	-	45	-	ns	10
t_{DSC}	Data Set-Up Time from $\overline{CE}$	30	-	35	-	45	-	ns	10
t_{DHW}	Data Hold Time from R/W	0	-	0	-	0	-	ns	10
t_{DHC}	Data Hold Time from $\overline{CE}$	0	-	0	-	0	-	ns	10
t_{ASC}	Address Set-Up Time	0	-	0	-	0	-	ns	11
t_{AHC}	Address Hold Time	20	-	25	-	30	-	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	-	15	-	15	-	ns	
t_{FC}	Auto Refresh Cycle Time	130	-	160	-	190	-	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from $\overline{CE}$	40	-	50	-	60	-	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	-	30	-	30	-	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	-	8,000	-	8,000	-	ns	12
t_{FRS}	$\overline{CE}$ Delay Time from $\overline{RFSH}$ (Self Refresh)	160	-	190	-	225	-	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	-	8	-	8	-	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

NOTES:

1) Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO} depends on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100μs with high $\overline{CE}$ is required after power-up, before proper device operation is achieved.
6) AC measurements assume $t_T = 5ns$.
7) Timing reference level

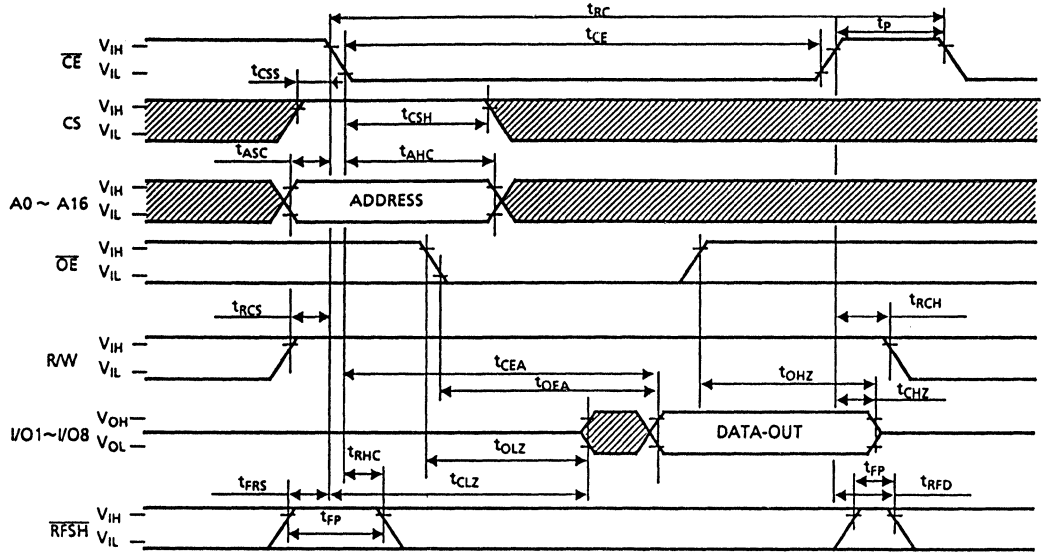
Input Level	:	V_{IH} = 2.6V
		V_{IL} = 0.6V
Input Reference Level	:	V_{IH} = 2.4V
		V_{IL} = 0.8V
Output Reference Level	:	V_{OH} = 2.2V
		V_{OL} = 0.8V



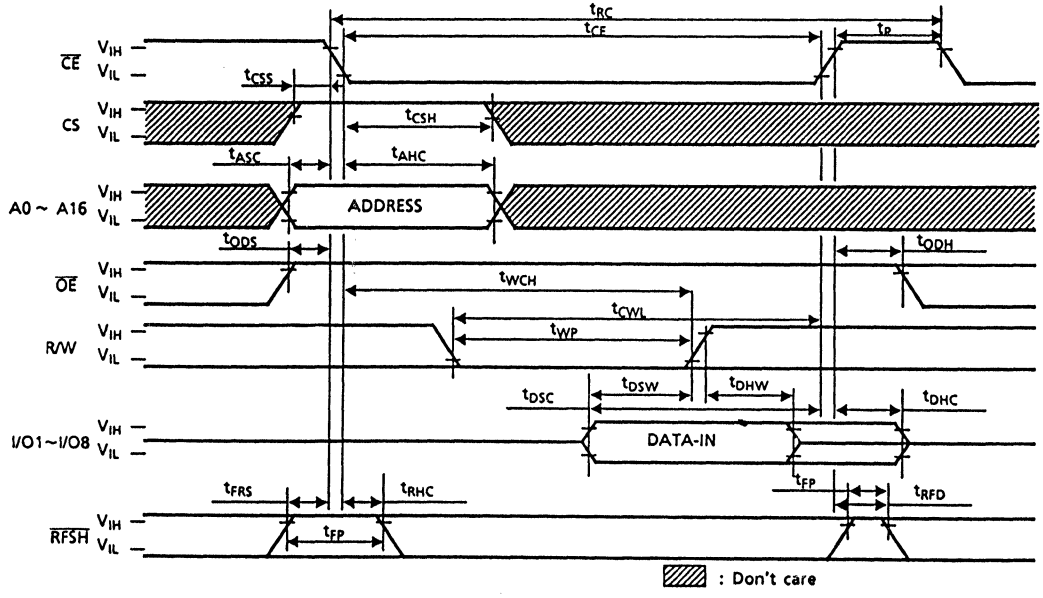
8) Measured with a load equivalent to 2 TTL loads and 100pF.
9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE}$ = V_{IH}.
    Auto refresh: $\overline{RFSH}$ pulse width $\leqq t_{FAP}$ (max.)
    Self refresh: $\overline{RFSH}$ pulse width $\geqq t_{FAS}$ (min.)
    The timing parameter (t_{FRS}) must be kept for proper device operation in the following conditions.
    - after self refresh
    - in case of "$\overline{RFSH}$" = "L" after power-up

TIMING WAVEFORMS

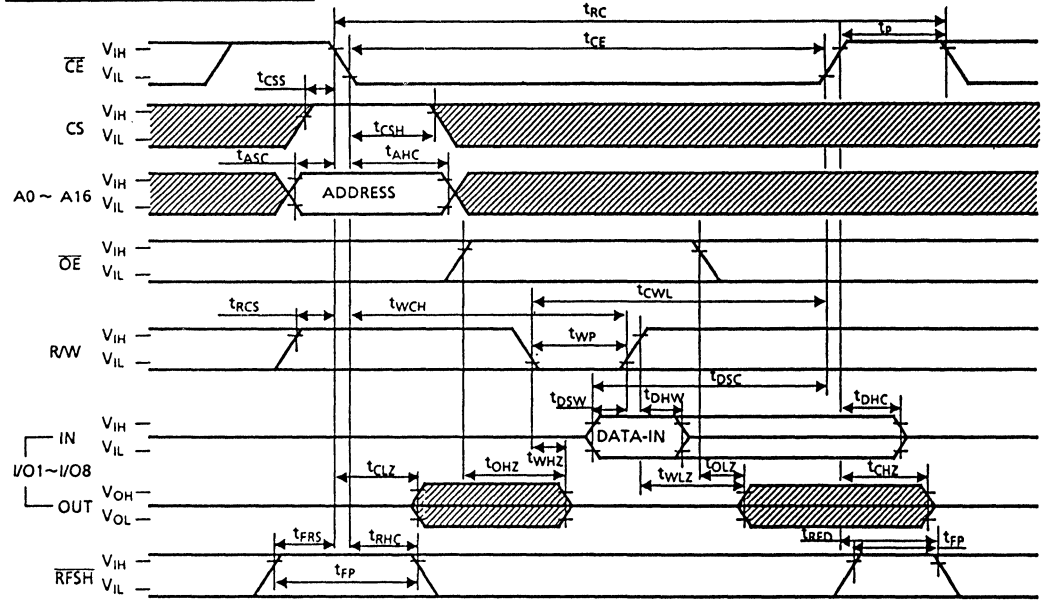
READ CYCLE



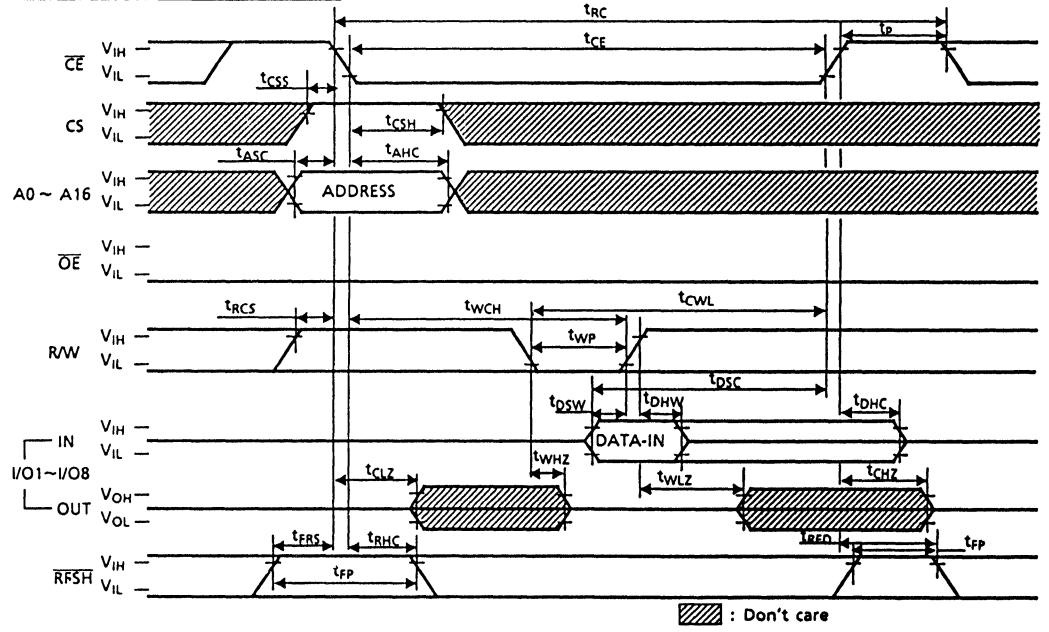
WRITE CYCLE-1 ($\overline{OE}$ Fix High)



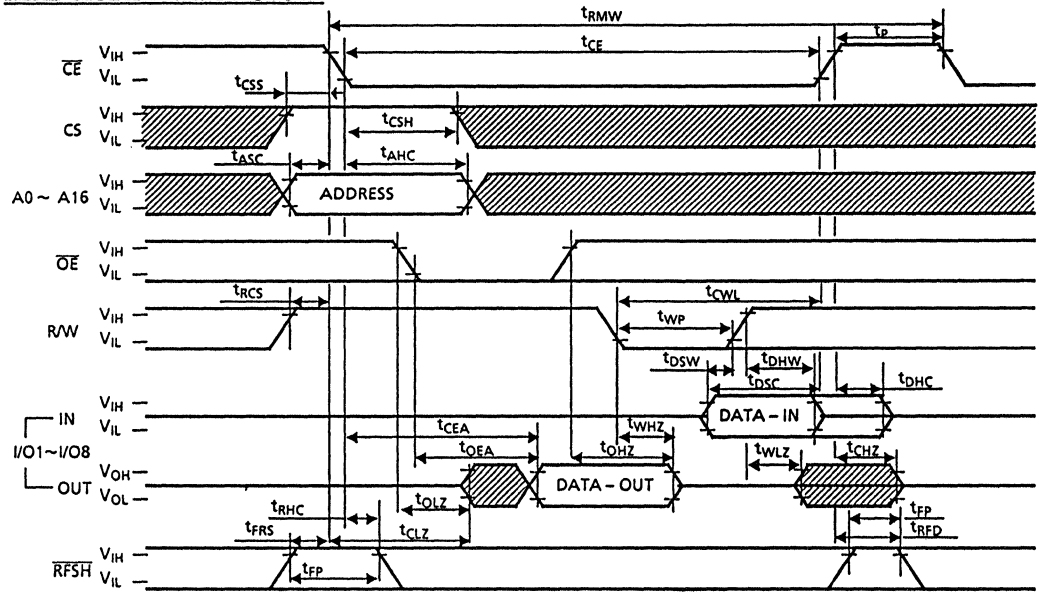
WRITE CYCLE - 2 ($\overline{OE}$ Clock)



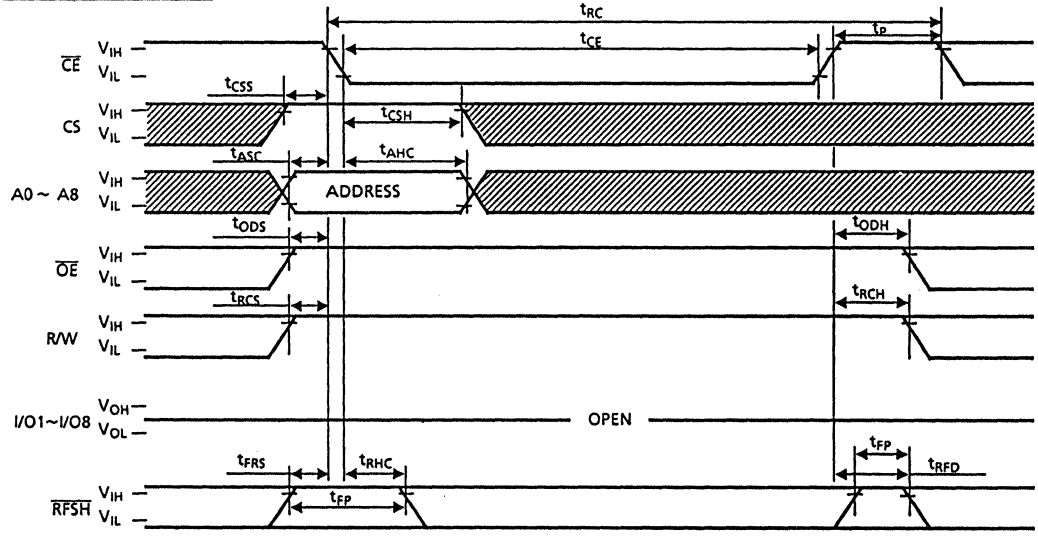
WRITE CYCLE - 3 ($\overline{OE}$ Fix Low)



READ MODIFY WRITE CYCLE

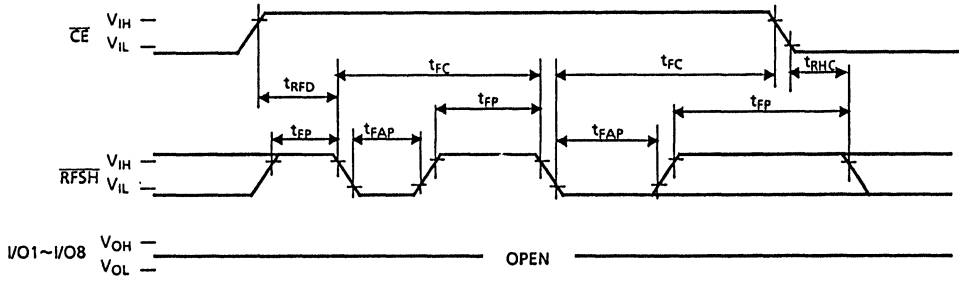


CE ONLY REFRESH



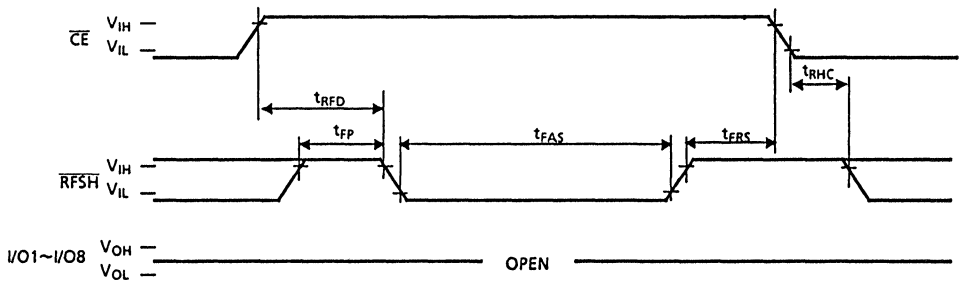
NOTE : A9 ~ A16 = Don't care, ▨ : Don't care

$\overline{RFSH}$ AUTO REFRESH



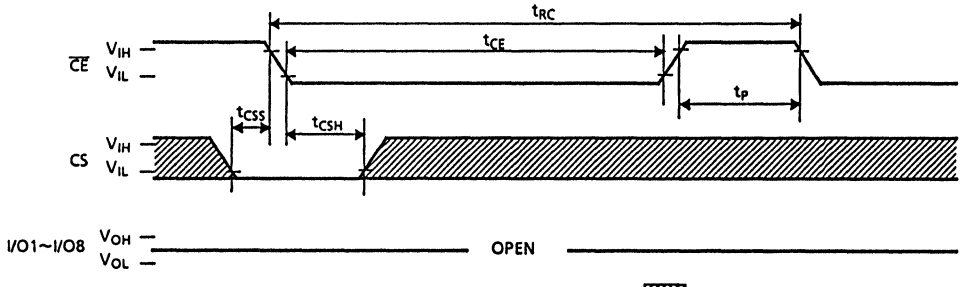
NOTE : CS, $\overline{OE}$, R/W, A0 ~ A16 = Don't care

SELF REFRESH



NOTE : CS, $\overline{OE}$, R/W, A0 ~ A16 = Don't care

CS STANDBY MODE



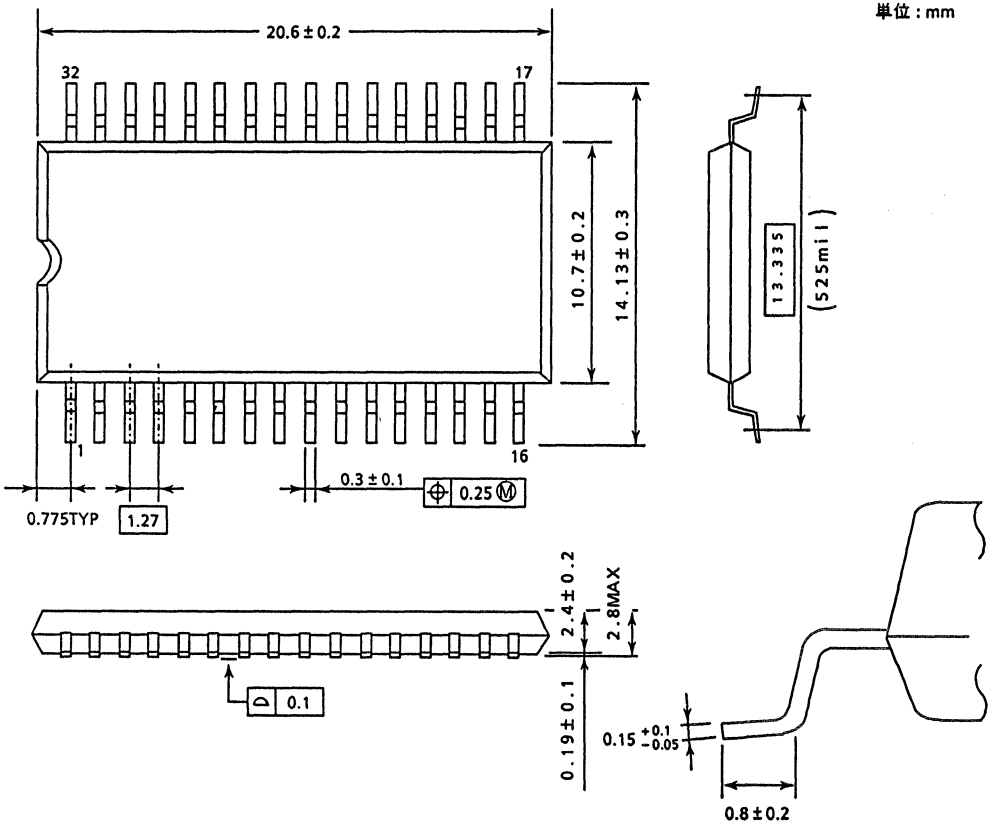
NOTE : $\overline{OE}$, R/W, A0 ~ A16 = Don't care

: Don't care

OUTLINE DRAWINGS

(SOP32-P-525)

単位 : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

131,072 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC518129A-LV Family is a 1M bit high-speed CMOS Pseudo-Static RAM organized as 131,072 words by 8 bits. The TC518129A-LV Family utilizes one transistor dynamic memory cell array with CMOS peripheral circuitry to achieve large capacity, high speed accesses, and low power requirements, using a single 5V power supply. The TC518129A-LV Family offers 3V data retention capability for battery back-up applications. The $\overline{RFSH}$ input allows two types of refresh operations: Auto Refresh and Self Refresh. The TC518129A-LV Family has a static RAM-like read/write functionality, which allows easy interfacing to a microprocessor. The TC518129AFWL-LV Family is pin-compatable with the 1M bit static RAM. The TC518129AFWL-LV is offered in a standard 28 pin 0.525 inch width small out-line plastic flat package.

FEATURES

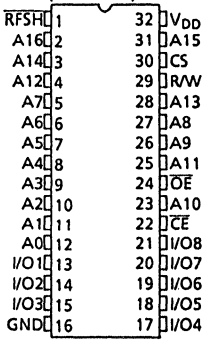
- Organization: 1M bit (131,072 word × 8bit)
- Fast Access Time and Low Power Dissipation

		TC518129AFWL Family		
		-80	-10	-12
t_{CEA} $\overline{CE}$ Access Time		80ns	100ns	120ns
t_{OEA} $\overline{OE}$ Access Time		35ns	40ns	50ns
t_{RC} Cycle Time		130ns	160ns	190ns
Power Dissipation		385mW	330mW	275mW
Self Refresh Current	5.5V	200μA		
	3.0V	100μA		

- Single Power Supply: 5V±10%
- Data Retention Supply Voltage: 3.0V ~ 5.5V
- Auto refresh uses an internal counter.
- Self refresh uses an internal timer.
- All inputs and outputs : TTL compatible
- CS standby cycle is capable
- 512 refresh cycle/8ms
- Logic Compatible: SRAM R/W Pin
- 32 Pin Standard Plastic PKG
  525mil SOP

PIN CONNECTION

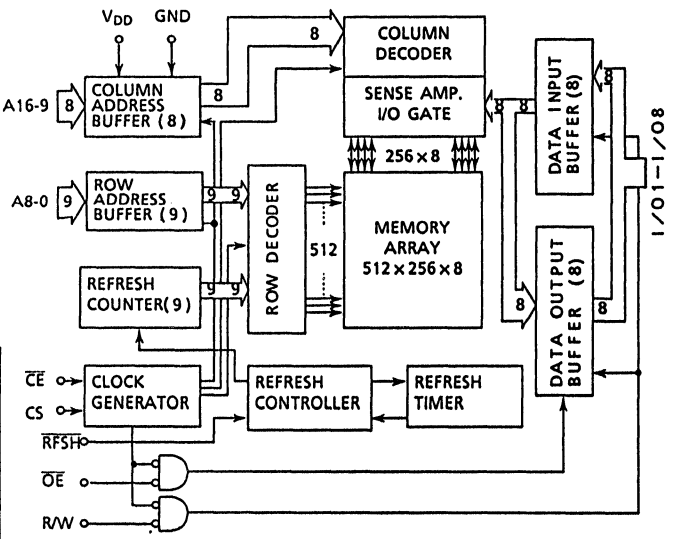
(TOP VIEW)



PIN NAMES

A0 ~ A16	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{RFSH}$	Refresh Input
$\overline{CE}$	Chip Enable Input
CS	Chip select Input
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



FUNCTION LOGIC

$\overline{CE}$	CS	$\overline{OE}$	R/W	$\overline{RFSH}$	A0 ~ A16	I/O1 ~ 8	CONDITION
↓	H	L	H	H	V*	OUT	Read
↓	H	*	L	H	V*	IN	Write
↓	H	H	H	H	V*	HZ	$\overline{CE}$ only Refresh
L	L	*	*	*	*	HZ	CS standby
H	*	*	*	L	*	HZ	Auto/Self Refresh
H	*	*	*	H	*	HZ	Stand by

H ··· High Level Input (V_{IN} = 6.5V ~ V_{IH} min.)
L ··· Low Level Input (V_{IN} = V_{IL} max. ~ −1.0V)
* ··· Don't care (6.5V ~ −1.0V)
V* ··· At $\overline{CE}$ falling edge, all address inputs are " IN ", and at the other condition, the address input are " * ".
HZ ··· High Impedance

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTE
V_{IN}	Input Voltage	− 1.0~7.0	V	1
V_{OUT}	Output Voltage	− 1.0~7.0	V	
V_{DD}	Power Supply Voltage	− 1.0~7.0	V	
T_{OPR}	Operating Temperature	0~70	°C	
T_{STG}	Storage Temperature	− 55~150	°C	
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

D.C. RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT.	NOTE
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	−	6.5	V	
V_{IL}	Input Low Voltage	− 1.0	−	0.8	V	

D.C. ELECTRICAL CHARACTERISTICS (V_{DD} = 5V ± 10%, Ta = 0~70°C)

SYMBOL	PARAMETER	PERIOD	MIN.	TYP.	MAX.	UNITS	NOTE
I_{DDO}	Operating Current (Average Power Supply Operating Current) $\overline{CE}$, Address cycling: t_{RC} = t_{RC} min.	130ns	–	50	70	mA	3, 4
		160ns	–	40	60		
		190ns	–	35	50		
I_{DDS1}	Standby Current $\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IH}		–	–	1	mA	
I_{DDS2}	Standby Current $\overline{CE}$ = V_{DD} – 0.2V, $\overline{RFSH}$ = V_{DD} – 0.2V		–	100	200	µA	
I_{DDF1}	Self Refresh Current $\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IL}		–	–	1	mA	
I_{DDF2}	Self Refresh Current $\overline{CE}$ = V_{DD} – 0.2V, $\overline{RFSH}$ = 0.2V		–	100	200	µA	
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ V_{DD}, All other Inputs not under test = 0V		– 10	–	10	µA	
$I_{O(L)}$	Output Leakage Current Output Disable ($\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or R/W = V_{IL}), 0V ≤ V_{OUT} ≤ V_{DD}		– 10	–	10	µA	
V_{OH}	Output High Level I_{OH} = – 5mA		2.4	–	–	V	
V_{OL}	Output Low Level I_{OL} = 4.2mA		–	–	0.4	V	

CAPACITANCE (V_{DD} = 5V, f = 1MHz, Ta = 25°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0 ~ A16)	–	5	pF
C_{I2}	Input Capacitance ($\overline{CE}$, CS, $\overline{OE}$, R/W, $\overline{RFSH}$)	–	7	pF
C_{IO}	Input/Output Capacitance	–	7	pF

Note) This parameter is periodically sampled and is not 100% tested.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

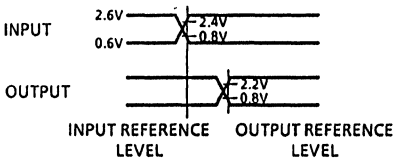
(V_{DD} = 5V ± 10%, Ta = 0~70 °C) (NOTES: 5, 6, 7, 8)

SYMBOL	PARAMETER	-80		-10		-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read, Write Cycle Time	130	–	160	–	190	–	ns	
t_{RMW}	Read Modify Write Cycle Time	195	–	235	–	280	–	ns	
t_{CE}	$\overline{CE}$ Pulse Width	80	10,000	100	10,000	120	10,000	ns	
t_P	$\overline{CE}$ Precharge Time	40	–	50	–	60	–	ns	
t_{CEA}	$\overline{CE}$ Access Time	–	80	–	100	–	120	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	35	–	40	–	50	ns	
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	30	–	30	–	30	–	ns	
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	0	–	ns	
t_{WLZ}	Output Active from End of Write	0	–	0	–	0	–	ns	
t_{CHZ}	Chip Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{OHZ}	$\overline{OE}$ Disable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{WHZ}	Write Enable to Output in High-Z	0	25	0	30	0	35	ns	9
t_{ODS}	$\overline{OE}$ Output Disable Set-Up Time	0	–	0	–	0	–	ns	
t_{ODH}	$\overline{OE}$ Output Disable Hold Time	10	–	10	–	10	–	ns	
t_{RCS}	Read Command Set-Up Time	0	–	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	
t_{CSS}	Chip Select Set-Up Time	0	–	0	–	0	–	ns	
t_{CSH}	Chip Select Hold Time	20	–	25	–	30	–	ns	
t_{WP}	Write Pulse Width	60	–	70	–	85	–	ns	
t_{WCH}	Write Command Hold Time	60	10,000	70	10,000	85	10,000	ns	
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	60	10,000	70	10,000	85	10,000	ns	
t_{DSW}	Data Set-Up Time from R/W	30	–	35	–	45	–	ns	10
t_{DSC}	Data Set-Up Time from $\overline{CE}$	30	–	35	–	45	–	ns	10
t_{DHW}	Data Hold Time from R/W	0	–	0	–	0	–	ns	10
t_{DHC}	Data Hold Time from $\overline{CE}$	0	–	0	–	0	–	ns	10
t_{ASC}	Address Set-Up Time	0	–	0	–	0	–	ns	11
t_{AHC}	Address Hold Time	20	–	25	–	30	–	ns	11
t_{RHC}	$\overline{RFSH}$ Command Hold Time	15	–	15	–	15	–	ns	
t_{FC}	Auto Refresh Cycle Time	130	–	160	–	190	–	ns	
t_{RFD}	$\overline{RFSH}$ Delay Time from $\overline{CE}$	40	–	50	–	60	–	ns	
t_{FAP}	$\overline{RFSH}$ Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	ns	12
t_{FP}	$\overline{RFSH}$ Precharge Time	30	–	30	–	30	–	ns	12
t_{FAS}	$\overline{RFSH}$ Pulse Width (Self Refresh)	8,000	–	8,000	–	8,000	–	ns	12
t_{FRS}	$\overline{CE}$ Delay Time from $\overline{RFSH}$ (Self Refresh)	160	–	190	–	225	–	ns	12
t_{REF}	Refresh Period (512 cycle, A0~A8)	–	8	–	8	–	8	ms	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

NOTES:

1) Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2) All voltage are referenced to GND.
3) I_{DDO} depends on cycle rate.
4) I_{DDO} depends on output loading. Specified values are obtained with the output open.
5) An initial pause of 100μs with high $\overline{CE}$ is required after power-up, before proper device operation is achieved.
6) AC measurements assume $t_T = 5ns$.
7) Timing reference level

Input Level	:	$V_{IH} = 2.6V$
		$V_{IL} = 0.6V$
Input Reference Level	:	$V_{IH} = 2.4V$
		$V_{IL} = 0.8V$
Output Reference Level	:	$V_{OH} = 2.2V$
		$V_{OL} = 0.8V$

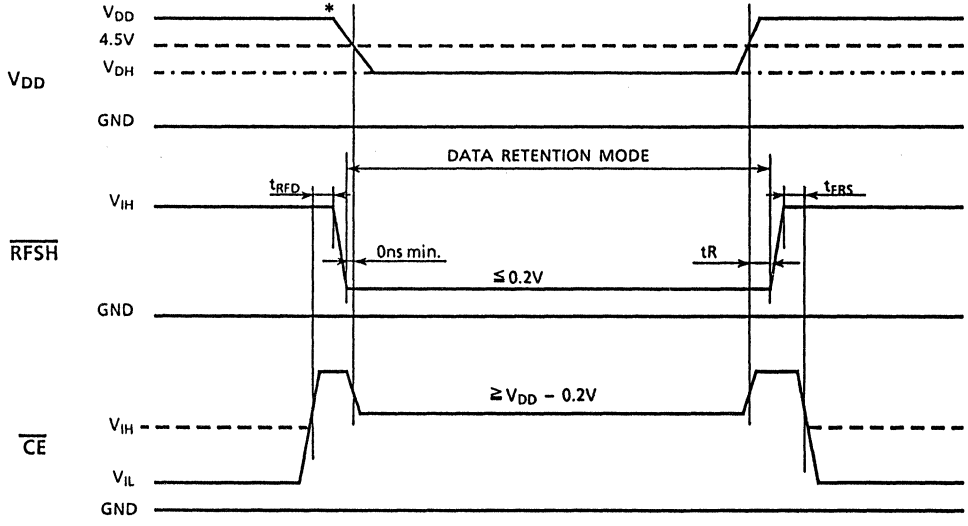


8) Measured with a load equivalent to 2 TTL loads and 100pF.
9) t_{CHZ}, t_{OHZ}, t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10) In write cycles, the input data is latched at the earlier of R/W or $\overline{CE}$ rising edge. Therefore the input data must be valid during set-up time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
11) All address inputs are latched at the falling edge of $\overline{CE}$. Therefore all address inputs must be valid during t_{ASC} and t_{AHC}.
12) Two refresh operation - auto refresh and self refresh are defined by the $\overline{RFSH}$ pulse width under the condition of $\overline{CE} = V_{IH}$.
    Auto refresh: $\overline{RFSH}$ pulse width $\leqq t_{FAP}$ (max.)
    Self refresh: $\overline{RFSH}$ pulse width $\geqq t_{FAS}$ (min.)
    The timing parameter (t_{FRS}) must be kept for proper device operation in the following conditions.
    - after self refresh
    - in case of "$\overline{RFSH}$" = "L" after power-up

DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		3.0	-	5.5	V
I_{DDF2}	Self Refresh Current	V_{DH} = 3.0V	-	40	100	μA
		V_{DH} = 5.5V	-	100	200	μA
t_R	Recovery Time		5	-	-	mS

*The falling slope of V_{DD} must be more than 50ms in order to operate the device safely. (20ms/V)



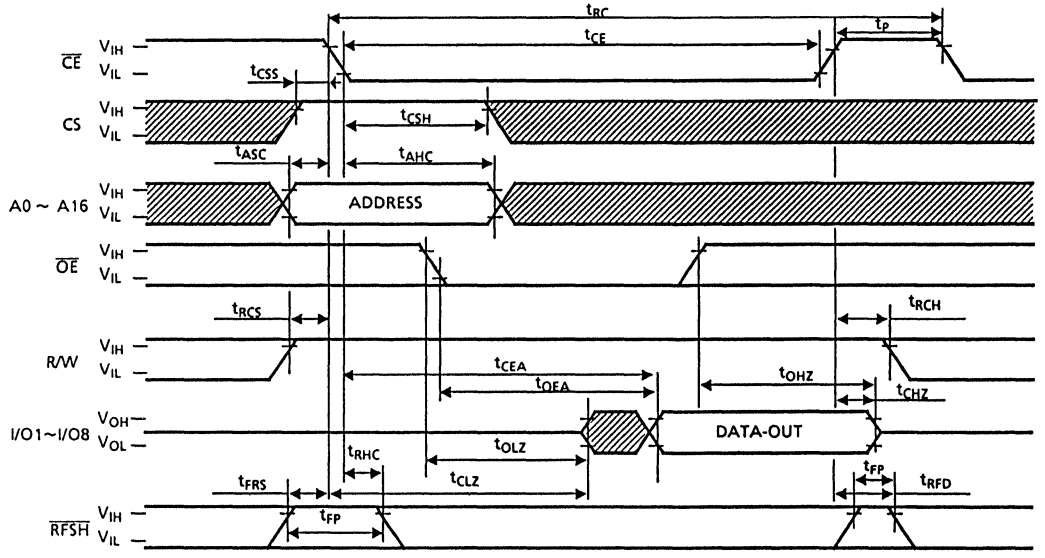
(Note) ∘ CS, $\overline{OE}$, R/W, A0~A16 = Don't care

∘ I_{DDF1} is applied in $\overline{RFSH} = V_{IL\ max.}$, $\overline{CE} = V_{III\ min.}$

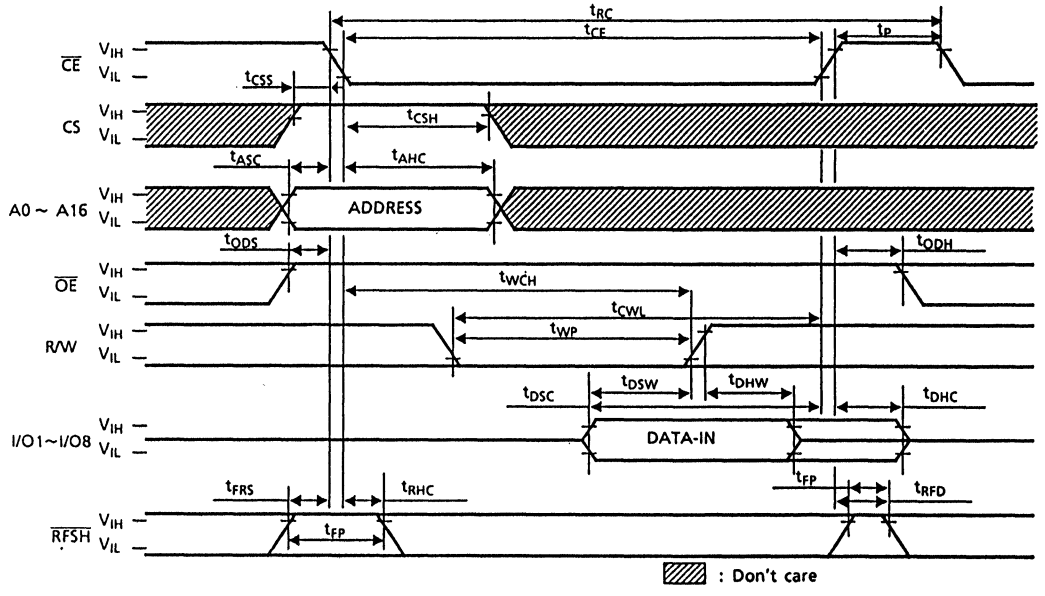
∘ At any state but Data Retention Mode, Auto Refresh or CE Only Refresh with 512cycle/8ms is required.

TIMING WAVEFORMS

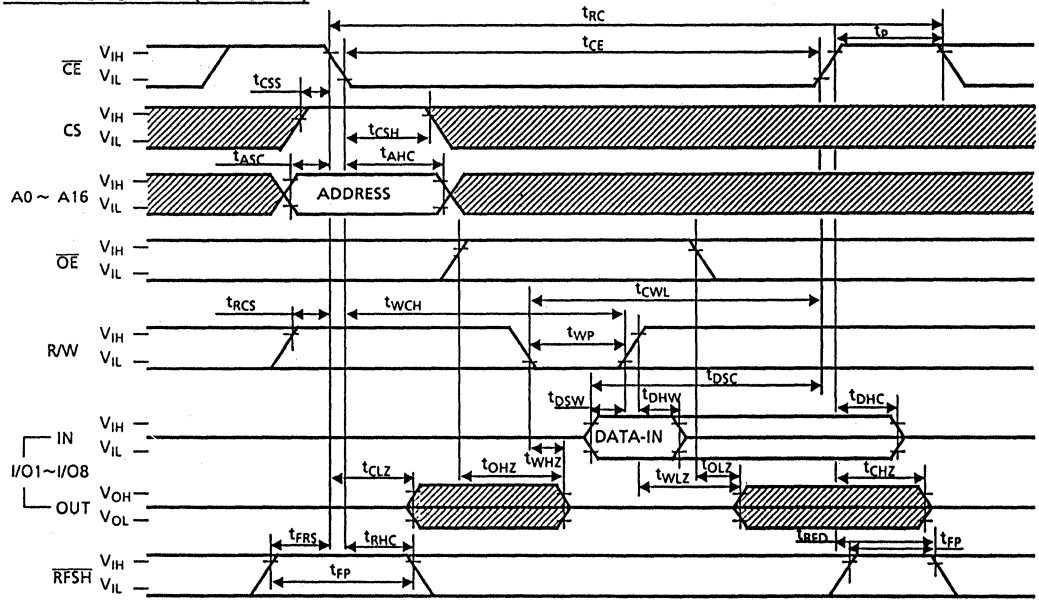
READ CYCLE



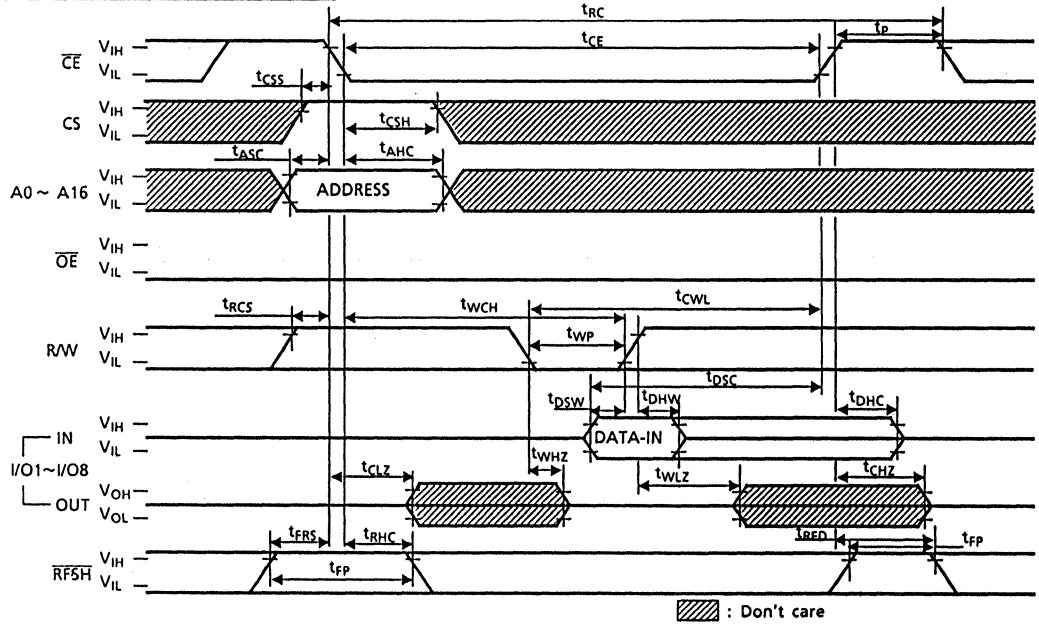
WRITE CYCLE-1 ($\overline{OE}$ Fix High)



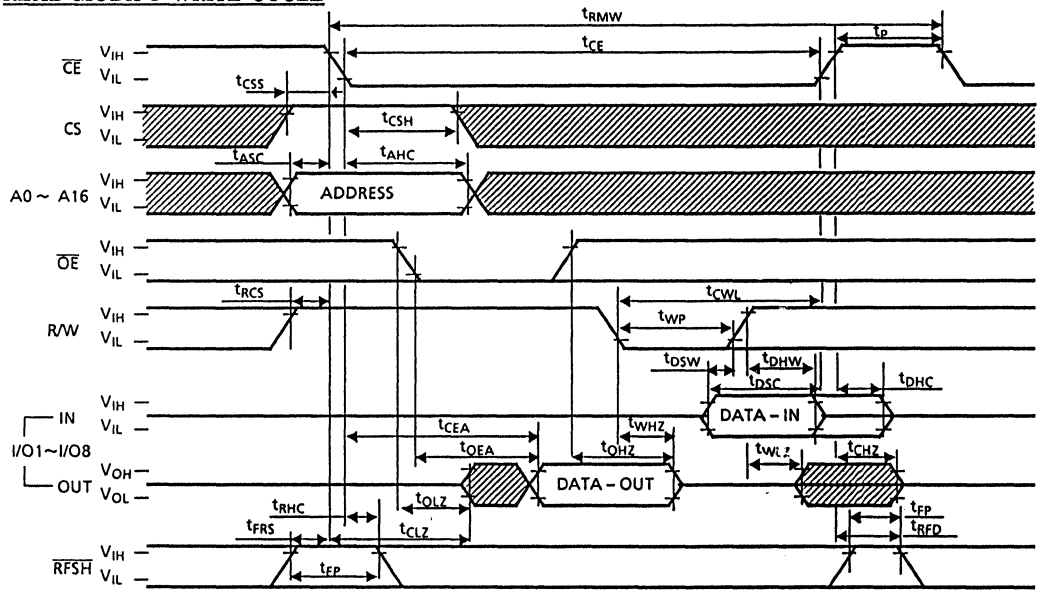
WRITE CYCLE - 2 ($\overline{OE}$ Clock)



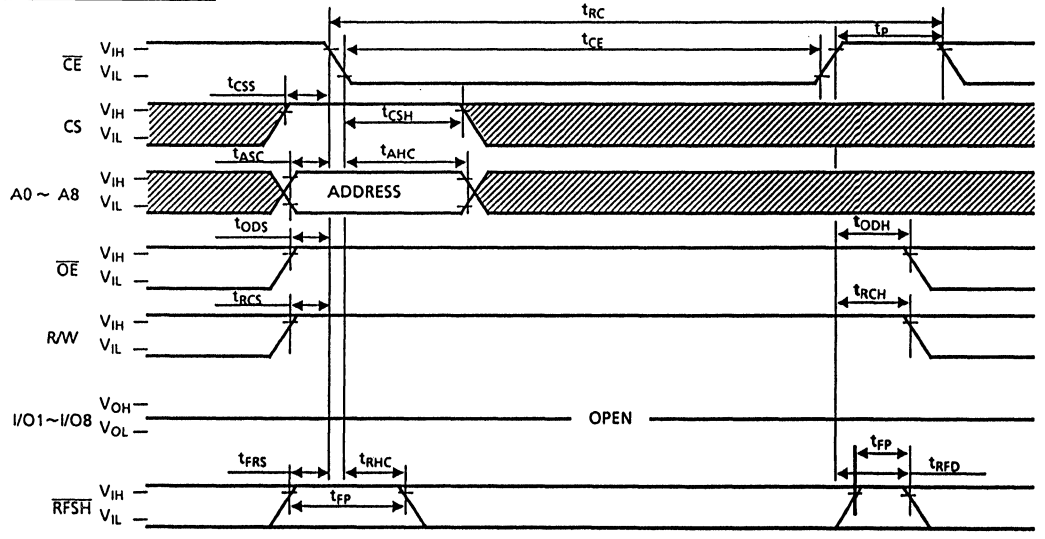
WRITE CYCLE - 3 ($\overline{OE}$ Fix Low)



READ MODIFY WRITE CYCLE

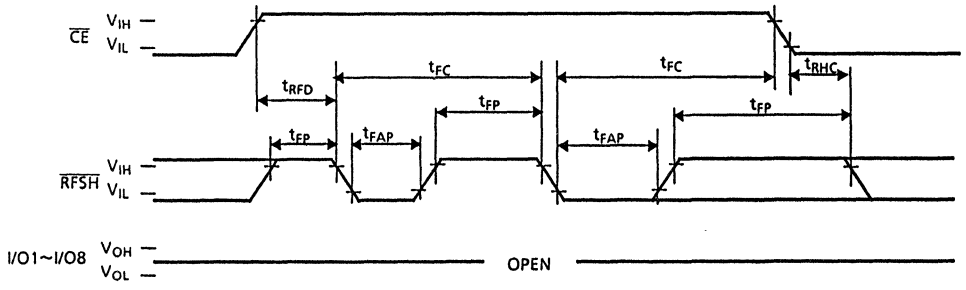


CE ONLY REFRESH



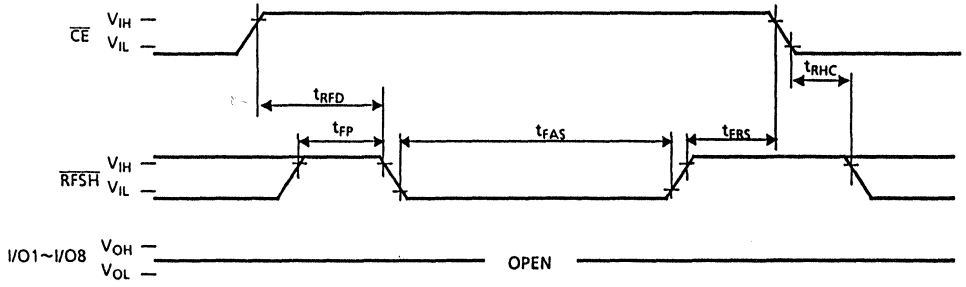
NOTE : A9 ~ A16 = Don't care, ▨ : Don't care

$\overline{RFSH}$ AUTO REFRESH



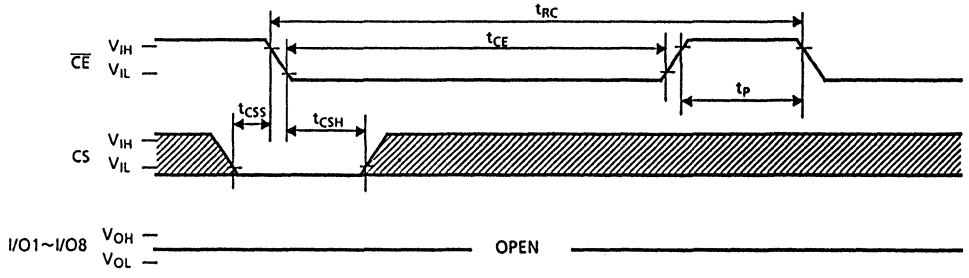
NOTE : CS, $\overline{OE}$, R/W, A0 ~ A16 = Don't care

SELF REFRESH



NOTE : CS, $\overline{OE}$, R/W, A0 ~ A16 = Don't care

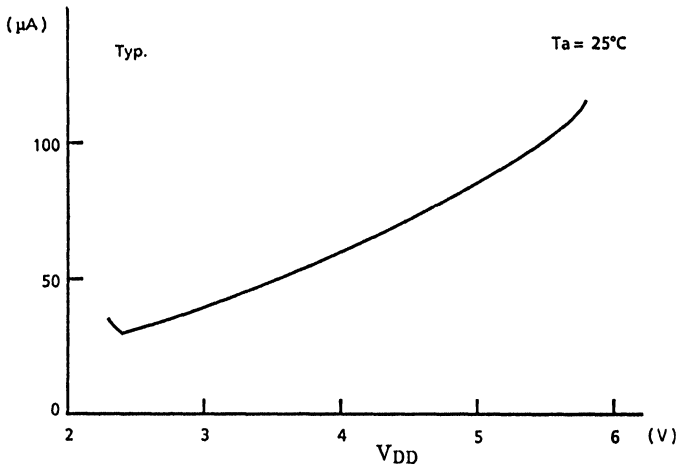
CS STANDBY MODE



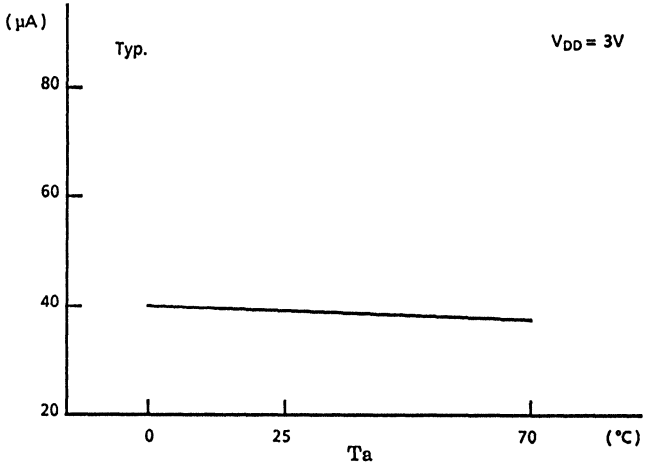
NOTE : $\overline{OE}$, R/W, A0 ~ A16 = Don't care

: Don't care

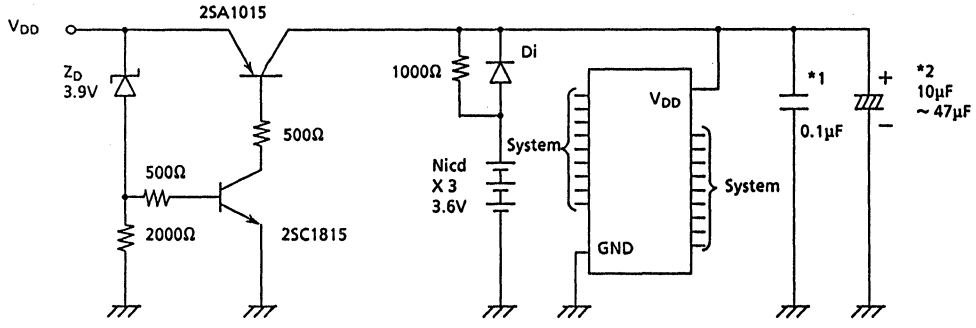
I_{DDF2} V_{DD} Characteristics



I_{DDF2} Temp. Characteristics



Battery Back Up applicable example



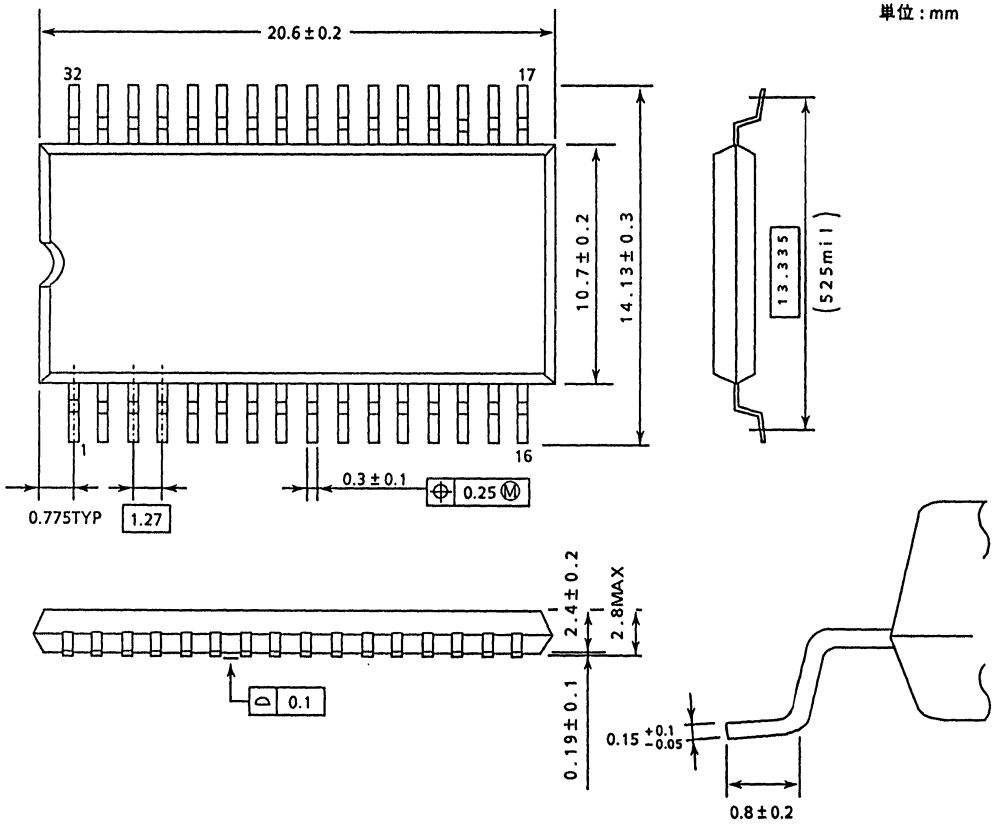
*1 : Ceramic condenser
*2 : Tantalum condenser
(The large Bypass condenser is preferable, as the noise is absorbed when the power supply is switched.)

This circuit does not have memory protection. Therefore, rapid turn off of the power supply must be avoided. Enter the Self Refresh Mode before changing to Battery Back Up Power Supply.

OUTLINE DRAWINGS

(SOP32-P-525)

単位：mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

524,288 WORDS × 8 BIT CMOS PSEUDO STATIC RAM

PRELIMINARY

DESCRIPTION

The TC518512 Family is a 4M bit high-speed CMOS Pseudo-Static RAM organized as 524,288 words by 8 bits. The TC518512 Family utilizes one transistor dynamic memory cell array with CMOS peripheral circuitry to achieve large capacity, high speed accesses, and low power requirements, using a single 5V power supply. The $\overline{RFSH}$ input allows two types of refresh operations: Auto Refresh and Self Refresh. The TC518512 Family has a static RAM-like write functionality, which allows easy interfacing to a microprocessor. The TC518512 Family is pin-compatible with the 1M bit static RAM. The TC518512PL is offered in a standard 32 pin 0.6 inch width plastic DIP. The TC518512FL is offered in a standard 32 pin 0.525 inch width small out-line plastic flat package.

FEATURES

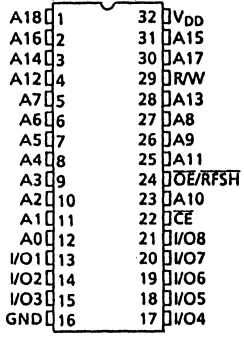
- Organization: 4M bit (524,288 word × 8bit)
- Fast Access Time and Low Power Dissipation

	TC518512PL Family	
	-80	-10
t_{CEA} $\overline{CE}$ Access Time	80ns	100ns
t_{OEA} $\overline{OE}$ Access Time	35ns	40ns
t_{RC} Cycle Time	130ns	160ns
Power Dissipation	385mW	330mW
Self Refresh Current	200μA	

- Single Power Supply: 5V±10%
- Auto refresh uses an internal counter.
- Self refresh uses an internal timer.
- All inputs and outputs : TTL compatible
- 2048 refresh cycle/32ms
- Logic Compatible: SRAM R/W Pin
- 32 Pin Standard Plastic PKG
  - PL : 600 mil DIP
  - FL : 525 mil SOP

PIN CONNECTION

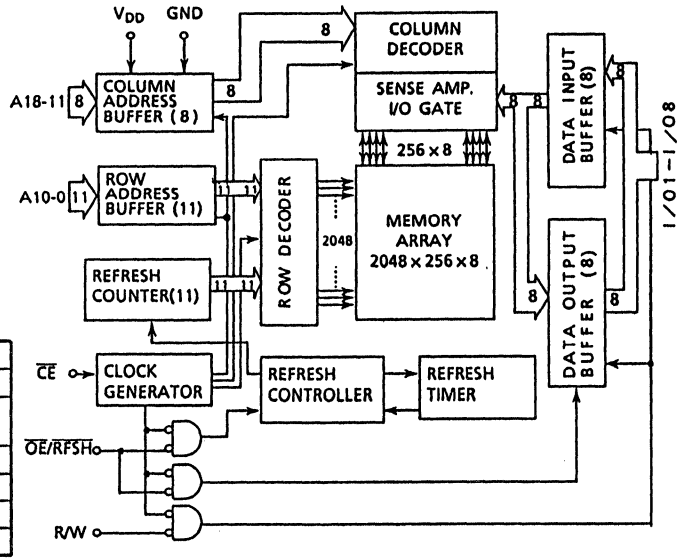
(TOP VIEW)



PIN NAMES

A0 ~ A18	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$/$\overline{RFSH}$	Output Enable Input Refresh Input
$\overline{CE}$	Chip Enable Inputs
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

BLOCK DIAGRAM



CMOS Static RAM

8,192 WORD X 8 BIT CMOS STATIC RAM

DESCRIPTION

The TC5563APL is a 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns.

When CE2 is a logical low or $\overline{CE1}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC5563APL has three control inputs. Two chip enables ($\overline{CE1}$, CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5563APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The TC5563APL also features pin compatibility with the 64K bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems. The TC5563APL is offered in a dual-in-line 28 pin standard 300 mil plastic package.

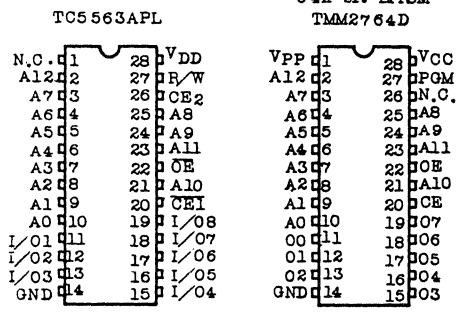
FEATURES

- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current: 100μA(Max.) Ta=70°C
- Access Time
  TC5563APL-10: 100ns(Max.)
  TC5563APL-12: 120ns(Max.)
  TC5563APL-15: 150ns(Max.)
- 5V Single Power Supply
- Power Down Features: CE2, $\overline{CE1}$
- Fully Static Operation
- Data Retention Supply Voltage: 2.0 ∿ 5.5V
- Directly TTL Compatible: All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package type)

Package Type	Device Name
600 mil DIP	*TC5565APL
300 mil DIP (Slim Package)	TC5563APL
Flat Package (SOP)	*TC5565AFL

*: See TC5565APL/AFL Technical Data.

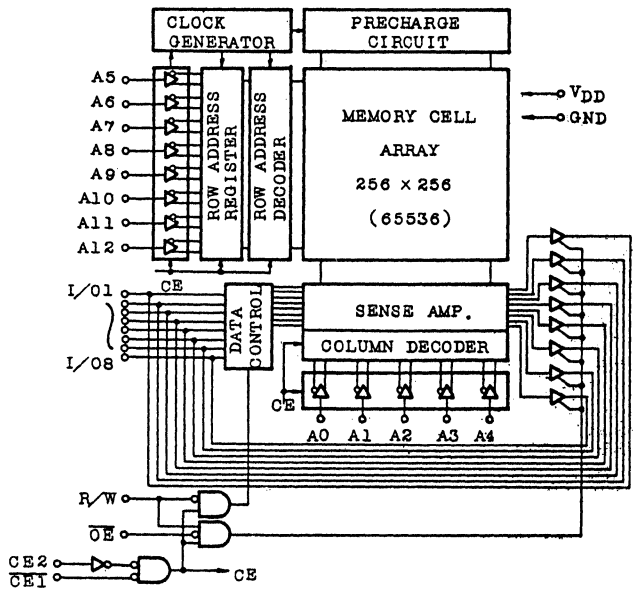
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A12	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ∿ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ∿ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ∿ 7.0	V
V_{IN}	Input Voltage	-0.3* ∿ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ∿ V_{DD}+0.5	V
P_D	Power Dissipation	0.8	W
T_{solder}	Soldering Temperature	260 • 10	°C • sec
T_{stg}	Storage Temperature	-55 ∿ 150	°C
T_{opr}	Operating Temperature	0 ∿ 70	°C

*: -3.0V at pulse width 50ns Max.

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	
V_{IL}	Input Low Voltage	-0.3*	-	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	

*: -3.0V at pulse width 50ns Max.

D.C. and OPERATING CHARACTERISTICS (Ta=0∿70°C, V_{DD}=5V±10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN}=0∿V_{DD}			-	-	±1.0	μA
I_{OH}	Output High Current	V_{OH}=2.4V			-1.0	-	-	mA
I_{OL}	Output Low Current	V_{OL}=0.4V			4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL} or R/$\overline{W}$=V_{IL} or $\overline{OE}$=V_{IH} V_{OUT}=0∿V_{DD}			-	-	±1.0	μA
I_{DDO1}	Operating Current	V_{DD}=5.5V $\overline{CE1}$=V_{IL} CE2=V_{IH} Other input=V_{IH}/V_{IL} I_{OUT}=0mA	t_{cycle}=1.0μs		-	-	10	mA
			TC5563APL-10	t_{cycle}=100ns	-	-	45	mA
			TC5563APL-12	t_{cycle}=120ns	-	-	40	mA
			TC5563APL-15	t_{cycle}=150ns	-	-	35	mA
I_{DDO2}		V_{DD}=5.5V $\overline{CE1}$=0.2V CE2=V_{DD}-0.2V Other input=V_{DD}-0.2V/0.2V I_{OUT}=0mA	t_{cycle}=1.0μs		-	-	5	mA
			TC5563APL-10	t_{cycle}=100ns	-	-	40	mA
			TC5563APL-12	t_{cycle}=120ns	-	-	35	mA
			TC5563APL-15	t_{cycle}=150ns	-	-	30	mA
I_{DDS1}	Standby Current	$\overline{CE1}$=V_{IH} or CE2=V_{IL}			-	-	3	mA
* I_{DDS2}	Standby Current	$\overline{CE1}$=V_{DD}-0.2V or CE2=0.2V		V_{DD}=5.5V	-	2	100	μA
				V_{DD}=3.0V	-	1	50	

*: In standby mode with $\overline{CE1} \geq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of CE2 ≥ V_{DD}-0.2V or CE2 ≤ 0.2V.

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC5563APL-10L		TC5563APL-12L		TC5563APL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	-	120	-	150	-	ns
t_{ACC}	Address Access Time	-	100	-	120	-	150	
t_{CO1}	$\overline{CE1}$ Access Time	-	100	-	120	-	150	
t_{CO2}	CE2 Access Time	-	100	-	120	-	150	
t_{OE}	Output Enable to Output Valid	-	50	-	60	-	70	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	-	10	-	15	-	
t_{OEE}	Output Enable to Output in Low-Z	5	-	5	-	5	-	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	-	35	-	40	-	50	
t_{ODO}	Output Enable to Output in High-Z	-	35	-	40	-	50	
t_{OH}	Output Data Hold Time	20	-	20	-	20	-	

WRITE CYCLE

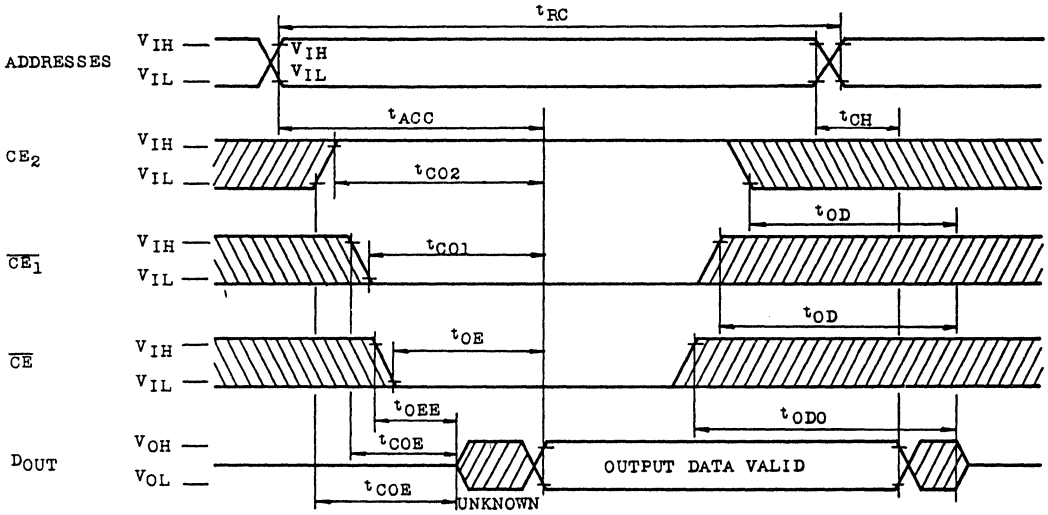
SYMBOL	PARAMETER	TC5563APL-10L		TC5563APL-12L		TC5563APL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	-	120	-	150	-	ns
t_{WP}	Write Pulse Width	60	-	70	-	90	-	
t_{CW}	Chip Selection to End of Write	80	-	85	-	100	-	
t_{AS}	Address Set up Time	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{ODW}	R/W to Output High-Z	-	35	-	40	-	50	
t_{OEW}	R/W to Output Low-Z	5	-	5	-	10	-	
t_{DS}	Data Set up Time	40	-	50	-	60	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

A.C. TEST CONDITION

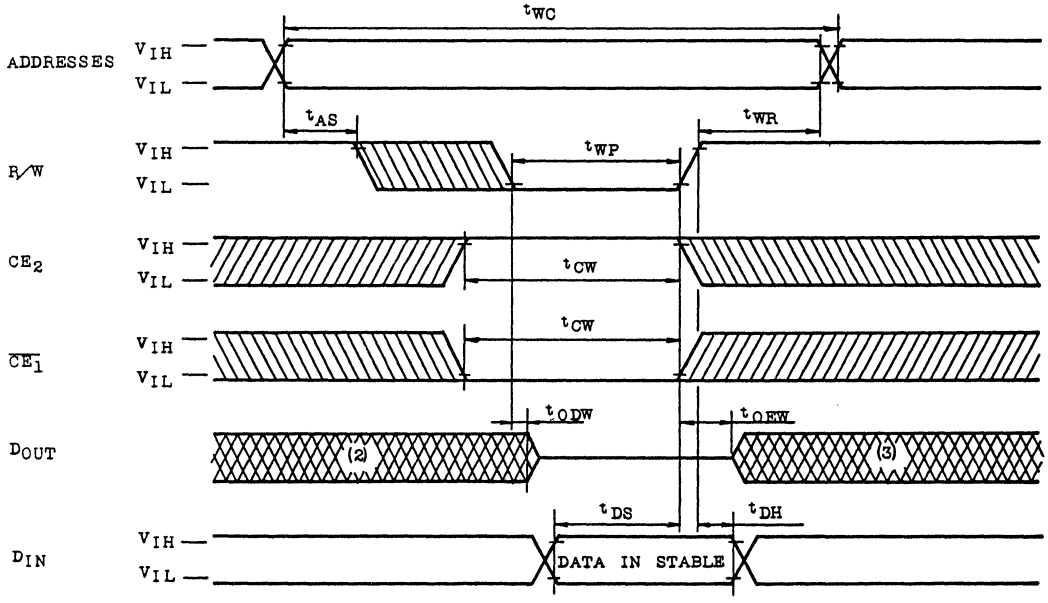
Output Load		: 100pF + 1 TTL Gate
Input Pulse Level		: 0.6V, 2.4V
Timing Measurement	V_{IN}	: 0.8V, 2.2V
Reference Level	V_{OUT}	: 0.8V, 2.2V
t_r, t_f		: 5ns

TIMING WAVEFORMS

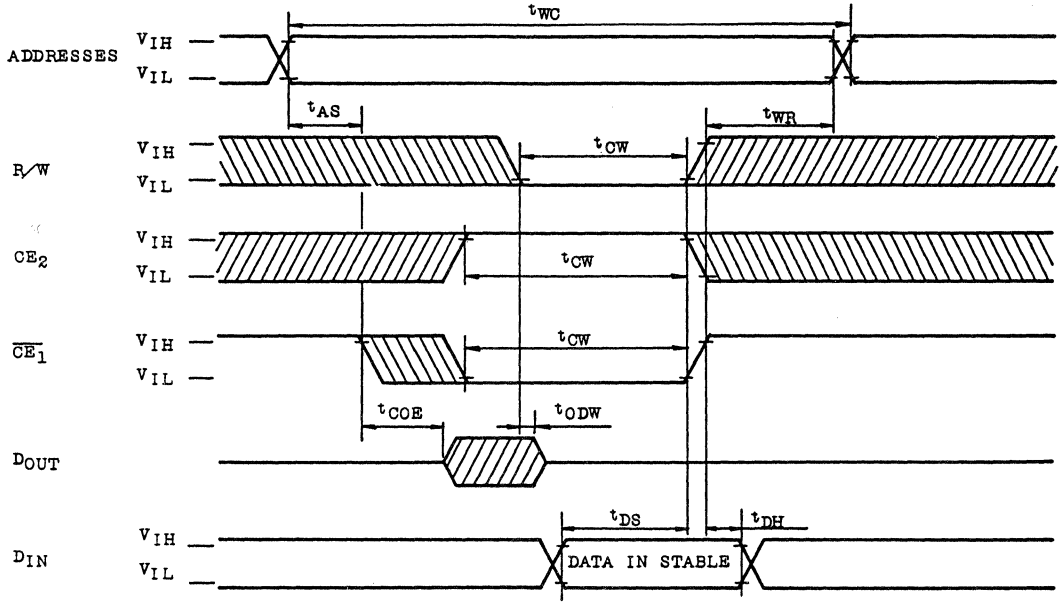
READ CYCLE (1)



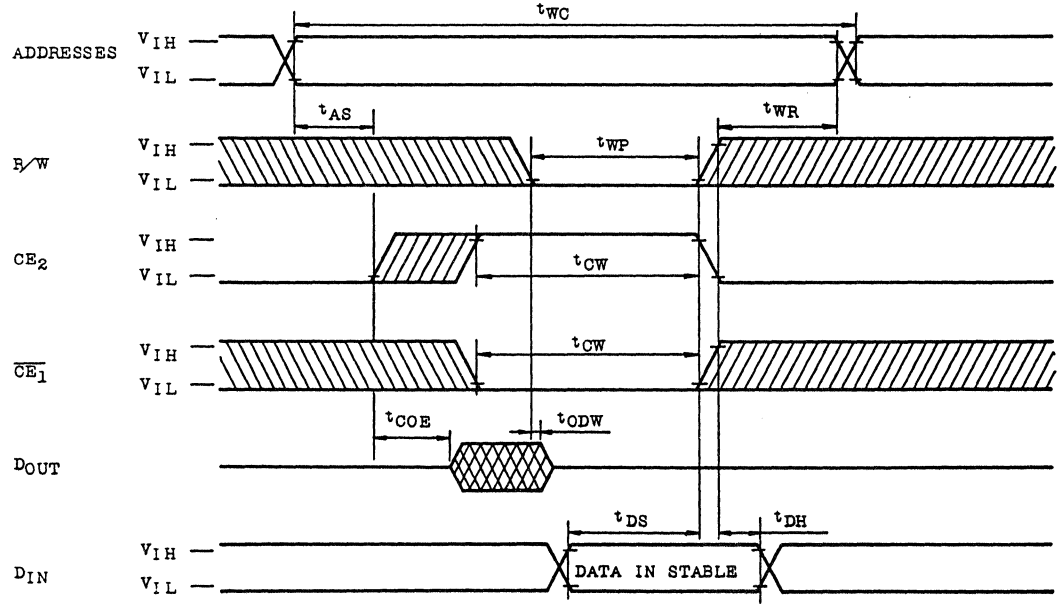
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



Note 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.

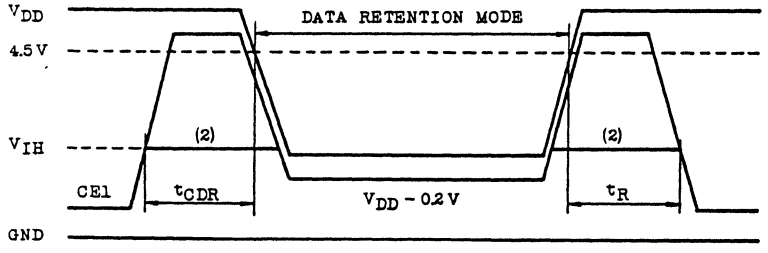
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0 ∿ 70°C)

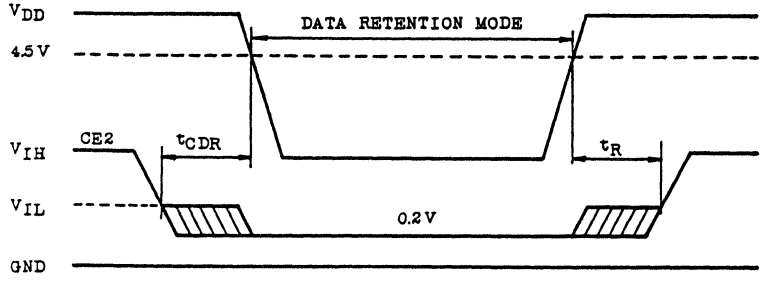
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	V_{DD}=3.0V	-	-	50	µA
		V_{DD}=5.5V	-	-	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	µs
t_R	Recovery Time		t_{RC}*	-	-	µs

*: Read cycle time.

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



Note 1: In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2V or CE2 ≧ V_{DD}-0.2V.

2: If the V_{IH} of $\overline{CE1}$ is 2.2V in active operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

3: In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2V.

DEVICE INFORMATION

The TC5563APL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.
This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.

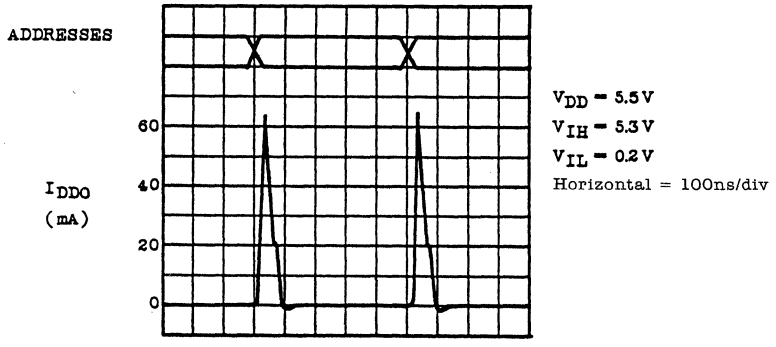
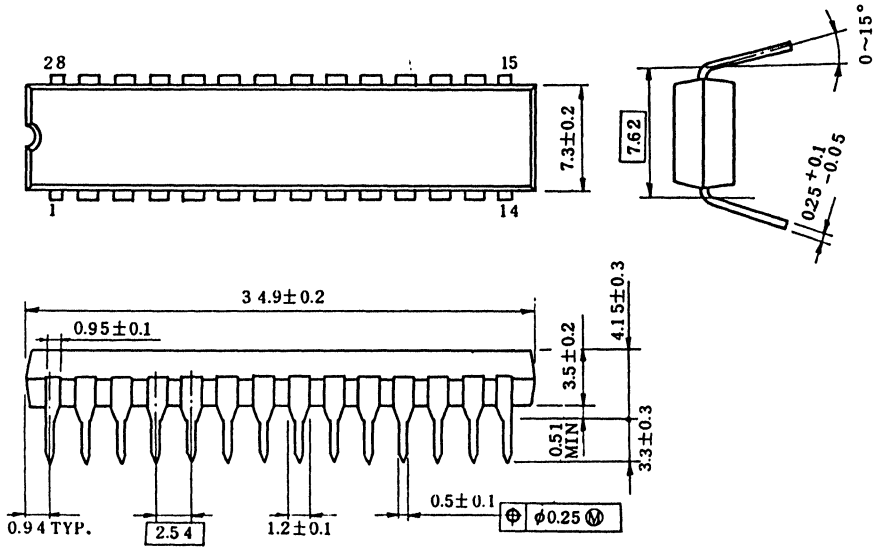


Fig. Typical Current Waveforms

OUTLINE DRAWINGS (DIP28-P-300B)

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

8,192 WORD X 8 BIT CMOS STATIC RAM

DESCRIPTION

The TC5563APL is a 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns.

When CE2 is a logical low or $\overline{CE1}$ is a logical high, the device is placed in low power standby mode in which standby current is 0.6μA typically. The TC5563APL has three control inputs. Two chip enables ($\overline{CE1}$, CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5563APL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The TC5563APL also features pin compatibility with the 64K bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems. The TC5563APL is offered in a dual-in-line 28 pin standard 300 mil plastic package.

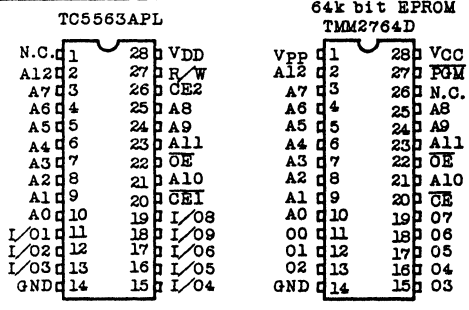
FEATURES

- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current: 1μA(Max.) Ta=25°C
- Access Time
  TC5563APL-10L: 100ns(Max.)
  TC5563APL-12L: 120ns(Max.)
  TC5563APL-15L: 150ns(Max.)
- 5V Single Power Supply
- Power Down Features: CE2, $\overline{CE1}$
- Fully Static Operation
- Data Retention Supply Voltage: 2.0 ∿ 5.5V
- Directly TTL Compatible: All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

Package Type	Device Name
600 mil DIP	*TC5565APL
300 mil DIP (Slim Package)	TC5563APL
Flat Package (SOP)	*TC5565AFL

*: See TC5565APL/AFL Technical Data.

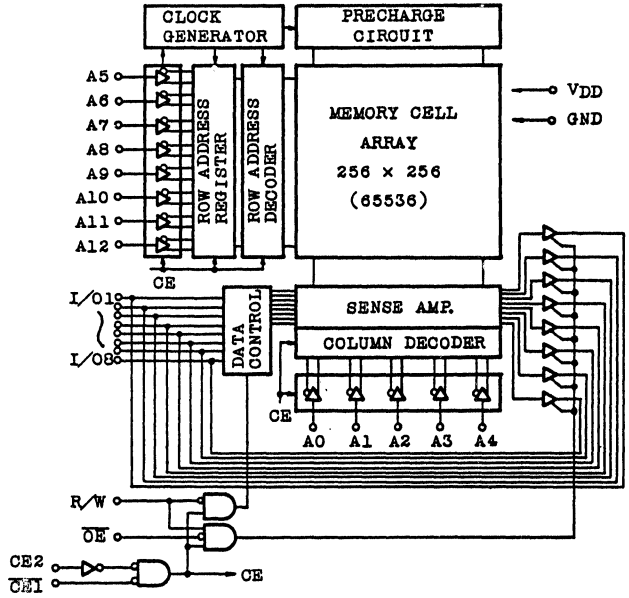
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A12	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ∿ I/O8	Data Inputs/Outputs
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ∿ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ∿ 7.0	V
V_{IN}	Input Voltage	-0.3* ∿ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ∿ V_{DD}+0.5	V
P_D	Power Dissipation	0.8	W
T_{solder}	Soldering Temperature	260 • 10	°C • sec
T_{stg}	Storage Temperature	-55 ∿ 150	°C
T_{opr}	Operating Temperature	0 ∿ 70	°C

*: -3.0V at pulse width 50ns Max.

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	
V_{IL}	Input Low Voltage	-0.3*	-	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	

*: -3.0V at pulse width 50ns Max.

D.C. and OPERATING CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$			-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$			-1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$			4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1}=V_{IH}$ or CE2=V_{IL} or R/W=V_{IL} or $\overline{OE}=V_{IH}$ $V_{OUT}=0 \sim V_{DD}$			-	-	±1.0	μA
I_{DDO1}	Operating Current	$V_{DD}=5.5V$ $\overline{CE1}=V_{IL}$ CE2=V_{IH} Other input= V_{IH}/V_{IL} $I_{OUT}=0mA$	$t_{cycle}=1.0\mu s$		-	-	10	mA
			TC5563APL-10L	t_{cycle} =100ns	-	-	45	mA
			TC5563APL-12L	t_{cycle} =120ns	-	-	40	mA
			TC5563APL-15L	t_{cycle} =150ns	-	-	35	mA
I_{DDO2}		$V_{DD}=5.5V$ $\overline{CE1}=0.2V$ CE2=$V_{DD}-0.2V$ Other input= $V_{DD}-0.2V/0.2V$ $I_{OUT}=0mA$	$t_{cycle}=1.0\mu s$		-	-	5	mA
			TC5563APL-10L	t_{cycle} =100ns	-	-	40	mA
			TC5563APL-12L	t_{cycle} =120ns	-	-	35	mA
			TC5563APL-15L	t_{cycle} =150ns	-	-	30	mA
I_{DDS1}	Standby Current	$\overline{CE1}=V_{IH}$ or CE2=V_{IL}			-	-	3	mA
* I_{DDS2}	Standby Current	$\overline{CE1}=V_{DD}-0.2V$ or CE2=0.2V		Ta=25°C	-	0.6	1.0	μA
				Ta=0 ∿ 70°C	-	-	30	

*: In standby mode with $\overline{CE1} \geq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $CE2 \geq V_{DD}-0.2V$ or $CE2 \leq 0.2V$.

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT}=GND$	10	

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC5563APL-10L		TC5563APL-12L		TC5563APL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	-	120	-	150	-	ns
t_{ACC}	Address Access Time	-	100	-	120	-	150	
t_{CO1}	$\overline{CE1}$ Access Time	-	100	-	120	-	150	
t_{CO2}	CE2 Access Time	-	100	-	120	-	150	
t_{OE}	Output Enable to Output Valid	-	50	-	60	-	70	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	-	10	-	15	-	
t_{OEE}	Output Enable to Output in Low-Z	5	-	5	-	5	-	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	-	35	-	40	-	50	
t_{ODO}	Output Enable to Output in High-Z	-	35	-	40	-	50	
t_{OH}	Output Data Hold Time	20	-	20	-	20	-	

WRITE CYCLE

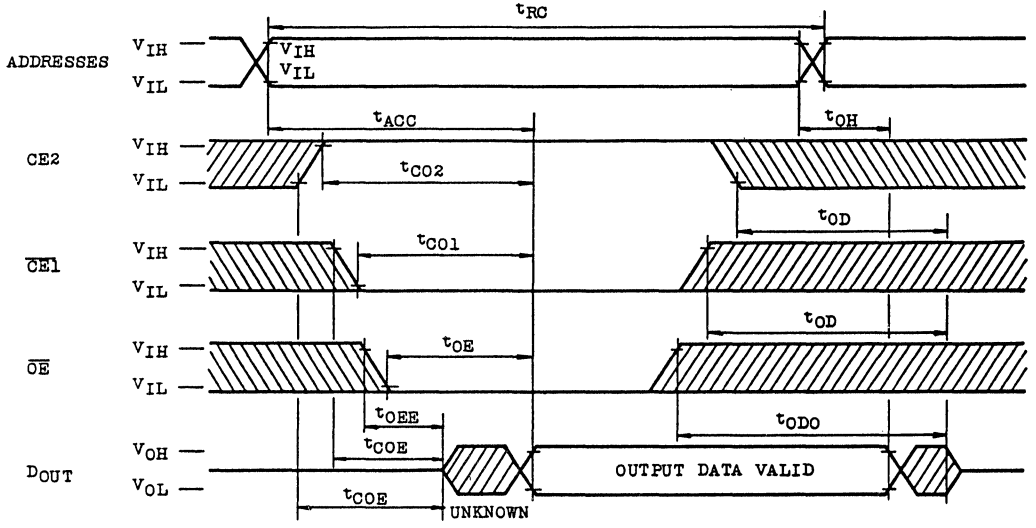
SYMBOL	PARAMETER	TC5563APL-10L		TC5563APL-12L		TC5563APL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	-	100	-	150	-	ns
t_{WP}	Write Pulse Width	60	-	70	-	90	-	
t_{CW}	Chip Selection to End of Write	80	-	85	-	100	-	
t_{AS}	Address Set up Time	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{ODW}	R/W to Output High-Z	-	35	-	40	-	50	
t_{OEW}	R/W to Output Low-Z	5	-	5	-	5	-	
t_{DS}	Data Set up Time	40	-	50	-	60	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

A.C. TEST CONDITION

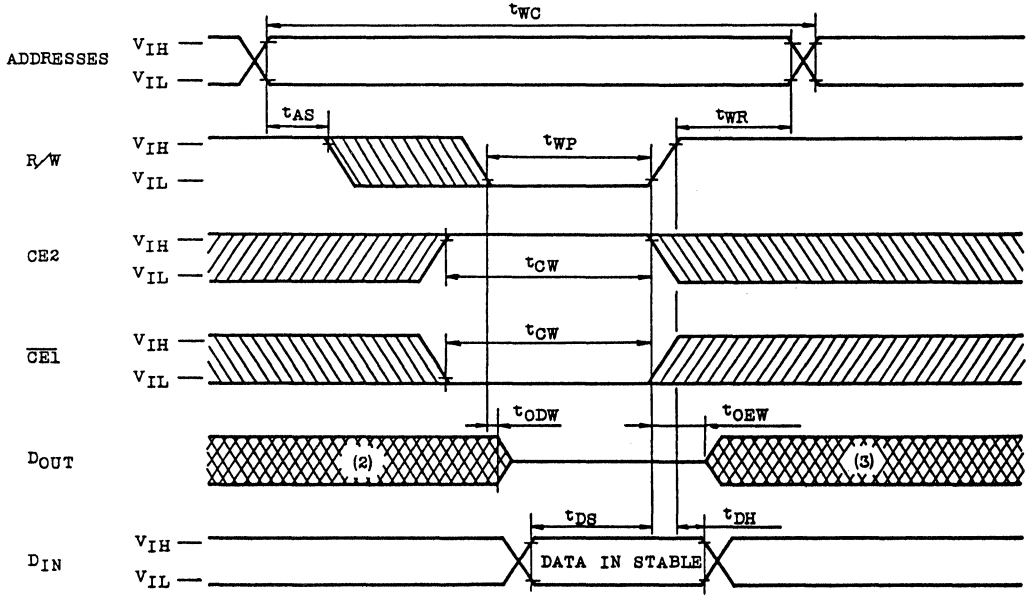
Output Load		: 100pF + 1 TTL Gate
Input Pulse Level		: 0.6V, 2.4V
Timing Measurement	V_{IN}	: 0.8V, 2.2V
Reference Level	V_{OUT}	: 0.8V, 2.2V
t_r, t_f		: 5ns

TIMING WAVEFORMS

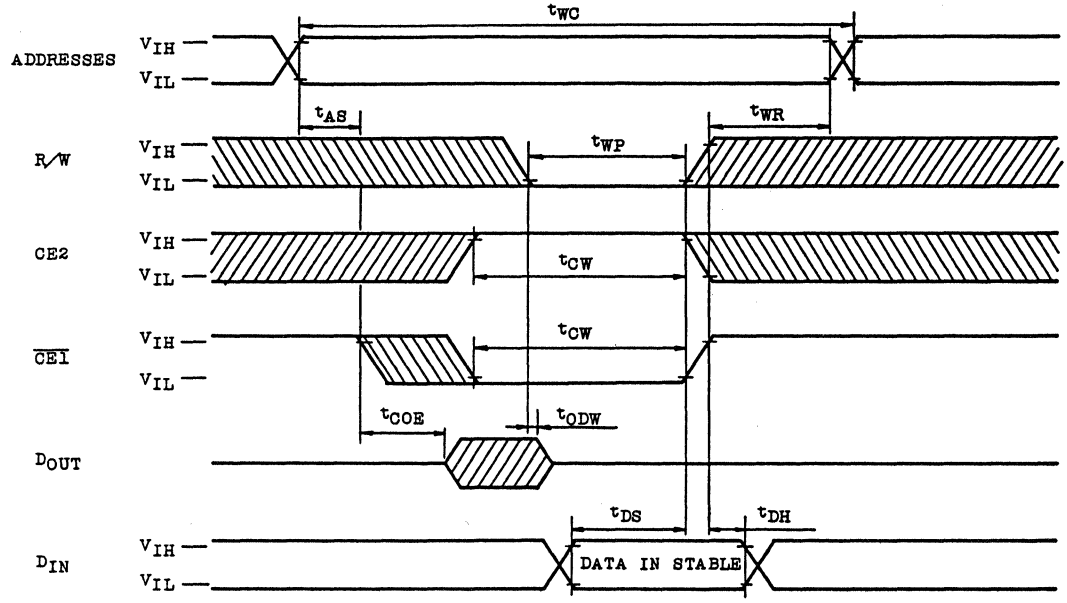
READ CYCLE (1)



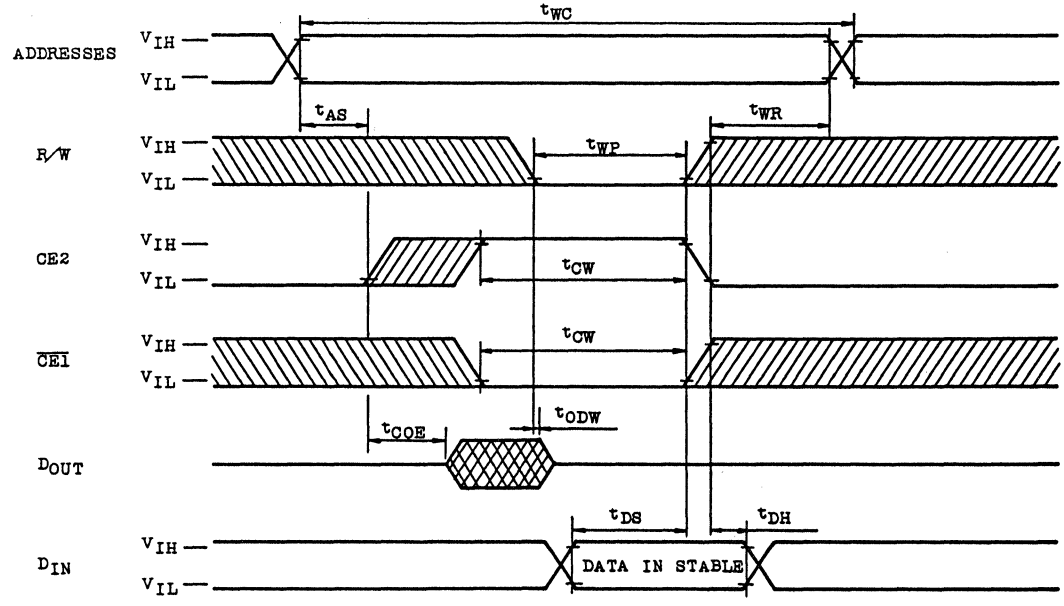
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



Note 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occure coincident with or prior to R/W High transition, Outputs remain in a high impedance state.

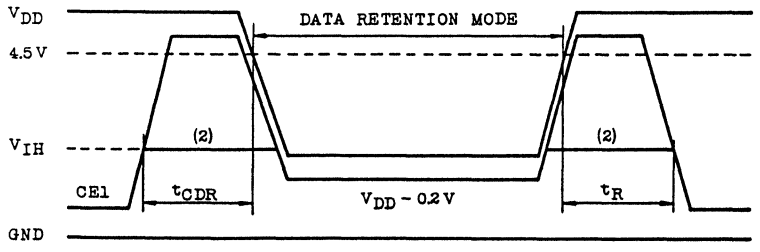
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0 ~ 70°C)

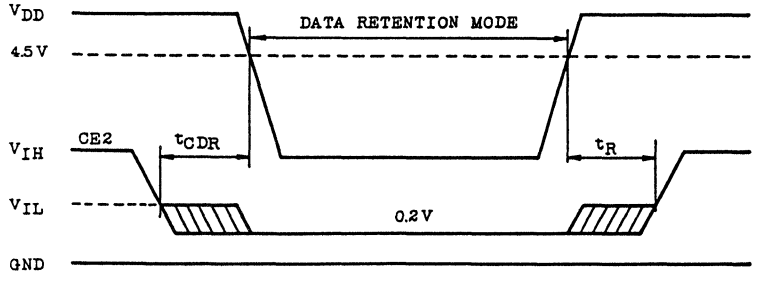
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	V_{DD}=3.0V	-	-	15	µA
		V_{DD}=5.5V	-	-	30	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	µs
t_R	Recovery Time		t_{RC}*	-	-	µs

*: Read cycle time.

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



Note 1: In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2V or CE2 $\geqq$ V_{DD}-0.2V.

2: If the V_{IH} of $\overline{CE1}$ is 2.2V in active operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

3: In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2V.

DEVICE INFORMATION

The TC5563APL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.
This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.

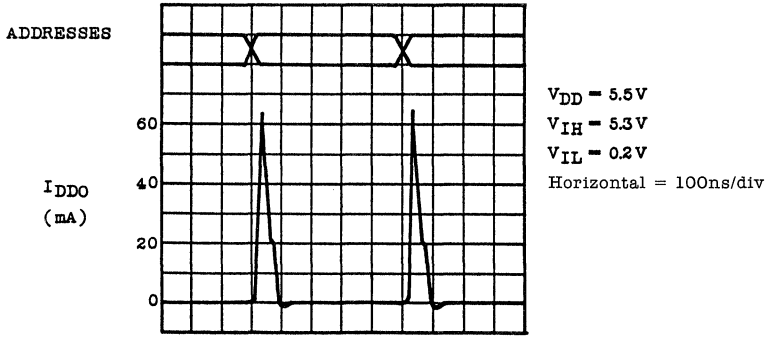
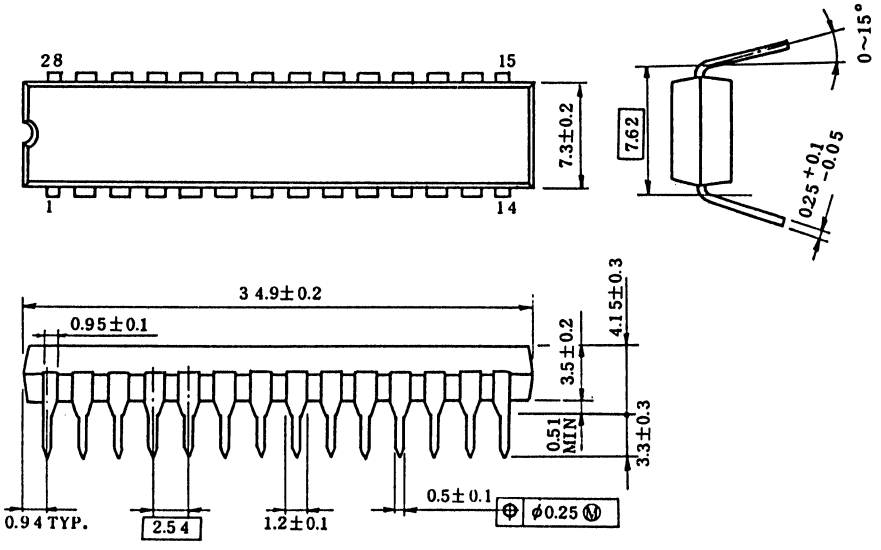


Fig. Typical Current Waveforms

OUTLINE DRAWINGS (DIP28-P-300B)

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

8,192 WORD X 8 BIT CMOS STATIC RAM

DESCRIPTION

The TC5565APL/AFL is a 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns.

When CE2 is a logical low or $\overline{CE1}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC5565APL/AFL has three control inputs. Two chip enables ($\overline{CE1}$, CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5565APL/AFL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC5565APL also features pin compatibility with the 65K bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems. The TC5565APL is offered in a dual-in-line 28 pin standard plastic package.

The TC5565AFL is offered in 28 pin mini Flat Package.

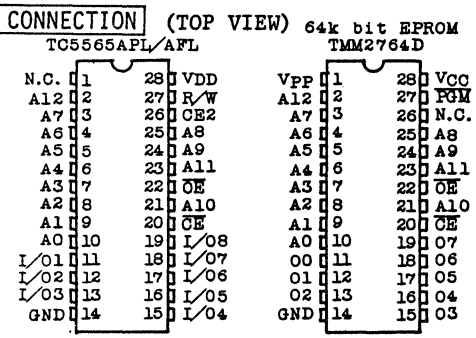
FEATURES

- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current: 100μA(Max.) Ta=70°C
- Access Time
  TC5565APL/AFL-10 : 100ns(Max.)
  TC5565APL/AFL-12 : 120ns(Max.)
  TC5565APL/AFL-15 : 150ns(Max.)
- 5V Single Power Supply
- Power Down Features: CE2, $\overline{CE1}$
- Fully Static Operation
- Data Retention Supply Voltage: 2.0 ∿ 5.5V
- Directly TTL Compatible: All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

Package Type	Device Name
600 mil DIP	TC5565APL
300 mil DIP (Slim Package)	*TC5563APL
Flat Package (SOP)	TC5565AFL

*: See TC5563APL Technical Data

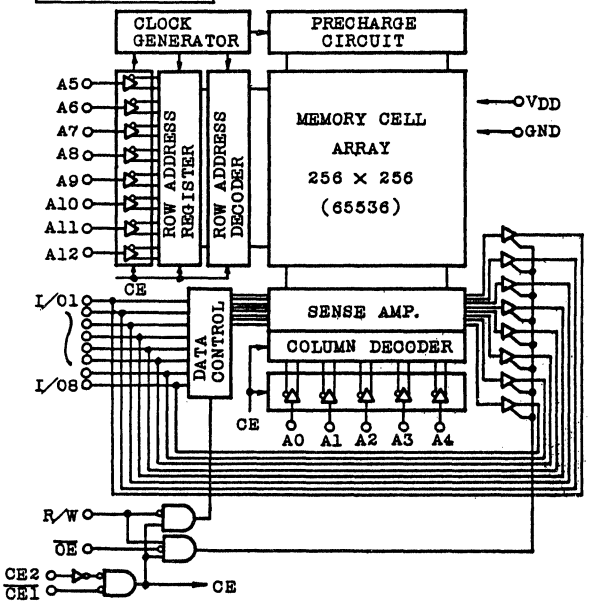
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0 ∿ A12	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
I/O1 ∿ I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ∿ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ∿ 7.0	V
V_{IN}	Input Voltage	-0.3*∿ 7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5 ∿ V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{solder}	Soldering Temperature	260 • 10	°C • sec
T_{stg}	Storage Temperature	-55 ∿ 150	°C
T_{opr}	Operating Temperature	0 ∿ 70	°C

* : -3.0V at pulse width 50ns Max.
**: Flat package

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	
V_{IL}	Input Low Voltage	-0.3*	-	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	

*: -3.0V at pulse width 50ns Max.

D.C. and OPERATING CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

SYMBOL	PARAMRTER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$			-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$			-1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$			4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE_1}=V_{IH}$ or $CE_2=V_{IL}$ or $R/\overline{W}=V_{IL}$ or $\overline{OE}=V_{IH}$ $V_{OUT}=0 \sim V_{DD}$			-	-	±1.0	μA
I_{DDO1}	Operating Current	$V_{DD}=5.5V$ $\overline{CE_1}=V_{IL}$ $CE_2=V_{IH}$ Other input= V_{IH}/V_{IL} $I_{OUT}=0mA$	$t_{cycle}=1.0\mu s$		-	-	10	mA
			TC5565APL-10 TC5565AFL-10	t_{cycle} =100ns	-	-	45	mA
			TC5565APL-12 TC5565AFL-12	t_{cycle} =120ns	-	-	40	mA
			TC5565APL-15 TC5565AFL-15	t_{cycle} =150ns	-	-	35	mA
I_{DDO2}		$V_{DD}=5.5V$ $\overline{CE_1}=0.2V$ $CE_2=V_{DD}-0.2V$ Other input= $V_{DD}-0.2V/0.2V$ $I_{OUT}=0mA$	$t_{cycle}=1.0\mu s$		-	-	5	mA
			TC5565APL-10 TC5565AFL-10	t_{cycle} =100ns	-	-	40	mA
			TC5565APL-12 TC5565AFL-12	t_{cycle} =120ns	-	-	35	mA
			TC5565APL-15 TC5565AFL-15	t_{cycle} =150ns	-	-	30	mA
I_{DDS1}	Standby Current	$\overline{CE_1}=V_{IH}$ or $CE_2=V_{IL}$			-	-	3	mA
*I_{DDS2}		$\overline{CE_1}=V_{DD}-0.2V$ or $CE_2=0.2V$		$V_{DD}=5.5V$	-	2	100	μA
				$V_{DD}=3.0V$	-	1	50	

*: In standby mode with $\overline{CE_1} \geq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $CE_2 \geq V_{DD}-0.2V$ or $CE_2 \leq 0.2V$.

CAPACITANCE ($Ta=25°C$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=GND$	-	-	10	pF
C_{OUT}	Output Capacitance	$V_{OUT}=GND$	-	-	10	

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{DD}=5V±10%)

Read Cycle

SYMBOL	PARAMETER	TC5565APL-10 TC5565AFL-10		TC5565APL-12 TC5565AFL-12		TC5565APL-15 TC5565AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	-	120	-	150	-	ns
t_{ACC}	Address Access Time	-	100	-	120	-	150	
t_{CO1}	$\overline{CE_1}$ Access Time	-	100	-	120	-	150	
t_{CO2}	GE_2 Access Time	-	100	-	120	-	150	
t_{OE}	Output Enable to Output Valid	-	50	-	60	-	70	
t_{COE}	Chip Enable ($\overline{CE_1}$, CE_2) to Output in Low-Z	10	-	10	-	15	-	
t_{OEE}	Output Enable to Output in Low-Z	5	-	5	-	5	-	
t_{OD}	Chip Enable ($\overline{CE_1}$, CE_2) to Output in High-Z	-	35	-	40	-	50	
t_{ODO}	Output Enable to Output in High-Z	-	35	-	40	-	50	
t_{OH}	Output Data Hold Time	20	-	20	-	20	-	

Write Cycle

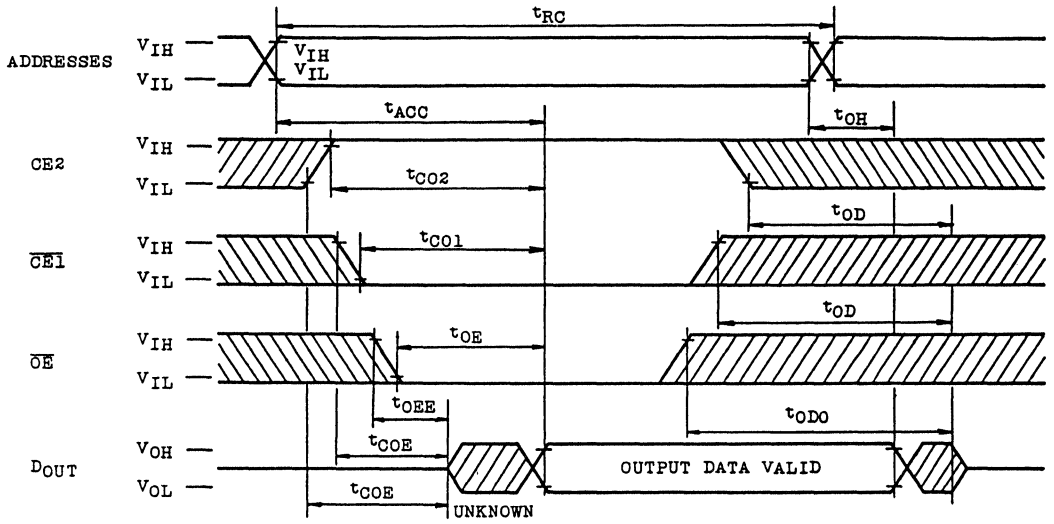
SYMBOL	PARAMETER	TC5565APL-10 TC5565AFL-10		TC5565APL-12 TC5565AFL-12		TC5565APL-15 TC5565AFL-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	-	120	-	150	-	ns
t_{WP}	Write Pulse Width	60	-	70	-	90	-	
t_{CW}	Chip Selection to End of Write	80	-	85	-	100	-	
t_{AS}	Address Set up Time	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{ODW}	R/W to Output High-Z	-	35	-	40	-	50	
t_{OEW}	R/W to Output Low-Z	5	-	5	-	10	-	
t_{DS}	Data Set up Time	40	-	50	-	60	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

A.C. TEST CONDITION

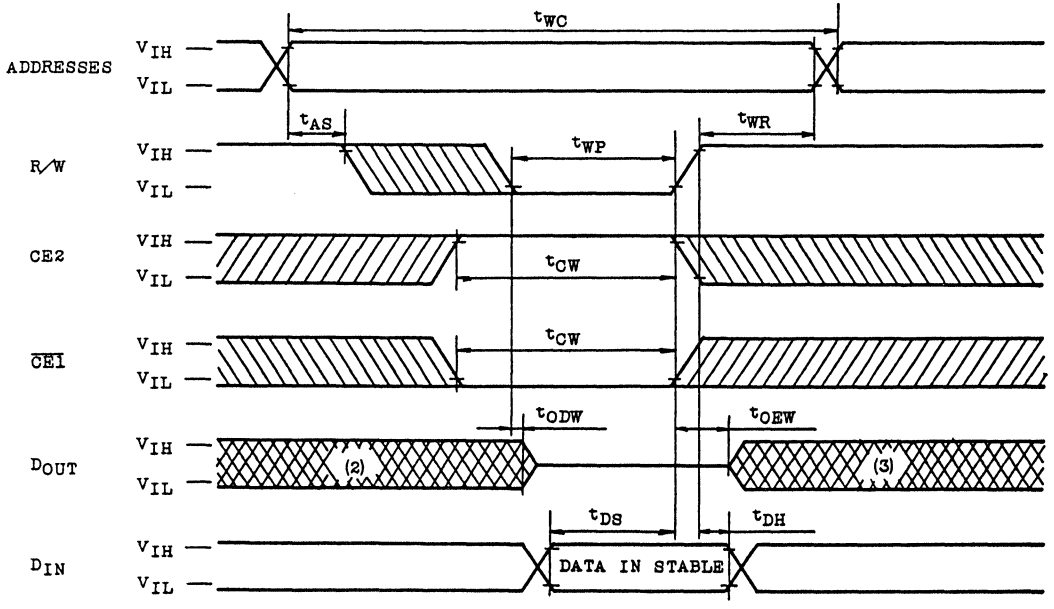
Output Load		: 100pF + 1 TTL Gate
Input Pulse Level		: 0.6V, 2.4V
Timing Measurement	V_{IN}	: 0.8V, 2.2V
Reference Level	V_{OUT}	: 0.8V, 2.2V
t_r, t_f		: 5ns

TIMING WAVEFORMS

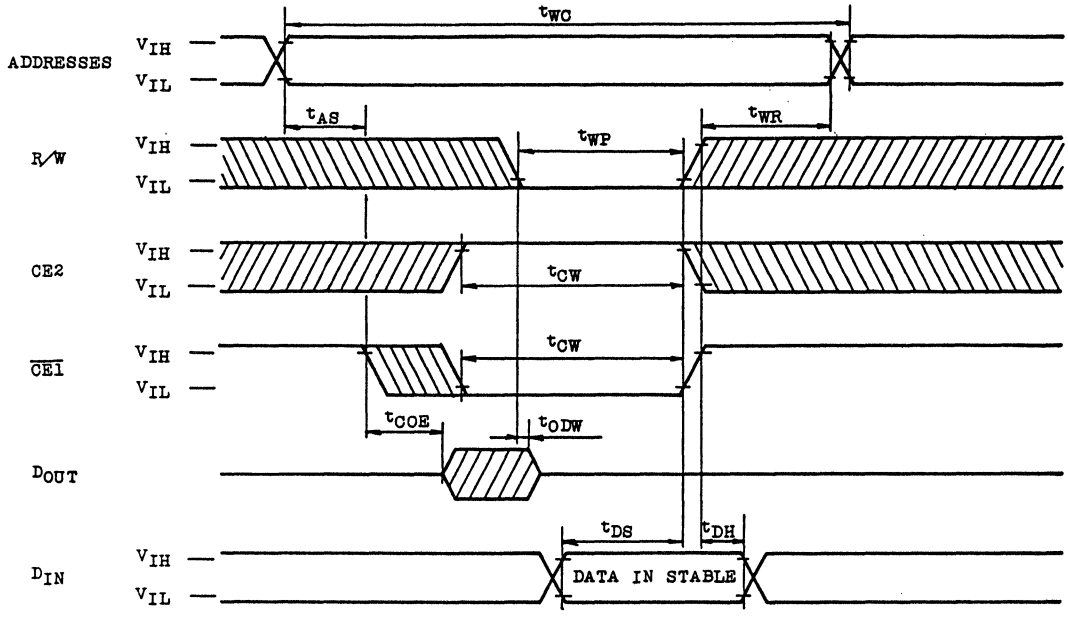
READ CYCLE (1)



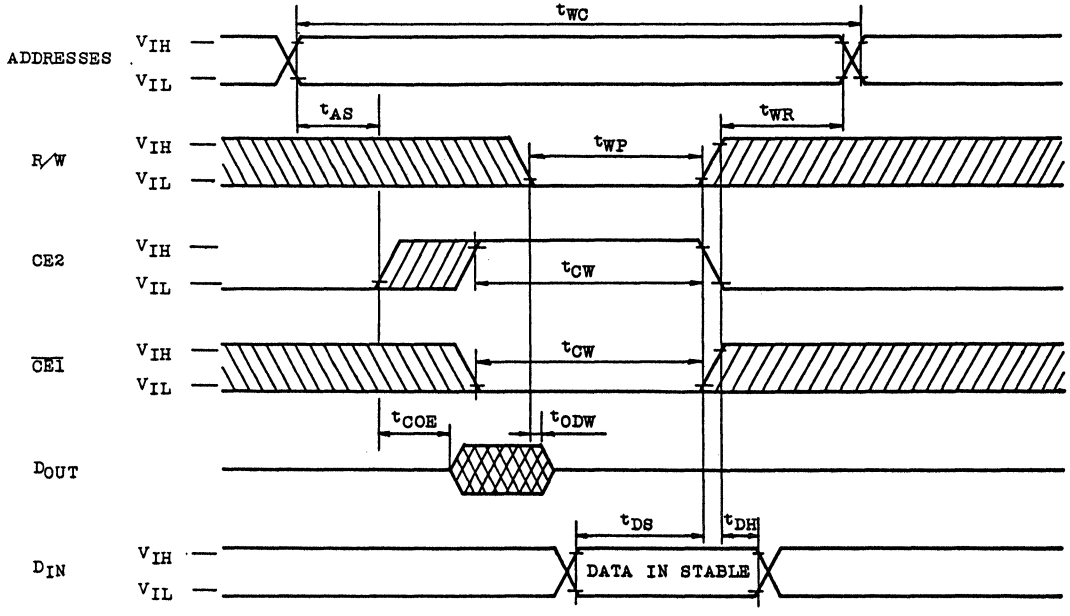
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (4) (CE2 Controlled Write)



Note 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.

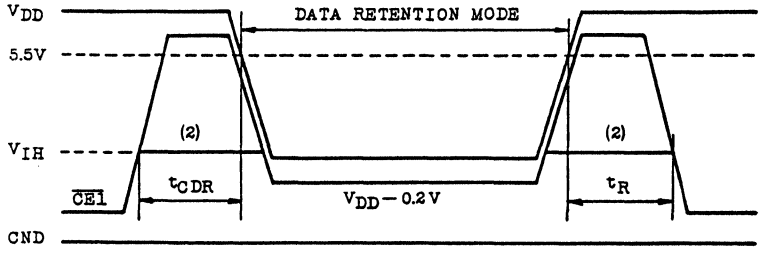
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0 ~ 70°C)

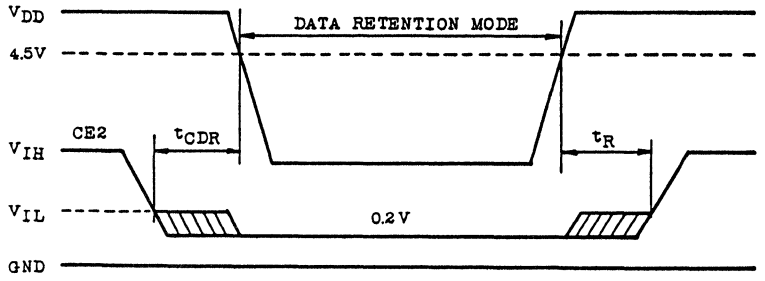
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	V_{DD}=3.0V	-	-	50	μA
		V_{DD}=5.5V	-	-	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	μs
t_R	Recovery Time		t_{RC}*	-	-	μs

*: Read cycle time.

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



Note 1: In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2V or CE2 $\geqq$ V_{DD}-0.2V.

2: If the V_{IH} of $\overline{CE1}$ is 2.2V in active operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

3: In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 $\leqq$ 0.2V.

DEVICE INFORMATION

The TC5565APL/AFL is an asynchronous RAM using address activated circuit technology, thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.
This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.

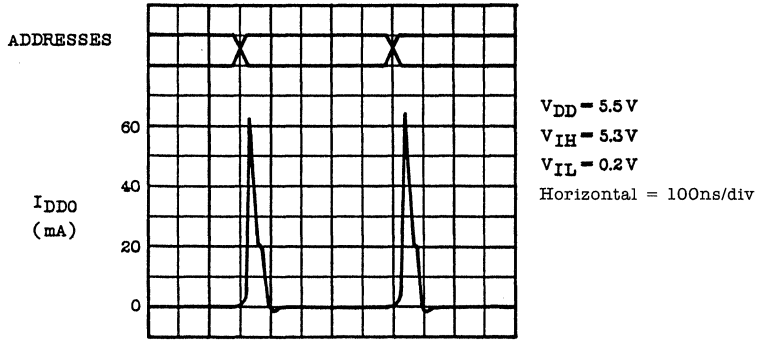
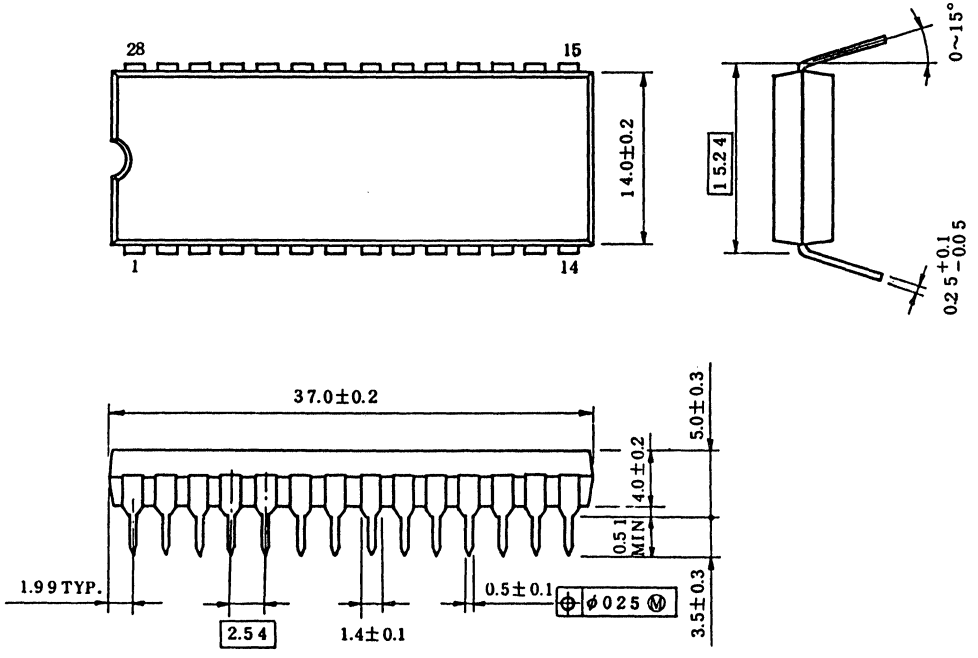


Fig.1 Typical Current Waveforms

OUTLINE DRAWINGS (DIP28-P-600)

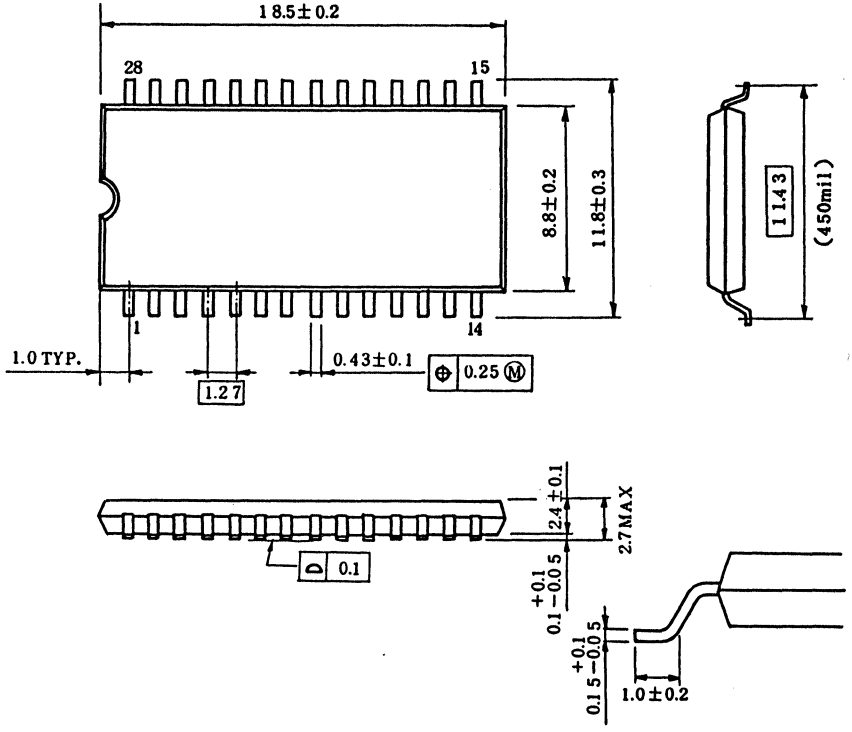
Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS (SOP28-P-450)

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

8,192 WORD X 8 BIT CMOS STATIC RAM

DESCRIPTION

The TC5565APL/AFL is a 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with a maximum operating current of 5mA/MHz and maximum access time of 100ns/120ns/150ns.

When CE_2 is a logical low or $\overline{CE}_1$ is a logical high, the device is placed in low power standby mode in which standby current is 0.6μA typically. The TC5565APL/AFL has three control inputs. Two chip enables ($\overline{CE}_1$, CE_2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC5565APL/AFL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The TC5565APL also features pin compatibility with the 64K bit EPROM (TMM2764D). RAM and EPROM are then interchangeable in the same socket, resulting in flexibility in the definition of the quantity of RAM versus EPROM in microprocessor application systems. The TC5565APL is offered in a dual-in-line 28 pin standard plastic package.

The TC5565AFL is offered in 28 pin mini Flat Package.

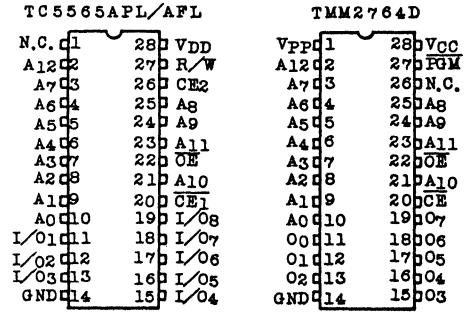
FEATURES

- Low Power Dissipation
  27.5mW/MHz(Max.) Operating
- Standby Current: 1μA(Max.) Ta=25°C
- Access Time
  TC5565APL/AFL-10L: 100ns(Max.)
  TC5565APL/AFL-12L: 120ns(Max.)
  TC5565APL/AFL-15L: 150ns(Max.)
- 5V Single Power Supply
- Power Down Features: CE_2, $\overline{CE}_1$
- Fully Static Operation
- Data Retention Supply Voltage: 2.0-5.5V
- Directly TTL Compatible
  : All Inputs and Outputs
- Pin Compatible with 2764 type EPROM
- TC5565APL Family (Package Type)

Package Type	Device Name
600 mil DIP	TC5565APL
300 mil DIP (Slim Package)	*TC5563APL
Flat Package (SOP)	TC5565AFL

*: See TC5563APL Technical Data.

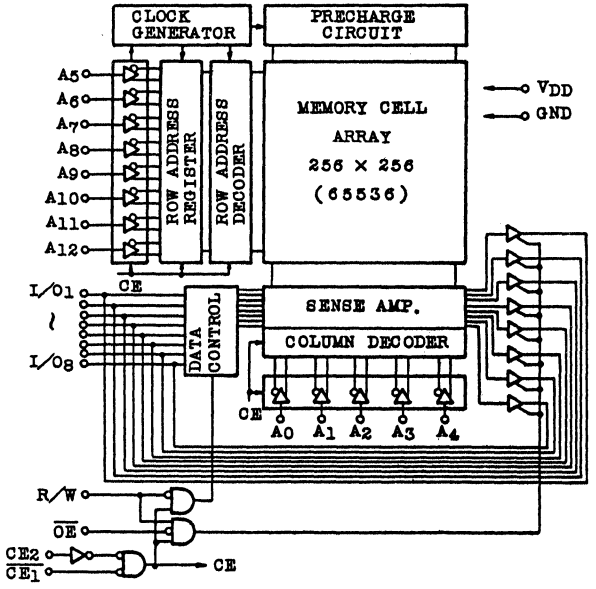
PIN CONNECTION (TOP VIEW)



PIN NAMES

A_0~A_{12}	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}_1$, CE_2	Chip Enable Inputs
I/O_1~I/O_8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE_1}$	CE_2	$\overline{OE}$	R/W	I/O_1-I/O_8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3-7.0	V
V_{IN}	Input Voltage	-0.3*-7.0	V
$V_{I/O}$	Input and Output Voltage	-0.5-V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.6**	W
T_{solder}	Soldering Temperature	260 · 10	°C·sec
T_{stg}	Storage Temperature	-55-150	°C
T_{opr}	Operating Temperature	0-70	°C

*: -3.0V at pulse width 50ns MAX.

**: Flat package

D.C RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3*	-	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

*: -3.0V at pulse width 50ns MAX.

D.C. and OPERATING CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$			-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$			-1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$			4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1}=V_{IH}$ or CE2=V_{IL} or R/W=V_{IL} or $\overline{OE}=V_{IH}$ $V_{OUT}=0 \sim V_{DD}$			-	-	±1.0	μA
I_{DDO1}	Operating Current	$V_{DD}=5.5V$	$t_{cycle}=1.0\mu s$		-	-	10	mA
		$\overline{CE1}=V_{IL}$ CE2=V_{IH} Other input= V_{IH}/V_{IL} $I_{OUT}=0mA$	TC5565APL-10L TC5565AFL-10L	t_{cycle} =100ns	-	-	45	mA
			TC5565APL-12L TC5565AFL-12L	t_{cycle} =120ns	-	-	40	mA
			TC5565APL-15L TC5565AFL-15L	t_{cycle} =150ns	-	-	35	mA
I_{DDO2}		$V_{DD}=5.5V$	$t_{cycle}=1.0\mu s$		-	-	5	mA
		$\overline{CE1}=0.2V$ CE2=V_{DD}-0.2V Other input= V_{DD}-0.2V/0.2V $I_{OUT}=0mA$	TC5565APL-10L TC5565AFL-10L	t_{cycle} =100ns	-	-	40	mA
			TC5565APL-12L TC5565AFL-12L	t_{cycle} =120ns	-	-	35	mA
			TC5565APL-15L TC5565AFL-15L	t_{cycle} =150ns	-	-	30	mA
I_{DDS1}	Standby Current	$\overline{CE1}=V_{IH}$ or CE2=V_{IL}			-	-	3	mA
* I_{DDS2}	Standby Current	$\overline{CE1}=V_{DD}$-0.2V or CE2=0.2V	Ta=25°C		-	0.6	1.0	μA
			Ta=0 ∿ 70°C		-	-	30	

*: In standby mode with $\overline{CE1} \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of CE2 ≧ V_{DD}-0.2V or CE2 ≦ 0.2V.

CAPACITANCE (Ta=25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	

Note: This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta=0~70°C, V_{DD}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TC5565APL-10L TC5565AFL-10L		TC5565APL-12L TC5565AFL-12L		TC5565APL-15L TC5565AFL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	100	-	120	-	150	-	ns
t_{ACC}	Address Access Time	-	100	-	120	-	150	
t_{CO1}	$\overline{CE}_1$ Access Time	-	100	-	120	-	150	
t_{CO2}	CE_2 Access Time	-	100	-	120	-	150	
t_{OE}	Output Enable to Output Valid	-	50	-	60	-	70	
t_{COE}	Chip Enable ($\overline{CE}_1$, CE_2) to Output in Low-Z	10	-	10	-	15	-	
t_{OEE}	Output Enable to Output in Low-Z	5	-	5	-	5	-	
t_{OD}	Chip Enable ($\overline{CE}_1$, CE_2) to Output in High-Z	-	35	-	40	-	50	
t_{ODO}	Output Enable to Output in High-Z	-	35	-	40	-	50	
t_{OH}	Output Data Hold Time	20	-	20	-	20	-	

WRITE CYCLE

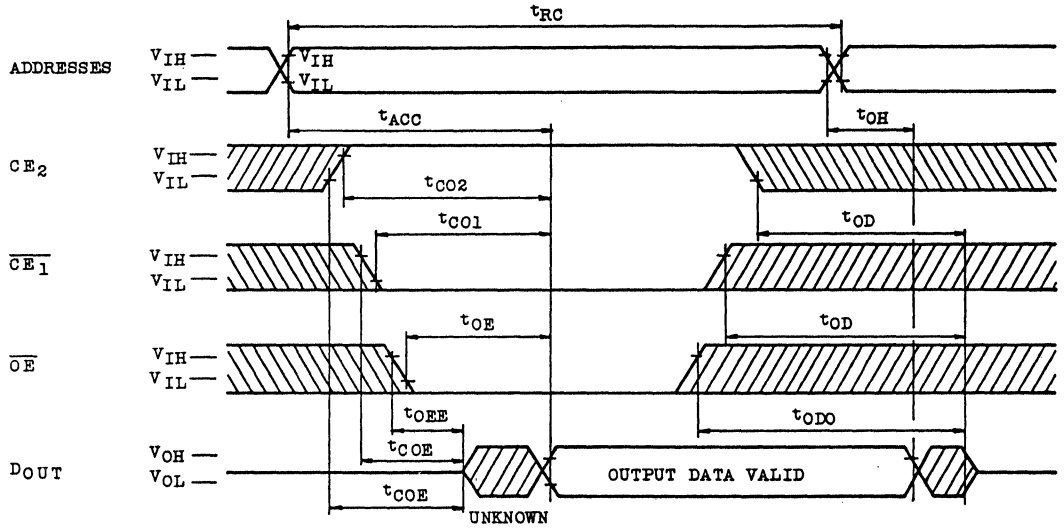
SYMBOL	PARAMETER	TC5565APL-10L TC5565AFL-10L		TC5565APL-12L TC5565AFL-12L		TC5565APL-15L TC5565AFL-15L		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	100	-	120	-	150	-	ns
t_{WP}	Write Pulse Width	60	-	70	-	90	-	
t_{CW}	Chip Selection to End of Write	80	-	85	-	100	-	
t_{AS}	Address Set up Time	0	-	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	
t_{ODW}	R/W to Output High-Z	-	35	-	40	-	50	
t_{OEW}	R/W to Output Low-Z	5	-	5	-	10	-	
t_{DS}	Data Set up Time	40	-	50	-	60	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	

A.C. TEST CONDITION

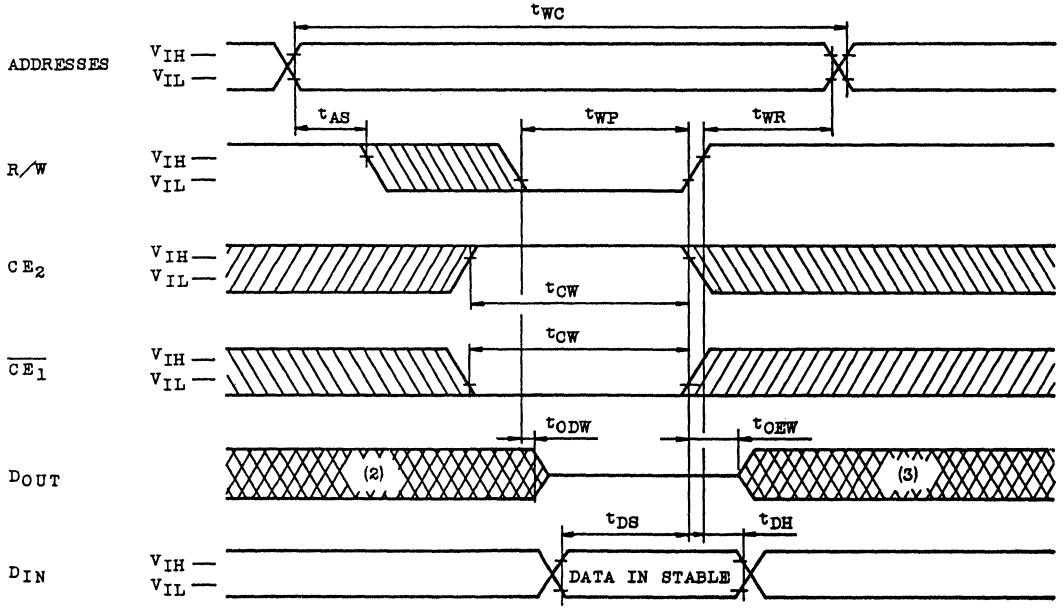
Output Load		: 100pF + 1 TTL Gate
Input Pulse Level		: 0.6V, 2.4V
Timing Measurement	V_{IN}	: 0.8V, 2.2V
Reference Level	V_{OUT}	: 0.8V, 2.2V
tr, tf		: 5ns

TIMING WAVEFORMS

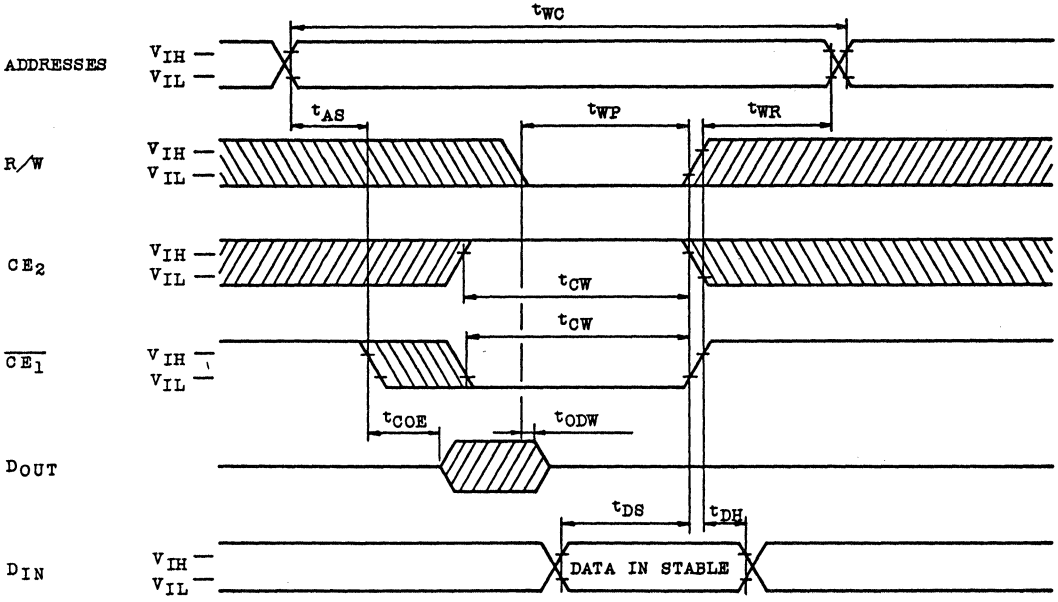
READ CYCLE (1)



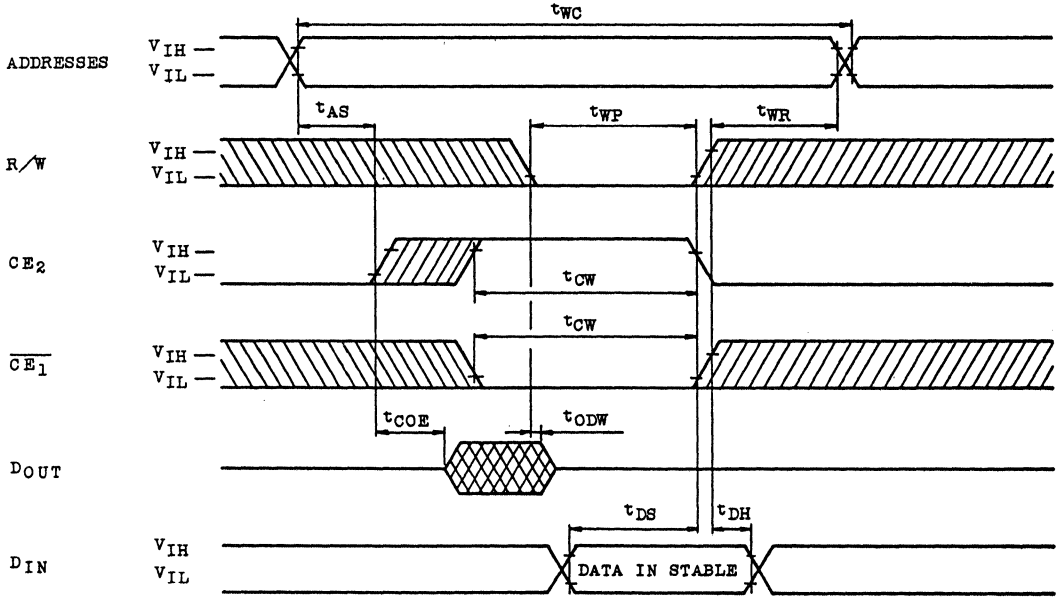
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}_1$ Controlled Write)



WRITE CYCLE 3 (4) (CE_2 Controlled Write)



Note 1. R/W is High for Read Cycle.

2. Assuming that $\overline{CE}_1$ Low transition or CE_2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

3. Assuming that $\overline{CE}_1$ High transition or CE_2 Low transition occurs coincident with or prior to R/W High transition, Outputs remain in a high impedance state.

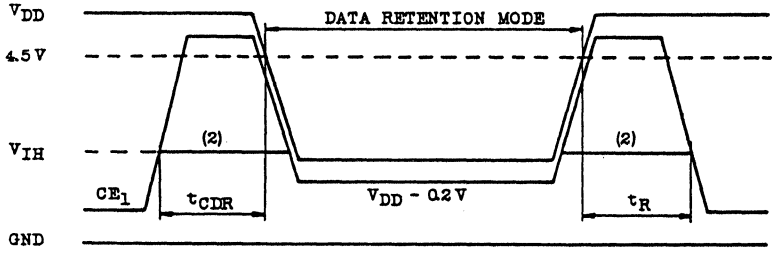
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta=0-70°C)

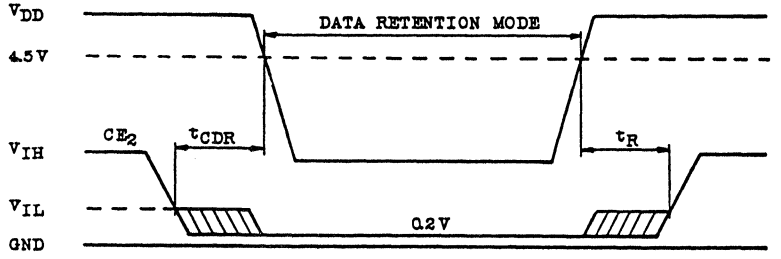
SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	V_{DD}=3.0V	-	-	15	µA
		V_{DD}=5.5V	-	-	30	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	µs
t_R	Recovery Time		t_{RC} *	-	-	µs

*: Read cycle time.

$\overline{CE}_1$ Controlled Data Retention Mode (1)



CE_2 Controlled Data Retention Mode (3)



Note 1 : In $\overline{CE}_1$ controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leq 0.2V$ or $CE_2 \geq V_{DD}-0.2V$.

2 : If the V_{IH} of $\overline{CE}_1$ is 2.2V in active operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

3 : In CE_2 controlled data retention mode, minimum standby current mode is achieved under the condition of $CE_2 \leq 0.2V$.

DEVICE INFORMATION

The TC5565APL/AFL is an asynchronous RAM using address activated circuit thus the internal operation is synchronous. Then once row address change occur, the precharge operation is executed by internal pulse generated from row address transient. Therefore the peak current flows only after row address change, as shown in the following figure.

This peak current may induce the noise on V_{DD}/GND lines. Thus the use of about 0.1μF decoupling capacitor for every device is recommended to eliminate such noise.

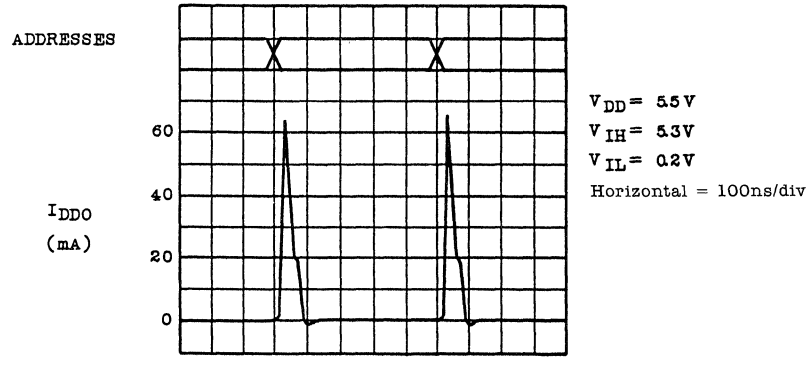
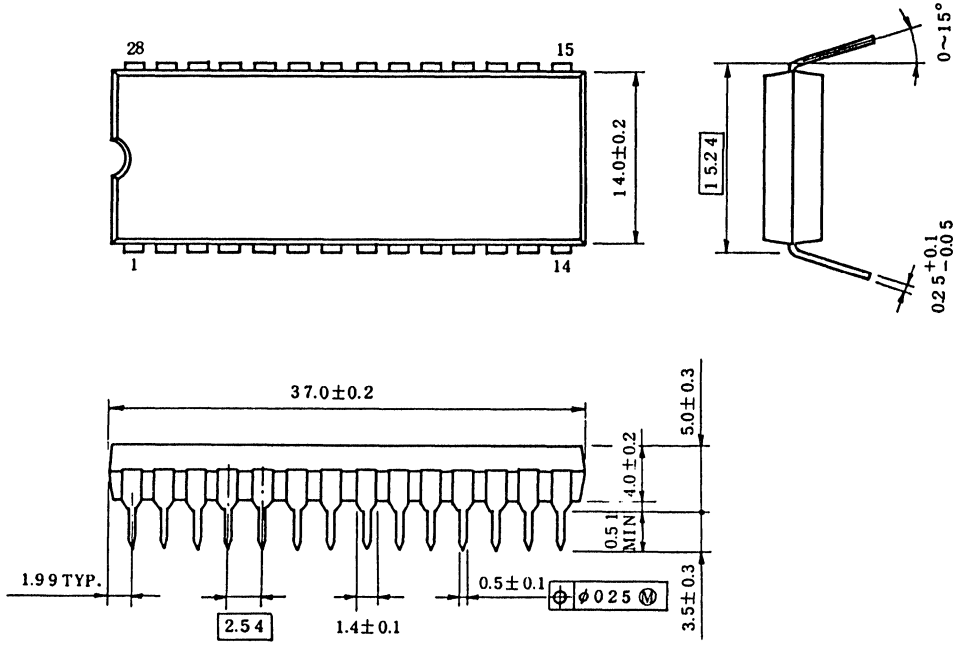


Fig.TYPICAL CURRENT WAVEFORMS

OUTLINE DRAWINGS (DIP28-P-600)

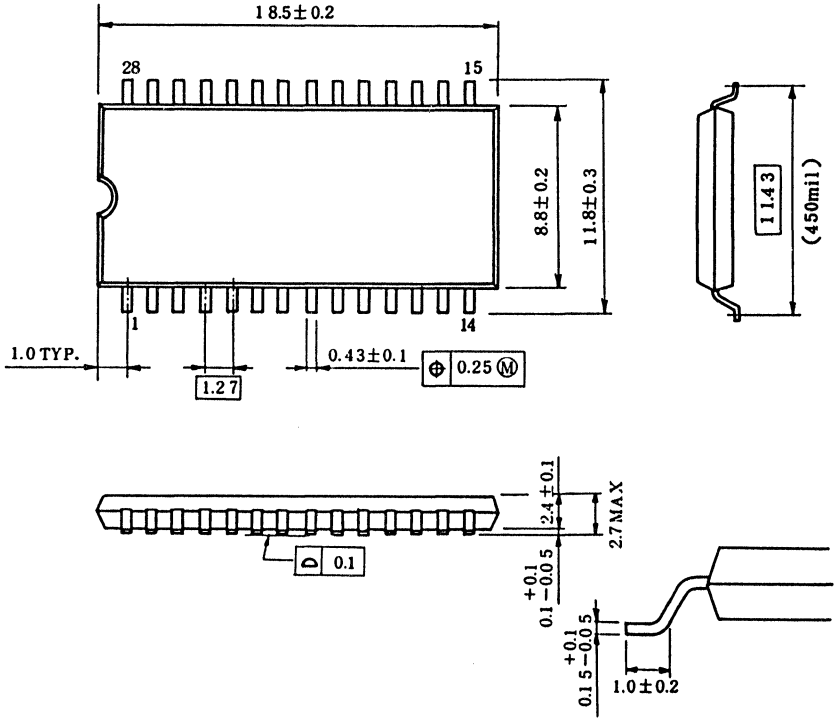
Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS (SOP28-P-450)

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

32,768 WORDS × 8 BIT STATIC RAM

DESCRIPTION

The TC55257BPL is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (Typ.) and minimum cycle time of 85ns.

When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA typically. The TC55257BPL has two control inputs. Chip enable ($\overline{CE}$) allows for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257BPL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC55257BPL is offered in both a standard dual-in-line 28 pin plastic package (0.6/0.3 inch width) and small-out-line plastic flat package.

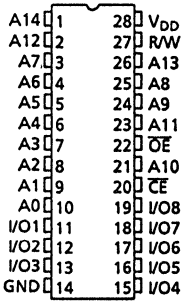
FEATURES

- Low Power Dissipation
  27.5mW / MHz (Typ.) Operating
- Standby Current
  100μA (Max.) :
  TC55257 BPL-85 / BFL-85 / BSPL-85
  BPL-10 / BFL-10 / BSPL-10
- 5V Single Power Supply
- Power Down Feature: $\overline{CE}$
- Data retention Supply Voltage:
  2.0~5.5V
- Access Time

	TC55257BPL-85 TC55257BFL-85 TC55257BSPL-85	TC55257BPL-10 TC55257BFL-10 TC55257BSPL-10
Access Time (max.)	85ns	100ns
Chip Enable Access Time (max.)	85ns	100ns
Output Enable Time (Max.)	45ns	50ns

- Directly TTL Compatible: All Inputs and Outputs
- Plastic DIP, Plastic FP and Plastic Slim Package

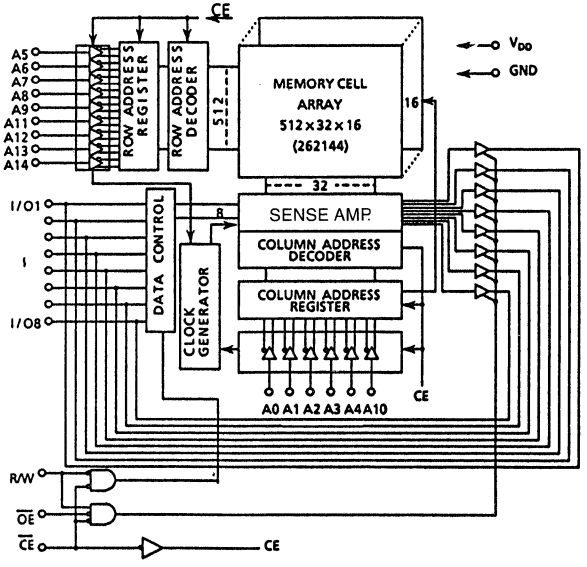
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1~I/O8	Data Input/Output
V_{DD}	Power (+ 5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1~I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5*~V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.8/0.6**	W
Tsolder	Soldering Temperature	260·10	°C·sec
Tstrg	Storage Temperature	−55~150	°C
Topr	Operating Temperature	0~70	°C

*) −3.0V at pulse width 50ns
**) 0.6inch 1.0W, 0.3inch 0.8W, 0.45inch 0.6W

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3*	−	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	−	5.5	V

*) −3.0V at pulse width 50ns

D.C. and OPERATING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNITS
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$		-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$		-1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$		4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/\overline{W} = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$		-	-	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ $R/\overline{W} = V_{IH}$ Other Input = V_{IH} / V_{IL} I_{OUT} = 0mA	$t_{cycle} = 1\mu s$	-	10	-	mA
			t_{cycle} = Min. cycle	-	-	70	
I_{DDO2}		$\overline{CE} = 0.2V$ $R/\overline{W} = V_{DD} - 0.2V$ Other Input = $V_{DD} - 0.2V$ / $0.2V$ I_{OUT} = 0mA	$t_{cycle} = 1\mu s$	-	5	-	mA
			t_{cycle} = Min. cycle	-	-	60	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$		-	-	3	mA
I_{DDS2}	Standby Current	$\overline{CE} = V_{DD} - 0.2V$ $V_{DD} = 2.0V \sim 5.5V$	$Ta = 0 \sim 70°C$	-	2	100	μA

CAPACITANCE ($Ta = 25°C$, $f = 1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = GND$	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{DD} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC55257BPL-85 TC55257BFL-85 TC55257BSPL-85		TC55257BPL-10 TC55257BFL-10 TC55257BSPL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	-	100	-	ns
t_{ACC}	Address Access Time	-	85	-	100	
t_{CO}	$\overline{CE}$ Access Time	-	85	-	100	
t_{OE}	Output Enable to Output in Valid	-	45	-	50	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low	10	-	10	-	
t_{OEE}	Output Enable to Output in Low-Z	5	-	5	-	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	-	30	-	50	
t_{ODO}	Output Enable to Output in High-Z	-	30	-	40	
t_{OH}	Output Data Hold Time	10	-	10	-	

WRITE CYCLE

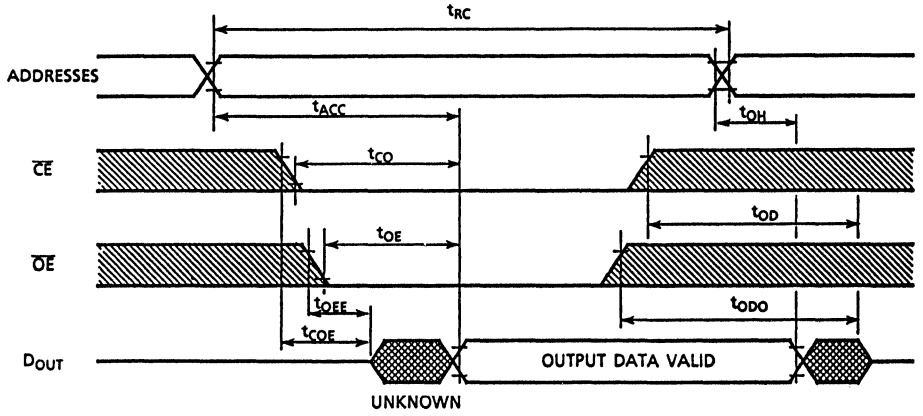
SYMBOL	PARAMETER	TC55257BPL-85 TC55257BFL-85 TC55257BSPL-85		TC55257BPL-10 TC55257BFL-10 TC55257BSPL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	-	100	-	ns
t_{WP}	Write Pulse Width	60	-	70	-	
t_{CW}	Chip Selection to End of Write	65	-	90	-	
t_{AS}	Address Set up Time	0	-	0	-	
t_{WR}	Write Recovery Time	5	-	5	-	
t_{ODW}	R/W to Output High-Z	-	30	-	50	
t_{OEW}	R/W to Output Low-Z	5	-	5	-	
t_{DS}	Data Set up Time	40	-	40	-	
t_{DH}	Data Hold Time	0	-	0	-	

A.C. TEST CONDITIONS

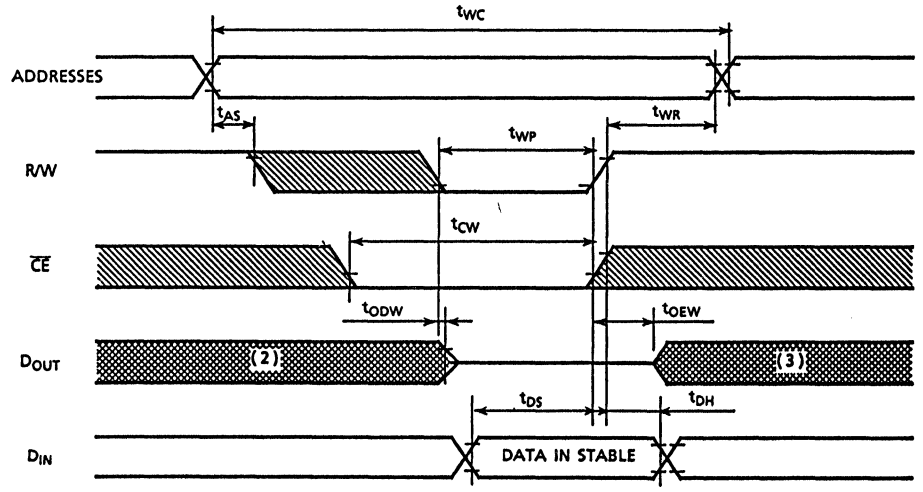
Output Load : 100pF + 1 TTL Gate
Input Pulse Level : 0.6V, 2.4V
Timing Measurement : 0.8V, 2.2V
Reference Level : 0.8V, 2.2V
t_r, t_f : 5ns

TIMING WAVEFROMS

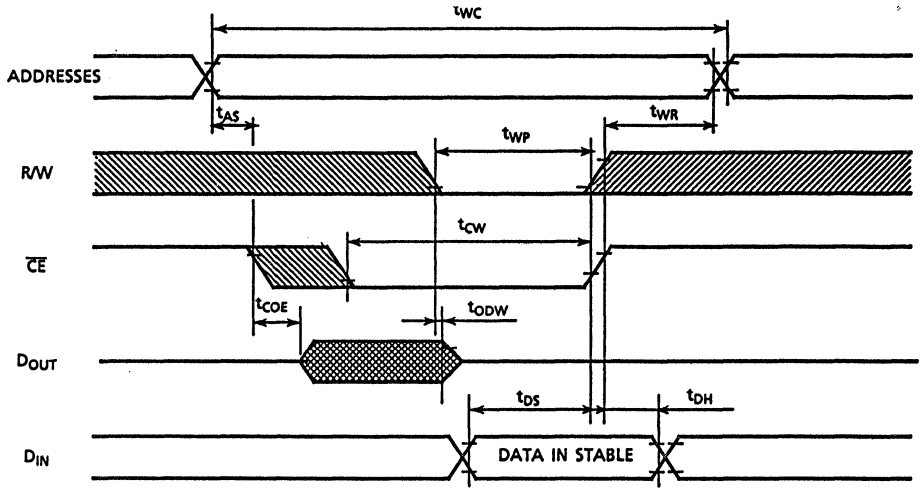
READ CYCLE (1)



WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}$ Controlled Write)



Note: 1. R/W is High for read cycle.

2. Assuming that $\overline{CE}$ low transition occurs coincident with or after R/W Low transition, Outputs remain a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R/W High transition, Outputs remain a high impedance state.

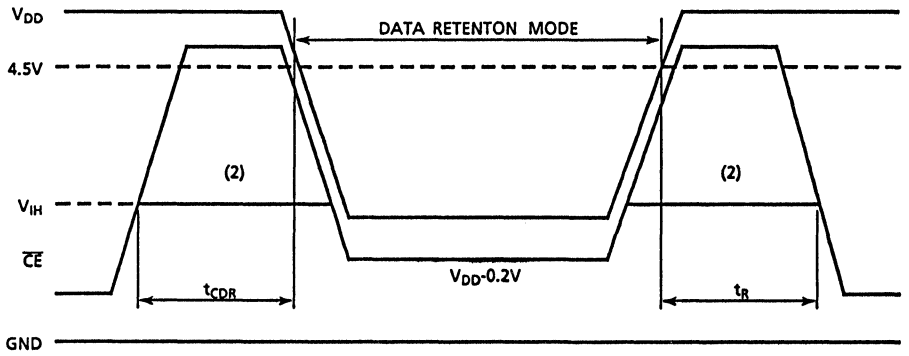
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	V_{DH} = 3.0V	-	-	50	µA
		V_{DH} = 5.5V	-	-	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	µS
t_R	Recovery Time		t_{RC} (1)	-	-	

Note (1): Read Cycle Time.

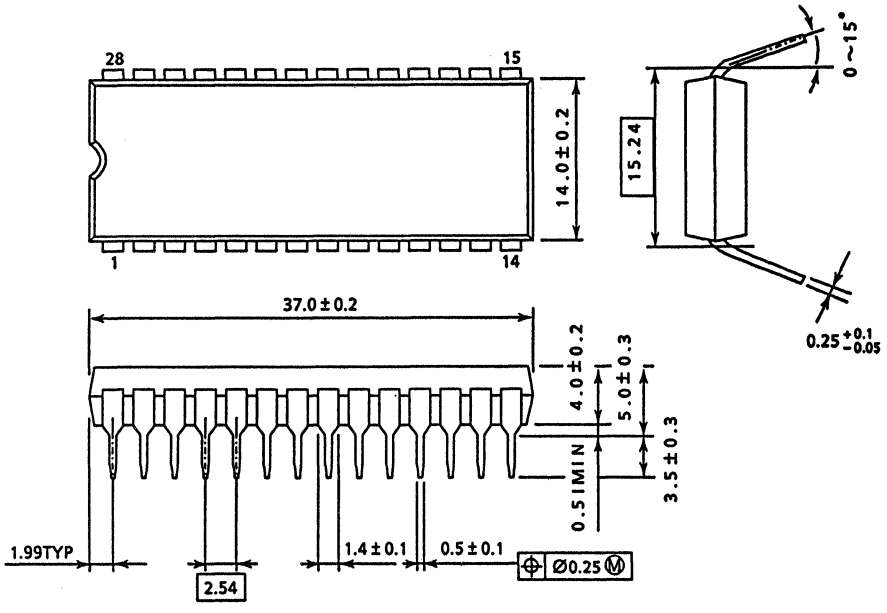
CE Controlled Data Retention Mode



Note (2): If the V_{IH} of $\overline{CE}$ is 2.2V in operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

OUTLINE DRAWINGS (DIP28 - P - 600)

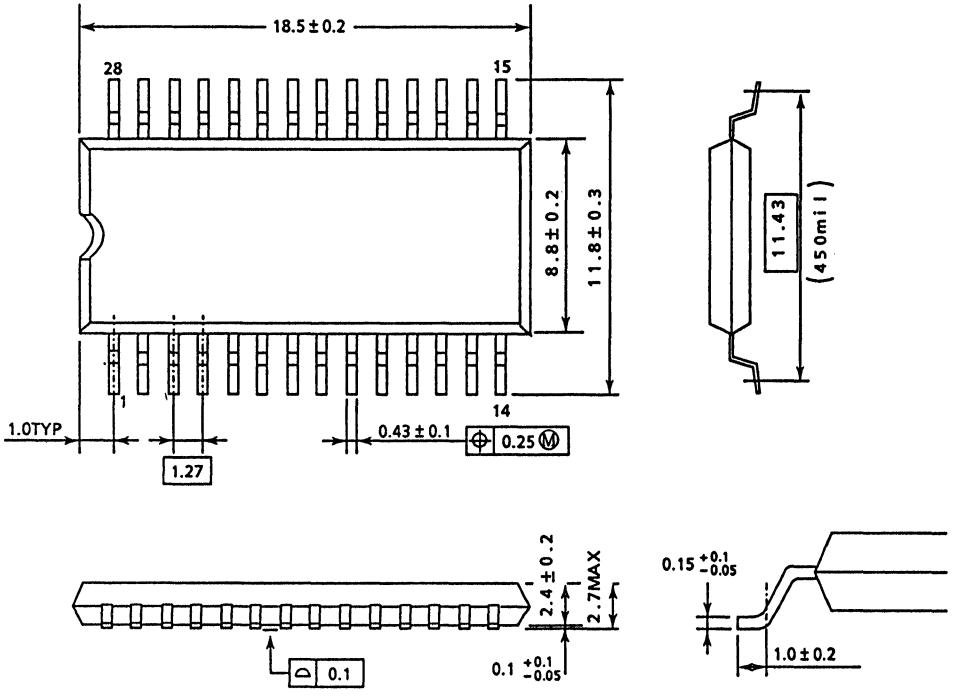
UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS (SOP28 - P - 450)

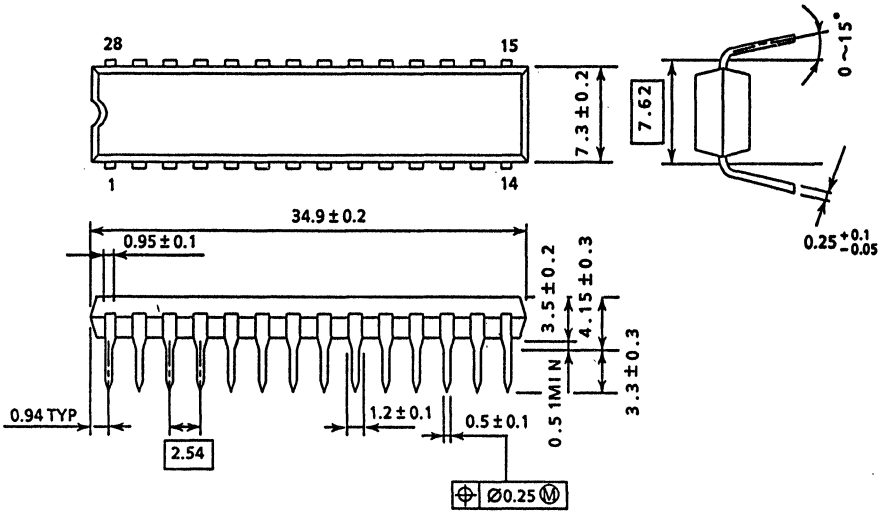
UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS (DIP28 – P – 300B)

UNIT: mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

32,768 WORDS × 8 BIT STATIC RAM

DESCRIPTION

The TC55257BPL is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operates from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (Typ.) and minimum cycle time of 85ns.

When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA at room temperature. The TC55257BPL has two control inputs. Chip enable ($\overline{CE}$) allows for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257BPL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC55257BPL is offered in both standard dual-in-line 28 pin 0.6 and 0.3 inch width plastic packages. The TC55257BFL is offered in a 28 pin 450 mil small outline plastic flat package.

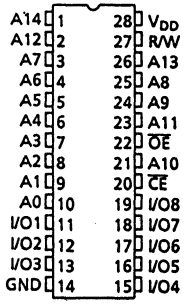
FEATURES

- **Low Power Dissipation**
  27.5mW / MHz (Typ.) Operating
- **Standby Current**
  2μA at Ta = 25°C (Max.):
  TC55257 BPL-85L / BFL-85L / BSPL-85L
  BPL-10L / BFL-10L / BSPL-10L
- **5V Single Power Supply**
- **Power Down Feature: $\overline{CE}$**
- **Data retention Supply Voltage:**
  2.0V ~ 5.5V
- **Access Time**

	TC55257BPL-85L TC55257BFL-85L TC55257BSPL-85L	TC55257BPL-10L TC55257BFL-10L TC55257BSPL-10L
Access Time (max.)	85ns	100ns
Chip Enable Access Time (max.)	85ns	100ns
Output Enable Time (Max.)	45ns	50ns

- **Directly TTL Compatible: All Inputs and Outputs**
- **Plastic DIP, Plastic FP and Plastic Slim Package**

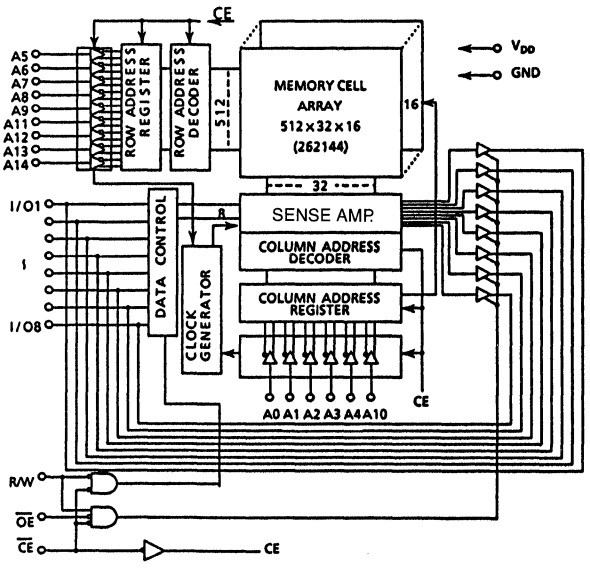
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1~I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1~I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5*~V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.8/0.6 **	W
Tsolder	Soldering Temperature	260·10	°C·sec
Tstrg	Storage Temperature	−55~150	°C
Topr	Operating Temperature	0~70	°C

*) −3.0V at pulse width 50ns
**) 0.6inch 1.0W, 0.3inch 0.8W, 0.45inch 0.6W

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3*	−	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	−	5.5	V

*) −3.0V at pulse width 50ns

D.C. and OPERATING CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNITS
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$		-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$		-1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$		4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/\overline{W} = V_{IL}$ or $\overline{OE} = V_{IH}$ $V_{OUT} = 0 \sim V_{DD}$		-	-	±1.0	μA
I_{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ $R/\overline{W} = V_{IH}$ Other Input = V_{IH} / V_{IL} $I_{OUT} = 0mA$	$t_{cycle} = 1\mu s$	-	10	-	mA
			t_{cycle} = Min. cycle	-	-	70	
I_{DDO2}		$\overline{CE} = 0.2V$ $R/\overline{W} = V_{DD} - 0.2V$ Other Input = $V_{DD} - 0.2V$ / $0.2V$ $I_{OUT} = 0mA$	$t_{cycle} = 1\mu s$	-	5	-	mA
			t_{cycle} = Min. cycle	-	-	60	
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$		-	-	3	mA
I_{DDS2}	Standby Current	$\overline{CE} = V_{DD} - 0.2V$ $V_{DD} = 2.0V \sim 5.5V$	$Ta = 0 \sim 70°C$	-	-	30	μA
			$Ta = 25°C$	-	-	2	

CAPACITANCE ($Ta = 25°C$, $f = 1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = GND$	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55257BPL-85L TC55257BFL-85L TC55257BSPL-85L		TC55257BPL-10L TC55257BFL-10L TC55257BSPL-10L		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	ns
t_{ACC}	Address Access Time	–	85	–	100	
t_{CO}	$\overline{CE}$ Access Time	–	85	–	100	
t_{OE}	Output Enable to Output in Valid	–	45	–	50	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low	10	–	10	–	
t_{OEE}	Output Enable to Output in Low-Z	5	–	5	–	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	–	30	–	50	
t_{ODO}	Output Enable to Output in High-Z	–	30	–	40	
t_{OH}	Output Data Hold Time	10	–	10	–	

WRITE CYCLE

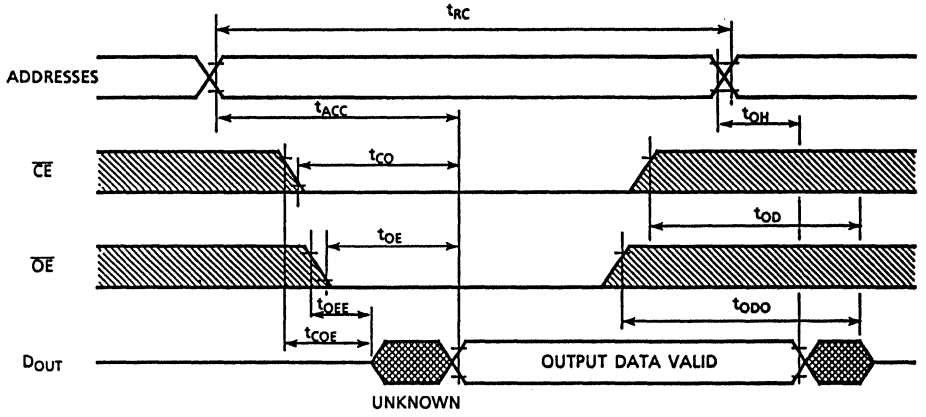
SYMBOL	PARAMETER	TC55257BPL-85L TC55257BFL-85L TC55257BSPL-85L		TC55257BPL-10L TC55257BFL-10L TC55257BSPL-10L		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	
t_{CW}	Chip Selection to End of Write	65	–	90	–	
t_{AS}	Address Set up Time	0	–	0	–	
t_{WR}	Write Recovery Time	5	–	5	–	
t_{ODW}	R/W to Output High-Z	–	30	–	50	
t_{OEW}	R/W to Output Low-Z	5	–	5	–	
t_{DS}	Data Set up Time	40	–	40	–	
t_{DH}	Data Hold Time	0	–	0	–	

A.C. TEST CONDITIONS

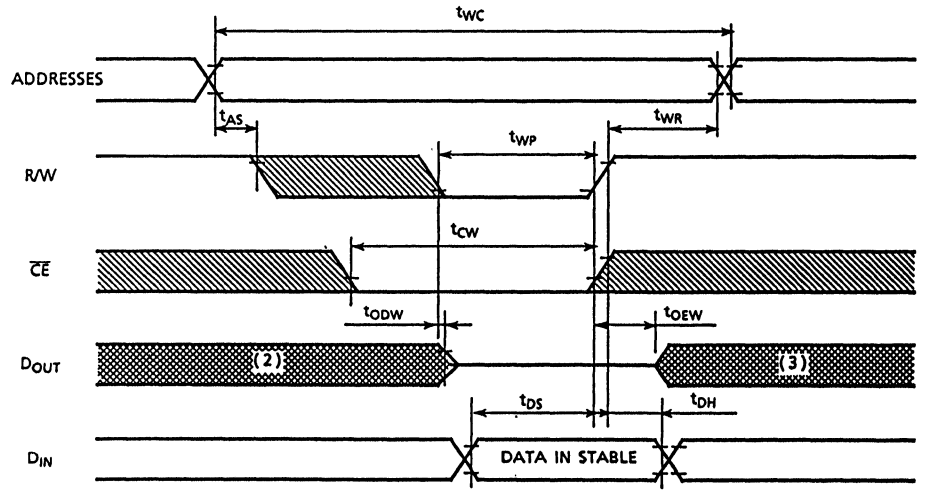
Output Load : 100pF + 1 TTL Gate
Input Pulse Level : 0.6V, 2.4V
Timing Measurement : 0.8V, 2.2V
Reference Level : 0.8V, 2.2V
t_r, t_f : 5ns

TIMING WAVEFROMS

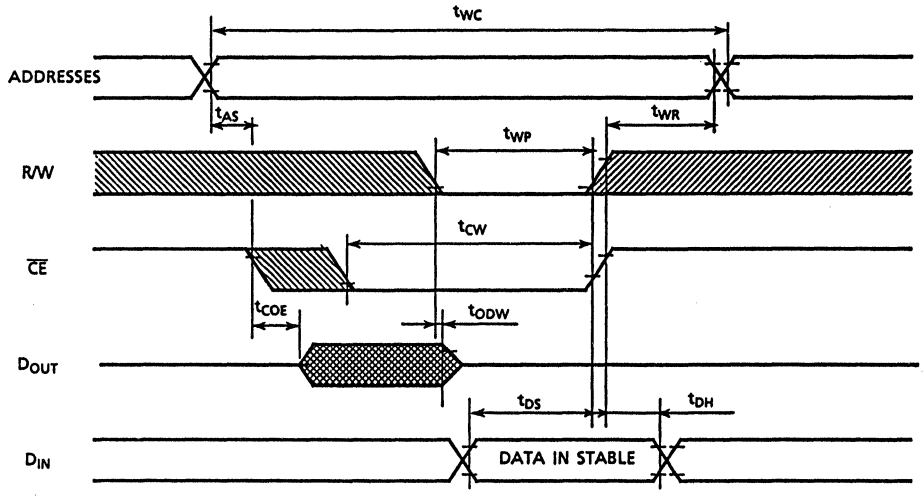
READ CYCLE (1)



WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}$ Controlled Write)



Note: 1. R/W is High for read cycle.

2. Assuming that $\overline{CE}$ low transition occurs coincident with or after R/W Low transition, Outputs remain a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R/W High transition, Outputs remain a high impedance state.

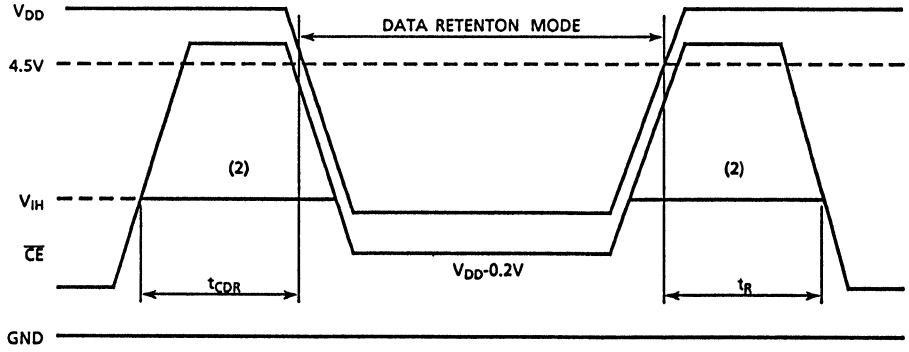
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	V_{DH} = 3.0V	-	-	20	µA
		V_{DH} = 5.5V	-	-	30	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	µS
t_R	Recovery Time		t_{RC} (1)	-	-	

Note (1): Read Cycle Time.

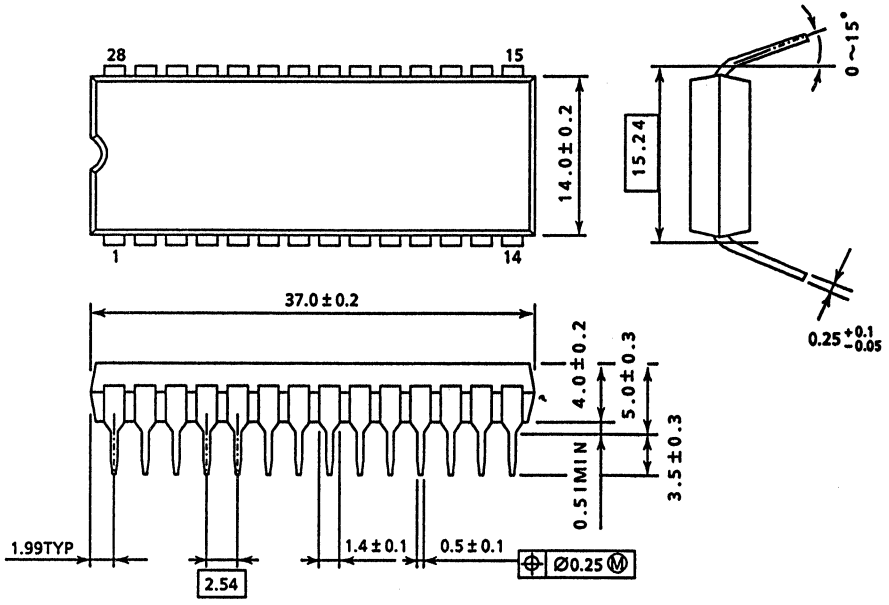
CE Controlled Data Retention Mode



Note (2): If the V_{IH} of $\overline{CE}$ is 2.2V in active operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

OUTLINE DRAWINGS (DIP28 - P - 600)

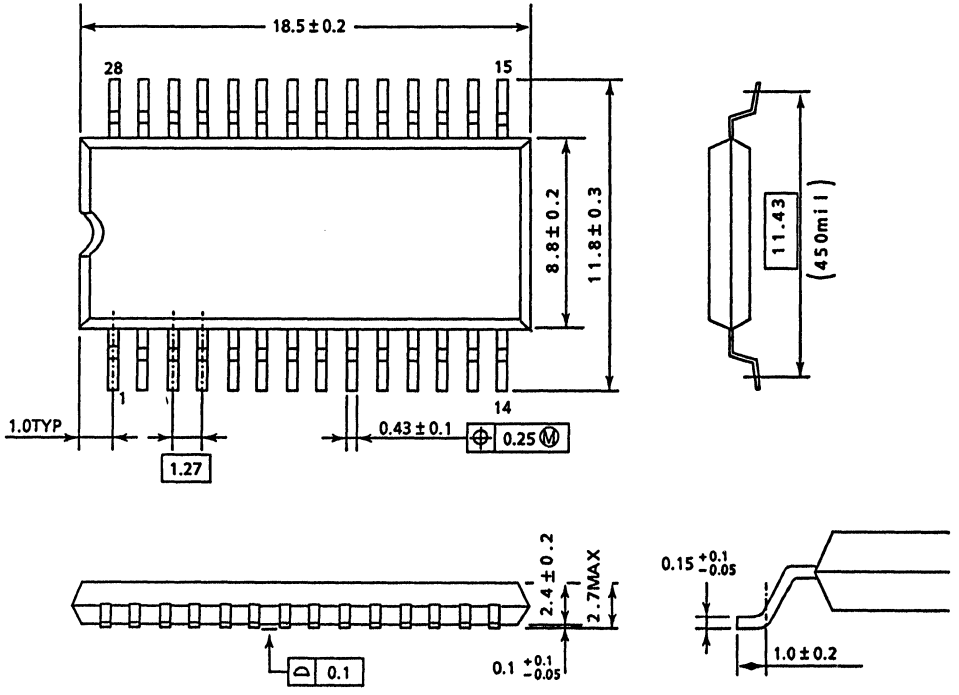
UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS (SOP28 – P – 450)

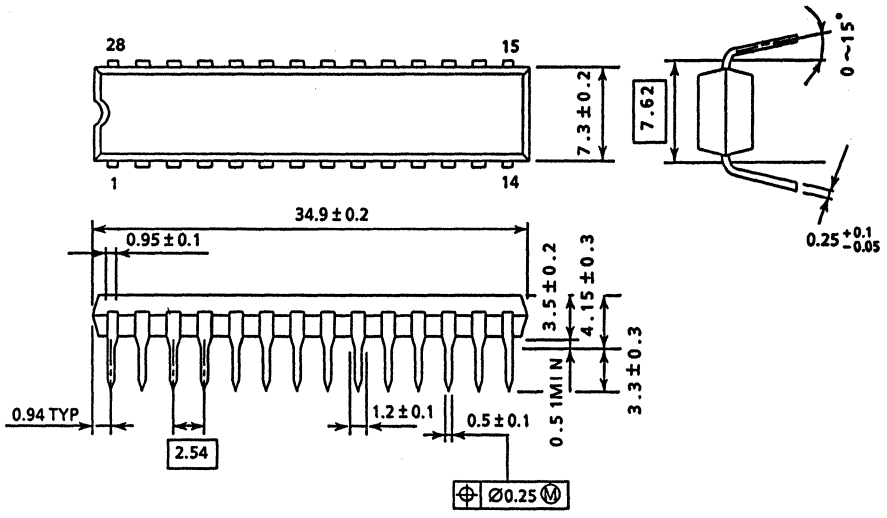
UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS (DIP28 - P - 300B)

UNIT: mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

32,768 WORDS × 8 BIT STATIC RAM

PRELIMINARY

DESCRIPTION

The TC55257BPI is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (Typ.) and maximum access time of 100ns. When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 2μA at room temperature.

The TC55257BPI has two control inputs. Chip enable ($\overline{CE}$) allows for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257BPI is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The TC55257BPI is guaranteed for a −40 ~ 85°C operating temperature range suitable for use in wide operating temperature systems.

The TC55257BPI is offered in both standard dual-in-line 28 pin 0.6 and 0.3 inch width plastic packages. The TC55257BFI is offered in a 28 pin 450 mil small outline plastic flat package.

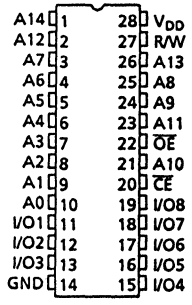
FEATURES

- **Low Power Dissipation**
  27.5mW/MHz (Typ.) Operating
- **Standby Current**
  2μA at Ta = 25°C (Max.) :
  TC55257BPI-10L/BFI-10L/BSPI-10L
- **5V Single Power Supply**
- **Power Down Feature : $\overline{CE}$**
- **Data retention Supply Voltage :**
  2.0V ~ 5.5V
- Wide Operating Temperature :
  −40 ~ 85°C
- **Access Time**

	TC55257BPI-10L TC55257BFI-10L TC55257BSPI-10L
Access Time (max.)	100ns
Chip Enable Access Time (max.)	100ns
Output Enable Time (Max.)	50ns

- **Directly TTL Compatible: All Inputs and Outputs**
- **Plastic DIP, Plastic FP and Plastic Slim Package**
  DIP, Plastic FP and Plastic Slim Package

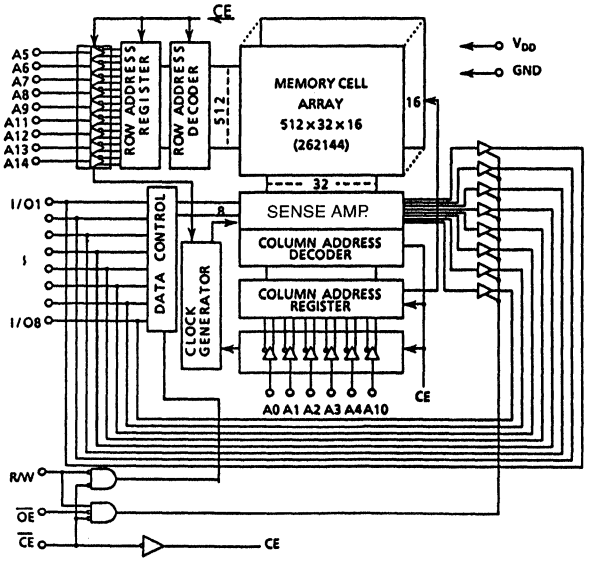
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A14	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1~I/O8	Data Input/Output
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1~I/O8	POWER
Read	L	L	H	D_{OUT}	I_{DDO}
Write	L	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	High-Z	I_{DDO}
Standby	H	*	*	High-Z	I_{DDS}

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5*~V_{DD}+0.5	V
P_D	Power Dissipation	1.0/0.8/0.6**	W
Tsolder	Soldering Temperature	260·10	°C·sec
Tstrg	Storage Temperature	−55~150	°C
Topr	Operating Temperature	−40~85	°C

*) −3.0V at pulse width 50ns
**) 0.6inch 1.0W, 0.3inch 0.8W, 0.45inch 0.6W

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	−0.3*	−	0.6	V
V_{DH}	Data Retention Supply Voltage	2.0	−	5.5	V

*) −3.0V at pulse width 50ns

D.C. and OPERATING CHARACTERISTICS (Ta = −40~85°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNITS
I_{IL}	Input Leakage Current	V_{IN} = 0 ~ V_{DD}		−	−	± 1.0	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		− 1.0	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		4.0	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or R/W = V_{IL} or $\overline{OE}$ = V_{IH} V_{OUT} = 0 ~ V_{DD}		−	−	± 1.0	μA
I_{DDO1}	Operating Current	$\overline{CE}$ = V_{IL} R/W = V_{IH} Other Input = V_{IH} / V_{IL} I_{OUT} = 0mA	t_{cycle} = 1μs	−	10	−	mA
			t_{cycle} = Min. cycle	−	−	70	
I_{DDO2}		$\overline{CE}$ = 0.2V R/W = V_{DD} − 0.2V Other Input = V_{DD} − 0.2V / 0.2V I_{OUT} = 0mA	t_{cycle} = 1μs	−	5	−	mA
			t_{cycle} = Min. cycle	−	−	60	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}		−	−	3	mA
I_{DDS2}	Standby Current	$\overline{CE}$ = V_{DD} − 0.2V V_{DD} = 2.0V~5.5V	Ta = −40~85°C	−	−	50	μA
			Ta = 25°C	−	−	2	

CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (T_a = −40~85°C, V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55257BPI-10L TC55257BFI-10L TC55257BSPI-10L		UNIT
		MIN.	MAX.	
t_{RC}	Read Cycle Time	100	–	ns
t_{ACC}	Address Access Time	–	100	
t_{CO}	$\overline{CE}$ Access Time	–	100	
t_{OE}	Output Enable to Output in Valid	–	50	
t_{COE}	Chip Enable ($\overline{CE}$) to Output in Low	5	–	
t_{OEE}	Output Enable to Output in Low-Z	0	–	
t_{OD}	Chip Enable ($\overline{CE}$) to Output in High-Z	–	50	
t_{ODO}	Output Enable to Output in High-Z	–	40	
t_{OH}	Output Data Hold Time	10	–	

WRITE CYCLE

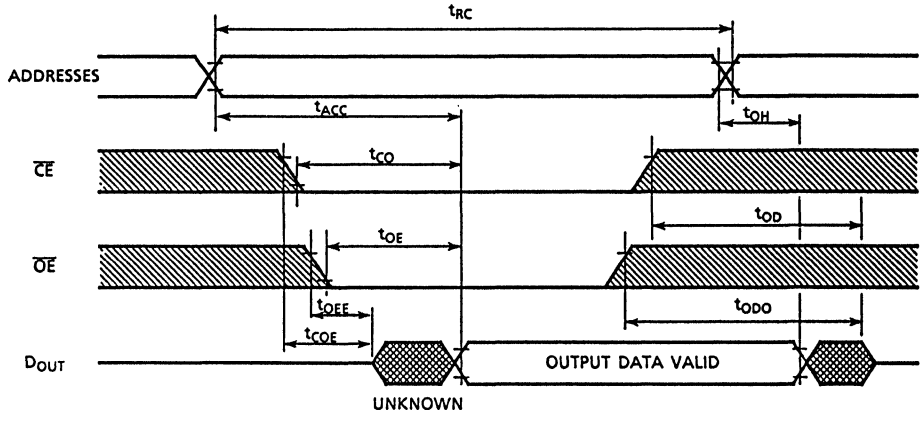
SYMBOL	PARAMETER	TC55257BPI-10L TC55257BFI-10L TC55257BSPI-10L		UNIT
		MIN.	MAX.	
t_{WC}	Write Cycle Time	100	–	ns
t_{WP}	Write Pulse Width	70	–	
t_{CW}	Chip Selection to End of Write	90	–	
t_{AS}	Address Set up Time	0	–	
t_{WR}	Write Recovery Time	5	–	
t_{ODW}	R/W to Output High-Z	–	50	
t_{OEW}	R/W to Output Low-Z	0	–	
t_{DS}	Data Set up Time	40	–	
t_{DH}	Data Hold Time	0	–	

A.C. TEST CONDITIONS

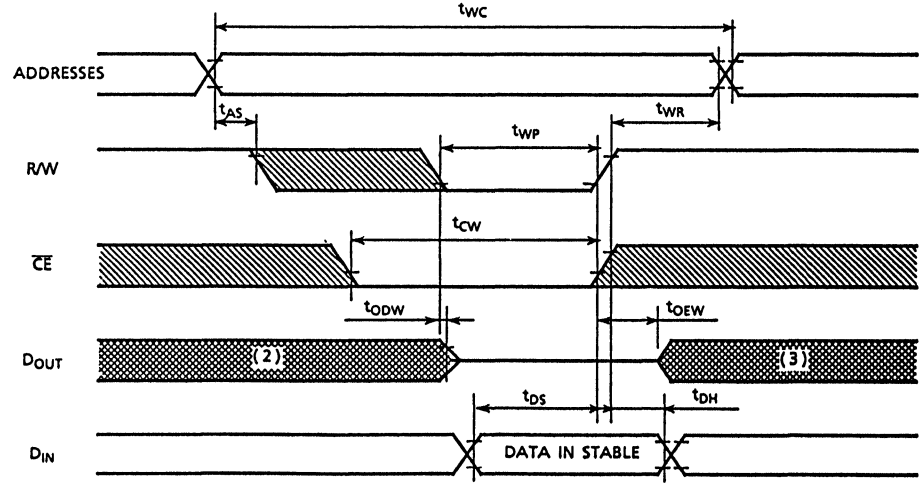
Output Load : 100pF + 1 TTL Gate
Input Pulse Level : 0.4V, 2.6V
Timing Measurement : 0.6V, 2.4V
Reference Level : 0.8V, 2.2V
t_r, t_f : 5ns

TIMING WAVEFROMS

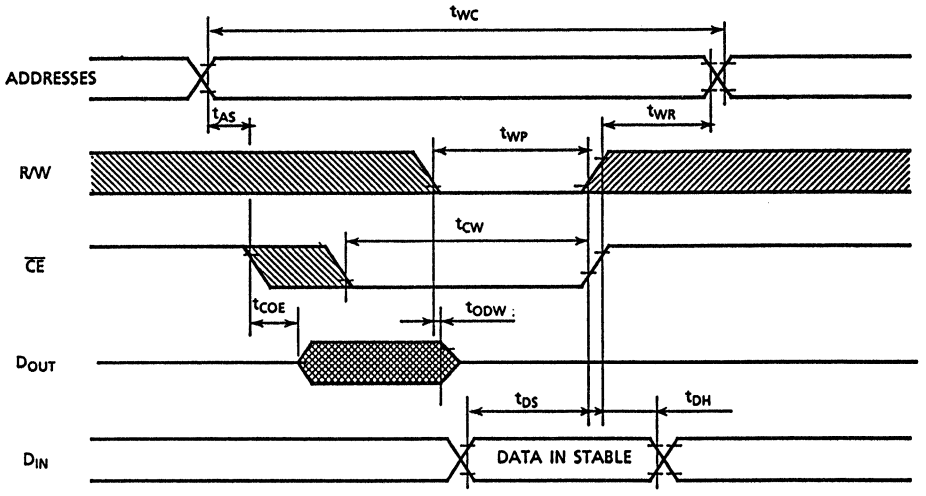
READ CYCLE (1)



WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 (4) ($\overline{CE}$ Controlled Write)



Note: 1. R/W is High for read cycle.

2. Assuming that $\overline{CE}$ low transition occurs coincident with or after R/W Low transition, Outputs remain a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to R/W High transition, Outputs remain a high impedance state.

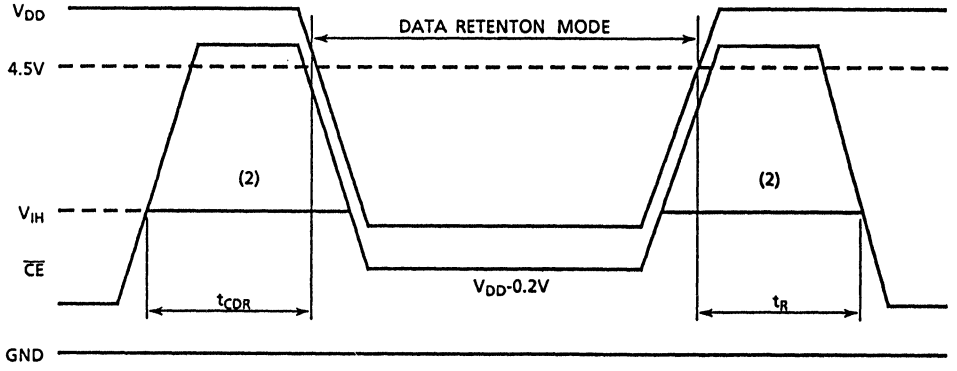
4. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

DATA RETENTION CHARACTERISTICS (Ta = −40~85°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	−	5.5	V
I_{DDS2}	Standby Supply Current	V_{DH} = 3.0V	−	−	30	µA
		V_{DH} = 5.5V	−	−	50	
t_{CDR}	Chip Deselection to Data Retention Mode		0	−	−	µS
t_R	Recovery Time		t_{RC} (1)	−	−	

Note (1): Read Cycle Time.

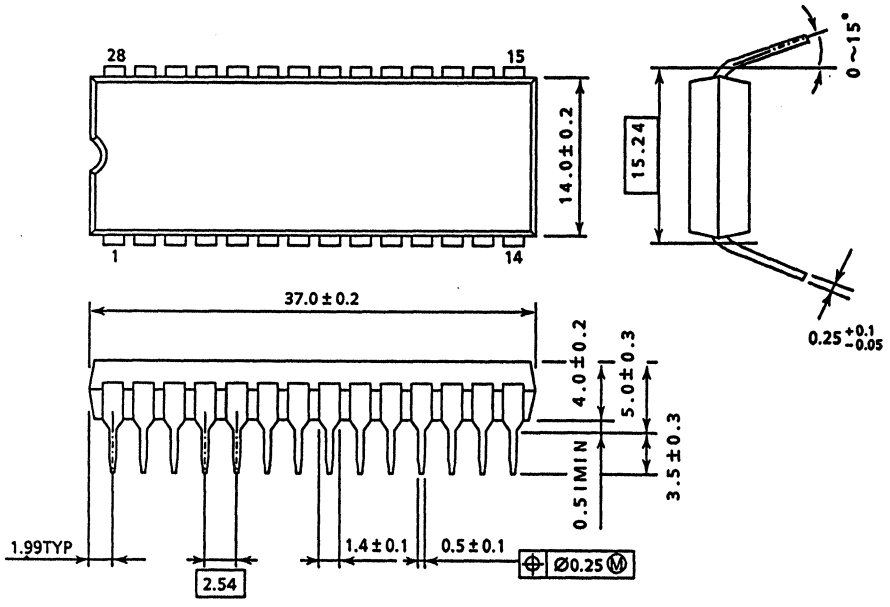
CE Controlled Data Retention Mode



Note (2): If the V_{IH} of $\overline{CE}$ is 2.4V in active operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

OUTLINE DRAWINGS (DIP28 - P - 600)

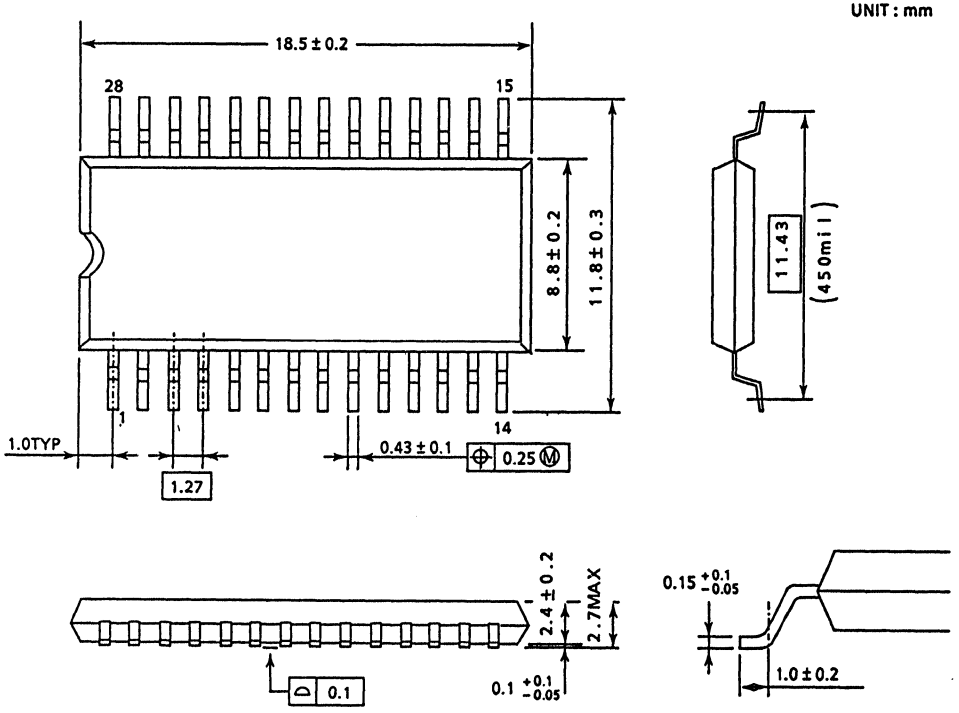
UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS (SOP28 - P - 450)

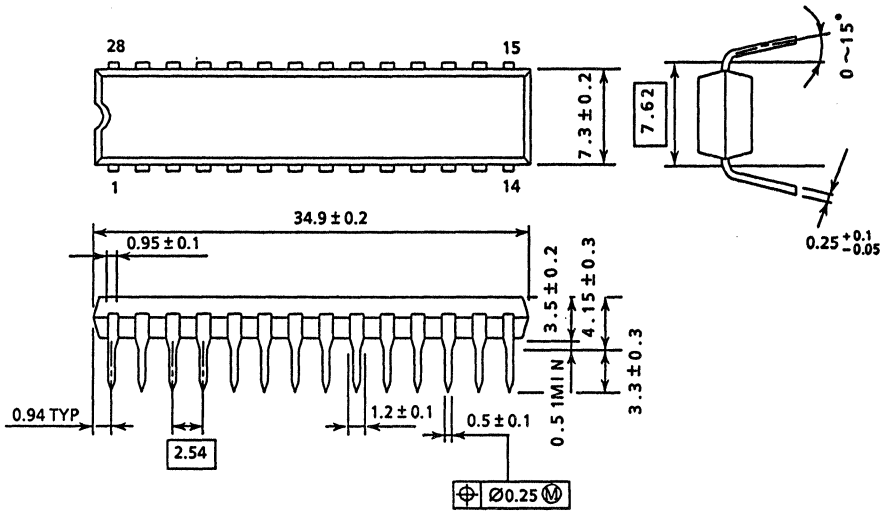
UNIT : mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS (DIP28 – P – 300B)

UNIT: mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

32,768 WORDS × 8 BIT STATIC RAM

PRELIMINARY

DESCRIPTION

The TC551001PL/FL is a 1,048,576 bit static random access memory organized as 131,072 words by 8 bits using CMOS technology, and operates from a single 5V power supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5mA/MHz (Typ.) and minimum cycle time of 85/100ns. When $\overline{CE1}$ is a logical high, or CE2 is a logical low, the device is placed in low power standby mode in which standby current is 2μA typically. The TC551001PL/FL has three control inputs. Chip enable inputs ($\overline{CE1}$,CE2) allow for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC551001PL/FL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required.

The TC551001PL is offered in a dual-in-line standard 32 pin 600 mil plastic package. The TC551001FL is offered in a 32 pin 525 mil small-outline plastic flat package.

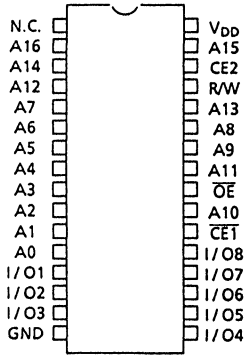
FEATURES

- Low Power Dissipation
  27.5mW / MHz (Typ.)
- Standby Current: 100μA (Max.)
- 5V Single Power Supply
- Power Down Feature: $\overline{CE1}$, CE2
- Data retention Supply Voltage: 2.0 ~ 5.5V
- Access Time

	TC551001 PL/FL-85	TC551001 PL/FL-10
Access Time (max.)	85ns	100ns
$\overline{CE1}$ Access Time (max.)	85ns	100ns
CE2 Access Time (max.)	85ns	50ns
$\overline{OE}$ Access Time (max.)	45ns	50ns

- Directly TTL Compatible: All Inputs and Outputs
- Plastic DIP, Plastic Flat Package

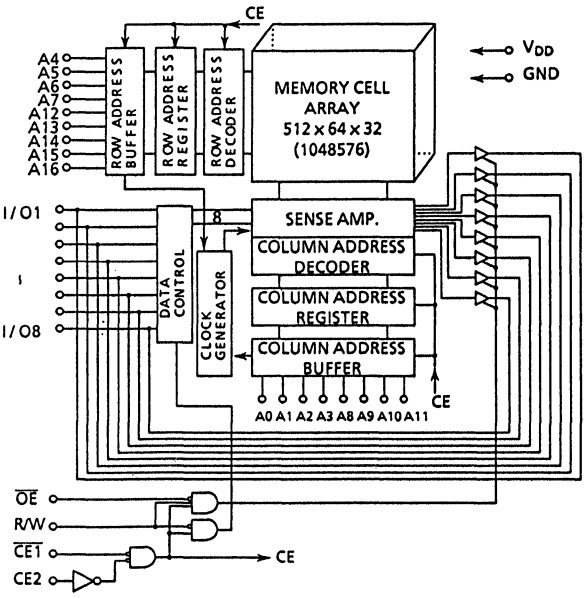
PIN CONNECTION (TOP VIEW)



PIN NAMES

A0~A16	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE1}$,CE2	Chip Enable Input
I/O1~I/O8	Data Input / Output
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	POWER
Read	L	H	L	H	D_{OUT}	I_{DDO}
Write	L	H	*	L	D_{IN}	I_{DDO}
Output Deselect	L	H	H	H	High-Z	I_{DDO}
Standby	H	*	*	*	High-Z	I_{DDS}
	*	L	*	*	High-Z	I_{DDS}

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5 ~ V_{DD} + 0.5	V
P_D	Power Dissipation	1.0 / 0.6**	W
Tsolder	Soldering Temperature	260 · 10	°C · sec
Tstrg.	Storage Temperature	−55 ~ 150	°C
Topr.	Operating Temperature	0 ~ 70	°C

*: −3.0V at pulse width 50ns MAX.

**: SOP

D.C. RECOMMENDED OPERATING CONDITIONS.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD} + 0.3	
V_{IL}	Input Low Voltage	−0.3*	−	0.8	
V_{DH}	Data Retention Supply Voltage	2.0	−	5.5	

*: −3.0V at pulse width 50ns MAX.

D.C. and OPERATING CHARACTERISTICS ($Ta = 0 \sim 70\,°C$, $V_{DD} = 5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	-	-	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4V$	- 1.0	-	-	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4V$	4.0	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	-	-	± 1.0	μA
I_{DDO1}	Operating Current	$\overline{CE1} = V_{IL}$ and $CE2 = V_{IH}$ and $R/W = V_{IH}$, $I_{OUT} = 0mA$ Other Inputs = V_{IH}/V_{IL} t_{cycle} = Min. cycle	-	-	80	mA
I_{DDO2}		$\overline{CE1} = 0.2V$ and $CE2 = V_{DD} - 0.2V$ $R/W = V_{DD} - 0.2V$, $I_{OUT} = 0mA$ Other Inputs = $V_{DD} - 0.2V / 0.2V$ t_{cycle} = Min. cycle	-	-	70	mA
I_{DDS1}	Standby Current	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$	-	-	3	mA
I_{DDS2} (1)		$\overline{CE1} = V_{DD} - 0.2V$ or $CE2 = 0.2V$ $V_{DD} = 2.0V \sim 5.5V$, $Ta = 0 \sim 70°C$	-	2	100	μA

Note : (1) In standby mode with $\overline{CE1} \geqq V_{DD} - 0.2V$, these specification limits are guaranteed under the condition of $CE2 \geqq V_{DD} - 0.2V$ or $CE2 \leqq 0.2V$.

CAPACITANCE ($Ta = 25°C$, $f = 1MHz$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = GND$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = GND$	10	

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS (Ta = 0 ~ 70°C, V_{DD} = 5V ± 10%)

Read Cycle

SYMBOL	PARAMETER	TC551001PL-85 TC551001FL-85		TC551001PL-10 TC551001FL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	-	100	-	ns
t_{ACC}	Address Access Time	-	85	-	100	
t_{CO1}	$\overline{CE1}$ Access Time	-	85	-	100	
t_{CO2}	CE2 Access Time	-	85	-	100	
tOE	Output Enable to Output in Valid	-	45	-	50	
t_{COE}	Chip Enable ($\overline{CE1}$, CE2) to Output in Low-Z	10	-	10	-	
t_{OEE}	Output Enable to Output in Low-Z	0	-	0	-	
t_{OD}	Chip Enable ($\overline{CE1}$, CE2) to Output in High-Z	-	30	-	35	
t_{ODO}	Output Enable to Output in High-Z	-	30	-	35	
t_{OH}	Output Data Hold Time	10	-	10	-	

Write Cycle

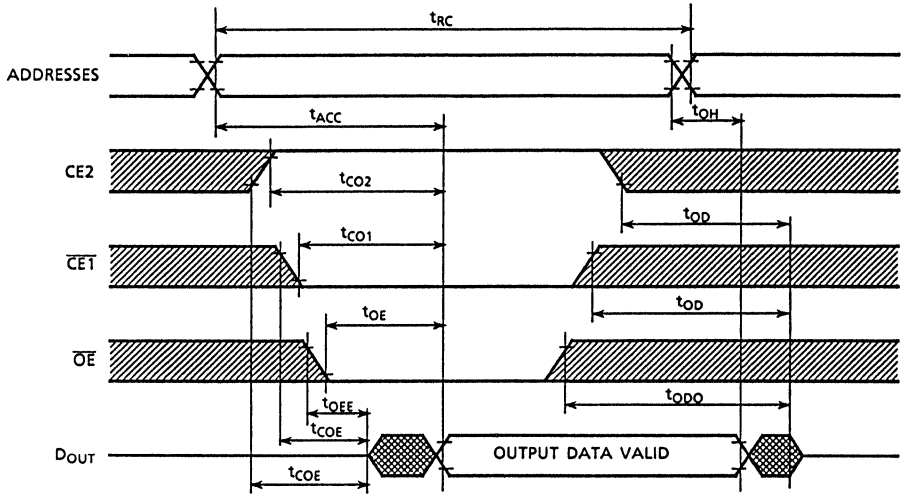
SYMBOL	PARAMETER	TC551001PL-85 TC551001FL-85		TC551001PL-10 TC551001FL-10		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	-	100	-	ns
t_{WP}	Write Pulse Width	60	-	60	-	
t_{CW}	Chip Selection to End of Write	75	-	80	-	
t_{AS}	Address Set up Time	0	-	0	-	
t_{WR}	Write Recovery Time	0	-	0	-	
t_{ODW}	R/W to Output in High-Z	-	30	-	35	
t_{OEW}	R/W to Output in Low-Z	0	-	0	-	
t_{DS}	Data Set up Time	35	-	40	-	
t_{DH}	Data Hold Time	0	-	0	-	

A.C. TEST CONDIONS

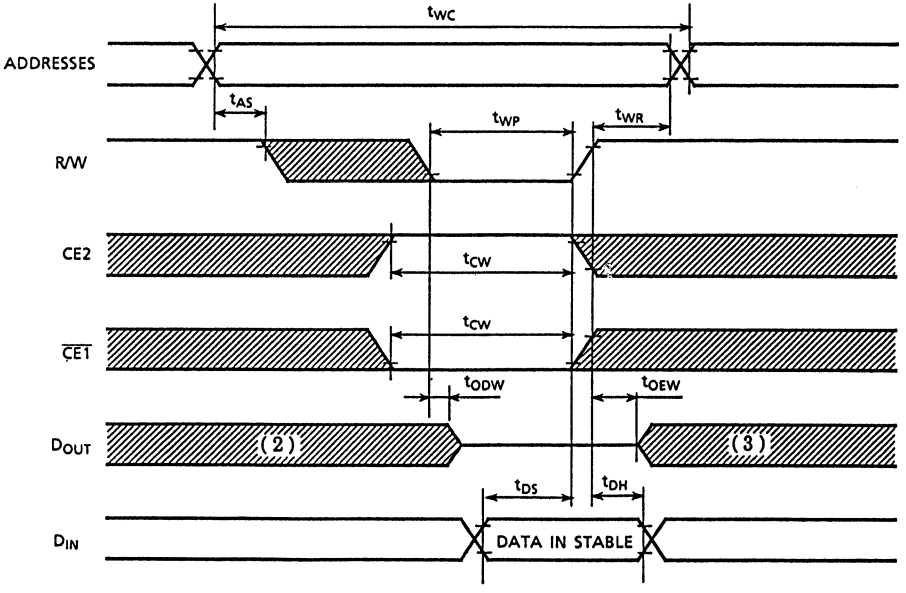
- Output Load : 100pF+1 TTL Gate
- Input Pulse Level : 0.6V, 2.4V
- Timing Measurement V_{IN} : 0.8V, 2.2V
  Reference Level V_{OUT} : 0.8V, 2.2V
- t_r, t_f : 5ns

TIMING WAVEFROMS

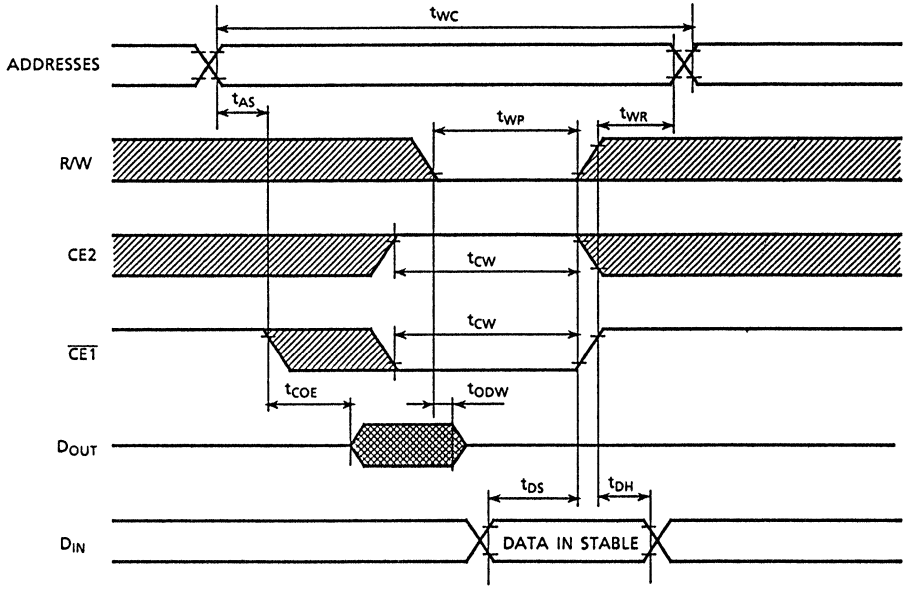
READ CYCLE (1)



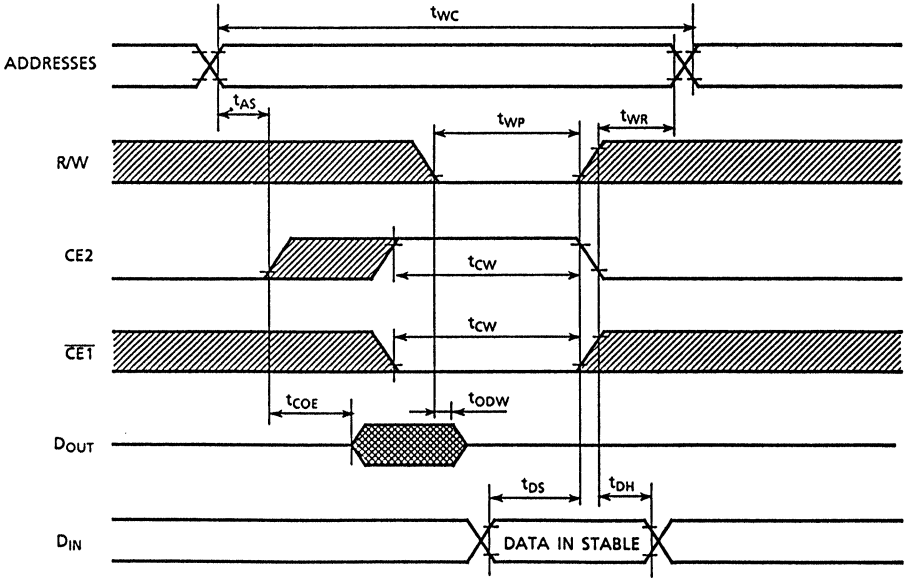
WRITE CYCLE 1 (4) (R/W Controlled Write)



WRITE CYCLE 2 [4] ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 [4] (CE2 Controlled Write)



NOTE:

(1) R/W is High for Read Cycle.

(2) Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after R/W Low transition, Outputs remain in a high impedance state.

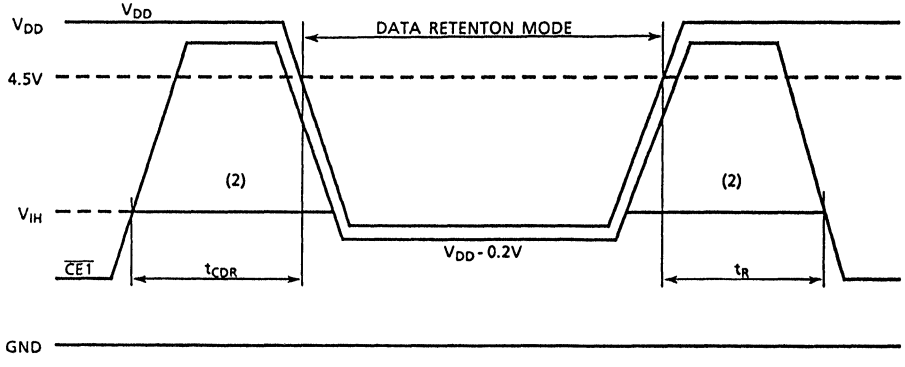
(3) Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to R/W High transition, outputs remain in a high impedance state.

(4) Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in high impedance state during this period.

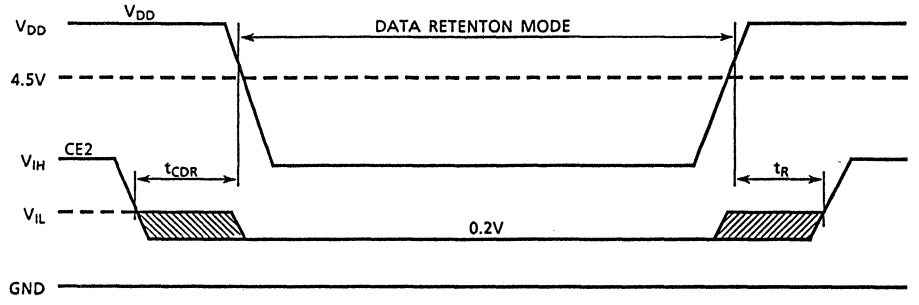
DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70 °C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Current	V_{DD} = 3.0V	-	-	50	µA
		V_{DD} = 5.5V	-	-	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	nS
t_R	Recovery Time		5	-	-	mS

$\overline{CE1}$ Controlled Data Retention Mode (1)



CE2 Controlled Data Retention Mode (3)



NOTE:

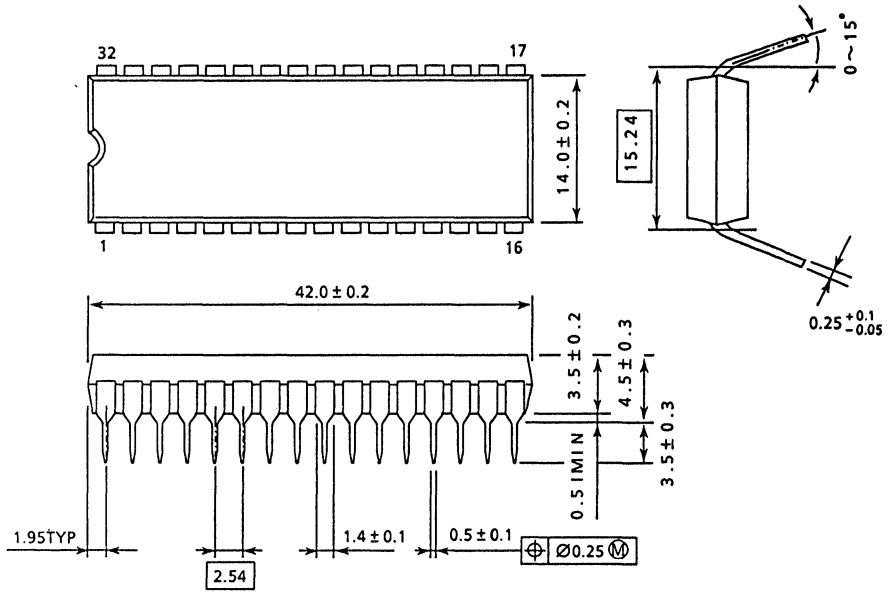
(1) In $\overline{CE1}$ controlled data retention mode, minmum standby current mode is achieved under the condition of CE2 ≦ 0.2V or CE2 ≧ V_{DD} − 0.2V.

(2) If the V_{IH} of $\overline{CE1}$ is 2.2V in active operation, during the period that the V_{DD} voltage is going down from 4.5V to 2.4V, I_{DDS1} current flows.

(3) In CE2 controlled data retention mode, minimum standby current mode is achieved under the condition of CE2 ≦ 0.2V.

OUTLINE DRAWING (DIP32 – P – 600)

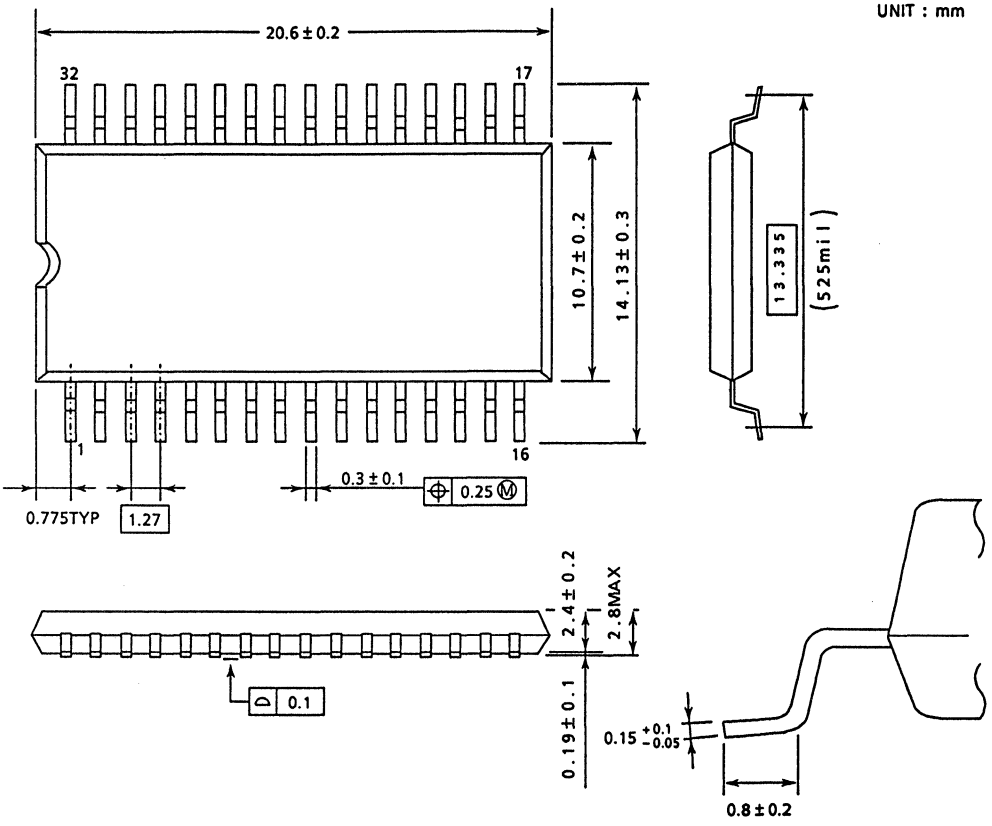
UNIT : mm



Note: Package width and length do not include mold protrusion. Allowable mold protrusion is 0.15mm.

OUTLINE DRAWING (SOP32 - P - 525)

UNIT : mm



Note: Package width and length do not include mold protrusion. Allowable mold protrusion is 0.15mm.

CMOS High Speed Static RAM

65,536 WORD x 1 BIT CMOS STATIC RAM

DESCRIPTION

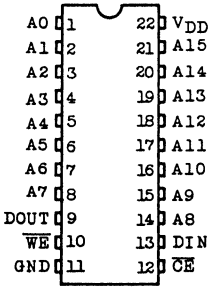
The TC5561P/J is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and operates from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 45ns/55ns/70ns and maximum operating current of 100mA at minimum cycle time. The TC5561P/J also features an automatic stand-by mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced from 100mA to 2mA. The TC5561P/J is suitable for use in main memory of high speed computer and pattern memory, where high speed/low power/high density are required. The TC5561P is offered in a 22 pin plastic DIP with 300 mil width for high density assembly and the TC5561J is offered in a 24 pin plastic SOJ with 300 mil width for high density surface assembly.
The TC5561P/J is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time: TC5561P/J-45 45ns(MAX.)
  TC5561P/J-55 55ns(MAX.)
  TC5561P/J-70 70ns(MAX.)
- Low power dissipation: Operation 100mA(MAX.)
  Standby 2mA(MAX.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible:
  All Inputs and Output
- I/O separate
- Package: 22 Pin plastic 300 mil DIP
  : TC5561P
  24 Pin plastic 300 mil SOJ
  : TC5561J

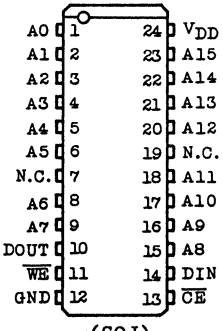
PIN CONNECTION

TC5561P
(TOP VIEW)



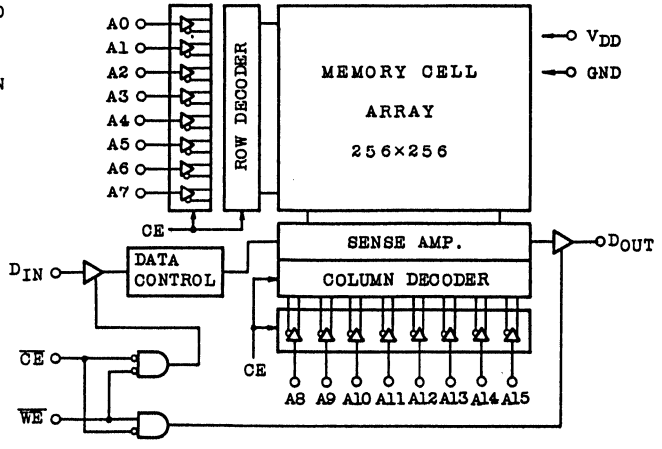
(DIP)

TC5561J
(TOP VIEW)



(SOJ)

BLOCK DIAGRAM



PIN NAMES

A0 ∿ A15	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ∿ 7.0	V
V_{IN}	Input Voltage	-2.0 ∿ 7.0	V
V_{OUT}	Output Voltage	-0.5 ∿ V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{solder}	Soldering Temperature	260 · 10	°C · sec
T_{stg}	Storage Temperature	-65 ∿ 150	°C
T_{opr}	Operating Temperature	0 ∿ 70	°C

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V
V_{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

D.C. and OPERATING CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$	-	-	±1.0	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$	-8	-	-	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$	8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{OUT}=0 \sim V_{DD}$	-	-	±1.0	μA
I_{DDO}	Operating Current	$V_{DD}=5.5V$, t_{cycle}=Min cycle $\overline{CE}=V_{IL}$ Other Input=V_{IH}/V_{IL}	-	-	100	mA
I_{DDS1}	Standby Current	$\overline{CE}=V_{IH}$	-	-	2	mA
I_{DDS2}		$\overline{CE}=V_{DD}-0.2V$	-	-	100	μA

CAPACITANCE ($Ta=25°C$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A.C. CHARACTERISTICS ($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

Read cycle

SYMBOL	PARAMETER	TC5561P-45 TC5561J-45		TC5561P-55 TC5561J-55		TC5561P-70 TC5561J-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	45	-	55	-	70	-	ns
t_{ACC}	Address Access Time	-	45	-	55	-	70	ns
t_{CO}	Chip Enable Access Time	-	45	-	55	-	70	ns
t_{COE}	Chip Enable to Output in Low-Z	5	-	5	-	5	-	ns
t_{COD}	Chip Enable to Output in High-Z	-	15	-	15	-	15	ns
t_{OH}	Output Data Hold Time	5	-	5	-	5	-	ns

Write cycle

SYMBOL	PARAMETER	TC5561P-45 TC5561J-45		TC5561P-55 TC5561J-55		TC5561P-70 TC5561J-70		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	45	-	55	-	70	-	ns
t_{WP}	Write Pulse Width	30	-	35	-	35	-	ns
t_{CW}	Chip Enable to End of Write	30	-	35	-	35	-	ns
t_{AW}	Address Set up Time	0	-	0	-	0	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{ODW}	$\overline{WE}$ to Output High-Z	-	15	-	15	-	15	ns
t_{OEW}	$\overline{WE}$ to Output Low-Z	0	-	0	-	0	-	ns
t_{DS}	Data Set up Time	25	-	25	-	30	-	ns
t_{DH}	Data Hold Time	0	-	0	-	0	-	ns

A.C. TEST CONDITIONS

Input Pulse Levels	0.6V, 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

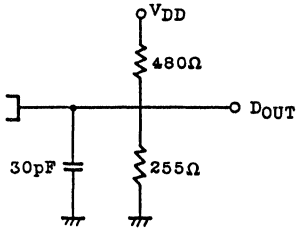
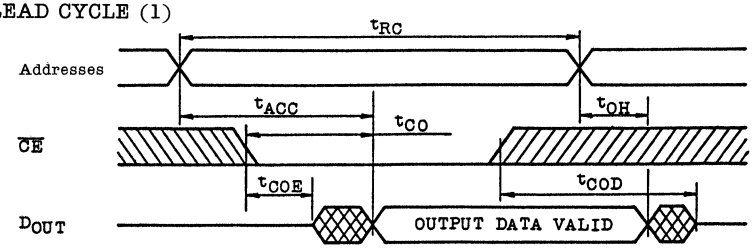


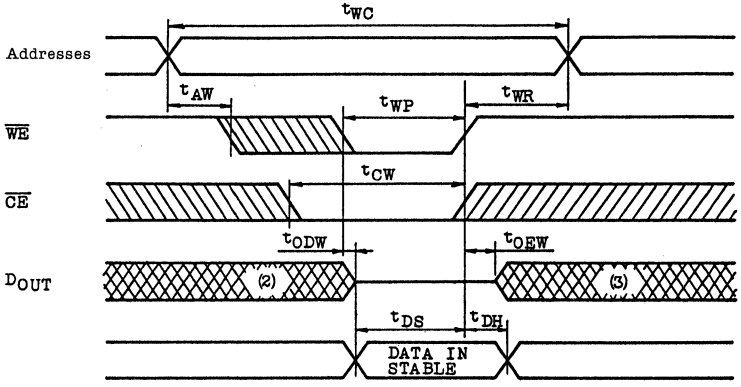
Fig.1 Output Load

TIMING WAVEFORMS

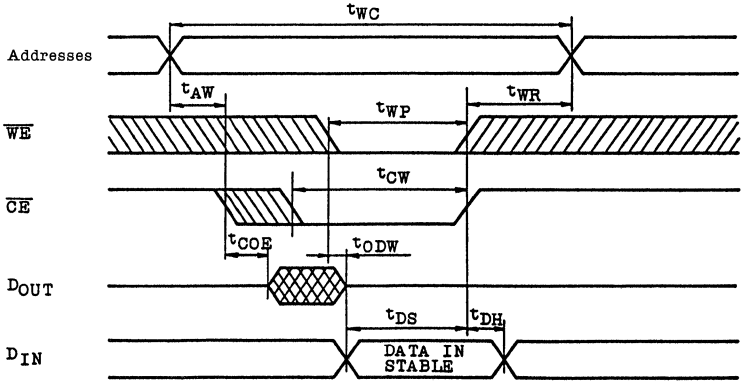
READ CYCLE (1)



WRITE CYCLE 1 ($\overline{WE}$ Controled Write)



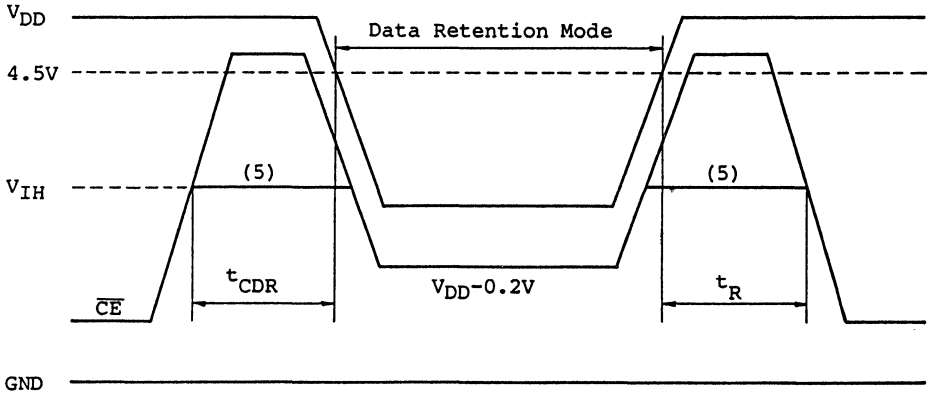
WRITE CYCLE 2 ($\overline{CE}$ Controled Write)



Note: 1. R/W is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincidently or after $\overline{WE}$ Low transition, outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincidently or prior to $\overline{WE}$ High transition, outputs remain in a high impedance state.
4. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

DATA RETENTION CHARACTERISTICS (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage		2.0	-	5.5	V
I_{DDS2}	Standby Supply Current	V_{DD}=3.0V	-	-	50	μA
		V_{DD}=5.5V	-	-	100	
t_{CDR}	Chip Deselection to Data Retention Mode		0	-	-	ns
t_R	Recovery Time	TC5561P-45	45	-	-	ns
		TC5561P-55	55	-	-	
		TC5561P-70	70	-	-	

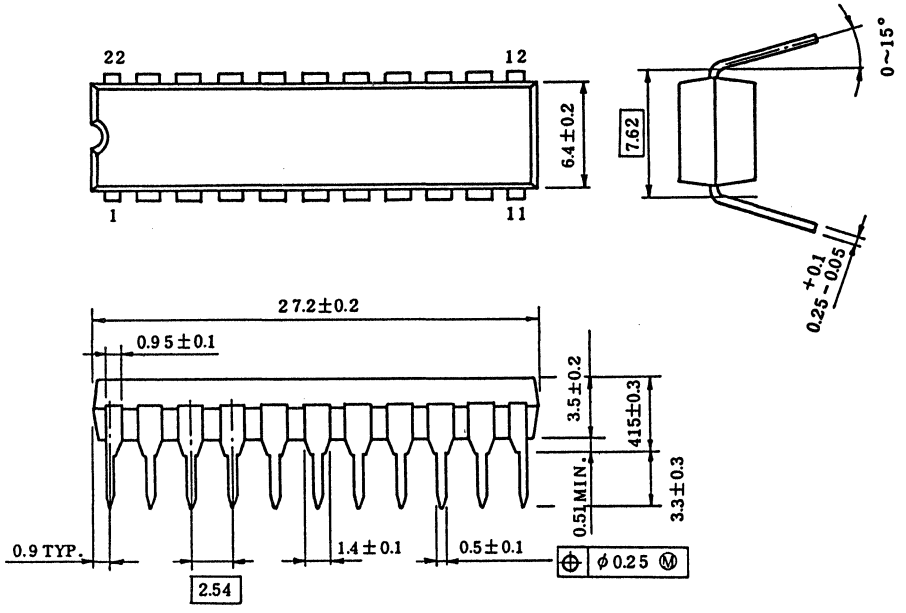


Note: 5. If the V_{IH} of $\overline{CE}$ is 2.2V in active operation, I_{DDS1} current flows during the period that the V_{DD} voltage is going down from 4.5V to 2.4V.

OUTLINE DRAWINGS

Unit in mm

• Plastic DIP (DIP22-P-300)

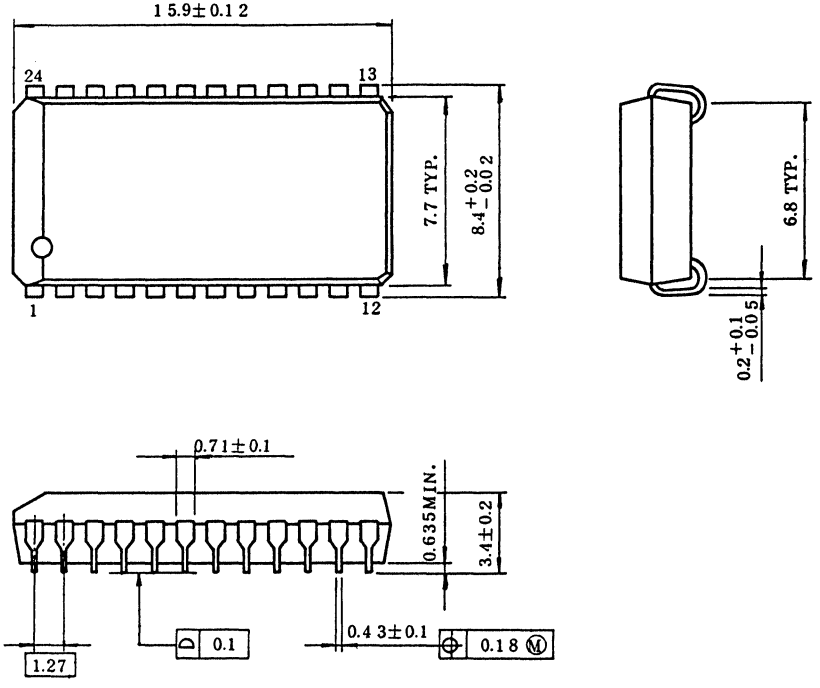


Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

• Plastic SOJ (SOJ24-P-300)

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

65,536 WORD x 1 BIT CMOS STATIC RAM

DESCRIPTION

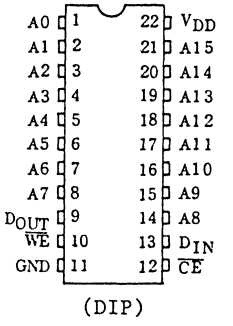
The TC5562P/J is a 65,536 bit high speed static random access memory organized as 65,536 words by 1 bit using CMOS technology, and operates from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 35ns/45ns and maximum operating current of 100mA at minimum cycle time. The TC5562P/J also features an automatic standby mode. When deselected by chip Enable ($\overline{CE}$), the operating current is reduced from 100mA to 20mA. The TC5562P/J is suitable for use in main memory of high speed computer and pattern memory, where high speed/high density are required. The TC5562P is offered in a 22 pin plastic DIP with 300 mil width for high density surface assembly and the TC5562J is offered in a 24 pin plastic SOJ with 300 mil width for high density surface assembly. The TC5562P/J is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast Access time: TC5562P/J-35 35ns(MAX.)
  TC5562P/J-45 45ns(MAX.)
- Low power dissipation:
  Operation 100mA (MAX.)
  Standby 20mA (MAX.)
- 5V single power supply
- Fully static operation
- Directly TTL compatible: All Inputs and Output
- I/O separate
- Package: 22 Pin Plastic 300 mil DIP : TC5562P
  24 Pin Plastic 300 mil SOJ : TC5562J

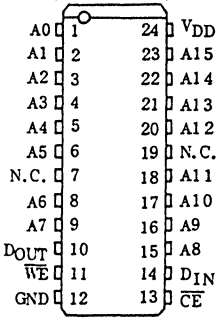
PIN CONNECTION

TC5562P (TOP VIEW)



(DIP)

TC5562J (TOP VIEW)

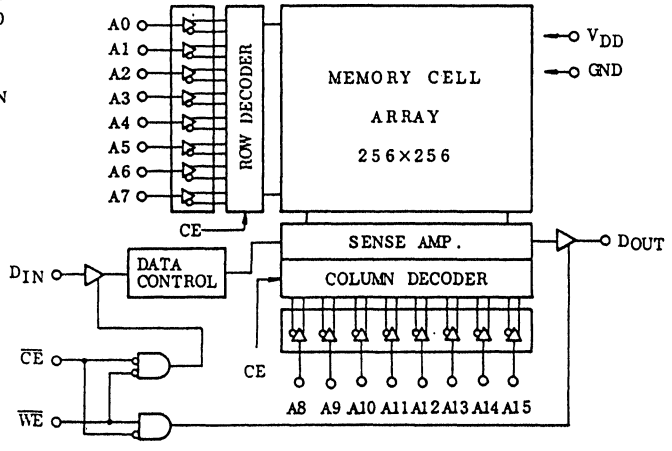


(SOJ)

PIN NAMES

A0 ∿ A15	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.3 ∿ 7.0	V
V_{IN}	Input Voltage	-2.0 ∿ 7.0	V
V_{OUT}	Output Voltage	-0.5 ∿ V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{solder}	Soldering Temperature	260 • 10	°C • sec
T_{stg}	Storage Temperature	-65 ∿ 150	°C
T_{opr}	Operating Temperature	0 ∿ 70	°C

D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

D.C. ELECTRICAL CHARACTERISTICS

($Ta=0 \sim 70°C$, $V_{DD}=5V \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0 \sim V_{DD}$	-	-	±1	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$	-8	-	-	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$	8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{OUT}=0 \sim V_{DD}$	-	-	±1	μA
I_{DDO}	Operating Current	$V_{DD}=5.5V$, t_{cycle}=Min cycle, $\overline{CE}=V_{IL}$ Other Input=V_{IH}/V_{IL}	-	-	100	mA
I_{DDS1}	Standby Current	$V_{DD}=5.5V$, t_{cycle}=Min cycle $\overline{CE}=V_{IH}$ Other Input=V_{IH}/V_{IL}	-	-	20	mA
I_{DDS2}		$\overline{CE}=V_{DD}-0.2V$ Other Input $V_{DD}-0.2V$ or $0.2V$	-	-	2	

CAPACITANCE

($Ta=25°C$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

A. C. CHARACTERISTICS (Ta=0 ∿ 70°C, V_{DD}=5V±10%)

READ CYCLE

SYMBOL	PARAMETER	TC5562P-35 TC5562J-35		TC5562P-45 TC5562J-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	35	-	45	-	ns
t_{ACC}	Address Access Time	-	35	-	45	ns
t_{CO}	Chip Enable Access Time	-	35	-	45	ns
t_{COE}	Chip Enable to Output in Low-Z	5	-	5	-	ns
t_{COD}	Chip Enable to Output in High-Z	-	15	-	15	ns
t_{OH}	Output Data Hold Time	5	-	5	-	ns

WRITE CYCLE

SYMBOL	PARAMETER	TC5562P-35 TC5562J-35		TC5562P-45 TC5562J-45		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	35	-	45	-	ns
t_{WP}	Write Pulse Width	25	-	30	-	ns
t_{CW}	Chip Enable to End of Write	25	-	30	-	ns
t_{AW}	Address Set up Time	0	-	0	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	ns
t_{ODW}	$\overline{WE}$ to Output High-Z	-	15	-	15	ns
t_{OEW}	$\overline{WE}$ to Output Low-Z	0	-	0	-	ns
t_{DS}	Data Set up Time	20	-	25	-	ns
t_{DH}	Data Hold Time	0	-	0	-	ns

A.C. TEST CONDITIONS

Input Pulse Levels	0.6V, 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1

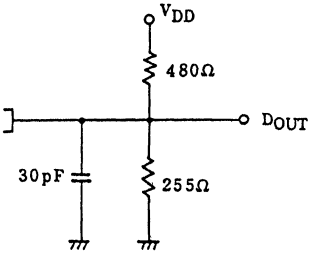
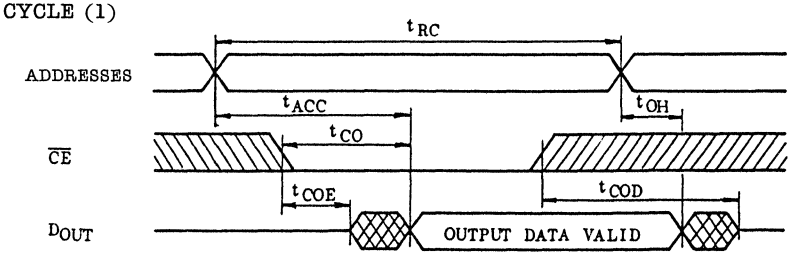


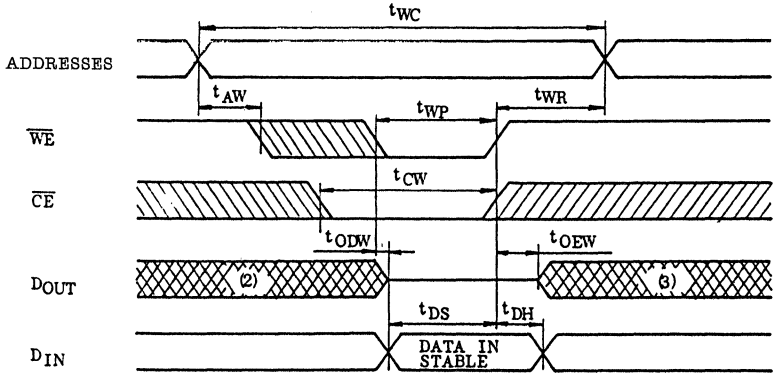
Fig. 1 Output Load

TIMING WAVEFORMS

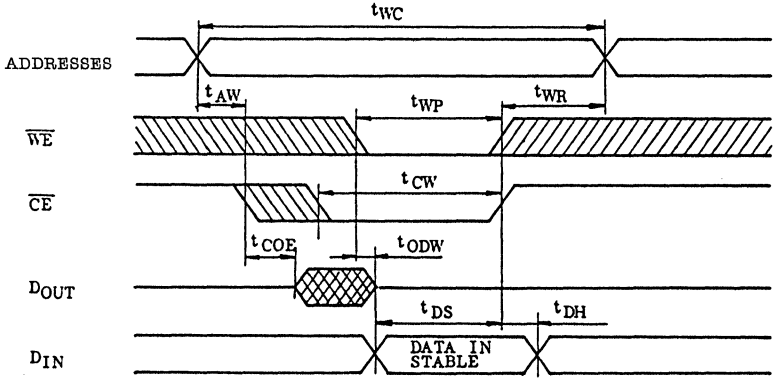
READ CYCLE (1)



WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)

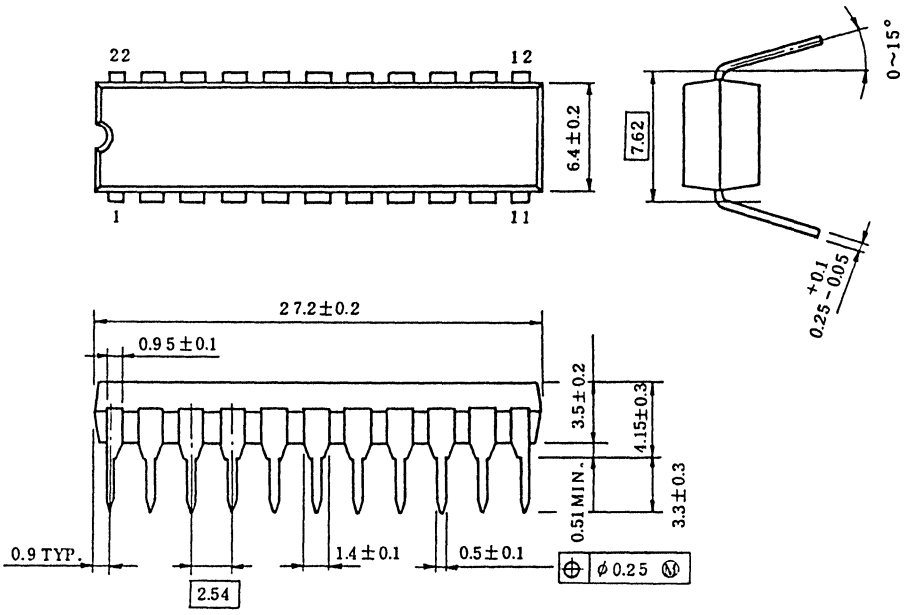


Note: 1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CE}$ Low transition occurs coincidently or after $\overline{WE}$ Low transition, outputs remain in a high impedance state.
3. Assuming that $\overline{CE}$ High transition occurs coincidently or prior to $\overline{WE}$ High transition, outputs remain in a high impedance state.
4. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

OUTLINE DRAWINGS

• Plastic DIP (DIP22-P-300)

Unit in mm

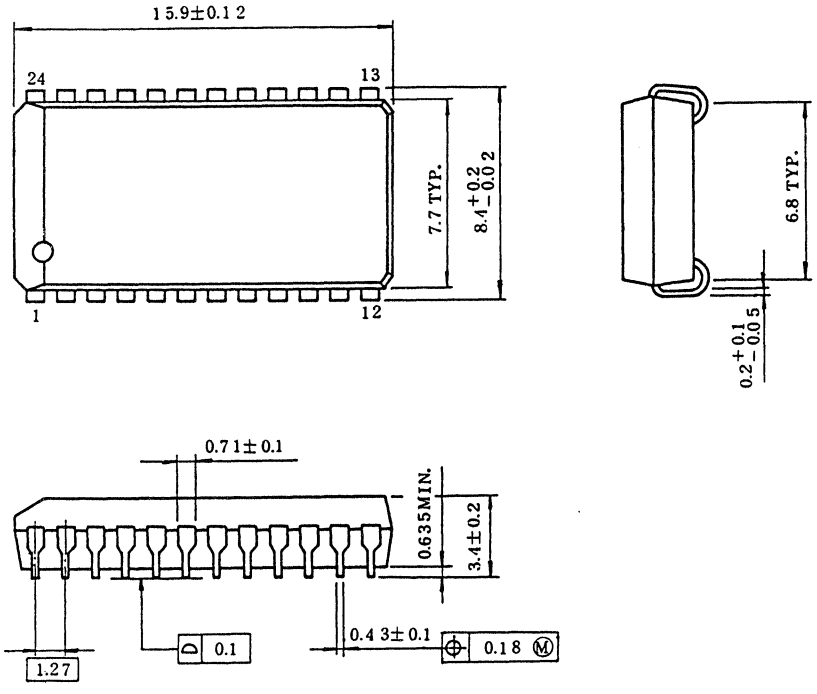


Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

• Plastic SOJ (SOJ24-P-300)

Unit in mm



Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

8,192 WORD × 8 BIT CMOS STATIC RAM

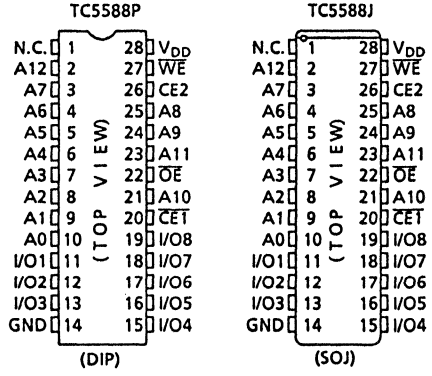
DESCRIPTION

The TC5588P/J is a 65,536 bit high-speed static random access memory organized as 8,192 words by 8 bits using CMOS technology, and operates from a single 5 volt supply. Toshiba's advanced CMOS circuitry provides high-speed characteristics. The TC5588P/J has low stand-by power using Chip Enables ($\overline{CE1}$/CE2), and has fast memory accesses using Output Enable ($\overline{OE}$). The TC5588P/J is suitable for use as cache memory where high speed is required. All inputs and outputs are directly TTL compatable. The TC5588P/J is offered in standard 28 pin 300 mil DIP and SOJ packages for high density assembly.

FEATURES

- Fast access time:
  - TC5588P/J-15 15ns (MAX.)
  - TC5588P/J-20 20ns (MAX.)
  - TC5588P/J-25 25ns (MAX.)
  - TC5588P/J-35 35ns (MAX.)
- Low power dissipation:
  - Operation TC5588P/J-15 135mA (MAX.)
  - TC5588P/J-20 115mA (MAX.)
  - TC5588P/J-25 115mA (MAX.)
  - TC5588P/J-35 115mA (MAX.)
  - Standby 1mA (MAX.)
- 5V single power supply : 5V±10%
- Fully static operation
- Directly TTL compatible : All Input and Output
- Output buffer control : $\overline{OE}$
- Package :
  - 28 Pin plastic 300 mil DIP : TC5588P
  - 28 Pin plastic 300 mil SOJ : TC5588J

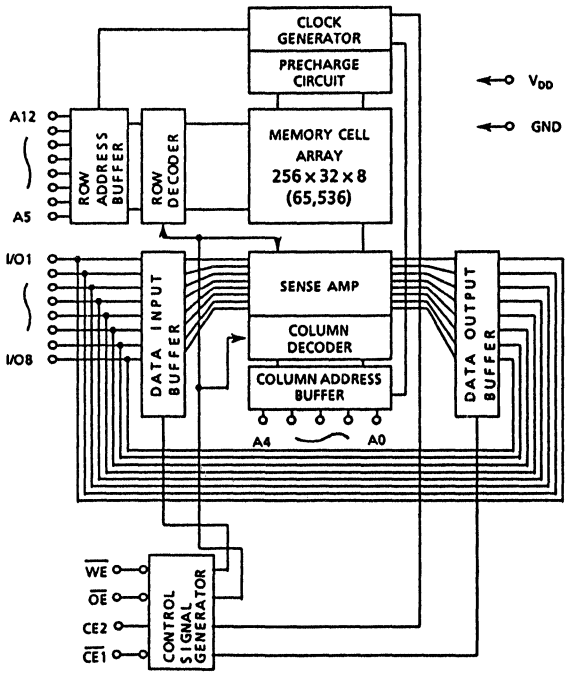
PIN CONNECTION



PIN NAMES

A0~A12	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
$\overline{CE1}$, CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
Tsolder	Soldering Temperature · Time	260 · 10	°C · sec
Tstrg	Storage Temperature	−65~150	°C
Topr	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	−0.5	−	0.8	V

DC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNITS
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}		−	−	±1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0~V_{DD}		−	−	±1	μA
I_{DD0}	Operating Current	V_{DD} = 5.5V tcycle = Min cycle $\overline{CE1}$ = V_{IL} and CE2 = V_{IH} Other Inputs = V_{IH}/V_{IL} I_{OUT} = 0mA	−15	−	−	135	mA
			−20	−	−	115	
			−25				
			−35				
I_{DDS1}	Standby Current	V_{DD} = 5.5V tcycle = Min cycle $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} Other Inputs = V_{IH}/V_{IL}		−	−	25	mA
I_{DDS2}*		$\overline{CE1}$ = V_{DD}−0.2V or CE2 = 0.2V Other Inputs = V_{DD}−0.2V or 0.2V		−	−	1	

* : In standby mode with $\overline{CE1} \geqq V_{DD}-0.2V$, these specification limits are guaranteed under the condition of $\overline{CE1} \geqq V_{DD}-0.2V$ or $CE2 \leqq 0.2V$.

CAPACITANCE** (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	7	pF

**: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS ($Ta = 0 \sim 70°C$ [1], $V_{DD} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC5588P/J-15		TC5588P/J-20		TC5588P/J-25		TC5588P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	25	–	35	–	ns
t_{ACC}	Address Access Time	–	15	–	20	–	25	–	35	
t_{CO1}	$\overline{CE1}$ Access Time	–	15	–	20	–	25	–	35	
t_{CO2}	CE2 Access Time	–	15	–	20	–	25	–	35	
t_{OE}	$\overline{OE}$ Access Time	–	9	–	10	–	12	–	12	
t_{OH}	Output Data Hold Time From Address Change	5	–	5	–	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE1}$ or CE2	5	–	5	–	5	–	5	–	
t_{COD}	Output Disable Time from $\overline{CE1}$ or CE2	–	6	–	6	–	6	–	6	
t_{OEE}	Output Enable Time from $\overline{OE}$	0	–	0	–	0	–	0	–	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	5	–	5	–	5	–	5	
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	
t_{PD}	Chip Deselection to Power Down Time	–	15	–	20	–	25	–	35	

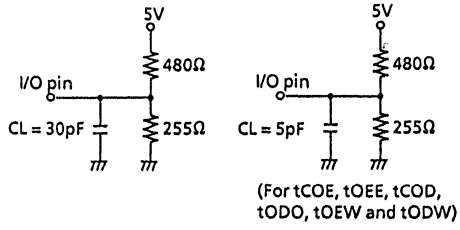
WRITE CYCLE

SYMBOL	PARAMETER	TC5588P/J-15		TC5588P/J-20		TC5588P/J-25		TC5588P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	25	–	35	–	ns
t_{CW}	Chip Enable to End of Write	12	–	13	–	15	–	15	–	
t_{AS}	Address Set Up Time	0	–	0	–	0	–	0	–	
t_{WP}	Write Pulse Width	12	–	13	–	15	–	15	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	
t_{DS}	Data Set Up Time	9	–	10	–	12	–	12	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	0	–	0	–	0	–	0	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	6	–	6	–	6	–	6	

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

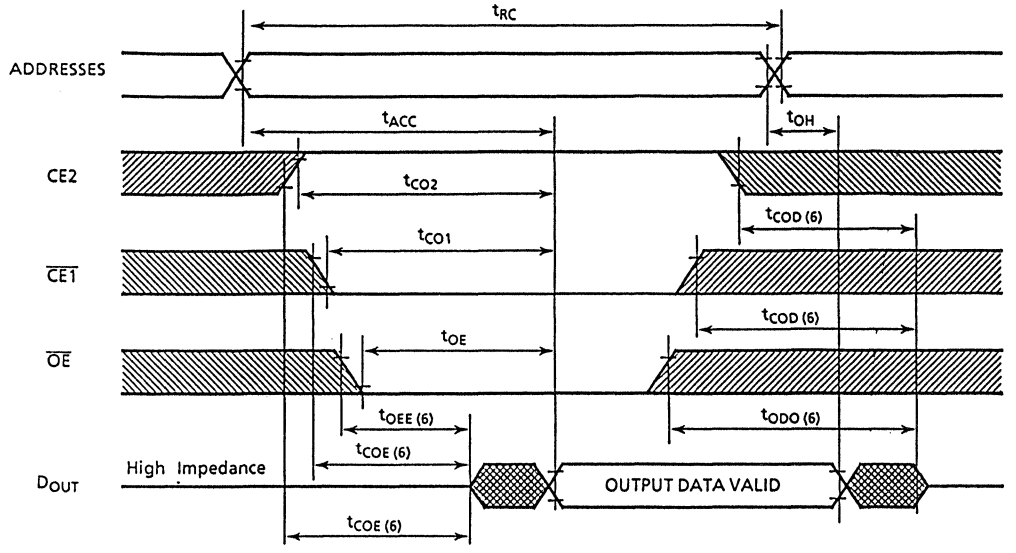
Fig. 1



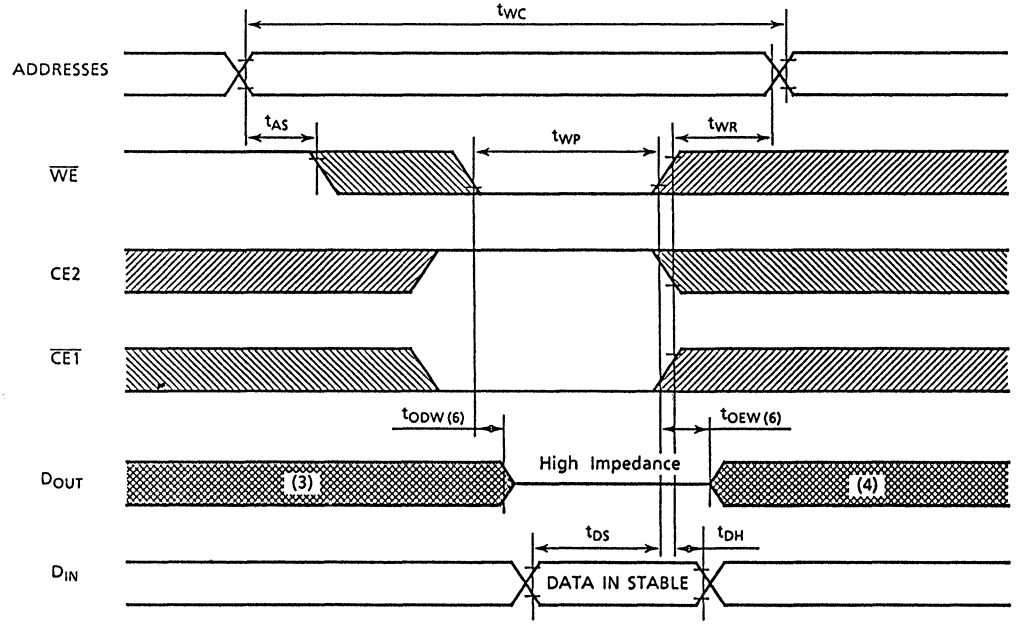
(For tCOE, tOEE, tCOD, tODO, tOEW and tODW)

TIMING WAVEFORMS

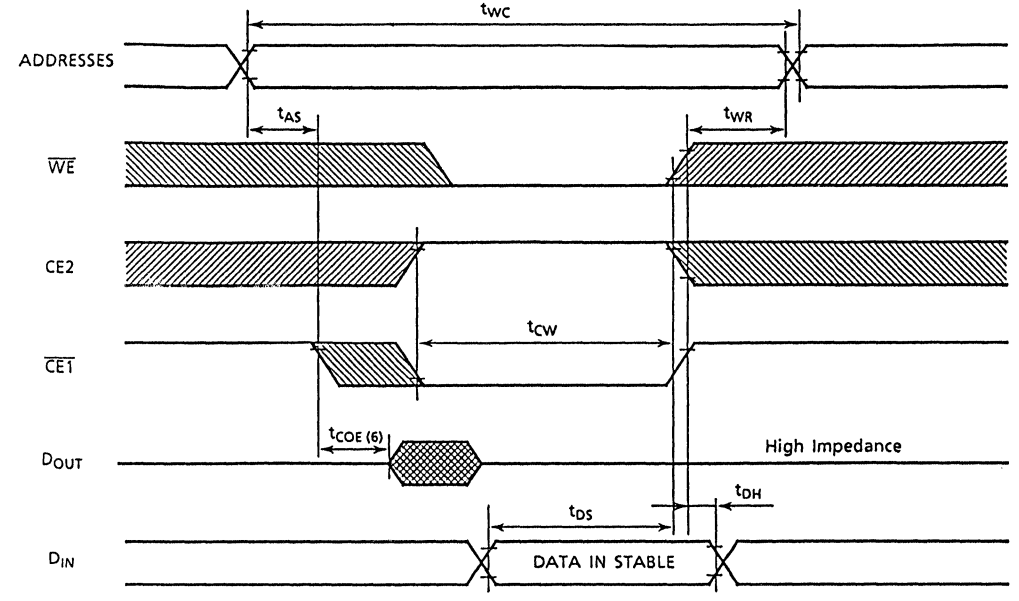
READ CYCLE (2)



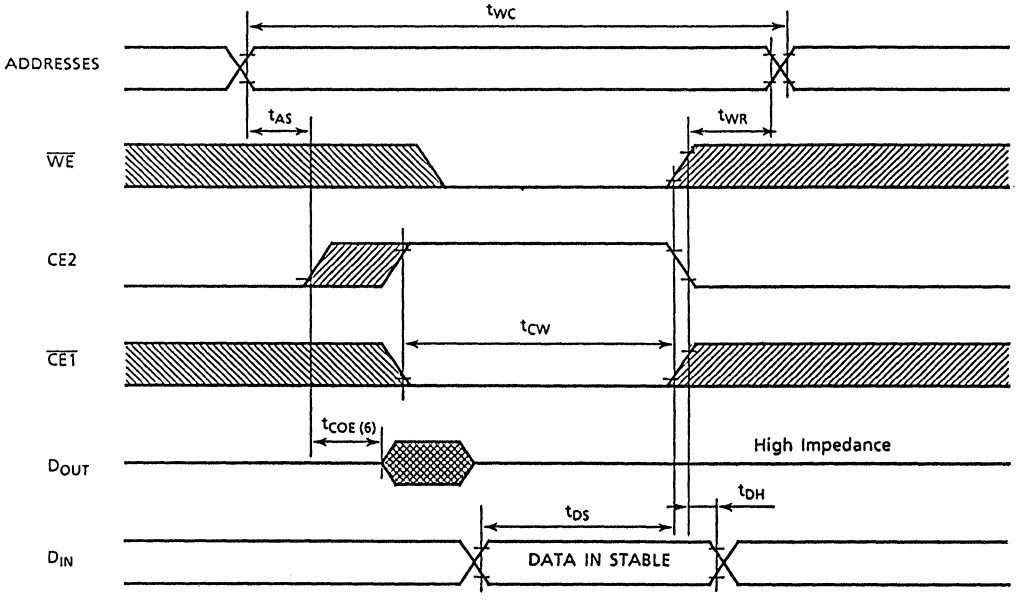
WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (5) ($\overline{CE1}$ Controlled Write)



WRITE CYLCE 3 (5) (CE2 Controlled Write)



NOTES: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

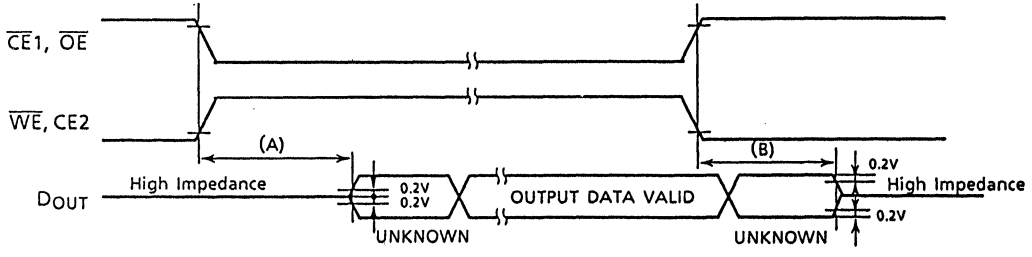
4. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

   (A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

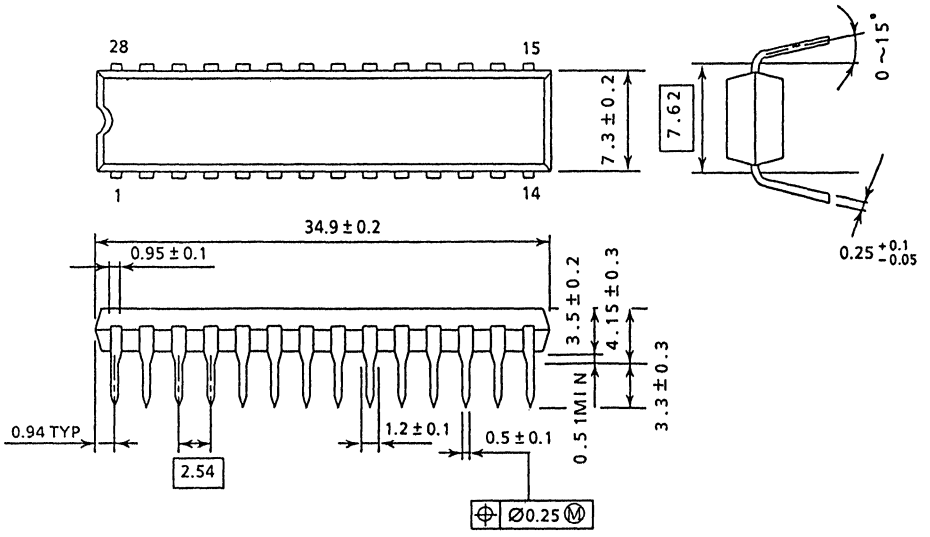
   (B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP28-P-300B)

UNIT : mm

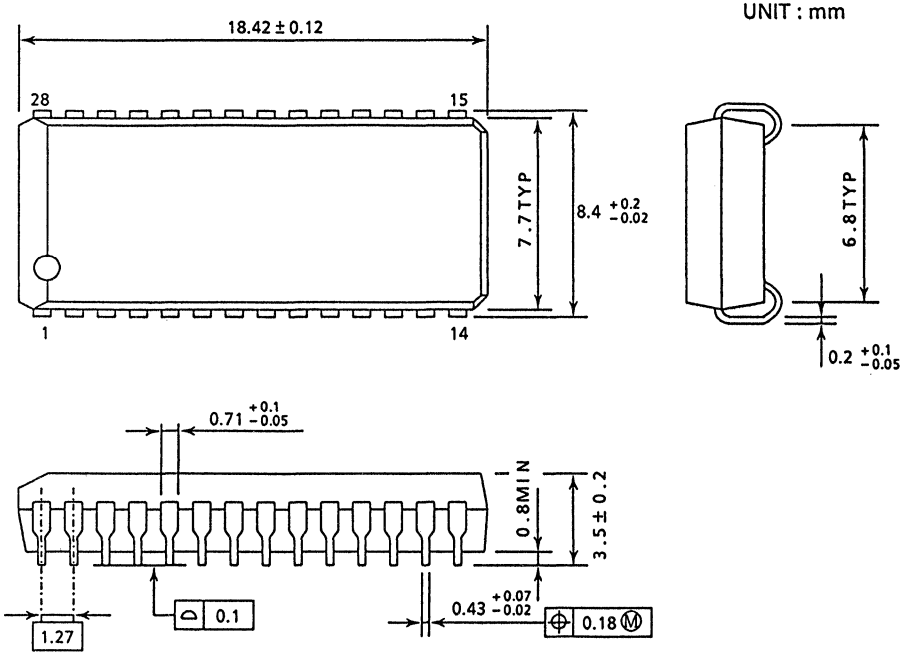


Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

Plastic SOJ (SOJ28-P-300A)

UNIT : mm



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

8,192 WORD × 9 BIT CMOS STATIC RAM

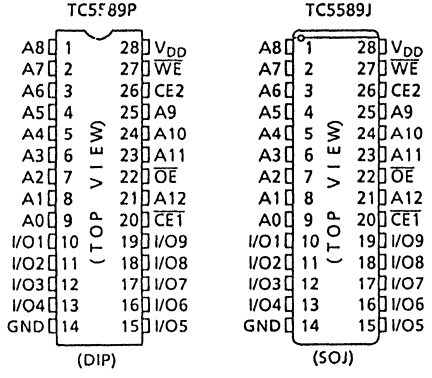
DESCRIPTION

The TC5589P/J is a 73,728 bit high-speed static random access memory organized as 8,192 words by 9 bits using CMOS technology, and operates from a single 5-volt supply. Toshiba's advanced CMOS circuitry provides high-speed characteristics. The TC5589P/J has low standby power using Chip Enables ($\overline{CE1}$/CE2), and has fast memory access using Output Enable ($\overline{OE}$). The TC5589P/J is suitable for use as cache memory where high speed is required. All inputs and outputs are directly TTL compatible. The TC5589P/J is offered in standard 28 pin 300 mil DIP and SOJ packages for high-density assembly.

FEATURES

- Fast access time:
  - TC5589P/J-15 15ns (MAX.)
  - TC5589P/J-20 20ns (MAX.)
  - TC5589P/J-25 25ns (MAX.)
  - TC5589P/J-35 35ns (MAX.)
- Low power dissipation:
  - Operation
    - TC5589P/J-15 135mA (MAX.)
    - TC5589P/J-20 115mA (MAX.)
    - TC5589P/J-25 115mA (MAX.)
    - TC5589P/J-35 115mA (MAX.)
  - Standby 1mA (MAX.)
- 5V single power supply : 5V±10%
- Fully static operation
- Directly TTL compatible : All Input and Output
- Output buffer control : $\overline{OE}$
- Package :
  - 28 Pin plastic 300 mil DIP : TC5589P
  - 28 Pin plastic 300 mil SOJ : TC5589J

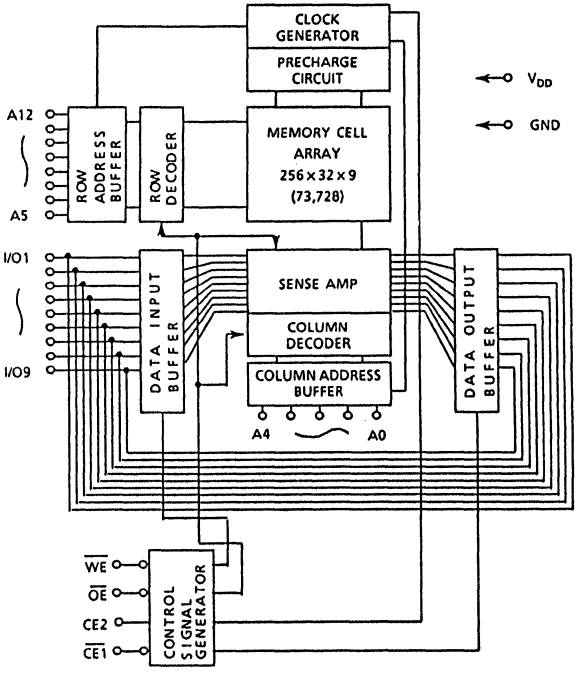
PIN CONNECTION



PIN NAMES

A0~A12	Address Inputs
I/O1~I/O9	Data Inputs/Outputs
$\overline{CE1}$, CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
Tsolder	Soldering Temperature · Time	260 · 10	°C · sec
Tstrg	Storage Temperature	−65~150	°C
Topr	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	−0.5	−	0.8	V

DC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNITS
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}		−	−	±1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0~V_{DD}		−	−	±1	μA
I_{DD0}	Operating Current	V_{DD} = 5.5V tcycle = Min cycle $\overline{CE1}$ = V_{IL} and CE2 = V_{IH} Other Inputs = V_{IH}/V_{IL} I_{OUT} = 0mA	−15	−	−	135	mA
			−20				
			−25	−	−	115	
			−35				
I_{DDS1}	Standby Current	V_{DD} = 5.5V tcycle = Min cycle $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} Other Inputs = V_{IH}/V_{IL}		−	−	25	mA
I_{DDS2}*		$\overline{CE1}$ = V_{DD} − 0.2V or CE2 = 0.2V Other Inputs = V_{DD} − 0.2V or 0.2V		−	−	1	

* : In standby mode with $\overline{CE1} \geqq V_{DD} - 0.2V$, these specification limits are guaranteed under the condition of $\overline{CE1} \geqq V_{DD} - 0.2V$ or $CE2 \leqq 0.2V$.

CAPACITANCE ** (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	7	pF

** : This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C [1], V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC5589P/J-15		TC5589P/J-20		TC5589P/J-25		TC5589P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	25	–	35	–	ns
t_{ACC}	Address Access Time	–	15	–	20	–	25	–	35	
t_{CO1}	$\overline{CE1}$ Access Time	–	15	–	20	–	25	–	35	
t_{CO2}	CE2 Access Time	–	15	–	20	–	25	–	35	
t_{OE}	$\overline{OE}$ Access Time	–	9	–	10	–	12	–	12	
t_{OH}	Output Data Hold Time From Address Change	5	–	5	–	5	–	5	–	
t_{COE}	Output Enable Time from $\overline{CE1}$ or CE2	5	–	5	–	5	–	5	–	
t_{COD}	Output Disable Time from $\overline{CE1}$ or CE2	–	6	–	6	–	6	–	6	
t_{OEE}	Output Enable Time from $\overline{OE}$	0	–	0	–	0	–	0	–	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	5	–	5	–	5	–	5	
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	
t_{PD}	Chip Deselection to Power Down Time	–	15	–	20	–	25	–	35	

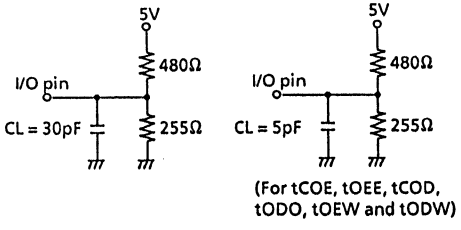
WRITE CYCLE

SYMBOL	PARAMETER	TC5589P/J-15		TC5589P/J-20		TC5589P/J-25		TC5589P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	25	–	35	–	ns
t_{CW}	Chip Enable to End of Write	12	–	13	–	15	–	15	–	
t_{AS}	Address Set Up Time	0	–	0	–	0	–	0	–	
t_{WP}	Write Pulse Width	12	–	13	–	15	–	15	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	
t_{DS}	Data Set Up Time	9	–	10	–	12	–	12	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	0	–	0	–	0	–	0	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	6	–	6	–	6	–	6	

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

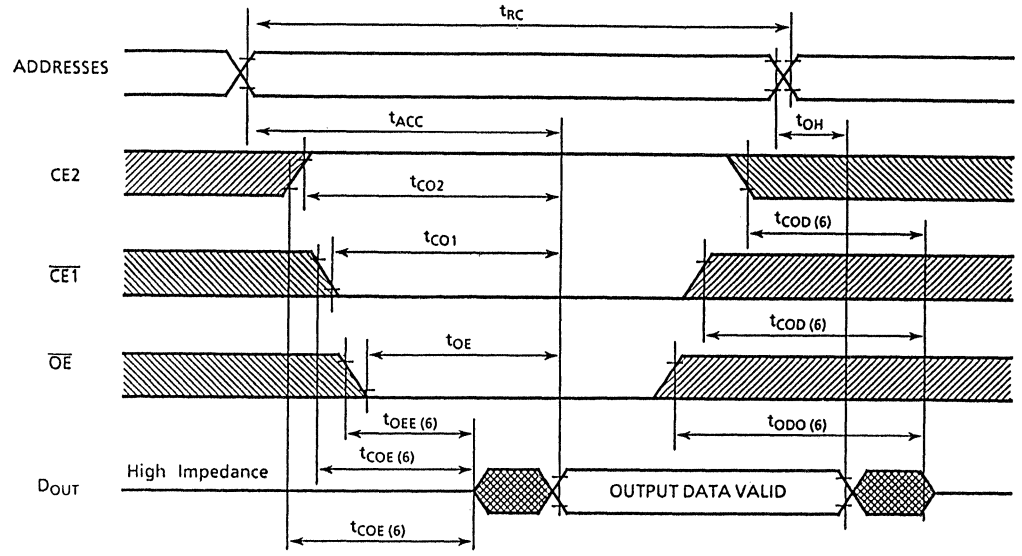
Fig. 1



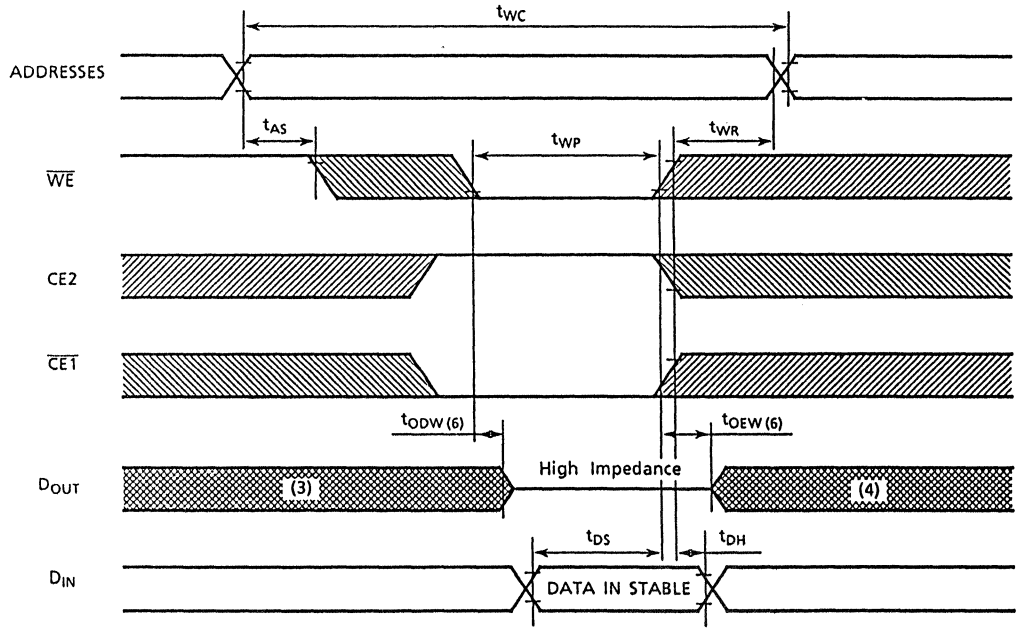
(For tCOE, tOEE, tCOD, tODO, tOEW and tODW)

TIMING WAVEFORMS

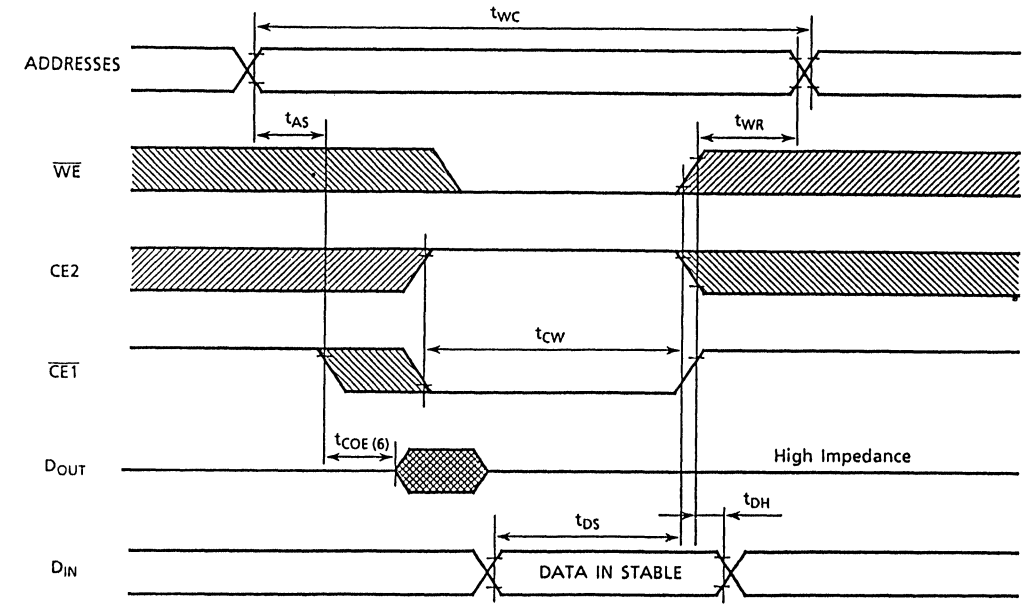
READ CYCLE (2)



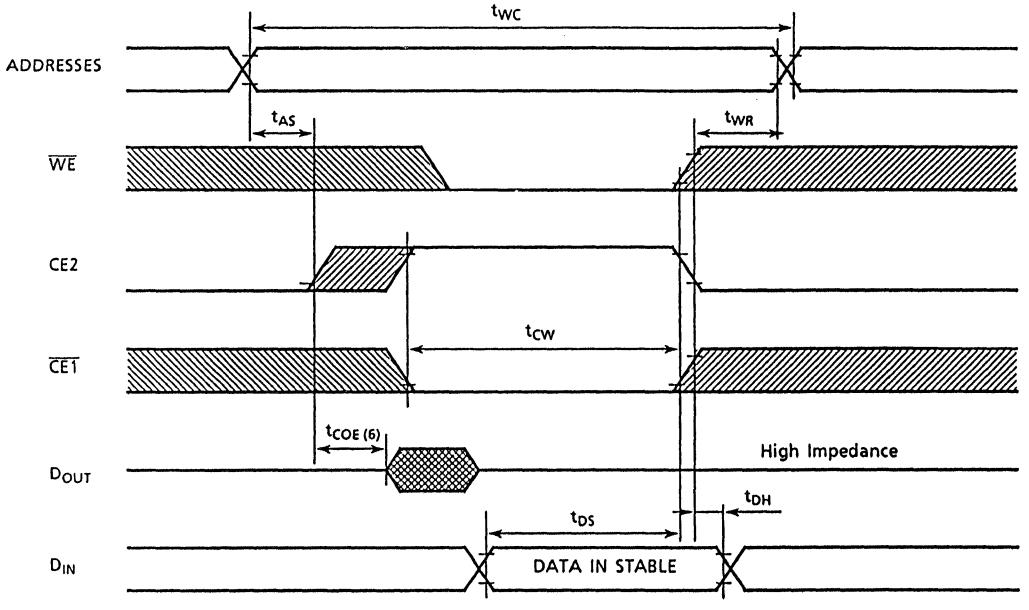
WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (5) ($\overline{CE1}$ Controlled Write)



WRITE CYLCE 3 (5) (CE2 Controlled Write)



NOTES: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE1}$ Low transition or CE2 High t ransition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

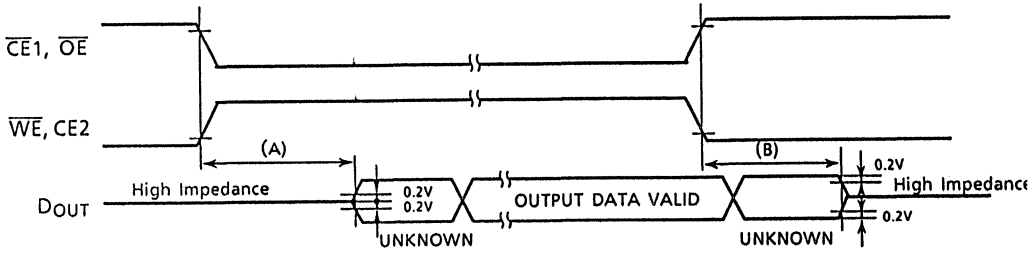
4. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

   (A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

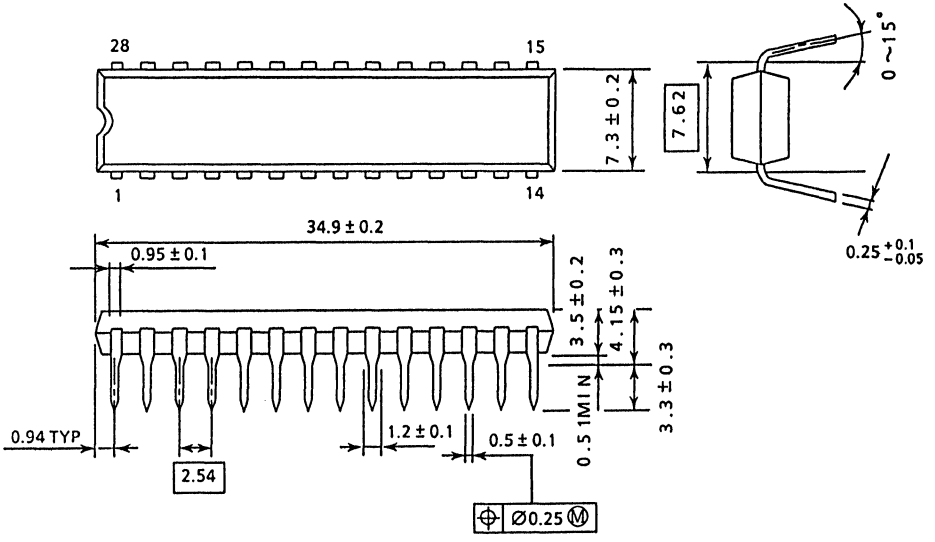
   (B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP28-P-300B)

UNIT : mm

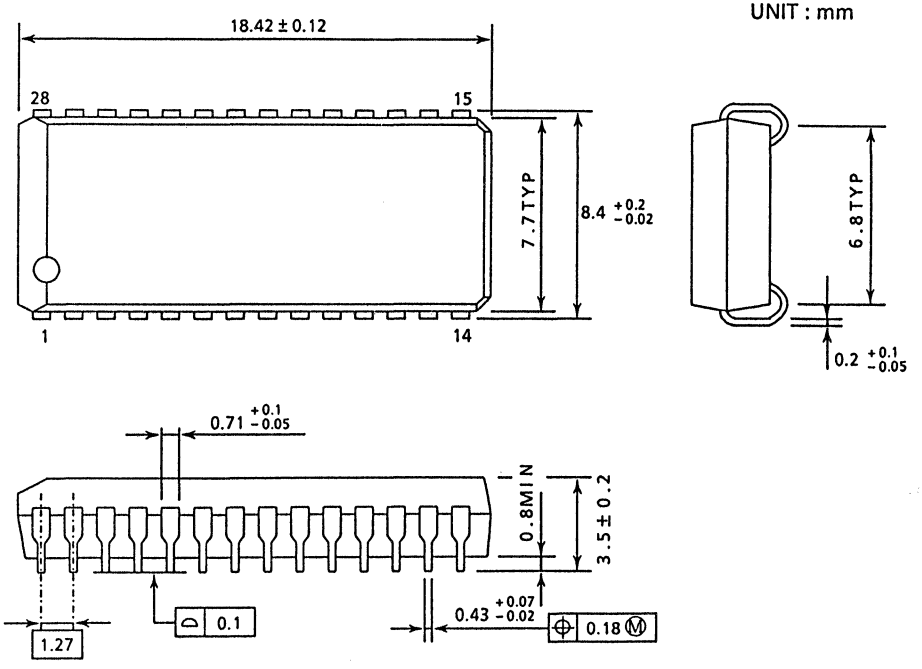


Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

Plastic SOJ (SOJ28-P-300A)

UNIT : mm



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

16,384 WORD × 4 BIT CMOS STATIC RAM

DESCRIPTION

The TC55416P–H is a 65,536 bit high speed static random access memory organized as 16,384 words by 4 bits using CMOS technology, and operates from a single 5–volt supply. Toshiba's high performance device technology provides both high speed and low power features with a maximum access time of 15ns / 20ns / 25ns / 35ns and maximum operating current of 120mA / 100mA / 100mA / 80mA at minimum cycle time.

The TC55416P–H also features an automatic stand-by mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced to 1mA.

The TC55416P–H is suitable for use in cache memory and high speed storage, where high speed/high density are required.

The TC55416P–H is offered in a 22 pin standard plastic DIP with 0.3 inch width for high density assembly.

The TC55416P–H is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time :

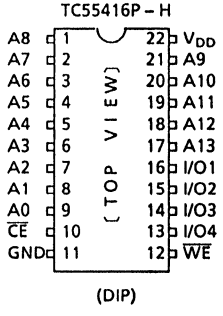
TC55416P–15H	15ns(MAX.)
TC55416P–20H	20ns(MAX.)
TC55416P–25H	25ns(MAX.)
TC55416P–35H	35ns(MAX.)

- 5V single power supply : 5V±10%
- Fully static operation
- Directly TTL compatible :
  All Input and Output
- Low power dissipation :

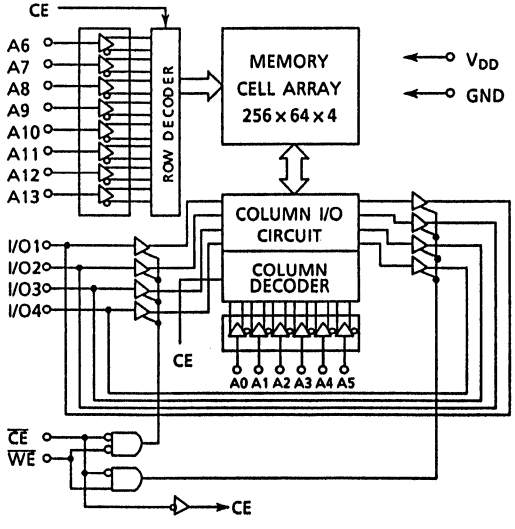
Operation	TC55416P–15H	120mA(MAX.)
	TC55416P–20H	100mA(MAX.)
	TC55416P–25H	100mA(MAX.)
	TC55416P–35H	80mA(MAX.)
Standby		1mA(MAX.)

- Package : 22pin plastic 300mil DIP (TC55416P-H)

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0 ~ A13	Address Inputs
I/O1 ~ I/O4	Data Input / Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power (+ 5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEMS	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
$V_{I/O}$	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
T_{solder}	Soldering Temperature · Time	260 · 10	°C·sec
T_{strg}	Storage Temperature	−65~150	°C
T_{opr}	Operating Temperature	−10~85	°C

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	−0.5	−	0.8	V

DC and OPERATING CHARACTERISTICS ($Ta=0\sim70°C$, $V_{DD}=5V\pm10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN}=0\sim V_{DD}$		−	−	±1	μA
I_{OH}	Output High Current	$V_{OH}=2.4V$		−4	−	−	mA
I_{OL}	Output Low Current	$V_{OL}=0.4V$		8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{OUT}=0\sim V_{DD}$		−	−	±1	μA
I_{DDO}	Operating Current	$V_{DD}=5.5V$, tcycle=Min cycle	−15H	−	−	120	mA
		$\overline{CE}=V_{IL}$, $I_{OUT}=0mA$	−20H	−	−	100	
			−25H	−	−	100	
		Other Input=V_{IH}/V_{IL}	−35H	−	−	80	
I_{DDS1}	Standby Current	$V_{DD}=5.5V$, tcycle=Min cycle $\overline{CE}=V_{IH}$, Other Input=V_{IH}/V_{IL}		−	−	25	mA
I_{DDS2}		$\overline{CE}=V_{DD}-0.2V$ Other Input=$V_{DD}-0.2V$ or 0.2V		−	−	1	

CAPACITANCE ($Ta=25°C$)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN}=GND$	5	pF
C_{OUT}	Output Capacitance	$V_{OUT}=GND$	7	pF

NOTE: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS ($Ta=0\sim70°C$ [4], $V_{DD}=5V\pm10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC55416P-15H		TC55416P-20H		TC55416P-25H		TC55416P-35H		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	25	–	35	–	ns
t_{ACC}	Address Access Time	–	15	–	20	–	25	–	35	
t_{CO}	Chip Enable Access Time	–	15	–	20	–	25	–	35	
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	5	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	6	–	6	–	6	–	6	
t_{OH}	Output Data Hold Time	5	–	5	–	5	–	5	–	
t_{PU}	Power Up Time	0	–	0	–	0	–	0	–	
t_{PD}	Power Down Time	–	15	–	20	–	25	–	35	

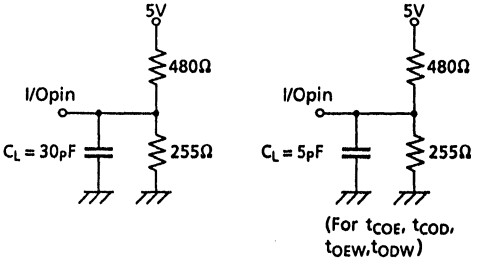
WRITE CYCLE

SYMBOL	PARAMETER	TC55416P-15H		TC55416P-20H		TC55416P-25H		TC55416P-35H		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	25	–	35	–	ns
t_{WP}	Write Pulse Width	12	–	13	–	13	–	13	–	
t_{CW}	Chip Enable to End of Write	12	–	13	–	13	–	13	–	
t_{AS}	Address Set Up Time	0	–	0	–	0	–	0	–	
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	0	–	0	–	0	–	0	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	6	–	6	–	6	–	6	
t_{DS}	Data Set Up Time	9	–	10	–	10	–	10	–	
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	

AC TEST CONDITIONS

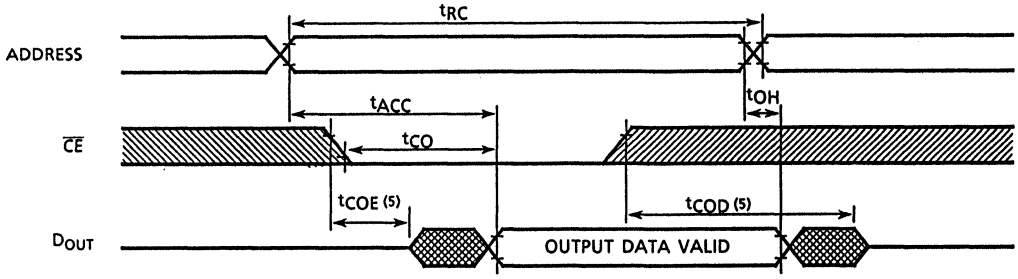
Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	See Fig. 1

Fig. 1

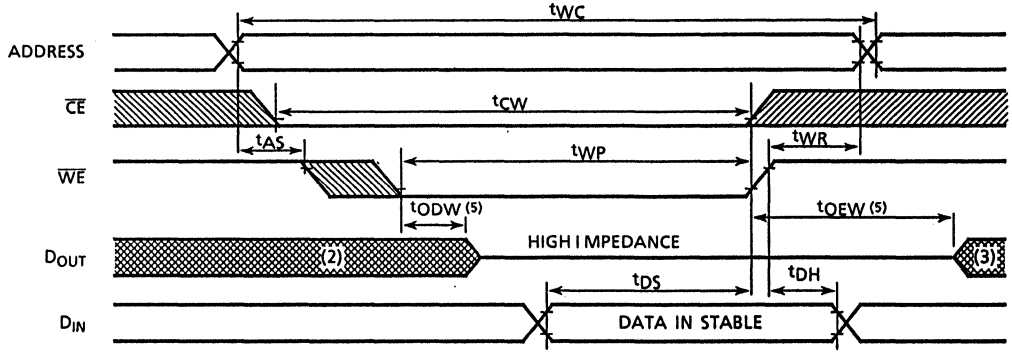


TIMING WAVEFORMS

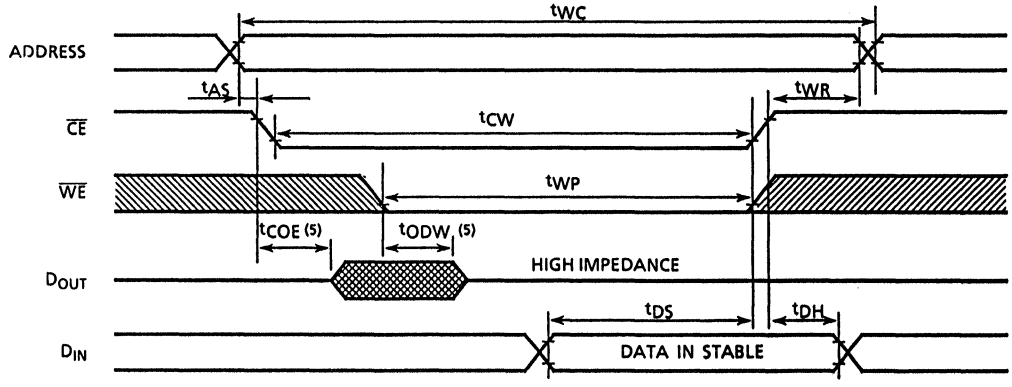
READ CYCLE (1)



WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)



(注) 1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

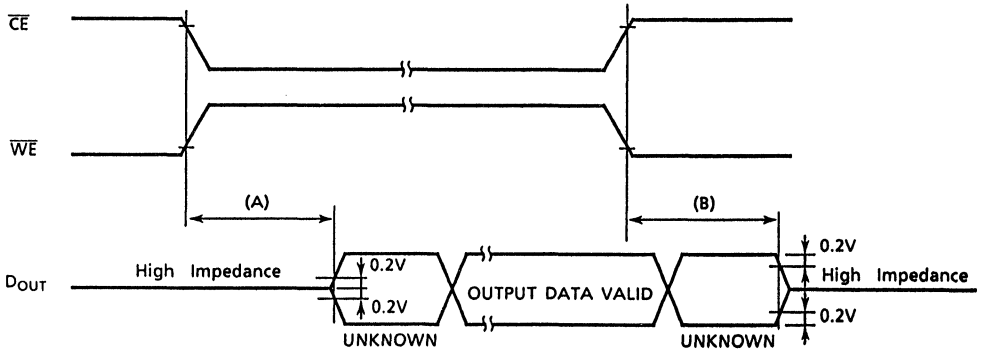
3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

5. These parameters are specified as follows and measured by using the load shown in Fig.1.

   (A) t_{COE}, t_{OEW} ····· Output Enable Time

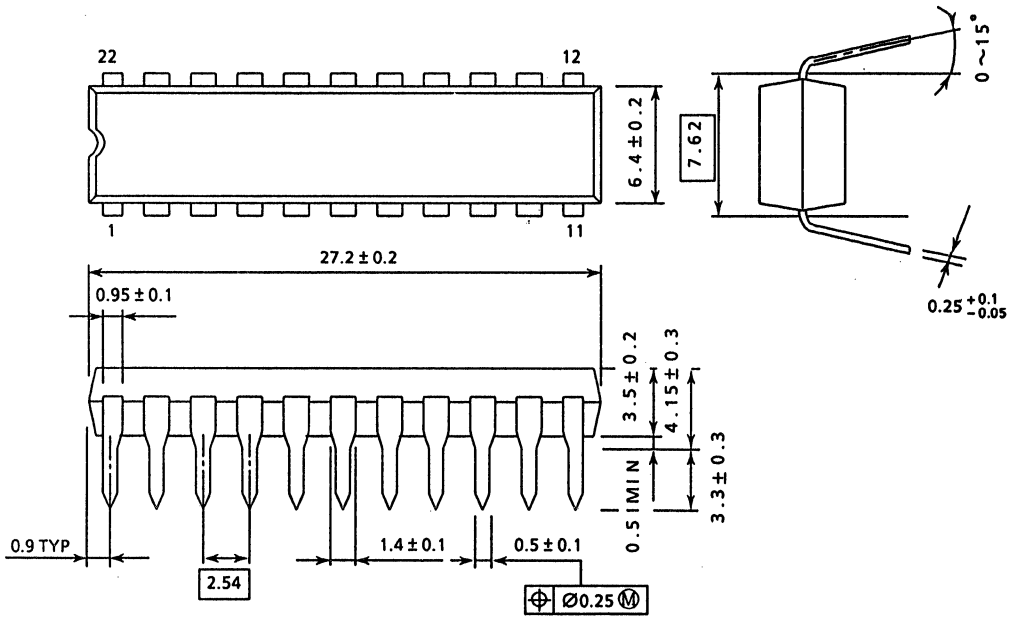
   (B) t_{COD}, t_{ODW} ····· Output Disable Time



OUTPUT DRAWINGS

Plastic DIP (DIP22-P-300)

UNIT : mm



NOTE . Package width and length do not include mole protrusion allowable mold protrusion is 0.15 mm.

16,384 WORD × 4 BIT CMOS STATIC RAM

DESCRIPTION

The TC55417P/J-H is a 65,536 bit high speed static random access memory organized as 16,384 words by 4 bits using CMOS technology, and operates from a single 5-volt supply. Toshiba's high performance device technology provides both high speed and low power features with maximum access times of 15ns / 20ns / 25ns / 35ns and maximum operating current of 120mA / 100mA / 100mA / 80mA at minimum cycle time.

The TC55417P/J-H also features an automatic stand-by mode. When deselected by Chip Enable ($\overline{CE}$), the operating current is reduced to 1mA.

The TC55417P/J-H is suitable for use in cache memory and high speed storage, where high speed/high density are required.

The TC55417P/J-H is offered in a 24 pin standard plastic DIP and a 24 pin plastic SOJ, with 0.3 inch width for high density assembly.

The TC55417P/J-H is fabricated with ion implanted CMOS silicon gate MOS technology for high performance and high reliability.

FEATURES

- Fast access time :

	TC55417P/J-15H	15ns(MAX.)
	TC55417P/J-20H	20ns(MAX.)
	TC55417P/J-25H	25ns(MAX.)
	TC55417P/J-35H	35ns(MAX.)

- 5V single power supply : 5V±10%
- Fully static operation
- Directly TTL compatible :

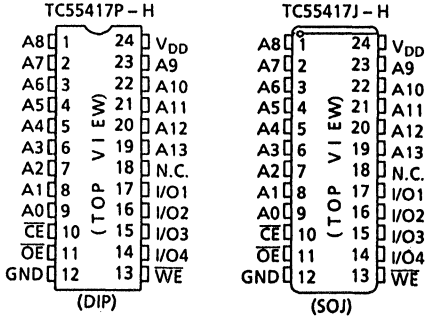
  All Input and Output

- Low power dissipation :

Operation	TC55417P/J-15H	120mA(MAX.)
	TC55417P/J-20H	100mA(MAX.)
	TC55417P/J-25H	100mA(MAX.)
	TC55417P/J-35H	80mA(MAX.)
Standby		1mA(MAX.)

- Output buffer control : $\overline{OE}$
- Package : 24Pin plastic 300mil DIP (TC55417P-H)
  24Pin plastic 300mil SOJ (TC55417J-H)

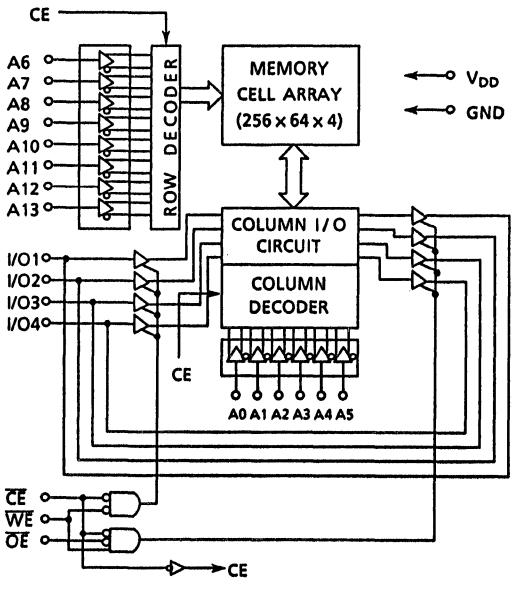
PIN CONNECTION



PIN NAMES

A0 ~ A13	Address Inputs
I/O1 ~ I/O4	Data Input / Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS
V_{DD}	Power Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-2.0~7.0	V
V_{OUT}	Output Voltage	-0.5~V_{DD}+0.5	V
P_D	Power Dissipation	650	mW
Tsolder	Soldering Temperature · Time	260 · 10	°C · sec
Tstrg	Storage Temperature	-65~150	°C
Topr	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	-	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	-0.5	-	0.8	V

DC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}		-	-	±1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		-4	-	-	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	-	-	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 0~V_{DD}		-	-	±1	μA
I_{DDO}	Operating Current	V_{DD} = 5.5V, tcycle = Min cycle $\overline{CE}$ = V_{IL}, I_{OUT} = 0mA Other Input = V_{IH}/V_{IL}	-15H	-	-	120	mA
			-20H	-	-	100	
			-25H	-	-	100	
			-35H	-	-	80	
I_{DDS1}	Standby Current	V_{DD} = 5.5V, tcycle = Min cycle $\overline{CE}$ = V_{IH}, Other Input = V_{IH}/V_{IL}		-	-	25	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} - 0.2V Other Input = V_{DD} - 0.2V or 0.2V		-	-	1	

CAPACITANCE (Ta = 25°C)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	7	pF

NOTE: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS ($Ta = 0 \sim 70°C$ [4], $V_{DD} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC55417P/J-15H		TC55417P/J-20H		TC55417P/J-25H		TC55417P/J-35H		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	15	–	20	–	25	–	35	–	ns
t_{ACC}	Address Access Time	–	15	–	20	–	25	–	35	ns
t_{CO}	Chip Enable Access Time	–	15	–	20	–	25	–	35	ns
t_{OE}	Output Enable to Output Valid	–	9	–	10	–	10	–	10	ns
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	5	–	ns
t_{COD}	Output Disable Time from $\overline{CE}$	–	6	–	6	–	6	–	6	ns
t_{OEE}	Output Enable Time from $\overline{OE}$	0	–	0	–	0	–	0	–	ns
t_{ODO}	Output Disable Time from $\overline{OE}$	–	5	–	5	–	5	–	5	ns
t_{OH}	Output Data Hold Time	5	–	5	–	5	–	5	–	ns
t_{PU}	Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}	Power Down Time	–	15	–	20	–	25	–	35	ns

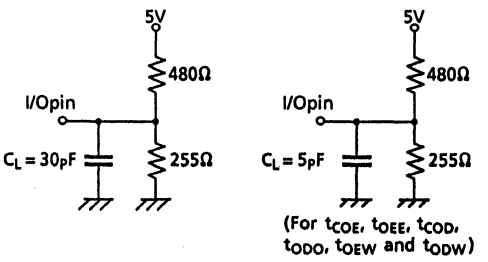
WRITE CYCLE

SYMBOL	PARAMETER	TC55417P/J-15H		TC55417P/J-20H		TC55417P/J-25H		TC55417P/J-35H		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	15	–	20	–	25	–	35	–	ns
t_{WP}	Write Pulse Width	12	–	13	–	13	–	13	–	ns
t_{CW}	Chip Enable to End of Write	12	–	13	–	13	–	13	–	ns
t_{AS}	Address Set Up Time	0	–	0	–	0	–	0	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{OEW}	Output Enable Time from $\overline{WE}$	0	–	0	–	0	–	0	–	ns
t_{ODW}	Output Disable Time from $\overline{WE}$	–	6	–	6	–	6	–	6	ns
t_{DS}	Data Set Up Time	9	–	10	–	10	–	10	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns

AC TEST CONDITIONS

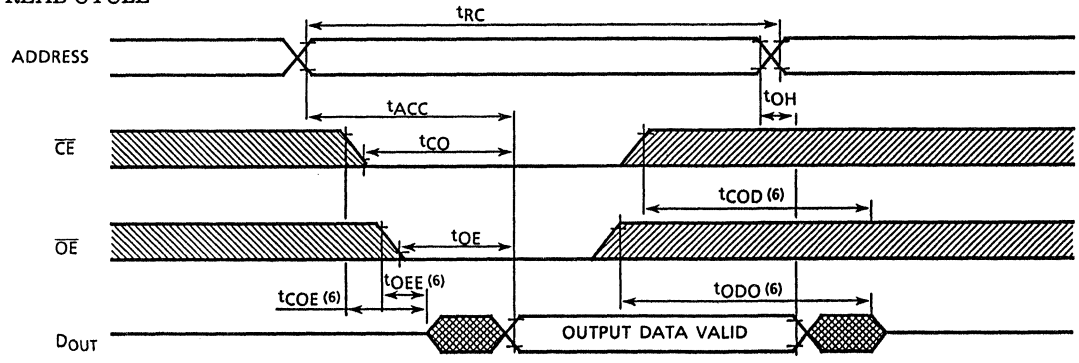
Input Pulse Levels	3.0V/0.0V
Input Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	See Fig. 1

Fig. 1

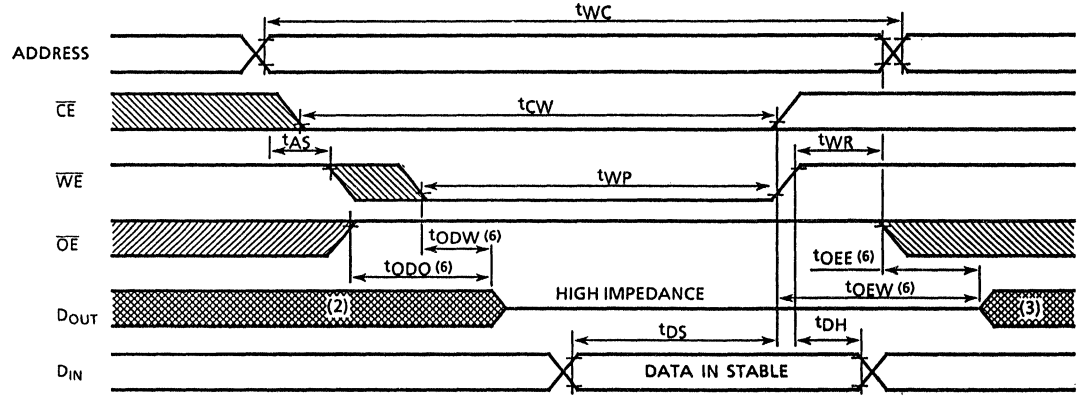


TIMING WAVEFORMS

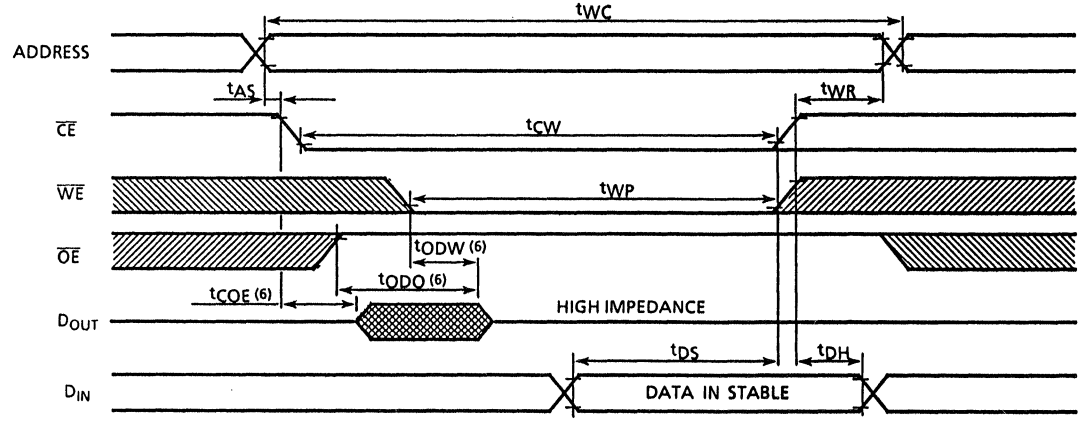
READ CYCLE [1]



WRITE CYCLE 1 [5] ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 [5] ($\overline{CE}$ Controlled Write)



Note: 1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occures coincident with or after $\overline{WE}$ Low transition, outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, outputs remain in a high impedance state.

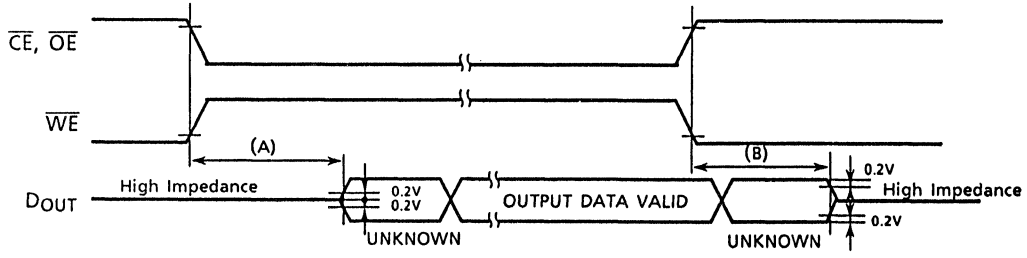
4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

5. The $\overline{OE}$ input can be held on low (V_{IL}) in write cycle.

6. These parameters are specified as follows and measured by using the load shown in Fig.1.

   (A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

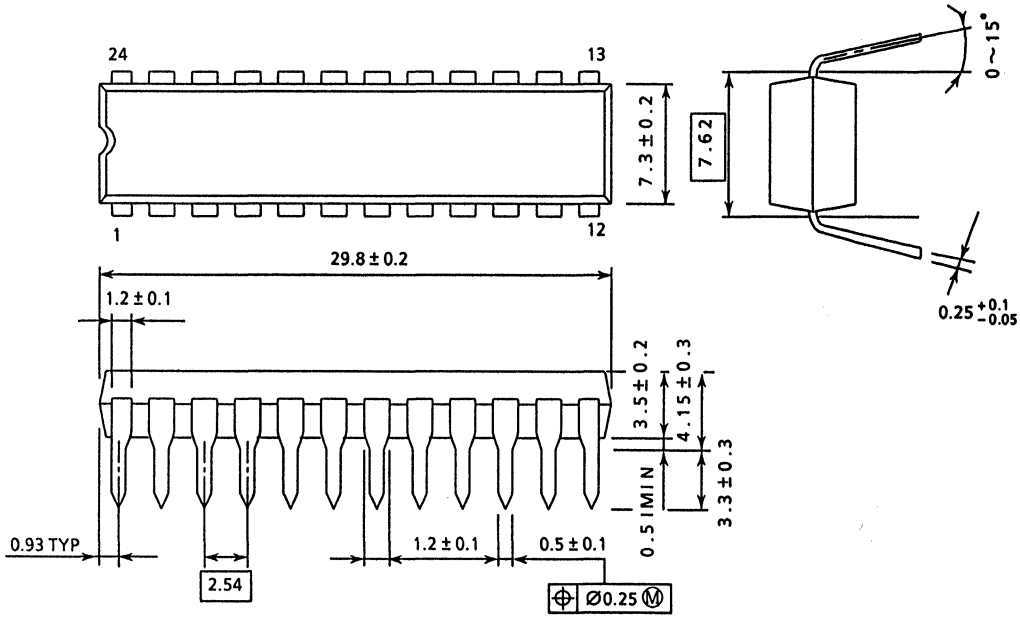
   (B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP–24–300B)

Unit : mm

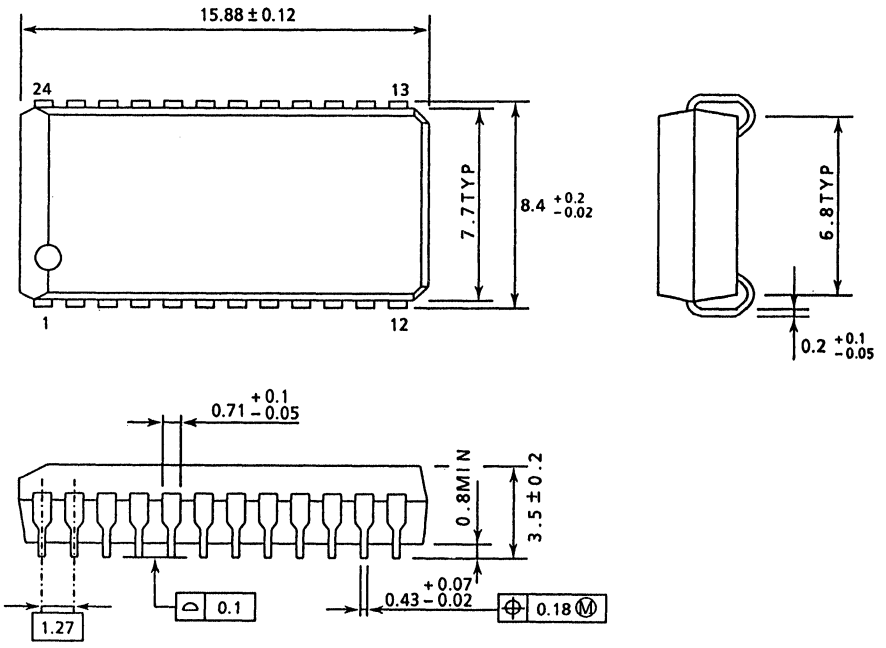


NOTE : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

Plastic SOJ (SOJ24-P-300A)

Unit : mm



NOTE : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

2-WAY 4,096 WORDS × 18 BITS / 8,192 WORDS × 18 BITS CMOS STATIC CACHE DATA RAM

DESCRIPTION

The TC55187T is a 147,456 bits high-speed static RAM which can be user-configured either as a 2-way 4,096 words by 18 bits or as 8,192 words by 18 bits. It is provided with byte control and on-chip address latches. The TC55187T is fabricated using Toshiba's CMOS technology and advanced circuit techniques which provide the high speed access. The TC55187T operates from a single 5-volt supply. This device features address access time as fast as 20ns, output-enable access as fast as 10ns and simple interfacing capability with bipolor TTL circuits is also offered. The TC55187T can directly interface with the INTEL 82385 cache controller without requiring additional peripheral circuit such as latches, transceivers and gates. Therefore, significant reductions in component count, board assembly area and power dissipation can be achieved by using the TC55187T cache data RAM. The MODE input of the TC55187T allows the user to configure the memory internally either as a 2-way 4,096 words by 18 bit organization suitable for 2-way set associative cache designs or as a 8,192 words by 18 bit organization suitable for direct map cache designs. The TC55187T can also be operated as a conventional asynchronous static RAM, which can be accessed from change of address, by holding the ALE input in the high state. The TC55187T is packaged in a 52-pin standard PLCC for high-density board level assembly.

FEATURES

- Fast Access Time (max.)

ITEM		TC55187T		
		-20	-25	-30
t_{RC}	Cycle Time	20ns	25ns	30ns
t_{AA}	Address Access Time	20ns	25ns	30ns
t_{OE}	$\overline{OE}$ Access Time	10ns	10ns	12ns

- Power dissipation

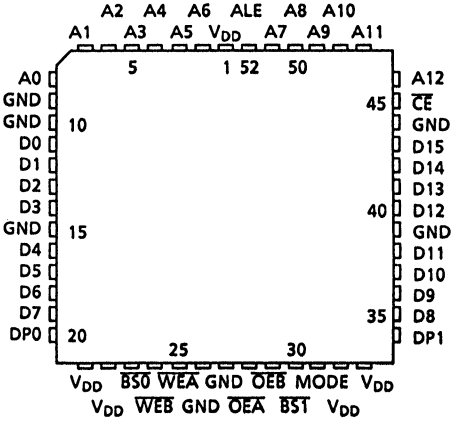
Operating	TC55187T-20	230mA (max.)
	TC55187T-25	220mA (max.)
	TC55187T-30	200mA (max.)
Standby		40mA (max.)

- Configurable for 2-way or direct RAM arrays
  2-way 4,096words×18bits (MODE=V_{IH})
  8,192words×18bits (MODE=V_{IL})
- Contains address latches (except A12) and byte control, $\overline{BS0}$ and $\overline{BS1}$
- Interfaces directly with the Intel 82385 Cache Controller
- Single power supply of 5V±10%
- All inputs and outputs TTL compatible
- Two Output buffer controls : $\overline{OEA}$, $\overline{OEB}$
- Two Write enable controls : $\overline{WEA}$, $\overline{WEB}$
- 52pin PLCC package

PIN NAMES

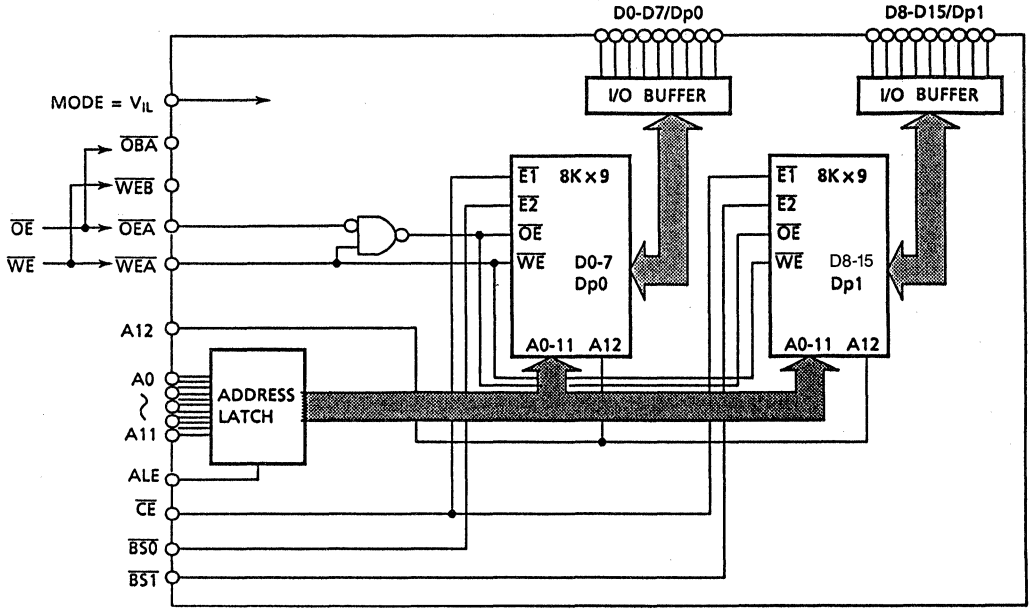
A0~A12	Address Inputs
D0~D15, DP0, DP1	Data Input/Output
ALE	Address Latch Input
$\overline{CE}$	Chip Enable Input
$\overline{BS0}$	Lower Byte Select Input
$\overline{BS1}$	Upper Byte Select Input
$\overline{OEA}$	Output Enable Input (Way-A)
$\overline{OEB}$	Output Enable Input (Way-B)
$\overline{WEA}$	Write Enable Input (Way-A)
$\overline{WEB}$	Write Enable Input (Way-B)
MODE	Mode Select Input
VDD	Power (+5V)
GND	Ground

PIN CONNECTION (TOP VIEW)

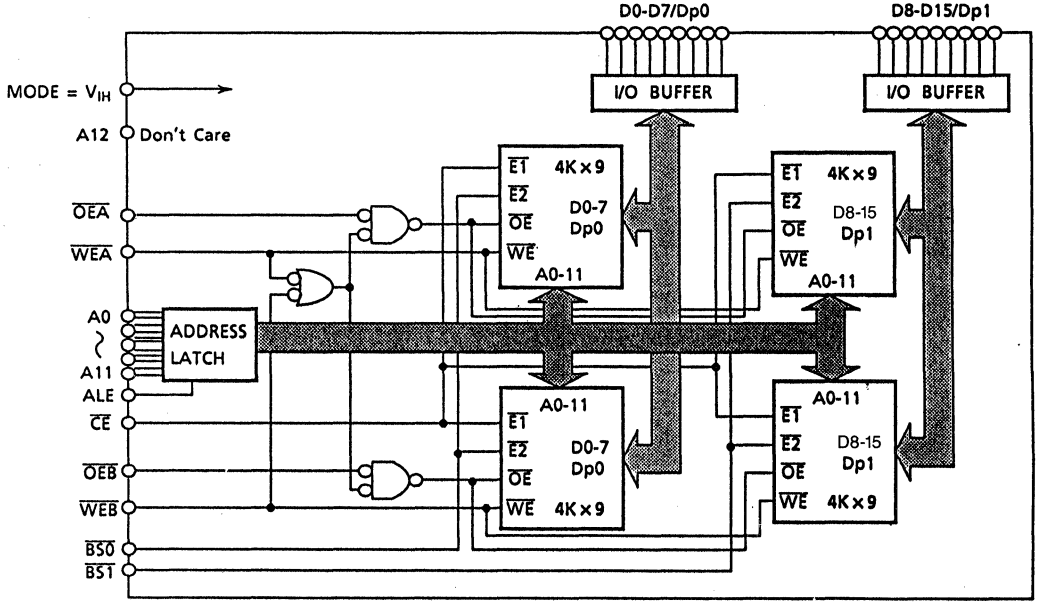


BLOCK DIAGRAM

1-WAY 8,192 words × 18 bits (MODE : V_{IL})



2-WAY 4,096 words × 18 bits (MODE : V_{IH})



TRUTH TABLE 1

CONTROL INPUT			ADDRESS		FUNCTION	
MODE	ALE	$\overline{CE}$	A0~A11	A12	CHIP	CONFIGURATION
H	H	H	*	*	Disable	4K x 18 x 2
H	H	L	Valid	*	Enable	
H	L	*	*	*	Enable or Disable	
L	*	H	*	*	Disable	8K x 18
L	H	L	Valid	Valid	Enable	
L	L	L	*	Valid	Enable	

* : H or L

TRUTH TABLE 2 (MODE = V_{IL} ··· 8K x 18)

INPUTS						OPERATION		
$\overline{WEA}$	$\overline{WEB}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{BS0}$	$\overline{BS1}$	CHIP	D0-D7 Dp0	D8-D15 Dp1
*	*	*	*	H	H	Deselect	Open	Open
H	H	H	H	*	*	Deselect	Open	Open
H	H	L	L	L	H	Read Cycle	Output	Open
				H	L		Open	Output
				L	L		Output	Output
L	L	*	*	L	H	Write Cycle	Input	Open
				H	L		Open	Input
				L	L		Input	Input
H	H	H	L	L	H	Undefine	Undefine	Undefine
				H	L			
				L	L			
H	H	L	H	L	H	Undefine	Undefine	Undefine
				H	L			
				L	L			
H	L	*	*	L	H	Undefine	Undefine	Undefine
				H	L			
				L	L			
L	H	*	*	L	H	Undefine	Undefine	Undefine
				H	L			
				L	L			

* : H or L

TRUTH TABLE 3 (MODE = V_{IH} ··· 4K x 18 x 2)

INPUTS						OPERATION			
$\overline{WEA}$	$\overline{WEB}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{BS0}$	$\overline{BS1}$	way-A	way-B	D0~D7 Dp0	D8~D15 Dp1
*	*	*	*	H	H	Deselect	Deselect	Open	Open
H	H	H	H	*	*	Deselect	Deselect	Open	Open
H	H	H	L	L	H	Deselect	Read Cycle	way-B Output	Open
				H	L			Open	way-B Output
				L	L			way-B Output	way-B Output
H	H	L	H	L	H	Read Cycle	Deselect	way-A Output	Open
				H	L			Open	way-A Output
				L	L			way-A Output	way-A Output
H	H	L	L	L	H	Deselect	Deselect	Open	Open
				H	L				
				L	L				
H	L	*	*	L	H	Deselect	Write Cycle	way-B Input	Open
				H	L			Open	way-B Input
				L	L			way-B Input	way-B Input
L	H	*	*	L	H	Write Cycle	Deselect	way-A Input	Open
				H	L			Open	way-A Input
				L	L			way-A Input	way-A Input
L	L	*	*	L	H	Write Cycle	Write Cycle	way-A/B Input	Open
				H	L			Open	way-A/B Input
				L	L			way-A/B Input	way-A/B Input

* : H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.3	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	−65~150	°C
T_{opr}	Operating Temperature	−10~85	°C

DC RECOMMENDED OPERATION CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	−0.5*	−	0.8	V

* : −3V pulse width less than 10ns

DC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}		−1	−	+1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	−	−	mA
I_{LO}	Output Leakage Current	Output Disable		−1	−	+1	μA
I_{DDO}	Operating Current	V_{DD} = 5.5V, t_{RC}, t_{WC} = min. cycle Addres, $\overline{WE}$, ALE = Clock (3.0V/0V), $\overline{OE}$ = 3.0V $\overline{CE}$, $\overline{BS}$ = 0V, MODE = 3.0V or 0V	−20	−	−	230	mA
			−25	−	−	220	
			−30	−	−	200	
I_{DDS}	Standby Current	V_{DD} = 5.5V, $\overline{CE}$, $\overline{BS}$, $\overline{WE}$, $\overline{OE}$ = V_{IH}, ALE = V_{IL} Address, Data, MODE = V_{IH} or V_{IL}		−	−	40	mA

CAPACITANCE (Ta = 25°C, freq = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Cin	Input Capacitance	V_{IN} = GND	−	−	5	pF
Cout	Output Capacitance	V_{OUT} = GND	−	−	7	pF

AC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	–20		–25		–30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	20	–	25	–	30	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	30	ns
t_{A12A}	A12 Access Time	–	15	–	17	–	20	ns
t_{LA}	ALE Access Time	–	20	–	25	–	30	ns
t_{CA}	$\overline{CE}$ Access Time	–	20	–	22	–	25	ns
t_{BA}	$\overline{BS}$ Access Time	–	20	–	22	–	25	ns
t_{OE}	$\overline{OE}$ Access Time	–	10	–	10	–	12	ns
t_{ASL}	Address Latch Set-Up Time	4	–	4	–	5	–	ns
t_{AHL}	Address Latch Hold Time	5	–	5	–	5	–	ns
t_{LP}	ALE Pulse Width	8	–	8	–	9	–	ns
t_{AOH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	ns
t_{LOH}	Output Data Hold Time from Address Latch	5	–	5	–	5	–	ns
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	5	–	5	–	5	–	ns
t_{BLZ}	$\overline{BS}$ to Output in Low-Z	5	–	5	–	5	–	ns
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	–	0	–	0	–	ns
t_{CHZ}	$\overline{CE}$ to Output in High-Z	–	10	–	10	–	12	ns
t_{BHZ}	$\overline{BS}$ to Output in High-Z	–	10	–	10	–	12	ns
t_{OHZ}	$\overline{OE}$ to Output in High-Z	–	8	–	8	–	10	ns
t_{OOI}	$\overline{OEA}$/$\overline{OEB}$ Inhibit Time	8	–	8	–	10	–	ns

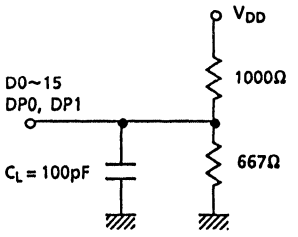
WRITE CYCLE

SYMBOL	PARAMETER	-20		-25		-30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	20	-	25	-	30	-	ns
t_{WP}	$\overline{WE}$ Pulse Width	12	-	15	-	18	-	ns
t_{BW}	$\overline{BS}$ to End of Write	12	-	15	-	18	-	ns
t_{CW}	$\overline{CE}$ to End of Write	12	-	15	-	18	-	ns
t_{AW}	Write Address to End of Write	12	-	15	-	18	-	ns
t_{A12W}	Write Address A12 to End of Write	12	-	15	-	18	-	ns
t_{AS}	Write Address Set-Up Time	0	-	0	-	0	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{DS}	Data Set-Up Time	8	-	10	-	10	-	ns
t_{DH}	Data Hold Time	0	-	0	-	0	-	ns
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	-	5	-	5	-	ns
t_{WHZ}	$\overline{WE}$ to Output in High-Z	-	7	-	8	-	10	ns
t_{OEH}	$\overline{OE}$ Command Hold Time	5	-	5	-	5	-	ns
t_{WEH}	$\overline{WE}$ Command Hold Time	-	5	-	5	-	5	ns
t_{WI}	Write Command Inhibit Time	10	-	10	-	10	-	ns
t_{WA}	$\overline{WE}$ Access Time	-	20	-	25	-	30	ns

AC TEST CONDITIONS

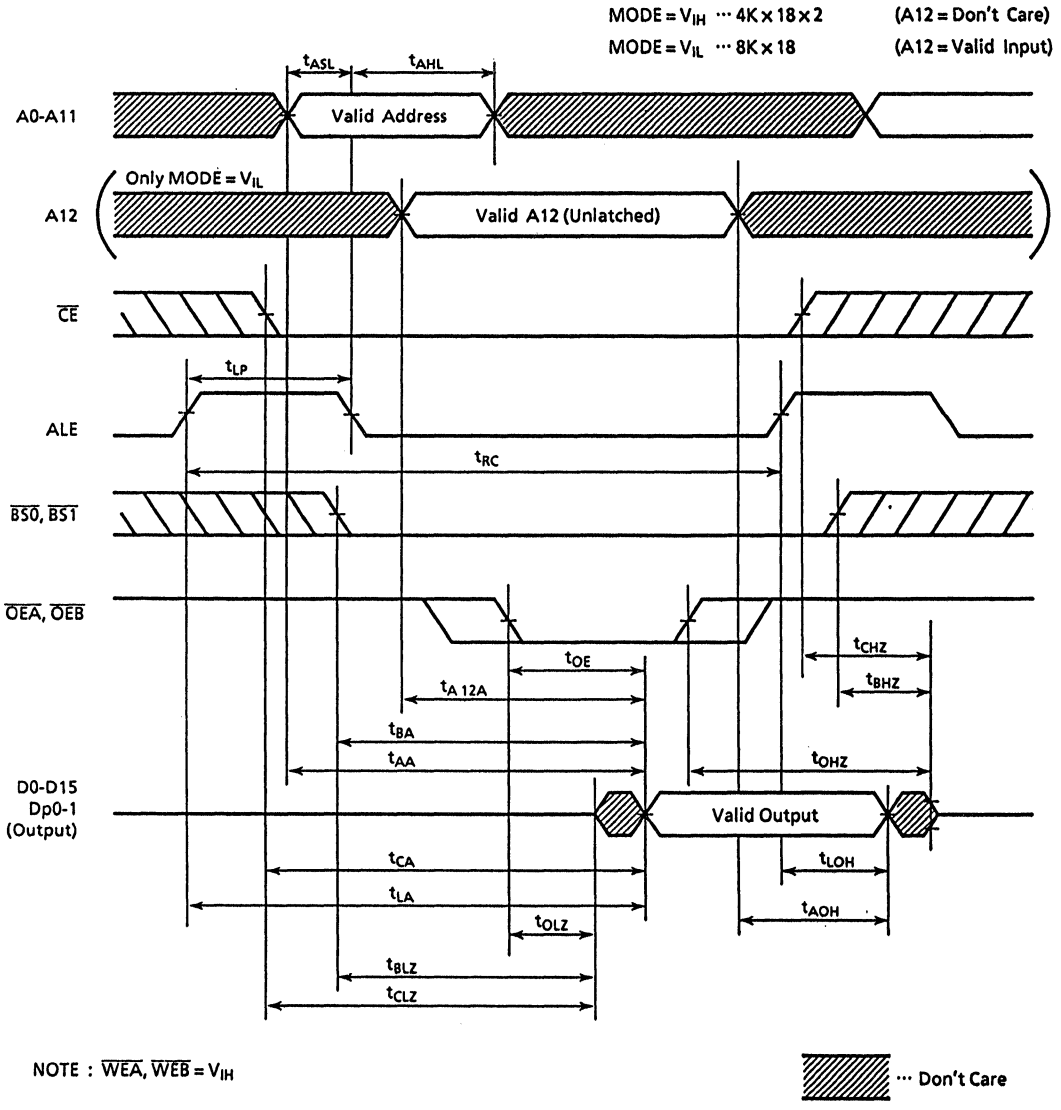
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time (0.3V~2.7V)	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

Fig. 1 OUTPUT LOAD

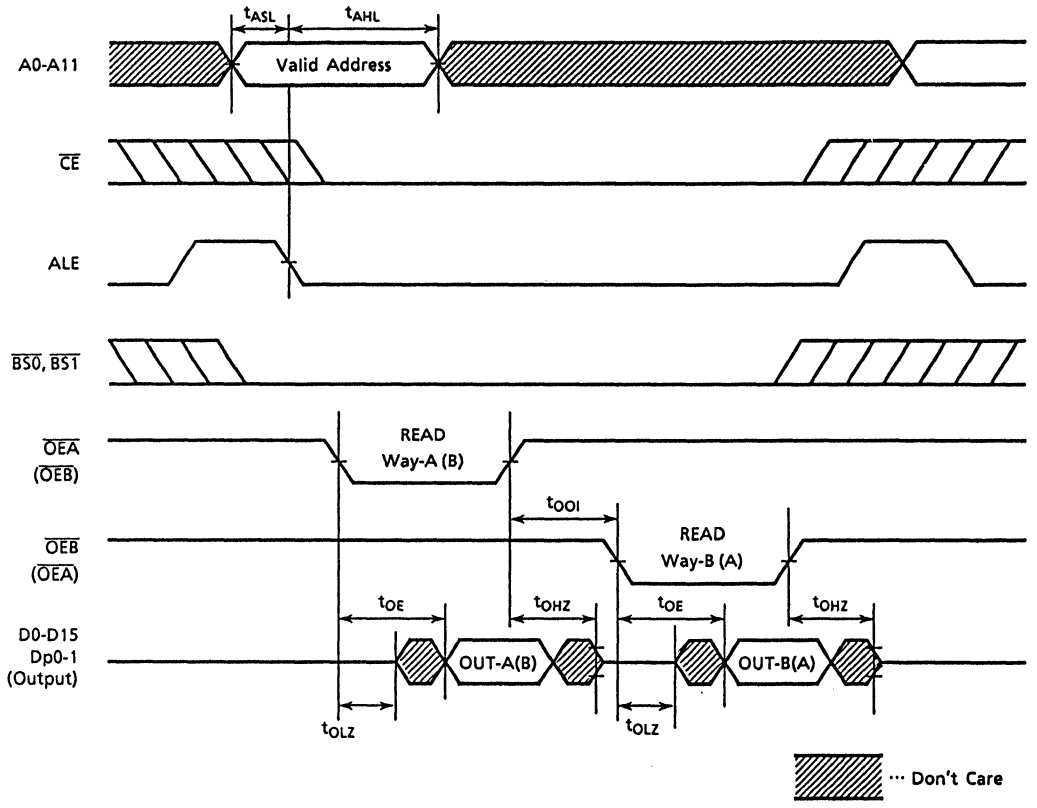


TIMING WAVEFORMS

READ CYCLE TIMING 1

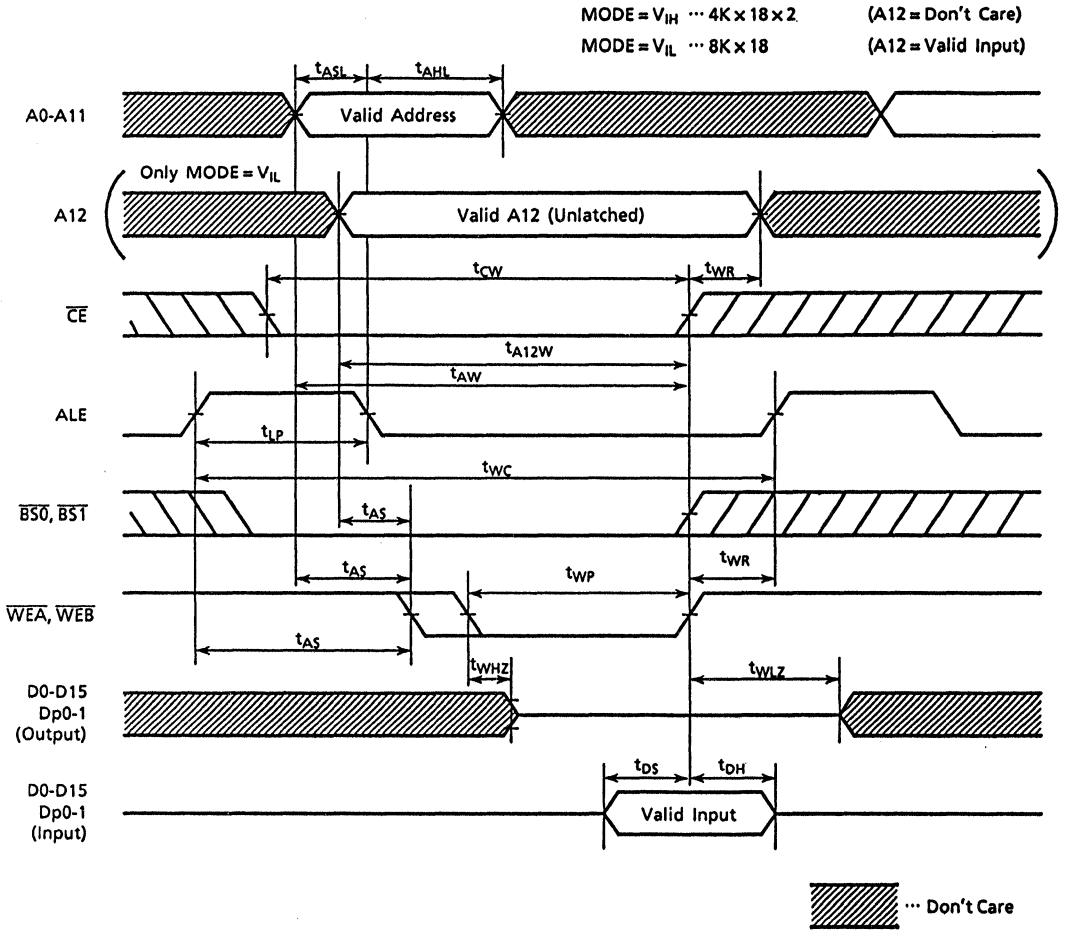


READ CYCLE TIMING 2 (t_{OOI} TIMING . MODE = V_{IH})

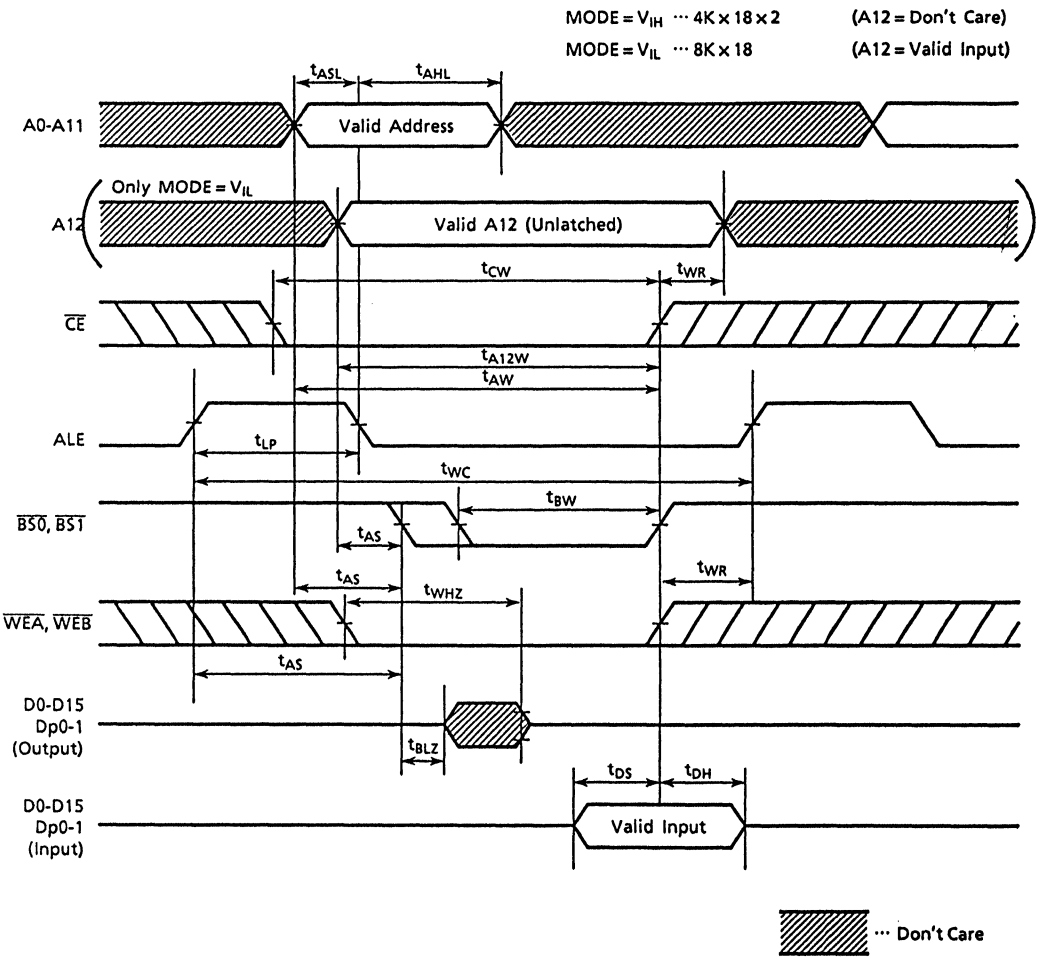


NOTE : $\overline{WEA}$, $\overline{WEB}$ = V_{IH}

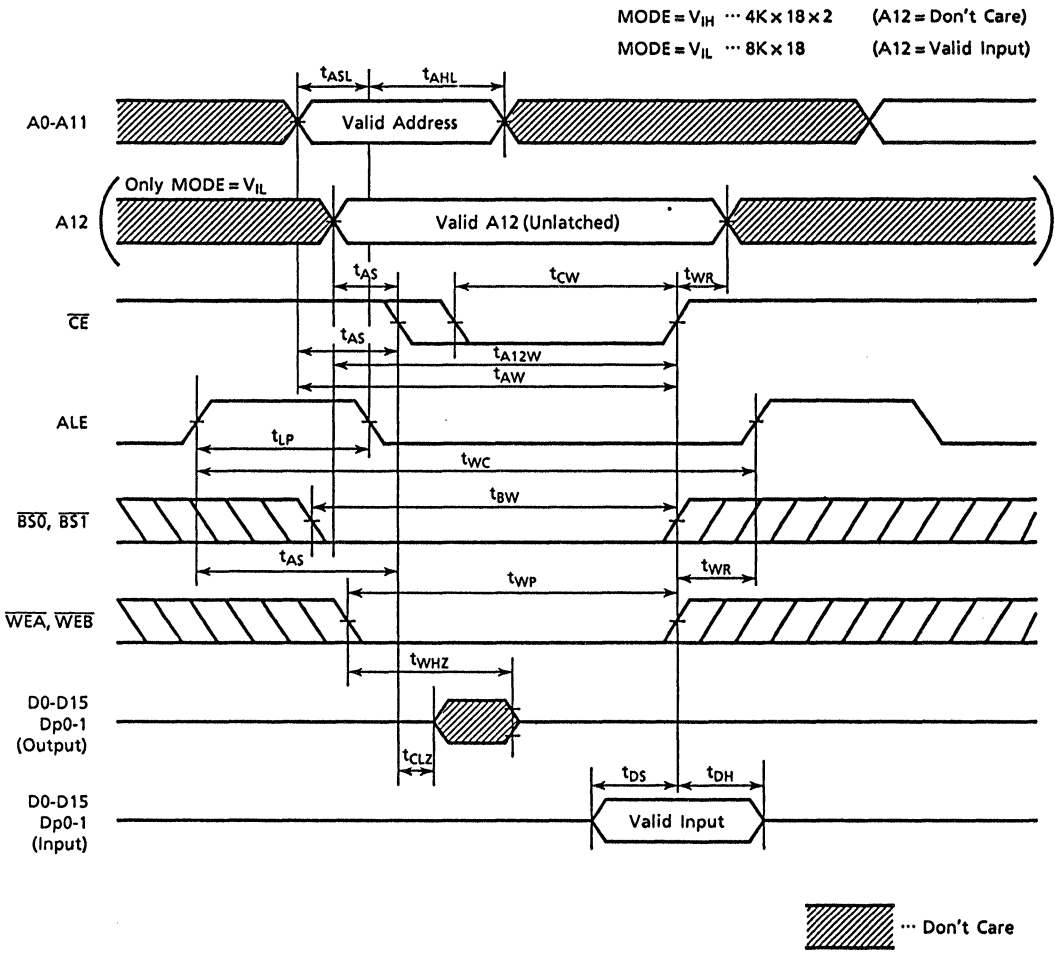
WRITE CYCLE TIMING 1 ($\overline{WE}$ Control)



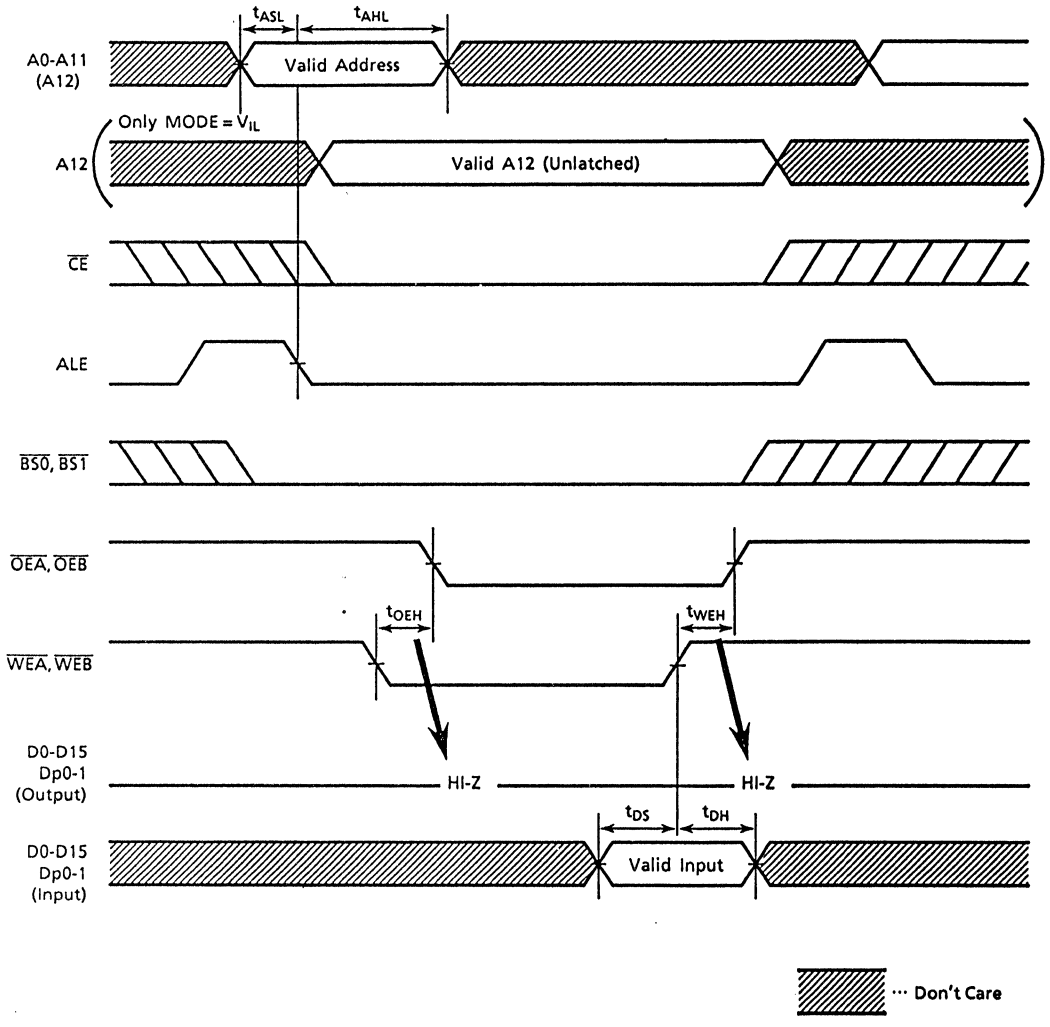
WRITE CYCLE TIMING 2 ($\overline{BS}$ Control)



WRITE CYCLE TIMING 3 ($\overline{CE}$ Control)

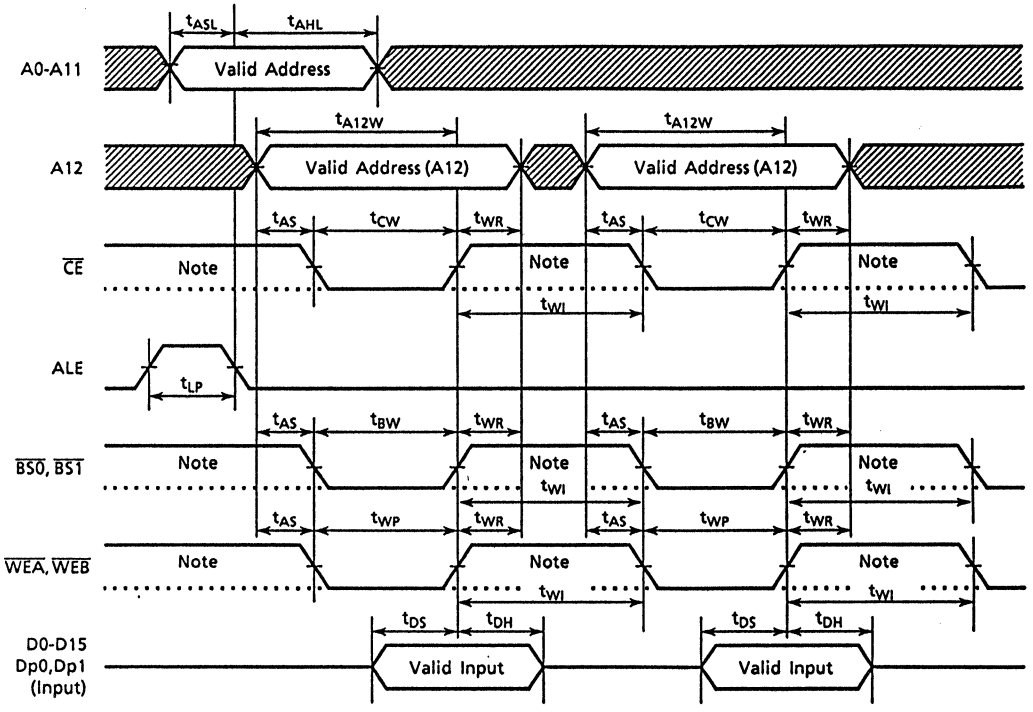


WRITE CYCLE TIMING 4 (t_{OEH} and t_{WEH})



WRITE CYCLE TIMING 5 (A12 Control)

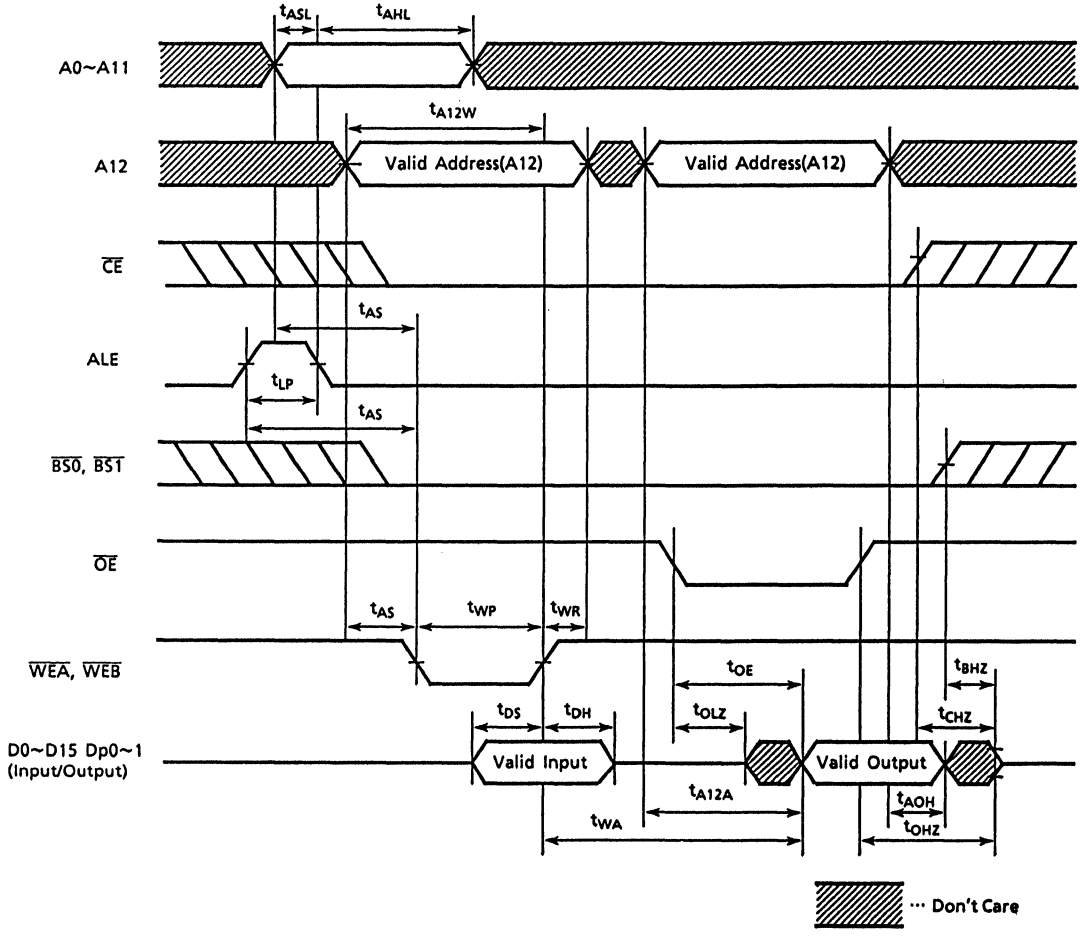
Only MODE = V_{IL} ··· 8K × 18 (A12 = Valid Input)



Note ; t_{WI} ··· Write Command Inhibit Time
($\overline{CE}$ = H or $\overline{BS0}$ = $\overline{BS1}$ = H or $\overline{WEA}$ = $\overline{WEB}$ = H)

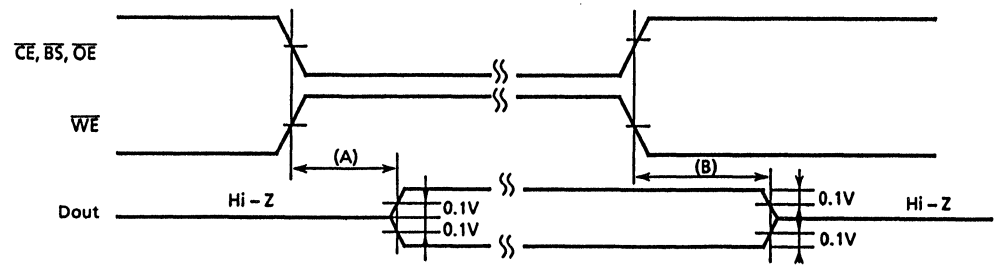
··· Don't Care

READ AFTER WRITE CYCLE TIMING



NOTE : These parameters are specified as follows and measured by using load shown in Fig.1

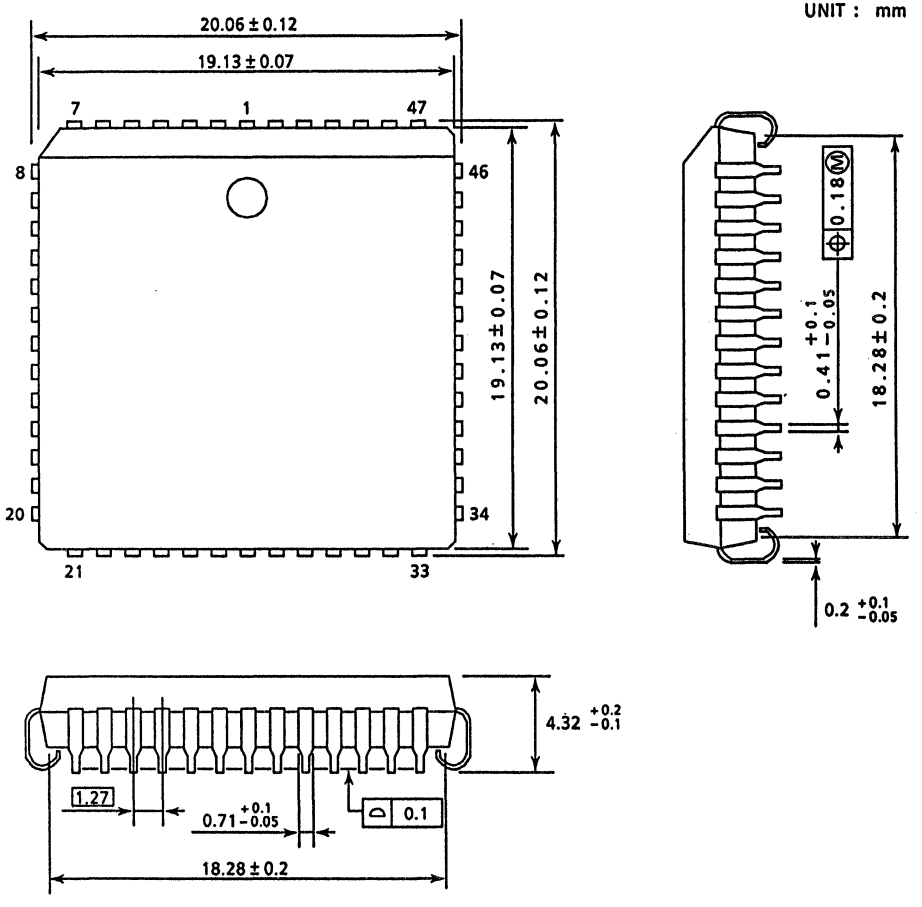
(A) t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{WLZ} ··· Output Enable Time
(B) t_{CHZ}, t_{BHZ}, t_{OHZ}, t_{WHZ} ··· Output Disable Time



OUTLINE DRAWING

QFJ52-P-S750

UNIT : mm



2-WAY 4,096 WORDS × 18 BITS / 8,192 WORDS × 18 BITS CMOS STATIC CACHE DATA RAM

DESCRIPTION

The TC55188T is a 147,456 bits high-speed static RAM which can be user-configured either as 2-way 4,096 words by 18 bits or as 8,192 words by 18 bits. It is provided with a byte control, on-chip address latches and chip-enable latch. The TC55188T is fabricated using Toshiba's CMOS technology and advanced circuit techniques which provide the high speed accesses. The TC55188T operates from a single 5-volt supply. This device features address access time as fast as 20ns, output-enable access as fast as 10ns and simple interfacing capability with bipolar TTL circuits. The TC55188T can directly interface with the INTEL 82385 cache controller, without requiring additional peripheral circuit such as latches, transceivers and gates. Therefore, significant reductions in component count, board assembly area and power dissipation can be achieved by using the TC55188T cache data RAM. The MODE input of the TC55188T allows the user to configure the memory internally either as a 2-way 4,096 words by 18 bits organization suitable for 2-way set associative cache designs or as a 8,192 operated as a conventional asynchronous static RAM, which can be accessed from change of address, by holding the ALE input in the high state. The TC55188T is packaged in a 52-pin standard PLCC for high-density board level assembly.

FEATURES

- Fast Access Time (max.)

ITEM		TC55188T		
		-20	-25	-30
t_{RC}	Cycle Time	20ns	25ns	30ns
t_{AA}	Address Access Time	20ns	25ns	30ns
t_{OE}	$\overline{OE}$ Access Time	10ns	10ns	12ns

- Power dissipation

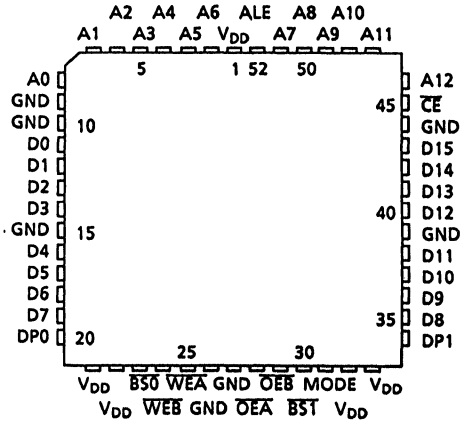
Operating	TC55188T-20	230mA (max.)
	TC55188T-25	220mA (max.)
	TC55188T-30	200mA (max.)
Standby		40mA (max.)

- Configurable for 2-way or direct RAM arrays
  2-way 4,096words×18bits (MODE = V_{IH})
  8,192words×18bits (MODE = V_{IL})
- Contains address latches, $\overline{CE}$ latch and byte control, $\overline{BS0}$ and $\overline{BS1}$
- Interfaces directly with the Intel 82385 Cache Controller
- Single power supply of 5V±10%
- All inputs and outputs TTL compatible
- Two Output buffer controls : $\overline{OEA}$, $\overline{OEB}$
- Two Write enable controls : $\overline{WEA}$, $\overline{WEB}$
- 52pin PLCC package

PIN NAMES

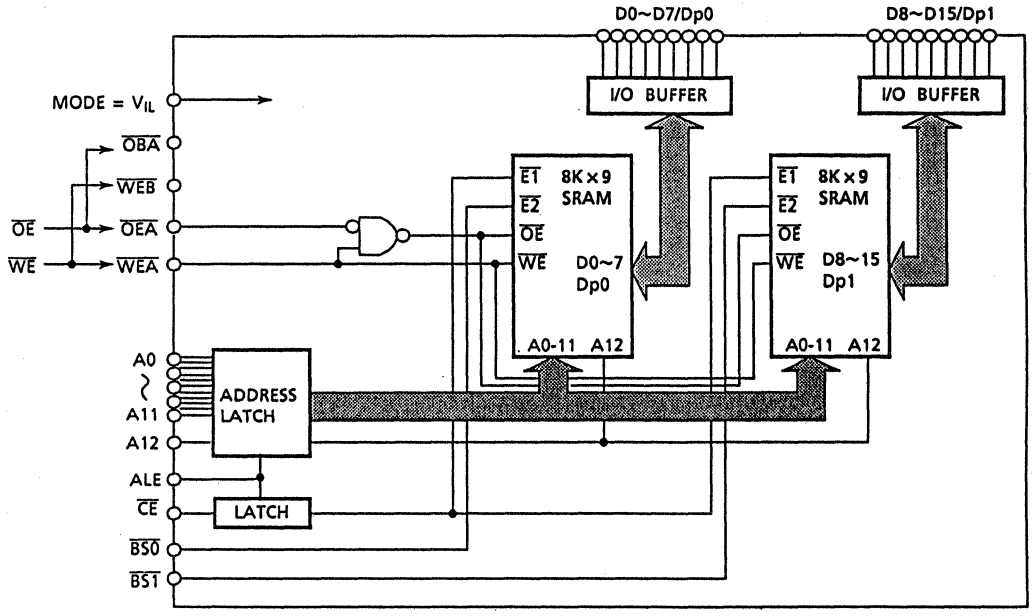
A0~A12	Address Inputs
D0~D15, DP0, DP1	Data Input / Output
ALE	Address / $\overline{CE}$ Latch Input
$\overline{CE}$	Chip Enable Input
$\overline{BS0}$	Lower Byte Select Input
$\overline{BS1}$	Upper Byte Select input
$\overline{OEA}$	Output Enable Input (Way-A)
$\overline{OEB}$	Output Enable Input (Way-B)
$\overline{WEA}$	Write Enable Input (Way-A)
$\overline{WEB}$	Write Enable Input (Way-B)
MODE	Mode Select Input
VDD	Power (+5V)
GND	Ground

PIN CONNECTION (TOP VIEW)

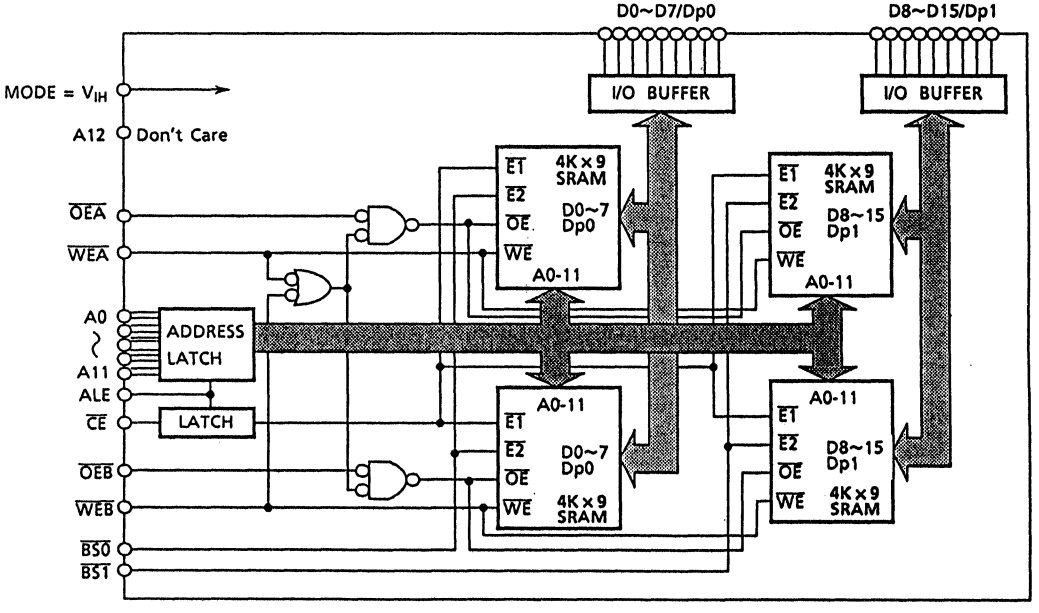


BLOCK DIAGRAM

1–WAY 8,192 words × 18 bits (MODE : V_{IL})



2–WAY 4,096 words × 18 bits (MODE : V_{IH})



TRUTH TABLE 1

CONTROL INPUT			ADDRESS		FUNCTION	
MODE	ALE	$\overline{CE}$	A0~A11	A12	CHIP	CONFIGURATION
H	H	H	*	*	Disable	4K x 18 x 2
H	H	L	Valid	*	Enable	
H	L	* *2	* *2	*	Enable or Disable	
L	H	H	*	*	Disable	8K x 18
L	H	L	Valid	Valid	Enable	
L	L	* *2	* *2	* *2	Enable or Disable	

* : H or L *2 : LATCHED as ALE from H to L.

TRUTH TABLE 2 (MODE = V_{IL} ··· 8K x 18)

INPUTS						OPERATION		
$\overline{WEA}$	$\overline{WEB}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{BS0}$	$\overline{BS1}$	CHIP	D0~D7 Dp0	D8~D15 Dp1
*	*	*	*	H	H	Deselect	Open	Open
H	H	H	H	*	*	Deselect	Open	Open
H	H	L	L	L	H	Read Cycle	Output	Open
				H	L		Open	Output
				L	L		Output	Output
L	L	*	*	L	H	Write Cycle	Input	Open
				H	L		Open	Input
				L	L		Input	Input
H	H	H	L	L	H	Undefine	Undefine	Undefine
				H	L			
				L	L			
H	H	L	H	L	H	Undefine	Undefine	Undefine
				H	L			
				L	L			
H	L	*	*	L	H	Undefine	Undefine	Undefine
				H	L			
				L	L			
L	H	*	*	L	H	Undefine	Undefine	Undefine
				H	L			
				L	L			

* : H or L

TRUTH TABLE 3 (MODE = V_{IH} ··· 4K x 18 x 2)

INPUTS						OPERATION			
$\overline{WEA}$	$\overline{WEB}$	$\overline{OEA}$	$\overline{OEB}$	$\overline{BS0}$	$\overline{BST}$	way-A	way-B	D0~D7 Dp0	D8~D15 Dp1
*	*	*	*	H	H	Deselect	Deselect	Open	Open
H	H	H	H	*	*	Deselect	Deselect	Open	Open
H	H	H	L	L	H	Deselect	Read Cycle	way-B Output	Open
				H	L			Open	way-B Output
				L	L			way-B Output	way-B Output
H	H	L	H	L	H	Read Cycle	Deselect	way-A Output	Open
				H	L			Open	way-A Output
				L	L			way-A Output	way-A Output
H	H	L	L	L	H	Deselect	Deselect	Open	Open
				H	L				
				L	L				
H	L	*	*	L	H	Deselect	Write Cycle	way-B Input	Open
				H	L			Open	way-B Input
				L	L			way-B Input	way-B Input
L	H	*	*	L	H	Write Cycle	Deselect	way-A Input	Open
				H	L			Open	way-A Input
				L	L			way-A Input	way-A Input
L	L	*	*	L	H	Write Cycle	Write Cycle	way-A/B Input	Open
				H	L			Open	way-A/B Input
				L	L			way-A/B Input	way-A/B Input

*: H or L

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.3	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	−65~150	°C
T_{opr}	Operating Temperature	−10~85	°C

DC RECOMMENDED OPERATION CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	−0.5 *	−	0.8	V

* : −3V pulse width less than 10ns.

DC CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}		−1	−	+1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V		−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V		8	−	−	mA
I_{LO}	Output Leakage Current	Output Disable		−1	−	+1	μA
I_{DDO}	Operating Current	V_{DD} = 5.5V, t_{RC}, t_{WC} = min. cycle Address, $\overline{WE}$, ALE = Clock (3.0V/0V), $\overline{OE}$ = 3.0V $\overline{CE}$, $\overline{BS}$ = 0V, MODE = 3.0V or 0V	−20	−	−	230	mA
			−25	−	−	220	
			−30	−	−	200	
I_{DDS}	Standby Current	V_{DD} = 5.5V, $\overline{CE}$, $\overline{BS}$, $\overline{WE}$, $\overline{OE}$ = V_{IH}, ALE = V_{IL} Address, Data, MODE = V_{IH} or V_{IL}		−	−	40	mA

CAPACITANCE (Ta = 25°C, freq = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Cin	Input Capacitance	V_{IN} = GND	−	−	5	pF
Cout	Output Capacitance	V_{OUT} = GND	−	−	7	pF

AC CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{DD} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	-20		-25		-30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	20	-	25	-	30	-	ns
t_{AA}	Address Access Time	-	20	-	25	-	30	ns
t_{LA}	ALE Access Time	-	20	-	25	-	30	ns
t_{CA}	$\overline{CE}$ Access Time	-	20	-	22	-	25	ns
t_{BA}	$\overline{BS}$ Access Time	-	20	-	22	-	25	ns
t_{OE}	$\overline{OE}$ Access Time	-	10	-	10	-	12	ns
t_{ASL}	Address Latch Set-Up Time	4	-	4	-	5	-	ns
t_{AHL}	Address Latch Hold Time	5	-	5	-	5	-	ns
t_{LP}	ALE Pulse Width	8	-	8	-	9	-	ns
t_{AOH}	Output Data Hold Time from Address Change	5	-	5	-	5	-	ns
t_{LOH}	Output Data Hold Time from Address Latch	5	-	5	-	5	-	ns
t_{LLZ}	ALE to Output in Low-Z	5	-	5	-	5	-	ns
t_{CLZ}	$\overline{CE}$ to Output in Low-Z	5	-	5	-	5	-	ns
t_{BLZ}	$\overline{BS}$ to Output in Low-Z	5	-	5	-	5	-	ns
t_{OLZ}	$\overline{OE}$ to Output in Low-Z	0	-	0	-	0	-	ns
t_{LHZ}	ALE to Output in High-Z	-	12	-	12	-	15	ns
t_{CHZ}	$\overline{CE}$ to Output in High-Z	-	10	-	10	-	12	ns
t_{BHZ}	$\overline{BS}$ to Output in High-Z	-	10	-	10	-	12	ns
t_{OHZ}	$\overline{OE}$ to Output in High-Z	-	8	-	8	-	10	ns
t_{OOI}	$\overline{OEA}/\overline{OEB}$ Inhibit Time	8	-	8	-	10	-	ns

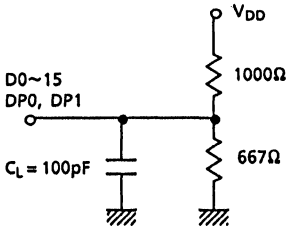
WRITE CYCLE

SYMBOL	PARAMETER	-20		-25		-30		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	20	-	25	-	30	-	ns
t_{WP}	$\overline{WE}$ Pulse Width	12	-	15	-	18	-	ns
t_{BW}	$\overline{BS}$ to End of Write	12	-	15	-	18	-	ns
t_{CW}	$\overline{CE}$ to End of Write	12	-	15	-	18	-	ns
t_{AW}	Write Address to End of Write	12	-	15	-	18	-	ns
t_{AS}	Write Address Set-Up Time	0	-	0	-	0	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{DS}	Data Set-Up Time	8	-	10	-	10	-	ns
t_{DH}	Data Hold Time	0	-	0	-	0	-	ns
t_{WLZ}	$\overline{WE}$ to Output in Low-Z	5	-	5	-	5	-	ns
t_{WHZ}	$\overline{WE}$ to Output in High-Z	-	7	-	8	-	10	ns
t_{OEH}	$\overline{OE}$ Command Hold Time	5	-	5	-	5	-	ns
t_{WEH}	$\overline{WE}$ Command Hold Time	-	5	-	5	-	5	ns
t_{WI}	Write Command Inhibit Time	10	-	10	-	10	-	ns

AC TEST CONDITIONS

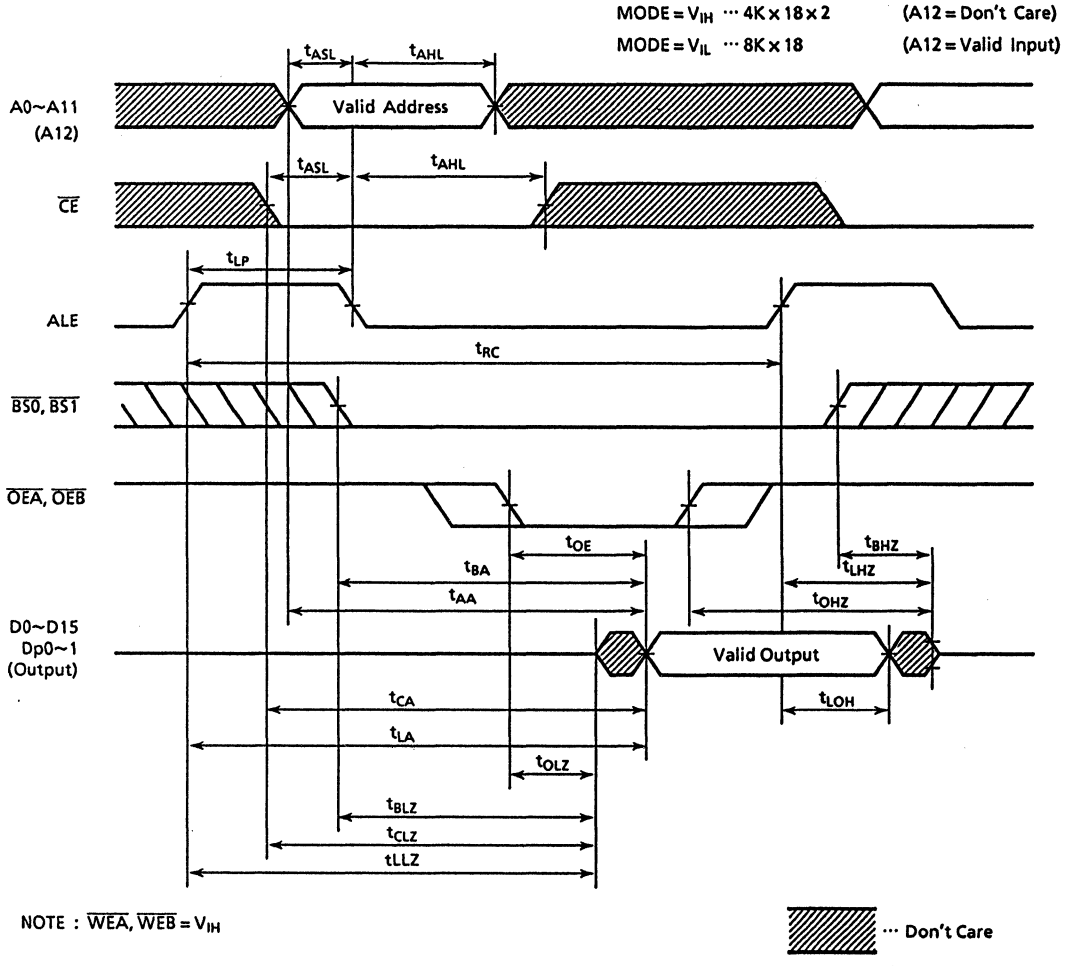
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time (0.3V~2.7V)	3ns
Input Timing Measurement Reference Level	1.5V
Output Timing Measurement Reference Level	1.5V
Output Load	Fig. 1

Fig. 1 OUTPUT LOAD



TIMING WAVEFORMS

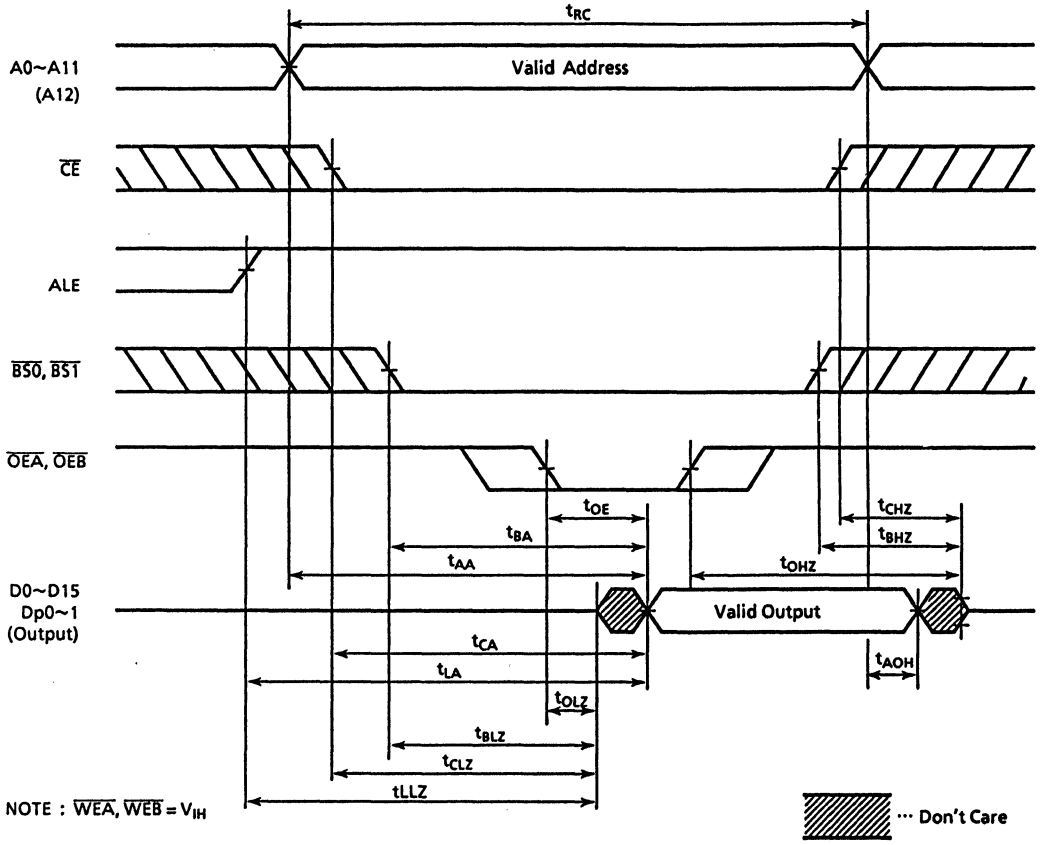
READ CYCLE TIMING 1 (ALE=Clock)



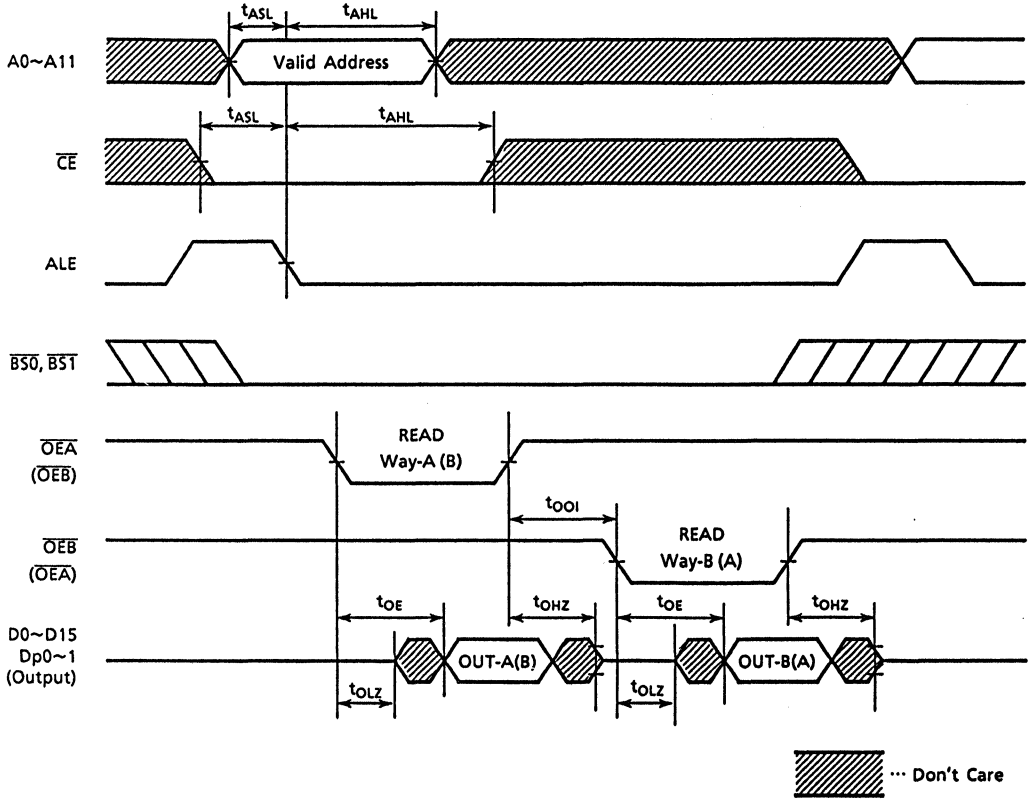
NOTE : $\overline{WEA}$, $\overline{WEB}$ = V_{IH}

READ CYCLE TIMING 2 (ALE = V_{IH})

MODE = V_{IH} ··· 4K × 18 × 2 (A12 = Don't Care)
MODE = V_{IL} ··· 8K × 18 (A12 = Valid Input)

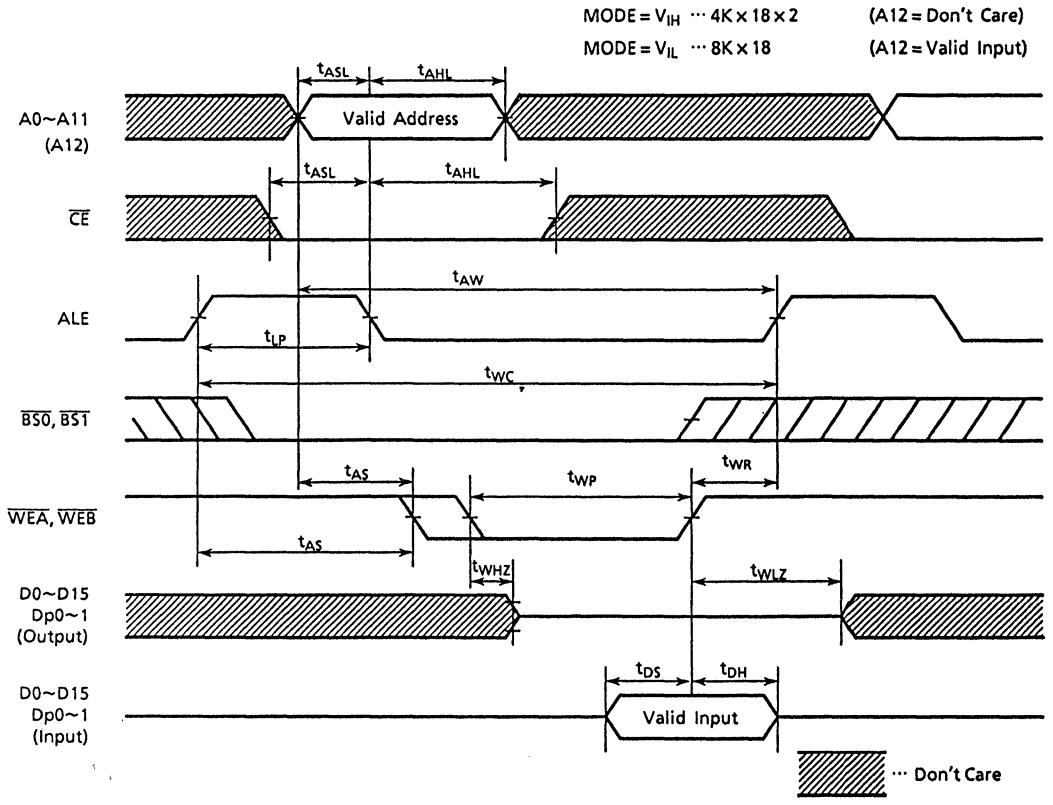


READ CYCLE TIMING 3 (t_{OOI} TIMING . MODE = V_{IH})

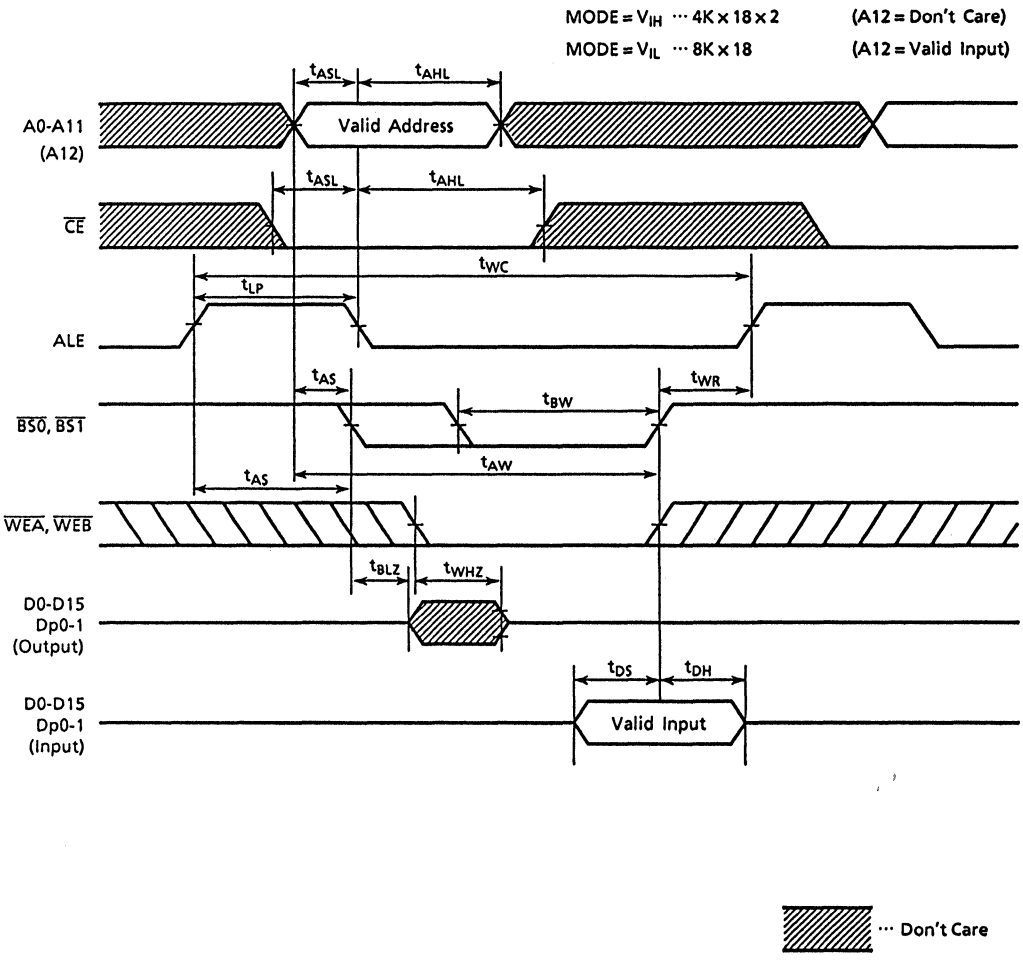


NOTE : $\overline{WEA}$, $\overline{WEB}$ = V_{IH}

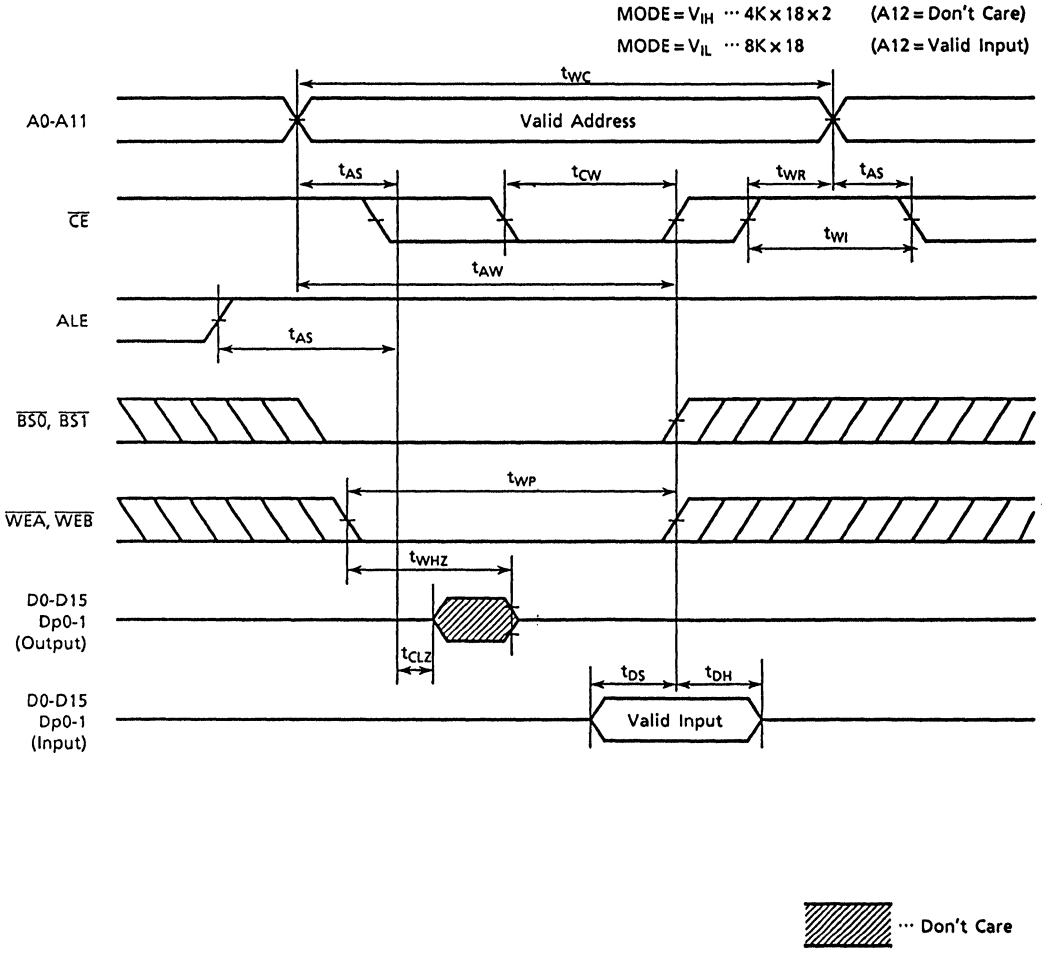
WRITE CYCLE TIMING 1 ($\overline{WE}$ Control)



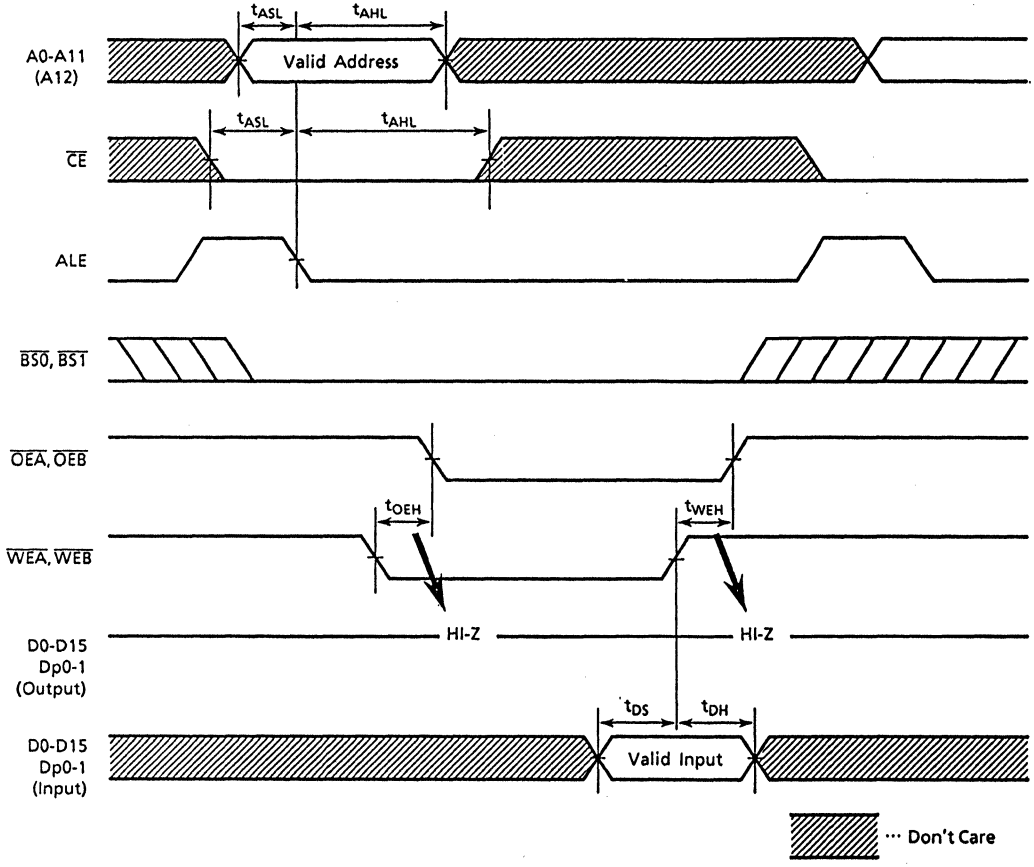
WRITE CYCLE TIMING 2 ($\overline{BS}$ Control)



WRITE CYCLE TIMING 3 ($\overline{CE}$ Control)

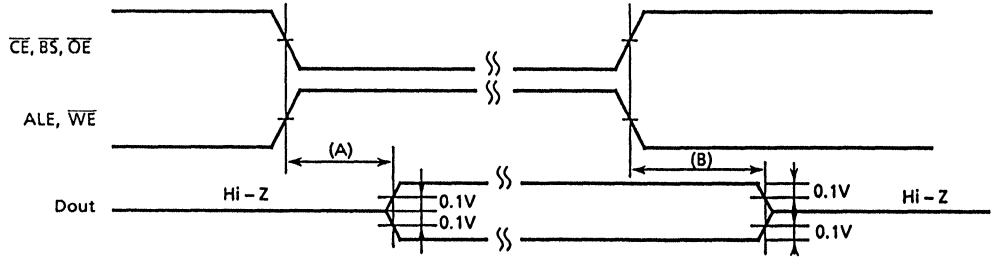


WRITE CYCLE TIMING 4 (t_{OEH} and t_{WEH})



NOTE : These parameters are specified as follows and measured by using load shown in Fig.1

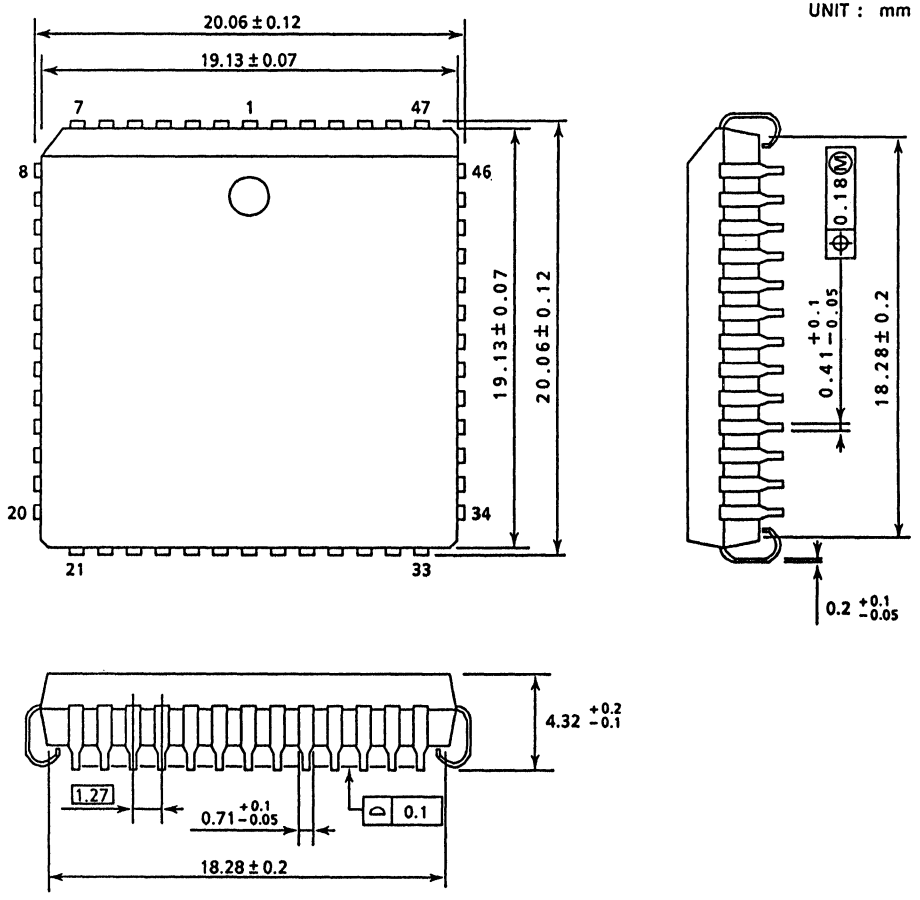
(A) t_{LLZ}, t_{CLZ}, t_{BLZ}, t_{OLZ}, t_{WLZ} ··· Output Enable Time
(B) t_{LHZ}, t_{CHZ}, t_{BHZ}, t_{OHZ}, t_{WHZ} ··· Output Disable Time



OUTLINE DRAWING

QFJ52-P-S750

UNIT : mm



65,536 WORD x 4 BIT CMOS STATIC RAM

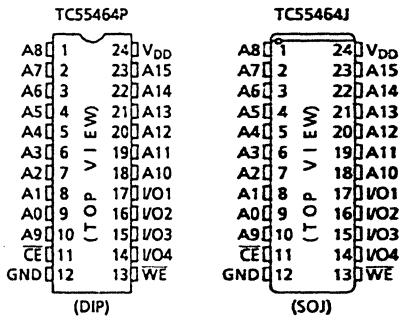
DESCRIPTION

The TC55464P/J is a 262,144 bit high-speed static random access memory organized as 65,536 words by 4 bits using CMOS technology, and operates from a single 5 volt supply. Toshiba's advanced CMOS circuitry provides high-speed characteristics. The TC55464P/J has low stand-by power using Chip Enable ($\overline{CE}$). The TC55464P/J is suitable for use as cache memory where high speed is required. All inputs and outputs are directly TTL compatable. The TC55464P/J is offered in standard 24 pin 300 mil DIP and SOJ packages for high density assembly.

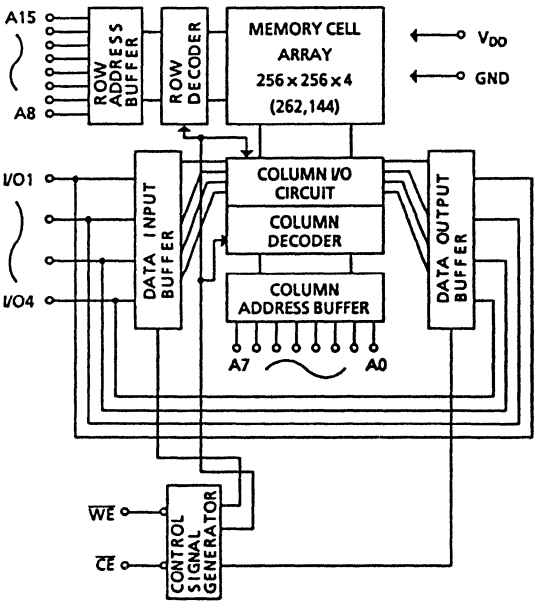
FEATURES

- Fast access time :
  - TC55464P/J-17 17ns(MAX.)
  - TC55464P/J-20 20ns(MAX.)
  - TC55464P/J-25 25ns(MAX.)
  - TC55464P/J-35 35ns(MAX.)
- Low power dissipation
  - Operation : TC55464P/J-17 120mA(MAX.)
  - TC55464P/J-20 120mA(MAX.)
  - TC55464P/J-25 120mA(MAX.)
  - TC55464P/J-35 100mA(MAX.)
  - Standby : 1mA(MAX.)
- 5V single power supply :
  - -17 : 5V±5%
  - -20/25/35 : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Package
  - 24pin plastic 300 mil DIP : TC55464P
  - 24pin plastic 300 mil SOJ : TC55464J

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0~A15	Address Inputs
I/O1~I/O4	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
V_{DD}	Power(+ 5V)
GND	Ground

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	−65~150	°C
T_{opr}	Operating Temperature	−10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	−17	4.75	5.0	5.25	V
		−20/25/35	4.5	5.0	5.5	
V_{IH}	Input High Voltage		2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage		−0.5 *	−	0.8	V

* −3V Pulse Width : 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, −17 : V_{DD} = 5V ± 5%, −20/25/35 : V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}			−	−	±1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0~V_{DD}			−	−	±1	μA
I_{DDO}	Operating Current	tcycle = Min cycle	V_{DD} = 5.25V	−17	−	−	120	mA
		$\overline{CE}$ = V_{IL}	V_{DD} = 5.5V	−20	−	−	120	
		Other Input = V_{IH}/V_{IL}		−25	−	−	120	
				−35	−	−	100	
I_{DDS1}	Standby Current	tcycle = Min cycle	V_{DD} = 5.25V	−17	−	−	20	mA
		$\overline{CE}$ = V_{IH}	V_{DD} = 5.5V	−20				
		Other Input = V_{IH}/V_{IL}		−25				
				−35				
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2V Other Input = V_{DD} − 0.2V or 0.2V			−	−	1	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS ($Ta = 0 \sim 70°C$ (1), $-17: V_{DD} = 5V \pm 5\%$, $-20/25/35: V_{DD} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC55464P/J-17		TC55464P/J-20		TC55464P/J-25		TC55464P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	17	–	20	–	25	–	35	–	ns
t_{ACC}	Address Access Time	–	17	–	20	–	25	–	35	ns
t_{CO}	$\overline{CE}$ Access Time	–	17	–	20	–	25	–	35	ns
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	5	–	ns
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	5	–	ns
t_{COD}	Output Disable Time from $\overline{CE}$	–	10	–	10	–	10	–	15	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	17	–	20	–	25	–	35	ns

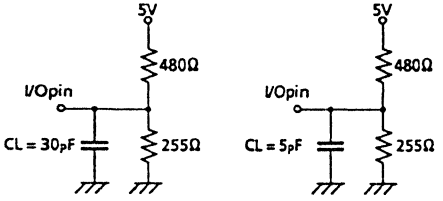
WRITE CYCLE

SYMBOL	PARAMETER	TC55464P/J-17		TC55464P/J-20		TC55464P/J-25		TC55464P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	17	–	20	–	25	–	35	–	ns
t_{CW}	Chip Enable to End of Write	13	–	13	–	15	–	20	–	ns
t_{AS}	Address Set Up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	13	–	13	–	15	–	20	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DS}	Data Set Up Time	10	–	10	–	12	–	15	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{OEW}	Output Enable Time from $\overline{WE}$	0	–	0	–	0	–	0	–	ns
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	8	–	10	–	15	ns

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

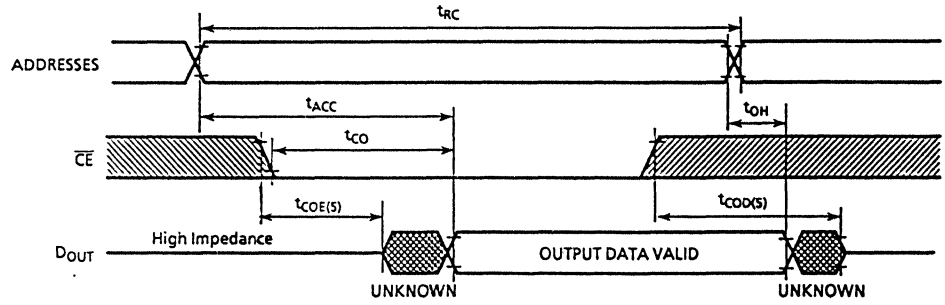
Fig. 1



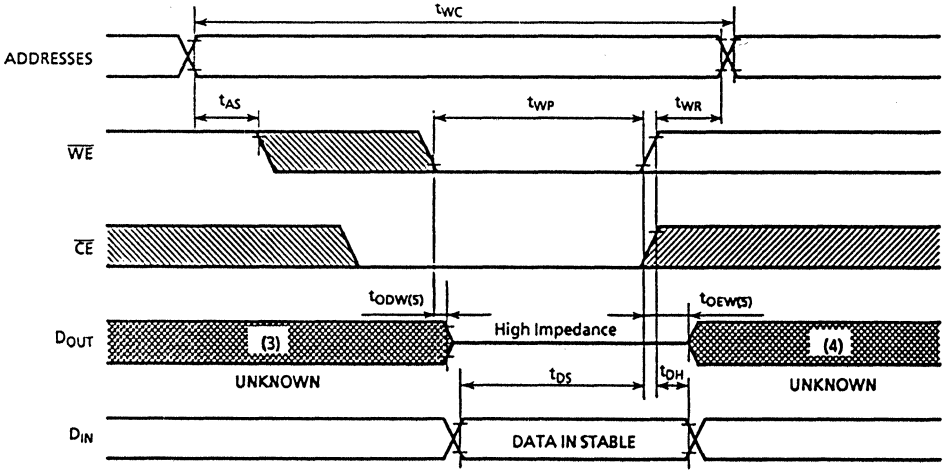
(For t_{COE}, t_{COD}, t_{OEW} and t_{ODW})

TIMING WAVEFORMS

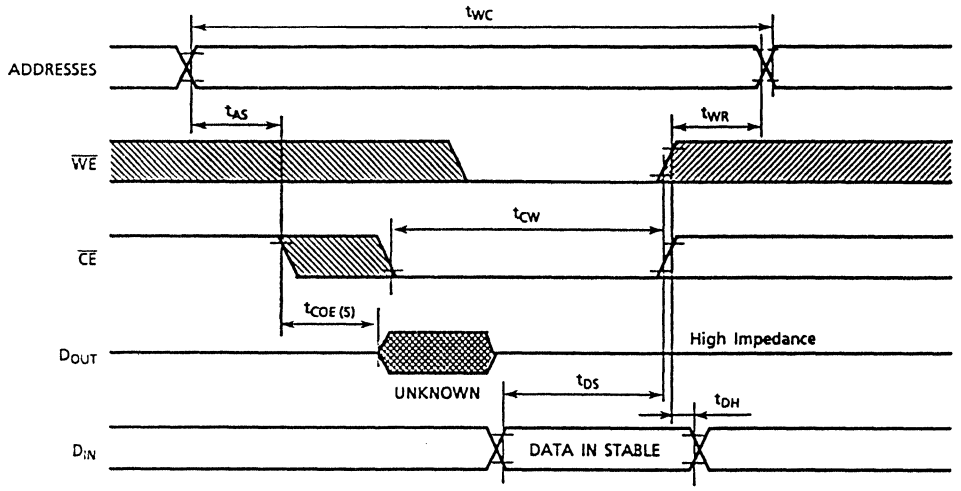
READ CYCLE (2)



WRITE CYCLE 1 ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 ($\overline{CE}$ Controlled Write)



Note: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

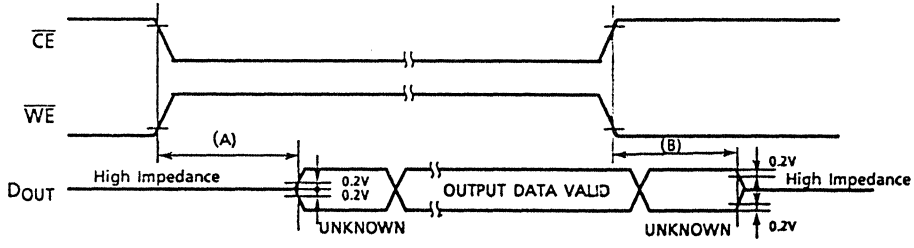
3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. These parameters are specified as follows and measured by using the load shown in Fig. 1.

   (A) t_{COE}, t_{OEW} ····· Output Enable Time

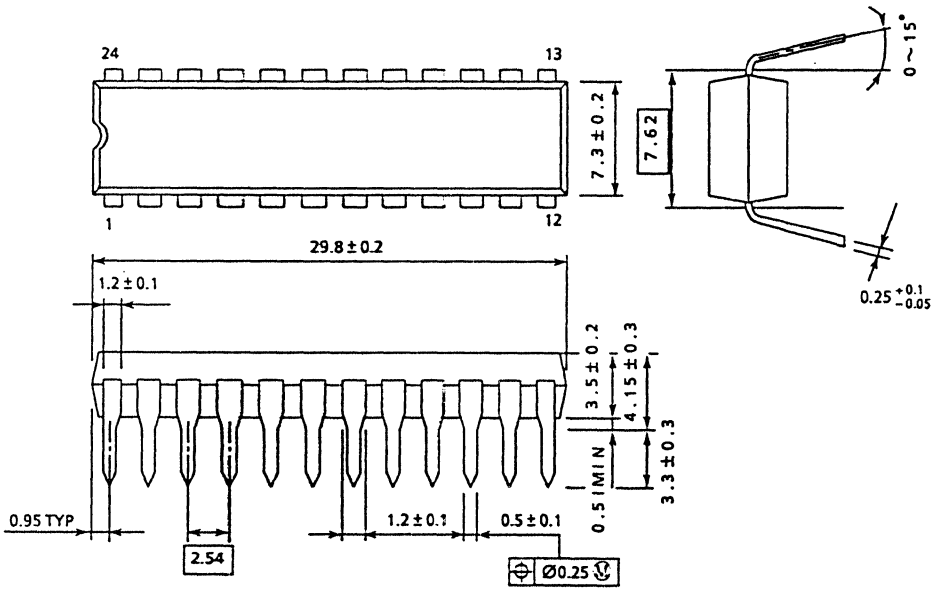
   (B) t_{COD}, t_{ODW} ····· Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP24-P-300B)

Unit in mm

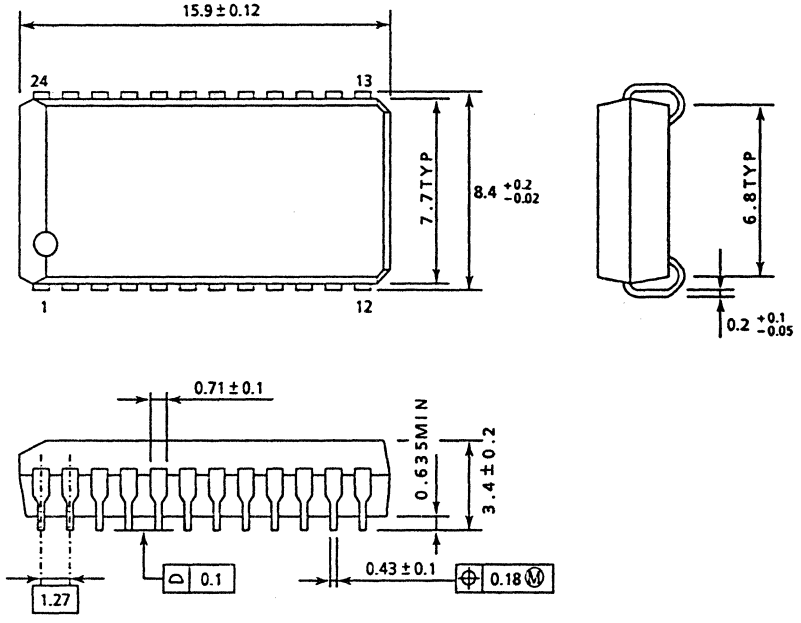


Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15 mm.

OUTLINE DRAWINGS

Plastic SOJ (SOJ24 - P - 300)

Unit in mm



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15 mm.

65,536 WORD x 4 BIT CMOS STATIC RAM

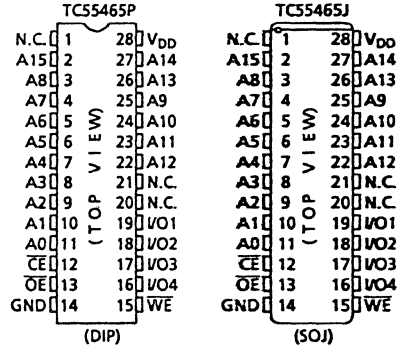
DESCRIPTION

The TC55465P/J is a 262,144 bit high-speed static random access memory organized as 65,536 words by 4 bits using CMOS technology, and operates from a single 5 volt supply. Toshiba's advanced CMOS circuitry provides high-speed characteristics. The TC55465P/J has low stand-by power using Chip Enable ($\overline{CE}$), and has fast memory accesses using Output Enable ($\overline{OE}$). The TC55465P/J is suitable for use as cache memory where high speed is required. All inputs and outputs are directly TTL compatable. The TC55465P/J is offered in standard 28 pin 300 mil DIP and SOJ packages for high density assembly.

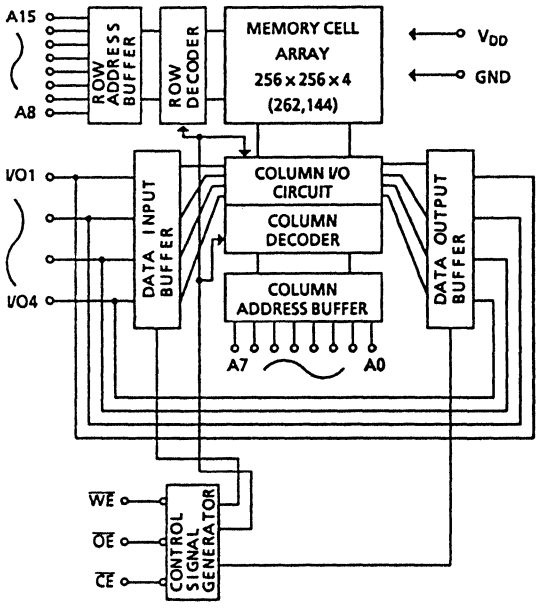
FEATURES

- Fast access time:
  - TC55465P/J-17 17ns(MAX.)
  - TC55465P/J-20 20ns(MAX.)
  - TC55465P/J-25 25ns(MAX.)
  - TC55465P/J-35 35ns(MAX.)
- Low power dissipation
  - Operation : TC55465P/J-17 120mA(MAX.)
  - TC55465P/J-20 120mA(MAX.)
  - TC55465P/J-25 120mA(MAX.)
  - TC55465P/J-35 100mA(MAX.)
  - Standby : 1mA(MAX.)
- 5V single power supply :
  - −17 : 5V±5%
  - −20/25/35 : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Package
  - 28 pin plastic 300 mil DIP : TC55465P
  - 28 pin plastic 300 mil SOJ : TC55465J

PIN CONNECTION



BLOCK DIAGRAM



PIN NAMES

A0~A15	Address Inputs
I/01~I/04	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
$V_{I/O}$	Input / Output Voltage	−0.5~V_{DD} + 0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	−65~150	°C
T_{opr}	Operating Temperature	−10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	−17	4.75	5.0	5.25	V
		−20/25/35	4.5	5.0	5.5	
V_{IH}	Input High Voltage		2.2	−	V_{DD} + 0.5	V
V_{IL}	Input Low Voltage		−0.5 *	−	0.8	V

* −3V Pulse Width : 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, −17 : V_{DD} = 5V ± 5%, −20/25/35 : V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}			−	−	±1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0~V_{DD}			−	−	±1	μA
I_{DDO}	Operating Current	tcycle = Min cycle $\overline{CE}$ = V_{IL} Other Input = V_{IH}/V_{IL}	V_{DD} = 5.25V	−17	−	−	120	mA
			V_{DD} = 5.5V	−20	−	−	120	
				−25	−	−	120	
				−35	−	−	100	
I_{DDS1}	Standby Current	tcycle = Min cycle $\overline{CE}$ = V_{IH} Other Input = V_{IH}/V_{IL}	V_{DD} = 5.25V	−17	−	−	20	mA
			V_{DD} = 5.5V	−20				
				−25				
				−35				
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2V Other Input = V_{DD} − 0.2V or 0.2V			−	−	1	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS ($Ta = 0 \sim 70°C$ (1), $-17: V_{DD} = 5V \pm 5\%$, $-20/25/35: V_{DD} = 5V \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC55465P/J-17		TC55465P/J-20		TC55465P/J-25		TC55465P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	17	–	20	–	25	–	35	–	ns
t_{ACC}	Address Access Time	–	17	–	20	–	25	–	35	ns
t_{CO}	$\overline{CE}$ Access Time	–	17	–	20	–	25	–	35	ns
t_{OE}	$\overline{OE}$ Access Time	–	9	–	10	–	12	–	15	ns
t_{OH}	Output Data Hold Time from Address Change	5	–	5	–	5	–	5	–	ns
t_{COE}	Output Enable Time from $\overline{CE}$	5	–	5	–	5	–	5	–	ns
t_{COD}	Output Disable Time from $\overline{CE}$	–	10	–	10	–	10	–	15	ns
t_{OEE}	Output Enable Time from $\overline{OE}$	0	–	0	–	0	–	0	–	ns
t_{ODO}	Output Disable Time from $\overline{OE}$	–	8	–	8	–	10	–	15	ns
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Deselection to Power Down Time	–	17	–	20	–	25	–	35	ns

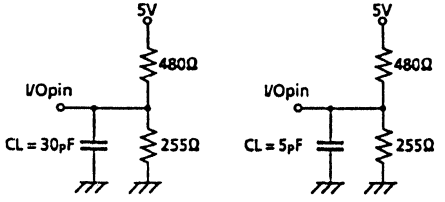
WRITE CYCLE

SYMBOL	PARAMETER	TC55465P/J-17		TC55465P/J-20		TC55465P/J-25		TC55465P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	17	–	20	–	25	–	35	–	ns
t_{CW}	Chip Enable to End of Write	13	–	13	–	15	–	20	–	ns
t_{AS}	Address Set Up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	13	–	13	–	15	–	20	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{DS}	Data Set Up Time	10	–	10	–	12	–	15	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{OEW}	Output Enable Time from $\overline{WE}$	0	–	0	–	0	–	0	–	ns
t_{ODW}	Output Disable Time from $\overline{WE}$	–	8	–	8	–	10	–	15	ns

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig. 1

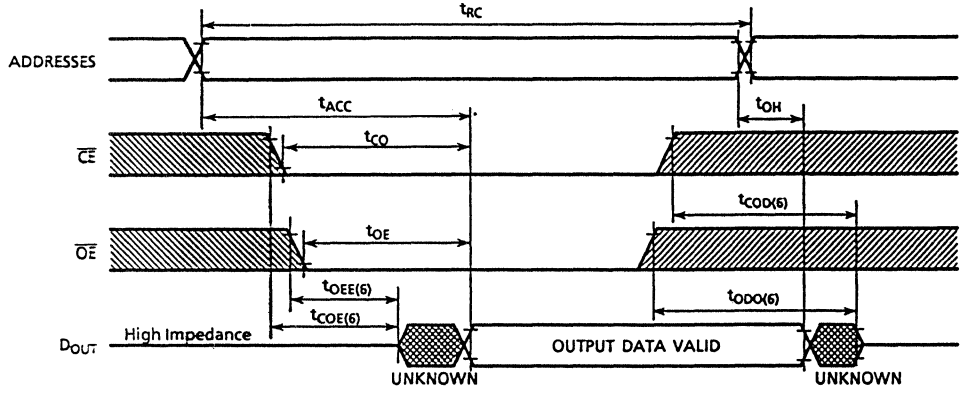
Fig. 1



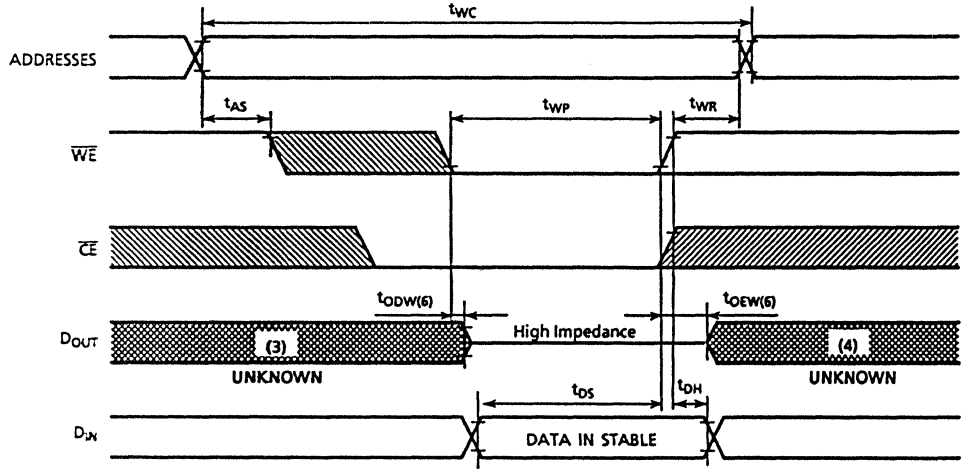
(For t_{COE}, t_{OEE}, t_{COD}, t_{ODO}, t_{OEW} and t_{ODW})

TIMING WAVEFORMS

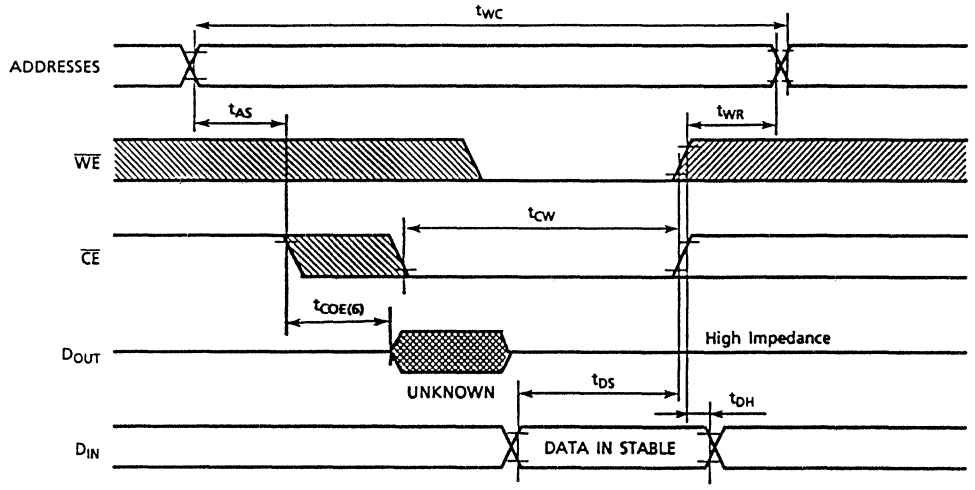
READ CYCLE (2)



WRITE CYCLE1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE2 (5) ($\overline{CE}$ Controlled Write)



NOTE: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

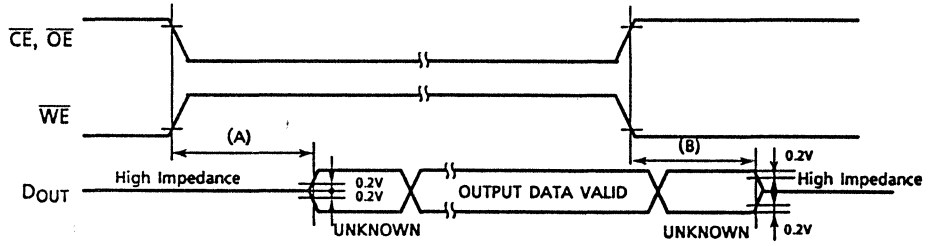
4. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig.1.

   (A) t_{COE}, t_{OEE}, t_{OEW} ····· Output Enable Time

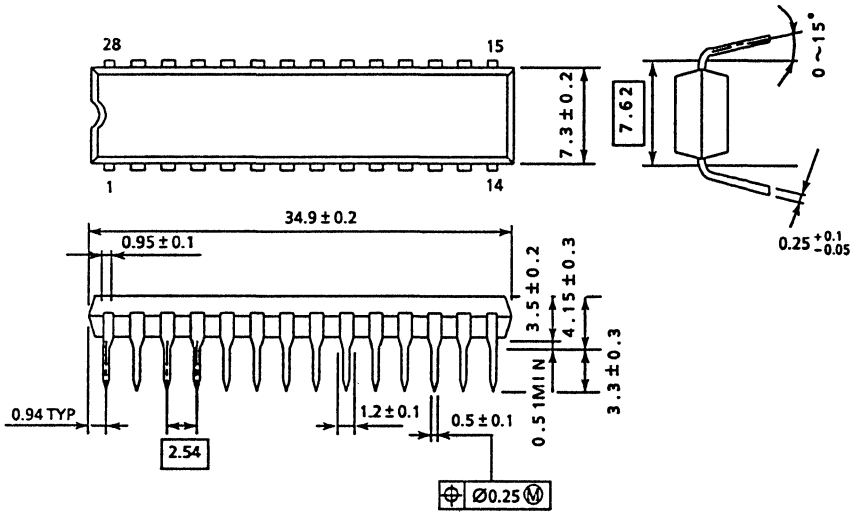
   (B) t_{COD}, t_{ODO}, t_{ODW} ····· Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP28-P-300B)

Unit in mm

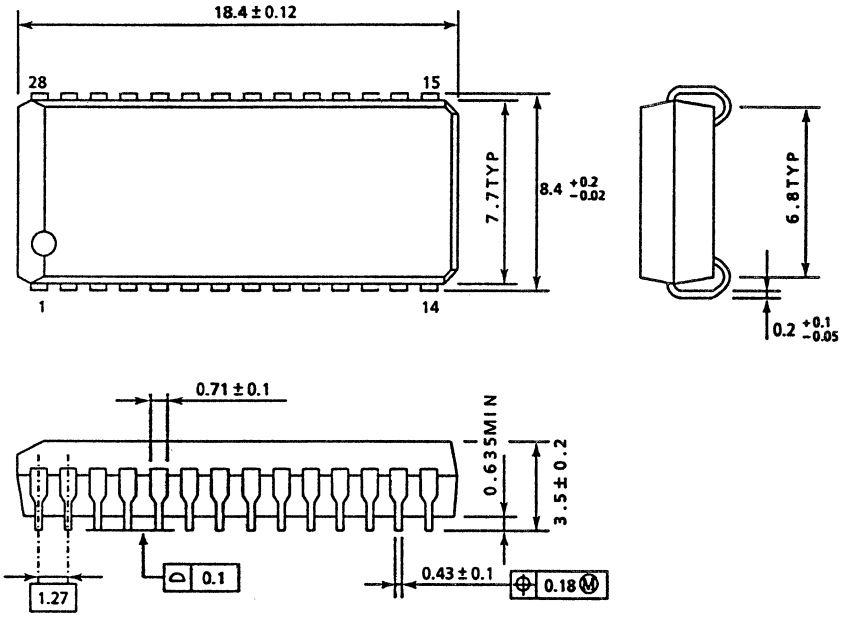


Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

Plastic SOJ (SOJ28-P-300)

Unit in mm



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm

32,768 WORD x 8 BIT CMOS STATIC RAM

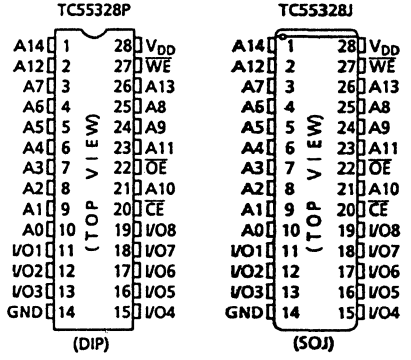
DESCRIPTION

The TC55328P/J is a 262,144 bit high-speed static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operates from a single 5 volt supply. Toshiba's advanced CMOS circuitry provides high-speed characteristics. The TC55328P/J has low stand-by power using Chip Enable ($\overline{CE}$), and has fast memory accesses using Output Enable ($\overline{OE}$). The TC55328P/J is suitable for use as cache memory where high speed is required. All inputs and outputs are directly TTL compatable. The TC55328P/J is offered in standard 28 pin 300 mil DIP and SOJ packages for high density assembly.

FEATURES

- Fast access time:
  - TC55328P/J-17 17ns(MAX.)
  - TC55328P/J-20 20ns(MAX.)
  - TC55328P/J-25 25ns(MAX.)
  - TC55328P/J-35 35ns(MAX.)
- Low power dissipation
  - Operation : TC55328P/J-17 140mA(MAX.)
  - TC55328P/J-20 140mA(MAX.)
  - TC55328P/J-25 140mA(MAX.)
  - TC55328P/J-35 120mA(MAX.)
  - Standby : 1mA(MAX.)
- 5V single power supply :
  - −17 : 5V±5%
  - −20/25/35 : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Package
  - 28 pin plastic 300 mil DIP : TC55328P
  - 28 pin plastic 300 mil SOJ : TC55328J

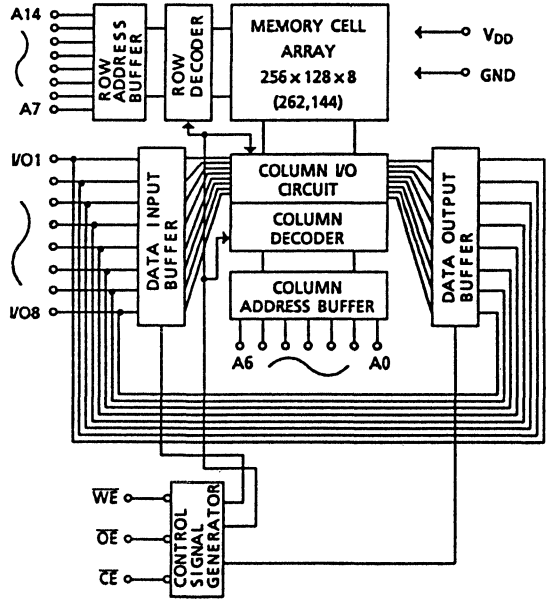
PIN CONNECTION



PIN NAMES

A0~A14	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
$V_{I/O}$	Input / Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260 · 10	°C · sec
T_{strg}	Storage Temperature	−65~150	°C
T_{opr}	Operating Temperature	−10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	−17	4.75	5.0	5.25	V
		−20/25/35	4.5	5.0	5.5	
V_{IH}	Input High Voltage		2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage		−0.5 *	−	0.8	V

* −3V Pulse Width : 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, −17 : V_{DD} = 5V ± 5%, −20/25/35 : V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}			−	−	±1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, V_{OUT} = 0~V_{DD}			−	−	±1	μA
I_{DDO}	Operating Current	tcycle = Min cycle $\overline{CE}$ = V_{IL} Other Input = V_{IH} / V_{IL}	V_{DD} = 5.25V	−17	−	−	140	mA
			V_{DD} = 5.5V	−20	−	−	140	
				−25	−	−	140	
				−35	−	−	120	
I_{DDS1}	Standby Current	tcycle = Min cycle $\overline{CE}$ = V_{IH} Other Input = V_{IH} / V_{IL}	V_{DD} = 5.25V	−17	−	−	20	mA
			V_{DD} = 5.5V	−20				
				−25				
				−35				
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2V Other Input = V_{DD} − 0.2V or 0.2V			−	−	1	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C (1), -17 : V_{DD} = 5V ± 5%, -20/25/35 : V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55328P/J-17		TC55328P/J-20		TC55328P/J-25		TC55328P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	17	-	20	-	25	-	35	-	ns
t_{ACC}	Address Access Time	-	17	-	20	-	25	-	35	
t_{CO}	$\overline{CE}$ Access Time	-	17	-	20	-	25	-	35	
t_{OE}	$\overline{OE}$ Access Time	-	9	-	10	-	12	-	15	
t_{OH}	Output Data Hold Time from Address Change	5	-	5	-	5	-	5	-	
t_{COE}	Output Enable Time from $\overline{CE}$	5	-	5	-	5	-	5	-	
t_{COD}	Output Disable Time from $\overline{CE}$	-	10	-	10	-	10	-	15	
t_{OEE}	Output Enable Time from $\overline{OE}$	0	-	0	-	0	-	0	-	
t_{ODO}	Output Disable Time from $\overline{OE}$	-	8	-	8	-	10	-	15	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	17	-	20	-	25	-	35	

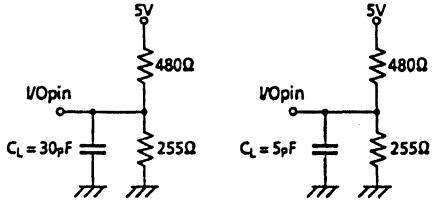
WRITE CYCLE

SYMBOL	PARAMETER	TC55328P/J-17		TC55328P/J-20		TC55328P/J-25		TC55328P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	17	-	20	-	25	-	35	-	ns
t_{CW}	Chip Enable to End of Write	13	-	13	-	15	-	20	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	13	-	13	-	15	-	20	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	0	-	
t_{DS}	Data Set Up Time	10	-	10	-	12	-	15	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	0		
t_{OEW}	Output Enable Time from $\overline{WE}$	0	-	0	-	0	-	0	-	
t_{ODW}	Output Disable Time from $\overline{WE}$	-	8	-	8	-	10	-	15	

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig.1

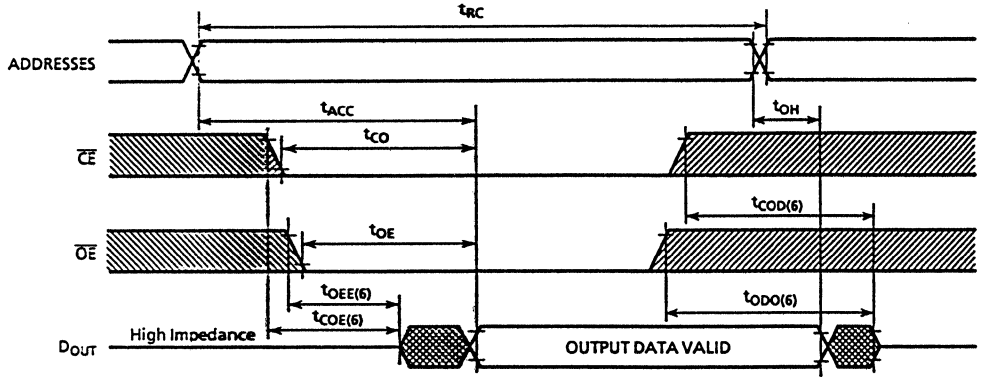
Fig.1



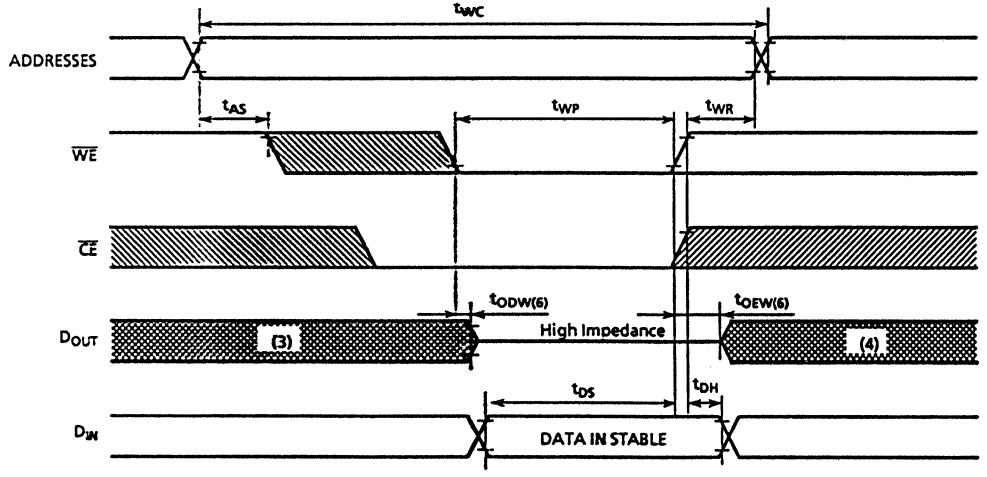
(For t_{COE}, t_{OEE}, t_{COD}, t_{ODO}, t_{OEW} and t_{ODW})

TIMING WAVEFORMS

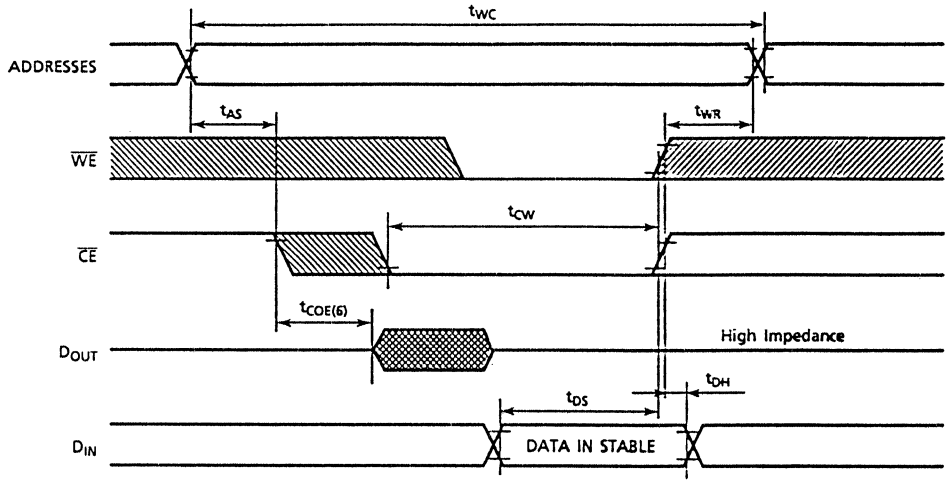
READ CYCLE (2)



WRITE CYCLE1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE2 (5) ($\overline{CE}$ Controlled Write)



NOTE: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

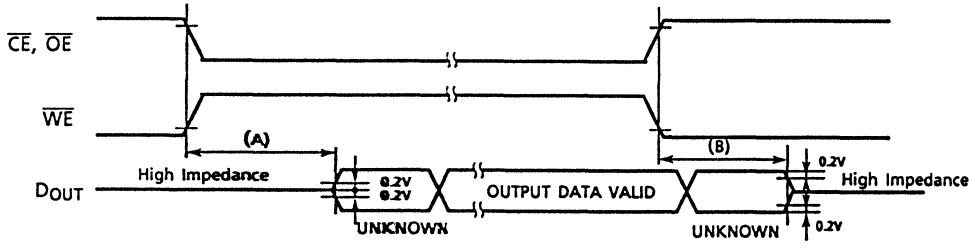
4 Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig.1.

(A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

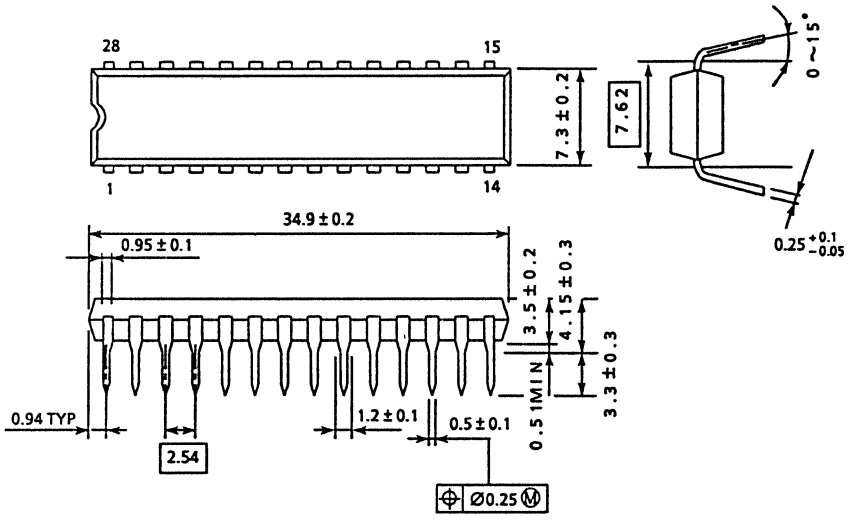
(B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP28-P-300B)

UNIT in mm

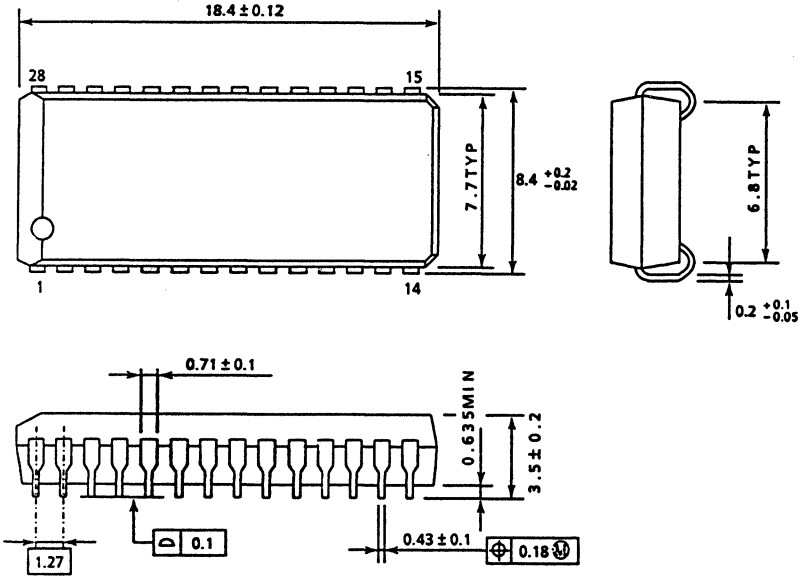


Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

Plastic SOJ (SOJ28 - P - 300)

UNIT in mm



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm

32,768 WORD × 9 BIT CMOS STATIC RAM

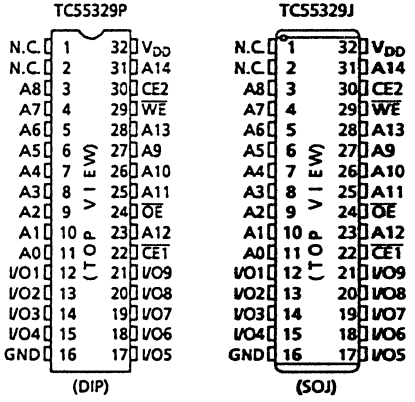
DESCRIPTION

The TC55329P/J is a 294,912 bit high-speed static random access memory organized as 32,768 words by 9 bits using CMOS technology, and operates from a single 5 volt supply. Toshiba's advanced CMOS circuitry provides high-speed characteristics. The TC55329P/J has low stand-by power using Chip Enables ($\overline{CE1}$/CE2), and has fast memory accesses using Output Enable ($\overline{OE}$). The TC55329P/J is suitable for use as cache memory where high speed is required. All inputs and outputs are directly TTL compatable. The TC55329P/J is offered in standard 32 pin 300 mil DIP and SOJ packages for high density assembly.

FEATURES

- Fast access time:
  - TC55329P/J-17 17ns(MAX.)
  - TC55329P/J-20 20ns(MAX.)
  - TC55329P/J-25 25ns(MAX.)
  - TC55329P/J-35 35ns(MAX.)
- Low power dissipation
  - Operation: TC55329P/J-17 140mA(MAX.)
  - TC55329P/J-20 140mA(MAX.)
  - TC55329P/J-25 140mA(MAX.)
  - TC55329P/J-35 120mA(MAX.)
  - Standby : 1mA(MAX.)
- 5V single power supply :
  - −17 : 5V±5%
  - −20/25/35 : 5V±10%
- Fully static operation
- All Inputs and Outputs : TTL compatible
- Output buffer control : $\overline{OE}$
- Package
  - 32 pin plastic 300 mil DIP : TC55329P
  - 32 pin plastic 300 mil SOJ : TC55329J

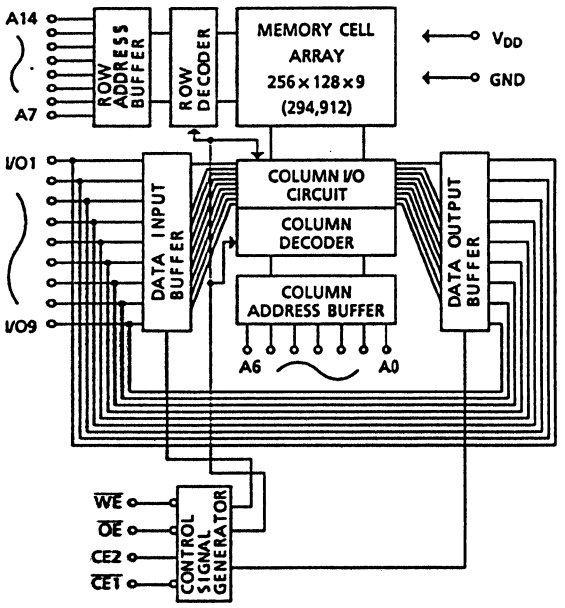
PIN CONNECTION



PIN NAMES

A0~A14	Address Inputs
I/O1~I/O9	Data Inputs/Outputs
$\overline{CE1}$, CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
$V_{I/O}$	Input/Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
T_{solder}	Soldering Temperature · Time	260·10	°C·sec
T_{strg}	Storage Temperature	−65~150	°C
T_{opr}	Operating Temperature	−10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	−17	4.75	5.0	5.25	V
		−20/25/35	4.5	5.0	5.5	
V_{IH}	Input High Voltage		2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage		−0.5 *	−	0.8	V

* −3V Pulse Width : 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, −17 : V_{DD} = 5V ± 5%, −20/25/35 : V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}			−	−	±1	μA
I_{OH}	Output High Current	V_{OH} = 2.4V			−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V			8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 0~V_{DD}			−	−	±1	μA
I_{DDO}	Operating Current	tcycle = Min cycle $\overline{CE1}$ = V_{IL} and CE2 = V_{IH} Other Input = V_{IH}/V_{IL}	V_{DD} = 5.25V	−17	−	−	140	mA
			V_{DD} = 5.5V	−20	−	−	140	
				−25	−	−	140	
				−35	−	−	120	
I_{DDS1}	Standby Current	tcycle = Min cycle $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} Other Input = V_{IH}/V_{IL}	V_{DD} = 5.25V	−17	−	−	20	mA
			V_{DD} = 5.5V	−20				
				−25				
				−35				
I_{DDS2}		$\overline{CE1}$ = V_{DD} − 0.2V or CE2 = 0.2V Other Input = V_{DD} − 0.2V or 0.2V			−	−	1	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	8	pF

Note : This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C (1), -17 : V_{DD} = 5V ± 5%, -20/25/35 : V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55329P/J-17		TC55329P/J-20		TC55329P/J-25		TC55329P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	17	-	20	-	25	-	35	-	ns
t_{ACC}	Address Access Time	-	17	-	20	-	25	-	35	
t_{CO1}	$\overline{CE1}$ Access Time	-	17	-	20	-	25	-	35	
t_{CO2}	CE2 Access Time	-	17	-	20	-	25	-	35	
t_{OE}	$\overline{OE}$ Access Time	-	9	-	10	-	12	-	15	
t_{OH}	Output Data Hold Time from Address Change	5	-	5	-	5	-	5	-	
t_{COE}	Output Enable Time from $\overline{CE1}$ or CE2	5	-	5	-	5	-	5	-	
t_{COD}	Output Disable Time from $\overline{CE1}$ or CE2	-	10	-	10	-	10	-	15	
t_{OEE}	Output Enable Time from $\overline{OE}$	0	-	0	-	0	-	0	-	
t_{ODO}	Output Disable Time from $\overline{OE}$	-	8	-	8	-	10	-	15	
t_{PU}	Chip Selection to Power Up Time	0	-	0	-	0	-	0	-	
t_{PD}	Chip Deselection to Power Down Time	-	17	-	20	-	25	-	35	

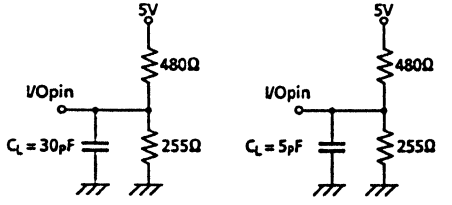
WRITE CYCLE

SYMBOL	PARAMETER	TC55329P/J-17		TC55329P/J-20		TC55329P/J-25		TC55329P/J-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	17	-	20	-	25	-	35	-	ns
t_{CW}	Chip Enable to End of Write	13	-	13	-	15	-	20	-	
t_{AS}	Address Set Up Time	0	-	0	-	0	-	0	-	
t_{WP}	Write Pulse Width	13	-	13	-	15	-	20	-	
t_{WR}	Write Recovery Time	0	-	0	-	0	-	0	-	
t_{DS}	Data Set Up Time	10	-	10	-	12	-	15	-	
t_{DH}	Data Hold Time	0	-	0	-	0	-	0		
t_{OEW}	Output Enable Time from $\overline{WE}$	0	-	0	-	0	-	0	-	
t_{ODW}	Output Disable Time from $\overline{WE}$	-	8	-	8	-	10	-	15	

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	Fig.1

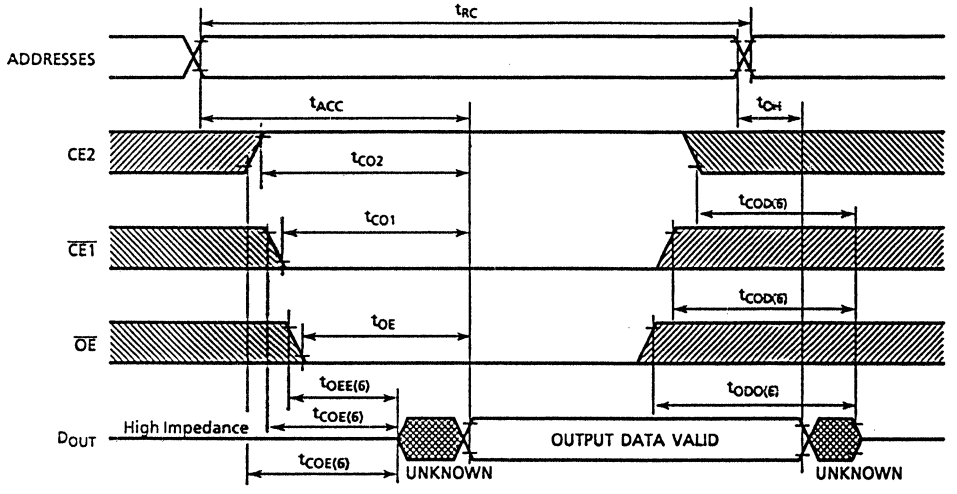
Fig.1



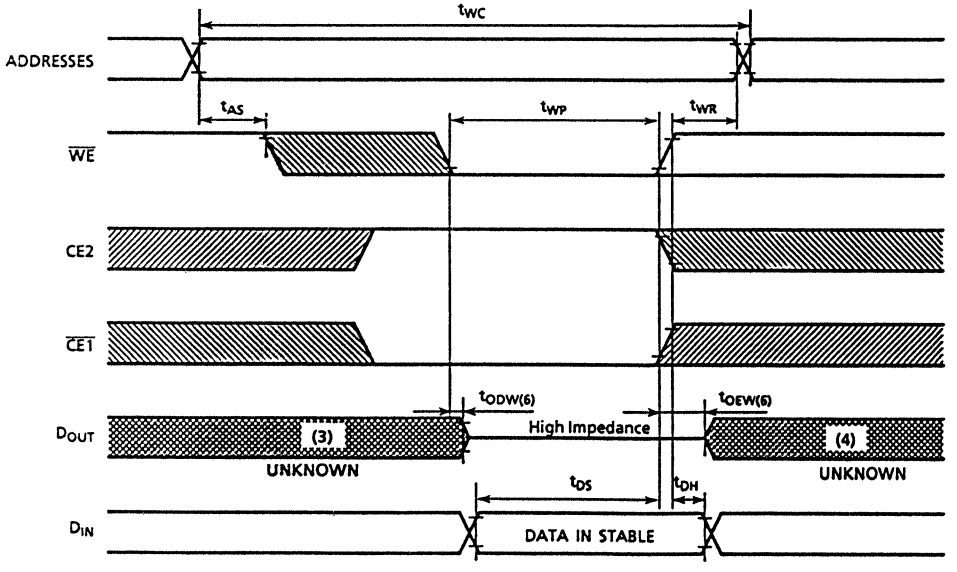
(For t_{COE}, t_{OEE}, t_{COD}, t_{ODO}, t_{OEW} and t_{ODW})

TIMING WAVEFORMS

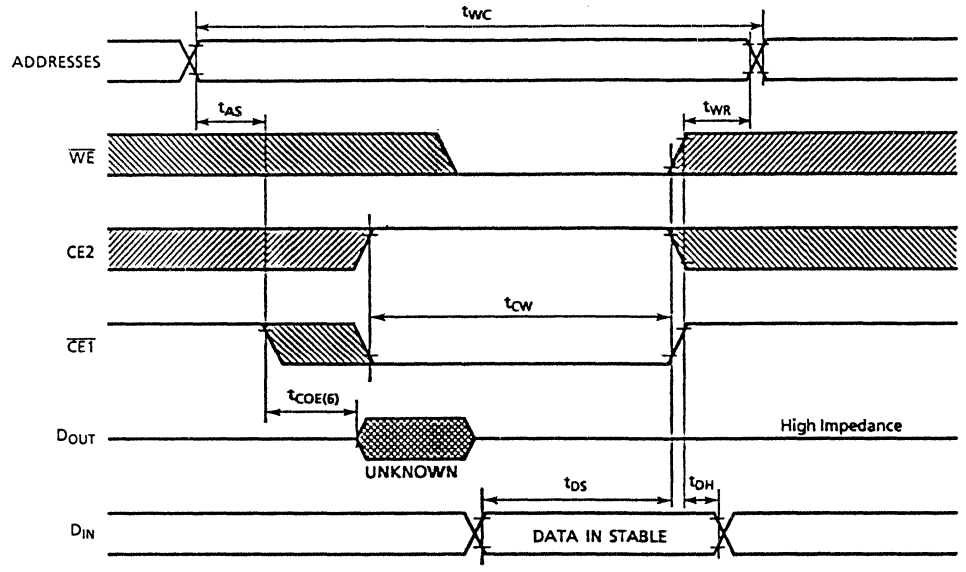
READ CYCLE (2)



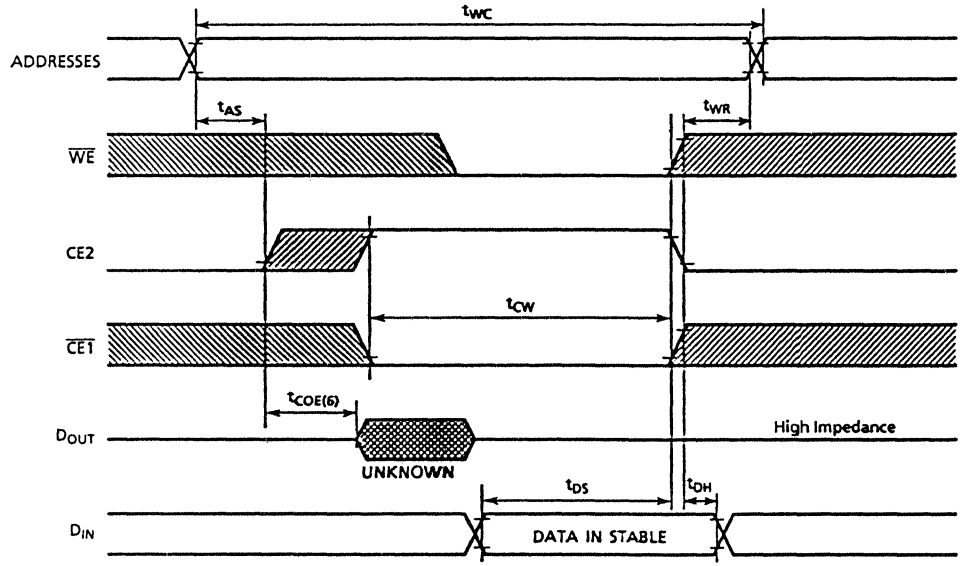
WRITE CYCLE1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE2 (5) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (5) (CE2 Controlled Write)



NOTE: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

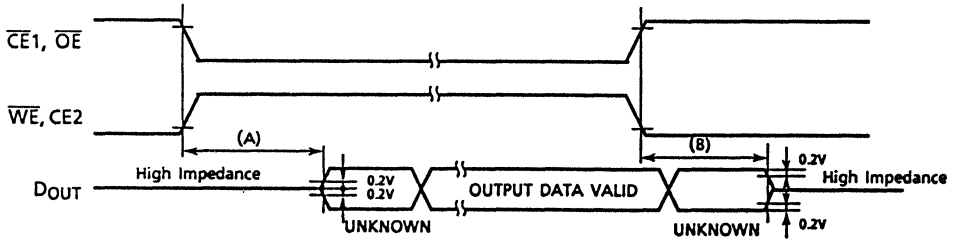
4 Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig.1.

(A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

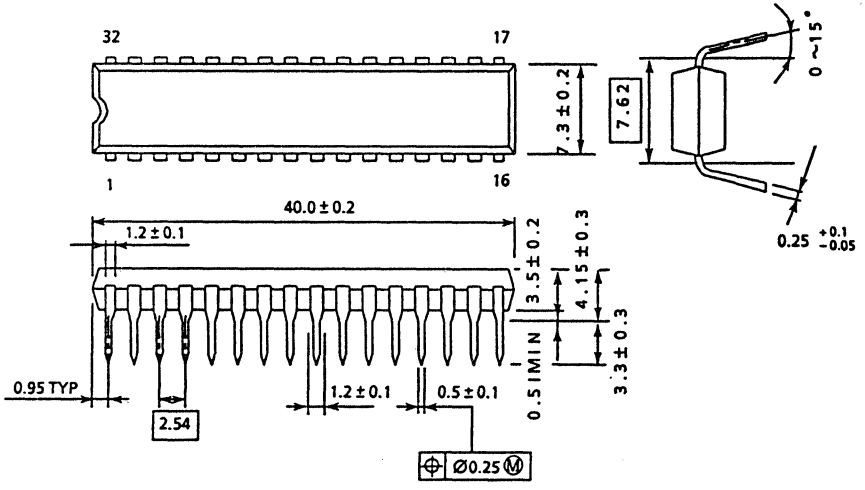
(B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP32-P-300)

UNIT in mm

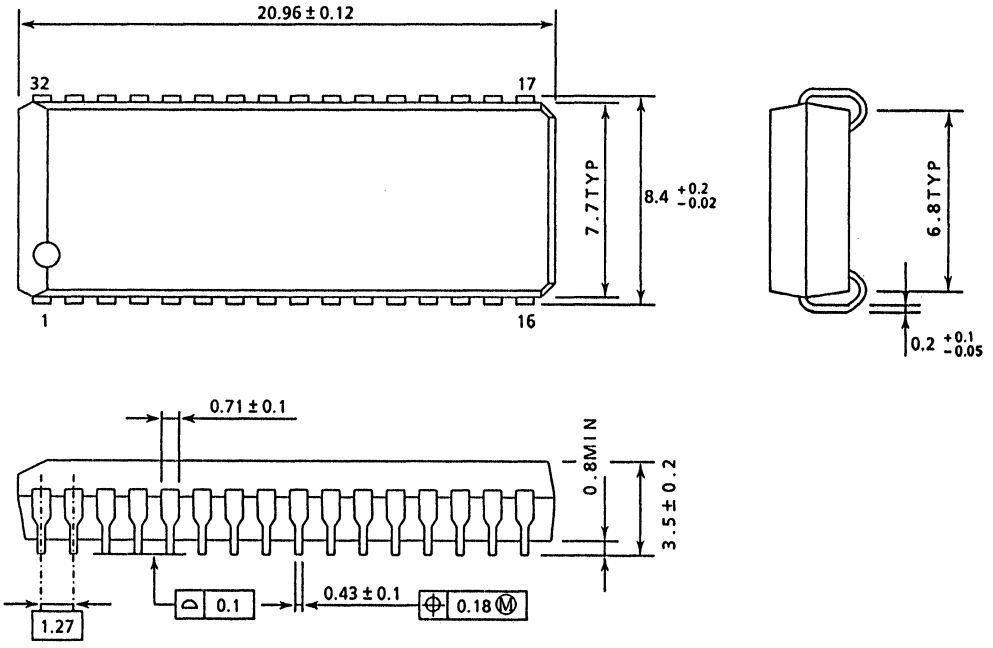


Note: Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

Plastic SOJ (SOJ32 - P - 300)

UNIT in mm



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm

BiCMOS High Speed Static RAM

8,192 WORD × 8 BIT BiCMOS STATIC RAM

PRELIMINARY

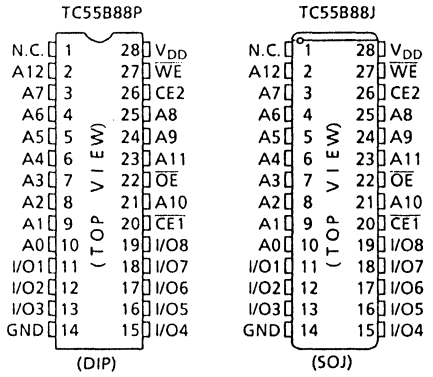
DESCRIPTION

The TC55B88P/J is a 65,536 bit high-speed static random access memory organized as 8,192 words by 8 bits using BiCMOS technology, and operates from a single 5 volt supply. Toshiba's advanced BiCMOS circuitry provides high-speed characteristics. The TC55B88P/J has low stand-by power using Chip Enables ($\overline{CE1}$/CE2), and has fast memory accesses using Output Enable ($\overline{OE}$). The TC55B88P/J is suitable for use as cache memory where high speed is required. All inputs and outputs are directly TTL compatible. The TC55B88P/J is offered in standard 28 pin 300 mil DIP and SOJ packages for high density assembly.

FEATURES

- Fast access time :
  - TC55B88P/J-10 10ns (MAX.)
  - TC55B88P/J-12 12ns (MAX.)
- Low power dissipation :
  - Operation 135mA (MAX.)
  - Standby 10mA (MAX.)
- 5V single power supply : 5V±10%
- Fully static operation
- Directly TTL compatible : All Inputs and Outputs
- Output buffer control : $\overline{OE}$
- Package :
  - 28 Pin plastic 300 mil DIP (TC55B88P)
  - 28 Pin plastic 300 mil SOJ (TC55B88J)

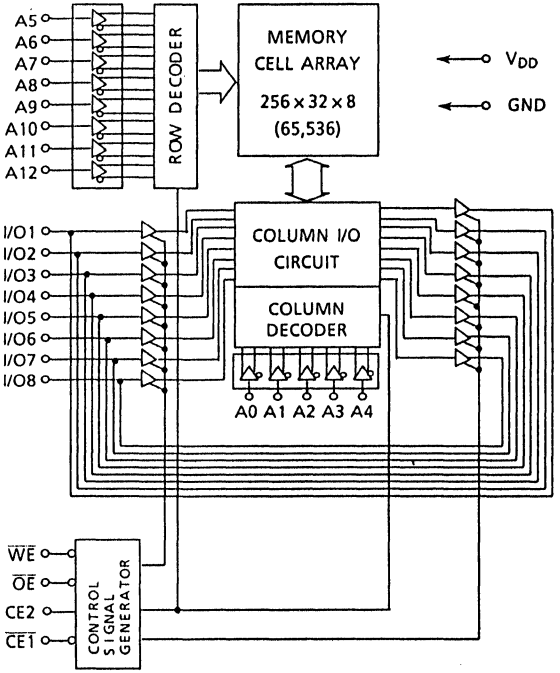
PIN CONNECTION



PIN NAMES

A0~A12	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
$\overline{CE1}$, CE2	Chip Enable Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	1.0	W
Tsolder	Soldering Temperature · Time	260 · 10	°C · sec
Tstrg	Storage Temperature	−65~150	°C
Topr	Operating Temperature	-10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	−0.5 *	−	0.8	V

* −3V Pulse Width : 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	−	−	± 10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0~V_{DD}	−	−	± 10	μA
I_{DDO}	Operating Current	V_{DD} = 5.5V tcycle = Min cycle $\overline{CE1}$ = V_{IL} and CE2 = V_{IH} Other Inputs = V_{IH}/V_{IL} I_{OUT} = 0mA	−	−	135	mA
I_{DDS1}	Standby Current	V_{DD} = 5.5V $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} Other Inputs = V_{IH}/V_{IL}	−	−	30	mA
I_{DDS2}		$\overline{CE1}$ = V_{DD} − 0.2V or CE2 = 0.2V Other Inputs = V_{DD} − 0.2V or 0.2V	−	−	10	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	7	pF

NOTE : This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C [1], V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55B88P/J – 10		TC55B88P/J – 12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	–	12	–	ns
t_{ACC}	Address Access Time	–	10	–	12	
t_{CO1}	$\overline{CE1}$ Access Time	–	10	–	12	
t_{CO2}	CE2 Access Time	–	10	–	12	
t_{OE}	$\overline{OE}$ Access Time	–	6	–	7	
t_{OH}	Output Data Hold Time from Address Change	3	–	3	–	
t_{COE}	Output Enable Time from $\overline{CE1}$ or CE2	3	–	3	–	
t_{COD}	Output Disable Time from $\overline{CE1}$ or CE2	–	5	–	6	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	5	–	6	
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	
t_{PD}	Chip Deselection to Power Down Time	–	10	–	12	

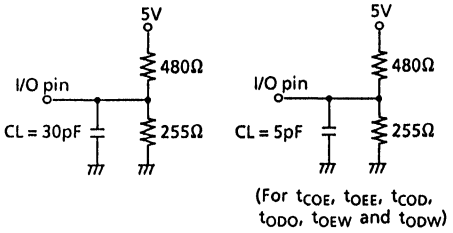
WRITE CYCLE

SYMBOL	PARAMETER	TC55B88P/J – 10		TC55B88P/J – 12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	–	12	–	ns
t_{CW}	Chip Enable to End of Write	7	–	8	–	
t_{AS}	Address Set Up Time	0	–	0	–	
t_{AW}	Address Valid to End of Write	7	–	8	–	
t_{WP}	Write Pulse Width	6	–	7	–	
t_{WR}	Write Recovery Time	1	–	1	–	
t_{DS}	Data Set Up Time	6	–	7	–	
t_{DH}	Data Hold Time	0	–	0	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	5	–	6	

AC TEST CONDITIONS

Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

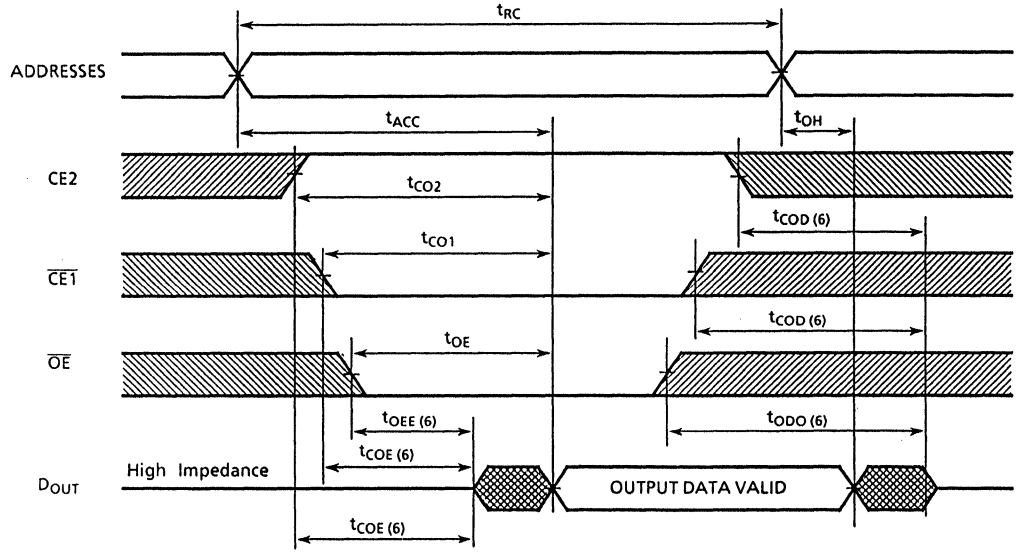
Fig. 1



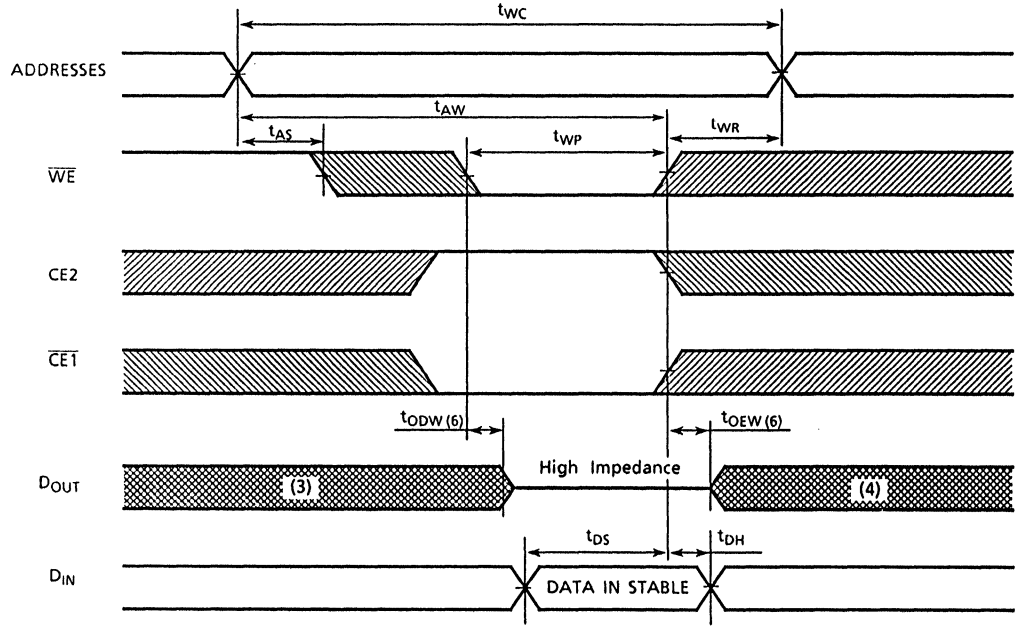
(For t_{COE}, t_{OEE}, t_{COD}, t_{ODO}, t_{OEW} and t_{ODW})

TIMING WAVEFORMS

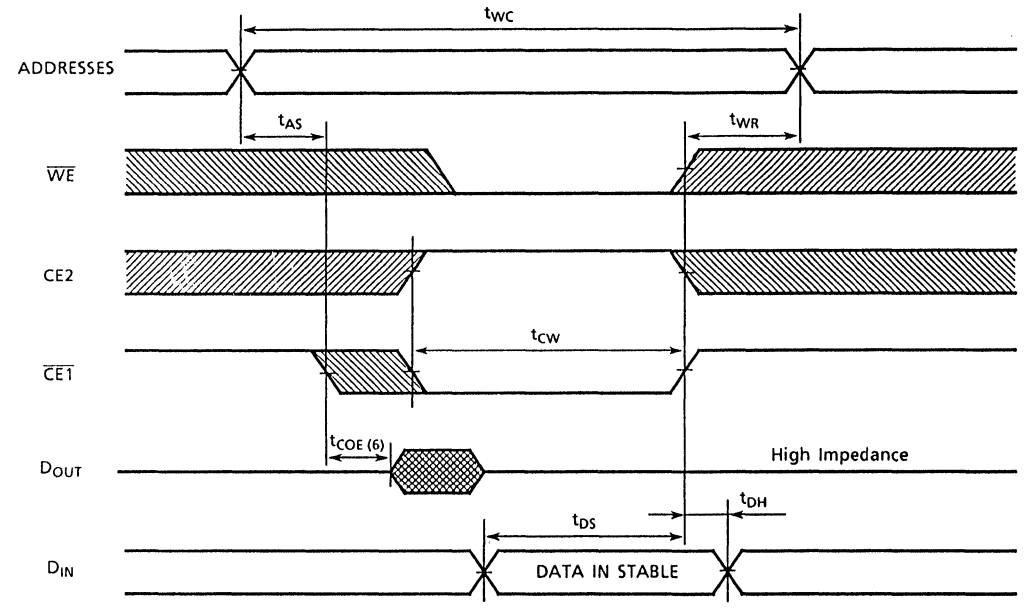
READ CYCLE (2)



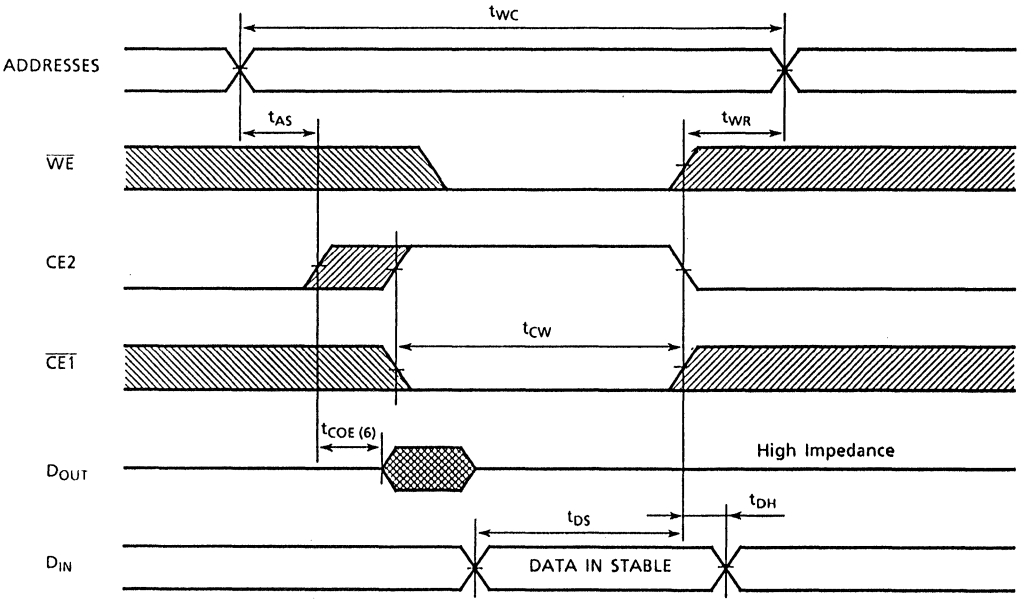
WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (5) ($\overline{CE1}$ Controlled Write)



WRITE CYCLE 3 (5) (CE2 Controlled Write)



NOTES: 1. The operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

2. $\overline{WE}$ is High for Read Cycle.

3. Assuming that $\overline{CE1}$ Low transition or CE2 High transition occurs coincident with or after $\overline{WE}$ Low transition, Outputs remain in a high impedance state.

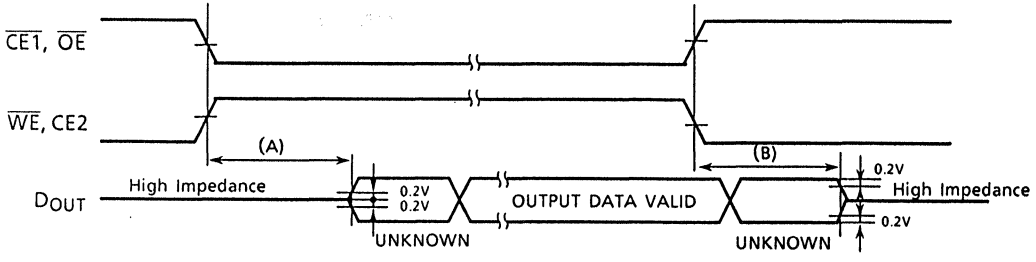
4. Assuming that $\overline{CE1}$ High transition or CE2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition, Outputs remain in a high impedance state.

5. Assuming that $\overline{OE}$ is High for Write Cycle, Outputs are in a high impedance state during this period.

6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

   (A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

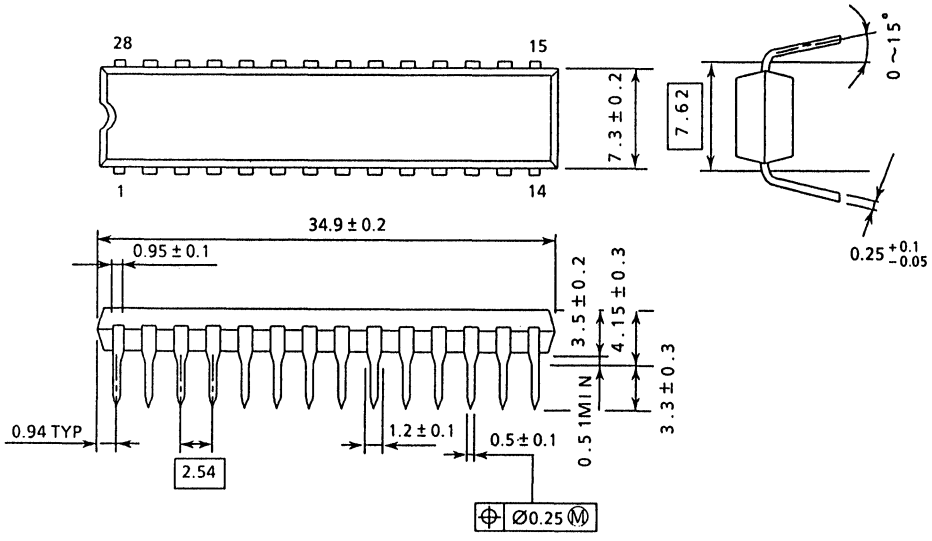
   (B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP28-P-300B)

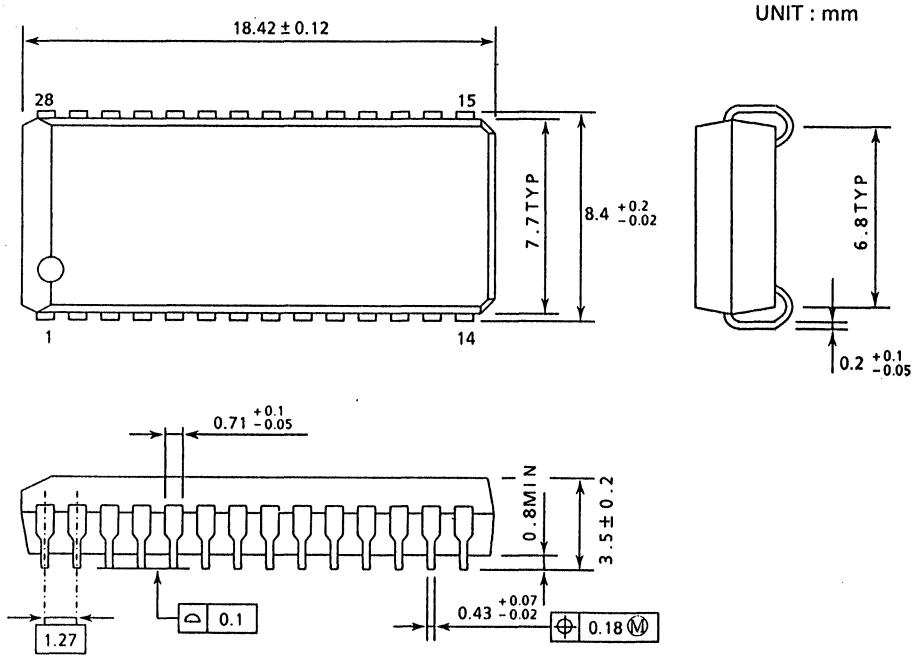
UNIT : mm



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

Plastic SOJ (SOJ28-P-300A)



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

16,384 WORD × 4 BIT BiCMOS STATIC RAM

PRELIMINARY

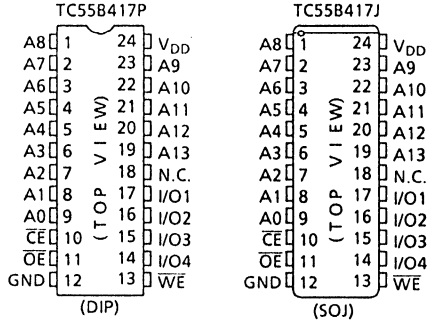
DESCRIPTION

The TC55B417P/J is a 65,536 bit high-speed static random access memory organized as 16,384 words by 4 bits using BiCMOS technology, and operates from a single 5 volt supply. Toshiba's advanced BiCMOS circuitry provides high-speed characteristics. The TC55B417P/J has low stand-by power using Chip Enable ($\overline{CE}$), and has fast memory accesses using Output Enable ($\overline{OE}$). The TC55B417P/J is suitable for use as cache memory where high speed is required. All inputs and outputs are directly TTL compatible. TC55B417P/J is offered in standard 24 pin 300 mil DIP and SOJ packages for high density assembly.

FEATURES

- Fast access time :
  - TC55B417P/J-10 — 10ns (MAX.)
  - TC55B417P/J-12 — 12ns (MAX.)
- Low power dissipation :
  - Operation — 120mA (MAX.)
  - Standby — 10mA (MAX.)
- 5V single power supply : 5V±10%
- Fully static operation
- Directly TTL compatible : All Inputs and Outputs
- Output buffer control : $\overline{OE}$
- Package :
  - 24 Pin plastic 300 mil DIP (TC55B417P)
  - 24 Pin plastic 300 mil SOJ (TC55B417J)

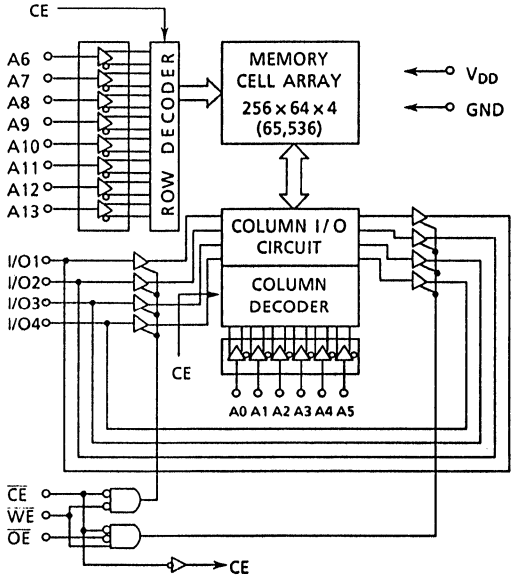
PIN CONNECTION



PIN NAMES

A0 ~ A13	Address Inputs
I/O1 ~ I/O4	Data Inputs / Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+5V)
GND	Ground
N.C.	No Connection

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	−0.5~7.0	V
V_{IN}	Input Voltage	−2.0~7.0	V
V_{OUT}	Output Voltage	−0.5~V_{DD}+0.5	V
P_D	Power Dissipation	850	mW
Tsolder	Soldering Temperature · Time	260 · 10	°C · sec
Tstrg	Storage Temperature	−65~150	°C
Topr	Operating Temperature	−10~85	°C

DC RECOMMENDED OPERATING CONDITIONS (Ta = 0~70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	V_{DD}+0.5	V
V_{IL}	Input Low Voltage	−0.5*	−	0.8	V

* −3V Pulse Width : 10ns

DC and OPERATING CHARACTERISTICS (Ta = 0~70°C, V_{DD} = 5V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0~V_{DD}	−	−	± 10	μA
I_{OH}	Output High Current	V_{OH} = 2.4V	−4	−	−	mA
I_{OL}	Output Low Current	V_{OL} = 0.4V	8	−	−	mA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0~V_{DD}	−	−	± 10	μA
I_{DDO}	Operating Current	V_{DD} = 5.5V, tcycle = Min cycle, $\overline{CE}$ = V_{IL} Iout = 0mA, Other Inputs = V_{IH} / V_{IL}	−	−	120	mA
I_{DDS1}	Standby Current	V_{DD} = 5.5V, $\overline{CE}$ = V_{IH} Other Inputs = V_{IH} / V_{IL}	−	−	30	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} − 0.2V Other Inputs = V_{DD} − 0.2V or 0.2V	−	−	10	

CAPACITANCE (Ta = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	7	pF

Note : This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS (Ta = 0~70°C [4], V_{DD} = 5V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC55B417P/J-10		TC55B417P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	10	–	12	–	ns
t_{ACC}	Address Access Time	–	10	–	12	
t_{CO}	Chip Enable Access Time	–	10	–	12	
t_{OE}	Output Enable Access Time	–	6	–	7	
t_{COE}	Output Enable Time from $\overline{CE}$	3	–	3	–	
t_{COD}	Output Disable Time from $\overline{CE}$	–	5	–	6	
t_{OEE}	Output Enable Time from $\overline{OE}$	1	–	1	–	
t_{ODO}	Output Disable Time from $\overline{OE}$	–	5	–	6	
t_{OH}	Output Data Hold Time from Address Change	3	–	3	–	
t_{PU}	Chip Selection to Power Up Time	0	–	0	–	
t_{PD}	Chip Deselection to Power Down Time	–	10	–	12	

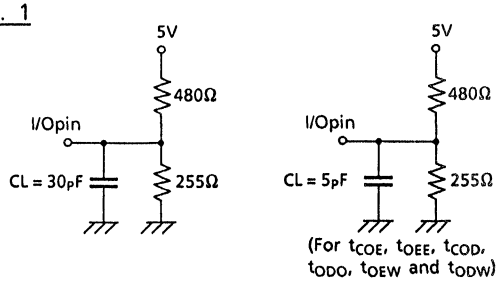
WRITE CYCLE

SYMBOL	PARAMETER	TC55B417P/J-10		TC55B417P/J-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	10	–	12	–	ns
t_{WP}	Write Pulse Width	6	–	7	–	
t_{AW}	Address Valid to End of Write	7	–	8	–	
t_{CW}	Chip Enable to End of Write	7	–	8	–	
t_{AS}	Address Set Up Time	0	–	0	–	
t_{WR}	Write Recovery Time	1	–	1	–	
t_{OEW}	Output Enable Time from $\overline{WE}$	1	–	1	–	
t_{ODW}	Output Disable Time from $\overline{WE}$	–	5	–	6	
t_{DS}	Data Set Up Time	6	–	7	–	
t_{DH}	Data Hold Time	0	–	0	–	

AC TEST CONDITIONS

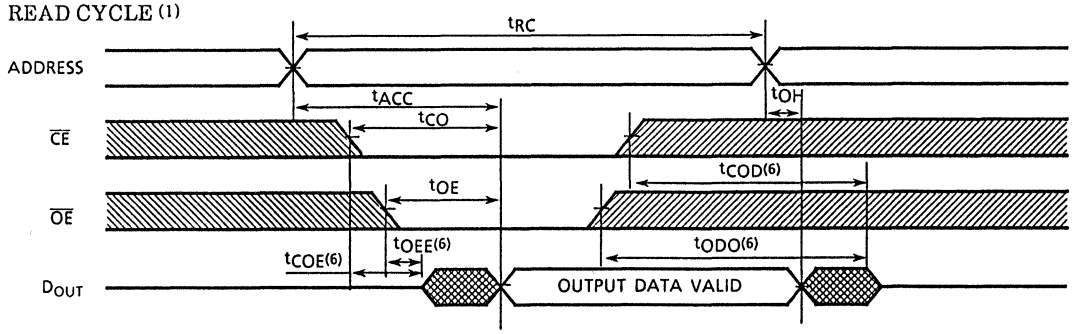
Input Pulse Levels	3.0V/0.0V
Input Pulse Rise and Fall Time	3ns
Input Timing Measurement Reference Levels	1.5V
Output Timing Measurement Reference Levels	1.5V
Output Load	Fig. 1

Fig. 1

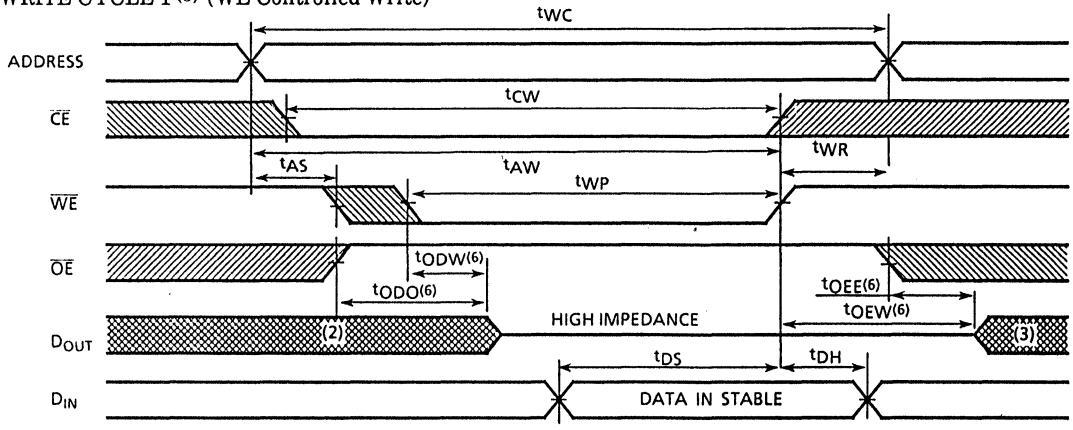


TIMING WAVEFORMS

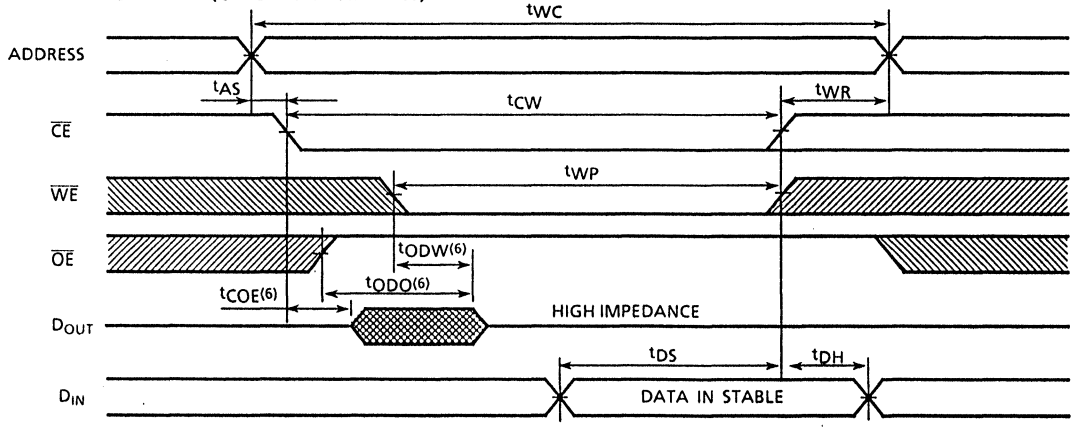
READ CYCLE (1)



WRITE CYCLE 1 (5) ($\overline{WE}$ Controlled Write)



WRITE CYCLE 2 (5) ($\overline{CE}$ Controlled Write)



Note : 1. $\overline{WE}$ is High for Read Cycle.

2. Assuming that $\overline{CE}$ Low transition occurs coincident with or after $\overline{WE}$ Low transition, outputs remain in a high impedance state.

3. Assuming that $\overline{CE}$ High transition occurs coincident with or prior to $\overline{WE}$ High transition, outputs remain in a high impedance state.

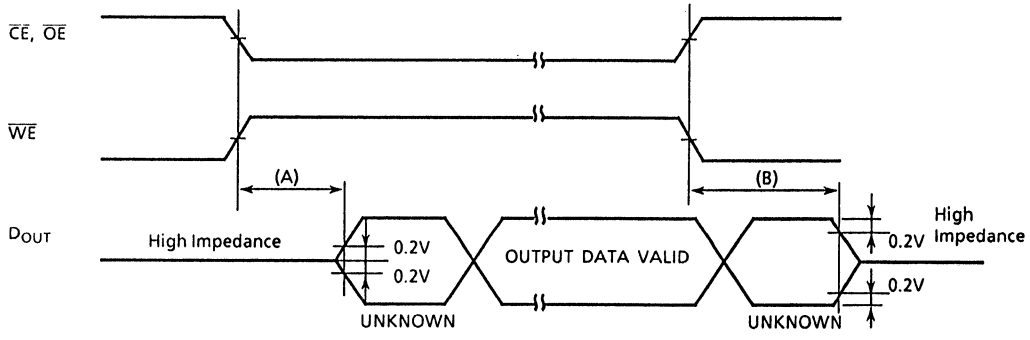
4. The Operating temperature (Ta) is guaranteed with transverse air flow exceeding 400 linear feet per minute.

5. The $\overline{OE}$ input can be held on low (V_{IL}) in write cycle.

6. These parameters are specified as follows and measured by using the load shown in Fig. 1.

(A) t_{COE}, t_{OEE}, t_{OEW} ..... Output Enable Time

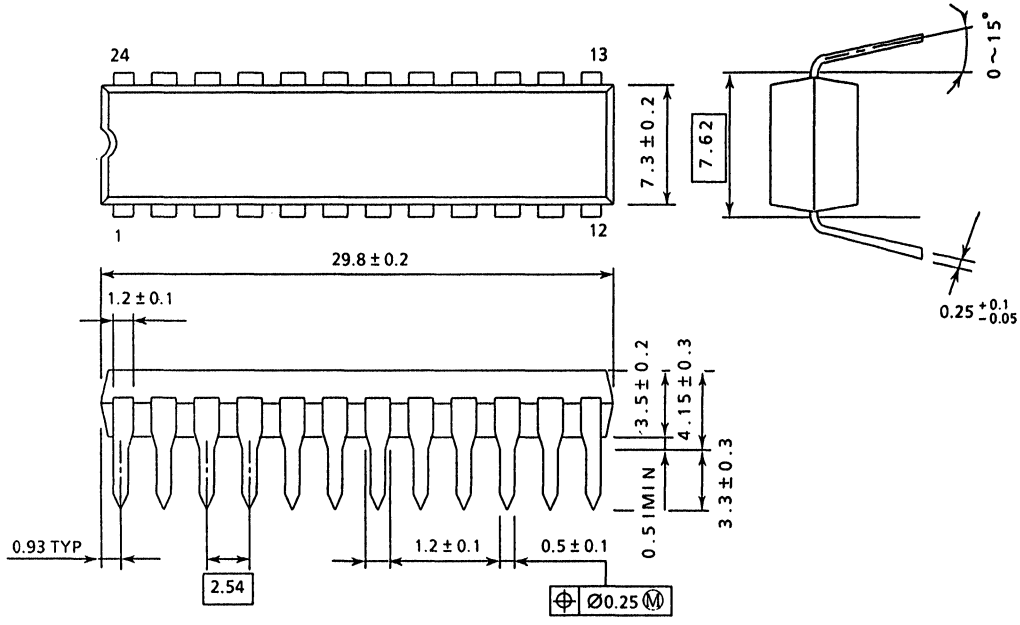
(B) t_{COD}, t_{ODO}, t_{ODW} ..... Output Disable Time



OUTLINE DRAWINGS

Plastic DIP (DIP24-P-300B)

Unit : mm

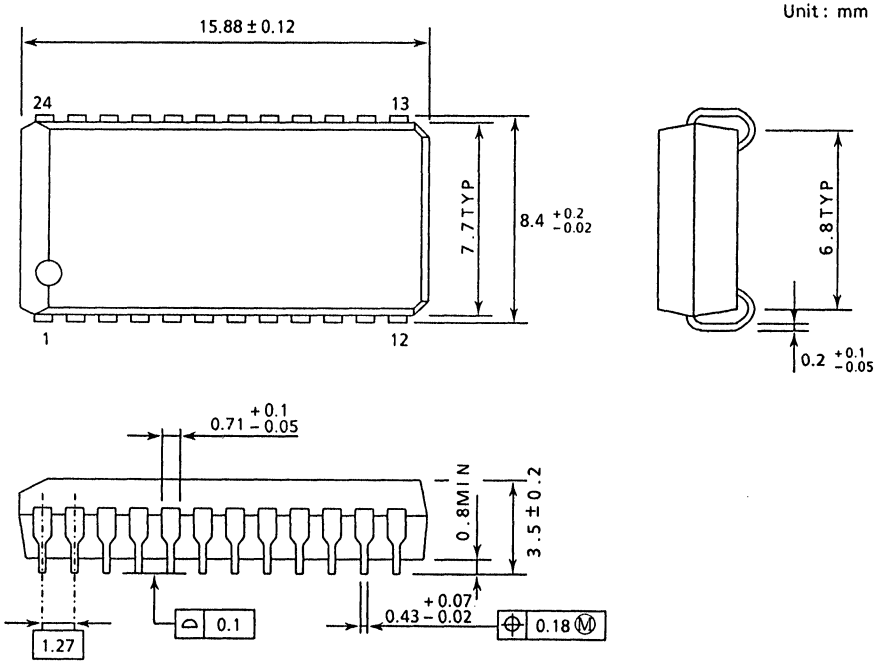


Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

OUTLINE DRAWINGS

Plastic SOJ (SOJ24-P-300A)

Unit : mm



Note : Package width and length do not include mold protrusion, allowable mold protrusion is 0.15mm.

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