TUNGSRAM

INTEGRATED CIRCUITS '80

BIPOLAR MEMORIES

NUMERICAL INDEX OF DEVICES

CROSS REFERENCE TABLE

TUNGSRAM	INTEL	INTERSIL	FAIRCHILD	MMI	NATIONAL	SIGNETICS	TEXAS
TM101PC	3101	IM 5501	93404	6560	DM 7489	8225	SN 7489
TM106PC	3106	IM 5523	93421	6531	DM 74200	82S16	SN 74S201
TM107PC	3107	IM 5533	93411	6530	DM 74S206	82S17	SN 74S301
TM188PC	–	IM 5600	–	6330-1	DM 74S188	82S23	SN 74S188[1]
TM601PC	3601	IM 5603	93417	6300-1	DM 8573	82S126	SN 74S387
TM621PC	3621	IM 5623	93427	6301-1	DM 8574	82S129	SN 74S287
TM622PC	3622	IM 5624	93446	6306-1	DM 74S571	82S131	SN 74S471[1]
TM624PC	3624	IM 5625	93448	6341-1	DM 87S296	82S141	SN 74S472[1]

[1] Functional replacement.

INTRODUCTION

TUNGSRAM Bipolar Memories are available in plastic dual-in-line packages for commercial and industrial applications.

TYPE DESIGNATION

The letters following the type designation consisting of five characters, are:
P refers to plastic packaging,
C indicates the operational temperature range (0 to +70 °C).

DEFINITION OF SYMBOLS

Voltages

V_{CC}	Supply Voltage
V_{CCP}	V_{CC} Required During Programming
V_I	Input Voltage
V_{IC}	Input Clamp Voltage
V_{IH}	HIGH Level Input Voltage
V_{IL}	LOW Level Input Voltage
V_O	Output Voltage (DC)
V_{OH}	HIGH Level Output Voltage
V_{OL}	LOW Level Output Voltage
V_{OUT}	Output Voltage
V_{OUTP}	Required Programming Voltage on Output Pin
V_{PP}	Required Programming Voltage on Program Pin

Currents

I_{CC}	Power Supply Current
I_{CEX}	Output Leakage Current
I_{HZ}	HIGH Level OFF State Output Current
I_I	Input Current
I_{IH}	HIGH Level Input Current
I_{IL}	LOW Level Input Current
I_{LP}	Required Current Limit of Power Supply Feeding Program Pin and Output During Programming
I_{LZ}	LOW Level OFF State Output Current
I_{OH}	HIGH Level Output Current
I_{OL}	LOW Level Output Current
I_{OLV1}	Output Current Required During Verification
I_{OLV2}	Output Current Required During Verification
I_{OS}	Output Short Circuit Current

Temperature

T_A	Ambient Temperature

AC Switching and Programming Parameters

f	Frequency
MDC (t_P/t_C)	Maximum Duty Cycle During Automatic Programming of Program Pin and Output Pin
t_{AA}	Address Access Time
t_C	Cycle Time
t_{DW}	Time Input Data Appears at Output Following a Write Command
t_{DWO}	Data In and Write Enable Overlap Time
t_{D1}	Required Time Delay between Disabling Memory Output and Application of Output Programming Pulse
t_{D2}	Required Time Delay between Removal of Programming Pulse and Enabling Memory Output
t_{EA}	Enable Access Time
t_{ER}	Enable Recovery Time
t_{OFF}	Chip Enable to HIGH Impedance Delay
t_{ON}	Chip Enable to LOW Impedance Delay
t_P	Program Pulse Width
t_R	Rise Time Rate of Program Pulse Applied to the Data Out or Program Pin
t_{WH}	Write Enable to Output HIGH Time
t_{WHA}	Address to Write Enable Hold Time
t_{WHCH}	Chip Enable to Write Enable Hold Time
t_{WO}	Data In and Write Enable Overlap Time
t_{WP}	Write Pulse Width
t_{WSA}	Address to Write Enable Setup Time
t_{WSCS}	Chip Enable to Write Enable Setup Time

Capacitances

C_I	Input Capacitance
C_O	Output Capacitance

DATA SHEET CONSTRUCTION

Data sheet construction is generally presented in the following sequence:

- Device Description
- Package Outline
- Connection Diagram
- Schematic Diagram
- Truth Table
- Absolute Maximum Ratings
- DC Characteristics
- AC Characteristics
- Definition of Waveforms
- Programming Instructions
- Programming Speed
- Programming Parameters

If necessary, circuit description and examples are provided.

DEVICE DESCRIPTION

It includes type number, technology used, shortform information on the typical applications and special features.

ABSOLUTE MAXIMUM RATINGS

These values are absolute maximum ratings, which under no operational and environmental conditions should be exceeded, irrespective of allowable maximum or minimum values. If any one of the ratings is exceeded, this could result in irreversible changes in the ratings. Generally the absolute maximum ratings are given under specified conditions and are valid only for these conditions.
Unless otherwise specified an ambient temperature of 25 °C is assumed for all absolute maximum ratings. These ratings are static characteristics, if they are measured by a pulse method then the associated measurement conditions are stated.

DC, AC CHARACTERISTICS AND DEFINITION OF WAVEFORMS

Under these headings are grouped the most important electrical characteristics (minimum, typical and maximum values) together with associated test conditions, waveforms and standard test loads.

PROGRAMMING INSTRUCTIONS

This paragraph contains the state of devices before programming, the procedure of programming with conditions to be kept and the way of verification considering output loads to guarantee the correct operation at extreme temperature ranges.

PROGRAMMING SPEED

The given pulse and voltage sequences have been found to maximize reliability, programming yield and thruput. Programming timing is given as well.

PROGRAMMING PARAMETERS

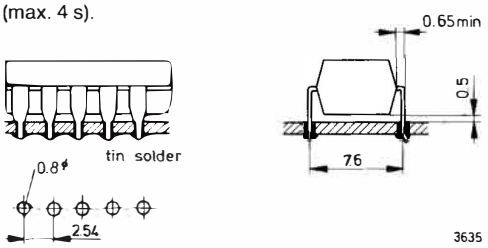
This table contains parameters required to program devices (minimum, typical and maximum values).

SOLDERING INSTRUCTIONS

The integrated circuits must be protected against overheating due to soldering. If necessary, adequate measures must be taken for sufficient heat transfer.

PLASTIC PLUG-IN PACKAGE

Plastic packages are soldered on the side of the printed circuit board opposite to the case, the pins are vertically bent and fit into holes at an equal distance of 7.6 × 2.54 mm and a diameter of .7 to .9 mm.
The distance between the package and the printed circuit board is determined by shoulders (see picture).
After inserting the package into the printed circuit board two or more pins should be bent at an angle of app. 30°. Thus the package need not be held down while soldering.
The maximum allowable solder temperature for iron soldering amounts to 260 °C (max. 10 s) and for dip soldering 245° C (max. 4 s).



QUALITY LEVEL

for types with letter C after Type Designation Code:

DEFECT	AQL, %
functional operating at 25 °C*	0.25
DC characteristics at 25 °C	1
DC characteristics at high temperatures (at +70 °C)	2.5
DC characteristics at low temperatures (at 0 °C)	2.5
AC characteristics at 25 °C	1.5

*Except the PROM-Programmability.

SAMPLING INSPECTION PLAN

PROMs are designed and tested to give a programming yield greater than 95%.

List of symbols:
AQL — Acceptable Quality Level
N — Lot size
n — Sample size
c — Acceptance number (acceptable number of defective items in a sample)
AOQL — Maximum of Average Outgoing Quality Level

Single sampling plan for testing:

NORMAL INSPECTION	AQL						REDUCED INSPECTION
	0.25	0.40	0.65	1.0	1.5	2.5	
N	n–c (AOQL in %)						N
2–15	50–0 (0.71)	32–0 (1.1)	20–0 (1.7)	13–0 (2.6)	8–0 (3.9)	5–0 (6.7)	2–15
16–50							16–150
51–150					32–1 (2.3)	20–1 (3.6)	151–280
151–280				50–1 (1.5)		32–2 (3.8)	281–500
281–500			80–1 (1.0)		50–2 (2.4)	50–3 (3.5)	501–1200
501–1200		125–1 (0.64)		80–2 (1.6)	80–3 (2.2)	80–5 (3.7)	1201–3200
1201–3200	200–1 (0.41)		125–2 (1.1)	125–3 (1.5)	125–5 (2.4)	125–7 (3.5)	3201–10000
3201–10000		200–2 (0.68)	200–3 (0.95)	200–5 (1.6)	200–7 (2.2)	200–10 (3.2)	10001–35000*
10001–35000*	315–2 (0.44)	315–3 (0.61)	315–5 (0.99)	315–7 (1.4)	315–10 (2.1)	315–14 (3.0)	

* Lot size above 35000 pcs must be divided.

RELIABILITY TEST

The following tests are performed on ICs by sample basis:

1. Mechanical Tests
1.1. Physical Dimensions
1.2. External Visual
1.3. Lead Fatigue Test
1.4. Solderability Test
1.5. Constant Acceleration
2. Environmental Tests
2.1. Climatic Tests
2.1.1. Biased Humidity Operating Life 85 °C and 85% Humidity
2.1.2. Steam Pressure
2.1.3. Marking Durability Test
2.2. Temperature Tests
2.2.1. Temperature Cycle
2.2.2. Thermal Shock
3. Life Tests
3.1. Operating Life
3.2. High Temperature Storage Life

MARKING OF CIRCUITS

Circuits are marked as follows:
— first line: Type Designation Code;
— second line: letter T (indicating device made by TUNGSRAM), followed by a Manufacturing Code.

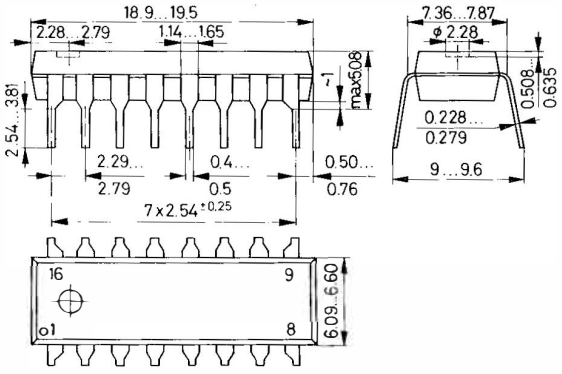
E. g.: TM101PC
T 7927

16×4-BIT FULLY DECODED RANDOM ACCESS MEMORY

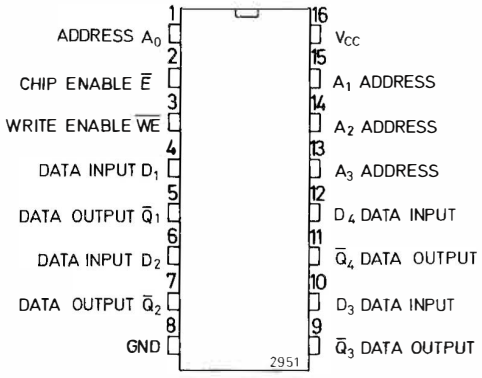
- **Open Collector Outputs**
- **50 ns Max. Access Time**
- **Advanced Schottky Processing**
- **Low Input Current (250 μA Max.)**
- **Single Layer Metal for Reliability**
- **Fully Decoded with One Chip Enable**

DESCRIPTION – The TM101PC is a high speed 64-bit Random Access Memory with full decoding on chip. It is organized as a 16 word by four bits and is designed for scratchpad, buffer and distributed main memory applications. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. An uncommitted collector output is provided to permit "OR-ties" for ease of memory expansion.

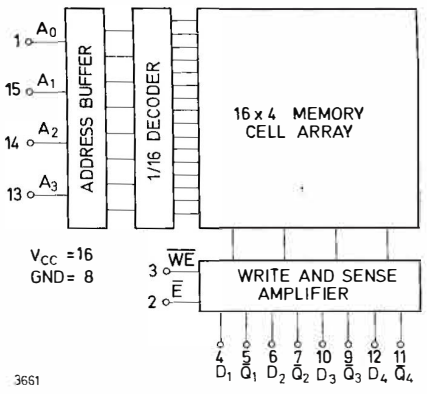
PACKAGE OUTLINE
(P) 9B 16-Lead Molded Dual In-line



CONNECTION DIAGRAM
(TOP VIEW)



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.5 V to 7.0 V
Input Voltage	−0.5 V to 5.5 V
Input Current	−25 mA to 5.0 mA
Output Current	100 mA
Storage Temperature	−65 °C to +150 °C
Ambient Temperature	0 °C to + 70 °C

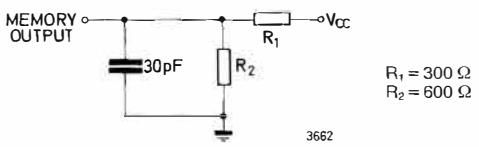
DC CHARACTERISTICS (Guaranteed over the Following Ranges: $V_{CC} = +5.0\ V \pm 5\%$, $T_A = 0\ °C$ to $+70\ °C$)

SYMBOL	PARAMETER	V_{CC}	OTHER CONDITIONS		MIN.	TYP.	MAX.	UNITS
V_{IL}	LOW Level Input Voltage						0.8	V
V_{IH}	HIGH Level Input Voltage				2.0			V
V_{IC}	Input Clamp Voltage	MIN.	$I_I = -5.0\ mA$				−1.0	V
I_{IL}	LOW Level Input Current	MAX.	$V_I = 0.45\ V$				−250	µA
I_{IH}	HIGH Level Input Current	MAX.	$V_I = 2.4\ V$				40	µA
I_I	Max. Level Input Current	MAX.	$V_I = 5.5\ V$				1.0	mA
I_{CC}	Power Supply Current	MAX.					105	mA
C_I	Input Capacitance	5.0 V	$V_I = 2.0\ V$	$T_A = 25\ °C$,		7.0		pF
C_O	Output Capacitance	5.0 V	$V_O = 2.0\ V$	$f = 1\ MHz$		8.0		pF
I_{CEX}	Output Leakage Current	MAX.	$V_O = 2.4\ V$				100	µA
V_{OL}	LOW Level Output Voltage	MIN.	$I_{OL} = 15\ mA$				0.5	V

AC CHARACTERISTICS (with Standard Test Load) $V_{CC} = +5.0\ V$, $T_A = 25\ °C$

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
t_{AA}	Address Access Time	10	50	ns
t_{EA}	Enable Access Time	5	35	ns
t_{ER}	Enable Recovery Time	5	35	ns
t_{WP}	Write Pulse Width	35		ns
t_{WH}	Write Enable to Output HIGH Time		35	ns
t_{DWO}	Data In and Write Enable Overlap Time	25		ns
t_{WSA}	Address to Write Enable Setup Time	0		ns
t_{WHA}	Address to Write Enable Hold Time	0		ns
t_{WSCS}	Chip Enable to Write Enable Setup Time	10		ns
t_{WHCH}	Chip Enable to Write Enable Hold Time	0		ns

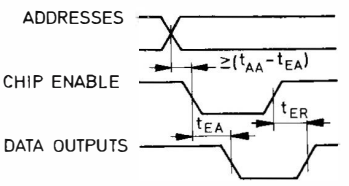
STANDARD TEST LOAD



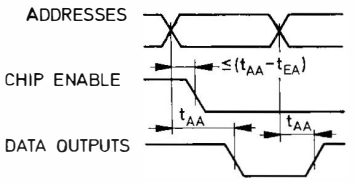
$R_1 = 300\ \Omega$
$R_2 = 600\ \Omega$

DEFINITION OF WAVEFORMS

READ CYCLE

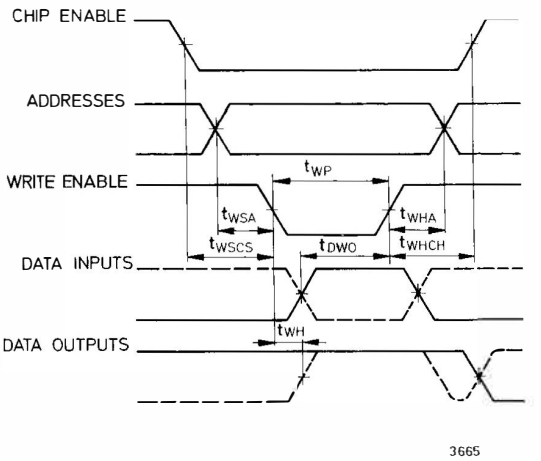


Chip Enable to Output Delay



Address to Output Delay

WRITE CYCLE



Input Pulse Amplitude 3.0 V
Input Rise and Fall Times
5 ns from 1.0 V to 2.0 V
Measurements Made at 1.5 V

TRUTH TABLE

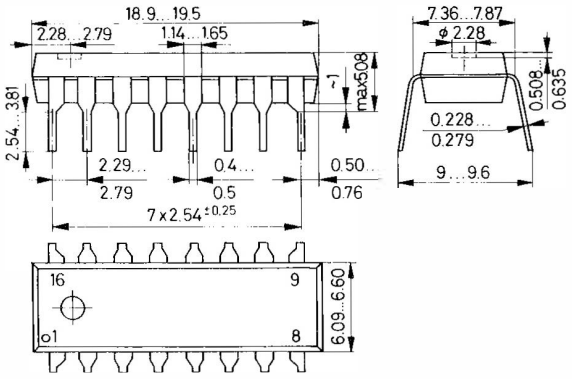
CHIP ENABLE	WRITE ENABLE	OPERATION	DATA OUTPUTS
LOW	LOW	Write	Off
LOW	HIGH	Read	Complement of Written Data
HIGH	Don't Care (HIGH or LOW)	Hold	Off

256×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

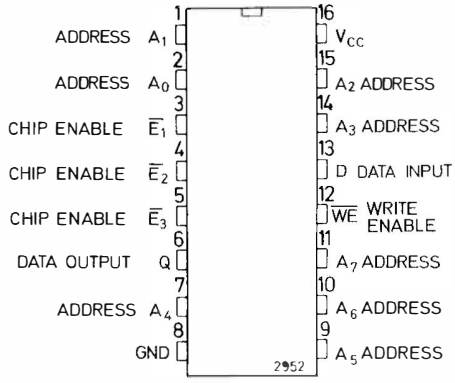
- **3-State Output**
- **55 ns Max. Access Time**
- **Advanced Schottky Processing**
- **Low Input Current (250 μA Max.)**
- **Single Layer Metal for Reliability**
- **The Data Stored is on the Data Out Pin During A Write Cycle**
- **Fully Decoded with 3 Chip Enables**

DESCRIPTION – The TM106PC is a high speed 256-bit Random Access Memory with full decoding on chip. It is organized 256 words by one bit and is designed for scratchpad, buffer and distributed main memory applications. The device has three chip enable lines to simplify their use in larger memory systems. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. A 3-state output is provided to drive bus organized system and/or highly capacitive loads.

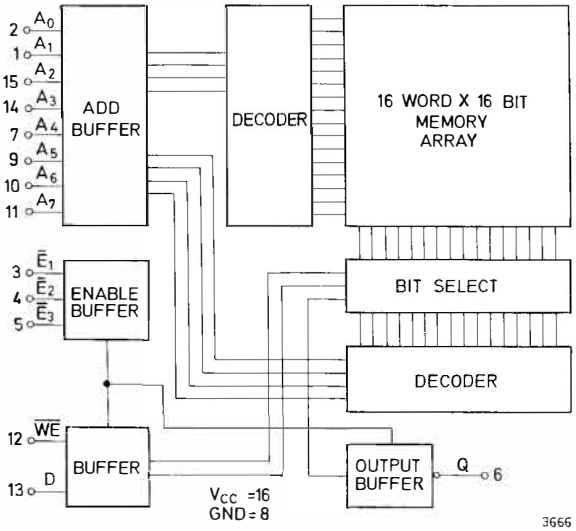
PACKAGE OUTLINE
(P) 9B 16-Lead Molded Dual In-line



CONNECTION DIAGRAM
(TOP VIEW)



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0.5 V to 7.0 V
Input Voltage	–0.5 V to 5.5 V
Input Current	–25 mA to 5.0 mA
Output Current	100 mA
Storage Temperature	–65 °C to +150 °C
Ambient Temperature	0 °C to + 70 °C

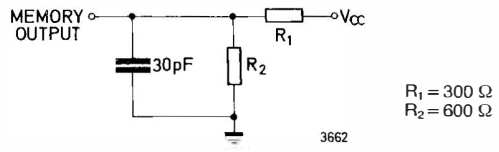
DC CHARACTERISTICS (Guaranteed over the Following Ranges: $V_{CC} = +5.0\ V \pm 5\%$, $T_A = 0\ °C$ to $+70\ °C$)

SYMBOL	PARAMETER	V_{CC}	OTHER CONDITIONS		MIN.	TYP.	MAX.	UNITS
V_{IL}	LOW Level Input Voltage						0.8	V
V_{IH}	HIGH Level Input Voltage				2.0			V
V_{IC}	Input Clamp Voltage	MIN.	$I_I = -5.0$ mA				−1.0	V
I_{IL}	LOW Level Input Current	MAX.	$V_I = 0.45$ V				−250	µA
I_{IH}	HIGH Level Input Current	MAX.	$V_I = 2.4$ V				40	µA
I_I	Max. Level Input Current	MAX.	$V_I = 5.5$ V				1.0	mA
I_{CC}	Power Supply Current	MAX.					130	mA
C_I	Input Capacitance	5.0 V	$V_I = 2.0$ V	$T_A = 25\ °C$,		7.0		pF
C_O	Output Capacitance	5.0 V	$V_O = 2.0$ V	$f = 1$ MHz		8.0		pF
I_{LZ}	LOW Level OFF State Output Current	MAX.	$V_O = 0.5$ V				−100	µA
I_{HZ}	HIGH Level OFF State Output Current	MAX.	$V_O = 2.4$ V				100	µA
I_{OS}	Output Short Circuit Current	5.0 V	$V_O = 0$ V		−20	−50	−90	mA
V_{OH}	HIGH Level Output Voltage	MIN.	$I_{OH} = -3.2$ mA		2.4			V
V_{OL}	LOW Level Output Voltage	MIN.	$I_{OL} = 15$ mA				0.5	V

AC CHARACTERISTICS (with Standard Test Load) $V_{CC} = +5.0$ V, $T_A = 25\ °C$

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
t_{AA}	Address Access Time	20	55	ns
t_{EA}	Enable Access Time	5	35	ns
t_{ER}	Enable Recovery Time	5	35	ns
t_{WP}	Write Pulse Width	50		ns
t_{DW}	Time Input Data Appears at Output Following a Write Command		90	ns
t_{WO}	Data In and Write Enable Overlap Time	45		ns
t_{WSA}	Address to Write Enable Setup Time	0		ns
t_{WHA}	Address to Write Enable Hold Time	0		ns
t_{WSCS}	Chip Enable to Write Enable Setup Time	10		ns
t_{WHCH}	Chip Enable to Write Enable Hold Time	0		ns
t_{ON}	Chip Enable to LOW Impedance Delay	0		ns
t_{OFF}	Chip Enable to HIGH Impedance Delay		25	ns

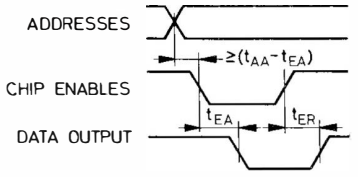
STANDARD TEST LOAD



$R_1 = 300\ \Omega$
$R_2 = 600\ \Omega$

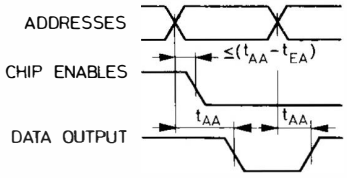
DEFINITION OF WAVEFORMS

READ CYCLE



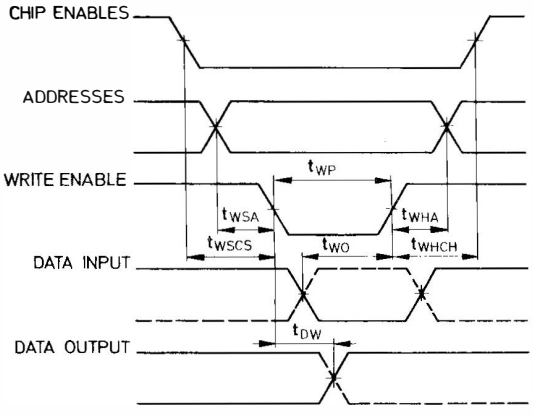
3667

Chip Enable to Output Delay



Address to Output Delay 3668

WRITE CYCLE



Input Pulse Amplitude 3.0 V
Input Rise and Fall Times
5 ns from 1.0 V to 2.0 V
Measurements Made at 1.5 V

3669

TRUTH TABLE

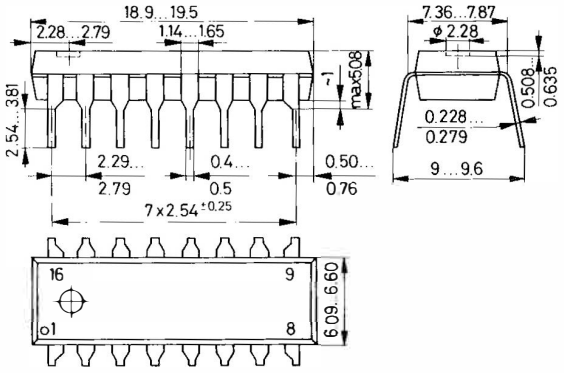
CHIP ENABLE	WRITE ENABLE	OPERATION	DATA OUTPUTS
All LOW	LOW	Write	Complement of Data Input
All LOW	HIGH	Read	Complement of Written Data
One or More HIGH	Don't Care (HIGH or LOW)	Hold	HIGH Impedance State

256×1-BIT FULLY DECODED RANDOM ACCESS MEMORY

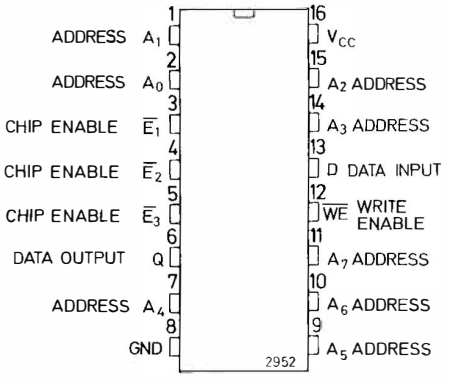
- **Open Collector Output**
- **55 ns Max. Access Time**
- **Advanced Schottky Processing**
- **Low Input Current (250 μA Max.)**
- **Single Layer Metal for Reliability**
- **The Data Stored is on the Data Out Pin During Write Cycle**
- **Fully Decoded with 3 Chip Enables**

DESCRIPTION – The TM107PC is a high speed 256-bit Random Access Memory with full decoding on chip. It is organized 256 words by one bit and is designed for scratchpad, buffer and distributed main memory applications. The device has three chip enable lines to simplify its use in larger memory systems. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. An uncommitted collector output is provided to permit "OR-ties" for ease of memory expansion.

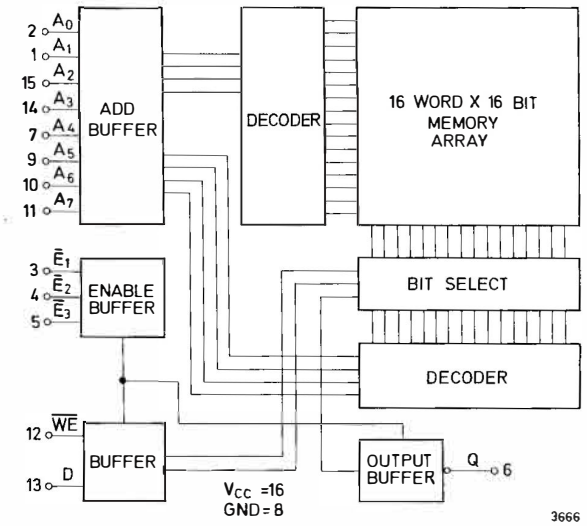
PACKAGE OUTLINE
(P) 9B 16-Lead Molded Dual In-line



CONNECTION DIAGRAM
(TOP VIEW)



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0.5 V to 7.0 V
Input Voltage	–0.5 V to 5.5 V
Input Current	–25 mA to 5.0 mA
Output Current	100 mA
Storage Temperature	–65 °C to +150 °C
Ambient Temperature	0 °C to + 70 °C

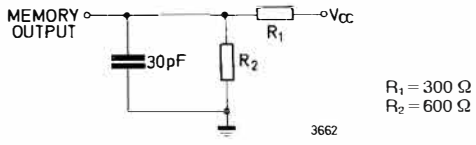
DC CHARACTERISTICS (Guaranteed over the Following Ranges: $V_{CC} = +5.0\ V \pm 5\%$, $T_A = 0\ °C$ to $+70\ °C$)

SYMBOL	PARAMETER	V_{CC}	OTHER CONDITIONS		MIN.	TYP.	MAX.	UNITS
V_{IL}	LOW Level Input Voltage						0.8	V
V_{IH}	HIGH Level Input Voltage				2.0			V
V_{IC}	Input Clamp Voltage	MIN.	$I_I = -5.0\ mA$				−1.0	V
I_{IL}	LOW Level Input Current	MAX.	$V_I = 0.45\ V$				−250	μA
I_{IH}	HIGH Level Input Current	MAX.	$V_I = 2.4\ V$				40	μA
I_I	Max. Level Input Current	MAX.	$V_I = 5.5\ V$				1.0	mA
I_{CC}	Power Supply Current	MAX.					130	mA
C_I	Input Capacitance	5.0 V	$V_I = 2.0\ V$	$T_A = 25\ °C$,		7.0		pF
C_O	Output Capacitance	5.0 V	$V_O = 2.0\ V$	$f = 1\ MHz$		8.0		pF
I_{CEX}	Output Leakage Current	MAX.	$V_O = 2.4\ V$				100	μA
V_{OL}	LOW Level Output Voltage	MIN.	$I_{OL} = 15\ mA$				0.5	V

AC CHARACTERISTICS (with Standard Test Load) $V_{CC} = +5.0\ V$, $T_A = 25\ °C$

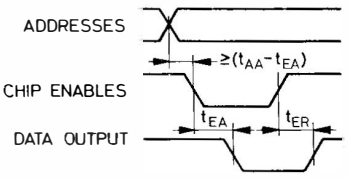
SYMBOL	PARAMETER	MIN.	MAX.	UNITS
t_{AA}	Address Access Time	20	55	ns
t_{EA}	Enable Access Time	5	35	ns
t_{ER}	Enable Recovery Time	5	35	ns
t_{WP}	Write Pulse Width	50		ns
t_{DW}	Time Input Data Appears at Output Following a Write Command		90	ns
t_{WO}	Data In and Write Enable Overlap Time	45		ns
t_{WSA}	Address to Write Enable Setup Time	0		ns
t_{WHA}	Address to Write Enable Hold Time	0		ns
t_{WSCS}	Chip Enable to Write Enable Setup Time	10		ns
t_{WHCH}	Chip Enable to Write Enable Hold Time	0		ns

STANDARD TEST LOADS



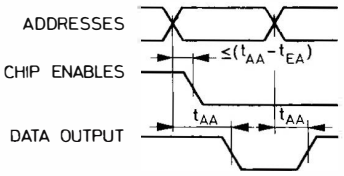
DEFINITION OF WAVEFORMS

READ CYCLE



3667

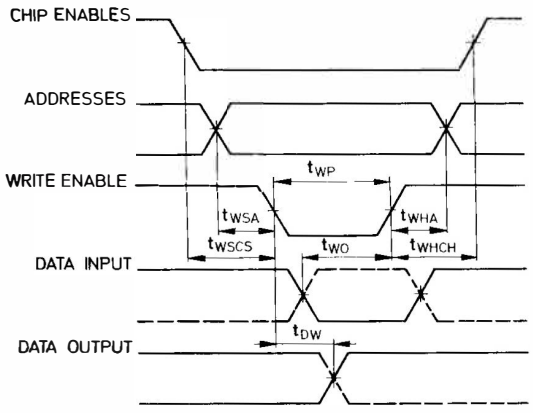
Chip Enable to Output Delay



3668

Address to Output Delay

WRITE CYCLE



3669

Input Pulse Amplitude 3.0 V
Input Rise and Fall Times
5 ns from 1.0 V to 2.0 V
Measurements Made at 1.5 V

TRUTH TABLE

CHIP ENABLE	WRITE ENABLE	OPERATION	DATA OUTPUTS
All LOW	LOW	Write	Complement of Data Input
All LOW	HIGH	Read	Complement of Written Data
One or More HIGH	Don't Care (HIGH or LOW)	Hold	HIGH

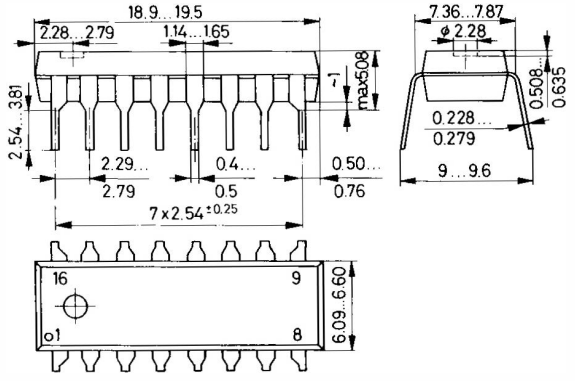
32×8-BIT PROGRAMMABLE READ ONLY MEMORY

- **Open Collector Outputs**
- **Field Programmable with Simple Programming Procedure**
- **Advanced Schottky Processing**
- **Fact Access Time – 40 ns**
- **Low Power Dissipation – 1.2 mW/bit**
- **Fully Decoded – On Chip Address Decoding**
- **DTL and TTL Compatible**
- **Enable Input Simplify Memory Expansion**

DESCRIPTION – The TM188PC is a field programmable, 256-bit, read only memory organized as 32 words of eight bits each. This monolithic, high-speed memory array is addressed in five-bit binary with full on chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the function causing all eight outputs to remain high. The TM188PC is supplied with all bits stored as logic "1"s and can be programmed to logic "0"s by following the programming procedure.

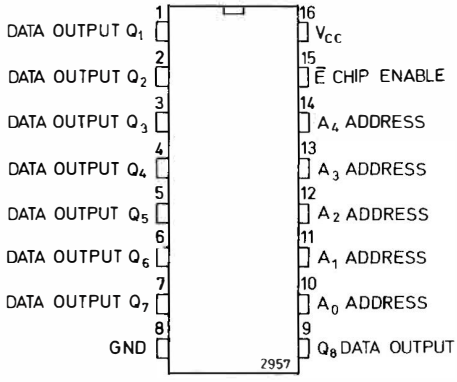
PACKAGE OUTLINE

(P) 9B 16-Lead Molded Dual In-line

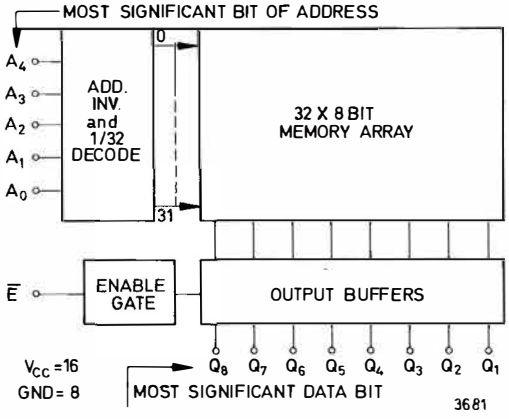


CONNECTION DIAGRAM

(TOP VIEW)



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0.5 V to 7.0 V
Input Voltage	–1.5 V to 5.5 V
Input Current	–20 mA to 5.0 mA
Output Current	100 mA
Storage Temperature	–65 °C to +150 °C
Ambient Temperature	0 °C to + 70 °C

DC CHARACTERISTICS (Guaranteed over the Following Ranges: $V_{CC} = +5.0\ V \pm 5\%$, $T_A = 0\ °C$ to $+70\ °C$)

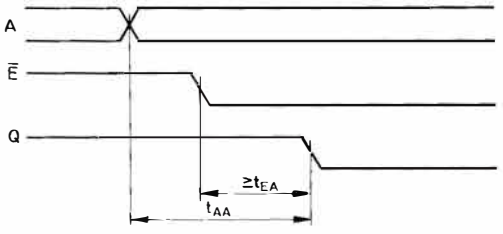
SYMBOL	PARAMETER	V_{CC}	OTHER CONDITIONS		MIN.	TYP.	MAX.	UNITS
V_{IL}	LOW Level Input Voltage						0.8	V
V_{IH}	HIGH Level Input Voltage				2.0			V
V_{IC}	Input Clamp Voltage	MIN.	$I_I = -18$ mA			−1.0	−1.5	V
I_{IL}	LOW Level Input Current	MAX.	$V_I = 0.45$ V				−250	μA
I_{IH}	HIGH Level Input Current	MAX.	$V_I = 2.4$ V				40	μA
I_I	Max. Level Input Current	MAX.	$V_I = 5.5$ V				1.0	mA
I_{CC}	Power Supply Current	5.0 V					125	mA
C_I	Input Capacitance	5.0 V	$V_I = 2.0$ V	$T_A = 25\ °C$,		7.0		pF
C_O	Output Capacitance	5.0 V	$V_O = 2.0$ V	$f = 1$ MHz		8.0		pF
I_{CEX}	Output Leakage Current	MAX.	$V_O = 2.4$ V				100	μA
V_{OL}	LOW Level Output Voltage	MIN.	$I_{OL} = 16$ mA			0.35	0.5	V

AC CHARACTERISTICS (with Standard Test Load) $V_{CC} = +5.0$ V, $T_A = 25\ °C$

SYMBOL	PARAMETER	MAX.	UNITS
t_{AA}	Address Access Time	55	ns
t_{EA}	Enable Access Time	30	ns
t_{ER}	Enable Recovery Time	30	ns

DEFINITION OF WAVEFORMS

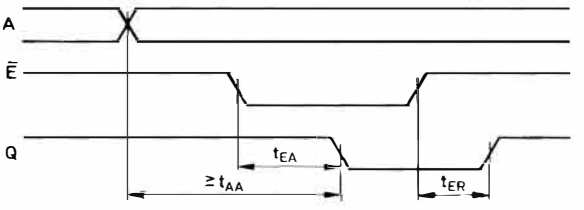
ADDRESS ACCESS TIME



3678

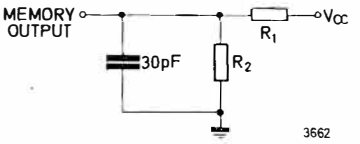
Input Pulse Amplitude 3.0 V
Input Rise and Fall Times
5 ns from 1.0 V to 2.0 V
Measurements Made at 1.5 V

CHIP ENABLE ACCESS TIME AND RECOVERY TIME



3679

STANDARD TEST LOAD



3662

$R_1 = 375\ \Omega$
$R_2 = 750\ \Omega$

PROGRAMMING INSTRUCTIONS

Device Description

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming.

Programming Description

To select a particular fusible link for programming, the word address is presented with TTL levels on all inputs, a V_{CC} of 5.5 V is applied or left applied, and the output to be programmed are taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.
Enable input ($\bar{E}$) must be high during programming.

Verification

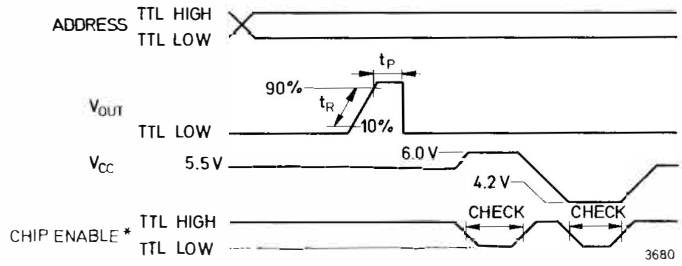
After programming a device, it can be checked for a low output by enabling the part. Since we must guarantee operation at minimum and maximum V_{CC}, load current and temperature, the device must be required to sink 12 mA at 4.2 V V_{CC} and 0.2 mA at 6.0 V V_{CC} at room temperature.

PROGRAMMING SPEED

Typically, fuses will blow on the rise time of the first pulse. In automated programmes which must copy devices in a short time because of production requirements, the following pulse and voltage sequences have been found to maximize reliability, programming yield and thruput. The device should be verified after each programming attempt and be advanced to the next bit in the device has programmed.

PULSE NUMBER	OUTPUT VOLTAGE
1 to 3	20 V
4 to 6	23 V
7 to 9	26 V

PROGRAMMING TIMING



*NOTE
Output Load = 0.2 mA During 6.0 V Check
Output Load = 12 mA During 4.2 V Check

PROGRAMMING PARAMETERS (Do not test these parameters or you may program the device)

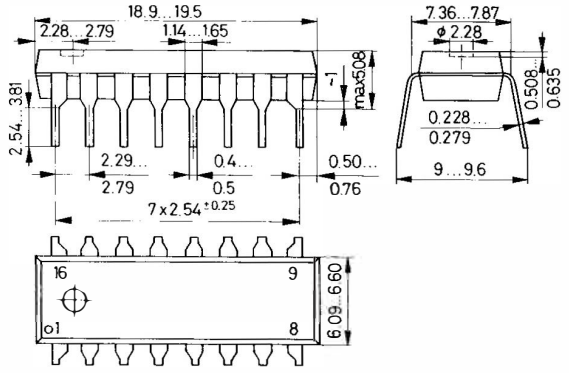
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
t_R	Rise Time Rate of Program Pulse Applied to the Data Out		0.34	0.40	0.46	V/µs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
t_P	Program Pulse Width		1		40	µs
I_{OLV1}	Output Current Required During Verification	Chip Enabled $T_A = 25$ °C, $V_{CC} = 4.2$ V	11	12	13	mA
I_{OLV2}	Output Current Required During Verification	Chip Enabled $T_A = 25$ °C, $V_{CC} = 6.0$ V	0.19	0.20	0.21	mA
MDC	Maximum Duty Cycle During Automatic Programming of Output Pin	t_P/t_C			25	%
V_{outP}	Required Programming Voltage on Output Pin		20	20	26	V
I_{LP}	Required Current Limit of Power Supply Feeding Output During Programming	$V_{outP} = 26$ V, $V_{CC} = 5.5$ V	240			mA

256×4-BIT PROGRAMMABLE READ ONLY MEMORY

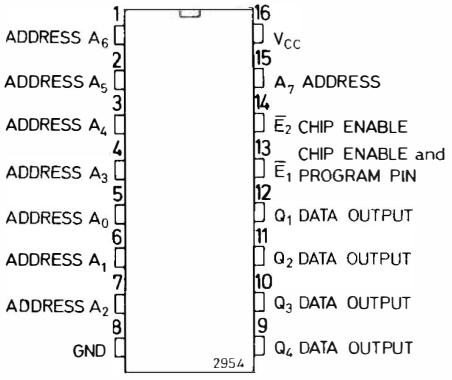
- **Open Collector Outputs**
- **The Lowest Power Dissipation in the Industry**
- **Advanced Schottky Processing**
- **Very High Programmability**
- **Field Programmable with Simple Programming Procedure**
- **Fast Programming Time – Average of 1 ms/Bit**
- **Very High Reliability**
- **Fully Decoded – On Chip Address Decoding**

DESCRIPTION – The TM601PC is a fully decoded high speed 1024-bit field Programmable ROM organized 256 words by four bits per word, and it has uncommited collector outputs. The outputs are disabled when either $\overline{E}_1$ or $\overline{E}_2$ are in the HIGH state. The TM601PC is supplied with all bits stored as logic "1"s and can be programmed to logic "0"s by following the programming procedure.

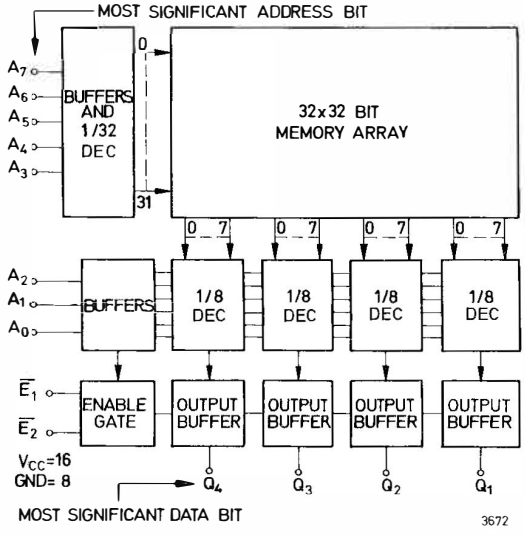
PACKAGE OUTLINE
(P) 9B 16-Lead Molded Dual In-line



CONNECTION DIAGRAM
(TOP VIEW)



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.5 V to 7.0 V
Input Voltage	−1.5 V to 5.5 V
Input Current	−20 mA to 5.0 mA
Output Current	100 mA
Storage Temperature	−65 °C to +150 °C
Ambient Temperature	0 °C to + 70 °C

DC CHARACTERISTICS (Guaranteed over the Following Ranges: $V_{CC} = +5.0\ V \pm 5\%$, $T_A = 0\ °C$ to $+70\ °C$)

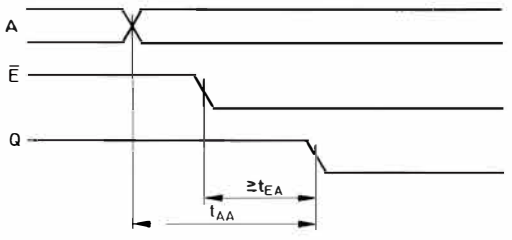
SYMBOL	PARAMETER	V_{CC}	OTHER CONDITIONS		MIN.	TYP.	MAX.	UNITS
V_{IL}	LOW Level Input Voltage						0.8	V
V_{IH}	HIGH Level Input Voltage				2.0			V
V_{IC}	Input Clamp Voltage	MIN.	$I_I = -18$ mA			−1.0	−1.5	V
I_{IL}	LOW Level Input Current	MAX.	$V_I = 0.45$ V				−250	μA
I_{IH}	HIGH Level Input Current	MAX.	$V_I = 2.4$ V				40	μA
I_I	Max. Level Input Current	MAX.	$V_I = 4.5$ V (Program Pin) 5.5 V (Other Inputs)				1.0	mA
I_{CC}	Power Supply Current	MAX.					130	mA
C_I	Input Capacitance	5.0 V	$V_I = 2.0$ V	$T_A = 25\ °C$,		7.0		pF
C_O	Output Capacitance	5.0 V	$V_O = 2.0$ V	$f = 1$ MHz		8.0		pF
I_{CEX}	Output Leakage Current	MAX.	$V_O = 2.4$ V				100	μA
V_{OL}	LOW Level Output Voltage	MIN.	$I_{OL} = 16$ mA			0.35	0.5	V

AC CHARACTERISTICS (with Standard Test Load) $V_{CC} = +5.0$ V, $T_A = 25\ °C$

SYMBOL	PARAMETER	MAX.	UNITS
t_{AA}	Address Access Time	55	ns
t_{EA}	Enable Access Time	30	ns
t_{ER}	Enable Recovery Time	30	ns

DEFINITION OF WAVEFORMS

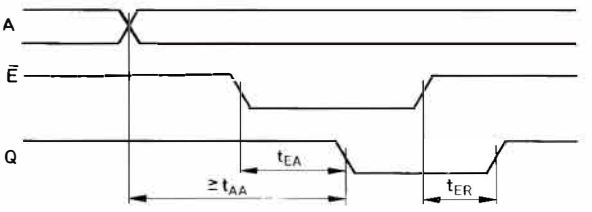
ADDRESS ACCESS TIME



3678

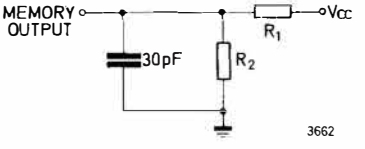
Input Pulse Amplitude 3.0 V
Input Rise and Fall Times
5 ns from 1.0 V to 2.0 V
Measurements Made at 1.5 V

CHIP ENABLE ACCESS TIME AND RECOVERY TIME



3679

STANDARD TEST LOAD



$R_1 = 300\ \Omega$
$R_2 = 600\ \Omega$

3662

PROGRAMMING INSTRUCTIONS

Device Description

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming.

Programming Description

To select a particular fusible link for programming, the word address is presented with TTL levels on all inputs, a V_{CC} of 5.5 V is applied or left applied, and the program pin (ordinarily an enable input) and the output to be programmed are taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.

Other Enable Input

Other enable input is logic enable and is not used during programming. It may be high, low or open during programming. When checking that an output is programmed (which is called verification), the PROM must be enabled. The simplest procedure is to tie other enables into the enable position for programming and verification.

Timing

The programming procedure involves the use of the program pin (an enable) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse. A 100 ns delay is adequate. The programming pulse applied to the output pin and program pin must have a rise time rate of 0.34 V/μs to 0.46 V/μs.

Verification

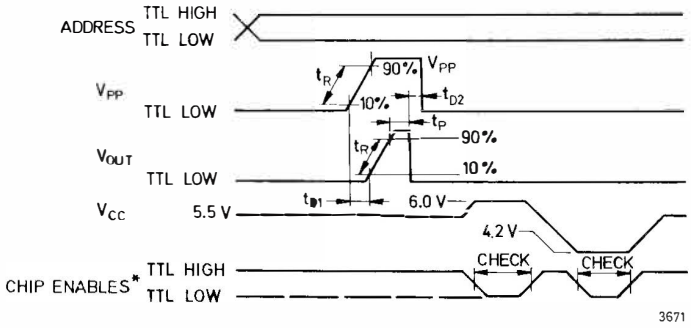
After programming a device, it can be checked for a low output by enabling the part. Since we must guarantee operation at minimum and maximum V_{CC}, load current and temperature, the device must be required to sink 12 mA at 4.2 V V_{CC} and 0.2 mA at 6.0 V V_{CC} at room temperature.

PROGRAMMING SPEED

Typically, fuses will blow on the rise time of the first pulse. In automated programmers which must copy devices in short time because of production requirements, the following pulse and voltage sequences have been found to maximize reliability, programming yield and thruput. The device should be verified after each programming attempt and be advanced to the next bit in the device has programmed.

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27 V	20 V
4 to 6	30 V	23 V
7 to 9	33 V	26 V

PROGRAMMING TIMING



$t_R = 0.4$ V/μs ± 15%
$t_P = 1$ μs MIN., 40 μs MAX.
$t_{D1} = 80$ μs ± 10 μs
$t_{D2} = 100$ ns MIN.

*NOTE
Output Load = 0.2 mA During 6.0 V Check
Output Load = 12 mA During 4.2 V Check

PROGRAMMING PARAMETERS (Do not test these parameters or you may program the device)

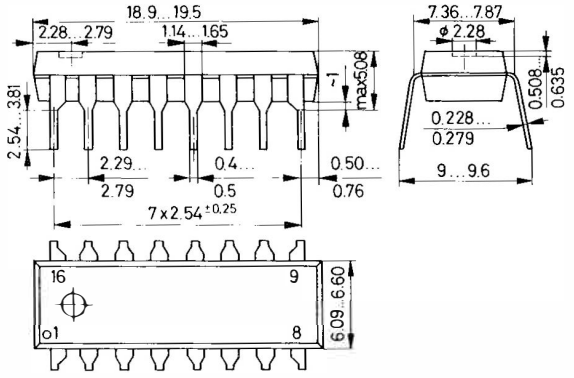
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
t_R	Rise Time Rate of Program Pulse Applied to the Data Out or Program Pin		0.34	0.40	0.46	V/μs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
I_{OLV1}	Output Current Required During Verification	Chip Enabled $T_A = 25$ °C, $V_{CC} = 4.2$ V	11	12	13	mA
I_{OLV2}	Output Current Required During Verification	Chip Enabled $T_A = 25$ °C, $V_{CC} = 6.0$ V	0.19	0.20	0.21	mA
MDC	Maximum Duty Cycle During Automatic Programming of Program Pin and Output Pin	t_P/t_C			25	%
V_{PP}	Required Programming Voltage on Program Pin		27	27	33	V
V_{outP}	Required Programming Voltage on Output Pin		20	20	26	V
I_{LP}	Required Current Limit of Power Supply Feeding Program Pin and Output During Programming	$V_{PP} = 33$ V, $V_{outP} = 26$ V, $V_{CC} = 5.5$ V	240			mA
t_{D1}	Required Time Delay between Disabling Memory Output and Application of Output Programming Pulse	Measure at 10% Levels	70	80	90	μs
t_{D2}	Required Time Delay between Removal of Programming Pulse and Enabling Memory Output	Measure at 10% Levels	100			ns

256×4-BIT PROGRAMMABLE READ ONLY MEMORY

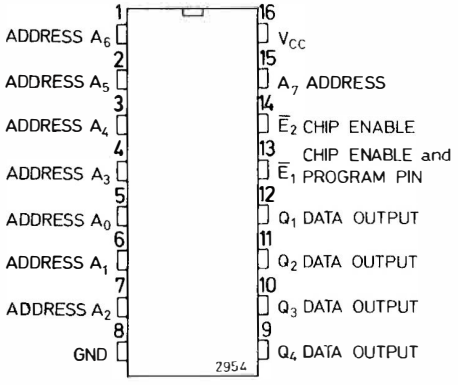
- **3-State Outputs**
- **The Lowest Power Dissipation in the Industry**
- **Advanced Schottky Processing**
- **Very High Programmability**
- **Field Programmable with Simple Programming Procedure**
- **Fast Programming Time-Average of 1 ms/Bit**
- **Very High Reliability**
- **Fully Decoded-On Chip Address Decoding**

DESCRIPTION – The TM621PC is a fully decoded high speed 1024-bit field Programmable ROM organized 256 words by four bits per word, and it has 3-state outputs. The outputs are disabled when either $\overline{E}_1$ or $\overline{E}_2$ are in the HIGH state. The TM621PC is suppled with all bits stored as logic "1"s and can be programmed to logic "0"s by following the programming procedure.

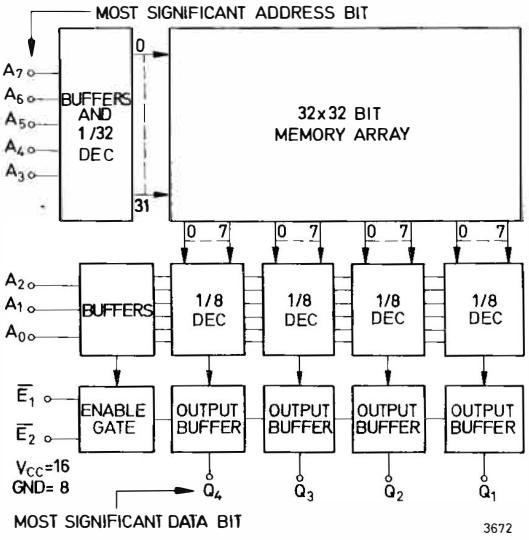
PACKAGE OUTLINE
(P) 9B 16-Lead Molded Dual In-line



CONNECTION DIAGRAM
(TOP VIEW)



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0.5 V to 7.0 V
Input Voltage	–1.5 V to 5.5 V
Input Current	–20 mA to 5.0 mA
Output Current	–100 mA to 100 mA
Storage Temperature	–65 °C to +150 °C
Ambient Temperature	0 °C to + 70 °C

DC CHARACTERISTICS (Guaranteed over the Following Ranges: $V_{CC} = +5.0\ V \pm 5\%$, $T_A = 0\ °C$ to $+70\ °C$)

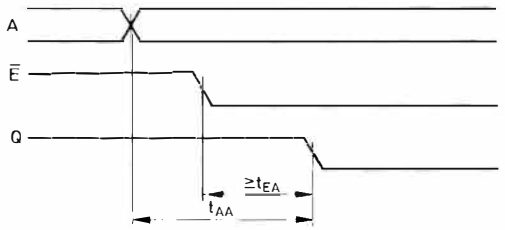
SYMBOL	PARAMETER	V_{CC}	OTHER CONDITIONS		MIN.	TYP.	MAX.	UNITS
V_{IL}	LOW Level Input Voltage						0.8	V
V_{IH}	HIGH Level Input Voltage				2.0			V
V_{IC}	Input Clamp Voltage	MIN.	$I_I = -18\ mA$			−1.0	−1.5	V
I_{IL}	LOW Level Input Current	MAX.	$V_I = 0.45\ V$				−250	µA
I_{IH}	HIGH Level Input Current	MAX.	$V_I = 2.4\ V$				40	µA
I_I	Max. Level Input Current	MAX.	$V_I = 4.5\ V$ (Program Pin) $5.5\ V$ (Other Inputs)				1.0	mA
I_{CC}	Power Supply Current	MAX.					130	mA
C_I	Input Capacitance	5.0 V	$V_I = 2.0\ V$	$T_A = 25\ °C$,		7.0		pF
C_O	Output Capacitance	5.0 V	$V_O = 2.0\ V$	$f = 1\ MHz$		8.0		pF
I_{LZ}	LOW Level OFF State Output Current	MAX.	$V_O = 0.5\ V$				−100	µA
I_{HZ}	HIGH Level OFF State Output Current	MAX.	$V_O = 2.4\ V$				100	µA
I_{OS}	Output Short Circuit Current	5.0 V	$V_O = 0\ V$		−20	−50	−90	mA
V_{OH}	HIGH Level Output Voltage	MIN.	$I_{OH} = -3.2\ mA$		2.4	3.2		V
V_{OL}	LOW Level Output Voltage	MIN.	$I_{OL} = 16\ mA$			0.35	0.5	V

AC CHARACTERISTICS (with Standard Test Load) $V_{CC} = +5.0\ V$, $T_A = 25\ °C$

SYMBOL	PARAMETER	MAX.	UNITS
t_{AA}	Address Access Time	90	ns
t_{EA}	Enable Access Time	30	ns
t_{ER}	Enable Recovery Time	30	ns

DEFINITION OF WAVEFORMS

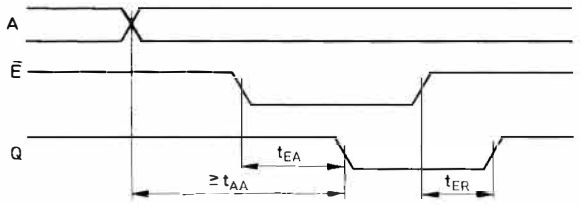
ADDRESS ACCESS TIME



3678

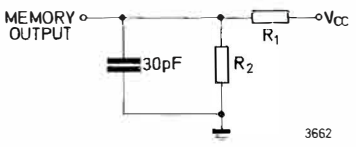
Input Pulse Amplitude 3.0 V
Input Rise and Fall Times
5 ns from 1.0 V to 2.0 V
Measurements Made at 1.5 V

CHIP ENABLE ACCESS TIME AND RECOVERY TIME



3679

STANDARD TEST LOAD



3662

$R_1 = 300\ \Omega$
$R_2 = 600\ \Omega$

PROGRAMMING INSTRUCTIONS

Device Descriptions

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming.

Programming Description

To select a particular fusible link for programming, the word address is presented with TTL levels on all inputs, a V_{CC} of 5.5 V is applied or left applied, and the program pin (ordinarily an enable input) and the output to be programmed are taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.

Other Enable Input

Other enable input is logic enable and is not used during programming. It may be high, low or open during programming. When checking that an output is programmed (which is called verification), the PROM must be enabled. The simplest procedure is to tie other enables into the enable position for programming and verification.

Timing

The programming procedure involves the use of the program pin (an enable) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse. A 100 ns delay is adequate. The programming pulse applied to the output pin and program pin must have a rise time rate of 0.34 V/μs to 0.46 V/μs.

Verification

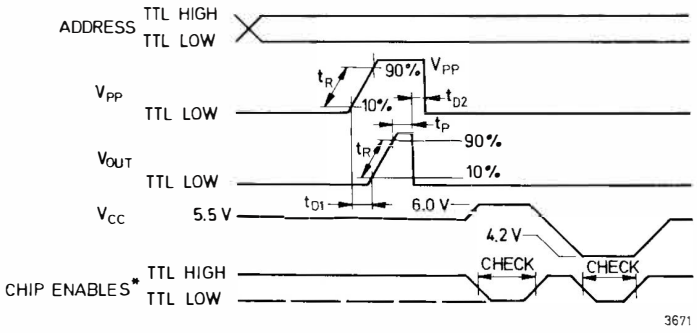
After programming a device, it can be checked for a low output by enabling the part. Since we must guarantee operation at minimum and maximum V_{CC}, load current and temperature, the device must be required to sink 12 mA at 4.2 V V_{CC} and 0.2 mA at 6.0 V V_{CC} at room temperature.

PROGRAMMING SPEED

Typically, fuses will blow on the rise time of the first pulse. In automated programmers which must copy devices in a short time because of production requirements, the following pulse and voltage sequences have been found to maximize reliability, programming yield and thruput. The device should be verified after each programming attempt and be advanced to the next bit in the device has programmed.

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27 V	20 V
4 to 6	30 V	23 V
7 to 9	33 V	26 V

PROGRAMMING TIMING



t_R = 0.4 V/μs±15%
t_P = 1 μs MIN., 40 μs MAX.
t_{D1} = 80 μs±10μs
t_{D2} = 100 ns MIN.

*NOTE
Output Load = 0.2 mA During 6.0 V Check
Output Load = 12 mA During 4.2 V Check

PROGRAMMING PARAMETERS (Do not test these parameters or you may program the device)

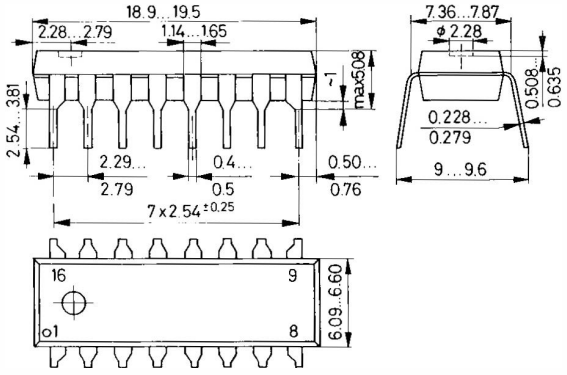
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
t_R	Rise Time Rate of Program Pulse Applied to the Data Out or Program Pin		0.34	0.40	0.46	V/μs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
I_{OLV1}	Output Current Required During Verification	Chip Enabled T_A = 25 °C, V_{CC} = 4.2 V	11	12	13	mA
I_{OLV2}	Output Current Required During Verification	Chip Enabled T_A = 25 °C, V_{CC} = 6.0 V	0.19	0.20	0.21	mA
MDC	Maximum Duty Cycle During Automatic Programming of Program Pin and Output Pin	t_P/t_C			25	%
V_{PP}	Required Programming Voltage on Program Pin		27	27	33	V
V_{outP}	Required Programming Voltage on Output Pin		20	20	26	V
I_{LP}	Required Current Limit of Power Supply Feeding Program Pin and Output During Programming	V_{PP} = 33 V, V_{outP} = 26 V, V_{CC} = 5.5 V	240			mA
t_{D1}	Required Time Delay between Disabling Memory Output and Application of Output Programming Pulse	Measure at 10% Levels	70	80	90	μs
t_{D2}	Required Time Delay between Removal of Programming Pulse and Enabling Memory Output	Measure at 10% Levels	100			ns

512×4-BIT PROGRAMMABLE READ ONLY MEMORY

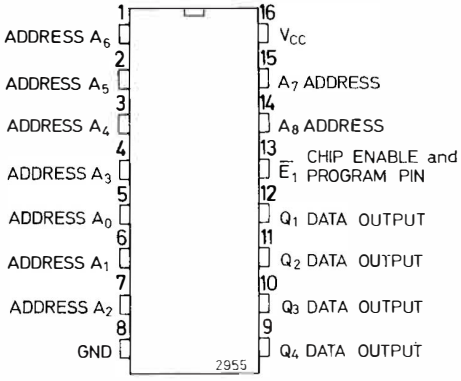
- **3-State Outputs**
- **Very High Programmability**
- **Advanced Schottky Processing**
- **Field Programmable with Simple Programming Procedure**
- **Fast Programming Time – Average of 1 ms/Bit**
- **Very High Reliability**
- **Fully Decoded – On Chip Address Decoding**

DESCRIPTION –The TM622PC is a fully decoded high speed 2048-bit field Programmable ROM organized 512 words by four bits per word, and it has 3-state outputs. The outputs are off when $\overline{E}_1$ input is in the HIGH state. The TM622PC is supplied with all bits stored as logic "1"s and can be programmed to logic "0"s by following the programming procedure.

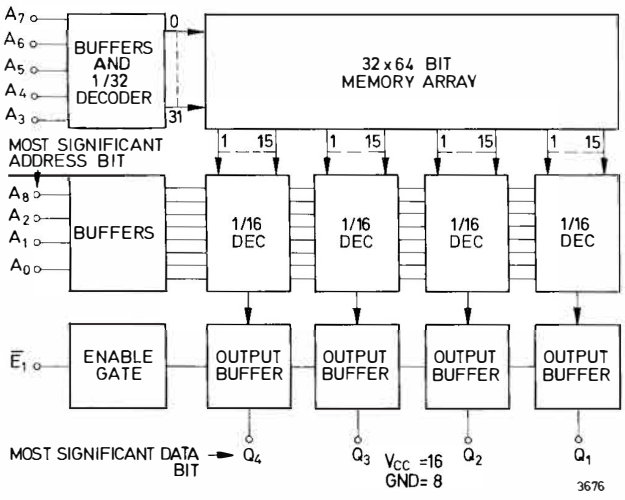
PACKAGE OUTLINE
(P) 9B 16-Lead Molded Dual In-line



CONNECTION DIAGRAM
(TOP VIEW)



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0.5 V to 7.0 V
Input Voltage	–1.5 V to 5.5 V
Input Current	–20 mA to 5.0 mA
Output Current	–100 mA to 100 mA
Storage Temperature	–65 °C to +150 °C
Ambient Temperature	0 °C to + 70 °C

DC CHARACTERISTICS (Guaranteed over the Following Ranges: $V_{CC} = +5.0\ V \pm 5\%$, $T_A = 0\ °C$ to $+70\ °C$)

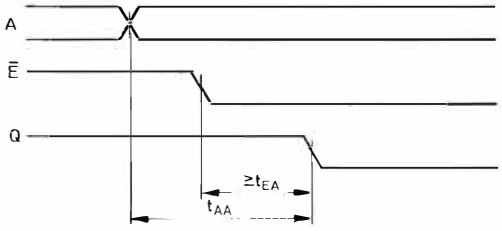
SYMBOL	PARAMETER	V_{CC}	OTHER CONDITIONS		MIN.	TYP.	MAX.	UNITS
V_{IL}	LOW Level Input Voltage						0.8	V
V_{IH}	HIGH Level Input Voltage				2.0			V
V_{IC}	Input Clamp Voltage	MIN.	$I_I = -18\ mA$			−1.0	−1.5	V
I_{IL}	LOW Level Input Current	MAX.	$V_I = 0.45\ V$				−250	μA
I_{IH}	HIGH Level Input Current	MAX.	$V_I = 2.4\ V$				40	μA
I_I	Max. Level Input Current	MAX.	$V_I = 4.5\ V$ (Program Pin) $5.5\ V$ (Other Inputs)				1.0	mA
I_{CC}	Power Supply Current	MAX.					130	mA
C_I	Input Capacitance	5.0 V	$V_I = 2.0\ V$	$T_A = 25\ °C$,		7.0		pF
C_O	Output Capacitance	5.0 V	$V_O = 2.0\ V$	$f = 1\ MHz$		8.0		pF
I_{LZ}	LOW Level OFF State Output Current	MAX.	$V_O = 0.5\ V$				−100	μA
I_{HZ}	HIGH Level OFF State Output Current	MAX.	$V_O = 2.4\ V$				100	μA
I_{OS}	Output Short Circuit Current	5.0 V	$V_O = 0\ V$		−20	−50	−90	mA
V_{OH}	HIGH Level Output Voltage	MIN.	$I_{OH} = -3.2\ mA$		2.4	3.2		V
V_{OL}	LOW Level Output Voltage	MIN.	$I_{OL} = 16\ mA$			0.35	0.5	V

AC CHARACTERISTICS (with Standard Test Load) $V_{CC} = +5.0\ V$, $T_A = 25\ °C$

SYMBOL	PARAMETER	MAX.	UNITS
t_{AA}	Address Access Time	60	ns
t_{EA}	Enable Access Time	30	ns
t_{ER}	Enable Recovery Time	30	ns

DEFINITION OF WAVEFORMS

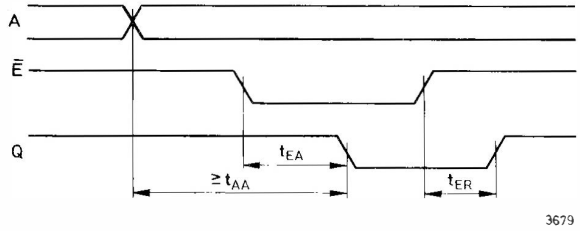
ADDRESS ACCESS TIME



3678

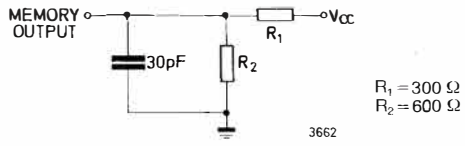
Input Pulse Amplitude 3.0 V
Input Rise and Fall Times
5 ns from 1.0 V to 2.0 V
Measurements Made at 1.5 V

CHIP ENABLE ACCESS TIME AND RECOVERY TIME



3679

STANDARD TEST LOAD



3662

PROGRAMMING INSTRUCTIONS

Device Description

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming.

Programming Description

To select a particular fusible link for programming, the word address is presented with TTL levels on all inputs, a V_{CC} of 5.5 V is applied or left applied, and the program pin (ordinarily an enable input) and the output to be programmed are taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.

Timing

The programming procedure involves the use of the program pin (an enable) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse. A 100 ns delay is adequate. The programming pulse applied to the output pin and program pin must have a rise time rate of 0.34 V/μs to 0.46 V/μs.

Verification

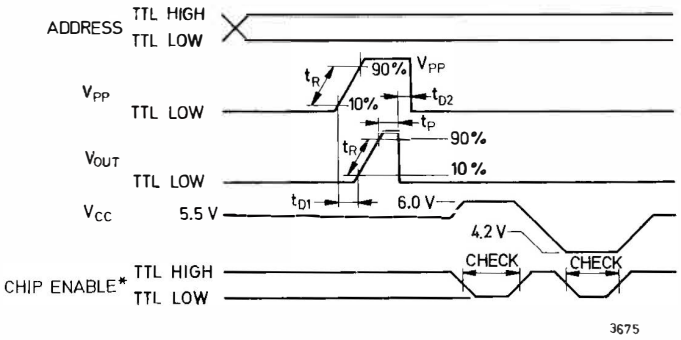
After programming a device, it can be checked for a low output by enabling the part. Since we must guarantee operation at minimum and maximum V_{CC}, load current and temperature, the device must be required to sink 12 mA at 4.2 V V_{CC} and 0.2 mA at 6.0 V V_{CC} at room temperature.

PROGRAMMING SPEED

Typically, fuses will blow on the rise time of the first pulse. In automated programmers which must copy devices in a short time because of production requirements, the following pulse and voltage sequences have been found to maximize reliability, programming yield and thruput. The device should be verified after each programming attempt and be advanced to the next bit in the device has programmed.

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27 V	20 V
4 to 6	30 V	23 V
7 to 9	33 V	26 V

PROGRAMMING TIMING



t_R = 0.4 V/μs±15%
t_P = 1 μs MIN., 40 μs MAX.
t_{D1} = 80 μs±10μs
t_{D2} = 100 ns MIN.

*NOTE
Output Load = 0.2 mA During 6.0 V Check
Output Load = 12 mA During 4.2 V Check

PROGRAMMING PARAMETERS (Do not test these parameters or you may program the device)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
t_R	Rise Time Rate of Program Pulse Applied to the Data Out or Program Pin		0.34	0.40	0.46	V/μs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
I_{OLV1}	Output Current Required During Verification	Chip Enabled T_A = 25 °C, V_{CC} = 4.2 V	11	12	13	mA
I_{OLV2}	Output Current Required During Verification	Chip Enabled T_A = 25 °C, V_{CC} = 6.0 V	0.19	0.20	0.21	mA
MDC	Maximum Duty Cycle During Automatic Programming of Program Pin and Output Pin	t_P/t_C			25	%
V_{PP}	Required Programming Voltage on Program Pin		27	27	33	V
V_{outP}	Required Programming Voltage on Output Pin		20	20	26	V
I_{LP}	Required Current Limit of Power Supply Feeding Program Pin and Output During Programming	V_{PP} = 33 V, V_{outP} = 26 V, V_{CC} = 5.5 V	240			mA
t_{D1}	Required Time Delay between Disabling Memory Output and Application of Output Programming Pulse	Measure at 10% Levels	70	80	90	μs
t_{D2}	Required Time Delay between Removal of Programming Pulse and Enabling Memory Output	Measure at 10% Levels	100			ns

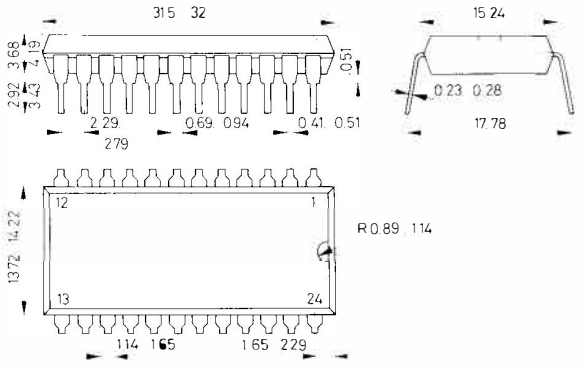
512×8-BIT PROGRAMMABLE READ ONLY MEMORY

- **3-State Outputs**
- **Very High Programmability**
- **Advanced Schottky Processing**
- **Field Programmable with Simple Programming Procedure**
- **Fast Programming Time – Average of 1 ms/Bit**
- **Very High Reliability**
- **Fully Decoded – On Chip Address Decoding**

DESCRIPTION – The TM624PC is a fully decoded high speed 4096-bit field Programmable ROM organized 512 words by eight bits per word, and it has 3-state outputs. The outputs are enabled when $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 and E_4 are HIGH. The TM624PC is supplied with all bits stored as logic "1"s and can be programmed to logic "0" by following the programming procedure.

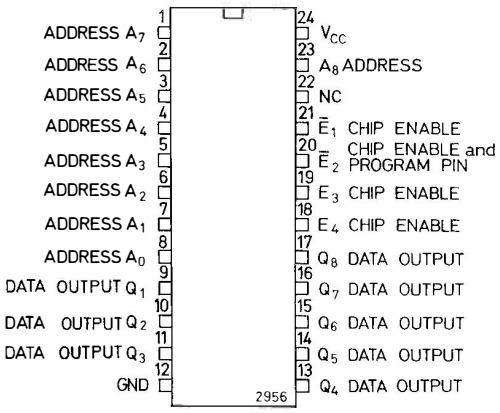
PACKAGE OUTLINE

9N 24-Lead Molded Dual In-line

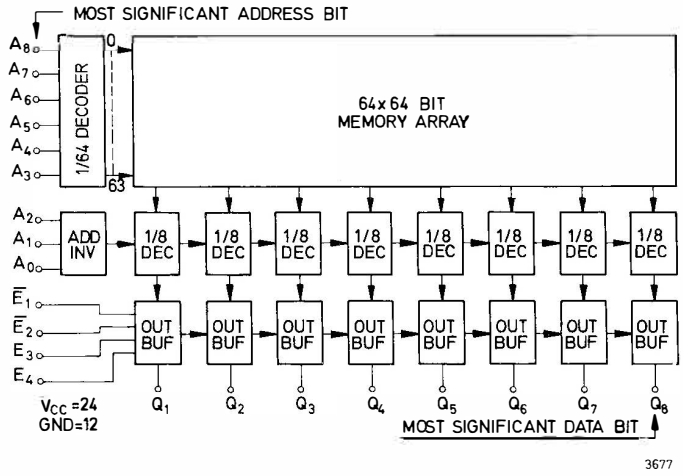


CONNECTION DIAGRAM

(TOP VIEW)



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0.5 V to 7.0 V
Input Voltage	–1.5 V to 5.5 V
Input Current	–20 mA to 5.0 mA
Output Current	–100 mA to 100 mA
Storage Temperature	–65 °C to +150 °C
Ambient Temperature	0 °C to + 70 °C

DC CHARACTERISTICS (Guaranteed over the Following Ranges: $V_{CC} = +5.0\ V \pm 5\%$, $T_A = 0\ °C$ to $+70\ °C$)

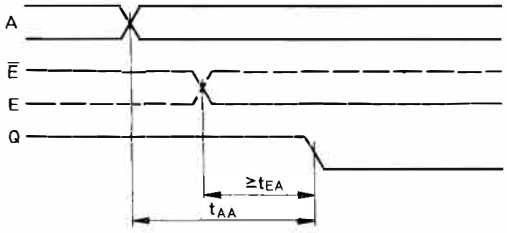
SYMBOL	PARAMETER	V_{CC}	OTHER CONDITIONS		MIN.	TYP.	MAX.	UNITS
V_{IL}	LOW Level Input Voltage						0.8	V
V_{IH}	HIGH Level Input Voltage				2.0			V
V_{IC}	Input Clamp Voltage	MIN.	$I_I = -18$ mA			−1.0	−1.5	V
I_{IL}	LOW Level Input Current	MAX.	$V_I = 0.45$ V				−250	µA
I_{IH}	HIGH Level Input Current	MAX.	$V_I = 2.4$ V				40	µA
I_I	Max. Level Input Current	MAX.	$V_I = 4.5$ V (Program Pin) 5.5 V (Other Inputs)				1.0	mA
I_{CC}	Power Supply Current	MAX.					170	mA
C_I	Input Capacitance	5.0 V	$V_I = 2.0$ V	$T_A = 25\ °C$,		7.0		pF
C_O	Output Capacitance	5.0 V	$V_O = 2.0$ V	$f = 1$ MHz		8.0		pF
I_{LZ}	LOW Level OFF State Output Current	MAX.	$V_O = 0.5$ V				−100	µA
I_{HZ}	HIGH Level OFF State Output Current	MAX.	$V_O = 2.4$ V				100	µA
I_{OS}	Output Short Circuit Current	5.0 V	$V_O = 0$ V		−20	−50	−90	mA
V_{OH}	HIGH Level Output Voltage	MIN.	$I_{OH} = -3.2$ mA		2.4	3.2		V
V_{OL}	LOW Level Output Voltage	MIN.	$I_{OL} = 12$ mA			0.35	0.5	V

AC CHARACTERISTICS (with Standard Test Load) $V_{CC} = +5.0$ V, $T_A = 25$ °C

SYMBOL	PARAMETER	MAX.	UNITS
t_{AA}	Address Access Time	55	ns
t_{EA}	Enable Access Time	30	ns
t_{ER}	Enable Recovery Time	30	ns

DEFINITION OF WAVEFORMS

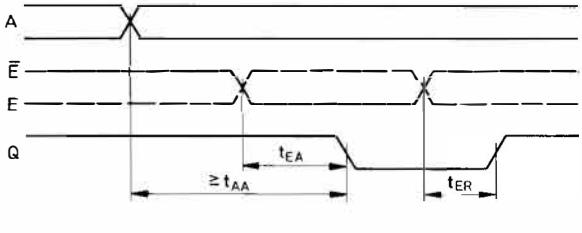
ADDRESS ACCESS TIME



3673

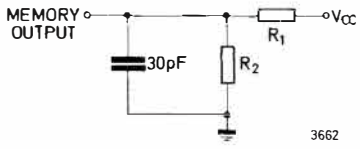
Input Pulse Amplitude 3.0 V
Input Rise and Fall Times
5 ns from 1.0 V to 2.0 V
Measurements Made at 1.5 V

CHIP ENABLE ACCESS TIME AND RECOVERY TIME



3674

STANDARD TEST LOAD



3662

$R_1 = 375\ \Omega$
$R_2 = 750\ \Omega$

PROGRAMMING INSTRUCTIONS

Device Description

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be changed from a low resistance to a high resistance. This procedure is called programming.

Programming Description

To select a particular fusible link for programming, the word address is presented with TTL levels on all inputs, a V_{CC} of 5.5 V is applied or left applied, and the program pin (ordinarily an enable input) and the output to be programmed are taken to an elevated voltage to supply the required current to program the fuse. The outputs must be programmed one output at a time, since internal decoding circuitry is capable of sinking only one unit of programming current at a time.

Other Enable Inputs

Other enable inputs are logic enables and are not used during programming. They may be high, low or open during programming. When checking that an output is programmed (which is called verification), the PROM must be enabled. The simplest procedure is to tie other enables into the enable position for programming and verification.

Timing

The programming procedure involves the use of the program pin (an enable) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse. A 100 ns delay is adequate. The programming pulse applied to the output pin and program pin must have a rise time rate of 0.34 V/μs to 0.46 V/μs.

Verification

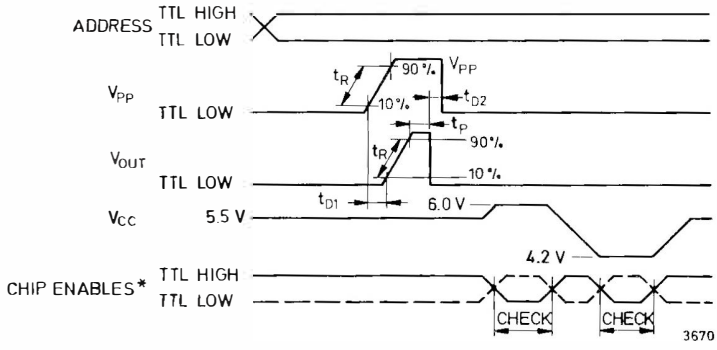
After programming a device, it can be checked for a low output by enabling the part. Since we must guarantee operation at minimum and maximum V_{CC}, load current and temperature, the device must required to sink 12 mA at 4.2 V V_{CC} and 0.2 mA at 6.0 V V_{CC} at room temperature.

PROGRAMMING SPEED

Typically, fuses will blow on the rise time of the first pulse. In automated programmers which must copy devices in a short time because of production requirements, the following pulse and voltage sequences have been found to maximize reliability, programming yield and thruput. The device should be verified after each programming attempt and be advanced to the next bit in the device has programmed.

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27 V	20 V
4 to 6	30 V	23 V
7 to 9	33 V	26 V

PROGRAMMING TIMING



t_R = 0.4 V/μs ± 15%
t_P = 1 μs MIN., 40 μs MAX.
t_{D1} = 80 μs ± 10μs
t_{D2} = 100 ns MIN.

*NOTE
Output Load 0.2 mA During 6.0 V Check
Output Load = 12 mA During 4.2 V Check

PROGRAMMING PARAMETERS (Do not test these parameters or you may program the device)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
t_R	Rise Time Rate of Program Pulse Applied to the Data Out or Program Pin		0.34	0.40	0.46	V/μs
V_{CCP}	V_{CC} Required During Programming		5.40	5.50	5.60	V
I_{OLV1}	Output Current Required During Verification	Chip Enabled T_A = 25 °C, V_{CC} = 4.2 V	11	12	13	mA
I_{OLV2}	Output Current Required During Verification	Chip Enabled T_A = 25 °C, V_{CC} = 6.0 V	0.19	0.20	0.21	mA
MDC	Maximum Duty Cycle During Automatic Programming of Program Pin and Output Pin	t_P/t_C			25	%
V_{PP}	Required Programming Voltage on Program Pin		27	27	33	V
V_{outP}	Required Programming Voltage on Output Pin		20	20	26	V
I_{IP}	Required Current Limit of Power Supply Feeding Program Pin and Output During Programming	V_{PP} = 33 V, V_{outP} = 26 V, V_{CC} = 5.5 V	240			mA
t_{D1}	Required Time Delay between Disabling Memory Output and Application of Output Programming Pulse	Measure at 10% Levels	70	80	90	μs
t_{D2}	Required Time Delay between Removal of Programming Pulse and Enabling Memory Output	Measure at 10% Levels	100			ns

FOR MORE INFORMATION ON TECHNICAL DATA
AND/OR TERMS OF DELIVERY APPLY TO: