UMC

UM82C231
System/Memory Controller

T-52-33-15

1. General Decription

The UM82C231 is a system/memory controller. It performs the CPU interface, AT system bus interface and memory interface functions.

2. Features

- CPU interface and bus control.
- PC/AT expansion bus interface.
- Clock generation.
- Numericl processor 80287 interface.
- Peripheral chip interface.
- Refresh and DMA logic.
- Reset and shut down logic.
- Supports 64K、256K and 1M DRAM
- Supports up to 4M Bytes on board memory.
- Advanced 1.2μ m CMOS technology.
- TTL compatible inputs.
- 136 pin flat package.

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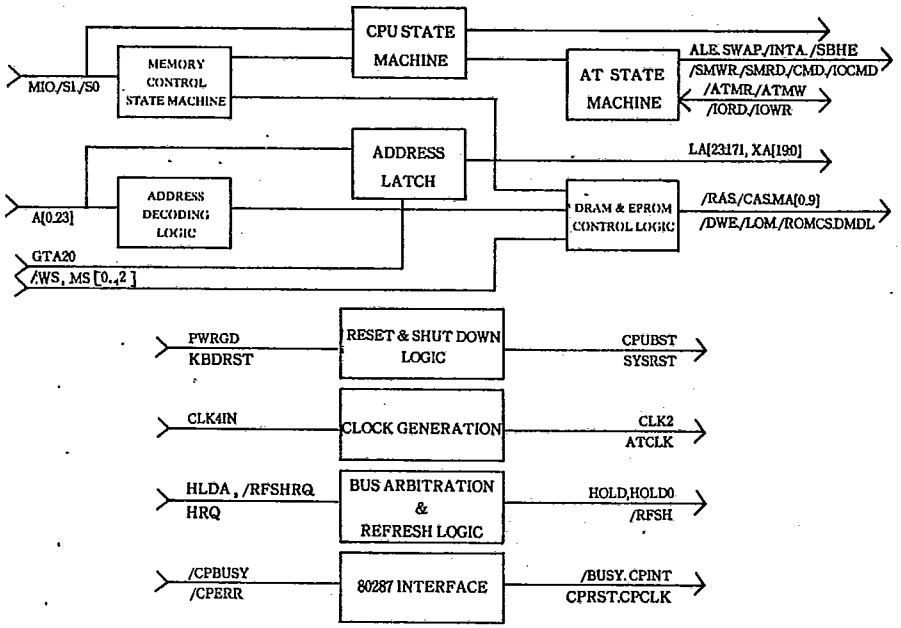
3. UM82C231 Block Diagram



PC Mainboard

UMC

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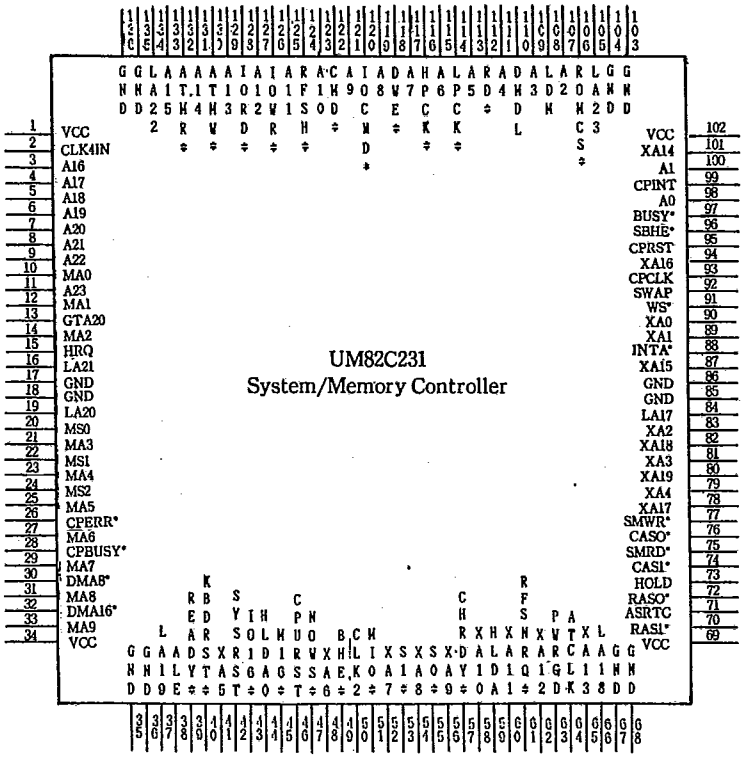
4.UM82C231 Pin Configuration



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5. 82C231 Pin Description

Pin Name.	Pin Type	Pin No.	Description
A(23:0)	I	11,9,8, 7,6, 5,4, 3,133, 131, 129, 127, 125, 123, 121, 119, 117, 115, 113, 111, 109, 107,100,98,	Local address lines from CPU; A(23:17) also connected to 82C206 to represent the DMA page address during DMA cycles.
LA(23:17)	B	105,134,16, 19,37,66,84	AT bus unlatched address bus Bit 23 - Bit 17; These pins are outputs during CPU or DMA cycles and become inputs during REFRESH or MASTER cycles. They have 24 ma current sinking cabability.
XA(19:17)	TO	80,82,78	AT bus latched address bus Bit 19 - Bit 17. They are activated during CPU and DMA cycles; tri-stated otherwise.
XA(16:1)	B	94,87,101, 65, 62, 60, 58, 56, 54, 52, 48, 41, 79,81,83, 89	AT bus latched address bus Bit 16; It is an output pin for CPU or REFRESH cycles and becomes input during DMA or MASTER cycles. XA15 and XA14 have 24 ma current. sinking capability.
XA0	B	90	AT bus latched address bus Bit 0; It is an output pin for CPU, REFRESH or 16-bit DMA cycles and becomes input during 8-bit DMA or MASTER cycles.
GTA20	I	13	AT bus unlatched address bit 20 enable control; the logic low of this signal will force LA20 stay low during CPU cycles.

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Pin Name.	Pin Type	Pin No.	Description
M-I/O.	I	51	Memory or I/O cycle status signal from CPU.
BHE*	I	49	Byte high enable signal from CPU to indicate that high byte accessing is required for the current cycle.
SBHE*	B	96	System Byte high enable to AT bus through buffer; it is output normally and becomes input when MASTER has the AT bus.
CLK4IN	I	2	OSC. input; divided by two to derive CPU CLK2. This signal is also used to control DRAM access timing.
CLK2	0	50	OSC. output; used as the CPU CLK2 source.
ATCLK	0	64	AT system clock connected to AT bus through buffer. This clock output synchronized with CLK2 and generated from CLK4IN/6.
SO*	I	55	CPU status line 0; normally it indicates that the current cycle is write cycle.
S1*	I	53	CPU status line 1; normally it indicates that the current cycle is read cycle.
INTA*	I	88	Interrupt acknowledge cycle indication; when S0*, S1* and M-I/O are monitored low, this signal will be activated.
READY*	O	39	CPU ready signal; CPU samples this signal at the end of every Tc state. The current cycle will be terminated if sampled low.
HLDA	I	59	Hold acknowledge input from CPU; CPU will relinquish the local buses when this signal is active.

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Pin Name.	Pin Type	Pin No.	Description
HRQ	I	15	DMA or MASTER cycle request from 82C206.
RFSHRQ*	I	61	Refresh request signal from 82C206's timer 1 output. normally this signal is activated around 15.6 micro second.
HOLD	O	73	Hold request to CPU; either HRQ or RFSHRQ* is arbitrated. Hold will be generated to ask for the buses.
HLDAO	O	44	DMA or MASTER cycle acknowledge signal to 82C206; if HRQ is arbitrated and CPU relinquishes the buses, HLDAO is activated to notice that the DMA controller or MASTER can issue the control signals to perfrom the transactions.
RFSH*	B	124	Refresh cycle indication; it is an output pin normally and become input pin during MASTER cycles.
PWRGD	I	63	Power good or bad indication; if this signal is low, the system will stay at the reset condition.
KBDRST*	I	40	CPU reset request from keyboard controller; when detect a low pulse of this signal, 82C231 will reset CPU.
CPURST	O	46	CPU reset; for both PWRGD and KBDRST* are low, CPURST will be activated.
SYSRST	O	42	System reset; for PWRGD is low Sysrst will be activated.
CPBUSY*	I	28	Co-processor busy signal; which indicates co-processor is accessed.

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Pin Name.	Pin Type	Pin No.	Description
CPERR*	I	26	Co-processor error signal; indicates co-processor's accessing has error.
BUSY*	O	97	Busy signal to CPU; which indicates that co-processor is busy or has error.
CPINT	O	99	Co-processor interrupt; which indicates that the co-processor has error and the system software has to do somthing.
CPRST	O	95	Co-processor reset; a system reset or a write to IO address F1 hex will trigger this signal active.
CPCLK	O	93	CLK4IN/3 clock output has 33% duty cycle.
DMA8*	I	30	8-bit DMA cycle indication.
DMA16*	I	32	16-bit DMA cycle indication.
CHRDY*	I	57	Channel ready signal from AT bus; 82C231 monitors this signal to determine that if the accessed device requires more wait states to complete the transaction.
NOWS*	I	47	No wait state signal from AT bus; 82C231 monitors this signal to terminate the current AT cycle immediately.
M16*	I	45	Memory data size 16-bit signal from AT bus; 82C231 monitors this signal to determine the memory slave's data size.
IO16*	I	43	IO data size 16-bit signal from AT bus; 82C231 monitors this signal to determine the IO slave's data size.
ALE	O	38	AT bus address latch enable; 82C231 issues this signal to start the AT cycle.

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Pin Name.	Pin Type	Pin No.	Description
RAS*(1:0)	O	70,72	Row address strobes for the local memory; used as bank select.
CAS*(1:0)	O	74,76	Column address strobe for the local memory; used as byte enable.
DWE*	O	118	DRAM write or read control signal.
ROMCS*	O	106	BIOS ROM output enable; this signal is activated when the BIOS area either from 0E0000-0FFFFF or FE0000-FFFFFF address range is accessed.
RD*	O	112	Read cycle status signal for CPU, DMA or MASTER cycle; either IO or memory read in CPU or MASTER cycle, and the the memory read in DMA cycle this signal is activated.
DMDL	O	110	Local DRAM read data latch enable; this signal is used to latch the data and parity bits read from local DRAM by the 82C232.
HPCK*	O	116	High byte parity checking enable; 82C231 issues this signal if to check high byte read data is required.
LPCK*	O	114	Low byte parity checking enable; 82C231 issues this signal if to check low byte read data is required.
LDM*	O	108	Local DRAM accessed indication; when local DRAM is accessed by the bus controllers, 82C231 enables this signal.
ASRTC	O	71	Read Time clock address strobe.
WS*	I	91	Local DRAM wait state control; a low input, 82C231 will insert one wait state.

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Pin Name.	Pin Type	Pin No.	Description
ATMW*	B	130	AT bus memory write command signal; it is an output pin during CPU cycle and becomes input during DMA and MASTER cycles.
ATMR*	B	132	AT bus memory read command signal; it is an output pin during CPU and REFRESH cycle and becomes input during DMA and MASTER cycles.
SMWR*	O	77	AT bus memory write command signal when the memory access address is below one mega byte.
SMRD*	O	75	AT bus memory read command signal when the memory access address is below one mega byte.
IOWR*	B	126	AT bus IO write command signal; it is an output pin during CPU cycle and becomes input during DMA and MASTER cycles.
IORD*	B	128	AT bus IO read command signal; it is an output pin during CPU cycle and becomes input during DMA and MASTER cycles.
SWAP	O	92	High byte data and low byte data swapping control signal; the 82C231 monitors the transaction data size and the slave device's data width, then enable this signal if required.
CMD*	O	122	Command signal; for every AT cycle's read or write cycle this signal will be active and has the same timing as read or write command.
IOCMD*	O	120	IO command signal; for every AT IO cycle's read or write cycle this signal will be active.
MA(9: 0)	O	33, 31, 29, 27, 25, 23, 21,14,12, 10	Multiplexed DRAM row and column address for the local memory

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Pin Name.	Pin Type	Pin No.	Description
MS(2:0)	I	24,22,20	Local DRAM memory configuration select.
VCC		1,34,69 102	
GND		17,18,35 36, 67,68 85,86, 103, 104, 135 136	
Total Pin		136	

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6. Functional Description

The UM82C231 Bus & Memory Controller consists of the following functional sub-modules:

* Reset and Shut Down Logic.

* Clock Generation.

* CPU State Machine, AT Bus State Machine and Memory Control State Machine.

* Bus Abitration Logic, DMA/Master and Refresh Logic.

* Numeric Processor Interface.

* System Control Logic.

* Address Decoding Logic.

* DRAM & EPROM Control Logic.

Overview

The UM82C231 performs the CPU interface, AT system bus interface and the memory control functions. The various functional modules are discussed in this section.

6.1 Reset and Shut Down Logic

Two reset inputs PWRGD and KBDRST# are provided on the UM82C231 chip. PWRGD is the Power Good signal from the power supply. When PWRGD is low, the UM82C231 asserts CPURST for CPU reset and SYSRST for system reset. KBDRST# is generated from the 8042 keyboard controller when a CPU reset is required. CPURST is also activated by the UM82C231 when a shut down condition is detected from CPU status. Both CPURST and SYSRST are asserted for at least 16 CLK2 cycles and are synchronized with respect to CLK2 to meet the setup and hold time requirements of the 80286 CPU.

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6.2 Clock Generation

The UM82C231 provides two synchronous clocks CLK2 and ATCLK for the system. There is only one input clock CLK4IN, driven from a TTL crystal oscillator, running at twice of the CPU clock frequency. ATCLK is also derived from CLK4IN at 1/3 of the CPU clock frequency.

6.3 CPU, AT Bus and Memory Control State Machine.

In order to achieve maximum performance of the 80286 CPU and maintain 100% IBM PC/AT compatibity, it is desirable to run the local memory at the rated maximum CPU frequency and the AT bus at a slower clock frequency. The two state machines still maintain a synchronous protocol.

6.3.1 CPU State Machine

Interface to the 80286 requires interpretation of the status lines S0#, S1# and M-I/O from CPU during phase 1 of TS and generation of READY# during TC to the CPU upon completion of the cycle. A(23:0) will be latched during phase 2 of TS for internal use. Address Decoding Logic then activates Memory Control State Machine for a local memory cycle or AT State Machine for AT cycle. Either State Machine terminates itself and CPU State machine upon completion of its function. READY# will be sent out to the 80286 CPU to finish the cycle.

6.3.2 AT Bus State Machine

The At Bus State Machine gains control when Address Decoding Logic decodes a non-local memory cycle. It uses BCLK which is twice the frequency of AT system clock ATCLK, it also performs the necessary synchronization of control and status signals between the AT bus and the processor. The UM82C231 supports 8 and 16 bit memory or I/O devices located on the AT bus.

AT bus cycle is initiated by asserting ALE in AT-TS 1 state. On the trailing edge of ALE, M16# is sampled for a memory cycle to determine the bus size.

It then enters AT-TC state and provides the command signal. For an I/O cycle, IO16* is sampled after the trailing edge of ALE till the end of the command. Typically, the wait state for an AT 8/16 bit transaction is 5/3 respectively. The command cycle is extended when CHRDY is detected inactive, or is terminated when zero wait state request signal NOW# from AT bus is active. Upon expiration of the wait states, AT State Machine terminates itself and passes internal READY to CPU State Machine for outputting synchronous READY# to the 80286.

6.3.3 Memory Control State Machine

Address Decoding Logic activates Memory Control State Machine when local memory is to be accessed. Memory Control State Machine initiates memory interfacing signals by adapting the configuration strap pin MS(2:0) and information from Address Decoding Logic. The definitions of MS(2:0) are given in the following table.

MS2	MS2	MS0	Bank0	Bank1	Total Memory
0	0	0	256k	-	512k
0	0	1	256k	64k	640k
0	1	0	256k	256k	1Meg
0	1	1	1M	-	2Meg
1	1	1	1M	1M	4Meg
1	0	X	Not Valid		
1	1	0	Not Valid		

6.4 Bus Arbitration Logic, DMA/Master and Refresh Logic

The UM82C231 provides arbitration between the CPU, DRAM refresh logic and DMA/Master devices. It handles HRQ and RESHRQ by generating HOLD request to the CPU. CPU will respond to an active HOLD signal by asserting HLDA and placing most of its output and I/O pins in a high impedance state after completing its current bus cycle. After the CPU relinquishes the bus, the UM82C231 responds by issuing RFSH# or HLDA0 depending on the requesting device.

The arbitration between Refresh and DMA/Master is based on FIFO or first come first serve. However, RFSHRQ will be internally latched and served immediately after DMA/Master finishes its request if RFSHRQ is queued behind HRQ. HRQ has to remain active to be served if RFSHRQ comes first.

During a refresh cycle, refresh address is put out on XA0-XA9 and MA0-MA9 address lines, RFSH# and LDM# are asserted, SMRD# is active 2 SYSCLK after RFSH# is active and RAS#(1: 0) are asserted to refresh DRAMS accordingly.

DMA and Bus Master share the same request pin HRQ. After the UM82C231 receives HRQ it asserts HOLD request to the CPU. Upon finishing the current cycle, the CPU relinquishes the bus by asserting HLDA. The UM82C231 issues HLDAO to the requesting device to start gaining control of the bus. During an active HLDAO period the only way to distinguish between DMA and Bus Master request is to monitor the DMA8# and DMA16# signals. DMA8#/DMA16# active indicates an 8-bit/16bit DMA transfer, while both inactive means a Master cycle.

6.5 Numeric Processor Interface

Incorporated in the UM82C231 is the circuitry to interface an 80287 Numeric Coprocessor to 80286. The circuitry handles the decoding required for selecting and resetting the Numeric Coprocessor, handling CPBUSY# and CPERR# signals from the 80287 to the CPU, and generating interrupt signals for error handling.

While executing a task, the 80287 issues a CPBUSY# signal to the UM82C231 and is passed to the CPU as BUSY#. If during this busy period, a numeric coprocessor error CPERR# occurs it results in an internal latching of the BUSY# output and assertion of IRQ13 for a NP exception request. Latched BUSY# stays active until cleared by an I/O write cycle to address 0F0H or 0F1H. IRQ13 is cleared only when CPERR# from 80287. The 80287 is reset through the CPRST output, which can be activated by a system reset or by performing a write operation to I/O port 0F1H.

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The 80287 can operate either directly from the CPU clock or with a 33% duty cycle 1/3 the frequency of the CPU clock. The UM82C231 provides both clock, CLK2 and CPCLK, to the 80287.

6.6 System Control Logic

The UM82C231 activates bus swapping control signal SWAP to the UM82C232 to guide the data bus flow during AT bus accessing and high low data byte swapping is required. Other control signals ALE, ATMW#, ATMW#, ATMR#, SMWR#, SMRD#, IOWR#, IORD# , CMD#, IOCMD# and RD# are provided for AT bus interfacing and controlling.

6.7 DRAM & EPROM Control Logic

The DRAM and EPROM control logic in the UM82C231 is responsible for the generation of the RAS#, CAS# and DWE# signals for DRAM accessed and ROMCS# for EPROM accesses. This sub-module also generates READY# to the CPU upon completion of the desired local memory operation. The appropriate number of wait states are inserted, as programmed by strap pins externally.

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7. Electrical Characteristics (Vcc=4.75~5.25V, TA=0°C-70°C)

7.1 DC Characteristics

Parameters	Symbol	Min.	Max.	Units
Input Low Voltage	Vil	-	0.8	V
Input High Voltage	Vih	2.0	-	V
Output Low Voltage	Vol	-	0.45	V
Output High Voltage	Voh	2.4V	-	V
Input Current	Iil	-	+-10	ua
Power Supply Current	Icc	-	100-	ma
Output High-Z Current	Ioz	-	+-10	ua
Standby Power Supply Current	Iccsb	-	1	ma

7.2 AC Characteristics

Symbol	Description	MIN	TYP	MAX	UNIT
t1	$\overline{RAS}$ active from CLK2↓	8	14	19	ns
t2	$\overline{RAS}$ inactive from CLK2↓	10	19	25	ns
t3	Column address valid from CLK2↑	8	15	20	ns
t4	Column address invalid from CLK2↑	9	18	24	ns
t5	$\overline{CAS}$ active from CLK2↓	8	14	19	ns
t6	$\overline{CAS}$ inactive from CLK2↓	10	19	25	ns
t7	$\overline{RDY}$ active from CLK2↓	11	20	30	ns
t8	$\overline{RDY}$ inactive from CLK2↓	13	22	32	ns
t9	$\overline{WE}$ active from CLK2↓	8	15	20	ns
t10	$\overline{WE}$ inactive from CLK2↑	9	16	21	ns
t11	$\overline{ROMCS}$ active from CLK2↓	8	15	20	ns
t12	$\overline{ROMCS}$ inactive from CLK2↓	9	16	21	ns
t13	$\overline{RAS}$ active from $\overline{ATMR}$↓	6	10	17	ns
t14	$\overline{RAS}$ inactive from $\overline{ATMR}$↑	7	12	19	ns
t15	ROW address hold time from $\overline{RAS}$↓		1		CLK2
t16	Column address hold time from $\overline{ATMR}$↑	6	10	17	ns
t17	Column address setup time from $\overline{CAS}$↓	0.5		1	CLK2
t18	$\overline{CAS}$ inactive from $\overline{ATMR}$↑	6	10	17	ns

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Symbol	Description	MIN	TYP	MAX	UNIT
t19	ALE active delay from ATCLK ↓	0	4	8	ns
t20	ALE inactive delay from ATCLK ↓	0	4	8	ns
t21	COMMAND active delay from ATCLK ↓	0	4	8	ns
t22	COMMAND inactive delay from ATCLK ↓	0	4	8	ns
t23	$\overline{M16}$ set-up time to ATCLK ↑	10			ns
t24	$\overline{M16}$ hold time to ATCLK ↑	4			ns
t25	$\overline{IO16}$ set-up time to ATCLK ↓	10			ns
t26	$\overline{IO16}$ hold time to ATCLK ↓	8			ns
t27	$\overline{NOWS}$ set-yp time to ATCLK ↑	8			ns
t28	$\overline{NOWS}$ hold time to ATCLK ↑	10			ns
t29	IOCHROY set-yp time to ATCLK ↑	10			ns
t30	IOCHROY hold time to ATCLK ↑	4	6	12	ns
t31	CPURST active delay from CLK20 ↓	2	6	16	ns
t32	CPURST inactive delay from CLK20 ↓	2	6	12	ns
t33	SYSRST active delay from CLK20 ↓	2	6	16	ns
t34	SYSRST inactive delay from CLK20 ↓	2			ns
t35	$\overline{READY}$ input set up from CLK20 ↓	12			ns
t36	$\overline{READY}$ input hold from CLK20 ↓	8			ns
t37	HOLD active delay from ATCLK ↑	2	4	8	ns

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Symbol	Description	MIN	TYP	MAX	UNIT
t38	HOLD inactive delay from ATCLK ↓	2	4	8	ns
t39	$\overline{\text{RFSH}}$ delay from HLDAI	3	7	14	ns
t40	$\overline{\text{RFSH}}$ inactive delsy from ATCLK ↑	2	4	8	ns
t41	$\overline{\text{ATMR}}$ active delay from ATCLK ↑	1	5	9	ns
t42	$\overline{\text{ATMR}}$ inactive delay from ATCLK ↓	2	4	6	ns
t43	HRQ set-yp time to ATCLK ↑	10			ns
t44	HRQ hold time to ATCLK ↑	4			ns
t45	HLDAO active delay from HLDAI	5	9	18	ns
t46	HLDAO inactive delay from HLDAI	5	10	20	ns
t47	overlap of $\overline{\text{CPBUSY}}$ & $\overline{\text{CPERR}}$	8			ns
t48	$\overline{\text{CPBUSY}}$ active pulse	12			ns
t49	IRQ13 active delay from $\overline{\text{CPBUSY}}$, $\overline{\text{CPERR}}$	7	12	16	ns
t50	IRQ13 inactive delay from $\overline{\text{CPERR}}$	3	7	11	ns
t51	$\overline{\text{BUSY}}$ active delay from $\overline{\text{CPBUSY}}$ ↓	4	8	16	ns
t52	$\overline{\text{BUSY}}$ inactive delay from $\overline{\text{CPBUSY}}$ ↑	4	8	16	ns
t53	CPRST active delay from $\overline{\text{ATIOW}}$ ↓	2	5	10	ns
t54	CPRST inactive delay from $\overline{\text{ATIOW}}$ ↑	2	5	10	ns
t55	REFRESH address valid from $\overline{\text{REF}}$ ↓	7	10	15	ns

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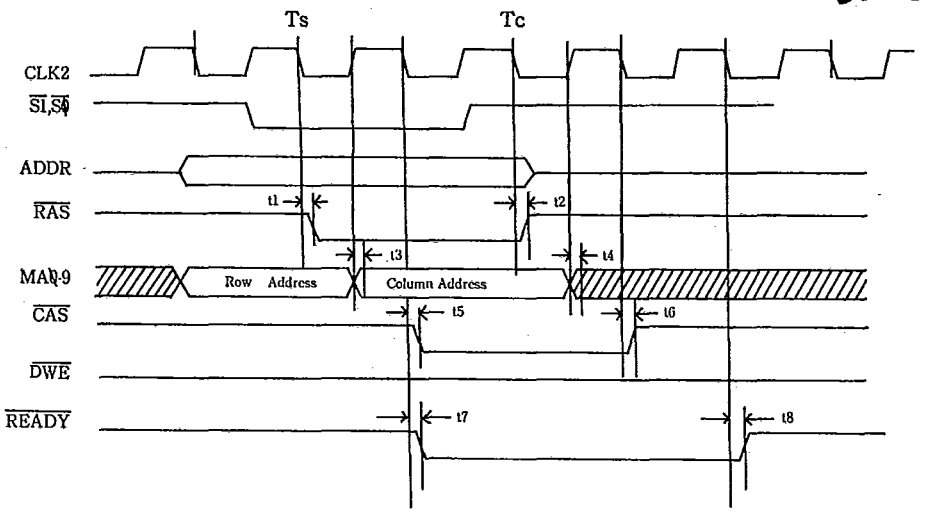
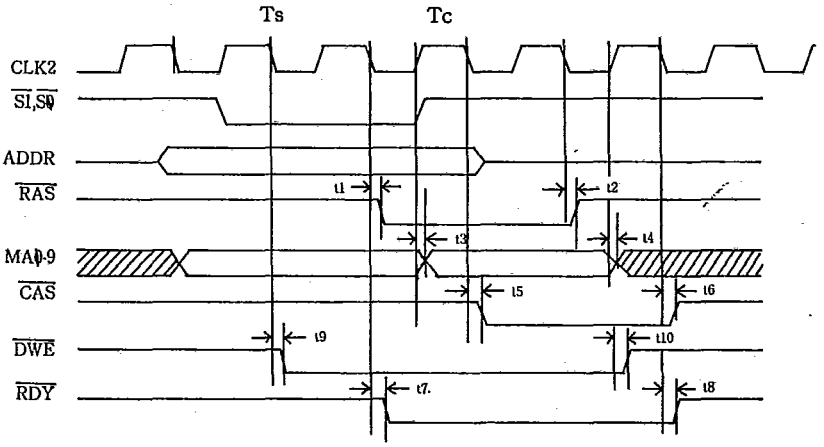


0 W.S. Read



0 W.S. Write

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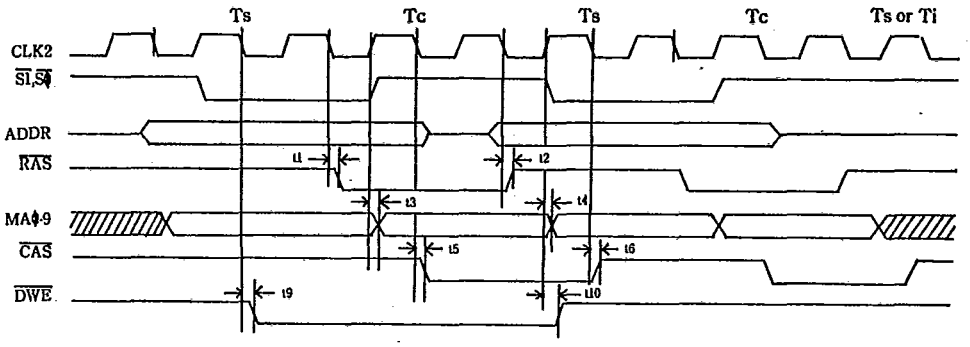
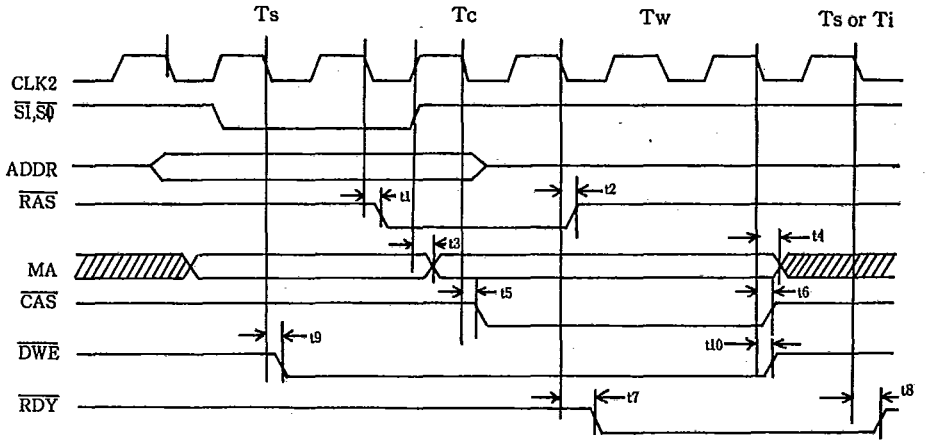


Read after Write 0 W.S.



1 W.S. Read/Write

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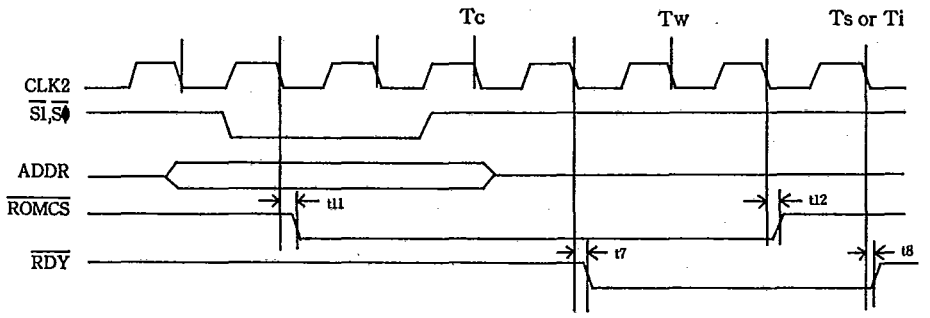
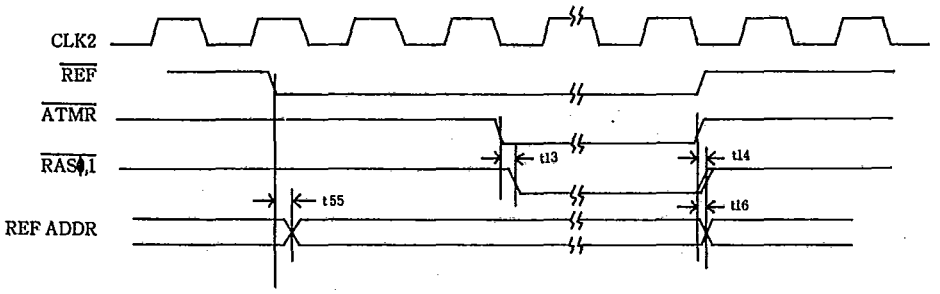


ROM Cycle



Refresh Cycle

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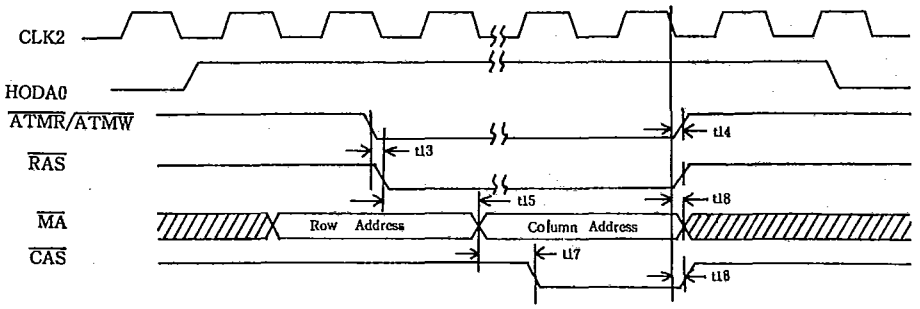
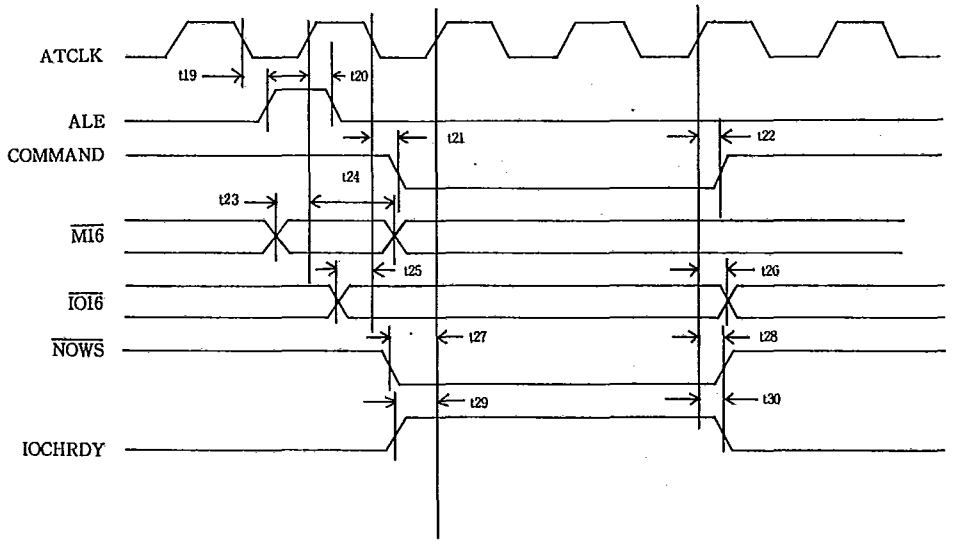


DMA Cycle



AT BUS TIMING

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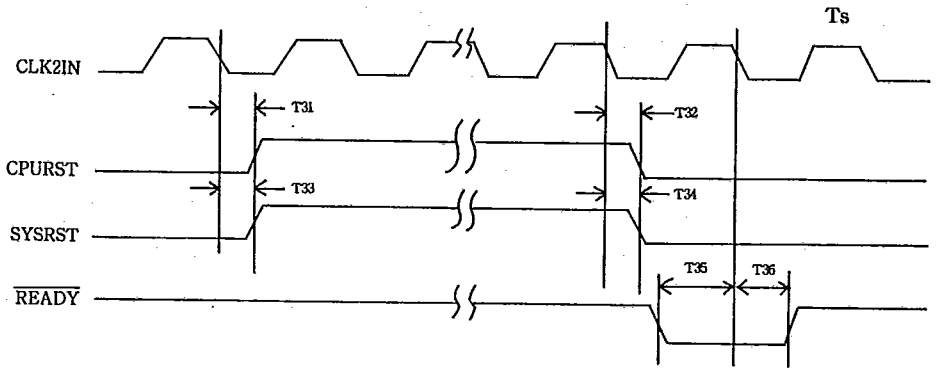
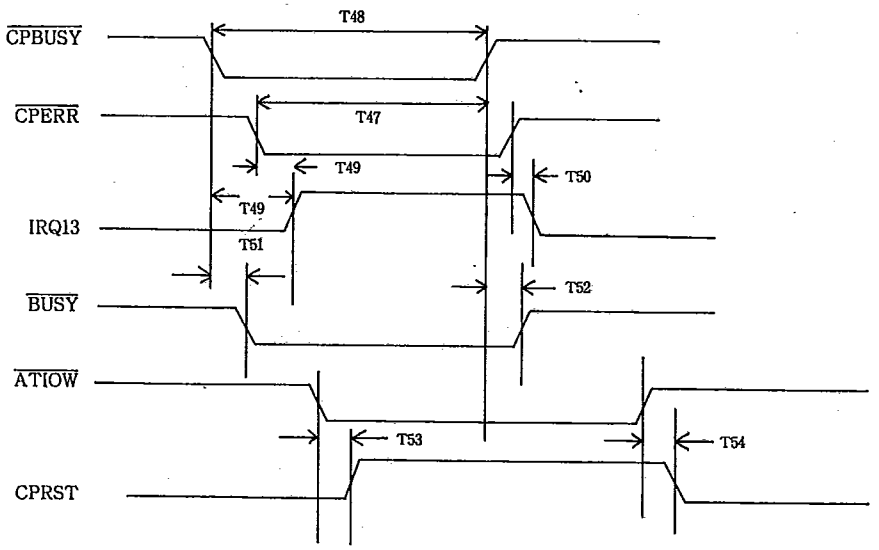


RESET & $\overline{\text{READY}}$ TIMING



COPROCESSOR SIGNALS TIMING

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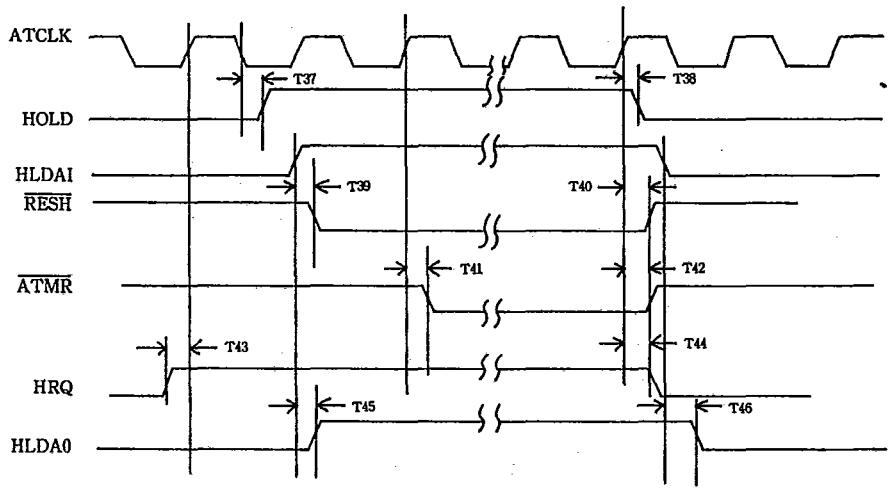

ARBITRATION SIGNALS' TIMING

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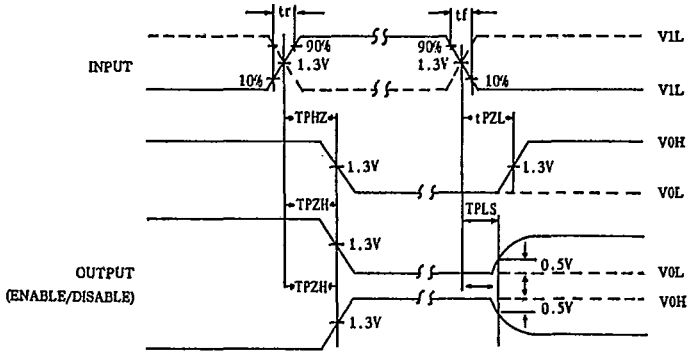
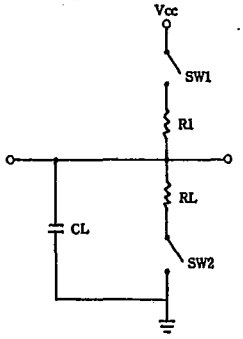
7.3 Testing Conditions

Load Circuit Measurerrient Conditions

Parameter	Output Type	Symbol	CL(pF)	Rt(Ω)	RL(Ω)	SW1	SW2
Propagation Delay Time	Totem pole 3-state Bidirectional	t_{PLH} t_{PHL}	50	—	1.0K	OFF	ON
Propagation Delay Time	Open drain or Open Collector	t_{PLH} t_{PHL}	50	0.5K	—	ON	OFF
Disable Time	3-state Bidirectional	t_{PLZ} t_{PHZ}	5	0.5K	1.0K	ON OFF	ON
Enable Time	3-state Bidirectional	t_{PLZ} t_{PHZ}	50	—	1.0K	ON OFF	ON ON



V_{IH}=3V, V_{IL}=0V, tr≤10ns, tf≤5ns



PC Mainboard