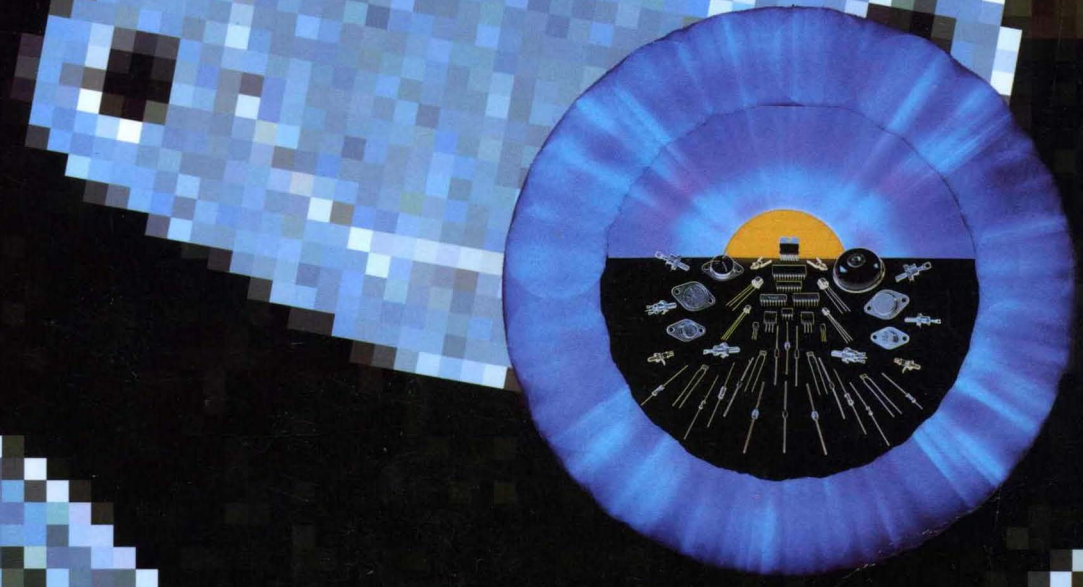
Applications HANDBOOK

A200

1987–1988



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Unitrode Applications HANDBOOK 1987–1988

Unitrode
Applications Handbook
1987-88

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TABLE OF CONTENTS

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SWITCHING REGULATOR DESIGN GUIDE

I. The Advantages of the Switching Regulator

Unlike conventional "dissipative" series or shunt regulators, in which the power-regulating transistor operates in a continuous-conduction mode, dissipating large amounts of power at high load currents – especially when the input-output voltage difference is large – the switching regulator has high efficiency under all input and output conditions. Furthermore, since the power-transistor "switch" is always either cut off or saturated (except for a very brief transition between those two states), the switching regulator can achieve good regulation despite large changes in input voltage, and maintains high efficiency over wide ranges in load current.

Because the switching regulator regulates by varying the ON-OFF duty cycle of the power-transistor switch, and the switching frequency can be made very much higher than the line frequency, the filtering elements used in the power supply can be made small, lightweight, low in cost, and very efficient – i.e., with almost negligible power losses. It is possible to drive the switching regulator with very poorly filtered DC (in fact, in high-power applications, three-phase rectification *without* filtering of any kind is often used to develop the input DC from the power line), thereby eliminating large and expensive line-frequency filtering elements.

Finally, it is possible to design switching regulators with excellent load-transient properties, so that step increases of load current cause relatively small instantaneous changes in output voltage, recovery from which is essentially completed in a few hundred microseconds.

The switching regulator has become increasingly popular in new-equipment designs, not only in aerospace and defense applications, but in computers, industrial process control systems, instrumentation, and communication.

Compared to the dissipative regulator, the switching regulator does have some disadvantages which preclude its use in some applications. The primary power source delivers current to the switching regulator in pulses which, for efficiency reasons, have short rise and fall times. In those applications where a significant series impedance appears between the supply and the regulator, the rapid changes in current can generate considerable noise. This problem can be reduced by reducing the series impedance, increasing the switching time, or by filtering the input to the regulator.

A second problem of the switching regulator, compared to the dissipative regulator, is its response time to rapid changes in load current. The switching regulator will reach a new equilibrium only when the average inductor current reaches its new steady-state value. In order to make this time short, it is advantageous to use low inductor values, or else to use a large difference between the input and output voltage.

Improved circuits for controlling switching regulators have been developed at Unitrode, thereby eliminating some earlier design constraints and optimizing the performance attainable with available hardware. These new circuits permit taking full advantage of the economy and efficiency of the Unitrode PIC600 Series Hybrid Power Switch.

The design approach used herein is believed to be original, and to be clearly superior to earlier methods of calculating the key parameters and designing the power inductor . . . yielding explicit, accurate results in significantly less time than the approximate equations in common use.

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II. The Switching Regulator Described and Characterized

The basic configuration of a switching regulator is shown in Figure 1. It accepts a DC voltage input, Ein, and regulates a DC ouput voltage, Eo, despite variations in Ein and load current. Although the static regulation, dynamic regulation, and ripple rejection of this type of regulator cannot be as easily optimized as they can in a continuous (so-called "dissipative") series regulator, its efficiency, power density (Watts output per cubic inch) and economy are all markedly superior to the series regulator . . . particularly for low-voltage, high-current supplies. Unlike a series regulator, it maintains high efficiency with high input voltages. Switching regulators can thus be employed with high efficiency to derive low voltage outputs from a high voltage unregulated supply.

All of these advantages derive from the method of regulating the output voltage: *by varying the duty cycle of a power-transistor switch,* rather than varying the voltage drop across a power transistor operating in the linear mode. Because the switch (Q1 in Figure 1) is always in the saturated state when it is conducting, and is otherwise completely non-conducting (except for a brief commutation time between the ON and OFF states), the power dissipated in the regulator is much lower than it would be in a series regulator for the same input and output conditions.

The basic switching regulator circuit functions as follows:

The control circuit causes transistor switch, Q1, to switch on and off at a predetermined frequency, f. During the time that Q1 is on, t_{on}, the input voltage, Ein, is applied to the input of the LC filter, causing current i_1 to increase. When Q1 is off, the energy stored in the inductor, L, maintains current flow to the load, circulating through "catch" diode D1. The input of the LC filter is now at zero Volts, i_1 decreases to its original value and the cycle repeats.

The output voltage, Eo, will equal the time average of the voltage at the input of the LC filter:

$$Eo = Ein\ t_{on}/\tau$$

where: $\tau = 1/f$

The control circuit senses and regulates Eo by controlling the duty cycle, $\alpha = t_{on}/\tau$. If Ein increases, the control circuit will cause a corresponding reduction in the duty cycle, α, so as to maintain a constant Eo.

$$Eo = \alpha\ Ein$$

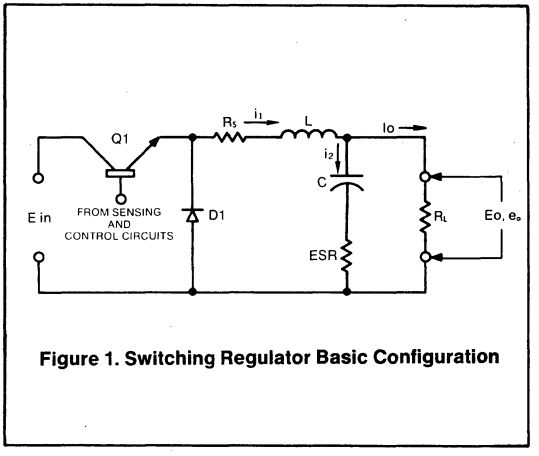
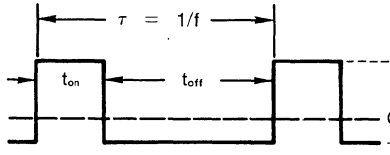


Figure 1. Switching Regulator Basic Configuration

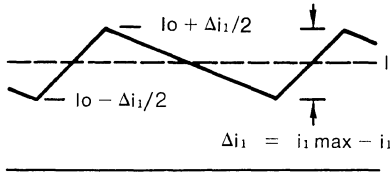
Figure 2a
V_L



$$t_{on} = \tau \frac{Eo}{Ein}$$

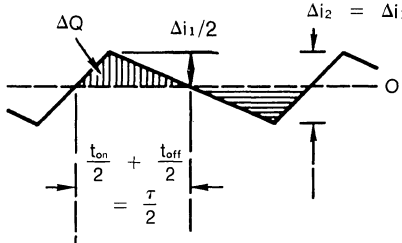
$$t_{off} = \tau - t_{on} = \tau\left(1 - \frac{Eo}{Ein}\right) = \frac{1}{f}\left(1 - \frac{Eo}{Ein}\right)$$

Figure 2b
i_1



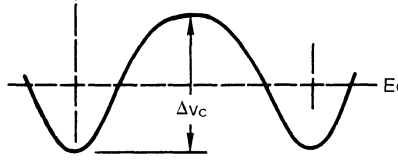
$$\Delta i_1 = \frac{Ein - Eo}{L} t_{on} = \frac{Eo}{L} t_{off}$$

Figure 2c
i_2



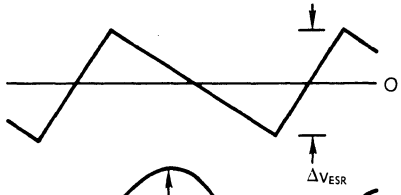
$$i_2 = i_1 - Io \quad ; \quad \Delta i_2 = \Delta i_1$$

Figure 2d
v_c



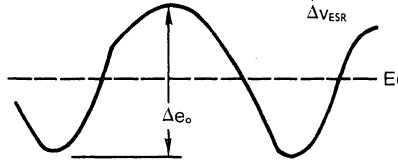
$$\Delta v_C = \frac{\Delta Q}{C} = \frac{\frac{1}{2} \cdot \frac{\Delta i_1}{2} \cdot \frac{\tau}{2}}{C} = \frac{\Delta i_1}{8fC}$$

Figure 2e
v_{ESR}



$$\Delta v_{ESR} = \Delta i_1 \cdot ESR$$

Figure 2f
e_o



$$e_o = v_C + v_{ESR}$$

$$\Delta e_o \simeq \Delta v_C \text{ OR } \Delta v_{ESR}, \text{ whichever is greater.}$$

NOTE: See Appendix A for rigorous analysis and justification

Figure 2. Switching Regulator Waveforms

Figure 2 shows some of the important waveforms and equations which define the operation of the switching regulator power circuit. The following discussion is based on several simplifying assumptions which are explained and justified or corrected in Appendix A. The most significant assumptions are to neglect the saturation voltage of Q1, the forward drop of D1, and the series loss resistance, R_S, of the inductor, L.

Figure 2a shows the voltage across inductor, L, which equals (Ein − Eo) during t_{on} and (−Eo) during t_{off}. Under equilibrium conditions, when output load current, Io, is constant, the average voltage across L must, by definition, equal zero.

Figure 2b shows the current i_1 through the inductor. Under equilibrium output current conditions, the increase in current during t_{on}, Δi_1, must equal the decrease in current during t_{off}. The average value of i_1 equals the output current, Io.

Figure 2c shows current i_2 through the capacitor, which is equal to (i_1 − Io). The average value of $i_2 = 0$, and $\Delta i_2 = \Delta i_1$. Current i_2 causes a ripple voltage to appear at the output. The output ripple voltage, e_o, has two components, a capacitive component, v_C, and a resistive component, v_{ESR}, caused by the equivalent series resistance of the capacitor.

Figure 2d shows the capacitive component, v_C, of the ripple voltage, which is the time integral of the capacitor current, i_2. Note that v_C is the integral of a triangular wave, and is not sinusoidal. Also note that v_C is in "quadrature" with i_2, in the sense that v_C min and v_C max occur at times A and B, midway in the t_{on} and t_{off} intervals, when i_2 is zero. The total charge, ΔQ flowing into C is computed graphically by finding the area of the triangular current waveform between time A and time B (Area = ½ bh; $\Delta Q = ½ \times \tau/2 \times \Delta i_2/2$). The peak to peak capacitive ripple component $\Delta v_C = \Delta Q/C = \Delta i_1/8fC$. (The factor 8f for a triangular current waveform is comparable to $2\pi f$ for a sinusoidal input current.)

Figure 2e shows the resistive component, v_{ESR}, of the ripple voltage which simply equals $i_2 \times$ ESR, and is in phase with i_2.

Figure 2f, the total output ripple voltage, e_o, is the sum of the waveforms in Figures 2d and 2e. Note that since v_C and v_{ESR} are in quadrature, the greater of these two components dominates, and for all practical purposes the peak to peak output ripple voltage, Δe_o, is equal to either Δv_C or Δv_{ESR} whichever is greater.

The magnitude of v_{ESR} in comparison with v_C shown in these waveforms is not exaggerated. Indeed, when designing a switching regulator to operate at frequencies greater than 20 kHz in order to achieve small size and low cost in the L and C filter elements, the ESR of the capacitor usually dominates completely. Even when high quality capacitors (low ESR) are employed, it is usually necessary to use a larger capacitance value than would otherwise be required in order to realize the ESR required to achieve the ripple objective of the design.

With conventional free running switching regulator control circuits, capacitor ESR also causes very significant departure from the design frequency, which can result in large ripple magnitude, inductor saturation, and switching transistor failure. In the circuits developed at Unitrode and presented in the next section, the frequency-variation effect caused by ESR is effectively eliminated, leaving only the ripple consideration.

Detailed design considerations for switching regulator power circuits are contained in Section IV.

III. Applications Circuits for Switching Regulators

The design and performance of conventional switching regulators are usually dominated by the ESR of the output capacitor. However, in the group of circuits described in this section, the following parametric relationships and circuit characteristics are easily and economically attained:

- The switching frequency may be selected and established at the optimum value for the switching components, and *will be independent of the value of the ESR of the output capacitor.*
- The value of t_{off} is held relatively constant, over wide ranges of load current and input voltage, and independent of the ESR of the output capacitor. Constant t_{off} results in constant ripple current and output ripple voltage.
- Settable overcurrent limiting is provided, thereby protecting both the load and the switching transistors under all conditions, and preventing saturation of the power inductor during the startup transient period, thereby minimizing startup overshoot.
- The overcurrent limiting circuit is significantly lower in dissipation than conventional current-limit-feedback arrangements.
- The drive current to the power output (switch) stage is regulated to a pre-determined value, for best efficiency and optimum switching speed. Drive current is automatically increased at low temperatures and decreased at high temperatures, thereby maintaining optimum drive conditions for the power switch.

Note that, although the use of this circuit approach permits essentially constant "t_{off}" operation even with capacitors having relatively high ESR, the output ripple voltage is increased by high ESR. (If the ripple developed across ESR is significantly larger than that developed across C, then the ripple is essentially proportional to ESR.)

Not all of the circuits that follow have all of the virtues listed above, but the exceptions will be noted. Figure 3 typifies this family of regulators. It is shown implemented by the popular LM305 regulator IC, and a Unitrode Series PIC600 Hybrid Power Switch, comprising a quasi-Darlington switching transistor, a fast recovery catch diode, and transistor bias resistors, all matched for optimum efficiency and switching speed (up to 100 kHz without derating). The configuration of Figure 3 is a *positive* output regulator, with performance characteristics as follows:

Ein = 20 to 40V

Eo = 5V ± 1%

Δe_o = 100 mV p-p (2% p-p ripple)

Io = 2 to 10A

Isc = 12A

Regulation versus Ein (20 to 40V) <25 mV

Transient Recovery Time for step change in load current from 2A to 10A, or 10A to 2A <150 μsec.

f = 50 kHz nominal

Efficiency >70%

The circuit of Figure 3 operates in the fixed-off-time mode; hence, output ripple is independent of input voltage over wide ranges. In this circuit, two feedback signal paths are provided:

- *DC Feedback.* A fraction of the DC output voltage, Eo, is fed back to the inverting input of the LM305 through voltage divider R1, R2. The DC voltage at the inverting input is compared to a reference voltage (approximately 1.8V) within the LM305, and the LM305 regulates Eo so that the voltage fed back to the inverting input is essentially equal to the built in reference voltage. The R1, R2 divider ratio therefore establishes the level of the DC output voltage, Eo. Resistor R5 improves output voltage regulation versus input voltage changes by feeding a small compensating voltage proportional to the input voltage into the inverting input of the LM305.

- *AC Feedback.* Capacitor C1 feeds back an AC voltage waveform to the inverting input of the LM305. This voltage is proportional to the output ripple voltage plus the AC voltage developed across R_I, $\Delta e_o + \Delta v_{RI}$.

  Capacitor C2 feeds back an AC voltage to the non-inverting input of the LM305. This voltage is proportional to the output ripple voltage plus the AC voltage across R3, $\Delta e_o + v_{R3}$.

When the circuit values are properly established, the same fraction of Δe_o is fed back to both inverting and non-inverting inputs, thereby effectively cancelling. The operation of the switching regulator is thus rendered independent of the output ripple voltage developed across the C or ESR of the output capacitor.

Since the Δe_o components cancel each other, the LM305 essentially compares Δv_{RI} at the inverting input to Δv_{R3} at the non-inverting input. Voltage Δv_{R3} is a rectangular waveform with a peak-to-peak amplitude equal to I drive × R3, where I drive is the base drive to the hybrid switching transistor provided by the LM305, and Δv_{RI} is a triangular waveform with a peak-to-peak amplitude equal to $\Delta i_1 \times R_I$, where Δi_1 is the ripple current through inductor L. When the drive current is on, Δv_{R3} is at its peak positive amplitude. As i_1 increases, v_{RI} increases proportionately. When the positive amplitude of Δv_{RI} reaches Δv_{R3}, this causes the LM305 to switch off the drive current, Δv_{R3} immediately drops to its peak negative amplitude, and i_1 starts to fall. When Δv_{RI} reaches a negative amplitude equal to Δv_{R3}, the LM305 switches the drive current back on, and the process repeats. In this manner, the LM305 controls the power switch so that Δi_1 is fixed. Since $t_{off} = \Delta i_1 \times L/Eo$, with fixed values of L and Eo, t_{off} is fixed and independent of changes in Ein or capacitor C or ESR values.

R4, connected between pins 1 and 8 of the LM305, establishes the desired level of base drive for the PIC600 Series Hybrid Power Switch, and determines the hysteresis voltage across R3.

Current-limiting action is provided by transistor Q1, the collector of which is connected to the "gate" or "inhibit" terminal of the LM305 (pin 7). When the load current is normal, Q1 is cut off and pin 7 floats; but when the voltage drop across R_I increases to a value greater than the sum of V_{BE} (Q1) and v_{R3}, Q1 turns on, cutting off the drive current from the LM305 and, ultimately, the power switch. This cutoff action is made to "latch" by the fact that, with the drive cut off, v_{R3} disappears. This keeps Q1 on, until the current through R_I drops significantly – enough to make the voltage drop across R_I fall below the V_{BE} of Q1.

The current through R_I, following such an overload cutoff action, falls linearly at the rate of Eo/L. When Q1 is cut off, drive current is restored. The circuit will then continue to switch on and off at a frequency comparable to normal operation, with the average current limited at the design limit, and power dissipation held to safe values.

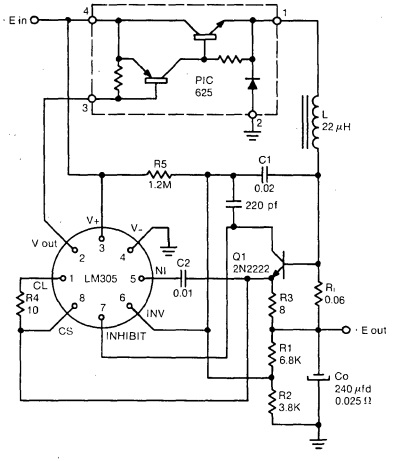


Figure 3. Positive Voltage Switching Regulator

Transient response of the switching regulator of Figure 3 is shown in Figures 4, 5, and 6.

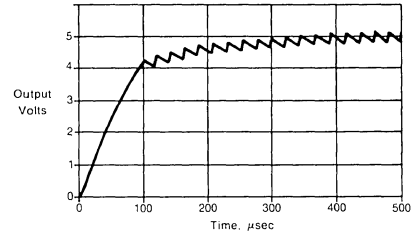


Figure 4. Ein from 0 to 25V

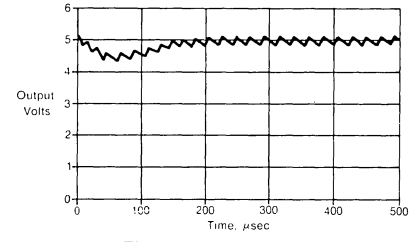


Figure 5. Io from 4A to 10A

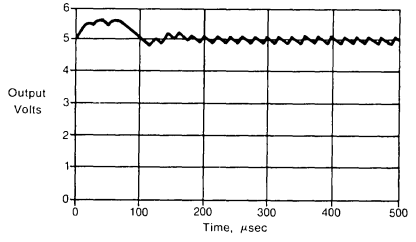


Figure 6. Io from 10A to 4A

It is usually necessary to employ a noise filtering capacitor across the input of any switching regulator. This functions to prevent the steep waveform of the rectangular current pulse associated with the power switch turning on and off from propagating into the Ein supply line. The capacitance value required is a function of the impedance characteristics of the Ein supply and intervening wiring. Watch out for underdamped resonance with the inductance of the input wiring, or transient induced ringing may occur. The input capacitor must have short leads, and the ground side should preferably be connected directly to the ground side of the output filter capacitor.

A 10A negative voltage switching regulator, utilizing an LM304 and PIC600 series, is shown in Figure 7.

A reference voltage is determined by resistor R1 and R2. The error amplifier controls the output voltage at twice the voltage across R2. Diode D1 is used to ensure a potential difference of less than 2V at the unregulated input (pin 5) with respect to the reference supply (pin 3). (If the unregulated supply terminal gets more than 2V positive with respect to reference supply, the collector isolation junction of transistor Q6 of LM304 becomes forward biased and disrupts the reference.)

Current limiting is achieved, in Figure 7, by means of reducing the reference voltage to ground with the help of transistor Q1 and resistor R8, instead of turning off the base drive to the power output switch as in Figure 3.

The functions of the rest of the components and the operation of the switching regulator are the same as described for Figure 3.

A positive switching regulator using a μA723 is shown in Figure 8.

The basic performance and circuit operation is the same as Figure 3.

The circuit shown in Figure 9 is a high voltage positive switching regulator. Because the LM305 (like almost all IC regulators) cannot be operated at supply voltage in excess of 40V, this circuit uses a fraction of Ein as a power supply for the IC circuit by means of zener diode and current limiting resistor R9. The voltage isolation between LM305 and power switch, and the regulated base drive to the power switch are provided by transistor Q2.

The basic operation of the circuit and design approach is the same as that of a low voltage positive switching regulator.

The circuit shown in Figure 10 is a negative high voltage switching regulator.

This circuit is similar to the low voltage negative switching regulator with a minor modification. Transistor Q2, resistor R10 and R11 are all used to provide regulated base drive to the power output stage and also to provide the voltage isolation between power output stage and LM305. The resistor R9 is used to limit current through zener diode under steady state and startup conditions.

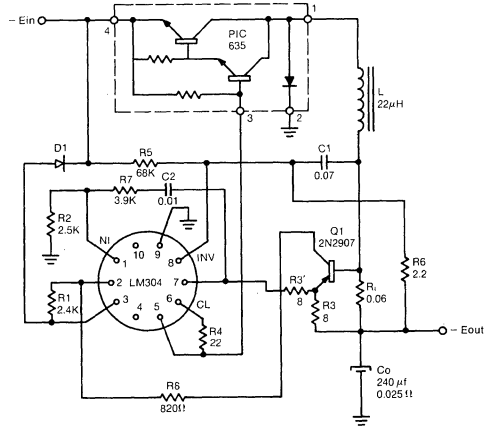


Figure 7. Negative Voltage Switching Regulator

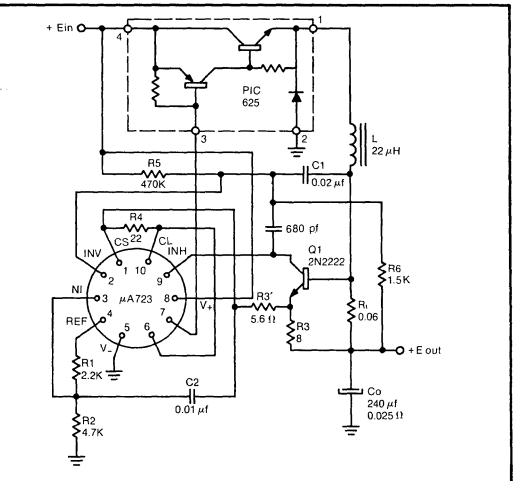


Figure 8. Positive Voltage Switching Regulator

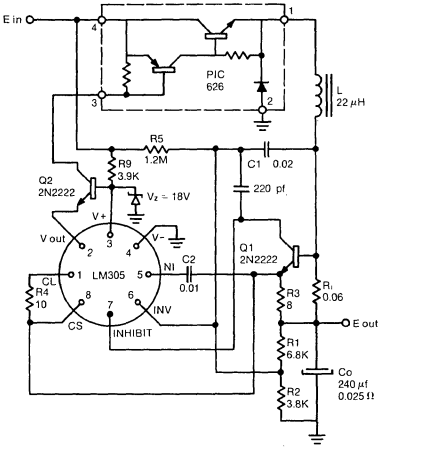


Figure 9. High Voltage Positive Switching Regulator

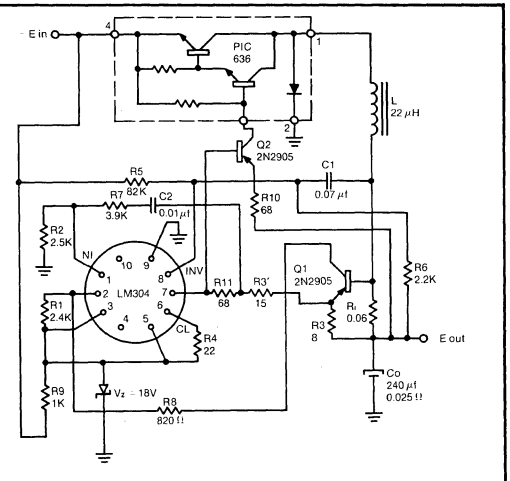


Figure 10. High Voltage Negative Switching Regulator

IV. Designing the Power Circuit

In designing a switching regulator power supply, the following parameters will normally be predefined. Specific values shown for each parameter will be used as the basis for a design example:

Eo = 5V Output Voltage

Δe_o = 100 mV Output Ripple Voltage, Peak to Peak

Io max = 10A Output Current, Full Load

Io min = 2A Output Current, Minimum Load

Ein max = 40V Input Voltage, Maximum

Ein min = 20V Input Voltage, Minimum

The first step in the design is to decide on the operating frequency of the switching regulator. No concrete rules can be given for this decision.

High frequency operation is distinctly advantageous in that the cost, weight and volume of both L and C filter elements are reduced. However, above the frequency where the capacitor ESR exceeds its capacitive reactance, no further reduction in capacitor size or cost will occur. This frequency, in the range of 1-50 kHz, depends upon the "quality" of the capacitor in terms of ESR. Above this frequency, the inductor will continue to diminish in size and cost, although when the inductor reaches a very small size, cost will level off.

Operation above 20 kHz is desirable to eliminate the possibility of audio noise.

The main factor limiting high frequency operation is the drop in efficiency caused by switching losses in the power switching transistor and "catch" diode. The higher cost of these fast switching semiconductors required to operate efficiently at high frequencies must be weighed against the reduced cost, size and weight of the L and C components to arrive at the optimum frequency for any specific application. It may be desirable to work the design through at several frequencies in order to make a decision.

In the specific application defined at the beginning of this section, the power output (Eo × Io max) is 50W.

Referring to the specification for the Unitrode PIC 625/635 Hybrid Power Switch, the DC losses (Transistor V_{CEsat}, Diode V_F) under the conditions of this application amount to 10W. The following tabulation shows the switching losses and overall efficiency at several frequencies.

Frequency	**1 kHz**	**20 kHz**	**50 kHz**	**100 kHz**
Power output	50	50	50	50
DC losses	10	10	10	10
Switching losses	0.05	1	2.5	5
Total power input	60.05	61	62.5	65
Realizable efficiency	83.3%	82%	80%	77%

For our example, we will choose a frequency of 50 kHz, even though the efficiency is not significantly reduced at 100 kHz. At 100 kHz most currently available tantalum and aluminum electrolytic capacitors begin to exhibit series inductance.

Transistors and diodes which do not have the fast switching capabilities of the PIC 625/635 will become efficiency limited at much lower frequencies. Note that in this specific application, a dissipative regulator design will incur power losses in the series transistor of 350W, resulting in an efficiency of 12.5 percent!

The control circuits shown in the previous section control the on-off switching periods by sensing and controlling the ripple current, Δi_1, through the inductor L. This mode of operation results in a constant ripple current and (assuming Eo and L are fixed) constant off time, t_{off}, independent of input voltage. The relationship between t_{off}, f, Eo, and Ein is as follows (from Figure 2a):

$$t_{off} = (1 - Eo/Ein) / f$$

With t_{off} and Eo fixed by the control circuit, f will change when Ein changes, and f will be maximum when Ein is maximum. In our specific example,

f max = 50 kHz

Ein max = 40 V

Eo = 5V

so that:

$$t_{off} = (1 - 5/40) / 50{,}000 = 17.5\,\mu sec$$

Now, with t_{off} fixed at 17.5 μsec, if Ein changes to Ein min = 20V,

$$f_{min} = \frac{(1 - Eo/Ein)}{t_{off}} = \frac{(1 - 5/20)}{17.5 \times 10^{-6}} = 43\ kHz$$

The fact that the frequency changes slightly with Ein is really not important, as stated earlier, because constant t_{off} operation results in more constant output ripple than constant frequency operation.

Having determined (or assumed) the maximum operating frequency and calculated t_{off}, we next proceed to find specific values for L and C. L and C together form a low pass filter which reduces the rectangular waveform at the filter input to a DC output voltage, Eo, with a small amount of ripple, Δe_o, superimposed. To achieve a specified Δe_o requires a specific LC product, independent of load current. Theoretically, this LC product can be achieved with any L/C ratio – small L and large C, or large L and small C (or very large L and no C at all, using instead the load resistance R_L as one element of an L/R filter). There are, however, several practical economic and performance considerations that apply to selecting specific L and C values.

It is favorable to push in the direction of small L and large C for the following reasons:

1. Under the power and frequency ranges commonly encountered in switching regulator circuits, it costs more to store energy in an inductor than in a capacitor. Also, an inductor will have considerably greater weight and volume than a capacitor with equal energy storage capacity. Small L and large C, within the limits defined below, will usually result in the lowest cost, weight and size design.
2. Small L and large C results in low "surge impedance" of the filter, hence better transient behavior with step changes in load current.
3. Losses in a practical inductor are higher than in a capacitor with equal energy storage capacity (assuming low ESR). This again argues for small L, large C.

One major objection to a low L/C ratio is that it causes large and sometimes intolerable overshoot in input current and output voltage on startup, when the circuit is first energized. Input current overshoot can saturate the inductor and destroy the switching transistor. The current limiting feature of the applications circuits shown in Section III effectively controls the startup transient, thereby protecting all components and minimizing voltage overshoot. With current limiting, this problem is eliminated and no longer pertains to the selection of L and C values.

Referring to Figure 2b and its associated equations, the peak-to-peak ripple current through the inductor, Δi_1, is inversely proportional to the inductance, L. As L is made smaller, Δi_1 increases. Maximum limits on Δi_1 determine how small L is permitted to be, as follows:

1. The instantaneous current through L ranges between a maximum of Io + $\Delta i_1/2$ and a minimum of Io − $\Delta i_1/2$. If $\Delta i_1/2$ is permitted to become larger than Io, the minimum inductor current becomes a negative value. This is impossible, since neither the switching transistor nor the "catch" diode will conduct. Therefore, the switching regulator goes into a discontinuous mode of operation which is perfectly safe, but the frequency changes considerably and regulation with output current changes becomes relatively poor. The worst case consideration to insure that discontinuous operation does not occur is to make $\Delta i_1/2$ equal to the *minimum* load output current, Io min, or $\Delta i_1 = 2$ Io min.

   It is not practical to apply this criterion if Io min is very small (<0.05 Io max) because Δi_1 would then be very small, forcing an impractically large L value. In applications

where Io min is very small, there are two alternatives: (a) raise Io min by preloading the supply, or (b) make $\Delta i_1 = 2(0.05$ Io max$) = 0.1$ Io max realizing that when Io becomes less than 0.05 Io max, the discontinuous mode will occur.

2. The maximum peak current is equal to the full load current, Io max $+ \Delta i_1/2$. As L is decreased, the corresponding increase in Δi_1 will begin to cause a significant increase in the maximum peak current. Since the inductor must be designed not to saturate at the maximum peak current, this begins to negate the cost, size and weight advantages of making the L value smaller. Higher peak currents will have an adverse effect on efficiency and transistor drive requirements, and may require transistor and "catch" diodes with higher current ratings (and higher cost). It is, therefore, recommended that $\Delta i_1/2$ be no greater than 0.25 Io max, which will limit the maximum peak current to 1.25 Io max, or Δi_1 max = 0.5 Io max.

In summary:

Δi_1 = 2 Io min, within the following somewhat arbitrary limits:

Δi_1 min = 0.1 Io max

Δi_1 max = 0.5 Io max

In our example, Io min = 2A, Io max = 10A. Calculating $\Delta i_1 = 2$ Io min = 4A, which is acceptable since Δi_1 max $= 0.5 \times 10A = 5A$, and Δi_1 min $= 0.1 \times 10A = 1A$.

Now that t_{off} and Δi_1 have been determined, L can be calculated as follows:

$$L = \frac{Eo \times t_{off}}{\Delta i_1} = \frac{5 \times 17.5 \times 10^{-6}}{4} = 21.9\,\mu H$$

The final step is to determine the requirements for the capacitor C and ESR values which will result in the desired output ripple voltage, Δe_o. Since the two components of Δe_o : Δv_C and Δv_{ESR}, are in "quadrature", we can consider each component separately, with a worst case error of less than 20 percent when both components are equal. This much error is highly unlikely, since the ESR component usually dominates completely when operating at high frequencies.

From Figure 2d:

$$C = \frac{\Delta i_1}{8f\,\Delta v_c}$$

note that C varies inversely with f. In order to achieve Δv_C less than the desired maximum Δe_o, the minimum value for C must be determined at the lowest frequency, f_{min}, calculated previously.

$$C\ min = \frac{\Delta i_1}{8 f_{min}\,\Delta e_o\ max} = \frac{4}{8 \times 43 \times 10^3 \times 100 \times 10^{-3}} = 114\,\mu F$$

From Figure 2e:

$$ESR\ max = \frac{\Delta v_{ESR}}{\Delta i_1} = \frac{\Delta e_o\ max}{\Delta i_1} = \frac{100 \times 10^{-3}}{4} = 0.025\Omega$$

With high frequency operation, capacitor ESR usually dominates, forcing the use of a C value much greater than C min in order not to exceed ESR max.

Subsequent sections deal with designing the inductor and selecting the capacitor and other components of the switching regulator.

V. Design of the Power Inductor

This simplified nomographic method facilitates selecting the smallest core that will achieve the desired characteristics of the power inductor. This procedure is useful in selecting the proper core and determining wire size, number of turns, copper losses, and temperature rise. It also permits investigating the effects of change in assumed initial conditions and in "trimming" the design.

A detailed analysis of this inductor design procedure is contained in Appendix B.

Tables 1 and 2 give core parameters for a variety of commonly used ferrite pot cores and Mo-Permalloy toroids. (Note: There is no significance to the selection of manufacturers, nor is any intended. Many manufacturers make roughly equivalent cores in these sizes, with similar magnetic properties.)

Ferrite and Mo-Permalloy powder are excellent core materials for the switching regulator inductor. Since the rms AC current through the inductor is small compared to the DC current, AC losses in the winding and core losses will be negligible compared with DC winding losses.

Selection of the proper core for a specific application is a process concerned with two factors: (1) The core must provide the desired inductance without saturating magnetically at the maximum peak overload current, i_1 max. In this respect each core has a specific $(LI^2)_{sat}$ energy storage capability. (2) The core must have a window area for the winding which admits the number of turns necessary to obtain the required inductance with a wire size which will result in acceptable DC losses in the winding at the full load output current, Io. Each core has a specific $(LI^2)_{diss}$ capability that will result in a specific power loss or temperature rise.

The significant core parameters are primarily core size and the magnetic gap in series with the flux path. Consider a very small (for the application) ferrite pot core with no air gap. The effective permeability, μ_e, will be very large because there is no gap. Relatively few turns will be required to achieve the desired inductance, and the power loss at Io will be small, but the core cannot store the required energy $L(i_1 \text{ max})^2$ without saturating. If we introduce a gap into this core, the energy storage capability increases (the extra energy is actually stored in the gap, not in the ferrite material). However, the gap causes the effective permeability to drop, which requires more turns of finer wire to achieve the desired inductance. If the core is too small, as the gap is increased to the point required to achieve the necessary energy storage capability without saturating, the DC resistance of the increased number of turns of finer wire has increased to the point where the power dissipation and temperature rise is too great. This conflict is resolved by going to a larger core with appropriate gap.

To facilitate core selection, Tables 1 and 2 contain tabulated values of $(LI^2)_{sat}$ energy storage capability (saturation limited) and $(LI^2)_{25C}$ capability (based on power dissipation resulting in 25°C temperature rise). These values have been calculated for various size cores with different gaps, by methods described in Appendix B. Also given in the tables are the power dissipation corresponding to a 25°C rise for each core size, and the effective window area for the winding, A_W'. Tabulated A_L values relate to different gaps. (A_L is the inductance index at a particular gap setting – defined as the inductance in mH for 1000 turns.)

The optimum cores for switching regulator inductor applications generally have quite large gaps, and consequent relatively low A_L values. This is fortuitous, since the core properties are then dependent mostly on the gap itself, and variations in the magnetic materials of the core are swamped out, resulting in excellent stability and linearity. Note, however, that in the ferrite pot core table, many of the lower A_L values are not supplied as stock items by the manufacturer, and the desired gap must be ground to size on a special order basis.

Mo-Permalloy powder cores are effectively "gapped" by the manufacturer by means of varying the amount of non-magnetic binder that holds the Mo-Permalloy particles together within the core, and by the size and shape of the Mo-Permalloy particles. Thus, the "gap" is actually distributed throughout the core material. These cores are supplied with many different A_L values in each size.

One of the main advantages of ferrite pot cores and ferrite E-I cores (not tabulated, but worth considering) is that the winding is easily formed on a bobbin which is subsequently assembled within the two-piece core assembly. Ferrite toroids are not recommended because of the practical difficulty of introducing a gap. Mo-Permalloy toroids are not as convenient to wind, but this is not a serious problem as most switching regulator inductor designs require few turns of relatively heavy wire.

Example of Inductor Design

The example shown below will illustrate the method of solution, as drawn on the nomograph of Figure 11.

Given:

$$\begin{aligned} L &= 21.9\,\mu H \\ Io &= 10A \\ i_1\,max &= 14A \text{ (current limited)} \\ Eo \times Io &= 50W \text{ (output of regulator)} \end{aligned}$$

Copper losses not to exceed 1% of output power, and temperature rise of inductor not to exceed 25°C.

Step 1: Draw line ① from Io = 10A on the "I" scale, to 0.0219 mH (21.9 μH) on the "L" scale through the "LI²" scale. Note that $LI_o^2 = 2.19$ millijoules.

Step 2: Draw line ② from i_1 max = 14A on the "I" scale to the 0.0219 mH on the "L" scale through the "LI²" scale. Note that $L(i_1\,max)^2 = 4.3$ millijoules.

Step 3: Find the smallest core in Tables 1 or 2 that has $(LI^2)_{25C}$ capability greater than LI_o^2 defined in step 1, and $(LI^2)_{sat}$ capability greater than $L(i_1max)^2$ defined in step 2. This appears to be a 2616-3B7 pot core with $A_L = 160$ from Table 1, or an A-291061-2 toroid from Table 2.

Step 4: Actual temperature rise of the core and power loss can be calculated as follows:

Temperature rise of pot core;

$$\text{Actual } \Delta T = 25°C \frac{LI_o^2 \text{ (step 1)}}{(LI^2)_{25C} \text{ from core table}}$$

$$= 25°C \times \frac{2.19}{2.288}$$

$$= 24°C$$

Power loss in inductor;

$$\text{Actual } P_W = P_{25C} \times \frac{LI_o^2}{(LI^2)_{25C}}$$

$$= 0.547 \times \frac{2.19}{2.288}\ W$$

$$= 0.524W$$

Actual power loss in the inductor as a percentage of the power output of the switching regulator is:

$$\frac{P_W \times 100\%}{Eo \times Io} = \frac{0.524 \times 100\%}{50} = 1.05\%$$

If power losses are not acceptable, then select a core with higher $(LI^2)_{25C}$ capability.

Step 5: In the nomogram, draw line ③ from 0.0219 mH on the "L" scale through $A_L = 160$ on "A_L" scale to the "N" scale. Note that 12 turns are required to obtain the desired inductance.

Step 6: Enter the $A_W' = 0.193$ from the table for the core selected on the "A_W'" scale. Draw ④ from "N" scale where N = 12 through $A_W' = 0.193$ to the "wire size" scale. From this scale, note that wire size is AWG 15.2. Select the next highest integer, AWG 16, in order to fit within the available window area. This will result in a slight increase in power loss and temperature rise.

The same procedure applies if a toroid is selected instead of a pot core.

If both the LI_o^2 and $L(i_1max)^2$ values calculated in steps 1 and 2 are less than the appropriate limiting (LI²) values for the core selected, it is suggested that the L value of the application be increased until one or the other of the core limits is reached. This will permit reduction of Δi_1, and reduce the requirements of the output capacitor.

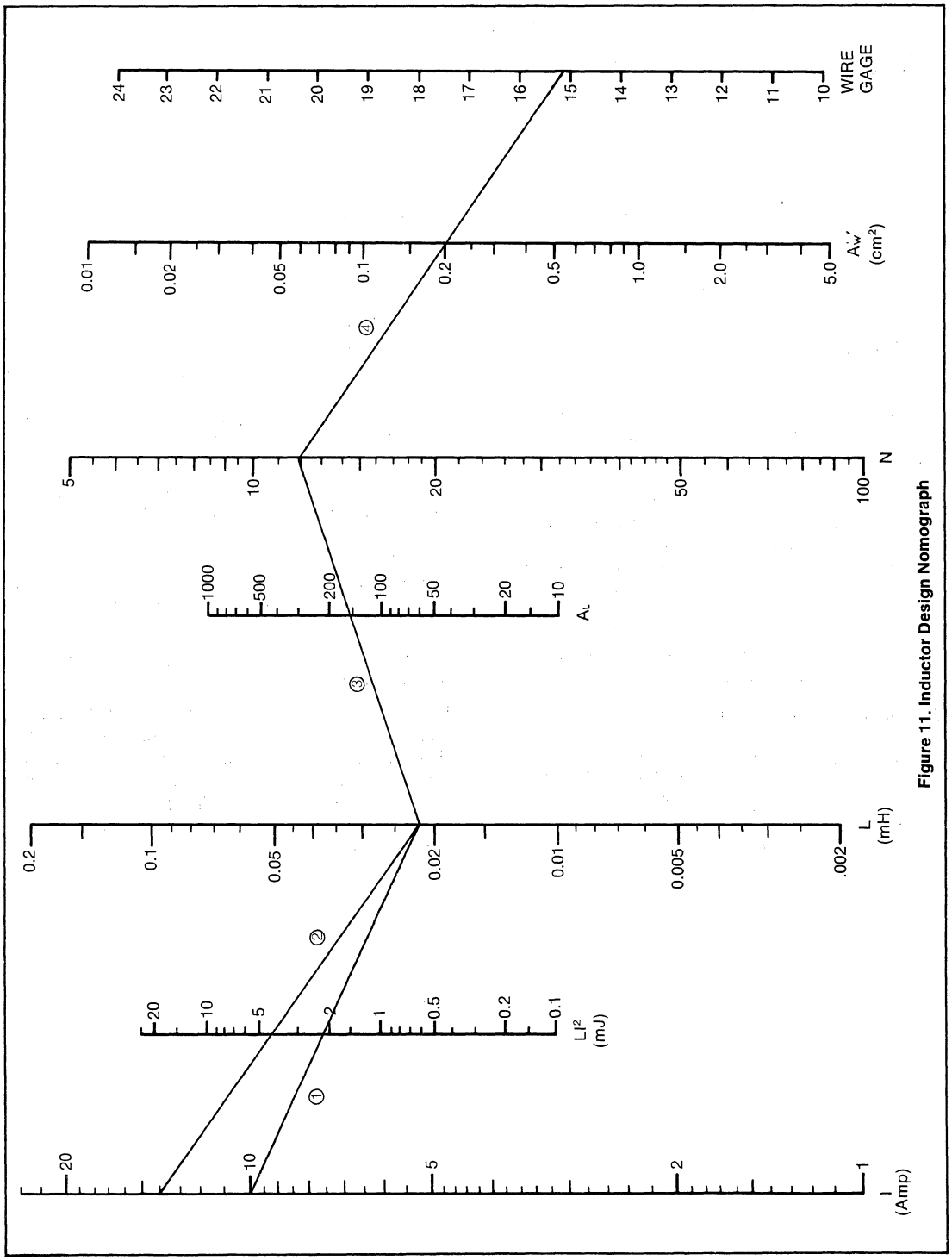


Figure 11. Inductor Design Nomograph

Table 1. Ferrite Pot Cores

Ferroxcube Part No.	Dimensions (inches)		Power Dissipation 25°C rise (watts)	Window Area 0.65 A_W (cm^2)	Inductor Index	Saturation Limit (mJ)	Dissipation Limit 25°C rise (mJ)
	(OD)	(HT)	(P_{25C})	(A_W')	(A_L)	($(LI^2)_{sat}$)	($(LI^2)_{25C}$)
1107-A100-3B7	0.445	0.264	0.100	0.034	100	0.200	0.077
1107-A160-3B7	0.445	0.264	0.100	0.034	160	0.144	0.124
1408-A100-3B7	0.559	0.334	0.158	0.063	100	0.490	0.180
1408-A160-3B7	0.559	0.334	0.158	0.063	160	0.324	0.288
1811-A160-3B7	0.716	0.428	0.259	0.122	160	1.02	0.719
2213-A160-3B7	0.858	0.538	0.358	0.193	160	2.12	1.32
2616- * -3B7	1.024	0.640	0.547	0.263	160*	5.06	2.29
2616-A250-3B7	1.024	0.640	0.547	0.263	250	3.24	3.58
3019- * -3B7	1.201	0.754	0.754	0.382	200*	8.57	4.90
3622- * -3B7	1.418	0.880	1.04	0.486	200*	18.4	7.21
4229- * -3B7	1.697	1.16	1.60	0.910	200*	31.8	17.9

*Indicates not stock item. Gap must be ground to obtain desired A_L.

Table 2. Mo-Permalloy Toroids

Arnold Part No.	Dimensions (inches)		Power Dissipation 25°C rise (watts)	Window Area 0.5 A_W (cm^2)	Inductor Index	Saturation Limit (mJ)	Dissipation Limit 25°C rise (mJ)
	(OD)	(HT)	(P_{25C})	(A_W')	(A_L)	($(LI^2)_{sat}$)	($(LI^2)_{25C}$)
A-307032-2	0.425	0.180	0.072	0.082	32	0.180	0.065
A-051027-2	0.530	0.217	0.125	0.192	27	0.296	0.199
A-189043-2	0.710	0.280	0.209	0.319	43	0.782	0.659
A-059043-2	0.930	0.330	0.346	0.703	43	1.55	2.06
A-894075-2	1.09	0.472	0.520	0.781	75	3.40	4.32
A-291061-2	1.33	0.457	0.708	1.47	61	4.54	8.97
A-298028-2	1.33	0.457	0.708	1.47	28	9.90	4.12
A-085035-2	1.60	0.605	1.04	2.14	35	20.1	8.65
A-087059-2	1.875	0.745	1.48	2.14	59	40.2	16.0

VI. Component Selection

1. *Power Switching Components*

Voltage ratings of the power switching transistor and catch diode must be greater than the maximum input voltage, Ein, including any transient voltages that may appear at the input of the switching regulator. Low transistor $V_{CE\,sat}$ and diode V_F at full load output current are important considerations to maintain high efficiency (Ref efficiency calculations – Appendix A).

Fast switching diodes and transistors are required to maintain good efficiency in high frequency switching regulators. Transistor switching losses become significant when combined rise time plus fall time exceeds approximately $0.025 \times \tau$. Thus, for 50 kHz operation, $t_r + t_f$ should be approximately 0.5 μsec or less. Transistor delay and storage times do not affect efficiency, but cause delays in turn on and turn off resulting in lowering the frequency of operation and increasing ripple. Combined $t_d + t_s$ should be less than $0.05 \times \tau$.

Unitrode manufactures a broad variety of fast switching power transistors and Darlingtons, which are listed in the Power Transistor & Darlington Product Selection Guide. Their combinational high voltage, high current, low saturation voltage and medium to fast switching characteristics make them ideal for this application.

The diode reverse recovery time must be no more than about half the current rise time through the transistor. If this requirement is not met, large amplitude reverse recovery current spikes will be drawn from the input power supply causing severe EMI problems. Large transient currents through the transistor may cause degradation or second breakdown. Referring to Figure 1, Section II, during the time that the transistor is off, the catch diode is conducting the output current, Io, and the transistor V_{CE} equals Ein. When base drive is applied to the transistor to turn it on, current through the transistor rises from 0 to Io. During this current rise time interval, t_{ri}, the diode remains in forward conduction, but the diode current declines from Io to 0, since the inductor maintains the total current at a constant value equal to Io. If the diode has recovered at the end of the t_{ri} interval, the voltage across the transistor will start to decrease and the diode will go into the reverse direction. This period of time is the transistor voltage rise time interval, t_{rv}, which is terminated when the transistor V_{CE} reaches $V_{CE\,sat}$ and the diode V_R reaches Ein. If the diode has *not* recovered at the end of the t_{ri} interval, it will remain a low impedance instead of proceeding smoothly into the reverse direction. Transistor current will increase well above Io until the diode recovers, pulling the additional current through the diode in the reverse direction.

This problem has probably caused more grief in switching regulator applications than any other, and almost completely dominates diode selection. Diode switching losses will be completely negligible if the diode is fast enough to minimize the recovery problem, i.e., two to three times faster than the transistor turn-on rate.

Unitrode UES rectifiers, listed in the Rectifier Product Selection Guide, are uniquely suited to this type of application. With low forward drop and typical recovery time of 20 nsec from forward currents as high as 50A, they cause no discernible recovery spike when used in conjunction with Unitrode's medium frequency switching transistors.

Unitrode PIC600 Hybrid Power Switches summarized in the Switching Regulator Power Circuits Product Selection Guide combine in a single package the UES rectifier and power switching transistor with its associated drive transistor and bias resistors. Power transistor, drive transistor and rectifier are matched to optimize switching speeds and $V_{CE\,sat}$. Available in NPN and PNP versions, the PIC600 series can operate at 50 kHz with only 2.5 percent loss of efficiency compared with operation at lower frequencies. Significant reduction of EMI can be achieved because of the reduction of circuit wiring.

2. *Output Filter Capacitor.*

The most difficult component selection problem for high frequency switching regulator applications is to find and specify an output capacitor with suitably low ESR. Most tantalum and aluminum electrolytic capacitor types do not have ESR specifications (probably because ESR is not very good). In some cases, the dissipation factor, DF, is given in the specification. However, DF is usually specified at 60 Hz, which is more indicative of effective *parallel* resistance, and is virtually useless in determining ESR. When DF is specified at 1 kHz or higher, it may be used to determine ESR:

$$ESR = DF(\%) \times 0.01 \times X_C = \frac{DF(\%) \times 0.01}{2\pi fC}$$

The power circuit design example given in Section IV requires an output capacitor with C_{min} of 114 μfd and ESR_{max} of 0.025Ω. The capacitor which comes closest to meeting this requirement (after a limited search) is solid tantalum, Mallory THF, 120 μfd @ 10V. This capacitor has a max DF of 8% at 1 kHz, which defines $ESR_{max} = 0.106\Omega$. ESR is typically 0.05Ω. Two of

these capacitors in parallel are required, based on typical ESR, to achieve an ESR of 0.025Ω; four in parallel are required, based on ESR_{max} of the capacitor. The aluminum electrolytic which comes closest (again based on a limited search) is the Sprague 672D series, 1000 μfd @ 12V, which has an ESR_{max} of 0.065Ω @ 50 kHz. Typical ESR is 0.025Ω. In either case, a much larger C value is required in order to achieve the desired ESR. This does have the advantage of reducing transient voltage changes with sudden changes in load current.

It is worth noting again that with the control circuits shown in Section III (unlike conventional switching regulator control circuits), the operating frequency will remain relatively constant, regardless of ESR, although the output ripple voltage will vary directly with ESR. In some cases, it may be economically advantageous to increase the value of L (and the size and cost of the inductor) in order to reduce ripple current, $\Delta i_1 = \Delta i_2$, and thereby increase the ESR_{max} requirement.

In addition to considering the C and ESR values and appropriate voltage derating for the application, most capacitors have maximum RMS ripple current or max RMS ripple voltage ratings which should not be exceeded. Actual RMS ripple current and voltage in the application can be calculated as follows:

$$\Delta e_{o\,RMS} = \Delta e_o\,p\text{-}p/3.0$$
$$\Delta i_{RMS} = \Delta i_1\,p\text{-}p/3.5$$

In the design example of Section IV, $\Delta e_{o\,RMS} = 0.033V$, which is less than the 0.05V max ripple rating of the 10V Mallory THF capacitor, and $\Delta i_{RMS} = 1.14A$, which is less than the 2.47A max ripple current rating of the 1000 μfd, 12V Sprague 672D capacitor.

Series inductance of the capacitor is usually not significant compared to ESR at frequencies below 100 kHz. However, inductance can become dominant if good wiring practices are not followed. Specifically, the ground side of the catch diode should be returned directly and as close as possible to the ground side of the capacitor, and capacitor lead length including circuit wiring on both sides of the capacitor should be minimized.

3. *Control Amplifier and Reference.*

Control circuits for switching regulators can be designed around IC operational amplifiers and separate voltage references, or around low power voltage regulator IC's which have built-in references. Voltage regulator IC's such as the LM304, LM305, and μA723 have the added advantage that the output current they provide to drive the power switching transistor can be caused to diminish at higher temperatures, which conforms to the transistor drive requirements vs. temperature and helps to maintain optimum switching speeds over a range of temperatures. Amplifiers used in the control circuit should be uncompensated in order to obtain fast switching speeds, otherwise the delay times introduced will result in lower frequency operation and larger ripple amplitudes, and may cause circuit instability.

Appendix A
Analysis of Power Circuit

The design equations for the switching regulator power circuit used throughout this design guide were based on several simplifying assumptions, which will now be dealt with.

The simplified equations neglected the effect of "catch" diode forward drop, V_F, transistor saturation voltage, V_{sat}, and the IR drops in the inductor and current sensing resistor, Io R_X. If a design is implemented using the values of L, C, ESR, and Δi derived from the simplified equations, then t_{on}, t_{off}, f, and Δe_o will differ from the design values because of the effect of the simplifying assumptions as follows, from Figure 2b:

Simplified :

$$\Delta i_1 = \frac{(Ein - Eo)t_{on}}{L} \quad (1)$$

Exact :

$$\Delta i_1 = \frac{(Ein - Eo - V_{sat} - Io\,R_X)t_{on}'}{L} \quad (2)$$

Simplified :

$$\Delta i_1 = \frac{Eo\,t_{off}}{L} \quad (3)$$

Exact :

$$\Delta i_1 = \frac{(Eo + V_D + Io\,R_X)t_{off}'}{L} \quad (4)$$

Note that Δi_1 is fixed, because the control circuit controls this value directly. Instead of the original design values of t_{on} and t_{off}, actual values t_{on}' and t_{off}' will be observed. Since Δi_1 is fixed, we can equate Equations (1) to (2) and (3) to (4):

$$\frac{t_{on}'}{t_{on}} = \frac{(Ein - Eo)}{(Ein - Eo - V_{sat} - IoR_X)} \quad \text{and}$$

$$\frac{t_{off}'}{t_{off}} = \frac{Eo}{Eo + V_D + IoR_X}$$

Although the actual t_{off}' is less than the assumed t_{off}, t_{on}' is greater than the assumed t_{on}, so that their net effect on the operating frequency is reduced. In the worst-case, when Eo is small (5V) and Ein is high (50V), the actual frequency will be 25 percent higher than the original assumed frequency, resulting in a very slight drop in efficiency. Output ripple component Δv_C will be smaller because of the higher frequency, and Δv_{ESR} will not change because Δi_1 is fixed. Component tolerances will result in larger deviations than those caused by the use of the simplified equations.

The only other assumption that could have possible significance is that the transistor switching times are negligible at the highest frequency of operation. The validity of this assumption is normally assured by selecting appropriate devices (see Section VI). This also applies to the speed of the control circuit. If delay time through the control circuit in addition to transistor turn-on and turn-off times is significant with respect to the total period, τ, the consequent delay in turning the power circuit on and off will cause a proportional increase in Δi_1 and Δe_o, and a proportional decrease in frequency.

Efficiency Calculations: The efficiency of a switching regulator depends upon the factors given in the following equation:

$$\text{Efficiency} = \frac{\text{Pout}}{\text{Pin}} \times 100\% = \frac{\text{Eo} \times \text{Io}}{\text{Eo} \times \text{Io} + P_T + P_D + p_T + p_D + P_L + P_I + p_C + P_C}$$

Note that the worst case for each factor does not necessarily occur under the same conditions.

1. *DC Losses – Transistor.* (Worst case when Ein is lowest because t_{on} is largest.)

$$P_T = V_{CE\,sat} \times \text{Io} \times \frac{t_{on}}{\tau}$$

where: $\frac{t_{on}}{\tau} = \frac{\text{Eo}}{\text{Ein}}$

2. *DC Losses – Diode.* (Worst case when Ein is highest.)

$$P_D = V_F \times \text{Io} \times \frac{t_{off}}{\tau}$$

where: $\frac{t_{off}}{\tau} = 1 - \frac{\text{Eo}}{\text{Ein}}$

3. *Switching Losses – Transistor.* (Worst case when Ein is high. $t_d + t_s$ do not contribute to power losses.)

$$p_T = \text{Ein} \times \text{Io} \frac{t_r + t_f}{2\tau}$$

where: $t_r = t_{rv} + t_{ri}$, $t_f = t_{fv} + t_{fi}$

4. *Switching Losses – Diode.*
This is a very complex calculation if diode recovery time is not much smaller than the transistor rise time, because the diode will short-circuit the power supply prior to turn-off, affecting the transistor dissipation, possibly causing second breakdown, and generating intolerable EMI. By using a diode whose recovery time is not more than half the transistor rise time, all these problems become negligible.

5. *DC Losses – Inductor.* (AC losses are negligible when Δi_1 is small compared to Io.)

$$P_L = \text{Io}^2 \times R_S$$

where: R_S is equal to effective series resistance of inductor.

6. *DC Losses – Current Sense Resistor.* (AC losses negligible when Δi_1 is small compared to Io.)

$$p_I = \text{Io}^2 \times R_I$$

7. *AC Losses – Capacitor.* (Usually negligible.)

$$p_C = \frac{\Delta i_1{}^2}{12} \times \text{ESR}$$

8. *Control Circuit Losses.* (Base drive to switching transistor is dominant, but usually negligible.)

$$P_C = \text{Ein} \times I_b \times \frac{t_{on}}{\tau} = \text{Eo} \times I_b$$

where: $\frac{t_{on}}{\tau} = \frac{\text{Eo}}{\text{Ein}}$

Appendix B
Analysis of Power Inductor Design

This appendix describes the methods used to develop the core tables given in Section V and the nomographic method for design of the power inductor. Core parameters for any cores not listed in the tables can be derived from the equations given.

The following equations provide the basis for this design approach. Equation (1a) defines the value of inductance, L, in terms of basic core parameters and the total number of turns, N, wound on the core:

$$L = N^2 \times 0.4\pi\mu\frac{A_e}{\ell_e} \times 10^{-5} \quad \text{mH} \qquad (1a)$$

where: μ = effective permeability of core

ℓ_e = effective magnetic path length – cm

A_e = effective magnetic cross section – cm^2

For most standard cores, the above calculation has been simplified by listing the compound parameter A_L, called the "inductor index", as follows:

$$L = N^2 A_L \times 10^{-6} \quad \text{mH} \qquad (1b)$$

where: $A_L = 0.4\pi\mu\frac{A_e}{\ell_e} \times 10$ mH for 1000 turns

Multiplying both sides of Equation (1b) by I^2,

$$LI^2 = (NI)^2 A_L \times 10^{-6} \quad \text{millijoules} \qquad (2)$$

Core Saturation Limits.

Any specific core has a maximum ampere-turn, NI, capability limited by magnetic saturation of the core material. $(NI)_{sat}$ is listed in some core catalogs, in which case the maximum $(LI^2)_{sat}$ capability of the core can be calculated from Equation (2). $(NI)_{sat}$ is related to the saturation flux density, B_{sat}, as follows:

$$(NI)_{sat} = 10\frac{B_{sat} A_e}{A_L} \quad \text{ampere-turns} \qquad (3)$$

Substituting Equation (3) into (2),

$$(LI^2)_{sat} = \frac{B_{sat}^2 A_e^2 \times 10^{-4}}{A_L} \quad \text{millijoules} \qquad (4)$$

Values of $(LI^2)_{sat}$ are given for each core represented in Tables 1 and 2 of Section III. Equation (2) *or* (4) was employed, using values for either B_{sat} or NI which would result in a reduction of A_L (and L) of 20 percent under maximum overload conditions, according to the core manufacturer's data. The core selected for an application must have an $(LI^2)_{sat}$ value greater than $L(i_1 \text{ max})^2$ to insure that the core will not saturate under maximum peak overload current conditions.

Power Dissipation and Temperature Rise Limits.

In switching regulator applications, the AC current component is small compared to the DC current through the power inductor. Power dissipation in the inductor is almost entirely DC losses in the winding. DC resistance of the winding, R_s, is calculated from the following:

$$R_s = \rho \frac{\ell_w}{A_x} N \quad \text{ohms} \qquad (5)$$

where: ℓ_w = mean length of turn – cm
A_x = effective area of wire – cm²
ρ = resistivity of wire – Ω-cm

Core geometry provides a certain window area, A_W, for the winding, but only a fraction of this area can be occupied by the actual conductor. The *effective* window area, A_W' is taken as 0.5 A_W for toroids, and 0.65 A_W for pot cores. This allows for wasted area of uniformly wound round wire with HF insulation, allows for the fact that the central fourth of the window area of a toroid cannot practically be filled, and allows for a single section bobbin in the case of the pot core. The number of turns, area of wire, and effective window area of a fully wound core are related by:

$$A_x = \frac{A_W'}{N} \text{ cm}^2 \qquad (6)$$

Substituting Equation (6) into (5):

$$R_s = \rho \frac{\ell_w}{A_W'} N^2 \quad \text{ohms} \qquad (7)$$

Multiplying both sides of Equation (7) by I^2, the power dissipation in the winding, P_L, is:

$$P_L = I^2 R_s = I^2 \rho \frac{\ell_w}{A_W'} N^2 \quad \text{Watts} \qquad (8)$$

Substituting for N from Equation (1b), and rearranging:

$$LI^2 = P_L \frac{A_L A_W'}{\rho \ell_w} \times 10^{-6} \quad \text{millijoules} \qquad (9)$$

Equation (9) shows that the LI^2 capability is directly related to, and is limited by the maximum permissible power dissipation. Using a value for P_L that will result in a 25°C rise in the temperature of the inductor, values of $(LI^2)_{25C}$ are calculated for each core in Tables 1 and 2 of Section III. For these calculations, resistivity, ρ, is assumed to be 1.9×10^{-6} Ω-cm, the resistivity of copper wire at 65°C. The power dissipation that will result in a 25°C rise is calculated and tabulated for each core as follows:

$$\Delta T = 850 \frac{P_L}{A_s} \quad °C \qquad (10)$$

where: ΔT = temperature rise
A_s = surface area of inductor – cm²

The factor 850 in the above equation represents a temperature rise of 850°C for 1W power dissipation from 1 cm² surface area, empirically determined for natural convection cooling. The surface area, A_s, used in the calculation is taken as the top and sides of the inductor, ignoring the mounted bottom surface. Substituting a temperature rise of 25°C:

$$P_{25C} = \frac{25 \times A_s}{850} \quad \text{Watts} \qquad (11)$$

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Appendix C
Analysis of Application Circuits

The design equations for the critical components and operating parameters of Figure 3, Section III, are given below, for the following design objectives:

Eo	=	+5V
Δe_o	=	100 mV p-p
Ein	=	20V min, 40V max
Io	=	2A min, 10A max
Current Limit	=	14A max peak

Using the procedure described in Section IV, the following parameters were established:

f	=	50 kHz (nominal)
t_{off}	=	17.5 μsec
L	=	22 μH
C	=	120 μF min
ESR of capacitor	=	0.025 Ωmax
Δi_1	=	4A

From the manufacturer's design data for the LM305, we know that: the internal reference voltage, V_{ref}, is 1.8V, nominal; the impedance of the inverting input is very high; the threshold level of the drive-current-limiting circuit is 0.30V; and the impedance of the noninverting input (Rin) is 2.4K, nominal.

From the Unitrode data for the PIC625 Hybrid Power Switch, the drive current (I drive) required for Io = 10A is 30 mA. The V_{BE} of Q1 is taken as 0.6V.

First, we may calculate the values R1 and R2 of the output divider. We will make the effective parallel resistance of R1 and R2 equal to 2.4K, so that the impedance at the inverting input will be approximately the same as the noninverting input of the LM305:

$$\frac{R2}{R1 + R2} = \frac{Vref}{Eo} = \frac{1.8}{5}$$

$$\frac{R1\,R2}{R1 + R2} = Rin = 2.4K$$

The resulting values are R1 = 6.8K, R2 = 3.8K. R2 may be trimmed for precise setting of Eo.

C1 and C2 function to provide negative and positive AC feedback, and should be large enough to result in small losses to the AC signals. Assuming that Rin = (R1 × R2)/(R1 + R2), the value of C1 should be twice the value of C2, so that the negative feedback will be dominant over positive feedback at all frequencies, thereby ensuring circuit stability. The following relationships satisfy these conditions:

$$C2 \geqslant \frac{1}{Rin \times f} \quad ; \quad C1 = 2 \times C2$$

where: f = the nominal switching frequency.

These equations are satisfied by C2 $\approx$ 0.01 μF and C1 = 0.02 μF. Making C1 and C2 too large will have an adverse effect on transient recovery time of the switching regulator.

R4 is calculated from the threshold voltage of the LM305 drive current limiting circuit and the required base drive current.

$$R4 = \frac{V\ threshold}{I\ drive} = \frac{0.3V}{0.03A} = 10\Omega$$

Current sampling resistor R_I is determined by the desired short circuit current limit and the V_{BE} of Q1. As described in Section III, under *current overload conditions,* current i_1 ranges between two values. The maximum instantaneous overload current is defined by: $i_1 \times R_I = V_{BE} + V_{R3}$. The minimum instantaneous overload current is defined by: $i_1 \times R_I = V_{BE}$.

Since Δi_1 has been previously defined as 4A p-p, if we assume a minimum value of 10A for i_1 under overload conditions, then the maximum peak overload value for i_1 will be 14A, and the average value of i_1 = Io under overload conditions is 12A.

$$R_I = \frac{V_{BE}}{i_1\ (min\ overload)} = \frac{0.6V}{10A} = 0.06\Omega$$

Power dissipation in R_I will be 6W under full load conditions, and 8.64W under overload conditions.

R3 determines Δi_1 under overload conditions as well as for normal operation of the switching regulator:

$$R3 \times I_{drive} = R_I \times \Delta i_1$$

$$R3 = \frac{R_I \times \Delta i_1}{I_{drive}} = \frac{0.06 \times 4}{0.030} = 8\Omega$$

The value of R5 is determined empirically to optimize regulation versus changes in Ein. With R5 omitted, Eo changes approximately 70 mV when Ein is changed from 20V to 40V. With R5 = 1.2 MΩ, the change in Eo is reduced to less than 25 mV.

THE IMPORTANCE OF RECTIFIER CHARACTERISTICS IN SWITCHING POWER SUPPLY DESIGN

With the increasing interest in switching regulated power supplies designers have directed much of their effort to selecting transistors with low switching losses and adequate power handling capability. While recognizing that they must use fast recovery rectifiers, less attention has been given to "how fast" or "what type of recovery characteristic" is desired. More detailed knowledge of rectifier behavior allows determination of the magnitude of increased losses and stress on the transistor by the non-ideal diode. By choosing the best available rectifier, transistor stress can be minimal, thereby resulting in higher reliability. Other benefits are:

A. Improved power supply efficiency
B. Lower noise
C. Lower cost and/or
D. Smaller size and weight

The performance of fast recitifiers in the most popular switching circuits is discussed below.

"Switcher" inputs use available DC voltages, or rectifiers directly off the AC line. This DC "input" is converted by semiconductor switches operating at high frequency in circuits such as buck, flyback or boost regulators and in pulse-width-modulated or square wave inverters.

Inverter output rectifiers and regulator "catch" diodes are subject to unusual stresses due to the fast switching rates and very low impedance seen by the diode during the reverse transient (diode turn-off) and a momentary high impedance during diode turn-on.

These new square wave switching supplies are limited in efficiency and frequency by transistor stress and switching losses, some of which is due to diode switching characteristics. Faster transistors and diodes are helping to increase efficiency and/or frequency. At low output voltages, and lower frequency the DC characteristics ($V_{CE(sat)}$ and V_F) have the major influence on efficiency. However, as frequency and/or input voltage increase the switching characteristics become increasingly important.

BUCK REGULATOR ANALYSIS

Ideal Diode — For better understanding consider the buck regulator and resulting waveforms, using an *ideal* diode and assuming linear current rise and fall in the power transistor during switching. Similar considerations apply to other types of switching regulator circuits.

The transistor "on" time, t controls the conversion such that,

$$(1)\ V_o = \frac{t}{\tau} V_i$$

where τ is the period. t is determined by the control circuit which senses output voltage and controls transistor base drive.

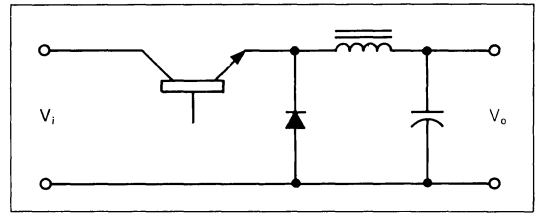

Figure 1a

In this regulator the inductor current is essentially constant as it flows alternately through the transistor or "catch" diode. The sum of the transistor current and diode current must always equal the current in the inductor, which cannot change instantaneously.

At t_o the diode is conducting inductor current while the transistor is blocking the input voltage.

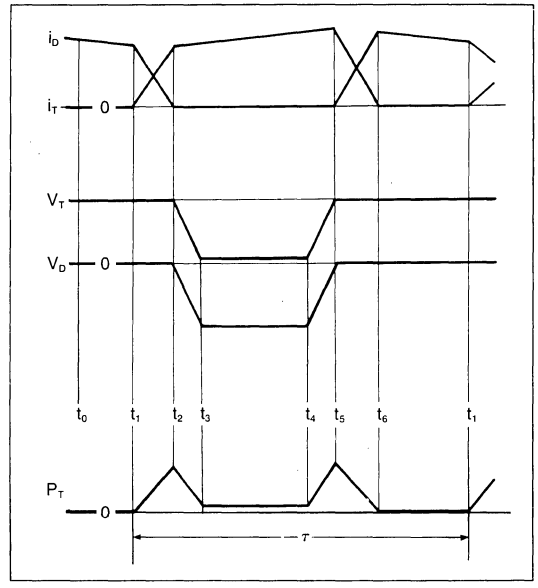

Figure 1b

t_1 to t_2 is the current rise time t_{ri} of the transistor. Since inductor current is not changing, the diode current must decrease. The forward biased diode maintains full input voltage across the transistor.

At t_2 the transistor is conducting all the inductor current so the diode turns off and voltage across the transistor

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starts to decrease toward $V_{CE\ (sat)}$.

t_2 to t_3 is the voltage rise time, t_{rv} of the transistor.

From t_3 to t_4 the transistor is saturated and conducting the inductor current i_L.

At t_4 the transistor starts to turn off and V_{CE} increases.

t_4 to t_5 is the voltage fall time t_{fv} of the transistor. During this time the transistor must conduct the entire inductor current because the diode is still reverse biased. At t_5 the diode is forward biased and the transistor is blocking the full input voltage. Diode current starts to increase and the transistor current decreases, the sum equalling i_L.

t_5 to t_6 is the current fall time t_{fi} of the transistor. Diode current increases in a complementary manner. From t_6 to t_1 the transistor is off and the diode is conducting all the inductor current.

To simplify the illustration assume the inductor current constant and equal to I_o. Transistor dissipation P_T is the sum of transient switching and DC losses. Neglecting losses due to DC leakages, which are generally negligible:

$$(2)\ P_T = \frac{V_i\, I_o}{2}\,\frac{(t_{ri} + t_{rv} + t_{fv} + t_{fi})}{\tau} + \frac{V_{CE\ (sat)}\, I_o\, (t_4 - t_3)}{\tau}$$

$$(3)\ P_T = \frac{I_o}{\tau}\left\{\frac{V_i}{2}(t_{ri} + t_{rv} + t_{fv} + t_{fi}) + V_{CE(sat)}\,(t_4 - t_3)\right\}$$

Practical diode — Now consider how the non-ideal diode with reverse recovery, junction capacitance, forward recovery and DC loss affects the circuit of Figure 1a.

In Figure 1c the solid lines are the waveforms using a practical diode in a buck regulator circuit. Comparing them with the dotted lines of the ideal diode previously considered we see three significant differences during transient switching and one during DC conduction:

1. The peak collector current increases (above I_o) during a period of high dissipation t_2 to t_2'.
2. Rise times t_{ri} and t_{rv} are increased. $(t_2' - t_1) > (t_2 - t_1)$ and $(t_3' - t_2') > (t_3 - t_2)$.
3. Maximum collector voltage peaks up above V_i briefly at t_5.
4. The diode has DC loss (from t_6 to t_1) and switching loss (principally from t_2' to t_3').

From the P_T curve of Figure 1c it is obvious that transistor power dissipation increases above that of (3) due to the "real" diode, — see the hatched regions.

The magnitude of these detrimental factors depends on the choice of rectifier. Before considering losses more fully let us examine the switching periods in greater detail.

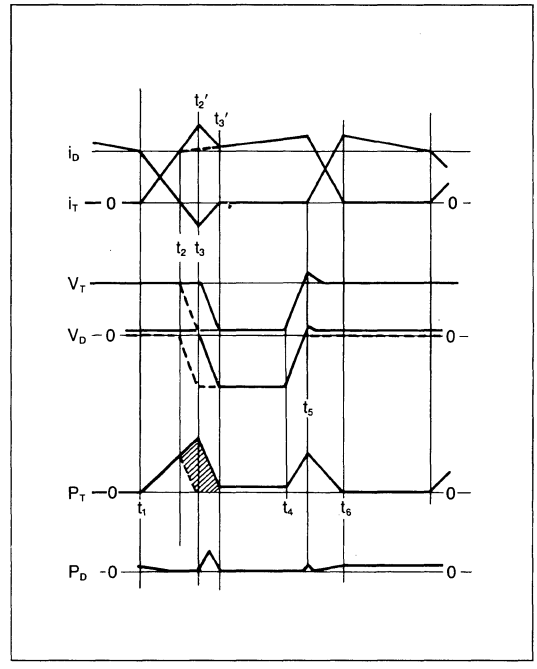


Figure 1c

TRANSISTOR TURN-ON BEHAVIOR

The transistor "turn-on transient", when the diode is switching from forward conduction to reverse blocking, results in the following transistor and diode waveforms:

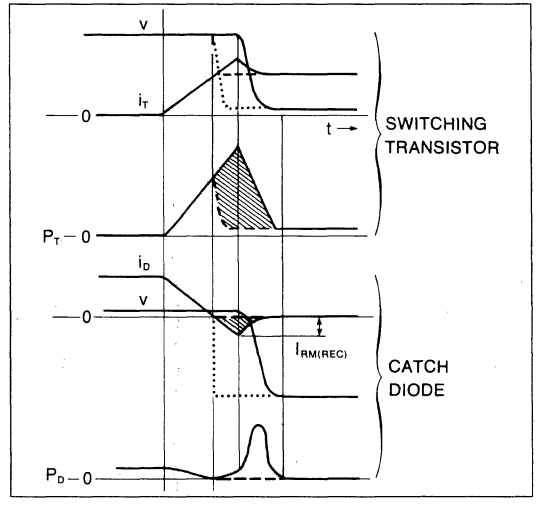


Figure 2

Dashed lines show what the current and power would be if the *diode* were ideal to the extent of having no reverse recovery time or junction capacitance. (Dotted

lines show the voltage for the ideal diode case.) The reverse diode current caused by diode capacitance and recovered charge is shown by the cross hatched area of the i_D curve. The transistor must conduct this reverse diode current as well as the inductor current. The grey area represents additional transistor dissipation due solely to the diode recovered charge and capacitance.

Faster switching transistors will not necessarily result in reduced switching losses. Unless a diode with recovery time 2 or 3 times faster than the transistor current rise time is used, a faster transistor will increase the peak recovery current in the diode and thus increase overall switching losses. Furthermore, a diode with a "soft" recovery characteristic will cause more dissipation than an "abrupt" type with the same peak recovery current. The relationship of recovery characteristic to switching rate is discussed in Appendix B. With many switching transistors now available a 200 nS fast-recovery rectifier will have a peak recovery current $I_{RM(REC)}$ greater than shown in the i_D waveform of Figure 2, where it is about ⅓ of the forward current. This rather modest additional collector current (of 33% above that limited by an ideal diode) can cause increased transistor power dissipation of 100 to 150% during the turn-on period. Other serious problems can occur from high peak currents, such as noise transients in the line, the transistor coming-out of saturation and forward-biased second breakdown.

Rectifiers are now available with recovery characteristics to keep these problems minimal. Their use is required for a switching supply of maximum reliability and efficiency.

TRANSISTOR TURN-OFF BEHAVIOR:

When the transistor turns off, the diode turn-on characteristic usually has little effect on power dissipation but may cause voltage spiking, with resulting noise and the possibility of exceeding the transistor voltage ratings. Diode characteristics and conditions under which these transients occur are discussed in Appendix C. The voltage spike is due to the forward recovery characteristic and, when present, will occur as shown (dotted) in Figure 3. To correct it a snubber (series RC across the diode) may be needed. However, the choice of an optimum diode will minimize or eliminate this need.

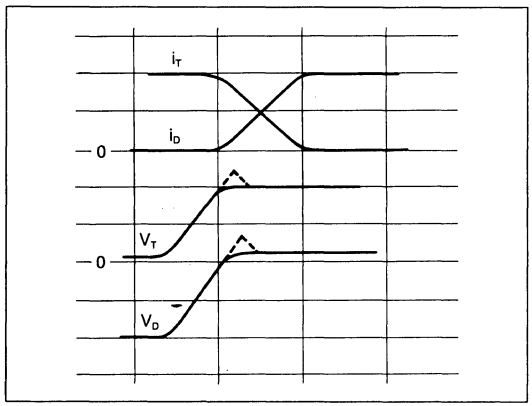


Figure 3

POWER LOSSES IN THE SEMICONDUCTOR DEVICES

DC Losses in the buck regulator occur alternately when the diode is forward conducting and when the transistor is turned on. Referring to Figure 1 these intervals are t_6 to t_1 and t_3 to t_4 respectively. During *either* interval the dissipation is independent of input voltage, V_i, or output voltage, V_o, depending only on load current and device voltage drop. *Total circuit DC losses* are a function of V_o/V_i because a) this ratio relates to "on" time and b) transistor $V_{CE(sat)}$ will probably not equal diode V_F. Neglecting switching intervals the dissipation due to DC losses is:

$$(4)\quad P_{DC} = V_F I_o \frac{V_i - V_o}{V_i} + V_{CE\,(sat)} I_o \frac{V_o}{V_i} .$$

Loss of efficiency due to DC losses is greatest when V_o is low, with diode loss being more significant when V_i is relatively high and transistor loss dominating when V_i is close to V_o.

Transient (switching) losses in the regulator vary considerably with voltage, being highest at "high line" V_i (see Eq. 3). Furthermore, high voltage transistors and rectifiers generally have longer switching times than low voltage types. Speed and "recovery characteristic" (see Appendix B), and consequently losses, can vary greatly between different device types and manufacturing processes. A relationship for calculating approximate transient dissipation of practical devices during the transistor turn-on interval is given in Appendix B. The other component (turn-off interval) can be similarly developed but it is not significantly affected by diode selection. However, when transistors and/or drive techniques are chosen for shorter fall times overall losses are reduced *and* the benefits of optimum diode selection become more significant. Proper diode (and transistor) selection is important in all switching supplies, but the higher the voltage (and frequency) the more significant will be the effect of selection on switching losses.

OTHER SWITCHING CIRCUITS

The pulse-width-modulated inverter (PWM) supply (Figure 4a) has much in common with the buck regulator. Output rectifiers also perform the catch diode function. Current waveforms are shown in Figure 4b,

with overshoot due to diode reverse recovery and capacitance. Here again slow diodes cause additional transistor stress, usually not reduced significantly by transformer impedance. Leakage reactance will often require the use of a snubber, to protect the transistor.

Transistor "on" time t and the turns-ratio control the conversion such that

$$(5)\ V_o = \frac{2t}{\tau}\frac{N_s}{N_p} V_i$$

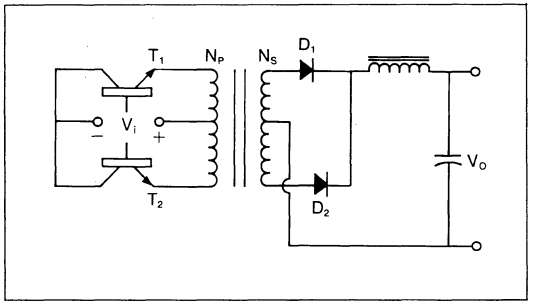


Figure 4a

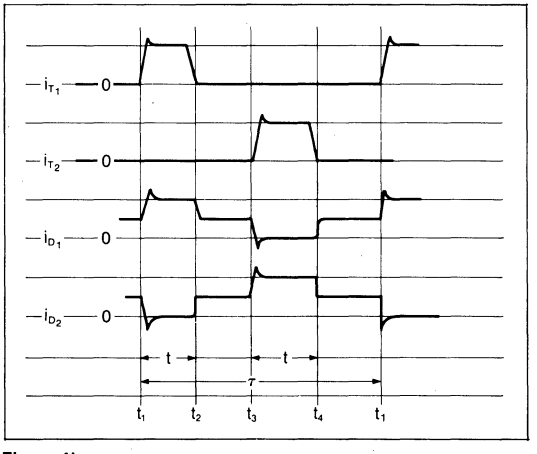


Figure 4b

From t_1 to t_2 transistor T_1 and diode D_1 conduct, with diode current equal to inductor current i_L.

At t_2 the transistor turns off and the inductor "pulls" i_L equally through D_1 and D_2.

At t_3 transistor T_2 turns on, driving full i_L through D_2 and causing D_1 to be reversed biased. D_2 current is increased by the recovery current of D_1, and T_2 current also increases proportionally.

From t_4 to t_1 both transistors are again off and at t_1 the events of t_3 occur on the opposite device pair.

One difference between the inverter and the regulator is that here the DC diode losses are more significant because they (D_1 and/or D_2) are conducting the full cycle regardless of V_i to V_o ratio. Another difference is that here the diode recovery is from half, rather than full, load current.

The square wave inverter can be considered, in terms of device operation, a special case of the PWM where 2t approaches τ. Regulation is achieved by varying V_i.

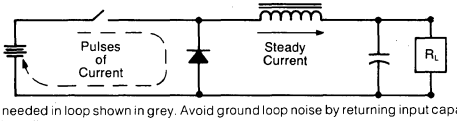
EMI, RFI, NOISE —

Given any inductance in a circuit "loop" of wiring, a rapid current change will generate a voltage transient, V = L di/dt, and the energy in such a transient will vary with the square of the current, $E = \frac{1}{2}LI^2$. The interference and voltage spiking will be easier to filter if the energy is low and has predominantly high frequency components.

We can establish a priority of factors for reducing EMI:
1. $I_{RM(REC)}$ should be as low as possible, — accomplish by diode selection (see Appendix B and Fig. 7).
2. L (circuit loop) should be minimum, — accomplish by layout and interconnect geometry. (See Fig. 5).
3. Use a "soft recovery" diode (See Appendix B). However, this is an item of possible trade-off since such a device may have longer t_{rr}, higher $I_{RM(REC)}$ and, thus, create much higher switching loss.

An ultra-fast device with moderate recovery (vs. abrupt or soft) will often be the best choice.

REDUCE EMI BY LOWERING CIRCUIT WIRING INDUCTANCE:



Low L needed in loop shown in grey. Avoid ground loop noise by returning input capacitor directly to diode.

Figure 5a

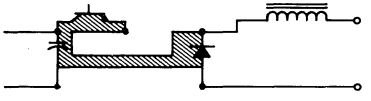


Figure 5b

SELECTING THE BEST SWITCHING RECTIFIER

Ratings and characteristics have different priorities and significance when they are to be applied to these power switching circuits. Selection should be based on the following:

1. Peak inverse voltage, PIV of "catch" diodes must at least equal the highest input voltage, while PIV of center-tap output rectifiers must be at least twice the maximum output voltage in a square wave inverter and much greater in the pulse width modulated inverter. More significant perhaps are the transient voltages in practical fast switching circuits partly due to wiring inductance and rectifier's own recovery. Unless these are intentionally clipped, damped, or "designed out" it is advisable to use a safety factor of 2 or 3. PIV selected

should apply over a range from lowest ambient to the highest expected junction temperature.

2. Reverse recovery time t_{rr} must be much lower than the rise time of the transistor with which it will be used, — preferably by at least 3 times when measured at conditions similar to circuit operation. Selection is complicated because rectifiers are normally specified at conditions less severe than in power switching circuits. Furthermore, correlation between test conditions is not always the same (see Table I of Appendix B).

Following preliminary selection from available data the devices should be compared in a circuit developing the highest current, junction temperature and rate of current switching (– di/dt) expected.

The desired goal is to minimize peak recovery current $I_{RM(REC)}$ and switching loss. Note that these are the same order of magnitude with Schottky rectifiers (due to high capacitance, principally) as with the fastest PN rectifiers. The figures below illustrate these points. Figure 6 shows the variation of peak current with switching rate, using the Unitrode UES 801 in a special test circuit. Figure 7 shows the difference in $I_{RM(REC)}$ and t_{rr} when representative fast recovery DO-5 devices are measured in a JEDEC test circuit at different temperatures. In Figure 8 the incremental collector current (the peak value in excess of 30 A) for a 30 A buck regulator using 50, 100, and 200 nS catch diodes is plotted as a function of transistor rise time (and resulting di/dt). Figures 9a, b, and c show the loss of efficiency due to transistor turn-on dissipation as a function of operating frequency, with 3 transistor rise times and 3 diode recovery times, in a regulator operated with 40 V in and 10 V out. Similar figures can be developed for other conditions using the model and assumptions in Appendix B.

3. Forward voltage should be as low as possible to optimize efficiency, especially for inverter output rectifiers and regulators with high V_i/V_o ratios. Loss of efficiency due to V_F is most significant at low output voltages. Figure 10, which relates this loss to device choice over the range of available forward voltages, applies to output rectifiers of inverter supplies with popular output voltages.

Schottky rectifiers have the lowest V_F and are therefore widely used as output rectifiers for 5 V supplies. Their limitations in PIV, transient voltage capability and temperature must be considered when applying them in other applications.

Selection should be based on conditions where losses are most significant, — at rated supply output current and anticipated junction temperature. The approximate range of V_F, at rated current and 25°C, as well as at more typical operating conditions, is shown in Figure 11 for representative fast rectifier types. Note that the Unitrode UES series is closest to the Schottky, especially at expected operating conditions.

4. Maximum average rectified output current at maximum expected case or ambient temperature must always be considered. Note however, that standard current rating is based on a half sine waveform. These square wave applications at average current equal to this rating will usually dissipate somewhat lower power, and, thus, be used conservatively. However, regulators with $V_i \lesssim 1.5\ V_o$ should use a catch diode with a higher rating than the average current it conducts at full load.

5. Peak voltage $V_{F(DYN)}$ during forward recovery will be of significance when using transistors with fast fall times at close to the V_{CE} rating. This is further discussed in Appendix C. See Table II for typical performance of representative devices. At lower values of di/dt the peak voltages will be lower.

6. Surge current (8.3 mS) is not of great significance because transistor saturation limits fault current. If the power supply is designed to provide rapid charging of a large output capacitor the "overload" requirement for the charge time (perhaps 0.1 to 2 seconds or so) must be considered.

$I_{RM(REC)}$ & t_{rr} vs $\frac{di}{dt}$

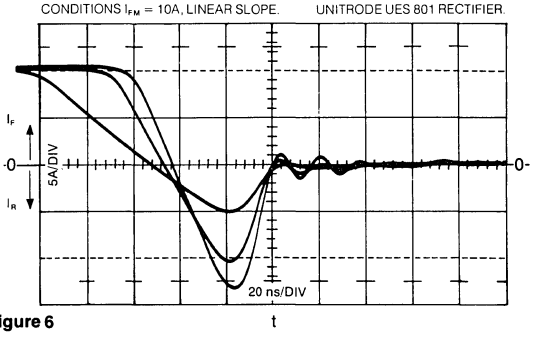


Figure 6

$I_{RM(REC)}$ & t_{rr} of DO5 FAST RECTIFIERS

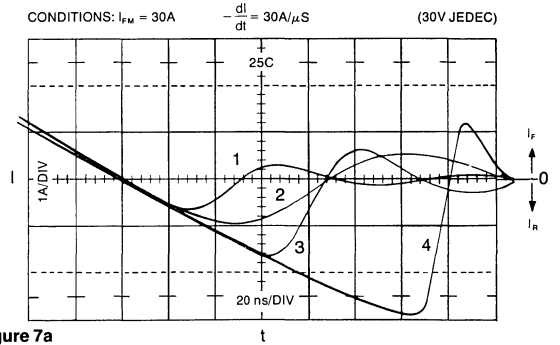


Figure 7a

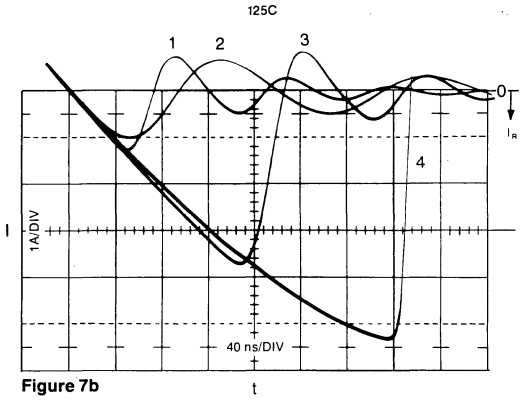


Figure 7b

DEVICE TYPE	$I_{RM(REC)}$		t_{rr}		t_{rr} MAX. At Low Current Cond'ns.
	25°C (A)	125°C (A)	25°C (nS)	125°C (nS)	
1	0.6	1.3	50	72	50
2	1.0	1.0	86	95	—
3	1.7	3.7	86	185	100
4	2.9	5.4	142	296	200

1 Unitrode UES 803
2 USD545
3 100nS rectifier.
4 200nS rectifier.

Figure 7c

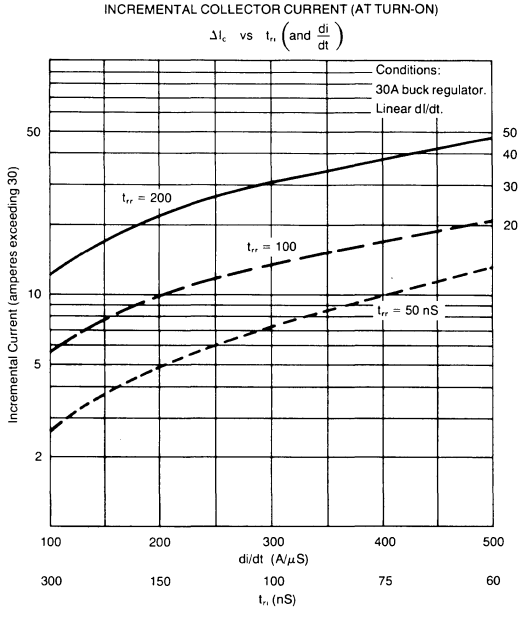


Figure 8

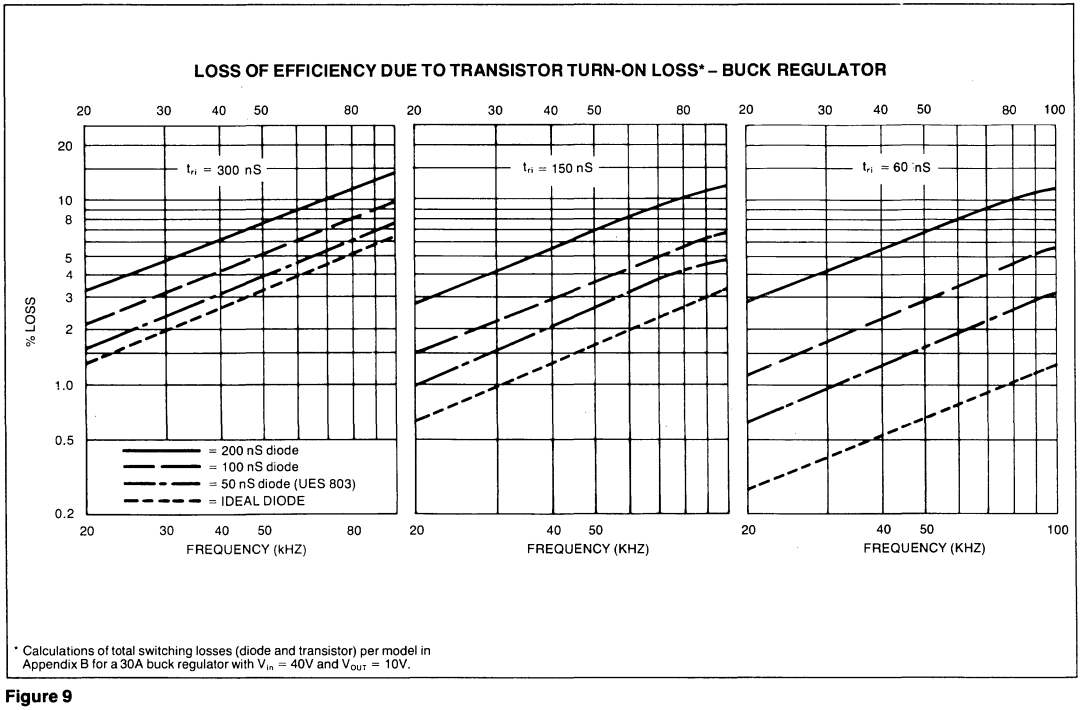


Figure 9

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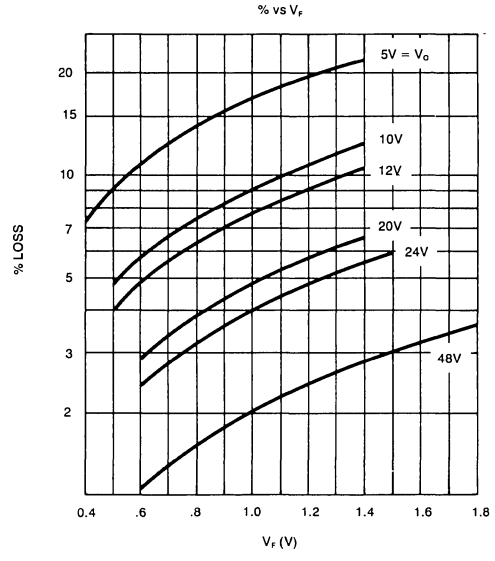
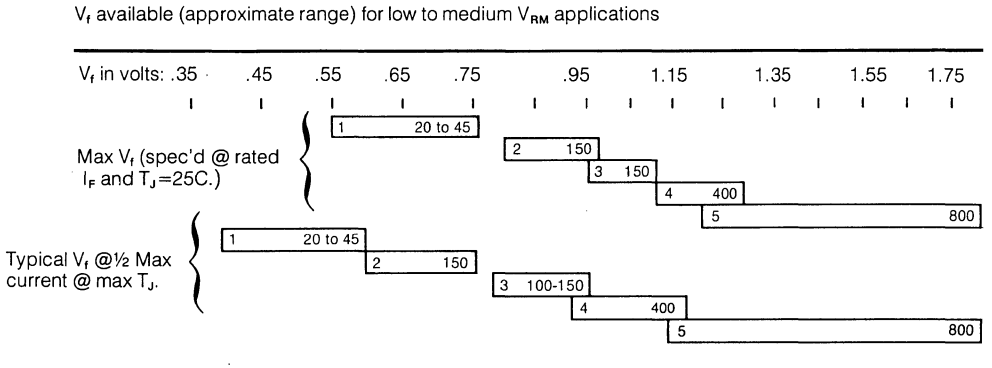


LOSS OF EFFICIENCY DUE TO FORWARD VOLTAGE OF INVERTER OUTPUT RECTIFIERS.

Figure 10



KEY: **N** XY

1 = Schottky. USD series.

2 = Unitrode UES 150 V series.

3 = Other devices for low forward voltage.

4 = Typical fast recovery (200 nS) devices.

5 = Fast devices to 800 V.

N = Device Class

XY = V_{RW}
(Max. at T_J noted above).

Figure 11

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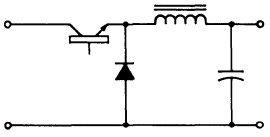
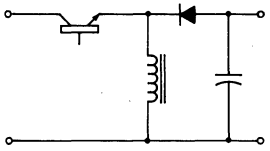
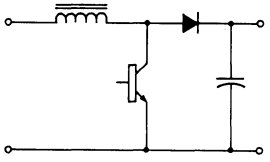
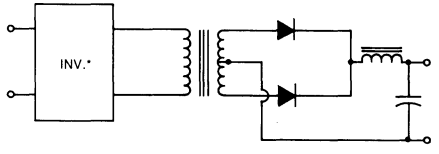
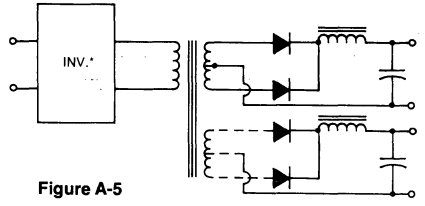
Appendix A
"Off-Line" Supplies

BASIC CIRCUIT	TYPE	FEATURES
Figure A-1 	a) Buck Regulator	$V_o < V_{in}$. Output non-isolated. Easy to filter output. Noisy input.
Figure A-2 	b) Flyback Regulator	V_o opposite polarity from V_{in}. (Unless isolated). Output can be isolated. Output can be stepped up to HV. Noisy input and output.
Figure A-3 	c) Boost Regulator	$V_o > V_{in}$. Output non-isolated. Hard to filter output. Quiet input.
FROM RECTIFIED, OFF-LINE (OR OTHER DC) SOURCE  **Figure A-4**	d) PWM (Variable Duty Cycle) Inverter.	Used with single V_o, - also common for lab supplies. Provides isolation. Does not need separate catch diode, - rectifiers serve this function, possibly with small HV diodes in primary for magnetizing current.
INPUT FROM a, b, or c.  **Figure A-5**	e) Square Wave Inverter (50% Duty)	Regulation provided by previous input. Regulates one of (possible) multiple outputs. Uses high transistor count. Provides isolation. Does not need separate catch diode, - rectifiers serve this function, possibly with small HV diodes in primary for magnetizing current.

(*) INV. = Bridge, center-tap, or half-bridge inverter.

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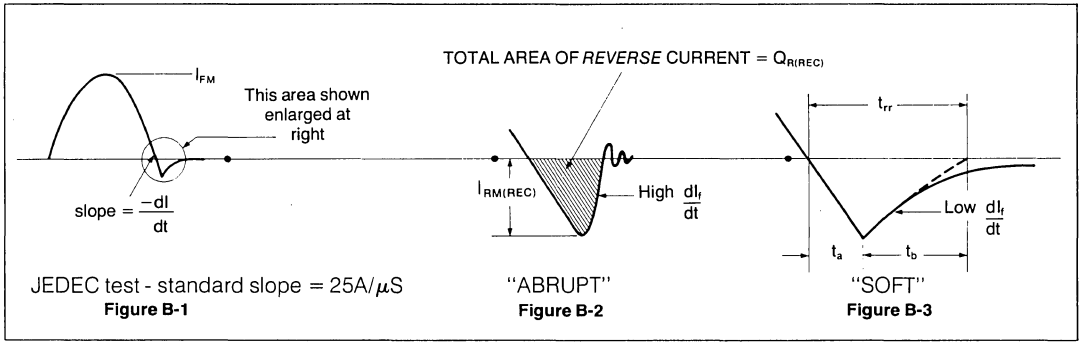
Appendix B
Reverse Recovery Behavior and Dissipation

1. Waveforms and definition of terms:



JEDEC test - standard slope = 25A/μS
Figure B-1

"ABRUPT"
Figure B-2

"SOFT"
Figure B-3

2. Discussion of Variables:

Any PN junction diode operating in the forward direction contains stored charge in the form of excess minority carriers. The amount of stored charge is proportional to the forward current level.

The diode or rectifier in a switching regulator is switched from forward conduction to reverse at a specific ramp rate ($-dI/dt$) determined by the external circuit, usually by the turn-on time of the associated switching transistor. During the first portion of the reverse recovery period, t_a, charge stored in the diode is able to provide more current than the circuit demands, so that the device appears to be a short circuit. Transition from t_a to t_b occurs when stored charge has been depleted to the point where it can no longer supply the increasing current demanded by the circuit. The device becomes a high impedance and during t_b the reverse voltage is permitted to increase. Reverse current, no longer circuit determined, dwindles as excess stored charge depletes to zero. Stored charge is depleted by the reverse current flow and also by recombination within the device.

At ($-dI/dt$) rates which are slow relative to the rate of recombination of the specific device relatively little stored charge is swept out. Recovery time, t_{rr} is determined mainly by the recombination rate, independent of ($-dI/dt$). Peak reverse recovery current $I_{RM(REC)}$, and total charge associated with reverse current, $Q_{R(REC)}$ are almost directly proportional to ($-dI/dt$) (Region I, Figure B-4). The recovery characteristic with slow ($-dI/dt$) rates tends to be soft.

When the ($-dI/dt$) rate is fast compared to recombination rate (transistor turn-on faster than diode recovery time), t_{rr} decreases as $-dI/dt$ increases, because more of the available stored charge is swept out sooner, leaving little to be depleted by recombination. As ($-dI/dt$) increases, peak recovery current increases and can become much greater than the original forward current level. However, $Q_{R(REC)}$ levels off as ($-dI/dt$) increases because it can only approach but not exceed the total stored charge which is a function of the original forward current level (Region II, Figure B-4).

Higher voltage devices have poorer recovery characteristics because they require thicker regions of higher resistivity, resulting in greater volume of stored charge and longer recombination rates.

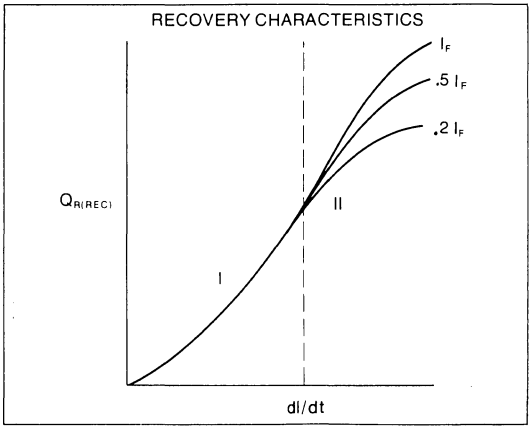


Figure B-4

With a given I_F and dI/dt the $Q_{R(REC)}$, $I_{RM(REC)}$, and t_{rr} all increase with temperature. Recovery characteristic changes as well (generally becoming more abrupt if reverse current is not circuit limited, and softer if limited). Furthermore, $Q_{R(REC)}$ increases and recovery generally softens if higher circuit voltage is applied to a given diode.

3. Comparison of devices at popular test conditions:
Table I, below, shows measured t_{rr} values (in nanoseconds) using ultra-fast and fast recovery DO-5 rectifiers.

I_F (A)	I_R (A)	−di/dt (A/μS)	T (°C)	$I_{R(REC)}$ (t_{rr} Measured to (A))	UNITRODE UES803	MANUFACTURER			
						B	C	D	E
0.5	1.0	step	25	0.25	38	50	42	—	—
1.0	1.0	step	25	0.10	45	75	50	63	120
1.0	1.0	step	125	0.10	60	90	122	135	300
	(85V JEDEC circuit)								
30	—	30	25	0	75	120	85	105	150
30	—	30	125	0	100	150	140	210	300
30	—	100	25	0	45	72	66	92	—
30	—	100	125	0	65	114	106	160	—
MAX t_{rr} per manufacturer's stated condition					50	50 to 100			200

Table I

4. Turn-on switching losses, assuming linear V and I transitions:

With an ideal diode, switching losses are entirely in the transistor as follows (from Eq. 2).

$$(B1)\ P_{(tri)} = V_{in} \cdot \frac{I_C}{2} \cdot \frac{t_{ri}}{\tau}$$

$$(B2)\ P_{(trv)} = \frac{V_{in}}{2} \cdot I_C \cdot \frac{t_{rv}}{\tau}$$

A practical diode with finite t_{rr} and $I_{RM(REC)}$ will cause *additional* switching losses as follows:

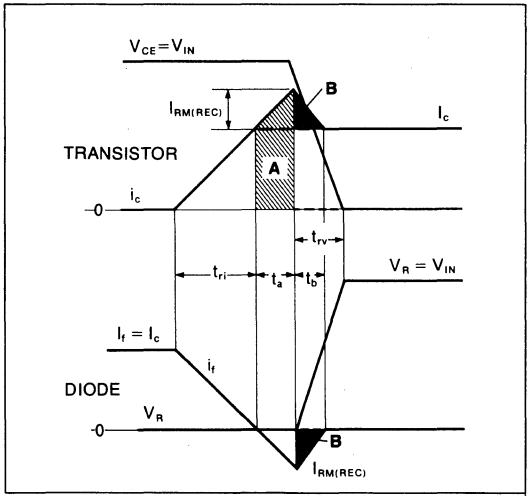


Figure B-5

Diode recovery time component t_a effectively increases transistor rise time, and delays the voltage transition, t_{rv}. During time t_a, the diode conducts reverse current but remains a low impedance. Transistor V_{CE} remains equal to V_{in} while collector current continues to rise above I_C to $I_C + I_{RM(REC)}$. The entire amount of charge shown in shaded area A results in increased switching loss in the *transistor only* (increase in diode loss is negligible):

$$(B3)\ P_{(t_a)} = V_{in}\left(I_C + \frac{I_{RM(REC)}}{2}\right)\frac{t_a}{\tau}$$

$$(B4)\quad t_a = t_{ri}\left(\frac{I_{RM(REC)}}{I_c}\right)$$

$$(B5)\ P_{(t_a)} = V_{in}\left(I_c + \frac{I_{RM(REC)}}{2}\right)\left(\frac{t_{ri}}{\tau}\ \frac{I_{RM(REC)}}{I_c}\right)$$

$$(B6)\ P_{(t_a)} = V_{in} \cdot I_{RM(REC)}\left(I + \frac{I_{RM(REC)}}{2I_c}\right)\frac{t_{ri}}{\tau}$$

If diode $I_{RM(REC)}$ is half of I_C (1.5:1 current overshoot in transistor) total transistor switching losses during current turn-on ($t_{ri} + t_a$) will be 2.25 times greater than with an ideal diode (Eq. B1).

During diode recovery time component t_b, the diode continues to conduct reverse current, but becomes a high impedance, permitting the transistor voltage transition, t_{rv}, to take place. Diode reverse current during t_b causes increased switching losses in the transistor and/or the diode. It is difficult to quantify these losses in the diode and transistor separately, since transistor V_{CE} is decreasing and diode V_R is increasing during all or part of period t_b. However, the total increase in losses in both diode and transistor during t_b is:

$$(B7)\ P_{(t_b)} = V_{in} \cdot \frac{I_{RM(REC)}}{2} \cdot \frac{t_b}{\tau}$$

$$(\text{area B} = \frac{I_{RM(REC)}}{2} \cdot t_b)$$

Note: $P_{(t_b)}$ loss is in *addition* to the ideal diode case transistor losses, $P_{(t_{rv})}$ (Eq. B2). With a very fast diode, t_b will be much shorter than t_{rv}, and most of the $P_{(t_b)}$ loss will occur in the transistor, although it will be negligible. With a slow diode, where t_b is much longer than t_{rv}, $P_{(t_b)}$ loss will be significant and will occur mostly in the diode.

$P_{(t_a)}$ is usually much greater than $P_{(t_b)}$. Since all of $P_{(t_a)}$ is dissipated in the transistor, it can be seen that most of the increased switching losses caused by diode reverse recovery are borne by the switching transistor, not by the rectifier.

Appendix C
Forward Recovery Behavior and Characterization

When used in some circuits, any diode may exhibit the phenomenon known as forward recovery. Under these conditions, the device has an impedance which, for a short time after initial application of forward current, is higher than its normal "on" value. The magnitude and duration of this transient impedance will depend on circuit conditions and device design, varying from no effect in many circuits to a few microseconds in the worst case. When present, the effect is generally less with fast-recovery rectifiers, and much less with "computer-type" switching diodes.

Circuits with very fast current rise time, in the direction of forward conduction, will allow this phenomenon to appear. Generally, these will be low-inductance circuits which allow the current to rise from zero to rated forward current in less than the reverse recovery time for fast stud-mounted rectifiers, and in less than $0.1 \times t_{rr}$ for lead mounted fast devices.

When such a source has a high voltage, of at least 10 times V_F, the forward recovery phenomenon exhibits an initial higher-than-steady-state forward voltage. The rise time of current is not limited by the diode and the peak voltage decays to the specified measurement level in the "forward recovery time" t_{fr}. The peak voltage $V_{F(DYN)}$ will be strongly influenced by the current rise time di/dt, and current I_F.

When a fast-rise source has an open circuit (compliance) voltage of less than several times the diode V_F, the forward recovery phenomenon may exhibit a delay in the rise of forward current. In this case the peak diode voltage is limited by the source, and the "turn-on" time is the rise time to 90% of I_F.

A comparison of the Unitrode UES 803 with a typical 200 nS rectifier is shown in Table II below.

Test Condition	Unitrode UES 803		DO5 200 nS	
	$V_{F(DYN)}$ (v)	t_{fr} (nS)	$V_{F(DYN)}$ (v)	t_{fr} (nS)
I_F to 1A in 8 nS	1.2	20	12	300
I_F to 1A in 125nS and continuing to 50A with $t_r = 10\mu S$	0.9	—	2.8	350

Table II

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FLYBACK AND BOOST SWITCHING REGULATOR DESIGN GUIDE

Section One – Flyback Regulator

I. Definition

The flyback switching regulator described in this application note accepts a DC voltage input and provides a regulated output voltage of opposite polarity. This method of conversion, compared to a conventional DC to DC converter, provides advantages of high efficiency, low cost, circuit simplicity, and a rather wide, easily selectable choice of the regulated output voltage. The switching transistor is not stressed to second breakdown in either the forward or reverse bias modes. Thus, it provides a reliable method of converting the input voltage. The disadvantage of the flyback switching regulator described here is that it provides no isolation and requires a large output filter capacitor. Primary usage of this type of regulator is in low current and/or high voltage applications.

II. Design Approaches to Flyback Regulator

The principal difference between a flyback regulator and a buck regulator (Ref. Unitrode Design Guide U-68) is the manner in which energy is transferred to the output capacitor. In a buck regulator, energy is provided continuously, while in a flyback regulator, energy is pumped in a discontinuous fashion. The flyback regulator can be operated in two modes.

A. Continuous Mode (see Figure 1a)

In this mode of operation, a large inductor is required to insure that the inductor current never goes to zero. Although the current through the inductor flows continuously, the charging current to the filter capacitor is in the form of discontinuous current pulses. This large peak-to-peak current waveform requires a much larger filter capacitor than the buck regulator. Component cost is higher than with the discontinuous mode of operation because of the large inductance required, and transient response is worse.

B. Discontinuous Mode (see Figure 1b, 1c)

In this mode, the regulator is designed such that at maximum output load current and minimum input voltage, the transistor starts conducting as soon as the catch diode stops conducting. At a lower output current or higher input voltage there is a dead time when neither device conducts.

The output voltage can be regulated by varying the duty cycle of the transistor switch.

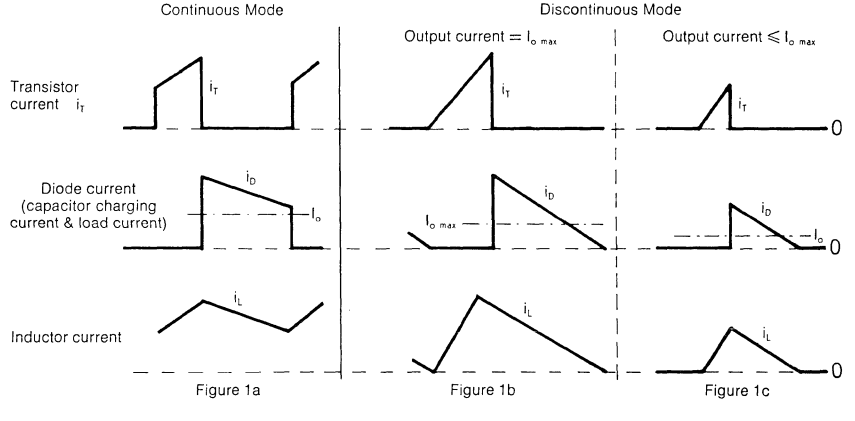

Figure 1. Current Waveforms

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III. The Flyback Switching Regulator Described and Characterized

The basic circuit configuration and generalized current waveforms are shown in Figure 2. When transistor Q_1 is turned on, the supply voltage, E_{IN}, is applied across power inductor L. The current through the inductor rises linearly to a peak current level I_p:

$$I_p = \frac{E_{IN} \times t_T}{L} \quad \text{.....A.}$$

This results in an energy transfer from the input supply to the power inductor:

$$W = \frac{1}{2} L I_p^2 \quad \text{.....B.}$$

When the transistor turns off, a voltage is induced across inductor L which forces the current to flow through diode D_1. All of the energy stored in the inductor is transferred to the output capacitor and load R_L, and the inductor current diminishes linearly from I_p to zero according to the relationship:

$$I_p = \frac{E_o \times t_D}{L} \quad \text{.....C.}$$

The power delivered to the load is equal to the peak energy stored in the inductor times the number of pump cycles per second:

$$P_{out} = E_o \times I_o = \frac{1}{2} L I_p^2 \times f \quad \text{.....D.}$$

The voltage induced in the inductor is such that E_o is opposite in polarity from E_{IN}. The relationship between E_o and E_{IN} is established by combining equations A and C, eliminating I_p and L:

$$\frac{E_o}{E_{IN}} = \frac{t_T}{t_D} \quad \text{.....E.}$$

DC output current I_o is equal to the average current through the diode:

$$I_o = \frac{I_p}{2} \times \frac{t_D}{\tau} = \frac{I_p}{2} \times t_D \times f$$

The output voltage can be regulated by operating at a fixed frequency and varying the transistor on time, t_T. However, because of the inherent "pumping" action of the flyback regulator, the output voltage diminishes while the switching transistor is on, and increases when the transistor is off. This characteristic makes it difficult to control on a fixed frequency basis.

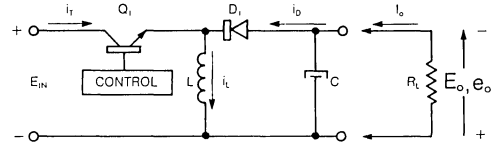


Figure 2a. Flyback Switching Regulator

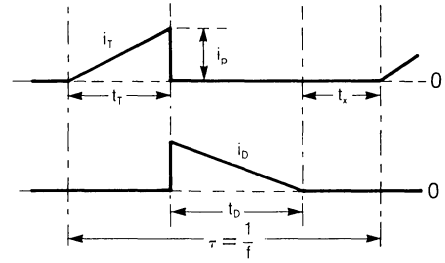
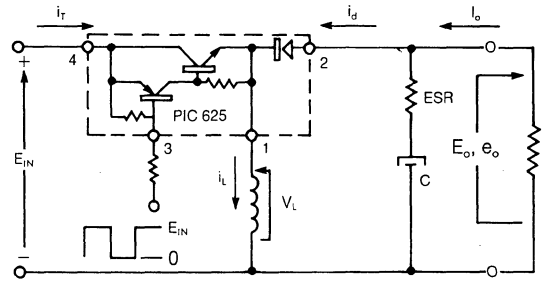


Figure 2b. Generalized Current Waveforms of a Flyback Switching Regulator

The simplest approach to controlling the flyback regulator in the discontinuous mode is to establish a fixed peak current through the inductor, which determines a fixed diode conduction time, t_D. Frequency then varies directly with output current, and transistor on-time varies inversely with input voltage. This is the approach used in this application note, resulting in a simple and economical control circuit.

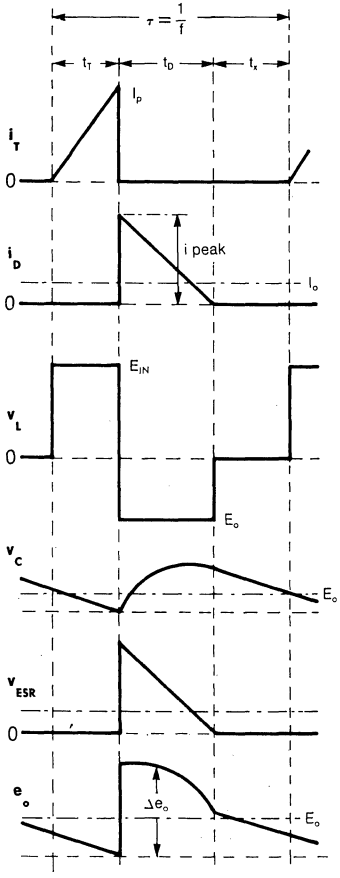
IV. Worst Case Design Conditions

Design equations based on the fixed peak current mode of operation are shown in Figure 3. The worst case condition exists when input voltage is low while output current is at maximum. Under these worst case conditions, frequency is maximum and t_x is zero because the pass transistor turns on as soon as diode stops conducting.



GIVEN:
- $E_{IN\ (min)}$
- E_o
- $I_{o\ (max)}$
- f_{max}
- Δe_o

WORST CASE:
- $E_{IN} = E_{IN\ (min)}$
- $I_o = I_{o\ (max)}$
- $t_x = 0$



$$I_p = 2\ I_{o\ max}\ (E_o/E_{IN\ (min)} + 1) = \text{constant}$$

$$t_D = \frac{1}{f_{max}\ (E_o/E_{IN\ (min)} + 1)} = \text{constant}$$

$$L = \frac{t_D \times E_o}{I_p} = \frac{t_T \times E_{IN}}{I_p}$$

$$f = \frac{1}{\tau} = f_{max}\ \frac{I_o}{I_{o\ (max)}}$$

$$C_{min} = \frac{I_p \times t_D}{2\ \Delta e_o}$$

(worst case $I_o \rightarrow 0$)

$$ESR_{max} = \frac{\Delta e_o}{I_p}$$

Figure 3. Flyback Regulator

V. Circuit Design and Description

In designing a flyback switching regulator power supply, the following parameters will normally be predefined. Numerical values are given and computed for the example shown in Figure 4.

E_o = 5V output
Δe_o = 100 mV output ripple voltage peak to peak
$I_o max$ = 2.5A
$E_{IN} min$ = 9V (minimum)
$E_{IN} max$ = 15V (maximum)

Since the output voltage is derived from pulses of current, it is desirable to keep the operating frequency as high as possible in order to obtain small size and lower cost of the filter inductor and capacitor. However, above 5-10 kHz, capacitor impedance is usually dominated by its equivalent series resistance, ESR, rather than C value. Since the ESR remains essentially constant regardless of operating frequency, operation at higher frequencies does not enable the size and cost of the capacitor to be further reduced.

Also, at higher frequencies, transistor switching losses become significant. Thus, a maximum operating frequency of 25 kHz is chosen for this design.

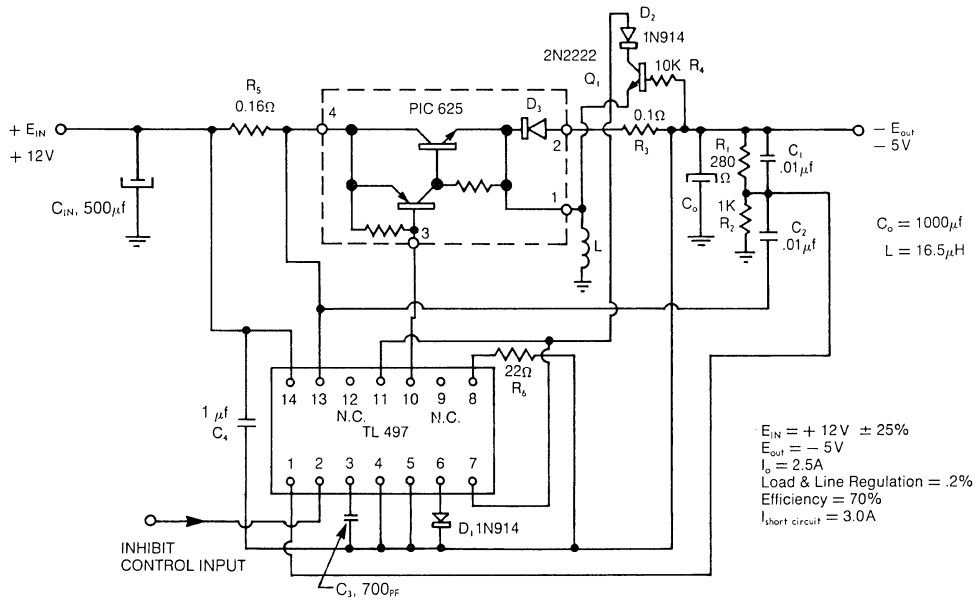


Figure 4. Flyback Regulator, +12V Input, −5V Output

Referring to Figure 3, the design calculations are:

$$I_p = 2\, I_o max\, (E_o/E_{IN} min + 1) = 2 \times 2.5\, (5/9 + 1)$$

$$= 7.8A \text{ (constant)}$$

$$t_D = \frac{1}{f_{max}\,(E_o/E_{IN} min + 1)} = \frac{1}{25 \times 10^3\,(5/9 + 1)}$$

$$= 25.7\ \mu s \text{ (constant)}$$

$$L = \frac{t_D \times E_o}{I_p} = \frac{25.7 \times 10^{-6} \times 5}{7.8}$$

$$= 16.47\ \mu H$$

$$C_{min} = \frac{I_p \times t_D}{2\,\Delta e_o} = \frac{7.8 \times 25.7 \times 10^{-6}}{2 \times 0.1}$$

$$= 1002\ \mu F$$

$$ESR_{max} = \frac{\Delta e_o}{I_p} = \frac{0.1}{7.8} = 0.0128\,\Omega$$

The operating frequency will change in proportion to load current, I_o:

$$f = f_{max} \times \frac{I_o}{I_{o\ max}}$$

The PIC625 hybrid power output stage incorporates a fast PNP quasi-darlington switching transistor and UES catch diode. The quasi-darlington switch requires 30 mA of drive current. This drive current is provided with diode D_1 and Resistor R_6 in conjunction with the Integrated circuit TL497. (Refer to Figure 4)

$$I_{DRIVE} = \frac{V_{be}}{R_6} = \frac{0.65}{R_6}$$

$$\therefore\ R_6 = 22\,\Omega$$

The output voltage is preset by divider network R_1 and R_2, according to the relationship:

$$E_o = \left[1 + \frac{R_2}{R_1}\right] V_{REF}$$

where $V_{REF} = 1.22V$. Assuming a nominal value for $R_2 = 1K$, then:

$$R_1 = 320\,\Omega$$

R_1 may be trimmed to obtain the precise output voltage.

The TL497 control circuit operates in the current limiting mode under normal operating condition. Thus, the peak current value, I_p, is determined by the current limiting resistor R_5. Capacitor C_3 is required to prevent the TL497 from terminating the transistor on-time prematurely. This causes an 8 μs delay, once over-current is detected at the short circuit sense input (pin 13 of TL497) before the transistor switch turns off. The delay time is the time required to charge capacitor C_3 to the predetermined voltage level before drive current to the pass transistor is removed. The current limit threshold voltage is about 1.2 volts.

$$R_5 = \frac{1.2V}{I_p}$$

$$= \frac{1.2}{7.8A}$$

$$= 0.153\,\Omega$$

The function of transistor Q_1, diode D_3 and resistor R_3 and R_4 is to provide short circuit protection. The transistor Q_1 prevents turn-on of the pass transistor as long as the catch diode continues to conduct. Thus, it limits the maximum current and operating frequency under short circuit conditions. D_2 and R_4 providing voltage isolation to transistor Q_1.

C_2 is required for circuit stabilization; capacitor C_1 provides AC coupling of ripple voltage to the control circuit. C_{IN} and C_o are filter capacitors.

Unitrode Switching Regulator Design Guide U-68 covers the design of a buck regulator, and contains a section on power inductor design which is applicable to the flyback and boost regulators.

Section Two — Boost Switching Regulator

The boost switching regulator is described briefly in this application note. It accepts a DC voltage input and provides a regulated output voltage which must be greater than input voltage.

The basic circuit configuration of a boost regulator is shown in Figure 5. When the transistor switch is turned on, the supply voltage E_{IN} is applied across power inductor L. The diode is reverse biased by voltage E_o. Energy is transferred from the input supply to the power inductor. When the transistor is turned off, the energy stored in the inductor L induces a voltage such that the diode conducts and transfers the energy to the load and the output capacitor. In addition to the energy stored in the inductor, additional energy is transferred from the input directly to the output during the diode conduction time.

This pumping action, similar to the flyback regulator, also makes it desirable to operate the boost regulator in the discontinuous mode with a fixed peak current through the inductor. However, unlike the flyback regulator, in the boost regulator the diode conduction time is not fixed, but varies according to the input voltage:

$$t_D = \frac{L\, I_p}{E_o - E_{IN}}$$

Output voltage is regulated by controlling the duty cycle:

$$\frac{E_o}{E_{IN}} = \frac{t_T}{t_D} + 1$$

Since the ripple voltage across the output capacitor is directly proportional to diode conduction time, t_D, capacitor requirements are determined by the maximum t_D:

$$t_D \text{ max} = \frac{L\, I_p}{E_o - E_{IN}\,(\text{max})}$$

The Figure 6 is a complete schematic diagram of a boost switching regulator. It accepts +12V of DC input voltage and provides regulated +24V of output voltage.

The design procedure and circuit description is similar to the flyback switching regulator.

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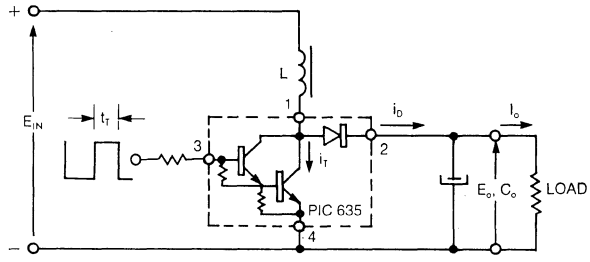
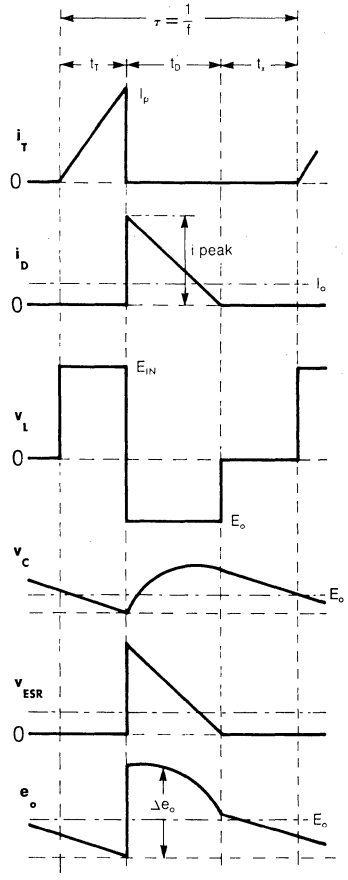


GIVEN:
- $E_{IN\ (max)}$
- $E_{IN\ (min)}$
- E_o
- $I_{o\ (max)}$
- $f_{(max)}$
- Δe_o

WORST CASE:
- $E_{IN} = E_{IN\ (min)}$
- $I_o = I_{o\ (max)}$
- $t_x = 0$



$$I_p = 2\, I_{o\ max}\, (E_o/E_{IN\ (min)}) = \text{constant}$$

$$t_{D\ (min)} = \frac{1}{f_{max}\, (E_o/E_{IN\ (min)})}$$

$$L = \frac{t_{D\ (min)}\, (E_o - E_{IN\ min})}{I_p}$$

$$f = \frac{1}{\tau} = f_{max}\, \frac{I_o}{I_{o\ (max)}} \times \frac{E_o - E_{IN}}{E_o - E_{IN\ (min)}}$$

$$C_{min} = \frac{I_p \times t_{D\ max}}{2\, \Delta e_o}$$

(worst case $I_o \rightarrow 0$)

$$ESR_{max} = \frac{\Delta e_o}{I_p}$$

Figure 5. Boost Regulator

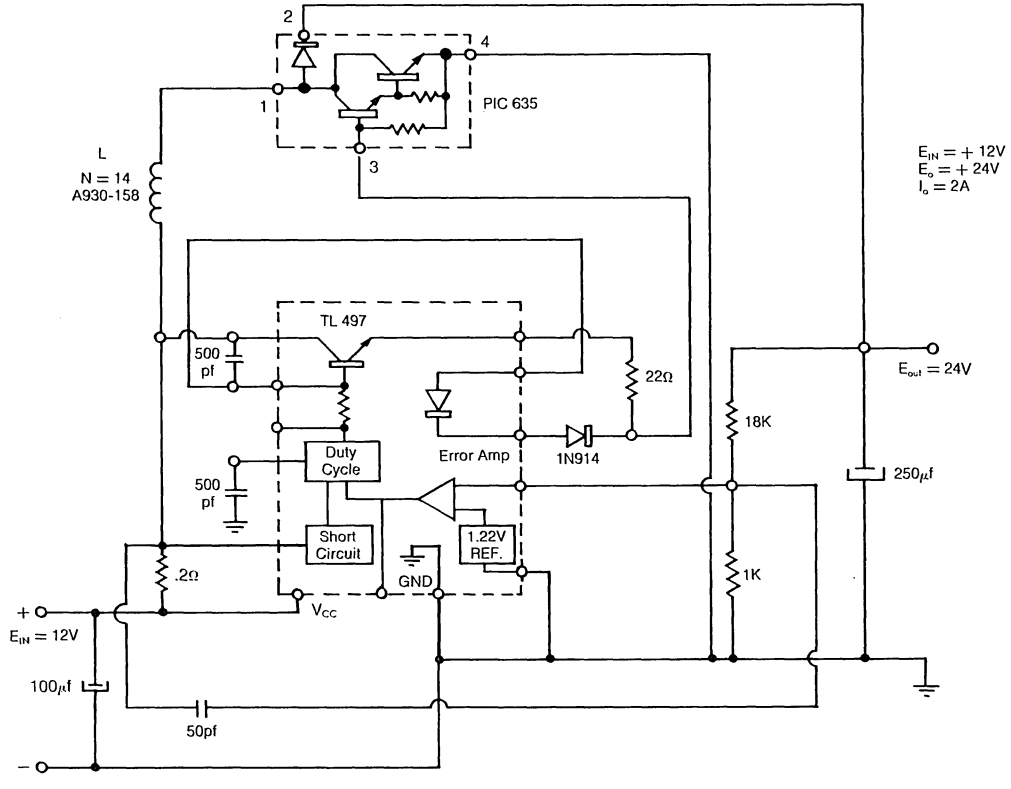


Figure 6. Boost Switching Regulator

Appendix A — Derivation of Design Equations

The basic circuit configuration of the flyback switching regulator is shown in Figure 3. Assuming a fixed value of peak current, I_p, and output volts, E_o, the following equations are evident:

$$E_{IN}\, t_T \doteq E_o\, t_D = I_p \times L \quad \text{.....1.}$$

$$t_T = t_D \times E_o / E_{IN} \quad \text{.....1a.}$$

$$\tau = t_T + t_D + t_X = 1/f \quad \text{.....2.}$$

Worst case $\tau = \tau_{min}$, $f = f_{max}$, $t_X = 0$, $E_{IN} = E_{IN}$ min. Substituting Equation 1a:

$$\tau_{min} = \frac{1}{f_{max}} = t_D\,(E_o/E_{IN}\,\text{min} + 1) \quad \text{.....2a.}$$

$$\therefore\ t_D = \frac{1}{f_{max}\,(E_o/E_{IN}\,\text{min} + 1)} \quad \text{.....2b.}$$

Since in Equation 1, E_o, I_p and L are all constant values for a given application, t_D is also a constant value.

By inspection of Figure 3 output current waveforms:

$$I_o = \frac{I_p}{2} \times \frac{t_D}{\tau} = \frac{I_p}{2} \times t_D \times f \quad \text{.....3.}$$

Taking worst case conditions and substituting Equation 2b:

$$I_o\,\text{max} = \frac{I_p}{2} \times f_{max} \times \frac{1}{f_{max}\,(E_o/E_{IN}\,\text{max} + 1)} \quad \text{.....3a.}$$

$$\therefore\ I_p = 2\, I_o\,\text{max}\,(E_o/E_{IN}\,\text{max} + 1) \quad \text{.....3b.}$$

Rearranging Equation 1:

$$L = \frac{t_D \times E_o}{I_p} \quad \text{.....1b.}$$

The ripple voltage, Δv_c, across the output filter capacitor:

$$\Delta v_c = \frac{\Delta Q}{C} \quad \text{.....4.}$$

The worst case net charge into the capacitor is equal to the area under the diode current waveform

$$\Delta Q_{max} = \frac{I_p \times t_D}{2} \quad \text{.....4a.}$$

Substituting into Equation 4 and rearranging:

$$\therefore\ C_{min} = \frac{I_p \times t_D}{2\,\Delta e_o} \quad \text{.....4b.}$$

The ripple voltage, v_{ESR} across the capacitor series resistance, ESR.

$$v_{ESR} = I_p \times \text{ESR} \quad \text{.....5.}$$

$$\therefore\ \text{ESR}_{max} = \frac{\Delta e_o}{I_p} \quad \text{.....5a.}$$

The frequency, f, will vary as a function of load current. Rearranging Equation 3:

$$\frac{I_o}{f} = \frac{I_p}{2} \times t_D = I_o\,\text{max}/f_{max} \quad \text{.....6.}$$

$$\therefore\ f = f_{max} \times \frac{I_o}{I_{o\ max}} \quad \text{.....6a.}$$

and

$$f_{min} = f_{max} \times \frac{I_{o\ min}}{I_{o\ max}}$$

THERMAL DESIGN CONSIDERATIONS FOR OPERATING UNITRODE'S TO-92 TRANSISTORS AND DARLINGTONS IN PULSED-POWER APPLICATIONS

Introduction

Unitrode's power Darlingtons (U2TA506, U2TA508, U2TA510) and power transistors (UPTA510, UPTA520, UPTA530 and UPTB520, UPTB530, UPTB540, UPTB550) in economical TO-92 plastic packages are ideally suited for use in pulsed power applications, such as lamp driving or printer driving where the inrush or pulse drive current can be as high as several amperes. When compared with transistors or Darlingtons in conventional power packages, the Unitrode TO-92 devices offer cost savings of 50% or more, take up significantly less board space, and lend themselves to tape and reeling and automatic insertion. They also offer the advantage of a maximum operating junction temperature ($T_{J(max)}$ of 175°C versus 150°C or 125°C) for other plastic packaged devices.

Thermal considerations are of prime concern when the TO-92 power transistors and Darlingtons are used in pulsed power applications. This Design Guide provides a method for determining the junction temperature and maximum allowable peak power dissipation for the U2TA506, U2TA606 and the UPTA510 and UPTB520 series when they are operated at frequencies of 10kHz or less, where the switching losses are negligible and can be ignored. This method is valid for the vast majority of pulse applications.

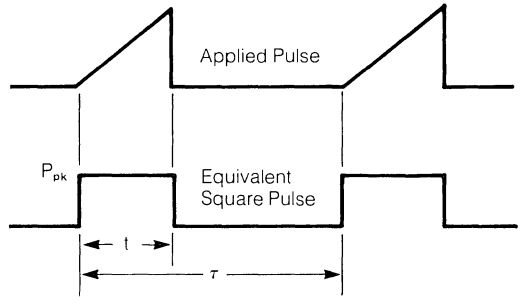
Thermal Analysis

A detailed transient thermal analysis is required to determine the peak junction temperature and maximum allowable power dissipation since the junctions of the transistor or Darlington are subjected to temperature excursions due to the applied, periodic power pulses.

A) Effective Pulsed Thermal Impedance

The effective pulsed thermal impedance (Θ_p) of a device subjected to a periodic train of power pulses can be calculated as follows:

$$\Theta_p = (\Theta_{j\text{-}A})(D) + (1-D)(r(t+\tau)) - r(\tau) + r(t) \quad \ldots\ldots\ldots (1)$$



Where: t = pulse width
τ = period
D = t/τ (Duty Cycle)
$r(t+\tau)$ = transient thermal impedance at time $t + \tau$
r(t) = transient thermal impedance at time t
$\Theta_{j\text{-}A}$ = DC junction to ambient thermal impedance
P_{pk} = The peak power of a square power pulse with equivalent energy to that of the actual power pulse.

Figure 1. Power Pulses

The DC junction to ambient thermal impedance ($\Theta_{j\text{-}A}$) is 200°C/W maximum for the UPTA510 and UPTB520 series and is 155°C/W maximum for the U2TA506 series.

The transient thermal impedance for the U2TA506, UPTA510 and UPTB520 series can be obtained from the curves presented in Figure 2:

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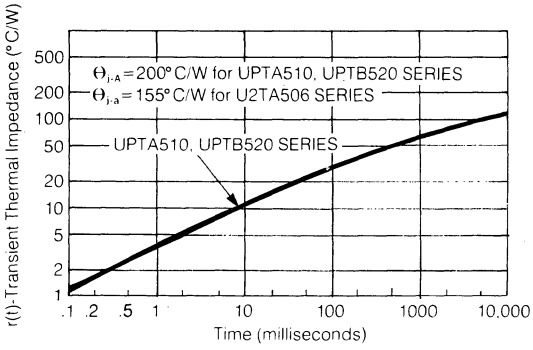


Figure 2. Junction to Ambient Transient Thermal Impedance

B) Peak Junction Temperature

The peak junction temperature of a device subjected to a periodic train of power pulses can be calculated using the previously derived effective pulsed thermal impedance as follows:

$$T_{j\,(peak)} = T_{Ambient} + (P_{pk})(\Theta_p) \quad \ldots\ldots\ldots\ldots\ldots (2)$$

In the case of a single shot pulse the term for Θ_p reduces to

$$\Theta_p = r(t)$$

and the equation used to calculate peak junction temperature becomes

$$T_{j\,(peak)} = T_{Ambient} + (P_{pk})(r(t)) \quad \ldots\ldots\ldots\ldots\ldots (3)$$

Allowable Peak Power Dissipation

The allowable peak power dissipation can be derived from the following equation:

$$P_{pk(max)} = \frac{T_{j\,(max)} - T_{Ambient}}{\Theta_p} \quad \ldots\ldots\ldots\ldots\ldots (4)$$

Where $T_{J(max)}$ is the maximum allowable junction temperature. For the U2TA506, UPTA510 and UPTB520 series the maximum junction temperature is 175°C.

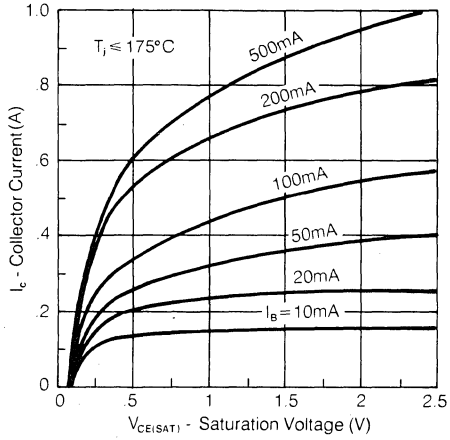


Figure 4. UPTA510 Series. Maximum Saturation Voltage vs. Collector Current

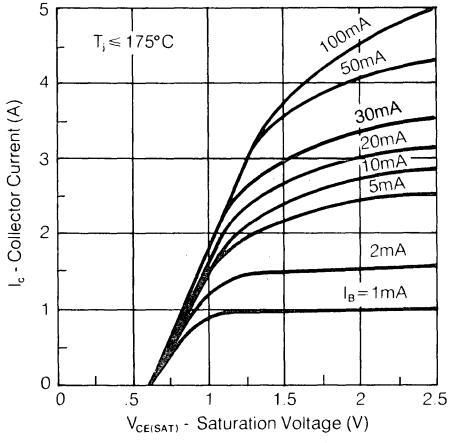


Figure 3. U2TA506 Series. Maximum Base to Emitter Saturation Voltage vs. Collector Current

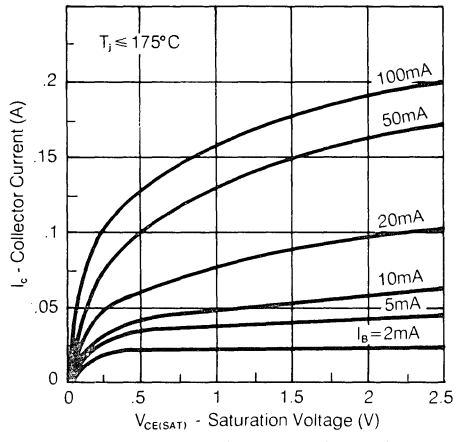


Figure 5. UPTB520 Series Maximum Saturation Voltage vs. Collector Current

Peak Power

The peak power can be expressed as follows:

$$P_{pk}=(V_{CE\,(SAT)})\,(I_{pk}) + (V_{BE\,(SAT)})\,(I_B) \quad \ldots\ldots\ldots\ldots (5)$$

Where I_{pk} is the peak collector current of a square pulse of current equivalent to the applied current pulse, $V_{CE(SAT)}$ is the transistor or Darlington saturation voltage at I_{pk}, $V_{BE(SAT)}$ is the base-to-emitter saturation voltage and I_B is the base current. Figures 3, 4, and 5 are plots of $V_{CE(SAT)}$ for the U2TA506, UPTA510 and UPTB520 series Darlingtons and transistors. Figures 6 and 7 are plots of the $V_{CE(SAT)}$. These curves can be used in determining P_{pk}.

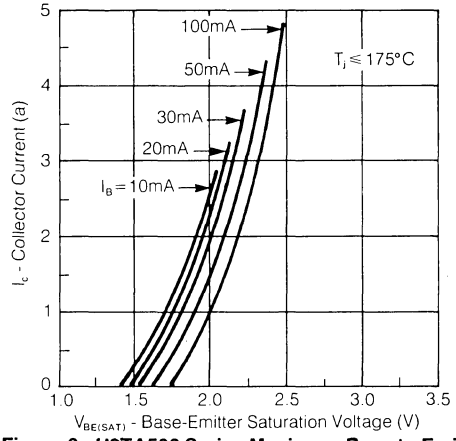


Figure 6. U2TA506 Series Maximum Base to Emitter Saturation Voltage vs. Collector Current

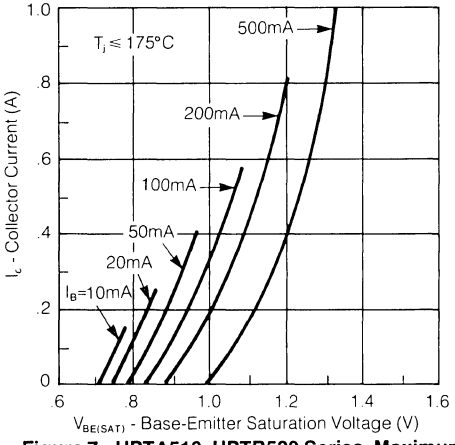


Figure 7. UPTA510, UPTB520 Series. Maximum Base to Emitter Saturation Voltage vs. Collector Current

Design Examples

1. An incandescent lamp is controlled by a U2TA506 Darlington operating from a 12V battery. When switched on the lamp draws an inrush current of 3A which decays exponentially to a steady-state value of 300mA. The time constant of the inrush current is 50 milliseconds and the worst case ambient temperature is 55°C. The Darlington's base drive is 30mA dc.

   Problem:
   Calculate the peak junction temperature due to the inrush pulse and the steady-state junction temperature.

   Solution:
   The inrush current can be approximated by a square wave of 3A peak and 50 milliseconds duration. The equivalent square pulse of current will have the same energy as the exponential pulse if the $V_{CE(SAT)}$ of the Darlington is assumed to remain constant. Since the $V_{CE(SAT)}$ will actually drop as the inrush current exponentially decays, the result obtained from using the square wave approximation will be conservative.

   Using equations (3) and (5)

   $$T_{j(peak)} = T_{Ambient} + (P_{pk})(r(t)) \quad \ldots\ldots\ldots\ldots (3)$$

   Where: $T_{Ambient}$ = 55°C
   r (t) = r(50mSec) = 17.5°C/W (from Figure 2)
   P_{pk} = $(V_{CE(SAT)})\,(I_{pk}) + (V_{BE(SAT)})\,(I_B) \ldots$ (5)
   = (1.5V) (3A) + (2.15V) (30mA)
   (from Figures 3 and 6)
   = 4.56W

   Therefore:

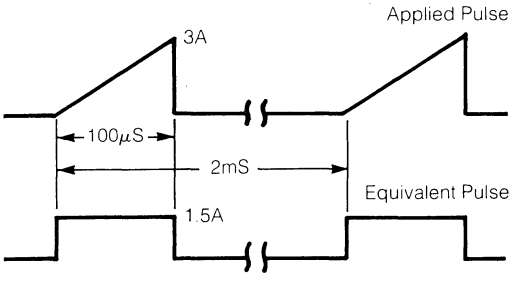
   $$T_{j(peak)} = 55°C + (4.56W)\,(17.5°C/W) = 135°C$$

   Since 135°C is 40°C less than the maximum operating junction temperature for the U2TA506 ($T_{j(max)}$ = 175°C), the Darlington is operating well within its rating.

   The Steady-state junction temperature can be determined as follows:

   $T_{j(ss)} = (P_{(ss)})\,(\Theta_{j\text{-}A}) + T_{Ambient}$
   = ((.3A)(.73V) + (.03A)(1.60V)) (155°C/W) + 55°C
   = 96°C

2. A U2TA508 is used to drive a solenoid load in an impact printer. The collector current waveform is as shown below along with the equivalent square pulse:



The Darlington is switching in a clamped mode so the energy stored in the solenoid inductance during the on-time is dissipated in the clamp and not in the Darlington. The maximum ambient temperature is 80°C and the base drive current is 20mA.

Problem:
Find the worst case junction temperature and determine if it is within the maximum rating of the U2TA508.

Solution:
Use equation (1) to determine Θ_p

$\Theta_p = (\Theta_{j\text{-}A})(D) + (1-D)(r(t+\tau)) - r(\tau) + r(t)$ .....(1)

$\Theta_{j\text{-}A} = 155°C/W$ (from Figure 2)

$D = \frac{.1mSec}{2mSec} = .05$

$r(t+\tau) = r(2.1mSec) = 4.2°C/W$ (from Figure 2)

$r(\tau) = r(2mSec) = 4.1°C/W$ (from Figure 2)

$r(t) = r(.1mSec) = 1.1°C/W$ (from Figure 2)

Therefore:

$\Theta_p = (155°C/W)(.05) + (.95)(4.2°C/W) - 4.1°C/W + 1.1°C/W$

$= 8.75°C/W$

Using equation (5)

$P_{pk} = (V_{CE(SAT)})(I_{pk}) + (V_{BE(SAT)})(I_B)$ ..... (5)

$I_{pk} = 1.5A$

$V_{CE(SAT)} + 2V$ (from Figure 3)

(The $V_{CE(SAT)}$ value at 3A was chosen to give a conservative answer. If T_j is found to be greater than 175°C it may be necessary to recompute using a closer approximation of the actual $V_{CE(SAT)}$ which varies as the current increases from 0 to 3A.)

$I_B = 20mA$

$V_{BE(SAT)} = 2.1V$ (from Figure 6)

(Again the $V_{BE(SAT)}$ value at 3A was chosen to give a conservative result.)

Therefore:

$P_{pk} = (2V)(1.5A) + (2.1V)(.02A) = 3.04W$

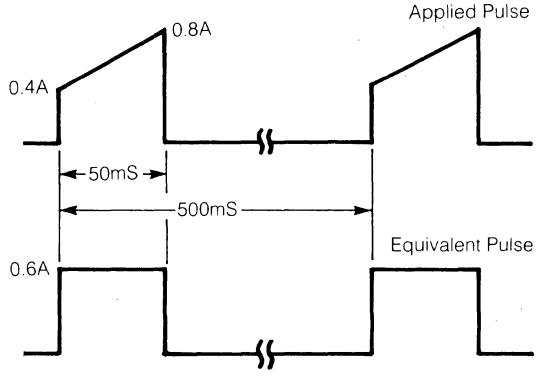
Now T_j can be determined from equation (2)

$T_j = T_{ambient} + (P_{pk})(\Theta_p)$ ..... (2)

$= 80°C + (3.04W)(8.75°C/W) = 107°C$

This is well within the maximum rating of 175°C for the U2TA508.

3. A UPTA530 is used to drive a high voltage DC motor in a display application the current waveform as is shown below:



The base drive is 200 mA and the worst case ambient temperature is 65°C.

Problem:
Determine the junction temperature to insure it is within the maximum rating of 175°C for the UPTA530.

Solution:
Using Equation (1)

$\Theta_p = (200°C/W)(.1) + (.9)(52°C/W) - 50°C/W + 21°C/W$

$= 37.8°C/W$

From equation (5) and Figures 4 and 7.

$P_{pk} = (2.3V)(.6A) + (1.2V)(.2A) = 1.6W$

(Again $V_{CE(SAT)}$ and $V_{BE(SAT)}$ values at .8A rather than .6A were used to insure a conservative answer).

Therefore, from equation (2)

$T_j = 65°C + (1.6W)(37.8°C/W) = 126°C$

It becomes readily apparent from these examples that Unitrode's TO-92 transistors and Darlingtons can be operated with significant safety margin in a wide variety of pulsed-power applications.

GUIDELINES FOR USING TRANSIENT VOLTAGE SUPPRESSORS

1.0 Introduction

During transient periods, system voltages and currents are often many times greater than their steady-state values. These transients must be considered in overall electronic systems design to insure required circuit performance and reliability both during and after the transient.

Transients may result from a variety of causes. The most common of these are: normal switching operations (power supply turn-on and turn-off cycles), routine AC line fluctuations, or abrupt circuit disturbances (faults, load switching, voltage dips, magnetic coupling by electro-mechanical devices, lightning surges, etc.). Voltage transients are a major cause of component failures in semiconductors. Random high voltage transient spikes can permanently damage these voltage sensitive devices and disrupt proper system operation. Catastrophic power supply conditions should not necessarily be the designer's prime concern, since lower level transients can cause improper operation of a system even though no component failures are caused. Normal power supply on-off cycles have the potential of emitting spikes with sufficient energy to destroy an entire semiconductor device chain. Any surviving devices are also suspect. Trouble shooting, isolating, and replacing damaged devices is time consuming and costly; especially when performed in the field.

Unitrode's TVS305 and TVS505 series of transient voltage suppressors (TVS) offer the designer significant price/performance advantages over other protection methods. Their miniature size permits simple "close-in" installation in applications where circuit boards are dispersed throughout one or more electronic racks. Dispersed usage aids system trouble shooting and affords transient voltage protection where internal system disturbances such as those caused by inductive load switching could occur.

In spite of their small size, the TVS305 and TVS505 suppressor series can dissipate 500 watts and 150 watts (respectively) of peak pulse power for 1 millisecond. Response time to transients is just about instantaneous — about 1×10^{-12} seconds. These devices perform to their data sheet specifications without significant degradation throughout their operating life. Unitrode has performed full power pulse life tests for 100,000 pulses with negligible change in characteristics. These devices are suitable for almost any equipment and environment.

2.0 Choosing the Correct Transient Voltage Suppressor for the Application

Certain critical terms must be defined before any discussion of "how to" choose the correct TVS.

1. Stand-Off Voltage (V_R) is the highest reverse voltage at which the TVS will be non-conducting.
2. Min. Breakdown Voltage (BV_{min}) is the reverse voltage at which the TVS conducts 1 mA. This is the point where the TVS becomes a low impedance path for the transient.
3. Max. Clamping Voltage (V_{Cmax}) is the maximum voltage drop across the TVS while it is subjected to the peak pulse current, usually for 1mS.

Figure 1 graphically shows all three terms.

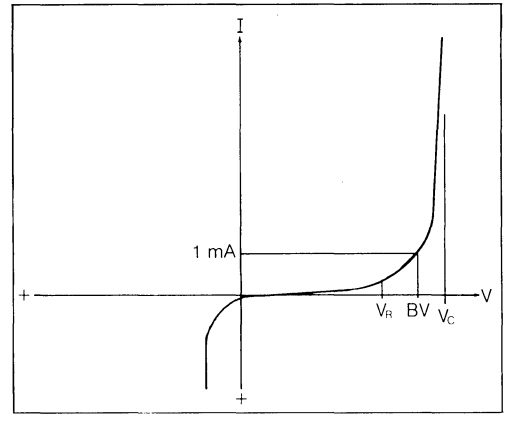


Figure 1 — TVS Characteristics

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2.1 Determining Pulse Power Levels

Since a zener TVS has an almost constant clamping voltage throughout a transient pulse, the transient pulse power (P_p) equals the peak pulse current (I_{pp}) multiplied by the clamping voltage (V_C).

$$P_p = V_C \times I_{pp}$$

2.2 Choosing the Appropriate Transient Voltage Suppressor

The three most important factors in choosing the appropriate TVS for your application, in their order of importance are:

1. Pulse power (P_p) — Choose the TVS series that will handle the Transient Pulse Power. To determine Transient Pulse Power use the simple equation in section 2.1. If I_{pp} is not known or measurable, it can be calculated — see Sections 3 and 4. The pulse duration vs. pulse power graph on the Unitrode TVS305/TVS505 data sheet can then be used to determine the TVS series that will handle the transient. This graph for the TVS505 series is shown in Figure 2.
2. Stand-off voltage (V_R) — From the TVS series selected, choose the device with the stand-off voltage equal to or greater than your normal circuit operating voltage. This insures that the TVS will draw a negligible amount of current from the circuit during normal circuit operation. The electrical specifications for the TVS505 series are shown in Figure 3.
3. Maximum Clamping Voltage (V_{Cmax}) — Determine the clamping voltage of the device chosen for the transient given and be sure it is below the voltage that might damage any components in the protected circuit. See Figure 3.

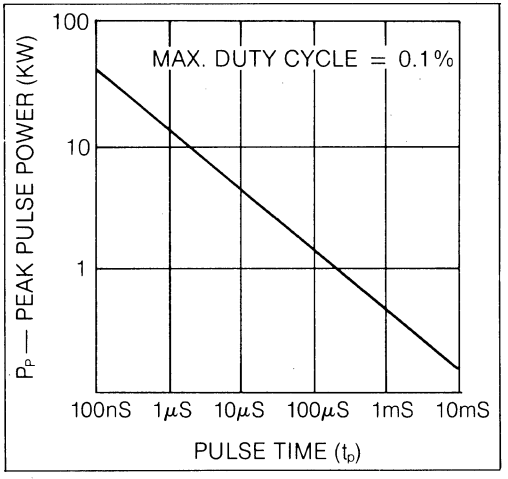

Figure 2 — Peak Pulse Power vs. Pulse Duration

TVS Part No.	Stand-off Voltage V_R	Min. Breakdown Voltage $BV_{(min)}$ @ 1mA	Max. Leakage Current I_R @ V_R	Max. Clamping Voltage V_C @ 1A	Max. Clamping Voltage V_C @ 5A	Max. Clamping Voltage V_C @ 10A	Max. Peak Pulse Current I_{pp}	Max. Clamping Voltage V_C @ I_{pp}
	V	V	μA	V	V		A	V
TVS505	5.0	6.0	300	7.4		7.9	53.7	9.3
TVS510	10.0	11.1	5	13.2		14.4	30.3	16.5
TVS512	12.0	13.8	5	16.5		18.5	23.8	21.0
TVS515	15.0	16.7	5	19.7		22.2	19.8	25.2
TVS518	18.0	20.4	5	23.8	26.0		16.3	30.5
TVS524	24.0	28.4	5	32.4	37.0		11.9	42.0
TVS528	28.0	30.7	5	35.9	41.0		10.7	46.5

Figure 3 — Electrical Specifications @ 25°C

If the actual pulse power and pulse width are different from those listed on the data sheet, the clamping voltage can be calculated. The actual calculation method is beyond the scope of this note. Instead, we offer a graphical approximation using Figure 4. The approximation is based on the ratio of the actual and rated pulse power.

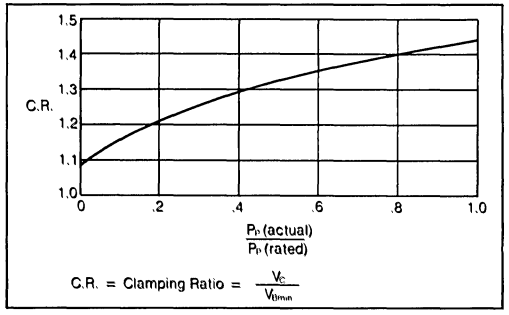

Figure 4 — Graphical Approximation for the Clamping Ratio

The procedure is as follows:

a. Calculate P_p (actual)$\approx 1.3BV_{min} I_{pp}$.
b. For P_p (rated) use value from TVS data sheet curve (See Fig. 2 for example).
c. Calculate P_p (actual)/P_p (rated).
d. Use Fig. 4 to find corresponding value of C.R.
e. Calculate V_C = C.R. × BV_{min}.

2.3 Installation Considerations

1. Locate the TVS as close to the device or circuit to be protected as possible.
2. Minimize the "common path" through the TVS to minimize voltage spikes produced by fast risetime transients in lead and wiring stray inductance. See Figure 5.

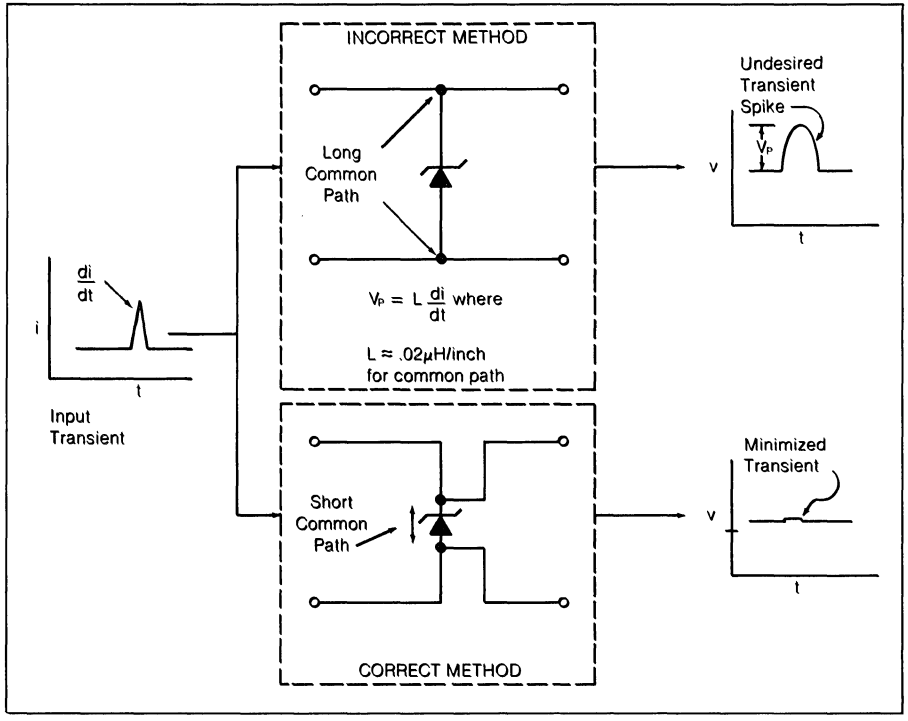

Figure 5 — Minimizing the Common Path

3.0 Transient Levels and Waveforms

3.1 Voltage, Current and Power Levels

Since TVS tests and specs may be written in terms of voltage, current or power levels, the relationships are shown in Figure 6 for (a) field conditions and (b) test conditions.

In addition to the magnitude of the voltage, current or power, the waveform or pulse width should be specified, as shown in Figure 7, for example.

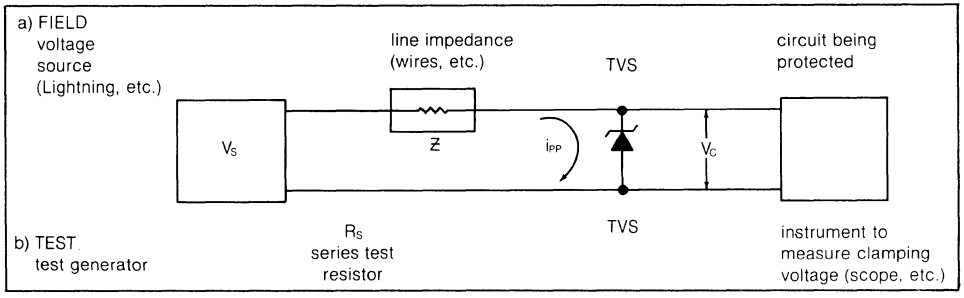

Figure 6 — Equivalent Circuit for Field and Test Conditions

3.2 Typical Transient Levels

Martzloff and Hahn in their paper on transients on 120 volt power lines* produced this table showing the surges recorded at a number of different locations over a two year period. The table indicates two primary causes of transients; load switching within the house and lightning storms.

Table 1*
Detailed Analysis of Recorded Surges

	Most Severe Surge			Most Frequent Surge				
House	Type†	Crest (volts)	Duration (μs or cycles)	1.5mHz Type†	Crest (volts)	Duration (μs or cycles)	Average Surges per Hour	Remarks
1	A-1.5	700	10 μs	A-1.5	300	10 μs	0.07	
2	A-2.0	750	20 μs	A-2.0	500	20 μs	0.14	fluorescent light
3	B-0.5	600	1 cycle	B-0.5	300	1 cycle	0.05	switching
4	B-0.5	400	2 cycles	B-0.5	300	2 cycles	0.2	
5	C	640	5 μs	too few to show typical			10 total	
6	B-0.3	400	1 cycle	B-0.3	250	1 cycle	0.01	
7	B-1	1800	1 cycle	B-1.0	800	1 cycle	0.03	lightning storm
8	C	1200	10 μs	B-0.5	300	4 cycles	0.1	
9	B-0.25	1500	1 cycle	same as most severe			0.2	oil burner
10	B-0.25	2500	1 cycle	B-0.25	2000	1 cycle	0.4	oil burner
11	B-0.2	1500	1 cycle	same as most severe			0.15	water pump
12	B-0.2	1700	1 cycle	B-0.2	1400	1 cycle	0.06	oil burner
13	B-0.1	350	1 cycle	too few to show typical			4 total	house next to 12
14	C	800	15 μs	—	—	—	1 total	lightning
15	B-0.25	800	3 cycles	B-0.25	600	3 cycles	0.05	rural area
16	B-0.15	400	15 μs	B-0.13	200	30 μs	0.4	surges
Street pole	B-0.5	5600	4 cycles	B-0.3	1000	1 cycle	0.1	lightning stroke nearby
Hospital	C	2700	9 μs	C	900	5 μs	0.1	lightning storm
Hospital	B-0.3	1100	1 cycle	too few to show typical			4 total	
Dept. store	B-0.5	300	1 cycle	B-0.5	300	1 cycle	0.5	
Street pole	B-0.2	1400	4 cycles	B-0.2	600	4 cycles	0.07	lightning storm

†A—long oscillation, B—damped oscillation, C—unidirectional. Number shows frequency in megahertz

*Reprinted from *Surge Voltages in Residential and Industrial Power Circuits* by Francois D. Martzloff, Member, IEEE, and Gerald J. Hahn. Reprinted by permission from *IEEE Transactions on Power Apparatus and Systems*, Vol. PAS-89, No. 6, July/August 1970, pp. 1049-1056. Copyright 1970, by the Institute of Electrical and Electronics Engineers, Inc. Printed in U.S.A.

3.3 Commonly Used Test Waveforms

1. The 10 × 1000μS Test Waveform used by many TVS manufacturers, also by incoming inspection departments of users, represents some commonly encountered transients. (See Figure 7).
2. The IEEE Standard (ANSI C 37.90a — 1974) for surge withstand capability. (See Figure 8).

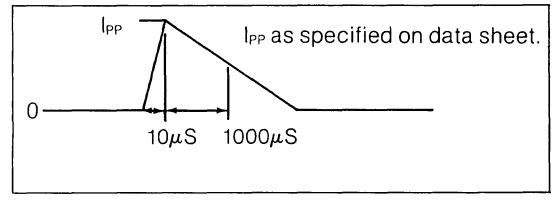

Figure 7 — Commonly Used Test Waveform

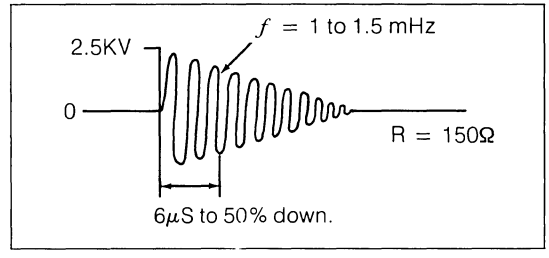

Figure 8 — More Complex Standard Waveform

3.4 Surge Testing

Figure 9 shows a typical test set used to produce an exponentially decaying current pulse of 1mS to 50% down. (10 × 1000μS). The 1mS waveform is used by many manufacturers to test and characterize their TVS devices for pulse power and clamping voltage.

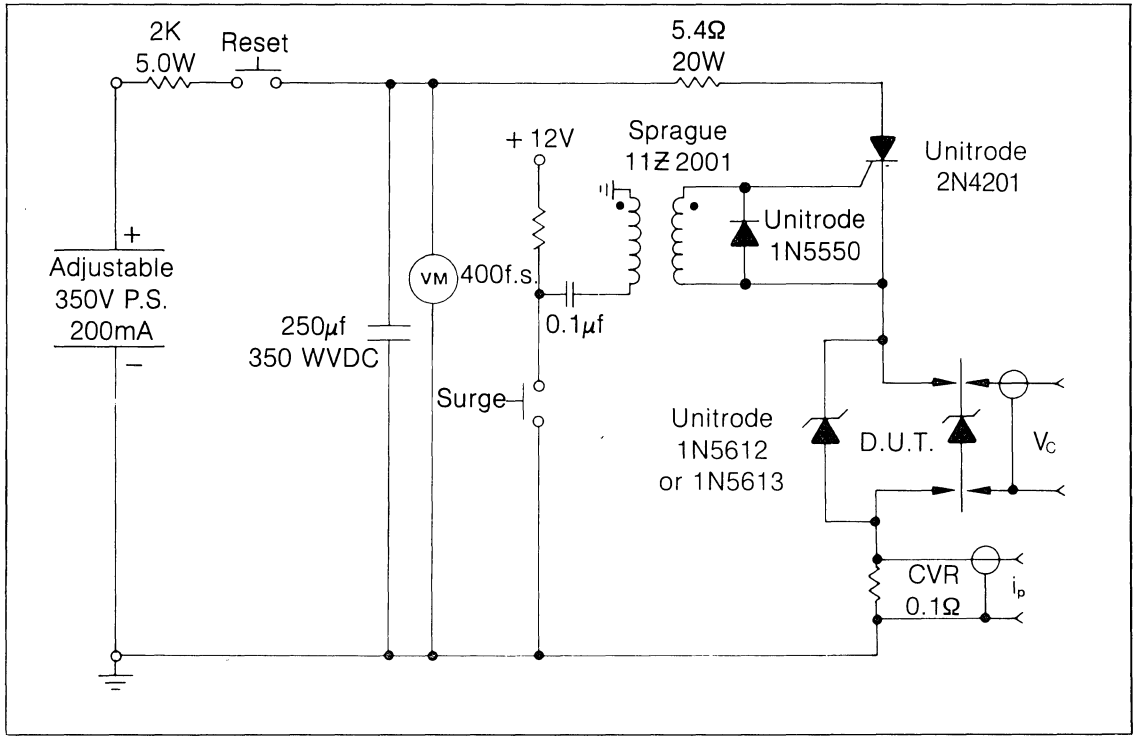

Figure 9 — Suggested Set-up for Surge Testing

4.0 Examples

4.1 Relay and Solenoid Applications

When the energy stored in the coil inductance of a relay or solenoid is released it can damage contacts or drive transistors. It can also produce EMI interference. A TVS used as shown in Figure 10 will provide reliable operation.

Just before the switch opens, the initial inductor current $I_O = \frac{V_{cc}}{R_L}$.

This is the worst case (maximum) current and assumes the switch was closed long enough for the circuit to reach steady-state.

After the contacts switch at t = 0, $e = -L\frac{di}{dt}$, and when using a TVS the change in coil current, $\frac{di}{dt} = \frac{V_c}{L}$. Referring to Figure 10d, $t_1 = \frac{I_O}{di/dt} = \frac{V_{cc}/R_L}{V_c/L} = \frac{V_{cc}L}{R_L V_c}$. Note that the higher the V_c of the TVS, the shorter the current decay time.

In order to select the proper TVS, determine:

1. Peak pulse power $P_p = I_p \times V_c$, where $I_p = I_o$.
2. Pulse time t_p (@ 50% down point of i_{TVS}) = $\frac{t_1}{2}$.
3. These values of P_p and t_p are used with graphs of pulse power vs. pulse duration provided on the TVS305 and TVS505 data sheet to select proper device. See example in Figure 2.

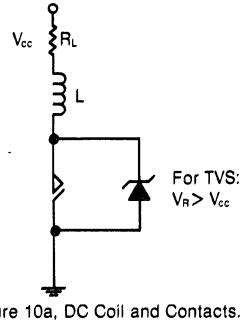

Figure 10a, DC Coil and Contacts.

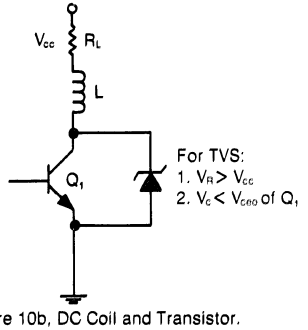

Figure 10b, DC Coil and Transistor.

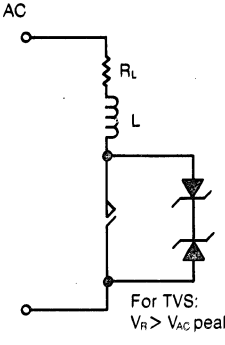

Figure 10c, AC Coil and Contacts.

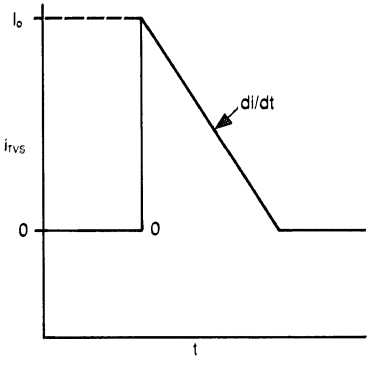

Figure 10d, Simplified Current Waveform in the TVS.

NOTE: In some cases, because of accessibility, the TVS must be located across the coil; in that case a diode should be used in series with the TVS, connected back to back as shown in Figure 11.

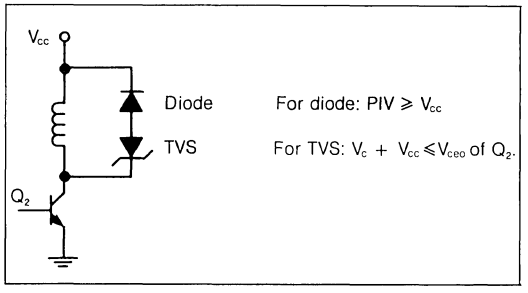

Figure 11 — Using TVS Across Coil

Sample Calculations:

For example, using the circuit of Figure 10a, and sample values of:

V_{cc} = 14V, L = 1mH, and R_L = 2Ω;

For V_{cc} = 14V, the next higher V_R is 15V. (Note that V_c = 22.2V at 10A).

STEP 1: $I_o = \frac{V_{cc}}{R_L} = \frac{14V}{2\Omega} = 7A$

$P_p = I_p \times V_c = 7.0A \times 22.2V = 155W$

STEP 2: $t_1 = \frac{V_{cc}/R_L}{V_c/L} = \frac{14/2}{22.2/10^{-3}} = 0.32mS$

so $t_p = \frac{0.32mS}{2} = 0.16mS = 160\mu S$

STEP 3: From Figure 2, P_{pmax} for $t_p = 160\mu S$ is 1200W, which is well above the circuit value of 155W.

4.2 Protecting Switching Power Supplies

The designer needs to protect against:

1. Load transients
2. Line transients
3. Internally generated transients including those produced by internal faults or failures.

Transients can produce failures because of their own high energy level; and also they can cause improper operation and component failure.

Figure 12 shows a simplified schematic of a typical switching power supply.

Referring to Figure 12, the TVS devices shown protect the following circuit components:

1. the rectifiers.
2. the HV switching transistors.
3. the output rectifiers.
4. the control circuitry.

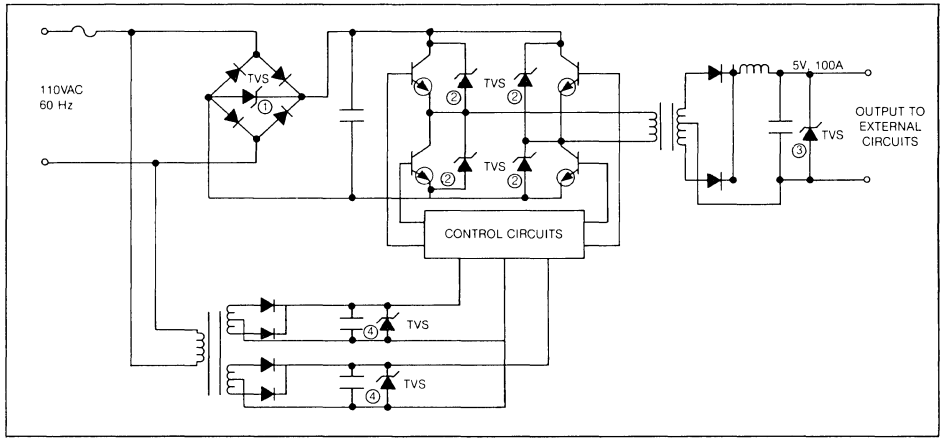

Figure 12 — Typical Switching Power Supply

4.3 Protecting Microprocessor Based Systems

While most microprocessor and IC semiconductor manufacturers design some form of diode-resistive input clamping network on the chip itself, transient voltage protection offered is very minimal — on the order of a few watts of pulse power. Manufacturers are also reluctant to make device performance and reliability claims when power supply operation extends beyond the maximum rated level of the individual device for even relatively short durations such as those that may be encountered during on-off transitions. Therefore, there is a need for some external protective device to suppress voltage transients, as shown in Figure 13.

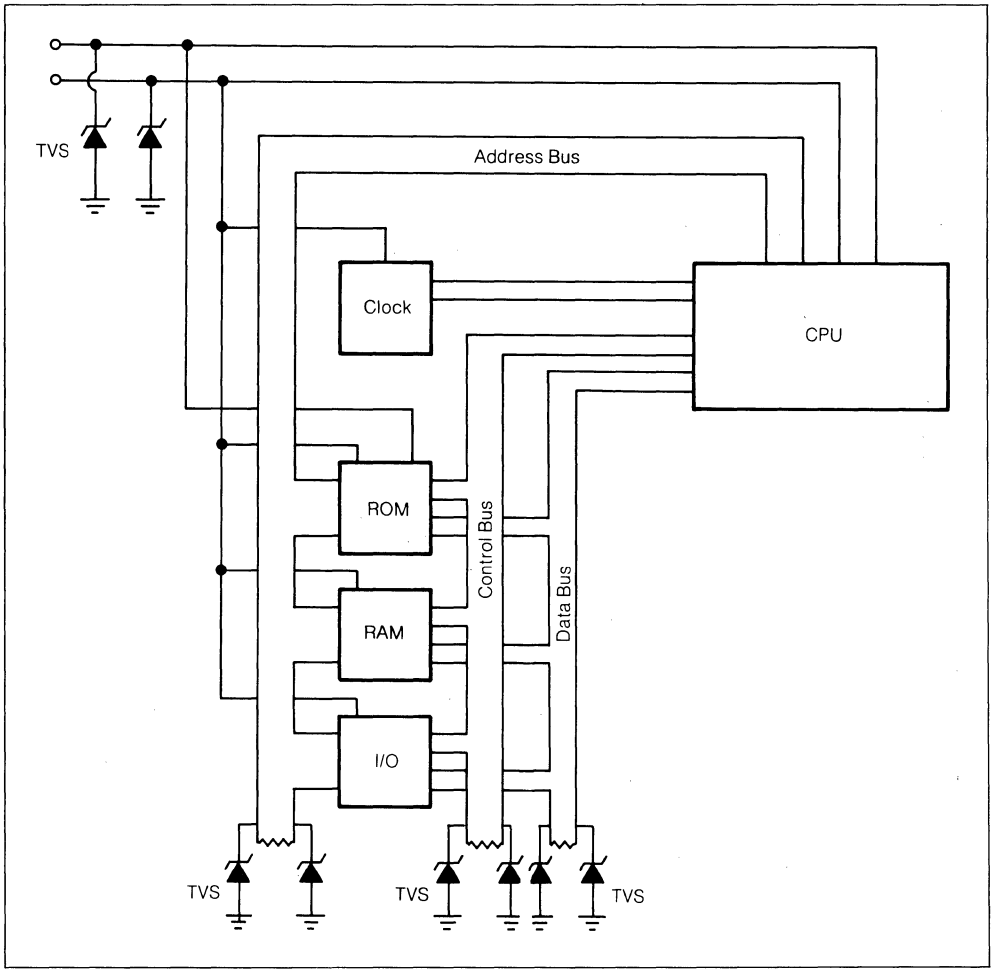

Figure 13 — Protecting Microprocessors

5.0 Alternative Protection Devices

Other protective devices such as MOVs, spark gaps, and crowbars have one common disadvantage when compared to zener TVS products; the response time is from nanoseconds to as much as tens of microseconds as compared to 1 pS for an avalanche zener diode. Even 50nS is long enough to allow a transient to destroy the small junctions used in most integrated circuits, logic, fast transistors, etc.

In circuits where transient pulses are fairly common, device degradation becomes a significant problem. TVS products do not significantly degrade even after 100,000 transients.

In many cases, the zener TVS and one of the alternative devices can complement each other. For example, when used with an SCR crowbar, the zener TVS will keep the voltage during a transient to an acceptable level until the crowbar, which may take 10μS to short the line, can protect the load circuits, and in the case of a heavy transient protect the smaller TVS as well.

DETECTING IMPENDING CORE SATURATION IN SWITCHED-MODE POWER CONVERTERS

ABSTRACT

A new low concept termed "mismatched flux" has been developed which not only prevents impending saturation of the core but also provides symmetrical switching current in power switches in Pulse Width Modulation switched-mode converters except at low flux density. The detecting signal is obtained by mismatching the flux in the outer legs of an E-E core configuration.

INTRODUCTION

Opposite polarity power pulses are applied to the power transformer in a PWM converter to transfer power from the primary to the secondary windings. The volt-second integral of these pulses averaged over one or more cycles should be zero to avoid any problems with transformer core saturation.

In practice, however, imbalance occurs due to non-ideal characteristics of power switches, mainly the switching times (including storage and delay times) and saturation voltage. Even though the imbalance in the pulse width of the drive current provided by a PWM control circuit is very small compared to power switches, it can drive the core into saturation.

Core saturation in PWM switched-mode converters can cause problems such as secondary breakdown in switching transistors, excessive voltage and current stress on the rectifiers, and EMI problems.

The unique circuit described in this paper develops voltages proportional to the flux density in the core. When the maximum flux densities at the end of the positive and negative cycles in the core are not the same, unequal voltages are produced during the positive and negative cycles. These voltages are fed back to the PWM control circuit which adjusts the widths of its output pulses until the amplitudes of these two voltages are equal.

This technique, which can be applied in push-pull converters as well as bridge type converters, prevents core saturation and provides symmetrical primary current during the positive and negative cycles. It allows the most efficient use of the power transformer. In a buck type regulator, the current limiting function can be performed with this same technique.

THE UNBALANCED PWM CONVERTER

Figure 1 shows the typical push-pull converter and its associated current and voltage waveforms. Due to the difference in switching times and $V_{CE(SAT)}$ of transistors Q_1 and Q_2, the transformer core is driven into saturation. The volt-seconds applied by transistor Q_2 is higher than Q_1 as shown in Figure 1d, even though the secondary current is the same during on-times of transistors Q_1 and Q_2.

Three important observations can be made from these figures:

1. Information concerning the magnitude of the imbalance of the flux can be derived by examining the current in the rectifier diodes (Figures 1e and 1f) during the dead-band period.
2. The slopes of the primary currents when Q_1 and Q_2 are conducting are not the same.
3. The familiar equation $I_{C1}/I_{D1}=N_2/N_1$ is not applicable when the flux density in the transformer is not symmetrical during the positive and negative half-cycle.

Under normal operating conditions and during dead-band period, the path for the current flowing in the output inductor L is provided by diodes D_1 and D_2. The inductor current is divided between these two diodes. The magnetizing current I_{MS} flows in the entire secondary winding. Note that the magnitude of I_{MS} remains the same during the entire dead-band period because the voltage across the secondary winding is zero. The overall result is that one diode conducts more current than the other diode. The current flowing in these diodes is:

$$i_{D_1} = \frac{i_L}{2} + I_{MS} \quad \text{Current in Rectifier Diode } D_1 \qquad (1)$$

$$i_{D_2} = \frac{i_L}{2} - I_{MS} \quad \text{Current in Rectifier Diode } D_2 \qquad (2)$$

Subtracting i_{D_1} from i_{D_2} and rearranging

$$I_{MS} = \frac{i_{D_1} - i_{D_2}}{2} \qquad (3)$$

Thus, the current flowing in diode D_1 and D_2 allows us to determine the exact amount of imbalance in the flux density during the positive and negative half-cycles. Figure 1g, which is calculated from diode current D_1 and D_2, shows the operating flux density of a core in only the 1st quadrant of a B-H curve.

When transistor Q_1 or Q_2 turns on, this magnetizing current is reflected back into the primary winding according to the equation:

$$I_{PM} = \frac{2(N_2)}{N_1} I_{MS} \qquad (4)$$

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The dotted line in Figures 1c and 1d shows the reflected current in the primary winding. Since the flux density is not symmetrical around zero in the B-H curve, the collector current in Transistor Q_1 is lower than in Transistor Q_2. When the magnetizing current (dotted line in Figure 1c) is added to the actual measured collector current (solid line) in Transistor Q_1, it will produce a linear slope compared to the rounded slope of the measured collector current. The equation

$$\frac{I'_{c_1}}{I_{D_1}} = \frac{N_2}{N_1} \qquad (5)$$

will hold true, where I'_{c_1} is equal to the magnetizing current reflected into the primary winding plus the actual measured collector current I_{c_1}.

Similarly, when Transistor Q_2 turns on, the transformer transfers energy from the input power source to the secondary. Some energy is also stored in the core due to the unsymmetrical flux density in the core. The magnetizing current (current level above dotted line in Figure 1d) is subtracted from the measured collector current.

The equation

$$\frac{I'_{c_2}}{I_{D_2}} = \frac{N_2}{N_1} \qquad (6)$$

will hold true, where I_{c_2} is equal to the actual measured collector current minus the magnetizing current reflected into the primary winding.

The imbalance in volt-seconds causes the flux density to drift towards one side of the hysteresis loop. This causes an imbalance in the collector currents of the transistor switches. The imbalance in volt-seconds will be compensated, to some extent, by an adjustment in the collector currents of the two transistor switches. As the collector current decreases the storage time increases and $V_{CE(SAT)}$ decreases as shown in Figures 2 and 3. This effectively increases the volt-seconds. The I_R drop in the primary winding also helps to balance the volt-seconds in the transformer. These collector currents will vary until the proper volt-second balance is obtained in the transformer. If no corrective scheme is provided to balance current in the switch, the following disadvantages are present:

1. The required current ratings of the transistors and rectifiers must be increased.
2. The $V_{CE(SAT)}$ losses will be increased. Furthermore switching losses will be even higher, especially in high voltage power converters.

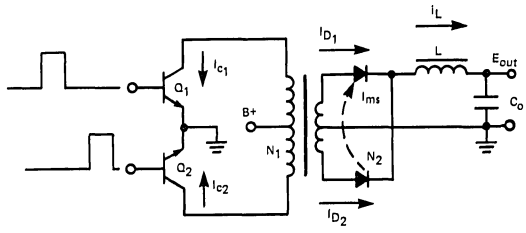

Figure 1a.

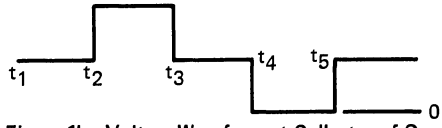

Figure 1b. Voltage Waveform at Collector of Q_2.

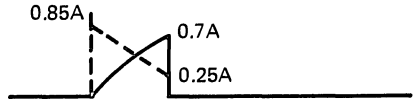

Figure 1c. I_{c_1} Current Flowing in Transistor Q_1.

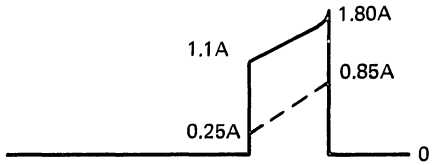

Figure 1d. I_{c_2} Current Flowing in Transistor Q_2.

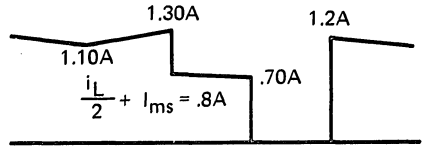

Figure 1e. Load Current in I_{D_1}.

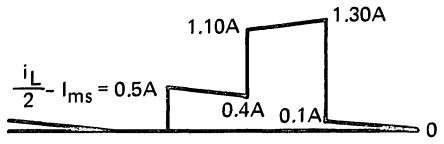

Figure 1f. Load Current in I_{D_2}.

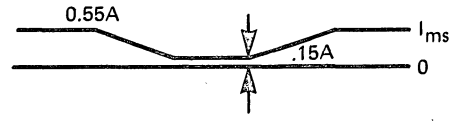

Figure 1g. Magnetizing Current in Secondary.

Figure 1. Gallery of Waveforms of a Push Pull P.W.M. Switching Regulator

3. Losses in the core increase as a function of the square of the maximum operating flux density. As the core temperature goes up, the losses in the core also increase, thus, the potential exists for thermal runaway in the core.
4. The leakage inductance is proportional to the maximum operating flux density. The imbalance causes high leakage inductance, and excess voltage stress across the transistor and rectifier.
5. If the core goes into saturation, it creates excessive current in the power switches, can result in forward bias second breakdown, clamped reverse bias second breakdown, and increased radiated and conducted EMI.

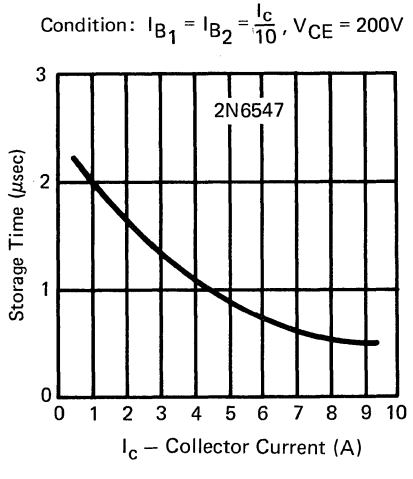

Figure 2. Storage Time vs Collector Current

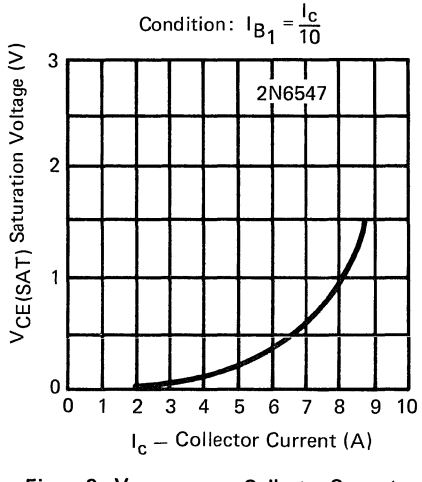

Figure 3. $V_{CE\ (SAT)}$ vs Collector Current

BASIC PRINCIPLE

An air gap in the E-E core can be used to prevent core saturation in PWM converters. The air gap reduces residual flux density in a square loop transformer and prevents core saturation during the start-up condition. However when there is a volt-second imbalance, the air gap does not prevent core saturation.

If the air gap is placed in only one of the outer legs of an E-E or EC core configuration, as shown in Figure 4a, then it allows a means of detecting core saturation, and by using this signal, to provide symmetrical flux swing in the core.

The primary winding and secondary winding are placed in the center leg of the E-E core, while the auxiliary winding is placed in the outer leg which contains the air gap.

The peak output voltage of the auxiliary winding is detected with Diode D_1, D_2 and Capacitor C_1. The Resistor R_1 in parallel with Capacitor C_1 provides the reset for another cycle by discharging the capacitor. The voltage developed across R_1 and C_1 is proportional to the maximum rate of change in flux at the instant when the transistor switch turns on.

The total amount of flux passing through the outer leg with the air gap is inversely proportional to the magnetic length of the opposite side of the leg. As the flux density in the center leg increases, a larger and larger area of the core at the point where the two E cores meet on the opposite side of the leg will become saturated. Note that only the edge of the core will saturate, while the rest of the core (leg with no air gap) will not saturate. As it saturates further, the reluctance of this leg increases, thus its effective magnetic length increases. This phenomenon forces more flux into the leg which has the air gap.

The voltage developed in the auxiliary winding is expressed by Faraday's Law:

$$V = N\left[\frac{d\Phi_2}{dt}\right] \times 10^{-8} \qquad (7)$$

Where N is the number of turns. Thus the magnitude of developed voltage will depend upon the rate of change in flux with respect to time. Since the air gap is in only one leg of the E-E core, the term $|d\Phi_2/dt|$ changes continuously and depends upon the flux density in the center leg. Thus the output voltage from the auxiliary winding also varies with respect to time.

The same results can be obtained with using a core as shown in Figure 4b. The advantage of using this core is that the leakage inductance will be less compared with the previous technique.

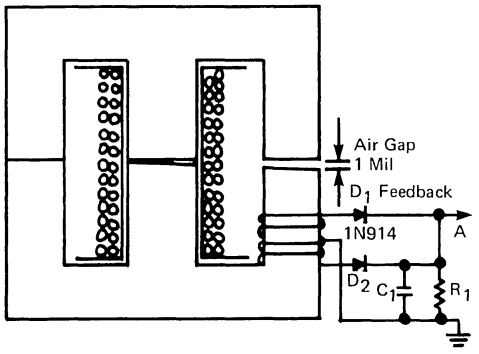

Figure 4a. Air Gap in Only One Leg of E-E Core

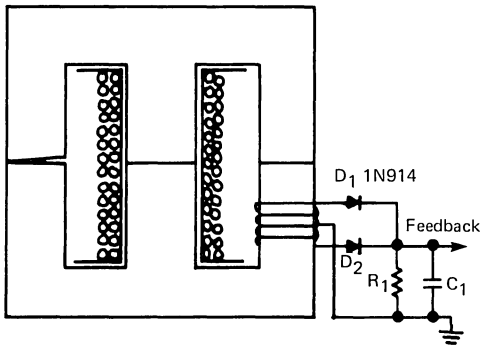

Figure 4b. Tapered Air Gap in One of the Outer Legs of the E-E Core

Figure 5 shows the B-H curve (solid line) of an E-E core with an air gap in only one leg. It lies between the E-E core with an equal air gap in both sides of the outer legs and a core with no air gap. From this figure it is obvious that $|d\Phi/dt|$ changes with the flux density and is a non linear function. Figure 6 shows variation in inductance with magneto-motive forces.

Figures 7 through 9 show the voltage developed in the auxiliary winding at different values of the magnetizing current. The magnetizing current is directly proportional to the maximum flux level for a given transformer. In these waveforms the initial flux density is set at zero and the allowed flux swing is in the 1st quadrant only. The magnitude of the error signal (when the transistor switch turns on) is the same in all three figures since $d\Phi_2/dt$ is the same. As the magnetizing current increases, the developed error signal due to $d\Phi_2/dt$ in the winding around the outer leg (with the air gap) also increases because $d\Phi_2/dt$ increases with flux density. From the shape of the collector current it is obvious that the core is not saturated.

Figure 10 shows the voltage developed across Resistor R_1 from the auxiliary winding and also the current in the two transistors I_{c1} and I_{c2}. The current waveforms show that there is no symmetry in the flux of the core. Figure 11 shows the same output voltage peak detected by paralleling Capacitor C_1 across Resistor R_1. The voltages developed are not symmetrical during the alternative half period of the cycle. Figure 12 shows that when the developed voltage is fed back to the control circuit, it produces flux symmetry in the core. This can be seen by the equal magnitude of the collector currents.

The initial amplitude of the voltage from the auxiliary winding (after the transistor turns on) can be used to further improve performance. This can be accomplished by gating the output voltage of the auxiliary winding with a pulse width of a few microseconds.

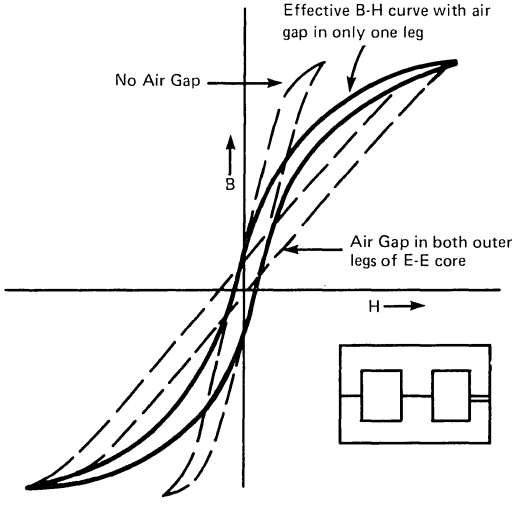

Figure 5. Effects on Hysteresis Curve with Air Gap in Only One Leg of E-E Core

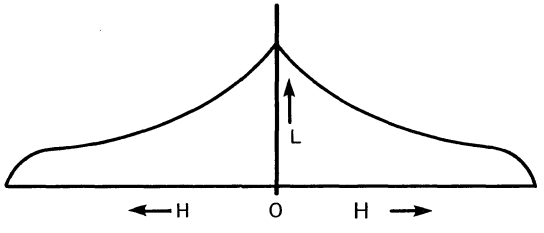

Figure 6. Inductance vs Magnetomotive Force

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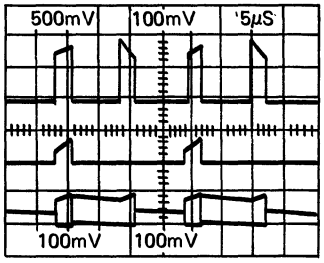
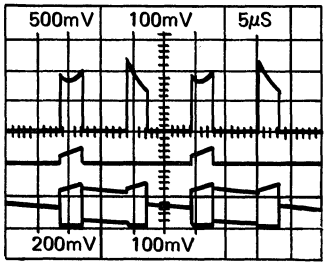


Error Signal V Scale = .5V/div

I_{C1} Collector Current 1A/cm

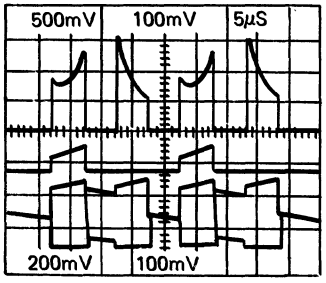
Diode Current I_{D1}, I_{D2} 1A/cm



Error Signal V Scale = .5V/div

I_{C1} Collector Current 2A/cm

Diode Current I_{D1}, I_{D2} 1A/cm

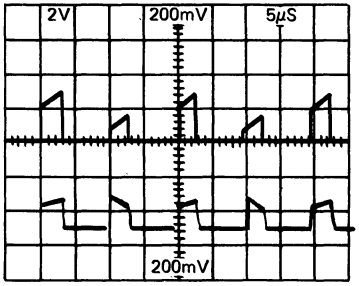


Error Signal V Scale = .5V/div

I_{C1} Collector Current 2A/cm

Diode Current I_{D1}, I_{D2} 1A/cm

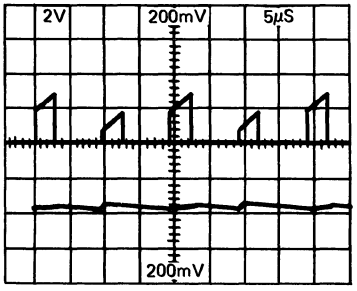
Figure 9. Error Signal Developed at Magnetizing Current = 700 mA



Primary current I_{C1}, I_{C2} 2A/cm.

Voltage developed at Point A in Fig. 4, due to unequal volt-sec, C_1 is removed 2V/cm.

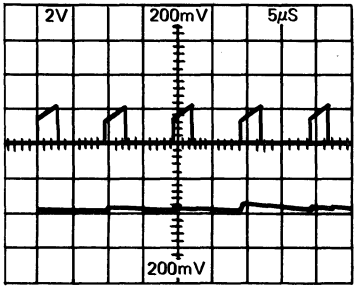
Figure 10. Without a Feedback



Primary current I_{C1}, I_{C2} 2A/cm.

Voltage developed at Point A in Fig. 4 due to unequal volt sec 2V/cm.

Figure 11. Without a Feedback



Primary current I_{C1}, I_{C2} 2A/cm.

Error Signal at Point A in a closed loop.

Figure 12. With a Closed Loop

CLOSING THE LOOP

The developed voltage across R_1 and C_1 is fed back to the control circuit (UC3524).
This voltage can be fed into the control circuit in one of three ways:

1. AC coupled into the output of the error amplifier. Since this amplifier is a transconductance design, the output has very high impedance (approximately 5 MΩ). The feedback signal from the auxiliary winding is modulated at this point with the output voltage of the error amplifier. The output pulse width is corrected to provide symmetry as well as to prevent core saturation.
2. Into the non-inverting input. This can be achieved by (a) lifting up 4.7K from ground in the NI circuit, (b) adding 100Ω in series with 4.7K and the other side of 100Ω returning to ground, and (c) adding a feedback signal at the junction of the 100Ω and 4.7K resistors. The peak to peak amplitude of the signal fed into the NI input has to be less than the output ripple voltage fed into the INV input. Feeding signals in the NI or INV inputs will provide flux symmetry in only DC conditions.
3. Feeding the signal at the INV input. This requires an opposite polarity signal, which can be obtained by reversing the diodes in

Figure 4. The modifications required to change the circuit are the same as listed above. Also in this case the peak to peak amplitude of the signal fed into the INV input has to be lower than the peak to peak output ripple voltage fed into the INV input.

To obtain adequate signal at very low input voltages may require a low V_F diode.

PWM PUSH-PULL CONVERTER

A complete schematic of the PWM Push-Pull Converter using this technique is shown in Figure 13. The power switch is a Unitrode hybrid circuit, the PIC636, which is housed in a 4 pin electrically isolated TO-66 package. It provides the advantages of low RFI and ease in heat sinking due to the electrically isolated package. Constant base drive is provided by small signal transistors (2N2905). The output rectifier is a center tap TO-220 fast recovery (35nS) rectifier. The control chip is a UC3524 PWM voltage regulator. The soft start function is performed at the NI input by allowing the reference voltage to come up slowly when the input power supply is turned on. The feedback signal from the auxiliary winding is fed into the compensation terminal (output of the error amplifier) with Resistors R_2, R_3 and Capacitor C_2. The steady state and transient response of the circuit was evaluated: it provides flux symmetry and prevents core saturation under these conditions.

HALF BRIDGE CONVERTER

The method described in this paper can be used for half bridge configurations as shown in Figure 14. It does not require a low ESR, high voltage capacitor in series with the primary of the transformer. The DC balance is provided by Capacitors C_1 and C_2. Thus, this technique offers a low cost solution in preventing core saturation and in providing flux symmetry.

BUCK REGULATOR

In a buck regulator, the method described here can be used to provide the current limiting function without a current sense resistor.

The circuit shown in Figure 15 is a high performance buck regulator. It utilizes the Unitrode power hybrid switching regulator circuit, PIC625. The high performance transistor chip and fast recovery (20nS) rectifier diode are mounted in an electrically isolated 4 pin TO-66 package. The control circuit is a Unitrode Corp. PWM voltage regulator chip. The inductor L utilizes the equal E-E core configuration with unequal air gaps in the side legs. The main winding is placed on the center leg while the two auxiliary windings are wound on the outer legs. The output voltage from these auxiliary windings are compared using Transistor Q_3. The magnitude of the current limiting is adjusted with Resistor R_1. When the current in the hybrid circuit, PIC625, exceeds the set current

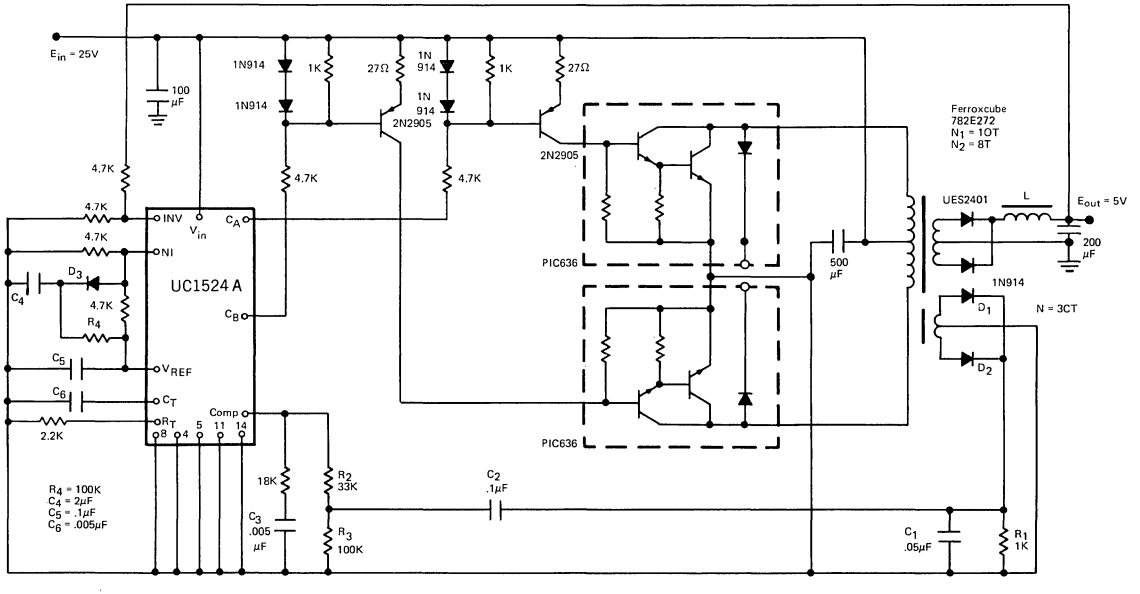
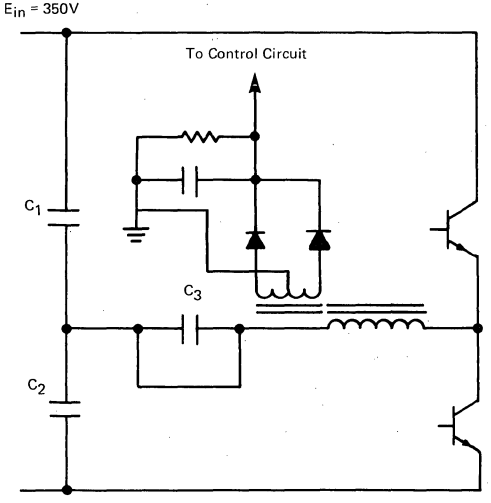


Figure 13. PWM Push-Pull Converter

limit, Q_3 turns on and the voltage developed across C_1 and R_2 is fed into transistor switches Q_1 and Q_2. The transistor Q_2 removes the drive current from the PIC625 instantaneously. It provides protection during the transient condition. The transistor switch Q_1 provides the function of current foldback by discharging the soft start capacitor C_2. The transient response of this circuit is shown in Figure 16. The current in the switching transistor during short circuit and normal operation mode is shown in Figure 17.



The flux correction circuit eliminates the need for capacitor C_3 in series with primary of the transformer

Figure 14. Half Bridge Converter

CONCLUSION

The low cost circuit described in this paper prevents core saturation due to unsymmetrical flux, and provides equal collector current in the transistor switch and in the rectifier diodes. The power dissipation of these switches is kept in balance.

Further advantages of this approach are:

1. a. In a push-pull converter, the need for an inductor is eliminated, thus, the size,cost and weight are reduced.
   b. Transient response time is improved.
2. In a bridge type converter, a capacitor (low ESR, high voltage) in series with the primary of the power transformer is not required. (In conventional designs even with this capacitor, there exists a danger that the core can be driven into saturation under transient conditions).
3. In a buck type converter, it allows the current limiting function to be performed without a current sense resistor, thus improving the performance.
4. Storage time and $V_{CE(SAT)}$ matching of the transistor switches are not required.
5. More efficient use of the transformer, allowing smaller, lower cost magnetics is achieved.
6. In an off-line converter, isolation is maintained.

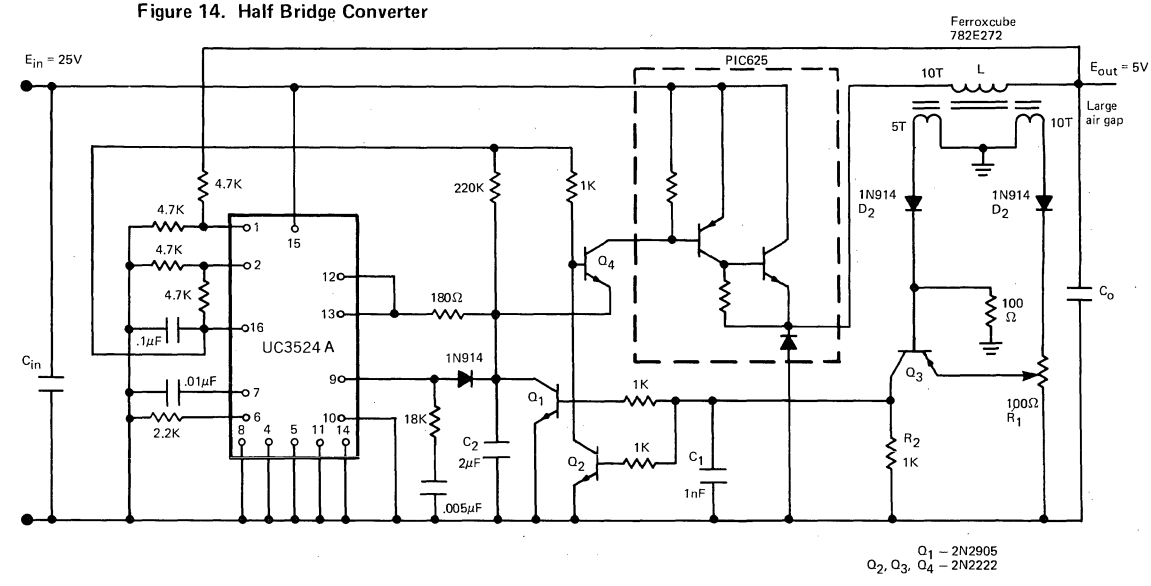
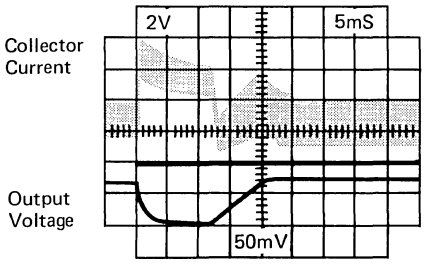
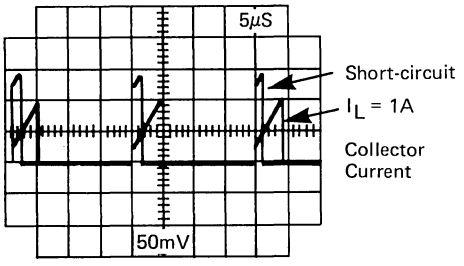


Figure 15. High Performance Buck-Type Switching Regulator



V = 2V/div, H = 5mS/div

Figure 16.
Collector currents for step change in load from 1A to 5A, to 1A.



V = 1A/div, H = 50μS/div

Figure 17.
Collector currents, I_L = 1A and under short circuit conditions.

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1. Walter J. Hirschberg, "A New PWM Control Technique That Eliminates Transformer Unbalance Problems in Power Converters", ACDC Electronics Powercon 6, 1979.
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HYBRID CIRCUITS FOR LOW VOLTAGE SWITCHED-MODE CONVERTERS

ABSTRACT

Hybrid circuits offer many advantages over the conventional discrete approach in switched-mode converters. This paper deals with the construction of the hybrid circuit and its thermal considerations. It examines the efficiency of a buck regulator employing a saturated transistor versus the optimized darlington configuration. Also considered are the effects of reverse recovery of the rectifier and base spreading resistance of the transistor on the efficiency of a switching regulator. Finally, applications of standard hybrid circuits for switched-mode converters are discussed.

I. INTRODUCTION

Recently a rapid increase in the use of hybrid circuits in switched-mode power converters is evident due to their inherent advantages. Some of these advantages are: dc and high frequency electrical isolation, ease in heat sinking multiple power components within the single hybrid package, reduced stray parasitics, and finally, lower overall cost compared to the discrete approach.

The hybrid circuit approach requires careful consideration of thermal design for maximum reliability and proper selection of silicon chips for best electrical performance. This paper provides an overview of the construction of a typical power hybrid switching regulator circuit and its thermal design considerations. Also considered are the effects of the reverse recovery time of the rectifier and the base spreading resistance $r_{BB'}$, of the power switching transistor on the efficiency of the switching regulator. Applications and advantages are also discussed for types of hybrid circuits which are designed for low voltage applications and other types designed for "off-line" switched mode converters.

II. CONSTRUCTION

The power hybrid circuit PIC600 is the power output stage of a buck type switching regulator as shown in Figure 1. It consists of a high speed darlington-connected transistor pair, a commutating diode and two thick film biasing resistors. These components are housed in a 4 pin electrically isolated TO-66 package.

The manufacturing procedure for these devices is divided into two stages. First, a BeO substrate is chosen because of its excellent thermal conductivity, — 70% as good as copper. The interconnection paths, pad areas for the wire bonds and the thick film resistors are screen printed onto the BeO substrate and then fired in high temperature furnaces. For optimum performance, the tolerances of the thick film resistors are maintained within 10% of their design values. The semiconductor devices used in the circuit are all silicon planar passivated devices and are gold eutectic mounted. Aluminum ultrasonic wire bonding is used for interconnections.

In the second stage the BeO substrate is soft soldered to the header for good heat transfer. A copper slug is interfaced between the BeO substrate and nickel plated steel header. The copper slug is used to relieve mechanical stress between the BeO substrate and the header and to provide heat spreading resulting in lower thermal resistance.

III. THERMAL CONSIDERATIONS

The design of the power hybrid circuit requires careful consideration to optimize important thermal requirements; thermal cycling, resistance, and partitioning. To obtain maximum thermal resistance, overlapping heat flow should be avoided. As shown in Figure 2, heat flow from silicon chips #2 and #3 overlaps, thus reducing the thermal capability. No overlapping heat flow occurs from chip #1.

Thermal resistance of the package can be calculated by the formula:

$$R_T = \rho \frac{t}{A}$$

where t is the thickness of material through which heat flows, ρ is the thermal resistivity of the material and A is the average area through which heat flows.

In making a conservative calculation, it is assumed that heat flux diverges at approximately a 45° angle for all the materials except the copper slug (62.5°) due to high conductivity.

The thermal resistance calculation of a hybrid circuit is shown in Figure 2. The copper slug between the BeO and header reduces the thermal resistance of the package (by about .32°C/W) by spreading the heat flow through a large area of the steel header.

This calculation assumes that no voids are present at the interfaces.

IV. COMPONENT AND CIRCUIT SELECTION

Achieving maximum efficiency in a buck-type regulator requires proper selection of electrical characteristics of the transistor switch and catch diode. Optimum efficiency can be obtained with a

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Schottky rectifier because it has lower forward drop than most PN junction devices. The Schottky rectifier is a majority carrier device and has zero reverse recovery time. However, the Schottky's high junction capacitance (10 times greater than PN junction devices) produces the same effect as the t_{rr} of PN junction devices. Junction capacitance does not change appreciably with temperature, so the effective reverse recovery time remains the same with respect to temperature. Since commercially available Schottky rectifiers have only a 45V PIV rating, the absolute maximum input voltage of the buck type regulator is limited to only 45V.

Ultra fast PN junction devices are available with the same effective reverse recovery as Schottky rectifiers with a higher (up to 400V) PIV capability. The somewhat higher forward drop of the PN junction devices does not degrade efficiency at higher voltages.

The way in which a device recovers from forward conduction is also important. In high voltage (>1000V) power supplies, it is desirable to have abrupt reverse recovery time for optimum efficiency. In low voltage, high current power supplies a soft reverse recovery rectifier is better suited from the RFI viewpoint.

Figure 3 shows the effect of a diode recovery time on transistor power dissipation. The reverse recovery time of the catch diode requires the transistor to conduct higher peak current for a longer duration in the active region. This significantly increases RFI and also increases the power dissipation in the transistor, and may cause second breakdown.

For reliable circuit operation, t_{rr} should be much less than the current rise time of the transistor. This ensures minimum current overshoot in the transistor and also minimizes the amount of time the transistor spends in the active region during turn-on, resulting in lower power dissipation and increased efficiency. However, to obtain maximum efficiency, all switching times, (including current rise time) should be as fast as possible. The rectifier should be selected such that its t_{rr} is one third or less of the current rise time of the transistor. In switching regulator applications, it is also essential that the storage and fall times be as low as possible.

When turn-off is achieved without the assistance of I_{B2}, it is important that the power output transistor have the following characteristics for best performance:

1. Larger emitter periphery area with a triple diffused or double diffused epitaxial construction to provide lowest effective collector series resistance to prevent forward biasing of the collector-base junction.
2. The base spreading resistance, r_{BB}', of the device should be lower than the external biasing resistor. This will provide low storage time and fast fall time.

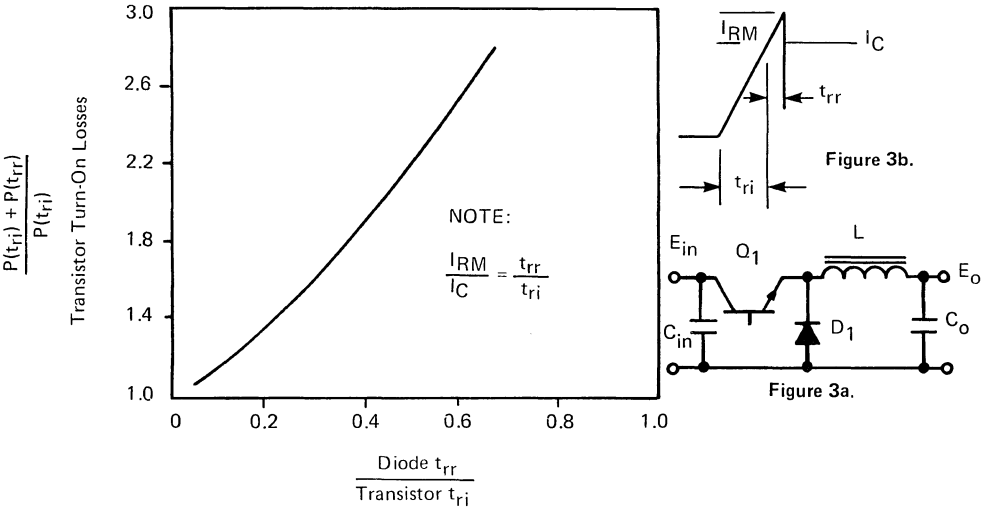


Figure 3. Importance of Reverse Recovery Time of a Rectifier

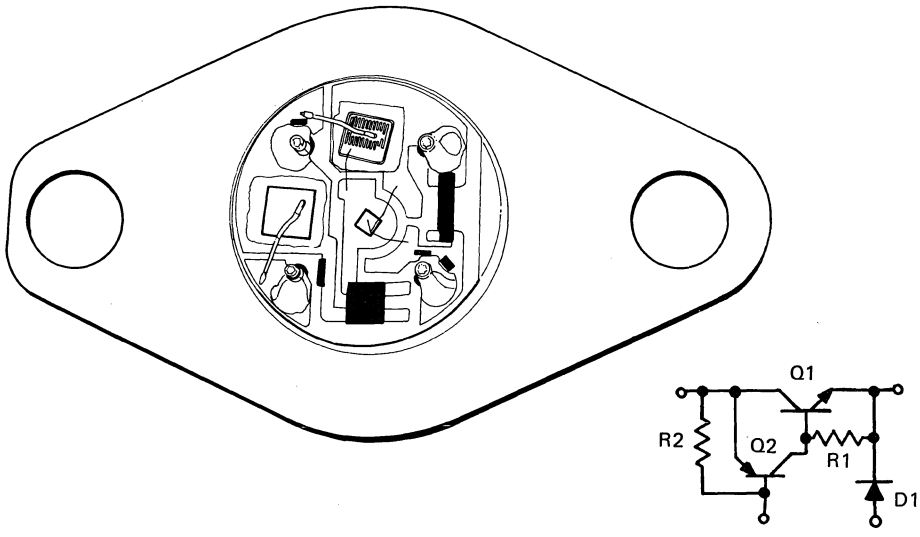
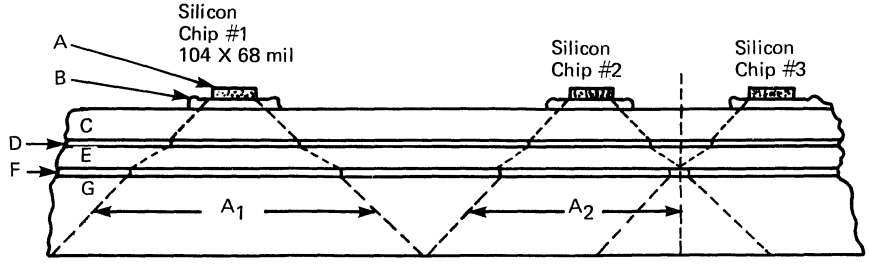


Figure 1. Unitrode power hybrid circuit (PIC600)



DEFINITION:

Material	Temp. Coef. 10^{-6} °C	ρ Rest. °C-in/W	t Thickness in mils		R_T* of PIC625
A – Silicon	4.2	.303	5		.214
B – Si Au Eut.	14	.182	3		.0718
C – BeO	6	.152	20		.249
D – Solder	23	.8	4		.187
E – Copper	16	.104	10		.04614
F – Solder	23	.8	3		.0836
G – Steel	11	.884	65		1.043
				Total	1.8954

*$R_T = \rho \left(\frac{t}{A}\right)$

Figure 2. Heat Flux Line in a Hybrid Circuit

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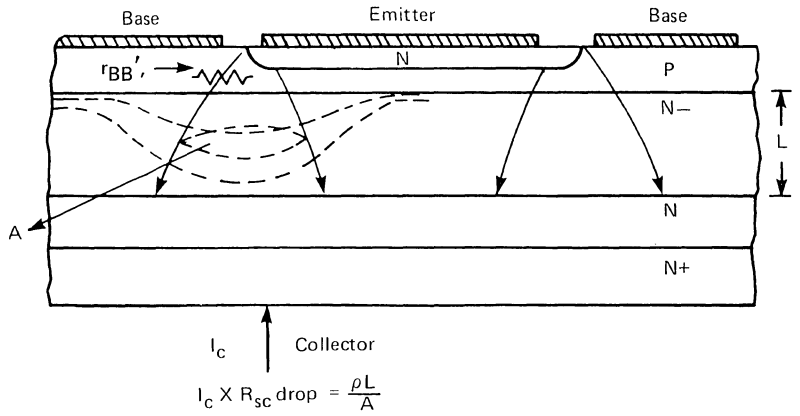


Figure 4. Effect of $r_{BB'}$ on Switching Times and Dynamic Saturation

The resistor turn-on biasing method works satisfactory up to 10A for a low voltage device without affecting the efficiency of the switching regulator. Another advantage of the resistive turn-off circuit is that it limits current crowding during turn-off thus increasing the reliability of the circuit. Since the driver transistor operates in a saturated mode, the device should have a high gain-bandwidth product to minimize overall storage time.

The hybrid circuit PIC600 consists of two transistors connected in a darlington configuration. The internal biasing resistors of these transistors are sufficient for fast turn-off without requiring any I_{B2}.

The table shown in Figure 5 compares the efficiency of a saturated transistor (2N4150) versus the hybrid darlington as the switching element in a 50 kHz buck regulator. In each case, the output device has the same size silicon chip.

Pass Transistor	Power Losses (Watts) $T_j = 25°C$	Efficiency	
		$\frac{E_o}{E_{in}} = 0.5$	$\frac{E_o}{E_{in}} = 0.2$
2N4150 (Saturated)	D.C. Losses . . . . . 0.7 Switching Losses . . . . . 2.27 Drive Losses . . . . . 0.13 Diode Losses 4.76	84.79%	81.66%
PIC625 (Darlington)	D.C. Losses . . . . . 1.4 Switching Losses . . . . . 1.53 Drive Losses . . . . . 0.15 Diode Losses 4.76	82.8%	81.69%

Conditions:
f = 50KHz
E_o = 5V
I_o = 7A
Same size output device for both cases.

Figure 5. Comparison Between Saturated and Darlington Pass Transistors in a Buck Type Switching Regulator

In the saturated transistor approach, the transistor is driven with a forced Beta of 5 during turn-on and turn-off. However, in the darlington configuration, no turn-off base drive is employed. Typical measured switching times and saturation voltages are used to calculate losses.

From the table in Figure 5, it is evident that the hybrid darlington approach provides best results in terms of efficiency when the ratio between the output and input voltage is less than 0.25. In a darlington configuration, if the output device is kept out of saturation, then the rise, fall and storage times will be reduced compared with the saturated transistor. Even at higher output/input voltage ratios the loss in efficiency because of higher $V_{CE(SAT)}$ is minimal compared to the complexity and cost of a drive circuit required for a saturated transistor.

The plot in Figure 6 shows dc power dissipation of a PIC625 at various duty cycles and temperatures. The efficiency of the regulator depends heavily upon output voltage. Switching losses of the PIC625 under conditions shown in Figure 6 are:

25°C – 0.875W
-55°C – 0.525W
125°C – 1.476W

V. APPLICATIONS

Different applications of power hybrid circuits are discussed in this section.

Low Voltage Hybrid Circuits (<100V)

Some applications of low voltage hybrid circuits are: low and high current positive and negative buck-type regulators, bidirectional motor driver circuits, PWM push-pull and half bridge converters. Each is discussed briefly as follows:

a. Buck Type Switching Regulator

The schematic of the low cost, free running buck switching regulator is shown in Figure 7. When the output voltage is lower than the reference voltage, transistor Q_2 is off and transistor Q_1 is on and provides the base drive to the power hybrid circuit PIC600. The current in inductor L_1 increases linearly and continues to charge the output capacitor C_o. When the output voltage exceeds the zener voltage of diode D_1 (plus some fixed fraction of V_{BE} of transistor Q_2) transistor Q_2 turns on and removes base drive current from transistor Q_1 and hybrid circuit PIC600. Resistor R_6 and capacitor C_1 are used to provide fast switching times. The output voltage is trimmed with resistor R_3.

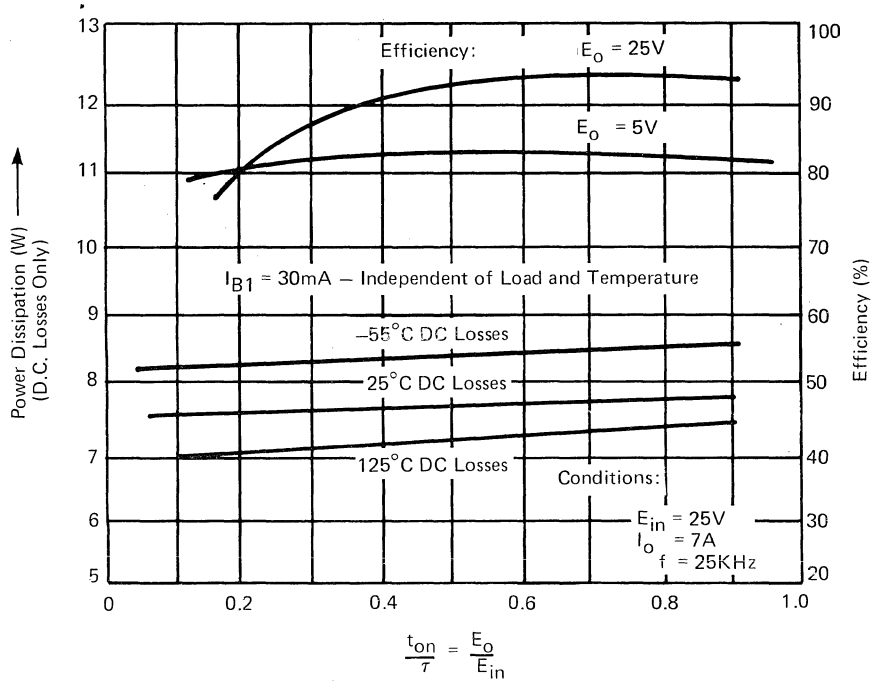


Figure 6. Losses and Efficiency – PIC625

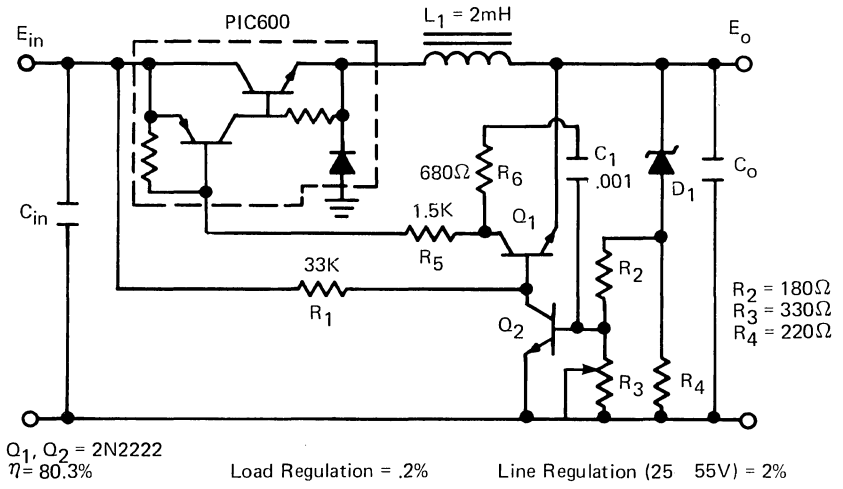


Figure 7. Low Cost Buck Regulator

b. High Frequency Switching Regulator

Low voltage hybrid circuits can be operated as high as 250 kHz due to their fast switching times. When these devices are used above 100 kHz, the storage time of the driver transistor must be reduced. This can be done by using a Baker clamp with resistor R_1 and diode D_1 as shown in Figure 8.

The advantages of operating a buck regulator at higher frequencies are:

- Lower filter cost
- Reduced size and weight
- Improved transient response
- Output ripple voltage less dependent upon ESR of capacitor
- Simpler EMI and RFI filtering

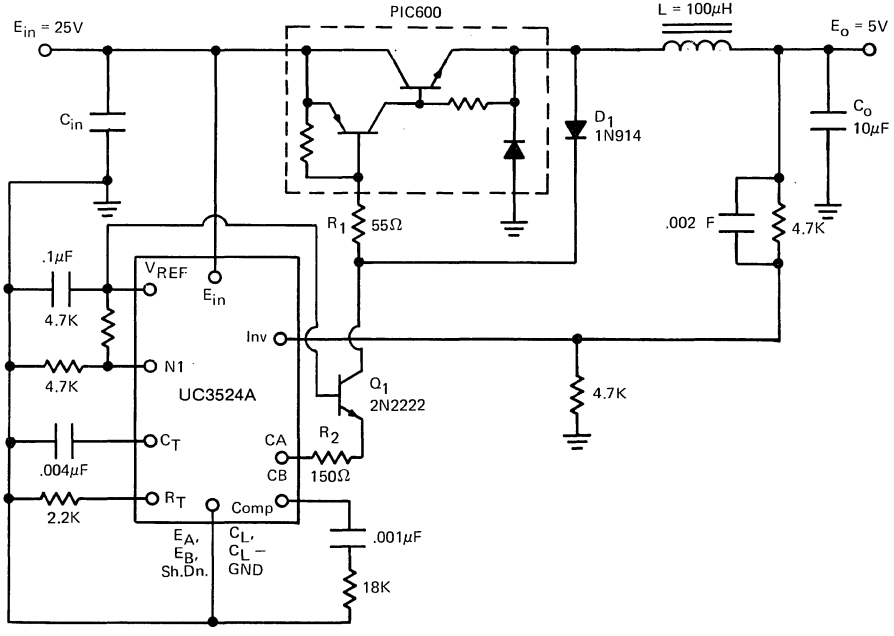


Figure 8. Operating a PWM Buck Regulator Above 100KHz

c) Extending Output Current Capability up to 20A

The output current capability of a buck regulator can be extended by (1) paralleling the output devices as shown in Figure 9 and (2) the use of a high current device as shown in Figure 10.

The advantages of paralleling output devices are that it allows the device to operate with a relatively simple drive circuit and provides simplicity of heat sinking. On the other hand, proper current sharing during the on-time period and turn-off time is required. The circuit shown in Figure 9 provides the circuit technique to do just that. The only drawback is that it requires a dead-band period which must be greater than 0.1L, where L is the inductance value of the common mode choke L_1.

PWM Push-Pull Converter

The circuit schematic shown in Figure 11 is a width modulated push-pull converter. It utilizes the Unitrode PIC636 power hybrid circuit.

Flux symmetry[5] in the transformer core is provided by introducing an air gap in only one leg of the EE core configuration. The voltage developed across resistor R_1 and capacitor C_1 is proportional to the flux density in the center leg of the EE core. This developed voltage is fed back into the control circuit at the output of the error amplifier. The output pulsewidth is corrected by the developed voltage across C_1 and R_1, providing flux symmetry in the power transformer.

Bidirectional Motor Drive Circuit

These power hybrid circuits can be employed to drive inductive loads, such as DC motors, stepper motors, and hammer drivers. Small inductors L_1 and L_2 limit cross-conduction current during switching times of the two hybrid circuits. The excellent switching properties of the hybrid circuit allow the circuit to be operated with high efficiency up to 100 kHz, improving transient response of the circuit.

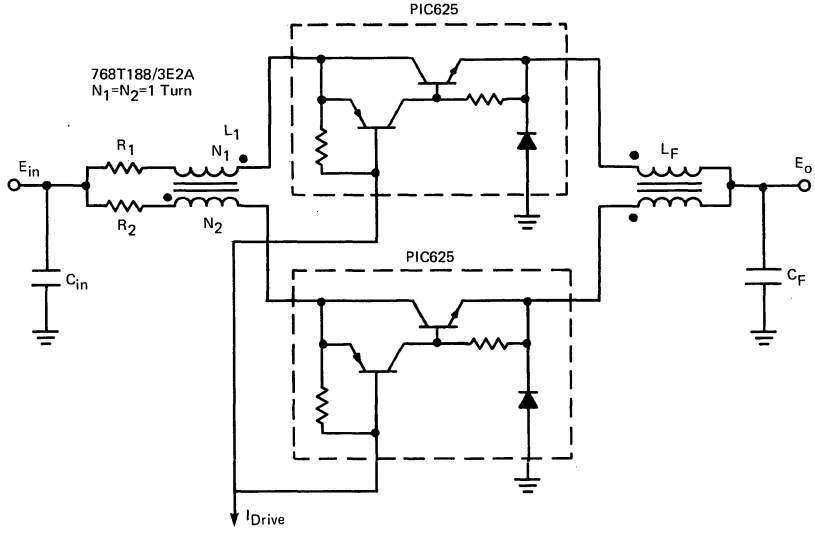


Figure 9. Current Sharing with a Common Mode Choke

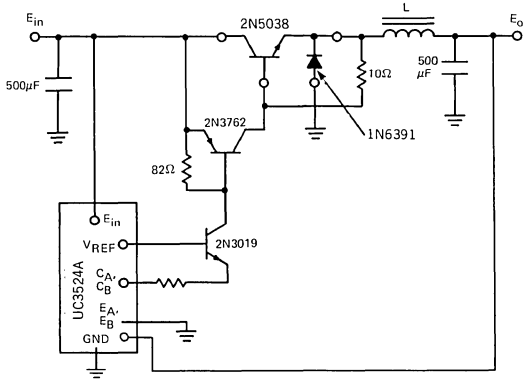


Figure 10. Simplified Schematic of 20A Buck Type High Efficiency Switching Regulator

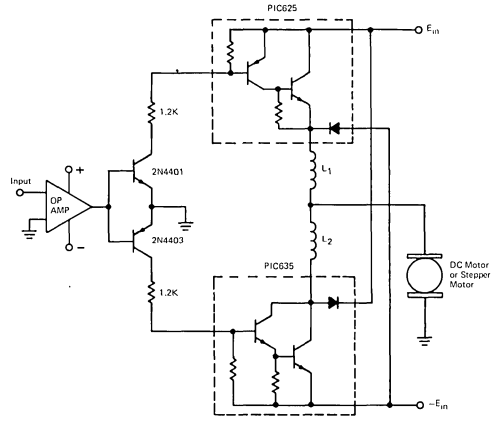


Figure 12. Bidirectional Motor Drive Circuit

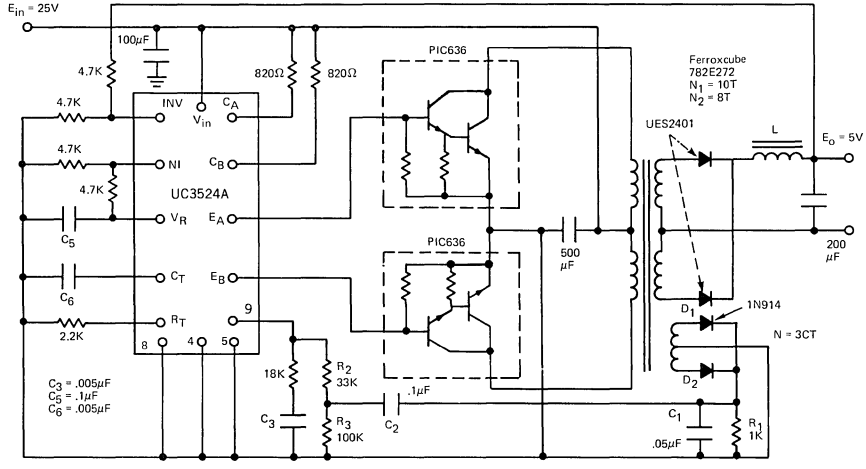


Figure 11. PWM Push-Pull Converter

VI. CONCLUSION

A wide variety of power hybrid circuits in standard packages for switched-mode converter applications have been developed by Unitrode. Power components were carefully selected for optimum electrical performance. In many instances these hybrid circuits not only provide superior electrical performance but also reduce the overall cost of the power supply by reducing production labor and repair cost.

INCORPORATE ACTIVE INRUSH CURRENT LIMITING TO IMPROVE RELIABILITY AND EFFICIENCY OF POWER SUPPLIES

Active inrush-current limiters—unlike fuses and circuit breakers—prevent dangerous situations instead of only reacting to them. Apply limiting techniques, and you need not employ extra-hefty rectifiers just to ensure rectifier survival during turn on.

The input filter capacitor employed in many power-supply designs creates a potential problem—high inrush current. Fortunately, though, adding a few extra components can prevent inrush current and its associated circuit damage.

How does the input capacitor cause such problems? Intentionally chosen for high storage capacity and low equivalent series resistance (ESR), it behaves like a nearly perfect short circuit when the supply first turns on. The resulting short-duration peak inrush current can reach levels much greater than the tolerable single-cycle ratings of the supply's semiconductor rectifiers (thus destroying them) and still not contain sufficient total energy to open protective fuses or circuit breakers. Additionally, the supply's rapidly rising voltage and current levels could cause dv/dt- or di/dt-sensitive devices in neighboring hardware to fail or malfunction.

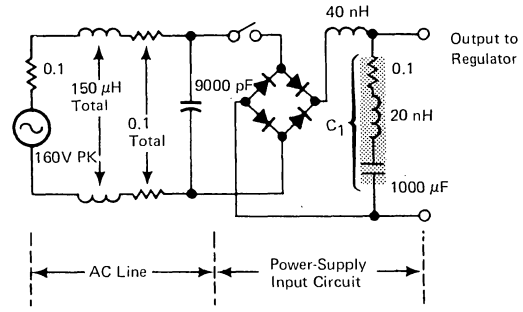
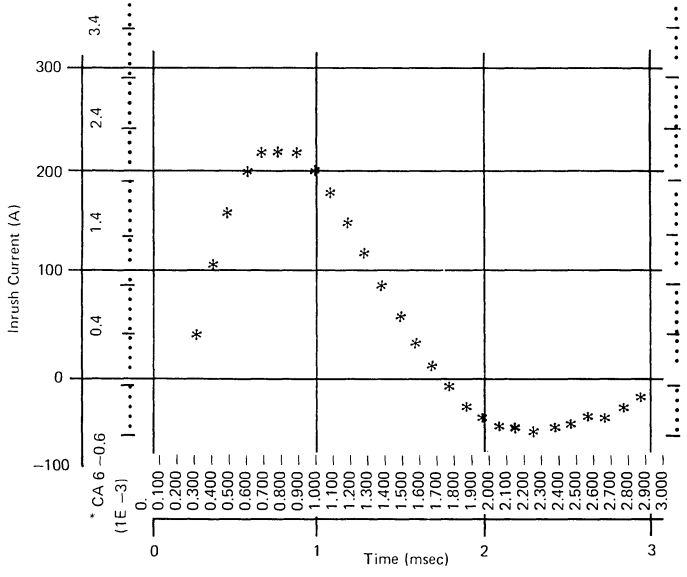


Figure 1. Based upon this generalized model, *analysis indicates the inrush-current problem's magnitude. Chosen for its low ESR, the input filter capacitor (C_1) behaves like a nearly perfect short circuit when the supply first turns on.*




```
                    ECAP
                    TRANSIENT ANALYSIS
C
B1      N(0,1), R = .1
B2      N(1,2), L = 150E − 6
B3      N(2,3), R = .1
B4      N(3,0), C = 7000E − 12
B5      N(3,4), R = .001
B6      N(4,5), L = 40E − 9
B7      N(5,6), R = .1
B8      N(6,7), L = 10E − 6
B9      N(7,0), C = 1000E − 6
E1      (1), 0, 0, 0, 160
        TIME STEP = 100E − 6
        FINISH TIME = 3E − 3
        1ERROR = 1
        PRINT NV, CA
        PLOT, (SCALED), CA(6)
        BINARY, NV, CA
```

Figure 2. Peaks greater than 200A *are predicted by ECAP for the circuit model shown in Figure 1.*

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Turn on an analysis before you turn on a power supply

Computer analysis proves useful

To appreciate the inrush-current problem, consider an estimate of its magnitude before examining possible control techniques. Figure 1 depicts a model of the ac-input and rectifier/filter sections for a typical power supply. Although shown in a straight off-the-power-mains configuration, the model should be valid for any other design with the same output-power capability.

An ECAP computer analysis performed for this circuit assumed worst-case conditions: switch closure at 160V (peak voltage). The results (Figure 3) of a typical design. The current pulse's high level and short duration could generate severe, localized hot spots in rectifier junctions or cause false triggering of rate-sensitive devices elsewhere in the circuit.

A standard approach to current limiting is depicted in Figure 4a—a resistor. It's simple, reliable and easy to design in, but efficient it isn't. At any current level, it dissipates power that would otherwise be available to the load. The resistor does perform a surge-current-limiting function, however.

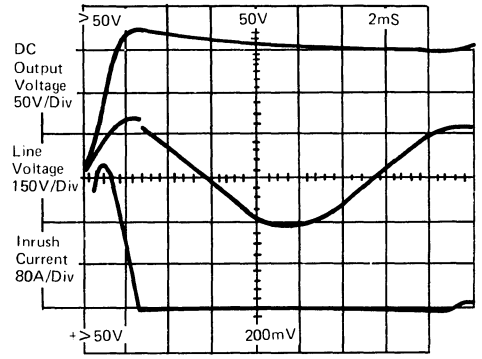


Figure 3. Measured inrush current *appears close to that predicted in Figure 2. This large current inrush could cause junction hot spots and generate troublesome EMI.*

Alternatively, a thermistor-controlled current limiter (Figure 4b) alleviates the resistor's efficiency problems to some extent, but it aggravates the dropout-recovery problem. The same cold-to-hot resistance variation that permits turn-on current limiting and high efficiency at low operating currents fails in dropout-recovery situations: The thermistor's long thermal time constant prohibits fast recovery.

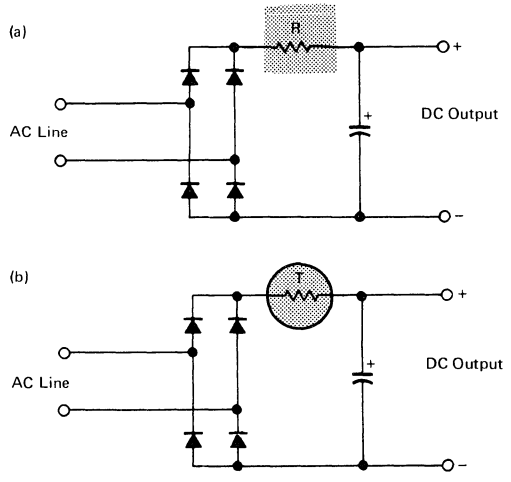
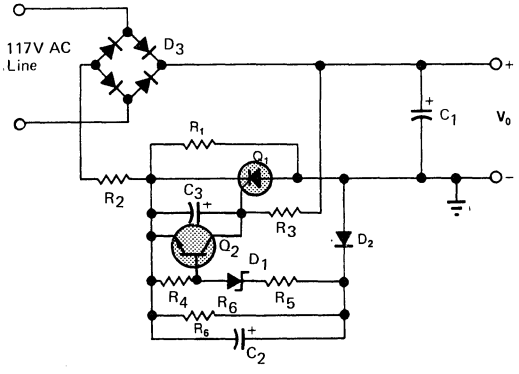


Figure 4. Two common methods *of inrush limiting employ either a resistor (a) or a thermistor (b). But if the resistor is large enough to effectively control surge currents, it also significantly reduces efficiency. The thermistor, while more efficient, offers little protection during dropout recovery because of its long thermal time constant.*



NOTES

R_1: 3, 5W	C_1: 1000 μF	Q_1: 400, V_{10A}
R_2: 0.2, 10W	C_2: 10 μF	Q_2: UPT312
R_3: 3k, 5W	C_3: 2 μF	
R_4: 1k	D_1: UZ4715	
R_5: 1k, 2W	D_2: 1N4245	
R_6: 2k	D_3: UT680-4	

Figure 5. SCR soft starting *bypasses the current-limiting resistor (R_1) only when the peak-detected voltage across Q_1 drops below the zener breakdown, i.e., when C_1 becomes almost fully charged through R_1.*

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SCR spells efficiency

In view of resistor and thermistor drawbacks, active soft-start designs offer a best-of-both-worlds solution—effective inrush limiting, fast recovery and high operating efficiency. This type of circuit, shown in Figure 5, essentially incorporates a current-limiting resistor (R_1) and a bypass switch (Q_1). At turn on, Q_1 is OFF, and the surge current (I_S) develops a voltage across R_1. This voltage is peak detected by D_2 and stored in C_2. When the voltage exceeds D_1's zener breakdown—an event that should occur almost instantaneously—Q_2 turns on, disabling Q_1's gate-triggering network (R_3C_3). As the power supply's filter capacitor C_1 charges up, the inrush peaks diminish until the detected I_SR_1 voltage falls below D_1's zener breakdown. Q_2 then turns off, and the R_3C_3 network charges up and fires Q_1, bypassing R_1.

This circuit recovers rapidly enough to limit inrush currents that could occur as a result of even short line dropouts. When the ac input voltage goes to zero, the voltage across Q_1 also goes to zero, and Q_1 turns off. When the input voltage reappears, Q_2 keeps Q_1's gate circuit OFF until R_1 has allowed C_1 to become almost fully charged.

Figure 6 graphically depicts this design's inrush-limiting ability. Note how the I_SR_1 voltage level (upper trace) tracks the diminishing inrush-current pulses (lower trace) for the first three cycles. At the 17-msec point (slightly after the third current pulse), the peak detected voltage has dropped below the zener breakdown point, and Q_1 switches on, bypassing R_1. Then R_2 limits inrush currents.

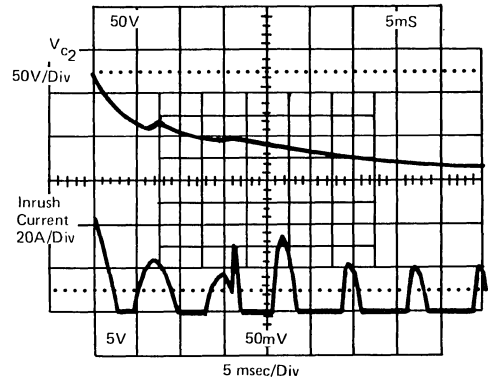

Figure 6. Inrush-current pulses of decreasing magnitude *(bottom trace) lower the SCR's hold-off voltage (upper trace). After 17 msec, the SCR fires.*

After determining your design's maximum continuous dc output current (I_O) and inrush limit (I_S), you can select an appropriate SCR. (The major SCR considerations are the peak repetitive blocking voltages and the maximum average plus peak current levels.) Typical SCRs exhibit a gate-turn-on voltage (V_{GT}) of about 0.6V; typical power-supply circuits exhibit a di/dt of about 1A/μsec—two quantities required for calculating the values of the other critical components:

$$R_1 = \sqrt{2}V_{AC}/I_S$$
$$R_2 = P_{R_2}/I_O^2$$
$$V_Z = I_SR_2$$
$$C3 \geq (2\sqrt{2}\,V_{AC}V_Z)/(R_3V_{GT}R_1(di/dt)).$$

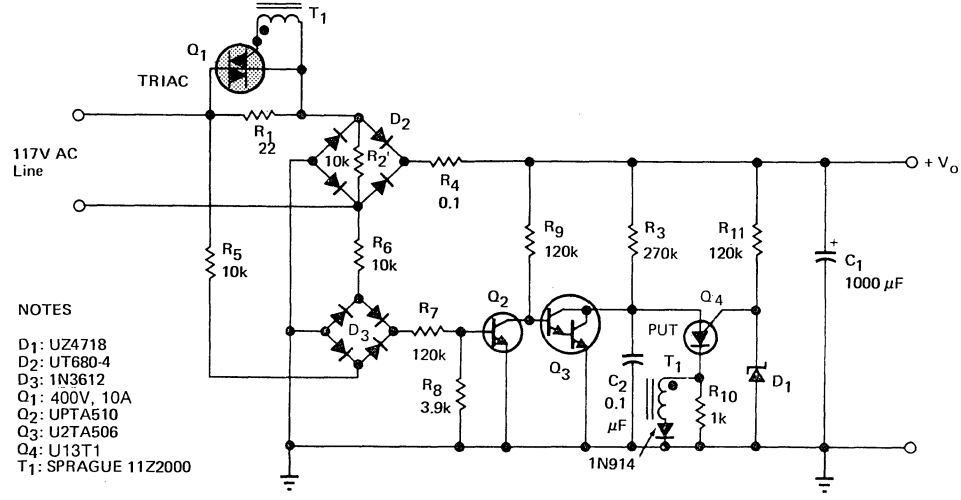

Figure 7. Phase controlling a triac *limits inrush-current pulses' amplitude and duration. Cycle-by-cycle triggering — handled by the PUT comparator — ensures instant recovery from line dropouts.*

Switch out the limiting resistor when the inrush is over

In the second equation, specify P_{R2} as the maximum power your requirements allow across R_2.

Another effective inrush-current limiter is the phase-controlled triac design shown in Figure 7, which operates by controlling the conduction time of the current surges. Initially, the dc voltage (V_O) across C_1 builds up slowly because of R_1's current-limiting action. This dc voltage helps establish a reference (via R_{11} and zener diode D_1) for the programmable unijunction transistor (PUT) Q_4 and charges the phase-control timing capacitor C_2 (via R_3). The PUT fires when its trigger point is reached, turning the triac on. Thus, when V_O is initially low, C_2 charges slowly, and the triac triggers on late in the half cycle. As V_O rises Q_1 turns on earlier in each cycle until nearly 100% conduction is achieved.

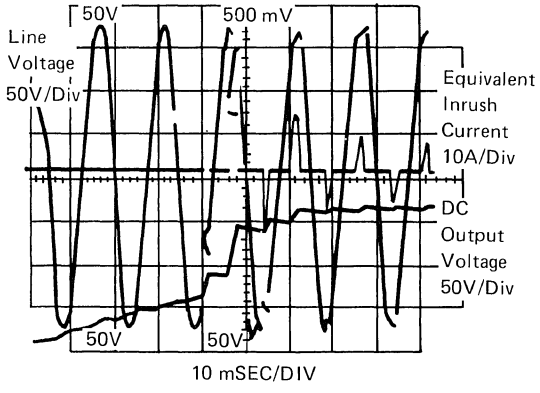

Figure 8. Triac conduction *follows the gradually increasing dc output voltage, decreasing the would-be inrush current. When the output voltage reaches design level, the triac is bypassing the current limiter nearly 100% of the time.*

The remaining circuit components (D_3, Q_2, Q_3, etc) discharge timing capacitor C_2 on each half cycle, thereby assuring cycle-by-cycle current limiting and fast recovery from dropouts. Figure 8 depicts the relationship between the ac input voltage, the dc output voltage and the varying conduction angle of the triac.

DESIGN GUIDE — POWER SCHOTTKY RECTIFIERS IN A SWITCHING REGULATOR

1. Introduction

Present technology is stimulating the development of more efficient power supplies. The switching regulated power supply is fast becoming the most popular type especially in industrial and military applications because it offers higher efficiency than a linear power supply.

Schottky rectifiers are widely used in switched-mode converters due to their inherently lower forward voltage characteristics compared with PN junction devices. Losses in the power supply are reduced considerably by the use of Schottky rectifiers, resulting in increased efficiency, improved reliability, and reduced size, weight and cost of the switched-mode converter.

In a +5V T^2L logic power supply, the efficiency of a switched-mode converter is reduced 11 to 15% due to rectifier losses. The trend is for information processing circuits to be operated at even lower voltages, making the forward characteristic of a Schottky rectifier even more important.

Since the Schottky rectifier is a majority carrier device, there is no reverse recovery characteristic caused by minority carrier storage when the devices switch from forward conduction to the blocking state. However, due to the large junction capacitance, Schottky rectifiers will exhibit reverse recovery time like a fast PN junction rectifier.

This application note describes, in brief, the theory of Schottky rectifiers and compares Schottky rectifier characteristics using different barrier metals and their effects on switching regulator efficiency.

The discussion also covers the parasitic elements in the Schottky rectifier and considers the effects of these elements in switched-mode converters. Design rules are derived for optimum snubber networks to protect against transient voltages and minimize RFI. Guidelines are provided for selecting the proper Schottky rectifier for different types of switched-mode converters.

2. Basic Structure

The basic construction of a Schottky rectifier is shown in Figure 1. The starting material is a heavily doped N^+ silicon wafer on which an N-type epitaxial layer is deposited. The resistivity of this layer determines the reverse blocking voltage capability of the rectifier. The Schottky barrier is formed by depositing a metal layer on the N-type epitaxial layer, and the junction formed between the metal and the semiconductor is an abrupt junction.

The most commonly used barrier metals or alloys are chromium, platinum, nickel platinum, molybdenum tungsten. A performance comparison of different barrier metals is summarized in Table 1. The chromium barrier provides low forward voltage with a very high leakage current. However, the tungsten barrier provides low leakage current with high forward voltage. Since efficiency is a major consideration in switched-mode converters, the nickel platinum barrier provides the best choice due to its low forward drop with a minimum of leakage current.

3. Theory And Discussion of Parasitic Elements in a Schottky Rectifier

The energy bands of a metal and semiconductor separated by a vacuum are shown in Figure 2a. This system is not in equilibrium. However, if an electrical connection is made between the semiconductor and metal, charge is allowed to flow from the semiconductor to the metal. Equilibrium will be established and the Fermi levels will become aligned.

When intimate contact is made between the metal and semiconductor, Figure 2b, the Fermi levels will line up and there will be an accumulation of positive charges at the surface of the semiconductor. A barrier will exist for electron flow from the metal to semiconductor and the barrier height will be the difference between the work function of the metal and the semiconductor.

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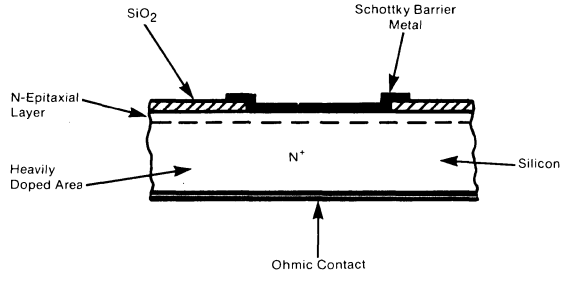


Figure 1 - Cross–Section of a Schottky Barrier Power Rectifier

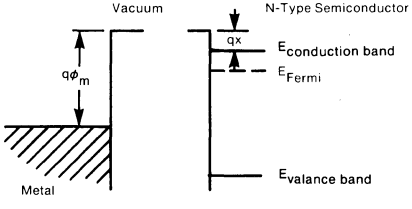


Figure 2a

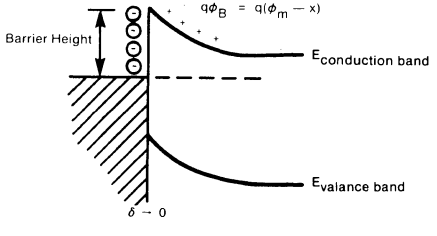


Figure 2b

Figure 2 - Energy Band Diagram of Metal Semiconductor Contact

TABLE 1 — PERFORMANCE COMPARISON OF DIFFERENT BARRIERS

SPECIFICATIONS				POWER LOST IN EACH RECTIFIER	
METAL BARRIER	V_F @ 20A (V) 125° C**	V_F @ 100A (V) 125° C**	LEAKAGE CURRENT (mA) 125° C**	LOSSES DUE TO LEAKAGE (W)*	V_F LOSSES @ 100A (W)*
Chromium	0.35	0.78	280	1.80	33.20
Molybdenum	0.45	0.75	65	0.46	34.07
Platinum	0.51	0.80	10	0.071	35.23
Ni-Platinum	0.433	0.73	30	0.2145	32.70
Tungsten	0.51	0.82	10	0.071	36.79

* Power dissipation calculations are based on 125° C operating junction temperature and a high line input voltage for an off-line PWM converter.

** V_F voltages are for 160 mil^2 die.

3.1 Forward Biased Junction

When the barrier or a junction is forward biased, the energy level of the conduction band in the semiconductor is raised, which allows electrons to flow into the metal as shown in Figure 3a. A small barrier does remain, but the electron energy distribution is sufficient to overcome this remaining barrier. Increased forward bias will overcome the barrier and current flow will be limited only by the series resistance of the device. Most of the forward drop at high current occurs in the high resistivity epitaxial layer which determines the reverse blocking voltage capability.

Schottky rectifier forward drop can be expressed by the following equation:

$$V_F = \frac{\Phi}{q} + \frac{KT}{q} \ln \left(\frac{I_F}{A \times RT^2} \right) + \frac{I_F \cdot \rho \cdot d}{A} \qquad (3.1)$$

\+ Voltage drop in ohmic contact of package

Where: I_F = Forward current (A)

A = Barrier area (cm^2)

$\frac{KT}{q}$ = 0.026 at room temperature

Φ = Barrier height - e_v

ρ = Resistivity of epitaxial layer (Ω-cm)

d = Thickness of epitaxial layer (cm)

R = Richardson constant

T = Absolute temperature (° K)

The term $[I_F \cdot \rho \cdot (d/A)]$ in the above equation is the forward drop in the high resistivity epitaxial layer and it is a significant portion of the forward drop at high current levels.

Since holes cannot exist in the metal, none can be injected into it. As a result, conduction is entirely due to electrons. This eliminates the minority carrier related reverse recovery time.

3.2 Reverse Biased Junction

When the device is reverse biased, the conduction band in the semiconductor is lowered by the applied reverse biased voltage as shown in Figure 3b. For any conduction to occur, electrons must surmount the potential barrier created at the metal-semiconductor junction. Some electrons in the metal gain sufficient thermal energy from the lattice structure to overcome the barrier while others are able to tunnel through the barrier. This leakage current is temperature dependent.

3.3 Junction Capacitance

The barrier metal and uniformly doped N-type epitaxial layer create an abrupt junction. This results in at least 5 times higher junction capacitance when compared with similar slightly graded ultra-fast PN junction devices. The depletion capacitance of a Schottky rectifier under reverse biased conditions can be expressed by the equation:

$$C = A \cdot \sqrt{\frac{(43 \cdot 10^{-6}) N_D}{V_R + 0.6 + (KT/q)}} \qquad (3.2)$$

Where: N_D = Carrier concentration of an epitaxial layer

$\frac{KT}{q}$ = 0.026 at room temperature

V_R = Applied reverse biased voltage

As can be seen from the equation, the junction capacitance is inversely proportional to the square root of the applied reverse voltage and is practically independent of temperature at reverse voltages greater than 1V. When the device switches from forward biased condition to the reverse blocking state, current is required to charge the depletion capacitance. The time required to charge up capacitance is determined by the circuit impedance. This charging current has the same effect as the reverse recovery current of a Unitrode fast recovery "UES" PN junction rectifier!

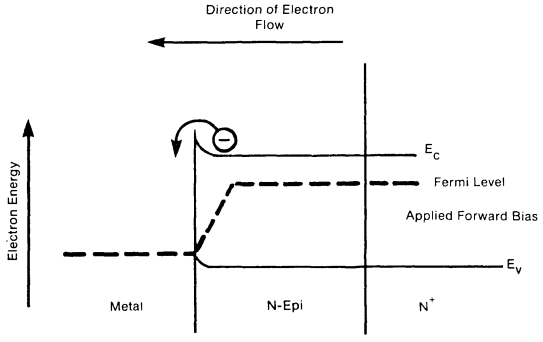


Figure 3a - Rectifier — Forward Biased

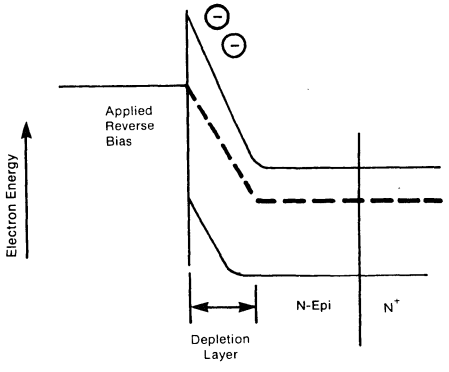


Figure 3b - Rectifier — Reverse Biased

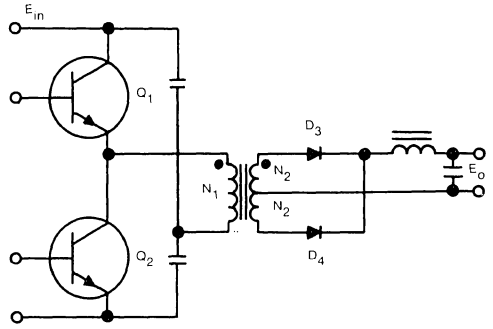
In a switched-mode converter, the apparent reverse recovery time is determined by the leakage inductance of the transformer and the junction capacitance of the Schottky rectifier. Since capacitance does not vary with temperature, the apparent recovery time and current overshoot remain constant with temperature. Ringing resonance of leakage inductance and Schottky capacitance can cause voltage overshoot. In a high frequency switched-mode converter where the transformer is designed with very low leakage inductance, careful consideration must be given in selecting the Schottky rectifier because of dv/dt limitations.

4. Applications of a Schottky Rectifier in Switched-Mode Converters

The simplified power output stage of a half-bridge switched-mode converter is shown in Figure 4a. When switching transistors Q_1 and Q_2 are in the "off" condition, diodes D_3 and D_4 conduct in the forward direction to provide a current path for inductor L_1. Each diode carries half of the load current. When transistor Q_1 turns on, current in diode D_3 starts to change from half the load current to full load current, while current in diode D_4 starts to change from half the load current into the "off" condition. Current transition time in the rectifier will depend on the current rise time of the transistor and the leakage inductance of power transformer T_2. When current in rectifier D_3 increases to full load current, current in rectifier D_4 decreases to zero.

Since a Schottky rectifier is a majority carrier device, it should turn off instantaneously. However, because of the larger junction capacitance of the Schottky rectifier compared with PN junction devices, transistor Q_1 supplies additional current to the secondary winding to charge up this larger junction capacitance. Note that the junction capacitance of the Schottky rectifier varies with reverse bias voltage as shown in Figure 5. Also the capacitance is five times that of equivalent PN junction devices.

As current is increased, the voltage across the junction capacitance of the rectifiers builds up toward the full reverse blocking state. The primary current will be higher than the output load current divided by the transformer turns ratio. During this period, energy is stored in the leakage inductance due to the excessive current on the primary side. As the



$\frac{N1}{N2}$ = N_1 transformer turns ratio
R_{PW} = Series resistance of primary windings
R_{SW} = Series resistance of one half secondary winding
L = Leakage inductance of transformer
C_{PW} = Primary windings distributed capacitance
C_{SW} = One half secondary winding capacitance
C_{ob} = Output capacitance of switching transistor
C_j = Junction capacitance of rectifier

Figure 4a - Typical Half-Bridge PWM Switching Converter

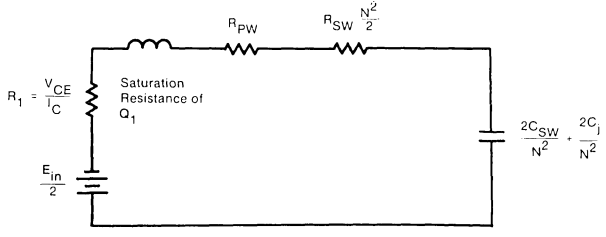


Figure 4b - Equivalent Circuit During Charging of a Junction Capacitance of a Schottky

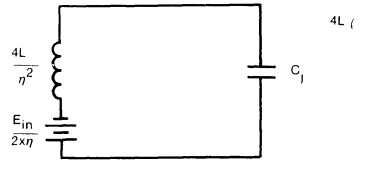


Figure 4c - Simplified Equivalent Circuit Referred Back to Secondary Side

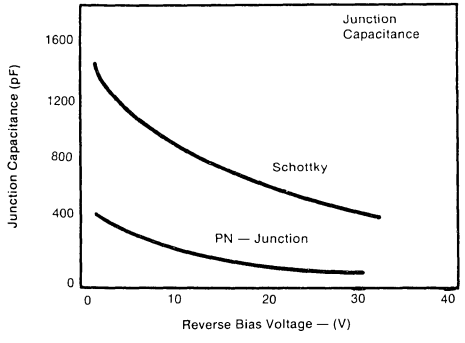


Figure 5 - Comparison of Junction Capacitance ultra-fast PN-Junction vs. Comparable Schottky Rectifier

voltage across the rectifier reaches full switching voltage, energy stored in the leakage inductance continues to charge up the junction capacitance of the rectifier above the switching voltage reflected back in the secondary. These voltages can force the device into the breakdown region if the proper snubber circuit is not employed.

4.1 Snubber Network Design

The equivalent circuit referred back to the primary side when the junction capacitance is charging up is shown in Figure 4b. The junction capacitance of the Schottky and the leakage inductance of transformer T_2 form a resonant circuit. The winding resistances, R_{PW} and R_{SW}, and saturation resistance, R_1, provide very little damping to this LC tuned circuit. Therefore, its effect on damping can be neglected. The interwinding capacitance of the power transformer is much lower than the junction capacitance of the Schottky rectifier and may be neglected. The simplified circuit referred back to the secondary side is shown in Figure 4c.

Since Schottkys are prone to excessive heating and possible damage in the breakdown mode, a proper snubber is required. The design of the snubber network minimizes voltage spikes and snubber losses. The snubber network also helps to reduce conducted and radiated RFI.

The optimum snubber network should be designed on the basis of critical damping of the LC tuned circuit and limiting the maximum excursion of the voltage below the PIV ratings of the rectifier.

Shown below is the LC tuned circuit with resistor R_{snb} paralleled across the junction capacitance of the Schottky rectifier for a critically damped condition.

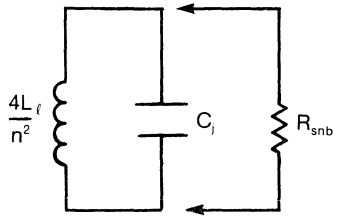


Figure 6 - Damping Resistor R_{snb} Added Across the LC Tuned Circuit for Critical Damping

The loaded Q_L should be 0.5 for a critically damped case to prevent any ringing of the voltage and to provide minimum losses in the snubber resistor. LC tuned circuits will have only real roots. Loaded Q_L can be described by the equation:

$$Q_L = 0.5 = \frac{R_{snb}}{X_L} \qquad (4.1)$$

Where: $X_L = j\omega L$

$$\therefore R_{snb} = 0.5 \cdot \omega \cdot L$$

$$= 0.5 \left(\frac{1}{\sqrt{(4L_\ell/n^2)C_j}} \right) \left(\frac{4L_\ell}{n^2} \right)$$

$$R_{snb} = \frac{1}{n} \sqrt{\frac{L_\ell}{C_j}} \qquad (4.2)$$

Where: C_j = Junction capacitance of rectifier

L_ℓ = Leakage inductance of power transformer

A capacitor is required in series with the resistor in order to block the dc voltage present. The blocking capacitor should be at least ten times the rectifier junction capacitance:

$$C_{snb} = 10(C_j) \qquad (4.3)$$

To transfer the power effectively from the input power source to the output load, the time constant (R_{snb} x C_{snb}) should at at most one-tenth the minimum pulse width of the switched-mode converter. This occurs at maximum input voltage. Therefore:

$$R_{snb} \cdot C_{snb} \leq \frac{(1/20)}{f} (E_{in_{min}}/E_{in_{max}}) \qquad (4.4)$$

Where: f is the operating frequency of the switching regulator.

The power dissipation in the snubber resistor R_{snb} can be calculated by the equation:

For Half-Bridge:

$$PR_{snb} = \tfrac{1}{2}C_{snb} \left[\frac{E_{in_{max}}}{n} \right]^2 \cdot f \qquad (4.5)$$

For Push-Pull for Full-Bridge:

$$PR_{snb} = \tfrac{1}{2}C_{snb}\left[\frac{2(E_{in_{max}})}{n}\right]^2 \cdot f \qquad (4.6)$$

Where: $E_{in_{max}}$ = Maximum input voltage
n = Primary to secondary turns ratio of power transformer

Every inch of wire represents 20 nanohenries of inductance. When the output current is high, the energy stored in the lead and package inductance in the secondary circuit can generate high voltage spikes across the rectifier during reverse recovery time. To reduce these spikes, two snubber networks are required. One should be placed across each Schottky rectifier as shown in Figure 7 below.

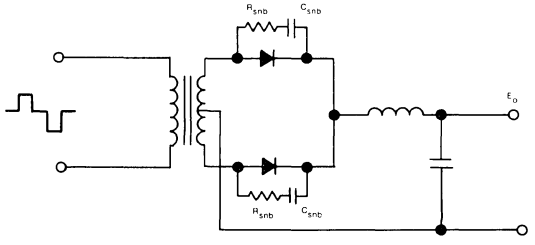


Figure 7 - High Current Outputs

For low current outputs, the snubber network can be connected across the secondary winding as shown in Figure 8.

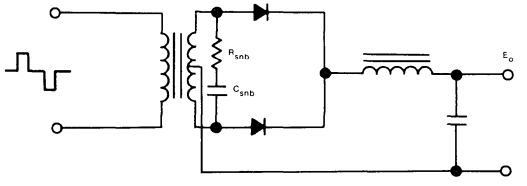


Figure 8 - Low Current Outputs

4.2 *Reverse Recovery Time and Overshoot Current, $I_{RM(REC)}$*

Reverse recovery time is defined as the time required to change a rectifier from the forward conduction state to the reverse blocking state. Although a Schottky rectifier is a majority carrier device, it takes time to "recover" because of its high junction capacitance. In a switched-mode converter, reverse recovery time is, to a large extent, determined by the parasitic leakage inductance of the transformer which resonates with the junction capacitance of the Schottky rectifier. Design equations for reverse recovery time and current overshoot can be derived as shown below.

Reverse Recovery Time:

From basic equations of an LC tuned circuit:

$$\omega = \frac{1}{\sqrt{LC}}$$

Substituting $f = 1/\tau$ and rearranging:

$$\tau = 2\pi\sqrt{LC}$$

Since $\tau/2 = t_{rr}$ by definition:

$$t_{rr} = \pi\sqrt{LC} \qquad (4.7)$$

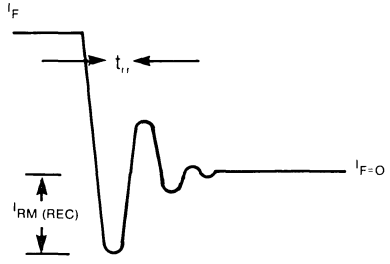


Figure 9 - Reverse Recovery Time of a Rectifier

Assuming the rise time of the transistor is much faster than t_{rr} of the rectifier, and substituting L_ℓ = leakage inductance of the transformer and C_j = junction capacitance of the Schottky rectifier. Neglecting the interwinding capacitance of the transformer, the reverse recovery time (when no snubber network is employed across the rectifier) can be calculated by the equation:

t_{rr} due to junction capacitance:

$$t_{rr} = \frac{2\pi}{n}\sqrt{L_\ell(C_j)} \qquad (4.8)$$

Where: n = Primary to secondary turns ratio

The ringing frequency can be calculated by the equation:

$$f = \frac{n}{4\pi\sqrt{L_\ell (C_j)}} \quad (4.9)$$

From the characteristic impedance of the LC tuned circuit, overshoot current, I_{RM}, in the Schottky rectifier can be calculated by:

$$I_{RM(REC)} = \frac{E_{in}}{2}\sqrt{\frac{C_j}{L_\ell}} \quad (4.10)$$

4.3 Practical Example

A detailed diagram of a 150W, multiple output switching regulated power supply is shown in Figure 10. The power supply is designed to operate with a line input voltage of 117V ac, 60 Hz or 220V ac, 50 Hz. The regulated output voltages are +5V @ 1A, +12V @ 1.2A, -12V @ 1A and -5V @ 1A. The output voltage is regulated by power switching hybrid circuits Q_1 and Q_2 which are housed in four pin electrically isolated packages.

Since the case is electrically isolated from the active devices, it provides the following advantages:

a) lower conducted and radiated RFI
b) ease in mounting — two devices can be mounted on the same heat sink.

The selected switching transistor provides fast switching time (<100ns) and the diode in the hybrid circuit provides low reverse recovery (<50ns) and forward recovery time. The proportional base drive current to the switching transistor is supplied by the current transformer T_1.

One of the output voltages (+5V) is regulated with a pulse width modulated (PWM) control chip Unitrode's UC3524. The auxiliary voltage to power the control circuit should be electrically isolated from the line voltage. Conventionally, the 60 Hz transformer is utilized to provide isolation and the transformer output voltage is rectified and regulated to supply bias voltage to the control circuit. Transistors, Q_3 and Q_4, provide a low cost approach in developing bias voltage for the control circuit without the use of a 60 Hz transformer. The operation of the circuit is described in detail below.

When the 117V ac input line voltage is applied to the switched-mode converter, capacitors C_1 and C_2 charge up to full input voltage. Meanwhile capacitor C_T charges up slowly through resistor R_T. When the voltage across C_T reaches the anode-gate voltage of the programmable unijunction transistor Q_4, it will turn on and dump the stored charge from capacitor C_T into one of the proportional base drive windings of the transformer T_1. The polarity of the windings is such that it will turn on only transistor Q_2, transferring energy from input capacitor C_2 into the output capacitor C_3 (isolated from the input line) through power transformer T_2. The control circuit LM3524 starts to switch transistor Q_2. At the instant when transistor Q_2 turns on, capacitor C_T will be isolated from current transformer T_1 with the help of transistor Q_3. The programmable unijunction transistor Q_4 now remains off. The capacitor C_3 is now continuously charging up through the secondary winding of the transformer.

The output circuit of the switched-mode converter utilizes coupled inductor L_1 to provide better tracking among all the output voltages and improve transient response. Coupled inductor L_2 (which is not in the control loop) maintains the sawtooth current in the +5V winding of L_1 (which is in the control loop) providing stability in the control circuit.

Calculations of Snubber Network:

In the 150W switching regulator shown in Figure 10, first calculate the current overshoot $I_{RM(REC)}$, the ringing frequency and the apparent reverse recovery time without the snubber network. Then determine the resistor and capacitor values (for critically damped case) of the network across the Schottky rectifier.

Given: L_ℓ, Leakage inductance of power transformer = 22μH

C_j, Junction capacitance of Schottky = 850pF

f, Operating frequency = 30 KHz

n, Primary to secondary turns ratio = 14

$E_{in_{min}}/E_{in_{max}}$, Ratio of maximum input voltage to minimum input voltage = 400/200 = 2

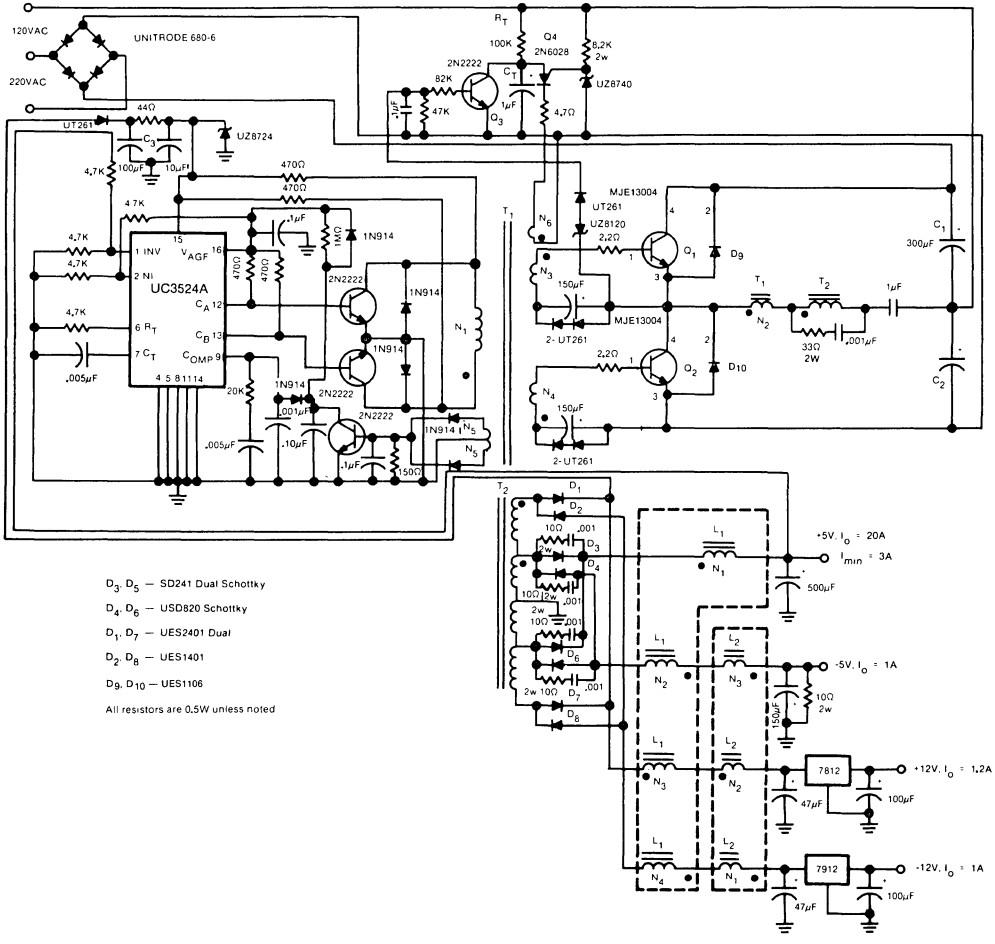


Figure 10 - 150 Watt Multiple Output "OFF Line" Switched-Mode Converter

Solution:

Current overshoot, $I_{RM(REC)}$, from Equation 4.10:

$$I_{RM(REC)} = \frac{E_{in}}{2}\sqrt{\frac{C_j}{I_\ell}}$$

$$= \frac{320V}{2}\sqrt{\frac{850 \times 10^{-12}}{22 \times 10^{-6}}}$$

$$= 1A$$

The ringing frequency from equation 4.9:

$$f = \frac{n}{4\pi\sqrt{L_\ell(C_j)}}$$

$$= \frac{14}{4\pi\sqrt{(22 \times 10^{-6})(850 \times 10^{-12})}}$$

$$= 8.1\ MHz$$

The apparent reverse recovery time from equation 4.8:

$$t_{rr} = \frac{2\pi}{n}\sqrt{C_j(L_\ell)}$$

$$= \frac{2\pi}{14}\sqrt{(850 \times 10^{-12})(22 \times 10^{-6})}$$

$$= 67ns$$

The value of the snubber resistor from Equation 4.2:

$$R_{snb} = \frac{1}{n}\sqrt{\frac{L_\ell}{C_j}}$$

$$= \frac{1}{14}\sqrt{\frac{22 \times 10^{-6}}{850 \times 10^{-12}}}$$

$$= 10.9\Omega$$

The value of the snubber capacitor from Equation 4.3:

$$C_{snb} = 10(C_j)$$

$$= 10(850 \times 10^{-12})$$

$$= 0.01\mu F$$

The power dissipation in snubber resistor, R_{snb}, from Equation 4.5:

$$PR_{snb} = \tfrac{1}{2}C_{snb}\left[\frac{E_{in_{max}}}{n}\right]^2 \cdot f$$

$$= \tfrac{1}{2}(0.01 \times 10^{-6})\left[\frac{400}{14}\right]^2 \cdot 30 \times 10^3$$

$$= 0.121W$$

∴ The snubber resistor R_{snb} should have at least 0.5W rating.

The criteria for the snubber network should satisfy the conditions below:

$$R_{snb}(C_{snb}) \leq \frac{1}{20f}\left[\frac{E_{in_{min}}}{E_{in_{max}}}\right]$$

$$10\Omega(0.01 \times 10^{-6}) \leq \frac{1}{20(30 \times 10^3)} \cdot \frac{1}{2}$$

$$0.1\mu s \leq 0.993\mu s$$

The voltage across the Schottky rectifier with and without the snubber network in a 150W off-line switched-mode converter is shown in Figures 11a and 11b. Note that the voltage across the Schottky rectifier with a snubber network has no voltage overshoot. Thus, it prevents failure of the Schottky due to large voltage transients during transistor turn-on. The ringing frequency is about 10 MHz without the snubber and is close to calculated values.

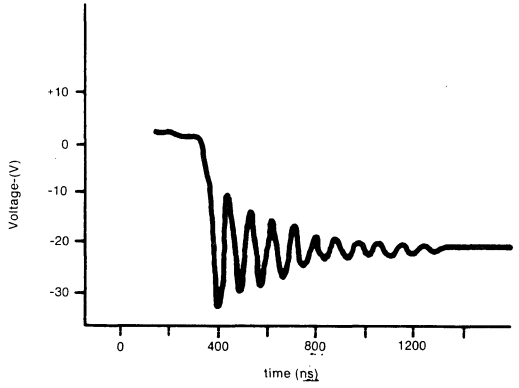


Figure 11a - Voltage Across Rectifier Without Snubber Network

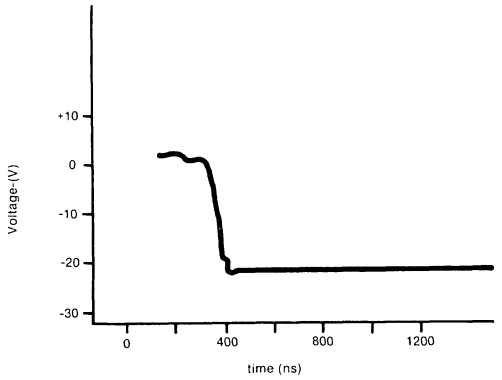


Figure 11b - Voltage Across Rectifier With Snubber Network 10Ω - 0.1μF

4.4 Thermal Stability Considerations

The reverse leakage current of a Schottky rectifier is much higher than PN junction devices because of the Schottky's lower barrier height. The magnitude of this leakage current doubles approximately every ten degrees Centigrade. Since it is temperature sensitive, the thermal stability of the system should be checked over to avoid thermal runaway. In a PWM switched-mode converter (i.e. push-pull, half-bridge, etc.) the rectifier can be operated at 50% duty cycle in the reverse blocking state while the remaining 50% of the time it will operate in the forward conduction mode under worst case conditions. However, forward drop is also a temperature sensitive parameter and this should also be considered when thermal stability calculations are made.

The criteria for thermal stability is defined as: "the rate of change in power pumped into a device with respect to temperature (dP_{in}/dt) should be less than the rate of change in power removed (in the applicable thermal environment) in the form of heat from the device with respect to temperature (dP_{out}/dt)".

In a switched-mode converter, the power dissipated in the device and the power removed can be expressed by:

$$V_R \cdot \frac{I_L(\tau - t_{on})}{\tau} + I_F \cdot V_F \cdot \frac{t_{on}}{\tau} \leq \frac{T_J - T_A}{R_{\Theta J\text{-}A}} \qquad (4.11)$$

Where: V_R = Applied reverse voltage
I_L = Leakage current at temperature
t_{on} = Rectifier on-time
τ = 1/f, where f is the operating frequency
I_F = Forward current
V_F = Forward voltage at forward current (at temperature)
T_J = Junction temperature

Since both I_L and V_F are temperature sensitive parameters, we can express I_L and V_F as functions of temperature in the above equation for thermal stability and obtain:

$$\left[\left\{\frac{(\tau - t_{on})}{\tau} \cdot V_R \cdot I_o \cdot 2^{\frac{(T_J - T_A)}{y}}\right\} + \left\{I_F \cdot \frac{t_{on}}{\tau} \cdot [V_{F_0} + X(T_J - T_A)]\right\}\right] \leq \frac{T_J - T_A}{R_{\Theta JA}} \qquad [4.12]$$

Where: I_o = Leakage current at room temperature
V_{F_0} = Forward voltage drop at room temperature
x = Temperature coefficient for forward voltage at operating current
y = Temperature difference for which leakage current doubles.

Differentiating the above equation:

$$\frac{(\tau - t_{on})}{\tau} \cdot V_R \cdot I_o \cdot 2^{\frac{(T_J - T_A)}{y}} \cdot \frac{1}{y} \cdot \ln 2 + I_F \cdot \frac{t_{on}}{\tau} \cdot X \leq \frac{1}{R_{\Theta J\text{-}A}} \qquad [4.13]$$

Defining $I_o \cdot 2^{\frac{(T_J - T_A)}{y}}$ as the critical current, $I_{R(crit)}$ at maximum temperature, and solving for $I_{R(crit)}$ we obtain:

$$I_{R(crit)} \leq y \left[\frac{(\tau/R_{\Theta J\text{-}A}) - I_F \cdot t_{on} \cdot X}{.693\,(\tau - t_{on})V_R}\right] \qquad [4.14]$$

Design Example

In the practical example previously discussed, the maximum reverse voltage across the rectifiers is 30V. Each rectifier is mounted on a heat sink. The

thermal resistance of the heat sink is 1° C/W. The Schottky rectifier, SD241, has a maximum thermal resistance of 1.4° C/W from case to junction. Its reverse leakage current doubles every ten degrees Centigrade, while the forward voltage at I_F=20A decreased by 1mV/° C as the junction temperature increases. The designer desires to limit the maximum operating junction temperature of the Schottky rectifier to 125° C under worst case conditions

Calculate the maximum reverse leakage current allowed for these rectifiers at 125° C to prevent thermal instability

Calculation:

$$R_{\theta JA} = (R_{\theta H} + R_{\theta J\text{-}C})\ ^\circ C/W$$
$$= 1^\circ C/W + 1.4^\circ C/W$$
$$= 2.4^\circ C/W$$
$$t_{on} = 16.6\mu s$$
$$t_{off} = 16.6\mu s$$
$$\tau = t_{on} + t_{off} = 33.2\mu s$$

Using equation 4.14:

$$I_{R(crit)} \leq 10^\circ C \times \left[\frac{(33.2 \times 10^{-6})/(2.4^\circ C/W) - (20A)(16.6 \times 10^{-6})(-1 \times 10^{-3}V)}{.693(33.2 \times 10^{-6}\ sec - 16.6 \times 10^{-6})(30V)}\right]$$

$$\leq 410mA$$

From the SD241 specification, the maximum reverse leakage current at 125° C is 100mA; therefore this system will be thermally stable.

4.5 Paralleling Rectifiers

When the output current required is greater than the maximum rated forward current of commercial rectifiers, it becomes necessary to parallel the devices. In some instances, it may be preferable to parallel devices even when a single device of higher current ratings is available. The advantages of paralleling these devices are:

1) Heat is easier to remove when compared to a single device with a higher current rating because the heat is spread between two or more devices.
2) The transformer is easier to wind since the wire size is smaller, using a separate winding for each rectifier.
3) Smaller chip size will have less chance of voids in the chip bond to the package, thus, the reliability of the system is improved.

The disadvantage of paralleling rectifiers is that some kind of circuit technique is required to share the current among the paralleled devices. If the current is not shared equally, the junction temperature of the device which conducts the higher current will increase. The forward voltage of the device will decrease due to its increased temperature and will conduct an even larger share of the load current. If adequate matching is not provided, this regenerative process continues; and if not checked in time, the junction temperature will exceed the maximum rating and the device will be damaged.

In switched-mode converter applications, current sharing can be accomplished by using separate windings for each rectifier and by matching forward drops. The series resistance of each winding acts as a current ballasting impedance.

5. Guidelines for Selecting the Schottky Rectifier in Pulse Width Mode (PWM) Switched-Mode Converter Applications

The minimum required dc blocking voltage of the Schottky rectifier and its maximum power dissipation can be calculated for different types of switched-mode power supplies summarized in Tables II and III. After calculating the maximum power dissipation, the designer can determine the required thermal resistance of the rectifier and the heat sink using the equation:

$$R_{\theta H} + R_{\theta JC} = \frac{T_{jmax} - T_{Amax}}{P_{max}} \qquad [5.1]$$

Where: $R_{\theta JC}$ = Thermal resistance of rectifier
$R_{\theta H}$ = Thermal resistance of heat sink
T_{jmax} = Maximum operating junction temperature of device
T_{Amax} = Maximum ambient temperature

When calculations are made for maximum power dissipation in a rectifier, the voltage drop V_F and leakage current I_R should be taken at the maximum operating junction temperature.

During start up and for step changes in the output load current, the voltage across the rectifier should be limited to below its maximum dc blocking voltage to avoid failures due to transient voltage across the Schottky.

TABLE 1 — GUIDELINES FOR DETERMINING THE RATING OF A RECTIFIER IN A PWM SWITCHED-MODE CONVERTER

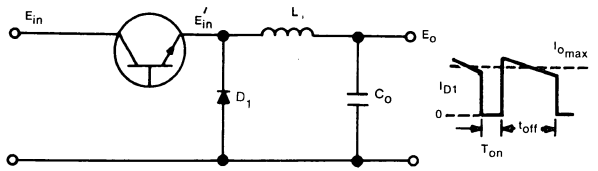
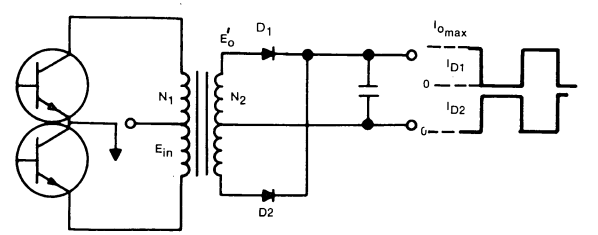
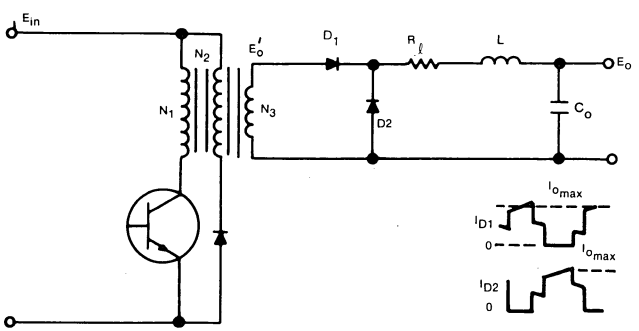
TYPES OF SWITCHING REGULATORS	OUTPUT VOLTAGE	STEADY STATE — POWER DISSIPATION IN RECTIFIERS	MINIMUM DC BLOCKING VOLTAGE REQUIRED
BUCK REGULATOR  	$E_o = E'_{in} \times \frac{t_{on}}{T}$ $E_o \approx E_{in} \times \frac{t_{on}}{T}$	Power dissipation in Diode D_1 due to forward conduction: $P_{D1_F} = I_{o_{max}} \times V_F \cdot \frac{E_{in_{max}} - E_o}{E_{in_{max}}}$ Power dissipation due to leakage current, I_R: $P_{D1_R} \leq I_R \times E_o$. $I_R @ E_{in_{max}}$	For Diode D_1: $1.2 \times E_{in_{max}}$
PUSH-PULL CONVERTER (50% Duty Cycle)  	$E'_o = E_o + V_F$ $E_o = E_{in} \times \frac{N_2}{N_1}$	Power dissipation in Rectifier D_1 or D_2 due to forward conduction: P_{D1_F} or $P_{D2_F} = \frac{I_{o_{max}} \times V_F}{2}$ Power dissipation due to leakage current, I_R: P_{D1_R} or $P_{D2_R} = 2.0 \times E_{in_{max}} \times \frac{N_2}{N_1} \times I_R$	For D_1 or D_2: $2.4\ (E_{in_{max}}) \times \frac{N_2}{N_1}$
PWM FORWARD CONVERTER  	$E'_o = E_o + V_F + I_{o_{max}} \times R$ $E_o = E_{in_{min}} \frac{N_3}{N_1 + N_2}$ Where: E_o = dc Output Voltage E'_o = Output of Secondary Winding When D_1 is conducting	Power dissipation due to forward conduction in Rectifier D_1: $P_{D1_F} = I_{o_{max}} \times V_F \frac{N_1}{N_1 + N_2}$ Power dissipation in Rectifier D_2: $P_{D2_F} \approx I_{o_{max}} \times V_F \left[1 - \frac{N_1}{N_1 + N_2} \cdot \frac{E_{in_{max}}}{E_{in_{min}}}\right]$ Power dissipation due to reverse leakage current: $P_{D1_R} = E_{in_{min}} \cdot I_R \cdot \frac{N_3}{N_1 + N_2}$ $P_{D2_R} = I_R \times \frac{N_3}{N_1 + N_2} \times E_{in_{min}}$	For D_1: $1.2 \times E_{in_{max}} \times \frac{N_3}{N_2}$ For D_2: $1.2 \frac{E_{in_{max}} \times N_3}{N_1}$

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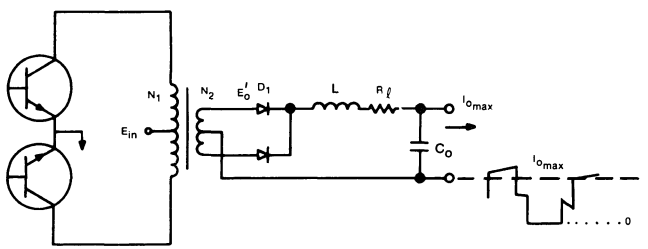
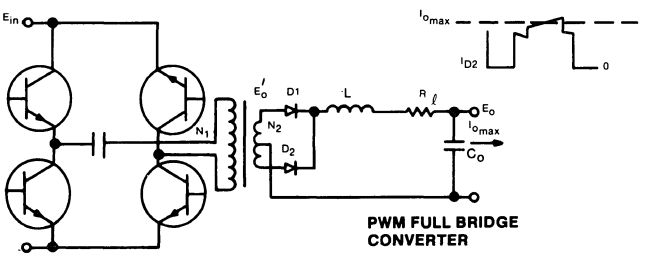
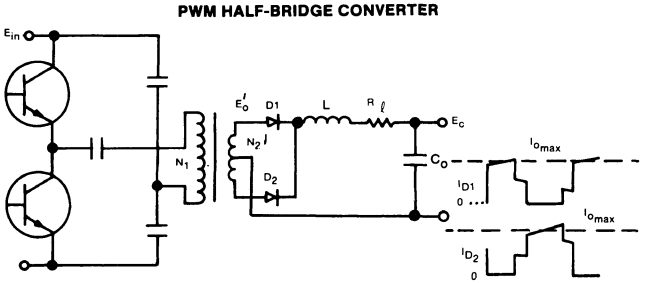
TABLE II

TYPES OF SWITCHING REGULATORS	OUTPUT VOLTAGE	STEADY STATE — POWER DISSIPATION IN RECTIFIERS	MINIMUM DC BLOCKING VOLTAGE REQUIRED
PWM PUSH-PULL CONVERTER   **PWM FULL BRIDGE CONVERTER**	$E_o' = E_o + V_F + I_{omax} \times R_\ell$ $E_o = E_{in_{min}} \times \frac{N_2}{N_1}$ For Push-Pull and Full Bridge	Power dissipation in Rectifier D_1 or D_2 due to forward conduction: P_{D1_F} or $P_{D2_F} = \frac{I_{omax} \times (V_F @ I_{omax})}{2} \times \frac{E_{in_{min}}}{E_{in_{max}}}$ $+ \frac{I_{omax}}{2} \left(V_F @ \frac{I_{omax}}{2}\right) \times \frac{E_{in_{max}} - E_{in_{min}}}{E_{max}}$ Power dissipation due to leakage current: P_{D1_R} or $P_{D2_R} = I_R(E_{in_{min}})(N_1/N_2)$ NOTE: $I_R @ 2(E_o + V_F + I_{omax} \times R\ell) \times \frac{E_{in_{max}}}{E_{in_{min}}}$	For D_1 or D_2: $2.4 (E_o + V_F + R$ $\times I_{omax}) \times \frac{E_{in_{max}}}{E_{in_{min}}}$
PWM HALF-BRIDGE CONVERTER  	$E_o' = E_o + V_F \times I_{omax} \times R_\ell$ $E_o = \frac{E_{in_{min}}}{2} \times \frac{N_2}{N_1}$ For Half-Bridge	SAME AS ABOVE	SAME AS ABOVE

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6 Conclusion

Complete design guidelines for Schottky rectifiers used in switched-mode converters have been provided. The Schottky, when compared to a fast PN junction rectifier, offers the advantages of lower forward voltage and a faster reverse recovery time which is independent of temperature. Efficiency is improved at least 3 to 5% when Schottky rectifiers are used in place of PN junction devices for power rectification in switched-mode converters. Schottky rectifiers are available with a maximum reverse blocking voltage up to only 50 to 60V. Thus, applications of Schottky devices are limited to low output voltages (+5V) in PWM switched-mode converters (except for buck type and 50% duty cycle converters). When the rectifier requires voltage blocking capability of greater than 60V, fast PN junction devices like UES800 series rectifier offers the optimum choice without sacrificing speed and forward voltage.

SCHOTTKY RECTIFIERS

AVERAGE DC OUTPUT CURRENT		6A	8A	12A[1]	12A	16A[2]	16A	25A	30A	50A	60A	75A
PEAK REVERSE VOLTAGE \ PACKAGE		TO-220 PLASTIC (2-LEAD)	TO-220 PLASTIC (2-LEAD)	TO-220 PLASTIC (3-LEAD)	TO-220 PLASTIC (2-LEAD)	TO-220 PLASTIC (3-LEAD)	TO-220 PLASTIC (2-LEAD)	DO-4 STUD	TO-3	DO-5 STUD	DO-5 DO-5F STUD	DO-5 DO-5F STUD
20V	TYPE V_F I_{FSM}	USD620 .55 @ 6A 150A	USD720 .55 @ 8A 200A	USD620C .65 @ 12A 150A	USD820 .45 @ 12A 200A	USD720C .65 @ 16A 200A	USD920 .50 @ 16A 250A		USD320 .6 @ 20A 400A			USD520 .6 @ 60A 1000A
30V	TYPE V_F I_{FSM}									1N6097 .86 @ 157A 800A		
35V	TYPE V_F I_{FSM}	USD635 .55 @ 6A 150A	USD735 .55 @ 8A 200A	USD635C .65 @ 12A 150A	USD835 .45 @ 12A 200A	USD735C .65 @ 16A 200A	USD935 .50 @ 16A 250A		USD335C .6 @ 20A 400A			USD535 .6 @ 60A 1000A
40V	TYPE V_F I_{FSM}	USD640 .55 @ 6A 150A	USD740 .55 @ 8A 200A	USD640C .65 @ 12A 150A	USD840 .45 @ 12A 200A	USD740C .65 @ 16A 200A	USD940 .50 @ 16A 250A			1N6098 .86 @ 157A 800A		
45V	TYPE " V_F I_{FSM}	USD645 .55 @ 6A 150A	USD745 .55 @ 8A 200A	USD645C .65 @ 12A 150A	USD845 .45 @ 12A 200A	USD745C .65 @ 16A 200A	USD945 .50 @ 16A 250A	1N6391[4]	USD345C SD241 .6 @ 20A 400A		1N6392[4] SD51[4] .6 @ 60A 800A	USD545 .6 @ 60A 1000A

1. CENTER-TAP 6A PER LEG
2. CENTER-TAP, 8A PER LEG
3. V_R AT 25° C IS 45V, V_R AT 150° C IS 35V
   JTX and JTXV

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500W, 200kHz OFF-LINE POWER SUPPLY USING POWER MOSFETS

Introduction

The power supply design discussed in this application note uses a fairly common, straight-forward circuit. It is the judicious selection of the components used, and careful layout of the circuit, which gives it its performance. As the operating frequency of switching power supplies continues to increase above 100kHz, attention to high frequency considerations is a necessity. A knowledge of component and circuit parasitics is essential as well as an understanding of RLC circuits and transient response, particularly LC resonant tank circuits. Because of the resonance of parasitic circuit and component inductance and capacitance at these high frequencies, the use of damping and snubbing techniques becomes increasingly important.

In the off-line converters some of these high frequency problem areas are aggravated by the large turns ratio of the step-down transformer, particularly for low voltage (5V) outputs. The use of Schottky rectifiers with their 5 to 10 times larger junction capacitance than PN junction rectifiers can cause additional difficulty with the design. At 200kHz these problems are manageable by careful component selection and circuit layout.

Specifications

Input - 115V or 220V ± 15%, 50Hz or 60Hz
Output - 5V @ 100A
Regulation - Line: 0.4%
Load: 0.5% (10% to 100% load)
Ripple: 100mV peak to peak
Frequency - 200kHz
Efficiency - 75% minimum

Circuit Description

The schematic and parts list of a 500W switching power supply are shown in Figure 9. The description of the circuit is as follows. The input rectifier bridge is arranged for connection either to the 117 or the 220V AC line. The circuit uses a pair of Unitrode UFN441 power MOSFETs in a half-bridge configuration. The MOSFET gates are driven directly from a UC3525A control chip output through step down and isolation transformer T_1. The UC3525A output terminals (pins 11 and 14) provide active pull-up and pull-down (dual source/sink) for the primary of T_1. This provides the fast, high current turn-on and turn-off pulses needed for the MOSFET gates. In addition, the two ends of the primary winding are shorted to ground during deadtime, which prevents accidental turn-on of an output transistor by transients. Note that the current supplied by the UC3525A output drops to a small value when the gate capacitance has been charged or discharged to the desired gate voltage. Damping resistors R_3 and R_4, with series blocking capacitors C_{16} and C_{17}, minimize ringing of the MOSFET gate capacitance with the inductance of T_1 and lead inductance; particularly during deadtime. In this design, where the gates are driven directly from the control chip via the gate drive transformer at 200kHz, it is necessary to use a small heat sink for the control chip. A Thermalloy #6007 is sufficient.

The output transformer uses a small E-E core, Ferroxcube EC52-3C8, operated at 1000 Gauss peak to reduce core loss at 200kHz. The primary is wound in 2 layers, 7 turns per layer, 2 #16 AWG wires in parallel. The secondaries are wound between the 2 primary layers to reduce leakage inductance, and are made of copper strap 10 mils thick by 0.8 inches wide, one turn on each side of the centertap.

Ringing of the primary winding, at a frequency of approximately 4MHz due to leakage inductance resonating with the output capacitance of the MOSFETS, is controlled by damping resistor R_{18} and blocking capacitor C_4.

Reverse voltage across Schottky rectifiers CR_1 to CR_4, due to ringing (at approximately 20MHz) of the LC circuit comprised of the Schottky rectifier capacitance with the leakage inductance of the transformer (transformed to the secondary by the square of the turns ratio), is controlled by damping resistors R_7 to R_{10} with blocking capacitors C_{10} to C_{13}.

The output filter capacitor C_5 is comprised of three 5μF, 100V polypropylene capacitors in parallel. These are TRW type 35, with an ESR of 12 milliohms each. The inductor is made with a Ferroxcube IF30-3C8 core, wound with 4 turns of 5 #12 AWG wires in parallel.

Current limiting is done with current transformer T_3

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in the return lead of the transformer primary. The signal is rectified, threshold sensed and adjusted, and is fed to the shutdown terminal pin 10 of the UC3525A control chip.

Performance

A curve of efficiency versus power output is shown in Figure 8. Note that the efficiency decreases for increasing power output. This is primarily due to resistive losses, other than the Schottky rectifier losses, such as the $R_{DS\ (on)}$ losses of the MOSFETs and the copper losses of the output transformer and filter inductor. The switching losses of the MOSFETs are low; the measured current rise and fall times were 10ns and 20ns, respectively.

When compared to a 25kHz switcher, the transient response of this circuit can be improved by a factor over 8 times since the LC output filter resonant frequency can be increased by this amount. There is an additional improvement factor, since polypropylene capacitors rather than electrolytic are used for 200kHz operation. The value of capacitance can be reduced considerably, because of the improved ESR. However, in order to realize the improved frequency response, careful attention to control circuit layout and shielding is important to minimize parasitic capacitance and inductance. The use of a ground plane is a necessity.

A dramatic reduction of the size of several major components is evident when comparing this 200kHz, 500W switcher to a 25kHz switcher. The power transformer, output filter inductor, and output filter capacitor are about half the volume, and the drive circuits for the MOSFETs are considerably smaller than the drive circuits for bipolars at 25kHz. The auxilliary power supply is half the size. The parts count is less, primarily due to the reduced parts count of the drive circuits.

Design Considerations

The choice of operating frequency and the decision to use MOSFETs or bipolars depends upon a number of factors, including the required power output level, size, weight, cost, etc., and a rapidly changing technology which includes circuit topology, new components, control chips and high frequency techniques.

There are some major advantages that are obtainable by using MOSFETs in place of bipolars, other than those associated with higher operating frequency. One of these is in the area of potential gate drive circuits. In the power supply described in this application note, the power MOSFET gates are driven directly by the control chip through a small step down isolation transformer.

The feedback loop compensation is comprised of an RC network at the error amplifier of the UC3525A. The resonant frequency of the LC output filter is approximately 40kHz. Closing the loop at 0_{dB} at 100kHz, this network adds two zeros (phase lead) at approximately one half the LC resonant frequency, and gives a 40° phase margin up to 100kHz.

Do's and Don'ts of High Frequency Switchers

For the control chip circuit, the use of a ground plane construction is recommended. A double sided PC board, with one side used for the ground plane, is preferable. If a single sided board is used, use as much copper area as possible for the ground plane. Keep traces fairly wide to reduce inductance. The judicious use of a few wire jumps to reduce trace length is helpful.

Power MOSFET gate drive circuits do not have to supply a continuous large current drive. MOSFET gates do require fairly large, fast current pulses to change the gate voltage rapidly because of the composite gate capacitance, including the Miller effect capacitance. This means that the gate drive circuit and transformer should be designed to minimize lead inductance by reducing loop areas to a minimum. Remember that each inch of wire adds about 20 nanohenries of inductance. Using fairly large diameter wires twisted together helps, as well as designing the layout to reduce lead lengths to a minimum.

The use of copper strapping in place of round wire is also helpful in reducing inductance. Use two closely spaced parallel strips if possible. Circuit by-passing with small high frequency capacitors is important, especially around the control chip circuit area. By-passing the fairly large electrolytic input energy storage capacitors is helpful, if the by-pass capacitors are located physically at the junction of the MOSFETs and the primary of the output transformer, as shown on the schematic.

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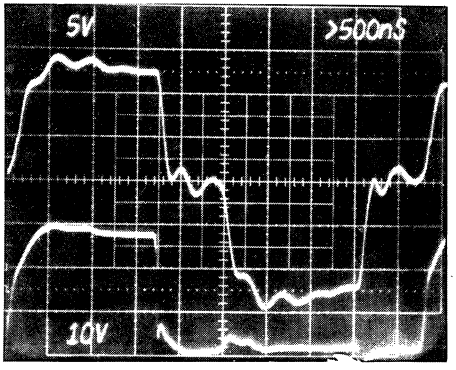
2. Raoji Patel, "Power Schottky Rectifiers in a Switching Regulator", Unitrode Application Note U-85.

Continued

3. Raoji Patel, "Operating Buck Regulator Above 100kHz", Unitrode Application Note U-80.

4. Raoji Patel, "Design Considerations for Power MOSFET Gate Drive Circuitry," Unitrode Switching Power Supply Design Seminar Manual, Spring 1982.

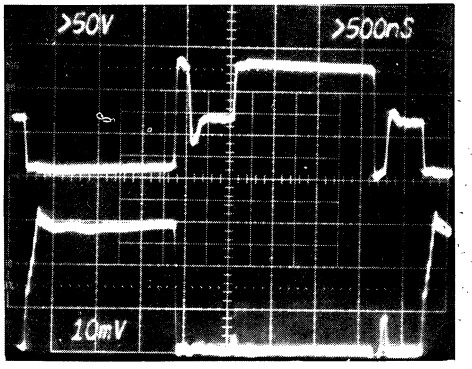
WAVEFORMS AT I_O = 100A



500ns/DIV

UPPER — V_{GS} OF Q_2
LOWER — V_{OUT} OF PIN 14, UC3525A

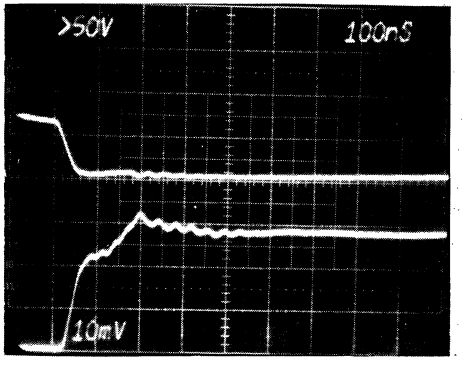
FIGURE 1. GATE DRIVE



500ns/DIV

UPPER — V_{DS} OF Q_2
LOWER — I_D OF Q_2

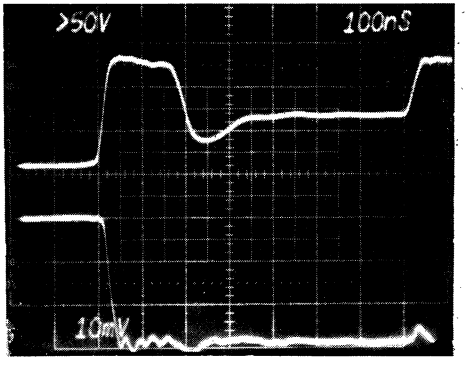
FIGURE 2. MOSFET SWITCHING



100ns/DIV

UPPER — V_{DS} OF Q_2
LOWER — I_D OF Q_2

FIGURE 3. RISE TIME



100ns/DIV

UPPER — V_{DS} OF Q_2
LOWER — I_D OF Q_2

FIGURE 4. FALL TIME

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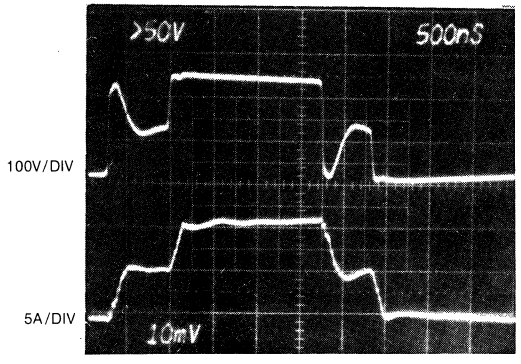
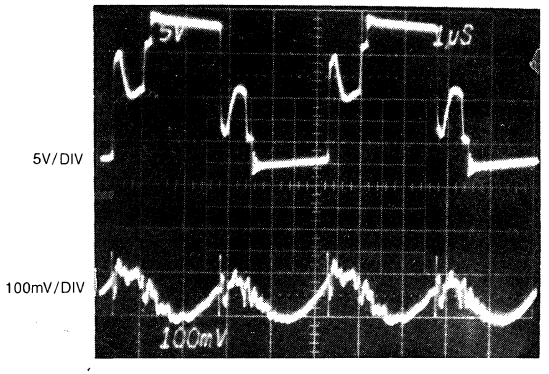


500ns/DIV

UPPER — $V_{PRIMARY}$
LOWER — $I_{PRIMARY}$

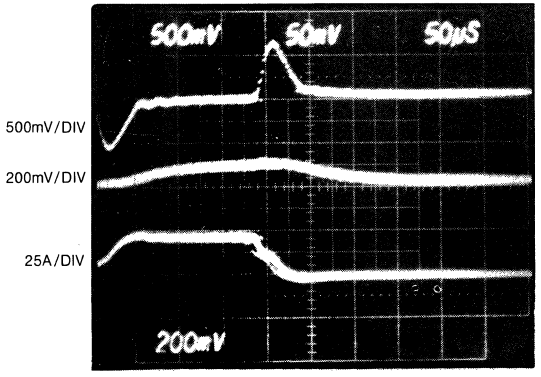
FIGURE 5. TRANSFORMER PRIMARY WAVEFORMS



1μs/DIV

UPPER — XFMR SEC VOLTAGE
LOWER — OUTPUT RIPPLE

FIGURE 6. TRANSFORMER SECONDARY VOLTAGE, AND OUTPUT RIPPLE



50μs/DIV

UPPER — 5V OUTPUT
MIDDLE — ERROR AMPLIFIER OUTPUT
LOWER — LOAD CURRENT

FIGURE 7. TRANSIENT RESPONSE, 25A LOAD CHANGE (LARGE SIGNAL CHANGE)

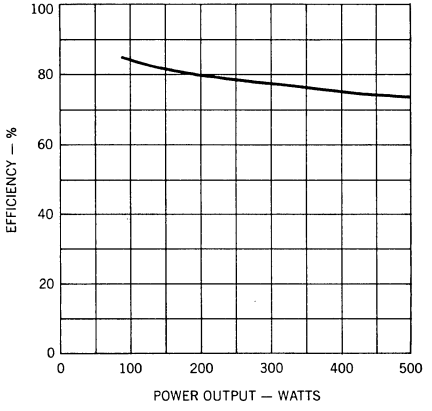


FIGURE 8. EFFICIENCY VS POWER OUTPUT

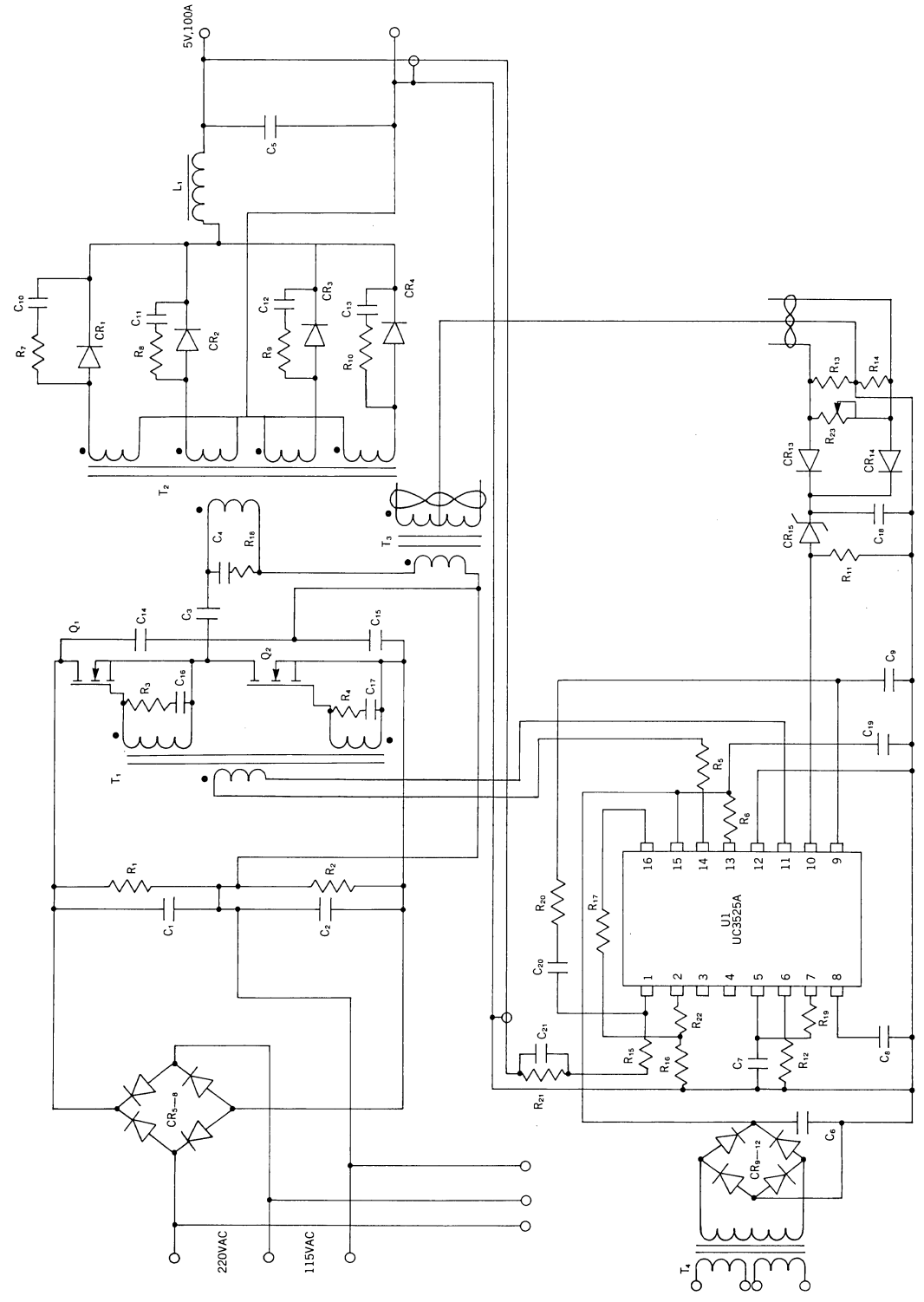


FIGURE 9. SCHEMATIC OF 500W, 200kHz HALF-BRIDGE POWER SUPPLY

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Parts List

U_1	UC3525A
Q_1, Q_2	UFN441
CR_1-CR_4	USD545
CR_5-CR_8	680-4 (Unitrode)
CR_9-CR_{12}	673-1 (Unitrode)
CR_{13}, CR_{14}	UES1003
CR_{15}	TVS310
C_1, C_2	600μF, 250V
C_3	1μF, 400V
C_4	500pF, 1kV
C_5	3x5μF, 100V (polypropy.)
C_6	500μF, 50V
C_7	1000pF, 50V
C_8	1μF, 50V
C_9	50pF, 50V
C_{10}-C_{13}	0.02μF, 50V
C_{14}, C_{15}	1μF, 200V
C_{16}, C_{17}	.002, μF, 50V
C_{18}	0.2, μF, 50V
C_{19}	0.1, μF, 50V
C_{20}	300pF, 50V
C_{21}	220pF, 50V
R_1, R_2	33K, 2W
R_3, R_4	47Ω
R_5	10Ω, ½W
R_6	4.7Ω
R_7-R_{10}	3.9Ω, 1/2W
R_{11}	10K
R_{12}	3.3K
R_{13}, R_{14}	220Ω
R_{15}	10K
R_{16}	10K
R_{17}	51Ω
R_{18}	50Ω, 4W
R_{19}	10Ω
R_{20}	27K
R_{21}	24K
R_{22}	33K
R_{23}	2K

T_1	Core, Ferrox 846T250-3C8 Pri, 14T #22AWG Sec (2) 7T #22AWG
T_2	Core, Ferrox EC52-3C8 Pri, 14T, 2 layers, 2 #16 AWG in parallel. Sec, (2), each 2T, C.T., copper strap 0.01″ x 0.8″ see text.
T_3	Core, Ferrox 846T250-3C8 Pri, 1T Sec, 20 turns CT #22AWG
T_4	220/117V, 25V, 0.15A
L_1	Core, Ferrox IF30-3C8, 4 turns, 5 #12AWG in parallel.

DESIGN CONSIDERATIONS FOR POWER MOSFET GATE DRIVE CIRCUITRY

1. Introduction

The power MOSFET promises exciting performance advantages over the more conventional bipolar transistor. However, much attention must be given to gate drive techniques to take full advantage of MOSFET characteristics. This application note develops simple, high performance gate drive circuits.

This application note also provides design engineers with a basic understanding of the relationship between parasitic elements and switching times. In addition, a circuit is developed which controls the switching time of the power MOSFET to reduce rectifier reverse recovery spikes; thus, reducing RFI and switching loss.

2. Features

The power MOSFET is becoming more and more popular in many applications due to its inherent features, such as:

2.a. Extremely Fast Switching Characteristics.

A power MOSFET is capable of switching rapidly because it is a majority carrier device. The speed at which it can switch depends upon the rate at which gate charge is supplied or removed by the gate driving source. In a practical application the MOSFET can be made to switch in less than 10 nanoseconds. This feature allows operation at higher frequencies than with bipolar devices, resulting in improved electrical performance (transient response), reduced size and cost of the magnetic components, and decreased weight of the overall system.

Other advantages derived from fast switching times are:

- The losses in the snubber circuit, if employed, are minimized.
- Switching times are independent of load and temperature variation. The variation in the frequency spectrum of conducted RFI is minimized.
- The cross-conduction problem in a switched-mode converter (half bridge, full bridge, push-pull) is reduced because power MOSFETs have no storage time.
- The problem of core saturation due to assymmetrical volt-seconds in circuits using a transformer is minimized because the major cause of this effect, differences in storage time is negligible for MOSFETs.
- If a voltage feed-forward control is being used, the nonlinearity introduced by the storage time of the switching device is eliminated, thus reducing the gain requirement of the error amplifier.

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2.b. High Gate Input Impedance.

The gate input impedance is a high resistance shunted by a capacitance. At high frequencies the capacitance completely dominates. This fact allows the design of a simple and efficient gate drive circuit.

2.c. No Forward or Reverse Biased Second Breakdown.

Because of the positive temperature co-efficient of channel resistance, power MOSFETs do not have forward or reverse biased second breakdown characteristics like bipolar devices. Thus power MOSFETs improve the overall reliability of systems. Snubber networks for turn-off load line shaping may be smaller and often eliminated. This reduces circuit complexity and cost. The voltage spikes due to stray inductance can be limited by simply controlling the switching times in many applications.

2.d. Integral Diode.

There is a built-in diode across the source to drain. The reverse recovery time of the diode depends upon the drain to source breakdown voltage. Low voltage (100V) devices have reverse recovery times as low as 200 nanoseconds, while high voltage devices (400-500V) have recovery times of about 600-700 nanoseconds. When a high speed diode is not required, the internal diode can be used effectively for free wheeling voltage damping. However, long recovery times might hinder the performance of the circuit in some applications, so this effect must be considered.

2.e. Current Sharing Capability

Since the channel resistance of a power MOSFET has a positive temperature co-efficient many devices can be paralleled with much less special design attention than with bipolar transistors. The power output capability can, thus, be extended.

The Undesirable Features of the Power MOSFET are:

2.f. Temperature Dependence of Saturation Resistance.

The saturation resistance ($R_{DS(on)}$) increases with temperature. It doubles approximately every 110°C. Thus, power dissipation will increase as the junction temperature increases. Consideration of the thermal stability of the system is required if a major part of the power losses occur in the on-state mode.

(In a bipolar transistor "off line" converter, most of the power losses are due to switching. The switching losses increase with temperature, usually doubling every 100°C. In this respect, power MOSFETs will be more thermally stable than bipolar transistors, as switching the times of a power MOSFET do not change with temperature.)

2.g. Silicon Chip Area.

The silicon chip area of a power MOSFET is about 50% larger than an equivalent bipolar transistor. This has some impact on the cost of the device.

3. Construction

The cross section of an N-channel vertical DMOS (double-diffused MOS) is shown in Figure 3.1. Sections of this structure affecting gate drive are discussed in the following sections.

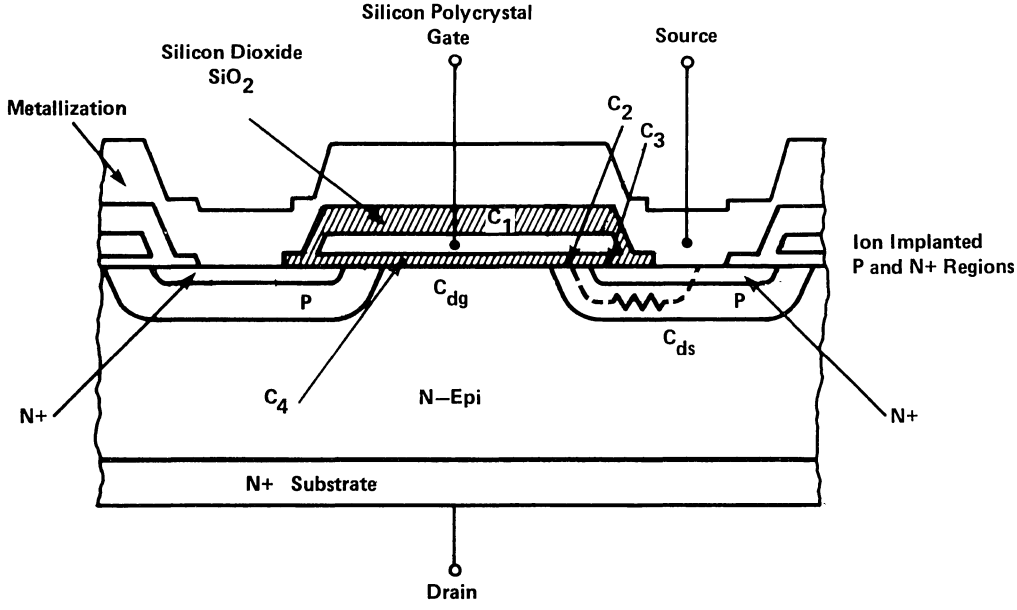


Figure 3.1 The Power MOSFET Physical Structure

4. Parasitic Elements and Switching

Since MOSFETs are majority carrier devices, they are theoretically capable of switching in picoseconds. In practical devices, however, parasitic elements adversely affect switching capability. MOSFET parasitic capacitances are shown in Figure 4.1.

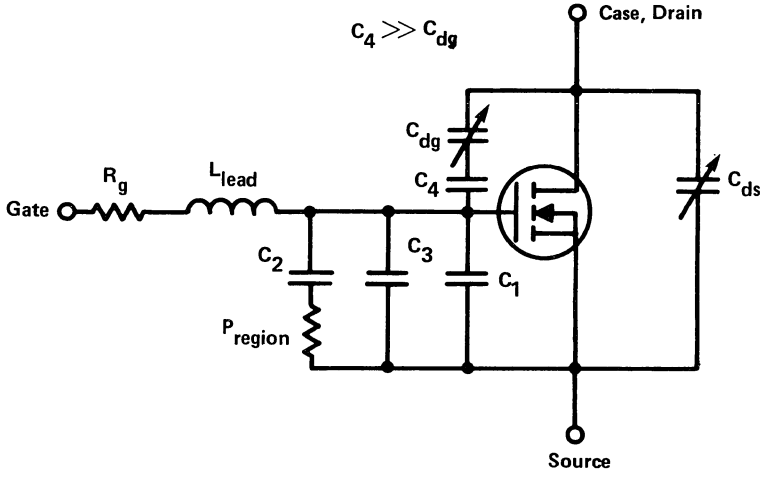


Figure 4.1 Power MOSFET Parasitic Capacitance

The thickness and area of SiO_2 dielectric material between gate and source determines the value of the gate capacitance. In the off-state, the total gate-to-source capacitance is composed of a) capacitance C_3 between the gate and the heavily doped N+ source region, b) capacitance C_2 between the gate and the moderately doped P region and c) capacitance C_1 between the gate and the source metallization on the top of the gate (C_1 is much less than capacitances C_3 and C_2 and can be neglected). The gate capacitance is practically independent of gate voltage, as shown in Figure 4.2.

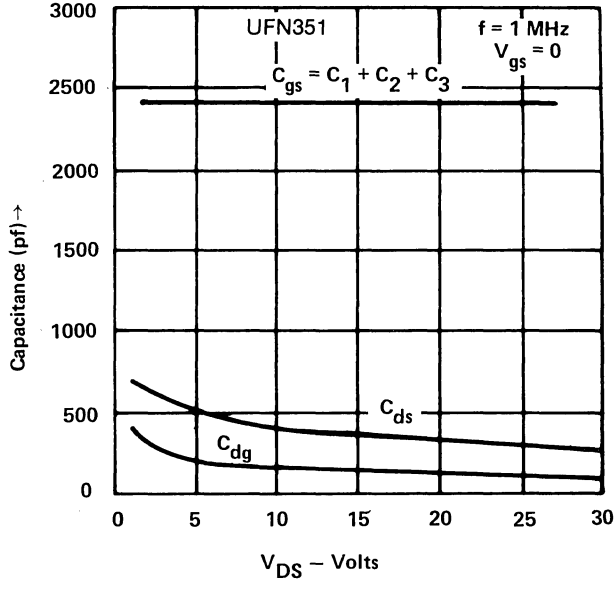


Figure 4.2 Capacitance Vs. Drain to Source Voltage

The Miller effect capacitance between drain and gate consists of a series combination of a space charge capacitance C_{dg} due to a depletion layer in the N-region and the dielectric capacitance C_4 between the N-region and the gate, as shown in Figure 3.1. The capacitance C_{dg} is a function of drain voltage (as shown in Figure 4.2), while dielectric capacitance C_4 is independent of the voltage. These drain capacitances effectively increase the input gate capacitance during switching transitions.

The capacitance C_{ds} between drain and source is a depletion capacitance and does not have a major effect on the switching behaviour of the device. It can be neglected in the switching analysis.

The turn-on and turn-off characteristics of a power MOSFET are shown in Figure 4.3.

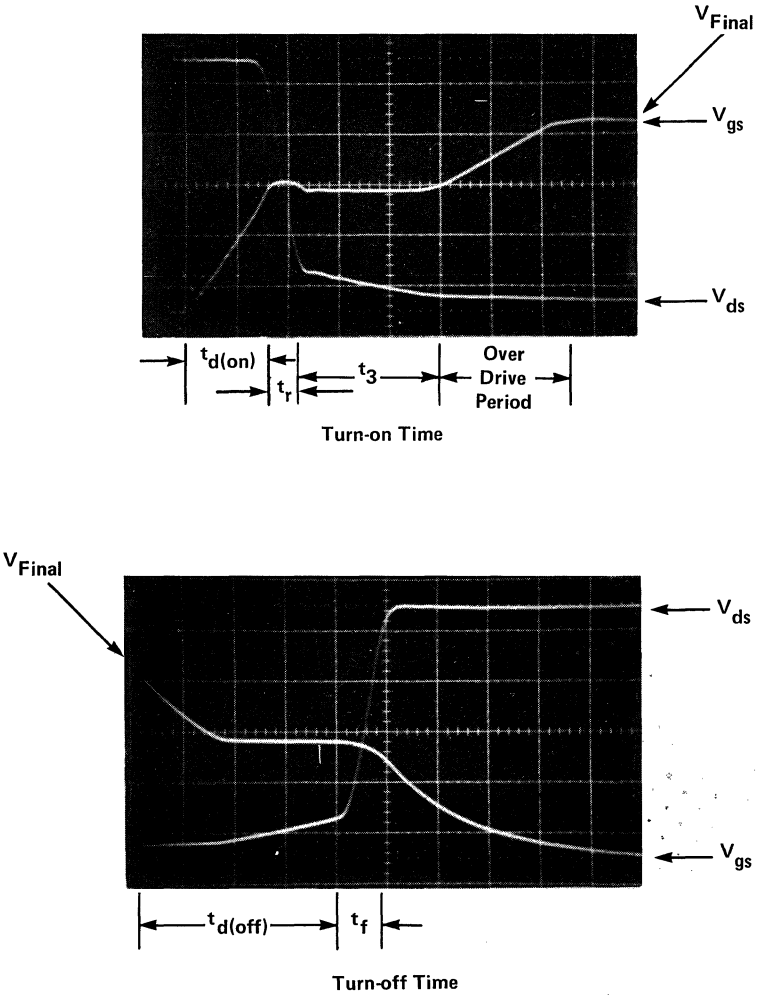


Figure 4.3 Power MOSFET Switching Waveforms

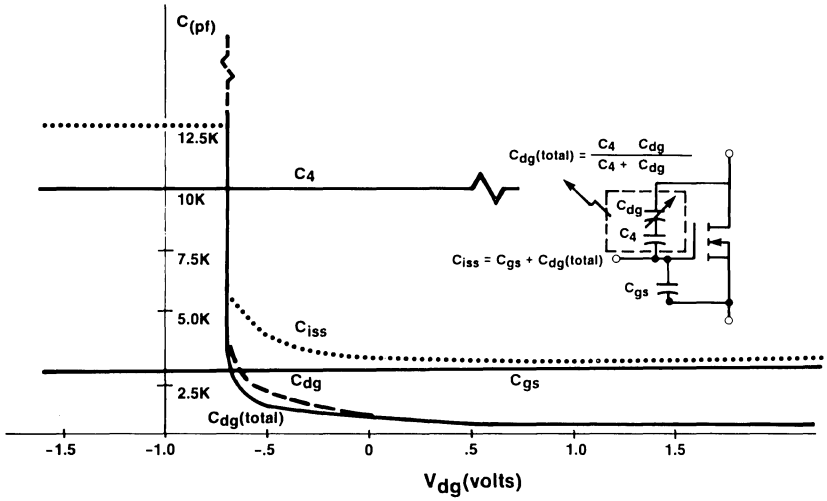


Figure 4.4A C vs V_{dg} - Static Case Expanded

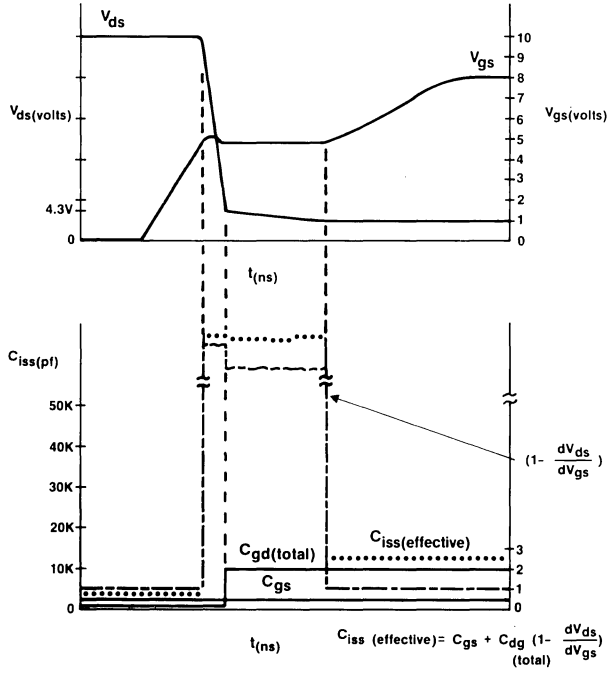


Figure 4.4B C vs t - Dynamic Case

Figure 4.4 Input Capacitance and Conditions at Turn-on

4.a. Turn-on Delay Time – $t_{d(on)}$

The effective gate input capacitance during this period is a parallel combination of capacitor C_1, C_2 and C_3. While the gate voltage builds up toward the gate threshold voltage, the drain voltage remains the same.

4.b. Rise Time – t_r

When the drain voltage starts to drop, during current rise time the effective gate capacitance increases significantly due to the Miller effect capacitance (C_{dg}), which absorbs nearly all the gate drive current. The rise time of the drain current is inversely proportional to the gate drive current supplied, and transition rise time can be controlled accurately by controlling the gate current, a feature particularly useful to reduce current overshoot due to rectifier reverse recovery. Since the magnitude of the gate and drain capacitances are determined by the structure of the device, they are very consistent from device to device and are temperature independent. This allows optimization of snubber network designs.

4.c. Dynamic Saturation – t_3

During this period, which follows the rise time, the drain voltage drops below the gate voltage. An inversion layer is established underneath the entire gate in the N- drain region. The gate capacitance is equal to the dielectric capacitance and is independent of voltage bias. At this point, the total drain to gate capacitance changes abruptly to a very high value. This can be seen in the gate voltage waveform of Figure 4.3 where effective gate capacitance is in the order of 50,000 pf and no further increase in gate voltage is noticed.

4.d. Overdrive Period

The input gate capacitance is approximately twice the value expected from Figure 4.2 during over-drive conditions, as can be seen by comparing the slopes of the gate voltage during the period $t_{d(on)}$ and overdrive (see Figure 4.3). This is because C_{gs} is measured with a greater voltage across the drain to source terminals than is present during this period.

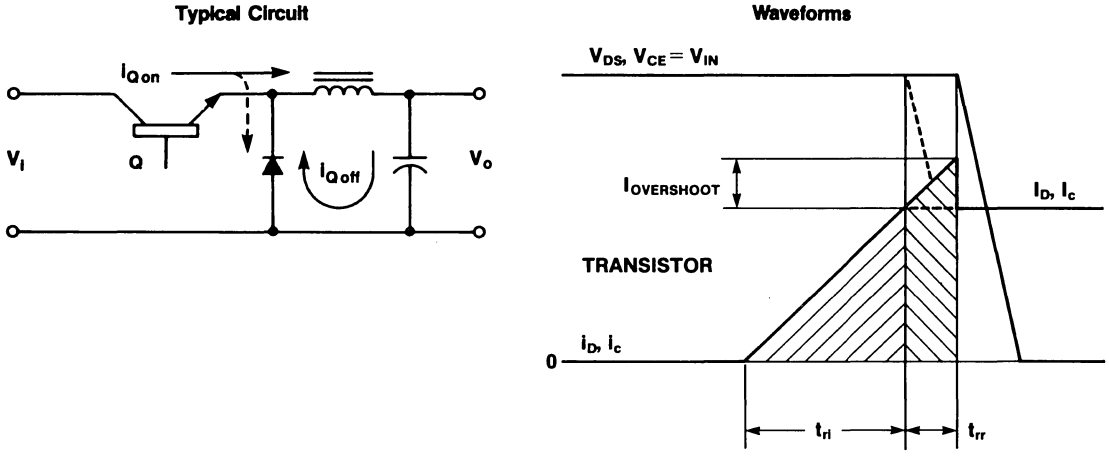
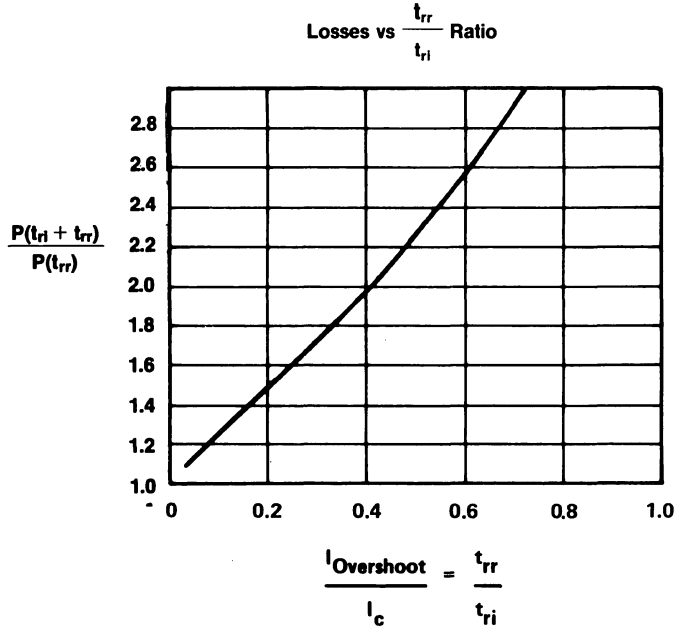


Figure 5.1A Transistor Current During Turn-On



Example: V_{CE} = 100V, I_c = 6A, t_{ri} = 100nS

t_{rr} (ns)	I_{PK} (A)	P_{AV} (W/Cycle)	E (μJ)
0	6	300	30
30	7.8	390	51
50	9	450	68
100	12	600	12

Figure 5.1B Effect of Reverse Recovery on Losses

Figure 5.1 Importance of Current Rise Time in a Transistor and Reverse Recovery in a Rectifier

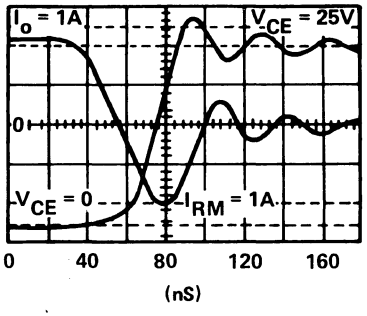


Figure 5.2A Schottky Rectifier (SD41)

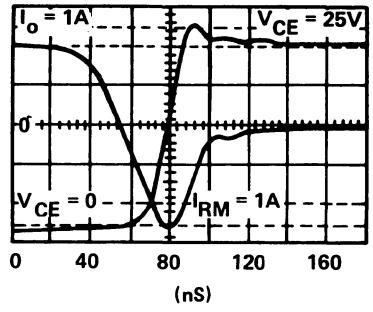


Figure 5.2B Ultra-fast PN Junction (UES701)

Figure 5.2 Reverse Recovery of Fast Rectifiers

5. Drive Circuit Considerations

The power MOSFET is a charge driven device, and the switching times can be controlled by the external circuit rather than by the device itself. In a buck switching regulator application (or similarly behaving circuit), the rise time of a power MOSFET may be controlled to prevent excessive current spikes and power dissipation due to rectifier reverse recovery. Current spikes also produce unwanted ringing and RFI in the circuit. The relationship between reverse recovery time, current rise time and power dissipation in the power MOSFET is shown in Figure 5.1. The fastest available power PN junction rectifiers have recovery times on the order of 20 ns. To minimize the recovery current spikes, the current rise time of the power MOSFET should be made at least 3 times slower than the reverse recovery of the rectifier. Even though Schottky rectifiers are majority carrier devices, they have about the same effective reverse recovery time as very fast PN junction diodes due to high junction capacitance, as shown in Figure 5.2. In transformer coupled switching regulators, leakage inductance will reduce the large current spikes to some extent depending upon the transformer design.

During turn-off time, voltage spikes will occur as a result of energy stored in the stray inductance of the drain circuit during the preceding on-time. The magnitude of these spikes directly depends upon the speed with which the device is turned off and upon lead inductance in the drain circuit. A snubber network in the drain may be required to limit these voltage spikes. The turn-off power dissipation can be optimized with a fast turn-off time along with the use of a snubber circuit.

The drive circuit described in this section allows control of the rise time in a power MOSFET during turn-on while providing fast turn-off.

5.a. Low Cost Gate Drive Circuit

A low cost power MOSFET gate drive circuit with isolation for off-line applications is shown in Figure 5.3. The circuit provides a controlled rate of increasing drain current to minimize spikes due to the reverse recovery of the output rectifier. The rise time of the power MOSFET is controlled by supplying a linearly increasing gate voltage. The relatively large capacitor C_1 (as compared with C_{gs}) is placed in parallel with the gate and source to minimize the effect of variations of C_{dg} on the switching characteristic of the device. C_1 also prevents spurious oscillations due to high frequency voltage feedback from C_{dg}. C_1 is charged with a constant current from the drive circuit, providing linearly increasing voltage at the gate of power MOSFET, Q_2. The rise time of the MOSFET depends on the rate at which capacitor C_1 charges. The drive circuit described provides a rise time of around 70 ns and current fall time of about 40 ns.

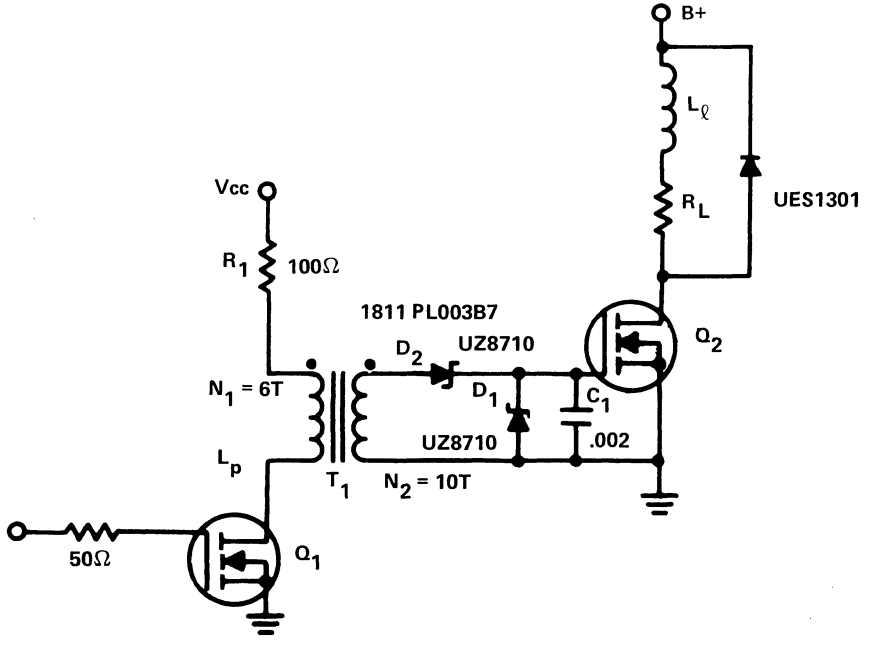


Figure 5.3 Low Cost Gate Drive Circuit with Isolation

The operation of the circuit can be described as follows: When drive transistor Q_1 turns on, the current transformer provides constant drive current into the secondary circuit. The constant drive current is determined by resistor R_1 and will charge capacitor C_1 linearly through diode D_2. Zener diode D_1 limits Q_2 gate to source voltage. When the voltage across the secondary winding drops due to primary time constant Lp/R1, the zener diode D_2 becomes reverse biased and prevents the discharge of capacitor C_1. While transistor Q_1 is on, the energy will be stored in the transformer core. When transistor Q_1 subsequently turns off, current will flow in the secondary side due to energy stored in the core of transformer T_1. The amount of energy stored must be greater than that stored in the capacitor C_1 in order to ensure complete discharge of the capacitor.

Capacitor C_1 discharges through zener diode D_2. Diode D_1 prevents any negative voltage swing across gate to source and provides a current path for discharge of the secondary inductance.

The circuit shown in Figure 5.4 improves the fall time compared to the previous circuit. The operation of the circuit is the same as that described above except during turn off. During Q_1 turn-off, capacitor C_1 discharges through winding N_3 and diode D_2. The discharge current will be 4 times greater than in the previous circuit because the current now flows through only one quarter of the winding, while the ampere-turns remain unchanged. Diode D_1 prevents current flow from the winding N_2 during turn off.

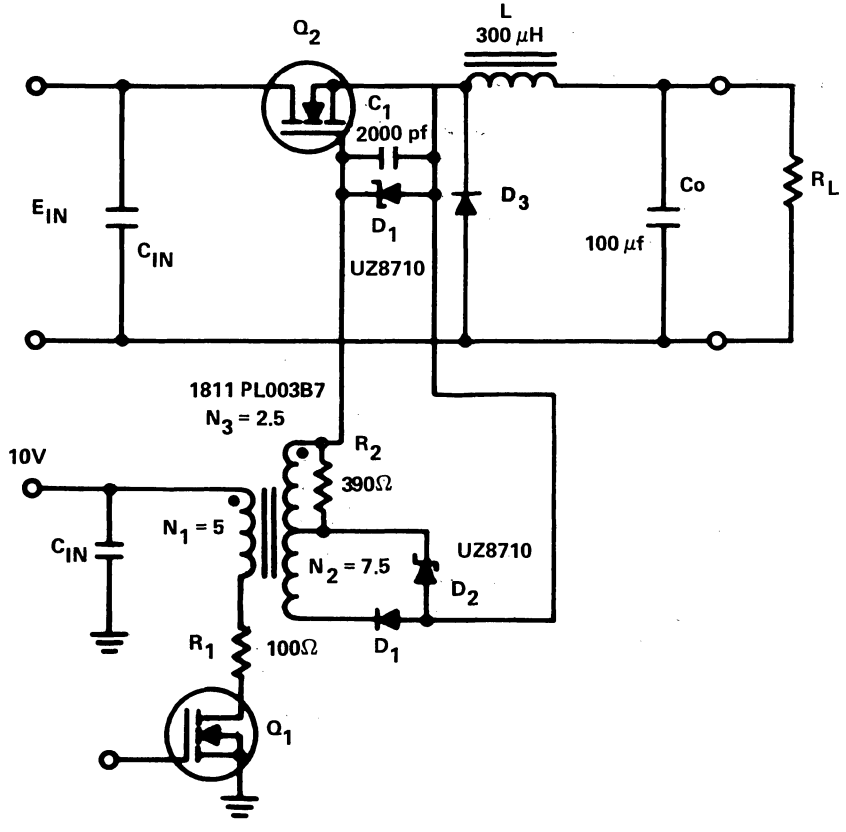


Figure 5.4 Fall Time Enhancement Drive Circuit

5.b. Pulse Drive Circuit

In some applications, as in a line driver, it is essential that power MOSFETs switch rapidly both during turn-on and turn-off. The drive circuit shown in Figure 5.5 provides these fast switching times while conserving drive power from the low voltage supply. The circuit is capable of switching a device with a high (2500 pf) gate input capacitance in 12 to 15 nanoseconds. During off time, low impedance is maintained across gate to source. This prevents turn-on of the power MOSFET due to dv/dt or noise at the drain terminal. The drive circuit can be operated from 1KHz to 100 KHZ without any changes. For low cost, it utilizes an inexpensive ferrite bead as a current transformer.

The drive circuit operates from a 25V power supply. The transformer is driven by a Unitrode UC1524A pulse width modulator control chip. With Q_3 off when the output transistor of the UC1524A turns on, the voltage V_{C1} is impressed across the primary of current transformer T_1. The energy stored in the capacitor C_1 is, thereby, transferred to the T_1 secondary. Secondary current flows through capacitor C_2, winding N_2, diode D_3, diode D_4, small signal MOSFET Q_2 and back to capacitor C_2. The secondary current discharges the initially charged capacitor C_2. MOSFET Q_2 turns off when the voltage across C_2 drops below the gate threshold voltage of Q_2. The negative voltage across the gate to source of Q_2 is clamped to a safe value by diode D_1. Now the secondary current starts to flow into the input gate capacitance of the output power MOSFET Q_3. When the gate voltage reaches the gate threshold voltage, Q_3 will begin to turn on. The gate voltage will continue to rise until the current transformer saturates and the current in the secondary ceases. The voltage across winding N_2 drops to zero. Charge stored in the gate capacitance of Q_3 is maintained because diode D_4 is back biased by the resulting gate voltage. The rate at which the gate capacitance discharges depends upon the leakage current of D_4 and the I_{DSS} of Q_2.

For 1.0 μA total leakage current, it will require about 25 milliseconds to discharge a device with a 2500 pf input capacitance.

When the output transistor of the UC1524A turns off, the magnetizing energy stored in the current transformer is transferred by current flow to the secondary circuit. The current will flow in the loop which consists of diode D_2, winding N_2, and capacitance C_2 in parallel with the input capacitance of Q_2. When the voltage on the gate reaches the threshold voltage, Q_2 turns on and discharges the gate capacitance of Q_3 with a low impedance, resulting in fast turn-off.

Capacitor C_2 remains charged because it has no discharge path. This keeps Q_2 on and Q_3 is held off. This prevents turn-on of Q_3 due to any dv/dt present at the drain terminal of Q_3, which is particularly useful in PWM half-bridge switching regulator circuits.

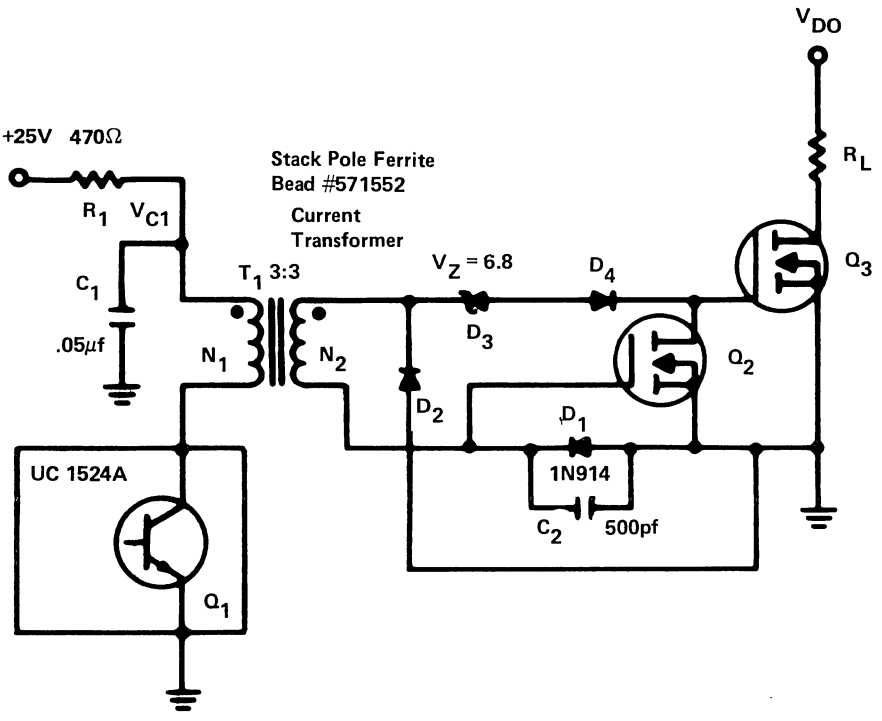
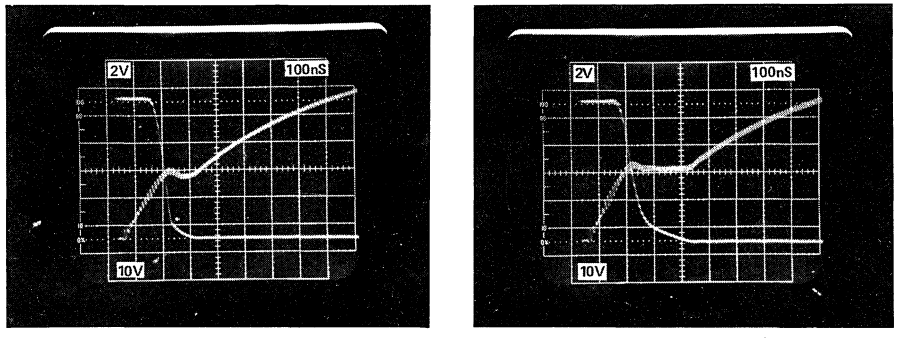


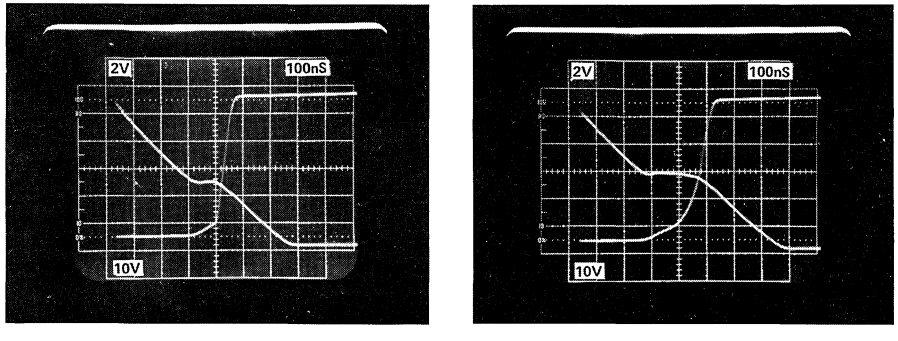
Figure 5.5 Pulse Drive Circuit

The power drawn from the drive circuit power supply is minimized by using this current pulse drive circuit, especially when operating at a low frequency for fast switching applications.

The switching times of a Unitrode power MOSFET are compared with those of a competitive device in Figure 5.6. The circuit described above was used. The devices have the same voltage and current ratings and comparable $R_{DS(on)}$. The Unitrode UFN351 switches faster, due to its 20 percent lower gate-to-drain and gate-to-source capacitances, than the competitive device.



Unitrode UFN351 — Turn-on Time — Competitive Device



Unitrode UFN351 — Turn-off Time — Competitive Device

Figure 5.6 Switching Times of Unitrode UFN44C1 Power MOSFET vs Competitive Device with Same Voltage and Current Ratings

Conclusion

The use of power MOSFETs in switching regulated power supplies is advantageous due to their fast switching capability with simple drive circuits. The overall system cost can be further reduced by operating these power MOSFETs at a high frequency. The reliability of the switching power supply is improved due to lack of forward or reverse bias second breakdown in the device and due to reduced parts count.

A SECOND-GENERATION IC SWITCH MODE CONTROLLER OPTIMIZED FOR HIGH FREQUENCY POWER MOSFET DRIVE

Introduction

Since the introduction of the SG1524 in 1976, integrated circuit controllers have played an important role in the rapid development and exploitation of high-efficiency switching power supply technology. The 1524 soon became an industry standard and was widely second-sourced (it is available from Unitrode as the UC1524). Although this device, as well as the MC3420 and TL494 which followed it, contained all the basic control elements required for switching regulator design; practical power supplies still required other functions which had to be implemented with additional external discrete circuitry.

An additional development within the semiconductor industry was the introduction of practical power FETs which offered the potential of higher efficiencies at higher speeds with resultant lower overall system costs. In order to be able to take full advantage of the speed capabilities of power FETs, it was necessary to provide high peak currents to the gate during turn-on and turn-off to quickly charge and discharge the gate capacitances of 800 to 2000pF present in higher current units.

The development of a second-generation regulating PWM IC, the UC1525A, and its complimentary output version, the UC1527A, was a direct result of the desire to add more power supply elements to the control IC, as well as to optimize the interfacing of high current power devices.

Integrating More Power Supply Functions

Having achieved the greatest level of acceptance among users of first generation control chips, the 1524 became the starting point for expanding IC controller capabilities. This early device, shown in *Figure 1*, contains a fixed-voltage reference source, an oscillator which generates both a clock signal and a linear ramp

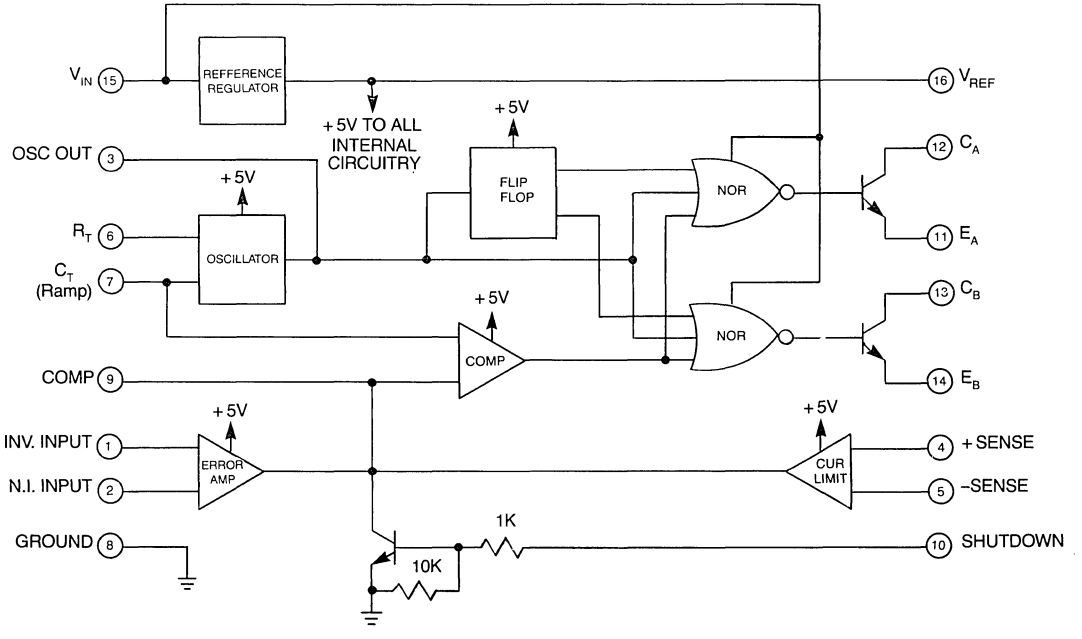


Figure 1. The UC1524 Regulating PWM Block Diagram. This design was the first complete IC control chip for switch mode power supplies.

waveform, a PWM comparator, and a toggle flip-flop with output gating to switch the PWM signal alternately between the two outputs.

With this circuitry already defined, a two pronged development effort was initiated: 1) to add additional features required by most power supply designs and 2) to improve the utility of features already included within the 1524. The resultant block diagram for the UC1525A is shown in *Figure 2.* Two general comments should be made relative to the overall block diagram. First, in optimizing the output stage for bi-directional, low impedance switching, commitments had to be made as to whether the output should be high or low during the active, or ON state. Since this is application defined there are needs for both output states, so both were developed with the UC1525A device defined by an output configuration which is high during the ON pulse, and the UC 1527A configured to remain high during the OFF state. This difference is implemented by a mask option which eliminates inverter Q_4 (see Figure 3) for the UC1527A. In all other respects, the 1525A and 1527A are identical and any description of the 1525A characteristics apply equally to the 1527A. Second, a major difference between this new controller and the earlier 1524 is the deletion of the current limit amplifier. There are so many system considerations in providing current control that it is preferable to leave this as a user-defined external option and allocate the package pins to other, more universally requested functions. Current limiting possibilities are discussed further under shutdown options.

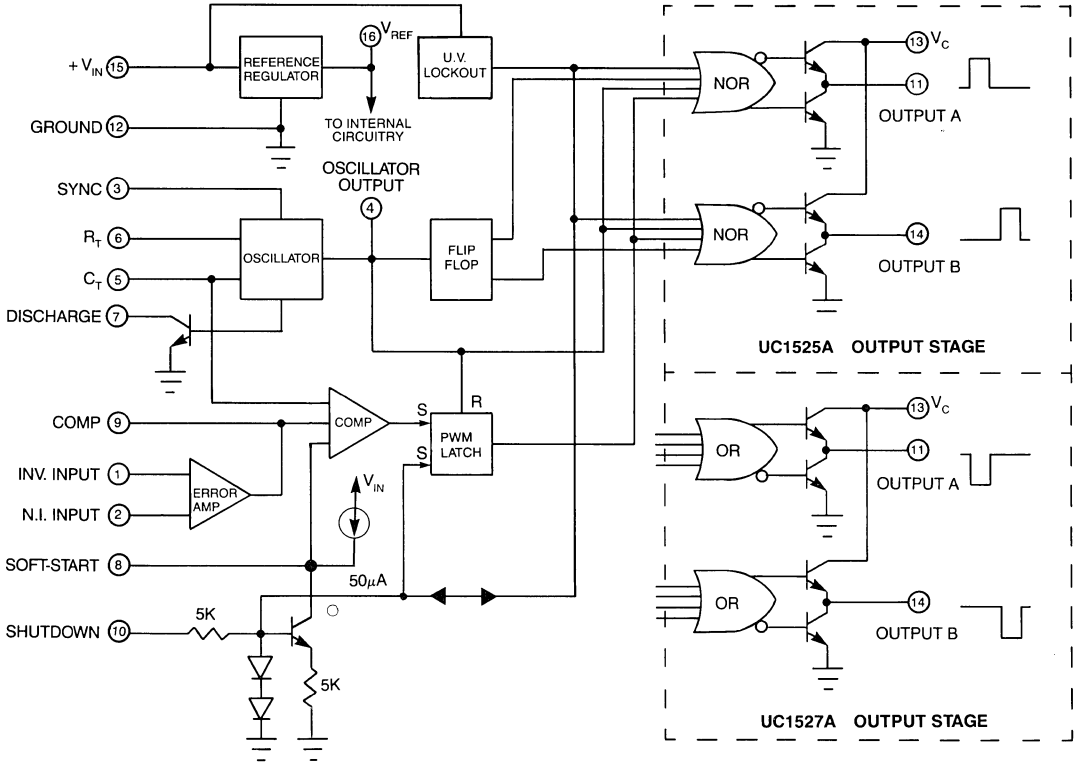


Figure 2. The UC1525A family represents a "second generation" of IC controllers.

"Totem-Pole" Output Stage

One of the most significant benefits in using the UC1525A is its output configuration. For the first time it has been recognized in an IC controller that it is more difficult to turn a power switch off than turn it on. With the UC1525A, a high-current, fast transition, low impedance drive is provided for both turn-on and turn-off of an external power transistor or FET. The circuit schematic of one of the two output stages contained within the device is shown in *Figure 3.* This is a two-state output, either Q_8 is on, forming a low saturation voltage pull-down, or Q_7 is on, pulling the output up to V_C. Note that V_C is a separate terminal from the V_{IN} supply to the rest of the device. This offers the benefits of potentially operating the output drive from a lower supply than the rest of the circuit for power efficiencies, decoupling of drive transients from more sensitive circuits, and a third terminal for extracting a drive signal. Note that even though V_C can be set either higher or lower than V_{IN}, the output cannot rise higher than approximately 1½ volts below V_{IN}.

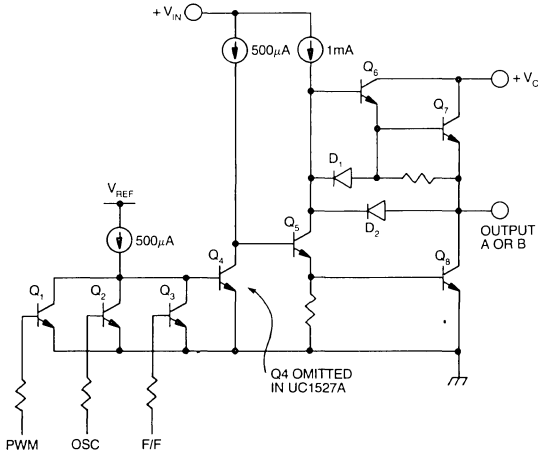


Figure 3. One of two power output stages contained within the UC1525A which conduct alternately due to the internal flip-flop.

During the transition between states, there is a slight conduction overlap between source and sink which results in a pulse of current flowing from V_C to ground. However, due to the high-speed design configuration of this stage, this current spike lasts for only about 100ns. A typical current waveform at V_C is shown in *Figure 4.* This transient will normally be decoupled from the rest of the control power by a 0.1mfd capacitor from V_C to ground but it should not, otherwise, cause a problem unless very high frequency operation is contemplated where it will contribute to overall device power dissipation, by becoming a significant portion of the total duty cycle.

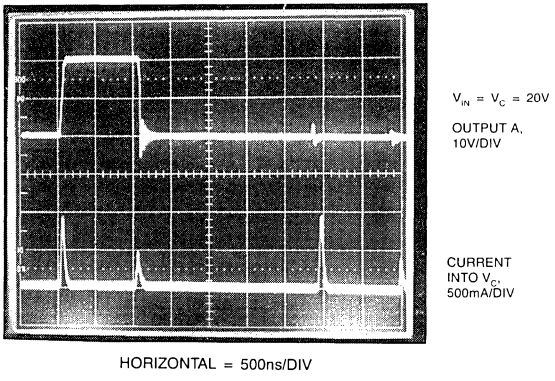


Figure 4. Current "spiking" on the V_C terminal caused by conduction overlap between source and sink is minimized by high-speed design techniques.

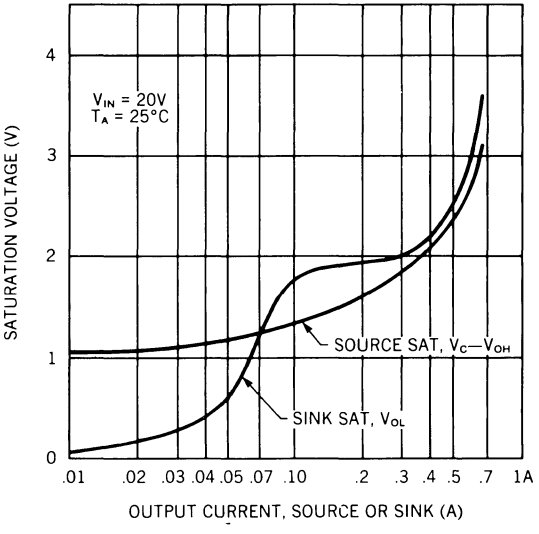


Figure 5. The ouput saturation characteristics of the UC1525A provide both high drive current and low hold-off voltage.

The output saturation characteristics of this stage are shown in *Figure 5.* The source transistor, Q_7, is a straight forward Darlington and its saturation voltage remains between 1 and 2V out to 400mA under the assumption that $V_{IN} \geq V_{CC}$. The sink transistor, Q_8, however, has a non-uniform characteristic which needs explanation. At low sink currents, the 1mA current source through Q_5 insures a very low saturation voltage at the output. As load current increases past 50mA, Q_8 begins to come out of saturation for lack of base drive but only up to about 2V. Here diode D_2 becomes forward biased shunting a portion of the load current through Q_5 to boost the base current into Q_8. With this circuit, the sink transistor can both support high peak discharge currents from a capacitive load, as well as insure the low static hold-off voltage required for bipolar transistors.

A typical output configuration for a push-pull, bipolar transistor power stage is shown in *Figure 6.* With a steady state base drive current from the UC1525A of 100mA, this stage should be able to switch 1 to 5A of transformer primary current, depending upon the choice of transistors. The sum of R_1 and R_2 determine the maximum steady state output current of the UC1525A while their ratio defines the voltage across C_2 which, at turn off, becomes the reverse V_{BE} for Q_1. With the values given, the output current and voltage waveforms are shown in *Figure 7* for a one microsecond pulse. If power FETs are used for the output switches as shown in *Figure 8,* the interfacing circuitry can become even simpler with only a small series gate resistor potentially required to damp spurious oscillations within the FET.

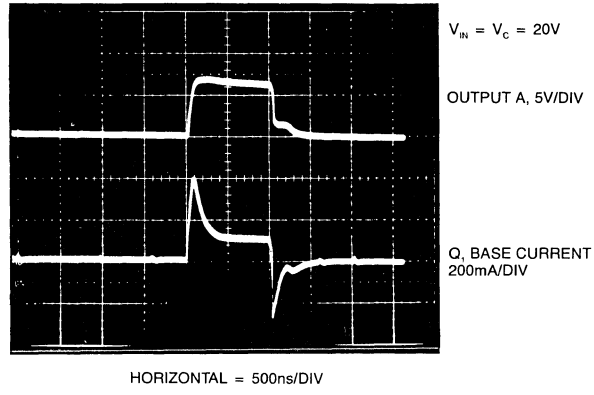


Figure 7. Base current waveforms (Figure 6 circuit) show the enhanced turn-on and turn-off current possible with the UC1525A.

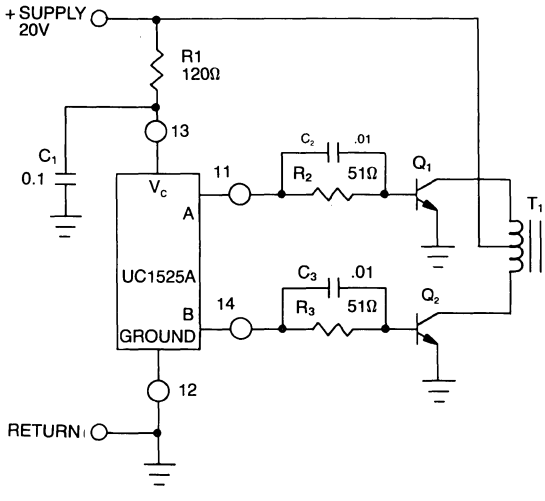


Figure 6. A typical push-pull converter power stage using external bipolar power transistor switches.

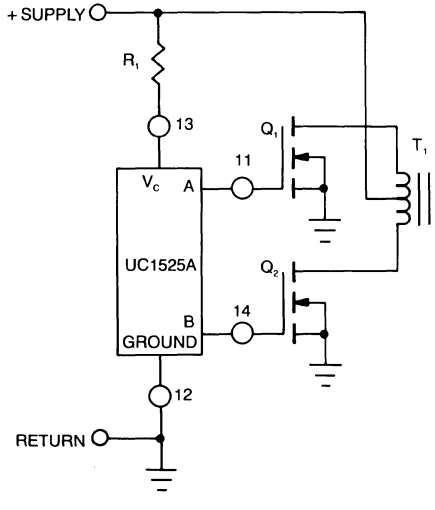


Figure 8. Replacing bipolar transistors with POWER MOSFETs provides even greater simplicity due to the low driving impedances of the UC1525A in each transition.

Push-pull direct transformer drive is also particularly advantageous with UC1525A as shown in *Figure 9.* A version of this configuration is required for isolation when the control circuit is referenced to the secondary side of an off-line power system, and to provide level shifting of drive signals for ½ bridge and full bridge switching. The configuration of *Figure 9* has a couple of important advantages. First, by connecting the drive transformer primary directly between the outputs of the UC1525A, no center-tap is needed and the full primary is driven with opposite polarities. Secondly, between each output pulse, both outputs are pulled to ground which effectively shorts the two ends of the primary winding together coupling a low-impedance turn-off signal to the switching transistors.

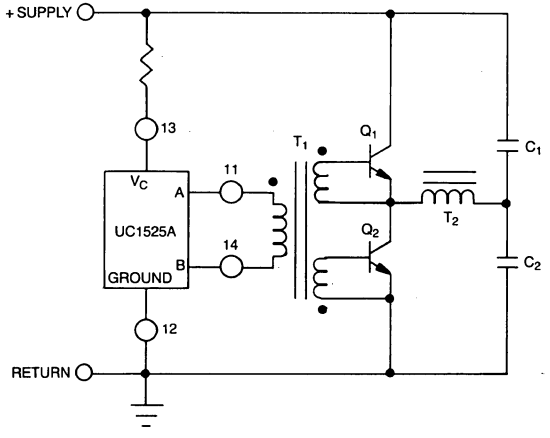


Figure 9. The UC1525A is ideally suited for driving a low-power base drive transformer and eliminates the need for a primary centertap.

A useful single-ended configuration, typical of buck regulators, is shown in *Figure 10.* Here the UC1525A outputs are grounded and the PWM signal is taken from the V_C terminal which switches close to ground during each clock period as the internal source transistors are alternately sequenced.

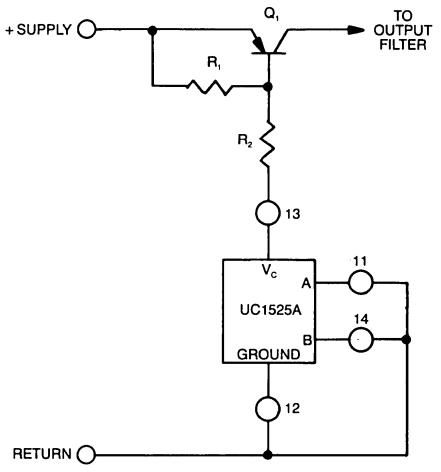


Figure 10. A single-ended, ground-referenced power stage for a flyback or boost regulator.

Controlling Power Supply Start-Up

Although the advantages of the UC1525A's output stage will often be reason enough for its selection, there are several other important and useful features incorporated within this product. One problem previously overlooked in PWM circuits is keeping the output under control as the supply voltage is turned on and off. Undefined states, particularly the possibility of turning on an output before the oscillator is running, can be quite awkward, if not catastrophic. To prevent this, the UC1525A has incorporated an under-voltage lockout circuit which effectively clamps the outputs to the off state with as little as 2½V of supply voltage which is less than the voltage required to turn the outputs on. This clamp is maintained until the supply reaches approximately 8V insuring that all the remaining UC1525A circuitry is fully operational prior to enabling the outputs. The clamp reactivates when the supply is lowered to approximately 7.5V. There is about 500mV of hysteresis built in to eliminate clamp oscillation at threshold.

Another important aspect of power sequencing is restraining the outputs from immediately commanding a 100% duty cycle when they are activated. This is accomplished by a slow turn on (soft-start) which is defined by an internal 50μA current source in conjunction with an externally applied capacitor. The details of this power sequencing system are shown in Figure 11.

Q_3 and Q_4 are the output gates normally driven by the oscillator through D_2 to provide output blanking between pulses. (One of these transistors is shown as Q_2 in Figure 3.) At low supply voltages, Q_2 conducts with base drive from the 20μA current source. Q_2 provides three functions. First, current through R_4 activates the output gates with minimum voltage drop. Second, current through R_5 activates the shutdown transistor Q_5 holding the soft-start capacitor, C_{SS}, discharged. Third, R_2 provides a small bucking voltage across R_3 for hysteresis at the switch point.

When the input voltage becomes high enough to provide a little more than one volt at the base of Q_1, that transistor turns on. This turns off Q_2, activating the outputs and allowing C_{SS} to begin to charge from the internal 50μA current source. The time to reach approximately 50% duty cycle will be

$$t = \left(\frac{2 \text{ volts}}{50\mu A} \right) Css$$

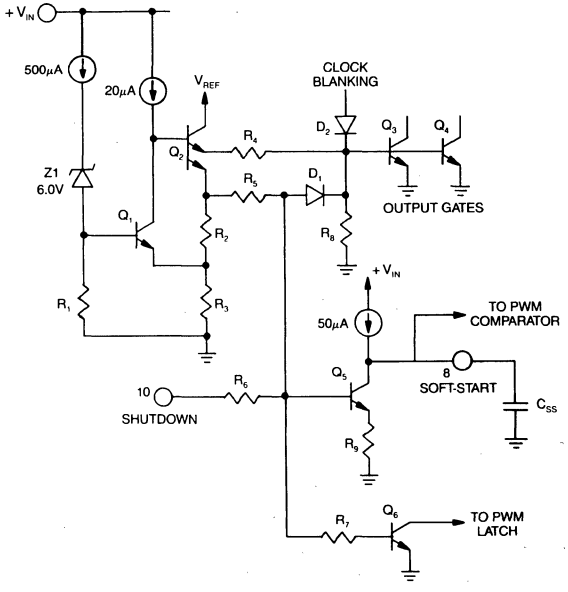


Figure 11. The internal power turn-on, soft-start, and shutdown circuitry of the UC1525A.

Power Supply Shutdown

An important part of any PWM controller is the ability to shut it down at any time for a variety of reasons, including system sequencing requirements or fault protection. Several options are available to the user of the UC1525A, which require an understanding of the capability of the shutdown terminal, pin 10. Referring to *Figure 11,* the base of Q_5 is turned on by a signal which is clamped to approximately 1.4V by the action of D_1 and the V_{BE} of gates Q_3 and Q_4. This holds the outputs off and keeps C_{SS} discharged by Q_5 which, with R9, becomes a 100μA net current sink.

If, during normal operation, pin 10 is pulled high, three things happen. First, the outputs are turned off within 200ns through D_1. Second, the PWM latch is set by Q_6 so that even if the signal at pin 10 were to disappear, the outputs would stay off for the duration of that period, being reset by the next clock pulse. Third, Q_5 is activated commencing a 100μA discharge of C_{SS}. However, if the activation pulse on pin 10 has a duration shorter than ⅓ of the clock period, the voltage on C_{SS} will remain high and soft-start will not be reactivated. Naturally, a fixed signal on pin 10 will eventually discharge C_{SS}, recycling soft-start. Thus, the shutdown pin provides both sequencing capability as well as a convenient port for protective functions, including pulse-by-pulse current limiting.

Regulating PWM Performance Improvements

The UC1525A also offers significant performance and application improvements in almost all of the additional basic functions of a PWM over those obtainable with earlier devices. A general description of these features is outlined below:

Reference Regulator: The output voltage of this regulator is internally trimmed to 5.1V ±1% during manufacture, eliminating the need for adjusting potentiomenters in most applications.

Error Amplifier: The UC1525A uses the same basic transconductance amplifier as the UC1524 with an important difference: it is powered by V_{IN} rather than V_{REF}. Now the input common-mode range includes V_{REF} eliminating the need for a voltage divider with its attendant tolerances. An additional feature relative to the error amplifier is that the shutdown circuitry feeds into a separate input to the PWM comparator allowing pulse termination without affecting the output of the error amplifier which might have a slow recovery, depending upon the external compensation network selected. An

important benefit of a transconductance amplifier is the ease with which its current mode output can be over-ridden by other external controlling signals.

PWM Comparator: The significant benefit of the UC1525A's PWM comparator is in its following latch. A common problem with earlier devices was that any noise or ringing on the output of the error amplifier would affect multiple crossings of the oscillator ramp signal resulting in multiple pulsing at the comparator's output. The UC1525A's latch terminates the output pulse with the first signal from the comparator, insuring that there can be only a single pulse per period, removing all jitter or threshold oscillation from the system. Another important advantage of this latch is the ability to easily implement digital or pulse-by-pulse current limiting by merely momentarily activating the shutdown circuitry within the UC1525A. This could be as simple as connecting pin 10 to a ground-referenced current sensing resistor. For greater accuracy, some added gain may be advantageous. Once a current signal causes shutdown, the output will remain terminated for the duration of the period, even though the current signal is now gone. An oscillator clock signal resets the latch to start each period anew.

Oscillator: The functions of the oscillator within the UC1525A have been broadened in two important aspects. One is the addition of a synchronization terminal, pin 3, allowing much easier interfacing to an external clock signal or to synchronize multiple UC1525A's together. The other is the separation of the oscillator's discharge network from its charging current source for deadtime control. Reference should be made to the schematic of *Figure 12* for an understanding of the operation of this circuit. The heart of this oscillator is a double-threshold comparator, Q_7 and Q_8, which allows the timing capacitor to charge to an upper threshold by means of the current source defined by R_T and mirrored by Q_1 and Q_2.The comparator then switches to a lower threshold by turning on Q_{10} and discharges C_T through Q_3 and Q_4 with a rate defined by R_D. As long as C_T is discharging, the clock output is high, blanking the outputs. Since the overall oscillator frequency is defined by the sum of the charge and discharge times, there are three elements now in the frequency equation which is approximately:

$$f \approx \frac{1}{C_T (0.7R_T + 3R_D)}$$

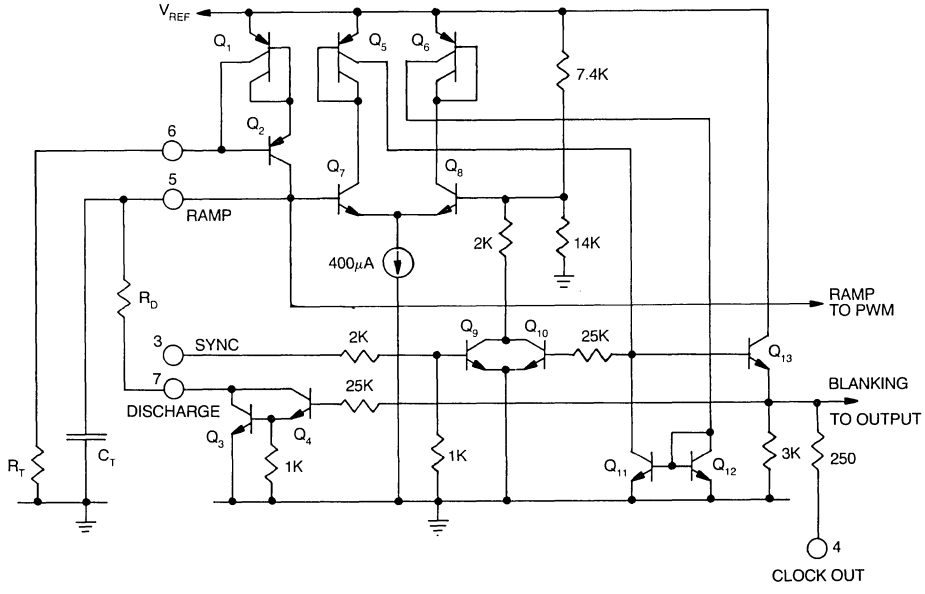


Figure 12. A simplified schematic of the UC1525A's oscillator circuitry.

External synchronization can easily be accomplished with a 2.8V positive pulse at pin 3. This will turn on Q_9, lowering the comparator threshold below wherever the voltage on C_T may happen to be. Two factors should be considered: First, the voltage on C_T determines the amplitude of the PWM ramp, and if the sync occurs too early, the loop gain will be higher and the resolution may be worse. Second, the sync circuit is regenerative within 200ns; and, while a wider pulse can be used, C_T will not begin to recharge as long as the sync pin is high. For synchronizing multiple UC1525A devices together, one need only to define a master with the correct R_TC_T time constant, connect its output pin to the slave sync pins, and set each slave R_TC_T for a time constant 10–20% longer than the master.

A 200 Watt, Off-Line, Forward Converter

The ease of interfacing the UC3525A into a practical power supply system can be illustrated by the off-line, power converter shown in *Figure 13.* This 200W supply places the control circuitry on the primary side of the power transformer where direct coupling can be used to drive the power switch. While simplifying the drive electronics, this configuration usually requires an isolated voltage feedback signal which is most easily accomplished by an optocoupler driven by some type of voltage regulator IC such as a SG723 or LM305. One other undefined block in *Figure 13* is the auxilliary power supply which suppplies the low voltage, low current bias supply for the UC1525A and the drive for Q_1, the power switch. The choice of the UFN443 POWER MOSFET

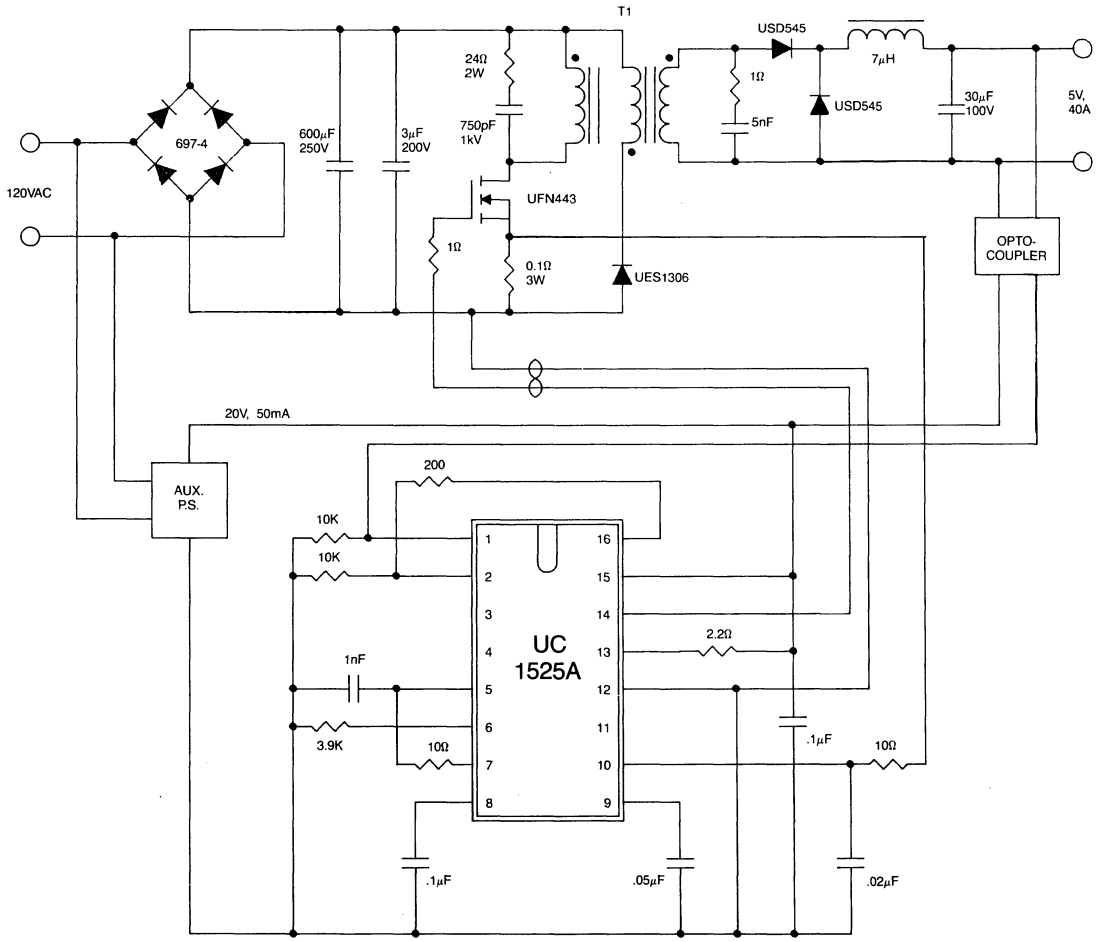


Figure 13. 200W, Off-Line Forward Converter.

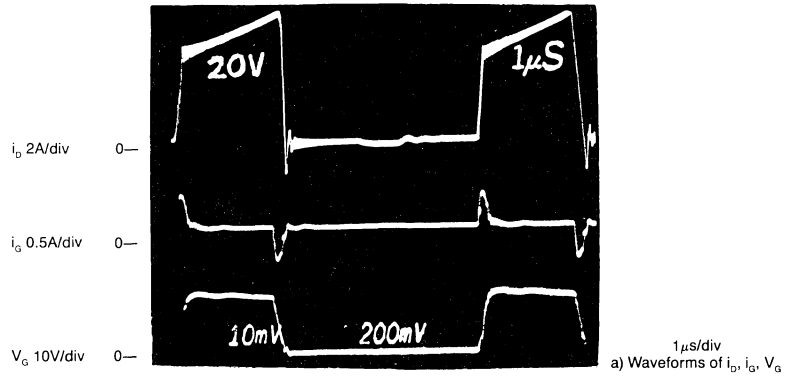
for this switch keeps the total power requirements from the auxiliary supply at less than 1W; readily implemented with a small, line-driven transformer.

This converter is designed to operate at 150kHz which is accomplished by running the UC1525A at 300kHz and using only one of the outputs. This also automatically insures that the duty cycle can never be greater than 50%, a requirement of the power transformer in this configuration. The high operating frequency allows the output filter's roll-off to be set at 12kHz, greatly simplifying the overall loop stability considerations as adequate response can be achieved with only the single-pole compensation of the error amplifier provided by the .05μF capacitor on pin 9.

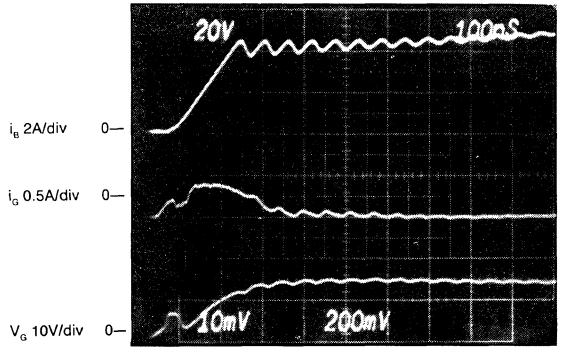
The totem-pole output of the UC1525A is used to advantage to drive Q_1 by providing a 400mA peak current to charge and discharge the MOSFET's gate capacitance while keeping overall power dissipation low. Waveform photographs of this operation are shown in *Figure 14.*

When operating at full load, the efficiency of this converter is 73% with by far the greatest power losses occurring in the output rectifiers—even though Schottky devices have been selected. Switching losses have been minimized by the fast current transitions, primarily defined by the leakage inductance of the transformer. Although this switching time could probably be even further reduced, there could be problems with current spikes during rise time due to Schottky rectifier capacitance.

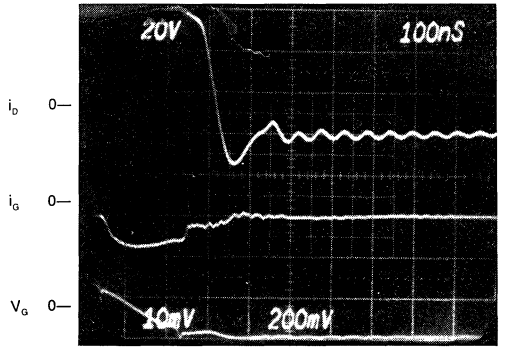
Current limiting for this converter is provided by measuring the current in UFN443 with the 0.1Ω resistor in series with the source and using this voltage to activate the shutdown circuitry within the UC1525A. While this will provide a fast-acting short circuit protection on a pulse-by-pulse basis, a comparator may need to be added for a more accurate current limit threshold.



a) Waveforms of i_D, i_G, V_G



b) Risetime
≈90ns



c) Falltime
≈30ns

Figure 14. Current and voltage waveforms for the 200W, Off-Line Forward Converter with a UC1525A direct driven MOSFET Power switch. (Operating frequency is 150kHz with output current equal to 40A.)

Transformer Winding Data

500 Watt, 100kHz, Off-Line, Half-Bridge Converter

T1 Core: Ferrox 846T250-3C8
Pri: 14T #22AWG
Sec (2): 7T #22AWG

T2 Core: Ferrox EC52-3C8 (EE)
Pri: 14T, 2 layers, 2 #16 AWG in parallel
Sec (2): each 2T, C.T., copper strap .01″ × .8″

T3 Core: Ferrox 846T250-3C8
Pri: 1T
Sec: 20T, C.T. #22AWG

T4 117V/220V, 25V, 0.15A, 50-60Hz

L1 Core: Ferrox IF30-3C8
4 turns, 5 #12AWG in parallel

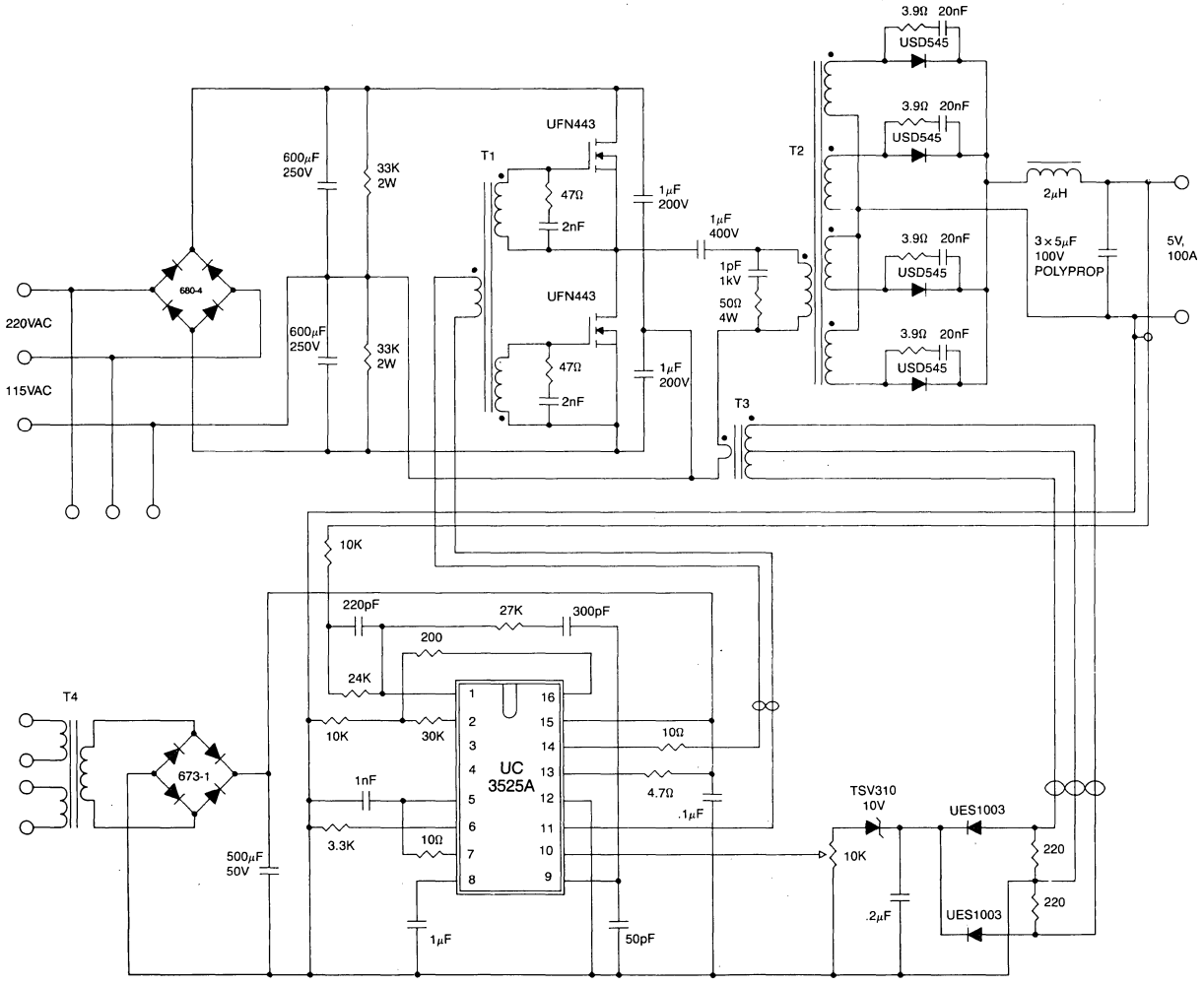


Figure 15. 500W, 100kHz Half-Bridge Schematic.

500 Watt, Off-Line, Half-Bridge Converter

The circuit shown in *Figure 15* uses a pair of Unitrode UFN443 POWER MOSFETs in a half-bridge configuration with the UC1525A chip referenced to the secondary side of the power transformer. The MOSFET gates are driven directly from the control chip output through step down and isolation transformer T_1. The UC1525A output terminals (pins 11 and 14) provide active pull-up and pull-down (dual source/sink) for the primary of T_1. This provides the fast, high current turn-on and turn-off pulses needed for the MOSFET gates. In addition, the two ends of the primary windings are shorted to ground during deadtime, which prevents accidental turn-on by transients. Note that the current supplied by the UC1525A outputs drops to a small value when the gate capacitance has been charged or discharged to the desired gate voltage. Damping resistors with series blocking capacitors across the two secondaries of T_1 minimize ringing due to the MOSFET gate capacitance and the inductance of T_1 and lead inductance, particularly during deadtime.

Deadtime for the UC1525A is set very simply by a single resistor between pins 5 and 7. Only a small amount of deadtime is needed since the MOSFETS have no storage time and a very short delay time.

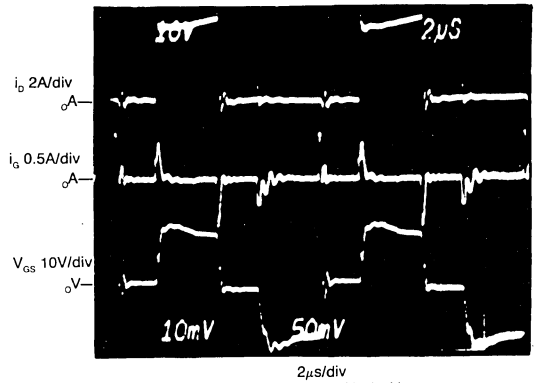
Slow turn-on is accomplished by a single capacitor at pin 8.

Current limiting is provided by current transformer T_3 in series with the primary of the power transformer T_2. The signal is rectified, threshold adjusted and sent to the shutdown terminal, pin 10, of the UC1525A.

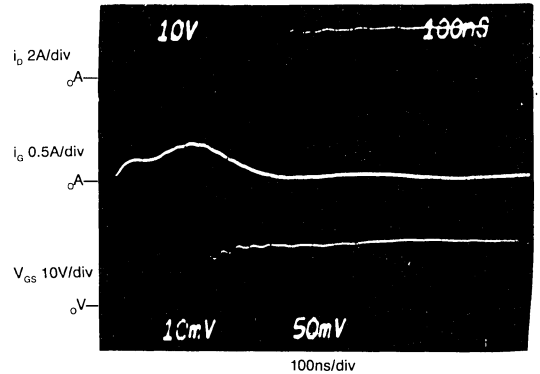
Waveforms of the converter are shown in the scope photos of *Figure 16*. Current rise and fall times are 20ns and 10ns. For additional details on this design, see Unitrode Application Note U-87, a 500W, 200kHz Off-Line Power Supply using POWER MOSFETS.

Improved Performance; Less Complexity

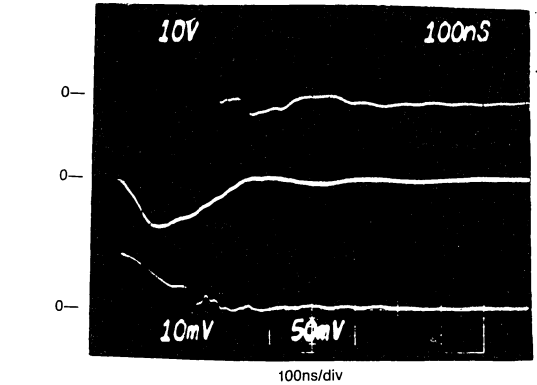
Although power supply designers for some time now have had an ever widening inventory of IC components available to ease their design tasks, the final measure of improvement has to be in terms of system performance versus cost. With fewer interface components to the power stages, freedom from potentiometer adjustments, protected start-up and shut-down, a built in soft-start network and several additional system-level features, the UC1525A provides a significant contribution to both performance and costs while simultaneously making the designer's task easier. With these accomplishments, it is clear that this device truly does represent a step-function improvement, introducing a second-generation of power control components.



2μs/div
a) Waveforms of i_D, i_G, V_G



100ns/div
b) Risetime



100ns/div
c) Falltime

Figure 16. Performance waveforms for the Half-Bridge, 500W, 100kHz Converter with output current of 80A.

THE UC1524A INTEGRATED PWM CONTROL CIRCUIT PROVIDES NEW PERFORMANCE LEVELS FOR AN OLD STANDARD

Introduction

The application of IC technology to the switching power supply really began with the introduction of the SG1524 in 1976. This device was the first IC to implement all the control blocks necessary for a wide range of PWM power systems. Its straight-forward approach to the classic PWM architecture gave it wide acceptance, and it has become the most commonly used IC controller today.

Even though the 1524 has gained great acceptance and engineers have praised its versatile and easy to understand architecture, they have many times cursed the simplistic, or idealistic, ways its individual blocks were implemented. While one would assume, at first glance, that all control functions necessary for most power supply applications are contained within the 1524, in the real world of practical power systems, additional circuitry is required to interface with the rest of the system, to protect against different types of fault conditions, to adjust for inaccuracies, or to improve control during power sequencing.

Although in the intervening years, many new IC control chips have been introduced which offer certain specialized advantages, it was found that design engineers still preferred the 1524 for its wide versatility and generalized architecture. From this understanding, it became apparent that a new design, which would improve many of the 1524's individual functions by making them more predictable and easier to apply, while retaining the same architecture, could be a winner. Thus, Unitrode undertook this task. The result is the UC1524A.

The UC1524A PWM Controller

A design goal set for the UC1524A was that it not only retain the same architecture but keep the same pin configuration as the 1524 and function equal to or better than the 1524 in most existing applications. In

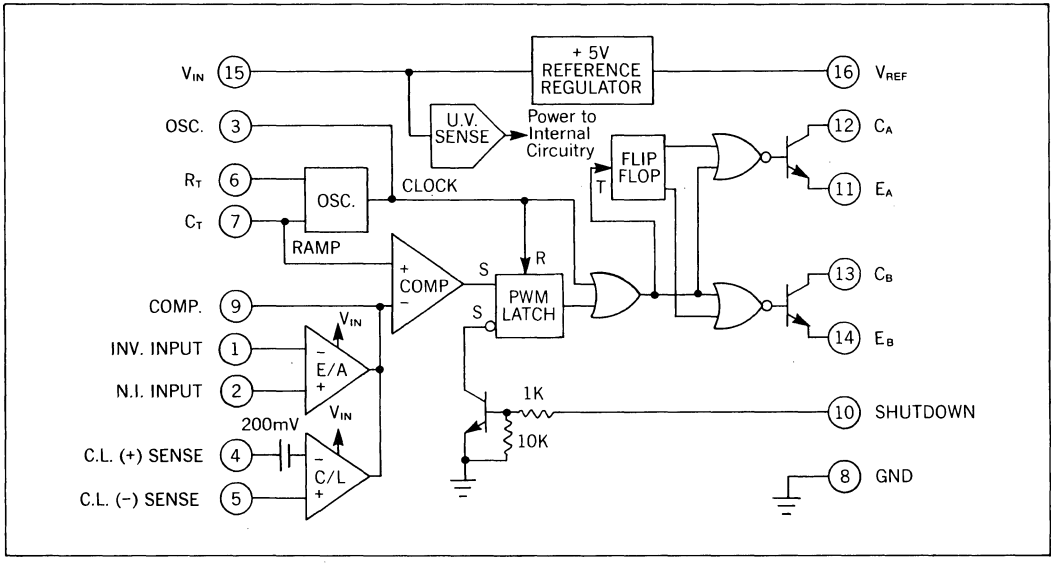


FIGURE 1 — The UC1524A Block Diagram Follows the Same Architecture As the UC1524 But With Several Significant Differences.

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TWX (710) 326-6509 • TELEX 95-1064

this way, engineers who were familiar with the 1524 could easily understand and evaluate the UC1524A. Performance improvements had to be significant, particularly in reducing the need for discrete support circuitry, so there would be a cost advantage in using the UC1524A in new designs. The block diagram of the UC1524A is shown in Figure 1 which, by intent, appears very similar to that of the older 1524.

The list of the improvements, however, is considerable and includes the following:

1. The 5V reference is now internally trimmed to ±1% accuracy, eliminating the need for potentiometer adjustments.
2. The error amplifier's input range now extends beyond 5V, eliminating the need for a pair of dividers and their attendant tolerances.
3. A high-gain, wide-band, current sense amplifier has been included which is useful for either linear or pulse-by-pulse current limiting in the ground or power supply output lines.
4. An under-voltage lockout circuit has been added which disables all the internal circuitry except the reference until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low-power, off-line converters. There is approximately 600mV of hysteresis included for jitter-free activation.
5. A PWM latch has been added insuring freedom from multiple pulsing within a period, even in noisy environments. In addition, the shutdown circuit feeds directly to this latch which will disable the outputs within 200ns of activation.
6. The oscillator circuit is usable to frequencies beyond 500kHz and is easier to synchronize with an external clock pulse.
7. The power capability of the output switches has been boosted by doubling the current capability to 200mA and increasing the voltage rating to 60V.

An understanding of some of these improvements is necessary for ease in application and will now be discussed in greater detail.

Internal Power Turn-on Circuit

The under-voltage lockout and turn-on hysteresis circuit is shown in Figure 2. This circuit requires approximately 2V for activation; but, since nothing else will turn on without at least 3V of supply voltage, lockout is assured. When V_{IN} rises above 2V, R_2 begins to

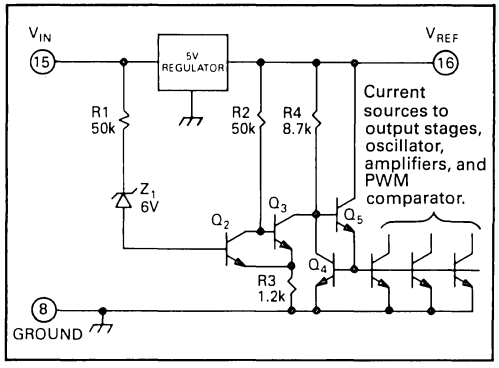


FIGURE 2 — The Under-Voltage Lockout and Power Turn-On Circuitry within the UC1524A.

conduct saturating Q_3 and holding the base of Q_5 too low to allow any of the current sources to conduct. The current through R_4 flows through Q_3 and R_3, developing a 600mV drop across R_3 when V_{REF} reaches 5V. At this level, the only current flowing is that used by the reference regulator and R_2 and R_4, a total of approximately 2.5mA at turn-on threshold.

When the input voltage reaches approximately 8V, diode, Z_1 begins to conduct turning on Q_2 which turns off Q_3 and allows the current sources to activate. Since the current through Q_2 is much less than through Q_3, the voltage across R_3 drops, providing positive feed-

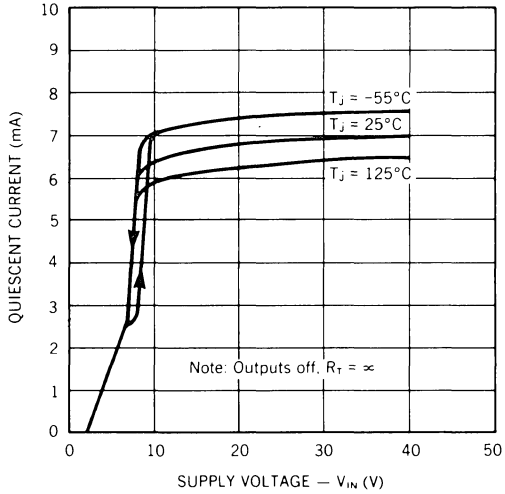


FIGURE 3 — Supply Current for the UC1524A vs. Input Voltage.

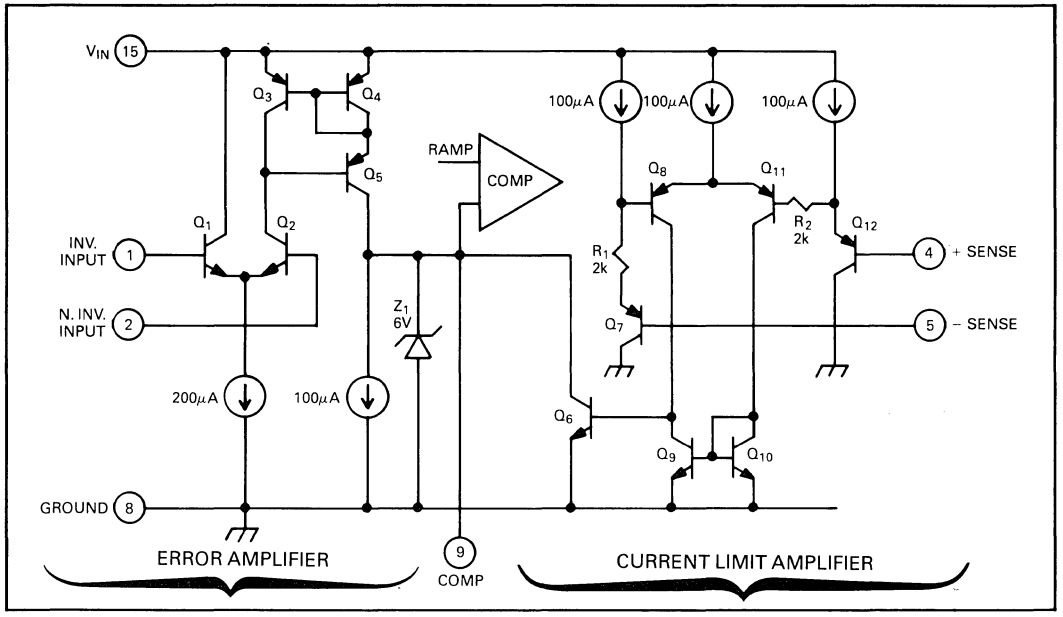


FIGURE 4 — Voltage and Current Sensing Amplifiers Have a Common Output at the Input to the PWM Comparator.

back. This gives about 600mV of hysteresis. This circuit, of course, works in reverse at turn off, insuring that the outputs can only operate when the supply is adequate for fully predictable operation. Figure 3 shows the relationship between quiescent current and input voltage. Designers should find this low current start-up characteristic quite advantageous for off-line, primary-side control with boot-strapped operation after turn on.

A New Current Limit Amplifier

Since the outputs of the current limit amplifier and the voltage-sensing error amplifier are summed at the PWM comparator input, they should be examined together as shown in Figure 4.

Since the error amplifier, consisting of transistors Q_1 through Q_5, must have the lowest priority in controlling the PWM, its output must be easily overruled by current faults or other programming functions, such as soft-start, which would hold pin 9 low. Therefore, a transconductance amplifier similar to that used in the earlier 1524 was again applied to the 1524A with one exception: it is now powered by V_{IN} instead of V_{REF}, so that the input common-mode range extends to within 2V of either rail. Zener diode, Z_1, is used on the output to keep the input level to the PWM comparator below 6 volts.

The error amplifier's output can be considered a 100μA current source or sink (0 - 200μA source with 100μA constant sink). When the current limit circuit activates, Q_6 turns on and can easily pull down pin 9 even though the error amplifier would nominally be calling for a high output at this point.

The current limit circuit consists of Q_6 through Q_{12}. Its differential PNP input stage gives it a common mode range extending from 300mV below ground to within −2V of V_{IN}. Its threshold, or offset, of 200mV is established by the 100μA current source through R_1, with R_2 added to null out the effect of any base current from Q_8.

This current sensing block within the UC1524A can actually be used either as a linear amplifier or as a comparator. The open loop small-signal gain is approximately 80dB while its transition delay with 10% overdrive is 600ns. This can be decreased substantially with additional overdrive. Use of the current sensing block as a comparator is usually preferred from a systems standpoint, since it does not have to be compensated and pin 9 can be dedicated solely to

error amplifier compensation. Under this condition, a current signal over the threshold level will pull pin 9 low, terminating the output signal. Recovery is determined by the 100μA pull-up current from the error amplifier in conjunction with any capacitance which may be present on pin 9.

When the current limit circuit is used as a linear amplifier, stabilization is performed by feedback to the inverting input (pin 4) or by capacitance from pin 9 to ground as shown in Figure 5.

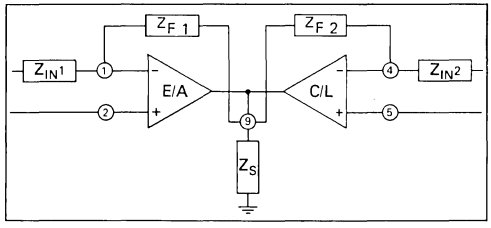


FIGURE 5 — Various Compensation Options Which Are Possible When Both Amplifiers Are Operated in the Linear Mode.

An additional feature of this circuit is its capability to perform as a duty-cycle limiting circuit in the configuration shown in Figure 6. If R_1 is made 100k, there will be minimal effect upon the error amplifier gain.

In current limiting, to achieve the fastest responding pulse-by-pulse control, consideration should be given to the use of the shutdown terminal on pin 10. While the input threshold of this circuit is not as accurately controlled as the current limit amplifier and has a negative temperature coefficient of −2mV/°C and is internally ground referenced; it does feed directly into the PWM latch with only 200ns delay from activation of pin 10 to shutdown of the outputs.

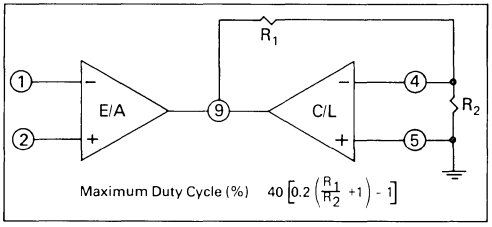


FIGURE 6 — The Fixed 200mV Threshold of the Current Limit Amplifier Can Be Multiplied to Form a Duty-Cycle Clamp or Dead-Band Control.

PWM Comparator and Latch

The PWM latch insures only a single pulse is allowed to reach the appropriate output stage within each period. The latch is reset with the oscillator clock pulse which also serves to blank the outputs. Thus, although the latch is reset at the start of the oscillator clock pulse, it is the termination of the clock pulse which initiates output conduction. The output then stays on until the latch is set, either by a signal from the PWM comparator or from a shutdown command from pin 10. Once the latch is set, it will hold the output off for the duration of the period.

There are several significant advantages to this circuit. First, the latch completely eliminates multiple outputs of the PWM comparator because of noise or ringing on the output of the error amplifier causing multiple crossings of the ramp signal. Second, current limiting can now be performed much more rapidly without instability. Without a latch, significant integration is needed to maintain a turn-off signal after the outputs have turned off. Finally, any instabilities which might potentially be present in the voltage or current loops, or the shutdown signal from pin 10, will cause much less stress on the output stages, since only two transitions through the high-dissipation active region can be made during each period.

The performance of this portion of the UC1524A can be evaluated using a triggerable pulse generator with a variable delay, set up as shown in Figure 7. R_T and C_T are selected for the desired operating frequency. The clock triggers the pulse generator, and the delay is adjusted so the generator output occurs during the PWM period. The output pulse width must be at least 200ns and the amplitude higher than the threshold of the UC1524A input being evaluated. Typical waveform photographs are shown in Figure 8.

Higher Power Output Switches

With the higher current and voltage rating of the UC1524A's output switches, significant economies can now be achieved in interfacing with higher power devices. For low power requirements, a broader range of applications may now be served by the 1524A itself without additional discrete output devices. Regardless of the power supply requirements, more current and voltage from the UC1524A will ease the design tradeoffs. Even with higher current and voltage, the UC1524A offers fast response time. Each output stage contains an anti-saturation network to keep the output transistors out of hard saturation. Although this adds

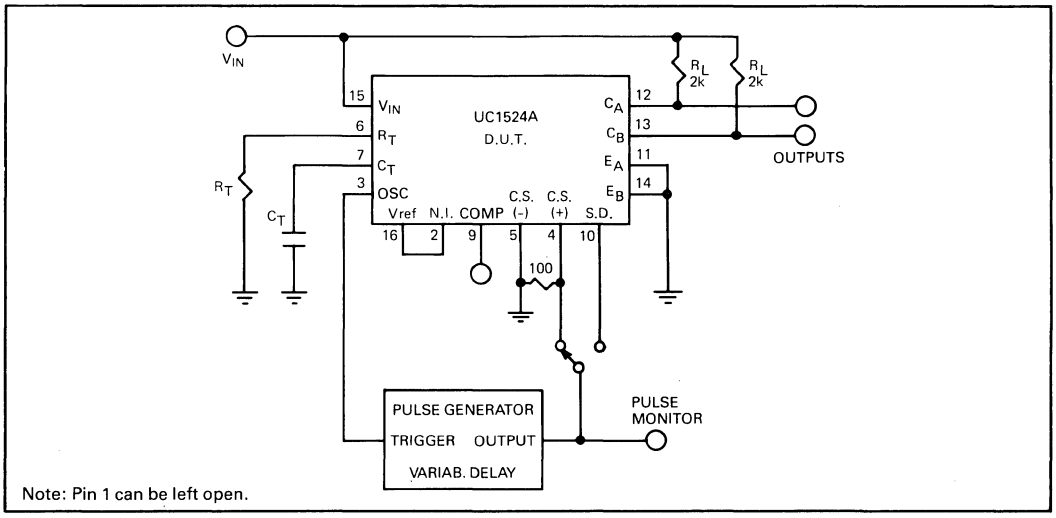


FIGURE 7 — Evaluating the Turn-off Delays of the UC1524A with the Aid of a Triggerable Pulse Generator With Variable Delay.

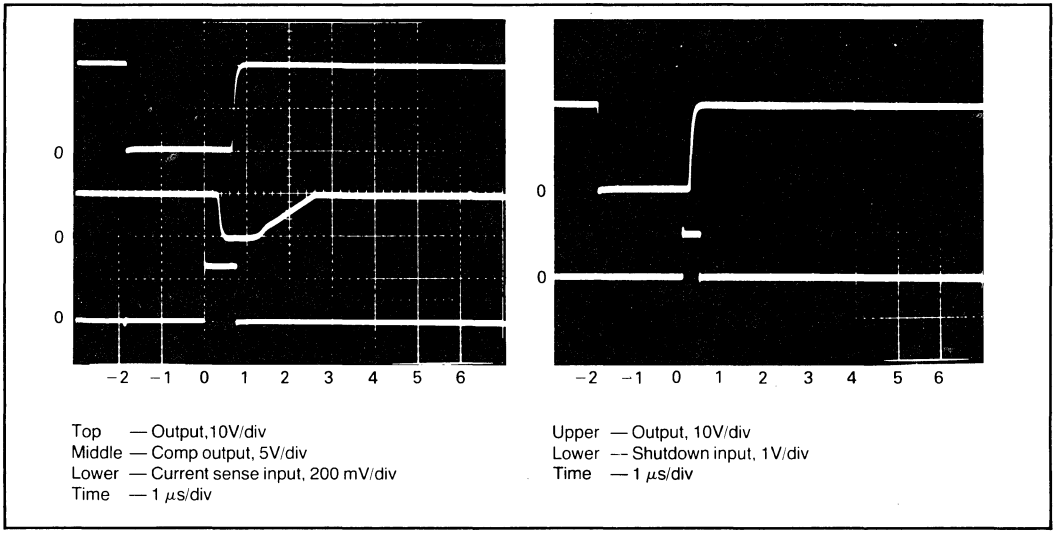


FIGURE 8 — Typical Turn-off Response From Both the Current Sense and Shutdown Inputs.

somewhat to the saturation voltage, it is more than offset by the benefits in reducing turn-off delay. Saturation voltage as a function of current is shown in Figure 9.

Since both collectors and emitters are available on the UC1524A's output transistors, many different coupling possibilities are offered. One useful configuration for enhanced turn-off is shown in Figure 10. The fast-rising signal appearing at the collector of the output transistor, Q_1, is capacitively coupled to saturate an external transistor, Q_2, greatly reducing the turn-off delay of Q_3 and allowing a much larger value to be selected for R_3. Many variations of this circuit are possible depending upon the power devices to be driven and the voltage levels required.

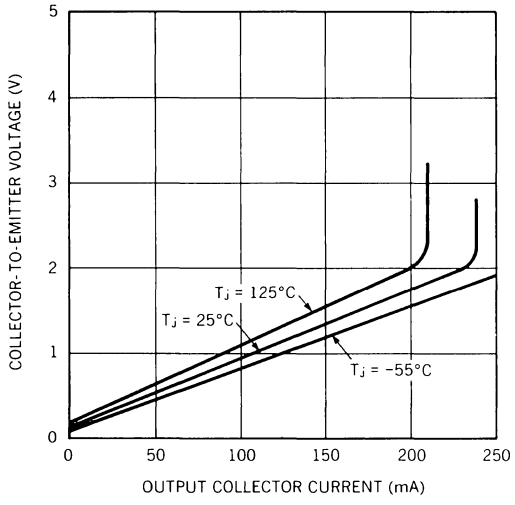


FIGURE 9 — Output Saturation Characteristics for Each of the UC1524A's Outputs.

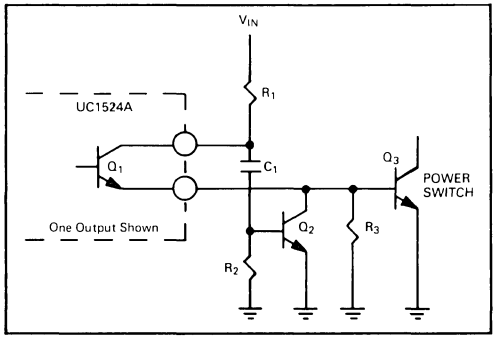


FIGURE 10 — The addition of C_1 and Q_2 Uses the Collector Signal of the UC1524A to Generate an Enhanced Turn-off Command for Q_3

Frequency Synchronization

The oscillator circuit within the UC1524A, shown in Figure 11, has been improved over that of the 1524 with the addition of C_2. Without this component, a synchronizing pulse externally applied to pin 3 had to do all the work of discharging the timing capacitor through Q_4 and Q_5. The simple addition of C_2 couples a positive pulse from pin 3 to the base of Q_{10}, momentarily reducing the threshold of comparator Q_8-Q_9 and regeneratively triggering the oscillator into its discharge state. The circuit is now leading-edge triggered and narrow pulses can be used. This is a consideration when minimum dead time is required, since the outputs are blanked off as long as pin 3 is held high.

As with the 1524, synchronization to an external clock should be done with the R_TC_T time constant set approximately 10 to 20% greater than that determined for the required clock frequency, taking into consideration the expected tolerances of the components. For synchronizing multiple UC1524A devices, all R_T, C_T, and OSC output terminals should be individually connected together and a single R_T and C_T used.

When considering blanking, the pulse on pin 3 may be extended somewhat by the addition of a capacitor of up to 100pF from pin 3 to ground. If narrower blanking pulses are required, adding a resistive load from pin 3 to ground of 1 kohm minimum will reduce the pulse width.

The best way to guarantee a large dead time is still to use a diode to clamp the peak output from the error amplifier to a divider from V_{REF}. This technique is quite accurate due to the accuracy of V_{REF} and the 100μA fixed current available from the amplifier.

A Simple Buck Regulator Circuit

The application of Figure 12 demonstrates the utility of the UC1524A used with a Unitrode PIC600 hybrid switch. This combination greatly simplifies the design of switching regulators, since the only other active device required is a small-signal 2N2222 which serves to provide a constant drive current to the output switch, regardless of the input voltage level. With the UC1524A, current sensing does not have to be done in the ground line, but will still function when the regulator output is shorted to ground.

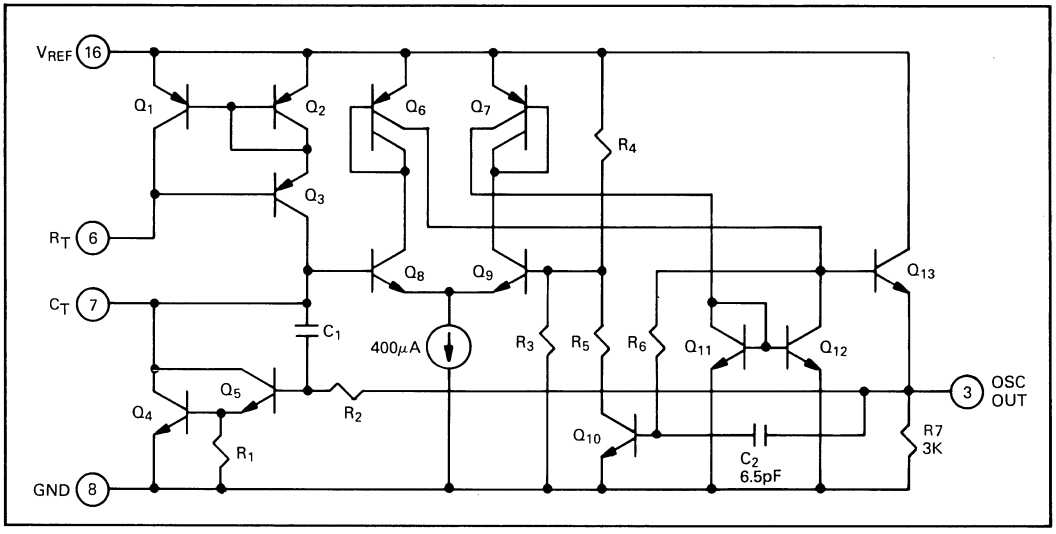


FIGURE 11 — The Oscillator Circuit of the UC1524A Allows Both High Frequency Operation and Ease of External Synchronization.

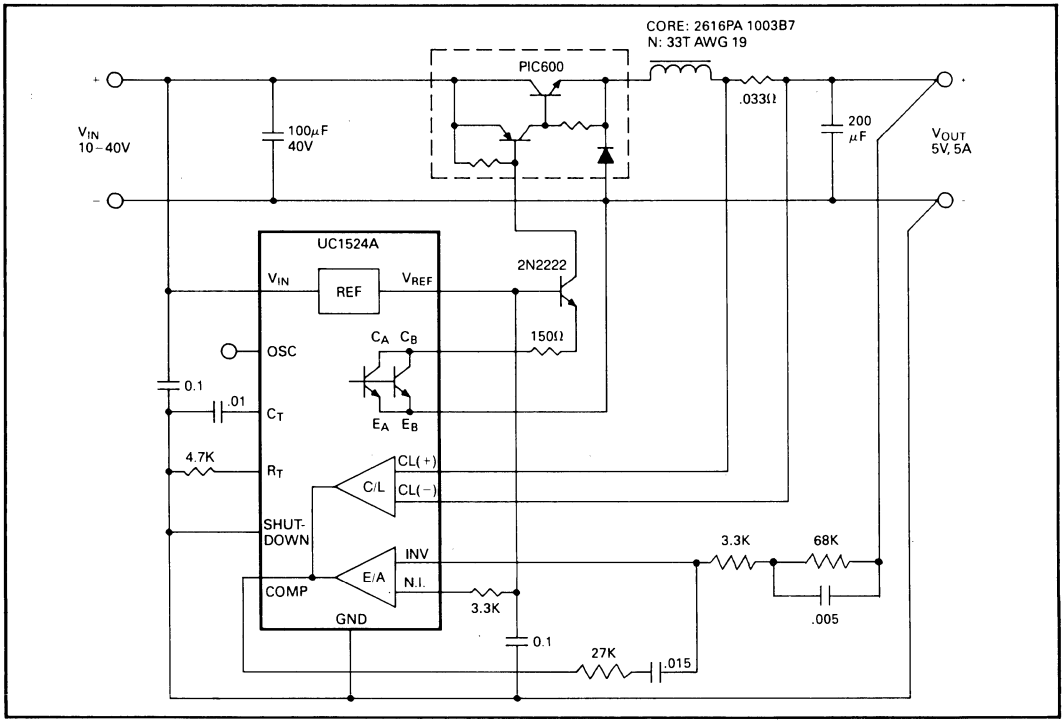


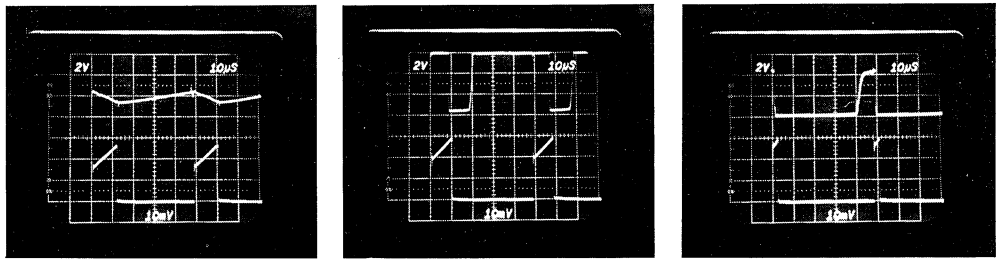
FIGURE 12 — The UC1524A Combines With the PIC 600 Hybrid Switch to Form A Simple But Powerful Buck Regulator.

The waveforms of Figure 13 demonstrate the performance of the current limiting comparator, showing that from the onset of current limiting to a complete short circuit, the peak input current increases from 5.2A to only 5.9A.

A Complete DC-DC Converter with the UC1524A

An important attribute of the new UC1524A family is the higher voltage rating on the output transistors. This now makes it possible to implement a practical 4W DC-DC converter operating from a common 28V bus with no additional output transistors. The schematic of Figure 14 uses a push-pull configuration which imposes a voltage of twice the supply across the "OFF" transistor. This is now within the rating of the UC1524A and, thus, with a 28:7 turns ratio in the transformer, a 5V, ¾A output is achieved with 78% efficiency at a significant minimum parts count.

The fast response of the current limit amplifier within the UC1524A again keeps the device well protected as shown in the waveforms of Figure 15.



A B C

Upper trace is Comp terminal (pin 9), 2 V/div
Lower trace is input current through power switch, 0.2A/div
Time base is 10 μsec/div.

A = Onset of current limiting, I_p = 5.2A
B = Into current limiting, Comp terminal held low until inductor current falls below threshold, Ip = 5.9A
C = Output shorted to ground. Pulse width reduced to 2μs. Ip still 5.9A.

FIGURE 13 — Performance Data for Figure 13's Regulator Shows the Tight Control of Peak Current, Even Under Shorted Output Conditions.

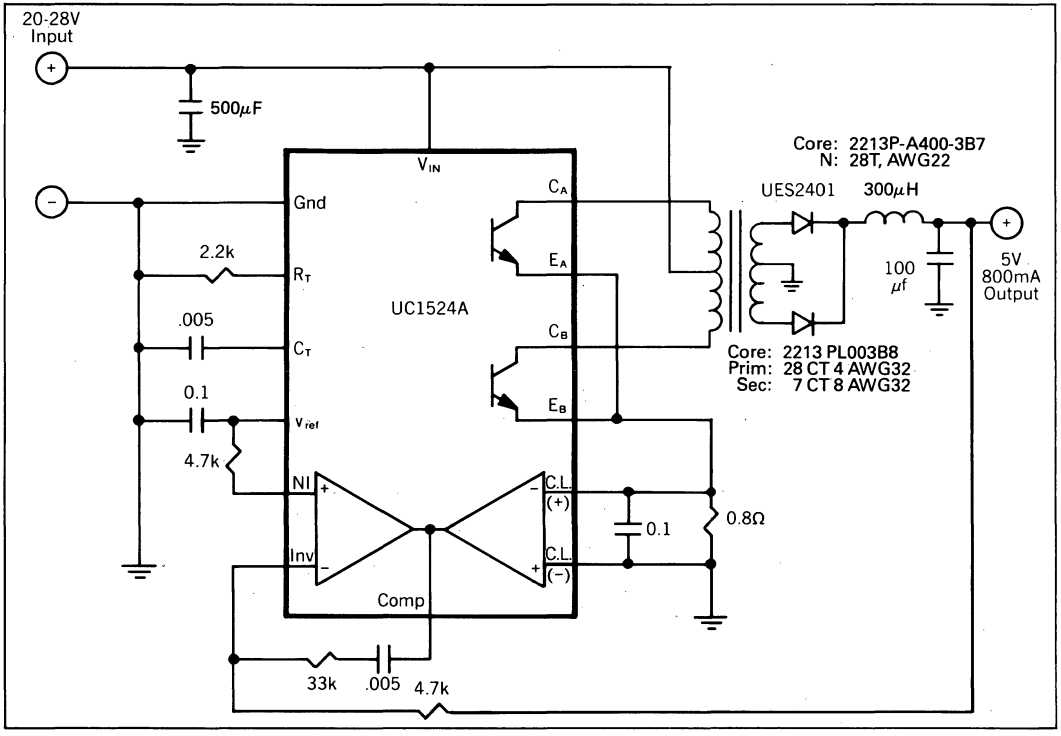
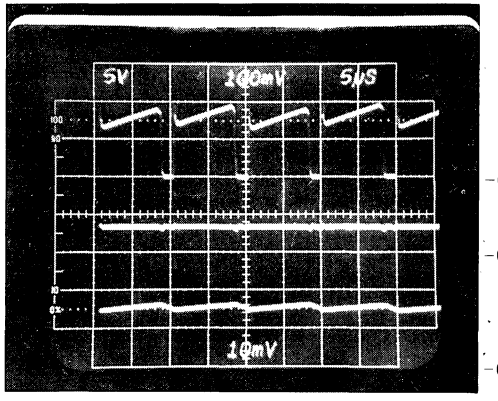
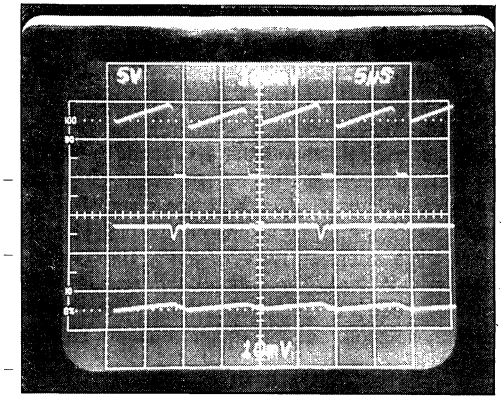


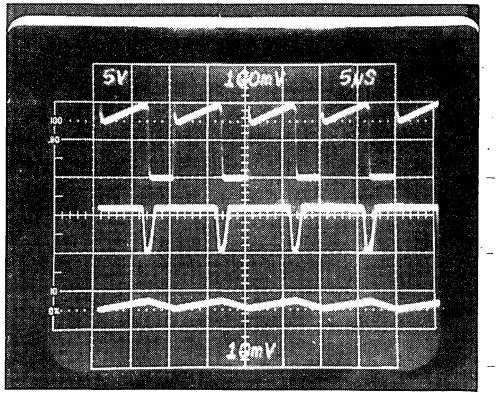
FIGURE 14 — With Higher Output Voltage Capability, the UC1524A can Implement a Complete 4 Watt DC to DC Converter with no Additional Switching Transistors.



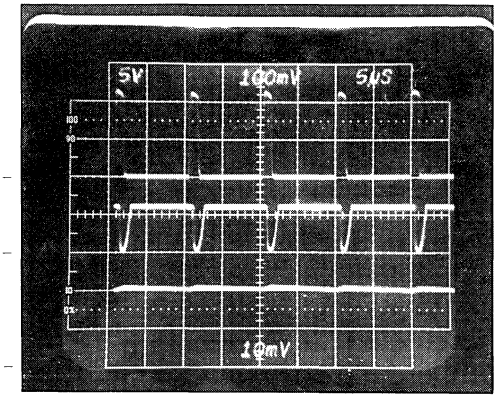
Circuit Under Normal Load



Circuit at Threshold of Current Limiting



Circuit Under Full Current Limit



Circuit Under Short Circuit Conditions

FIGURE 15 — Operating waveforms for the PWM DC-DC converter (Figure 14)
Upper trace = Primary current at 0.1 A/division
Middle trace = Pin 9 voltage at 5V/division
Lower trace = Load current at 0.5A/division
Time base = 5 μs/division

An Off-line Forward Converter

For low to medium power applications, a single-ended flyback or forward converter with all the control on the primary side of the isolation step-down transformer is usually the most economical solution. However there are two complications with this approach. The first is that although the control circuitry can easily be driven from a low-voltage winding on the power transformer, starting energy must be taken from the high-voltage rectified line where, at 170VDC, every 10mA represents a 1.7W loss. The second complication is in obtaining adequate regulation of the output while still meeting isolation requirements from output back to the line.

The 50W forward converter of Figure 16 offers innovative solutions to both these problems. In this circuit, the UC1524A provides all the control with its operating drive power coming from winding N_2. The low-current start-up characteristics of the UC1524A allow starting energy to be developed in C_2 with only approximately 8mA required through R_1.

The problem of isolated feedback control is solved in this application by sampling the 5V output level at the switching frequency by means of the 2N2222 transistor and transformer T_2. With every switching cycle, the output voltage is transferred from N_1 to N_2 where it is peak detected to generate a primary-referenced signal to drive the PWM error amplifier. Diode D_2 is used to temperature compensate for the loss in the rectifier, D_1 and the net result is better than 1% regulation with the main added cost that of a very inexpensive signal transformer.

Some of the other features of this application include a duty-cycle clamp on the PWM formed by diode D_3

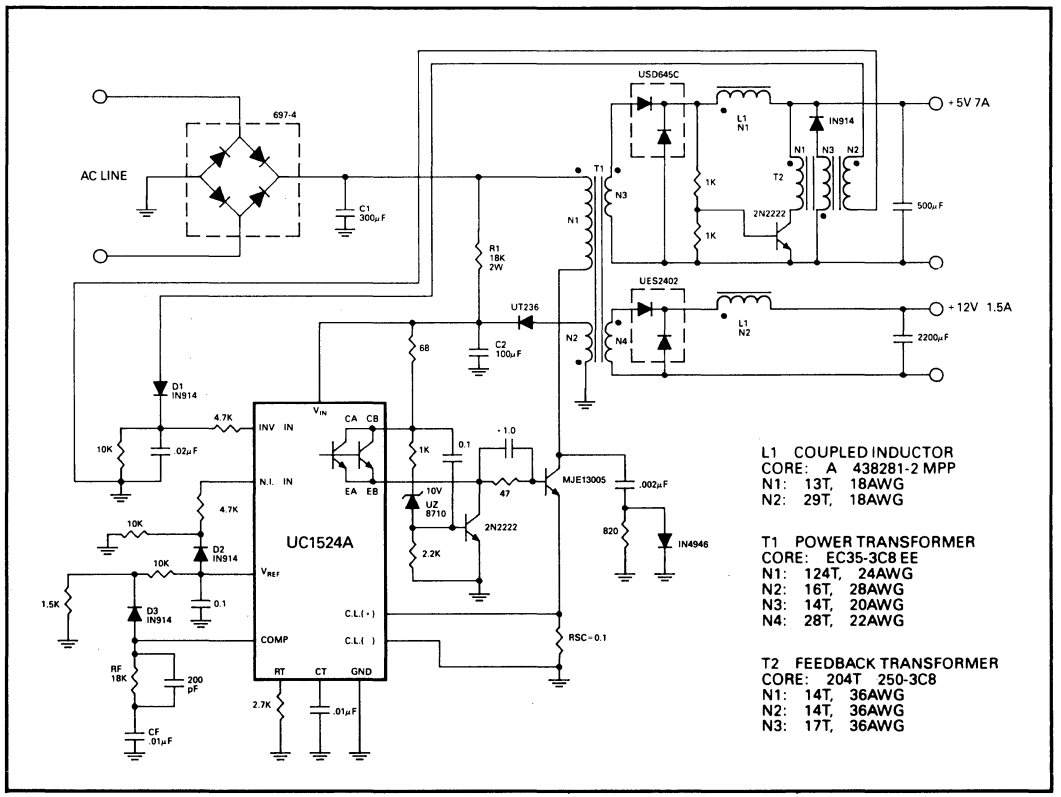


FIGURE 16 —This 50W Off-Line Forward Converter Features Both High Efficiency and Good Regulation while Maintaining Input-Output Isolation.

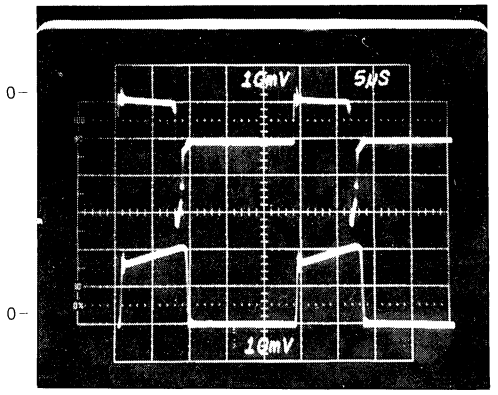
and the 10k - 1.5k divider from V_{REF}. This method of clamping is more effective with the UC1524A since the UV lockout keeps the outputs off until the reference, error amplifier, and oscillator are all operating within specification.

Drive for the UMT13005 high-voltage switch is accomplished by using the emitters of the UC1524A's output transistors for turn-on and the 2N2222 in conjunction with the 1μfd base capacitor to provide a negative base voltage for rapid turn-off as described in Figure 10.

The resultant drive signal is shown in Figure 17. Operating at 40kHz, this regulator provides an isolated 50W of power with an efficiency of 83%, a high degree of regulation, and fast overload protection.

Conclusion

Although there are now many new integrated circuits from which to choose in attempting to build more cost-effective power supplies, it always helps to review well established ideas. In the case of the UC1524A, updating and improving an earlier product has resulted in a significant advancement: providing greater performance and versatility while reducing system costs.



at Full Load (50W)

FIGURE 17 — Base Current (Upper Trace) and Collector Current for the UMT 13005 of Figure 16. The Time Base is 5μs per Division.

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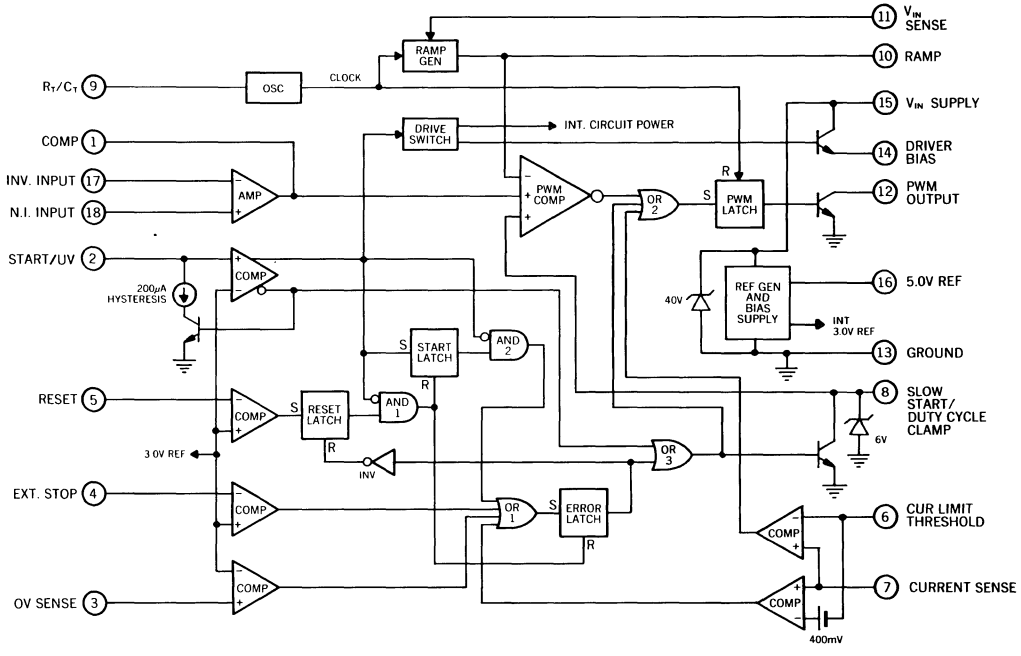
APPLYING THE UC1840 TO PROVIDE TOTAL CONTROL FOR LOW COST, PRIMARY REFERENCED SWITCHING POWER SYSTEMS

1. Introduction

There are many potential approaches to be considered in switch mode power supply design; however, the contradictory requirements of minimum cost and compatibility with ever more demanding line isolation specifications make primary control very attractive. Application of the UC1840 as a primary-side, off-line controller presents an extremely cost-effective approach to supplying isolated power from a widely varying input line while maintaining a high degree of efficiency.

Primary control means referencing all of the control electronics along with the power switching device on the input line side of an isolation transformer. An obvious advantage to this approach is the simplified interface between the control and power switch. This eliminates many of the transitions across the isolation boundary which significantly increase the cost of the magnetics portion of the power supply's budget.

There are two disadvantages to primary control: (1) operating or at least starting, the control electronics from the line voltage (typically 300 VDC), and (2) providing adequate regulation (which requires feedback from the secondary across the isolation boundary). The capability of the UC1840 Control IC to solve these problems while providing all of the regulating, sequencing, monitoring, and protection functions referenced to the primary side, makes this device very attractive.



Note: Positive true logic, latch outputs high with set, reset has priority.

FIGURE 1. THE OVERALL BLOCK DIAGRAM OF THE UC1840, AN INTEGRATED CIRCUIT OPTIMIZED FOR PRIMARY-SIDE CONTROL OF OFF-LINE SWITCHING POWER SUPPLIES.

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2. The UC1840 Controller

The overall block diagram of the UC1840, shown in Figure 1, includes the following features:

(1) Fixed-frequency operation set by user-selected components

(2) A variable-slope ramp generator for constant volt-second operation providing open-loop line regulation and minimizing, or in some cases even eliminating, the need for feedback control

(3) A drive switch for low current start-up off the high-voltage line

(4) A precision reference generator with internal over-voltage protection

(5) Complete under-voltage, over-voltage, and over-current protection including programmable shutdown and restart

(6) A high-current, single-ended PWM output optimized for fast turn-off of an external power switch

(7) Logic control for pulse-commandable or DC power sequencing

For an understanding of how these individual blocks work together in a typical, medium-power, flyback power supply, reference should be made to Figure 2 and the functional description which follows.

3. UC1840 Functional Description

3.1 Power Sequencing

A simplified schematic of the UC1840's internal power turn-on circuitry is shown in Figure 3. The key elements of this function are: (1) the Driver Bias Switch, Q3, which keeps the loading on the control voltage line, Vc, to a minimum during start up; (2) the Under-voltage Comparator which also functions as a Start Threshold Detector with programmable hysteresis; and (3) an auxiliary, primary-referenced, low-voltage winding on the main power transformer which provides normal control power after turn-on. The sequence of events is as follows:

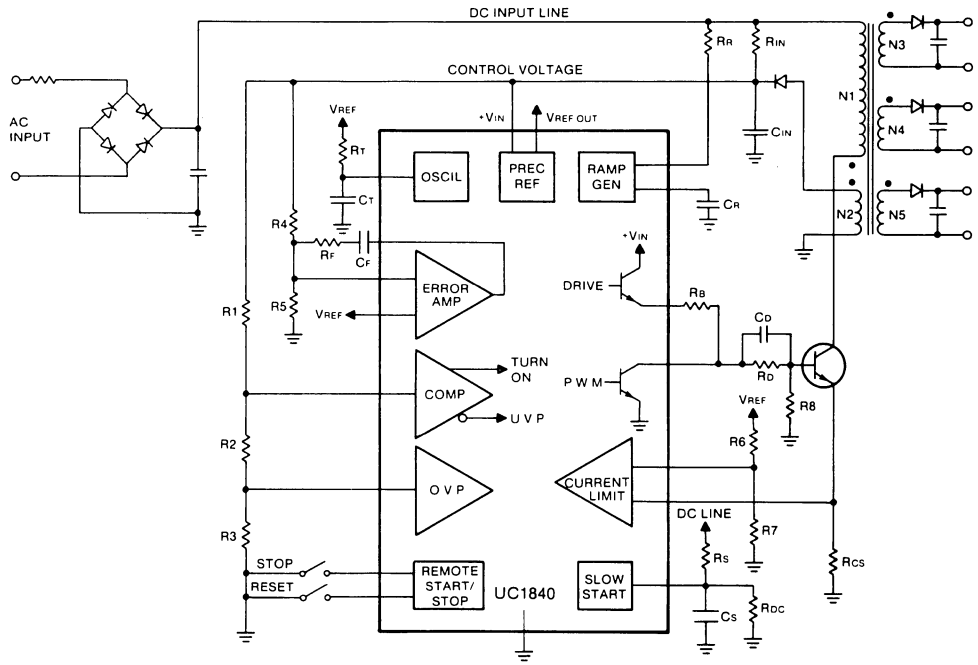


FIGURE 2. A FULLY PROTECTED, ISOLATED FLYBACK POWER SUPPLY CAN BE IMPLEMENTED WITH THE UC1840, A HIGH-VOLTAGE POWER SWITCH, THE TRANSFORMER, AND A SMALL HANDFUL OF PASSIVE COMPONENTS.

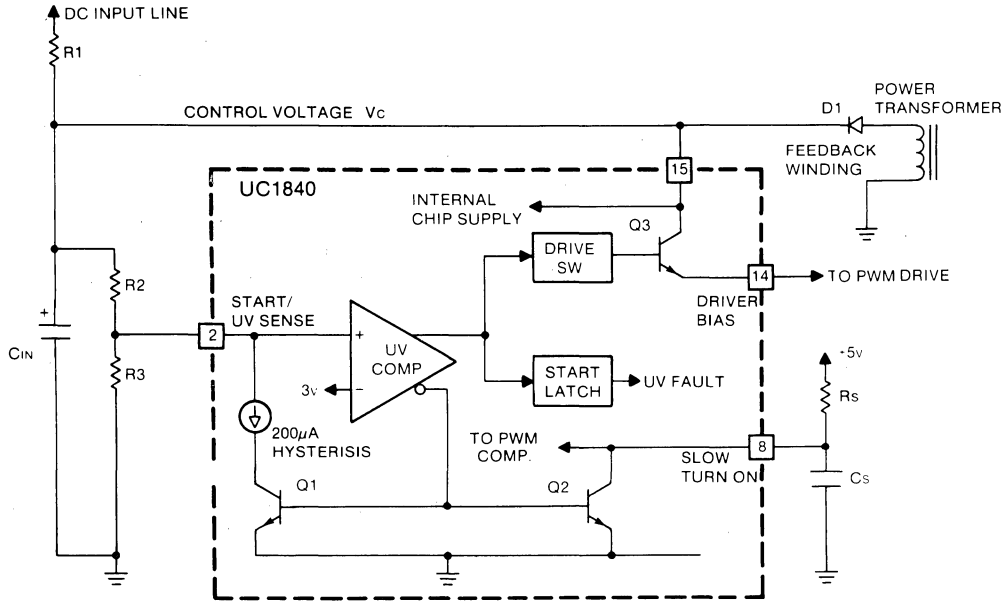


FIGURE 3. THE UC1840's START CIRCUITRY REQUIRES LOW STARTING CURRENT FROM THE DC INPUT LINE WITH NORMAL OPERATING CURRENT SUPPLIED FROM A LOW-VOLTAGE FEEDBACK WINDING ON THE POWER TRANSFORMER.

(1) While the control voltage, Vc, is low enough so that the voltage on pin 2 is less than 3V, the Start/UV Comparator does the following:

(a) A 200μA hysteresis current is flowing into pin 2 through Q1 causing an added drop across R2.

(b) The drive switch is holding the Driver Bias transistor, Q3, OFF. This insures that the only current required through R1 is the start-up current of the UC1840, plus external dividers (R2, R3, Rs, etc.).

(c) The Slow Turn-on transistor, Q2, is ON, holding pin 8 and Cs low.

(d) The Start Latch keeps the under-voltage signal from being defined as a fault.

(2) The start level is defined by:

$$Vc\ (start) = 3\left(\frac{R2 + R3}{R3}\right) + 0.2\ R2.$$

When Vc rises to this level, the Start/UV Comparator then does the following:

(a) Turns off Q1, eliminating the 200μA hysteresis current. This allows the voltage on Vc to drop before reaching the under-voltage fault level defined by:

$$Vc\ (U.V.\ fault) = 3\left(\frac{R2 + R3}{R3}\right)$$

(b) Sets the Start Latch to monitor for an under-voltage fault.

(c) Activates Q3 providing Driver Bias to the power switch, pulling the added current out of Cin.

(d) Turns off Q2 allowing for programmed slow turn-on defined by Rs and Cs.

(3) A normal start-up occurs with the control voltage, Vc, following the path shown in Figure 4. If the power supply does not start, Vc will fall to an under-voltage fault which will then either initiate a restart attempt or hold the power switch off, depending upon

the status of the Reset terminal as defined under Fault Sequencing (Para. 3.4.2). If start-up does not occur because of some fault in the Driver Bias line, Vc will continue to rise until the 40V zener across the reference circuit conducts. This will then clamp Vc to that level, protecting the control chip.

After start-up occurs, current will continue to flow in R1 providing a power loss of:

$$Pd = \frac{(Vline - Vc)^2}{R1}$$

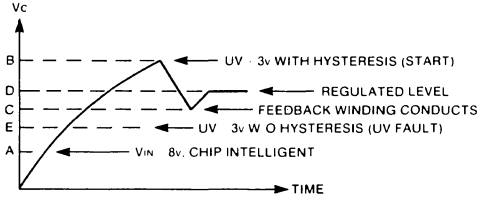


FIGURE 4. UNDER A NORMAL TURN-ON, THE SUPPLY VOLTAGE TO THE UC1840, Vc, WOULD RISE LIGHTLY LOADED TO THE START LEVEL, FALL UNDER THE TURN-ON LOAD, AND THEN REGULATE AT SOME INTERMEDIATE LEVEL.

If this loss is objectionable, it can be reduced more than an order of magnitude by the addition of a two-transistor switch shown in Figure 5. In this circuit, Q1 is initially driven on by current through R2. When the feedback winding starts to conduct through D1, however, Q2 turns on leaving only R2 conducting from the input line.

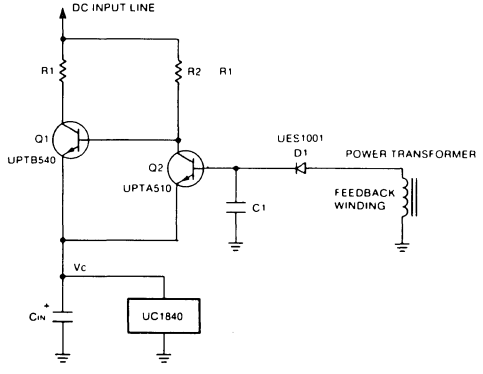


FIGURE 5. THE ADDITION OF Q1 AND Q2 CAN ELIMINATE THE STEADY-STATE CURRENT THROUGH R1 AFTER TURN-ON. Q2 IS SELECTED TO PASS ALL CONTROL CURRENT THROUGH ITS BASE-EMITTER JUNCTION.

3.2 Slow Turn-on Circuit

The PWM comparator input connected to pin 8 accommodates several programming functions, shown in Figure 6. Since this comparator will only follow the lowest positive input, holding pin 8 low will effectively eliminate a PWM signal, regardless of the status of the Error Amplifier output. Prior to turn-on, and at all times when a fault has been sensed, Q1 is ON, holding pin 8 low.

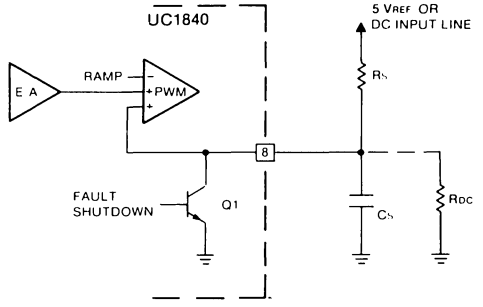


FIGURE 6. PIN 8 ON THE UC1840 CAN BE USED FOR BOTH SLOW TURN-ON AND DUTY-CYCLE LIMITING AS WELL AS A PWM SHUTDOWN PORT.

When Q1 turns off, allowing pin 8 to rise with a controlled rate will cause the output pulses to increase from zero to nominal widths at the same rate. This is accomplished by the addition of Cs and a charging source, such as Rs, to the 5V reference.

Note that where starting energy is stored in an input capacitor, the time for PWM turn-on must be less than the time required for the added Driver Bias load current to discharge the input capacitor to the under-voltage fault level. In other words, referring back to Figure 4, the slow turn-on must be faster than the time required for Vc to fall from level B to level E.

Another function of pin 8 is to establish a maximum duty cycle limit. This is achieved by clamping the voltage on pin 8 with a divider formed by adding Rdc to ground. If Rs is taken to the 5V reference, the clamp voltage will be fixed, which is desirable if the ramp slope is also fixed. If the ramp slope is varied with the input line—for constant volt-second operation—then the clamp voltage on pin 8 must also vary. This is readily accomplished by connecting Rs to the DC input line. The divider voltage:

$$VPin\ 8 = \left(\frac{Rdc}{Rs + Rdc}\right) V\ DC\ input$$

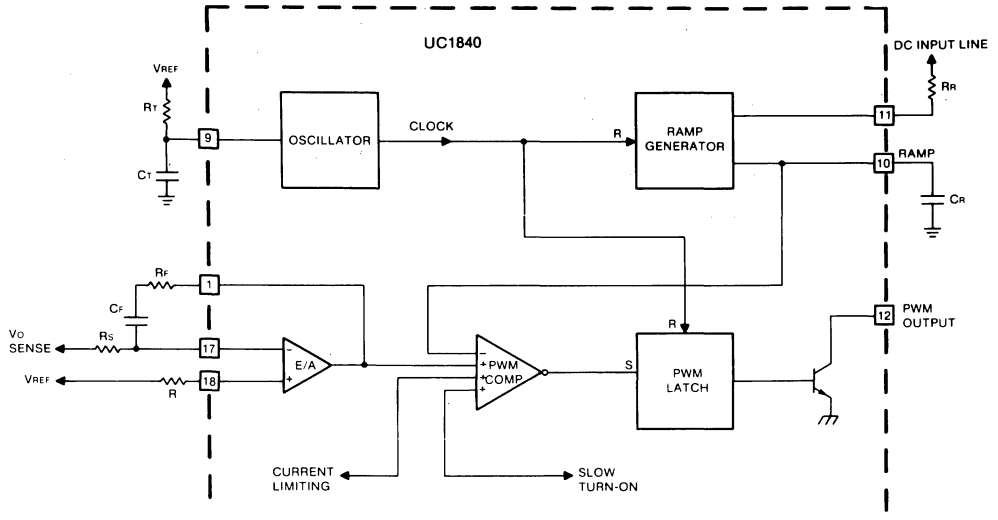


FIGURE 7. THE PULSE-WIDTH MODULATOR WITHIN THE UC1840 SEPARATES THE RAMP FUNCTION FROM THE FIXED-FREQUENCY OSCILLATOR.

should be equal to the ramp voltage level that yields the desired maximum duty cycle, at the same DC input level.

3.3 PWM Control

Pulse-Width Modulation within the UC1840 consists of the blocks shown in Figure 7. This architecture, with the possible exception of the separation between the time-base and ramp functions, is fairly conventional. It is described in greater detail in the paragraphs which follow.

3.3.1 Oscillator

A constant clock frequency is established by connecting Rt from pin 9 to the 5V reference and Ct from pin 9 to ground. The frequency is approximated by:

$$f \approx \frac{1}{Rt\ Ct}$$

where the value of Rt can range from 1kΩ to 100kΩ and Ct from 300pF to 0.1μF. The best temperature coefficients occur with Ct in the range of 1000 to 3000pF. Although the clock output pulse is not available external to the UC1840, synchronization to an external clock can still be accomplished with the circuit of Figure 8, where R1 and C1 are selected to provide a 0.5V, 200ns pulse across the 51Ω resistor, and Rt and Ct define a frequency slightly lower than the synchronizing source.

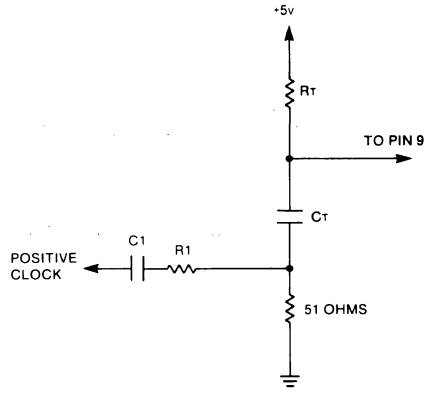


FIGURE 8. SYNCHRONIZATION TO AN EXTERNAL TIME BASE CAN BE ACCOMPLISHED BY ADDING A 51Ω RESISTOR IN SERIES WITH CT.

To achieve minimum start-up current, the oscillator is not activated until the input voltage is high enough to give a start command to the drive switch.

3.3.2. Ramp Generator

The ramp generator function of the UC1840 is shown in simplified form in Figure 9.

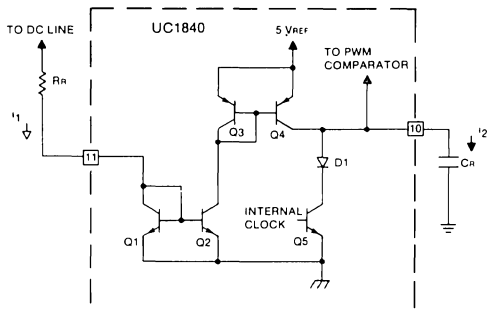


FIGURE 9. CURRENT MIRRORS Q1-Q4 ARE USED TO MAKE THE RAMP CHARGING CURRENT i2, LINEARLY PROPORTIONAL TO THE DC INPUT LINE

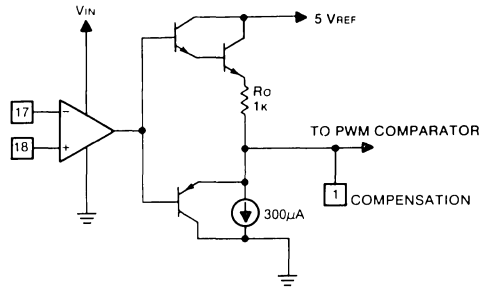


FIGURE 10. THE OUTPUT OF THE ERROR AMPLIFIER OPERATES CLASS A TO 300μA, BUT CAN SOURCE AND SINK MORE THAN 1 mA FOR FAST RESPONSE

The NPN and PNP current mirrors provide a charging current to Cr of:

$$i2 = il = \frac{Vline - 0.7V}{Rr} \simeq \frac{Vline}{Rr}$$

The current mirrors are useful over a current range of 1μA to 1mA, but optimum tracking occurs between 30μA and 300μA. Since the voltage across Q1 is very small, i2 accurately represents the input line voltage. The ramp slope, therefore, is:

$$\frac{dv}{dt} = \frac{Vline}{Rr\ Cr}$$

The peak voltage across Cr is clamped to approximately 4.2V while the valley, or low voltage, is determined by the on-voltage of the discharge network, D1 and Q5. This is typically 0.7V.

If line sensing is not required, Rr should be connected to the 5V reference for constant ramp slope.

3.3.3 Error Amplifier

This is a voltage-mode operational amplifier with an uncommitted NPN differential input stage and an output configuration as shown in Figure 10.

The 1kΩ output resistor, Ro, is used both for short circuit protection and to limit the peak output voltage to less than 4.0V so it cannot rise above the clamped ramp waveform. At sink currents less than 300μA, the low output level will be within 200mV of ground but it rises to 1V at higher current levels.

The input common mode range is from 1V to within 2V of the input supply voltage, Vin, and thus either input can be connected directly to the 5V reference.

The small signal, open-loop gain characteristics are shown in Figure 11. The amplifier is unity-gain stable and has a maximum slew rate of just under 1V/μs.

3.3.4 PWM Comparator and Latch

This comparator (see Figure 7) generates the output pulse which starts at the termination of the clock pulse and ends when the ramp waveform crosses the lowest of the three positive inputs. The clock forms a blanking pulse which keeps the maximum duty cycle less than 100%. The PWM latch insures there will be only one pulse per period and eliminates oscillation at comparator cross-over.

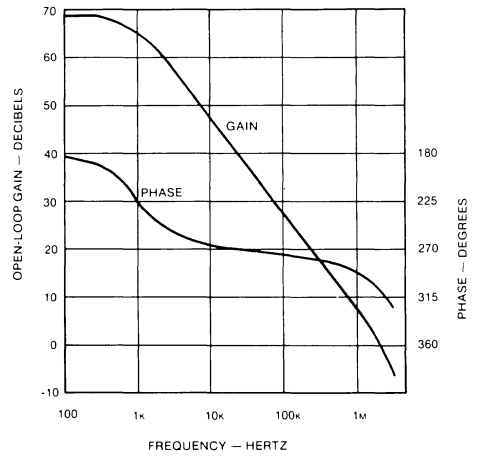


FIGURE 11. THE UC1840 ERROR AMPLIFIER HAS A DC GAIN OF 67 db, A 2 MEGAHERTZ BANDWIDTH, AND PHASE MARGIN OF APPROXIMATELY 45°

3.3.5 PWM Output Stage

In addition to the PWM output signal on pin 12, the UC1840 also includes an output gating, or arming function as Driver Bias on pin 14. Both functions should be considered together in interfacing to the external high-voltage power switch. These are illustrated in simplified form in Figure 12.

At very low input voltages (Vin < 3V), both Q2 and Q4 are OFF. This may necessitate the use of R2, but its value can be high since it does not have to turn the output switch off. It merely holds it in the off state during the early portion of start-up.

Between Vin = 3V and the start threshold (pin 2 = 3V with hysteresis on), Q2 is OFF and Q4 is ON, clamping the power switch off with a low impedance. A start command (UV high) turns on Q2, applying (Vin - 2V) to R1. This provides a source for power switch activation; however, since Q4 is still conducting, the current through R1 is shunted to ground and the power switch remains held off.

At the same time Q2 turns on, the clamping transistor at the slow-start terminal, pin 8, turns off allowing the voltage on pin 8 to rise according to the external slow-start time constant described earlier. This allows PWM pulses to begin to activate Q4—narrow at first and widening to the point where the error amplifier takes command.

The interface between the UC1840 and the primary power switch may be implemented in several different ways to meet varying system requirements. One obvious application is when the use of a bipolar transistor switch requires more drive current than the Driver Bias output can provide. Figure 13 shows a more typical bipolar drive scheme where Q5 has been added to boost the turn-on current with the UC1840 still providing the high-speed turn-off. The circuit now serves as a more efficient "totem-pole" driver since Q5 turns off when Q4 conducts. It also illustrates the use of a Baker Clamp to minimize storage time in Q6 and the capacitors for rapid turn-on and high-current pulse turn-off.

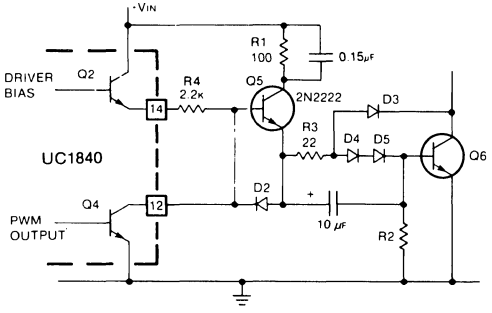


FIGURE 13. ADDING Q5 AS A SWITCHED, DRIVE-BOOST TRANSISTOR PROVIDES ADDED BASE DRIVE FOR Q6 WHILE REDUCING THE STEADY-STATE CURRENT THROUGH BOTH Q2 AND Q4.

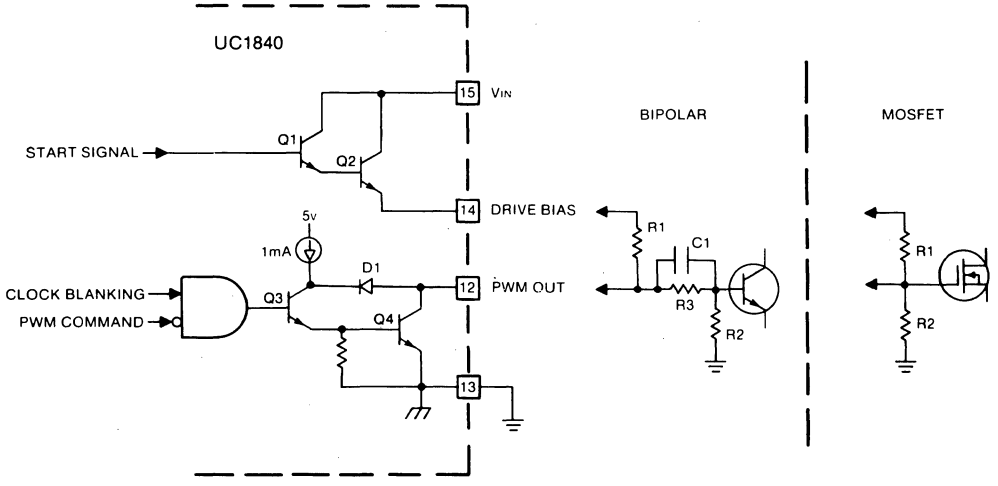


FIGURE 12. INTERFACING THE UC1840 PWM OUTPUT STAGE TO EITHER BIPOLAR OR POWER MOSFET SWITCHES.

Another application is the two-transistor, off-line, forward converter topology shown in Figure 14. This circuit uses proportional base drive where the UC1840 need only supply a short, turn-off current pulse with transformer regeneration through T1 providing the steady-state drive. The magnetizing current is controlled by R1, with Q5 added to rapidly recharge C1 from which the turn-off current is supplied.

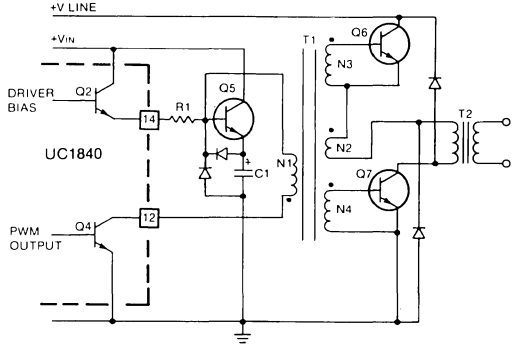


FIGURE 14. INTERFACING THE UC1840 SINGLE PWM OUTPUT TO A TWO-TRANSISTOR OFF-LINE FORWARD CONVERTER WHICH USES PROPORTIONAL BASE DRIVE.

3.4 Fault Protection

A significant benefit in using the UC1840 is the multi-faceted fault-sensing and programming capability built into the device. With the intent to provide complete control to the power system under all types of potential malfunctions, fault-sensing circuitry has been included to sense over-voltage, under-voltage, or over-current conditions. Additionally, high-speed, pulse-by-pulse digital current limiting is included as a separate function. The operation of these circuits is described below.

3.4.1 Current Limiting

The current limit comparators have differential inputs for noise rejection but are intended to be used with ground-referenced current sensing as in Figure 15. Comparator A1 is delegated to pulse-by-pulse current limiting. The output of this comparator drives the PWM comparator, where it activates the PWM latch, terminating each pulse when the current sensed by Rsc reaches a threshold defined by divider R1, R2, and the 5V reference. Since Vc is intended to track the supply's output voltage, the addition of a resistor from pin 6 to Vc will provide some foldback to the current limit characteristic. Since comparator A1 has zero offset

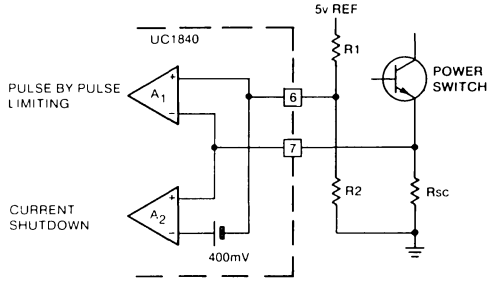


FIGURE 15. CURRENT LIMITING AND OVERCURRENT SHUTDOWN ARE IMPLEMENTED WITH COMPARATORS OF DIFFERENT THRESHOLDS AND A SINGLE CURRENT SENSE RESISTOR.

voltage, it is activated when the voltage across Rsc equals that across R2. Comparator A2, with an offset voltage of 400mV, will activate for over-current shutdown when the voltage across Rsc rises to 400mV higher than the voltage across R2. Since the input bias to both comparators is less than 5μA, a low-pass filter for noise rejection may be inserted between Rsc and the sense inputs. Activation of comparator A2 is defined as an over-current fault and it triggers the Error Latch. Its operation follows.

3.4.2 Fault Sequencing

The fault sequencing logic of the UC1840 is shown in Figure 16. Since a fault is defined by this device as an activation of the Error Latch, it makes sense to start here in an attempt to understand this portion of the circuitry. Setting the Error Latch immediately turns on Q1 and Q2, discharging the slow-start capacitor and terminating the PWM output. Note that there is an additional path from the inverted output of the Start/UV comparator through OR2 which keeps pin 8 low. This is to keep the slow-start low during initial turn-on which is not intended to be classified as a fault.

The input to the Error Latch is from OR1 which triggers on signals resulting from four possible events:

(1) A voltage less than 3V (after prior turn-on) at the Start/UV sense terminal, pin 2

(2) A voltage greater than 3V at the Over-Voltage Sense terminal, pin 3

(3) A voltage of less than 3V on the Ext. Stop terminal, pin 4

(4) An over-current signal resulting in a differential voltage between pins 7 and 6 of greater than 400mV

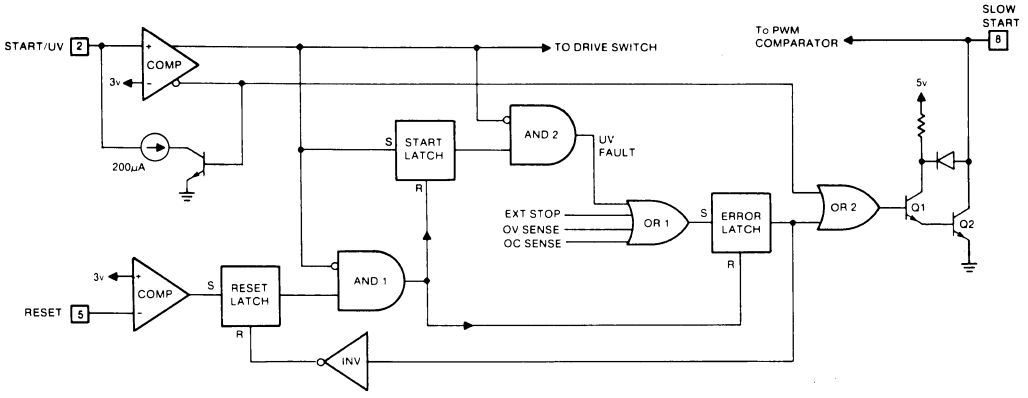


FIGURE 16. FAULT SEQUENCE LOGIC IS DESIGNED TO INSURE A COMPLETE SHUTDOWN AND FULLY CONTROLLED RESTART UPON ANY OF FOUR POSSIBLE FAULT CONDITIONS.

Any of these inputs need only be momentary to set the Error Latch. Transient protection may be necessary to eliminate false triggering, but it can be readily accomplished as all the comparator inputs are high impedances requiring less than 2μA of input current, and the 3.0V reference yields a high noise immunity.

The Start Latch can be understood by recognizing that at initial turn-on it is reset with a low output. This prevents AND2 from transmitting a UV fault signal from the Start/UV non-inverting output to the Error Latch. At the start voltage level, defined by a high level on the Start/UV non-inverting ouput, the Start Latch sets but AND2 still provides no output. Only when the Start/UV input goes low again, with the Start Latch output held high, will AND2 yield an output into the Error Latch.

The status of the Reset terminal, pin 5, determines what happens after the Error Latch is set. The choices are:

(1) Latch off and require a recycle of input voltage to restart
(2) Continuously attempt to restart
(3) Attempt some number of restarts and then latch off
(4) Latch off and await a momentary reset pulse to restart

To examine the operation of the Reset Latch, note that prior to setting the Error Latch, its low output is inverted to hold the reset input to the Reset Latch high. This forces the Reset Latch's ouput low, regardless of the voltage on pin 5, and, thus, insures no signal out of AND1. With the setting of the Error Latch, the Reset Latch is free to take the state commanded by pin 5: high if pin 5 is low and vice-versa. The latch allows merely a pulse to set the Reset Latch; the voltage on pin 5 need not be steady state.

With a high Reset Latch output, the Error Latch still does not reset until a low signal is sensed on the Start/UV sense terminal. At that point, AND1 then resets both the Error Latch and the Start Latch, re-establishing the initial conditions for a normal start after fully charging the input capacitor. Of course, if the fault is still present, when the Start/UV input reaches the start level terminating the Error Latch reset signal, this latch will immediately set again.

To aid in the understanding of this logic, Figure 17 gives a pictorial representation of its operation with both steady-state and momentary signals on both the Ext. Stop and Reset terminals.

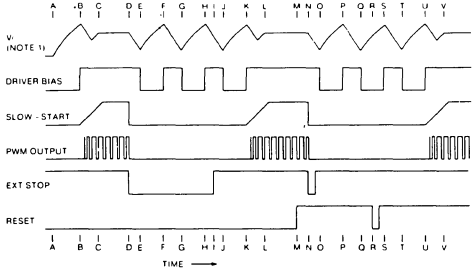
If Driver Bias turn-on is used to pump an increment of charge into an integrating capacitor, and that capacitor voltage is applied to the Reset Terminal, some number of retrys could be programmed to take place before the Reset voltage rises to 3V, which would then lock the output OFF. Since Driver Bias continues to cycle in the latched-off state, the Reset terminal will remain high until it is either remotely pulled low or the input voltage to the controller is interrupted.

Note that an important element in any restart after a shutdown is the lowering of the voltage at the Start/UV terminal below its UV threshold. While this will occur normally in bootstrap-driven applications, this device can also be used with a con-

stant driving voltage by externally applying a momentary pull-down signal to the Start/UV input after a fault shutdown.

4. Conclusion

With the UC1840, power supply designers now have a device specifically developed for off-line, primary control and one which has addressed the problems of operation under less than "ideal" or normal conditions. Not only does this device make it easier to comply with stringent isolation requirements by requiring a minimum of communication between primary and secondary, but it is also ideally suited for powering systems in remote locations where only a simple transmitted pulse is available for power sequencing.



NOTE 1: Vc REPRESENTS AN ANALOG OF THE SUPPLY OUTPUT VOLTAGE GENERATED BY A PRIMARY-REFERENCED SECONDARY WINDING ON THE POWER TRANSFORMER. IT IS THE VOLTAGE MONITORED BY THE START/UV COMPARATOR AND, IN MOST CASES, IS THE SUPPLY VOLTAGE, VIN, FOR THE UC1840.

TIME	EVENT
A	INITIAL TURN-ON. Vc RISES WITH LIGHT LOAD.
B	START THRESHOLD. DRIVER BIAS LOADS Vc.
C	OPERATING PWM REGULATES Vc.
D	STOP INPUT SETS. ERROR LATCH TURNING OFF PWM.
E	UV LOW THRESHOLD. ERROR LATCH REMAINS SET.
F	START TURNS ON DRIVER BIAS BUT ERROR LATCH STILL SET.
G	Vc AND DRIVER BIAS CONTINUE TO CYCLE.
H	
I	STOP COMMAND REMOVED.
J	ERROR LATCH RESET AT UV LOW THRESHOLD.
K	START THRESHOLD NOW REMOVES SLOW-START CLAMP.
L	RETURN TO NORMAL RUN STATE.
M	RESET LATCH SET SIGNAL REMOVED.
N	ERROR LATCH SET WITH MOMENTARY FAULT.
O	ERROR LATCH DOES NOT RESET AS RESET LATCH IS RESET.
P	Vc AND DRIVER BIAS RECYCLE WITH NO TURN-ON.
Q	
R	RESET LATCH IS SET WITH MOMENTARY RESET SIGNAL.
S	Vc MUST COMPLETE CYCLE TO TURN ON.
T	START AND ERROR LATCHES RESET.
U	NORMAL START INITIATED.
V	RETURN TO NORMAL RUN STATE.

FIGURE 17. THE INTERRELATIONSHIP BETWEEN THE FUNCTIONS CONTROLLED BY THE FAULT SEQUENCE LOGIC IS ILLUSTRATED WITH BOTH STATIC AND PULSE COMMANDS ON THE EXT. STOP AND RESET TERMINALS.

A NEW INTEGRATED CIRCUIT FOR CURRENT-MODE CONTROL

Abstract

The inherent advantages of current-mode control over conventional PWM approaches to switching power converters read like a wish list from a frustrated power supply design engineer. Features such as automatic feed forward, automatic symmetry correction, inherent current limiting, simple loop compensation, enhanced load response, and the capability for parallel operation all are characteristics of current-mode conversion. This paper introduces the first control integrated circuit specifically designed for this topology, defines its operation and describes practical examples illustrating its use and benefits.

1.0 Introduction

Over the past several years an increased interest in current-mode control of switching inverters has surfaced in the literature. Originally invented in the late 1960s, this scheme was not publicly reported until 1977[1] and has seen rapid development by many authors to date.[2-6] In short, current-mode control uses an inner or secondary loop to directly control peak inductor current with the error signal rather than controlling duty ratio of the pulse width modulator as in conventional converters. Practically, this means that instead of comparing the error voltage to a voltage ramp, it is compared to an analogue of the inductor current forcing the peak current to follow the error voltage.

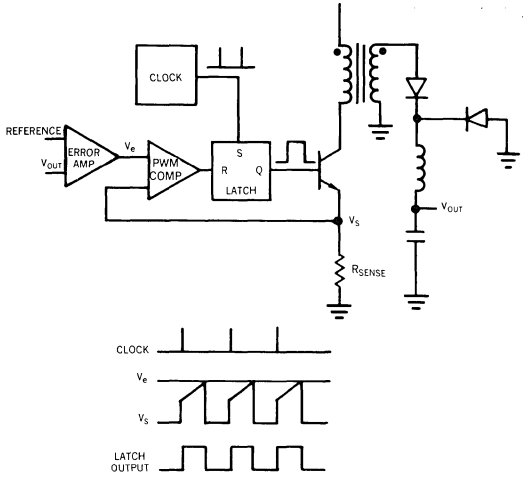


FIGURE 1. A FIXED FREQUENCY CURRENT-MODE CONTROLLED REGULATOR.

Figure 1 illustrates a simplified block diagram of a fixed frequency buck regulator employing current-mode control. As shown, the error signal, V_e, is controlling peak switch current which, to a good approximation, is proportional to average inductor current. Since the average inductor current can change only if the error signal changes, the inductor may be replaced by a current source, and the order of the system reduced by one. This results in a number of performance advantages including improved transient response, a simpler, more easily designed control loop, and line regulation comparable to conventional feed-forward schemes. Peak current sensing will automatically provide flux balancing thereby eliminating the need for complex balance schemes in push-pull systems. Additionally, by simply limiting the peak swing of the error voltage V_e, instantaneous peak current limiting is accomplished. Lastly, by feeding identical power stages with a common error signal, outputs may be paralleled while maintaining equal current sharing.

Although the advantages of current-mode control are abundant, wide acceptance of this technique has been hampered by a lack of suitable integrated circuits to perform the associated control functions. This paper introduces a new integrated circuit designed specifically for control of current-mode converters. Circuit function and features are described in detail, and a comparative design example is used to illustrate the numerous advantages of this approach.

2.0 UC1846 Chip Architecture

In addition to all the functions required of conventional PWM controllers, a current-mode controller

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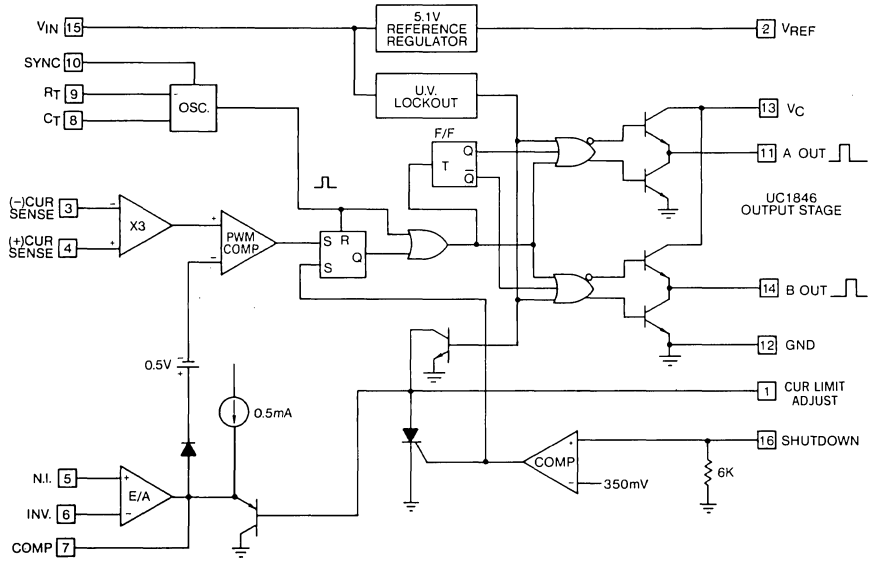


FIGURE 2. UC1846 BLOCK DIAGRAM

must be able to sense switch or inductor current and compare it on a pulse-by-pulse basis with the output of the error amplifier. As may be seen in the block diagram of Figure 2, this is accomplished in the UC1846 by using a differential current sense amplifier with a fixed gain of 3. The amplifier allows sensing of low level voltages while maintaining high noise immunity. A list of other features, while not unique to current-mode conversion, demonstrates the advanced, state-of-the-art architecture of the UC1846:

- A ± 1%, 5.1V trimmed bandgap reference used both as an external voltage reference and internal regulated power source to drive low level circuitry.
- A fixed frequency sawtooth oscillator with variable deadtime control and external synchronization capability. Circuitry features an all NPN design capable of producing low distortion waveforms well in excess of 1MHz .
- An error amplifier with common mode range from ground to V_{CC}-2V.
- Current limiting through clamping of the error signal at a user-programmed level.
- A shutdown function with built in 350mV threshold. May be used in either a latching, or non-latching mode. Also capable of initiating a "hiccup" mode of operation.
- Under-voltage lockout with hysteresis to guarantee outputs will stay "off" until reference is in regulation.
- Double pulse suppression logic to eliminate the possibility of consecutively pulsing either output.
- Totem pole output stages capable of sinking or sourcing 100mA continuous, 400mA peak currents.

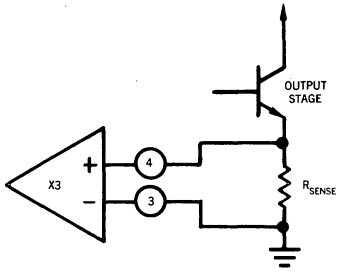
These various features, along with their interrelationships and applications to switched-mode regulators, will be further discussed in the following sections.

3.0 UC1846 Functional Description

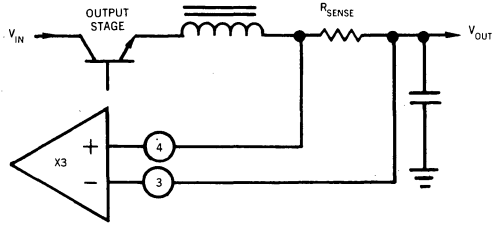
3.1 Current Sense Amplifier

The current sense amplifier may be used in a variety of ways to sense peak switch current for comparison with an error voltage. Referring to Figure 2, maximum swing on the inverting input of the PWM comparator is limited to approximately 3.5V by the internal regulated supply. Accordingly, for a fixed gain of 3, maximum differential voltages must be kept below 1.2V at the current sense inputs. Figure 3 depicts several methods of configuring sense schemes. Direct resistive sensing is simplest, however, a lower peak voltage may be required to minimize power loss in the sense resistor. Transformer coupling can provide isolation and increase effi-

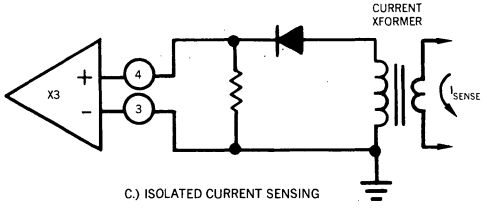
ciency at the cost of added complexity. Regardless of scheme, the largest sense voltage consistent with low power losses should be chosen for noise immunity. Typically, this will range from several hundred millivolts in some resistive sense circuits to the maximum of 1.2V in transformer coupled circuits.



A.) RESISTIVE SENSING WITH GROUND REFERENCE



B.) RESISTIVE SENSING ABOVE GROUND



C.) ISOLATED CURRENT SENSING

FIGURE 3. VARIOUS CURRENT SENSE SCHEMES

In addition, caution should be exercised when using a configuration that senses switch current (Figure 3A) instead of inductor current (Figure 3B). As the switch is turned on, a large instantaneous current spike can be generated in the sense resistor as the collector capacitance of the switch is discharged. This spike will often be of sufficient magnitude and duration to trip the current sense latch and result in erratic operation of the PWM circuit, particularly at lower duty cycles. A small RC filter (Figure 4) in series with the input is generally all that is required to reduce the spike to an acceptable level.

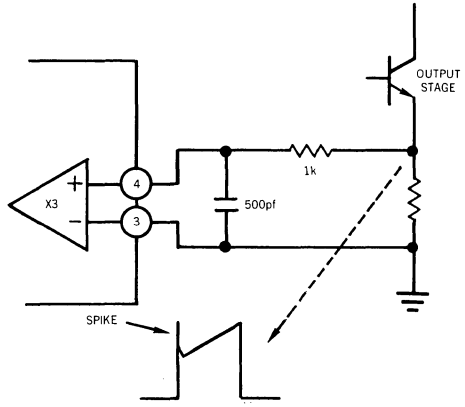


FIGURE 4. RC FILTER FOR REDUCING SWITCH TRANSIENTS

3.2 Oscillator

Although many data sheets tout 300 to 500kHz operation, virtually all PWM control chips suffer from both poor temperature characteristics and waveform distortions at these frequencies. Practical usage is generally limited to the 100 to 200kHz range. This is a direct consequence of having slow (f_t = 2MHz) PNP transistors in the oscillator signal path. By implementing the oscillator using all NPN transistors, the UC1846 achieves excellent temperature stabillity and waveform clarity at frequencies in excess of 1MHz.

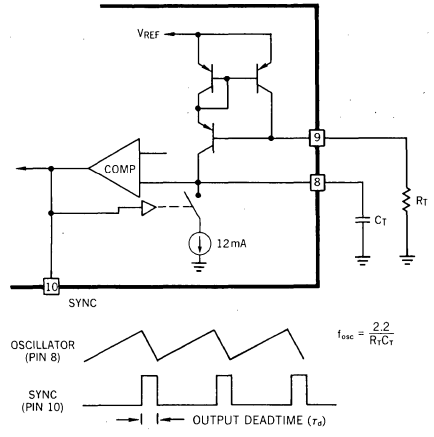


FIGURE 5. OSCILLATOR CIRCUIT

Referring to Figure 5, an external resistor R_T is used to generate a constant current into a capacitor C_T to

produce a linear sawtooth waveform. Oscillator frequency may be approximated by selecting R_T and C_T such that:

$$f_{osc} = \frac{2.2}{R_T C_T} \quad (1)$$

Where R_T can range from 1K to 500K and C_T is above 100pF. For quick reference a plot of frequency versus R_T and C_T is given in Figure 6.

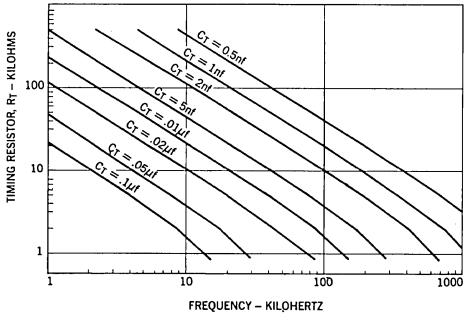


FIGURE 6. OSCILLATOR FREQUENCY AS A FUNCTION OF R_T AND C_T

Again referring to Figure 5, the oscillator generates an internal clock pulse used, among other things, to blank both outputs and prevent simultaneous cross conduction during switching transitions. This output "deadtime" is controlled by the oscillator fall time. Fall time, in turn, is controlled by C_T according to the formula:

$$\tau d = 145\ C_T \left[\frac{12}{12 - 3.6/R_T(k\Omega)}\right] \quad (2)$$

For large values of R_T:

$$\tau d = 145\ C_T \quad (3)$$

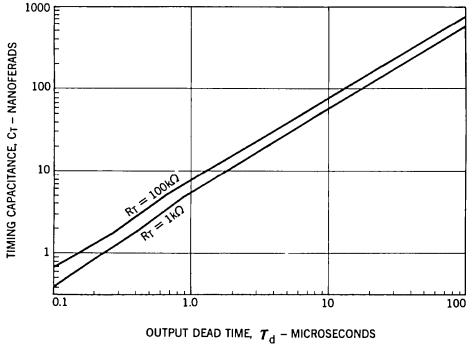


FIGURE 7. OUTPUT DEADTIME AS A FUNCTION OF TIMING CAPACITOR C_T

A plot of output deadtime versus C_T for two values of R_T is given in Figure 7.

Although timing capacitors as small as 100pF can be used successfully in low noise environments, it is generally recommended that C_T be kept above 1000pF to minimize noise effects on the oscillator frequency (see Section 4.0).

Synchronization of one or more devices to either an external time base or another UC1846 is accomplished via the bi-directional SYNC pin. To synchronize devices, first, C_T must be grounded to disable the internal oscillator on all slaved devices. Second, an external synchronization pulse must be applied to the SYNC terminal. This pulse can come directly from the SYNC terminal of a master UC1846 or, alternatively, from an external time base as shown in Figure 8.

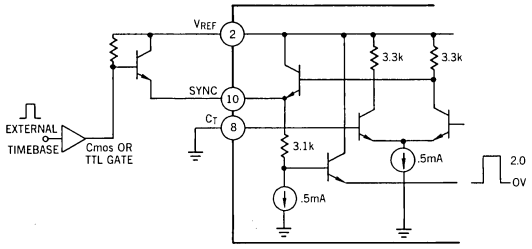


FIGURE 8. SYNCHRONIZING THE 1846 TO AN EXTERNAL TIME BASE

3.3 Current Limit

One of the most attractive features of a current-mode converter is its ability to limit peak switch currents on a pulse-by-pulse basis by simply limiting the error voltage to a maximum value. Referring to Figure 9, peak current limiting in the UC1846 is accomplished using a divider network, R_1 and R_2, to set a pre-determined voltage at pin 1.

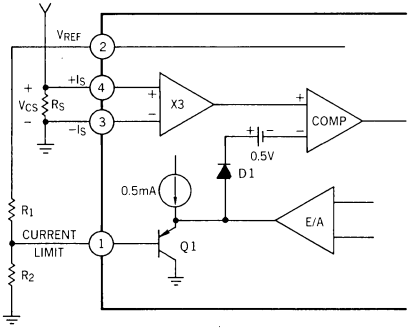


FIGURE 9. PEAK CURRENT LIMIT SET UP

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This voltage, in conjunction with Q_1, acts to clamp the output of the error amplifier at a maximum value. Since the base emitter drop of Q_1 and the forward drop of diode D_1 very nearly cancel, the negative input of the comparator will be clamped at the value $V_{PIN\ 1}$ −0.5V. Following this through to the input of the current sense amplifier yields:

$$V_{cs} = \frac{V_{PIN\ 1} - 0.5}{3} \quad (4)$$

Where V_{cs} is the differential input voltage of the current sense amplifier. Using this relationship, a value for maximum switch current in terms of external programming resistors can be derived, resulting in:

$$I_{CL} = \frac{\frac{R_2\ (V_{REF})}{R_1 + R_2} - 0.5}{3R_S} \quad (5)$$

While still on the subject of resistor selection, it should be pointed out that R_1 also supplies holding current for the shutdown circuit, and therefore should be selected prior to selecting R_2 as outlined in the next section.

One last word on the current limit circuit. As may be seen from equation 5, any signal less than 0.5V at the current limit input will guarantee both outputs to be off, making pin 1 a convenient point for both shutting down and slow starting the PWM circuit. For example, both the under-voltage lockout and shutdown functions are connected internally to this point. If a capacitor is used to hold pin 1 low (Figure 10) then as the input voltage increases above the under-voltage lockout level, the capacitor will charge and gradually increase the PWM duty cycle to its operating point. In a similar manner if the shutdown amplifier is pulsed, the shutdown SCR will be fired and the capacitor discharged, guaranteeing a shutdown and soft restart cycle independent of input pulse width.

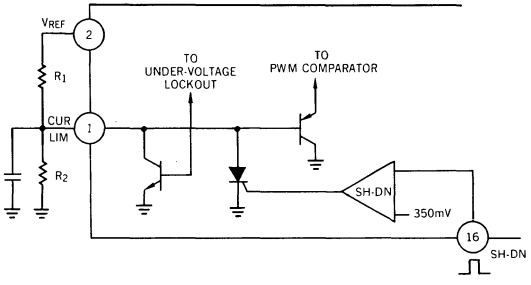

FIGURE 10. USING UNDER-VOLTAGE LOCKOUT AND SHUTDOWN TO INITIATE A SLOW START.

3.4 Shutdown

The shutdown circuit, shown in Figure 11, was designed to provide a fast acting general purpose shutdown port for use in implementing both protection circuitry and remote shutdown functions. The circuit may be divided into an input section consisting of a comparator with a 350mV temperature compensated offset, and an output section consisting of a three transistor latch. Shutdown is accomplished by applying a signal greater than 350mV to pin 16, causing the output latch to fire, and setting the PWM latch to provide an immediate signal to the outputs. At this point, several things can happen. Q_1 requires a minimum holding current, I_H, of approximately 1.5mA to remain in the latched state. Therefore, if R_1 is chosen greater than 5kΩ, Q_1 will discharge any capacitance, C_S, on pin 1 to ground and commutate the output latch, allowing C_S to recharge. If R_1 is chosen less than 2.5kΩ, Q_1 will discharge C_S and remain in the latched state until power is externally cycled off. In either case, C_S is required only if a soft-start or soft-restart function is desired.

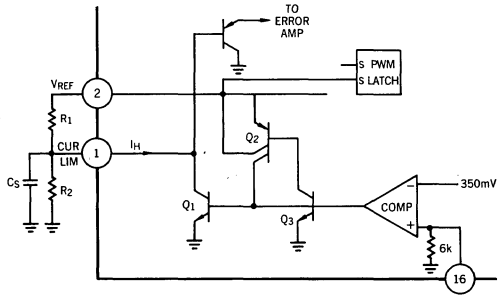

FIGURE 11. SHUTDOWN CIRCUITRY

For example, the shutdown circuit of Figure 12, operating in a nonlatched mode, will protect the supply from overcurrent fault conditions. Many times, if the output of a supply is shorted, circulating currents in the output inductor will build to dangerous levels. Pulse-by-pulse current limiting with its inherent time delay, will in general not be able to limit these currents to acceptable levels. Figure 12 details a circuit which will provide shutdown and soft-restart if the overcurrent threshold set by R_3 and R_4 is exceeded. This level should be greater than the peak current limit value determined by R_1 and R_2 (see equation 5). Sometimes called a "hiccup mode", this overcurrent function will limit both power and peak current in the output stages until the fault is removed.

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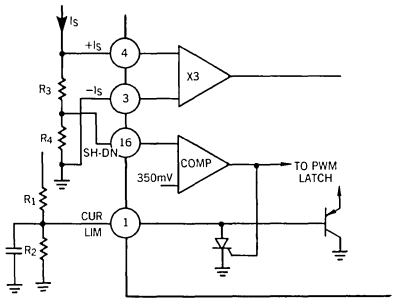


FIGURE 12. OVER CURRENT SENSING WITH THE SHUTDOWN CIRCUIT PRODUCES A SHUTDOWN — SOFT RESTART CYCLE TO PROTECT OUTPUT DRIVERS

4.0 Noise Immunity

As in all PWM circuits, some simple precautions should be observed to prevent switching noise from prematurely triggering the oscillator as it approaches its upper threshold. This is most evident when large capacitive loads — such as the gates of power FETS — are directly driven from outputs A and B. As the duty cycle approaches 100%, the current spike associated with this output capacitance can cause the oscillator to prematurely trigger with a resulting shift upward in frequency. By separating high current ground paths from low level analog grounds, using C_T values greater than 1000pF grounded directly to pin 12, and decoupling both V_{IN} and V_{REF} with good quality bypass capacitors, noise problems can be avoided.

5.0 Comparative Design Example

To more vividly illustrate the advantages of current-mode control, a relatively simple push-pull forward converter was designed using two interchangeable control sections, as shown in Figure 13. The control modules consist of (a) a UC1846 current-mode controller with associated circuitry, and (b) a conventional UC1525A PWM controller with its support circuitry. Loop compensation of the UC1525A was implemented by placing a zero in the feedback loop to cancel one of the poles in the output stage, resulting in a unity gain bandwidth of approximately 3kHz — a commonly used technique. Compensating the current-mode converter requires somewhat of a different approach. Since the output stage contains only a single pole, in theory closing the loop will produce a stable system with no additional compensation. In practice, however, it has been shown that subharmonic oscillation will result from excess gain at half the switching frequency[5]. Therefore, a pole-zero combination has been placed in the feedback loop to reduce high frequency gain and allow the output capacitor (low ESR) to roll off loop gain to 0dB at 3kHz.

While not demonstrated in Figure 13, fixed frequency current-mode converters are known to be unstable above 50% duty cycle without some form of slope compensation[4-6]. By injecting a small current from the sawtooth oscillator into the positive terminal of the current sense amplifier, slope compensation is accomplished, and the converter can be operated in excess of 50% duty cycle. An alternate, but just as effective, scheme would be to inject the signal into the negative terminal of the error amplifier.

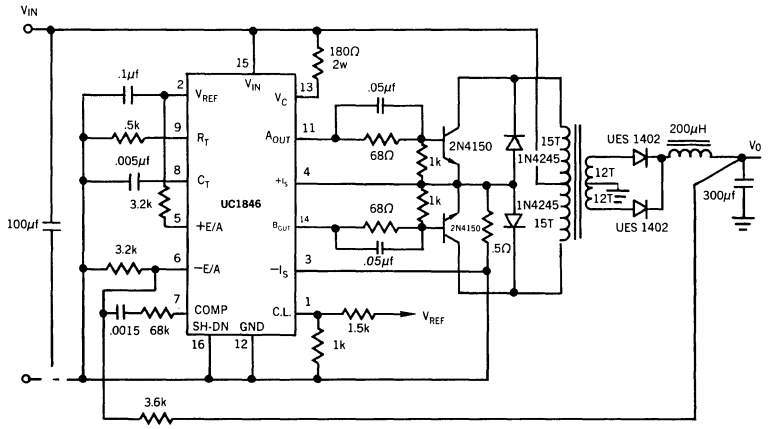
As may be seen, a similar parts count for both supplies was encountered. Topologically, using the UC1525A shutdown terminal provided only a crude current limit in contrast to the UC1846. Furthermore, internal double pulse suppression circuitry of the UC1846 gave an added level of protection against core saturation — important if your regulator is prone to subharmonic oscillations. Since both regulators were over-designed to withstand a short circuit on the output with resultant high peak currents, the shutdown-restart mode of the UC1846 was not used.

It should be pointed out at this time that one of the main features of a current-mode converter of this type is its ability to be paralleled with similar units. By disabling the oscillator and error amplifiers (C_T grounded, +E/A to V_{REF}, -E/A grounded) of one or more slave modules, and connecting SYNC and COMP pins of the slave(s) respectively, the outputs may be connected together to provide a modular approach to power supply design.

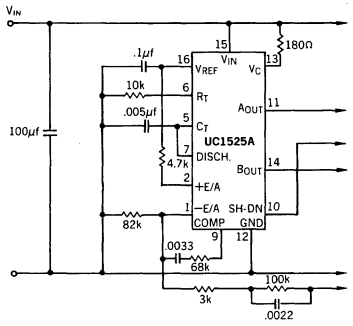
Starting with Figure 14, a comparison of line and load step responses is made between the two converters. As a result of the feed-forward effect of the current-mode converter, response to a step input change shows more than an order of magnitude improvement (Figure 14a) when compared to the conventional converter (Figure 14b). Although not as pronounced, response to a step load change leaves the UC1846 converter (Figure 15) with a clear advantage in output response — 40mV as compared to 70mV for the UC1525A.

Virtually all conventional push-pull converters are prone to flux imbalance caused by mismatched storage delays, etc., in the output stage. Figure 16 shows both converters operating with the same power stage. No effort was made to match output devices. As may be seen, there is little noticeable

difference between switch currents of the UC1846. However, the UC1525A — with identical output transistors — shows phase B driving the core close to saturation with 50% more current than phase A.

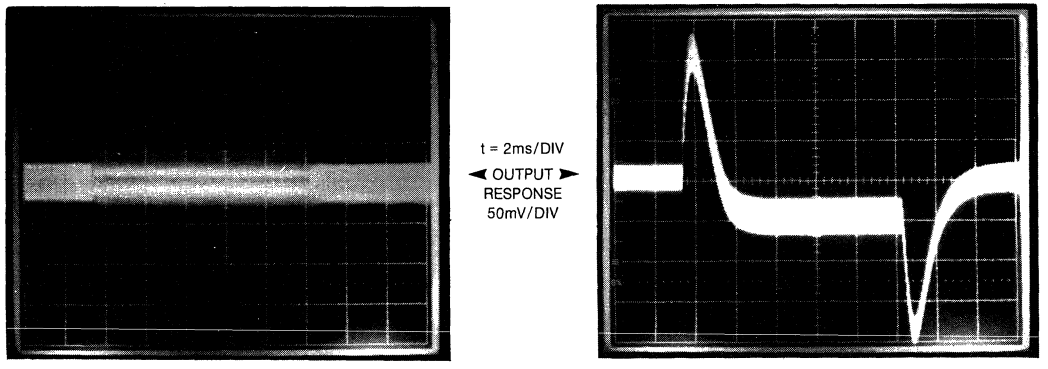


(A) UC1846 CURRENT-MODE CONTROLLED REGULATOR



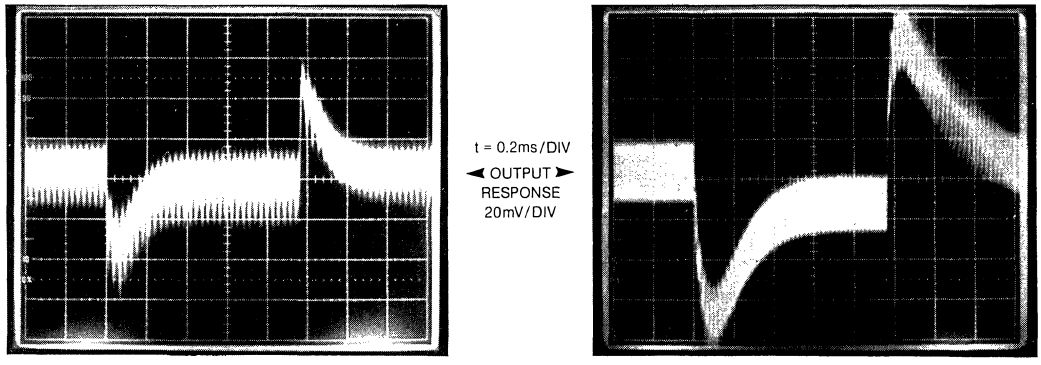
(B) UC1525A VOLTAGE MODE CONTROLLER

FIGURE 13. PUSH-PULL FORWARD CONVERTER WITH (A) CURRENT-MODE CONTROL AND (B) VOLTAGE MODE CONTROL



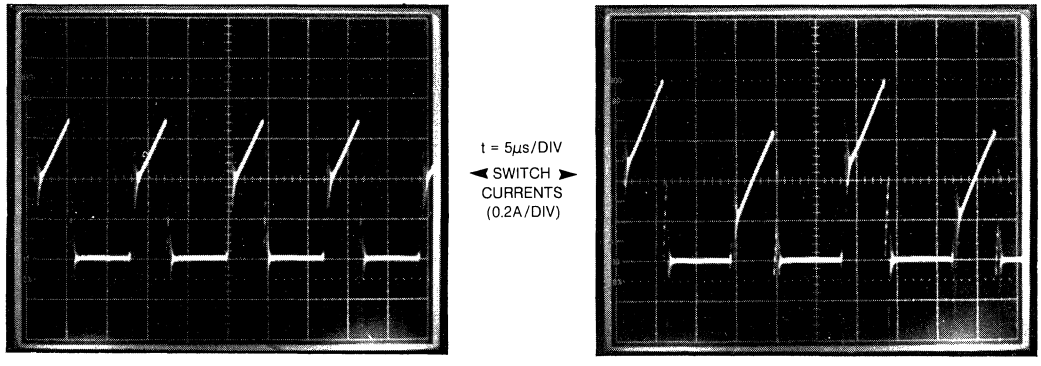
(A) (B)

FIGURE 14. RESPONSE TO A STEP INPUT CHANGE OF 25 TO 35V BY (A) UC1846 and (B) UC1525A CONVERTERS



(A) (B)

FIGURE 15. RESPONSIVE TO A STEP LOAD CHANGE OF 1 AMP BY (A) UC1846 AND (B) UC1525A CONVERTERS



(A) (B)

FIGURE 16. SWITCH CURRENTS SHOWING FLUX IMBALANCE IN (A) UC1846 AND (B) UC1525A CONVERTERS

6.0 Conclusion

Rarely do new design techniques evolve that can promise as much as current-mode control for the power supply engineer. We have shown this to be a simple technique easily extended from present converter topologies, that will increase dynamic performance and provide a higher degree of reliability while permitting new approaches to modular design. Until recently, current-mode converters could not compete with the economics of conventional converters designed with I.C. controllers. Now, with the UC1846 designed specifically for this task, current-mode control can provide all of the above performance advantages on a cost competitive basis.

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THE UC1901 SIMPLIFIES THE PROBLEM OF ISOLATED FEEDBACK IN SWITCHING REGULATORS

1. Introduction

The UC1901 simplifies the task of closing the feedback loop in isolated, primary-side control, switching regulators by combining a precision reference and error amplifier with a complete amplitude modulation system. Using the IC's amplitude modulated output, loop error signals can be transformer coupled across high voltage isolation boundaries, providing stable and repeatable closed-loop characteristics. Coupling across an isolation boundary is nothing new in transformer technology, and the UC1901's ability to generate carrier frequencies of up to 5MHz keeps the transformer size and cost at a minimum. With a secondary reference and accurate coupling path for the feedback signal, isolated off-line supplies can reliably achieve the tolerances, regulation, and transient performance of their non-isolated counter parts and still take advantage of the benefits of primary-side control.

Closing a feedback loop in a simple or complex system requires a thorough understanding of all of the loop elements. Worse case variations of each element must be taken into account when loop stability, dynamic response, and operating point are determined. Unpredictability in any of the loop components will affect the overall design by making it, necessarily, more conservative. The transient response of a control loop, for example, will usually suffer if a loop must be heavily compensated to guarantee stability with component variations.

To obtain high levels of load and line regulation, the output voltage of a power supply must be sensed and compared to an accurate reference voltage. Any error voltage must be amplified and fed back to the supply's control circuitry where the sensed error can be corrected. In an isolated supply, the control circuitry is frequently located on the primary, or line, side of the supply. As shown in Figure 1, the feedback signal in this type of supply must cross the isolation boundary. Coupling this signal requires an element that will withstand the isolation potentials and still transfer the loop error signal. Though some significant drawbacks to their use exist, optical couplers are widely used for this function due to their ability to couple DC signals. Primarily, optocouplers suffer from poor initial tolerance and stability. The gain, or current transfer ratio, through an opto-coupler is loosely specified and changes as a function of time and temperature. This variation will directly affect the overall loop gain of the system, making loop analysis more difficult and the resulting design more conservative. In addition, limited bandwidth capability prevents the use of optical couplers when an extended loop response is required.

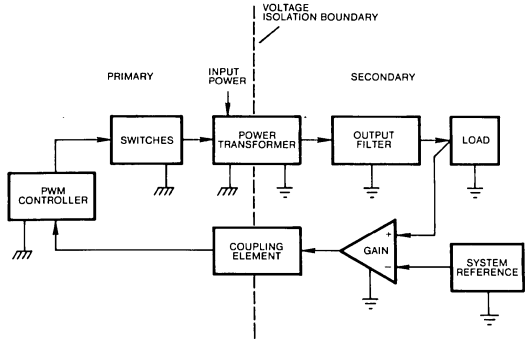

FIGURE 1: A Typical Closed-Loop Isolated Power Supply With Primary-Side Control.

With reliability firmly situated as an important aspect of electrical design, the benefits of primary-side control are increasingly attractive in off-line designs. The organization of an off-line switcher with primary-side control (See Figure 1) puts the control function on the same side of the isolation boundary as the switching elements. Not only does this simplify the interface between the controller and switches, it makes the protection of these switches much easier. Sensing of the switch currents and voltage can avoid failures and improve over-all supply performance. The argument for primary-side control has been further strengthened by the introduction of a new generation of control IC's. The controllers incorporate such features as low current start-up, high speed current sensing for pulse-by-pulse current limiting, and voltage feed-forward. Low current start-up alleviates the problem of efficiently supplying power to a line-side controller, while fast current limit circuitry and voltage feed-forward take advantage of the proximity of a primary-side controller to both the power switch(es) and the input supply voltage.

Combining all of the necessary functions to generate an AM feedback signal on the UC1901 make it the

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first IC of its type. As will be seen, the UC1901 can be used in several modes to take full advantage of its functions. Recognizing the continuing evolution of power converter technology the UC1901 is intended to simplify the design of a new era of reliable and higher performance power converters.

2. The UC1901 Functions

The operation of the UC1901 is best undestood by considering a typical application. In Figure 2, the UC1901 is shown providing the feedback signal to close the loop in an isolated switching power supply. With any feedback system it is desirable to compare the system output to the system reference with a minimum of intermediate circuitry. With the UC1901 situated on the secondary, or output side of the supply, the output voltage is simply divided down and compared to the 1.5V reference using the chip's high gain error amplifier. In this manner DC errors at the supply output are kept minimal even if significant non-linearities, or offsets, occur in the remainder of the power supply loop. Since the 1.5V output on the UC1901 is a trimmed, precision, reference, the need for a trim-pot to fine tune the output voltage is eliminated.

To make the UC1901 compatible with single output 5V power supplies it is designed to operate with input voltages as low as 4.5V. This allows the part to be powered directly from a TTL compatible 5V output. A nominal supply current of only 5mA allows the part to be easily operated at its maximum input voltage rating of 40V without worry of excessive power dissipation.

The amplified error signal at the UC1901's compensation output is internally inverted and applied to the modulator. The other input to the modulator is the carrier signal from the oscillator. The modulator combines these two signals to produce a square wave output signal with an amplitude that is directly proportional to the error signal and whose frequency is that of the oscillator input. This output is buffered and applied to the coupling transformer. With the internal oscillator, carrier frequencies into the megahertz range can be generated. Operating at high frequencies can reduce both the size and cost of the coupling transformer. The secondary winding on the coupling transformer drives a diode-capacitor peak detector. With a simple resistive load to allow discharging of the holding capacitor an effective amplitude demodulator is formed. The small signal voltage gain from the error amplifier input to the detector output is a function of the feedback network around the error-amp, the modulator gain, the turns ratio of coupling transformer, and any loss in the demodulator.

In Figure 2 the relationship of the detector output to the sense supply voltage is non-inverting. This is necessary to guarantee start-up of the supply. Since the UC1901, as shown, is powered from the supply's output, the initial feedback signal back to the PWM controller will always be zero. The required 180° of DC phase shift is easily achieved by inverting the signal with the error amplifier that is present in most any PWM controller circuit.

In some applications it may be desirable to operate the carrier frequency of the UC1901 in synchroni-

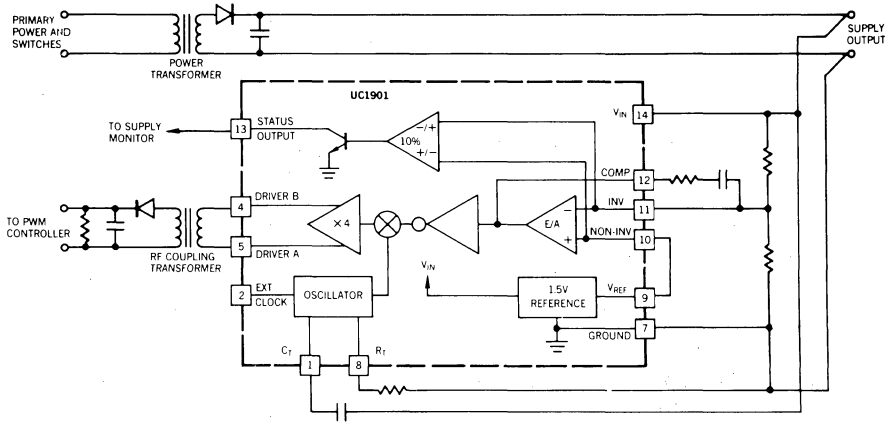


FIGURE 2: With a Precision Reference, and a Complete Amplitude Modulation System, the UC1901 Lets Isolated Feedback Loops be Closed Using a Small Signal Transformer.

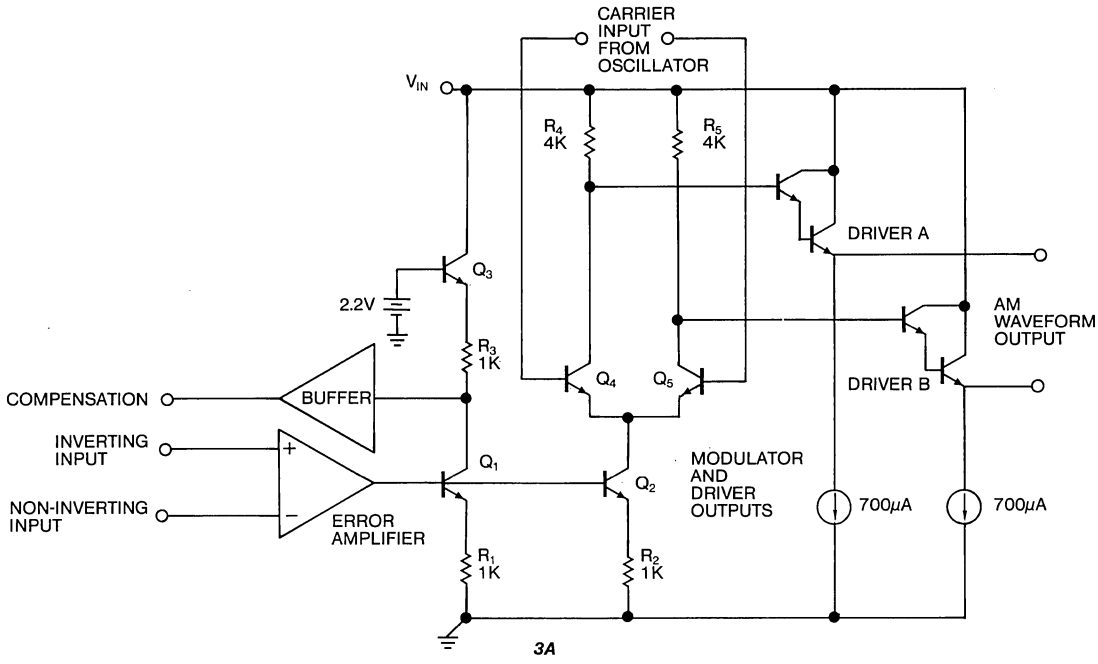


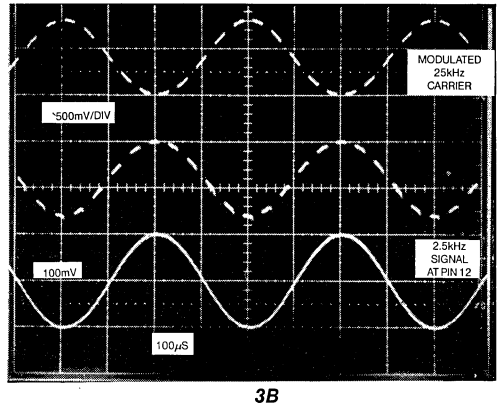
FIGURE 3: The Compensation Output on the UC1901 can be used to Accurately Control the AM Waveform Output. A Simplified Schematic, (a) Shows the internal Signal Split into the Modulator. Voltage Waveforms, (b) Across the Modulator Outputs, and at the Compensation Output show the Modulator Transfer Characteristic.

zation with a system clock, or reference frequency. In many situations, operation of the UC1901 at the switching frequency of the power supply can be beneficial. One such application is presented in this article. To accommodate this need the UC1901 has an external clock input.

One additional mode of operation is possible if the oscillator is left disabled and the external clock signal is kept low (or floated). In this condition the error amplifier can be used in a linear fashion with its output taken at the driver A output. The driver B output will be at a fixed DC voltage about 1.4V from the input supply voltage. If the external clock signal is tied high the roles of the two driver outputs are reversed. With 15mA of output current capacity, the two outputs can easily be combined to reference and drive an optical coupler. Although the instabilities of the coupler will still be present, the advantages of the UC1901's precision reference, high gain amplifier-driver, and 4.5V supply operation can be utilized.

3. A Controlled Feedback Response

There are many different topologies which can be used when implementing a switching power supply. For off-line supplies, fly-back and forward converters are often designed. In the near future current-mode control versions of these may also be widely used. Each of these converter topologies has a different forward transfer characteristic and, within each type of converter, operating point, continuous or discontinuous inductor current, and voltage or current-mode duty cycle control are a few of the factors which can alter this characteristic. In short, the task of optimally designing a feedback network for one supply must usually be repeated when the next supply is designed.



3B

Once the forward transfer function of a particular converter has been determined, various factors such as stability, line regulation, load regulation, and transient response will determine the overall loop response, and therefore feedback response, required. One of the objectives of the UC1901, in addition to allowing a controlled isolated feedback response, is to make the task of implementing a given response as easy as possible. With the compensation node on the UC1901, local R-C feedback networks can be used to shape the small signal gain and phase frequency response of the overall feedback network.

The error amplifier on the chip has a typical open loop gain of 60dB and is internally compensated to have a unity gain bandwidth of just above 1MHz. Both of these characteristics are measured with respect to the compensation node (Pin12). As shown in Figure 3a, the amplified error signal is internally split, at the collectors of Q_1 and Q_2, and fed to both the modulator and the compensation output. Applying feedback from the compensation output to the error amplifier's inverting input controls the small signal collector current through Q_1. Since Q_2 sees the same base voltage, and its emitter resistance is the same, its collector current will track that of Q_1. The collector current of Q_2 feeds the modulator and determines the amplitude of its output signal. The 4-to-1 ratio of resistors R_4 (or R_5) and R_2 results in a fixed 12dB of small signal gain measured as the ratio of the amplitude of the differential signal at the modulator outputs to the compensation mode signal. This relationship, as well as the function of the modulator, is shown in Figure 3b. The scope traces show a 200mV peak to peak sinusoid at 2.5kHz, measured at the compensation output, and the resulting 800mV variations in the peak amplitude of a 25kHz square wave carrier as measured across the modulator's differential output.

The remaining factors influencing the response of the feedback path are the signal gain through the transformer, the detector circuit, and the circuitry between the detector output and the supply's PWM. The signal gain through the transformer is simply the turns ratio of transformer. The small signal detector gain can usually be assumed to be unity as long as the AC load presented to the detector is kept small. Some load on the detector is necessary to allow its output to slew in a negative direction. Figure 4 summarizes the transfer and output characteristics of a typical transformer and detector.

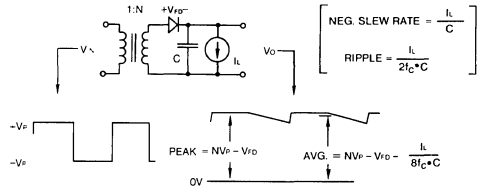


FIGURE 4: A Typical Detector Model and its Output Characteristics.

Here the load on the detector is modeled as a current source, simplifying the equations. In actual practice the operating point of the detector output will be determined by the circuitry which interfaces it with the PWM input. Since the minimum recovery from the detector is zero volts a nominal positive operating level which provides adequate dynamic range for DC and transient conditions should be chosen.

The UC1901 is specified to generate maximum carrier levels equal to or in excess of 1.6V peak. This indicates that a turns ratio of greater than one-to-one will be required for the coupling transformer if the detector output must exceed approximately 1V, (allowing for a detector diode drop of 0.6V). It should be noted that many switching power supplies now being designed include an integrated PWM control IC. A typical PWM IC includes a dedicated error amplifier which amplifies and buffers the input error voltage and applies it to the PWM ramp comparator. This amplifier can be readily used to fix a nominal detector operating point that is compatible with a one-to-one transformer. Additionally, the error amplifier on the UC1901 and the PWM's amplifier can be combined to achieve both large DC loop gains for improved load and line regulation, and the optimization of the loop gain and phase frequency response for improved transient and stability performance.

4. Transformer Requirements

The coupling transformer used with the UC1901 has two primary requirements. First, it must provide DC isolation. Secondly, it should transfer voltage information across the isolation boundary. Meeting the first requirement of DC isolation will depend on specific applications. In general, though, small signal transformers can be readily built to meet the isolation requirements of today's line-operated systems.

For the most stringent applications, E-type cores with bobbin carried windings are inexpensively available or built. Where small size is most important, a simple toroid core can be used.

The second requirement of the transformer primarily determines the amount of magnetizing inductance it must have. The magnetizing inductance of a transformer refers to the actual inductance formed by the windings around the core material. In many classical transformer examples, the magnetizing inductance is ignored. This is a valid approximation since, in these examples, the magnetizing current required is much less than the reflected load currents. In this case, the load currents are small and, as the transformer inductance is reduced, the magnetizing currents become dominant.

The driver outputs on the UC1901 are emitter followers which are biased at 700μA. Therefore, if the drivers are operated without additional bias current the peak current through the transformer's primary winding cannot exceed this value. Figure 5a illustrates the relationship of the magnetizing current to the voltage across the transformer's input. If the reflected load currents are neglected, it can be seen that the minimum magnetizing inductance required for linear transfer of the modulator square-wave is given by:

$$(1) \qquad L_M \geq \frac{V_P}{4 f_c I_P}$$

Where:
- L_M = the magnetizing inductance,
- V_P = the peak carrier voltage across transformer inputs,
- f_c = the UC1901 operating frequency,
- I_P = the bias current of the UC1901 drivers.

As an example, consider the case where Vp is equal to 2V, f_c is 100kHz, and the drivers are operating at their internal bias levels. Using equation 1, the inductance looking into the primary winding with no secondary load must be greater than 7.1mH. Alternatively, if the carrier frequency is raised to 1MHz and the bias levels of the UC1901 drivers are increased to 3.5mA, then L_M can be as low as 150μH. Using high permeability ferrite material, this level of magnetizing inductance can be realized with as little as 10 turns on a small toroid core.

Equation 1 sets a minimum limit on the magnetizing inductance for linear transfer of the carrier wave-

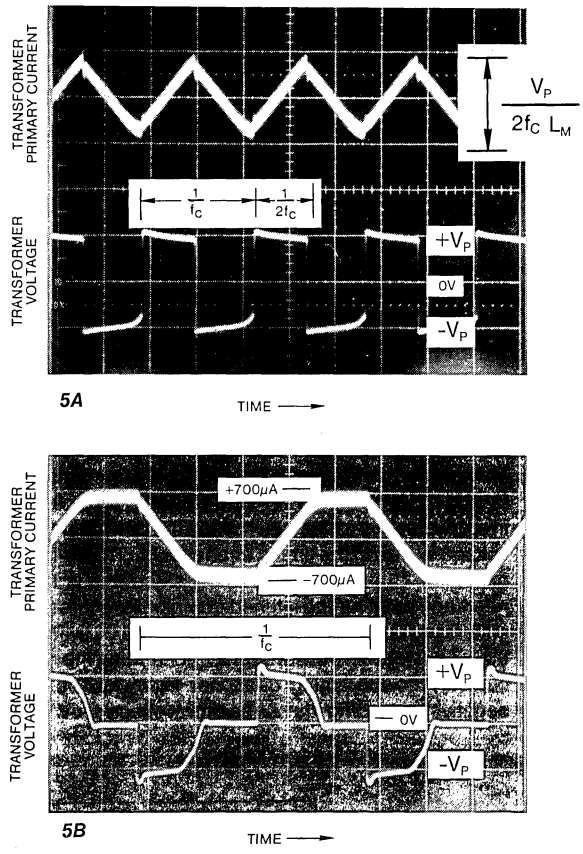


FIGURE 5: The UC1901 Driver Outputs Follow the Modulator Output Square Wave, (a.), Sourcing and Sinking Current Levels Dependent on Transformer Inductance, Carrier Frequency, and Voltage Level. When the Bias Level of the Driver Outputs, I_P, is Reached, (b.), a Tri-state Waveform is Coupled Across the Transformer, the Peak Voltage Level Though, Remains Approximately the Same. The Reflected Load Currents are Assumed Negligible.

form. Actually, the amplitude information is still coupled even when the inductance is less than this minimum. In this case, the UC1901 drivers will support the voltage across the coil until the peak current is reached. The result, illustrated in Figure 5b, is a tri-state waveform at the transformer's input and output. Peak detection of this waveform yields the same amplitude information as the linear transfer case, although detection ripple will increase. Another situation which results in a tri-state waveform exists when the carrier duty cycle is not 50%. In this case, the volt-seconds across the transformer will be balanced by an "imbalancing" of the driver

bias levels. The imbalance will be sufficient to cause the peak current to be reached during the > 50% portion of the carrier waveform.

5. The High Frequency Oscillator

The oscillator circuit on the UC1901 is designed to operate at frequencies of up to 5MHz. To achieve this operating range the circuit shown in Figure 6 uses only NPN transistors in those parts of circuit which are dynamically involved in the actual oscillation. The standard bipolar process used to produce the UC1901 characteristically yields high f_T, typically 250MHz, NPN devices. Conversely, the same process has PNP structures with f_T's of only 1 to 2MHz. In the oscillator, PNP's are used only in determining quiescent operating points of the circuit.

The latched comparator formed by Q_1-Q_4, diodes D_1 and D_2, and resistors R_1 and R_2 has a controlled input hysteresis which determines the peak to peak voltage swing on the timing capacitor C_T. The timing capacitor C_T is referenced to V_{IN} since this is the reference point for the latched comparator's thresholds. The comparator's outputs at D_1 and D_2 switch the 2X current source through Q_{10} changing the net current into the timing capacitor from positive to negative, reversing the capacitor voltage's dv/dt. When the resulting ramp reaches the comparator's lower threshold, the current is switched back to Q_{11} and the ramp reverses until the upper threshold is reached and the process begins again. This results in a triangle waveform at C_T and a squarewave signal at D_1 and D_2.

The magnitude of the charging current is controlled by the external resistor, R_T and the internally generated voltage across it. This voltage is compensated to track variations in the comparator hysteresis. The tracking characteristics of this voltage stabilize the oscillation frequency over temperature and enhance the initial frequency tolerance. Typically, repeatability and temperature stability of the operating frequency are both better than 5%.

The oscillator circuit has been optimized for a nominal R_T of 10kΩ. A desired operating frequency is obtained by choosing the correct value for C_T. As shown in Figure 7, the oscillator frequency is give by the relation:

$$(2) \qquad fosc. = \frac{1.24}{R_T C_T},$$

for frequencies below 500kHz. Above 500kHz, the solid line indicates appropriate C_T values. There is

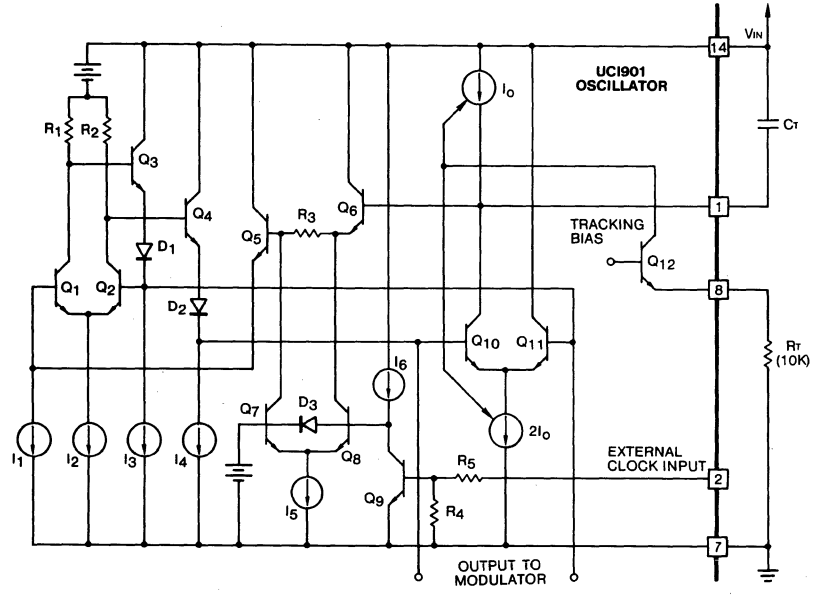


FIGURE 6: UC1901 High Frequency Oscillator Simplified Schematic.

no upper limit on the size of the capacitor used, thus allowing the oscillator to have an arbitrarily long period if desired.

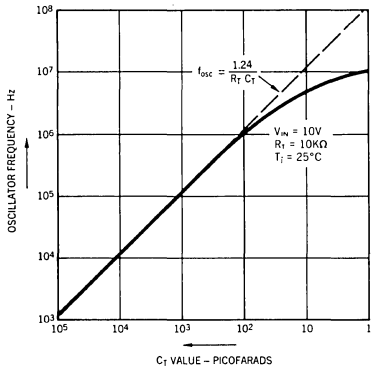


FIGURE 7: UC1901 Oscillator Frequency.

To allow operation of the modulator with a carrier frequency that is driven from a system operating frequency or clock, the oscillator can be over-ridden. Tying C_T to the input supply voltage disables the oscillator. The modulator circuit can now be switched in synchronization with a signal at the external clock input. Internally, the clock signal is applied to the latched comparator via the input device Q_9, and the differential pair Q_7 and Q_8. As the clock input goes high, Q_9 turns Q_8 off and Q_7 on, creating an offset across R_3 that is sufficient to switch the comparator. The comparator then, as before, drives the modulator. When the clock input returns low, the process is reversed. Using the external clock input, both the frequency and duty cycle of the modulator outputs are controlled.

6. A Status Output is More Than Just a Green Light

Many systems today require a monitoring function on the supply output. The status output on the UC1901 can fill this need, a green light function, and can also be used to fill some more "sophisticated" needs. The circuit in Figure 8 takes advantage of the status output in the start-up of an off-line forward converter. The UC1901 is being used in an application where the switching supply must be synchronized to a system clock. The clock signal is generated on the secondary or output side of the supply. To allow start-up, the PWM oscillator is free-running when the line voltage is applied. As the supply voltage rises, the UC1901's external clock input is driven at the switching frequency rate through resistors R_1 and R_2. When the supply output

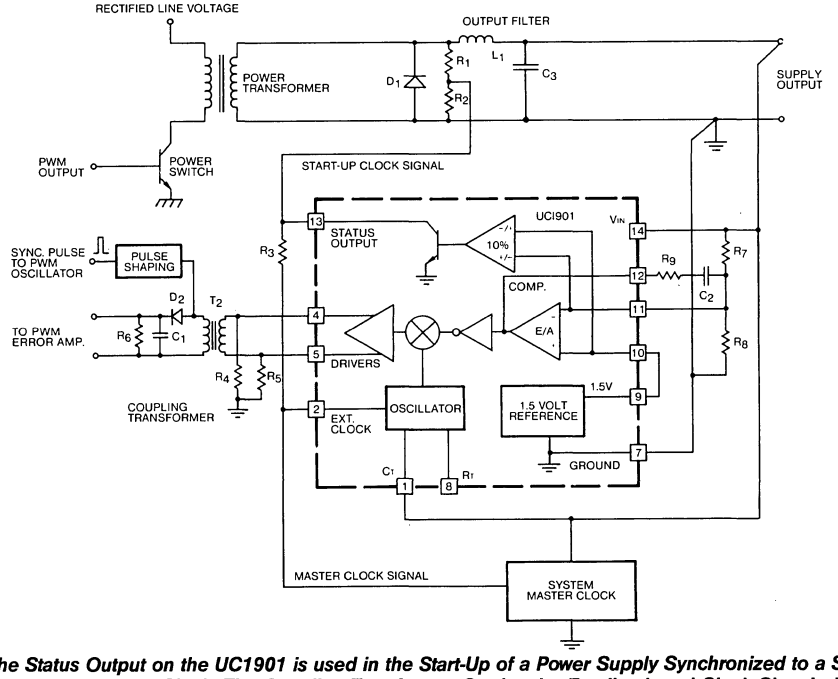


FIGURE 8: The Status Output on the UC1901 is used in the Start-Up of a Power Supply Synchronized to a Secondary Referenced Master Clock. The Coupling Transformer Carries the Feedback and Clock Signals. The Status Output is used to Sequence Clock Signals to the UC1901 External Clock Input During Start-Up.

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reaches 90% of its operating level, the status output decouples the external clock input from the switcher and enables the UC1901's clock input to be driven from the now operational system clock.

On the primary side, the output of the coupling transformer is used before demodulation to provide a synchronization pulse to the PWM control oscillator. Under normal operation, the entire power supply, including the feedback system, will be synchronized to the system clock.

7. The UC1901 in an Off Line Flyback Converter

As alluded to previously, flyback converters see wide use in off-line applications. The flyback topology has some general cost benefits which have spurred its use in low cost, low power (<150W), off-line systems. Perhaps the two most significant of which are the need for only a single power magnetic element in the supply (no output filter inductor is required), and the ability to easily obtain multi-output systems by adding one additional winding to the coupling power inductor for each extra output. Also, the flyback topology, especially when used in the discontinuous mode, lends itself very well to the benefits of voltage feed-forward.

7a. 60 Watt Dual Output Converter

Shown in Figure 9 is a flyback converter designed with the UC1901 and a primary side control IC, the UC1840. The converter has two 30W outputs, one at 5V/6A, and another at 12V/2.5A. Minimum loads of 1A are specified at each output. The UC1901 is used to sense and regulate the 5V output. This output is specified at ±2 percent (untrimmed), with load and line regulation of better than 0.2 percent. Respectively, the 12V output is specified at ±5 percent with ±6 percent load and line regulation. Regulation of the 12V output relies on close coupling between the 5V and 12V output circuits.

The UC1840 controller has all of the features discussed previously for an off-line controller. In addition, it has some advanced fault protection features. Only parts of the UC1840's capabilities are discussed here. For those desiring a more complete description, it can be found in the second reference mentioned at the end of this article. In the supply, the UC1840 sequences itself through start-up using the energy stored in C_4 by the trickle resistor R_{11}. Once the supply is up and running W_4, the auxiliary winding on L_1, provides power to the controller and the switch drive circuitry. The primary winding on the coupled inductor, W_1 is applied across the rectified and filtered line voltage at a 60kHz rate via the FET switching device. L_1 is referred to as a coupled inductor, rather than as a transformer, since the primary and secondary windings do not conduct at the same time. Energy is stored in the inductor core as the switching device conducts, and then "dumped" to the secondary outputs when the device is turned off.

The converter operates in the discontinuous mode. Operating in this mode, the total current in the coupled inductor goes to zero during each cycle of operation. In other words, the energy stored in the core during the beginning of a cycle is entirely expended to the load before the end of the cycle. This allows the inductor size to be minimized since its average energy level is kept low. The price paid for discontinuous operation is higher peak currents in the switching and rectifying devices. Also, high ripple currents at the supply's output(s) make ESR, (equivalent series resistance), requirements on the output filter capacitors more stringent.

7b. Discontinuous Flyback's Forward Transfer Function

The process of designing a feedback network for the supply begins with determining the small signal transfer function of the converter's forward control path. This path can be defined as the small signal dependency of the output voltage, V_{OUT}, to, V_C, the control voltage at the input to the PWM comparator. As defined, the control voltage on the UC1840 appears at the compensation output of its internal error amplifier. The transfer function of this path for the discontinuous converter is given by equation (3).

$$(3) \quad \frac{v_{OUT}}{v_C}(s) = \frac{V_{IN}}{V_R}\sqrt{\frac{T_P R_L}{2L_M}} \cdot \frac{1 + sC_F R_S}{1 + \frac{sC_F R_L}{2}}$$

Where:

- V_{IN} = level of the rectified line voltage,
- V_R = The equivalent peak PWM ramp voltage-equal to the extrapolated control voltage input which would result in a 100% switch duty cycle,
- T_P = One period of the switching frequency,
- L_M = Magnetizing inductance of the primary winding,
- C_F = A total effective output filter capacitor,

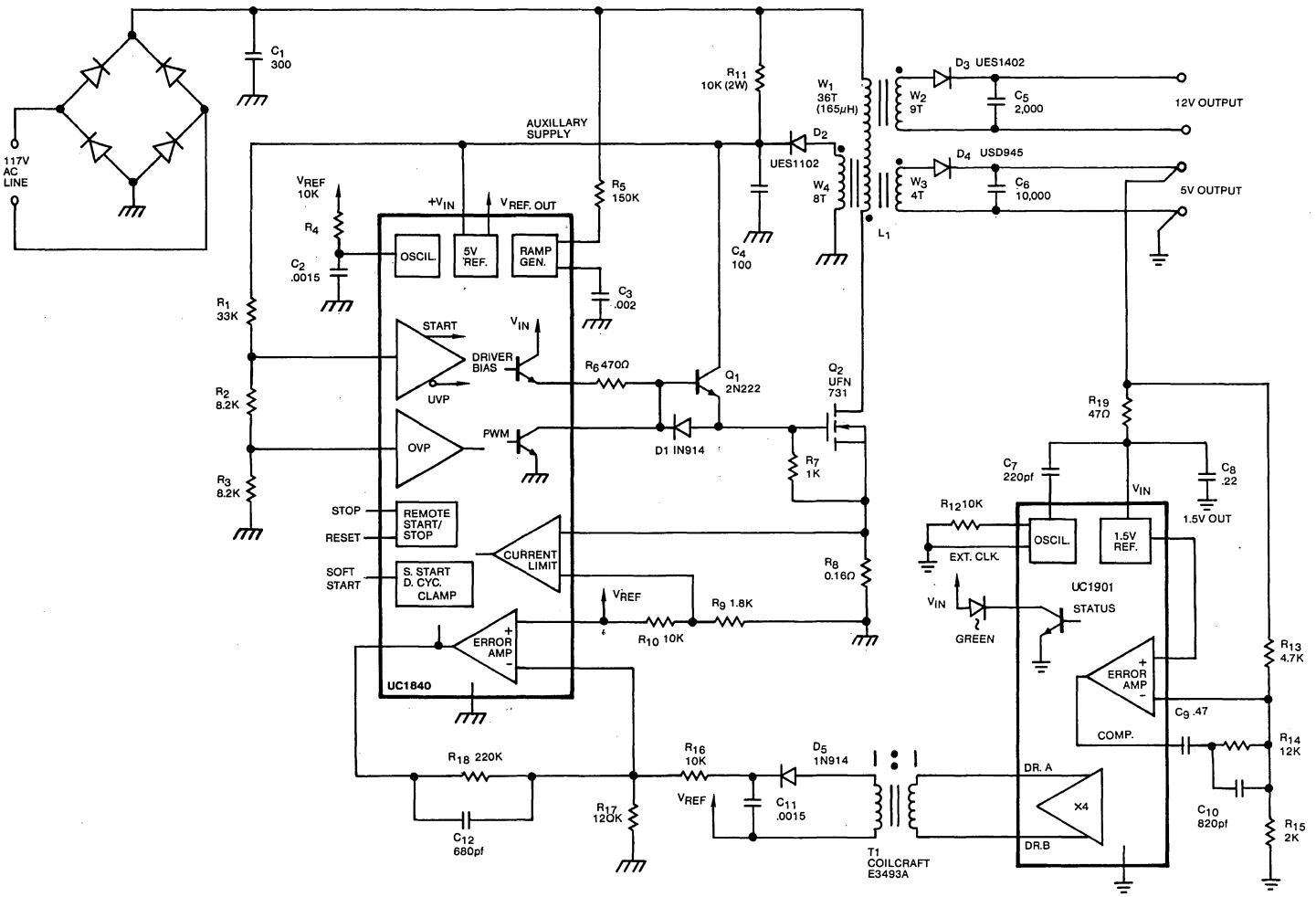

FIGURE 9: The UC1901 Combines With an Advanced PWM Controller in a 60W Off-Line Converter.

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R_L = The total effective load, (assumed resistive),
R_S = ESR of the filter capacitor,
s = $2\pi jf$, f is frequency in hertz.

The word effective is used in describing R_L and C_F since, although we are interested in calculating the response to the 5V output, the loads at the 12V and auxiliary outputs must be accounted for. This is easily done by reflecting these loads to the 5V output using the corresponding turns ratio on the inductor.

7c. Voltage Feedforward Steadies Response

Equation 3 indicates a substantial dependency of the control response to both the load R_L, and the input voltage, V_{IN}. This can slightly complicate the design of the feedback network since both the gain and phase response of the loop will vary with operating conditions.

The benefits of feed-forward are easily illustrated at this point by examining its effect in this circuit. The UC1840 controller uses resistor R_5 to sense the input voltage and proportionately scale the charging current into the PWM ramp capacitor, C_3. Scaling the ramp slope is the same as scaling V_R, the equivalent peak ramp voltage. The result is a modeled ramp voltage given by:

$$(4) \qquad V_R = \frac{V_{IN}\, T_P}{R_5\, C_3}$$

When this expression for V_R is substituted into equation 3, the result is a forward transfer function that is independent of the input voltage. Not only does this simplify the feedback analysis, it also vastly improves the supply's inherent rejection of line voltage variations.

The forward response of the converter, plotted in Figure 10, has a single pole roll-off occurring between 11Hz and 38Hz depending on the load. The single pole roll-off allows the feedback network a bit of latitude since, from a stability standpoint, the loop bandwidth can be extended by simply adding broadband gain with an appropriate roll-off frequency. No mid-band zeros or led-lag networks are necessary, as might be for converters with double pole responses. Although, the zero resulting from the ESR of the filter capacitors can, if not taken into account, appreciably extend the loop bandwidth beyond its intended value.

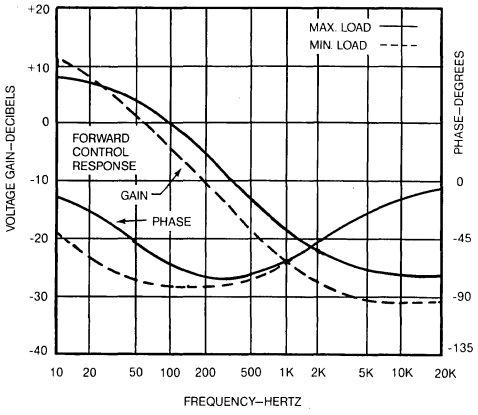

FIGURE 10: Closing the Feedback Loop is Preceeded by the Characterization of the Converter's Forward Small Signal Transfer Function.

7d. Wide Bandwidth Gives Fast Transient Response At 5V Output

This supply was designed to have a unity gain loop bandwidth of between 5 and 10kHz. With this bandwidth the supply's control response to step load and line changes occurs in fractions of a millisecond. This is only true with regard to the 5V output. There is no feedback from the 12V output therefore the output impedence of the 12V supply will be determined by IR losses, the dynamic impedence of the rectifying diodes, and the coupling efficiency between the inductor windings. This impedence is not reduced by the loop gain, as it is at the 5V output. As a result, the time constant of the response at this output will be considerably longer.

The fast response of the 5V output and the relatively slow response of the 12V output are illustrated in Figure 11 which shows three oscilliscope traces in response to a 3.0A load change at the 5V output. The upper trace is the response of the 5V output

which has been expanded and lowpass (< 15kHz) filtered slightly so the small signal loop characteristics can be seen. The trace below this is the 12V output's deviation due to cross-regulation limitations, the longer time constants involved are obvious. Both the fast response of the 5V loop, and the longer settling time of the 12V output are apparent in the third trace. This trace is the fed back correction signal at the UC1840's error amplifier output. From the middle trace the output impedence of the 12V supply can be estimated by noting the approximate 1ms time constant and dividing it by the 2000μF value of the 12V output filter capacitor. This gives a value of 0.5Ω for the output impedence. This agrees well with actual measurements of the 12V output's load regulation.

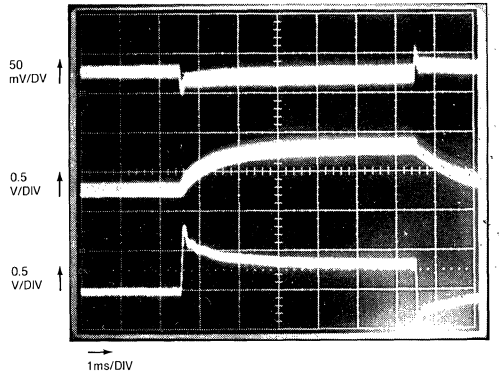

FIGURE 11: The Transient Response of the 5V Output (Top Trace), to a 3.0A Step Load Change Reflects the Extended Bandwidth of the 5V Loop. The Open-Loop 12V Output (Middle), Responds to the Effects of Cross Regulation. The Feedback Error Signal (Lower), Coupled Through the UC1901 is Measured at the UC1840 Error Amp. Output.

7e. The Feedback Response

Plotted in Figure 12 is the response of the feedback network. Also plotted are the asymptotic gain lines of the two contributing gain blocks, the UC1901 response (from 5V output to detector output) and the UC1840 error amp response (detector output to the PWM control voltage). The UC1901's error amplifier is run open loop at DC but is quickly rolled off to 8dB. With the 12dB of modulator gain, the UC1901 feedback system has a broadband gain of 20dB. A pole at 16kHz is added to reduce the gain through the UC1901 error amplifier at the 60kHz switching frequency. As mentioned earlier, excessive gain at the switching frequency can "use up" the dynamic range of the UC1901's AM output.

The UC1901 is operated with a carrier frequency of 500kHz. The coupling transformer, a Coilcraft E3493A, (double E core, bobbin wound construction), has a magnetizing inductance of 2.1mH. At 500kHz the peak current required to drive the primary winding is only 475μA per peak volt. The reflected load current is kept much smaller. This allows the transformer to be easily driven from the UC1901 driver outputs. The E3493A is widely used as a common mode line choke, and is rated for V.D.E. and U.L. isolation requirements. The transformer has a current rating of 2A, greatly exceeding the requirements of this application. Even though the device is larger than some alternatives, its availability and high volume pricing, as well as its isolation capability, make it a very suitable choice.

At the output of the transformer the diode-capacitor detector is referenced, along with the inverting input of the UC1840 error amplifier, to the UC1840's 5V reference. The operating point of the detector is fixed at 0.5V by the divider formed by R_{16} and R_{17} in Figure 9. This in turn sets the operating point of the carrier, with a detector diode drop of 0.5V, at about 1V peak. This level is reflected back through the one-to-one transformer to the UC1901 outputs. A 1V operating point is approximately at the center of the devices dynamic range.

The load current at the detector output is 50μA, set by the 0.5V operating level and R_{16}. The peak to peak detector ripple, at 500kHz, across the .0015μF holding capacitor is about 35mV. The gain through the UC1840 error amplifier at 500kHz is -26dB,

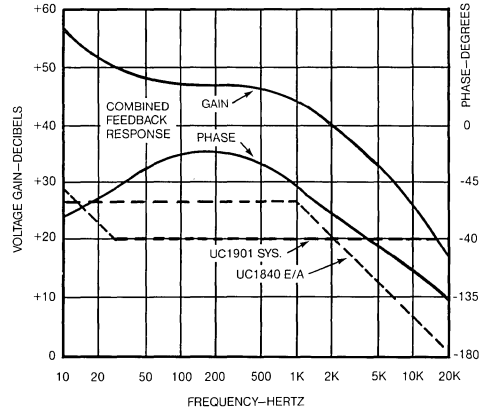

FIGURE 12: Local Feedback Around the UC1901 and 1840 Error Amplifiers is Used to Obtain the Desired Feedback Response.

attenuating the ripple to less than 2mV at the error amplifier output.

The response of the UC1840 error amplifier is flat out to 1kHz where the gain is rolled off to set the loop's 0db frequency. The DC gain is kept as high as possible, to fix the detector operating point, without actually having a series integrating capacitor in the feedback. If both the UC1901 and the UC1840 error amplifiers are run open loop at DC, with series R-C networks to set the AC gain, the total phase margin at low frequencies can become small or nonexistent. The result can be instability or, more likely, a peaked closed loop response that can increase the low frequency noise level of the supply.

The distribution of gain between the UC1901 and UC1840 error amplifiers is somewhat, although not entirely, arbitrary. Keeping the 500kHz ripple at the PWM comparator input below a certain level puts restrictions on the AC gain of the PWM's error amplifier. To much AC gain through the UC1901's amplifier can degrade the supply's transient response under large signal conditions. A suitable distribution for any application will, more than likely, be an iterative procedure. A simple computer or programmable calculator program can be a great tool when massaging these aspects of a design.

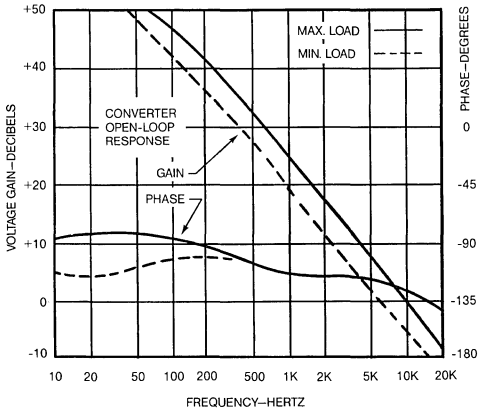

FIGURE 13: The Over-All Open-Loop Response of the Supply Will Determine the Supply's Over-All Stability and Small Signal Transient Response.

The overall open-loop responses, plotted in Figure 13, will not vary significantly except as indicated with load. The desired loop bandwidth has been achieved with an adequate phase margin of $> 50°$.

The result is a supply with very repeatable, as well as stable, operating characteristics. The same type of analysis for determining the required feedback response can be used in applying the UC1901 to any type of isolated closed loop supply. The choice of coupling transformer and carrier frequency used with the UC1901 should be based on individual system requirements.

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3.) R.D. Middlebrook and S. Cuk, "Modeling and Analysis Methods for DC-to-DC Switching Converters", Advances in Switched-Mode Power Conversion, TESLAco, Pasadena, Calif., 1981.

4.) R. Patel and G. Fritz, "Switching Power Supply Design Review–60 Watt Flyback Regulator, Unitrode Power Supply Design Seminar Manual, Unitrode Corporation, Lexington, Mass., 1983.

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VERSATILE UC1834 OPTIMIZES LINEAR REGULATOR EFFICIENCY

Linear voltage regulators have long been an important resource to power supply designers. Three terminal, fixed-voltage linear regulators find extensive use as "spot" regulators and as post-regulation stages fed by switched-mode supplies. However, while inexpensive and simple to use, these devices have several performance limitations.

First, three terminal regulators are inefficient power converters. Power dissipation in a linear regulator is given by the relation:

$$P = I_O \cdot (V_{IN} - V_{OUT}).$$

Most monolithic regulators now available require an input-to-output voltage differential of at least 2 to 3V. This requirement can result in substantial inefficiency, particularly in low voltage supplies. As switched-mode power technology matures, power losses incurred in linear post-regulation stages are becoming more significant in terms of overall system efficiency.

Second, fixed-voltage regulators, with fixed maximum output currents, lack versatility. The use of these devices requires that OEMs maintain large, diverse inventories in order to support a broad range of power supply requirements.

Third, fixed three-terminal devices lack the capability of remote voltage sensing, and therefore can exhibit poor load regulation.

Finally, the most common failure mechanism for linear regulators is a shorted pass transistor. All critical loads, therefore, require over-voltage protection not provided by three-terminal regulators.

IMPROVED PERFORMANCE WITH UC1834

The UC1834 is a programmable linear regulator control IC which, with an external pass transistor, forms a complete linear power supply. This IC provides solutions to all the above-mentioned drawbacks of three-terminal devices.

Figure 1 shows the basic elements of positive and negative regulators implemented with the UC1834. An error amplifier monitors the output voltage and provides appropriate bias to the pass transistor (Q1) through a driver stage. This high-gain error amplifier (E/A) allows good dynamic regulation while allowing Q1 to operate near saturation in the common-emitter mode. The circuits can achieve high efficiency by maintaining output regulation with an input-to-output voltage differential as low as 0.5V (at 5A).

The UC1834 has both positive and negative reference voltage outputs, as well as a sink-or-source driver stage, as shown in Figure 1. These features allow implementation of either positive or negative regulators with this single IC, as shown. Output voltages from 1.5V to nearly 40V can be programmed by appropriate choice of remote sensing divider elements. Remote sensing also allows improved DC and dynamic load regulation.

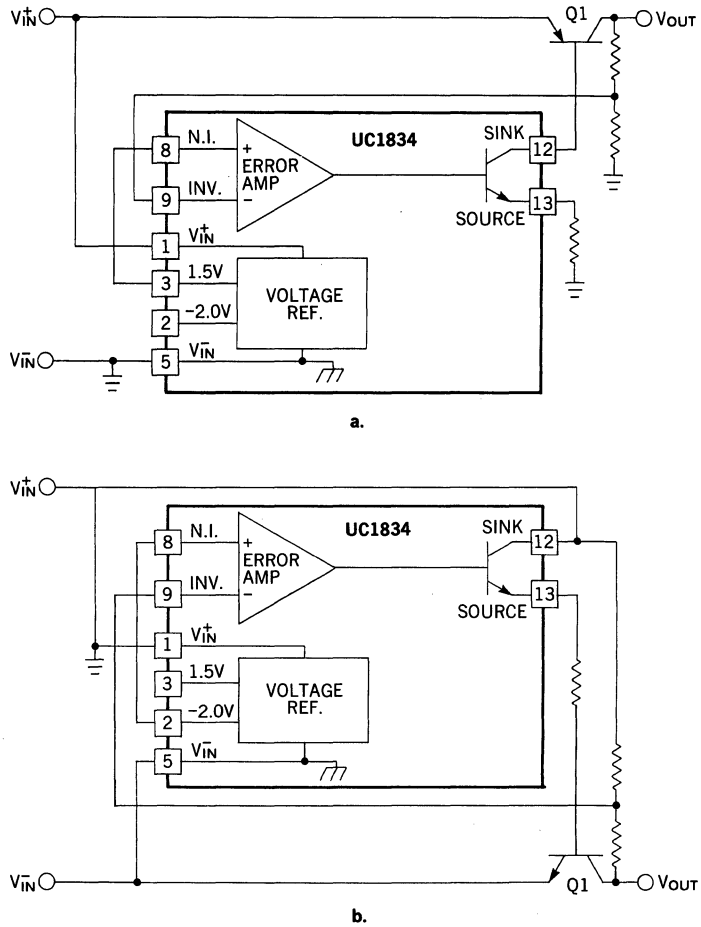


Figure 1. Basic Elements of (a.) Positive and (b.) Negative Regulators implemented with a UC1834

The UC1834 is intended to provide a complete linear regulation system. Therefore, many auxiliary features are included on this IC which eliminate the need for additional circuit elements. Figure 2 shows a more complete block diagram including on-chip provisions for current sensing, fault monitoring, remote voltage sensing, and thermal protection.

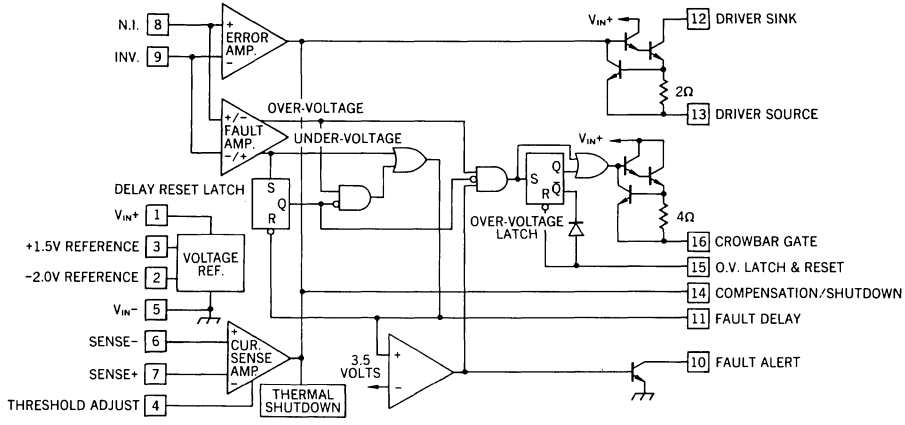


Figure 2. UC1834 Block Diagram

DRIVING THE PASS TRANSISTOR

Figure 3 shows suggested pass transistor configurations for implementing either positive or negative regulators with the UC1834. For those low current (≤200mA) applications in which efficiency is not extremely critical, the UC1834 output transistor can serve as the pass element, resulting in the simple configurations of Figure 3a. An external pass transistor is needed for output currents greater than 200mA. With the circuits of Figure 3c, the UC1834 can maintain regulation while operating the pass transistor near saturation. Operation at very high output currents (to ~30A) is possible with the Darlington pass elements of Figure 3d.

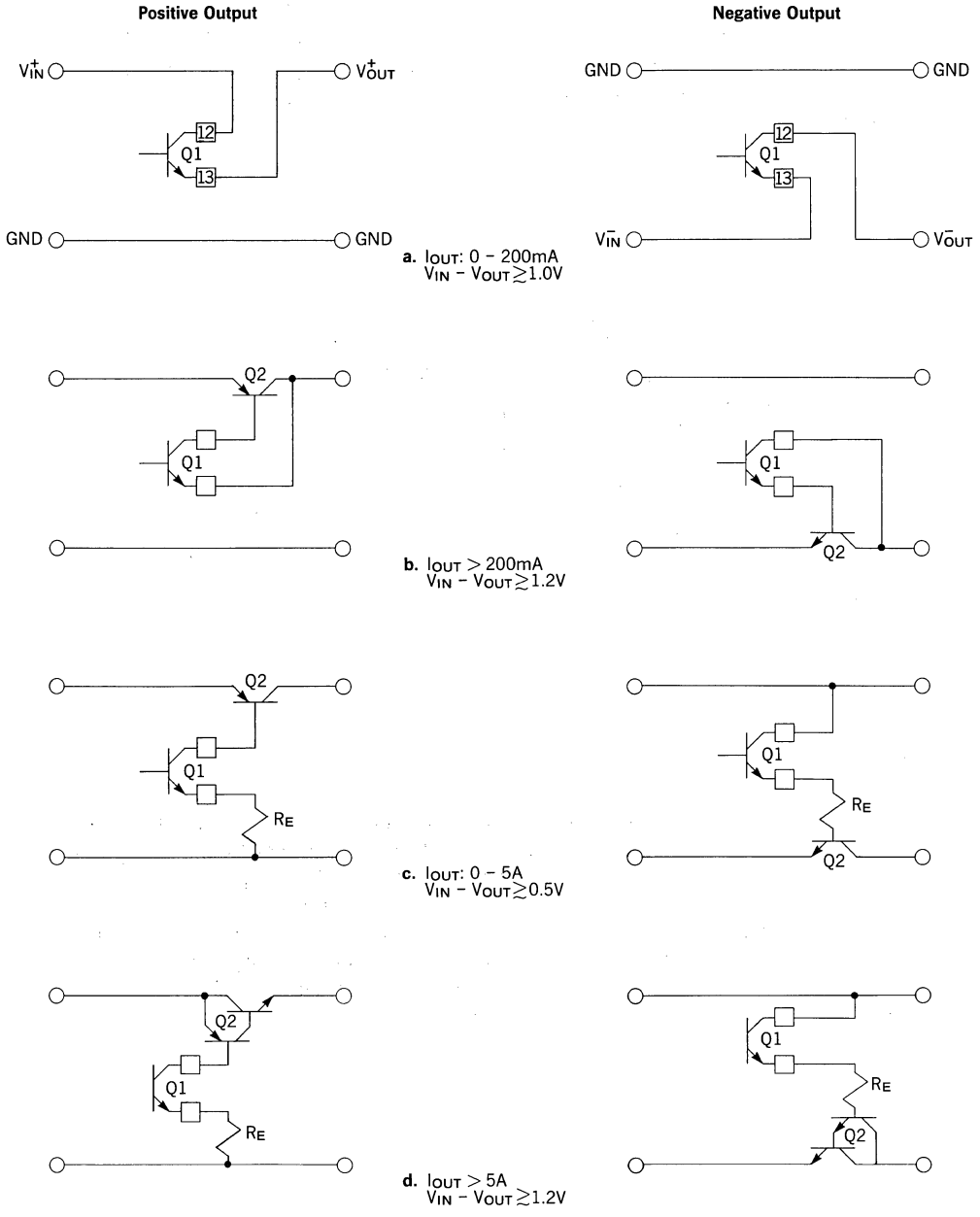


Figure 3. Pass Transistor Configurations

Current in the UC1834 output transistor is self-limiting, for improved reliability. This limiting is achieved by Q3 and R1 in Figure 4a. The resulting maximum output current is a function of temperature as shown in Figure 4b.

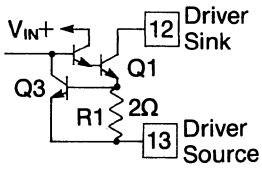
A resistor (R_E) is shown in series with the drive transistor in Figures 3c, d. This resistor shares base-drive power with the transistor, allowing cooler, more reliable operation of the IC. R_E should be as large as possible while still supporting adequate pass transistor base current under worst-case conditions of low input voltage and maximum output current:

$$V_{R_E(min)} = V_{IN(min)} - V_{BE(max)(Q2)} - V_{CE(sat)(max)(Q1)}$$
$$I_{B(max)(Q2)} = I_{O(max)} / \beta_{(min)(Q2)}$$
$$R_{E(opt)} = V_{R_E(min)} / I_{B(max)(Q2)}$$

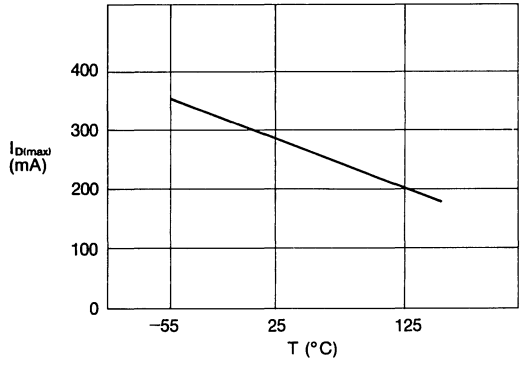
where: $V_{R_E(min)}$ is minimum voltage available to R_E
$I_{B(max)\ (Q2)}$ is maximum required base drive to Q2
$R_{E(opt)}$ is optimum value of R_E.

R_E also enhances stability by allowing operation of Q1 as an emitter-follower, thereby eliminating β_{Q1} from the loop transfer function:

$$I_{C(Q1)} \approx I_{E(Q1)} = (V_{E/A\ out} - V_{BE(Q1)} - V_{BE(Q2)}) / R_E \quad (\beta \text{ independent}).$$



a.



b.

Figure 4 a. Driver Current Limiting Circuit
b. Resulting Maximum Current vs Temperature

CURRENT SENSING

In order to protect the pass transistor from damage due to overheating, one must sense its emitter current (I_E) and then decrease the base drive if I_E is excessive. The UC1834 current sense amplifier (CS/A) accomplishes these tasks.

The UC1834 CS/A has a common mode range which includes both input supply "rails". This extended range is made possible by introducing matched voltage offsets in the differential input paths, as shown in Figure 5. Internal current sources bias the offset diodes in their appropriate direction. Which bias source (+ or -) is active is determined by whether the CS/A positive (+) input is greater or less than $V_{IN}/2$. Therefore, it is advisable to configure the sensing circuit such that the voltage at CS/A(+) will not cross $V_{IN}/2$ during operation. This precludes sensing in series with the load for most applications.

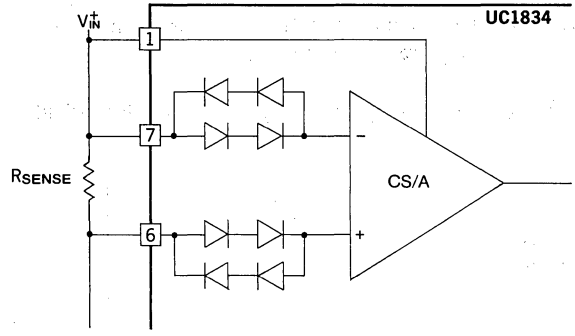


Figure 5. Two Diode-Drop Offset Allows Current Sensing at Supply Rail

The CS/A has a programmable current limit threshold which can be set between 0mV and 150mV. Programming is achieved by setting the voltage at the "Threshold Adjust" terminal (pin 4) to $10 \cdot V_{TH(desired)}$. The factor of 10 provides good noise immunity at pin 4 while allowing low power dissipation in the current sensing resistor. Figure 6 shows the guaranteed relationship between V_{PIN4} and the actual resulting threshold across the CS/A inputs. Note that the threshold is clamped at 150mV if pin 4 is open or if $V_{PIN4} > 1.5V$. The "Threshold Adjust" input is high impedance (bias current is less than $10\mu A$), allowing simple programming through a voltage divider from the 1.5V reference output. However, loading the 1.5V reference will affect the regulation of the -2.0V reference. Figure 7 shows how to compensate for this loading with a single resistor when the -2.0V reference is needed.

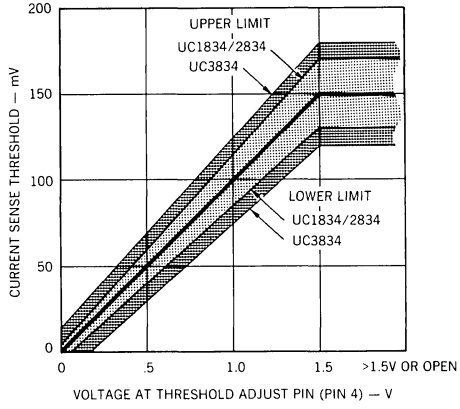


Figure 6. Guaranteed Tolerances on C/S Threshold Adjustment

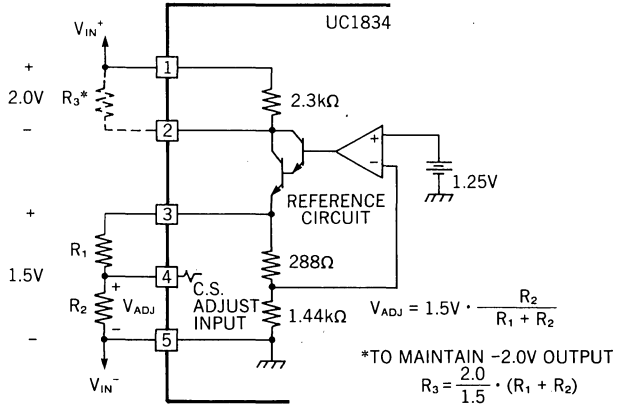


Figure 7. Setting the Current Threshold and Compensating the −2.0V Reference

The CS/A functions by pulling the E/A output low, turning off the output driver (Figure 8). As current approaches the threshold value, the E/A attempts to correct for the CS/A output, resulting in an E/A input offset voltage.The supply output voltage can decrease a proportional amount. When the CS/A input voltage differential reaches the current sense threshold, then the pass transistor is totally controlled by the CS/A. The combined CS/A and E/A gains and output configurations result in the current limit knee characteristic of Figure 9.

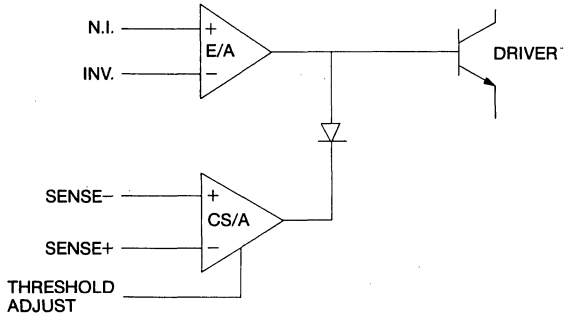


Figure 8. Current Sense Tied to E/A Output

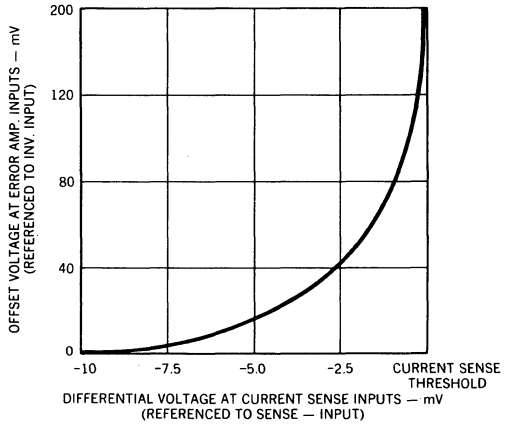


Figure 9. Current Limiting Knee Characteristic

FOLDBACK CURRENT LIMITING

It is desirable to put an upper limit on pass transistor power dissipation in order to protect that device. Ideally, for a constant power limit:

$I_{E(max)} \cdot V_{CE} \simeq K$ where K is a constant

or: $I_{E(max)} \simeq K/(V_{IN} - V_{OUT})$ (ignoring the sense resistor voltage drop).

As the input-to-out voltage differential increases, it is necessary to "fold back" the maximum allowable current. This ideal foldback characteristic is shown in Figure 10, along with a practical characteristic achievable with the circuit of Figure 11.

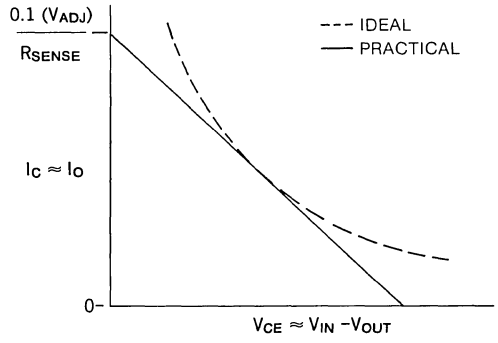


Figure 10. Ideal (Dashed Line) and Practical (Solid Line) Foldback Current Limiting Characteristics

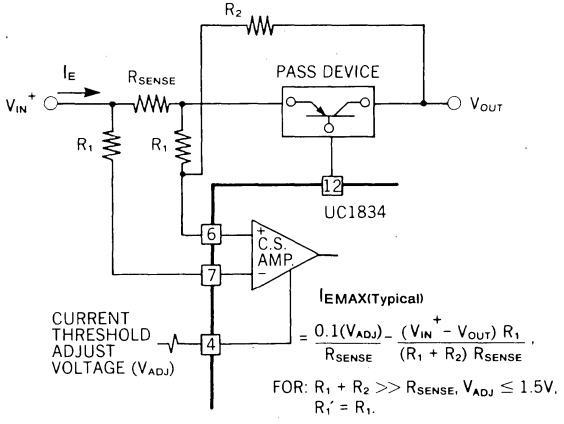


Figure 11. Foldback Current Limiting — Responds to Changes in V_{IN} or V_{OUT}

This circuit responds to changes in either V_{IN} or V_{OUT}. The voltage differential V_{IN} - V_{OUT} causes proportional current flow through R_1 and R_2. The additional drop across R_1 is interpreted by the CS/A as additional load current. The result is that the real current limit decreases linearly with V_{IN} - V_{OUT}:

$$I_{E(max)} = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN} - V_{OUT})\,R_1}{(R_1 + R_2)\,R_{SENSE}}$$

for: $R_1 + R_2 \gg R_{SENSE}$
$V_{ADJ} \leq 1.5V$
$R_1' = R_1$.

This technique can be susceptible to "latch-off". If a momentary short at the supply output causes I_E to drop to zero (pass transistor cut off), then V_{OUT} cannot recover when the short is subsequentially removed. To prevent this undesirable operation, one must ensure that $I_{E(max)} > 0$ when $V_{OUT} = 0$ and V_{IN} is at its minimum:

$$I_{E(max)} \Big|_{\substack{V_{OUT}=0 \\ V_{IN(min)}}} = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN} - V_{OUT})\,R_1}{(R_1 + R_2)\,R_{SENSE}} > 0$$

$$\frac{0.1(V_{ADJ})}{V_{IN(min)}} > \frac{R_1}{R_1 + R_2}$$

$$R_2 > \frac{V_{IN(min)}\,R_1}{0.1\,(V_{ADJ})}\left(1 - \frac{0.1\,(V_{ADJ})}{V_{IN(min)}}\right)$$

Figure 12 shows an alternative foldback current limiting scheme which responds to decreased V_{OUT} only. This circuit gives the output characteristics of Figure 13, defined by the following relation:

$$I_{E(max)} = \frac{0.1}{R_{SENSE}} \cdot \left(\frac{R_1R_2\,V_{OUT} + R_2R_3\,V_{REF}}{R_1R_2 + R_1R_3 + R_2R_3}\right)$$

This technique is immune to "latch-off" because the minimum current limit is always non-zero.

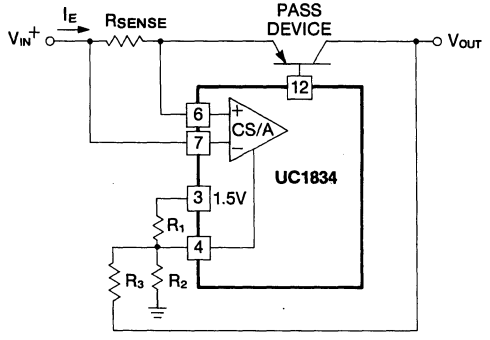


Figure 12. Foldback Current Limiting — Responds to Changes in V_{OUT} Only

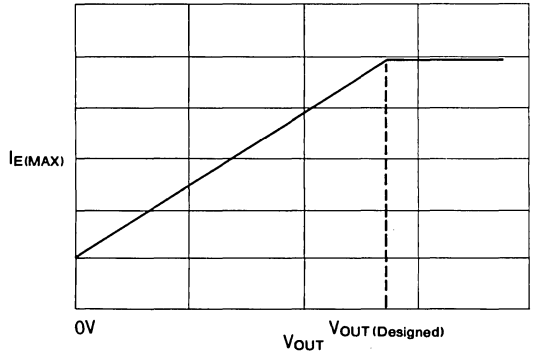


Figure 13. Foldback Current Limiting Characteristic

FAULT CIRCUITRY AND SYSTEM INTERFACING

In order to minimize the need for additional components, the UC1834 has on-chip provisions for fault detection and logic interfacing. These features are particularly useful when the linear regulator is part of a larger power supply system.

As shown in Figure 14, an internal comparator monitors the UC1834 E/A inputs. This comparator has two thresholds, for over- and under-voltage detection. Comparator thresholds are fixed at $|V_{N.I.} - V_{INV.}| = 150mV$. The resulting output voltage windows for non-fault operation are:

$$\frac{\pm .150V}{1.5V} = \pm 10\% \text{ for positive (+) supplies}$$

$$\frac{\pm .150V}{2V} = \pm 7.5\% \text{ for negative (-) supplies.}$$

A fault delay circuit prevents transient over- or under-voltage conditions (due to a rapidly changing load) being defined as faults. The delay time is programmable. An external capacitor at pin 11 is charged from an internal 75μA source. The delay period ends when the capacitor voltage reaches ~3.5V. The delay time is therefore ~47ms/μF. The fault alert output (pin 10) becomes an active low if an out-of-tolerance condition persists after the delay period. When no fault exists, this output is an open collector.

An over-voltage fault activates a 100mA crowbar gate drive output (pin 16) which can be used to switch on a shunt SCR. Such a fault also sets an over-voltage latch if the reset voltage (pin 15) is above the latch reset threshold (typically 0.4V). When the latch is set its $\overline{Q}$ output will pull pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents $\overline{Q}$ from pulling pin 15 below the reset threshold. However, pin 15 is pulled low enough to disable the driver outputs if pins 15 and 14 are tied together. With pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.

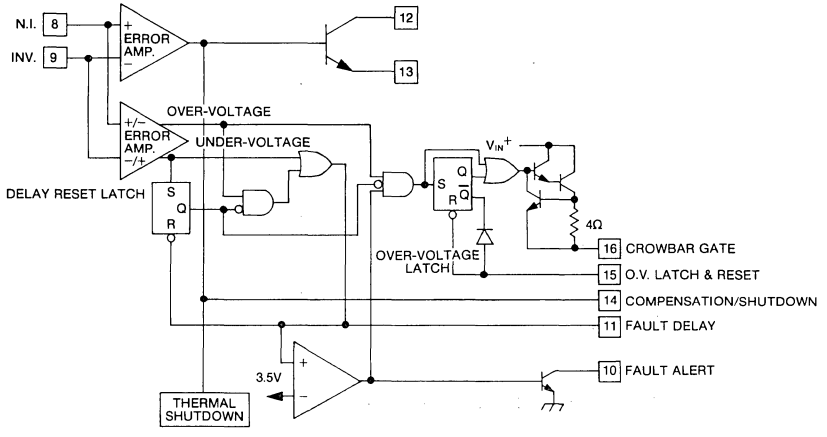


Figure 14. Fault Circuitry

An internal "delay reset latch" prevents crowbar turn-on when an under-voltage condition is immediately followed by a transient over-voltage condition. Such a situation could arise from a momentary short circuit at the supply output.

A thermal shutdown circuit pulls the E/A output low when junction temperatures reach 165°C, in order to protect the IC from excessive power dissipation in the drive transistor.

COMPENSATING THE FEEDBACK LOOP

A reliable design for any feedback system must yield a closed-loop frequency response which ensures unconditional stability. An optimum power supply response provides this stability while maximizing broadband gain for good dynamic voltage regulation with changing loads. Figure 15 illustrates such a response. The 0dB crossover frequency (f_c) should be as high as possible while maintaining phase margin above -360° at all lower frequencies (Nyquist stability criterion). In practice, this criterion dictates a single-pole response below f_c.

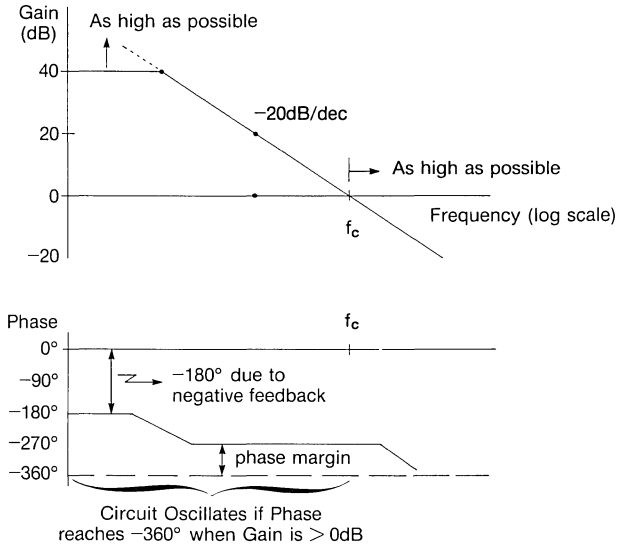


Figure 15. Desired Closed-Loop Response

Linear supplies using the UC1834 will usually have a current limiting loop in addition to the voltage control loop, as illustrated for two basic configurations* in Figure 16. Both loops must be stabilized for reliable operation. This is accomplished by appropriately compensating the E/A and CS/A at their common output (pin 14). Design of the compensation networks will often require an iterative procedure, since the compensation for one loop will affect the response of the other. A straightforward approach is outlined below:

1). Determine the frequency response of all voltage loop elements excluding the E/A. Appendix I offers guidelines for this step.

2). Design E/A compensation giving a frequency response which , when added to the response calculated in step 1, will yield a total loop characteristic consistent with the objectives outlined above. (Appendix II.)

3). Calculate the current loop response and determine whether it satisfies the Nyquist stability criterion. (Appendix III.) If not, add additional compensation and then recalculate the voltage loop response.

4). Iterate if necessary.

*All other configurations of Figure 3 are variants of these two, and can be treated in essentially the same ways.

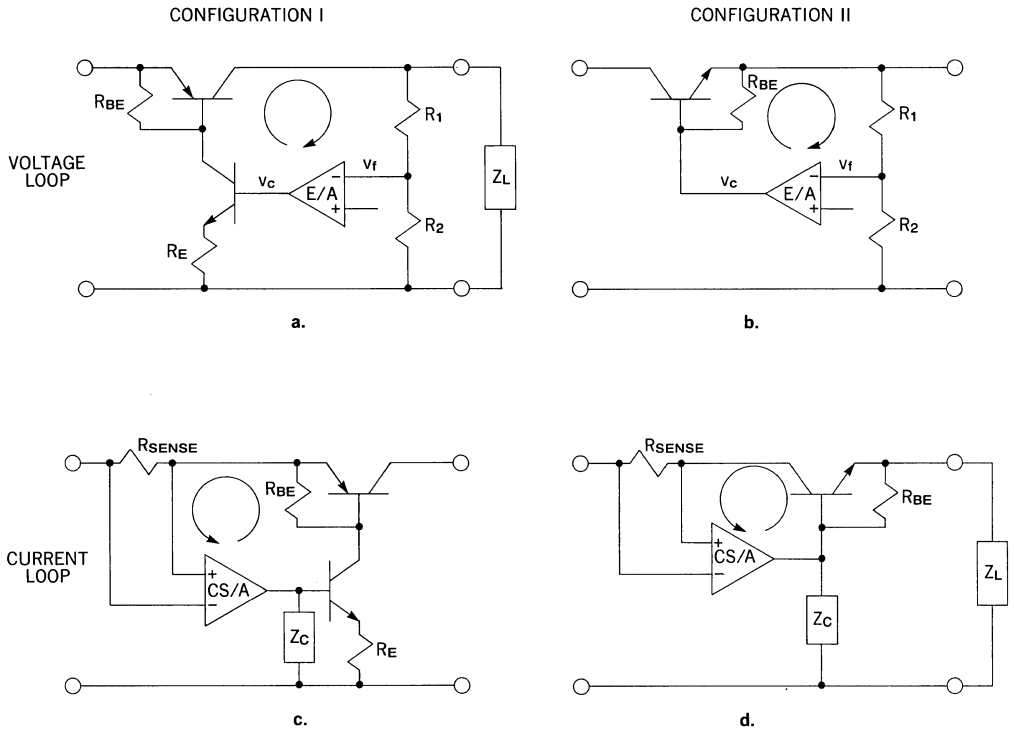


Figure 16. Voltage and Current Loops for Two Basic Configurations

EXAMPLE

Figure 17 shows a 5V, 5A (positive output) supply of the class shown in Figures 16a, c. This circuit tends toward instability when it is lightly loaded because of the high gain (β = 200) of the pass transistor at low currents. Output capacitor C_2 is needed to introduce a pole which rolls off the gain of the voltage loop to 0dB at 100kHz, avoiding instability due to the additional phase shift of a transistor pole at:

$$f = \frac{f_T}{\beta} = \frac{50\text{MHz}}{200} = 250\text{kHz}$$

Assuming a minimum load of 1A (R_L = 5Ω), the low frequency voltage loop gain, excluding the E/A, is (from Appendix I):

$$A_V = \frac{1}{15\Omega} \cdot 200 \cdot 5\Omega \cdot \frac{0.51\text{k}\Omega}{(1.7 + 0.51)\ \text{k}\Omega} = 20 = 26\text{dB}.$$

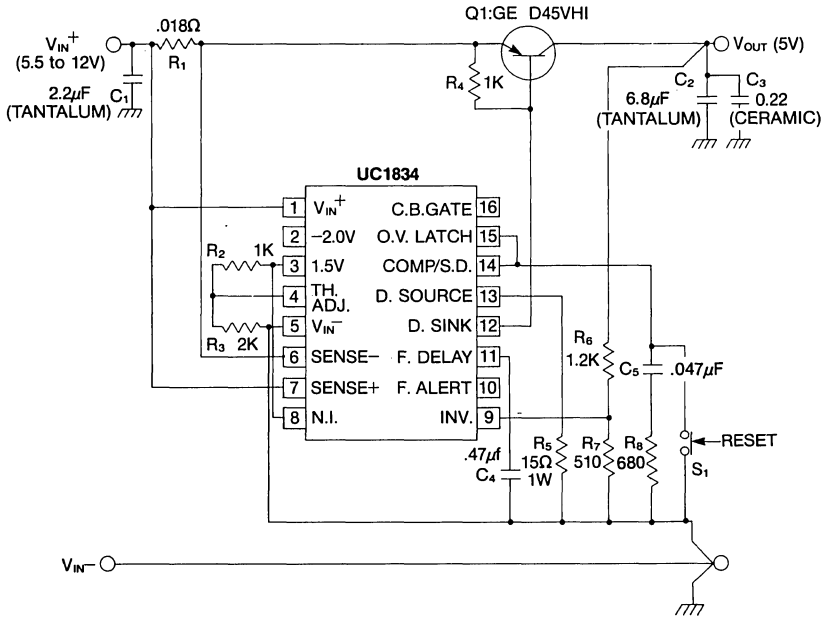


Figure 17. 0.5V Input-Output Differential 5A Positive Regulator

A pole at 5kHz is required in order to roll off from 26dB to 0dB at 100kHz. The required value of C_2 is therefore given by:

$$C_2 \doteq \frac{1}{2\pi \cdot R_L \cdot f_p} = \frac{1}{2\pi \cdot 5\Omega \cdot 5kHz} = 6.4\mu F \text{ (6.8}\mu F \text{ used).}$$

The dashed curves of Figure 18a show the resulting voltage loop response, excluded the compensated E/A. Notice that the 5kHz pole (just added) itself introduces undesirable phase lag. This can be corrected by positioning the compensation zero (see Appendix II) at the same frequency. With $R_8 = 680\Omega$ (providing ~0dB E/A gain above 5kHz), then:

$$C_5 = \frac{1}{2\pi \cdot 680\Omega \cdot 5kHz} = .047\mu F.$$

The gain and phase of the compensated E/A (dotted lines) and complete voltage loop (solid lines) are also shown in Figure 18a.

The resulting current loop response (Figure 18b) is seen to meet the stability criterion. Gain above 5kHz is given by (from Appendix III):

$$A_I = \frac{1}{70\Omega} \cdot 680\Omega \cdot \frac{1}{15\Omega} \cdot 200 \cdot 0.018\Omega = 2.3 = 7.4dB.$$

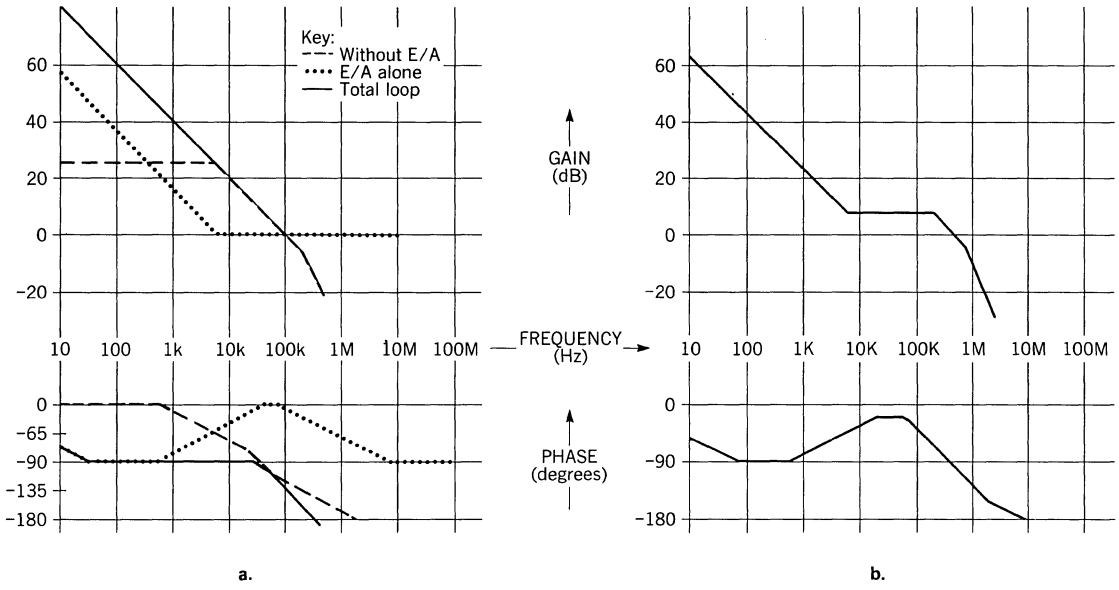


Figure 18. Loop Responses for Circuit of Figure 17
a. Voltage Loop
b. Current Loop

Reasonable phase margin (~40°) is maintained as the transistor and CS/A poles roll off this small gain to 0dB.

Figure 19 shows the UC1834 used to implement a negative output supply. A Darlington pass element provides adequate gain for operation at output current levels up to 10A.

CONCLUSION

Ever-increasing requirements for improved power supply economy and efficiency have produced a need for a versatile control IC capable of minimizing power losses in linear regulators. The UC1834 meets this need while also supporting all the auxilliary functions required of such supplies. This control circuit provides for optimized performance in a broad range of linear regulators, and in fact extends the range of applications for which such regulators are appropriate.

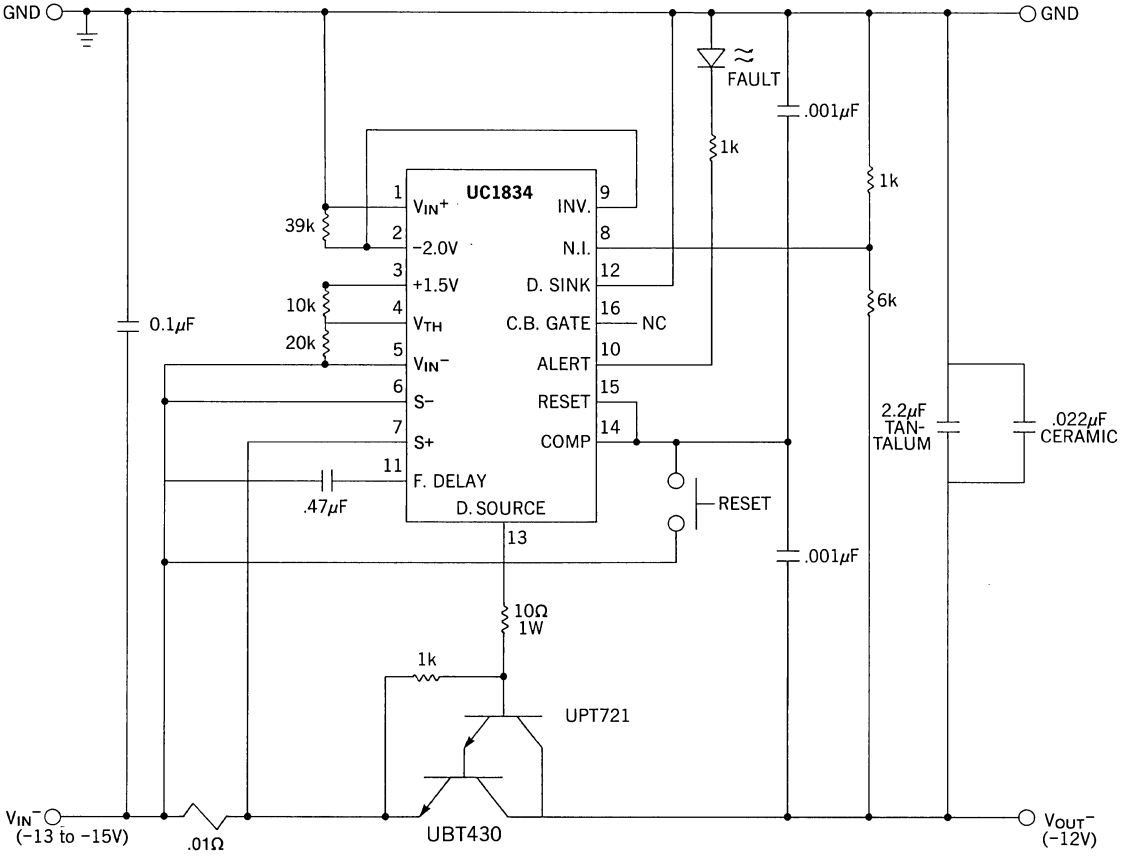


Figure 19. −12V, −10A Negative Regulator

APPENDIX I - FREQUENCY RESPONSE OF VOLTAGE LOOP ELEMENTS

A. The configuration of Figure 16a has, in addition to the compensated E/A, the following loop elements:

- **Drive Transistor** - R_E allows operation of the driver as an emitter follower. Together these elements have an effective small signal AC conductance of $1/R_E$.

- **Pass Transistor** - Low frequency gain (β) and unity-gain frequency (f_T) are usually specified. The pass transistor adds a pole to the loop transfer function at $f_p = f_T/\beta$. Therefore, in order to maintain phase margin at low frequencies, the best choice for a pass device is often a high frequency, low gain switching transistor. Further improvement can be obtained by adding a base-emitter resistor (R_{BE} in Figure 16a) which increases the pole frequency to:

$$f_p = \frac{f_T}{\beta}\left(1 + \frac{\beta \cdot r_e}{R_{BE}}\right)$$

where: $r_e = \frac{kT}{qI_C} = \frac{0.026mV}{I_C}$ (at T = 300K).

- **Load Impedance** - Load characteristics vary greatly with application and operating conditions. The most commonly used models and their respective (s domain) transfer functions are given in Table 1. Note that there are no poles in the transfer functions of those loads which lack shunt capacitance. This can result in a loop transfer function which cannot be rolled off to 0dB at a suitably low frequency using simple E/A compensation networks. For this reason a shunt output capacitor is often added to supplies which must drive loads having low or indeterminant capacitance.

- **Voltage Divider** - The output sensing network introduces a gain of $R_2/(R_1 + R_2)$.

- **Total Loop Gain,** excluding the E/A, is therefore given by:

$$A_V = \frac{v_c}{v_f} = \frac{1}{R_E} \cdot \beta_{PASS} \cdot Z_L \cdot \frac{R_2}{R_1 + R_2} \qquad \text{for } f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right).$$

B. The circuit of Figure 16b has a more straightforward response, since the only element (other than the E/A) which introduces any gain is the voltage divider:

$$A_V = \frac{R_2}{R_1 + R_2}$$

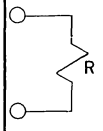
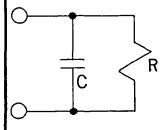
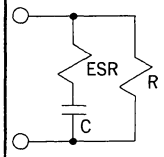
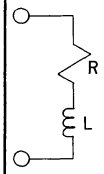
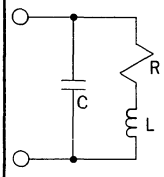
Load Model	Transfer Function	Poles @ f =	Zeros @ f =
	$Z_L(s) = R$	———	———
	$Z_L(s) = \frac{R}{1 + sRC}$	$\frac{1}{2\pi RC}$	———
	$Z_L(s) = \frac{R(1 + s(ESR)C)}{1 + s(R + ESR)C}$	$\frac{1}{2\pi(R + ESR)C}$	$\frac{1}{2\pi(ESR)C}$
	$Z_L(s) = R + sL$	———	$\frac{R}{2\pi L}$
	$Z_L(s) = \frac{s\left(s + \frac{R}{L}\right)}{s^2 + \frac{R}{L}s + \frac{1}{LC}}$	$\frac{-R/L \pm \sqrt{R^2/L^2 - 4/LC}}{4\pi}$	$0, \frac{R}{2\pi L}$

Table 1. Load Models and their Transfer Functions

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APPENDIX II - ERROR AMPLIFIER RESPONSE

Figure 20 shows the open-loop gain and phase response of the UC1834 E/A when lightly loaded. The gain curve represents an upper limit on the gain available from the compensated amplifier. Note that a second-order pole occurs near 800kHz. Stable circuits will require a 0dB crossover well below this frequency ($f_c \lesssim 500kHz$).

The E/A can be compensated with or without the use of local feedback. When operated without such feedback (Figure 21a) the transconductance properties of the E/A become evident; i.e. the voltage gain in given by:

$$A_{V(E/A)} = g_M Z_C \qquad (f \lesssim 500kHz)$$

where: $g_M \approx \frac{1}{700\Omega} = 1.4mS$

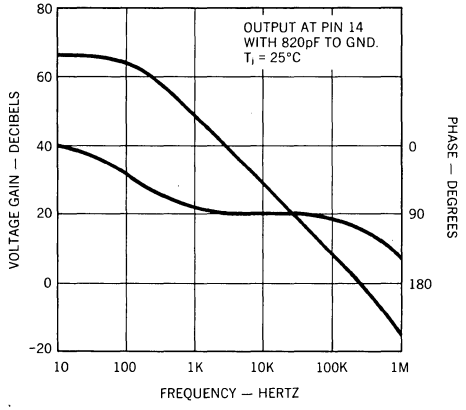


Figure 20. Error Amplifier Gain and Phase Frequency Response

When the E/A has local feedback (Figure 21b), its gain is, to a first approximation, independent of transconductance:

$$A_{V(E/A)} = \frac{Z_F}{Z_{IN}} \qquad (f \lesssim 500kHz)$$

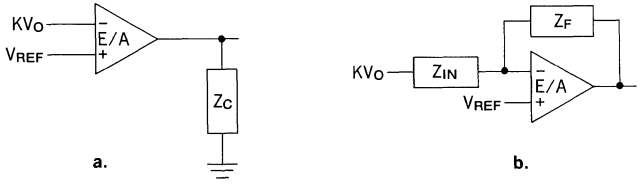


Figure 21. E/A Compensation (a.) Without and (b.) With Local Feedback

However, the use of local feedback creates an additional loop which must be independently stable. The UC1834 has no internal compensation to ensure this stability, so additional external compensation is usually required. An 820pF capacitor from the E/A output to ground will stabilize this inner voltage loop while also enhancing current loop stability.

An additional drawback to the use of local feedback is that Z_F places a DC load on the E/A output. With a transconductance amplifier this results in additional input offset voltage:

$$\Delta V_{IO} = \frac{I_{E/A\,OUT}}{g_M}$$

This offset results in degradation of DC regulation. The problem can be averted by taking local feedback from the emitter of the drive transistor if the driver is configured as an emitter-follower.

Whatever the compensation scheme, the UC1834 E/A output can sink or source a maximum of 100μA.

Table 2 shows two typical compensation schemes and the resulting E/A transfer functions. The first of these circuits is most widely used.

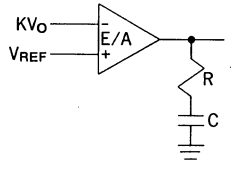
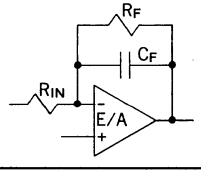
Compensation Circuit	E/A Gain ($A_{V(E/A)}(s)$)	Poles @ f =	Zeros @ f =
	$A_V = \frac{g_M(1 + sRC)}{sC}$	0	$\frac{1}{2\pi RC}$
	$A_V = \frac{R_F}{R_{IN}(1 + s R_F C_F)}$	$\frac{1}{2\pi R_F C_F}$	———

Table 2. E/A Compensation Circuits and Gain Response

APPENDIX III - FREQUENCY RESPONSE OF THE CURRENT LOOP

- **CS/A** - Figure 22 shows the open-loop gain and phase response of the UC1834 CS/A. This is also a transconductance amplifier, having $g_M \approx 1/70\Omega = 14mS$. The voltage gain is analogous to that of the E/A. The E/A compensation impedance (Z_C or $Z_{F(E/A)}$) is also seen by the CS/A output. For purposes of small signal AC analysis, the CS/A will always see this impedance as being returned to $V_{\overline{IN}}$ (as shown in Figures 16c, d) when the E/A is compensated by either of the methods shown in Table 2.

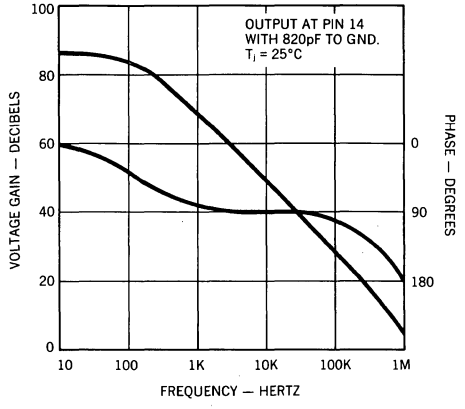


Figure 22. Current Sense Amplifier Gain and Phase Frequency Response

- **Pass Transistor** - Introduces current gain β to the loop transfer of both basic configurations (Figures 16c, d).Considerations outlined in Appendix I also apply here.

- **Sense Resistor** - Resistance value R_{SENSE} appears in transfer function for both configurations.

- **Drive Transistor** - In the circuit of Figure 16c, R_E allows operation of the driver as an emitter-follower. Effective conductance is $1/R_E$.

Closed-loop responses are given by the following:

for circuit of Figure 16c:

$$A_I = g_M \cdot Z_C \cdot \frac{1}{R_E} \cdot \beta \cdot R_{SENSE} \qquad \left(f < 500kHz,\ f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)\right)$$

for circuit of Figure 16d:

$$A_I = g_M \cdot \frac{Z_C}{Z_C + \beta Z_L} \cdot \beta \cdot R_{SENSE} \qquad \left(f < 500kHz,\ f < \frac{f_T}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)\right)$$

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A 25 WATT OFF-LINE FLYBACK SWITCHING REGULATOR

Introduction

This Application Note describes a low cost (less than $10.00) switching power supply for applications requiring multiple output voltages, e.g. personal computers, instruments, etc...The discontinuous mode flyback regulator used in this application provides good voltage tracking between outputs, which allows the use of primary side voltage sensing. This sensing technique reduces costs by eliminating the need for an isolated secondary feedback loop.

The low cost, (8 pin) UC1842 current mode control chip employed in this power supply provides performance advantages such as:

1) Fast transient response
2) Pulse by pulse current limiting
3) Stable operation

To simplify drive circuit requirements, a TO-220 power MOSFET (UFN833) is utilized for the power switch. This switch is driven directly from the output of the control chip.

Power Supply Specifications

1. Input voltage: 95VAC to 130VAC (50Hz/60Hz)
2. Output voltage:
   A. +5V, ±5%: 1A to 4A load
      Ripple voltage: 50mV P-P Max.
   B. +12V, ±3%: 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max.
   C. −12V, ±3%: 0.1A to 0.3A load
      Ripple voltage: 100mV P-P Max.
3. Line Isolation: 3750 Volts
4. Switching Frequency: 40KHz
5. Efficiency @ Full Load: 70%

Basic Circuit Operation

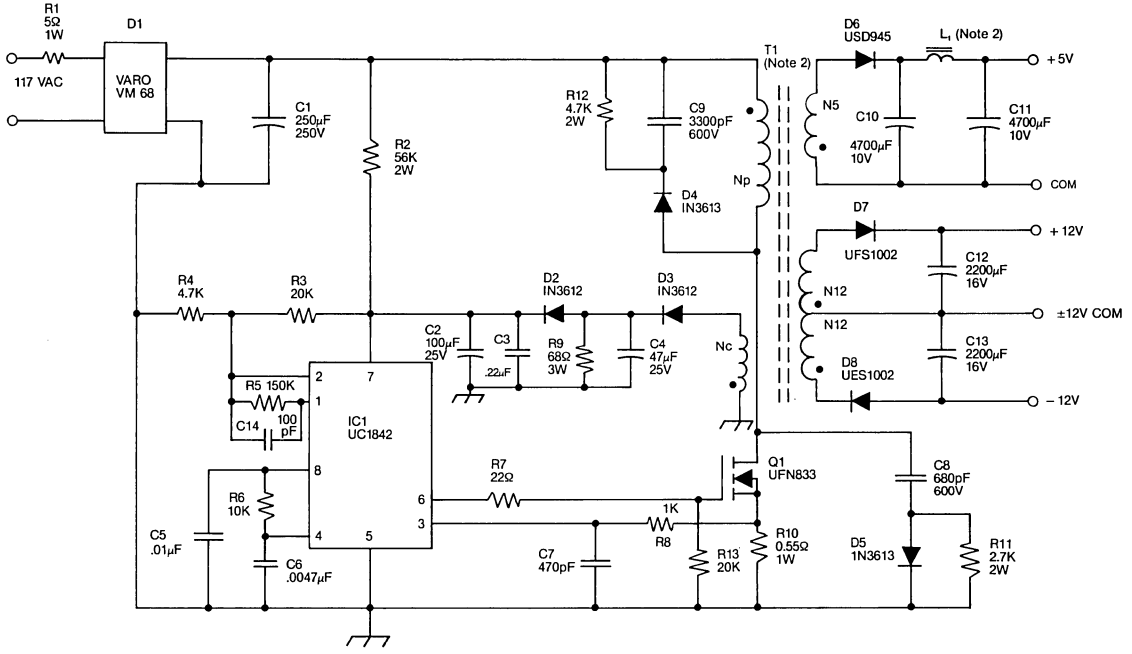
The 117VAC input line voltage is rectified and smoothed to provide DC operating voltage for the circuit. When power is initially applied to the circuit, capacitor C2 charges through R2. When the voltage across C2 reaches a level of 16V the output of IC1 is enabled, turning on power MOSFET Q1. During the on time of Q1, energy is stored in the air gap of transformer (inductor) T1. At this time the polarity of the output windings is such that all output rectifiers are reverse biased and no energy is transferred. Primary current is sensed by a resistor, R10, and compared to a fixed 1 volt reference inside IC1. When this level is reached, Q1 is turned off and the polarity of all transformer windings reverses, forward biasing the output rectifiers. All the energy stored is now transferred to the output capacitors. Many cycles of this store/release action are needed to charge the outputs to their respective voltages. Note that C2 must have enough energy stored initially to keep the control circuitry operating until C4 is charged to a level of approximately 13V. The voltage across C4 is fed through a voltage divider to the error amplifier (pin 2) and compared to an internal 2.5V reference.

Energy stored in the leakage inductance of T1 causes a voltage spike which will be added to the normal reset voltage across T1 when Q1 turns off. The clamp consisting of D4, C9 and R12 limits this voltage excursion from exceeding the BVDSS rating of Q1. In addition, a turn-off snubber made up of D5, C8 and R11 keeps power dissipation in Q1 low by delaying the voltage rise until drain current has decreased from its peak value. This snubber also damps out any ringing which may occur due to parasitics.

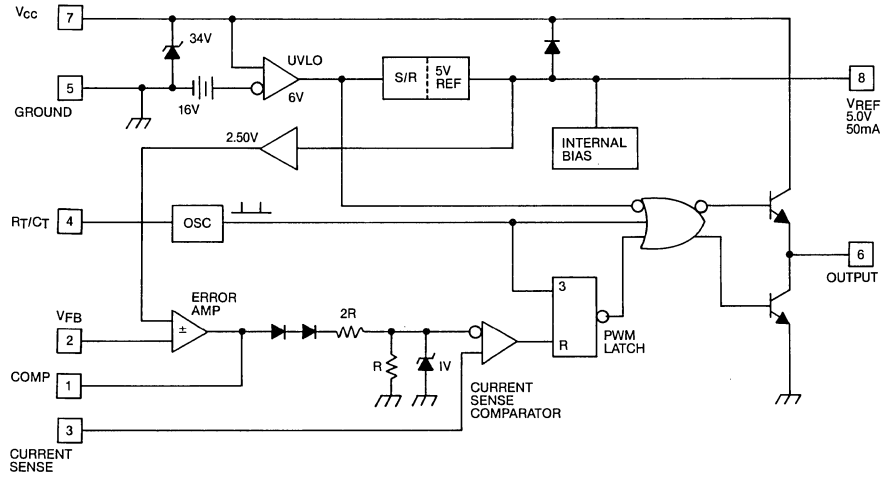
Less than 3.5% line and load regulation is achieved by loading the output of the control winding, Nc, with R9. This resistor dissipates the leakage energy associated with this winding. Note that R9 must be isolated from R2 with diode D2, otherwise C2 could not charge to the 16V necessary for initial start-up.

A small filter inductor in the 5V secondary is added to reduce output ripple voltage to less than 50mV. This inductor also attenuates any high frequency noise.

25W OFF-LINE FLYBACK REGULATOR



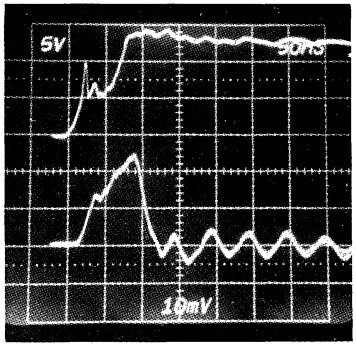
Notes: 1. All resistors are ¼ watt unless noted
2. See Appendix for construction details



BLOCK DIAGRAM: UC1842 CURRENT MODE CONTROLLER

TYPICAL SWITCHING WAVEFORMS

T_{on} — Drive waveforms

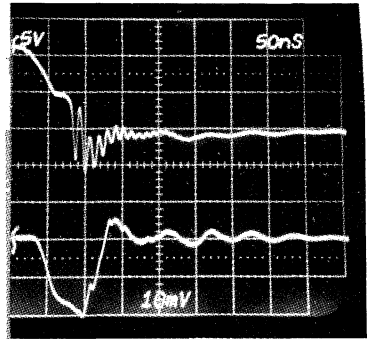


5V/DIV

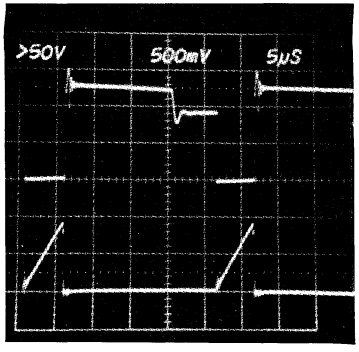
200mA/DIV

Upper trace: Q_1 — Gate to source voltage
Lower trace: Q_1 — Gate current

T_{off} — Drive waveforms



Upper trace: Q_1 — Gate to source voltage
Lower trace: Q_1 — Gate current



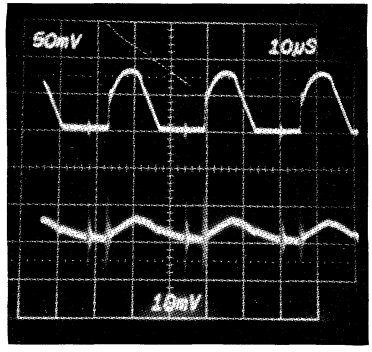
100V/DIV

0.5A/DIV

Upper trace: Q_1 — Drain to source voltage
Lower trace: Primary current — I_D

5A/DIV

50mV/DIV



Upper trace: +5V charging current
Lower trace: +5V output ripple voltage

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PERFORMANCE DATA

CONDITIONS		5V out	12V out	−12V out
Low Line (95VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.211	12.05	−12.01
	4.0A	4.854	12.19	−12.14
± 12 @ 300mA	+5V @ 1.0A	5.199	11.73	−11.69
	4.0A	4.950	11.68	−11.63
Nominal Line (120VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.220	12.07	−12.03
	4.0A	4.875	12.23	−12.18
± 12 @ 300mA	+5V @ 1.0A	5.208	11.73	−11.68
	4.0A	4.906	11.67	−11.62
High Line (130VAC)				
± 12 @ 100mA	+5V @ 1.0A	5.207	12.06	−12.02
	4.0A	4.855	12.21	−12.15
± 12V @ 300mA	+5V @ 1.0A	5.200	11.71	−11.67
	4.0A	4.902	11.66	11.61
Overall Line and Load Regulation		±3.5%	±2.3%	±2.4%

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PARTS LIST

IC's	
IC1	UC1842
POWER MOSFET	
Q1	UFN833
RECTIFIERS	
D1	VM68 varo
D2, D3	1N3612
D4, D5	1N3613
D6	USD945
D7, D8	UES1002
CAPACITORS	
C1	250μF, 250V
C2	100μF, 25V
C3	0.22μF, 25V
C4	47μF, 25V
C5	.01μF, 25V
C6	.0047μF, 25V
C7	470pF, 25V
C8	680pF, 600V
C9	3300pF, 600V
C10, C11	4700μF, 10V
C12, C13	2200μF, 16V
C14	100pF, 25V
RESISTORS	
R1	5Ω, 1W
R2	56K, 2W
R3	20K
R4	4.7K
R5	150K
R6	10K
R7	22Ω
R8	1K
R9	68Ω, 3W
R10	0.55Ω, 1W
R11	2.7K, 2W
R12	4.7K, 2W
R13	20K
MAGNETICS	
T_1	see appendix
L_1	see appendix

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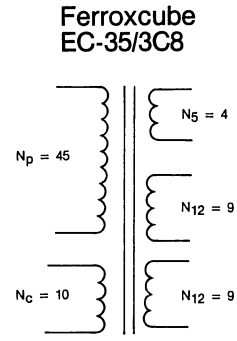
APPENDIX

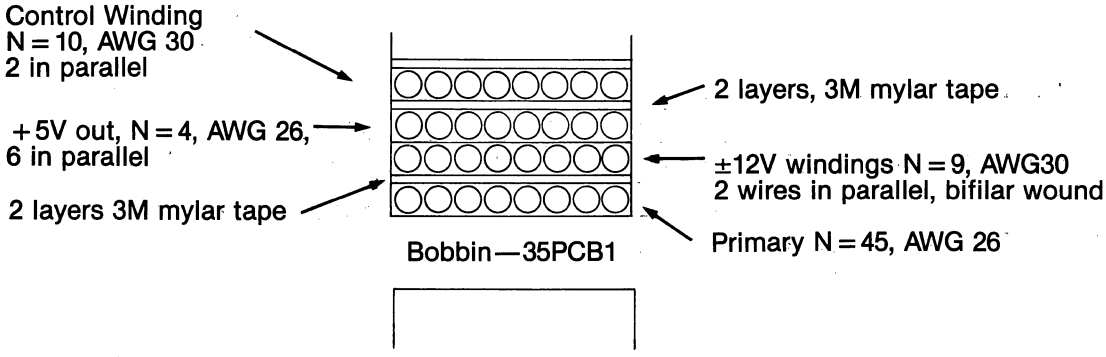
POWER TRANSFORMER—T1

Core: Ferroxcube EC-35/3C8
Gap: 10 mil in each outer leg

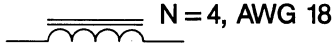
NOTE: For reduced EMI put gap in center leg only. Use 20 mil.



TRANSFORMER CONSTRUCTION



5V OUTPUT INDUCTOR



Ferroxcube
204 T 250 — 3C8 (toroid)

MODELLING, ANALYSIS AND COMPENSATION OF THE CURRENT-MODE CONVERTER

Abstract

As current-mode conversion increases in popularity, several peculiarities associated with fixed-frequency, peak-current detecting schemes have surfaced. These include instability above 50% duty cycle, a tendency towards subharmonic oscillation, non-ideal loop response, and an increased sensitivity to noise. This paper will attempt to show that the performance of any current-mode converter can be improved and at the same time all of the above problems reduced or eliminated by adding a fixed amount of "slope compensation" to the sensed current waveform.

1.0 INTRODUCTION

The recent introduction of integrated control circuits designed specifically for current mode control has led to a dramatic upswing in the application of this technique to new designs. Although the advantages of current-mode control over conventional voltage-mode control has been amply demonstrated[1-5], there still exist several drawbacks to a fixed frequency peak-sensing current mode converter. They are (1) open loop instability above 50% duty cycle, (2) less than ideal loop response caused by peak instead of average inductor current sensing, (3) tendency towards subharmonic oscillation, and (4) noise sensitivity, particularly when inductor ripple current is small. Although the benefits of current mode control will, in most cases, far out-weight these drawbacks, a simple solution does appear to be available. It has been shown by a number of authors that adding slope compensation to the current waveform (Figure 1) will stabilize a system above 50% duty cycle. If one is to look further, it becomes apparent that this same compensation technique can be used to minimize many of the drawbacks stated above. In fact, it will be shown that any practical converter will nearly always perform better with some slope compensation added to the current waveform.

The simplicity of adding slope compensation – usually a single resistor – adds to its attractiveness. However, this introduces a new problem – that of analyzing and predicting converter performance. Small signal AC models for both current and voltage-mode PWM's have been extensively developed in the literature. However, the slope compensated or "dual control" converter possesses properties of both with an equivalent circuit different from, yet containing elements of each. Although this has been addressed in part by several authors[1, 2], there still exists a need for a simple circuit model that can provide both qualitative and quantitative results for the power supply designer.

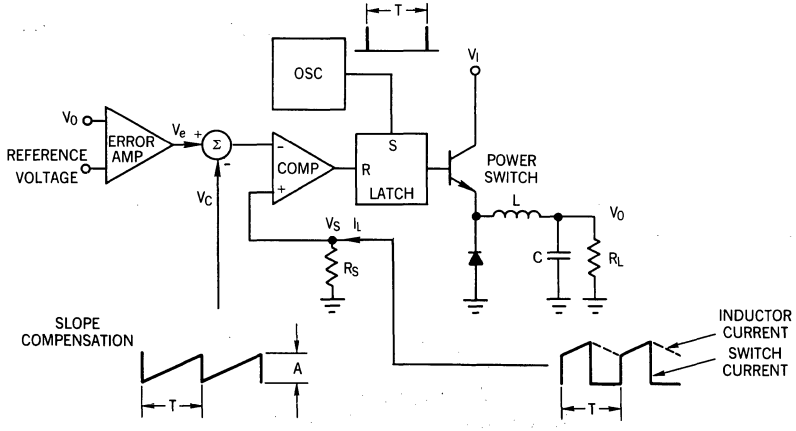


FIGURE 1 – A CURRENT-MODE CONTROLLED BUCK REGULATOR WITH SLOPE COMPENSATION.

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The first objective of this paper is to familiarize the reader with the peculiarities of a peak-current control converter and at the same time demonstrate the ability of slope compensation to reduce or eliminate many problem areas. This is done in section 2. Second, in section 3, a circuit model for a slope compensated buck converter in continuous conduction will be developed using the state-space averaging technique outlined in(1). This will provide the analytical basis for section 4 where the practical implementation of slope compensation is discussed.

2.1 OPEN LOOP INSTABILITY

An unconditional instability of the inner current loop exists for any fixed frequency current-mode converter operating above 50% duty cycle – regardless of the state of the voltage feedback loop. While some topologies (most notably two transistor forward converters) cannot operate above 50% duty cycle, many others would suffer serious input limitations if greater duty cycle could not be achieved. By injecting a small amount of slope compensation into the inner loop, stability will result for all values of duty cycle. Following is a brief review of this technique.

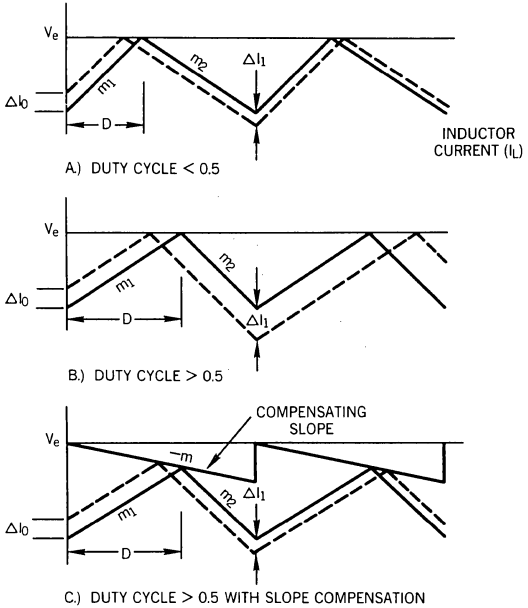

FIGURE 2 – DEMONSTRATION OF OPEN LOOP INSTABILITY IN A CURRENT-MODE CONVERTER.

Figure 2 depicts the inductor current waveform, I_L, of a current-mode converter being controlled by an error voltage V_e. By perturbing the current I_L by an amount ΔI, it may be seen graphically that ΔI will decrease with time for $D < 0.5$ (Figure 2A), and increase with time for $D > 0.5$ (Figure 2B). Mathematically this can be stated as

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2}{m_1}\right) \qquad (1)$$

Carrying this a step further, we can introduce a linear ramp of slope $-m$ as shown in Figure 2C. Note that this slope may either be added to the current waveform, or subtracted from the error voltage. This then gives

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2 + m}{m_1 + m}\right) \qquad (2)$$

Solving for m at 100% duty cycle gives

$$m > -\tfrac{1}{2}m_2 \qquad (3)$$

Therefore, to guarantee current loop stability, the slope of the compensation ramp must be greater than one-half of the down slope of the current waveform. For the buck regulator of Figure 1, m_2 is a constant equal to $\frac{V_0}{L} R_S$, therefore, the amplitude A of the compensating waveform should be chosen such that

$$A > T R_S \frac{V_0}{L} \qquad (4)$$

to guarantee stability above 50% duty cycle.

2.2 RINGING INDUCTOR CURRENT

Looking closer at the inductor current waveform reveals two additional phenomenon related to the previous instability. If we generalize equation 2 and plot I_n vs nT for all n as in Figure 3, we observe a damped sinusoidal response at one-half the switching frequency, similar to that of an RLC circuit. This ring-out is undesirable in that it (a) produces a ringing response of the inductor current to line and load transients, and (b) peaks the control loop gain at ½ the switching frequency, producing a marked tendency towards instability.

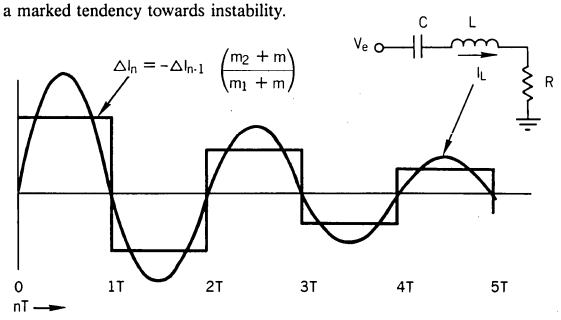

FIGURE 3 – ANALOGY OF THE INDUCTOR CURRENT RESPONSE TO THAT OF AN RLC CIRCUIT.

It has been shown in (1), and is easily verified from equation 2, that by choosing the slope compensation m to be equal to $-m_2$ (the down slope of the inductor current), the best possible transient response is obtained. This is analogous to critically damping the RLC circuit, allowing the current to correct itself in exactly one cycle. Figure 4 graphically demonstrates this point. Note that while this may optimize inductor current ringing, it has little bearing on the transient response of the voltage control loop itself.

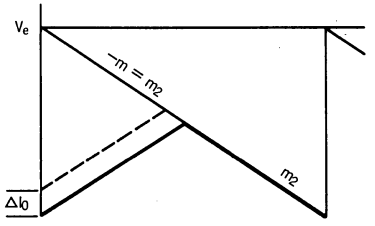

FIGURE 4 – FOR THE CASE OF $m = -m_2$, A CURRENT PERTURBATION WILL DAMP OUT IN EXACTLY ONE CYCLE.

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2.3 SUBHARMONIC OSCILLATION

Gain peaking by the inner current loop can be one of the most significant problems associated with current-mode controllers. This peaking occurs at one-half the switching frequency, and – because of excess phase shift in the modulator – can cause the voltage feedback loop to break into oscillation at one-half the switching frequency. This instability, sometimes called subharmonic oscillation, is easily detected as duty cycle asymmetry between consecutive drive pulses in the power stage. Figure 5 shows the inductor current of a current-mode controller in subharmonic oscillation (dotted waveforms with period 2T).

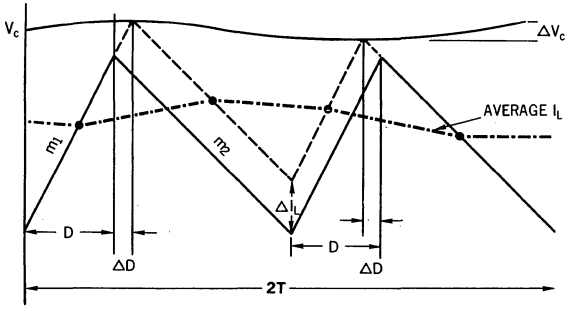


FIGURE 5 – CURRENT WAVE FORM (DOTTED) OF A CURRENT-MODE CONVERTER IN SUBHARMONIC OSCILLATION.

To determine the bounds of stability, it is first necessary to develop an expression for the gain of the inner loop at one-half the switching frequency. The technique used in (2) will be paralleled for a buck converter with the addition of terms to include slope compensation.

2.3.1 LOOP GAIN CALCULATION AT ½f_s

Referring to figures 5 and 6, we want to relate the input stimulus, ΔV_e, to an output current, ΔI_L. From figure 5, two equations may be written

$$\Delta I_L = \Delta D\, m_1\, T - \Delta D\, m_2\, T \qquad (4)$$

$$\Delta V_C = \Delta D\, m_1\, T + \Delta D\, m_2\, T \qquad (5)$$

Adding slope compensation as in figure 6 gives another equation

$$\Delta V_e = \Delta V_C + 2\Delta D\, m\, T \qquad (6)$$

Using (5) to eliminate ΔV_C from (6) and solving for $\Delta I_L/\Delta V_e$ yields

$$\frac{\Delta I_L}{\Delta V_e} = \frac{m_1 - m_2}{m_1 + m_2 + m} \qquad (7)$$

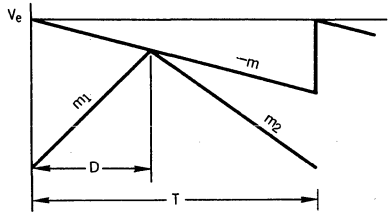


FIGURE 6 – ADDITION OF SLOPE COMPENSATION TO THE CONTROL SIGNAL

For steady state condition we can write

$$D\, m_1\, T = (1 - D)\, m_2\, T \qquad (8)$$

or

$$D = \frac{-m_2}{m_1 - m_2} \qquad (9)$$

By using (9) to reduce (7), we obtain

$$\frac{\Delta I_L}{\Delta V_e} = \frac{1}{1 - 2D\,(1 + m/m_2)} \qquad (10)$$

Now by recognizing that ΔI_L is simply a square wave of period 2T, we can relate the first harmonic amplitude to ΔI_L by the factor $4/\pi$ and write the small signal gain at $f = \frac{1}{2}f_S$ as

$$\frac{i_L}{v_e} = \frac{4\pi}{1 - 2D\,(1 + m/m_2)} \qquad (11)$$

If we assume a capacitive load of C at the output and an error amplifier gain of A, then finally, the expression for loop gain at $f = \frac{1}{2}\, f_S$ is

$$\text{Loop gain} = \frac{\frac{4TA}{\pi^2\, C}}{1 - 2D\,(1 + m/m_2)} \qquad (12)$$

2.3.2 USING SLOPE COMPENSATION TO ELIMINATE SUBHARMONIC OSCILLATION

From equation 12, we can write an expression for maximum error amplifier gain at $f = \frac{1}{2}f_S$ to guarantee stability as

$$A_{max} = \frac{1 - 2D\,(1 + m/m_2)}{\frac{4T}{\pi^2\, C}} \qquad (13)$$

This equation clearly shows that the maximum allowable error amplifier gain, A_{max}, is a function of both duty cycle and slope compensation. A normalized plot of A_{max} versus duty cycle for several values of slope compensation is shown in figure 7. Assuming the amplifier gain cannot be reduced to zero at $f = \frac{1}{2}f_S$, then for the case of $m = 0$ (no compensation) we see the same instability previously discussed at 50% duty cycle. As the compensation is increased to $m = -\frac{1}{2}m_2$, the point of instability moves out to a duty cycle of 1.0, however in any practical

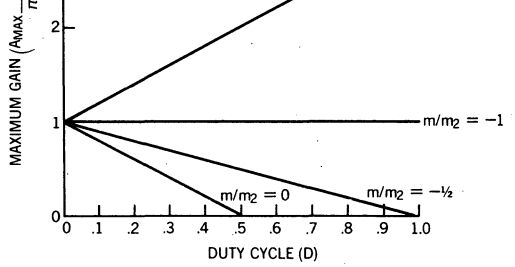


FIGURE 7 – MAXIMUM ERROR AMPLIFIER GAIN AT ½ f_s (NORMALIZED) V.S. DUTY CYCLE FOR VARYING AMOUNTS OF SLOPE COMPENSATION. REFER TO EQUATION 13.

system, the finite value of A_{max} will drive the feedback loop into subharmonic oscillation well before full duty cycle is reached. If we continue to increase m, we reach a point, $m = -m_2$, where the maximum gain becomes independent of duty cycle. This is the point of critical damping as discussed earlier, and increasing m above this value will do little to improve stability for a regulator operating over the full duty cycle range.

2.4 PEAK CURRENT SENSING VERSUS AVERAGE CURRENT SENSING

True current-mode conversion, by definition, should force the average inductor current to follow an error voltage – in effect replacing the inductor with a current source and reducing the order of the system by one. As shown in Figure 8, however, peak current detecting schemes are generally used which allow the average inductor current to vary with duty cycle while producing less than perfect input to output – or feedforward characteristics. If we choose to add slope compensation equal to $m = -\frac{1}{2} m_2$ as shown in Figure 9, we can convert a peak current detecting scheme into an average current detector, again allowing for perfect current mode control. As mentioned in the last section, however, one must be careful of subharmonic oscillations as a duty cycle of 1 is approached when using $m = -\frac{1}{2} m_2$.

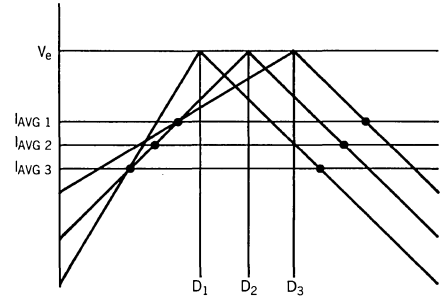


FIGURE 8 – PEAK CURRENT SENSING WITHOUT SLOPE COMPENSATION ALLOWS AVERAGE INDUCTOR CURRENT TO VARY WITH DUTY CYCLE

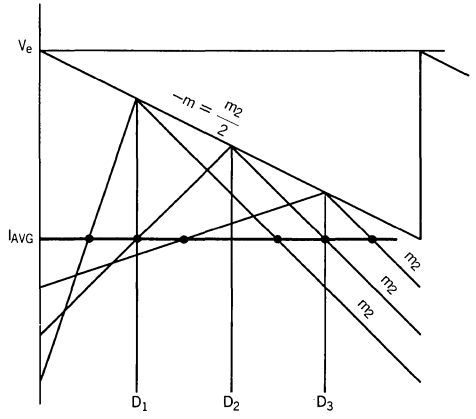


FIGURE 9 – AVERAGE INDUCTOR CURRENT IS INDEPENDENT OF DUTY CYCLE AND INPUT VOLTAGE VARIATION FOR A SLOPE COMPENSATION OF $m = -\frac{1}{2} m_2$.

2.5 SMALL RIPPLE CURRENT

From a systems standpoint, small inductor ripple currents are desirable for a number of reasons – reduced output capacitor requirements, continuous current operation with light loads, less output ripple, etc. However, because of the shallow slope presented to the current sense circuit, a small ripple current can, in many cases, lead to pulse width jitter caused by both random and synchronous noise (Figure 10). Again, if we add slope compensation to the current waveform, a more stable switchpoint will be generated. To be of benefit, the amount of slope added needs to be significant compared to the total inductor current – not just the ripple current. This usually dictates that the slope m be considerably greater than m_2 and while this is desirable for subharmonic stability, any slope greater than $m = -\frac{1}{2} m_2$ will cause the converter to behave less like an ideal current mode converter and more like a voltage mode converter. A proper trade-off between inductor ripple current and slope compensation can only be made based on the equivalent circuit model derived in the next section.

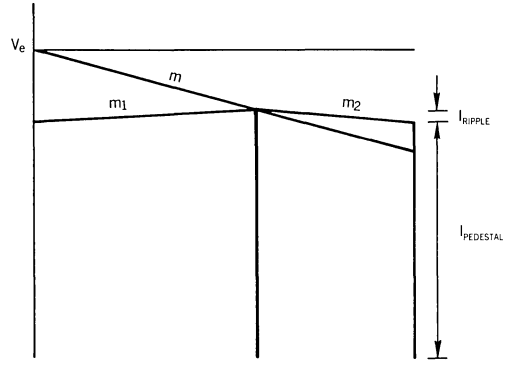


FIGURE 10 – A LARGE PEDESTAL TO RIPPLE CURRENT RATIO.

3.0 SMALL SIGNAL A.C. MODEL

As we have seen, many drawbacks associated with current-mode control can be reduced or eliminated by adding slope compensation in varying degrees to the current waveform. In an attempt to determine the full effects of this same compensation on the closed loop response, a small signal equivalent circuit model for a buck regulator will now be developed using the state-space averaging technique developed in (1).

3.1 A.C. MODEL DERIVATION

Figure 11a shows an equivalent circuit for a buck regulator power stage. From this we can write two state-space averaged differential equations corresponding to the inductor current and capacitor voltage as functions of duty cycle D

$$\dot{I}_L = \frac{(V_I - V_0)}{L} D - \frac{V_0 (1 - D)}{L} \qquad (14)$$

$$\dot{V}_0 = \frac{I_L}{C} - \frac{V_0}{R} \qquad (15)$$

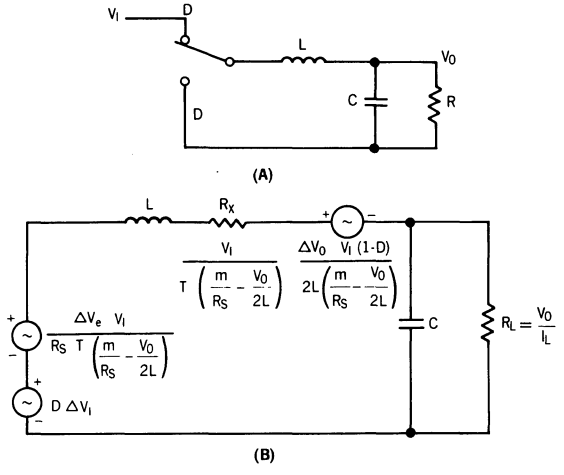


FIGURE 11 – BASIC BUCK CONVERTER (A) AND ITS SMALL SIGNAL EQUIVALENT CIRCUIT MODEL (B).

If we now perturb these equations – that in substitute $V_I + \Delta V_I$, $V_0 + \Delta V_0$, $D + \Delta D$ and $I_L + \Delta I_L$ for their respective variables – and ignore second order terms, we obtain the small signal averaged equations

$$\Delta \dot{I}_L = \frac{D\Delta I_L}{L} - \frac{\Delta V_0}{L} + \frac{V_I \Delta D}{L} \qquad (16)$$

$$\Delta \dot{V}_0 = \frac{\Delta I_L}{C} - \frac{\Delta V_0}{CR} \qquad (17)$$

A third equation – the control equation – relating error voltage, V_e, to duty cycle may be written from Figure 6 as

$$I_L R_S = V_e - mDT - \frac{(1-D)\, V_0\, T\, R_S}{2L} \qquad (18)$$

Perturbing this equation as before gives

$$\Delta I_L = \frac{\Delta V_e}{R_S} - \Delta DT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right) - \frac{T}{2L}(1-D)\,\Delta V_0 \qquad (19)$$

By using 19 to eliminate ΔD from 16 and 17 we arrive at the state-space equations

$$\Delta \dot{I}_L = \frac{D}{L}\Delta V_I + \frac{\Delta V_e\, V_I}{R_S\, LT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} - \frac{\Delta V_0\, V_I\,(1-D)}{2L^2\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} - \frac{\Delta I_L V_I}{LT\left(\frac{m}{R_S} - \frac{V_0}{2L}\right)} \qquad (20)$$

$$\Delta \dot{V}_0 = \frac{\Delta I_L}{C} - \frac{\Delta V_0}{CR} \qquad (21)$$

An equivalent circuit model for these equations is shown in Figure 11B and discussed in the next section.

3.2 A.C. MODEL DISCUSSION

The model of Figure 11B can be used to verify and expand upon our previous observations. Key to understanding this model is the interaction between R_X and L as the slope compensation, m is changed. In most cases, the dependent source between R_X and C can be ignored.

If R_X is much greater than L, as is the case for little or no compensation ($m = 0$), the converter will have a single pole response and act as a true current mode converter. If R_X is small compared to $L\left(m \gg \frac{R_S V_0}{2L}\right)$, then a double pole response will be formed by the LRC output filter similar to any voltage-mode converter. By appropriately adjusting m, any condition between these two extremes can be generated.

Of particular interest is the case when $m = \frac{R_S V_0}{2L}$. Since the down slope of the inductor current (m_2 from Figure 6) is equal to $\frac{R_S V_0}{L}$, we can write $m = -\frac{1}{2}m_2$. At this point, R_X goes to infinity, resulting in an ideal current mode converter. This is the same point, discussed in section 2.4, where the average inductor current exactly follows the error voltage. Note that although this compensation is ideal for line rejection and loop response, maximum error amp gain limitations as higher duty cycles are approached (section 2.3) may necessitate using more compensation.

Having derived an equivalent circuit model, we may now proceed in its application to more specific design examples. Figure 12 plots open loop ripple rejection ($\Delta V_0/\Delta V_I$) at 120Hz versus slope compensation for a typical 12 volt buck regulator operating under the following conditions:

V_0	=	12V
V_I	=	25V
L	=	200μH
C	=	300μf
T	=	20μS
R_S	=	.5Ω
R_L	=	1Ω, 12Ω

Again, as the slope compensation approaches $-\frac{1}{2}m_2$, the theoretical ripple rejection is seen to become infinite. As larger values of m are introduced, ripple rejection slowly degrades to that of a voltage-mode converter (−6.4dB for this example).

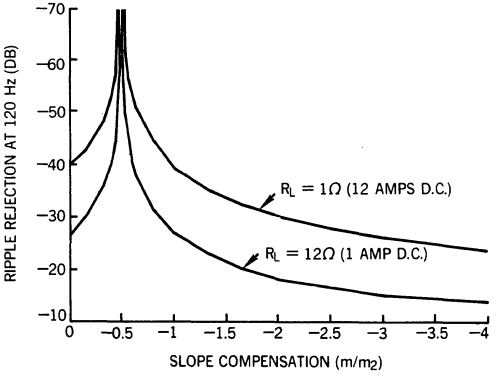


FIGURE 12 – RIPPLE REJECTION AT 120Hz V.S. SLOPE COMPENSATION FOR 1AMP AND 12AMP LOADS.

If a small ripple to D.C. current ratio is used, as is the case for R_L = 1ohm in the example, proportionally larger values of slope compensation may be injected while still maintaining a high ripple rejection ratio. In other words, to obtain a given ripple rejection ratio, the allowable slope compensation varies proportionally to the average D.C. current, not the ripple current. This is an important concept when attempting to minimize noise jitter on a low ripple converter.

Figure 13 shows the small signal loop response ($\Delta V_0/\Delta V_e$) versus frequency for the same example of Figure 12. The gains have all been normalized to zero dB at low frequency to reflect the actual difference in frequency response as slope compensation m is varied. At m = $-\frac{1}{2}$ m_2, an ideal single-pole roll-off at 6dB/octave is obtained. As higher ratios are used, the response approaches that of a double-pole with a 12dB/octave roll-off and associated 180° phase shift.

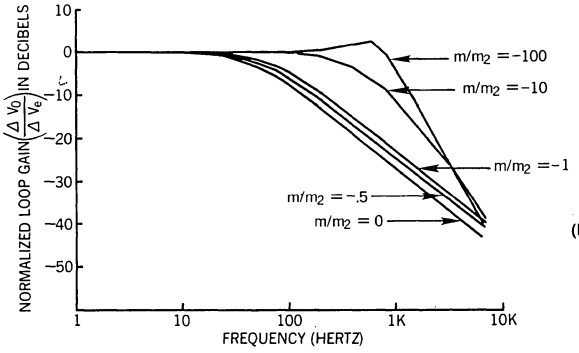
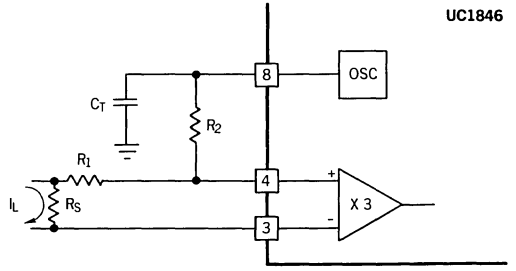
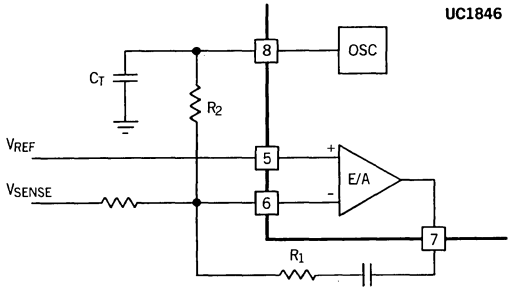


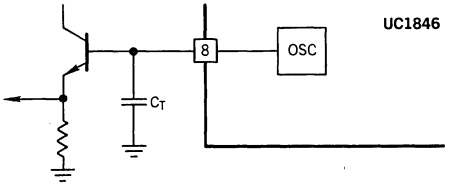
FIGURE 13 – NORMALIZED LOOP GAIN V.S. FREQUENCY FOR VARIOUS SLOPE COMPENSATION RATIO'S.



(a) SUMMING OF SLOPE COMPENSATION DIRECTLY WITH SENSED CURRENT SIGNAL



(b) SUMMING OF SLOPE COMPENSATION WITH ERROR SIGNAL



(c) EMITTER FOLLOWER USED TO LOWER OUTPUT IMPEDANCE OF OSCILLATOR.

FIGURE 14 – ALTERNATIVE METHODS OF IMPLEMENTING SLOPE COMPENSATION WITH THE UC1846 CURRENT-MODE CONTROLLER.

4.0 SLOPE COMPENSATING THE UC1846 CONTROL I.C.

Implementing a practical, cost effective current-mode converter has recently been simplified with the introduction of the UC1846 integrated control chip. This I.C. contains all of the control and support circuitry required for the design of a fixed frequency current-mode converter. Figures 14A and B demonstrate two alternative methods of implementing slope compensation using the UC1846. Direct summing of the compensation and current sense signal at Pin 4 is easily accomplished, however, this introduces an error in the current limit sense circuitry. The alternative method is to introduce the compensation into the negative input terminal of the error amplifier. This will only work if (a) the gain of the error amplifier is fixed and constant at the switching frequency (R_1/R_2 for this case) and (b) both error amplifier and current amplifier gains are taken into consideration when calculating the required slope compensation. In either case, once the value of R_2 has been calculated, the loading effect on C_T can be determined and, if necessary, a buffer stage added as in Figure 14C.

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A NEW IC OPTIMIZES HIGH SPEED POWER MOSFET DRIVE FOR SWITCHING POWER SUPPLIES

Abstract

Although touted as a high-impedance, voltage-controlled device, prospective users soon learn that it takes high drive currents to achieve high-speed switching with Power MOSFETS. This paper describes the construction techniques which lead to the parasitic effects which normally limit FET performance, and discusses several circuit approaches useful to improve switching speed. IC drivers optimized for driving FETS are compared and a new high-speed efficient driver is introduced.

INTRODUCTION

An investigation of Power MOSFET construction techniques will identify several parasitic elements which make the highly-touted "simple gate drive" of MOSFET devices less than obvious. These parasitic elements, primarily capacitive in nature, can require high peak drive currents with fast rise times coupled with care that excessive di/dt does not cause current overshoot or ringing with rectifier recovery current spikes.

This paper develops a switching model for Power MOSFET devices and relates the individual parameters to construction techniques. From this model, ideal drive characteristics are defined and practical IC implementations are discussed. Specific applications to switch-mode power systems involving both direct and transformer coupled drive are described and evaluated.

POWER MOSFET CHARACTERISTICS

The advantages which power MOSFET's have over their bipolar competitors have given them an ever-increasing utilization in power systems and, in the process, opened the way to new performance levels and new topologies.

A major factor in this regard is the potential for extremely fast switching. Not only is there no storage time inherent with MOSFET's, but the switching times can be user controlled to suit the application. This, of course, requires that the designer have an understanding of the switching dynamics inherent in these devices. Even though power MOSFET's are majority carrier devices, the speed at which they can switch is dependent upon many parameters and parasitic effects related to the device's construction.

THE POWER MOSFET MODEL

An understanding of the parasitic elements in a power MOSFET can be gained by comparing the construction details of a MOSFET with its electrical model as shown in Figure 1. This construction diagram is a simplified sketch of a single cell – a high power device such as the UFN 150 would have $\approx$ 20,000 of these cells all connected in parallel.

In operation, when the gate voltage is below the gate threshold, Vg(th), the drain voltage is supported by the N- drain region and its adjacent implanted P region and there is no conduction.

When the gate voltage rises above Vg(th), however, the P area under the gate inverts to N forming a conductive layer between the N+ source and the N− drain. This allows electrons to migrate from source to drain where the electric field in the drain sweeps them to the drain terminal at the bottom of the structure.

In the equivalent electrical model, the parameters are defined as follows:

1. Lg and Rg represent the inductance and resistance of the wire bonds between the package terminal and the actual gate, plus the resistance of the polysilicon gate runs.

2. C1 represents the capacitance from the gate to both the N+ source and the overlying source interconnecting metal. Its value is fixed by the design of the structure.

3. C2 + C4 represents additional gate-source capacitance into the P region. C2 is the dielectric capacitance and is fixed while C4 is

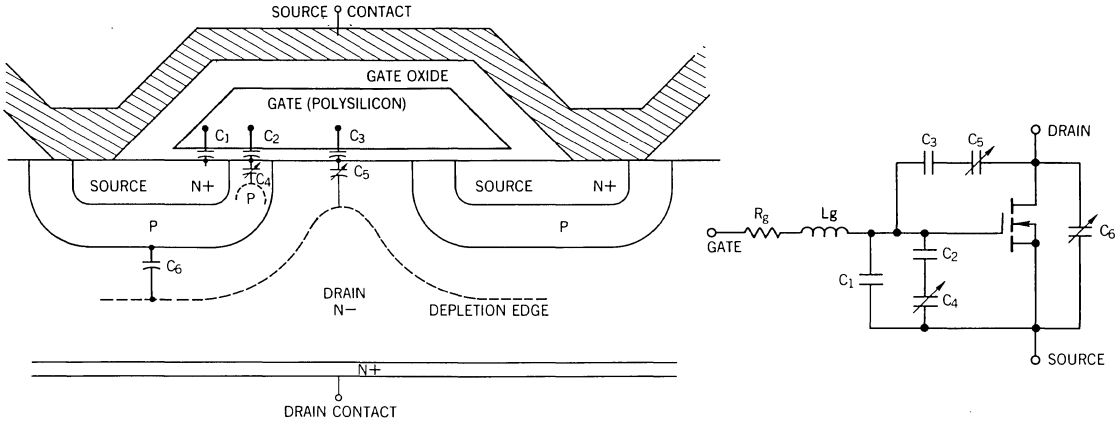

FIGURE 1 - SIMPLIFIED CROSS SECTION OF A POWER MOSFET CELL AND ITS ELECTRICAL EQUIVALENT.

due to the depletion region between source and drain and varies with the gate voltage. Its contribution causes total gate-source capacitance to increase 10-15% as the gate voltage goes from zero to Vg(th).

4. C3 + C5 is also made up of a fixed dielectric capacitance plus a value which becomes significant when the drain to gate voltage potential reverses polarity.

5. C6 is the drain-source capacitance and while it also varies with drain voltage, it is not a significant factor with respect to switching times.

EVALUATING FET PARASITIC ELEMENTS

Although it is clearly not the best way to drive a power MOSFET, using a constant gate current to turn the device on allows visualization of the capacitive effects as they affect the voltage waveforms. Thus the demonstration circuit of Figure 2 is configured to show the gate dynamics in a typical buck-type switching regulator circuit. This simulates the inductive switching of a large class of applications and is implemented here with a UFN-510 FET, which is a 4 amp, 100V device with the following capacitances:

$$\left.\begin{array}{lll} Ciss \approx C1 + C4 + C5 & = & 135 - 150\ pF \\ Crss \approx C5 & = & 20 - 25\ pF \\ Coss \approx C5 + C6 & = & 80 - 100\ pF \end{array}\right\} \quad Vgs = 0V$$

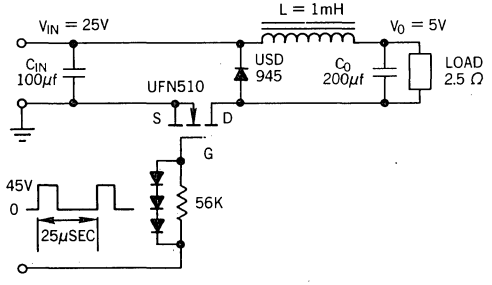

FIGURE 2 - SWITCHING TIME EVALUATION CIRCUIT.

In this illustration, the load portion of the circuit is established with Vin = 25V, Io = 2A, and f = 25Khz. The resultant turn-on waveforms are shown in Figure 3 from which the following observations may be made:

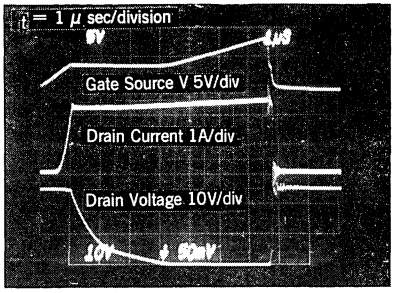

FIGURE 3 - FET TURN-ON SWITCHING CHARACTERISTICS WHEN DRIVEN WITH A CONSTANT GATE CURRENT

1. For a fixed gate drive current, the drain current rise time is 5 times faster than the voltage fall time.

2. There is a 10-15% increase in gate capacitance when the gate voltage reaches Vg(th).

3. The gate voltage remains unchanged during the entire time the drain voltage is falling because the Miller effect increases the effective gate capacitance.

4. The input gate capacitance is approximately twice as high when drain current is flowing as when it is off.

5. The drain voltage fall time has two slopes because the effective drain-gate capacitance takes a signifcant jump when the drain-gate potential reverses polarity.

6. Unless limited by external circuit inductance, the current rise time depends upon the large signal g_M and the rate of change of gate voltage as $\Delta Id = g_M \Delta Vg$

CHANGES IN EFFECTIVE CAPACITANCE

The waveform drawings of Figure 4 illustrate the dynamic effects which take place during turn-on. As the gate voltage rises from zero to threshold, C2 is not significant since C4 is very small. At threshold, the drain current rises quickly while the drain voltage is unchanged. This, of course, is due to the buck regulator circuit configuration which will not let the voltage fall until all the inductor current is transfered from the free-wheeling diode to the FET.

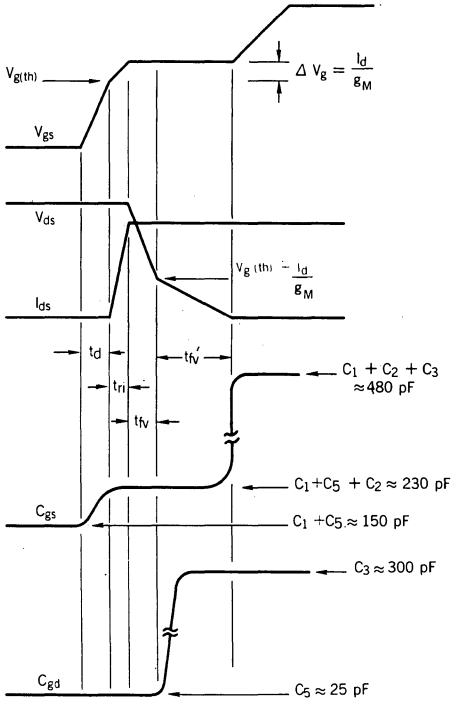

FIGURE 4 - PARASITIC CAPACITANCE VARIATION FOR A UFN510 MOS FET DURING TURN-ON

While the drain current is increasing, there is a slight increase in the gate capacitance due to the large current density underneath the gate in the N-region close to the P areas.

As the drain voltage begins to fall, its slope depends upon gate to drain capacitance and not that from gate to source. During this time, all the gate current is utilized to charge this gate to drain capacitance and no change in gate voltage is observed. This capacitance initially increases slightly as the voltage across it drops but then there is a significant jump in value when the drain voltage falls lower than the gate. When the polarity reverses from drain to gate, a surface charge accumulation takes place and the entire gate structure becomes part of the gate to drain capacitance. At this point the drain voltage fall time slows for the duration of its transition.

AN OPTIMUM GATE DRIVE

In most switching power supply applications, if a step function in gate current is provided, the drain current rise time is several times faster than the voltage fall time. This can result in substantial switching power losses which are most often combated by increasing the gate drive current. This creates a problem, however, in that it further reduces current rise time which can cause overshoot, ringing, EMI and power dissipation due to recovery time for the rectifiers which are much happier with a more slowly changing drain current.

In an effort to meet these conflicting requirements, an idealized gate current waveform was derived based upon the goal of making the voltage fall time equal to the current rise time. This optimum gate current waveform is shown in Figure 5 and consists of the following elements.

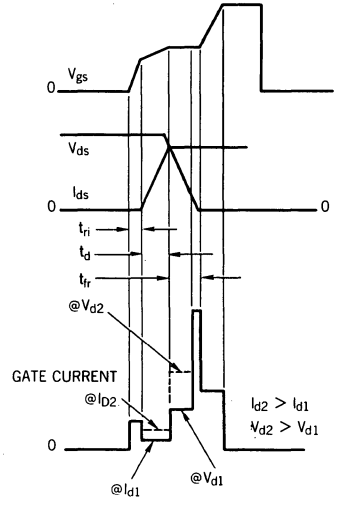

FIGURE 5 - AN "IDEAL" GATE CURRENT TURN-ON DRIVE TO PROVIDE EQUAL CURRENT RISE AND VOLTAGE FALL TIMES WITH AN INDUCTIVE LOAD

1. An initial fast pulse to get the gate voltage up to threshold.
2. A lesser amount to slow the drain current rise time. This value however, will also be a function of the required drain current.
3. Another increase to get the drain voltage to fall rapidly with a large current pulse added when the drain gate potential reverses.
4. A continued amount to allow the gate voltage to charge to its final value.

Obviously this might be a little difficult to implement in exact form, however, it can be approximated by a gate current waveform which, instead of being constant, has a rise time equal to the desired sum of the drain current rise time and the voltage fall time, and a peak value high enough to charge the large effective capacitance which appears during the switching transition. The peak current requirement can be calculated on the basis of defining the amount of charge required by the parasitic capacitance through the switching period.

A linear current ramp will deliver a charge equal to

$$Q = \frac{Ip \cdot ton}{2} \quad \text{where we define} \quad ton = td + tri + tfv$$

The total charge required for switching is

$$Q = Ciss\,[Vg\,(th) + \frac{Id}{g_M}] + Crss\,[V_{DD} - Vg\,(th)] + Crss' Vg\,(th)$$

where Crss' is the gate-drain capacitance after the polarity has reversed during turn-on and is related to Ciss by the basic geometry design of the device. A reasonable approximation is that Crss'≈1.5 Ciss. With this assumption,

$$Ip \approx \frac{2}{ton}\,[Ciss\,(2.5\ Vg\,(th) + \frac{Id}{g_M}) + Crss\,(V_{DD} - Vg\,(th))]$$

As an example, if one were to implement a 40 V, 10A buck regulator with a UFN150, it would not be unreasonable to extend the total switching time to 50 nsec to accomodate rectifier recovery time. An optimim drive current for this application would then take 50 nsec to ramp from zero to a peak value calculated from

Ciss = 2000 pF	ton = 50 nsec
Crss = 350 pF	V_{DD} = 40 V
Vg(th) = 3 V	Id = 10 A
$g_M = \frac{10A}{2.5\ V} = 4$ s	

$$\text{as } Ip = \frac{2}{50 \times 10^{-9}}[2000 \times 10^{-12}(2.5 \times 3 + \frac{10}{4}) + 350 \times 10^{-12}(40 - 3)]$$

$\therefore$ Ip = 1.32 amps peak

The above has shown that while high peak currents are necessary for fast power MOSFET switching, controlling the rise time of the gate current will yield a more well-behaved system with less stress caused by rectifier recovery times and capacitance. This type of switching requirement can be fulfilled with integrated circuit technology and several IC's have been developed and applied as MOSFET drivers.

FET DRIVER IC'S

In searching for IC's capable of providing the high peak currents required by power MOSFETS, one of the first devices which became popular was DS0026 shown in Figure 6. While this IC was originally designed to be a clock driver for MOS logic, it was capable of supplying up to 1.5 amps as either a source or sink. In addition, it was made with a gold doped, all-NPN process which minimizes storage delays and, as a result, offers transition times of approximately 20 nsec. Its disadvantage is that pull-up resistors R3 and R4 require excessive supply current when the output is in the low state.

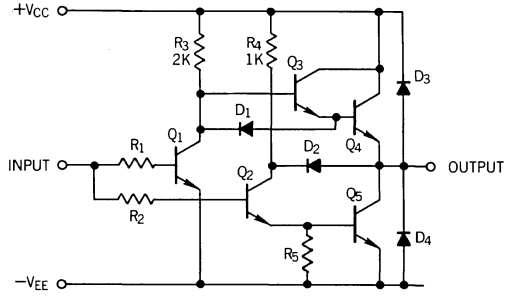

FIGURE 6 - A SIMPLIFIED SCHEMATIC OF THE DS0026 DRIVER IC

The first PWM IC's to include FET compatible output stages were the 1525A, followed by the 1526. Both of these designs feature push-pull outputs, each of which is configured as shown in Figure 7. Again with source and sink – this time driven by constant current sources – these devices can provide high FET switching drive with low stand-by current regardless of the state of the outputs. Frustratingly, these designs also suffer from some limitations. First, the maximum peak current is approximately ½ amp which is just not adequate for larger geometry FET's and, secondly, there are delays in turning off the output transistors which allow a high cross conduction current from Vc to ground as the conduction of source and sink overlap at each switch transition. This current spiking is shown in Figure 8 and while its not too much of a problem at low frequencies, at 200 KHz the internal power dissipation of the IC increases by a factor of 3 - 4.

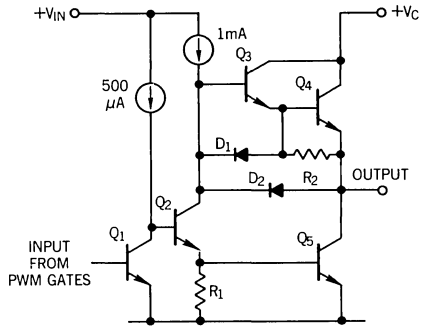

FIGURE 7 - ONE OF TWO OUTPUT STAGES FOUND IN THE 1525A and 1527A IC's

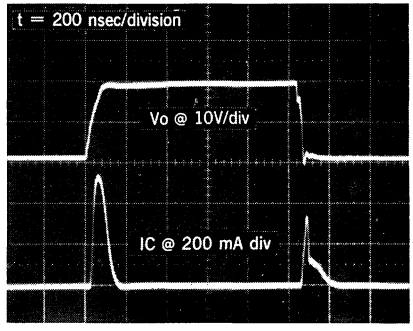

FIGURE 8 - CROSS-CONDUCTION CURRENT IN THE 1525A OUTPUT STAGE

INTRODUCING THE UC1706

This brings us to a new IC designed specifically as a power MOSFET driver compatible with PWM circuits for switching power supplies. As seen from the block diagram shown in Figure 9, this device is an interface circuit based upon the philosophy that the analog PWM control circuitry can best be done on a separate chip from the digital output driving stages. The UC1706 is made with a high-speed, high-voltage Schottky clamped process and while it isn't as fast as the DS0026, it does have delay times of only 100nsec while requiring much less supply current.

Referring again to Figure 9 it can be seen that the UC1706 is designed to provide three basic functions:

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UC1706 BLOCK DIAGRAM

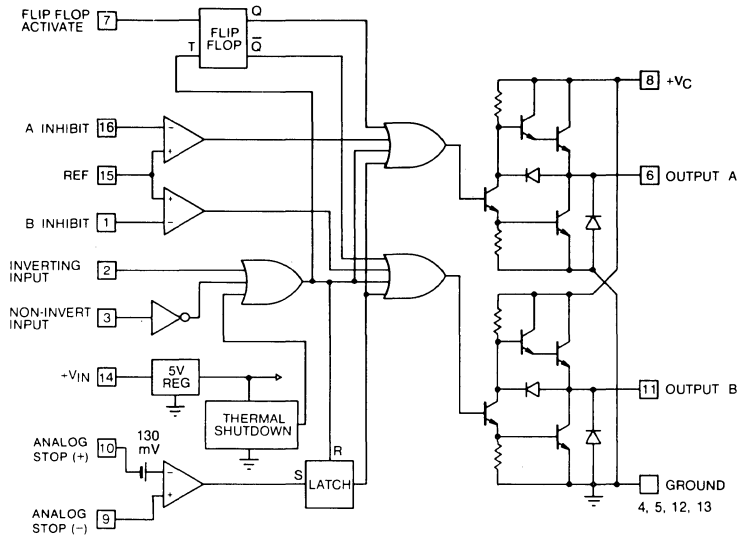

FIGURE 9 - UC1706 BLOCK DIAGRAM.

1. The main feature of this chip is a pair of totem-pole output stages, each designed to provide peak currents of 1.5 amp source or sink, with a fast turn-off optimized to minimize cross-conduction current.

2. With an internal flip-flop, the UC1706 will accept a single-ended PWM signal and drive the outputs alternately for push-pull or bridge applications. This flip-flop can be externally disabled so both outputs work in parallel. They can then be combined for 3A peak operation. Inputs can be of either polarity insuring compatibility with all available PWM chips, i.e. UC1840, UC1842, NE5560, MC30060, NE5561, etc.

3. Several protection functions associated with output drive are also included in the UC1706. These include a latching analog comparator with a 130mV threshold useful for pulse-by-pulse current limiting, an inhibit circuit designed for automatic dead-band control when slower bipolar power transistors are used as the final power switch, and thermal shutdown for it's own protection.

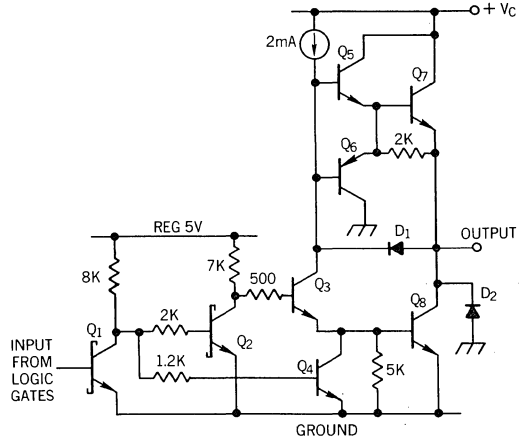

FIGURE 10- ONE OF TWO OUTPUT CIRCUITS CONTAINED WITHIN THE UC1706

INSIDE THE UC1706

The schematic of one of the output circuits in the UC1706 is shown in Figure 10. While appearing as a fairly conventional totem-pole design, the subtleties of this circuit are the slowing of the turn-off of Q3 and the addition of Q4 for rapid turn-off of Q8. The result is shown in Figure 11 where it can be seen that while maintaining fast transitions, the cross-conduction current spike has been reduced to zero when going low and only 20nsec with a high transition. This offers negligible increase in internal circuit dissipation at frequencies in excess of 500Khz.

The overall transition time through the UC1706 is shown in Figure 12 with the upper photograph recording the results with a drive to the inverting input while the lower picture is with the non-inverting input driven. Note that the only difference in speed between the two inputs is an additional 20nsec delay in turning off when the non-inverting input is used. (Note- here and in all further discussions, ON or OFF relates to the driven output power switch, i.e., ON is with the UC1706 output high and vice versa. The shutdown, blanking, and protective functions all force the UC1706 output low when active).

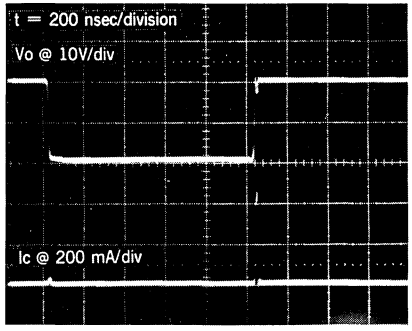

FIGURE 11 - CROSS CONDUCTION CURRENT IN THE UC1706 OUTPUT STAGE

Note that the rise and fall times of the output waveform average 20nsec with no load, 40nsec with 1000pF, and 60nsec when the capacitive load is 2200 pF.

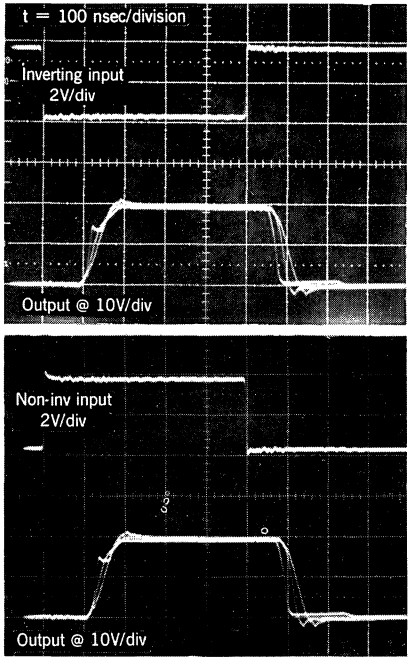

FIGURE 12 - SWITCHING RESPONSE WITH OUTPUT CAPACITANCE OF 0, 1000, AND 2200 PF.

The peak output current of each output, either source or sink, is 1.5A but with the flip/flop externally disabled, the outputs may be paralled for peak currents of 3 amps as shown in Figure 13. Saturation voltage is high at this level but falls to under 2V at 500 mA per output.

It should be noted that while optimized for FET drive, the UC1706 is equally at home when driving bipolar NPN transistors. The saturation voltage in the low state, after the turn-off transient, is less than 0.4 volt at currents to 50mA.

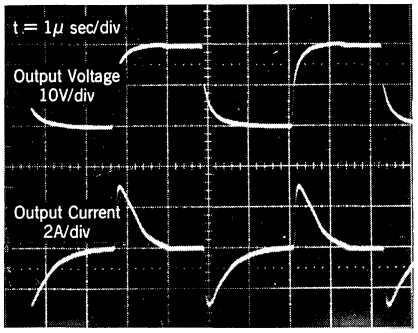

FIGURE 13 - PEAK OUTPUT CURRENT WITH BOTH OUTPUTS OF THE UC1706 CONNECTED IN PARALLEL. CL = 0.1 μF

The input logic circuitry of the UC1706 is shown in Figure 14. Since it is driven from an internally regulated 5 volt supply, TTL compatibility is assured with the driving signal only required to sink less than 1.0 mA. Input Zener clamps are included so that higher driving voltages may be used as long as the current is limited to less than 10 mA. While external pull-up resistors may speed-up the drive signal, they are not required.

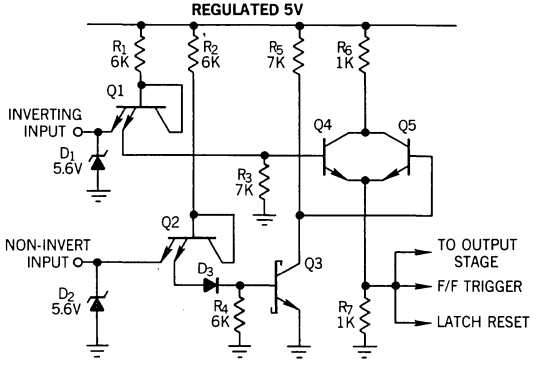

FIGURE 14 - INPUT LOGIC IN THE UC1706

The logic configuration is such to favor an output low. To get the output high requires both a low Inverting input and a high N.I. input. An output low is achieved with either a high Inv. input or a low N.I. input. To put it another way: if the Inv. input is used, the N.I. input must be high or open. Using the N.I. input requires that the Inv. input be held low. Obviously, one input could be used to override the other to force a shutdown.

Note that the output from the logic gate performs three functions when going high: it blanks both output stages to OFF, changes the state of the flip-flop, and resets the internal shutdown latch. These last two functions require at least 200nsec which means the input signal must have an off-time of at least that duration. By triggering the flip-flop from the same signal that drives the outputs, double-pulsing is prevented. When one output turns off, only the other one can turn on next, regardless of the intervening time.

SUPPLYING POWER TO THE UC1706

From the block diagram of Figure 9, note that the UC1706 has two supply terminals: Vin on pin 14 and Vc on pin 8. These pins can be driven from the same or different voltages and either can range from 5 to 40 volts. Vin drives both the input logic and the current sources providing the pull-up for the outputs. Thus Vin also can be used to activate the outputs and no current is drawn from Vc when Vin is low. Thus the UC1706 interfaces conveniently with the UC1840 Off-Line PWM Controller where low-current start-up is desired. Figure 15 shows this application where Vin is powered from the Drive Bias switch in the UC1840. In this way, the UC1706 draws no supply current while C2 initally charges through R3. R3 only has to provide 5.5 mA for the UC1840 plus the start threshold divider of R1 and R2. When there is adequate charge in C2, the start command from the UC1840 activates the UC1706 which, in turn, drives Q1 bringing up sustaining low-voltage power from N2 of the power transformer.

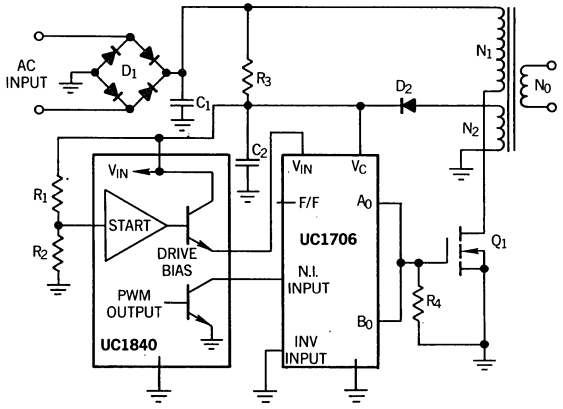

FIGURE 15- POWERING THE UC1706 FROM THE UC1840 PWM CONTROLLER

In applications where the PWM control is desired to be referenced to the load, or secondary side of the isolation transformer, the UC1706 can still be operated on the primary side for direct coupling to the power switch. With this topology, a secondary referenced auxilliary power source is necessary to operate the control circuitry whose output pulses can be either transformer or optically coupled to the input to the UC1706 on the primary side. Since only gate capacitance charging current is required from the source, at lower frequencies it is feasable to supply all the drive power directly from the line via Rin and Cin as shown in Figure 16.

In this configuration, it's still helpful to use a threshold switch with hysteresis to apply power to the UC1706 so that there is no possibility of turning on the power switch until the input voltage is adequate. Q1-Q3 implement a discrete version of such a switch.

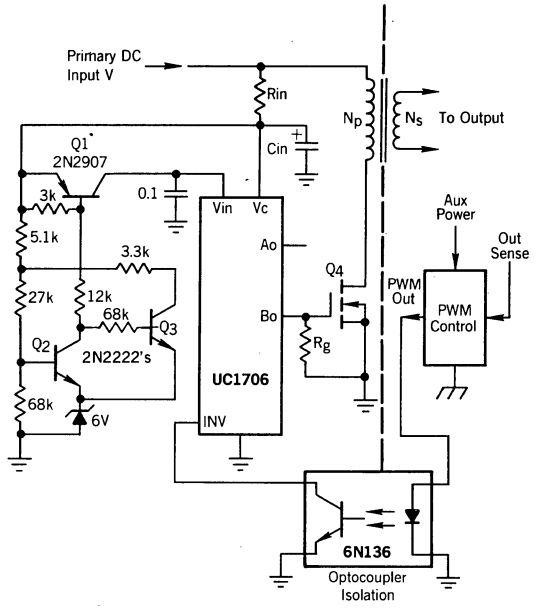

FIGURE 16- TRANSISTORS Q1 - Q3 FORM A HYSTERESIS SWITCH TO ENERGIZE THE UC1706 WHEN THE VOLTAGE ON CIN HAS CHARGED TO 15V. ISOLATED PWM DRIVE CAN BE WITH EITHER AN OPTICAL COUPLER AS SHOWN OR WITH A SMALL TRANSFORMER

DIRECT COUPLED MOSFET DRIVE

The circuit of Figure 17 shows the simplest interface to a power MOSFET - in this case the UFN 150, a large geometry 100V, 40A device with a gate capacity of typically 2000 pF. Only one output of the UC1706 was used for this demonstration and the load was the buck regulator circuit described earlier. As indicated by the use of a sense resistor in the source line, this circuit was also used to evaluate the capability of the latched shutdown comparator as a current limiter.

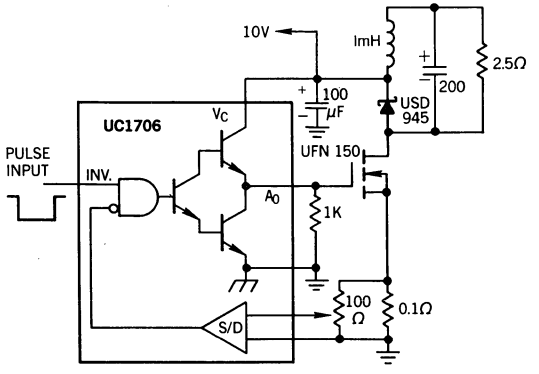

FIGURE 17 - DIRECT FET DRIVE WITH THE UC1706 WITH CURRENT SENSING IN THE SOURCE LEAD.

While directly connecting the FET gate to the output of the UC1706 is both simple and fast, it must be done with care as any wiring inductance can cause severe ringing which could take the gate voltage past its allowable limits. Usually, it merely requires some series resistance in the gate circuit to damp this ringing, but this is at the expense of switching speed as the gate resistance reacts with the input capacitance. Another justification of gate resistance is to slow switching to accommodate output rectifier recovery time as mentioned earlier in this paper.

For this example, however, maximum speed was desired and considerable care was taken to minimize lead inductance with the results as shown in Figure 18 and with an expanded time base for turn-on, in Figure 19. These photos show the requirements of this FET for one amp peak gate current at turn-on and turn-off with the hesitation in gate voltage rise time at threshold as the falling drain voltage robs gate current through the gate-drain capacitance. The drain current spike at turn-on is due to the recovery of the freewheeling diode in the output load.

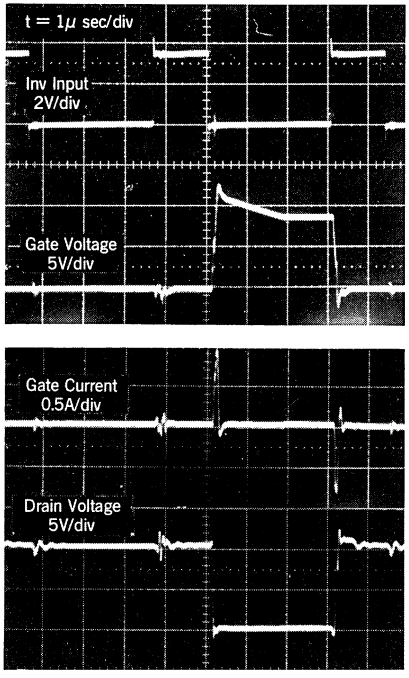

FIGURE 18- DIRECT COUPLED POWER MOS FET DRIVE

In order to evaluate the threshold of the shutdown comparator, the buck regulator circuit load on the drain was replaced with a wire wound resistor whose inductance provided a slower turn-on of drain current. Since it is a latching circuit, this comparator is another area where considerable care must be taken to eliminate the possibility of noise triggering. These problems are eased somewhat since the inputs are differential with a large common-mode range capability and the threshold of 130 mV is built in. However, these inputs should still be connected to the current sensor as a closely coupled, and perhaps even shielded pair.

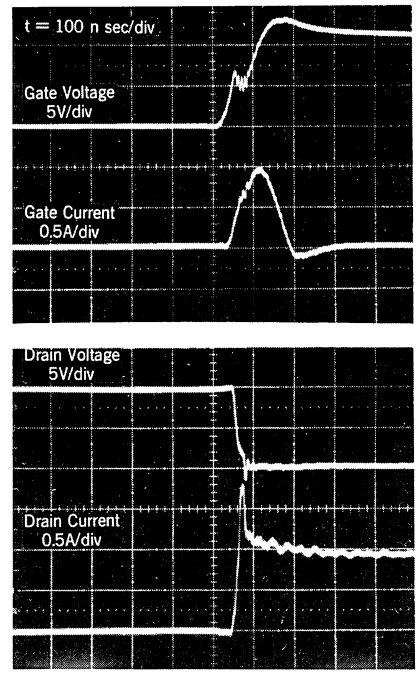

FIGURE 19- DIRECT DRIVE TURN-ON WITH EXPANDED TIME SCALE

For this example, a 0.1 ohm non-inductive resistor was used as a current sensor with a 100 ohm potentiometer used to adjust the current threshold to 2 amps. The multiple exposure print of Figure 20 shows the effect of increasing load current. At 2 amps, the comparator begins to reduce the pulse width. As current increases, the comparator is overdriven and its response time quickens to approximately 200nsec plus the turn-off time of the power switch. Beyond this point, one must rely on circuit inductance or go to more elaborate means to clamp the current.

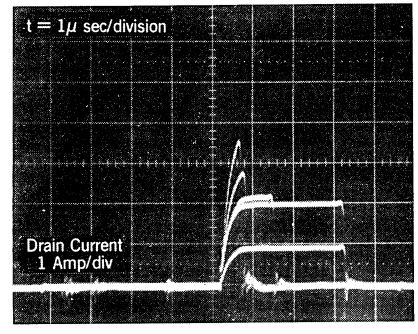

FIGURE 20- CURRENT LIMITING WITH THRESHOLD SET FOR 2 amps

ISOLATED GATE DRIVE

The single-ended transformer-coupled drive circuit shown in Figure 21 is often useful for either isolation or to optimally match the voltage and current between the driving source and the gate. In this case, outputs A and B were paralleled merely to get close to 100% modulation - the full output current capability was not required as the transformer provided additional current gain. Since this is a unipolar drive, capacitor C1 is used to block the DC voltage and provide adequate volt-seconds for core reset. C2 and the zener diode provide DC restoration and clamp the gate to only one diode drop negative. The 10V positive clamp of the zener also protects the gate from any transient overshoot.

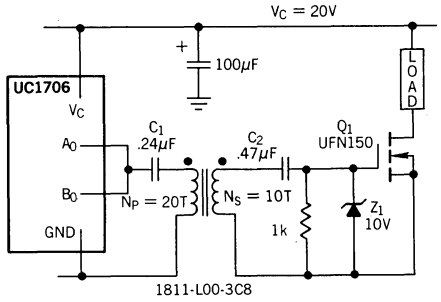

FIGURE 21 - BOTH UC1706 OUTPUTS ARE COMBINED FOR A SINGLE-ENDED TRANSFORMER-COUPLED DRIVE.*

The criteria for the transformer design was the arbitrary specification to keep the magnetization current to less than 50 mA to keep the steady-state power consumption low. Magnetization current may be made lower with more transformer turns which yields higher leakage inductance and slower response. In this circuit, with f = 100 kHz, τ = 10 μ sec, and Vin = 20V,

$$Lm = \frac{Vin \cdot \tau}{2\ Im} = \frac{20 \times 10 \times 10^{-6}}{2 \times 50 \times 10^{-3}} = 2\ mH$$

and since $L = A_L N^2 \times 10^{-6}$ mH, for a 1811P-L00-3C8 core

$$Np = \sqrt{\frac{Lx10^6}{A_L}} = 20\ turns$$

and Ns was made equal to 10 turns for a 10V output.

With this design, the energy stored in the core is

$$E = \tfrac{1}{2}\ Lm\ Im^2 = .05\ \mu J$$

which is considerably below the saturation level of

$$E = \frac{B^2\ Ae\ le \times 10^{-8}}{2\ \mu e} = \frac{2000^2 \times .43 \times 2.58 \times 10^{-8}}{2 \times 1930} = 11.4\ \mu J$$

The coupling capacitor value was defined by setting a requirement that it charge to no more than 10% of Vin with each pulse.

$$C_1 = \frac{Im\ \tau}{0.1\ Vin} = \frac{50 \times 10^{-3} \times 10 \times 10^{-6}}{0.1 \times 20} = .25\ \mu F$$

*Circuit design courtesy of J. Potasse, Canadair Limited.

The resultant waveforms through this circuit are shown in Figure 22. Note that when switching is complete,the gate circuit goes to a high impedance and the transformer leakage inductance causes a slight voltage over-shoot at both the gate and at the output of the UC1706. Otherwise, these waveforms should be self-explanatory.

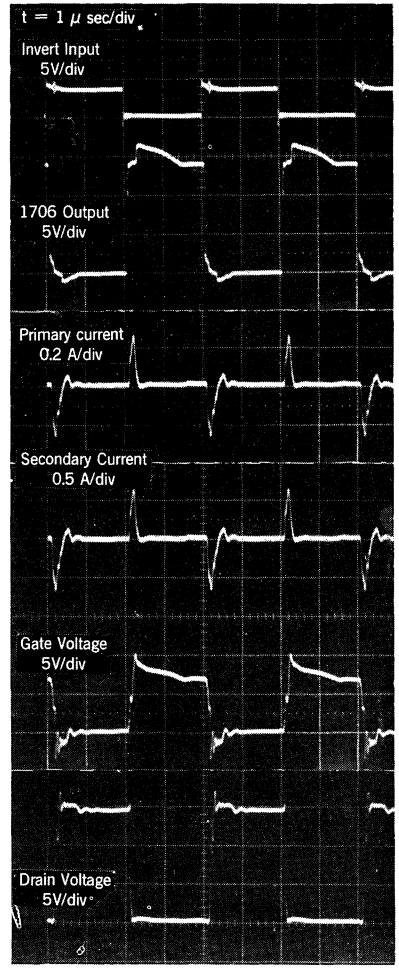

FIGURE 22 - SINGLE ENDED TRANSFORMER COUPLED PERFORMANCE

PUSH-PULL TRANSFORMER COUPLING

The totem-pole outputs of the UC1706 can easily be interfaced for balanced transformer drive as shown in Figure 23. A and B outputs are alternating now as the internal flip-flop is active and the output frequency is halved. Note that when one UC1706 output goes high, the other is held low and both are low during the dead time between output pulses.

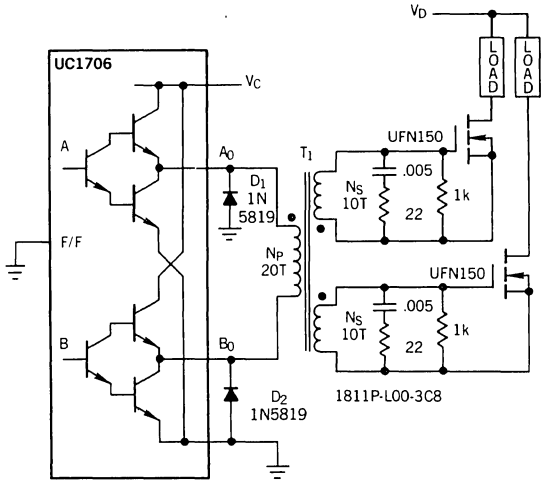

FIGURE 23 - BALANCED PUSH-PULL TRANSFORMER COUPLING

For this circuit, the same transformer as in the previous example was used except that now there are two identical secondary windings. With balanced operation, no coupling capacitor is necessary as there is no net DC current through the primary.

One precaution which must be taken however, is that transformer leakage inductance may force the output of the UC1706 negative when it turns off. If both the frequency and current are low, the output diodes in the UC1706 may suffice for clamping. Otherwise, external diodes as shown in Figure 23 should be added. An added complication of transformer leakage inductance is the requirement for snubbing circuits to keep the gate voltage ringing under control.

Again, waveforms at all significant points within this circuit are shown in Figure 24.

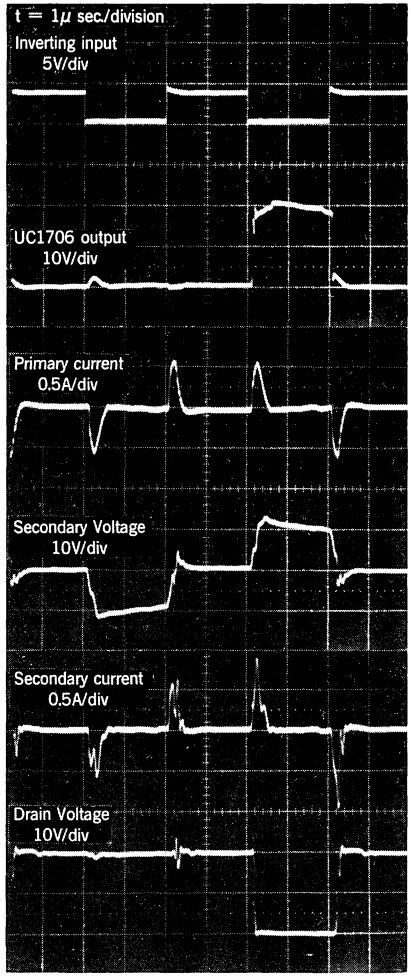

FIGURE 24 - BALANCED PUSH-PULL TRANSFORMER COUPLING PERFORMANCE.

A SQUARE WAVE INVERTER EXAMPLE

To illustrate the usage of the UC1706 as a bipolar transistor switch driver, a simple square wave generator is shown in Figure 25, with the operating

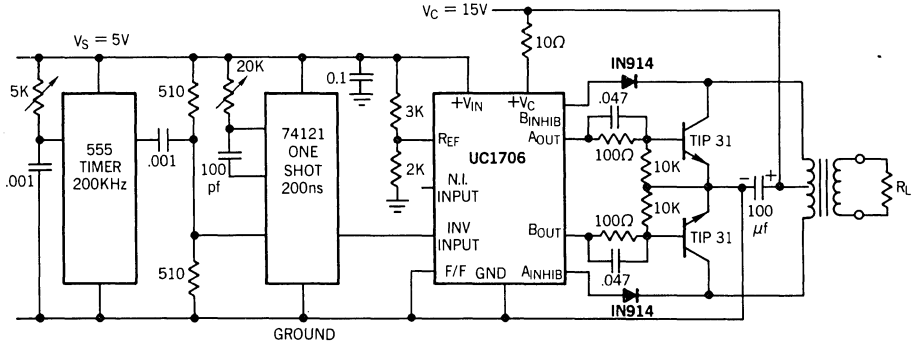

FIGURE 25 - A SQUARE WAVE INVERTER CIRCUIT USING THE UC1706 TO DRIVE BIPOLAR TRANSISTOR SWITCHES.

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circuit waveforms pitured in Figure 26. This application demonstrates the advantages in using the UC1706 to efficiently drive relatively slow transistors in high-speed applications.

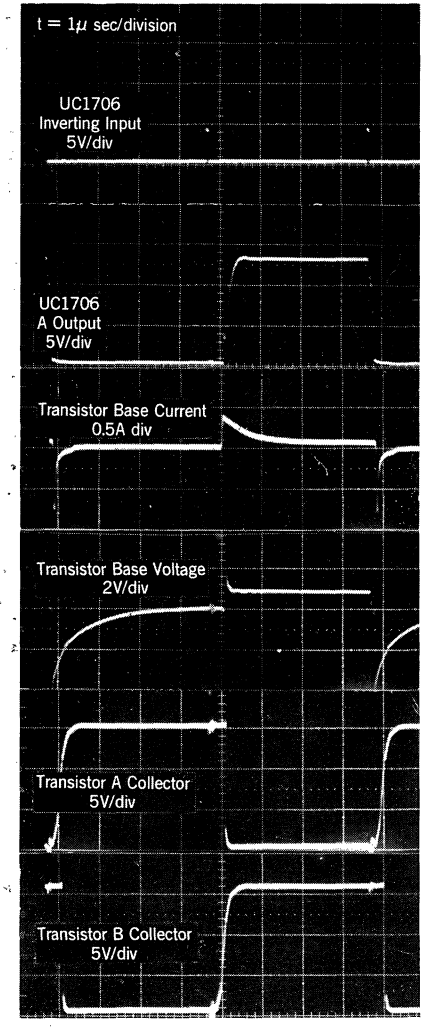

FIGURE 26- BIPOLAR SQUARE WAVE GENERATOR WAVEFORMS

This circuit starts with a 555 timer oscillating at 200 kHz to establish the operating frequency of the inverter at 100 kHz.

Its output triggers the 74121 one-shot which provides an input pulse to the UC1706. This signal is actually the off-time or blanking pulse to the outputs. For an ideal push-pull square wave generator, its pulse width should be zero. If the storage time of the power switches were a known constant, then this pulse width could be adjusted such that one switch turns on just as the other comes out of saturation. Since this is not very realistic and since the UC1706 needs 200nsec to switch from one output to the other, that's the pulse width set by the one-shot.

The high-current output from the UC1706 is utilized with .047 mfd speed-up capacitors to provide one amp of peak turn-on current, 100 mA of drive, and 1.5A turn-off, thus reducing the typical 2 micro-second turn-off time of the TIP-31 to approximately 400nsec. Since this is still longer then the blanking pulse, conduction overlap would take place were it not for the use of the inhibit circuit of the UC1706 which is connected to the outputs through the 1N914 diodes. This circuit insures that regardless of the input, side A will not turn on until the diode connected to side B's collector rises above the reference established by the 3K/2K divider. Waveform photos of this inhibit action are shown in Figure 27. There is now a dead time resulting from the inhibit delay in the UC1706 plus the turn-on delay of the TIP-31 which can be used to advantage to allow time for the output rectifiers to recover.

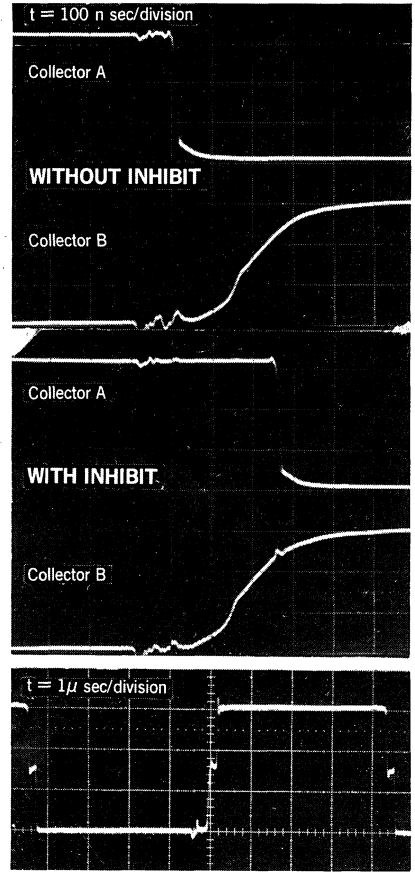

FIGURE 27- SQUARE WAVE GENERATOR OUTPUT WITH INHIBIT - CONTROLLED DEADBAND

SUMMARY

This paper has attempted to present an understanding of the dynamics of high-speed power MOSFET switching to aid in defining optimum gate drive signals to meet specific applications. The need for high peak gate currents with controlled rise times has led to the development of several integrated circuits aimed toward these goals. The most recent of these, the UC1706, provides high-speed response, three amps of peak current, and the ease of implementing either direct or transformer drive to a broad range of MOS FET devices. With this new device one more specialized function has been developed to further aid the power supply designer simplify his tasks.

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UC3717 and L-C Filter Reduce EMI and Chopping Losses in Step Motor

A chopper drive which uses the inductance of the motor as the controlling element causes a temperature rise in the motor due to hysteresis and eddy current losses. For most motors, especially solid rotor constructions, this extra heat can force the designer to go to a larger motor and then derate it, or to a more expensive laminated construction in order to produce enough output torque for the job. Regardless of the motor type, *any* extra heat generated within a system will have to be removed or else other system components will be stressed unnecessarily. This could mean using a fan where convection cooling might otherwise have sufficed. In addition, the EMI generated from both the motor and its leads is of serious concern to the designer in view of ever-increasing EMI regulations.

These problems can be virtually eliminated by borrowing a simple technique from switching power supply designs, i.e., by placing a properly designed low-pass L-C filter across the output and using *this* L to control the UC3717. This removes the high frequency AC chopping losses in the motor by providing it with almost pure DC current. It also confines the EMI-causing, high frequency AC components to within the driver where they are easier to handle. This could allow increased wire lengths and possibly free up some design constraints, but remember that even though DC emits no EMI, the driver will still commutate the windings and can produce some components of frequency as high as 10 kHZ. The design of the L-C filter is straight-forward and its small additional cost can be recovered easily. The Unitrode UC3717, a complete chopper drive for one phase winding on a monolithic IC, makes the design job simple. The end result, a cooler running and EMI quieter step motor, can be achieved with just a few additional passive components.

Preliminary Considerations

For our analysis, we will use a "23" frame, bipolar motor with a solid rotor and the following specifications:

P_{max} =	9.0 Watts	= Maximum power dissipation at 25°C
V_{max} =	3.75 Volts	= Maximum voltage per motor phase at 25°C
I_{max} =	1.25 Amps	= Maximum current per motor phase at 25°C
R_m =	3.0 Ohms	= Resistance of one phase at 25°C
*L_m =	8.4 mH	= Inductance of one phase winding

*It should be noted that L_m, as given in a manufacturer's data sheet, is not always *true average* inductance as seen at high current in a circuit, but rather the inductance reading you would obtain from a low current inductance bridge. This value can differ from in-circuit inductance by a factor of 2 or more! The in-circuit inductance for this motor is 5.0 mH.

We begin by calculating the electrical time constant of one phase winding using the resistance value given above and the *actual* motor inductance:

$$\tau_m = \frac{L_m}{R_m} = \frac{5.0\ \text{mH}}{3.0\ \text{Ohms}} = 1.67\ \text{msec} \quad (1)$$

If one were using a standard voltage drive then it would take approximately τ_m or 1.67 msec to reach the current level required for proper operation. This places a severe restriction on motor speed. Increasing the drive voltage will allow the motor to run faster but will cause it to draw too much current and overheat. Maximum motor speed may be increased by decreasing the time constant. Since L_m is fixed, the only parameter we can change is the effective value of R_m by placing a resistor in series with it. If we place a resistor 4 times R_m in series such that total R is 5 times R_m and increase the drive voltage by a factor of 5 then we will have reduced the time constant by a factor of 5 to 330 μsec and also increased both the maximum motor speed and maximum power output by a factor of 5 each. Unfortunately, we will have increased wasted power by a factor of 5 also.

The Chopper Drive

Using a chopper drive enables one to run at a higher voltage and thus reach proper operating current faster while still protecting the motor from excessive current that would otherwise flow due to the higher voltage. The high voltage is first applied across the motor winding and then, when I_{max} is reached, it is switched off. (If it were not switched off then the maximum current rating of the motor would be quickly exceeded.) The current is then allowed to circulate in a loop within the driver and motor for a fixed time period (t_{off}) after which the voltage is re-applied to the motor. The operating frequency, which is determined by both the motor inductance and t_{off} should be high enough that the resulting current ripple is small compared to the average DC current. Power efficiency is relatively high because there is no external resistor used.

Nothing is free in the world of physics, however, and the price one pays for the extra power output capability is an increase in wasted heat due to hysteresis and eddy current losses *within* the motor instead of in an external resistor. Being within the motor, it can now cause overheating as well as reliability problems. Since the excess heat increases rapidly with the overdrive ratio, this means that at low overdrive ratios (less than 5-to-1) there will be almost negligible heating, but at higher overdrive ratios (more than 10-to-1) the induced motor losses can beome as great as, or actually *exceed*, the I^2R losses! By placing a low-pass L-C filter in the circuit these induced losses can once again become negligible. The L and C components selected should be capable of operating at frequencies of 25 kHz or higher without heating effects in the inductor core or inductive effects in the capacitor.

UC3717 and L-C Filter

Designing with the UC3717

Using a supply voltage (v_s) of 40 volts (approximately a 10/1 overdrive), the turn-on rise-time becomes:

$$t_{rise} = -\tau_m \times Ln\,(1 - V_m/V_s) = -1.67 \times 10^{-3} \times Ln\,(1 - 3.75 / 40)$$
$$= 164\ \mu sec \qquad (2)$$

or *an improvement of approximately 10-to-1 in speed capability.*

Using an off-time (t_{off}) of 30 μsec as suggested on the UC3717 data sheet and limiting current (I_w) to 850 mA establishes a voltage across the resistive component of the winding ($V_{w\text{-}on}$) during the "on" time of:

$$V_{w\text{-}on} = I_w \times R_w = .85 \times 3.0 = 2.55\ Volts \qquad (3)$$

and during the "off" time (due to a 2.6 volt drop across the upper transistor, as shown in the data sheet, and a 0.4 volt drop across the Schottky "catch" diode) of:

$$V_{w\text{-}off} = V_{transistor} + V_{diode} = 2.6 + 0.4 = 3.0\ Volts \qquad (4)$$

Since the voltage and current changes are small, we can substitute a resistance (R_e) equivalent to $V_{w\text{-}off}/I_w$ in series with R_w to adjust the time constant and allow us to calculate the approximate current ripple (ΔI_w) during t_{off}:

$$\Delta I_w = I_w \left(1 - \exp\left[\frac{-t_{off}(R_w + R_e)}{L_m}\right]\right)$$
$$= .85 \times \left(1 - \exp\left[\frac{-30\times10^{-6} \times (3.0 + 3.5)}{5\times10^{-3}}\right]\right)$$
$$= 33\ mA\ p\text{-}p \qquad (5)$$

Knowing ΔI_w, we can now calculate the on-time (t_{on}):

$$t_{on} = \frac{\Delta I_w \times L_m}{V_s - V_{w\text{-}on}} = \frac{33\times10^{-3} \times 5\times10^{-3}}{40 - 2.55} = 4.4\ \mu sec \qquad (6)$$

and can also find our operating frequency (f) by:

$$f = 1 / (t_{on} + t_{off}) = 1 / (4.4 + 30) \times 10^{-6} = 29.1\ kHz \qquad (7)$$

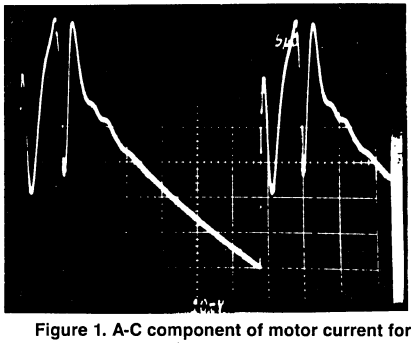

Figure 1. A-C component of motor current for standard chopper configuration.

Since this frequency is well above audible ranges, it will not cause any objectionable sound, but there are still the problems of EMI and excess motor heating to deal with. It is possible to generate EMI due to the current switching that occurs in the motor leads because they carry not only the primary frequency, but also many higher harmonics as well, so they require careful routing, shielding, or both. We can put in a low pass L-C filter to remove these high frequencies and still pass normal commutation currents without any significant loss of motor performance.

Design of the L-C Filter

Figure 2 is a block diagram of a motor connected to 2 UC3717s with the low-pass L-C filters in place.

Again we will use a current of 850 mA in each winding, an off-time of 30 μsec, and an on-time of 4.4 μsec but now we will use an

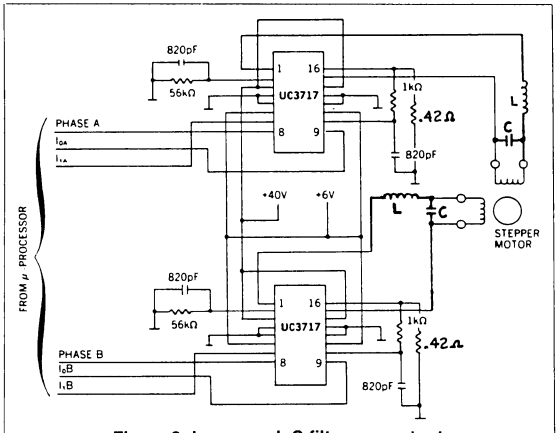

Figure 2. Low-pass L-C filters on outputs.

external inductance (L) to control the chopping. V_{drop} is the sum of the source (V_{so}) and sink (V_{si}) voltage drops at 850 mA:

$$V_{drop} = V_{so} + V_{si} + V_{sense} = (2.6 + 1.9 + 0.36)$$
$$= 4.9\ volts \qquad (8)$$

In order to minimize the effects of L on the motor current risetime we will make it 10 times smaller than L_m or 500 μH. In order to keep the peak current in the UC3717 below 1 amp we will use a 0.42 ohm sense resistor and also limit $_{\Delta}I_L$ to 300 mA. Using a variation of equation (6) we can check that:

$$L = \frac{(V_s - V_{drop}) \times t_{on}}{{}_{\Delta}I_L} = \frac{(40 - 4.9) \times 4.4\times10^{-6}}{300\times10^{-3}} = 515\ \mu H \qquad (9)$$

is in keeping with the constraints outlined above.

Similarly, we would like to find a value for the capacitor (C) such that it will have less than 1/10 the impedance of L at 29.1 kHz:

$$C = \frac{10}{(2 \times \pi \times f)^2 \times L} = \frac{10}{(2 \times 3.14 \times 29100)^2 \times 500\times10^{-6}} \qquad (10)$$
$$= 0.6\ \mu F$$

The test motor and driver, operated unloaded (nothing connected to the output shaft) and in the configuration of *Figure 2*, used values of 500 μH for the inductor and 0.47 μF for the capacitor. *Figure 1* and *Figures 3* through *6* are waveforms obtained from that motor.

The lower trace of *Figure 3* (*Figure 3b*) shows the 330 mA current sawtooth in the inductor, while the upper trace (*Figure 3a*) shows an 8 mA p-p current ripple in the motor winding. While this may seem to indicate only a 12 dB reduction in EMI over *Figure 1*, comparing the *sinusoidal* waveform of *Figure 3a* to the "noisy" *sawtooth* waveform of *Figure 1* will quickly point out sources of

UC3717 and L-C Filter

EMI. In *Figure 1*, the oscillations immediately following each switch of the driver are due to the motor's distributed capacitance resonating with its inductance and are a possible source of EMI. In addition, sharp current spikes are allowed to pass along the motor leads and through the motor's distributed capacitance unhindered, thus creating high frequency EMI. EMI spikes were virtually eliminated from *Figure 3a* by using a low ESR capacitor and connecting the motor leads close to the body of the capacitor.

Figure 4 shows motor current superimposed over the inductor current. Just to the left of the center graticle line a ringing occurs in the inductor current that also appears in the motor current, although attenuated. This ringing occurs at a frequency of:

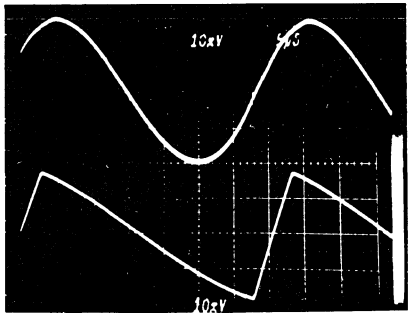

Figure 3. Motor and inductor current waveforms.

$$f_{res} = 1 / 2\pi\sqrt{L \times C} = 1 / 6.28 \times \sqrt{500\times10^{-6} \times 0.47\times10^{-6}} = 10.4 \text{ kHz} \quad (11)$$

which is the resonant frequency of the L-C filter. This frequency can be lowered by increasing the value of either L or C, although at a cost of reducing the high speed performance of the motor.

The high frequency sawtooth waveforms at the upper, flat portion of the motor current waveform are the 29.1 kHz chopping currents in the inductor. They cause a small corresponding ripple in the motor current but, because the chopping frequency is more than twice the break frequency of the 2-pole L-C filter, we would expect, and can see, an attenuation greater than 12 dB.

In a 2 phase step motor (sometimes referred to as a 4 phase step motor because of the 4 windings used in the unipolar version) the STEP RATE, in full steps per second (FSPS), is 4 times the primary frequency of the motor current waveform. The two phases of the step motor are operated in quadrature and thus will generate 4 distinct states in the 2 phases which correspond to 4 mechanical steps for each electrical cycle.

FSPS = 4 x frequency (for a 2 or "4" phase step motor) (12)

It is important to note at this time that 10.4 kHz is the highest *frequency* that can be passed to this motor without attenuation using the selected components, but that this corresponds to a *step rate* of 41,600 FSPS! The test motor was able to run at 17,000 full steps per second with the L-C filter in place, which is high enough for most situations.

Figures 5 and *6* are current waveforms for the motor running at 1600 FSPS and 16,000 FSPS respectively. The motor was operated with the L-C filter on only the lower trace winding so that the waveforms could be compared easily. Looking at *Figure 5*, one can see that the leading edges of both waveforms have the same

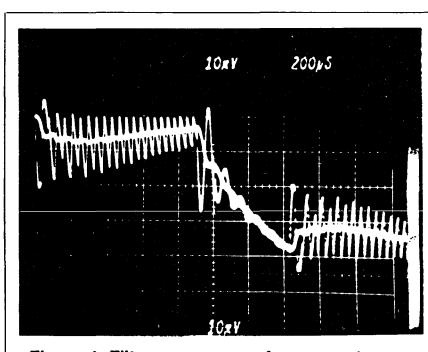

Figure 4. Filter current waveform superimposed over motor current waveform.

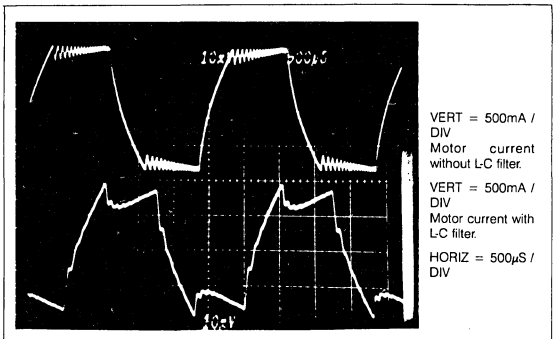

Figure 5. Motor currents at 1600 FSPS.

risetimes, although the filtered one has more suscepibility toward ringing. From *Figure 6*, one can see that torque is down only 3 dB at 16,000 FSPS and that there are "glitches" in the unfiltered waveform that do not appear in the filtered waveforms.

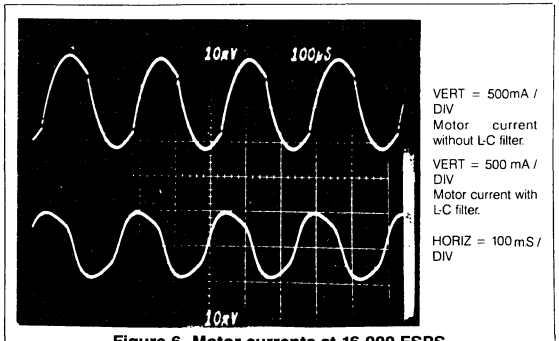

Figure 6. Motor currents at 16,000 FSPS.

Conclusions

The use of a low-pass filter can be an effective heat and EMI reduction mechanism when used with a step motor chopper driver such as the UC3717. The price one pays for a "clean" EMI environment is a *small* loss in very high speed performance. The technique may be applied equally well to non-IC chopper drivers but the peak currents must be accounted for and the minimum value of L adjusted accordingly. 500 µH is the smallest practical L that should be used with the UC3717 since we do not want the

UC3717 and L-C Filter

peak of the ripple to exceed 1.0 amps. This limits the usefulness of the technique to motors with inductances of 2 mH or more. At average currents less than 300 mA, the value of L may have to be larger in order to maintain continuous current in the inductor, but the physical size may be decreased. If an average current in excess of 850 mA is required, then a PIC900 Power Amplifier may be added as shown in *Figure* 7. This will extend the peak current capabilities of the chopper drive to 5A and will also allow the value of L to be decreased.

η

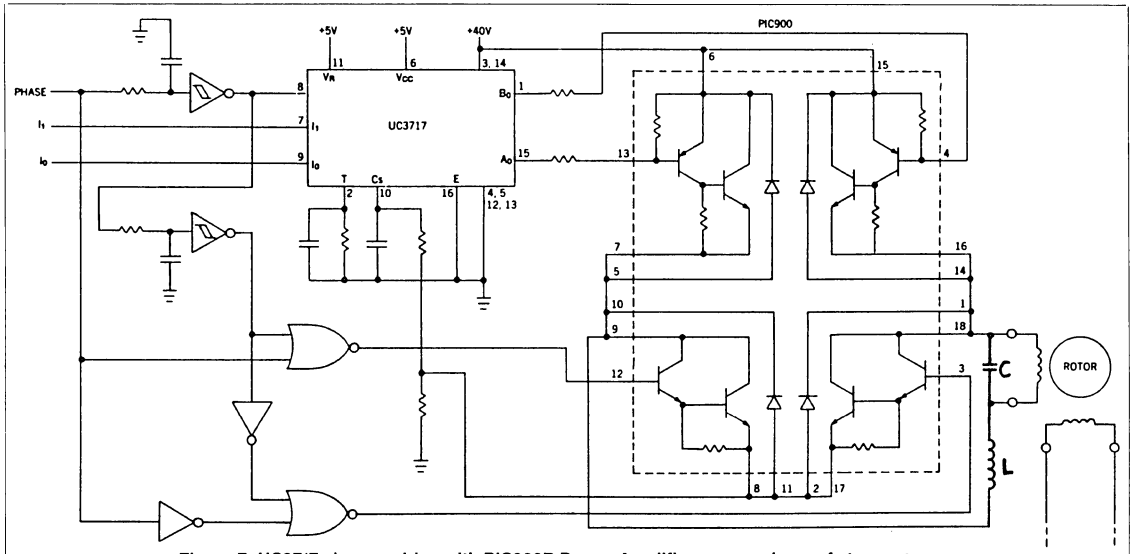

Figure 7. UC3717 chopper drive with PIC900B Power Amplifier on one phase of step motor.

UC3842 PROVIDES LOW-COST CURRENT-MODE CONTROL

The fundamental challenge of power supply design is to simultaneously realize two conflicting objectives: good electrical performance and low cost. The UC3842 is an integrated pulse width modulator (PWM) designed with both these objectives in mind. This IC provides designers an inexpensive controller with which they can obtain all the performance advantages of current-mode operation. In addition, the UC3842 is optimized for efficient power sequencing of off-line converters and for driving increasingly popular power MOSFETs.

This application note gives a functional description of the UC3842 and suggests how to incorporate the IC into practical power supplies. A review of current-mode control and its benefits is included and methods of avoiding common pitfalls discussed. The final section presents designs of two power supplies utilizing UC3842 control.

CURRENT-MODE CONTROL

Figure 1 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

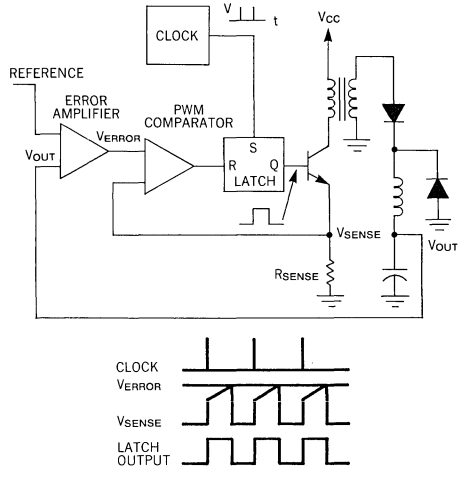

FIGURE 1. TWO-LOOP CURRENT-MODE CONTROL SYSTEM.

Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved; i.e., the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an error-voltage-controlled-current-source for the purposes of small-signal analysis. This is illustrated by Figure 2. The

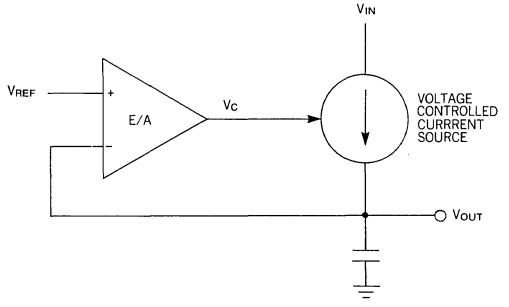

FIGURE 2. INDUCTOR LOOKS LIKE A CURRENT SOURCE TO SMALL SIGNALS.

two-pole control-to-output frequency response of these converters is reduced to a single-pole (filter capacitor in parallel with load) response. One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gain-bandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler and better behaved, as illustrated in Figure 3. Capacitor C_i and resistor R_{iz} in Figure 3a add a low frequency zero which cancels one of the two control-to-output poles of non-current-mode converters. For large-signal load changes, in which converter response is limited by inductor slew rate, the error amplifier will saturate while the inductor is catching up with the load. During this time, C_i will charge to an abnormal level. When the inductor current reaches its required level, the voltage on C_i causes a corresponding error in supply output voltage. The recovery time is $R_{iz}C_i$, which may be

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milliseconds. However, the compensation network of Figure 3b can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of C_i.

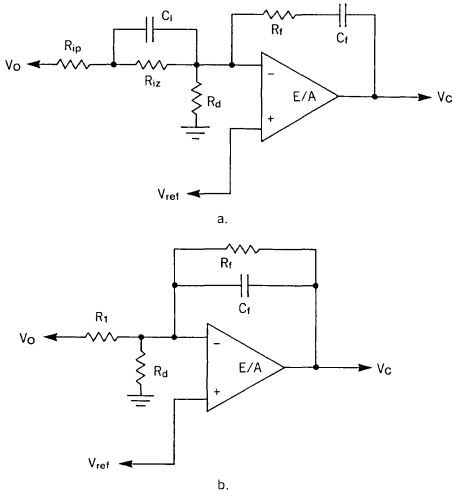

FIGURE 3. REQUIRED ERROR AMPLIFIER COMPENSATION FOR CONTINUOUS INDUCTOR CURRENT DESIGNS USING (a.) DUTY CYCLE CONTROL AND (b.) CURRENT-MODE CONTROL.

Current limiting is simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

FUNCTIONAL DESCRIPTION

A block diagram of the UC3842 appears in Figure 4. This IC will operate from a low impedance DC source of 10V to 30V. Operation between 10V and 16V requires a start-up bootstrap to a voltage greater than 16V in order to overcome the under-voltage lockout. V_{cc} is internally clamped to 34V for operation from higher voltage current-limited sources ($I_{cc} \leq 30mA$).

Under-Voltage Lockout (UVLO)

This circuit insures that V_{cc} is adequate to make the UC3842 fully operational before enabling the output stage. Figure 5a shows that the UVLO turn-on and turn-off thresholds are fixed internally at 16V and 10V respectively.* The 6V hysteresis prevents V_{cc} oscillations during power sequencing. Figure 5b shows supply current requirements. Start-up current is less than 1mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by Figure 6. During normal circuit operation, V_{cc} is developed from auxiliary winding W_{AUX} with D_1 and C_{IN}. At start-up, however, C_{IN} must be charged to 16V through R_{IN}. With a start-up current of 1mA, R_{IN} can be as large as 100kΩ and still charge C_{IN} when V_{AC} = 90V RMS (low line). Power dissipation in R_{IN} would then be less than 350mW even under high line (V_{AC} = 130V RMS) conditions.

During UVLO, the UC3842 output driver is biased to a high impedance state. However, leakage currents (up to 10μA), if not shunted to ground, could pull high the gate of a MOSFET. A 100kΩ shunt, as shown in Figure 6, will hold the gate voltage below 1V.

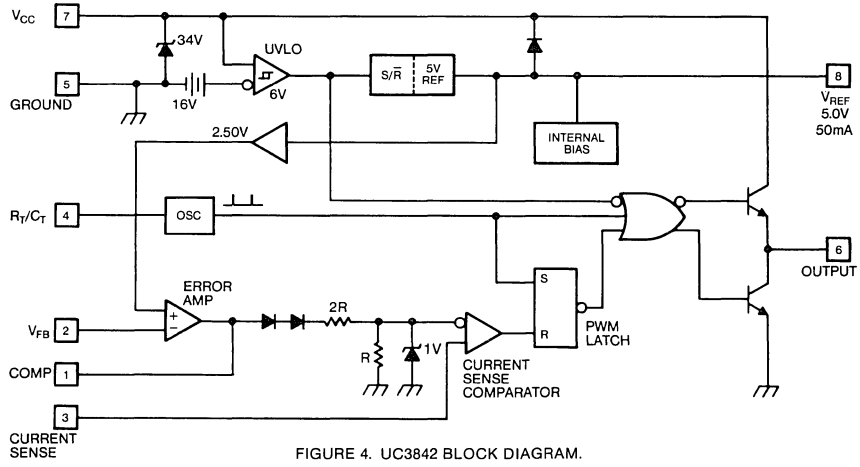

FIGURE 4. UC3842 BLOCK DIAGRAM.

*For operation from a low voltage input, the UC3843 is available. This IC has UVLO thresholds of 10.8V and 7.9V, and is otherwise identical to UC3842.

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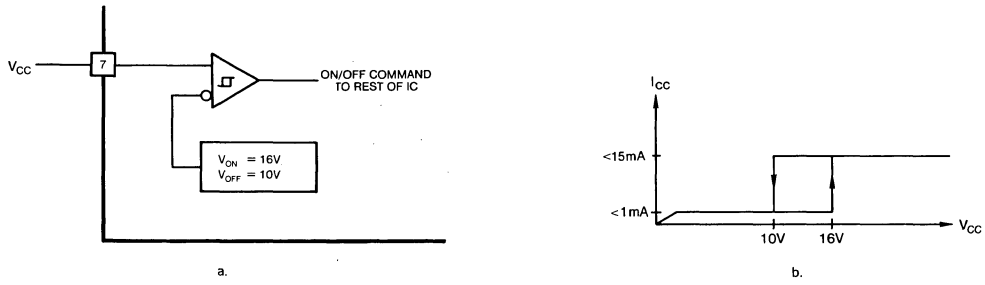

FIGURE 5. (a.) UNDER-VOLTAGE LOCKOUT AND (b.) SUPPLY CURRENT REQUIREMENTS.

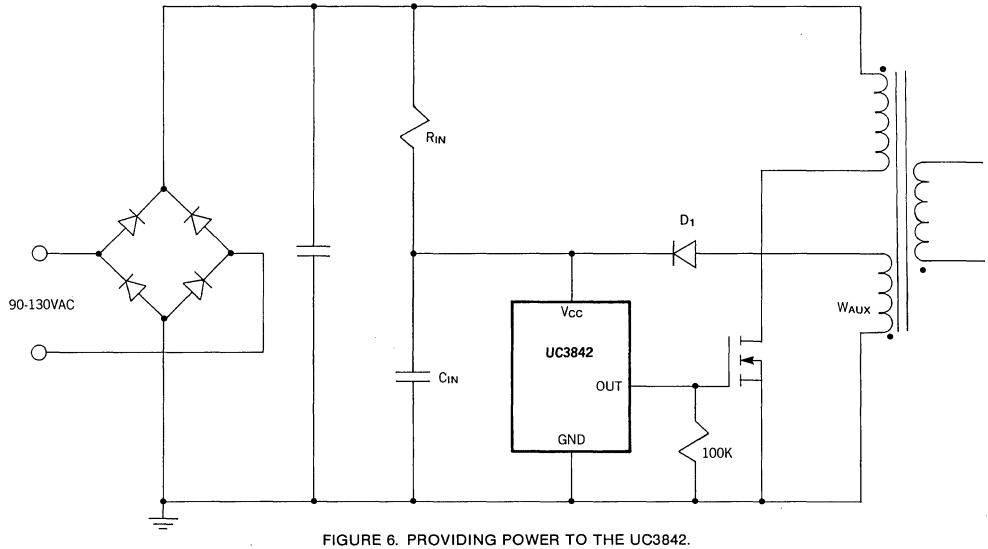

FIGURE 6. PROVIDING POWER TO THE UC3842.

Oscillator

The UC3842 oscillator is programmed as shown in Figure 7a. Oscillator timing capacitor C_T is charged from V_{REF} (5V) through R_T, and discharged by an internal current source. Charge and discharge times are given by:

$$t_c \approx 0.55\ R_T C_T$$

$$t_d \approx R_T C_T\ \ell n \left(\frac{.0063\ R_T - 2.7}{.0063\ R_T - 4.0} \right)$$

Frequency, then, is:

$$f = \frac{1}{t_c + t_d}.$$

For $R_T > 5k\Omega$, t_d is small compared to t_c, and:

$$f \approx \frac{1}{0.55\ R_T C_T} \approx \frac{1.8}{R_T C_T}.$$

During the discharge time, the internal clock signal blanks the output to the low state. Therefore, t_d limits maximum duty cycle (D_{MAX}) to:

$$D_{MAX} = \frac{t_c}{t_c + t_d} = 1 - \frac{t_d}{T}$$

where: $T = 1/f$ = switching period.

The timing capacitor discharge current is not tightly controlled, so t_d may vary somewhat over temperature and from unit to unit. Therefore, when very precise duty cycle limiting is required, the circuit of Figure 7b is recommended.

One or more UC3842 oscillators can be synchronized to an external clock as shown in Figure 8. Noise immunity is enhanced if the free-running oscillator frequency ($f = 1/(t_c + t_d)$) is programmed to be ~20% less than the the clock frequency.

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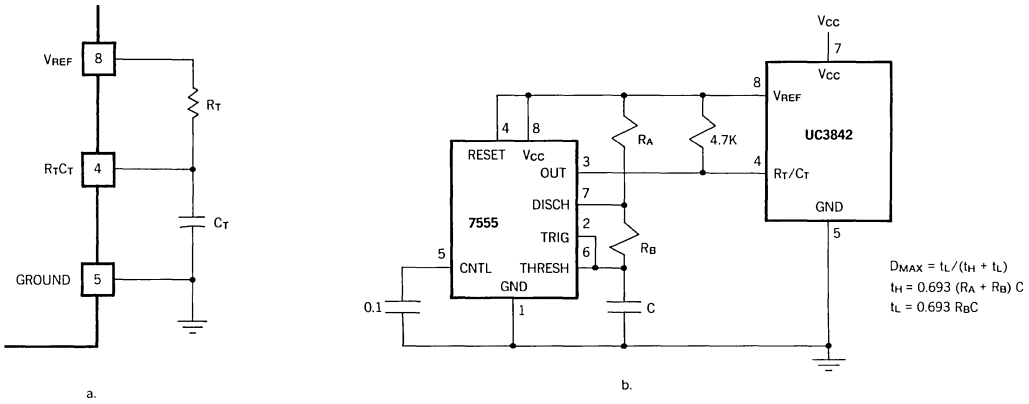

FIGURE 7. (a.) OSCILLATOR TIMING CONNECTIONS AND (b.) CIRCUIT FOR LIMITING DUTY CYCLE.

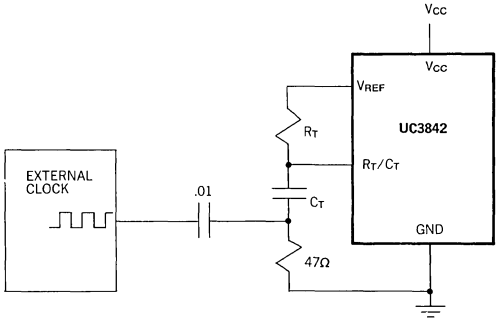

FIGURE 8. SYNCHRONIZATION TO AN EXTERNAL CLOCK.

Error Amplifier

The error amplifier (E/A) configuration is shown in Figure 9. The non-inverting input is not brought out to a pin, but is internally biased to 2.5V ± 2%. The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 10a shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with continuous inductor current. The feedback components add a pole to the loop transfer function at $f_p = 1/2\pi R_f C_f$. R_f and C_f are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit. R_i and R_f fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to unity (0dB) at $f \approx f_{switching}/4$. This technique insures converter stability while providing good dynamic response.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. R_p and C_p in the circuit of Figure 10b provide this pole.

The E/A output will source 0.5mA and sink 2mA. A lower limit for R_f is given by:

$$R_{f(MIN)} \approx \frac{V_{E/A\ OUT\ (MAX)} - 2.5V}{0.5mA} = \frac{6V - 2.5V}{0.5mA} = 7k\Omega.$$

E/A input bias current (2μA max) flows through R_i, resulting in a DC error in output voltage (V_O) given by:

$$\Delta V_{O\ (MAX)} = (2\mu A)\ R_i.$$

It is therefore desirable to keep the value of R_i as low as possible.

Figure 11 shows the open-loop frequency response of the UC3842 E/A. The gain represents an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1MHz due to second-order poles at ~10MHz and above.

Current Sensing and Limiting

The UC3842 current sense input is configured as shown in Figure 12. Current-to-voltage conversion is done externally with ground-referenced resistor R_S. Under normal operation the peak voltage across R_S is controlled by the E/A according to the following relation:

$$V_{R_S(pk)} = \frac{V_C - 1.4V}{3}$$

where: V_C = control voltage = E/A output voltage.

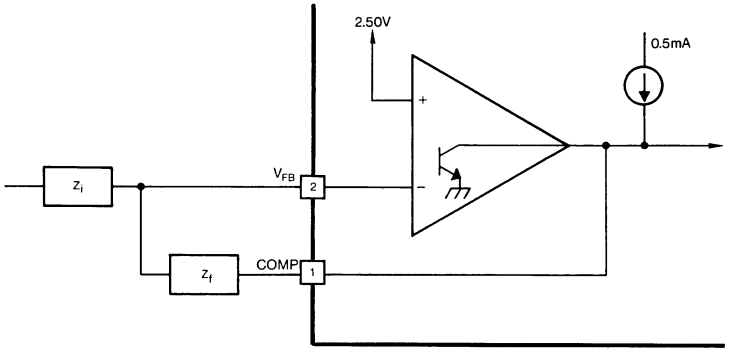

FIGURE 9. UC3842 ERROR AMPLIFIER.

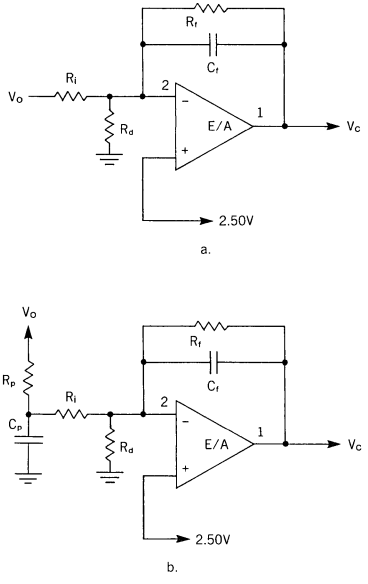

FIGURE 10. (a.) ERROR AMPLIFIER COMPENSATION. ADDITIONAL POLE (b.) NEEDED FOR CONTINUOUS-INDUCTOR-CURRENT BOOST AND FLYBACK TOPOLOGIES.

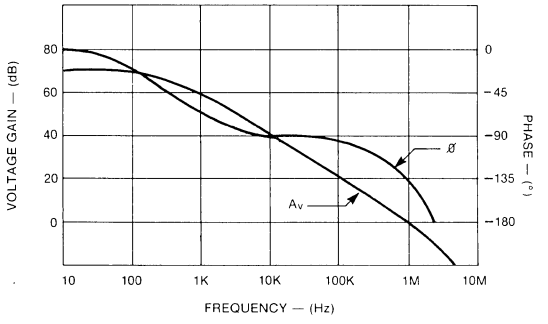

FIGURE 11. ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE.

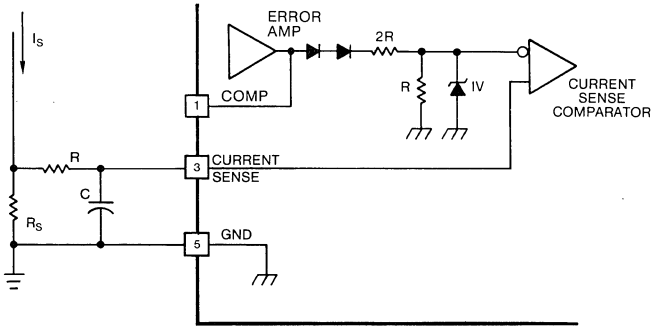

FIGURE 12. CURRENT SENSING.

R_S can be connected to the power circuit directly or through a current transformer, as Figure 13 illustrates. While a direct connection is simpler, a transformer can reduce power dissipation in R_S, reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-referenced sensing. The relation between v_C and peak current in the power stage is given by:

$$i_{(pk)} = N \left(\frac{V_{R_S\,(pk)}}{R_S} \right) = \frac{N}{3R_S} \left(v_C - 1.4V \right)$$

where: N = current sense transfomer turns ratio
= 1 when transformer not used.

For purposes of small-signal analysis, the control-to-sensed-current gain is:

$$\frac{i_{(pk)}}{v_C} = \frac{N}{3R_S}$$

When sensing current in series with the power transistor, as shown in Figure 13, the current waveform will often have a large spike at its leading edge. This is due to rectifier recovery and/or inter-winding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC3842 current-sense comparator is internally clamped to 1V (Figure 12). Current limiting occurs if the voltage at pin 3 reaches this threshold value, i.e. the current limit is defined by:

$$i_{MAX} = \frac{N \cdot 1V}{R_S}$$

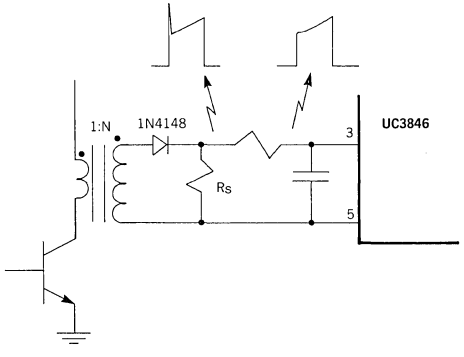

FIGURE 13. TRANSFORMER-COUPLED CURRENT SENSING.

Totem-Pole Output

The UC3842 has a single totem-pole output. The output transistors can be operated to ±1A peak current and ±200mA average current. The peak current is self-limiting, so no series current-limiting resistor is needed when driving a MOSFET gate. Cross-conduction between the output transistors is minimal, as Figure 14 shows. The average added power due to cross-conduction with V_{IN} = 30V is only 80mW at 200kHz.

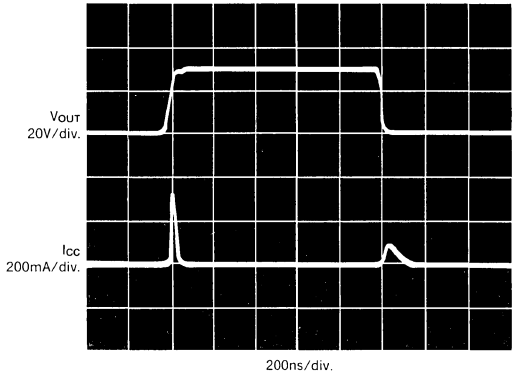

FIGURE 14. OUTPUT CROSS-CONDUCTION.

Figures 15-17 show suggested circuits for driving MOSFETs and bipolar transistors with the UC3842 output. The simple circuit of Figure 15 can be used when the control IC is not electrically isolated from the MOSFET. Series resistor R_1 provides damping for a parasitic tank circuit formed by the MOSFET input capacitance and any series wiring inductance. Resistor R_2 shunts output leakage currents (10μA maximum) to ground when the undervoltage lockout is active. Figure 16 shows an isolated MOSFET drive circuit which is appropriate when the drive signal must be level-shifted or transmitted across an isolation boundary. Bipolar transistors can be driven effectively with the circuit of Figure 17. Resistors R_1 and R_2 fix the on-state base current. Capacitor C_1 provides a negative base current pulse to remove stored charge at turn-off.

Since the UC3842 has only a single output, an interface circuit is needed in order to control push-pull or full bridge topologies. The UC3706 Dual Output Driver performs this function. A circuit example at the end of this paper illustrates a typical application for these two ICs. For more information on the UC3706, consult Reference 3.

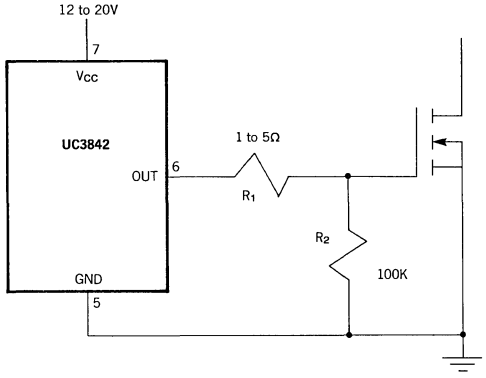

FIGURE 15. DIRECT MOSFET DRIVE.

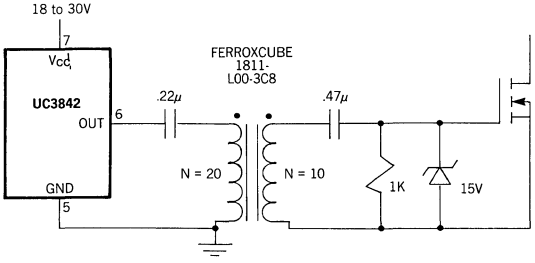

FIGURE 16. ISOLATED MOSFET DRIVE.

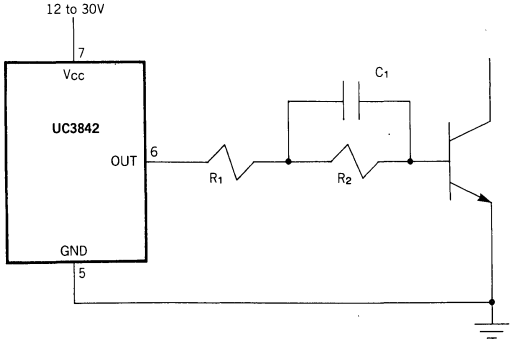

FIGURE 17. BIPOLAR DRIVE WITH NEGATIVE TURN-OFF BIAS.

PWM Latch

This flip-flop, shown in Figure 4, ensures that only a single pulse appears at the UC3842 output in any one oscillator period. Excessive power transistor dissipation and potential saturation of magnetic elements are thereby averted.

Shutdown Techniques

Shutdown of the UC3842 can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below 1V. Either method causes the output of the PWM comparator to be high (refer to block diagram, Figure 4). The PWM latch is reset dominant so that the output will remain low until the first clock pulse following removal of the shutdown signal at pin 1 or pin 3. As shown in Figure 18, an externally latched shutdown can be accomplished by adding an SCR which will be reset by cycling V_{CC} below the lower under-voltage lockout threshold (10V). At this point all internal bias is removed, allowing the SCR to reset.

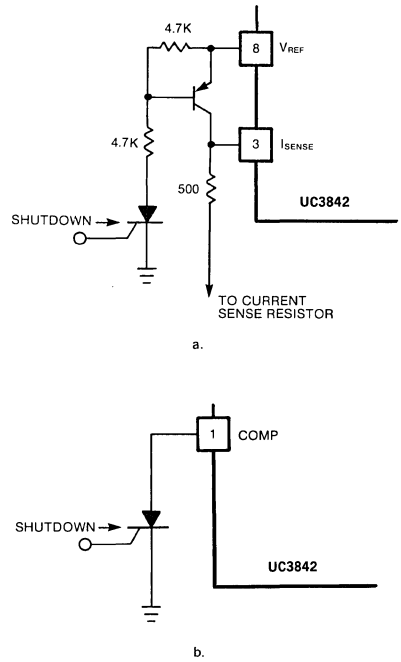

FIGURE 18. SHUTDOWN ACHIEVED BY
(a.) PULLING PIN 3 HIGH OR
(b.) PULLING PIN 1 LOW.

AVOIDING COMMON PITFALLS

Current-mode controlled converters can exhibit performance peculiarities under certain operating conditions. This section explains these situations and how to correct them when using the UC3842.

Slope Compensation Prevents Instabilities

It is well documented that current-mode controlled converters can exhibit subharmonic oscillations when operated at duty cycles greater than 50% (References 4, 5 and 6).

Fortunately, a simple technique (usually requiring only a single resistor to implement) exists which corrects this problem and at the same time improves converter performance in other respects. This "slope compensation" technique is described in detail in Reference 6. It should be noted that "duty cycle" here refers to output pulse width divided by oscillator period, even in push-pull designs where the transformer period is twice that of the oscillator. Therefore, push-pull circuits will almost always require slope compensation to prevent subharmonic oscillation.

Figure 19 illustrates the slope compensation technique. In Figure 19a the uncompensated control voltage and current sense waveforms are shown as a reference. Current is often sensed in series with the switching transistor for buck-derived topologies. In this case, the current sense signal does not track the decaying inductor current when the transistor is off, so dashed lines indicate this inductor current. The negative inductor current slope is fixed by the values of output voltage (V_O) and inductance (L):

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{-V_F - V_O}{L} = \frac{-(V_F + V_O)}{L}$$

where: V_F = forward voltage drop across the freewheeling diode. The actual slope (m_2) of the dashed lines in Figure 19a is given by:

$$m_2 = \frac{R_S}{N} \cdot \frac{di_L}{dt} = \frac{-R_S(V_F + V_O)}{NL}$$

where: R_S and N are defined as in the "Current Sensing" section of this paper.

In Figure 19b, a sawtooth voltage with slope m has been added to the control signal. The sawtooth is synchronized with the PWM clock, and in practice is most easily derived from the control chip oscillator as shown in Figure 20a. The sawtooth slope in Figure 19b is $m = m_2/2$. This particular slope value is significant in that it yields "perfect" current-mode control; i.e. with $m_2/2$ the *average* inductor current follows the control signal so that, in the small-signal analysis, the inductor acts as a controlled current source. All current-mode controlled converters having continuous inductor current therefore benefit from this amount of slope compensation, whether or not they operate above 50% duty.

More slope is needed to prevent subharmonic oscillations at high duty cycles. With slope $m = m_2$, such oscillations will not occur if the error amplifier gain ($A_{V(E/A)}$) at half the switching frequency ($f_s/2$) is kept below a threshold value (Reference 6):

$$A_{V(E/A)} \Big|_{\substack{m = m_2 \\ f = f_S/2}} < \frac{\pi^2 C_O}{4\tau}$$

where: C_O = sum of filter and load capacitances.
$\tau = 1/f_s$.

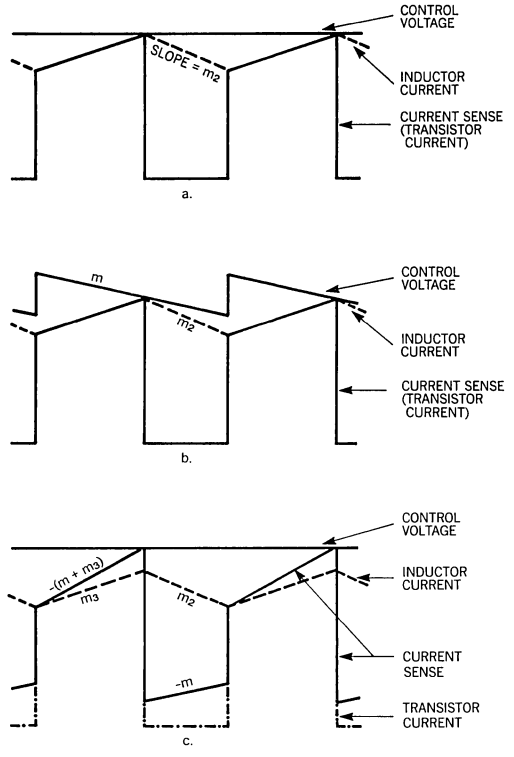

FIGURE 19. SLOPE COMPENSATION WAVEFORMS:
(a.) NO COMP.
(b.) COMP. ADDED TO CONTROL VOLTAGE.
(c.) COMP. ADDED TO CURRENT SENSE.

Slope compensation can also improve the noise immunity of a current-mode controlled supply. When the inductor ripple current is small compared to the average current (as in Figure 19a), a small amount of noise on the current sense or control signals can cause a large pulse-width jitter. The magnitude of this jitter varies inversely with the difference in slope of the two signals. By adding slope as in Figure 19b, the jitter is reduced. In noisy environments it is sometimes necessary to add slope $m > m_2$ in order to correct this problem. However, as m increases beyond $m = m_2/2$, the circuit becomes less perfectly current controlled. A complex trade-off is then required; for very noisy circuits the optimum amount of slope compensation is best found empirically.

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Once the required slope is determined, the value of R_{SLOPE} in Figure 20a can be calculated:

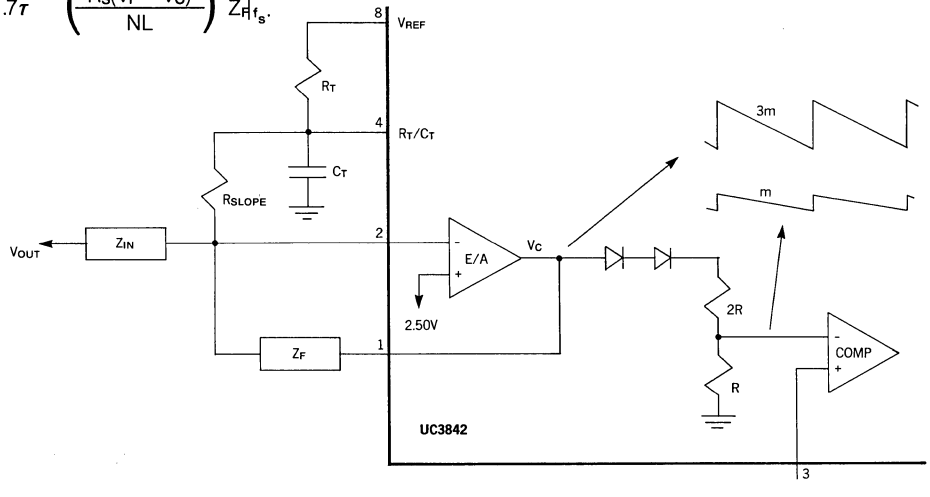
$$3m = \frac{\Delta V_{RAMP}}{\Delta t_{RAMP}} \cdot A_{V(E/A)} = \frac{0.7V}{\tau/2}\left(\frac{R_{SLOPE}}{Z_F|_{f_s}}\right) = \frac{1.4}{\tau}\left(\frac{R_{SLOPE}}{Z_F|_{f_s}}\right)$$

$$R_{SLOPE} = \frac{3m\tau}{1.4}\,(Z_F|_{f_s}) = 2.1 \cdot m \cdot \tau \cdot Z_F|_{f_s}$$

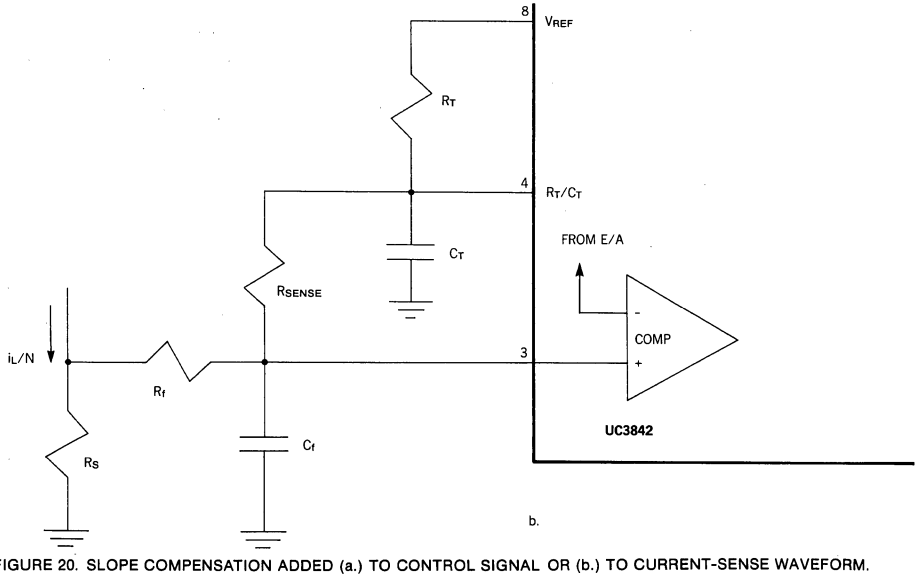
where: $Z_F|_{f_s}$ is the E/A feedback impedance at the switching frequency.

For $m = m_L$: $\Delta\tau_{RAMP}$

$$R_{SLOPE} = 1.7\tau \left(\frac{R_S(V_F + V_O)}{NL}\right) Z_F|_{f_s}.$$



a.



b.

FIGURE 20. SLOPE COMPENSATION ADDED (a.) TO CONTROL SIGNAL OR (b.) TO CURRENT-SENSE WAVEFORM.

Note that in order for the error amplifier to accurately replicate the ramp, Z_F must be constant over the frequency range f_s to at least $3f_s$.

In order to eliminate this last constraint, an alternative method of slope compensation is shown in Figures 19c and 20b. Here the artificial slope is added to the current sense waveform rather than subtracted from the control signal. The magnitude of the added slope still relates to the downslope of inductor current as described above. The requirement for R_{SLOPE} is now:

$$m = \frac{\Delta V_{RAMP}}{\Delta t_{RAMP}} \left(\frac{R_f}{R_f + R_{SLOPE}} \right) = \frac{0.7}{\tau/2} \left(\frac{R_f}{R_f + R_{SLOPE}} \right)$$

$$R_{SLOPE} = \frac{1.4R_f}{m\tau} - R_f = R_f \left(\frac{1.4}{m\tau} - 1 \right).$$

For $m = m_2$:

$$R_{SLOPE} = R_f \left(\frac{1.4NL}{R_S(V_F + V_O)\tau} - 1 \right).$$

R_{SLOPE} loads the UC3842 R_T/C_T terminal so as to cause a decrease in oscillator frequency. If $R_{SLOPE} >> R_T$ then the frequency can be corrected by decreasing R_T slightly. However, with $R_{SLOPE} \lesssim 5R_T$ the linearity of the ramp degrades noticeably, causing over-compensation of the supply at low duty cycles. This can be avoided by driving R_{SLOPE} with an emitter-follower as shown in Figure 21.

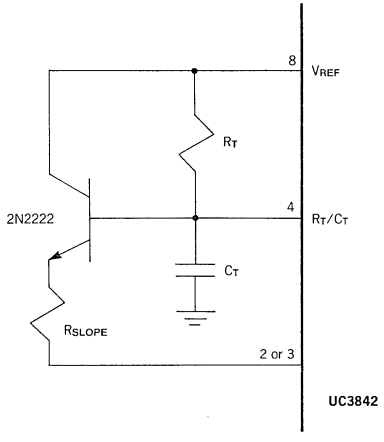


FIGURE 21. EMITTER-FOLLOWER MINIMIZES LOAD AT R_T/C_T TERMINAL.

Noise

As mentioned earlier, noise on the current sense or control signals can cause significant pulse-width jitter, particularly with continuous-inductor-current designs. While slope compensation helps alleviate this problem, a better solution is to minimize the amount of noise. In general, noise immunity improves as impedances decrease at critical points in a circuit.

One such point for a switching supply is the ground line. Small wiring inductances between various ground points on a PC board can support common-mode noise with sufficient amplitude to interfere with correct operation of the modulating IC. A copper ground plane and separate return lines for high-current paths greatly reduce common-mode noise. Note that the UC3842 has a single ground pin. High sink currents in the output therefore cannot be returned separately. If this causes erratic operation, then use the output to drive the high impedance input of a UC3706.

Ceramic bypass capacitors (.1μF) from V_{CC} and V_{REF} to ground will provide low-impedance paths for high frequency transients at those points. The input to the error amplifier, however, is a high-impedance point which cannot be bypassed without affecting the dynamic response of the power supply. Therefore, care should be taken to lay out the board in such a way that the feedback path is far removed from noise generating components such as the power transistor(s).

Figure 22a illustrates another common noise-induced problem. When the power transistor turns off, a noise spike is coupled to the oscillator R_T/C_T terminal. At high duty cycles the voltage at R_T/C_T is approaching its threshold level (~2.7V, established by the internal oscillator circuit) when this spike occurs. A spike of sufficient amplitude will prematurely trip the oscillator as shown by the dashed lines. In order to minimize the noise spike, choose C_T as large as possible, remembering that deadtime increases with C_T. It is recommended that C_T never be less than ~1000pF. Often the noise which causes this problem is caused by the output (pin 6) being pulled below ground at turn-off by external parasitics. This is particularly true when driving MOSFETs. A diode clamp from ground to pin 6 will prevent such output noise from feeding to the oscillator. If these measures fail to correct the problem, the oscillator frequency can always be stabilized with an external clock. Using the circuit of Figure 8 results in an R_T/C_T waveform like that of Figure 22b. Here the oscillator is much more immune to noise because the ramp voltage never closely approaches the internal threshold.

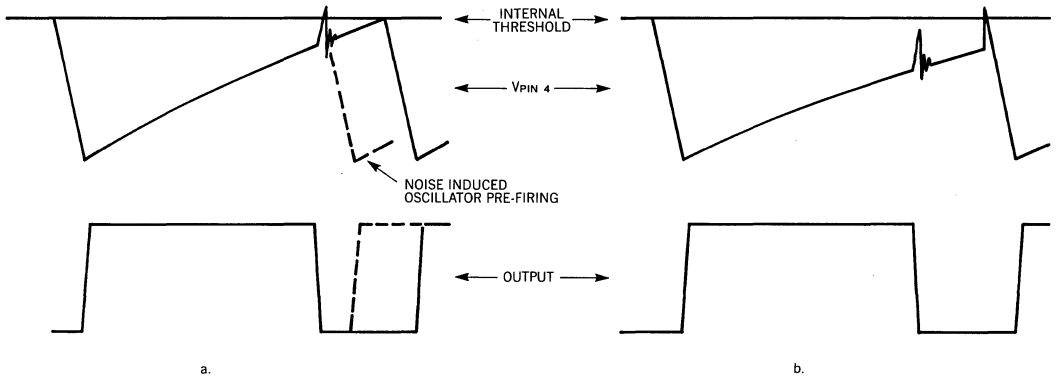


FIGURE 22. (a.) NOISE ON PIN 4 CAN CAUSE OSCILLATOR TO PRE-TRIGGER.
(b.) WITH EXTERNAL SYNC., NOISE DOES NOT APPROACH THRESHOLD LEVEL.

Maximum Operating Frequency

Since output deadtime varies directly with C_T, the restraint on minimum C_T (1000pF) mentioned above results in a minimum deadtime capability for the UC3842. This minimum deadtime varies with R_T and therefore with frequency, as shown in Figure 23. Above 100kHz, the deadtime significantly reduces the maximum duty cycle obtainable at the UC3842 output (also shown in Figure 23). Circuits not requiring large duty cycles, such as the forward converter and flyback topologies, could operate as high as 500kHz. Operation at higher frequencies is not recommended because the deadtime becomes less predictable.

The speed of the UC3842 current sense section poses an additional constraint on maximum operating frequency. A maximum current sense delay of 400ns represents 10% of the switching period at 250kHz and 20% at 500kHz. Magnetic components must not saturate as the current continues to rise during this delay period, and power semiconductors must be chosen to handle the resulting peak currents. In short, above ~250kHz, many of the advantages of higher-frequency operation are lost.

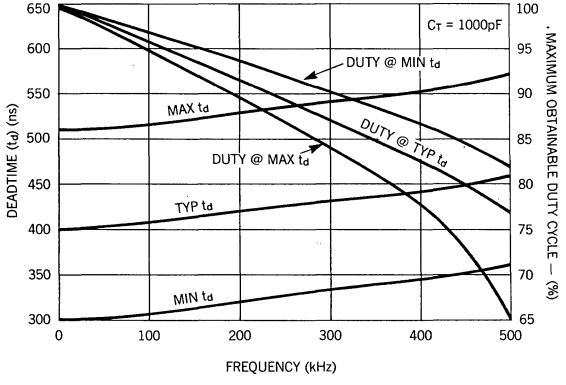


FIGURE 23. DEADTIME AND OBTAINABLE DUTY CYCLE VS. FREQUENCY WITH MINIMUM RECOMMENDED C_T.

Half-Bridge Topology

Figure 24 shows a typical half-bridge converter operable from either 110VAC or 220VAC. While okay at 110V with a fixed capacitor center-tap voltage, when operated from 220VAC, the input rectifiers act as a full-wave bridge and charge C_1 and C_2 in series. In this configuration, the circuit will always be unstable if current-mode controlled. While the input capacitors charge at the same rate, they will discharge at different rates because the modulator will imbalance the pulse widths in order to provide symmetry correction for the transformer. This is a runaway condition which will quickly cause all of the input voltage to appear across one capacitor only. While a resistive voltage divider connected in parallel with C_1 and C_2 would correct the problem, power dissipation in the resistors would be prohibitively large. A capacitor in series with the transformer primary provides no correction for this particular problem.

CIRCUIT EXAMPLES

1. Off-Line Flyback

Figure 25 shows a 25W multiple-output off-line flyback regulator controlled with the UC3842. This regulator is low in cost because it uses only two magnetic elements, a primary-side voltage sensing technique, and an inexpensive control circuit. Specifications are listed below. For a more detailed description of this circuit, consult Reference 7.

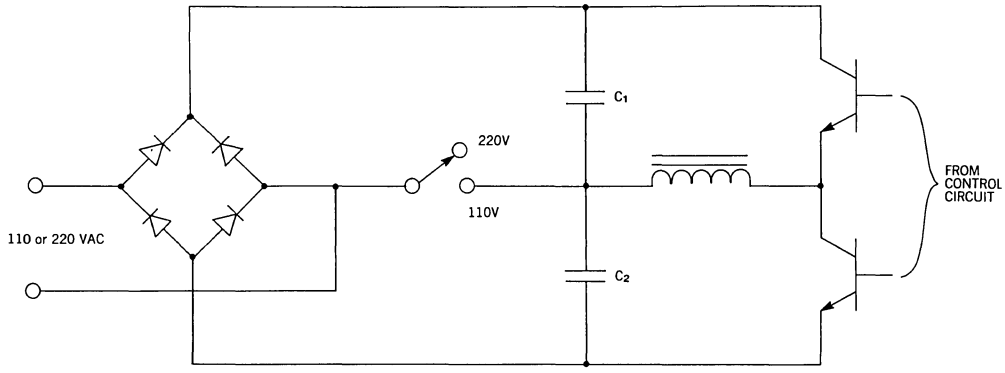


FIGURE 24. HALF-BRIDGE CIRCUIT IS NOT STABLE WHEN C_1 AND C_2 CHARGE IN SERIES AND TRANSISTORS ARE CURRENT-MODE CONTROLLED.

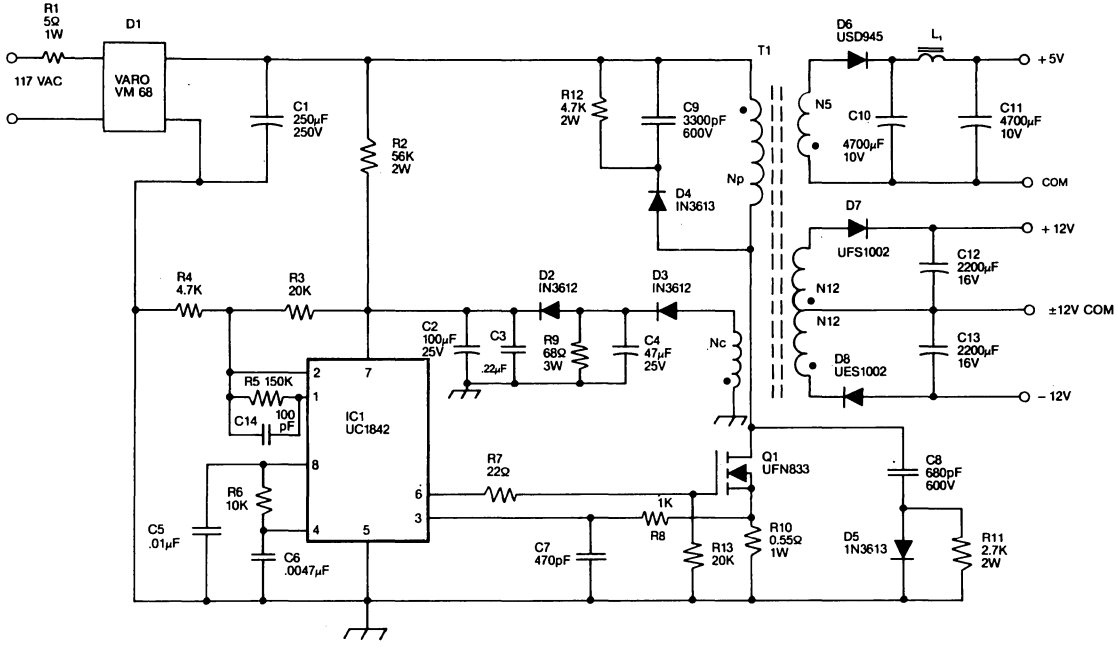
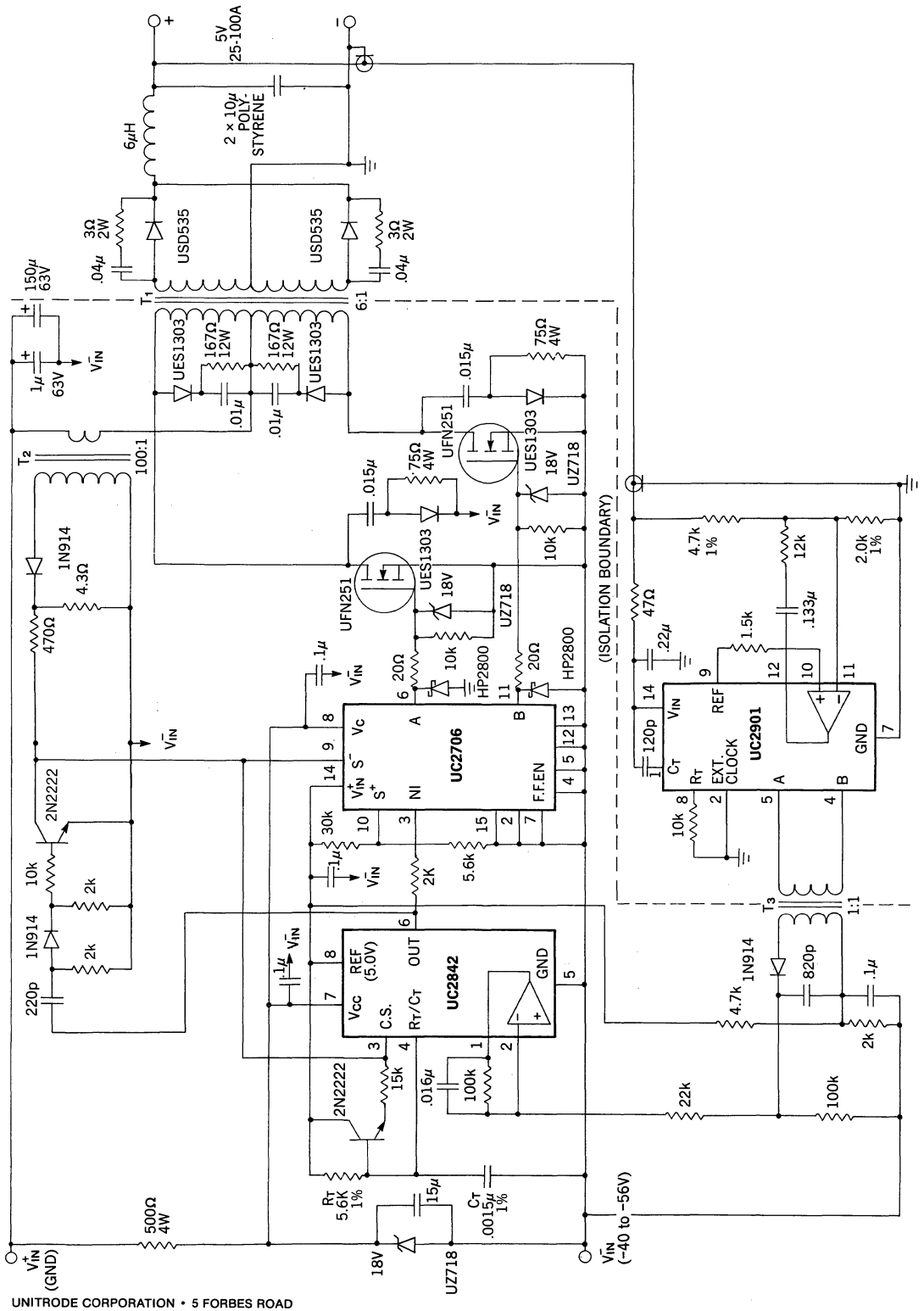


FIGURE 25. 25W OFF-LINE FLYBACK REGULATOR.



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1. Off-Line Flyback (continued)

SPECIFICATIONS:

Input Voltage:		95VAC to 130VAC (50Hz/60Hz)
Output Voltage:	A.	+5V, 5%: 1A to 4A load Ripple voltage: 50mV P-P Max
	B.	+12V, 3%: 0.1A to 0.3A load Ripple voltage: 100mV P-P Max
	C.	-12V, 3% 0.1A to 0.3A load Ripple voltage: 100mV P-P Max
Line Isolation:		3750 Volts
Switching Frequency:		40kHz
Efficiency @ full load:		70%

2. DC-To-DC Push-Pull Converter

Figure 26 is a 500W push-pull DC-to-DC converter utilizing the UC3842, UC3706 and UC3901 ICs. It operates from a standard telecommunications bus to produce 5V at up to 100A. Operation of this circuit is detailed in Reference 8.

SPECIFICATIONS:

Input Voltage:	-48V ± 8V
Output Voltage:	+5V
Output Current:	25A to 100A
Oscillator Frequency:	200kHz
Line Regulation:	0.1%
Load Regulation:	1%
Efficiency @ V_{IN} = 48V	
I_O = 25A:	75%
I_O = 50A:	80%
Output Ripple Voltage:	200mV P-P

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ACKNOWLEDGMENT

Lloyd Dixon was instrumental in clarifying the half-bridge problem.

200KHz CURRENT-MODE CONVERTER PROVIDES 500W

This Application Note describes a push-pull converter which develops up to 100A at 5V from a standard 48V input. It provides equations used to specify all critical components, so that a designer can adapt the circuit to meet a different set of requirements. Specifications, performance data, and waveform photographs are included. The schematic appears in Figure 1.

SPECIFICATIONS

Input Voltage ..... −48V ± 8V
Output Voltage ..... +5V
Output Current ..... 25A to 100A
Short-Circuit Current 120A
Oscillator Frequency 200KHz
Line Regulation 0.12%
Load Regulation 0.25%
Efficiency 75%
Output Ripple Voltage 300mV
Large-Signal Output Slew Rate 30A/ms

PERFORMANCE DATA

Test Conditions		Performance			
I_O	V_{IN}	V_O	I_{IN}	Efficiency	Ripple
(A)	(V)	(V)	(A)	(%)	(mV p-p)
25	40	5.002	3.9	80	50
25	56	4.996	3.0	75	75
50	40	5.000	7.8	80	100
50	56	4.995	5.8	77	150
75	40	5.000	11.8	79	200
75	56	4.996	8.6	78	220
100	40	4.990	16.7	75	250
100	56	4.990	11.8	76	300

OVERVIEW[1, 2, 3, 4]

This design utilizes a center-tap push-pull topology operating with continuous inductor current and current-mode control. This push-pull configuration optimizes transformer utilization while allowing common-source operation of the power MOSFETs.

Current-mode control was chosen for this application for several reasons. Power transformer flux balancing is achieved without the cost of added sensing circuits. The filter inductor behaves like a current source, which allows a closed-loop frequency response of greater bandwidth than would otherwise be possible for stable operation. More importantly, the error amplifier compensation becomes simpler and better behaved under conditions of large-signal load changes.[4] Finally, current-mode control provides instantaneous (single-cycle) correction for input voltage variations.

The UC2842 pulse width modulator provides all these advantages at an extremely low cost. Since this IC has only a single output, a UC2706 Dual Output Driver is used to perform a single-ended to push-pull conversion. The UC2706 provides the added advantages of rapid (180ns) current limiting and high peak current MOSFET drive needed to operate at high frequencies. Since input-to-output isolation is required, a UC2901 Isolated Feedback Generator is employed to return a feedback signal from the output to the primary-side PWM controller.

Block diagrams of these three ICs appear in Figures 2-4. Waveforms at critical circuit points are shown in Figures 5-8.

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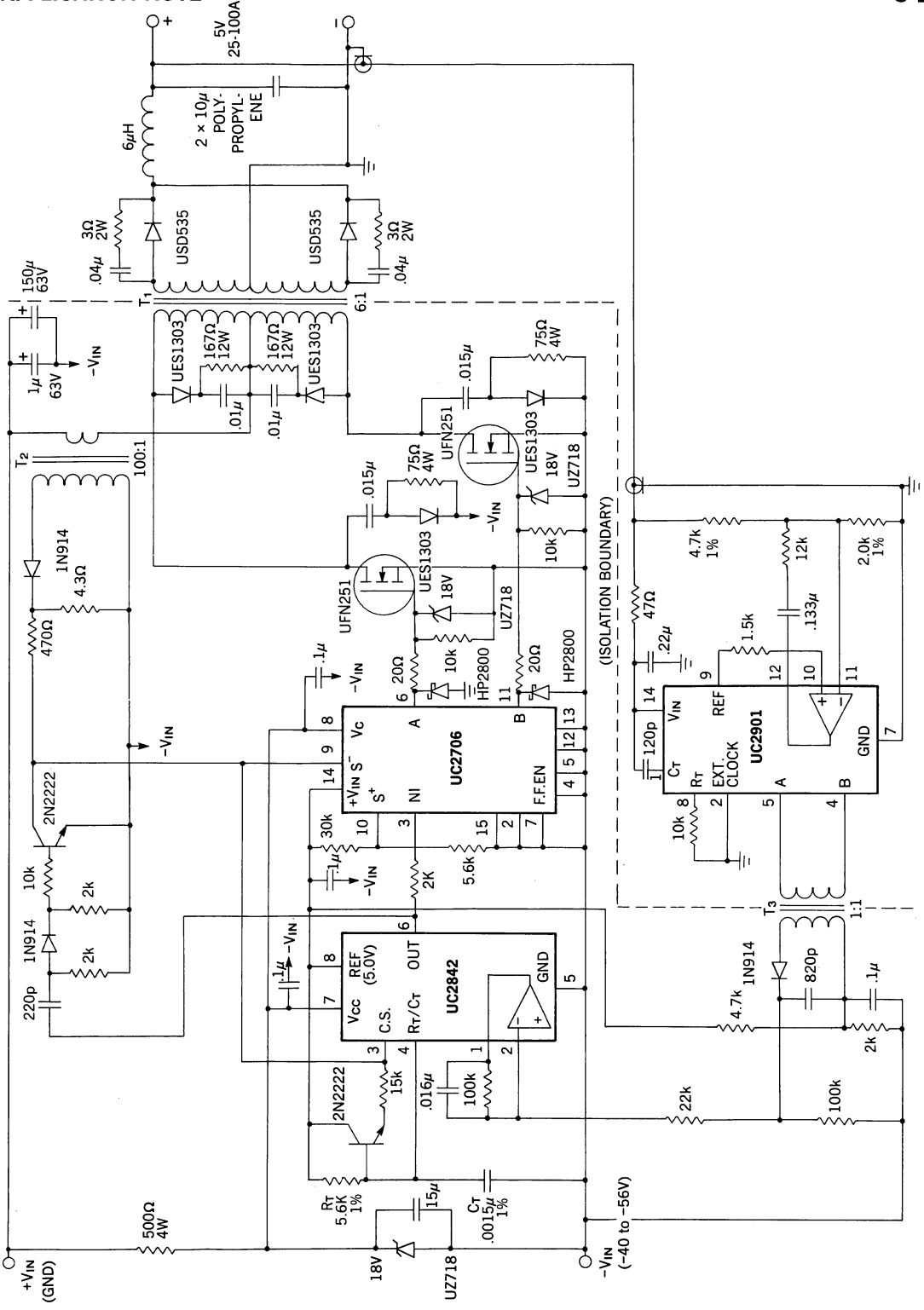

FIGURE 1. 500W PUSH-PULL DC-TO-DC CONVERTER.

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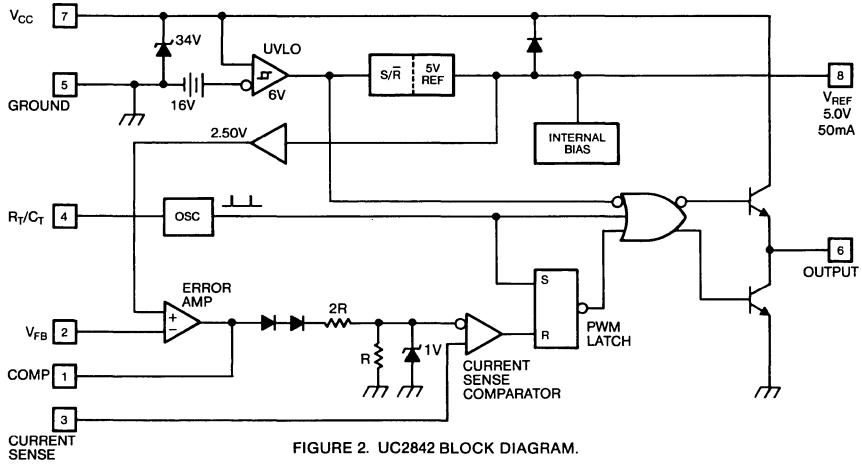

FIGURE 2. UC2842 BLOCK DIAGRAM.

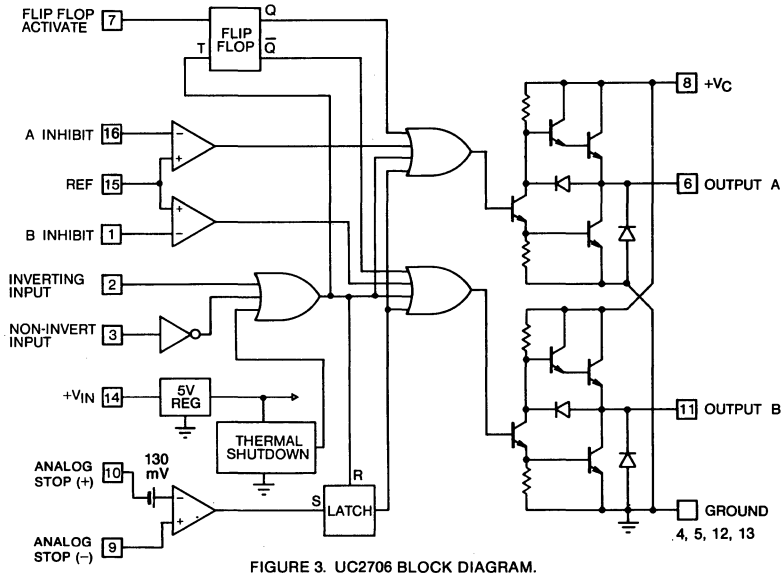

FIGURE 3. UC2706 BLOCK DIAGRAM.

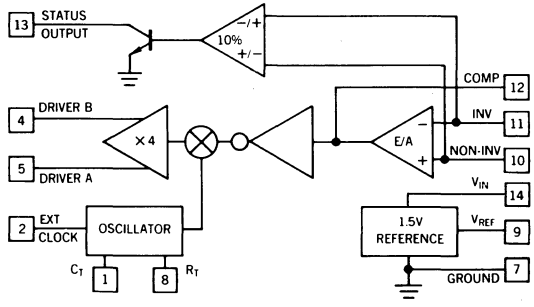

FIGURE 4. UC2901 BLOCK DIAGRAM

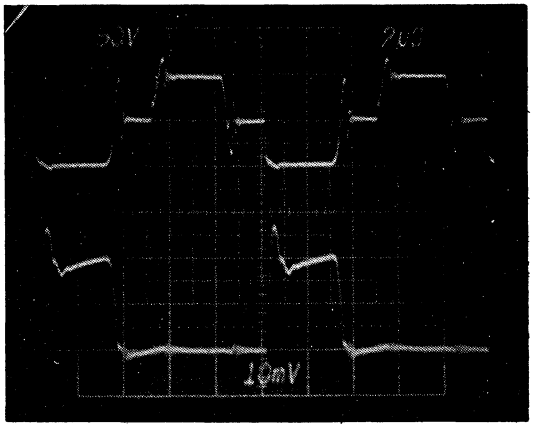

FIGURE 5. TOP: MOSFET V_{DS} @ 50V/div.
BOTTOM: MOSFET I_D @ 5A/div.
2μs/div.

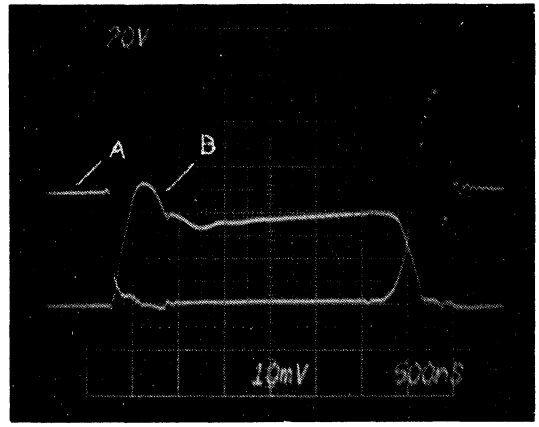

FIGURE 6. A: MOSFET V_{DS} @ 20V/div.
B: MOSFET I_D @ 5A/div.
500ns/div.

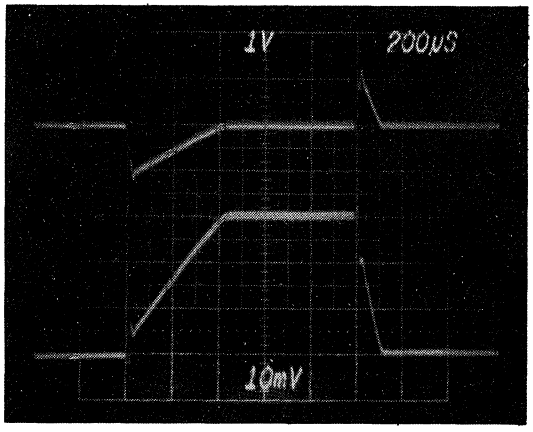

FIGURE 7. LARGE-SIGNAL OUTPUT SLEW RATE.
TOP: OUTPUT VOLTAGE @ 1V/div.
BOTTOM: OUTPUT CURRENT @ 5A/div.
200μs/div.

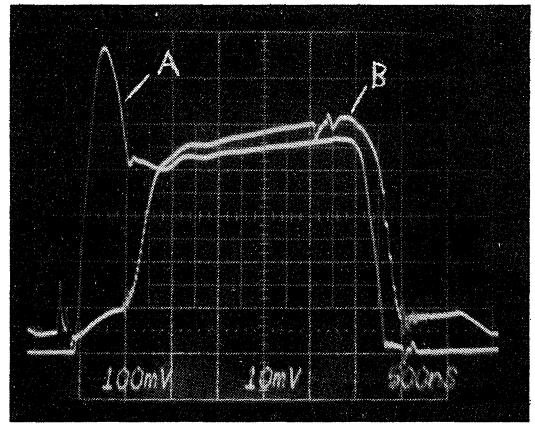

FIGURE 8. A: MOSFET I_D @ 2A/div.
B: CURRENT SENSE (UC2842 — PIN 3) @ 100mV/div.
500ns/div.

DESIGN EQUATIONS

Power Transformer[5]

Several design iterations resulted in the choice of a Ferroxcube EC52-3C8 ferrite core for the power transformer. This is the smallest EC core with a wire window area A_w large enough for the required high-current windings.

For this buck-derived converter, duty cycle D is given by:

$$D = \frac{(V_O + V_F)N}{V_{IN} - V_{DS(ON)}}$$

where: V_O, V_F, V_{IN} and $V_{DS(ON)}$ are defined as in Figure 9.

N = primary-to-secondary turns ratio (N_P/N_S).

This equation is used for selecting N to give an optimum range of D as V_{IN} varies from 40V to 56V. D should be as large as possible in order to minimize peak currents, but not so large that circuit delays and losses limit D when V_{IN} = 40V.

For this design, N = 5 was chosen so that:

$$D_{MAX} \approx \frac{(5V + .6V)5}{40V - 1V} = .72$$

$$D_{MIN} \approx \frac{(5V + .6V)5}{56V - 1V} = .51$$

Next, the minimum number of primary turns required to prevent core saturation is determined from the following equation:[5]

$$N_P > \frac{V_{IN(MIN)}\, t_{ON(MAX)}}{\Delta B\, A_e} \cdot 10^8$$

where: ΔB = maximum flux swing (Gauss).
A_e = effective magnetic area (cm^2).

A safe peak operating flux density for 3C8 ferrite is ~2500 Gauss (saturation occurs at ~ 3000 Gauss). Therefore, B = 2 × 2500 = 5000 Gauss for push-pull operation.

$$N_P > \frac{40V \cdot 5\mu s}{5000G \cdot 1.83\ cm^2} \cdot 10^8 = 2.2$$

This design uses N_P = 5, N_S = 1.

Wire size requirements are determined by the worst-case RMS current in each winding. Refer to Figure 9.

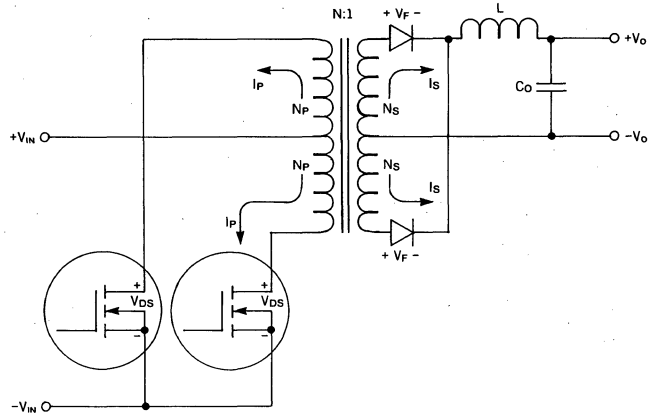

FIGURE 9. BASIC PUSH-PULL POWER CIRCUIT AND FILTER.

Primary:

$$I_{P(AVG)(MAX)} = \frac{\frac{1}{2} P_{IN(MAX)}}{V_{IN(MIN)} - V_{DS(ON)}} \approx \frac{P_{O(MAX)}}{2\eta(V_{IN(MIN)} - V_{DS(ON)})}$$

$$= \frac{500W}{2(.75)(40V - 1V)} = 8.5A$$

$$I_{P(PK)(MAX)} = \frac{I_{P(AVG)(MAX)}}{\frac{1}{2} D_{MAX}} = \frac{8.5A}{\frac{1}{2}(.72)} = 24A$$

$$I_{P(RMS)(MAX)} = I_{P(PK)(MAX)} \sqrt{\frac{1}{2} D_{MAX}} = 24A \sqrt{\frac{1}{2}(.72)}$$

$$= 14A$$

Secondary:

$$I_{S(RMS)(MAX)} = \sqrt{I^2_{O(MAX)} (\frac{1}{2} D_{MAX}) + \left(\frac{I_{O(MAX)}}{2}\right)^2 (1 - D_{MAX})}$$

$$= \sqrt{(100A)^2 (\frac{1}{2})(.72) + \left(\frac{100A}{2}\right)^2 (1 - .72)}$$

$$= 66A$$

For a core with an "area product" $AP=(A_e A_W)$, an RMS current density of:

$J = 450 (AP)^{-.125}$ A/cm^2

gives a core temperature rise of ~30°C above ambient for natural convection cooling.[5] For an EC-52, AP = 5.7cm^4, and:

$J = 450 (5.7)^{-.125}$ A/cm^2 = 362 A/cm^2.

The required wire cross-sectional areas A_X are:

Primary:

$A_{XP} = \frac{14A}{362A/cm^2} = .039$ cm^2; used 4 parallel AWG18 for A_{XP} = .033 cm^2.

Secondary:

$A_{XS} = \frac{66A}{362A/cm^2} = .18$ cm^2; used 3 parallel copper straps, each 20 × 400 mil, giving A_{XS} = .16 cm^2.

OUTPUT FILTER

The filter capacitor (C_O) and inductor (L) are chosen to minimize output ripple voltage (v_R) while allowing fast response to a changing load. This design uses a polypropylene capacitor with extremely low ESR (7mΩ), allowing relatively high ripple currents, a small L, and therefore good large-signal dynamic response.

Maximum ripple current $i_{R(MAX)}$ occurs at minimum duty cycle and relates to $v_{R(MAX)}$ as follows:

$$i_{R(MAX)} = \frac{v_{R(MAX)}}{\frac{\tau D_{MIN}}{2C_O} + ESR} = \frac{200mV}{\frac{5\mu s(.51)}{2(20\mu F)} + 7m\Omega} = 2.8A.$$

The inductance requirement:

$$L_{MIN} = \left(\frac{V_{IN(MAX)}}{N} - V_F - V_O\right) \frac{\tau D_{MIN}}{i_{R(MAX)}}$$

$$= \left(\frac{56V}{5V} - 0.6V - 5V\right) \frac{5\mu s(.51)}{2.8A} = 5.1\mu H.$$

An Arnold A325360-2 ferrite toroid was chosen. It has an inductance index A_L of 360mH/1000 turns; the required number of turns T is:

$$T \geq \sqrt{\frac{10^6 \cdot L_{MIN(mH)}}{A_L}} = \sqrt{\frac{10^6 (.0051)}{360}} = 3.8.$$

Four turns gives L = 5.8μH. Wire size is given by:

$J_L = 450(8.64)^{-.125}$ A/cm^2 = 344 A/cm^2.

$A_{XL} = \frac{100A}{344\ A/cm^2} = .29$ cm^2; used 12 parallel AWG14 for A_{XL} = .25 cm^2.

CURRENT SENSING AND LIMITING

A current sense transformer is used to lower power dissipation in the sense resistor and to provide level shifting. A 100:1 turns ratio allows use of a 1/4 - Watt resistor. Large spikes occur at the leading edge of each current sense pulse as the junction capacitances of the secondary-side rectifiers are charged. If unattenuated, these spikes would falsely activate the current limit section of the control circuit. Therefore, the circuit of Figure 10 is used to blank the current sense signal during the first 200nS of each power pulse.

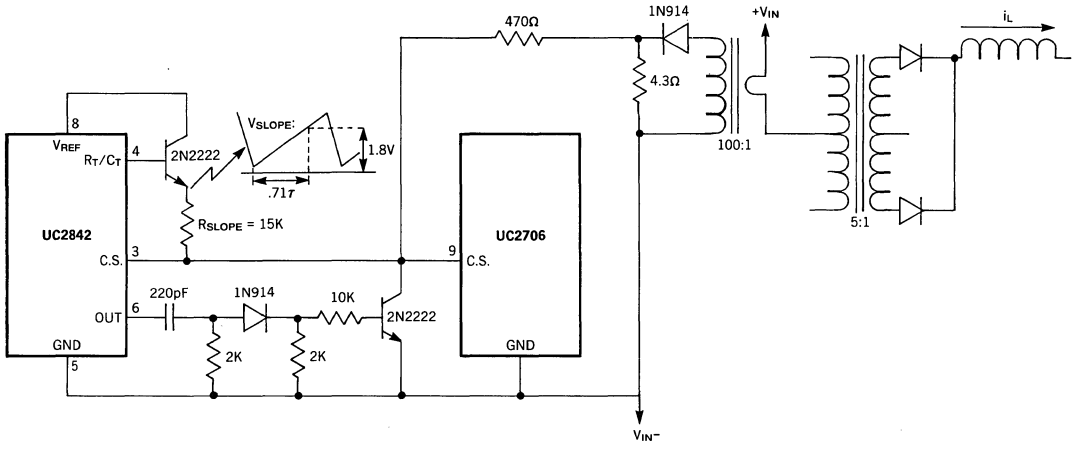

FIGURE 10. CURRENT SENSE WITH SPIKE SUPPRESSION AND SLOPE COMPENSATION.

Current limiting is performed by the UC2706 in order to achieve the fastest possible response. The UC2706 current limit threshold V_{TH} is programmed to be less than the 1 volt threshold of the UC2842.

$$V_{TH} = \frac{I_{O(MAX)}}{NN'} \cdot R_S + V_{SLOPE}\Big|_{D = .72}$$

$$= \frac{100A}{5(100)} \cdot 4.3\ \Omega + \frac{1.8V(470\Omega)}{15K\Omega + 470\Omega} = .91V$$

$$V_{PIN\ 10} = V_{TH} - .13V = .78V$$

CONTROL LOOP COMPENSATION[4]

1. Relevant Data:

f_S = 200KHz, τ = 5μs
40V ≤ V_{IN} ≤ 56V
V_O = 5V, 25A ≤ I_O ≤ 100A
0.2 Ω ≥ R_O ≥ 0.05Ω
I_{SC} = 120A

$i_{R(MAX)}$ = 2.8A
0.51 ≤ D ≤ 0.72
C_O = 20μF
ESR = 7mΩ
N = 5, N′ = 100 (transformer turns ratios)

2. Control-to-Output Response:

For the UC2842, the small signal control-to-inductor-current gain is given by:[1]

$$\frac{i_L}{V_C} = \frac{NN'}{3\ R_S}$$

The control-to-output-voltage gain is:

$$\frac{V_O}{V_C} = \frac{i_L}{V_C} \cdot R_O \cdot H_f(s)$$

$$= \frac{NN'\ R_O}{3\ R_S}\left(\frac{1 + s(2\pi \cdot ESR \cdot C_O)}{1 + s(2\pi \cdot R_O \cdot C_O)}\right)$$

Note that this response is load dependant:

a. At maximum load (minimum R_O):

$$\frac{V_O}{V_C}\Big|_{f \to o} = \frac{5(100).05\Omega}{3(4.3\Omega)} = 1.9$$

= 5.7dB (low frequency gain)

$f_P = 1/(2\pi(.05\Omega)\ 20\mu F)$
= 160KHz (filter pole frequency)

$f_Z = 1/(2\pi(7m\Omega)\ 20\mu F)$
= 1.1MHz (filter zero frequency)

b. At minimum load (maximum R_O):

$$\frac{V_O}{V_C}\Big|_{f \to o} = \frac{5(100)0.2\Omega}{3(4.3\Omega)} = 7.8 = 18dB$$

$f_P = 1/(2\pi(0.2\Omega)\ 20\mu F)$ = 40KHz

f_Z = 1.1MHz

These responses are plotted in Figure 11.

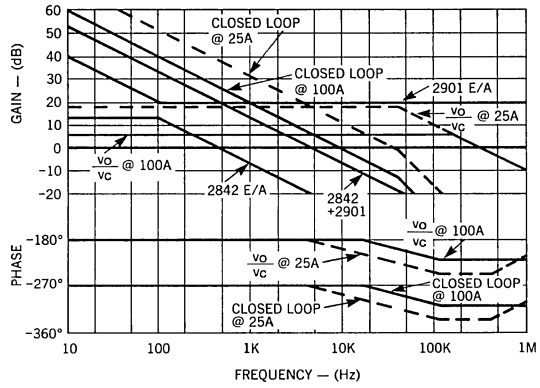

FIGURE 11. SMALL SIGNAL FREQUENCY RESPONSE.

3. Desired Closed-Loop Response:

While high gain-bandwidth is desired for fast response to dynamic loads, two stability criteria limit the achievable response characteristic. The Nyquist criterion dictates that phase margin above −360° be maintained at the frequency (f_c) at which gain crosses 0dB. Furthermore, it has been shown[6] that f_c must satisfy the following relation:

$$f_c \leq \frac{f_s}{2\pi D}$$

Using D = 0.9 to provide some margin for component tolerances,

$$f_c \approx \frac{200KHz}{2\pi(0.9)} = 35KHz.$$

4. Error Amplifier Compensation for UC2901 and UC2842:

Figure 11 shows a combined UC2901-UC2842 response curve which, when added to the control-to-output curves, yields a loop response which meets the above-mentioned stability criteria. One way of achieving this combined response is also indicated. Design equations and compensation components are shown in Figure 12.

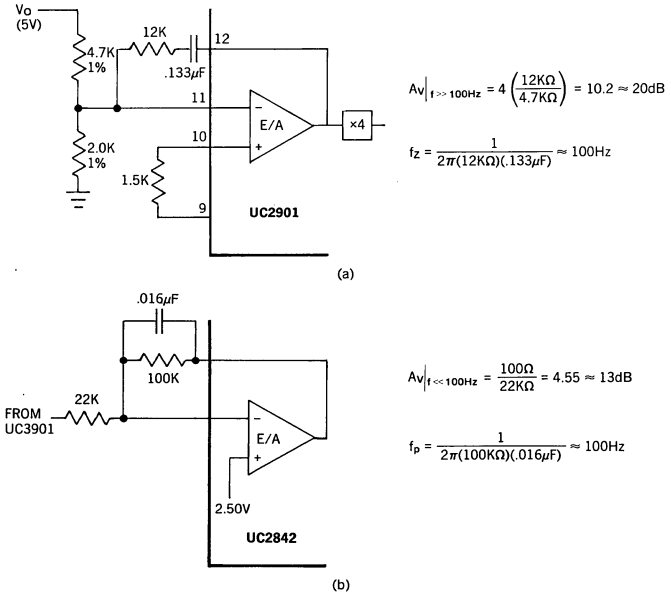

FIGURE 12. ERROR AMPLIFIER COMPENSATION FOR (a) UC2901 AND (b) UC2842.

SLOPE COMPENSATION

Current-mode converters operated with D $\gtrsim$ 0.5 require "slope compensation" to prevent subharmonic oscillations.[7, 8, 9] In particular, if an artificial ramp is added to the current sense waveform, and if the slope magnitude of that ramp equals the deadband downslope of the inductor current (as projected to the current sense point), then any perturbations in inductor current will die out within a single cycle.[7] A resistor R_{SLOPE} connected from the timing capacitor to the current sense input can provide this ramp. Referring to Figure 10, the required value of R_{SLOPE} for the UC2842 is given by:[1]

$$R_{SLOPE} = R_f \left(\frac{(1.4V)\ NN'L}{R_S(V_O + V_F)\ T} - 1 \right)$$

$$= 470\Omega \left(\frac{1.4V(5)100(5.8\mu H)}{4.3\Omega\ (5.6V)5\mu S} - 1 \right) = 15K\Omega.$$

The emitter follower in Figure 10 prevents R_{SLOPE} from increasing the oscillator frequency.

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UC1637/2637/3637
SWITCHED MODE CONTROLLER FOR DC MOTOR DRIVE

INTRODUCTION

There is an increasing demand today for motor control circuits, as a result of the incredible proliferation of automated position control equipment, which is itself made possible by recent developments in the field of digital computation.

The UC1637 Switched Mode Controller for DC motors is one of several integrated circuits offered by Unitrode for motor controls. This Application Note presents the general principles of its operation and the circuit details that optimize its use. As an illustration we will carry out an actual design, which will involve not only the UC1637, but also a power H-bridge using MOSFET transistors, and a modern DC motor tachometer. Using the tach output and UC1637's error amplifier, we will close the velocity control loop after a brief analysis of the factors that affect the feedback loop stability.

To achieve high efficiency power amplification, the UC1637 uses pulse width modulation, or PWM. This technique is employed today in many different circuits where power losses must be minimized, and is most suitable in applications involving inductive loads such as motors, voice coils, etc.

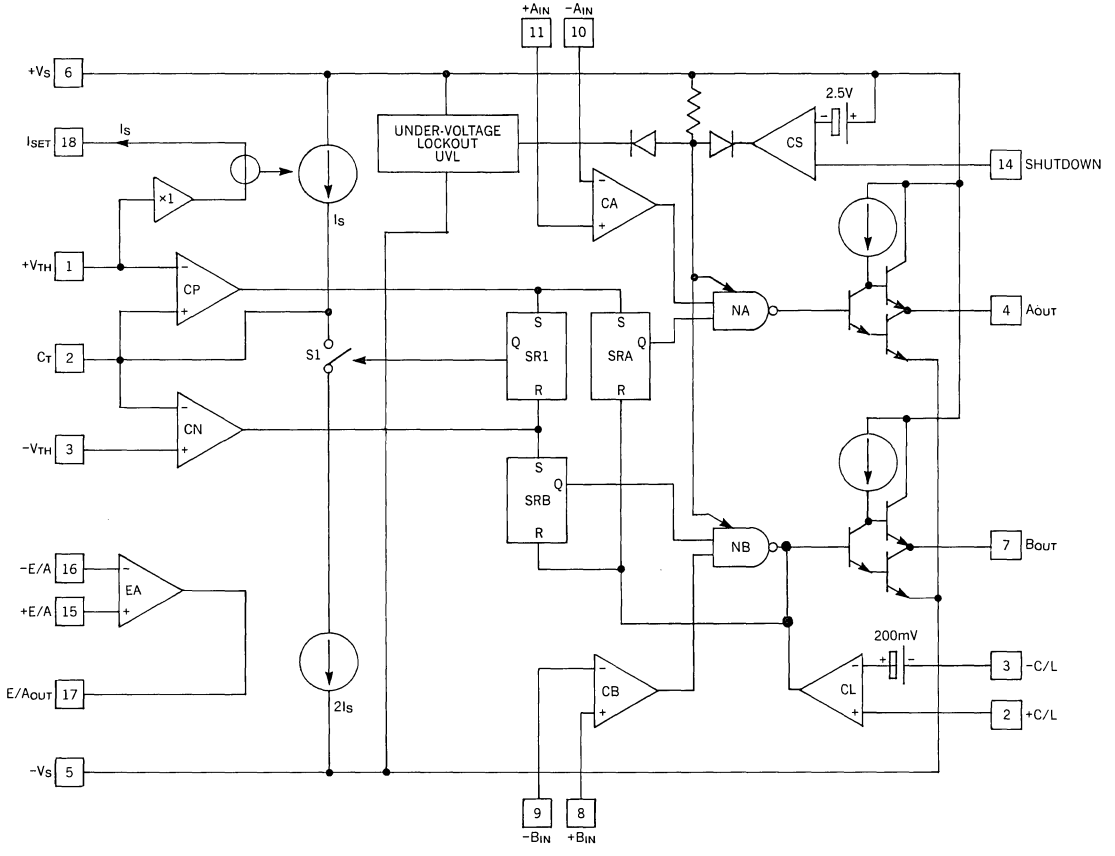

FIGURE 1. BLOCK DIAGRAM OF UC1637.

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PULSE WIDTH MODULATION (PWM)

The function of a power amplifier is to regulate the flow of energy from a power supply to a load, under the control of an input signal. A linear amplifier does this by interposing a controlled voltage drop in series with the load, while carrying the full load current. The product of this voltage and current represents the amount of power that must be dissipated by the amplifier itself, and it is easy to see that the method is not very efficient. In fact, its usefulness diminishes rapidly as the amount of power to be controlled increases and, at some point, a more efficient method becomes imperative.

PWM is a switching technique in which the supply voltage is fully applied (switched) to the load and then removed, the "on" and "off" times being precisely controlled. The effect on the load is the same as if some lower voltage were continuously applied whose value depended on the duty-cycle, that is, the ratio of "on" time to the full switching period. Since supply current only flows during the "on" times, it is apparent that the efficiency should be much higher than in the linear amplifier, as in fact it is. Still, switching transistors have small but finite "on" voltages and transition times, all of which introduce losses, which limit practical PWM efficiencies to something between 75% and 90%.

THE UC1637

The diagram of Figure 1 shows in block form the internal organization of the device. The main functions are:

A) Triangular wave generator; CP, CN, S1, SR1
B) PWM comparators; CA, CB
C) Output control gates; NA, NB
D) Current limit; CL, SRA, SRB
E) Error amplifier; EA
F) Shutdown comparator; CS
G) Undervoltage lockout; UVL

The two output lines, A_{OUT} and B_{OUT}, are meant to drive the two legs of an H-bridge power amplifier, with the load driven in bipolar fashion. The A_{OUT} and B_{OUT} outputs themselves are rated at 500mA peak and 100mA continuous, which makes it easy to interface the device with most amplifiers.

In order to generate two PWM output signals, we first produce a triangular waveform, or linear ramp. This is done by charging a capacitor C_T (pin 2) with constant current I_S until the comparator CP, with a fixed threshold voltage of $+V_{TH}$, delivers a pulse to "set" the SR1 latch circuit. This forces Q high, which closes the switch S1 and adds a negative current, $2\times I_S$, to the node of pin 2. As a result, a net current equal to I_S now flows out of C_T, discharging it linearly until the comparator CN resets SR1, and the cycle restarts. Thus, the voltage at pin 2 ramps continuously between $-V_{TH}$ and $+V_{TH}$ at a frequency that depends on these two threshold voltages, on C_T, and on I_S.

The current I_S is programmed by means of a resistor connected to pin 18. The voltage at this pin is equal to $+V_{TH}$ and an internal current mirror forces the charging current I_S to be equal to the current flowing out of pin 18. If a resistor R_S is connected from pin 18 to $-V_S$ (pin 5) instead of to ground, the ramp frequency becomes independent of power supply voltage variations, since I_S will then change together with V_{TH}.

As Figure 2 shows, a triangular waveform can be compared with a reference voltage to generate a PWM signal. The UC1637 uses two separate comparators to generate the two output signals A_{OUT} and B_{OUT}. The way the signals are handled, and the results, are shown in Figure 3 where it can be seen that the difference between V_A and V_B is the cause of the time intervals during which both outputs are low.

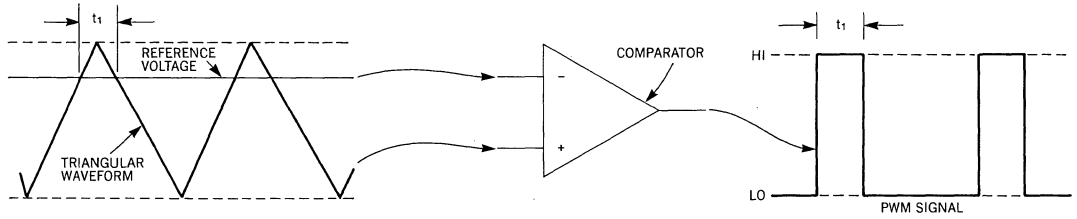

FIGURE 2. HOW A PWM SIGNAL IS GENERATED.

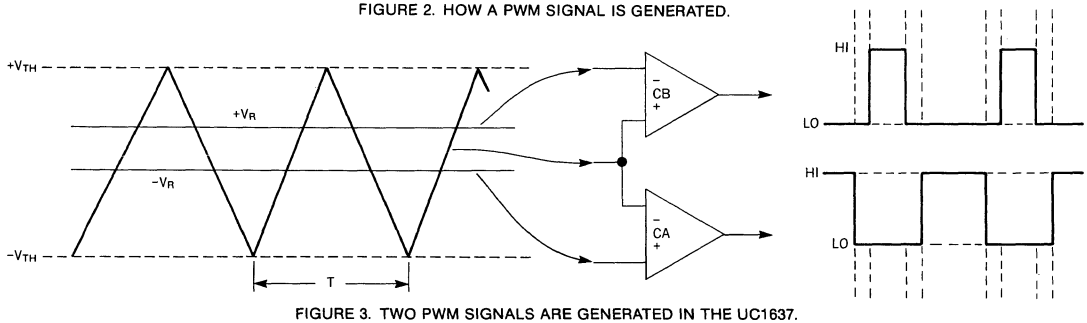

FIGURE 3. TWO PWM SIGNALS ARE GENERATED IN THE UC1637.

The two nand gates, NA and NB, will be enabled if the following two conditions are met:

A) supply voltage $+V_S$ is greater than +4.15 volts (typ)
B) the shut-down input line (pin 14) is at least 2.5 volts (typ) negative with respect to $+V_S$.

If these are satisfied, the A_{OUT} output line will be high if the CA output *and* Q of SRA are both high. Since SRA is set at each positive peak of the oscillator ramp, the output A_{OUT} can be controlled by CA singly — as long as a current-limit pulse from CL does not occur. The operation of the NB gate is similar.

The timing diagrams of Fig. 4 show the sequence of events before and after a current limit pulse occurs. Before time t_1 the PWM action is smoothly controlled by the ramp comparisons with V_A and V_B. The pulse from CL at time t_1 resets both SRA and SRB; the output lines are now disabled until SRA is set (at time t_2) and SRB is set (at time t_3).

The current limit comparator CL provides a means to protect both driver and motor from the consequences of very high currents. If the current delivered by the driver to the motor is made to flow through a low value resistor (for example, see R_S in Figure 7) the voltage drop across this resistor will be a measure of motor current. This voltage is applied between pins 12 and 13 of the UC1637, with pin 12 positive. A 200mV threshold is provided internally (see Figure 1) so that when the R_S voltage is equal to 200mV, the output of CA goes high, resetting both SRA and SRB and, consequently, terminating any active output pulse. This pulse-by-pulse method of current limiting is very fast and provides effective protection, not only for the driver components, but also for the motor, where the possibility of demagnetization due to excessive current is a matter of serious concern.

Finally, the UC1637 contains also an operational amplifier, EA, that can be used to provide gain and phase compensation, as will be seen later.

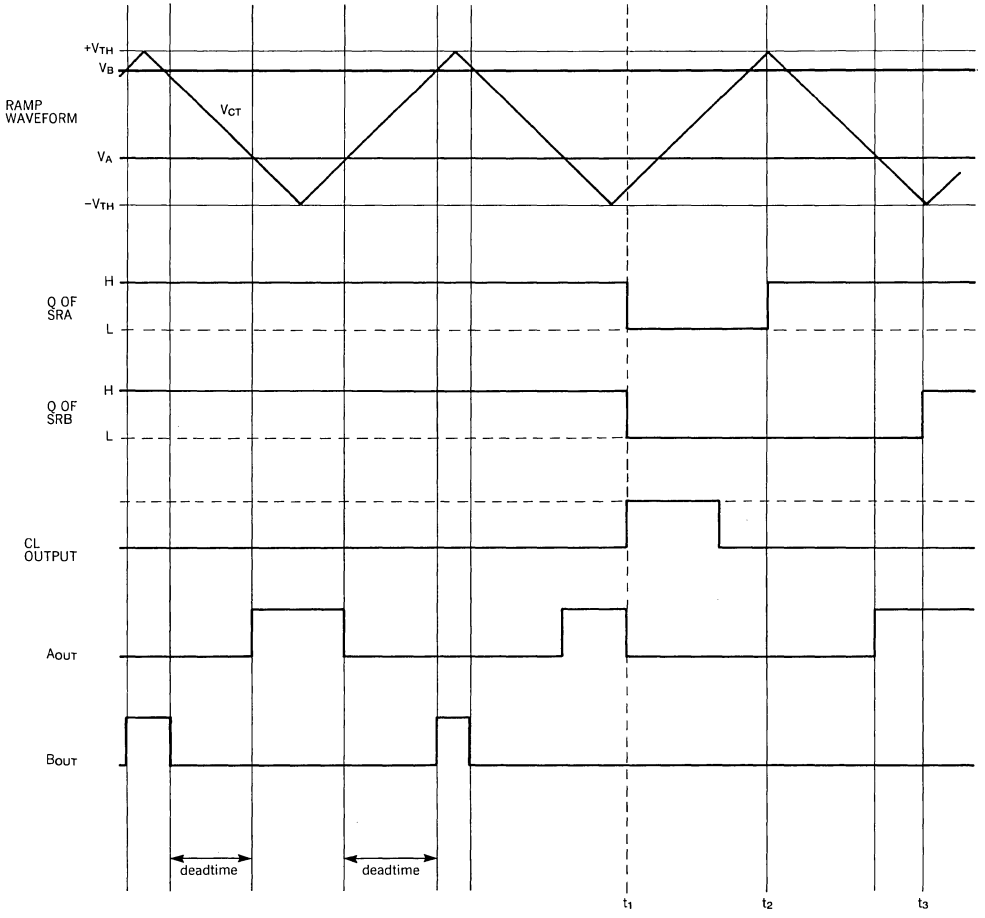

FIGURE 4. TIMING DIAGRAM SHOWING THE GENERATION OF PWM PULSES AT A_{OUT} AND B_{OUT}. BEFORE TIME t_1, THE Q OUTPUTS OF SRA AND SRB ARE BOTH HIGH AND THE OUTPUT PULSES ARE CONTROLLED BY THE RAMP INTERSECTIONS WITH V_A AND V_B. AT TIME t_1, THE CURRENT LIMIT COMPARATOR HAS SENSED EXCESS CURRENT AND THE CL OUTPUT HAS GONE HIGH, RESETTING BOTH SRA AND SRB. THIS TERMINATES THE A_{OUT} PULSE THAT WAS ACTIVE AT THE TIME. A_{OUT} CAN RESUME ONLY AFTER SRA IS SET AT t_2; B_{OUT} CAN RESUME ONLY AFTER SRB IS SET AT t_3.

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Figure 5 shows the connections needed to get the ramp generator and the two comparators ready to go. There is no great difficulty in calculating values for the various resistors, which are no more than two simple voltage dividers. Still, certain things should be considered before proceeding.

The input impedance R_{IN}, seen by the control voltage V_C will be

$$R_{IN} = \frac{R_3 + R_4}{2} \quad (1)$$

and this value may be specified or determined in advance. Also, it would be economical to have a minimum number of different values of resistors. If we make

$$R_1 = R_3 \quad (2)$$

we will have four resistors of equal value in the final circuit.

There is also the question of deciding on the separation V_G between the reference voltages $+V_R$ and $-V_R$. The voltage gain of the PWM amplifier will have one of the four characteristics depicted in Figure 6, depending on your choice of reference voltage separation: You can get a linear response by making $V_G = 0$, as in Curve #1, or by making $V_B - V_A = 2V_{TH}$, as in Curve #3. In Curve #2, there is a change in slope due to the contribution, near zero, of both V_A and V_B to the output changes, which in some systems may be undesirable, but which may be of interest due to the fact that it results in zero losses at null.

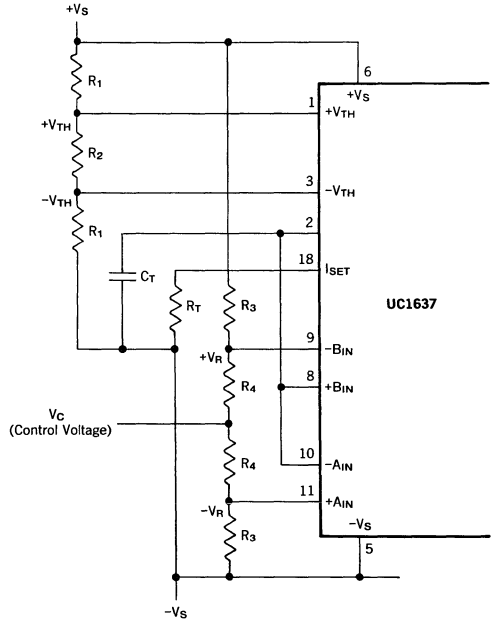

FIGURE 5. SETTING UP THE A AND B COMPARATOR INPUTS.

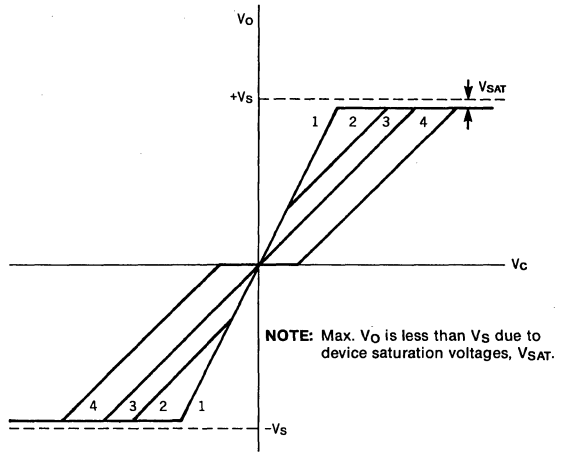

FIGURE 6. PWM VOLTAGE GAIN CHARACTERISTICS OBTAINABLE WITH VARIOUS VALUES OF REFERENCE VOLTAGE SEPARATION, OR GAP VOLTAGE 2 V_R.
1. LINEAR GAIN WITH $V_R = 0$ (a = 0).
2. NON-LINEAR GAIN WITH V_R GREATER THAN ZERO BUT LESS THAN V_{TH} (0 < a < 1).
3. LINEAR GAIN WITH $V_R = V_{TH}$ (a = 1).
4. NON-LINEAR GAIN WITH V_R GREATER THAN V_{TH} (a > 1).
NOTE: THE SLOPE OF LINE 1 IS TWICE THAT OF LINE 3.

At this point, this choice of PWM gain characteristic amounts only to the choice of the ratio between V_R and V_{TH}:

$$a = \frac{V_R}{V_{TH}} \quad (3)$$

The values of V_{TH} and V_R, as well as R_3 and R_4, depend on the following:

$\pm V_S$: power supply voltages
R_{IN}: desired control input resistance
$V_C$max: peak value or input voltage V_C. This is the input voltage at which the output reaches 100% duty cycle
a: ratio of V_R to V_{TH}

These values being known, the designer can proceed to calculate the following circuit values:

$$R_3 = \frac{2\,R_{IN}\,V_S\left(1 + \frac{1}{a}\right)}{V_C\text{max} + V_S\left(1 + \frac{1}{a}\right)} \quad (4)$$

$$R_4 = 2\,R_{IN} - R_3 \quad (5)$$

$$V_A = \frac{V_S R_4}{2 R_{IN}} \quad (6)$$

$$V_{TH} = \frac{V_R}{a} \quad (7)$$

$$R_2 = 2 R_3 \frac{V_{TH}}{V_S - V_{TH}} \quad (8)$$

and, from Eq. (2), $R_1 = R_3$.

Having chosen a frequency f_T for the PWM timing circuit, you can now calculate C_T and R_T. A suitable starting value for the charging current I_S is 0.5mA which gives

$$R_T = \frac{V_S + V_{TH}}{.0005} \quad (9)$$

$$C_T = \frac{.0005}{4 f_T V_{TH}} \quad (10)$$

You will probably need to make an adjustment here, so as to get a standard value for capacitor C_T, and it is best to keep I_S in the range from 0.3mA to 0.5mA when you do this.

It may be desirable, or even necessary in some conditions, to bypass the $+V_{TH}$ and $-V_{TH}$ inputs to ground, and for this, ceramic capacitors of 0.1μf should be adequate. Remember also that terminal 14, the shut-down line, must be held "low" (at least 2.5V below the positive rail) in order to enable the drive. With an external switch to ground, or to $-V_S$, and a pull-up resistor to $+V_S$, this line can be used to enable (low), and disable (high), the output. Both A_{OUT} and B_{OUT} will be low when the shut-down line is high.

The next step is to connect the UC1637 to a suitable power amplifier, and the amplifier to the motor. The UC1637 has provisions for current limiting, as discussed earlier, and you must make arrangements to develop a voltage proportional to motor current at the driver side. This can be done by adding to an H-bridge a low value resistor in series with rail connections. The current limit comparator has a common mode range that reaches all the way down to the negative rail (on the positive side the limit is 3V below the positive rail). A resistor R_S is then added at the bottom of the bridge, and its value is selected so as to give a voltage drop to 200mV when the desired limit current flows.

$$R_S = \frac{.2}{I_{MAX}} \text{ (ohms)} \quad (11)$$

where I_{MAX} is the maximum desired motor current in amperes. In a breadboard, a twisted pair of wires should be used to make the connection from this resistor to pins 12 and 13, and an RC filter should be added, as shown in Figure 7.

On a PC board, it is a good idea to keep R_S close to the UC1637 to minimize the length of the connecting traces. The RC filter should still be used.

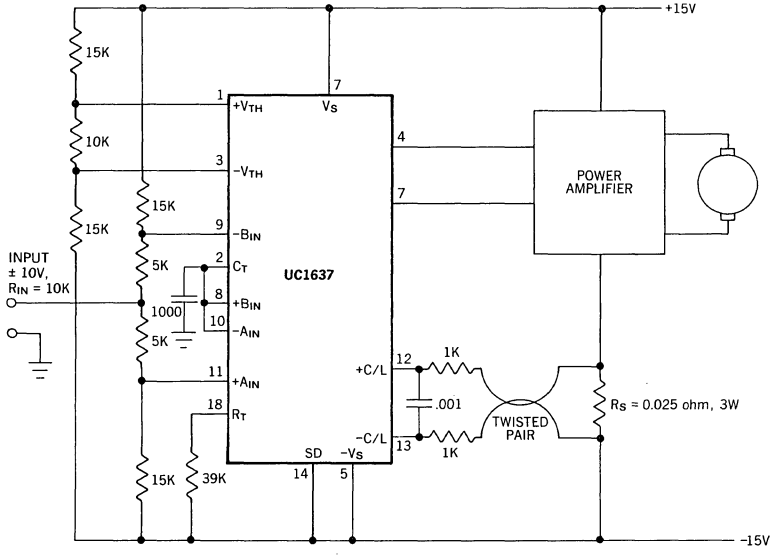

FIGURE 7. CIRCUIT DIAGRAM OF PWM VOLTAGE AMPLIFIER WITH GAIN OF 3.

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AN EXAMPLE

We are ready now to design a current limited, PWM voltage amplifier to drive a small DC servomotor. Here are the requirements:

Supply voltages: ±15V
Input: ±10V max.; 10K input res.
PWM frequency: 30KHz
Motor current limited at 8A
Minimum power losses at idle

We have:
$V_S = 15V$
$V_C max = 10V$
$R_{IN} = 10^4$ ohm
$f_T = 3 \times 10^4$ Hz
and $I_{MAX} = 8A$

and also, from the last requirement, a = 1.

FROM EQUATIONS

(4) $$R_3 = \frac{2 \times 10^4 \times 15 \times 2}{10 + 15 \times 2} = 15K$$

(5) $$R_4 = 2 \times 10^4 - 15 \times 10^3 = 5K$$

(6) $$V_R = \frac{15 \times 5 \times 10^3}{2 \times 10^4} = 3.75V$$

(7) $$V_{TH} = 3.75V$$

(8) $$R_2 = (2 \times 15 \times 10^3) \times \frac{3.75}{15 - 3.75} = 10K$$

(9) $$R_T = \frac{15 + 3.75}{.0005} = 37.5K$$

and of course, $R_1 = R_3 = 15K$.

(10) $$C_T = \frac{.0005}{4 \times 30 \times 10^3 \times 3.75} = 1.11 \times 10^{-9} fd$$

If we settle for R_T = 39K, I_S becomes slightly less than 0.5mA and if we then pick C_T = 1000pf, the nominal frequency becomes 32KHz.

To limit the motor current at 8A, we need, from Eq. 11,

$$R_S = \frac{.2}{8} = 0.025 \text{ ohm}$$

The peak power in the resistor will be

$P_S = 8^2 \times .025 = 1.6$ watts.

Incidentally, the voltage gain of the amplifier can be determined from the fact that a 10V change at the input results in a 30V change at the output; therefore, the gain from input to motor terminals is 3. The above circuit is shown in Figure 7.

THE POWER AMPLIFIER

Where space is tight and motor current is less than five amperes, the Unitrode PIC900 offers a perfect solution to your power bridge design. This device comes in a DIL-18 package, requires only 5mA of input drive current, and is rated at 5A absolute maximum output current. It contains all you need for the output H-bridge — including the circulating diodes — and with only a few added parts, you are ready to go. A circuit diagram showing a velocity feedback loop using one UC1637 and one PIC900 appears in the UC1637 data sheet.

For higher currents, you will have to design your own amplifier, and for the purposes of this application note, a sample design is shown in Figure 8. Referring to that circuit, note that with $+V_S$ and $-V_S$ applied, if the inputs are left open, the power MOSFETs are all "off". If Drive A, for example, is driven to within 3.6V of either power rail, then the corresponding output is switched to that rail. Note that since the PNP and NPN junction transistors are by nature faster switching "on" than "off", while the MOSFETs are much faster than the junction transistors driving them, this connection provides a simple guarantee against cross-conduction. Also working toward this goal is the fact that the junction transistor can discharge the MOSFET's input capacitance faster than the 1K, 1W resistor can charge it. The arrangement shown in Figure 8 results in a transition time of about 1.5μS during which both MOSFETs in a given leg are off. This amount of time is a very small portion of the 33μS period toward which we are designing our example.

The power MOSFET transistors, in TO-220 package, are rated at 60V and 12A. The channel "on" resistance is quite low, 0.25 ohms at 8A, for the UFN533, resulting in low thermal losses. You can easily find other devices with even lower R_{DS} values, if needed, but as always, the price you pay is that you must pay the price.

Finally, a word about circulating diodes — conspicuous in Figure 8 by their absence. All power MOSFETs have an intrinsic rectifier, or body diode, a junction rectifier whose current rating is the same as that of the transistor. With the drive format provided by the UC1637, the two bottom MOSFETs (N-channel) are "on" during the time when motor current circulates, and as a result, the reversed diode carries only a small portion of the current; most of it flows from source to drain through the channel. In fact, the diode fully conducts only during the 1.5μS when both devices in one bridge leg are off. You can add fast recovery diodes in shunt with the MOSFETs if you find that they are essential. The intrinsic MOSFET diode is not particularly fast, and as your output current requirements increase, the need for fast external diodes will become more and more apparent.

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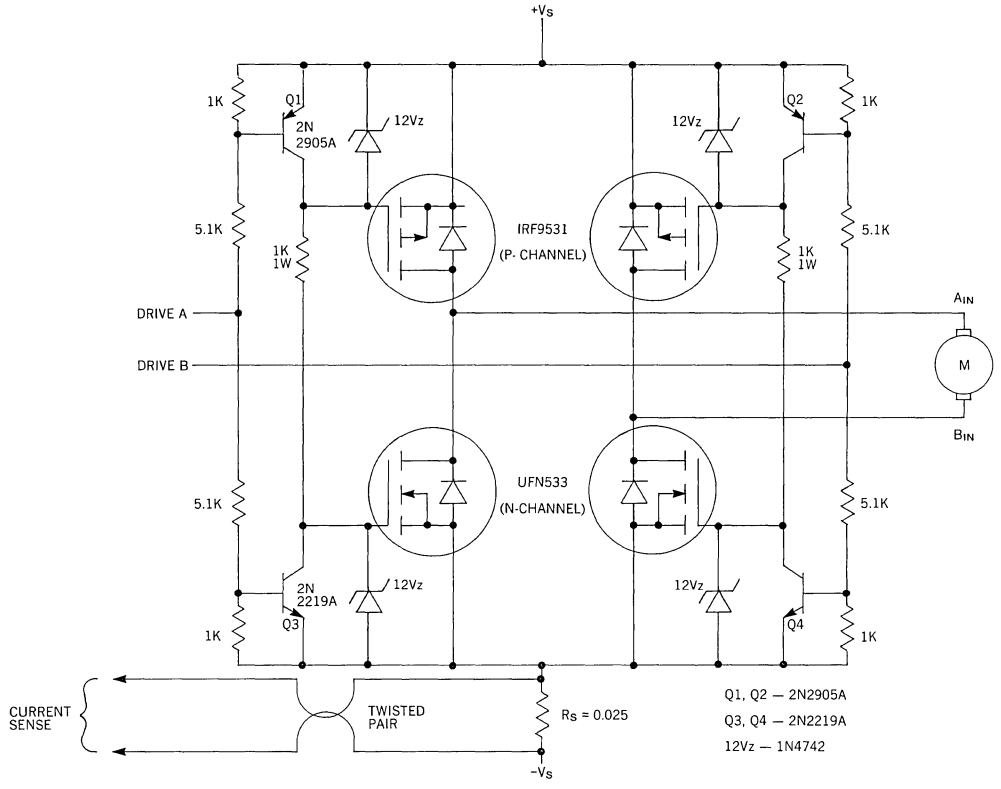

FIGURE 8. THIS 8A POWER AMPLIFIER IS SUITABLE FOR 30KHz OPERATION.

THE SERVOMOTOR

It is convenient to represent the DC servomotor by a simple equivalent circuit, and one such circuit is shown in Figure 9. Note that by expressing the moment of inertia J and the motor constant K in metric units (Nm sec^2 and Nm/A respectively), we avoid the need to include a multiplying constant in the expressions for C_M and e_o. Also, the motor constant K, in metric units, defines both the voltage constant in volt-sec/rad, and the torque constant in Nm/A, as one and the same number.

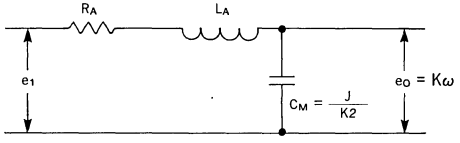

FIGURE 9. EQUIVALENT CIRCUIT OF MOTOR, WHERE J IS THE TOTAL MOMENT OF INERTIA OF ROTOR PLUS LOAD.

R_A = armature resistance; ohms.
L_A = armature inductance; henrys.
C_M = equivalent capacitance; farads.
J = total moment of inertia; Nm sec^2.
K = motor constant; volt sec/rad, or Nm/A.
ω = rotor angular velocity; rad/sec.

TO CONVERT FROM	TO	MULTIPLY BY
oz in sec^2	Nm sec^2	7.06×10^{-3}
volts/KRPM	volt sec/rad	9.55×10^{-3}

The ratio J/K^2 has the dimensions of capacitance, with a value runnng to several thousand microfarads. The voltage across this capacitor is equal to $K\omega$ where ω is the angular velocity of the rotor in rad/sec. Consequently, this voltage is the analog of shaft velocity.

Our equivalent circuit, then, is a simple series connection of R_A, the armature resistance; L_A, the armature inductance; and C_M, the equivalent capacitance, equal to J/K^2. It should come as no surprise that such a circuit will have a natural resonant frequency ω_N, and a resonant Q as well. This is indeed the case, and we have for its transfer function,

$$\frac{e_o(s)}{e_{i(s)}} = \frac{1}{(s/\omega_N)^2 + s/Q\omega_N + 1} \quad (12)$$

where $\omega_N = \sqrt{\frac{K}{L_A J}}$ (13)

and $Q = \frac{K}{R_A}\sqrt{\frac{L_A}{J}}$ (14)

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We can now use these sample results in our sample design. Here are some of the data given by a motor manufacturer:

EG & G TORQUE SYSTEMS
MODEL NO. MT-2605-102CE
(motor - tach assembly)

MOTOR: K_T = 4.7 oz in/amp
K_V = 3.5V/KRPM
R_A = 0.7 ohms
J_M = 0.0018 oz in sec^2
τ_M = 8.6 ms (mech. time const.)
τ_e = 1.6 ms (el. time const.)
TACH: J_T = 0.001 oz in sec^2
K_V = 3V/KRPM

The several motors in this series and size have the same electrical time constant τ_E, and since we know R_A,

$L_A = \tau_E R_A = 0.016 \times 0.7$
L_A = 1.12 mH

The total moment of inertia is

$J = J_M + J_T = 0.0018 + 0.001$
J = 0.0028 oz in sec^2

In metric units,

$$J = \frac{0.0028}{141.612} \text{ (Nm sec}^2\text{)}$$

Putting K_T in metric units,

$$K = \frac{4.7}{141.612} \text{ (Nm/amp)}$$

The equivalent capacitance is

$$C_M = \frac{J}{K^2} = \frac{141.612 \times 0.0028}{(4.7)^2} = 18{,}000\mu f$$

For the equivalent circuit, then, the values are

R_A = 0.7 ohms
L_A = 1.12 mH
C_M = 18,000μf

The angular velocity will be proportional to the voltage e_o across C_M;

$$\omega = \frac{e_o}{K}$$

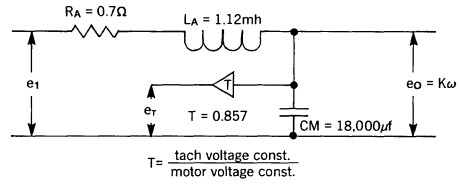


FIGURE 10. THE TACH VOLTAGE e_T IS PROPORTIONAL TO ω.

If the motor has a tachometer attached, we can include it in the equivalent circuit by deriving an equivalent tach voltage proportional to e_o. This is illustrated in Figure 10, where

$$T = \frac{\text{Tach. voltage constant}}{\text{Motor voltage constant}}$$

$$T = \frac{3\text{V/KRPM}}{3.5\text{V/KRPM}} = .857$$

From Eq. 13, ω_N = 222.7 rad/sec

From Eq. 14, Q = 0.356

(Note: Since $\zeta = \frac{1}{2Q}$, the damping factor here is 1.4)

From Eq. 12 and the above data, we can write the ratio of tach voltage to input as

$$\frac{e_T(s)}{e_i(s)} = \frac{.857}{\left(\frac{s}{222.7}\right)^2 + \frac{s}{79.3} + 1} \qquad (15)$$

THE VELOCITY LOOP

Our objective is to put together a feedback loop using our UC1637, H-bridge, and motor: the controlled variable is ω, the motor shaft's angular velocity. For high accuracy, we need a high loop gain, so that small velocity errors are magnified and corrected. The UC1637 internal ERROR amplifier is appropriate for this purpose, and will be used as a summing amplifier. But before proceeding, let us take a look at Figure 11, where a plot of the motor-tach transfer function (Eq. 17) is shown. The plot shows that as the frequency increases, the tach output decreases and the phase lag increases towards a maximum of 180°. This means that although we can introduce plenty of gain at very low frequencies, where the phase lag is low, the added gain must be reduced at the higher frequencies, where the 180° phase lag tends to make our loop a regenerative one. If we want the closed loop response to be "snappy", that is, if we want a bandwidth of several tens of hertz, then the loop gain must be

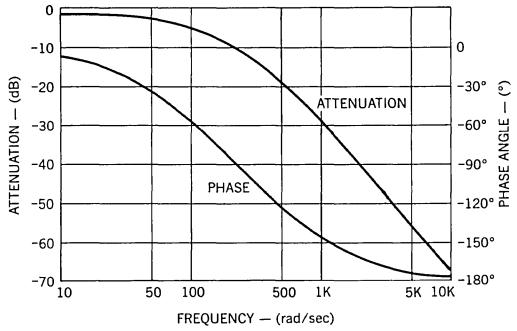
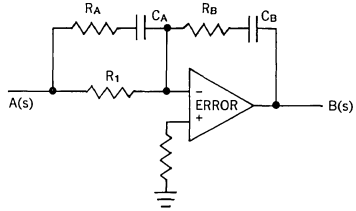


FIGURE 11. PLOT OF MAGNITUDE AND ANGLE OF EQ. 15, WHICH DESCRIBES PERFORMANCE OF OUR TEST MOTOR.

fairly high at all frequencies in the band; yet, for flat response and fast step response with no overshoot we must make certain that the overall phase shift is less than 180° at any frequency at which the gain is greater than unity.



$$\frac{A(s)}{B(s)} = \frac{(1 + sR_BC_B)\,[1 + s(R_1 + R_A)\,C_A]}{sR_1C_B\,(1 + sR_AC_A)}$$

FIGURE 12. ERROR AMPLIFIER WITH ITS FREQUENCY COMPENSATION NETWORK.
THE MAGNITUDE AND ARGUMENT OF THE TRANSFER FUNCTION CAN BE EASILY PLOTTED WITH THE AID OF A PROGRAMMABLE CALCULATOR.

The high gain ERROR amplifier of the UC1637, together with a few external components, is shown in Figure 12. Without R_A and C_A, the phase response of the circuit would go from −90° at low frequencies to 0° at high frequencies. This amount of phase correction is inadequate if we want a tight loop with good transient response. With R_A and C_A shunting R_1, it becomes possible to have a leading phase angle

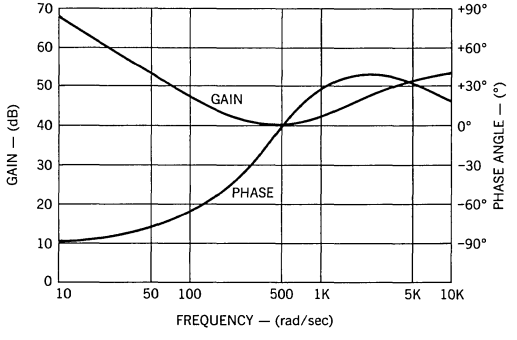


FIGURE 13. MAGNITUDE AND ANGLE OF COMPENSATION AMPLIFIER OF FIGURE 12.

somewhere at midrange, even though the high frequency asymptote is still at zero degrees (R_A and C_A introduce both a zero and a pole). The transfer function of the circuit shown in Figure 12 is plotted in Figure 13 for the following component values:

$R_1 = 9.1K$
$R_A = 1K$
$C_A = .22\mu f$
$R_B = 470K$
$C_B = .0047\mu f$

The break frequencies are:

$$\frac{1}{R_BC_B} = \frac{1}{(R_1 + R_A)\,C_A} = 450 \text{ rad/sec}$$

$$\frac{1}{R_1C_B} = 23{,}400 \text{ rad/sec}$$

$$\frac{1}{R_AC_A} = 4{,}500 \text{ rad/sec}$$

The plot shown in Figure 14 shows the result of cascading the compensation amplifier, PWM amplifier, and motor-tach. All gain contributions have been simply added together, and all phase contributions have also been added. The result, shown in Figure 14, shows the open loop frequency response of the complete velocity control system.

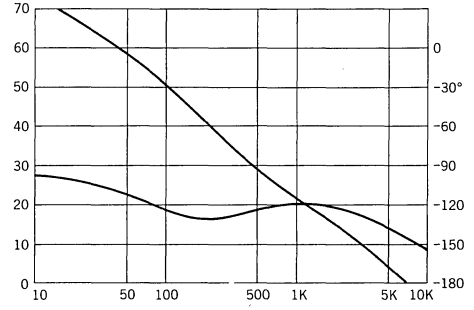


FIGURE 14. OVERALL OPEN-LOOP RESPONSE, INCLUDING +8dB DUE TO PWM AMPLIFIER GAIN AND MOTOR-TACH DC GAIN.

The inclusion of the ERROR amplifier with its compensation components has had the effect of introducing a large amount of gain at the lower frequencies, and also of reducing the phase lag at the higher frequencies. The loop gain is 0dB at about 7KHz, and the phase margin is about 40°.

Moreover, since the phase never exceeds 180°, we have the needed indication of *relative stability*, and can proceed to close the loop as shown in Figure 15 and make measurements. Note that a noise filter has neen added at the output of the tachometer. Such a filter is usually necessary, especially in PWM control loops of relatively wide bandwidth, because of the inevitable AC coupling between the motor signal and the tach output. In our filter, the 3dB cut-off point is at 21KHz, which is high enough not to affect the loop behavior.

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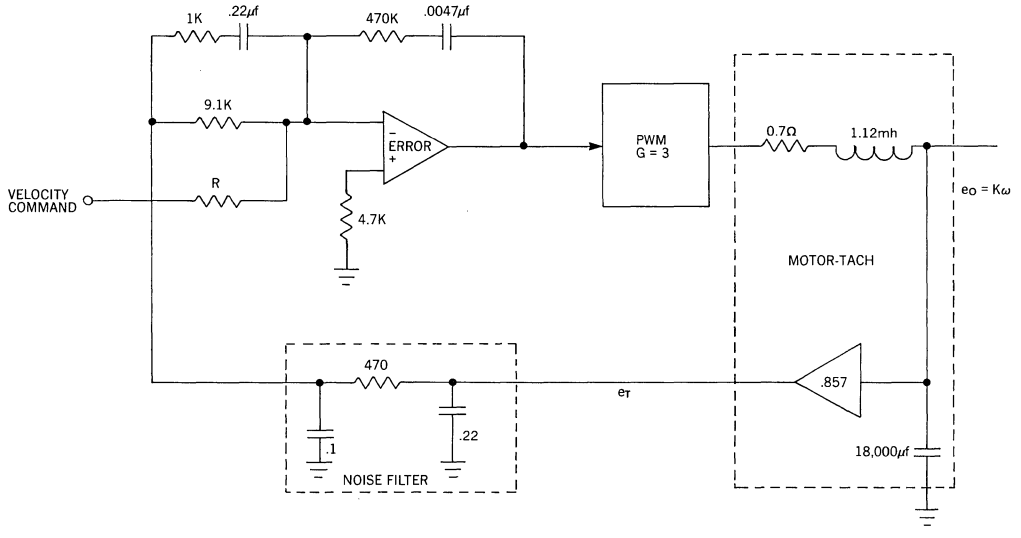
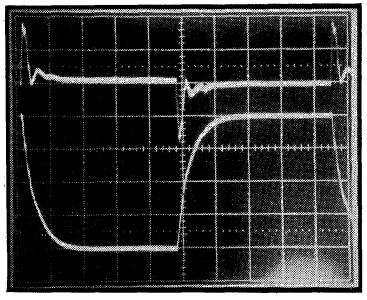


FIGURE 15. THE COMPLETE VELOCITY LOOP.

The oscilloscope trace shown in Figure 16 reveals that the step response of our loop is very well behaved. The motor shaft reaches full speed in less than 10mS, and there is no noticeable overshoot. The net velocity change in Figure 16 amounts to 133 RPM, and the current trace shows that the current does not quite reach the chosen limit of 8A. With larger input steps, the motor accelerates at constant 8A current, and the acceleration rate is approximately 100RPM per millisecond. The 3dB bandwidth of the loop measured about 80Hz.



Top trace: 5A/cm
Bottom trace: 100mV/cm
Horizontal: 5 msec/cm

FIGURE 16. STEP RESPONSE OF THE VELOCITY CONTROL LOOP OF FIGURE 15. THE UPPER TRACE SHOWS THE MOTOR CURRENT; THE LOWER TRACE SHOWS THE TACH OUTPUT VOLTAGE, I.E., MOTOR VELOCITY.

CONCLUSIONS

We have discussed in some detail the characteristics of Unitrode's UC1637 and have presented in detail a design approach which illustrates those points. The sample design was built and tested, with the measured results as presented above. These results show that excellent performance can be obtained with few components, and that the design technique is quite simple. Our velocity loop would perform well as an inner loop in a position control system, for example, although a different response might perhaps be desirable. However that may be, using the UC1637 a sizable portion to the job is completed beforehand.

See Figure 17.

ACKNOWLEDGMENTS

We are grateful to EG & G Torque Systems for providing the motor-tachometer used in the sample design.

The Electro-Craft Corporation generously supplied a copy of their engineering handbook on DC Motors, 5th Edition. This book is highly recommended.

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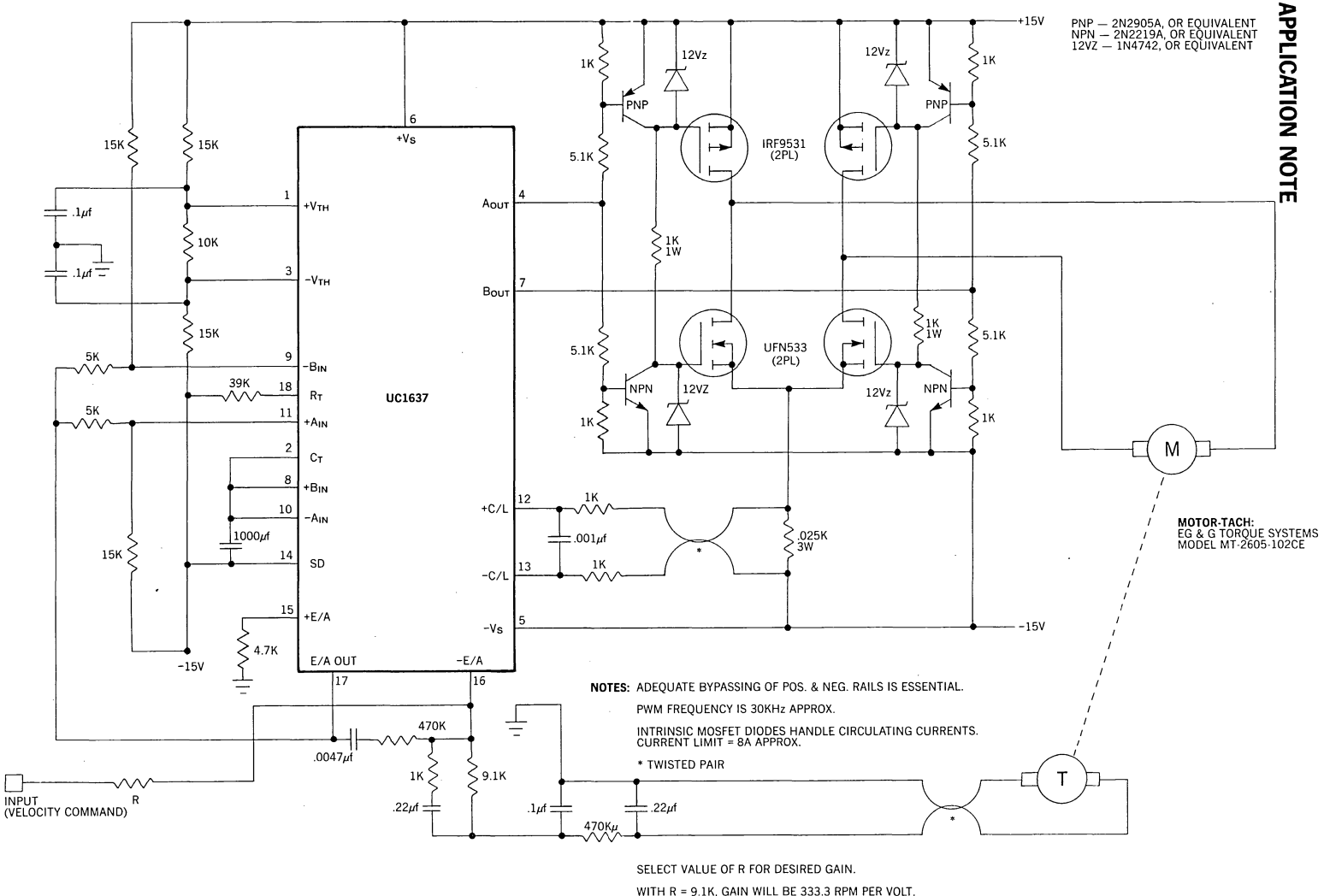

FIGURE 17. COMPLETE VELOCITY CONTROL LOOP OF SAMPLE DESIGN.

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USING BIPOLAR SYNCHRONOUS RECTIFIERS IMPROVES POWER SUPPLY EFFICIENCY

INTRODUCTION

In an off-line, switching regulated, low voltage power supply for applications such as high density CMOS logic, high speed ECL logic, etc., the power dissipated in the output rectifiers accounts for 20-30% of the total input power. These rectifier losses could be reduced significantly with a synchronous rectifier technique. The bipolar synchronous rectifier (BISYN™) provides a cost-effective approach compared to power MOSFET synchronous rectifiers. A low saturation resistance ($R_{CE(sat)}$) on the order of a few milliohms is accomplished by cancelling two forward biased junctions while in saturation. The BISYN is designed for low (<5.0V) voltage outputs and has the following features:

a) Low saturation voltage with high forced gain.

b) Ultra-fast switching times.

c) First and third quadrant switching capability.

The BISYN not only provides low forward voltage but also has a lower temperature co-efficient compared to power MOSFETs. Thus, it maintains the high efficiency of a switching regulated power supply. The storage time of a BISYN is on the order of 300-400 nano seconds. However, the circuit presented in this paper eliminates even this storage time limitation of the BISYN. The device characteristics are also briefly described.

The rectifier losses of the Schottky, power MOSFET, and BISYN are compared when used as output rectifiers. The half-wave and center-tapped full-wave BISYN output circuit for a switching regulated power supply is presented.

CONVERSION EFFICIENCY

The power conversion efficiency for a switching regulated power supply is a measure of heat generated and lost in the system. The temperature rise in the system affects the reliability. Note that the failure rate increases rapidly (log function) with an increase in operating junction temperature. Lower efficiency not only affects the reliability but also increases the operating cost of the system. Higher efficiency results in a compact and lighter power supply with simple thermal management requirements. In a typical line-operated switch-mode converter, as shown in Figure 1, the power lost in the output rectifiers accounts for 20-30% of the total input power. The circuit shown is a single ended forward converter. Energy from the input bulk capacitor C_{IN} is transferred to output filter inductor L and the load, through a power transformer T_1 and rectifier diode D_1, when transistor Q_1 is on.

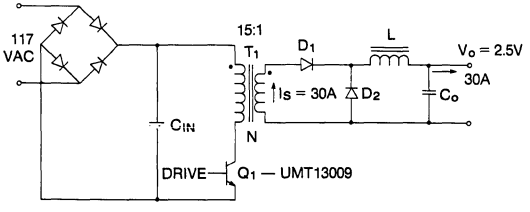

FIGURE 1. SINGLE ENDED FORWARD CONVERTER.

However, when transistor Q_1 is off, diode D_1 becomes reverse biased and the output load receives the energy from the output filter inductor L_1 through rectifier diode D_2. During this period the transformer core is reset with an equal and opposite volt-second product. Note that maximum conduction duty for transistor Q_1 is 50% and that one of the rectifiers (D_1 or D_2) is always conducting. From Figure 1, the fraction of input power lost in the rectifier can be calculated as follows:

$$\text{Output Power } P_O = V_o \times I_o = (2.5)(30) = 75W \quad (1)$$

$$\text{Transistor } Q_1 \text{ DC losses} = [V_{CE(sat)}] \times \left[\frac{I_o}{\text{Turns ratio}}\right] \text{ [Duty cycle]} \quad (2)$$

$$P_{Tdc} = (1.0V)\left(\frac{30A}{15}\right)(0.5) = 1.0W$$

Assuming transistor switching losses are equal to DC losses.

$$\text{Total transistor losses } P_T = 2 \times P_{Tdc} = 2W \quad (3)$$

Since one of the rectifiers always conducts; the total rectifier losses

$$P_D = I_o \quad V_F = (30A)(1V) = 30W \quad (4)$$

Therefore the fraction of input power lost in the output rectifiers;

$$P_{FR} = \frac{P_D}{P_o + P_D + P_T} = \frac{30}{75 + 30 + 2} = 0.28 \quad (5)$$

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The above calculation shows that rectifier losses are a significant portion of total power lost in a low voltage output supply. The reduction in efficiency due to these rectifier losses can be represented in terms of forward voltage drop by a simple equation:

$$\text{Loss of efficiency due to rectifier, \%} \approx \frac{V_F}{V_O + V_F} \times 100\% \approx \frac{1.0}{2.5 + 1.0} \times 100\% = 28.6\% \quad (6)$$

Note that the temperature dependent forward offset voltage V_F and and output voltage influences the efficiency of a switching power supply. The rectifier losses are minimized with the low forward voltage of a Schottky rectifier; but it still represents 20% of the total input power lost in these rectifiers when used in 2.5V supply. From the above equation, it is obvious that there is a nearly fixed fraction of input power lost in the output rectifiers regardless of load current. To improve the efficiency of the switching power supply, one must select an alternative such as synchronous rectification using either a power MOSFET or a BISYN.

The typical application of a synchronous rectifier using a power MOSFET is shown in Figure 2.

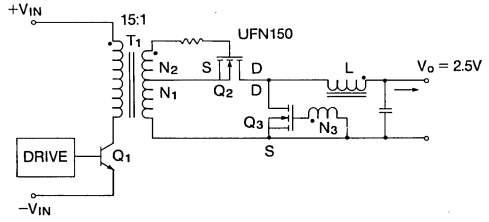

FIGURE 2. POWER MOSFET SYNCHRONOUS RECTIFIER.

During the on-time of primary transistor Q_1, power MOSFET Q_2 is turned on with a voltage generated across winding N_2, this allows secondary current to flow through the low source-to-drain resistance $R_{DS(on)}$. When primary transistor Q_1 is off, the power MOSFET Q_2 reverts to its blocking state. The MOSFET Q_3 turns on and facilitates a path for inductor current. Some inductor energy through winding N_3 is used to turn on power MOSFET Q_3. Since a power MOSFET is a majority carrier device, the turn-off delay is negligible. The switching losses are negligible due to its fast switching times. The fraction of power lost in this synchronous rectifier:

$$P_{FR} = (1 - \eta) = \frac{R_{DS(on)}\, I_o}{V_o = R_{DS(on)}\, I_o} \quad (7)$$

Unlike conventional rectifiers, the rectifier loss and consequently the efficiency of the power supply is a function of output current. The power supply efficiency can be increased by utiiizing a power MOSFET with a low on-resistance. Unfortunately, the power MOSFET synchronous rectifier is not a cost-efficient approach because:

1) Twice the silicon chip area is required when compared with a BISYN for the same forward voltage drop at room temperature.
2) $R_{DS(on)}$ of a power MOSFET increases three times faster with temperature than R_{CE} of a BISYN.

As such the power MOSFET requires three to four times as large a silicon chip for the same output current and performance as the BISYN.

BIPOLAR SYNCHRONOUS RECTIFIER

Unlike a bipolar transistor, BISYNs offer features such as low saturation resistance (8 milliohms for 4.5mm sq. chip) with light base drive (forced gain ≥ 25) and symmetrical voltage blocking capability for both positive and negative input voltages. The device is specifically designed for synchronous rectifier applications with low output voltages such as required for high density CMOS logic and high speed ECL.

Like a power MOSFET, the saturation resistance of the BISYN has a positive temperature co-efficient; however, it is three times smaller in magnitude. Thus it maintains high efficiency even at elevated temperatures. The switching times are optimized through a lightly doped, narrow base region. The storage time and fall time of the device is on the order of 300 and 80 nano seconds, respectively.

Unlike a power MOSFET, the BISYN has both positive and negative input voltage blocking capability. This opens the door for new applications, such as a synchronous PWM regulator in which the output voltage is regulated with a BISYN by controlling the conduction period in synchronization with the primary switching voltage.

The cross-sectioned area of a BISYN and waveforms of its electrical characteristics are shown in Figures 3 through 6.

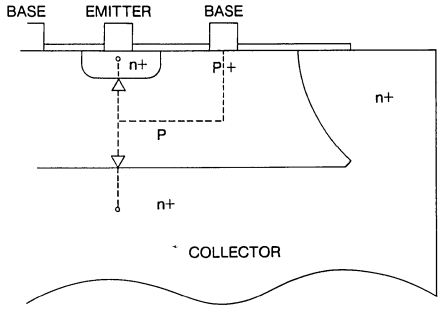

FIGURE 3. CROSS SECTION OF BISYN TRANSISTOR (TWO BIPOLAR JUNCTIONS TEND TO CANCEL EACH OTHER IN THE ON-STATE).

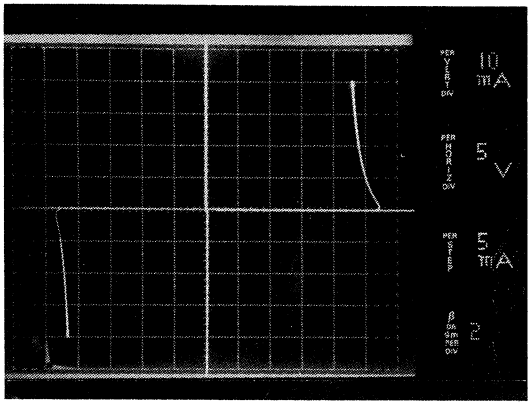

FIGURE 4. SYMMETRICAL REVERSE CHARACTERISTICS OF A BISYN RECTIFIER.

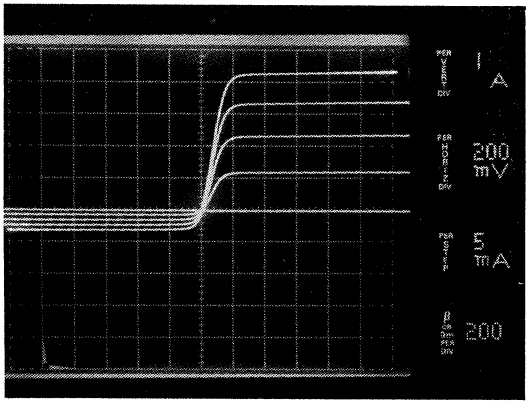

FIGURE 5. FIRST AND THIRD QUADRANT V_{CE} vs I_C CHARACTERISTICS OF A BISYN RECTIFER.

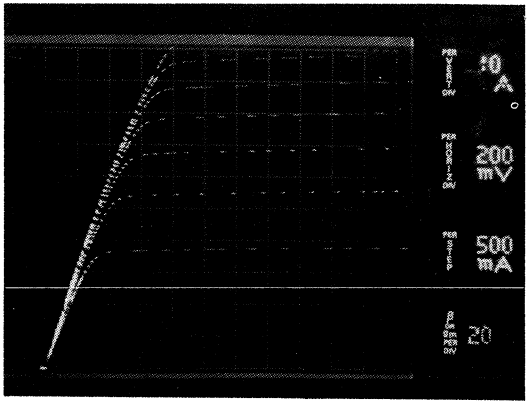

FIGURE 6. FIRST QUADRANT V_{CE} vs I_C CHARACTERISTICS.

A BISYN is a classical low voltage bipolar transistor. When both junctions are forward biased, the forward drops cancel each other and provide a low drop from collector to emitter. The saturation resistance of a BISYN is less than 2 milliohms while the rest of the 6 milliohms is contributed by metallization, wire bond and package resistances. This is the main reason for low composite temperature co-efficient of saturation resistance. Both positive and negative collector to emitter voltage blocking capability of the device, with base open, are shown in Figure 4. The first and third quadrant V_{CE} vs. I_C characteristics of the BISYN are displayed in Figure 5. It is obvious that the DC gain is as high as 200 in the first quadrant and 40 in the third quadrant; and is practically independent of collector to emitter voltage. First quadrant V_{CE} vs I_C characteristics up to 100A are presented in Figure 6. The saturation resistance $R_{CE(sat)}$, independent of collector current, is less than 8 milliohms, and the device has a high gain (30) even at 100 amperes.

PERFORMANCE COMPARISON AMONG SCHOTTKY, POWER MOSFET & BISYN

The power losses of a Schottky, a power MOSFET and a BISYN when used as a rectifier are compared in Figure 8.

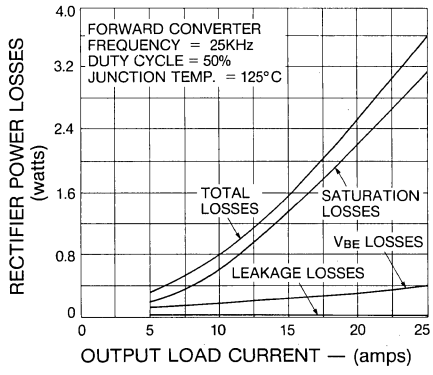

FIGURE 7. RECTIFIER POWER LOSSES.

The devices are *normalized* to the same size chip and reverse blocking voltage. For example, the commercially available power MOSFET IRFZ40 has 28 milliohms $R_{DS(on)}$ and B_{VDSS} = 40V ratings. The chip size is about the same as that of a BISYN, however, the normalized MOSFET with B_{VDSS} = 25V, not commercially available, will have only 18 milliohms $R_{DS(on)}$ and is used as a comparison with the BISYN. Similarly, the power Schottky rectifier is a 25V Schottky (not yet commercially available). Again the area of the silicon chips is normalized against the BISYN area.

Let us first define the losses in the BISYN.

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The power losses can be expressed by the equation:

$$P_{LBI} = [R_{CE(sat)}\, I_o^2]\,[D] + [V_{BE(on)}\, \frac{I_o}{B_F}]\,[D] + [I_R\, V_R]\,[1-D]$$

Where: I_o: output current
D: BISYN on Duty cycle
B_F: Forced gain to keep BISYN in saturation
I_R: Emitter to collector leakage current I_{ECX}
V_R: Emitter to collector voltage

From the above equation, it is obvious that the lower the saturation resistance and higher the forced beta, the lower the rectifier losses. The individual components of power loss at 125°C junction for the BISYN are presented in Figure 7. The worst case BISYN rectifier losses are realized at elevated temperatures. Unlike the Schottky rectifier, the power losses are a square function of the output load current instead of linear function.

The rectifier losses in a secondary output circuit are compared for a Schottky, a power MOSFET and a BISYN at a typical operating junction temperature (75°C) in a single ended forward converter, as shown in Figure 8. All the curves are normalized for devices with equal blocking voltage and silicon chip area.

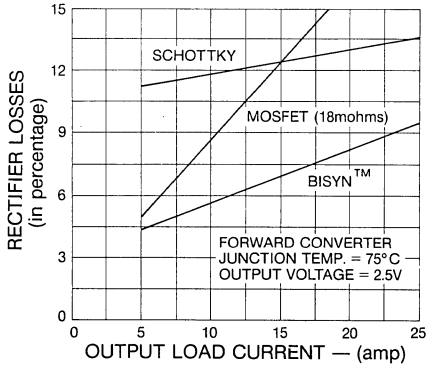

FIGURE 8. COMPARISON — TOTAL SECONDARY RECTIFIER LOSSES.

The BISYN rectifier uses a 4.5mm sq. silicon chip. For a 2.5V output supply, and output load current below 4A, the power MOSFET offers high efficiency because there are no $V_{BE(on)}$ losses. At elevated temperatures the output current crossover point favoring the BISYN will be even lower due to the higher temperature co-efficient of $R_{DS(on)}$ for the MOSFET. At high output currents use of a BISYN reduces the power losses to half of the losses of Schottky rectifiers.

For most low voltage applications the BISYN provides the most cost-effective and efficient approach for secondary rectification.

BISYN SYNCHRONOUS RECTIFIER APPLICATIONS

Two popular types of synchronous rectifiers are detailed in this section.

1) Single Ended Forward Converter; Half-Wave Synchronous Rectifier

In a single ended forward converter, the output voltage is developed by half wave rectification in the secondary circuit as previously shown in Figure 1. The rectifier diode D_2, which carries filter inductor current, must recover fast, when primary switch Q_1 is closed to prevent problems due to shorting the secondary through diode D_1. During the recovery period high peak current will be reflected back to the primary side. Besides EMI generation, the high peak current will increase the power dissipation in the switch Q_1 and can damage the power switch. Therefore, diode D_2 must have very short reverse recovery time. However, the BISYN utilized for diode D_2 had long recovery time (storage time), on the order of 300-400 nano seconds. This necessitated development of a unique circuit as shown in Figure 9, which eliminates the storage time limitation.

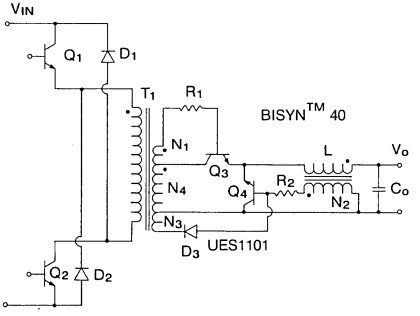

FIGURE 9. BIPOLAR SYNCHRONOUS RECTIFIER IN A TWO TRANSISTOR FORWARD CONVERTER.

The operation of the circuit is as follows. During the on-time of transistors Q_1 and Q_2, BISYN Q_3 is biased on and delivers output load current through filter inductor L. The polarity of voltage developed across winding N_2 is such that BISYN Q_4 remains in a blocking state. Diode D_3 is also biased off. When transistors Q_1 and Q_2 turn off, some of the energy stored in the magnetizing and leakage inductance enhances the recovery process of BISYN Q_3. The recovery time (300-400 nano seconds) of BISYN Q_3 extends the reset time of the core. However, in a typical design, half of the switching period is allocated for core reset time. Thus, the storage time has no significant effect on operation. The

BISYN Q_4 starts conducting filter inductor current as soon as the voltage across the secondary collapses. BISYN Q_4 receives base drive energy from the filter inductor L, through winding N_2. The diode D_3 still remains reverse biased.

When transistors Q_1 and Q_2 turn on again, the voltage across winding N_3 is clamped to approximately zero by diode D_3 and the forward biased collector to base junction of BISYN Q_4. This junction acts as a voltage source (≈0.7V) as long as BISYN Q_4 is conducting during the storage time. The turn-on of BISYN Q_3 is held off due to lack of base drive because winding N_3 is shorted, through diode D_3 and the collector-base junction of BISYN Q_4. Meanwhile, the current through the shorted turns (the rate of rise of which is limited by leakage inductance) is utilized to commutate BISYN Q_4 off rapidly. Diode D_3 is then reverse biased and BISYN Q_3 turns on through winding N_1.

The effect of the turn-off circuit (consisting of winding N_3 and diode D_3) on secondary current is demonstrated in Figure 9a. The upper waveform shows secondary current identical to the lower waveform except for high peak current.

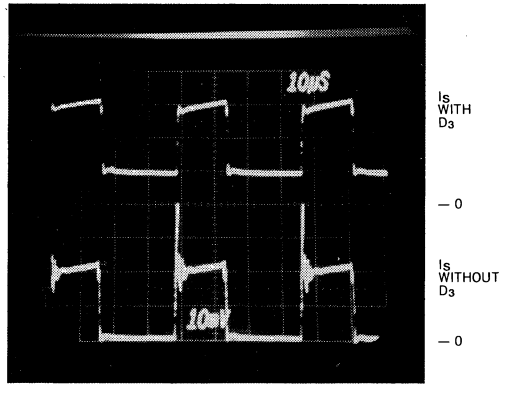

FIGURE 9a. SECONDARY CURRENT EFFECT OF DIODE D_3. VERTICAL SCALE: 5A/cm.

The oscillograms 9b and c demonstrate that there are practically no switching losses in a single ended forward converter.

2) Push-Pull Converter; Center-Tapped Full Wave Synchronous Rectifier

The center-tapped push-pull BISYN synchronous rectifier circuit is shown in Figure 10.

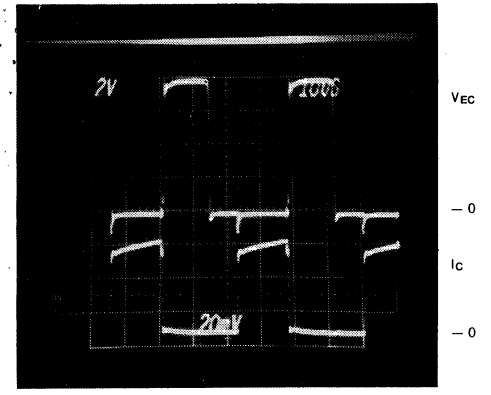

FIGURE 9b. TURN-ON WAVEFORMS. VERTICAL SCALE: 2V/cm.

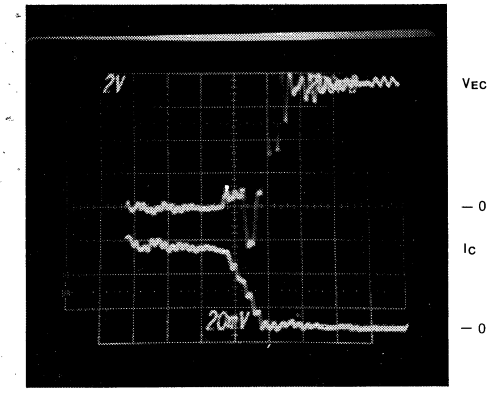

FIGURE 9c. TURN-OFF WAVEFORM. VERTICAL SCALE: 2V/cm.

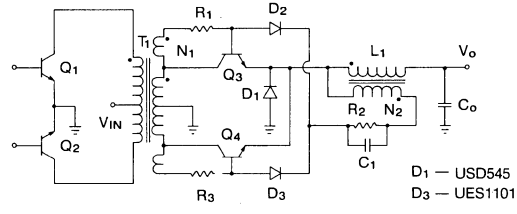

FIGURE 10a. BIPOLAR SYNCHRONOUS RECTIFIER IN A CENTER-TAP OUTPUT CONFIGURATION.

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During the on-time of primary transistor Q_1, BISYN Q_3 is on. At this time all other devices in the secondary circuit are in the off state. The energy from the primary side is being transferred to the secondary through the transformer and the BISYN Q_3. When primary transistor Q_1 turns off, current flow in the secondary winding ceases and the voltage across the secondary winding collapses. The catch diode D_1 provides the path for inductor current. The filter inductor energy causes current flow through diode D_2 and speeds up the turn-off process of BISYN Q_3. When Q_3 recovers, diode D_2 becomes reverse biased. The induced voltage, caused by stored magnetizing energy in the core, will turn on BISYN Q_4 and remains on until magnetizing current drops below diode D_3 current. When both transistors Q_1 and Q_2 are off, Q_3 remains off. The catch diode D_1 provides the current path for the filter inductor. Since BISYN Q_3 is off prior to turn-on of primary transistors Q_2, recovery time of the BISYN is of no consequence other than limiting maximum dead-band period of the circuit. The input voltage and current waveforms of the BISYN are shown in Figure 10a.

SYNCHRONOUS PWM REGULATORS

In a typical switching regulated power supply only one of the outputs is regulated through a closed loop; while other auxiliary outputs may provide rough regulation. When these outputs require tighter regulation, usually linear or switching regulators are utilized.

In a synchronous PWM regulator, the regulated auxiliary output is derived in one step through rectification and regulation of the secondary winding output voltage. A BISYN is the only device which can perform this function because of its unique third quadrant characteristics. Also, its low saturation resistance maintains high efficiency. The output voltage is regulated by gating the input pulsating DC voltage (from secondary winding) to the LC filter, in synchronism with the primary switching cycle. The detailed schematic of the regulator is shown in Figure 11.

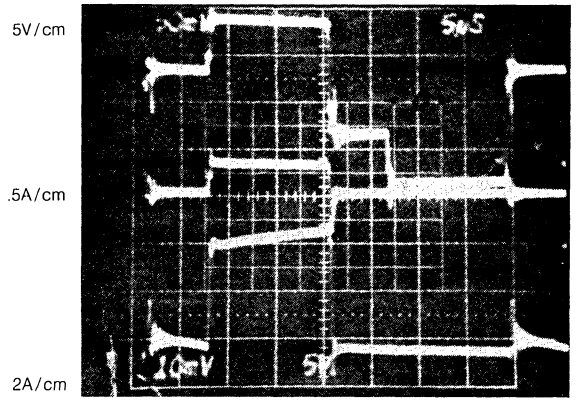

FIGURE 10b. WAVEFORMS. CENTER-TAP RECTIFIERS.

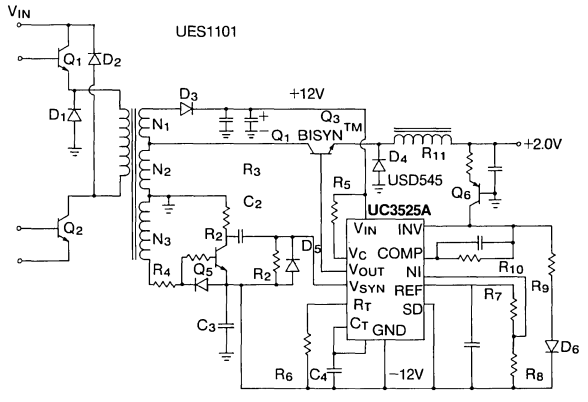

FIGURE 11. BISYN SYNCHRONOUS PWM VOLTAGE REGULATOR.

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Note that there is no standard commercially available PWM circuit which can perform these functions without some additional circuitry. The biasing requirements of the BISYN Q_3 necessitate the use of a positive and negative supply voltage for the PWM control chip. A commonly required ±12V output voltage can serve as a bias supply for the PWM circuit. However, in this circuit the PWM supply voltage is developed directly from the secondary winding as shown in the previous figure.

The BISYN is controlled by one of the totem-pole outputs of the control chip 3525A. The drive current (200mA) is limited by resistor R_5 during on-time. However, during initial turn-on, it receives a large peak value of bias drive current because the emitter of BISYN Q_3 is maintained at a negative 0.7V potential by catch diode D_3 which carries the filter inductor current. The turn-on waveform shown in Figure 12a demonstrates that turn-on drive current is three times higher than steady state base drive current.

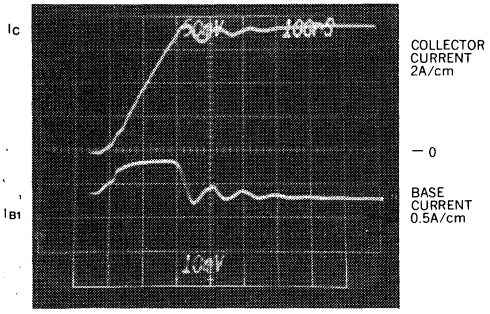

FIGURE 12a. RISE TIME.

The totem-pole output of the control chip also provides high negative base drive current (Figure 12b) during turn-off times, and also maintains proper biasing voltage to the base of the BISYN Q_3 during off-time.

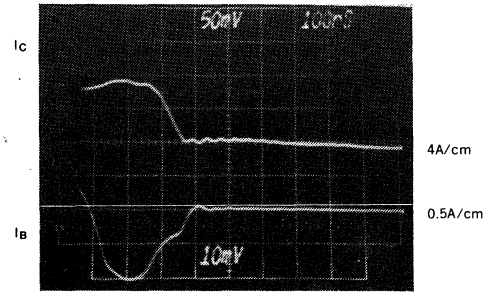

FIGURE 12b. FALL TIME.

A level shifter is required to feed back the output voltage sample because the control chip ground reference is different from the output voltage. The circuit consists of transistor Q_6, diode D_6 and resistors R_9 and R_{11}. A diode D_6 temperature compensates for the V_{BE} of transistor Q_6. The transistor Q_6 in conjunction with resistor R_{11} converts the output voltage into an output voltage dependent current source. The output voltage, referenced to the negative supply rail, is developed across resistor R_9 and diode D_6.

The sync pulses, referenced to the negative supply voltage, are developed with transistors Q_5, diode D_5 and the associated R_C circuit. The resistor R_2 and capacitor C_2 function as a differentiator circuit, while D_5 clamps the negative voltage excursion to prevent a malfunction of the control chip. The free running frequency is set about two times higher than the primary transistors switching frequency by capacitor C_4 and resistor R_4.

SUMMARY

In addition to synchronous rectifier, the application of a BISYN is demonstrated for voltage regulation with improved transient response through a synchronous PWM regulation technique. This is possible due to its unique third quadrant characteristics, unlike power MOSFETs. Ultra fast switching times allow the switching regulator to be operated up to 250kHz.

The BISYN has extremely low (<8 milliohm) saturation resistance with a small size (4.5mm sq.) chip. Thus it provides an efficient and cost-effective approach for synchronous rectifiers and synchronous PWM regulators when compared to power MOSFETs and Schottky rectifiers. The output current capability can be extended by paralleling these devices, which is possible because of the positive temperature co-efficient.

ACKNOWLEDGEMENT

I want to thank Lloyd Dixon for his insight into problems that required solving using bipolar transistors in these applications and David Reilly for constructing and assisting in the evaluation of these circuits. And finally, to Fred Blatt for his contributions.

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IMPROVED CHARGING METHODS FOR LEAD-ACID BATTERIES USING THE UC3906

ABSTRACT

This paper describes the operation and application of the UC3906 Sealed Lead-Acid Battery Charger. This IC provides reductions in the cost and design effort of implementing optimal charge and hold cycles for lead-acid batteries. Described are the design and operation of several charging circuits using this IC. The charger designs use current and voltage sensing combined with sequenced current and voltage control to maximize battery capacity and life for various applications. The presented material provides insight into expected improvements in battery performance with respect to these specific charging methods. Also presented are uses of the many auxiliary functions included on this part. The unique combination of features on this control IC has made it practical to create charge and hold cycles that truly get the most out of a battery.

AN IC FOR CHARGING LEAD-ACID BATTERIES

Battery technology has come a long way in recent years. Driven by the reduction of size and power requirements of processing functions, batteries now are used to provide portability and failsafe protection to a new generation of electronic systems. Although a number of battery technologies have evolved, the lead-acid cell remains the workhorse of the industry due to its combination of prolonged standby and cycle life with a high energy storage capacity. The makers of uninterruptible power supplies, portable equipment, and any system that requires failsafe protection are taking advantage of the improvements in this technology to provide secondary power sources to their products, for example, the sealed cell, using a trapped or gelled electrolyte, has eliminated the positional sensitivity and greatly reduced the dehydration problem.

The charging methods used to replenish or maintain the charge on a lead-acid battery have a significant effect on the performance of the cells. Building an optimum charger, one that gets the most out of a battery, is not a trivial task. Making sure that a battery undergoes the proper charge and hold cycle requires precision sensing and control of both voltage and current, logic to sequence the charger through its cycle, and temperature corrections — added to the charger's control and sensing circuits — to allow proper charging at any temperature. In the past this has required a significant number of components, and a substantial design effort as well. The UC3906 Sealed Lead-

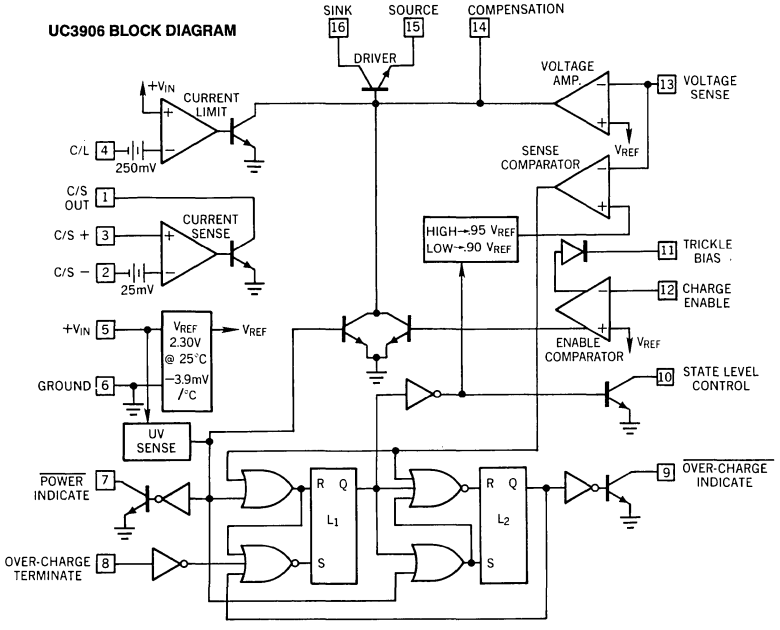

FIGURE 1. The UC3906 Sealed Lead-Acid Battery Charger combines precision voltage and current sensing with voltage and current control to realize optimum battery charge cycles. Internal charge state logic sequences the device through charging cycles. Voltage control and sensing is referenced to an internal voltage that specially tracks the temperature characteristics of lead-acid cells.

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Acid Battery Charger has all the control and sensing functions necessary to optimize cell capacity and life in a wide range of battery applications.

The block diagram for the UC3906 is shown in figure 1. Separate voltage loop and current limit amplifiers regulate the output voltage and current levels in the charger by controlling the onboard driver. The driver will supply 25mA of base drive to an external pass element. Voltage and current sense comparators are used to sense the battery condition and respond with logic inputs to the charge state logic. The charge enable comparator on this IC can be used to remotely disable the charger. The comparator's 25mA trickle bias output is active high when the driver is disabled. These features can be combined to implement a low current turn-on mode in a charger, preventing high current charging during abnormal conditions such as a shorted or reversed battery.

A very important feature of the UC3906 is its precision reference. The reference voltage is specially temperature compensated to track the temperature characteristics of lead-acid cells. The IC operates with very low supply current, only 1.7mA, minimizing on-chip dissipation and permitting the accurate sensing of the operating environmental temperature. In addition, the IC includes a supply under-voltage sensing circuit, used to initialize charging cycles at power on. This circuit also drives a logic output to indicate when input power is present. The UC3906 is specified for operation over the commercial temperature range of 0°C to 70°C. For operation over extended temperatures, −40°C to 70°C the UC2906 is available.

WHAT IS IMPORTANT IN A CHARGER?

Capacity and life are critical battery parameters that are strongly affected by charging methods. Capacity, C, refers to the number of ampere-hours that a charged battery is rated to supply at a given discharge rate. A battery's rated capacity is generally used as the unit for expressing charge and discharge current rates, i.e., a 2.5 amp-hour battery charging at 500mA is said to be charging at a C/5 rate. Battery life performance is measured in one of two ways; cycle life or stand-by life. Cycle life refers to the number of charge and discharge cycles that a battery can go through before its capacity is reduced to some threshold level. Standby life, or float life, is simply a measure of how long the battery can be maintained in a fully charged state and be able to provide proper service when called upon. The measure which actually indicates useful life expectancy in a given application will depend on the particulars of the application. In general, both aspects of battery life will be important.

During the charge cycle of a typical lead-acid cell, lead sulfate, $PbSO_4$, is converted to lead on the battery's negative plate and lead dioxide on the battery's positive plate. Once the majority of the lead sulfate has been converted, over-charge reactions begin. The typical result of over-charge is the generation of hydrogen and oxygen gas. In unsealed batteries this results in the immediate loss of water. In sealed cells, at moderate charge rates, the majority of the hydrogen and oxygen recombine before dehydration occurs. In either type of cell, prolonged charging rates significantly above C/500, will result in dehydration, accelerated grid corrosion, and reduced service life.

The onset of the over-charge reaction will depend on the rate of charge. At charge rates of >C/5, less than 80% of the cell's previously discharged capacity will be returned as the over-charge reaction begins. For over-charge to coincide with 100% return of capacity, charge rates must typically be reduced to less than C/100. Also, to accept higher rates the battery voltage must be allowed to increase as over-charge is approached. Figure 2 illustrates this phenomenon, showing cell voltage vs. percent return of previously discharged capacity for a variety of charge rates. The over-charge reaction begins at the point where the cell voltage rises sharply, and becomes excessive when the curves level out and start down again.

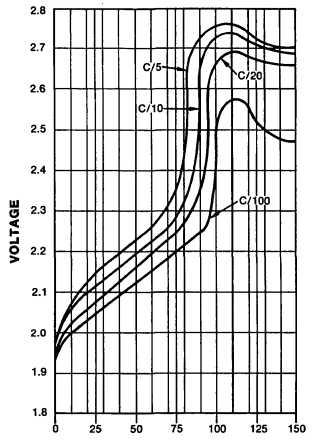

FIGURE 2. Depending on the charge rate, over-charge reactions begin, (indicated by the sharp rise in battery voltage), well below 100% return of capacity. (Reprinted with the permission of Gates Energy Products, Inc.)

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Once a battery is fully charged, the best way to maintain the charge is to apply a constant voltage to the battery. This burdens the charging circuit with supplying the correct float charge level; large enough to compensate for self-discharge, and not too large to result in battery degradation from excessive overcharging. With the proper float charge, sealed lead-acid batteries are expected to give standby service for 6 to 10 years. Errors of just five percent in a float charger's characteristics can halve this expected life.

To compound the above concerns, the voltage characteristics of a lead-acid cell have a pronounced negative temperature dependence, approximately -4.0mV/°C per 2V cell. In other words, a charger that works perfectly at 25°C may not maintain or provide a full charge at 0°C and conversely may drastically over-charge a battery at +50°C. To function properly at temperature extremes a charger must have some form of compensation to track the battery temperature coefficient.

To provide reasonable re-charge times with a full 100% return of capacity, a charge cycle must adapt to the state of charge and the temperature of the battery. In sealed, or recombinate, cells, following a high current charge to return the bulk of the expended capacity, a controlled over-charge should take place. For unsealed cells the over-charge reaction must be minimized. After the over-charge, or at the onset of over-charge, the charger should convert to a precise float condition.

A DUAL LEVEL FLOAT CHARGER

A state diagram for a sealed lead-acid battery charger that would meet the above requirements is shown in figure 3.

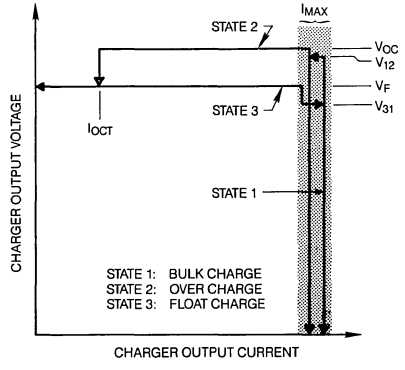


FIGURE 3. The dual level float charger has three charge states. A constant current bulk charge returns 70-90% of capacity to the battery with the remaining capacity returned during an elevated (constant) voltage over-charge. The float charge state maintains a precision voltage across the battery to optimize stand-by life.

This charger, called a dual level float charger, has three states, a high current bulk charge state, an over-charge state, and a float state. A charge cycle begins with the charger in the bulk charge state. In this state the charger acts like a current source providing a constant charge rate at I_{MAX}. The charger monitors the battery voltage and as it reaches a transition threshold, V_{12}, the charger begins its over-charge cycle. During the over-charge, the charger regulates the battery at an elevated voltage, V_{OC}, until the charge rate drops to a specified transition current, I_{OCT}. When the current tapers to I_{OCT}, with the battery at the elevated level, the capacity of the cell should be at nearly 100%. At this point the charger turns into a voltage regulator with a precisely defined output voltage, V_F. The output voltage of the charger in this third state sets the float level for the battery.

With the UC3906, this charge and hold cycle can be implemented with a minimum of external parts and design effort. A complete charger is shown in figure 4. Also shown are the design equations to be used to calculate the element values for a specific application. All of the programming of the voltage and current levels of the charger are determined by the appropriate selection the external resistors R_S, R_A, R_B, R_C.

Operation of this charger is best understood by tracing a charge cycle. The bulk charge state, the beginning, is initiated by either of two conditions. One is the cycling on of the input supply to the charger; the other is a low voltage condition on the battery that occurs while the charger is in the float state. The under-voltage sensing circuit on the UC3906 measures the input supply to the IC. When the input supply drops below about 4.5V the sensing circuit forces the two state logic latches (see figure 1) into the bulk charge condition (L1 reset and L2 set). This circuit also disables the driver output during the under-voltage condition. To enter the bulk charge state while power is on, the charger must first be in the float state (both latches set). The input to the charge state logic coming from the voltage sense comparator reports on the battery voltage. If the battery voltage goes low this input will reset L1 and the bulk charge state will be initiated.

With L1 reset, the state level output is always active low. While this pin is low the divider resistor, R_B is shunted by resistor R_C, raising the regulating level of the voltage loop. If we assume that the battery is in need of charge, the voltage amplifier will be in its stops trying to turn on the driver to force the battery voltage up. In this condition the voltage amplifier output will be over-ridden by the current limit amplifier. The current limit amplifier will control the driver, regulating the output current to a constant level. During this

time the voltage at the internal, non-inverting, input to the voltage sense comparator is equal to 0.95 times the internal reference voltage. As the battery is charged its voltage will rise; when the scaled battery voltage at PIN 13, the inverting input to the sense comparator, reaches 0.95Vref the sense comparator output will go low. This will reset the second latch and the over-charge state will be entered. At this time the over-charge indicator output will go low. Other than this there is no externally observable change in the charger. Internally, the starting of the over-charge state arms the set input of the first latch — assuming no reset signal is present — so that when the over-charge terminate input goes high, the charger can enter the float state.

In the over-charge state, the charger will continue to supply the maximum current. As the battery voltage reaches the elevated regulating level, V_{OC}, the voltage amplifier will take command of the driver, regulating the output voltage at a constant level. The voltage at PIN 13 will now be equal to the internal reference voltage. The battery is completing its charge cycle and the charge acceptance will start to taper off.

As configured in figure 4, the current sense comparator continuously monitors the charge rate by sensing the voltage across R_S. The output of the comparator is connected to the over-charge terminate input. Whenever the charge current is less than I_{OCT}, ($25mV/R_S$), the open collector output of the comparator will be off. When this transition current is reached, as the charge rate tapers in the over-charge state, the off condition of the comparator output will allow an internal 10μA pull-up current at PIN 8 to pull that point high. A capacitor can be added from ground to this point to provide a delay to the over-charge-terminate function, preventing the charger from prematurely entering the float state if the charging current temporarily drops due to system noise or whatever. When the voltage at PIN 8 reaches its 1V threshold, latch L1 will be set, setting L2 as well, and the charger will be in the float state. At this point the state level output will be off, effectively eliminating R_C from the divider and lowering the regulating level of the voltage loop to V_F.

In the float state the charger will maintain V_F across the battery, supplying currents of zero to I_{MAX} as required. In addition, the setting of L1 switches the voltage sense comparator's reference level from 0.95 to 0.90 times the internal reference. If the battery is now discharged to a voltage level 10% below the float level, the sense comparator output will reset L1 and the charge cycle will begin anew.

The float voltage V_F, as well as V_{OC} and the transition voltages, are proportional to the internal reference on the UC3906. This reference has a temperature coefficient of

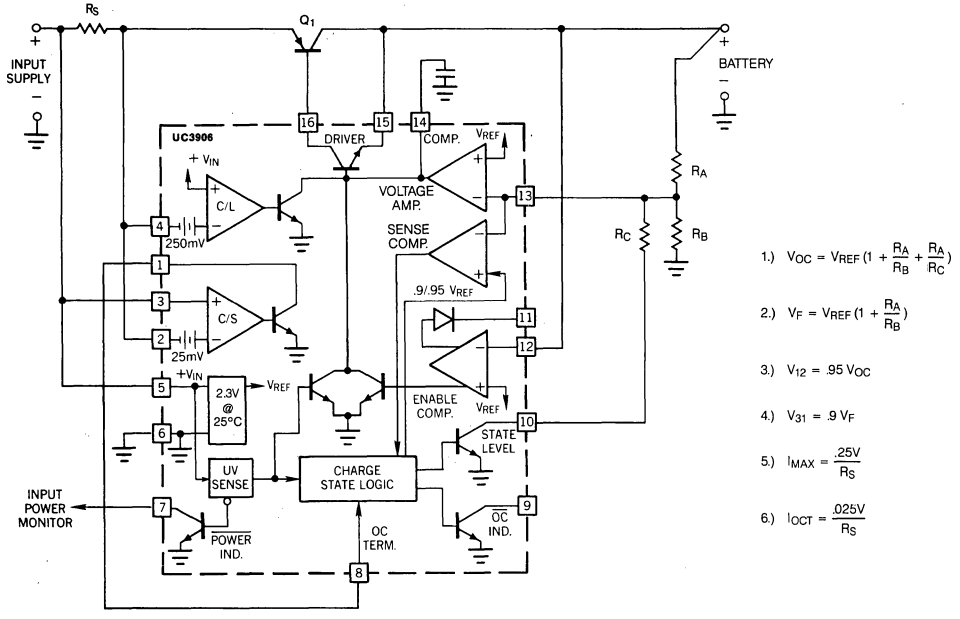


FIGURE 4. Using a few external parts and following simple design equations the UC3906 can be configured as a dual level float charger.

–3.9mV/°C. This temperature dependence matches the recommended compensation of most battery manufacturers. The importance of the control of the charger's voltage levels is reflected in the tight specification of the tolerance of the UC3906's reference and its change with temperature, as shown in figure 5.

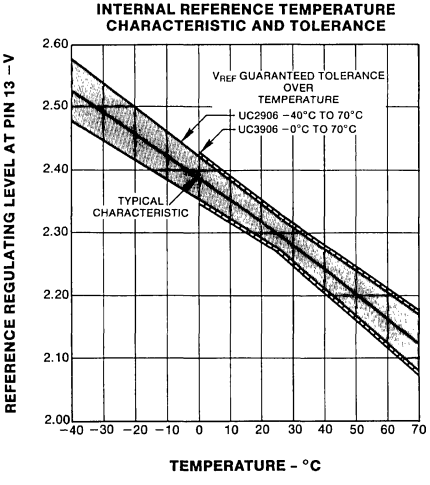


FIGURE 5. The specially temperature compensated reference on the UC3906 is tightly specified over 0 to 70°C, (–40 to 70°C for the UC2906), to allow proper charge and hold characteristics at all temperatures.

I_{MAX}, I_{OCT}, V_{OC}, and V_F can all be set independently. I_{MAX}, the bulk charge rate can usually be set as high as the available power source will allow, or the pass device can handle. Battery manufacturers recommend charge rates in the C/20 to C/3 range, although some claim rates up to and beyond 2C are OK if protection against excessive overcharging is included. I_{OCT}, the over-charge terminate threshold, should be chosen to correspond, as close as possible, to 100% recharge. The proper value will depend on the over-charge voltage (V_{OC}) used and on the cell's charge current tapering characteristics at V_{OC}.

I_{MAX} and I_{OCT} are determined by the offset voltages built into the current limit amplifier and current sense comparator respectively, and the resistor(s) used to sense current. The offsets have a fixed ratio of 250mV/25mV. If ratios other than ten are necessary separate current sensing resistors or a current sense network, must be used. The penalty one pays in doing this is increased input-to-output differential requirements on the charger during high current charging. Examples of this are shown in figure 6.

An alternative method for controlling the over-charge state is to use the over-charge indicate output, PIN 9, to initiate an external timer. At the onset of the over-charge cycle the over-charge indicate pin will go low. A timer triggered by this signal could then activate the over-charge terminate input, PIN 8, after a timed over-charge has taken place. This method is particularly attractive in systems with a centralized system controller where the controller can provide the timing function and automatically be aware of the state of charge of the battery.

The float, V_F, and over-charge, V_{OC}, voltages are set by the internal reference and the external resistor network, R_A, R_B, and R_C as shown in figure 4. For the dual level float charger the ranges at 25°C for V_F and V_{OC} are typically 2.3V-2.40V and 2.4V-2.7V, respectively. The float charge level will normally be specified very precisely by the battery manufacturer, little variation exists among most battery suppliers. The over-charge level, V_{OC}, is not as critical and will vary as a function of the charge rate used. The absolute value of the divider resistors can be made large, a divider current of 50μA will sacrifice less than 0.5% in accuracy due to input bias current offsets.

AUXILIARY CAPABILITIES OF THE CHARGER IC

Besides simply charging batteries, the UC3906 can be used to add many related auxiliary functions to the charger that would otherwise have to be added discretely. The enable comparator and its trickle bias output can be used in a number of different ways. The modification of the state diagram in figure 2 to establish a low current turn-on mode

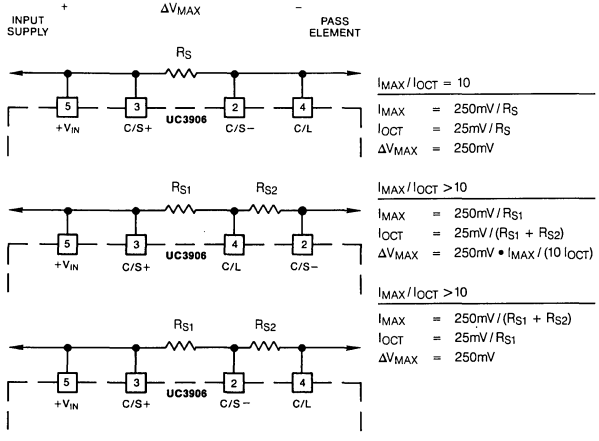


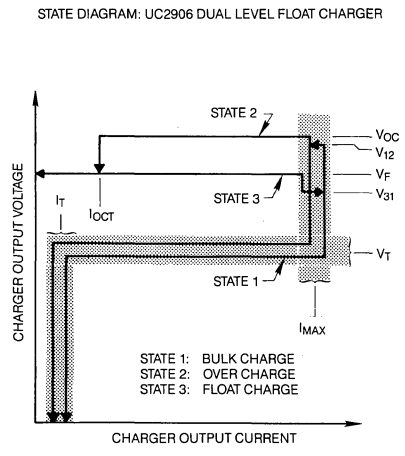
FIGURE 6. Although the ratio of input offset voltages on the current limit and current sense stages is fixed at 10, other ratios for I_{MAX}/I_{OCT} are easily obtained. Note that a penalty for ratios greater than 10 is increased voltage drop across the sensing network at I_{MAX}.

of the charger (see figure 7) is easily done. By reducing the output current of the charger when the battery voltage is below a programmable threshold, the charging system protects against: One, high current charging of a string with a shorted cell that could result in excessive outgassing from the remaining cells in the string. Two, dumping charge into a battery that has been hooked up backwards. Three, excessive power dissipation in the charger's pass element. As shown in figure 7, the enable comparator input taps off the battery sensing divider. When the battery voltage is below the resulting threshold, V_T, the driver on the UC3906 is disabled and the trickle bias output goes high. A resistor, R_T, connected to the battery from this output can then be used to set a trickle current, ($\leq$25mA) to the battery to help the charger discriminate between severely discharged cells and damaged, or improperly connected, cells.

In applications where the charger is integral to the system, i.e. always connected to the battery, and the load currents on the battery are very small, it may be necessary to absolutely minimize the load on the battery presented by the charger when input power is removed. There are two simple precautions that, when taken, will remove essentially all reverse current into the charging circuit. In figure 8 the diode in series with the pass element will prevent any reverse current through this path. The sense divider should still be referenced directly to the battery to maintain accurate control of voltage. To eliminate this discharge path, the divider in the figure is referenced to the open collector power indicate output, PIN 7, instead of ground. Connected in this manner the divider string will be in series with essentially an open when input power is removed. When power is present, the open collector device will be on, holding the divider string end at nearly ground. The saturation voltage of the open collector output is specified to be less than 50mV with a load current of 50μA.

Figure 9 illustrates the use of the enable comparator and its output to build over-discharge protection into a charger. Over-discharging a lead-acid cell, like over-charging, can severely shorten the service life of the cell. The circuit monitors the discharging of the battery and disconnects all load from the battery when its voltage reaches a specified cutoff point. The load will remain disconnected from the battery until input power is returned and the battery recharged.

This scheme uses a relay between the battery and its load that is controlled by Q1 and the presence of voltage across the load. When primary power is available Q1 is on via D5. The battery is charging, or charged, and the trickle bias output at PIN 11 is off. When input power is removed, C2 provides enough hold-up time at the load to let Q1 turn off, and the relay to close as current flows through R1. The battery is now providing power to the load and, through D1, power to the charger. The charger current draw will typically be less than 2mA. As the battery discharges, the UC3906 will continue to monitor its voltage. When the vol-



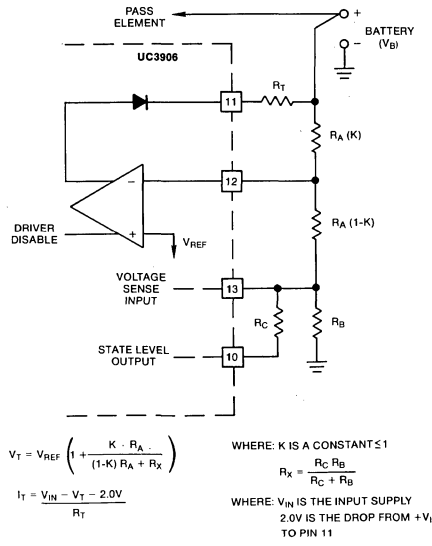


FIGURE 7. The charge enable comparator, with its trickle bias output, can be used to build protection into the charger. The current foldback at low battery voltages prevents high current charging of batteries with shorted cells, or improperly connected batteries, and also protects the pass element from excessive power dissipation.

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tage reaches the cut-off level, set by the divider network, R5-R8, the trickle bias output, PIN 11, will go high. Q1 will turn back on and the relay current will collapse opening its contacts. As the load voltage drops, capacitor C1 supplies power to the UC3906 to keep Q1 on. Once the input to the charger has collapsed the power indicate pin, as shown in figure 8, will open the divider string. The battery will remain open-circuited until input power is returned. At that time the battery will begin to recharge.

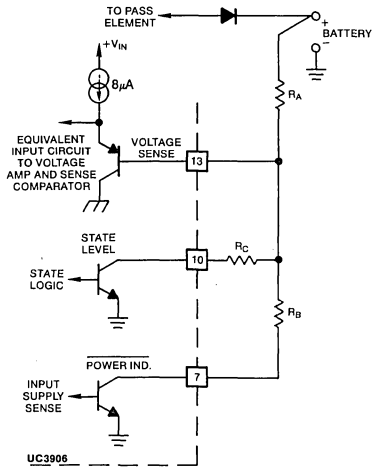


FIGURE 8. By using a diode in series with the pass element, and referencing the divider string to the power indicate pin, pin 7, reverse current into the charger, (when the charger is tied to the battery with no input power), can be eliminated.

CHARGING LARGE SERIES STRINGS OF LEAD-ACID CELLS

When large series strings of batteries are to be charged, a dual step current charger has certain advantages over the float charger of figures 3 and 4. A state diagram and circuit implementation of this type of charger is shown in figure 10. The voltage across a large series string is not as predictable as a common 3 or 6 cell string. In standby service varying self discharge rates can significantly alter the state of charge of individual cells in the string if a constant float voltage is used. The elevated voltage, low current holding state of the dual step current charger maintains full and equal charge on the cells. The holding, or trickle current, I_H, will typically be on the order of 0.005C to 0.0005C.

To give adequate and accurate recharge this charger has a bulk charge state with temperature compensated transition thresholds, V_{12}, and V_{21}. Instead of entering an elevated voltage over-charge, upon reaching V_{12} the charger switches to a constant current holding state. The holding current will maintain the battery voltage at a slightly elevated level but not high enough to cause significant overcharging. If the battery current increases, the charger will attempt to hold the battery at the V_F level as shown in the state diagram. This may happen if the battery temperature increases significantly, increasing the self-discharge rate beyond the holding current. Also, immediately following the transition from the bulk to float states, the battery will only be 80% to 90% charged and the battery voltage will drop to the V_F level for some period of time until full charging is achieved.

In this charger the current sense comparator is used to regulate the holding current. The level of holding current is determined by the sensing resistor, R_{SH}. The other series

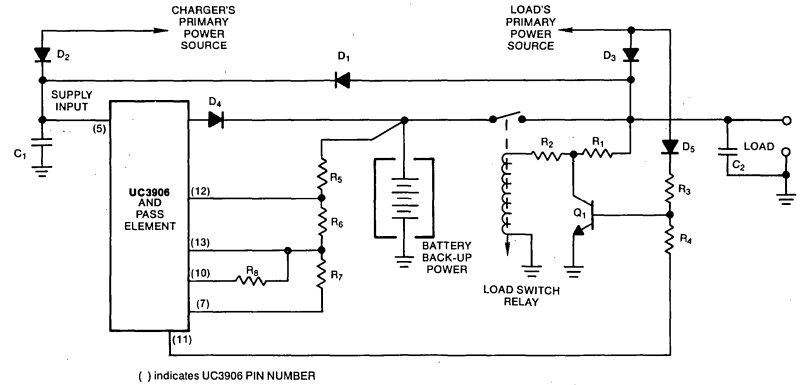


FIGURE 9. Using the enable comparator to monitor the battery voltage a precise discharge cut-off voltage can be set. When the battery reaches the cut-off threshold the trickle bial output switches off the load switch relay and the battery is left open circuited until input power is returned.

resistor, R_E, is necessary for the current sense comparator to regulate the holding current. Its value is selected by dividing the value of I_H into the minimum input to output differential that is expected between the battery and the input supply. If the supply variation is very large, or the holding current large, (>25mA), then an external buffering element may be required at the output of the current sense comparator.

The operating supply voltage into the UC3906 should be kept less than 45V. However, the IC can be adapted to charge a battery string of greater than 45V. To charge a large series string of cells with the dual step current charger the ground pin on the UC3906 can be referenced to a tap point on the battery string as shown in figure 11. Since the charger is regulating current into the batteries, the cells will all receive equal charge. The only offset results from the bias current of the UC3906 and the divider string current adding to the current charging the battery cells below the tap point. R_B can be added to subtract the bulk of this current improving the ability of the charger to control the low level currents. The voltage trip points using this technique will be based on the sum of the cell voltages on the high side of the tap.

PICKING A PASS ELEMENT AND COMPENSATING THE CHARGER

There are four factors to consider when choosing a pass device. These are:

1. The pass device must have sufficient current and power handling capability to accommodate the desired maximum charging rate at the maximum input to output differential.
2. The device must have a high enough current gain at the maximum charge rate to keep the drive current required to less than 25mA.
3. The type of device used, (PNP, NPN, or FET), and its configuration, may be dictated by the minimum input to output differential at which the charger must operate.
4. The open loop gain of both the voltage and the current control loops are dependent on the pass element and its configuration.

Figure 12 contains a number of possible driver configurations with some rough break points on applicable current ranges as well as the resulting minimum input to output differentials. Also included in this figure are equations for the dissipation that results on the UC3906 die, equations for a resistor, R_D, that can be added to minimize this dissipation, and expressions for the open loop gains of both the voltage and current loops.

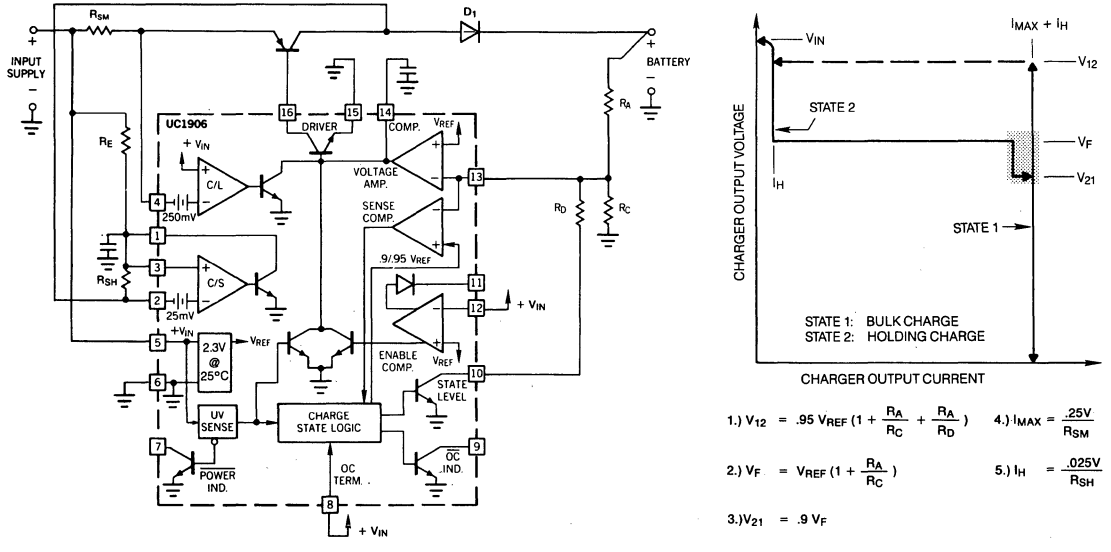


FIGURE 10. A dual step current charger has some advantages when large series strings must be charged. This type of charger maintains constant current during normal charging that results in equal charge distribution among battery cells.

As reflected in the gain expressions in figure 12, the open loop voltage gains of both the voltage and current control loops are dependent on the impedance, Z_C at the compensation pin. Both loops can be stabilized by adjusting the value of this impedance. Using the expressions given, one can go through a detailed analysis of the loops to predict respective gain and phase margins. In doing so one must not forget to account for all the poles in the open loop expressions. In the common emitter driver examples, 1 and 3, the equivalent load impedance at the output of the charger directly affects loop characteristics. In addition, a pole, or poles, will be added to the loop response due to the roll-off of the pass device's current gain, Beta. This effect will occur at approximately the rated unity gain frequency of the device divided by its low frequency current gain. The transconductance terms for the voltage and current limit amplifiers, (1/1.3K and 1/300 respectively), will start to roll off at about 500KHZ. As a rule of thumb, it is wise to kill the loop gain well below the point that any of these, not-so-predictable poles, enter the picture.

If you prefer not to go through a BODE analysis of the loops to pick a compensation value, and you recognize the fact that battery chargers do not require anything close to optimum dynamic response, then loop stability can be assured by simply oversizing the value of the capacitor used at the compensation pin. In some cases it may be necessary to add a resistor in series with the compensation capacitor to put a zero in the response. Typical values for the compensation capacitor will range from 1000pF to 0.22μF depending on the pass device and its configuration. With composite common emitter configurations, such as example 3 in figure 12, compensation values closer to the 0.22μF value will be required to roll off the large open loop gain that results from the Beta squared term in the gain expression. Series resistance should be less than 1K, and may range as low as 100 ohms and still be effective.

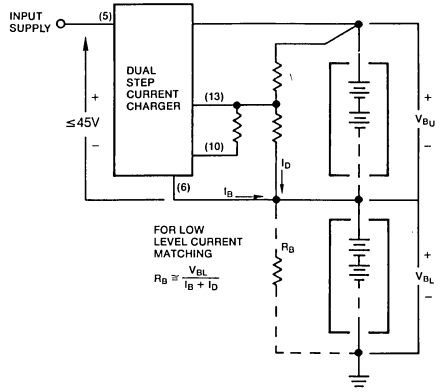
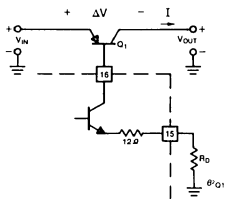
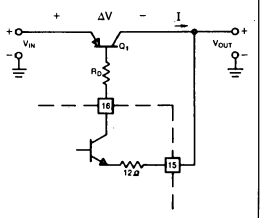
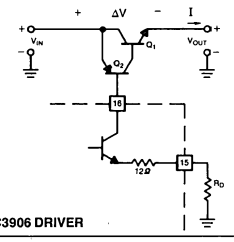
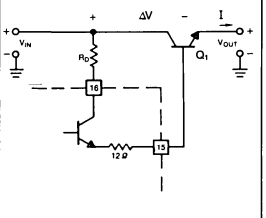


FIGURE 11. A dual step current charger can be configured to operate with input supplies of greater than 45V by using a tap on the battery to reference the UC3906. The charger uses the voltage across the upper portion of the battery to sense charging transition points. To minimize charging current offsets, R_B can be added to cancel the UC3906 bias and divider currents.

The power dissipated by the UC3906 requires attention since the thermal resistance, (100°C/Watt) of the DIP package can result in significant differences in temperature between the UC3906 die and the surrounding air, (battery), temperature. Different driver/pass element configurations result in varying amounts of dissipation at the UC3906. The dissipation can be reduced by adding external dropping resistors in series with the UC3906 driver,

	COMMON EMITTER PNP	COMPOSITE FOLLOWER	COMPOSITE COMMON EMITTER	NPN EMITTER FOLLOWER
TOPOLOGY	 UC3906 DRIVER	 UC3906 DRIVER	 UC3906 DRIVER	 UC3906 DRIVER
CURRENT RANGE	25mA <I <1000mA	25mA <I <1000mA	600mA <I <15A	25mA <I <1000mA
MINIMUM ΔV	ΔV >0.5V	ΔV >2.0V	ΔV >1.2V	ΔV >2.7V
UC3906 DRIVER DISSIPATION	$P_D \approx \frac{V_{IN} - 0.7V}{\beta_{Q1}} \bullet I - \frac{I^2 R_D}{\beta^2_{Q1}}$	$P_D \approx \frac{V_{IN} - 0.7V - V_{OUT}}{\beta_{Q1}} \bullet I - \frac{I^2 R_D}{\beta^2_{Q1}}$	$P_D \approx \frac{V_{IN} - 0.7V}{\beta_{Q1}\beta_{Q2}} \bullet I - \frac{I^2 R_D}{\beta^2_{Q1}\beta^2_{Q2}}$	$P_D \approx \frac{V_{IN} - 0.7V - V_{OUT}}{\beta_{Q1}} \bullet I - \frac{I^2 R_D}{\beta^2_{Q1}}$
EXPRESSION FOR R_D	$R_D \approx \frac{V_{IN\,MIN} - 2.0V}{I_{MAX}} \bullet \beta_{Q1\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - V_{OUT\,MAX} - 1.2V}{I_{MAX}} \bullet \beta_{Q1\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - 0.7V}{I_{MAX}} \bullet \beta_{Q1\,MIN}\beta_{Q2\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - V_{OUT\,MAX} - 1.2V}{I_{MAX}} \bullet \beta_{Q1\,MIN}$
OPEN LOOP* GAIN OF THE VOLTAGE CONTROL LOOP	$A_{OV} \approx \frac{Z_C}{1.3K} \bullet \frac{1}{R_D + 12} \bullet \beta_{Q1} \bullet Z_O \bullet \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \bullet \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \bullet \frac{1}{R_D + 12} \bullet \beta_{Q1} \bullet \beta_{Q2} \bullet Z_O \bullet \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \bullet \frac{V_{REF}}{V_{OUT}}$
OPEN LOOP* GAIN OF THE CURRENT LIMIT LOOP	$A_{OC} \approx \frac{Z_C}{300} \bullet \frac{1}{R_D + 12} \bullet \beta_{Q1} \bullet R_S$	$A_{OC} \approx \frac{Z_C}{300} \bullet \frac{1}{12/\beta_{Q1} + Z_O} \bullet R_S$	$A_{OC} \approx \frac{Z_C}{300} \bullet \frac{1}{R_D + 12} \bullet \beta_{Q1} \bullet \beta_{Q2} \bullet R_S$	$A_{OC} \approx \frac{Z_C}{300} \bullet \frac{1}{12/\beta_{Q1} + Z_O} \bullet R_S$

*Z_C = IMPEDANCE AT COMPENSATION PIN, PIN 14. Z_O = IMPEDANCE AT CHARGER OUTPUT.

FIGURE 12. There are a large number of possible driver/pass element configurations, a few are summarized here. The trade-offs are between current gain, input to output differential, and in some cases, power dissipation on the UC3906. When dissipation is a problem it can be reduced by adding a resistor in series with the UC3906 driver.

(see figure 12). These resistors will then share the power with the die. The charger parameters most affected by increased driver dissipation are the transition thresholds, (V_{12} and V_{21}), since the charger is, by design, supplying its maximum current at these points. The current levels will not be affected since the input offset voltages on the current amplifier and sense comparator have very little temperature dependence. Also, the stand-by float level on the charger will still track ambient temperature accurately since, normally, very little current is required of the charger during this condition.

To estimate the effects of dissipation on the charger's voltage levels, calculate the power dissipated by the IC at any given point, multiply this value by the thermal resistance of the package, and then multiply this product by –3.9mV/°C and the proper external divider ratio. In most cases, the effect can be ignored, while in others the charger design must be tweaked to account for die dissipation by adjusting charger parameters at critical points of the charge cycle.

SOME RESULTS WITH THE DUAL LEVEL FLOAT CHARGER

In figure 13 the schematic is shown for a dual level, float charger designed for use with a 6V, 2.5amp-hour, sealed lead-acid battery. The specifications, at 25°C, for this charger are listed below.

Input supply voltage . . . . . 9.0V to 13V
Operating temperature range . . . . . 0°C to 70°C
Start-up trickle current (I_T) . . . . . 10mA (V_{IN} = 10V)
Start-up voltage (V_T) 5.1V
Bulk charge rate (I_{MAX}) 500mA (C/5)
Bulk to OC transition voltage (V_{12}) . . 7.125V
OC voltage (V_{OC}) 7.5V
OC terminate current (I_{OCT}) 50mA (C/50)
Float voltage (V_F) 7.0V
Float to Bulk transition voltage (V_{31}) 6.3V
Temperature coefficient on voltage levels . . . . . –12mV/°C
Reverse current at charger output with the input supply at 0.0V . . . . $\leq 5\mu A$

In order to achieve the low input to output differential, (1.5V), the charger was designed with a PNP pass device that can operate in its saturation region under low input supply conditions. The series diode, required to meet the reverse current specification, accounts for 1.0V of the 1.5V minimum differential. Keeping the reverse current under 5μA also requires the divider string to be disconnected when input power is removed. This is accomplished, as discussed earlier, by using the input power indicate pin to reference the divider string.

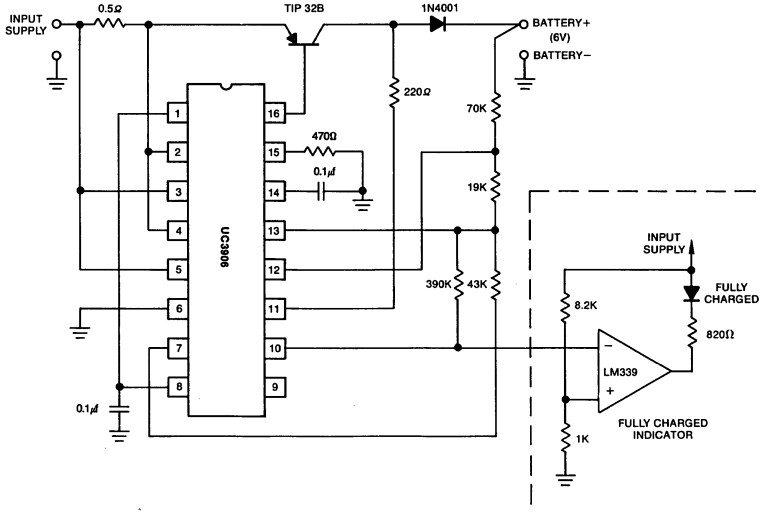


FIGURE 13. This dual level float charger was designed for a 6V (three 2V cells) 2.5AH battery. A separate "fully charged" indicator was added for visual indication of charge completion.

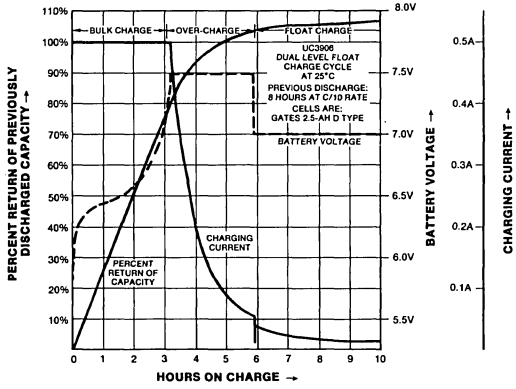


FIGURE 14. The nearly ideal characteristics of the dual level float charger are illustrated in these curves. The over-charge state is entered at about 80% return of capacity and float charging begins at just over 100% return.

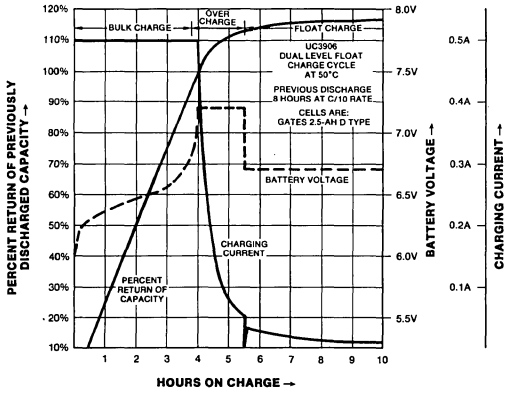


FIGURE 15. At elevated temperatures the maximum capacity of lead-acid cells is increased allowing greater charge acceptance. To prevent excessive over-charging though, the charging voltage levels are reduced.

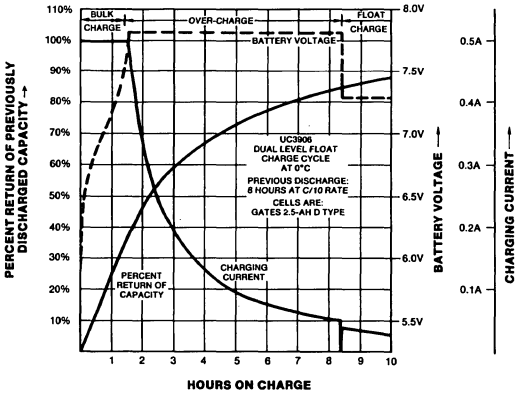


FIGURE 16. At lower temperatures the capacity of lead-acid cells is reduced as reflected by the less-than-100% return of capacity in this 0°C charge cycle, illustrating the need for elevated charging voltages to maximize returned capacity.

The driver on the UC3906 shunts the drive current from the pass device to ground. The 470ohm resistor added between PIN 15 and ground keeps the die dissipation to less than 100mW under worst case conditions, assuming a minimum forward current gain in the pass element of 35 at 500mA.

The charger in figure 13 includes a circuit to detect full charge and gives a visual indication of charge completion with an LED. This circuit turns on the LED when the battery enters the float state. Entering of the float state is detected by sensing when the state level output turns-off.

Figures 14-16 are plots of charge cycles of the circuit at three temperatures, 25°C, 50°C and 0°C. The plots show battery voltage, charge rate, and percent return of previously discharged capacity. This last parameter is the integral of the charge current over the time of the charge cycle, divided by the total charge volume removed since the last full charge. For all of these curves the previous discharge was an 80% discharge, (2amp-hours), at a C/10, (250mA), rate. The discharges were preceded by an over-night charge at 25°C.

The less than 100% return of capacity evident in the charge cycle at 0°C is the result of the battery's reduced capacity at this temperature. The tapering of the charge current in the over-charge state still indicates that the cells are being returned to a full state of charge.

REFERENCES

1. Eagle-Picher Industries, Inc., Battery Notes #200, #205A, #206, #207, #208.
2. Gates Energy Products, Inc., Battery Application Manual, 1982.
3. Panasonic, Sealed Lead-Acid Batteries Technical Handbook.
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HOW TO MEASURE K_T and K_V WITHOUT MEASURING TORQUE OR ANGULAR VELOCITY

INTRODUCTION

Motor manufacturers must be able to supply a good deal of technical details concerning the mechanical, electrical, and thermal specifications of their motors to enable the equipment designer to optimize their use. Among these specifications, there are two that state a motor's performance in converting electrical into mechanical energy, namely the torque constant K_T, and the voltage constant K_V.

The torque constant relates the torque produced at the motor shaft to the applied current, and is measured in units of torque per ampere. Thus, a motor having a K_T of 2 Nm/A will produce a torque of 2 Nm when driven with a current of 1 ampere. (The Newton-meter, Nm, is equal to 141.612 in oz.) To measure K_T, one applies a known current to the motor winding — or windings — and measures the resulting shaft torque.

The voltage constant is a measure of the motor's back emf, which is the voltage generated in the windings as a consequence of the rotor's movement. This back emf increases directly as the angular velocity increases, and is usually given in units of volts per thousand revolutions per minute, or V/KRPM, in this country. But there are certain advantages in stating this parameter in terms of volts per radian per second, or Vsec/rad. To measure it, you must measure voltage and angular velocity. This, by the way, applies to DC tachometers as well. Torque and angular velocity are not easy to measure, and measuring current in the amperes range is at best inconvenient. Can one obtain reliable values for K_T and K_V through a simple measurement that is easy and inexpensive to make? A positive answer to this question is given below.

It was James Watt, the Scottish engineer and inventor (1738-1819), who first thought of defining the output power of his steam engines in terms of horse-power. There was a demand for these engines to replace the working horses that were used in the various industrial operations of the time, such as textile, flour mills, etc. In those early days of the Industrial Revolution, Watt and his helpers must have been up to their necks in problems that ranged from strength of materials, fuel selection and handling, lubrication, corrosion, mechanics, dynamics, thermodynamics, noise, and safety, to the effects of mineral deposits in boilers, and so on. And then, there was the problem of how to rate the engine's power so that a given customer could be assured that his engine, once installed, would be adequate for the job.

Power is the work done per unit time. In the English system, this can be measured, for example, in foot-pounds per minute (ft lb/min). Borrowing some typical horses, and with the aid of harness, weights, ropes, pulleys, and a handful of whips, Watt determined by actual measurement that a horse can do work at the rate of 33,000 ft lb/min — on the average. This number is used to this day to define the unit of mechanical work known as the horsepower:

1HP = 33,000 ft lb/min
or
1HP = 550 ft lb/sec

Suppose a certain motor can produce torque of T ft lb at a speed of M rpm. The work done in one revolution is 2π T ft lb, and the rate of doing this work is 2π TM ft lb/min. This, divided by James Watt's measured horse equivalent, will be the motor's horsepower rating.

$$HP = \frac{2\pi T_E M}{33{,}000}$$

HP → horsepower
T_E → ft lb
M → RPM
33,000 → ft lb/HP min

If, instead of M (RPM) we prefer to use ω (rad/sec) for the angular velocity, this relationship becomes

$$HP = \frac{T_E \omega}{550}$$

ω → rad/sec
550 → ft lb/HP sec

Again, if we express the torque in metric units of Newton-meters, at 1.356 Nm/ft lb, we get:

$$HP = \frac{T_M \omega}{745.7}$$

T_m → Nm
ω → rad/sec
745.7 → Nm/HP sec

Finally if we express power in Watts instead of horsepower, using 745.7 watts/HP, we have:

$$W = T_M \omega$$

W → Watts

which tells us where the number of watts per horsepower comes from. Consequently, the shaft power in watts is simply the product of the torque in Nm and the angular velocity in rad/sec. And since W = VI we can write:

$$VI = T_M \omega$$

V → Volts

and

$$\frac{V}{\omega} = \frac{T_M}{I}$$

I → amperes
ω → rad/sec

This is an interesting result, for it states that the quantity $\frac{V}{\omega}$, in volts per rad/sec is identical to the quantity $\frac{T_M}{I}$ in Nm per ampere. Thus, in any electric motor, since

$$\frac{V}{\omega} = K_V \text{ and } \frac{T_M}{I} = K_T \qquad K_V = K_T$$

K_V → volt sec/rad
K_V → Nm/A

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By the way, expressing the torque in in. oz, and the shaft speed in KRPM, we get, as you can verify,

$$VI = \frac{T_e M_K}{1.352} \qquad T_e \rightarrow \text{in oz.}, \quad M_K \rightarrow \text{KRPM}$$

so that

$$K_{TE} = 1.352\ K_{VE} \qquad K_{TE} \rightarrow \text{in oz/A}, \quad K_{VE} \rightarrow \text{volts/KRPM}$$

This brings us from James Watt's steam engines and his customer's horses all the way to the modern electric motor, and the fixed ratio between torque constant and voltage constant turns out to be just a matter of definition. Both K_V and K_T have the same mks dimensions: $ML^2T^{-1}Q^{-1}$. If you know one, you also know the other; once you have measured one, you are through.

Measuring the voltage or torque constant of a permanent magnet brush motor or tachometer, for example, can be an extremely simple affair, requiring almost no equipment. Note that the units of K_V are volt sec/rad, which suggests that a measurement by means of an integrating circuit should be possible. In fact, if you integrate the voltage generated at the terminals as you turn the shaft through a given angle, you will have it.

Figure 1 shows a possible circuit.

The operational amplifier used should have very low input current and should be carefully balanced to minimize drift. All you need do is this:

A) Push the reset switch initially to discharge C and set the output voltage e_o to zero.

B) Rotate the motor shaft by a known angle, such as T turns.

C) Measure the voltage e_o.

D) The motor's voltage constant will be:

$$K_V = \frac{e_o RC}{2\pi T} \text{ volt sec/rad}$$

or,

$$K_{VE} = \frac{16.67\ e_o RC}{T} \text{ volt/KRPM}$$

E) The motor's torque constant in Nm/A will be the same number as K_V.

To convert K_V (volt sec/rad) to K_{VE} (volt/KRPM);

$K_{VE} = K_V \times (104.72)$

To convert K_T (Nm/A) to K_{TE} (in oz/A);

$K_{TE} = K_T \times (141.612)$

An interesting thing about this method is that it makes no difference how fast you rotate the shaft during the measurement — provided that your integrator drift is negligible. Furthermore, if you overshoot your angle, simply turn the shaft back to the right place before you read the output voltage.

This method gives a true and accurate measurement of two important motor parameters, without any need to measure current, torque, or angular velocity. In principle, and with a few more parts, it should be adaptable to measurements of hybrid steppers and brushless DC motors as well.

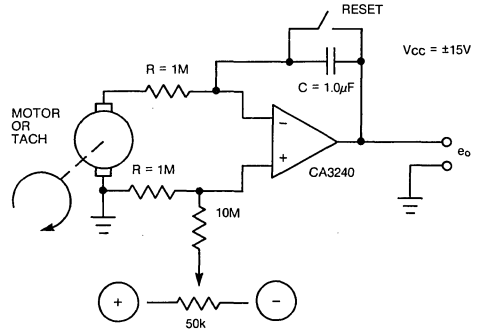

FIGURE 1. ACTIVE INTEGRATOR FOR MEASURING K_V. THE OP-AMP SHOULD BE WELL BALANCED TO MINIMIZE DRIFT.

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UC3620
BRUSHLESS DC MOTORS GET A CONTROLLER IC THAT REPLACES COMPLEX CIRCUITS

A COMMUTATOR AND DRIVER CHIP, COMPLETE WITH THERMAL AND UNDER-VOLTAGE PROTECTION AND TRANSIENT SUPPRESSION, RADICALLY SIMPLIFIES THE CONTROL OF BRUSHLESS DC MOTORS

INTRODUCTION

The popularity of the three-phase, brushless DC motor is on the rise for a number of good reasons: There are no brushes to wear out or to arc over, heat dissipation is better because the windings are on the stator, and good torque control is both possible and relatively easy to achieve with the availability of electronic circuits. The motor's main drawback has been the need to design and assemble a complex circuit consisting of six output power transistors with transient suppression diodes, a switching current control circuit, and a Hall logic decoder, plus loop control and protection circuitry.

The advent of the UC3620 controller chip greatly simplifies the designer's problem, for it integrates all these elements. This chip easily and safely controls motors requiring up to 2A of continuous current, and has a peak rating of 3A. The device has a maximum V_{CC} rating of 40V and is available in a 15-pin package rated at 25W. Only a half dozen external components are needed to get a motor running.

A three-phase brushless DC motor has two, four, or more permanent magnet poles mounted on its rotor. The required rotating field is produced by the stator's stationary windings, whose three phases must be commutated in the proper sequence. This sequence is governed by the rotor's angular position, and consequently, some means must be provided both to sense this position and to use that information to control the commutation sequence.

The sensing is accomplished by three Hall-effect devices mounted on the stator close to the rotor magnets, at the correct rotational angles. An electronic circuit decodes the Hall device signals and controls the direction of the currents applied to the three motor phases. This power switching is done by power transistors.

Another function must be added to the driving electronics, namely, that of controlling the motor current and maintaining it at the correct value. At high speed, the electric motor's back emf limits the phase currents. But at low speeds, the back emf is low (it is zero at stall), and therefore if the current is to be kept constant, the applied voltage must be reduced. This is done by sensing the motor current and using its value to regulate the duty cycle of the applied voltage, thereby controlling the average motor voltage. In this way, a constant-current source of motor power is obtained.

HOW IT WORKS

In the controller chip, each of the three output stages is a totem-pole pair (Figure 1) capable of sourcing and sinking the motor's full rated current. Inductive transients from the load are clamped to V_{CC} by Schottky diodes and to ground by the intrinsic substrate diodes, thus obviating the need for external clamping devices.

The power output stages have two functions. The first is to commutate the three motor phases in the proper sequence, producing unidirectional torque in the rotor. The second is to switch the applied motor voltage in the manner selected and programmed by the user, maintaining the output current at the desired level. This switching control of current is accomplished in a fixed-off-time, two-quadrant mode, providing the automatic peak current limiting and low ripple current essential to high electrical efficiency at the motor windings.

The emitters of the three bottom transistors of the totem-pole output stages are connected to Pin 1, through which all the motor current flows. If a low-value resistor is placed between this pin and ground, a usable voltage proportional to motor current is derived without appreciable I^2R losses.

This current-sensing voltage serves as a feedback signal for the switching current control loop. It is applied to the I_{SENSE} input through an RC filter, which prevents false triggering due to noise spikes in the current waveform.

An internal voltage comparator determines whether the voltage $V_{I\ SENSE}$ is equal to V_{REF}, a positive variable reference voltage dependent on the output of the chip's error amplifier. If Q of the monostable multivibrator (that follows the comparator) is high, the chip's output stages are enabled, the output current increases, and $V_{I\ SENSE}$ also increases until it becomes positive with respect to V_{REF}.

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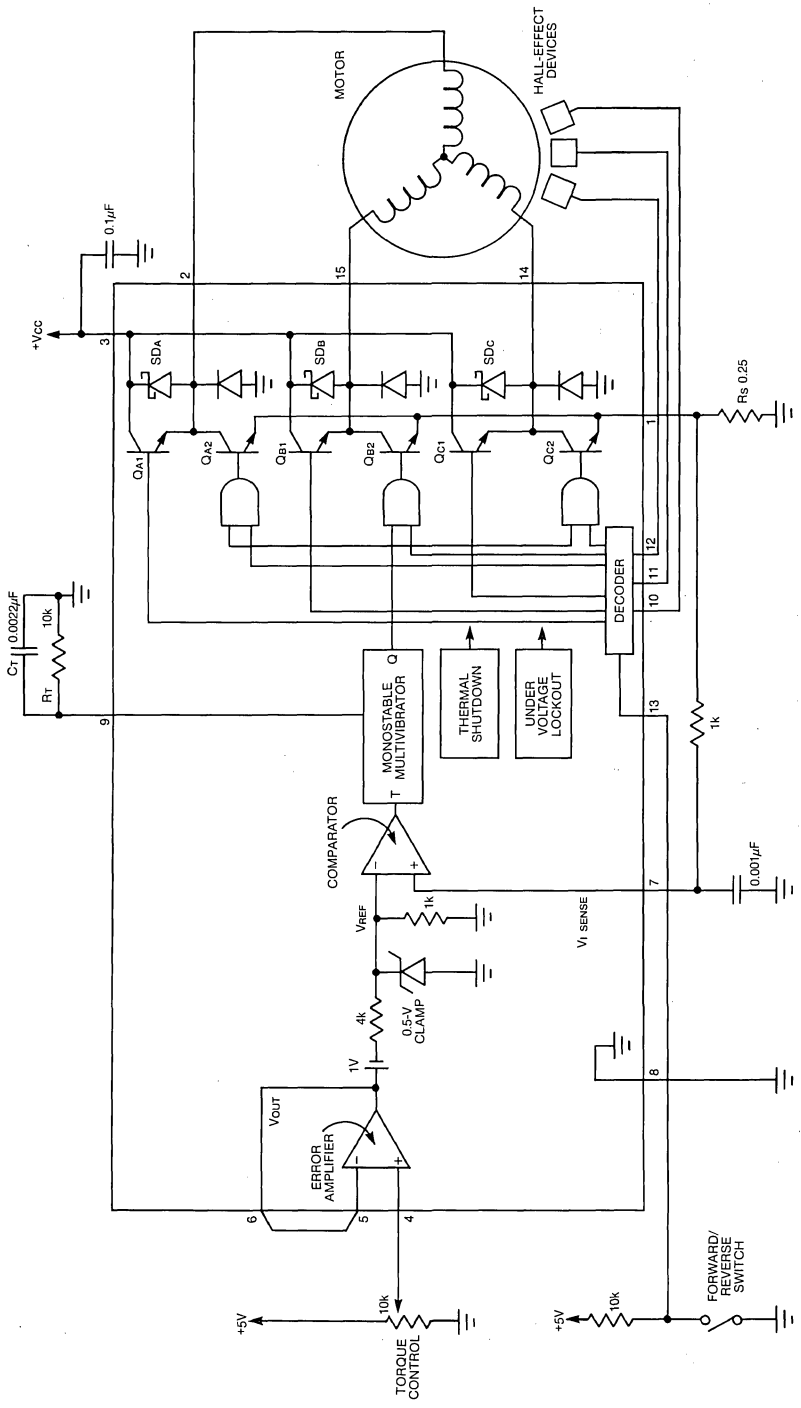

FIGURE 1. THE UC3620 CHIP PROVIDES FULL CONTROL OF MOTOR CURRENTS UP TO 2A, WITH ROTATION IN BOTH DIRECTIONS. HALL-EFFECT DEVICES INTERNAL TO THE MOTOR PROVIDE POSITION INFORMATION THROUGH A DECODER TO THREE TOTEM-POLE DRIVERS. COMPARING THE CHANGING VOLTAGE ACROSS RS WITH THE ERROR AMPLIFIER OUTPUT HELPS KEEP THE CURRENT CONSTANT.

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At this point the comparator resets the monostable, forcing Q low and disabling the output stages. The motor current now circulates through one of the Schottky diodes and the conducting upper transistor because of the stored inductive energy, until the monostable off-time has elapsed (Figure 2). Q then returns to the high state and the cycle is repeated.

The switching off-time is fixed, since it is determined by the user's choice of timing components R_T and C_T. At the start of the off-time, capacitor C_T is charged to +5V, and the monostable outputs are held in the off state until this voltage decays exponentially to a level of 2V. Since resistor R_T supplies the only path for the discharging current, it is possible to calculate the time required, t_{OFF}, in seconds:

$$\exp\left(\frac{-t_{OFF}}{R_T C_T}\right) = \frac{2}{5}$$

or:

$$\frac{-t_{OFF}}{R_T C_T} = \ln(2/5) = -0.916$$

$$t_{OFF} = 0.916 R_T C_T$$

When the 2 volt level is reached, the monostable is set again, and the cycle repeats.

The reference voltage, V_{REF}, then, is the controlling voltage of what is in effect a transconductance amplifier of which the controlled output is the motor current through resistor R_S. To repeat, the circuit controls the peak value of the current. If the switching frequency is high (low current ripple), the assumption may be made that the average value of motor current, I_M, is approximately equal to the peak, and so:

$$V_{REF} = I_M R_S$$

$$G_T = \frac{I_M}{V_{REF}} = \frac{1}{R_S} \text{ Siemens}$$

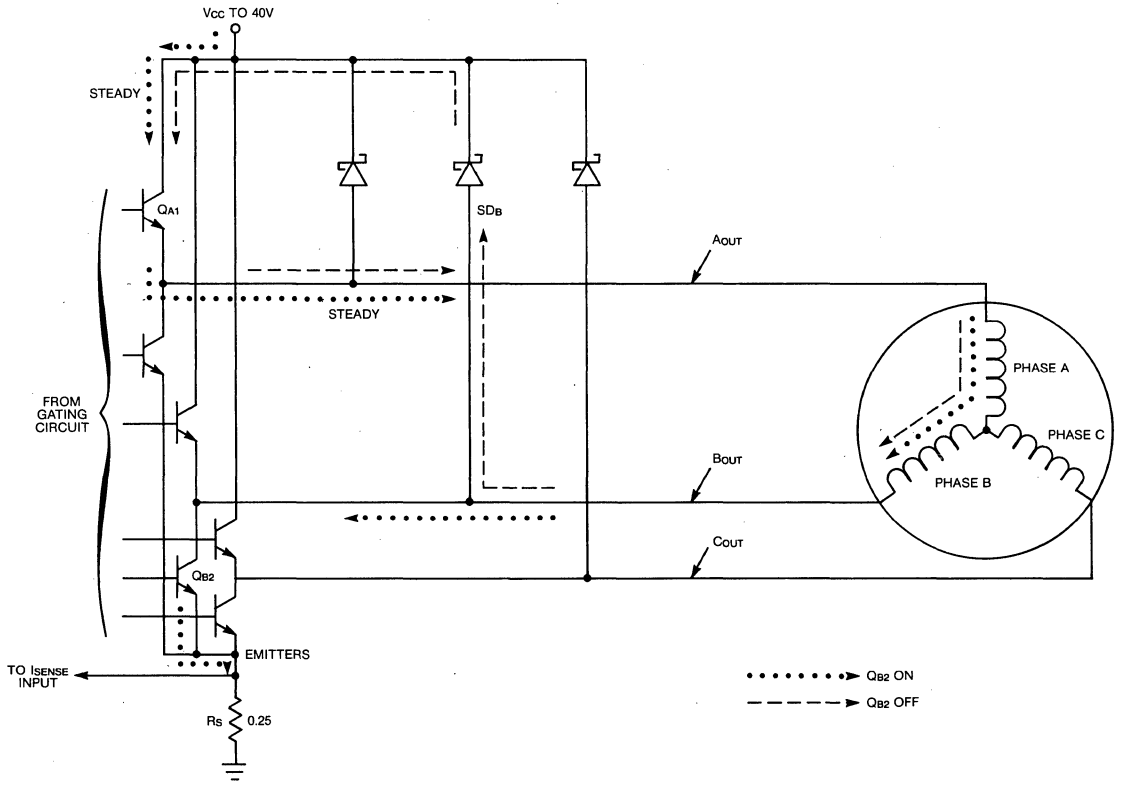

FIGURE 2. WHEN Q_{B2} IS ON, CURRENT FLOWS THROUGH Q_{A1} AND TWO MOTOR WINDINGS TO GROUND (DOTTED ARROWS). DURING THE TIME THAT Q_{B2} IS OFF, THE STORED ENERGY IN THE WINDING INDUCTANCE FLOWS THROUGH SCHOTTKY DIODE SD_B, TRANSISTOR Q_{A1}, AND BACK THROUGH THE WINDINGS (DASHED ARROWS).

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The maximum value of V_{REF} is limited to 0.5V by a zener diode (Figure 1 again). This value sets a limit to the maximum motor current as well, since:

$$I_{MAX} = \frac{0.5}{R_S} \text{ amperes}$$

Consequently, the proper selection of R_S protects both the motor and the chip from excess current.

The motor is connected to the chip's three outputs A_{OUT}, B_{OUT}, and C_{OUT}. The motor windings are Y-connected, and the driver energizes two phases at a time, the third one being off. Thus each driver output will be in one of three states: high (V_{CC}), off (high impedance), or low (0V), generating six possible combinations (Table 1).

Table 1. Terminal Conditions for Different Driver Output States

OUTPUT STATE	TERMINAL A	TERMINAL B	TERMINAL C
$A\bar{B}Z$	High	Low	High Z
$AZ\bar{C}$	High	High Z	Low
$ZB\bar{C}$	High Z	High	Low
$\bar{A}BZ$	Low	High	High Z
$\bar{A}ZC$	Low	High Z	High
$Z\bar{B}C$	High Z	Low	High

SIX STATES

In each of the six possible states, one of the upper transistors is on, together with one of the bottom transistors. In any of the states, it is the bottom transistor that controls switching, while the upper device remains conducting. For example, in state $A\bar{B}Z$, current flows continually through upper transistor Q_{A1}, but switches between lower transistor Q_{B2} and Schottky diode SD_B (Figure 2 again). This switching action results in low current ripple through the motor and is known as two-quadrant operation, in which the power supply current flows only in one direction, namely, into the driver (Figure 3). One advantage of this unidirectionality is that a shunt regulator is not necessary to prevent an overvoltage at the V_{CC} bus during motor deceleration.

A more significant advantage is that it results in the least current ripple for a given switching rate. More precisely, the current waveform's form factor (the ratio of its rms to its average value) is closer to unity. Since the amount of I^2R heating depends on the rms value of I, whereas torque depends on the average value, a form factor approaching unity results in greater motor efficiency.

The current reference voltage V_{REF} at the inverting input of the chip's comparator depends on the output voltage, V_{OUT}, of the error amplifier. The relationship between the two is:

$$V_{REF} = \frac{V_{OUT} - 1}{5}$$

The offset of 1V between V_{OUT} and the 5:1 voltage divider ensures that the error amplifier can always achieve zero current at the motor. The amplifier itself has a high gain of 80dB minimum, an f_t of 0.8MHz; and is internally compensated for stable operation.

In a feedback speed control application, even with a reduction in gain of 14dB due to the 5:1 resistive attenuator between the amplifier and the comparator, there is still a minimum DC gain of 66dB, which is more than adequate for most requirements. The same consideration applies to the 1V offset, which is overshadowed by the high-gain loop as well.

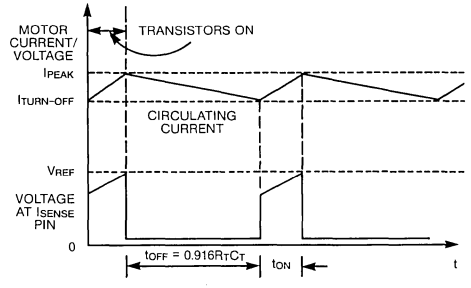

FIGURE 3. THE CHIP'S SWITCHING CIRCUIT CONTROLS MOTOR CURRENT ON A PULSE-BY-PULSE BASIS. WHEN THE BOTTOM TRANSISTOR OF AN OUTPUT STAGE IS ON, THE CURRENT AT FIRST RISES RAPIDLY AND THEN DECAYS SLOWLY AS IT CIRCULATES THROUGH THE TRANSISTOR'S ASSOCIATED DIODE. THE FORM FACTOR OF THE WAVEFORM IS THEREFORE CLOSE TO UNITY, SO THAT HEATING OF THE COILS IS REDUCED.

The chip also includes two protection circuits to help make it more reliable. The under-voltage lockout prevents the output stages from being energized unless the supply voltage can provide sufficient base current to the drive transistors. The maximum V_{CC} start-up threshold is set at 8V and has a built-in hysteresis of 0.5V.

A thermal shutdown circuit affords protection against excessive junction temperatures. This circuit disables the drive transistors when the chip's temperature is between 150°C and 180°C. When the temperature returns to a safe value, normal operation is automatically restored.

When the power source for a motor is DC, a commutator is needed to, in a sense, alternate the power applied to the windings. A brushless DC motor uses an external power commutator. As a rule, however, the motor has an electronic device internal to it that generates information relative to angular position for use in controlling the commutator.

CONTROLLING BRUSHLESS MOTORS TO 2A

The control chip was designed to drive any three-phase brushless DC motor of up to 2A and is particularly suited for motors with integral Hall-effect devices. H_A, H_B, and H_C (Figure 1 again) are TTL-compatible inputs that, together with the Forward-Reverse input (FWD/REV), determine the output states (Table 2).

The Hall input sequence available in the standard control device, for either forward or reverse rotation, is a modified Gray code with 000 and 111 not used. Motors with Hall output codes that include 000 and 111 can be handled by the addition of an inverter to one of the Hall lines, so that the 000 and 111 exclusion required by the chip is obtained. Alternative logic schemes can be supplied to accommodate not only different Hall codes, but also variations in driver output format.

When used as described, the device operates in a current feedback mode and acts as a current controller, or rather as a transconductance amplifier. This closed-loop circuit can be made part of another feedback loop to control the motor speed. Controlled speed loops are of interest in many applications, some of which require a very high degree of control accuracy. For example, a crystal-referenced phase-locked loop is needed to control the spindle speed of magnetic disk drives.

Table 2. Hall Device Logic Coding

HALL DEVICE INPUTS			FORWARD/ REVERSE LINE	DRIVER OUTPUT
H_A	H_B	H_C		
1	0	1	1	$A\bar{B}Z$
1	0	0	1	$AZ\bar{C}$
1	1	0	1	$ZB\bar{C}$
0	1	0	1	$\bar{A}BZ$
0	1	1	1	$\bar{A}ZC$
0	0	1	1	$Z\bar{B}C$

Note: A change of state in the Forward/Reverse line inverts the output states, thus reversing the direction.

USING A FREQUENCY-CONTROLLED LOOP

In less stringent applications, a frequency-controlled loop may be used in which the motor speed error is minimized, although it is never zero. Such a loop can be built using the signal from one of the Hall-effect devices as a measure of motor speed. This approach has the merit of being inexpensive, but because of the relatively low frequencies involved, it is not always easy to implement.

A tachometer circuit that uses a sample-and-hold technique which provides a control voltage that is relatively free of ripple yet responds quickly is shown in Figure 4. It uses a 4538 dual one-shot IC to generate two sequential pulses at the beginning of each Hall cycle.

Op-amp A_1 interfaces the TTL signal from the Hall device with the CMOS 4538. This device contains two one-shots, P_1 and P_2, that trigger on the negative transition of a signal. The P_1 output is a positive pulse 50μs wide, determined by R_1 and C_1. This pulse enables analog switch G_1 (14066), causing the voltage at capacitor C_4 to equal that of C_3.

The termination of the P_1 pulse triggers P_2, producing a negative 4ms pulse that turns on transistor Q_1 and charges C_3 to +12V. At the end of pulse P_2, C_3 is discharged exponentially by resistors R_4 and R_5. The decay of the C_3 voltage lasts for the remainder of the Hall signal period. The next P_1 pulse transfers the new C_3 voltage to C_4, again through G_1.

After that, the P_2 pulse recharges C_3 for a new measurement. Since the discharge time of C_3 decreases with increasing motor speed, the tachometer's output voltage increases with speed. G_1, together with C_4, acts as a sample-and-hold circuit. Because the output voltage of C_4 is a sampled function of speed, updated at each Hall cycle, the output ripple is minimal with varying speed and approaches zero at constant speed.

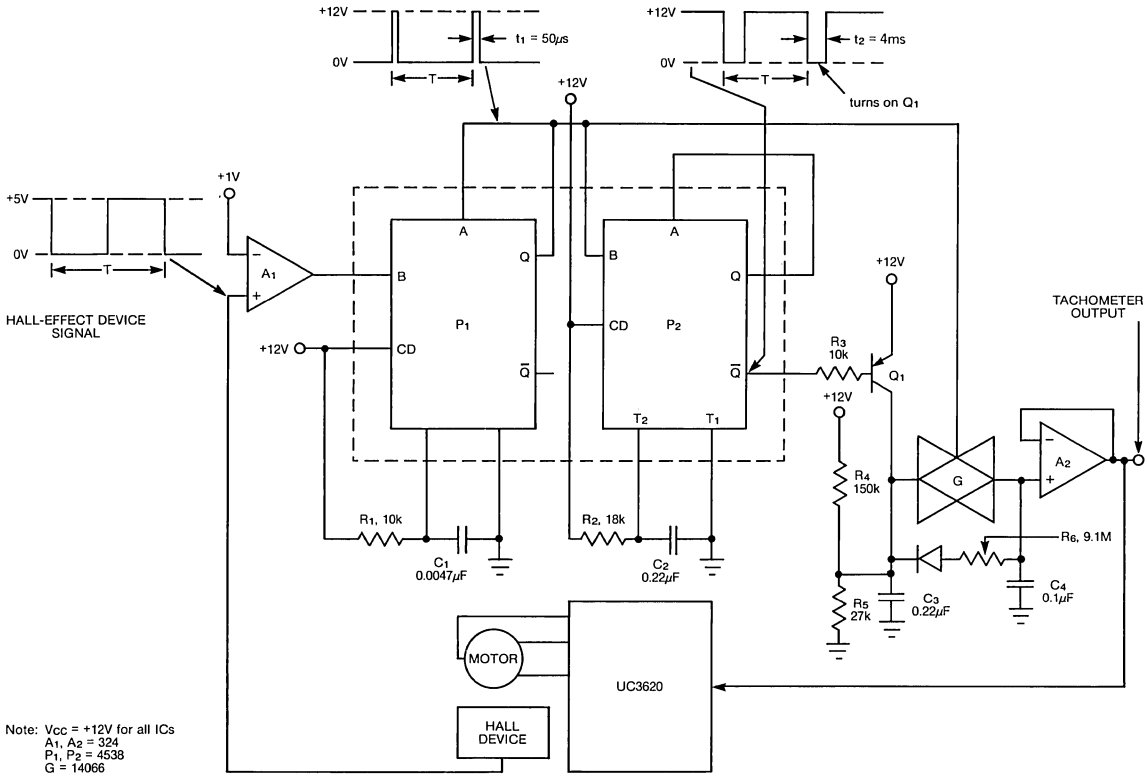

FIGURE 4. IN THIS APPLICATION, THE UC3620 SERVES IN A MOTOR SPEED CONTROL CIRCUIT. TWO ONE-SHOTS, P_1 AND P_2, CONTROL A SAMPLE-AND-HOLD CIRCUIT MADE UP OF ANALOG SWITCH G_1 AND CAPACITOR C_4. THE LATTER'S OUTPUT FEEDS AN AMPLIFIER PROVIDING A TACHOMETER OUTPUT PROPORTIONAL TO SPEED. THAT OUTPUT IS FED BACK TO THE UC3620 INPUT, THEREBY CONTROLLING THE MOTOR'S SPEED.

NEW PULSE WIDTH MODULATOR CHIP CONTROLS 1 MHz SWITCHERS

ABSTRACT

Controversy prevails as to the benefits of pushing switched mode pulse width modulated power supplies higher and higher in frequency. Two facts are undisputed though: the industry is pushing switching frequencies up daily and no PWM control IC has been available to optimally control circuits running above several hundred kilohertz. A new IC, the UC3825, has been developed with the top end of the PWM frequency spectrum in mind to simplify high speed control problems. This chip, suitable to either voltage or current mode control, addresses the speed critical parameters that have been glossed over in the past: error amp bandwidth, output drive capability, oscillator frequency range, and propagation delay. A one megahertz, 50 watt supply has been built to demonstrate the chip.

PWM CONTROLLER REVIEW

Briefly reviewing popular control IC's on the market today should serve to illustrate one source of the headaches belonging to designers of high frequency switching power supplies. The snaggle-toothed appearance of the table illustrates the fact that high speed parameters have generally been ignored. The entries in this table represent the tried and true first and second generation standbys (1524, 1525, 494), dedicated off line control (1840), and current mode (1846). All these architectural approaches have certainly proven sufficient for numerous converter designs, but all lack the processing speed required to keep track of a 1 MHz switcher, or even 200 kHz for that matter. Many specifications in the table are missing completely, some are only typical, and the few guaranteed limits leave much room for improvement.

Of prime importance here is the delay time between fault detection and turning off the power switch – the speed critical path. When a fault occurs, either the on chip over-current sense section or an off chip fault detector plus the shutdown section of the chip must work fast enough to turn off the power switch before destructive current levels introduce an automatic (and permanent) power down feature to the supply. This feature, of course, is manifested in blown power devices. The problem is aggravated at the onset of core saturation, since switch currents then rise at much faster rates.

Also important is the drive capability of the output stage of the control chip chosen. Rise and fall times must be consistent with switching speeds or else an output buffer will have to be added. This, of course, adds delay to the speed critical path placing tighter demands on the delays through the chip or forcing the designer to over-specify the power elements to insure fault survival. Over-specifying, however, adds cost, weight and volume as transistors, heat-sinks, and transformers are beefed-up. These consequences are in direct opposition to the very motives for going to higher frequencies in the first place – reduced volume and lower cost.

On-chip error amplifiers have also been a design obstacle in the past. Why build a high frequency switcher and then over compensate the loop due to lack of error amp bandwidth? Designers have been forced to conser-

SPEED COMPARISON OF PWM CONTROLLER IC'S

	SHUT DOWN DELAY (ns)		OVER-CURRENT SENSE DELAY (ns)		ERROR AMP BANDWIDTH (MHz)		ERROR AMP SLEW RATE (V/ s)		OUTPUT RISE/FALL TIME (ns)	
	TYP	MAX	TYP	MAX	TYP	MIN	TYP	MIN	TYP	MAX
SG3524	–	–	–	–	3	–	–	–	200	–
UC3524A	200	–	600	–	3	–	–	–	200	–
UC3525A	200	500	–	–	2	1	–	–	100	600
TL494	–	–	–	–	0.8	–	–	–	200	400
UC3840	–	–	200	400	2	1	0.8	–	–	–
UC3846	300	600	200	500	1	0.7	–	–	50	300
UC3825	50	80	50	80	5.5	3	12	6	30	60

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vatively use the bandwidth available simply due to a lack of guaranteed specifications in many cases. Also, some characteristics which would prove useful haven't been specified at all. Slew rate is such a specification that has great bearing on the large signal response of the supply.

By comparison, the 3825 specifically addresses the speed critical parameters. Maximum propagation delays of 80 ns nearly belong in the "order of magnitude" improvement catagory. Slicing delays yielded a hefty output stage capable of 1.5 Amp peak currents. The guaranteed rise time is, in fact, more a function of internal slew rates than external loading in the 1000 pF range. **The error amp guaranteed to 3 MHz and 6 V/μs promises ease of use when controlling wide-band loops.**

UC3825 BLOCK DIAGRAM

The design philosophy for the 3825 was to build a chip faster than any other available and tailor it to fit neatly into high frequency converter designs. It includes a dual totem-pole output stage capable of driving most power mosfet gates stand-alone, and the versatility to be useful for DC to DC, off-line, bridge, flyback, push-pull, and even resonant mode converter topologies. The member of a family covering the conventional temperature ranges, the UC3825 is specified for zero to 70 degrees centigrade while the UC2825 spans −25 to 85, and the UC1825, −55 to 125.

The block diagram of the 3825 (figure 1) is architecturally similar in many respects to a number of previous PWM controllers. It includes an oscillator, undervoltage-lock-out circuit, trimmed bandgap voltage reference, wideband error amplifier, PWM comparator, PWM latch, toggle flip-flop, soft start section, comparators for over-current sensing and reinitializing soft start, and dual totem-pole outputs. The input to the PWM comparator is brought out to a separate pin so that it can be connected either to the timing capacitor for conventional PWM designs or a current sensing network for current mode control schemes.

In normal operation, the oscillator establishes a fixed clock frequency issuing blanking pulses to terminate one period and begin the next. These pulses serve to reset the PWM comparator while blanking the outputs off. After the blanking pulse, one output turns on until the ramp input (level shifted 1.25 Volts) exceeds the error amp output voltage. This sets the PWM latch which turns the output off and triggers the toggle flip-flop, selecting the other output for the next period.

THE SPEED CRITICAL PATH

The blocks that set the 3825 aside as the controller best suited for frequencies over several hundred kilohertz are those in the speed critical path (high-lighted blocks in figure 1.): the PWM comparator and current limit comparator in the front end; the PWM latch and associated internal logic; and the ouput stage. Signal

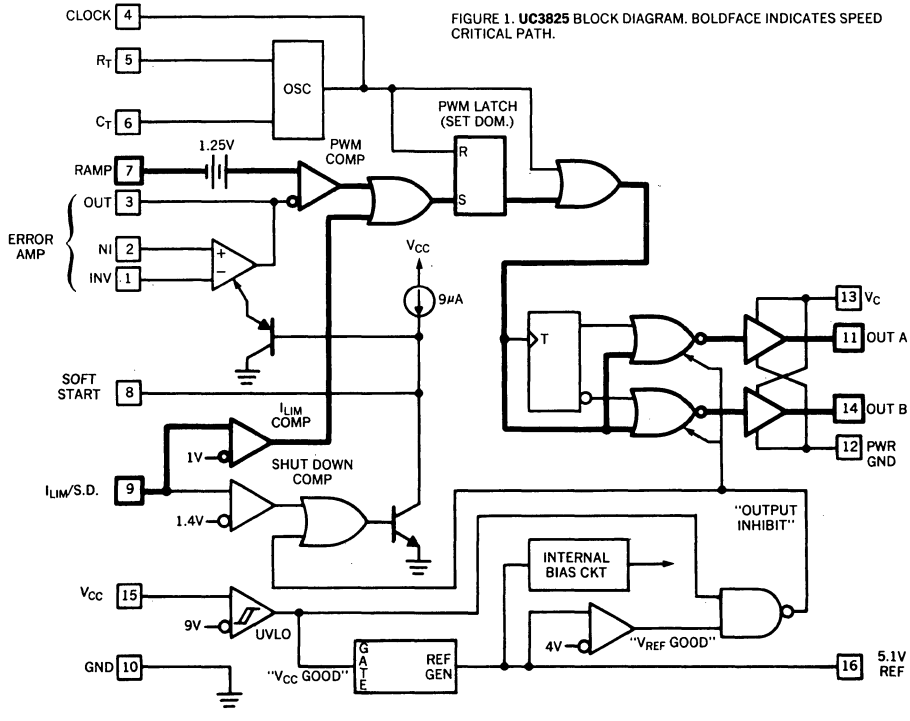

FIGURE 1. **UC3825** BLOCK DIAGRAM. BOLDFACE INDICATES SPEED CRITICAL PATH.

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propagation through these subcircuits makes or breaks a design during a fault condition. In the 3825, the propagation delay from either the Ramp input or the Current-limit sense input to the output pins is typically 50ns, very much faster than any chip available today.

Comparators

The PWM comparator is basically an npn differential pair with an emitter follower output (figure 2a). The pair is biased so that the output swing is one Vbe. This guarantees none of the transistors in the comparator will saturate while providing output voltage levels compatible with the internal logic. In order to assure that the input common mode range of the comparator is not exceeded (the range of an npn input pair cannot go below approximately one Volt), a 1.25 Volt level shift is included between the non-inverting input of the comparator and the input pin of the chip. This allows the ramp input to swing from zero to approximately three Volts. The inverting input is tied directly to the output of the error amplifier.

The benefit of this approach is ease of use both in current mode and conventional PWM applications. For the older PWM circuit approach, the ramp input pin can be tied directly to the oscillator Ct pin while current mode users can simply tie a ground referenced current sense network directly to the Ramp pin.

The current limit comparator is very similar in design to the PWM comparator. Its inverting input is referenced internally to a one Volt level derived from the 5.1 Volt reference allowing the non-inverting input to be brought directly to the current limit pin. Functionally, when a fault causes the Current-limit pin to exceed one Volt, it acts just like the PWM comparator, setting the PWM latch and causing the outputs to remain off for the duration of the clock cycle.

The current-limit comparator can also be combined with the 3825 outputs and a few external components to form a constant volt-second product clamp (figure 2b). This clamp is useful in current mode systems to prevent core saturation during load transients. When either output turns on (goes high), capacitor, C, is charged from Vin through resistor, R. Normal circuit operation would turn off the outputs causing C to be discharged before it reaches one Volt. If, however, it does reach one Volt, the current-limit comparator terminates the output pulse. Since the charge rate is proportional to Vin (assuming Vin is much greater than one Volt), then a constant Volt-second product clamp of one Volt times RC is achieved.

Logic

All of the speed critical logic, including the PWM latch, the toggle flip-flop, and various gates are a cross between emitter coupled logic and emitter function logic. In either case, their speed relies on emitter coupled pairs and emitter follower buffers biased to insure that no transistor saturates. Although two OR's, a NOR and the PWM latch are directly in the critical path between the input comparators and the output drivers, they account for only twenty percent of the total delay, the remainder being shared between the comparators and the output stage.

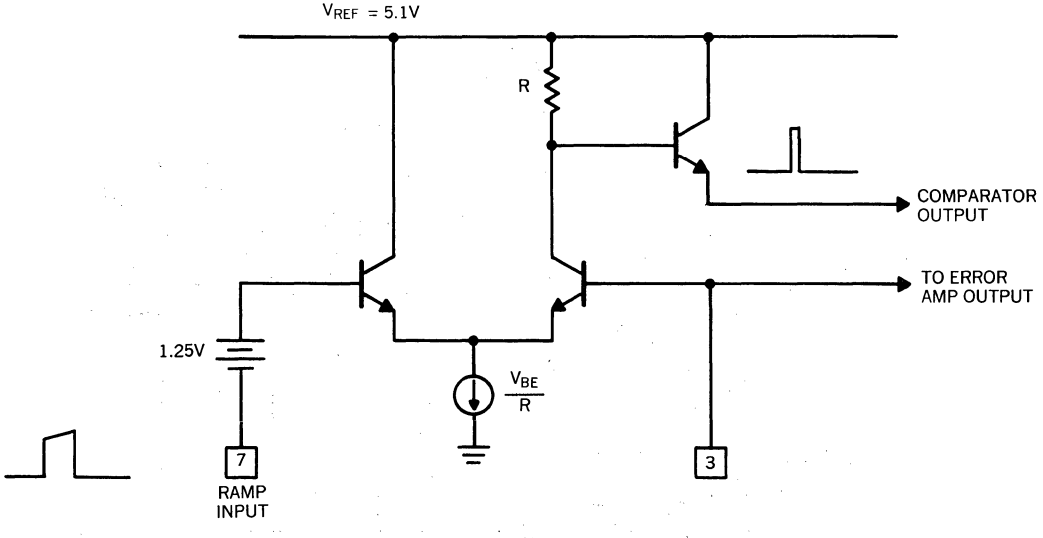
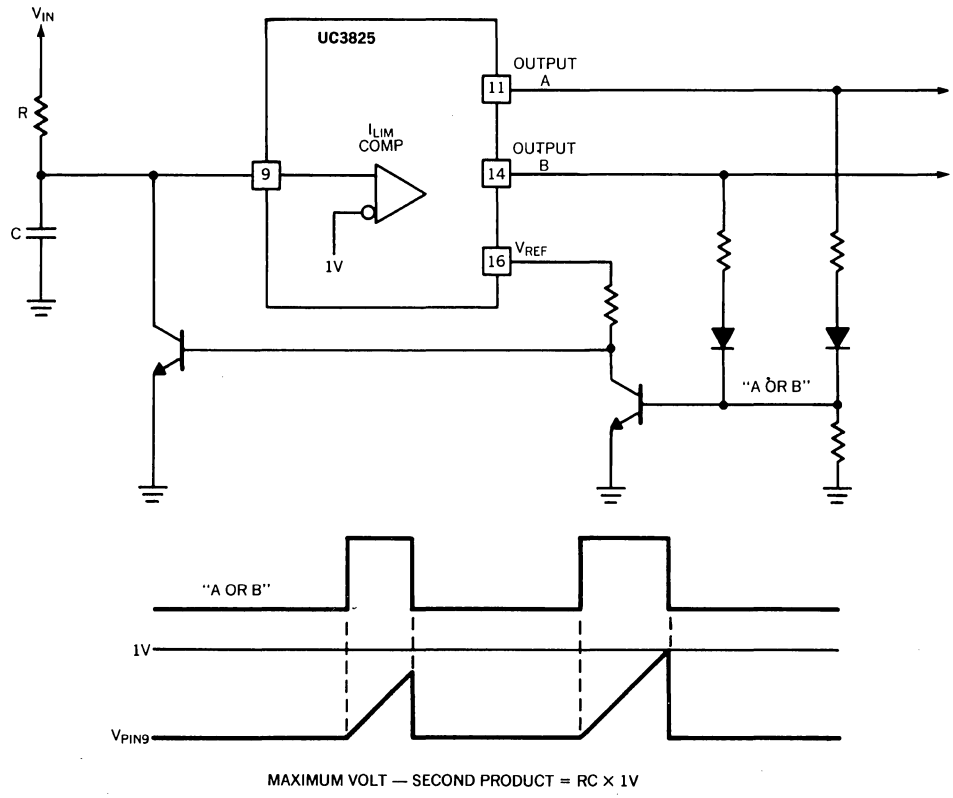


FIGURE 2a. PWM COMPARATOR SCHEMATIC.



MAXIMUM VOLT — SECOND PRODUCT = RC × 1V

FIGURE 2b. CONSTANT VOLT-SECOND PRODUCT CLAMP IMPLEMENTED USING THE CURRENT LIMIT COMPARATOR.

Outputs

Speed from one pin to another does little or no good unless the signal coming out of the chip has the strength to do its job. The dual totem-pole drivers of the 3825 are capable of driving 1000 picofarads from one rail to the other in a mere 30 nanoseconds. In fact the peak current avilable is in excess of 1.5 Amps. This kind of brute strength is sufficient for driving a wide range of power mosfet's in a variety of applications.

Some older PWM controllers with totem-pole output stages are plagued with hefty amounts of cross conducted charge during output transitions. This can result in major self heating problems especially at higher clock rates. The 3825 output stage (figure 3a) has been modeled after the successful designs of the UC3846 and UC3842. The differences are in bias values and the addition of Schottky diodes. This circuit guarantees the output transistors, Q1 and Q2, are driven with complementary signals to keep cross conducted charge under control. This approach necessarily involves a compromise since speed is of the utmost concern. Delays could be inserted to guarantee zero cross conducted charge, but that would be contrary to the required propagation delays for high speed operation. The outputs have been adjusted to yield these rise and fall times at a penalty of only 20 nanocoulombs of cross conducted charge per transition. At a clock frequency of 500 kHz, this only adds an additional 10 mA to the supply current.

Rather than dwell on cross conducted charge, which is measured with no load on the outputs, it is more appropriate to examine the performance with typical loads. The most anticipated load is a power mosfet. The impedence presented by the gate of the fet is application dependent, but is primarily capacitive. Therefore, consider the requirements of driving a capacitor with a square wave voltage. The charge required for one cycle is equal to the capacitance times the voltage. The average current taken from the supply is that charge times the switching frequency. This determines the power required from the supply to drive the cap. Since the cap is an energy storage element, all the power

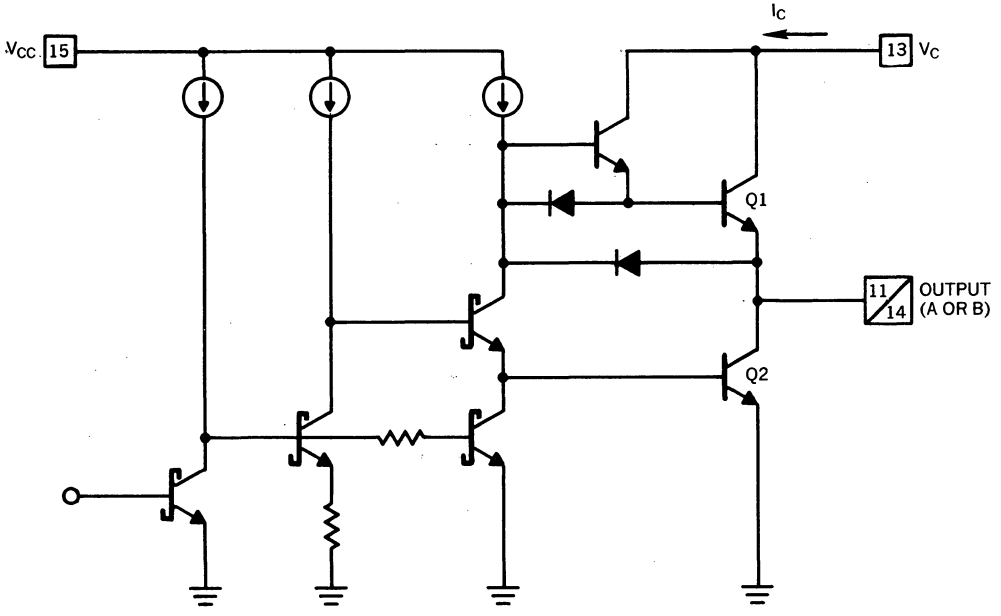
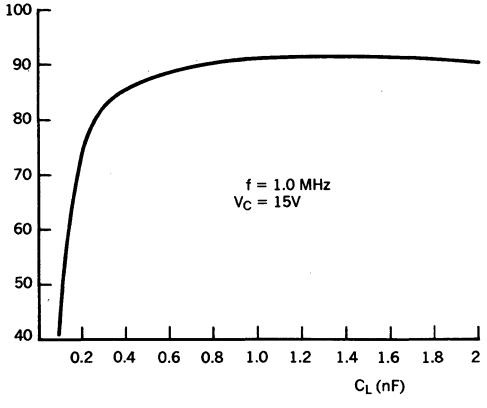


FIGURE 3a. OUTPUT STAGE SIMPLIFIED SCHEMATIC.

taken from the supply is dissipated by the chip. An efficiency figure for the chip can be defined as the ratio of the theoretical power dissipation to the actual power dissipated by the chip. This can be determined for a given frequency and supply voltage by measuring the average supply current into the Vc pin (assuming the peak output voltage is approximately equal to the supply voltage). The figure of efficiency, then, is: (CVf)/Ic. The graph of figure 3b shows the 3825 optimized to drive capacitances above 200pF. Care should always be taken when driving high capacitive loads to make sure the maximum power dissipation level of the chip is not exceeded.

FIGURE 3b

$$\text{EFFICIENCY} = \frac{cvf}{I_C} (\%)$$



Another side effect of the output stage should be considered. Any node in a circuit capable of driving large capacitances at these rates begins quickly to resemble an LC tank. Transmission lines, even one inch in length, can become troublesome. The trouble occurs when, on the falling edge at an output, the load rings and actually pulls the output pin below ground. For years IC manufacturers have been warning users not to allow certain pins to go below ground and the 3825 output pins carry the same warning. The collector of the pull down transistor becomes a parasitic npn emitter when pulled below the chip's substrate, which is grounded (figure 4). The collector, or collectors as the case is, are every other npn collector and pnp base on the chip. The ones that are closer to the parasitic emitter collect proportionally more current than ones further away. Physical size of the parasitic collectors also plays a similar role. The results of this phenomenon can range from nonobservable to severe. Resembling leakage current internally, reference voltages can be altered, oscillator frequency can jitter, or chip temperature can be elevated. Dummy collectors tied to ground are inserted into the 3825 chip which help to attenuate this problem but the designer still needs to be aware of it. The problem's potential is not a horror story, though. Among the easiest of solutions is some form of damping in the load circuit (for example ten ohms series resistance) and a good high speed diode, Schottky if possible, to clamp the output pin's negative going excursion.

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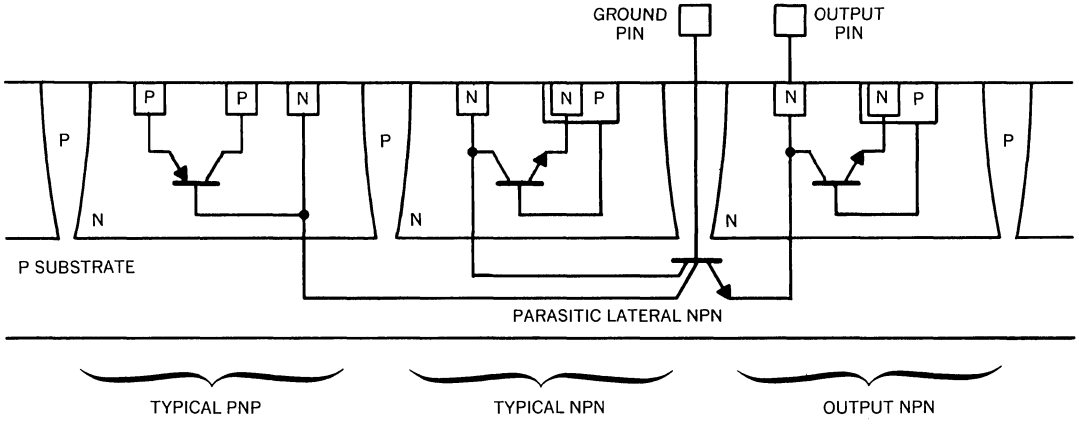

FIGURE 4. PARASITIC NPN TURNS ON WHEN SUBSTRATE – EPI JUNCTION IS FORWARD BIASED.

HIGH SPEED COMPLEMENTARY BLOCKS

An integrated circuit controller with delays of 50ns through its speed critical path is certainly a leading candidate for high frequency switcher applications. There are a few blocks just off the race path that need also to be fast in order to fully qualify the chip for such applications. The oscillator and error amplifier are two such blocks.

Oscillator

From the users point of view, the oscillator looks identical to many that have gone before it (figure 5a). Composed of an all npn comparator, this oscillator has dual thresholds – the upper at 2.8 Volts and the lower at one Volt. Charging current for the timing capacitor, Ct, is mirrored from the timing resistor, Rt. The Rt pin is held at a temperature stable 3 Volts. Temperature stability of the oscillator, then, is achieved by maintaining stable thresholds at the comparator. When Ct has charged to the upper threshold, Q3 turns on to sink a controlled current of approximately 10 mA. The effect of this action is that the discharge of Ct is done in an orderly manner allowing the comparator to reliably catch it when crossing the lower threshold. This also prevents Q3 from saturating, reducing delays in the oscillator and enabling it to operate at higher frequencies. The 3825 oscillator is nominally specified at 400kHz with an initial guaranteed accuracy of 10%. Temperature stability is typically better than 5% while voltage stability (frequency shift over supply voltage) is 0.2%. Oscillator dead time, which effects controller dynamic range, can typically be held to 100ns at 1MHz, allowing 90% duty cycles.

In applications where two 3825's are used in close proximity and synchronization is desired (figure 5b), the oscillator in one chip can be disabled by tying Rt to the reference Voltage. That chip, then, must be clocked by joining the clock pins of both chips. Multiple 3825's also can be synchronized from a master 3825 or other external sync signal. The slave chips are programmed to run at a frequency somewhat lower than the master chip. The master then inserts a sync pulse forcing each slave's Ct over the top threshold and causing discharge action to occur. This way, each chip generates its own clock pulses synchronized to a master clock.

Error Amplifier

The 3825 error amplifier is a voltage gain amp with premium bandwidth and slew rate. Again using only npn's in the signal path, a compensated unity gain bandwidth of 5.5 MHz is achieved. The simplified schematic (figure 6) shows the signal path of the amplifier. Note that while the compensation scheme is not extremely complex or brand new in nature, neither is it the simple dominant pole approach. Included are two zeros located beyond the unity gain frequency to enhance phase margin. One is created by a capacitor across the emitter degeneration resistors in the first stage and the second is formed by a resistor in series with the dominant pole capacitor.

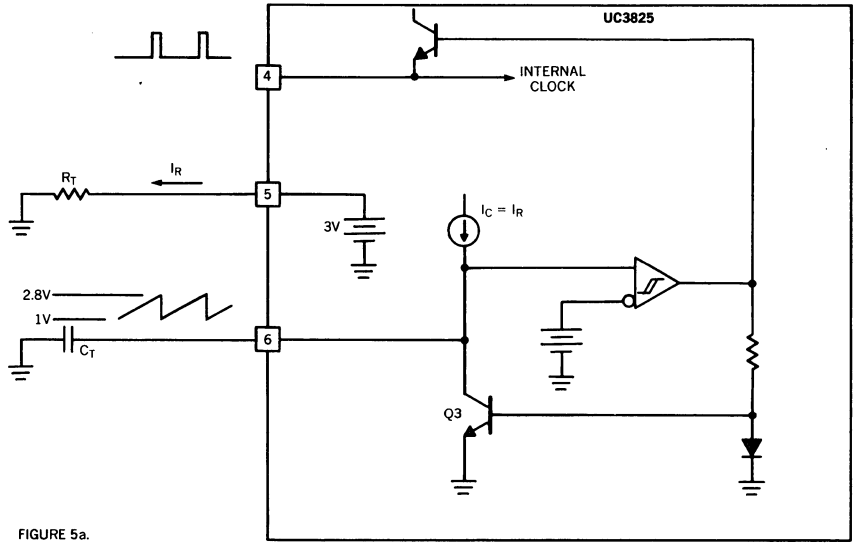

FIGURE 5a.

FIGURE 5b.

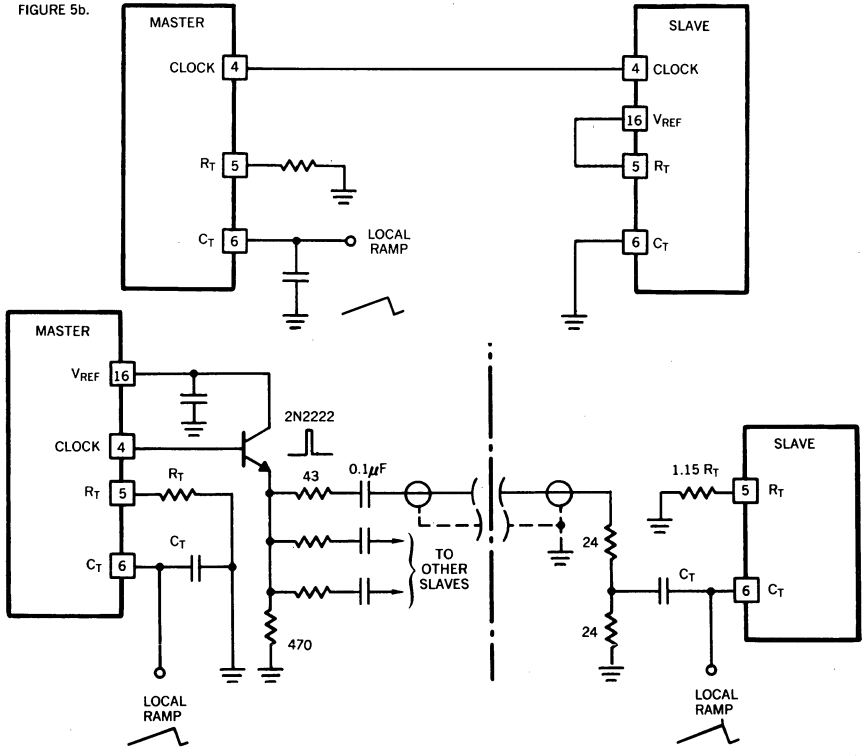

FIGURE 5. OSCILLATOR SIMPLIFIED SCHEMATIC (a) AND TWO SYNCHRONIZATION METHODS (b).

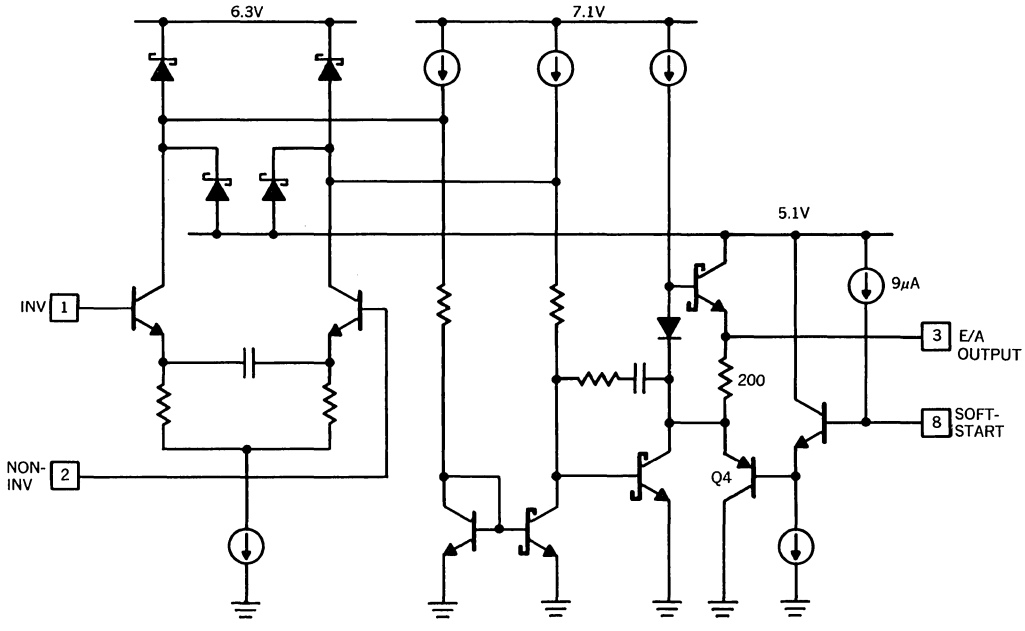

FIGURE 6. SIMPLIFIED SCHEMATIC OF WIDE BAND ERROR AMPLIFIER SHOWING SOFT START CLAMP SCHEME.

By degenerating Gm, the emitter resistors allow an increased first stage bias current level. This contributes to a 12 V/μs typical slew rate. High slew rate, while desirable for good large signal transient response, is not enough to guarantee minimal response time. Often an amplifier may have high slew rates yet exhibit long delay times coming out of saturation when it has been driven to a rail. To defeat this problem, all critical nodes within the amp have been Schottky clamped.

GLUE BLOCKS

The remaining blocks, while not speed critical, mold the 3825 into a more complete PWM controller. The reference, a time proven design, is trimmed to guarantee 5.1 Volts at better than one percent tolerance. This voltage is then held over conditions of line, load, and temperature changes to a two percent total spread.

Soft-start is very simply implemented by a pnp clamp transistor merged into the output stage of the error amp (figure 6). During soft start, while the 9 μA current source is charging the external capacitance on pin 8, Q4 actively forces pin 3 to follow pin 8. In this manner a controlled slow start can be achieved for either voltage or current mode systems. When the error amp comes into regulation, Q4's emitter-base junction is reverse biased and offers no further interference to the normal operation of the amp.

In addition to slow starts, the soft-start pin can be used to other ends. Clamping the maximum voltage this pin is allowed to rise to will then effectively clamp the maximum swing of the error amplifier. In a conventional PWM scheme this results in a duty cycle clamp while in a current mode application, it establishes the maximum peak current level.

Fault conditions are sensed by the 3825 at pin 9 which is shared by the inputs of the current limit comparator and the shut down comparator. When this pin exceeds one Volt, the current limit comparator sets the PWM latch, terminating the output for the remainder of that cycle. As with normal operation, setting the PWM latch causes the toggle flip-flop to switch states. If the pin is further raised to exceed 1.4 Volts, the shut-down comparator forces the soft-start pin to sink a guaranteed minimum of one milliampere rather than sourcing 9 microamperes. Thus the shut down comparator causes the soft start capacitor to be discharged rapidly. After the fault signal is removed the 3825 will then execute a normal soft-start sequence.

One method of combining current-limit and shut-down signals is shown in figure 7. Here, in a current mode control example, a current sense transformer is used to translate switch current to proper voltage analogs for optimal control at both the Ramp and Current-limit sense pins while the shut-down signal is inserted with a resistive summing technique.

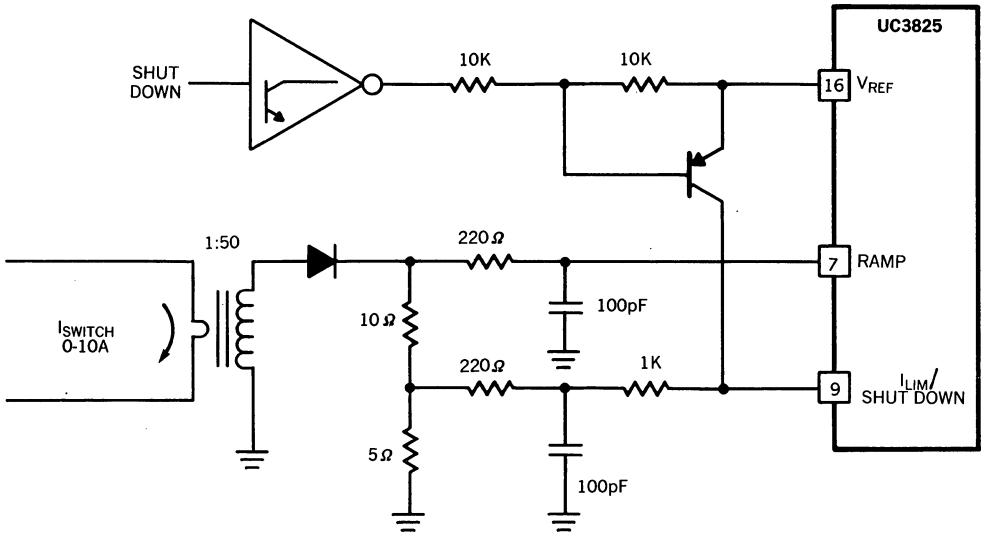

FIGURE 7. CURRENT LIMIT SENSE AND SHUT DOWN SIGNALS ARE COMBINED AT PIN 9 IN THIS CURRENT MODE EXAMPLE.

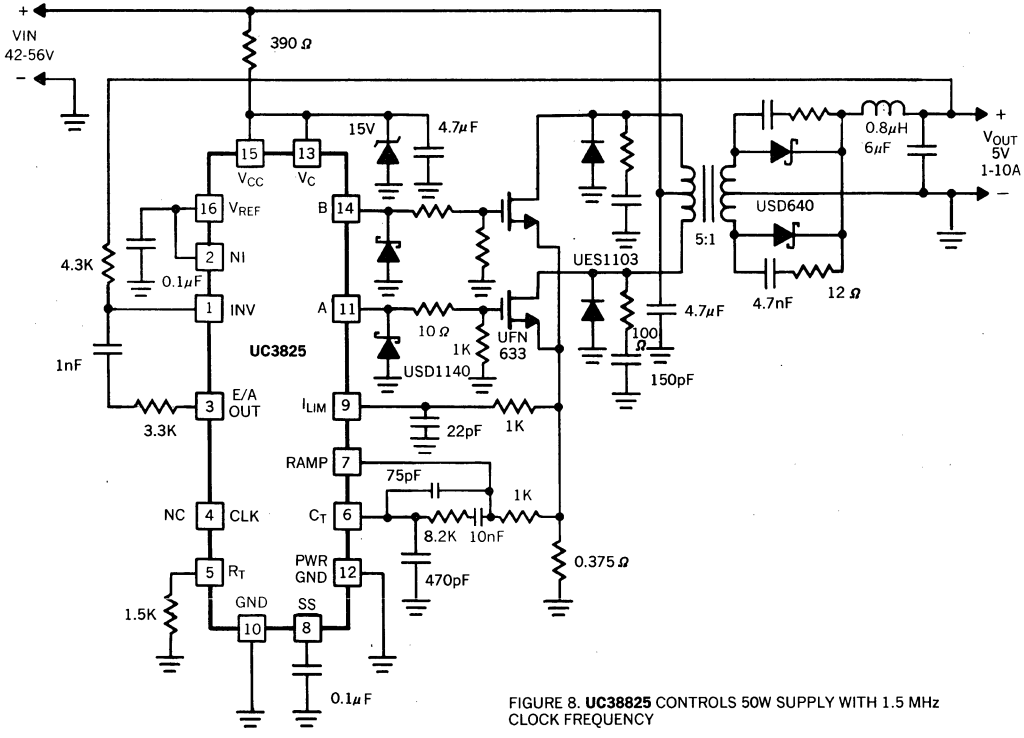

FIGURE 8. **UC38825** CONTROLS 50W SUPPLY WITH 1.5 MHz CLOCK FREQUENCY

Starting the 3825 involves the Under-voltage lockout portion of the chip. This block acts like a comparator with it's inverting input biased to 9 Volts and having 0.8 Volts of hysteresis. If Vcc is below the UVLO threshold, the reference generator and the internal bias are turned off, Keeping Icc at a typical 1.1 mA and the outputs in a high impedence state. When Vcc exceeds the UVLO threshold, the reference is turned on and the chip comes alive. Bedlam is avoided, however, as a second comparator monitors the reference voltage and inhibits the outputs until the reference is high enough to ensure intelligent operation. This inhibit signal also holds the soft start pin at a low voltage. After the reference is sufficiently high, the chip begins a soft start sequence.

50 WATT DC-DC PUSH-PULL CONVERTER

A 48 to 5 Volt, 50 Watt converter has been built as a test vehicle for the chip (figure 8). Designed around a push pull, current mode controlled topology, the circuit runs from a 1.5 MHz clock. In the interest of simplicity, the ramp input and current limit pins were tied together underutilizing the available dynamic range of the Ramp pin by a factor of 3. A ground plane, judicious bypass capacitors and tight layout technique yielded a circuit that could be easily interrogated without significant noise interference problems.

In this simple application, the 3825 performs all the tasks required to regulate the 50 W power stage. The gate drive for the two power mosfets comes directly from the chip. Current loop slope compensation is resistively summed with the current sense signal at pin 7. Overall loop compensation is implemented with two resistors and a capacitor on the error amplifier. Taking advantage of the 1.5 MHz switching frequency and the wide bandwidth characteristics of the error amp, the control loop was compensated to zero dB at 300kHz.

CONCLUSION

Presenting an easy to use PWM architecture, the UC3825 possesses the necessary high speed characteristics to control switchers in the higher frequency ranges. This fills a void that has hindered high frequency applications in the past. A simple example running at 1.5 MHz points to a future of faster switching supplies.

SCHOTTKY RECTIFIERS FOR LOW-VOLTAGE OUTPUTS

ABSTRACT

Schottky rectifier device designs are reviewed with the aim of obtaining minimum power loss for output rectifier applications operating in the 2 to 3 volt range. The performance of a new low V_F Schottky design is described.

INTRODUCTION

Schottky rectifiers are routinely used as output rectifiers in switching power supplies. For output voltages of 5 volts or more, the efficiencies achieved are satisfactory for most applications. As output voltages decrease to the 2 to 3 volt range needed for the latest MOS ICs and to 2V needed for bipolar ECL, we need to look critically at the Schottky rectifier to see whether there is anything that can be done to reduce the losses in this device.

In this paper the circuit and device are treated together as one problem. The circuit operating conditions are taken as parameters and the device design is varied with the aim of achieving minimum rectification loss. The intention is to present results in terms which are familiar to most device users and circuit designers. Device physics nomenclature and analyses are kept to a minimum.

The paper concludes with a discussion of a new low V_F Schottky rectifier design which is currently in production. The implications of improved cooling techniques on the optimum Schottky design are also discussed.

DEVICE DESIGN

A cross-section of a typical Schottky rectifier is shown in Figure 1. Recent Schottky designs make use of a p-n junction "guard ring" which is the p-type region that is used to terminate the edge of the Schottky. A major reason for incorporating the guard ring is to provide a transient voltage suppressor with good energy absorption capability as close as possible to the main Schottky junction.

Device Variables

Consider the behavior under reverse bias. If the current flowing over the guard ring is I_1, and I_2 is the current in the Schottky portion, then the two components will behave with voltage as indicated in Figure 2. The guard ring is designed to give a breakdown voltage BV_1 slightly less than BV_2, the breakdown voltage of the Schottky junction. With this approach, transient reverse current, e.g. due to transformer leakage inductance, which would be destructive if carried by the I_2 path will be safely shunted by the p-n junction.

There are five variables which are generally used to describe each design. These are:

N_d, W_n: doping and thickness of the n-type epitaxial layer

x_j: metallurgical junction depth of the p-type diffusion

A_J: area of the Schottky junction

φ_B: barrier height (V) for the Schottky junction

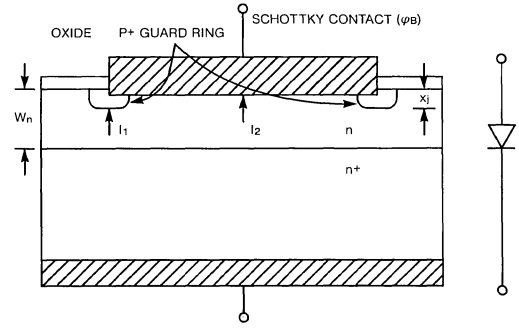

FIGURE 1. SCHOTTKY RECTIFIER CROSS-SECTION.

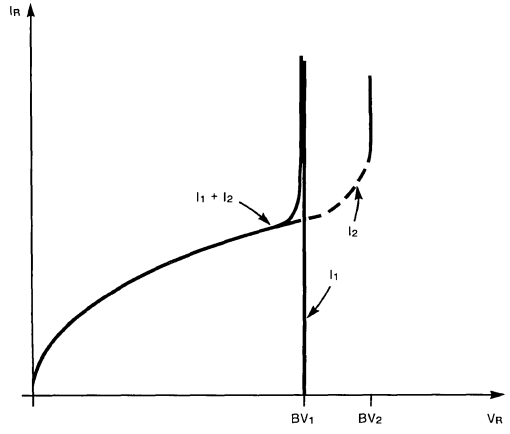

FIGURE 2. REVERSE I-V CHARACTERISTICS SHOWING THE CURRENT COMPONENTS I_1 AND I_2 of FIGURE 1.

The vertical dimensions W_n and x_j together with N_d determine the breakdown voltage and thereby the reverse voltage rating of the rectifier. These variables are usually chosen to meet a given BV requirement and at the same time minimize the series resistance contributed by the epitaxial layer.

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The (electron) barrier height φ_B is defined here in volts, and it refers to the energy band diagram shown in Figure 3, where $q\varphi_B$ is the distance in eV from the metal fermi level at the surface to the conduction band edge in the silicon. The barrier height is a function of the metal used for the barrier material which is normally deposited by RF sputtering. Metals such as platinum, tungsten, nickel, chromium, and molydenum which form a silicide are preferred for the barrier material.

The choice of barrier height represents a compromise between trying to achieve a low forward drop (small φ_B) and the ability to survive high temperatures without thermal runaway (large φ_B). The influence of barrier height on rectification losses is considered later in the paper.

From a manufacturing standpoint, it is desirable to limit the number of variations of the list of five variables while still providing a product line that meets market needs. Usually what is done is to fix everything except A_J which is then varied by selecting various die sizes to meet a range of forward current ratings.

The next level of adjustment involves designing to meet a different reverse voltage while still keeping the same barrier height. This is the type of design variation considered at the end of the paper.

Adjusting φ_B can be done, but it represents the most costly of the changes available in terms of capital equipment and process development. Therefore, manufacturers need to be convinced of a satisfactory market size before they undertake a change in barrier material.

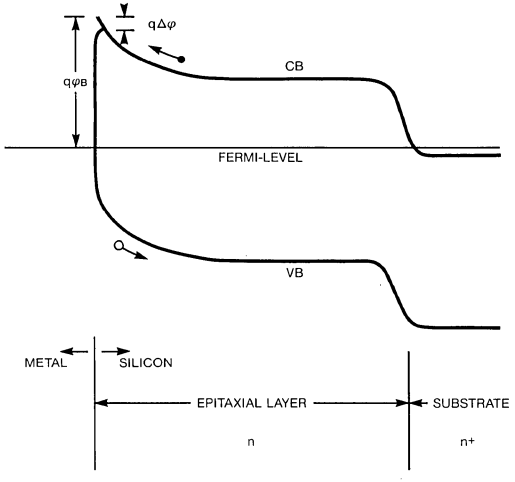

FIGURE 3. ENERGY BAND DIAGRAM AT EQUILIBRIUM ($V_F = 0$).

Circuit Conditions

For a given application, each rectifier is subjected to current and voltage waveforms which determine P_L, the average power dissipated by one rectifier. This power flows through the device package and associated heat sink to the surrounding ambient which is at temperature T_A. The junction temperature T_J is given by

$$T_J = T_A + P_L \cdot R_{\theta JA} \quad (1)$$

where $R_{\theta JA}$ is the net junction-to-ambient thermal resistance.

A full-wave or push-pull type of output circuit with each rectifier conducting 1/2 of the period is taken to be representative of a typical Schottky application. For an inductive input filter, the wave forms can be approximated as shown in Figure 4. Actual waveforms will show a recovery type of behavior during turn-off which can become important at switching frequencies comparable to 1MHz. For this analysis, we are ignoring switching losses.

For each application we assume that these quantities are defined:

I_F: the peak rectified forward current

V_R: peak reverse voltage

T_A: ambient temperature

$R_{\theta JA}$: junction-to-ambient thermal resistance. This value includes the junction-to-case thermal resistance of the package.

If we use (1) to convert T_A and $R_{\theta JA}$ input data to T_J, then this list is equivalent to defining three quantities which must be met by a design which is a function of the five device variables. That is, there are two degrees of freedom in selecting the device design. The usual procedure is to try to minimize both the power losses P_L and the device size, which is roughly equivalent to minimizing the device cost.

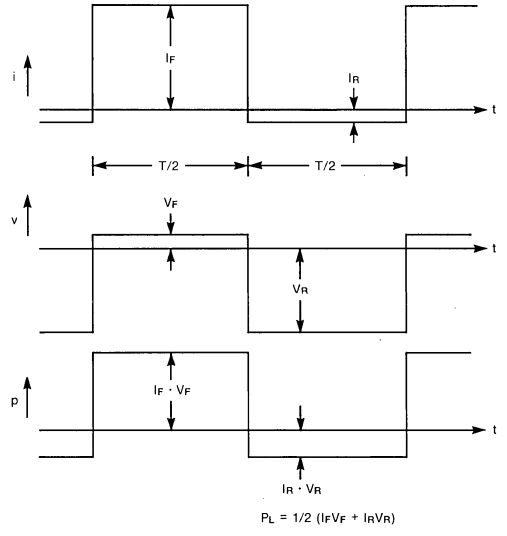

FIGURE 4. CURRENT, VOLTAGE, AND POWER WAVEFORMS.

The scheme followed in this paper is to determine how the power losses change as a function of $R_{\theta JA}$ and T_A, with various device variables or suitable combinations of variables taken as parameters.

Device Model

Accurate predictions of device performance can only be achieved if one has an accurate device model. We have found that the usual Schottky model of an ideal barrier in series with a fixed resistance works well for a wide range of situations, but it is also frequently necessary to account for conductivity modulation of the n-layer. This modulation is not due to the guard ring, which injects a relatively small amount of excess charge, but is due to the Schottky barrier itself (1). For a given barrier this effect becomes more important when N_d is small (higher BVs) or when the junction temperature is raised.

The curves of Figure 5 show the comparison between measured and calculated forward I-V characteristics for a BV = 55V Schottky, which is similar to a Unitrode USD545 ($A_J = 0.176\ cm^2$). The dashed line shows the calculated I-V curve assuming a fixed series resistance, that is, no conductivity modulation. Note that there is a significant discrepancy between this and the solid curve at high currents and 125°C.

When there is significant conductivity modulation, most of the current is still carried by electrons. The major effects of hole injection are to reduce the series resistance of the n-layer and to increase the magnitude of recovered charge during turn-off [1], [2]. For these reasons high-voltage Schottky rectifiers (BV $\gtrsim$ 100V) tend to look more like p-i-n rectifiers than a Schottky. The junction vs. Schottky rectifier trade-off study of Page [3] does not take into account conductivity modulation, and it is probably worthwhile to re-examine some of the conclusions of this paper. For the device designs discussed here, conductivity modulation effects are generally negligible except for the larger values of φ_B at high junction temperatures.

Reverse Current

Figure 6 shows a plot of high-temperature leakage current for a device similar to that of Figure 5. The increase in leakage current with reverse voltage is due to "barrier lowering" or Schottky effect [4], in which the magnitude of $\Delta\varphi$ indicated in Figure 3 increases with V_R.

Barrier lowering effects can be greatly reduced by using an embedded grid of p-type regions under the Schottky to achieve the "pinch rectifier" proposed by Baliga [5]. Unfortunately the dimensions of these p-regions have to be rather small compared to W_n to avoid a severe increase in series resistance that penalizes high-current performance. This means p-regions with lateral metallurgical dimensions of about 1μm or less for the device designs being considered here. Dimensions in this range can be achieved by the more advanced microwave and VLSI technologies, but the cost of using such an approach should be weighed against the fact that the major benefit appears to be a reduction in high temperature leakage current by about two or threefold.

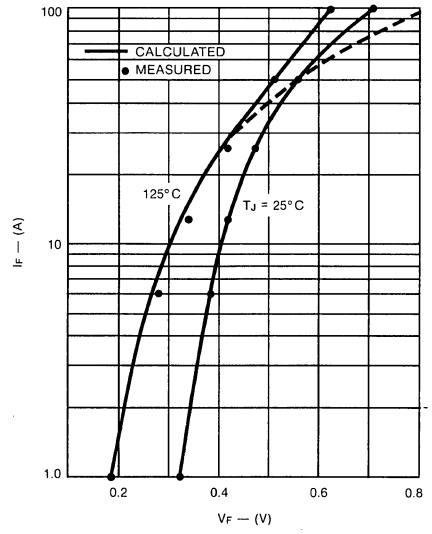

FIGURE 5. COMPARISON OF MEASURED AND CALCULATED FORWARD I-V CHARACTERISTICS FOR A USD545.

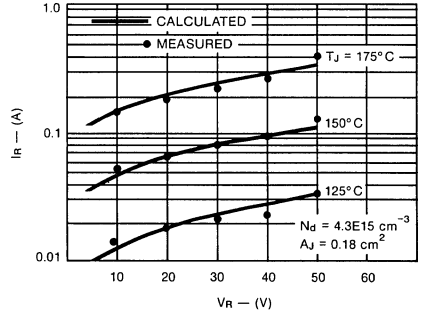

FIGURE 6. REVERSE I-V CHARACTERISTIC FOR A DEVICE SIMILAR TO THAT OF FIGURE 5. φ_B = 0.695V.

Thermal Instability

The major consequence of the temperature dependence of I_R is that the reverse power increases with T_J and at some point the combination of the device and its heat sink become thermally unstable. Some device data sheets reflect this situation by giving a $T_{J\,MAX}$ value, but this number can only approximate the onset of thermal instability.

One way to describe the problem is shown in Figure 7. Here the solid curves represent the power $I_R \cdot V_R$ which will be "generated" by the Schottky junction under reverse bias V_R. The waveforms of Figure 4 are assumed with negligible

forward power. The dashed curves are plots of (1) which gives the value of T_J that must occur if P_R is to flow through $R_{\theta JA}$ to some ambient temperature T_A.

If the system is to be stable, the heat sinking system must be capable of removing more power than the junction can generate. That is, the dashed curve must lie above the solid curve for some value of T_J. In the example shown, it can be seen that for a T_A of 75°C, there is no problem with thermal instability for a wide range of $R_{\theta JA}$ values.

The second set of dashed curves shows the situation when T_A is increased to 175°C, which is the T_{JMAX} for the USD545. In this case, $R_{\theta JA}$ must be less than 2°C/W if the system is to be stable. These curves correspond to a φ_B = 0.695V. If φ_B is decreased, for example, to reduce forward power losses, then the solid curves will shift upward. Over the temperature range shown, P_R will double for a decrease of about 22mV in φ_B. Thus if barrier height is to be used as a method of decreasing losses, more effective cooling methods must accompany this change. These tradeoffs are considered in more detail in the next section.

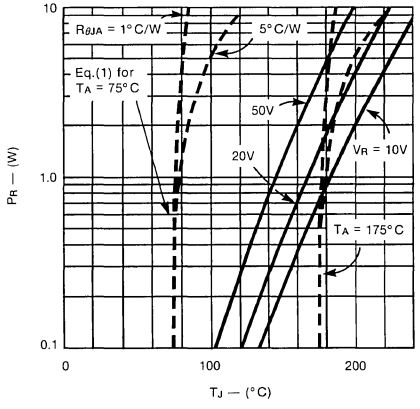

FIGURE 7. REVERSE POWER VS. JUNCTION TEMPERATURE FOR A USD545 (SOLID CURVES). T_J PREDICTED BY (1) FOR DIFFERENT CONDITIONS (DASHED CURVES).

POWER LOSS COMPARISONS

One way to see the benefits and penalties of various changes in the device design is to use the model to calculate total power losses under a variety of conditions. To be strictly correct, the influence of each of the five device variables should be examined separately; however, the problem is simplified by combining W_n, x_j, and N_d into a function which minimizes the series resistance for a given breakdown voltage. A slightly different procedure has been used to analyze a foward converter [6], but the results obtained are in general agreement with the method used here.

P_L vs. $R_{\theta JA}$ Curves

The results of this type of comparison are conveniently displayed as plots of total power lost P_L vs. $R_{\theta JA}$. Various combinations of device variables and input conditions are used to give an accurate picture of the tradeoffs involved.

For the first set of comparisons (Figures 8-13) the following conditions are used:

A_J = 0.176 cm^2, which is the same as for the USD545.

N_d = 1.4E16 cm^3, x_j = 1.1 μm, W_n = 1.9 μm, corresponding to a breakdown voltage (BV_1 of Figure 2) of 25V.

This value of breakdown voltage is approximately one-half that of the USD545. The ratio V_R to output voltage V_R/V_O, ignoring any inductive voltage spikes, is typically less than about 5 for a forward converter and 2.5 for a push-pull output. If we consider an output voltage of 2.5V, then a BV of 25V will provide a margin of at least 12V for any inductive spikes. Probably the BV could be reduced even further, and for this reason the tradeoff is considered later in Figure 14. In this connection it should be noted that the guard ring is capable of absorbing inductive spikes, but the corresponding power will contribute to the temperature rise of the Schottky.

Efficiency will depend on the output voltage being considered and can be calculated using

$$\text{Efficiency} = \frac{I \cdot V_O}{I \cdot V_O + 2 \cdot P_L} \quad (2)$$

Influence of Forward Current

The relation between power loss P_L and forward current is shown in Figure 8, where the waveforms of Figure 3 are assumed. P_L is approximately proportional to I_F, with the change being slightly greater than calculated from this rule due to an additional term which varies logarithmically with current. The slight negative slope of the curves in Figure 8 is due to the decrease in V_F that occurs as T_J increases. For each curve, P_L is calculated as $R_{\theta JA}$ is increased from zero. The plot is terminated when thermal instability is reached.

For the plots of Figures 9-13, I_F is fixed at 100A. Figure 8 can be used to extrapolate most of these results, at least up to the point where a minimum in P_L is reached.

It should also be noted that $R_{\theta JA}$ will always be greater than the junction-to-case thermal resistance $R_{\theta JC}$. For the USD545 which uses a DO-5 package, $R_{\theta JC}$ is about 0.7°C/W. Typical heat sinks are several times this value. If $R_{\theta JA}$ is to approach values less than 1°C/W, liquid cooling must be used.

Influence of T_A

Figures 9 and 10 show how P_L behaves vs. $R_{\theta JA}$ for different ambient temperatures. Points to the right of the minimum in P_L are stable, but there is no advantage in operating in this

range. These results show that for a given barrier height there will be a minimum power dissipation that can be achieved.

This minimum can be further reduced by decreasing φ_B as shown in Figure 10; however, ambient temperature must also be reduced significantly in order to avoid thermal instability. That is, approximately 6W could be saved, in this example, by going from a combination of T_A = 75°C/W, $R_{\theta JA}$ = 4°C/W (point 'a') to T_A = 25°C, $R_{\theta JA}$ = 1°C/W (point 'b'). The second pair of numbers would probably require liquid cooling, which is currently used in some mainframe computer designs.

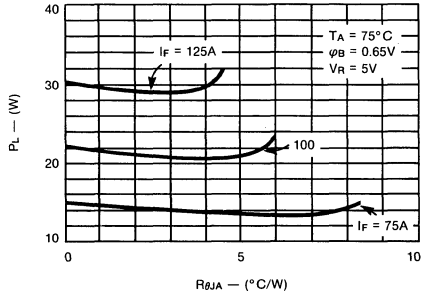

FIGURE 8. POWER LOSS VS. THERMAL RESISTANCE FOR DIFFERENT FORWARD CURRENTS. A_J = 0.176 cm^2.

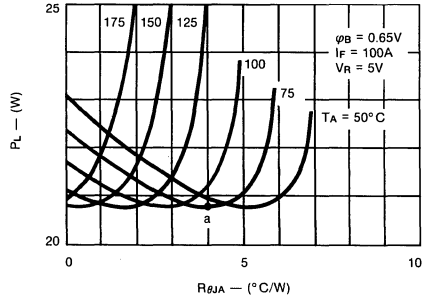

FIGURE 9. POWER LOSS VS. THERMAL RESISTANCE FOR DIFFERENT AMBIENT TEMPERATURES.

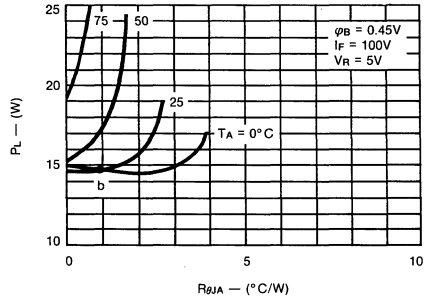

FIGURE 10. SIMILAR TO FIGURE 9, BUT FOR A LOWER BARRIER HEIGHT.

Influence of Barrier Height

Figures 11-13 show power loss curves with φ_B as the parameter for three different values of ambient temperature. These figures provide additional quantitative detail to the arguments advanced in connection with Figures 9 and 10.

Surface mount conditions represent extremes in the other direction. For example, Figure 13 shows that a T_A of 100°C and $R_{\theta JA}$ of 7°C/W can still be accommodated by a Schottky giving a respectable P_L of 21W provided φ_B is increased to 0.75V. In this case, increasing the barrier height is beneficial.

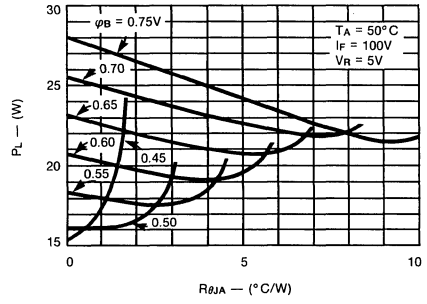

FIGURE 11. POWER LOSS VS. THERMAL RESISTANCE FOR DIFFERENT BARRIER HEIGHTS.

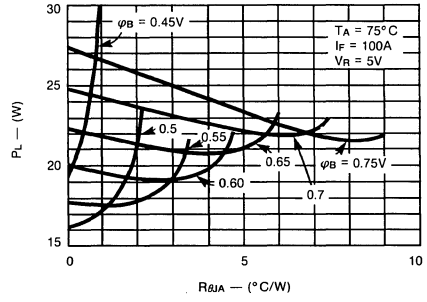

FIGURE 12. SIMILAR TO FIGURE 11, BUT FOR AN AMBIENT TEMPERATURE OF 75°C.

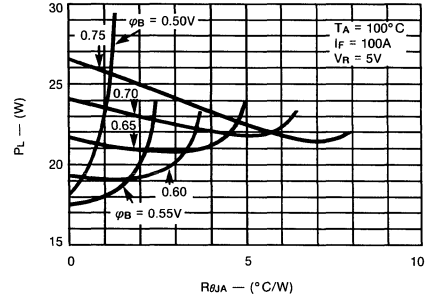

FIGURE 13. SIMILAR TO FIGURE 11, BUT FOR AN AMBIENT TEMPERATURE OF 100°C.

Influence of Breakdown Voltage

It is desirable to minimize the series resistance of the epitaxial layer by keeping the avalanche breakdown voltage BV small. Note that this BV is equivalent to the BV_1 defined in Figure 2. The effect of changing BV on power losses is shown in Figure 14. Two sets of conditions are assumed corresponding to "low" and "high" temperature designs. The device A_J is 0.176 cm^2, the same as the USD545.

For small values of BV, the series resistance of the substrate, backside contact, and package begin to dominate the total. For the USD545 size, these resistances add up to about 0.65 mohm which contributes 3.2W to P_L. As BV increases the epitaxial layer resistance becomes important and P_L shows a strong increase. For BV greater than about 50V, the P_L curves show only small increases. This is because N_d has decreased to a point where conductivity modulation of the n-layer reduces its effective series resistance.

The nominal BV of the USD545 is about 55V. If this is decreased to the 25 to 30V range, Figure 14 indicates that P_L is decreased by about 10W. This is a substantial savings in power dissipation. For the low temperature design, the decrease in P_L is even larger.

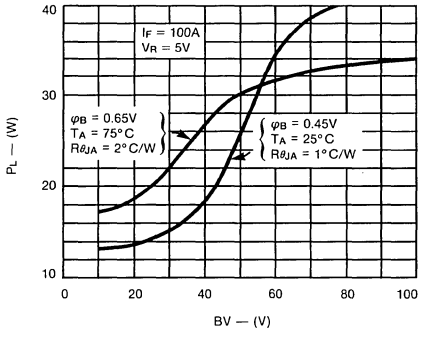

FIGURE 14. POWER LOSS VS. BREAKDOWN VOLTAGE FOR HIGH AND LOW TEMPERATURE DESIGNS.

Influence of Die Size

Increasing the die area will decrease the series resistance and also reduce the voltage drop accross the Schottky junction. Figure 15 shows how the power losses will decrease with increasing A_J. Note that the physical die dimension will be slightly larger than $\sqrt{A_J}$ to account for the guard ring diffusion and other "overhead" dimensions such as the width of saw streets.

Figure 15 shows that some decrease in power losses can be achieved by increasing die area. For small A_J, say less than 10mm^2, series resistance dominates and rather dramatic improvements can be made by increasing A_J. As A_J becomes comparable to the size of the USD545 (17.6mm^2), the V_F becomes dominated by the Schottky junction. For this situation the terminal V_F will change logarithmically with A_J, and an order of magnitude increase in A_J is needed to reduce V_F by 60mV at 25°C.

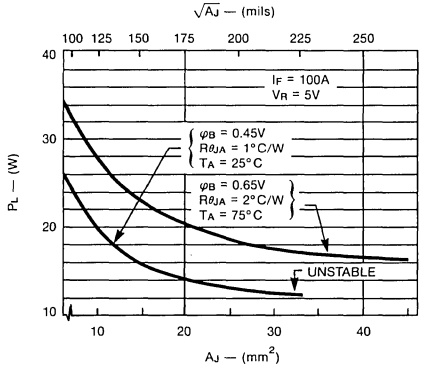

FIGURE 15. POWER LOSS VS. (SCHOTTKY) JUNCTION AREA FOR A HIGH AND LOW TEMPERATURE DESIGN.

LOW V_F DESIGN

Using the results of the analysis given in the previous section, we have developed a new Schottky rectifier which is currently in production. For this design, A_J is increased to 28mm^2, and BV is decreased to a nominal value of 30V. The power savings over the USD545 represent about a 30 to 40 percent decrease in power losses, depending on the forward current and other operating conditions.

Figure 16 shows the typical forward characteristic for the new design. As one might expect, there is little influence of conductivity modulation.

The difference in P_L values comparing the new design with the USD545 is the power saved ΔP. A plot of ΔP vs. forward current is shown in Figure 17. As defined here, ΔP is per device and therefore the total power saved in the output rectifier circuit will be $2\Delta P$. For the plot of Figure 17, V_R is 5V, and two values of thermal resistance have been assumed.

It can be seen that the curve increases more strongly than linearly with I_F which indicates that the series resistance is important. At large values of I_F, reverse power becomes important and the curve tends to bend over as shown.

DISCUSSION

Although the Schottky rectifier has many strong points for low-voltage output applications, other approaches are of interest. For example, MOSFET synchronous rectifiers have received a great deal of attention in the technical literature. More recently it has been demonstrated that a bipolar transistor may be a better choice for this application [7].

The possibility of using germanium rectifiers should also be considered (8). Low V_F junction diodes are possible in this material, but it is more limited in temperature and has lower breakdown fields than for silicon. The comparison of this type of rectifier with a silicon Schottky is an interesting topic which deserves further study.

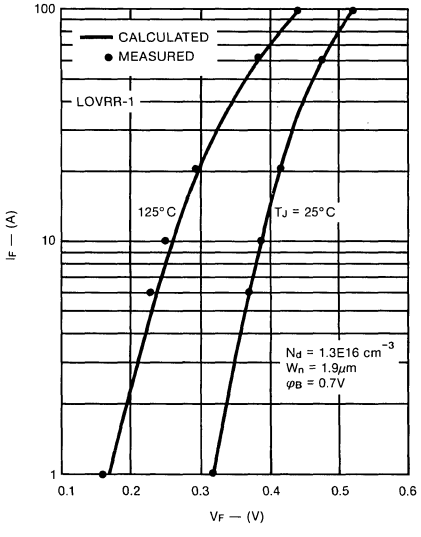

FIGURE 16. FORWARD I-V CHARACTERISTIC FOR A NEW LOW V_F DESIGN.

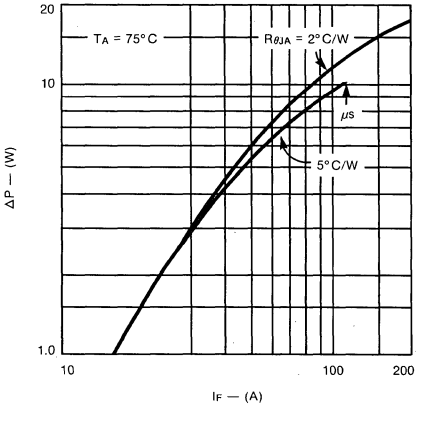

FIGURE 17. POWER SAVED (PER DEVICE) COMPARING A USD545 VS. THE NEW DESIGN.

Comparison with Bipolar Synchronous Rectifiers

Synchronous rectifiers are of interest because their I-V characteristic is linear down to zero volts, unlike the Schottky or p-n junction which have an apparent "offset" voltage. Offsetting this advantage is the need for a more complicated circuit, including additional components and transformer windings. The UBS430 BISYN™ bipolar transistor has a relatively low on-resistance of about 7mΩ, which is the smallest value obtainable for any commercial device in a TO-3 package. This resistance is still relatively large when compared with the series resistance of a Schottky, which is typically in the range of 1 to 2mΩ.

This means that the BISYN will have smaller power losses up to some current which is approximately equal to I_X, the current where the forward characteristics intersect (7). For the UBS430, I_X is in the range of 40 to 60A.

Figure 18 shows a plot of ΔP (per device), where the bipolar is compared against two different Schottky rectifiers, the USD545, and the new lower BV design described in this paper. The curves reach a peak at approximately $I_X/2$. As noted previously, the total power saved in the output circuit is 2ΔP.

Our view is that the present BISYN designs offer a useful alternative for currents less than approximately 30A, but it will take a new packaging approach to bring the synchronous rectifier to the point where it can compete with the Schottky at currents in the 60 to 200A range.

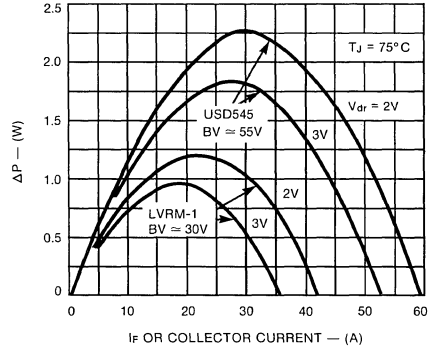

FIGURE 18. POWER SAVED (PER DEVICE) COMPARING THE UBS430 BISYN™ BIPOLAR WITH A USD545 AND THE NEW LOW V_F SCHOTTKY.

CONCLUSION

The new Schottky rectifier design described in this paper represents the next logical extension that can be made from the present designs. Power loss savings are in the 30 to 40 percent range. Other alternatives for decreasing power losses require a new choice for barrier material and the accompanying considerations of cooling requirements. Attainable reductions in power losses have been estimated. With these results it is believed that device users will be able to determine various benefits and penalties as they consider new circuit applications.

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DETERMINING THE CHANGE IN ZENER VOLTAGE WHEN THE CURRENT IS CHANGED

A common question concerning zener diodes is "what will be the zener voltage at a current different from the current now specified?"

The difficulty is that the impedance of a zener is not a constant, and changes with the current, so the zener voltage is a non-linear function of current.

Here is a useful equation that gives a good approximation to the change in zener voltage when the current is changed from one value to another value.

$$\Delta V_Z \doteq k_Z \ln\left(\frac{I_2}{I_1}\right)$$

where $k_Z = I_Z \times Z_Z$ and I_Z is chosen approximately midway between I_1 and I_2

The equation does not include the effect of pulse or dc-heating on the zener voltage. If appreciable junction heating is involved the thermal model must also be used.

Here is an example of how the equation is used.

Question: If the voltage of a UZ5733 is specified as 33V at 40mA, what will be its voltage when measured at 5mA?

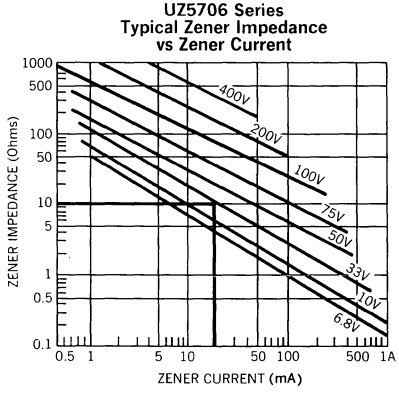
Using the graph of Z_Z versus I_Z on the data sheet for this device, and choosing a value of I_Z at 20mA,

$Z_Z = 10\Omega$

So $k_Z = I_Z \times Z_Z = 20\text{mA} \times 10\Omega = 0.20\text{V}$

$$\Delta V_Z \doteq k_Z \ln\left(\frac{I_2}{I_1}\right) = 0.20 \times \ln\left(\frac{5\text{mA}}{40\text{mA}}\right) = 0.20 \times \ln(0.125) = 0.20\text{V}\ (-2.08) = -0.42\text{V}$$

Thus the zener voltage at 5mA will be 33V — 0.42V = 32.6V



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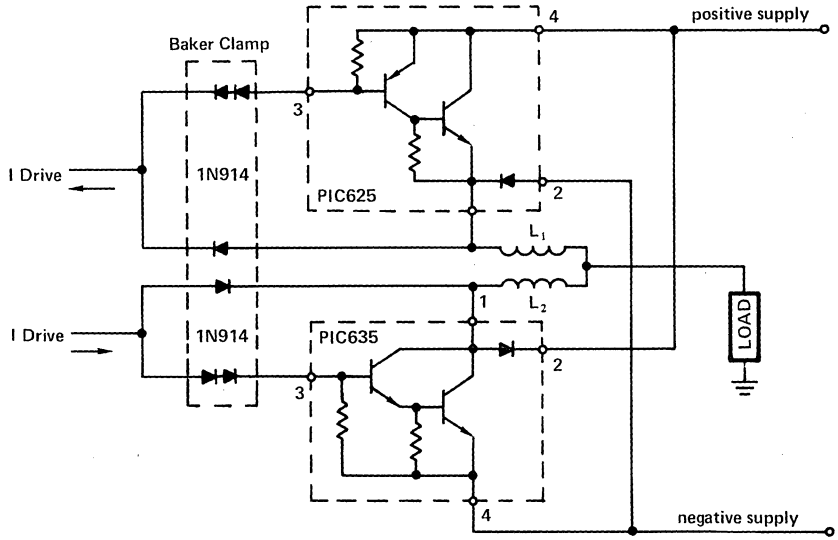
MINIMIZING STORAGE TIME WHEN USING UNITRODE SWITCHING REGULATOR POWER OUTPUT CIRCUITS (PIC600 SERIES)

In some applications (such as a reversing motor drive, for example: stepper motor) where storage time is an important consideration in the design, the normal storage time of PIC600 series (approximately 600ns) can be reduced to acceptable level.

At lower output currents, the excess storage time is a result of the driver stage operating well under saturation, while at higher output currents it is a result of the output transistor operating into quasi-saturation region.

The storage time can be reduced to less than 100ns by utilizing a Baker Clamp technique as shown in the circuit below:



The Baker Clamp will increase the $V_{CE(sat)}$ losses but this disadvantage will be more than offset by the improved switching speed.

The Baker Clamp circuit varies the drive current of the PIC600 series for optimum switching speed at any given load current. The drive current required to the Baker Clamp can be unregulated, as long as it is greater than 30mA.

The small value of the inductor L_1 and L_2 (5 to 10 μH) stops cross conduction during the switching of PIC600 series.

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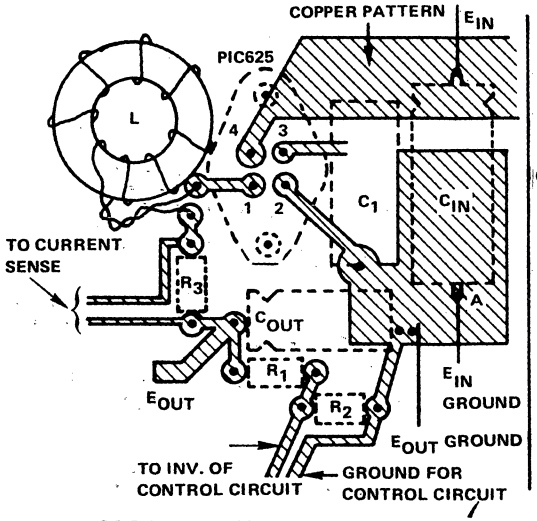
AVOIDING SPURIOUS OSCILLATION WHEN USING UNITRODE SWITCHING REGULATOR POWER OUTPUT CIRCUITS (PIC600 SERIES)

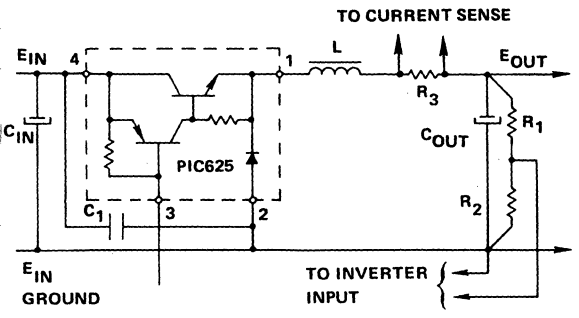
Avoid spurious oscillation due to ground loops and RFI when using a Unitrode Switching Regulator Power Output Circuit (PIC600 Series) in a switching regulator.

The Unitrode switching regulator power output stage (PIC600 Series) is a high frequency fast switching device. Its control circuitry must also operate at high frequency and high gain. Therefore, it is necessary to avoid any ground loops and RFI for stable circuit operation.

The high frequency roll-off of the control circuit should be adjusted properly with a compensation network. The typical layout of the power circuit is shown in the figure below.



PC BOARD LAYOUT OF POWER CIRCUIT



CIRCUIT DIAGRAM

Capacitor C_1 (0.2 μf) reduces the RFI generated due to the reverse recovery current spike of the catch diode, and should be physically located near pin 4 and pin 2 of the PIC625. The capacitor should be a high frequency by-pass capacitor, such as Polystyrene.

The current sense resistor R_3 should be a non-inductive (carbon) type. The current sense signal should be picked up right across this resistor.

If the switching regulator is operated at the higher end of the input voltage, the inductor should be shielded with an electrostatic shield, grounded to Point A. The case of PIC625 should also be connected to Point A.

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OPERATING THE SWITCHING REGULATOR OUTPUT CIRCUIT (PIC600 SERIES) AT LOW FREQUENCIES

The Unitrode switching regulator power output circuit consists basically of a power transistor switch and a catch diode. The appropriate data sheets in the Unitrode Semiconductor Databook provide the necessary information for determining junction temperature and power dissipation at frequencies above 10 kHz.

This Design Note provides a method for determining the junction temperature and maximum allowable power dissipation for the transistor switch and catch diode when the switching regulator is operated at frequencies under 10 kHz, where the switching losses are negligible and can be safely ignored.

The method of determining safe power dissipation requires a detailed transient thermal analysis, since the junctions of the transistor and diode are subjected to temperature excursions due to the applied pulse power.

When the device is subjected to a train of periodical power pulses, the maximum power dissipation and junction temperature can be calculated from the effective pulse thermal resistance (θ_p) as follows:

$$\theta_p = R_T \times D + (1-D)\, r(t + \tau) - r(\tau) + r(t)$$

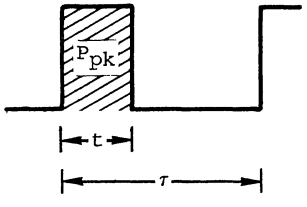

Figure 1. Power Pulses

where: t = pulse width

τ = period

Duty cycle $D = \frac{t}{\tau}$

Peak Power, P_{pk} is peak of an equivalent square power pulse

$r(t + \tau)$ = transient resistance at time $t + \tau$

$r(t)$ = transient thermal resistance at time t

R_T = DC thermal resistance (from data sheets)

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1. Calculating the Junction Temperatures (Pulse Train)

A. Power Transistor Switch

The peak junction temperature of the transistor switch under repetitive peak power pulse conditions is calculated as follows:

$$T_{j(peak)} = T_{CASE} + P_{pk} \times \theta_p$$

$$T_{j(peak)} = T_{CASE} + V_{CE} \times I_C \times \left[R_T \frac{t_T}{\tau} + \left(1 - \frac{t_T}{\tau} \right) \times r(t_T + \tau) - r(\tau) + r(t_T) \right]$$

The transient thermal impedances $r(t_T + \tau)$, $r(\tau)$, $r(t_T)$ are obtained from the transient thermal impedance plot for the transistor (see Figure 2),

t_T = transistor on-time

B. Catch Diode

The peak junction temperature of the catch diode under repetitive peak power pulse condition is calculated as follows:

$$T_{j(peak)} = T_{CASE} + I_F \times V_F \left[R_T \times \frac{t_D}{\tau} + \left(1 - \frac{t_D}{\tau} \right) r(t_D + \tau) - r(\tau) + r(t_D) \right]$$

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where:

t_D = diode on-time

The Transient thermal impedances $r(t_D + \tau)$, $r(\tau)$, $r(t_D)$, are obtained from the transient thermal impedance plot for the catch diode (see Figure 2).

C. Power Dissipation

The maximum allowable power dissipation in either the transistor or the diode is determined by the maximum junction temperature of 150°C:

$$P_{pk(max)} = \frac{150°C - T_{CASE}}{\theta_p}$$

2. Calculating the Junction Temperature (Single Shot Power Pulse)

For a non-repetitive power pulse, the rise of junction temperature can be calculated as follows:

$$T_j = P_{pk} \times r(t) + T_{CASE}$$

For a pulse with less than 100 millisec, the case temperature is assumed to remain at ambient temperature.

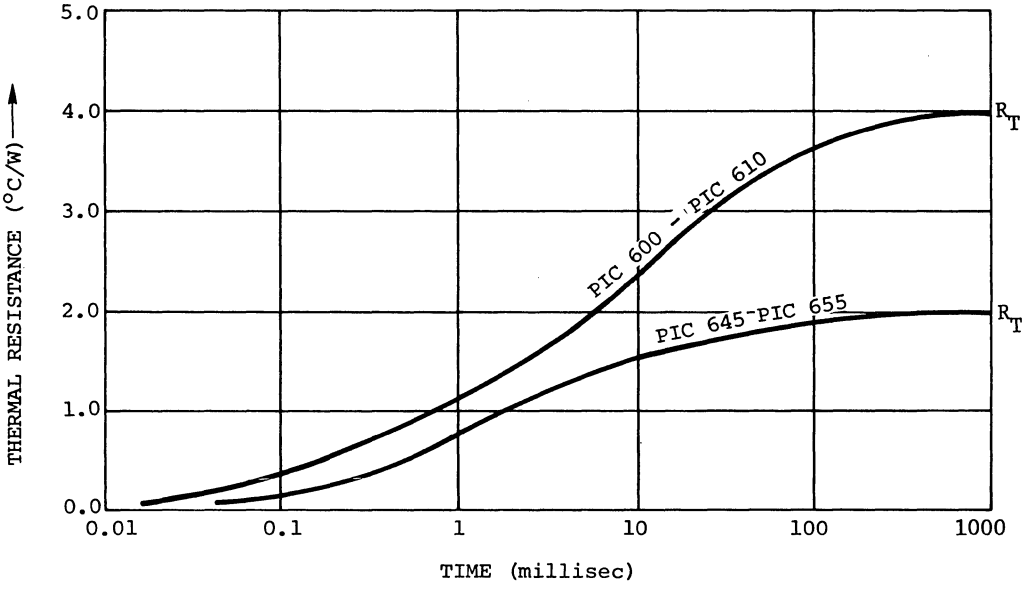

Figure 2. Transient Thermal Resistance — Power Transistor or Catch Diode

SQUIB-FIRING CIRCUIT PROVIDES FOR RELIABLE FIRING, FROM LOW LEVEL INPUTS

The design of reliable squib-firing circuitry often presents particular problems. Squib functions are typically quite critical, and the initial triggering source for these systems is, by nature, usually minute.

Conventional transistor squib-firing circuits usually require several gain stages, together with a power transistor to handle the squib-firing current. Mechanical squib switches, on the other hand, cannot be operated repetitively to allow for complete testing of the device and associated circuitry during check-out.

The high sensitivity planar Silicon Controlled Rectifier (SCR) can be triggered directly from low-level input circuitry, with significant reduction in circuit complexity and size. Reliability is thus considerably enhanced.

The unique characteristics of the planar SCR have resulted in wide usage of this semiconductor component in squib-firing circuits for rocket engine ignition, detonation, and explosive bolt applications. Compared with conventional transistor techniques or mechanical squib switches, this proven approach has significant reliability advantages, with circuit simplicity, size reduction, mechanical ruggedness and elimination of electrical contacts.

An SCR, with surge current ratings at 100 °C of 5 amperes-50 milliseconds or 20 amperes-1 millisecond can easily handle the current required for firing most squibs. Input circuits can be designed to trigger reliably at levels below 100 microamperes and 1.0 Volt, making the SCR particularly well-suited for direct drive from low level control logic circuits and simple RC time delay networks. In addition, the bistable properties of the SCR enable it to be triggered on by a pulse input—remaining in the "ON" state until reset. This inherent "memory" is frequently used to advantage in arming circuits.

Two circuits typical of squib firing applications are shown in Figures 1 and 2. Both will operate from −65 °C to over 125 °C.

In Figure 1, Capacitor C_1 is charged to +28 Volts through R_1 and stores energy for firing the squib. A positive pulse of 1 mA applied to the gate of SCR_1 will cause it to conduct, discharging C_1 into the squib load X_1. With the load in the cathode circuit, the cathode rises immediately to +28 Volts as soon as the SCR is triggered on. Diode D_1 decouples the gate from the gate trigger source, allowing the gate to rise in potential along with the cathode so that the negative gate-to-cathode voltage rating is not exceeded. This circuit will reset itself after test firing, since the available current through R_1 is less than the holding current of the SCR. After C_1 has been discharged, the SCR automatically turns off—allowing C_1 to recharge.

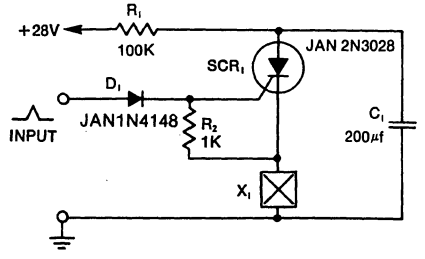

FIGURE 1

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In Figure 2, energy for firing the squib is supplied directly from the +28 Volt supply. Caution must be exercised when arming this type of circuit. If anode voltage is applied too rapidly, the SCR may fire. This dv/dt effect acts through the SCR anode-gate capacitance (15 pf), which couples current to the SCR gate (in proportion to anode dv/dt). The effect is negligible if dv/dt is under 1 Volt/μs—as in Figure 1, where it is limited by the charging of C_1. Faster rates of rise can be safely handled by increasing the SCR gate bias.

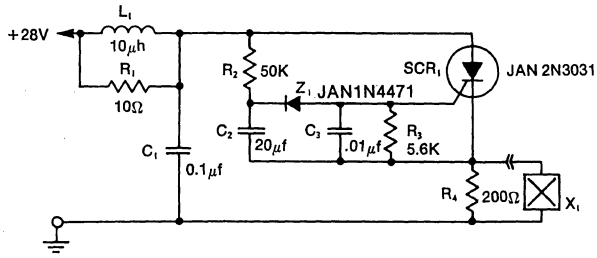

FIGURE 2

In Figure 2, the LRC input network limits the anode dv/dt to a safe value—below 30 Volts/μs. R_1 provides critical damping to prevent voltage overshoot. While a simple RC filter section could be used, the high current required by the squib would dictate a small value of resistance and a much larger capacitor. Resistor R_3 provides DC bias stabilization, while C_3 provides stiff gate bias during the transient interval when anode voltage is applied.

In this circuit the SCR is fired one second after arming by means of the simple R_2 C_2 Z_1 time delay network. R_4 provides a load for the SCR for testing the circuit with the squib disconnected—limiting the current to a level well within the continuous rating of the SCR. The circuit can be reset by opening the +28 Volt supply and then re-arming.

NANOSECOND SCR SWITCH FOR RELIABLE HIGH CURRENT PULSE GENERATORS AND MODULATORS

The design of reliable modulator and pulse generator circuitry often presents the design engineer with seemingly conflicting requirements. In order to obtain fast rise times, "hard tubes" or hydrogen thyratrons are often used. This results in a large system which consumes considerable power and has relatively low conversion efficiency. Reliability, jitter, and stability are also common problems in these systems.

To improve reliability, as well as decrease standby power consumption and improve conversion efficiency, semiconductor devices are a natural choice. However, at the voltage and current levels most often encountered in these applications, conventional semiconductors are usually too slow.

The nanosecond SCR switch developed by Unitrode allows the designer to upgrade high current, high voltage modulator and pulse generator circuitry. A single device (GA201 or GA301*) is capable of operating in circuits with supply voltages up to 100 Volts DC and pulsed load currents in excess of 50 Amperes. It can be triggered directly from logic level signals (1 Volt, 200 microamps) and exhibits a rise time of less than 10 nanoseconds to 1 Ampere with only 10 milliamps of drive signal. Single switches operated in this mode can be used as high current replacements for avalanche transistors, modulators, and harmonic wave form generators.

Special circuity has been developed to apply these nanosecond switches in applications where supply voltages exceed the forward blocking capability of a single device. The simplest of these is shown in Figure 1.

The 1 meg-ohm resistors act as a voltage-sharing network to insure that no single device is overvoltaged because of unequal leakage currents. Turn-on is accomplished by applying a trigger signal to the primary of the pulse transformer, T1. The capacitor, which has been charged to the supply voltage through R_C, discharges through R_L, and the string of SCRs. This circuit is useful until the number of stages used requires a pulse transformer that becomes objectionably bulky. Beyond that point the circuit of Figure 2 or 3 is used.

Figure 2 illustrates an approach that uses a pulse transformer to trigger only part of the string, while the rest of the devices in the string are supplied with gate drive through the zener diodes. With a supply voltage of 360 Volts DC, a 95 Volt ±5% zener diode across each SCR in the string prevents unequal voltage distribution. When SCR_3 and SCR_4 are triggered, 360 Volts appear across SCR_1 and SCR_2 causing zener diodes Z_1 and Z_2 to conduct. Since D_1 and D_2 are back-biased, the current must flow through the gate-to-cathode junctions of SCR_1 and SCR_2, thus driving them on. Up to eight stages can be stacked in this manner using a pulse transformer to drive only the bottom two SCRs in the string. Driving three SCRs with a pulse transformer allows stacking sixteen stages, which can switch a 1440 Volt load using a pulse transformer that needs to have a dielectric isolation rating of less than 300 Volts.

Figure 3 uses no pulse transformer and can be extended to virtually any number of stages. When SCR_1 is triggered, the cathode of SCR_2 drops from +100 to essentially 0 Volts. Capacitor C_1 discharges into the gate of SCR_2 causing it to conduct, and this process is repeated for SCR_3 and SCR_4. This circuit has the added feature of providing negative bias to the SCRs during recharge of the load in order to minimize the effect of dv/dt. As the voltage rises on the anode of SCR_4, current flows through the path consisting of C_4, R_4, C_3, R_3, C_2, R_2, etc. This provides negative bias for the gate-to-cathode junctions of the SCR in the string, making them less sensitive to dv/dt triggering. This allows the use of rapid recharge circuits which permits operation at higher repetition rates. Either resonant recharge or active (SCR) rapid recharge techniques may be used with these circuits.

*GA201 recommended for military, GA301 for commercial applications.

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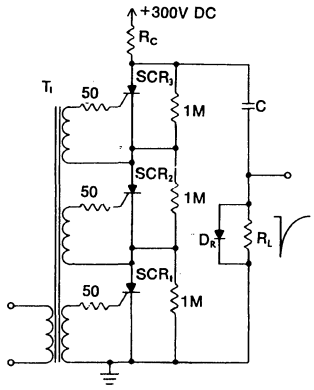

FIGURE 1

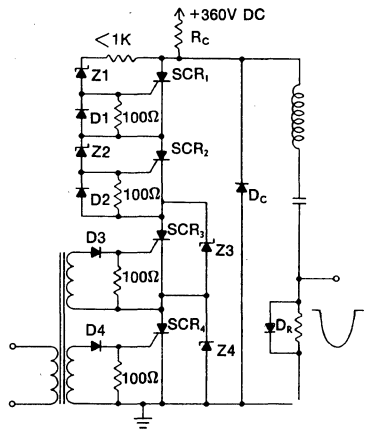

FIGURE 2

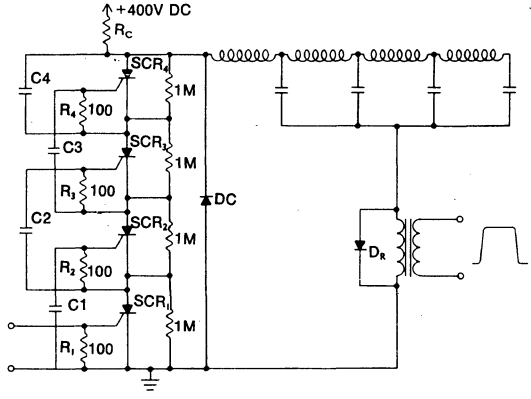

FIGURE 3

If the energy storage element(s) and load consist only of R and C components, the charging resistor must be large enough to limit the DC current to a value less than the minimum holding current of the SCRs in the string. When the load contains an inductive component, as is usually the case in modulator circuits, the network can be designed to "ring" in order to reverse-bias the SCR string momentarily, permitting the SCRs to regain their forward blocking capability even though R_C allows more than the minimum holding current to flow. Diode D_R may be used in all circuits so that the recharge current will not flow through the output element. In Figures 2 and 3, D_R shunts the reverse "ringing" current around the output element. Diode D_C must be used in circuits that contain inductive elements to protect the string from being excessively back-biased due to circuit ringing.

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NANOSECOND SCR FOR LASER DIODE PULSE DRIVER

The use of pulsed gallium-arsenide lasers requires a reliable high speed, high current switch to drive these devices. In the past the only solid state devices that could be used in this application were avalanche transistors and fast medium power transistors. Avalanche transistors presented reliability problems, while the standard medium power transistors available were too slow. The GA200 series "Nanosecond SCR" with a rise time capability of 10 nsec to 1 Amp or 20 nsec to 30 Amps provides a solution to both the reliability and the speed problems and appears to be ideal for this type of application.

The circuit shown in Figure 1 utilizes a GA201 device along with a lumped constant delay line to generate the desired square current pulse. For simplicity, a single capacitor could be used instead of the delay line. The delay line, however, has the advantage of producing a square pulse that provides sharp turn-off, which limits the excess power dissipation that would occur in the laser diode if the pulse fell exponentially. The impedance of the delay line ($= \sqrt{L/C}$) is chosen to produce a slight mismatch, which produces overshoot on the trailing edge of the pulse. This overshoot acts as a reverse bias on the anode of the SCR, assisting in turning it off. A typical value for the delay line impedance would be 1 to 2 ohms, which approximates the impedance of the load formed by the SCR and laser diode in series. The time duration of the pulse ($= \sqrt{L/C}$ per section) can be made as short as desired with a value of 50 to 100 nsec being typical.

With the SCR in the off state, the delay line will charge to the supply voltage (100 Volts with GA201). A gate current at the input of as little as 200 μA will trigger the SCR. The delay line will then discharge, producing a square current pulse through the gallium-arsenide laser diode. R_1 and R_{GK} are chosen so that the current, after the delay line discharges, will be less than the holding current of the GA201 ($= 3$ mA with $R_{GK} = 100$ ohms.) C_1 should be about .001μf and is necessary to prevent false triggering through noise or through dv/dt commutation. D_2 provides a charging path for the delay line, while $R_2 \cong 50K$ provides a stable ground reference. Diode D_3 insures that the reverse breakover voltage of the GA201 will not be exceeded during the turn-off period.

The forward current level will depend upon the total impedance of the GA201 and the laser diode and the charging voltage used. With a 100 Volt device and a practical minimum circuit impedance of about 1 ohm, it is possible to develop peak currents of up to 100 Amps. (See Figure 2 for Time vs Current curve for GA200/GB200 Series.) Pulse of 60 Amps with rise times of approximately 30 nsec have actually been achieved. For improved performance at high current levels, the SCRs may be operated in parallel or in series. Parallel operation is achieved by providing equal series resistors to the gates of the devices and driving them from the same source. By overdriving the gates with 50 to 100 mA, simultaneous turn-on is guaranteed. Parallel operation results in lower forward voltage drop and faster rise time at high current levels. Series stringing techniques can be used in circuits with a higher total impedance where higher voltages are needed to obtain the desired current levels. For a description of series operation see Design Note 14.

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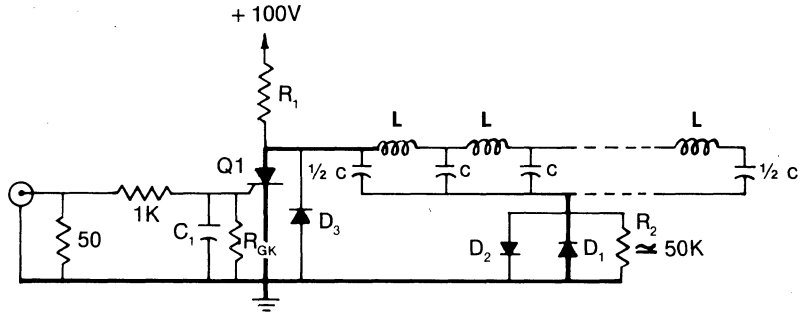


Q1—GA201/GB201, GA301/GB301

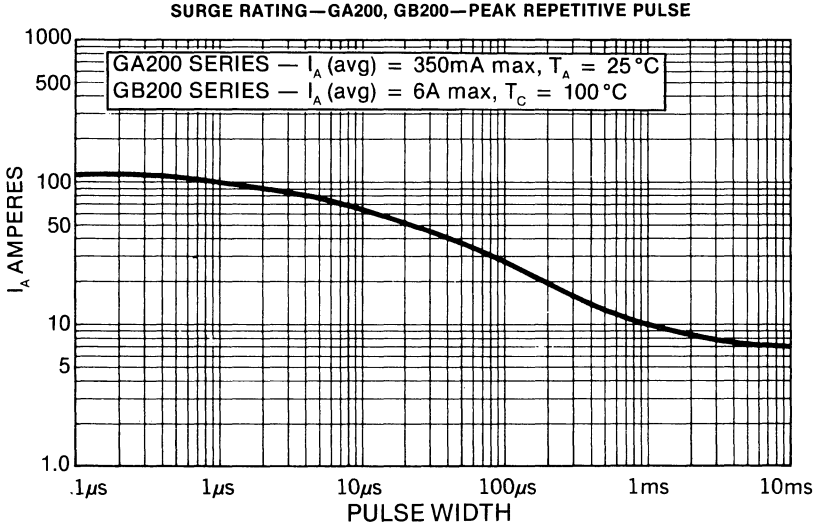
D_1 —Gallium-Arsenide Laser Diode

D_2 —JAN 1N5802 or 1N5807* (Alternative: UES1101 or UES1301)

D_3 —JAN 1N5804 or 1N5809* (Alternative: UES1102 or UES1302)

Note: Heavy lines indicate braided connections for reduced inductance and resistance.

Figure 1



Note: For MIL and high Rel series applications, use GA/GB 200/201 and JAN Diodes.

For high rep rate (high average current), use GB series with 1N5809 or UES1302 rectifiers.

GA300 and UES series are intended for commercial applications.

Figure 2

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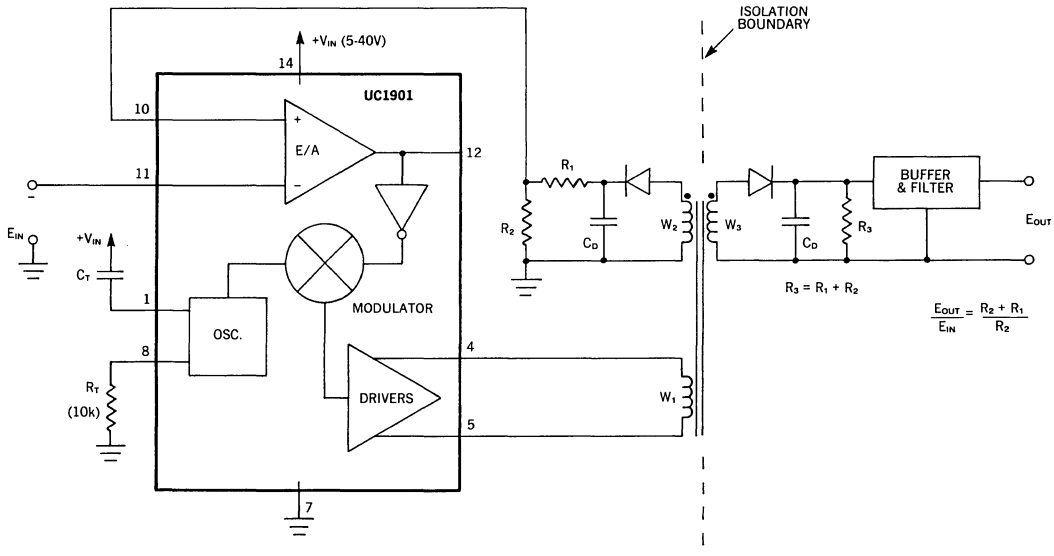
A SIMPLE ISOLATION AMPLIFIER USING THE UC1901

The UC1901 Isolated Feedback Generator has other applications besides providing isolated feedback in switching power supplies. This IC's amplitude modulation system and error amplifier can be used to implement a very low cost, high bandwidth, isolation amplifier. Isolation amplifiers of this type find use in switching power supplies, motor controls, instrumentation, industrial controls and medical systems.

The UC1901 generates a programmable high frequency carrier signal (up to 5MHz) with an amplitude that is controlled by a high gain error amplifier. In a typical feedback application, this amplifier and modulator are used, in conjunction with the UC1901's 1.5V reference and a small signal coupling transformer, to provide precision regulation for an isolated switching power supply. Capacitively coupled feedback around the UC1901 error amplifier determines the device's small signal AC response, but the DC operating point is determined by the requirements of the overall power supply loop. By adding an additional winding on the coupling transformer and a demodulator circuit for this winding, local DC feedback can be provided to the UC1901's error amplifier. In this mode very accurate DC, as well as small signal AC, transfer functions can be established across the isolation boundary.



A Low Cost, High Bandwidth, Isolation Amplifier: An additional feedback winding linearizes the transfer function of the amplifier by matching the coupling characteristics to the isolated output.

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The configuration of an isolation amplifier using the UC1901 is shown in the figure below. The drivers on the UC1901 couple an amplitude modulated carrier to two matched windings (W_2 and W_3) on a small signal transformer. The demodulated signal from winding W_2 is used to provide feedback to the UC1901's error amplifier while the demodulated signal from W_3 is the isolated output signal. The use of the feedback winding linearizes the transfer function of the overall amplifier and allows DC signals to be accurately transferred. Matching of the two demodulator windings and demodulator circuits is important to maximize linearity and minimize DC offsets. An optional output buffer and filter will reduce residual carrier ripple and isolate the output demodulator from its load. The internal gain compensation on the UC1901 is sufficient for stable operation with overall gains down to 12dB. This circuit requires a supply voltage to the UC1901 that, if not available in the system already, can be generated using a second similar circuit operating in the reverse direction.

The primary features of this circuit are:

1. Good Signal Linearity
2. Wide Bandwidth (3dB Bandwidths > 500kHz)
3. High Isolation Capability
4. Low Cost

NEW HIGH EFFICIENCY CIRCUIT DESIGNS UTILIZING LOW SATURATION DROP TRANSISTOR

The new UBT430 transistor with $V_{CE(sat)}$ drops of .10V at 10A, 3V at 3A gives the circuit design engineer the opportunity to develop new circuits with greatly enhanced efficiency. This design note describes some of these circuits in detail.

High Efficiency Battery Back-up System

The circuit shown in Figure 1 is a high efficiency battery back-up system. Since the UBT430 has low saturation drop (with a high gain) the power dissipation in the control switch circuit is reduced by 40-50% when compared with low forward drop of a Schottky rectifier.

The voltage sense circuit monitors the line voltage and output voltage. When the voltage drops below a pre-determined value, transistor Q_2 turns on and drives the control switch Q_1. At an output current of 20A, the power dissipation in the transistor switch Q_1 is only 3W while an equivalent Schottky rectifier will dissipate about 8.6W.

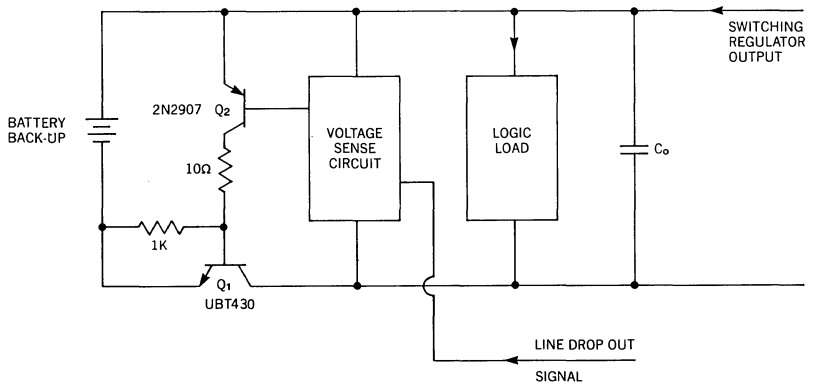

FIGURE 1. HIGH EFFICIENCY BATTERY BACK-UP SYSTEM

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Current-Mode Controlled 50W High Efficiency Switching Regulator

The circuit shown in Figure 2 is a low cost, current-mode controlled 50W, high efficiency switching regulator. This circuit utilizes the 8 Pin UC3843 current-mode control chip. The totem-pole output of the UC3843 delivers 250mA of drive current to output switch Q_2.
switch 10A with a $V_{CE(sat)}$ of less than 80mV. The fast turn-off times (<400ns) are achieved through a speed-up capacitor C_4. With a 5V output an efficiency of better than 80% can be realized. The UC3843 is designed for low voltage applications with an under-voltage lockout feature. The use of current-mode control removes one of the poles from the control loop making loop compensation easier. Current-mode control also provides small signal voltage feed forward characteristics, which reduces the gain requirement of the error amplifier.

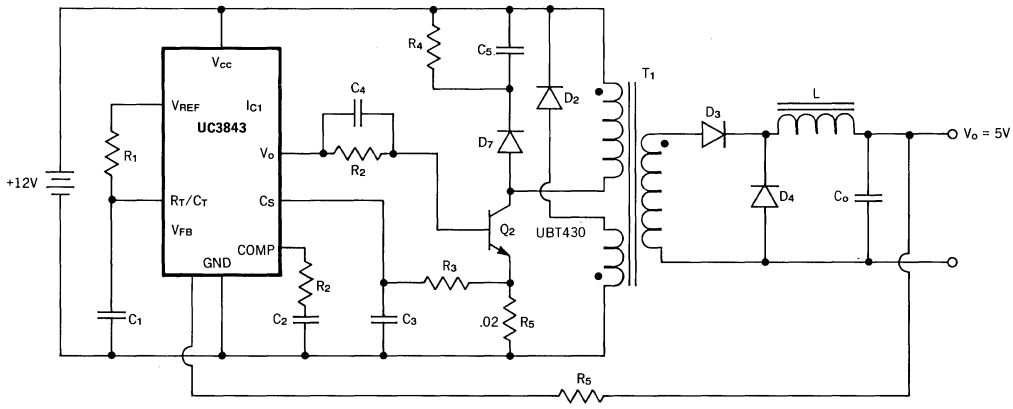

FIGURE 2. CURRENT-MODE CONTROLLED 50W HIGH EFFICIENCY SWITCHING REGULATOR

High Efficiency Emitter Control Switch

The circuit shown in Figure 3 is an emitter controlled switch. Transistor Q_2 (UBT430) is controlled with a totem-pole output switch of control chip UC3843. The power loss in the emitter control switch is an order of magnitude less than high voltage switch Q_1. The turn-off time of high voltage switch Q_1 is extremely fast because the negative base drive current is equal to collector current. The zener diode D_2 clamps the voltage across the base and provides a path for negative base drive current. The initial turn-on current is delivered from capacitors C_1 and C_2 and then is supplemented by winding N_2 through resistor R_2.

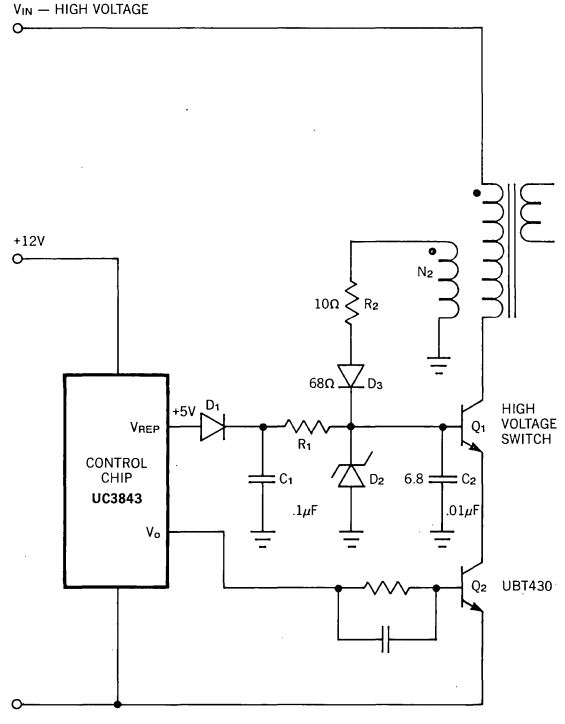

FIGURE 3. EMITTER CONTROL SWITCH

250 WATT OFF-LINE FORWARD CONVERTER DESIGN REVIEW

by

Raoji Patel

This paper gives a practical example of the design of an off-line switching power supply with forward converter topology. Topics include transformer and filter inductor design, proportional base drive, component selection, output filter design, and closing the control loop using the new Unitrode UC1524A control circuit.

POWER SUPPLY SPECIFICATIONS:

TOPOLOGY:	Forward Converter with Proportional Base Drive	
LINE INPUT:	117 Volts +/- 15% (99-135V), 60Hz	
	230 Volts +/- 15% (195-265V), 50Hz	
OUTPUT:	Voltage:	5 Volts
	Current:	5 to 50 Amperes
	Current Limit:	60 Amperes Short Circuit
	Ripple Voltage:	100mV p-p maximum
	Line Regulation:	+/- 1%
	Load Regulation:	+/- 1%
OTHER FEATURES:	Efficiency:	75%
	Line Isolation:	3750 Volts
	Switching Frequency:	40KHz

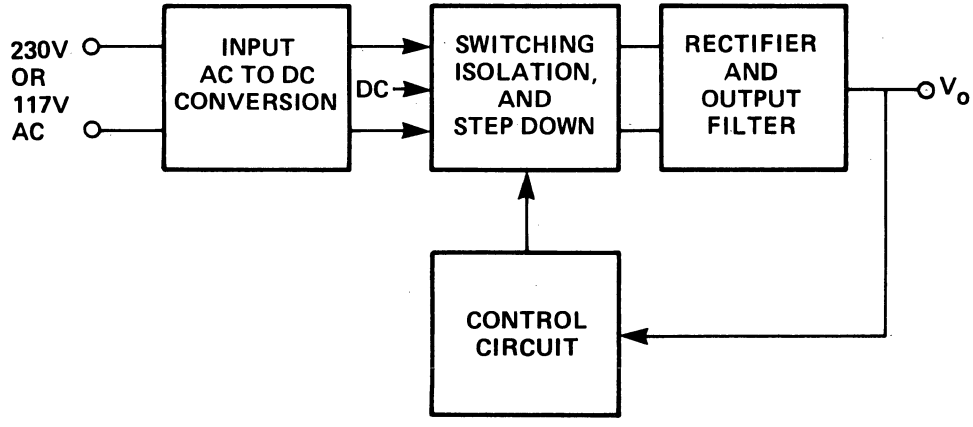

Figure 1. Block Diagram of the Switching Power Supply

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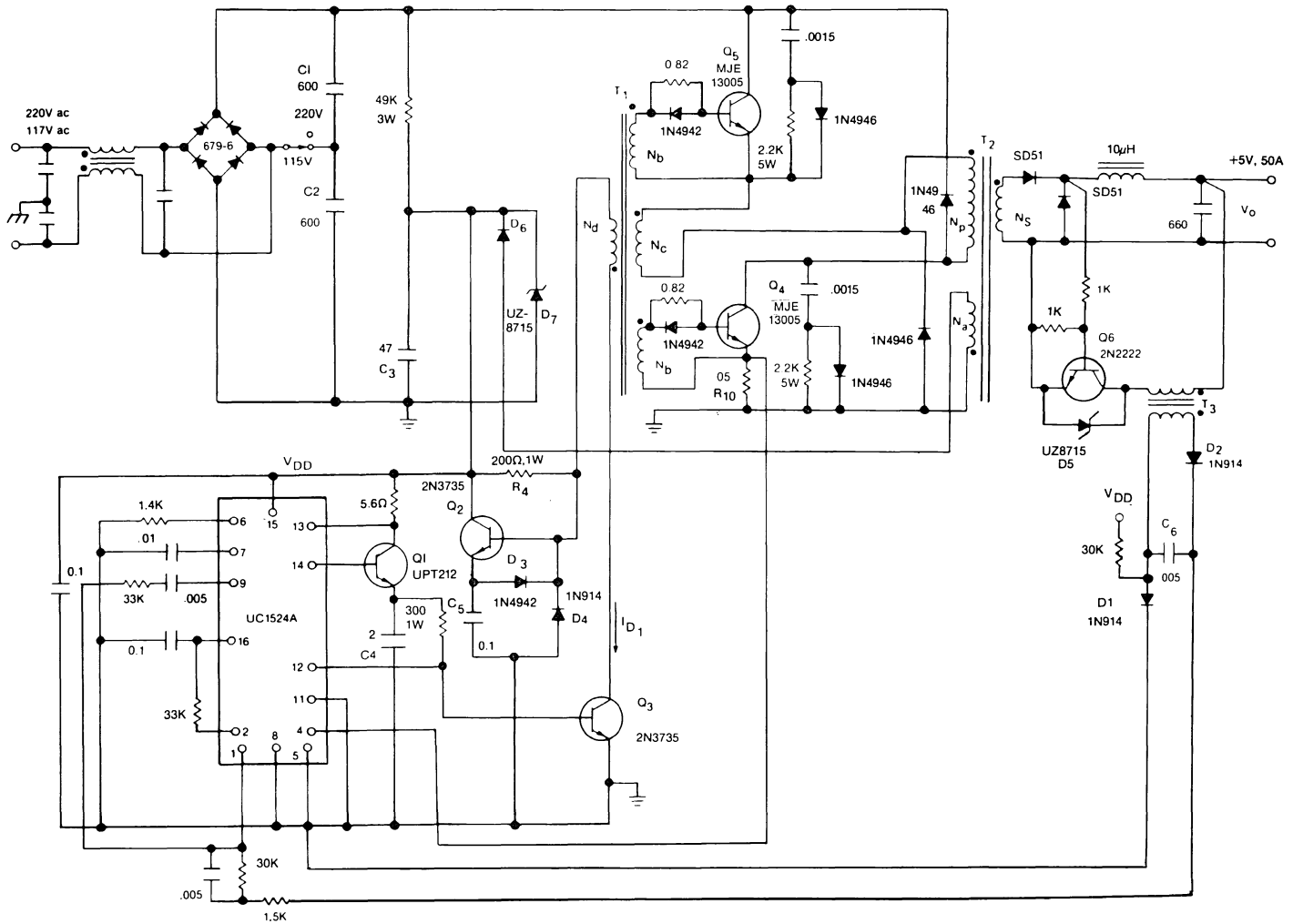

Figure 2. Complete 250 Watt Switching Power Supply

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THE COMPLETE POWER SUPPLY CIRCUIT

The complete 250 watt switching power supply schematic is given in Figure 2. This supply meets all of the specification requirements defined on page 1.

LINE INPUT AC TO DC CONVERSION

The input rectifier/filter section converts the AC line voltage into a crudely filtered and unregulated DC voltage, V_{in}, which powers the downstream switching regulator. The input section is configured as a full-wave bridge when operating from the 230 volt line, and as a voltage doubler when operated from 117 volts. This provides approximately the same V_{in} range (200-380 volts) for the switching regulator with either line voltage. Minimum input voltage, V_{min}, is 200 volts at low line.

The design of the input section is covered extensively in Section I1 of the Design Reference Addenda at the end of this book. The power input required in this application equals power output (250W) divided by efficiency (75%), or 333 watts. Circuit values for this application can be obtained by multiplying the 100 watt input values given in Table I of Section I1 by $P_{in}/100 = 3.33$, using the worst case voltage doubler configuration:

$$C_1 = C_2 = 3.33(160) = 533\ \mu F \quad \text{(use 600 } \mu F\text{)} \tag{1}$$

$$I_{chg} = 3.33(1.126) = 3.75\ \text{Amps RMS AC} \tag{2}$$

The switching regulator draws 40 KHz rectangular current pulses which discharge the input capacitors. Peak discharge current, i_{dis}, occurs at Vmin when the duty cycle, D, is maximum (50%):

$$i_{dis} = Pin/(VminD) = 333/(200\ .5) = 3.33\ \text{A peak} \tag{3}$$

The RMS AC component of the discharge current, I_{dis}, which flows through the input capacitors at worst case 50% duty cycle is:

$$I_{dis} = (i_{dis})/2 = 3.33/2 = 1.67\ \text{Amps RMS AC} \tag{4}$$

The total RMS AC current rating required for the input capacitors is calculated from Equation 8 of Section I1:

$$I_{CAP} = \sqrt{I_{chg}^2 + I_{dis}^2} = \sqrt{3.75^2 + 1.67^2} \tag{5}$$

SWITCHING CIRCUIT TOPOLOGY

The two transistor forward converter configuration shown in Figure 3 was used in this 250 watt switching power supply for the following reasons:

1. Transistor voltage ratings are half the voltage required in a comparable single transistor circuit (400V vs. 800V). Only 1/4 the silicon chip area is required for the same current rating, and the switching speeds will be twice as fast.

2. The snubber networks are for load line shaping only and are not required to absorb all the energy stored in the transformer leakage reactance. Instead, clamp diodes D_5 and D_6 conserve most of this energy by returning it to the input, improving the efficiency.

3. Closed-loop stability is easier to achieve than with a flyback converter because there is no right half plane zero.

4. Filter capacitor requirements are much less severe than in boost or flyback converters because of the output filter inductor.

5. Transformer construction is simplified because there is no need for a clamp winding (N_a is used for the auxiliary supply).

6. Reliability is improved because faster transistors result in reduced switching losses, and each transistor dissipates only one half of these reduced losses.

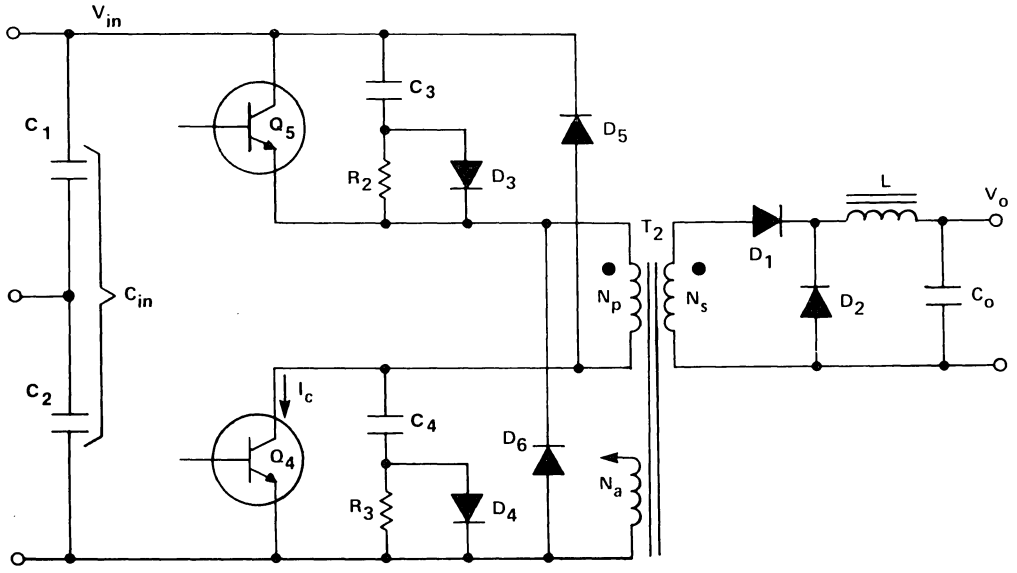

Figure 3. Two Transistor Forward Converter

Disadvantages of this topology are:

1. Two transistors are required instead of one (but cost may be less).

2. Restricted to less than 50% duty cycle to permit core reset. This results in poorer transformer utilizetion.

3. Added cost of filter inductor, which is not required for the flyback converter.

SPECIFYING THE SWITCHING TRANSISTORS

Maximum peak primary current flowing through the transistors, I_{CM}, is the same as i_{dis} from Equation 3, or 3.33 A.

The transistors should have good VCE(sat) and switching speeds at a collector current of at least 4.0 amperes, which includes an allowance for unusual conditions such as short circuit current. (Disregard spec sheet "maximum current ratings" which are inflated for competitive marketing reasons, and focus on the specified test conditions.)

The collector voltage rating must be greater than maximum V_{in}, or 380 volts in this application. Conservatively, this should be the BV_{CEO} rating, but with careful load line shaping to make certain the transistor is completely off before voltage is applied, a less conservative designer might specify BV_{CEX} greater than $V_{in(max)}$.

The UMT13007 satisfies the above requirements, with BV_{CEO} of 400V, $V_{CE(sat)}$ less than 2.0V at 5A, and worst case fall time of 400ns under the proportional base drive conditions provided.

SNUBBER NETWORK DESIGN

The turn-off snubber networks shown across each transistor in Figure 3 provide shaping of the load line to ensure that it remains below the reverse bias safe operating area (RBSOA) of the transistors. Capacitors C_3 and C_4 accomplish this by holding the voltage across each transistor low during current turn-off. The snubber capacitors thus absorb the turn-off transition energy that otherwise would have been dissipated in the transistors (see Figure 4).

$$C_3 = C_4 = \frac{I_{CM}\, t_f}{2\, V_{in(max)}} \qquad (6)$$

$$= \frac{3.33 \times .4 \times 10^{-6}}{2 \times 380} = .00175\ \mu F \quad \text{(use } .0015\ \mu F\text{)}$$

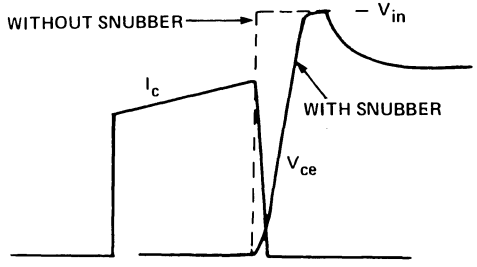

Figure 4. Effect of Snubber Network on Turn-Off Characteristic

Resistors R_2 and R_3 are designed to discharge the snubber capacitors with a discharge time constant of one-half the minimum on time, $t_{on(min)}$.

$$t_{on(min)} = \frac{D(max)}{f}\frac{V_{in(min)}}{V_{in(max)}} = \frac{0.5}{40{,}000}\frac{200}{380} = 6.58\ \mu s \qquad (7)$$

$$R2 = R3 = \frac{t_{on(min)}}{2C_3} = \frac{6.58\times10^{-6}}{2 \times 1.5\times10^{-9}} = 2.2K$$

Maximum power dissipation in each resistor:

$$P_{R2} = P_{R3} = \frac{1}{2} C2 V_{in(max)}^2 f \qquad (8)$$

$$= \frac{1.5\times10^{-9}}{2} \times 380^2 \times 40{,}000 = 4.3 \text{ watts}$$

POWER TRANSFORMER DESIGN

The design of the 40KHz inverter transformer is detailed in Appendix A. A primary to secondary turns ratio of 148/9, or 15.33, ensures that 5 volts output is provided with minimum Vin of 200 volts at 50% duty cycle, including voltage drops in rectifiers, transistors and windings.

Transformer winding N_a is used to provide an auxiliary supply to power the control and base drive circuits. This makes good use of the energy stored in the transformer primary inductance.

OUTPUT FILTER DESIGN

The output filter and its associated waveforms are shown in Figure 5. The filter inductor calculation is based on the maximum "off" time:

$$D(min) = D(max)\frac{V_{in(min)}}{V_{in(max)}} = 0.5\frac{200}{380} = .263 \qquad (9)$$

$$t_{off(max)} = \frac{1-D(min)}{f} = \frac{1-.263}{40{,}000} = 18.4\ \mu s \qquad (10)$$

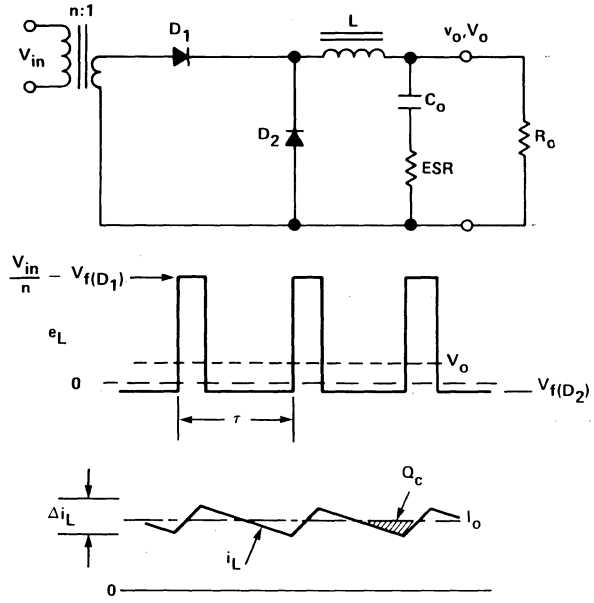

Figure 5. Output Power Filter Design

The inductance required to prevent discontinuous mode operation depends upon the minimum load current:

$$\Delta I_{L(max)} = 2I_{o(min)} = 2 \times 5 = 10A \quad (11)$$

$$L = \frac{(V_o + V_F)t_{off(max)}}{\Delta I_{L(max)}} = \frac{(5 + 0.6)18.35}{10} = 10\ \mu H \quad (12)$$

The capacitance required to achieve the output ripple voltage specification of 0.1 volts is:

$$C_o = \frac{1}{2}\frac{\Delta I_{L(max)}}{2}\frac{1}{2f\ v_o} = \frac{10}{8 \times 40{,}000 \times 0.1} = 312\ \mu F \quad (13)$$

The maximum ESR of the capacitor is:

$$ESR = v_o/\Delta I_{L(max)} = 0.1/10 = .01\ \Omega \quad (14)$$

To obtain the necessary ESR requires a capacitor much larger than the 312 microfarads calculated. This design will use three 220 microfarad solid tantalum capacitors, Mallory THF227M010P1G, in parallel. A single 14,000 microfarsd aluminum electrolytic capacitor, Mallory CG0143M10R2C3PL could also be used.

With the tantalum capacitor, the resonant frequency of the filter is 2KHz. With the aluminum electrolytic, the resonant frequency is reduced to 425Hz, changing the closed-loop design.

CLOSING THE CONTROL LOOP

The Unitrode UC1524A is used for the control circuit. It has additional features such as pulse by pulse current limiting and high current and voltage output capability (200mA, 60V) compared with the SG1524. The UC1524A reference is trimmed to +/- 1% which makes it possible to avoid using a voltage-setting potentiometer in many instances.

The control to output transfer function, dV_O/dV_C, shown in Figure 6, incudes the cascaded gain of the sawtooth modulator within the UC1524A control IC, the power switching circuit, and the output filter characteristic, $H_e(s)$.

In the control IC, a control voltage V_C is compared with sawtooth ramp voltage V_S (2.5 volts) to establish the drive pulse width to the power switches. For the forward converter, only one of the two alternating outputs of the UC1524A is used so as to limit the duty cycle to 50% maximum and allow for transformer core reset:

$$D = 0.5V_C/V_S = 0.5V_C/2.5 = V_C/5 \qquad (15)$$

The forward converter is a member of the buck regulator family. Transformer turns ratio n = 16.44:

$$V_O = \frac{V_{in}}{n} D = \frac{V_{in}\, V_C}{n\, 2V_S} \qquad (16)$$

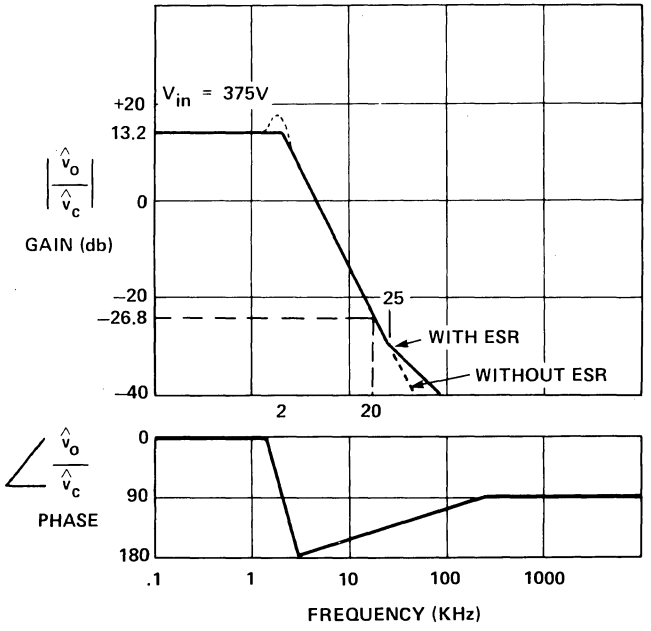

Figure 6. Control to Output Transfer Function LC Filter and Modulator

The low frequency control to output transfer characteristic is obtained by differentiating with respect to Vc:

$$\frac{\partial V_O}{\partial V_C} = \frac{V_{in}}{n\ 2V_s} = \frac{380}{15.33 \times 5} = 4.95 = 13.2\ db \qquad (17)$$

Note that gain is greatest at maximum V_{in}. The overall control to output transfer characteristic including the filter is:

$$\frac{\partial V_O}{\partial V_C} = \frac{V_{in}}{n\ 2V_s} H_e(s) \qquad (18)$$

The filter introduces a two-pole characteristic at its resonant frequency (2 KHz). Above resonance, the gain drops 40db per decade, and the phase shift becomes −180 degrees. Combined with the −180 degree phase shift of the feedback network, this will cause instability and oscillations unless compensated.

Closing the loop involves feeding back the error voltage from the output terminal of the supply ($\hat{v}_O$) to the IC control voltage port ($\hat{v}_C$) through the UC1524A error amplifier. The approach taken is to make the gain of the feedback network such that the overall loop gain crosses zero db (with adequate phase margin) at one half the switching frequency.

As shown in Figure 6, control to output gain is 13.2db at low frequencies, rolling off above 2KHz at −40db per decade, so that at 20 KHz the control to output gain is 13.2 − 40, or −26.8db. For overall loop gain of zero,the feedback network gain must be made +26.8 db at 20 KHz.

From 20KHz down to 2Kz, there is a net single zero in the feedback network which cancels one of the two filter poles and reduces the phase shift in this region to −270 degrees.

Below the filter resonant frequency the two filter poles are gone. However, the resonant frequency may be less than 2KHz because of plus tolerances on the filter capacitor. The feedback network is therefore designed to transition from a net single zero to a single pole at 1KHz, half the resonant frequency.

Figure 7 shows the gain and phase plot of the error amplifier and the overall feedback loop. Figure 8 shows the specific feedback network used to achieve this result.

The high frequency error amplifier gain is set by R_2 and R_3. An R_3 value of 33K is chosen to minimize amplifier loading:

$$Av1 = R3/R2 = 26.8db = 21.9 \qquad (19)$$
$$R2 = R3/Av1 = 33000/21.9 = 1500\ \Omega$$

The required error amplifier gain at 1KHz is:

$$Av2 = Av1 \times 1KHz/20KHz = 21.9 \times 1/20 = 1.095\ (0.8db) \qquad (20)$$

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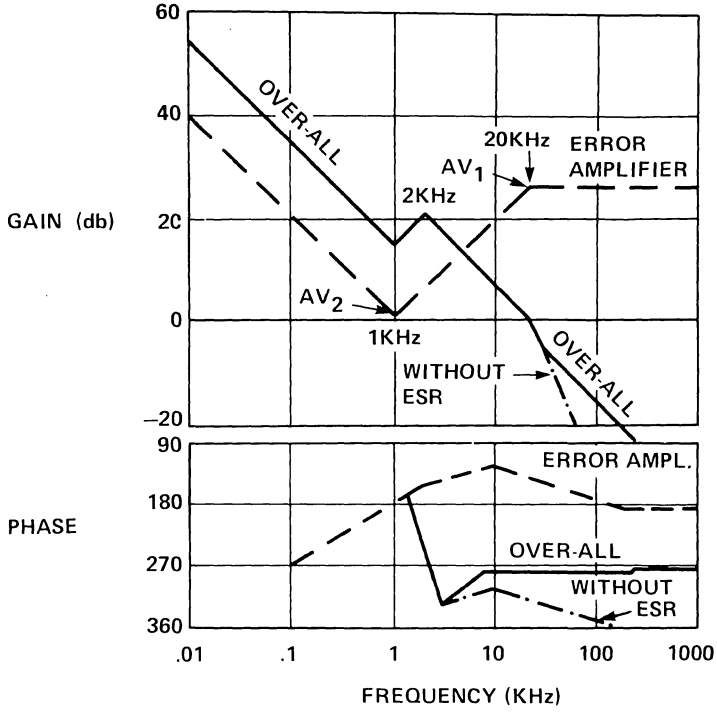

Figure 7. Open Loop Gain and Phase Plot

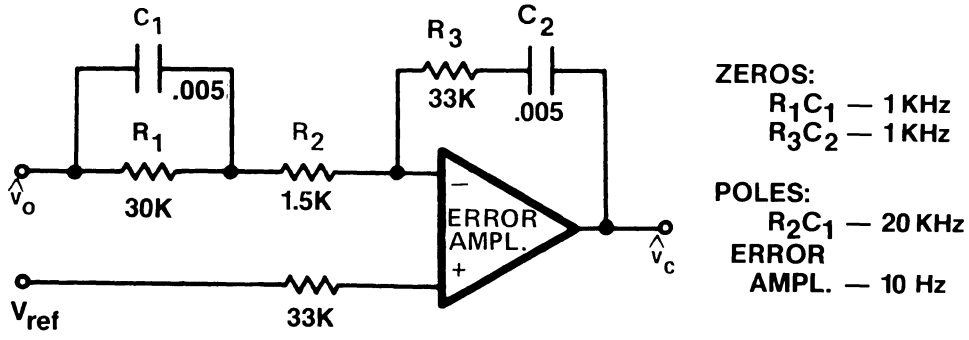

Figure 8. Error Amplifier with Compensation

The gain at 1KHz is determined by R_1, R_2 amd R_3:

$$Av2 = R3/(R1+R2) = 33K/(R1+1500) = 1.095 \quad [21]$$

$$R1 = 28.6K \quad \text{(use 30K)}$$

The two zeros at 1KHz which changes the feedback network from a net single zero to single pole are equal to:

$$f_1 = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_3 C_2} = 1 \text{ KHz} \quad (22)$$

$$C_1 = .0053 \ \mu F, \qquad C_2 = .0048 \ \mu F$$

C_1 and R_1 in parallel with R_2 result in an additional pole at 20KHz. This flattens the error amplifier gain above 20 KHz. The overall phase shift will gradually increase toward 360 degrees, but it doesn't matter because the overall gain is less than one.

An additional pole occurs below 10 Hz. This is the inherent single-pole characteristic of the error amplifier's 5 megohm output impedance loaded by feedback capacitor C_2.

PROPORTIONAL BASE DRIVE

In Figure 2, transistors Q_2 and Q_3 and base drive transformer T_1 provide proportional drive to the bases of power switching transistors Q_4 and Q_5. The proportional base drive technique provides excellent performance from high voltage bipolar transistors. It provides large base current pulses for fast turn-on and turn-off, but with modest drive power requirements. Sustaining base drive is provided regeneratively from a collector current winding on the drive transformer. The transistors are never overdriven, even under light load conditions, since the sustaining base drive is proportional to the collector current. Design considerations for the proportional base drive technique are given in Section D1 in the design section at the back of this book.

Referring to the circuit of Figure 2, when Q_3 is on, R_4 establishes 75 mA magnetizing current in drive winding N_d of T_1. When Q_3 turns off, the energy stored in T_1 drives 150 mA into the base of each transistor. Collector current starting to flow in N_c provides sustaining base drive. With I_C of 3.33 A under full load conditions, an additional 667 mA of drive is provided to each base.

While Q_3 is off, capacitor C_5 charges through Q_2 in less than 1 microsecond. Then, when Q_3 turns back on, C_5 provides a negative base drive pulse of -1.5 A to each transistor, achieving turn-off in less than 1 microsecond.

Drive transformer T_1 has a drive winding inductance of 0.7 mH and is designed to saturate at 75 mA. High voltage insulation is not required because all windings are on the line side of the supply.

Core: Ferroxcube 1107P-L00-3B7 Pot Core
N_d: 20 turns AWG34
N_b: 5 turns AWG28x2 (2 wires, one for each base)
N_c: 2 turns 5xAWG28 (5 wires paralleled)

AUXILIARY POWER SUPPLY

A 15 volt auxiliary supply powers the control and driver circuits, obtaining its energy from capacitor C_3. Flyback energy is normally provided by T_2 through winding N_a and D_6 to maintain the charge on C_3 every switching cycle. However, at initial power-up it is neccessary to provide separate means to activate the V_{dd} supply. Otherwise, the control and driver circuits could not become functional and the supply could not start to switch.

The unique under-voltage lockout feature of the UC1524A facilitates this technique. All of its internal circuits are disabled (except the reference) until the Vdd voltage reaches 8 volts. This holds the standby current to less than 4mA until the 8 volt threshold is reached, and permits C3 to be initially charged through R1 from the unregulated input. Enough energy is stored in C3 to operate the control/drive circuits for several switching cycles, until flyback energy from winding N_a can take over and maintain the voltage on C_3.

It is also necessary to eliminate base drive to Q_3 during initial power-up, otherwise Q_3 will draw current through R_4 which will prevent C_3 from initially charging. This is accomplished by transistor Q_1 which disconnects base drive source capacitor C_4. When the UC1524A becomes active, its second output turns Q_1 on periodically to charge C_4.

The amount of energy stored in the power transformer is twice the drive/control circuit requirements. Excess energy is dumped into 15 volt zener diode D_7 which establishes the V_{dd} supply voltage at that level. This also provides a constant clamp voltage across the switching transistors, regardless of line voltage. With good coupling between N_a and primary winding N_p, it may be possible to eliminate clamp diodes D_{12} and D_{13}.

OUTPUT VOLTAGE SENSE AND OVERCURRENT SENSE

A small, inexpensive transformer, T_3, couples the output voltage to the line side control circuit with high voltage isolation. The transformer is wound on a Ferroxcube 204-T250-3E2A ferrite toriodal core. Primary and secondary windings are both 14 turns AWG32.

During the time the power switching transistors are on, Q_6 is on, applying V_o to the primary of T_3. Through D_2, this provides a real-time feedback voltage to the control circuit across C_6. When Q_6 is off, D_5 clamps the flyback voltage to 15 volts. Core reset is accomplished well before the end of the "off" time, since the "off" time of the forward converter is always more than 50%. All transformer windings then go to zero volts, establishing a DC coupling level. D_1 in series with the ground return compensates for the forward voltage drop and temperature coefficient of D_2.

Pulse by pulse current limiting is set by sense resistor R_{10}. Primary current is limited to 4A, corresponding to 62A load current.

Transient response of the switching supply is shown in Figure 9 with changes in load from 20A to 60A and back to 20A. This behavior is a large signal phenomenon. It doesn't matter how fast the control loop is, it is temporarily driven into the bounds because the load change is much larger than the output filter inductor current can accomodate in one cycle. Nevertheless, recovery is smooth and there is no evidence of ringing or oscillations, demonstrating the stability of the control loop. Step changes in load current that are small enough for the control loop to remain functional are barely noticable at the output.

Transient response can be improved by reducing the filter inductor and increasing the filter capacitor size, but this will increase the minimum load current required to keep the inductor current from becoming discontinuous.

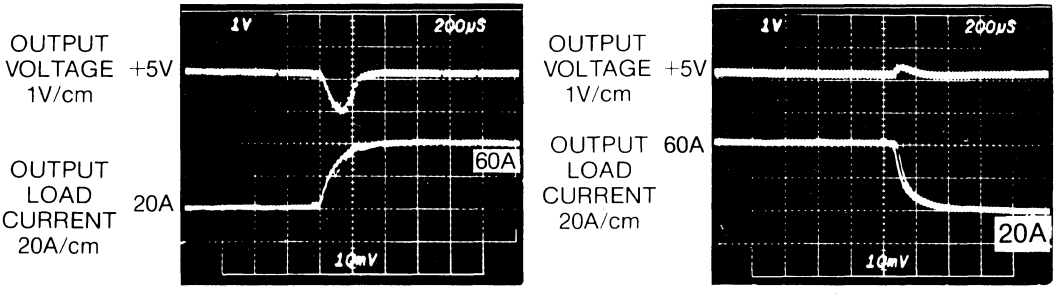

Figure 9. Step Change in Output Load

APPENDIX A
DESIGN OF THE POWER TRANSFORMER AND FILTER INDUCTOR

The design procedure used herein is defined in Design Reference Section M5. Symbols, definitions and various core and wire data are given in Reference Sections M1, M2, and M3. Equation references are to Section M5.

Flux Density Excursion

In this forward converter application, the flux excursion is entirely within the first quadrant of the B-H characteristic, from zero flux density toward saturation. With simple duty cycle control, using the UC1524A control IC, it is possible to have nearly twice the normal volt-seconds, $V_{in(max)}t_{on(max)}$, during startup or after a large step increase in load current. This means that the flux density cannot be permitted to go more than half way toward saturation under normal conditions or the core will saturate under transient conditions.

Saturation flux density for 3C8 power ferrite material is greater than 0.3 Tesla (3000 Gauss), allowing a ΔB of 0.15 T (0 to 0.15 T) in this application. (With volt-second control, available in the UC1840 control IC, a ΔB of 0.3 T would be permissible, significantly reducing the transformer size.)

Core Selection

The core area product, AP, requirements in this application are calculated using Equation 1 and Table I of Section M5 with power input of 333 watts and frequency of 40 KHz.

$$AP = A_w A_e = \left(\frac{11.1\ P_{in}}{K\ \Delta B\ f}\right)^{1.143} = \left(\frac{11.1\ 333}{0.141\ 0.15\ 40{,}000}\right)^{1.143} = 5.4\ cm^4$$

This equation is based on the assumptions that the windings occupy 40% of the window area, the primary and secondary windings are of equal area, and the windings are operated at a current density that will result in a temperature rise of 30°C with natural convection cooling.

Designing the Windings

The minimum number of primary turns required to support the volt-seconds required for normal operation is calculated from Equation 2 of Section M5:

$$N_{p(min)} > \frac{5000\ V_{in(min)}}{\Delta B\ Ae\ f} > \frac{5000\ 200}{0.15\ 1.83\ 40{,}000} > 91 \text{ turns}$$

From Equation 3, the primary to secondary turns ratio is:

$$n = \frac{N_p}{N_s} = \frac{0.9\ D\ [V_{in(min)} - V_{CE(sat)}]}{V_O + V_F} = \frac{0.45(200-2)}{5+0.8} = 15.36$$

Secondary turns from Equation 4:

$$N_s = \text{Integer}(N_p/n) = \text{Integer}(91/15.36) = 6 \text{ turns}$$

Recalculate the primary turns:

$$N_p = 6 \times 15.36 = 92 \text{ turns}$$

RMS primary current from Equation 6:

$$I_p = I_{in(max)}/K_t = \frac{P_{in(max)}}{V_{in(min)}\ K_t} = \frac{333}{200\ 0.71} = 2.34 \text{ A}$$

From Equation 7, the maximum current density for this size core is:

$$J_{max} = 450\ AP^{-.125} = 450(5.71)^{-.125} = 362 \quad \Omega/cm^2$$

The minimum primary wire area, A_{xp}, is:

$$A_{xp} = I_{p(max)}/J_{max} = 2.34/362 = .0065 \text{ cm}^2$$

From the Wire Table in Section M2 under 'AREA, Copper', AWG 19 is appropriate.

The maximum RMS secondary current, I_s, occurs at 50% duty cycle:

$$I_{s(max)} = I_{o(max)}/1.414 = 50/1.414 = 35.3 \text{ A}$$

Minimum secondary wire area, A_{xs}, is:

$$A_{xs} = I_{s(max)}/J_{max} = 35.3/362 = .0975 \text{ cm}^2$$

From the Wire Table, this calls for AWG 7 to 8. Ten AWG 18 wires in parallel will carry the required secondary current and provide a smooth winding with less leakage inductance and acceptable eddy curent losses. Copper strip 2.5x.04 cm could also be used.

Th number of turns required for the auxiliary winding is:

$$N_a = \frac{V_{dd}\ N_p}{V_{in(min)}} = \frac{15\ 92}{200} = 7 \text{ turns}$$

This will provide enough volt-seconds during flyback to reset the core (back to zero flux density) at 50% maximum duty cycle. AWG 32 wire is adquate to carry the V_{dd} supply current. This winding should be tightly coupled to the primary.

Double-check the wire fit in the window (neglect N_a). The total copper area of all windings should be less than 40% of the total window area of the core (0.40x3.12 = 1.25 cm² max).

$$A_w' > N_p A_{xp} + N_s A_{xs} = 92(.0065) + 6x10(.00823) = 1.09 \text{ cm}^2$$

Calculate Losses and Temperature Rise

The total losses in the windings is calculated from Equation 12. The mean length per turn, l_t, for the EC52 core is 7.3 cm, and AWG 19 wire is .000353 Ω/cm from the Wire Table at 100°C.

$$P_w = 2\, I_p^2\, N_p\, l_t\, (\Omega/\text{cm}) = 2(2.34)^2 x92x7.3x.000353 = 2.59 \text{ watts}$$

The total core losses for 3C8 ferrite are obtained from Figure 1 in Section M3. The flux density axis of this graph assumes the transformer is operating with a symmetrical flux swing about the origin. The forward converter operates asymmetrically, so enter the graph with ΔB/2, or .075 T. The resulting 0.01 W/cm³ must be multiplied by the core volume to obtain the total core loss, P_c.

$$P_c = .01x18.7 = .187 \text{ watts}$$

Total transformer losses are:

$$P_t = P_w + P_c = 2.59 + .187 = 2.78 \text{ watts}$$

The temperature rise of the core for natural convection cooling is calulated from Equation 14:

$$\Delta\theta = \frac{850\ Pt}{As} = \frac{850(2.78)}{91} = 25.9^\circ C$$

Summarizing the transformer design:

Core: Ferroxcube EC52, 3C8 Ferrite E-E core
Np: 92 turns AWG19
Na: 7 turns AWG32
Ns: 6 turns 10xAWG18 (10 wires paralleled)

The primary and auxiliary windings are tightly coupled. The secondary is insulated with 2mil mylar tape to provide 3750 volt line isolation capability.

Filter Inductor Design

The design of the filter inductor is covered extensively in Unitrode Application Note U68A, in the Unitrode Databook. Using this approach, the inductor design is summarized as follows:

Core: Ferroxcube 4229-3C8 Ferrite Pot Core
Winding: 7 turns 10xAWG17 (10 wires paralleled)
Losses: 2.2 watts
Temperature Rise: 35°C

HIGH FREQUENCY SERIES RESONANT POWER SUPPLY — DESIGN REVIEW

By Raoji Patel and Roger Adair

I. INTRODUCTION

In the past decade, power conversion technology has advanced from linear to switching due to the inherent high efficiency, smaller size, and lower cost of the latter technology. Recently, designers involved with conversion technology have started to consider resonant sine wave power supplies because they offer even smaller size, improved reliability, and reduced EMI.

It is possible to operate these power supplies at high frequency for two reasons. First, low-cost power MOSFETs, which, unlike bipolar transistors, have no storage time, are now available. Second, series resonant topologies are tolerant of some undesirable features of power semiconductor devices, (e.g., switching transition time and reverse recovery times.)

This paper explains the basic operation of the power output stage of a series resonant converter and examines its advantages and disadvantages compared to a conventional switching-regulated power supply. To provide a practical example, the paper details the design of an off-line series resonant power supply. The Unitrode low-cost UC3524A PWM Control Circuit is utilized to provide control for the series resonant power supply.

The 200kHz resonant power supply developed herein, as shown in Figure 1, operates from a 117V(±15%), 60Hz line and meets the following requirements:

1. Output Voltage
   A. +5V ±5% 2.5A — 5.0A
      Ripple Voltage: 100mV P-P maximum
   B. +12V ±3% 1A — 2A
      Ripple voltage: 100mV P-P maximum
   C. +24V ±5% 1A — 2A
      Ripple Voltage: 200mV P-P maximum
2. Efficiency 80% minimum.
3. Short-circuit protected.

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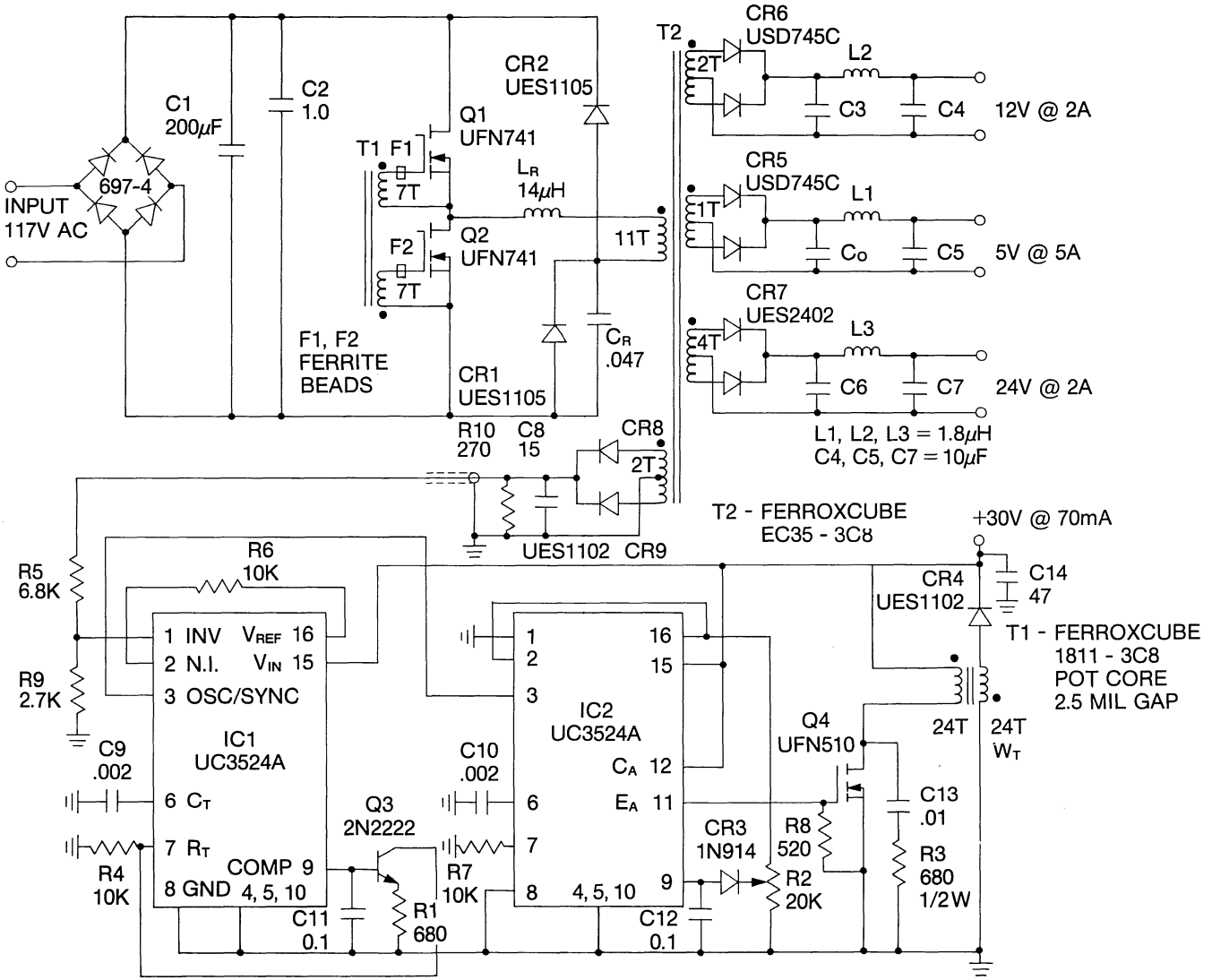

Figure 1. Schematic of Resonant Converter

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Basic Principle and Operation

The power output stage and its associated waveforms at typical input voltage are shown in Figures 2 and 3. During the on-time of power switch Q1, the energy is delivered from the input supply to the output load and series resonant capacitor C_R. During the on-time of transistor Q2, the energy is transferred from capacitor C_R to the output load. Note that the rectifier diodes, CR1 and CR2, clamp the voltage across capacitor C_R by providing a current path through the V_{in} supply or ground. The AC current in the secondary winding of the transformer is rectified by rectifier diodes CR3 and CR4 and filtered with output filter capacitor C_O.

Under steady state condition, the output voltage V_o is reflected back to the primary side by NV_O, where N is the transformer turns ratio. The polarity of the reflected voltage depends upon the state of transistors Q1 and Q2. When transistor Q1 turns on, the input voltage V_{in} is applied across the series resonant network L_RC_R and the primary of the power transformer. Since voltage across the primary is fixed by its turns ratio and the output voltage, the current i_R in the primary increases in a sinusoidal manner (starting at zero) because it is controlled by the series resonant network. The voltage across capacitor C_R increases in a sinusoidal manner starting at zero, while the voltage across the inductor decreases toward zero. When the voltage across the inductor reaches zero, the current in the resonant network ceases to increase. At this instant, the peak current I_{RP} can be expressed by the equation:

$$I_{RP} = \frac{V_{in} - NV_O - V_{Ci}}{|Z_O|}$$

Where Z_O is the characteristic impedance of the series resonant network

V_{Ci} is the initial voltage across the capacitor; $V_{Ci} = 0$ for input voltage above $V_{in(min)}$

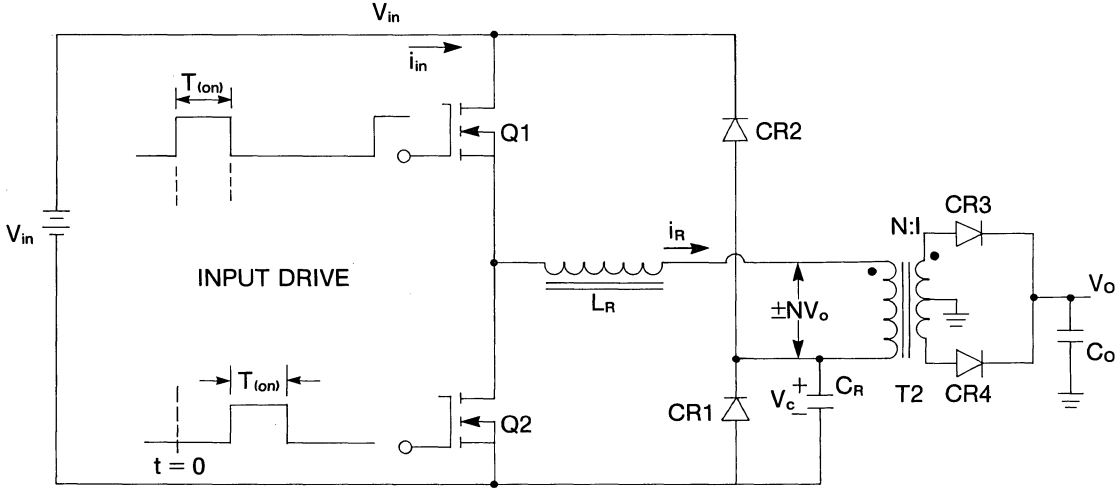

Figure 2. Power Output Stage

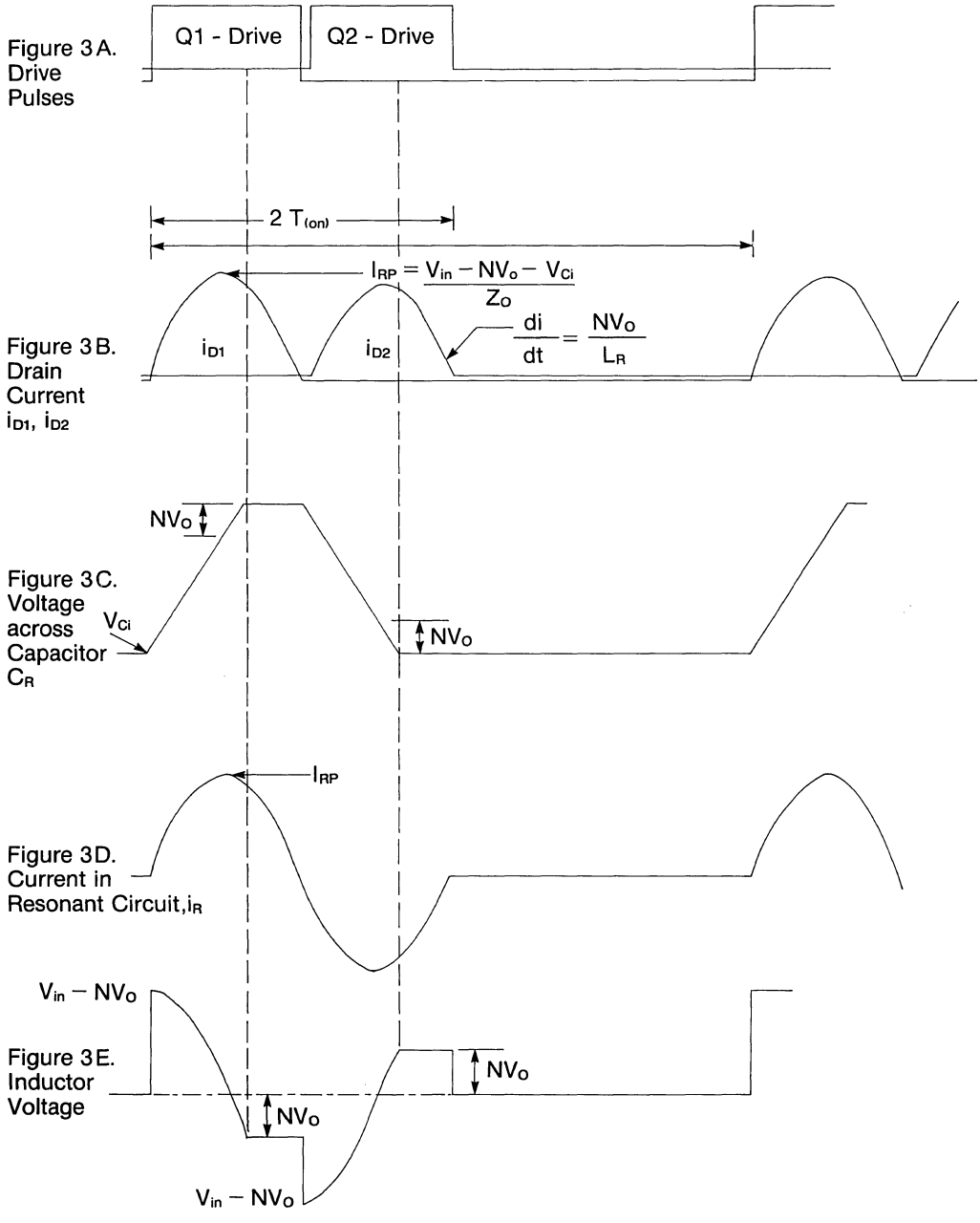

Figure 3. Voltage and Current Waveforms of the Power Output Stage of a Series Resonant Converter (with Input Volt V_{in} greater than $V_{in(min)}$)

The polarity of the voltage across series resonant inductor L_R reverses and the current starts to decrease from its peak value. The voltage across the resonant capacitor C_R continues to increase until it is clamped by diode CR2. The voltage across the series resonant inductor L_R ceases to increase when the voltage across capacitor C_R is equal to one diode drop above the input voltage V_{in}. The voltage across the inductor L_R is equal to the reflected output voltage NV_O. The current in the primary decreases in a linear manner. The slope of the current can be expressed by the equation:

$$\text{slope: } \frac{di}{dt} = \frac{NV_O}{L_R}$$

For proper operation, transistor Q1 must remain on until the current in the resonant network reaches zero. When the current in the resonant network reaches zero, the transistor Q2 is turned on and the current in the primary increases from zero, but this time in the reverse direction. The cycle repeats itself as described previously.

For maximum power transfer in a given design the selected turns ratio of the transformer should be such that the reflected output voltage across the primary is equal to half the value of the minimum input supply voltage. This can be expressed by the equation:

$$NV_O = \frac{V_{in(min)}}{2}$$

The output voltage is regulated by controlling the duty cycle, using a single cycle sine wave. Note that the required on-time of the power switches varies somewhat depending upon the input voltage variation. To maintain zero current switching, high efficiency and prevent cross conduction, the on-time should be determined at the maximum input voltage.

The maximum on-time of the power switch, referring to Figure 4A, can be calculated as follows:

Maximum on-time: $T_{on} = t_1 + t_2$

Where t_1 = time period for sinusoidal part of the current waveform.

Where t_2 = time period for linear part of the current waveform.

The time t_1 can be expressed by the equation:

$$t_1 = \frac{2\pi\sqrt{LC}}{360^\circ}\left[90^\circ + \text{SIN}^{-1}\frac{(V_{in(min)}/2)}{V_{in(max)} - \left(\frac{V_{in(min)}}{2}\right)}\right]$$

The peak current in diode CR2, to calculate the linear portion of the current waveform:

$$I_{d(pk)} = \frac{V_{in(max)} - NV_O}{|Z_O|}\text{SIN}\left\{90^\circ + \text{SIN}^{-1}\left[\frac{(V_{in(min)}/2)}{V_{in(max)} - (V_{in(min)}/2)}\right]\right\}$$

Where $Z_O = \sqrt{\frac{L_R}{C_R}}$ = Characteristic impedance of series resonant network.

Thus, the time needed for the linear portion of the current waveform:

$$t_2 = I_{d(pk)}\left[\frac{L_R}{\left(\frac{V_{in(min)}}{2}\right)}\right]$$

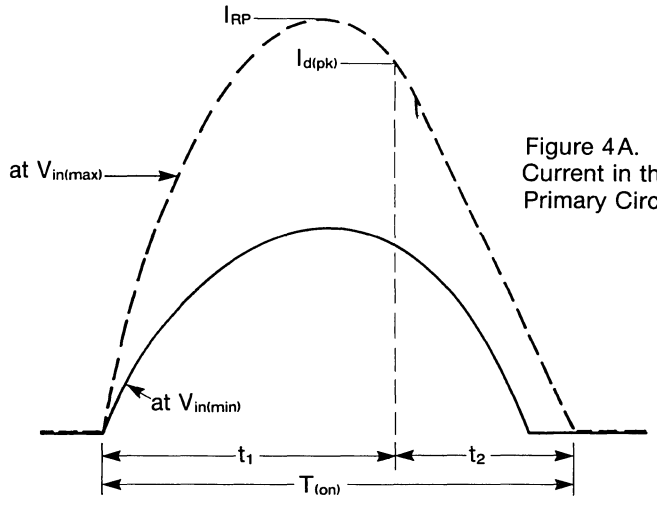

Figure 4A. Current in the Primary Circuit

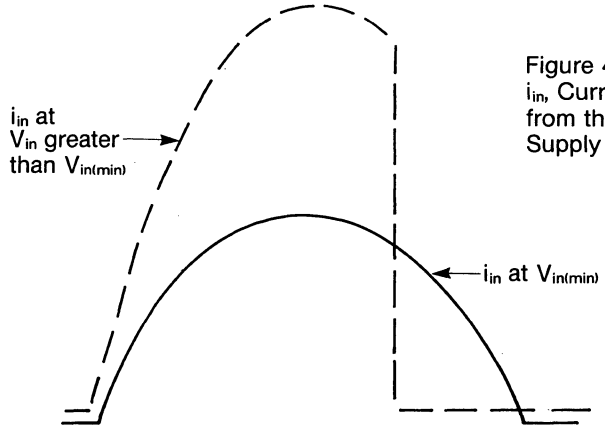

Figure 4B. i_{in}, Current Drawn from the Input Power Supply

Figure 4. Current Waveforms at Minimum and Maximum Input Voltage

III. ADVANTAGES AND DISADVANTAGES OF SERIES RESONANT CONVERTERS

Advantages

The resonant sine-wave converter, when compared to buck-derived switching regulator topologies, has the following advantages.

(A) Higher overall efficiency:

(1) There are no power losses due to the switching of the power switch or rectifier reverse recovery. Therefore, the conversion efficiency is higher.

(B) Smaller weight and volume:

(1) Because the voltage is switched when the drain current is zero, operation at a higher frequency is possible. This results in smaller magnetic elements and filter components.

(2) Due to the absense of switching losses, the required heat sink is smaller.

(3) Simpler drive circuit when power MOSFETs are used.

(4) The output filter inductor is smaller.

(C) Reduction in EMI:

(1) No high frequency rectifier reverse recovery current spikes are reflected back to the transformer primary.

(2) The transistor voltage is switched when current in the switch is zero. Therefore, there is no high di/dt other than at the fundamental frequency. Thus, a smaller amount of high frequency energy is radiated from the circuit.

(3) Undesirable effects of leakage inductance (L_ℓ) in the transformer primary are minimized in a resonance converter because L_ℓ is utilized as part of the series resonance circuit. Thus, high frequency current and voltage spikes due to leakage inductance are eliminated.

(4) Current drawn from the input filter capacitor has only the odd harmonics of the resonance frequency and their amplitude is lower.

(D) Increased reliability (high MTBF):

(1) The resonant inductor L_R provides inherent short-circuit protection.

(2) The inductor L_R also minimizes large current spikes in the power switch during start-up.

(3) Zero current switching eliminates high peak power stress on the power semiconductor and localized peak junction temperature.

(4) When using a MOSFET as a power switch, there is no danger of forward bias (I_{SB}) or RBSOA.

(5) Voltage and current overshoot are minimized.

(6) Resonant converters are stable under no-load operation.

Disadvantages

(A) This topology requires the additional resonant circuit (inductor and capacitor), when compared to a buck type converter. The inductor and capacitor must carry high current, but are small in value.

(B) The required current or voltage rating of the power switch is $\sqrt{2}$ times higher compared to a switching regulator topology.

(C) Output filter capacitors must have low ESR and high ripple current ratings.

IV. HIGH FREQUENCY CONSIDERATIONS

A. Circuit Layout Guidelines

The following circuit layout guidelines should be used to optimize performance and prevent spurious oscillation or ringing, reduce radiated RFI, improve efficiency and regulation, and allow proper circuit operation.

(1) Use a short, wide ground plane and minimize the component lead inductance to that ground plane.

(2) Use separate ground returns for the power stage and the low-level control circuit.

(3) Minimize circuit lead inductance:

(a) Keep leads short.

(b) Minimize the loop area enclosed by wire carrying high frequency current.

(c) When necessary, use copper straps/foils for high current.

(4) Use shielded wire in the feedback path to minimize pick-up and spurious oscillation.

(5) Be aware of package inductances, junction capacitances, heat sink capacitances, and other undesirable circuit parasitics.

(6) Use high frequency, low ESR capacitors and ferrite beads for EMI filtering.

(7) Use resistive damping when applicable. For example, a resistor or ferrite bead in the gate circuit can help to prevent spurious oscillation.

(8) Place the gap in the magnetic structure of the inductor directly under the coil winding.

B. Component Selection Guidelines

The following considerations are required when selecting or designing the components.

(1) Transformer and Inductor

Core losses are an important consideration in the design of a high-frequency converter. The core losses depend not only upon the peak flux density and the frequency, but also on the core geometry. These losses increase linearly with operating frequency, in ferrite with negligible eddy losses. Also, core losses increase as the peak operating flux density to the power of 2.5, approximately. Therefore, when the operating frequency is doubled for a given transformer (without changing the number of turns) the volt-seconds delivered to the primary and the peak operating flux density each decrease by a factor of two. The overall result is that core losses are reduced by approximately a factor of three at the higher frequency. If the transformer is redesigned to obtain the same core losses, the core will be smaller by a factor of $1/\sqrt[2.5]{3.} = 0.65$.

Use many parallel wires of small AWG size for the windings to minimize the proximity and skin effects. The proximity effect is a function of skin depth, conductor diameter, turns/layer, number of conductors per turn, and number of layers in the coil. The proximity effect produces eddy currents which distort the current distribution in the wire. Thus it increases the effective series resistance of the coil.

For low-voltage, high-current windings, copper strip or foil may be more practical than Litz wire because few turns are required. The gap in the inductor should be directly underneath the coil to minimize the radiated flux.

(2) Capacitors

Capacitors for high frequency circuits should be selected on the basis of ESR, ESL, ripple current rating (i_{RMS}) and self-resonant frequency (f_R), as well as cost and size. The resonant capacitor in the primary needs a good ESR and i_{RMS} rating. The output filter capacitors need low ESR and ESL, and high i_{RMS} and f_R. Bypass capacitors need low ESR and high f_R.

(3) Rectifiers

In this circuit, the parasitic diode of the power MOSFET should have fast forward recovery with low voltage overshoot, otherwise the other power device can be driven into breakdown during the deadband period.

In a series resonant converter, the reverse recovery of the output rectifier need not be extremely fast because of the low di/dt during diode turn-off.

V. DISCUSSION: PRACTICAL CIRCUIT

A. Power Output Stage

The output stage functions as follows. Assume both MOSFETs are off and the voltage on C_R is zero. When Q1 is turned on, the supply voltage is applied to the series resonant circuit comprised of L_R, the primary of T2, and C_R. The current starts to increase from zero in a sinusoidal manner, charging C_R and delivering energy through T2 to the load. Shortly after the peak of the sinewave current waveform is past, the voltage on C_R reaches the positive supply rail and CR2 conducts. The energy left in L_R continues to be released through T2 to the load, and the current ramps down toward zero. Note that the MOSFET voltage is switched when the current is close to zero, resulting in negligible switching loss. Also note that because of the intervening impedance of L_R, negligible reverse recovery spikes are drawn from the output rectifiers when Q1 or Q2 turn on.

The second of the two adjacent pulses produced by the drive circuit turns Q1 off and Q2 on. The above half cycle is repeated, except that the current flows in the opposite direction, thus producing the negative half-sine. Note that energy is drawn from the previously charged capacitor. C_R should be chosen for low ESR and good high frequency ripple current rating.

The output of the centertapped transformer secondary is rectified and is fed to capacitor C_O. Since the peak current in C_O is high, C_O must have low ESR and high ripple current rating.

Polypropylene type capacitors can be used. If lower cost is desired, a low ESR electrolytic of much larger capacitance (and size) may be suitable. A small low-pass filter comprised of L1 and C5 reduces the ripple appearing at the output to the desired value.

Note that the leakage inductance of the power transformer is in series with the inductance of L_R. Thus the total series resonant inductance is equal to the sum of the two. Also note the absence of snubbers across the Schottky rectifiers, permissible because of the low di/dt sinusoidal waveforms at the secondaries of the transformer.

B. Regulation and Drive Circuit

The drive circuit regulates the output voltage by varying the repetition rate of the waveform that drives the gates of the power MOSFETs. The two gates are driven by adjacent pulses of fixed pulse width. (This is not pulse width modulation.) Two of the standard PWM chips, the UC3524A, are used for the regulation circuit because they contain the necessary functions for this type of regulation.

The error amplifier and reference voltage of the first UC3524A are used in the normal manner. The output of the error amplifier, however, is used to control the amount of current at the R_T terminal of the oscillator, thus controlling the oscillator frequency. Q3, with a resistor R1 from emitter to ground, amplifies the error amplifier output. The collector of Q3 then sinks a variable amount of current out of the R_T terminal. The external C_T and R_T values set the minimum frequency. If the output power can vary by a factor of 2, then the frequency must be adjustable over a 2 to 1 range. The maximum frequency is set by the series resonant frequency of the output stage. If that is chosen at 200kHz, the minimum frequency for a 2 to 1 load change will be 100kHz.

The second IC chip is used as a one-shot. This is achieved by duty cycle limiting at the output of the error amplifier with diode CR3 and potentiometer R2. The pulse width is set equal to the width of a half sine of the output stage resonant circuit. By connecting their osc/sync pins together, the second IC is driven at the same frequency as the first IC. One of the output transistors drives the gate of Q4. Q4 drives the primary of T1 to produce a positive gate pulse for power switch Q1. When Q4 turns off, energy stored in the transformer core is returned to the 30V drive supply through "tertiary" winding W_T and CR4. Q2 is driven on at this time. The primary and tertiary windings of T1 have an equal number of turns and are clamped to the same voltage (30V) when conducting. Therefore, the time for the current to decay to zero in the tertiary winding will be the same as the time Q4 drove the primary. In this way Q2 and Q1 are operated at identical pulse widths. (Core saturation in T1 is prevented by using only one of the output transistors of the UC3524A, so the duty cycle is limited to 50%.) The snubber across Q4 (C13 and R3) damps out ringing to prevent Q1 or Q2 being turned on again after the desired double pulse is produced.

The rise and fall time of the MOSFET gate drive waveforms do not have to be ultra-fast in order to reduce switching losses, because those losses are already low due to zero current. Reasonably fast waveforms are desirable, however, to reduce deadtime between half-sine waveforms at maximum output. This minimizes the peak current in the MOSFETs, in the resonant circuit inductor and capacitor, and in the transformer and output rectifier and filter capacitors.

The circuit provides an efficiency of 81% and line and load regulation of ±5%.

VI. STABILITY CONSIDERATIONS

A simplified functional diagram of the regulator is shown in Figure 5. The small signal response of this converter is similar to that of a discontinuous-mode flyback regulator. The response of each of these topologies has only a single pole roll-off, the break frequency of which is determined by the output load R_L and the output filter capacitor C_O.

In the simplified functional diagram, the control chip IC1 converts the output of the error amplifier into regularly spaced sync pulses for control chip IC2. For each sync pulse, the control chip IC2 and the interfacing circuit provide two identical drive pulses in sequence. The total period of these pulses is equal to $1/f_R$. The duty cycle D can be related to the error output voltage V by the equation:

$$D = \frac{f}{f_R} = \frac{(1.15)2\pi\sqrt{L_R C_R}}{R_T C_T} = \frac{(1.15)V_c(2\pi)\sqrt{L_R C_R}}{V_{REF} R_{T_E} C_T}$$

The approximate DC transfer function of the power output stage, in terms of input supply voltage V_{in} and output R_L, is:

$$V_O = \frac{V_{in}}{1 + \frac{Z_O \pi}{2R_L D}}$$

The small signal gain varies with the input supply voltage and with output load. No special considerations are required, however, because the transfer function has only a single pole roll-off. It will provide 90° phase margin, which results in stable operation.

$$T_{(on)} = \frac{R_T'C_T'}{1.15} \geq \pi\sqrt{L_RC_R}$$

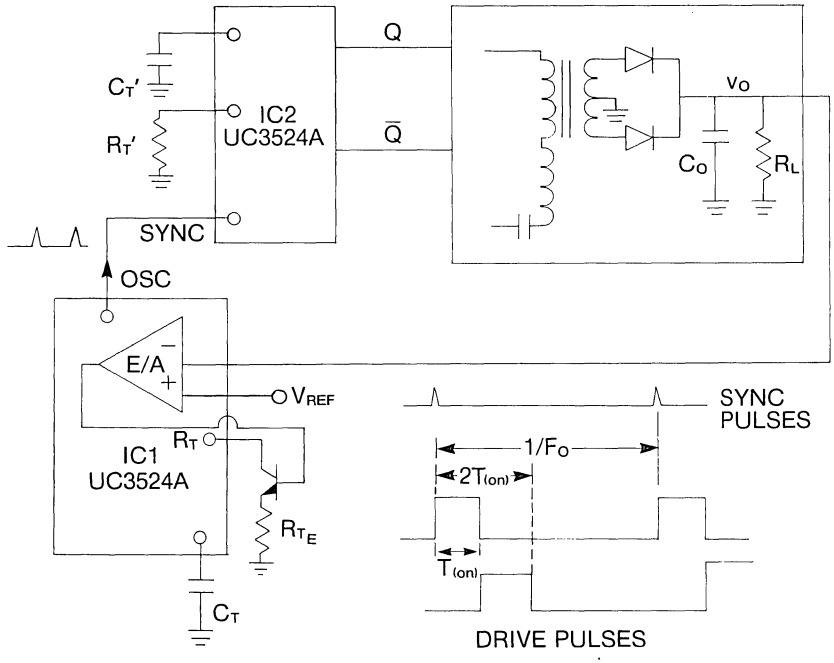

Figure 5. Simplified Functional Diagram

VII. SUMMARY

The availability of power MOSFETs, which have negligible storage times, has made practical the use of high frequency resonant sinewave converters. Switching losses are minimized by switching at approximately zero current crossings. Considerable improvements are realized in efficiency and reliability when compared to switched-mode designs.

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APPENDIX I.

Power Switch Selection and Design for a Series Resonant Circuit.

In this section, the maximum ratings of the power switch and the values of L_R and C_R in the series resonant circuit are determined.

A. Transistor Selection

At minimum input voltage $V_{in(min)}$, the converter will operate in an approximately continuous mode. Also, the voltage across the transformer primary at low line with a full load is half the input supply voltage for maximum power transfer. Note that for ease in calculation, the waveforms are approximated by a sinusoidal waveform.

The average primary current:

$$\bar{I}_{pri} = \frac{2P_{in}}{V_{in(min)}} = \frac{2(125)}{120} \approx 2.0A \tag{I.1}$$

Therefore, the peak current at low line:

$$I_{pk(L)} = \frac{\pi}{2} \cdot \bar{I}_{pri} = \frac{\pi}{2}(2.0) = 3.14A \tag{I.2}$$

The worse case peak current in a series resonant circuit will be at high line. Note that the same current also flows through the power switch. The maximum peak current in the transistors Q1 and Q2 can be expressed by the equation:

$$I_{pk(H)} = \frac{V_{in(max)} - \frac{V_{in(min)}}{2}}{\frac{V_{in(min)}}{2}} I_{pk(L)}$$

$$= \frac{190 - \left(\frac{120}{2}\right)}{\left(\frac{120}{2}\right)} \cdot 3.14A = 6.8A \tag{I.3}$$

Therefore, the selected transistor must have peak current ratings of 6.8A and blocking voltage greater than the maximum input supply voltage $V_{in(max)}$.

B. Calculation of the Component Values for the Series Resonant Network

The component values for the resonant network L_R and C_R can be calculated as follows.

First, the characteristic impedance:

$$Z_O = \frac{\eta V^2_{in(min)}}{2\pi P_O} \qquad \text{where } \eta \text{ is the efficiency}$$

$$= \frac{0.8(120)^2}{2\pi(100)} = 18.3\Omega \tag{I.4}$$

The capacitor:

$$C_R = \frac{1}{2\pi f_R |Z_O|} = \frac{1}{2\pi(200 \cdot 10^3)18.3} \approx .05\mu F \tag{I.5}$$

The inductor:

$$L_R = \frac{|Z_O|}{2\pi f_R} = \frac{18.3}{2\pi(200 \cdot 10^3)} \approx 14.5\mu H \tag{I.6}$$

Note that the total value of the resonant inductor must include the leakage inductance of the transformer as well as any lead inductance.

C. Inductor Design

The maximum energy storage in the core occurs at high line; the maximum circuit energy storage required is:

$$W_M = \frac{1}{2} L_R I^2_{pk(H)} = \frac{1}{2}(14.5 \cdot 10^{-6})(6.8)^2 = 335 \text{ micro joules} \tag{I.7}$$

The energy storage capability of the core must be equal to or greater than circuit energy storage W_M; therefore:

$$W_M \leq \frac{1}{2} BA_e H \ell_e 10^{-8} \tag{I.8}$$

Use a Ferroxcube 1F30 U-core at 1500 guass; from the previous equation,

$$H\ell_e = \frac{2W_M}{BA_e} 10^8 = \frac{2(335)10^{-6}10^8}{1500(.864)} = .52 \text{ amperes/turn} \tag{I.9}$$

Since for an inductor, all the energy is stored in the gap,

$$H\ell_g = NI_{pk(H)} = 52 \text{ A-T} \tag{I.10}$$

The number of turns required, from above equation, is:

$$N = \frac{H\ell_e}{I_{pk(H)}} = \frac{52}{6.8} \approx 8 \text{ turns} \tag{I.11}$$

The gap required to store the energy is:

$$\ell_g = \frac{NI}{H} = \frac{NI}{\left(\frac{B}{\mu}\right)} = \frac{52}{\left(\frac{.15}{(4\pi)10^{-7}}\right)} = .435 \text{ mm.} \tag{I.12}$$

The windings must cover this gap to reduce fringing of the flux. The core and copper losses are maximum at high line. For this design, the total losses are equal to 1.4 watts and result in an increase in core temperature above ambient of 31°.

D. Transformer Design

The reflected output voltage across the transformer primary should be equal to half the value of the minimum input supply voltage. This will determine the primary to secondary turns ratio. For the +5V output, the turns ratio is:

$$N = \frac{V_{in(min)}}{2(V_O + V_F)} = \frac{120}{2(5 + 0.6)} = 11 \tag{I.13}$$

The rest of the transformer design procedure is straightforward.

150 WATT FLYBACK REGULATOR

R. PATEL, D. REILLY, AND R. ADAIR

This paper describes the design of a low cost 150 Watt flyback switching regulated power supply. Output voltage regulation is achieved through the UC3842, a low cost current mode control IC, and the UC3901 isolated feedback generator. The complete schematic is shown in Figure 1.

The adverse effect of flyback transformer leakage inductance on power transfer to the output is discussed in detail.

SPECIFICATIONS:

Switching frequency, f_S:	100 kHz	
Efficiency, η:	80% minimum	
Output Voltages, V_{out}:	+5 V ±1%,	7.5 - 15 A
	+12 V ±3%,	1.5 - 3.0 A
	+24 V ±10%,	.75 - 1.5 A

TOPOLOGY SELECTION:

Current mode control used in this supply provides inherent good line regulation and optimum dynamic response. The two-transistor discontinuous mode flyback circuit shown in Figure 2 is a low cost approach with multiple output capability. Advantages and disadvantages of this topology are:

Discontinuous Mode Flyback - Advantages:

1. Because there are no filter inductors in series with each output (as in buck regulator circuits), all output voltages will track each other within ±5-10% without post-regulation. This minimizes the headroom required and its associated losses in the +12 V linear post-regulator. Dynamic cross-regulation is also very good with this topology.

2. Only one rectifier is required in each output instead of the two required in buck regulator circuits, reducing overall component and assembly costs.

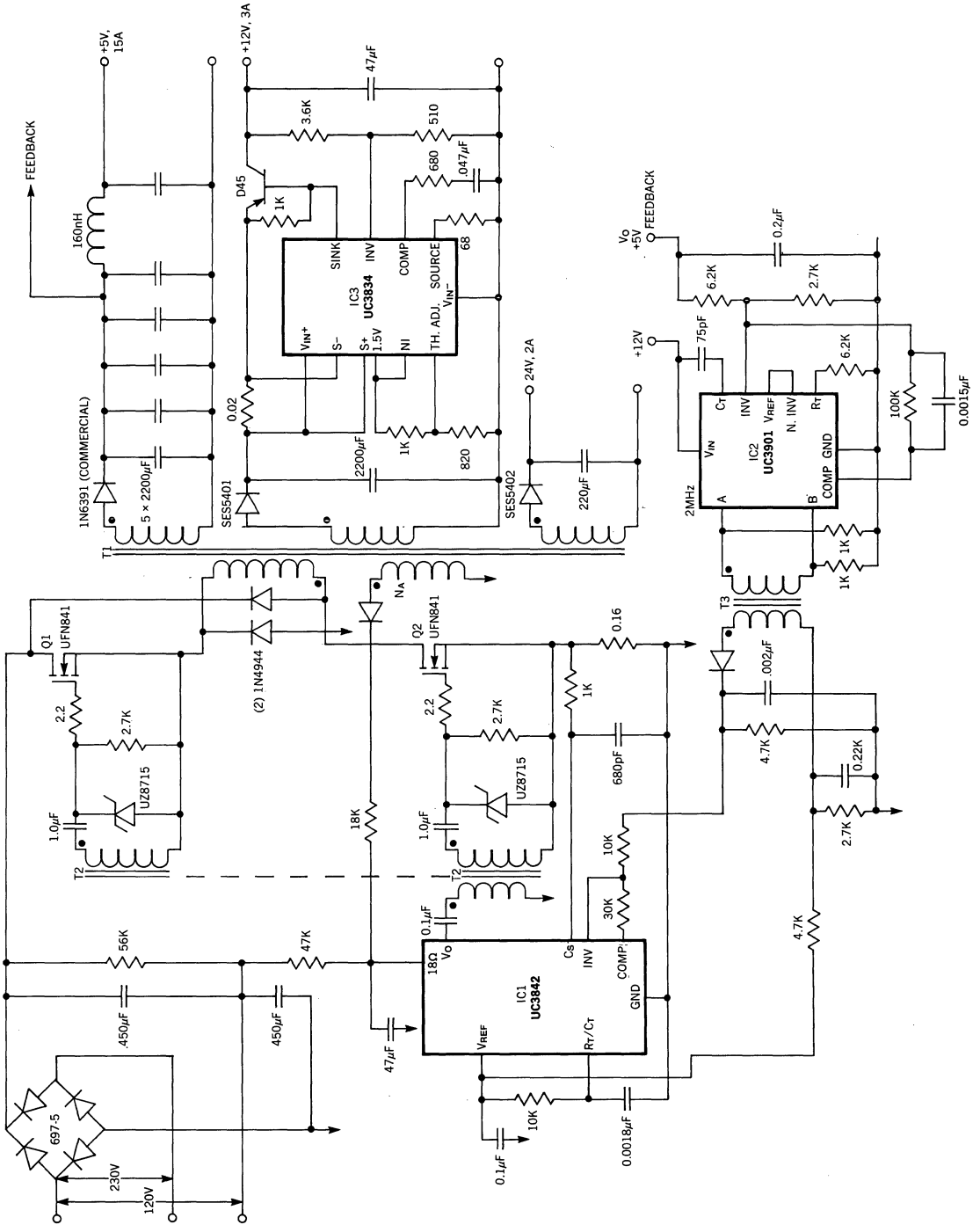
3. Rectifier reverse recovery time is not critical because forward current is zero well before reverse voltage is applied.

4. The flyback transformer used in the discontinuous mode is much smaller because the inductive energy stored is only 1/5 to 1/10 of the energy required in comparable continuous mode circuits.

5. Turn-on circuits are simplified because load current in the power switch is zero during turn-on. There is no concern for turn-on losses or turn-on snubber circuits.

6. Closing the feedback loop is simplified because of the single pole roll-off characteristic of the power circuit.

Figure 1. 150 Watt Flyback Supply -- Complete Schematic



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7. Transient response is excellent. The circuit can be designed to correct for large step changes in line or load in little more than one cycle of the switching frequency

8. Conducted EMI is reduced because transistor turn-on occurs with zero collector current. The triangular waveforms of the discontinuous mode contain only the odd harmonics which are attenuated much more rapidly than the even harmonics present in the rectangular waveforms of continuous mode flyback circuits or buck regulators.

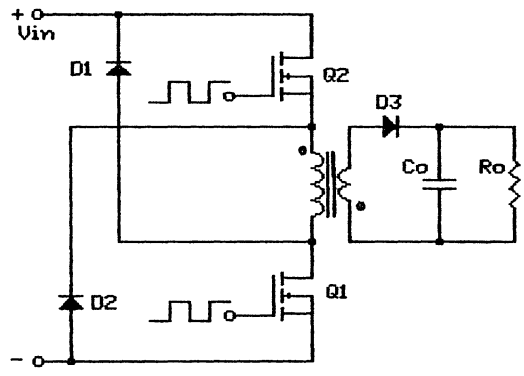


Fig. 2 - Two Transistor Flyback

Discontinuous Mode Flyback - Disadvantages:

1. Switching transistor and rectifier peak currents are nearly two times greater than in the comparable continuous mode circuit. However, the average currents are the same and transistor and diode dissipation is only slightly greater than in the continuous mode.

2. Output filter capacitor ESR and ESL requirements are quite stringent because of the high peak currents encountered in the discontinuous mode. Capacitance values must be nearly twice the comparable continuous mode requirements, and 10-20 times larger than a buck regulator with the same output capability. Nevertheless, transient response is much better because the flyback transformer inductance is so small.

Two-Transistor vs. Single Transistor - Advantages:

1. Voltage rating requirements of MOSFET power switches Q1 and Q2 are half that of a single transistor. This results in much better switching dynamics and much less than half the chip area for the same saturation voltage drop.

2. Cross-coupled diodes D1 and D2 provide a simple non-dissipative way to clamp the voltage backswing caused by T1 leakage inductance. The clamp energy is returned to the bulk input filter capacitor, thus the efficiency is not significantly impaired. Single transistor circuits require an additional transformer winding closely coupled to the primary to obtain non-dissipative clamping, or else the dump the energy (which usually amounts to 15-20% of the output power) into a dissipative snubber circuit.

3. Conducted and radiated EMI is significantly reduced because switching voltages at each end of the transformer move simultaneously in equal and opposite directions. Thus the current spikes that result from charging the stray capacitance to ground (from the wiring, switching transistors and within the transformer) tend to cancel, especially if the capacitance to ground from each end of the transformer is deliberately balanced.

Two-Transistor vs. Single Transistor - Disadvantages:

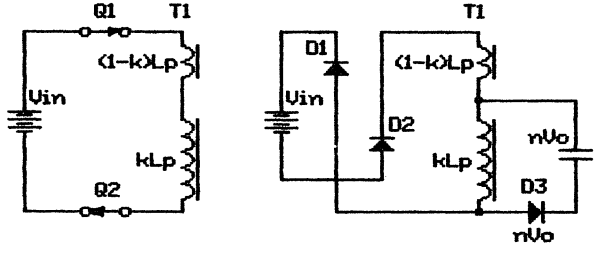
1. Two transistors are required rather than one, but for a 150 watt application, devices are available in the TO-220 package. Because of the lower voltage and smaller size, lower cost can be realized.

2. Requires more complex drive circuit for the upper of the two transistors.

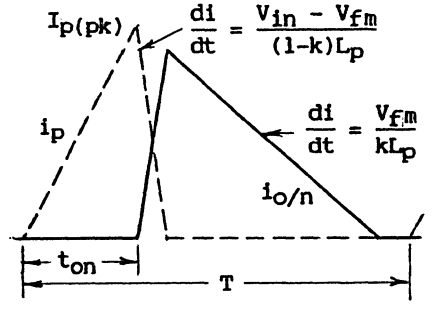
ENERGY TRANSFER IN THE FLYBACK CONVERTER -- LEAKAGE INDUCTANCE EFFECTS

In a flyback converter operated in the discontinuous mode, the energy stored in the flyback transformer (actually an inductor) must be zero at the beginning and end of each switching period. During the "on" time, energy taken from the input is stored in the transformer. When the switching transistors turn off, this stored energy is all delivered somewhere -- mostly to the output. However, the transformer leakage inductance causes much of the stored energy to be dumped into the primary side snubber or clamp, diverting it from the output. The leakage inductance dumps not only its own energy, but also causes much of the energy stored in the mutual inductance to be diverted into the clamp circuit. The amount of energy diverted is typically 15-25% of the total energy stored. In the two-transistor circuit, this diverted energy is returned to the input so the efficiency is not hurt, but peak primary current is greater and the total stored energy in the flyback transformer must be increased.

The amount of energy returned depends upon the transformer turns ratio as well as its leakage inductance. To explain the power transfer process, the simplified equivalent converter circuits during "on" and "off" times are shown in Fig. 3.



3A - "On" time 3B - "Off" time



3C - Current Waveforms

When switches Q1 and Q2 are closed as shown in Figure 3A, energy from the input filter capacitor is transferred to the transformer primary mutual inductance, kL_p, and the leakage inductance, $(1-k)L_p$, where k is the coupling coefficient between primary and secondary. The total energy stored equals $1/2\ LI_p^2$. Energy cannot be transferred to the secondary side at this

time because the output rectifiers are reverse biased.

During the "off" time (see Figure 3B), the current established in the inductor forces the transformer voltage to reverse, or "flyback", until the output rectifier D3 conducts and hopefully transfers the energy stored in the mutual inductance to the output. The current flowing in the leakage inductance causes its voltage to reverse an *additional* amount so that clamp diodes D1 and D2 conduct. This transfers the leakage inductance energy back to the bulk input filter capacitor. Unfortunately, the leakage inductance also causes some of the *mutual* inductance energy to be returned to the input through D1 and D2. This is because whatever current flows in the leakage inductance forces the same current flow on the primary side through the mutual inductance. Thus the leakage inductance delays current transfer to the secondary (see Fig. 3C) and diverts a substantial portion of the mutual inductance energy back to the input. This diversion of energy raises peak primary currents and requires a larger flyback transformer which must store more energy for the same output power. Energy diversion is reduced by making the leakage inductance smaller and by providing a large additional flyback voltage across the leakage inductance so as to reset its current to zero as rapidly as possible.

As shown in Figure 3B and 3C, during the "off" time the output voltage, V_O, and forward rectifier drop, V_f, are reflected across the mutal inductance on the primary side by the transformer turns ratio, $n = N_P/N_S$. The flyback voltage across the mutual inductance is:

(1) $$V_{fm} = n(V_O+V_f).$$

The voltage across the entire primary side inductance L_P is clamped by diodes D1 and D2 to the supply voltage V_{in}. The flyback voltage, $V_{f\ell}$, which resets leakage inductance $(1-k)L_P$ is therefore:

(2) $$V_{f\ell} = V_{in} - V_{fm} = V_{in} - n(V_O+V_f)$$

Referring to Fig. 3C, the time required for the current through the primary side leakage inductance to reach zero is proportional to $V_{f\ell}$. This determines how fast the current can transfer to the secondary side and therefore the amount of mutual inductance energy that will be transferred to the output rather than being diverted into the clamp (see Fig. 3C). Equation 3 shows the total flyback transformer energy, W_L, required to make up for losses and for energy diverted back to the input:

(3) $$\frac{W_L}{W_{out}} = \frac{W_L f_s}{P_{out}} = \frac{1-V_{fm}/V_{in}}{n(k-V_{fm}/V_{in})}$$

Higher efficiency, n, and better transformer coupling, k, improve the energy transfer and reduce the stored energy required in the transformer. The leakage inductance in a flyback transformer with high voltage insulation is typically 5% of the primary inductance, corresponding to a k of 0.95. A smaller turns ratio decreases V_{fm} which increases reset voltage $V_{f\ell}$ across the leakage inductance, reducing the energy diverted back to the input.

However, the smaller V_{fm} decreases duty ratio D and increases peak primary current, $I_{p(pk)}$, at a given power output:

(4) $$D = \frac{1}{1+kV_{in}/V_{fm}} ; \quad D_{max} \text{ (at mode boundary) occurs at min } V_{in}$$

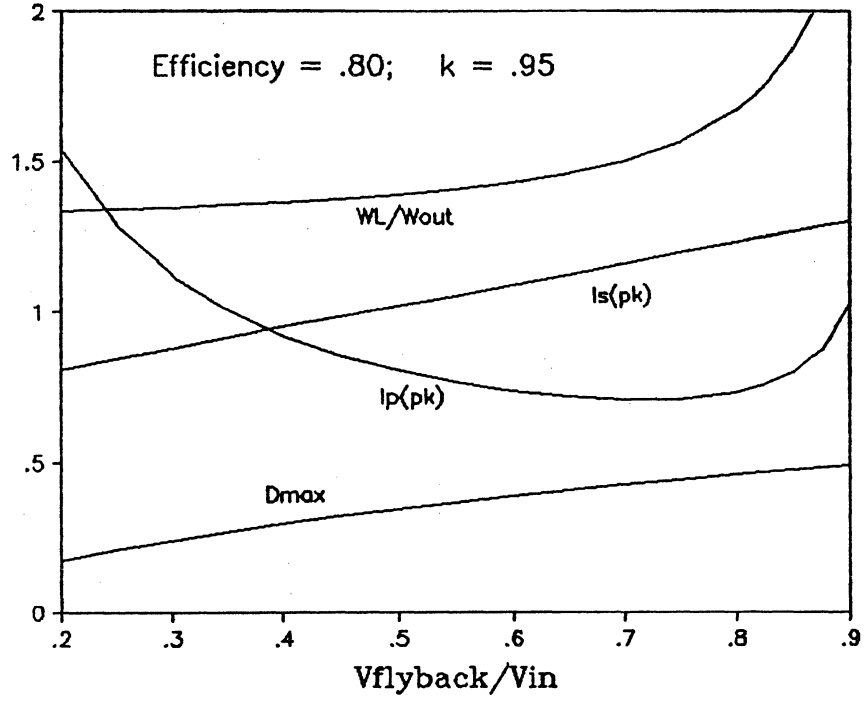
(5) $$I_{p(pk)} = \frac{2\ W_L\ f_s}{V_{in}\ D}$$

On the other hand, smaller V_{fm} *reduces* peak currents on the secondary side, $I_{s(pk)}$:

(6) $$I_{s(pk)} = \frac{2\ I_{out}}{(1-D)}$$

Figure 4 shows the values calculated from Equations 3 - 6: W_L/W_{out}, D_{max}, $I_{p(pk)}$, and $I_{s(pk)}$, plotted against the ratio V_{fm}/V_{in}. Note that $i_{p(pk)}$ and $I_{s(pk)}$ are calculated at minimum V_{in} and maximum P_{out} values and are plotted on a *relative* basis. These curves suggest that a good design compromise is to use a transformer turns ratio such that $n(V_{out}+V_f) = V_{fm}$ is approximately 1/2 of the worst case minimum V_{in} at low line voltage. The energy transfer process will be more efficient at line voltages above the minimum because V_{fm} remains constant but reset voltage $V_{f\ell}$ across the leakage inductance becomes larger.

Figure 4. Peak Current and Energy Requirements vs. Clamp Ratio.



DESIGNING THE INPUT RECTIFIER AND FILTER

Refer to Design Reference Section I1, "Line Input AC to DC Conversion and Input Filter Capacitor Selection". The input circuit may be connected as a voltage doubler from the 120 V line or as a full-wave bridge from the 230 V line. In either case the input bulk filter capacitors must store enough energy to provide 200 Vdc minimum to the switching converter during the milliseconds that the instantanteous AC line voltage is below 200 V.

Section I1, Table I shows that for a 100 Watt input supply in the worst case doubler configuration, two 160 µF capacitors maintain the required 200 V at mimimum RMS line voltage. The full load input power required for 150 Watt output is 150/η, or 187.5 Watts. This requires 160x187.5/100, or 300 µF for each voltage doubler capacitor. Considering tolerances and temperature coefficients of aluminum electrolytic capacitors, 450µF is used. Peak repetitive charging current from Table I is 3.28x187.5/100 = 6.15 A. RMS charging current is 1.126x187.5/100 = 2.11 A.

DESIGN OF THE POWER INVERTER

Table A below shows the winding turns definition that comes reasonably close to achieving the desired output voltages and the desired 100 V primary side flyback voltage (approximately 1/2 of the 200 V minimum V_{in}):

TABLE A:	Winding	Turns	Vfm	$V_{out}+V_f$	V_f	V_{out}
	Primary	36	100.8			
	5 V, 15A	2		5.6	0.6	5.0
	12 V, 3A	5		14.0	1.0	13.0
	24 V,1.5A	9		25.2	1.0	24.2
	16 V Aux.	6		16.8	.8	16.0

The 16 V Auxiliary output provides power for the control and gate drive circuits. It is not closely coupled to the other secondaries because it is on the primary side of the isolation boundary, so its load regulation is an acceptable 20%. The 12 volt secondary provides 13 V, allowing 1 Volt of headroom for the linear post-regulator which achieves 3% regulation.

During the flyback time all windings will have 2.8 Volts per turn. The turns ratios between secondaries are critical because they determine the output voltage ratios. Each winding must have an integral number of turns, making it impossible to use fewer secondary turns than Table A without hurting the output voltage ratios. The number of primary turns is not as critical because flyback voltage V_{fm} is not rigidly defined. Obviously the number of turns could be any integral number times the values given above.

The total maximum energy storage, W_L, required in the primary inductance of the flyback transformer at full load output and minimum V_{in} is:

$$(3R) \quad \frac{W_L}{W_{out}} = \frac{W_L f_s}{P_{out}} = \frac{1-V_{fm}/V_{in}}{\eta(k-V_{fm}/V_{in})} = \frac{1-100/200}{0.8(.95-100/200)} = 1.3889$$

$$W_L = 1.3889 \times P_{out}/f_s = 1.3889 \times 150/100{,}000 = 2083\ \mu J$$

From Equation 4, the maximum duty ratio and t_{on} at min. V_{in} are calculated:

$$(4R) \qquad D_{max} = \frac{1}{1+kV_{in}/V_{fm}} = \frac{1}{1+.95x200/100} = .3448$$

$$\max t_{on} = DT = D/f_s = .3448/100{,}000 = 3.448\ \mu sec$$

The maximum peak primary current is, from Equation 5:

$$(5R) \qquad I_{p(pk)} = \frac{2\ W_L\ f_s}{V_{in}\ D} = \frac{2x2083x0.1}{200x0.3448} = 6.04\ A$$

The primary current limit need not exceed 6.04 A because it represents a combination of worst case conditions that are not likely to coexist. For example, with minimum V_{in} slightly larger than 200 V (because the bulk filter capacitors are larger than required), less energy is returned to the source, so that less inductor energy and less $I_{p(pk)}$ is required for full load output.

The total primary inductance required is:

$$(7) \qquad L_p = 2\ W_L/I_{p(pk)}^2 = 2x2083/6.04^2 = 114.2\ \mu H$$

Transformer Design: Design Reference Section M6, "Filter Inductor and Flyback Transformer Design for Switching Power Supplies", defines the approach and the equations used. An EC41 core is chosen based on operating frequency, maximum flux density and hot spot temperature rise limitations.

At 100 kHz operating frequency, the maximum flux density, B_{max}, is limited by core losses, not magnetic saturation. The EC41 core has an effective thermal resistance of 16.5°C/W to the centerpost hot spot. An acceptable hot spot temperature rise of 33°C allows 2 Watts total dissipation -- 1 Watt winding and 1 Watt core losses. Since the EC41 core volume is 11 cm^3, 1 Watt total core loss equals .091 W/cm^3. This occurs with a flux density swing of 0.155 Tesla (1550 Gauss) at 100 kHz, from the core loss data in Design Reference Section M3. Flux remnance is nearly zero at the beginning of each switching period because of the air gap used to store energy in the flyback transformer. Therefore the 0.155 Tesla flux density swing results in B_{max} of 0.155 T for normal conditions at full load. Under the temporary conditions requiring maximum stored energy at V_{in} = 200 V, B_{max} is allowed to reach 0.17 Tesla.

The *minimum* number of primary turns, N_p, needed to store the worst case energy requirement at minimum V_{in} without exceeding 0.17 T flux density is:

$$(8) \qquad N_{p(min)} = \frac{L_p\ I_{max}}{B_{max}\ A_e} = \frac{114x10^{-6}x6.04}{0.17x1.25x10^{-4}} = 32.4\ ; \quad N_p = 36\ turns$$

Referring back to Table I, N_p must be 36 turns or an integer multiple such as 72 or 108. The 32.4 turns defined in Eq. 8 is the *minimum* N_p, so 36 turns is the obvious choice. This will require a slightly larger gap to obtain the desired inductance. The flux swing and core losses will be less than would be obtained with $N_{p(min)}$, but winding losses will be greater.

The actual flux swing can be recalculated from Eq. 8, plugging in 36 turns and solving for B_{max} = 0.153 Tesla. In this case, N_p is not much more than $N_{p(min)}$ and there will be little increase in total transformer dissipation and temperature rise. If N_p had to be much larger than $N_{p(min)}$, winding losses would be much higher and might force the use of a larger core size.

The core center-post is ground to the desired gap length calculated by the classic inductance formula, using the actual N_p of 36 turns:

(9) $\ell_g = \mu_o N^2 A_e / L_p = 4\pi x10^{-7} x36^2 x1.25x10^{-4} / 114x10^{-6} = .00178 \text{ m} = .178 \text{ cm}$

The required gap can also be obtained without grinding the center-post by spacing the core halves apart by one-half the total gap. This puts half the gap in the center-post and half in the outer legs of the core (provided the combined area of the outer legs is the same as the center-post area). Using this method, considerable magnetic field is propagated outside the core, and EMI problems may be worsened.

Designing the Windings: AC eddy current losses (skin effect and proximity effect) will be very significant in the 100 kHz flyback transformer unless the windings are designed specifically to minimize these effects. The skin or penetration depth, Δ = .024 cm at 100 kHz, so even a single layer of AWG 24 starts to incur AC losses. Another major concern is to minimize the leakage inductance between primary and secondaries, in spite of the high voltage isolation requirements which force them to be physically separated. Good coupling between secondaries is easier to achieve because they may be co-mingled or even wound multifilar.

First, the 36 turn primary winding is split into two 18 turn portions. The secondaries are in a single closely coupled group. One primary portion is wound around the center post inside of the grouped secondaries, the other primary portion is wound on top of the secondaries. This interleaving results in a dramatic reduction of the magnetic field (energy) between the windings. Leakage inductance between primary and secondary, $L_p(1-k)$, is reduced by a factor of 3, and there is a similar beneficial effect in reducing eddy current losses in both primary and secondaries.

Second, windings are made up of many paralleled wires with diameters less than 2 times the penetration depth, Δ, so that AC current is not excluded from the central portions of the conductors. Thin copper strip may also be used for the same purpose in low voltage, high current windings.

The total cross-section area of all windings is limited by the core window area, A_W = 2.15 cm^2 for the EC41 core. Much of the window area is wasted, taken up by insulation around wires, voids between round wires, insulation between winding portions, and necessary creepage distance at the ends of the windings. Window utilization factor, k_u = 0.4 is the fraction of the window area that is actual conductor. All windings in the flyback transformer are single ended, so that winding losses are minimized by apportioning equal winding cross-section areas to the primary and to the group of secondaries, hence primary area factor, k_p = 0.5. The maximum primary conductor area available is:

(10) $A_p = A_w \cdot k_u \cdot k_p = 2.15x0.4x0.5 = 0.43 \text{ cm}^2$

The average length of each turn around the core is ℓ_t = 6 cm (otherwise known as MLT -- mean length per turn). The total length of the entire 36 turn primary is then 6x26 = 216 cm. The RMS primary current, I_p, is:

(11) $$I_p = I_{p(pk)} \cdot (D_{max}/3)^{1/2} = 6.04x(.345/3)^{1/2} = 2.05 \text{ A}$$

Total power dissipation allowed in all windings is 1 Watt, so the primary may dissipate 0.5 watts. The maximum resistance of the primary winding is therefore:

(12) $$R_p = P_p/I_p^2 = 0.5/2.05^2 = 0.119 \text{ Ohms}$$

$$R_p/cm = 0.119/216 = .000551 \text{ Ohms/cm}$$

AWG 21 copper wire comes close to this with .000561 Ohms/cm at 100°C. But a single layer (after interleaving) of AWG 21 at 100 kHz has an AC resistance factor, $F_R = R_{ac}/R_{dc}$ of 2.45, which more than doubles the loss.

An acceptable F_R value of 1.4 is obtained by using 7 AWG 29 wires paralleled in place of a single AWG 21 wire. The 7 wires are twisted together into a 7-strand cable, or Litz wire, with 6 outer strands packed in a hexagonal pattern about the 7th central strand. The DC resistance of the paralleled strands is .000512 Ohms/cm, less than a single AWG 21 conductor. The 36 turn primary is wound with 18 turns of the seven strand cable inside the secondaries and 18 turns top of (outside) the secondaries. The breadth of the winding window in the EC41 core is 2.78 cm. The 18 turns of 7-strand cable will occupy the central 1.75 cm of the window, leaving plenty of creepage distance.

Peak and rms secondary currents are proportional to the DC output currents as follows. The results of these calculations are given in Table B below:

(6R) $$I_{s(pk)} = 2 \cdot I_{out}/(1-D_{max}) = 3.05 \cdot I_{out}$$

(13) $$I_s = I_{s(pk)} \cdot ((1-D_{max})/3)^{1/2} = .467 \cdot I_{s(pk)}$$

The conductor area for each winding is proportioned to operate at the same rms current density as the primary. The results are shown in Table B.

TABLE B WINDING DATA

Winding	$I_{s(pk)}$	Irms	Area(cm^2)	Configuration
Primary		2.05	.0041	18+18 turns, 7xAWG29
5V, 15A	45.75	21.36	.0429	2 turns, .025x1.75 cm strip
12V, 3A	9.15	4.27	.0086	5 turns, 2 - 7xAWG29 paralleled
24V,1.5A	4.58	2.14	.0043	9 turns, 7xAWG29
16V Aux	.21	.05	.0001	6 turns, AWG 29

Three layers of 1 mil mylar tape (.016 cm - 6.6 mil incl. adhesive) are used to meet VDE 3750 V isolation requirements, applied between the two primary halves and the secondary bundle.

Copper strip is used for the two turn 5 Volt secondary. The thickness of the strip is comparable to the skin depth, Δ, so that F_R is only slightly

greater than 1.0.

Note that the same 7-strand AWG29 cable is used for the primary and the 12 and 24 Volt secondaries. The 12 and 24 Volt windings are mingled in a single layer as follows: Four lengths of cable -- A, B, C, and D are wound simultaneously side by side for 5 turns. This results in a single smooth layer 20 cable diameters wide across the winding breadth, in the sequence A,B,C,D,A,B,C,D,A....etc. A and C are paralleled for the 5 turn 12 Volt output. One turn is taken off D, leaving a total of 19 cable diameters across the winding. The 5 turns of B are put in series with the 4 turns left in D for the 9 turn 24 Volt output.

The 16 Volt auxiliary windings are put on last, spread over the outer half primary. The auxiliary winding must be separated from the other secondaries because of the line isolation requirements.

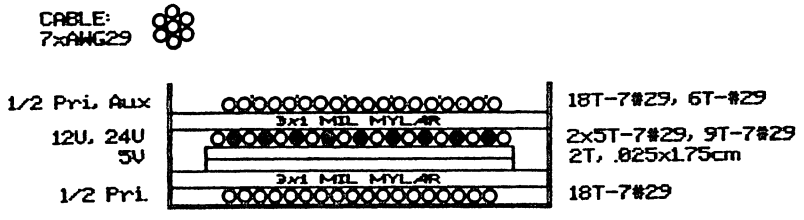


Figure 5. Transformer Winding Layout

Output Filter Capacitors: Aluminum electolytic capacitors have the lowest cost and are therefore most widely used in commercial/industrial supplies. Filter capacitor selection is dominated entirely by the ESR (Equivalent Series Resistance) necessary to obtain acceptable peak-peak ripple voltage.

$$ESR_{max} = V_{ripple}/I_{S(pk)}$$

Table C shows the parameters and results of the capacitor selection process:

TABLE C -- OUTPUT FILTER CAPACITORS

Output	V_{ripple}	$I_{S(pk)}$	ESR_{max}	Capacitor Selection
5V, 15A	0.3	45.75	.0066	(5) 2200 µF, 16 V, Panasonic HF
12V, 3A	0.3	9.15	.033	(1) 2200 µF, 16 V, "
24V,1.5A	0.5	4.58	.11	(1) 220 µF, 50 V, "
16V Aux	0.3	.21	1.42	(1) 47 µF, 25 V, "

The 5 Volt output ripple voltage is further reduced to below 0.1 V by the additional L-C filter section (actually L-R because of ESR). The 160 nH inductor is 0.1 Ω at 100 kHz, and the additional 2200 µF capacitor has an ESR of .03 Ω, for a ripple reduction factor of 3.3.

CONTROL AND GATE DRIVE CIRCUITS:

The auxiliary supply provides an average current of 50 mA to power the UC3842 control IC and power MOSFET gate drive circuits. The auxiliary supply is maintained from the 7 turn auxiliary winding on T1 through an 18 Ω resistor which limits the peak charging current and prevents the supply from charging to the high peak voltage of the leakage inductance spike.

During initial startup of the supply, the UC3842 undervoltage lockout disables the control and drive circuits so that the total current drawn is less than 1 mA. This enables the 47K resistor from the input bulk filter to initially charge the auxiliary supply capacitor to 16 volts, where the circuit comes alive and starts the converter. It takes 200 - 300 switching periods for the output voltages and the T1 auxiliary winding voltage to rise to normal levels and recharge the aux supply capacitor, so the capacitor must be large enough to supply 50 mA for 300x10μs without dropping below 11 Volts (where the UC3842 turns off).

The totem pole output of the UC3842 drives the gates of the two MOSFETs through transformer T2, consisting of three 20 turn windings of AWG 30 wire on a 1/2 inch O.D. ferrite toriodal core, 204XT250, 3E2A material. The three wires are wound together (trifilar). High voltage insulation between primary and secondaries is not needed, as all windings are on the same side of the isolation boundary.

Primary current in T1 is sensed by a 0.16 Ω resistor. This current sense voltage is applied through a spike filter to the current sense terminal of the UC1840, where it is compared against the amplified output error voltage. The comparator input voltage is clamped to 1 V, which effectively limits the peak primary current to 1/0.16 = 6.25 A and indirectly limits the duty ratio. The error amplifier output (pin 1 - Compensation) must swing from 1 to 4.5 Volts in order to swing the comparator input from 0 to 1 Volt for full range control of the current. This is because there are two forward diode offsets and a 3 to 1 divider between the error amplifier output and the comparator input within the IC.

The 30K feedback resistor and 10K input resistor together establish an error amplifier gain of 3. Combining this with the 3/1 divider at output of the error amplifier results in an overall gain of 1 from the input of the 10K resistor to the current control comparator. The inverting input of the error amplifier normally sits at 2.5 V. This makes it necessary to provide +1.8 V bias to the input demodulator so that the input will swing from 1.8 to 3.0 V in order to swing the output full range from 4.5 to 1 V.

A UC3901 isolated feedback generator compares the 5 volt output against an internal reference, amplifies the resulting error and uses it to amplitude modulate a 2 mHz carrier. This signal is easily coupled through a tiny isolation transformer T3 back to the primary side where it is demodulated and the error voltage recovered and applied to the UC3842 error amplifier input. Transformer T3 has two 15 turn, AWG 30 windings on the same 1/2" O.D. epoxy coated ferrite toriodal core (204XT250, 3E2A material) used for T2. These windings must be wound individually on opposite sides of the core to provide 3750 Volt isolation. Although the coupling is hurt because the windings are not distributed uniformly around the entire core, leakage inductance in this application is not critical.

CLOSING THE FEEDBACK LOOP:

The 5 Volt output has the most critical regulation requirement. and is used as the basis for closed loop control. The 12 Volt output uses a simple linear post-regulation technique to achieve better than 3% regulation. The 24 Volt output achieves better than 10% line and load regulation by simply tracking the 5 Volt output without additional post-regulation.

The feedback loop design approach is taken from Design Reference Section C1 - "Closing the Feedback Loop". The Bode plot of Figure 6 shows the overall loop gain and phase, along with its two major components -- the control to output gain and the feedback circuit gain.

The overall loop gain Bode plot shows the 0 dB crossover frequency to be 8.4 kHz. The solid lines show the gain and phase with maximum filter capacitor ESR. Minimum ESR, shown in the dash lines, is assumed to be 1/5 of the maximum. The worst case phase shift of 135 degrees which occurs with minimum ESR provides an adaquate phase margin of 45 degrees. The gain of 333 (50 dB) below 60 Hz is sufficient that a .015 Volt error on the 5 Volt output swings the output over its full range, which is much better than the 1% regulation required.

The control to output portion of the loop gain includes the current control comparater and pulse width modulator in the UC3842, the power switching circuit, flyback transformer and filter. The formulae from which the plots were calculated are from Design Reference Section C1, Appendix C, pages 5 and 6. These equations give no consideration to the power transformer turns ratio, so the control to output gain must be multiplied by n = 36/2. (These equations apply to current mode control, and the current is stepped up.)

Before beginning the calculations, the primary inductance, filter capacitance and load resistance values are all referred into the 5 Volt output according to their respective turns ratios squared:

$$C' = 2200x6 + 2200x(5/2)^2 + 220x(9/2)^2 = 31400\ \mu F$$

$$ESR' = .03x2200/31400 = .002\ \Omega\ max,\ .002/5 = .0004\ \Omega\ min$$

$$R_O' = V_O^2/P_O = 5^2/150 = .1667\ \Omega\ min;\ = 5^2/75 = .333\ \Omega\ max$$

$$L' = L_p/n^2 = 114.2/(36/2)^2 = 0.352\ \mu H$$

$$k = I_{p(pk)}/maxV_C = 6/1 = 6 \quad (6A\ controlled\ by\ 1V\ comparator\ swing)$$

Below 60 Hz, the control to output gain at full load is 14 dB:

$$(14)\quad v_O/v_C = nK(R_O'L'f/2)^{1/2} = 18x6x(.1667x.352x0.1/2)^{1/2} = 5.85$$

Considering losses, actual gain will be slightly less -- assume gain of 5, or 14 dB. The gain rolls off above 60 Hz with a single pole characteristic (-20 dB/decade with -90° phase shift). This pole frequency is determined by output filter capacitance and load resistance:

$$(15)\quad f_p = 2/(2\pi RoC) = 2/(2\pi x.1667x.0314) = 60.8\ Hz$$

At 2400 Hz, a zero is encountered attributable to the maximum ESR of the filter capacitor. This zero cancels the pole, flattening out the gain and bringing the phase lag gradually back to zero.

(16) $f_Z = 1/(2\pi x ESR x C) = 1/(2\pi x.002x.0314) = 2413$ Hz (ESR max)
$= 1/(2\pi x.0004x.0314) = 12670$ Hz (ESR min)

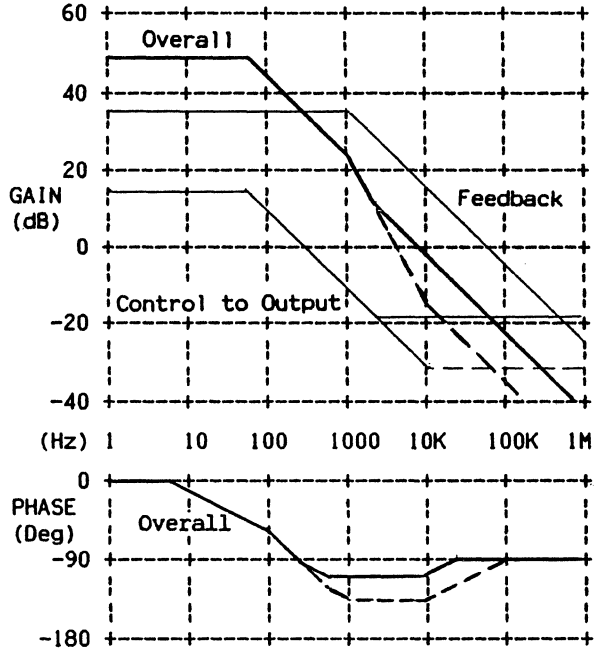


Figure 6. Loop Gain Bode Plot

Stability considerations dictate that the overall loop gain must cross 0 dB below 1/4 or 1/5 of the switching frequency. In designing the gain of the feedback circuits, it is necessary to add a pole to compensate (cancel) the ESR zero, otherwise the ESR zero would cause the overall loop gain to flatten out and not cross 0 dB as required. If the compensating pole is put exactly at the ESR zero frequency, the overall loop gain will have a single pole -20 dB/decade slope with -90' phase shift from 60 Hz to well above 100 kHz. The phase margin would be 90', which is much more than necessary. The overall low frequency loop gain can be increased by putting the compensating pole *below* the ESR zero frequency. This results in a 2 pole slope between the compensating pole and the ESR zero, increasing phase shift and reducing phase margin. A pole frequency of 1 kHz is used in this design, which reduces the phase margin to 45' with the worst case *minimum* ESR.

The control to output gain at 20 kHz is -18 dB. To set the crossover frequency at 20 kHz ($f_S/5$) requires +18 dB feedback circuit gain. However, this causes another problem: With feedback circuit gain of +18 db at 20 kHz, decreasing 20 dB/decade as it must to compensate the ESR zero, the feedback gain is 4 dB at the 100 kHz switching frequency. There is nearly 0.3 V of switching frequency ripple at the 5 Volt output where it is sampled

for feedback control. The 0.3 Volts ripple will be amplified 4 dB to 0.48 Volts by the feedback circuit and applied to the current sense comparator in the UC3842 along with the amplified output error voltage. The sawtooth waveform representing primary current at the other input of the comparator is a *maximum* 1 Volt amplitude at full load, and 0.5 Volts at 1/4 load. The 0.48 Volts of 100 kHz ripple will cause erratic behavior of the modulator at moderate load levels. Solving this problem requires lower feedback circuit gain at 100 kHz, which lowers the gain at all frequencies and reduces the crossover frequency. In this application, 0.2 Volts ripple amplitude at the current sense comparator input is acceptable, which dictates a feedback circuit gain of 2/3, or .667 (-3.5 dB) at 100 kHz. Thus the gain is 7.5 dB (2.37) less than originally attempted, and the crossover frequency is 2.37 less, or 8.4 kHz. With a gain of .667 at 100 kHz, the feedback circuit gain at the pole frequency, 1 kHz, is .667x100K/1K = 66.7 (36 dB).

As stated earlier, the gain from the demodulator at the input of the UC3842 to the input of the current sense comparator is 1 (0 dB), to well above 100 kHz. The AC gain through the coupling transformer and demodulator is also 1. The gain of the driver section of the UC3901 isolated feedback generator is fixed at 4. The 100K feedback resistor around the UC3901 error amplifier together with the 6.2K input resistor to provides a gain of 16.5, for a total gain of 16.5x4 = 66, as required. the .0015 µF across the 100K resistor establishes the 1 kHz pole frequency.

PROPORTIONAL BASE DRIVE OF BIPOLAR POWER TRANSISTORS IN SWITCHING POWER SUPPLIES

Proportional base drive is a simple and effective method of achieving improved performance with high voltage bipolar power switching transistors in off-line applications. As shown in Figure 1, a current transformer provides regenerative base drive current whose amplitude is proportional to the collector current being switched. The drive current ratio is established by the turns ratio of the collector and base windings.

The proportional drive method may be employed with any power switching circuit topology. Advantages over conventional fixed base current drive methods include:

1. Fixed base drive current must be large enough to handle the full load (or short-circuit load) collector current. Under lightly loaded conditions, the switching transistors are severely overdriven, resulting in long storage and fall times and more difficult turn-off. Proportional drive provides optimal performance under varying load current conditions.

2. Proportional base drive requires less drive power from the control circuit. During the "on" time of the switching transistor, base drive is provided regeneratively from the collector circuit through the current transformer. The control drive circuit is not required to provide sustaining base drive current. It must only provide short pulses of drive current to initiate turn-on and turn-off. The amplitude of these drive current pulses can easily be made large enough to obtain good switching performance from high voltage bipolar devices in off-line applications.

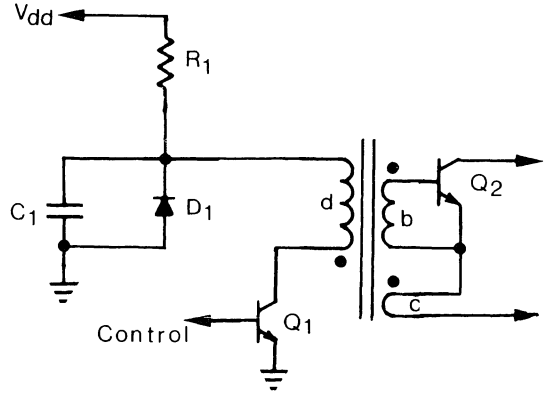


Figure 1. Proportional Base Drive Circuit

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Referring to Figures 1 and 2, when driver transistor Q_1 is on, power switch Q_2 is off. Magnetizing current I_{d1} in the control drive winding N_d approaches a steady-state value equal to the drive circuit supply voltage V_{dd} divided by R_1. Capacitor C_1 is discharged and there is zero voltage across all windings of T_1.

When the output of the control circuit turns on, driver Q_1 turns off and primary current I_{d1} must cease. Energy stored in T_1 causes the voltage at the dotted ends of all windings to flyback in the positive direction. I_{d1} multiplied by turns ratio N_d/N_b becomes I_{b1}, the turn-on base drive current pulse to Q_2.

Collector current I_c starting to flow in winding N_c causes a regenerative increase in base drive to Q_2 until it is switched fully on. The final value of I_c induces a proportional base drive current, I_b, according to the turns ratio N_b/N_c.

During the time that Q_2 is on and Q_1 is off, capacitor C_1 charges through R_1 to supply voltage V_{dd}. At the end of this "on" period, driver transistor Q_1 is turned on again, applying the voltage on capacitor C_1 to the drive transformer primary. This drives the voltage on the base of Q_2 sharply negative. The turn-off base current pulse, I_{b2}, can be made larger than Q_2 collector current, resulting in very rapid turn-off of Q_2.

After Q_2 is off and I_{b2} ceases, any remaining voltage on C_1 across the drive transformer primary helps to rebuild the magnetizing current. Diode D_1 prevents the possibility of any underdamped ringing from driving the upper end of N_d negative. At the end of the "off" period, magnetizing current I_{d1} has been re-established and the cycle repeats.

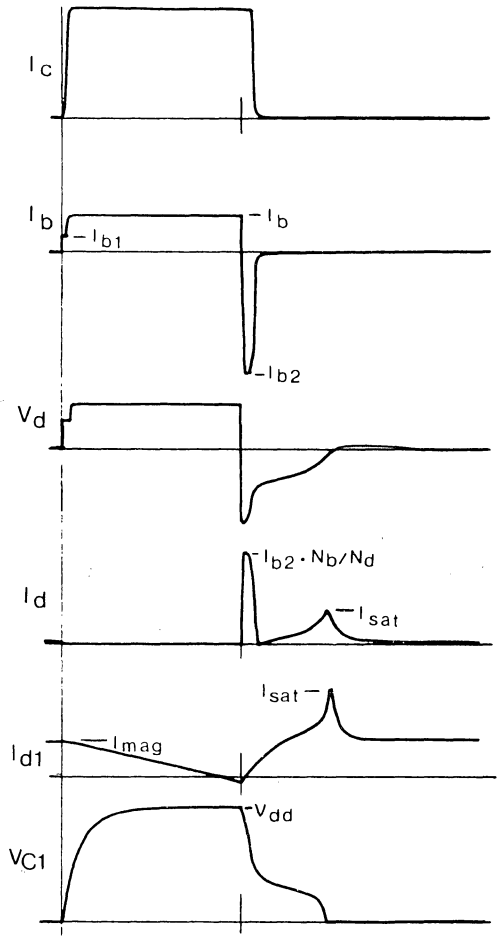

Figure 2. Waveforms

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It is quite feasible to operate high voltage bipolar transistors at frequencies above 50 KHz with reasonable efficiency because of the large amplitude base drive pulses obtainable with this method. However, the circuit of Figure 1, as just described, is not capable of operation at frequencies above a few kilohertz. This is because capacitor C must charge to V_{dd} during the "on" period of Q_2, and the R_1C_1 charging time constant is far too long for this to be accomplished at 50 KHz.

This problem is solved by the addition of a rapid recharge circuit as shown in Figure 3. During the time that Q_2 is on and Q_1 is off, current through R_1 is multiplied by the current gain of Q_3, which significantly reduces the charging time of C_1. When Q_1 turns on, C_1 discharges through D_2. The base-emitter of Q_3 is reverse biased, holding it off during the entire Q_2 "off" time.

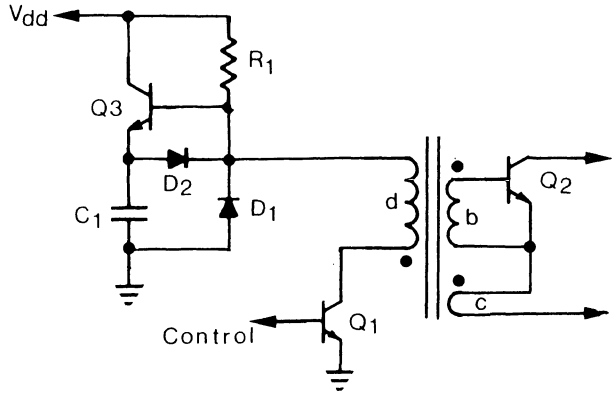

Figure 3. Improved Proportional Base Drive Circuit

DESIGN PROCEDURE:

Application parameter values must be defined, including drive requirements for the power switching transistors:

I_c	Maximum collector current
I_{b1}	Initial turn-on base drive current
I_c/I_b	Sustaining proportional base drive ratio
I_{b2}	Turn-off base drive current at max. I_c
V_{bb2}	Turn-off base drive source voltage at max. I_c
t_2	Maximum transistor turn-off time
V_{dd}	Drive circuit supply voltage
f	Operating frequency

Drive transformer base/collector turns ratio is equal to the desired proportional base drive ratio:

$$N_b/N_c = I_c/I_b \quad (1)$$

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Drive transformer driver/base turns ratio is established by the desired turn-off base source voltage and the drive circuit supply voltage, minus 1 volt diode drop:

$$N_d/N_b = (V_{dd}-1)/V_{bb2} \quad (2)$$

When Q_1 turns off, primary magnetizing current, I_{d1}, transferred to the base winding must provide the required turn-on base drive, I_{b1}.

$$I_{d1} = I_{b1}/(N_d/N_b) \quad (3)$$

The R_1 value required to obtain this magnetizing current is:

$$R_1 = V_{dd}/I_{d1} \quad (4)$$

During initial turn-off, driver primary current I_{d2} must absorb the proportional base drive current and transformer magnetizing current I_{d1} in addition to the turn-off base drive current:

$$I_{d2} = \frac{I_{b2} + I_a/(N_b/N_c)}{(N_d/N_b)} + I_{d1} \quad (5)$$

Capacitor C_1 is designed to supply the worst-case energy required to turn off Q_2:

$$W = \frac{1}{2}C_1(V_{dd}-1)^2 = (V_{dd}-1)I_{d2}\,t_2$$

$$C_1 = \frac{2\,I_{d2}\,t_2}{V_{dd}-1} \quad (6)$$

When Q_2 is operated at very low duty cycle (such as immediately after a sudden decrease in load current), C_1 may not have time to fully charge to V_{dd} during the very short "on" time, in spite of the assistance provided by Q_3. This will probably not be a problem, because Q_2 will also not have time to store much charge and will be much easier to turn off. The time required for Q_2 to reach equilibrium charge storage is comparable to the time required to remove this charge during turn-off. The C_1 charging time constant (reduced according to the gain, H_{fe}, of Q_3) will generally be adquate if it is less than 1/2 the Q_2 turn off time, t_2. C_1 charging time constant:

$$TC1 = R_1C_1/H_{fe} \quad (7)$$

DRIVE TRANSFORMER DESIGN:

Turns ratios for the drive transformer were established in equations (1) and (2). Only certain integral number of turns are permissible for each winding. For example, if N_d/N_c is 25, the permissible number of drive winding turns are 25, 50, 75, etc., corresponding to 1, 2, and 3 collector turns.

Winding I^2R losses are usually negligible. The drive transformer design is based on the following two considerations:

1. Magnetizing current I_{b1} is required for initial turn-on of the power switching transistor. During the time Q_2 is on, the magnetizing current will decrease due to voltage V_{be} across the base winding. The magnetizing current must not be allowed to decrease to less than zero, or it will cause premature turnoff under light load conditions by overcoming the small proportional drive current I_b. Referred to the primary, the drive winding inductance must be large enough to prevent I_{d1} (Equation 3) from reaching zero with voltage $V_{be}(N_d/N_b)$ during the longest possible "on" time (usually half the switching period, 1/2f):

2. Under light load conditions, relatively little charge is required to turn off Q_2. C_1 will then have substantial voltage remaining which will be applied to the drive winding during the remainder of the "off" period. This will cause the magnetizing current (and its associated energy storage) to become much larger than desired. The problem is solved by designing the drive winding to saturate at a current level slightly greater than the desired value of magnetizing current, I_{d1}. This will result in dumping any excess energy remaining in C_1 and establishing a consistent starting point on the B-H characteristic at the beginning of each "on" period.

Figure 4 shows the B-H characteristic of the core as seen from the drive winding. For the vertical axis, B times core area A_e and N_d equals $\int V_d dt$ (Faraday's Law). For the horizontal axis, H times effective core length, l, and divided by N_d equals the magnetizing current I_d, (Ampere's Law). The characteristic slope equals the drive winding inductance, L_d, and the area to the left equals the energy stored.

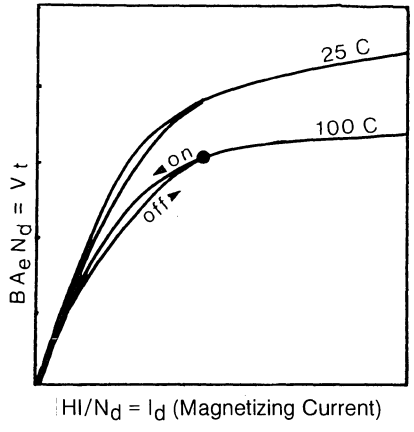

Figure 4.

The operating point shown will satisfy the two requirements above if it exceeds I_{d1} on the horizontal axis and if it exceeds $V_{be}(N_d/N_b)/2f$ on the vertical axis under worst case conditions at high temperature. Procedurally, use Faraday's Law with B close to saturation at high temperature and with the area, A_e, of the core selected. Solve for N_d:

$$\frac{V_{be}(N_d/N_b)}{2f} = B A_e N_d \qquad (8)$$

Use the smallest permissible N_d equal to or greater than the value calculated above. An N_d value larger than the calculated amount simply means that the change in flux density will be less than the maximum permitted.

Next, use Ampere's law with a value for H corresponding to the B value chosen before, the smallest permissible N_d from above, and I equal to I_{d1}. Solve for the magnetic path length, l.

$$N_d I_{d1} = Hl \qquad (9)$$

Compare the actual l_e value for the core selected with the value calculated above. If the actual l_e of the core is significantly larger than the calculated l, it will be necessary to use either a smaller core, or use a larger permissible number of turns, N_d. Otherwise, the operating point will not be close enough to saturation, and the B and H levels will both be too low to prevent the magnetizing current from becoming negative at the end of the "off" period.

If the actual core l_e is smaller than the calculated l, the core will be too heavily saturated, and will not store enough energy to provide the desired I_{b1}. Either go to a larger core, or introduce a small gap, lg, according to the relationship:

$$l = (l_e + \mu_a l_g), \quad \text{where } \mu_a = B/H \qquad (10)$$

Driving Two Transistors. Two power switching transistors are often used in series in order to halve their high voltage V_{ce} rating requirements. It is usually desirable to drive these two transistors from a single drive circuit. This can be accomplished by means of two identical base windings in the transformer. N_b/N_c must be halved and N_d/N_b doubled from the values calculated in Eq. (1) and (2) because the total base current is twice as much as with a single transistor.

As shown in Figure 5, it is also necessary to add a small amount of resistance in series with each base in order to ensure current sharing. A resistor which drops 0.5 volts at maximum sustaining base drive, I_b, should be adequate. The added resistance does not affect the calculation of N_d in Equation (8) because its voltage drop is negligible compared to V_{be} under light load conditions, when the sustaining base drive is small. However, during turn-off, each series base resistor must be shunted by a

small diode. Otherwise, a very large V_{bb2} value would be required in order to pull the desired I_{b2} out of each base. The forward drop of this diode must be added to the V_{bb2} requirement in Equation (2).

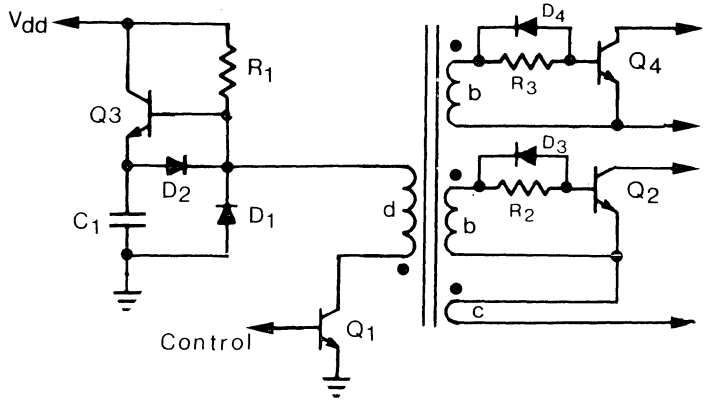

Figure 5. Two-Transistor Driver

Line-side vs Output-side Control Circuit. The base and collector windings of the drive transformer are normally on the input, or line side, of the power supply. When the control/driver circuits are located on the output side of the supply, high voltage insulation is required between the drive winding and the base and collector windings. This high voltage insulation, usually greater than 3000 volts, will impair the coupling between line-side and output-side windings. This results in high leakage inductance, causing voltage spikes during turn-on and turn-off which may necessitate additional snubbing or clamping the drive transistor collector and the power switching transistor base.

When the control and driver circuits are are located on the line side, the drive transformer does not require high voltage insulation. Leakage reactance can be made almost negligible, especially if multifilar windings are employed.

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(2) P. Wood, "High Efficiency, Cost Effective Off-line Switching Converters," TRW Applications Note 143, April 1978, pp. 3-4

(3) R. Severns, "A New Improved and Simplified Proportional Base Drive Circuit," Proceedings of POWERCON 6, May 1979, pp. B2(1-12).

PROTECTING CIRCUITS FROM TRANSIENT ENERGY SOURCES

Transient energy pulses are notorious among designers of all kinds of electronic hardware for their ability to cause failures in circuits of apparently conservative design. Logic circuits, for example, are subject to "glitches" and timing problems if even small transient voltages appear on supply lines. The problem is not limited to sensitive integrated circuits. Transient energy "spikes", either coupled from AC lines or internally generated in medium and high-power equipment, can generate blown fuses, misfired thyristors and other problems having various degrees of subtlety. Worse, unsuppressed transients can drive reverse biased semiconductor junctions into their highly dissipative breakdown regions. The heat generated at these junctions can then lead to the onset of second breakdown and permanent degradation or outright failure of semiconductor devices and the equipment of which they are a part. Even circuit failures of short duration or apparently minor importance can cause serious damage to the reputations of manufacturers and designers.

Fortunately, various devices exist for protecting circuits from damage due to transient energy pulses. The method chosen depends on the type of transient expected.

Transient Pulses Characterized

In terms of capability of causing damage, the key characteristics of a transient energy pulse are its total energy and energy distribution in time. A large amount of energy delivered in a short period of time is most damaging to semiconductor components. Unfortunately, total energies of transients from many sources are unpredictable. Figure 1 shows where transients produced by various common sources fall on a scale of energy predictability.

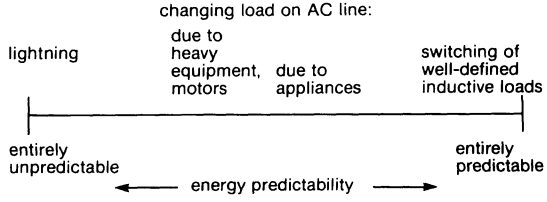

Fig. 1 Predictability of Common Transient Energy Sources

Some common transient energy pulses are quite unpredictable; still, designers want to protect their circuits from these transients as best as is practical. What, then, can be said to characterize these transients as much as is possible?

Figures 2a and 2b show generalized models which are widely useful in evaluating the effect that transient energy sources can have on circuit-protecting devices (transient suppressors). Some transient sources behave like voltage sources (Figure 2a), and can deliver to a transient suppressor currents which are limited only by the source-to-suppressor impedance. Other energy sources behave more like current sources (Figure 2b). One or the other of these models can help us to understand some of the kinds of transients shown in Figure 1.

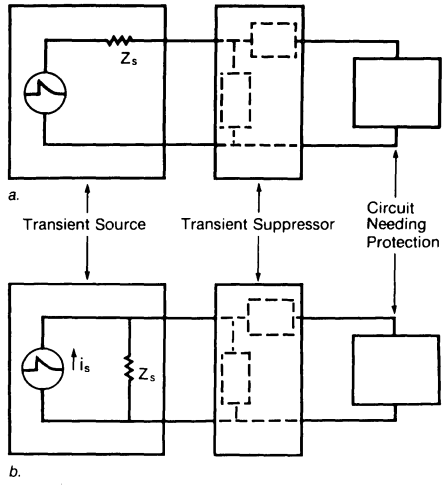

Fig.2 Transient Source Models
a. Voltage Source b. Current Source

Lightning is a voltage source having virtually unlimited available current. Voltages of 1kV to 100kV for 1μs to 50μs are typical at the point at which lightning strikes an AC power line. The source-to-suppressor impedance can be thought of as having two resistive components:

$$Z_S = R_{line} + R_{int}$$

where R_{line} is the resistance of the AC line between the strike point and the susceptible equipment, and R_{int} is any additional line-to-suppressor resistance internal to the equipment. Commonly, $R_{int} \approx 0\Omega$; the transient suppressor is directly across the AC line in the equipment. R_{line} depends very much on where the lightning strikes, and is, therefore, extremely unpredictable.

Transients produced on AC power lines due to sudden load changes differ qualitatively from those produced by lightning, and cannot easily be interpreted as arising from voltage sources. In fact, no simple model composed of discrete components is particularly useful in describing these transients, because their nature is determined by the complex distributed impedance of the AC line. In general, it can only be stated that energy stored in inductive components of the distributed line impedance—when some load is drawing current from the line—is released as transient energy when that load is switched off of the line. The transient so generated can then be thought of as arising from a current source and as having a peak amplitude that does not exceed the peak current drawn by any single piece of equipment located near the circuit being protected. Experience shows that these transients are typically less than 100ms in duration.

Up to this point, we have been discussing transients produced on AC power lines and have reached rather tentative conclusions. Transients generated internal to the equipment being protected are another matter and can be much better described and predicted. Designers simply know much more about the equipment they are designing than they do about AC power distribution systems or long-range meteorological forecasts. The generalized models of Figure 2 can be replaced by detailed schematic diagrams showing the transient sources and their connection to sensitive components. The tools of circuit analysis can be used to predict with great precision the power dissipation, as a function of time, required of a transient suppressor.

For example: bipolar transistors are commonly used to switch inductive loads in switching power supplies. Often the circuit has the basic form of Figure 3a. In this case, the danger is that the energy stored in the inductor while the transistor is on cannot safely be dissipated by the transistor after it turns off. The common method of protecting the transistor is to provide a voltage clamp which prevents the reverse biased collector-base junction being operated beyond breakdown. This, too, is shown in Figure 3a. Inductor current i_L is forced through the transient suppressor when the transistor is off. This i_L is about the same as just before turn-off, since the current through an inductor cannot change instantaneously. After that, i_L decreases at a rate determined by the inductor voltage v_L and the inductance value L:

$$\frac{di_L}{dt} = \frac{v_L}{L}$$

If the clamp voltage V_C is assumed constant until $i_L \approx 0$, then i_L behaves as in Figure 3b. The resultant transient suppressor current, voltage and power waveforms are as in Figure 3c.

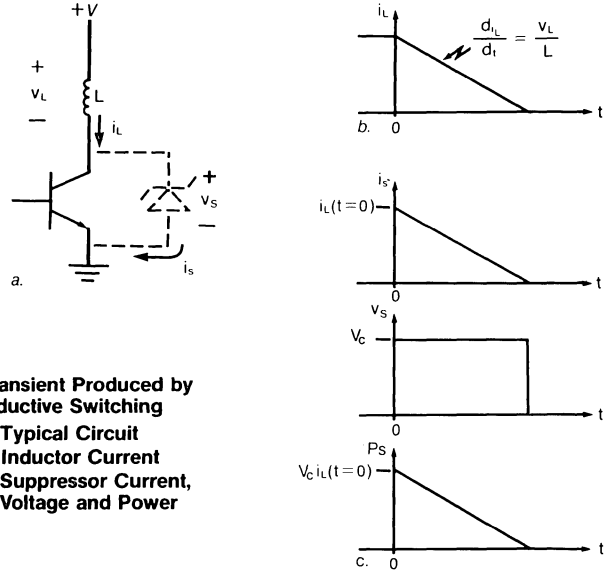

Fig.3 Transient Produced by Inductive Switching
a. Typical Circuit
b. Inductor Current
c. Suppressor Current, Voltage and Power

This type of internally generated transient is so common and its effects so precisely definable, that the current waveform it generates has become a standard waveform for testing transient suppressors. Figure 4 shows two specific linearly decaying waveforms used by manufacturers and users of semiconductor transient voltage suppressors. (The finite slopes of the leading edges of these waveforms reflect the fact that in a real circuit, di/dt is limited by wiring inductances and transistor fall times.) These test waveforms have the additional advantage that they can be closely approximated by an easily generated exponential waveform (see Figure 5).

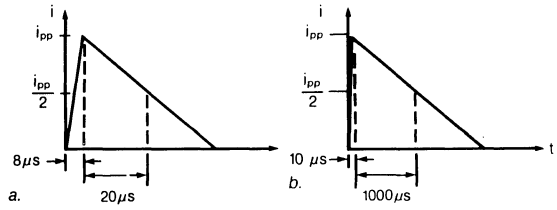

Fig. 4 Commonly used Test Waveforms
a. "8x20" μs
b."10 x 1000" μs

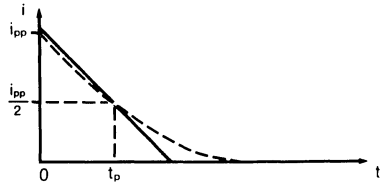

Fig. 5 Similarity of Triangular and Exponential Pulses

Desired Transient Suppressor Characteristics

In principle, it is possible to limit the transient energy that can be delivered to a sensitive component by limiting either the voltage or the current that that component can experience. In practice, however, transient current limiting is difficult to implement, and most designs employ some type of transient voltage suppressor (TVS) connected in parallel with the circuit to be protected. What, then, are the qualities required of a practical TVS?

First, a TVS must not interfere with the normal operation of the circuit; i.e., at voltages less than the maximum non-transient circuit voltage, a TVS must initially draw little current. We define that voltage at which a TVS can be guaranteed to draw less than some specified current as the stand-off voltage (V_R) for that current. A second requirement of the TVS is that it quickly clamps the voltage to a safe level when a transient does occur. Clamping voltage (V_C) is defined as the maximum voltage that will appear across the TVS under some pulsed current condition after the TVS has been fully activated. Clamping time (t_C) is the time it takes the TVS to activate. "Protected" circuits may experience voltages in excess of V_C during this defined clamping time. A figure of merit commonly used to describe TVSs is the clamping ratio (CR), defined by:

$$CR = \frac{V_C}{V_R}$$

An ideal clamp would have CR = 1.

A third TVS requirement is that it be capable of safely dissipating expected transient energy pulses. This capability is usually described in terms of allowable power dissipation as a function of pulse time.

Earlier, we discussed the predictability of various types of transients. Predictability greatly influences the process by which TVS power requirements are determined. For predictable pulses, the procedure is to minimize cost by specifying power requirements just safely in excess of the expected power for the known pulse duration. The design process is more complex for unpredictable transients. In this case, greater TVS power capability translates into great reliability. Therefore, the designer must make a trade-off between reliability and cost.

Other qualities desired of a transient voltage suppressor include freedom from the need to be "reset" after a surge and the ability to allow the protected circuit to function even during the transient period. With respect to these qualities there are two classes of TVS widely in use. *Passive* devices are those with monotonic characteristic curves, as shown in Figure 6a, while *active* TVSs are switches, with negative resistance regions on their I-V curves (Figure 6b). A passive TVS has CR $>$ 1, does not need to be reset, and allows many circuits to function during a transient. Metal Oxide Varistors (MOVs) and semiconductor avalanche TVSs* are passive. An active TVS works by switching to a near-short condition when it senses a transient pulse, so that CR $\approx$ 0. Circuits protected by an active TVS do not funciton during the transient period (since they effectively become shorted out) and, in fact, will continue not to function after the transient period until the TVS "switch" is somehow turned off. Active transient suppressors include spark gap, gas tube and thyristor "crowbars". Combinations of active and passive TVSs, together with isolating elements and special reset circuits may be designed to keep circuits functional during most transients while utilizing the best features of both types of TVS.

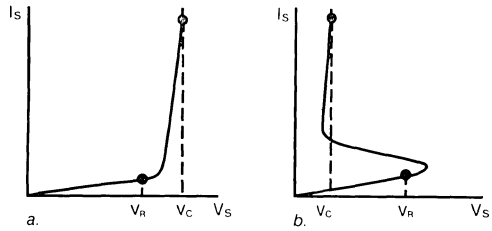

Fig.6 Comparison of (a) Passive and (b) Active Transient Suppressor Characteristics

Comparison of Commonly Used Suppressors

Active TVSs, in addition to their need to be reset, have the added disadvantage of being bulky and costly in comparison to passive devices. Furthermore, they do not protect below V_C during the clamping time t_C. Their advantage, and the reason for their continued use, is their ability to safely handle very large pulse currents. Passive devices cannot operate at extreme current levels for two reasons. They clamp at higher voltages and are physically smaller than the active TVSs, and therefore—at any given current level—the passive devices dissipate more power and operate at higher current densities. An advantage of semiconductor TVSs is their freedom from overshoot during the transient.

MOVs have other limitations. They degrade with use, and their rated pulse currents decrease markedly as the number of lifetime pulses they are to experience increases (Figure 7). MOVs have higher clamping ratios than those of equivalent semiconductor TVSs (Figure 8). MOVs are bidirectional devices, i.e. they clamp at approximately the same voltage in each direction.

*Hereafter referred to as simply "semiconductor TVSs".

This can be a disadvantage when protecting many unidirectional circuits (particularly logic circuits), as will later be discussed in greater detail.

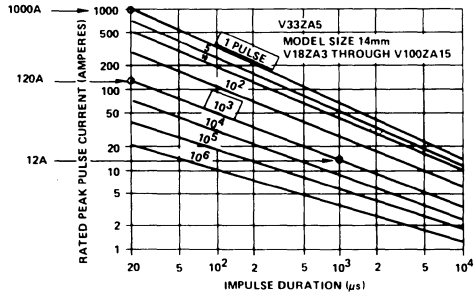

Fig.7 MOV Lifetime Pulse Ratings

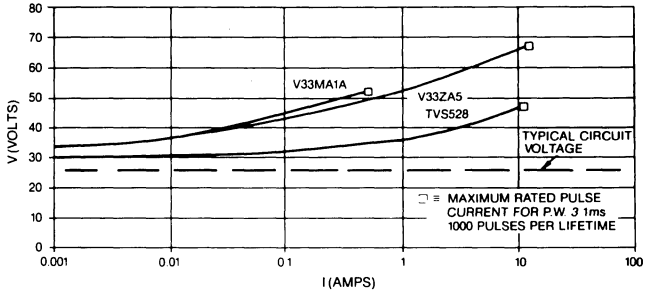

Fig.8 Clamping Voltage Versus Current

Table I summarizes the relative merits of typical transient voltage suppressors.

	Clamping Ratio	Clamping Speed (typical)	Active or Passive	Allowable Current (for 1ms)	Available Voltages	Degradation?	Size	Cost	Typical Applications	Protection From:
Spark Gap or Gas Tube	~0*	10^{-5}s	Active	10^{3}-10^{5}A	to 20kV DC	No	Large	Very High	Phone Lines, Input to Heavy Equip.	Lightning
Thyristor Crowbar	~0*	10^{-7}-10^{-4}s	Active	to 10^{3}A	to 800V AC or DC	No	Moderate to Large	High	DC Power Supply	Output Over-voltage Protection
Metal Oxide Varistor	1—2	10^{-8}-10^{-7}s	Passive	~100A	10-260V AC (RMS)	Yes	Small to Moderate	Low to Moderate	AC Line to Equip. and Instruments	Transients due to Load Changes and Lightning
Semi-conductor TVS	1—1.5	10^{-12}s	Passive	~50A	5-400V AC or DC	No	Small	Low to Moderate	"on-board" Protection	Internally Generated Transients

After t_C only.

Table 1 Comparison of Transient Suppressors

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Semiconductor TVS devices are preferred by power supply designers who must guard against predictable, moderate energy transients. The following section describes these devices in more detail, and offers selection guidelines and design examples.

Semiconductor TVSs

Unitrode offers several semiconductor TVS lines to commercial, industrial and military customers. Unitrode TVSs exploit the extremely rapid avalanche breakdown of a p-n junction in order to function as voltage clamps. TVS power ratings are specified for 1ms (for 50% decay) exponentially decaying pulses (ref. Figure 5). Units are available with 150W and 500W power ratings for industrial/commercial applications, and 500W and 1500W military types meet MIL-S-19500/551 and /434 respectively. Also, Unitrode markets zener diodes (1 to 10W DC) which have the same avalanche characteristics as the TVS devices, and can be used as transient suppressors.

To select the appropriate TVS for a given application, begin by determining the required stand-off voltage. V_R should be equal to or greater than the maximum non-transient voltage that is expected to appear across the TVS. Next, determine the TVS power requirements. Unitrode publishes room temperature pulsed power curves, in conjunction with junction temperature derating curves, for each TVS family (Figure 9). The pulse power rating curves (Figures 9a and 9b) apply to exponential pulses. If the expected pulse is not exponential, or approximately so, then construct an exponential pulse having the same peak power and total energy (i.e. area under the power curve) as the expected pulse (see Figure 5). Use the duration of this pulse when using the peak pulse power curves to determine which device family has adequate capability. The power and stand-off voltage considerations should point to one TVS part number.

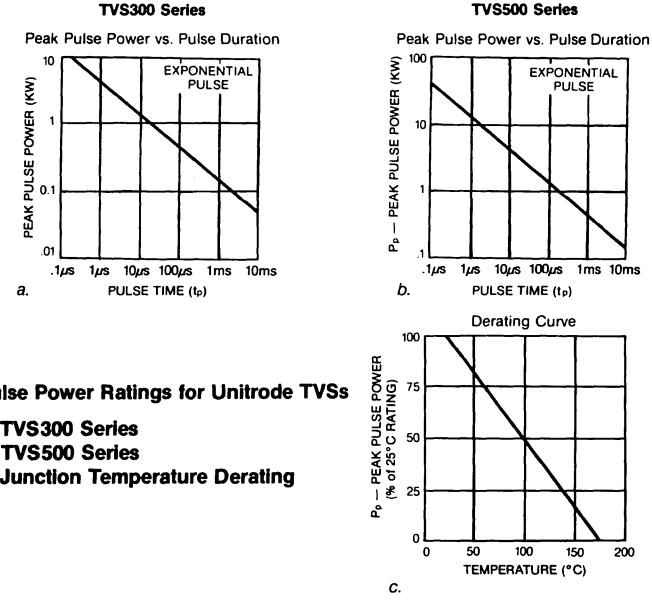

Fig.9 Pulse Power Ratings for Unitrode TVSs

a. TVS300 Series
b. TVS500 Series
c. Junction Temperature Derating

As a final step in the selection process, determine if the clamping voltage of the tentatively selected TVS is low enough at the expected pulse current. Figure 10 is a convenient graph used to quickly determine if the clamping voltage will be adequate. If not, try a TVS with a higher power rating.

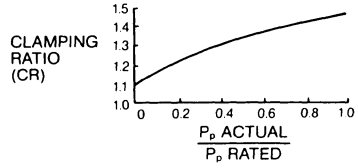

Fig. 10 Clamping Ratio vs. Peak Power for for Unitrode TVSs

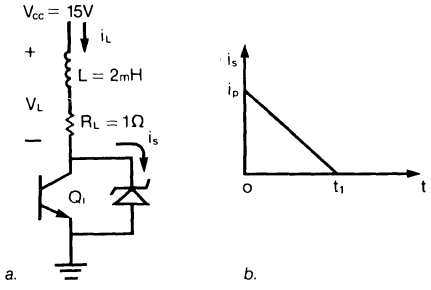

Fig. 11 A Typical TVS Application
a. Typical Circuit
b. (Idealized) Resultant Current in the TVS

To illustrate this selection process, let us consider in detail an inductive switching application of the type earlier mentioned. Figure 11a shows such an application.

Determining the required stand-off voltage rating is simple. The greatest non-transient voltage that will appear across the TVS is just the supply voltage V_{CC} = 15V. So a TVS with V_R = 15V will not interfere with the normal operation of the circuit.

As discussed before, the transient current induced in the TVS will show a linearly decaying time response (see Figure 11b). The peak current i_P is equal to the inductor current just prior to the turn-off of Q1. Making the worst-case assumptions that this system is in equilibrium before Q1 turns off, and that Q1 is then well saturated;

$$i_P = i_L\,(t = o-) = 15V/1\Omega = 15A$$

The peak pulse power p_P is given by:

$$p_P = i_P V_C$$

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For a first estimate of this power, assume $V_C = 1.3\ V_R = 19.5V$.

Then:

$$p_P = 15A \times 19.5V = 290W$$

The time for the current pulse to decay to zero is:

$$t_1 = \frac{i_P}{\frac{di_L}{dt}} = \frac{i_P L}{V_C} = \frac{15A \times 2mH}{19.5V} = 1.5ms$$

The equivalent exponential pulse would have $t_P \approx t_1/2 = .75ms$. Referring to Figures 9a and 9b, we can see that a Unitrode TVS300 series device would not be adequate for this application, but that a TVS515 would operate with a comfortable margin for error.

Finally, we check to see if our estimate that $V_C = 1.3\ V_R$ is reasonable. To use Figure 10, we first calculate:

$$\frac{p_{P\ (ACTUAL)}}{p_{P\ (RATED)}} = \frac{290W}{600W} \approx .5$$

The clamping ratio curve then gives $V_C/V_R \approx 1.32$. Had our original estimate been less accurate, we could have re-itterated the calculations, using the clamping voltage obtained in the final step.

If available TVS devices do not meet all the needs of a particular application, consider using a Unitrode zener diode. These diodes are not characterized as conveniently as are the TVS series for use as transient suppressors. However, designers can assume that these zeners will stand off voltages up to 85% of their minimum V_Z, and that they follow the clamping voltage curve of Figure 10. Other requirements for improved P and/or CR can be serviced by series connected TVSs or zeners.

Designers often ask about the use of bidirectional semiconductor TVSs. Bidirectional suppressors should only be used when the non-transient voltage is bidirectional; i.e. when both positive and negative non-zero stand-off voltages are required. This applies regardless of the expected transient polarities. The reason for this is that the unidirectional TVS has a lower voltage clamp for negative polarity transients than does the bidirectional. Consider the protection of a bipolar transistor, as shown in Figure 12. If a bidirectional TVS is used (Figure 12a), then a negative transient current i_S will break over the transistor's emitter-base junction if the TVS has V_S greater than the breakdown voltage of that junction. On the other hand, a unidirectional TVS (Figure 12b) becomes forward biased and clamps at no more than a few volts even at very high currents. The low voltage emitter-base junction is safe in this case. Knowledge of the usefulness of this low voltage negative clamping characteristic has prompted the military to include reverse clamping voltage specifications for new 1N-type transient suppressors. (See, for instance, MIL-S-19500/551.)

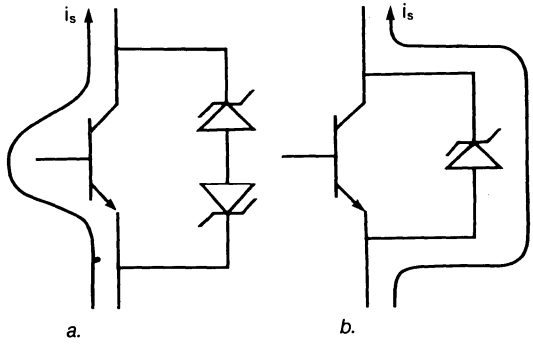


Fig. 12 (a) Bidirectional vs. (b) Unidirectional Protection for a Bipolar Transistor

The predictability of transient energy sources was earlier discussed. Often, it was found, the designer cannot accurately characterize expected transients.

It is possible, then, that a TVS could experience a pulse with energy in excess of that predicted by the designer. Faced with this potential situation, the designer should consider how the TVS behaves if overpowered.

A TVS, operating at a power level it cannot sustain, must react either to decrease the current that is flowing through it, or to decrease the voltage across which the current flows. Either the TVS tends toward an open circuit, or it becomes nearly a short circuit.

From a design standpoint, it is most often advantageous for the TVS to become a short circuit or very low resistance when subjected to a high energy transient. The primary purpose of the TVS is to protect other components. This is not accomplished if the TVS becomes highly resistive.

When overpowered by high transient field conditions, Unitrode Transient Voltage Suppressors and zener diodes fail in the "shorted" mode. The mechanism is the same "second breakdown" phenomenon observed in power transistors.

Only under very extreme pulse conditions will Unitrode TVSs fail "open". The pulse would need to have enough energy to initiate the second breakdown of the silicon junction followed by enough "follow through" energy to cause considerable heating in the now low resistance silicon.

Unitrode TVSs are of a voidless construction, so that even at very high chip temperatures the units cannot "explode" by igniting a contained gas. Cracking and chipping of the glass can occur, but this does not normally result in damage to surrounding components.

Reliability has always been important in electronic equipment; today it is even more so. Complex military and industrial systems must be built with circuit blocks of unquestioned reliability, if the overall system reliability is to be acceptable. Consumers now rightly demand long life for the products they buy. By better understanding the nature of transient energy sources and of available transient suppressors, the designer is better able to meet toughening reliability goals.

LIMITING INRUSH CURRENT TO A SWITCHING POWER SUPPLY IMPROVES RELIABILITY, EFFICIENCY

Active inrush-current limiters—unlike fuses and circuit breakers—prevent dangerous situations instead of only reacting to them. Apply limiting techniques, and you need not employ extra-hefty rectifiers just to ensure rectifier survival during turn on.

Roger Adair, Unitrode Corp

The input filter capacitor employed in many dc power-supply designs creates a potential problem—high inrush current. Fortunately, though, adding a few extra components can prevent inrush current and its associated circuit damage.

How does the input capacitor cause such problems? Intentionally chosen for high storage capacity and low equivalent series resistance (ESR), it behaves like a nearly perfect short circuit when the supply first turns on. The resulting short-duration peak inrush current can reach levels much greater than the tolerable single-cycle ratings of the supply's semiconductor rectifiers (thus destroying them) and still not contain sufficient total energy to open protective fuses or

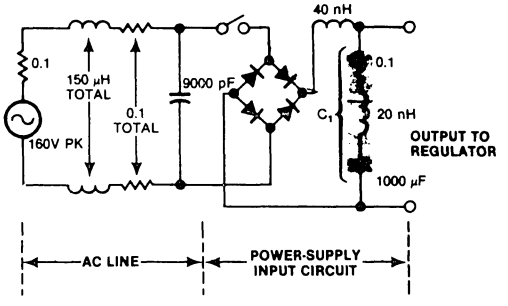
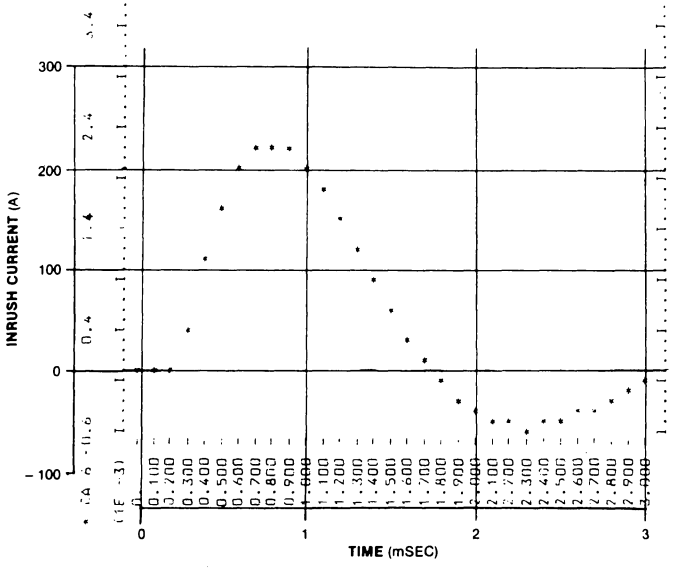


Fig 1—Based upon this generalized model, *analysis indicates the inrush-current problem's magnitude. Chosen for its low ESR, the input filter capacitor (C_1) behaves like a nearly perfect short circuit when the supply first turns on.*




```
                ECAP
                TRANSIENT ANALYSIS
C
B1      N(0,1),R=.1
B2      N(1,2),L=150E-6
B3      N(2,3),R=.1
B4      N(3,0),C=9000E-12
B5      N(3,4),R=.001
B6      N(4,5),L=40E-9
B7      N(5,6),R=.1
B8      N(6,7),L=10E-6
B9      N(7,0),C=1000E-6
E1      (1),0,0,0,160
        TIME STEP=100E-6
        FINISH TIME=3E-3
        IERROR=1
        PRINT NV,CA
        PLOT,(SCALED),CA(6)
        BINARY,NV,CA
```

Fig 2—Peaks greater than 200A *are predicted by ECAP for the circuit model shown in* **Fig 1.** *Rectifier-diode reverse-recovery capability would inhibit the indicated 50A overshoot in an actual circuit design.*

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Turn on an analysis before you turn on a power supply

circuit breakers. Additionally, the supply's rapidly rising voltage and current levels could cause dv/dt- or di/dt-sensitive devices in neighboring hardware to fail or malfunction.

Computer analysis proves useful

To appreciate the inrush-current problem, consider an estimate of its magnitude before examining possible control techniques. **Fig 1** depicts a model of the ac-input and rectifier/filter sections for a typical dc power supply. Although shown in a straight off-the-power-mains configuration, the model should be valid for any other design with the same output-power capability.

An ECAP computer analysis performed for this circuit assumed worst-case conditions: switch closure at 160V (peak voltage). The results (**Fig 2**) indicate that an inrush current greater than 200A can exist for several milliseconds.

Now compare this predicted performance with the measured characteristics (**Fig 3**) of a typical design. The current pulse's high level and short duration could generate severe, localized hot spots in rectifier junctions or cause false triggering of rate-sensitive devices elsewhere in the circuit.

A standard approach to current limiting is depicted in **Fig 4a**—a resistor. It's simple, reliable and easy to design in, but efficient it isn't. At any current level, it dissipates power that would otherwise be available to the load. The resistor does perform a surge-current-limiting function, however.

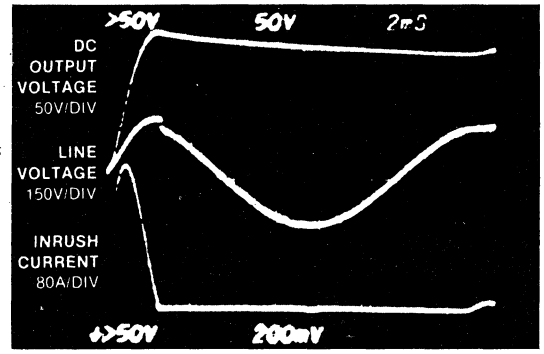

Fig 3—Measured inrush current *appears close to that predicted in* **Fig 2.** *This large current inrush could cause junction hot spots and generate troublesome EMI.*

Alternatively, a thermistor-controlled current limiter (**Fig 4b**) alleviates the resistor's efficiency problems to some extent, but it aggravates the dropout-recovery problem. The same cold-to-hot resistance variation that permits turn-on current limiting and high efficiency at low operating currents fails in dropout-recovery situations: The thermistor's long thermal time constant prohibits fast recovery.

SCR spells efficiency

In view of resistor and thermistor drawbacks, active soft-start designs offer a best-of-both-worlds

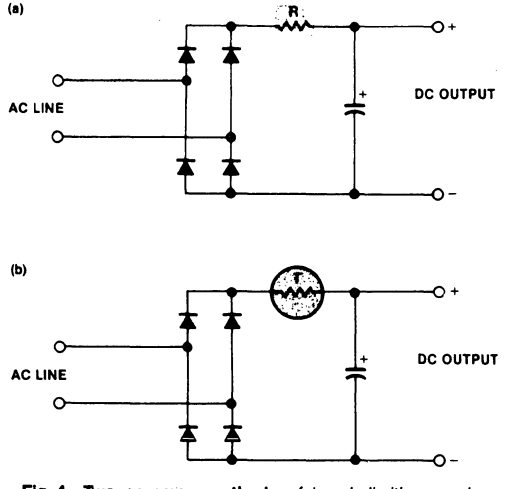

Fig 4—Two common methods *of inrush limiting employ either a resistor* **(a)** *or a thermistor* **(b).** *But if the resistor is large enough to effectively control surge currents, it also significantly reduces efficiency. The thermistor, while more efficient, offers little protection during dropout recovery because of its long thermal time constant.*

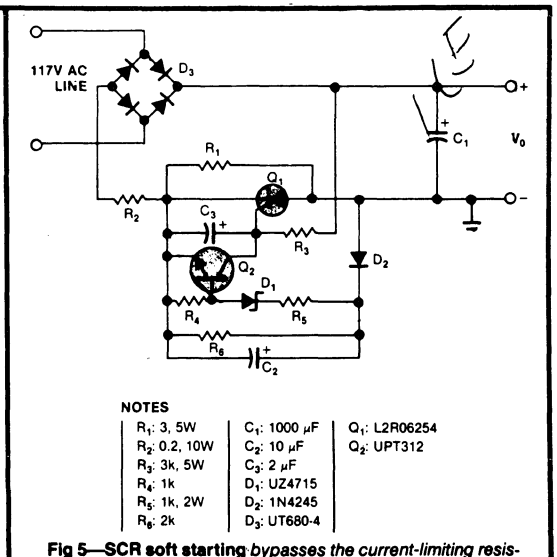

Fig 5—SCR soft starting *bypasses the current-limiting resistor (R_1) only when the peak-detected voltage across Q_1 drops below the zener breakdown, ie, when C_1 becomes almost fully charged through R_1.*

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solution—effective inrush limiting, fast recovery and high operating efficiency. This type of circuit, shown in **Fig 5**, essentially incorporates a current-limiting resistor (R_1) and a bypass switch (Q_1). At turn on, Q_1 is OFF, and the surge current (I_S) develops a voltage across R_1. This voltage is peak detected by D_2 and stored in C_2. When the voltage exceeds D_1's zener breakdown—an event that should occur almost instantaneously—Q_2 turns on, disabling Q_1's gate-triggering network (R_3C_3). As the power supply's filter capacitor C_1 charges up, the inrush peaks diminish until the detected I_SR_1 voltage falls below D_1's zener breakdown. Q_2 then turns off, and the R_3C_3 network charges up and fires Q_1, bypassing R_1.

This circuit recovers rapidly enough to limit inrush currents that could occur as a result of even short line dropouts. When the ac input voltage goes to zero, the voltage across Q_1 also goes to zero, and Q_1 turns off. When the input voltage reappears, Q_2 keeps Q_1's gate circuit OFF until R_1 has allowed C_1 to become almost fully charged.

Fig 6 graphically depicts this design's inrush-limiting ability. Note how the I_SR_1 voltage level (upper trace) tracks the diminishing inrush-current pulses (lower trace) for the first three cycles. At the 17-msec point (slightly after the third current pulse), the peak detected voltage has dropped below the zener breakdown point, and Q_1 switches on, bypassing R_1. Then R_2 limits inrush currents.

After determining your design's maximum continuous dc output current (I_O) and inrush limit (I_S), you can select an appropriate SCR. (The major SCR considerations are the peak repetitive blocking voltages and the maximum average plus peak current levels.) Typical SCRs exhibit a gate-turn-on voltage (V_{GT}) of about 0.6V; typical power-supply circuits exhibit a rate

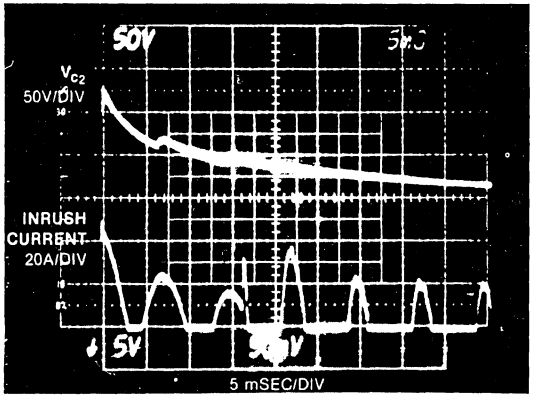

Fig 6—Inrush-current pulses of decreasing magnitude *(bottom trace) lower the SCR's hold-off voltage (upper trace). After 17 msec, the SCR fires.*

sensitivity (di/dt) of about 1A/μsec—two quantities required for calculating the values of the other critical components:

$$R_1=\sqrt{2}V_{AC}/I_S$$
$$R_2=P_{R_2}I_O^2$$
$$V_Z=I_SR_2$$
$$C3\geq(2\sqrt{2}\ V_{AC}V_Z)/(R_3V_{GT}R_1(di/dt)).$$

In the second equation, specify P_{R_2} as the maximum power your requirements allow across R_2.

Another effective inrush-current limiter is the phase-controlled triac design shown in **Fig 7**, which operates by controlling the conduction time of the current surges. Initially, the dc voltage (V_O) across C_1 builds up slowly because of R_1's current-limiting action. This dc voltage helps establish a reference (via R_{11} and zener diode D_1) for the programmable unijunction transistor (PUT) Q_4 and charges the phase-control

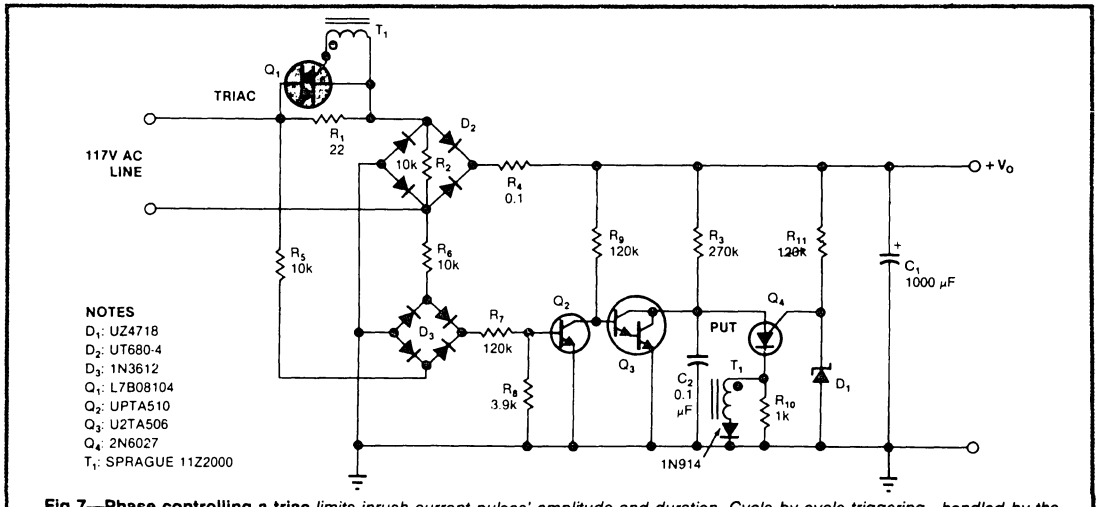

Fig 7—Phase controlling a triac *limits inrush-current pulses' amplitude and duration. Cycle-by-cycle triggering—handled by the PUT comparator—ensures instant recovery from line dropouts.*

Switch out the limiting resistor when the inrush is over

timing capacitor C_2 (via R_3). The PUT fires when its trigger point is reached, turning the triac on. Thus, when V_O is initially low, C_2 charges slowly, and the triac triggers on late in the half cycle. As V_O rises, Q_1 turns on earlier in each cycle until nearly 100% conduction is achieved.

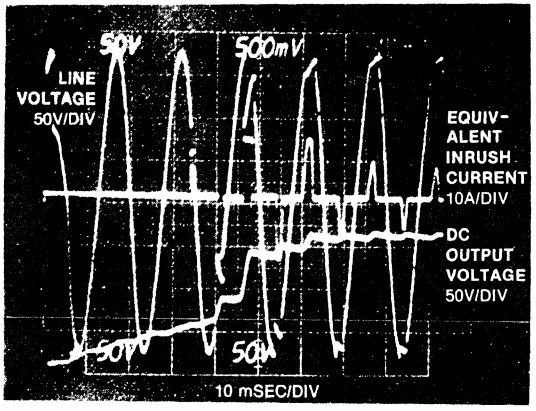

Fig 8—Triac conduction *follows the gradually increasing dc output voltage, decreasing the would-be inrush current. When the output voltage reaches design level, the triac is bypassing the current limiter nearly 100% of the time.*

The remaining circuit components (D_3, Q_2, Q_3, etc) discharge timing capacitor C_2 on each half cycle, thereby assuring cycle-by-cycle current limiting and fast recovery from dropouts. **Fig 8** depicts the relationship between the ac input voltage, the dc output voltage and the varying conduction angle of the triac. **EDN**

SWITCHING POWER SUPPLY DESIGN REVIEW

60 WATT FLYBACK REGULATOR

By Raoji Patel and Glenn Fritz

This paper gives a practical example of the design of an off-line switching power supply. Factors governing the choice of a discontinuous flyback topology are discussed. The design uses a pulsed-width modulation (PWM) control scheme implemented with a Unitrode UC3840 IC. This chip's voltage-feed-forward feature is used to achieve improved output regulation. The paper discusses closing the control loop to achieve both stability and adequate dynamic regulation, and provides guidelines for transformer design and component selection.

The circuit developed herein operates from a 117V (±15%), 60 Hz line and meets the following objectives:

1. Output voltages:
   a. +5V, ±5%: 2.5A-5A
      Ripple voltage: 50mV P-P maximum
   b. +12V, ±3%: 1A-2.9A
      Ripple voltage: 100mV P-P maximum
2. Efficiency: 70% minimum
3. Line isolation: 3750V

These objectives are met by using a flyback converter topology with a MOSFET power switch operating at 80kHz. The design features primary side control.

I. SELECTION OF FLYBACK TOPOLOGY

The flyback, when compared to other switching regulator topologies, has several cost and performance advantages:

Cost Advantages:

1. For output power levels less than ~150W, the design of the power transformer (coupled inductor) is relatively simple.
2. Assembly costs for the flyback regulator are low due to a low overall component count. In particular, only one magnetic element (i.e., the transformer) is employed as no inductors are used in the output filters.
3. Output rectifier BV requirements are low, since they do not need to block voltages which in other topologies are developed across the filter inductor.

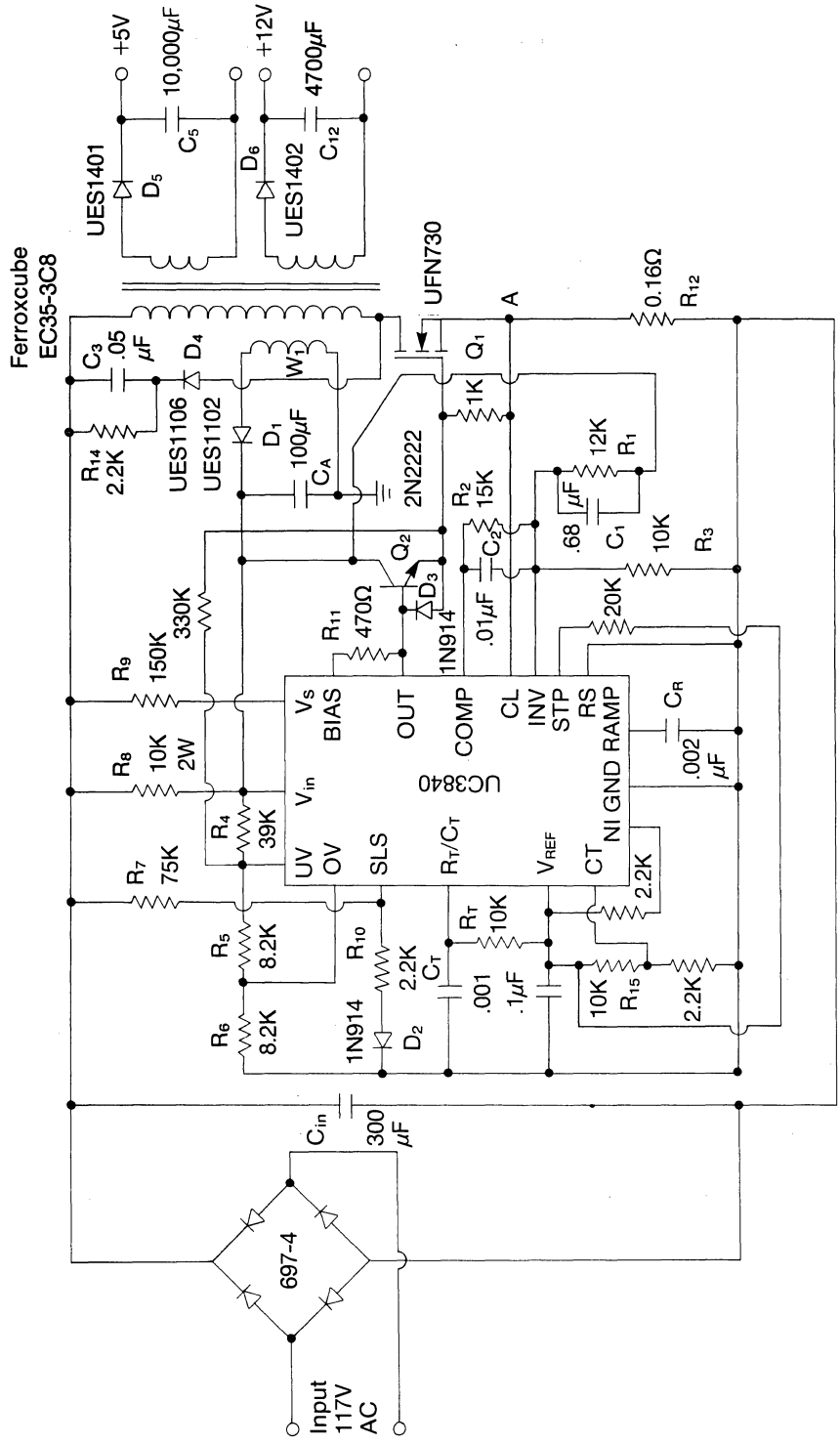

Figure 1. 60W "Off-Line" Flyback Regulator

Performance Advantages:

1. The flyback topology offers good voltage tracking in multiple output supplies due to the lack of intervening inductances in the secondary circuits.
2. Since there is no need to charge an output inductor each cycle, good transient response is achievable.

For these reasons, the flyback topology was chosen for this 60W, dual-output regulator.

Discontinuous Current Mode

Once a converter topology is chosen, the next decision with which the designer is faced is the choice between continuous and discontinuous current modes. Figure 2 compares primary and secondary current and transformer energy storage waveforms for these two cases.

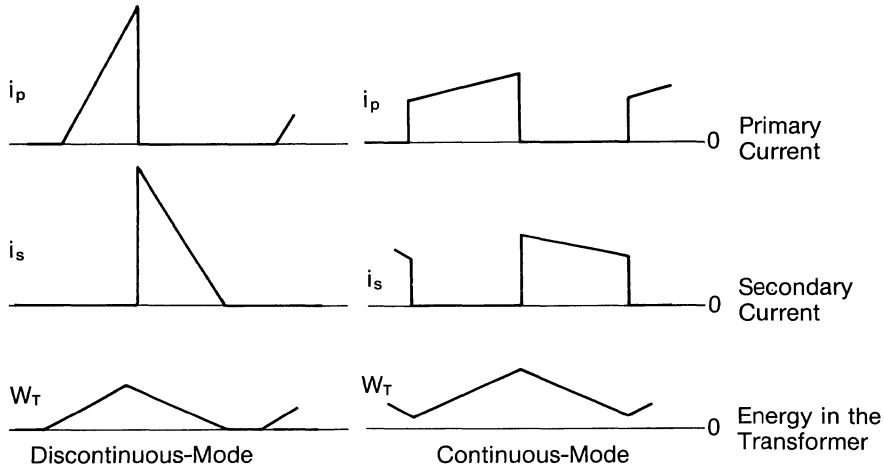

Figure 2. Discontinuous vs Continuous Flyback Waveforms

For the present design, a discontinuous current mode was chosen for reasons relating to component performance requirements dictated by these waveforms.

Advantages of Discontinuous Operation:

1. A small transformer can be used because the average energy storage (W_T in Figure 2) is low. Use of fewer turns also translates into reduced I^2R losses.
2. Stability is easier to achieve because at frequencies less than one half the switching frequency there is no net inductance reflected to the transformer secondary, and hence no second pole in the input-to-output transfer function. Also, no right half-plane (RHP) zero appears since energy delivered to the output each cycle is directly proportional to the power transistor on-time (t_{on}) for the discontinuous case.

3. Output rectifiers are operating at zero current just prior to becoming reverse biased. Therefore, reverse recovery requirements are not critical for these rectifiers.
4. Similarly, the power transistor turns on to a current level which is initially zero, so its turn-on time is not critical.
5. Transistor turn-on to zero current also results in low RFI generation.

Unfortunately, some disadvantages also accrue from the use of a discontinuous current scheme.

Disadvantages of Discontinuous Operations:

1. Transistor and diode peak current requirements are approximately twice what they would be in a continuous mode design. Average current requirements remain unchanged.
2. Transformer $d\phi/dt$ and leakage inductance are both high under discontinuous operation, resulting in some loss of cross-regulation.
3. High values of ripple current make output capacitor ESR requirements quite stringent. In most practical discontinuous flyback circuits, capacitance values must be increased in order to achieve adequate ESR. Transient response is correspondingly slower.

In the present design, these few disadvantages were not deemed sufficient to warrant a choice of continuous mode operation. In particular, low output current requirements (5A max.) reduce the impact of the capacitor ESR problem.

Figure 3 shows a basic flyback circuit and the associated voltage and current waveforms for discontinuous operation. Regulation is achieved by varying the duty cycle of power switch T_1. During the period when Q_1 is on, energy is transferred from input capacitor C_{in} to the primary inductance L_p of the transformer. The magnitude of this stored energy is given by:

$$W = \frac{1}{2} L_p i_{pp}^2 \qquad (1)$$

where i_{pp} = peak primary current

No energy is transferred to the secondary circuit during this period. When Q_1 is off, energy stored in the transformer is delivered by way of the secondary winding to the output filter capacitor and load. The average power delivered to the load is given by:

$$P_o = \frac{W}{T} = \frac{L_p i_{pp}^2}{2T} \qquad (2)$$

where T = switching period

The peak primary current (i_{pp}) is dependent on the input voltage (V_{in}), the primary inductance L_p, and the on-time of Q_1 (t_{on}):

$$i_{pp} = \frac{V_{in}\, t_{on}}{L_p}$$

Also, the average power output is related to the output voltage and load resistance:

$$P_o = \frac{V_o^2}{R_L}$$

Substituting for P_o and i_{pp} in equation 2, one obtains:

$$\frac{V_o^2}{R_L} = \frac{V_{in}^2\, t_{on}^2}{2L_pT}$$

The DC output voltage is therefore:

$$V_o = V_{in}\, t_{on} \sqrt{\frac{R_L}{2L_pT}} = V_{in}D \sqrt{\frac{R_LT}{2L_p}} \qquad (3)$$

where duty cycle $D = \frac{t_{on}}{T}$

Note that for a discontinuous flyback, the output voltage varies directly with both V_{in} and $\sqrt{R_L}$ when a conventional PWM control chip is used.

II. SELECTION OF A CONTROL CIRCUIT

A PWM control technique is used in this design rather than a variable frequency scheme. Reasons for this decision follow, and are again related to cost and performance.

1. The transformer design can be optimized with PWM control because switching occurs at a fixed frequency.
2. Fixed frequency operation results in a narrow EMI spectrum. EMI is, therefore, filterable.
3. Output ripple under light load conditions is minimized with a PWM technique.
4. Integrated circuits are available for PWM control, while variable frequency techniques require discrete implementation. Modern PWM control ICs, such as the UC3840, also provide various auxiliary functions which further reduce the overall number of components required.
5. Implementation with PWM control allows for the use of a voltage-feed-forward technique to achieve improved output regulation and volumetric efficiency.
6. Power supply switching can be synchronized with external circuits, such as CRT amplifiers, to reduce the display interferences.

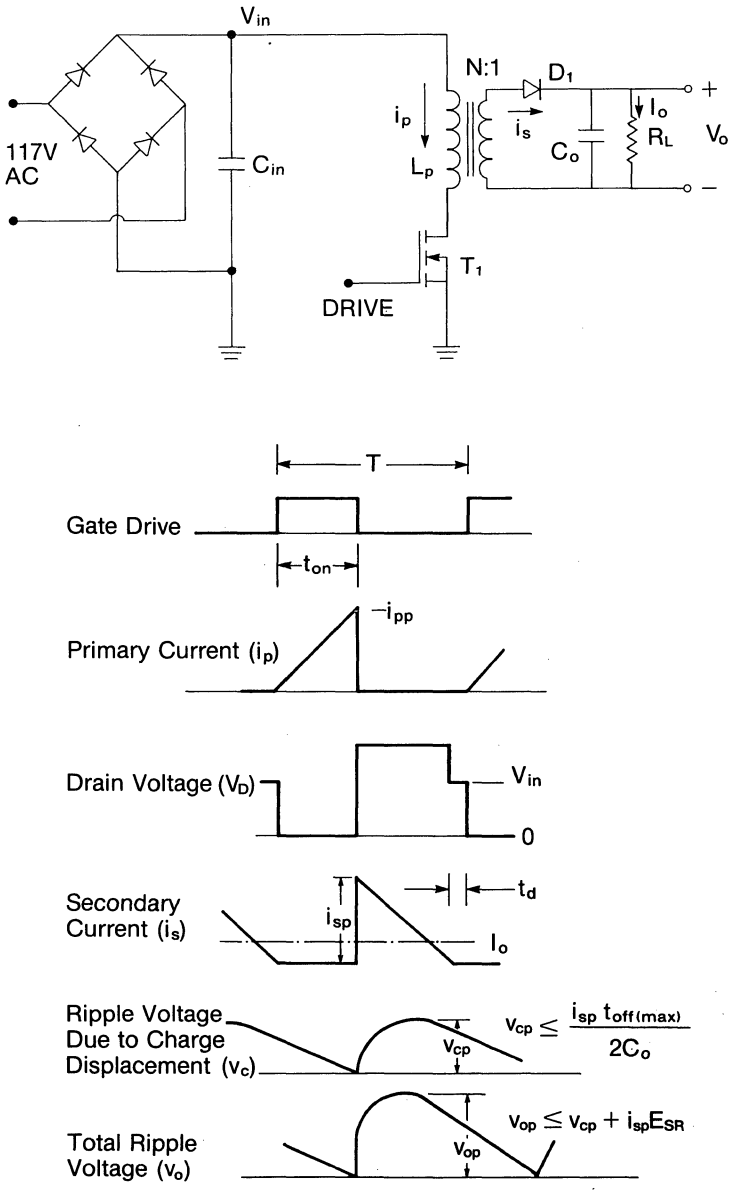

Figure 3. Voltage and Current Waveforms, Discontinuous-Mode Flyback Regulator

The voltage-feed-forward technique is illustrated in Figure 4. The rate of increase of the sawtooth waveform (internally generated by the PWM IC) is directly proportional to the input voltage V_{in}. As V_{in} increases, the output pulse width (transistor on-time) decreases in such a manner as to provide a constant "volt-second" product (constant energy) to the transformer primary. Therefore, variations in V_{in} do not affect output regulation. The operation of this feed-forward scheme is described by two relations:

$$V_s = \frac{V_{in}}{K}$$

where K = constant
V_c = control voltage
V_s = P-P sawtooth voltage

$$D = \frac{t_{on}}{T} = \frac{V_c}{V_s} = \frac{KV_c}{V_{in}}$$

Application of these relations to equation 3 yields the following as the open-loop response of the voltage-feed-forward discontinuous flyback regulator:

$$V_o = KV_c \sqrt{\frac{R_L T}{2L_p}} \qquad (4)$$

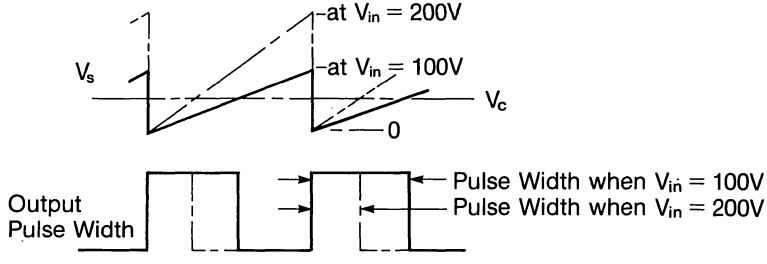

Figure 4. Voltage-Feed-Forward Technique

Note that the output voltage is independent of V_{in}, but varies directly with $\sqrt{R_L}$. Figure 5 shows the open-loop dependence of V_o on V_{in} and R_L for both conventional PWM and feed-forward controls. The curves show experimental results, and are in good agreement with equations 3 and 4. Deviations from flat response in the feed-forward case are due to variations in the MOSFET turn-off delay time, $t_{d(off)}$.

Freedom of V_o from V_{in} dependence minimizes the error amplifier gain requirement while maintaining adequate output regulation. In addition, the audio susceptibility of the feed-forward implementation is good due to the cycle-by-cycle compensation for input voltage variations.

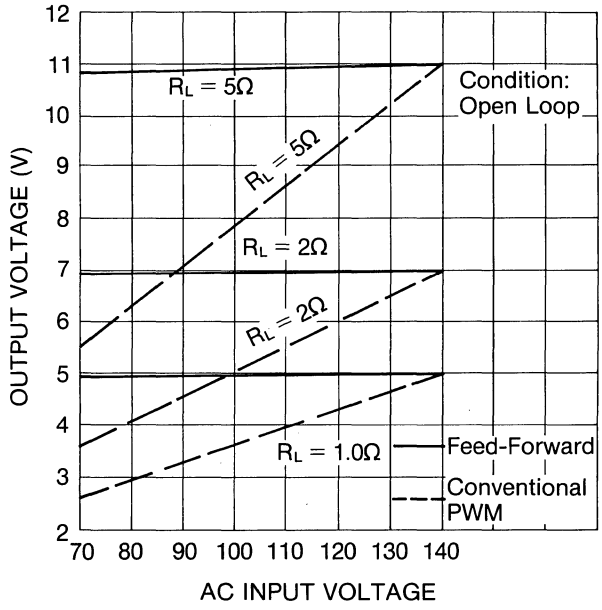

Figure 5. Comparison between Voltage-Feed-Forward and Conventional PWM Operation (Experimental Results)

The UC3840 IC provides a terminal which can be used to clamp the control signal internally to any desired level. When used in conjunction with the feed-forward circuitry, this feature allows the designer to set an upper limit on the transformer "volt-second" product. The design of the transformer can then be further optimized for size and cost.

III. CLOSING THE LOOP

The 60W regulator utilizes a primary side control technique wherein an auxiliary transformer winding on the primary side is used to develop a control voltage which is fed back to the PWM error amplifier. External compensation of this amplifier gives the designer control over the closed-loop frequency response of the entire system. The objectives in designing the error amplifier compensation are to insure circuit stability while achieving adequate dynamic output regulation. Figure 6 illustrates an optimum practical open-loop frequency response for a switching regulator.

Good DC and transient regulation requires high closed loop gain at frequencies below $f_s/2$. Signals at higher frequencies do not contribute to regulation because they are "sampled" at too low a rate by the circuit. Unwanted oscillation results if the closed-loop phase reaches $-360°$ at any frequency for which the gain is greater than 0dB. Conservative designs should maintain a 45° phase margin above $-360°$ at these frequencies. In practice, this criterion is most easily met if the 0dB gain cross-over point is at as low a frequency as possible. To compromise between transient response and stability requirements, the 0dB cross-over is usually designed to occur near $f_s/2$.

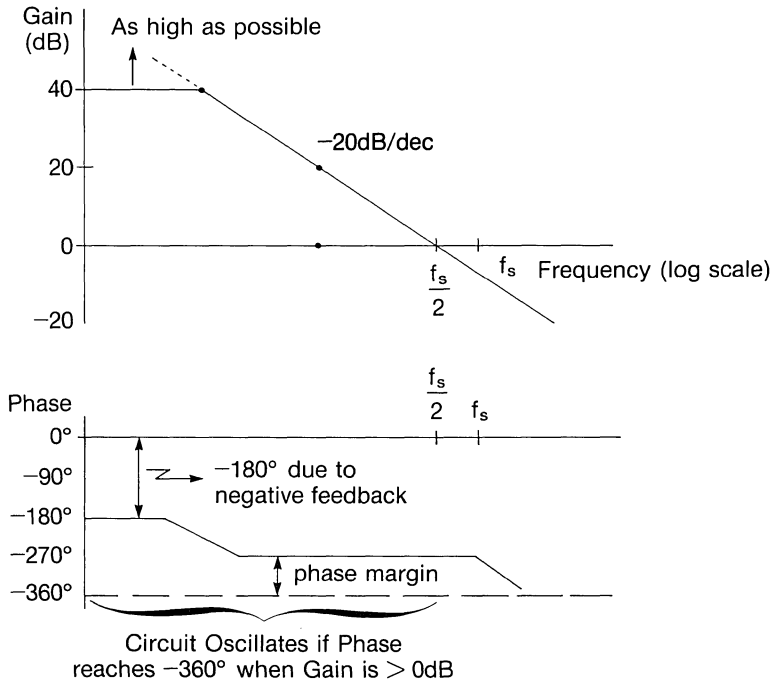

Figure 6. Desired Closed-Loop Response

In order to determine the error amplifier response required to stabilize the 60W regulator, while achieving the desired regulation, the small-signal open-loop response of the PWM modulator and the power output stage is first determined. The DC response, as previously developed, is:

$$V_o = KV_c \sqrt{\frac{TR_L}{2L_p}} \tag{5}$$

For low frequencies, the small signal variation in output voltage is obtained by differentiating equation 5 with respect to V_c:

$$\frac{dV_o}{dV_c} = K \sqrt{\frac{TR_L}{2L_p}} \tag{6}$$

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The effective output capacitance C_E and load resistance R_L form a low-pass filter which causes additional attenuation above the break frequency of the filter. The overall control-to-output transfer function is:

$$\frac{v_o}{v_c} = K\sqrt{\frac{TR_L}{2L_p}}\left(\frac{1}{(s/\omega_0 + 1)}\right) \tag{7}$$

where $\omega_0 = \dfrac{2}{R_L C_E}$

$$K = \frac{V_{in(min)}}{V_s}$$

C_E = effective output capacitance

R_L = effective output load resistance

In order to evaluate equation 7, it is first neccesary to determine values for the primary inductance L_p and for the effective filter components C_E and R_L. This is done in appendices I and II. The results are:

$L_p = 165\mu H$
$C_E = 4500\mu F$
$R_{L(min)} = 2.40\Omega$
$R_{L(max)} = 5.88\Omega.$

For purposes of graphing the control-to-output transfer function, it is only necessary to determine the DC gain and the filter cutoff frequency.

DC Gain:

$$\frac{v_o}{v_c} = K\sqrt{\frac{TR_L}{2L_p}} = \frac{V_{in(min)}}{V_s}\sqrt{\frac{TR_L}{2L_p}}$$

$$\left.\frac{v_o}{v_c}\right|_{DC,\ max.\ load} = \frac{100V}{3.5V}\sqrt{\frac{(12.5\mu s)\ (2.40\Omega)}{2\ (165\mu H)}} = 8.6 = 18.7dB$$

$$\left.\frac{v_o}{v_c}\right|_{DC,\ min.\ load} = \frac{100V}{3.5V}\sqrt{\frac{(12.5\mu s)\ (5.88\Omega)}{2\ (165\mu H)}} = 13.4 = 22.5dB$$

Cutoff Frequency:

The transfer function break frequencies for maximum and minimum load conditions are:

$$f_1\ (P_{o(max)}) = \frac{2}{2\pi\ 2.4\Omega\ 4500\mu F} = 29.5\ Hz$$

$$f_1\ (P_{o(min)}) = \frac{2}{2\pi\ 5.8\Omega\ 4500\mu F} = 12.2\ Hz$$

The resulting frequency response is illustrated in Figure 7A.

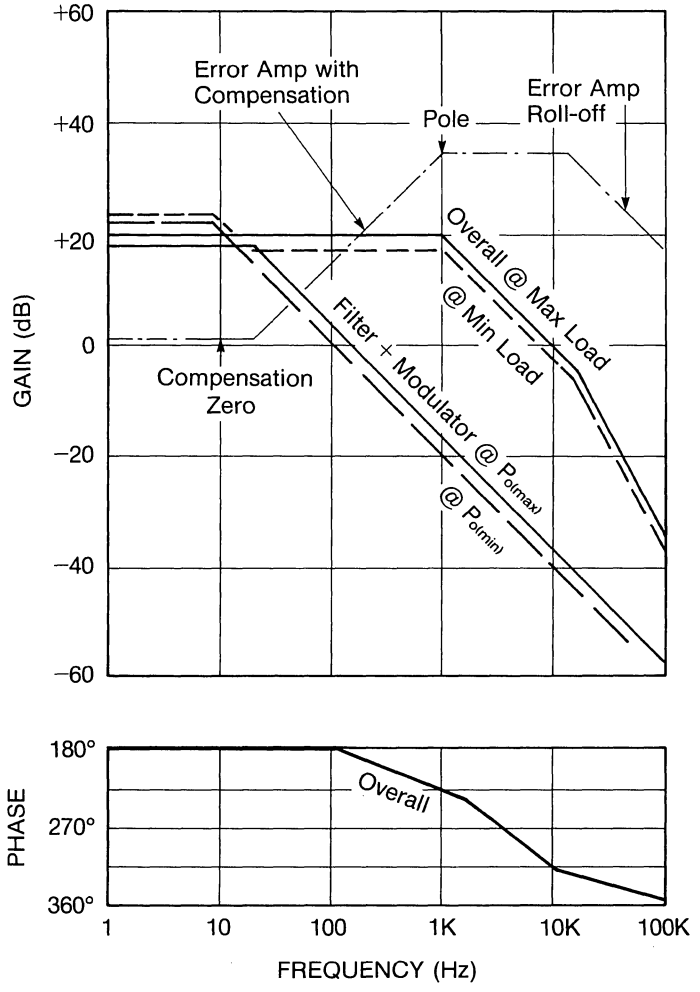

Figure 7A. Gain and Phase Plots

Figure 7B shows the open-loop error amplifier response for the UC3840. The gain plot can be thought of as representing an upper limit on the gain response of the error amplifier when compensated. Note that at frequencies above ~15kHz, the closed-loop gain (filter + modulator + error amplifier) would be less than 0dB even if compensation networks did not cause further attenuation. Therefore, a 40kHz gain cross-over is not obtainable with this particular design. We chose 15kHz as a best case practical 0dB point.

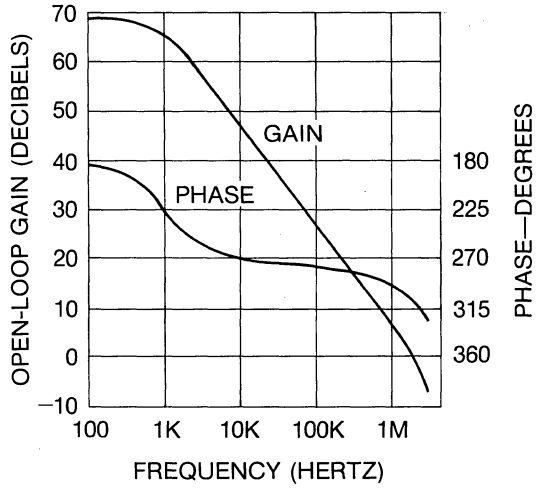

Figure 7B. Open-Loop Response of UC3840 Error Amplifier

In order to obtain adequate gain below 15kHz, a zero is needed in the closed-loop response near 20 Hz in order to compensate for the low frequency filter pole. The desired response of the compensated error amplifier is shown in Figure 7A. Also shown is the resulting overall closed-loop response. Figure 8 shows the error amplifier with the compensation elements required to achieve this response.

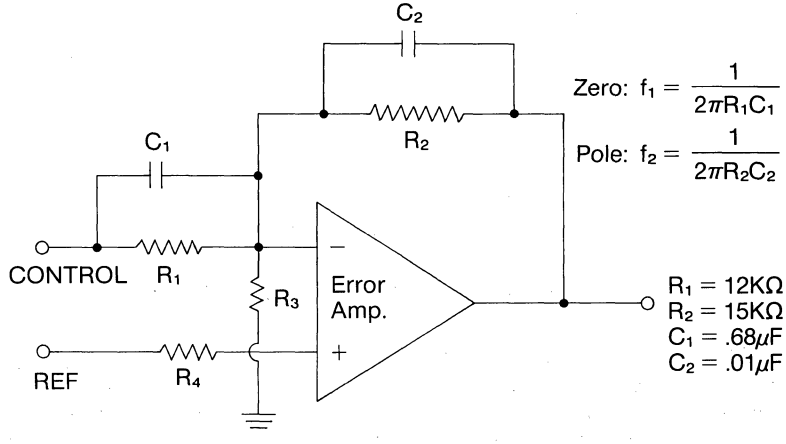

Figure 8. Error Amplifier with Compensation

IV. DESIGN DETAILS AND PERFORMANCE (Refer to Figure 1)

The AC input voltage for this supply is rectified with a full-wave bridge and filtered by input capacitor C_{in}. The UC3840 control chip is equipped with under- and over-voltage lockout features. The under-voltage feature initially disables all internal circuits except the (low current) reference voltage circuit. The lockout voltage is set by divider network R_4-R_5-R_6 in Figure 1. This feature allows capacitor C_A to charge through R_8 and to store enough energy to power the drive circuitry. The UC3840 under-voltage lockout has built-in hysteresis to prevent hesitant start-up.

After the control IC is enabled, drive energy is provided each cycle from an auxiliary primary side transformer winding W_1. In conjunction with C_A and diode D_1, this winding forms a regulated 12V drive supply. This supply is also used to provide primary-side control for the 5 and 12V outputs. This voltage is fed to the UC3840 control input through R_1. This low-cost control scheme is not optimum in terms of output coupling, but, with a careful transformer design, ±2% regulation is still achievable.

The UC3840 operates at a fixed frequency $f_s = 1/(R_T C_T)$. This frequency is independent of the ramp slope, which varies directly with input voltage V_{in}, to provide voltage-feed-forward compensation. This ramp slope variation is accomplished as follows. Control chip input V_s is no more than one forward-biased diode drop above ground. Therefore, the current through R_9 is almost directly proportional to V_{in}. This current is fed internally to a current mirror which in turn drives ramp-control capacitor C_R at a charging rate proportional to V_{in}. Ramp linearity is better than 2%.

In order to optimize the transformer, it is desirable to limit the maximum duty cycle, as previously mentioned. This is accomplished with the UC3840 by clamping the control voltage to a level determined by voltage divider R_7-R_{10} and diode D_2.

Transistor Q_2 and diode D_3 provide a low impedance drive for fast switching of power FET Q_1. An internal transistor always pulls the UC3840 bias output to a level near supply voltage V_c unless the under-voltage lockout is active. When the open-collector control chip output is high, then drive to Q_2 is provided from the bias output through R_{11}. In this way the input capacitance of Q_1 is quickly charged for fast turn-on. This input capacitance is discharged through D_3 at turn-off.

The UC3840 also provides dynamic current limiting to protect costly power components. Primary current flows through R_{12} to develop a current-limit input signal at point A. This signal is compared to a reference signal established by R_{15} and R_3. When the current-limit signal exceeds this reference by 400mV, an internal error latch forces the PWM output low but leaves the bias output enabled. Capacitor C_A discharges through R_{11} until the under-voltage feature is activated, turning off the bias transistor. Not until this time does the control chip attempt a restart.

The snubber network R_{14}-C_2-D_4 prevents turn-off voltage spikes from exceeding the FET breakdown voltage. This snubber does not provide load-line shaping.

Power FET Q_1 and output rectifiers D_5 and D_6 are all in TO-220 packages to provide high volumetric efficiency. The rectifiers were chosen for fast forward recovery to minimize

switching losses. The higher-current 5V output utilizes a Schottky rectifier for low forward-biased power dissipation. The power FET provides fast switching when driven with the simple, efficient circuit already described.

Figure 9 shows the output regulation achieved with this design. Note that loading one output effects the regulation of the other output. This results from changes in the energy stored in the transformer leakage inductance. Transient response is shown in Figure 10.

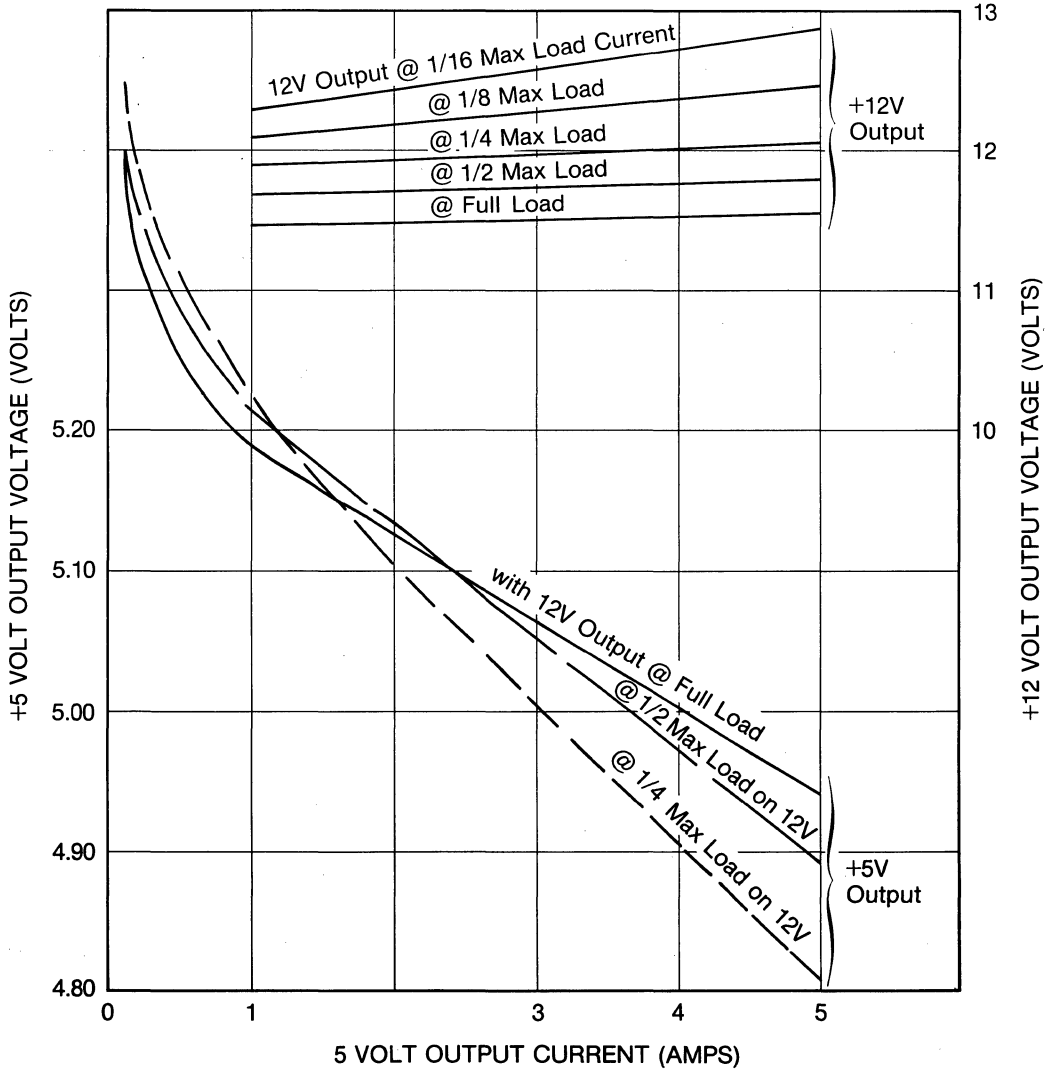

Figure 9. Output Load Regulation

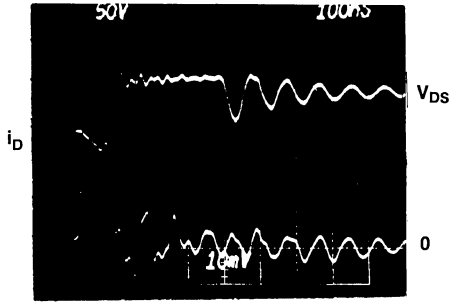

Figure 10A. Drain Voltage and Current Waveform Showing the Effect of the De-Spiking Network

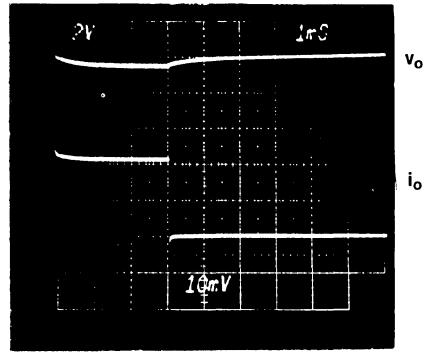

Figure 10B. Transient Response: Step Change of Load Current from 1A to 3A in +12V Output

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APPENDIX I

TRANSFORMER DESIGN

In a discontinuous-mode flyback regulator, the first design step is to determine the maximum on-time of the power transistor. This determines the maximum "volt-second" product and affects the primary current. For the flyback regulator with constant power output and frequency, Figures IA and IB show the required component ratings for designs having different maximum duty cycles. Note that all parameters are normalized to a maximum duty cycle of 50%. When this duty cycle is reduced in a given design:

(A) Current ratings of the switching transistor will be higher. However, the minimum blocking voltage required will be lower.

(B) Current ratings of the output rectifier will be lower. However, the minimum peak inverse voltage required will be higher.

(C) An output filter capacitor with higher ESR may be used to achieve the desired ripple voltage.

(D) I^2R losses remain constant even though the peak primary current increases.

(E) The maximum amount of energy stored in the transformer will remain the same.

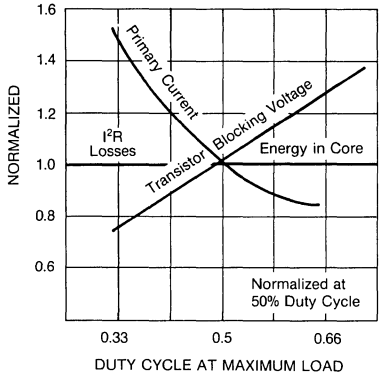

Figure IA. Primary Side

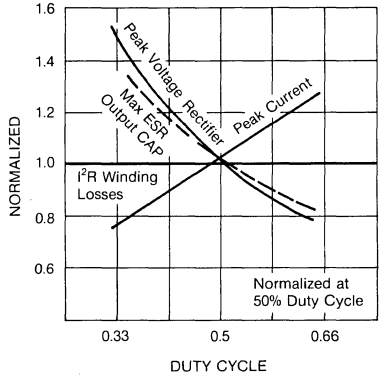

Figure IB. Secondary Side

Figure I. Effect of the Maximum Duty Cycle on the Design of a Flyback Regulator

In this design, the maximum duty cycle D_{max} was chosen at 45% to optimize the operating condition for the power MOSFET.

The maximum on-time:

$$t_{on(max)} = \frac{1}{f_s} D_{max} = \frac{0.45}{80 \times 10^3} = 5.62\mu s$$

The peak primary current:

$$I_{pp} = \frac{2P_o}{\eta f_s V_{in(min)} t_{on(max)}} = \frac{2\ (60)}{(0.8)\ (80 \times 10^3)\ (100)\ (5.62 \times 10^{-6})}$$

where η = efficiency

$$= 3.44A$$

The required primary inductance is therefore:

$$L_p = \frac{V_{in(min)}\ t_{on(max)}}{i_{pp}} = \frac{100\ (5.62 \times 10^{-6})}{3.44}$$

$$= 165\mu H$$

To determine the necessary core parameters, we compute the required energy storage in the primary inductance per cycle:

$$\Delta W = \tfrac{1}{2} L\ i_{pp}^2 = \tfrac{1}{2}\ (165 \times 10^{-6})\ (3.44)^2 = 969 \times 10^{-6}\ \text{Joules}$$

The Ferroxcube EC core provides low leakage flux because its outer legs have a cross-sectional area equal to that of the center leg. This design uses the EC35 core, which is the smallest EC core available. To minimize leakage flux, the linear portion of the B-H curve is used. The 3C8 material is linear up to 2000 gauss at 100°C. In the flyback transformer the energy is stored in the air gap. The required length of the air gap:

$$l_g = \frac{\Delta W}{.0312 \left(\frac{B_{max}}{2800}\right)^2 A_e}$$

where $B_{max} = 2800$
$A_e = .843$

$$= \frac{969 \times 10^{-6}}{.0312 \left(\frac{2000}{2800}\right)^2 (.843)}$$

$$= .072cm$$

The air gap l_g is divided equally among the two flux paths in the EC core.

The number of primary turns:

$$N_p \approx \frac{B_{max}\, l_g}{.4\pi\, i_{pp}} = \frac{(2000)\,(.072)}{(.4)\,(3.14)\,(3.44)} = 34 \text{ turns}$$

Figure IC shows details of the transformer construction.

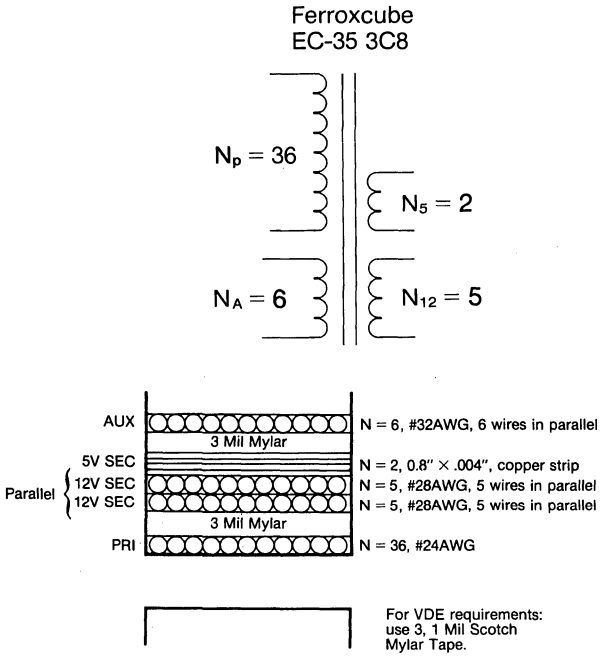

Figure IC. Construction of the Transformer Windings

The turns-ratio between primary to secondary can be calculated by the equation:

$$N_5 = N_P \frac{(Vo_5 + V_F)\,(4 - D_{max})}{V_{in(min)}\, D_{max}}$$

For +5V output, the turns-ratio;

$$N_5 = 34 \frac{(5 + 0.6)\,(1 - 0.45)}{(100)\,(0.45)} = 2.4; \text{ use 2 turns.}$$

APPENDIX II

Effective R_L and C in the Feedback Loop

Effective Load:

The output power range for this regulator is 24.5W to 60.0W. The reflected resistance in the auxiliary 12V primary-side supply is therefore:

$$R_{L(min)} = \frac{V_A^2}{P_{o(max)}} = \frac{144V^2}{60W} = 2.4\Omega$$

$$R_{L(max)} = \frac{144V^2}{24.5W} = 5.88\Omega$$

assuming that losses in the transformer and output filters are negligible.

Effective Filter Capacitor:

ESR considerations prevail in the choice of output filter capacitors. For a 50% maximum duty cycle, peak output ripple currents are calculated as follows:

$$I_o = \frac{i_{sp}}{2} D$$

where i_{sp} = peak secondary current

$$i_{sp} = \frac{2I_o}{D}$$

for the 5V output:

$$i_{sp5} = \frac{(2)\ (5A)}{.5} = 20A$$

for the 12V output:

$$i_{sp12} = \frac{(2)\ (2.9A)}{.5} = 11.6A$$

The ESR requirements are therefore:

for C_5:

$$ESR = \frac{\Delta V_o}{i_{sp5}} = \frac{50mV}{20A} = 2.5m\Omega$$

for C_{12}:

$$ESR = \frac{100mV}{11.6A} = 8.6m\Omega$$

Using low-cost aluminum electrolytic capacitors, these ESR requirements can be met with the following capacitance values:

$$C_5 = 10{,}000\mu F$$

$$C_{12} = 4700\mu F$$

The total effective capacitance in the auxiliary supply is given by:

$$C_E = \left(\frac{N_5}{N_A}\right)^2 C_5 + \left(\frac{N_{12}}{N_A}\right)^2 C_{12} + C_A$$

$$= \left(\frac{2}{6}\right)^2 10^4\mu F + \left(\frac{5}{6}\right)^2 4700\mu F + 100\mu F$$

$$= 4500\mu F$$

THERMAL CONSIDERATIONS FOR SEMICONDUCTOR DEVICE RELIABLITY

By Glenn Fritz

This paper is a guide to enhancing reliability and avoiding semiconductor failures in switching power supplies. Since semiconductor reliability is strongly related to junction temperature, a brief thermal design review is included. Several semiconductor failure modes are discussed, with emphasis on power supply circuits susceptible to such failure modes, methods of identifying failure mechanisms, and techniques for avoiding same.

Many semiconductor failures are the result of overheating the semiconducting silicon. Such failures can be broadly classified into two groups. First, failure can be due to excessive "average" heating, characterized by an expected distribution of high temperatures throughout the active regions, including junctions. For the purpose of this discussion, this includes repetitive transient heating within temperature ratings. Such heating is quantitatively predictable and can be controlled by appropriate device selection and heat sinking. The other failure mechanisms are related to localized overheating, and cannot be effectively addressed with the thermal models used for the average heating failure modes. A better approach to these potential problems involves relating identifiable transient circuit conditions to device ratings and safe operating area curves.

SECTION 1. AVERAGE HEATING CONSIDERATIONS

Degradation of semiconductors results from chemical reactions which change the structure of such devices on an atomic scale. The rate at which such reactions occur is found to follow the Arrhenius equation:

$$R(T) = Ce^{-E_a/KT} \qquad \text{(Eq. 1)}$$

where: $R(T)$ = temperature dependent reaction rate
C = constant
E_a = activation energy
K = Boltzmann's constant
T = temperature

Figure 1 is a typical plot of semiconductor failure rate, as a function of junction temperature, which follows Equation 1. Note that failure rate decreases rapidly as the operating junction temperature is lowered.

Semiconductor manufacturers commonly specify an absolute maximum junction temperature for any given device. This temperature is chosen to correspond to an "acceptable" failure rate for that device. However, as shown by Figure 1, improved reliability can be obtained by operating semiconductors at temperatures below their maximum rating. A tradeoff ultimately must be made between reliability and the cost and size of the semiconductor device and its associated heat sink.

Appendix A describes the thermal model usually used by designers to predict semiconductor junction temperatures and to thereby determine device and heat sink requirements. Readers unfamiliar with such a model are referred to this material. Following are illustrations of the application of this model to various power semiconductor devices commonly used in switching power supplies.

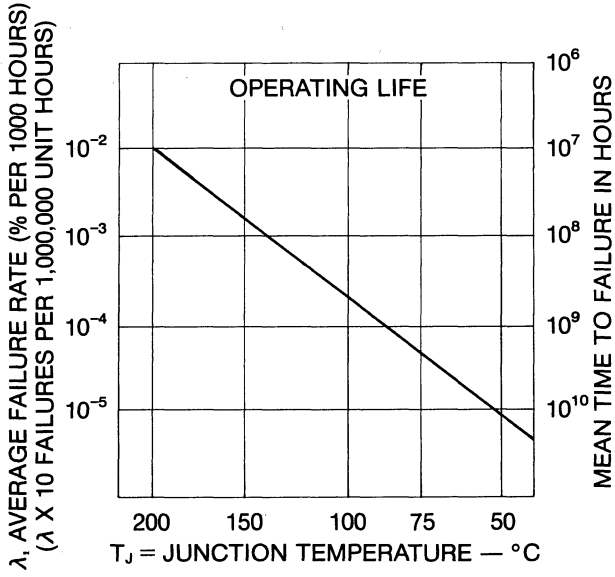

Figure 1. Approximate Arrhenius Model for Unitrode Bipolar Transistors

BIPOLAR TRANSISTORS

Power losses due to leakage current in the off state are usually negligible for bipolar transistors in switched-mode supplies. Therefore, equation A2 reduces to:

$$\overline{P} = \overline{P}_{conducting} + \overline{P}_{switching} \qquad \text{(Eq. 2)}$$

Conducting losses for bipolars can be expressed:

$$\overline{P}_{conducting} = \frac{t_{on}}{\tau} (i_c \cdot v_{ce} + i_b \cdot v_{be}) \qquad \text{(Eq. 3)}$$

where: t_{on} = transistor on time per cycle

τ = switching period

The variables i_c, v_{ce}, i_b and v_{be} in Equation 3 are mutually dependent. This is illustrated by the characteristic curves of Figures 2 and 3, which are curves typically supplied by power semiconductor manufacturers. In order to minimize conduction losses (Eq. 3) for a

particular bipolar transistor, it is necessary that the designer choose an optimum base current (i_b). If i_b is too small, then the transistor will fail to saturate resulting in high power dissipation due to the v_{ce} term in Equation 3. However, too large an i_b will result in higher transistor dissipation due to the i_b term in Equation 3, and overall supply economy and efficiency might be affected adversely by losses in the high current drive circuitry. Finally, excessive i_b will result in increased minority carrier storage in the bipolar transistor base region. It will be shown below that such a "hard saturation" condition causes poorer switching performance due to increased storage and fall times (t_s, t_f).

Unfortunately, while providing general guidance for selecting a transistor and determining base drive requirements, the curves of Figures 2 and 3 are insufficient for making the choice of optimum i_b. Figure 2 gives current gain (h_{FE}) values only for non-saturation conditions ($v_{ce} = 3$ or 10V), while Figure 3 shows saturation voltage at only one gain ($i_c/i_b = 5$). A family of curves such as that shown in Figure 4 is more useful in this connection. From these curves the designer can determine just how much base current is needed to keep v_{ce} low without overdriving the transistor.

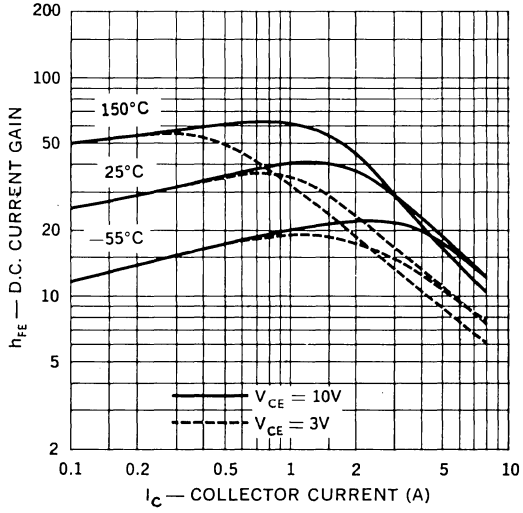

Figure 2. D.C. Current Gain for Typical Transistor

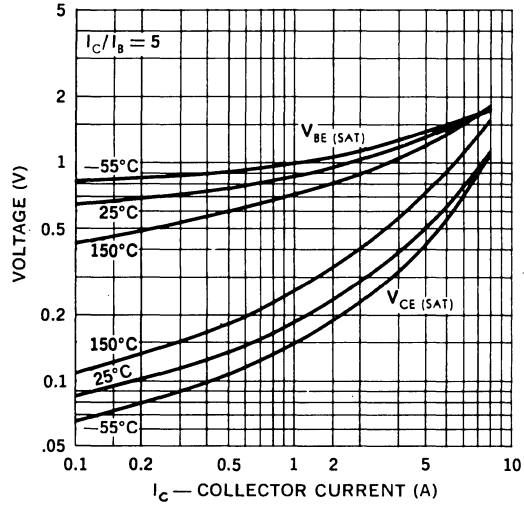

Figure 3. Saturation Voltages for Typical Transistor

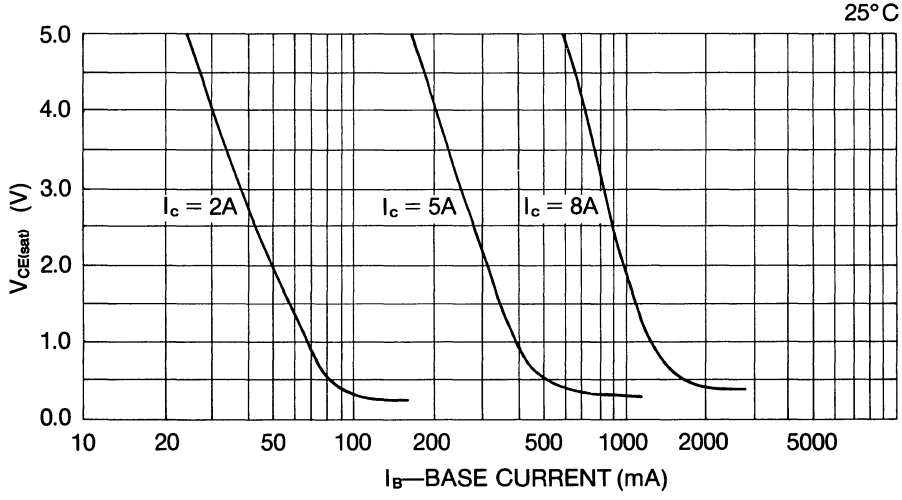

Figure 4. Typical V_{CE} vs I_C and I_B for Typical Transistor

Bipolar Switching Losses

The other element contributing to average heating in bipolar transistors is power dissipation during switching (see Equation 2). Power pulses—which are large in magnitude compared to the average power, but short in duration—occur both at turn-on and turn-off of the power transistor in switched-mode supplies.

In some topologies, turn-on losses are negligible when compared to turn-off losses. Figure 5 shows a basic flyback converter, with the associated transistor i_c and v_{ce} waveforms. Transformer leakage inductance, L_ℓ, is in series with the switching transistor and prevents i_c from rising significantly until v_{ce} has fallen at turn-on. Therefore, the peak power dissipation, which is proportional to the area of the shaded region under the curves of Figure 5, is not great. During turn-off, L_ℓ again restrains i_c from changing significantly until v_{ce} has completed its transition. In this case, however, a large power pulse occurs because both i_c and v_{ce} momentarily have large values. Figure 6 shows an expanded scale of this turn-off period. In order to calculate the energy dissipated during this transition, a method of triangular approximation is well suited. The energy under the curves is given by:

$$E_{sw} \simeq \frac{1}{2} \cdot i_{c(on)} \cdot v_{ce(off)} \cdot t_f \qquad \text{(Eq. 4)}$$

where: E_{sw} = switching energy dissipated per cycle
$i_{c(on)}$ = on-state transistor current
$v_{ce(off)}$ = off-state transistor voltage
t_f = total fall time (sometimes called "crossover" time (t_c) by manufacturers)

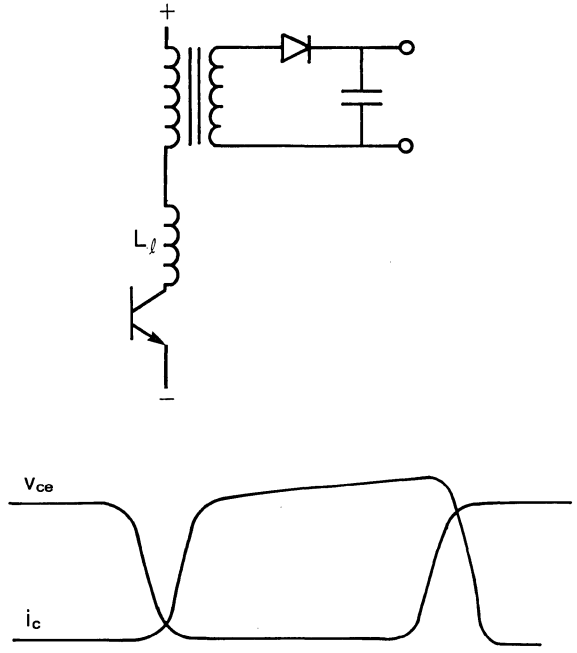

Figure 5. Flyback Topology and Associated Transistor Waveforms

The average transistor power due to switching in the flyback converter is therefore:

$$\overline{P}_{sw} = \frac{E_{sw}}{\tau} = \frac{1}{2} \cdot i_{c(on)} \cdot v_{ce(off)} \cdot \frac{t_f}{\tau} \qquad \text{(Eq. 5)}$$

If total fall time t_f is not specified, then current fall time t_{fi} can be used to calculate the area of region II in Figure 6, and the area of region I can be estimated. For a more careful study of switching losses, transition times should be measured under actual circuit conditions. Using the former method, and assuming $t_f \approx 2t_{fi}$:

$$E_{sw} \simeq i_{c(on)} \cdot v_{ce(off)} \cdot t_{fi} \qquad \text{(Eq. 6)}$$

$$\overline{P}_{sw} \simeq i_{c(on)} \cdot v_{ce(off)} \cdot \frac{t_{fi}}{\tau} \qquad \text{(Eq. 7)}$$

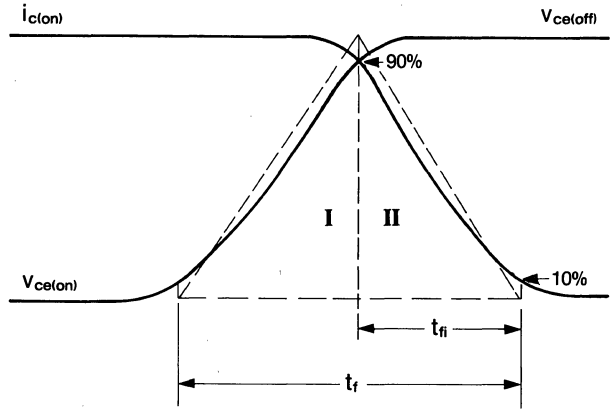

Figure 6. Bipolar Turn-Off

In the case of a buck regulator, turn-on losses are also significant. Figure 7 shows the buck topology and its associated transistor waveforms. In this case, the catch diode forces the transistor to see the full input voltage, V_{in}, at any time that diode carries any forward current. This results in the switching waveforms of Figure 7, with much energy dissipated during both turn-on and turn-off. Turn-off losses can be calculated by the same method used for the flyback regulator (Equation 7). Figure 8 shows the turn-on transition in more detail. If the catch diode recovery time is negligible, then:

$$E_{sw(turn\text{-}on)} = \frac{1}{2} \cdot i_{c(on)} \cdot v_{ce(off)} \cdot t_r \qquad \text{(Eq. 8)}$$

where t_r = current rise time (as defined in Figure 8)

Also: $$\overline{P}_{sw(turn\text{-}on)} = \frac{1}{2} \cdot i_{c(on)} \cdot v_{ce(off)} \cdot \frac{t_r}{\tau} \qquad \text{(Eq. 9)}$$

The effect of diode recovery time on transistor turn-on losses will be considered on subsequent pages. Total switching losses for the transistor in the buck configuration are given by (from Equations 5 and 9):

$$\overline{P}_{sw} = \overline{P}_{turn\text{-}on} + \overline{P}_{turn\text{-}off}$$

$$\overline{P}_{sw} = \frac{1}{2} \cdot i_{c(on)} \cdot v_{ce(off)} \cdot \frac{t_r}{\tau} + \frac{1}{2} \, i_{c(on)} \cdot v_{ce(off)} \cdot \frac{t_f}{\tau}$$

$$\overline{P}_{sw} = \frac{f_s}{2} \cdot i_{c(on)} \cdot v_{ce(off)} \cdot (t_r + t_f) \qquad \text{(Eq. 10)}$$

where: $f_s = 1/\tau$ = switching frequency

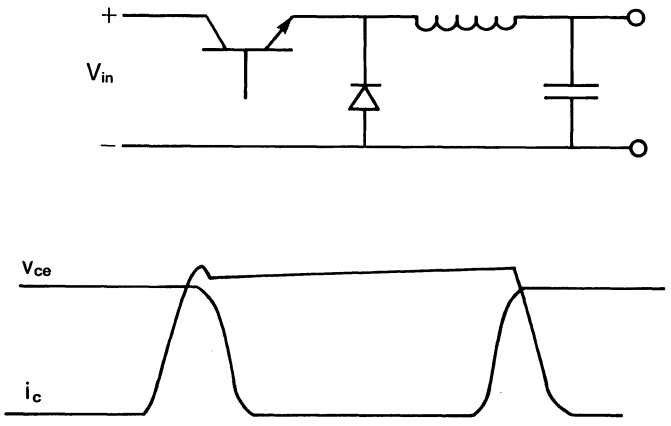

Figure 7. Buck Topology and Associated Transistor Waveforms

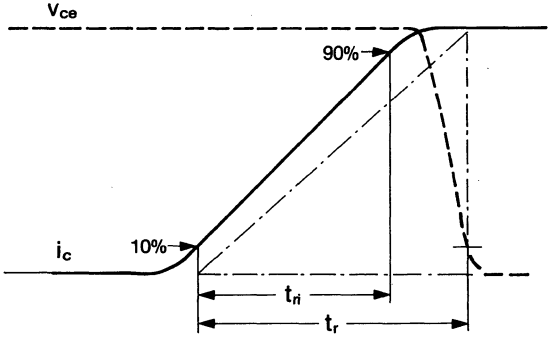

Figure 8. Bipolar Turn-On

Reducing Losses

In order to minimize bipolar transistor switching losses in any given circuit (for which $i_{c(on)}$, $v_{ce(off)}$ and f_s are fixed), the designer has two methods available. First, he can seek to minimize t_f and t_r by providing appropriate base drive. Second, designers can alter the switching waveforms by using snubber circuits.

1. Drive Circuit Optimization

Stored minority carriers in the base region are the cause of bipolar transistor storage and, to a lesser extent, fall times. Fall time, as seen above, relates directly to switching power dissipation. Storage time, while typically having little effect on power dissipation, must nevertheless be controlled in order to avoid problems of flux imbalance and poor dynamic response with some topologies.

Designers commonly use two techniques to minimize stored-charge-induced transition times. First, the amount of stored charge is kept low by driving the transistor with the lowest possible turn-on base current (i_{b1}). This current is usually chosen to drive the transistor just into "hard" saturation at maximum i_c in order to keep v_{ce} low and minimize on-state losses. Higher base currents would cause increased switching losses without significant improvement in on-state losses. When switching losses are extremely critical, as in high frequency circuits (see Equation 10), a Baker clamp is sometimes used to keep the transistor out of hard saturation altogether. Second, designers seek to remove from the base region as quickly as possible that stored charge which does develop. This is accomplished by reverse biasing the base-emitter junction during turn-off so that an electrical field is set up in the base region which acts to drive out the unwanted minority carriers. Storage and fall times are inversely related to both turn-off curent (i_{b2}) and voltage ($v_{be(off)}$), as shown in Figure 9.

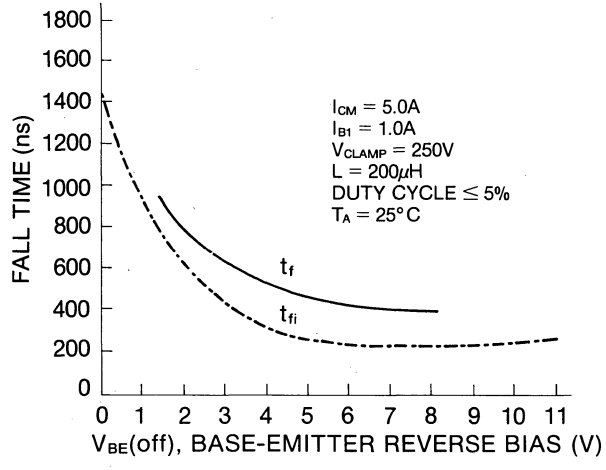

Figure 9 A. Typical Clamped Inductive Turn-Off Switching Times vs $V_{BE(off)}$

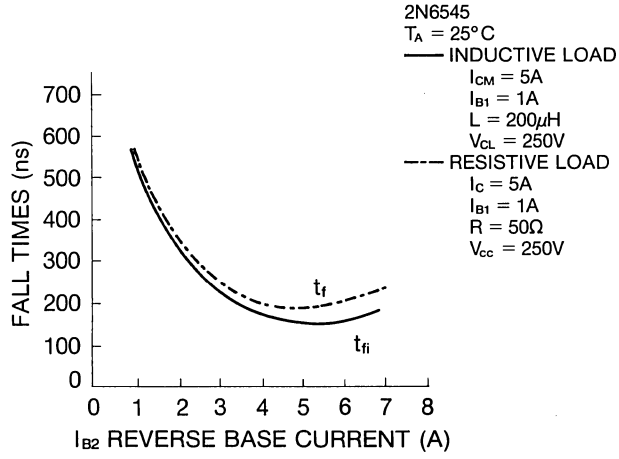

Figure 9 B. Typical Fall Times for Resistive and Clamped Inductive Loads as a Function of Reverse Base Current I_{B2}

This method must remain within the limitations of allowable on-state dissipation and base drive circuit complexity. Further improvements can result from innovative practices such as proportional base drive and "speed-up" capacitors.

2. Snubbers

Figure 10 shows a simple turn-off snubber used to limit switching power dissipation in the transistor by delaying the collector-to-emitter voltage rise until after the collector current has fallen. Power previously dissipated in the transistor is now lost in the snubber resistor R_s. This leads to improved transistor reliability, but does not increase overall circuit efficiency.

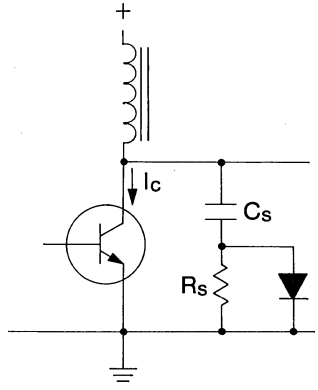

Figure 10 A. Turn-Off Snubber

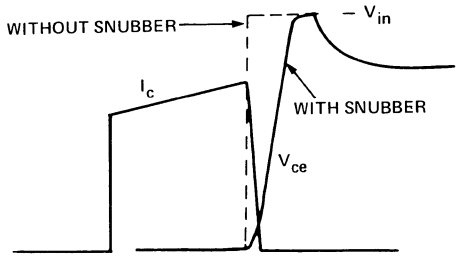

Figure 10 B. Effect of Snubber Network on Turn-Off Characteristics

Capacitor C_s holds v_{ce} low during current turn-off. Resistor R_s is designed to discharge C_s in less than the minimum transistor on time, $t_{on(min)}$. Hence, time constant R_sC_s is chosen to be one half of $t_{on(min)}$:

$$C_s = i_{c(max)} \cdot t_f / v_{ce(max)} \quad \text{(Eq. 11)}$$

$$R_s = t_{on(min)} / 2\ C_s \quad \text{(Eq. 12)}$$

Example - Transistor Losses in a Buck Regulator

To illustrate the relationships among transistor drive conditions, power dissipation, heat sinking, and reliability, we consider a typical transistor operated in the buck regulator circuit of Figure 7. We assume that the following worst-case conditions exist:

$V_{in(max)} = 400V$
$i_{c(max)} = 4A$
$f_s = 50kHz$
$t_{on(max)} = 10\mu s$
$T_{A(max)} = 80°C$

From Figure 4, it is apparent that 400mA of base drive is adequate to insure $v_{ce(on)} \lesssim 0.5V$ at $i_c = 4A$ and $T_J = 25°C$. Figure 3 indicates that this value could increase to 0.75V at $T_J = 150°C$, and that 1.2V is a conservative value for v_{be}. Therefore, from equation 3:

$$\overline{P}_{conducting} = 50kHz \cdot 10\mu s\ (4A \cdot 0.75V + 0.4A \cdot 1.2V) = 1.74W$$

Datasheet curves indicate that t_r and t_f will both be ~250ns. This assumes a turn-off base current (i_{B2}) of 400mA from a −5V source. From equation 10:

$$\overline{P}_{sw} = \frac{50kHz}{2} \cdot 4A \cdot 400V \cdot (250ns + 250ns) = 20W.$$

The total average power dissipation, which is clearly dominated by switching losses, is 21.7W.

$R_{\theta JC}$ for a typical transistor is specified as less than 1.4°C/W, and $R_{\theta CS}$ is ~0.2°C/W for a TO-3 package mounted with a thermally conductive paste.

Designing for a worst-case junction temperature of 150°C, we can expect a transistor MTBF of $7 \cdot 10^7$ hours (from Figure 1). The required heat sink is determined as follows, from equations A1 and A3:

$$150°C = 80°C + 21.7W \cdot (1.4 \frac{°C}{W} + 0.2 \frac{°C}{W} + R_{\theta SA})$$

$$R_{\theta SA} = 1.6 \frac{°C}{W}$$

Figure A1 shows that with natural convection cooling (no fan), a 10 in^3 heat sink would be needed to fulfill this requirement. In order to reduce this volume, we consider using a turn-off snubber which can reasonably be expected to reduce total switching losses by 40% to 12W. Calculating as above, we obtain $R_{\theta SA} = 3.5\,°C/W$, requiring a 5.3 in^3 sink. The addition of a turn-off snubber can therefore decrease the required transistor heat sink volume by nearly one half. Conversely, keeping the same heat sink, the transistor can be operated cooler:

$$T_J = 80°C + 13.7W \cdot (1.4 \frac{°C}{W} + 0.2 \frac{°C}{W} + 1.6 \frac{°C}{W}) = 124°C$$

Now a MTBF of $\sim 1.7 \cdot 10^8$ hours can be anticipated, so that the snubber improves transistor reliability by a factor of ~2.4.

MOSFETS

MOSFET power dissipation in a switching power supply is analogous to that of a bipolar transistor:

$$\bar{P} = \bar{P}_{conducting} + \bar{P}_{switching} \qquad \text{(Eq. 13)}$$

$$\bar{P} = \frac{t_{on}}{\tau} \cdot i_{d(on)} \cdot v_{ds(on)} + \frac{1}{2} \cdot \left(\frac{t_r + t_f}{\tau}\right) \cdot i_{d(on)} \cdot v_{ds(off)}$$

$$\bar{P} = f_s \cdot t_{on} \cdot r_{ds(on)} \cdot i^2_{d(on)} + \frac{f_s}{2} \cdot (t_r + t_f) \cdot i_{d(on)} \cdot v_{ds(off)}$$

where: $r_{ds(on)}$ = drain-to-source resistance in the on state

Values of $r_{ds(on)}$ for MOSFETs are of such a magnitude as to produce greater on-state losses than with the equivalent bipolar transistor operated in saturation. Furthermore, $r_{ds(on)}$ increases markedly with junction temperature, as illustrated in Figure 11. Note that $r_{ds(on)}$, and therefore on-state dissipation, doubles with an increase in junction temperature of 100°C.

Switching times, however, do not increase with temperature, as they do with bipolar devices. Low switching losses somewhat offset the high on-state MOSFET dissipation, particularly at high frequencies. Since MOSFETs are majority carrier devices, they are immune from stored-charge related switching constraints. MOSFET switching times are dependent on the rate at which the input capacitance, C_{iss}, can be charged or discharged by the gate drive circuit. Transition times of 10-20ns are readily achievable with MOSFETs driven from

simple gate circuits. In practical power supply circuits, however, the designer must plan on somewhat slower MOSFET switching in order to avoid rectifier recovery problems. This will be discussed later.

With bipolar transistors, the power supply designer is faced with a complex trade-off among on-state losses, switching losses, drive circuit dissipation and complexity, and reliability. MOSFET designs are more straightforward, largely because on-state and switching losses can be independently optimized.

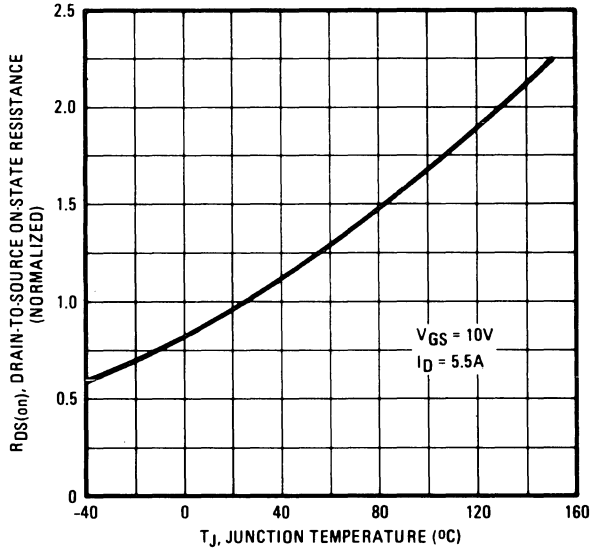

Figure 11. Normalized On-Resistance vs Temperature for UFN342

RECTIFIERS

Rectifier losses are given by the equation:

$$\overline{P} = i_f \cdot v_f \cdot \frac{t_{fb}}{\tau} + \frac{E_{sw}}{\tau} \qquad \text{(Eq. 14)}$$

where: t_{fb} = rectifier forward bias time per cycle

Expected values of v_f can easily be found from manufacturers' specifications and design curves. Calculating E_{sw}, however, requires careful consideration of rectifier reverse recovery characteristics. Figure 12 shows rectifier current and voltage waveforms during reverse recovery. Note that the voltage does not begin to fall appreciably until after the end of period t_a. Significant switching dissipation occurs only during t_b, so that:

$$E_s \simeq \frac{1}{2} \cdot v_{RM} \cdot i_{RM} \cdot t_b \qquad \text{(Eq. 15)}$$

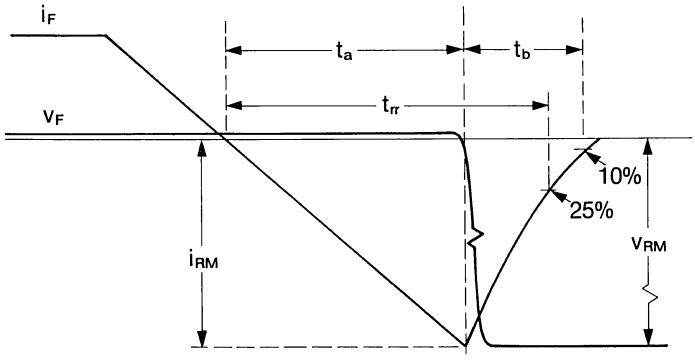

Figure 12. Rectifier Current and Voltage Waveforms During Reverse Recovery

As mentioned earlier, rectifier recovery can also cause increased power dissipation in switching transistors. In the buck regulator circuit of Figure 13 rectifier recovery results in a collector (or drain) current overshoot at turn-on. Since the collector voltage cannot fall until the rectifier is beyond transition period t_a, large power dissipation occurs in the transistor throughout that period. In Figure 14 cross-hatched area II corresponds to transistor switching dissipation in addition to the losses incurred due to t_{ri} (area I). Figure 15 shows how transistor switching losses are affected by the ratio of t_a to t_{ri}. Note that even when t_a is only $0.4 \cdot t_{ri}$, that switching losses are doubled.

Typical Circuit

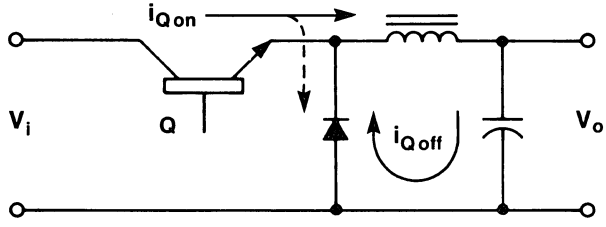

Figure 13. Buck Topology — Typical Circuit in Which Diode Recovery Affects Transistor Dissipation

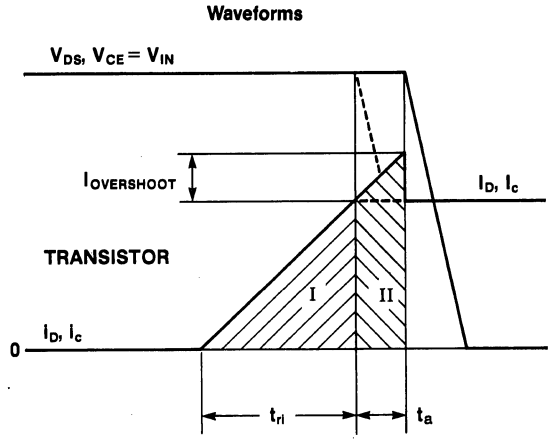

Figure 14. Additional Transistor Losses Due to t_a

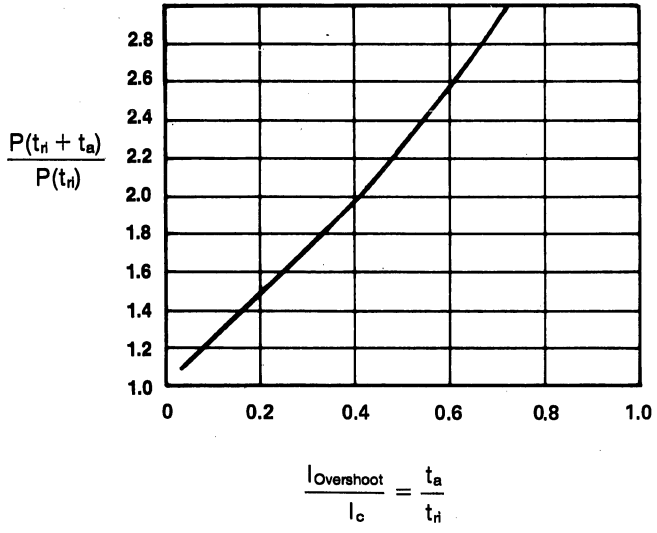

Figure 15. Relative Magnitude of Losses as a Function of t_a/t_{ri}

Rectifier manufacturers normally publish only a single t_{rr} specification, without separate indication of t_a and t_b. The ratio t_a/t_b can vary widely, but lacking other information, a value of 2 is a good approximation. But since transistor losses depend so heavily on t_a, designers may want to obtain more complete characterization as shown in Figures 16 and 17.

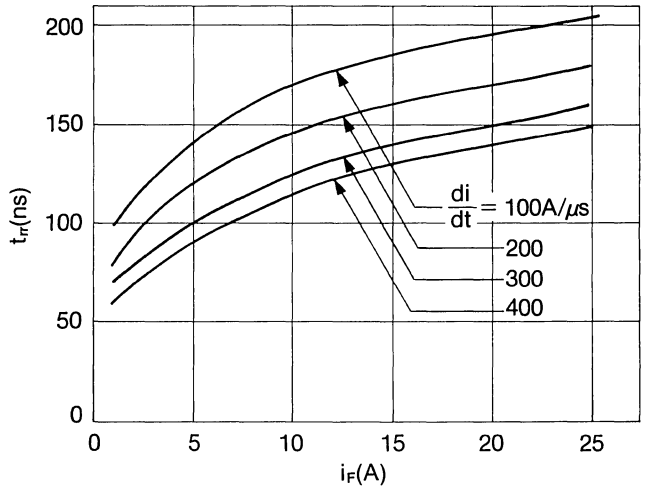

Figure 16. Typical t_{rr} vs i_F and $\frac{di}{dt}$ for a Fast Recovery Rectifier

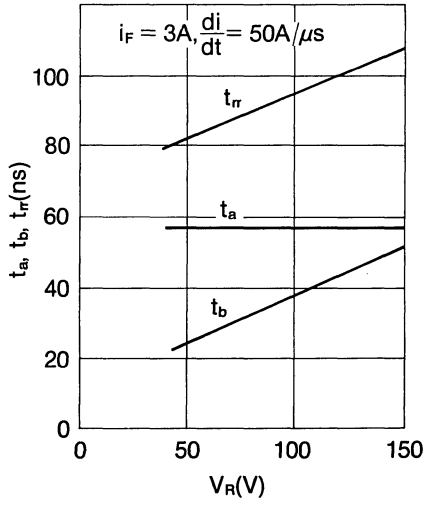

Figure 17. Typical Effect of Reverse-Bias Voltage on Relative Values of t_a and t_b During Rectifier Recovery

SECTION 2. OTHER FAILURE MODES

The previous section described how to design against unreliable semiconductor performance due to excessive average power consumption. The assumptions were made that the entire semiconductor junction or active region was at a safe temperature which varied little through the switching period. These assumptions allowed the use of the very simple time invariant thermal model of Appendix A. However, these assumptions can become invalid if a semiconductor is exposed to transient overheating conditions resulting from excessively high rates of change of current or voltage, or by extreme energy levels. Generalized time-variant thermal models can be developed for such situations, but are too complex to serve as useful design tools. Instead, designers address separately each such potential problem by relating circuit conditions to device ratings or safe operating area curves.

Voltage Spiking

One such potential problem relates to transient voltage "spiking" which can drive semiconductors into their highly-dissipative or possibly unreliable breakdown regions. This problem is particularly important when using Schottky rectifiers because their energy-handling capability when reverse biased can be significantly less than the forward biased capability. The usual approach to reliable designs when voltage spiking is possible is to limit the spike voltage, using clamps or snubbers, to a level below the rated breakdown voltage of the endangered semiconductor device.

Figure 18 shows a buck regulator circuit, in which the catch diode is susceptible to voltage spiking. During turn-on of power switch Q1, parasitic wiring inductance L_W charges to a peak current (i_{pk}) which exceeds the filter inductor current (i_L) by an amount determined by the t_a portion of the catch diode recovery time. After period t_a, the catch diode can no longer support that portion of i_{pk} which exceeds i_L, except by operating in the breakdown region. The solution is to provide an alternative current path through a snubber network as shown in Figure 18. This snubber also helps to reduce conducted and radiated RFI.

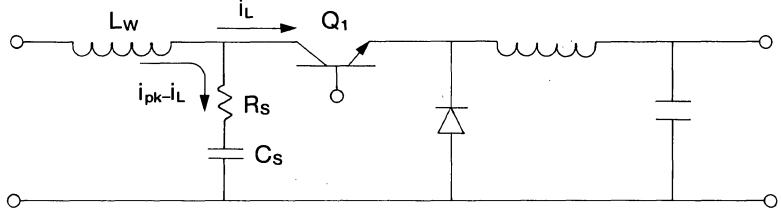

Figure 18. Snubber Prevents Catch Diode Breakdown

Bipolar $E_{s/b}$

During turn-off of an inductive load with a bipolar transistor, current crowding occurs at the center of each emitter region as illustrated in Figure 19. With conditions easily obtainable using typical switching power supply base-drive circuits, high current densities under the

emitter region can cause severe localized heating. Under such conditions, the transistor can lose its ability to sustain its rated voltage and lapse into destructive second breakdown. The result is a collector-to-emitter short.

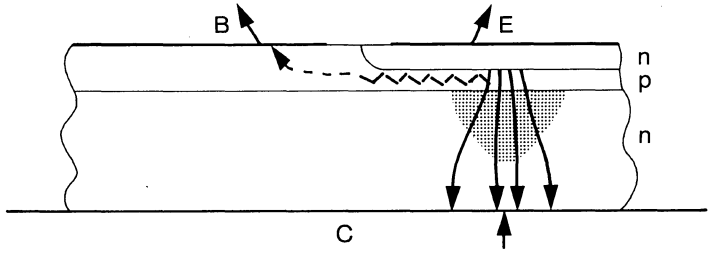

Figure 19. Reverse-Biased Current Crowding

The extent to which current flow is restricted depends largely on the turn-off reverse bias voltage and current across the base-emitter junction. Increased negative bias results in narrower current constriction. While $v_{BE(off)}$ determines the effective device area for dissipating inductive energy, the inductance value L determines the total amount of energy which is converted to heat within that area:

$$E = \frac{1}{2} Li_c^2 \text{ (for unclamped inductive switching)}$$

Therefore, transistor $E_{s/b}$ capability varies qualitatively as shown in Figure 20.

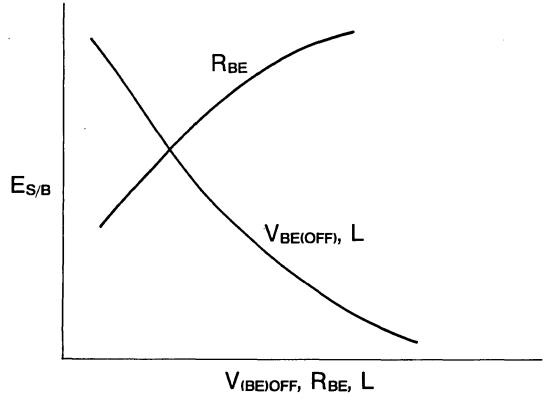

Figure 20. $E_{S/B}$ vs $V_{BE(OFF)}$, L, and R_{BE}

A device which has failed due to $E_{s/b}$ can often be identified, after the fact, by observing the damaged die with a microscope. A localized damage area which has its center near the middle of an emitter "finger" is evidence of $E_{s/b}$ failure. Figure 21 shows an example of this kind of damage.

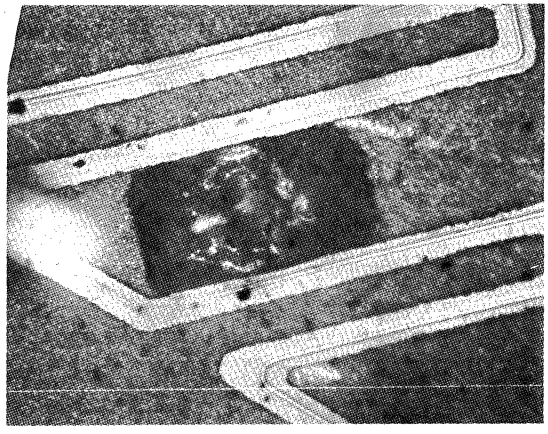

Figure 21. Photomicrograph of Damage Due to $E_{S/B}$

Transistor manufacturers supply several pieces of information which can be used as guides to preventing $E_{s/b}$ failure. First, a minimum "unclamped $E_{s/b}$" specification is sometimes given. This figure guarantees that the given amount of inductive energy can be safely dissipated by the transistor for a specific set of turn-off conditions. Designers must keep in mind, however, that $E_{s/b}$ capability will vary with base drive parameters as shown in Figure 20.

Often, in switched-mode converters, the unclamped $E_{s/b}$ capability of the power transistor is inadequate to handle the highly inductive load. In these cases, designers provide a voltage clamp which diverts inductive energy while keeping the collector-to-emitter voltage below the level sustainable by the bipolar transistor. Figure 22 illustrates the use of non-dissipative clamps in a two-transistor forward converter. Diodes D1 and D2 return inductive energy to the input supply.

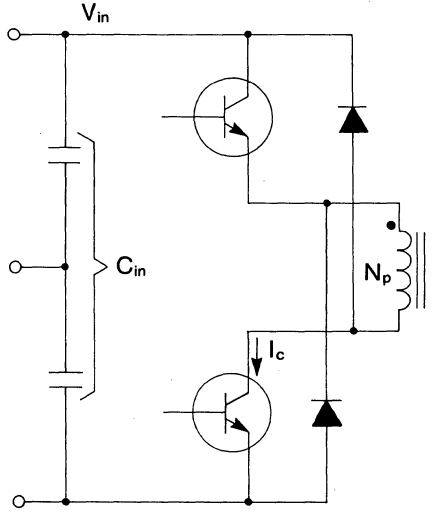

Figure 22. Two-Transistor Forward Converter With Non-Dissipative Voltage Clamps

The second manufacturers' specification relating to $E_{s/b}$ capability is a "sustaining voltage" figure ($V_{cex(sus)}$) for clamped inductive turn-off. This specification puts an upper limit on the allowable clamp voltage for reliable operation of the transistor. Again, however, this figure applies to a particular set of turn-off bias conditions.

A more general characterization is provided by the "reverse biased safe operating area" (RBSOA) curve, shown in Figure 23. This curve essentially defines clamping voltage requirements at collector currents up to the DC current rating of the device. Using this curve, designers can design against potential $E_{s/b}$ problems. Although less conservative, the $V_{cex(sus)}$ specification can be used if the turn-off bias condition applies.

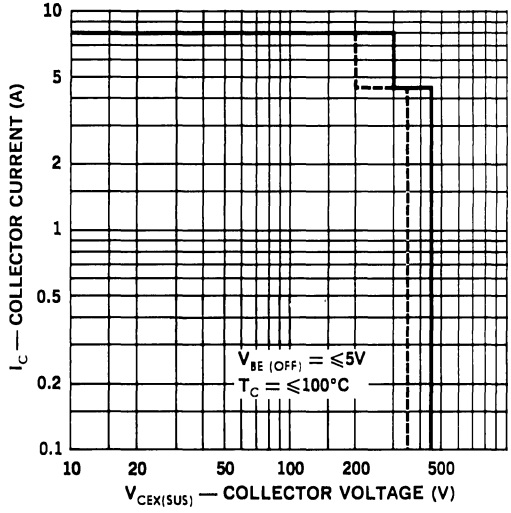

Figure 23. Reverse-Biased Safe Operating Area for a Typical Transistor

Bipolar $I_{s/b}$ and FBSOA

Figure 24 shows "forward biased safe operating area" (FBSOA) curves for a typical transistor under DC or pulsed operation. These curves are a guide to reliable transistor operation in the unsaturated "on" state and during a slow turn-on. (As such, they are often not critical in switching power supply applications.) Three distinct segments of these curves each correspond to a limit imposed by a specific potential failure mechanism.

Region I (Figure 24) is a device limitation based on the fusing characteristics of the collector bond wire. With low v_{CE}, this wire can melt due to resistive heating at current levels which will not cause damage to the semiconductor die. Operation of the transistor below its rated collector current will prevent this type of failure.

At higher voltages, power dissipation (as discussed in Section I of this paper) becomes the limiting factor for reliable operation. In region II, the FBSOA curves follow lines of constant power dissipation. The line for DC operation will vary in position somewhat as a function of thermal mounting condition.

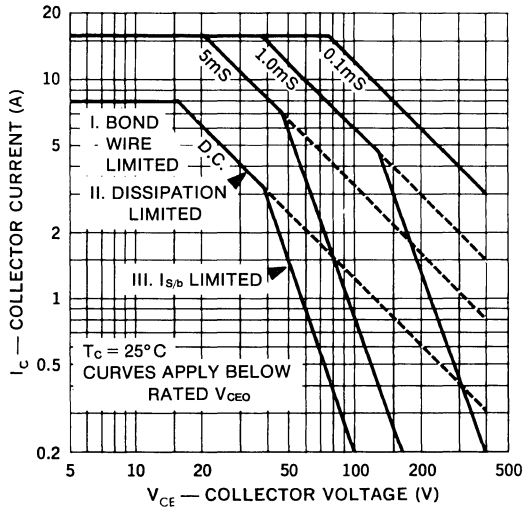

Figure 24. Forward-Biased Safe Operating Area for a Typical Transistor

Finally, in region III, FBSOA is further reduced by forward biased second breakdown ($I_{s/b}$) limitations. Under forward biased operation at high collector-to-emitter voltages, current crowding occurs beneath the periphery of each emitter finger, as shown in Figure 25. High current densities in these areas can result in "hot spots". As with the reverse biased case ($E_{s/b}$), excessive localized temperature extremes can result in destructive second breakdown. The current $I_{s/b}$ at which this can occur varies inversely with v_{CE}. Manufacturers determine the position of the FBSOA curve in region III by taking many devices to second breakdown under a number of v_{CE} and pulse width conditions. A guardband is applied to the results to ensure reliable operation within FBSOA curves.

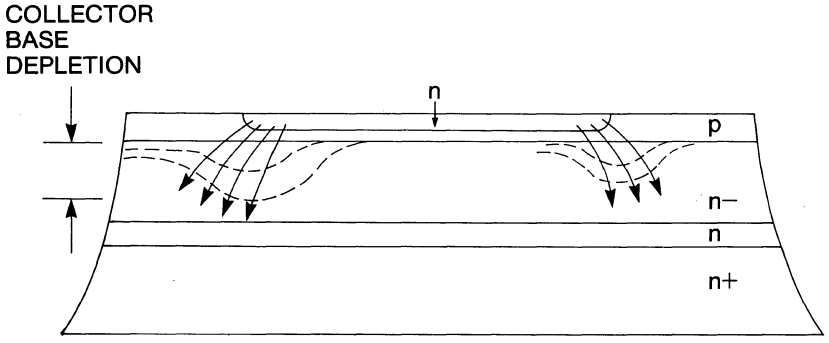

Figure 25. Forward-Biased Current Crowding

A transistor which has experienced $I_{s/b}$ failure may be identifiable by a damaged die area which centers on an emitter finger edge, as shown in Figure 26.

Figure 26. Photomicrograph of Damage Due to $I_{S/B}$

As noted, transistor operating points in switching supplies usually fall well within the area defined by the FBSOA curves. In many topologies, transformer leakage inductance delays turn-on current rise until v_{CE} has fallen, thus preventing operation near the $I_{s/b}$ limit line. With those topologies for which this is not the case, a small inductor ($<100\mu H$) can be purposely connected in series with the collector to serve as a turn-on snubber. Figure 27 illustrates this technique.

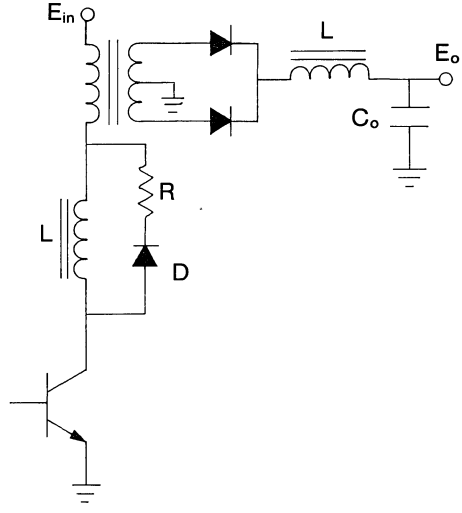

Figure 27. Turn-On Snubber

POWER MOSFET $\frac{dv_{ds}}{dt}$

A highly touted advantage of power MOSFETs is that their safe operating area curves are not limited by second breakdown considerations, as is shown by Figure 28. However, with the high currents and short pulse widths typical of switching power supplies, a MOSFET parasitic effect can limit the user's ability to utilize the entire "SOA". Figure 29 shows a parasitic npn transistor which can cause problems when a MOSFET is operated at high turn-off dv_{ds}/dt.

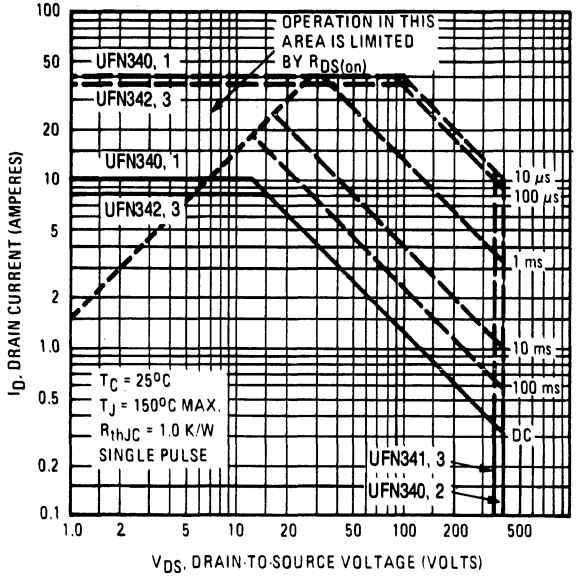

Figure 28. MOSFET Safe Operating Area

If "collector-base" junction capacitance C_{cb} cannot be charged through shorting resistance R_{be} at the desired rate of dv_{ds}/dt (= dv_{ce}/dt), the "base" voltage v_{be} will rise. This can cause turn-on action in the parasitic npn which opposes the desired MOSFET turn-off. The initial effect is delayed turn-off, but observations show that with repetitive pulses second breakdown can occur.

This undesirable effect can be minimized by keeping shorting resistance r_{be} low. Unitrode power MOSFETs use a hexagonal geometry which is optimal for achieving low r_{be}, and have far better dv_{ds}/dt capabilities than do devices with other constructions.

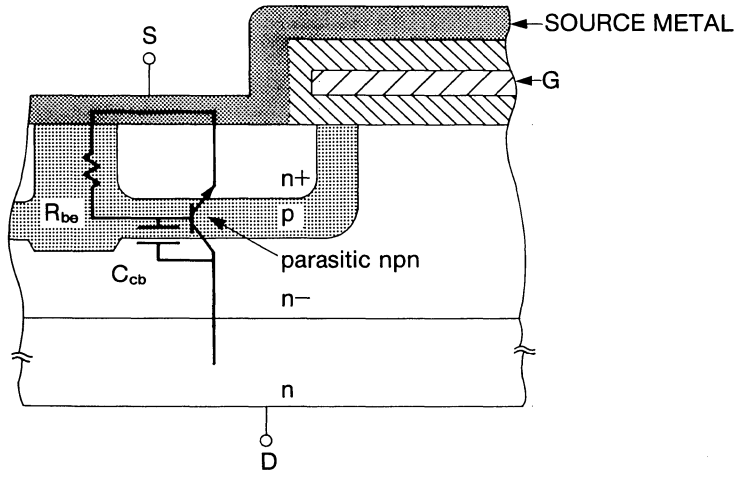

Figure 29. Power MOSFET Construction Showing Parasitic npn

Power MOSFET Gate Voltage

Power MOSFETs are constructed with a very thin (~1000A°) dielectric oxide between the gate and source. Because of its thinness, this oxide is unable to withstand large gate-to-source voltages, and most manufacturers have ±20V ratings for this parameter. MOSFET gates are highly susceptible to damage caused by transient circuit voltages or electrostatic discharge. This is particularly true of low-current devices, because their small die have low gate-to-source capacitance. Evidence of this type of failure includes high gate-to-source leakage current (I_{GSS}) and degraded transfer characteristics ($V_{GS(th)}$, g_{fs}).

A simple method of protecting against gate oxide breakdown is to clamp the gate-to-soure voltage with an avalanche breakdown transient suppressor such as the Unitrode TVS315 (see Figure 30). This device will clamp positive gate transients to approximately 18V, without leading-edge overshoot.

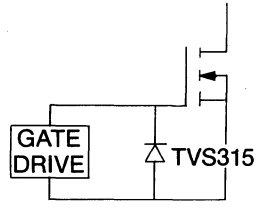

Figure 30. MOSFET Gate Protection

TO-220 PACKAGE MOUNTING AND THERMAL CONSIDERATIONS

The leads of the TO-220 transistors, SCRs, rectifiers and Schottky diodes may be formed, but they are not intended to be flexible or ductile enough for unrestrained lead wrapping.

The TO-220 is generally considered as the economic replacement for the TO-66 power package. Unlike the TO-66, the leads of the TO-220 may be formed if the following considerations are met.

The figures show the typical device and hardware recommended. Several typical configurations of lead forming are illustrated.

The advantages of mounting the flange to the printed circuit board is that improved thermal heat transfer allows operating at higher levels of power dissipation. The individual specification sheets give the safe operating area as a function of a case temperature.

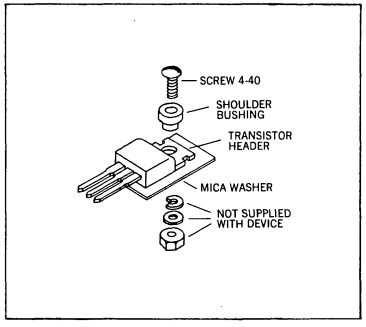

Figure A. Device and Hardware for Insulated Mounting.

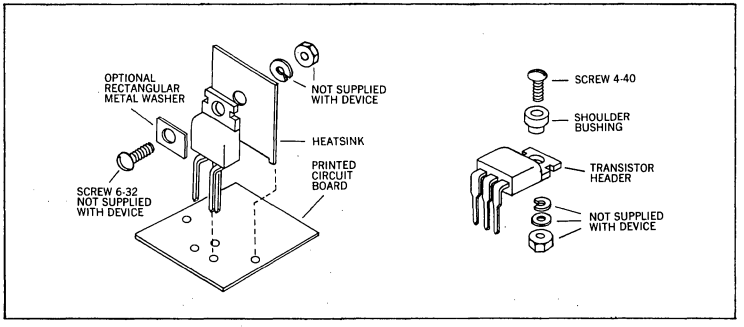

Figure B. Two Alternative Configurations for Axial Strain Relief and Electrical Isolation.

BENDING THE LEADS

Whenever the leads of the T-220 are to be formed, whether by a special fixture or by the use of long-nosed pliers, several important considerations must be followed. Internal damage to the device or lead damage may result if any or all of these precautions are not considered.

1. Minimum bend distance between the plastic body and the bend is $\frac{1}{8}$ inch.
2. The minimum radius of the bend is $\frac{1}{16}$ inch.
3. Avoid repeating bending at the same flexure point.
4. Whenever possible, use one of the lead forming configurations which relieve strain induced by mechanical or thermal loads.
5. Leads should not be bent greater than 90 degrees.
6. Avoid axial pulling or bending that would induce axial strain. The maximum axial component is 4 pounds.
7. Forming fixtures or pliers should not touch the plastic case because axial strain of $\simeq$ .005" could cause irreversible internal damage.
8. The leads must be fully restrained during the lead forming operation to prevent relative movement between the body and the leads.

SOLDERING INTO THE CIRCUIT

The leads on the TO-220 are solderable; however, there are a few precautions that must be observed.

1. Soldering temperature must not exceed 270°C.
2. Maximum soldering temperature must not be applied for more than 5 seconds.
3. Maximum soldering temperature should not be applied closer than $\frac{1}{8}$ inch from the plastic body of the device.

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MOUNTING THE FLANGE

Flange mounting is recommended for maximum power handling applications. A 6-32 machine screw is recommended. Eyeletting (hollow rivet) is acceptable if care is taken not to distort the flange. For insulated mount, a 4-40 screw and a shoulder bushing is recommended (see figure). Suggested material for bushings are: Diallphthalate, fiber-glass-filled nylon, or fiber-glass-filled polycarbonate. Note unfilled nylon should be avoided. The flange should not be directly soldered because the use of lead-tin could produce temperatures in excess of the maximum storage temperature. See the individual specification for the device.

Check list and summary for flange mounting:

1. Use recommended hardware.
2. Always fasten the flange prior to lead soldering.
3. Do not allow the forming tool to come in contact with the plastic body.
4. Maximum mounting torque is 8 inch-pounds.
5. Avoid modifying the flange by machining and do not use oversized screws.
6. Provide axial and transverse strain relief of the leads.
7. Use recommended insulation bushings. Avoid materials that exhibit hot-creep problems.

Thermal Considerations TO-220 Power Transistors

Thermal Resistance, Case to Ambient;
Free Air, No Heatsink ..... 60°C/W typical
Thermal Capacitance
of Package ..... 4.8 watt-seconds/°C
Thermal Time Constant ..... 305 seconds

Device Type	I_C A Continuous	I_C A Peak	Power Dissipation W	Power Derating mW°C	Thermal Resistance Junction Case °C/W
UMT/MJE 13004 UMT/MJE 13005	4	8	75	600	1.67
UMT/MJE 13006 UMT/MJE 13007	8	16	80	640	1.56
UMT/MJE 13008 UMT/MJE 13009	12	24	100	800	1.25
UFN732	4.5	18	75	600	1.67
UFN742	8.0	32	125	1000	1.00

Note: When using a 2 mil MICA washer for electrical isolation, add 0.4°C/W to heatsink thermal resistance.

Thermal joint compound should be used at the interface of the TO-220 flange and the heatsink to which it is attached.

Consider a TO-220 power transistor with a thermal resistance junction to case of 1.25°C/W. The junction temperature produced depends upon the mounting conditions and power dissipated in the circuit. The table below shows junction temperature resulting from 50W of dissipation when mounted on an infinite heatsink at 25°C with different methods of interfacing.

Interface Condition Between Case and Heatsink	Thermal Resistance Case-Heatsink °C/W	Junction Temperature °C
Assumed direct, ideal metallic contact (no interference)	0.0	87.5
1 mil air gap*	1.2	147.5
Thermal compound; Tab screw torqued at 8 inch-pound	0.09	92
2 mil mica washer with thermal compound applied to both surfaces; tab screw torqued at 8 inch pound	0.58	116.5

* A film of air one mil in length has the thermal resistance of ≃ 1.2°C/W.

When using a small heat sink in free air one must consider the additional thermal resistance of the heat sink to ambient and operate at an appropriate power level. For example with an 18°C/W rated sink and thermal compound as above the device will have a junction temperature of 122°C when operating at 5W in an ambient of 25°C free air.

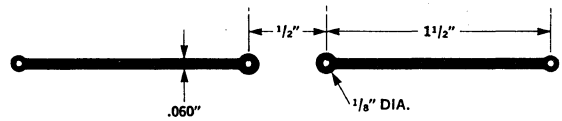
THERMAL DESIGN CONSIDERATIONS FOR LEADED DEVICES

For Lead Mounted Rectifiers and Zeners, for 5 types of mounting.

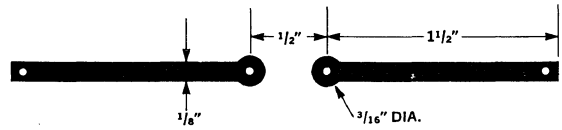
Determining The Power Rating for Your Application.
The information given in this section is presented for straight-forward use by the designer. The value given in this table is $R_{\theta JA}$, the "Total" thermal resistance of the diode and mounting together; no other graphs or tables are needed.

$$P_{max} = \frac{T_{Jmax} - T_{Amax}}{R_{\theta JA}}$$

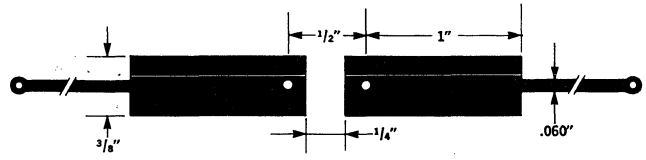
Where: P_{max} is the maximum power that can be dissipated in the device reliably. T_{Jmax} is the maximum of the operating temperature range, usually 175°C, unless derated for a military or hi rel application.
T_{Amax} is the max temp that the ambient reference (air below the device) will reach during operation.
Alternately,
Junction Temp Rise = $PR_{\theta JA}$



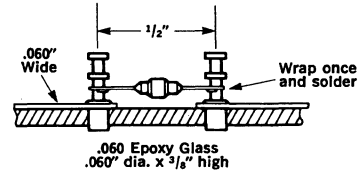
TYPE 1 PC BOARD, LIGHT



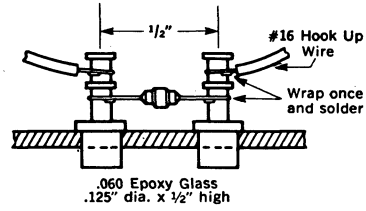
TYPE 2 PC BOARD, MEDIUM



TYPE 3 PC BOARD, HEAVY



TYPE 4 PC BOARD WITH CHESSMEN TERMINALS



TYPE 5 TERMINALS AND HOOK-UP WIRES

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$R_{\theta JA}$ Total Thermal Resistance in Degrees C/Watt					
	Mounting Type				
Type	1	2	3	4	5
1N3611-3614	105	92	75	97	65
1N4245-4249	105	92	75	97	65
1N4461-4489	105	92	75	97	65
1N4736-4764	140	127	110	132	100
1N4942-4946	98	85	68	90	58
1N4954-4996	75	62	45	67	35
1N5063-5117	94	81	64	86	54
1N5186-5189	75	62	45	67	35
1N5186-5190	72	59	42	64	32
1N5550-5553	75	62	45	67	35
1N5614-5622	93	80	63	85	53
1N5802-5806	94	81	64	86	54
1N5807-5811	75	62	45	67	35
TVS 505-528	75	62	45	67	35
UES1101-1106	94	81	64	86	54
UES1301-1306	75	62	45	67	35
UR105-125	142	129	112	134	102
UR205-225	98	85	68	90	58
UT236-347	127	114	97	119	87
UT249-363	110	97	80	102	70
UT251-364	105	92	75	97	65
UT261-268	98	85	68	90	58
UT2005-2060	97	84	67	89	57
UT3005-3060	85	72	55	77	45
UT4005-4060	80	67	50	73	40
UTR01-61	127	114	97	119	87
UTR02-62	98	85	68	90	58
UTR10-60	176	163	146	168	136
UTR2305-2360	97	84	67	89	57
UTR3305-3360	85	72	55	77	45
UTR4305-4360	80	67	50	72	40
UTX105-125	142	129	112	134	102
UTX205-225	98	85	68	90	58
UTX3105-3120	85	72	55	77	45
UTX4105-4120	80	67	50	72	40
UZ706-140	94	81	64	86	54
UZ4706-4120	75	62	45	67	35
UZ5706-5140	75	62	45	67	35
UZ7706L-7710L	73	60	43	65	33
UZ8706-8120	140	127	110	132	100
UZS 306-440	94	81	64	86	54

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Introduction

This guide presents an overview of power conversion technology and lists the major features of the most popular topologies. Basic guidance in selecting the proper topology and its associated components is provided, first through listing the advantages and disadvantages for each topology and secondly through component selection tables which are based on topology, output power and other significant factors.

Clarification of some of the basic questions related to power conversion technology are presented in Appendix I; furthermore, the task of designing of a power supply is made easier by providing some important design equations and related information in Appendix II.

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Overview of Power Supply Technology

In recent years, there have been many significant technological changes in power supply design. These became possible with advances in power transistors, integrated circuits, capacitors, and design techniques. This has resulted in lower cost per watt with improved performance.

Techniques for conversion of unregulated DC voltage into the desired DC level continue to center around linear and switching regulators. Linears continue to be heavier, larger, and less efficient than switchers, but they are still less expensive, less complex, and offer better ripple, noise and EMI/RFI specs. Advances affecting linear regulators have been in capacitors with greater "CV" product in small sizes, three terminal regulators with better regulation specs, (like the UC7800A and UC7900A) and control integrated circuits like the UC3834 which offer the ability to build a high efficiency linear using PNP transistors.

Switching regulators continue to incorporate the most changes with many innovations and improvements in technology. Multiple output switchers (40 to 150 watts) are used in high volume for home computers and games. Their cost is setting new record lows, at 40 to 60 cents per watt. Large multiple output switchers (150 to 500 watts) are benefiting from Schottky rectifiers, like the USD TO220 series rectifiers, and broader selection of UC integrated circuits designed to replace large quantities of discrete parts needed to control pulse width modulation, current limit, over-voltage protection, and a variety of other control and monitor functions.

Conventional pulse width modulation (PWM) techniques are being challenged by two major innovations. One is the current mode control integrated circuit, like the UC3842 and UC3846, offering faster and more predictable response than conventional PWM techniques. Another is the voltage feed forward PWM technique which provides faster correction for input voltage changes. A third innovation allows an order of magnitude upward change in switching frequency. The latest technique, the series resonant power supply, operates from 100KHz to several megahertz. Using a sine wave instead of a square wave, this results in lower EMI, lower switching losses and practical reverse recovery requirements.

Unitrode's power MOSFET's are prime contributors to new designs, including the series resonant technique. MOSFET's are enabling power supply designers to raise PWM switching frequencies from 25KHz to 100KHz and up. This results in a reduction in size of the magnetic and capacitive components.

Designers are continuing to advance the state of the art in switching regulator technology by using new products which help to reduce the size and weight of power packages. Power MOSFET's, Integrated Circuits, high speed platinum and Schottky rectifiers are such examples.

In an Uninterruptible Power Supply (UPS), some interesting advances are taking place. Small UPS products are emerging to serve the home and office computer market. Another new concept is Direct UPS (DUPS). Only a few small computers have incorporated this option, but its simplicity should attract widespread attention in the years to come. DUPS simply connects battery storage to the DC bus in the system power supply, instead of having to regenerate AC power. To make this a usable concept, designers will need to plan ahead for it in the early stages of system and power supply development.

How to use this "Guide"

The most common power sources and output voltages in a switching regulated power supply are shown in table I. The output voltage and its load current will depend upon the application. The power supply designs are tailored for each individual application.

There is no simple procedure in selecting the right topology for a given application; however, the factors which influence the selection of topology are identified in detail in the next section. One or more of the factors, listed in order of importance for a given application, will help to select the best topology.

1) Efficiency
2) Single vs. multiple output
3) Power output
4) Input voltage source
5) Maximum output current from each output
6) Performance
   - RFI
   - transient response
   - output ripple etc...
7) Size, weight & volume
8) Cost
9) Reliability

The chart shown in figure II provides an overview of most commonly used topologies, and lists the most important characteristics, in brief, for each topology. These characteristics are matched against applications needs for a proper choice of the topology. Further details for the selected topology should be evaluated for the final choice. Guidance for this evaluation is provided in section IV.

Most commonly used topologies in various applications are listed below:

A. Computer Main Frames
   - full-bridge switching regulator
   - current fed followed with a full-bridge
   - step-down or linears in secondary outputs

B. Personal computer, Word processor, Point of sale terminals
   - flyback switching regulator
   - half-bridge switching regulator
   - single transistor or two transistor forward converter
   - step-down or linears in secondary outputs

C. Home computer
   - linear regulator
   - low cost flyback regulator

D. Printer
   - linear regulator
   - step-down regulator
   - flyback regulator

E. PBX systems (switching station)
   - two transistor forward converter
   - half and full bridge regulator
   - step-down or linears in secondary outputs

F. CATV
   - step-down
   - linear regulator
   - flyback regulator

G. Video games
   - linear regulator
   - step-down regulator
   - flyback regulator
   - half-bridge regulator

H. Portable equipment (medical)
   - buck regulator
   - linear regulator

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The component selection tables for the switching transistor are developed based on topology, input voltage and output power. The rectifier selection table uses the output voltage and output load current to determine the proper rectifier. The component selection table includes the effect of PWM regulation with 2:1 variation of input voltage.

The next section contains guidelines for selecting the appropriate PWM control circuit for a selected topology. It also describes features for various power supply supervisory circuits, support and monitoring circuits.

Appendices include answers to most often asked questions about power conversion technology and some design equations which will be helpful in the design of a switching regulated power supply.

MOST COMMON POWER SOURCES FOR SWITCHING POWER SUPPLIES

VOLTAGE	DC RANGE USED FOR WORST CASE DESIGN	WHERE USED
A. A.C. Lines		
100V, 60Hz	90–165V	Japanese Power Lines
117V, 60Hz	100–190V	U.S. Power Lines
220/230V, 50Hz	200–380V	European Power Lines
B. Transformer Secondary	Output Voltage:	
25V AC	20–40V	From AC lines in small equipment
C. DC Source		
+12V	7–15V	Automotive batteries
+24V	14–30V	Truck, etc., batteries
+28V	18–36V	Aircraft
+48V	42–56V	Telecommunications
+400V	300–450V	Mines

COMMON OUTPUT VOLTAGE FROM POWER SUPPLIES

VOLTAGE	TYPICAL APPLICATION
A. −5V, 2.5V	ECL Logic
B. 3 to 18V, [Typical 12V]	CMOS
C. +5V	Bipolar Logic
D. −5 to −12V	PMOS
E. +5 to +12V	NMOS
F. ±12V, ±15V, +30V	Operational Amplifier, Commercial Aircraft
G. +28V	Aerospace, IC Regulators, DC Motors
H. +48V	Telephone
I. 1.5KV to 8KV	Focus Voltage CRT
J. 7KV to 30KV	Anode Voltage CRT

Table I. *Possible input-output requirements of a switching regulated power supply.*

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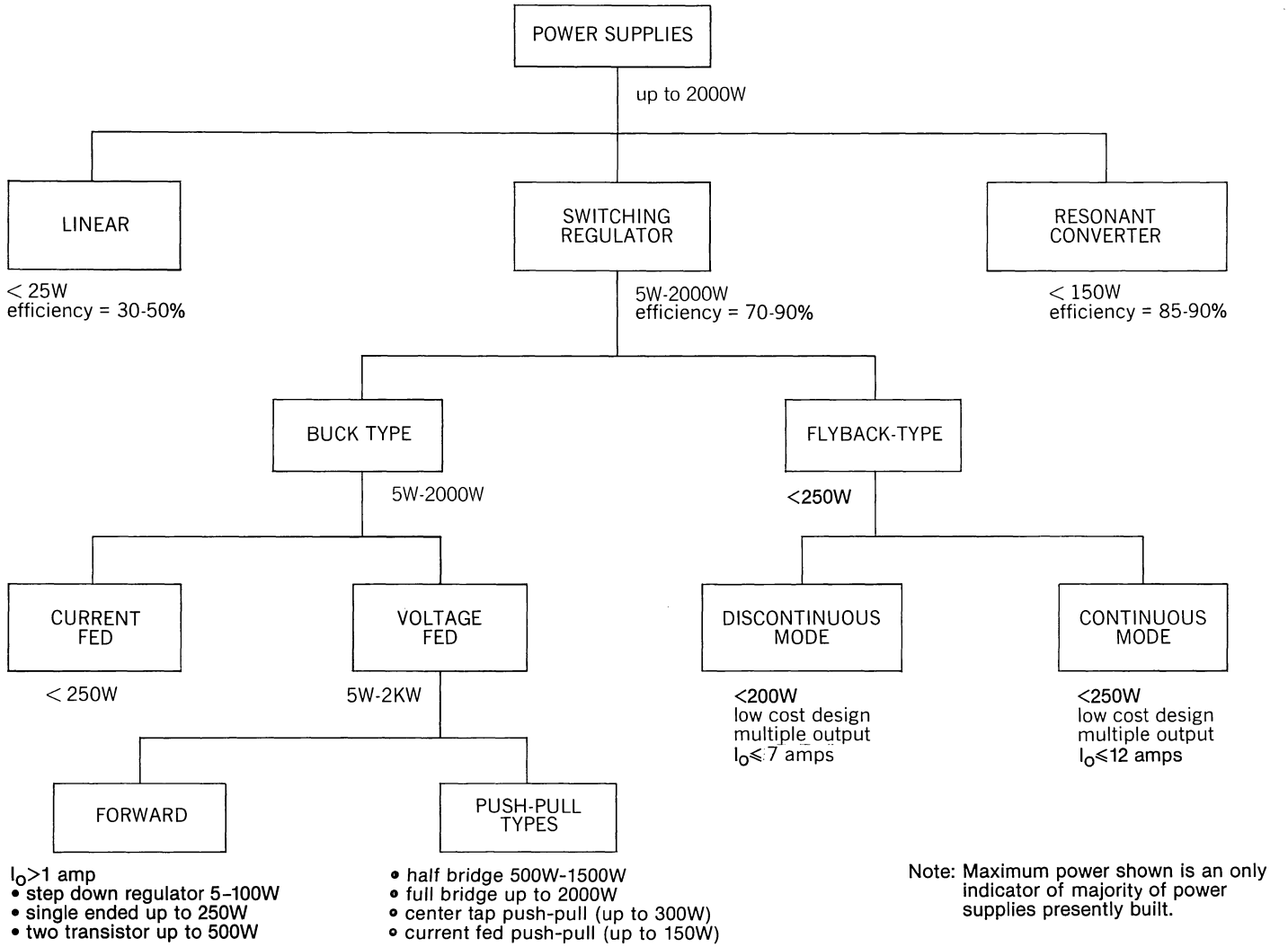

Figure II. *Overview of Power Supply Technology*

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Power Conversion Technology

This section considers advantages, disadvantages and component selection for various topologies which are commonly used for power conversion.

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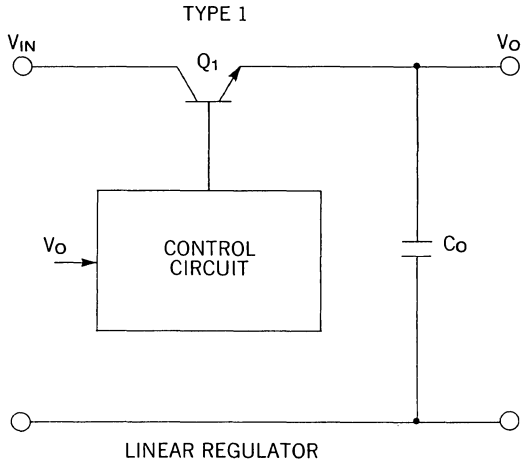
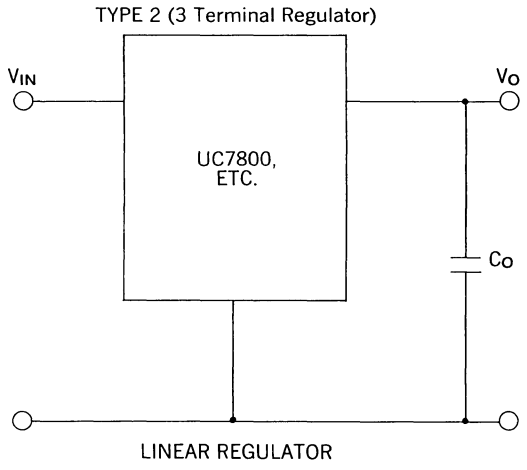
LINEAR REGULATOR

Output Power: Up To 25 Watts





IT'S USED FOR:

- Extremely low ripple and noise.
- Low input to output voltage difference.
- Tight regulation.
- Fast transient response.

ADVANTAGES

- Low output ripple and noise
- Fast transient response
- Low cost under 1.0 amp of output current
- No RFI or EMI
- No need for high speed switching transistor

DISADVANTAGES

- Efficiency
  Main Regulator ≈ 45%,
  Post Regulator ≈ 65%,
  (with ± 5% line).
- Large heat sink needed to remove the heat, bulky in size
- In a 25 watt off line power supply, bulky 60Hz transformer is required
- Lower watt per cubic inch compared to switching regulator

TRANSISTOR SELECTION (Type 1)

BV_{CEO} or $BV_{DSS} \geq 1.2\ V_{in(max)}$

$I_{c(max)}$ or I_D (max) $\geq I_{o(max)}$

$I_{S/B} \geq I_{o(max)}$ at $V_{in(max)}$ at 125 °C junction.

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Linear Regulator

A. DEVICE SELECTION (Type 1)

IC control circuit (used for both positive and negative regulators)

UC3834 High Efficiency
Linear Regulator
Low Input-Output
Differential

Output transistor:

Q_1 Positive Regulator (>200mA)
2N2907 and 2N4150, GE D44
Negative Regulator (>200mA)
2N4150

- Minimum V_{IN}—V_{OUT} less than 0.5V at 5A Load with External Pass Device
- No additional pass device required for $I_O \leqslant 200mA$
- Adjustable Low Threshold Current Sense Amplifier
- Under- and Over-Voltage Fault Alert with Programmable Delay
- Over-Voltage Fault Latch with 100mA Crowbar Drive Output

B. DEVICE SELECTION (Type 2)

Positive Linear Regulator

Output Current	Output Voltages*			
	+5V	+12V	+15V	adjustable +1.2 to 37V
1.0A	UC340-05K UC340-05T	UC340-12K UC340-12T	UC340-15K UC340-15T	
1.5A	UC7805CK UC7805CT 5V±4%	UC7812CK UC7812CT 12V±4%	UC7815CK UC7815CT 15V±4%	UC317T ±0.1%
1.5A	UC7805ACK UC7805ACT 5V±1%	UC7812ACK UC7812ACT 12V±1%	UC7815ACK UC7815ACT 15V±1%	
3.0A				UC350K

*Max. Input Voltage≈ +40V

Negative Linear Regulator

Output Current	Output Voltages*			
	−5V	−12V	−15V	adjustable −1.2 to −37V
1.0A	UC320-05K UC320-05T	UC320-12K UC320-12T	UC320-15K UC320-15T	
+1.5A	UC7905CK UC7905CT −5V±4%	UC7912CK UC7912CT −12V±4%	UC7915CK UC7915CT −15V±4%	UC337T ±3%
+1.5A	UC7905ACK UC7905ACT −5V±1%	UC7912ACK UC7912ACT −12V±1%	UC7915ACK UC7915ACT −15V±1%	

*Max. Input Voltage≈ −40V

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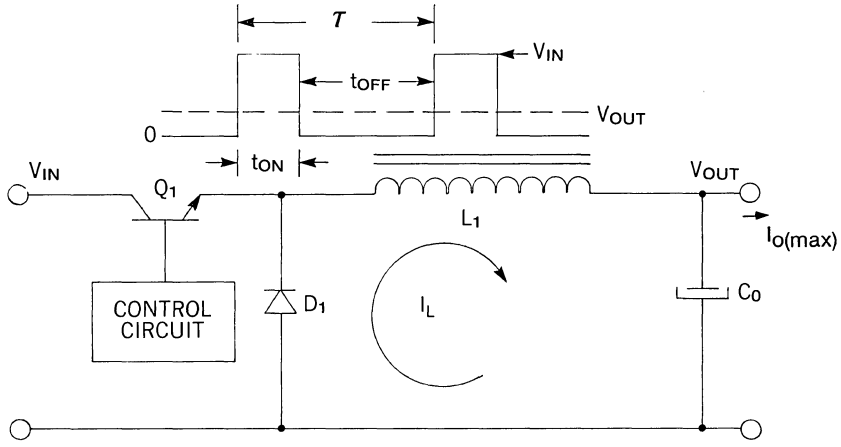
SWITCHING REGULATOR

BUCK REGULATOR—(Step Down Regulator)

Output Power: 5 Watts And Up



IT'S USED FOR:

- High efficiency
- Ease of thermal management
- When only one or two outputs are required
- Large input to output voltage difference
- Spot regulation/point of load
- Battery operated portable equipment

ADVANTAGES

- Provides high efficiency
- Lower cost, size and weight
- Tolerant of line input variations

DISADVANTAGES

- No DC isolation between input and output (to protect output load: it requires a crow-bar and fuse).
- Provides only one output per circuit
- Output ripple higher than Linear
- Slow transient response compared to Linear
- Power circuit has 2 pole roll-off characteristics

TRANSISTOR SELECTION

BV_{CEO} or $BV_{DSS} \geq 1.2\ V_{in}$ (max)

I_C (max) or I_D (max) $\geq 1.2\ I_{o(max)}$

$R_{DS\ (on)} \approx \frac{.75}{I_D} \Omega$ for $V_{in} \leq 100V$

$R_{DS\ (on)} \approx \frac{2}{I_D} \Omega$ for $V_{in} \geq 100V$

RECTIFIER SELECTION

Catch Diode

$V_R \geq 1.2 V_{in(max)}$

$I_F \geq I_{o(max)}$; $I_{F(avg)} = I_O$ (max) $(1\text{-}D_{min})$

Reverse recovery of diode should be at least 3 times faster than the current rise time of the transistor.

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Buck Regulator (Step Down Regulator)
Semiconductor Component Selection

Max. Output Load Current	Max. Input Voltage					
	40V	60V	80V	100V	190V	380V
2A	Hybrid: PIC660	PIC601	PIC602			
	Transistor: UFN523	UFN522	UFN522	UFN631	UFN733	UFN833
	Rectifier: USD645* or UES1401 or UES1301 (axial)	UES1402 or UES1302	UES1402 or UES1302	UES1403 UES1303	UES1305 UES1411	UES1412
5A	Hybrid: PIC660	PIC661	PIC662			
	Transistor: UFN531	—	—			
		UFN530	UFN530	UFN641	UFN743	UFN841
	Rectifier: USD645* UES1401	UES1402	UES1402	UES1403	UES705 or UES1411	UES1412
10A	Hybrid: PIC625	PIC626				
	Transistor: UFN541	UFN540	UFN540	UFN251	UFN351	UFN451
	Rectifier: USD845* or UES1501	UES1502	UES1502	UES1503	UES705	
15A	Hybrid: PIC645	PIC646	PIC647			
	Transistor: UFN151	UFN150	UFN150	UFN251	—	—
	Rectifier: UES701	UES702	UES702	UES703	UES705	
20A	Transistor: UFN151	UFN150	UFN150	UFN251 (x2)	—	—
	Rectifier: UES701	UES702	UES702	UES703	UES805	
50A	Rectifier: USD545* or UES801	UES802	UES802	UES803	UES805	

PIC600 series are power output stages for buck regulators which contain switching transistors and catch diodes.

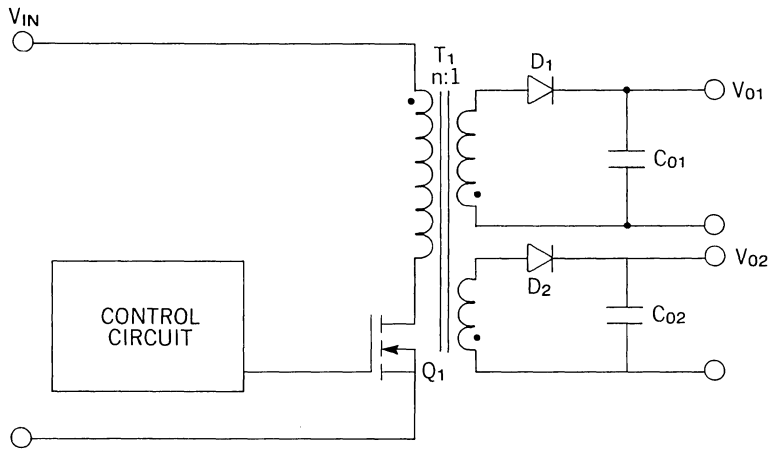
*Input voltage 35 volts max.

RECOMMENDED PWM CONTROL CIRCUIT: Refer to section "Selection of PWM control circuit"

Nomenclature: UFN: Power MOSFET; USD: Schottky Rectifier; UES: t_r = 20–50ns Rectifier; SES: t_r = 100ns Rectifier; PIC: Hybrid Circuit.

DISCONTINUOUS MODE FLYBACK REGULATOR

Power Output: Up To 200 Watts



FLYBACK REGULATOR

IT'S USED FOR:

- Low cost
- Multiple outputs
- Wide variations in output load currents
- Providing input to output isolation
- Output current less than 7 Amps for any given output
- Good voltage tracking between outputs

ADVANTAGES

- All the output voltages track each other
- Output voltage can be sensed through power transformer
- Transformer is 3 times smaller than continuous mode flyback regulator.
- Fast transient response
- Slow (trr) rectifier is acceptable in outputs
- Only one diode in secondary per output
- No filter inductor in secondary
- Easy to stabilize the closed loop. (single pole)

DISADVANTAGES

- Large peak current in the switching diodes and transistors.
- Output capacitor must be twice as large (to obtain lower ESR) when it is compared with continuous mode.
- In some cases V_F matching is required to obtain proper output DC level for multiple outputs.

TRANSISTOR SELECTION

$$BV_{CEO} \geq 1.2 V_{in(max)}$$

$$BV_{CER} \text{ or } BV_{DSS} \geq V_{in(max)} + nV_O + \left\{ \begin{matrix} \text{leakage} \\ \text{inductance} \\ \text{spike} \end{matrix} \right\}$$

$$I_{cpk} \text{ or } I_{Dpk} \geq \frac{2\ P_O}{\eta\ V_{in(min)} D_{max}}$$

$$R_{DS(on)} \approx \frac{2}{I_D} \Omega$$

RECTIFIER SELECTION

$$V_R \geq V_O + \frac{V_{in(max)}}{n}$$

$$I_{F_{pk}} \geq \frac{2\ P_O}{(1\text{-}D_{max})\ V_O} \qquad I_{F(avg)} = 0.4 I_{F_{pk}}$$

Slow diode (100-400ns) is acceptable due to low di/dt during turn-off.

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DISCONTINUOUS MODE FLYBACK REGULATOR

A. TRANSISTOR SELECTION

Output Power	Input voltage 117/ 220V AC line input	Input voltage 117V AC line input
50W	UFN1130	UFN742
100W	UFN1130	UFN740
150W	UFN1130	UFN740
200W	UFN1150	UFN350

B. RECTIFIER SELECTION

I_O = Output Current	V_O = Output Voltage				
	+5V	+12V	+15V	+28V	+48V
0.5A	USD1130	SES5001	SES5002	SES5003	UES1104
1.0A	USD1130	SES5002	SES5002	SES5003	UES1304
3.0A	USD635	SES5402 SES5301 (axial)	SES5302 (axial) SES5402	SES5303 (axial) SES5403	SES5404
5.0A	USD835	SES5401	SES5402	SES5403	SES5404
10A	USD935	UES1402 SES5501	SES5502	SES5503	SES5404
15A	USD935	UES701	UES702	UES703	

Snubber Diode —1N3613, 1N3614

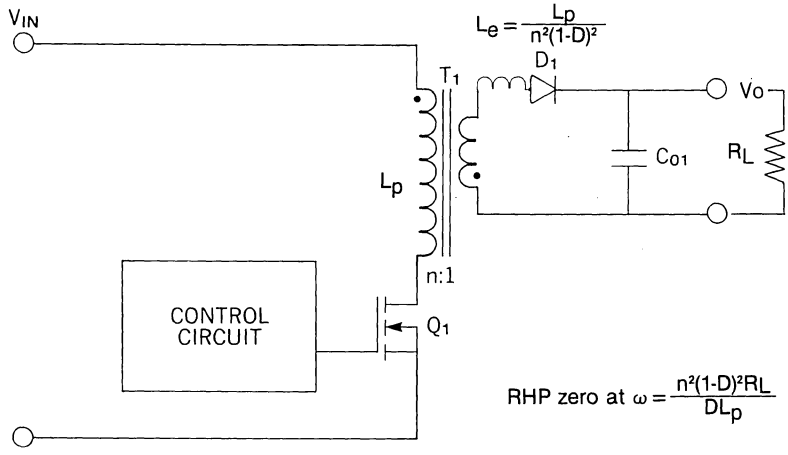
Clamp Diode —1N3613

C. CONTROL CIRCUIT SELECTION

Refer to section "Selection of PWM Control Circuits"

CONTINUOUS MODE FLYBACK REGULATOR

Power Output: Up To 250 Watts



FLYBACK REGULATOR

IT'S USED FOR:

- Low cost
- Multiple outputs
- Wide variation in output load current
- Output current is less than 15A per output
- Providing input to output isolation

ADVANTAGES

- Output filter cap is half the size when it is compared with discontinuous mode flyback
- Peak diode and transistor current is approximately ½ times discontinuous mode

DISADVANTAGES

- Rectifier diodes should be 4 times faster than discontinuous mode flyback (trr ≅ 25-100 ns)
- Transformer T_1 is larger than discontinuous mode flyback regulator
- Difficult to stabilize the loop because the power circuit has 2 poles and RHP zero

TRANSISTOR SELECTION

$$BV_{CEO} \geq 1.2\ V_{in(max)}$$

$$BV_{CER} \text{ or } BV_{DSS} \geq V_{in(max)} + n\ V_O + \left\{ \begin{matrix} \text{leakage} \\ \text{inductance} \\ \text{spike} \end{matrix} \right\}$$

$$I_{c(max)} \text{ or } I_{D(max)} \approx \frac{(1.2)\ P_O}{\eta\ V_{in(min)}\ D_{(max)}}$$

$$R_{DS(on)} \approx \frac{2}{I_D} \Omega$$

RECTIFIER SELECTION

$$V_R \geq V_O + \frac{V_{in(max)}}{n}$$

$$I_{Fpk} \geq \frac{1.2\ P_O}{(1-D_{max})V_O} \qquad I_{F(avg)} = 0.7 I_{Fpk}$$

Rectifiers with fast reverse recovery are required.

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A. TRANSISTOR SELECTION

Output Power	Input voltage 220V AC line or 117V line with doubler	Input voltage 117V AC line
50W	UFN1130	UFN732
100W	UFN1130	UFN742
150W	UFN1130	UFN740
250W	UFN1150	UFN350

B. RECTIFIER SELECTION

I_O = Output Current	V_O = Output Voltage				
	+5V	+12V	+15V	+28V	+48V
0.5A	USD1130	UES1001	UES1002	UES1003	UES1104
1.0A	USD1130	UES1001	UES1102	UES1103	UES1304
3.0A	USD635 1N5821 (axial)	UES1401 UES1301 (axial)	UES1402 UES1302 (axial)	UES1403 UES1303 (axial)	UES1404 UES1304 (axial)
5.0A	USD835	UES1401	UES1402	UES1403	UES1404
10A	USD935	UES1501	UES1502	UES1503	UES1504
15A	USD935	UES1501 UES701	UES1502 UES702	UES1503 UES703	

Snubber Diode —1N3613, 1N3614

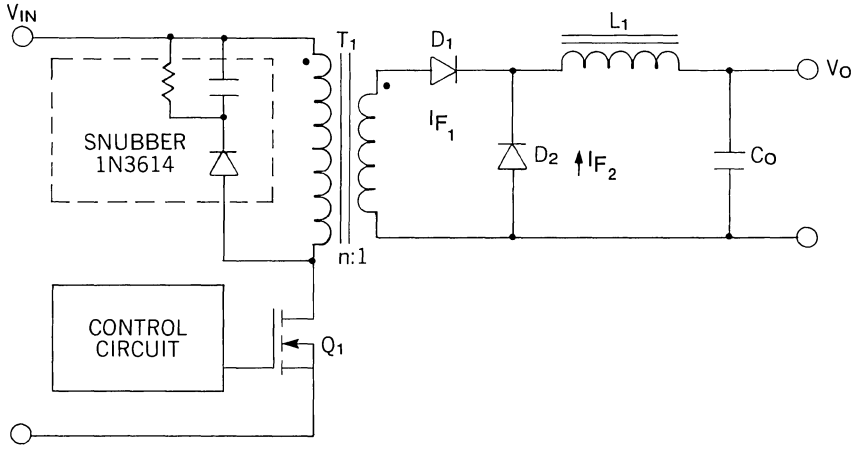
Clamp Diode —1N3613

C. CONTROL CIRCUIT SELECTION

Refer to section "Selection of PWM Control Circuits"

SINGLE ENDED FORWARD CONVERTER

Power Output: Up To 250 Watts



FORWARD CONVERTER

IT'S USED FOR:

- Low output noise and ripple voltage
- Avoiding flux symmetry problems

ADVANTAGES

- Drive circuit is simpler compared to other forward converters
- Only one switching transistor is required

DISADVANTAGES

- Higher cost than flyback design
- Inefficient use of power Transformer T_1 ($D_{max} \leq 50\%$) compared to bridge or push-pull topology
- Blocking voltage of transistor Q1 is 2 times input voltage
- Regulation problem at light load for multiple output
- Power circuit has 2 pole small signal characteristic

TRANSISTOR SELECTION

$$V_{CEO} \geq 1.2\ V_{in(max)}$$

$$BV_{CER} \text{ or } BV_{DSS} \geq V_{in(max)} \frac{1}{1\text{-}D_{max}} \left\{ \begin{matrix} \text{leakage} \\ \text{inductance} \\ \text{spike} \end{matrix} \right\}$$

$$I_{c(max)} \text{ or } I_{D(max)} \geq \frac{1.2\ P_O}{\eta\ V_{in(min)} D_{max}}$$

$$R_{DS(on)} \approx \frac{2}{I_{D(max)}} \Omega$$

RECTIFIER SELECTION

Output rectifier D1

$$V_R \geq \frac{1.2\ (V_O + V_F)\ V_{in(max)}}{V_{in(min)}\ D_{max}} + \left\{ \begin{matrix} \text{leakage} \\ \text{inductance} \\ \text{spike} \end{matrix} \right\}$$

$$I_{F_{pk}} \geq I_{o(max)}$$

$$I_{F1(avg)} = D_{(max)}\ I_{o(max)}$$

$$I_{F2(avg)} \approx (1\text{-}D_{min}) I_{o(max)}$$

D_1 Reverse recovery≈100–200 ns

D_2 Reverse recovery≈25–100 ns

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SINGLE ENDED FORWARD CONVERTER

A. TRANSISTOR SELECTION

Output Power	Input voltage 220V AC line or 117V line with doubler	Input voltage 117V AC line	Input voltage 12,24,28,48 Vdc
75W	UFV1130	UFN732	UFN500 series (TO-220) or UFN100 series (TO-3) 50 to 100V, 4 to 40A
150W	UFN1130	UFN740	
250W	UFN1150		

B. RECTIFIER SELECTION

I_O = Output Current	V_O = Output Voltage			
	±5V	±12, ±15V	±28V	±48V
1A, 2A	USD640C 1N5819 (axial)	UES2402 UES1002	UES2404 UES1104 (axial)	UES1105
5A	USD640C	UES2402	UES2404	UES1305
10A	USD740C	UES2402	UES2404	UES2605
20A	USD345C	UES2602 UES1502		
40A	USD545 (DO-5)			
70A	USD545 (DO-5)			

Snubber Diode 1N3613, 1N3614

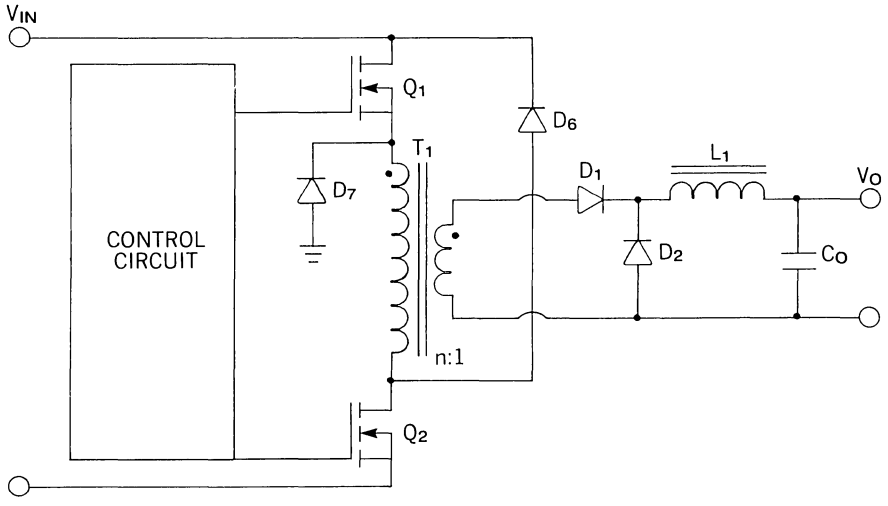
Clamp Diode 1N3614

C. IC SELECTION

Refer to section "Selection of PWM Control Circuits"

B. TWO TRANSISTOR FORWARD CONVERTER

Power Output: Up To 500 Watts



FORWARD CONVERTER

IT'S USED FOR:

- High input and transient voltage
- High efficiency and reliability
- Low output ripple and noise

ADVANTAGES

- Lower transistor voltage rating compared to single ended circuit
- High efficiency because of simple non-dissipative snubber and clamp
- Larger input transient capability

DISADVANTAGES

- Dual output drive circuits required
- Poor transformer utilization compared to push-pull and half bridge topology
- Other disadvantages are same as for single ended circuit
- Power circuit has 2 pole small signal characteristics

TRANSISTOR SELECTION

BV_{CEO} or $BV_{DSS} \geq 1.1 V_{in(max)}$

$$I_{D(max)} \text{ or } I_{c(max)} \geq \frac{1.2\ P_O}{\eta\ V_{in(min)}\ D_{max}}$$

Reasonable switching time is required at $I_{c(max)}$

$$R_{DS(on)} \approx \frac{2}{I_D}(max)$$

RECTIFIER SELECTION

Output rectifier

$$V_{R(min)} \geq \frac{1.2(V_O + V_F)V_{in(max)}}{V_{in(min)}\ D_{max}} + \left\{\begin{matrix}\text{leakage} \\ \text{inductance} \\ \text{spike}\end{matrix}\right\}$$

$I_{F_{pk}} \geq I_{O(max)}$

$I_{F_1(avg)} = D_{(max)}\ I_{O(max)}$

$I_{F_2}\ (avg) = (1\text{-}D_{min})\ I_{O(max)}$

D_1 Reverse Recovery: 100–200 ns

D_2 Reverse Recovery: 25–100 ns

Clamp diodes D_6-D_7 reverse recovery: 200–400 ns

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A. TRANSISTOR SELECTION

Output Power	Input voltage 220V AC line or 117V line with doubler	Input voltage 117V AC line
75W	UFN833	UFN731
150W	UFN843 UFN742	UFN741
250W	UFN841	UFN351
500W	UFN451	

B. OUTPUT RECTIFIER—DIODE D_1 and D_2 SELECTION

I_O = Output Current	V_O = Output Voltage			
	±5V	±12, ±15V	±28V	±48V
1A, 2A	USD640C 1N5819 (axial)	UES2402 UES1002	UES2404 UES1104 (axial)	UES1105
5A	USD640C	UES2402	UES2404	UES1305
10A	USD740C	UES2402	UES2404	UES2605
20A	USD345C	UES2602 UES1502		
40A	USD545 (DO-5)			
70A	USD545 (DO-5)			

Snubber Diode 1N3613 (2A-800V)

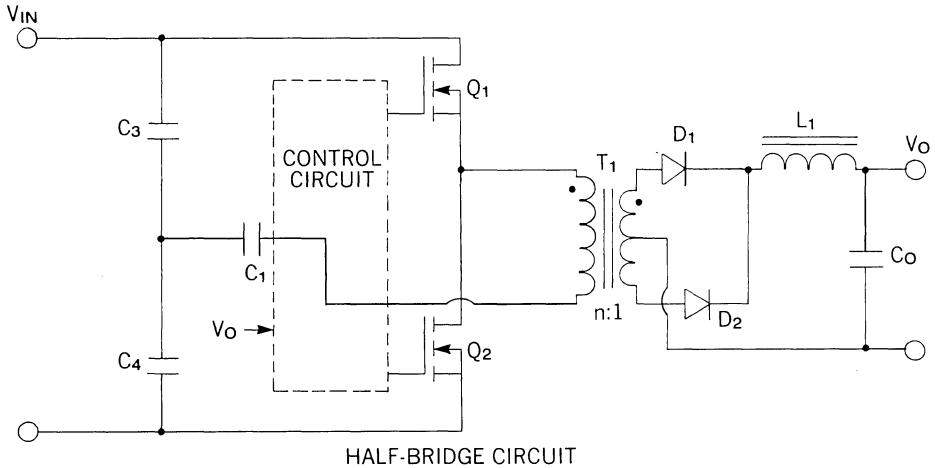
Clamp Diode—D_6, D_7 1N5420
1N4946

C. IC SELECTION

Refer to section "Selection of PWM Control Circuits"

HALF-BRIDGE CIRCUIT

Power Level: Up To 500 Watts



HALF-BRIDGE CIRCUIT

IT'S USED FOR:

- Providing high output power
- Optimizing transformer utilization by operating in 1st and 3rd quadrant
- To provide efficient design

ADVANTAGES

- Flux symmetry problems are corrected with capacitor C1
- Leakage inductance and magnetizing energy are pumped into input and output filter caps thus improving efficiency
- Transformer utilization is better than forward converter

DISADVANTAGES

- It requires two 60cps filter caps
- Transistor's storage time should have tight tolerances to avoid gross imbalance in operating flux level
- Power circuit has 2 pole small signal characteristics

TRANSISTOR SELECTION

BV_{CEO} or $BV_{DSS} \geq 1.1\ V_{in(max)}$

$$I_{c(max)} \text{ or } I_{D(max)} \geq \frac{2\ P_O}{\eta\ V_{in(min)}}$$

$$R_{DS(on)} \approx \frac{2}{I_{D(max)}}\ \Omega$$

RECTIFIER SELECTION

$$V_R \geq 2.2\frac{[V_O + V_F]\ V_{in(max)}}{V_{in(min)}} + \left\{\begin{matrix}\text{Voltage}\\ \text{spike due}\\ \text{to leakage}\\ \text{inductance}\end{matrix}\right\}$$

$I_{F_{pk}} \geq I_{o(max)}$; $I_{F(avg)} = 0.5\ I_{o(max)}$

D_1 and D_2 should be fast (20-100ns)

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A. TRANSISTOR SELECTION

Output Power	Input voltage 220V AC line or 117V line with doubler	Input voltage 117V AC line
50W	UFN821	UFN733
100W	UFN831	UFN743
150W	UFN843	UFN741
250W	UFN841	UFN353
500W	UFN451	UFN351

B. RECTIFIER SELECTION

I_O = Output Current	V_O = Output Voltage			
	±5V	±12, ±15V	±28V	±48V
1A, 2A	USD640C 1N5819 (axial)	UES2402 UES1002	UES2404 UES1104 (axial)	UES1105
5A	USD640C	UES2402	UES2404	UES1305
10A	USD740C	UES2402	UES2402	UES2605
20A	USD345C	UES2602 UES1502		
40A	USD545 (DO-5)			
70A	USD545 (DO-5)			
100A	2xUSD545			
250A	3xUES801			

Snubber Diode 2N3613

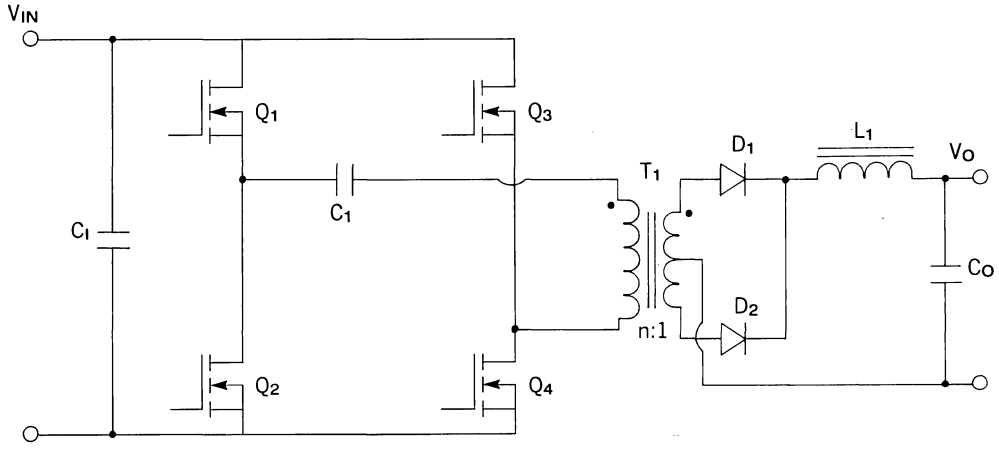
Clamp Diode—D_3, D_4 1N4946, 1N5420

C. IC SELECTION

Refer to section "Selection of PWM Control Circuits"

FULL BRIDGE—SWITCHING REGULATOR

Power Level: 500–2000 Watts



FULL-BRIDGE SWITCHING REGULATOR

IT'S USED FOR:

- Providing over 500 watts of output power. Sometimes transformers are paralleled to provide higher power output.

ADVANTAGES

- Provides same advantages as listed for half-bridge regulator
- Only one 60 cps filter cap is required except in doubler configurations
- Provides 2 times the output power of the half-bridge circuit with the same type switching transistor

DISADVANTAGES

- 4 switching transistors and clamp diodes are required
- Power circuit has 2 pole small signal characteristics

TRANSISTOR SELECTION

BV_{CEO} or $BV_{DSS} \geq 1.1\ V_{in(max)}$

$$I_{c(max)} \text{ or } I_{D(max)} \geq \frac{P_o}{\eta\ V_{in(min)}}$$

$$R_{DS(on)} \approx \frac{2}{I_D}\ \Omega$$

RECTIFIER SELECTION

$$V_{R(min)} \geq 2.2\frac{[V_o + V_F]V_{in(max)}}{V_{in(min)}} + \left\{\begin{array}{l}\text{Voltage}\\ \text{spike due}\\ \text{to leakage}\\ \text{inductance}\end{array}\right\}$$

$I_{F(max)} \geq I_{o(max)}$

$I_{F_{1,2}}(avg) = 0.5\ I_o$

D_1 and D_2 should be fast (20-100ns)

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A. TRANSISTOR SELECTION

Output Power	Input voltage 220V AC line or 117 V line with doubler	Input voltage 117V AC line
200W	UFN831	UFN743
300W	UFN843	UFN741
500W	UFN841	UFN353
1000W	UFN451	UFN351
2000W	UFN451(x2)	

B. RECTIFIER SELECTION

I_O = Output Current	V_O = Output Voltage			
	±5V	±12, ±15V	±28V	±48V
1A, 2A	USD640C 1N5819 (axial)	UES2402 UES1002	UES2404 UES1104 (axial)	UES1105
5A	USD640C	UES2402	UES2404	UES1305
10A	USD740C	UES2402	UES2404	UES2605
20A	USD345C	UES2602 UES1502		
40A	USD545 (DO-5)			
70A	USD545 (DO-5)			
100A	2xUSD545(DO-5)			
250A	4xUSD545			

Snubber Diode 1N3613, 1N3614

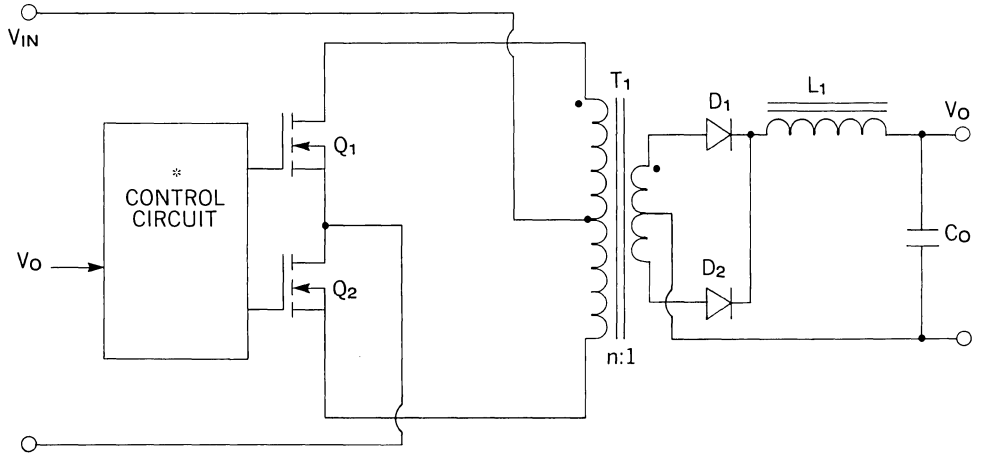
Clamp Diode 1N4946, 1N5420

C. IC SELECTION

Refer to section "Selection of PWM Control Circuits"

CENTER TAPPED PUSH-PULL SWITCHING REGULATOR

Power Level: Up To 300 Watts



PUSH-PULL REGULATOR

IT'S USED FOR:

- Small size and weight

*New control chip UC1846 solves flux symmetry problems associated with push-pull switching regulator.

ADVANTAGES

- Smaller size, weight and cost
- Efficient design
- Easier base drive (both referenced to ground)

DISADVANTAGES

- Inherent flux symmetry problems can be corrected with current-mode PWM control circuit
- Transformer must be slightly over-designed
- Transistor rating twice the input supply voltage
- Power circuit has 2 pole small signal characteristics
- Power circuit has 1 pole small signal characteristics with current-mode control

TRANSISTOR SELECTION

$$BV_{CEO(min)} \geq 1.1\ V_{in(max)}$$

$$BV_{CER(min)} \text{ or } BV_{DSS} \geq 2V_{in(max)} + \left\{\begin{matrix}\text{leakage} \\ \text{inductance} \\ \text{spike}\end{matrix}\right\}$$

$$I_{c(max)} \text{ or } I_{D(max)} \geq \frac{P_o}{\eta\ V_{in(min)}}$$

$$R_{DS(on)} \approx \frac{0.75}{I_{D(max)}}$$

RECTIFIER SELECTION

$$V_R \geq 2.2\frac{[V_o + V_F]V_{in(max)}}{V_{in(min)}} + \left\{\text{Voltage spike}\right\}$$

$$I_{F_{pk}} \geq I_{o(max)}$$

$$I_{F\,1,2\,(avg)} = 0.5\ I_{o(max)}$$

D_1 and D_2 should be fast reverse recovery rectifiers.

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A. TRANSISTOR SELECTION

Output Power	12V DC Input	28V DC Input	117 VAC
20W	PIC610 UFN531	PIC612 UFN522	UFN821
50W	PIC635 UFN541	PIC637 UFN530	UFN821
100W		UFN542	UFN831
150W			UFN841
300W	UFN151	UFN251	UFN450

B. RECTIFIER SELECTION

I_O = Output Current	V_O = Output Voltage			
	±5V	±12, ±15V	±28V	±48V
1A-2A	USD640C 1N5819 (axial)	UES2402 UES1002	UES2404 UES1104 (axial)	UES1105
5A	USD640C	UES2402	UES2404	UES1305
10A	USD740C	UES2402	UES2404	UES2605
20A	USD345C	UES2602 UES1502		
40A	USD545 (DO-5)			

Snubber Diode 1N3613

Clamp Diode 1N3613

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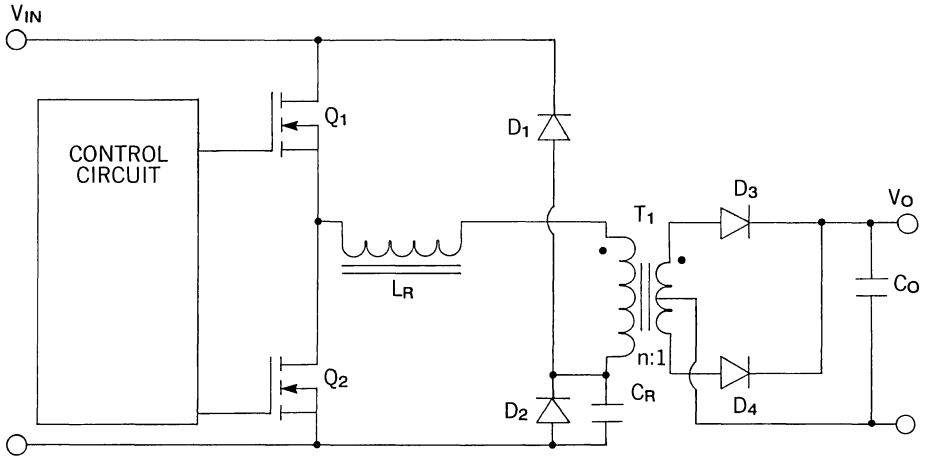
SERIES RESONANT SINE WAVE SWITCHING REGULATOR

Power Level: Less Than 150 Watts



SERIES RESONANT REGULATOR

IT'S USED FOR:

- Reduced size, weight and sometimes cost
- Low RFI and EMI
- Increased efficiency (85-90%)
- Higher frequency

ADVANTAGES

- Higher efficiency
- Smaller weight and volume
- Low switching losses allows high frequency operation. Thus reduced size of magnetics and heat sink.
- Reduced EMI—no trr related current spike, low di/dt current waveforms
- Increased reliability
  —L_R acts as current limiter
  —zero current switching, no heat generated
- Problem with leakage inductance is minimized.

DISADVANTAGES

- Requires additional resonant network, L_R and C_R
- Current rating of the switch is 3 to 4 times higher than conventional switching regulator
- Output filter cap carries high ripple current

TRANSISTOR SELECTION

$BV_{DSS} \geq 1.1\ V_{in(max)}$

$$I_{D(max)} \geq 3.5\ \frac{2\ P_O}{V_{in(min)}}$$

$I_{D(rms)} = 0.5\ I_{D(max)}$

$$R_{DS(on)} \approx \frac{2V}{I_{D(rms)}}$$

RECTIFIER SELECTION

For D_3, D_4:

$V_R \geq 2.2\ V_O$ + Voltage Spike

$I_{F_{pk}} \geq \sqrt{2}\ I_{o(max)}$

$I_{F(avg)} = 0.35\ I_{F_{pk}}$

For D_1 and D_2; $V_R = 1.2\ V_{in(max)}$

For D_3 and D_4; slow reverse recovery diodes relative to frequency of operation can be used.

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A. TRANSISTOR SELECTION

Output Power	Input voltage 220V AC line or 117V line with doubler	Input voltage 117V AC line
50W	UFN831	UFN743
100W	UFN841	UFN741
150W	UFN451	UFN351

B. OUTPUT RECTIFIER—DIODE D_3 or D_4 SELECTION

I_O = Output Current	V_O = Output Voltage			
	±5V	±12V	±15V, ±28V	±48V
1A, 2A	USD635C USD1130 (axial)	SES5401C SES5001 (axial)	SES5402C SES5002 (axial)	SES5403C SES5003 (axial)
3A	USD635C	SES5401C SES5301 (axial)	SES5402C SES5302 (axial)	SES5403C SES5303 (axial)
5A	USD635C	SES5401C	SES5402C	SES5403C
10A	USD635C	SES5401C	SES5402C	SES5403C
20A	USD835	SES5501	SES5502	
40A	USD535	UES701	UES702	

Snubber Diode —1N4944, 1N4946

Clamp Diodes D_1, D_2 —1N4944, 1N4946

C. IC SELECTION

Refer to section "Selection of PWM Control Circuits"

SELECTION OF PWM CONTROL CIRCUITS

The important features of the PWM control circuit and their recommended applications are listed below. It should be used as a guideline for selecting the PWM control circuit.

Conventional PWM Circuits	Features	Recommended Applications
UC3524A	• pin to pin compatible with UC3524 • uncommitted push-pull with 200mA and 60V capability • under voltage lockout (8V) • ±1% reference • fast pulse by pulse current limit with wide common mode input range • double pulse suppression circuit • low stand-by current	• step-down regulator • flyback-type • single ended forward • two transistor forward
UC3525A/3527A	• push-pull totem pole output with 500mA peak current capability • oscillator range up to 500KHz • ±1% reference • under voltage lock out (8V)	• power MOSFET single ended flyback and forward • two transistor forward • half bridge • push-pull/full bridge
UC3526	• push-pull totem pole output with 200mA peak current capability • oscillator range up to 400KHz • ±1% reference • under voltage lock out (8V) • fast pulse by pulse current limit with wide common-mode input voltage • double pulse suppression circuit	• power MOSFET flyback regulator • power MOSFET single ended forward • two transistor forward • half bridge • push-pull/full bridge • current-fed
UC493A series	• uncommitted push-pull output with a 200mA capability • under voltage lock out (6.5V) • ±1% reference • two independent error amplifiers with a wide common-mode input voltage range • double pulse protection • 80mV internal threshold included in one of the error amplifiers forUC493A and UC495B • UC495A and B includes 39V zener for over 40V input supply	• single ended forward • two transistor forward • flyback-type

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SELECTION OF PWM CONTROL CIRCUITS (Cont'd)

Feed-Forward PWM control circuit	Features	Recommended Applications
UC3840	• single ended output with a 400mA output current capability • pulse by pulse and over current limiting amplifiers with a 3.0V common-mode input voltage range • ±1% reference • low stand-by current with a programmable start voltage • programmable under and over voltage protection circuit • intended for primary side control • UC3840 + UC3706 allows push-pull operation	• single ended forward • two transistor forward • flyback-type • current fed

Current-mode PWM Control Circuits	Features	Recommended Applications
UC3842	• low cost 8 pin IC circuit • single totem pole output circuit with a 200mA peak current capability • less than 1mA start-up current up to 16 volt • pre-set 16V start-up voltage and 10V under voltage lock-out • + 1 volt internally set threshold for pulse by pulse current limiting	• single ended forward • two transistor forward • flyback-type • current-fed
UC3846/47	• push-pull totem pole output with 500mA peak current capability • ±1% reference • under voltage lock out (8V) • double pulse suppression • current sense amplifier with wide common-mode input voltages	• step-down regulators • push-pull/full bridge (*not* half bridge circuit)

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POWER SUPPLY SUPPORT FUNCTIONS

Type	Description	Key Features
UC3543 UC3544	Power Supply Supervisory Circuit, Monitors and Controls Power Supply Output	• Over/Under-Voltage, and Current Sensing Circuits • Programmable Time Delays • SCR "Crowbar" Drive of 300mA • Optional Over-Voltage Latch • Internal 1% Accurate Reference • Remote Activation Capability • Uncommitted Comparator • Inputs for Low Voltage Sensing (UC3544 series only)
UC3706	Dual High Current MOSFET Compatible Output Driver	• Dual 1.5A Totem Pole Outputs • Parallel or Push-Pull Operations • Single-Ended to Push-Pull Conversion • Internal Overlap Protection • Analog, Latched Shutdown • High-Speed, Power MOSFET Compatible • Thermal Shutdown Protection • 5 to 40V Operation • Low Quiescent Current
UC3901	Isolated Feedback Generator Stable and Reliable Alternative to an Optical Coupler	• An Amplitude-Modulation System for Transformer Coupling an Isolated Feedback Error Signal • Internal 1% Reference and Error Amplifier • Loop Status Monitor • Low-Cost Alternative to Optical Couplers • Internal Carrier Oscillator Usable to 5MHz • Modulator Synchronizable to an External Clock
UC3903	Quad Supply and Line Monitor Precision System	• Monitor Four Power Supply Output Voltage Levels • Both Over- and Under-Voltage Indicators • Internal Inverter for Negative Level Sense • Adjustable Fault Window • Additional Input for Early Line Fault Sense • On Chip, High-Current General Purpose OP-AMP

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APPENDIX I

QUESTIONS MOST OFTEN ASKED

1. *Define Topology.*
   The circuit configuration by which power is transferred from the input power source to the output. Topology refers to the type of power transfer circuit.

2. *What is an error amplifier and error voltage?*
   The voltage difference between the fixed reference and the regulated output is amplified by the error amplifier of the control circuit. The output of this amplifier is called the error voltage. The error voltage is used to change the on-time of the power output switch.

3. *What is the PWM technique?*
   PWM is the abbreviation for Pulse Width Modulation. This technique translates the voltage level of an analog signal into the appropriate pulse width by comparison with a voltage ramp circuit. At the beginning of the cycle, the ramp voltage starts at zero and the output of the comparator is set high. Ramp voltage increases linearly through the entire cycle. When the ramp voltage is equal to the analog signal, the comparator output is set low (the analog signal represents the output of an error amplifier). The peak amplitude of the ramp voltage is fixed in a conventional PWM technique.

4. *Describe the input voltage feed-forward PWM technique & its advantages.*
   It is a variation of the pulse width modulation technique. The output pulse-width of the control circuit is not only controlled by the error voltage but also the input supply voltage. The level of the error voltage remains fairly constant for several cycles. (Note that the ramp voltage starts from zero at the beginning of the cycle, and continues to increase linearly for the entire cycle.) The ramp slope is proportional to the input line voltage. Thus any change in input line voltage is immediately translated into a change of pulse width in the same cycle.
   The main advantages of the PWM technique are:
   - Low input audio susceptibility
   - Smaller transformer
   - Less loop gain required

5. *What are the basic differences between current-fed converter (topology) and current-mode control (control method) converters, and what are the main advantages of the current-mode PWM technique?*
   In a current-fed converter the power source used to power the post converter has constant current characteristics. Usually a filter inductor is used in the input line to achieve constant current source characteristics. With a current-mode control, the primary current is utilized to generate the ramp voltage, instead of the fixed ramp voltage which is used for the conventional PWM technique. This ramp voltage is needed to determine the output pulse width of the control chip. The major advantages of current-mode PWM techniques are:
   - Stable circuit
   - Fast transient response
   - Pulse by pulse current limiting

6. *What is the main function of the compensation network?*
It provides stabilization necessary to avoid oscillation, with the higher loop gain necessary for good line and load regulation.

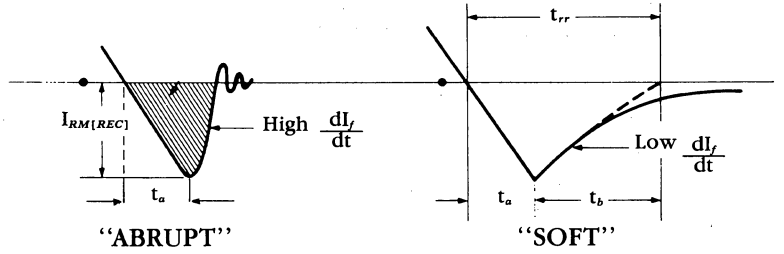
7. *What is a right half plane (RHP) zero?*
The RHP zero is a particular characteristic of the closed loop system. A right half plane zero in a control loop occurs only in a continous-mode flyback topology rather than the control circuit. The continuous-mode flyback is an example. In a switching regulator, the on-time of the power switch increases when the output voltage drops below the desired level. This results in increased output power until output voltage reaches the desired level. However, in a continuous-mode flyback, this increase in on-time results in reduction of output power temporarily. (Note that power is delivered to output only during off-time.) This provides additional 90° phase lag in the control loop. This can result in unstable circuit operation at high frequency.

8. *What is pulse by pulse current limiting?*
The pulse by pulse current limit circuit senses the switching current and if it exceeds the pre-set maximum current level, it terminates conduction of the output voltage control loop and switching transistor. The transistor turns on again at the beginning of the next cycle and if the switching current is over the current limit, the transistor immediately turns off.

9. *What is ripple?*
The AC voltage across the output filter capacitor is referred to as the output ripple voltage. The peak to peak variation in current in an output filter inductor is also sometimes known as ripple current.

10. *Why is minimum reverse recovery time desirable?*
To reduce current pulses which will result in;
- Reduced radio frequency interference (RFI)
- Reduced turn-on switching losses in transistor
- Reduced turn-off losses in the rectifier

11. *What is the difference between a soft and an abrupt reverse recovery characteristic?*
The rate at which reverse recovery current (di/dt) goes to zero determines the characteristic. Turn-off current waveforms for soft and abrupt reverse recoveries are shown below:



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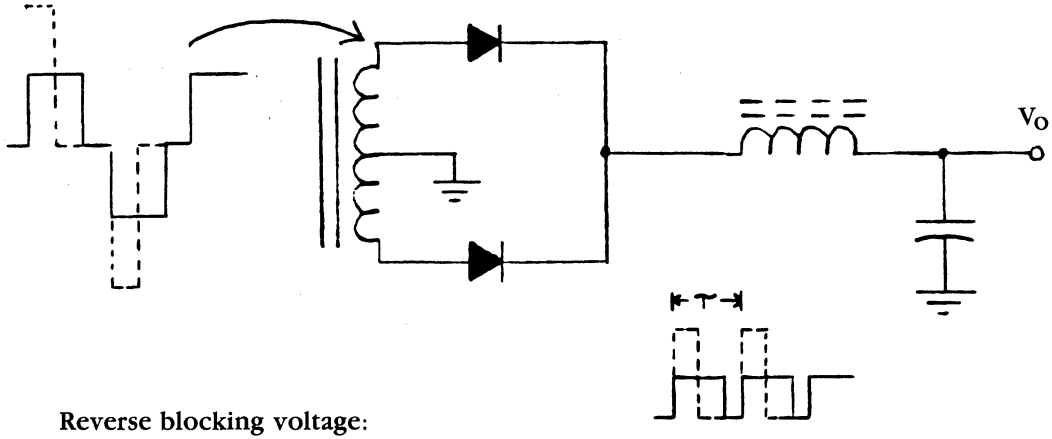
12. *List advantages of a soft reverse recovery characteristic over an abrupt one.*

Soft reverse recovery advantages are:

- Lower RFI
- Less voltage ringing

13. *Determine the reverse blocking voltage requirements for the output rectifiers in a +5V off-line PWM switching regulator.*

The voltage waveforms to determine voltage requirements of the rectifier at low line are shown below:



Reverse blocking voltage:

$\rightarrow\!|\ \ |\!\leftarrow$ t_d = dead-band period

$$= 2R\left[\frac{V_O}{(T - t_d)/T} + V_F\right] + \text{leakage inductance spike} \qquad \frac{(T - t_d)}{T} = 0.9 \text{ to } 0.95$$

$$= 4\left[\frac{5}{0.9} + 0.8\right] + 7 = 32 \text{ volts}$$

Note that the ratio (R) between the maximum input DC voltage across 60cps input filter capacitor (just before capacitor recharges—at minimum input voltage with full load) to the maximum DC voltage (at high line with no load) is approximately two.

14. *What are the functional differences between clamp, catch and rectifier diodes?*

Clamp diode—Limits the maximum voltage excursions across device.

Catch diode—Provides current path for the inductor load current or transformer magnetizing current.

Rectifier diode—Directly converts AC voltage into pulsating DC voltage.

15. *What is the main function of a crow-bar circuit?*

The output voltage of the power supply provides power for many logic circuits. The voltage across these logic circuits must be limited to a safe value to prevent damage to these devices. The techniques used to limit excessive voltage are:

A. Zener clamp—

It is used to limit voltage due to short duration transient pulses. Voltage is clamped with a power zener.

B. Crow-bar circuit—
When output voltage exceeds pre-determined value, the silicon controlled rectifier (SCR) across the output turns on, and clamps the voltage by the forward drop of the SCR. Crow-bar needs to be reset to resume normal operation.

16. *What is a Synchronous rectifier?*
A power MOSFET or bipolar transistor can be used in place of a rectifier to improve the efficiency. Operating these devices in on-state, the developed voltage drop is considerably less than the low forward drop of a schottky rectifier. The device operates from the AC input voltage and conducts when input voltage is slightly greater than output voltage.

17. *What is the difference between a buck regulator and a step-down regulator?*
They are the same circuit. This circuit converts a high input voltage to a lower output voltage.

18. *What are the advantages and disadvantages of the single transistor forward converter compared to a buck regulator?*
Advantages:
Provides DC isolation between input supply voltage and the output voltage.
Provides multiple outputs.
Optimizes the switching transistor and rectifier utilization when there is a large difference between input and output voltage.
Disadvantages:
Needs transformer in addition to filter inductor.
Less efficient, it needs snubber network, switching losses are higher.
More expensive.

19. *Which is the lowest cost topology for multiple output power supply?*
Discontinuous-mode flyback.

20. *List the differences between a continuous-mode and a discontinuous-mode flyback.*

DISCONTINUOUS-MODE
- current in transformer drops to zero every cycle
- smaller transformer
- output filter caps 2 times larger
- single-pole

CONTINUOUS MODE
- it has RHP zero and 2 poles
- needs fast output rectifier
- approx. 2 times lower peak currents in transistor and rectifier

21. *What is the main difference between an inverter and a converter?*
Inverter has DC input and AC output;
converter has AC or DC input and DC output.

22. *What is proportional base drive?*
A base drive circuit where base current is always a certain fraction of the collector current. The ratio between these two currents is determined by the turns ratio of the current transformer used in the base drive circuit.

23. *Define storage-time and why minimum storage-time is desirable.*
The time elapsed between the on-set of the turn-off signal to the instant when collector voltage starts to increase. It is important to have low storage-time to:
- control minimum pulse width
- reduce saturation losses during storage time
- prevent core saturation due to transformer asymmetry

24. *Give two main functions for the snubber network.*
- to reduce peak power dissipation during switching
- to reduce radiated noise

25. *What are the advantages of a power MOSFET over a bipolar device in a switching regulator application?*
A. Higher Efficiency
B. Faster Switching Characteristics
C. Lower System Cost
   - drive circuit simpler
   - no snubber circuit required
   - smaller magnetics & filter capacitor
   - in a high current application, devices can be paralleled easily
D. Improved Performance
   - no cross conduction current in push-pull circuits (no storage time)
E. Allows the use of new topology—series resonant converter
F. Improved Reliability
   - no forward or clamped reverse bias second breakdown problems
   - uniform junction temperature
   - integral diode can reduce component count

26. *Why is isolation necessary?*
When an output is derived from a 117V or 220V AC line input voltage, the output should have 3750V isolation (VDE requirements) from the 117V or 220V AC line for safety reasons.

27. *What is the function of a Baker Clamp?*
The collector current of the power transistor in a switching regulator is proportional to variable output load current. Normally, with bipolar transistors the fixed base drive current is optimized for a maximum output load current. This can result in unacceptably large storage time at light load, because the transistor will be driven into deep saturation. The baker clamp prevents deep transistor saturation by providing a path for excessive base drive current. Many applications, such as flyback and forward converters, are utilizing this technique. The baker clamp diode must have a fast reverse recovery time.

28. *Define power factor and why it is important to keep close to one.*
In an off-line switching regulator, the pulsating DC input voltage is derived through an input bridge rectifier. This pulsating DC voltage is utilized to charge the (60cps) input filter capacitor. The capacitor charges during the peak portion of the input pulsating DC voltage. The input AC voltage is isolated from the capacitor during the rest of the cycle.

When the capacitor charges from the input line voltage, it draws large peak currents, rather than continuous currents during the entire cycle. This large current drawn from the line, during a short period of the cycle, causes additional I^2R losses in the lines. The power factor can be defined by equation:

$$\text{P.F.} = \frac{\text{Output power}}{\text{Input AC voltage x RMS input current}}$$

29. *Why does the input supply line see a negative input impedance when the output load is a switching regulator?*

With a fixed output load current, the peak current drawn from the input supply voltage remains the same even if input voltage is increased; however, the duty cycle is reduced to maintain output voltage regulation. Therefore average current drawn from the supply voltage is reduced while the input voltage increased to maintain constant power output. This negative change in current results in a line which sees a negative input impedance. Any inductance in the input line will cause oscillation if proper damping is not provided.

30. *Is efficiency affected by the absolute value of the output voltage?*

$$\text{Efficiency} = \frac{\text{Output Power}}{\text{Input Power}} = \frac{\text{Output Power}}{\text{Output Power + Losses}}$$

Most of the power losses in a switching regulated power supply are due to the forward losses of the output rectifiers. For example, in a 5V supply, 20% of the output power will be lost in the rectifiers. This will limit the maximum efficiency to less than 80%. However, in a +12V supply only 8% of the output power will be lost in the rectifiers. This will result in maximum efficiency of approximately 92%.

APPENDIX II

ENGINEERING NOTE-BOOK "DESIGN EQUATIONS"

This section lists some of the important switching regulator design equations.

I. Input filter capacitor for 60 Hz rectification;

$$C_{in} = \frac{P_O}{\eta f_L (V_{PK}^2 - V_{min}^2)} \qquad \text{(EQ. 1)}$$

Where: V_{PK}—peak voltage at min. input line
V_{min}:V_{PK}—ripple across the capacitor
f_L—line frequency
P_O—output power
η—efficiency

with a line drop-out specification:

$$C_{in} \approx \frac{P_O\, N}{f_L\, \eta (V_{PK}^2 - V_{min}^2)} \qquad \text{(EQ.2)}$$

Where: N—number of drop-out cycles

II. The output filter capacitor:

$$c_O = \frac{\Delta I_L}{8\, f_S \Delta V_O} \qquad \text{(EQ. 3)}$$

Where: ΔV_O = output ripple voltage

The selected capacitor must have ESR$\leqslant \Delta V_O / \Delta I_L$

III. Magnetic design

Energy stored in the core material

$$Wc = \tfrac{1}{2} \frac{B\, Ae\, Hle}{.4\pi} 10^{-8} \qquad \text{(EQ.4)}$$

Where: B—magnetic flux density in gauss
H—magnetic field intensity in oersted
Ae—effective magnetic cross section area in cm. sq.
le—mean magnetic path length in cm.

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The required circuit energy:

$$W_R = \tfrac{1}{2} L i_p^2 \qquad \text{(EQ. 5)}$$

Where: L— circuit inductance
i_p— peak current in inductor

Magnetic potential, from Ampere's law:

$$\frac{Hle}{.4\pi} = N_p i_p \qquad \text{(EQ. 6)}$$

lg = gap in the magnetic path in cm.
le = lg
B = H for gapped inductor

The inductor value:

$$L = A_L N_p^2 \times 10^{-9} \text{ henries} \qquad \text{(EQ. 7)}$$

A_L — inductance index
L — henries

From Faraday's law, the minimum number of primary turns for the push-pull converter:

$$N_{P_{min}} \geqslant \frac{V_{in(max)}\ 10^8}{4\ f_s\ B_{max}\ Ae} \qquad \text{(EQ. 8)}$$

Where: $V_{in(max)}$ = max. input DC voltage
f_s = switching frequency

For forward converter

$$N_{P_{min}} \geqslant \frac{V_{in(max)}\ 10^8}{2\ f_s\ B_{max}\ Ae} \qquad \text{(EQ. 9)}$$

The output filter inductor in PWM switching regulator:

$$L \approx \frac{V_O + V_F}{f_s\ \Delta I_L} \qquad \text{(EQ. 10)}$$

Where: V_O = output voltage
V_F = forward voltage drop in the rectifier
ΔI_L = peak to peak inductor current
$\approx 2\ I_{O(max)}$ or $I_{O(min)}$

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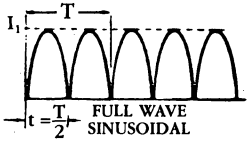
The temperature rise of the core with natural convection cooling:

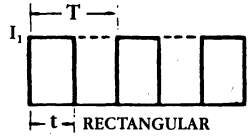
$$\Delta t = \frac{850 P_L}{A_S} \qquad \text{(EQ. 11)}$$

Where: P_L = power losses (copper and core losses)
A_S = core surface area in cm^2

IV. Equations for determining RMS current

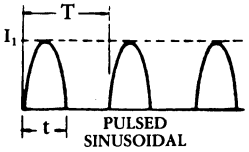


$$I_{RMS} = \frac{I_1}{\sqrt{2}}$$



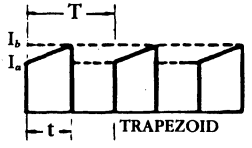
$$I_{RMS} = I_1\sqrt{D}$$

$$D = \frac{t}{T}$$



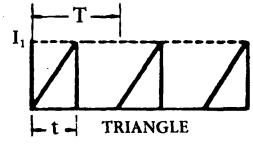
$$I_{RMS} = I_1\sqrt{\frac{D}{2}}$$

$$D = \frac{t}{T}$$



$$I_{RMS} = D\left[\frac{I_a^2 + I_a I_b + I_b^2}{3}\right]^{1/2}$$

$$D = \frac{t}{T}$$



$$I_{RMS} = I_1\sqrt{\frac{D}{3}}$$

$$D = \frac{t}{T}$$

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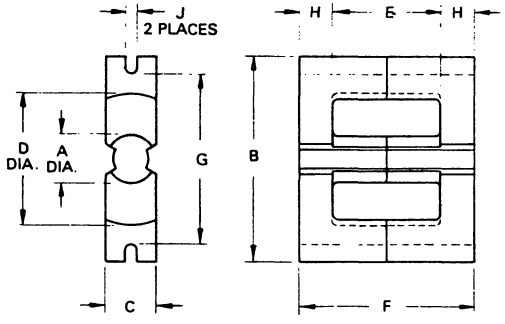
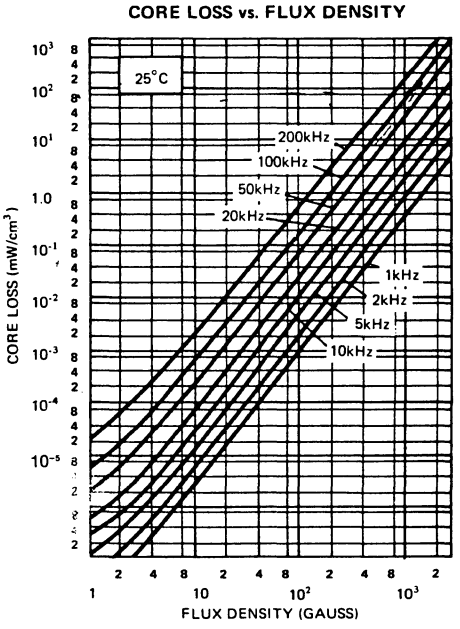
V. EC CORE DATA

EC core data is from Ferroxcube databook. There are many suppliers of this core series. Pregapped cores are available. All dimensions are in centimeters:

CORE	EC35	EC41	EC52	EC70
B	3.45	4.06	5.22	7.0
D	3.46	3.9	4.84	6.9
C	.95	1.16	1.34	1.64
A	.95	1.16	1.34	1.64
A_e	.843	1.25	1.83	2.83
l_e	7.74	8.8	10.3	14.1
V_e Core Volume	6.53	11.0	18.7	39.8
b_W (E)	2.45	2.78	3.18	5.55
h_W (H)	.66	.77	.98	1.22
A_W Bobbin Cross Section Area	1.03	1.35	2.13	4.77
A_S	43.5	59	91	170
$A_S A_W$	1.39	2.69	5.71	18.1





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WINDING DATA

WIRE TABLE—Copper Wire—Heavy Insulation:

AWG	DIAMETER Copper cm	AREA Copper cm^2	DIAMETER Insulated cm	AREA Ins. cm^2	OHMS/CM 20 C	OHMS/CM 100 C	AMPS for $450A/cm^2$
16	.129	.013088	.139	.015207	.000132	.000176	5.890
17	.115	.010379	.124	.012164	.000166	.000222	4.671
18	.102	.008231	.111	.009735	.000209	.000280	3.704
19	.091	.006527	.100	.007794	.000264	.000353	2.937
20	.081	.005176	.089	.006244	.000333	.000445	2.329
21	.072	.004105	.080	.005004	.000420	.000561	1.847
22	.064	.003255	.071	.004013	.000530	.000708	1.465
23	.057	.002582	.064	.003221	.000668	.000892	1.162
24	.051	.002047	.057	.002586	.000842	.001125	.921
25	.045	.001624	.051	.002078	.001062	.001419	.731
26	.040	.001287	.046	.001671	.001339	.001789	.579
27	.036	.001021	.041	.001344	.001689	.002256	.459
28	.032	.000810	.037	.001083	.002129	.002845	.364
29	.029	.000642	.033	.000872	.002685	.003587	.289
30	.025	.000509	.030	.000704	.003386	.004523	.229
31	.023	.000404	.027	.000568	.004269	.005704	.182
32	.020	.000320	.024	.000459	.005384	.007192	.144
33	.018	.000254	.022	.000371	.006789	.009070	.114

TRANSIENT VOLTAGE SUPPRESSOR GUIDE

Introduction

Unitrode has been a leading supplier of discrete components for more than 25 years. Our Transient Voltage Suppressors (TVS) are used by some of the largest corporations in the world — Lockheed, IBM, Hughes and Univac, for example — in applications where high reliability and performance are important. These have included military programs such as Trident, INTELSAT VI, and Peacekeeper.

In addition to its traditional suppressor products, Unitrode now also offers a variety of bipolar and unipolar devices in custom packages, ranging from miniature plastic smaller than 1×10^{-3} cubic inches to 20-pin DIP zener arrays.

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INTRODUCTION TO TRANSIENTS

Unsuppressed transients can cause circuit malfunctions or even circuit failure. Voltage transients from sources external to a circuit occur randomly, and with a frequency which is virtually impossible to predict. Transients which are created by the circuit itself can be very specifically defined. Figure 1 illustrates the range of predictability of both internally and externally generated transients.

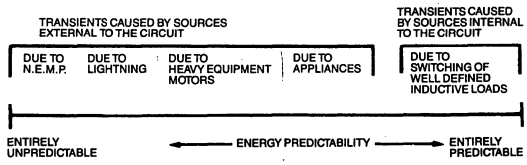


FIGURE 1

Both types must be considered by the designer in order to achieve optimum performance and reliability.

TRANSIENT MODELS

The models in Figure 2 represent transient sources. As the diagram illustrates, externally generated transients may appear to be like a voltage or a current source. In circuits which switch inductive loads, internally generated transients appear to be from a current source.

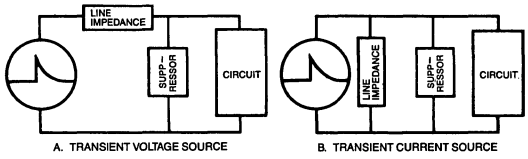


FIGURE 2 TRANSIENT SOURCE MODELS

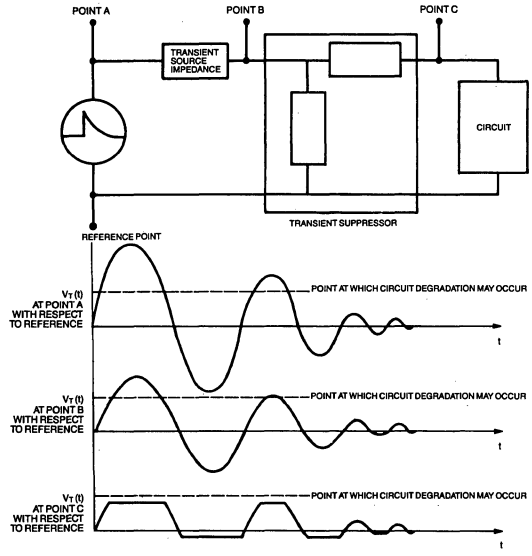
When considering how to protect against transients generated from external sources, the value of impedance in series with the transient is relevant. If it is known, an approximation of the current — and therefore of the surge power handling capability of the required suppressor — can be determined. However, this impedance value is often difficult to determine accurately.

EXAMPLES OF EXTERNALLY GENERATED TRANSIENTS

An example of an externally generated transient would be lightning striking a power transmission line. The effective impedance of a typical U.S. residential branch network could be as much as 300 ohms. The peak currents associated with the high frequency components of the transient could be limited by this effective impedance.

The lower frequency components could, of course, see a much lower impedance which would be the impedance of the network associated with the 60 hertz transmitted power frequency. The value of impedance could be significantly lower if the lightning were to strike at a point close to the susceptible equipment.

In other words, the effective impedance in such a case is hard to estimate, and thus the surge current would be difficult to resolve. Figure 3 illustrates response to such a random transient.



Another type of external transient is generated when parallel inductive loads are switched on and off on the same branch of a power distribution system. These transients would appear to come from a current source.

Still another transient source of concern to many designers today is the Nuclear Electromagnetic Pulse (N.E.M.P.).

In the event of a nuclear explosion, voltage fields of very high intensity are generated. These transients are of great concern because of their far reaching effects.

For example, a nuclear explosion occuring at a height of 300 miles above the center of the United States would generate an intense electromagnetic field that would affect electrical circuits from coast to coast.

While the explosive power of such a blast is classified, it is of sufficient military concern to have started a major effort to develop E.M.P. hardened systems.

While shielding may help to provide proper protection from such transients, the effects from input and output lines would remain of concern. Ultimate protection, therefore, would have to involve effective suppression of voltage transients on these lines.

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EXAMPLES OF INTERNALLY GENERATED TRANSIENTS

Internally generated transients, unlike external, can be very specifically defined. When switching inductive loads, energy built-up in the magnetic field of the inductor during the transistor on time must not be transferred to the voltage sensitive load. Such a transfer could have a serious detrimental effect on the performance of the circuit. A solution is to provide a fast acting voltage clamp which would safely limit the peak voltage across the load. An example of a voltage sensitive item would be the reverse biased collector-base junction. The value of voltage, in this case, should never exceed the applicable BV rating of the transistor.

Figure 4 shows the current and voltage waveforms associated with the application of a semiconductor transient voltage suppressor in an inductive switching situation.

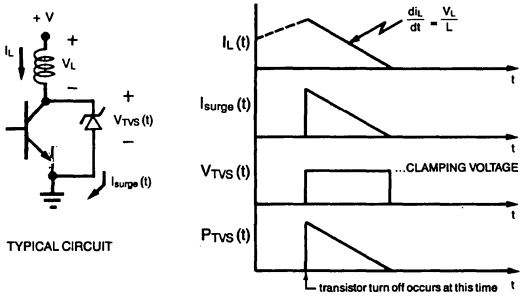

FIGURE 4

CHOOSING AN APPROPRIATE TRANSIENT VOLTAGE SUPPRESSOR

With this brief discussion of transients behind us, it now becomes time to get a clearer understanding of how to choose an appropriate transient voltage suppressor (TVS). The key items of concern are as follows:

1. Stand-off voltage
2. Peak pulse power capability
3. Maximum clamping volt
4. Maximum junction temperature
5. Response time

First, a definition of terms is warranted.

Stand-off Voltage

This is the circuit operating voltage which relates to the suppression device. At the stand-off voltage, the TVS will be essentially non-conducting such that the insertion loss will be minimal. A device should be chosen with a stand-off voltage equal to, or greater than, the maximum normal circuit operating voltage. The stand-off voltage of a device is clearly defined in the manufacturer's electrical specifications table.

Peak Pulse Power

The peak pulse power is equal to the clamping voltage times the peak current. A device must be chosen which has the capability to handle this peak pulse power. The pulse power vs pulse duration graph on manufacturers' datasheets can be used to determine whether a particular device would be operating within its safe operating region. (For examples of these types of curves see the Appendix.)

Maximum Clamping Voltage

This is the maximum voltage that will occur across the TVS for the duration of the transient. A device must be chosen which will clamp below the voltage that may damage any components. For effective use, it is necessary to define the surge current that will equate to the clamping voltage.

Maximum Junction Temperature

The junction temperature is equal to the pulsed thermal impedance times the peak pulse power, plus the junction temperature just prior to the transient pulse. An understanding of the maximum junction temperature is vital with regard to reliability of the TVS itself.

Response Time

When protecting sensitive components, the response time of the protection device is also of importance. Special attention must be paid to insuring that the protection device is inherently fast enough in its response time and that parasitic inductance is kept to a minimum. The intrinsic characteristics of a semiconductor TVS enable it to effectively respond to transients of extremely short duration, or transients of longer duration with very fast rise times. Other forms of protection are much slower in their response. A semiconductor TVS is the fastest device available, responding in pico seconds.

SELECTION CRITERIA

To properly select a device, it is essential to understand the maximum clamping voltage as accurately as possible, since this value impacts on whether proper protection has been achieved. It is also necessary to know this value to determine the peak power and peak junction temperature.

Unitrode TVS's are characterized as having a minimum breakdown voltage at some very low current, usually 1 milliampere. For reverse currents other than this, the TVS voltage will differ due to three factors:

1. TVS *dynamic impedance* varies as a function of bias current and is evident at intermediate currents (less than 1 ampere). Dynamic impedance is closely tied to the physics of the breakdown mechanism.
2. *Surge impedance* dominate the TVS's I-V characteristics at large reverse currents. The surge impedance is essentially the sum of the semiconductor bulk resistance, contact, pin, and lead resistance and varies little with bias current.

3. *Power dissipation* in the TVS, varies directly with reverse current. As a result, an increase in reverse current will create an increase in junction temperature. *Power related heating* gives rise to increased reverse voltage in TVSs because of the positive temperature coefficient of reverse voltage associated with the semiconductor junction.

Model to Determine Clamping Voltage

The expected TVS voltage under bias conditions other than the low current condition described in the data table would therefore be:

$V_{clamp} = V_{TVS}$ at 1mA + ΔV_{TVS} (dynamic) + ΔV_{TVS} (surge) + ΔV_{TVS} (thermal)

Where: ΔV_{TVS} (dynamic) = change in TVS voltage due to dynamic impedance.

ΔV_{TVS} (surge) = change in TVS voltage due to surge impedance.

ΔV_{TVS} (thermal) = change in TVS voltage due to ambient and power induced temperature excursions.

Vclamp = voltage which will occur across the TVS as a result of the surge.

ΔV_{TVS} (dynamic):
A rigorous way to obtain a value for ΔV_{TVS} (dynamic) involves the integration of the impedance-current product over the current range from the low current test point to the surge current. The results of this integration, for Unitrode axial TVSs are:

$\Delta V_{TVS}(\text{dynamic}) = 0.133\,(V_{TVS})^{1.08}\,[I_{surge}^{0.138\sqrt[8]{V_{TVS}}} - I_{test}^{0.138\sqrt[8]{V_{TVS}}}]$ for 150W TVSs

$\Delta V_{TVS}(\text{dynamic}) = 0.029\,(V_{TVS})^{1.28}\,[I_{surge}^{0.101\sqrt[5]{V_{TVS}}} - I_{test}^{0.101\sqrt[5]{V_{TVS}}}]$ for 500W and 600W TVSs

$\Delta V_{TVS}(\text{dynamic}) = 0.031\,(V_{TVS})^{1.23}\,[I_{surge}^{0.105\sqrt[4]{V_{TVS}}} - I_{test}^{0.105\sqrt[4]{V_{TVS}}}]$ for 1500W TVSs

Where: V_{TVS} = low current breakover voltage which is defined in the data table.

I_{surge} = peak surge current.

I_{test} = low level test current; defined in manufacturers data tables.

ΔV_{TVS} (surge):
Figure 5 shows surge impedance as a function of stand-off voltage for Unitrode axial transient voltage suppressors. The voltage increase due to surge impedance is simply

$\Delta V_{TVS}(\text{surge}) = Z_S\,(I_{surge} - I_{test})$

ΔV_{TVS} (thermal):
Power is dissipated at a semiconductor junction as heat and acts to raise the temperature of the junction and, in turn, the semiconductor bulk, the pins, and the leads. To understand how heat transfer occurs it is useful to consider both the thermal resistance and thermal impedance models.

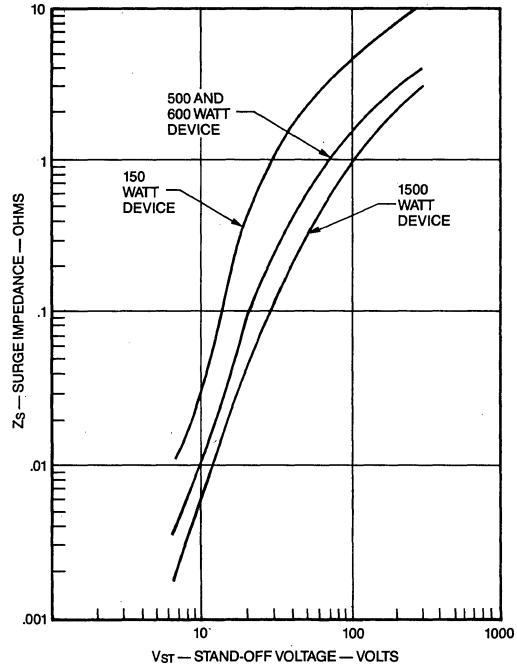

FIGURE 5

Thermal Resistance Model

In a situation where a repetitive transient occurs at a fixed frequency, it is simple to determine the average and estimate the peak junction temperature. To determine the average junction temperature one should derive the average power dissipation by using the following relation:

Pd (average) = (Vclamp x Isurge) tp/t

Where tp = duration of the rectangular equivalent pulse

τ = period of the waveform

The average junction temperature then becomes:

T_j (average) = $T_A + (R_{\theta J-A}) \times$ Pd (average)

where: T_A = ambient temperature

$R_{\theta J-A}$ = thermal resistance, junction to ambient

In order to assure a safe operating junction temperature, the designer must achieve a sufficiently low thermal resistance, junction to ambient.

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$R_{\theta J-A}$ is dependent on both device construction and mounting conditions. It is useful to separate these dependencies by invoking the relation:

$R_{\theta J-A} = R_{\theta J-L} + R_{\theta L-A}$

Where: $R_{\theta J-L}$ = thermal resistance junction to lead and is device construction dependent.

$R_{\theta L-A}$ = thermal resistance lead to ambient and is mounting dependent.

For a simple conservative estimate of the peak junction temperature, the designer needs only add to the average junction temperature the excursion of junction temperature obtained by utilizing the thermal impedance model. Figure 6 offers a qualitative representation of the effects produced by a transient which occurs at a fixed frequency.

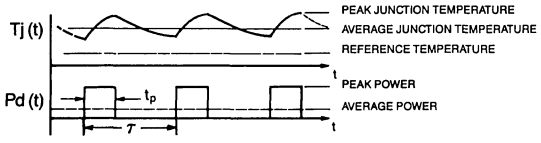

FIGURE 6

Thermal Impedance Model

Under single pulse reverse bias conditions the thermal capacitance of the TVS becomes evident, and its thermal behavior is best characterized by a pulse-width-dependent thermal impedance. For pulse widths less than one half second in duration, heat flow from the lead to a typical mounting is minimal, and the thermal response is nearly independent of mounting conditions. In this situation:

$\Delta Tj = P_D \times Z_\theta$

Where: P_D = pulsed power

Z_θ = pulsed thermal impedance

Figure 7 shows pulsed thermal impedance versus pulse duration for Unitrode transient voltage suppressors. These curves give Z_θ values for rectangular power pulses. A designer should determine the pulse energy equivalent for his specific pulse, and use the duration of that pulse when employing Figure 7.

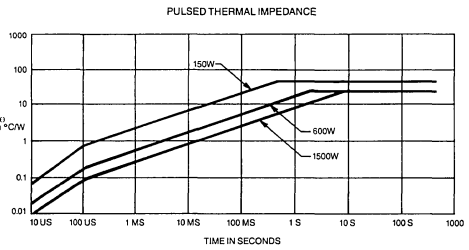

FIGURE 7

To carry the thermal analysis one step further, and to be more rigorous, one can consider the effective thermal impedance for a given repetitive pulsing situation to be as follows:

$Z_{\theta eff} = (R_{\theta J-A})\,(t/\tau) + (1-t/\tau)\,[r(t+\tau)] - r(\tau) + r(t)$

Where: $Z_{\theta eff}$ = effective pulsed thermal impedance

t = pulse width

τ = period

$r(t+\tau)$ = transient thermal impedance at time $t+\tau$

$r(t)$ = transient thermal impedance at time t

$r(\tau)$ = transient thermal impedance at time τ

The peak junction temperature of a device subjected to a periodic train of power pulses can be calculated by using the following relation:

$T_{j\,(peak)} = T_{ambient} + (P_D) \times (Z_{\theta eff})$

IMPORTANCE OF JUNCTION TEMPERATURE

A clear understanding of the junction temperature is important to the designer for two reasons:

1. The maximum junction temperature is the fundamental criterion for device reliability assurance. Unitrode transient voltage suppressors will operate with virtually no permanent degradation if the junction temperature is kept below 175°C. This criterion allows the designer to choose the proper TVS (body size/rated maximum power dissipation) for his application.
2. The thermally related change in V_{TVS} is given by

   ΔV_{TVS} (thermal) = $Tj \times TC/100 \times BV_{min}$

   Where TC = temperature coefficient of reverse voltage in percent of BV_{min}/°C

   BV_{min} = minimum breakover voltage

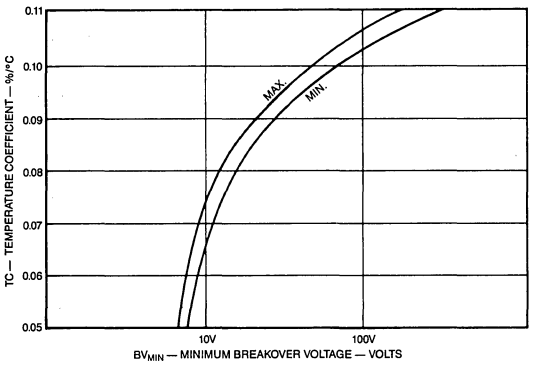

FIGURE 8

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Figure 8 shows TC as a function of stand off voltage for Unitrode transient voltage suppressors.

Although, as stated above, the junction temperature is clearly related to the long term reliability of the TVS, it must be noted that a failure mechanism not strongly related to junction temperature, but rather to current density manifests itself — when the transients are very short in duration (less than 1 micro second) and the values of current are very high. Conditions which may generate this type of transient may possibly occur in some equipment as a result of an electromagnetic pulse.

COMPARISON OF SUPPRESSOR TECHNOLOGIES

It would be helpful to the designer to have a better feel for the relative merits associated with the different types of transient suppression devices and schemes available today. A comparison of the different suppression technologies available today is presented in Table 1.

R-C snubber networks, though not shown in the table, are often used alone or in combination with other types of transient voltage suppressors. Often a snubber can be chosen which would limit the voltage across a sensitive component until the current has reached a safe level. However, in certain situations, an R-C network designed to minimize transients can have negative effects. R-C networks may cause undesirable time delays in relay or solenoid applications. The use of a semiconductor TVS would minimize the problem and the component count would be less.

In conclusion, the advantages of a semiconductor transient suppressor are as follows:

- low insertion loss
- simplification of protection circuitry
- immediate recovery after operation
- most effective clamping
- protection against fast rising transients
- circuit operation can continue for the duration of the transients

Unitrode offers a wide range of transient voltage suppressors that are suitable for many common transient suppression applications.

Table 1

	Clamping Ratio	Clamping Speed (Typical)	Active or Passive	Allowable Current (for 1ms)	Available Voltages	Degradation?	Size	Cost	Typical Applications	Protection From:
Spark Gap or Gas Tube	~0*	10^{-5}s	Active	10^{3}–10^{5}A	to 20kV DC	No	Large	Very High	Phone Lines Input to Heavy Equip.	Lightning
Thyristor Crowbar	~0*	10^{-7}–10^{-4}s	Active	to 10^{3}A	to 800V AC or DC	No	Moderate to Large	High	DC Power Supply	Output Over-Voltage Protection
Metal Oxide Varistor	1–2	10^{-9}–10^{-7}s	Passive	100A	10–260V AC (RMS)	Yes	Small to Moderate	Low to Moderate	AC Line to Equip. and Instruments	Transients due to Load Changes and Lightning
Semi-conductor TVS	1–1.5	10^{-12}s	Passive	50A (See Note)	5–400V AC or DC	No	Small	Low to Moderate	"on-board" Protection	Internally** Generated Transients

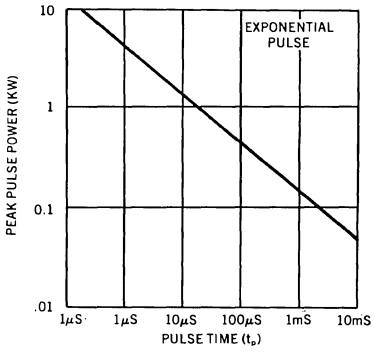
*After triggering on only.
**All types of transients as a final line of defense.

TABLE 1. COMPARISON OF TRANSIENT SUPPRESSORS

NOTE: Though the values in this column are useful for comparing suppressor technologies on a one to one basis it must be noted that for shorter pulse widths a semiconductor TVS is capable of sustaining hundreds of amperes. For example the smallest TVS component Unitrode presently offers was tested with a 200 nanosecond exponentially decaying waveform with a rise time of 10 nanoseconds. This device did not suffer degradation until peak values of 600 amperes had been reached. This is an extremely important point as the other technologies have response times which severely limit their effectiveness when the pulse widths and the associated current rise times are of this nature. Non-semiconductor types are excessively slow in response such that the circuit is not adequately protected. In cases where the transients are of very short duration the only viable solution is to use a semiconductor TVS.

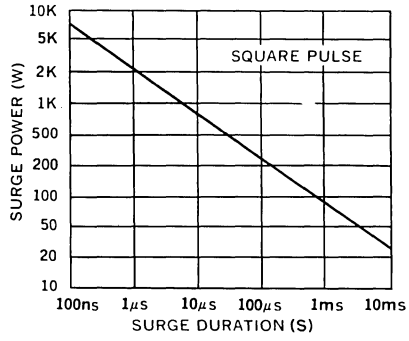
Appendix

Peak Pulse Power vs. Pulse Duration



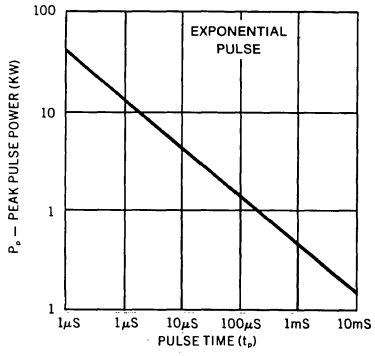
150W Devices[1]

Surge Power vs. Surge Duration



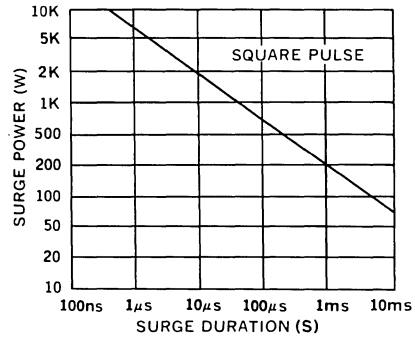
150W Devices[1]

Peak Pulse Power vs. Pulse Duration



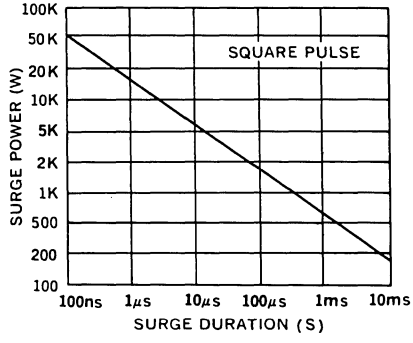
500W Devices[1]

Surge Power vs. Surge Duration



500W Devices[1]

Surge Power vs. Surge Duration



1500W Devices[1]

[1]Power level based on standard 1ms exponential waveform.

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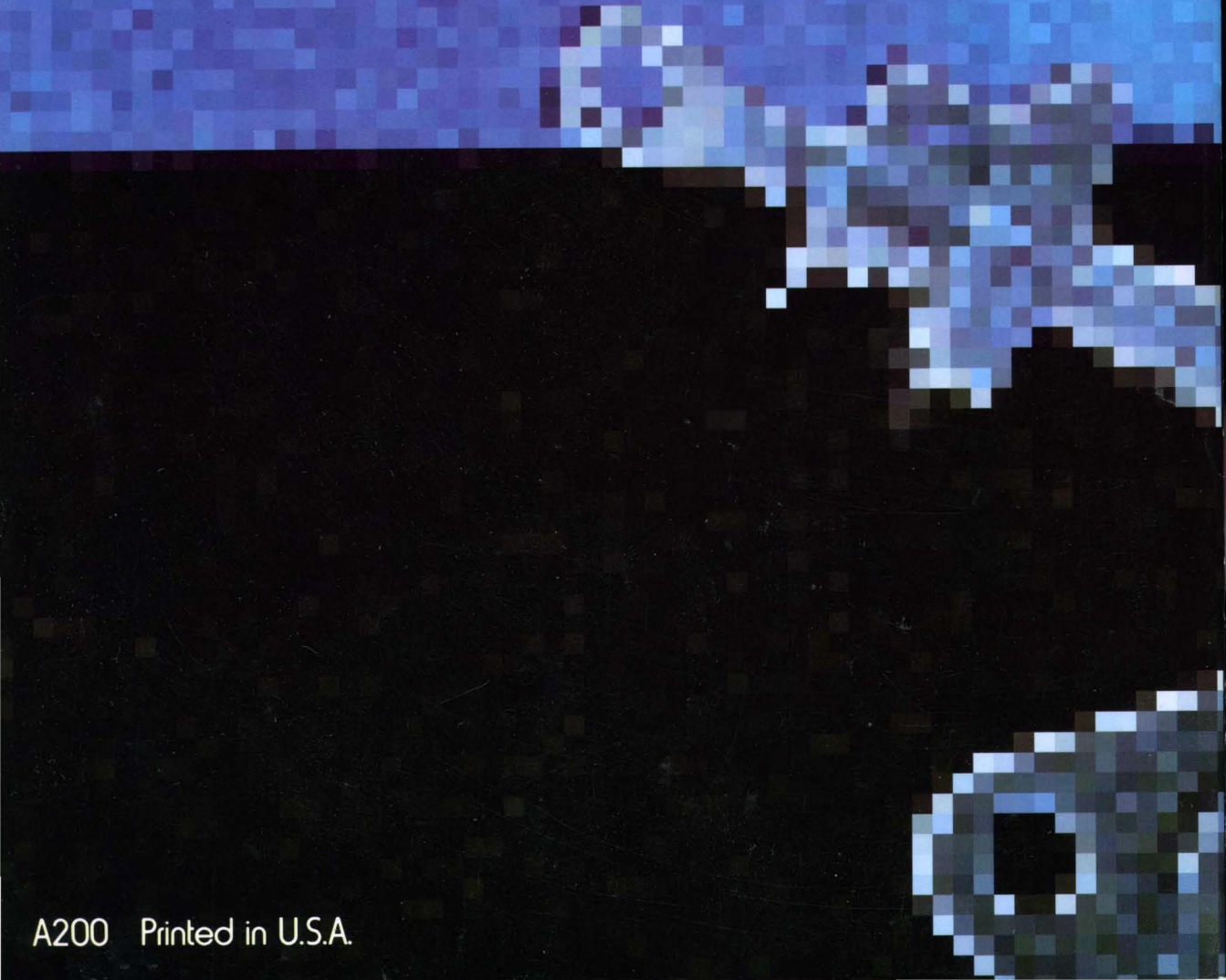

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