The FlexSet™ PC/AT
80386SX System & Memory Controller
SL9252

PRELIMINARY

FEATURES

- 100% PC/AT Compatible
- Supports 80386SX-based Systems
- Up to 25 MHz Performance
- ISA Bus Control Logic
  - Synchronous or Asynchronous System Control Operation
  - Programmable Command Delays
  - Numerical Co-processor Support
  - Programmable Wait States for Local and Off-board Cycles
  - Fast Gate A20 and Fast Reset
- Memory Control Logic
  - Enhanced Page Mode/2-Way Word/4-Way and Multi-Page Interleave
  - Supports up to 16M bytes of On-Board Memory
  - Shadow RAM Feature for System, Video
  - Can use 4M, 1M and 256K DRAMs or a mix
  - Staggered Memory (RAS) Refresh
- Programmable Memory Options
  - User Selectable 8 or 16 bit ROM with Selectable wait states
  - Selectable Hit (0-3) and Miss (1-4) wait states for DRAM access
  - 512 X 512 Split Memory Mapping Option
  - Disable (On Board) Memory to 0K in 128K Resolution
  - Memory Backfill
  - EMS Mapping Registers
    - 1 Set of 4 Registers
    - Each Register Maps 16K anywhere above 1M Memory
- Advanced Testability Features
- Advanced, Low Power CMOS Technology, Ideal for Notebooks
- 160-Pin PQFP

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VIA Technologies, Inc. (408) 746-2200
860 East Arques Avenue
Sunnyvale, CA 94086

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BLOCK DIAGRAM SL9252

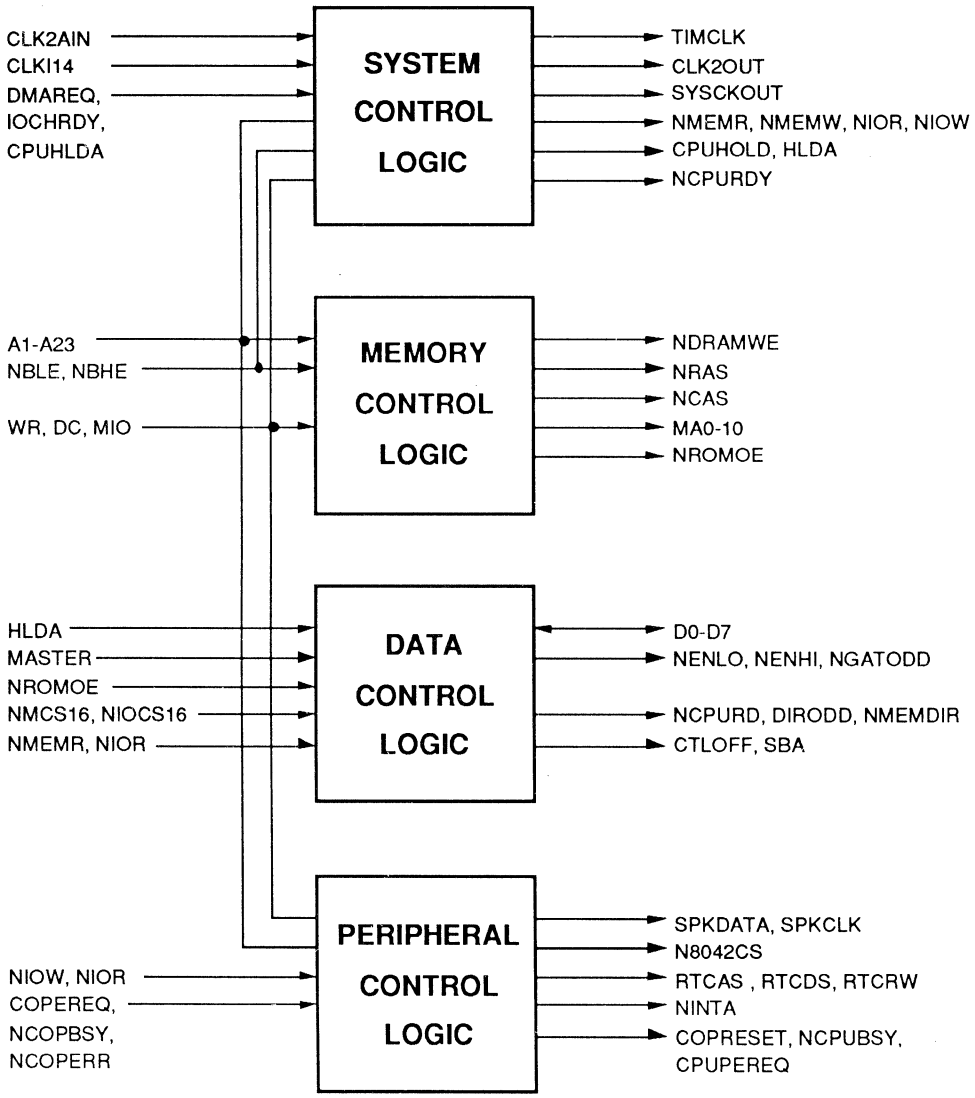


Fig. 1 Functional Block Diagram

I. GENERAL DESCRIPTION

VIA's System and Memory Controller SL9252, has integrated the logic for the System Control, Memory Control, Data Control and, in addition, provides chip select for many of the peripherals used in an AT system. The SL9252 provides a high degree of flexibility with configurability via software control. No external hardware jumpers are needed to configure features. Default values are provided to boot any system configuration. On reset, BIOS routines are used to program the device, transparent to the user, to utilize its enhanced capabilities.

Four configuration registers in the System Control Logic control the AT bus and peripheral bus operations. Synchronous and asynchronous bus operations are supported. In synchronous mode, bus clock is derived from the processor's CLK2. In asynchronous mode, it is derived from an independent external bus clock pin.

Support for page mode and non-page mode operations with non-interleave or word/multi-page interleave, along with programmable memory timing, allow the system designer to get maximum performance for the chosen DRAMs. High drive for RAS, CAS, memory address, and write lines are provided to connect the SL9252 directly to a large DRAM memory array without external buffering. In addition, CAS for all the banks in non-interleave and 2-way interleave are provided to reduce external logic typically required in other solutions.

Shadowing features are supported in 16K granularity from 640K to 1M. Remap options allow shadowing of eight different combinations of top of memory, Local ROM, and Video ROM to 640K to 1M region.

VIA's System and Memory Controller, SL9252, can be used either with one of VIA's SL9020 Data Controllers, or with discrete latches and buffers. Data direction and enable signals for the data controller are provided for both modes of operation.

SL9252 provides decoding for the Real Time Clock and the Keyboard Controller, thus avoiding external decoding logic. In addition, Port B logic, PS/2 Compatible Port 92 for fast reset, and A20GATE provide the necessary logic support for a one-chip solution.

All outputs except clocks and reset can be tri-stated for on-board testing.

Figure 1 shows the Functional Block Diagram of SL9252. The SL9252 is logically divided into 4 blocks:

a. System Control Logic
b. Memory Control Logic
c. Data Control Logic
d. Peripheral Control Logic

Sections III-VI provide detailed operational descriptions of these four internal blocks.

PINOUT

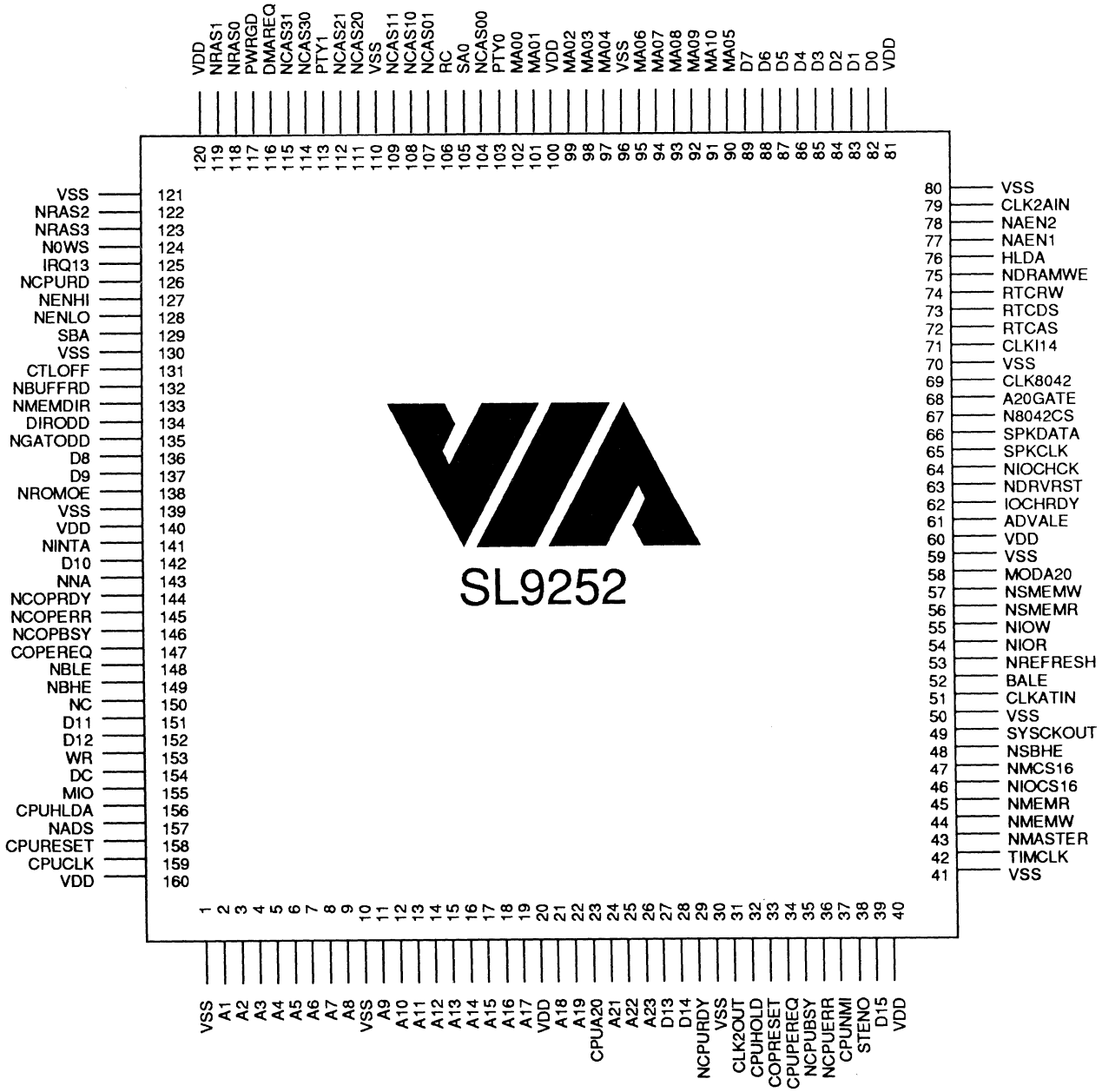


Fig. 2 SL9252 Pinout

II. PIN DESCRIPTIONS SL9252

SYMBOL	PIN	TYPE	DESCRIPTION
			CLOCK AND RESET SIGNALS
CLKI14	71	I	Clock In 14.31818 MHz. 14 MHz input from oscillator.
CLK2AIN	79	I	Input Clock used to generate CLK2 and clock internal state machine. It is twice the frequency of the CPU clock.
CLKATIN	51	I	Asynchronous AT Clock Input. CLKATIN is twice the BUSCLK frequency, generated from the oscillator.
CLK2OUT	31	O	Clock 2 Output to CPU.
CLK8042	69	O	CLK8042 is CLKI14 divided by two. It is the keyboard controller clock.
COPRESET	33	O	Reset 387 is an active HIGH output. It is generated in response to any one of the following signals: PWRGD, RC, and PS/2 Fast Reset. It is also asserted when I/O port 00F1 is written to. The signal is active for 96 CPUCLK cycles.
CPURESET	158	O	Reset Signal to the CPU is an active HIGH output. It is generated in response to any one of the following signals: PWRGD, RC and PS/2 fast reset.
NDRVRST	63	O	Device Reset is an active LOW output. It is used to reset the SL9025 Address Controller and Keyboard Controller.
PWRGD	117	I	Power Good is an active HIGH input from the power supply. A reset switch can be connected to this signal.
SYSCKOUT	49	O	System Clock Out is a free running system clock generated by dividing CPUCLK by 2. In synchronous mode it is synchronized with NADS. In asynchronous mode, it is generated from CLKATIN.
TIMCLK	42	O	1.19 MHz Timer Clock.
			CPU INTERFACE SIGNALS
A1-19, A21-23	2, 3,4,5,6,7,8,9,11, 12,13,14,15,16,17 18,19,21,22,24, 25,26	I/O	These address lines are inputs for CPU, DMA, and AT bus MASTER accesses and outputs during refresh cycle. A1 to A11 have the refresh address. A12-A19 and A21-A23 are LOW during refresh.

PIN DESCRIPTIONS SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			CPU INTERFACE SIGNALS Cont'd
A20GATE	68	I	Internal Address 20 is forced LOW when A20GATE is LOW and is same as generated by CPU when A20GATE is HIGH.
ADVALE	61	O	Advanced Address Latch Enable from the memory control logic. It latches local bus address for the system bus.
CPUA20	23	I/O	CPU Address Bus, bit 20. Output for ATbus MASTER accesses.
CPUCLK	159	O	Clock synchronized with 386SX internal clock. It is CLK2 divided by two.
CPUNMI	37	O	CPU Non-Maskable Interrupt, generated from PERR or NIOCHCK. Output to 80386.
CPUPEREQ	34	O	CPU Processor Extension Request. When active (HIGH) it indicates to CPU that NPX is ready for data transfer to/from its data FIFO. When FIFO is empty, this signal is negated. CPUPEREQ connects directly to the PEREQ pin on the CPU.
D0-D15	82,83,84,85, 86,87,88,89, 136,137,142, 151,152,27,28,39	I/O	CPU data bus to read/write SL9252 registers, and to generate and check memory parity.
DC	154	I	CPU Status Signal. Differentiates between Data and Control instructions.
MIO	155	I	Memory Input/Output signal from the CPU. When HIGH, it indicates a memory cycle, when LOW, it indicates an I/O cycle.
NCPURDY	29	O	Ready to CPU to terminate the cycle. Ready for local RAM, ROM (16 or 8 bit) accesses, on-chip I/O and AT bus accesses generated in SL9252. External Coprocessor ready is an input to the SL9252 and is OR'd with internal ready.
NADS	157	I	Address Strobe is an active LOW input generated by the CPU. When asserted it indicates the start of a new cycle.

PIN DESCRIPTIONS SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			CPU INTERFACE SIGNALS Cont'd
NNA	143	O	CPU control input, Next Address. Asserted for address pipe-lining. Enables CPU to output address and status signals for the next Bus cycle during the current cycle.
WR	153	I	CPU output control signal Write.
			MEMORY INTERFACE SIGNALS
MA00-MA10	102,101,99,98,97, 90,95,94,93,92,91	O	RAM Address Bus Output. Directly drives DRAM address inputs.
NCAS00	104	O	Memory Column Address Strobe. Asserted when CPU, DMA or MASTER is accessing Bank 0, byte 0.
NCAS01	107	O	Memory Column Address Strobe for Bank 0, byte 1.
NCAS10	108	O	CAS for Bank 1, byte 0.
NCAS11	109	O	CAS for Bank 1, byte 1.
NCAS20	111	O	CAS for Bank 2, byte 0.
NCAS21	112	O	CAS for Bank 2, byte 1.
NCAS30	114	O	CAS for Bank 3, byte 0.
NCAS31	115	O	CAS for Bank 3, byte 1.
NDRAMWE	75	O	Active Low Memory Write signal. Used to drive DRAM write input.
NMEMDIR	133	O	Direction Select between D Bus and MD Bus. When LOW, direction is from MD Bus to D Bus (MEM Read). When HIGH, the direction is from D Bus to MD Bus (MEM Write). It is also used to drive SL9020 NMEMDIR input, when using the SL9020.
PTY0	103	I/O	Parity for LOW byte (D0 - D7).
PTY1	113	I/O	Parity for HIGH byte (D8 - D15).

PIN DESCRIPTIONS SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			MEMORY INTERFACE SIGNALS Cont'd
NRAS0-3	118,119,122,123	O	Row Address Strobes for Banks 0,1,2 and 3 for the on-board memory. Generated during CPU, DMA or MASTER cycle for memory access. Used to directly drive DRAM RAS inputs for banks 0 - 3.
NROMOE	138	I/O	Bi-directional pin which enables ROM output during ROM read cycles. During power-up, this is an input, and if pulled LOW an 8 bit ROM is assumed. Connects directly to ROMOE pin.
			COPROCESSOR INTERFACE SIGNALS
COPEREQ	147	I	NPX Peripheral Request is an active HIGH input from NPX. When asserted it causes CPUPEREQ to assert, indicating to the CPU that NPX is ready to transfer data to/from its data FIFO. When all data is written to or read from the data FIFO, PEREQ is negated.
IRQ13	125	O	Interrupt Request 13 is an active HIGH output which indicates an interrupt from the numeric coprocessor. It connects to the SL9030 pin IRQ13.
NCOPBSY	146	I	Numerical Coprocessor (NPX) Busy is an active LOW input indicating that NPX is currently executing a command. It is used to generate a busy signal to the CPU, NCPUBSY.
NCOPERR	145	I	NPX Error is an active LOW input from 80387SX. When asserted it indicates that a non-maskable exception has occurred during the current command cycle. It is used to generate NCPUERR.
NCOPRDY	144	I	Coprocessor Ready is an active LOW input from the NPX to terminate an NPX bus cycle.
NCPUBSY	35	O	CPU Busy is an active LOW output to the CPU indicating that the NPX is busy executing a command. It connects to the CPU pin BUSY.
NCPUERR	36	O	CPU Error is an active LOW output from the NPX to the CPU indicating that an unmasked error condition exists. NCPUERR connects to the ERROR input pin on the CPU.

PIN DESCRIPTIONS SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			COPROCESSOR INTERFACE SIGNALS, Cont'd
STENO	38	O	Status Enable is an active HIGH output. This pin serves as a chip select for the 80387. When inactive, it forces the NPX outputs NBUSY, PEREQ, NERROR and NRDY into floating state.
			BUS CONTROL AND INTERFACE SIGNALS
ADVALE	61	O	Advanced Address Latch Enable from the memory control logic. It latches local bus address for the system bus.
BALE	52	O	Buffered Address Latch Enable. Directly drives AT slot signal BALE.
CTLOFF	131	O	Control Output Flag. Rising edge clocks data from SD [7:0] to D[7:0] latches during Bus-conversion cycles. Connects directly to the SL9020 pin CTLOFF.
DIRODD	134	O	Direction ODD. Controls data transfer direction between SD[7:0] and SD[15:8] in the SL9020 Data Controller. NGAT1 must be asserted. It is used during data conversion (8 bit SLOT Read/Writes) cycles.
IOCHRDY	62	I/O	I/O Channel Ready is an active HIGH input from the AT bus. When LOW it indicates a not ready condition and inserts wait states in AT bus or peripheral bus cycles. It is used to generate NCPURDY, and is an output during the NPX reset cycle.
MODA20	58	I/O	CPU Address 20 gated with A20GATE.
NAEN1,2	77,78	I	DMA Enable 1,2 are active LOW inputs from the SL9030. When NAEN1 is asserted LOW it indicates an 8-bit DMA cycle. When NAEN2 is asserted LOW it indicates a 16-bit DMA cycle. When both are HIGH it indicates that a non-DMA device owns the system's bus controls. They should not be LOW at the same time. They are used to generate direction control signals NSBHE, SBA, NENHI and NENLO.
NBLE	148	I	Active LOW Byte Enable 0 from CPU.
NBHE	149	I	Active LOW Byte Enable 1 from CPU.

PIN DESCRIPTIONS SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			BUS CONTROL AND INTERFACE SIGNALS Cont'd
NBUFFRD	132	O	Direction control for buffer between SD Bus and XD Bus.
NCPURD	126	O	CPU Read is an active LOW output to the SL9020 Data Controller or D to SD buffers that sets the direction of data between D0-D15 and SD0-SD15. When asserted, the direction is from SD to D.
NENHI	127	O	Enable HIGH byte to the SL9020 Data Controller or D to SD buffers, is asserted LOW to enable HIGH byte data transfer between D8-D15 and SD8-SD15.
NENLO	128	O	Enable LOW byte to the SL9020 Data Controller, is asserted LOW to enable LOW byte data transfers between D0-D7 and SD0-SD7.
NGATODD	135	O	This is asserted LOW to enable the data buffer between HIGH byte and LOW byte of SD Bus. It is used in bus conversion cycles to assemble 8 bit bytes into 16 bit words in the SL9020 Data Controller.
NIOCHCK	64	I	I/O Channel Check is an active LOW signal from the AT bus to assert CPUNMI.
NIOCS16	46	I	Peripheral I/O Chip Select 16 is an active LOW input. It is asserted from the AT bus by a 16-bit I/O device to indicate a 16-bit bus cycle. When HIGH it implies an 8-bit I/O transfer. It is used to control NGATODD.
NIOR	54	I/O	Input/Output Read is an active LOW bi-directional signal. It is an output when the CPU is reading peripheral or AT bus ports. It is an input for DMA and AT bus Master.
NIOW	55	I/O	Input/Output Write is an active LOW bi-directional signal. It is an output when CPU is writing to peripheral or AT bus ports. It is an input for DMA and AT bus Master.
NMASTER	43	I	External Master is an active LOW input from the AT bus. When asserted, it indicates that an external master device is currently active.

PIN DESCRIPTIONS SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			BUS CONTROL AND INTERFACE SIGNALS Cont'd
NMCS16	47	I	Memory Chip Select 16 is an active LOW input from the AT bus. When asserted it indicates a 16 bit memory cycle. When HIGH it implies an 8-bit memory transfer. It is used to control NGATODD.
NMEMR	45	I/O	Memory Read is an active LOW bi-directional signal. It is an output when CPU is reading peripheral or AT bus memory, and during refresh cycle. It is an input for DMA and AT bus Master.
NMEMW	44	I/O	Memory Write is an active LOW bi-directional signal. It is an output when CPU is writing peripheral or ATbus memory. It is an input for DMA and AT bus Master.
N0WS	124	I	Zero Wait State is an active LOW input from the AT System bus. It causes termination of a bus cycle.
NSBHE	48	I/O	Byte HIGH Enable is an active LOW bi-directional pin for the AT bus. It indicates the transfer of data on the HIGH byte of the data bus. It is also asserted for 16-bit bus cycles. It is an output for CPU and DMA cycles and an input for an external master cycle.
NSMEMR	56	O	System Memory Read is active for a read access to lower 1 Meg memory. At all other times it is tri-stated.
NSMEMW	57	O	System Memory Write is active for a write access to lower 1 Meg memory. At all other times it is tri-stated.
SA0	105	I/O	System Bus Address 0-bit is a bi-directional pin. It is an output for CPU, Refresh and an input for DMA and AT bus Master. During refresh, it has the LSB refresh address.
SBA	129	O	Select Data Buffer Data. This signal drives the SL9020 Data Controller. When HIGH it selects latched SD Bus LOW byte data during bus conversions cycles. When LOW, unlatched SD Bus LOW byte data will pass onto D Bus.

PIN DESCRIPTIONS SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			HOLD INTERFACE SIGNALS
CPUHLDA	156	I	CPU Hold Acknowledge. It is active HIGH whenthe bus is granted in response to hold request (HOLD). It is used to generate HLDA.
CPUHOLD	32	O	Hold is asserted HIGH whenever another bus master device like DMA or an external master wants to become a bus master. The signal goes to the CPU.
DMAREQ	116	I	DMA Request is asserted HIGH to request a bus from CPU. It initiates hold request (HOLD) to the CPU for a DMA cycle to begin. Normally, the SL9030 Integrated Peripheral Controller (IPC) signal CPUHRQ is connected to this.
HLDA	76	O	Hold Acknowledge is an active HIGH output to the SL9030 IPC. When asserted it indicates that the CPU has released its control on the local bus in favor of another bus master device (DMA external master). It is generated by resynchronizing CPUHLDA with CPUCLK.
NREFRESH	53	I	On-board RAM refresh signal.
			PERIPHERAL INTERFACE SIGNALS
N8042CS	67	O	Active LOW keyboard controller Chip Select.
NINTA	141	O	Interrupt Acknowledge is an active LOW output for the interrupt controller. It is also used to direct data from the XD bus to SD bus during an interrupt acknowledge cycle.
RC	106	I	External CPU Reset is an active LOW input. When asserted it resets the CPU by generating CPURESET. It is connected to the Keyboard Controller.
RTCAS	72	O	Active HIGH Real Time Clock Address Strobe.
RTCDS	73	O	Active LOW Real Time Clock Address Strobe.
RTCRW	74	O	Active LOW Real Time Clock Write Enable.
SPKCLK	65	I	Speaker Clock.

PIN DESCRIPTIONS SL9252 (Cont'd)

SYMBOL	PIN	TYPE	DESCRIPTION
			PERIPHERAL INTERFACE SIGNALS Cont'd
SPKDATA	66	O	Active HIGH speaker data output. This is used to gate the timer tone signal to the speaker.
			POWER AND GROUND SIGNALS
VDD	20,40,60,81,100, 120,140,160	-	+5V. Power.
VSS	1,10,30,41,50,59, 70,80,96,110,121, 130,139	-	0V. Ground.
			MISCELLANEOUS SIGNALS
NC	150	-	No Connect.

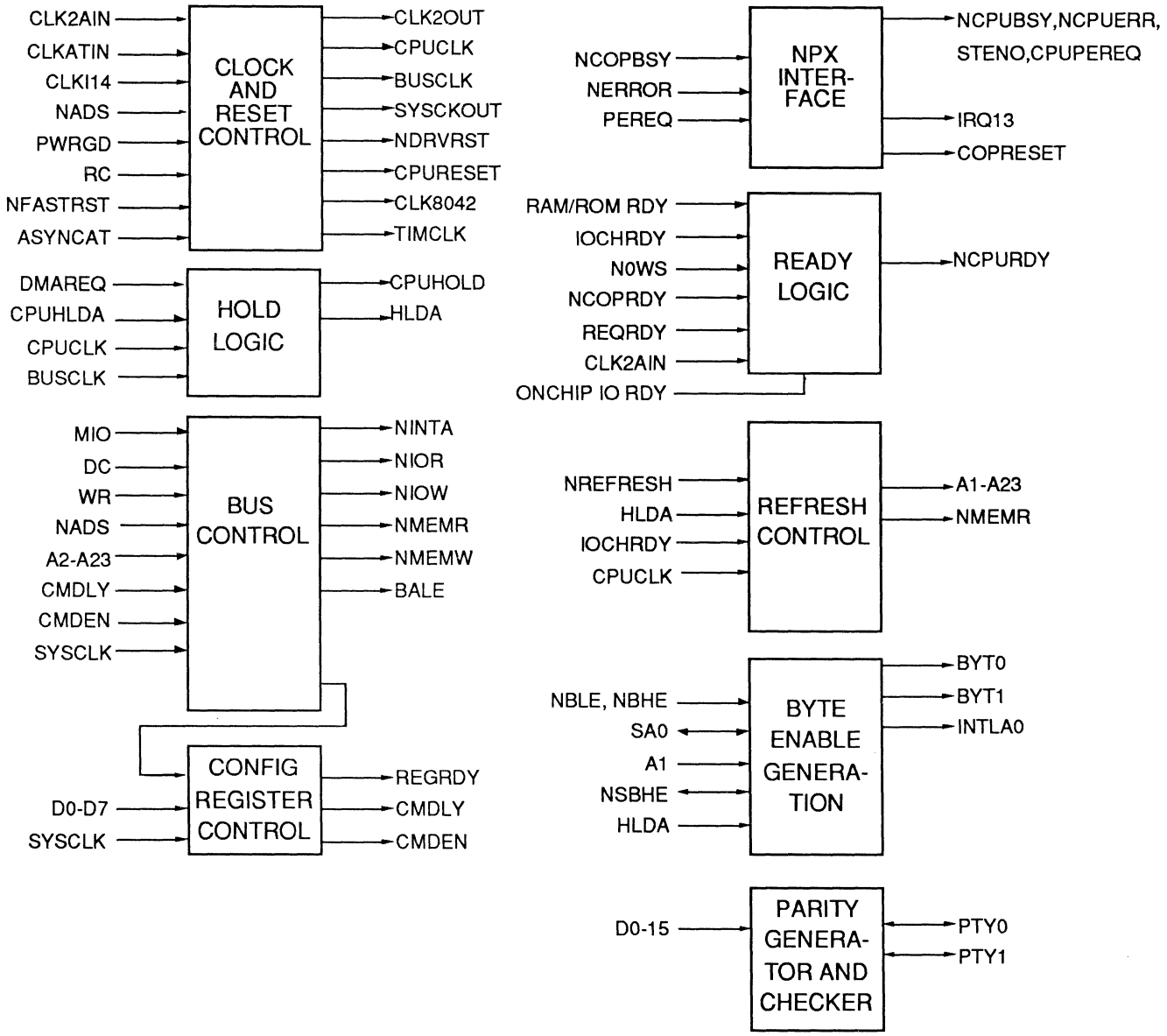


Fig. 3 SL9252 System Control Internal Logic Block Diagram

III. SYSTEM CONTROL LOGIC

Figure 2 shows the block diagram of the system control logic. System control is divided into ten sections:

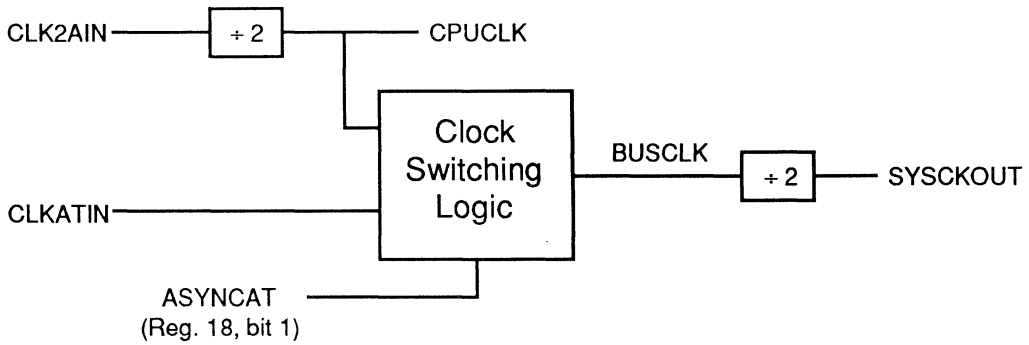
a. Clock and Reset Control
b. Hold Logic
c. Bus Control Logic
d. BALE Control
e. Coprocessor Interface
f. Ready Logic
g. Refresh Counter Logic
h. Byte Enable Generation
i. PS/2 Compatible Port 92
j. Test Mode Logic

a. Clock and Reset Control

The clock inputs to the chip are:

1. CLK2AIN
2. CLKI14
3. CLKATIN.

The processor clock, CLK2, CPUCLK, and system clock SYSCKOUT are derived from CLK2AIN. In asynchronous mode SYSCKOUT is derived from CLKATIN. Asynchronous clock selection for the system clock is performed using the control bit ASYNAT in register 18h. CLKI14 is the 14MHz clock used to derive the 8042 clock and TIMCLK. SYSCKOUT generation is as shown in diagram below:



The SL9252 generates CPU reset (CPURESET), coprocessor reset (COPRESET) and system bus reset (NDRVRST) from PWRGD, RC, and PS/2 compatible port 92 fast reset. External reset through a switch can be provided by pulling the PWRGD line low. RC is the keyboard controller output that generates software reset. CPURESET will go active from 3 to 11 CPUCLKs after RC is asserted. It will go inactive either 16 CPUCLKs later or 16 CPUCLKs after RC is negated. An equivalent high speed reset can be generated through port 92 bit 0. As with RC and fast reset, CPURESET will go active within 3 to 11 CPUCLKs of detecting the shutdown command and be negated 16 CPUCLKs later. CPURESET is always asserted and negated at the beginning of Phase 1.

b. Hold Logic

The hold request to the CPU and hold acknowledge to external devices (e.g. VIA SL9030 Integrated Peripheral Controller) are synchronized with CPUCLK and BUSCLK. External devices that request the bus should assert DMAREQ and use HLDA as the hold acknowledge.

c. Bus Control Logic

The SL9252 contains logic to generate bus command and control signals in four modes of operation. The most commonly used is the CPU mode. This is active whenever there is no HLDA. The other three modes, DMA, MASTER and REFRESH, can be active only when HLDA is high (active).

During CPU mode the commands NMEMR, NMEMW, NIOR, NIOW are in output mode. One of these is asserted for an AT-bus or peripheral bus access. The command delay can be programmed separately for 8-bit and 16-bit memory and I/O devices through Register 1Bh (Sec VII, p. 60). The command delay is from BALE trailing edge in multiples of BUSCLKs.

The bus activity and signal state of the SL9252 depend on the mode of operation. DMA is master when NAEN1 or NAEN2 (but not both) is asserted during HLDA. If NREFRESH is asserted during HLDA, it is in refresh mode. The AT bus Master is a master when NMASTER is asserted during HLDA. Table 1 below lists the various signals and their state for the modes mentioned above.

SIGNAL	MODE			
	CPU	DMA	AT Bus MASTER	REFRESH
NMEMR	O	I	I	O
NMEMW	O	I	I	I
NIOR	O	I	I	I
NIOW	O	I	I	I
SA0	O	I	I	I
NSBHE	O	O	I	O
A2-19,A21-23	I	I	I	O
CPUA20	I	I	O	I
LA20	O	O	I	O

O = Output I = Input

Table 1 Signal Direction Descriptions

d. BALE Control

The position and width of BALE can be programmed using Register 18h (sec VII, p. 57), bits 4-6 are shown in the diagrams below. During BALE's active period, SYSCKOUT is low.

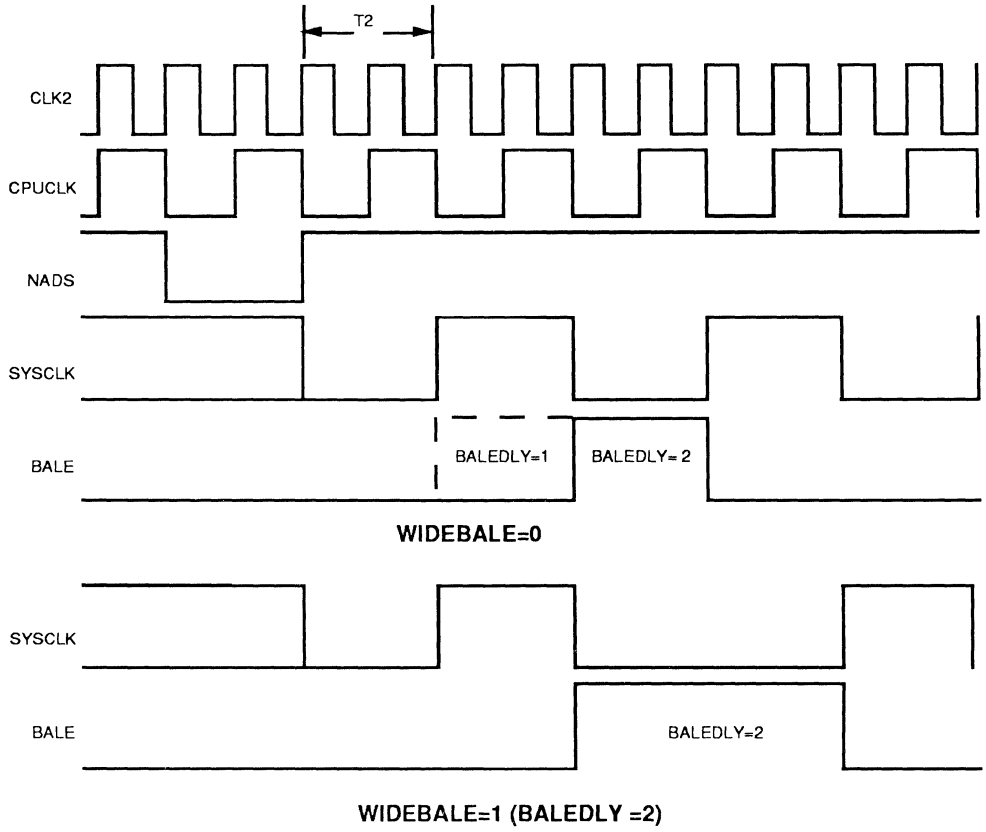


Fig. 4 BALE Waveforms (Sync Mode)

Table 2 shows the values of the SYSCTL Register 18h bits 4 and 5, the BALEDLY bits:

Register 18h		
Bit 5	Bit 4	BALEDLY
0	0	0
0	1	1
1	0	2
1	1	Reserved

Table 2 BALEDLY Bits

Bit 6 of the SYSCTL Register 18h is the WIDEBALE bit. When Bit 6 is 0, BALE equals the BUSCLK period. When Bit 6 is set to 1, BALE equals two times the BUSCLK period.

Register 18h	
Bit 6	BALE Width
0	BALE = BUSCLK
1	BALE = 2 x BUSCLK

Table 3 BALE Width

e. Coprocessor Interface

The SL9252 generates reset for coprocessor 387 and is asserted whenever CPURESET is asserted. The reset to the coprocessor can be disabled during RC and SHUTDOWN resets by setting Bit 1 in Register 17h (sec VII, p. 56). It can also be activated through an I/O write to address 0F1h. It is active for 96 CPUCLK cycles. IOCHRDY will be asserted when COPRESET is active. It will be negated 95 CPUCLKs after COPRESET is negated.

From reset until the first CPU cycle, coprocessor error NERROR is routed to the CPU as NCPUERR. If the coprocessor error is detected during a coprocessor busy period, STENO is negated and interrupt request 13 is asserted. It also latches CPUBSY. CPUBSY is asserted to prevent the processor from accessing the coprocessor until the error handling routine is completed. The interrupt handler clears the latched BUSY condition, by performing a dummy write to I/O port 0F0h. STENO and IRQ13 are also negated by writing to port 0F0h.

During a coprocessor access, if there is no ready from the coprocessor, the SL9252 will issue a coprocessor timeout ready to the CPU. The timeout can be disabled by setting Bit 3, DICPTMOUT, of Register 18h (sec VII, p. 57).

f. Ready Logic

The SL9252 generates ready for DRAM, on-chip I/O and bus accesses. Wait states for DRAM accesses may be programmed separately for HIT and MISS cycles through register 08h. For the same number of wait states the pipeline mode ready will be one CPUCLK later compared to non-pipeline mode ready. On-chip I/O accesses have 1 wait state. The bus access wait states can be programmed separately for 16 bit and 8 bit devices. They can also be programmed separately for memory and I/O devices using Registers 19h and 1Ah. The CPU ready is asserted (if IOCHRDY is high) after the programmed number of wait states. The wait states are calculated from BALE's leading edge in steps of SYSCLK's. IOCHRDY can be pulled low to extend the cycle. Wait states are introduced until IOCHRDY is de-asserted. N0WS overides IOCHRDY and the programmed wait states and current cycle is terminated as soon as it is detected internally and synchronized to CLK2. These three ready sources are combined with NCOPRDY (coprocessor ready) to generate the ready to the CPU.

g. Refresh Logic

The SL9252 contains logic for a refresh counter and refresh RAS generation. The refresh cycle starts when NREFRESH is asserted low and HLDA is active. Staggered refresh is enabled by setting the two stagger RAS control bits in Register 12h. During refresh NRAS0-3 are asserted low, NCAS00 and NCAS31 are held high, and the current bus state is ignored. The Refresh counter is incremented at the end of the refresh cycle. The refresh address is an output on SA0 and A1 through A11. During refresh, the address bus can be tri-stated by setting Bit 7, DIRFADSOUT, of Register 17h (sec VII, p. 56). A12 through A19 and A21 through A23 are zero during refresh.

h. Byte Enable Generation

Two byte enable controls for asserting CAS are generated using the enables from the CPU, SA0 and NSBHE. During DMA and MASTER address input, SA0 and NSBHE decide the low or high byte within a word. During a DMA mode, NSBHE is generated internally by the SL9252, based upon 8 bit or 16 bit DMA mode.

i. PS/2 Compatible Port 92

PS/2 compatible port 92 to issue fast reset and fast A20GATE are provided in the SL9252 System and Memory Controller. On reset, fast reset logic is disabled. It can be enabled through bit 1 of Register 13h (sec VII, p. 53).

j. Test Mode

For in-socket on-board testing, all outputs except CLK2OUT, CLK8042, SYSCKOUT, TIMCLK, CPUCLK, CPURESET, COPRESET, and NDRVRST can be tri-stated by forcing the following inputs to the specified logic level: DMAREQ = 0, CPUHLDA = 0, NAEN1 = 0, NAEN2 = 0, NMASTER = 0, NREFRESH = 0.

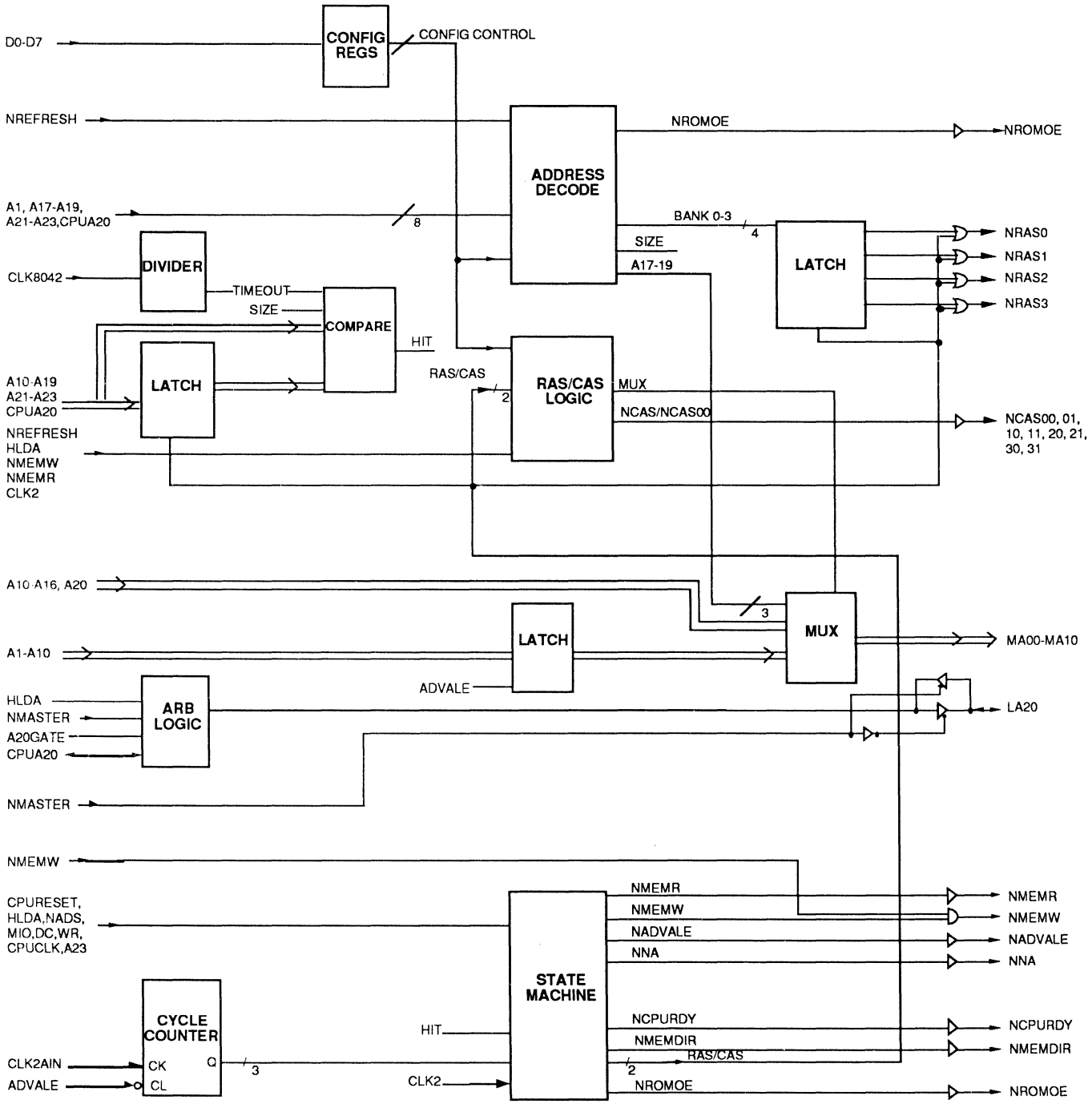


Fig. 5 SL9252 Memory Control Internal Logic Block Diagram

IV. MEMORY CONTROL LOGIC

SL9252's Memory Control Logic section provides the control interface between the CPU, DMA, MASTER and local DRAM for non-interleave and interleave modes of operation in page mode. The SL9252 provides an advanced page mode capability that allows multiple pages in different banks to be active simultaneously. Page misses are reduced and performance is enhanced by utilizing this capability. When memory interleaving is used, up to four pages, one for each bank, may be active at any instant in time. Below are descriptions of VIA's non-interleave and interleave modes.

Non-Interleave
In page non-interleave mode there is only one page active. The page size is 2K bytes for 256K, 4K bytes for 1M and 8K bytes for 4M memories. It is doubled for 2-way word interleave and quadrupled for 4-way word interleave.

Word/Block Interleave
In word interleave and block interleave mode, the memory is arranged in interleave mode with successive words in alternate banks. All RASes will go active and inactive together. There are two main differences between word and block interleave. The first is the way the decode is handled to interleave the successive words, and where they are placed. The second difference is the facility in the block interleave mode that allows two pages to be active simultaneously.

Multipage Interleave
Multipage interleave is a combination of page-mode and block interleave. Multipage interleave has the greatest impact on applications that need more than 512K of memory.

Figure 5 shows the block diagram of the Memory Control Logic. It is logically divided into eight sections:

a. Address Decode
b. HIT/MISS Detection
c. RAS/CAS Logic
d. Memory Address Generation
e. Next Address and Ready Logic
f. EMS Memory
g. ROM Data Conversion Logic
h. Parity Logic

a. Address Decode

In addition to shadow and remap decoding, the SL9252 provides all necessary circuitry to decode on-board RAM, ROM, and on-chip I/O. Sixteen memory type and select combinations can be chosen to support one to four banks of DRAM using 256K, 1M, 4M or many combination of these using regular or static column DRAMs. The controller can be configured to support from 512K bytes to 16M bytes. The memory address range for different bank select codes are shown in Table 4. The bank selection code is written to Register 11h (sec VII, p. 51).

For page word interleave, the selection code and size are the same as shown in Table 4 except that the address range of the bank depends on address A2 for 2-way interleave and addresses A2 and A3 for 4-way interleave.

D3	D2	D1	D0	BANK 0	BANK 1	BANK 2	BANK 3	MEMORY SIZE
0	0	0	0	0-512KΔ				512K
0	0	0	1	0-512KΔ	512K-640K/SHDWΔ			1M
0	0	1	0	0-512KΔ	512K-640K/SHDWΔ	1M-1M + 512KΔ		1M + 512K
0	0	1	1	0-512KΔ	512K-640K/SHDWΔ	1M-1M + 512KΔ	1M + 512K-2MΔ	2M
0	1	0	0	0-512KΔ	512K-640K/1M-2M + 512K/SHDW*			2M + 512K
0	1	0	1	RESERVED				
0	1	1	0	0-512KΔ	512K-640K/SHDWΔ	1M-3M *		3M
0	1	1	1	0-512KΔ	512K-640K/SHDWΔ	1M-3M*	3M-5M*	5M
1	0	0	0	0-640K/1M-8M/SHDW†				8M
1	0	0	1	0-640K/1M-8M/SHDW†	8M-16M†			16M
1	0	1	0	RESERVED				
1	0	1	1	RESERVED				
1	1	0	0	0-640K/2M-4M/SHDW				2M
1	1	0	1	0-640K/2M-4M/SHDW	2M-4M*			4M
1	1	1	0	0-640K/2M-4M/SHDW	2M-4M*	4M-6M*		6M
1	1	1	1	0-640K/2M-4M/SHDW	2M-4M*	4M-6M*	6M-8M*	8M

Δ(256Kx2) *(1Mx2) †(4Mx2)

Table 4 Bank Select Codes and Memory Address Range

`SHDW' depicts to the 384K memory available from 640K to 1M. This area corresponds to the shadow address range or remap range. The shadow address range is decoded based on the bits set in Registers 00h to 07h (sec VII, pp. 37-41) and the remap decoding is based on Register 09h (sec VII, pp. 43) setting. Remap RAM address is always above the maximum DRAM memory (top of memory) specified in Table 4 for the selected memory select code. The programmer should make sure two or more address ranges do not overlap to the same physical area.

On reset, ROM is decoded from FE0000h to FFFFFFh and from 0F0000 to 0FFFFF. The second area can be disabled by resetting bits 0 and 1 in ROM control register 0Ch. Local ROM can be decoded from 0C0000 to 0EFFFF in 16k granularity by setting the control bits in ROM control register 0Ah and 0Bh. For the selected address range NROMOE is asserted active low.

b. Hit/Miss Detection

After reset and after every HLDA cycle, the first access to memory is treated as a MISS cycle asserting RAS and CAS as programmed in registers 0Dh, 0Eh, 0Fh, and 13h. The page number is stored internally in a page register, and at the end of the cycle RAS is left low and CAS returned high. During all subsequent accesses, the access page number is compared with the stored page number and a HIT is detected if they are same. If a mismatch (MISS) is detected, RAS is negated and asserted again after the programmed number of clocks for RAS precharge. The new page number is stored for subsequent cycle comparisons. For word page interleave on a MISS, all bank RASes are negated and asserted together. For multiple page interleave only the bank for which there is a MISS will have its RAS negated. Thus, in multi-page interleave different banks can have different active pages. In non-page mode, each access is treated as a MISS cycle.

c. RAS/CAS Logic

On-board memory timing is programmable as a multiple of CLK2. This gives great flexibility in matching DRAM specifications to the CPU speed for optimal performance and cost. Four configuration registers are used for programming RAS and CAS precharge and RAS to column address delay. These values can be different for HIT and MISS cycles and for read and write cycles. CAS is negated for every cycle and asserted after the specified number of CLK2's. RAS is negated for a MISS cycle and asserted after the specified number of CLK2's. The RAS and CAS access times are provided by programming the number of wait states correctly. The programmed values affect only CPU accesses. DMA, REFRESH and MASTER timings are fixed as shown in the timing diagrams in Section VIII. During refresh cycles, support for one or two CLK2 staggered refreshing is provided. During staggered refreshing, Bank 0 RAS is asserted first and Bank 3 RAS is asserted last.

RAS timeout logic may be optionally enabled by setting bit 5 in register 10h to ensure that the RAS active time limit is not violated during page mode operation. If RAS remains active for a period greater than the selected period, RAS is negated during the next CPU access. The cycle is treated as a MISS cycle even if the access is to the same page.

d. Memory Address Generation

The SL9252 provides the necessary circuitry to multiplex the access address as a row address and a column address. During refresh, the internal refresh counter output is read as a raw address. The physical address used for row and column depends on the memory size and mode of operation. Table 5 provides the address generation states. Row address hold time (RAS to column address) can be programmed through Register 0Dh (sec VII, p. 47).

MODE	MEMORY		MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8	MA9	MA10
NON-INTERLEAVE	256K	ROW	11	12	13	14	15	16	17	18	10		
		COL	1	2	3	4	5	6	7	8	9		
	1M	ROW	11	12	13	14	15	16	17	18	19	20	
		COL	1	2	3	4	5	6	7	8	9	10	
	4M	ROW	21	12	13	14	15	16	17	18	19	20	22
		COL	1	2	3	4	5	6	7	8	9	10	11
2-WAY INTERLEAVE	256K	ROW	11	12	13	14	15	16	17	18	19		
		COL	10	2	3	4	5	6	7	8	9		
	1M	ROW	21	12	13	14	15	16	17	18	19	20	
		COL	11	2	3	4	5	6	7	8	9	10	
	4M	ROW	21	22	13	14	15	16	17	18	19	20	23
		COL	11	2	3	4	5	6	7	8	9	10	12
4-WAY INTERLEAVE	256K	ROW	20	12	13	14	15	16	17	18	19		
		COL	10	11	3	4	5	6	7	8	9		
	1M	ROW	21	22	13	14	15	16	17	18	19	20	
		COL	11	12	3	4	5	6	7	8	9	10	
2-WAY BLOCK INTERLEAVE	256K	ROW	11	12	13	14	15	16	17	18	19		
		COL	1	2	3	4	5	6	7	8	9		
	1M	ROW	21	12	13	14	15	16	17	18	19	20	
		COL	1	2	3	4	5	6	7	8	9	10	
	4M	ROW	21	22	13	14	15	16	17	18	19	20	23
		COL	1	2	3	4	5	6	7	8	9	10	11
4-WAY BLOCK INTERLEAVE	256K	ROW	20	12	13	14	15	16	17	18	19		
		COL	1	2	3	4	5	6	7	8	9		
	1M	ROW	21	22	13	14	15	16	17	18	19	20	
		COL	1	2	3	4	5	6	7	8	9	10	

Note: Polarity of MA address bits is not reflected in above table.

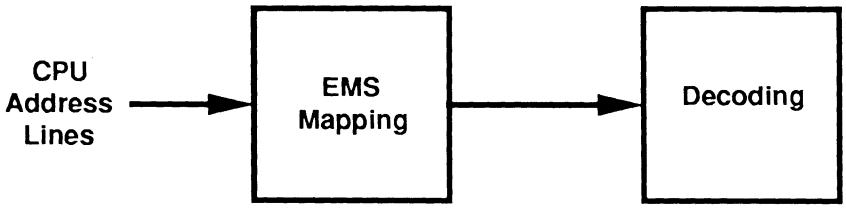
TABLE 5 Address Generation

e. Next Address and Ready Logic

The SL9252 provides logic for pipeline mode and non-pipeline mode CPU operation. Setting bit 3 in register 12h disables pipeline operation. In pipeline mode, the next address to the CPU is asserted for on-board DRAM accesses before ready is asserted. For the same number of wait states the ready for non-pipeline operation will be one CPUCLK earlier than in pipeline operation. The number of wait states for HIT and MISS can be programmed separately. In addition, the wait state generation for write cycles can be one less than the read. Next address is not asserted for ROM on-chip I/O and bus accesses.

f. EMS Memory

The SL9252 has the capability for mapping up to four 16K blocks of memory (starting on a 64K boundary below 1MB) to any 16K boundary.



The SL9252 contains an EMS Control Register (see VII, p. 61) which is an 8-bit register used to perform the following functions:

EMSCTLREG , Index 1Ch	
Bit	Function
0-3	Set Base Address in bottom 1M
4	Enable/Disable EMS Mapping
5	EMS I/O Address Select
6	EMS I/O Enable
7	EMS Wait State Select

TABLE 6 Address Generation

The page register base address must occur on a 64K boundary. The following example illustrates the four page registers located at a base address of 896K.

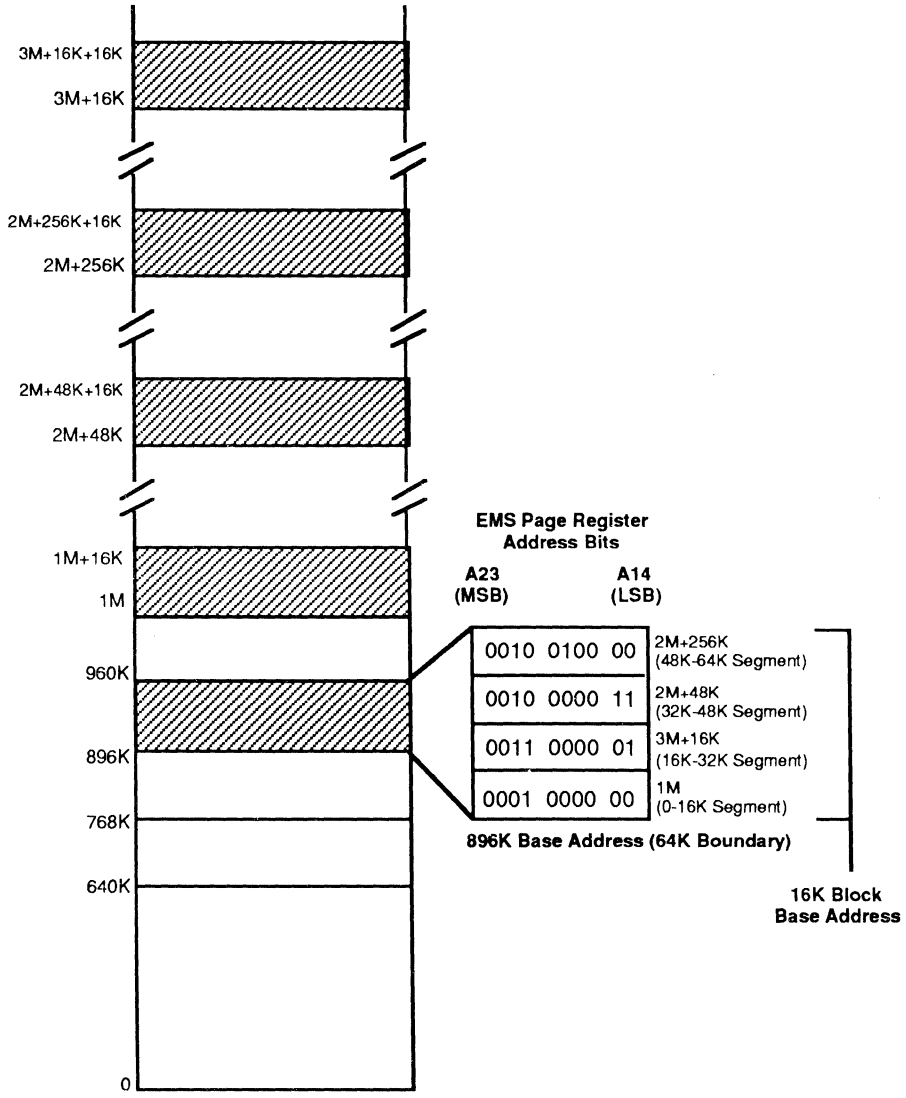


Fig. 6 EMS Page Registers

Note the four page registers each contain the base addresses for the four 16K blocks of EMS memory. Each of these four page registers is associated with one of two I/O port addresses determined by Bit 5 of the EMS Control Register (1Ch), as described in the table below:

EMS Page Register	I/O Addresses		EMS Memory Block
	Bit 5=0	Bit 5=1	
00	0208	0218	0-16K
01	4208	4218	16K-32K
10	8208	8218	32K-48K
11	C208	C218	48K-64K

Table 7 EMS Register Configuration

The address examples in the above figure illustrate how EMS memory is mapped above 1MB. Each register contains the base address for a particular 16K block of EMS memory that is located above 1MB.

In mapping the CPU physical address to the EMS memory address, Bits A15 and A14 are used to select one of the four page registers. Bits A19 through A16 select the base address for the page registers in the lowest 1MB of memory (i.e., 896K). The following diagram describes the base address for EMS mapping registers:

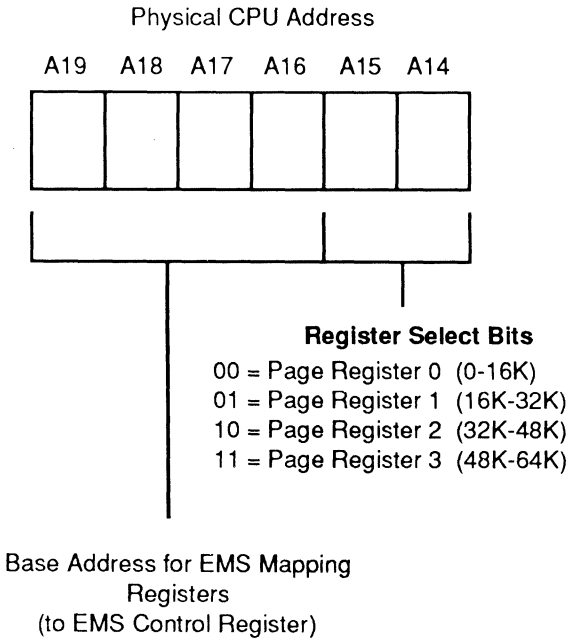


Fig. 7 EMS Memory Mapping

To program EMS Page Registers:

```
MOV   AX,   0122        ;     Set D5 = 1, Reg 0122, Index 17h
MOV   DX,   AX
MOV   AX,   0177
OUT   DX,   AX
MOV   AX,   0200
OUT   DX,   AX

MOV   AX,   001C        ;     Intialize EMSCTRLREG
OUT   DX,   AX
MOV   AX,   005E
OUT   DX,   AX

MOV   DX,   0208        ;     Write to Page Reg 1
MOV   AX,   0040
OUT   DX,   AX

MOV   DX,   4208        ;     Write to Page Reg 2
MOV   AX,   00C1
OUT   DX,   AX

MOV   DX,   8208        ;     Write to Page Reg 3
MOV   AX,   0083
OUT   DX,   AX

MOV   DX,   C208        ;     Write to Page Reg 4
MOV   AX,   0090
OUT   DX,   AX

MOV   AX,   0122        ;     Reset D5, Reg 0122, Index 17h
MOV   DX,   AX
MOV   AX,   0177
OUT   DX,   AX
MOV   AX,   0
OUT   DX,   AX
.
.
.
```

g. ROM Data Conversion Logic

With the SL9252, the system designer has the flexibility to choose either an 8 bit or 16 bit ROM data path. If NROMOE is pulled low on reset, an 8 bit ROM is assumed and the SL9252 does the necessary data conversion cycles for ROM accesses. During word access to ROM the low byte is accessed first (SA0 = 0) and latched. SA0 is then toggled to 1 and high byte is accessed. Ready to CPU is issued after the specified number of wait states for the second access. The first access also assumes the same number of wait states.

h. Parity Logic

The figure below shows the parity generation and checking logic. For memory writes, PTY0 is generated for D0-D7 (low byte) and PTY1 is generated for D8-D15 (high byte). If PORTBEN (PORT 61 bit) and VIA Parity Enable (VIAPYEN, Register 17h, bit 3) are set, an NMI will be generated for a read parity error.

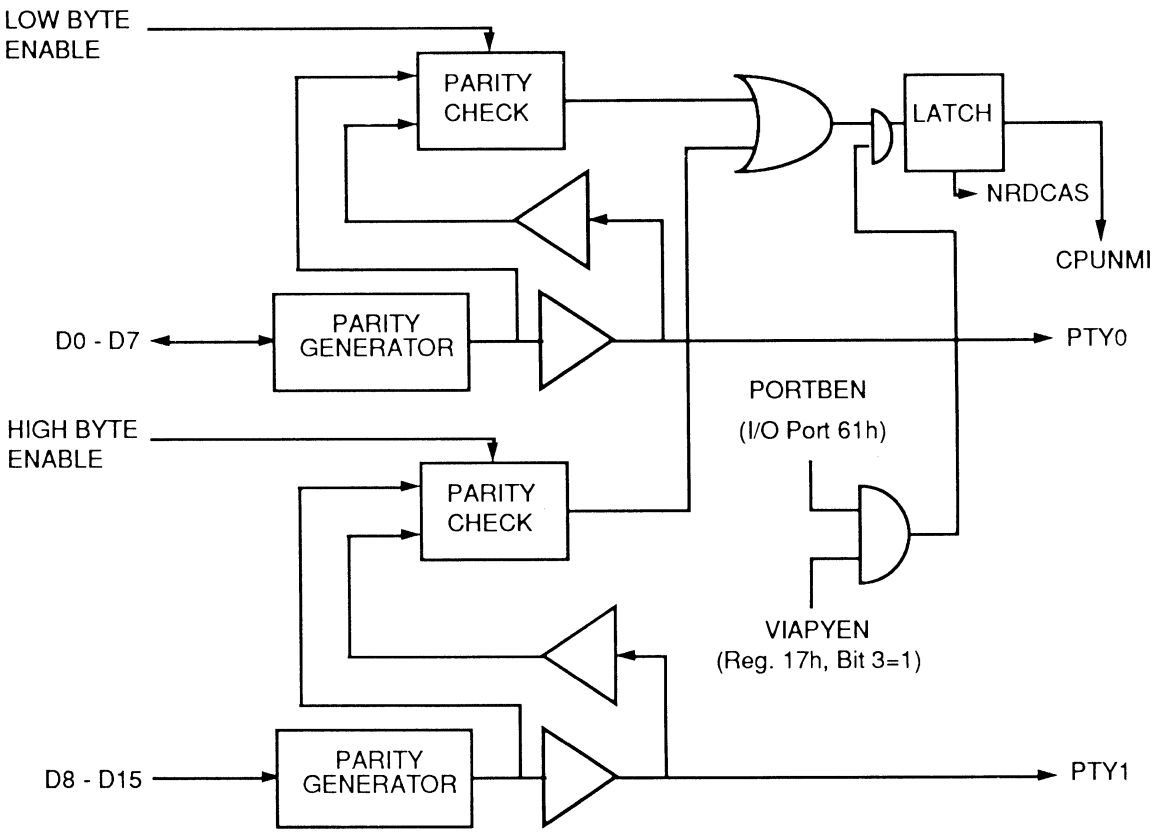
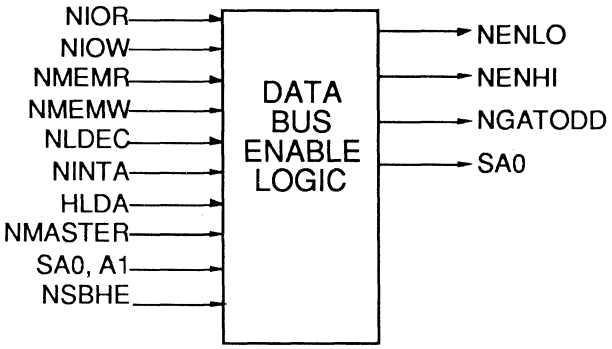
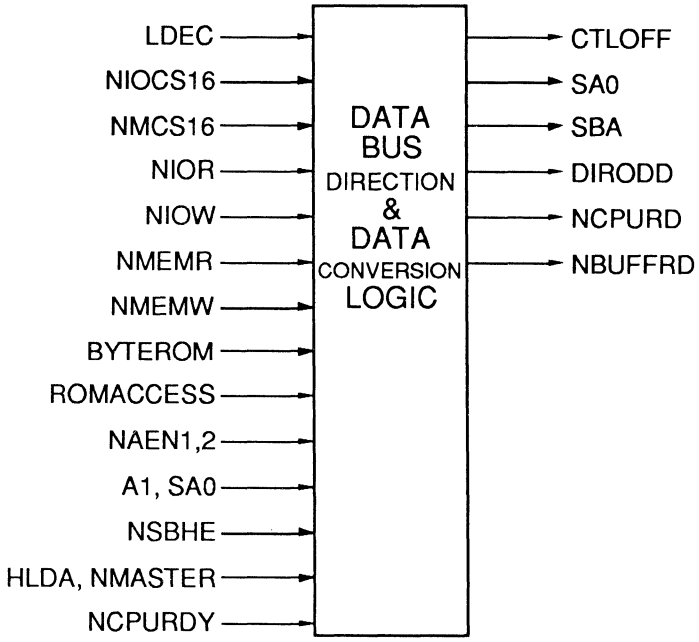


Fig. 8 Parity Internal Logic Diagram





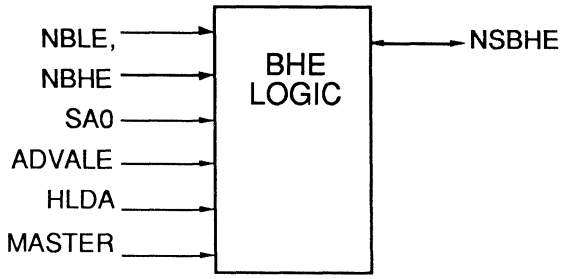


Fig. 9 SL9252 Data Control Internal Logic Block Diagram

V. DATA CONTROL LOGIC

Figure 9 shows the block diagram of the Data Control Logic. The three major blocks are:

a. Bus Enable Logic
b. Bus Direction and Data Conversion Logic
c. High Byte Enable Logic

a. Bus Enable Logic

The SL9252 provides logic support for use of an external SL9020 Data Controller, or TTL buffers and latches. The SL9252 generates the necessary buffer enable controls for these two modes of operation. Register 19h, bit 0 must be set if the SL9020 Data Controller is used with DRAM and ROM on the MD bus. The following three enable controls are used to enable the buffers between D and SD bus. NENLO and NENHI enable low and high byte respectively. NGATODD enables the swap buffer between SD0-SD7 and SD8-SD15.

b. Bus Direction and Data Conversion Logic

The following signals control direction of the AT bus and peripheral bus data buffers: NCPURD for SD0-SD15 to D0-D15 buffer, DIRODD for the SD0-SD7 to SD8-SD15 swap buffer, and NBUFFRD for XD0-XD7 to SD0-SD7 buffer. NMEMDIR is used to direct data to and from the memory data bus to the DBus when local memory is on MD bus when local memory is on MD bus. Table 8 describes the pin assignments for these signals. The following table lists directions of the data bus signals:

Signal	Direction	
NCPURD	0	SD to D
	1	D to SD
DIRODD	0	SD8-SD15 to SD0-SD7
	1	SD0-SD7 to SD8-SD15
NBUFFRD	0	XD0-XD7 to SD0-SD7
	1	SD0-SD7 to XD0-XD7
NMEMDIR	0	MD to D
	1	D to MD

Table 8 Buffer Direction Control Signals

In addition to these enable and direction controls, the SL9252 provides a clock and select signal for data conversion during word access to a byte port. CTLOFF is used to clock the low byte data, and SBA is used to select the latched data.

c. High Byte Enable Logic

NSBHE is an AT-bus byte high enable signal and is also an input during MASTER mode. It is an output at all other times. During CPU mode, NSBHE is asserted whenever the CPU acceses a high byte. During 8 bit DMA mode, NSBHE is of opposite polarity to SA0 and during 16 bit DMA mode it is low.

VI. PERIPHERAL CONTROL LOGIC

Figure 10 shows the block diagram of Peripheral Control Logic. It provides logic for the following:

a. Peripheral Address Decoding
b. Port B Logic

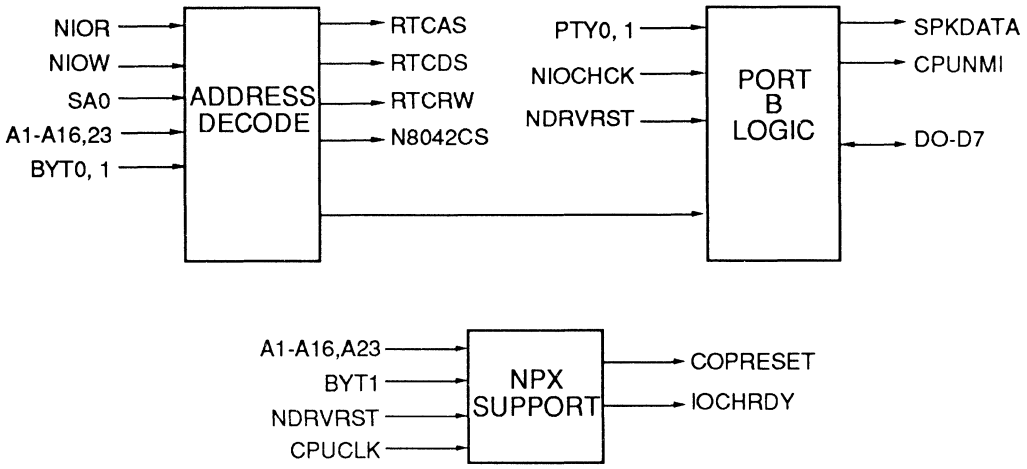


Fig. 10 SL9252 Peripheral Control Internal Logic Block Diagram

a. Peripheral Address Decoding

The SL9252 provides address decoding logic to support the Real Time Clock and Keyboard Controller. The SL9252 is designed to support either the Dallas 1287 Real Time Clock with 64 bytes of CMOS SRAM or the Dallas 1387 Real Time Clock which provides 4K bytes of CMOS SRAM in addition to the standard 64 bytes. Dallas real time clock devices integrate the battery necessary to maintain the data integrity of the CMOS memory. If Bit 0 of Register 17h is reset (RTC1287 mode), then RTCAS, RTCRW and RTCDS are generated for write access to 70h, 71h, and read access to 71h respectively. To increase the amount of CMOS RAM (battery-backed), the RTC1387 mode may be used instead of RTC1287 by setting Bit 0 of Register 17h. In this mode, use external decoders to generate read and write port decoding to interface with RTC1387. If Bit 0 of Register 17h, RTC1387 mode, is set, then write access to 70h and 74h are decoded on RTCAS and RTCRW, respectively. Read and write accesses from 70h to 77h are decoded on RTCDS.

Keyboard controller chip select goes active for port 60h read and write accesses. The number of wait states for these accesses depends on the programmed number of wait states for bus accesses. These devices must be located on XD bus.

b. Port B Logic

SL9252 also provides the port B (address 61h) logic for CPUNMI, Parity Enable, and speaker data.

VII. CONFIGURATION REGISTERS

The SL9252 provides 32 configuration registers for all programmable functions in the device. All of the registers are accessed through an index/data addressing scheme. Only one I/O address is used to access both index and data registers. The address defaults to 0122h after reset and can be remapped to any other unused I/O address (must be on a 16 bit, byte 1 boundary) between 0000h and FFFFh by loading the new I/O address into the relocation registers. The addresses from these registers are transferred to a pipeline register, for comparing, with a write to configuration register 3 (using the unrelocated address i.e., 0122h) with bit 0 = 1. After this the temporary relocation registers are also in the new address space until the reset, when it defaults again to 0122h.

The data registers are selected by writing their addresses in the index register. An internal pointer is used to determine whether the on-chip I/O write is for the index or data registers. After reset, the pointer points to the index register. Any write to the index register or data register will toggle the pointer. Only data registers can be read back and any read to the data registers will leave the pointer pointing to the index register.

The following table lists all the configuration registers by their index address, name and description:

INDEX ADDRESS	NAME	REGISTER
00	SDWREG0	Shadow control 0
01	SDWREG1	Shadow control 1
02	SDWREG2	Shadow control 2
03	SDWREG3	Shadow control 3
04	SDWREG4	Shadow control 4
05	SDWREG5	Shadow control 5
06	SDWREG6	Shadow control 6
07	SDWREG7	Shadow control 7
08	RAMWAIT	RAM wait state select
09	REMAP	Remap
0A	ROMCTL0	Local ROM control register 0
0B	ROMCTL1	Local ROM control register 1
0C	ROMCTL2	Local ROM control register 2
0D	RASTIM	RAS timing register
0E	CASTIM1	CAS timing register 1
0F	CASTIM2	CAS timing register 2
10	DISMEM	Disable to 0K
11	MEMTYPE	Memory type and size select
12	CONFIG1	Configuration register 1
13	CONFIG2	Configuration register 2
14	CONFIG3	Configuration register 3
15	IOMAPLOW	Relocation register low
16	IOMAPHI	Relocation register high
17	CONFIG4	Configuration register 4
18	SYSCTL	System control register
19	WAIT16	System bus 16 bit device wait state select
1A	WAIT8	System bus 8 bit device wait state select
1B	CMDDLY	System bus command delay
1C	EMSCTLREG	EMS Control Register
1D	Reserved	
1E	Reserved	
1F	IDREG	ID Register

Table 9 Configuration Registers

REGISTER BIT(S) DESCRIPTIONS

CONVENTIONS:

The following conventions will be used in register bit(s) descriptions:

[]	Brackets denote bit fields that are affected. Example: [7,5] denotes bits 7 and 5 are referenced.
..	Two dots (..) indicates that the bits referenced are inclusive. Example: [7..5] indicates bits 7, 6 and 5 are referenced.
R	Read only bit(s). The value depends on the mode of operation. Example: R[7] indicates that bit 7 is read only.
R0	Indicates bit or bit field is read only and reads 0 when accessed. Software should set these bit(s) to zero. Example: [7..5] R0 indicates bits seven through five inclusive are read only bits. When accessed these bits will read zero.
R1	Indicates bit or bit field is read only and reads 1 when accessed. Software should set these bit(s) to zero. Example: [7..5] R1 indicates bits seven through five inclusive are read only bits. When accessed these bits will read one.
W1	Write only bit(s). Bit(s) may be written, but when accessed will always read as one.
R/W	Read/Write bit(s). Bit may be written any value. When accessed the bit(s) will read the value previously written.
rsvd	Reserved. This bit(s) is reserved by VIA for future use.

REGISTER NAME, INDEX #

D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R/W	R/W	R/W	R/W	R/W	R/W
>			Bit Names				<
1	1	0	0	0	0	0	0

The top row indicates the bit position.
The second row indicates the bit type; e.g., read only, write only.
The third row indicates the bit(s) name, if any.
The bottom row indicates the default values after reset.

SHADOW CONTROL REGISTERS

Index address (hex) : 00 to 07

These 8 registers control the use of 640K - 1M byte in 16K granularity. All are read/write registers. The most significant 2 bits always read back as ones. Two bits control one 16K region as defined below.

SDWRx	SDWWx	Function
0	0	Read/Write to system bus
0	1	Read system bus, write local DRAM
1	0	Read local DRAM, write system bus.
1	1	Read/Write local DRAM

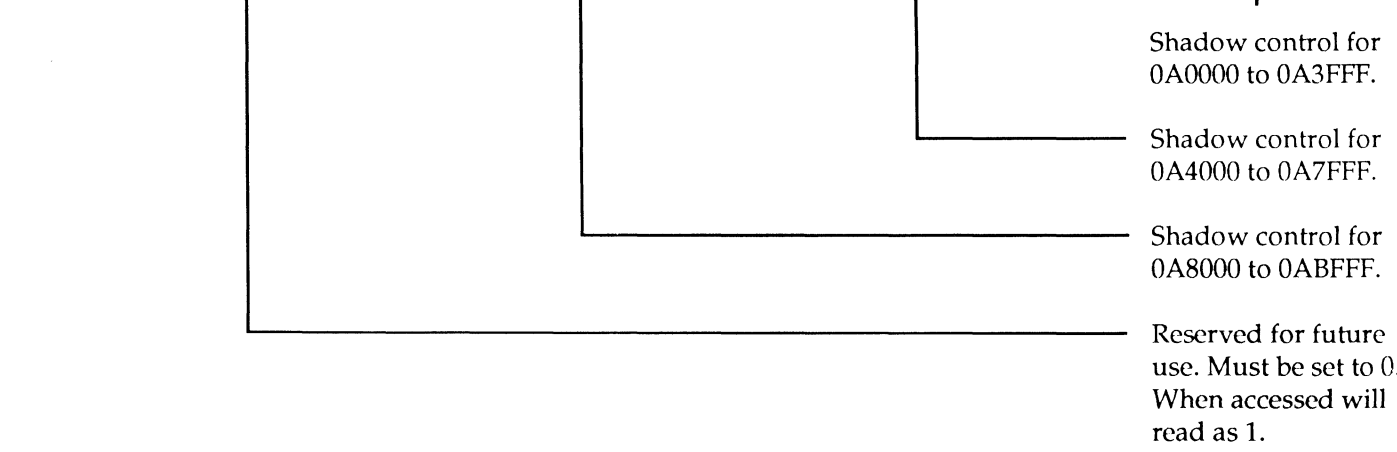
(x : 00h to 17h)

Note: Local ROM is decoded from 0F0000 to 0FFFFF after reset. Local ROM should be disabled through ROM control register for shadowing ROM.

SHADOW CONTROL REGISTER 0, INDEX 00h, R/W

SDWREG0, Register 00h

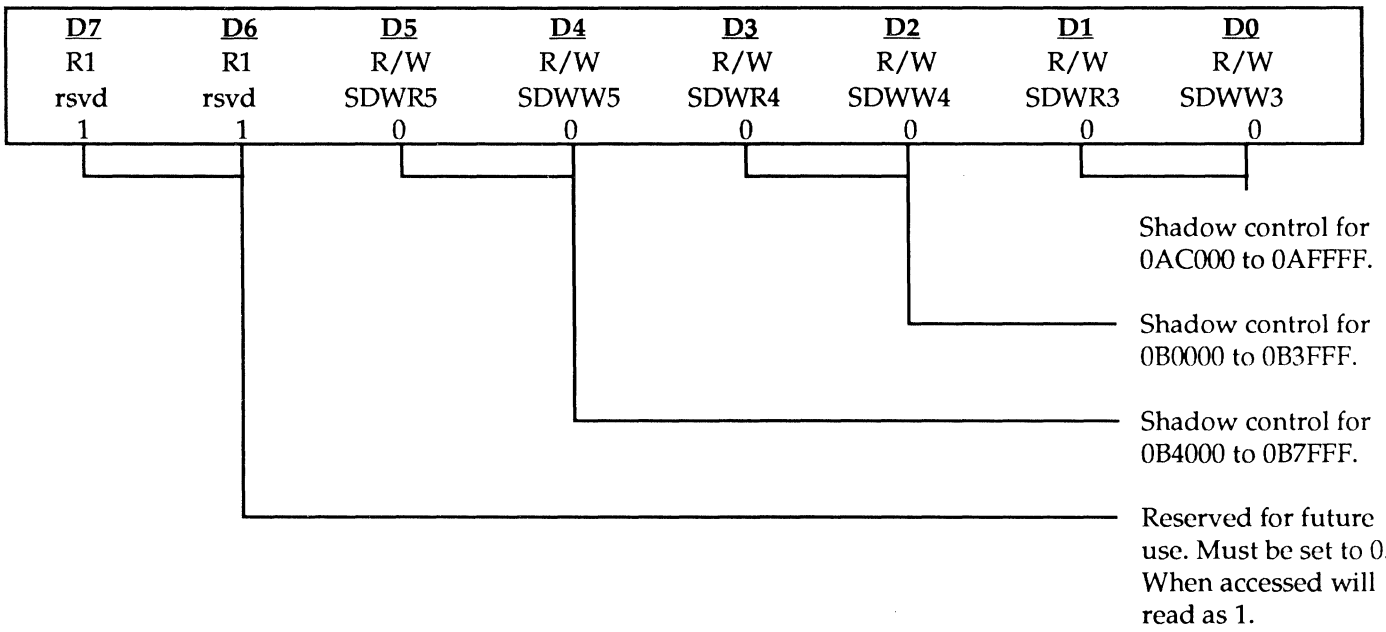
D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R/W	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	SDWR2	SDWW2	SDWR1	SDWW1	SDWR0	SDWW0
1	1	0	0	0	0	0	0



SHADOW CONTROL REGISTER 1, INDEX 01h, R/W

SDWREG1, Register 01h

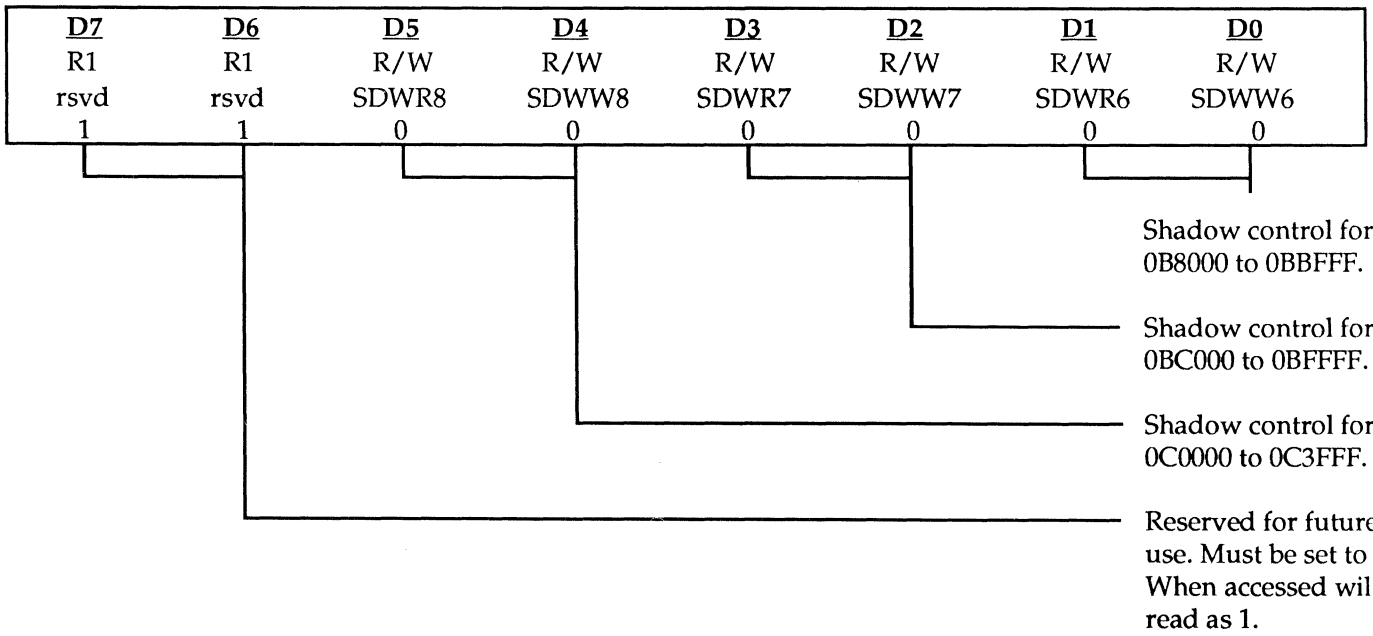
D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R/W	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	SDWR5	SDWW5	SDWR4	SDWW4	SDWR3	SDWW3
1	1	0	0	0	0	0	0



SHADOW CONTROL REGISTER 2, INDEX 02h, R/W

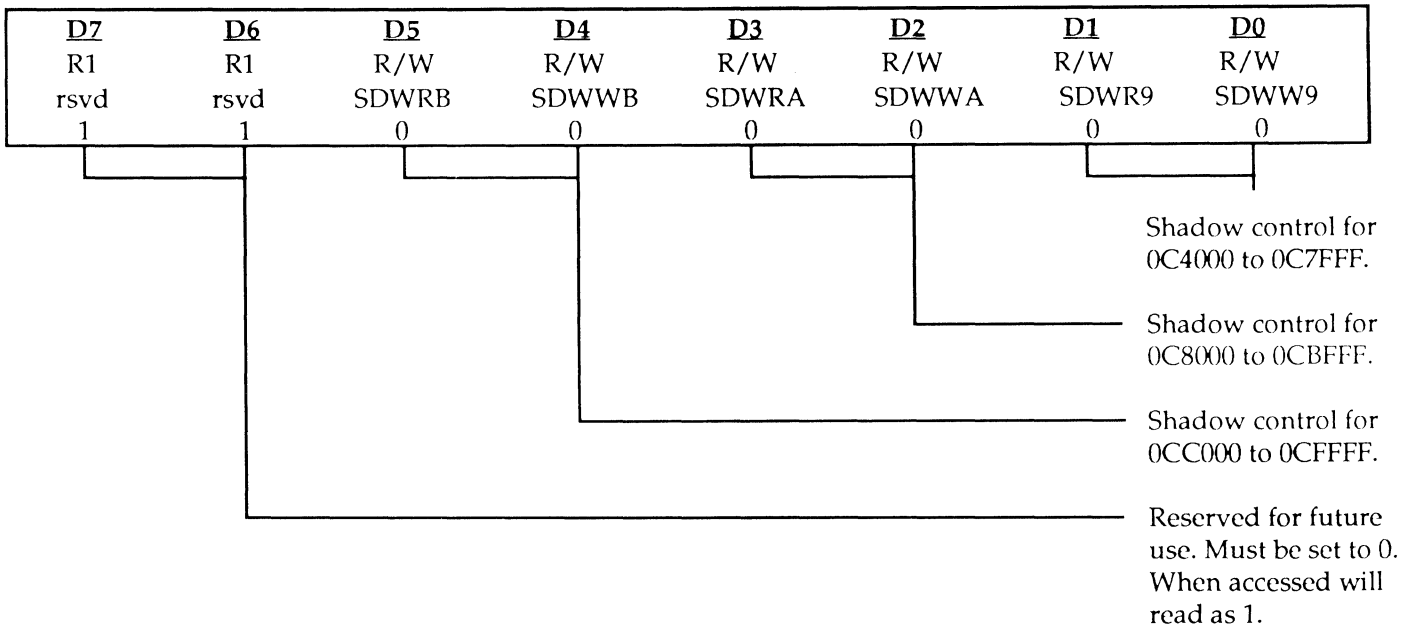
SDWREG2, Register 02h

D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R/W	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	SDWR8	SDWW8	SDWR7	SDWW7	SDWR6	SDWW6
1	1	0	0	0	0	0	0



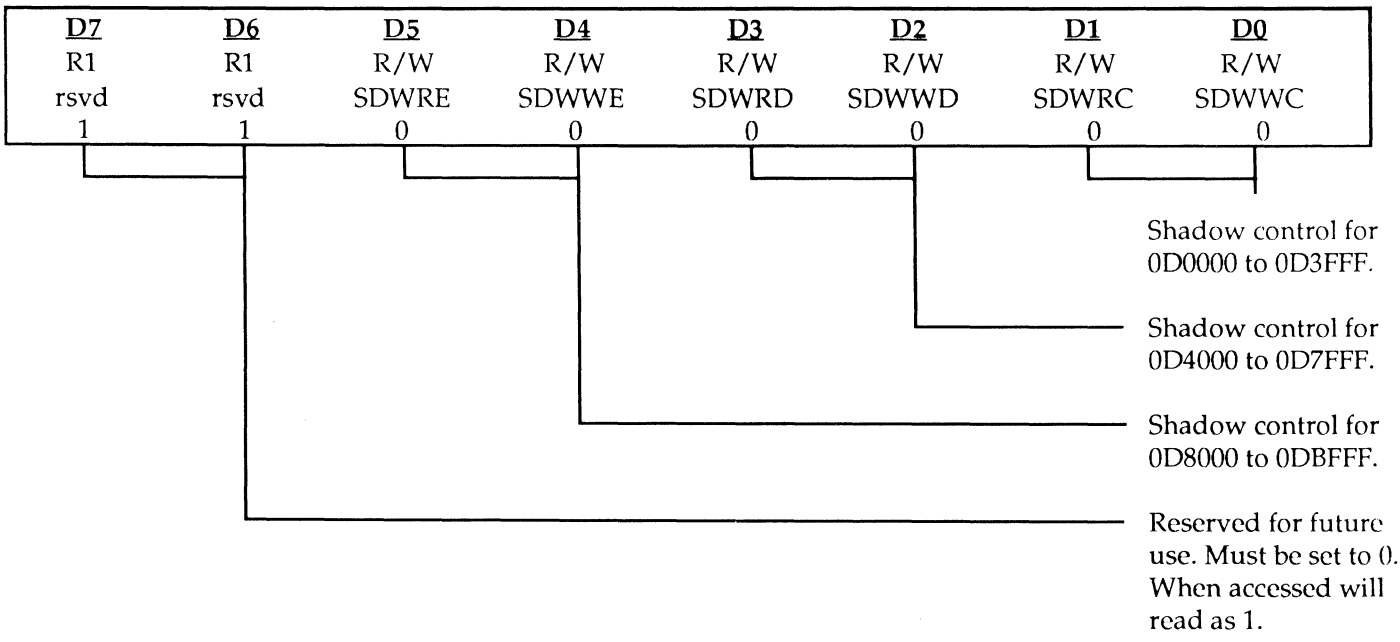
SHADOW CONTROL REGISTER 3, INDEX 03h, R/W

SDWREG3, Register 03h



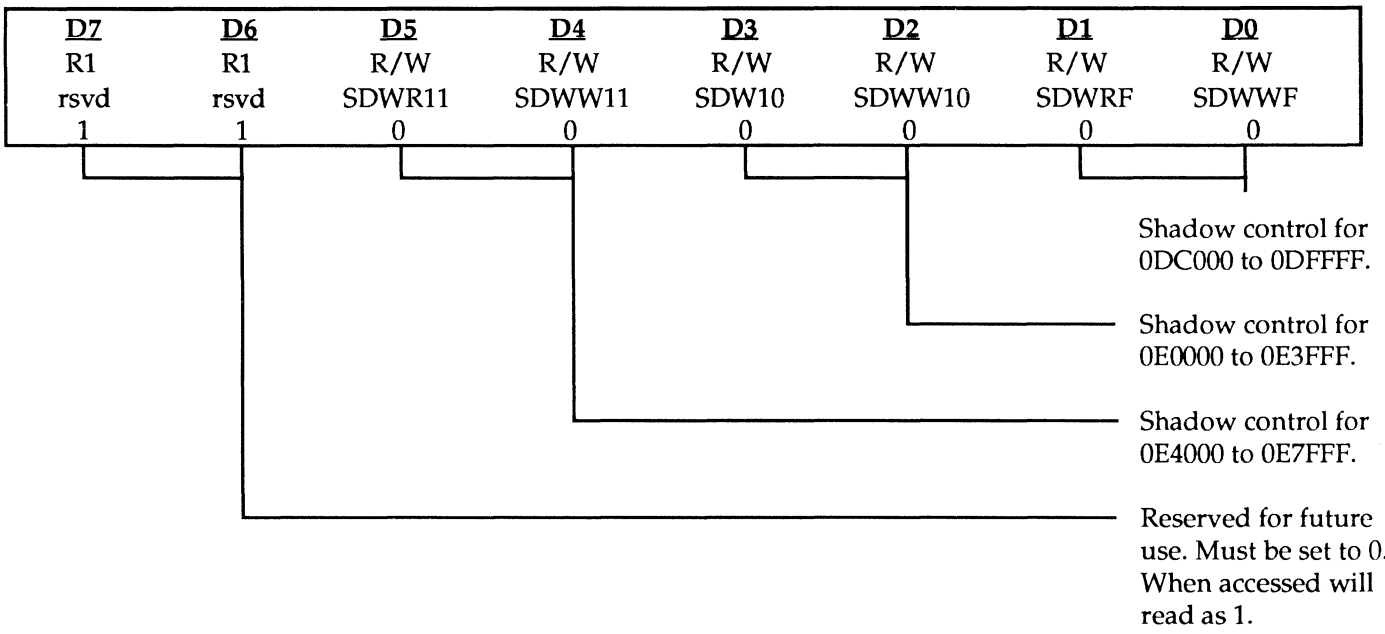
SHADOW CONTROL REGISTER 4, INDEX 04h, R/W

SDWREG4, Register 04h



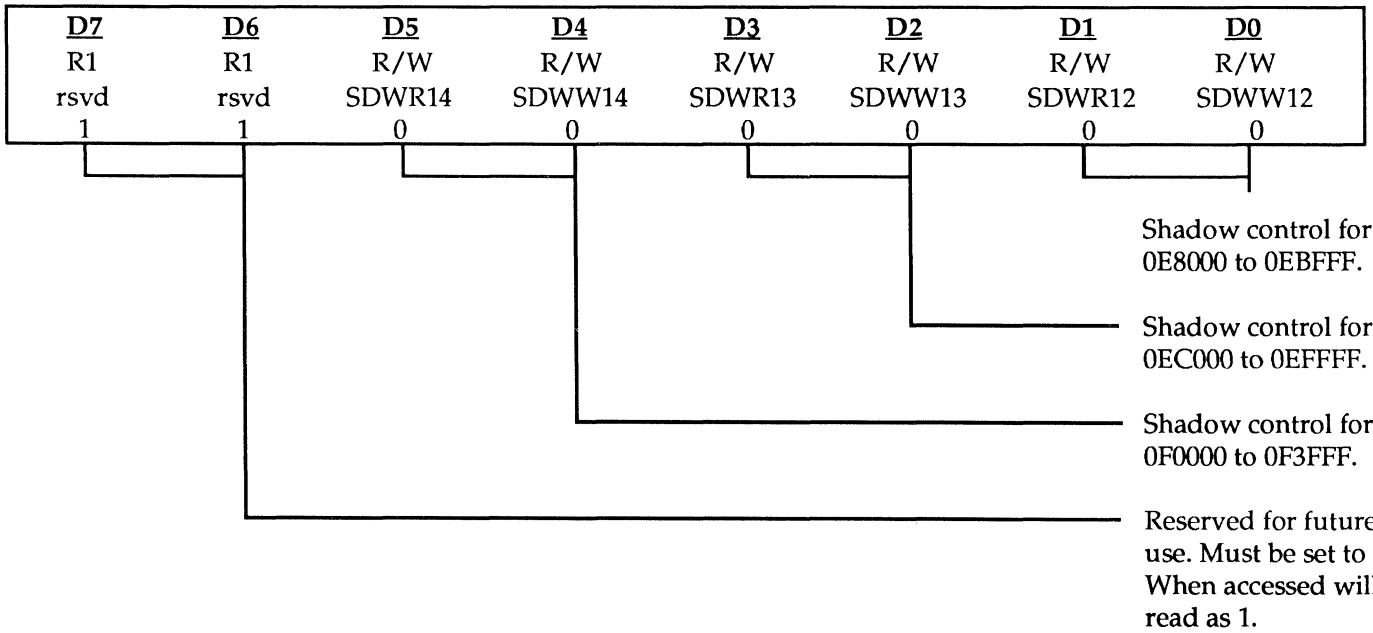
SHADOW CONTROL REGISTER 5, INDEX 05h, R/W

SDWREG5, Register 05h



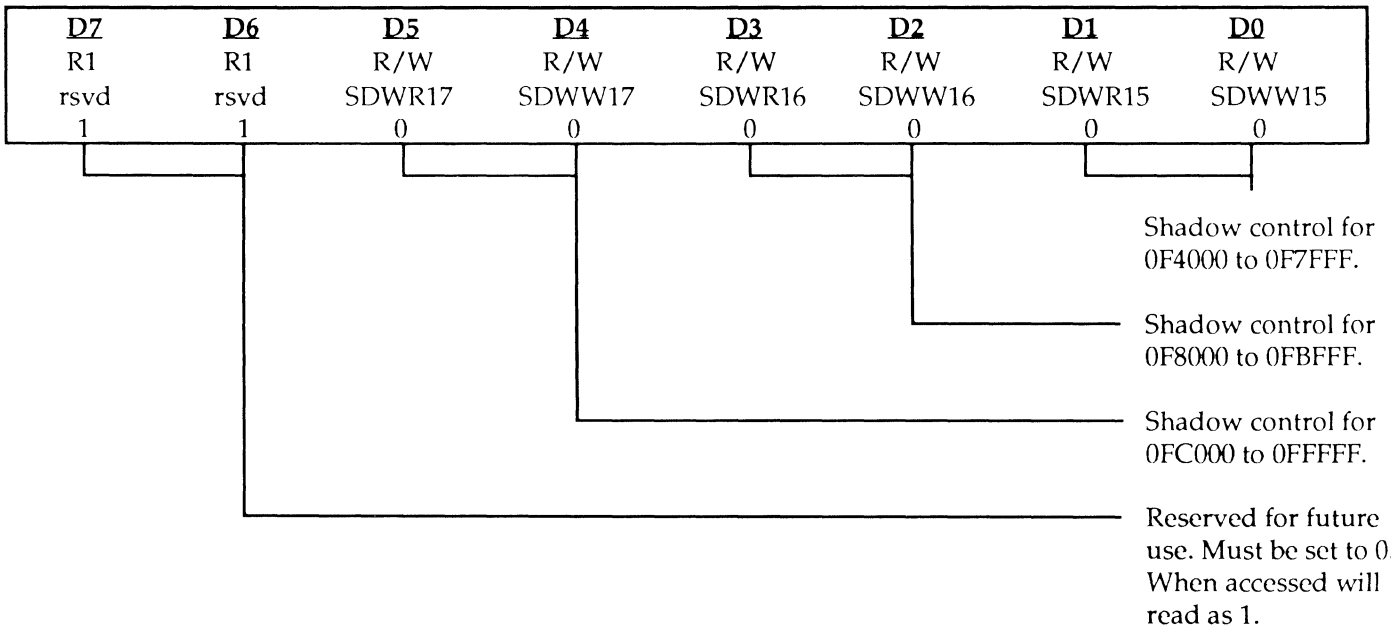
SHADOW CONTROL REGISTER 6, INDEX 06h, R/W

SDWREG6, Register 06h



SHADOW CONTROL REGISTER 7, INDEX 07h, R/W

SDWREG7, Register 07h



RAM WAIT STATE REGISTER, INDEX 08h

RAMWAIT, Register 08h

D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R/W	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	RDMSWT1	RDMSWT0	WRMSWT1	WRMSWT0	HITWTB1	HITWTB0
1	0	0	0	0	0	0	0

Wait states for page HIT

D1	D0	cycles
0	0	0
0	1	1
1	0	2
1	1	3

Wait states for MISS write cycles

D3	D2	
0	0	1
0	1	2
1	0	3
1	1	4

Wait states for MISS read cycles

D5	D4	
0	0	1
0	1	2
1	0	3
1	1	4

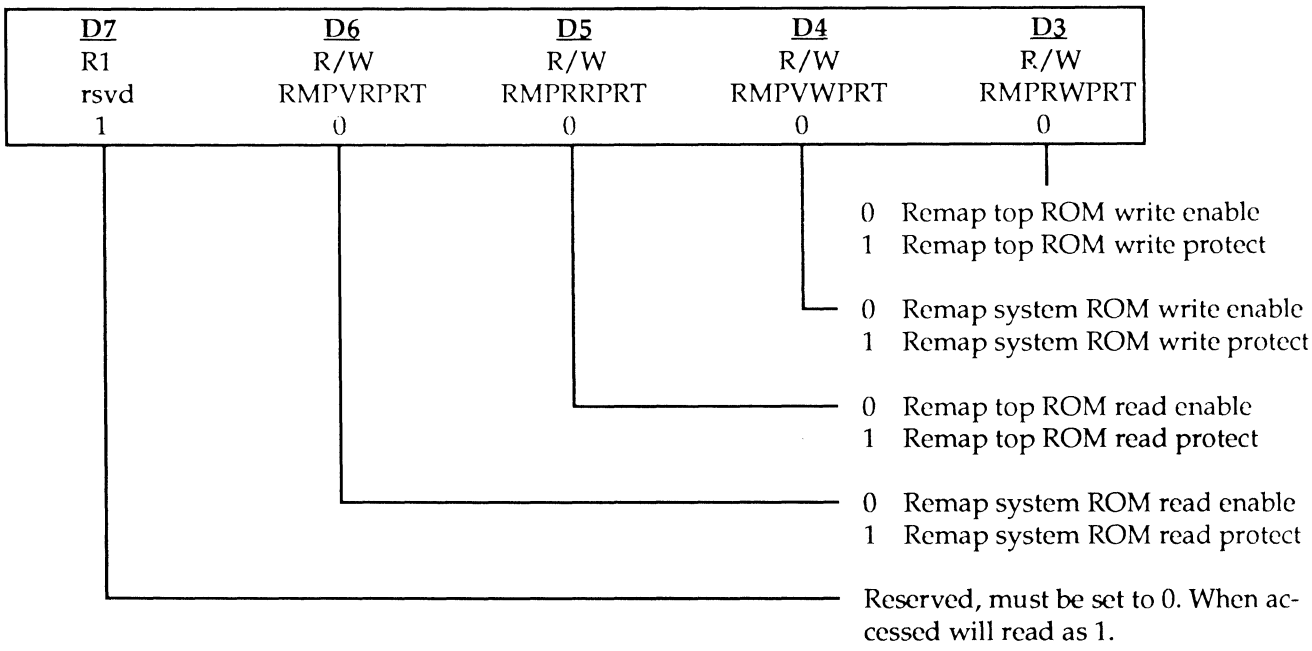
Reserved for future use. Must be set to 0. When accessed will read as 0.

Reserved for future use. Must be set to 0. When accessed will read as 1.

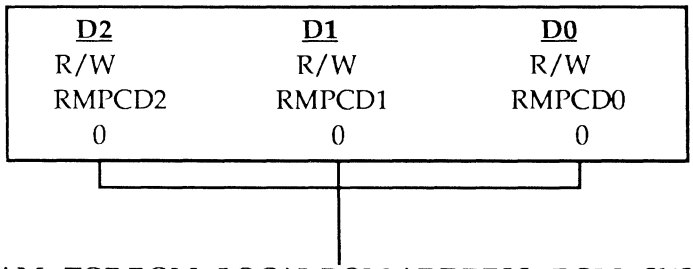
REMAP REGISTER, INDEX 09h, R/W

Remap top RAM, local ROM and System ROM.

REMAP, Register 09h



REMAP, Register 09h



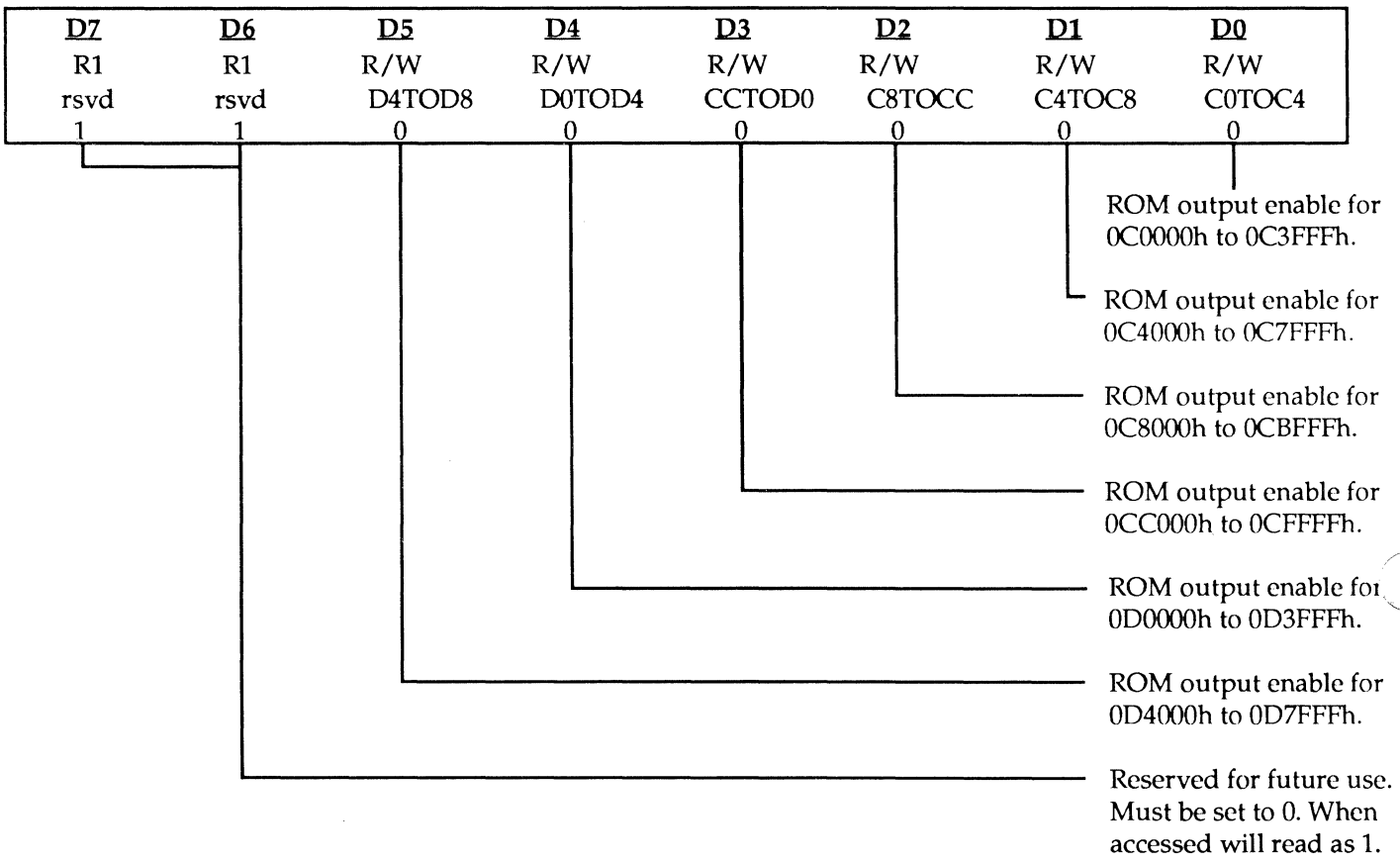
D2	D1	D0	TOP RAM	TOP ROM	LOCAL ROM ADDRESS	ROM	SYSTEM ROM ADDRESS
0	0	0	0	0K	0K		
0	0	1	512K	0K	0K		
*0	1	0	128K	128K	(0E0000 - 0FFFFF)	128K	(0C0000 - 0DFFFF)
0	1	1	256K	128K	(0E0000 - 0FFFFF)	0K	
*1	0	0	288K	64K	(0F0000 - 0FFFFF)	32K	(0C0000 - 0C3FFF)
1	0	1	320K	64K	(0F0000 - 0FFFFF)	0K	
1	1	0	352K	32K	(0F8000 - 0FFFFF)	0K	
1	1	1	384K	0K		0K	

*Note: Remap options are not valid for memory type 2 and 4.

ROM CONTROL REGISTER 0, INDEX 0Ah, R/W

For each bit in this register, 0 is disable and 1 is enable.

ROMCTL0, Register 0Ah

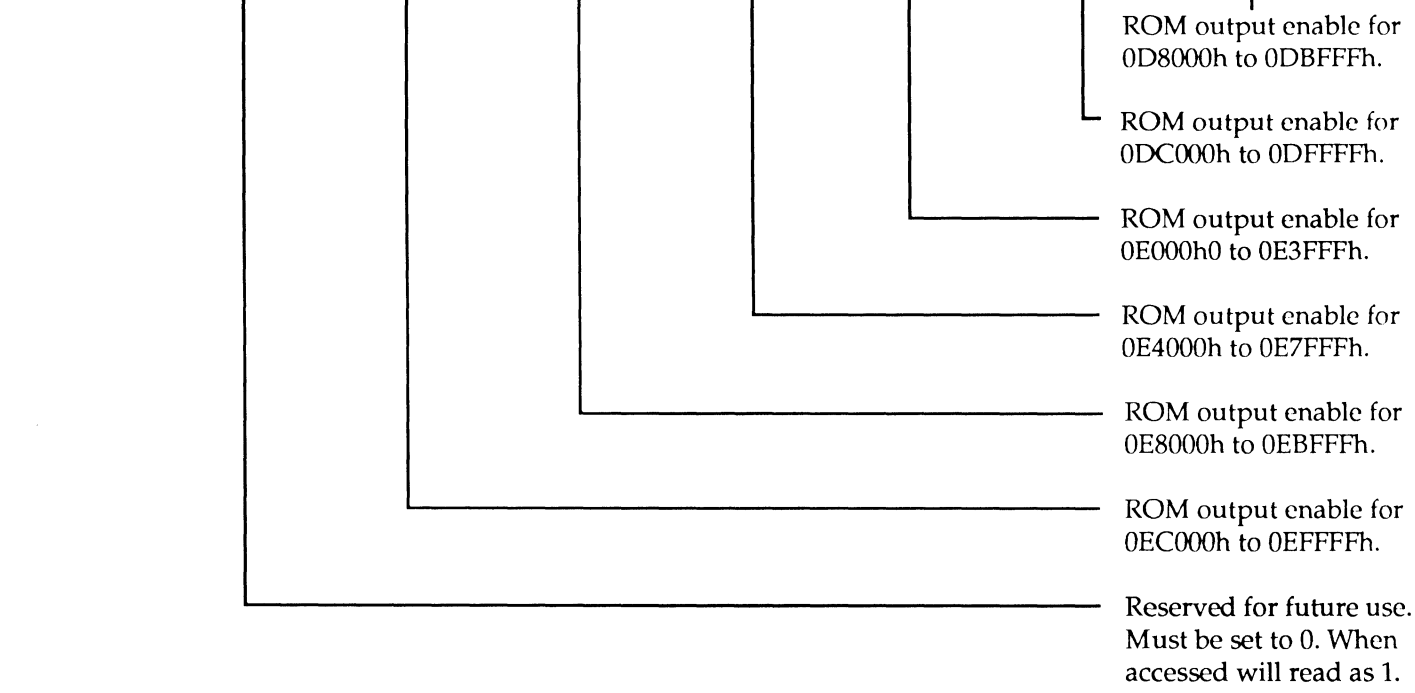


ROM CONTROL REGISTER 1, INDEX 0Bh, R/W

For each bit in this register, 0 is disable and 1 is enable.

ROMCTL1, Register 0Bh

D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R/W	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	ECTOFO	E8TOEC	E4TOE8	E0TOE4	DCTOE0	D8TODC
1	1	0	0	0	0	0	0



ROM CONTROL REGISTER 2, INDEX 0Ch, R/W

For bit 0 and 1 in this register, 0 is disable and 1 is enable.

ROMCTL2, Register 0Ch

D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R0	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	rsvd	PRMSW2	PRMSW1	PRMSW0	F8TOFF	F0TOF8
1	1	0	1	1	1	1	1

0 ROM output disable for 0F0000h to 0F7FFFh.
1 ROM output enable for 0F0000h to 0F7FFFh.

0 ROM output disable for 0F8000h to 0FFFFFh.
1 ROM output enable for 0F8000h to 0FFFFFh.

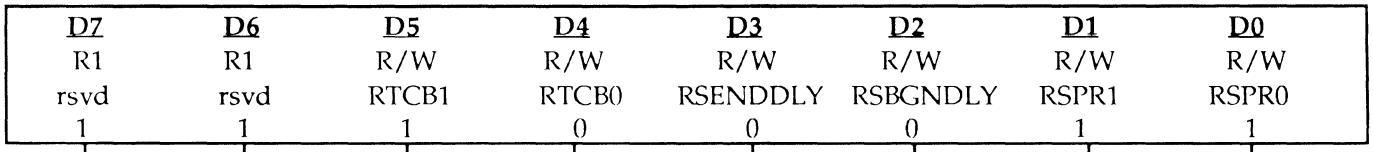
D4	D3	D2	ROM Wait State Select
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	6
1	1	0	8
1	1	1	10

Reserved for future use. Must be set to 0. When accessed will read as 0.

Reserved for future use. Must be set to 0. When accessed will read as 1.

RAS TIMING REGISTER, INDEX 0Dh, R/W

RASTIM, Register 0Dh



D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R/W	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	RTCB1	RTCB0	RSENDDLY	RSBGNDLY	RSPR1	RSPR0
1	1	1	0	0	0	1	1

RAS Precharge

D1	D0	CLK2 cycles
0	0	2
0	1	3
1	0	4
1	1	5

0= RAS assertion as defined by bits RSPR1 - RSPR0
1= RAS assertion as defined by bits RSPR1 - RSPR0 delayed by half CLK2 cycle.

0= RAS negation on T2 beginning.
1= RAS negation delayed by half CLK2 cycle.

RAS to Column

D5	D4	Address Delay
0	0	Fast mode (10ns)
0	1	1/2 CLK2
1	0	1 CLK2
1	1	1 1/2 CLK2

Reserved for future use. Must be set to 0. When accessed will read as 1.

CAS TIMING REGISTER 1, INDEX 0Eh, R/W

CASTIM1, Register 0Eh

D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R/W	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	MSWRCSB2	MSWRCSB1	MSWRCSB0	MSRDCSB2	MSRDCSB1	MSRDCSB0
1	1	1	1	0	1	1	1

CAS start delay for MISS read cycles from T2 beginning (1 - 8 CLK2)

Bits 2-0 are coded in multiples of CLK2 cycles as shown below

D2	D1	D0	Multiple
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

CAS start delay for MISS write cycles from T2 beginning (1 - 8 CLK2)

Bits 5-3 are coded in multiples of CLK2 cycles as shown below

D5	D4	D3	Multiple
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Reserved for future use. Must be set to 0. When accessed will read as 1.

CAS TIMING REGISTER 2, INDEX 0Fh, R/W

CASTIM2, Register 0Fh

D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R/W	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	CSENDDLY	HTWRCSB1	HTWRCSB0	HTRDCSB2	HTRDCSB1	HTRDCSB0
1	1	0	0	1	0	0	1

CAS start delay for HIT read cycles from T2 beginning (1 - 8 CLK2).

Bits 2 - 0 are coded in multiples of CLK2 cycles as shown below.

D2	D1	D0	Multiple
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

CAS start delay for HIT write cycles (0-3 CLK2).

D4	D3	Start Delay
0	0	0
0	1	1
1	0	2
1	1	3

CSENDDLY CAS 1
1 = negation delayed by half CLK2
0 = No delay

Reserved for future use. Must be set to 0. When accessed will read as 1.

DISABLE MEMORY REGISTER, INDEX 10h, R/W

DISMEM, Register 10h

D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R/W	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	ENRSLMT	DI512	DI384	DI256	DI128	DI0
1	1	0	0	0	0	0	0

D0=0 Enable local DRAM from 0K to 128K .
D0=1 Disable local DRAM from 0K to 128K.

D1=0 Enable local DRAM from 128K to 256K.
D1=1 Disable local DRAM from 128K to 256K.

D2=0 Enable local DRAM from 256K to 384K.
D2=1 Disable local DRAM from 256K to 384K

D3=0 Enable local DRAM from 384K to 512K.
D3=1 Disable local DRAM from 384K to 512K.

D4=0 Enable local DRAM from 512K to 640K.
D4=1 Disable local DRAM from 512K to 640K.

D5=0 Disable RAS timeout.
D5=1 Enable RAS timeout.

Reserved for future use. Must be set to 0. When accessed will read as 1.

MEMORY TYPE REGISTER, INDEX 11h, R/W

MEMTYPE, Register 11h

D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R/W	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	rsvd	rsvd	>	Memory Type/Bank Selects		<
1	1	0	0	0	0	0	0

Define the type of memory devices to be used for each of four banks:

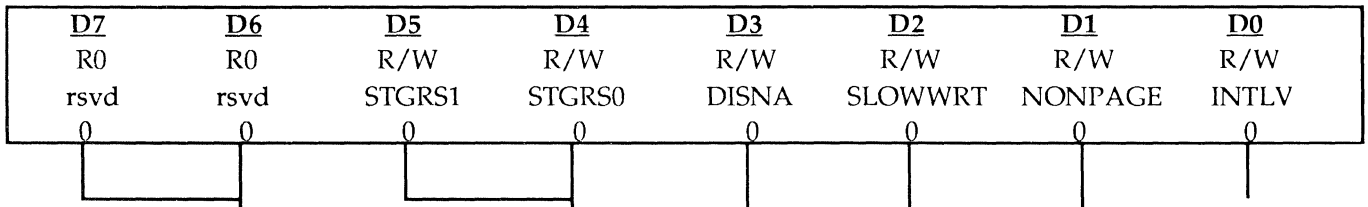
D3	D2	D1	D0	BANK0	BANK1	BANK2	BANK3
0	0	0	0	256K			
0	0	0	1	256K	256K		
0	0	1	0	256K	256K	256K	
0	0	1	1	256K	256K	256K	256K
0	1	0	0	256K	1M		
0	1	0	1	Reserved			
0	1	1	0	256K	256K	1M	
0	1	1	1	256K	256K	1M	1M
1	0	0	0	4M			
1	0	0	1	4M	4M		
1	0	1	0	Reserved			
1	0	1	1	Reserved			
1	1	0	0	1M			
1	1	0	1	1M	1M		
1	1	1	0	1M	1M	1M	
1	1	1	1	1M	1M	1M	1M

Reserved for future use. Must be set to 0. When set will read as 0.

Reserved for future use. Must be set to 0. When set will read as 1.

CONFIGURATION REGISTER 1, INDEX 12h, R/W

CONFIG1, Register 12h



D7	D6	D5	D4	D3	D2	D1	D0
R0	R0	R/W	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	STGRS1	STGRS0	DISNA	SLOWWRT	NONPAGE	INTLV
0	0	0	0	0	0	0	0

D0=0 Non interleave/ block interleave mode.
D0=1 Word Interleave mode.

D1=0 Page mode.
D1=1 Non page mode.

D2=0 Write HIT wait state(s) 1 less than read HIT cycles.

D2=1 Write HIT wait state(s) same as for read HIT cycles.

D3=0 Enable pipeline mode.
D3=1 Disable pipeline mode.

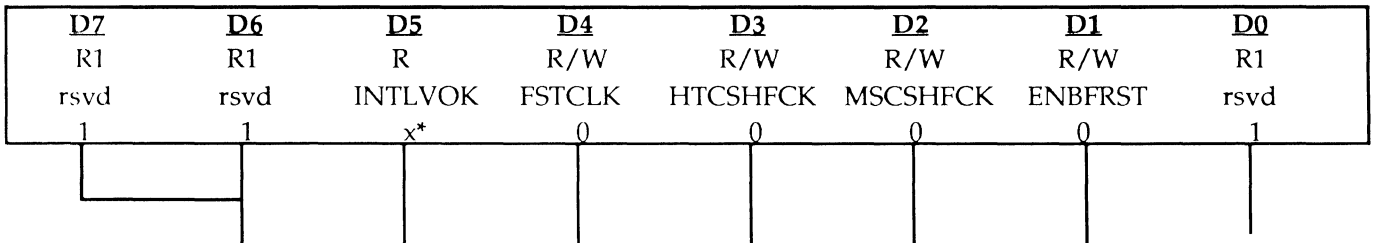
Staggered refresh in CLK2 cycles.

D5	D4	
0	0	Disable
0	1	Reserved
1	0	1 CLK2 staggering
1	1	2 CLK2 staggering

Reserved for future use, must be set to 0. When accesse will read as 0.

CONFIGURATION REGISTER 2, INDEX 13h, R/W

CONFIG2, Register 13h



D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R	R/W	R/W	R/W	R/W	R1
rsvd	rsvd	INTLVOK	FSTCLK	HTCSHFCK	MSCSHFCK	ENBFRST	rsvd
1	1	x*	0	0	0	0	1

Reserved for future use. Must be set to 0. When accessed will read as 1.

D1=0 Disable fast reset.
D1=1 Enable fast reset.

D2=0 MISS cycle CAS start as in CASTIM1.
D2=1 MISS cycle CAS start delayed by 1/2 CLK2.

D3=0 HIT cycles CAS start as in CASTIM2.
D3=1 HIT cycles CAS start delayed by 1/2 CLK2.

D4=0 Select CLK2 for RAS timeout.
D4=1 Select CPUCLK for RAS timeout.

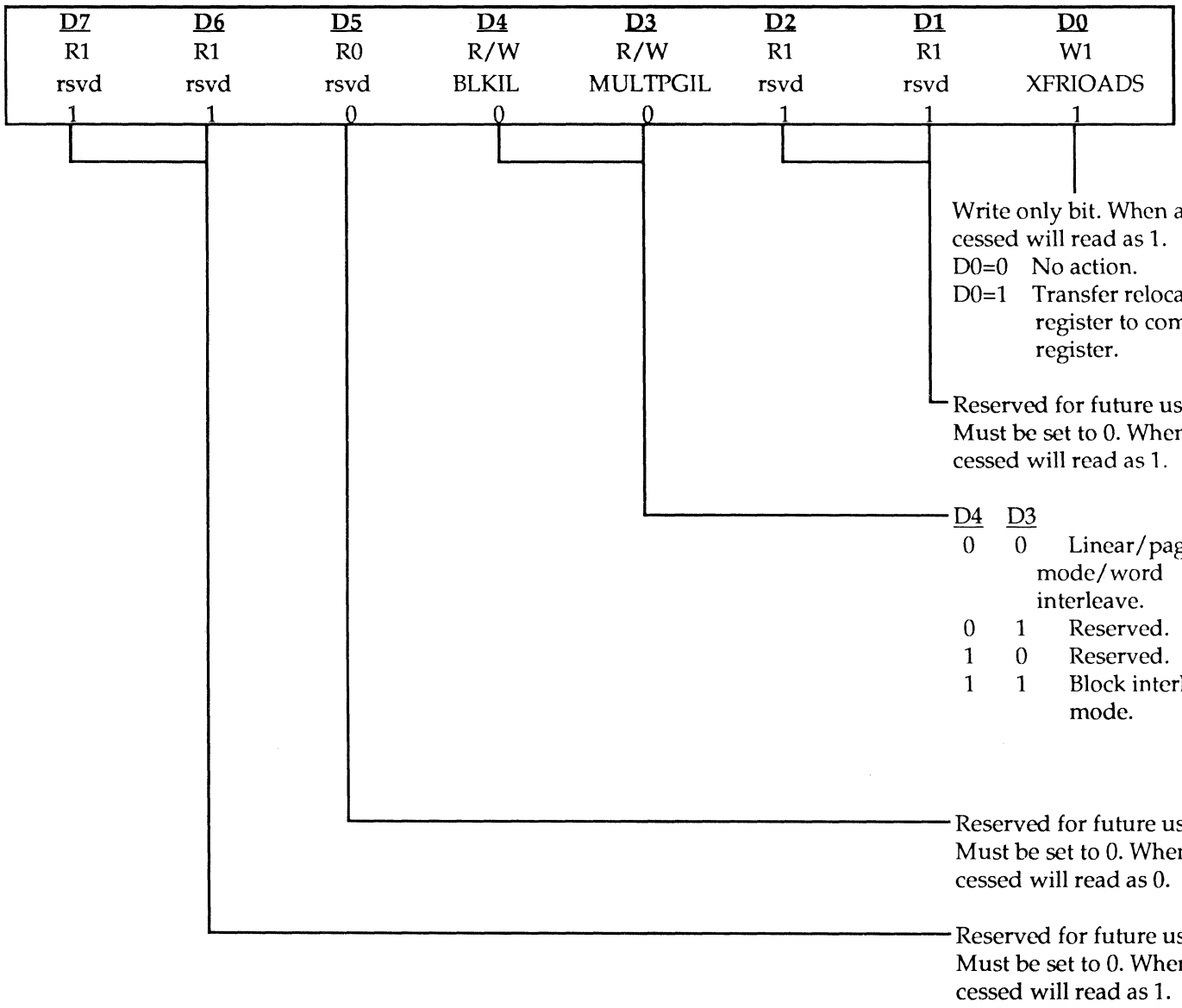
This is read only bit. This is set for valid interleave mode.

Reserved for future use. Must be set to 0. When accessed will read as 1.

*x = 1 for word interleave
0 for non-interleave/block interleave

CONFIGURATION REGISTER 3, INDEX 14h, R/W

CONFIG3, Register 14h



I/O MAP LOW REGISTER, I/O MAP HIGH REGISTER, INDEX 15h-16h, R/W

These two registers are used to remap the SL9252 configuration registers. To remap the register, load registers 15 and 16 with the target address (should be on a byte 2, 16 bit, boundary). Then write to configuration register 3 (14h) with bit 0=1. For example, to remap the configuration registers to address 162h, load register 16h with 01h, register 15h with 62h and set bit 0 in register 14h. All future accesses to configuration registers will then refer to the new address.

IOMAPLOW, Register 15h

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
AD7	AD6	AD5	AD4	AD3	AD2	AD1	0
0	0	1	0	0	0	1	0

IOMAPHI, Register 16h

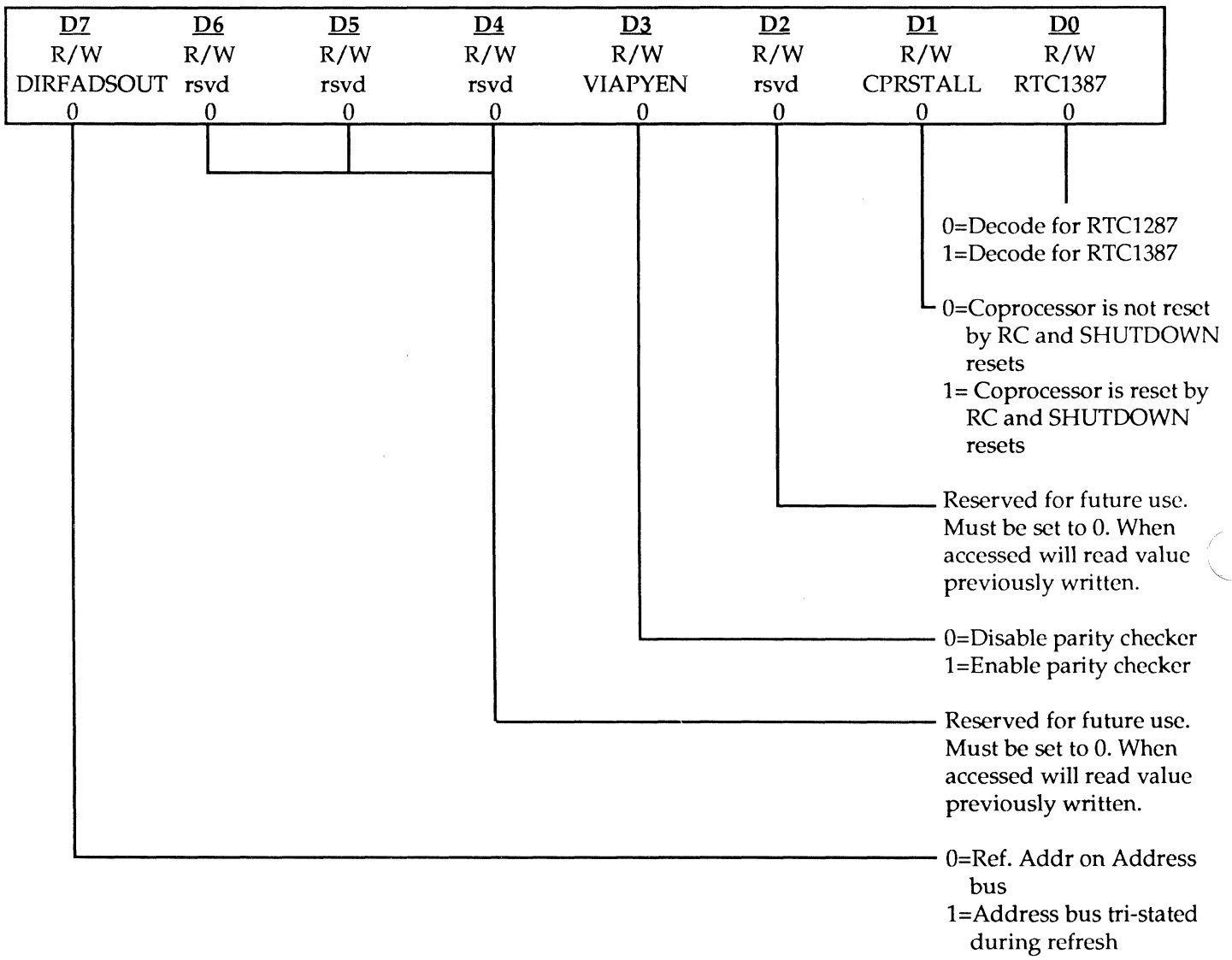
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
0	0	0	0	0	0	0	1

Example to indicate relocation (remap configuration registers to address 162h):

```
MOV     AX, 0122h
MOV     DX, AX
IN      AL, DX      ; dummy read ensures that pointer points to
                    the address register
MOV     AL, 15h
OUT     DX, AL      ; select index, Register 15h
MOV     AL, 62h
OUT     DX, AL      ; write data
MOV     AL, 16h
OUT     DX, AL      ; select index, Register 16h
MOV     AL, 01h
OUT     DX, AL      ; write data
MOV     AL, 14h
OUT     DX, AL      ; select Config. 3 register
IN      AH, DX      ; read current data
OR      AH, 01h     ; set LSB bit
OUT     DX, AH      ; transfer address to holding register
IN      AH, DX      ; read current value
AND     AH, FEh     ; reset LSB bit
OUT     DX, AH      ; restore original value to Config. 3 register.
```

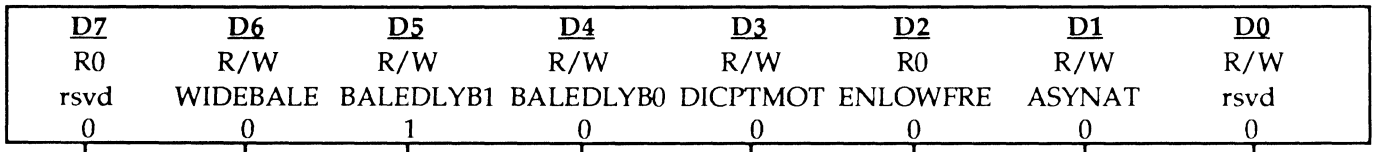
CONFIGURATION REGISTER 4, INDEX 17H, R/W

CONFIG4, Register 17h



SYSTEM CONTROL REGISTER, INDEX 18h, R/W

SYSCTL, Register 18h



D7	D6	D5	D4	D3	D2	D1	D0
R0	R/W	R/W	R/W	R/W	R0	R/W	R/W
rsvd	WIDEBALE	BALEDLYB1	BALEDLYB0	DICPTMOT	ENLOWFRE	ASYNAT	rsvd
0	0	1	0	0	0	0	0

Reserved for future use. Must be set to 0. When accessed will read value previously written.

D2	D1	
0	0	Synchronous (CLK2+4)
0	1	Asynchronous (ATCLK+2)
1	0	Synchronous (CLK2+8)
1	1	Reserved

D3=0 Co-processor timeout enable
D3=1 Co-processor timeout disable

D5	D4	BALEDLY in BUSCLK's
0	0	0
0	1	1
1	0	2
1	1	Reserved

D6=0 One BUSCLK wide BALE
D6=1 Two BUSCLK's wide BALE

Reserved, must be set to 0. When accessed will read as 0.

WAIT STATE 16 BIT MODE REGISTER, INDEX 19h, R/W

WAIT16, Register 19h

D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R/W	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	IO16RY2	IO16RY1	IO16RY0	MEM16RY2	MEM16RY1	MEM16RY0
1	1	0	0	1	0	0	1

Wait state select for 16 bit memory devices.

Bits 2-0 are coded as shown below.

D2	D1	D0	Wait States
0	0	0	1
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Wait state select for 16 bit I/O devices.

Bits 5 - 3 are coded as shown below.

D5	D4	D3	Wait States
0	0	0	1
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Reserved for future use. Must be set to 0. When accessed will read as 1.

WAIT STATE 8 BIT MODE REGISTER, INDEX 1Ah, R/W

WAIT8, Register 1Ah

D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R/W	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	IO8RY2	IO8RY1	IO8RY0	MEM8RY2	MEM8RY1	MEM8RY0
1	1	0	1	1	0	1	1

Wait state select for 8 bit memory devices.

Bits 2 - 0 are coded as shown below.

D2	D1	D0	Wait States
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Wait state select for 8 bit I/O devices.

Bits 5 - 3 are coded as shown below.

D5	D4	D3	Wait States
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Reserved for future use. Must be set to 0. When accessed will read as 1.

SYSTEM BUS COMMAND DELAY REGISTER, INDEX 1Bh, R/W

CMDDLY, Register 1Bh

D7	D6	D5	D4	D3	D2	D1	D0
R1	R1	R/W	R/W	R/W	R/W	R/W	R/W
rsvd	rsvd	IODLY1	IODLY0	MEM16DLY1	MEM16DLY0	MEM8DLY1	MEM8DLY0
1	1	0	0	0	0	0	1

Command delay for 8-bit AT-bus memory in BUSCLK's:

D1	D0	BUSCLK's
0	0	0
0	1	1
1	0	2
1	1	3

Command delay for 16-bit AT-bus memory in BUSCLK's:

D3	D2	BUSCLK's
0	0	0
0	1	1
1	0	2
1	1	3

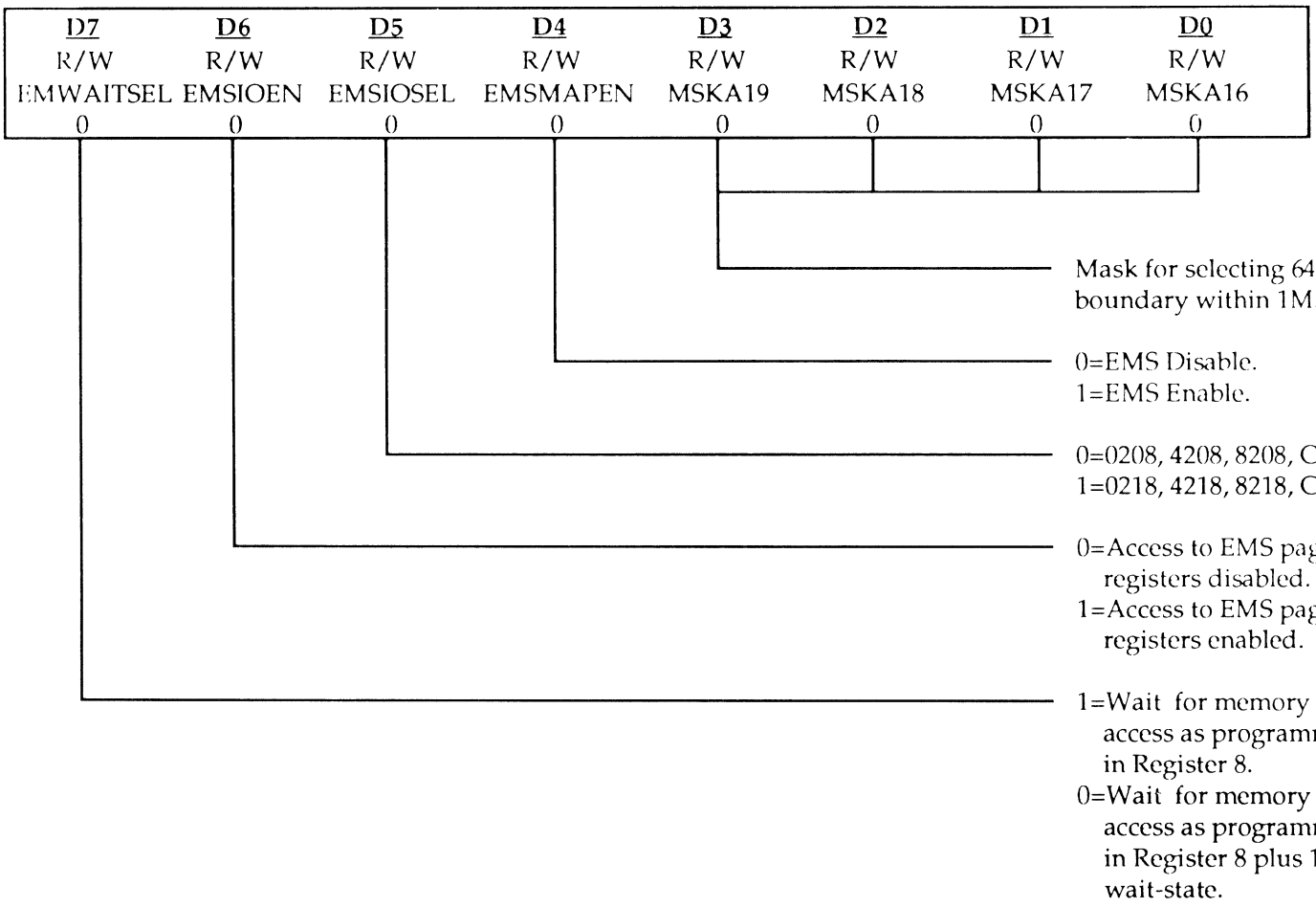
Command delay for I/O devices:

D5	D4	BUSCLK's
0	0	0
0	1	1
1	0	2
1	1	3

Reserved, must be set to 0. When accessed will read as 1.

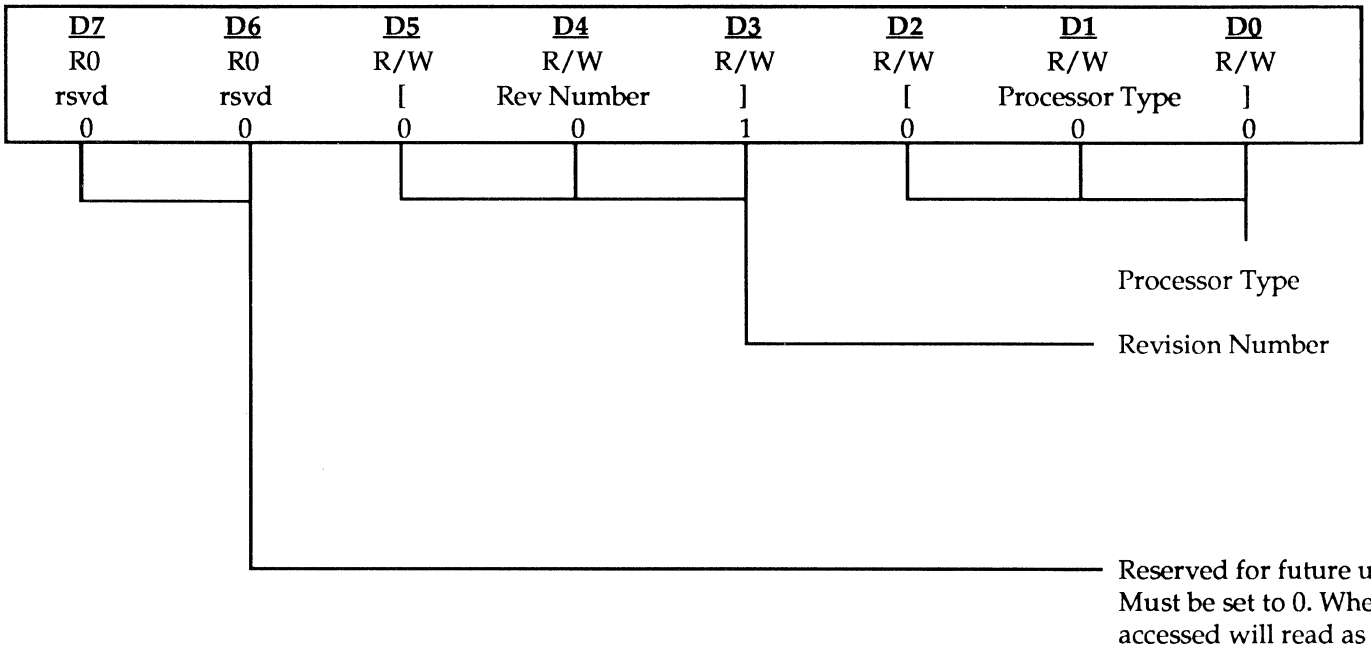
EMS CONTROL REGISTER, INDEX 1Ch, R/W

EMSCTLREG, Register 1Ch



ID REGISTER, INDEX 1Fh (Read Only)

IDREG, Register 1Fh



CONFIGURATION REGISTER, cont'd

Table 10 shows the chip default configuration values after reset.

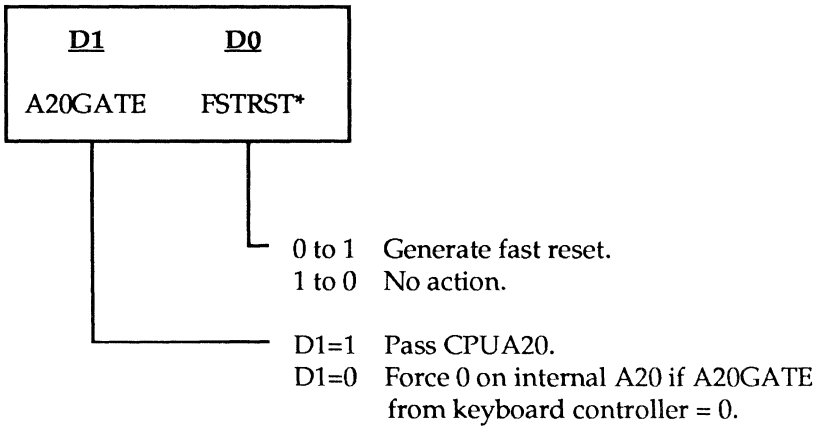
INDEX REGISTER		DEFAULTS								
ADDRESS	NAME	D7	D6	D5	D4	D3	D2	D1	D0	
0	SDWREG0	R1	R1	0	0	0	0	0	0	C0h
1	SDWREG1	R1	R1	0	0	0	0	0	0	C0h
2	SDWREG2	R1	R1	0	0	0	0	0	0	C0h
3	SDWREG3	R1	R1	0	0	0	0	0	0	C0h
4	SDWREG4	R1	R1	0	0	0	0	0	0	C0h
5	SDWREG5	R1	R1	0	0	0	0	0	0	C0h
6	SDWREG6	R1	R1	0	0	0	0	0	0	C0h
7	SDWREG7	R1	R1	0	0	0	0	0	0	C0h
8	RAMWAIT	R1	0	1	1	1	1	1	1	BFh
9	REMAP	R1	0	0	0	0	0	0	0	80h
A	ROMCTL0	R1	R1	0	0	0	0	0	0	C0h
B	ROMCTL1	R1	R1	0	0	0	0	0	0	C0h
C	ROMCTL2	R1	R1	R0	1	1	1	1	1	DFh
D	RASTIM	R1	R1	1	0	0	0	1	1	E3h
E	CASTIM1	R1	R1	1	1	0	1	1	1	F7h
F	CASTIM2	R1	R1	0	0	1	0	0	1	C9h
10	DISMEM	R1	R1	0	0	0	0	0	0	C0h
11	MEMTYPE	R1	R1	0	0	0	0	0	0	C0h
12	CONFIG1	0	0	0	0	0	0	0	0	00h
13	CONFIG2	R1	R1	R	0	0	0	0	R1	E1h (if D5=1)
14	CONFIG3	R1	R1	R0	0	0	R1	R1	W	C6h
15	IOMAPLOW	0	0	1	0	0	0	1	0	22h
16	IOMAPHI	0	0	0	0	0	0	0	1	01h
17	CONFIG4	0	0	0	0	0	0	0	0	00h
18	SYSCTL	R0	0	1	0	0	R0	0	0	20h
19	WAIT16	R1	R1	0	0	1	0	0	1	C9h
1A	WAIT8	R1	R1	0	1	1	0	1	1	DBh
1B	CMDDLY	R1	R1	0	0	0	0	0	1	C1h
1C	EMSCTLREG	0	0	0	0	0	0	0	0	00h
1D		RESERVED								
1E										
1F	IDREG	R0	R0	R0	R0	R1	R0	R0	R0	08h

Table 10 Configuration Values

W : Write only bit(s). See Configuration register description.
R : Read only bit(s). See CONFIG2 register description.
R1: Read only bit(s). Reads "one".
R0: Read only bit(s). Reads "zero".

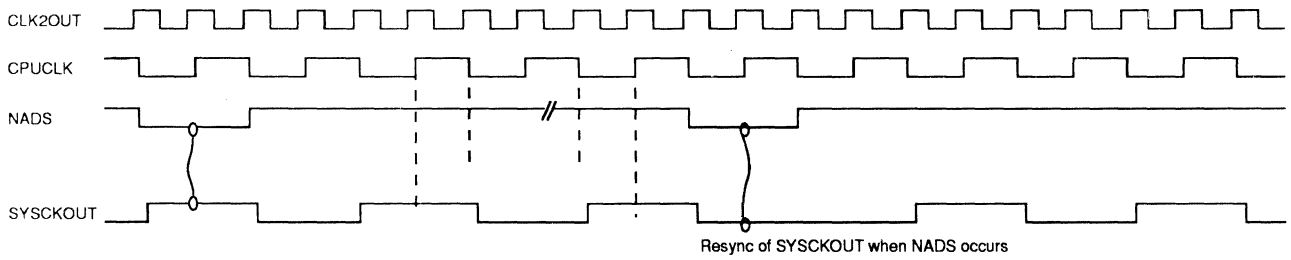
PORT92

Port92

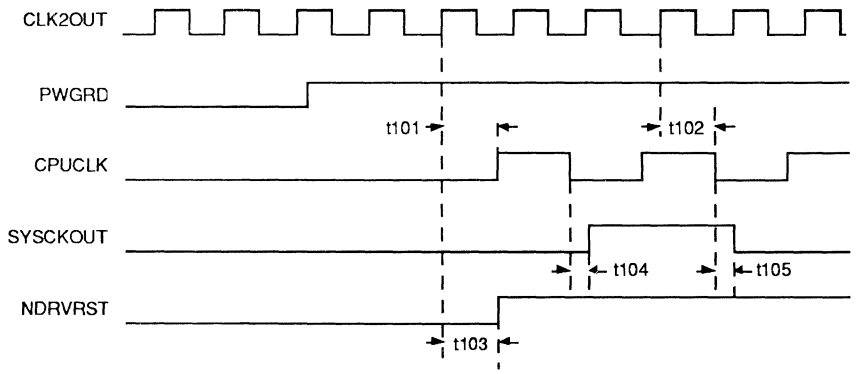


*FSTRST: After the "0 to 1" transition, the status is maintained after a CPURESET so that BIOS can determine if the reset was caused by a reset through this port. To generate a reset again, a "0" should be written before a "1" is written into this bit.

VIII. AC TIMING DIAGRAMS SL9252

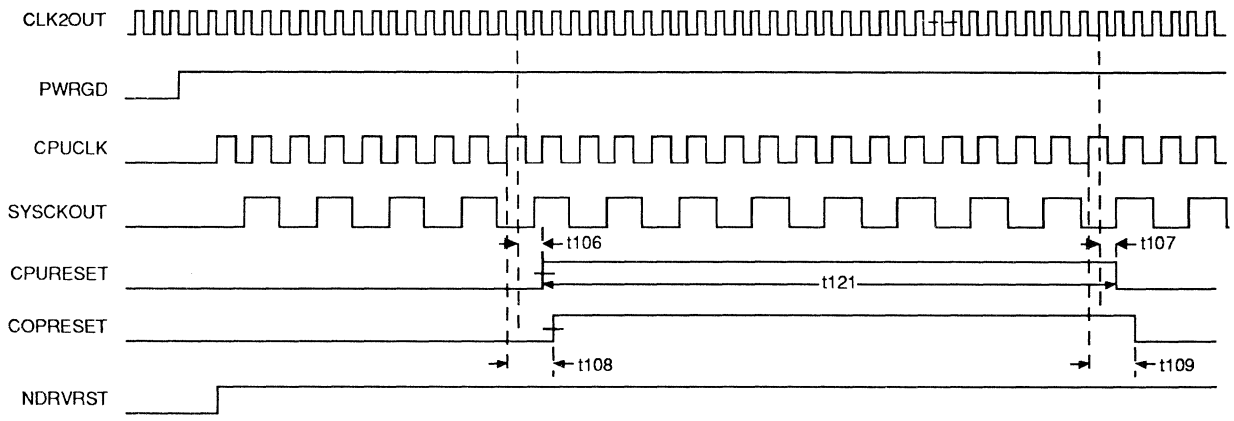


Timing 1 SYSCKOUT Relationship with CPUCLK and Synchonization with NADS in Sync Mode

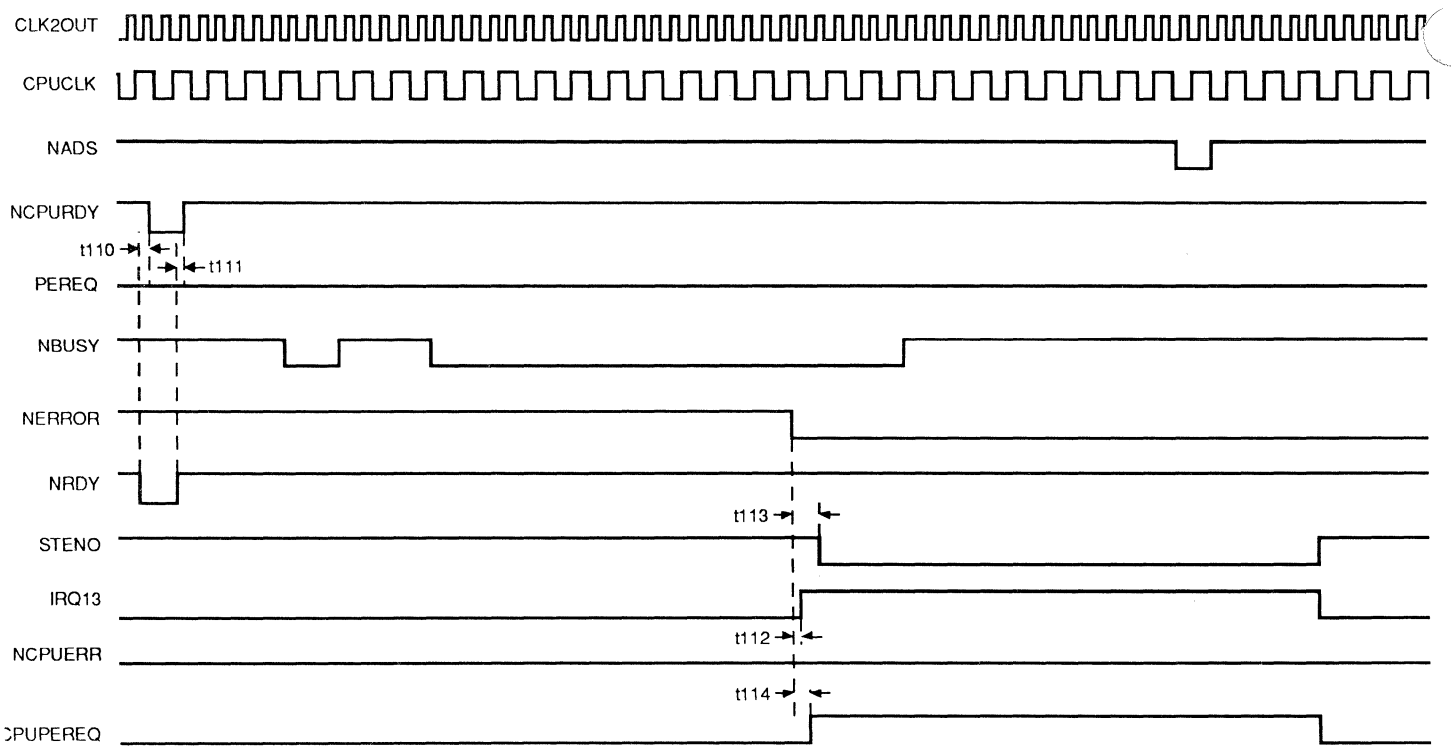


Timing 2 PWRGD and CLOCKS

AC TIMING DIAGRAMS SL9252, cont'd

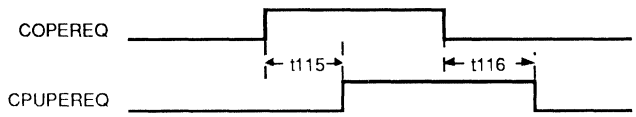


Timing 3 CPURST and COPRESET

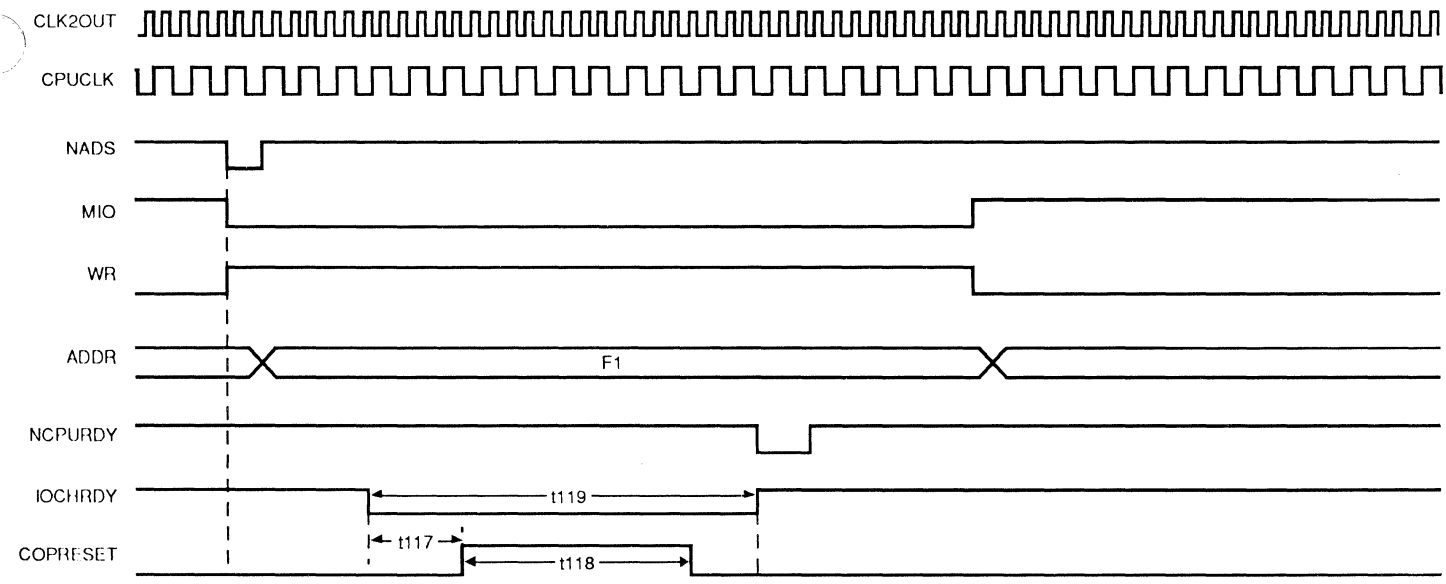


Timing 4 Coprocessor Interface

AC TIMING DIAGRAMS SL9252, cont'd

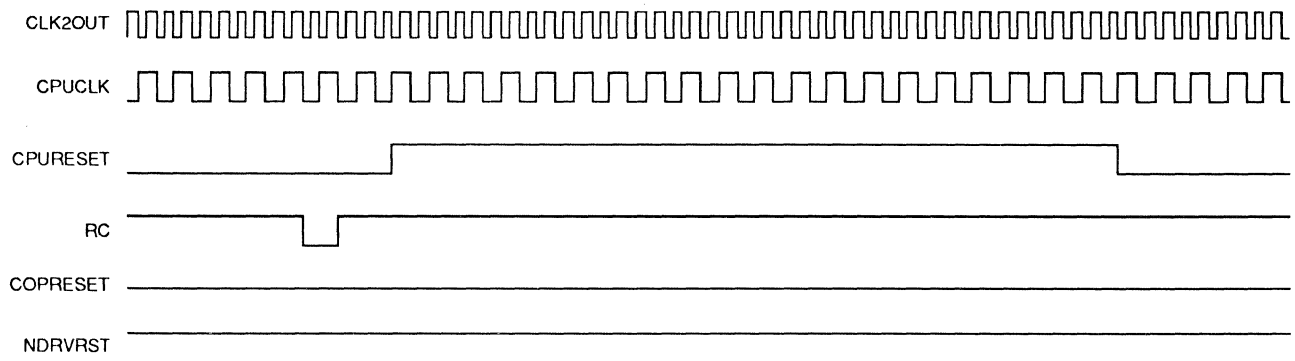


Timing 5 COPEREQ and CPUPEREQ

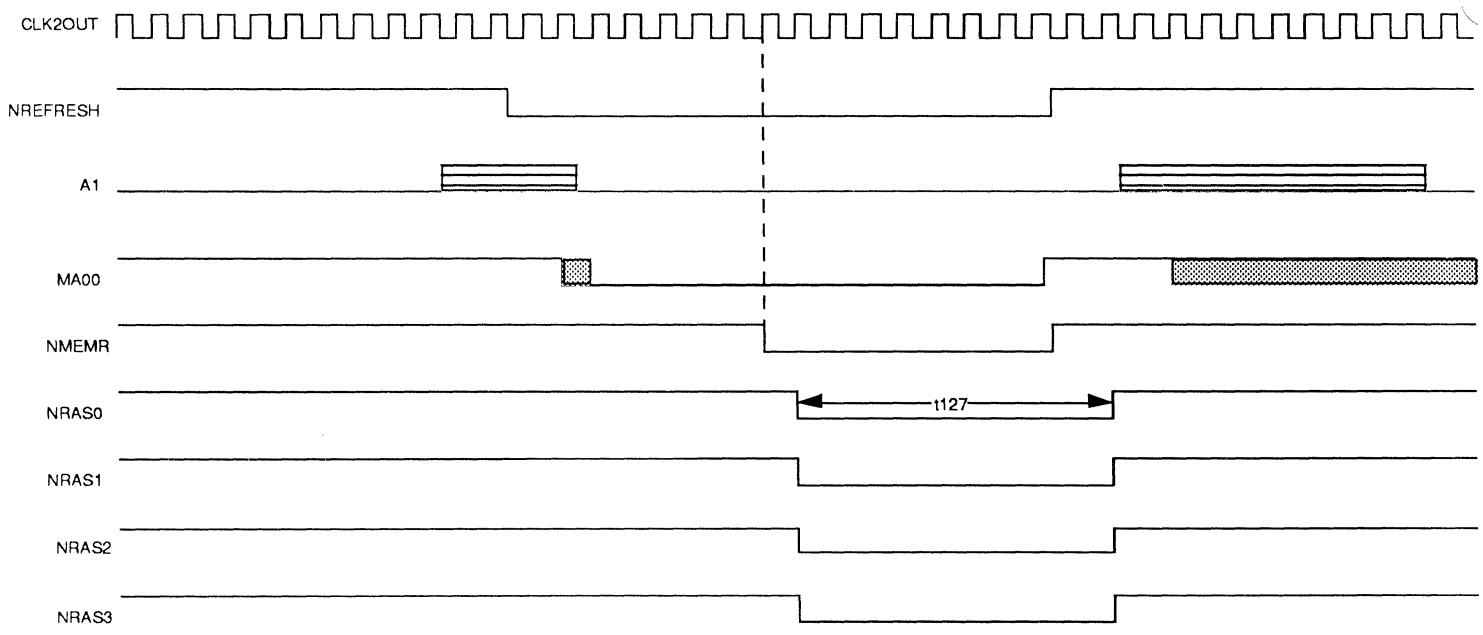


Timing 6 IOCHRDY and COPRESET

AC TIMING DIAGRAMS SL9252, cont'd

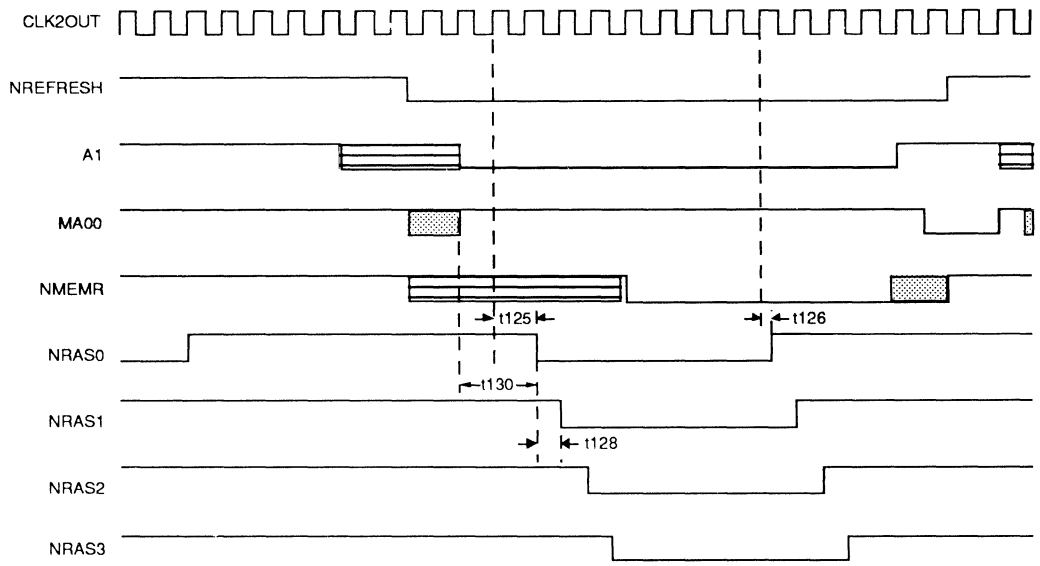


Timing 7 RC RESET

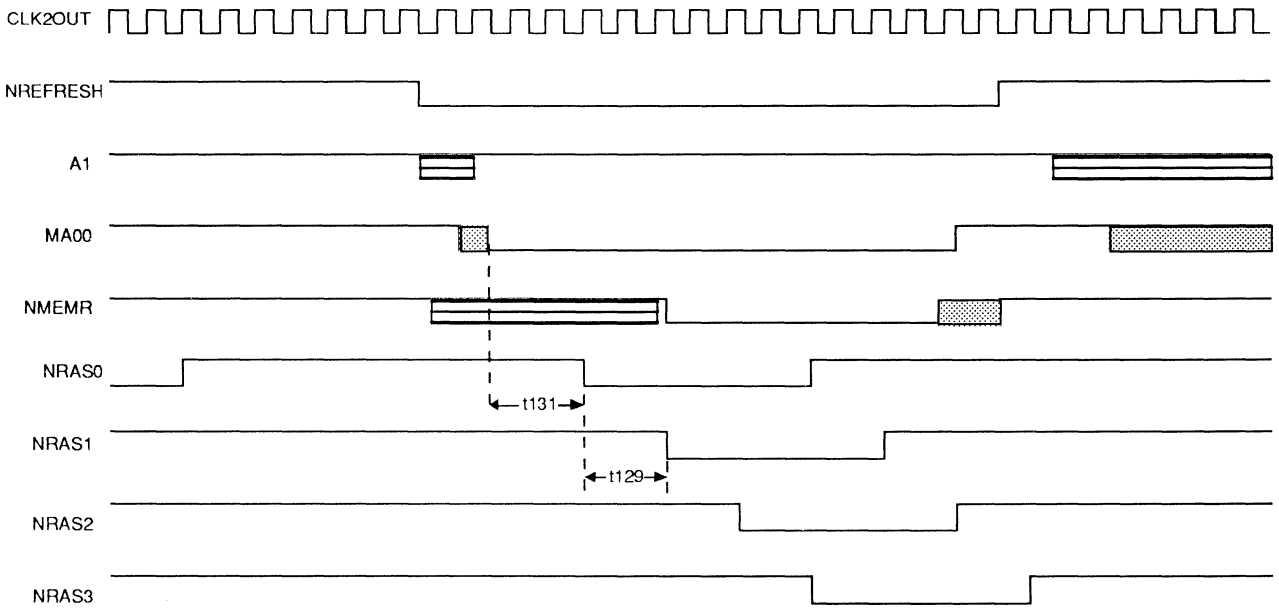


Timing 8 Non-Staggered Refresh

AC TIMING DIAGRAMS SL9252, cont'd

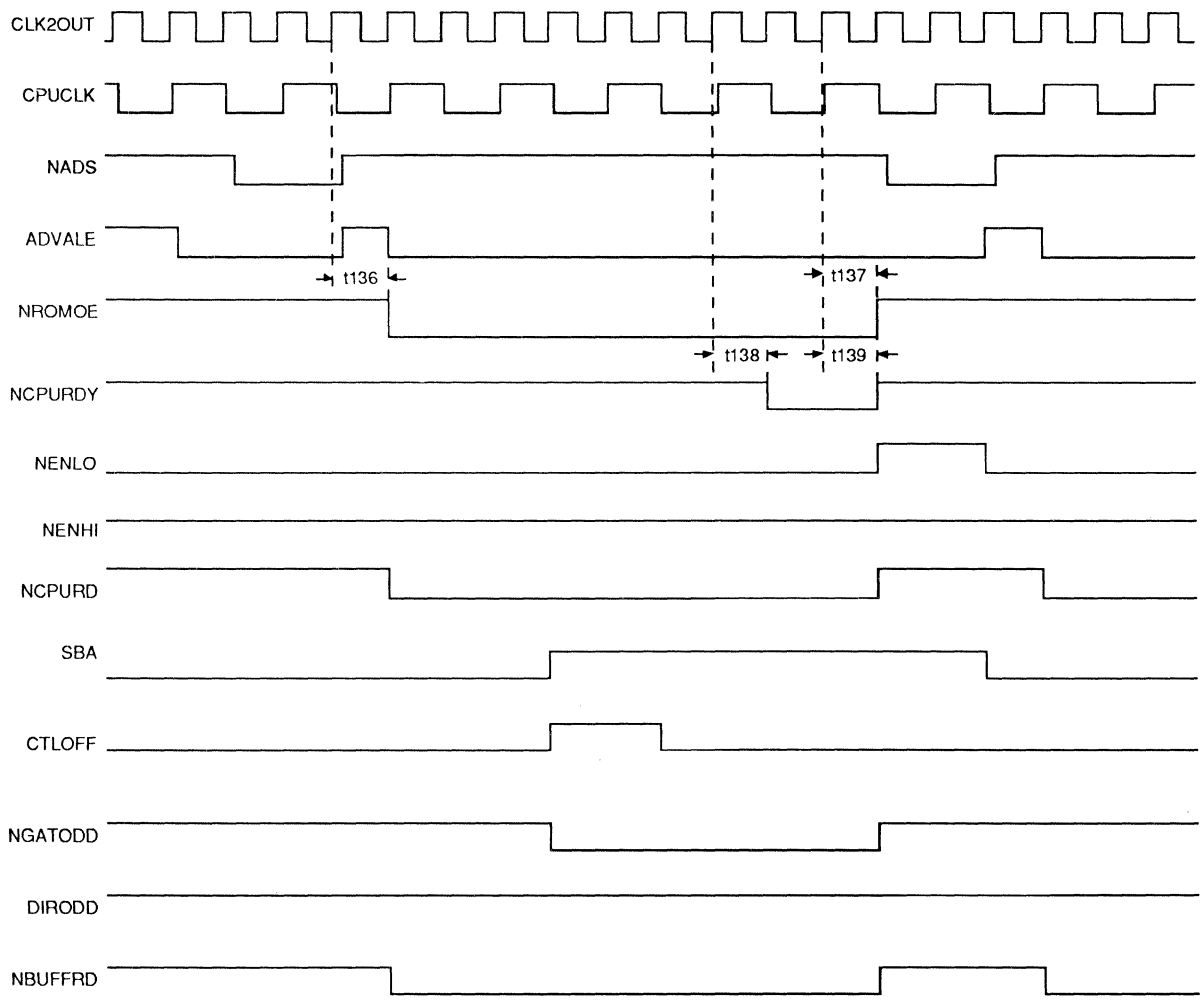


Timing 9 One CLK2 Staggered Refresh



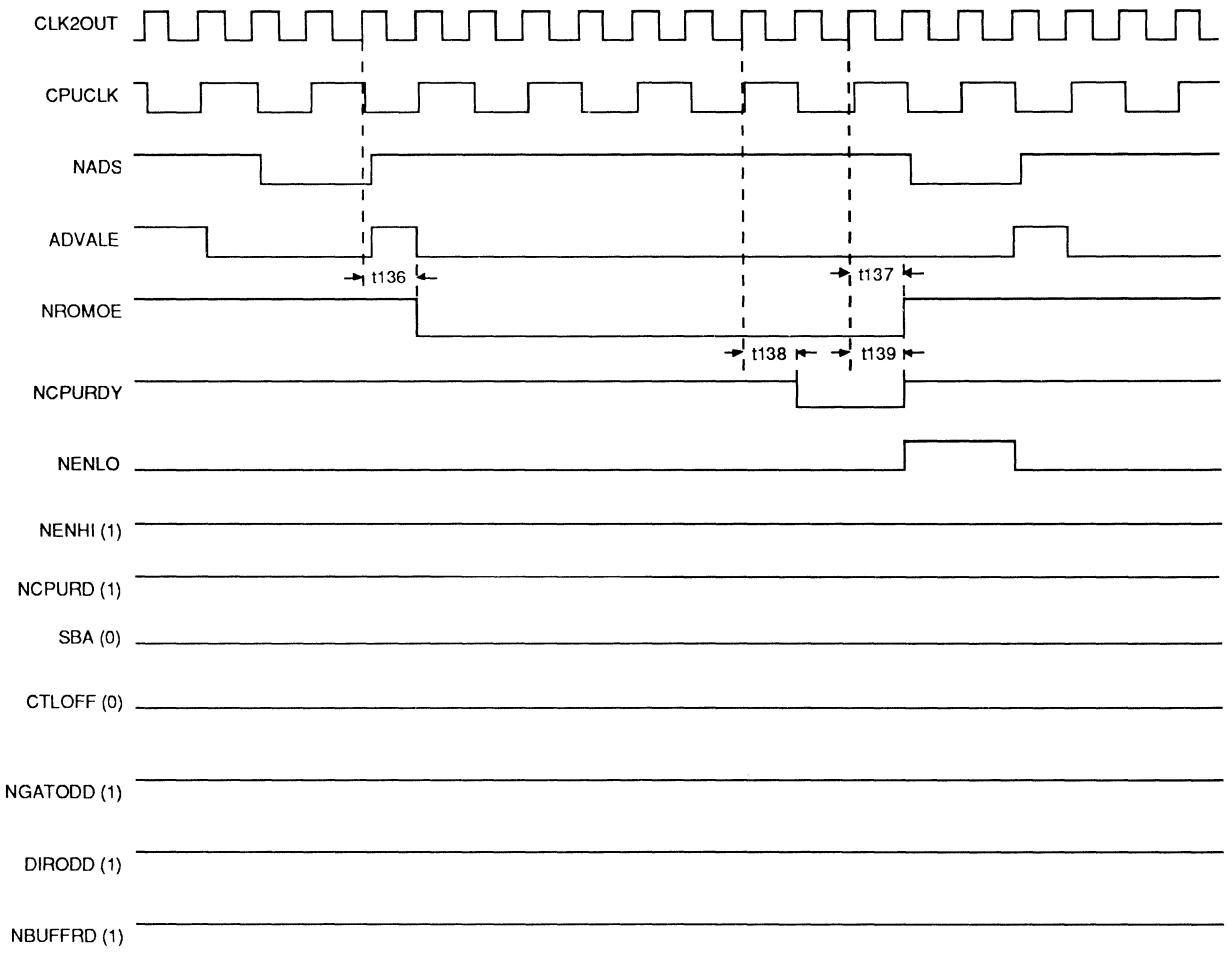
Timing 10 Two CLK2 Staggered Refresh

AC TIMING DIAGRAMS SL9252, cont'd



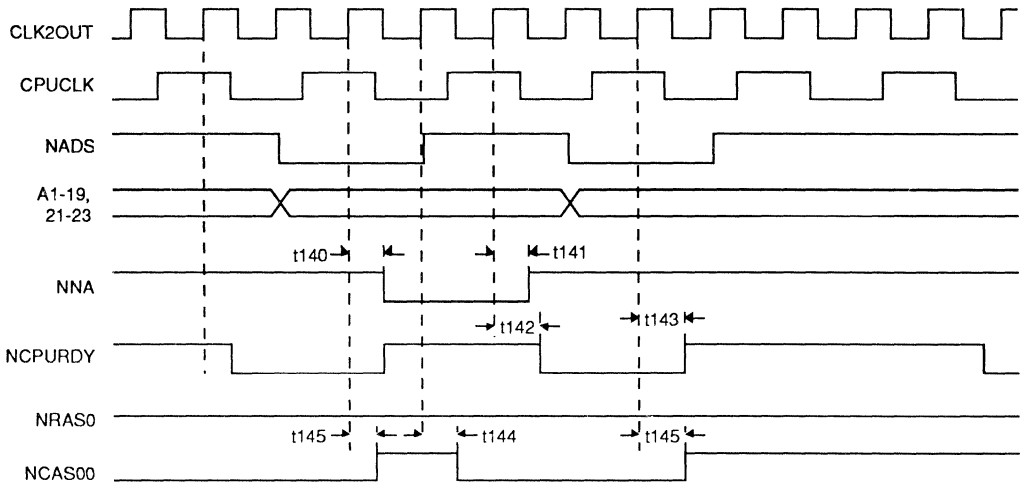
Timing 11 One Wait State Byte ROM Access

AC TIMING DIAGRAMS SL9252, cont'd

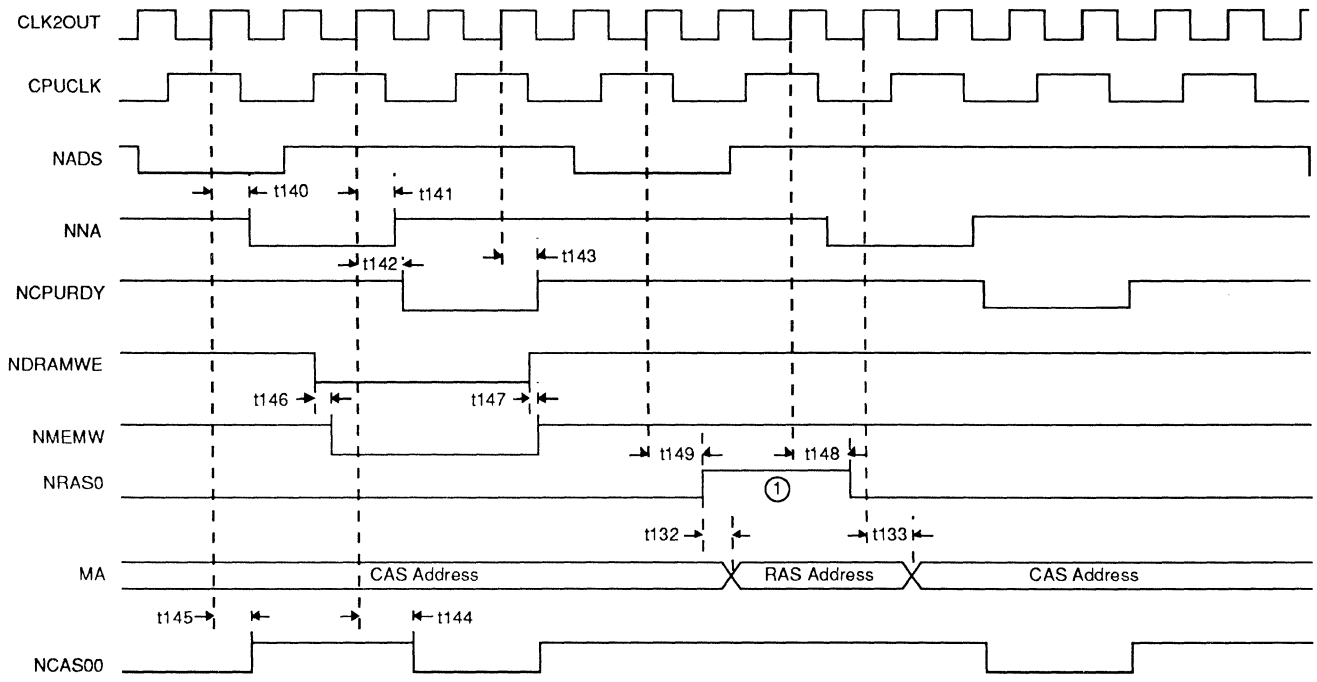


Timing 12 Four Wait State Word ROM Access

AC TIMING DIAGRAMS SL9252, cont'd



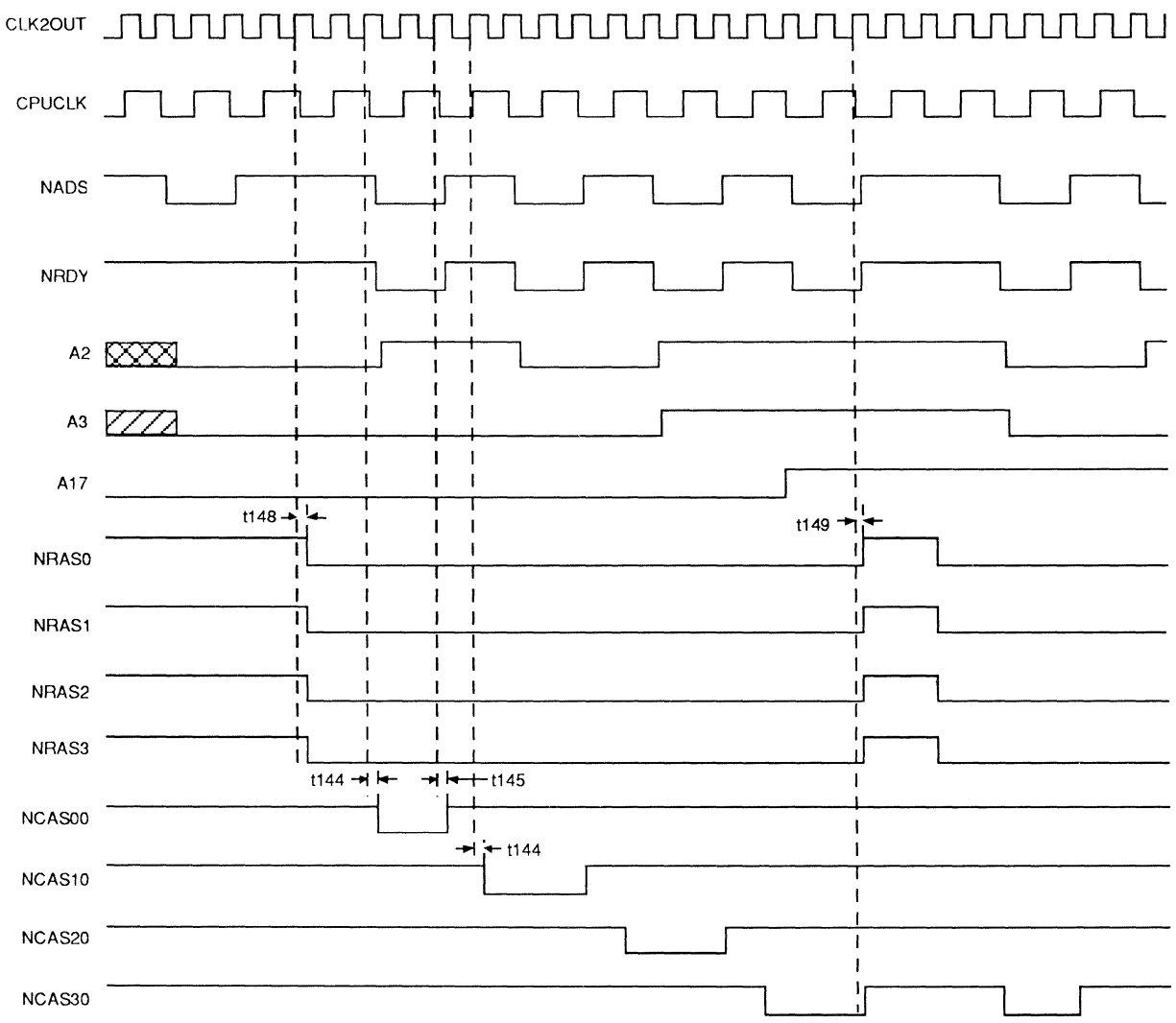
Timing 13 Zero Wait RAM Read Hit Cycle (Pipelined Mode)



Note 1: 2CLK2 RAS Precharge for miss cycle.

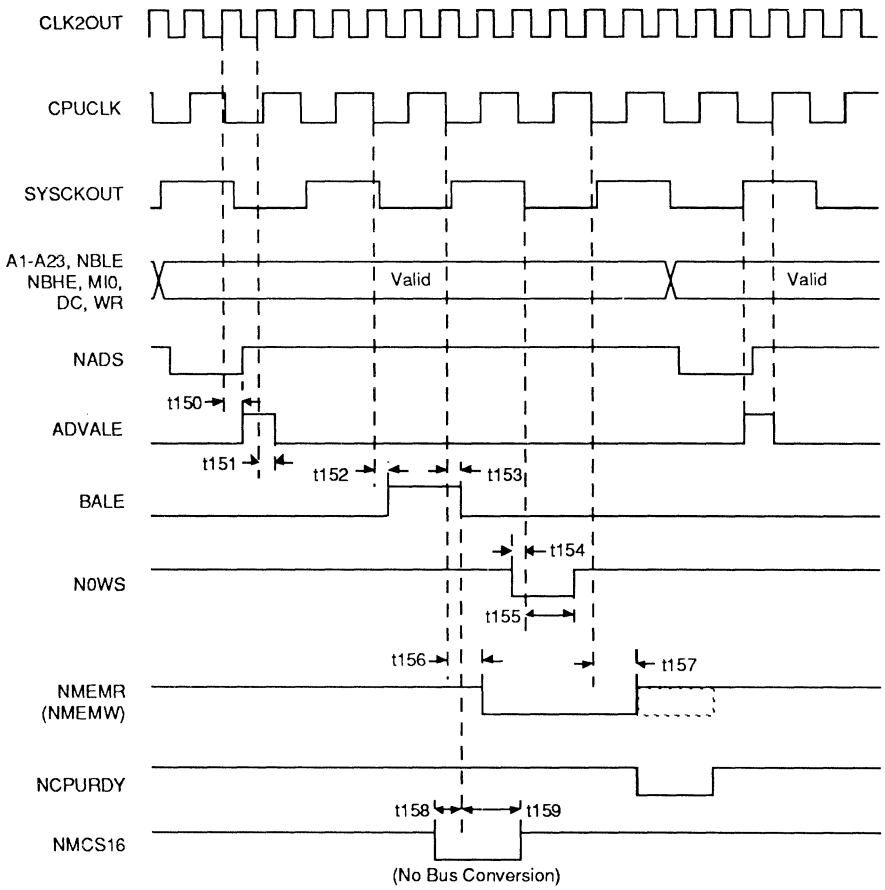
Timing 14 Zero Wait State RAM Write Hit Cycle Followed by One Wait State RAM Read Miss Cycle

AC TIMING DIAGRAMS SL9252, cont'd



Note: Address A17 used to show different page selection.

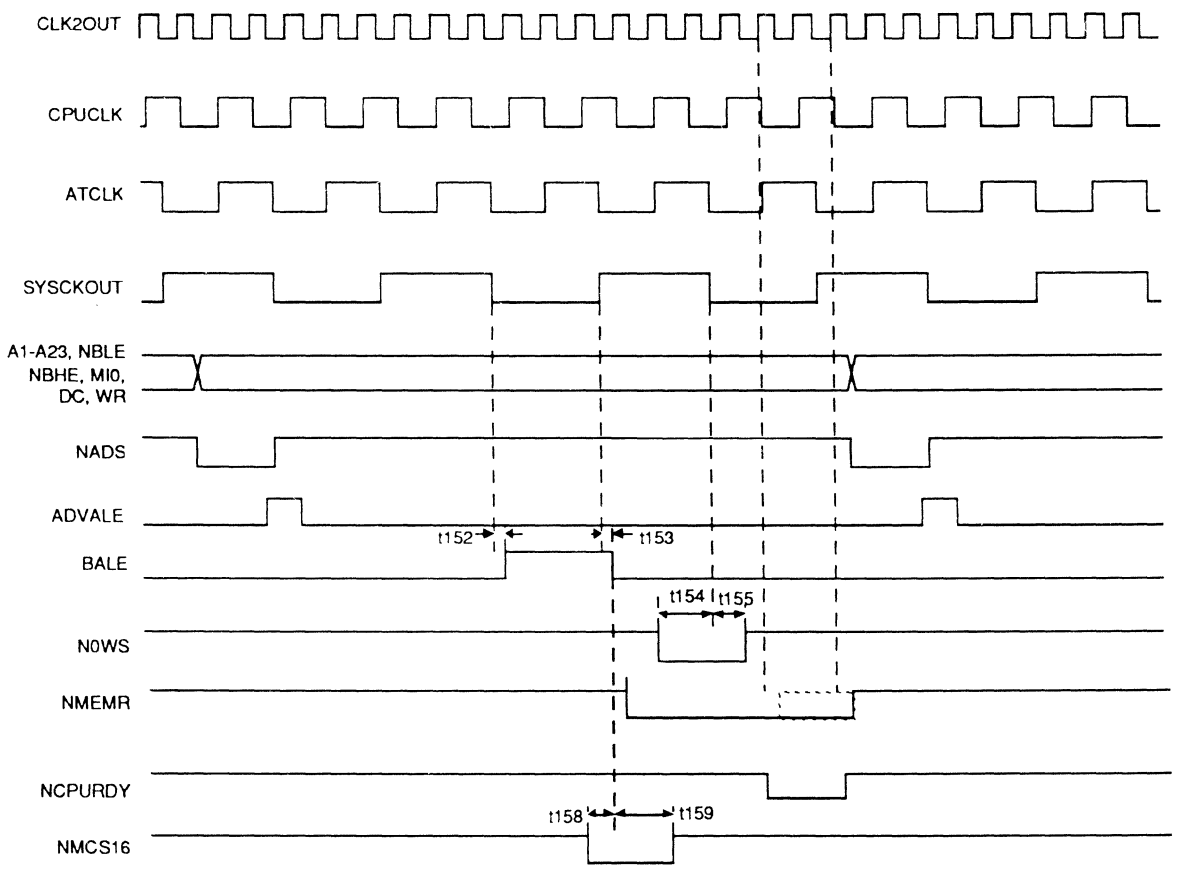
Timing 15 4-Way Page Interleave



NOTES:
1. NOWS active setup to SYSCKOUT falling edge is to ensure AT (ISA) 0 wait state cycle.
2. NMCS16 setup ensures that no bus conversion cycle takes place.
3. NMEMW is negated with NCPURDY assertion.
4. NMEMR is negated with NCPURDY negative.

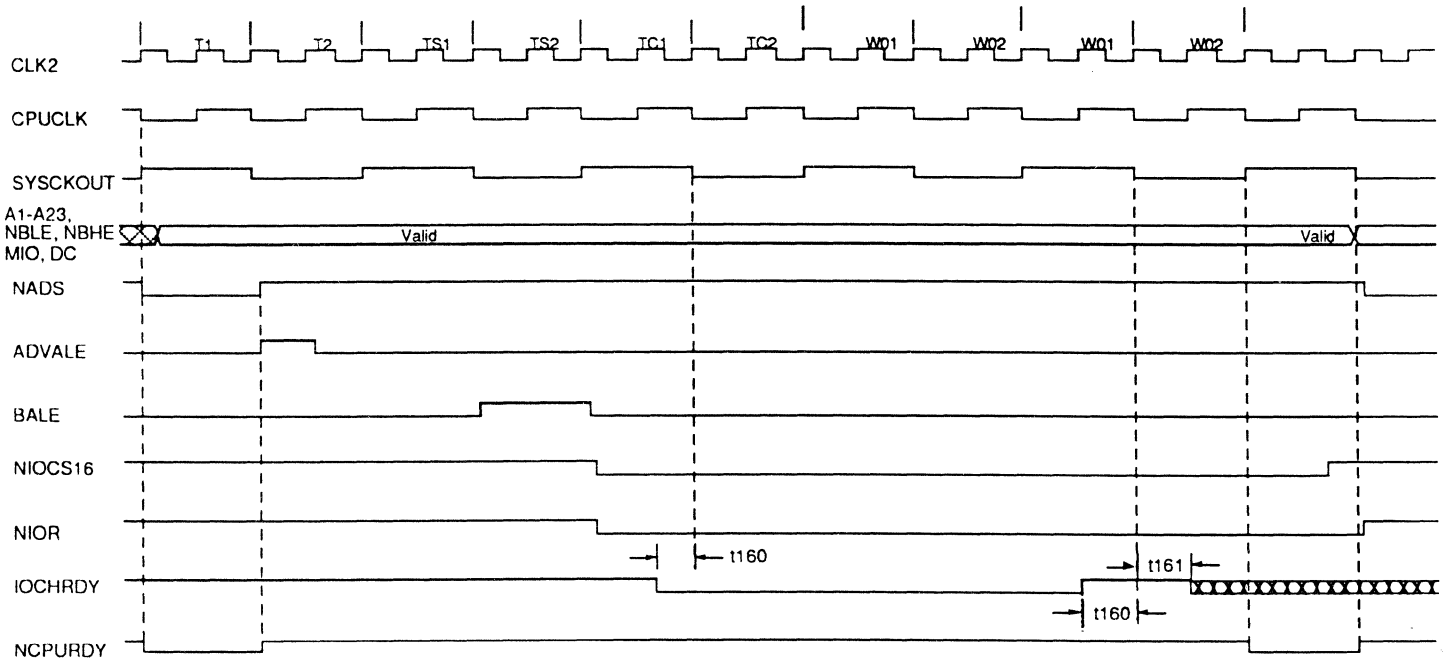
Timing 16 16-Bit External Memory Cycle, Zero Wait State Nonpipelined Synchronous Mode

AC TIMING DIAGRAMS SL9252, cont'd



Timing 17 16-Bit External Memory Cycle, Zero Wait State Asynchronous Mode

AC TIMING DIAGRAMS SL9252, cont'd



Timing 18 16-Bit External I/O Read Cycle, Synchronous Mode, 2 Wait State Using IOCHRDY to Extend the Cycle Non-Pipelined

IX. ABSOLUTE MAXIMUM RATINGS SL9252 *note 1

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage *note 2	VDD	VSS-0.5	6.0	V
Input Voltage *note 2	VI	VSS-0.5	VDD+0.5	V
Output Voltage *note 2	VO	VSS-0.5	VDD+0.5	V
Output Current (IOL = 3.2mA) *note 2	IOS	-40	+40	mA
Output Current (IOL = 8mA) *note 3	IOS	-40	+80	mA
Output Current (IOL = 12mA) *note 3	IOS	-60	+120	mA
Output Current (IOL = 24mA) *note 3	IOS	-90	+180	mA
Storage Temp.	TSTG	-40	+125	°C
Storage Temp.	TBIAS	-25	+85	°C

* NOTES:

1. Permanent device damage may occur if device ratings are exceeded. Reliability may be affected by sustained exposure to absolute maximum values.
2. VSS = 0V
3. Not more than one output may be shortened at a time for a maximum duration of one second.

X. RECOMMENDED OPERATING CONDITIONS SL9252

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	VDD	4.75	5.25	V
Operating Temperature	TA	0	70	°C
Input High Voltage for Normal Input	VIH	2.2		V
Input Low Voltage for Normal Input	VIL		0.8	V
Input High Voltage for CMOS Input	VIH	VDDx0.7		V
Input Low Voltage for CMOS Input	VIL		VDDx0.3	V

NOTE: Conditions for outgoing functional test are VIH = 3.0V VIL = 0V

XI. DC CHARACTERISTICS SL9252

(Recommended Operating Conditions Unless Otherwise Noted)

PARAMETERS	SYMBOL	MIN.	MAX	UNITS	CONDITIONS
Power Supply Current	IDDS	0	100	µA	Steady state *note 1
Output High Voltage for Normal Output (IOL = 4 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 8 mA)	VOH	4.0	VDD	V	IOH = - 2 mA
Output High Voltage for Driver Output (IOL = 12 mA)	VOH	4.0	VDD	V	IOH = - 4 mA
Output High Voltage for Driver Output (IOL = 24 mA)	VOH	4.0	VDD	V	IOH = - 8 mA
Output Low Voltage for Normal Output (IOL = 4 mA)	VOL	Vss	0.4	V	IOL = 3.2 mA
Output Low Voltage for Driver Output (IOL = 8 mA)	VOL	Vss	0.4	V	IOL = 8 mA
Output Low Voltage for Driver Output (IOL = 12 mA)	VOL	Vss	0.4	V	IOL = 12.0 mA
Output Low Voltage for Driver Output (IOL = 24 mA)	VOL	Vss	0.5	V	IOL = 24.0 mA
Input High Voltage for Normal Input	VIH	2.2		V	
Input Low Voltage for Normal Input	VIL		0.8	V	
Input High Voltage for CMOS Input	VIH	VDD x0.7		V	
Input Low Voltage for CMOS Input	VIL		VDD x0.3	V	
Input Leakage Current	ILI	-10	10	µA	VI = 0 - VDD
Input Leakage Current	ILZ	-10	10	µA	Tri-state VI = 0 - VDD
Input Pull-up/Down Resistor	RP	25	100	KΩ	VIH = VDD VIL = VSS

* NOTES:

1. VIH = VDD, VIL = VSS
2. 24 mA drive: CLK2OUT, SA0.
3. 12 mA drive: BALE, IOCHRDY, MA0-MA10, MODA20, NCAS00, NCAS01, NCAS10, NCAS11, NCAS20, NCAS21, NCAS30, NCAS31, NDRAMWE, NIOR, NIOW, NMEMR, NMEMW, NRAS0-3, NSBHE, NSMEMR, NSMEMW, SYSCKOUT.
4. 8 mA drive: ADVALE, CLK8042, CPUCLK, NCPURDY.
5. 4 mA drive: All other outputs.

XII. AC CHARACTERISTICS SL9252

SYMBOL	DESCRIPTION	MIN.	TYP	MAX.	NOTE
t101	CLK2OUT to CPUCLK (low to high)	6		18.6	
t102	CLK2OUT to CPUCLK (high to low)	6		19.7	
t103	CLK2OUT to NDRVRST (low to high)			TBD	
t104	CPUCLK low to SYSCKOUT (low to high)	6		25	1
t105	CPUCLK low to SYSCKOUT (high to low)	6		26	1
t106	CLK2OUT to CPURST (low to high)	149		631	
t107	CLK2OUT to CPURST (high to low)	5		23	
t108	CPUCLK to COPRESET (low to high)		12		
t109	CPUCLK to COPRESET (high to low)		11		
t110	NCOPRDY low to NCPURDY low	4		18	
t111	NCOPRDY high to NCPURDY high	3		13	
t112	NERROR low to IRQ13 high	4		17	
t113	NERROR low to STENO low	6		24	
t114	NERROR low to CPUPEREQ low	4		19	
t115	COPEREQ high to CPUPEREQ high	3		13	
t116	COPEREQ low to CPUPEREQ low	4		18	
t117	IOCHRDY low to COPRESET		2 CLK2's		
t118	IO Access 'F1' 'COPRESET' width		192 CLK2's		
t119	IO Access 'F1' 'IOCHRDY' low width		292 CLK2's		
t121	CPURST active width		32 CLK2's		
t125	NRAS(i) active delay from CLK2 high	5		21	
t126	NRAS(i) inactive delay from CLK2 high	7		29	
t127	NRAS(i) pulse width		7 CLK2's		2
t128	NRAS(i + 1) active delay from NRAS(i) active		1 CLK2		3
t129	NRAS(i + 1) active delay from NRAS(i) active		2 CLK2's		4
t130	Refresh address setup time to NRAS0	16			3
t131	Refresh address setup time to NRAS0	11			4
t132	Row address from NRAS negation	5		22	
t133	CLK2OUT to column address		17		
t136	NROMOE active delay from CLK2OUT	6		25	
t137	NROMOE inactive delay from CLK2OUT	6		23	
t138	NCPURDY active from CLK2OUT high	5		20	
t139	NCPURDY inactive from CLK2OUT high	5		21t140	
t140	NNA active from CLK2OUT	7		31	
t141	NNA inactive from CLK2OUT	6		26	

Notes:

1: In Sync mode
2: Non-staggered refresh
3: One CLK2 staggered refresh
4: Two CLK2's staggered refresh

XII. AC CHARACTERISTICS SL9252, cont'd

SYMBOL	DESCRIPTION	MIN.	TYP	MAX.	NOTE
t142	NCPURDY active from CLK2OUT	5		19	
t143	NCPURDY inactive from CLK2OUT	5		21	
t144	CLK2OUT to NCASX active	7		30	5
t145	CLK2OUT to NCASX inactive	7		30	5
t146	NDRAMWE active to NMEMW active		7		
t147	NDRAMWE inactive to NMEMW inactive		5		
t148	CLK2OUT to NRASX active	8		32	6
t149	CLK2OUT to NRASX inactive	9		38	6
t150	ADVALE active from CLK2OUT	4		16	
t151	ADVALE inactive from CLK2OUT	4		15	
t152	BALE active from SYSCKOUT low (CPU access)	4		15	
t153	BALE inactive from SYSCKOUT high (CPU access)	6		26	
t154	N0WS setup time to SYSCKOUT low		3		
t155	N0WS hold time to SYSCKOUT low		3		
t156	NMEMR active from SYSCKOUT high		15		
t157	NMEMR inactive from SYSCKOUT low		13		
t158	NMCS16 setup time to BALE low	2		9	
t159	NMCS16 hold time to BALE low	1		6	
t160	IOCHRDY setup time to SYSCKOUT low	2		10	
t161	IOCHRDY hold time to SYSCKOUT low	2		8	

Notes:

5: NCASX corresponds to NCAS00, 01, 10, 11, 20, 21, 30, 31

6: NRASX corresponds to NRAS0, 1, 2, 3

XIII. CAPACITANCE SL9252

(TA = 25 ° C, VDD = V1 = 0V, fo = 1MHz)

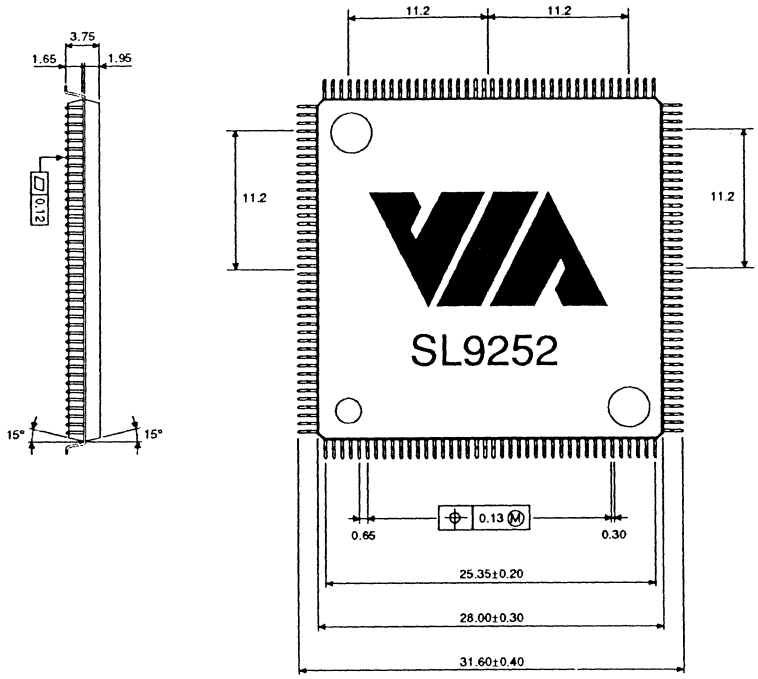
PARAMETERS	SYMBOL	MIN.	MAX	UNITS
Input Pin Capacitance	CIN	---	16	pF
Output Pin Capacitance (IOL = 3.2 mA, 8 mA, or 12 mA)	COUT	---	16	pF
Output Pin Capacitance (IOL = 24 mA)	COUT	---	18	pF
I/O Pin Capacitance (IOL = 3.2 mA, 8 mA, or 12 mA)	CI/O	---	16	pF
I/O Pin Capacitance (IOL = 24 mA)	CI/O	---	23	pF

The FlexSet™ PC/AT 80386SX System & Memory Controller SL92

PRELIMINARY

PACKAGE INFORMATION

160 Pin Flat Pack



ORDERING INFORMATION

Device Type:
SL9252

Package Type:
FP-Plastic Flat Pack

Temperature Range:
C- Commercial temperature range, 0 to 70 °C, 4.75 to 5.25 V

SL9252 XX X

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January, 1991

VIA Technologies, Inc. (408) 746-2200
860 East Arques Avenue
Sunnyvale CA 94086