System Programming Manual

VX800 / VX820 Series

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VIA TECHNOLOGIES, INC.

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Offices:

VIA Technologies Incorporated
USA Office:
940 Mission Court
Fremont, CA 94539
USA
Tel: (510) 683-3300
Fax: (510) 683-3301 or (510) 687-4654
Home Page: http://www.viatech.com

VIA Technologies Incorporated
Taiwan Office:
1st Floor, No. 531
Chung-Cheng Road, Hsin-Tien
Taipei, Taiwan ROC
Tel: (886-2) 2218-5452
Fax: (886-2) 2218-5453
Home page: http://www.via.com.tw

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REGISTERS OVERVIEW

Register Document Introduction

This document includes the registers for VIA VX800 and VX820 Series. Please refer to Table 1 for the specification differences of these products.

This chip integrates functional modules of the traditional North Bridge and South Bridge chips, plus 3D/2D and Video Processors, Video Decoding Accelerator and controller for external display interface. The register set is partitioned into three blocks: North Module, South Module and Graphics and Video Module; of which, North Module and South Module registers are described in this **System Programming Manual** while graphics and video registers are described in the **Graphics and Video Programming Guide**.

Table 1. VX800 / VX820 Series Feature Comparison Table

Product Model	VX800UT	VX800	VX820UT	VX820
FSB Speed (MHz)	400-533	400-800	533	400-800
Integrated GFX Clock (MHz)	200	250	200	250
Memory Type	DDR2 533	DDR2 667	DDR2 533	DDR2 667
PCI Express Ports	3x1	1x4 + 2x1	2x1	2x1
PCI	Yes	Yes	No	No
SATA	Yes (SATA 1.0)	Yes (SATA 2.0)	No	No
Core Voltage	1.25V	1.5V	1.25V	1.5V
Package Dimension	33 x 33mm FCBGA 1236 balls		21 x 21mm FCBGA 1086 balls	

Note 1. Registers related to features that the product does not support should be reserved.

Module and Register Scope Definitions

Module Name Abbreviations

NM: North Module. It contains functional modules of the traditional North Bridge chip.
SM: South Module. It contains functional modules of the traditional South Bridge chip.
NSMIC: North-South Module Interface Control
SNMIC: South-North Module Interface Control
PM: Power Management
HDAC: High Definition Audio Controller

Register Scope Map Within Modules

To specifically identify every function, the following abbreviations will be applied in subsequent sections.

Abbreviation of Register Space / Module Name	Register Space	Function
North Module		
D0F0	PCI Device 0. Function 0	Host Controller
D0F1	PCI Device 0, Function 1	Error Reporting
D0F2	PCI Device 0, Function 2	Host Bus Control
D0F3	PCI Device 0, Function 3	DRAM Bus Control
D0F4	PCI Device 0, Function 4	Power Management and Chip Testing Control
D0F5	PCI Device 0, Function 5	APIC and Central Traffic Control
D0F6	PCI Device 0, Function 6	Scratch Registers
D0F7	PCI Device 0, Function 7	North-South Module Interface Control **<NSMIC>**
D2F0 / PEG0	PCI Device 2, Function 0	PCI Express Root Port G0 – x4, x2, x1
D3F0 / PE0	PCI Device 3, Function 0	PCI Express Root Port 0 – x1
D3F1 / PE1	PCI Device 3, Function 1	PCI Express Root Port 1 – x1
RCRB-H	Memory Space	PCI Express Root Complex Register Block for Host

Abbreviation of Register Space / Module Name	Register Space	Function
South Module		
D12F0	PCI Device 12, Function 0	SDIO Host Controller
SDIO-MMIO	Memory Space	SDIO Memory Mapped I/O Space Registers
D13F0	PCI Device 13, Function 0	Security Digital Controller
SDC-MMIO	Memory Space	Security Digital Controller Memory Mapped I/O Space
Data DMA-MMIO	Memory Space	Data DMA Memory Mapped I/O Space Registers
CICH DMA-MMIO	Memory Space	CICH DMA Memory Mapped I/O Space Registers
PCI Control-MMIO	Memory Space	PCI Control Memory Mapped I/O Space Registers
D15F0	PCI Device 15, Function 0	Serial ATA and EIDE Controller
D16F0	PCI Device 16, Function 0	USB 1.1 UHCI Ports 0-1
D16F1	PCI Device 16, Function 1	USB 1.1 UHCI Ports 2-3
D16F2	PCI Device 16, Function 2	USB 1.1 UHCI Ports 4-5
D16F4	PCI Device 16, Function 4	USB 2.0 EHCI Controller
D17F0	PCI Device 17, Function 0	Bus and Power Management Control
PMIO	IO Space	ACPI I/O Registers
PM-MMIO	Memory Space	Power Management Memory Mapped I/O Space Registers
SMIO	Memory Space	System Management Bus I/O Space Registers
D17F7	PCI Device 17, Function 7	South-North Module Interface Control **<SNMIC>**
D19F0	PCI Device 19, Function 0	PCI-to-PCI Bridge
D20F0 / HDAC	PCI Device 20, Function 0	High Definition Audio Controller
HDAC-MMIO	Memory Space	HDAC Memory Mapped I/O Space Registers
SPI-MMIO	Memory Space	Special Peripheral Interface Memory Mapped I/O Space
FIR	IO Space	IrDA Host Controller / IO Space Registers

Register Table Format

Column Definitions

In the register descriptions, column "**Default**" indicates the power-on default value of register bit(s), while column "**Attribute**" indicates access type of register bit.

Attribute Definitions:

Read / Write Attributes: read / write attributes may be used together to specify combined attributes

RO:	Read Only.
RZ:	Read as Zero.
R1:	Read as 1.
WO:	Write Only. (register value can not be read by the software)
IW:	Ignore Write.
MW:	Must Write back what is read.
XW:	Backdoor Write.
RW:	Read / Write.
RW1:	Write Once then Read Only after that.
RW1C:	Read / Write of "1" clears bit to zero.
RsvdP:	Reserved. Must do a read-modify-write to preserve the bit values.
RsvdZ:	Reserved. Must write 0's.
RSM:	Bits are in resume-well.

Sticky Attributes: adding a "S" in tail to indicate a sticky register, which means that register will not be set or altered by hot reset.
Ex. RWS: Sticky-Read/Write. **ROS**: Sticky-Read Only. **RW1CS**: Sticky-Write-1-to-Clear.

Special Default Value Definitions

Dip:	Means the default value is set by dip switch or strapping.
HwInit:	Hardware initialized; bit default value is set by hardware to reflect related status.

PCI Arbiter Control

I/O Port Address: 22h
PCI Arbiter Disable **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**PCI2 Arbiter Control** 0: Enable PCI2 Bus Arbiter 1: Disable PCI2 Bus Arbiter
0	RW	0	**PCI1 Arbiter Control** 0: Enable PCI1 Bus Arbiter (arbiter will respond to REQ# assertion) 1: Disable PCI1 Bus Arbiter (arbiter will not respond to PCI-1 REQ# and PREQ# assertion)

PCI Configuration Space I/O

This chip's PCI space registers are addressed via the following configuration mechanism:

Mechanism #1

These ports respond only to double-word accesses. Byte or word accesses will be passed on unchanged.

I/O Port Address: CFB-CF8h
PCI Configuration Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Configuration Space Enable** 0: Disable 1: Convert configuration data port writes to configuration cycles on the PCI bus
30:24	RO	0	**Reserved** (always reads 0)
23:16	RW	0	**PCI Bus Number** Used to choose a specific PCI bus in the system
15:11	RW	0	**Device Number** Used to choose a specific device in the system
10:8	RW	0	**Function Number** Used to choose a specific function if the selected device supports multiple functions
7:2	RW	0	**Register Number (also called the "Offset")** Used to select a specific DWORD in the configuration space
1:0	RW	0	**Fixed** (always reads 0)

I/O Port Address: CFF-CFCh
PCI Configuration Data **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**PCI Configuration Data**

Note: Refer to PCI Bus Specification Version 2.3 for further details on operation of the above configuration registers.

NORTH MODULE REGISTER DESCRIPTIONS

Device 0 Function 0 (D0F0): Host Controller

Device 0 Function 0, the host controller, is connected to the PCI bus through AD11 as the IDSEL.
All registers are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with bus number 0, device number 0 and function number 0.

Header Registers (00-3Fh)

Offset Address: 01-00h (D0F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F0)

Device ID **Default Value: 0353h**

Bit	Attribute	Default	Description
15:0	RO	0353h	**Device ID Code**

Offset Address: 05-04h (D0F0)

PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0. (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F0)
PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error** (SERR# asserted)
13	RW1C	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RW1C	0	**Master Data Parity Error** This bit is set when bus master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as A Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	1b	**Support New Capability List** 0: No new capability 1: Support new capability
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F0)
Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Chip Revision Code**

Offset Address: 0B-09h (D0F0)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F0)
Class Code **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cacheline Size**

Offset Address: 0Dh (D0F0)
PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**PCI Bus Time Slice for CPU as A Master** (in Unit of PCI clocks)
2:0	RO	0	**Reserved** Bit [2:1] is programmable; however, it's read as 0.

Offset Address: 0Eh (D0F0)
Header Type **Default Value: 00 or 80h**

Bit	Attribute	Default	Description
7:0	RO	00 or 80h	**Header Type** Could be 80 when Rx4F[0] = 1

Offset Address: 0Fh (D0F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST Support** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 10-2Bh (D0F0) – Reserved

Offset Address: 2D-2Ch (D0F0)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F0)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F0) – Reserved

Offset Address: 34h (D0F0)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** An offset address from the start of the configuration space

Offset Address: 35-4Eh (D0F0) – Reserved

Multiple Function and Legacy Space Access Control (4F-C6h)

Offset Address: 4Fh (D0F0)

Multiple Function Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Multi-Function Support** 0: Disable. Registers of functions 1-7 cannot be accessed, and the value returned will be 0FFFFFFFFh when accessed. 1: Enable. The status will be reflected on Rx0E[7].

Offset Address: 50-B9h (D0F0) – Reserved

Offset Address: C0h (D0F0)

Graphics Memory and IO Space Access Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Memory Space Access** Three memory spaces of GFX are used: SL, MMIO, LL. Please see the following diagram for details. 0: Does not respond to memory space access 1: Responds to memory space access
0	RW	0	**I/O Space Access** The IO address ranges are 3B0h~3B7h, 3B8h~3BBh and 3C0h~3DFh. 0: Does not respond to I/O space access 1: Responds to I/O space access

Offset Address: C1-C5h (D0F0) – Reserved

Offset Address: C6h (D0F0)

Legacy Space Access Control **Default Value: 18h**

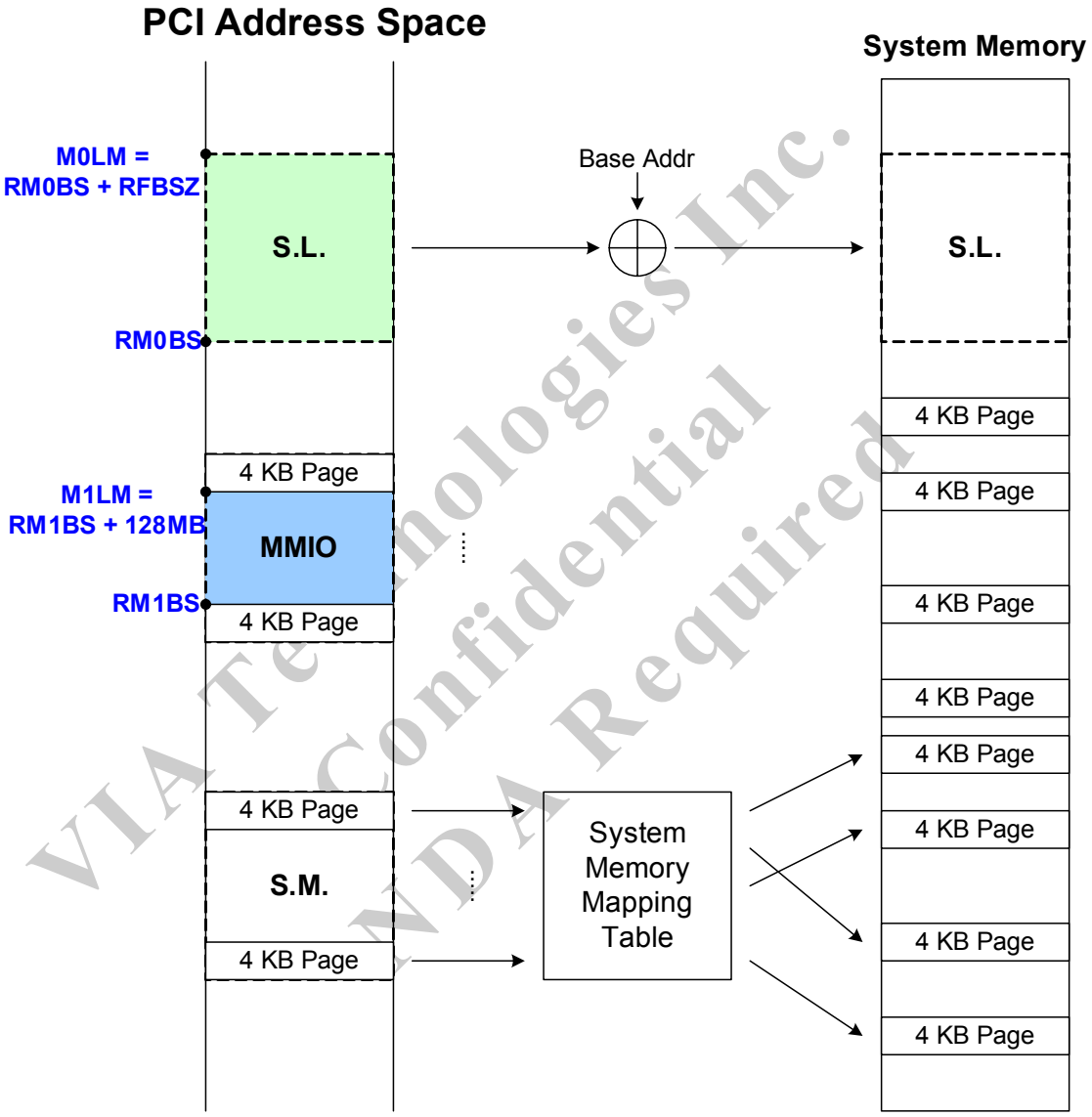
Bit	Attribute	Default	Description
7:2	RO	06h	**Reserved**
1	RW	0	**MDA Resource Location** 0: PCI2. Forward MDA access cycles to PCI2. 1: PCI1. Forward MDA access cycles to PCI1. The setting of this bit overwrites the settings on the IO / Memory's Base and Limit of other devices. MDA Resources include Memory: B0000h-B7FFFFh and I/O Ports 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh.
0	RO	0	**Reserved**

Control Registers for Integrated Graphics / Video Processor (C7-FFh)

Offset Address: C7h (D0F0) – Reserved

The integrated Graphics / Video processor uses up to two memory spaces; they are S.L. (**S**ystem memory **L**ocal frame buffer) and MMIO.

1. S.L. : Base address, RM0BS, is decided by D0F0 RxCF-C8, SL size is decided by D0F3 RxA1[6:4]
2. MMIO : Base address, RM1BS, is decided by D0F0 RxD7-D0, MMIO size is fixed to 128MB



Offset Address: CB-C8h (D0F0)
GFX Shadow Memory Base 0 - S.L. **Default Value: FFF0 0000h**

Bit	Attribute	Default	Description
31:4	RW	FFF0 000h	**GFX's Memory Base 0 Address[31:4] for S.L.**
3:0	RO	0h	**GFX's Memory Base 0 Address[3:0] for S.L.**

Offset Address: CF-CCh (D0F0)
GFX Shadow Memory Base 1 - MMIO **Default Value: FFF0 0000h**

Bit	Attribute	Default	Description
31:20	RW	FFFh	**GFX's Memory Base 1 Address[31:20] for MMIO**
19:0	RO	0	**GFX's Memory Base 1 Address[19:0] for MMIO**

Offset Address: D0-FDh (D0F0) - Reserved

Offset Address: FEh (D0F0)
Internal GFX Related Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Enable Base VGA 16 bits Decode** 0: All VGA alias range will be forwarded 1: Only forward base VGA range (Alias range will not be forwarded)
3:2	RO	0	**Reserved**
1	RW	0	**Internal GFX Memory Space Access Control for MMIO (RM1BS~M1LM)** 0: Disable. The cycle which belongs to GFX MMIO memory address range will not be passed to Internal GFX. 1: Enable. The cycle which belongs to GFX MMIO memory address range will be passed to Internal GFX.
0	RW	0	**Internal GFX Memory Space Access Control for S.L. (RM0BS~M0LM)** 0: Disable. The cycle which belongs to S.L memory address range will not be passed to Internal GFX. 1: Enable. The cycle which belongs to S.L memory address range will be passed to Internal GFX.

Offset Address: FFh (D0F0) - Reserved

Device 0 Function 1 (D0F1): Error Reporting

Header Registers (00-3Fh)

Offset Address: 01-00h (D0F1)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F1)

Device ID **Default Value: 1353h**

Bit	Attribute	Default	Description
15:0	RO	1353h	**Device ID Code**

Offset Address: 05-04h (D0F1)

PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0 (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F1)
PCI Status **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR# asserted)**
13	RO	0	**Received Master-Abort (except special cycle)** 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error** This bit is set when bus master PERR# is asserted or observed ; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as A Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F1)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Chip Revision ID**

Offset Address: 0B-09h (D0F1)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F1)
Class Code **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cacheline Size**

Offset Address: 0Dh (D0F1)
PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**PCI Bus Time Slice for CPU as a Master** (in Unit of PCI Clocks)
2:0	RO	0	**Reserved** Bit [2:1] are programmable; however, it's read as 0.

Offset Address: 0Eh (D0F1)
Header Type **Default Value: 00 or 80h**

Bit	Attribute	Default	Description
7:0	RO	00 or 80h	**Header Type** Could be 80 when D0F0 Rx4F[0] = 1

Offset Address: 0Fh (D0F1)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST Support** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 10-2Bh (D0F1) – Reserved

Offset Address: 2D-2Ch (D0F1)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F1)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F1) – Reserved

Offset Address: 34h (D0F1)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** An offset address from the start of the configuration space

Offset Address: 35-5Fh (D0F1) – Reserved

Host Bus Error Report (60-6Fh)

Offset Address: 60h (D0F1)

Host Parity Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Host Address Parity Error Detected** 0: Not detected 1: Detected
6	RW1C	0	**Host Data Parity Error Detected** 0: Not detected 1: Detected
5	RW1C	0	**AGP Access Above 4G Detected** 0: No above 4GB AGP cycles being detected 1: AGP Access Above 4GB detected
4	RW1C	0	**Host LOCK Cycle to PCI Detected** 0: Not detected 1: Detected
3:0	RO	0	**Reserved**

Offset Address: 61-67h (D0F1) – Reserved

Offset Address: 68h (D0F1)

Host Parity Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Parity Test Mode** 0: Disable (normal mode) 1: Enable (invert the parity bit)
2:0	RO	0	**Reserved**

Offset Address: 69-FFh (D0F1) – Reserved

Device 0 Function 2 (D0F2): Host Bus Control

Header Registers (00-3Fh)

Offset Address: 01-00h (D0F2)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F2)

Device ID **Default Value: 2353h**

Bit	Attribute	Default	Description
15:0	RO	2353h	**Device ID Code**

Offset Address: 05-04h (D0F2)

PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0 (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F2)
PCI Status **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error** (SERR# asserted)
13	RW1C	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort.
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RW1C	0	**Master Data Parity Error** This bit is set when bus Master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F2)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Chip Revision ID**

Offset Address: 0B-09h (D0F2)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F2) – Reserved

Offset Address: 0Dh (D0F2)
PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**PCI Bus Time Slice for CPU as a Master** (in Unit of PCI clocks)
2:0	RO	0	**Reserved** Bit[2:1] is programmable; however, it's read as 0.

Offset Address: 0Eh (D0F2)
Header Type **Default Value: 00 or 80h**

Bit	Attribute	Default	Description
7:0	RO	00 or 80h	**Header Type** Could be 80 when D0F0 Rx4F[0] = 1

Offset Address: 0Fh (D0F2)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST Support** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 10-2Bh (D0F2) – Reserved

Offset Address: 2D-2Ch (D0F2)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F2)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F2) – Reserved

Offset Address: 34h (D0F2)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** An offset address from the start of the configuration space

Offset Address: 35-4Fh (D0F2) – Reserved

Host CPU Control (50-5Fh)

Offset Address: 50h (D0F2)

Request Phase Control **Default Value: n0h**

Bit	Attribute	Default	Description
7	RO	dip	**IOQ (In-Order Queue) Depth** 0: 1 level 1: 12 levels (or 8 levels. Please refer to Rx55[7] for details.) Default sets from the inverse of the SYSIDLE signal during system initialization. For strap pin information, check the Strap Pin table for details.
6	RO	dip	**Dual CPU** 0: Single CPU 1: Dual CPU Default sets from the inverse of the PDA1 signal during system initialization. For strap pin information, check the Strap Pin table for details.
5	RW	0	**Fast ADS Assertion to DRAM Controller** 0: Disable 1: Enable
4:0	RW	0	**Dynamic Defer Snoop Stall Count** Value for the Defer Snoop Stall Counter. The timer starts counting at the beginning of the snoop phase of C2P cycle; it increases one for every 2 HCLKs. If the C2P cycle is pending when the timer expires, and there are pending ADS, a Defer/Retry response will be replied to the host. For medium decoding PCI slave device; the optimal value for bit[4:0] is 8.

Table 2. Dynamic Defer Snoop Stall Table

Timer Expire	New Pending ADS	PCI Completion	Action
No	-	No	Snoop stall till PCI complete
No	-	Yes	Normal Data Response
Yes	No	No	Snoop stall till either arrival of new pending ADS or PCI complete
Yes	No	Yes	Normal Data Response
Yes	Yes	No	Defer/Retry Response
Yes	Yes	Yes	Normal Data Response

Offset Address: 51h (D0F2)

CPU Interface Control – Basic Option **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Fast Ready for CPU Memory Read Cycle** 0: Disable. Wait until all 8QWs are received before DRDY assertion. 1: Enable. DRDY assertion timing is set up through Rx60-67.
6	RW	0	**Read Around Write** 0: Disable 1: Enable
5	RW	0	**Host Memory Request Queue Control (DXQ)** 0: Disable pipeline ADS assertion 1: Enable pipeline ADS assertion to DRAM controller
4	RW	0	**CPU to PCI Read Defer** 0: Disable 1: Enable
3	RW	0	**2-Entry Defer / Retry Queue Usage** 0: Disable 1: Enable
2	RW	0	**2-Entry Defer / Retry Queue Sharing Policy** 0: One entry for each host processor 1: Each entry is shared by the two host processors
1	RW	0	**Special Cycle Will Be Regarded as Posted Write Cycles** 0: As posted write cycles 1: As non-posted write cycles
0	RW	0	**IOW Cycles Can Be Deferred** 0: IOW cycles will be deferred 1: Cannot be deferred, only retried

Offset Address: 52h (D0F2)
CPU Interface Control – Advanced Option **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CPU 0WS Read / Write DRAM for Back-to-Back Pipeline Access** 0: Disable 1: Enable
6	RW	0	**HREQ (Host Continuous DRAM Ownership) / HPRI (Host High Priority DRAM Request) Assertion to DRAM Controller** 0: Disable 1: Enable assertion of HREQ / HPRI to DRAM controller for efficient memory utilization / faster memory data access.
5	RO	0	**Enable Pull-up Termination of AGTL+ Output Buffer When Pulling GTL Bus Signal from Voltage Low to Voltage High** 0: Disable 1: Enable Default sets from the inverse of the GPIO3 signal during system initialization. For strap pin information, check the Strap Pin table for details.
4	RO	0	**Reserved**
3	RW	0	**Write Retire Policy After 2 Writes** 0: Disable 1: Enable
2	RW	0	**2-Level Defer Queue With Lock Cycle** 0: Disable 1: Enable
1	RW	0	**Consecutive Speculative Read** 0: Disable 1: Enable
0	RW	0	**Speculative Read** 0: Disable 1: Enable

Offset Address: 53h (D0F2)
Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Host Occupancy Timer** (in unit of 4 HCLKs) Host Occupancy timer guarantees a time slot of bit[7:4] * 4 HCLK for pipelined CPU's ADS.
3:0	RW	0	**Master Occupancy Timer** (in unit of 4 HCLKs) Master Occupancy timer guarantees a time slot of bit[3:0] *4 HCLK for pending master requests.

Offset Address: 54h (D0F2)
Miscellaneous Control 1 **Default Value: n0h**

Bit	Attribute	Default	Description
7:5	RO	dip	**CPU FSB Frequency (Powell)** 000: 100MHz 001: 133MHz 010: 166MHz (auto mode only) 011: 200MHz Others: Reserved Default sets from the GPIO12 and CSTATE1signals during system initialization. For strap pin information, check the Strap Pin table for details.
4	RW	0	**Host 8QW Burst Memory Access** 0: Disable (not supported) 1: Enable This bit must be set to 1.
3	RW	0	**Host-Memory DRDY Assertion 1T Adjustment** 0: Normal mode, no adjustment 1: Special mode This bit's setting should follow Rx60 - Rx67 settings. Check Rx55[1] for details of DRDY assertion adjustment.
2	RW	0	**PCI Master 8QW Burst Memory Access** 0: Disable 1: Enable
1	RW	0	**Memory-to-Host Conversion Circuit** 0: Transparent mode 1: Sync 1T in certain clock phases Transparent mode (default operating mode) is faster than Sync mode.
0	RO	0	**Reserved**

Offset Address: 55h (D0F2)
Miscellaneous Control 2 **Default Value: 20h**

Bit	Attribute	Default	Description
7	RW	0	**Host Interface IOQ Size** **Rx50[7] Rx55[7] Host IF IOQ Size** 0 x 1 1 1 8 1 0 12
6	RO	0	**Reserved**
5	RO	1b	**Reserved** (Do not program)
4	RW	0	**Early Read DRDY Assertion for Host Interface DRDY Table** 0: 2T early 1: 3T early
3	RO	0	**Reserved**
2	RW	0	**Enable Medium Threshold for Write Policy** 0: Disable medium threshold 1: Add a medium threshold (defined by Rx56[7:4]), in Write Queue to enable earlier memory write. Refers to Rx5D for write policy.
1	RW	0	**Host-Memory DRDY Assertion 2T Adjustment** 0: 2T early 1: 2T late This bit is effective when Rx54[3] is 1.
0	RO	0	**Reserved**

Offset Address: 56h (D0F2)
Write Policy 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Medium Threshold for Write Policy**
3	RO	0	**Reserved**
2	RW	0	**TL Request 1T Pipeline** 0: Disable 1: Enable
1	RW	0	**P6IF Will Flush the Post-write Request When HBHIT Asserts** 0: Disable 1: Enable
0	RW	0	**Treat TLPRI as High Priority for P2C Read Cycle in Acquiring Host Bus Ownership** 0: Disable 1: Enable

Offset Address: 57h (D0F2)
Calibration Function **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Enable to Sample 4X HA/HREQ Signals Issued by The Processor in V4 Bus** This bit must be set to 1. 0: Disable (not supported) 1: Enable
1	RW	0	**Auto-calibration Function of HDFWRING to Correct Noisy TE Due to Residual HDSTBP/HDSTBN** 0: Disable 1: Enable
0	RW	0	**Fast TRDY Support** 0: The chipset will never support fast TRDY assertion regardless of the setting of Rx96[3]. 1: When Rx96[3] is set to 1,the chipset supports dynamical fast TRDY assertion in V4 bus.

Offset Address: 58h (D0F2) – Reserved

Offset Address: 59h (D0F2)
CPU Miscellaneous Control 1 **Default Value: 08h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Enable 8QW SDRAM Access for Direct Frame Buffer** 0: 8QW access for direct frame buffer is disabled 1: 8QW access for direct frame buffer is enabled
5:4	RW	0	**Warm CPU Reset (CPURST#) Duration Control** 00: 475ns 01: 1050ns 10: 1425ns 11: 1905ns
3	RW	1b	**Warm CPU Reset (CPURST#) Trigger** Write 0 → 1 transition will trigger warm CPURST# Firmware will have to reset this bit to "0" before trigger another CPURST#.
2	RW	0	**Sync DADS for Better DRAM Access Timing** 0: Disable 1: Enable
1	RO	0	**Report Delay Mode of HCLK** 0: Disable 1: Enable
0	RW	0	**Lowest-Priority IPI (Inter-Processor Interrupt) Support** 0: Disable 1: Enable

Offset Address: 5A-5Bh (D0F2) – Reserved

Offset Address: 5Ch (D0F2)
CPU Miscellaneous Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**APIC Data Bit 11 (D11) Mask** 0: D11 is not masked 1: D11 is masked to 0
3:2	RO	0	**Reserved**
1	RW	0	**APIC Cluster Mode Support** 0: Disable 1: Enable
0	RO	0	**Reserved**

Offset Address: 5Dh (D0F2)
Write Policy 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Write Request High Threshold**
3:0	RW	0	**Write Request Low Threshold**

Table 3. CPU Write Request Policy

Rx51[6]	Rx52[3]	Rx5D[7:4]	Rx5D[3:0]	Write Policy
1	0	x	x	Will not handle write request until FIFO is full
1	1	4	2	Will start processing write request when write request count reaches Rx5D[7:4], and stop processing write request when write request count drops to Rx5D[3:0].

Offset Address: 5Eh (D0F2)
Bandwidth Timers **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Host Bandwidth Timer**
3:0	RW	0	**DRAM Bandwidth Timer**

Offset Address: 5Fh (D0F2)
CPU Miscellaneous Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Enable Reorder Retry Queue** 0: Retried CPU transaction always complete in order 1: Allow second entry of retried (IOW/MEMW) transaction to complete before first queued entry
5:3	RO	0	**Reserved**
2	RW	0	**Host Bandwidth Restriction** 0: Disable 1: Enable Host Bandwidth Timer is set up by Rx5E[7:4].
1	RW	0	**DRAM Bandwidth Restriction** 0: Disable 1: Enable DRAM Bandwidth Timer is set up by Rx5E[3:0].
0	RO	0	**Reserved**

Table 4. Host / DRAM Bandwidth Policy

Rx5F[2]	Rx5F[1]	Host / DRAM Bandwidth Setting Policy
0	0	Disable the new DRAM/Host Bandwidth Arbiter
0	1	Use the DRAM Bandwidth Timer only
1	0	Use the HOST Bandwidth Timer only
1	1	Dynamically toggles between the two timers: Host and DRAM bandwidth timers. Both timers, Rx5E[7:4] and Rx5E[3:0] are used by the arbitration logic.

Host Interface DRDY Timing Control (60-6Fh)

Offset Address: 60h (D0F2)

DRDY Timing Control 1 for Read Line Access **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Read Line Phase 4 Wait State** The number of wait states should be added into this phase. (n wait states mean nT delay)
5:4	RW	0	**Read Line Phase 3 Wait State** See the bit descriptions above.
3:2	RW	0	**Read Line Phase 2 Wait State** See the bit descriptions above.
1:0	RW	0	**Read Line Phase 1 Wait State** See the bit descriptions above.

Offset Address: 61h (D0F2)

DRDY Timing Control 2 for Read Line Access **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Read Line Phase 8 Wait State** Refer to Rx60[7:6] bit descriptions for details.
5:4	RW	0	**Read Line Phase 7 Wait State** Refer to Rx60[7:6] bit descriptions for details.
3:2	RW	0	**Read Line Phase 6 Wait State** Refer to Rx60[7:6] bit descriptions for details.
1:0	RW	0	**Read Line Phase 5 Wait State** Refer to Rx60[7:6] bit descriptions for details.

Offset Address: 62h (D0F2)

DRDY Timing Control 3 for Read Line Access **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	0	**Read Line Phase 10 Wait State** Refer to Rx60[7:6] bit descriptions for details.
1:0	RW	0	**Read Line Phase 9 Wait State** Refer to Rx60[7:6] bit descriptions for details.

Offset Address: 63h (D0F2)

DRDY Timing Control 1 for Read Quad-Word Access **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Read QW Phase 4 Wait State** Refer to Rx60[7:6] bit descriptions for details.
5:4	RW	0	**Read QW Phase 3 Wait State** Refer to Rx60[7:6] bit descriptions for details.
3:2	RW	0	**Read QW Phase 2 Wait State** Refer to Rx60[7:6] bit descriptions for details.
1:0	RW	0	**Read QW Phase 1 Wait State** Refer to Rx60[7:6] bit descriptions for details.

Offset Address: 64h (D0F2)

DRDY Timing Control 2 for Read Quad-Word Access **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Read QW Phase 8 Wait State** Refer to Rx60[7:6] bit descriptions for details.
5:4	RW	0	**Read QW Phase 7 Wait State** Refer to Rx60[7:6] bit descriptions for details.
3:2	RW	0	**Read QW Phase 6 Wait State** Refer to Rx60[7:6] bit descriptions for details.
1:0	RW	0	**Read QW Phase 5 Wait State** Refer to Rx60[7:6] bit descriptions for details.

Offset Address: 65h (D0F2)

DRDY Timing Control 3 for Read Quad-Word Access **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	0	**Read QW Phase 10 Wait State** Refer to Rx60[7:6] bit descriptions for details.
1:0	RW	0	**Read QW Phase 9 Wait State** Refer to Rx60[7:6] bit descriptions for details.

Offset Address: 66h (D0F2)

Burst DRDY Timing Control 1 for Read Line Access **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Phase 8 Wait State** Refer to Rx60[7:6] bit descriptions for details.
6	RW	0	**Phase 7 Wait State** Refer to Rx60[7:6] bit descriptions for details.
5	RW	0	**Phase 6 Wait State** Refer to Rx60[7:6] bit descriptions for details.
4	RW	0	**Phase 5 Wait State** Refer to Rx60[7:6] bit descriptions for details.
3	RW	0	**Phase 4 Wait State** Refer to Rx60[7:6] bit descriptions for details.
2	RW	0	**Phase 3 Wait State** Refer to Rx60[7:6] bit descriptions for details.
1	RW	0	**Phase 2 Wait State** Refer to Rx60[7:6] bit descriptions for details.
0	RW	0	**Phase 1 Wait State** Refer to Rx60[7:6] bit descriptions for details.

Offset Address: 67h (D0F2)

Burst DRDY Timing Control 2 for Read Line Access **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Phase 10 Wait State** Refer to Rx60[7:6] bit descriptions for details.
4	RW	0	**Phase 9 Wait State** Refer to Rx60[7:6] bit descriptions for details.
3:0	RO	0	**Reserved**

Offset Address: 68h (D0F2)
APIC CPU Priority 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#0**

Offset Address: 69h (D0F2)
APIC CPU Priority 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#1**

Offset Address: 6Ah (D0F2)
APIC CPU Priority 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#2**

Offset Address: 6Bh (D0F2)
APIC CPU Priority 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#3**

Offset Address: 6Ch (D0F2)
APIC CPU Priority 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#4**

Offset Address: 6Dh (D0F2)
APIC CPU Priority 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#5**

Offset Address: 6Eh (D0F2)
APIC CPU Priority 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#6**

Offset Address: 6Fh (D0F2)
APIC CPU Priority 7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Priority of CPU ID#7**

Host AGTL+ I/O Circuit (70–8Fh)

Offset Address: 70h (D0F2)

Host Address Pad Pullup Driving **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Address Strobe Pad Pullup Driving – (HADSTB1#, HADSTB0#)**
3	RO	0	**Reserved**
2:0	RW	0	**Address Pad Pullup Driving – (HA[30, 16:03]#, HREQ[2:0]#)**

Offset Address: 71h (D0F2)

Host Address Pad Pulldown Driving **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Address Strobe Pad Pulldown Driving – (HADSTB1#, HADSTB0#)**
3	RO	0	**Reserved**
2:0	RW	0	**Address Pad Pulldown Driving – (HA[30, 16:03]#, HREQ[2:0]#)**

Offset Address: 72h (D0F2)

Host Data Pad (4x) Pullup Driving **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Reserved**
6:4	RW	0	**4X Data Strobe Pad Pulldup Driving – (HDSTB[3:0]N#, HDSTB[3:0]P#)**
3	RW	0	**Reserved**
2:0	RW	0	**4X Data Pad Pullup Driving – (HD[63:0]#, HDBI[3:0]#)**

Offset Address: 73h (D0F2)

Host Data Pad (4x) Pulldown Driving **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**4X Data Strobe Pad Pulldown Driving – (HDSTB[3:0]N#, HDSTB[3:0]P#)**
3	RO	0	**Reserved**
2:0	RW	0	**4X Data Pad Pulldown Driving – (HD[63:0]#, HDBI[3:0]#)**

Offset Address: 74h (D0F2)

Host Data / Address Interface Timing Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Output Stagger Delay on HD[63:48]#, HD[31:16]#, HDBI[3,1]#, HDSTB3P#, HDSTB3N#, HDSTB1P#, HDSTB1N#** 0: No delay 1: 0.5 ns delay
4	RW	0	**HA30# Output Stagger Delay** 0: No delay 1: 0.5 ns delay
3:2	RO	0	**Reserved**
1:0	RW	0	**AGTL+ 1X Pad Extra Output Delay** 00: No delay 01: 0.1 ns 10: 0.2 ns 11: 0.3 ns

Offset Address: 75h (D0F2)

AGTL+ I/O Configuration 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**AGTL+ Slew Rate** 0: Disable 1: Enable
4:3	RO	0	**Reserved**
2	RW	0	**Behavior Control of AGTL+ Pull-up Termination for STROBE Signal** 0: Pull-up termination of AGTL+ output buffer will be open-drained when driving STROBE signal of GTL bus from high to low. 1: Pull-up termination of AGTL+ output buffer will function as a current –sharing impedance, as well as the other pull-up termination of AGTL+ output buffer at the processor side when driving STROBE signal of GTL bus from high to low to uplift the low voltage of STORBE signal of GTL bus.
1	RW	0	**Behavior Control of AGTL+ Pull-up Termination for DATA Signal** 0: Pull-up termination of AGTL+ output buffer will be open-drained when driving DATA signal of GTL bus from high to low. 1: Pull-up termination of AGTL+ output buffer will function as a current –sharing impedance, as well as the other pull-up termination of AGTL+ output buffer at the processor side when driving DATA signal of GTL bus from high to low to uplift the low voltage of DATA signal of GTL bus.
0	RO	0	**Reserved**

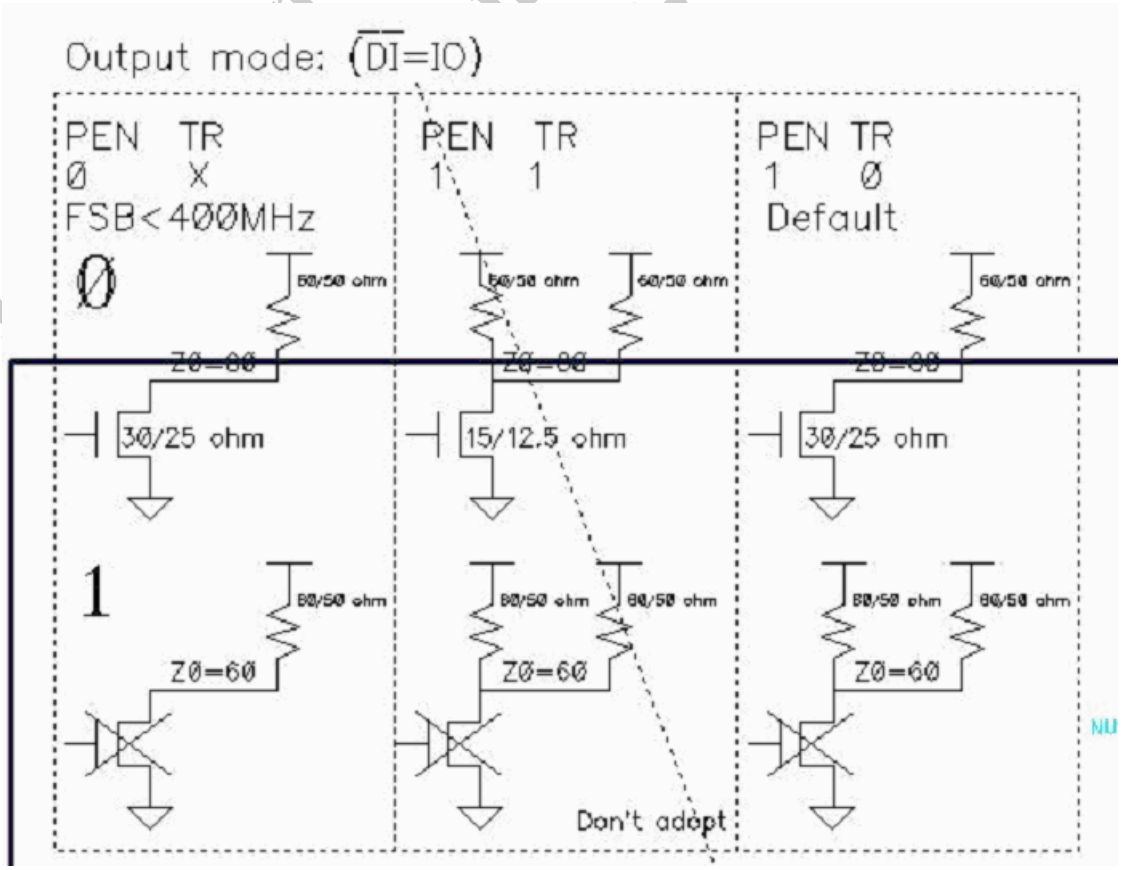
Equivalent Circuit Illustration of GTL IO Buffer Output Mode Control:

All the information is based on Rx52[5] and Rx75[2] / Rx75[1]

Rx52[5] attaches to PEN port of GTL IO Buffer (for DATA & STROBE)
Rx75[2] attaches to TR port of GTL IO Buffer (for STROBE)
Rx75[1] attaches to TR port of GTL IO Buffer (for DATA)

Drive GTL bus signal from voltage-high to voltage-low

Drive GTL bus signal from voltage-low to voltage-high



Offset Address: 76h (D0F2)
AGTL+ I/O Configuration 2 **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	1b	**Power Down Input Comparators of AGTL+ IO Buffers When Entering S3 State (Suspend to DRAM State)** 0: Disable 1: Enable
2	RO	1b	**Reserved** (Do not program)
1	RW	0	**Disable DBI Function** 0: Enable DBI 1: Disable DBI (DBI always high including DBI double-check)
0	RW	0	**DBI Functional Mode** 0: Minimize data change count (through data comparison with previous data) 1: Minimize AGTL+ pulldown count

Offset Address: 77h (D0F2) – Reserved

Offset Address: 78h (D0F2)
2X AGTL+ Auto Compensation Offset **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**2X AGTL+ IO Pad Driving Offset to Compensation PMOS Result**
3:0	RW	0	**2X AGTL+ IO Pad Driving Offset to Compensation NMOS Result**

Offset Address: 79h (D0F2)
4X AGTL+ Auto Compensation Offset **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**4X AGTL+ IO Pad Driving Offset to Compensation PMOS Result**
3:0	RW	0	**4X AGTL+ IO Pad Driving Offset to Compensation NMOS Result**

Offset Address: 7Ah (D0F2)
AGTL Compensation Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Auto-Compensation Driving** 0: Disable auto mode 1: Enable auto mode
6:4	RO	0	**GTL Compensation Result**
3	RO	0	**Reserved**
2:0	RO	0	**GTL Compensation Result**

Offset Address: 7Bh (D0F2)

Input Host Address / Host Strobe Delay Control for HA Group **Default Value: 18h**

HA lower address group definitions:

HA30#
HA[16:03]#
HREQ[2:0]#

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	001b	**Host Address Input Delay Relative to Host Address Strobe for HA Lower Address Group** 000: delay(data) = delay(strobe) – 200 ps 001: delay(data) = delay(strobe) – 150 ps 010: delay(data) = delay(strobe) – 100 ps 011: delay(data) = delay(strobe) – 50 ps 100: delay(data) = delay(strobe) 101: delay(data) = delay(strobe) + 50 ps 110: delay(data) = delay(strobe) + 100 ps 111: delay(data) = delay(strobe) + 150 ps
3	RO	1b	**Reserved** (Do not program)
2:0	RO	0	**Reserved**

Offset Address: 7Ch (D0F2)

Output Delay Control of PAD for HA Group **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	0	**HA[30, 16:03]#,HREQ[2:0]# Extra Delay for Output** 00: 0 ps 01: 100 ps 10: 200 ps 11: 300 ps
3:2	RW	0	**HADSTB1# Extra Delay for Output** 00: 0 ps 01: 100 ps 10: 200 ps 11: 300 ps
1:0	RW	00b	**HADSTB0# Extra Delay for Output** 00: 0 ps 01: 100 ps 10: 200 ps 11: 300 ps

Offset Address: 7Dh (D0F2)

Host Address / Address Clock Output Delay Control **Default Value: AAh**

Bit	Attribute	Default	Description
7:6	RW	10b	**Output Delay of HA Lower Address Group Signals** Delay the output at the physical macro before driven into the host bus. 00: – 150 ps 01: 0 ps 10: 150 ps 11: 300 ps The suggested value is 01b.
5:4	RW	10b	**Output Delay of HADSTB0# Signal** Delay the output at the physical macro before driven into the host bus. 00: – 150 ps 01: 0 ps 10: 150 ps 11: 300 ps The suggested value is 01b.
3:0	RO	1010b	**Reserved** (Do not program)

Offset Address: 7Eh (D0F2)

Host Address CKG Rising / Falling Time Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Falling Time Output Delay of HA Lower Address Group Signals*** Delay the output at the physical macro before driven into the host bus. 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
5:4	RW	00b	**Rising Time Output Delay of HA Lower Address Group Signals*** Delay the output at the physical macro before driven into the host bus. 00: Typical, rising edge transition time < 50 ps 01: Rising edge transition time: 100 ps 10: Rising edge transition time: 200 ps 11: Rising edge transition time: 300 ps
3:0	RO	0	**Reserved**

* : Refer to the HA lower address group definitions of Rx7B.

Offset Address: 7Fh (D0F2)

Host Address Clock CKG Rising / Falling Time Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**HASTB0N# Falling Time Delay** 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
5:4	RW	00b	**HADSTB0# Falling Time Delay** 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
3:0	RO	0	**Reserved**

Offset Address: 80h (D0F2)

Host Data / Strobe Input Delay Control 1 **Default Value: 33h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	011b	**Host Data Input Delay Relative to Host Data Strobe for HD/HDBI Group 1** 000: delay(data) = delay(strobe) – 200 ps 001: delay(data) = delay(strobe) – 150 ps 010: delay(data) = delay(strobe) – 100 ps 011: delay(data) = delay(strobe) – 50 ps 100: delay(data) = delay(strobe) 101: delay(data) = delay(strobe) + 50 ps 110: delay(data) = delay(strobe) + 100 ps 111: delay(data) = delay(strobe) + 150 ps
3	RO	0	**Reserved**
2:0	RW	011b	**Host Data Input Delay Relative to Host Data Strobe for HD/HDBI Group 0** 000: delay(data) = delay(strobe) – 200 ps 001: delay(data) = delay(strobe) – 150 ps 010: delay(data) = delay(strobe) – 100 ps 011: delay(data) = delay(strobe) – 50 ps 100: delay(data) = delay(strobe) 101: delay(data) = delay(strobe) + 50 ps 110: delay(data) = delay(strobe) + 100 ps 111: delay(data) = delay(strobe) + 150 ps

Offset Address: 81h (D0F2)
Host Data / Strobe Input Delay Control 2 **Default Value: 33h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	011b	**Host Data Input Delay Relative to Host Data Strobe for HD/HDBI Group 3** 000: delay(data) = delay(strobe) – 200 ps 001: delay(data) = delay(strobe) – 150 ps 010: delay(data) = delay(strobe) – 100 ps 011: delay(data) = delay(strobe) – 50 ps 100: delay(data) = delay(strobe) 101: delay(data) = delay(strobe) + 50 ps 110: delay(data) = delay(strobe) + 100 ps 111: delay(data) = delay(strobe) + 150 ps
3	RO	0	**Reserved**
2:0	RW	011b	**Host Data Input Delay Relative to Host Data Strobe for HD/HDBI Group 2** 000: delay(data) = delay(strobe) – 200 ps 001: delay(data) = delay(strobe) – 150 ps 010: delay(data) = delay(strobe) – 100 ps 011: delay(data) = delay(strobe) – 50 ps 100: delay(data) = delay(strobe) 101: delay(data) = delay(strobe) + 50 ps 110: delay(data) = delay(strobe) + 100 ps 111: delay(data) = delay(strobe) + 150 ps

Offset Address: 82h (D0F2)
Output Delay of PAD for HDSTB **Default Value: 33h**

Bit	Attribute	Default	Description
7:6	RW	00b	**HDSTB3P#, HDSTB3N# Extra Output Delay** 00: 0ps 01: 100ps 10: 200ps 11: 300ps
5:4	RW	11b	**HDSTB2P#, HDSTB2N# Extra Output Delay**
3:2	RW	00b	**HDSTB1P#, HDSTB1N# Extra Output Delay**
1:0	RW	11b	**HDSTB0P#, HDSTB0N# Extra Output Delay**

Offset Address: 83h (D0F2)
Output Delay of PAD for HD **Default Value: 33h**

Bit	Attribute	Default	Description
7:6	RW	00b	**HD[63:48]#, HDBI3# Extra Output Delay** 00: 0ps 01: 100ps 10: 200ps 11: 300ps
5:4	RW	11b	**HD[47:32]#, HDBI2# Extra Output Delay**
3:2	RW	00b	**HD[31:16]#, HDBI1# Extra Output Delay**
1:0	RW	11b	**HD[15:00]#, HDBI0# Extra Output Delay**

Offset Address: 84h (D0F2)

Host Data / Strobe CKG Control (Group 0) **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Falling Time Output Delay of HDSTB0N# Signal** 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
5:4	RW	00b	**Falling Time Output Delay of HDSTB0P# Signal** 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
3:2	RW	00b	**Falling Time Output Delay of HD/HDBI Group 0 Signals** Delay the output at the physical macro before driven into the host bus. 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
1:0	RW	00b	**Rising Time Output Delay of HD/HDBI Group 0 Signals** Delay the output at the physical macro before driven into the host bus. 00: Typical, rising edge transition time < 50 ps 01: Rising edge transition time: 100 ps 10: Rising edge transition time: 200 ps 11: Rising edge transition time: 300 ps

Offset Address: 85h (D0F2)

Host Data / Strobe CKG Control (Group 1) **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Falling Time Output Delay of HDSTB1N# Signal** 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
5:4	RW	00b	**Falling Time Output Delay of HDSTB1P# Signal** 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
3:2	RW	00b	**Falling Time Output Delay of HD/HDBI Group 1 Signals** Delay the output at the physical macro before driven into the host bus. 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
1:0	RW	00b	**Rising Time Output Delay of HD/HDBI Group 1 Signals** Delay the output at the physical macro before driven into the host bus. 00: Typical, rising edge transition time < 50 ps 01: Rising edge transition time: 100 ps 10: Rising edge transition time: 200 ps 11: Rising edge transition time: 300 ps

Offset Address: 86h (D0F2)

Host Data / Strobe CKG Control (Group 2) **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Falling Time Output Delay of HDSTB2N# Signal** 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
5:4	RW	00b	**Falling Time Output Delay of HDSTB2P# Signal** 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
3:2	RW	00b	**Falling Time Output Delay of HD/HDBI Group 2 Signals** Delay the output at the physical macro before driven into the host bus. 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
1:0	RW	00b	**Rising Time Output Delay of HD/HDBI Group 2 Signals** Delay the output at the physical macro before driven into the host bus. 00: Typical, rising edge transition time < 50 ps 01: Rising edge transition time: 100 ps 10: Rising edge transition time: 200 ps 11: Rising edge transition time: 300 ps

Offset Address: 87h (D0F2)

Host Data / Strobe CKG Control (Group 3) **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Falling Time Output Delay of HDSTB3N# Signal** 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
5:4	RW	00b	**Falling Time Output Delay of HDSTB3P# Signal** 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
3:2	RW	00b	**Falling Time Output Delay of HD/HDBI Group 3 Signals** Delay the output at the physical macro before driven into the host bus. 00: Typical, falling edge transition time < 50 ps 01: Falling edge transition time: 100 ps 10: Falling edge transition time: 200 ps 11: Falling edge transition time: 300 ps
1:0	RW	00b	**Rising Time Output Delay of HD/HDBI Group 3 Signals** Delay the output at the physical macro before driven into the host bus. 00: Typical, rising edge transition time < 50 ps 01: Rising edge transition time: 100 ps 10: Rising edge transition time: 200 ps 11: Rising edge transition time: 300 ps

Offset Address: 88-8Fh (D0F2) – Reserved

Miscellaneous Control (90–9Eh)

Offset Address: 90h (D0F2)

Miscellaneous Control 3 **Default Value: 08h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Disable Continuous Data Pop to Host Bus** 0: Enable continuous data pop to host bus 1: Disable continuous data pop to host bus
4	RW	0	**Add One Pipe When Issuing Speculative Read** 0: Disable 1: Enable
3	RO	1b	**Reserved** (Do not program)
2	RO	0	**Reserved**
1:0	RW	00b	**Control DRAM Read Ready Signal** 00: 2T early RRDY 01: 3T early RRDY 10: 4T early RRDY 11: 5T early RRDY

Offset Address: 91-95h (D0F2) – Reserved

Offset Address: 96h (D0F2)

Miscellaneous Control 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**V4 Fast TRDY Mode** 0: Disable 1: Enable
2	RO	0	**Reserved**
1	RW	0	**HDPWR# Assertion Policy** 0: Always assert HDPWR# (no gating) 1: Dynamic HDPWR# assertion (Dynamic gating)
0	RW	0	**HDPWR# Assertion Control** (Activate if bit 1is enabled) 0: Assert HDPWR# for both read / write cycles 1: Assert HDPWR# for read or APIC write cycles

Offset Address: 97h (D0F2)

APIC Related Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Pipeline APIC / Master Transaction** 0: APIC requests will not be pipelined with master requests. 1: APIC requests can be pipelined with normal master requests. **This bit must be set to 0.**
0	RW	0	**Redirect Lowest Priority APIC Requests to CPU0** (i.e. CPU0 is treated as the lowest priority processor) 0: Disable 1: Enable.

Offset Address: 98-9Dh (D0F2) – Reserved

Offset Address: 9Eh (D0F2)

Miscellaneous Control 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Miscellaneous Control** 0: Turn-off unused pad in V4 bus 1: Turn-on unused pad in V4 bus

Offset Address: 9F-FFh (D0F2) – Reserved

Device 0 Function 3 (D0F3): DRAM Bus Control

There are three DDR2 DRAM controllers in this chip.
- Channel A: It can be 64 or 32 bits decided by Rx6C[5], and can also be used as the system memory.
- Channel C: It is dedicated to 16 bits, and can also store still display data in the snapshot mode.

All registers in Device 0 Function 3 are implemented in Powell. For the register setting of DRAM channels, please refer to the following table.

Table 5. Programming Setting for DRAM Channels

DRAM Mode		Rx6C[2]	Rx6C[5] for Channel A	RxDB[7]
Channel A	Channel C			
64-bit	N/A	1	0	0
32-bit	N/A	1	1	0
64-bit	16-bit	0	0	1
32-bit	16-bit	0	1	1

DRAM channel selection and dynamic clock setting:
For Channel A only –
D0F3 Rx6C[2] = 1
D0F4 RxA2[6] = 1
D0F4 RxA2[5] = 1

Header Registers (00–3Fh)

Offset Address: 01-00h (D0F3)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 03-02h (D0F3)
Device ID **Default Value: 3353h**

Bit	Attribute	Default	Description
15:0	RO	3353h	**Device ID**

Offset Address: 05-04h (D0F3)

PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0 (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RO	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F3)

PCI Status **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error** (SERR# asserted)
13	RW1C	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort.
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RW1C	0	**Master Data Parity Error** This bit is set when bus Master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F3)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D0F3)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	Class Code

Offset Address: 0Ch (D0F3) – Reserved

Offset Address: 0Dh (D0F3)
Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	Latency Timer

Offset Address: 0Eh (D0F3)
Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	Header Type

Offset Address: 0Fh (D0F3)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	BIST

Offset Address: 10-13h (D0F3) – Reserved

Offset Address: 2D-2Ch (D0F3)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	Subsystem Vendor ID

Offset Address: 2F-2Eh (D0F3)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	Subsystem ID

Offset Address: 30-33h (D0F3) – Reserved

Offset Address: 34h (D0F3)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	Capability Pointer

Offset Address: 37-3Fh (D0F3) – Reserved

DRAM Rank (Row) Ending / Beginning Address (40–4Fh)

Offset Address: 40h (D0F3)
DRAM Rank 0 Ending Address **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RW	01h	Virtual Rank 0 Ending Address (Host Address Bits[33:26])

Offset Address: 41h (D0F3)
DRAM Rank 1 Ending Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Virtual Rank 1 Ending Address (Host Address Bits[33:26])

Offset Address: 42h (D0F3)
DRAM Rank 2 Ending Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Virtual Rank 2 Ending Address (Host Address Bits[33:26]

Offset Address: 43h (D0F3)
DRAM Rank 3 Ending Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Virtual Rank 3 Ending Address (Host Address Bits[33:26])

Offset Address: 44-47h (D0F3) – Reserved

Offset Address: 48h (D0F3)
DRAM Rank 0 Beginning Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Virtual Rank 0 Beginning Address (Host Address Bits[33:26])

Offset Address: 49h (D0F3)
DRAM Rank 1 Beginning Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Virtual Rank 1 Beginning Address (Host Address Bits[33:26])

Offset Address: 4Ah (D0F3)
DRAM Rank 2 Beginning Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Virtual Rank 2 Beginning Address (Host Address Bits[33:26])

Offset Address: 4Bh (D0F3)
DRAM Rank 3 Beginning Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	Virtual Rank 3 Beginning Address (Host Address Bits[33:26])

Offset Address: 4C-4Fh (D0F3) – Reserved

MA Map / Command Rate (50–53h)

Offset Address: 51-50h (D0F3)

DRAM MA Map Type **Default Value: 2022h**

Bit	Attribute	Default	Description
15:13	RW	001b	**Rank 0 of Channel C MA Map Type (see the following table)**
12	RW	0	**Rank 0 of Channel C 1T Command Rate** 0: Disable (2T command) 1: 1T command
11:8	RO	0	**Reserved**
7:5	RW	001b	**Rank 0/1 MA Map Type**
4	RW	0	**Rank 0/1 1T Command Rate** 0: Disable (2T command) 1: 1T command
3:1	RW	001b	**Rank 2/3 MA Map Type**
0	RW	0	**Rank 2/3 1T Command Rate** 0: Disable (2T command) 1: 1T command

Table 6. Rank MA Map Type Table

Rank MA Map Type	000	001	010	011	100	101	110	111
Bank Address Bits	2	2	2	2	Rsvd	3	3	3
Row Address Bits	13-12	14-12	15-12	15-13		15-12	15-12	15-13
Column Address Bits	9	10	11	12		10	11	12
DRAM Size (Byte)	128M-64M	512M-128M	2G-256M	4G-1G		2G-256M	4G-512M	8G-2G

Offset Address: 52h (D0F3)

Bank Interleave Address Select **Default Value: 11h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	001b	**BA0 Address Select** Refer to DRAM Bank Address table below for details.
3	RO	0	**Reserved**
2:0	RW	001b	**BA1 Address Select** Refer to DRAM Bank Address table below for details.

Offset Address: 53h (D0F3)

Bank / Rank Interleave Address Select – Channel A Only **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**BA2 Support** Must be enabled if any 8-bank device exists. 0: Disable 1: Enable
6:4	RW	001b	**BA2 Address Select** Refer to the DRAM Bank Address table below for details.
3:2	RW	00b	**Rank Interleave Address Bit 1 (RA1) Select** Refer to the DRAM Interleave Address table below for details.
1:0	RW	00b	**Rank Interleave Address Bit 0 (RA0) Select** Refer to the DRAM Interleave Address table below for details.

Table 7. DRAM Bank Address Table

	000	001	010	011	100	101	110	111
Rx53[6:4] for BA2	A14	A15	A18	A19	rsvd	rsvd	rsvd	rsvd
Rx52[2:0] for BA1	A12	A14	A16	A18	A20	rsvd	rsvd	rsvd
Rx52[6:4] for BA0	rsvd	A13	A15	A17	A19	rsvd	rsvd	rsvd

Table 8. Rank Interleave Address Table

	00	01	10	11
Rx53[3:2] for Rank Interleave Address Bit 1	A14	A16	A18	A20
Rx53[1:0] for Rank Interleave Address Bit 0	A15	A17	A19	A21

Notes. 1. Rank Interleave Address Bit 2 is fixed at A6.
2. BA2, BA1, BA0, INLV1, INLV0 should select 5 different address bits for Rx53[7] =1.
3. BA1, BA0, INLV1, INLV0 should select 4 different address bits for Rx53[7] =0.

Physical-to-Virtual Rank Mapping (54–57h)

Offset Address: 54h (D0F3)

Physical-to-Virtual Rank Mapping 1 **Default Value: 81h**

Bit	Attribute	Default	Description
7	RW	1b	**Enable Physical Rank 0** 0: Disable 1: Enable
6:4	RW	0	**Virtual Rank Number of Physical Rank 0**
3	RW	0	**Enable Physical Rank 1** 0: Disable 1: Enable
2:0	RW	001b	**Virtual Rank Number of Physical Rank 1**

Note:
1. Inserting the DRAM on DIMM1, please set Rx54[7] =1 and Rx54[3] =1
2. Please enable Rx54[7, 3], Rx55[7, 3] and Rx56[7] while initializing this rank. (MRS cycle for each rank)

Offset Address: 55h (D0F3)

Physical-to-Virtual Rank Mapping 2 **Default Value: 23h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Physical Rank 2** 0: Disable 1: Enable
6:4	RW	010b	**Virtual Rank Number of Physical Rank 2**
3	RW	0	**Enable Physical Rank 3** 0: Disable 1: Enable
2:0	RW	011b	**Virtual Rank Number of Physical Rank 3**

Offset Address: 56h (D0F3)

Physical-to-Virtual Rank Mapping 3 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**Enable Physical Rank 0 of Channel C** 0: Disable 1: Enable
6:0	RO	0	**Reserved**

Offset Address: 57h (D0F3) – Reserved

Virtual Rank Interleave Address Select / Enable (58–5Fh)

Offset Address: 58h (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 0 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Rank #0 Interleave Address Select (RINLV0AS[2:0])** This 3-bits field determines the Rank Interleave Address of Rank #0. If RINLV0ASn is 1 (where n = 0, 1, 2), the corresponding Rank Interleave Address bit of Rank 0 is 1, and vice versa.
3	RO	0	**Reserved**
2:0	RW	0	**Rank #0 Interleave Address Enable (RINLV0AEN[2:0])** 0: Mask 1: Enable This 3-bits field determines if the Rank Interleave Address of Rank #0 to be masked (used) or not. If RINLV0AENn is 0 (where n = 0, 1, 2), the corresponding Rank Interleave Address bit will be masked (ignored), and vice versa.

Offset Address: 59h (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Rank #1 Interleave Address Select** See the description on Rank 0 (Rx58).
3	RO	0	**Reserved**
2:0	RW	0	**Rank #1 Interleave Address Enable** See the description on Rank 0 (Rx58).

Offset Address: 5Ah (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Rank #2 Interleave Address Select** See the description on Rank 0 (Rx58).
3	RO	0	**Reserved**
2:0	RW	0	**Rank #2 Interleave Address Enable** See the description on Rank 0 (Rx58).

Offset Address: 5Bh (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Rank #3 Interleave Address Select** See the description on Rank 0 (Rx58).
3	RO	0	**Reserved**
2:0	RW	0	**Rank #3 Interleave Address Enable** See the description on Rank 0 (Rx58).

Offset Address: 5Ch (D0F3)

Virtual Rank Interleave Address Select / Enable – Rank 0 of Channel B **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	0	**Rank 0 of Channel B Interleave Address Select** See the description on Rank 0 (Rx58).
3	RO	0	**Reserved**
2:0	RW	0	**Rank 0 of Channel B Interleave Address Enable** See the description on Rank 0 (Rx58).

Offset Address: 5D-5Fh (D0F3) – Reserved

Following is an example, which shows a possible register settings for a system with 2 double-sided DIMM installed.

(1) Rx53[3:2] = 2 and Rx53[1:0] =2 selects A6, A18, A19 as the Rank Interleave Address for the system.

(2) If the settings on the Rank Interleave Address Selection of Rank 0, 1, 2, 3 (Rx58-5B[6:4]) are
Rx58[6:4] = 001b
Rx59[6:4] = 000b
Rx5A[6:4] = 010b
Rx5B[6:4] = 011b

And if the Rank Interleave Address Enable of Rank 0, 1, 2, 3 (Rx58-5B[2:0]) are
Rx58[2:0] = 011b
Rx59[2:0] = 011b
Rx5A[2:0] = 011b
Rx5B[2:0] = 011b

With the above register settings, Rank Interleave Address 2, A6, is ignored for the system, and the four ranks of the system are decided by A18 and A19 as shown in the following table.

A18	A19	Selected Rank
0	0	Rank#1
0	1	Rank#0
1	0	Rank#2
1	1	Rank#3

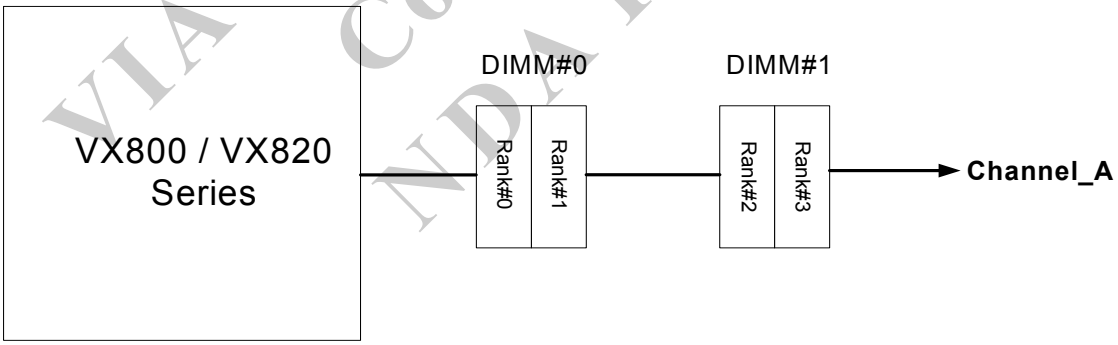


Figure 1. DIMM / Channel Mapping Diagram

DRAM Timing (60–64h)

Offset Address: 60h (D0F3)

DRAM Pipeline Turn-Around Setting **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**0ws Back-to-Back Write to Different DDR Rank** 0: Disable 1: Enable
6	RW	0	**Fast Read-to-Read Turn Around** 0: Disable 1: Enable (DQS post-amble overlap with preamble)
5	RW	0	**Fast Read-to-Write Turn Around** 0: Disable 1: Enable
4	RW	0	**Fast Write-to-Read Turn Around** 0: Disable 1: Enable
3:2	RO	0	**Reserved**
1	RW	0	**0ws DRAM Channel Switching Between Read Cycles** 0: Disable 1: Enable This function is valid in 64-bit mode.
0	RW	0	**0ws DRAM Channel Switching Between Write Cycles** 0: Disable 1: Enable This function is valid in 64-bit mode.

Offset Address: 61h (D0F3)

DRAM Timing for All Ranks 1 **Default Value: 04h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Active-to-Active Period (tRRD)** 00: 2T 01: 3T 10: 4T 11: 5T
5:0	RW	04h	**Refresh-to-Active or Refersh-to-Refresh (tRFC)** 00h: 8T 01h: 9T … 0nh: (8+n)T 3eh: 70T 3f:h: 71T

Offset Address: 62h (D0F3)

DRAM Timing for All Ranks 2 **Default Value: 21h**

Bit	Attribute	Default	Description
7:4	RW	0010b	**Active-to-Precharge (tRAS)** 0000: 5T 0001: 6T … 0nh: (5+n)T 1110: 19T 1111: 20T
3	RW	0	**Enable DDR2 8-Bank Device Timing Constraint (tRRD and tRP)**
2:0	RW	001b	**CAS Latency** DDR DDR2 000 1.5 2 001 2 3 010 2.5 4 011 3 5 1xx reserved 6

Offset Address: 63h (D0F3)
DRAM Timer for All Ranks 3 **Default Value: 20h**

Bit	Attribute	Default	Description
7:5	RW	001b	**Write Recovery Time (tWR)** 000: 2T 001: 3T 010: 4T 011: 5T 100: 6T Others: reserved
4	RO	0	**Reserved**
3	RW	0	**Read-to-Precharge Delay (tRTP)** 0: 2T 1: 3T
2	RO	0	**Reserved**
1:0	RW	00b	**Write to Read Command Delay (tWTR)** DDR DDR2 00 1T 2T 01 2T 3T 10 3T 4T 11 4T 5T

Offset Address: 64h (D0F3)
DRAM Timer for All Ranks 4 **Default Value: 22h**

Bit	Attribute	Default	Description
7:5	RW	001b	**Active to Read or Write Delay (tRCD)** 000: 2T 001: 3T 010: 4T 011: 5T 100: 6T Others: reserved
4	RW	0	**CKE Minimum Pulse Width** 0: 2T 1: 3T This function is valid when Dynamic CKE, D0F4 RxA1[6], is set to 1.
3:1	RW	001b	**Precharge Period (tPR)** 000: 2T 001: 3T 010: 4T 011: 5T 100: 6T Others: reserved
0	RW	0	**Exit Precharge/Active Power Down to Any Command Delay** 0: 1T 1: 2T This function is valid when Dynamic CKE, D0F4 RxA1[6], is set to 1.

DRAM Queue / Arbitration (65–67h)

Offset Address: 65h (D0F3)

DRAM Arbitration Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**AGP Timer** (unit of 4 DCLKS) DRAMC time slot allocated for AGP device. Active when there is pending memory requests from other requesters.
3:0	RW	0	**Host Timer** (unit of 4 DCLKS) DRAMC time slot allocated for Host. Active when there is pending memory requests from other requesters.

Offset Address: 66h (D0F3)

DRAM Queue / Arbitration **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DRAMC Queue Size Greater Than 2** 0: No 1: Yes
6	RW	0	**DRAMC Queue Size Not Equal To 4** 0: No 1: Yes To setup DRAMC queue size of 2, set Rx66[7:6] to 00b; set Rx66[7:6] to 11b for queue size of 3; set Rx[7:6] to 10b for queue size of 4.
5:4	RW	00b	**Arbitration Parking Policy** 00: Park at the last bus owner 01: Park at CPU 10: Park at AGP 11: Park at VGA
3:0	RW	0	**Priority Promotion Timer** (in unit of 4 DCLKs) A DRAM request is promoted to become a high priority request when it is pending over PTIM*4 DRAM cycles.

Offset Address: 67h (D0F3)

DIMM Command / Address Selection **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	00b	**DIMM 1 Command / Address Selection** 00: SCMD/MA Bus A Others: Reserved
1:0	RW	00b	**DIMM 0 Command / Address Selection** 00: SCMD/MA Bus A Others: Reserved

DRAM Control (68–69h)

Offset Address: 68h (D0F3)

DDR2 Page Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DRAM Expired Page Threshold** Close expired pages with precharge-all command when the number of expired pages exceeds the value.
3:0	RW	0	**Page Register Life Timer** (in unit of 16 DCLKs) When timer expired, the expired page will be closed.

Offset Address: 69h (D0F3)

DDR2 Page Control 2 **Default Value: 82h**

Bit	Attribute	Default	Description
7:6	RW	10b	**Bank Interleave – Channel A** 00: No interleave 01: 2-bank 10: 4-bank 11: 8-bank
5	RW	0	**Enable Bank Address Scramble** When set to 1, BA0=A13^A15^A17^A19, BA1=A12^A14^A16^A18^A20
4	RW	0	**Auto-Precharge for TLB Read and CPU Write-Back** 0: Disable 1: Enable
3	RO	0	**Reserved**
2	RW	0	**Promote Priority of Refresh Request** 0: Low 1: High
1	RW	1b	**Keep Page Active When Cross Bank** 0: Disable 1: Enable
0	RW	0	**Multiple Page Mode** 0: Disable 1: Enable

Refresh Control (6A–6Bh)

Offset Address: 6Ah (D0F3)

Refresh Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Refresh Counter** (in unit of 16 DRAM CLKs) When set to 0, DRAM refresh is disabled

Offset Address: 6Bh (D0F3)

DRAM Miscellaneous Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**DQS Input DLL Adjustment** 0: Disable 1: Enable
6	RW	0	**DQS Output DLL Adjustment** 0: Disable 1: Enable
5	RW	0	**Burst Refresh** 0: Disable 1: Enable
4	RW	1b	**DLL Manual Reset** 0: Disable 1: Enable
3	RO	0	**Reserved**
2:0	RW	000b	**SDRAM Operation Mode Select** 000: Normal SDRAM Mode 001: NOP Command Enable 010: All-Banks-Precharge Command Enable 011: MRS to SCMD 100: CBR, CAS-before-RAS refresh, Cycle Enable 101: Reserved 11x: Reserved

DDR SDRAM Control (6C–6Fh)

Offset Address: 6Ch (D0F3)

DRAM Type **Default Value: C0h**

Bit	Attribute	Default	Description
7	RO	1b	**Reserved** (Do not program)
6	RO	1b	**Memory Type Detected** 0: DDR 1: DDR2
5	RW	0	**Enable 32-bit Memory Width Mode – Channel A** 0: Disable 1: Enable
4	RW	0	**Disable DQM Signals** 0: Enable 1: Disable
3	RW	0	**SDRAM Burst Length** For 64-bit mode ranks, SDRAM MRS 0: BL4 1: BL8
2	RW	0	**Channel A Mode** 0: Channel A & Channel C mode 1: Channel A mode
1:0	RO	0	**Reserved**

Offset Address: 6Dh (D0F3)

DQ Channel Select **Default Value: C0h**

Bit	Attribute	Default	Description
7:6	RO	11b	**Reserved** (Do not program)
5:0	RO	0	**Reserved**

Offset Address: 6Eh (D0F3)

DRAM Control **Default Value: 08h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**DRAM Scrubber** Issues a read-modify-write cycle before each REF 0: Disable 1: Enable
5	RW	0	**DRAM Scrubber Redirect** 0: Disable 1: Enable
4	RW	0	**Non-page Mode Support** 0: Disable 1: Enable
3	RW	1b	**Enable 1 Pipeline Stage on DRAM Command Path** 0: Disable 1: Enable 1 pipeline stage on DRAM command (CS/SCMD/MA) path.
2:0	RO	0	**Reserved**

Offset Address: 6Fh (D0F3)

Miscellaneous Control **Default Value: 42h**

Bit	Attribute	Default	Description
7	RW	0	**Non-ONBD Protection for GART Table Fetching** 0: Disable 1: Enable
6	RW	1b	**DRAM-Side-Input-Pointer Non-Return-Zero Mode** 0: Disable 1: Enable Enable to avoid overwrite data
5	RW	0	**Disallow the 2nd Cycle of a 2T Command Overlapped with Command of Different Type on a Different MA/SCMD Bus** 0: Allow 1: Not allow
4	RW	0	**Read-Modify-Write (RMW) Option** When enabled, RMW is processed in relaxed mode.
3	RW	0	**Applying Same-Channel IO Turn-Around Constraints between Different Channels**
2	RW	0	**Exclusive SCMD Buses** When enabled, the two SCMD buses are exclusive. Do not have commands in the same cycle.
1	RW	1b	**Compact Refresh Mode** (skip CS for non-existing rank while refresh) 0: Disable 1: Enable
0	RW	0	**GART Table Access Option** When enabled, GART Table accessing is in relaxed mode.

DRAM Signal Timing Control (70–7Fh)

Offset Address: 70h (D0F3)

DQS Output Delay - Channel A **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**DQS Output Delay**

Offset Address: 71h (D0F3)

MD Output Delay - Channel A **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**MD Output Delay**

Offset Address: 72-73h (D0F3) – Reserved

Offset Address: 74h (D0F3)

DQS Output Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**Initial Phase of Internal Clocks for DQS Output - Channel A** Each steps increase a phase of 1/8 T

Offset Address: 75h (D0F3)

DQ Output Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	0	**Initial Phase of Internal Clocks for DQ (MD) Output - Channel A** Each steps increase a phase of 1/8 T

Offset Address: 76h (D0F3)
Write Data Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**1 More Pipeline Stage on Write Data Path** Will provide safer timing margin.
6	RW	0	**1 More Pipeline Stage on Write Data Path for DDR2-667 and Above** Will provide safer timing margin.
5	RW	0	**MD/DQS Output Clocks Bypass Delay Component** (i.e. when enabled, Rx70-73 becomes functionless)
4	RO	0	**Reserved**
3:2	RW	00b	**Advance Write Phase Signals to Make Room for the Long Bus Delay** 00: Normal mode 01: Advance 1 cycle 10: Advance 2 cycle 11: Forbidden The 2 bits must be used with bit [1:0].
1:0	RW	0	**Write MD/DQS/CAS Output Timing Range Control** Each increased step delays the output range by 1/4 T.

Offset Address: 77h (D0F3)
DQS Input Delay Calibration **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Manual DQS Input Delay Setting** 0: Auto 1: Manual
6	RO	0	**Reserved**
5:0	RW/RO	00h	**DDR DQS Input Delay** This is the base delay value of DQS input signal in unsigned binary format. The reading value depends on Rx77[7]. If Rx77[7] = 0 (auto mode), DLL calibration result is returned when read. When Rx77[7] = 0 , RO When Rx77[7] = 1 , RW

Offset Address: 78h (D0F3)
DQS Input Capture Range Control - Channel A **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**Manual DQS Input Capture Range Setting** 0: Auto 1: Manual
6	RW	0	**Enable DQS Input Capture Range Detection** 0: Disable 1: Enable
5:0	RW	00h	**DQS Input Capture Range** **Bit [5:4]** 00: 1T prior to 1st DQS rising edge 01: At 1st DQS rising edge 10: 1T after 11: Reserved **Bit [3:1]** Each unit adds 1/8T delay **Bit [0]** Add 0.35ns fine tune delay

Offset Address: 79h (D0F3) – Reserved

Offset Address: 7Ah (D0F3)

DQS Input Capture Range Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Select DQS Input Pin as Input Capture Range Detection Signal** 0: DQSA0 1: DQSA4
2:0	RW	0	**DQS Input Capture Range Offset Value - Channel A** 1/8T per step, 2's complement

Offset Address: 7Bh (D0F3)

Read Data Phase Control **Default Value: 02h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	000b	**MD Input Data Push Timing Control** 000: Start moving data into internal buffer 1T after the 1st DRAM strobe 001: 1.5T 010: 2T 011: 2.5T Bit 6 is always 0.
3	RO	0	**Reserved**
2	RW	0	**Read Data Bus from DIO to Data Path Module 1/2T Earlier**
1	RW	1b	**Extend the Seed of DQS Input** 0: Disable (2T) 1: Enable (3T)
0	RW	0	**Extend DQS Input Capture Range 1/2T Earlier**

Read-Only Control (7C-7Fh)

Offset Address: 7Ch (D0F3)

DQS Input Delay Offset Control - Channel A **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:0	RW	00h	**DQS Input Delay Offset (In two's complement)** This is the offset values (in 2's complement format) from the base delay value (Rx77[5:0]) for Channel A DIMM.

Offset Address: 7D-7Fh (D0F3) – Reserved

Shadow RAM Control (80–83h)

Offset Address: 80h (D0F3)

Page-C ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**CC000-CFFFFh Memory Space Access Control** 00: Read from PCI. Write to PCI. 01: Read from PCI. Writer to DRAM. 10: Read from DRAM. Writer to PCI. 11: Read from DRAM. Write to DRAM.
5:4	RW	00b	**C8000-CBFFFh Memory Space Access Control** See bit[7:6] description.
3:2	RW	00b	**C4000-C7FFFh Memory Space Access Control** See bit[7:6] description.
1:0	RW	00b	**C0000-C3FFFh Memory Space Access Control** See bit[7:6] description.

Note: If a non-PCI device claims this cycle, it will be passed to to ROM (ISA/LPC/SPI).

Offset Address: 81h (D0F3)

Page-D ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DC000-DFFFFh Memory Space Access Control** 00: Read from PCI. Write to PCI. 01: Read from PCI. Writer to DRAM. 10: Read from DRAM. Writer to PCI. 11: Read from DRAM. Write to DRAM.
5:4	RW	00b	**D8000-DBFFFh Memory Space Access Control** See bit[7:6] description.
3:2	RW	00b	**D4000-D7FFFh Memory Space Access Control** See bit[7:6] description.
1:0	RW	00b	**D0000-D3FFFh Memory Space Access Control** See bit[7:6] description.

Note: If a non-PCI device claims this cycle, it will be passed to to ROM (ISA/LPC/SPI).

Offset Address: 82h (D0F3)

Page-E ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**EC000-EFFFFh Memory Space Access Control** 00: Read from PCI. Write to PCI. 01: Read from PCI. Writer to DRAM. 10: Read from DRAM. Writer to PCI. 11: Read from DRAM. Write to DRAM.
5:4	RW	00b	**E8000-EBFFFh Memory Space Access Control** See bit[7:6] description.
3:2	RW	00b	**E4000-E7FFFh Memory Space Access Control** See bit[7:6] description.
1:0	RW	00b	**E0000-E3FFFh Memory Space Access Control** See bit[7:6] description.

Note: If a non-PCI device claims this cycle, it will be passed to to ROM (ISA/LPC/SPI).

Offset Address: 83h (D0F3)

Page-F ROM, Memory Hole and SMI Decoding **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	00b	**F0000-FFFFFh Memory Space Access Control** 00: Read from PCI. Write to PCI. 01: Read from PCI. Writer to DRAM. 10: Read from DRAM. Writer to PCI. 11: Read from DRAM. Write to DRAM. If a non-PCI device claims this cycle, it will be passed to to ROM (ISA/LPC/SPI).
3:2	RW	00b	**Memory Hole** 00: None 01: 512K – 640K 10: 15M – 16M (1M) 11: 14M – 16M (2M)
1	RW	0	**Disable Data Access on SMRAM (Page A, B) in SM Mode** 0: In SM mode, page A,B CPU Data R/W cycles are forwarded to the memory controller. 1: In SM mode, page A,B CPU Data R/W cycles are forwarded to the PCI bus Notes: 1. This bit is effective when Rx83[0] is set to 0. 2. SMRAM page A,B Code R/W cycles are always forwarded to the memory controller in SM mode.
0	RW	0	**Enable Page A, B DRAM Access In Normal Mode** 0: Page A, B CPU R/W cycles could be forwarded to memory controller or PCI bus depends on the setting of bit 1, the CPU operating mode (Normal or SM mode) as well as the type (Code or Data) of the CPU cycle. 1: Page A, B CPU R/W cycles (Code and Data) are always (in either Normal or SM mode) forwarded to the memory controller. Check the following table for details.

Table 9. CPU-to-SMRAM Cycle Flow

Rx83[1]	Rx83[0]	CPU MODE	Target of CODE Access Cycle	Target of DATA Access Cycle
x	0	Normal	PCI	PCI
0	0	SMM	DRAM	DRAM
1	0	SMM	DRAM	PCI
x	1	Normal / SMM	DRAM	DRAM

DRAM Above 4G Support (84-8Dh)

Offset Address: 84h (D0F3)

Low Top Address - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Low Top Address - A[23:20]**
3:0	RO	0	**Reserved**

Offset Address: 85h (D0F3)

Low Top Address - High **Default Value: FFh**

Bit	Attribute	Default	Description
7:0	RW	FFh	**Low Top Address – A[31:24]**

Offset Address: 86h (D0F3)

SMM and APIC Decoding **Default Value: 03h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Top SM Memory Size** 00: 1M 01: 2M 10: 4M 11: 8M When Rx86[2] = 1, the SM memory enables.
5	RW	0	**APIC Lowest Interrupt Arbitration** 0: Disable 1: Enable
4	RW	0	**IO APIC Decoding** 0: Cycles accessing FECx_xxxxh are passed to PCI1 1: Cycles accessing FEC7_FFFFh - FEC0_0000h are passed to PCI1; cycles accessing FECF_FFFFh - FEC8_0000h access cycles are passed to PCI2.
3	RW	0	**MSI Support (Processor Message Enable)** 0: Cycles accessing FEEx_xxxxh from masters are passed to PCI1 (PCIC will not claim) 1: Cycles accessing FEEx_xxxxh from masters are passed to the Host side for snooping
2	RW	0	**Enable Top SM Memory** 0: Disable 1: Enable
1	RW	1b	**SDIO Support for Using System Memory 4Kbytes** 0: Disable 1: Enable
0	RW	1b	**Enable Compatible SMM** 0: Disable 1: Enable

Offset Address: 87h (D0F3) – Reserved

Offset Address: 89-88h (D0F3)

The Address Next to the Last DRAM Bank Ending Address **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10:0	RO	0	**The Address Next to the Last Valid DRAM Address**

Offset Address: 8A-8Bh (D0F3) – Reserved

Offset Address: 8Ch (D0F3)

DQS Output Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**MD/DQS Earlier Output Enable** 0: Disable 1: Enable DQ Output Enable (MDOE) 1/2T earlier DQS Output Enable (DQSOE) 1/2T earlier if bit 0 =0
0	RW	0	**DQS Earlier Output Enable** 0: Disable 1: Enable DQSOE 1/4T earlier if bit 1 =1

Offset Address: 8D-8Fh (D0F3) – Reserved

DRAM Clocking Control (90-9Fh)

Offset Address: 90h (D0F3)

DRAM Clock Operation Mode and Frequency **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DCLK Switch to Non-Feedback Mode** 0: Feedback mode 1: Non-feedback mode (feed-forward mode). There is no need to feed DCLKO back through MCLKIN port.
6:3	RO	0	**Reserved**
2:0	RW	000b	**DRAM Operating Frequency** 000: 100MHz 001: 133MHz 010: 166MHz 011: 200MHz 100: 266MHz 101: 333MHz 110: 400MHz 111: Reserved

Offset Address: 91h (D0F3)

DCLK (MCLK) Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Disable DCLKOA for Power Saving Issue** 0: Enable 1: Disable Must set 0 for Rx90[7] = 0 mode and DCLKOA is fed back to DCLKIA
2:0	RW	0	**DCLKOA Phase Select** Each step increases 1/8T

Offset Address: 92h (D0F3)

CS/CKE Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Sampling Clock Delay Select for CS/CKE - Channel A** 0: Bypass delay 1: Delay 0.15ns
2:0	RW	0	**Sampling Clock Phase Select for CS/CKE - Channel A** Each step increases a phase of 1/8 T

Offset Address: 93h (D0F3)

SCMD/MA Clock Phase Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Sampling Clock Delay Select for SCMD/MA - Channel A** 0: Bypass delay 1: Delay 0.15ns
2:0	RW	0	**Sampling Clock Phase Select for SCMD/MA - Channel A** Each step increases a phase of 1/8 T

Offset Address: 94h (D0F3) – Reserved

Offset Address: 95h (D0F3)

By-Rank Self Refresh Related Registers - Channel A **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Check GFX Vertical Blank When Rank3 Enters By-Rank Self Refresh** 0: Not check 1: Check
6	RW	0	**Check Self-Refresh Request When Rank3 Enters By-Rank Self Refresh** 0: Not check 1: Check
5	RW	0	**Check GFX Vertical Blank When Rank2 Enters By-Rank Self Refresh** 0: Not check 1: Check
4	RW	0	**Check Self-Refresh Request When Rank2 Enters By-Rank Self Refresh** 0: Not check 1: Check
3	RW	0	**Check GFX Vertical Blank When Rank1 Enters By-Rank Self Refresh** 0: Not check 1: Check
2	RW	0	**Check Self-Refresh Request When Rank1 Enters By-Rank Self Refresh** 0: Not check 1: Check
1	RW	0	**Check GFX Vertical Blank When Rank0 Enters By-Rank Self Refresh** 0: Not check 1: Check
0	RW	0	**Check Self-Refresh Request When Rank0 Enters By-Rank Self Refresh** 0: Not check 1: Check

Offset Address: 96h (D0F3)

By-Rank Self Refresh Related Registers – Channel A **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	000b	**The Number of Idle Auto-Refresh Before A Rank Will Do By-Rank Self Refresh** 111: This rank will enter self refresh after 7 continuous auto refreshes. 110: This rank will enter self refresh after 6 continuous auto refreshes. 101: This rank will enter self refresh after 5 continuous auto refreshes. 100: This rank will enter self refresh after 4 continuous auto refreshes. 011: This rank will enter self refresh after 3 continuous auto refreshes. 010: This rank will enter self refresh after 2 continuous auto refreshes. 001: This rank will enter self refresh after 1 continuous auto refresh. 000: This rank will enter self refresh after 0 continuous auto refresh.
3	RW	0	**Enable Rank3 to Do By-Rank Self Refresh** 0: Disable 1: Enable
2	RW	0	**Enable Rank2 to Do By-Rank Self Refresh** 0: Disable 1: Enable
1	RW	0	**Enable Rank1 to Do By-Rank Self Refresh** 0: Disable 1: Enable
0	RW	0	**Enable Rank0 to Do By-Rank Self Refresh** 0: Disable 1: Enable

Offset Address: 97h (D0F3) – Reserved

Offset Address: 98h (D0F3)

DRAM Channel Pipeline Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Pipelining Stage on Request Page Decoding** Improve DRAMC internal timing for DDR2-667 and above, but increase latency.
6	RW	0	**2T Page Close Command**
5	RW	0	**2T Command Scheduling** Improve DRAMC internal timing for DDR2-667 and above when Rx50 = 1, but may affect performance.
4	RO	0	**Reserved**
3	RW	0	**2T Internal Active and Precharge Command Scheduling**
2:1	RO	0	**Reserved**
0	RW	0	**CKE Pipeline - Channel A** Enable 1T PIPE for CKEA output to balance internal timing of CKE and SCMD/MA when Rx6E[3] = 0

Offset Address: 99h (D0F3)

DCLKO (MCLK) Phase Control **Default Value: 7Eh**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:1	RW	111111b	**Select MCLKO Output (bit-wise)** If Rx99[6:1] are set to 111111b, all MCLKOA[5:0] will output MCLK. If Rx99[6:1] are set to 001111b, only MCLKOA[3:0] will output MCLK.
0	RW	0	**MCLKOB (Signal Name of DRAM Module Used for Channel C) Output Clock** 0: Disable 1: Enable

Offset Address: 9Ah (D0F3) – Reserved

Offset Address: 9Bh (D0F3)

DRAM MD PADs ODTA[7:4] Pullup / Pulldown Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Enable DRAM MD Pad ODTA[7:4]** 0: Disable ODT unless Rx9B[1] is not equal to 0 1: Enable ODT when reading data
3:2	RO	0	**Reserved**
1	RW	0	**MD PAD ODTA[7:4] Pulldown/Pullup Enable – Channel A** 0: Disable 1: Enable
0	RO	0	**Reserved**

Offset Address: 9Ch (D0F3)

ODT Lookup Table - Channel A **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Rank 3 ODT Signal Selection** 00: ODTA0 01: ODTA1 10: ODTA2 11: ODTA3
5:4	RW	00b	**Rank 2 ODT Signal Selection** See bit [7:6] description.
3:2	RW	00b	**Rank 1 ODT Signal Selection** See bit [7:6] description.
1:0	RW	00b	**Rank 0 ODT Signal Selection** See bit [7:6] description.

Offset Address: 9Dh (D0F3) – Reserved

Offset Address: 9Eh (D0F3)

SDRAM ODT Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DDR2 SDRAM ODT Control** 0: Disable 1: Enable
6	RW	0	**2T Write Command when Rx50 = 1** 0: Disable 1: Enable
5:4	RW	00b	**Add MD Bus Turn-Around Wait State for DDR2 ODT** 00: Disable 01: 1T wait state 10: 2T wait state 11: 3T wait state
3:2	RO	0	**Reserved**
1	RW	0	**Differential DQS Input - Channel C** 0: Disable 1: Enable
0	RW	0	**Differential DQS Input - Channel A** 0: Disable 1: Enable

Offset Address: 9Fh (D0F3)

SDRAM ODT Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DDR2 SDRAM ODT Write Cycle Late Extension** 0: Disable 01: 1T extension 10: 2T extension 11: 3T extension
5:4	RW	00b	**DDR2 SDRAM ODT Read Cycle Late Extension** 00: Disable 01: 1T extension 10: 2T extension 11: 3T extension
3:2	RO	0	**Reserved**
1:0	RW	00b	**DDR2 SDRAM ODT Early Extension** 00: Disable 01: 1T extension 10: 2T extension 11: 3T extension

UMA Registers (A0–AFh)

Offset Address: A1-A0h (D0F3)

CPU Direct Access Frame Buffer Control **Default Value: 00h**

Bit	Attribute	Default	Description
15	RW	0	**Integrated Graphics Enable** 0: Disable 1: Enable
14:12	RW	000b	**System Frame Buffer Size Selection – Channel A** 000: none 001: 8M 010: 16M 011: 32M 100: 64M 101: 128M 110: 256M 111: Reserved
11:1	RW	0	**A[31:21]**
0	RW	0	**CPU Direct Access Frame Buffer Enable** 0: Disable 1: Enable

Offset Address: A2h (D0F3)

VGA Timer 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**VGA High Priority Timer** (in unit of 16 DCLK)
3:0	RW	0	**VGA Timer** (in unit of 16 DCLK)

Offset Address: A3h (D0F3) – Reserved

Offset Address: A5-A4h (D0F3)

GFX Misc. **Default Value: 00h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RW	0	**Reset Internal GFX by BIOS** 0: Not reset 1: Reset
12	RO	0	**Reserved**
11:10	RW	00b	**Fine Tune GFX PCICLK** 00: Default 01: Delay 0.1 ns 10: Early 0.15 ns 11: Early 0.3 ns
9:8	RW	00b	**Fine Tune GFX MCK** 00: Default 01: Delay 0.1 ns 10: Early 0.15 ns 11: Early 0.3 ns
7:3	RO	0	**Reserved**
2	RW	0	**Turn Off All PCIe Lanes to Save Power Consumption** 0: Turn on 1: Turn off
1	RO	0	**Reserved**
0	RW	0	**GFX Data Delay to Sync with Clock** 0: Not sync 1: Sync with clock

Offset Address: A6h (D0F3)

Page Register Life Timer 1 in CPU Power Saving States **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Enable Page Register Life Timer 1 in C4 State** 0: Disable 1: Enable
5	RW	0	**Enable Page Register Life Timer 1 in C3 State** 0: Disable 1: Enable
4	RW	0	**Enable Page Register Life Timer 1 in C2 State** 0: Disable 1: Enable
3:0	RW	0	**Page Register Life Timer 1** (in unit of 4 DCLKs) When timer expires, the expired page will be closed.

Offset Address: A7h (D0F3)

GMINT (GFX-Memory Interface) and GFX Related Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Dynamic Snoop Selection** x0: GMINT dynamic snoop syncs with GFX dynamic snoop signal. 01: GMINT dynamic snoop syncs with GFX read signal. 11: GMINT dynamic snoop syncs with GFX read signal and GFX dynamic snoop signal (suggested value).
5:4	RO	0	**Reserved**
3	RW	0	**VGA Enable – for Address Allocate** 0: External GFX 1: For internal GFX's allocation way
2	RW	0	**Channel-A GFX to DRAM Read Snoop CMFIFO** 0: Not snoop 1: Snoop
1	RW	0	**Asynchronous Test Mode for GMINTB** 0: Normal mode 1: Async test mode
0	RW	0	**Asynchronous Test Mode for GMINTA** 0: Normal mode 1: Async test mode

Offset Address: A8-AFh (D0F3) – Reserved

GMINT and AGPCINT Registers (B0–BFh)

Offset Address: B1-B0h (D0F3)

GMINT Misc. 1 **Default Value: 00h**

Bit	Attribute	Default	Description
15:12	RW	0	**GMINT Arbiter Timer for HighChannel-to-LowChannel Switching** (unit of 16 DCLK)
11:8	RW	0	**GMINT Arbiter Timer for LowChannel-to-HighChannel Switching** (unit of 16 DCLK)
7	RW	0	**Bypass the MCLK Sync Logic for GFX-to-GMINT Signals** 0: Sync the signals (1T) 1: Bypass the sync logic
6:4	RO	0	**Reserved**
3	RW	0	**Improve GMINT Arbitration Performance** 0: Disable 1: Enable arbitration policy of priority agent bus request/symmetric bus agent request
2:0	RO	0	**Reserved**

Offset Address: B2h (D0F3)

AGPCINT Misc. **Default Value: A0h**

Bit	Attribute	Default	Description
7	RW	1b	**Enable AGPCINT-to-GFX Interface Power Management** 0: Disable 1: Enable
6	RW	0	**GADS from AGPC will be strict priority** 0: Disable 1: Enable (Cooperate with RxB2[5])
5	RW	1b	**Enable High Priority GFX Request** 0: Disable 1: Enable (When the high priority signal of GADS wants to come from GADSH, RAGPPRIEN should be de-assert.)
4	RO	0	**Reserved**
3	RW	0	**Allow AGPCINT to Issue 8QW Request** (Coordinate with D0F2 Rx54[4])
2	RW	0	**GFX AGP Read Data Sync 1T** 0: Disable 1: Enable
1	RW	0	**Disable AGPCINT Pipe Mode** 0: Enable 1: Disable
0	RO	0	**Reserved**

Offset Address: B3h (D0F3)
GMINT Misc. 2 **Default Value: 9Eh**

Bit	Attribute	Default	Description
7:5	RW	100b	**Flush Counter Used when RxB3[2] =1 & Write Queue Full** For ex: if number =4, it will pop 4~5 write requests.
4:3	RW	11b	**Flush Counter Used when RxB3[1] =1 & Write Queue Full** For ex: if number = 3, it will pop 3~4 write requests.
2	RW	1b	**GMINT A Read Pass Write** 0: Read write in order (only read queue active) 1: Read pass write
1	RW	1b	**GMINT B Read Pass Write** 0: Read write in order (only read queue active) 1: Read pass write
0	RO	0	**Reserved**

Offset Address: B4h (D0F3)
EPLL Register **Default Value: 03h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	011b	**EPLL Feed-Back Clock Tree Delay Control** Each bit for 60ps 000: No delay 001: Delay 60ps 010: Delay 120ps 011: Delay 180ps …. i: Delay i*60 ps

Offset Address: B5-BFh (D0F3) – Reserved

DDR2 – I/O Pad Termination and Driving Control (D0–DFh)

Offset Address: D0h (D0F3)

DQ / DQS Termination Strength Manual Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQ/DQS Pull-up Termination Strength Manual Setting**
3:0	RW	0	**DQ/DQS Pull-down Termination Strength Manual Setting**

Offset Address: D1h (D0F3)

DQ / DQS Termination Strength Auto-Comp Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**DQ/DQS Pull-up Termination Strength Auto-comp Value**
3:0	RO	0	**DQ/DQS Pull-down Termination Strength Auto-comp Value**

Offset Address: D2h (D0F3)

DQ Driving Strength Auto-Comp Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**DQ Pull-up Driving Strength Auto-comp Value**
3:0	RO	0	**DQ Pull-down Driving Strength Auto-comp Value**

Offset Address: D3h (D0F3)

Compensation Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Disable DDR Compensation Auto Mode** 0: Enable Auto Mode 1: Disable Auto Mode If DDR Compensation and DDR Auto Compensation are both enabled, the ODT settings for all DRAM pads are from auto-comp circuit (RxD1); otherwise, if Auto Compensation is disabled, the ODT settings are from manual setting (RxD0).
0	RW	0	**Enable DDR Compensation** 0: Disable 1: Enable Disable DDR Compensation provides a power saving mode; however, the values of RxD1 and RxD2 should be ignored.

Note: The DQ driving bits of RxD2 is the result of the auto-comp circuit; however, there is no "auto-mode" for the DQ/DQB driving control since it depends on the actual number of ranks in the DRAM data channel

Offset Address: D4h (D0F3)

ODT Pullup / Pulldown Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable NM Pad ODT** 0: Disable ODT unless RxD4[3:0] is not equal to 0 1: Enable ODT when reading data
6	RW	0	**Enable DDR Pad Static Termination** 0: Disable 1: Enable
5	RW	0	**Enable MCLKI ODT** 0: Disable 1: Enable
4	RW	0	**PRE PAD ODT for 1st Write Data** 0: Disable 1: Enable
3	RW	0	**ODT Pullup Enable – Channel A** 0: Disable 1: Enable
2	RW	0	**ODT Pullup Enable – Channel C** 0: Disable 1: Enable
1	RW	0	**ODT Pulldown Enable – Channel A** 0: Disable 1: Enable
0	RW	0	**ODT Pulldown Enable – Channel C** 0: Disable 1: Enable

MD PADs ODT Control

The MD PADs ODT control will affect the current leakage. Please set D0F3 Rx9B and RxD4 control registers for different DRAM channel (A or C) modes with saving power.

Table 10. MD PADs ODT Control in different DRAM Mode

DRAM Mode		Group Set *(Please refer to the following Group table)*
Channel A	**Channel C**	
Channel A 64-bit	N/A	{1 & 2}
Channel A 32-bit	N/A	{2}
Channel A 64-bit	Channel C 16-bit	{1 & 3 & 4}
Channel A 32-bit	Channel C 16-bit	{2 & 4}

Table 11. PAD ODT Control Group Setting

Group	MD Byte	Register	MD ODT Control State		
			Turn-off	Static-on	Dynamic-on
1	Channel A upper byte7~4	Rx9B[4]	0	x	1
		Rx9B[1]	0	1	0
2	Channel A lower byte3~0	RxD4[7]	0	x	1
		RxD4[3] RxD4[1]	0	1	0

Offset Address: D5h (D0F3)

DQ / DQS Burst Function and ODT Range Select **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable DQ Burst Function – Channel A** 0: Disable 1: Enable
6	RW	0	**Enable DQ Burst Function – Channel C** 0: Disable 1: Enable
5	RW	0	**DQS Burst Function – Channel A** 0: Disable 1: Enable
4	RW	0	**DQS Burst Function – Channel C** 0: Disable 1: Enable
3	RW	0	**DQ ODT Range Select – Channel A** 0: 150 ohm 1: 75 ohm
2	RW	0	**DQ ODT Range Select – Channel C** 0: 150 ohm 1: 75 ohm
1	RW	0	**DQS ODT Range Select – Channel A** 0: 150 ohm 1: 75 ohm
0	RW	0	**DQS ODT Range Select – Channel C** 0: 150 ohm 1: 75 ohm

Offset Address: D6h (D0F3)

DCLK / SCMD / CS Driving Select **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DCLKOA Driving Select** 0: Weak driving for DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
6	RW	0	**DCLKOB Driving Select – Channel C** 0: Weak driving for DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
5	RW	0	**SCMD/MAA Driving Select** 0: Weak driving for DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
4	RW	0	**SCMD/MAB Driving Select – Channel C** 0: Weak driving for DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
3	RW	0	**CKE/CSA Driving Select** 0: Weak driving for DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
2	RW	0	**CKE/CSB Driving Select – Channel C** 0: Weak driving for DDR2 without series resistance on MB 1: Strong driving for DDR2 with series resistance on MB
1:0	RO	0	**Reserved**

Offset Address: D7h (D0F3)
SCMD/MA Burst Function **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SCMD/MAA Burst Function Enable** 0: Disable 1: Enable
6:0	RO	0	**Reserved**

Offset Address: D8h (D0F3)
DCLKI Termination Strength **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DCLKI Pull-up Termination Strength**
3:0	RW	0	**DCLKI Pull-down Termination Strength**

Offset Address: D9-DAh (D0F3) – Reserved

Offset Address: DBh (D0F3)
Operation Mode Control – Channel C **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Channel C** 0: Disable 1: Enable
6	RW	0	**Initialization Clock** Choose NM PLL's 166/133MHz clock as DRAMCC's clock source in order to precede initialization or function test. See the bit 5 for operating mode select.
5	RW	0	**Initialization Select** The clocks of DRAMCC and MCLKO0B P/N are always supplied when this bit has been programmed to 1. After initialization is done, this bit must be programmed to 0. There are 4 different operation modes:

Bit 6	Bit 5	Description
0	0	Normal snapshot operation mode
0	1	Initialization with GFX's display clock
1	0	DRAMCC snapshot function test mode (RxDD[3]=1)
1	1	Initialization with NB's PLL clock (RxDD[3] =0)

<table>
<tr>
<td>4:2</td>
<td>RW</td>
<td>0</td>
<td>Command Type
Command types will be triggered by bit RxDB[1]
<table>
<tr><th>RAS</th><th>CAS</th><th>WE</th><th>Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>NOP</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Ready/completion for Read/Write.
This command must be triggered once before/after Read/Write command is issued. This command is only used by NM for preparing/terminating. Read/Write state machine of initialization and won't be really issued on DRAM bus.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Read command.
BA[1:0]=RxF9-F8[14:13], MA[12:0]=RxF9-F8[12:0], the returned data can be read from D0F7 RxDF-D0 after this command. Bank-Activate command must be triggered before this command can be triggered.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Write command.
BA[1:0]=RxF9-F8[14:13], MA[12:0]=RxF9-F8[12:0], write data will be D0F7 RxCF-C0. Bank-Activate command must be triggered before this command can be triggered.</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Bank-Activate command.
BA[1:0]=RxF9-F8[14:13], MA[12:0]=RxF9-F8[12:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Single-Bank-Precharge (RxF9-F8[10] =0)/Precharge-All-Banks (RxF9-F8[10]=1), BA[1:0]=RxF9-F8[14:13], MA[12:0]=RxF9-F8[12:0].</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Auto-Refresh</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>MRS(RxF9-F8h[14:13]=00b)/EMRS(1)(RxF9-F8[14:13]=01b)/EMRS(2)(RxF9-F8[14:13]=10b)/EMRS(3)(RxF9-F8[14:13]=11b), the written content should be pre-programmed in RxF9-F8[12:0] which will be placed on MA[12:0] when the command is asserted.</td></tr>
</table>
To save more DRAM power consumption, please set RxF9-F8[1] to enable quarter array self-refresh during EMRS(2) and reduce output driving strength during EMRS. Actually, snapshot mode will work fine even without any DRAM refresh. And in this situation, it may work fine when the frequency is low.
To save more DRAM power consumption, please set RxF9-F8[0]=1 to disable DLL during EMRS. It may work fine when the frequency is low.
RxF9-F8[3:0] must be set to 1011b during MRS in order to set interleave mode and burst length 8 which is the only one working condition of DRAMCC.</td>
</tr>
<tr>
<td>1</td>
<td>RW</td>
<td>0</td>
<td>Command Trigger
Issue a command which is defined by RxDB[3:2] to DRAM bus. Once this bit is writing 0 then 1 will trigger one command to DRAM bus.</td>
</tr>
<tr>
<td>0</td>
<td>RW</td>
<td>0</td>
<td>Precharge Power Down
Snapshot DRAM will enter Precharge power down instead of Self-Refresh.
It will take less recovery time from pending to access DRAM. This bit only can be turned on/off during initialization.</td>
</tr>
</table>

Offset Address: DCh (D0F3)

Timing Parameters Control – Channel C **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Read CAS Latency** Normally, RxDC[7:6] = RxDF[7:6]. But if DRAM's DLL has been disabled, it might be set as (RxDF[7:6]-1) or (RxDF[7:6]+1) according to the actual read data timing. 00: 2T 01: 3T 10: 4T 11: 5T Notes: 1. tRCD is always 4T. 2. tRP is always 4T.
5	RW	0	**Pull Up Chip's ODT When Read** 0: Disable 1: Enable
4	RW	0	**Pull Down Chip's ODT When Read** 0: Disable 1: Enable
3	RW	0	**Pull Up Chip's ODT When Write** 0: Disable 1: Enable
2	RW	0	**Pull Down Chip's ODT When Write** 0: Disable 1: Enable
1	RW	0	**Enable DRAM's ODT When Read** 0: Disable 1: Enable
0	RW	0	**Enable DRAM's ODT When Write** 0: Disable 1: Enable Notes: 1. It is always 1T command. 2. It only supports X16 DRAM chip X 1. 3. It only supports 2 bank address pins, BA1~BA0. 4. It only supports burst length 8.

Offset Address: DDh (D0F3)

PADs Power-Down Control – Channel C **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**ODT (On Die Termination) PAD Power Down** 0: Disable 1: Enable
6	RW	0	**Column Address Type** 0: MA8~MA0 1: MA9~MA0
5:4	RW	00b	**Power Down Unused MAB PADs**. 00: MAB12, MAB11 are available 01: DRAMCC debug mode. MAB12, MAB11, and CASB[3:0] are not available. 10: MAB12 is not available, but MAB11 is available. 11: MAB12, MAB11 are not available The corresponding MAB[12:11] pins of DRAM chips must be tied to 0 to prevent high impedance.
3	RW	0	**Power Down Data Mask [1:0] PADs** DQM pins must be tied to 0 on boards.
2:0	RW	000b	**Adjust The Timing Window of Capturing 2X Read Data** 000: Rising Clock Edge without extra delay 001: Rising Clock Edge with 0.5~1ns Delay 010: Rising Clock Edge with 1~2ns Delay 011: Rising Clock Edge with 1.5~3ns Delay 100: Falling Clock Edge with 2~4ns Delay 101: Falling Clock Edge with 2.5~5ns Delay 110: Falling Clock Edge with 3~6ns Delay 111: Falling Clock Edge with 3.5~7ns Delay

Offset Address: DEh (D0F3)

GMINT's Merge Function **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Disable GMINTA Merge Mode** 0: Merge 2QW request 1: Disable 2QW merge
0	RO	0	**Reserved**

Offset Address: DFh (D0F3)

Write Cycle Timing Control – Channel C **Default Value: 04h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Write CAS Latency** **It should be set as (tCL(MRS[6:4]) - 1)T** 00: 1T 01: 2T 10: 3T 11: 4T Note: MRS: Mode Register Set, a programming sequence to DRAM DIMM at the beginning of the system boot up. The bits programmed in this register should be corresponding to the MRS[6:4] which defines the CAS latency as: MRS[6:4] CL[2:0] CAS Latency Bit[7:6] 111 111 Reserved - 110 110 Reserved - 101 101 5T 11 (4T) 100 100 4T 10 (3T) 011 011 3T 01 (2T) 010 010 2T 00 (1T) 001 001 Reserved - 000 000 Reserved -
5	RW	0	**Tri-state Output Signal Enable for Self-refresh and Precharge Power-down** Tri-state all output signals except CKE during self-refresh, or tri-state all output signals except CKE, ODT and MCLKO during Precharge Power-down. It must be set to 0 in DRAMCC debug mode. 0: Disable 1: Enable
4:3	RW	00b	**Adjust Write DQ Delay** 00: Delay 1 ~ 2 ns from DQS 01: Delay 1.1 ~ 2.2 ns from DQS 10: Delay 1.2 ~ 2.4 ns from DQS 11: Delay 1.3 ~ 2.6 ns from DQS
2	RW	1b	**Tri-state Output Signal Enable for Active Power-down** Tri-state all output signals except CKE, ODT and MCLKO during Active Power-down. 0: Disable 1: Enable
1:0	RW	00b	**Adjust MCLKO (DRAM clock) Delay** 00: -0.2 ~ 0.4 ns 01: -0.1 ~ 0.2 ns 10: 0 ns 11: 0.1 ~ 0.2 ns

DRAM Driving Control (E0–EBh)

Table 12. Physical Pin to Driving Group Mapping Table

Physical Pins	MCLK[A, B]	CKE[A, B]	CS[A, B]	MA[A, B]	DQ[A, B]	DQS[A, B]	DQM[A, B]
Driving Group	MCLK[A, B]	CS[A, B]	CS[A, B]	MA[A, B]	DQ[A, B]	DQS[A, B]	DQ[A, B]

Offset Address: E0h (D0F3)
DRAM Driving – Group DQSA **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQSA - PMOS Driving**
3:0	RW	0	**DQSA - NMOS Driving**

Offset Address: E1h (D0F3)
DRAM Driving – Group DQSB **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQSB - PMOS Driving**
3:0	RW	0	**DQSB - NMOS Driving**

Offset Address: E2h (D0F3)
DRAM Driving – Group DQA (MD, DQS, DQM) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQA - PMOS Driving**
3:0	RW	0	**DQA - NMOS Driving**

Offset Address: E3h (D0F3)
DRAM Driving – Group DQB (MD, DQS, DQM) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**DQB – PMOS Driving**
3:0	RW	0	**DQB – NMOS Driving**

Offset Address: E4h (D0F3)
DRAM Driving – Group CSA (CS, DQM) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**CSA – PMOS Driving**
3:0	RW	0	**CSA – NMOS Driving**

Offset Address: E5h (D0F3)
DRAM Driving – Group CSB (CS, DQM) **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**CSB – PMOS Driving**
3:0	RW	0	**CSB – NMOS Driving**

Offset Address: E6h (D0F3)
DRAM Driving – Group MCLKA **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**MCLKA – PMOS Driving**
3:0	RW	0	**MCLKA – NMOS Driving**

Offset Address: E7h (D0F3)
DRAM Driving – Group MCLKB **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**MCLKB – PMOS Driving**
3:0	RW	0	**MCLKB – NMOS Driving**

Offset Address: E8h (D0F3)
DRAM Driving – Group SCMDA/MAA **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**MAA – PMOS Driving**
3:0	RW	0	**MAA – NMOS Driving**

Offset Address: E9h (D0F3)
DRAM Driving – Group SCMDB/MAB **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**MAB – PMOS Driving**
3:0	RW	0	**MAB – NMOS Driving**

Offset Address: EA-EBh (D0F3) – Reserved

DRAM CKG Control (EC–EFh)

Offset Address: ECh (D0F3)

Channel-A DQS / DQ CKG Output Duty Cycle Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DQS CKG Falling Edge Control** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
5:4	RW	00b	**DQS CKG Rising Edge Control** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps
3:2	RW	00b	**DQ CKG Falling Edge Control** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
1:0	RW	00b	**DQ CKG Rising Edge Control** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps

Offset Address: EDh (D0F3)

DQS / DQ CKG Output Duty Cycle Control – Channel C **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DQS CKG Falling Edge Control** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
5:4	RW	00b	**DQS CKG Rising Edge Control** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps
3:2	RW	00b	**DQ CKG Falling Edge Control** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
1:0	RW	00b	**DQ CKG Rising Edge Control** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps

Offset Address: EEh (D0F3)

DCLK Output Duty Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Duty Control for DCLKA** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
5:4	RW	00b	**Duty Control for DCLKA** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps
3:2	RW	00b	**Duty Control for DCLKB - Channel C** 00: Default 01: Falling edge delays 100 ps 10: Falling edge delays 200 ps 11: Falling edge delays 300 ps
1:0	RW	00b	**Duty Control for DCLKB - Channel C** 00: Default 01: Rising edge delays 100 ps 10: Rising edge delays 200 ps 11: Rising edge delays 300 ps

Offset Address: EFh (D0F3)

DQ CKG Input Delay Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	00b	**DQS Input Delay Control for MDA** 00: -150 ps 01: 0 ps 10: 150 ps 11: 300 ps
3:2	RO	0	**Reserved**
1:0	RW	00b	**DQS Input Delay Control for MDB - Channel C** 00: -150 ps 01: 0 ps 10: 150 ps 11: 300 ps

DQ / DQS CKG Output Delay Control (F0–F9h)

Offset Address: F0-F3h (D0F3)

DQ/DQS CKG Output Delay Control - Channel A **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:28	RW	000b	**DQ/DQS Delay Control for Group A7** 000: Default 001: Delay 60ps 010: Delay 120ps 011: Delay 180ps 100: Delay 240ps 101: Delay 300ps 110: Delay 360ps 111: Delay 420ps
27	RO	0	**Reserved**
26:24	RW	0	**DQ/DQS Delay Control for Group A6**
23	RO	0	**Reserved**
22:20	RW	0	**DQ/DQS Delay Control for Group A5**
19	RO	0	**Reserved**
18:16	RW	0	**DQ/DQS Delay Control for Group A4**
15	RO	0	**Reserved**
14:12	RW	0	**DQ/DQS Delay Control for Group A3**
11	RO	0	**Reserved**
10:8	RW	0	**DQ/DQS Delay Control for Group A2**
7	RO	0	**Reserved**
6:4	RW	0	**DQ/DQS Delay Control for Group A1**
3	RO	0	**Reserved**
2:0	RW	0	**DQ/DQS Delay Control for Group A0**

Offset Address: F7-F4h (D0F3)

DQ/DQS CKG Output Delay Control - Channel C **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RO	0	**Reserved**
30:28	RW	000b	**DQ/DQS Delay Control for Group B7** 000: Default 001: Delay 60ps 010: Delay 120ps 011: Delay 180ps 100: Delay 240ps 101: Delay 300ps 110: Delay 360ps 111: Delay 420ps
27	RO	0	**Reserved**
26:24	RW	0	**DQ/DQS Delay Control for Group B6**
23	RO	0	**Reserved**
22:20	RW	0	**DQ/DQS Delay Control for Group B5**
19	RO	0	**Reserved**
18:16	RW	0	**DQ/DQS Delay Control for Group B4**
15	RO	0	**Reserved**
14:12	RW	0	**DQ/DQS Delay Control for Group B3**
11	RO	0	**Reserved**
10:8	RW	0	**DQ/DQS Delay Control for Group B2**
7	RO	0	**Reserved**
6:4	RW	0	**DQ/DQS Delay Control for Group B1**
3	RO	0	**Reserved**
2:0	RW	0	**DQ/DQS Delay Control for Group B0**

Offset Address: F9-F8h (D0F3)

DRAM Mode Register Setting (MRS) Control – DRAM Channel C (DRAMCC) **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14:0	RW	0	**DRAMCC MRS Register** The content will be placed on MA and BA when MRS/EMRS(1,2,3)/Bank-Activate/Write/Read commands are triggered. RDC_MRS[14:13] - BA[1:0] RDC_MRS[12:0] - MA[12:0]

DDR2 – DQ De-Skew Control (FA–FFh)

Offset Address: FAh (D0F3)

DQ De-Skew Function Control **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**Enable DQ Input De-Skew Circuit** 0: Disable 1: Enable
6	RW	1b	**Manual DQ Output Delay Setting** 0: Auto 1: Manual
5	RW	0	**Manual DQ Input Delay Setting** 0: Auto 1: Manual
4	RW	0	**Manual Setting for RX / TX Select** 0: RX 1: TX
3	RO	0	**Reserved**
2:0	RW	000b	**Manual Setting DQ Group Select** 000: DQ[7:0] 001: DQ[15:8] … 110: DQ[55:48] 111: DQ[63:56]

Offset Address: FBh (D0F3)

Power Management - Channel A **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable By-Rank Self-Refresh Clock. Being dynamic** 0: Disable 1:Enable
6	RW	0	**Enable Auto Fresh Self-Refresh Clock** 0: Disable 1:Enable
5	RW	0	**Enable SCMD Top Logic Clock** 0: Disable 1:Enable
4	RW	0	**Enable CAS Top Logic Clock** 0: Disable 1:Enable
3	RW	0	**Enable MDA Top Logic Clock** 0: Disable 1:Enable
2	RW	0	**Enable DQS Top Logic Clock** 0: Disable 1:Enable
1	RW	0	**Enable DRAM Page Control Module Dynamic Clock** 0: Disable 1:Enable
0	RW	0	**Enable MCLKO Being Dynamic Clock** 0: Disable 1:Enable

Offset Address: FCh (D0F3) – Reserved

Offset Address: FDh (D0F3)

Power Management 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Stop Page Timer's Clock when DRAMCA's Ranks All Enter Self Refresh** 0: Free running 1: Enable dynamic
6	RO	0	**Reserved**
5	RW	0	**Stop MCLKOA When All Ranks Enter Self Refresh** 0: Free running 1: Enable dynamic
4	RO	0	**Reserved**
3	RW	0	**Power Management of Reference Clock Enable - Channel A** 0: Free running 1: Enable dynamic
2:1	RO	0	**Reserved**
0	RW	0	**Power Management of Dynamic DQA Clock's Source – Channel A** 0: Free running 1: Enable dynamic

Offset Address: FEh (D0F3)

Power Management 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Power Management Unit (PMU) in S1 State** 0: S1 will not turn off PLL. 1: S1 will turn off PLL.
6	RW	0	**Precise Power Management of Internal DBX C2M FIFO's Clock** 0: Precise power management 1: Normal power management
5	RW	0	**Enable Auto Refresh Clock of Refresh Control Module Stop While DRAM Enters Sleep Mode** 0: Disable 1: Enable
4	RO	0	**Reserved**
3:0	RW	0	**Enable the PIN - Chip Select A as Power Saving Mode When This Rank Enters Self Refresh** Bit3 – Chip Select A3 Bit2 – Chip Select A2 Bit1 – Chip Select A1 Bit0 – Chip Select A0 0: Disable 1: Enable

DRAM Power Saving Mode

Please refer to these following Power Saving Mode tables for the details of DRAM power management.

Table 13. SCMD and MA Pins Power Saving Mode Setting

Power Saving Mode Setting	D0F4 RxA1[5]	D0F3 RxFF[0]
S1: Extra power saving mode (recommended)	1	0
S2: More power saving mode	0	1
S3: Less power saving mode	1	1
S4: No power saving mode	0	0

Note: The power saving of all modes is S1>S2>S3>S4.

The following table is an example of Rank 0, and this setting rule can be applied to other Ranks respectively.

Table 14. Chip Select Pins Power Saving Mode Usage

Power Saving Mode Usage	D0F3 Rx54[7]	D0F3 RxFE[0]
Power saving mode	1	1
No power saving mode (recommended)	1	0
No Rank 0	0	1
No Rank 0	0	0

Offset Address: FFh (D0F3)

DQS Input Delay of Channel C and Registers for STR Mode **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**DQSB Input Delay – Channel C** The adjustment of DQSB in the read path and each step can delay 30~50p.
1	RO	0	**Reserved**
0	RW	0	**Enable SCMD** MA Bus floats during suspend state. 0:Disable 1:Enable

Device 0 Function 4 (D0F4): Power Management Control

Header Registers (00-3Fh)

Offset Address: 01-00h (D0F4)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F4)

Device ID **Default Value: 4353h**

Bit	Attribute	Default	Description
15:0	RO	4353h	**Device ID Code**

Offset Address: 05-04h (D0F4)

PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0 (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F4)
PCI Status **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error** (SERR# asserted)
13	RW1C	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RW1C	0	**Master Data Parity Error** This bit is set when bus master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F4)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Chip Revision Code**

Offset Address: 0B-09h (D0F4)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F4) – Reserved

Offset Address: 0Dh (D0F4)
PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**PCI Bus Time Slice for CPU as a Master** (in Unit of PCI clocks)
2:0	RO	0	**Reserved.** Bit [2:1] is programmable; however, it is read as 0.

Offset Address: 0Eh (D0F4)
Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type**

Offset Address: 0Fh (D0F4)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST Support** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 10-2Bh (D0F4) – Reserved

Offset Address: 2D-2Ch (D0F4)
Subsystem Vendor ID **Default Value: 00h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F4)
Subsystem ID **Default Value: 00h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F4) – Reserved

Offset Address: 34h (D0F4)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** An offset address from the start of the configuration space

Offset Address: 35-7Fh (D0F4) – Reserved

Power Management Control (80–EFh)

Offset Address: 80-83h (D0F4) – Reserved

Offset Address: 84h (D0F4)
Central Traffic Controller Power Management Registers 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Level-1 Host Clock (HCLK) Enable** 0: Free-running clock 1: Dynamic clock
6	RW	0	**Level-1 Global PCI Clock (GCLK, running at 66MHz)Enable** 0: Free-running clock 1: Dynamic clock
5	RW	0	**Level-1 PCIe Clock (ECLK, running at 250MHz) Enable** 0: Free-running clock 1: Dynamic clock
4	RW	0	**Down-Stream HCLK Enable** 0: Free-running clock 1: Dynamic clock
3	RW	0	**Down-Stream GCLK Enable** 0: Free-running clock 1: Dynamic clock
2	RW	0	**Down-Stream ECLK Enable** 0: Free-running clock 1: Dynamic clock
1	RW	0	**Up-Stream HCLK Enable** 0: Free-running clock 1: Dynamic clock
0	RW	0	**Up-Stream GCLK Enable** 0: Free-running clock 1: Dynamic clock

Offset Address: 85h (D0F4)

Central Traffic Controller Power Management Registers 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic ECLK Control for Up-stream** 0: Free-running clock 1: Dynamic clock
6	RW	0	**Dynamic HCLK Control for PE0 Up-Stream Pop and Push** 0: Free-running clock 1: Dynamic clock
5	RW	0	**Dynamic HCLK Control for PE1 Up-Stream Pop and Push** 0: Free-running clock 1: Dynamic clock
4	RW	0	**Dynamic HCLK Control for PEG0 Up-Stream Pop and Push Enable** 0: Free-running clock 1: Dynamic clock
3	RO	0	**Reserved**
2	RW	0	**Dynamic Configuration Controller Clock Control for the Register Access** 0: Free-running clock 1: Dynamic clock
1	RW	0	**Dynamic APIC Clock Control** 0: Free-running clock 1: Dynamic clock
0	RW	0	**Dynamic Configuration Controller Clock Control for the Register Error Report** 0: Free-running clock 1: Dynamic clock

Offset Address: 86-87h (D0F4) – Reserved

Offset Address: 88h (D0F4)

APIC Power Management **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Dynamic PCIe Clock (running at 250MHz) of APIC** 0: Free-running clock 1: Dynamic clock
0	RW	0	**Dynamic Global PCI Clock (running at 66MHz) of APIC** 0: Free-running clock 1: Dynamic clock

Offset Address: 89h (D0F4)

Graphics-Memory Interface (GMINT) Power Management 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic DRAM Clock Control for GMINTA Request Queue** 0: Free-running clock 1: Dynamic clock
6	RW	0	**Dynamic Push Clock Control for GMINTA Data FIFO** 0: Free-running clock 1: Dynamic clock
5	RW	0	**Dynamic Pop Clock Control for GMINTA Data FIFO** 0: Free-running clock 1: Dynamic clock
4	RW	0	**Dynamic GFX Data Read Ready Clock for GMINTA** 0: Free-running clock 1: Dynamic clock
3	RW	0	**Dynamic Snooping C2M Write Data FIFO Clock for GMINTA Request Queue** 0: Free-running clock 1: Dynamic clock
2	RW	0	**Dynamic DRAM Clock Control for GMINTB Request Queue** 0: Free-running clock 1: Dynamic clock
1	RW	0	**Dynamic Push Clock Control for GMINTB Data FIFO** 0: Free-running clock 1: Dynamic clock
0	RW	0	**Dynamic Pop Clock Control for GMINTB Data FIFO** 0: Free-running clock 1: Dynamic clock

Offset Address: 8Ah (D0F4)

GMINT Power Management 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Dynamic GFX Data Read Ready Clock for GMINTB** 0: Free-running clock 1: Dynamic clock

Offset Address: 8Bh (D0F4)

Data Path Module (DBX) Power Management Registers **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Power Management of C2M Read Cycle Data Bus of Channel-A (M2AI)** 0: The pipeline of M2AI has free-running clocks 1: The pipeline of M2AI has dynamic clocks
6	RW	0	**Power Management of C2M Read Cycle Data Bus of Channel-B (M2BI)** 0: The pipeline of M2BI has free-running clocks 1: The pipeline of M2BI has dynamic clocks
5	RW	0	**Power Management of C2M Write Data FIFO (CMFIFO)** 0: CMFIFO has free-running clocks 1: CMFIFO has dynamic clocks
4	RW	0	**Power Management of C2M Read Data FIFO (MCFIFO)** 0: MCFIFO has free-running clocks 1: MCFIFO has dynamic clocks
3	RW	0	**Power Management of C2P Write Data FIFO (CPWFIFO)** 0: CPWFIFO has free-running clocks 1: CPWFIFO has dynamic clock
2	RW	0	**Power Management of C2P Read Data FIFO (CPRFIFO)** 0: CPRFIFO has free-running clocks 1: CPRFIFO has dynamic clocks
1	RW	0	**Power Management of P2C Write Data FIFO (PMWFF)** 0: PMWFF has free-running clocks 1: PMWFF has dynamic clocks
0	RW	0	**Power Management of P2C Read Data FIFO (PMRFF)** 0: PMRFF has free-running clocks 1: PMRFF has dynamic clocks

Offset Address: 8Ch (D0F4) – Reserved

Offset Address: 8Dh (D0F4)

PMU Related Registers 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Snapshot Mode in C3 State** 0: Disable 1: Enable BIOS needs to set this register to 1'b0 if supports DRAM Channel A only.
6	RW	0	**Snapshot Mode in C4 State** 0: Disable 1: Enable BIOS needs to set this register to 1'b0 if supports DRAM Channel A only.
5	RW	0	**Self Refresh Mode in C3 State** 0: Disable 1: Enable
4	RW	0	**Self Refresh Mode in C4 State** 0: Disable 1: Enable
3	RW	0	**PLL1 Control** 0: Reset PLL1 1: Turn off PLL1
2	RW	0	**PLL2 Control** 0: Reset PLL2 1: Turn off PLL2
1	RW	0	**EPLL Control** 0: Reset EPLL 1: Turn off EPLL
0	RW	0	**PCIe Turn Off EPLL for Low Power Feature At Electric Idle Assert** 0: Disable 1: Enable

Offset Address: 8Eh (D0F4)

PMU Related Registers 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**EPLL Gating Enable Option** 0: Disable 1: Enable
6	RW	0	**PLL_OK Source Selection from PLL or SM** 0: Select PLL_OK from PLLs 1: Select PLL_OK from SM
5	RW	0	**Suspend State PLL Always on Option** 0: Suspend State will Reset/Turn_off PLLs 1: Suspend State never Reset/Turn_off PLLs
4	RW	0	**Enable PLL's RESETI to Go High 20us After PLL's PU Is On** 0: Disable 1: Enable
3	RW	0	**Force Exit Snapshot Mode in C0 State** 0: C0 state will exit snapshot mode 1: C0 state will force to exit snapshot mode
2:1	RO	0	**Reserved**
0	RW	0	**Allow Software to Enter Snapshot Mode** 0: Not Allowed 1: Allowed

Offset Address: 8Fh (D0F4) – Reserved

Offset Address: 90h (D0F4)

P6IF Power Management Registers 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CPURST# Flip-flops Gate Clock Control** Enable to gate clocks for flip-flops, only active during assertion of CPURST#. 0: Disable 1: Enable
6	RW	0	**GTL Flip-flops Gate Clock Control** Enable to gate clocks for flip-flops, only active during the duration of computing auto-compensation values for GTL pads and power-down GTLCOMP after this process has completed. 0: Disable 1: Enable
5	RW	0	**CPU ADS/ PCI Master Snoop Cycles Flip-flops Gate Clock Control** Enable to gate clocks for flip-flops, only active when CPU issues ADS or PCI master issues snooping cycles. 0: Disable 1: Enable
4	RW	0	**ROMSIP Flip-flops Gate Clock Control** 0: Disable 1: Enable
3	RW	0	**Host Data Transmit DIO & GTL Pads Gate Clock Control** Enable to gate clocks for DIOs & GTL pads, only active for transmitting HD#. 0: Disable 1: Enable
2	RW	0	**Host Address / Request Transmit DIO & GTL Pads Gate Clock Control** Enable to gate clocks for DIOs & GTL pads, only active for transmitting HA# / HREQ#. 0: Disable 1: Enable
1	RW	0	**Host Address / Request Receive DIO Gate Clock Control** Enable to gate clocks for DIOs, only active for receiving HA# / HREQ#. 0: Disable 1: Enable
0	RW	0	**1x Host Signal Transmit DIO & GTL Gate Clock Control** Enable to gate clocks for DIOs & GTL pads, only active for transmitting 1X host signals. 0: Disable 1: Enable

Offset Address: 91h (D0F4)

P6IF Power Management Registers 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Set as 1'b1 for the Case When BREQ0# Always Parks on the Host Bus. (e.g. VIA-Centaur CPU, CN Series) to Invoke Another Power – Saving Technique** 0: Disable 1: Enable
6	RW	0	**CPU-to-PCI Flip-flops Gate Clock Control** Enable to gate clocks for flip-flips, only active for C2P cycles. 0: Disable 1: Enable
5	RW	0	**Defer Queue Request Flip-flops Gate Clock Control** Enable to gate clocks for flip-flops, only active when writing requests to Defer Queue. 0: Disable 1: Enable
4	RW	0	**CPU-to-Memory Flip-flops Gate Clock Control** Enable to gate clocks for flip-flops, only active for C2M cycles. 0: Disable 1: Enable
3	RW	0	**Address Strobe Assertion Gate Clock Control** Enable to gate clock for IOQ entries, only active when ADS1 asserts. 0: Disable 1: Enable
2	RW	0	**Enable to Gate Clock for C2P Request Queue Entries, Only Active When Push Signal of PAQ Asserts** 0: Disable 1: Enable
1	RW	0	**Enable to Gate Clock for Post-Write Queue Entries, Only Active When Push Signal of C2M Write Queue Asserts** 0: Disable 1: Enable
0	RW	0	**Triggering Warm Reset Flip-flops Gate Clock Control** Enable to gate clock for flip-flops, only active for triggering warm reset. 0: Disable 1: Enable

Offset Address: 92h (D0F4)

P6IF Power Management Registers 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Host Data Dynamic Input Differential Buffer Control** 0: Disable this function 1: Dynamically enable/disable input differential buffer for HD pad.
6	RW	0	**Host Address / Request Dynamic Input Differential Buffer Control** When turned on, it will observe BREQ0 to dynamically enable/disable input differential buffer for HA, HREQ pad. If BREQ0 always parks on FSB (e.g. VIA-Centaur CPU, CN series), please also set Rx91[7] = 1'b1 to invoke another power-saving technique. The suggested value is 1'b1.
5:4	RO	0	**Reserved**
3	RO	0	**Power Down Input Comparators of AGTL+ Pads of HA#/HREQ#/HLOCK#/HBNR#/HBREQ0# at PMU C2 State** 0: Disable 1: Enable
2	RO	0	**Power Down Input Comparators of All AGTL+ Pads at PMU C3/C4/S1 State** 0: Disable 1: Enable
1:0	RO	0	**Reserved**

Offset Address: 93h (D0F4) – Reserved

Offset Address: 94h (D0F4)

MSGC Power Management Registers **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**MSGC PEG0 Power Management** 0: Disable 1: Enable
1	RW	0	**MSGC PE0 Power Management** 0: Disable 1: Enable
0	RW	0	**MSGC PE1 Power Management** 0: Disable 1: Enable

Offset Address: 95-9Fh (D0F4) – Reserved

Offset Address: A0h (D0F4)
Power Management Mode **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamic Power Management** 0: Disable 1: Enable
6	RW	0	**Power Management During HALT / SHUTDOWN** 0: Disable 1: Enable
5	RW	0	**Power Management During STPCLK** 0: Disable 1: Enable
4	RW	0	**Power Management During Suspend State** 0: Disable 1: Enable
3:0	RO	0	**Reserved**

Offset Address: A1h (D0F4)
DRAM Power Management **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable DRAM Self-Refresh During Power-Management Mode** 0: Disable 1: Enable
6	RW	0	**Dynamic CKE When DRAM Idle** 0: Disable 1: Enable Note: Before entering STR Mode, please turn off this bit
5	RW	0	**Dynamic Power Down DRAM I/O Pad** (i.e. Float) 0: Disable 1: Enable
4:0	RO	0	**Reserved**

Note: The DRAM power management mode is defined as HALT / SHUTDOWN, STPCLK and Suspend State triggered.

Offset Address: A2h (D0F4)
Dynamic Clock Stop Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Host Interface Power Management** 0: Disable 1: Enable
6	RW	0	**DRAM Channel A Interface Power Management** 0: Disable 1: Enable
5	RO	0	**Reserved**
4	RW	0	**DBX Interface Power Management** 0: Disable 1: Enable
3	RW	0	**APIC Interface Power Management** 0: Disable 1: Enable
2	RW	0	**Graphics Interface (GMINT) Power Management** 0: Disable 1: Enable
1	RW	0	**NM Configuration Interface Power Management** 0: Disable 1: Enable
0	RO	0	**Reserved**

Offset Address: A3h (D0F4)
MA / SCMD Pad Toggle Reduction **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Toggle Reduction on DRAM MA / SCMD Signals** (i.e. do not switch MA / SCMD signal if not accessed) 0: Disable 1: Enable
6:0	RO	0	**Reserved**

Offset Address: A4h (D0F4) – Reserved

Offset Address: A5h (D0F4)
Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Dynamically Gates Phase Signals on Pseudo Synchronous Conversion Circuit Between Host/DRAM Interface** 0: Disable 1: Enable
6:1	RO	0	**Reserved**
0	RW	0	**Enable Dynamic Clock STOP for PE1 Port for PHY** 0: Disable 1: Enable

Offset Address: A6-A7h (D0F4) – Reserved

Offset Address: A8h (D0F4)
PCIe Dynamic Clock Stop **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Dynamic Clock STOP for PEG0 Port for PHY** 0: Disable 1: Enable
6	RW	0	**Enable Dynamic Clock STOP for PE0 Port for PHY** 0: Disable 1: Enable
5	RW	0	**Central Traffic Controller Dynamic Clock STOP** 0: Disable 1: Enable
4	RW	0	**PEG0 Dynamic Clock STOP** 0: Disable 1: Enable
3:2	RO	0	**Reserved**
1	RW	0	**PE1 Dynamic Clock STOP** 0: Disable 1: Enable
0	RW	0	**PE0 Dynamic Clock STOP** 0: Disable 1: Enable

Offset Address: A9h (D0F4)
PCIe Power Management Registers 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Transaction Layer (TRANS) Downstream Request Gating Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
6	RW	0	**TRANS Downstream Non-Posted Cycle Gating Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
5	RW	0	**TRANS Downstream Flow Control Update / Lock Cycle / NA State Machine Dynamic Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
4	RW	0	**TRANS Downstream DBX Dynamic Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
3	RW	0	**TRANS Upstream Request Gating Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
2	RW	0	**TRANS Upstream Read Cycle Gating Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
1	RW	0	**TRANS Upstream Write Cycle Gating Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
0	RW	0	**TRANS Upstream DBX Gating Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock

Offset Address: AAh (D0F4)

PCIe Power Management Registers 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**L1 State PCIe Dynamic Clock Stop Control - PEG0** 0: Disable dynamic clock 1: Enable dynamic clock
1	RW	0	**L1 State PCIe Dynamic Clock Stop Control - PE0** 0: Disable dynamic clock 1: Enable dynamic clock
0	RW	0	**L1 State PCIe Dynamic Clock Stop Control - PE1** 0: Disable dynamic clock 1: Enable dynamic clock

Offset Address: ABh (D0F4)

PCIe Power Management Registers 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DLLM Downstream DLLP Schedule Gating Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
6	RW	0	**DLLM Downstream TLP Schedule Gating Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
5	RW	0	**DLLM Upstream Gating Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
4:0	RO	0	**Reserved**

Offset Address: ACh (D0F4)

PCIe Power Management Registers 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Link Active Gating Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
5	RW	0	**Sync NM Configuration Register Bits Gating Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
4	RW	0	**OS Generate and Manipulation Gating Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
3	RW	0	**Timer/Counter Gating Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
2	RW	0	**Lane Gating Clock Control** 0: Disable dynamic clock 1: Enable dynamic clock
1:0	RO	0	**Reserved**

Offset Address: ADh (D0F4)

PCIe Power Management Registers 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Power Management for Word Alignment Control** 0: Disable 1: Enable

Offset Address: AEh (D0F4)

PCIe Power Management Registers 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**PEG0 250MHz ECLK Gated** 0: This bit has no effect on ECLK 1: ECLK is gated by this bit from Clock Group Center
1	RW	0	**PE0 250MHz ECLK Gated** 0: This bit has no effect on ECLK 1: ECLK is gated by this bit from Clock Group Center
0	RW	0	**PE1 250MHz ECLK Gated** 0: This bit has no effect on ECLK 1: ECLK is gated by this bit from Clock Group Center

Offset Address: AF-CFh (D0F4) – Reserved

Offset Address: DF-D0h (D0F4)

BIOS Extended Scratch Registers D **Default Value: 0**

Bit	Attribute	Default	Description
127:0	RW	0	**BIOS Extended Scratch Registers D**

Offset Address: E3-E0h (D0F4)

BIOS Extended Scratch Registers E **Default Value: 0**

Bit	Attribute	Default	Description
127:0	RW	0	**BIOS Extended Scratch Registers E**

Offset Address: E4-FFh (D0F4) – Reserved

Device 0 Function 5 (D0F5): APIC and Central Traffic Control

Header Registers (00–3Fh)

Offset Address: 01-00h (D0F5)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F5)

Device ID **Default Value: 5353h**

Bit	Attribute	Default	Description
15:0	RO	5353h	**Device ID – For Power Management Control**

Offset Address: 05-04h (D0F5)

PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0 (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F5)

PCI Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR# asserted)**
13	RW1C	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort
10:9	RO	00b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RW1C	0	**Master Data Parity Error** This bit is set when bus master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F5)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D0F5)

Class Code **Default Value: 08 0020h**

Bit	Attribute	Default	Description
23:0	RO	080020h	**Class Code**

Offset Address: 0Ch (D0F5)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D0F5)

Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer**

Offset Address: 0Eh (D0F5)

Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type**

Offset Address: 0Fh (D0F5)
Build In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Build In Self Test (BIST)**

Offset Address: 10-2Bh (D0F5) – Reserved

Offset Address: 2D-2Ch (D0F5)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F5)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F5) – Reserved

Offset Address: 34h (D0F5)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability Pointer**

Offset Address: 35-3Fh (D0F5) – Reserved

Legacy APIC Base I/O Registers (40–5Fh)

Offset Address: 40h (D0F5)
APIC Legacy Configuration **Default Value: 4Ch**

Bit	Attribute	Default	Description
7	RW	0	**Legacy APIC** 0: Disable 1: Enable. Range FECxyz00 to FECxyzFF, where x,y,z are defined in Rx40[3:0] and Rx41[7:0]
6	RO	1b	**Reserved** (Do not program)
5	RW	0	**Issues MSI Cycle for the Interrupt Deassertions** 0: Disable. There will be no corresponding MSI cycle for IRQ deassertion. 1: Enable. IRQ assertion and de-assertion will both issue MSI cycle out.
4	RO	0	**Reserved**
3:0	RW	Ch	**APIC Legacy Address Range – x** Value can be programmed from 0h~Fh

Offset Address: 41h (D0F5)
APIC Legacy Address Range – y / z **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**APIC Legacy Address Range – y** Value can be programmed from 0h~Fh
3:0	RW	0	**APIC Legacy Address Range – z** Value can be programmed from 0h~Fh

Offset Address: 42h (D0F5)
APIC Interrupt Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Disable INTx Transparent Mode** 0: Enable Transparent mode 1: Disable Transparent mode
2	RW	0	**APIC Nonshare Mode Enable** 0: Disable 1: Enable
1	RW	1b	**Interrupt Disable Function of the APIC Module** 0: Disable 1: Enable
0	RW	1b	**Boot Interrupt Function** 0: Disable 1: Enable

Offset Address: 43h (D0F5) – Reserved

Offset Address: 44h (D0F5)
Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**For PEG0, Configuration Cycles to the Secondary Bus behind the P2P Bridge** 0: Configuration cycles for all the devices will be passed through. 1: Only configuration cycles for device 0 will be passed to the secondary bus.
6:2	RO	0	**Reserved**
1	RW	0	**PCIe Device Uses MSI Cycle Wake Up System from C3** 0: Disable 1: Enable
0	RW	0	**APIC Data Voltage for CPU Voltage Select** 0: 2.5V 1: 1.5V

Offset Address: 45-46h (D0F5) – Reserved

Offset Address: 47h (D0F5)
Device Strapping Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Strapping Value for P2 Device Value**
3:0	RW	0	**Strapping Value for NM Device Value**

Offset Address: 48h (D0F5)
Device Strapping Value of PCIX and PCIe **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Strapping Value for PCIX Device Value**
3:0	RW	0	**Strapping Value for PCIe Device Value**

Offset Address: 49-5Fh (D0F5) – Reserved

Central Traffic - Downstream Control (60–7Fh)

Offset Address: 60h (D0F5)

Extended CFG Address Support **Default Value: 28h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	1b	**Convert Device-2 CF8 Cycles to Device-1 while Passing it to the SM (in PCIe Mode)** 0: CF8 access cycles are passed to the SM normally 1: CF8 with data[15:11]=00010 will be changed to data[15:11]=00001
4	RW	0	**CF8 Byte Write Enable** 0: Only supports CF8 write with all byte-enable active 1: Allow CF8 write with partial byte-enable active
3	RW	1b	**For Device 2 and Device 3, Configuration Cycles to the Secondary Bus behind the P2P Bridge** 0: Configuration cycles for all the devices will be passed through. 1: Only configuration cycles for device 0 will be passed to the secondary bus.
2	RO	0	**Reserved**
1:0	RW	00b	**Extended CFG Mode** 00: Extended CFG mode is off 01: Reserved 10: Capability header for extended configuration address supported 11: Memory mapped extended CFG address supported (Rx61[7:0] should also be programmed)

Offset Address: 61h (D0F5)

Memory Mapped Extended CFG Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Extended Configuration Address: A[35:28]** 00h: No extended configuration address Other: Extended configuration address A[35:28] from host side

Offset Address: 62h (D0F5)

Memory Mapped Extended RCRB Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**RCRB Base Address** 00h: No RCRB is supported

Offset Address: 63h (D0F5) – Reserved

Offset Address: 64h (D0F5)
Miscellaneous 1 **Default Value: F2h**

Bit	Attribute	Default	Description
7	RW	1b	**Block P2P Request During Arbiter Disable** 0: Non-block 1: Block
6	RW	1b	**Central Traffic Controller Split GFX 1/8QW Request Into DW Access** 0: Disable 1: Enable
5	RW	1b	**Upstream MSI Cycles Forces Flush of the Queued P2C Write Data** 0: Disable 1: Enable Note: Upstream MSI cycles include FEEx_xxxx from the internal APIC and cycles with address as programmed in Rx74-7B of Dev2, Dev3 Fun0-3.
4	RW	1b	**Downstream C2P Forces Flush of the Upstream P2C Write to the Host Side before Return LRDY to the Host Side** 0: Disable 1: Enable Note: C2P Downstream cycles include MEMR, IOR and IOW
3	RW	0	**Downstream to PCIe Cycle Being Blocked During EPLL Gated/Reset** 0: Disable 1: Enable
2	RW	0	**Block ACK for Upstream PCIe Cycle During PLL1 Gated/Reset** 0: Disable 1: Enable
1	RW	1b	**Downstream Write Request Timing** 0: Wait for the write data to issue downstream request 1: Issue downstream request once request from the host is received
0	RW	0	**Traffic Controller Downstream Cycles Are Processed in Order** 0: Disable. Downstream post write transaction can be issued out before the completion of the data phase of the previous read transaction. 1: Enable. Downstream post write transaction won't be issued out until the data phase of the previous read transaction is finished.

Offset Address: 65h (D0F5)
Address FED4_xxxx Upstream Redirection **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	000b	**PCIe Port Select to End the Illegal TPM Cycle** (Upstream with Address FED4_xxxx) 000: An upstream cycle with address FED4_xxxx will redirect to PEG0 010: An upstream cycle with address FED4_xxxx will redirect to PE0011: An upstream cycle with address FED4_xxxx will redirect to PE1 Others: Reserved
3:0	RO	0	**Reserved**

Offset Address: 67-66h (D0F5)
Miscellaneous 2 **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:0	RW	0	**Trusted Configuration Space Base Address for PE0-PE1, PEG0**

Offset Address: 6B-68h (D0F5)
Memory Mapped Extended RCRBH Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:0	RO	0	**RCRBH Base Address Is Composed By RCRBH[35:12] and Register – Map to Address [11:2]** RCRBH addressing is enabled when RCRBH[35:12] != 'h00

Offset Address: 6C -7Fh (D0F5) – Reserved

Central Traffic - Upstream Control (80-85h)

Offset Address: 80h (D0F5)

Central Traffic-Upstream Control 1 **Default Value: 90h**

Bit	Attribute	Default	Description
7	RO	1b	**PCI Express (PEG0) Interface Selection** 0: PCI Express (PEG0) interface is not supported 1: PCI Express (PEG0) interface is supported
6	RW	0	**VC1 Upstream Path** 0: VC1 requests are forwarded to the host side (snoop) 1: VC1 requests are forwarded to the DRAMC side. Those required snoops are reported as MalFunction TLPs.
5	RW	0	**CPU-to-Memory FIFO (CMFIFO) Snoop Policy for Upstream Request to DRAMC** 0: Upstream requests are sent to DRAMC directly. 1: Upstream requests to DRAMC have to wait for the snoop result from CPU-to-Memory FIFO. When hit, DRAMC will postpone handling these upstream requests till cycles in the CMFIFO been flushed to the DRAM.
4	RO	1b	**Reserved** (Do not program)
3	RW	0	**Upstream Request 1T earlier** 0: Normal latency for upstream request 1: Reduced 1T latency for upstream request
2	RW	0	**Host Side Upstream Write** Transaction ends with 1T earlier notice. 0: Disable 1: Enable
1	RW	0	**Host Side Upstream Read Data Returning Path** 0: 2-level synchronous FIFO 1: 1-level synchronous FIFO
0	RW	0	**Host Side Upstream Write, Data Return With a 1T Notice** 0: Disable 1: Enable

Offset Address: 81h (D0F5) – Reserved

Offset Address: 82h (D0F5)

Central Traffic-Upstream Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Non-posted Request Queue Size** 0: 1 level 1: 2 level
6	RW	0	**Traffic Controller Blocks Upstream Request in C3 Mode** 0: Block all upstream requests(except PCCA) until deassertion of Arbiter Disable 1: Block all upstream requests(except PCCA) until receiving STPCLK# deassert msg.
5	RW	0	**PCIe VC1 Read/Write Ordering Rule** 0: Obey PCIe VC1 read/write ordering rule 1: PCIe VC1 read cycle can pass VC1write cycle
4	RW	0	**PCIe VC1 Command Rate** 0: PCIe VC1 reads/writes in 2T command rate 1: PCIe VC1 reads in 2T command rate, but writes in 1T command rate
3:2	RO	0	**Reserved**
1	RW	0	**Fair Arbitration Latency for the Host Side Arbitration Unit at D0F0 Extended Register Space Rx230 - Rx23D** 0: 2T 1: 1T
0	RW	0	**Port Arbitration Latency for the Port Arbitration Unit at D0F0 Extended Register Space Rx210 - Rx219** 0: 2T 1: 1T

Offset Address: 83h (D0F5)

Downstream Arbitration Timeout Timer Control **Default Value: 11h**

Bit	Attribute	Default	Description
7:4	RW	0001b	**P2PW (PCI-to-PCI Write) Downstream Arbitration Timeout Timer** (* 4 LCLK) 0000: Occupancy timer is off, i.e. the arbitration will be in a fairly RR scheme. 0001: 4 T 0010: 2 x 4 T ….. 1111: 15 x 4 T (* 4 LCLK) Note: LCLK is a clock name which is equal to Host Clock (HCLK)
3:0	RW	0001b	**P2PR (PCI-to-PCI Read) Downstream Arbitration Timeout Timer** (* 4 LCLK) 0000: Occupancy timer is off, i.e. the arbitration will be in a fairly RR scheme. 0001: 4 T 0010: 2 x 4 T ….. 1111: 15 x 4 T (* 4 LCLK)

Offset Address: 84h (D0F5)

Upstream Control – for the VC1 Paths **Default Value: 08h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	1000b	**Downstream Arbitration Timeout Timer for C2P (* 4 LCLK)** 0000: Occupancy timer is off, i.e. the arbitration will be in a fairly RR scheme. 0001: 4 T 0010: 2 x 4 T ….. 1111: 15 x 4 T (* 4 LCLK)

Offset Address: 85h (D0F5)

P2P Related Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Abort P2P Cycle Issued to PCI1, Discard Write, Return FF for Read** 0: Disable 1: Enable
6	RW	0	**CPU to PCI1 Read Cycle Blocks the Following C2P Cycle** 0: Disable 1: Enable
5	RO	0	**Reserved**
4	RW	0	**PCIe P2C Cycles Request for Arbitration 1T Earlier for P2P Issues** 0: Arbitrate as PCIe requests queue is not empty 1: Arbitrate for 1T earlier.
3	RW	0	**PCIe P2CR Cycles Do Not Flush PCIe P2PR Cycles** 0: Flush 1: Not Flush
2:1	RO	0	**Reserved**
0	RW	0	**Use Previous Stage of P6IF Read Data Ready Signal** 0: Disable 1: Enable

Offset Address: 86-9Fh (D0F5) – Reserved

PCIe Message Controller and Power Management (A0–FFh)

Offset Address: A0h (D0F5)

PCIe PMU Control and Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RWS	0	**PCI Express Wake Activation Control** 0: Disable 1: Enable
6	RW	0	**PCI Express PME SCI (System Control Interrupt to Indicate Power Management Event) Activation Control** 0: Disable 1: Enable
5	RW	0	**PCI Express Hot-Plug SCI (System Control Interrupt to Indicate Hot-Plug Event) Activation Control** 0: Disable 1: Enable
4	RW1C	0	**PEG0 L2L3 PME Acknowledge Status** 0: Disable 1: 1 indicates that upon set RxF0[7] to 1, PEG0 goes to L2L3 ready state and PME_TO_ACK message has been returned from the device at PEG0.
3:2	RO	0	**Reserved**
1	RW1C	0	**PE1 L2L3 PME Acknowledge Status** 0: Disable 1: 1 indicates that upon set RxF0[7] to 1, PE1 goes to L2L3 ready state and PME_TO_ACK message has been returned from the device at PE1.
0	RO	0	**Reserved**

Offset Address: A1h (D0F5)

PCIe PMU Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**PM_PME Message Status** 0: No PM_PME message 1: At least one PM_PME message was received at the PCIe ports Note: Wake up the system through either PEWAKE# or PEPMESCI# depends on the settings on RxA0[7:6].
6	RW1C	0	**PEG0 L2L3 PME Acknowledge Status** 0: Disable 1: 1 indicates that upon set RxF0[7] to 1, PEG0 goes to L2L3 ready state and PME_TO_ACK message has been returned from the device at PEG0.
5	RO	0	**Hot Plug Event Status** 0: No Hot Plug event 1: At least one Hot Plug event was received at the PCIe ports. This event is triggered by PEHPSCI# (check RxA0[5] for activation control.)
4:0	RO	0	**Reserved**

Offset Address: A2h (D0F5)

PMU Downstream Address [15:8] **Default Value: 40h**

Bit	Attribute	Default	Description
7:0	RW	40h	**Downstream Address Bits [15:8]** This register is used for monitoring S3/S4/S5 downstream command. Refers to RxA3[7] for address [7].

Offset Address: A3h (D0F5)

PMU Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Address Bit [7]** This bit is used for monitoring S3/S4/S5 downstream command. Refers to RxA2 for address [15:8].
6:1	RO	0	**Reserved**
0	RW	0	**Monitor S3/S4/S5 Command** 0: Disable 1: Enable When enable, the controller will monitor S3/S4/S5 commands (e.g. IOW 4005, 'h24 or 'h28) in the following procedure: 1. The controller receives the STPGNT cycles from the CPU 2. The controller triggers MSGC to issue PME_TURNOFF message to PCIe devices (D2F0, D2Fx) 3. The controller waits for the acknowledge from all the devices to issue the STPGNT cycle received in step 1 to SM.

Offset Address: A4-EF(D0F5) – Reserved

Offset Address: F0h (D0F5)

PMU Control 2 **Default Value: 26h**

Bit	Attribute	Default	Description
7	RW	0	**PCIe Device Power Management Control** 0: Disable 1: Enable Programmed this bit to 1 will trigger a PME_TURNOFF message sent to PCIe Root Ports, where devices are activated. This bit has to be programmed to 0 before it can be programmed to 1 again.
6	RO	0	**Reserved**
5	RW	1b	**Device 2 Function 0 Exist or Not** 0: Absent 1: Exist
4	RW	0	**Device 3 Function 3 Exist or Not** 0: Absent 1: Exist
3	RW	0	**Device 3 Function 2 Exist or Not** 0: Absent 1: Exist
2	RW	1b	**Device 3 Function 1 Exist or Not** 0: Absent 1: Exist
1	RW	1b	**Device 3 Function 0 Exist or Not** 0: Absent 1: Exist
0	RO	0	**Reserved**

Note: For the PCIe port support, please refer to the PCIe Port Support table in D2F0 for details.

Offset Address: F1h (D0F5)

Device 1 / 2 Configuration Control 1 **Default Value: 02h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	1b	**Device 1 Exist or Not** 0: Absent 1: Exist
0	RW	0	**Device 2 Function 1 Exist or Not** 0: Absent 1: Exist

Offset Address: F2h (D0F5) – Reserved

Offset Address: F3h (D0F5)

PCIe EPHY Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	1b	**Enable PCIe EPHY** This bit can control the highest-level power-on control pin of PCIe 6 lanes. 0: Power down 99 percent of analog circuit inside EPHY. 1: Power on analog circuit inside EPHY.
0	RW	1b	**Reset Control of PCIe PLL** 0: Reset asserted 1: Reset deasserted

Offset Address: F4-FFh (D0F5) – Reserved

Device 0 Function 6 (D0F6): Scratch Registers

Header Registers (00-3Fh)

Offset Address: 01-00h (D0F6)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F6)

Device ID **Default Value: 6353h**

Bit	Attribute	Default	Description
15:0	RO	6353h	**Device ID Code**

Offset Address: 05-04h (D0F6)

PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0 (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F6)
PCI Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error (SERR# asserted)**
13	RW1C	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort
10:9	RO	00b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RW1C	0	**Master Data Parity Error** This bit is set when bus master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F6)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**North Module Chip Revision ID**

Offset Address: 0B-09h (D0F6)
Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F6) – Reserved

Offset Address: 0Dh (D0F6)
PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**PCI Bus Time Slice for CPU as a Master** (in Unit of PCI clocks)
2:0	RO	0	**Reserved** Bit [2:1] is programmable; however, it's read as 0

Offset Address: 0Eh (D0F6)
Header Type **Default Value: 00 or 80h**

Bit	Attribute	Default	Description
7:0	RO	00 or 80h	**Header Type** Could be 80 when D0F0 Rx4F[0] = 1

Offset Address: 0Fh (D0F6)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST Support** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 10-2Bh (D0F6) – Reserved

Offset Address: 2D-2Ch (D0F6)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F6)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F6) – Reserved

Offset Address: 34h (D0F6)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** An offset address from the start of the configuration space

Offset Address: 35-3Fh (D0F6) – Reserved

Scratch Registers (40-7F)

Offset Address: 4F-40h (D0F6)
BIOS Scratch Register 1 **Default Value: 0**

Bit	Attribute	Default	Description
127:0	RW	0	**BIOS Scratch Register**

Offset Address: 5F-50h (D0F6)
BIOS Scratch Register 2 **Default Value: 0**

Bit	Attribute	Default	Description
127:0	RW	0	**BIOS Scratch Register**

Offset Address: 6F-60h (D0F6)
BIOS Scratch Register 3 **Default Value: 0**

Bit	Attribute	Default	Description
127:0	RW	0	**BIOS Scratch Register**

Offset Address: 7F-70h (D0F6)
BIOS Scratch Register 4 **Default Value: 0**

Bit	Attribute	Default	Description
127:0	RW	0	**BIOS Scratch Register**

Offset Address: 80-BFh (D0F6) – Reserved

Hash Data Control Registers (C0–FFh)

Offset Address: C3-C0h (D0F6)
Hash Start Base Address Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Hash Start Base Address[31:2]**
1:0	RO	0	**Reserved**

Offset Address: C5-C4h (D0F6)
Hash Start Base Address High **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3:0	RW	0	**Hash Start Base Address[35:32]**

Offset Address: C6-C7h (D0F6) – Reserved

Offset Address: CB-C8h (D0F6)
Hash Start Size **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Set Hash Cycle as Branch Trace Message Cycle** The hash cycle will be a branch message cycle when this bit is set to 1.
30	RW	0	**Set Hash Cycle as IO Cycle** The hash cycle will be an IO cycle when this bit is set to 1.
29	RW	0	**Set Hash Cycle as Memory Cycle** The hash cycle will be a MEM cycle when this bit is set to 1.
28	RW	0	**Set Hash Cycle as Special Cycle** The hash cycle will be a special cycle when this bit is set to 1.
27:20	RW	0	**Special Cycle Select for Hash Start Cycle** Indicates which special cycle will be used as a hash start cycle.
19:0	RW	0	**Size XOR Bits** If bit[i] (i=0..19) is set to 1, the corresponding bit in Hash Start Base Address (RxC0[19:0]) will be ignored.

Offset Address: CCh (D0F6)

TPM (Trusted Platform Module) Function Support **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Forward CPU Cycle to Protected TPM Reserved Range** 00: The host controller will forward the CPU cycle which hits TPM reserved range to the SM. Others: The host controller will accept the CPU cycle which hits TPM reserved range, but will not do anything further.
5	RW	0	**TPM Hash Decode and Transmit** Enable TPM hash start/end/data address decoding and transmit a cycle with addr=FED4_4028/FED4_4020/FED4_4024. 0: Disable 1: Enable
4	RW	0	**TPM Transmit in Mem / IO Ccyle Select** Enable to forward the cycle which hits TPM hash data address to NSMIC by IO Command 0: Transmit in memory cycle 1: Transmit in IO cycle
3:0	RO	0	**Reserved**

Offset Address: CD-CFh (D0F6) – Reserved

Offset Address: D3-D0h (D0F6)

Hash End Base Address Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Hash End Base Address[31:2]**
1:0	RO	0	**Reserved**

Offset Address: D5-D4h (D0F6)

Hash End Base Address High **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3:0	RW	0	**Hash End Base Address[35:32]**

Offset Address: D6-D7h (D0F6) – Reserved

Offset Address: DB-D8h (D0F6)

Hash End Size **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**The Hash Cycle Will Be A Branch Message**
30	RW	0	**The Hash Cycle Will Be An IO Cycle**
29	RW	0	**The Hash Cycle Will Be A MEM Cycle**
28	RW	0	**The Hash Cycle Will Be A Special Cycle**
27:20	RW	0	**Special Cycle Select for Hash End Cycle** If bit 28 = 1, then the Hash Cycle will be a special cycle. In addition, if bit[27:20] are equal to corresponding byte enabling bits of CPU request, this special cycle will be used as a Hash End Cycle.
19:0	RW	0	**Size XOR Bits** If bit[i] (i=0..19) is set to 1, the corresponding bit in Hash End Base Address (RxD0[19:0]) will be ignored.

Offset Address: DC-DFh (D0F6) – Reserved

Offset Address: E3-E0h (D0F6)
Hash Data Base Address Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Hash Data Base Address[31:2]**
1:0	RO	0	**Reserved**

Offset Address: E5-E4h (D0F6)
Hash Data Base Address High **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3:0	RW	0	**Hash Data Base Address[35:32]**

Offset Address: E6-E7h (D0F6) – Reserved

Offset Address: EB-E8h (D0F6)
Hash Data Size **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**The Hash Cycle Will Be A Branch Message**
30	RW	0	**The Hash Cycle Will Be An IO Cycle**
29	RW	0	**The Hash Cycle Will Be A MEM Cycle**
28	RW	0	**Control TPM Data From High DW or Low DW** 0: From Low DW 1: From High DW
27:20	RW	0	**Reserved**
19:0	RW	0	**Size XOR Bits** If bit[i] (i=0..19) is set to 1, the corresponding bit in Hash Data Base Address (RxE0[19:0]) will be ignored.

Offset Address: EC-FFh (D0F6) – Reserved

Device 0 Function 7 (D0F7): North-South Module Interface Control

Header Registers (00-3Fh)

Offset Address: 01-00h (D0F7)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technologies ID Code**

Offset Address: 03-02h (D0F7)

Device ID **Default Value: 7353h**

Bit	Attribute	Default	Description
15:0	RO	7353h	**Device ID – North-South Module Interface**

Offset Address: 05-04h (D0F7)

PCI Command **Default Value: 0006h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0 (Not supported)
8	RO	0	**SERR# Enable** Hardwired to 0 (Not supported)
7	RO	0	**Address / Data Stepping** Hardwired to 0 (Not supported)
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0 (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles)
2	RO	1b	**PCI Master Function** Hardwired to 1 (May behave as a bus master)
1	RO	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access)
0	RO	0	**I/O Space Access** Hardwired to 0 (Does not respond to I/O space)

Offset Address: 07-06h (D0F7)

PCI Status **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error** (SERR# asserted)
13	RW1C	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip dose not assert Target-Abort
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RW1C	0	**Master Data Parity Error** This bit is set when bus master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as A Target** Hardwired to 0 (Not implemented)
6	RO	0	**User Definable Features** Hardwired to 0
5	RO	0	**66 MHz Capable** Hardwired to 0 (Not implemented)
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D0F7)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D0F7)

Class Code **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D0F7)

Cacheline Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cacheline Size**

Offset Address: 0Dh (D0F7)

PCI Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**PCI Bus Time Slice for CPU as a Master** (in Unit of PCI clocks)
2:0	RO	0	**Reserved** Bit[2:1] are programmable; however, it's read as 0.

Offset Address: 0Eh (D0F7)
Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00	**Header Type**

Offset Address: 0Fh (D0F7)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST Support** Hardwired to 0 (Not supported)
6:0	RO	0	**Reserved**

Offset Address: 10-2Bh (D0F7) – Reserved

Offset Address: 2D-2Ch (D0F7)
Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D0F7)
Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW1	0	**Subsystem ID**

Offset Address: 30-33h (D0F7) – Reserved

Offset Address: 34h (D0F7)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Capability List Pointer** An offset address from the start of the configuration space

Offset Address: 35-3Fh (D0F7) – Reserved

North-South Module Interface Control (40–60h)

Offset Address: 40h (D0F7)
Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:1	RW	00b	**Options of Combining Multiple STPGNT Cycles into NSMIC Command** 00: Compatible mode: a NSMIC command per STPGNT cycle 01: Combines 2 STPGNT cycles into a NSMIC command 10: Combines 3 STPGNT cycles into a NSMIC command 11: Combines 4 STPGNT cycles into a NSMIC command
0	RW	0	**0CF8h Configuration Cycle Address Bit[27:24] Usage** 0: Normal PCI usage 1: Address bit[27:24] are used as extended register address bit[11:8]

Offset Address: 41-4Fh (D0F7) – Reserved

Offset Address: 50h (D0F7)
Enable PCI1 MMIO Cycle Loopback **Default Value: 0nh**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	dip	**PLL_OK Signal Source Selection** 0: Use PLL_OK from PLL 1: Use PLL_OK from the PLLOK counter Default is set by the strapping signal PDA2 during system initialization. For strap pin information, check the Strap Pin table for details.

Offset Address: 51-56h (D0F7) – Reserved

Offset Address: 57h (D0F7)
DRAM Bank 7 Ending Address **Default Value: 04h**

Bit	Attribute	Default	Description
7:0	RO	04h	**DRAM Bank 7 Ending Address (Host Address Bits[31:24])**

Offset Address: 58-60h (D0F7) – Reserved

Shadow RAM Control (61-6Fh)

Offset Address: 61h (D0F7)
Page-C ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**CC000-CFFFF** 00: Read/Write disable 01: Write enable 10: Read enable 11: Read/Write enable
5:4	RW	00b	**C8000-CBFFFF**
3:2	RW	00b	**C4000-C7FFFF**
1:0	RW	00b	**C0000-C3FFFF**

Offset Address: 62h (D0F7)

Page-D ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DC000-DFFFF** 00: Read/Write disable 01: Write enable 10: Read enable 11: Read/Write enable
5:4	RW	00b	**D8000-DBFFF**
3:2	RW	00b	**D4000-D7FFF**
1:0	RW	00b	**D0000-D3FFF**

Offset Address: 63h (D0F7)

Page-E ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**EC000-EFFFF** 00: Read/Write disable 01: Write enable 10: Read enable 11: Read/Write enable
5:4	RW	00b	**E8000-EBFFF**
3:2	RW	00b	**E4000-E7FFF**
1:0	RW	00b	**E0000-E3FFF**

Offset Address: 64h (D0F7)

Page-E/F ROM, Memory Hole and SMM Decoding **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:4	RW	00b	**F0000-FFFFF** 00: Read/Write disable 01: Write enable 10: Read enable 11: Read/Write enable
3:2	RW	00b	**Memory Hole** 00: None 01: 512K – 640K 10: 15M – 16M (1M) 11: 14M – 16M (2M)
1	RW	0	**Disable Data Access on SMRAM (Page A, B) during SM mode** 0: In SM mode, page A,B CPU Data R/W cycles are forwarded to NM memory controller. 1: In SM mode, page A,B CPU Data R/W cycles are forwarded to PCI bus (SMRAM page A,B Code R/W cycles are always forwarded to memory controller).
0	RW	0	**Enable Page A, B Access to DRAM** 0: Page A, B CPU R/W cycles could be forwarded to the memory controller or the PCI bus depends on the setting of bit 1 and the CPU operating mode (Normal or SM mode) as well as the type (Code or Data) of the CPU cycle.. 1: Page A, B CPU R/W cycles (Code and Data) are always (in either Normal or SM mode) forwarded to the memory controller. Check the following table for details.

Rx64[1]	Rx64[0]	CPU MODE	Target of CODE Access Cycle	Target of DATA Access Cycle
x	0	Normal	PCI	PCI
0	0	SMM	DRAM	DRAM
1	0	SMM	DRAM	PCI
x	1	Normal / SMM	DRAM	DRAM

Offset Address: 65-6Fh (D0F7) – Reserved

Host-PCI Bridge Control (70-FFh)

Offset Address: 70h (D0F7) – Reserved

Offset Address: 71h (D0F7)
CPU to PCI Flow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Compatible TYPE#1 Configuration Cycle AD31** 0: Fixed AD31 1: AD31 will be 1'b0.
0	RO	0	**Reserved**

Offset Address: 72-75h (D0F7) – Reserved

Offset Address: 76h (D0F7)
PCI Arbitration **Default Value: 80h**

Bit	Attribute	Default	Description
7	RW	1b	**IO Port 22h Cycle Control (South-North Module Interface)** 0: CPU accesses to I/O address 22h are passed to the PCI bus 1: CPU accesses to I/O address 22h are processed internally
6:0	RO	0	**Reserved**

Offset Address: 77-BFh (D0F7) – Reserved

Offset Address: CF-C0h (D0F7)
Write Data for DRAM Channel-C **Default Value: 0**

Bit	Attribute	Default	Description
127:0	RW	0	**Write Data for Write Command** Only Supports Interleave Mode

Offset Address: DF-D0h (D0F7)
Read Data for DRAM Channel-C **Default Value: 0**

Bit	Attribute	Default	Description
127:0	RO	0	**Returned Data for Read Command** Those are Read-Only Registers. DRAM must be programmed to Interleave Mode

Offset Address: E0-FFh (D0F7) – Reserved

Device 2 Function 0 (D2F0) – PCI Express Root Port G0 (PCI-to-PCI Virtual Bridge)

Device 2 Function 0, a 4-Lane PCI Express Root Port, is connected to the PCI bus through AD14 as the IDSEL.
All registers are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with Bus Number 0, Device Number 2 and Function Number 0.

For the PCI Express port support option, please refer to the following table for details.

Table 15. PCIe Port Support

PCIe Port Support	Register Setting	Product
2 x 1 lane	D2F0 RxCF[4]=1 D3F0 RxCF[4]=0 D3F1 RxCF[4]=0 D2F0 RxE2[5]=0 D0F5 RxF3[1]=1 D0F5 RxF0[5]=0 D0F5 RxF0[2]=1 D0F5 RxF0[1]=1	VX820 VX820UT
1 x 4 lane + 2 x 1 lane	D2F0 RxCF[4]=0 D3F0 RxCF[4]=0 D3F1 RxCF[4]=0 D2F0 RxE2[5]=0 D0F5 RxF3[1]=1 D0F5 RxF0[5]=1 D0F5 RxF0[2]=1 D0F5 RxF0[1]=1	VX800
3 x 1 lane	D2F0 RxCF[4]=0 D3F0 RxCF[4]=0 D3F1 RxCF[4]=0 D2F0 RxE2[5]=0 D0F5 RxF3[1]=1 D0F5 RxF0[5]=1 D0F5 RxF0[2]=1 D0F5 RxF0[1]=1	VX800UT

Note: The register setting for every type of PCIe port support should follow the sequence above.

Header Registers (00-3Fh)

Offset Address: 01-00h (D2F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 03-02h (D2F0)

Device ID **Default Value: C353h**

Bit	Attribute	Default	Description
15:0	RO	C353h	**Device ID**

Offset Address: 05-04h (D2F0)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable** Set when the device is prevented from generating INTx messages. 0: Disable 1: Enable
9	RO	0	**Reserved**
8	RW	0	**SERR# Enable** 0: Disable error report. 1: Enable reporting of non-fatal and fatal errors.
7	RO	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors and continue. 1: Take normal action on detected parity errors.
5:3	RO	0	**Reserved**
2	RW	0	**Bus Master Enable** 0: Disable 1: Enable Controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. Disabling this bit is to disable MSI messages.
1	RW	0	**Memory Space** 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the SM. 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.
0	RW	0	**I/O Space** 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the SM. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.

Offset Address: 07-06h (D2F0)
PCI Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set whenever a poisoned TLP is received, regardless the state of Parity Error Enabled (Rx4[6]).
14	RW1C	0	**Signaled System Error** This bit is set when: A device sends an ERR_FATAL or ERR_NONFATAL message. Rx04[8] = 1
13	RW1C	0	**Received Master Abort** This bit is set when receiving a completion with Unsupported Request Completion Status.
12	RW1C	0	**Received Target Abort** This bit is set when receiving a completion with Completer Abort Completion Status.
11	RW1C	0	**Signaled Target Abort** This bit is set when completing a Request with Completer Abort Completion Status.
10:9	RO	0	**Reserved** Always reads 0.
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx04[6] is set and either one of the following two conditions occurs: Requestor receives a Completion marked poisoned. Requestor poisons a write Request.
7:5	RO	0	**Reserved**
4	RO	1b	**Capabilities List** Indicates the presence of an extended capability list item. Always set to 1 for PCI Express device.
3	RO	0	**Interrupt Status** Indicates an INTx message is pending internally.
2:0	RO	0	**Reserved**

Offset Address: 08h (D2F0)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision Code**

Offset Address: 0B-09h (D2F0)
Class Code **Default Value: 06 0400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Ch (D2F0)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size** Reserved

Offset Address: 0Dh (D2F0)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Master Latency Timer** Reserved

Offset Address: 0Eh (D2F0)
Header Type **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Header Type**

Offset Address: 0Fh (D2F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support**

Offset Address: 17-10h (D2F0)
Base Address Register **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RO	0	**Base Address**

Offset Address: 18h (D2F0)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Primary Bus Number**

Offset Address: 19h (D2F0)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Secondary Bus Number**

Offset Address: 1Ah (D2F0)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subordinate Bus Number**

Offset Address: 1Bh (D2F0) – Reserved

Offset Address: 1Ch (D2F0)

I/O Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	Fh	**I/O Base (AD[15:12] - Inclusive)** This bridge will forward the cycles from primary side to PCI if the I/O address AD[15:12] is between I/O base and I/O limit. (Rx1D[7:4]).
3:0	RO	0	**I/O Addressing Capability** 0 means I/O addressing is 16-bit only.

Offset Address: 1Dh (D2F0)

I/O Limit **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**I/O Limit (AD[15:12] - Inclusive)** This bridge will forward the cycles from primary side to PCI if the I/O address is between I/O base (Rx1C) and I/O limit.
3:0	RO	0	**I/O Addressing Capability** 0 means I/O addressing is 16-bit only.

Offset Address: 1F-1Eh (D2F0)

Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set when secondary side receives a poisoned TLP regardless of Rx04[6].
14	RW1C	0	**Received System Error** This bit is set when Rx04[8] is 1 and a device sends an ERR_FATAL or ERR_NONFATAL message.
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RW1C	0	**Signaled Target Abort**
10:9	RO	0	**Reserved**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx04[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned. 2. Requestor poisons a write Request.
7:0	RO	0	**Reserved**

Offset Address: 21-20h (D2F0)

Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Memory Base (AD[31:20] – Inclusive)** The address bits [19:0] are not decoded.
3:0	RO	0	**Reserved**

Offset Address: 23-22h (D2F0)

Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Memory Limit (AD[31:20] – Inclusive)** The address bits [19:0] are not decoded.
3:0	RO	0	**Reserved**

Offset Address: 25-24h (D2F0)
Prefetchable Memory Base **Default Value: FFF1h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Prefetchable Memory Base AD[31:20]**
3:1	RO	0	**Reserved**
0	RO	1b	**Report Support Prefetchable 64 Bits Memory Addressing** 0: Not supported 1: Supported

Offset Address: 27-26h (D2F0)
Prefetchable Memory Limit **Default Value: 0001h**

Bit	Attribute	Default	Description
15:4	RW	0	**Prefetchable Memory Limit AD[31:20]**
3:1	RO	0	**Reserved**
0	RO	1b	**Report Support Prefetchable 64 Bits Memory Addressing** 0: Not supported 1: Supported

Offset Address: 2B-28h (D2F0)
Prefetchable Memory Upper Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:0	RW	0	**AD[35:32]** This chip supports up to 16G.

Offset Address: 2F-2Ch (D2F0)
Prefetchable Memory Upper Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:0	RW	0	**AD[35:32]** This chip supports up to 16G.

Offset Address: 31-30h (D2F0)
Upper I/O Base **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Upper I/O Base 16 Bits Address for PCI**

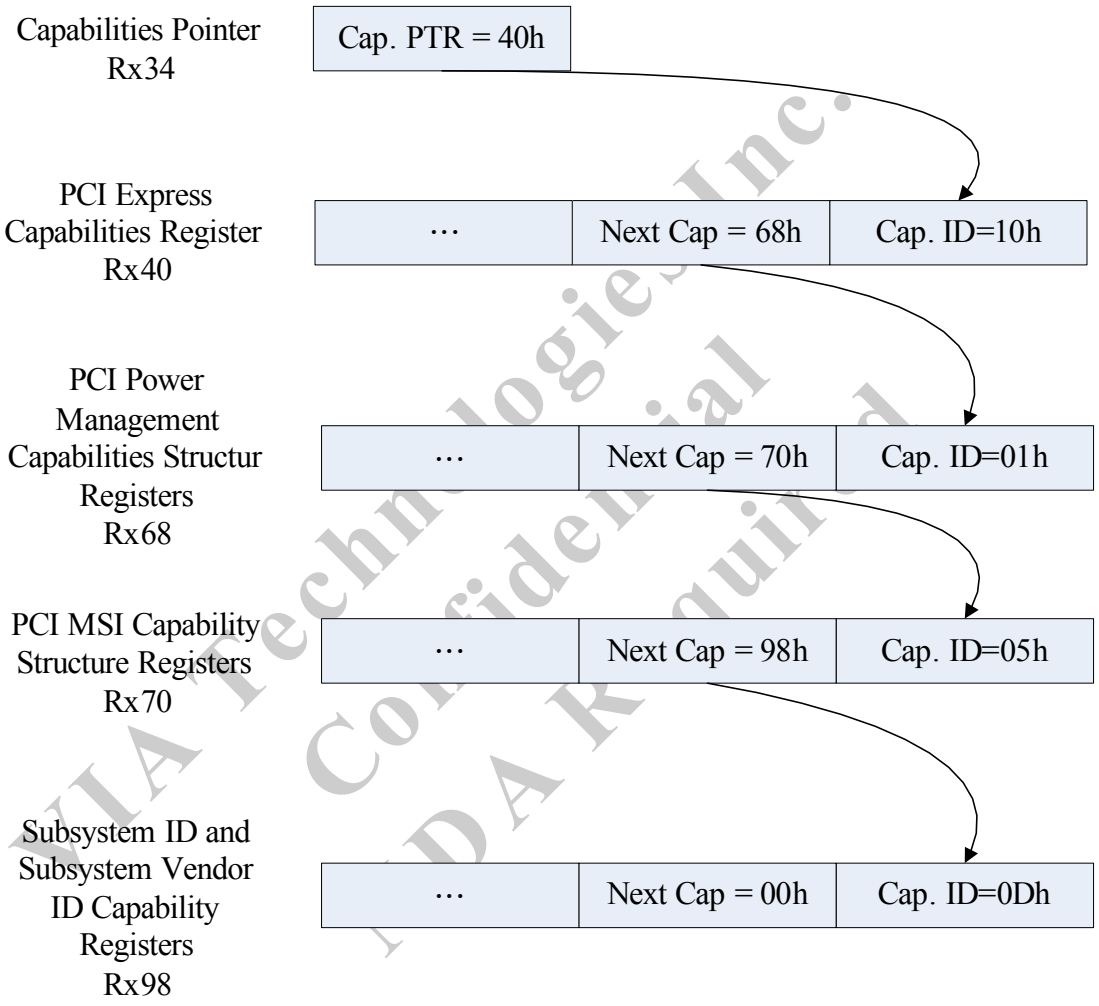
Offset Address: 33-32h (D2F0)
Upper I/O Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Upper I/O Limit 16 Bits Address for PCI**

Offset Address: 34h (D2F0)

Capability Pointer **Default Value: 40h**

Bit	Attribute	Default	Description
7:0	RO	40h	**Capability Pointer** This register contains the offset address from the start of the configuration space. Always reads 40h. Capability Pointer link list: Rx34 → Rx40 → Rx68 → Rx70 → Rx98 → NULL



Offset Address: 35-3Bh (D2F0) – Reserved

Offset Address: 3Ch (D2F0)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**INT Line** (For Software Use Only)

Offset Address: 3Dh (D2F0)
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**INT Pin = INTA#**

Offset Address: 3F-3Eh (D2F0)
Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	RO	0	**Reserved**
6	RW	0	**Secondary Bus Reset** 0: No reset 1: Trigger a warm reset on the corresponding PCI Express Port.
5	RO	0	**Reserved**
4	RW	0	**Base VGA 16 Bits Decode** 0: All VGA alias range will be forwarded. 1: Only forward base VGA range (Alias range will not be forwarded).
3	RW	0	**VGA Compatible I/O and Memory Address Range** 0: Do not forward VGA compatible memory and I/O. 1: Forward VGA compatible memory and I/O. Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses, 3Bx-3Cxh and Color VGA uses3Cx-3Dxh. If a MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.
2	RW	0	**Block / Forward ISA I/O Cycles** 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit. 1:Do not forward ISA I/O that are in the top 768 bytes of each 1K byte block address range.
1	RW	0	**SERR Enable** Controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary. 0: Disable 1: Enable
0	RW	0	**Parity Error Response Enable** 0: Ignore the response to poisoned TLPs. 1: Enable the response to poisoned TLPs.

PCI Express Capability Registers (40-67h)

Offset Address: 41-40h (D2F0)

PCI Express List **Default Value: 6810h**

Bit	Attribute	Default	Description
15:8	RO	68h	**Next Pointer**
7:0	RO	10h	**Capability ID** 10h indicates a PCI Express Capability Structure.

Offset Address: 43-42h (D2F0)

PCI Express Capabilities **Default Value: 0141h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RO	0	**TCS Routing Support** 0: Not supported 1: Supported
13:9	RO	0	**Interrupt Message Number**
8	RO	1b	**Slot Implemented** This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled).
7:4	RO	0100b	**Device / Port Type** 0100b: Root Port of PCI Express Root Complex
3:0	RO	1h	**Capability Version**

Offset Address: 47-44h (D2F0)

Device Capabilities **Default Value: 0000 8001h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:26	RO	0	**Captured Slot Power Limit Scale** Reserved. For upstream port only.
25:18	RO	0	**Captured Slot Power Limit Value** Reserved. For upstream port only.
17:16	RO	0	**Reserved**
15	RO	1b	**Role-Based Error Reporting** 0: Role-based error reporting is not supported 1: Role-based error reporting is supported
14	RO	0	**Power Indicator Present** Reserved. For upstream port or endpoint only.
13	RO	0	**Attention Indicator Present** Reserved. For upstream port or endpoint only.
12	RO	0	**Attention Button Present** Reserved. For upstream port or endpoint only.
11:9	RO	000b	**Endpoint L1 Acceptable Latency**
8:6	RO	000b	**Endpoint L0s Acceptable Latency**
5	RO	0	**Extended Tag Field Supported** 0: 5-bit Tag field supported 1: 8-bit Tag field supported
4:3	RO	0	**Phantom Functions Supported** Reserved
2:0	RO	001b	**Max Payload Size Supported** 001b: 32QW (256 bytes)

Offset Address: 49-48h (D2F0)

Device Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14:12	RO	000b	**Max Read Request Size** 000b: 128 bytes This field sets the maximum Read Request size for the device as a Requestor.
11	RW	0	**Enable No Snoop** 0: Disable 1: Enable If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requestor Attributes of the transactions to indicate that it does not require hardware enforced cache coherence.
10	RWS	0	**Auxiliary Power PM Enable** 0: Disable 1: Enable This bit when set enables device to draw AUX power independent of PME AUX power.
9	RO	0	**Phantom Functions Enable** Not supported.
8	RO/RW	0	**Extended Tag Field Enable** 0: Disable 1: Enable When Rx44[5] is set to 0, this bit is RO. When Rx44[5] is set to 1, this bit is RW.
7:5	RW	0	**Max Payload Size** Maximum TLP payload size.
4	RW	0	**Enable Relaxed Ordering** 0: Disable 1: Enable If this bit is set to 1, the device is permitted to set the Relaxed Ordering bit in the Requestor Attributes of the transactions to indicate that it does not require strong write ordering.
3	RW	0	**Unsupported Request Reporting Enable** 0: Disable 1: Enable
2	RW	0	**Fatal Error Reporting Enable** 0: Disable 1: Enable For a Root Port, the report of Fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	RW	0	**Non-Fatal Error Reporting Enable** 0: Disable 1: Enable For a Root Port, the report of Non-Fatal errors is internal to the root. No external ERR_NONFATAL message is generated.
0	RW	0	**Correctable Error Reporting Enable** 0: Disable 1: Enable For a Root Port, the report of correctable errors is internal to the root. No external ERR_COR message is generated.

Offset Address: 4B-4Ah (D2F0)

Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RO	0	**Transactions Pending** This bit when set indicates that the port has issued Non-Posted Requests on its own behalf (using Requestor ID of the port) which have not been completed.
4	RO	1b	**AUX Power Detected** 0: Not detected 1: Detected
3	RW1C	0	**Unsupported Request Detected** 0: Not detected 1: Detected
2	RW1C	0	**Fatal Error Detected** 0: Not detected 1: Detected
1	RW1C	0	**Non-Fatal Error Detected** 0: Not detected 1: Detected
0	RW1C	0	**Correctable Error Detected** 0: Not detected 1: Detected

Offset Address: 4F-4Ch (D2F0)

Link Capabilities **Default Value: 0118 3C41h**

Bit	Attribute	Default	Description
31:24	RO	01h	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link.
23:21	RO	0	**Reserved**
20	RO	1b	**Data Link Layer Link Active Reporting Capable** 0: Not supported 1: Supported
19	RO	1b	**Surprise Down Error Reporting Capable** This bit indicates support of detecting and reporting a Surprise Down error condition. 0: Not supported 1: Supported
18	RO	0	**Clock Power Management** 0: Not supported 1: Supported
17:15	RO	0	**L1 Exit Latency**
14:12	RO	011b	**L0s Exit Latency**
11:10	RO	11b	**Active State Link PM (ASPM) Support** 11b means entry support of L0S and L1
9:4	RO	01h	**Maximum Link Width** 04h: x4 lanes 02h: x2 lanes 01h: x1 lane
3:0	RO	0001b	**Maximum Link Speed** 0001b: 2.5Gb/s Link speed

Offset Address: 51-50h (D2F0)

Link Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8	RO	0	**Enable Clock Power Management** 0: Disable 1: Enable
7	RW	0	**Extended Synch** 0: FCU Timer limit is 30 us. 1: FCU Timer limit is 120 us.
6	RW	0	**Common Clock Configuration** 0: Indicates that this Port and the component on the opposite end of the Link are operating with **asynchronous** reference clock. 1: Indicates that this Port and the component on the opposite end of the Link are operating with a **distributed common** reference clock.
5	RW	0	**Retrain Link** Link retrain is initiated by writing 1 to this bit. This will direct the Physical Layer LTSSM to the Recovery state.
4	RW	0	**Link Disable** 0: Enable 1: Disable This bit disables the Link when set to 1.
3	RO	0	**Read Completion Boundary** 0: 64 byte
2	RO	0	**Reserved**
1:0	RW	00b	**Active State Link PM (ASPM) Control** 00: Disable 01: Enable L0s Entry 10: Enable L1 Entry 11: Enable L0s and L1 Entry

Offset Address: 53-52h (D2F0)

Link Status **Default Value: 1nn1h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RO	0	**Data Link Layer Link Active** 0: Inactive 1: Active
12	RO	1b	**Slot Clock Configuration** 0: Use an independent clock irrespective of the presence of a reference on the connector. 1: Use the same physical reference clock that the platform provides on the connector.
11	RO	0	**Link Training** This bit indicates the Link training is in progress (Physical Layer LTSSM in Configuration or Recovery state) or the Retrain Link bit is set 1 but Link training has not yet begun. Hardware will clear this bit once Link training is complete.
10	RO	0	**Training Error** Set when a Link training error occurred. Cleared by hardware upon successful training of the Link to the L0 Link state.
9:4	RO	HwInit	**Negotiated Link Width** 000001: x1 000010: x2 000100: x4 Others: Reserved
3:0	RO	0001b	**Link Speed** 0001: 2.5Gb/s negotiated Link speed 0000b: when DLUP =0

Offset Address: 57-54h (D2F0)

Slot Capabilities **Default Value: 0000 0060h**

Bit	Attribute	Default	Description
31:19	RO	0	**Physical Slot Number** Physical slot number attached to the Port.
18	RO	0	**No Command Completed Support** 0: Not supported 1: Supported
17	RO	0	**Electromechanical Interlock Present** 0: Not supported 1: Supported
16:15	RO	0	**Slot Power Limit Scale** Reserved
14:7	RO	0	**Slot Power Limit Value** Reserved
6	RO	1b	**Hot-plug Capable** Reserved (Do not program)
5	RO	1b	**Hot-plug Surprise** Reserved (Do not program)
4	RO	0	**Power Indicator Present** Reserved
3	RO	0	**Attention Indicator Present** Reserved
2	RO	0	**MRL Sensor Present** Reserved
1	RO	0	**Power Controller Present** Reserved
0	RO	0	**Attention Button Present** Reserved

Offset Address: 59-58h (D2F0)

Slot Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved**
12	RW	0	**Enable Data Link Layer State Change Report** 0: Disable 1: Enable
11	RW	0	**Electromechanical Interlock Control** 0: Disable 1: Enable
10	RO	0	**Power Controller Control** Reserved
9:8	RW	0	**Power Indicator Control** Reserved
7:6	RW	0	**Attention Indicator Control** Reserved
5	RW	0	**Hot-Plug Interrupt Enable** Reserved
4	RW	0	**Command Completed Interrupt Enable** Reserved
3	RW	0	**Presence Detect Changed Enable** Reserved
2	RO	0	**MRL Sensor Changed Enable** Reserved
1	RO	0	**Power Fault Detected Enable** Reserved
0	RW	0	**Attention Button Pressed Enable** Reserved

Offset Address: 5B-5Ah (D2F0)

Slot Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8	RW1C	0	**Data Link Layer State Changed** 0: No state changed 1: State changed
7	RO	0	**Electromechanical Interlock Status**
6	RO	0	**Card Presence State** 0: Slot empty 1: Card present in slot
5	RO	0	**MRL (Manually Operated Retention Latch) Sensor State** Reserved
4	RW1C	0	**Command Completed** 0: Not completed 1: Completed
3	RW1C	0	**Presence Detect Changed** 0: Not changed 1: Changed
2	RO	0	**MRL Sensor Changed** 0: Not changed 1: Changed
1	RO	0	**Power Fault Detected** 0: Not detected 1: Detected
0	RW1C	0	**Attention Button Pressed** 0: No state changed 1: State changed

Offset Address: 5D-5Ch (D2F0)

Root Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:5	RO	0	**Reserved**
4	RW	0	**CRS Software Visibility Enable** 0: Disable 1: Enable the Root Port to return Configuration Request Retry Status (CRS) Completion Status to software.
3	RW	0	**PME Interrupt Enable** 0: Disable 1: Enable interrupt generation upon receipt of a PME message as reflected in the PME status register bit. A PME interrupt is also generated if the PME status register bit is set when this bit is set from a cleared state.
2	RW	0	**System Error on Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Fatal Error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
1	RW	0	**System Error on Non-Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Non-Fatal Error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
0	RW	0	**System Error on Correctable Error Enable** 0: Disable 1: Enable generation of a System Error if a Correctable Error (ERR_COR) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.

Offset Address: 5Eh (D2F0)

Root Capabilities Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RO	0	**Capability of CRS Software Visibility** 0: Disabled 1: Enabled. The Root Port will return CRS Completion Status to software.

Offset Address: 5Fh (D2F0) – Reserved

Offset Address: 63-60h (D2F0)

Root Status **Default Value: 000n 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	HwInit	**PME Pending** 0: No pending PME 1: Indicate that another PME is pending when the PME Status (bit 16) is set.
16	RW1C	0	**PME Status** Indicate that the PME was asserted by the Requestor ID indicated in PME Requestor ID (bit[15:0]).
15:0	RO	0	**PME Requestor ID** The Requestor ID of the last PME Requestor.

Offset Address: 64-67h (D2F0) – Reserved

PCI Power Management Capability Structure Registers (68-6Fh)

Offset Address: 6B-68h (D2F0)

Power Management Capabilities **Default Value: C822 7001h**

Bit	Attribute	Default	Description
31:27	RO	19h	**PME Support** 0: Not supported 1: Supported Bit 31, 30 and 27 are set to 1b (PME Message will be forwarded).
26	RO	0	**D2 Support** 0: Not supported 1: Supported
25	RO	0	**D1 Support** 0: Not supported 1: Supported
24:22	RO	0	**AUX Current**
21	RO	1b	**Reserved** (Do not program)
20:19	RO	0	**Reserved**
18:16	RO	010b	**Version**
15:8	RO	70h	**Next Capability Pointer**
7:0	RO	01h	**Capability ID** 01h indicates extended capability ID for the advanced error reporting capability.

Offset Address: 6F-6Ch (D2F0)

Power Management Status / Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Power Management Data**
23:16	RO	0	**Reserved**
15	RW1CS	0	**PME Status** This bit's setting is not modified by hot, warm, or cold reset.
14:9	RO	0	**Reserved**
8	RWS	0	**PME Enable** This bit's setting is not modified by hot, warm, or cold reset.
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** 00b: D0 01b: D1 10b: D2 11b: D3hot

PCI Message Signal Interrupt (MSI) Capability Structure Registers (70-87h)

Offset Address: 73-70h (D2F0)

MSI Capability Support **Default Value: 0180 9805h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24	RO	1b	**Supports Pre-vector Masking Capability** 0: Not supported 1: Supported
23	RO	1b	**Supports 64 Bit Message Address Only** 0: Not supported 1: Supported
22:20	RW	000b	**Multiple Message Enable** 000: 1 message allocated 001: 2 messages allocated 010: 4 messages allocated 011: 8 messages allocated 100: 16 messages allocated 101: 32 messages allocated 11x: Reserved
19:17	RO	000b	**Multiple Messages Capable** 000: 1 message requested 001: 2 messages requested 010: 4 messages requested 011: 8 messages requested 100: 16 messages requested 101: 32 messages requested 11x: Reserved
16	RW	0	**MSI Enable** 0: This Port is prohibited from using MSI to request service. 1: This Port is permitted to use MSI to request service.
15:8	RO	98h	**Next Capability Pointer**
7:0	RO	05h	**Capability ID** 05h indicates the extended capability ID for the root complex link declaration capability.

Offset Address: 77-74h (D2F0)

System-Specified Message Address - Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**System-Specified Message Address Bit [31:2]**
1:0	RO	0	**System-Specified Message Address Bit [1:0]** These bits will always read as 0.

Offset Address: 7B-78h (D2F0)

System-Specified Message Address - High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**System-Specified Message Address Bit [63:32]**

Offset Address: 7D-7Ch (D2F0)

Message Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data** The message data is to be put on data [15:0] of MSI cycles.

Offset Address: 7E-7Fh (D2F0) – Reserved

Offset Address: 83-80h (D2F0)
Message Mask Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RW	0	**Mask Bit for Message 0** 0: Not masked 1: Mask message 0

Offset Address: 87-84h (D2F0)
Message Pending Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RO	0	**Pending Bit for Message 0** 0: Not pending 1: Pending

Message Signal Interrupt (MSI) Capability Registers (88-97h)

Offset Address: 88-97h (D2F0) – Reserved

Subsystem ID and Subsystem Vendor ID Capability Registers (98-9Fh)

Offset Address: 98h (D2F0)
Capability ID **Default Value: 0Dh**

Bit	Attribute	Default	Description
7:0	RO	0Dh	**Capability ID** 0Dh is the capability ID for "Subsystem ID / Subsystem Vendor ID."

Offset Address: 99h (D2F0)
Next Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Pointer**

Offset Address: 9A-9Bh (D2F0) – Reserved

Offset Address: 9D-9Ch (D2F0)
Subsystem Vendor ID Control **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 9F-9Eh (D2F0)
Subsystem ID Control **Default Value: C353h**

Bit	Attribute	Default	Description
15:0	RO	C353h	**Subsystem ID**

PCI Express Transaction Layer Registers (A0-AFh)

Offset Address: A0h (D2F0)

Downstream Control 1 **Default Value: 11h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Cycles Have Traffic Class TC1** 0: Disable 1: Enable
6	RW	0	**Downstream Cycles Have Attribute "No Snoop" Set** 0: Disable 1: Enable
5	RW	0	**Downstream Cycles Have Attribute "Relaxed Ordering" Set** 0: Disable 1: Enable
4	RW	1b	**Downstream Lock Cycle Support** 0: Disable 1: Enable
3	RW	0	**Downstream Arbitration Scheme** 0: Fixed priority: VC1 CPL > VC0 CPL > Down Stream Command 1: Round Robin arbitration priority between VC1 CPL, VC0 CPL and Down Stream Command.
2	RW	0	**Downstream Post-Write Allowed to Pass IOW** 0: Not allowed 1: Allowed
1	RW	0	**Downstream Post-Write Allowed to Pass Read** 0: Not allowed 1: Allowed
0	RW	1b	**Downstream Pipeline** 0: Disable 1: Enable

Offset Address: A1h (D2F0)

Downstream Control 2 **Default Value: 14h**

Bit	Attribute	Default	Description
7	RW1C	0	**Downstream Configuration Completion Status** 0: Normal completion 1: At least one configuration request ended with a CRS completion.
6	RW	0	**TRANS Assert Wait State Control** 0: TRANS cannot assert wait state at receiving downstream write data (original design). 1: TRANS can assert wait state at receiving downstream write data.
5	RW	0	**Data Return of Upstream Read Requests** 0: The chip always checks CPL credit unless the endpoint advertises infinite CPL credits. 1: The chip does not check CPL credit even when endpoint advertises finite CPL credits.
4	RW	1b	**Not Check Downstream PH Credit for PME_TURN_OFF Message** 0: Disable 1: Enable
3	RW	0	**Enable C2P Read Completion Timer for Vector Development Mode** 0: Disable 1: Enable When this bit is set to 1, the timer defined in bit[2:0] becomes: 000: 1 us 001: 3 us 010: 10 us 011: 20 us 100: 50 us 101: 100 us 110: 200 us 111: 500 us
2:0	RW	100b	**C2P Read Completion Timeout Timer** 000: Reserved 001: 1 ms 010: Reserved 011: 10 ms (Spec. lower bound) 100: 30 ms 101: Reserved 11x: Reserved

Offset Address: A2h (D2F0)

Downstream Control 3 **Default Value: 30h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Ordering Queue Timing O ption** 0: 1T setup time 1: 2T setup time
6:4	RW	011b	**Waiting Time for GNT Timer in Priority Arbitration Mode** 000: 4 ns 001: 16 ns 010: 32 ns 011: 64 ns 100: 96 ns 101: 128 ns 110: 256 ns 111: 512 ns If GNT timer of VC0 / C2P request expires, VC0 / C2P request will become higher priority. Priority VC1 > VC0 > C2P request when set RxA0[3] =0
3	RO	0	**Reserved**
2	RW	0	**Pending C2P NP Completion Cycle to Block L1 Entry** 0: Disable. L1 entry does not wait for C2P NP completion 1: Enable. L1 entry waits for C2P NP completion
1:0	RW	00b	**Downstream Arbitration Parking** 00: GNT parks on the last request source. 01: GNT parks on VC1 completion. If VC1 is not enabled (or no VC1), park on VC0 completion. 10: GNT parks on VC0 completion. 11: GNT parks on C2P request.

Offset Address: A3h (D2F0)

Downstream Control 4 **Default Value: 78h**

Bit	Attribute	Default	Description
7:4	RW	0111b	**Retry Buffer Level:** 0000: 1-level 0001: 2-level 0010: 3-level 0011: 4-level 0100: 5-level 0101: 6-level 0110: 7-level 0111: 8-level Others: Reserved
3	RW	1b	**Downstream Read Retry Time Out Control in DL_Down State** 1: Enable downstream read retry time out. The timer is the same as completion time out timer. After time out, this read request will not be retried again even DL_DLUp assertion occurred. 0: Disable downstream read retry time out. If RxA3[0] is set to 1, downstream read request will always wait for DL_DLUp assertion then retry.
2	RW	0	**Downstream Cycle Control/Latency Improvement** 0: Disable 1: Enable
1	RW	0	**CPL Timer Control** 0: Enable. Refer to D2F0 RxA1[2:0]. 1: Disable
0	RW	0	**Downstream Read Cycle Retry** 0: When DL_DOWN is asserted, transaction layer returns “FF” to Central Traffic Controller for C2P read cycle. 1: When DL_DOWN is asserted, transaction layer holds C2P read cycle. This incomplete C2P read cycle will be retried when DL_UP is asserted.

Offset Address: A4h (D2F0)

Upstream Control **Default Value: 1Dh**

Bit	Attribute	Default	Description
7	RW	0	**Force Upstream Address A35~A31 to 0** 0: Disable 1: Enable for system testing or loop back mode test. The upcoming data may be checked in the system memory.
6	RO	0	**Reserved**
5	RW	0	**Upstream Check Malformed TLP through "Byte Enable Rule" and "Over 4K Boundary Rule"** 0: Disable 1: Enable
4	RW	1b	**Downstream Read Waits till the Upstream Write Data Flushed** 0: Disable 1: Enable
3	RW	1b	**CPLH, CPLD, and NPD Become Infinite Mode** 0: Disable 1: Enable
2	RW	1b	**Update Header Credit Whenever Received TLPH (including PH, NPH and CPLH** 0: Disable 1: Enable
1	RW	0	**VC1 Request Queue Usage** (when VC1 is disabled in the capability header; i.e. Rx144[0] = 0) 0: Disable 1: Enable. It allows Transaction Layer maps non-snoop upstream request through VC1 Request Queue to the Central Traffic Controller (Note: When this bit is 1, bit-0 must be 0).
0	RW	1b	**Disable Virtual Channel 1 Support** 0: Enable VC1. Data FIFO of VC1 is used by VC1. 1: Disable VC1. Data FIFO of VC1 is reallocated to VC0, which doubles the size of VC0 data FIFO.

Offset Address: A5h (D2F0)

Credit Advertisement Control 1 **Default Value: FFh**

Bit	Attribute	Default	Description
7:4	RW	1111b	**Upstream Posted (write) Data FIFO Size, and the Initial PD Credit Value** 0000: 1-line upstream write FIFO size, and initial PD credit = 4h 0001: 2-line upstream write FIFO size, and initial PD credit = 8h 0010: 3-line upstream write FIFO size, and initial PD credit = Ch 0011: 4-line upstream write FIFO size, and initial PD credit = 10h 0100: 5-line upstream write FIFO size, and initial PD credit = 14h 0101: 6-line upstream write FIFO size, and initial PD credit = 18h 0110: 7-line upstream write FIFO size, and initial PD credit = 1Ch 0111: 8-line upstream write FIFO size, and initial PD credit = 20h 1xxx: 8-line upstream write FIFO size, and initial PD credit = 20h
3:0	RW	1111b	**Upstream PH Header Queues Size, and the Initial PH Credit** 0000: 1-level PH header queue, and initial PH credit = 2h 0001: 2-level PH header queue, and initial PH credit = 4h 0010: 4-level PH header queue, and initial PH credit = 6h 0011: 8-level PH header queue, and initial PH credit = 8h 01xx: 8-level PH header queue, and initial PH credit = 8h 1xxx: 8-level PH header queue, and initial PH credit = 8h

Offset Address: A6h (D2F0)

Credit Advertisement Control 2 **Default Value: 7Fh**

Bit	Attribute	Default	Description
7	RW	0	**Upstream Non-Posted Header Credit Infinite Mode Control** 0: The non-posted header credit is finite and has to update NPH credits. 1: The non-posted header credit is infinite and not necessary to update NPH credits.
6:4	RW	111b	**Upstream Read CPL Header Size** 0xx: 32QW 4-level 1xx: 32QW 4-level
3:0	RW	1111b	**Upstream Non-Posted Request Queue Size, and Initial NPH Credit Value** 0000: 1-level NPH header queue, and initial NPH credit = 2h 0001: 2-level NPH header queue, and initial NPH credit = 4h 0010: 4-level NPH header queue, and initial NPH credit = 6h 0011: 8-level NPH header queue, and initial NPH credit = 8h 01xx: 8-level NPH header queue, and initial NPH credit = 8h 1xxx: 8-level NPH header queue, and initial NPH credit = 8h

Offset Address: A8-A7h (D2F0)

Upstream Performance Control **Default Value: 01C4h**

Bit	Attribute	Default	Description
15	RW	0	**C2P Completion Timeout Method when PHY Retrains or Re-configures** 0: Keep the timeout value 1: Reset the timeout value
14	RO	0	**Reserved**
13:12	RW	00b	**Configuration Request Timeout Timer** 00: 100 ms 01: 500 ms 10: 1000 ms 11: 1500 ms
11:10	RO	0	**Reserved**
9:8	RW	01b	**Downstream Configuration Retry Request Timing after Receiving CRS Completion** 00: Assert 1T after CRS is received 01: Assert 4T after CRS is received 10: Assert 8T after CRS is received 11: Assert 16T after CRS is received
7:6	RW	11b	**Control the Maximum Number of Outstanding Expected WPOP Issued** 00: TRANS accepts 48 outstanding expected WPOP 01: TRANS accepts 56 outstanding expected WPOP 10: TRANS accepts 64 outstanding expected WPOP 11: No constraint on consecutive WPOP
5	RW	0	**Enable Transaction Layer Header Queue Pre-load Design Dynamic Clock for Power Management** 1: Enable 0: Disable
4	RW	0	**Upstream Read FIFO Entry Release Timing Control** 0: Upstream read FIFO entry release when the last data pops into retry data FIFO. 1: Upstream read FIFO entry release when the first data pops into retry data FIFO
3	RW	0	**Downstream Read Data Waits for Previous Upstream Write Complete** 0: Disable 1: Enable
2	RW	1b	**Upstream Requests Read and Write Orders** 0: Upstream requests are served in order. 1: Upstream write always passes upstream read.
1	RW	0	**Upstream Read Data TLP Return Policy** 0: One upstream request with over 16DW length or non-8-QW boundary alignment must be split into multiple CPL TLPs. 1: Multiple CPL TLPs belong to the same upstream request can be merged into one single CPL TLP.
0	RO	0	**Upstream Write Cycle will be 4QW Align** 0: Disable 1: Enable

Offset Address: A9h (D2F0)
CRS Retry Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Enable CRS Retry Mechanism** 0: No retry cycle for CRS regardless of Rx5C[4] setting and return 'hffffffff for read cycles. 1: Follow Rx5C[4] setting.

Offset Address: AAh (D2F0)
Upstream Read Timing Option **Default Value: 10h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	1b	**UpdateFC-P Generation to The Endpoint for Upstream Write TLPs** 0: UpdateFC-P is generated only when PD update is requested 1: UpdateFC-P is generated when PH or PD update is requested
3:1	RO	0	**Reserved**
0	RW	0	**Upstream Read Timing Option** 0: Fast timing, better read performance 1: Moderate timing, medium read performance

Offset Address: AB-AFh (D2F0) – Reserved

PCI Express Data Link Layer Registers (B0-BFh)

Offset Address: B0h-B1h (D2F0) – Reserved

Offset Address: B2h (D2F0)
Flow Control Initialization (FCI) / Flow Control Unit (FCU) and Status **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW1C	0	**FCI/FCU Timeout Status** 0: No time out 1 The FCI / FCU timeout has occurred.
6	RW	1b	**FCI/FCU Receive Timer Enable Control** 0: Disable the timeout mechanism. 1: Enable the timeout mechanism.
5	RW	0	**FCI/FCU Receive Timer Limit** 0: Timeout limit of 200 us 1: Timeout limit of 300 us
4	RW	0	**FCI/FCU Receive Timer Reset Control** 0: Timer reset by FCI / FCU only. 1: Timer reset by any received DLLPs.
3:0	RO	0	**Reserved**

Offset Address: B3h (D2F0)
Replay Timer Control **Default Value: 81h**

Bit	Attribute	Default	Description
7:6	RW	10b	**Replay Timer Control While Rewinding** (resend those DLLPs which do not have corresponded ACK / NAK received) 00: Hold Replay Timer during rewinding. 01: During rewinding, if ACK / NAK comes in, reset and hold the Replay Timer. 10: During rewinding, reset and hold the Replay Timer as long as the Retry Buffer is empty. 11: Reserved.
5:3	RO	0	**Reserved**
2:0	RW	001b	**Count of Replay Timer Expired During RXL0s (Receiving Physical in L0s State) Before Resend the TLP** **When Rx50[7] is set to 0:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 1 x Replay timer expired 010: Resend the TLP after 2 x Replay timer expired 011: Resend the TLP after 4 x Replay timer expired 100: Resend the TLP after 8 x Replay timer expired 101: Resend the TLP after 16 x Replay timer expired 110: Resend the TLP after 32 x Replay timer expired 111: Resend the TLP after 64 x Replay timer expired **When RX50[7] is set to 1:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 16 x Replay timer expired 010: Resend the TLP after 32 x Replay timer expired 011: Resend the TLP after 64 x Replay timer expired 100: Resend the TLP after 128 x Replay timer expired 101: Resend the TLP after 256 x Replay timer expired 110: Resend the TLP after 512 x Replay timer expired 111: Resend the TLP after 1024 x Replay timer expired

Offset Address: B4h (D2F0)
Arbitration Control **Default Value: 05h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**TLP Flow Control Initialization for VC0 in Arbitration** 0: TLP is not allowed to pass Flow Control Initialization 2 (FCI2) for VC0. 1: TLP is allowed to pass Flow Control Initialization 2 (FCI2) for VC0
2:0	RW	101b	**Data Link TX Packets Arbitration Scheme** 000: Round Robin 001: Reserved 010: Strict priority: TLP > ACK/NAK > FCU 011: Strict priority: TLP > FCU > ACK/NAK 100: Strict priority: ACK/NAK > TLP > FCU 101: Strict priority: ACK/NAK > FCU > TLP 110: Strict priority: FCU > TLP > ACK/NAK 111: Strict priority: FCU > ACK/NAK > TLP

Offset Address: B5h (D2F0)

FCU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**FCU Timer Control** 0: Update flow control credit when either Transaction Layer requested packets being sent or when FCU timer expired. 1: Update flow control credit only when FCU timer expired.
5:4	RW	00b	**ACK DLLP Collapse Method** 00: Send ACK when the latency timer expired 01: Send ACK every 4 correct TLPs have been received 10: Send ACK every 8 correct TLPs have been received 11: Send ACK every 16 correct TLPs have been received
3:2	RO	0	**Reserved**
1	RW	0	**FCI Process End Condition** 0: Complete FCI process when TLP/FCU has been received. 1: Do not complete FCI process even when TLP/FCU has been received.
0	RW	0	**VC1 FCI DLLP Transmission Scheme** 0: Transmit FCI DLLP (Data Link Layer Packet) only when FCI timer expired. 1: Transmit FCI DLLP continuously as long as the FCI process is not finished.

Offset Address: B6h (D2F0)

Transaction / Link Layer Checking Control **Default Value: A1h**

Bit	Attribute	Default	Description
7	RW	1b	**Nak_Scheduled Flag Control** Nak_Scheduled Flag is set after a Nak is scheduled by receiving a TLP with CRC or Seq_Num ERROR, and Nak_Scheduled Flag is cleared after receiving a new Ack. 0: Disable Nak_Scheduled Flag. Schedule Nak regardless of Nak_Scheduled Flag. 1: Enable Nak_Scheduled Flag. Nak can only be scheduled when Nak_Scheduled Flag is cleared.
6:5	RW	01b	**TLP Receiving Timer** When timeout, reset error-framing byte-counter. 00: Reset byte-counter when 1us after TLP header received. 01: Reset byte-counter when 2us after TLP header received. 10: Reset byte-counter when 3us after TLP header received. 11: Reset byte-counter when 4us after TLP header received.
4	RW	0	**The First Downstream TLP is Popped out from TL 1T Earlier**
3	RW	0	**Enable the Receive Buffer Controller Reset Scheme when PM_Request_Ack DLLP Sequences Are Generated** 0: Enable. When PM_Request_Ack sequences are generated, the Receive Buffer Controller will reset. 1: Disable. When PM_Request_Ack sequences are generated, the Receive Buffer Controller will not reset.
3:1	RO	0	**Reserved**
0	RW	1b	**LCRC Check Control** 0: Do not check LCRC. 1: Check LCRC.

Offset Address: B7h (D2F0) – Reserved

Offset Address: B8h (D2F0)
Data Link Layer Header Position **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Data Link Layer Header Position** 0: SDP (Start DLLP) can be in Lane 0 / 4 / 8 / 12. 1: SDP (Start DLLP) always at Lane 0.

Offset Address: B9h (D2F0) – Reserved

Offset Address: BAh (D2F0)
ACK / NAK Latency Timer Limit 1 **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:0	RW	0Ch	**Ack / Nak Latency Timer in Large LSNLW Setting** This timer is used for AckNak_latency_timer when LSNLW (Link Status Register-Negotiation Link Width) is X16. 00h: 4 x 1 Clocks (250Mhz) 01h: 4 x 2 Clocks 02h: 4 x 3 Clocks. ….. FFh: 4 x 256 Clocks

Offset Address: BBh (D2F0)
ACK / NAK Latency Timer Limit 2 **Default Value: 12h**

Bit	Attribute	Default	Description
7:0	RW	12h	**ACK / NAK Latency Timer in Medium LSNLW Setting** This timer is used for AckNak_latency_timer when LSNLW is x8 / x4. 00h: 4 x 1 Clocks (Clock = 250Mhz) 01h: 4 x 2 Clocks 02h: 4 x 3 Clocks. ….. FFh: 4 x 256 Clocks.

Offset Address: BCh (D2F0)
ACK / NAK Latency Timer Limit 3 **Default Value: 3Bh**

Bit	Attribute	Default	Description
7:0	RW	3Bh	**ACK / NAK Latency Timer in Small LSNLW Setting** This timer is used for AckNak_latency_timer when LSNLW is x2 / x1. 00h: 4 x 1 Clocks (Clock =250Mhz) 01h: 4 x 2 Clocks 02h: 4 x 3 Clocks ….. FFh: 4 x 256 Clocks

Offset Address: BDh (D2F0)
Replay Timer Limit 1 **Default Value: 12h**

Bit	Attribute	Default	Description
7:0	RW	12h	**Replay_timer_limit in Large LSNLW Setting** This timer is used for Replay_timer when LSNLW is x16. 00h: 8 x 1 Clocks (Clock = 250Mhz) 01h: 8 x 2 Clocks 02h: 8 x 3 Clocks ……. FFh: 8 x 256 Clocks

Offset Address: BEh (D2F0)
Replay Timer Limit 2 **Default Value: 1Bh**

Bit	Attribute	Default	Description
7:0	RW	1Bh	**Replay_timer_limit in Medium LSNLW Setting** This timer is used for Replay_timer when LSNLW is x8/x4. 00h: 8 x 1 Clocks (250Mhz) 01h: 8 x 2 Clocks 02h: 8 x 3 Clocks ……. FFh: 8 x 256 Clocks

Offset Address: BFh (D2F0)
Replay Timer Limit 3 **Default Value: 58h**

Bit	Attribute	Default	Description
7:0	RW	58h	**Replay_timer_limit in Small LSNLW Setting** This timer is used for Replay_timer when LSNLW is x2 / x1 00h: 8 x 1 Clocks (Clock =250Mhz) 01h: 8 x 2 Clocks 02h: 8 x 3 Clocks …… FFh: 8 x 256 Clocks

PCI Express Physical Layer Registers (C0-CFh)

Offset Address: C0h (D2F0)

PHY General Control **Default Value: 03h**

Bit	Attribute	Default	Description
7	RW	0	**Quick Timeout Counter Setting** When set to 1, PHY timeout period will be shorter as below: 2 ms → 4 us 12 ms → 24 us 24 ms → 48 us 48 ms → 96 us 1024 ts → 32 ts Receiver Detection: 15x1024 ns → 1x1024 ns
6	RW	0	**Disable Data Scrambling / Descrambling** 0: Enable 1: Disable
5:3	RW	000b	**Loopback Mode Selection** 000: No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: External loopback from TX end to RX end 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved See the figure below for details.
2:0	RW	011b	**COMMA Detection Window** 000 / 001: Illegal values. Others: Delay number of T to determine correct lane-to-lane deskew value.

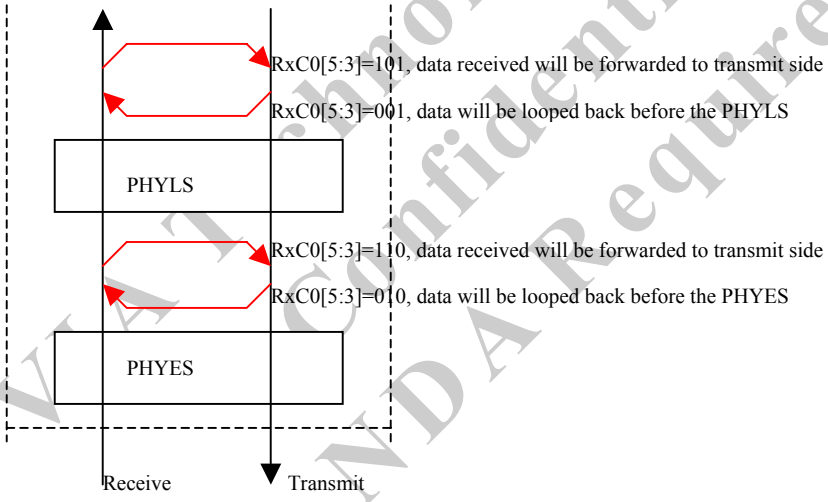


Figure 2. Loop Back Mode Selections

Offset Address: C1h (D2F0)
PHYLS General Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Enable Aggressive Power Management When No Device Plug** 0: Disable 1: Enable
5	RW	0	**Enable Aggressive Power Management in Rx Path to Data Link Layer Module** 0: Disable 1: Enable
4:0	RW	00000b	**PHY Lane Configuration Setting** 00000: Use PHY negotiation 00001: x1 with normal connection 10101: Force into L0s state (for testing and measurement used only) 11000: Force into DETECT_QUIET state (for testing / measurement used only) 11001: Force into DETECT_ACTIVE state (for testing / measurement used only) Other values are not allowed.

Offset Address: C2h (D2F0)
PHYLS MAC and PCS **Default Value: 27h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Reset Elastic Buffer** Always reads 0.
5	RW	1b	**Lane Enable** 0: Enable lanes based on LTSSM negotiation results 1: Enable lanes based on receiver detection's results
4	RW	0	**Bypass PHYES Device Detection in Detect Phase of LTSSM** 0: Enable PHYES to actually perform receiver detection in Detect phase. 1: Bypass receiver detection, and assume device exists. Usually, only set to "1" for testing or debugging.
3	RO	0	**Reserved**
2	RW	1b	**Wait IDL Ordered Set or Electrical Idle When L1 / L23 Entry** 0: Always wait IDL ordered set for L1 / L23 entry. 1: Wait Electrical Idle and ignore IDL ordered set for L1 / L23 entry.
1	RW	1b	**Disparity Check Enable** 0: Disable 1: Enable
0	RW	1b	**State Machine LTSSM (Link Training and Status State Machine) Control** 0: Wait for the electrical idle signal from the PHYES or wait 12 ms after LTSSM enters Detect.Quiet state. 1: Always wait for 12ms after LTSSM enters Detect.Quiet state.

Offset Address: C3h (D2F0)

PHYLS LTSSM State **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**PHYLS LTSSM State** See the table below.

Table 16. Mapping Table for D2F0 RxC3

LTSSM States	Binary Coding	Hexadecimal Coding
DETECT_QUIET	8'B0000_0000	8'H00
DETECT_ACTIVE	8'B0000_0001	8'H01
POLLING_ACTIVE	8'B0001_0000	8'H10
POLLING_CONFIGURATION	8'B0001_0001	8'H11
POLLING_SPEED	8'B0001_0010	8'H12
POLLING_COMPLIANCE	8'B0001_0100	8'H14
CONFIGURATION_RCVRCFG_STEP_1	8'B0010_0001	8'H21
CONFIGURATION_RCVRCFG_STEP_2	8'B0010_0010	8'H22
CONFIGURATION_RCVRCFG_STEP_3	8'B0010_0011	8'H23
CONFIGURATION_RCVRCFG_STEP_4	8'B0010_0100	8'H24
CONFIGURATION_RCVRCFG_STEP_5	8'B0010_0101	8'H25
CONFIGURATION_RCVRCFG_STEP_6	8'B0010_0110	8'H26
CONFIGURATION_RCVRCFG_STEP_7	8'B0010_0111	8'H27
CONFIGURATION_IDLE	8'B0010_1000	8'H28
RECOVERY_RCVRLOCK	8'B0011_0000	8'H30
RECOVERY_RCVRCFG	8'B0011_0001	8'H31
RECOVERY_IDLE	8'B0011_0011	8'H33
LOOPBACK_MSTR_ENTRY	8'B0100_0000	8'H40
LOOPBACK_MSTR_ACTIVE	8'B0100_0001	8'H41
LOOPBACK_MSTR_EXIT	8'B0100_0011	8'H43
LOOPBACK_SLAV_ENTRY	8'B0100_0100	8'H44
LOOPBACK_SLAV_ACTIVE	8'B0100_0101	8'H45
LOOPBACK_SLAV_EXIT	8'B0100_0111	8'H47
DISABLED_ENTRY	8'B0101_0000	8'H50
DISABLED_DISABLED	8'B0101_0001	8'H51
HOTRESET_ACTIVE	8'B0110_0000	8'H60
L0L0_TXL0_RXL0	8'B1000_1010	8'H8A
L0L0S_TXL0_RXENTRY	8'B1001_1000	8'H98
L0L0S_TXL0_RXIDLE	8'B1001_1001	8'H99
L0L0S_TXL0_RXFTS	8'B1001_1011	8'H9B
L0SL0_TXENTRY_RXL0	8'B1010_0010	8'HA2
L0SL0_TXIDLE_RXL0	8'B1010_0110	8'HA6
L0SL0_TXFTS_RXL0	8'B1010_1110	8'HAE
L0SL0S_TXENTRY_RXENTRY	8'B1011_0000	8'HB0
L0SL0S_TXENTRY_RXIDLE	8'B1011_0001	8'HB1
L0SL0S_TXENTRY_RXFTS	8'B1011_0011	8'HB3
L0SL0S_TXIDLE_RXENTRY	8'B1011_0100	8'HB4
L0SL0S_TXIDLE_RXIDLE	8'B1011_0101	8'HB5
L0SL0S_TXIDLE_RXFTS	8'B1011_0111	8'HB7
L0SL0S_TXFTS_RXENTRY	8'B1011_1100	8'HBC
L0SL0S_TXFTS_RXIDLE	8'B1011_1101	8'HBD
L0SL0S_TXFTS_RXFTS	8'B1011_1111	8'HBF
L1_ENTRY	8'B1100_0000	8'HC0
L1_IDLE	8'B1100_0001	8'HC1
L23READY_ENTRY	8'B1101_0000	8'HD0
L23READY_IDLE	8'B1101_0001	8'HD1

Offset Address: C4h (D2F0)
Elastic Buffer Base Registers for Lane 0 to 1 **Default Value: 04h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	4h	**Elastic Buffer Base Register for Lane 0** 0, 1, 7: Illegal values. Others: Delay numbers of T for elastic buffer operations.

Offset Address: C5-CCh (D2F0) – Reserved

Offset Address: CDh (D2F0)
PHYLS MAC **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Downstream Tx Arbitration between DLLM and PHYLS** 0: Normal arbitration 1: Arbitration with lower latency

Offset Address: CEh (D2F0) – Reserved

Offset Address: CFh (D2F0)
SKP Ordered Set Control **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Enable PHYES Level-2 Power Down** 0: Disable 1: Enable
3:2	RO	11b	**Reserved** (Do not program)
1:0	RW	00b	**SKP Order-set Scheduling Time** 00: Send out "SKP" Order-set on the PCIe bus every 1180 symbol time, it is around 4.72us. 01: Send out "SKP" Order-set on the PCIe bus every 118 symbol time, it is around 472ns. 10: Send out "SKP" Order-set on the PCIe bus every 6.12 us. 11: Reserved

PCI Express Power Management Module Registers (D0-D3h)

Offset Address: D0h (D2F0)

Power Management Controller PHYLS Control **Default Value: 50h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	101b	**Timeout Period** This timer is used when waiting for ACK from a device after issued PME_TURNOFF message to notify the device to move to power down mode. 000: 1 us 001: 2 us 010: 4 us 011: 8 us 100: 16 us 101: 32 us 110: 64 us 111: 128 us
3	RO	0	**Reserved**
2	RW	0	**Retrain Link when Bad DLLP is Checked** 0: Disable 1: Enable
1	RW	0	**Link Loopback** 0: Normal operation 1: Direct device to enter Loopback mode. Received data in the device will be sent to the transmit side.
0	RW	0	**Link Reconfigure Linkwidth** 0: When reconfigure linkwidth, LTSSM must be Detect state. 1: When reconfigure linkwidth, LTSSM can go to Configuration state.

Offset Address: D1h (D2F0)

PMU (Power Management Unit) Timeout **Default Value: 20h**

Bit	Attribute	Default	Description
7	RW1C	0	**Error Status Report** This bit is set when device cannot have electrical idle after the waiting period programmed at RxD1[5:4] expired.
6	RO	0	**Reserved**
5:4	RW	10b	**Electrical Idle Waiting Period before Move to L1 State** (after issue ACK to the L1 request from the device) 00: Always wait for electrical idle 01: Wait 32 clock 10: Wait 64 clock 11: Reserved
3:2	RO	0	**Reserved**
1:0	RW	00b	**Downstream Cycles Triggered C2P Cycles** Period of staying at L0 before returned to L1 for PHY (when PMU is not in D0 state). 00: Immediately 01: 1 cfgW or message + delay 10T 10: 1 32QW + 1 cfgW or message + delay 10T 11: 2 32QW + 1 cfgW or message + delay 10T

Offset Address: D2h (D2F0)

PMU L0s Idle Timeout **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Idle Period to Enter L0s** Minimum time period is 128ns (RxD2 = 00). 00h: 128 ns 01h: 2x128 ns 02h: 3x128 ns … FFh: 256x128 ns

Offset Address: D3h (D2F0)
PMU L1 Idle Timeout **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Idle Period to Enter ASL1** Minimum time period is 128 ns. 00h: 128 ns 01h: 2x128 ns 02h: 3x128 ns … FFh: 256x128 ns

Offset Address: D4-D7h (D2F0) – Reserved

PCI Express Message Controller Related Registers (D8-DFh)

Offset Address: D8h (D2F0)
Power Management Controller Express Message Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Excessive Errors Occurred But Not Reported in MSGC** 0: Normal operation. 1: There are errors not reported to the system.
6:0	RO	0	**Reserved**

Offset Address: D9-DFh (D2F0) – Reserved

PCI Express Electrical PHY Registers (E0-EFh)

Offset Address: E0h (D2F0)
PHYES Module Overall Control **Default Value: 0Eh**

Bit	Attribute	Default	Description
7	RW	0	**Enable New PLL_LOCK Scheme to Monitor Any Abnormal Jitter** 0: Disable 1: Enable
6:4	RO	0	**Reserved**
3:1	RW	111b	**Charge Pump Current Control** Reserved
0	RW	0	**Charge Pump Style Control** Reserved

Offset Address: E1h (D2F0)
4-Lane PHYES Module And Squelch Window Control **Default Value: 08h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Receiving Polarity Change Control** 0: Have the same polarity on the loop-back / received data. 1: Have reverse polarity on the loop-back / received data.
3:2	RW	10b	**Squelch Window Select (64~175 mv) – For all 6 lanes**
1	RW	0	**Number of Non Idle Signal Detected Before Exit Idle State** (Electrical Idle State Exit Condition) 0: 10 bits 1: 2 bits
0	RW	0	**Number of Idle Signal Detected Before Enter Idle State** (Electrical Idle State Enter Condition) 0: 10 bits 1: 2 bits

Offset Address: E2h (D2F0)

6 Lanes PHYES Module Control – Rx/Tx 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Mobile Swing** 0: Disable 1: Enable
5	RW	0	**PHYES Clock Buffer Power Down on Lane 0-5** 0: All enable 1: Power down
4	RW	0	**Lane Clock Buffer Power Down** 0: All enable 1: Lane power down
3:2	RW	00b	**Receiver Input Rise Delay** (duty cycle adjustment for the first 6 lanes) 00: 0 ps 01: 4 ps 10: 15 ps 11: 50 ps
1:0	RW	00b	**Receiver Input Fall Delay** (duty cycle adjustment for the first 6 lanes) 00: 0 ps 01: 7 ps 10: 24 ps 11: 55 ps

Offset Address: E3h (D2F0)

6 Lanes PHYES Module Control – Rx/Tx 2 **Default Value: 9Dh**

Bit	Attribute	Default	Description
7	RW	1b	**PCIe Pads Driving Control** 0: Autocomp 1: Manual setting through bits RxE3[2:0]
6:5	RW	00b	**Filter Depth Valid Only When CDR Type (Bit 4) is Set to 0** 00: Filter depth = 2 01: Filter depth = 3 10: Filter depth = 5 11: Filter depth = 7
4	RW	1b	**CDR Type** 0: 1/N type 1: Pseudo 6X scheme
3	RW	1b	**CDR Filter Depth**, **Valid only when Bit 4 is Set 1** 0: Filter depth = 6 1: Filter depth = 8
2:0	RW	101b	**6 Lanes, Lane 0 –5, Termination Resistance Selection** Resistance Range: 62Ω (000b) - 43Ω (111b) Default: 50Ω

Offset Address: E4h (D2F0)

6 Lanes PHYES Module Control – Rx/Tx 3 **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:4	RW	0	**Pre/De-Emphasis Level Selection** Reserved
3:0	RW	Ch	**Driver Current Source Selection** Reserved

Offset Address: E5-EFh (D2F0) – Reserved

PCI Express Electrical PHY Test Registers (F0-FFh)

Offset Address: F0h (D2F0) – Reserved

Offset Address: F1h (D2F0)

Repeated Count of the Test Pattern **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Repeated Count of the Test Pattern** (as selected in RxF2[7:4]) When using loopback mode to test electrical PHY, the following should be satisfied: RxF1 x 8 > loopback latency / 4 ns 00-0Bh: Illegal value 0Ch: Test pattern repeats 12 times 0Dh: Test pattern repeats 13 times … FFh: Test pattern repeats 255 times

Offset Address: F2h (D2F0)

Test Pattern Selection **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Select Test Pattern** 0000: SKP order-set 0001: User define, use RxF6[9:0] 0010: K28.5 test bit sequence 0011: K28.7 test bit sequence 0100: K test for differential pair current 0101: J test for differential pair current 0110: D21.5 test bit sequence 0111: D30.3 test bit sequence 1000: Ten contiguous run of 3 test bit sequence 1001: Low transition density test bit sequence 1010: Half-rate/quarter-rate test bit sequence 1011: Low frequency spectral test bit sequence 1100: Simultaneous switching test bit sequence 1101: D 10.2 test bit sequence 1110: D 24.3 test bit sequence 1111: Compliance test bit sequence
3:0	RO	0	**Reserved**

Offset Address: F3h (D2F0)

Test Mode Control **Default Value: 06h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Electrical PHY Test Mode** Program this bit to 1 to start Electrical PHY test. 0: Disable 1: Enable
6:4	RO	0	**Reserved**
3:0	RW	6h	**Test Pattern Check Length** Number of T when the receiving side starts to check transmitted and received patterns. Suggested Value Settings: (Lane 0 for example) RxC0[5:3] = 001b: RxC4[2:0] + 2 RxC0[5:3] = 010b: RxC4[2:0] + 2 + (Loopback Path Latency / 4 ns)+1

Offset Address: F5-F4h (D2F0)

BIST Status 1 **Default Value: 0000h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9:0	RO	00h	**Received Symbol** (When RxF3[7] is set to 1) 00: When RxF3[7] is 0.

Offset Address: F7-F6h (D2F0)

BIST Status 2 **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Electrical PHY Test Error** 0: No error detected 1: Indicates that there is an error detected in the receiving side during the loop back test mode.
14	RO	0	**Electrical PHY Built-In Self Test Error of Symbol Comparison** 0: No error detected 1: Indicates that some errors detected or COMMA symbols are never detected during PHYBIST period; reported from PTNCMP.
13:10	RO	0	**Reserved**
9:0	RW	0	**Transmitted Symbol** (When RxF3[7] is set to 1) 10b'0: When RxF3[7] is set to 0.

Offset Address: F9-F8h (D2F0)

PHY BIST Counter Test Mode **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0000h	**PHY BIST Period for Electrical PHY Test Error**

Offset Address: FA-FFh (D2F0) – Reserved

Device 2 Function 0 (D2F0) – PCI Express Root Port G0 Extended Space

Registers defined in the Extended Space can be accessed through PCI Express Enhanced Configuration Access Mechanism, which utilizes a flat memory-mapped address space to access the configuration registers. Please check PCI Express Specification for the detailed information.

Advanced Error Reporting Capability (100-13Fh)

Offset Address: 103-100h (D2F0)

Advance Error Reporting Enhanced Capability Header **Default Value: 1401 0001h**

Bit	Attribute	Default	Description
31:20	RO	140h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0001h	**PCI Express Extended Capability ID**

Offset Address: 107-104h (D2F0)

Uncorrectable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20	RW1CS	0	**Unsupported Request Error Status (TL)**
19	RW1CS	0	**ECRC Error Status (TL)**
18	RW1CS	0	**Malformed TLP Status (TL)**
17	RW1CS	0	**Receiver Overflow Status (TL)**
16	RW1CS	0	**Unexpected Completion Status (TL)**
15	RW1CS	0	**Completer Abort Status (TL)**
14	RW1CS	0	**Completion Timeout Status (TL)**
13	RO	0	**Flow Control Protocol Error Status (TL)**
12	RW1CS	0	**Poisoned TLP Status (TL)**
11:6	RO	0	**Reserved**
5	RW1CS	0	**Surprise Down Error Status**
4	RW1CS	0	**Data Link Protocol Error Status (DLL)**
3:1	RO	0	**Reserved**
0	RW1CS	0	**Training Error Status (PHY)**

Offset Address: 10B-108h (D2F0)

Uncorrectable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20	RWS	0	**Unsupported Request Error Mask (TL)**
19	RWS	0	**ECRC Error Mask (TL)**
18	RWS	0	**Malformed TLP Mask (TL)**
17	RWS	0	**Receiver Overflow Mask (TL)**
16	RWS	0	**Unexpected Completion Mask (TL)**
15	RWS	0	**Completed Abort Mask (TL)**
14	RWS	0	**Completion Timeout Mask (TL)**
13	RWS	0	**Flow Control Protocol Error Mask (TL)**
12	RWS	0	**Poisoned TLP Mask (TL)**
11:6	RO	0	**Reserved**
5	RWS	0	**Surprise Down Error Mask**
4	RWS	0	**Data Link Protocol Error Mask (DLL)**
3:1	RO	0	**Reserved**
0	RWS	0	**Training Error Mask (PHY)**

Offset Address: 10F-10Ch (D2F0)

Uncorrectable Error Severity **Default Value: 0006 2031h**

Bit	Attribute	Default	Description
31:21	RO	0	Reserved
20	RWS	0	Unsupported Request Error Severity (TL)
19	RWS	0	ECRC Error Severity (TL)
18	RWS	1b	Malformed TLP Severity (TL)
17	RWS	1b	Receiver Overflow Error Severity (TL)
16	RWS	0	Unexpected Completion Error Severity (TL)
15	RWS	0	Completed Abort Error Severity (TL)
14	RWS	0	Completion Timeout Error Severity (TL)
13	RWS	1b	Flow Control Protocol Error Severity (TL)
12	RWS	0	Poisoned TLP Severity (TL)
11:6	RO	0	Reserved
5	RWS	1b	Surprise Down Error Severity
4	RWS	1b	Data Link Protocol Error Severity (DLL)
3:1	RO	0	Reserved
0	RWS	1b	Training Error Severity (PHY)

Offset Address: 113-110h (D2F0)

Correctable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13	RW1CS	0	Advisory Non-Fatal Error Status
12	RW1CS	0	Replay Timer Timeout Status (DLL)
11:9	RO	0	Reserved
8	RW1CS	0	REPLAY_NUM Rollover Status (DLL)
7	RW1CS	0	Bad DLLP Status (DLL)
6	RW1CS	0	Bad TLP Status (DLL)
5:1	RO	0	Reserved
0	RW1CS	0	Receiver Error Status (PHY)

Offset Address: 117-114h (D2F0)

Correctable Error Mask **Default Value: 0000 2000h**

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13	RWS	1b	Advisory Non-Fatal Error Mask
12	RWS	0	Replay Timer Timeout Mask (DLL)
11:9	RO	0	Reserved
8	RWS	0	REPLAY_NUM Rollover Mask (DLL)
7	RWS	0	Bad DLLP Mask (DLL)
6	RWS	0	Bad TLP Mask (DLL)
5:1	RO	0	Reserved
0	RWS	0	Receiver Error Mask (PHY)

Offset Address: 11B-118h (D2F0)

Advanced Error Capabilities and Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:9	RO	0	Reserved
8	RWS	0	ECRC Check Enable (TL)
7	RO	0	ECRC Check Capable (TL)
6	RWS	0	ECRC Generation Enable (TL)
5	RO	0	ECRC Generation Capable (TL)
4:0	ROS	0	First Error Pointer (TL)

Offset Address: 11F-11Ch (D2F0)
Header Log (TL) Register 1st DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 1st DW**

Offset Address: 123-120h (D2F0)
Header Log (TL) Register 2nd DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 2nd DW**

Offset Address: 127-124h (D2F0)
Header Log (TL) Register 3rd DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 3rd DW**

Offset Address: 12B-128h (D2F0)
Header Log (TL) Register 4th DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 4th DW**

Offset Address: 12F-12Ch (D2F0)
Root Error Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	RO	0	**Reserved**
2	RW	0	**Fatal Error Reporting Enable**
1	RW	0	**Non-Fatal Error Reporting Enable**
0	RW	0	**Correctable Error Reporting Enable**

Offset Address: 133-130h (D2F0)
Root Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	0	**Advanced Error Interrupt Message Number (TL)**
26:7	RO	0	**Reserved**
6	RW1CS	0	**Fatal Error Messages Received (TL)**
5	RW1CS	0	**Non-Fatal Error Messages Received (TL)**
4	RW1CS	0	**First Uncorrectable Fatal Error Message Received (TL)** Set to 1 when the first Uncorrectable Error Message received is for a Fatal Error.
3	RW1CS	0	**Multiple ERR_FATAL/NONFATAL Received (TL)**
2	RW1CS	0	**ERR_FATAL / NONFATAL Received (TL)**
1	RW1CS	0	**Multiple ERR_COR Received (TL)**
0	RW1CS	0	**ERR_COR Received (TL)**

Offset Address: 137-134h (D2F0)
Error Source Identification **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	ROS	0	**ERR_FATAL/NONFATAL Source Identification (TL)**
15:0	ROS	0	**ERR_COR Source Identification (TL)**

Offset Address: 138-13Fh (D2F0) – Reserved

Virtual Channel Capability (140-14Fh)

Virtual Channel Capability is defined for Egress direction of the device. For Root Port, since only VC0 is defined.

- VC0 mapping: TC0, TC1, TC2, TC3, TC4, TC5, TC6, TC7
- No VC arbitration table
- No port arbitration table

Offset Address: 143-140h (D2F0)

Virtual Channel Enhanced Capability Header — **Default Value: 1801 0002h**

Bit	Attribute	Default	Description
31:20	RO	180h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0002h	**PCI Express Extended Capability ID**

Offset Address: 147-144h (D2F0)

Port VC Capability 1 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:10	RO	0	**Port Arbitration Table Entry Size** Reserved for root port.
9:8	RO	0	**Reference Clock** Reserved for root port.
7	RO	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count**
3	RO	0	**Reserved**
2:0	RO	0	**Extended VC Count**

Offset Address: 14B-148h (D2F0)

Port VC Capability 2 — **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**VC Arbitration Table Offset** 00: Since only VC0 is defined.
23:8	RO	0	**Reserved**
7:0	RO	0	**VC Arbitration Capability** Reserved

Offset Address: 14D-14Ch (D2F0)

Port VC Control — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3:1	RO	0	**VC Arbitration Select** Reserved
0	RO	0	**Local VC Arbitration Table** Reserved

Offset Address: 14F-14Eh (D2F0)

Port VC Status — **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	0	**VC Arbitration Table Status** Reserved

VC0 Resource (150-15Bh)

Offset Address: 153-150h (D2F0)

VC Resource Capability (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Arbitration Table Offset (VC0)** Reserved for Root Port.
23	RO	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)**
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching** Reserved
13:8	RO	0	**Reserved**
7:0	RO	0	**Port Arbitration Capability** Reserved for Root Port.

Offset Address: 157-154h (D2F0)

VC Resource Control (VC0) **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1b	**VC Enable**
30:27	RO	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	RO	0	**Reserved**
19:17	RO	0	**Port Arbitration Select** Reserved for Root Port.
16	RO	0	**Load Port Arbitration Table** Reserved for Root Port.
15:8	RO	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC / VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit-0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (D2F0)

VC Resource Status (VC0) **Default Value: 0002 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	1b	**VC Negotiation Pending (TL)** This bit indicates whether the Virtual Channel negotiation is in Pending state (set / clear by hardware). 0: Negotiation is complete. 1: Negotiation is on-going.
16	RO	0	**Port Arbitration Table Status** Reserved for Root Port.
15:0	RO	0	**Reserved**

VC1 Resource (15C-19Fh)

Offset Address: 15C-17Fh (D2F0) – Reserved

Offset Address: 183-180h (D2F0)

Root Complex Link Declaration Capabilities Header **Default Value: 0001 0005h**

Bit	Attribute	Default	Description
31:20	RO	0	**Next Capability**
19:16	RO	1h	**Capability Version**
15:0	RO	0005h	**Capability ID** Bit[15:0]=0005 indicates the Extended Capability ID for the Root Complex Link Declaration Capability.

Offset Address: 187-184h (D2F0)

Element Self Description **Default Value: 0101 0100h**

Bit	Attribute	Default	Description
31:24	RO	01h	**Port Number (Root Port Graphic)**
23:16	RO	01h	**Component ID**
15:8	RO	01h	**Number of Link Entries**
7:4	RO	0	**Reserved**
3:0	RO	0	**Element Type** 0h: Configuration Space Element 1h: System egress port or internal sink 2h: Internal Root Complex Link

Offset Address: 188-18Fh (D2F0) – Reserved

Offset Address: 193-190h (D2F0)

Upstream Link Descriptor **Default Value: 0001 0001h**

Bit	Attribute	Default	Description
31:24	RO	0	**Target Port Number** Indicates the port number of RCRB-H.
23:16	RO	01h	**Target Component ID**
15:2	RO	0	**Reserved**
1	RO	0	**Link Type** Indicates the link points to RCRB-H.
0	RO	1b	**Link Valid**

Offset Address: 194-197h (D2F0) – Reserved

Offset Address: 19F-198h (D2F0)

Upstream Link Base Address for RCRB-H[63:12] **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:32	RO	0	**Base Address Upper**
31:0	RO	0	**Base Address Lower**

Device 3 Function 0 (D3F0) – PCI Express Root Port 0 (PCI-to-PCI Virtual Bridge)

Device 3 Function 0, a 1-Lane PCI Express Root Port, is connected to the PCI bus through AD14 as the IDSEL.
All registers are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with Bus Number 0, Device Number 3 and Function Number 0.

Header Registers (00-3Fh)

Offset Address: 01-00h (D3F0)
Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 03-02h (D3F0)
Device ID **Default Value: E353h**

Bit	Attribute	Default	Description
15:0	RO	E353h	**Device ID**

Offset Address: 05-04h (D3F0)
PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable** Set when the device is prevented from generating INTx messages. 0: Disable 1: Enable
9	RO	0	**Reserved**
8	RW	0	**SERR# Enable** 0: Disable error report. 1: Enable reporting of non-fatal and fatal errors.
7	RO	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors and continue. 1: Take normal action on detected parity errors.
5:3	RO	0	**Reserved**
2	RW	0	**Bus Master Enable** 0: Disable 1: Enable Controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. Disabling this bit is to disable MSI messages.
1	RW	0	**Memory Space** 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the SM. 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.
0	RW	0	**I/O Space** 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the SM. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.

Offset Address: 07-06h (D3F0)
PCI Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set whenever a poisoned TLP is received, regardless the state of Parity Error Enabled (Rx4[6]).
14	RW1C	0	**Signaled System Error** This bit is set when: A device sends an ERR_FATAL or ERR_NONFATAL message. Rx04[8] = 1
13	RW1C	0	**Received Master Abort** This bit is set when receiving a completion with Unsupported Request Completion Status.
12	RW1C	0	**Received Target Abort** This bit is set when receiving a completion with Completer Abort Completion Status.
11	RW1C	0	**Signaled Target Abort** This bit is set when completing a Request with Completer Abort Completion Status.
10:9	RO	0	**Reserved** Always reads 0.
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx04[6] is set and either one of the following two conditions occurs: Requestor receives a Completion marked poisoned. Requestor poisons a write Request.
7:5	RO	0	**Reserved**
4	RO	1b	**Capabilities List** Indicates the presence of an extended capability list item. Always set to 1 for PCI Express device.
3	RO	0	**Interrupt Status** Indicates an INTx message is pending internally.
2:0	RO	0	**Reserved**

Offset Address: 08h (D3F0)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision Code**

Offset Address: 0B-09h (D3F0)
Class Code **Default Value: 06 0400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Ch (D3F0)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D3F0)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Master Latency Timer**

Offset Address: 0Eh (D3F0)
Header Type **Default Value: 81h**

Bit	Attribute	Default	Description
7:0	RO	81h	**Header Type**

Offset Address: 0Fh (D3F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support**

Offset Address: 17-10h (D3F0)
Base Address Register **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RO	0	**Base Address**

Offset Address: 18h (D3F0)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Primary Bus Number**

Offset Address: 19h (D3F0)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Secondary Bus Number**

Offset Address: 1Ah (D3F0)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subordinate Bus Number**

Offset Address: 1Bh (D3F0) – Reserved

Offset Address: 1Ch (D3F0)
I/O Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	Fh	**I/O Base (AD[15:12] - Inclusive)** This bridge will forward the cycles from primary side to PCI if the I/O address AD[15:12] is between I/O base and I/O limit (Rx1D[7:4]).
3:0	RO	0	**I/O Addressing Capability** 0 means I/O addressing is 16-bit only.

Offset Address: 1Dh (D3F0)

I/O Limit **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**I/O Limit (AD[15:12] - Inclusive)** This bridge will forward the cycles from primary side to PCI if the I/O address is between I/O base (Rx1C) and I/O limit.
3:0	RO	0	**I/O Addressing Capability** 0 means I/O addressing is 16-bit only.

Offset Address: 1F-1Eh (D3F0)

Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set when secondary side receives a poisoned TLP regardless of Rx04[6].
14	RW1C	0	**Received System Error** This bit is set when Rx04[8] is 1 and a device sends an ERR_FATAL or ERR_NONFATAL message.
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RW1C	0	**Signaled Target Abort**
10:9	RO	0	**Reserved**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx04[6] is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned. 2. Requestor poisons a write Request.
7:0	RO	0	**Reserved**

Offset Address: 21-20h (D3F0)

Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Memory Base (AD[31:20] – Inclusive)** The address bits [19:0] are not decoded.
3:0	RO	0	**Reserved**

Offset Address: 23-22h (D3F0)

Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Memory Limit (AD[31:20] – inclusive)** The address bits [19:0] are not decoded.
3:0	RO	0	**Reserved**

Offset Address: 25-24h (D3F0)

Prefetchable Memory Base **Default Value: FFF1h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Prefetchable Memory Base AD[31:20]**
3:1	RO	0	**Reserved**
0	RO	1b	**Report Support Prefetchable 64 Bits Memory Addressing** 0: Not supported 1: Supported

Offset Address: 27-26h (D3F0)
Prefetchable Memory Limit **Default Value: 0001h**

Bit	Attribute	Default	Description
15:4	RW	0	**Prefetchable Memory Limit AD[31:20]**
3:1	RO	0	**Reserved**
0	RO	1b	**Report Support Prefetchable 64 Bits Memory Addressing** 0: Not supported 1: Supported

Offset Address: 2B-28h (D3F0)
Prefetchable Memory Upper Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:0	RW	0	**AD[35:32]** This chip supports up to 16G.

Offset Address: 2F-2Ch (D3F0)
Prefetchable Memory Upper Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:0	RW	0	**AD[35:32]** This chip supports up to 16G.

Offset Address: 31-30h (D3F0)
Upper I/O Base **Default Value: 0000h**

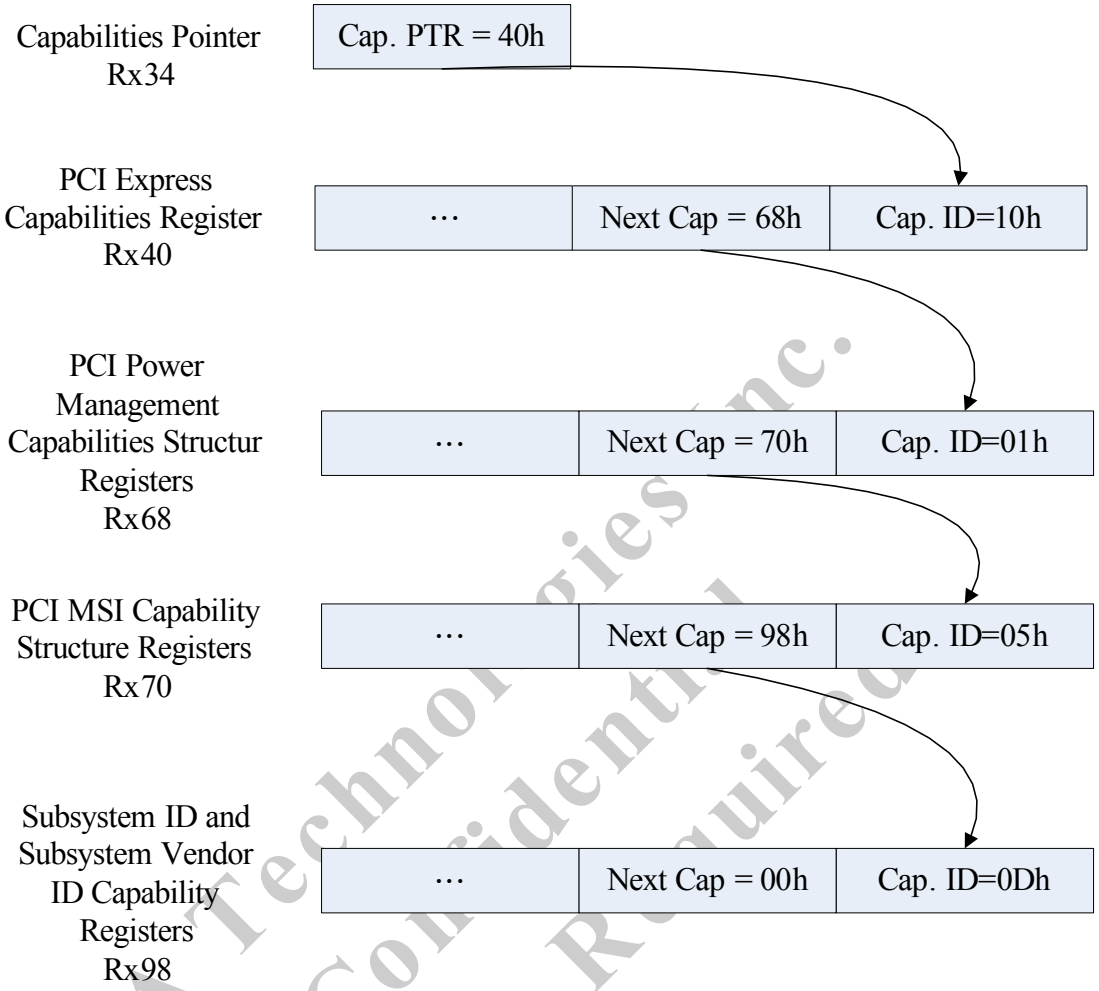
Bit	Attribute	Default	Description
15:0	RO	0	**Upper I/O Base 16 Bits Address for PCI**

Offset Address: 33-32h (D3F0)
Upper I/O Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Upper I/O Limit 16 Bits Address for PCI**

Offset Address: 34h (D3F0)
Capability Pointer **Default Value: 40h**

Bit	Attribute	Default	Description
7:0	RO	40h	**Capability Pointer** This register contains the offset address from the start of the configuration space. Always reads 40h. Capability Pointer link list: Rx34 → Rx40 → Rx68 → Rx70 → Rx98 → NULL



Offset Address: 35-3Bh (D3F0) – Reserved

Offset Address: 3Ch (D3F0)

Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**INT Line** (For Software Use Only)

Offset Address: 3Dh (D3F0)

Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**INT Pin = INTA#**

Offset Address: 3F-3Eh (D3F0)

Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	RO	0	**Reserved**
6	RW	0	**Secondary Bus Reset** 0: No reset. 1: Triggers a warm reset on the corresponding PCI Express Port.
5	RO	0	**Reserved**
4	RW	0	**Base VGA 16 Bits Decode** 0: All VGA alias range will be forwarded. 1: Only forward base VGA range (Alias range will not be forwarded).
3	RW	0	**VGA Compatible I/O and Memory Address Range** 0: Do not forward VGA compatible memory and I/O. 1: Forward VGA compatible memory and I/O. Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If a MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.
2	RW	0	**Block/Forward ISA I/O Cycles** 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit. 1: Do not forward ISA I/O that are in the top 768 bytes of each 1K byte block address range.
1	RW	0	**SERR Enable** Controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary. 0: Disable 1: Enable
0	RW	0	**Parity Error Response Enable** 0: Ignore the response to poisoned TLPs. 1: Enable the response to poisoned TLPs.

PCI Express Capability Registers (40-67h)

Offset Address: 41-40h (D3F0)

PCI Express List **Default Value: 6810h**

Bit	Attribute	Default	Description
15:8	RO	68h	**Next Pointer**
7:0	RO	10h	**Capability ID** 10h indicates a PCI Express Capability Structure.

Offset Address: 43-42h (D3F0)

PCI Express Capabilities **Default Value: 0141h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RO	0	**TCS Routing Support** 0: Not supported 1: Supported
13:9	RO	0	**Interrupt Message Number**
8	RO	1b	**Slot Implemented** This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled).
7:4	RO	0100b	**Device / Port Type** 0100b: Root Port of PCI Express Root Complex
3:0	RO	1h	**Capability Version**

Offset Address: 47-44h (D3F0)

Device Capabilities **Default Value: 0000 8001h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:26	RO	0	**Captured Slot Power Limit Scale** Reserved. For upstream port only.
25:18	RO	0	**Captured Slot Power Limit Value** Reserved. For upstream port only.
17:16	RO	0	**Reserved**
15	RO	1b	**Role-Based Error Reporting** 0: Role-based error reporting is not supported 1: Role-based error reporting is supported
14	RO	0	**Power Indicator Present** Reserved. For upstream port or endpoint only.
13	RO	0	**Attention Indicator Present** Reserved. For upstream port or endpoint only.
12	RO	0	**Attention Button Present** Reserved. For upstream port or endpoint only.
11:9	RO	000b	**Endpoint L1 Acceptable Latency**
8:6	RO	000b	**Endpoint L0s Acceptable Latency**
5	RO	0	**Extended Tag Field Supported** 0: 5-bit Tag field supported. 1: 8-bit Tag field supported.
4:3	RO	0	**Phantom Functions Supported** Reserved
2:0	RO	001b	**Max Payload Size Supported** 001b: 32QW (256 bytes)

Offset Address: 49-48h (D3F0)

Device Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14:12	RO	000b	**Max Read Request Size** 000b: 128 bytes This field sets the maximum Read Request size for the device as a Requestor.
11	RW	0	**Enable No Snoop** 0: Disable 1: Enable If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requestor Attributes of the transactions to indicate that it does not require hardware enforced cache coherence.
10	RWS	0	**Auxiliary Power PM Enable** 0: Disable 1: Enable This bit when set enables device to draw AUX power independent of PME AUX power.
9	RO	0	**Phantom Functions Enable** Not supported.
8	RO/RW	0	**Extended Tag Field Enable** 0: Disable 1: Enable When Rx44[5] is set to 0, this bit is RO. When Rx44[5] is set to 1, this bit is RW.
7:5	RW	0	**Max Payload Size** Maximum TLP payload size.
4	RW	0	**Enable Relaxed Ordering** 0: Disable 1: Enable If this bit is set to 1, the device is permitted to set the Relaxed Ordering bit in the Requestor Attributes of the transactions to indicate that it does not require strong write ordering.
3	RW	0	**Unsupported Request Reporting Enable** 0: Disable 1: Enable
2	RW	0	**Fatal Error Reporting Enable** 0: Disable 1: Enable For a Root Port, the report of Fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	RW	0	**Non-Fatal Error Reporting Enable** 0: Disable 1: Enable For a Root Port, the report of Non-Fatal errors is internal to the root. No external ERR_NONFATAL message is generated.
0	RW	0	**Correctable Error Reporting Enable** 0: Disable 1: Enable For a Root Port, the report of correctable errors is internal to the root. No external ERR_COR message is generated.

Offset Address: 4B-4Ah (D3F0)

Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RO	0	**Transactions Pending** This bit when set indicates that the port has issued Non-Posted Requests on its own behalf (using Requestor ID of the port) which have not been completed.
4	RO	1b	**AUX Power Detected** 0: Not detected 1: Detected
3	RW1C	0	**Unsupported Request Detected** 0: Not detected 1: Detected
2	RW1C	0	**Fatal Error Detected** 0: Not detected 1: Detected
1	RW1C	0	**Non-Fatal Error Detected** 0: Not detected 1: Detected
0	RW1C	0	**Correctable Error Detected** 0: Not detected 1: Detected

Offset Address: 4F-4Ch (D3F0)

Link Capabilities **Default Value: 0218 3C11h**

Bit	Attribute	Default	Description
31:24	RO	02h	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link.
23:21	RO	0	**Reserved**
20	RO	1b	**Data Link Layer Link Active Reporting Capable** 0: Not supported 1: Supported
19	RO	1b	**Surprise Down Error Reporting Capable** This bit indicates support of detecting and reporting a Surprise Down error condition. 0: Not supported 1: Supported
18	RO	0	**Clock Power Management** 0: Not supported 1: Supported
17:15	RO	0	**L1 Exit Latency**
14:12	RO	011b	**L0s Exit Latency**
11:10	RO	11b	**Active State Link PM (ASPM) Support** 11b means entry support of L0S and L1.
9:4	RO	000001b	**Maximum Link Width** x1 lane supported
3:0	RO	0001b	**Maximum Link Speed** 0001: 2.5G b/s Link speed

Offset Address: 51-50h (D3F0)

Link Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8	RO	0	**Enable Clock Power Management** 0: Disable 1: Enable
7	RW	0	**Extended Synch** 0: FCU Timer limit is 30us. 1: FCU Timer limit is 120us.
6	RW	0	**Common Clock Configuration** 0: Indicates that this Port and the component on the opposite end of the Link are operating with **asynchronous** reference clock. 1: Indicates that this Port and the component on the opposite end of the Link are operating with a **distributed common** reference clock.
5	RW	0	**Retrain Link** Link retrain is initiated by writing 1 to this bit. This will direct the Physical Layer LTSSM to the Recovery state.
4	RW	0	**Link Disable** 0: Enable 1: Disable This bit disables the Link when set to 1.
3	RO	0	**Read Completion Boundary** 0: 64 byte
2	RO	0	**Reserved**
1:0	RW	00b	**Active State Link PM (ASPM) Control** 00: Disable 01: Enable L0s Entry 10: Enable L1 Entry 11: Enable L0s and L1 Entry

Offset Address: 53-52h (D3F0)

Link Status **Default Value: 1nn1h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RO	0	**Data Link Layer Link Active** 0: Inactive 1: Active
12	RO	1b	**Slot Clock Configuration** 0: Use an independent clock irrespective of the presence of a reference on the connector. 1: Use the same physical reference clock that the platform provides on the connector.
11	RO	0	**Link Training** This bit indicates the Link training is in progress (Physical Layer LTSSM in Configuration or Recovery state) or the Retrain Link bit is set 1 but Link training has not yet begun. Hardware will clear this bit once Link training is complete.
10	RO	0	**Training Error** Set when a Link training error occurred. Cleared by hardware upon successful training of the Link to the L0 Link state.
9:4	RO	HwInit	**Negotiated Link Width** 000001: x1 Others: Reserved
3:0	RO	0001b	**Link Speed** 0001: 2.5Gb/s negotiated Link speed 0000b: when DLUP =0

Offset Address: 57-54h (D3F0)

Slot Capabilities **Default Value: 0000 0060h**

Bit	Attribute	Default	Description
31:19	RO	0	**Physical Slot Number** Physical slot number attached to the Port.
18	RO	0	**No Command Completed Support** 0: Not supported 1: Supported
17	RO	0	**Electromechanical Interlock Present** 0: Not presented 1: Presented
16:15	RO	0	**Slot Power Limit Scale** Reserved
14:7	RO	0	**Slot Power Limit Value** Reserved
6	RO	1b	**Hot-plug Capable** Reserved (Do not program)
5	RO	1b	**Hot-plug Surprise** Reserved (Do not program)
4	RO	0	**Power Indicator Present** Reserved
3	RO	0	**Attention Indicator Present** Reserved
2	RO	0	**MRL Sensor Present** Reserved
1	RO	0	**Power Controller Present** Reserved
0	RO	0	**Attention Button Present** Reserved

Offset Address: 59-58h (D3F0)

Slot Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved**
12	RW	0	**Enable Data Link Layer State Change Report** 0: Disable 1: Enable
11	RW	0	**Electromechanical Interlock Control** 0: Disable 1: Enable
10	RO	0	**Power Controller Control** Reserved
9:8	RW	0	**Power Indicator Control** Reserved
7:6	RW	0	**Attention Indicator Control** Reserved
5	RW	0	**Hot-Plug Interrupt Enable** Reserved
4	RW	0	**Command Completed Interrupt Enable** Reserved
3	RW	0	**Presence Detect Changed Enable** Reserved
2	RO	0	**MRL Sensor Changed Enable** Reserved
1	RO	0	**Power Fault Detected Enable** Reserved
0	RW	0	**Attention Button Pressed Enable** Reserved

Offset Address: 5B-5Ah (D3F0)

Slot Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8	RW1C	0	**Data Link Layer State Changed** 0: No state changed 1: State changed
7	RO	0	**Electromechanical Interlock Status**
6	RO	0	**Card Presence State** 0: Slot empty 1: Card present in slot
5	RO	0	**MRL (Manually Operated Retention Latch) Sensor State** Reserved
4	RW1C	0	**Command Completed** 0: Not completed 1: Completed
3	RW1C	0	**Presence Detect Changed** 0: Not changed 1: Changed
2	RO	0	**MRL Sensor Changed** 0: Not changed 1: Changed
1	RO	0	**Power Fault Detected** 0: Not detected 1: Detected
0	RW1C	0	**Attention Button Pressed** 0: No state changed 1: State changed

Offset Address: 5D-5Ch (D3F0)

Root Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:5	RO	0	**Reserved**
4	RW	0	**CRS Software Visibility Enable** 0: Disable 1: Enable the Root Port to return Configuration Request Retry Status (CRS) Completion Status to software.
3	RW	0	**PME Interrupt Enable** 0: Disable 1: Enable interrupt generation upon receipt of a PME message as reflected in the PME status register bit. A PME interrupt is also generated if the PME status register bit is set when this bit is set from a cleared state.
2	RW	0	**System Error on Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Fatal Error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
1	RW	0	**System Error on Non-Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Non-Fatal Error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
0	RW	0	**System Error on Correctable Error Enable** 0: Disable 1: Enable generation of a System Error if a Correctable Error (ERR_COR) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.

Offset Address: 5Eh (D3F0)

Root Capabilities Register **Default Value: 0000h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RO	0	**Capability of CRS Software Visibility** 0: Disabled 1: Enabled. The Root Port will return CRS Completion Status to software.

Offset Address: 5Fh (D3F0) – Reserved

Offset Address: 63-60h (D3F0)

Root Status **Default Value: 000n 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	HwInit	**PME Pending** 0: No pending PME 1: Indicate that another PME is pending when the PME Status (bit 16) is set.
16	RW1C	0	**PME Status** Indicate that the PME was asserted by the Requestor ID indicated in PME Requestor ID (bit[15:0]).
15:0	RO	0	**PME Requestor ID** The Requestor ID of the last PME Requestor.

Offset Address: 64-67h (D3F0) – Reserved

PCI Power Management Capability Structure Registers (68-6Fh)

Offset Address: 6B-68h (D3F0)

Power Management Capabilities **Default Value: C822 7001h**

Bit	Attribute	Default	Description
31:27	RO	19h	**PME Support** 0: Not supported 1: Supported Bit 31, 30 and 27 are set to 1b (PME Message will be forwarded).
26	RO	0	**D2 Support** 0: Not supported 1: Supported
25	RO	0	**D1 Support** 0: Not supported 1: Supported
24:22	RO	0	**AUX Current**
21	RO	1b	**Reserved** (Do not program)
20:19	RO	0	**Reserved**
18:16	RO	010b	**Version**
15:8	RO	70h	**Next Capability Pointer**
7:0	RO	01h	**Capability ID** 01h indicates extended capability ID for the advanced error reporting capability.

Offset Address: 6F-6Ch (D3F0)

Power Management Status / Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Power Management Data**
23:16	RO	0	**Reserved**
15	RW1CS	0	**PME Status** This bit's setting is not modified by hot, warm, or cold reset.
14:9	RO	0	**Reserved**
8	RWS	0	**PME Enable** This bit's setting is not modified by hot, warm, or cold reset.
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** 00b: D0 01b: D1 10b: D2 11b: D3hot

PCI Message Signal Interrupt (MSI) Capability Structure Registers (70-87h)

Offset Address: 73-70h (D3F0)

MSI Capability Support **Default Value: 0180 9805h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24	RO	1b	**Supports Pre-vector Masking Capability** 0: Not supported 1: Supported
23	RO	1b	**Supports 64 Bit Message Address Only** 0: Not supported 1: Supported
22:20	RW	000b	**Multiple Message Enable** 000: 1 message allocated 001: 2 messages allocated 010: 4 messages allocated 011: 8 messages allocated 100: 16 messages allocated 101: 32 messages allocated 11x: Reserved
19:17	RO	000b	**Multiple Messages Capable** 000: 1 message requested 001: 2 messages requested 010: 4 messages requested 011: 8 messages requested 100: 16 messages requested 101: 32 messages requested 11x: Reserved
16	RW	0	**MSI Enable** 0: This Port is prohibited from using MSI to request service. 1: This Port is permitted to use MSI to request service.
15:8	RO	98h	**Next Capability Pointer**
7:0	RO	05h	**Capability ID** 05h indicates the extended capability ID for the root complex link declaration capability.

Offset Address: 77-74h (D3F0)

System-Specified Message Address - Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**System-Specified Message Address Bit [31:2]**
1:0	RO	0	**System-Specified Message Address Bit [1:0]** These bits will always read as 0.

Offset Address: 7B-78h (D3F0)

System-Specified Message Address - High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**System-Specified Message Address Bit [63:32]**

Offset Address: 7D-7Ch (D3F0)

Message Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data** The message data is put on data [15:0] of MSI cycles.

Offset Address: 7E-7Fh (D3F0) – Reserved

Offset Address: 83-80h (D3F0)
Message Mask Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RW	0	**Mask Bit for Message 0** 0: Not masked 1: Mask message 0

Offset Address: 87-84h (D3F0)
Message Pending Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RO	0	**Pending Bit for Message 0** 0: Not pending 1: Pending

Message Signal Interrupt (MSI) Capability Registers (88-97h)

Offset Address: 88-97h (D3F0) – Reserved

Subsystem ID and Subsystem Vendor ID Capability Registers (98-9Fh)

Offset Address: 98h (D3F0)
Capability ID **Default Value: 0Dh**

Bit	Attribute	Default	Description
7:0	RO	0Dh	**Capability ID** 0Dh is the capability ID for "Subsystem ID / Subsystem Vendor ID."

Offset Address: 99h (D3F0)
Next Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Pointer**

Offset Address: 9A-9Bh (D3F0) – Reserved

Offset Address: 9D-9Ch (D3F0)
Subsystem Vendor ID Control **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 9F-9Eh (D3F0)
Subsystem ID Control **Default Value: E353h**

Bit	Attribute	Default	Description
15:0	RO	E353h	**Subsystem ID**

PCI Express Transaction Layer Registers (A0-AFh)

Offset Address: A0h (D3F0)

Downstream Control 1 **Default Value: 11h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Cycles Have Traffic Class TC1** 0: Disable 1: Enable
6	RW	0	**Downstream Cycles Have Attribute "No Snoop" Set** 0: Disable 1: Enable
5	RW	0	**Downstream Cycles Have Attribute "Relaxed Ordering" Set** 0: Disable 1: Enable
4	RW	1b	**Downstream Lock Cycle Support** 0: Disable 1: Enable
3	RW	0	**Downstream Arbitration Scheme** 0: Fixed priority: VC1 CPL > VC0 CPL > Down Stream Command 1: Round Robin arbitration priority between VC1 CPL, VC0 CPL and Down Stream Command.
2	RW	0	**Downstream Post-Write Allowed to Pass IOW** 0: Not allowed 1: Allowed
1	RW	0	**Downstream Post-Write Allowed to Pass Read** 0: Not allowed 1: Allowed
0	RW	1b	**Downstream Pipeline** 0: Disabled 1: Enabled

Offset Address: A1h (D3F0)

Downstream Control 2 **Default Value: 14h**

Bit	Attribute	Default	Description
7	RW1C	0	**Downstream Configuration Completion Status** 0: Normal completion. 1: At least one configuration request ended with a CRS completion.
6	RW	0	**TRANS Assert Wait State Control** 0: TRANS cannot assert wait state at receiving downstream write data (original design). 1: TRANS can assert wait state at receiving downstream write data.
5	RW	0	**Data Return of Upstream Read Requests** 0: The chip always checks CPL credit unless the endpoint advertises infinite CPL credits. 1: The chip does not check CPL credit even when endpoint advertises finite CPL credits.
4	RW	1b	**Not Check Downstream PH Credit for PME_TURN_OFF Message** 0: Disable 1: Enable
3	RW	000b	**Enable C2P Read Completion Timer for Vector Development Mode** 0: Disable 1: Enable When this bit is set to 1, the timer is defined in RxA1[2:0] becomes: 000: 1 us 001: 3 us 010: 10 us 011: 20 us 100: 50 us 101: 100 us 110: 200 us 111: 500 us
2:0	RW	100b	**C2P Read Completion Timeout Timer** 000: Reserved 001: 1ms 010: Reserved 011: 10 ms (Spec. lower bound) 100: 30 ms 101: Reserved 11x: Reserved

Offset Address: A2h (D3F0)

Downstream Control 3 **Default Value: 30h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Ordering Queue Timing Option** 0: 1T setup time 1: 2T setup time
6:4	RW	011b	**Waiting Time for GNT Timer in Priority Arbitration Mode** 000: 4 ns 001: 16 ns 010: 32 ns 011: 64 ns 100: 96 ns 101: 128 ns 110: 256 ns 111: 512 ns If GNT timer of VC0 / C2P request expires, VC0 / C2P request will become higher priority. Priority VC1 > VC0 > C2P request when set RxA0[3] = 0
3	RO	0	**Reserved**
2	RW	0	**Pending C2P NP Completion Cycle to Block L1 Entry** 0: Disable. L1 entry does not wait for C2P NP completion. 1: Enable. L1 entry waits for C2P NP completion.
1:0	RW	00b	**Downstream Arbitration Parking** 00: GNT parks on the last request source. 01: GNT parks on VC1 completion. If VC1 is not enabled (or no VC1), park on VC0 completion. 10: GNT parks on VC0 completion. 11: GNT parks on C2P request.

Offset Address: A3h (D3F0)

Downstream Control 4 **Default Value: 78h**

Bit	Attribute	Default	Description
7:4	RW	0111b	**Retry Buffer Level:** 0000: 1-level 0001: 2-level 0010: 3-level 0011: 4-level 0100: 5-level 0101: 6-level 0110: 7-level 0111: 8-level Others: Reserved
3	RW	1b	**Downstream Read Retry Time Out Control in DL_Down State** 1: Enable downstream read retry time out. The timer is the same as completion time out timer. After time out, this read request will not be retried again even DL_DLUp assertion occurred. 0: Disable downstream read retry time out. If RxA3[0] is set to 1, downstream read request will always wait for DL_DLUp assertion then retry.
2	RW	0	**Downstream Cycle Control / Latency Improvement** 0: Disable 1: Enable
1	RW	0	**CPL Timer Control** 0: Enable. Refer to D3F0 RxA1[2:0]. 1: Disable
0	RW	0	**Downstream Read Cycle Retry** 0: When DL_DOWN is asserted, transaction layer returns "FF" to Central Traffic Controller for C2P read cycle. 1: When DL_DOWN is asserted, transaction layer holds C2P read cycle. This incomplete C2P read cycle will be retried when DL_UP is asserted.

Offset Address: A4h (D3F0)

Upstream Control **Default Value: 1Dh**

Bit	Attribute	Default	Description
7	RW	0	**Force Upstream Address A35~A31 to 0** 0: Disable 1: Enabled for system testing or loop back mode test. The upcoming data may be checked in the system memory.
6	RO	0	**Reserved**
5	RW	0	**Upstream Check Malformed TLP through "Byte Enable Rule" and "Over 4K Boundary Rule"** 0: Disable 1: Enable
4	RW	1b	**Downstream Read Waits till the Upstream Write Data Flushed** 0: Disable 1: Enable
3	RW	1b	**CPLH, CPLD, and NPD Become Infinite Mode** 0: Disable 1: Enable
2	RW	1b	**Update Header Credit Whenever Received TLPH (including PH, NPH and CPLH** 0: Disable 1: Enable
1	RW	0	**VC1 Request Queue Usage** (when VC1 is disabled in the capability header; i.e. Rx144[0] = 0) 0: Disable 1: Enable. It allows Transaction Layer maps non-snoop upstream request through VC1 Request Queue to the Central Traffic Controller (Note: When this bit is 1, bit-0 must be 0).
0	RW	1b	**Disable Virtual Channel 1 Support** 0: Enable VC1. Data FIFO of VC1 is used by VC1. 1: Disable VC1. Data FIFO of VC1 is reallocated to VC0, which doubles the size of VC0 data FIFO.

Offset Address: A5h (D3F0)

Credit Advertisement Control 1 **Default Value: FFh**

Bit	Attribute	Default	Description
7:4	RW	1111b	**Upstream Posted (write) Data FIFO Size, and the Initial PD Credit Value** 0000: 1-line upstream write FIFO size, and initial PD credit = 4h 0001: 2-line upstream write FIFO size, and initial PD credit = 8h 0010: 3-line upstream write FIFO size, and initial PD credit = Ch 0011: 4-line upstream write FIFO size, and initial PD credit = 10h 0100: 5-line upstream write FIFO size, and initial PD credit = 14h 0101: 6-line upstream write FIFO size, and initial PD credit = 18h 0110: 7-line upstream write FIFO size, and initial PD credit = 1Ch 0111: 8-line upstream write FIFO size, and initial PD credit = 20h 1xxx: 8-line upstream write FIFO size, and initial PD credit = 20h
3:0	RW	1111b	**Upstream PH Header Queue Size, and the Initial PH Credit** 0000: 1-level PH header queue, and initial PH credit = 2h 0001: 2-level PH header queue, and initial PH credit = 4h 0010: 4-level PH header queue, and initial PH credit = 6h 0011: 8-level PH header queue, and initial PH credit = 8h 01xx: 8-level PH header queue, and initial PH credit = 8h 1xxx: 8-level PH header queue, and initial PH credit = 8h

Offset Address: A6h (D3F0)

Credit Advertisement Control 2 **Default Value: 7Fh**

Bit	Attribute	Default	Description
7	RW	0	**Upstream Non-Posted Header Credit Infinite Mode Control** 0: The non-posted header credit is finite and has to update NPH credits. 1: The non-posted header credit is infinite and not necessary to update NPH credits.
6:4	RW	111b	**Upstream Read CPL Header Size** 0xx: 32QW 4-level 1xx: 32QW 4-level
3:0	RW	1111b	**Upstream Non-Posted Request Queue Size, and Initial NPH Credit Value** 0000: 1-level NPH header queue, and initial NPH credit = 2h 0001: 2-level NPH header queue, and initial NPH credit = 4h 0010: 4-level NPH header queue, and initial NPH credit = 6h 0011: 8-level NPH header queue, and initial NPH credit = 8h 01xx: 8-level NPH header queue, and initial NPH credit = 8h 1xxx: 8-level NPH header queue, and initial NPH credit = 8h

Offset Address: A8-A7h (D3F0)

Upstream Performance Control **Default Value: 01C4h**

Bit	Attribute	Default	Description
15	RW	0	**C2P Completion Timeout Method when PHY Retrains or Re-configures** 0: Keep the timeout value 1: Reset the timeout value
14	RO	0	**Reserved**
13:12	RW	00b	**Configuration Request Timeout Timer** 00: 100 ms 01: 500 ms 10: 1000 ms 11: 1500 ms
11:10	RO	0	**Reserved**
9:8	RW	01b	**Downstream Configuration Retry Request Timing after Receiving CRS Completion** 00: Assert 1T after CRS is received 01: Assert 4T after CRS is received 10: Assert 8T after CRS is received 11: Assert 16T after CRS is received
7:6	RW	11b	**Control the Maximum Number of Outstanding Expected WPOP Issued** 00: TRANS accepts 48 outstanding expected WPOP 01: TRANS accepts 56 outstanding expected WPOP 10: TRANS accepts 64 outstanding expected WPOP 11: No constraint on consecutive WPOP
5	RW	0	**Enable Transaction Layer Header Queue Pre-load Design Dynamic Clock for Power Management** 1: Enable 0: Disable
4	RW	0	**Upstream Read FIFO Entry Release Timing Control** 0: Upstream read FIFO entry release when the last data pops into retry data FIFO. 1: Upstream read FIFO entry release when the first data pops into retry data FIFO
3	RW	0	**Downstream Read Data Waits for Previous Upstream Write Complete** 0: Disable 1: Enable
2	RW	1b	**Upstream Requests Read and Write Orders** 0: Upstream requests are served in order. 1: Upstream write always passes upstream read.
1	RW	0	**Upstream Read Data TLP Return Policy** 0: One upstream request with over 16DW length or non-8-QW boundary alignment must be split into multiple CPL TLPs. 1: Multiple CPL TLPs belong to the same upstream request can be merged into one single CPL TLP.
0	RO	0	**Upstream Write Cycle will be 4QW Align** 0: Disable 1: Enable

Offset Address: A9h (D3F0)

CRS Retry Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Enable of CRS Retry Mechanism** 0: No retry cycle for CRS, regardless of Rx5C[4] setting and return 'hffffffff for read cycles. 1: Follow Rx5C[4] setting.

Offset Address: AAh (D3F0)

Upstream Read Timing Option **Default Value: 10h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	1b	**UpdateFC-P Generation to The Endpoint for Upstream Write TLPs** 0: UpdateFC-P is generated only when PD update is requested 1: UpdateFC-P is generated when PH or PD update is requested
3:1	RO	0	**Reserved**
0	RW	0	**Upstream Read Timing Option** 0: Fast timing, better read performance 1: Moderate timing, medium read performance

Offset Address: AB-AFh (D3F0) – Reserved

PCI Express Data Link Layer Registers (B0-BFh)

Offset Address: B0h-B1h (D3F0) – Reserved

Offset Address: B2h (D3F0)

Flow Control Initialization (FCI) / Flow Control Unit (FCU) and Status **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW1C	0	**FCI / FCU Timeout Status** 0: No time out 1 The FCI / FCU timeout has occurred.
6	RW	1b	**FCI / FCU Receive Timer Enable Control** 0: Disable the timeout mechanism 1: Enable the timeout mechanism
5	RW	0	**FCI / FCU Receive Timer Limit** 0: Timeout limit of 200 us 1: Timeout limit of 300 us
4	RW	0	**FCI / FCU Receive Timer Reset Control** 0: Timer reset by FCI / FCU only 1: Timer reset by any received DLLPs
3:0	RO	0	**Reserved**

Offset Address: B3h (D3F0)
Replay Timer Control **Default Value: 81h**

Bit	Attribute	Default	Description
7:6	RW	10b	**Replay Timer Control While Rewinding** (resend those DLLPs which do not have corresponded ACK / NAK received) 00: Hold Replay Timer during rewinding. 01: During rewinding, if ACK / NAK comes in, reset and hold the Replay Timer. 10: During rewinding, reset and hold the Replay Timer as long as the Retry Buffer is empty. 11: Reserved.
5:3	RO	0	**Reserved**
2:0	RW	001b	**Count of Replay Timer Expired During RXL0s (Receiving Physical in L0s State) Before Resend the TLP** **When Rx50[7] is set to 0:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 1x Replay timer expired 010: Resend the TLP after 2x Replay timer expired 011: Resend the TLP after 4x Replay timer expired 100: Resend the TLP after 8x Replay timer expired 101: Resend the TLP after 16x Replay timer expired 110: Resend the TLP after 32x Replay timer expired 111: Resend the TLP after 64x Replay timer expired **When RX50[7] is set to 1:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 16 x Replay timer expired 010: Resend the TLP after 32 x Replay timer expired 011: Resend the TLP after 64 x Replay timer expired 100: Resend the TLP after 128 x Replay timer expired 101: Resend the TLP after 256 x Replay timer expired 110: Resend the TLP after 512 x Replay timer expired 111: Resend the TLP after 1024 x Replay timer expired

Offset Address: B4h (D3F0)
Arbitration Control **Default Value: 05h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**TLP Flow Control Initialization for VC0 in Arbitration** 0: TLP is not allowed to pass Flow Control Initialization 2 (FCI2) for VC0. 1: TLP is allowed to pass Flow Control Initialization 2 (FCI2) for VC0.
2:0	RW	101b	**Data Link TX Packets Arbitration Scheme** 000: Round Robin 001: Reserved 010: Strict priority: TLP > ACK/NAK > FCU 011: Strict priority: TLP > FCU > ACK/NAK 100: Strict priority: ACK / NAK > TLP > FCU 101: Strict priority: ACK / NAK > FCU > TLP 110: Strict priority: FCU > TLP > ACK/NAK 111: Strict priority: FCU > ACK / NAK > TLP

Offset Address: B5h (D3F0)

FCU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**FCU Timer Control** 0: Update flow control credit when either Transaction Layer requested packets being sent or when FCU timer expired. 1: Update flow control credit only when FCU timer expired.
5:4	RW	00b	**ACK DLLP Collapse Method** 00: Send ACK when the latency timer expired 01: Send ACK every 4 correct TLPs have been received 10: Send ACK every 8 correct TLPs have been received 11: Send ACK every 16 correct TLPs have been received
3:2	RO	0	**Reserved**
1	RW	0	**FCI Process End Condition** 0: Complete FCI process when TLP / FCU has been received. 1: Do not complete FCI process even when TLP / FCU has been received.
0	RW	0	**VC1 FCI DLLP Transmission Scheme** 0: Transmit FCI DLLP (Data Link Layer Packet)only when FCI timer expired. 1: Transmit FCI DLLP continuously as long as the FCI process is not finished.

Offset Address: B6h (D3F0)

Transaction / Link Layer Checking Control **Default Value: A1h**

Bit	Attribute	Default	Description
7	RW	1b	**Nak_Scheduled Flag Control** Nak_Scheduled Flag is set after a Nak is scheduled by receiving a TLP with CRC or Seq_Num ERROR, and Nak_Scheduled Flag is cleared after receiving a new Ack. 0: Disable Nak_Scheduled Flag. Schedule Nak regardless of Nak_Scheduled Flag. 1: Enable Nak_Scheduled Flag. Nak can only be scheduled when Nak_Scheduled Flag is cleared.
6:5	RW	01b	**TLP Receiving Timer** When timeout, reset error-framing byte-counter. 00: Reset byte-counter 1 us after TLP header received. 01: Reset byte-counter 2 us after TLP header received. 10: Reset byte-counter 3 us after TLP header received. 11: Reset byte-counter 4 us after TLP header received.
4	RW	0	**The First Downstream TLP is Popped out from TL 1T Earlier**
3:1	RO	0	**Reserved**
0	RW	1b	**LCRC Check Control** 0: Do not check LCRC. 1: Check LCRC.

Offset Address: B7h (D3F0) – Reserved

Offset Address: B8h (D3F0)
Data Link Layer Header Position **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Data Link Layer Header Position** 0: SDP (Start DLLP) can be in Lane 0 / 4 / 8 / 12. 1: SDP (Start DLLP) is always at Lane 0.

Offset Address: B9h (D3F0) – Reserved

Offset Address: BAh (D3F0)
ACK / NAK Latency Timer Limit 1 **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:0	RW	0Ch	**ACK / NAK Latency Timer in Large LSNLW Setting** This timer is used for AckNak_latency_timer when LSNLW (Link Status Register-Negotiation Link Width) is x16. 00h: 4 x 1 Clocks (Clock = 250 Mhz) 01h: 4 x 2 Clocks 02h: 4 x 3 Clocks ….. FFh: 4 x 256 Clocks

Offset Address: BBh (D3F0)
ACK / NAK Latency Timer Limit 2 **Default Value: 12h**

Bit	Attribute	Default	Description
7:0	RW	12h	**ACK / NAK Latency Timer in Medium LSNLW Setting** This timer is used for AckNak_latency_timer when LSNLW is x8 / x4. 00h: 4 x 1 Clocks (Clock = 250Mhz) 01h: 4 x 2 Clocks 02h: 4 x 3 Clocks. ….. FFh: 4 x 256 Clocks

Offset Address: BCh (D3F0)
ACK / NAK Latency Timer Limit 3 **Default Value: 3Bh**

Bit	Attribute	Default	Description
7:0	RW	3Bh	**ACK / NAK Latency Timer in Small LSNLW Setting** This timer is used for AckNak_latency_timer when LSNLW is x2 / x1. 00h: 4 x 1 Clocks (Clock =250Mhz) 01h: 4 x 2 Clocks 02h: 4 x 3 Clocks ….. FFh: 4 x 256 Clocks

Offset Address: BDh (D3F0)
Replay Timer Limit 1 **Default Value: 12h**

Bit	Attribute	Default	Description
7:0	RW	12h	**Replay_timer_limit in Large LSNLW Setting** This timer is used for Replay_timer when LSNLW is x16. 00h: 8 x 1 Clocks (Clock = 250Mhz) 01h: 8 x 2 Clocks 02h: 8 x 3 Clocks ……. FFh: 8 x 256 Clocks

Offset Address: BEh (D3F0)
Replay Timer Limit 2 **Default Value: 1Bh**

Bit	Attribute	Default	Description
7:0	RW	1Bh	**Replay_timer_limit in Medium LSNLW Setting** This timer is used for Replay_timer when LSNLW is x8 / x4. 00h: 8 x 1 Clocks (Clock =250Mhz) 01h: 8 x 2 Clocks 02h: 8 x 3 Clocks ……. FFh: 8 x 256 Clocks

Offset Address: BFh (D3F0)
Replay Timer Limit 3 **Default Value: 58h**

Bit	Attribute	Default	Description
7:0	RW	58h	**Replay_timer_limit in Small LSNLW Setting** This timer is used for Replay_timer when LSNLW is x2 / x1 00h: 8 x 1 Clocks (Clock =250Mhz) 01h: 8 x 2 Clocks 02h: 8 x 3 Clocks ……. FFh: 8 x 256 Clocks

PCI Express Physical Layer Registers (C0-CFh)

Offset Address: C0h (D3F0)

PHY General Control **Default Value: 03h**

Bit	Attribute	Default	Description
7	RW	0	**Quick Timeout Counter Setting** When set to 1, PHY timeout period will be shorter as below: 2 ms → 4 us 12 ms → 24 us 24 ms → 48 us 48 ms → 96 us 1024 ts → 32 ts Receiver Detection: 15x1024 ns → 1x1024 ns
6	RW	0	**Disable Data Scrambling / Descrambling** 0: Enable 1: Disable
5:3	RW	000b	**Loopback Mode Selection** 000: No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: External loopback from TX end to RX end 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved See the figure below for details.
2:0	RW	011b	**COMMA Detection Window** 000 / 001: Illegal values. Others: Delay number of T to determine correct lane-to-lane deskew value.

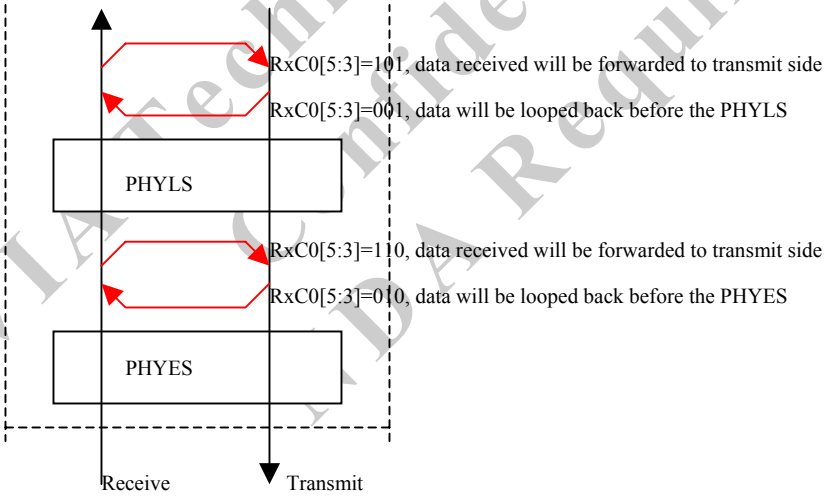


Figure 3. Loop Back Mode Selections

Offset Address: C1h (D3F0)
PHYLS General Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Enable Aggressive Power Management When No Device Plug** 0: Disable 1: Enable
5	RW	0	**Enable Aggressive Power Management in Rx Path to Data Link Layer Module** 0: Disable 1: Enable
4:0	RW	00000b	**PHY Lane Configuration Setting** 00000: Use PHY negotiation 00001: x1 with normal connection 10101: Force into L0s state (for testing and measurement used only) 11000: Force into DETECT_QUIET state (for testing measurement used only) 11001: Force into DETECT_ACTIVE state (for testing measurement used only) Other values are not allowed.

Offset Address: C2h (D3F0)
PHYLS MAC and PCS **Default Value: 27h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Reset Elastic Buffer** Always reads 0.
5	RW	1b	**Lane Enable** 0: Enable lanes based on LTSSM negotiation results. 1: Enable lanes based on receiver detection's results.
4	RW	0	**Bypass PHYES Device Detection in Detect Phase of LTSSM** 0: Enable PHYES to actually perform receiver detection in Detect phase. 1: Bypass receiver detection, and assume device exists. Usually, only set to "1" for testing or debugging.
3	RO	0	**Reserved**
2	RW	1b	**Wait IDL Ordered Set or Electrical Idle When L1 / L23 Entry** 0: Always wait IDL ordered set for L1 / L23 entry. 1: Wait Electrical Idle and ignore IDL ordered set for L1 / L23 entry.
1	RW	1b	**Disparity Check Enable** 0: Disable 1: Enable
0	RW	1b	**State Machine LTSSM (Link Training and Status State Machine) Control** 0: Wait for the electrical idle signal from the PHYES or wait 12 ms after LTSSM enters Detect.Quiet state. 1: Always wait for 12ms after LTSSM enters Detect.Quiet state.

Offset Address: C3h (D3F0)

PHYLS LTSSM State **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**PHYLS LTSSM State** See the table below.

Table 17. Mapping Table for D3F0 RxC3

LTSSM States	Binary Coding (RxC3)	Hexadecimal Coding
DETECT_QUIET	8'B0000_0000	8'H00
DETECT_ACTIVE	8'B0000_0001	8'H01
POLLING_ACTIVE	8'B0001_0000	8'H10
POLLING_CONFIGURATION	8'B0001_0001	8'H11
POLLING_SPEED	8'B0001_0010	8'H12
POLLING_COMPLIANCE	8'B0001_0100	8'H14
CONFIGURATION_RCVRCFG_STEP_1	8'B0010_0001	8'H21
CONFIGURATION_RCVRCFG_STEP_2	8'B0010_0010	8'H22
CONFIGURATION_RCVRCFG_STEP_3	8'B0010_0011	8'H23
CONFIGURATION_RCVRCFG_STEP_4	8'B0010_0100	8'H24
CONFIGURATION_RCVRCFG_STEP_5	8'B0010_0101	8'H25
CONFIGURATION_RCVRCFG_STEP_6	8'B0010_0110	8'H26
CONFIGURATION_RCVRCFG_STEP_7	8'B0010_0111	8'H27
CONFIGURATION_IDLE	8'B0010_1000	8'H28
RECOVERY_RCVRLOCK	8'B0011_0000	8'H30
RECOVERY_RCVRCFG	8'B0011_0001	8'H31
RECOVERY_IDLE	8'B0011_0011	8'H33
LOOPBACK_MSTR_ENTRY	8'B0100_0000	8'H40
LOOPBACK_MSTR_ACTIVE	8'B0100_0001	8'H41
LOOPBACK_MSTR_EXIT	8'B0100_0011	8'H43
LOOPBACK_SLAV_ENTRY	8'B0100_0100	8'H44
LOOPBACK_SLAV_ACTIVE	8'B0100_0101	8'H45
LOOPBACK_SLAV_EXIT	8'B0100_0111	8'H47
DISABLED_ENTRY	8'B0101_0000	8'H50
DISABLED_DISABLED	8'B0101_0001	8'H51
HOTRESET_ACTIVE	8'B0110_0000	8'H60
L0L0_TXL0_RXL0	8'B1000_1010	8'H8A
L0L0S_TXL0_RXENTRY	8'B1001_1000	8'H98
L0L0S_TXL0_RXIDLE	8'B1001_1001	8'H99
L0L0S_TXL0_RXFTS	8'B1001_1011	8'H9B
L0SL0_TXENTRY_RXL0	8'B1010_0010	8'HA2
L0SL0_TXIDLE_RXL0	8'B1010_0110	8'HA6
L0SL0_TXFTS_RXL0	8'B1010_1110	8'HAE
L0SL0S_TXENTRY_RXENTRY	8'B1011_0000	8'HB0
L0SL0S_TXENTRY_RXIDLE	8'B1011_0001	8'HB1
L0SL0S_TXENTRY_RXFTS	8'B1011_0011	8'HB3
L0SL0S_TXIDLE_RXENTRY	8'B1011_0100	8'HB4
L0SL0S_TXIDLE_RXIDLE	8'B1011_0101	8'HB5
L0SL0S_TXIDLE_RXFTS	8'B1011_0111	8'HB7
L0SL0S_TXFTS_RXENTRY	8'B1011_1100	8'HBC
L0SL0S_TXFTS_RXIDLE	8'B1011_1101	8'HBD
L0SL0S_TXFTS_RXFTS	8'B1011_1111	8'HBF
L1_ENTRY	8'B1100_0000	8'HC0
L1_IDLE	8'B1100_0001	8'HC1
L23READY_ENTRY	8'B1101_0000	8'HD0
L23READY_IDLE	8'B1101_0001	8'HD1

Offset Address: C4h (D3F0)

Elastic Buffer Base Registers for Lane 0 to 1 **Default Value: 04h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	4h	**Elastic Buffer Base Register for Lane 0** 0, 1, 7: Illegal values. Others: Delay numbers of T for elastic buffer operations.

Offset Address: C5-CCh (D3F0) – Reserved

Offset Address: CDh (D3F0)

PHYLS MAC **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Downstream Tx Arbitration between DLLM and PHYLS** 0: Normal arbitration 1: Arbitration with lower latency

Offset Address: CEh (D3F0) – Reserved

Offset Address: CFh (D3F0)

SKP Ordered Set Control **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Enable PHYES Level-2 Power Down** 0: Disable 1: Enable
3:2	RO	11b	**Reserved** (Do not program)
1:0	RW	00b	**SKP Order-set Scheduling Time** 00: Send out "SKP" Order-set on the PCIe bus every 1180 symbol time, it is around 4.72us. 01: Send out "SKP" Order-set on the PCIe bus every 118 symbol time, it is around 472ns. 10: Send out "SKP" Order-set on the PCIe bus every 6.12 us. 11: Reserved

PCI Express Power Management Module Registers (D0-D3h)

Offset Address: D0h (D3F0)

Power Management Controller PHYLS Control **Default Value: 50h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	101b	**Timeout Period** This timer is used when waiting for ACK from a device after issued PME_TURNOFF message to notify the device to move to power down mode. 000: 1 us 001: 2 us 010: 4 us 011: 8 us 100: 16 us 101: 32 us 110: 64 us 111: 128 us
3	RO	0	**Reserved**
2	RW	0	**Retrain Link when Bad DLLP is Checked** 0: Disable 1: Enable
1	RW	0	**Link Loopback** 0: Normal operation 1: Direct device to enter Loopback mode. Received data in the device will be sent to the transmit side.
0	RW	0	**Link Reconfigure Linkwidth** 0: When reconfigure linkwidth, LTSSM must be Detect state. 1: When reconfigure linkwidth, LTSSM can go to Configuration state.

Offset Address: D1h (D3F0)

PMU (Power Management Unit) Timeout **Default Value: 20h**

Bit	Attribute	Default	Description
7	RW1C	0	**Error Status Report** This bit is set when device cannot have electrical idle after the waiting period programmed at RxD1[5:4] expired.
6	RO	0	**Reserved**
5:4	RW	10b	**Electrical Idle Waiting Period before Move to L1 State** (after issue ACK to the L1 request from the device) 00: Always wait for electrical idle 01: Wait 32 clock 10: Wait 64 clock 11: Reserved
3:2	RO	0	**Reserved**
1:0	RW	00b	**Downstream Cycles Triggered C2P Cycles** Period of staying at L0 before returned to L1 for PHY (when PMU is not in D0 state). 00: Immediately 01: 1 cfgW or message + delay 10T 10: 1 32QW + 1 cfgW or message + delay 10T 11: 2 32QW + 1 cfgW or message + delay 10T

Offset Address: D2h (D3F0)

PMU L0s Idle Timeout **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Idle Period to Enter L0s** Minimum time period is 128ns (RxD2 = 00). 00h: 128 ns 01h: 2x128 ns 02h: 3x128 ns … FFh: 256x128 ns

Offset Address: D3h (D3F0)
PMU L1 Idle Timeout **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Idle Period to Enter ASL1** Minimum time period is 128 ns. 00h: 128 ns 01h: 2x128 ns 02h: 3x128 ns … FFh: 256x128 ns

Offset Address: D4-D7h (D3F0) – Reserved

PCI Express Message Controller Related Registers (D8-DFh)

Offset Address: D8h (D3F0)
Power Management Controller Express Message Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Excessive Errors Occurred But Not Reported in MSGC** 0: Normal operation. 1: There are errors not reported to the system.
6:0	RO	0	**Reserved**

Offset Address: D9-DFh (D3F0) – Reserved

PCI Express Electrical PHY Registers (E0-EFh)

Offset Address: E0h (D3F0) – Reserved

Offset Address: E1h (D3F0)
1 Lane Related Control of PHYES Module **Default Value: 08h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Receiving Polarity Change Control** 0: Have the same polarity on the loop-back / received data. 1: Have reverse polarity on the loop-back / received data.
3:2	RW	10b	**Squelch Window Select (64~175 mv) – For PE0**
1	RW	0	**Number of Non Idle Signal Detected Before Exit Idle State** (Electrical Idle State Exit Condition) 0: 10 bits 1: 2 bits
0	RW	0	**Number of Idle Signal Detected Before Enter Idle State** (Electrical Idle State Enter Condition) 0: 10 bits 1: 2 bits

Offset Address: E2-EFh (D3F0) – Reserved

PCI Express Electrical PHY Test Registers (F0-FFh)

Offset Address: F0h (D3F0) – Reserved

Offset Address: F1h (D3F0)

Repeated Count of the Test Pattern **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Repeated Count of the Test Pattern** (as selected in RxF2[7:4]) When using loopback mode to test electrical PHY, the following should be satisfied: RxF1 x 8 > loopback latency / 4 ns. 00-0Bh: Illegal value 0Ch: Test pattern repeats 12 times 0Dh: Test pattern repeats 13 times … FFh: Test pattern repeats 255 times

Offset Address: F2h (D3F0)

Test Pattern Selection **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Select Test Pattern** 0000: SKP order-set 0001: User define, use RxF6[9:0] 0010: K28.5 test bit sequence 0011: K28.7 test bit sequence 0100: K test for differential pair current 0101: J test for differential pair current 0110: D21.5 test bit sequence 0111: D30.3 test bit sequence 1000: Ten contiguous run of 3 test bit sequence 1001: Low transition density test bit sequence 1010: Half-rate/quarter-rate test bit sequence 1011: Low frequency spectral test bit sequence 1100: Simultaneous switching test bit sequence 1101: D 10.2 test bit sequence 1110: D 24.3 test bit sequence 1111: Compliance test bit sequence
3:0	RO	0	**Reserved**

Offset Address: F3h (D3F0)

Test Mode Control **Default Value: 06h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Electrical PHY Test Mode** Program this bit to 1 to start Electrical PHY test. 0: Disable 1: Enable
6:4	RO	0	**Reserved**
3:0	RW	6h	**Test Pattern Check Length** Number of T when the receiving side starts to check transmitted and received patterns. Suggested Value Settings: (Lane 0 for example) RxC0[5:3] = 001b: RxC4[2:0] + 2 RxC0[5:3] = 010b: RxC4[2:0] + 2 + (Loopback Path Latency / 4 ns)+1

Offset Address: F5-F4h (D3F0)

BIST Status 1 **Default Value: 0000h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9:0	RO	0	**Received Symbol** (When RxF3[7] is set 1) 10b'0: When RxF3[7] is 0.

Offset Address: F7-F6h (D3F0)

BIST Status 2 **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Electrical PHY Test Error** 0: No error detected 1: Indicates that there is an error detected in the receiving side during the loop back test mode.
14	RO	0	**Electrical PHY Built-In Self Test Error of Symbol Comparison** 0: No error detected 1: Indicates that some errors detected or COMMA symbols are never detected during PHYBIST period; reported from PTNCMP.
13:10	RO	0	**Reserved**
9:0	RW	0	**Transmitted Symbol** (When RxF3[7] is set to 1) 10b'0: When RxF3[7] is set to 0.

Offset Address: F9-F8h (D3F0)

PHY BIST Counter- Test Mode **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0000h	**PHY BIST Period for Electrical PHY Test Error**

Offset Address: FA-FFh (D3F0) – Reserved

Device 3 Function 0 (D3F0) – PCI Express Root Port 0 Extended Space

Registers defined in the Extended Space can be accessed through PCI Express Enhanced Configuration Access Mechanism, which utilizes a flat memory-mapped address space to access the configuration registers. Please check PCI Express Specification for the detailed information.

Advanced Error Reporting Capability (100-13Fh)

Offset Address: 103-100h (D3F0)

Advance Error Reporting Enhanced Capability Header **Default Value: 1401 0001h**

Bit	Attribute	Default	Description
31:20	RO	140h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0001h	**PCI Express Extended Capability ID**

Offset Address: 107-104h (D3F0)

Uncorrectable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20	RW1CS	0	**Unsupported Request Error Status (TL)**
19	RW1CS	0	**ECRC Error Status (TL)**
18	RW1CS	0	**Malformed TLP Status (TL)**
17	RW1CS	0	**Receiver Overflow Status (TL)**
16	RW1CS	0	**Unexpected Completion Status (TL)**
15	RW1CS	0	**Completer Abort Status (TL)**
14	RW1CS	0	**Completion Timeout Status (TL)**
13	RO	0	**Flow Control Protocol Error Status (TL)**
12	RW1CS	0	**Poisoned TLP Status (TL)**
11:6	RO	0	**Reserved**
5	RW1CS	0	**Surprise Down Error Status**
4	RW1CS	0	**Data Link Protocol Error Status (DLL)**
3:1	RO	0	**Reserved**
0	RW1CS	0	**Training Error Status (PHY)**

Offset Address: 10B-108h (D3F0)

Uncorrectable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20	RWS	0	**Unsupported Request Error Mask (TL)**
19	RWS	0	**ECRC Error Mask (TL)**
18	RWS	0	**Malformed TLP Mask (TL)**
17	RWS	0	**Receiver Overflow Mask (TL)**
16	RWS	0	**Unexpected Completion Mask (TL)**
15	RWS	0	**Completed Abort Mask (TL)**
14	RWS	0	**Completion Timeout Mask (TL)**
13	RWS	0	**Flow Control Protocol Error Mask (TL)**
12	RWS	0	**Poisoned TLP Mask (TL)**
11:6	RO	0	**Reserved**
5	RWS	0	**Surprise Down Error Mask**
4	RWS	0	**Data Link Protocol Error Mask (DLL)**
3:1	RO	0	**Reserved**
0	RWS	0	**Training Error Mask (PHY)**

Offset Address: 10F-10Ch (D3F0)

Uncorrectable Error Severity **Default Value: 0006 2031h**

Bit	Attribute	Default	Description
31:21	RO	0	Reserved
20	RWS	0	Unsupported Request Error Severity (TL)
19	RWS	0	ECRC Error Severity (TL)
18	RWS	1b	Malformed TLP Severity (TL)
17	RWS	1b	Receiver Overflow Error Severity (TL)
16	RWS	0	Unexpected Completion Error Severity (TL)
15	RWS	0	Completed Abort Error Severity (TL)
14	RWS	0	Completion Timeout Error Severity (TL)
13	RWS	1b	Flow Control Protocol Error Severity (TL)
12	RWS	0	Poisoned TLP Severity (TL)
11:6	RO	0	Reserved
5	RWS	1b	Surprise Down Error Severity
4	RWS	1b	Data Link Protocol Error Severity (DLL)
3:1	RO	0	Reserved
0	RWS	1b	Training Error Severity (PHY)

Offset Address: 113-110h (D3F0)

Correctable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13	RW1CS	0	Advisory Non-Fatal Error Status
12	RW1CS	0	Replay Timer Timeout Status (DLL)
11:9	RO	0	Reserved
8	RW1CS	0	REPLAY_NUM Rollover Status (DLL)
7	RW1CS	0	Bad DLLP Status (DLL)
6	RW1CS	0	Bad TLP Status (DLL)
5:1	RO	0	Reserved
0	RW1CS	0	Receiver Error Status (PHY)

Offset Address: 117-114h (D3F0)

Correctable Error Mask **Default Value: 0000 2000h**

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13	RWS	1b	Advisory Non-Fatal Error Mask
12	RWS	0	Replay Timer Timeout Mask (DLL)
11:9	RO	0	Reserved
8	RWS	0	REPLAY_NUM Rollover Mask (DLL)
7	RWS	0	Bad DLLP Mask (DLL)
6	RWS	0	Bad TLP Mask (DLL)
5:1	RO	0	Reserved
0	RWS	0	Receiver Error Mask (PHY)

Offset Address: 11B-118h (D3F0)

Advanced Error Capabilities and Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:9	RO	0	Reserved
8	RWS	0	ECRC Check Enable (TL)
7	RO	0	ECRC Check Capable (TL)
6	RWS	0	ECRC Generation Enable (TL)
5	RO	0	ECRC Generation Capable (TL)
4:0	ROS	0	First Error Pointer (TL)

Offset Address: 11F-11Ch (D3F0)
Header Log (TL) Register 1st DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 1st DW**

Offset Address: 123-120h (D3F0)
Header Log (TL) Register 2nd DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 2nd DW**

Offset Address: 127-124h (D3F0)
Header Log (TL) Register 3rd DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 3rd DW**

Offset Address: 12B-128h (D3F0)
Header Log (TL) Register 4th DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 4th DW**

Offset Address: 12F-12Ch (D3F0)
Root Error Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	RO	0	**Reserved**
2	RW	0	**Fatal Error Reporting Enable**
1	RW	0	**Non-Fatal Error Reporting Enable**
0	RW	0	**Correctable Error Reporting Enable**

Offset Address: 133-130h (D3F0)
Root Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	00h	**Advanced Error Interrupt Message Number (TL)**
26:7	RO	0	**Reserved**
6	RW1CS	0	**Fatal Error Messages Received (TL)**
5	RW1CS	0	**Non-Fatal Error Messages Received (TL)**
4	RW1CS	0	**First Uncorrectable Fatal Error Message Received (TL)** Set to 1 when the first Uncorrectable Error Message received is for a Fatal Error.
3	RW1CS	0	**Multiple ERR_FATAL/NONFATAL Received (TL)**
2	RW1CS	0	**ERR_FATAL / NONFATAL Received (TL)**
1	RW1CS	0	**Multiple ERR_COR Received (TL)**
0	RW1CS	0	**ERR_COR Received (TL)**

Offset Address: 137-134h (D3F0)
Error Source Identification **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	ROS	0	**ERR_FATAL/NONFATAL Source Identification (TL)**
15:0	ROS	0	**ERR_COR Source Identification (TL)**

Offset Address: 138-13Fh (D3F0) – Reserved

Virtual Channel Capability (140-14Fh)

Virtual Channel Capability is defined for Egress direction of the device. For Root Port, since only VC0 is defined.

- VC0 mapping: TC0, TC1, TC2, TC3, TC4, TC5, TC6, TC7
- No VC arbitration table
- No port arbitration table

Offset Address: 143-140h (D3F0)

Virtual Channel Enhanced Capability Header **Default Value: 1801 0002h**

Bit	Attribute	Default	Description
31:20	RO	180h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0002h	**PCI Express Extended Capability ID**

Offset Address: 147-144h (D3F0)

Port VC Capability 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:10	RO	0	**Port Arbitration Table Entry Size** Reserved for root port.
9:8	RO	0	**Reference Clock** Reserved for root port.
7	RO	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count**
3	RO	0	**Reserved**
2:0	RO	000b	**Extended VC Count**

Offset Address: 14B-148h (D3F0)

Port VC Capability 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**VC Arbitration Table Offset** 00 since only VC0 is defined.
23:8	RO	0	**Reserved**
7:0	RO	0	**VC Arbitration Capability** Reserved

Offset Address: 14D-14Ch (D3F0)

Port VC Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3:1	RO	0	**VC Arbitration Select** Reserved
0	RO	0	**Local VC Arbitration Table** Reserved

Offset Address: 14F-14Eh (D3F0)

Port VC Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	0	**VC Arbitration Table Status** Reserved

VC0 Resource (150-15Bh)

Offset Address: 153-150h (D3F0)

VC Resource Capability (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Arbitration Table Offset (VC0)** Reserved for Root Port.
23	RO	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)**
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching** Reserved
13:8	RO	0	**Reserved**
7:0	RO	0	**Port Arbitration Capability** Reserved for Root Port.

Offset Address: 157-154h (D3F0)

VC Resource Control (VC0) **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1b	**VC Enable**
30:27	RO	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	RO	0	**Reserved**
19:17	RO	0	**Port Arbitration Select** Reserved for Root Port.
16	RO	0	**Load Port Arbitration Table** Reserved for Root Port.
15:8	RO	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC / VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit-0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (D3F0)

VC Resource Status (VC0) **Default Value: 0002 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	1b	**VC Negotiation Pending (TL)** This bit indicates whether the Virtual Channel negotiation is in Pending state (set/clear by hardware). 0: Negotiation is complete. 1: Negotiation is on-going.
16	RO	0	**Port Arbitration Table Status** Reserved for Root Port.
15:0	RO	0	**Reserved**

VC1 Resource (15C-19Fh)

Offset Address: 15C-17Fh (D3F0) – Reserved

Offset Address: 183-180h (D3F0)

Root Complex Link Declaration Capabilities Header **Default Value: 0001 0005h**

Bit	Attribute	Default	Description
31:20	RO	0	**Next Capability**
19:16	RO	1h	**Capability Version**
15:0	RO	0005h	**Capability ID**

Offset Address: 187-184h (D3F0)

Element Self Description **Default Value: 0201 0100h**

Bit	Attribute	Default	Description
31:24	RO	02h	**Port Number**
23:16	RO	01h	**Component ID**
15:8	RO	01h	**Number of Link Entries**
7:4	RO	0	**Reserved**
3:0	RO	0	**Element Type** 0h: Configuration Space Element 1h: System egress port or internal sink 2h: Internal Root Complex Link

Offset Address: 188-18Fh (D3F0) – Reserved

Offset Address: 193-190h (D3F0)

Upstream Link Descriptor **Default Value: 0001 0001h**

Bit	Attribute	Default	Description
31:24	RO	0	**Target Port Number** Indicates the port number of RCRB-H.
23:16	RO	01h	**Target Component ID**
15:2	RO	0	**Reserved**
1	RO	0	**Link Type** Indicates the link points to RCRB-H.
0	RO	1b	**Link Valid**

Offset Address: 194-197h (D3F0) – Reserved

Offset Address: 19F-198h (D3F0)

Upstream Link Base Address for RCRB-H[63:12] **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:32	RO	0	**Base Address Upper**
31:0	RO	0	**Base Address Lower**

Device 3 Function 1 (D3F1) – PCI Express Root Port 1 (PCI-to-PCI Virtual Bridge)

Device 3 Function 1, a 1-Lane PCI Express Root Port, is connected to the PCI bus through AD14 as the IDSEL.
All registers are located in PCI configuration space and should be programmed using PCI configuration mechanism 1 through I/O registers CF8 / CFC with Bus Number 0, Device Number 3 and Function Number 1.

Header Registers (00-3Fh)

Offset Address: 01-00h (D3F1)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 03-02h (D3F1)

Device ID **Default Value: F353h**

Bit	Attribute	Default	Description
15:0	RO	F353h	**Device ID**

Offset Address: 05-04h (D3F1)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable** Set when the device is prevented from generating INTx messages. 0: Disable 1: Enable
9	RO	0	**Reserved**
8	RW	0	**SERR# Enable** 0: Disable error report. 1: Enable reporting of non-fatal and fatal errors.
7	RO	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors and continue. 1: Take normal action on detected parity errors.
5:3	RO	0	**Reserved**
2	RW	0	**Bus Master Enable** 0: Disable 1: Enable Controls the ability to forward Memory and I/O Read/Write requests in the upstream direction. Disabling this bit is to disable MSI messages.
1	RW	0	**Memory Space** 0: Ignore downstream memory transactions; memory cycles with address falling in the claimed range will be forwarded to the SM. 1: Enable downstream memory cycle to this port if its address falling in the claimed range of this device.
0	RW	0	**I/O Space** 0: Ignore downstream I/O transactions; I/O cycles with address falling in the claimed range will be forwarded to the SM. 1: Enable downstream I/O cycle to this port if its address falling in the claimed range of this device.

Offset Address: 07-06h (D3F1)
PCI Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set whenever a poisoned TLP is received, regardless the state of Parity Error Enabled (Rx4[6]).
14	RW1C	0	**Signaled System Error** This bit is set when: A device sends an ERR_FATAL or ERR_NONFATAL message. Rx04[8] = 1
13	RW1C	0	**Received Master Abort** This bit is set when receiving a completion with Unsupported Request Completion Status.
12	RW1C	0	**Received Target Abort** This bit is set when receiving a completion with Completer Abort Completion Status.
11	RW1C	0	**Signaled Target Abort** This bit is set when completing a Request with Completer Abort Completion Status.
10:9	RO	0	**Reserved** Always reads 0.
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6] is set and either one of the following two conditions occurs: Requestor receives a Completion marked poisoned. Requestor poisons a write Request.
7:5	RO	0	**Reserved**
4	RO	1b	**Capabilities List** Indicates the presence of an extended capability list item. Always set to 1 for PCI Express device.
3	RO	0	**Interrupt Status** Indicates an INTx message is pending internally.
2:0	RO	0	**Reserved**

Offset Address: 08h (D3F1)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	nnh	0	**Revision Code**

Offset Address: 0B-9h (D3F1)
Class Code **Default Value: 06 0400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Ch (D3F1)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D3F1)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Master Latency Timer**

Offset Address: 0Eh (D3F1)
Header Type **Default Value: 81h**

Bit	Attribute	Default	Description
7:0	RO	81h	**Header Type**

Offset Address: 0Fh (D3F1)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST Support**

Offset Address: 17-10h (D3F1)
Base Address Register **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:0	RO	0	**Base Address**

Offset Address: 18h (D3F1)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Primary Bus Number**

Offset Address: 19h (D3F1)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Secondary Bus Number**

Offset Address: 1Ah (D3F1)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subordinate Bus Number**

Offset Address: 1Bh (D3F1) – Reserved

Offset Address: 1Ch (D3F1)
I/O Base **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	Fh	**I/O Base (AD[15:12] - Inclusive)** This bridge will forward the cycles from primary side to PCI if the I/O address AD[15:12] is between I/O base and I/O limit (Rx1D[7:4]).
3:0	RO	0	**I/O Addressing Capability** 0 means I/O addressing is 16-bit only.

Offset Address: 1Dh (D3F1)
I/O Limit **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**I/O Limit (AD[15:12] - Inclusive)** This bridge will forward the cycles from primary side to PCI if the I/O address is between I/O base (Rx1C) and I/O limit.
3:0	RO	0	**I/O Addressing Capability** 0 means I/O addressing is 16-bit only.

Offset Address: 1F-1Eh (D3F1)
Secondary Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** This bit is set when secondary side receives a poisoned TLP regardless of Rx4[6].
14	RW1C	0	**Received System Error** This bit is set when Rx4[8] is 1 and a device sends an ERR_FATAL or ERR_NONFATAL message.
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RW1C	0	**Signaled Target Abort**
10:9	RO	0	**Reserved**
8	RW1C	0	**Master Data Parity Error** This bit is set if Parity Error Enable bit (Rx4[6]) is set and either one of the following two conditions occurs: 1. Requestor receives a Completion marked poisoned. 2. Requestor poisons a write Request.
7:0	RO	0	**Reserved**

Offset Address: 21-20h (D3F1)
Memory Base **Default Value: FFF0h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Memory Base (AD[31:20] – Inclusive)** The address bits [19:0] are not decoded.
3:0	RO	0	**Reserved**

Offset Address: 23-22h (D3F1)
Memory Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RW	000h	**Memory Limit (AD[31:20] – inclusive)** The address [19:0] is not decoded.
3:0	RO	0	**Reserved**

Offset Address: 25-24h (D3F1)
Prefetchable Memory Base **Default Value: FFF1h**

Bit	Attribute	Default	Description
15:4	RW	FFFh	**Prefetchable Memory Base AD[31:20]**
3:1	RO	0	**Reserved**
0	RO	1b	**Report Support Prefetchable 64 Bits Memory Addressing** 0: Not supported 1: Supported

Offset Address: 27-26h (D3F1)
Prefetchable Memory Limit **Default Value: 0001h**

Bit	Attribute	Default	Description
15:4	RW	0	**Prefetchable Memory Limit AD[31:20]**
3:1	RO	0	**Reserved**
0	RO	1b	**Report Support Prefetchable 64 Bits Memory Addressing** 0: Not supported 1: Supported

Offset Address: 2B-28h (D3F1)
Prefetchable Memory Upper Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:0	RW	0	**AD[35:32]** This chip supports up to 16G.

Offset Address: 2F-2Ch (D3F1)
Prefetchable Memory Upper Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3:0	RW	0	**AD[35:32]** This chip supports up to 16G.

Offset Address: 31-30h (D3F1)
Upper I/O Base **Default Value: 0000h**

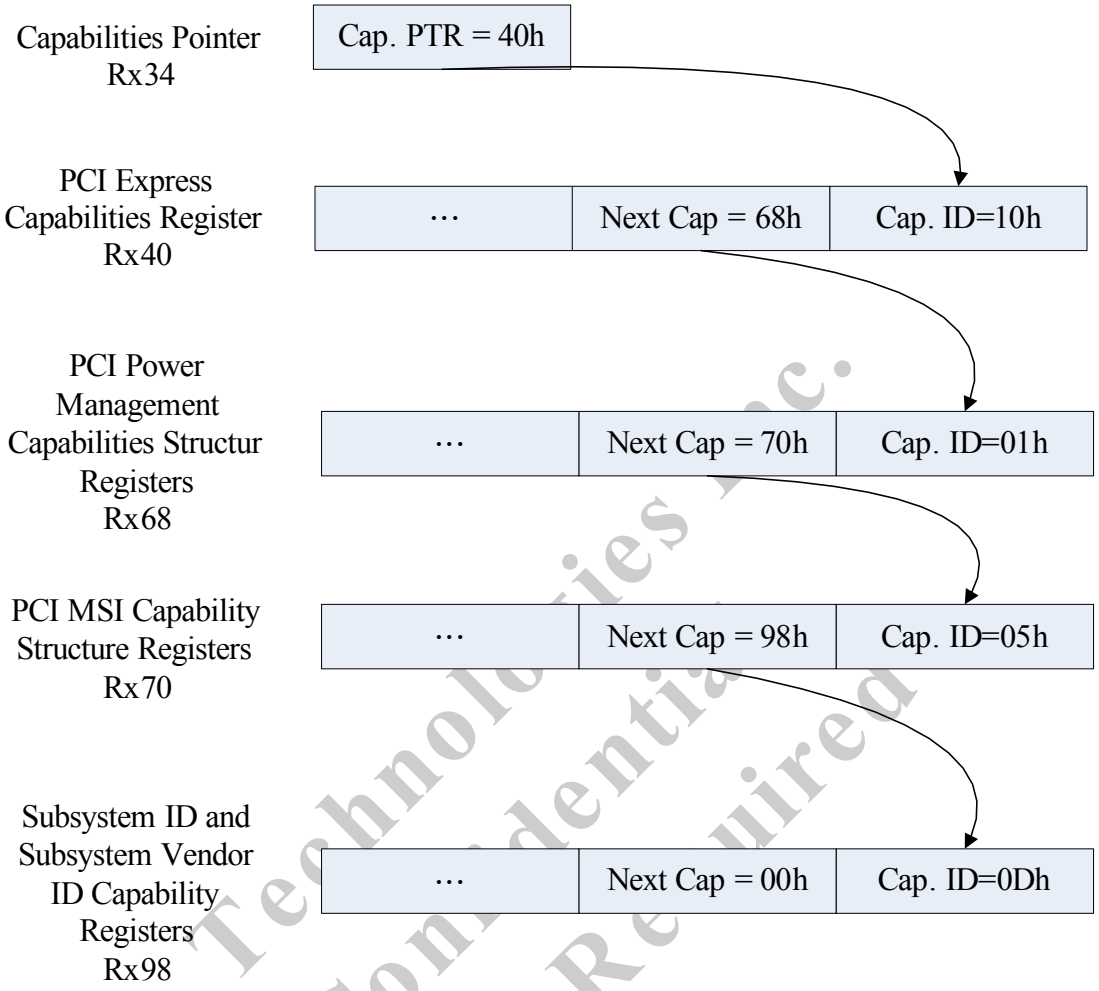
Bit	Attribute	Default	Description
15:0	RO	0	**Upper I/O Base 16 Bits Address for PCI**

Offset Address: 33-32h (D3F1)
Upper I/O Limit **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Upper I/O Limit 16 Bits Address for PCI**

Offset Address: 34h (D3F1)
Capability Pointer **Default Value: 40h**

Bit	Attribute	Default	Description
7:0	RO	40h	**Capability Pointer** This register contains the offset address from the start of the configuration space. Always reads 40h. Capability Pointer link list: Rx34 → Rx40 → Rx68 → Rx70 → Rx98 → NULL



Offset Address: 35-3Bh (D3F1) – Reserved

Offset Address: 3Ch (D3F1)

Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**INT Line** (For Software Use Only)

Offset Address: 3Dh (D3F1)

Interrupt Pin **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RO	02h	**INT Pin = INTB#**

Offset Address: 3F-3Eh (D3F1)

Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:7	RO	0	**Reserved**
6	RW	0	**Secondary Bus Reset** 0: No reset. 1: Triggers a warm reset on the corresponding PCI Express Port.
5	RO	0	**Reserved**
4	RW	0	**Base VGA 16 Bits Decode** 0: All VGA alias range will be forwarded. 1: Only forward base VGA range (Alias range will not be forwarded).
3	RW	0	**VGA Compatible I/O and Memory Address Range** 0: Do not forward VGA compatible memory and I/O. 1: Forward VGA compatible memory and I/O. Note: VGA addresses are memory A0000-BFFFFh and I/O addresses 3B0-3BBh, 3C0-3CFh and 3D0-3DFh (10-bit decode). "Mono" text mode uses B0000-B7FFFh and "Color" Text Mode uses B8000-BFFFFh. Graphics modes use Axxxxh. Mono VGA uses I/O addresses 3Bx-3Cxh and Color VGA uses 3Cx-3Dxh. If a MDA is present, a VGA will not use the 3Bxh I/O addresses and B0000-B7FFFh memory space; if not, the VGA will use those addresses to emulate MDA modes.
2	RW	0	**Block/Forward ISA I/O Cycles** 0: Forward all I/O cycles with address in the range defined by the I/O Base and I/O Limit. 1: Do not forward ISA I/O that are in the top 768 bytes of each 1K byte block address range.
1	RW	0	**SERR Enable** Controls the forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL from secondary to primary. 0: Disable 1: Enable
0	RW	0	**Parity Error Response Enable** 0: Ignore the response to poisoned TLPs. 1: Enable the response to poisoned TLPs.

PCI Express Capability Registers (40-67h)

Offset Address: 41-40h (D3F1)

PCI Express List **Default Value: 6810h**

Bit	Attribute	Default	Description
15:8	RO	68h	**Next Pointer**
7:0	RO	10h	**Capability ID** 10h indicates a PCI Express Capability Structure.

Offset Address: 43-42h (D3F1)

PCI Express Capabilities **Default Value: 0141h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RO	0	**TCS Routing Supported** 0: Not supported 1: Supported
13:9	RO	0	**Interrupt Message Number**
8	RO	1b	**Slot Implemented** This bit when set indicates that the PCI Express Link associated with this Port is connected to a slot (as compared to being connected to an integrated component or being disabled).
7:4	RO	0100b	**Device / Port Type** 0100b: Root Port of PCI Express Root Complex
3:0	RO	1h	**Capability Version**

Offset Address: 47-44h (D3F1)

Device Capabilities **Default Value: 0000 8001h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:26	RO	0	**Captured Slot Power Limit Scale** Reserved. For upstream port only.
25:18	RO	0	**Captured Slot Power Limit Value** Reserved. For upstream port only.
17:16	RO	0	**Reserved**
15	RO	1b	**Role-Based Error Reporting** 0: Role-based error reporting is not supported 1: Role-based error reporting is supported
14	RO	0	**Power Indicator Present** Reserved. For upstream port or endpoint only.
13	RO	0	**Attention Indicator Present** Reserved. For upstream port or endpoint only.
12	RO	0	**Attention Button Present** Reserved. For upstream port or endpoint only.
11:9	RO	000b	**Endpoint L1 Acceptable Latency**
8:6	RO	000b	**Endpoint L0s Acceptable Latency**
5	RO	0	**Extended Tag Field Supported** 0: 5-bit Tag field supported. 1: 8-bit Tag field supported.
4:3	RO	0	**Phantom Functions Supported** Reserved
2:0	RO	001b	**Max Payload Size Supported** 001b: 32QW (256 bytes)

Offset Address: 49-48h (D3F1)

Device Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14:12	RO	000b	**Max Read Request Size** 000b: 128 bytes This field sets the maximum Read Request size for the device as a Requestor.
11	RW	0	**Enable No Snoop** 0: Disable 1: Enable If this bit is set to 1, the device is permitted to set the No Snoop bit in the Requestor Attributes of the transactions to indicate that it does not require hardware enforced cache coherence.
10	RWS	0	**Auxiliary Power PM Enable** 0: Disable 1: Enable This bit when set enables device to draw AUX power independent of PME AUX power.
9	RO	0	**Phantom Functions Enable** Not supported.
8	RO/RW	0	**Extended Tag Field Enable** 0: Disable 1: Enable When Rx44[5] is set to 0, this bit is RO. When Rx44[5] is set to 1, this bit is RW.
7:5	RW	0	**Max Payload Size** Maximum TLP payload size.
4	RW	0	**Enable Relaxed Ordering** 0: Disable 1: Enable If this bit is set to 1, the device is permitted to set the Relaxed Ordering bit in the Requestor Attributes of the transactions to indicate that it does not require strong write ordering.
3	RW	0	**Unsupported Request Reporting Enable** 0: Disable 1: Enable
2	RW	0	**Fatal Error Reporting Enable** 0: Disable 1: Enable For a Root Port, the report of Fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	RW	0	**Non-Fatal Error Reporting Enable** 0: Disable 1: Enable For a Root Port, the report of Non-Fatal errors is internal to the root. No external ERR_NONFATAL message is generated.
0	RW	0	**Correctable Error Reporting Enable** 0: Disable 1: Enable For a Root Port, the report of correctable errors is internal to the root. No external ERR_COR message is generated.

Offset Address: 4B-4Ah (D3F1)

Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RO	0	**Transactions Pending** This bit when set indicates that the port has issued Non-Posted Requests on its own behalf (using Requestor ID of the port) which have not been completed.
4	RO	1b	**AUX Power Detected** 0: Not detected 1: Detected
3	RW1C	0	**Unsupported Request Detected** 0: Not detected 1: Detected
2	RW1C	0	**Fatal Error Detected** 0: Not detected 1: Detected
1	RW1C	0	**Non-Fatal Error Detected** 0: Not detected 1: Detected
0	RW1C	0	**Correctable Error Detected** 0: Not detected 1: Detected

Offset Address: 4F-4Ch (D3F1)

Link Capabilities **Default Value: 0318 3C11h**

Bit	Attribute	Default	Description
31:24	RO	03h	**Port Number** This field indicates the PCI Express Port number for the given PCI Express Link.
23:21	RO	0	**Reserved**
20	RO	1b	**Data Link Layer Link Active Reporting Capable** 0: Not supported 1: Supported
19	RO	1b	**Surprise Down Error Reporting Capable** This bit indicates support of detecting and reporting a Surprise Down error condition. 0: Not supported 1: Supported
18	RO	0	**Clock Power Management** 0: Not supported 1: Supported
17:15	RO	0	**L1 Exit Latency**
14:12	RO	011b	**L0s Exit Latency** 011b defines the number of FTS Order Set that is required for Design to lock symbol from RXL0S to L0.
11:10	RO	11b	**Active State Link PM (ASPM) Support** 11b means entry support of L0S and L1.
9:4	RO	000001b	**Maximum Link Width** x1 lane supported
3:0	RO	0001b	**Maximum Link Speed** 0001: 2.5G b/s Link speed

Offset Address: 51-50h (D3F1)

Link Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8	RO	0	**Enable Clock Power Management** 0: Disable 1: Enable
7	RW	0	**Extended Synch** 0: FCU Timer limit is 30us. 1: FCU Timer limit is 120us.
6	RW	0	**Common Clock Configuration** 0: Indicates that this Port and the component on the opposite end of the Link are operating with **asynchronous** reference clock. 1: Indicates that this Port and the component on the opposite end of the Link are operating with a **distributed common** reference clock.
5	RW	0	**Retrain Link** Link retrain is initiated by writing 1 to this bit. This will direct the Physical Layer LTSSM to the Recovery state.
4	RW	0	**Link Disable** 0: Enable 1: Disable This bit disables the Link when set to 1.
3	RO	0	**Read Completion Boundary** 0: 64 byte
2	RO	0	**Reserved**
1:0	RW	00b	**Active State Link PM (ASPM) Control** 00: Disable 01: Enable L0s Entry 10: Enable L1 Entry 11: Enable L0s and L1 Entry

Offset Address: 53-52h (D3F1)

Link Status **Default Value: 1nn1h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RO	0	**Data Link Layer Link Active** 0: Inactive 1: Active
12	RO	1b	**Slot Clock Configuration** 0: Use an independent clock irrespective of the presence of a reference on the connector. 1: Use the same physical reference clock that the platform provides on the connector.
11	RO	0	**Link Training** This bit indicates the Link training is in progress (Physical Layer LTSSM in Configuration or Recovery state) or the Retrain Link bit is set 1 but Link training has not yet begun. Hardware will clear this bit once Link training is complete.
10	RO	0	**Training Error** Set when a Link training error occurred. Cleared by hardware upon successful training of the Link to the L0 Link state.
9:4	RO	HwInit	**Negotiated Link Width** 000001: x1 Others: Reserved
3:0	RO	0001b	**Link Speed** 0001: 2.5Gb/s negotiated Link speed 0000b: when DLUP =0

Offset Address: 57-54h (D3F1)

Slot Capabilities **Default Value: 0000 0060h**

Bit	Attribute	Default	Description
31:19	RO	0	**Physical Slot Number** Physical slot number attached to the Port.
18	RO	0	**No Command Completed Support** 0: Not supported 1: Supported
17	RO	0	**Electromechanical Interlock Present** 0: Not presented 1: Presented
16:15	RO	0	**Slot Power Limit Scale**
14:7	RO	0	**Slot Power Limit Value** Reserved
6	RO	1b	**Hot-plug Capable** Reserved (Do not program)
5	RO	1b	**Hot-plug Surprise** Reserved (Do not program)
4	RO	0	**Power Indicator Present** Reserved
3	RO	0	**Attention Indicator Present** Reserved
2	RO	0	**MRL Sensor Present** Reserved
1	RO	0	**Power Controller Present** Reserved
0	RO	0	**Attention Button Present** Reserved

Offset Address: 59-58h (D3F1)

Slot Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved**
12	RW	0	**Enable Data Link Layer State Change Report** 0: Disable 1: Enable
11	RW	0	**Electromechanical Interlock Control** 0: Disable 1: Enable
10	RO	0	**Power Controller Control** Reserved
9:8	RW	0	**Power Indicator Control** Reserved
7:6	RW	0	**Attention Indicator Control** Reserved
5	RW	0	**Hot-Plug Interrupt Enable** Reserved
4	RW	0	**Command Completed Interrupt Enable** Reserved
3	RW	0	**Presence Detect Changed Enable** Reserved
2	RO	0	**MRL Sensor Changed Enable** Reserved 0: Disable 1: Enable
1	RO	0	**Power Fault Detected Enable** Reserved
0	RW	0	**Attention Button Pressed Enable** Reserved

Offset Address: 5B-5Ah (D3F1)

Slot Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:9	RO	0	**Reserved**
8	RW1C	0	**Data Link Layer State Changed** 0: No state changed 1: State changed
7	RO	0	**Electromechanical Interlock Status**
6	RO	0	**Card Presence State** 0: Slot empty 1: Card present in slot
5	RO	0	**MRL (Manually Operated Retention Latch) Sensor State** Reserved
4	RW1C	0	**Command Completed** 0: Not completed 1: Completed
3	RW1C	0	**Presence Detect Changed** 0: Not changed 1: Changed
2	RO	0	**MRL Sensor Changed** 0: Not changed 1: Changed
1	RO	0	**Power Fault Detected** 0: Not detected 1: Detected
0	RW1C	0	**Attention Button Pressed** 0: No state changed 1: State changed

Offset Address: 5D-5Ch (D3F1)

Root Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:5	RO	0	**Reserved**
4	RW	0	**CRS Software Visibility Enable** 0: Disable 1: Enable the Root Port to return Configuration Request Retry Status (CRS) Completion Status to software.
3	RW	0	**PME Interrupt Enable** 0: Disable 1: Enable interrupt generation upon receipt of a PME message as reflected in the PME status register bit. A PME interrupt is also generated if the PME status register bit is set when this bit is set from a cleared state.
2	RW	0	**System Error on Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Fatal Error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
1	RW	0	**System Error on Non-Fatal Error Enable** 0: Disable 1: Enable generation of a System Error if a Non-Fatal Error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.
0	RW	0	**System Error on Correctable Error Enable** 0: Disable 1: Enable generation of a System Error if a Correctable Error (ERR_COR) is reported by any of the devices in the hierarchy associated with the Root Port, or by the Root Port itself.

Offset Address: 5Eh (D3F1)

Root Capabilities Register **Default Value: 0000h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RO	0	**Capability of CRS Software Visibility** 0: Disable 1: Enable the Root Port to return CRS Completion Status to software.

Offset Address: 5Fh (D3F1) – Reserved

Offset Address: 63-60h (D3F1)

Root Status **Default Value: 000n 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	HwInit	**PME Pending** 0: No pending PME 1: Indicate that another PME is pending when the PME Status (bit 16) is set.
16	RW1C	0	**PME Status** Indicate that the PME was asserted by the Requestor ID indicated in PME Requestor ID (bit[15:0]).
15:0	RO	0	**PME Requestor ID** The Requestor ID of the last PME Requestor.

Offset Address: 64-67h (D3F1) – Reserved

PCI Power Management Capability Structure Registers (68-6Fh)

Offset Address: 6B-68h (D3F1)

Power Management Capabilities **Default Value: C822 7001h**

Bit	Attribute	Default	Description
31:27	RO	19h	**PME Support** 0: Not supported 1: Supported Bit 31, 30 and 27 are set to 1b (PME Message will be forwarded).
26	RO	0	**D2 Support** 0: Not supported 1: Supported
25	RO	0	**D1 Support** 0: Not supported 1: Supported
24:22	RO	0	**AUX Current**
21	RO	1b	**Reserved** (Do not program)
20:19	RO	0	**Reserved**
18:16	RO	010b	**Version**
15:8	RO	70h	**Next Capability Pointer**
7:0	RO	01h	**Capability ID** 01h indicates extended capability ID for the advanced error reporting capability.

Offset Address: 6F-6Ch (D3F1)

Power Management Status / Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Power Management Data**
23:16	RO	0	**Reserved**
15	RW1CS	0	**PME Status** This bit's setting is not modified by hot, warm, or cold reset.
14:9	RO	0	**Reserved**
8	RWS	0	**PME Enable** This bit's setting is not modified by hot, warm, or cold reset.
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** 00b: D0 01b: D1 10b: D2 11b: D3hot

PCI Message Signal Interrupt (MSI) Capability Structure Registers (70-87h)

Offset Address: 73-70h (D3F1)

MSI Capability Support **Default Value: 0180 9805h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24	RO	1b	**Supports Pre-vector Masking Capability** 0: Not supported 1: Supported
23	RO	1b	**Supports 64 Bit Message Address Only** 0: Not supported 1: Supported
22:20	RW	000b	**Multiple Message Enable** 000: 1 message allocated 001: 2 messages allocated 010: 4 messages allocated 011: 8 messages allocated 100: 16 messages allocated 101: 32 messages allocated 11x: Reserved
19:17	RO	000b	**Multiple Messages Capable** 000: 1 message requested 001: 2 messages requested 010: 4 messages requested 011: 8 messages requested 100: 16 messages requested 101: 32 messages requested 11x: Reserved
16	RW	0	**MSI Enable** 0: This Port is prohibited from using MSI to request service. 1: This Port is permitted to use MSI to request service.
15:8	RO	98h	**Next Capability Pointer**
7:0	RO	05h	**Capability ID** 05h indicates the extended capability ID for the root complex link declaration capability.

Offset Address: 77-74h (D3F1)

System-Specified Message Address - Low **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**System-Specified Message Address Bit [31:2]**
1:0	RO	0	**System-Specified Message Address Bit [1:0]** These bits will always read as 0.

Offset Address: 7B-78h (D3F1)

System-Specified Message Address - High **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**System-Specified Message Address Bit [63:32]**

Offset Address: 7D-7Ch (D3F1)

Message Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Message Data** The message data is to be put on data [15:0] of MSI cycles.

Offset Address: 7E-7Fh (D3F1) – Reserved

Offset Address: 83-80h (D3F1)
Message Mask Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RW	0	**Mask Bit for Message 0** 0: Not masked 1: Mask message 0

Offset Address: 87-84h (D3F1)
Message Pending Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RO	0	**Pending Bit for Message 0** 0: Not pending 1: Pending

Message Signal Interrupt (MSI) Capability Registers (88-97h)

Offset Address: 88-97h (D3F1) – Reserved

Subsystem ID and Subsystem Vendor ID Capability Registers (98-9Fh)

Offset Address: 98h (D3F1)
Capability ID **Default Value: 0Dh**

Bit	Attribute	Default	Description
7:0	RO	0Dh	**Capability ID** 0Dh is the capability ID for "Subsystem ID / Subsystem Vendor ID."

Offset Address: 99h (D3F1)
Next Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Pointer**

Offset Address: 9A-9Bh (D3F1) – Reserved

Offset Address: 9D-9Ch (D3F1)
Subsystem Vendor ID Control **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 9F-9Eh (D3F1)
Subsystem ID Control **Default Value: F353h**

Bit	Attribute	Default	Description
15:0	RO	F353h	**Subsystem ID**

PCI Express Transaction Layer Registers (A0-AFh)

Offset Address: A0h (D3F1)

Downstream Control 1 **Default Value: 11h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Cycles Have Traffic Class TC1** 0: Disable 1: Enable
6	RW	0	**Downstream Cycles Have Attribute "No Snoop" Set** 0: Disable 1: Enable
5	RW	0	**Downstream Cycles Have Attribute "Relaxed Ordering" Set** 0: Disable 1: Enable
4	RW	1b	**Downstream Lock Cycle Support** 0: Disable 1: Enable
3	RW	0	**Downstream Arbitration Scheme** 0: Fixed priority: VC1 CPL > VC0 CPL > Down Stream Command 1: Round Robin arbitration priority between VC1 CPL, VC0 CPL and Down Stream Command.
2	RW	0	**Downstream Post-Write Allowed to Pass IOW** 0: Not allowed 1: Allowed
1	RW	0	**Downstream Post-Write Allowed to Pass Read** 0: Not allowed 1: Allowed
0	RW	1b	**Downstream Pipeline** 0: Disabled 1: Enabled

Offset Address: A1h (D3F1)

Downstream Control 2 **Default Value: 14h**

Bit	Attribute	Default	Description
7	RW1C	0	**Downstream Configuration Completion Status** 0: Normal completion. 1: At least one configuration request ended with a CRS completion.
6	RW	0	**TRANS Assert Wait State Control** 0: TRANS cannot assert wait state at receiving downstream write data (original design). 1: TRANS can assert wait state at receiving downstream write data.
5	RW	0	**Data Return of Upstream Read Requests** 0: The chip always checks CPL credit unless the endpoint advertises infinite CPL credits. 1: The chip does not check CPL credit even when endpoint advertises finite CPL credits.
4	RW	1b	**Not Check Downstream PH Credit for PME_TURN_OFF Message** 0: Disable 1: Enable
3	RW	0	**Enable C2P Read Completion Timer for Vector Development Mode** 0: Disable 1: Enable When this bit is set to 1, the timer is defined in RxA1[2:0] becomes: 000: 1 us 001: 3 us 010: 10 us 011: 20 us 100: 50 us 101: 100 us 110: 200 us 111: 500 us
2:0	RW	100b	**C2P Read Completion Timeout Timer** 000: Reserved 001: 1 ms 010: Reserved 011: 10 ms (Spec. lower bound) 100: 30 ms 101: Reserved 11x: Reserved

Offset Address: A2h (D3F1)

Downstream Control 3 **Default Value: 30h**

Bit	Attribute	Default	Description
7	RW	0	**Downstream Ordering Queue Timing Option** 0: 1T setup time 1: 2T setup time
6:4	RW	011b	**Waiting Time for GNT Timer in Priority Arbitration Mode** 000: 4 ns 001: 16 ns 010: 32 ns 011: 64 ns 100: 96 ns 101: 128 ns 110: 256 ns 111: 512 ns If GNT timer of VC0 / C2P request expires, VC0 / C2P request will become higher priority. Priority VC1 > VC0 > C2P request when set RxA0[3] = 0
3	RO	0	**Reserved**
2	RW	0	**Pending C2P NP Completion Cycle to Block L1 Entry** 0: Disable. L1 entry does not wait for C2P NP completion. 1: Enable. L1 entry waits for C2P NP completion.
1:0	RW	00b	**Downstream Arbitration Parking** 00: GNT parks on the last request source. 01: GNT parks on VC1 completion. If VC1 is not enabled (or no VC1), park on VC0 completion. 10: GNT parks on VC0 completion. 11: GNT parks on C2P request.

Offset Address: A3h (D3F1)

Downstream Control 4 **Default Value: 78h**

Bit	Attribute	Default	Description
7:4	RW	0111b	**Retry Buffer Level:** 0000: 1-level 0001: 2-level 0010: 3-level 0011: 4-level 0100: 5-level 0101: 6-level 0110: 7-level 0111: 8-level Others: Reserved
3	RW	1b	**Downstream Read Retry Time Out Control in DL_Down State** 1: Enable downstream read retry time. The timer is the same as completion time out timer. After time out, this read request will not be retried again even DL_DLUp assertion occurred. 0: Disable downstream read retry time out. If RxA3[0] is set to 1, downstream read request will always wait for DL_DLUp assertion then retry.
2	RW	0	**Downstream Cycle Control / Latency Improvement** 0: Disable 1: Enable
1	RW	0	**CPL Timer Control** 0: Enable. Refer to D3F1 RxA1[2:0]. 1: Disable
0	RW	0	**Downstream Read Cycle Retry** 0: When DL_DOWN is asserted, transaction layer returns “FF” to Central Traffic Controller for C2P read cycle. 1: When DL_DOWN is asserted, transaction layer holds C2P read cycle. This incomplete C2P read cycle will be retried when DL_UP is asserted.

Offset Address: A4h (D3F1)
Upstream Control **Default Value: 1Dh**

Bit	Attribute	Default	Description
7	RW	0	**Force Upstream Address A35~A31 to 0** 0: Disable 1: Enabled for system testing or loop back mode test. The upcoming data may be checked in the system memory.
6	RO	0	**Reserved**
5	RW	0	**Upstream Check Malformed TLP through "Byte Enable Rule" and "Over 4K Boundary Rule"** 0: Disable 1: Enable
4	RW	1b	**Downstream Read Waits till the Upstream Write Data Flushed** 0: Disable 1: Enable
3	RW	1b	**CPLH, CPLD, and NPD Become Infinite Mode** 0: Disable 1: Enable
2	RW	1b	**Update Header Credit Whenever Received TLPH (including PH, NPH and CPLH** 0: Disable 1: Enable
1	RW	0	**VC1 Request Queue Usage** (when VC1 is disabled in the capability header; i.e. Rx144[0] = 0) 0: Disable 1: Enable. It allows Transaction Layer maps non-snoop upstream request through VC1 Request Queue to the Central Traffic Controller (Note: When this bit is 1, bit-0 must be 0).
0	RW	1b	**Disable Virtual Channel 1 Support** 0: Enable VC1, data FIFO of VC1 is used by VC1. 1: Disable VC1, data FIFO of VC1 is reallocated to VC0, which doubles the size of VC0 data FIFO.

Offset Address: A5h (D3F1)
Credit Advertisement Control 1 **Default Value: FFh**

Bit	Attribute	Default	Description
7:4	RW	1111b	**Upstream Posted (write) Data FIFO Size, and the Initial PD Credit Value** 0000: 1-line upstream write FIFO size, and initial PD credit = 4h 0001: 2-line upstream write FIFO size, and initial PD credit = 8h 0010: 3-line upstream write FIFO size, and initial PD credit = Ch 0011: 4-line upstream write FIFO size, and initial PD credit = 10h 0100: 5-line upstream write FIFO size, and initial PD credit = 14h 0101: 6-line upstream write FIFO size, and initial PD credit = 18h 0110: 7-line upstream write FIFO size, and initial PD credit = 1Ch 0111: 8-line upstream write FIFO size, and initial PD credit = 20h 1xxx: 8-line upstream write FIFO size, and initial PD credit =20h
3:0	RW	1111b	**Upstream PH Header Queue Size, and the Initial PH Credit** 0000: 1-level PH header queue, and initial PH credit = 2h 0001: 2-level PH header queue, and initial PH credit = 4h 0010: 4-level PH header queue, and initial PH credit = 6h 0011: 8-level PH header queue, and initial PH credit = 8h 01xx: 8-level PH header queue, and initial PH credit = 8h 1xxx: 8-level PH header queue, and initial PH credit = 8h

Offset Address: A6h (D3F1)
Credit Advertisement Control 2 **Default Value: 7Fh**

Bit	Attribute	Default	Description
7	RW	0	**Upstream Non-Posted Header Credit Infinite Mode Control** 0: The non-posted header credit is finite and has to update NPH credits. 1: The non-posted header credit is infinite and not necessary to update NPH credits.
6:4	RW	111b	**Upstream Read CPL Header Size** 0xx: 32QW 4-level 1xx: 32QW 4-level
3:0	RW	1111b	**Upstream Non-Posted Request Queue Size, and Initial NPH Credit Value** 0000: 1-level NPH header queue, and initial NPH credit = 2h 0001: 2-level NPH header queue, and initial NPH credit = 4h 0010: 4-level NPH header queue, and initial NPH credit = 6h 0011: 8-level NPH header queue, and initial NPH credit = 8h 01xx: 8-level NPH header queue, and initial NPH credit = 8h 1xxx: 8-level NPH header queue, and initial NPH credit = 8h

Offset Address: A8-A7h (D3F1)
Upstream Performance Control **Default Value: 01C4h**

Bit	Attribute	Default	Description
15	RW	0	**C2P Completion Timeout Method when PHY Retrains or Re-configures** 0: Keep the timeout value 1: Reset the timeout value
14	RO	0	**Reserved**
13:12	RW	0	**Configuration request timeout timer** 00: 100 ms 01: 500 ms 10: 1000 ms 11: 1500 ms
11:10	RO	0	**Reserved**
9:8	RW	01b	**Downstream Configuration Retry Request Timing after Receiving CRS Completion** 00: Assert 1T after CRS is received 01: Assert 4T after CRS is received 10: Assert 8T after CRS is received 11: Assert 16T after CRS is received
7:6	RW	11b	**Control the Maximum Number of Outstanding Expected WPOP Issued** 00: TRANS accepts 48 outstanding expected WPOP 01: TRANS accepts 56 outstanding expected WPOP 10: TRANS accepts 64 outstanding expected WPOP 11: No constraint on consecutive WPOP
5	RW	0	**Enable Transaction Layer Header Queue Pre-load Design Dynamic Clock for Power Management** 1: Enable 0: Disable.
4	RW	0	**Upstream Read FIFO Entry Release Timing Control** 0: Upstream read FIFO entry release when the last data pops into retry data FIFO. 1: Upstream read FIFO entry release when the first data pops into retry data FIFO
3	RW	0	**Downstream Read Data Waits for Previous Upstream Write Complete** 0: Disable 1: Enable
2	RW	1b	**Upstream Requests Read and Write Orders** 0: Upstream requests are served in order. 1: Upstream write always passes upstream read.
1	RW	0	**Upstream Read Data TLP Return Policy** 0: One upstream request with over 16DW length or non-8-QW boundary alignment must be split into multiple CPL TLPs. 1: Multiple CPL TLPs belong to the same upstream request can be merged into one single CPL TLP.
0	RO	0	**Upstream Write Cycle will be 4QW Align** 0: Disable 1: Enable

Offset Address: A9h (D3F1)
CRS Retry Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Enable of CRS Retry Mechanism** 0: No retry cycle for CRS, regardless of Rx5C[4] setting and return 'hffffffff for read cycles. 1: Follow Rx5C[4] setting.

Offset Address: AAh (D3F1)
Upstream Read Timing Option **Default Value: 10h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	1b	**UpdateFC-P Generation to The Endpoint for Upstream Write TLPs** 0: UpdateFC-P is generated only when PD update is requested 1: UpdateFC-P is generated when PH or PD update is requested
3:1	RO	0	**Reserved**
0	RW	0	**Upstream Read Timing Option** 0: Fast timing, better read performance 1: Moderate timing, medium read performance

Offset Address: AB-AFh (D3F1) – Reserved

PCI Express Data Link Layer Registers (B0-BFh)

Offset Address: B0h-B1h (D2F0) – Reserved

Offset Address: B2h (D3F1)

Flow Control Initialization / Flow Control Unit and Status **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW1C	0	**FCI / FCU Timeout Status** 0: No time out 1 The FCI / FCU timeout has occurred.
6	RW	1b	**FCI / FCU Receive Timer Enable Control** 0: Disable the timeout mechanism 1: Enable the timeout mechanism
5	RW	0	**FCI / FCU Receive Timer Limit** 0: Timeout limit of 200 us 1: Timeout limit of 300 us
4	RW	0	**FCI / FCU Receive Timer Reset Control** 0: Timer reset by FCI / FCU only 1: Timer reset by any received DLLPs
3:0	RO	0	**Reserved**

Offset Address: B3h (D3F1)

Replay Timer Control **Default Value: 81h**

Bit	Attribute	Default	Description
7:6	RW	10b	**Replay Timer Control While Rewinding** (resend those DLLPs which do not have corresponded ACK / NAK received) 00: Hold Replay Timer during rewinding. 01: During rewinding, if ACK / NAK comes in, reset and hold the Replay Timer. 10: During rewinding, reset and hold the Replay Timer as long as the Retry Buffer is empty. 11: Reserved.
5:3	RO	0	**Reserved**
2:0	RW	001b	**Count of Replay Timer Expired During RXL0s (Receiving Physical in L0s State) Before Resend the TLP** **When Rx50[7] is set to 0:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 1x Replay timer expired 010: Resend the TLP after 2x Replay timer expired 011: Resend the TLP after 4x Replay timer expired 100: Resend the TLP after 8x Replay timer expired 101: Resend the TLP after 16x Replay timer expired 110: Resend the TLP after 32x Replay timer expired 111: Resend the TLP after 64x Replay timer expired **When RX50[7] is set to 1:** 000: Wait forever for the Acknowledge from the device side 001: Resend the TLP after 16 x Replay timer expired 010: Resend the TLP after 32 x Replay timer expired 011: Resend the TLP after 64 x Replay timer expired 100: Resend the TLP after 128 x Replay timer expired 101: Resend the TLP after 256 x Replay timer expired 110: Resend the TLP after 512 x Replay timer expired 111: Resend the TLP after 1024 x Replay timer expired

Offset Address: B4h (D3F1)
Arbitration Control **Default Value: 05h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**TLP Flow Control Initialization for VC0 in Arbitration** 0: TLP is not allowed to pass Flow Control Initialization 2 (FCI2) for VC0. 1: TLP is allowed to pass Flow Control Initialization 2 (FCI2) for VC0.
2:0	RW	101b	**Data Link TX Packets Arbitration Scheme** 000: Round Robin 001: Reserved 010: Strict priority: TLP > ACK/NAK > FCU 011: Strict priority: TLP > FCU > ACK/NAK 100: Strict priority: ACK / NAK > TLP > FCU 101: Strict priority: ACK / NAK > FCU > TLP 110: Strict priority: FCU > TLP > ACK/NAK 111: Strict priority: FCU > ACK / NAK > TLP

Offset Address: B5h (D3F1)
FCU Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**FCU Timer Control** 0: Update flow control credit when either Transaction Layer requested packets being sent or when FCU timer expired. 1: Update flow control credit only when FCU timer expired.
5:4	RW	00b	**ACK DLLP Collapse Method** 00: Send ACK when the latency timer expired 01: Send ACK every 4 correct TLPs have been received 10: Send ACK every 8 correct TLPs have been received 11: Send ACK every 16 correct TLPs have been received
3:2	RO	0	**Reserved**
1	RW	0	**FCI (Flow Control Initialization) Process End Condition** 0: Complete FCI process when TLP / FCU has been received. 1: Do not complete FCI process even when TLP / FCU has been received.
0	RW	0	**VC1 FCI DLLP Transmission Scheme** 0: Transmit FCI DLLP (Data Link Layer Packet) only when FCI timer expired. 1: Transmit FCI DLLP continuously as long as the FCI process is not finished.

Offset Address: B6h (D3F1)
Transaction / Link Layer Checking Control **Default Value: A1h**

Bit	Attribute	Default	Description
7	RW	1b	**Nak_Scheduled Flag Control** Nak_Scheduled Flag is set after a Nak is scheduled by receiving a TLP with CRC or Seq_Num ERROR, and Nak_Scheduled Flag is cleared after receiving a new Ack. 0: Disable Nak_Scheduled Flag. Schedule Nak regardless of Nak_Scheduled Flag. 1: Enable Nak_Scheduled Flag. Nak can only be scheduled when Nak_Scheduled Flag is cleared.
6:5	RW	01b	**TLP Receiving Timer** When timeout, reset error-framing byte-counter. 00: Reset byte-counter 1 us after TLP header received. 01: Reset byte-counter 2 us after TLP header received. 10: Reset byte-counter 3 us after TLP header received. 11: Reset byte-counter 4 us after TLP header received.
4	RW	0	**The First Downstream TLP is Popped out from TL 1T Earlier**
3:1	RO	0	**Reserved**
0	RW	1b	**LCRC Check Control** 0: Do not check LCRC. 1: Check LCRC.

Offset Address: B7h (D3F1) – Reserved

Offset Address: B8h (D3F1)
Data Link Layer Header Position **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Data Link Layer Header Position** 0: SDP (Start DLLP) can be in Lane 0 / 4 / 8 / 12. 1: SDP (Start DLLP) is always at Lane 0.

Offset Address: B9h (D3F1) – Reserved

Offset Address: BAh (D3F1)
ACK / NAK Latency Timer Limit 1 **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:0	RW	0Ch	**ACK / NAK Latency Timer in Large LSNLW Setting** This timer is used for AckNak_latency_timer when LSNLW (Link Status Register-Negotiation Link Width) is x16. 00h: 4 x 1 Clocks (Clock = 250 Mhz) 01h: 4 x 2 Clocks 02h: 4 x 3 Clocks ….. FFh: 4 x 256 Clocks

Offset Address: BBh (D3F1)
ACK / NAK Latency Timer Limit 2 **Default Value: 12h**

Bit	Attribute	Default	Description
7:0	RW	12h	**ACK / NAK Latency Timer in Medium LSNLW Setting** This timer is used for AckNak_latency_timer when LSNLW is x8 / x4. 00h: 4 x 1 Clocks (Clock = 250Mhz) 01h: 4 x 2 Clocks 02h: 4 x 3 Clocks. ….. FFh: 4 x 256 Clocks

Offset Address: BCh (D3F1)
ACK / NAK Latency Timer Limit 3 **Default Value: 3Bh**

Bit	Attribute	Default	Description
7:0	RW	3Bh	**ACK / NAK Latency Timer in Small LSNLW Setting** This timer is used for AckNak_latency_timer when LSNLW is x2 / x1. 00h: 4 x 1 Clocks (Clock =250Mhz) 01h: 4 x 2 Clocks 02h: 4 x 3 Clocks ….. FFh: 4 x 256 Clocks

Offset Address: BDh (D3F1)
Replay Timer Limit 1 **Default Value: 12h**

Bit	Attribute	Default	Description
7:0	RW	12h	**Replay_timer_limit in Large LSNLW Setting** This timer is used for Replay_timer when LSNLW is x16. 00h: 8 x 1 Clocks (Clock = 250Mhz) 01h: 8 x 2 Clocks 02h: 8 x 3 Clocks ……. FFh: 8 x 256 Clocks

Offset Address: BEh (D3F1)
Replay Timer Limit 2 **Default Value: 1Bh**

Bit	Attribute	Default	Description
7:0	RW	1Bh	**Replay_timer_limit in Medium LSNLW Setting** This timer is used for Replay_timer when LSNLW is x8 / x4. 00h: 8 x 1 Clocks (Clock =250Mhz) 01h: 8 x 2 Clocks 02h: 8 x 3 Clocks ……. FFh: 8 x 256 Clocks

Offset Address: BFh (D3F1)
Replay Timer Limit 3 **Default Value:58h**

Bit	Attribute	Default	Description
7:0	RW	58h	**Replay_timer_limit in Small LSNLW Setting** This timer is used for Replay_timer when LSNLW is x2 / x1 00h: 8 x 1 Clocks (Clock =250Mhz) 01h: 8 x 2 Clocks 02h: 8 x 3 Clocks ……. FFh: 8 x 256 Clocks

PCI Express Physical Layer Registers (C0-CFh)

Offset Address: C0h (D3F1)

PHY General Control **Default Value: 03h**

Bit	Attribute	Default	Description
7	RW	0	**Quick Timeout Counter Setting** When set to 1, PHY timeout period will be shorter as below: 2 ms → 4 us 12 ms → 24 us 24 ms → 48 us 48 ms → 96 us 1024 ts → 32 ts Receiver Detection: 15x1024 ns → 1x1024 ns
6	RW	0	**Disable Data Scrambling / Descrambling** 0: Enable 1: Disable
5:3	RW	000b	**Loopback Mode Selection** 000: No loop back 001: PHYLS loopback from TX end to RX end 010: PHYES loopback from TX end to RX end 011: External loopback from TX end to RX end 100: Reserved 101: PHYLS loopback from RX end to TX end 110: PHYES loopback from RX end to TX end 111: Reserved See the figure below for details.
2:0	RW	011b	**COMMA Detection Window** 000 / 001: Illegal values. Others: Delay number of T to determine correct lane-to-lane deskew value.

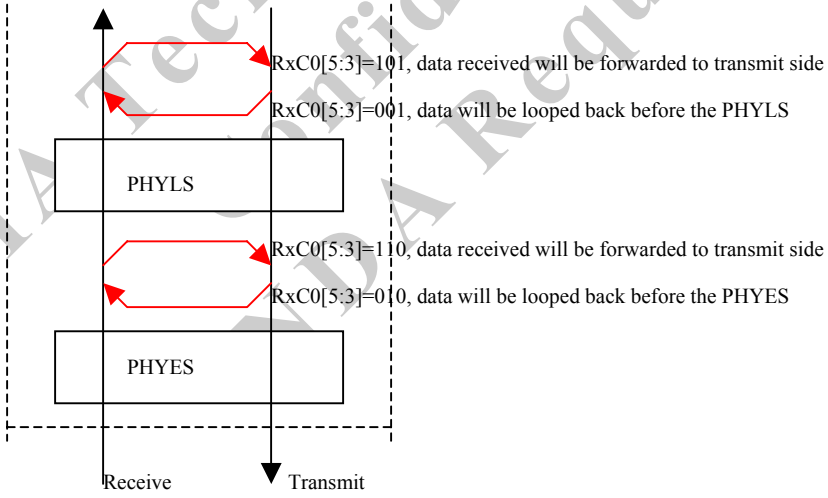


Figure 4. Loop Back Mode Selections

Offset Address: C1h (D3F1)
PHYLS General Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Enable Aggressive Power Management when No Device Plug** 0: Disable 1: Enable
5	RW	0	**Enable Aggressive Power Management in Rx Path to Data Link Layer Module** 0: Disable 1: Enable
4:0	RW	00000b	**PHY Lane Configuration Setting** 00000: Use PHY negotiation 00001: x1 with normal connection 10101: Force into L0s state (for testing and measurement used only) 11000: Force into DETECT_QUIET state (for testing measurement used only) 11001: Force into DETECT_ACTIVE state (for testing measurement used only) Other values are not allowed.

Offset Address: C2h (D3F1)
PHYLS MAC and PCS **Default Value: 27h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Reset Elastic Buffer** Always reads 0.
5	RW	1b	**Lane Enable** 0: Enable lanes based on LTSSM negotiation results. 1: Enable lanes based on receiver detection's results.
4	RW	0	**Bypass PHYES Device Detection in Detect Phase of LTSSM** 0: Enable PHYES to actually perform receiver detection in Detect phase. 1: Bypass receiver detection, and assume device exists. Usually, only set to "1" for testing or debugging.
3	RO	0	**Reserved**
2	RW	1b	**Wait IDL Ordered Set or Electrical Idle When L1 / L23 Entry** 0: Always wait IDL ordered set for L1 / L23 entry. 1: Wait Electrical Idle and ignore IDL ordered set for L1 / L23 entry.
1	RW	1b	**Disparity Check Enable** 0: Disable 1: Enable
0	RW	1b	**State Machine LTSSM (Link Training and Status State Machine) Control** 0: Wait for the electrical idle signal from the PHYES or wait 12 ms after LTSSM enters Detect.Quiet state. 1: Always wait for 12ms after LTSSM enters Detect.Quiet state.

Offset Address: C3h (D3F1)

PHYLS LTSSM State **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**PHYLS LTSSM State** See the table below

Table 18. Mapping Table for D3F1 RxC3

LTSSM States	Binary Coding (RxC3)	Hexadecimal Coding
DETECT_QUIET	8'B0000_0000	8'H00
DETECT_ACTIVE	8'B0000_0001	8'H01
POLLING_ACTIVE	8'B0001_0000	8'H10
POLLING_CONFIGURATION	8'B0001_0001	8'H11
POLLING_SPEED	8'B0001_0010	8'H12
POLLING_COMPLIANCE	8'B0001_0100	8'H14
CONFIGURATION_RCVRCFG_STEP_1	8'B0010_0001	8'H21
CONFIGURATION_RCVRCFG_STEP_2	8'B0010_0010	8'H22
CONFIGURATION_RCVRCFG_STEP_3	8'B0010_0011	8'H23
CONFIGURATION_RCVRCFG_STEP_4	8'B0010_0100	8'H24
CONFIGURATION_RCVRCFG_STEP_5	8'B0010_0101	8'H25
CONFIGURATION_RCVRCFG_STEP_6	8'B0010_0110	8'H26
CONFIGURATION_RCVRCFG_STEP_7	8'B0010_0111	8'H27
CONFIGURATION_IDLE	8'B0010_1000	8'H28
RECOVERY_RCVRLOCK	8'B0011_0000	8'H30
RECOVERY_RCVRCFG	8'B0011_0001	8'H31
RECOVERY_IDLE	8'B0011_0011	8'H33
LOOPBACK_MSTR_ENTRY	8'B0100_0000	8'H40
LOOPBACK_MSTR_ACTIVE	8'B0100_0001	8'H41
LOOPBACK_MSTR_EXIT	8'B0100_0011	8'H43
LOOPBACK_SLAV_ENTRY	8'B0100_0100	8'H44
LOOPBACK_SLAV_ACTIVE	8'B0100_0101	8'H45
LOOPBACK_SLAV_EXIT	8'B0100_0111	8'H47
DISABLED_ENTRY	8'B0101_0000	8'H50
DISABLED_DISABLED	8'B0101_0001	8'H51
HOTRESET_ACTIVE	8'B0110_0000	8'H60
L0L0_TXL0_RXL0	8'B1000_1010	8'H8A
L0L0S_TXL0_RXENTRY	8'B1001_1000	8'H98
L0L0S_TXL0_RXIDLE	8'B1001_1001	8'H99
L0L0S_TXL0_RXFTS	8'B1001_1011	8'H9B
L0SL0_TXENTRY_RXL0	8'B1010_0010	8'HA2
L0SL0_TXIDLE_RXL0	8'B1010_0110	8'HA6
L0SL0_TXFTS_RXL0	8'B1010_1110	8'HAE
L0SL0S_TXENTRY_RXENTRY	8'B1011_0000	8'HB0
L0SL0S_TXENTRY_RXIDLE	8'B1011_0001	8'HB1
L0SL0S_TXENTRY_RXFTS	8'B1011_0011	8'HB3
L0SL0S_TXIDLE_RXENTRY	8'B1011_0100	8'HB4
L0SL0S_TXIDLE_RXIDLE	8'B1011_0101	8'HB5
L0SL0S_TXIDLE_RXFTS	8'B1011_0111	8'HB7
L0SL0S_TXFTS_RXENTRY	8'B1011_1100	8'HBC
L0SL0S_TXFTS_RXIDLE	8'B1011_1101	8'HBD
L0SL0S_TXFTS_RXFTS	8'B1011_1111	8'HBF
L1_ENTRY	8'B1100_0000	8'HC0
L1_IDLE	8'B1100_0001	8'HC1
L23READY_ENTRY	8'B1101_0000	8'HD0
L23READY_IDLE	8'B1101_0001	8'HD1

Offset Address: C4h (D3F1)
Elastic Buffer Base Registers for Lane 0 to 1 **Default Value: 04h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	4h	**Elastic Buffer Base Register for Lane 0** 0, 1, 7: Illegal values. Others: Delay numbers of T for elastic buffer operations.

Offset Address: C5-CCh (D3F1) – Reserved

Offset Address: CDh (D3F1)
PHYLS MAC **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Downstream Tx Arbitration between DLLM and PHYLS** 0: Normal arbitration 1: Arbitration with lower latency

Offset Address: CEh (D3F1) – Reserved

Offset Address: CFh (D3F1)
SKP Ordered Set Control **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Enable PHYES Level-2 Power Down** 0: Disable 1: Enable
3:2	RO	11b	**Reserved** (Do not program)
1:0	RW	00b	**SKP Order-set Scheduling Time** 00: Send out "SKP" Order-set on the PCIe bus every 1180 symbol time, it is around 4.72us. 01: Send out "SKP" Order-set on the PCIe bus every 118 symbol time, it is around 472ns. 10: Send out "SKP" Order-set on the PCIe bus every 6.12 us. 11: Reserved

PCI Express Power Management Module Registers (D0-D3h)

Offset Address: D0h (D3F1)

Power Management Controller PHYLS Control **Default Value: 50h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	101b	**Timeout Period** This timer is used when waiting for ACK from a device after issued PME_TURNOFF message to notify the device to move to power down mode. 000: 1 us 001: 2 us 010: 4 us 011: 8 us 100: 16 us 101: 32 us 110: 64 us 111: 128 us
3	RO	0	**Reserved**
2	RW	0	**Retrain Link when Bad DLLP is Checked** 0: Disable 1: Enable
1	RW	0	**Link Loopback** 0: Normal operation 1: Direct device to enter Loopback mode. Received data in the device will be sent to the transmit side.
0	RW	0	**Link Reconfigure Linkwidth** 0: When reconfigure linkwidth, LTSSM must be Detect state. 1: When reconfigure linkwidth, LTSSM can go to Configuration state.

Offset Address: D1h (D3F1)

PMU (Power Management Unit) Timeout **Default Value: 20h**

Bit	Attribute	Default	Description
7	RW1C	0	**Error Status Report** This bit is set when device cannot have electrical idle after the waiting period programmed at RxD1[5:4] expired.
6	RO	0	**Reserved**
5:4	RW	10b	**Electrical Idle Waiting Period before Move to L1 State** (after issue ACK to the L1 request from the device) 00: Always wait for electrical idle 01: Wait 32 clock 10: Wait 64 clock 11: Reserved
3:2	RO	0	**Reserved**
1:0	RW	00b	**Downstream Cycles Triggered C2P Cycles** Period of staying at L0 before returned to L1 for PHY (when PMU is not in D0 state). 00: Immediately 01: 1 cfgW or message + delay 10T 10: 1 32QW + 1 cfgW or message + delay 10T 11: 2 32QW + 1 cfgW or message + delay 10T

Offset Address: D2h (D3F1)

PMU L0s Idle Timeout **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Idle Period to Enter L0s** Minimum time period is 128ns (RxD2 = 00). 00h: 128 ns 01h: 2x128 ns 02h: 3x128 ns … FFh: 256x128 ns

Offset Address: D3h (D3F1)
PMU L1 Idle Timeout **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Idle Period to Enter ASL1** Minimum time period is 128 ns. 00h: 128 ns 01h: 2x128 ns 02h: 3x128 ns … FFh: 256x128 ns

Offset Address: D4-D7h (D3F1) – Reserved

PCI Express Message Controller Related Registers (D8-DFh)

Offset Address: D8h (D3F1)
Power Management Controller Express Message Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Excessive Errors Occurred But Not Reported in MSGC** 0: Normal operation. 1: There are errors not reported to the system.
6:0	RO	0	**Reserved**

Offset Address: D9-DFh (D3F1) – Reserved

PCI Express Electrical PHY Registers (E0-EFh)

Offset Address: E0h (D3F1) – Reserved

Offset Address: E1h (D3F1)

1 Lane Related Control of PHYES Module **Default Value: 08h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Receiving Polarity Change Control** 0: Have the same polarity on the loop-back / received data. 1: Have reverse polarity on the loop-back / received data.
3:2	RW	10b	**Squelch Window Select (64~175 mv) – For PE1**
1	RW	0	**Number of Non Idle Signal Detected Before Exit Idle State** (Electrical Idle State Exit Condition) 0: 10 bits 1: 2 bits
0	RW	0	**Number of Idle Signal Detected Before Enter Idle State** (Electrical Idle State Enter Condition) 0: 10 bits 1: 2 bits

Offset Address: E2-EFh (D3F1) – Reserved

PCI Express Electrical PHY Test Registers (F0-FFh)

Offset Address: F1h (D3F1)

Repeated Count of the Test Pattern **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Repeated Count of the Test Pattern** (as selected in RxF2[7:4]) When using loopback mode to test electrical PHY, the following should be satisfied: RxF1 x 8 > loopback latency / 4 ns. 00-0Bh: Illegal value 0Ch: Test pattern repeats 12 times 0Dh: Test pattern repeats 13 times … FFh: Test pattern repeats 255 times

Offset Address: F2h (D3F1)

Test Pattern Selection **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Select Test Pattern** 0000: SKP order-set 0001: User define, use RxF6[9:0] 0010: K28.5 test bit sequence 0011: K28.7 test bit sequence 0100: K test for differential pair current 0101: J test for differential pair current 0110: D21.5 test bit sequence 0111: D30.3 test bit sequence 1000: Ten contiguous run of 3 test bit sequence 1001: Low transition density test bit sequence 1010: Half-rate/quarter-rate test bit sequence 1011: Low frequency spectral test bit sequence 1100: Simultaneous switching test bit sequence 1101: D 10.2 test bit sequence 1110: D 24.3 test bit sequence 1111: Compliance test bit sequence
3:0	RO	0	**Reserved**

Offset Address: F3h (D3F1)

Test Mode Control **Default Value: 06h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Electrical PHY Test Mode** Program this bit to 1 to start Electrical PHY test. 0: Disable 1: Enable
6:4	RO	0	**Reserved**
3:0	RW	6h	**Test Pattern Check Length** Number of T when the receiving side starts to check transmitted and received patterns. Suggested Value Settings: (Lane 0 for example) RxC0[5:3] = 001b: RxC4[2:0] + 2 RxC0[5:3] = 010b: RxC4[2:0] + 2 + (Loopback Path Latency / 4 ns)+1

Offset Address: F5-F4h (D3F1)
BIST Status 1 **Default Value: 00h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9:0	RO	0	**Received Symbol** (When RxF3[7] is set 1) 10b'0: When RxF3[7] is 0.

Offset Address: F7-F6h (D3F1)
BIST Status 2 **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Electrical PHY Test Error** 0: No error detected 1: Indicates that there is an error detected in the receiving side during the loop back test mode.
14	RO	0	**Electrical PHY Built-In Self Test Error of Symbol Comparison** 0: No error detected 1: Indicates that some errors detected or COMMA symbols are never detected during PHYBIST period; reported from PTNCMP.
13:10	RO	0	**Reserved**
9:0	RW	0	**Transmitted Symbol** (When RxF3[7] is set to 1) 10b'0: When RxF3[7] is set to 0.

Offset Address: F9-F8h (D3F1)
PHY BIST Counter Test Mode **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0000h	**PHY BIST Period for Electrical PHY Test Error**

Offset Address: FA-FFh (D3F1) – Reserved

Device 3 Function 1 (D3F1) – PCI Express Root Port 1 Extended Space

Registers defined in the Extended Space can be accessed through PCI Express Enhanced Configuration Access Mechanism, which utilizes a flat memory-mapped address space to access the configuration registers. Please check PCI Express Specification for the detail information.

Advanced Error Reporting Capability (100-13Fh)

Offset Address: 103-100h (D3F1)

Advance Error Reporting Enhanced Capability Header **Default Value: 1401 0001h**

Bit	Attribute	Default	Description
31:20	RO	140h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0001h	**PCI Express Extended Capability ID**

Offset Address: 107-104h (D3F1)

Uncorrectable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20	RW1CS	0	**Unsupported Request Error Status (TL)**
19	RW1CS	0	**ECRC Error Status (TL)**
18	RW1CS	0	**Malformed TLP Status (TL)**
17	RW1CS	0	**Receiver Overflow Status (TL)**
16	RW1CS	0	**Unexpected Completion Status (TL)**
15	RW1CS	0	**Completer Abort Status (TL)**
14	RW1CS	0	**Completion Timeout Status (TL)**
13	RO	0	**Flow Control Protocol Error Status (TL)**
12	RW1CS	0	**Poisoned TLP Status (TL)**
11:6	RO	0	**Reserved**
5	RW1CS	0	**Surprise Down Error Status**
4	RW1CS	0	**Data Link Protocol Error Status (DLL)**
3:1	RO	0	**Reserved**
0	RW1CS	0	**Training Error Status (PHY)**

Offset Address: 10B-108h (D3F1)

Uncorrectable Error Mask **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:21	RO	0	**Reserved**
20	RWS	0	**Unsupported Request Error Mask (TL)**
19	RWS	0	**ECRC Error Mask (TL)**
18	RWS	0	**Malformed TLP Mask (TL)**
17	RWS	0	**Receiver Overflow Mask (TL)**
16	RWS	0	**Unexpected Completion Mask (TL)**
15	RWS	0	**Completed Abort Mask (TL)**
14	RWS	0	**Completion Timeout Mask (TL)**
13	RWS	0	**Flow Control Protocol Error Mask (TL)**
12	RWS	0	**Poisoned TLP Mask (TL)**
11:6	RO	0	**Reserved**
5	RWS	0	**Surprise Down Error Mask**
4	RWS	0	**Data Link Protocol Error Mask (DLL)**
3:1	RO	0	**Reserved**
0	RWS	0	**Training Error Mask (PHY)**

Offset Address: 10F-10Ch (D3F1)

Uncorrectable Error Severity **Default Value: 0006 2031h**

Bit	Attribute	Default	Description
31:21	RO	0	Reserved
20	RWS	0	Unsupported Request Error Severity (TL)
19	RWS	0	ECRC Error Severity (TL)
18	RWS	1b	Malformed TLP Severity (TL)
17	RWS	1b	Receiver Overflow Error Severity (TL)
16	RWS	0	Unexpected Completion Error Severity (TL)
15	RWS	0	Completed Abort Error Severity (TL)
14	RWS	0	Completion Timeout Error Severity (TL)
13	RWS	1b	Flow Control Protocol Error Severity (TL)
12	RWS	0	Poisoned TLP Severity (TL)
11:6	RO	0	Reserved
5	RWS	1b	Surprise Down Error Severity
4	RWS	1b	Data Link Protocol Error Severity (DLL)
3:1	RO	0	Reserved
0	RWS	1b	Training Error Severity (PHY)

Offset Address: 113-110h (D3F1)

Correctable Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13	RW1CS	0	Advisory Non-Fatal Error Status
12	RW1CS	0	Replay Timer Timeout Status (DLL)
11:9	RO	0	Reserved
8	RW1CS	0	REPLAY_NUM Rollover Status (DLL)
7	RW1CS	0	Bad DLLP Status (DLL)
6	RW1CS	0	Bad TLP Status (DLL)
5:1	RO	0	Reserved
0	RW1CS	0	Receiver Error Status (PHY)

Offset Address: 117-114h (D3F1)

Correctable Error Mask **Default Value: 0000 2000h**

Bit	Attribute	Default	Description
31:14	RO	0	Reserved
13	RWS	1b	Advisory Non-Fatal Error Mask
12	RWS	0	Replay Timer Timeout Mask (DLL)
11:9	RO	0	Reserved
8	RWS	0	REPLAY_NUM Rollover Mask (DLL)
7	RWS	0	Bad DLLP Mask (DLL)
6	RWS	0	Bad TLP Mask (DLL)
5:1	RO	0	Reserved
0	RWS	0	Receiver Error Mask (PHY)

Offset Address: 11B-118h (D3F1)

Advanced Error Capabilities and Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:9	RO	0	Reserved
8	RWS	0	ECRC Check Enable (TL)
7	RO	0	ECRC Check Capable (TL)
6	RWS	0	ECRC Generation Enable (TL)
5	RO	0	ECRC Generation Capable (TL)
4:0	ROS	0	First Error Pointer (TL)

Offset Address: 11F-11Ch (D3F1)
Header Log (TL) Register 1st DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 1st DW**

Offset Address: 123-120h (D3F1)
Header Log (TL) Register 2nd DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 2nd DW**

Offset Address: 127-124h (D3F1)
Header Log (TL) Register 3rd DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 3rd DW**

Offset Address: 12B-128h (D3F1)
Header Log (TL) Register 4th DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	ROS	0	**Header Log Register 4th DW**

Offset Address: 12F-12Ch (D3F1)
Root Error Command **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:3	RO	0	**Reserved**
2	RW	0	**Fatal Error Reporting Enable**
1	RW	0	**Non-Fatal Error Reporting Enable**
0	RW	0	**Correctable Error Reporting Enable**

Offset Address: 133-130h (D3F1)
Root Error Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:27	RO	00h	**Advanced Error Interrupt Message Number (TL)**
26:7	RO	0	**Reserved**
6	RW1CS	0	**Fatal Error Messages Received (TL)**
5	RW1CS	0	**Non-Fatal Error Messages Received (TL)**
4	RW1CS	0	**First Uncorrectable Fatal Error Message Received (TL)** Set to 1 when the first Uncorrectable Error Message received is for a Fatal Error.
3	RW1CS	0	**Multiple ERR_FATAL/NONFATAL Received (TL)**
2	RW1CS	0	**ERR_FATAL / NONFATAL Received (TL)**
1	RW1CS	0	**Multiple ERR_COR Received (TL)**
0	RW1CS	0	**ERR_COR Received (TL)**

Offset Address: 137-134h (D3F1)
Error Source Identification **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	ROS	0	**ERR_FATAL/NONFATAL Source Identification (TL)**
15:0	ROS	0	**ERR_COR Source Identification (TL)**

Offset Address: 138-13Fh (D3F1) – Reserved

Virtual Channel Capability (140-14Fh)

Virtual Channel Capability is defined for Egress direction of the device. For Root Port, since only VC0 is defined.

- VC0 mapping: TC0, TC1, TC2, TC3, TC4, TC5, TC6, TC7
- No VC arbitration table
- No port arbitration table

Offset Address: 143-140h (D3F1)

Virtual Channel Enhanced Capability Header **Default Value: 1801 0002h**

Bit	Attribute	Default	Description
31:20	RO	180h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0002h	**PCI Express Extended Capability ID**

Offset Address: 147-144h (D3F1)

Port VC Capability 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:10	RO	0	**Port Arbitration Table Entry Size** Reserved for root port.
9:8	RO	0	**Reference Clock** Reserved for root port.
7	RO	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count**
3	RO	0	**Reserved**
2:0	RO	000b	**Extended VC Count**

Offset Address: 14B-148h (D3F1)

Port VC Capability 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**VC Arbitration Table Offset** 00 since only VC0 is defined.
23:8	RO	0	**Reserved**
7:0	RO	0	**VC Arbitration Capability** Reserved

Offset Address: 14D-14Ch (D3F1)

Port VC Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3:1	RO	0	**VC Arbitration Select** Reserved
0	RO	0	**Local VC Arbitration Table** Reserved

Offset Address: 14F-14Eh (D3F1)

Port VC Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	0	**VC Arbitration Table Status** Reserved

VC0 Resource (150-15Bh)

Offset Address: 153-150h (D3F1)
VC Resource Capability (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Arbitration Table Offset (VC0)** Reserved for Root Port.
23	RO	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)**
15	RO	0	**Reject Snoop Transactions**
14	RO	0	**Advanced Packet Switching** Reserved
13:8	RO	0	**Reserved**
7:0	RO	0	**Port Arbitration Capability** Reserved for Root Port.

Offset Address: 157-154h (D3F1)
VC Resource Control (VC0) **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1b	**VC Enable**
30:27	RO	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	RO	0	**Reserved**
19:17	RO	0	**Port Arbitration Select** Reserved for Root Port.
16	RO	0	**Load Port Arbitration Table** Reserved for Root Port.
15:8	RO	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC / VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit-0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 15B-158h (D3F1)
VC Resource Status (VC0) **Default Value: 0002 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	1b	**VC Negotiation Pending (TL)** This bit indicates whether the Virtual Channel negotiation is in Pending state (set/clear by hardware). 0: Negotiation is complete. 1: Negotiation is on-going.
16	RO	0	**Port Arbitration Table Status** Reserved for Root Port.
15:0	RO	0	**Reserved**

VC1 Resource (15C-19Fh)

Offset Address: 15C-17Fh (D3F1) – Reserved

Offset Address: 183-180h (D3F1)

Root Complex Link Declaration Capabilities Header **Default Value: 0001 0005h**

Bit	Attribute	Default	Description
31:20	RO	0	**Next Capability**
19:16	RO	1h	**Capability Version**
15:0	RO	0005h	**Capability ID**

Offset Address: 187-184h (D3F1)

Element Self Description **Default Value: 0301 0100h**

Bit	Attribute	Default	Description
31:24	RO	03h	**Port Number**
23:16	RO	01h	**Component ID**
15:8	RO	01h	**Number of Link Entries**
7:4	RO	0	**Reserved**
3:0	RO	0	**Element Type** 0h: Configuration Space Element 1h: System egress port or internal sink 2h: Internal Root Complex Link

Offset Address: 188-18Fh (D3F1) – Reserved

Offset Address: 193-190h (D3F1)

Upstream Link Descriptor **Default Value: 0001 0001h**

Bit	Attribute	Default	Description
31:24	RO	0	**Target Port Number** Indicates the port number of RCRB-H.
23:16	RO	01h	**Target Component ID**
15:2	RO	0	**Reserved**
1	RO	0	**Link Type** Indicates the link points to RCRB-H.
0	RO	1b	**Link Valid**

Offset Address: 194-197h (D3F1) – Reserved

Offset Address: 19F-198h (D3F1)

Upstream Link Base Address for RCRB-H[63:12] **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:32	RO	0	**Base Address Upper**
31:0	RO	0	**Base Address Lower**

PCI Express Root Complex Register Block – Host

Virtual Channel Capability (000-00Fh)

Offset Address: 003-000h (RCRB-H)

Virtual Channel Enhanced Capability Header **Default Value: 0401 0002h**

Bit	Attribute	Default	Description
31:20	RO	040h	**Next Capability Offset**
19:16	RO	1h	**Capability Version**
15:0	RO	0002h	**PCI Express Extended Capability ID**

Offset Address: 007-004h (RCRB-H)

Port VC Capability 1 **Default Value: 0000 0800h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:10	RO	10b	**Port Arbitration Table Entry Size** The upstream arbitration unit of this chip supports up to 6 ports. 10b indicates the size of port arbitration table entry is 4 bits.
9:8	RO	0	**Reference Clock**
7	RO	0	**Reserved**
6:4	RO	0	**Low Priority Extended VC Count**
3	RO	0	**Reserved**
2:0	RO	0	**Extended VC Count** This chip supports VC0 only.

Offset Address: 00B-008h (RCRB-H)

Port VC Capability 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	00h	**VC Arbitration Table** 00: Table is not present.
23:8	RO	0	**Reserved**
7:0	RO	0	**VC Arbitration Capability** Use hardware fixed arbitration scheme.

Offset Address: 00D-00Ch (RCRB-H)

Port VC Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:4	RO	0	**Reserved**
3:1	RW	0	**VC Arbitration Select**
0	RO	0	**Load VC Arbitration Table**

Offset Address: 00F-00Eh (RCRB-H)

Port VC Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	0	**VC Arbitration Table Status** Reserved

VC0 Resource (010-01Bh)

Offset Address: 013-010h (RCRB-H)

VC Resource Capability (VC0) **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Arbitration Table (VC0)**
23	RO	0	**Reserved**
22:16	RO	0	**Maximum Time Slots (TL)** Reserved
15	RO	0	**Reject Snoop Transactions** Reserved
14	RO	0	**Advanced Packet Switching** Reserved
13:8	RO	0	**Reserved**
7:0	RO	01h	**Port Arbitration Capability** Round Robin (RR)

Offset Address: 017-014h (RCRB-H)

VC Resource Control (VC0) **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RW	1b	**VC Enable**
30:27	RO	0	**Reserved**
26:24	RO	0	**VC ID**
23:20	RO	0	**Reserved**
19:17	RW	0	**Port Arbitration Select** Reserved
16	RO	0	**Load Port Arbitration Table**
15:8	RO	0	**Reserved**
7:0	RW Bit 0: RO	FFh	**TC/VC Mapping** This field indicates the TCs that are mapped to VC0. If bit [n] is 1, the corresponding traffic class TCn is mapped to VC0 (0 <= n <= 7). Default is TC0, TC1, TC2, TC3, C4, TC5, TC6 and TC7 are all mapped to VC0. Note: Bit 0 is hardwired to 1 (i.e. TC0 is always mapped to VC0).

Offset Address: 01B-018h (RCRB-H)

VC Resource Status (VC0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17	RO	0	**VC Negotiation Pending (TL)**
16	RO	0	**Port Arbitration Table Status** Reserved
15:0	RO	0	**Reserved**

Offset Address: 01C-03Fh (RCRB-H) – Reserved

Root Complex Link Declaration Enhanced Capability (040-04Fh)

Offset Address: 043-040h (RCRB-H)

Root Complex Link Declaration Capabilities Header **Default Value: 0001 0005h**

Bit	Attribute	Default	Description
31:20	RO	0	**Next Capability**
19:16	RO	1h	**Capability Version**
15:0	RO	0005h	**PCI Express Extended Capability ID**

Offset Address: 047-044h (RCRB-H)

Element Self Description **Default Value: 0001 0401h**

Bit	Attribute	Default	Description
31:24	RO	0	**Port Number** 0: Egress port
23:16	RO	01h	**Component ID**
15:8	RO	04h	**Number of Link Entries** 4 Links
7:4	RO	0	**Reserved**
3:0	RO	1h	**Element Type** 0h: Configuration space element 1h: System egress port or internal sink 2h: Internal Root Complex Link

Offset Address: 048-04Fh (RCRB-H) – Reserved

Link Entry for PEG0 (050-05Fh)

Offset Address: 053-050h (RCRB-H)

PEG0 Link Description **Default Value: 0101 0003h**

Bit	Attribute	Default	Description
31:24	RO	01h	**Target Port Number**
23:16	RO	01h	**Target Component ID**
15:2	RO	0	**Reserved**
1	RO	1b	**Link Type** Link points to PEG0.
0	RO	1b	**Link Valid**

Offset Address: 054-057h (RCRB-H) – Reserved

Offset Address: 05F-058h (RCRB-H)

PEG0 Link Address **Default Value: 0000 0000 0001 0000h**

Bit	Attribute	Default	Description
63:28	RO	0	**PCI Express Configuration Space Base Address** A Root Complex that does not implement multiple configuration spaces is allowed to report this field as 0.
27:20	RO	0	**Bus Number**
19:15	RO	02h	**Device Number**
14:12	RO	0	**Function Number**
11:0	RO	0	**Reserved**

Link Entry for PE0 (060-06Fh)

Offset Address: 063-060h (RCRB-H)

PE0 Link Description **Default Value: 0201 0003h**

Bit	Attribute	Default	Description
31:24	RO	02h	**Target Port Number**
23:16	RO	01h	**Target Component ID**
15:2	RO	0	**Reserved**
1	RO	1b	**Link Type** Link points to PE0.
0	RO	1b	**Link Valid**

Offset Address: 064-067h (RCRB-H) – Reserved

Offset Address: 06F-068h (RCRB-H)

PE0 Link Address **Default Value: 0000 0000 0001 8000h**

Bit	Attribute	Default	Description
63:28	RO	0	**PCI Express Configuration Space Base Address** A Root Complex that does not implement multiple configuration spaces is allowed to report this field as 0.
27:20	RO	0	**Bus Number**
19:15	RO	03h	**Device Number**
14:12	RO	0	**Function Number**
11:0	RO	0	**Reserved**

Link Entry for PE1 (070-07Fh)

Offset Address: 073-070h (RCRB-H)

PE1 Link Description **Default Value: 0301 0003h**

Bit	Attribute	Default	Description
31:24	RO	03h	**Target Port Number**
23:16	RO	01h	**Target Component ID**
15:2	RO	0	**Reserved**
1	RO	1b	**Link Type** Link points to PE1.
0	RO	1b	**Link Valid**

Offset Address: 074-077h (RCRB-H) – Reserved

Offset Address: 07F-078h (RCRB-H)

PE1 Link Address **Default Value: 0000 0000 0001 9000h**

Bit	Attribute	Default	Description
63:28	RO	0	**PCI Express Configuration Space Base Address** A Root Complex that does not implement multiple configuration spaces is allowed to report this field as 0.
27:20	RO	0	**Bus Number**
19:15	RO	03h	**Device Number**
14:12	RO	1h	**Function Number**
11:0	RO	0	**Reserved**

Link Entry for HDAC (080-08Fh)

Offset Address: 083-080h (RCRB-H)

HDAC Link Description **Default Value: 0401 0003h**

Bit	Attribute	Default	Description
31:24	RO	04h	**Target Port Number**
23:16	RO	01h	**Target Component ID**
15:2	RO	0	**Reserved**
1	RO	1b	**Link Type** Link points to HDAC.
0	RO	1b	**Link Valid**

Offset Address: 084-087h (RCRB-H) – Reserved

Offset Address: 08F-088h (RCRB-H)

HDAC Link Address **Default Value: 0000 0000 000A 0000h**

Bit	Attribute	Default	Description
63:28	RO	0	**PCI Express Configuration Space Base Address** A Root Complex that does not implement multiple configuration spaces is allowed to report this field as 0.
27:20	RO	0	**Bus Number**
19:15	RO	14h	**Device Number**
14:12	RO	0	**Function Number**
11:0	RO	0	**Reserved**

Offset Address: 090-1FFh (RCRB-H) – Reserved

VC Arbitration Timer (200-20Fh)

The arbitration schemes of PCI Express and DRAM controller are the same. Occupancy Timer is used to guarantee the number of time slots so that one requester will be granted when there is no high priority requester. Promote Timer is used for a requester to upgrade its requests to high priority if it is not served after the Promote Timer times out. However, priority request promoted by the expiration of the Promote Timer will be served once only.

Offset Address: 200h (RCRB-H)
VC0 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**VC0 Occupancy Timer** (in unit of 125MHz) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 201h (RCRB-H)
VC0 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**VC0 Promote Timer** (in unit of 125MHz) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 202-20Fh (RCRB-H) – Reserved

Port Arbitration Timer for VC0 (210-219h)

Offset Address: 210h (RCRB-H)
PEG0 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Occupancy Timer** (in unit of 125MHz) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 211h (RCRB-H)
PEG0 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Promote Timer** (in unit of 125MHz) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 212h (RCRB-H)

PE0 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Occupancy Timer** (in unit of 125MHz) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 213h (RCRB-H)

PE0 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Promote Timer** (in unit of 125MHz) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 214h (RCRB-H)

PE1 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Occupancy Timer** (in unit of 125MHz) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 215h (RCRB-H)

PE1 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Promote Timer** (in unit of 125MHz) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 216-22Fh (RCRB-H) – Reserved

Host Side Upstream Arbitration Timers (230-23Fh)

A fair arbitration timer is designed for the upstream traffic, which provides a fair arbitration between PCI express devices and other devices like PCI2 master, IO APIC and North-South Module Interface Control. The arbitration scheme is also used by DRAM controller.

Offset Address: 230h (RCRB-H)
PCIe – VC0 Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Occupancy Timer** (in unit of host frequency) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 231h (RCRB-H)
PCIe – VC0 Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Promote Timer** (in unit of host frequency) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 232-233h (RCRB-H) – Reserved

Offset Address: 234h (RCRB-H)
PCCA Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**High Priority to SM Request** 0: Disable 1: Enable
6:4	RO	0	**Reserved**
3:0	RW	0000b	**Occupancy Timer** (in unit of host frequency) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 235h (RCRB-H)
PCCA P2C Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Promote Timer** (in unit of host frequency) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 236-237h (RCRB-H) – Reserved

Offset Address: 238h (RCRB-H)
IGFX Arbitration Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Strict Priority to GADS from IGFX** 0: Disable 1: Enable
6:4	RO	0	**Reserved**
3:0	RW	0000b	**Occupancy Timer** (in unit of host frequency) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 239h (RCRB-H)
IGFX Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Promote Timer** (in unit of host frequency) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 23A-23Bh (RCRB-H) – Reserved

Offset Address: 23Ch (RCRB-H)
IO APIC Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Occupancy Timer** (in unit of host frequency) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 23Dh (RCRB-H)
IO APIC Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Promote Timer** (in unit of host frequency) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 23Eh (RCRB-H)
IPI Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Occupancy Timer** (in unit of host frequency) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 23Fh (RCRB-H)
IPI Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Promote Timer** (in unit of host frequency) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 240-24Fh (RCRB-H) – Reserved

PXPTRF (Central Traffic Controller) P2P Arbitration Timer of PCIe (250-253h)

Offset Address: 250-251h (RCRB-H) – Reserved

Offset Address: 252h (RCRB-H)

P2P Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Occupancy Timer** (in unit of host frequency) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 253h (RCRB-H)

P2P Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Promote Timer** (in unit of host frequency) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 254h (RCRB-H)

PCCA Occupancy Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Occupancy Timer** (in unit of host frequency) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 255h (RCRB-H)

PCCA P2P Promote Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Promote Timer** (in unit of host frequency) 0000: Timer is off 0nh: n x 4 T, where 1< n <= 15

Offset Address: 256-25Fh (RCRB-H) – Reserved

SOUTH MODULE REGISTER DESCRIPTIONS

Legacy I/O Ports

This group of registers includes the DMA Controllers, Interrupt Controllers, and Timer/Counters as well as a number of miscellaneous ports originally implemented by using discrete logic on original PC/AT motherboards. All the registers listed are integrated on-chip. These registers are implemented in a precise manner for backwards compatibility with previous generations of PC hardware. These registers are listed for information purposes only. Detailed descriptions of the actions and programming of these registers are included in numerous industry publications (duplication of that information here is beyond the scope of this document). All the registers reside in I/O space.

System I/O Ports Map

Port	Function
00-1F	**Master DMA Controller**
20-3F	**Master Interrupt Controller**
40-5F	**Timer / Counter**
60-6F	**Keyboard Controller**
60h	**KBC Data**
61h	**Misc Functions & Speaker Control**
64h	**KBC Command / Status**
70-77	**RTC/CMOS/NMI-Disable**
78-7F	**-available for system use**
80	**-reserved- (debug port)**
81-8F	**DMA Page Registers**
90-91	**-available for system use**
92	**System Control**
93-9F	**-available for system use**
A0-BF	**Slave Interrupt Controller**
C0-DF	**Slave DMA Controller**
E0-FF	**-available for system use**
100-CF7	**-available for system use**
CF8-CFB	**PCI Configuration Address**
CFC-CFF	**PCI Configuration Data**
D00-FFFF	**-available for system use**

I/O Port Address: 61h

Miscellaneous Functions & Speaker Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**SERR# Status** 0: SERR# has not been asserted 1: SERR# was asserted by a PCI agent Note: This bit is set when the PCI bus SERR# signal is asserted. Once set, this bit may be cleared by setting bit-2 of this register. Bit-2 should be cleared to enable recording of the next SERR# (i.e., bit-2 must be set to 0 to enable this bit to be set).
6	RO	0	**IOCHK# Status** 0:IOCHK# has not been asserted 1: IOCHK # was asserted by an ISA agent Note: This bit is set when the ISA bus IOCHCK# signal is asserted. Once set, this bit may be cleared by setting bit-3 of this register. Bit-3 should be cleared to enable recording of the next IOCHCK# (i.e., bit-3 must be set to 0 to enable this bit to be set). IOCHCK# generates NMI to the CPU if NMI is enabled.
5	RO	0	**Timer/Counter 2 Output** This bit reflects the output of Timer/Counter 2 without any synchronization.
4	RO	0	**Refresh Detected** This bit toggles to reflect timer update on every rising edge of the ISA bus REFRESH# signal.
3	RW	0	**IOCHK# Enable** 0: Enable (see bit-6 above) 1: Disable (force IOCHCK# inactive and clear any "IOCHCK# Active" condition in bit-6)
2	RW	0	**SERR# Enable** 0: Enable (see bit-7 above) 1: Disable (force SERR# inactive and clear any "SERR# Active" condition in bit-7)
1	RW	0	**Speaker Enable** 0: Disable 1: Enable Timer/Counter 2 output to drive SPKR pin
0	RW	0	**Timer/Counter 2 Enable** 0: Disable 1: Enable Timer/Counter 2

I/O Port Address: 92h

System Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**A20 Address Line Enable** 0: A20 disabled / forced 0 (real mode) 1: A20 address line enabled
0	RW	0	**High Speed Reset** 0: Normal 1: Briefly pulse system reset to switch from protected mode to real mode

Keyboard Controller I/O Registers

The keyboard controller handles the keyboard and mouse interfaces. Two ports are used: port 60 and port 64. Reads from port 64 return a status byte. Writes to port 64h are command codes (see command code list following the register descriptions). Input and output data is transferred via port 60h.

A "Control" register is also available. It is accessible by writing commands 20h / 60h to the command port (port 64h); the control byte is written by first sending 60h to the command port, then sending the control byte value. The control register may be read by sending a command of 20h to port 64h, waiting for "Output Buffer Full" status = 1, then reading the control byte value from port 60h.

Traditional (non-integrated) keyboard controllers have an "Input Port" and an "Output Port" that control pins dedicated to specific functions. These ports are defined as follows:

Bit	Input Port
0	Keyboard Data In
1	Mouse Data In

Bit	Output Port
0	System Reset (1 = Execute Reset)
1	Gate A20 (1 = A20 Enabled)
2	Mouse Data Out
3	Mouse Clock Out
6	Keyboard Clock Out
7	Keyboard Data Out

Bit	Test Port
0	Keyboard Clock In
1	Mouse Clock In

The above definitions are provided for reference only as actual keyboard and mouse control is no longer performed bit by bit using the above ports but controlled directly by keyboard / mouse controller internal logic. Data is sent and received using the command codes listed on the following page.

I/O Port Address: 60h

Keyboard Controller Input / Output Buffer

Bit	Attribute	Description
7:0	RW	When Write: **Keyboard Controller Input Buffer** Only write to port 60h if port 64h bit-1 = 0 (1=full). When Read: **Keyboard Controller Output Buffer** Only read from port 60h if port 64h bit-0 = 1 (0=empty).

Only write to port 60h if port 64h bit-1 = 0 (1=full).

I/O Port Address: 64h (When Read)

Keyboard / Mouse Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Parity Error** 0: No parity error (odd parity received) 1: Even parity occurred on last byte received from keyboard / mouse
6	RO	0	**General Receive / Transmit Timeout** 0: No Error 1: Error
5	RO	0	**Mouse Output Buffer Full** 0: Mouse output buffer empty 1: Mouse output buffer holds mouse data
4	RO	0	**Keylock Status** 0: Locked 1: Free
3	RO	0	**Command / Data** 0: Last write was data write 1: Last write was command write
2	RO	0	**System Flag** 0: Power-On default 1 Self test successful
1	RO	0	**Input Buffer Full** 0: Input buffer empty 1: Input buffer full
0	RO	0	**Keyboard Output Buffer Full** 0: Keyboard output buffer empty 1: Keyboard output buffer full

I/O Port Address: 64h (When Write)
Keyboard / Mouse Command

This port is used to send commands to the keyboard / mouse controller. The command codes recognized by this chip are listed in the table below.

Table 19. Keyboard Controller Command Codes

Code	Keyboard Command Code Description
20h	Read Control Byte (next byte is Control Byte)
21-3Fh	Read SRAM Data (next byte is Data Byte)
60h	Write Control Byte (next byte is Control Byte)
61-7Fh	Write SRAM Data (next byte is Data Byte)
A1h	Output Keyboard Controller Version #
A4h	Test if Password is installed (always returns F1h to indicate not installed)
A7h	Disable Mouse Interface
A8h	Enable Mouse Interface
A9h	Mouse Interface Test (puts test results in port 60h) Value: 0=OK, 1=clock stuck low, 2=clock stuck high, 3=data stuck low, 4=data stuck high, FF=general error
AAh	KBC self test (returns 55h if OK, FCh if not)
ABh	Keyboard Interface Test (see A9h Mouse Test)
ADh	Disable Keyboard Interface
AEh	Enable Keyboard Interface
AFh	Return Version #
C0h	Read Input Port (read input data to output buffer)
C1h	Poll Input Port (read Mouse Data In continuously to status bit 5)
C8h	Unblock Mouse Output (use before D1 to change active mode)
C9h	Reblock Mouse Output (protection mechanism for D1)
CAh	Read Mode (output KBC mode info to port 60 output buffer: bit 0=0 if ISA, bit 0=1 if PS/2)
D0h	Read Output Port (copy output port values to port 60)
D1h	Write Output Port (data byte following is written to keyboard output port as if it came from keyboard)
D2h	Write Keyboard Output Buffer & clear status bit 5 (write following byte to keyboard)
D3h	Write Mouse Output Buffer & set status bit 5 (write following byte to mouse; put value in mouse input buffer so it appears to have action from the mouse)
D4h	Write Mouse (write following byte to mouse)
E0h	Read Keyboard Clock In and Mouse Clock In (return in bits 0-1 respectively of response byte)
Exh	Set Mouse Clock Out per command bit 3 Set Mouse Data Out per command bit 2 Set Gate A20 per command bit 1
Fxh	Pulse Mouse Clock Out low for 6 us per command bit 3 Pulse Mouse Data Out low for 6 us per command bit 2 Pulse Gate A20 low for 6 us per command bit 1 Pulse System Reset low for 6 us per command bit 0

All other codes not listed are undefined.

KBC Control Register (R/W via Commands 20h/60h)

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	1b	**PC Compatibility** 0: Disable scan conversion 1: Convert scan codes to PC format; convert 2-byte break sequences to 1-byte PC-compatible break codes.
5	RW	0	**Mouse Interface** 0: Enable 1: Disable
4	RW	0	**Keyboard Interface** 0: Enable 1: Disable
3	RO	0	**Reserved**
2	RO	0	**System Flag** This bit may be read back as status register bit-2.
1	RW	0	**Mouse Interrupts** 0: Disable 1: Enable. Generate interrupt on IRQ12 when mouse data comes into output buffer.
0	RW	0	**Keyboard Interrupts** 0: Disable 1: Enable. Generate interrupt on IRQ1 when output buffer has been written.

DMA Controller I/O Registers

I/O Ports Address: 00-0Fh
Master DMA Controller

Channels 0-3 of the Master DMA Controller control System DMA Channels 0-3. There are 16 Master DMA Controller registers:

I/O Address Bits 15-0	Attribute	Description
0000 0000 000x 0000	RW	**Channel 0 Base / Current Address**
0000 0000 000x 0001	RW	**Channel 0 Base / Current Count**
0000 0000 000x 0010	RW	**Channel 1 Base / Current Address**
0000 0000 000x 0011	RW	**Channel 1 Base / Current Count**
0000 0000 000x 0100	RW	**Channel 2 Base / Current Address**
0000 0000 000x 0101	RW	**Channel 2 Base / Current Count**
0000 0000 000x 0110	RW	**Channel 3 Base / Current Address**
0000 0000 000x 0111	RW	**Channel 3 Base / Current Count**
0000 0000 000x 1000	RW	**Status / Command**
0000 0000 000x 1001	WO	**Write Request**
0000 0000 000x 1010	WO	**Write Single Mask**
0000 0000 000x 1011	WO	**Write Mode**
0000 0000 000x 1100	WO	**Clear Byte Pointer**
0000 0000 000x 1101	WO	**Master Clear**
0000 0000 000x 1110	WO	**Clear Mask**
0000 0000 000x 1111	RW	**Read/Write All Mask Bits**

I/O Ports Address: C0- DFh
Slave DMA Controller

Channels 0-3 of the Slave DMA Controller control System DMA Channels 4-7. There are 16 Slave DMA Controller registers:

I/O Address Bits 15-0	Attribute	Description
0000 0000 1100 000x	RW	**Channel 4 Base / Current Address**
0000 0000 1100 001x	RW	**Channel 4 Base / Current Count**
0000 0000 1100 010x	RW	**Channel 5 Base / Current Address**
0000 0000 1100 011x	RW	**Channel 5 Base / Current Count**
0000 0000 1100 100x	RW	**Channel 6 Base / Current Address**
0000 0000 1100 101x	RW	**Channel 6 Base / Current Count**
0000 0000 1100 110x	RW	**Channel 7 Base / Current Address**
0000 0000 1100 111x	RW	**Channel 7 Base / Current Count**
0000 0000 1101 000x	RW	**Status / Command**
0000 0000 1101 001x	WO	**Write Request**
0000 0000 1101 010x	WO	**Write Single Mask**
0000 0000 1101 011x	WO	**Write Mode**
0000 0000 1101 100x	WO	**Clear Byte Pointer F/F**
0000 0000 1101 101x	WO	**Master Clear**
0000 0000 1101 110x	WO	**Clear Mask**
0000 0000 1101 111x	WO	**Read/Write All Mask Bits**

Note that not all bits of the address are decoded.

The Master and Slave DMA Controllers are compatible with the Intel 8237 DMA Controller chip. Detailed description of 8237 DMA controller operations can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

I/O Ports Address: 80-8Fh

DMA Page Registers

There are eight DMA Page Registers, one for each DMA channel. These registers provide bits 16-23 of the 24-bit address for each DMA channel (address bits 0-15 are stored in registers in the Master and Slave DMA Controllers). They are located at the following I/O Port addresses:

I/O Address Bits 15-0	Attribute	Description
0000 0000 1000 0111	RW	**Channel 0 DMA Page (M-0)**
0000 0000 1000 0011	RW	**Channel 1 DMA Page (M-1)**
0000 0000 1000 0001	RW	**Channel 2 DMA Page (M-2)**
0000 0000 1000 0010	RW	**Channel 3 DMA Page (M-3)**
0000 0000 1000 1111	RW	**Channel 4 DMA Page (S-0)**
0000 0000 1000 1011	RW	**Channel 5 DMA Page (S-1)**
0000 0000 1000 1001	RW	**Channel 6 DMA Page (S-2)**
0000 0000 1000 1010	RW	**Channel 7 DMA Page (S-3)**

DMA Controller Shadow Registers

The DMA Controller shadow registers are enabled by setting D17F0 Rx40 bit[1]. If the shadow registers are enabled, DMA control registers' contents could be read back from the indicated I/O port instead of the standard DMA controller registers (writes are unchanged).

Port Address	Attribute	Description
Port 0	RO	**Channel 0 Base Address**
Port 1	RO	**Channel 0 Byte Count**
Port 2	RO	**Channel 1 Base Address**
Port 3	RO	**Channel 1 Byte Count**
Port 4	RO	**Channel 2 Base Address**
Port 5	RO	**Channel 2 Byte Count**
Port 6	RO	**Channel 3 Base Address**
Port 7	RO	**Channel 3 Byte Count**
Port 8	RO	**1st Read Channel 0-3 Command Register**
Port 8	RO	**2nd Read Channel 0-3 Request Register**
Port 8	RO	**3rd Read Channel 0 Mode Register**
Port 8	RO	**4th Read Channel 1 Mode Register**
Port 8	RO	**5th Read Channel 2 Mode Register**
Port 8	RO	**6th Read Channel 3 Mode Register**
Port F	RO	**Channel 0-3 Read All Mask**
Port C4	RO	**Channel 5 Base Address**
Port C6	RO	**Channel 5 Byte Count**
Port C8	RO	**Channel 6 Base Address**
Port CA	RO	**Channel 6 Byte Count**
Port CC	RO	**Channel 7 Base Address**
Port CE	RO	**Channel 7 Byte Count**
Port D0	RO	**1st Read Channel 4-7 Command Register**
Port D0	RO	**2nd Read Channel 4-7 Request Register**
Port D0	RO	**3rd Read Channel 4 Mode Register**
Port D0	RO	**4th Read Channel 5 Mode Register**
Port D0	RO	**5th Read Channel 6 Mode Register**
Port D0	RO	**6th Read Channel 7 Mode Register**
Port DE	RO	**Channel 4-7 Read All Mask**

Interrupt Controller I/O Registers

This chip integrates two Interrupt Controllers, Master and Slave Interrupt Controllers, either one is compatible with the Intel 8259 Interrupt Controller chip. Detailed descriptions of 8259 Interrupt Controller operations can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

I/O Ports Address: 21-20h
Master Interrupt Controller

The Master Interrupt Controller controls system interrupt channels 0-7 and occupies two register locations:

I/O Address Bits 15-0	Attribute	Description
0000 0000 001x xxx0	RW	**Master Interrupt Control**
0000 0000 001x xxx1	RW	**Master Interrupt Mask**

Note that not all bits of the address are decoded.

I/O Ports Address: A1-A0h
Slave Interrupt Controller

The Slave Interrupt Controller controls system interrupt channels 8-15. The slave system interrupt controller also occupies two register locations:

I/O Address Bits 15-0	Attribute	Description
0000 0000 101x xxx0	RW	**Slave Interrupt Control**
0000 0000 101x xxx1	RW	**Slave Interrupt Mask**

Note that not all address bits are decoded.

Interrupt Controller I/O Shadow Registers

The following shadow registers are enabled by setting D17F0 Rx40[1]. If the shadow registers are enabled, Interrupt Controller control registers' contents could be read back from the indicated I/O port instead of the standard interrupt controller registers (writes are unchanged).

I/O Ports Address: 20h
Master Interrupt Control Shadow

Bit	Attribute	Description
7	RO	**Reserved**
6	RO	**OCW3 bit 2 for Poll Mode (POLL)**
5	RO	**OCW3 bit 0 for Read IS Register (RIS)**
4	RO	**OCW3 bit 5 for Special Mask Mode (SMM)**
3	RO	**OCW2 bit 7 for Rotation (R)**
2	RO	**ICW4 bit 4 for Special Fully Nest Mode (SFNM)**
1	RO	**ICW4 bit 1 for Automatic End of Interrupt (AEOI)**
0	RO	**ICW1 bit 3 for Level Trigger Mode (LTIM)**

Note: OCW: Operation Command Word; ICW: Initialization Command Word

I/O Ports Address: A0h
Slave Interrupt Control Shadow

Bit	Attribute	Description
7	RO	**Reserved**
6	RO	**OCW3 bit 2 for Poll Mode (POLL)**
5	RO	**OCW3 bit 0 for Read IS Register (RIS)**
4	RO	**OCW3 bit 5 for Special Mask Mode (SMM)**
3	RO	**OCW2 bit 7 for Rotation (R)**
2	RO	**ICW4 bit 4 for Special Fully Nest Mode (SFNM)**
1	RO	**ICW4 bit 1 for Automatic End of Interrupt (AEOI)**
0	RO	**ICW1 bit 3 for Level Trigger Mode (LTIM)**

Note: OCW: Operation Command Word; ICW: Initialization Command Word

I/O Ports Address: 21h
Master Interrupt Mask Shadow

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RO	—	**T7-T3 of Interrupt Vector Address**

I/O Ports Address: A1h
Slave Interrupt Mask Shadow

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RO	—	**T7-T3 of Interrupt Vector Address**

Timer / Counter I/O Registers

The Timer / Counters are compatible with the Intel 8254 Timer / Counter chip. Detailed descriptions of 8254 Timer / Counter operation can be obtained from the Intel Peripheral Components Data Book and numerous other industry publications.

There are 4 Timer / Counter registers:

I/O Address Bits 15-0	Attribute	Description
0000 0000 010x xx00	RW	**Timer / Counter 0 Count**
0000 0000 010x xx01	RW	**Timer / Counter 1 Count**
0000 0000 010x xx10	RW	**Timer / Counter 2 Count**
0000 0000 010x xx11	WO	**Timer / Counter Command Mode**

Note that not all bits of the address are decoded.

Timer / Counter Shadow Registers

The following shadow registers are enabled for readback by setting D17F0 Rx40[1]. If the shadow registers are enabled, Timer / Counter registers are read back from the indicated I/O port instead of the standard timer / counter registers (writes are unchanged).

Port Address	Attribute	Description
Port 40	RO	**Counter 0 Base Count Value (LSB 1st MSB 2nd)**
Port 41	RO	**Counter 1 Base Count Value (LSB 1st MSB 2nd)**
Port 42	RO	**Counter 2 Base Count Value (LSB 1st MSB 2nd)**

CMOS / RTC I/O Registers

I/O Ports Address: 70h
CMOS Address

Bit	Attribute	Default	Description
7	RW	1b	**NMI Disable** 0: Enable NMI Generation. NMI is asserted on encountering SERR# on the PCI bus. 1: Disable NMI Generation
6:0	RW	—	**CMOS Address** (lower 128 bytes of the CMOS memory)

I/O Ports Address: 71h
CMOS Data

Bit	Attribute	Default	Description
7:0	RW	0	**CMOS Data** (128 bytes of the CMOS memory)

Ports 70-71 may be accessed if D17F0 Rx51[3] is set to one to select the internal RTC. If Rx51[3] is set to zero, accesses to ports 70-71 will be directed to an external RTC.

I/O Ports Address: 74h
CMOS Address

Bit	Attribute	Default	Description
7:0	RW	0	**CMOS Address** (256 bytes of the CMOS memory)

I/O Ports Address: 75h
CMOS Data

Bit	Attribute	Default	Description
7:0	RW	0	**CMOS Data** (256 bytes of the CMOS memory)

Ports 74-75 may be accessed only if D17F0 Rx4E[3] (Port 74/75 Access Enable) is set to one to enable port 74/75 access.

Ports 70-71 are compatible with PC industry-standards and may be used to access the lower 128 bytes of the 256-byte on-chip CMOS RAM. Ports 74-75 may be used to access the full on-chip extended 256-byte space in cases where the on-chip RTC is disabled.

Note: The system Real Time Clock (RTC) is part of the "CMOS" block. The RTC control registers are located at specific offsets in the CMOS data area (00-0Dh and 7D-7Fh). Detailed descriptions of CMOS / RTC operation and programming can be obtained from the VIA VT82887 Data Book or numerous other industry publications. For reference, the definition of the RTC register locations and bits are summarized in the following table:

Table 20. CMOS Register Summary

Offset	Description		
	Register Function	Binary Range	Decimal Range
00	Seconds	00-3Bh	00-59
01	Seconds Alarm	00-3Bh	00-59
02	Minutes	00-3Bh	00-59
03	Minutes Alarm	00-3Bh	00-59
04	Hours	am 12hr 01-0Ch	01-12
		pm 12hr 81-8Ch	129-140
		24hr: 00-17h	00-23
05	Hours Alarm	am 12hr 01-0Ch	01-12
		pm 12hr 81-8Ch	129-140
		24hr: 00-17h	00-23
06	Day of the Week	Sun=1: 01-07h	01-07
07	Day of the Month	01-1Fh	01-31
08	Month	01-0Ch	01-12
09	Year	00-63h	00-99

Offset	Description		
	Register Function	Bit Description	
0A	Register A	7: UIP	Update In Progress
		6:4: DV2-0	Divide (010=Enable oscillator & keep time)
		3:0: RS3-0	Rate Select for Periodic Interrupt
0B	Register B	7: SET	Inhibit Update Transfers
		6: PIE	Periodic Interrupt Enable
		5: AIE	Alarm Interrupt Enable
		4: UIE	Update Ended Interrupt Enable
		3: SQWE	No function (read/write bit)
		2: DM	Data Mode (0= BCD; 1= Binary)
		1: 24/12	Hours Byte Format
		0: DSE	Daylight Savings Enable
0C	Register C	7: IRQF	Interrupt Request Flag
		6: PF	Periodic Interrupt Flag
		5: AF	Alarm Interrupt Flag
		4: UF	Update Ended Flag
		3:0	Unused (always read 0)
0D	Register D	7: VRT	Reads 1 if VBAT voltage is OK
		6:0	Unused (always read 0)
0E-7C	Software-Defined Storage Registers		
Offset	**Extended Function**	**Binary Range**	**Decimal Range**
7D	Date Alarm	01-1Fh	01-31
7E	Month Alarm	01-0Ch	01-12
7F	Century Field	13-14h	19-20

Keyboard / Mouse Wakeup Index / Data Registers

The Keyboard / Mouse Wakeup registers are accessed by performing I/O operations to / from an index / data pair of registers in system I/O space at port addresses 2Eh and 2Fh. The registers accessed using this mechanism are used to initialize Keyboard / Mouse Wakeup functions at index values in the range of E0-EFh.

Keyboard / Mouse Wakeup initialization is accomplished in three steps:

Step 1) Enter KBC initialization mode (set D17F0 Rx51[1] = 1)

Step 2) Initialize the chip

- a) Write index to port 2Eh
- b) Read / write data from / to port 2Fh
- c) Repeat a and b for all desired registers

Step 3) Exit KBC initialization mode (set D17F0 Rx51[1] = 0)

I/O Ports Address: 2Eh
Keyboard Wakeup Index

Bit	Attribute	Default	Description
7:0	RW	0	**Index Value** D17F0 PCI configuration space register Rx51[1] must be set to 1 to enable access to the configuration registers.

I/O Ports Address: 2Fh
Keyboard Wakeup Data

Bit	Attribute	Default	Description
7:0	RW	0	**Data Value**

Keyboard / Mouse Wakeup Registers

These registers are accessed via the port 2E / 2F index / data register pair with D17F0 Rx51[1] = 1 using the indicated index values below.

Index: E0h

Keyboard / Mouse Wakeup Enable **Default Value: 08h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved** Always reads 0.
4	RO	0	**Reserved**
3	RW	1b	**Win98 Keyboard Power Key Wake-up** 0: Disable 1: Enable
2	RW	0	**Password Wake-up** 0: Disable 1: Enable
1	RW	0	**PS/2 Mouse Wake-up** 0: Disable 1: Enable
0	RW	0	**Keyboard Wake-up** 0: Disable 1: Enable

Index: E1h

Keyboard Wakeup Scan Code Set 0 **Default Value: F0h**

Bit	Attribute	Default	Description
7:0	RW	F0h	**Keyboard Wakeup First Reference Scan Code** Write 00 means that Keyboard supports any key wake up.

Index: E2h

Keyboard Wakeup Scan Code Set 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Keyboard Wakeup Second Reference Scan Code** Write 00 means that PS/2 mouse supports anykey wake up.

Index: E3h

Keyboard Wakeup Scan Code Set 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Keyboard Wakeup Third Reference Scan Code**

Index: E4h

Keyboard Wakeup Scan Code Set 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Keyboard Wakeup Fourth Reference Scan Code**

Index: E5h

Keyboard Wakeup Scan Code Set 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	**Keyboard Wakeup Fifth Reference Scan Code**

Index: E6h

Keyboard Wakeup Scan Code Set 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	Keyboard Wakeup Sixth Reference Scan Code

Index: E7h

Keyboard Wakeup Scan Code Set 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	Keyboard Wakeup Seventh Reference Scan Code

Index: E8h

Keyboard Wakeup Scan Code Set 7 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	Keyboard Wakeup Eighth Reference Scan Code

Index: E9h

Mouse Wakeup Scan Code Set 1 **Default Value: 09h**

Bit	Attribute	Default	Description
7:0	RW	09h	Mouse Wakeup Scan Code Set 1

Index: EAh

Mouse Wakeup Scan Code Set 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	Mouse Wakeup Scan Code Set 2

Index: EBh

Mouse Wakeup Scan Code Mask **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	00h	Mouse Wakeup Scan Code Mask

Memory Mapped I/O APIC Registers

The IO APIC registers are accessed by an indirect addressing scheme using Index Registers and Data Registers that are mapped into memory space.

Memory Address: FEC00000h

APIC Index **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7:0	RW	0	**I/O APIC Index** 8-bit pointer to the I/O APIC register.

Memory Address: FEC00010h

APIC Data **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**I/O APIC Data** This is a 32-bit register for the data to be read or written to the I/O APIC indirect register pointed by the Index Register.

Memory Address: FEC00020h

APIC IRQ Pin Assertion **Default Value: nnh**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	WO	nnh	**IRQ Number** Bit[4:0] written to this register contain the IRQ number for this interrupt. The only valid values are 0-23.

Memory Address: FEC00040h

APIC EOI **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	WO	nnh	**Redirection Entry Clear** When a write is issued to this register, the I/O APIC will check this field and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, the "Remote_IRR" bit for that I/O Redirection Entry will be cleared.

Indexed I/O APIC Registers

For index registers setting, please refer to Memory Address FEC00000h (APIC Index) and FEC00010 (APIC Data).

Index: 00h

I/O APIC Identification **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:24	RW	0	**I/O APIC Identification** Software must program this value before using the I/O APIC.
23:0	RO	0	**Reserved**

Index: 01h

I/O APIC Version **Default Value: 0017 8003h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:16	RO	17h	**Maximum Redirection Entry** This value is equal to the number of interrupt input pins for the I/O APIC minus one. For this I/O APIC, the value is 17h.
15	RO	1b	**PCI IRQ** This bit is set to 1 to indicate that this version of the I/O APIC implements the IRQ Assertion register and that PCI devices are allowed to write to it to cause interrupt.
14:8	RO	0	**Reserved**
7:0	RO	03h	**APIC Version** The implementation version for this I/O APIC is 03h.

Index: 02h

I/O APIC Arbitration **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27:24	RO	0	**I/O APIC Arbitration ID**
23:0	RO	0	**Reserved**

Index: 03h

Boot Configuration **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RW	0	**Delivery Type** 0: Interrupt Delivery Mechanism is via the APIC Serial Bus. 1: Interrupt Delivery Mechanism is a Front-side Bus Message.

There are 24 64-bit I/O Redirection Table entry registers. Each register is a dedicated entry for each interrupt input signal.

Table 21. I/O Redirection Table

Index	Function	Mnemonic
11-10h	I/O APIC Redirection – APIC IRQ0	IOREDTBL0
13-12h	I/O APIC Redirection – APIC IRQ1	IOREDTBL1
15-14h	I/O APIC Redirection – APIC IRQ2	IOREDTBL2
17-16h	I/O APIC Redirection – APIC IRQ3	IOREDTBL3
19-18h	I/O APIC Redirection – APIC IRQ4	IOREDTBL4
1B-1Ah	I/O APIC Redirection – APIC IRQ5	IOREDTBL5
1C-1Dh	I/O APIC Redirection – APIC IRQ6	IOREDTBL6
1E-1Fh	I/O APIC Redirection – APIC IRQ7	IOREDTBL7
21-20h	I/O APIC Redirection – APIC IRQ8	IOREDTBL8
23-22h	I/O APIC Redirection – APIC IRQ9	IOREDTBL9
25-24h	I/O APIC Redirection – APIC IRQ10	IOREDTBL10
27-26h	I/O APIC Redirection – APIC IRQ11	IOREDTBL11
29-28h	I/O APIC Redirection – APIC IRQ12	IOREDTBL12
2B-2Ah	I/O APIC Redirection – APIC IRQ13	IOREDTBL13
2D-2Ch	I/O APIC Redirection – APIC IRQ14	IOREDTBL14
2F-2Eh	I/O APIC Redirection – APIC IRQ15	IOREDTBL15
31-30h	I/O APIC Redirection – APIC IRQ16	IOREDTBL16
33-32h	I/O APIC Redirection – APIC IRQ17	IOREDTBL17
35-34h	I/O APIC Redirection – APIC IRQ18	IOREDTBL18
37-36h	I/O APIC Redirection – APIC IRQ19	IOREDTBL19
39-38h	I/O APIC Redirection – APIC IRQ20	IOREDTBL20
3B-3Ah	I/O APIC Redirection – APIC IRQ21	IOREDTBL21
3D-3Ch	I/O APIC Redirection – APIC IRQ22	IOREDTBL22
3F-3Eh	I/O APIC Redirection – APIC IRQ23	IOREDTBL23

I/O Redirection Entry **Default Value: nnn1 nnnn nnnn nnnnh**

Bit	Attribute	Default	Description
63:56	RW	nnh	**Destination Field** In Physical Mode (bit-11=0), bits [59:56] contain an APIC ID. In Logical Mode (bit-11=1), bits [63:56] of the Destination Field specify the logical destination address. Destination Mode IOREDTBLx[11] Logical Destination Address 0: Physical Mode IOREDTBLx[59:56] = APIC ID 1: Logical Mode IOREDTBLx[63:56] = Set of processors
55:17	RO	0	**Reserved**
16	RW	0	**Interrupt Mask** 0: Not Mask 1: Masked
15	RW	0	**Trigger Mode** Indicates the type of signal on the interrupt pin that triggers an interrupt. 1: Level Sensitive 0: Edge Sensitive
14	RO	0	**Remote Interrupt Request Register (IRR)** This bit is used for level triggered interrupts. Its meaning is undefined for edge triggered interrupts. For level triggered interrupts, this bit is set to 1 when local APIC(s) accept the level interrupt sent by the IOAPIC. 0: EOI message with a matching interrupt vector is received from a local APIC 1: Level sensitive interrupt sent by IOAPIC accepted by local APIC(s)
13	RW	0	**Interrupt Input Pin Polarity** Specifies the polarity of the interrupt signal. 0: High active 1:Low active
12	RO	0	**Delivery Status** Contains the current status of the delivery of this interrupt. 0: Idle (there is currently no activity for this interrupt.) 1: Send Pending (the interrupt has been injected but its delivery is temporarily held either because the APIC bus is busy or because the receiving APIC unit can not currently accept the interrupt.)
11	RW	0	**Destination Mode** Determines the interpretation of the Destination field. 0: Physical Mode 1: Logical Mode
10:8	RW	000b	**Delivery Mode** Specify how the APICs listed in the destination field should act upon reception of this signal. 000: Fixed 001: Lowest Priority 010: SMI 011: Reserved 100: NMI 101: INIT 110: Reserved 111: ExtINT
7:0	RW	nnh	**Interrupt Vector** Contain the interrupt vector for this interrupt. Vector values range from 10h to FEh.

Indexed I/O UART DMA Control Registers

The base address is located at D17F0 RxB8[15:0] and through D17F0 RxB7[3] to enable or disable access.

Index: 00h

UART Port1 DMA Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved** Always reads 0.
5	RW	0	**COM1 Transmit Using High Performance Way with DMA** 0: Disable 1: Enable
4	RW	0	**COM1 Receive Using High Performance Way with DMA** 0: Disable 1: Enable
3	RW	0	**Generate Interrupt for COM1 Transmit Complete** 0: The interrupt signal of COM1 will not active even the Index 01h[1] is set. 1: The interrupt signal of COM1 will active if the Index 01h[1] is set.
2	RW	0	**Generate Interrupt for COM1 Receive Complete** 0: The interrupt signal of COM1 will not active even the Index 01h[0] is set. 1: The interrupt signal of COM1 will active if the Index 01h[0] is set.
1	RW	0	**COM1 Use DMA to Transmit Data** 0: Disable 1: Enable When reset as 0, it will be: 1) COM1 will not issue any DMA request for transmit data from memory to peripheral. 2) COM1 will ignore DMA acknowledge for its transmit. 3) Index 01h[1] will be cleared. When set as 1, it will be: 1) COM1 will issue DMA request for transmit data from memory to peripheral when COM1 transmit FIFO is available. 2) COM1 will respond to DMA acknowledge for data transmit.
0	RW	0	**COM1 Use DMA to Receive Data** 0: Disable 1: Enable When reset as 0, it will be: 1) COM1 will not issue any DMA request for transmit data from peripheral to memory. 2) COM1 will ignore DMA acknowledge for its receive. 3) Index 01h[0] will be cleared. When set as 1, it will be: 1) COM1 will issue DMA request for receive data from peripheral to memory when COM1 receive FIFO is available. 2) COM1 will respond to DMA acknowledge for data receive.

Index: 01h

UART Port1 DMA Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved** Always reads 0.
1	RW	0	**Status of Interrupt for COM1 Transmit Complete** 0: The DMA for transmit of COM1 has not finished yet. 1: The DMA for transmit of COM1 has finished. Write 1 or disable Index 00h[1] to clear.
0	RW	0	**Status of Interrupt for COM1 Receive Complete** 0: The DMA for receive of COM1 has not finished yet. 1: The DMA for receive of COM1 has finished. Write 1 or disable Index 00h[0] to clear.

Index: 02h

UART Port2 DMA Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved** Always reads 0.
5	RW	0	**COM2 Transmit Using High Performance Way with DMA** 0: Disable 1: Enable
4	RW	0	**COM2 Receive Using High Performance Way with DMA** 0: Disable 1: Enable
3	RW	0	**Generate Interrupt for COM2 Transmit Complete** 0: The interrupt signal of COM2 will not active even the Index 03h[1] is set. 1: The interrupt signal of COM2 will active if the Index 03h[1] is set.
2	RW	0	**Generate Interrupt for COM2 Receive Complete** 0: The interrupt signal of COM2 will not active even the Index 03h[0] is set. 1: The interrupt signal of COM2 will active if the Index 03h[0] is set.
1	RW	0	**COM2 Use DMA to Transmit Data** 0: Disable 1: Enable When reset as 0, it will be: 1) COM2 will not issue any DMA request for transmit data from memory to peripheral. 2) COM2 will ignore DMA acknowledge for its transmit. 3) Index 03h[1] will be cleared. When set as 1, it will be: 1) COM2 will issue DMA request for transmit data from memory to peripheral when COM2 transmit FIFO is available. 2) COM2 will respond to DMA acknowledge for data transmit.
0	RW	0	**COM2 Use DMA to Receive Data** 0: Disable 1: Enable When reset as 0, it will be: 1) COM2 will not issue any DMA request for transmit data from peripheral to memory. 2) COM2 will ignore DMA acknowledge for its receive. 3) Index 03h[0] will be cleared. When set as 1, it will be: 1) COM2 will issue DMA request for receive data from peripheral to memory when COM2 receive FIFO is available. 2) COM2 will respond to DMA acknowledge for data receive.

Index: 03h

UART Port2 DMA Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved** Always reads 0.
1	RW	0	**Status of Interrupt for COM2 Transmit Complete** 0: The DMA for transmit of COM2 has not finished yet. 1: The DMA for transmit of COM2 has finished. Write 1 or disable Index 02h[1] to clear.
0	RW	0	**Status of Interrupt for COM2 Receive Complete** 0: The DMA for receive of COM2 has not finished yet. 1: The DMA for receive of COM2 has finished. Write 1 or disable Index 02h[0] to clear.

When enabling high performance on Tx, it can transfer 16 bytes on one request for DMAC if transmit FIFO is empty, and it can gain much more performance with demand transfer mode and line buffer enabled.

When disabling high performance on Tx, it only transfers 1 byte of single transfer mode and 2 bytes of demand transfer mode on one request for DMAC if transmit FIFO is empty.

When enabling high performance on Rx, it will transfer all data in FIFO when receiver buffer trigger point reached or timeout and it can gain much more performance with demand transfer mode and line buffer enabled.

When disabling high performance on Rx, it will transfer data whenever receive data is not empty.

Device 12 Function 0 (D12F0) - SDIO Host Controller

PCI Configuration Space Header (00-3Fh)

Offset Address: 01-00h (D12F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 03-02h (D12F0)

Device ID **Default Value: 95D0h**

Bit	Attribute	Default	Description
15:0	RO	95D0h	**Device ID**

Offset Address: 05-04h (D12F0)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable**
9	RO	0	**Fast Back to Back**
8	RO	0	**SERR# Enable**
7	RO	0	**Address Stepping**
6	RO	0	**Parity Error Response**
5	RO	0	**VGA Palette Snooping**
4	RW	0	**Memory Write and Invalidate**
3	RO	0	**Respond to Special Cycle**
2	RW	0	**Bus Master**
1	RW	0	**Memory Space Access**
0	RW	0	**I/O Space Access**

Offset Address: 07-06h (D12F0)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RO	0	**Detect Parity Error**
14	RO	0	**Signaled System Error (SERR#)**
13	RO	0	**Received Master Abort**
12	RO	0	**Received Target Abort**
11	RO	0	**Signaled Target Abort**
10:9	RO	01b	**DEVSEL# Timing**
8	RO	0	**Data Parity Detected**
7	RO	0	**Fast Back-to-Back Capability**
6:5	RO	0	**Reserved**
4	RO	1b	**Capability List**
3	RO	0	**Interrupt Status**
2:0	RO	0	**Reserved**

Offset Address: 08h (D12F0)
Revision ID **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	**Revision ID**

Offset Address: 0B-09h (D12F0)
Class Code **Default Value: 08 0501h**

Bit	Attribute	Default	Description
23:0	RO	080501h	**Class Code**

Offset Address: 0C-0Dh (D12F0) – Reserved

Offset Address: 0Eh (D12F0)
Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type**

Offset Address: 0Fh (D12F0) – Reserved

Offset Address: 13-10h (D12F0)
SDIO Slot 1 Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**Base Address**
7:1	RO	0	**Fixed at 0.**
0	RO	0	**Space Indicator** Set to 0 if mapped to the memory space

Offset Address: 17-14h (D12F0)
SDIO Slot 2 Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**Base Address**
7:1	RO	0	**Fixed at 0.**
0	RO	0	**Space Indicator** Set to 0 if mapped to the memory space

Offset Address: 18-2Bh (D12F0) – Reserved

Offset Address: 2D-2Ch (D12F0)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D12F0)
Subsystem ID **Default Value: 95D0h**

Bit	Attribute	Default	Description
15:0	RO	95D0h	**Subsystem ID**

Offset Address: 30-33h (D12F0) – Reserved

Offset Address: 34h (D12F0)
Capabilities Pointer **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Capabilities Pointer** Point to the power management capability

Offset Address: 35-3Bh (D12F0) – Reserved

Offset Address: 3Ch (D12F0)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Interrupt Line**

Offset Address: 3Dh (D12F0)
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin**

Offset Address: 3E-3Fh (D12F0) – Reserved

PCI Device Specific Registers (40-FFh)

Offset Address: 40h (D12F0)
Slot Information **Default Value: 10h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RO	001b	**Number of Slots** 000: One slot 001: Two slots
3	RO	0	**Reserved**
2:0	RO	0	**First Base Address Register Number**

Offset Address: 41-7Fh (D12F0) – Reserved

Offset Address: 81-80h (D12F0)

PCI Power Management Capabilities ID **Default Value: 0001h**

Bit	Attribute	Default	Description
15:8	RO	0	**Point to the Next Capability Structure**
7:0	RO	01h	**PCI Power Management Capability**

Offset Address: 83-82h (D12F0)

PCI Power Management Capabilities **Default Value: FFC2h**

Bit	Attribute	Default	Description
15:11	RO	1Fh	**PME Can Be Generated from D3 and D0 State**
10	RO	1b	**D2 State Support** 0: Not supported 1: Supported
9	RO	1b	**D1 State Support** 0: Not supported 1: Supported
8:6	RO	111b	**Report D3 Max Suspend Current** 111b indicates 375mA required.
5	RO	0	**No Device-Specific Initialization is Required**
4	RO	0	**Reserved**
3	RO	0	**Hardwired to 0**
2:0	RO	010b	**Support PCI Power 1.1 Specific**

Offset Address: 87-84h (D12F0)

Power Management Control and Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:22	RO	0	**Hardwired to 0**
21:16	RO	0	**Reserved**
15	RW1C RSM	0	**PME Status** This bit is set when the SDIO Host Controller would assert the PME# independent of the state of bit 8. This bit is in resume well.
14:9	RO	0	**Reserved**
8	RWS RSM	0	**Enable PME** Enable PME wake up if bit 15 is set. This bit is in resume well
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** This field is used both to determinate the current power state and to set a new power state. 00: D0 01: D1 10: D2 11: D3 If software attempts to write an unsupported, optional state to this field, the write operation will complete normally on the bus; however, the data is discarded and no state change occurs.

Offset Address: 8B-88h (D12F0)

SDIO Host Capabilities **Default Value: 0560 0181h**

Bit	Attribute	Default	Description
31:27	RO	0	**Reserved**
26	RW	1b	**Voltage Support 1.8v** 0: Not supported 1: Supported
25	RO	0	**Reserved**
24	RW	1b	**Voltage Support 3.3v** 0: Not supported 1: Supported
23	RW	0b	**Suspend / Resume Support** 0: Not supported 1: Supported
22	RW	1b	**DMA Support** 0: Not supported 1: Supported
21	RW	1b	**High Speed Support** 0: Not supported 1: Supported
20:18	RO	0	**Reserved**
17:16	RW	00b	**Max Block Length** 00: 512 bytes 01: 1024 bytes (not supported) 10: 2048 bytes (not supported) 11: Reserved
15:9	RO	0	**Reserved**
8	RW	1b	**Base Clock Frequency For SD Clock** 0: 33MHz 1: 48MHz
7	RW	1b	**Timeout Clock Unit** 0: KHz (Not supported) 1: MHz
6:1	RO	0	**Reserved**
0	RW	1b	**Timeout Clock Frequency** 0: 33MHz 1: 48MHz Must ensure the setting is the same as bit 8.

Offset Address: 8Ch (D12F0)

SDIO Host Capabilities **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Slot2 Receiving Logic Clock Enable**
6	RW	0	**Slot1 Receiving Logic Clock Enable**
5:4	RW	00b	**Slot 2 SDCLK (**SDIO1CLK**) Latency** 00: Bypass mode 01: Delay Line mode 1 10: Delay Line mode 2 11: Delay Line mode 3
3:2	RW	00b	**Slot 1 SDCLK (**SDIO0CLK**) Latency** 00: Bypass mode 01: Delay Line mode 1 10: Delay Line mode 2 11: Delay Line mode 3
1	RW	0	**Slot 2 Data Output Bus Timing at Transmitting Data under High Speed** 0: Rising Trigger 1: Falling Trigger
0	RW	0	**Slot 1 Data Output Bus Timing at Transmitting Data under High Speed** 0: Rising Trigger 1: Falling Trigger

Offset Address: 8Dh (D12F0)
SDIO Host Capabilities 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Slot 2 Receiver Delay Clock Select** 0: 2-clock period 1: 3-clock period
1	RW	0	**Slot 1 Receiver Delay Clock Select** This register is used to control how to generate read wait signal and stop clock. 0: 2-clock period 1: 3-clock period
0	RW	0	**Receiving Logic Control** 0: Enable 1: Disable. Bypass receiving logic

Offset Address: 8Eh (D12F0)
SDIO Host Capabilities 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Debug Port Select** 0: Host controller 1: DMA buffer

Offset Address: 8F (D12F0) – Reserved

Offset Address: 93-90h (D12F0)
SDIO Host Debug Signals - High DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**SDIO Host Debug Signals - High DW**

Offset Address: 97-94h (D12F0)
SDIO Host Debug Signals - Low DW **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**SDIO Host Debug Signals - Low DW**

Offset Address: 98h (D12F0)
SDIO Host Capabilities 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**Command Conflict Judge Feature** 0: Enable 1: Disable
2	RW	0	**Reserved**
1:0	RW	0	**De-bouncing Time Select** 00: 0.5 sec 01: 1 sec 10: 2 sec 11: Reserved

Offset Address: 99h (D12F0)

SDIO Host Capabilities 4 **Default Value: FCh**

Bit	Attribute	Default	Description
7	RW	1b	**Enable Dynamic Clock for PCI Configuration Clock** 0: Disable 1: Enable
6	RW	1b	**Enable Dynamic Clock for North-South Module Interface Path Clock of Slot 1** 0: Disable 1: Enable
5	RW	1b	**Enable Dynamic Clock for North-South Module Interface Path Clock of Slot 2** 0: Disable 1: Enable
4	RW	1b	**Enable Dynamic Clock for SDIO Host Controller Slot 1** 0: Disable 1: Enable
3	RW	1b	**Enable Dynamic Clock for SDIO Host Controller Slot 2** 0: Disable 1: Enable
2	RW	1b	**Second Slot of SDIO Card Support** 0: One slot 1: Two slots
1:0	RO	0	**Reserved**

Offset Address: 9A-FFh (D12F0) – Reserved

SDIO Host Standard Registers (00-FFh)

This section describes memory mapped I/O registers. Please refer to SD Host Controller Standard Specification 1.0 for details.

The following attributes are implemented specifically in the SDIO host standard registers.

ROC: Read-only status. These bits are initialized to zero at reset. Writes to these bits are ignored
RWAC: Read-Write, automatic clear register. The Host Controllers shall clear the bit automatically when the operation is completed. Writing a 0 to RWAC bits has no effect.

Offset Address: 03-00h (SDIO-MMIO)

DMA System Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**DMA System Address**

Offset Address: 05-04h (SDIO-MMIO)

Data Block Size **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14:12	RW	000b	**Host DMA Buffer Boundary** 000: 4K Bytes (Detects A11 carry out) 001: 8K Bytes (Detects A12 carry out) 010: 16K Bytes (Detects A13 carry out) 011: 32K Bytes (Detects A14 carry out) 100: 64K Bytes (Detects A15 carry out) 101: 128K Bytes (Detects A16 carry out) 110: 256K Bytes (Detects A17 carry out) 111: 512K Bytes (Detects A18 carry out)
11:0	RW	0000h	**Transfer Block Size** These bits specify the block size for block data transfers for CMD17, CMD18, CMD24, CMD25 and CMD53. 0000: No data transfer 0001: 1 Byte 0002: 2 Bytes 0003: 3 Bytes 0004: 4 Bytes …… 01FF: 511 Bytes 0200: 512 Bytes …… 0800: 2048 Bytes

Offset Address: 07-06h (SDIO-MMIO)

Block Count Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0000h	**Block Count for Current Transfer** This bit is enabled when Block Count Enable (bit 1) in the Transfer Mode Register (Rx0C) is set to 1 and is valid only for multiple black transfers. 0000h: Stop Count 0001h: 1 block 0002h: 2 blocks …… FFFFh: 65535 blocks

Offset Address: 0B-08h (SDIO-MMIO)

Command Argument **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Command Argument**

Offset Address: 0D-0Ch (SDIO-MMIO)

Data Transfer Mode **Default Value: 0000h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RW	0	**Multi / Single Block Select** 0: Single Block 1: Multiple Block
4	RW	0	**Data Transfer Direction Select** 0: Write (Host to Card) 1: Read (Card to Host)
3	RO	0	**Reserved**
2	RW	0	**Enable Auto CMD12** 0: Disable 1: Enable
1	RW	0	**Enable Block Count** 0: Disable 1: Enable
0	RW	0	**Enable DMA** This bit can be enabled only when DMA is supported (SDIO-MMIO Rx40[22]=1) 0: Disable 1: Enable

Table 22. Determination of Transfer Type

Rx0C[5] (Multi/Single Block Select)	Rx0C[1] (Block Count Enable)	Rx07-06 (Block Count)	Function
0	Don't care	Don't care	Single Transfer
1	0	Don't care	Infinite Transfer
1	1	Not Zero	Multiple Transfer
1	1	Zero	Stop Multiple Transfer

Offset Address: 0F-0Eh (SDIO-MMIO)

Command Register **Default Value: 0000h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13:8	RW	0	**Command Index**
7:6	RW	00b	**Command Type** 00: Normal (Other commands) 01: Suspend (CMD52 for writing "Bus Suspend" in CCCR) 10: Resume (CMD52 for writing "Function Select" in CCCR) 11: Abort (CMD12, CMD52 for writing "I/O Abort" in CCCR) Note: CCCR (Card Common Control Register)
5	RW	0	**Data Present Select** 0: No data present 1: Data present
4	RW	0	**Enable Command Index Check** 0: Disable 1: Enable
3	RW	0	**Enable Command CRC (Cyclic Redundancy Check) Check** 0: Disable 1: Enable
2	RO	0	**Reserved**
1:0	RW	00b	**Response Type Select** 00: No Response 01: Response length 136 10: Response length 48 11: Response length 48 check Busy after response

Offset Address: 1F-10h (SDIO-MMIO)

Command Response **Default Value: 0**

Bit	Attribute	Default	Description
127:0	ROC	0	**Command Response**

Offset Address: 23-20h (SDIO-MMIO)

Buffer Data Port **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Buffer Data** The Host Controller buffer can be accessed through this 32-bit data port register.

Offset Address: 27-24h (SDIO-MMIO)

Present State **Default Value: 01F2 0000h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24	RO	1b	**CMD Line (**SDIO[1:0]CMD#**) Signal Level**
23:20	RO	Fh	**DAT Line (**SDIO[1:0]D[3:0]**) Signal Level**
19	RO	0	**Write Protect Signal Level** 0: Write protected (SDIO[1:0]WPD# = 0) 1: Write enabled (SDIO[1:0]WPD# = 1)
18	RO	0	**Card Detect Signal Level** 0: No card present (SDIO[1:0]CD# = 1) 1: Card present (SDIO[1:0]CD# = 0)
17	RO	1b	**Card State Stable** 0: Reset or de-bouncing 1: No card or inserted
16	RO	0	**Card Inserted** 0: Reset or de-bouncing or no card 1: Card inserted
15:12	RO	0	**Reserved**
11	ROC	0	**Enable Buffer Read** This status is used for non-DMA read transfers. 0: Read disable 1: Read enable
10	ROC	0	**Enable Buffer Write** This status is used for non-DMA write transfers. 0: Write disable 1: Write enable
9	ROC	0	**Read Transfer Active** 0: No valid data 1: Transferring data
8	ROC	0	**Write Transfer Active** 0: No valid data 1: Transferring data
7:3	RO	0	**Reserved**
2	ROC	0	**DAT Line Active** This bit indicates whether one of the data lines on SD Bus is in use. 0: DAT line inactive 1: DAT line active
1	ROC	0	**Command Inhibit for DAT Line** 0: Can issue command using the DAT line 1: Cannot issue command using the DAT line
0	ROC	0	**Command Inhibit for CMD Line** 0: Can issue command using only the CMD line 1: Cannot issue command

Offset Address: 28h (SDIO-MMIO)

Host Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Enable High Speed** 0: Normal speed mode 1: High speed mode
1	RW	0	**Data Transfer Width** 0: 1-bit mode 1: 4-bit mode
0	RW	0	**LED Control** 0: LED off 1: LED on

Offset Address: 29h (SDIO-MMIO)

Power Control **Default Value: 0Eh**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:1	RW	111b	**SD Bus Voltage Select** 000-100: Reserved 101: 1.8V 110: 3.0V (not supported) 111: 3.3V
0	RW	0	**SD Bus Power** 0: Power off 1: Power on

Offset Address: 2Ah (SDIO-MMIO)

Block Gap Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Interrupt at Block Gap** 0: Disable 1: Enable
2	RW	0	**Read Wait Control** 0: Disable 1: Enable
1	RWAC	0	**Continue Request** 0: Not affect 1: Restart
0	RW	0	**Stop at Block Gap Request** 0: Transfer 1: Stop

Offset Address: 2Bh (SDIO-MMIO)

Wakeup Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Enable Wakeup Event on SD Card Removal** 0: Disable 1: Enable
1	RW	0	**Enable Wakeup Event on SD Card Insertion** 0: Disable 1: Enable
0	RW	0	**Enable Wakeup Event on Card Interrupt** 0: Disable 1: Enable

Offset Address: 2D-2Ch (SDIO-MMIO)

Clock Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RW	00h	**SDCLK (**SDIO[1:0]CLK**) Frequency Select** 00h: Base clock (10MHz-63MHz) 01h: Base clock divided by 2 02h: Base clock divided by 4 04h: Base clock divided by 8 08h: Base clock divided by 16 10h: Base clock divided by 32 20h: Base clock divided by 64 40h: Base clock divided by 128 80h: Base clock divided by 256 Others: Reserved
7:3	RO	0	**Reserved**
2	RW	0	**Enable SD Clock** 0: Disable 1: Enable (This bit is effective when the card is in the slot.)
1	ROC	0	**Internal Clock Stable** 0: Not ready 1: Ready
0	RW	0	**Enable Internal Clock** 0: Stop 1: Oscillate

Offset Address: 2Eh (SDIO-MMIO)

Timeout Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Data Timeout Counter Value** 0000: TMCLK x 2^{13} 0001: TMCLK x 2^{14} ……. 1110: TMCLK x 2^{27} 1111: Reserved

Offset Address: 2Fh (SDIO-MMIO)

Software Reset **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RWAC	0	**Software Reset for DAT (**SDIO[1:0]D[3:0]**) Line** 0: Work 1: Reset
1	RWAC	0	**Software Reset for CMD (**SDIO[1:0]CMD#**) Line** 0: Work 1: Reset
0	RWAC	0	**Software Reset for All** 0: Work 1: Reset

Offset Address: 31-30h (SDIO-MMIO)

Normal Interrupt Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	ROC	0	**Error Interrupt** 0: No Error 1: Error
14:9	RO	0	**Reserved**
8	ROC	0	**Card Interrupt** 0: No card interrupt 1: Generate card interrupt
7	RW1C	0	**Card Removal** 0: Card state stable or de-bouncing 1: Card removed
6	RW1C	0	**Card Insertion** 0: Card state stable or de-bouncing 1: Card inserted
5	RW1C	0	**Buffer Read Ready** 0: Not ready to read buffer 1: Ready to read buffer
4	RW1C	0	**Buffer Write Ready** 0: Not ready to write buffer 1: Ready to write buffer
3	RW1C	0	**DMA Interrupt** 0: No DMA interrupt 1: DMA interrupt is generated
2	RW1C	0	**Block Gap Event** 0: No block gap event 1: Transaction stopped at block gap
1	RW1C	0	**Transfer Complete** 0:No transfer complete 1: Data transfer complete
0	RW1C	0	**Command Complete** 0: No command complete 1: Command complete

Offset Address: 33-32h (SDIO-MMIO)

Error Interrupt Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RW1C	0	**Vendor Specific Error Status**
11:9	RO	0	**Reserved**
8	RW1C	0	**Auto CMD12 Error** 0: No error 1: Error
7	RW1C	0	**Current Limit Error** 0: No error. The host controller is supplying power. 1: Power fail. The host controller is not supplying power to SD card.
6	RW1C	0	**Data End Bit Error** 0: No error 1: Error
5	RW1C	0	**Data CRC Error** 0: No error 1: Error
4	RW1C	0	**Data Timeout Error** 0: No error 1: Time out
3	RW1C	0	**Command Index Error** 0: No error 1: Error
2	RW1C	0	**Command End Bit Error** 0: No error 1: End bit error generated
1	RW1C	0	**Command CRC Error** 0: No error 1: CRC error generated
0	RW1C	0	**Command Timeout Error** 0: No error 1: Time out

Offset Address: 35-34h (SDIO-MMIO)

Enable Normal Interrupt Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Fixed at 0**
14:9	RO	0	**Reserved**
8	RW	0	**Enable Card Interrupt Status** 0: Mask 1: Enable
7	RW	0	**Enable Card Removal Status** 0: Mask 1: Enable
6	RW	0	**Enable Card Insertion Status** 0: Mask 1: Enable
5	RW	0	**Enable Buffer Read Ready Status** 0: Mask 1: Enable
4	RW	0	**Enable Buffer Write Ready Status** 0: Mask 1: Enable
3	RW	0	**Enable DMA Interrupt Status** 0: Mask 1: Enable
2	RW	0	**Enable Block Gap Event Status** 0: Mask 1: Enable
1	RW	0	**Enable Transfer Complete Status** 0: Mask 1: Enable
0	RW	0	**Enable Command Complete Status** 0: Mask 1: Enable

Offset Address: 37-36h (SDIO-MMIO)

Enable Error Interrupt Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RW	0	**Enable Vendor Specific Error Status** 0: Mask 1: Enable
11:9	RO	0	**Reserved**
8	RW	0	**Enable Auto CMD12 Error Status** 0: Mask 1: Enable
7	RW	0	**Enable Current Limit Error Status** 0: Mask 1: Enable
6	RW	0	**Enable Data End Bit Error Status** 0: Mask 1: Enable
5	RW	0	**Enable Data CRC Error Status** 0: Mask 1: Enable
4	RW	0	**Enable Data Timeout Error Status** 0: Mask 1: Enable
3	RW	0	**Enable Command Index Error Status** 0: Mask 1: Enable
2	RW	0	**Enable Command End Bit Error Status** 0: Mask 1: Enable
1	RW	0	**Enable Command CRC Error Status** 0: Mask 1: Enable
0	RW	0	**Enable Command Timeout Error Status** 0: Mask 1: Enable

Offset Address: 39-38h (SDIO-MMIO)

Enable Normal Interrupt Signal **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Fixed at 0**
14:9	RO	0	**Reserved**
8	RW	0	**Enable Card Interrupt Signal** 0: Mask 1: Enable
7	RW	0	**Enable Card Removal Signal** 0: Mask 1: Enable
6	RW	0	**Enable Card Insertion Signal** 0: Mask 1: Enable
5	RW	0	**Enable Buffer Read Ready Signal** 0: Mask 1: Enable
4	RW	0	**Enable Buffer Write Ready Signal** 0: Mask 1: Enable
3	RW	0	**Enable DMA Interrupt Signal** 0: Mask 1: Enable
2	RW	0	**Enable Block Gap Event Signal** 0: Mask 1: Enable
1	RW	0	**Enable Transfer Complete Signal** 0: Mask 1: Enable
0	RW	0	**Enable Command Complete Signal** 0: Mask 1: Enable

Offset Address: 3B-3Ah (SDIO-MMIO)

Enable Error Interrupt Signal **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RW	0	**Enable Vendor Specific Error Signal** 0: Mask 1: Enable
11:9	RO	0	**Reserved**
8	RW	0	**Enable Auto CMD12 Error Signal** 0: Mask 1: Enable
7	RW	0	**Enable Current Limit Error Signal** 0: Mask 1: Enable
6	RW	0	**Enable Data End Bit Error Signal** 0: Mask 1: Enable
5	RW	0	**Enable Data CRC Error Signal** 0: Mask 1: Enable
4	RW	0	**Enable Data Timeout Error Signal** 0: Mask 1: Enable
3	RW	0	**Enable Command Index Error Signal** 0: Mask 1: Enable
2	RW	0	**Enable Command End Bit Error Signal** 0: Mask 1: Enable
1	RW	0	**Enable Command CRC Error Signal** 0: Mask 1: Enable
0	RW	0	**Enable Command Timeout Error Signal** 0: Mask 1: Enable

Offset Address: 3D-3Ch (SDIO-MMIO)

Auto CMD12 Error Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7	ROC	0	**Command Not Issued by Auto CMD12 Error** 0: No error 1: Command not issued
6:5	RO	0	**Reserved**
4	ROC	0	**Auto CMD12 Index Error** 0: No error 1: Error
3	ROC	0	**Auto CMD12 End Bit Error** 0: No error 1: End bit error generated
2	ROC	0	**Auto CMD12 CRC Error** 0: No error 1: CRC error generated
1	ROC	0	**Auto CMD12 Timeout Error** 0: No error 1: Timeout
0	ROC	0	**Auto CMD12 Not Executed** 0: Executed 1: Not executed

Offset Address: 47-40h (SDIO-MMIO)

Capabilities Register **Default Value: 0000 0000 0560 30B0h**

Bit	Attribute	Default	Description
63:32	RO	0	**Reserved**
31:27	RO	0	**Reserved** Reserved for voltage support.
26	RO	1b	**Voltage Support 1.8V** 0: Not supported 1: Supported
25	RO	0	**Voltage Support 3.0V** 0: Not supported 1: Supported
24	RO	1b	**Voltage Support 3.3V** 0: Not supported 1: Supported
23	RO	0	**Suspend / Resume Support** 0: Not supported 1: Supported
22	RO	1b	**DMA Support** 0: DMA not supported 1: DMA supported
21	RO	1b	**High Speed Support** 0: High speed not supported 1: High speed supported
20:18	RO	0	**Reserved**
17:16	RO	00b	**Max Block Length** 00: 512 bytes 01: 1024 bytes 10: 2048 bytes 11: Reserved
15:14	RO	0	**Reserved**
13:8	RO	110000b	**Base Clock Frequency for SD Clock** 0: Get information via another method Not 0: 1MHz to 63MHz
7	RO	1b	**Timeout Clock Unit** 0: KHz 1: MHz
6	RO	0	**Reserved**
5:0	RO	110000b	**Timeout Clock Frequency** These bits indicate the base clock frequency for Data Timeout Error. 0: Get information via another method Not 0: 1KHz to 63KHz or 1MHz to 63MHz

Offset Address: 4F-48h (SDIO-MMIO)

Maximum Current Capabilities **Default Value: 0000 0000 00F0 01F0h**

Bit	Attribute	Default	Description
63:24	RO	0	**Reserved**
23:16	RO	F0h	**Maximum Current for 1.8V** 0: Get information via another method 1: 4 mA 2: 8 mA 3: 12 mA …… 255: 1020 mA:
15:8	RO	01h	**Maximum Current for 3.0V**
7:0	RO	F0h	**Maximum Current for 3.3V**

Offset Address: FD-FCh (SDIO-MMIO)

Slot Interrupt Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:0	RO	0	**Interrupt Signal for Each Slot** Bit [n] is for Slot [n] (n = 0 ~ 7).

Offset Address: FF-FEh (SDIO-MMIO)

Host Controller Version **Default Value: 0000h**

Bit	Attribute	Default	Description
15:8	RO	0	**Vendor Version Number**
7:0	RO	0	**Specification Version Number** 00h: SD Host Specification Version 1.0 Others: Reserved

IrDA Host Controller I/O Space Registers

These registers are located in the I/O address space at offsets from the "FIR I/O Address Base" located in D17F0 RxB6.

I/O Offset: 10h (IrDA-IO)

Infrared Mode Configuration - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CRC** 0: 32-bit CRC 1: 16-bit CRC
6	RW	0	**FIR Mode** 0: Disable 1: Enable
5	RW	0	**MIR Mode** 0: Disable 1: Enable
4	RW	0	**SIR Mode** 0: Disable 1: Enable
3	RW	0	**Receive SIR Byte Filter** 0: Disable 1: Enable (if SIR mode bit is set)
2	RW	0	**SIR Test Mode** 0: Disable 1: Enable (allow SIR filter to be used when it is not in SIR mode)
1	RW	0	**Tx LED Output Inversion (IRTX Pin)** 0: Do not Invert 1: Invert
0	RW	0	**Rx LED Input Inversion (IRRX Pin)** 0: Do not Invert 1: Invert

I/O Offset: 11h (IrDA-IO)

Infrared Mode Configuration - High **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**FIFO Size Selection** See descriptions in bit 0
6	RO	0	**Reserved**
5	RW	0	**VFIR Mode** 0: Disable 1: Enable (enables the VFIR mode 16Mbit/s)
4	RW	0	**Physical Layer Transmitter** 0: Disable 1: Enable
3	RW	0	**Physical Layer Receiver** 0: Disable 1: Enable. If the transmitter is active (bit 4 is set to 1), loopback must be enabled; otherwise, the receiver will not be enabled even if this bit is set.
2	RW	0	**Memory Access through ISA DMA Controller** 0: Disable 1: Enable
1	RW	0	**Receive Small / Runtime Packets (<4 Bytes) (SIR Mode Only)** 0: Disable 1: Enable
0	RW	0	**FIFO Size Selection** **Bit 7** / **Bit 0** / **FIFO Size** 0 / 0 / 64 Bytes 0 / 1 / 32 Bytes 1 / 0 / 128 Bytes 1 / 1 / Reserved

I/O Offset: 12h (IrDA-IO)
Infrared SIR BOF **Default Value: C0h**

Bit	Attribute	Default	Description
7:0	RW	C0h	**SIR Format Begin-of-Frame**

I/O Offset: 13h (IrDA-IO)
Infrared SIR EOF **Default Value: C1h**

Bit	Attribute	Default	Description
7:0	RW	C1h	**SIR Format End of Frame**

I/O Offset: 14h (IrDA-IO)
Infrared Status - High **Default Value: 26h**

Bit	Attribute	Default	Description
7:1	RO	13h	**Reserved** (Do not program)
0	RO	0	**Valid VFIR Configuration** Indicates a valid VFIR configuration when this bit is set to 1. 0: Not valid 1: Valid

I/O Offset: 15h (IrDA-IO)
Infrared Status and Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Physical Layer Interface and Clock Generation Circuits** 0: Disable 1: Enable
6	RO	0	**Configuration Error** 0: No error 1: More than one mode selected
5	RO	0	**FIR On** 0: FIR not configured 1: Valid FIR configuration
4	RO	0	**MIR On** 0: MIR not configured 1: Valid MIR configuration
3	RO	0	**SIR On** 0: SIR not configured 1: Valid SIR configuration
2	RO	0	**Physical Layer Transmitter** 0: Disable 1: Enable
1	RO	0	**Physical Layer Receiver** 0: Disable 1: Enable
0	RO	0	**16-bit CRC** 0: 32-bit CRC 1: 16-bit CRC

I/O Offset: 16h (IrDA-IO)
Infrared Status 1 - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**SIR / Indication Pulse Width [2:0]**
4:0	RO	0	**MIR Start / FIR Preamble Bytes to Send** MIR: Number of start flags plus one (0 = 1 Byte) FIR: Number of preamble bytes plus one (0 = 1 Byte)

I/O Offset: 17h (IrDA-IO)
Infrared Status 1 - High **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Baud Rate [5:0]**
1:0	RO	0	**SIR / Indication Pulse Width [4:3]**

I/O Offset: 18h (IrDA-IO)

Infrared Packet Configuration - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RW	0	**SIR / Indication Pulse Width [2:0]**
4:0	RW	0	**MIR Start / FIR Preamble Bytes to Send** MIR: Number of start flags plus one (0 = 1 Byte) FIR: Number of preamble bytes plus one (0 = 1 Byte)

I/O Offset: 19h (IrDA-IO)

Infrared Packet Configuration - High **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**Baud Rate [5:0]**
1:0	RW	0	**SIR / Indication Pulse Width [4:3]**

Table 23. Programming Values for I/O Registers at Offset 16-19h

Mode	Baud Rate	Pulse Width			Preamble
		Min	Nom	Max	
SIR (2400)	47	0	12	12	Don't Care
SIR (9600)	11	0	12	12	Don't Care
SIR (19200)	5	1	12	12	Don't Care
SIR (38400)	2	3	12	14	Don't Care
SIR (57600)	1	5	12	16	Don't Care
SIR (115200)	0	11	12	20	Don't Care
MIR	0	8			1
FIR	0	Don't Care			14

I/O Offset: 1B-1Ah (IrDA-IO)

Infrared Packet Length Configuration **Default Value: 0000h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved**
12:8	RW	0	**Max Receive Packet Length [12:8]** (In unit of Bytes)
7:0	RW	0	**Max Receive Packet Length [7:0]** (In unit of Bytes)

I/O Offset: 1Eh (IrDA-IO)

Infrared Property Configuration **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**FIR Adjustment Filter Rate** 00: High filter 01: Medium high filter 10: Medium low filter 11: Low filter
5	RW	0	**FIR Adjacent Pulse Width Packet Circuit** 0: Enable 1: Disable
4	RW	0	**FIR Pulse Width Adjustment Circuit** 0: Enable 1: Disable
3:2	RO	0	**Reserved**
1	RW	0	**Number of Receive Paths** 0: 1 receive & 1 output pin (slow or fast) 1: 2 receive paths
0	RW	0	**Optical Module Mode Pin Polarity** (1 Receive Path) 0: Low signal select slow speed 1: High signal selects slow speed

I/O Offset: 20h (IrDA-IO)

IR Host Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Interrupt Enable** 0: Disable 1: Enable
6	WO	0	**Transmit Start** Writing a 1 to this bit initiates execution of the IR transmit mode programmed in the IR configuration registers. DMA and all necessary registers must be set up prior to writing a 1 to this register. Writing 0 has no effect. This bit always reads 0; I/O Offset 21h[0] can be used to determine when the IR Host Controller has finished executing the transmission.
5	WO	0	**Receive Start** Writing a 1 to this bit initiates execution of the IR receive mode programmed in the IR configuration registers. DMA and all necessary registers must be set up prior to writing a 1 to this register. Writing 0 has no effect. This bit always reads 0; I/O Offset 21h[0] can be used to determine when the IR Host Controller has finished executing the reception.
4	RW	0	**Interrupt Clear** 0: Disable interrupt output 1: Enable interrupt output
3:0	RO	0	**Reserved**

I/O Offset: 21h (IrDA-IO)

IR Host Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RO	0	**Timer Interrupt Pending** 0: Timer interrupt not pending 1: Timer interrupt pending
5	RO	0	**Transmit Interrupt Pending** 0: Timer interrupt not pending 1: Timer interrupt pending
4	RO	0	**Receive Interrupt Pending** 0: Timer interrupt not pending 1: Timer interrupt pending The following conditions clear this interrupt. 1) Reading the receive ring packet counter low register 2) Issuing a reset receive special condition interrupt 3) Hardware reset 4) Software reset
3:1	RO	0	**Interrupt Identification** This code provides an alternative method for identifying the interrupt source by indicating the interrupt type and priority level.
0	RO	0	**IR Host Controller Busy** 0: IR Controller host interface is not processing a transaction 1: IR Controller host interface is in the process of completing any receive or transmit transaction (no other registers should be accessed)

Bits[3:1]	Priority	Interrupt Type
0xx	N/A	Reserved
100	Highest	Receive special condition – FIFO overrun, CRC error, End of packet (EOF), PHY error, Maximum length, SIR bad
101	Second	Receive data available
110	Third	Transmit buffer empty
111	Fourth	Transmit special condition – FIFO underrun, EOM, Early EOM

I/O Offset: 22h (IrDA-IO)

Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Transmit DMA Enable** 0: Disable transmit DMA channel 1: Enable DREQB as transmit DMA channel if FIR dual DMA channel is selected (D17F0 RxB0[1] = 0).
6	RW	0	**Receive DMA Enable** 0: Disable receive DMA channel. DREQA is used also for transmit if FIR single DMA channel is selected (D17F0 RxB0[1] =1) and "Transmit DMA Enable"(bit 7) is set to 1. 1: Enable DREQA as receive DMA channel if FIR single DMA channel is selected.
5	RW	0	**Swap DMA Channels** 0: Normal DREQA/B 1: Swap DREQA and DREQB
4	RW	0	**Physical Layer Internal Loopback** 0: Disable 1: Enable
3	RW	0	**Transmit on Loopback** 0: Disable 1: Enable transmission to LED when bit 4 is set to 1
2:0	RO	0	**Reserved**

I/O Offset: 23h (IrDA-IO)

Transmit Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Transmit FIFO Ready Interrupt** 0: Disable 1: Enable interrupt when FIFO reaches threshold. See bit [4:3] for detail.
5	RW	0	**Transmit FIFO Underrun/EOM Interrupt** 0: Disable 1: Enable interrupt on underrun or EOM
4:3	RW	00b	**Transmit FIFO Threshold Level** The transmit FIFO ready interrupt will be triggered when bit 6 is set to 1 and the threshold is lower than the setting level. 00: Full. The FIFO size depends on I/O Offset 11h bit 7 and bit 0 01: 3/4 10: 1/2 11: 1/4
2:0	RO	0	**Reserved**

I/O Offset: 24h (IrDA-IO)

Transmit Control 2 **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**Force Underrun** Write 1 to force an underrun on this packet (for testing). For an underrun to occur, the transmit count should be greater than 18 bytes. This bit will be cleared by hardware when the packet has been transmitted.
6	RW	1b	**Transmit CRC** 0: Disable (for SIR mode or bridging applications where CRC should not be generated by hardware) 1: Enable for synchronous packets. This bit will be cleared by hardware when the packet has been transmitted.
5	RW	0	**Bad CRC** Write 1 to send inverted or bad CRC to allow test of CRC verification hardware by the receiver. This bit will be cleared by hardware when the packet has been transmitted.
4	RW	0	**Need Pulse** Write 1 to transmit an indication pulse after this packet has been transmitted. This bit will be cleared by hardware when the packet has been transmitted.
3	RW	0	**Request to Clear "Transmit Enable" Bit** Write 1 to clear the "Enable Transmit" bit (I/O Offset 11h[4]) after this packet has been transmitted. Should be set on the last packet of a transmit sequence.
2:0	RW	000b	**Early EOM Interrupt Level** This field specifies the number of bytes that must remain in the Transmit Byte Count before an Early EOM interrupt is generated. The reason for having an interrupt occur before transmission is actually completed is to allow enough time for software to enter the proper interrupt handler routine, turn the DMA channel around for reception (Singe DMA mode), and prepare for another back-to-back transmission. Once in the interrupt handler routine, software can poll the EOM bit in the Transmit Status register to determine exactly when the transmission ends. 000: Interrupt by EOM 001: EOM interrupt occurs when the remaining count is 16 010: EOM interrupt occurs when the remaining count is 32 011: EOM interrupt occurs when the remaining count is 64 100: EOM interrupt occurs when the remaining count is 128 101: EOM interrupt occurs when the remaining count is 256 110: EOM interrupt occurs when the remaining count is 512 111: EOM interrupt occurs when the remaining count is 1024

I/O Offset: 25h (IrDA-IO)

Transmit Status **Default Value: 02h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RO	0	**Transmit FIFO Underrun** 1 indicates that the transmit FIFO ran out of data before the transmitter could finish transmitting all the data (i.e., transmit FIFO empty and a transmit byte count value greater than zero). This bit must be reset by an explicit FIFO underrun / EOM latch command.
2	RO	0	**End Of Message (EOM)** 1 indicates transmission completed successfully. The EOM interrupt occurs immediately after the CRC and ending flag have been transmitted. This bit is reset by reading the transmit status register or by a Reset FIFO underrun / EOM latch command from the reset command register.
1	RO	1b	**Transmit FIFO Ready** 1 indicates that the transmit FIFO is ready for more data transfers. When I/O Offset 23[6] is set to 1, an interrupt is generated when this condition becomes true.
0	RO	0	**Early End Of Message** 1 indicates that the transmit byte count has reached the level set by the early EOM interrupt level (I/O Offset 24[2:0]). This bit is cleared by reading the transmit status register.

I/O Offset: 26h (IrDA-IO)

Receive Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**Receive FIFO Threshold Level** The receive FIFO Ready Interrupt will be triggered when bit 1 is set to 1 and the Receive FIFO level reaches the following settings: 00: Full Level 01: 1/ 4 Level. The FIFO size depends on I/O Offset 11h bit 7 and bit 0 10: 1/2 11: 3/4
5:4	RW	00b	**Receive Address Mode** Specifies the type of address filtering to apply for determining which receive packets to accept. 00: All packets are received and no filtering applied 01: Packets with addresses that match the address setting in bit[7:1] of the Address Registers (I/O Offset 29h) will be received 10: Packets with addresses that match the address setting in bit[7:4] of the Address Registers will be received. 11: Packets with addresses that match the address setting in bit[7:0] of the Address Register will be received.
3:2	RO	0	**Reserved**
1	RW	0	**Receive FIFO Ready Interrupt** 0: Disable 1: Enable interrupt on receive FIFO ready
0	RW	0	**Receive FIFO Special Condition Interrupt** 0: Disable 1: Enable interrupt on overrun, CRC error, End of Packet (EOP), PHY error (physical layer detected an encoding error), max length exceeded (the maximum length packet is encountered), or SIR bad

I/O Offset: 27h (IrDA-IO)

Receive Status **Default Value: 02h**

Bit	Attribute	Default	Description
7	RO	0	**PHY Error** 1 indicates that the physical layer has detected an encoding error. This bit is automatically cleared upon detection of the ending / stop flag of the next incoming packet.
6	RO	0	**CRC Error** 1 indicates that a CRC error was detected on an incoming packet. CRC values are checked against known constants for either 16 or 32 bits depending on the length chosen in I/O offset 10h. Valid for MIR and FIR modes only. This bit is automatically cleared upon detection of the ending / stop flag of the next incoming packet.
5	RO	0	**FIFO Overrun Interrupt** 1 indicates that the Receive FIFO overflowed. This bit is cleared by a Reset Receive Special Condition Interrupt command from the Reset Command register (I/O Offset 28h).
4	RO	0	**EOP (End Of Packet)** 1 indicates reception of a complete packet. This bit is automatically cleared upon detection of the start flag of the next incoming packet.
3	RO	0	**Receive Data Available** 0: Receive FIFO empty 1: Receive FIFO not empty (i.e., FIFO contains receive data). Does not cause an interrupt.
2	RO	0	**Reserved**
1	RO	1b	**Maximum Receive Packet Length** 1 indicates that a maximum length packet was encountered. For SIR, this means that the packet was closed and another will be opened without any data being truncated. In other modes, once the maximum length is reached, no other data will be received. This bit is automatically cleared upon detection of the start flag of the next incoming packet.
0	RO	0	**SIR Bad** 1 indicates (if the SIR filter is on) that a begin flag was seen followed by valid data, then followed by another begin flag (without an end flag). This bit is automatically cleared upon detection of the start flag of the next incoming packet.

I/O Offset: 28h (IrDA-IO)

Reset Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	WO	0000b	**Reset Command** Used to send a reset signal to the appropriate hardware in order to clear a particular status condition, clear a counter, or send a general reset. These bits are self clearing (i.e., the programmer does not have to write 0 to the Reset Command register). 0001: Reserved 0010: Reset Rx FIFO pointer 0011: Reset Rx special condition interrupt 0100: Reset Rx ring packet pointer 0101: Reset FIFO underrun / EOM latch 0110: Reset Tx FIFO pointer 0111: Software reset 1xxx: Reserved These bits always read as 0000b.
3:0	RO	0	**Reserved**

I/O Offset: 29h (IrDA-IO)

Packet Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Receive Packet Address** Specifies the address value that must be contained in the address field of incoming packets. See also the "Receive Address Mode" setting in Receive Control Register (I/O Offset 26h[5:4]).

I/O Offset: 2Ah (IrDA-IO)

Receive Byte Count - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Receive Byte Count [7:0]** Provides a running count (low-order value) of the number of bytes of data being received. This information is useful for checking if a reception is in progress and should not be used to determine packet length . RFP would be use to do this.

I/O Offset: 2Bh (IrDA-IO)

Receive Byte Count - High **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4:0	RO	0	**Receive Byte Count [12:8]** Provides a running count (high-order value) of the number of bytes of data being received. This information is useful for checking if a reception is in progress and should not be used to determine packet length. RFP would be use to do this.

I/O Offset: 2Ch (IrDA-IO)

Receive Ring Packet Pointer- Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Ring Frame Pointer[7:0]** Used in back-to-back packet reception to provide the end-of-packet pointer value (i.e., pointer to the last byte of a frame received in the receive buffer). The order of byte access to the Ring Packet Pointer is critical for obtaining a valid pointer value. The programmer must ensure that the low byte is read first, followed by the high byte.

I/O Offset: 2Dh (IrDA-IO)

Receive Ring Packet Pointer - High **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:0	RO	0	**Receive Frame Pointer[14:8]** Used in back-to-back packet reception to provide the end-of-packet pointer value (i.e., pointer to the last byte of a frame received in the receive buffer). The order of byte access to the Ring Packet Pointer is critical for obtaining a valid pointer value. The programmer must ensure that the low byte is read first, followed by the high byte.

I/O Offset: 2Eh (IrDA-IO)
Transmit Byte Count - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Transmit Byte Count [7:0]** Provides a running count of the number of bytes remaining to be transmitted. Before enabling transmission, software loads this register with the low-order byte length of the data packet. Each time the transmit FIFO is written to, the value of this counter decrements by one. When the counter reaches zero, the transmitter ceases to make DMA requests. Transmission continues until the transmit FIFO is depleted.

I/O Offset: 2Fh (IrDA-IO)
Transmit Byte Count - High **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RO	1111b	**Reserved** (Do not program)
3:0	RW	0	**Transmit Byte Count [11:8]** Provides a running count of the number of bytes remaining to be transmitted. Before enabling transmission, software loads this register with the high-order byte length of the data packet. Each time the transmit FIFO is written to, the value of this counter decrements by one. When the counter reaches zero, the transmitter ceases to make DMA requests. Transmission continues until the Transmit FIFO is depleted.

I/O Offset: 32h (IrDA-IO)
General Purpose Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Timer Target Value (W) / Current Value (R)** This counter increments every 125 usec and stops when it reaches the programmed target value. Reading this register returns the current value of the up counter. Writes set the target value and reset the counter to 0.

I/O Offset: 33h (IrDA-IO)
Infrared Timer Interrupt Configuration **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Timer Interrupt Enable** 0: Disable 1: Enable
0	RW	0	**Timer Interrupt Pending** A timer interrupt will be generated when the value of offset 32h reaches the programmed target value. Writes a 1 to this bit will clear the interrupt. 0: Not Pending 1: Pending

I/O Offset: 34h (IrDA-IO)

Infrared Transceiver Control - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**GFX GPIO Data for I/O Function** ***When read:*** The data is directly from IRSCLK pad. ***When write:*** The data is directly to IRSCLK pad.
5:4	RO	0	**Reserved**
3	RO	0	**IRRX Pin Value** Read the value from the IRRX pin.
2:1	RO	0	**Reserved**
0	RW	0	**Force IRTX** 0: IRTX pin is de-asserted 1: IRTX pin is asserted

I/O Offset: 35h (IrDA-IO)

Infrared Transceiver Control - High **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Enable IRSCLK for GFX GPIO Mode** 0: Disable 1: Enable IRSCLK as the interface signal for GFX GPIO mode. Bit 6 is for data transfer.
5:0	RO	0	**Reserved**

Device 13 Function 0 (D13F0) – Secure Digital Memory Card Controller

PCI Configuration Space Header (00-3Fh)

Offset Address: 01-00h (D13F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID Code**

Offset Address: 03-02h (D13F0)

Device ID **Default Value: 9530h**

Bit	Attribute	Default	Description
15:0	RO	9530h	**Device ID Code**

Offset Address: 05-04h (D13F0)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable** 0: Enable interrupt 1: Disable interrupt
9:3	RO	0	**Reserved**
2	RW	0	**Bus Master** 0: Never behaves as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space** 0: Does not respond to memory space access 1: Responds to memory space access
0	RW	0	**I/O Space** 0: Does not respond to I/O space access 1: Responds to I/O space access

Offset Address: 07-06h (D13F0)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RO	0	**Signaled System Error** (SERR# asserted)
13	RW1C	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** 0: No abort signaled 1: Transaction aborted by this chip.
10:9	RO	01b	**DEVSEL# Timing** Fixed at 01. 00: Fast 01: Medium 10: Slow 11: Reserved
8:5	RO	0	**Reserved**
4	RO	1b	**Support New Capability List**
3	RO	0	**Interrupt Status**
2:0	RO	0	**Reserved**

Offset Address: 08h (D13F0)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D13F0)

Class Code **Default Value: 05 0100h**

Bit	Attribute	Default	Description
23:0	RO	050100h	**Class Code**

Offset Address: 0Ch (D13F0)

Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D13F0)

Latency Timer **Default Value: 16h**

Bit	Attribute	Default	Description
7:0	RW	16h	**Latency Timer**

Offset Address: 0Eh (D13F0)

Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type**

Offset Address: 0Fh (D13F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST (Build In Self Test)** Fixed at 0.

Offset Address: 13-10h (D13F0)
Card Reader (CR) MMIO Register Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:11	RW	0	**Card Reader MMIO Register Base Address [31:11]**
10:0	RO	0	**Card Reader MMIO Register Base Address [10:0]**

Offset Address: 17-14h (D13F0)
Card Reader (CR) IO Register Base Address **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:3	RW	0	**Card Reader I/O Register Base Address [31:3]**
2:0	RO	001b	**Card Reader I/O Register Base Address [2:0]**

Offset Address: 18-2Bh (D13F0) – Reserved

Offset Address: 2D-2Ch (D13F0)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D13F0)
Subsystem ID **Default Value: 9530h**

Bit	Attribute	Default	Description
15:0	RO	9530h	**Subsystem ID**

Offset Address: 30-33h (D13F0) – Reserved

Offset Address: 34h (D13F0)
Capability Pointer **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Capability List Pointer** Fixed at 80h.

Offset Address: 35-3Bh (D13F0) – Reserved

Offset Address: 3Ch (D13F0)

Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**Interrupt Line Selection** 0000: Disable 0001: IRQ1 0010: Reserve 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: Disable 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: Disable 1110: IRQ14 1111: IRQ15

Offset Address: 3Dh (D13F0)

Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin** Fixed at 01h (INTA#).

Offset Address: 3E-3Fh (D13F0) – Reserved

PCI Card Reader - Specific Configuration Registers (40-FFh)

Offset Address: 40h (D13F0)

Card Reader Working Mode Selection **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Scatter-Gather Mode Select** 0: PIO mode 1:Scatter-Gather DMA mode

Offset Address: 41h (D13F0)

Debug Mode Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Upstream Cycle Goes to External PCI Bus** 0: Disable 1: Enable
2	RW	0	**Enable Write Debugging Code to Port 80h** 0: Disable 1: Enable
1	RW	0	**Enable Single Step Mode** When this bit is enabled, descriptors will be executed slot by slot.
0	RO	0	**Reserved**

Offset Address: 42-7Fh (D13F0) – Reserved

Offset Address: 80h (D13F0)

Power Management Capability ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Power Management Capability ID**

Offset Address: 81h (D13F0)

Next Item Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Item Pointer** Fixed at 0.

Offset Address: 83-82h (D13F0)

Power Management Capability **Default Value: FFC2h**

Bit	Attribute	Default	Description
15:11	RO	1Fh	**PME# Support** This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. xxxx1: PME# can be asserted from D0 xxx1x: PME# can be asserted from D1 xx1xx: PME# can be asserted from D2 x1xxx: PME# can be asserted from D3 hot 1xxxx: PME# can be asserted from D3 cold
10	RO	1b	**D2 Support** 0: Not supported 1: Supported
9	RO	1b	**D1 Support** 0: Not supported 1: Supported
8:6	RO	111b	**Aux Current (Maximum Current Required)** 111: 375 mA
5	RO	0	**Device Specific Initialization <DSI>** 1 indicates that beyond the standard PCI configuration header , the function requires a device specific initialization sequence following transition to the D0 uninitialized state, which is before the generic class device driver is able to use it. Note that this bit is not used by some operating systems. Microsoft Windows and Windows NT, for instance, do not use this bit to determine whether to use D3. Instead, they use the driver's capabilities to determine this.
4	RO	0	**Reserved**
3	RO	0	**PME# Clock** 0 indicates that no PCI clock is required for the function to generate PME#. 1 indicates that the function relies on the presence of the PCI clock for PME# operation.
2:0	RO	010b	**Version** 010: Complies with Revision 1.1 of the PCI Power Management Interface Specification.

Offset Address: 85-84h (D13F0)

Power Management Capability Control / Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**PME# Status**
14:9	RO	0	**Reserved**
8	RW	0	**PME# Assertion** 0: Disable 1: Enable
7:2	RO	0	**Reserved**
1:0	RW	00b	**Device Status Control** 00: D0 01: D1 10: D2 11: D3 hot

Offset Address: 86-FFh (D13F0) – Reserved

PCI CardReader-Specific MMIO Registers

Offset Range	
200h~~2FFh	SDC
400h~~4FFh	Data DMA
500h~~5FFh	CICH DMA
600h~~6FFh	PCI Control

SDC MMIO Registers (00-FFh)

Offset Address: 00h (SDC-MMIO)

Control Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Command Type** Refer to the Command Type Field Encoding table below for valid encoding and descriptions.
3	RW1C	0	**Response FIFO Reset** Writing 1 to this bit will clear the contents of response register SDC-MMIO Rx10-1Fh. The response will be loaded to the corresponding registers according to response type whether response FIFO is reset or not.
2	RW	0	**Read or Write Operation** 0: Specifies that the data transfer direction of the current command is from card to system memory. 1: Specifies that the data transfer direction of the current command is from system memory to card
1	RO	0	**Reserved**
0	RW1C	0	**Command Start/Busy** This bit is set to initiate a command. The bit is reset once the last bit of the command argument is transmitted. SDC-MMIO Rx00[7:4], Rx00[2], Rx01, Rx02[3:0] and Rx07-04 must be configured before this bit is set.

Table 24. Command Type Field Encodings

Command Type[3:0]	Action applied to SD Memory	Action applied to SDIO
0000b	Non-data-write, non-data-read, non-data-stop, non-io-abort commands.	Non-data-write, non-data-read, non-data-stop, non-io-abort commands.
0001b	Single block write. Use when doing a WRITE_BLOCK (CMD24) command. Block size is defined in CSD or programmed by SET_BLOCKLEN (CMD16) command (see p.41 of SD spec) and is also programmed into **Block Length Register[BS] (offset 08,09)** field. **Block Count Register[BC] (offset 0A,0B)** field is ignored.	Single block IO write. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 1 (direction is write) and Block Mode = 0 (byte mode). The block size is defined in Byte/Block Count. A 0x0 value in Byte/Block Count is considered to be 256 Bytes (see p.18 of SDIO spec). The block size is also programmed into **Block Length Register[BS] (offset 08,09)** field. **Block Count Register[BC] (offset 0A,0B)** field is ignored.
0010b	Single block read. Use when doing a READ_SINGLE_BLOCK (CMD17) command. Block size is defined in CSD or programmed by SET_BLOCKLEN (CMD16) command (see p.41 of SD spec) and is also programmed into **Block Length Register[BS] (offset 08,09)** field. **Block Count Register[BC] (offset 0A,0B)** field is ignored.	Single block IO read. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 0 (direction is read) and Block Mode = 0 (byte mode). The block size is defined in Byte/Block Count. A 0x0 value in Byte/Block Count is considered to be 256 Bytes (see p.18 of SDIO spec). The block size is also programmed into **Block Length Register[BS] (offset 08,09)** field. **Block Count Register[BC] (offset 0A,0B)** field is ignored.
0011b	Multiple block write requires STOP command to end transfer. Use when doing a WRITE_MULTIPLE_BLOCK (CMD25) command. Block size is defined in CSD or programmed by SET_BLOCKLEN (CMD16) command (see p.41 of SD spec) and is also programmed into **Block Length Register[BS] (offset 08,09)** field. Based on the Block Count, the **Block Count Register[BC] (offset 0A,0B)** field is programmed with the correct number of blocks. If BC = ffffh, **Block Count Register[BC] (offset 0A,0B)** field is ignored. The transfer has to be terminated by issuing a STOP_TRANSMISSION (CMD12) command.	Multiple block IO write requires writing to CCCR to end transfer.Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 1 (direction is write) and Block Mode = 1 (block mode) and Byte/Block Count = 0x0 (infinite block count) (see p.18 of SDIO spec). For function 0, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to FN0 Block Size Registers (2 of them) inside CCCR (see p.26 of SDIO spec). For Functions 1 to 7, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to the I/O Block Size registers (2 of them) inside FBR (see p.28 of SDIO spec). The Block size is also programmed into **Block Length Register[BS] (offset 08,09)** field. Based on the Block Count, the **Block Count Register[BC] (offset 0A,0B)** field is programmed with the correct number of blocks. If BC = FFFFh, **Block Count Register[BC] (offset 0A,0B)** field is ignored. The transfer has to be terminated by issuing a IO_RW_DIRECT (CMD52) command to write to the abort register in CCCR (bits [2:0] of register 6) (see p.23 of SDIO spec).

Command Type[3:0]	Action applied to SD Memory	Action applied to SDIO
0100b	Multiple block read requires STOP command to end transfer. Use when doing a READ_MULTIPLE_BLOCK (CMD18) command. Block size is defined in CSD or programmed by SET_BLOCKLEN (CMD16) command (see p.41 of SD spec) and is programmed into **Block Length Register[BS] (offset 08,09)** field. Based on the Block Count, the **Block Count Register[BC] (offset 0A,0B)** field is programmed with the correct number of blocks. If BC = FFFFh, **Block Count Register[BC] (offset 0A,0B)** field is ignored. The transfer has to be terminated by issuing a STOP_TRANSMISSION (CMD12) command.	Multiple block IO read requires writing to CCCR to end transfer. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 0 (direction is read) and Block Mode = 1 (block mode) and Byte/Block Count = 0x0 (infinite block count) (see p.18 of SDIO spec). For function 0, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to FN0 Block Size registers (2 of them) inside CCCR (see p.26 of SDIO spec). For functions 1 to 7, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to the I/O Block Size registers (2 of them) inside FBR (see p.28 of SDIO spec). The block size is also programmed into **Block Length Register[BS] (offset 08,09)** field. Based on the Block Count, the **Block Count Register[BC] (offset 0A,0B)** field is programmed with the correct number of blocks. If BC = FFFFh, **Block Count Register[BC] (offset 0A,0B)** field is ignored. The transfer has to be terminated by issuing a IO_RW_DIRECT (CMD52) command to write to the abort register in CCCR (bits [2:0] of register 6) (see p.23 of SDIO spec).
0101b	Not applicable.	Multiple block IO write with fixed number of blocks. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 1 (direction is write) and Block Mode = 1 (block mode) and Byte/Block Count set to the desired number of blocks to transfer (must Be non-zero) (see p.18 of SDIO spec). For function 0, block size is programmed by using the IO_RW_DIRECT (CMD52) command To write to FN0 Block Size registers (2 of them) inside CCCR (see p.26 of SDIO spec). For functions 1 to 7, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to the I/O Block Size registers (2 of them) inside FBR (see p.28 of SDIO spec). The block size is also programmed into the **Block Length Register[BS] (offset 08,09)** field. Based on the Byte/Block Count, the **Block Count Register[BC] (offset 0A,0B)** field is programmed with the correct number of blocks. Using either 1-bit or 4-bit wire will not affect this number because in the 4-bit wire case, 1 block of data is split into 4 sub-blocks (each 1/4 of the original block size) on each data wire. The start and stop bits still define the boundary of a block. The transfer will be terminated when the correct number of blocks have been transmitted. No abort action is required.
0110b	Not applicable.	Multiple block IO read with fixed number of blocks. Use when doing an IO_RW_EXTENDED (CMD53) with fields R/W Flag = 0 (direction is read) and Block Mode = 1 (block mode) and Byte/Block Count set to the desired number of blocks to transfer (must be non-zero) (see p.18 of SDIO spec). For function 0, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to FN0 Block Size registers (2 of them) inside CCCR (see p.26 of SDIO spec). For functions 1 to 7, block size is programmed by using the IO_RW_DIRECT (CMD52) command to write to the I/O Block Size registers (2 of them) inside FBR (see p.28 of SDIO spec). The block size is also programmed into the **Block Length Register[BS] (offset 08,09)** field. Based on the Byte/Block Count, the **Block Count Register[BC] (offset 0A,0B)** field is programmed with the correct number of blocks. Using either 1-bit or 4-bit wire will not affect this number because in the 4-bit wire case, 1 block of data is split into 4 sub-blocks (each 1/4 of the original block size) on each data wire. The start and stop bits still define the boundary of a block. The transfer will be terminated when the correct number of blocks have been transmitted. No abort action is required.
0111b	Terminate transfer of a multiple block write or read. Use when doing a STOP_TRANSMISSION (CMD12) command (see p.41 of SD spec).	Not applicable.
1000b	Not applicable.	Terminate transfer of a multiple block IO write or read without a fixed desired number of block count. Use when issuing a IO_RW_DIRECT (CMD52) command to write to the abort register In CCCR (bits [2:0] of register 6) to stop the transfer (see p.23 of SDIO spec).
1001b to 1111b	Reserved.	Reserved.

Offset Address: 01h (SDC-MMIO)

Command Index **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Command Index** Bits[13:8] will be the contents of bits[45:40] in SD command token.

Offset Address: 02h (SDC-MMIO)

Response Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Low Voltage (1.8V) Selection** If card supports dual voltage, set this bit to select 1.8V as pad voltage. 0: 3.3V pad voltage 1: 1.8V pad voltage
4	RO	0	**Response Ready.** This bit is set by the SD block once the command-response sequence is finished and reset once response FIFO is read.
3:0	RW	0000b	**Response Type** 0000: No response 0001: R1 response (48 bits) 0010: R2 response (136 bits) 0011: R3 response (48 bits) 0100: R4 response (48 bits) 0101: R5 response (48 bits) 0110: R6 response (48 bits) 1001: R1b response (48 bits) All other values are reserved.

Offset Address: 03h (SDC-MMIO) – Reserved

Offset Address: 07-04h (SDC-MMIO)

Command Argument **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Command Argument**

Offset Address: 08h (SDC-MMIO)

Bus Mode **Default Value: 40h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RO	1b	**Reserved** (Do not program)
5	RO	0	**Reserved**
4	RW	0	**SD Host Power Down Clock Stop** Set this bit in order to save power if there is no cycle. It must be cleared before transferring any data or command. In fact, it is a software programmable clock gating.
3:2	RO	0	**Reserved**
1	RW	0	**Bus Width** 0: 1-bit mode 1: 4-bits mode Before changing the value of this bit, set card bus width with corresponding command first.
0	RO	0	**Reserved**

Offset Address: 09-0Bh (SDC-MMIO) – Reserved

Offset Address: 0D-0Ch (SDC-MMIO)

Block Length **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**Enable SD Host Interrupt** 0: Disable 1: Enable
14:13	RO	0	**Reserved**
12	RW	0	**Active Polarity of Card Detection Pin** 0: Indicates the card insertion is active low. Low means the existence of memory card. 1: Indicates the card insertion is active high
11	RW	0	**Enable Transaction Abort When Multiple Blocks R/W Command CRC Error Occurs** 0: Disable 1: Enable
10:0	RW	0	**Block Length** The block length = Bits[10:0] + 1 For example: Block length = 512B, set bits[10:0] = 511.

Offset Address: 0F-0Eh (SDC-MMIO)

Block Count **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Block Count** Block Count = Bits[15:0] When Rx0F-0Eh is set to FFFFh, this field is ignored in multiple blocks R/W command. Data are transferred infinitely until the controller is programmed to generate CMD12 to terminate data transfer.

Offset Address: 1F-10h (SDC-MMIO)

Response Register **Default Value: 00h**

Bit	Attribute	Default	Description
127:0	RO	0	**Bits [5:0]: Index or reserved bit according to response type.** Bits [15:8], [23:16]…: Response Content (except start bit, transmission bit, index or reserved bits, CRC, end bit). *For response type R1, R1b, R3, R6:* Response data bits [7:1] (CRC or reserved) and bit [0] (end bit) will not be updated into the response register *For response type R2:* Response data bit [135] (start bit), bit [134] (transmission bit), bits [133:128] (reserved bits), bits [127:8] (CID beside internal CRC) will be updated into the response register.

Offset Address: 21-20h (SDC-MMIO)

Current Block Count **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Current Block Count** The number of blocks that has not been transmitted in multiple blocks R/W command. When the command is done, this field value must be 0000h.

Offset Address: 22-23h (SDC-MMIO) – Reserved

Offset Address: 24h (SDC-MMIO)

Interrupt Mask 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Enable Interrupt for Block Data Transfer Done** Generate an interrupt at the completion of each block of data transfer. 0: Disable 1: Enable
4	RW	0	**Enable Interrupt for Multiple Blocks Transfer Done** Generate an interrupt at the completion of all successful data transfer no matter it is single block or multiple blocks data transfer. 0: Disable 1: Enable
3:0	RO	0	**Reserved**

Offset Address: 25h (SDC-MMIO)

Interrupt Mask 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Write Data CRC Error Interrupt Enable** 0: Disable 1: Enable
6	RO	0	**Reserved**
5	RW	0	**Response CRC Error Interrupt Enable** 0: Disable 1: Enable
4	RW	0	**Data Access Timeout Interrupt Enable** 0: Disable 1: Enable
3	RW	0	**Enable Interrupt for Multiple Blocks R/W Auto Stop Command-Response Transfer Done** 0: Disable 1: Enable
2	RW	0	**Enable Interrupt for Command-Response Response Access Timeout** 0: Disable 1: Enable
1	RW	0	**Command-Response Transfer Done Interrupt Enable (or Command Only if the Command Does Not Require A Response)** 0: Disable 1: Enable
0	RO	0	**Reserved**

Offset Address: 26-27h (SDC-MMIO) – Reserved

Offset Address: 28h (SDC-MMIO)

SD Status 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Card Detect Interrupt by GPI Pin** Card insertion or removal interrupt, using CRSD_CD# as card detection pin. 0: No interrupt 1: Card insertion or removal interrupt is detected
6	RO	0	Reserved
5	RW1C	0	**Block Data Transfer Done Interrupt Status** 0: No interrupt 1: Completion of one block data transfer
4	RW1C	0	**Multiple Blocks Transfer Done Interrupt Status** All data are transferred whether it is single block or multiple blocks data. 0: No interrupt 1: Block transfer complete interrupt
3	RO	0	**SD Slot Status (GPI)** Card insertion and removal share the same interrupt, so software use this bit to determine whether it is insertion or removal. The value is valid only if SDC-MMIO Rx0C[13] is set, otherwise it always is 0. 0: No card in the slot 1: SD card in the slot.
2	RO	0	**Reserved**
1	RO	0	**SD Card Write Protect Status** 0: Write protected 1: Write freely
0	RO	0	**Reserved**

Offset Address: 29h (SDC-MMIO)

SD Status 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**Write Data CRC Error Interrupt Status** 0: No error (Normal) 1: Error detected
6	RW1C	0	**Read Data CRC Error Interrupt Status** 0: No error 1: Error detected
5	RW1C	0	**Response CRC Error Interrupt Status** 0: No error 1: Error detected
4	RW1C	0	**Data Access Timeout Interrupt Status (NAC)** 0: Normal 1: Timeout
3	RW1C	0	**Multiple Block R/W Auto Stop Command-Response Transfer Done Interrupt Status** During multiple blocks read and write cycles, when SDC-MMIO Rx21-20 is zero, controller will generate CMD12 automatically. When receiving response of CMD12, this bit is set.
2	RW1C	0	**Command-Response Response Access Timeout Interrupt (NCR) Status** 0: Normal 1: Timeout. There is no response during the given time.
1	RW1C	0	**Command-Response Transfer Done Interrupt Status (or Command Only if the Command Does Not Require A** Response). 0: No interrupt 1: Interrupt occurred
0	RO	0	**Reserved**

Offset Address: 2Ah (SDC-MMIO)

SD Status 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SD Host Automatic Clock Freezing Enable** 0: Disable. Card always transfers data without stopping clock. 1: Enable. When DMA can not transfer data, controller can stop the clock of card in order to block the card data. It is highly recommended to set this bit always.
6	RO	0	**Clock Freezing Status** 0: Normal clocking 1: Clock frozen (potential overrun / underrun)
5	RO	0	**SD Data Response Busy Status** 0: SD card has finished programming and is idle. 1: SD card is busy in programming after write block.
4:3	RO	0	**Reserved**
2:0	RO	0	**SD Mode : Write Data CRC Status** These 3 bits contains the CRC status data of write operation. SPI Mode: Write Data Response

Offset Address: 2Bh (SDC-MMIO) – Reserved

Offset Address: 2Ch (SDC-MMIO)

Response Time Out **Default Value: 40h**

Bit	Attribute	Default	Description
7:0	RW	40h	**Number of Clocks Before A Response Timeout**

Offset Address: 2D-33h (SDC-MMIO) – Reserved

Offset Address: 34h (SDC-MMIO)

Extended Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**High Speed Bus Mode Selection** Set this bit when the controller works under clock frequency 33MHz or 48MHz. 0: Normal speed mode 1: High speed mode
6	RW	0	**Auto Stop Token Generation When Multiple Blocks Write Command Completes** For SPI mode only. 0: No stop token generated after multiple block Write command complete 1: Generate stop token automatically after multiple block Write command complete
5	RW	0	**Issue Bad Data (CRC is 0)** 0: Not issue 1: Issue data with wrong CRC
4	RW	0	**Issue Bad Command (CRC is 0)** 0: Not issue 1: Issue command with wrong CRC
3	RW1C	0	**Reload Block Count** This bit only takes effect during multiple blocks write. If this bit is set, controller will generate the same multiple blocks write transfer directly after finishing current multiple blocks transfer. When the new transfer starts, this bit is cleared.
2	RW	0	**MMC 8-bits Bus Width Selection** 0: Normal mode 1: 8-bits mode. Before set this bit, set SDC-MMIO Rx08[1] =1 first. Otherwise SD bus will meet error. SDC-MMIO Rx08[1] and this bit can not be set at the same time.
1	RW	0	**Command Argument Shift 9-bits During R/W Command**
0	RW	0	**Auto Stop Command Generation When Multiple Blocks R/W Command Completes** For SD mode only. It is highly recommended to set this bit. 0: No CMD12 after multiple blocks data transfer. 1: Generate stop command CMD12 automatically after finishing multiple blocks data transfer.

Offset Address: 35-FFh (SDC-MMIO) – Reserved

Data DMA Control Registers (00-FFh)

Offset Address: 03-00h (Data DMA-MMIO)

Data DMA Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Data DMA Base Address** ***When Write***: Base Address for Data DMA. ***When Read*:** Current memory address will be read or write if DMA is busy or Base Address for Data DMA if DMA is idle. When DMA hang and the transfer direction is from device to memory, read from this register can be refer to judge how many data in bytes are valid in memory. When DMA hang and the transfer direction if from memory to device, read from this register is no meaning for the DMA has a FIFO and shift register.

Offset Address: 07-04h (Data DMA-MMIO)

Data DMA Terminate Count **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Data DMA Terminate Count** ***When Write*:** This register indicates the data length wanted in the next DMA transaction. ***When Read*:** The data count left to transfer if DMA is busy or terminate count if DMA is idle.

Offset Address: 0B-08h (Data DMA-MMIO)

Data DMA Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24	RW	0	**Data DMA Soft Reset** Write 1 to reset data DMA
23:17	RO	0	**Reserved**
16	RW	0	**Enable IRQ after Transfer Finished** 0:Disable 1:Enable
15:11	RO	0	**Reserved**
10	RW	0	**Mode Select for DMA Data Empty / Full** 0:Nature mode. The empty and full from Data DMA will reflect the actual state of internal FIFO; thus, when DMA is idle, full will be 0 and empty will be 1. 1:Hold mode. The empty and full from Data DMA will reflect the actual state of internal FIFO when DMA is busy. But when DMA is idle, full will be 0 and empty will be 1 if bit 8 is 1; full will be 1 and empty will be 0 if bit 8 is 0.
9	RW	0	**Controller Data Bus Width** 0:8 bits 1:16 bits
8	RW	0	**Transaction Direction** 0: From Card to Memory 1: From Memory to Card
7:0	RO	0	**Reserved**

Offset Address: 0F-0Ch (Data DMA-MMIO)

Data DMA Status 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:17	RO	0	**Reserved**
16	RW1C	0	**IRQ Status** IRQ will assert when this bit is set and IRQ is enabled.
15:0	RO	0	**Reserved**

Offset Address: 13-10h (Data DMA-MMIO)

Data DMA Status 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:1	RO	0	**Reserved**
0	RW	0	**DMA Busy Status** 0: DMA is idle. 1: Start DMA Transfer and DMA is busy. Set this bit will trigger data transfer, and it can reset automatically after data transfer.

Offset Address: 14-FFh (Data DMA-MMIO) – Reserved

CICH DMA Control Registers (00-FFh)

Offset Address: 03-00h (CICH DMA-MMIO)

Scatter-Gather Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Scatter-Gather Descriptor Base Address** The starting address of the first descriptor in the Scatter-Gather descriptor list.
1:0	RO	0	**Reserved**

Offset Address: 07-04h (CICH DMA-MMIO)

Control Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RO	0	**Current Descriptor Address** After Rx08[0] is triggered, this register will keep update to reflect descriptor execution process. This register always contains the current descriptor starting address.
1:0	RO	0	**Reserved**

Offset Address: 0B-08h (CICH DMA-MMIO)

Engine Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved**
3	RW	0	**Stop Current Descriptor List Execution** 0: Disable 1: Enable Sometimes the driver wants to cancel current descriptor list execution. When this bit asserts, the descriptor engine will stop after current descriptor execution finishes. This bit will de-assert automatically.
2	RW	0	**Reset Engine** 0: Disable 1: Enable After exception handling, software can set this bit to reset the SG DMA, Descriptor Register File and the Descriptor Interpreter. This will terminate execution of the current descriptor list. This bit will de-assert automatically after several clocks when reset complete.
1	RW	0	**Resume Descriptor Execution** 0: Disable 1: Enable After exception handling, software can set this bit to resume the descriptor execution from the next descriptor in current list. This bit will de-assert automatically after one clock cycle.
0	RW	0	**Start Descriptor Execution** 0: Disable 1: Enable Software can set this bit to start to execute a new descriptor list. The starting address of the list is specified by Rx00[31:2]. This bit will de-assert automatically after one clock cycle.

Offset Address: 0F-0Ch (CICH DMA-MMIO)

Status Register **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:22	RO	0	**Reserved**
21:20	RO	00b	**Descriptor Engine Status** 00: Idle. Engine is not executing any descriptor. 01: Busy. Engine is fetching or executing descriptor. 10: Wait. Engine is waiting for controller interrupt. 11: Stall. Exception happens, engine stalls.
19	RO	0	**Reserved**
18	RO	0	**SDC Interrupt Request** This bit reflects the interrupt request status of SDC. 0: SDC is not requesting to interrupt CPU. 1: SDC is requesting to interrupt CPU.
17	RO	0	**Reserved**
16	RO	0	**DMA Interrupt Request** This bit reflects the interrupt request status of normal DMA engine. 0: Normal DMA engine is not requesting to interrupt CPU. 1: Normal DMA engine is requesting to interrupt CPU.
15:10	RO	0	**Reserved**
9	RW1C	0	**Slot Execution Done**
8	RW1C	0	**Current Descriptor List Execution Stopped** This bit will assert after current descriptor finishes when the software try to stop current descriptor list execution by programming Rx08[3]. 0: Normal execution 1: Execution stopped
7	RW1C	0	**Interrupt Clear Failed** This bit will assert when the descriptor engine try to clear the interrupt status but the interrupt signal keeps asserting. 0: Interrupt cleared successfully. 1: Failed to clear interrupt.
6	RW1C	0	**Interrupt Status Error** This bit will assert when the status register bit hits the exception pattern. 0: No exception detected from card controller 1: Exception detected from card controller
5	RO	0	**Reserved**
4	RW1C	0	**Descriptor List Execution Complete** After the last descriptor in the list execution finishes, this bit will assert and interrupt CPU if interrupt generation is enabled. 0: Descriptor list execution is not complete. 1: Descriptor list execution is complete.
3	RW1C	0	**Descriptor Execution Complete** After current descriptor execution finishes, this bit will assert and interrupt CPU if interrupt generation is enabled. 0: Descriptor execution is not complete. 1: Descriptor execution is complete.
2	RW1C	0	**Descriptor Format Errors Interrupt** When there is any error exists within the descriptor itself, this bit will assert and interrupt CPU if interrupt generation is enabled. For example: Reserved encoding used by the software. 0: No error detected 1: Error detected
1	RW1C	0	**Controller Exceptions Interrupt** When the card host controllers or the normal DMA engine assert interrupt request signal caused by exception conditions, this bit will assert and interrupt CPU if interrupt generation is enabled. 0: No exception condition reported by controller 1: Exception condition reported by controller
0	RW1C	0	**Interrupt of Waiting for Controller Interrupt Time Out** When the CRDE (CardReader Description Engine) is waiting for the controller to issue interrupt request signal, if no interrupt is detected after timer expires, this register bit will assert and interrupt CPU if interrupt generation is enabled. 0: Not time out 1: Time out happens

Offset Address: 13-10h (CICH DMA-MMIO)

Engine Setting **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:18	RO	0	**Reserved**
17:16	RW	00b	**Wait for Controller Interrupt Time Out Counter** 00: Never time out 01: Time out after 1 us 10: Time out after 1 ms 11: Time out after 1024 ms
15:11	RO	0	**Reserved**
10	RW	0	**Enable Interrupt On Complete** 0: Disable 1: Enable
9	RW	0	**Enable Slot Execution Done Interrupt** 0: Disable 1: Enable
8	RW	0	**Enable Current Descriptor List Execution Stopped Interrupt** 0: Disable 1: Enable
7	RW	0	**Enable Interrupt Clear Failed Interrupt** 0: Disable 1: Enable
6	RW	0	**Enable Interrupt Status Error Interrupt** 0: Disable 1: Enable
5	RW	0	**Enable Wrong Interrupt Source Interrupt** 0: Disable 1: Enable
4	RW	0	**Enable Descriptor List Execution Complete Interrupt** 0: Disable 1: Enable
3	RW	0	**Enable Descriptor Execution Complete Interrupt** 0: Disable 1: Enable
2	RW	0	**Enable Descriptor Format Errors Interrupt** 0: Disable 1: Enable
1	RW	0	**Enable Controller Exceptions Interrupt** 0: Disable 1: Enable
0	RW	0	**Enable Interrupt of Waiting for Controller Interrupt Time Out** 0: Disable 1: Enable

Offset Address: 14-FFh (CICH DMA-MMIO) – Reserved

PCI Control Registers (00-FFh)

Offset Address: 00-01h (PCI Control-MMIO) – Reserved

Offset Address: 02h (PCI Control-MMIO)

Clock Gating Control **Default Value: 01h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	0	**SD Output Clock Select Mode** 0x: Use card detection to select 10: Dedicated for SD 11: Reserved
1	RW	0	**Enable Clock Gating** 0: Disable 1: Enable
0	RW	1b	**Soft Reset** 0: Soft reset all the controller and it will be de-asserted automatically 1: Soft reset is de-asserted

Offset Address: 03-04h (PCI Control-MMIO) – Reserved

Offset Address: 05h (PCI Control-MMIO)

SDC Clock Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	011b	**Clock Select** 000: 12M 001: 24M 010: 48M 011: 375K 100: 8M 101: 16M 110:33M 111: Reserved

Offset Address: 06-07h (PCI Control-MMIO) – Reserved

Offset Address: 08h (PCI Control-MMIO)

Interrupt Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Enable CICH Interrupt** 0: Disable 1: Enable
4	RW	0	**Enable DMA Interrupt** 0: Disable 1: Enable
3	RO	0	**Reserved**
2	RW	0	**Enable SDC Interrupt** 0: Disable 1: Enable
1:0	RO	0	**Reserved**

Offset Address: 09h (PCI Control-MMIO)

Interrupt Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RO	0	**CICH Interrupt Status** 0: No interrupt occurred 1: Interrupt occurred
4	RO	0	**DMA Interrupt Status** 0: No interrupt occurred 1: Interrupt occurred
3	RO	0	**Reserved**
2	RO	0	**SDC Interrupt Status** 0: No interrupt occurred 1: Interrupt occurred
1:0	RO	0	**Reserved**

Offset Address: 0Ah (PCI Control-MMIO)

Time Out Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RW	000b	**Time Out Control** 000: No time out 001: 32 us time out 010: 256 us time out 011: 1024 us time out 100: 256 ms time out 101: 512 ms time out 110: 1024 ms time out 111: Reserved

Offset Address: 0B-FFh (PCI Control-MMIO) – Reserved

Device 15 Function 0 (D15F0): Serial ATA & EIDE Controller

** VX820 Series do not support Serial ATA.*

Device 15 Function 0 integrates one EIDE controller and two SATA ports. Please refer to the following table for the IDE/SATA mode configuration.

Table 25. IDE/SATA Support Option

Function	Device Status			D15F0						D17F0
				SATA Register				PATA Register		
	SATA Port0	SATA Port1	IDE	RX40[1]	RXA4[1]	RXA5[1]	RXB9[7]	Rx89[7]	RxC0[0]	Rx50[3]
Off Mode	OFF	OFF	OFF	0	1	1	1	0	0	1
IDE Mode	OFF	OFF	ON	0	1	1	1	1	1	0
IDE + SATA Port 0 Mode	ON	OFF	ON	1	0	1	0	1	1	0
IDE + SATA Port 1 Mode	OFF	ON	ON	1	1	0	0	1	1	0
SATA Port 0 Mode	ON	OFF	OFF	1	0	1	0	0	0	0
SATA Port 1 Mode	OFF	ON	OFF	1	1	0	0	0	0	0
SATA Port 0 + Port 1 Mode	ON	ON	OFF	1	0	0	0	0	0	0
Normal Mode	ON	ON	ON	1	0	0	0	1	1	0

Header Registers (00-3Fh)

Offset Address: 01-00h (D15F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 03-02h (D15F0)

Device ID **Default Value: 5324h**

Bit	Attribute	Default	Description
15:0	RO	5324h	**Device ID** Note: The value of this field will change dependent on Sub Class Code (Rx0Ah). If Rx0A = 04h (RAID), Device ID = 0581h If Rx0A = 01h (IDE), Device ID = 5324h

Offset Address: 05-04h (D15F0)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable**
9:7	RO	0	**Reserved**
6	RO	0	**Parity Error Response**
5	RO	0	**VGA Palette Snooping** Reserved
4	RO	0	**Memory Write and Invalidate**
3	RO	0	**Respond to Special Cycle**
2	RW	0	**Bus Master**
1	RW	0	**Memory Space Access**
0	RW	0	**I/O Space Access** When the "I/O Space" bit is disabled, the device will not respond to I/O addresses. 0: Not respond to I/O address 1: Respond to I/O address

Offset Address: 07-06h (D15F0)

PCI Status **Default Value: 0290h**

Bit	Attribute	Default	Description
15	RO	0	**Detected Parity Error**
14	RO	0	**Signaled System Error** (SERR# asserted)
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort.
10:9	RO	01b	**DEVSEL# Timing** 01: Medium (Default)
8	RO	0	**Master Data Parity Error** This bit is set when bus master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	1b	**Fast Back-to-Back Capability**
6	RO	0	**Reserved**
5	RO	0	**66 MHz Capable**
4	RO	1b	**Power Management Capability List**
3	RO	0	**Interrupt Status**
2:0	RO	0	**Reserved**

Offset Address: 08h (D15F0)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 09h (D15F0)
Programming Interface **Default Value: 8Ah**

If Rx0A = 04h, this register will be read as configuration RAID while if Rx0A = 01h, this register will be read as Configuration IDE.

Bit	Attribute	Default	Description
Configuration RAID: (if Rx0A = 04h) RAID class			
7:0	RO	00h	**Programming Interface** 00: RAID controller
Configuration IDE: (if Rx0A = 01h) IDE class			
7	RO	1b	**Master IDE Device**
6:4	RO	0	**Fixed at 0.**
3	RO	1b	**Programmable Indicator - Secondary**
2	RW	0	**Channel Operating Mode – Secondary** 0: Compatible mode 1: Native mode The configuration of bit[2,0] is listed below: 00b / 01b / 10b: Compatible mode 11b: Native mode
1	RO	1b	**Programmable Indicator – Primary**
0	RW	0	**Channel Operating Mode – Primary** Bit descriptions refer to bit[2].

Offset Address: 0Ah (D15F0)
Sub Class Code **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Sub Class** 01h: IDE Controller 04h: RAID Controller When setting Rx45[7] to 0b, the Sub Class code is allowed to be modified.

Offset Address: 0Bh (D15F0)
Base Class Code **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Base Class** 01h: Mass Storage Controller

Offset Address: 0Ch (D15F0)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Cache Line Size** Fixed at 0.

Offset Address: 0Dh (D15F0)

Latency Timer **Default Value: 20h**

Bit	Attribute	Default	Description
7:4	RW	2h	**Latency Timer**
3:0	RO	0	**Fixed at 0.**

Offset Address: 0Eh (D15F0)

Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Multiple Function Device**
6:0	RO	0	**Fixed at 0.**

Offset Address: 0Fh (D15F0) – Reserved

Offset Address: 13-10h (D15F0)

SATA (Primary Channel) Data / Command Base Address **Default Value: 0000 0000h**

Specifies an 8-bytes I/O address space.

Bit	Attribute	Default	Description
Configuration IDE Class (if Rx0A = 01h) and Compatible Mode (if Rx09[0] = 0)			
31:16	RO	0	**Reserved** (Must set to 0)
15:0	RO	0	**Port Address**
Configuration IDE Class (if Rx0A = 01h) and Native Mode (if Rx09[0] = 1) or Configuration RAID Class (if Rx0A = 04h)			
31:16	RO	0	**Reserved** (Must set to 0)
15:3	RW	3Eh	**Port Address [15:3]**
2:0	RO	001b	**Port Address [2:0]** Fixed at 001b.

Offset Address: 17-14h (D15F0)

SATA (Primary Channel) Control / Status Base Address **Default Value: 0000 0000h**

Specifies a 4-bytes I/O address space of which only the third byte is active.

Bit	Attribute	Default	Description
Configuration IDE Class (if Rx0A = 01h) and Compatible Mode (if Rx09[0] = 0)			
31:16	RO	0	**Reserved** (Must set to 0)
15:0	RO	0	**Port Address**
Configuration IDE Class (if Rx0A = 01h) and Native Mode (if Rx09[0] = 1) or Configuration RAID Class (if Rx0A = 04h)			
31:16	RO	0	**Reserved** (Must set to 0)
15:2	RW	FDh	**Port Address [15:2]**
1:0	RO	01b	**Port Address [1:0]** Fixed at 01b.

Offset Address: 1B-18h (D15F0)

PATA (Secondary Channel) Data / Command Base Address **Default Value: 0000 0000h**

Specifies an 8-bytes I/O address space.

Bit	Attribute	Default	Description
Configuration IDE Class (if Rx0A = 01h) and Compatible Mode (if Rx09[2] = 0)			
31:16	RO	0	**Reserved** (Must set to 0)
15:0	RO	0	**Port Address**
Configuration IDE Class (if Rx0A = 01h) and Native Mode (if Rx09[2] = 1) or Configuration RAID Class (if Rx0A = 04h)			
31:16	RO	0	**Reserved** (Must set to 0)
15:3	RW	2Eh	**Port Address [15:3]**
2:0	RO	001b	**Port Address [2:0]** Fixed at 001b.

Offset Address: 1F-1Ch (D15F0)

PATA (Secondary Channel) Control / Status Base Address **Default Value: 0000 0000h**

Specifies a 4 byte I/O address space of which only the third byte is active.

Bit	Attribute	Default	Description
Configuration 2: if Rx0A = 01 (IDE Class) and Rx09 bit-2 = 1 (Native Mode) or if Rx0A = 04 (RAID Class)			
31:16	RO	0	**Reserved** (Must set to 0)
15:2	RW	DDh	**Port Address [15:2]**
1:0	RO	01b	**Port Address [1:0]** Fixed at 01b.
Configuration 1(Default): if Rx0A = 01 (IDE Class) and Rx09 bit-2 = 0 (Compatible Mode)			
31:16	RO	0	**Reserved** (Must set to 0)
15:0	RO	0	**Port Address**

Offset Address: 23-20h (D15F0)

SATA / PATA Bus Master Mode Base Address **Default Value: 0000 CC01h**

Specifies a 16-bytes I/O address space for SATA and EIDE bus master controllers.

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved** (Must be set to 0)
15:0	RW	CC01h	**Port Address** Bits [3:0] are RO. Fix at 0001b.

Offset Address: 27-24h (D15F0)

SATA Control / Status Base Address **Default Value: 0000 0000h**

A 128-bytes (2 SATA ports) I/O address space

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:0	RO	0	**Fixed at 0000h.**

Offset Address: 28-2Bh (D15F0) - Reserved

Offset Address: 2D-2Ch (D15F0)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID** The read back value can be changed by writing to RxBC-BD.

Offset Address: 2F-2Eh (D15F0)
Subsystem ID **Default Value: 5324h**

Bit	Attribute	Default	Description
15:0	RO	5324h	**Subsystem ID** The read back value can be changed by writing to RxBE-BF.

Offset Address: 30-33h (D15F0) - Reserved

Offset Address: 34h (D15F0)
Power Management Capabilities Pointer **Default Value: B0h**

Bit	Attribute	Default	Description
7:0	RO	B0h	**Power Management Capabilities Pointer**

Offset Address: 35-3Bh (D15F0) - Reserved

Offset Address: 3Ch (D15F0)
Interrupt Line **Default Value: 0Eh**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	Eh	**IDE Interrupt Routing** If bit [7:4] is set to Fh, interrupt is routed to IRQ0. Otherwise, bit [3:0] are decoded to IRQ0~IRQ15.

Offset Address: 3Dh (D15F0)
Interrupt Pin **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Interrupt Routing Mode (use INTA#)** 00: Legacy Mode Interrupt Routing Others: Native Mode Interrupt Routing When in native mode, default is 01h (INTA# used).

Offset Address: 3E-3Fh (D15F0) - Reserved

SATA Registers (40-47h)

Offset Address: 40h (D15F0)
SATA Channel Enable **Default Value: 03h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RO	1b	**SATA Downstream IO and Configuration Cycles Control** 0: SATA downstream IO cycles are blocked, i.e. SATA will not serve ATA commands. SATA downstream configuration cycles work as normal. 1: Enable both SATA downstream IO and configuration cycles. Please refer to the IDE/SATA Support Option table for details.
0	RO	1b	**Reserved** (Do not program)

Offset Address: 41h (D15F0)
SATA Interrupt Gating **Default Value: 03h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**PERR Check** 0: Disable 1: Enable
2	RW	0	**SERR Check** 0: Disable 1: Enable
1	RW	1b	**SATA Primary Channel Interrupt Gating** Interrupt asserted until data are all flushed. 0: Disable 1: Enable
0	RO	1b	**Reserved** (Do not program)

Offset Address: 42h (D15F0)
SATA Native Mode Enable **Default Value: F1h**

Bit	Attribute	Default	Description
7	RW / RO	1b	***IDE Mode:*** The attribute of this bit is RW when the controller is set to IDE mode (Rx0A=01h). And this bit can be further programmed to either compatible mode or native mode. **Primary Channel I/O Native Mode** 0: Disable 1: Enable See the notes below for the details about native mode and compatible mode. ***RAID Mode:*** The attribute of this bit is RO when the controller is set to RAID mode (Rx0A=04h). **Reserved** (Do not program)
6	RO	1b	**Reserved** (Do not program)
5	RW / RO	1b	**Primary Channel Interrupt Native Mode** 0: Disable 1: Enable Do not program. This field is RO when Rx0A is set to 04h.
4:0	RO	10001b	**Reserved** (Do not program)

Note: 1. Compatible mode means the old PC AT IDE mode which uses 1F0-1F7 and 170-17F IO addresses.
2. Native mode means the addresses to be used will be defined in BAR (RX10 – RX27).

Offset Address: 43h (D15F0)
SATA FIFO Threshold Control **Default Value: 44h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	100b	**Primary Channel Threshold Control** (FIFO size: 128 DW) 000: Zero threshold 001: 1/8 FIFO size 010: 1/4 FIFO size 011: 3/8 FIFO size 100: 1/2 FIFO size 101: 5/8 FIFO size 110: 3/4 FIFO size 111: 7/8 FIFO size
3:0	RO	4h	**Reserved** (Do not program)

Offset Address: 44h (D15F0)
Miscellaneous Control 1 **Default Value: 87h**

Bit	Attribute	Default	Description
7	RW	1b	**Disable SATA 66MHz Data Path Dynamic Clock Gating** 0: Enable 1: Disable
6:5	RO	0	**Reserved**
4	RW	0	**Wait Until PHY Ready if Device Has Been Detected When Executing SW Reset** 0: Jump the ports that PHY is not ready 1: Wait until PHY ready
3	RW	0	**Bus Master IDE Status Register Read Retry** 0: Disable 1: Enable
2	RW	1b	**Clear All FIFO Internal States when Accessed Drive is Changed** 0: Disable 1: Enable
1	RW	1b	**Split the Data Access Requests to the Primary and Secondary Channels** 0: Disable 1: Enable
0	RO	1b	**Reserved** (Do not program)

Offset Address: 45h (D15F0)
Miscellaneous Control 2 **Default Value: AFh**

Bit	Attribute	Default	Description
7	RW	1b	**Sub Class (Rx0A) Write Protect** 0: Write enable 1: Write disable
6	RW	0	**Disable PCICLK / Host Clock Gating** a) 33MHz PCICLK which used in clock register configuration. b) 66MHz Host Clock which used to DMAC controller. 0: Enable clock gating 1: Disable clock gating
5	RO	1b	**Reserved** (Do not program)
4	RW	0	**Interrupt Line (Rx3C) Write Protect** 0: Rx3C write enable 1: Rx3C write disable
3:2	RO	11b	**Reserved** (Do not program)
1	RW	1b	**Flush Primary Channel Read DMA Data After Interrupt** 0: Disable 1: Enable
0	RO	1b	**Reserved** (Do not program)

Offset Address: 46h (D15F0)
Miscellaneous Control 3 **Default Value: 08h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Transport Dynamic Clock Gating** 0: Enable clock gating 1: Disable clock gating
5	RW	0	**Assert IRQ When a SATA Device is Hot-Plugged** 0: Disable 1: Enable
4	RO	0	**Reserved**
3	RO	1b	**Reserved** (Do not program)
2	RO	0	**Reserved**
1	RW	0	**Improve SATA PIO Performance** 0: Off 1: On
0	RO	0	**Reserved**

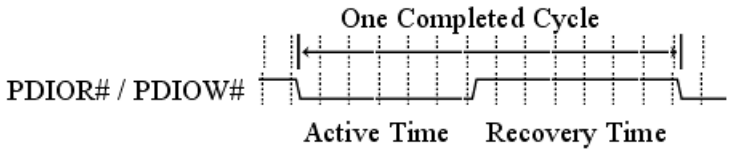
Offset Address: 47h (D15F0) - Reserved

EIDE Registers (48-54h)

Offset Address: 49-48h (D15F0)

EIDE (Secondary Channel) PIO & Multi-Word DMA Timing Control **Default Value: A8A8h**

The following waveform defines the Active Pulse Width and Recovery Time for the EIDE PDIOR# and PDIOW# signals when accessing the data ports (170h):



The actual pulse width is the encoded value in the field plus one in unit of PCI clocks. For example, if the value of the field is 1010b (10 decimal), the active pulse width or recovery time is 11 PCI clocks.

Bit	Attribute	Default	Description
15:12	RW	1010b	**IDE Drive 0 Active Pulse Width (Master)**
11:8	RW	1000b	**IDE Drive 0 Recovery Time (Master)**
7:4	RW	1010b	**IDE Drive 1 Active Pulse Width (Slave)**
3:0	RW	1000b	**IDE Drive 1 Recovery Time (Slave)**

Offset Address: 4A-4Bh (D15F0) - Reserved

Offset Address: 4Ch (D15F0)

Address Setup Time **Default Value: 0Fh**

The following fields define the Address Setup Time. The Address Setup Time is measured from the point when address signals are stable to the point when PDIOR# and PDIOW# are asserted. The IDE specification requires the setup time to not exceed 1T. However, this chip provides flexibility for devices that could not meet the 1T requirement.

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:2	RW	11b	**IDE Drive 0 Address Setup Time (Master)** 00: 1T 01: 2T 10: 3T 11: 4T
1:0	RW	11b	**IDE Drive 1 Address Setup Time (Slave)** 00: 1T 01: 2T 10: 3T 11: 4T

Note: Address Setup Time = (Program Value + 1) * 30 ns, 1T = 30ns.

Offset Address: 4Dh (D15F0) - Reserved

Offset Address: 4Eh (D15F0)

EIDE (Secondary Channel) Non-Data Port Access Timing **Default Value: B6h**

IDE Non-Data Port (171h ~ 177h) access timing control: pulse width = (Program Value + 1) * 30ns.

Bit	Attribute	Default	Description
7:4	RW	Bh	**DIOR# / DIOW# Active Pulse Width**
3:0	RW	6h	**DIOR# / DIOW# Recovery Time**

Offset Address: 4Fh (D15F0) - Reserved

Offset Address: 50h (D15F0)

EIDE (Secondary Channel) Slave Ultra DMA Mode Control **Default Value: 07h**

Bit	Attribute	Default	Description
7	RW	0	**Way to Enable UltraDMA Mode for Slave Device** 0: Enabled by the Set Feature (EFh) command 1: UltraDMA On/Off is decided by the setting of Rx50[6]
6	RW	0	**Ultra DMA Mode Enable** 0: Disable 1: Enable
5	RO	0	**Current Transfer Mode** 0: Multi-words DMA Mode or PIO Mode 1: Ultra DMA Mode
4	RW	0	**Cable Type Reporting** 0: 40-pin cable is used 1: 80-pin cable is used
3:0	RW	7h	**Ultra DMA Write Strobe Timing Control** 0: (Program Value + 2) * 7.5ns 1: (Program Value + 2) * 10ns (for Ultra DMA 100) 2-15: (Program Value + 2) * 7.5ns

Offset Address: 51h (D15F0)

EIDE (Secondary Channel) Master Ultra DMA Mode Control **Default Value: 07h**

Bit	Attribute	Default	Description
7	RW	0	**Way to Enable UltraDMA Mode for Master Device** 0: Enabled by the Set Feature (EFh) command 1: UltraDMA On/Off is decided by the setting of Rx51[6]
6	RW	0	**Ultra DMA Mode Enable** 0: Disable 1: Enable
5	RO	0	**Current Transfer Mode** 0: Multi-words DMA Mode or PIO Mode 1: Ultra DMA Mode
4	RW	0	**Cable Type Reporting** 0: 40-pin cable is used 1: 80-pin cable is used
3:0	RW	7h	**Ultra DMA Write Strobe Timing Control** 0: (Program Value + 2) * 7.5ns 1: (Program Value + 2) * 10ns (for Ultra DMA 100) 2-15: (Program Value + 2) * 7.5ns

Offset Address: 52-54h (D15F0) - Reserved

SATA Link Control Registers (55-56h)

Offset Address: 55h (D15F0)

SATA Control Register 1 **Default Value: 9Ch**

Bit	Attribute	Default	Description
7	RW	1b	**Host Transmit COMRESET and Keep 6 Bursts for Power-on Sequence** 0: Disable 1: Enable
6	RW	0	**Asynchronous Recovery Stop When Asynchronous Recovery Five Times** 0: Disable 1:Enable
5	RW	0	**When SATA Is Out of C4P State for The 1st Time, Whether Allow It to Enter C4P State Again with Different Condition Control** 0: Until host PHYRDY, then allow enter C4P state again. 1: Until host receive XRDY, then allow enter C4P state again.
4	RW	1b	**66MHz GCLK Dynamic Gating which for Latching the Auto-compensation** 0: Disable 1: Enable
3	RW	1b	**SATA 33MHz Dynamic Clock Gating for Power Mode – Port 1** 0: Disable 1: Enable
2	RW	1b	**SATA 33MHz Dynamic Clock Gating for Power Mode – Port 0** 0: Disable 1: Enable
1:0	RO	0	**Reserved**

Offset Address: 56h (D15F0)

SATA Link Control **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**Wait for Device to Synchronize Primitive After Returned from Power Down Mode** 0: Disable 1: Enable
6	RW	1b	**Disable SATA 33MHz Dynamic Clock Gating for Downstream Cycles** 0: Enable 1: Disable
5	RW	0	**Receive Scrambler** 0: Enable 1: Disable
4	RW	0	**Transmit Scrambler** 0: Enable 1: Disable
3	RW	0	**Align Primitive Transmission** 0: Enable 1: Disable
2	RW	0	**Continue Primitive Transmission** 0: Enable 1: Disable
1	RW	0	**Continue Primitive after Alignment** 0: Disable 1: Enable
0	RW	0	**Disable SATA Link Layer Dynamic Clock Gating** 0: Enable 1: Disable

SATA PHY Control Registers (57-5Eh)

Offset Address: 57h (D15F0)

PHY Test Mode Control 1 **Default Value: 30h**

Bit	Attribute	Default	Description
7:6	RO	0b	**Reserved**
5	RW	1b	**Enable SATA AFE Output Signal Gating** 0: Disable 1: Enable
4	RW	1b	**Enable SATA PLL Turn Off When C4P State** 0: Disable 1: Enable Note: C4P state means "special power state for VIA CPU. It is equivalent to ACPI C4 state. SnapShot can be turned on and PLL can be shut-off."
3	RW	0	**When C4P State, SATA Enters** 0: Partial 1: Slumber
2	RW	0	**Enable Host Wakeup when Device in C4P State PWR Mode** 0: Enable 1: Disable
1	RW	0	**Enable Host Resend COMRESET when SATA Device Wakeup from C4P State** 0: Disable 1: Enable
0	RO	0	**Reserved**

Offset Address: 58h (D15F0)

PHY Test Mode Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PHY Operating Mode Select** 0: Gen1 1: Gen2
6	RW	0	**Serial Data Transmit Internal Loop Back** 0: Disable look back 1: Enable look back
5	RW	0	**PHY Test Mode Enable** (Test Only) 0: Disable 1: Enable
4	RW	0	**PHY Test Port Select** (Test Only) 0: Port 0 1: Port 1
3:0	RW	0	**PHY Test Pattern Select** 9h: LTD (Low Transition Density pattern) Ah: HTD (Half-rate/quarter-rate High Transition Density pattern) Bh: LFS (Low Frequency Spectral Content pattern) Ch: SS (Simultaneous Switching Outputs pattern)

Offset Address: 59h (D15F0) – Reserved

Offset Address: 5Ah (D15F0)

PHY Test Mode Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Support Asynchronous Recovery Function** 0: Disable 1: Enable
6:0	RO	0	**Reserved**

Offset Address: 5Bh (D15F0) – Reserved

Offset Address: 5Ch (D15F0)

PHY Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Bypass Oscillator**
6	RW	0	**FTMODE** 0: Normal mode 1: FT mode
5	RW	0	**SATA PHY Dynamic Clock Gating** 0: Enable 1: Disable
4	RW	0	**Double (6 to 12) OOB Burst Number** 0: No (6) 1: Yes (12)
3	RW	0	**SATA PHY 150MHz Dynamic Clock Gating** 0: Enable 1: Disable
2	RO	0	**Reserved**
1	RW	0	**Disable Port 1** 0: Disable 1: Enable
0	RW	0	**Disable Port 0** 0: Disable 1: Enable

Offset Address: 5Dh (D15F0)

PHY Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Port 1 Gen2 Support** 0: Enable 1: Disable
4	RW	0	**Port 0 Gen2 Support** 0: Enable 1: Disable
3	RW	0	**PHY Operating Speed Decision Scheme** 0: Retry Gen2 three times, if fail, force into Gen1 speed 1: Keep on retry at Gen2 speed
2	RO	0	**Reserved**
1	RW	0	**Port 1 TX Pin Swap** 0: Not swap 1: Swap the signal pin STX2+ with STX2-
0	RW	0	**Port 0 TX Pin Swap** 0: Not swap 1: Swap the signal pin STX1+ with STX1-

Offset Address: 5Eh (D15F0) - Reserved

SATA Hot Plug and RAMBIST Status Registers (5F-63h)

Offset Address: 5Fh (D15F0)

SATA Hot Plug Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW1C	0	**Primary Channel (SATA Port 1) Slave Plug Out Status**
2	RW1C	0	**Primary Channel (SATA Port 1) Slave Plug In Status**
1	RW1C	0	**Primary Channel (SATA Port 0) Master Plug Out Status**
0	RW1C	0	**Primary Channel (SATA Port 0) Master Plug In Status**

Offset Address: 60h (D15F0)

SATA RAM BIST **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RO	0	**Primary RAM BIST Error Status**
0	RW	0	**Trigger SATA RAM BIST / Busy Status of RAM BIST** ***When write 1:*** It will trigger SATA RAM BIST function. ***When read:*** It will be SATA RAM BIST Busy status. 0: Idle 1: Busy

Offset Address: 61h (D15F0) – Reserved

Offset Address: 62h (D15F0)

SATA Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Option to Not Assert BSY and Gate Command When PHY is not Ready** 0: Assert BSY and do not gate command even PHY is not ready. 1: Do not assert BSY and gate command when PHY is not ready.
1	RW	0	**Option to Cut the Connection of Rx42 to Control Compatible/Native Mode** 0: Cut the connection of Rx42 to control compatible/native mode. 1: Keep the connection of Rx42 to control compatible/native mode.
0	RO	0	**Reserved**

Offset Address: 63h (D15F0) – Reserved

SATA Analog PHY Control (64-77h)

Offset Address: 64h (D15F0)
Analog PHY Control Register 1 — **Default Value: 35h**

Bit	Attribute	Default	Description
7	RW	0	**When CDR Disperses, Re-assign Phase-mode and CDR Reset Signals** 0: Disable 1: Enable
6:5	RW	01b	**CDR Bandwidth Select Bit [1:0]** 0: Disable 1: Enable
4:3	RW	10b	**Squelch Window Select Bit [1:0]** 0: Disable 1: Enable
2:0	RW	101b	**Options for CDR Charge Pump Bit [2:0]** 0: Disable 1: Enable

Offset Address: 65h (D15F0)
Analog PHY Control Register 2 — **Default Value: AAh**

Bit	Attribute	Default	Description
7:4	RW	Ah	**Port 0 Driver Current Source Bit [3:0]** 0: Disable 1: Enable
3:0	RW	Ah	**Port 1 Driver Current Source Bit [3:0]** 0: Disable 1: Enable

Offset Address: 66h (D15F0)
SATA Control Register 3 — **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Resend COMRESET When Recovering SATA Gen2 Device Error** 0: Disable 1: Enable
6:2	RO	0	**Reserved**
1	RW	0	**Enable Noise Filter on SQEULCH of Port B When SATA Stay in C4P** 0: Disable 1: Enable
0	RW	0	**Enable Noise Filter on SQEULCH of Port A When SATA Stay in C4P** 0: Disable 1: Enable

Offset Address: 67h (D15F0)
Analog PHY Control Register 3 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Port 0 Pre / De-emphasis Level Bit [3:0]** 0: Disable 1: Enable
3:0	RW	0	**Port 1 Pre / De-emphasis Level Bit [3:0]** 0: Disable 1: Enable

Offset Address: 68h (D15F0)
Analog PHY Control Register 4 — **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Port 0 Pre / De-emphasis Level Bit [3:0] for Gen2** 0: Disable 1: Enable
3:0	RW	0	**Port 1 Pre / De-emphasis Level Bit [3:0] for Gen2** 0: Disable 1: Enable

Offset Address: 69h (D15F0)

Analog PHY Control Register 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Port 0 Supports External Interconnect** (For Box-to-Box / Long-Haul - Gen1x or Gen2x Support) 0:Disable 1: Enable
6	RW	0	**Select CDR Regulator Reset Source** 0: PCI Reset 1: Driver Reset
5	RO	0	**Reserved**
4	RO	0	**1.2V Low Voltage Mode** 0: 1.5V 1: 1.2V
3	RW	0	**Gen1 Port 0 Pre / De-emphasis Enable** 0: Disable 1: Enable
2	RW	0	**Gen1 Port 1 Pre / De-emphasis Enable** 0: Disable 1: Enable
1:0	RO	0	**Reserved**

Offset Address: 6Ah (D15F0)

Analog PHY Control Register 6 **Default Value: 03h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Mode Select** 0: Auto Mode 1: Manual Mode
2:0	RW	011b	**50-Ohm Termination Manual Setting Bit [2:0]** 000: Single-end impedance 65.5 ohm 001: Single-end impedance 57.5 ohm 010: Single-end impedance 53.5 ohm 011: Single-end impedance 51 ohm 100: Single-end impedance 49.4 ohm 101: Single-end impedance 48.3 ohm 110: Single-end impedance 47.4 ohm 111: Single-end impedance 46.7 ohm

Offset Address: 6Bh (D15F0)

Analog PHY Control Register 7 **Default Value: 02h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RO	0	**Autocomp Status** 0: Autocomp is disabled 1: Autocomp is enabled
2:0	RO	010b	**Termination Autocomp Values Bit [2:0]**

Offset Address: 6Ch (D15F0)

Analog PHY Control Register 8 **Default Value: 44h**

Bit	Attribute	Default	Description
7:6	RW	01b	**Duty-Balance Control: Rising Time for Serial Data Port 0 Bit [1:0]**
5:4	RW	0	**Duty-Balance Control: Falling Time for Serial Data Port 0 Bit [1:0]**
3:2	RW	01b	**Duty-Balance Control: Rising Time for Serial Data Port 1 Bit [1:0]**
1:0	RW	0	**Duty-Balance Control: Falling Time for Serial Data Port 1 Bit [1:0]**

Note:

		Falling Time FT[1:0]			
	Bit	00	01	10	11
Rising Time RT[1:0]	00		Could increase 5ps for high pulse	Could increase 20ps for high pulse	Could increase 50ps for high pulse
	01	Could increase 5ps for low pulse			
	10	Could increase 20ps for low pulse			
	11	Could increase 50ps for low pulse			

Offset Address: 6D-6Fh (D15F0) - Reserved

Offset Address: 70h (D15F0)

Analog PHY Control Register 9 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Latch Up Test Pins for Port 0 Tx PAD [1:0]** 0: Disable 1: Enable
5:4	RW	0	**Latch Up Test Pins for Port 0 Tx PAD [1:0] - NTREE** 0: Disable 1: Enable
3:2	RW	0	**Latch Up Test Pins for Port 0 Rx PAD [1:0]** 0: Disable 1: Enable
1:0	RW	0	**Latch Up Test Pins for Port 0 Rx PAD [1:0] – NTREE** 0: Disable 1: Enable

Offset Address: 71h (D15F0)

Analog PHY Control Register 10 **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	0	**Latch Up Test Pins for Port 1 Tx PAD [1:0]** 0: Disable 1: Enable
5:4	RW	0	**Latch Up Test Pins for Port 1 Tx PAD [1:0] - NTREE** 0: Disable 1: Enable
3:2	RW	0	**Latch Up Test Pins for Port 1 Rx PAD [1:0]** 0: Disable 1: Enable
1:0	RW	0	**Latch Up Test Pins for Port 1 Rx PAD [1:0] - NTREE** 0: Disable 1: Enable

Offset Address: 72-73h (D15F0) - Reserved

Offset Address: 74h (D15F0)

Analog PHY Control Register 11 **Default Value: FFh**

Bit	Attribute	Default	Description
7:6	RO	11b	**Latch Up Test Pin Status for Port 0 Tx PAD [1:0]** 0: Disable 1: Enable
5:4	RO	11b	**Latch Up Test Pin Status for Port 0 Rx PAD [1:0]** 0: Disable 1: Enable
3:2	RO	11b	**Latch Up Test Pin Status for Port 1 Tx PAD [1:0]** 0: Disable 1: Enable
1:0	RO	11b	**Latch Up Test Pin Status for Port 1 Rx PAD [1:0]** 0: Disable 1: Enable

Offset Address: 75h (D15F0) - Reserved

Offset Address: 76h (D15F0)

Analog PHY Control Register 12 **Default Value: 35h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:5	RW	01b	**CDR Charge Pump Current Select Bit [1:0] – Gen2** 00: Charge pump current 10uA 01: Charge pump current 5uA 10: Charge pump current 20uA 11: Charge pump current 15uA
4:3	RW	10b	**Differential Squelch Window Select Bit [1:0] – Gen2** 00: 92.5mv 01: 109mv 10: 137mv 11: 146mv
2	RW	1b	**Options for CDR Charge Pump Pulse Width Bit 2 – Gen2** 0: Pulse width=2/20T 1: Pulse width=5/20T
1:0	RW	01b	**Options for CDR Divided by N Select Bit [1:0] – Gen2** 00: DIV1 01: DIV2 10: DIV3 11: DIV4

Offset Address: 77h (D15F0)

Analog PHY Control Register 13 **Default Value: 44h**

Bit	Attribute	Default	Description
7:4	RW	4h	**Port 0 Driver Current Source Bit [3:0] – Gen2** 0000: TX output current 10mA 0001: TX output current 10.5mA 0010: TX output current 11.2mA 0011: TX output current 11.8mA 0100: TX output current 12.4mA 0101: TX output current 13mA 0110: TX output current 13.6mA 0111: TX output current 14.3mA 1000: TX output current 14.9mA 1001: TX output current 15.5mA 1010: TX output current 16.1mA 1011: TX output current 16.7mA 1100: TX output current 17.4mA 1101: TX output current 18mA 1110: TX output current 18.6mA 1111: TX output current 19.2mA
3:0	RW	4h	**Port 1 Driver Current Source Bit [3:0] – Gen2** 0000: TX output current 10mA 0001: TX output current 10.5mA 0010: TX output current 11.2mA 0011: TX output current 11.8mA 0100: TX output current 12.4mA 0101: TX output current 13mA 0110: TX output current 13.6mA 0111: TX output current 14.3mA 1000: TX output current 14.9mA 1001: TX output current 15.5mA 1010: TX output current 16.1mA 1011: TX output current 16.7mA 1100: TX output current 17.4mA 1101: TX output current 18mA 1110: TX output current 18.6mA 1111: TX output current 19.2mA

Miscellaneous Registers (78-7Fh)

Offset Address: 78h (D15F0)

SATA (Primary Channel) Transport Status 1 **Default Value: 01h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RO	0	**DMA Read Device Cycle Active** 0: Inactive 1: Active
3	RO	0	**DMA Write Device Cycle Active** 0: Inactive 1: Active
2	RO	0	**SG Operation Active** 0: Inactive 1: Active
1	RO	0	**Interrupt Status** 0: No interrupt 1: Interrupt occurred
0	RO	1b	**FIFO Empty Status** 0: Not empty 1: Empty

Offset Address: 79h (D15F0)

SATA (Primary Channel) Transport Status 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RO	0	**Primary Channel Slave Drive Select** 0: Not selected 1: Selected
3	RO	0	**Transmit PIO Data Cycle Active** 0: Inactive 1: Active
2	RO	0	**Receive PIO Data Cycle Active** 0: Inactive 1: Active
1	RO	0	**Transmit DMA Data Cycle Active** 0: Inactive 1: Active
0	RO	0	**Receive DMA Data Cycle Active** 0: Inactive 1: Active

Offset Address: 7A-7Ch (D15F0) - Reserved

Offset Address: 7Dh (D15F0)

SATA PHY Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RO	0	**Internal PHY Port 1 Receive COMINIT** 0: Not received 1: Received
2	RO	0	**Internal PHY Port 1 Receive COMWAKE** 0: Not received 1: Received
1	RO	0	**Internal PHY Port 0 Receive COMINIT** 0: Not received 1: Received
0	RO	0	**Internal PHY Port 0 Receive COMWAKE** 0: Not received 1: Received

Offset Address: 7E-7Fh (D15F0) - Reserved

SATA Transport Control Registers (80-8Fh)

Offset Address: 80h (D15F0)

SATA PHY Power Management Mode – Software Request **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Request for Slumber Mode on Internal PHY Port 1** 0: Disable 1: Enable
2	RW	0	**Request for Partial Slumber Mode on Internal PHY Port 1** 0: Disable 1: Enable
1	RW	0	**Request for Slumber Mode on Internal PHY Port 0** 0: Disable 1: Enable
0	RW	0	**Request for Partial Slumber Mode on Internal PHY Port 0** 0: Disable 1: Enable

Note: The internal request is triggered when the request bit value is changed from 0 to 1.

Offset Address: 81h (D15F0)

SATA PHY Power Mode – for Hardware Setup **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Let the Idle Device Enter Power Mode when the Active Drive is Switched between Master and Slave Drives** 0: Disable 1: Enable
6	RW	0	**Power Mode Selection for the Idle Device when the Active Drive is Switched between Master and Slave Drives** 0: Partial slumber mode 1: Slumber mode
5	RO	0	**Reserved**
4	RW	0	**Disable Partial Process in Power Mode Control Process** 0: Enable partial slumber process 1: Disable partial slumber process When set to 1, SATA controller will skip the Partial Slumber mode and requests for Slumber mode (if it's enabled in bit-3) when the Power Clock (10T) is expired. When set to 0, SATA controller will request for the Partial Slumber mode when Power Clock (2T) expired.
3	RW	0	**Disable Slumber Process in Power Mode Control Process** 0: Enable slumber process 1: Disable slumber process When set to 1, SATA controller will never request for the Slumber mode. When set to 0, SATA controller will request for Slumber mode when Power Clock (10T) is expired.
2:0	RW	000b	**Power Mode Switch Timer** (in unit of t = 0.425s) 000: T = 1t 001: T = 2t… **Power Mode Control Process:** 1. Partial mode will be requested if transport layer has been idle for 2T. 2. Slumber mode will be requested if transport layer has been idle for 10T.

Offset Address: 82h (D15F0)
Transport Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Transport Issue Early Request to Link** 0: Disable 1: Enable
5	RO	0	**Reserved**
4	RW	0	**Single Data FIS Transmission Size** 0: Maximum size: 8K bytes 1: Allow over 8K bytes.
3	RO	0	**Reserved**
2	RW	0	**SATA Flow Control High Water Mark** 0: 52DW 1: 40DW
1:0	RO	0	**Reserved**

Offset Address: 83-87h (D15F0) - Reserved

Offset Address: 88h (D15F0)
PHY Wakeup Request Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	0	**Assert Wakeup Request to Port 1Internal PHY** 0: Disable 1: Enable
0	RW	0	**Assert Wakeup Request to Port 0 Internal PHY** 0: Disable 1: Enable

Note: The internal request is triggered when the request bit value is changed from 0 to 1.

Offset Address: 89h (D15F0)
PATA Function Control **Default Value: A0h**

Bit	Attribute	Default	Description
7	RW	1b	**Enable IDE Function** 0: Disable (IDE controller won't decode CFG, IDE IO cycle) 1: Enable Please refer to the IDE/SATA Support Option table for details.
6	RO	0	**Reserved**
5	RO	1b	**Reserved** (Do not program)
4:0	RO	0	**Reserved**

Offset Address: 8A-9Fh (D15F0) - Reserved

SATA SCR Registers (A0-AFh)

Offset Address: A0h (D15F0)

Primary Channel Master Device Status (SStatus) **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RO	0	**SATA Gen 2 (3Gb) Status**
3	RO	0	**Slumber Mode Power Management Status** When read 1, it indicates that the device and the controller are currently in Slumber mode. 0: Not in slumber mode 1: Slumber mode
2	RO	0	**Partial Mode Power Management Status** When read 1, it indicates that the device and the controller are currently in Partial mode. 0: Not in partial mode 1: Partial mode
1	RO	0	**PHY Ready Status**
0	RO	0	**Device Detection Status**

Offset Address: A1h (D15F0)

Primary Channel Slave Device Status (SStatus) **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RO	0	**SATA Gen 2 (3Gb) Status**
3	RO	0	**Slumber Mode Power Management Status** When read 1, it indicates that the device and the controller are currently in Slumber mode. 0: Not in slumber mode 1: Slumber mode
2	RO	0	**Partial Mode Power Management Status** When read 1, it indicates that the device and the controller are currently in Partial mode. 0: Not in partial mode 1: Partial mode
1	RO	0	**PHY Ready Status**
0	RO	0	**Device Detection Status**

Offset Address: A2-A3h (D15F0) - Reserved

Offset Address: A4h (D15F0)

SATA (Primary Channel) Master Device Control (SControl) **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	1b	**Transition to Slumber Power State** 0: Enable 1: Disable
2	RW	1b	**Transition to Partial Power State** 0: Enable 1: Disable
1	RW	0	**SATA Interface and Put PHY In Offline Mode** 0: Enable 1: Disable Please refer to the IDE/SATA Support Option table for details.
0	RW	0	**Perform SATA Interface Initialization Sequence to Establish Communication** 0: Disable 1: Enable

Offset Address: A5h (D15F0)

SATA (Primary Channel) Slave Device Control (SControl) **Default Value: 0Ch**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	1b	**Transition to Slumber Power State** 0: Enable 1: Disable
2	RW	1b	**Transition to Partial Power State** 0: Enable 1: Disable
1	RW	0	**SATA Interface and Put PHY In Offline Mode** 0: Enable 1: Disable Please refer to the IDE/SATA Support Option table for details.
0	RW	0	**Perform SATA Interface Initialization Sequence to Establish Communication** 0: Disable 1: Enable

Offset Address: A6-A7h (D15F0) - Reserved

Offset Address: AB-A8h (D15F0)

SATA (Primary Channel) Master SCR Detection Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:28	RO	0	**Reserved**
27	RW1C	0	**Port Selector Presence Detected**
26	RW1C	0	**COMINIT Detected**
25	RW1C	0	**Unrecognized FIS Type**
24	RW1C	0	**Transport State Transition Error** 0: No error 1: Error occurred
23	RW1C	0	**Link Sequence Error** 0: No error 1: Error occurred
22	RW1C	0	**Handshake Error** 0: No error 1: Error occurred
21	RW1C	0	**CRC Error** 0: No error 1: Error occurred
20	RW1C	0	**Disparity Error** 0: No error 1: Error occurred
19	RW1C	0	**10B to 8B Decode Error** 0: No error 1: Error occurred
18	RW1C	0	**COMWAKE Detected** 0: Not detected 1: Detected
17	RW1C / RO	0 / 1b	**PHY Internal Error** 0: No error 1: Error occurred When device exists, the attribute is RW1C and the default value is 0b. When no device exists, the attribute is RO and the default value will be 1b after reset inactive.
16	RW1C	0	**PhyRdy Change** 0: No change 1: Changed
15:12	RO	0	**Reserved**
11	RW1C	0	**Internal Error** 0: No error 1: Error occurred
10	RW1C	0	**Protocol Error** 0: No error 1: Error occurred
9	RW1C	0	**Non-recovered Persistent Communication or Data Integrity Error**
8	RW1C	0	**Non-recovered Transient Data Integrity Error**
7:2	RO	0	**Reserved**
1	RW1C	0	**Recovered Communications Error**
0	RW1C	0	**Recovered Data Integrity Error**

Offset Address: AF-ACh (D15F0)

SATA (Primary Channel) Slave SCR Detection Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW1C	0	**Refers to RxAB-A8 for the register bit definitions for SATA slave device.**

Legacy / Back Door Registers (B0-BFh)

Offset Address: B1-B0h (D15F0)

Power Management Capability ID **Default Value: 0001h**

Bit	Attribute	Default	Description
15:8	RO	0	**Fixed at 0**
7:0	RO	01h	**Capability ID** A PCI power management capability pointer.

Offset Address: B3-B2h (D15F0)

Power Management Interface Revision **Default Value: 0002h**

Bit	Attribute	Default	Description
15:3	RO	0	**Fixed at 0**
2:0	RO	010b	**Power Management Interface Revision** Indicates that this function compiles with Revision 1.1 of PCI Power Management Interface Spec.

Offset Address: B5-B4h (D15F0)

Power Management Capability Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	**Fixed at 0**
1:0	RW	00b	**Power Management Capability Status** 00: D0 11: D3 Hot

Offset Address: B6-B8h (D15F0) - Reserved

Offset Address: B9h (D15F0)

Interrupt Back Door **Default Value: 01h**

Bit	Attribute	Default	Description
7	RW	0	**Option to Reset SATA Function and Gate Off SATAPHY Operation** 0: SATA controller is in normal working mode 1: Reset SATA function and gate off SATAPHY operation. Note: When set to 1, SATA controller's registers and IO ports are still accessible by the CPU if D17F0 Rx50[3] is 0. To completely block downstream cycles to SATA controller, set D17F0 Rx50[3] to 1. Please refer to the IDE/SATA Support Option table for details.
6	RO	0	**Reserved**
5	RW	0	**Staggered Spin-Up Port 1** 0: Wait state 1: Start OOB sequence
4	RW	0	**Staggered Spin-Up Port 0** 0: Wait state 1: Start OOB sequence
3:0	RO	1h	**Reserved**

Offset Address: BB-BAh (D15F0)

Device ID (IDE) Back Door **Default Value: 5324h**

Bit	Attribute	Default	Description
15:0	RW	5324h	**Device ID Back Door** Merge Device ID back door for RAID mode and Device ID back door for IDE mode. These are backdoor registers of Rx03-02, and writing RxBB-BA can change the Device ID value.

Offset Address: BD-BCh (D15F0)

Subsystem Vendor ID Back Door **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW	1106h	**Subsystem Vendor ID (Rx2C-2D) Back Door** Specifies whether Rx2C-2D are RO or RW 0: Read Only 1: Read / Write

Offset Address: BF-BEh (D15F0)

Subsystem ID Back Door **Default Value: 5324h**

Bit	Attribute	Default	Description
15:0	RW	5324h	**Subsystem ID (Rx2E-2F) Back Door** Specifies whether Rx2E-2F are RO or RW 0: Read Only 1: Read / Write

EIDE Registers (C0-FFh)

Offset Address: C0h (D15F0)

EIDE Control **Default Value: 08h**

Bit	Attribute	Default	Description
7:4	RO	0	**Chip ID**
3:1	RO	100b	**Reserved** (Do not program)
0	RW	0	**EIDE (Secondary Channel) Enable** 0: Disable 1: Enable Please refer to the IDE/SATA Support Option table for details.

Offset Address: C1h (D15F0)

EIDE Configuration **Default Value: 02h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**EIDE Secondary PIO Read Prefetch Enable** 0: Disable 1: Enable
4	RW	0	**EIDE Secondary PIO Post Write Enable** 0: Disable 1: Enable
3:0	RO	2h	**Reserved**

Offset Address: C2h (D15F0)

Reserved **Default Value: 09h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	1b	**Reserved** (Do not program)
2:1	RW	0	**Reserved**
0	RW	1b	**Reserved** (Do not program)

Offset Address: C3h (D15F0)

EIDE FIFO Threshold **Default Value: 01h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1:0	RW	01b	**EIDE (Secondary Channel) FIFO** This field determines the FIFO threshold before the secondary channel FIFO is flushed 00: FIFO is flushed when reach 1/4 full 01: FIFO is flushed when reach 1/2 full 10: FIFO is flushed when reach 3/4 full 11: FIFO is flushed when completely filled up (Cannot be used when UDMA is read) Check RxF2 for additional FIFO threshold control.

Notes:
1. If RxF2[4] = 1, bit 1-0 selects the threshold for Device-to-Memory data transfer.
2. If RxF2[4] = 0, bit 1-0 selects the threshold for both Device-to-Memory and Memory-to-Device data transfer.

Offset Address: C4h (D15F0)

EIDE Configuration 1 **Default Value: 08h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**EIDE PIO Read Pre-Fetch Byte Counter** 0: Disable. Pre-fetch will continue when FIFO has vacancy. 1: Enable. The pre-fetch byte count is determined by RxE9-E8[11:0] for EIDE PIO Read.
3	RW	1b	**Bus Master IDE Status Register Read Retry** Determines whether a read to the bus master IDE status register is retried when DMA operation is not complete. 0: Disable. Reads will return status even if DMA operation is not complete 1: Enable. Reads of the status register are automatically retried while DMA operation is not complete.
2	RW	0	**Packet Command Pre-fetch** Determines whether pre-fetching is enabled for packet commands. Packet commands are commands for ATAPI, which is used for devices such as CD-ROM drives. 0: Disable 1: Enable
1	RO	0	**Reserved**
0	RW	0	**Ultra DMA Host Transfer Termination** 0: Enable. The UltraDMA host must wait until at least the first transfer is completed before it can terminate a transaction. 1: Disable

Offset Address: C5h (D15F0) - Reserved

Offset Address: C6h (D15F0)

EIDE Configuration 2 **Default Value: 40h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	1b	**Secondary Channel Read DMA FIFO Flush** 0: Disable 1: Enable. The secondary channel DMA FIFO is flushed when interrupt request is asserted.
5:4	RO	0	**Reserved**
3	RW	0	**This bit should be programmed to 0.**
2	RW	0	**This bit should be programmed to 0.**
1:0	RO	0	**Reserved**

Offset Address: C7-D3h (D15F0) - Reserved

Offset Address: D4h (D15F0)
EIDE Configuration 3 **Default Value: 0Ch**

Bit	Attribute	Default	Description
7	RW	0	**IRQ15 Usage when IDE Channel is Disabled** 0: Release IRQ15 for system usage when IDE Channel is disable (–i.e. RxC0[0] is cleared) 1: IRQ15 is reserved.
6	RO	0	**Reserved**
5	RW	0	**Clear Native Mode Interrupt on Falling Edge of Gated Interrupt** 0: Disable 1: Enable. The interrupt will be automatically cleared on the falling edge of the gated interrupt.
4	RO	0	**Reserved**
3	RW	1b	**Prefetch Line Count** This bit determines how many memory lines are prefetched for IDE transactions. 0: Prefetch 1 line 1: Prefetch 2 lines (16 DoubleWords).
2	RW	1b	**Change Drive Clears All FIFO & Internal States** 0: Disable 1: When command switch from one drive to another drive on the same channel, the controller will terminate the outstanding transactions involving the previous drive.
1:0	RO	0	**Reserved**

Offset Address: D5h (D15F0)
EIDE Clock Gating **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Clock Gating for 33MHz** 0: Enable 1: Disable
3	RW	0	**FIFO 133/100 MHz Dynamic Clock Gating** 0: Enable 1: Disable
2	RW	0	**Reserved**
1	RW	0	**EIDE 133/100 MHz Dynamic Clock Gating** 0: Enable 1: Disable
0	RW	0	**EIDE 66 MHz Dynamic Clock Gating** 0: Enable 1: Disable

Offset Address: D6-E7h (D15F0) - Reserved

Offset Address: E9-E8h (D15F0)
EIDE Sector Size (for Pre-fetch Control) **Default Value: 0200h**

Bit	Attribute	Default	Description
15:12	RO	0	**Reserved**
11:0	RW	200h	**Prefetch Sector Size** (unit: bytes)

Offset Address: EA-F1h (D15F0) - Reserved

Offset Address: F2h (D15F0)
EIDE FIFO Threshold Control **Default Value: 01h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Two FIFO Thresholds** 0: Disable (Use one threshold, defined in RxC3[1:0], for both direction of data transfer between Device and Memory) 1: Enable (Memory-to-Device and Device-to-Memory use RxF2[1:0] and RxC3[1:0] settings, respectively as threshold settings)
3:2	RO	0	**Reserved**
1:0	RW	01b	**Memory-to-Device FIFO Threshold** 00: 1/4 01: 1/2 10: 3/4 11: Full

Offset Address: F3-F7h (D15F0) - Reserved

Offset Address: F8h (D15F0)
EIDE (Secondary Channel) Status **Default Value: 02h**

Bit	Attribute	Default	Description
7	RO	0	**Interrupt Status** 0: No interrupt 1: Interrupted
6	RO	0	**PIO Prefetch Status** 0: No PIO prefetch 1: IDE controller is doing PIO prefetch
5	RO	0	**PIO Post Write Status** 0: No PIO Post write 1: IDE controller is doing PIO Post write
4	RO	0	**DMA Read Operation Status** 0: No DMA read operation 1: IDE controller is doing DMA read operation
3	RO	0	**DMA Write Operation Status** 0: No DMA write operation 1: IDE controller is doing DMA write operation
2	RO	0	**Bus Master Operation Complete** 0: Complete 1: Not complete
1	RO	1b	**FIFO Empty Status** 0: Not empty 1: Empty
0	RO	0	**External DMA Request** 0: No external DMA request 1: There is an external DMA request

Offset Address: F9h (D15F0)
Secondary Channel (IDE) Interrupt Gating **Default Value: 01h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	1b	**Interrupt Gating** 0: Disable 1: Enable (IRQ output gated until FIFO is completed flushed.)

Offset Address: FA-FFh (D15F0) - Reserved

Device 16 Function 0-2 (D16F0-F2) – USB 1.1 UHCI Ports 0-5

This Universal Serial Bus host controller interface is fully compatible with UHCI specification v1.1. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the Device 16 Function 0-2 PCI configuration space of the chip. The USB I/O registers are defined in UHCI specification v1.1. The registers are identical in the Device 16 Functions 0-2 where each function controls different USB ports (function 0 for ports 0-1, function 1 for ports 2-3, and function 2 for ports 4-5).

PCI Configuration Space Header (00-3Fh)

Offset Address: 01-00h (D16F0-F2)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID Code**

Offset Address: 03-02h (D16F0-F2)

Device ID **Default Value: 3038h**

Bit	Attribute	Default	Description
15:0	RO	3038h	**Device ID Code**

Offset Address: 05-04h (D16F0-F2)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable**
9:5	RO	0	**Reserved**
4	RW	0	**Memory Write and Invalidate**
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles).
2	RW	0	**Bus Master**
1	RW	0	**Memory Space**
0	RW	0	**I/O Space**

Offset Address: 07-06h (D16F0-F2)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RW1C	0	**Received Master Abort**
12	RW1C	0	**Received Target Abort**
11	RO	0	**Reserved**
10:9	RO	01b	**DEVSEL# Timing** Fixed at 01. 00: Fast 01: Medium 10: Slow 11: Reserved
8:4	RO	01h	**Fixed at 01h** (for PCI PMI)
3	RW1C	0	**Interrupt Status**
2:0	RO	0	**Fixed at 0** (for PCI PMI)

Offset Address: 08h (D16F0-F2)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D16F0-F2)
Class Code **Default Value: 0C 0300h**

Bit	Attribute	Default	Description
23:0	RO	0C0300h	**Class Code** To indicate the USB1.1 Host Controller.

Offset Address: 0Ch (D16F0-F2)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D16F0-F2)
Latency Timer **Default Value: 16h**

Bit	Attribute	Default	Description
7:0	RW	16h	**Latency Timer**

Offset Address: 0Eh (D16F0-F2)
Header Type Default **Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type**

Offset Address: 0Fh (D16F0-F2)
BIST **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST (Build In Self Test)** Fixed at 0.

Offset Address: 10-1Fh (D16F0-F2) – Reserved

Offset Address: 23-20h (D16F0-F2)
USB I/O Register Base Address **Default Value: 0000 FCE1h**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:5	RW	7E7h	**USB I/O Register Base Address** Port Address for the base of the 32-byte USB I/O Register block, corresponding to AD[15:5].
4:0	RO	01h	**32 Byte Aligned IO Space**

Offset Address: 24-2Bh (D16F0-F2) – Reserved

Offset Address: 2D-2Ch (D16F0-F2)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW1	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D16F0-F2)
Subsystem ID **Default Value: 3038h**

Bit	Attribute	Default	Description
15:0	RW1	3038h	**Subsystem ID**

Offset Address: 30-33h (D16F0-F2) – Reserved

Offset Address: 34h (D16F0-F2)
Power Management Capabilities **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Power Management Capabilities** Fixed at 80h.

Offset Address: 35-3Bh (D16F0-F2) – Reserved

Offset Address: 3Ch (D16F0-F2)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**USB Interrupt Routing** 0000: Disabled 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: Disabled

Offset Address: 3Dh (D16F0)
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin** Fixed at 01h (INTA#).

Offset Address: 3Dh (D16F1)
Interrupt Pin **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RO	02h	**Interrupt Pin** Fixed at 02h (INTB#).

Offset Address: 3Dh (D16F2)
Interrupt Pin **Default Value: 03h**

Bit	Attribute	Default	Description
7:0	RO	03h	**Interrupt Pin** Fixed at 03h (INTC#).

Offset Address: 3E-3Fh (D16F0-F2) – Reserved

USB 1.1-Specific Configuration Registers (40-FFh)

Offset Address: 40h (D16F0-F2)

Control Register 1 **Default Value: 40h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	1b	**Babble Option** This bit controls whether the port is disabled when EOF (End-Of-Frame) babble occurs. Babble is unexpected bus activity that persists into the EOF interval. 0: Automatically disable babbled port when EOF babble occurs. 1: Do not disable babbled port.
5	RW	0	**Reserved**
4	RW	0	**Frame Interval Select** 0: 1ms frame time 1: 0.1ms frame time
3	RW	0	**USB Data Length Option** 0: Supports TD length up to 1280 1: Supports TD length up to 1023
2	RW	0	**Improve FIFO Latency** 0: Improve latency if packet size < 64 bytes. 1: Disable improvement.
1	RW	0	**DMA Option** 0: Enhanced performance (8 DW burst access with better FIFO latency). 1: Normal performance (16 DW burst access with normal FIFO latency).
0	RO	0	**Reserved**

Offset Address: 41h (D16F0-F2)

Control Register 2 **Default Value: 12h**

Bit	Attribute	Default	Description
7	RW	0	**USB 1.1 Improvement for EOP** This bit controls whether USB Specification 1.1 or 1.0 is followed when a stuffing error occurs before an EOP (End-Of-Packet). A stuffing error results when the receiver sees seven consecutive ones in a packet. Under USB specification 1.1, when this occurs in the interval just before an EOP, the receiver will accept the packet. Under USB specification 1.0, the packet is ignored. 0: USB Spec 1.1 Compliant (packet accepted) 1: USB Spec 1.0 Compliant (packet ignored)
6:5	RO	0	**Reserved**
4	RO	1b	**Reserved** (Do not program)
3	RO	0	**Reserved**
2	RW	0	**I/ O Port 60/64 Trap Option** Under the UHCI spec, port 60 / 64 is trapped only when its corresponding enable bits are set. When this bit is set, trap can be set without checking the enable bits. 0: Set trap 60/64 status bits without checking enable bits. 1: Set trap 60/64 status bits only when trap 60/64 enable bits are set.
1	RW	1b	**A20Gate Pass Through Option** This bit controls whether the A20Gate pass-through sequence (as defined in UHCI) is followed. The A20Gate sequence consists of 4 commands. When this bit is 0, the 4-command sequence is followed. When this bit is 1, the last command (write FFh to port 64) is skipped. 0: A20GATE Pass-through command sequence as defined in UHCI. 1: Last command skipped.
0	RO	0	**Reserved**

Offset Address: 42h (D16F0-F2)
Control Register 3 **Default Value: 03h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Hold Data Transmission till FIFO Reaches Transmission Threshold** 0: Enable 1: Disable
1:0	RO	11b	**Reserved** (Do not program)

Offset Address: 43h (D16F0-F2)
Control Register 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Continue Transmitting Erroneous Data When FIFO Underrun** 0: Enable 1: Disable
2	RW	0	**Issue CRC Error Instead of Stuffing Error on FIFO Underrun** 0: Enable 1: Disable
1:0	RO	0	**Reserved**

Offset Address: 44-47h (D16F0-F2) – Reserved

Offset Address: 48h (D16F0-F2)
Control Register 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	0	**Issue Bad CRC5 in SOF After FIFO Underrun** 0: Enable 1: Disable
1	RW	0	**Lengthen PreSOF Time** The preSOF time point determines whether there is enough time in the remaining frame period to perform a 64-byte transaction. It prevents a packet that may not fit in the remaining frame period from being initiated. This bit controls whether the preSOF time point is moved back so that the preSOF time is lengthened. 0: Disable 1: Enable (PreSOF time lengthened)
0	RW	0	**Issue Non-Zero Bad CRC Code on FIFO Underrun** A FIFO underrun occurs when there is no data in the FIFO to supply data transmission. When this occurs, the controller invalidates the data by sending an incorrect CRC code to the device. This bit controls the type of incorrect CRC sent. 0: Non zero CRC (recommended) 1: All zero CRC This option isn't really needed now as non-zero CRC always works.

Offset Address: 49h (D16F0-F2)
Control Register 6 **Default Value: 0Bh**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Bypass 1M Oscillator, Uses CLK_LS Instead** 0: Disable 1: Enable
4	RW	0	**Test Mode for Vector Generation** When enabled, CLK48M also comes from external test pins. 0: Disable 1: Enable
3:2	RO	10b	**Reserved** (Do not program)
1	RW	1b	**EHCI Supports PME Assertion in D3 Cold State** 0: Not Supported 1: Supported
0	RW	1b	**UHCI Supports PME Assertion in D3 Cold State** 0: Not Supported 1: Supported

Offset Address: 4Ah (D16F0-F2)
Control Register 7 **Default Value: A0h**

Bit	Attribute	Default	Description
7:3	RW	14h	**USB 1.1 Bus Timeout Parameter**
2:1	RO	0	**Reserved**
0	RW	0	**Use External 60 MHz Clock** Set this bit to use external 60 MHz input clock. 0: Disable 1: Enable

Offset Address: 4Bh (D16F0-F2)
Control Register 8 **Default Value: 8Bh**

Bit	Attribute	Default	Description
7	RO	1b	**Reserved** (Do nor program)
6:4	RO	0	**Reserved**
3	RO	1b	**Reserved** (Do not program)
2	RO	0	**Reserved**
1	RO	1b	**Reserved** (Do not program)
0	RW	1b	**Enable Clock Auto Stop** 0: Disable (No Stop) 1: Enable (Auto Stop)

Offset Address: 4C-5Fh (D16F0-F2) – Reserved

Offset Address: 60h (D16F0-F2)
Serial Bus Release Number **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	**Serial Bus Release Number** Fixed at 10h.

Offset Address: 61-7Fh (D16F0-F2) – Reserved

Offset Address: 83-80h (D16F0-F2)
Power Management Capability **Default Value: FFC2 0001h**

Bit	Attribute	Default	Description
31:0	RO	FFC2 0001h	**Power Management Capability** If 49[0] = 1, this register is fixed at FFC20001h. If 49[0] = 0, this register is fixed at 7E0A0001h.

Offset Address: 84h (D16F0-F2)
Power Management Capability Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power Management Capability Status** 00b: D0 01b: Reserved 10b: Reserved 11b: D3 Hot

Offset Address: 85-BFh (D16F0-F2) – Reserved

Offset Address: C1-C0h (D16F0-F2)

Legacy Support (for UHCI v1.1 Compliant) **Default Value: 2000h**

Bit	Attribute	Default	Description
15	RW1C	0	**End of A20Gate Pass Through Status (A20PTS)** 1 to indicate A20Gate pass through sequence has ended.
14	RO	0	**Reserved** Fixed to 0.
13	RW	1b	**USB PIRQ Enable (USBPIRQDEN)** 0: Disable 1: Enable
12	RO	0	**USB IRQ Status (USBIRQS)** 1 to indicate USB IRQ is active.
11	RW1C	0	**Trap By 64h Write Status (TBY64W)** 1 to indicate a write to port 64h occurred.
10	RW1C	0	**Trap By 64h Read Status (TBY64R)** 1 to indicate a read to port 64h occurred.
9	RW1C	0	**Trap By 60h Write Status (TBY60W)** 1 to indicate a write to port 60h occurred.
8	RW1C	0	**Trap By 60h Read Status (TBY60R)** 1 to indicate a read to port 60h occurred.
7	RW	0	**SMI At End Of Pass Through Enable (SMIEPTE)** 0: Disable 1: Enable
6	RO	0	**Pass Through Status (PSS)** 1 to indicate A20Gate pass through sequence is currently in progress.
5	RW	0	**A20Gate Pass Through Enable (A20PTEN)** 0: Disable 1: Enable
4	RW	0	**Trap/SMI ON IRQ Enable (USBSMIEN)** 0: Disable 1: Enable
3	RW	0	**Trap/SMI On 64h Write Enable (64WEN)** 0: Disable 1: Enable
2	RW	0	**Trap/SMI On 64h Read Enable (64REN)** 0: Disable 1: Enable
1	RW	0	**Trap/SMI On 60h Write Enable (60WEN)** 0: Disable 1: Enable
0	RW	0	**Trap/SMI On 60h Read Enable (60REN)** 0: Disable 1: Enable

Note: This register provides control and status capability for the legacy keyboard and mouse functions. Please refer to UHCI Spec. for further details.

Offset Address: C2-FFh (D16F0-F2) – Reserved

USB 1.1 I/O Registers (00-13h)

These registers are compliant with the UHCI v1.1 standard. Refer to the UHCI v1.1 specification for further details.

I/O Offset Address: 01-00h (USB 1.1-IO)

USB Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0000h	USB Command

I/O Offset Address: 03-02h (USB 1.1-IO)

USB Status **Default Value: 0020h**

Bit	Attribute	Default	Description
15:0	RW1C	0020h	USB Status

I/O Offset Address: 05-04h (USB 1.1-IO)

USB Interrupt Enable **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0000h	USB Interrupt Enable

I/O Offset Address: 07-06h (USB 1.1-IO)

Frame Number **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0000h	Frame Number

I/O Offset Address: 0B-08h (USB 1.1-IO)

Frame List Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	Frame List Base Address

I/O Offset Address: 0Ch (USB 1.1-IO)

Start of Frame Modify **Default Value: 40h**

Bit	Attribute	Default	Description
7:0	RW	40h	Start of Frame Modify

I/O Offset Address: 0D-0Fh (USB 1.1-IO) – Reserved

I/O Offset Address: 11-10h (USB 1.1-IO)

Port 0 Status / Control **Default Value: 0080h**

Bit	Attribute	Default	Description
15:0	RW1C	0080h	Port 0 Status / Control

I/O Offset Address: 13-12h (USB 1.1-IO)

Port 1 Status / Control **Default Value: 0080h**

Bit	Attribute	Default	Description
15:0	RW1C	0080h	Port 1 Status / Control

Device 16 Function 4 Registers - USB 2.0 EHCI

This Enhanced Serial Bus host controller interface is fully compatible with EHCI specification v1.0. There are two sets of software accessible registers: PCI configuration registers and USB I/O registers. The PCI configuration registers are located in the Bus 0 Device 16 Function 4 PCI configuration space of the chip. The USB I/O registers are defined in EHCI specification v1.0.

PCI Configuration Space Header (00-3Fh)

Offset Address: 01-00h (D16F4)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID Code**

Offset Address: 03-02h (D16F4)

Device ID **Default Value: 3104h**

Bit	Attribute	Default	Description
15:0	RO	3104h	**Device ID Code**

Offset Address: 05-04h (D16F4)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable** Fixed at 0b (Not supported).
9:5	RO	0	**Reserved**
4	RW	0	**Memory Write and Invalidate**
3	RO	0	**Reserved** Special cycle monitoring. Fixed at 0b.
2	RW	0	**Bus Master**
1	RW	0	**Memory Space**
0	RW	0	**I/O Space**

Offset Address: 07-06h (D16F4)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15:14	RO	0	**Reserved**
13	RW1C	0	**Received Master Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Reserved**
10:9	RO	01b	**DEVSEL# Timing** Fixed at 01b. 00: Fast 01: Medium 10: Slow 11: Reserved
8:4	RO	01h	**Fixed at 01h** (for PCI PMI)
3	RW1C	0	**Interrupt Status**
2:0	RO	0	**Reserved**

Offset Address: 08h (D16F4)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D16F4)
Class Code **Default Value: 0C 0320h**

Bit	Attribute	Default	Description
23:0	RO	0C0320h	**Class Code for USB2.0 EHCI Host Controller**

Offset Address: 0Ch (D16F4)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D16F4)
Latency Timer **Default Value: 16h**

Bit	Attribute	Default	Description
7:0	RW	16h	**Latency Timer**

Offset Address: 0Eh (D16F4)
Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type**

Offset Address: 0Fh (D16F4)
BIST **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**BIST (Built In Self Test)** Fixed at 00h.

Offset Address: 13-10h (D16F4)
EHCI Memory Mapped I/O Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**EHCI Memory Mapped I/O Registers Base Address** Memory Address for the base of the USB 2.0 EHCI I/O Register block, corresponding to AD[31:8].
7:3	RO	0	**Reserved**
2:1	RO	00b	**Memory Mapping** Reads 00b for 32-bit addressing. Fixed at 00b.
0	RO	0	**Reserved**

Offset Address: 14-2Bh (D16F4) – Reserved

Offset Address: 2D-2Ch (D16F4)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RW1	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D16F4)
Subsystem ID **Default Value: 3104h**

Bit	Attribute	Default	Description
15:0	RW1	3104h	**Subsystem ID**

Offset Address: 30-33h (D16F4) – Reserved

Offset Address: 34h (D16F4)
Power Management Capabilities **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Power Management Capabilities** Fixed at 80h.

Offset Address: 35-3Bh (D16F4) – Reserved

Offset Address: 3Ch (D16F4)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0000b	**USB Interrupt Routing** 0000: Disable 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: Disable

Offset Address: 3Dh (D16F4)
Interrupt Pin **Default Value: 04h**

Bit	Attribute	Default	Description
7:0	RO	04h	**Interrupt Pin** Fixed at 04h (INTD#).

Offset Address: 3E-3Fh (D16F4) – Reserved

USB 2.0-Specific Configuration Registers (40-FCh)

Offset Address: 40h (D16F4)

Control Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Babble Option** This bit controls whether the port is disabled when EOF (End-Of-Frame) babble occurs. Babble is unexpected bus activity that persists into the EOF interval. When this bit is 0, the port with the EOF babble is disabled. When it is 1, it is not disabled. 0: Automatically disable babbled port when EOF babble occurs 1: Do not disable babbled port
5	RO	0	**Reserved**
4	RW	0	**Micro-Frame Interval Select** 0: 125 us micro-frame time 1: 62.5 us micro-frame time
3	RW	0	**Select Signal to Detect Idle microFrame for C4P** 0: Use internal SOF counter overflow signal to detect idle microframes. 1: Detect idle microframes after sending SOF to USB bus.
2	RO	0	**Reserved**
1	RW	0	**DMA Options** Also used to control FIFO over/under run criteria. 0: 16 DW burst access 1: 8 DW burst access
0	RO	0	**Reserved**

Offset Address: 41h (D16F4)

Test Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable USB 2.0-MMIO Rx17-14[12] (HCHALT Bit) in USB Status Register (USBSTS) Software Transparent in C4P State** 0: Disable 1: Enable
6	RW	0	**Select Which RUN Bit is Used to Check Idle microFrame for C4P** 0: Use C2P CFG RUN Bit to check Idle microFrame detection, which is not changed with the C4P function. 1: Use internal RUN Bit to check Idle microFrame detection, which is changed with the C4P function.
5:0	RO	0	**Reserved**

Offset Address: 42h (D16F4) – Reserved

Offset Address: 43h (D16F4)

Control Register 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable 66MHz New Dynamic Scheme** 0: Disable 1: Enable
6	RW	0	**Enable 33MHz New Dynamic Scheme** 0: Disable 1: Enable
5:0	RO	0	**Reserved**

Offset Address: 44-47h (D16F4) – Reserved

Offset Address: 48h (D16F4)
Control Register 3 **Default Value: BEh**

Bit	Attribute	Default	Description
7	RW	1b	**USB 2.0 EOP Pattern (FEh) Error Check** 0: Disable 1: Enable
6	RW	0	**Extra-Handshake Error Checking in Isochronous Transaction** 0: Disable 1: Enable
5	RW	1b	**CCA Burst Access** 0: Burst Enable 1: Burst Disable
4	RW	1b	**USB 2.0 Reference Bus Idle Status** When set this bit to 1, the hardware refers to the bus idle status from PHY to check the start and the end of an incoming packet. 0: Disable 1: Enable
3:2	RO	11b	**Reserved** (Do not program)
1	RW	1b	**USB 2.0 CRC16 Check Enable for Toggle Mismatch** 0: Disable 1: Enable
0	RW	0	**Disable HS (High Speed) Port Align Most to Micro-Frame Boundary** 0: Align 1: Not Align

Offset Address: 49h (D16F4)
Control Register 4 **Default Value: 68h**

Bit	Attribute	Default	Description
7	RW	0	**MAC Allows More Delay between Transactions** The delay parameter could be specified in Rx4A. 0: Disable 1: Enable
6	RW	1b	**MAC Provides Timeout to Device When Receiver Detects Error** The delay parameter could be specified in Rx51. 0: Disable 1: Enable
5	RW	1b	**EHCI Clock Auto Stop** 0: Disable (No stop) 1: Enable (Auto stop)
4	RW	0	**Auto Power Down Receiver Squelch Detector** 0: Auto power down 1: Always power up
3	RW	1b	**New USB C4P State Support** 0: Disable 1: Enable
2	RO	0	**USB Analog PLL Control When Entering C4P State** 0: Not turn off 48MHz PLL 1: PMU will control to turn off PHY PLL in USBC
1:0	RW	00b	**NULL-SOF (Null Start Of Frame) Valid Time Selection** (for C4P state support) 00: 8 (micro) frames 01: 16 (micro) frames 10: 24 (micro) frames 11: 32 (micro) frames

Offset Address: 4Ah (D16F4)
MAC Inter-Transaction Delay Parameter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**MAC Inter-Transaction Delay Parameter**

Offset Address: 4Bh (D16F4)
MAC Turn Around Time Parameter **Default Value: 09h**

Bit	Attribute	Default	Description
7	RW	0	**SOF (Start of Frame) Disconnect Detection Period** 0: Narrow 1: Not narrow
6:5	RW	00b	**EHCI Sleep Time Select** 00: 1 us 01: 10 us 10: 10 us 11: 80 us
4	RW	0	**Issue UTM_SOF When Run Bit Clears** 0: Issue 1: Not issue
3:0	RW	9h	**USB 2.0 MAC Transmit Turn Around Time Parameter**

Offset Address: 4Ch (D16F4)

PHY Control 1 **Default Value: 12h**

Bit	Attribute	Default	Description
7	RW	0	**Resume ACK Control** 0: 20ms resume, then send ACK to C4P state resume request 1: Quickly send ACK to C4P state resume request
6	RO	0	**Reserved**
5	RW	0	**USB1.0 UTM Tx Speed Up** 0: Disable 1: Enable
4	RW	1b	**USB2.0 EHCI Debug Port Support Enable** 0: Disable 1: Enable
3	RW	0	**Sync-Fast Enable** 0: Disable 1: Enable
2	RW	0	**Sync-J_End Enable** 0: Disable 1: Enable
1:0	RW	10b	**Squelch Detector Fine Tune**

Offset Address: 4Dh (D16F4) – Reserved

Offset Address: 4F-4Eh (D16F4)

PHY Control 2 **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**Clear Idle microFrame Counter When Hardware is Doing Port Reset** 0: Disable 1: Enable
14	RW	0	**Wait over 1 MicroFrame after C4P 20ms Resume Time and Before Sending 1st SOF** 0: Disable 1: Enable
13	RW	0	**RUN Bit Recovery Control** 0: Recover RUN bit just at the end of resumeK signal, after exiting C4P state. 1: Recover RUN bit at 1st SOF sending to USB bus, after exiting C4P state.
12	RW	0	**Clear RUN Bit When EHCI_IDLE (if Software Clears RUN Bit)** 0: Clear RUN bit only when EHCI is idle. 1: Clear RUN bit at any time.
11	RW	0	**Enable UHCI Detect Connect Status and Device Speed if POwner (Port Owner) Bit is Cleared** 0:Disable 1: Enable
10:8	RO	0	**Reserved**
7:6	RW	00b	**Idle microFrame Selection for UHCI1** If reach indicated idle frame number, it is allowed to enter C4P state. 00: No ISO (Isochronous endpoint) or valid Interrupt IN transaction for 8 frames 01: No ISO or valid Interrupt IN transaction for 16 frames 10: No ISO or valid Interrupt IN transaction for 32 frames 11: No ISO or valid Interrupt IN transaction for 40 frames
5:4	RW	00b	**Idle microFrame Selection for UHCI2** If reach indicated idle frame number, it is allowed to enter C4P state. 00: No ISO or valid Interrupt IN transaction for 8 frames 01: No ISO or valid Interrupt IN transaction for 16 frames 10: No ISO or valid Interrupt IN transaction for 32 frames 11: No ISO or valid Interrupt IN transaction for 40 frames
3:2	RW	00b	**Idle microFrame Selection for UHCI3** If reach indicated idle frame number, it is allowed to enter C4P state. 00: No ISO or valid Interrupt IN transaction for 8 frames 01: No ISO or valid Interrupt IN transaction for 16 frames 10: No ISO or valid Interrupt IN transaction for 32 frames 11: No ISO or valid Interrupt IN transaction for 40 frames
1	RW	0	**Enable Using New Reset Mechanism to Idle microFrame Detection Function for UHCI** 0: Disable idle microFrame detection reset new mechanism. Reset UHCI idle microFrame detection and idle microFrame counter when there is transaction of any type 1: Enable reset UHCI idle microFrame detection and idle microFrame counter when ISO transaction, Interrupt OUT transaction and Interrupt IN transaction with Data packet back
0	RW	0	**Enable Patch Golden Tree** 0: Disable reset internal EHCI FSM when RUN bit is cleared. 1: Enable reset internal EHCI FSM when RUN bit is cleared.

Offset Address: 50h (D16F4)
USB 2.0 Doorbell Bit Function **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Fetch One More QH Before De-asserting Doorbell Bit** 0: Disable 1: Enable
6:0	RO	0	**Reserved**

Offset Address: 51h (D16F4)
USB 2.0 MAC Timeout Parameter **Default Value: 60h**

Bit	Attribute	Default	Description
7:0	RW	60h	**USB 2.0 Receive Timeout Parameter** The unit is byte time. According to the core spec, the host controller or a device expecting a response to a transmission must not timeout the transaction if the inter-packet delays in 736 and 816 bit times. The worst round trip delay is 721 bit times.

Offset Address: 52h (D16F4)
Control Register 5 **Default Value: 18h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	1b	**Reset NULLSOF and NULLSOF Counter When Exiting C4P State** 0: Disable 1: Enable
3	RW	1b	**Send Out Interrupt of IOC and RollOver When USB is in C4P State** 0: Disable 1: Enable
2	RW	0	**Enable USB Responding to PMU C4P State Request by Entering / Exiting D3 State** 0: Enable 1: Disable (without entering / exiting D3 state)
1	RW	0	**Enable New PLL Power Down Scheme** When there is no high-speed device connection, power down PLL 0: Disable 1: Enable
0	RW	0	**USB Physical Circuitry Power Down Condition** 0: When the port is disabled or suspended. 1: When the port is disabled or suspended, or when there is no TX (transmit) activity.

Offset Address: 53h (D16F4)
C4P State Control **Default Value: F0h**

Bit	Attribute	Default	Description
7	RO	1b	**Reserved** (Do not program)
6	RW	1b	**PLLOK Selection Control** 0: Use logic control PLLOK 1: Use circuit control PLLOK
5:0	RO	110000b	**Reserved** (Do not program)

Offset Address: 54-57h (D16F4) – Reserved

Offset Address: 58h (D16F4)
PHY Control 2 **Default Value: 04h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RW	1b	**Detect High-Speed Disconnect During SOF Period** 0: Disable 1: Enable
1:0	RW	0	**XCVR1.1 Slew Rate Control**

Offset Address: 59h (D16F4)
PHY Control 3 **Default Value: 0Bh**

Bit	Attribute	Default	Description
7	RW	0	**Disable PHY Auto Power-Down Feature** When set this bit, if port is suspended or is not EHCI owned, the port will auto power-down. 0: Auto power-down 1: Disable Auto power-down
6	RW	0	**Transit POwner Control** This bit controls port route logic to be programmable if port connection is not present, default is to transit POwner only at falling edge of connect status. 0: Falling edge 1: Level
5:4	RO	0	**Reserved**
3	RW	1b	**DPLL Fast Lock Enable** 0: Disable 1: Enable
2	RO	0	**Reserved**
1	RW	1b	**Disable PHY Receiver Including Squelch Detector Power up Time Improvement** 0: Enable improvement 1: Disable improvement
0	RO	1b	**Reserved** (Do not program)

Offset Address: 5B-5Ah (D16F4)
High-Speed Port Pad Termination Resistor Fine Tune 1 **Default Value: 8888h**

Bit	Attribute	Default	Description
15:8	RW	88h	**Bit 15-12: USB Port 0** **Bit 11-8: USB Port 1**
7:0	RW	88h	**Bit 7-4: USB Port 2** **Bit 3-0: USB Port 3**

Offset Address: 5Ch (D16F4)
PHY Control 4 **Default Value: 53h**

Bit	Attribute	Default	Description
7	RW	0	**DPLL Zero Phase Start Select** 0: ZPS takes 8-bit times to start 1: ZPS takes 4-bit times to start
6:4	RW	101b	**Delay DPLL Input Data Control**
3:2	RW	0	**DPLL Track Speed Select**
1:0	RW	11b	**DPLL Lock Speed Select**

Offset Address: 5E-5Dh (D16F4)
High-Speed Port Pad Termination Resistor Fine Tune 2 **Default Value: 0088h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7:0	RW	88h	**Bit 7-4: USB Port 4** **Bit 3-0: USB Port 5**

Offset Address: 5Fh (D16F4) – Reserved

Offset Address: 60h (D16F4)
Serial Bus Release Number **Default Value: 20h**

Bit	Attribute	Default	Description
7:0	RO	20h	**Serial Bus Release Number** Fixed at 20h for USB2.0.

Offset Address: 61h (D16F4)
Frame Length Adjustment **Default Value: 20h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5:0	RW	20h	**Frame Length Adjustment**

Offset Address: 63-62h (D16F4)
Port Wake Capability **Default Value: 0001h**

Bit	Attribute	Default	Description
15:7	RO	0	**Reserved**
6:1	RW	0	**Port Wake Capability**
0	RO	1b	**Port Wake Capability**

Offset Address: 64-67h (D16F4) – Reserved

Offset Address: 6B-68h (D16F4)
USB Legacy Support Extended Capability **Default Value: 0000 0001h**

Bit	Attribute	Default	Description
31:25	RO	0	**Reserved**
24	RW	0	**USB Host Controller OS Owned Semaphore**
23:17	RO	0	**Reserved**
16	RW	0	**USB Host Controller BIOS Owned Semaphore**
15:8	RO	0	**Next EHCI Extended Capability Pointer**
7:0	RO	01h	**Capability ID**

Offset Address: 6F-6Ch (D16F4)
USB Legacy Support Control / Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:29	RW1C	0	**USB Legacy Support Control / Status** Reference EHCI Spec. for details.
28:22	RO		
21:16	RO		
15:13	RW		
12:6	RO		
5:0	RW		

Offset Address: 70-7Fh (D16F4) – Reserved

Offset Address: 80h (D16F4)
Power Management Capability ID **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Power Management Capability ID**

Offset Address: 81h (D16F4)
Next Item Pointer **Default Value: 88h**

Bit	Attribute	Default	Description
7:0	RO	88h	**Next Item Pointer** If Rx4C[4] = 1, this register is fixed at 88h. If Rx4C[4] = 0, this register is fixed at 00h.

Offset Address: 83-82h (D16F4)
Power Management Capability **Default Value: FFC2h**

Bit	Attribute	Default	Description
31:0	RO	FFC2h	**Power Management Capability** If D16F0-F2 Rx49[1]= 1, this register is fixed at FFC2h. If D16F0-F2 Rx49[1]= 0, this register is fixed at 7E0Ah.

Offset Address: 85-84h (D16F4)
Power Management Capability Control / Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**PME Status** 0: Not active 1: Active
14:9	RO	0	**Reserved**
8	RW	0	**PME Enable** 0: Disable 1: Enable
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** 00: D0 01: D1 10: D2 11: D3 Hot

Offset Address: 86-87h (D16F4) – Reserved

Offset Address: 88h (D16F4)
Debug Port Capability ID **Default Value: 0Ah**

Bit	Attribute	Default	Description
7:0	RO	0Ah	**Debug Port Capability ID** If Rx4C[4] = 1, this register is fixed at 0Ah. If Rx4C[4] = 0, this register is fixed at 00h.

Offset Address: 89h (D16F4)
Next Item Pointer 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Next Item Pointer 2**

Offset Address: 8B-8Ah (D16F4)
Debug Port Base Offset **Default Value: 20A0h**

Bit	Attribute	Default	Description
15:0	RO	20A0h	**Debug Port Base Offset** If Rx4C[4] = 1, this register is fixed at 20A0h If Rx4C[4] = 0, this register is fixed at 0000h

Offset Address: 8C-FFh (D16F4) – Reserved

EHCI USB 2.0 I/O Registers (00-B3h)

These registers are compliant with the EHCI v1.0 standard. Refer to the EHCI v1.0 specification for further details.

EHCI Capabilities (00-0Bh)

I/O Offset Address: 00h (USB 2.0-IO)

Capability Register Length **Default Value: 10h**

Bit	Attribute	Default	Description
7:0	RO	10h	**Capability Register Length**

I/O Offset Address: 01h (USB 2.0-IO)– Reserved

I/O Offset Address: 03-02h (USB 2.0-IO)

Interface Version Number **Default Value: 0100h**

Bit	Attribute	Default	Description
15:0	RO	0100h	**Interface Version Number**

I/O Offset Address: 07-04h (USB 2.0-IO)

Structure Parameters **Default Value: 0000 3206h**

Bit	Attribute	Default	Description
31:0	RO	0000 3206h	**Structure Parameters** If Rx4C[4] = 1, fixed at 0010 3206h. If Rx4C[4] = 0, fixed at 0000 3206h.

I/O Offset Address: 0B-08h (USB 2.0-IO)

Capability Parameters **Default Value: 0000 6872h**

Bit	Attribute	Default	Description
31:0	RO	0000 6872h	**Capability Parameters**

I/O Offset Address: 0C-0Fh (USB 2.0-IO) - Reserved

Host Controller Operations (10-9Fh)

I/O Offset Address: 13-10h (USB 2.0-IO)

USB Command **Default Value: 0008 0000h**

Bit	Attribute	Default	Description
31:0	RW	0008 0000h	**USB Command**

I/O Offset Address: 17-14h (USB 2.0-IO)

USB Status **Default Value: 0000 1000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 1000h	**USB Status**

I/O Offset Address: 1B-18h (USB 2.0-IO)

USB Interrupt Enable **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**USB Interrupt Enable** 0: Disable 1: Enable

I/O Offset Address: 1F-1Ch (USB 2.0-IO)

USB Frame Index **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**USB Frame Index**

I/O Offset Address: 23-20h (USB 2.0-IO)

4G Segment Selector **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**4G Segment Selector**

I/O Offset Address: 27-24h (USB 2.0-IO)

Frame List Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Frame List Base Address**

I/O Offset Address: 2B-28h (USB 2.0-IO)

Next Asynchronous List Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Next Asynchronous List Address**

I/O Offset Address: 2C-4Fh (USB 2.0-IO) - Reserved

I/O Offset Address: 53-50h (USB 2.0-IO)

Configured Flag **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Configured Flag**

I/O Offset Address: 57-54h (USB 2.0-IO)

Port 1 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 3000h	**Port 1 Status / Control**

I/O Offset Address: 5B-58h (USB 2.0-IO)

Port 2 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 3000h	**Port 2 Status / Control**

I/O Offset Address: 5F-5Ch (USB 2.0-IO)

Port 3 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 3000h	**Port 3 Status / Control**

I/O Offset Address: 63-60h (USB 2.0-IO)

Port 4 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 3000h	**Port 4 Status / Control**

I/O Offset Address: 67-64h (USB 2.0-IO)

Port 5 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 3000h	**Port 5 Status / Control**

I/O Offset Address: 6B-68h (USB 2.0-IO)

Port 6 Status / Control **Default Value: 0000 3000h**

Bit	Attribute	Default	Description
31:0	RW1C	0000 3000h	**Port 6 Status / Control**

I/O Offset Address: 6C-9Fh (USB 2.0-IO) - Reserved

Debug Port Controller Operational Registers (A0-B3h)

I/O Offset Address: A3-A0h (USB 2.0-IO)

Debug Port Control / Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW/RO /RW1C	0000 0000h	**Debug Port Control / Status**

I/O Offset Address: A7-A4h (USB 2.0-IO)

Debug Port USB PIDs **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW/RO	0000 0000h	**Debug Port USB PIDs**

I/O Offset Address: AF-A8h (USB 2.0-IO)

Debug Port Data Buffer **Default Value: FFFF FFFF FFFF FFFFh**

Bit	Attribute	Default	Description
63:0	RW	FFFF FFFF FFFF FFFFh	**Debug Port Data Buffer**

I/O Offset Address: B3-B0h (USB 2.0-IO)

Debug Port Device Address **Default Value: 0000 7F01h**

Bit	Attribute	Default	Description
31:0	RW/RO	0000 7F01h	**Debug Port Device Address**

Device 17 Function 0 (D17F0) - Bus Control and Power Management

All registers are located in the device 17 function 0 configuration space of VX800 / VX820 Series. These registers are accessed through PCI configuration mechanism #1 via I/O address 0CF8h / 0CFCh.

PCI Configuration Space Header (00-3Fh)

Offset Address: 01-00h (D17F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 03-02h (D17F0)

Device ID **Default Value: 8353h**

Bit	Attribute	Default	Description
15:0	RO	8353h	**Device ID**

Offset Address: 05-04h (D17F0)

PCI Command **Default Value: 0003h**

Bit	Attribute	Default	Description
15:7	RO	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5:4	RO	0	**Reserved**
3	RO	0	**Respond To Special Cycle** Hardwired to 0 (Does not monitor special cycles).
2	RO	0	**PCI Master Function**
1	RW	1b	**Memory Space Access** Hardwired to 1 (Responds to memory space access).
0	RW	1b	**I/O Space Access** Hardwired to 1 (Responds to I/O space access).

Offset Address: 07-06h (D17F0)

PCI Status **Default Value: 0210h**

Bit	Attribute	Default	Description
15:	RO	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RO	0	**Signaled System Error** (SERR# asserted)
13	RO	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion** This chip does not assert Target-Abort.
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RO	0	**Master Data Parity Error** This bit is set when bus Master PERR# is asserted or observed; Rx04[6] should be set first to enable this function.
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Hardwired to 0 (Not implemented)
6:0	RO	10h	**Reserved** (Do not program)

Offset Address: 08h (D17F0)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D17F0)

Class Code **Default Value: 06 0100h**

Bit	Attribute	Default	Description
23:0	RO	060100h	**Class Code**

Offset Address: 0C-0Dh (D17F0) – Reserved

Offset Address: 0Eh (D17F0)

Header Type **Default Value: 80h**

Bit	Attribute	Default	Description
7:0	RO	80h	**Header Type** 80h means multi-function device.

Offset Address: 0Fh (D17F0)

BIST **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**BIST (Built In Self Test)** Fixed at 00h.

Offset Address: 10-2Bh (D17F0) – Reserved

Offset Address: 2D-2Ch (D17F0)

Subsystem Vendor ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D17F0)

Subsystem ID **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Subsystem ID**

Offset Address: 30-3Fh (D17F0) – Reserved

ISA Bus Control (40-49h)

Offset Address: 40h (D17F0)

ISA Bus Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Extra / Normal ISA Command Delay** 0: Normal 1: External
6	RW	0	**I/O Recovery Time** 0: Disable 1: Enable
5	RO	0	**Reserved**
4	RW	0	**ROM Write** 0: Disable 1: Enable
3	RW	0	**Double DMA Clock** 0: Disable 1: Enable
2	RW	0	**4D0 / 4D1 Support** 0: Disable 1: Enable
1	RW	0	**MEGA Cells (DMAC, INTC and TMRC) Shadow Register Read** 0: Disable 1: Enable
0	RW	0	**BCLK (Bus Clock) = PCLK (PCI Bus Clock) / 2** 0: Disable 1: Enable

Offset Address: 41h (D17F0)

ROM Decode Control **Default Value: 80h**

Setting these bits to 1 enables the indicated address range to be included in the LPC BIOS ROM address decode:

Bit	Attribute	Default	Description
7	RW	1b	**000E0000h-000EFFFFh**
6	RW	0	**FFF00000h-FFF7FFFFh** **FFB00000h-FFB7FFFFh**
5	RW	0	**FFE80000h-FFEFFFFFh** **FFA80000h-FFAFFFFFh**
4	RW	0	**FFE00000h-FFE7FFFFh** **FFA00000h-FFA7FFFFh**
3	RW	0	**FFD80000h-FFDFFFFFh** **FF980000h-FF9FFFFFh**
2	RW	0	**FFD00000h-FFD7FFFFh** **FF900000h-FF97FFFFh**
1	RW	0	**FFC80000h-FFCFFFFFh** **FF880000h-FF8FFFFFh**
0	RW	0	**FFC00000h-FFC7FFFFh** **FF800000h-FF87FFFFh**

Offset Address: 42h (D17F0)

Line Buffer Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DMA Line Buffer** Controls whether the DMA line buffer is used in DMA data transfer. 0: Disable 1: Enable. The bit when set to 1 indicates Master DMA waits until the line buffer is full (8 DW) before transmitting data (bit-6 must also be enabled to ensure that there are no coherency issues).
6	RW	0	**Gate INTR Assertion Until Line Buffer Flush Complete** This bit should be enabled if bit-7 is enabled. 0: Disable 1: Enable. INTR assertion is gated until the line buffer is flushed.
5	RW	0	**IRQ Flush Line Buffer When No DMA is Granted** This bit is to enable line buffer flushing when interrupt request is received. However, the line buffer flushing is performed only when no DMA is granted. 0: Disable 1: Enable
4	RW	0	**Uninterruptible Burst Read** 0: Disable 1: Enable. The PCI bus is not granted to DMA until burst read transactions from the host are completed.
3	RW	0	**Gate Serial IRQ Inputs Until Line Buffer Flush Completed** 0: Disable 1: Enable
2	RW	0	**IRQ Flush Line Buffer Even When DMA Is Granted** Line buffer is flushed even if DMA is granted with Rx42[5] =1 0: Disable 1: Enable
1:0	RO	0	**Reserved**

Offset Address: 43h (D17F0)
Delay Transaction Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Delayed Transactions (PCI Spec Rev 2.1)** This bit controls whether delayed transactions (delayed read / write and posted write) are enabled. 0: Disable 1: Enable
2	RW	0	**Delayed Transaction – Posted Write Only** This bit controls whether posted write is enabled, as opposed to bit-3 which controls whether delayed read / write as well as posted write are enabled. 0: Disable 1: Enable
1	RW	0	**Write Delay Transaction Timeout Timer** When enabled, if a delayed transaction (write cycle only) is not retried after 2^15 PCI clocks, the transaction is terminated. 0: Disable 1: Enable
0	RW	0	**Read Delay Transaction Timeout Timer** When enabled, if a delayed transaction (read cycle only) is not retried after 2^15 PCI clocks, the transaction is terminated. 0: Disable 1: Enable

Offset Address: 44h (D17F0) – Reserved

Offset Address: 45h (D17F0)
PCI PNP Interrupt Routing INTH# **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI INTH# Routing** (Refer to Table 26 PnP IRQ Routing Table)
3:0	RO	0	**Reserved**

Offset Address: 46h (D17F0)
PCI INTH# Interrupt Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**FIR / UART Multiplex with DVP or VCP Pad** 0: Multiplex with VCP pad when FIR or UART enabled 1: Multiplex with DVP pad when FIR or UART enabled Must set bit-6 =1 or set RxB0[0] =1 to enable this function. If both FIR and UART are disabled, neither DVP nor VCP pad is used.
6	RW	0	**UART Function Multiplex with DVP or VCP Pad** 0: Disable 1: Enable
5	RO	0	**Reserved**
4	RW	0	**PCI INT Sharing Control** 0: INTH# shared with INTD# 1: INTH# routing according to Rx45[7:4]
3	RW	0	**PCI INTH# Invert / Non-Invert Trigger** 0: Non-Invert 1: Invert
2:0	RO	0	**Reserved**

Note: For routing control of PCI INTA# ~ INTD#, see Device 17 Function 0 Rx54-57 and PnP IRQ Routing Table (Table 26).

Offset Address: 47h (D17F0)

PATA PAD Control **Default Value: 03h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**SPI IRQ Routing** 0000: IRQ0 0001: IRQ1 … … 1111: IRQ15
3:2	RW	00b	**IDE Pad Mux Select** 00: The pads mux is determined by strapping value (registers default value). 01: The IDE pads are dedicated to IDE (no matter what strapping values are). Others: Reserved
1	RW	1b	**Pull Up PATA IORDY** 0: Disable 1: Enable
0	RW	1b	**Pull Down PATA DMA Request** 0: Disable 1: Enable

Offset Address: 48h (D17F0)

Read Pass Write Control **Default Value: 0Ch**

Bit	Attribute	Default	Description
7	RW	0	**FSB Fixed at Low DW** 0: Disable. (Address Bit-2 is not masked) 1: Enable. (Force A2 from APIC FSB to low.) Address bit A2 controls whether data is in the lower (0) or upper (1) doubleword of a quadword sent to the CPU. When this bit is enabled, A2 is masked which means it is always 0 to select the lower doubleword.
6	RO	0	**Reserved**
5	RW	0	**CARDREAD Read Pass Write** 0: Disable. (A read cannot be performed before a preceding write has been completed.) 1: Enable. (The internal CARDREAD controller is allowed to perform a read before a preceding write.)
4	RW	0	**SDIO Read Pass Write** 0: Disable. (A read cannot be performed before a preceding write has been completed.) 1: Enable. (The internal SDIO controller is allowed to perform a read before a preceding write.)
3	RW	1b	**LPC Read Pass Write** 0: Disable. (A read cannot be performed before a preceding write has been completed.) 1: Enable. (LPC devices are allowed to perform a read before a preceding write.)
2	RW	1b	**IDE Read Pass Write** 0: Disable. (A read cannot be performed before a preceding write has been completed.) 1: Enable (The internal IDE controller is allowed to perform a read before a preceding write.)
1	RW	0	**USB Read Pass Write** 0: Disable. (A read cannot be performed before a preceding write has been completed.) 1: Enable. (The internal USB controllers are allowed to perform a read before a preceding write.)
0	RO	0	**Reserved**

Offset Address: 49h (D17F0)
SM Peripheral Device Control **Default Value: 20h**

Bit	Attribute	Default	Description
7	RW	0	**SERR from Host Directed to PMU (SMI, SCI)** 0: Disable 1: Enable
6	RO	0	**Reserved**
5	RW	1b	**Gated IRQ before SM Buffer Clean** Controls whether interrupt requests are gated until data is written to memory. 0: Disable 1: Enable
4	RW	0	**PCIM Address Stepping** 0: Disable 1: Enable
3	RW	0	**PCIM Wait State** 0: Disable 1: Enable
2	RW	0	**WSC Mask Off INTR** Controls whether INTR is masked until write snoop is complete. 0: Disable 1: Enable
1:0	RO	0	**Reserved**

LPC Firmware Memory Control (4A-4Bh)

Offset Address: 4Ah (D17F0)
LPC Firmware Memory Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**LPC Firmware Memory Base Address A[23:17]**
0	RW	0	**LPC Firmware Memory Programmable IDSEL** 0: Disable 1: Enable When enabled, the memory cycles in the address range, specified by Rx4A-4Bh, will be transferred into LPC firmware memory cycles no matter what the setting of Rx[59] is.

Offset Address: 4Bh (D17F0)
LPC Firmware Memory Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	000b	**LPC Firmware Memory Base Address Mask** Set bit-6 to 1 to mask A19 decoding. Set bit-5 to 1 to mask A18 decoding. Set bit-4 to 1 to mask A17 decoding.
3:0	RW	0	**LPC Firmware Memory IDSEL Value**

Miscellaneous Control (4C-4Fh)

Offset Address: 4Ch (D17F0)
IDE Interrupt Select **Default Value: 04h**

Bit	Attribute	Default	Description
7:6	RW	00b	**I/O Recovery Time Select** When Rx40[6] is enabled, this field determines the I/O recovery time. 00: 1 Bus Clock 01:2 Bus Clock 10: 4 Bus Clock 11:8 Bus Clock
5:4	RO	0	**Reserved**
3:2	RW	01b	**IDE Secondary Channel IRQ Routing** 00: IRQ14 01: IRQ15 10: IRQ10 11: IRQ11
1:0	RW	00b	**IDE Primary Channel IRQ Routing** 00: IRQ14 01: IRQ15 10: IRQ10 11: IRQ11

Offset Address: 4Dh (D17F0)

Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**LPC Firmware Memory 16 Bytes Burst Read** 0: Disable 1: Enable
6	RW	0	**LPC Firmware Memory 4 Bytes Burst Read / Write Access** 0: Disable 1: Enable
5	RW1	0	**Firmware Memory Burst Detection** Write 1 to start to detect the Firmware memory burst ability 0: Complete 1: Incomplete If the LPC Firmware memory supports 16-byte burst, the Rx4D[7] will be set to 1 after burst detection complete. If the LPC Firmware memory support 4-byte burst, the Rx4D[6] will be set 1 after burst detection complete.
4	RW	0	**LPC Firmware Memory IDSEL Value** 0: IDSEL is from Rx75[7:4] 1: IDSEL is from AD28-AD31 This control bit is valid when Rx4D[1] is set to 1.
3	RW	0	**Enable Fixed Path of External Interrupt Delivery Only in APIC Ch0 When the Interrupt Controller Has Not Been Masked Yet** 0: Disable 1: Enable
2	RW	0	**Serial IRQs Always be Shared in APIC Mode** 0: Disable 1: Enable
1	RW	0	**LPC Firmware Memory Cycle Configuration** 0: Only cycles which are targeting the specified programmable ROM space are converted into LPC firmware memory cycles (LPC ROM range and IDSEL value is determined by registers in Rx75-76h and Rx7C-7Fh) 1: All memory cycles are converted into LPC firmware memory cycles (IDSEL value is decided by Rx4D[4].) This register bit is used to select the memory ranges that are treated as LPC Firmware Memory space when Rx59[7] is set to 0.
0	RW	0	**LPC TPM Function** 0: Disable 1: Enable

Offset Address: 4Eh (D17F0)

Internal RTC Test Mode and Extra Feature Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**RTC High Bank Rx38-3F R/W Protect** 0: Disable (allow R/W) 1: Enable (Protect)
6	RW	0	**RTC Low Bank Rx38-3F R/W Protect** 0: Disable (allow R/W) 1: Enable (Protect)
5	RO	0	**Reserved**
4	RO	0	**RTC Last Write Status** 0: Last write was to port 70 1: Last write was to port 74
3	RW	0	**Enable RTC Port 74/75** The RTC is normally accessed though ports 70/74. This bit controls whether two extra ports (74 / 75) can be used to access the RTC. 0: Disable 1: Enable
2:0	RO	0	**Reserved**

Offset Address: 4Fh (D17F0)

PCI Reset Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**Software PCI Reset** Write 1 to generate PCI reset 0: Disable 1: Enable Software reset can also be initiated through I/O port CF9 as follows: Write 1 to I/O port CF9 bit-2 for software reset: if CF9 bit-1 is 0, INIT will be asserted; if CF9 bit-1 is 1 (default), PCIRST will be asserted.

Function Control (50-51h)

Offset Address: 50h (D17F0)

Function Control 1 **Default Value: 80h**

Bit	Attribute	Default	Description
7	RO	1b	**Reserved** (Do not program)
6	RO	0	**Reserved**
5	RW	0	**Device 16 Function 1 (USB 1.1 UHCI Port 2-3)** 0: Enable 1: Disable
4	RW	0	**Device 16 Function 0 (USB 1.1 UHCI Port 0-1)** 0: Enable 1: Disable
3	RW	0	**Device 15 Function 0 (Serial ATA and EIDE)** 0: Enable 1: Disable EIDE controller's ON/OFF configuration register is in D15F0. Please refer to the D15F0 IDE/SATA Support Option table for details.
2	RW	0	**Device 16 Function 2 (USB 1.1 UHCI Port 4-5)** 0: Enable 1: Disable
1	RW	0	**Device 16 Function 4 (USB 2.0 EHCI Port 0-5)** 0: Enable 1: Disable
0	RO	0	**Reserved**

Offset Address: 51h (D17F0)

Function Control 2 **Default Value: 0Dh**

Bit	Attribute	Default	Description
7	RW	0	**SDC (SD Controller) Disable** 0: Enable controller 1: Disable controller
6:5	RO	0	**Reserved**
4	RW	0	**SDIO Disable** 0: Enable 1: Disable
3	RW	1b	**Internal RTC** 0: Disable 1: Enable
2	RW	1b	**Internal PS2 Mouse** 0: Disable 1: Enable
1	RW	0	**Internal Keyboard Controller Configuration** 0: Disable 1: Enable
0	RW	1b	**Internal Keyboard Controller** 0: Disable 1: Enable

Serial IRQ, LPC and PC / PCI DMA Control (52-53h)

Offset Address: 52h (D17F0)

Serial IRQ, PCI / DMA Control and LPC Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**LPC Short Wait Abort** 0: Disable 1: Enable. In a short wait, the cycle is aborted after 8Ts.
5	RW	0	**LPC Frame Wait State** 0: Disable 1: Enable
4	RW	0	**LPC Stop to Start Frame Wait State** 0: Disable. One idle state is inserted between Stop and Start. 1: Enable. Stop is followed immediately by Start.
3	RW	0	**Serial IRQ** 0: Disable 1: Enable. (IRQ asserted via SERIRQ)
2	RW	0	**Serial IRQ Quiet Mode** 0: Continuous Mode 1: Quiet Mode
1:0	RW	00b	**Serial IRQ Start-Frame Width** 00: 4 PCI Clocks 01: 6 PCI Clocks 10: 8 PCI Clocks 11: 10 PCI Clocks

Offset Address: 53h (D17F0)

PC / PCI DMA Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PC/PCI DMA Control** 0: Disable PC/PCI DMA. (The signal balls are used for GPIO.) 1: Enable PC/PCI DMA
6	RW	0	**DMA Channel 7 for PC/PCI DMA** 0: Disable 1: Enable
5	RW	0	**DMA Channel 6 for PC/PCI DMA** 0: Disable 1: Enable
4	RW	0	**DMA Channel 5 for PC/PCI DMA** 0: Disable 1: Enable
3	RW	0	**DMA Channel 3 for PC/PCI DMA** 0: Disable 1: Enable
2	RW	0	**DMA Channel 2 for PC/PCI DMA** 0: Disable 1: Enable
1	RW	0	**DMA Channel 1 for PC/PCI DMA** 0: Disable 1: Enable
0	RW	0	**DMA Channel 0 for PC/PCI DMA** 0: Disable 1: Enable

Plug and Play Control – PCI (54-57h)

Offset Address: 54h (D17F0)

PCI Bus and CPU Interface Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved** The following bits all default to "Low Active Level " triggered (0)
4	RW	0	**Enable External Debug Card by SDIO Pad** 0: Disable 1: Enable
3	RW	0	**PCI INTA# Invert / Non-Invert Trigger** 0: Non-Invert 1: Invert
2	RW	0	**PCI INTB# Invert / Non-Invert Trigger** 0: Non-Invert 1: Invert
1	RW	0	**PCI INTC# Invert / Non-Invert Trigger** 0: Non-Invert 1: Invert
0	RW	0	**PCI INTD# Invert / Non-Invert Trigger** 0: Non-Invert 1: Invert

Note: PCI INTA-D# normally connect to PCI interrupt pins INTA-D# (see signal descriptions for more information).

Offset Address: 55h (D17F0)

PCI PNP Interrupt Routing 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI INTA# Routing** (see PnP IRQ Routing table)
3:0	RO	0	**Reserved** Always reads 0.

Offset Address: 56h (D17F0)

PCI PNP Interrupt Routing 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI INTC# Routing** (see PnP IRQ Routing Table)
3:0	RW	0	**PCI INTB# Routing** (see PnP IRQ Routing Table)

Offset Address: 57h (D17F0)

PCI PNP Interrupt Routing 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**PCI INTD# Routing** (see PnP IRQ Routing Table)
3:0	RO	0	**Reserved** Always reads 0.

Table 26. PnP IRQ Routing Table

Bit Value	IRQ-N
0000	Reserved
0001	IRQ1
0010	Reserved
0011	IRQ3
0100	IRQ4
0101	IRQ5
0110	IRQ6
0111	IRQ7
1000	Reserved
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	Reserved
1110	IRQ14
1111	IRQ15

Note1. FIR IRQ routing is set via D17F0 RxB1[7:4].
Note2. UART2 IRQ routing is set via D17F0 RxB2[7:4].
UART1 IRQ routing is set via D17F0 RxB2[3:0].

When enable internal APIC, PCI devices and internal function IRQ routing are shown as below:

Table 27. Internal APIC, PCI Devices IRQ Routing Table

INTA#, HPET IRQ	IRQ16
INTB#, HPET IRQ	IRQ17
INTC#, HPET IRQ	IRQ18
INTD#, HPET IRQ	IRQ19
UHCI Port 0-1 IRQ and Card Boot IRQ	IRQ20
SATA IRQ and UHCI Port 4-5 IRQ	IRQ21
UHCI Port 2-3 IRQ and SDIO IRQ	IRQ22
INTH#, Card Reader IRQ and EHCI Port 0-5	IRQ23

Table 28. HPET IRQ Routing Table

Mode	Timer 0	Timer 1	Timer 2
Legacy Mode	IRQ0(PIC) / IRQ2(APIC)	IRQ8(PIC) / IRQ8(APIC)	—
Non-legacy Mode	IRQ16-19 for APIC only	IRQ16-19 for APIC only	IRQ11, IRQ16-19 for APIC only

GPIO and Miscellaneous Control (58-5Bh)

Offset Address: 58h (D17F0)

South Module Miscellaneous Control 1 **Default Value: 20h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Internal APIC** 0: Disable 1: Enable
5	RW	1b	**South Module Interrupt Cycles are Sync. by 33 MHz Clock** 0: Disable (8MHz) 1: Enable
4	RW	0	**South Module PCI Cycle Decode** 0: Subtractive 1: Positive
3	RW	0	**RTC High Bank Access** 0: Disable 1: Enable
2	RW	0	**RTC Rx32 Write Protect** 0: Disable (not protected) 1: Enable (write protected)
1	RW	0	**RTC Rx0D Write Protect** 0: Disable (not protected) 1: Enable (write protected)
0	RW	0	**RTC Rx32 Map to Century Byte** Controls whether RTC Rx32 is mapped to the century byte. 0: Disable 1: Enable

Offset Address: 59h (D17F0)

South Module Miscellaneous Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**LPC/SPI Memory Space** 0: All memory cycles are forwarded to LPC/SPI 1: Memory cycles with address in the ranges specified by the ROM Memory Address Range registers are forwarded to LPC/SPI.
6	RO	0	**Reserved**
5	RW	0	**LPC RTC** 0: Disable 1: Enable
4	RW	0	**LPC Keyboard** 0: Disable (ISA Keyboard) 1: Enable (LPC Keyboard)
3	RW	0	**Port 62h / 66h (MCCS#) to LPC** 0: Disable 1: Enable
2	RW	0	**Port 62h / 66h (MCCS#) Decoding** 0: Disable 1: Enable
1	RW	0	**Mask A20M# Active** 0: Disable. (A20M# acts normally) 1: Enable (A20M# signal de-asserted)
0	RW	0	**NMI on PCI Parity Error** 0: Disable 1: Enable (to generate NMI, Port 61[3] and Port 70[7] must also be set)

Note: To trigger NMI assertion correctly, both IO port 61 bit3 and IO port70 bit7 must be set to 0 since data parity error report is combined with IOCHK.

Offset Address: 5Ah (D17F0)

DMA Bandwidth Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**DMA Channel 7 Bandwidth** 0: Normal 1: Improved
6	RW	0	**DMA Channel 6 Bandwidth** 0: Normal 1: Improved
5	RW	0	**DMA Channel 5 Bandwidth** 0: Normal 1: Improved
4	RW	0	**DMA Single Transfer Mode Bandwidth** 0: Normal 1: Improved
3	RW	0	**DMA Channel 3 Bandwidth** 0: Normal 1: Improved
2	RW	0	**DMA Channel 2 Bandwidth** 0: Normal 1: Improved
1	RW	0	**DMA Channel 1 Bandwidth** 0: Normal 1: Improved
0	RW	0	**DMA Channel 0 Bandwidth** 0: Normal 1: Improved

Note: The above bits determine if DMA bandwidth is improved for the specified channel. If enabled, bandwidth improvement is accomplished by reducing the transaction latency between the DMA Controller and the LPC Bus Controller.

Offset Address: 5Bh (D17F0)

Miscellaneous Control **Default Value: 01h**

Bit	Attribute	Default	Description
7	RW	0	**LPC Firmware Memory Read TRDY 1 Wait State** 0: Disable 1: Enable
6	RW	0	**Control the Destination of IO Port 0x80** 0: IO Port 0x80 goes to ISA bus. 1: IO Port 0x80 goes to LPC bus.
5	RW	0	**PCI/DMA Memory Cycles Output to PCI Bus** 0: Disable 1: Enable
4	RW	0	**APIC Clock Gating Enable** 0: Disable 1: Enable
3	RW	0	**Bypass APIC De-Assert Message** 0: Disable 1: Enable
2	RO	0	**Reserved**
1	RW	0	**Enable NM PCIe Interrupt** 0: Disable 1: Enable
0	RW	1b	**Dynamic Clock Stop** 0: Disable 1: Enable

Programmable Chip Select (PCS) Control (5C-66h)

Offset Address: 5D-5Ch (D17F0)

PCS 0 I/O Port Address **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**PCS 0 I/O Port Address**

Offset Address: 5F-5Eh (D17F0)

PCS 1 I/O Port Address **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**PCS 1 I/O Port Address**

Offset Address: 61-60h (D17F0)

PCS 2 I/O Port Address **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**PCS 2 I/O Port Address**

Offset Address: 63-62h (D17F0)

PCS 3 I/O Port Address **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**PCS 3 I/O Port Address**

Offset Address: 65-64h (D17F0)

PCS I/O Port Address Mask **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RW	0	**PCS 3 I/O Port Address Mask 3-0** 0000: Decode range is 1 byte. 0001: Decode range is 2 bytes. 0011: Decode range is 4 bytes. 0111: Decode range is 8 bytes. 1111: Decode range is 16 bytes.
11:8	RW	0	**PCS 2 I/O Port Address Mask 3-0** 0000: Decode range is 1 byte. 0001: Decode range is 2 bytes. 0011: Decode range is 4 bytes. 0111: Decode range is 8 bytes. 1111: Decode range is 16 bytes.
7:4	RW	0	**PCS 1 I/O Port Address Mask 3-0** 0000: Decode range is 1 byte. 0001: Decode range is 2 bytes. 0011: Decode range is 4 bytes. 0111: Decode range is 8 bytes. 1111: Decode range is 16 bytes.
3:0	RW	0	**PCS 0 I/O Port Address Mask 3-0** 0000: Decode range is 1 byte. 0001: Decode range is 2 bytes. 0011: Decode range is 4 bytes. 0111: Decode range is 8 bytes. 1111: Decode range is 16 bytes.

Offset Address: 66h (D17F0)

PCS Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**PCS 3** 0: Disable 1: Enable
2	RW	0	**PCS 2** 0: Disable 1: Enable
1	RW	0	**PCS 1** 0: Disable 1: Enable
0	RW	0	**PCS 0** 0: Disable 1: Enable

Output Control (67h)

Offset Address: 67h (D17F0)

Output and PCS Control **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW	0	**PCS 3 IO Cycle is Directed to** PCS 3 is defined in Rx63-62. 0: Internal ISA Bus 1: LPC Bus
6	RW	0	**PCS 2 IO Cycle is Directed to** PCS 2 is defined in Rx61-60. 0: Internal ISA Bus 1: LPC Bus
5	RW	0	**PCS 1 IO Cycle is Directed to** PCS 1 is defined in Rx5F-5E. 0: Internal ISA Bus 1: LPC Bus
4	RW	0	**PCS 0 IO Cycle is Directed to** PCS 0 is defined in Rx5D-5C. 0: Internal ISA Bus 1: LPC Bus
3	RO	0	**Reserved**
2	RW	1b	**FERR# Voltage** 0: 2.5V 1: 1.5V
1:0	RW	0	**IDE Pad Driving Select** 00: 12 mA 01: 13.3 mA 10: 14 mA 11: 15.2 mA

Note: PCS IO cycle can be claimed in two ways:

1. Positive decoding: Set D17F0 Rx58[4] and the corresponding bits in (D17F0 Rx6C[1:0], D17F0 Rx6F[5]) to 1, and program the PCS address range.
2. Subtractive decoding: Program the PCS address range.

High Precision Event Timers (HPET) (68-6Bh)

Offset Address: 68h (D17F0)

HPET Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**High Precision Event Timers** 0: Disable 1: Enable
6:4	RO	0	**Reserved**
3	RW	0	**PCS 3 256-Byte IO Range Decoding Enable** 0: Disable 1: Enable
2	RW	0	**PCS 2 256-Byte IO Range Decoding Enable** 0: Disable 1: Enable
1	RW	0	**PCS 1 256-Byte IO Range Decoding Enable** 0: Disable 1: Enable
0	RW	0	**PCS 0 256-Byte IO Range Decoding Enable** 0: Disable 1: Enable

Offset Address: 6B-69h (D17F0)

HPET Address **Default Value: 00h**

Bit	Attribute	Default	Description
23:2	RW	0	**HPET Memory Base Address [31:10]**
1:0	RO	0	**Reserved**

ISA Decoding Control (6C-6Fh)

Offset Address: 6Ch (D17F0)

ISA Positive Decoding Control 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**On-Board I/O (Ports 00-FFh) Positive Decoding** 0: Disable 1: Enable
6	RW	0	**Microsoft-Sound System I/O Port Positive Decoding** 0: Disable 1: Enable (bits 5-4 determine the decode range)
5:4	RW	00b	**Microsoft-Sound System I/O Decode Range** 00: 0530h-0537h 01: 0604h-060Bh 10: 0E80h-0E87h 11: 0F40h-0F47h
3	RW	0	**APIC Positive Decoding** 0: Disable 1: Enable
2	RW	0	**ROM Positive Decoding** 0: Disable 1: Enable
1	RW	0	**PCS1# Positive Decoding** 0: Disable 1: Enable
0	RW	0	**PCS0# Positive Decoding** 0: Disable 1: Enable

Offset Address: 6Dh (D17F0)

ISA Positive Decoding Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**FDC Positive Decoding** 0: Disable 1: Enable
6	RW	0	**LPT Positive Decoding** 0: Disable 1: Enable
5:4	RW	00b	**LPT Decode Range** 00: 3BCh-3BFh, 7BCh-7BEh 01: 378h-37Fh, 778h-77Ah 10: 278h-27Fh, 678h-67Ah 11: Reserved
3	RW	0	**Game Port Positive Decoding** 0: Disable 1: Enable
2	RW	0	**MIDI Positive Decoding** 0: Disable 1: Enable
1:0	RW	00b	**MIDI Decode Range** 00: 300h-303h 01: 310h-313h 10: 320h-323h 11: 330h-333h

Offset Address: 6Eh (D17F0)

ISA Positive Decoding Control 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**COM Port B Positive Decoding** 0: Disable 1: Enable
6:4	RW	000b	**COM Port B Decode Range** 000: 3F8h-3FFh (COM1) 001: 2F8h-2FFh (COM2) 010: 220h-227h 011: 228h-22Fh 100: 238h-23Fh 101: 2E8h-2EFh (COM4) 110: 338h-33Fh 111: 3E8h-3EFh (COM3)
3	RW	0	**COM Port A Positive Decoding** 0: Disable 1: Enable
2:0	RW	000b	**COM Port A Decode Range** 000: 3F8h-3FFh (COM1) 001: 2F8h-2FFh (COM2) 010: 220h-227h 011: 228h-22Fh 100: 238h-23Fh 101: 2E8h-2EFh (COM4) 110: 338h-33Fh 111: 3E8h-3Efh (COM3)

Offset Address: 6Fh (D17F0)

ISA Positive Decoding Control 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SPI Positive Decoding Control** 0: Disable 1: Enable
6	RW	0	**LPC TPM Positive Decoding** 0: Disable 1: Enable
5	RW	0	**PCS2# and PCS3# Positive Decoding** 0: Disable 1: Enable
4	RW	0	**I/O Port 0CF9h Positive Decoding** 0: Disable 1: Enable
3	RW	0	**Floppy Disk Controller (FDC) Decoding Range** 0: Primary 1: Secondary
2	RW	0	**Sound Blaster Positive Decoding** 0: Disable 1: Enable
1:0	RW	00b	**Sound Blaster Decode Range** 00: 220-22F, 230-233h 01: 240-24F, 250-253h 10: 260-26F, 270-273h, 11: 280-28F, 290-293h

Offset Address: 70-73h (D17F0) – Reserved

PCI I/O Cycle Control (74-7Fh)

Offset Address: 74h (D17F0)

PCI I/O Cycle Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Forward Card Reader DMA Cycles to the External PCI Bus** 0: Disable 1: Enable
6	RW	0	**Forward SDIO DMA Cycles to the External PCI Bus** 0: Disable 1: Enable
5	RW	0	**Forward LPC DMA Cycles to the External PCI Bus** 0: Disable 1: Enable
4	RW	0	**Forward LAN Cycles to the External PCI Bus** 0: Disable 1: Enable
3	RW	0	**Forward USB 2.0 Cycles to the External PCI Bus** 0: Disable 1: Enable
2	RW	0	**Forward USB 1.1 Cycles to the External PCI Bus** 0: Disable 1: Enable
1	RW	0	**Forward SATA Cycles to the External PCI Bus** 0: Disable 1: Enable
0	RW	0	**Forward PATA Cycles to the External PCI Bus** 0: Disable 1: Enable

Offset Address: 75h (D17F0)

LPC ROM Memory Address Range **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Firmware Memory IDSEL for All Memory Range** Used when Rx4D[1] is 1 and Rx4D[4] is 0.
3	RW	0	**Select LPC ROM Memory Address Range 1 {FF700000h-FF7FFFFFh, FF300000h-FF3FFFFFh}** 0: Not select 1: Select
2	RW	0	**Select LPC ROM Memory Address Range 2 {FF600000h-FF6FFFFFh, FF200000h-FF2FFFFFh}** 0: Not select 1: Select
1	RW	0	**Select LPC ROM Memory Address Range 3 {FF500000h-FF5FFFFFh, FF100000h-FF1FFFFFh}** 0: Not select 1: Select
0	RW	0	**Select LPC ROM Memory Address Range 4 {FF400000h-FF4FFFFFh, FF000000h-FF0FFFFFh}** 0: Not select 1: Select

Offset Address: 76h (D17F0)

Firmware Memory IDSEL 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Firmware Memory IDSEL for the Two 1MB Memory Ranges {FF500000h-FF5FFFFFh, FF100000h-FF1FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0	**Firmware Memory IDSEL for the Two 1MB Memory Ranges {FF400000h-FF4FFFFFh, FF000000h-FF0FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 77h (D17F0)
Firmware Memory IDSEL 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0000	**Firmware Memory IDSEL for the Two 1MB Memory Ranges {FF700000h-FF7FFFFFh, FF300000h-FF3FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0000	**Firmware Memory IDSEL for the Two 1MB Memory Ranges {FF600000h-FF6FFFFFh, FF200000h-FF2FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 78-7Bh (D17F0) – Reserved

Offset Address: 7Ch (D17F0)
Firmware Memory IDSEL 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFC80000h-FFCFFFFFh, FF880000h-FF8FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFC00000h-FFC7FFFFh, FF800000h-FF87FFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 7Dh (D17F0)
Firmware Memory IDSEL 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFD80000h-FFDFFFFFh, FF980000h-FF9FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFD00000h-FFD7FFFFh, FF900000h-FF97FFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 7Eh (D17F0)

Firmware Memory IDSEL 5 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFE80000h-FFEFFFFFh, FFA80000h-FFAFFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFE00000h-FFE7FFFFh, FFA00000h-FFA7FFFFh}** 0000: IDSEL0 … 1111: IDSEL15

Offset Address: 7Fh (D17F0)

Firmware Memory IDSEL 6 **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Firmware Memory IDSEL for the Two 512K Memory Ranges { FFB80000h-FFBFFFFFh, 000E0000h-000FFFFFh}** 0000: IDSEL0 … 1111: IDSEL15
3:0	RW	0	**Firmware Memory IDSEL for the Two 512K Memory Ranges {FFF00000h-FFF7FFFFh, FFB00000h-FFB7FFFFh }** 0000: IDSEL0 … 1111: IDSEL15

Power Management-Specific Configuration Registers (80-CFh)

Offset Address: 80h (D17F0)

PM General Configuration 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Enable GPIO7 (THRMTRIP#) as SLPBTN#** 0: Disable 1: Enable
5	RW	0	**Power Button De-bounce** 0: Disable 1: Enable
4	RO	0	**Reserved**
3	RW	0	**Microsoft Sound Monitor in Audio Access** This bit controls monitoring on I/O cycle to the sound port as specified in D17F0 Rx6C[5:4]. 0: Disable 1: Enable
2	RW	0	**Game Port Monitor in Audio Access** This bit controls monitoring on I/O cycle to the game port: 200h-207h. 0: Disable 1: Enable
1	RW	0	**Sound Blaster Monitor in Audio Access** This bit controls monitoring on I/O cycle to the sound blaster port as specified in D17F0 Rx6F[1:0] or 388h-38bh. 0: Disable 1: Enable
0	RW	0	**MIDI Monitor in Audio Access** This bit controls monitoring on I/O cycle to the midi port as specified in D17F0 Rx6D[1:0]. 0: Disable 1: Enable

Offset Address: 81h (D17F0)

PM General Configuration 2 **Default Value: 04h**

Bit	Attribute	Default	Description
7	RW	0	**Enable ACPI I/O** 0: Disable access to ACPI I/O block. 1: Allow access to Power Management I/O Register Block (see offset 89-88h to set the base address for this register block). The definitions of the registers in the Power Management I/O Register Block are included later in this document, following the Power Management Subsystem overview.
6:4	RO	0	**Reserved** Always reads 0.
3	RW	0	**ACPI Timer with 32 Bit Width**
2	RW	1b	**RTC Enable Signal Gated with PSON (SUSC#) in Soft-Off Mode** This bit controls whether RTC control signals are gated during system suspend state. This is to prevent CMOS and Power-Well register data from being corrupted during system on/off when the control signals (PWRGD) may not be stable. 0: Disable 1: Enable
1	RW	0	**Throttle Timer Base Clock Period (for STPCLK#)** This bit controls the timer tick base for the throttle timer. 0: 30 usec (480 usec cycle time when using a 4-bit timer) 1: 1 msec (16 msec cycle time when using a 4-bit timer) The timer tick base can be further lowered to 7.5 usec (120 usec cycle time when using a 4-bit timer) by setting Rx8D[4] = 1. When Rx8D[4] = 1, the setting of this bit is ignored.
0	RO	0	**Reserved**

Offset Address: 82h (D17F0)

ACPI Interrupt Select **Default Value: 40h**

Bit	Attribute	Default	Description
7	RO	0	**ATX / AT Power Indicator** 0: ATX 1: AT
6	RO	1b	**PSON (SUSC#) Current State** 0: PSON Gating Active 1: PSON Gating Complete During system on/off, this status bit reports whether PSON gating state has been completed, 0 meaning that gating is active now and 1 meaning that gating is complete. Software should not access any CMOS or Power-Well registers until this bit becomes 1 if Rx81[2] = 1.
5	RO	0	**Reserved** Always reads 0.
4	RO	0	**SUSC# AC-Power-On Default Value** This bit reflects the value of RTC Index 0D bit-7. If 0, the system is configured to "default on" when power is connected.
3:0	RW	0000b	**ACPI IRQ Select** This field determines the routing of the ACPI IRQ. 0000: Disabled 0001: IRQ1 0010: Reserved 0011: IRQ3 0100: IRQ4 0101: IRQ5 0110: IRQ6 0111: IRQ7 1000: IRQ8 1001: IRQ9 1010: IRQ10 1011: IRQ11 1100: IRQ12 1101: IRQ13 1110: IRQ14 1111: IRQ15

Offset Address: 83h (D17F0)

Internal Timer Read Test **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Internal Timer Read Test**

Offset Address: 85-84h (D17F0)

IRQn as Primary Interrupt **Default Value: 0000h**

If an IRQ is enabled as a Primary IRQ, its assertion can be used as a wakeup event in system power management. This register is used in conjunction with:

- PMIO Rx28[7] – Primary Resume Status
- PMIO Rx2A[7] – Primary Resume Enable

If a device's IRQ is enabled as a Primary Interrupt, once the device asserts the IRQ, the PMIO Rx28[7] status bit will be set to 1 to report the occurrence of the Primary IRQ. If PMIO Rx2A[7] is set to 1 to enable the Resume-on-Primary-IRQ function, the IRQ becomes a wakeup event.

Bit	Attribute	Default	Description
15	RW	0	**IRQ15 as Primary Interrupt Channel** 0: Disable 1: Enable
14	RW	0	**IRQ14 as Primary Interrupt Channel** 0: Disable 1: Enable
13	RW	0	**IRQ13 as Primary Interrupt Channel** 0: Disable 1: Enable
12	RW	0	**IRQ12 as Primary Interrupt Channel** 0: Disable 1: Enable
11	RW	0	**IRQ11 as Primary Interrupt Channel** 0: Disable 1: Enable
10	RW	0	**IRQ10 as Primary Interrupt Channel** 0: Disable 1: Enable
9	RW	0	**IRQ9 as Primary Interrupt Channel** 0: Disable 1: Enable
8	RW	0	**IRQ8 as Primary Interrupt Channel** 0: Disable 1: Enable
7	RW	0	**IRQ7 as Primary Interrupt Channel** 0: Disable 1: Enable
6	RW	0	**IRQ6 as Primary Interrupt Channel** 0: Disable 1: Enable
5	RW	0	**IRQ5 as Primary Interrupt Channel** 0: Disable 1: Enable
4	RW	0	**IRQ4 as Primary Interrupt Channel** 0: Disable 1: Enable
3	RW	0	**IRQ3 as Primary Interrupt Channel** 0: Disable 1: Enable
2	RO	0	**Reserved** Always reads 0
1	RW	0	**IRQ1 as Primary Interrupt Channel** 0: Disable 1: Enable
0	RW	0	**IRQ0 as Primary Interrupt Channel** 0: Disable 1: Enable

Offset Address: 87-86h (D17F0)

IRQn as Secondary Interrupt **Default Value: 0000h**

This register is used in conjunction with:

- PMIO Rx28[1] – Secondary Event Timer Timeout Status
- PMIO Rx2A[1] – SMI on Secondary Event Timer Timeout

Secondary IRQ is different from Primary IRQ in systems that resume due to a Secondary IRQ event can return to the suspend state after the secondary event timer times out. For this to work, PMIO Rx2A[1] needs to be set to one to enable SMI-on-Secondary-Event-Timer-Timeout (when PMIO Rx28[1] = 1). The timer's count value can be set via Rx90[27:26].

Bit	Attribute	Default	Description
15	RW	0	**IRQ15 as Secondary Interrupt Channel** 0: Disable 1:Enable
14	RW	0	**IRQ14 as Secondary Interrupt Channel** 0: Disable 1:Enable
13	RW	0	**IRQ13 as Secondary Interrupt Channel** 0: Disable 1:Enable
12	RW	0	**IRQ12 as Secondary Interrupt Channel** 0: Disable 1:Enable
11	RW	0	**IRQ11 as Secondary Interrupt Channel** 0: Disable 1:Enable
10	RW	0	**IRQ10 as Secondary Interrupt Channel** 0: Disable 1:Enable
9	RW	0	**IRQ9 as Secondary Interrupt Channel** 0: Disable 1:Enable
8	RW	0	**IRQ8 as Secondary Interrupt Channel** 0: Disable 1:Enable
7	RW	0	**IRQ7 as Secondary Interrupt Channel** 0: Disable 1:Enable
6	RW	0	**IRQ6 as Secondary Interrupt Channel** 0: Disable 1:Enable
5	RW	0	**IRQ5 as Secondary Interrupt Channel** 0: Disable 1:Enable
4	RW	0	**IRQ4 as Secondary Interrupt Channel** 0: Disable 1:Enable
3	RW	0	**IRQ3 as Secondary Interrupt Channel** 0: Disable 1:Enable
2	RO	0	**Reserved** Always reads 0.
1	RW	0	**IRQ1 as Secondary Interrupt Channel** 0: Disable 1:Enable
0	RW	0	**IRQ0 as Secondary Interrupt Channel** 0: Disable 1:Enable

Offset Address: 89-88h (D17F0)

Power Management I/O Base **Default Value: 0001h**

Bit	Attribute	Default	Description
15:7	RW	0	**ACPI IO Base Register**
6:0	RO	01h	**Hardwired to 01h.**

Offset Address: 8Ah (D17F0)

Auto-Switching Processor Power State **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**C2 to C3 / C4 Auto Mode** 0: Processor power state will not be auto-switched from C2 to the previous C3 or C4 state. 1: In C2 state, if no bus master activity after a period of time, it will return to the previous C3 or C4 state. Note: This bit is used in conjunction with bit 3. If bit 3 is 0, this bit must be 0.
3	RW	0	**C3/C4 to C2 Auto Mode** 0: Bus master request is treated as a break event, when it occurs, processor will be switched from C3/C4 to C0. 1: Bus master request, when asserted, will cause the processor power state be switched from C3/C4 to C2 and automatically enable the bus arbiter, so that snooping and memory access could be processed correctly.
2	RW	0	**Bus Master Status Report Disable** 0: PMIO Rx0[4] is set when there is bus master activity. 1: PMIO Rx0[4] is not set by bus master activity. Notes: 1. It is expected that if bit 3 is set, bit 2 should also be set. 2. PMIO Rx0[4] will be set by LPC DMA or LPC masters even if this bit is set.
1	RW	0	**C4 to C3 Auto Mode** 0: When entering C4 state, even if bus master request occurs before VRDSLP assertion, the processor will be moved to C4 state. 1: When entering C4 state, if bus master request occurs before VRDSLP assertion, the C4 state transition will be aborted and the processor will stay in C3 state.
0	RW	0	**Bus Master Request Delays C3/C4 Mode** 0: When entering C3/C4 state, if bus master request occurs before SLP# assertion, the processor will be moved to C3/C4 without waiting. 1: When entering C3/C4 state, if bus master request occurs before SLP# assertion, the processor will stay in C2 state then moved into C3/C4 state after bus master request is finished.

Offset Address: 8Bh (D17F0) – Reserved

Offset Address: 8Ch (D17F0)

Host Power Management Control **Default Value: 07h**

Bit	Attribute	Default	Description
7:4	RW	0000b	**Thermal Duty Cycle** This field determines STPCLK# duty cycle when the THRM# signal is asserted. The duty cycle of STPCLK#, if not activated by the assertion of THRM#, is controlled by PMIO Rx10[3:0]. The duty cycle indicates the percentage of host bus activation (the lower the percentage, the lower the performance and the higher the power savings). If the Throttling Timer Width (Rx8D[6:5]) is set to 3-bit width, bit-0 of this field should be set to 0 (and the performance increment is in unit of 12.5%). If the Throttling Timer Width is set to 2-bit width, bits 1-0 of this field should be set to 0 (and the performance increment is in unit of 25%). **Throttling Timer Width** 4-Bit / 3-Bit / 2-Bit 0000 Reserved / Reserved / Reserved 0001 6.25% / Reserved / Reserved 0010 12.50% / 12.50% / Reserved 0011 18.75% / Reserved / Reserved 0100 25.00% / 25.00% / 25.00% 0101 31.25% / Reserved / Reserved 0110 37.50% / 37.50% / Reserved 0111 43.75% / Reserved / Reserved 1000 50.00% / 50.00% / 50.00% 1001 56.25% / Reserved / Reserved 1010 62.50% / 62.50% / Reserved 1011 68.75% / Reserved / Reserved 1100 75.00% / 75.00% / 75.00% 1101 81.25% / Reserved / Reserved 1110 87.50% / 87.50% / Reserved 1111 93.75% / Reserved / Reserved
3	RW	0	**THRM# Enable** 0: Disable 1: Enable
2	RW	1b	**Processor Break Events** 0: Disable 1: Enable Allows processor break events, such as FERR#, to wake up processor from C1/C2/C3/C4 to C0.
1	RW	1b	**Disable Bus Arbiter C3/C4 Auto Gating** 0: Bus arbiter is auto-disabled when processor state is switched to C3/C4 state. 1: Disable the bus arbiter auto-disabled mode. The arbiter is disabled through IO Port 22h.
0	RO	1b	**Reserved**

Offset Address: 8Dh (D17F0)

Throttle / Clock Stop Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Throttle Timer Reset** Write 1 to reset the throttle timer.
6:5	RW	00b	**Throttle Timer Counter Width** This field determines the counter width of the throttle timer, which in conjunction with the throttle timer tick determines the cycle time of STPCLK#. For example, if a 2-bit timer and a 7.5 usec timer tick are selected, the STPCLK# cycle time would be 30 usec (2**2 x 7.5). If a 4-bit timer and a 7.5 usec timer tick is selected, the cycle time would be 120 usec (2**4 x 7.5). 0x: 4-Bit 10: 3-Bit 11: 2-Bit (See also Rx8C[7:4] and PMIO Rx10[3:0].)
4	RW	0	**Use Fast Clock (7.5us) as Throttle Timer Tick** 0: Timer Tick is selected by Rx81[1]. 1: Timer Tick is 7.5usec (setting of Rx81[1] is ignored)
3	RW	0	**SMI# Low Level Output** 0: Disable 1: Enable (during an SMI event, SMI# is held low until SMI event status is cleared)
2	RW	0	**Internal Clock Stop for PCI Idle** This bit controls whether the internal PCI clock is stopped when CLKRUN# is high. 0: PCI clock is not stopped 1: PCI clock is stopped
1	RW	0	**Internal Clock Stop During C3/C4** This bit controls whether the internal PCI clock is stopped during C3/C4 state. 0: PCI clock is not stopped 1: PCI clock is stopped
0	RW	0	**Internal Clock Stop During Suspend** This bit controls whether the internal PCI clock is stopped during Suspend state. 0: PCI clock is not stopped 1: PCI clock is stopped

Offset Address: 8E-8Fh (D17F0) – Reserved

Offset Address: 93-90h (D17F0)

Power Management Timer Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:30	RW	00b	**Power Conserve Mode Timer Period** 00: 1/16 second 01: 1/8 second 10: 1 second 11: 1 minute
29	RW1C	0	**Power Conserve Mode Status** This bit reads 1 when in Conserve Mode
28	RW	0	**Power Conserve Mode** This bit controls whether conserve mode (through throttling) is enabled. When this bit is set, the system can enter conserve mode when primary activity is not detected within a given time period (determined by bits 31-30 of this register). Primary activity is defined in PMIO Rx33-30. 0: Disable 1: Enable
27:26	RW	00b	**Secondary Event Timer Count Value** 00: 2 milliseconds 01: 64 milliseconds 10: ½ second 11: by EOI + 0.25 milliseconds
25	RW1C	0	**Secondary Event Occurred Status** This bit reads 1 to indicate that a secondary event has occurred (to resume the system from suspend) and the secondary event timer is counting down.
24	RW	0	**Secondary Event Timer Enable** 0: Disable 1: Enable
23:16	RO/WO	0	**GP1 Timer Count Value** (base defined by bits 5-4) Write to load count value; Read to get current count
15:8	RO/WO	0	**GP0 Timer Count Value** (base defined by bits 1-0) Write to load count value; Read to get current count
7	RW	0	**GP1 Timer Enable** When this bit is set to 1, the GP1 timer loads the value defined in bits 23-16 of this register and starts counting down. The GP1 timer will be reloaded at the occurrence of peripheral events that are enabled in the GP Timer Reload Enable Register (PMIO Rx38). If no such event occurs and the GP1 timer counts down to zero, then the GP1 Timer Timeout Status bit PMIO Rx28[3] is set to one. Additionally, if the GP1 Timer Timeout Enable bit PMIO Rx2A[3] is set, an SMI is generated.
6	RW	0	**GP1 Timer Automatic Reload** 0: GP1 Timer stops at 0 1: Reload GP1 timer automatically after counting down to 0
5:4	RW	00b	**GP1 Timer Tick Select** 00: Disable 01: 1/16 second 10: 1 second 11: 1 minute
3	RW	0	**GP0 Timer Start** When this bit is set to 1, the GP0 timer loads the value defined by bits 15-8 of this register and starts counting down. The GP0 timer is reloaded at the occurrence of peripheral events that are enabled in the GP Timer Reload Enable Register (PMIO Rx38). If no such event occurs and the GP0 timer counts down to zero, then the GP0 Timer Timeout Status bit PMIO Rx28[2] is set to one. Additionally, if the GP0 Timer Timeout Enable bit PMIO Rx2A[2] is set, then an SMI is generated.
2	RW	0	**GP0 Timer Automatic Reload** 0: GP0 Timer stops at 0 1: Reload GP0 timer automatically after counting down to 0
1:0	RW	00b	**GP0 Timer Tick Select** 00: Disable 01: 1/16 second 10: 1 second 11: 1 minute

Offset Address: 94h (D17F0)

Miscellaneous Configuration 1 (Power Well) **Default Value: 88h**

Bit	Attribute	Default	Description
7	RW	1b	**SMBus Clock Select** 0: SMBus from divider of 14.318 Mhz 1: SMBus from RTC clock Note: If set, SMBus always uses RTC clock. If not set, SMBus uses RTC clock in suspend mode and uses 128K when RxD2[2] is set.
6	RW	0	**Check Power Button Enable when PWRBTN# Asserted to Resume from STR / STD** 0: No Check 1: Check. Power Button Enable is controlled through register Rx3[0] of ACPI I/O Space.
5	RW	0	**Reset North Module PLL During S1 State** Set this bit to 1 will let North Module PLL stop during S1. 0: Disable 1: Enable
4	RW	0	**KBC D2 Command Interrupt Gating**
3	RW	1b	**Pull up Pad of Card Reader / SDIO Power Switch**
2	RW	0	**Multi-Function Signals: GPO[9:8] vs. SUS[C:B]# Select** 0: SUS[C:B]# 1: GPO[9:8]
1:0	RW	00b	**GPO0 Output Select** This field controls the GPO0 output signal for Pulse Width Modulation. 00: Fixed output port (output value is defined by PMIO Rx4C[0]). 01: GPO0 output is 1 Hz "SLOWCLK". 10: GPO0 output is 4 Hz "SLOWCLK". 11: GPO0 output is 16 Hz "SLOWCLK".

Offset Address: 95h (D17F0)

Miscellaneous Configuration 2 (Power Well) **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**SUS[A:C]# to CPUSTP# and CPUSTP# to SUSSTAT# (internal signal) Delay Select** This bit controls the following two minimum delays of the resume process: A. De-assertion of SUS[A:C]# to the de-assertion of CPUSTP#. B. De-assertion of CPUSTP# to the de-assertion of SUSSTAT# (internal signal). 0: (A) 16msec, (B) 1 msec 1: (A) 1msec, (B) 125 usec
6	RW	1b	**SUSSTAT# (internal signal) De-asserted Before PWRGD when Resume from STD** 0: Disable 1: Enable (SUSSTAT# is de-asserted before PWRGD when resuming from STD)
5	RW	0	**Keyboard / Mouse Port Swap** This bit determines whether the keyboard and mouse ports can be swapped. 0: Disable 1: Enable
4	RW	0	**PWRGD Reset**
3	RW	0	**Multi-Function Signals: SMBDT2, SMBCK2 vs. GPIO0, GPIO1 Select** 0: SMBDT2, SMBCK2 1: GPIO0, GPIO1
2	RW	0	**SMB Slave (through SMB Port2)** This bit controls whether external SMB masters can access internal SMB registers (for Alert-On-LAN). 0: Enable 1: Disable
1	RO	0	**Reserved**
0	RW	0	**USB Wakeup for POS / STR / STD / Soft Off** This bit controls whether USB Wakeup is enabled when PMIO Rx20[14] = 1. This allows wakeup from STR, STD, Soft Off and POS. 0: Disable 1: Enable

Note: SUSSTAT# provides the information on host clock status from SM to NM.

Offset Address: 96h (D17F0)

Miscellaneous Configuration 3 (Battery Well) **Default Value: 0Fh**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved** Always reads 0.
5	RO	0	**Reserved**
4	RW	0	**Enable SMB GPOUT6 and GPOUT7 as PWRGD and PWRBTN** Enable ASF function. Used by Alert-on-LAN to reset the system.
3:0	RW	Fh	**CPU Frequency Strapping Value** Output through NMI, INTR, IGNNE#, and A20M# during RESET#. The value written to this field is reflected through NMI, INTR, IGNNE#, and A20M# during RESET# to determine the multiplier of the CPU's internal frequency. If the CPU hangs due to inappropriate settings written here, the GP3 timer (second timeout) can be used to initiate a system reboot (PMIO Rx42[2] set to 1). Refer to the BIOS Porting Guide for additional details.

Offset Address: 97h (D17F0)

Miscellaneous Configuration 3 (Power Well) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Wait for PWRGD Low Before Wake up during S3/S4 State** 0: No qualified PWRGD. 1: Wake up after PWRGD is low.
6	RW	0	**Multi-Function Signals: MSDT, MSCK vs. GPIO2, GPIO3 Select** 0: MSDT, MSCK 1: GPIO2, GPIO3
5	RW	0	**Enable PCIe PME S1 State Wake Event** 0: Disable 1: Enable
4:3	RO	0	**Reserved**
2	RW	0	**SMBALT and PWRBTN Pull Up** 0: Enable 1: Disable (Not pull up)
1	RW	0	**PCIe Wake Enable (PMIO Rx2[14]) Attribution Option** 0: Disable 1: Enable
0	RW	0	**Multi-Function Signals: KBDT / KBC_CPURST#, KBCK / A20GATE vs. GPIO4, GPIO5 Select** 0: KBDT / KBC_CPURST#, KBCK / A20GATE 1: GPIO4, GPIO5

Offset Address: 98h (D17F0)
GP2 / GP3 Timer Control **Default Value: 10h**

Bit	Attribute	Default	Description
7	RW	0	**GP3 Timer Start** When set to 1, the GP3 timer loads the value specified by Rx9A and starts counting down. The GP3 timer is reloaded at the occurrence of certain events enabled in the GP Timer Reload Enable Register (PMIO Rx38). If no such event occurs and the GP3 timer counts down to zero, then the GP3 Timer Timeout Status bit PMIO Rx28[13] is set to one, a SMI will be asserted if the GP3 Timer Timeout Enable bit PMIO Rx2A[13] is set.
6	RW	0	**GP3 Timer Automatic Reload** 0: GP3 Timer stops at 0 1: Reload GP3 timer automatically after counting down to 0
5:4	RW	01b	**GP3 Timer Tick Select** 00: Disable 01: 1/16 second 10: 1 second 11: 1 minute
3	RW	0	**GP2 Timer Start** When set to 1, the GP2 timer loads the value specified by Rx99 and starts counting down. The GP2 timer is reloaded at the occurrence of certain events enabled in the GP Timer Reload Enable Register (PMIO Rx 38). If no such event occurs and the GP2 timer counts down to zero, then the GP2 Timer Timeout Status bit PMIO Rx28[12] is set to one, a SMI will be asserted if the GP2 Timer Timeout Enable bit PMIO Rx2A[12] is set.
2	RW	0	**GP2 Timer Automatic Reload** 0: GP2 Timer stops at 0 1: Reload GP2 timer automatically after counting down to 0
1:0	RW	00b	**GP2 Timer Tick Select** 00: Disable 01: 1 ms 10: 1 second 11: 1 minute

Offset Address: 99h (D17F0)
GP2 Timer Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO/WO	0	**Write will set GP2 Timer Load Value.** **Read will get GP2 Timer Current Count.**

Offset Address: 9Ah (D17F0)
GP3 Timer Counter **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO/WO	0	**Write will set GP3 Timer Load Value.** **Read will get GP3 Timer Current Count.**

Offset Address: 9Bh (D17F0)
Boot Option Bit Mask (ASF) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Lock Sleep Button** To lock sleep button means SLPBTN# is always de-asserted. 0: Disable 1: Enable
5	RW	0	**Lock Keyboard Controller Access** 0: Enable 1: Disable
4:3	RO	0	**Reserved**
2	RW	0	**Lock Reset Button** To lock reset button means Reset button is always de-asserted. 0: Disable 1: Enable
1	RW	0	**Lock Power Button** To lock reset button means PWRBTN# button is always de-asserted. 0: Disable 1: Enable
0	RO	0	**Reserved**

Offset Address: 9Ch (D17F0)

ASF Byte Write Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Command Decode Table** 00h: Reserved 01h: Generate ASF wakeup event and SCI or SMI event PMIO Rx3A[0]: SCI enable, PMIO Rx3B[0]: SMI enable. 02h: Unconditional Power Down 03h: System Reset 04h: Power Cycle Reset 05h: Reserved 06h: Watch Dog Timer Reload 07h: Reserved

Offset Address: 9Dh (D17F0)

ASF Data Message1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**ASF Data Message 1**

Offset Address: 9Eh (D17F0)

ASF Data Message 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**ASF Data Message 2**

Offset Address: 9Fh (D17F0)

Voltage Change Function Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Reserved**
3	RW	0	**PAD TP7 Output Selection** 0: PAD TP7 outputs internal suspend power 32K clock 1: PAD TP7 is an input PAD
2	RW	0	**Multi-Function Signals: GPO0 vs. SUSA# Selecttion** 0: SUSA# 1: GPO0
1	RW	0	**Card Reader Voltage Change Function** 0: Disable 1: Enable
0	RW	0	**SDIO Port 0 Voltage Change Function** 0: Disable 1: Enable

Offset Address: A0-AFh (D17F0) – Reserved

UART / FIR Misc Control Registers (B0-BFh)

Offset Address: B0h (D17F0)

UART and FIR Control **Default Value: 08h**

Bit	Attribute	Default	Description
7	RW	0	**UART2 MIDI Mode Enable** 0: Disable 1: Enable
6	RW	0	**UART1 MIDI Mode Enable** 0: Disable 1: Enable
5	RW	0	**UART 2** 0: Disable 1: Enable
4	RW	0	**UART 1** 0: Disable 1: Enable
3	RW	1b	**APIC C4P State Mode Control** 0: Disable 1: Enable
2	RW	0	**FIR Positive Decoding** 0: Disable 1: Enable
1	RW	0	**FIR DMA Channel Select** 0: Dual DMA Channel 1: Signal DMA Channel
0	RW	0	**FIR** 0: Disable 1: Enable

Offset Address: B1h (D17F0)

FIR IRQ and DRQ Routing **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**FIR IRQ Routing** (see PnP IRQ Routing Table)
3:2	RW	00b	**FIR2 DRQ Routing** 00: Disable 01: DRQ5 10: DRQ6 11: DRQ7
1:0	RW	00b	**FIR1 DRQ Routing** 00: Disable 01: DRQ5 10: DRQ6 11: DRQ7

Offset Address: B2h (D17F0)

UART IRQ Routing **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**UART2 IRQ Routing** (see PnP IRQ Routing Table)
3:0	RW	0	**UART1 IRQ Routing** (see PnP IRQ Routing Table)

Offset Address: B3h (D17F0) – Reserved

Offset Address: B4h (D17F0)

UART 1 I/O Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**UART 1 Positive Decoding** 0: Disable 1: Enable
6:0	RW	0	**UART 1 I/O Base Address A[9:3]**

Offset Address: B5h (D17F0)

UART 2 I/O Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**UART 2 Positive Decoding** 0: Disable 1: Enable
6:0	RW	0	**UART 2 I/O Base Address A[9:3]**

Offset Address: B6h (D17F0)
FIR I/O Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**FIR IO Base Address A[15:8]**

Offset Address: B7h (D17F0)
COM Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**Enable UART DMA I/O Cycle Positive Decoding** 0: Disable 1: Enable
3	RW	0	**Enable UART DMA Function** 0: Disable 1: Enable
2	RW	0	**COM2 Speed-up Mode Enable** 0: Disable 1: Enable
1	RW	0	**COM1 Speed-up Mode Enable** 0: Disable 1: Enable
0	RO	0	**Reserved**

Offset Address: B8h (D17F0)
UART DMA I/O Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:2	RW	0	**UART DMA Control Registers Base Address A[7:2]**
1:0	RO	0	**Reserved**

Offset Address: B9h (D17F0)
UART DMA I/O Base Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**UART DMA Control Registers Base Address A[15:8]**

Offset Address: BAh (D17F0)
COM1 DMA Channel Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	000b	**COM1 Receive DMA Channel Select** 000: No channel selected 100: DMA Channel 0 101: DMA Channel 1 110: DMA Channel 2 111: DMA Channel 3 Others: reserved
3	RO	0	**Reserved**
2:0	RW	000b	**COM1 Transmit DMA Channel Select** 000: No channel selected 100: DMA channel 0 101: DMA channel 1 110: DMA channel 2 111: DMA channel 3 Others: reserved

Offset Address: BBh (D17F0)
COM2 DMA Channel Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	000b	**COM2 Receive DMA Channel Select** 000: No channel selected 100: DMA channel 0 101: DMA channel 1 110: DMA channel 2 111: DMA channel 3 Others: reserved
3	RO	0	**Reserved**
2:0	RW	000b	**COM2 Transmit DMA Channel Select** 000: No channel selected 100: DMA channel 0 is selected for COM2 transmit. 101: DMA channel 1 is selected for COM2 transmit. 110: DMA channel 2 is selected for COM2 transmit. 111: DMA channel 3 is selected for COM2 transmit. Others: reserved

Offset Address: BCh (D17F0)
SPI Memory Map Base Address 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SPI Memory Map Base Address A[15:8]**

Offset Address: BDh (D17F0)
SPI Memory Map Base Address 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SPI Memory Map Base Address A[23:16]**

Offset Address: BEh (D17F0)
SPI Memory Map Base Address 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SPI Memory Map Base Address A[31:24]**

Offset Address: BFh (D17F0) – Reserved

Offset Address: C3-C0h (D17F0)
Power Management Capability **Default Value: 0002 0001h**

Bit	Attribute	Default	Description
31:16	RO	0002h	**Power Management Capability** 0002h indicates that: 1. This function does not support D2 or D1 power state. 2. This function does not require PCI clock to generate PME#. 3. This function complies with PCI Power Management Interface Specification Revision 1.1.
15:8	RO	0	**Next Pointer** 0 indicates that there are no additional items in the Capabilities List.
7:0	RO	01h	**Capability ID**

Offset Address: C7-C4h (D17F0)
Power Management Capability **Default Value: 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Power Management Capability Data**
23:16	RO	0	**PM CSR (Certificate Signing Request) P2P Support Extensions**
15:2	RO	0	**PM Control / Status (D0/D3 Only) High**
1:0	RW	00b	**PM Control / Status (D0/D3 Only) Low** 00: D0 11: D3

Offset Address: C8-CFh (D17F0) – Reserved

System Management Bus-Specific Configuration Registers (D0-E7h)

Offset Address: D1-D0h (D17F0)
SMBus I/O Base **Default Value: 0001h**

Bit	Attribute	Default	Description
15:4	RW	0	**SMBus I/O Base (16-byte I/O space)**
3:0	RO	01h	**Hardwire to 01h.** 01h: I/O Base Address

Offset Address: D2h (D17F0)
SMBus Host Configuration **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**SMBus Alert IRQ SCI / SMI Select** 0: SMI 1: SCI
2	RW	0	**SMBus Clock from 128K Source** Divider from 14.318Mhz
1	RW	0	**SMBus IRQ** Enable SMBus IRQ assertion.
0	RW	0	**Enable SMBus Host Controller** 0: Disable SMB controller functions 1: Enable SMB controller functions

Offset Address: D3h (D17F0)
SMBus Host Slave Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Host Slave Command**

Offset Address: D4h (D17F0)
SMBus Slave Address for Port 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**SMBus Slave Address for Port 1**
0	RW	0	**Read / Write for Shadow Port 1**

Offset Address: D5h (D17F0)
SMBus Slave Address for Port 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RW	0	**SMBus Slave Address for Port 2**
0	RW	0	**Read / Write for Shadow Port 2**

Offset Address: D6h (D17F0)
SMBus Revision ID **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**SMBus Revision ID**

Offset Address: D7-DFh (D17F0) – Reserved

Offset Address: E0h (D17F0)
GPI Trigger Level for SCI / SMI Generation **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**GPI Input Trigger Mode for SCI/SMI Generation** Bit [7:2]: GPIO [13:10, 1:0] Bit 1: PEHPSGPI3 Bit 0: PEPMESGPI2 Refer to PMIO Rx50 for more detail of PEHPSGPI3 and PEPMESGPI2. 0: Falling edge 1: Rising edge

Offset Address: E1h (D17F0)
GPI SCI / SMI Select **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**GPI SCI / SMI Select** Bit [7:2]: GPIO [13:10, 1:0] Bit 1: PEHPSGPI3 Bit 0: PEPMESGPI2 Refer to PMIO Rx50 for more detail of PEHPSGPI3 and PEPMESGPI2. 0: SCI 1: SMI

Offset Address: E2h (D17F0)
Internal PCIe and NM PLL Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Inhibit C4 State During USB Isochronous Transaction** 0: Disable 1: Enable
6:3	RO	0	**Reserved**
2	RW	0	**Enable Internal Hot Plug to Generate SCI/SMI** 0: Disable 1: Enable
1	RW	0	**Enable Internal PM_PME to Generate SCI/SMI** 0: Disable 1: Enable
0	RO	0	**Reserved**

Offset Address: E3h (D17F0)

Pullup Option **Default Value: 03h**

Bit	Attribute	Default	Description
7	RW	0	**PCIe Hot Plug Wakeup in S1 State** 0: Not supported 1: Supported
6	RW	0	**VR Change Timer Select** 0: 7.5 us 1: 45us
5	RW	0	**Enable SDIO Device 2 Break Event** 0: Disable 1: Enable
4	RW	0	**Enable SDIO Device 1 Break Event** 0: Disable 1: Enable
3	RW	0	**Enable Card Boot Break Event** 0: Disable 1: Enable
2	RW	0	**Multi-Function Signals: PCIDREQ, PCIDGNT vs. GPIO8, GPIO9 Select** 0: PCIDREQ, PCIDGNT 1: GPIO8, GPIO9
1	RW	1b	**Enable IO Pads (INTR, IGNNE#, A20M#, SMI#, INIT#, FERR#, THRMTRIP#) to Use CPU Power Rail**
0	RW	1b	**Enable IO Pads (DPSLP#, STPCLK#, SLP#) to Use CPU Power Rail**

Offset Address: E4h (D17F0)

Multi Function Select 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Short C3/C4 Mode** When enabled, fast entry and recovery latencies of C3/C4 state are performed. In detail, please refer to C3/C4 latency configuration tables. 0: Normal entry and recovery latencies 1: Fast entry and recovery latencies
6	RW	0	**Multi-Function Signals: SYSIDLE vs. GPO10 Select** 0: SYSIDLE 1: GPO10
5	RW	0	**Multi-Function Signals: CSTATE1, C4PSTOP# vs. GPO5, GPO6 Select** 0: CSTATE1, C4PSTOP# 1: GPO5, GPO6
4	RW	0	**Multi-Function Signals: SPKR vs. GPO7 Select** 0: SPKR 1: GPO7
3	RW	0	**Enable Slow C4 Recovery Mode in Short C4 Setting** When enabled with short C4 setting, slow recovery latencies of C3/C4 state are performed. In detail, please refer to C3/C4 latency configuration tables. 0: Normal entry and recovery latencies 1: Slow recovery latencies
2	RW	0	**Multi-Function Signals: SATALED0# vs. GPO4 Select** 0:SATALED0# 1:GPO4
1	RW	0	**Multi-Function Signals: SPI vs. GPIO Select** 0: 1: SPIDI GPI0 SPICLK GPIO6 SPIDO GPO1 SPISS1# GPO2 SPISS0# GPO3
0	RW	0	**Multi-Function Signals: THRMTRIP# vs. GPIO7 Select** 0: THRMTRIP# 1: GPIO7

Table 29. C3 Latency Configuration Table

<table>
<tr><th>RxEC[2]</th><th>RxE4[7]</th><th>STOP GRANT
to SLP# 1->0</th><th>SLP# 1->0
to CPUSTP# 1->0</th><th>Break Event
to CPUSTP# 0->1</th><th>CPUSTP# 0->1
to SLP# 0->1</th><th>SLP# 0->1
to STPCLK# 0->1</th></tr>
<tr><td>0</td><td>0</td><td>7.5~15 us</td><td>8~11.25 us</td><td>7.5~15 us</td><td><table><tr><th>RxFC[2:1]</th><th>DPSLP# 0->1
to SLP# 0->1</th></tr><tr><td>00</td><td>7~8 us</td></tr><tr><td>01</td><td>14.5~15.5 us</td></tr><tr><td>10</td><td>22~23 us</td></tr><tr><td>11</td><td>29.5~30.5 us</td></tr></table></td><td>7.5 us</td></tr>
<tr><td>0</td><td>1</td><td>0.83~1.66 us</td><td>1~1.25 us</td><td>0.83~1.66 us</td><td><table><tr><th>RxFC[2:1]</th><th>DPSLP# 0->1
to SLP# 0->1</th></tr><tr><td>00</td><td>0.83 us</td></tr><tr><td>01</td><td>7.5~16 us</td></tr><tr><td>10</td><td>15~23.5 us</td></tr><tr><td>11</td><td>22.5~31 us</td></tr></table></td><td>0.83 us</td></tr>
<tr><td>1</td><td>x</td><td>0.56~1.12 us</td><td>0.84 us</td><td>0.56~1.12 us</td><td>0.56 us</td><td>0.56 us</td></tr>
</table>

Table 30. C4 Latency Configuration Table

<table>
<tr><th>RxEC[2]</th><th>RxE4[7]</th><th>STOP GRANT
to
SLP# 1->0</th><th>SLP# 1->0
to
CPUSTP# 1->0</th><th>CPUSTP# 1->0
to
VRDSLP 0->1</th><th>Break Event
to
VRDSLP 1->0</th><th>VRDSLP 1->0
to
CPUSTP# 0->1</th><th>CPUSTP# 0->1
to
SLP# 0->1</th><th>SLP# 0->1
to
STPCLK# 0->1</th></tr>
<tr><td>0</td><td>0</td><td>7.5~15 us</td><td>8~11.25 us</td><td>3.75~7.5 us</td><td>0~7.5 us</td><td><table><tr><th>RxE5[7] & RxE3[6]</th><th>VRDSLP 1->0 to CPUSTP# 0->1</th></tr><tr><td>0x</td><td>90~132 us</td></tr><tr><td>10</td><td>31~39 us
or 7.5 us</td></tr><tr><td>11</td><td>30~70 us</td></tr></table></td><td><table><tr><th>RxFC[2:1]</th><th>DPSLP# 0->1 to SLP# 0->1</th></tr><tr><td>00</td><td>7~8 us</td></tr><tr><td>01</td><td>14.5~15.5 us</td></tr><tr><td>10</td><td>22~23 us</td></tr><tr><td>11</td><td>29.5~30.5 us</td></tr></table></td><td>7.5 us</td></tr>
<tr><td>0</td><td>1</td><td>0.83~1.66 us</td><td>1~1.25 us</td><td>0.63~0.83 us</td><td>0~0.83 us</td><td><table><tr><th>RxE4[3]</th><th>RxE5[7] & RxE3[6]</th><th>VRDSLP 1->0 to CPUSTP# 0->1</th></tr><tr><td rowspan="3">0</td><td>0x</td><td>11.5~13.5 us</td></tr><tr><td>10</td><td>3.3~4.5 us
or 0.84 us</td></tr><tr><td>11</td><td>3.5~7.5 us</td></tr><tr><td rowspan="3">1</td><td>0x</td><td>35~45us</td></tr><tr><td>10</td><td>Not suggested</td></tr><tr><td>11</td><td>20~25 us</td></tr></table></td><td><table><tr><th>RxFC[2:1]</th><th>DPSLP# 0->1 to SLP# 0->1</th></tr><tr><td>00</td><td>0.83 us</td></tr><tr><td>01</td><td>7.5~16 us</td></tr><tr><td>10</td><td>15~23.5 us</td></tr><tr><td>11</td><td>22.5~31 us</td></tr></table></td><td>0.83 us</td></tr>
<tr><td>1</td><td>x</td><td>0.56~1.12 us</td><td>0.84 us</td><td>0.28~0.56 us</td><td>0~0.56 us</td><td colspan="2">0.56 us</td><td>0.56 us</td></tr>
</table>

Offset Address: E5h (D17F0)

Multi Function Select 2 **Default Value: 01h**

Bit	Attribute	Default	Description
7	RW	0	**C4 VR Recovery Latency Selection Bit** VRDSLP de-assertion to DPSLP de-assertion latency. In detail, please refer to C3/C4 latency configuration tables. RxE5[7] / RxE3[6] — VR Change Timer 00 — 90~100 us 01 — 90~100 us 10 — 7.5~15 us 11 — 30~45 us RxE4[7] and RxEC[2] must set to 0.
6	RW	0	**AGPBZ# as Source of Bus Master Status (BM_STS)** 0: Disable 1: Enable
5	RW	0	**Enable North Bridge Interrupt to Wake up Cx State** 0: Disable 1: Enable
4	RO	0	**Reserved**
3	RW	0	**CPU Frequency Change** 0: DPSLP# 1: Disable (output high) 0: VRDSLP 1: Disable (output high)
2	RW	0	**PCS1 Chip Select Output via PDIOW#** When enabled, if any C2P cycle hits PCS1 I/O port address range (D17F0 Rx5E-5F), the chip select of PCS1 is asserted and output via PDIOW#. 0: Disable 1: Enable
1	RW	0	**PCS0 Chip Select Output via PDIOR#** When enabled, if any C2P cycle hits PCS0 I/O port address range (D17F0 Rx5C-5D), the chip select of PCS0 is asserted and output via PDIOR#. 0: Disable 1: Enable
0	RW	1b	**SATALEDO# Enable** 0: Disable 1: Enable

Offset Address: E6h (D17F0)

Cx State Break Event Enable 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Parallel IDE / SATA Bus Master as Break Event** 0: Disable 1: Enable
6	RO	0	**Reserved**
5	RW	0	**PCI Bus Master as Break Event** 0: Disable 1: Enable
4	RW	0	**Card Reader as Break Event** 0: Disable 1: Enable
3	RW	0	**NM Bus Master as Break Event** 0: Disable 1: Enable
2	RW	0	**EHCI Bus Master as Break Event** 0: Disable 1: Enable
1	RW	0	**UHCI Bus Master as Break Event** 0: Disable 1: Enable
0	RW	0	**HDAC / PCI DMA Bus Master as Break Event** 0: Disable 1: Enable

Offset Address: E7h (D17F0)

Cx State Break Event Enable 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable APIC Cycle Reflect to ALL Bus Master Activity Effective Signal** 0: Disable 1: Enable
6	RW	0	**HD Audio Record FIFO Status Reflect Control** Enable HD audio record FIFO not empty signal reflect to HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. 0: Disable 1: Enable
5	RW	0	**C4P Can Be Inhibited When HD Audio Play Run Bit Is Open** 0: Disable 1: Enable
4	RW	0	**C4P Can Be Inhibited When HD Audio Record Run Bit Is Open** 0: Disable 1: Enable
3	RW	0	**HD Audio CORB / RIRB RW Pointer Compare Reflect to DMA Control** Enable HD audio CORB / RIRB write / read pointer compare signal reflect to HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. This run bit reflects to bus master status (PMIO Rx0[4]). 0: Disable 1: Enable
2	RW	0	**HD Audio CORB / RIRB Run Bit Reflect to DMA Control** Enable HD audio CORB / RIRB run bit reflect to HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. This run bit reflects to bus master status (PMIO Rx0[4]). 0: Disable 1: Enable
1	RW	0	**HD Audio Record Run Bit Reflect to DMA Control** Enable HD audio record run bit reflect to HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. This run bit reflects to bus master status (PMIO Rx0[4]). 0: Disable 1: Enable
0	RW	0	**HD Audio Play Run Bit Reflect to DMA Control** Enable HD audio play run bit reflect to HD/PCI DMA bus master activity effective signal if HDAC break event enable is set. This run bit reflects to bus master status (PMIO Rx0[4]). 0: Disable 1: Enable

Watchdog Timer Registers (E8-FFh)

Offset Address: EB-E8h (D17F0)

Watchdog Timer Memory Base **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RW	0	**Watchdog Timer Memory Base**
7:0	RO	0	**Hardwire to 0.** 0: Memory base address

Offset Address: ECh (D17F0)

Watchdog Timer Control & C3 Latency Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Extends Delay from SLP# De-assert to STPCLK# De-assert** In detail, please refer to C3/C4 latency configuration tables. 0: Disable 1: Enable
2	RW	0	**Enable Fast C3 Mode** Enable C4 is not allowed. In detail, please refer to C3/C4 latency configuration tables. 0: Depends on RxE4[7] setting 1: Enable fast C3 mode
1	RW	0	**Enable Watch Dog Timer** If set, can be reset only by PCIRST#. 0: Disable 1: Enable
0	RW	0	**Watchdog Timer Memory** 0: Disable 1: Enable

Offset Address: ED-FBh (D17F0) – Reserved

Offset Address: FCh (D17F0)

Processor Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**PCIERST1# of PCIe Device on PCB Is Driven from GPIO11 Output Signal** 1: Output GPIO11 0: Output PCIERST1#
3	RW	0	**PCIERST0# of PCIe Device on PCB Is Driven from GPIO10 Output Signal** 1: Output GPIO10 0: Output PCIERST0#
2:1	RW	0	**DPSLP# to SLP# Latency Adjustment** ***When RxE4[7] =0:*** 00: 7.5 us 01: 15 us 10: 22.5 us 11: 30 us ***When RxE4[7]=1:*** 00: 0.83 us 01: 1.5~7.5 us 10: 7.5~15 us 11: 10~22.5 us
0	RO	0	**Reserved**

Offset Address: FD-FFh (D17F0) – Reserved

ACPI IO Space Registers (PMIO 00-0Bh)

Offset Address: 01-00h (PMIO)

Power Management Status **Default Value: 0000h**

The bits in this register are set by hardware and can be reset by software by writing a one to the desired bit position.

Bit	Attribute	Default	Description
15	RW1C	0	**Wakeup Status** This bit is set when the system is in the suspend state (S1 … S5) and an enabled resume event occurs. Upon setting this bit, the system automatically transitions from the suspend state to the normal working state (from C3/C4 to C0 for the processor).
14	RW1C	0	**PCIe Wakeup Status** This bit is set when PCIe is waken up.
13:12	RO	0	**Reserved**
11	RW1C	0	**Power Status** 0: Core power on 1: Abnormal power off
10	RW1C	0	**RTC Alarm Status** This bit is set when the RTC generates an alarm (on assertion of the RTC IRQ signal).
9	RW1C	0	**Sleep Button Status** This bit is set when the sleep button is pressed (SLPBTN# signal asserted low).
8	RW1C	0	**Power Button Status** This bit is set when the PWRBTN# signal is asserted low. If the PWRBTN# signal is held low for more than four seconds, this bit is cleared, the Power Button Status bit is set, and the system will transition into the soft off state.
7:6	RO	0	**Reserved**
5	RW1C	0	**Global Status** This bit is set by hardware when the BIOS Release bit (PMIO Rx2C[1]) is set (typically by an SMI routine to release control of the SCI / SMI lock). When this bit is cleared by software (by writing a one to this bit position) the BIOS Release bit is also cleared at the same time by hardware.
4	RW1C	0	**Bus Master Status** This bit is set when a bus master request is asserted. All PCI master, ISA master and ISA DMA devices are included.
3:1	RO	0	**Reserved**
0	RW1C	0	**ACPI Timer Carry Status** The bit is set when the 23rd (31st) bit of the 24 (32) bit ACPI power management timer changes.

Offset Address: 03-02h (PMIO)

Power Management Enable **Default Value: 0100h**

The bit, which is defined in this register, corresponds to the bit in the same location of the Power Management Status Register at offset 1-0.

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14	RW	0	**Enable PCIe Wake** 0: Disable 1: Enable
13:11	RO	0	**Reserved**
10	RW	0	**RTC Alarm Enable** This bit, when set, triggers either a SCI or a SMI (depending on the setting of the SCI Enable bit) to be generated when the RTC Status bit is set. 0: Disable 1: Enable
9	RW	0	**Sleep Button Enable** This bit, when set, triggers either a SCI or a SMI (depending on the setting of the SCI Enable bit) to be generated when the Sleep Button Status bit is set.
8	RW	1b	**Power Button** This bit, when set, triggers either a SCI or a SMI (depending on the setting of the SCI Enable bit) to be generated when the Power Button Status bit is set. 0: Disable 1: Enable
7:6	RO	0	**Reserved**
5	RW	0	**Global Enable** This bit, when set, triggers either a SCI or a SMI (depending on the setting of the SCI Enable bit) to be generated when the Global Status bit (PMIO Rx0[5]) is set. 0: Disable 1: Enable
4:1	RO	0	**Reserved**
0	RW	0	**ACPI Timer Enable** This bit, when set, triggers either a SCI or a SMI (depending on the setting of the SCI Enable bit) to be generated when the Timer Status bit is set. 0: Disable 1: Enable

Offset Address: 05-04h (PMIO)

Power Management Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	WO	0	**Soft Resume** This bit is used to allow a system using an AT power supply to operate as if an ATX power supply were being used. Refer to the BIOS Porting Guide for implementation details. 0: Disable 1: Enable
14	RO	0	**Reserved**
13	WO	0	**Sleep Enable** This is a write-only bit; reads from this bit always return zero. Writing a one to this bit causes the system to sequence into the sleep (suspend) state defined by the Sleep Type, bits 12-10, field.
12:10	RW	000b	**Sleep Type** 000: Normal On 001: Suspend to RAM (STR) 010: Suspend to Disk (STD) (also called Soft Off). The VCC power plane is turned off while the VSUS33 and VBAT planes remain on. 011: Reserved 100: Power On Suspend without Reset 101: Power On Suspend with CPU/PCI Reset 11x: Reserved In any sleep state, there is minimal interface between powered and non-powered planes so that the effort for hardware design may be well managed.
9	RO	0	**Reserved**
8	RW	0	**Suspend-to-Disk Command Generates System Reset Only** 0: Disable. STD command will trigger normal STD power off sequence. 1: Enable. STD command triggers a system reset but not STD power off.
7:3	RO	0	**Reserved**
2	WO	0	**Global Release** This bit is set by ACPI software to indicate the release of the SCI / SMI lock. Upon setting of this bit, the hardware automatically sets the BIOS Status bit (PMIO Rx28[5]). This bit is cleared by hardware when the BIOS Status bit is cleared by software. Note that setting on this bit will cause an SMI to be generated if the BIOS Enable bit (PMIO Rx2A[5]) is set.
1	RW	0	**Bus Master Reload** This bit controls whether bus master request (PMIO Rx0[4]) resumes the processor from C3/C4 to C0 state. 0: Bus master requests are ignored by power management logic 1: Bus master requests resume the processor from the C3/C4 state to the C0 state
0	RW	0	**SCI / SMI Select** This bit controls either SCI or SMI is generated for power management events triggered by the Power Button, Sleep Button and RTC (when PMIO Rx0 bits 8, 9, or 10 equal one). 0: SMI 1: SCI Note that certain power management events can be programmed to select either SCI or SMI interrupt independently of the setting of this bit (refer to the General Purpose SCI Enable and General Purpose SMI Enable registers at PMIO Rx22 and 24). Also, Timer Status & Global Status always generate SCI and BIOS Status always generates SMI.

Offset Address: 0B-08h (PMIO)

ACPI Timer **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Extended Timer Value** This field reads back 0 if the 24-bit timer option is selected (D17F0 Rx81[3]).
23:0	RO	0	**Timer Value** This read-only field returns the running count of the power management timer. This is a 24/32-bit counter that runs off a 3.579545 MHz clock, and counts while in the S0 (working) system state. The timer is reset to an initial value of zero during system reset, and then continues counting until the 14.31818 MHz input clock of the chip is stopped. If the clock is restarted without a reset, the counter will continue counting from where it was stopped.

Processor Power Management Registers (PMIO 10-16h)

Offset Address: 13-10h (PMIO)

Processor Control **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:5	RO	0	**Reserved**
4	RW	0	**Throttling Enable** Setting this bit starts clock throttling (modulating the STPCLK# signal) regardless of the CPU state. Its duty cycle is determined by bits 3-0 of this register.
3:0	RW	0	**Throttling Duty Cycle**

Offset Address: 14h (PMIO)

Processor Level 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Processor Level 2**

Offset Address: 15h (PMIO)

Processor Level 3 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Processor Level 3**

Offset Address: 16h (PMIO)

Processor Level 4 **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Processor Level 4**

General Purpose Power Management Registers (PMIO 20-52h)

Offset Address: 21-20h (PMIO)

General Purpose Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**North Module SERR# Status**
14	RW1C	0	**USB Wake-Up in Suspend** For suspend states: STR / STD / Soft off.
13	RW1C	0	**HDAC Wake-Up Status** Can be set only in suspend mode.
12	RW1C	0	**Battery Low Status** Set when the BATLOW# input is asserted low.
11	RW1C	0	**LID# Status** Set when the edge changes as selected by PMIO Rx2C bit7 on the LID# input is detected.
10	RW1C	0	**Thermal Detect Status** Set when the edge changes as selected by PMIO Rx2C bit6 on the THRM# input is detected.
9	RW1C	0	**Mouse Controller PME Status**
8	RW1C	0	**RING# Status** Set when the RING# input is asserted low.
7	RW1C	0	**GP3 Timer Time Out Status**
6	RW1C	0	**INTRUDER# Status** Set when the INTRUDER# pin is asserted low.
5	RW1C	0	**PME# Status** Set when the PME# pin is asserted low.
4	RW1C	0	**EXTSMI# Status** Set when the EXTSMI# pin is asserted low.
3	RO	0	**Reserved**
2	RW1C	0	**Internal KBC (Keyboard Controller) PME Status** Set when the internal KBC PME signal is asserted.
1	RW1C	0	**GPI1 Status** Set when the GPI1 pin is asserted low.
0	RW1C	0	**GPI0 Status** Set when the GPI0 pin is asserted low.

Note that the above bit corresponds to the respective bit at the same location of the General Purpose SCI Enable and General Purpose SMI Enable registers at offset address 22h and 24h: an SCI or SMI is generated if the corresponding bit of the General Purpose SCI or SMI Enable registers, respectively, is set to one. The above bits are set by hardware only and can only be cleared by writing a one.

Offset Address: 23-22h (PMIO)

General Purpose SCI / RESUME Enable **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**Enable SCI on North Module SERR Event** 0: Disable 1: Enable
14	RW	0	**Enable SCI on USB Wake-up Event**
13	RW	0	**Enable SCI on HDAC Wake-up Event**
12	RW	0	**Enable SCI on BATLOW# Event**
11	RW	0	**Enable SCI on LID# Event**
10	RW	0	**Enable SCI on THRM# Event**
9	RW	0	**Enable SCI on Mouse PME**
8	RW	0	**Enable SCI on RING# Event**
7	RW	0	**Enable SCI on GP3 Timer Timeout**
6	RW	0	**Enable SCI on INTRUDER# Event**
5	RW	0	**Enable SCI on PME# Assertion**
4	RW	0	**Enable SCI on EXTSMI# Assertion**
3	RO	0	**Reserved**
2	RW	0	**Enable SCI on Internal KBC PME**
1	RW	0	**Enable SCI on GPI1 Assertion**
0	RW	0	**Enable SCI on GPI0 Assertion**

Offset Address: 25-24h (PMIO)

General Purpose SMI / Resume Enable **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW	0	**Enable SMI on North Module SERR Event** 0: Disable 1: Enable
14	RW	0	**Enable SMI on USB Wake-up Event**
13	RW	0	**Enable SMI on HDAC Wake-up Event**
12	RW	0	**Enable SMI on BATLOW# Event**
11	RW	0	**Enable SMI on LID# Event**
10	RW	0	**Enable SMI on THRM# Event**
9	RW	0	**Enable SMI on Mouse PME**
8	RW	0	**Enable SMI on RING# Event**
7	RO	0	**Reserved**
6	RW	0	**Enable SMI on INTRUDER# Event**
5	RW	0	**Enable SMI on PME# Assertion**
4	RW	0	**Enable SMI on EXTSMI# Assertion**
3	RO	0	**Reserved**
2	RWC	0	**Enable SMI on Internal KBC PME**
1	RWC	0	**Enable SMI on GPI1**
0	RWC	0	**Enable SMI on GPI0**

Offset Address: 26h (PMIO)

Processor Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**PCISTP# Assertion while CLKRUN# is De-asserted** 0: Assert PCISTP# 1: Not assert PCISTP# (no stop on PCICLK)
3	RW	0	**PCI CLKRUN# Control** 0: CLKRUN# is always asserted 1: CLKRUN# will be de-activated after the PCI bus is idle for 26 clocks
2	RW	0	**Host Clock Stop (CPUSTP#) Control** This bit controls whether CPUSTP# is asserted in C3/C4 and S1 states. Normally CPUSTP# is not asserted in C3/C4 and S1 states, only STPCLK# is asserted. 0: CPUSTP# will not be asserted in C3/C4 and S1 states (only STPCLK# is asserted) 1: CPUSTP# will be asserted in C3/C4 and S1 states
1	RW	0	**SLP# Assertion in Processor Level 3 Read** This bit controls whether SLP# is asserted in C3 state. 0: SLP# is not asserted in C3 state 1: SLP# is asserted in C3 state
0	RW	0	**Lower CPU Voltage (Activate VRDSLP) During C3 / S1** This bit controls whether the CPU voltage is lowered in C3/S1 state. The CPU voltage is lowered using the VRDSLP signal to the voltage regulator. To activate this control bit, bits 2 and 1 of this register must be set to 1. 0: Disable (normal voltage during C3/S1) 1: Enable (lower voltage during C3/S1) **Notes:** 1. To enter C4 state in C3 command read, register bit[2:0] must be set. 2. Reading LVL4 (PMIO Rx16) has the same effect as reading LVL3 with bit[2:0] are set to1. 3. VRDSLP will be activated either in C3 with this control bit set or LVL4 register is read.

Note: PMIO Rx26[4:0] can be written by PMIO Rx64[4].

Offset Address: 29-28h (PMIO)

Global Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RW1C	0	**GPIO Range 1 Access Status**
14	RW1C	0	**GPIO Range 0 Access Status**
13	RW1C	0	**GP3 Timer Time Out Status**
12	RW1C	0	**GP2 Timer Time Out Status**
11	RW1C	0	**SERIRQ SMI Status**
10	RW1C	0	**PMIO Rx5[5] (Sleep Enable) Write Status** This bit reports whether PMIO Rx5[5] has been write-accessed. If PMIO Rx2B[3] is set to enable SMI, an SMI in generated when this bit is 1.
9	RW1C	0	**THRMTRIP# Activity Status**
8	RW1C	0	**CLKRUN# Resume Status** This bit is set when PCI bus peripherals asserting CLKRUN#
7	RW1C	0	**Primary IRQ/INIT/NMI/SMI Resume Status** This bit is set at the occurrence of primary IRQs as defined in Rx85-84 of PCI configuration space
6	RW1C	0	**Software SMI Status** This bit is set when the SMI Command port (PMIO Rx2F) is write-accessed.
5	RW1C	0	**BIOS Status** This bit is set when the Global Release bit is set to one (typically by the ACPI software to release control of the SCI/SMI lock). When this bit is reset (by writing a one) the Global Release bit is reset at the same time by hardware.
4	RW1C	0	**Legacy USB Status** This bit is set when a legacy USB event occurs. This is normally used for USB keyboards.
3	RW1C	0	**GP1 Timer Time Out Status** This bit is set when the GP1 timer times out.
2	RW1C	0	**GP0 Timer Time Out Status** This bit is set when the GP0 timer times out.
1	RW1C	0	**Secondary Event Timer Time Out Status** This bit is set when the secondary event timer times out.
0	RO	0	**Primary Activity Status** This bit can be cleared by writing 1 to clear APIC PMIO Rx30-33

Notes:

1. SMI can be generated when any of the above bits is set if the corresponding control bit is enabled (see the Rx2A Global Enable register bit descriptions).
2. The above status bits are set by hardware and can only be cleared by writing a one to the desired bit position.
3. The above status bits, when set, will trigger assertion of SMI.

Offset Address: 2B-2Ah (PMIO)

Global Enable **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RW	0	**SMI Enable on GPIO Range 1 Access** 0: Disable 1: Enable
14	RW	0	**SMI Enable on GPIO Range 0 Access**
13	RW	0	**SMI Enable on GP3 Timer Timeout**
12	RW	0	**SMI Enable on GP2 Timer Timeout**
11	RW	0	**SMI Enable on SERIRQ SMI**
10	RW	0	**SMI Enable on Rx5[5] Write**
9	RW	1b	**THRMTRIP# Activity Power Off Enable**
8	RW	0	**CLKRUN# Resume Enable** This bit may be set to trigger an SMI assertion when the CLKRUN# Resume Status bit is set.
7	RW	0	**Primary IRQ/INIT/NMI/SMI Resume Enable in POS State** This bit may be set to trigger an SMI assertion when the Primary IRQ / INIT / NMI / SMI Resume Status bit is set.
6	RW	0	**SMI Enable on Software SMI** This bit may be set to trigger an SMI assertion when the Software SMI Status bit is set.
5	RW	0	**SMI Enable on BIOS** This bit may be set to trigger an SMI assertion when the BIOS Status bit is set.
4	RW	0	**SMI Enable on Legacy USB** This bit may be set to trigger an SMI assertion when the Legacy USB Status bit is set.
3	RW	0	**SMI Enable on GP1 Timer Timeout** This bit may be set to trigger an SMI assertion when the GP1 Timer Timeout Status bit is set.
2	RW	0	**SMI Enable on GP0 Timer Timeout** This bit may be set to trigger an SMI assertion when the GP0 Timer Timeout Status bit is set.
1	RW	0	**SMI Enable on Secondary Event Timeout** This bit may be set to trigger an SMI assertion when the Secondary Event Timer Timeout Status bit is set.
0	RW	0	**SMI Enable on Primary Activity** This bit may be set to trigger an SMI assertion when the Primary Activity Status bit is set.

Offset Address: 2D-2Ch (PMIO)

Global Control **Default Value: 0010h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**IDE Bus Power-Off** 0: Disable 1: Enable
9	RO	0	**Reserved**
8	RW1C	0	**SMI Active Status** 0: SMI inactive 1: SMI active. If the SMI Lock bit is set, this bit must be written 1 to clear it before the next SMI can be generated.
7	RW	0	**LID# Triggering Polarity** 0: Rising edge 1: Falling edge
6	RW	0	**THRM# Triggering Polarity** 0: Rising edge 1: Falling edge
5	RW	0	**Disable Battery Low Resume** 0: Enable resume 1: Disable resume from suspend when BATLOW# is asserted.
4	RO	1b	**Reserved** (Do not program)
3	RO	0	**Reserved**
2	RW	0	**Power Button Triggering Polarity** 0: Rising edge 1: Falling edge Set to zero to avoid the situation where the Power Button Status bit is set to wake up the system then reset again by 4's-Override status to switch the system into the soft-off state.
1	RW	0	**BIOS Release** This bit is set by legacy software to indicate release of the SCI/SMI lock. Upon setting of this bit, hardware automatically sets the Global Status bit. This bit is cleared by hardware when the Global Status bit cleared by software. Note that if the Global Enable bit is set (Power Management Enable register Rx2[5]), then setting this bit causes an SCI or SMI to be generated (since setting on this bit causes the Global Status bit to be set).
0	RW	0	**SMI Enable** 0: Disable all SMI generation 1: Enable SMI generation

Offset Address: 2Fh (PMIO)

Software SMI Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SMI Command** Writing to this port triggers SMI assertion.

Offset Address: 33-30h (PMIO)

Primary Activity Detect Status **Default Value: 0000 0000h**

The Primary Activity Detect Status bits have one-to-one correspondence to the Primary Activity Detect Enable bits in Rx37-34. If the corresponding bit is set in the Enable register, setting of a bit in the Status register will cause the Primary Activity Status (PMIO Rx28[0]) bit to be set. Bit in this register default to be 0, is set by hardware only and it could only be cleared by writing 1 to the desired bit.

Bit	Attribute	Default	Description
31:11	RO	0	**Reserved**
10	RW1C	0	**Audio Status** Set if Audio is accessed.
9	RW1C	0	**Keyboard Controller Access Status** Set if the KBC is accessed via I/O port 60h.
8	RW1C	0	**VGA Access Status** Set if the VGA port is accessed via I/O ports 3B0-3DFh or memory space A0000-BFFFFh.
7	RW1C	0	**LPT Port Status** Set if the parallel port is accessed via I/O ports 278-27Fh or 378-37Fh (LPT2 or LPT1).
6	RW1C	0	**Serial Port B Access Status** Set if the serial port is accessed via I/O ports 2F8-2FFh or 2E8-2EFh (COM2 and COM4 respectively).
5	RW1C	0	**Serial Port A Access Status** Set if the serial port is accessed via I/O ports 3F8-3FFh or 3E8-3EFh (COM1 and COM3, respectively).
4	RW1C	0	**Floppy Access Status** Set if the floppy controller is accessed via I/O ports 3F0-3F5h or 3F7h.
3	RW1C	0	**IDE Access Status** Set if the EIDE controller is accessed via I/O ports 170-177h or 376h.
2	RW1C	0	**SATA Access Status** Set if the SATA controller is accessed via I/O ports 1F0-1F7h or 3F6h.
1	RW1C	0	**Primary Interrupt Activity Status** Set on the occurrence of a primary interrupt (enabled via the register at D17F0 PCI configuration Rx84h.).
0	RW1C	0	**PCI Master Access Status** Set on the occurrence of PCI master activity.

Notes:

1. Setting of Primary Activity Status may be done to enable a "Primary Activity Event": an SMI will be generated if the Primary Activity Enable bit (PMIO Rx2A[0]) is set and/or the GP0 timer will be reloaded if the "GP0 Timer Reload on Primary Activity" bit (PMIO Rx38[0]) is set.
2. Bits 2-9 above also correspond to bits of GP Timer Reload Enable register Rx38: If bits are set in that register, setting a corresponding bit in this register will cause the GP1 timer to be reloaded.

Offset Address: 37-34h (PMIO)

Primary Activity Detect Enable

Default Value: 0000 0000h

The Primary Activity Detect Enable bits have one-to-one correspondence to the Primary Activity Detect Status bits in Rx33-30. Setting of any of Status bits also sets the Primary Activity Status (PMIO Rx28[0]) bit which causes the GP0 timer to be reloaded (if the Primary Activity GP0 Enable bit is set) or generates an SMI (if Primary Activity Enable is set).

Bit	Attribute	Default	Description
31:11	RO	0	**Reserved**
10	RW	0	**SMI on Audio Status** 0: Do not set PMIO Rx28[0] if PMIO Rx30[10] is set. 1: Set PMIO Rx28[0] if PMIO Rx30[10] is set.
9	RW	0	**SMI on Keyboard Controller Status** 0: Do not set PMIO Rx28[0] if PMIO Rx30[9] is set. 1: Set PMIO Rx28[0] if PMIO Rx30[9] is set.
8	RW	0	**SMI on VGA Status** 0: Do not set PMIO Rx28[0] if PMIO Rx30[8] is set. 1: Set PMIO Rx28[0] if PMIO Rx30[8] is set.
7	RW	0	**SMI on LPT Status**
6	RW	0	**SMI on Serial Port B Status** 0: Do not set PMIO Rx28[0] if PMIO Rx30[6] is set. 1: Set PMIO Rx28[0] if PMIO Rx30[6] is set.
5	RW	0	**SMI on Serial Port A Status** 0: Do not set PMIO Rx28[0] if PMIO Rx30[5] is set. 1: Set PMIO Rx28[0] if PMIO Rx30[5] is set.
4	RW	0	**SMI on Floppy Status** 0: Do not set PMIO Rx28[0] if PMIO Rx30[4] is set. 1: Set PMIO Rx28[0] if PMIO Rx30[4] is set.
3	RW	0	**SMI on IDE Status** 0: Do not set PMIO Rx28[0] if PMIO Rx30[3] is set. 1: Set PMIO Rx28[0] if PMIO Rx30[3] is set.
2	RW	0	**SMI on SATA Status** 0: Do not set PMIO Rx28[0] if PMIO Rx30[2] is set. 1: Set PMIO Rx28[0] if PMIO Rx30[2] is set.
1	RW	0	**SMI on Primary IRQ Status** 0: Do not set PMIO Rx28[0] if Rx30[1] is set. 1: Set PMIO Rx28[0] if Rx30[1] is set.
0	RW	0	**SMI on PCI Master Status** 0: Do not set PMIO Rx28[0] if PMIO Rx30[0] is set. 1: Set PMIO Rx28[0] if PMIO Rx30[0] is set.

Offset Address: 38h (PMIO)

GP Timer Reload Enable **Default Value: 00h**

All bits in this register default to 0 on power up.

Bit	Attribute	Default	Description
7	RW	0	**GP1 Timer Reload on KBC Access** 0: Normal GP1 Timer Operation 1: Setting of PMIO Rx30[9] causes the GP1 timer to reload.
6	RW	0	**GP1 Timer Reload on Serial Port Access** 0: Normal GP1 Timer Operation 1: Setting of PMIO Rx30[5] or Rx30[6] causes the GP1 timer to reload.
5	RO	0	**Reserved**
4	RW	0	**GP1 Timer Reload on VGA Access** 0: Normal GP1 Timer Operation 1: Setting of VGA_STS causes the GP1 timer to reload.
3	RW	0	**GP1 Timer Reload on Drive Access** 0: Normal GP1 Timer Operation 1: Setting of PMIO Rx30[4:2] causes the GP1 timer to reload.
2	RW	0	**GP3 Timer Reload on GPIO Range 1 Access** 0: Normal GP3 Timer Operation 1: Setting of Rx28[15] causes the GP3 timer to reload.
1	RW	0	**GP2 Timer Reload on GPIO Range 0 Access** 0: Normal GP2 Timer Operation 1: Setting of Rx28[14] causes the GP2 timer to reload.
0	RW	0	**GP0 Timer Reload on Primary Activity** 0: Normal GP0 Timer Operation 1: Setting of PMIO Rx28[0] causes the GP0 timer to reload. Primary activities are enabled via the Primary Activity Detect Enable register (PMIO Rx37-34) with status recorded in the Primary Activity Detect Status register (PMIO Rx33-30).

Offset Address: 39h (PMIO)

General Purpose Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW1C	0	**ASF Wake-up Status**

Offset Address: 3Ah (PMIO)

General Purpose SCI Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**SCI Enable on ASF Wake**

Offset Address: 3Bh (PMIO)

General Purpose SMI Enable **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**SMI Enable on ASF Wake**

Offset Address: 40h (PMIO)
Extend SMI/IO Trap Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW1C	0	**BIOS Write Access Status**
3	RW1C	0	**GP3 Timer Second Timeout With No Cycles** 0: No cycles occurred in between GP3 timer 2nd time out and reset assertion. 1: One or more cycles occurred in between GP3 timer 2nd time out and reset assertion.
2	RW1C	0	**GP3 Timer Second Timeout Status** Set to 1 when GP3 timer has two consecutive timeouts.
1	RW1C	0	**GPIO Range 3 Access Status**
0	RW1C	0	**GPIO Range 2 Access Status**

Offset Address: 42h (PMIO)
Extend SMI/IO Trap Enable **Default Value: 04h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**SMI on BIOS Write Access** This bit controls whether SMI is asserted when BIOS Write Access Status PMIO Rx40[4] is set. 0: Disable 1: Enable (can be reset only through PCI Reset)
3	RW	0	**Override GP3 Timer Second Timeout Reboot** 0: No override. GP3 timer second timeout resets the system only when bit 2 is set and AZSDOUT is strapped to enable auto reboot. 1: Enable GP3 timer second timeout reset anyway (override bit 2 and strapping)
2	RW	1b	**GP3 Timer Second Timeout Reboot** This bit controls whether the system is rebooted when the GP3 timer times out twice (PMIO Rx40[2] = 1). 0: Disable 1: Enable
1	RW	0	**SMI on GPIO Range 3 Access** This bit controls whether SMI is generated when PMIO Rx40[1]=1 0: Disable 1: Enable
0	RW	0	**SMI on GPIO Range 2 Access** This bit controls whether SMI is generated when PMIO Rx40[0]=1. 0: Disable 1: Enable

Offset Address: 45-44h (PMIO)
EXTSMI and Miscellaneous Input Value **Default Value: 0000h**

Bit	Attribute	Default	Description
15:13	RO	0	**Reserved**
12	RO	0	**Latest PCS (PCS0-PCS3) IOR/IOW Status** 0: IOR 1: IOW
11	RO	0	**FM SMI or Serial SMI Status**
10	RO	0	**Reserved**
9	RO	0	**SMBus IRQ Status**
8	RO	0	**SMBus Resume Status**
7:0	RO	0	**Reserved**

Offset Address: 4B-48h (PMIO)

General Purpose Input Status **Default Value: —**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:0	RO	—	**General Purpose Input** Bit 0: GPI0 Bit 1: GPI1 Bit 2: GPI2 Bit 3: GPI3 Bit 4: GPI4 Bit 5: GPI5 Bit 6: GPI6 Bit 7: GPI7 Bit 8: GPI8 Bit 9: GPI9 Bit 10: GPIO0 Bit 11: GPIO1 Bit 12: GPIO2 Bit 13: GPIO3 Bit 14: GPIO4 Bit 15: GPIO5 Bit 16: GPIO6 Bit 17: GPIO7 Bit 18: GPIO8 Bit 19: GPIO9 Bit 20: GPIO10 Bit 21: GPIO11 Bit 22: GPIO12 Bit 23: GPIO13

Offset Address: 4F-4Ch (PMIO)

General Purpose Output **Default Value: FFFF FFFFh**

Reads from this register return the last value written (held on chip). Some GPIO pins can be used as both input and output, the output type of these pins is OD (open drain) so to use one of these pins as an input pin, a one must be written to the corresponding bit of this register.

Bit	Attribute	Default	Description
31:25	RO	7Fh	**Reserved**
24:0	RW	1FF FFFFh	**General Purpose Output** Bit 0: GPO0 Bit 1: GPO1 Bit 2: GPO2 Bit 3: GPO3 Bit 4: GPO4 Bit 5: GPO5 Bit 6: GPO6 Bit 7: GPO7 Bit 8: GPO8 Bit 9: GPO9 Bit 10: GPO10 Bit 11: GPIO0 Bit 12: GPIO1 Bit 13: GPIO2 Bit 14: GPIO3 Bit 15: GPIO4 Bit 16: GPIO5 Bit 17: GPIO6 Bit 18: GPIO7 Bit 19: GPIO8 Bit 20: GPIO9 Bit 21: GPIO10 Bit 22: GPIO11 Bit 23: GPIO12 Bit 24: GPIO13

Offset Address: 50h (PMIO)

GPI Change Status **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW1C	0	**Pin Change Status** Bit 0: PEPMESGPI2 Bit 1: PEHPSGPI3 Bit 2: GPIO0 Bit 3: GPIO1 Bit 4: GPIO10 Bit 5: GPIO11 Bit 6: GPIO12 Bit 7: GPIO13 Notes for PEPMESGPI2 and PEHPSGPI3: Please refer to RxE0[1:0], RxE1[1:0] and RxE2[2:1] for related setting

Note:

1. PEPMESGPI2: When RxE2[1] = 1, PEPMESGPI2 is decided by PCIe PM_PME message from North Module.
   When RxE2[1] = 0, PEPMESGPI2 is decided by GPI2
2. PEHPSGPI3: When RxE2[2] = 1, PEHPSGPI3 is decided by PCIe HOTPLUG message from North Module.
   When RxE2[2] = 0, PEHPSGPI3 is decided by GPI1

Offset Address: 52h (PMIO)

GPIO SCI / SMI Generation **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**GPIO SCI / SMI Generation** Bit 0: PEPMESGPI2 Bit 1: PEHPSGPI3 Bit 2: GPIO0 Bit 3: GPIO1 Bit 4: GPIO10 Bit 5: GPIO11 Bit 6: GPIO12 Bit 7: GPIO13 0: Disable 1: Enable

IO Trap Registers (PMIO 54-69h)

Offset Address: 57-54h (PMIO)

I/O Trap PCI Data **Default Value: —**

Bit	Attribute	Default	Description
31:0	RO	—	**PCI Data During I/O Trap SMI**

Offset Address: 59-58h (PMIO)

I/O Trap PCI I/O Address **Default Value: —**

Bit	Attribute	Default	Description
15:0	RO	—	**PCI Address During I/O Trap SMI**

Offset Address: 5Ah (PMIO)

I/O Trap PCI Command / Byte Enable **Default Value: —**

Bit	Attribute	Default	Description
7:4	RO	—	**PCI Command Type During I/O Trap SMI**
3:0	RO	—	**PCI Byte Enable During I/O Trap SMI**

Offset Address: 5Ch (PMIO)

CPU FSB Frequency **Default Value: 00h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**CPU Frequency Select** 0: Normal 1: Low

Offset Address: 5Dh (PMIO)

Scratch Register **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Scratch Register**

Offset Address: 60h (PMIO)

C4P State Event Enable **Default Value: 00h**

All bits in this register default to 0 on power up.

Bit	Attribute	Default	Description
7	RW	0	**Enable to Support PLL Off State during C4 State** If this bit is set to 1, the bus master monitor timer is enabled. 0: Disable 1: Enable
6	RW	0	**Enable to Support PLL Off during C3 State** If this bit is set to 1, the bus master monitor timer is enabled. 0: Disable 1: Enable
5:4	RW	00b	**Bus Master Idle Timer Tick** 00: 0.125KHz (the max time out = 2 sec) 01: 0.5KHz (the max time out = 512 ms) 10: 1KHz (the max time out = 256 ms) 11: 32KHz (the max time out = 7 ms)
3	RW	0	**Enable Mouse Interrupt to Wake Up C4P State** 0: Disable 1: Enable
2	RW	0	**C4PSTP# Output to the Clock Generator** 0: Disable 1: Enable
1	RW	0	**C4 PLL Wake Up Events Combines with All Interrupt Requests** 0: Disable 1: Enable
0	RW	0	**PLL Power Off / Gating during C4P State** 0: PLL gating during C4P state 1: PLL turn off during C4P state

Offset Address: 61h (PMIO)

C4P State Bus Master Idle Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Current Count Value of the Bus Master Idle Timer** If this timer is not time out, a C4P state is inhibitive.

Offset Address: 62h (PMIO)

C4P State Bus Master Idle Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Initial Value of the Bus Master Idle Timer** Refer to PMIO Rx60[5:4] for detail of the time unit.

Offset Address: 63h (PMIO)

C4P State H2R Timer Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Initial Value of Resume Time Out Using 4KHz Clock**

Offset Address: 64h (PMIO)

C4P State SATA and USB Related Enable **Default Value: 00h**

All bits in this register default to 0 on power up.

Bit	Attribute	Default	Description
7	RW	0	**Turn Off USB PHY 120MHz PLL** 0: Disable 1: Enable
6	RW	0	**USB Wake Up Event for C4P State** 0: Disable 1: Enable
5	RW	0	**Enable SATA Master Reset Bus Master Idle Timer** 0: Ignore SATA master reset bus master idle timer. 1: Enable bus master idle timer reset signal. Note: If SATA is not used, this bit and bit 3 can be set to 0
4	RW	0	**PMIO Rx26[4:0] Write Protection Enable Register** 0: PMIO Rx26[4:0] can be written normally. 1: PMIO Rx26[4:0] can not be written.
3	RW	0	**PMU Request to SATA to Enter C4P State and Wait for SATA Slumber Mode Acknowledge Signal** 0: Disable 1: Enable
2	RW	0	**SATA PHY 150MHz Clock Gating** 0: Disable 1: Enable
1	RW	0	**Turn Off SATA PHY 150MHz PLL** 0: Disable 1: Enable
0	RW	0	**SATA C4 PLL Wake Up Event from C4P State** 0: Disable 1: Enable

Offset Address: 65h (PMIO)

C4P State USB and NM Related Enable **Default Value: 00h**

All bits in this register default to 0 on power up.

Bit	Attribute	Default	Description
7	RW	0	**NM PLL Gating** 0: Disable 1: Enable
6	RW	0	**Turn Off NM PLL** 0: Disable 1: Enable
5	RW	0	**NM Wake Up Event for C4P State** 0: Disable 1: Enable
4	RW	0	**APIC Interrupt Wake Up System from C4P State** 0: Disable 1: Enable
3	RW	0	**Enable USB Controller Master Reset Bus Master Idle Timer** 0: Ignore USB controller master reset bus master idle timer. 1: Enable bus master idle timer reset signal.
2	RW	0	**Enable Keyboard Interrupt to Wake Up C4P State** 0: Disable 1: Enable
1	RW	0	**PMU Request to USB to Enter C4P State And Wait for USB D3 Mode Acknowledge Signal** 0: Disable 1: Enable
0	RW	0	**Enable USB PHY 120MHz PLL Gating** 0: Disable 1: Enable

Offset Address: 66h (PMIO)

C4P State NM and HDAC Related Enable **Default Value: 00h**

All bits in this register default to 0 on power up.

Bit	Attribute	Default	Description
7	RW	0	**Enable HDAC Master Reset Bus Master Idle Timer** 0: Ignore HDAC master reset bus master idle time. 1: Enable bus master idle timer reset signal.
6	RO	0	**Reserved**
5	RW	0	**HD Wakeup Event for C4P State** 0: Disable 1: Enable
4	RW	0	**Enable PCI REQ# as a C4 PME Event** 0: Disable 1: Enable Note: If PCICLK keeps running (disable CLKRUN# or PCISTP#) during C4P state, this bit must be set to make PCI REQ# be a C4 PME event.
3	RW	0	**Turn Off PCICLK Driven from the Clock Generator** 0: Disable 1: Enable
2	RW	0	**Enable NM Master Reset Bus Master Idle Timer** 0: Ignore NM master reset bus master idle timer. 1: Enable bus master idle timer reset signal.
1	RW	0	**Select Signal to Indicate STPGNT Special Cycle** 0: SM will notify NM of getting into power management C2 state from C0 state when SM observes stop-grant from NM. 1: SM will notify NM of getting into power management C2 state from C0 state when SM observes stop-grant from NM and host side (P6IF) has no pending cycle.
0	RW	0	**PMU Request to USB to Enter C4P State And Wait for NM D3 Mode Acknowledge Signal** 0: Disable 1: Enable

Offset Address: 67h (PMIO)

C4P State IDE Related Enable **Default Value: 00h**

All bits in this register default to 0 on power up.

Bit	Attribute	Default	Description
7	RW	0	**Enable C4P State Back to C2** 0: Disable 1: Enable
6	RO	0	**Reserved**
5	RW	0	**Enable C4P State Wakeup for Resume Timer Out** 0: Disable 1: Enable
4	RW	0	**Enable PIC Wakeup Event in C4P State** 0: Disable 1: Enable
3	RW	0	**Enable UART Wakeup Event in C4P State** 0: Disable 1: Enable
2	RW	0	**Enable IDE Master Reset Bus Master Idle Timer** 0: Ignore IDE master reset bus master idle timer. 1: Enable bus master idle timer reset signal.
1	RO	0	**Reserved**
0	RW	0	**IDE Wake Up Event for C4P State** 0: Disable 1: Enable

Offset Address: 68h (PMIO)

C4P State Other Devices Related Enable **Default Value: 00h**

All bits in this register default to 0 on power up.

Bit	Attribute	Default	Description
7	RW	0	**Enable PCI Master Reset Bus Master Idle Timer** 0: Disable 1: Enable
6	RW1C	0	**PWRGD Status** This bit records PWRGD signal state change. 0: The PWRGD signal state remains no change since last clear to 0. It indicates that no core power lost since then. 1: The PWRGD signal state has been toggled since last clear to 0 or power up. It indicates that the last system reset is due to core power lost. When 1, this register bit can be cleared to 0 by "Write 1" to it.
5	RW	0	**Enable CR (Card Reader) Master Reset Bus Mater Idle Timer** 0: Disable 1: Enable
4	RO	0	**Reserved**
3	RW	0	**Card Reader Wake Up Event for C4P State** 0: Disable 1: Enable
2	RW	0	**Enable SDIO Master Reset Bus Mater Idle Timer** 0: Ignore SDIO master reset bus master idle timer. 1: Enable bus master idle timer reset signal.
1	RO	0	**Reserved**
0	RW	0	**SDIO Wake Up Event for C4P State** 0: Disable 1: Enable

Offset Address: 69h (PMIO)

Clock Generator Resume Timer Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3:0	RW	0	**Initial Value of Clock Generator Resume Timer**

Watchdog Timer Memory Base (PM-MMIO 00-07h)

The memory base address for these registers is defined in RxEB-E8h of the D17F0 PCI configuration registers.

Offset Address: 03-00h (PM-MMIO)

Watchdog Control / Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:8	RO	0	**Reserved**
7	WO	0	**Watchdog Trigger** Setting this bit triggers the watchdog to start a new count interval, counting down from the value that was last written to the Watchdog Count Register. This bit is always read as zero. Setting this bit has no effect if the watchdog is disabled or stopped.
6:4	RO	0	**Reserved**
3	RO	0	**Disable Watchdog** This bit reflects the state of the watchdog timer hardware. 0: Enable 1: Disable
2	RW	0	**Watchdog Action** This bit determines the action to be taken when the watchdog timer expires. 0: System reset 1: System power off The bit is only valid when the watchdog is enabled.
1	RW1C	0	**Watchdog Fired** When set, the watchdog timer expired and caused the current restart. The bit is cleared by writing a 1 to bit 1 in the Watchdog Control register. Writing a 0 has no effect. The bit is cleared by a power cycle or by the operating system and it must remain cleared for any restart that is not caused by the watchdog timer firing. The bit is only valid when the watchdog is enabled.
0	RW	0	**Watchdog Enable** This bit is used to control or indicate whether the watchdog is in the Enabled\Running and Enabled\Stopped states. 1: Watchdog is in the Enabled\Running state 0: Watchdog is in the Enabled\Stopped state If the watchdog is in the Enabled\Stopped state and a 1 is written to bit 0, the watchdog moves to the running state but a count interval is not started until a 1 is written to bit 7.If the watchdog is in the Enabled\Running state, writing a 1 to bit 0 has no effect. The bit is only valid when the watchdog is enabled.

Offset Address: 07-04h (PM-MMIO)

Watchdog Count **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:10	RO	0	**Reserved**
9:0	WO	0	**Count Register** This defines the countdown time for the counter. A value of zero is reserved. Reading this register results in the current counter value. Writing to the register has no effect until a one is written to the watchdog trigger bit of the Watchdog Control/Status Register. These bits are only valid when the watchdog is enabled.

System Management Bus I/O Space Registers (SMIO 00-0Fh)

The base address for these registers is defined in RxD1-D0 of the D17F0 PCI configuration registers. The System Management Bus I/O space is enabled for access by the system if D17F0 RxD2[0] = 1.

Offset Address: 00h (SMIO)

SMBus Host Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**SMB Host PEC Error** 0: SMBus Host PEC calculation is correct. 1: SMBus Host PEC calculation is error. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
6	RW1C	0	**SMB Semaphore** This bit is used as a semaphore among various independent software threads that may need to use the Host SMBus logic and it has no effect on hardware. After reset, this bit reads 0. Write 1 to this bit causes the next read to return 0, all reads after that return 1. Write 0 to this bit has no effect. Software can therefore write 1 to request control and if readback is 0 then it will own usage of the host controller.
5	RO	0	**Reserved**
4	RW1C	0	**Failed Bus Transaction** 0: SMBus interrupt is not caused by failed bus transaction 1: SMBus interrupt is caused by failed bus transaction. This bit may be set when the SMIO Rx2[1] is set and can be cleared by write 1 to this bit position.
3	RW1C	0	**Bus Collision** 0: SMBus interrupt is not caused by transaction collision 1: SMBus interrupt is caused by transaction collision. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
2	RW1C	0	**Device Error** 0: SMBus interrupt is not caused by SMBus transaction error 1: SMBus interrupt is caused by SMBus transaction error (illegal command field, unclaimed host-initiated cycle, or host device timeout). This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
1	RW1C	0	**SMBus Interrupt** 0: SMBus interrupt is not caused by host command completion 1: SMBus interrupt is caused by host command completion. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
0	RO	0	**Host Busy** 0: SMBus controller host interface is not processing a command 1: SMBus host controller is busy in processing a command. None of the other SMBus registers should be accessed if this bit is set.

Offset Address: 01h (SMIO)

SMBus Slave Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW1C	0	**SMB GPIO Slave PEC Error** 0: SMBus GPIO slave PEC calculation is correct. 1: SMBus GPIO slave PEC calculation is error. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
6	RW1C	0	**SMB Host Slave PEC Error** 0: SMBus Host Slave PEC calculation is correct. 1: SMBus Host Slave PEC calculation is error. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
5	RW1C	0	**Alert Status** 0: SMBus interrupt is not caused by SMBALRT# signal. 1: SMBus interrupt is caused by SMBALRT# signal. This bit will be set only if the Alert Enable bit in SMIO Rx8[3] is set. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
4	RW1C	0	**Shadow 2 Status** 0: SMBus interrupt is not caused by address match to SMBus Slave Address Port 2 1: SMBus interrupt / resume event is caused by slave cycle address match to SMBus Shadow Address Port 2. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
3	RW1C	0	**Shadow 1 Status** 0: SMBus interrupt is not caused by address match to SMBus Slave Address Port 1 1: SMBus interrupt / resume event is caused by slave cycle address match to SMBus Shadow Address Port 1. This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
2	RW1C	0	**Slave Status** 0: SMBus interrupt is not caused by slave event match. 1: SMBus interrupt / resume event is caused by slave cycle event match of the SMBus Slave Command Register at SMIO RxD3 (command match) and the SMBus Slave Event Register at SMIO Rx0A (data event match). This bit is only set by hardware and can be cleared by writing a 1 to this bit position.
1	RO	0	**Reserved**
0	RO	0	**Slave Busy** 0: SMBus controller slave interface is not processing data 1: SMBus controller slave interface is busy in receiving data. None of the other SMBus registers should be accessed if this bit is set.

Offset Address: 02h (SMIO)
SMBus Host Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PEC Enable** 0: Disable 1: Enable SMBus Host to support PEC calculation.
6	RW	0	**Start** 0: Write 0 has no effect 1: Start Execution of Command Write 1 to this bit causes the SMBus controller host interface to initiate execution of the command in the SMBus Command Protocol field (bits 5-2). All necessary registers should be programmed prior to writing 1 to this bit. The Host Busy bit SMIO Rx0[0] can be used to identify when the SMBus controller has completed command execution.
5:2	RW	0	**SMBus Command Protocol** Selects the command type the SMBus host controller will execute. Reads or Writes are determined by Rx4[0]. **Protocol** 0000: Quick 0001: Byte 0010: Byte Data 0011: Word Data 0100: Process Call 0101: Block 0110: I2C with 10-bit Address 0111: Reserved 10xx: Reserved 1100: I2C Process Call 1101: I2C Block 1110: I2C with 7-bit Address 1111: Universal
1	RW	0	**Kill Transaction in Progress** 0: Normal host controller operation 1: Stop host transaction currently in progress. Setting this bit also sets the status bit SMIO Rx0[4] and asserts the interrupt selected by the SMB Interrupt Select bit SMIO RxD2[3].
0	RW	0	**Interrupt Enable** 0: Disable interrupt generation. 1: Enable generation of interrupts on completion of the current host transaction.

Offset Address: 03h (SMIO)
SMBus Host Command **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Host Command** This field contains the data transmitted in the command field of the SMBus host transaction.

Offset Address: 04h (SMIO)
SMBus Host Address **Default Value: 00h**

The contents of this register are transmitted in the address field of the SMBus host transaction.

Bit	Attribute	Default	Description
7:1	RW	0	**SMBus Address** This field contains the 7-bit address of the targeted slave device.
0	RW	0	**SMBus Read or Write** 0: Execute a WRITE command 1: Execute a READ command

Offset Address: 05h (SMIO)

SMBus Host Data 0 **Default Value: 00h**

The contents of this register are transmitted in the Data 0 field of SMBus host transaction writes. On reads, Data 0 byte is stored here.

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Data 0** For Block Write commands, this field is programmed with the block transfer count (a value between 1 and 32). Counts of 0 or greater than 32 are undefined. For Block Read commands, the count received from the SMBus device is stored here.

Offset Address: 06h (SMIO)

SMBus Host Data 1 **Default Value: 00h**

The contents of this register are transmitted in the Data 1 field of SMBus host transaction writes. On reads, Data 1 byte is stored here.

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Data 1** This register should be programmed with the value to be transmitted in the Data 1 field of an SMBus host interface transaction

Offset Address: 07h (SMIO)

SMBus Block Data **Default Value: 00h**

Reads and writes to this register are used to access the 32-byte block data storage array. An internal index pointer is used to address the array. It is reset to 0 by reads of the SMIO Rx2 and incremented automatically by each access to this register. The transfer of block data into (read) or out of (write) this storage array during an SMBus transaction always starts at index address 0.

Bit	Attribute	Default	Description
7:0	RW	0	**SMBus Block Data Byte**

Offset Address: 08h (SMIO)

SMBus Slave Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**SMBus GPIO Slave PEC Enable** 0: Disable 1: Enable SMBus GPIO Slave to support PEC calculation.
6	RW	0	**SMBus Host Slave PEC Enable** 0: Disable 1: Enable SMBus Host Slave to support PEC calculation.
5	RW	0	**PEC Abort** 0: Disable 1: Enable SMBus to abort PEC calculation error.
4	RW	0	**SMBus GPIO Slave Enable** 0: Disable 1: Enable the generation of a resume event when an external SMBus master generates a transaction with an address that matches the GPIO Slave Address register (SMIO Rx0F).
3	RW	0	**SMBus Alert Enable** 0: Disable 1: Enable generation of an interrupt or resume event on the assertion of the SMBALRT# signal
2	RW	0	**SMBus Shadow Port 2 Enable** 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 2 register (PCI configuration register: F0RxD5).
1	RW	0	**SMBus Shadow Port 1 Enable** 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus Slave Shadow Port 1 register (PCI configuration register: F0RxD4).
0	RW	0	**SMBus Slave Enable** 0: Disable 1: Enable generation of an interrupt or resume event on external SMBus master generation of a transaction with an address that matches the SMBus host controller slave port of 10h, a command field which matches the SMBus Slave Command register (PCI configuration register: F0RxD3), and a match of one of the corresponding enabled events in the SMBus Slave Event Register (SMIO Rx0A).

Offset Address: 09h (SMIO)

SMBus Shadow Command **Default Value: 00h**

This register is used to store command values for external SMBus master accesses to the host slave and slave shadow ports.

Bit	Attribute	Default	Description
7:0	RO	0	**Shadow Command** This field contains the command value which was received during an external SMBus master access whose address field matched the host slave address (10h) or one of the slave shadow port addresses.

Offset Address: 0B-0Ah (SMIO)

SMBus Slave Event **Default Value: 0000h**

This register is used to enable generation of interrupt or resume events for accesses to the host controller's slave port.

Bit	Attribute	Default	Description
15:0	RW	0	**SMBus Slave Event** This field contains data bits used to compare against incoming data to the SMBus Slave Data Register (SMIO Rx0C). When a bit in this register is set and the corresponding bit in the Slave Data register is also set, an interrupt or resume event will be generated if the command value matches the value in the SMBus Slave Command register and the access was to SMBus host address 10h.

Offset Address: 0D-0Ch (SMIO)

SMBus Slave Data **Default Value: 0000h**

This register is used to store data values for external SMBus master accesses to the shadow ports or the SMBus host controller's slave port.

Bit	Attribute	Default	Description
15:0	RO	0	**SMBus Slave Data** This field contains the data value which was transmitted during an external SMBus master access whose address field matched one of the slave shadow port addresses or the SMBus host controller slave port address of 10h.

Offset Address: 0Eh (SMIO) – Reserved

Offset Address: 0Fh (SMIO)

SMBus GPIO Slave Address **Default Value: 00h**

This register is used to store data values of SMBus GPIO Slave address.

Bit	Attribute	Default	Description
7:1	RW	0	**SMBus GPIO Slave Address** Specifies the address used to match against incoming SMBus addresses for GPIO slave.
0	RO	0	**Reserved**

SPI Controller

SPI controller is connected to the LPC controller. All registers are memory-mapped and the base address are located in D17F0 RxBEh~RxBCh of the LPC controller.

SPI Memory-Mapped Base Address (SPIBAR) = D17F0 RxBEh~RxBCh [23:0] << 8

Offset Address: 01-00h (SPI-MMIO)

SPI Status (SPIS) **Default Value: 0000h**

Bit	Attribute	Default	Description
15	R/WLO (note)	0	**SPI Configuration Lock-Down** 0: No Lock-Down 1: SPI Static Configuration information from Rx50 to Rx6F cannot be overwritten. Once set to 1, this bit can only be cleared through hardware reset.
14:4	RO	0	**Reserved**
3	RW1C	0	**Blocked Access Status** 0: Not blocked 1: Blocked. Hardware sets this bit to 1 when an access is blocked from running on the SPI interface due to one of the protection policies or when any of the programmed cycle registers is written while a programmed access is already in progress. This bit is set for both programmed accesses and direct memory reads that get blocked. Note: This bit remains asserted until cleared by software writing a 1 or hardware reset.
2	RW1C	0	**Cycle Done Status** 0: Not done 1: Completes the SPI Cycle after software sets the Rx02[1] SCGO bit Note: This bit remains asserted until cleared by software writing a 1 or hardware reset. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access. This bit gets set after the Status Register Polling sequence completes after reset deasserts. It is cleared before and during that sequence.
1	RO	0	**SPI Access Grant** 0: Not granted 1: Access granted This bit is set in response to software setting the SPI Access Request bit and completing the Future Pending handshake with the LAN component. This bit is cleared in response to software clearing the SPI Access Request bit. Note: Software uses this bit to know whether the other SPI master will initiate long transactions on the SPI bus or not.
0	RO	0	**SPI Cycle Progress <SCIP>** 0: Cycle not in progress 1: Cycle in progress Hardware sets this bit when software sets the Rx02[1] SCGO bit in the Command register. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Note: Software must only program the next command when this bit is 0.

Note: **R/WLO** means **Read/Write Lock-Once**. A register bit can be written to the non-locked value multiple times, but to the locked value only once. After the locked value has been written, the bit becomes read only.

Offset Address: 03-02h (SPI-MMIO)

SPI Control (SPIC) **Default Value: 4005h**

Bit	Attribute	Default	Description
15	RW	0	**SPI SMI# Enable** 0: Disable 1: Enable The SPI asserts an SMI# request whenever Rx0[2] Cycle Done Status bit is 1.
14	RW	1b	**DATA Cycle** 0: No data is delivered for this cycle. The DBC (Data Byte Count) and data fields themselves are ignored. 1: There is data corresponding to this transaction.
13	RW	0	**SPI Fast Read Enable (FREN)** 0: Disable 1: Enable
12	RW	0	**Port Select** 0: Select port0 (CS0). When AZBITCLK=1, this port connects to SPI ROM. When AZBITCLK=0, this port connects to SPI device. 1: Select port1 (CS1). Connects to SPI device.
11:8	RW	0	**Data Byte Count <DBC>** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid setting is any value from 0 to 15. The number of bytes transferred is the value of this field plus 1.
7	RW	0	**Data Atomic Cycle Sequence** 0: No data atomic cycle sequence 1: When set to 1 along with the SCGO (SPI Cycle Go) assertion, the chip will execute a sequence of data on the SPI interface without allowing the LAN component to arbitrate and interleave cycles.
6:4	RW	0	**Cycle Opcode Pointer** The field selects one of the programmed opcodes in the Opcode Menu and uses it as the SPI command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command.
3	RW	0	**Sequence Prefix Opcode Pointer** 0: Points to the opcode in the ***least*** significant byte of the Prefix Opcodes register 1: Points to the opcode in the ***maximum*** significant byte of the Prefix Opcodes register This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. By making this programmable, this chip supports flash devices that have different opcodes for enabling writes to the data space vs. status register.
2	RW	1b	**Atomic Cycle Sequence** 0: No atomic cycle sequence. 1: When set to 1 along with the SCGO assertion, the chip will execute a sequence of commands on the SPI interface without allowing the LAN component to arbitrate and interleave cycles.
1	RW	0	**SPI Cycle Go <SCGO>** 0: SPI cycle not started 1: Set this bit to 1 to start the SPI cycle defined by the other bits in this register. The SCIP bit (SPI Cycle in Progress, Rx00[0]) gets set through this action. This bit always returns 0 on reads. Note: Writes to this bit while the Cycle In Progress bit is set are ignored. Other bits in this register can be programmed for the same transaction when writing this bit to 1.
0	RW	1b	**SPI Access Request** 0: No request 1: Request that the other SPI master stop initiating long transactions on the SPI bus This bit defaults to a 1 and must be cleared by BIOS after completing the accesses for the boot process.

Offset Address: 07-04h (SPI-MMIO)
SPI Address (SPIA) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:0	RW	0	**SPI Cycle Address <SCA>** This field is shifted out as the SPI Address (MSb first). Bit[23:0] correspond to Address bit[23:0].

Offset Address: 0F-08h (SPI-MMIO)
SPI Data 0 Register (SPID0) **Default Value: 0h**

Bit	Attribute	Default	Description
63:0	RW	0	**SPI Cycle Data[0] <SCD[0]>** This field is shifted out as the SPI Data on the Master-Out Slave-in Data pin during the data portion of the SPI cycle. The register also shifts in the data from the Master-in Slave-Out pin into this register during the data portion of the SPI cycle. The data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.

Offset Address: 17-10h (SPI-MMIO)
SPI Data 1 Register (SPID1) **Default Value: 0h**

Bit	Attribute	Default	Description
63:0	RW	0	**SPI Cycle Data[1] <SCD[1]>** (Same as SPID0)

Notes for SPI Cycle Data:

SCD Memory Address

SPI Data[0]: SPIBAR + 08h (Size:64bits)
SPI Data[1]: SPIBAR + 10h (Size:64bits)
SPI Data[2..7]: SPIBAR + (18h~47h) Reserved

SCD Shift Order

The SCD[N] register does not begin shift until SPID[N-1] has completely shifted in/out. The data is always shifted starting with the least significant byte, msb to lsb, followed by the next least significant byte, msb to lsb, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13-…-8-23-22-…-16-31…-24-39..32…-etc. Bit 56 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address.

Default values

1. For SPI Data [7:1]: Default values are 0.
2. For SPI Data 0: This register is initialized to 0 by the reset assertion. However, the least significant byte of this register is loaded with the first Status Register read of the Atomic Cycle Sequence that the hardware automatically runs out of reset. Therefore, bit 0 of this register can be read later to determine if the platform encountered the boundary case in which the SPI flash was busy with an internal instruction when the platform reset deasserted.

Offset Address: 18-4Fh (SPI-MMIO) – Reserved

Offset Address: 53-50h (SPI-MMIO)

BIOS Base Address (BBAR) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Reserved**
23:8	RW	0	**Bottom of System Flash** This field determines the bottom of the System BIOS. The chip will not run programmed commands nor memory reads whose address field is less than this value. This field corresponds to bit[23:8] of the 3-Bytes address; bit[7:0] are assumed to be 00h for this vector when comparing to a potential SPI address. Note: Software must always program 1s into the upper, Don't Care, bits of this field based on the flash size. Hardware does not know the size of the flash array and relies upon the correct programming by software. The default value of 0000h results in all cycles allowed. In the event that this value is programmed below some of the BIOS Memory segments, this protection policy takes precedence.
7:0	RO	0	**Reserved**

Note: This register is not writable when the SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 55-54h (SPI-MMIO)

Prefix Opcode Configuration (PREOP) **Default Value: 0004h**

Bit	Attribute	Default	Description
15:8	RW	0	**Prefix Opcode 1** Software programs an SPI pcode into this field that is permitted to run as the first command in an atomic cycle sequence.
7:0	RW	04h	**Prefix Opcode 0** Software programs an SPI pcode into this field that is permitted to run as the first command in an atomic cycle sequence.

Note: This register is not writable when the SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 57-56h (SPI-MMIO)

Opcode Type Configuration (OPTYPE) **Default Value: 0000h**

Bit	Attribute	Default	Description
15:14	RW	00b	**Opcode Type7** (Refer to the description in bit[1:0])
13:12	RW	00b	**Opcode Type6** (Refer to the description in bit[1:0])
11:10	RW	00b	**Opcode Type5** (Refer to the description in bit[1:0])
9:8	RW	00b	**Opcode Type4** (Refer to the description in bit[1:0])
7:6	RW	00b	**Opcode Type3** (Refer to the description in bit[1:0])
5:4	RW	00b	**Opcode Type2** (Refer to the description in bit[1:0])
3:2	RW	00b	**Opcode Type1** (Refer to the description in bit[1:0])
1:0	RW	00b	**Opcode Type0** This field specifies information about the corresponding Opcode 0. This information allows the hardware to: 1) Decide whether to use the address field and 2) Provide BIOS and Shared Flash protection capabilities. The encoding of the two bits is: 00: No address associated with this opcode; Read cycle type 01: No address associated with this opcode; Write cycle type 10: Address required; Read cycle type 11: Address required; Write cycle type

Note: This register is not writable when the SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 5F-58h (SPI-MMIO)

Opcode Menu Configuration (OPMENU) **Default Value: 0**

Bit	Attribute	Default	Description
63:56	RW	0	**Opcode 7** (See the description for bit[7:0].)
55:48	RW	0	**Opcode 6** (See the description for bit[7:0].)
47:40	RW	0	**Opcode 5** (See the description for bit[7:0].)
39:32	RW	0	**Opcode 4** (See the description for bit[7:0].)
31:24	RW	0	**Opcode 3** (See the description for bit[7:0].)
23:16	RW	0	**Opcode 2** (See the description for bit[7:0].)
15:8	RW	0	**Opcode 1** (See the description for bit[7:0].)
7:0	RW	0	**Opcode 0** Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register.

Note: This register is not writable when the SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 63-60h (SPI-MMIO)

Protected BIOS Range[0] (PBR0) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31	RW	0	**Write Protection Enable** 0: Disable. The base and limit field are ignored when this bit is cleared. 1: Enable. The base and limit fields in this register are valid.
30:24	RO	0	**Reserved**
23:12	RW	0	**Protected Range Limit** This field corresponds to SPI address bit[23:12] and specifies the upper limit of the protected range. Note: Any address greater than the value programmed in this field is unaffected by this protected range.
11:0	RW	0	**Protected Range Base** This filed corresponds to SPI address [23:12] and specifies the lower base of the protected range. Note: Address bit[11:0] are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

Note: This register is not writable when the SPI Configuration Lock-Down bit (Rx00[15]) is set.

Offset Address: 67-64h (SPI-MMIO)

Protected BIOS Range[1] (PBR1) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	(Register description is the same as PBR[0])

Offset Address: 6B-68h (SPI-MMIO)

Protected BIOS Range[2] (PBR2) **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	(Register description is the same as PBR[0])

Offset Address: 6Ch (SPI-MMIO)

Clock Divider **Default Value: 02h**

Bit	Attribute	Default	Description
7:0	RW	02h	**SPI Master Clock Divider Value** 02h to indicate 8 MHz. The exact frequency: 33/2^n MHZ n = value (Rx6C)

Offset Address: 6Dh (SPI-MMIO)

Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Latch MISO (Master In / Slave Out) at Negative Edge of CLK** 0: Disable 1: Enable SPI controller will latch MISO (ballname: SPIDI) at the negative edge of bus clock if this option is enabled.
4	RW	0	**SPI Interrupt Enable** 0: Disable 1: Enable
3	RW	0	**Dynamic Clock On** 0: Free clock 1: Dynamic clock
2:1	RW	00b	**Debug Mode** 00: S-state 01: DDBC 10: {block0, block1, data_cycle, SPIGNT, WIP1} 11: {SPICFGHIT, SPIDEVCYC, ROMHIT, 2'b0}
0	RW	0	**Command Post Write Enable** 0: Disable 1: Enable

Device 17 Function 7 (D17F7): South-North Module Interface Control

This configuration is provided to facilitate the configuration of the North Module Interface logic of the South Module ("SM") without requiring new enumeration code. This function is represented as Device 17, Function 7.

PCI Configuration Space Header (00-3Fh)

Offset Address: 01-00h (D17F7)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 03-02h (D17F7)

Device ID **Default Value: A353h**

Bit	Attribute	Default	Description
15:0	RO	A353h	**Device ID**

Offset Address: 05-04h (D17F7)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0. (Not supported)
8	RW	0	**SERR# Enable**
7	RO	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5	RO	0	**VGA Palette Snooping** Hardwired to 0. (Not implemented)
4	RO	0	**Memory Write and Invalidate** Hardwired to 0 (Not supported)
3	RO	0	**Respond To Special Cycle** Hardwired to 0.
2	RW	0	**Bus Master** 0: Never behave as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space Access** 0: Not respond to memory space access 1: Respond to memory space access
0	RO	0	**I/O Space Access** 0: Not respond to I/O space access 1: Respond to I/O space access

Offset Address: 07-06h (D17F7)

PCI Status **Default Value: 0200h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** Set by PERRS, reset by writing 1.
14	RW1C	0	**Detected SERR#** Note: Set if ECC error
13	RW1C	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
12	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion**
10:9	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium (default) 10: Slow 11: Reserved
8	RW1C	0	**Set When Set or Observed SERR# and Parity Error** Reserved
7	RO	0	**Capable of Accepting Fast Back-to-back as a Target** Reserved
6	RO	0	**Reserved**
5	RO	0	**66 MHz Capable**
4	RO	0	**Support New Capability List**
3:0	RO	0	**Reserved**

Offset Address: 08h (D17F7)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D17F7)

PCI Header Registers **Default Value: 06 0000h**

Bit	Attribute	Default	Description
23:0	RO	060000h	**Class Code**

Offset Address: 0Ch (D17F7) – Reserved

Offset Address: 0Dh (D17F7)

Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RW	0	**PCI Bus Time Slice Bit[7:3] for CPU as A Master (in unit of PCI clocks)** Bit[7:3] is programmable; however it is always read 0 if RxE0[5] = 1.
2:0	RO	0	**Reserved**

Offset Address: 0Eh (D17F7)
Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Header Type** It adheres to the PCI-PCI Bridge Configuration.

Offset Address: 0Fh (D17F7)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST Support**
6:0	RO	0	**Reserved**

Offset Address: 10F-1Fh (D17F7) – Reserved

Offset Address: 2D-2Ch (D17F7)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D17F7)
Subsystem ID **Default Value: 7323h**

Bit	Attribute	Default	Description
15:0	RO	7323h	**Subsystem ID**

Offset Address: 30h-3Fh (D17F7) – Reserved

Offset Address: 34h (D17F7)
Capability Pointer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Capability Pointer** Byte offset into configuration space to capability list

Offset Address: 35-3Fh (D17F7) – Reserved

South -North Module Interface Control (40-5F)

Offset Address: 40-4Eh (D17F7) – Reserved

Offset Address: 4Fh (D17F7)

South-North Module Interface Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Enable P2P Bridge Header for External PCI Bus** 0: Disable 1: Enable
5:3	RO	0	**Reserved**
2	RW	0	**Hide C2P (CPU to PCI) Cycle for Internal Devices on PCI BUS** When Bit[6] set to 1, only cycles which act with external PCI devices will appear on PCI Bus. 0: Cycles of internal PCI devices show on PCI bus then to internal device 1: Cycles of internal PCI devices go to internal devices directly.
1	RW	0	**Support Extended Configuration Space Up to 4096 Bytes** 0: Disable 1: Enable
0	RW	0	**C2P Cycle Wait till P2C Write Flushed** (except C2P Post-Write) 0: Disable. C2PRA is not blocked. 1: Enable. C2PRA waits for PCI1 P2C write FIFO empty.

Offset Address: 50h (D17F7)

Bus Priority of SM Peripheral Device **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Card Reader Priority** 0: Low Priority 1: High Priority
6	RW	0	**SDIO Priority** 0: Low Priority 1: High Priority
5	RW	0	**SATA Priority** 0: Low Priority 1: High Priority
4	RW	0	**USB Priority** 0: Low Priority 1: High Priority
3	RW	0	**HDAC Priority** 0: Low Priority 1: High Priority
2	RW	0	**IDE Priority** 0: Low Priority 1: High Priority
1	RW	0	**LPC/UART/FIR Priority** 0: Low Priority 1: High Priority
0	RW	0	**PCI1 Priority** 0: Low Priority 1: High Priority

Offset Address: 51h (D17F7)

P2P Bridge Related Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Enable Subtract Decode for P2P Cycle** 0: Disable 1: Enable
6:3	RO	0	**Reserved**
2	RW	0	**Enable PCI Master Function** 0: Enable PCI master function by D19F0 Rx04[2] 1: Enable PCI master function even when D19F0 Rx04[2] is disabled.
1	RO	0	**Reserved**
0	RW	0	**Support Subtract Decode in P2P Bridge Class Code** 0: Class code will be 060400 as positive decode P2P Bridge 1: Class code will be 060401 as subtractive decode P2P Bridge

Offset Address: 52h (D17F7)

CCA Arbitration Occupy Timer Control **Default Value: 11h**

Bit	Attribute	Default	Description
7:4	RW	0001b	**SM Internal Device Occupy Timer** 0000: Disable timer, granted as long as request asserted 0001: Time out after 1 grant 0010: Time out after 2 grants …. 1111: Time out after 15 grants
3:0	RW	0001b	**HDAC Occupy Timer** 0000: Disable timer, granted as long as request asserted 0001: Time out after 1 grant 0010: Time out after 2 grants …. 1111: Time out after 15 grants

Offset Address: 53h (D17F7)

CCA Arbitration Promote Timer Control **Default Value: 11h**

Bit	Attribute	Default	Description
7:4	RW	0001b	**SM Internal Device Promote Timer** 0000: Disable timer, granted as long as request asserted 0001: Time out after 1 grant 0010: Time out after 2 grants …. 1111: Time out after 15 grants
3:0	RW	0001b	**HDAC Promote Timer** 0000: Disable timer, granted as long as request asserted 0001 : Time out after 1 grant 0010: Time out after 2 grants …. 1111: Time out after 15 grants

Offset Address: 54h (D17F7)
CCA REQ Timing Option **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RO	0	**Reserved**
5	RW	0	**Synchronize Card Reader REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
4	RW	0	**Synchronize SDIO REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
3	RW	0	**Synchronize IDE REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
2	RW	0	**Synchronize SATA REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
1	RW	0	**Synchronize USB REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using
0	RW	0	**Synchronize LPC/ISA REQ for Better Timing** 0: Use original REQ 1: Synchronize REQ before using

Offset Address: 55h (D17F7)
RIOPU for PAD **Default Value: 0Fh**

Bit	Attribute	Default	Description
7:3	RO	00001b	**Reserved** (Do not program)
2	RW	1b	**IRQ15, PDIOR#, PDIOW# Signal Pad Internal Pull-Up** 0: Disable 1: Enable
1	RW	1b	**REQ[3:0]#, GNT[3:0]#, INT[A:D]# Signal Pad Internal Pull-Up** 0: Disable 1: Enable
0	RW	1b	**FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, PERR#, SERR# Signal Pad Internal Pull-Up** 0: Disable 1: Enable

Offset Address: 56h (D17F7)
Strapping Pin Value **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2	RO	0	**LPC FWH Command** 0: Enable 1: Disable
1	RO	0	**System Auto Reboot** 0: Enable 1: Disable
0	RO	0	**SPI/LPC ROM Select** 0: LPC ROM 1: SPI ROM

Offset Address: 57-5Fh (D17F7) – Reserved

DRAM Configuration (60h)

Offset Address: 60h (D17F7)
DRAM Ending for Bank 7 **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RW	01h	**DRAM Bank 7 Ending Address High (Host Address Bits[31:24])**

Shadow RAM Control (61-64h)

Offset Address: 61h (D17F7)

Page-C ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**CC000-CFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00b	**C8000-CBFFFh Memory Space Access Control** (See Bit[7:6] for bit value descriptions.)
3:2	RW	00b	**C4000-C7FFFh Memory Space Access Control** (See Bit[7:6] for bit value descriptions.)
1:0	RW	00b	**C0000-C3FFFh Memory Space Access Control** (See Bit[7:6] for bit value descriptions.)

Offset Address: 62h (D17F7)

Page-D ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**DC000-DFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00b	**D8000-DBFFFh Memory Space Access Control** (See Bit[7:6] for bit value descriptions.)
3:2	RW	00b	**D4000-D7FFFh Memory Space Access Control** (See Bit[7:6] for bit value descriptions.)
1:0	RW	00b	**D0000-D3FFFh Memory Space Access Control** (See Bit[7:6] for bit value descriptions.)

Offset Address: 63h (D17F7)

Page-E / F ROM, Memory Hole and SMI Decoding **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**E0000-EFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00b	**F0000-FFFFFh Memory Space Access Control** See Bit[7:6] descriptions.
3:2	RW	00b	**Memory Hole** 00: None 01: 512K – 640K 10: 15M – 16M (1M) 11: 14M – 16M (2M)
1:0	RO	0	**Reserved**

Offset Address: 64h (D17F7)

Page-E ROM Shadow Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:6	RW	00b	**EC000-EFFFFh Memory Space Access Control** 00: Read / Write Disable 01: Write Enable 10: Read Enable 11: Read / Write Enable
5:4	RW	00b	**E8000-EBFFFh Memory Space Access Control** (See Bit[7:6] for bit value descriptions.)
3:2	RW	00b	**E4000-E7FFFh Memory Space Access Control** (See Bit[7:6] for bit value descriptions.)
1:0	RW	00b	**E0000-E3FFFh Memory Space Access Control** (See Bit[7:6] for bit value descriptions.)

Offset Address: 65-6Fh (D17F7) – Reserved

Conventional PCI Bus Control (70-7Fh)

Offset Address: 70h (D17F7)

CPU to PCI Flow Control – 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**CPU to PCI Post-Write** 0: Disable 1: Enable C2P posted cycle could be delayed by PCI master cycles (i.e. PCI master access is allowed even if C2P buffer is not flushed).
6	RW	0	**PCI Delay Transaction for Master Read when Timer Time-Out** 0: Disable 1: Enable To enable this function, D17F7 RxE3[0] must be set to 1. When this bit is set, the PCI controller will assert STOP# when a PCI master read occupies the PCI bus longer than the PCI Master Timer period. PCI Master Timer is setup through Rx75[2:0].
5:4	RW	00b	**PCI Master to DRAM Prefetch Control** 00: Always prefetch 10: Prefetch only for enhancing command x1: Disable prefetch
3	RW	0	**PCI Delay Transaction for Master Read** 0: Disable 1: Assert STOP# for PCI master read cycle and start delay transaction.
2	RO	0	**Reserved**
1	RW	0	**Delay Transaction** 0: Disable 1: Enable
0	RW	0	**Cacheline Size** 0: 4QW 1: 8QW

Offset Address: 71h (D17F7)

CPU to PCI Flow Control – 2 **Default Value: 48h**

Bit	Attribute	Default	Description
7	RW1C	0b	**Retry Status** 0: No retry occurred 1: Retry occurred
6	RW	1b	**Action When Retry Timeout** 0: Continuous retry (record status only) 1: Flush buffer (write) or return 0FFFFFFFFh (read)
5:4	RW	00b	**Retry Count (before back off CPU)** 00: Retry 2 times, back off CPU 01: Retry 16 times, back off CPU 10: Retry 4 times, back off CPU 11: Retry 64 times, back off CPU
3	RW	1b	**PCI Burst Timeout Enable** 0: Disable 1: Enable
2	RO	0	**Reserved**
1	RW	0	**Compatible TYPE#1 Configuration Cycle AD31** 0: Fix AD31 1: Support type#1 configuration cycle
0	RO	0	**Reserved**

Offset Address: 72h (D17F7)

PCI P2C Read Caching and Prefetch Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**No Arbitration on PCI Bus during PCI-DMA Period** 0: Disable 1: Enable
6	RO	0	**Reserved**
5	RW	0	**Conservative Read Caching** 0: Disable 1: Enable When set to 1, the previous prefetched data will be flushed when PCI master changes or starting address is not consecutive.
4	RO	0	**Reserved**
3	RW	0	**P2CR Pre-fetched Data Flushing Condition** 0: Pre-fetched data will only be flushed when C2P cycle occurs or when interrupt comes. 1: Besides the above conditions, the pre-fetched data will also be flushed when the next FRAME# comes with different REQ/GNT or address
2	RW	0	**PCI Master Read ("P2CR") Pre-fetched Data Control** 0: Pre-fetched data is invalidated when FRAME# is de-asserted without STOP 1: Pre-fetched data is invalidated based on the setting of bit 3.
1:0	RW	00b	**P2CR FIFO Prefetch Depth** 00: Prefetch if outstanding read <= 1 line 01: Prefetch if outstanding read <= 2 line 10: Prefetch if outstanding read <= 3 line 11: Prefetch if outstanding read <= 5 line

Offset Address: 73h (D17F7)

PCI Master Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**PCI Master 1-Wait State Write** 0: Disable 1: Enable
5	RW	0	**PCI Master 1-Wait State Read** 0: Disable 1: Enable
4	RW	0	**APIC Cycle Block P2C Write Cycle** 0: Enable 1: Disable
3	RW	0	**P2CR Caching Flush by NM Special Cycle** 0: Disable 1: Enable
2:1	RO	0	**Reserved**
0	RW	0	**PCI Master Broken Timer Enable** 0: Disable 1: Enable. Force into arbitration when there is no FRAME# 16 PCICLK after GNT.

Offset Address: 74h (D17F7)

South-North Module Interface Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Disable Dynamic CCA Clock Stop** 0: Enable 1: Disable
6	RW	0	**Disable Dynamic PCI1 Clock Stop** (including VKCKG) 0: Enable 1: Disable
5	RO	0	**Reserved**
4	RW	0	**Lock Cycle Issued by CPU Flush P2C Cycles Before C2P**
3	RW	0	**Lock Cycle Issued by CPU Block P2C Cycles**
2	RW	0	**APIC FSB Directly up through CCA (not on PCI)** To enable this function, both Rx74[2] and Rx7C[1] must be set to 1.
1:0	RO	0	**Reserved**

Offset Address: 75h (D17F7)

PCI Arbitration 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**Arbitration Mode** 0: REQ-based (arbitrate at the end of REQ#) 1: Frame-based (arbitrate as FRAME# asserts)
6:4	RW	0	**PCI Bus Time Slice Bit[2:0] for CPU as A Master (in unit of PCI clocks)**
3	RW	0	**Disable PCI Master Time-out / Enable New Grant Mechanism** 0: Enable PCI Master time-out / disable new grant mechanism 1: Disable PCI Master time-out / enable new grant mechanism
2:0	RW	000b	**PCI Master Bus Timeout** 000: Disable 001: 1x16 PCLKs 010: 2x16 PCLKs 011: 3x16 PCLKs 111: 7 x 16 PCLKs

Offset Address: 76h (D17F7)

PCI Arbitration 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**IO Port 22 Enable (SM)** 0: CPU access to IO address 22 is passed onto the PCI bus 1: CPU access to IO address 22 is processed internally IO
6	RW	0	**PCI Bus Parking at the Last PCI Master** 0: Disable 1: Enable
5:4	RW	00b	**Master Priority Rotation Control** 00: Disable 01: Grant to CPU after every PCI master grant 10: Grant to CPU after every 2 PCI master grants 11: Grant to CPU after every 3 PCI master grants
3:2	RW	00b	**Selected REQ# as RQ4** 00: REQ4 01: REQ0 10: REQ1 11: REQ2
1	RO	0	**Reserved**
0	RW	0	**Enable RQ4 as High Priority Master** 0: Disable 1: Enable

Offset Address: 77h (D17F7)

South Module Miscellaneous Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**CPU to PCI Peripheral Device Read Blocked by PCI1 FIFO Empty** 0: CPU to PCI peripheral device read blocked by PCI master to memory write 1: CPU to PCI peripheral device read blocked by PCI1 FIFO empty CPU to PCI peripheral device read is blocked by PCI master to memory write when Rx4F[0] = 1. Note: This bit needs to work with Rx4F[0] assertion.
5	RO	0	**Reserved**
4:3	RW	00	**Read FIFO Timer** 00: No timer 01: Timeout after 1 ms 10: Timeout after 4 ms 11: Timeout after 16 ms
2:0	RO	0	**Reserved**

Offset Address: 78-79h (D17F7) – Reserved

Offset Address: 7Ah (D17F7)
PCI V2X Device Capability **Default Value: 00h**

Bit	Attribute	Default	Description
7	RW	0	**PREQ's Device Is Capable of V2X** Internal devices pass to PCI bus in V2X mode. 0: Not support V2X mode 1: Support V2X mode
6	RW	0	**REQ6's Device Is Capable of V2X** 0: Not support V2X mode 1: Support V2X mode
5	RW	0	**REQ5's Device Is Capable of V2X** 0: Not support V2X mode 1: Support V2X mode
4	RW	0	**REQ4's Device Is Capable of V2X** 0: Not support V2X mode 1: Support V2X mode
3	RW	0	**REQ3's Device Is Capable of V2X** 0: Not support V2X mode 1: Support V2X mode
2	RW	0	**REQ2's Device Is Capable of V2X** 0: Not support V2X mode 1: Support V2X mode
1	RW	0	**REQ1's Device Is Capable of V2X** 0: Not support V2X mode 1: Support V2X mode
0	RW	0	**REQ0's Device Is Capable of V2X** 0: Not support V2X mode 1: Support V2X mode

Offset Address: 7Bh (D17F7)
REQ Status **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**PREQ Status** PREQ is for internal devices. 0: Inactive 1: Active
6	RO	0	**REQ6 Status** 0: Inactive 1: Active
5	RO	0	**REQ5 Status** 0: Inactive 1: Active
4	RO	0	**REQ4 Status** 0: Inactive 1: Active
3	RO	0	**REQ3 Status** 0: Inactive 1: Active
2	RO	0	**REQ2 Status** 0: Inactive 1: Active
1	RO	0	**REQ1 Status** 0: Inactive 1: Active
0	RO	0	**REQ0 Status** 0: Inactive 1: Active

Offset Address: 7Ch (D17F7)
MSI Related Control **Default Value: 02h**

Bit	Attribute	Default	Description
7:2	RO	0	**Reserved**
1	RW	1b	**APIC FSB Directly up through CCA (not on PCI)** To enable this function, both Rx74[2] and Rx7C[1] must be set to 1.
0	RO	0	**Reserved**

Offset Address: 7D-CFh (D17F7) – Reserved

HDAC Control (D0-DFh)

Offset Address: D0h (D17F7) – Reserved

Offset Address: D1h (D17F7)

HDAC and P2P Related **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Enable the Capability / Status Write of the P2P Bridge Configuration Capability** 0: Disable 1: Enable
2	RW	0	**Disable HDAC** 0: Enable HDAC 1: Disable HDAC
1:0	RO	0	**Reserved**

Offset Address: D2-DFh (D17F7) – Reserved

Dynamic Clock Control (E0-E3h)

Offset Address: E0h (D17F7)

Dynamic Clock Control 1 **Default Value: 40h**

Bit	Attribute	Default	Description
7	RW	0	**CCA New Dynamic Clock Scheme Enable** 0: Old dynamic clock scheme 1: New dynamic clock scheme
6	RW	1b	**CCA Dynamic Clock On** 0: CCA uses dynamic clock 1: CCA uses free running clock
5	RW	0	**Enable Rx0D Latency Timer - Always Read as 0** 0: Disable 1: Enable
4	RW	0	**Enable Retry When Entering C3 State** 0: When entering C3 state, the upstream will be blocked after current PCI master cycle is done. 1: When entering C3 state, current PCI master cycle will be retried at once, then be blocked.
3	RW	0	**APIC Cycle Flush HDAC Upstream Write Cycle** 0: Disable 1: Enable
2	RW	0	**HDAC Upstream Read Cycle Passes Write** 0: Enable 1: Disable
1	RW	0	**Enable Outputting the Signal of Upstream Read Cycle from Legacy Devices to NM** Legacy devices include LPC, FIR, UART and SPI. 0: Disable 1: Enable
0	RW	0	**Enable Outputting the Signal of Upstream Write Cycle from Legacy Devices to NM** Legacy devices include LPC, FIR, UART and SPI. 0: Disable 1: Enable

Offset Address: E1h (D17F7)

Dynamic Clock Control 2 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6:4	RW	000b	**Frame Buffer Size for PCI1 Decode.** 000: Disable 001: 2M 010: 4M 011: 8M 100: 16M 101: 32M 11x: Reserved
3:0	RO	0	**Reserved**

Offset Address: E2h (D17F7)

Dynamic Clock Control 3 **Default Value: 1Fh**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	1b	**Downstream Interface Clock Control** 0: New dynamic clock scheme in this chip 1: Free run
3	RW	1b	**PCI1 Clock Control** 0: New dynamic clock scheme in this chip 1: Free run
2	RW	1b	**Downstream HDAC Clock Control** 0: New dynamic clock scheme in this chip 1: Free run
1	RW	1b	**Downstream SM Internal PCI Device Clock Control** 0: New dynamic clock scheme in this chip 1: Free run
0	RO	1b	**Reserved** (Do not program)

Offset Address: E3h (D17F7)

PCI1 Internal 33/66MHz Dynamic Clock Control **Default Value: 6Eh**

Bit	Attribute	Default	Description
7	RW	0	**Improve P2C Read (P2CR) Performance** 0: Allocate one cacheline of FIFO for P2CR prefetch. 1: Allocate two cacheline of FIFO for P2CR prefetch. Set 1 when only one PCI master has requested (no pending PCI REQ); otherwise, allocate one cacheline of FIFO for prefetch.
6	RW	1b	**Improve the PCI1 Dynamic Clock** 0: Clock enable until FIFO release 1: Clock enable until cycle is done and can save more power
5	RW	1b	**PCI1 33/66MHz Dynamic Clock Control** 0: PCI clock (33/66MHz) is kept ON as long as GRANT# is asserted to PCI device. 1: PCI clock (33/66 MHz) will be gated OFF whenever PCI1 is idle (with or without GRANT# asserted)
4	RW	0	**P2CR Data Timout Enable** Back off PCI Master while not getting TRDY and PCI time out (PCI timer is at Bit [3:1]) 0: Disable 1: Enable
3:1	RW	111b	**P2CR Data Timer** (PCI Master TRDY Timeout) 000: Disable 001: 1*8 PCICLKs 010: 2*8 PCICLKs 011: 3*8 PCICLKs 100: 4*8 PCICLKs 101: 5*8 PCICLKs 110: 6*8 PCICLKs 111: 7*8 PCICLKs
0	RW	0	**Enable P2C Read Back Off Even when Only One PCI Master** It can't retry when only one PCI master and Rx76[6] = 1. (This bit works with Rx70[6] =1.) 0: Not retry when only one PCI Master and bus times out. 1: Retry when bus times out, even though there is only one PCI Master.

DRAM Above 4G Support (E4-FFh)

Offset Address: E4h (D17F7)

Low Top Address - Low **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**Low Top Address – [23:20]**
3:0	RW	0	**DRAM Granularity** (Powell) Total DRAM Bit[3:0] Less than Granularity 0h 4G 16M 1h 8G 32M 2h 16G 64M 3h 32G 128M 4h 64G 256M RANK Ending Address Formula: ENDxA[35:24] = RENDxA << Bit [3:0]; (x = 0,1,2,3,4,5,6,7)

Offset Address: E5h (D17F7)

Low Top Address - High **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Low Top Address – [31:24]**

Offset Address: E6h (D17F7)

System Management Mode (SMM) and APIC Decoding **Default Value: 01h**

Bit	Attribute	Default	Description
7:5	RO	0	**Reserved**
4	RW	0	**IO APIC Decoding** 0: Cycles accessing FECx_xxxx are passed to PCI1. 1: Cycles accessing to FEC7_FFFF - FEC0_0000 are passed to PCI1. Cycles accessing to FECF_FFFF - FEC8_0000 are passed to PCI2.
3	RW	0	**MSI Support (Processor Message Enable)** 0: Cycles accessing FEEx_xxxx from masters are passed to PCI1. (PCIC will not claim). 1: Cycles accessing FEEx_xxxx from masters are passed to the Host side for snooping.
2	RW	0	**Top SMM Enable** 0: Disable 1: Enable
1	RW	0	**High SMM Enable** 0: Disable 1: Enable
0	RW	1b	**Compatible SMM Enable** 0: Disable 1: Enable

Offset Address: E7-FBh (D17F7) – Reserved

Offset Address: FCh (D17F7)

PCI Bus Control **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RO	0	**Reserved**
3	RW	0	**Enable STPCLK# / A20M# / IGNNE# for FSB** 0: STPCLK# / A20M# / IGNNE# to CPU through external pins 1: STPCLK# / A20M# / IGNNE# to CPU through up message
2:0	RO	0	**Reserved**

Offset Address: FD-FFh (D17F7) – Reserved

Device 19 Function 0 (D19F0): PCI to PCI Bridge

** VX820 Series does not support PCI.*

PCI Configuration Space Header (00-3Fh)

Offset Address: 01-00h (D19F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**VIA Technology ID**

Offset Address: 03-02h (D19F0)

Device ID **Default Value: 3353h**

Bit	Attribute	Default	Description
15:0	RO	B353h	**Device ID**

Offset Address: 05-04h (D19F0)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:10	RO	0	**Reserved**
9	RO	0	**Fast Back-to-Back Cycle Enable** Hardwired to 0. (Not supported)
8	RW	0	**SERR# Enable**
7	RO	0	**Reserved**
6	RW	0	**Parity Error Response** 0: Ignore parity errors 1: Perform parity check and take normal action on detected parity errors
5:4	RO	0	**Reserved**
3	RO	0	**Respond To Special Cycle** Hardwired to 0.
2	RW	0	**Bus Master** 0: Never behave as a bus master 1: Enable to operate as a bus master on the secondary interface
1	RW	0	**Memory Space Access** 0: Not respond to memory space access 1: Respond to memory space access
0	RW	0	**I/O Space Access** 0: Not respond to I/O space access 1: Respond to I/O space access

Offset Address: 07-06h (D19F0)

PCI Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
14	RW1C	0	**Detected SERR#**
13	RW1C	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
12	RO	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
11	RO	0	**Target-Abort Assertion**
10:9	RO	00b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
8	RW1C	0	**Master Data Parity Error** Reserved
7	RO	0	**Capable of Accepting Fast Back-to-Back as a Target** Reserved
6:0	RO	10h	**Reserved**

Offset Address: 08h (D19F0)

Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D19F0)

Class Code **Default Value: 06 0400h**

Bit	Attribute	Default	Description
23:0	RO	060400h	**Class Code**

Offset Address: 0Ch (D19F0) – Reserved

Offset Address: 0Dh (D19F0)

Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer, Reserved** Guarantee time slice for CPU master.

Offset Address: 0Eh (D19F0)

Header Type **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Header Type**

Offset Address: 0Fh (D19F0)
Built In Self Test (BIST) **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**BIST Support**
6:0	RO	0	**Reserved**

Offset Address: 10-17h (D19F0) – Reserved

Offset Address: 18h (D19F0)
Primary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Primary Bus Number**

Offset Address: 19h (D19F0)
Secondary Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Secondary Bus Number**

Offset Address: 1Ah (D19F0)
Subordinate Bus Number **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Subordinate Bus Number**

Offset Address: 1Bh (D19F0)
Master Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Master Latency Timer**

Offset Address: 1Ch (D19F0)
IO Base Address **Default Value: F0h**

Bit	Attribute	Default	Description
7:4	RW	Fh	**IO Base Address**
3:0	RO	0	**Reserved**

Offset Address: 1Dh (D19F0)
IO Limit Address **Default Value: 00h**

Bit	Attribute	Default	Description
7:4	RW	0	**IO Limit Address**
3:0	RO	0	**IO Addressing Capability**

Offset Address: 1Eh (D19F0)
Secondary Status Register 1 **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Fast Back to Back Cycle**
6	RO	0	**Reserved**
5	RO	0	**66MHz Capability**
4:0	RO	0	**Reserved**

Offset Address: 1Fh (D19F0)
Secondary Status Register 2 **Default Value: 02h**

Bit	Attribute	Default	Description
7	RW1C	0	**Detected Parity Error** 0: No parity error detected 1: Error detected in either address or data phase
6	RW1C	0	**Detected SERR#**
5	RO	0	**Received Master-Abort** (except special cycle) 0: No abort received 1: Transaction aborted by the Master
4	RW1C	0	**Received Target-Abort** 0: No abort received 1: Transaction aborted by the Target
3	RO	0	**Target-Abort Assertion**
2:1	RO	01b	**DEVSEL# Timing** 00: Fast 01: Medium 10: Slow 11: Reserved
0	RW1C	0	**Master Data Parity Error** Reserved

Offset Address: 23-20h (D19F0)
Memory Limit and Base **Default Value: 0000 FFF0h**

Bit	Attribute	Default	Description
31:20	RW	0	**Memory Limit [31:20]**
19:16	RO	0	**Reserved**
15:4	RW	FFFh	**Memory Base [31:20]**
3:0	RO	0	**Reserved**

Offset Address: 27-24h (D19F0)
Prefetchable Memory Limit and Base **Default Value: 0001 FFF1h**

Bit	Attribute	Default	Description
31:20	RW	0	**Prefetchable Memory Limit [31:20]**
19:16	RO	1h	**Reserved**
15:4	RW	FFFh	**Prefetchable Memory Base [31:20]**
3:0	RO	1h	**Reserved**

Offset Add[redacted] 461ss: 2F-28h (D19F0)

Prefetchable Upper Limit and Base **Default Value: 0000 0000 0000 0000h**

Bit	Attribute	Default	Description
63:36	RW	0	**Prefetchable Upper Limit 32 Bits [31:4]** (Not Supported)
35:32	RW	0	**Prefetchable Upper Limit 32 Bits [3:0]**
31:4	RW	0	**Prefetchable Upper Base 32 Bits [31:4]** (Not Supported)
3:0	RW	0	**Prefetchable Upper Base 32 Bits [3:0]**

Offset Address: 33-30h (D19F0)

Upper IO Base and Limit **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:16	RO	0	**Upper IO Limit [15:0]**
15:0	RO	0	**Upper IO Base [15:0]**

Offset Address: 34h (D19F0)

Capability Pointer **Default Value: 70h**

Bit	Attribute	Default	Description
7:0	RO	70h	**Capability Pointer**

Offset Address: 35-3Dh (D19F0) – Reserved

Offset Address: 3F-3Eh (D19F0)

Bridge Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:12	RO	0	**Reserved**
11	RW	0	**Discard Timer SERR# Enable** 0: Disable 1: Enable
10	RW1C	0	**Discard Timer Status** This bit is not set in this chip design. 0: Disable 1: Enable
9	RW	0	**Secondary Discard Timer**
8	RW	0	**Primary Discard Timer**
7	RO	0	**Fast Back-to-Back Enable** 0: Disable 1: Enable
6	RW	0	**Secondary Bus Reset** 0: Disable 1: Enable
5	RW	0	**Master Abort Mode** 0: Disable 1: Enable
4	RW	0	**VGA 16-Bit Decode** 0: Disable 1: Enable
3	RW	0	**VGA Enable** 0: Disable 1: Enable
2	RW	0	**ISA Enable** 0: Disable 1: Enable
1	RW	0	**SERR# Enable** 0: Disable 1: Enable
0	RW	0	**Parity Error Response Enable** 0: Disable 1: Enable

Offset Address: 40h (D19F0)

External PCI Device Enable Control **Default Value: 00h**

Bit	Attribute	Default	Description
7	RO	0	**Reserved**
6	RW	0	**Hide AD25 on External PCI Bus when Assert** 0: Disable 1: Enable
5	RW	0	**Hide AD24 on External PCI Bus when Assert** 0: Disable 1: Enable
4	RW	0	**Hide AD23 on External PCI Bus when Assert** 0: Disable 1: Enable
3	RW	0	**Hide AD22 on External PCI Bus when Assert** 0: Disable 1: Enable
2	RW	0	**Hide AD21 on External PCI Bus when Assert** 0: Disable 1: Enable
1	RW	0	**Hide AD20 on External PCI Bus when Assert** 0: Disable 1: Enable
0	RW	0	**Hide AD19 on External PCI Bus when Assert** 0: Disable 1: Enable

Offset Address: 41-6Fh (D19F0) – Reserved

Offset Address: 73-70h (D19F0)

Capability ID and Pointer **Default Value: 0000 000Dh**

Bit	Attribute	Default	Description
31:16	RO	0	**Reserved**
15:8	RO	00h	**Capability Next Pointer**
7:0	RO	0Dh	**Capability ID** 0Dh is the capability ID for "Subsystem ID / Subsystem Vendor ID".

Offset Address: 77-74h (D19F0)

Subsystem ID and Subsystem Vendor ID **Default Value: 9323 1106h**

Bit	Attribute	Default	Description
31:16	RO/ RW	9323h	**Subsystem ID** RW if D17F7 RxD1[3]=1
15:0	RO/ RW	1106h	**Subsystem Vendor ID** RW if D17F7 RxD1[3]=1

Offset Address: 78-FFh (D19F0) – Reserved

Device 20 Function 0 (D20F0) - High Definition Audio Controller (HDAC)

PCI Configuration Space Header (00-3Fh)

Offset Address: 01-00h (D20F0)

Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Vendor ID**

Offset Address: 03-02h (D20F0)

Device ID **Default Value: 3288h**

Bit	Attribute	Default	Description
15:0	RO	3288h	**Device ID**

Offset Address: 05-04h (D20F0)

PCI Command **Default Value: 0000h**

Bit	Attribute	Default	Description
15:11	RO	0	**Reserved**
10	RW	0	**Interrupt Disable**
9	RO	0	**Fast Back to Back**
8	RO	0	**SERR# Enable**
7	RO	0	**Address Stepping**
6	RO	0	**Parity Error Response**
5	RO	0	**VGA Palette Snooping**
4	RO	0	**Memory Write and Invalidate**
3	RO	0	**Respond to Special Cycle**
2	RW	0	**Bus Master**
1	RW	0	**Memory Space Access**
0	RO	0	**I/O Space Access**

Offset Address: 07-06h (D20F0)

PCI Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15	RO	0	**Detectd Parity Error**
14	RO	0	**Signaled System Error (SERR# asserted)**
13	RO	0	**Received Master Abort**
12	RO	0	**Received Target Abort**
11	RO	0	**Signaled Target Abort**
10:9	RO	0	**DEVSEL# Timing**
8	RO	0	**Master Data Parity Error**
7	RO	0	**Fast Back-to-Back Capability**
6:5	RO	0	**Reserved**
4	RO	1b	**Capability List**
3	RO	0	**Interrupt Status**
2:0	RO	0	**Reserved**

Offset Address: 08h (D20F0)
Revision ID **Default Value: nnh**

Bit	Attribute	Default	Description
7:0	RO	nnh	**Revision ID**

Offset Address: 0B-09h (D20F0)
Class Code **Default Value: 04 0300h**

Bit	Attribute	Default	Description
23:0	RO	040300h	**Class Code**

Offset Address: 0Ch (D20F0)
Cache Line Size **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Cache Line Size**

Offset Address: 0Dh (D20F0)
Latency Timer **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Latency Timer**

Offset Address: 0Eh (D20F0)
Header Type **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Header Type**

Offset Address: 0Fh (D20F0)
Built In Self Test **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Built In Self Test**

Offset Address: 13-10h (D20F0)
HDAC Lower Base Address **Default Value: 0000 0004h**

Bit	Attribute	Default	Description
31:14	RW	0	**Lower Base Address** 16 KB are required by hardwiring [13:4] to 0.
13:4	RO	0	**Hardwired to 0**
3	RO	0	**Not Prefetchable**
2:1	RO	10b	**Reserved** (Do not program)
0	RO	0	**Reserved**

Offset Address: 17-14h (D20F0)
HDAC Upper Base Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**HDAC Upper Base Address**

Offset Address: 18-2Bh (D20F0) – Reserved

Offset Address: 2D-2Ch (D20F0)
Subsystem Vendor ID **Default Value: 1106h**

Bit	Attribute	Default	Description
15:0	RO	1106h	**Subsystem Vendor ID**

Offset Address: 2F-2Eh (D20F0)
Subsystem ID **Default Value: 3288h**

Bit	Attribute	Default	Description
15:0	RO	3288h	**Subsystem ID**

Offset Address: 33-30h (D20F0)
Expansion ROM **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Expansion ROM**

Offset Address: 34h (D20F0)
Capability Pointer **Default Value: 50h**

Bit	Attribute	Default	Description
7:0	RO	50h	**Capability Pointer** Points to the power management capability.

Offset Address: 35-3Bh (D20F0) – Reserved

Offset Address: 3Ch (D20F0)
Interrupt Line **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RW	0	**Interrupt Line**

Offset Address: 3Dh (D20F0)
Interrupt Pin **Default Value: 01h**

Bit	Attribute	Default	Description
7:0	RO	01h	**Interrupt Pin** Fixed at 01h (INTA#).

Offset Address: 3Eh (D20F0)
Minimum Grant Period **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Minimum Grant Period** Used to specify how long a burst period is needed.

Offset Address: 3Fh (D20F0)
Maximum Latency **Default Value: 00h**

Bit	Attribute	Default	Description
7:0	RO	0	**Maximum Latency**

HDAC PCI Extended Configuration Space (40-260h)

Offset Address: 40h (D20F0) – Reserved

Offset Address: 41h (D20F0)

HDAC Control **Default Value: 30h**

Bit	Attribute	Default	Description
7:1	RO	0	**Reserved**
0	RW	0	**HDAC Dynamic Stop** 0: Free running 1:Enable dynamic stop clock

Offset Address: 42-43h (D20F0) – Reserved

Offset Address: 44h (D20F0)

Traffic Class Select **Default Value: 00h**

Bit	Attribute	Default	Description
7:3	RO	0	**Reserved**
2:0	RO	000b	**HDAC Traffic Class Assignment** 000 indicates TC0

Offset Address: 45-4Fh (D20F0) – Reserved

Offset Address: 51-50h (D20F0)

PCI Power Management Capabilities ID **Default Value: 6001h**

Bit	Attribute	Default	Description
15:8	RO	60h	**Next Capability Pointer** Points to the structure (MSI)
7:0	RO	01h	**PCI Power Management Capability** 01h indicates the linked list item as being the PCI Power Management register.

Offset Address: 53-52h (D20F0)

PCI Power Management Capabilities **Default Value: C842h**

Bit	Attribute	Default	Description
15:11	RO	19h	**PME# Can Be Generated from D3 and D0 State** Indicates the power states in which the function may assert PME#. Bit-15: PME# can be asserted from D3cold Bit-14: PME# can be asserted from D3hot Bit-13: PME# can be asserted from D2 Bit-12: PME# can be asserted from D1 Bit-11: PME# can be asserted from D0
10	RO	0	**D2 State Supported** 0: Not supported 1: Supported
9	RO	0	**D1 State Supported** 0: Not supported 1: Supported
8:6	RO	001b	**Report D3 Max Suspend Current** Reports the 3.3Vaux auxiliary current requirements for the PCI function. 000: 0 mA 001: 55 mA 010: 100 mA 011: 160 mA 100: 220 mA 101: 270 mA 110: 320 mA 111: 375 mA
5	RO	0	**Device-Specific Initialization Requirement** 0: Not required 1: Required
4	RO	0	**Reserved**
3	RO	0	**Hardwired to 0**
2:0	RO	010b	**PCI Power Support** 010b indicates that this function complies with the PCI Power Management Interface specification version 1.1.

Offset Address: 57-54h (D20F0)

Power Management Control and Status **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Hardwired to 0**
23	RO	0	**Hardwired to 0**
22	RO	0	**Hardwired to 0**
21:16	RO	0	**Reserved**
15	RW1C RSM	0	**PME Status** This bit is set when the HDAC would assert the PME# independent of the state of the bit 8.
14:9	RO	0	**Reserved**
8	RWS RSM	0	**PME Enable** Enable PME wake up.
7:2	RO	0	**Reserved**
1:0	RW	00b	**Power State** This field is used both to determinate the current power state and to set a new power state. 00: D0 01: D1 10: D2 11: D3 If software attempts to write a value of 10b or 01b into this field, the write operation will complete normally; however, no state change will occur.

Offset Address: 58-5Fh (D20F0) – Reserved

Offset Address: 61-60h (D20F0)
MSI Capability ID **Default Value: 7005h**

Bit	Attribute	Default	Description
15:8	RO	70h	**Point to the Next Capability Structure (PCIe)**
7:0	RO	05h	**MSI Capability**

Offset Address: 63-62h (D20F0)
MSI Message Control **Default Value: 0080h**

Bit	Attribute	Default	Description
15:8	RO	0	**Reserved**
7	RO	1b	**64 Bit Address Capability** 0: 32-bit 1: 64-bit
6:4	RO	0	**Multiple Message Enable** Normally these are RW bits, but software will always read 000b to indicate only 1 message is supported.
3:1	RO	0	**Hardwired to 0 Indicating Request for 1 Message**
0	RW	0	**MSI Enable** 0: Assert INTx instead of MSI. 1: MSI will be generated instead of INTx assertion.

Offset Address: 67-64h (D20F0)
MSI Message Lower Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:2	RW	0	**Message Lower Address**
1:0	RO	0	**Reserved**

Offset Address: 6B-68h (D20F0)
MSI Message Upper Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RW	0	**Message Upper Address**

Offset Address: 6D-6Ch (D20F0)
MSI Data **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RW	0	**Data Used for MSI Message**

Offset Address: 6E-6Fh (D20F0) – Reserved

Offset Address: 71-70h (D20F0)
PCI Express Capability ID **Default Value: 0010h**

Bit	Attribute	Default	Description
15:8	RO	0	**Capability Link** This is the last capability structure of the list.
7:0	RO	10h	**PCI Express Capability**

Offset Address: 73-72h (D20F0)
PCI Express Capability **Default Value: 0091h**

Bit	Attribute	Default	Description
15:8	RO	0	**Hardwired to 0**
7:4	RO	1001b	**Device / Port Type** 0000: PCI Express Endpoint device 0001: Legacy PCI Express Endpoint device 0100: Root Port of PCI Express Root Complex 0101: Upstream Port of PCI Express Switch 0110: Downstream Port of PCI Express Switch 0111: PCI Express -_to-_PCI/PCI-X Bridge 1000: PCI/PCI-X to PCI Express Bridge 1001: Root Complex Integrated Endpoint Device 1010: Root Complex Event Collector
3:0	RO	0001b	**Capability Version** Hardwired to 0001b, which indicates the PCIe Specification version.

Offset Address: 77-74h (D20F0)
Device Capabilities **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Device Capabilities** Hardwired to 0.

Offset Address: 79-78h (D20F0)
Device Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15	RO	0	**Reserved**
14:12	RO	0	**Hardwired to 0**
11	RO	0	**Snoop**
10:0	RO	0	**Hardwired to 0**

Offset Address: 7B-7Ah (D20F0)
Device Status **Default Value: 0010h**

Bit	Attribute	Default	Description
15:6	RO	0	**Reserved**
5	RO	0	**Transaction Pending** 0: All non-posted requests have been executed. 1: Some non-posted request are still pending.
4	RO	1b	**AUX Power Detected** Hardwired to 1b.
3:0	RO	0	**Hardwired to 0**

Offset Address: 7C-FFh (D20F0) – Reserved

Offset Address: 103-100h (D20F0)
Virtual Channel Enhanced Capability **Default Value: 1301 0002h**

Bit	Attribute	Default	Description
31:20	RO	130h	**Next Capability Pointer** Hardwired to 130h.
19:16	RO	1h	**Capability Structure Revision** This field is a PCI-SIG defined version number that indicates the version of the capability structure present. Hardwired to 1h to indicate PCIe version 1.1.
15:0	RO	0002h	**Extended Capability ID** This field is a PCI-SIG defined ID number that indicates the nature and format of the extended capability. Hardwired to 0002h to indicate the virtual channel capability.

Offset Address: 107-104h (D20F0)
Port VC Capability 1 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Reserved**
11:3	RO	0	**Hardwired to 0**
2:0	RO	0	**Hardwired to 0** Indicates that one extended VC is supported by the controller.

Offset Address: 10B-108h (D20F0)
Port VC Capability 2 **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:24	RO	0	**Hardwired to 0** Indicates that a VC arbitration table is not present.
23:8	RO	0	**Reserved**
7:0	RO	0	**Hardwired to 0**

Offset Address: 10D-10Ch (D20F0)
Port VC Control **Default Value: 0000h**

Bit	Attribute	Default	Description
15:0	RO	0	**Port VC Control** Reserved.

Offset Address: 10F-10Eh (D20F0)
Port VC Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:1	RO	0	**Reserved**
0	RO	0	**Hardwired to 0** Indicates that VC arbitration table is not present.

Offset Address: 113-110h (D20F0)
VC0 Resource Capability **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:0	RO	0	**Hardwired to 0** This field is not valid for endpoint devices.

Offset Address: 117-114h (D20F0)
VC0 Resource Control **Default Value: 8000 00FFh**

Bit	Attribute	Default	Description
31	RO	1b	**VC0 Enable** Hardwired to 1 for VC0**.**
30:27	RO	0	**Reserved**
26:24	RO	0	**VC0 ID** Hardwired to 0 since this field is assigned to VC0.
23:20	RO	0	**Reserved**
19:16	RO	0	**Hardwired to 0**
15:8	RO	0	**Reserved**
7:1	RW	7Fh	**TC/VC0 Map** Bit[7:1] are implemented as RW bits.
0	RO	1b	**TC/VC0 Map** Bit 0 is Hardwired to 1 since TC0 is always mapped to VC0.

Offset Address: 118-119h (D20F0) – Reserved

Offset Address: 11B-11Ah (D20F0)
VC0 Resource Status **Default Value: 0000h**

Bit	Attribute	Default	Description
15:2	RO	0	**Reserved**
1	RO	0	**Hardwired to 0** This bit is not applied to integrated device.
0	RO	0	**Hardwired to 0** This bit is not valid for endpoint devices.

Offset Address: 11C-12Fh (D20F0) – Reserved

Offset Address: 133-130h (D20F0)
Root Complex Link Declaration Enhanced Capability Header Register **Default Value: 0001 0005h**

Bit	Attribute	Default	Description
31:16	RO	0001h	**Next Capability** Hardwired to 0001h.
15:0	RO	0005h	**PCI Express Extended Capability ID** Hardwired to 0005h.

Offset Address: 137-134h (D20F0)
Element Self Description **Default Value: 0401 0100h**

Bit	Attribute	Default	Description
31:24	RO	04h	**Port Number** Hardwired to 04h indicating HDAC controller is assigned as port #5.
23:16	RO	01h	**Component ID** Hardwired to 01h.
15:8	RO	01h	**Number of Link Entries** Hardwired to 01h.
7:4	RO	0	**Reserved**
3:0	RO	0	**Element Type** The HDAC controller is an integrated root complex device, and this field reports a value of 0h.

Offset Address: 138-13Fh (D20F0) – Reserved

Offset Address: 143-140h (D20F0)
Link Description **Default Value: 0001 0001h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Target Port Number** Hardwired to 00h.
23:16	RO	01h	**Component ID** Hardwired to 01h.
15:2	RO	0	**Reserved**
1	RO	0	**Link Type** Indicates that the link points to RCRB.
0	RO	1b	**Link Valid**

Offset Address: 144-147h (D20F0) – Reserved

Offset Address: 14B-148h (D20F0)
Link Lower Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:12	RO	0	**Link Lower Address** (RCRBH Memory Address)
11:0	RO	0	**Reserved** Always reads 0.

Offset Address: 14F-14Ch (D20F0)
Link Upper Address **Default Value: 0000 0000h**

Bit	Attribute	Default	Description
31:4	RO	0	**Reserved** Always reads 0.
3:0	RO	0	**Link Upper Address**. (RCRBH Memory Address)

Offset Address: 150-260h (D20F0) – Reserved

High Definition Audio Controller Memory Mapped I/O Registers (HDAC-MMIO)

This section describes the memory mapped HDAC registers. Please refer to High Definition Audio Specification 1.0 for details.

Global Capabilities and Control (00-1Bh)

Offset Address: 01-00h (HDAC-MMIO)

Global Capabilities – GCAP **Default Value: 4401h**

Bit	Attribute	Default	Description	Mnemonic
15:12	RO	4h	**Number of Output Streams Supported** 0h: No output streams supported. 1h: 1 output streams suppported. 2h: 2 output streams suppported. Fh: 15 output streams supported.	**OSS**
11:8	RO	4h	**Number of Input Streams Supported** 0h: No input streams supported. 1h: 1 input streams suppported. 2h: 2 input streams suppported. Fh: 15 input streams supported.	**ISS**
7:3	RO	0	**Number of Bidirectional Streams Supported** 0h: No bidirectional stream supported. 1h: 1 bidirectional stream supported. 2h: 2 bidirectional stream supported. 1Eh: 30 bidirectional streams supported.	**BSS**
2	RO	0	**Reserved**	
1	RO	0	**Number of Serial Data Out Signals** 0: 1 SDOUT line is supported. 1: 2 SDOUTs are supported.	**NSDO**
0	RO	1b	**64 Bit Address Supported** 0: Only 32-bit addressing is available. 1: 64-bit addressing is supported.	**64OK**

Offset Address: 03-02h (HDAC-MMIO)

Version Number **Default Value: 0100h**

Bit	Attribute	Default	Description	Mnemonic
15:8	RO	01h	**Major Version**	**VMAJ**
7:0	RO	00h	**Minor Version**	**VMIN**

Note: The version number "0100h" indicates this chip complies with High Definition Audio Specification Rev 1.0.

Offset Address: 07-04h (HDAC-MMIO)

Payload Capability **Default Value: 001D 003Ch**

Bit	Attribute	Default	Description	Mnemonic
31:16	RO	001Dh	**Input Payload Capability** 001Dh indicates 29-word payload (464 bits). Note: This does not include bandwidth used for command and control.	**INPAY**
15:0	RO	003Ch	**Output Payload Capability** 003Ch indicates 60-word payload (960 bits). It indicates the total output payload available on the link is 60 word (960 bits).	**OUTPAY**

Offset Address: 0B-08h (HDAC-MMIO)
Global Control – GCTL **Default Value: 0000 000nh**

Bit	Attribute	Default	Description	Mnemonic
31:9	RO	0	**Reserved**	
8	RW	0	**Accept Unsolicited Response Enable** 0: Unsolicited response from codec are not accepted. 1: Unsolicited response from codec are accepted by the controller.	**UNSOL**
7:2	RsvdP	0	**Reserved**	
1	RW	0	**Flush Control** Writing a 1 to this bit initiates a flush.	***FCNTRL**
0	RWS	HwInit	**Controller Reset** For read: 0: In reset state. 1: Controller is ready for operations. For write: 0: Reset the controller. 1: Write 1 causes the controller exit its reset state and de-assert link AZRST#.	**CRST**

Offset Address: 0D-0Ch (HDAC-MMIO)
Wake Enable – WAKEEN **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:3	RsvdP	0	**Reserved**	
2:0	RW RSM	0	**AZSDIN Wake Enable Flags** 0: Disable 1: Allow the associated AZSDIN signal to generate a wake or processor interrupt. The bit[i] corresponds to AZSDIN[i] signal.	**SDI2WEN** **SDI1WEN** **SDI0WEN**

Offset Address: 0F-0Eh (HDAC-MMIO)
AZSDIN State Change Status – STATESTS **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:3	RsvdZ	0	**Reserved**	
2:0	RW1CS RSM	0	**AZSDIN State Change Status Flags** 0: No state change. 1: The associated AZSDIN signal received a "State Change" event. The bit[i] corresponds to SDIN[i] signal.	**SDI2WAKE** **SDI1WAKE** **SDI0WAKE**

Offset Address: 11-10h (HDAC-MMIO)
Global Status – GSTS **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:2	RsvdZ	0	**Reserved**	
1	RW1C	0	**Flush Status** 0: No flush cycle completed 1: Flush cycle completed This bit is set to 1 by the hardware to indicate that the flush cycle initiated by the Rx08[1] has completed. Software must write 1 to clear this bit before the next time Rx08[1] is set.	**FSTS**
0	RsvdZ	0	**Reserved**	

Offset Address: 1B-18h (HDAC-MMIO)
Stream Payload Capability **Default Value: 001D 003Ch**

Bit	Attribute	Default	Description	Mnemonic
31:16	RO	1Dh	**Input Stream Payload Capability** 1Dh indicates 29-word payload	**OUTSTRMPAY**
15:0	RO	3Ch	**Output Stream Payload Capability** 3Ch indicates 60-word payload	**INSTRMPAY**

Interrupt Control (20-27h)

Offset Address: 23-20h (HDAC-MMIO)

Interrupt Control – INTCTL **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31	RW	0	**Global Interrupt Enable** 0: Disable 1: Enable device interrupt generation.	**GIE**
30	RW	0	**Controller Interrupt Enable** 0: Disable 1: Enable controller's general interrupt. When set to 1, the controller generates an interrupt when the corresponding status bit is set due to a response interrupt, a response buffer overrun, and wake events.	**CIE**
29:8	RsvdP	0	**Reserved**	
7:4	RW	0	**Stream Interrupt Enable – for Output Stream [3:0]** 0: Disable 1: Enable	**SIE[7:4]**
3:0	RW	0	**Stream Interrupt Enable – for Input Stream [3:0]** 0: Disable 1: Enable	**SIE[3:0]**

Offset Address: 27-24h (HDAC-MMIO)

Interrupt Status – INTSTS **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31	RO	0	**Global Interrupt Status** This bit is set when one of the interrupt status bits is set. 0: No interrupt occurred 1: Some interrupt(s) occurred	**GIS**
30	RW1C	0	**Controller Interrupt Status** 0: No interrupt occurred 1: Some interrupt(s) occurred A 1 indicates that an interrupt condition occurred due to a response interrupt, a response overrun, or a codec state change request. The exact cause can be determined by interrogating the RIRB status register and the state change status register.	**CIS**
29:8	RsvdP	0	**Reserved**	
7:4	RW1C	0	**Stream Interrupt Status – for Output Stream [3:0]** 0: No interrupt occurred 1: Interrupt occurred	**SIS[7:4]**
3:0	RW1C	0	**Stream Interrupt Status – for Input Stream [3:0]** 0: No interrupt occurred 1: Interrupt occurred	**SIS[3:0]**

Synchronization Control (30-3Bh)

Offset Address: 33-30h (HDAC-MMIO)

Wall Clock Counter **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:0	RO	0	**Wall Clock Counter** 32 bits counter that is increamented at the link bitclk rate and rolls over from FFFF_FFFFh to 0000_0000h. This counter will roll over to zero with a period of approximately 179 seconds.	**WCounter**

Offset Address: 3B-38h (HDAC-MMIO)

Stream Synchronization – SSYNC **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:8	RsvdP	0	**Reserved**	
7:4	RW	0	**Stream Synchronization Bits – for Output Stream [3:0]** 0: Do not block data. 1: Stop in sending data to the link.	***SSYNC [7:4]**
3:0	RW	0	**Stream Synchronization Bits – for Input Stream [3:0]** 0: Do not block data. 1: Stop in receiving data from the link.	***SSYNC [3:0]**

HDAC CORB (Command Output Ring Buffer) Control (40-4Eh)

Offset Address: 43-40h (HDAC-MMIO)

CORB Lower Base Address – CORBLBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:7	RW	0	**CORB Lower Base Address** Lower address of the Command Output Ring Buffer.	**CORBLBASE**
6:0	RO	0	**Reserved** Hardwired to 0 for alignment to 128-byte boundary.	

Offset Address: 47-44h (HDAC-MMIO)

CORB Upper Base Address – CORBUBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	**CORB Upper Base Address** Upper 32 bits of address of the Command Output Ring Buffer.	**CORBUBASE**

Offset Address: 49-48h (HDAC-MMIO)

CORB Write Pointer **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:8	RsvdP	0	**Reserved**	
7:0	RW	0	**CORB Write Pointer** Software writes the last valid CORB entry offset into this field in Dword granularity. The DMA engine fetches commands from the CORB until the read point matches the write pointer. The field may be written while the DMA engine is running.	**CORBWP**

Offset Address: 4B-4Ah (HDAC-MMIO)

CORB Read Pointer **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15	WO	0	**CORB Read Pointer Reset** Writes a 1 to reset the CORB Read Pointer to 0. DMA engine must be stopped prior to resetting the read pointer or DMA transfer may be corrupted. This bit will always be read 0.	**CORBRPRST**
14:8	RO	0	**Reserved**	
7:0	RO	0	**CORB Read Pointer** Software reads this field to determine how many commands it can write to the CORB without over-running. The value read indicates the CORB read pointer offset in Dword granularity. The offset entry read from this field has been successfully fetched by the DMA controller and may be over-written by software. Supports up to 256 CORB entries (256*4B = 1KB) in the cyclic buffer.	**CORBRP**

Offset Address: 4Ch (HDAC-MMIO)
CORB Control – CORBCTL **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:2	RO	0	**Reserved**	
1	RW	0	**Enable CORB DMA Engine** 0: DMA stop 1: DMA run (when read pointer lags write pointer). Software must read the value back.	**CORBRUN**
0	RW	0	**CORB Memory Error Interrupt Enable** 0: Disable 1: Enable. The controller will generate an interrupt when CMEI (offset address 4D, bit 0) is set to 1.	***CMEIE**

Offset Address: 4Dh (HDAC-MMIO)
CORB Status – CORBSTS **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:1	RO	0	**Reserved**	
0	RW1C	0	**CORB Memory Error Indication** 0: No error. 1: Error detected. The controller has detected an error in the pathway between the controller and memory. An interrupt is asserted if CMEIE (offset address 4C, bit 0) is set to 1.	***CMEI**

Offset Address: 4Eh (HDAC-MMIO)
CORB Size – CORBSIZE **Default Value: 42h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RO	4h	**CORB Size Capability** 0100 indicates 256 entries (1 KB).	**CORBSZCAP**
3:2	RO	0	**Reserved**	
1:0	RO	10b	**CORB Size** 00: 2 entries (8 bytes) 01: 16 entries (64 bytes) 10: 256 entries (1 KB) 11: Reserved	**CORBSIZE**

HDAC RIRB (Response Input Ring Buffer) Control (50-5Eh)

Offset Address: 53-50h (HDAC-MMIO)
RIRB Lower Base Address – RIRBLBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:7	RW	0	**RIRB Lower Base Address** Lower address of the Response Input Ring Buffer.	**RIRBLBASE**
6:0	RO	0	**Reserved** Hardwired to 0 for alignment to 128-byte boundary.	

Offset Address: 57-54h (HDAC-MMIO)
RIRB Upper Base Address – RIRBUBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	**RIRB Upper Base Address** Upper 32 bits of address of the Response Input Output Ring Buffer.	**RIRBUBASE**

Offset Address: 59-58h (HDAC-MMIO)

RIRB Write Pointer – RIRBWP **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15	WO	0	**RIRB Write Pointer Reset** Writes 1 to reset the RIRB Write Pointer to 0. The DMA engine must be stopped prior to resetting the write pointer or DMA transfer may be corrupted. This bit always read as 0.	**RIRBWPRST**
14:8	RsvdP	0	**Reserved**	
7:0	RO	0	**RIRB Write Pointer** Indicates the last valid RIRB entry written by the DMA controller. Software reads this field to determining how many responses it can read from the RIRB. The value read indicates the RIRB write pointer offset in 2 Dword units. Supports up to 256 RIRB entries in the cyclic buffer.	**RIRBWP**

Offset Address: 5B-5Ah (HDAC-MMIO)

Response Interrupt Count – RINTCNT **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:8	RO	0	**Reserved**	
7:0	RW	00h	**Response Interrupt Count – N Response** 00h: 256 responses 01h to FFh: 1 to 255 responses The DMA engine should be stopped when changing this field or else an interrupt may be lost.	**RINTCNT**

Offset Address: 5Ch (HDAC-MMIO)

RIRB Control – RIRBCTL **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:3	RO	0	**Reserved**	
2	RW	0	**Response Overrun Interrupt Control** 0: Disable 1: Enable	**RIRBOIC**
1	RW	0	**Enable RIRB DMA Engine** 0: DMA Stop 1: DMA Run (when response queue is not empty).	**RIRBDMAEN**
0	RW	0	**Response Interrupt Control** 0: Disable 1: Enable. Generate an interrupt after N number of response are sent to the RIRB buffer or when an empty response slot is encountered on all SDINx input after a frame which returned a response. The N counter is reset when the interrupt is generated.	**RINTCTL**

Offset Address: 5Dh (HDAC-MMIO)

RIRB Status – RIRBSTS **Default Value: 00h**

Bit	Attribute	Default	Description	Mnemonic
7:3	RO	0	**Reserved**	
2	RW1C	0	**Response Overrun Interrupt Status** Hardware sets this bit to 1 when an overrun occurs in the RIRB. An interrupt may be generated if the response overrun interrupt control bit is set. 0: No overrun 1: Overrun occurred	**RIRBOIS**
1	RO	0	**Reserved**	
0	RW1C	0	**Response Interrupt** Hardware sets this bit to 1 when an interrupt has been generated after N number of response are sent to the RIRB buffer or when an empty response slot is encountered on all SDINx inputs. 0: No response interrupt 1: Response interrupt occurred	**RINTFL**

Offset Address: 5Eh (HDAC-MMIO)
RIRB Size – RIRBSIZE **Default Value: 42h**

Bit	Attribute	Default	Description	Mnemonic
7:4	RO	0100b	**RIRB Size Capability** 0100b indicates 256 entries (2 KB).	**RIRBSZCAP**
3:2	RO	0	**Reserved**	
1:0	RO	10b	**RIRB Size** 00: 2 entries (16 bytes) 01: 16 entries (128 bytes) 10: 256 entries (2 KB) 11: Reserved	**RIRBSIZE**

HDAC Immediate Command Control (60-69h)

Offset Address: 63-60h (HDAC-MMIO)
Immediate Command Input / Output Interface **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:0	WO	0	**Immediate Command Write** The written value will be sent out over the link in the next available frame. Reads always return 0's. Software must ensure that the ICB bit (bit-0) in the Immediate Command Status register is cleared before writing a value into this register or undefined behavior will result.	**ICW**

Offset Address: 67-64h (HDAC-MMIO)
Immediate Response Input Interface **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	**Immediate Response Read** Reads return the last response came over the link.	**IRR**

Offset Address: 69-68h (HDAC-MMIO)
Immediate Command Status **Default Value: 0000h**

Bit	Attribute	Default	Description	Mnemonic
15:8	RsvdZ	0	**Reserved**	
7:4	RO	0	**Immediate Response Result Address** This is the address of the codec which sent the response currently been latched in the Immediate Response Input register.	**IRRADD**
3	RO	0	**Immediate Response Result Unsolicited** This bit indicates whether the response latched in the Immediate Response Input register is a solicited response or unsolicited response. 0: A solicited response latched. 1: An unsolicited response latched.	**IRRUNSOL**
2	RO	0	**Immediate Command Version** This bit is corresponding to Rx40[4]. 0: Bit[7:4] and Bit[3] are reserved. 1: Both IRRADD and IRRUNSOL are implemented.	
1	RW1C	0	**Immediate Result Valid** This bit is set to 1 by hardware when a new response has been received. 0: No new response. 1: A new response arrived.	**IRV**
0	RO	0	**Immediate Command Busy** 0: Ready for accepting an immediate command. 1: Not ready. Software must wait until this bit becomes 0 before writing a value in Rx63-60 (ICW). Before codec initialization finishes, this bit is 1.	***ICB**

DMA Position Base Address (70-77h)

Offset Address: 73-70h (HDAC-MMIO)

DMA Position Lower Base Address – DPLBASE **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:7	RW	0	**DMA Position Lower Base Address**	**DPLBASE**
6:1	RO	0	**DMA Position Lower Base Unimplemented Bits** Hardwired to 0.	
0	RW	0	**DMA Position Buffer Enable** 0: Disable 1: Enable	**DPBE**

Offset Address: 77-74h (HDAC-MMIO)

DMA Position Upper Base Address – DPUBASE **Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	**DMA Position Upper Base Address** Upper 32 bits of address of the DMA Position Buffer Base Address.	**DPUBASE**

HDAC Stream Descriptors (80-17Fh)

HDAC Stream Descriptor Control (HDAC-MMIO)

Default Value: 00 0000h

Offset Address 82-80h: Input Stream 0
Offset Address A2-A0h: Input Stream 1
Offset Address C2-C0h: Input Stream 2
Offset Address E2-E0h: Input Stream 3
Offset Address 102-100h: Output Stream 0
Offset Address 122-120h: Output Stream 1
Offset Address 142-140h: Output Stream 2
Offset Address 162-160h: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
23:20	RW	0h	**Stream ID** A tag corresponds to the transferred data on the link. 0h: Unused 1h to 0Fh: Stream 1 to 15	**SID**
19	RO	0	**Bidirectional Direction Control** Hardwired to 0. Bidirectional engine is not supported.	**DIR**
18	RW	0	**Traffic Priority** Hardwired to 0. The traffic will be handled on a best effort basis. 0: Handles on a "best effort" basis 1: Handles as preferred traffic	**TP**
17:16	RO	00b	**Stripe Control** Hardwired to 0 indicating that the controller supports 1 SDO line. 00: 1 SDO 01: 2 SDOs 10: 4 SDOs 11: Reserved (Read Only for input streams)	**STRIPE**
15:5	RsvdP	0	**Reserved**	
4	RW	0	**Descriptor Error Interrupt Enable** Controls whether an interrupt is generated when the descriptor error status bit is set. 0: Disable 1: Enable	**DEIE**
3	RW	0	**FIFO Error Interrupt Enable** Controls whether an interrupt is generated when FIFO error (underrun/overrun) occurs. 0: Disable 1: Enable	**FEIE**
2	RW	0	**Interrupt On Completion Enable** Controls whether an interrupt occurs when a buffer completion with the IOC bit set in its descriptor. 0: Disable 1: Enable.	**IOCE**
1	RW	0	**Stream Run** 0: DMA disable. The DMA engine associated with this input stream will be disabled. If the corresponding Rx38 (SSYNC) bit is 0, input stream data will be taken from the link and moved to the FIFO and an overrun may occurs. 1: DMA enable. The DMA engine associated with this input stream is enabled to transfer data in the FIFO to main memory.	**RUN**
0	RW	0	**Stream Reset** For read: 0: Ready (not in reset state) 1: In reset state For write: 0: Exit reset 1: Reset the steam Write a 1 causes the corresponding stream to be reset. The stream descriptor registers (except the SRST bit), FIFOs, and cadence generator for the corresponding stream are reset. After the stream hardware has completed sequencing into the reset state, it will report a 1 in this bit. Software must read a 1 from this bit to verify that the stream is in reset. Writing a 0 causes the corresponding stream to exit reset. When the stream hardware is ready to being operation, it will report 0 in this bit. Software must read a 0 from this bit before accessing any of the stream registers. The run bit must be cleared before SRST is asserted.	***SRST**

HDAC Stream Descriptor Status (HDAC-MMIO) **Default Value: 00h**

Offset Address 83h: Input Stream 0
Offset Address A3h: Input Stream 1
Offset Address C3h: Input Stream 2
Offset Address E3h: Input Stream 3
Offset Address 103h: Output Stream 0
Offset Address 123h: Output Stream 1
Offset Address 143h: Output Stream 2
Offset Address 163h: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
7:6	RsvdZ	0	**Reserved**	
5	RO	0	**FIFO Ready** For an output stream: 0: Not enough data for transferring. 1: The output DMA FIFO contains enough data to maintain the output stream on the link. This bit default to 0 on reset because the fifo is cleared on a reset. For an input stream: This bit is not meaningful for an input stream. Therefore, it is always read 0 for input stream.	**FIFORDY**
4	RW1C	0	**Descriptor Error** 0: No error 1: Error occurred during the fetch of a descriptor - something bad happened. This could be a result of a master abort, a parity error, or ECC error on the bus, or any other error which renders the current buffer descriptor or BDL list useless.	**DESE**
3	RW1C	0	**FIFO Error** For an input stream, it indicates a FIFO overrun occurred while run bit is set. For an output stream, it indicates a FIFO underrrun occurred while there are still buffers to send. 0: No error 1: Error occurred	**FIFOE**
2	RW1C	0	**Buffer Completion Interrupt Status** 0: Not completed 1: Buffer operation completed This bit is set to 1 by the controller after the last sample of a buffer has been processed and the interrupt on completion bit is set in the command byte of the buffer descriptor. It remains active until software clears it by writing a 1 to this bit.	**BCIS**
1:0	RsvdZ	0	**Reserved**	

HDAC Stream Descriptor Link Position in Buffer (HDAC-MMIO) **Default Value: 0000 0000h**

Offset Address 87-84h: Input Stream 0
Offset Address A7-A4h: Input Stream 1
Offset Address C7-C4h: Input Stream 2
Offset Address E7-E4h: Input Stream 3
Offset Address 107-104h: Output Stream 0
Offset Address 127-124h: Output Stream 1
Offset Address 147-144h: Output Stream 2
Offset Address 167-164h: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
31:0	RO	0	**Link Position in Buffer** Indicates the number of bytes that have been received off the link. This register will count from 0 to the value in the cyclic buffer length register and then wrap to 0.	**LPIB**

HDAC Stream Descriptor Cyclic Buffer Length (HDAC-MMIO)

Default Value: 0000 0000h

Offset Address 8B-88h: Input Stream 0
Offset Address AB-A8h: Input Stream 1
Offset Address CB-C8h: Input Stream 2
Offset Address EB-E8h: Input Stream 3
Offset Address 10B-108h: Output Stream 0
Offset Address 12B-128h: Output Stream 1
Offset Address 14B-148h: Output Stream 2
Offset Address 16B-168h: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	**Cyclic Buffer Length** Indicates the number of bytes in the cyclic buffer. Link position in buffer will be reset when it reaches this value.	**CBL**

HDAC Stream Descriptor Last Valid Index (HDAC-MMIO)

Default Value: 0000h

Offset Address 8D-8Ch: Input Stream 0
Offset Address AD-ACh: Input Stream 1
Offset Address CD-CCh: Input Stream 2
Offset Address ED-ECh: Input Stream 3
Offset Address 10D-10Ch: Output Stream 0
Offset Address 12D-12Ch: Output Stream 1
Offset Address 14D-14Ch: Output Stream 2
Offset Address 16D-16Ch: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
15:8	RsvdP	0	**Reserved**	
7:0	RW	0	**Last Valid Index** The value written to this register indicates the index for the last valid buffer descriptor in the BDL. After the controller has processed this descriptor, it will wrap back to the first descriptor in the list on continue processing. This register must be at least 1.	**LVI**

HDAC Stream Descriptor FIFO Size (HDAC-MMIO)

Offset Address 91-90h: Input Stream 0 **Input Stream Default Value: 0060h**
Offset Address B1-B0h: Input Stream 1
Offset Address D1-D0h: Input Stream 2
Offset Address F1-F0h: Input Stream 3
Offset Address 111-110h: Output Stream 0 **Output Stream Default value: 00C0h**
Offset Address 131-130h: Output Stream 1
Offset Address 151-150h: Output Stream 2
Offset Address 171-170h: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
Input Stream				
15:8	RO	0	**Reserved**	
7:0	RO	60h	**FIFO Size** The max number of bytes that can be fetched by the controller at one time.	**FIFOSZ**
Output Stream				
15:9	RO	0	**Reserved**	
8:0	RO	C0h	**FIFO Size** The max number of bytes that can be fetched by the controller at one time. Note: Bit 8 can *only* be modified together with [7:0].	**FIFOSZ**

HDAC Stream Descriptor Format (HDAC-MMIO)

Default Value: 0000h

Offset Address 93-92h: Input Stream 0
Offset Address B3-B2h: Input Stream 1
Offset Address D3-D2h: Input Stream 2
Offset Address F3-F2h: Input Stream 3
Offset Address 113-112h: Output Stream 0
Offset Address 133-132h: Output Stream 1
Offset Address 153-152h: Output Stream 2
Offset Address 173-172h: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
15	RO	0	**Reserved**	
14	RW	0	**Sample Base Rate** 0: 48 KHz 1: 44.1 KHz	**BASE**
13:11	RW	0	**Sample Base Rate Multiple** 000: x1 001: x2 010: x3 011: x4 Others (100 to 111): Reserved	**MUL**
10:8	RW	0	**Sample Base Rate Divisor** 000 to 111: the actual sample rate divisor is DIV + 1 000: divide by 1 (48 KHz, 44.1 KHz) 001: divide by 2 (24 KHz, 22.05 KHz) 010: divide by 3 (16 KHz, 32 KHz) …	***DIV**
7	RsvdP	0	**Reserved**	
6:4	RW	0	**Bits per Sample** 000: 8 bits, packed in memory in 8-bit containers on 16bit boundary. 001: 16 bits, packed in memory in 8-bit containers on 16bit boundary. 010: 20 bits, packed in memory in 8-bit containers on 16bit boundary. 011: 24 bits, packed in memory in 8-bit containers on 16bit boundary. 100: 32 bits, packed in memory in 8-bit containers on 16bit boundary. Others (101 to 111): Reserved.	**BITS**
3:0	RW	0	**Number of Channels** 0000 to 1111: 1 to 16 channels	**CHNO**

HDAC Stream Descriptor BDL Pointer Lower Base Address (HDAC-MMIO)

Default Value: 0000 0000h

Offset Address 9B-98h: Input Stream 0
Offset Address BB-B8h: Input Stream 1
Offset Address DB-D8h: Input Stream 2
Offset Address FB-F8h: Input Stream 3
Offset Address 11B-118h: Output Stream 0
Offset Address 13B-138h: Output Stream 1
Offset Address 15B-158h: Output Stream 2
Offset Address 17B-178h: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
31:7	RW	0	**Buffer Descriptor List Lower Base Address**	**BDLLBASE**
6:0	RO	0	**Unimplemented Bits** Hardwired to 0 for alignment to 128 bytes boundary.	

Stream Descriptor BDL Pointer Upper Base Address (HDAC-MMIO) **Default Value: 0000 0000h**

Offset Address 9F-9Ch: Input Stream 0
Offset Address BF-BCh: Input Stream 1
Offset Address DF-DCh: Input Stream 2
Offset Address FF-FCh: Input Stream 3
Offset Address 11F-11Ch: Output Stream 0
Offset Address 13F-13Ch: Output Stream 1
Offset Address 15F-15Ch: Output Stream 2
Offset Address 17F-17Ch: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
31:0	RW	0	**Buffer Descriptor List Upper Base Address**	**BDLUBASE**

Alias Registers (2030-2167h)

Offset Address: 2033-2030h (HDAC-MMIO)
Wall Clock Counter Alias – WALCLKA **Default Value: 0000 0000h**

Bit	Attribute	Default	Description	Mnemonic
31:0	RO	0	**Wall Clock Counter Alias**	**Wcounter**

HDAC Stream Descriptor Link Position in Buffer Alias (HDAC-MMIO) **Default Value: 0000 0000h**

Offset Address 2087-2084h: Input Stream 0
Offset Address 20A7-20A4h: Input Stream 1
Offset Address 20C7-20C4h: Input Stream 2
Offset Address 20E7-20E4h: Input Stream 3
Offset Address 2107-2104h: Output Stream 0
Offset Address 2127-2124h: Output Stream 1
Offset Address 2147-2144h: Output Stream 2
Offset Address 2167-2164h: Output Stream 3

Bit	Attribute	Default	Description	Mnemonic
31:0	RO	0	**Link Position in Buffer Alias** An alias of the link position in buffer register for each stream descriptor.	**LPIB**