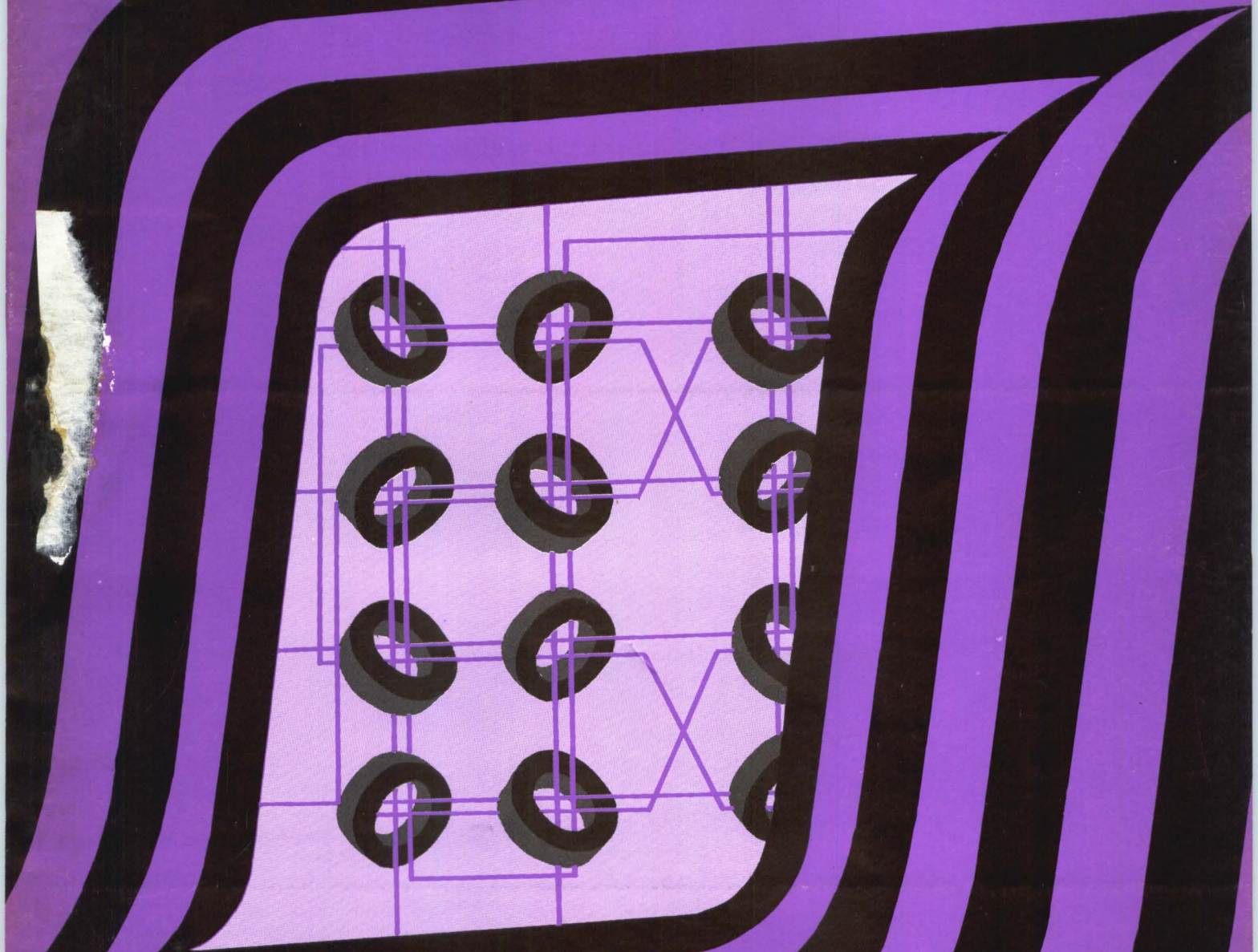
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS DECEMBER 1968



in this issue

The new Varian Data dual-environment 520/i.

Tag this one to upset the present balance of power and price.

We've hung some other powerful attractions on this system-oriented computer besides that price tag. Two complete sets of hardware registers, including index registers.

They allow the 520/i to run dual programs. A single 1.5 μs instruction transfers control between programs, or between processing and I/O programs. Data may be manipulated in multiple 8-bit bytes—it'll do arithmetic in 8, 16, 24 or 32-bit lengths within the same program. Program precision is changeable any time.

Hardware includes two 32-bit accumulators, two 16-bit index registers, two program counters, and two overflow registers. Eleven interrupt lines with four hardware priority levels. Expandable 4K to 32K 1.5 μs memory. IC construction. 50 basic instructions. Interface modules for I/O devices. Proven software. Current delivery: 60 days.

If you're comparing price/performance ratios, 520/i is the new power to be reckoned with—write for your brochure.

varian data machines

a varian subsidiary
2722 Michelson Drive/Irvine/California 92664
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SALES OFFICES: U.S., Santa Monica and San Francisco, California; Vernon and Westport, Connecticut; Chicago, Illinois; Houston, Texas; Fort Washington, Pennsylvania; Washington, D.C.; Waltham, Massachusetts; Fort Lauderdale, Florida. INTERNATIONAL: Australia, France, Germany, Sweden, Switzerland, United Kingdom, Ireland and Belgium.

CIRCLE NO. 1 ON INQUIRY CARD

Fact:

We support our drum memories

It's all done with paper. Start with the proposal . . . a clear, complete, and factual summary of all performance figures . . . all interface connections and levels . . . all timing data . . . all physical dimensions . . . all you need to design and build a complete interface. Continue with an Installation and Operation Manual, with all you need to install and operate your drum. Behind that, there's a Service and Maintenance Manual, with detailed schematics, theory, trouble-shooting, adjustments, repairs, tool lists, diagrams, photos, test program outline . . . all the facts and procedures you'll ever want. Behind these you'll find a comprehensive training course for your personnel. And behind that, there's another piece of paper—VRC's total warranty for one year on drum and electronics . . . backed by a staff of trained field engineers, who fly to your site for installations or emergencies.

It's surprising, the support you can get from pieces of paper. Try the first piece . . . our general drum memory brochure, DB-6808.

Computers are known by their MEMORIES...

...so is **Vermont Research CORPORATION**

DRUM MEMORIES • SYSTEMS • DISK PACKS

Box 20a, Precision Park, North Springfield, Vermont 05150 • Telephone 802/886-2256 • TWX 710-363-6533

When it comes to engineering opportunities (and the good life, North Country style), the place to come is Vermont Research Corporation. For specific information, contact: RICHARD A. STOVER, Vice President-Engineering.

CIRCLE NO. 2 ON INQUIRY CARD

This is the house that Jack built.

Inside is a single micro-logic circuit card from Control Logic. It's all the cards Jack needs. Only one, because a Control Logic card is compatible and versatile with capability in process control systems, and versatility in automatic wire-wrap assemblies and component combinations. And it fits his design easily. But, you may need more than one micro-logic circuit card from Control Logic. And your design may not be as simple as Jack's. No matter. Control Logic's packaging capability can adapt to your design. With its card frames, racks, cages, and power drawers, Control Logic can fit as many micro-logic circuit cards as you need . . . Into the house that you built!
To find out how, call or write:

CONTROL LOGIC, INC. 3 Strathmore Road
Natick, Massachusetts 01760 / Tel: (617) 235-1865

DECEMBER 1968 • VOLUME 7 • NUMBER 12

COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

Editorial & Executive Offices
Prof. Bldg., Baker Ave.,
W. Concord, Mass. 01781
Tel. 369-6660

FEATURES

DEPARTMENTS

If you're building any computer except a Computer, you need CTμL.

CTμL integrated circuits will give you more speed for less money than any other ICs. They're perfect for process control systems, test instrumentation, central processing units, computer peripheral equipment—just about anything short of an airborne computer.

Keep it in the family.

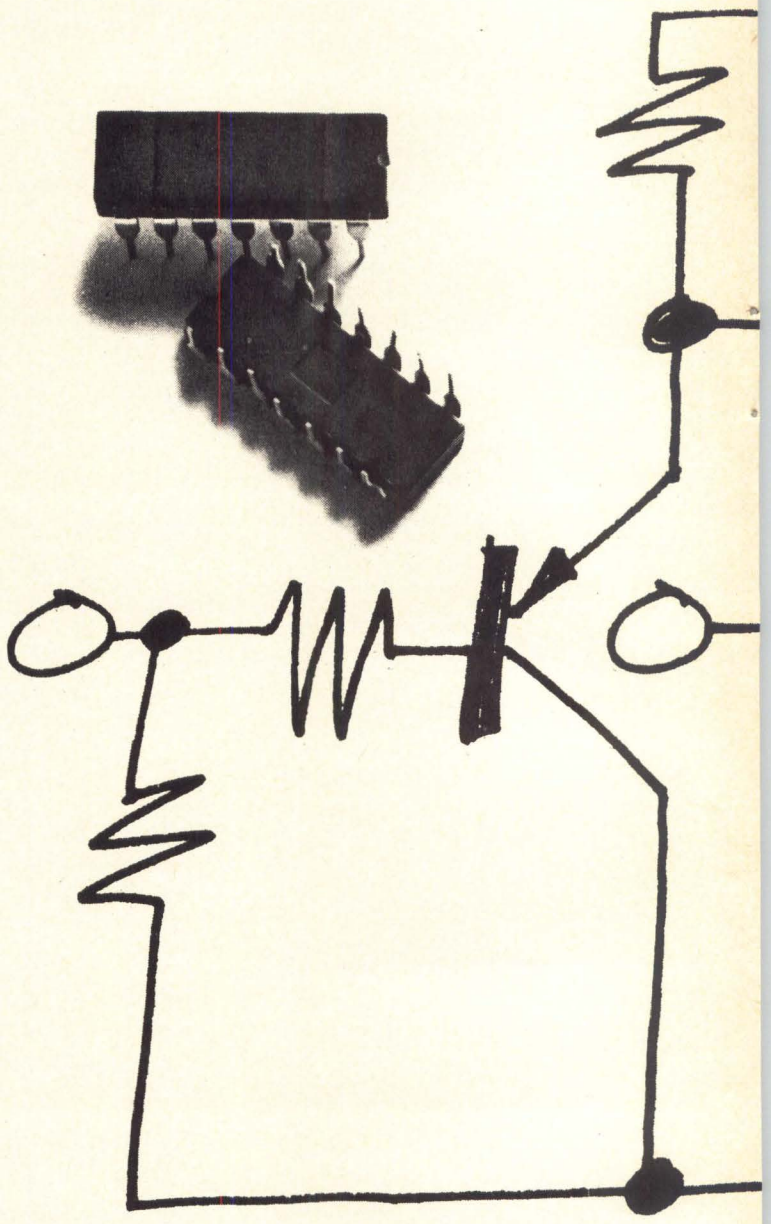
You can build a complete digital logic system with Fairchild's family of CTμL devices. We have gates, flip-flops, inverters and memory circuits. A dozen different devices that make a computer easy to package. And, you'll need only about 80 percent as many packages as required with TTL.

You get out of it what you put into it.

The key CTμL characteristic is non-saturating logic. That means you get fast gate propagation delay (typically 3nsec) with slow rise and fall times (typically 6nsec). So, there's no need for transmission lines or complex packaging. You can build an entire computer with normal two-sided circuit boards. Also, CTμL can handle signal swings as large as 3V. It also provides typical noise immunity of 500mV.

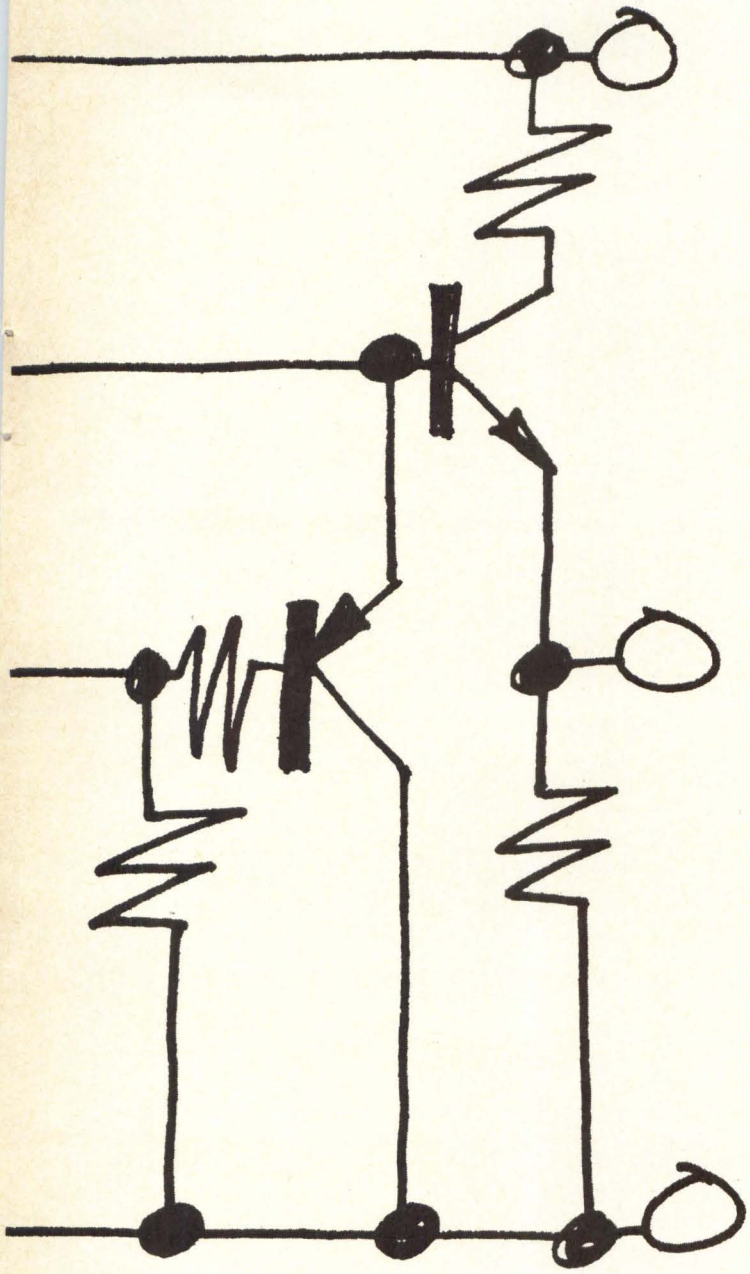
What we'll do for an encore:

MSI CTμL will be out before the year ends. CTμL-II will be out even sooner, offering improvements like gate propagation delay of 1.5nsec. (typical, loaded) and a buffer and



The world's largest manufacturer

inverter with propagation delays of 5nsec, compared with 12nsec in standard CTμL. And, the new MSI and CTμL-II circuitry will interface beautifully with all these standard CTμL devices:



Device	Price (100-999)
9952 Dual NOR Gate	$1.25
9953 Triple AND Gate	1.25
9954 Dual Four-input AND Gate	1.25
9955 Eight-input AND Gate	1.25
9956 Dual Buffer	1.25
9957 Dual-rank Flip-flop	2.00
9964 Dual Three-input and Single-input AND Gates	1.25
9965 Quad Single-input AND Gate	1.25
9966 Quad Two-input AND Gates, one pair with OR-tie	1.25
9967 JK Flip-flop	2.00
9968 Dual Latch	2.00
9971 Quad Two-input AND Gates with OR-tied pairs	1.25
9972 Quad Two-input AND Gates, one pair with OR-tie	1.25

If you want CTμL-II in sample quantities, call Fairchild. If you want standard CTμL in production quantities, call a Fairchild distributor. He has everything you need to build any computer.
Even a Computer.

FAIRCHILD
SEMICONDUCTOR

Fairchild Semiconductor/A Division of Fairchild Camera and Instrument Corporation/313 Fairchild Drive, Mountain View, Calif. 94040 (415) 962-5011/TWX: 910-379-6435

# of LSI admits there's another way:

CIRCLE NO. 4 ON INQUIRY CARD

Mag tape too expensive?
Punched tape too slow?
Your small computer deserves PEC data power!

High Speed—Low Price

Seems a shame to shackle that fast new computer of yours with slow, maintenance-prone punched tape. Yet digital magnetic tape recorders are so expensive.

Not now, they aren't.

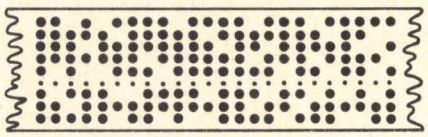
PEC can give your small computer real write/read data power. 10 KHz data transfer rates for under $3,000. 20 KHz transfer rates from $5,000. (Less than $4,000 in quantities).

Discriminating computer users are demanding higher input/output performance on even the smallest machines.

That's why more and more major computer manufacturers are offering PEC digital magnetic tape recorders as standard equipment.

Insist on low cost-high performance PEC data power for your computer.

Compare With Punched Tape

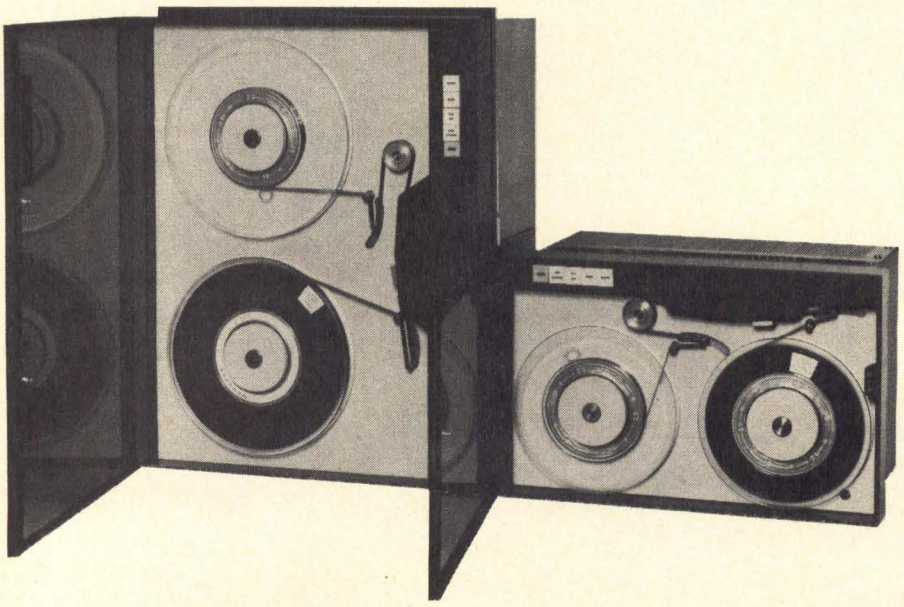


You can store ten characters on an inch of punched tape. You can store up to 800 characters on an inch of magnetic tape. That's 80 times more data per inch!

What about data transfer rates? A paper tape perforator plods along at 150 characters a second. Pretty slow for today's fast computers.

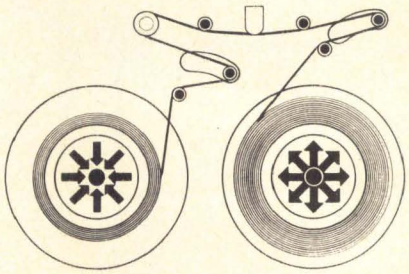
PEC digital magnetic tape recorders zip data in and out at speeds to 25 ips. Data transfer rates up to 20 KHz. That's 133 times faster than punched tape.

PEC data power costs just a little more than punched tape. Yet look at the tremendous increase in storage capacity and data transfer rates you get.



Compare With Other Mag Tape Models

PEC digital magnetic tape recorders use an elegantly simple single capstan velocity servo system. Pinch roller, a major source of skew and tape wear, is eliminated.



PEC recorders cost half as much as competitive makes, yet perform even better.

IBM compatible? You bet. Including the precise requirements for System/360, 9 channel, 800 bpi operation.

Choose the speed you want from 4 to 25 ips, at 800, 556, or 200 bpi. 7 track dual density available too. And up to 4 PEC recorders can operate from a single computer.

Select the data capacity, transfer rate, rack height and price from 3 distinct models.

Three Reel Sizes

Reel Size	Max. Transfer Rates	Tape capacity
7 inch	10 KHz	600 feet
8½ inch	20 KHz	1200 feet
10½ inch	20 KHz	2400 feet

PEC also makes synchronous write-only and read-only recorders. A complete line of incremental models too. Perfect for data acquisition systems, off-line plotters, line printers, and data terminals. Perfect for just about any input or output requirement, for that matter.

Write or phone today for our 8 page brochure.

PEC

PERIPHERAL EQUIPMENT CORPORATION
9551 Irondale Avenue ■ Chatsworth, California 91311 ■ (213) 882-0030 ■ TWX (910) 494-2093

CIRCLE NO. 5 ON INQUIRY CARD

Is your computer ready for memory expansion?

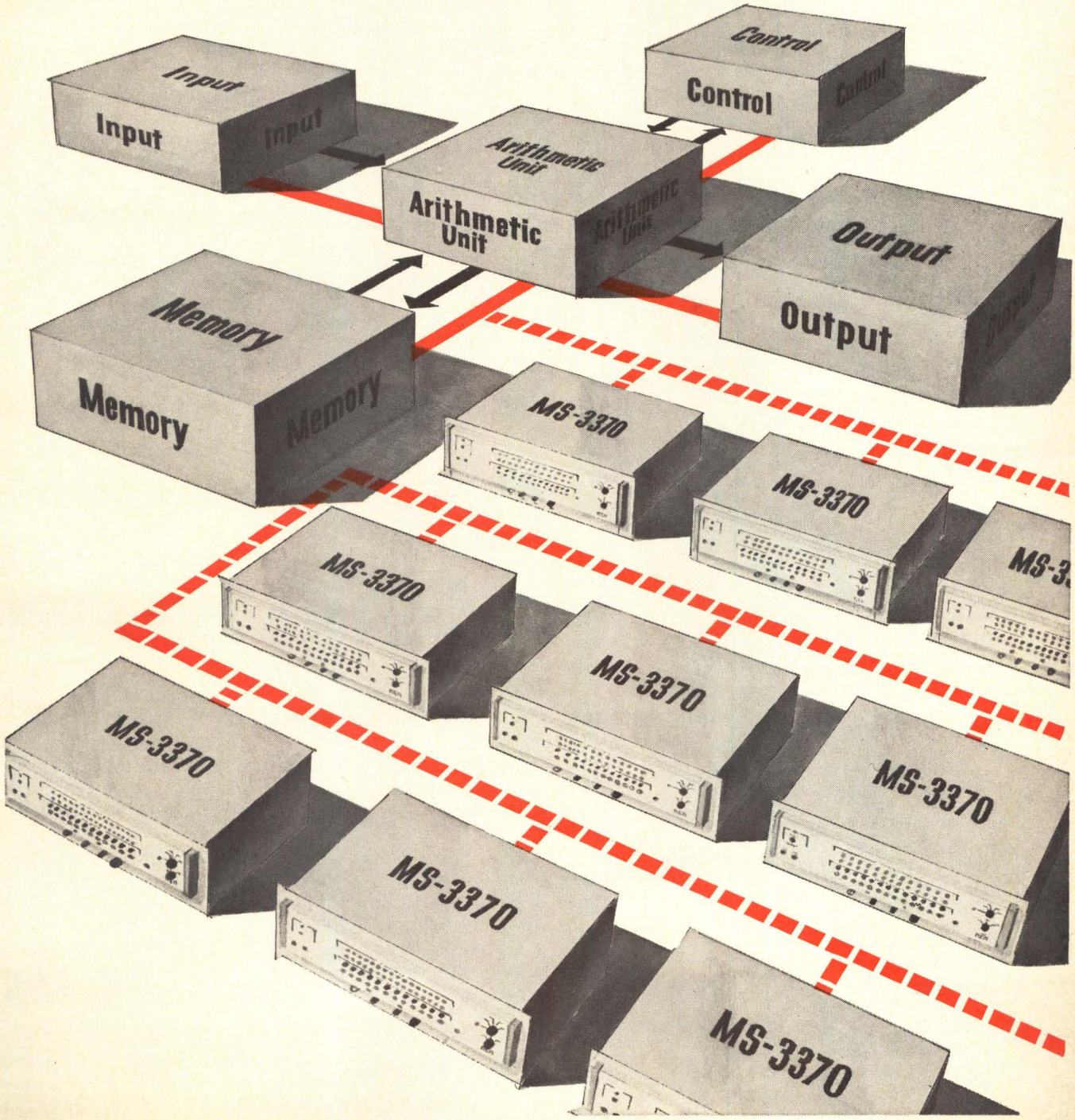
You would be surprised how RCA's "plug-in" compatibility makes it easy and inexpensive to add more memory capacity.

Experience shows that every computer soon runs out of memory. If your computer has reached this point, RCA Memory Products Division can provide compatible high speed memory systems for significantly less than you would expect to pay.

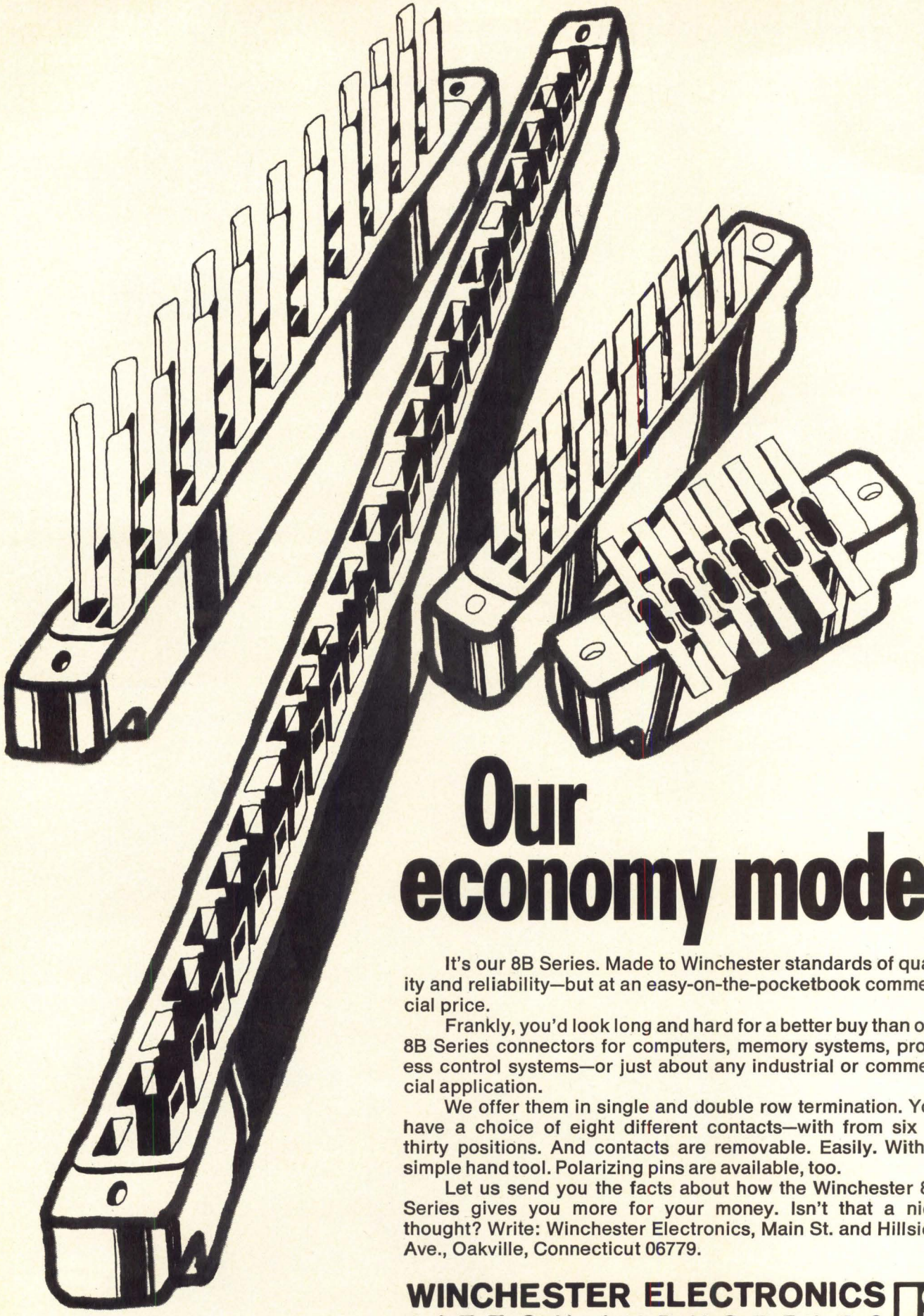
RCA offers standard off-the-shelf memories with cycle time as fast as 750 nanoseconds and access time of 290 nanoseconds, capacities of 4K x 4 to 32K x 72. We'll quickly work out the "plug-in" compatibility for you, including voltage levels, timing and hardware. Simply let us know what your interfacing requirements are, and we'll take it from there. Or, we'll assist you, if you wish to do the job yourself.

An RCA Field Representative will be glad to discuss your needs. Or, call or write Marketing Department (617-444-7200, Ext. 233) RCA Memory Products Div., 150 "A" St., Needham Hts., Mass. 02194.

RCA



CIRCLE NO. 6 ON INQUIRY CARD



Our economy model

It's our 8B Series. Made to Winchester standards of quality and reliability—but at an easy-on-the-pocketbook commercial price.

Frankly, you'd look long and hard for a better buy than our 8B Series connectors for computers, memory systems, process control systems—or just about any industrial or commercial application.

We offer them in single and double row termination. You have a choice of eight different contacts—with from six to thirty positions. And contacts are removable. Easily. With a simple hand tool. Polarizing pins are available, too.

Let us send you the facts about how the Winchester 8B Series gives you more for your money. Isn't that a nice thought? Write: Winchester Electronics, Main St. and Hillside Ave., Oakville, Connecticut 06779.

WINCHESTER ELECTRONICS
LITTON INDUSTRIES

CIRCLE NO. 7 ON INQUIRY CARD

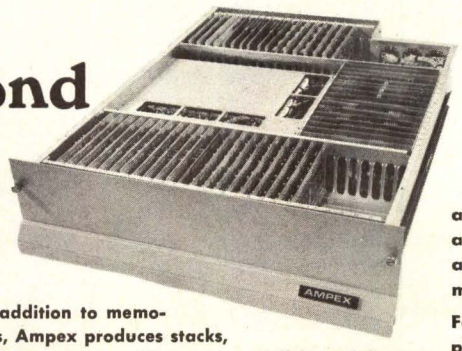
Erma is gone, but her memory lives on.

Erma's memory is alive and processing traveler's checks in San Jose, California. We built the core memories for Bank of America's ERMA computers back in 1959. They contained 80-mil cores providing a cycle time of 32 microseconds and an access time of 12 microseconds. Capacity was 4000 words (28 bits/word). One of those memories is still in use. It's slow by today's standards but perfectly suited for its job.

AMPEX

THE ONE COMPANY THAT CAN REMINISCE ABOUT OLD MEMORIES.

Meet our newest: The 500 nanosecond 25DM-500.



The new Ampex 25DM-500 has a full cycle time of 500 nanoseconds and an access time of 300 nanoseconds. The basic memory module is 8K x 36 bits. It uses 18-mil cores in a 3-wire 2.5D configuration. Maximum capacity is 32K x 72 bits. This fast new memory is the latest in our wide line of core memories. They include small, inexpensive 1.5 microsecond memories (RF-1), the 1.0 microsecond RF-4, the fast access (350-nanosecond) 900 nanosecond RG memory, the 3-wire 3D 750 nanosecond 3DM750, and the new 500 nanosecond 25DM-500.

In addition to memories, Ampex produces stacks, arrays and cores. We supply a full line of ferrite cores from 18 to 80-mils O.D., including a line of standard cores for wide temperature requirements. The memory designer will find help in our design assistance and our catalog of commercial and military arrays. Stacks are available in 2.5D and 3D (3 or 4 wire) configurations; 18-, 22-, 30- and 50-mil core sizes; regular or ruggedized to meet MIL-E-16400 or MIL-E-5400.

For full information about any of our memory products, circle the reader card number or write Ampex Corporation, 401 Broadway, Redwood City, California 94063.

CIRCLE NO. 8 ON INQUIRY CARD

Standardizing a military memory has its ups and downs.

The ups:

Apollo
Airborne navigation computer
X-15 computer
Missile re-entry
Supersonic aircraft
Side-looking radar

The downs:

Counter-mortar radar
Counter-measures computer
Deep-submergence vehicle
Underground bomb tests
Ground-mobile marine radar

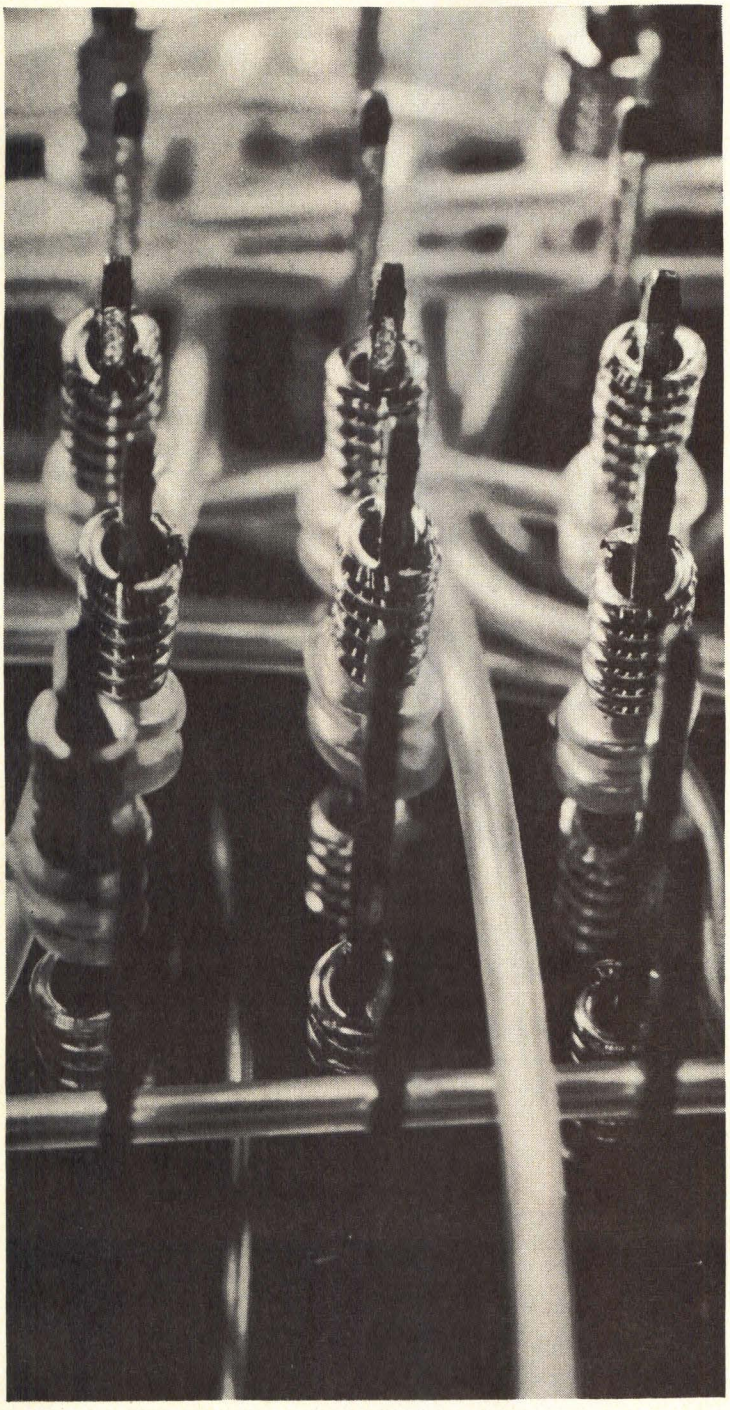
Let's face it—there's no way to standardize on a single configuration for a product that goes into as many diverse applications as our military memories do, so we've built two types that fit a wide variety of requirements. Maybe yours? Our SEMS-5 has a cycle time of 2 μsec, storage capacity to 131,062 bits, and meets all the specs to qualify it as an airborne system, but you'll find it in ground-based and oceanographic applications. Our SEMS-7 has a cycle time of 2 μsec, storage capacity to 327,680 bits and was designed for ground-based applications, but it's also designed into a supersonic aircraft.

Delivery is fast for almost any application, and to help you choose the right configuration, we're offering a paper entitled "How to Specify a Special-Purpose Memory" as well as product literature. Just ask.

EM electronic memories
12621 Chadron Ave., Hawthorne, California 90250 • (213) 772-5201

CIRCLE NO 9 ON INQUIRY CARD

We know somebody with connections.



So we told them about wire insulation made of Kynar®.

That was five years ago.

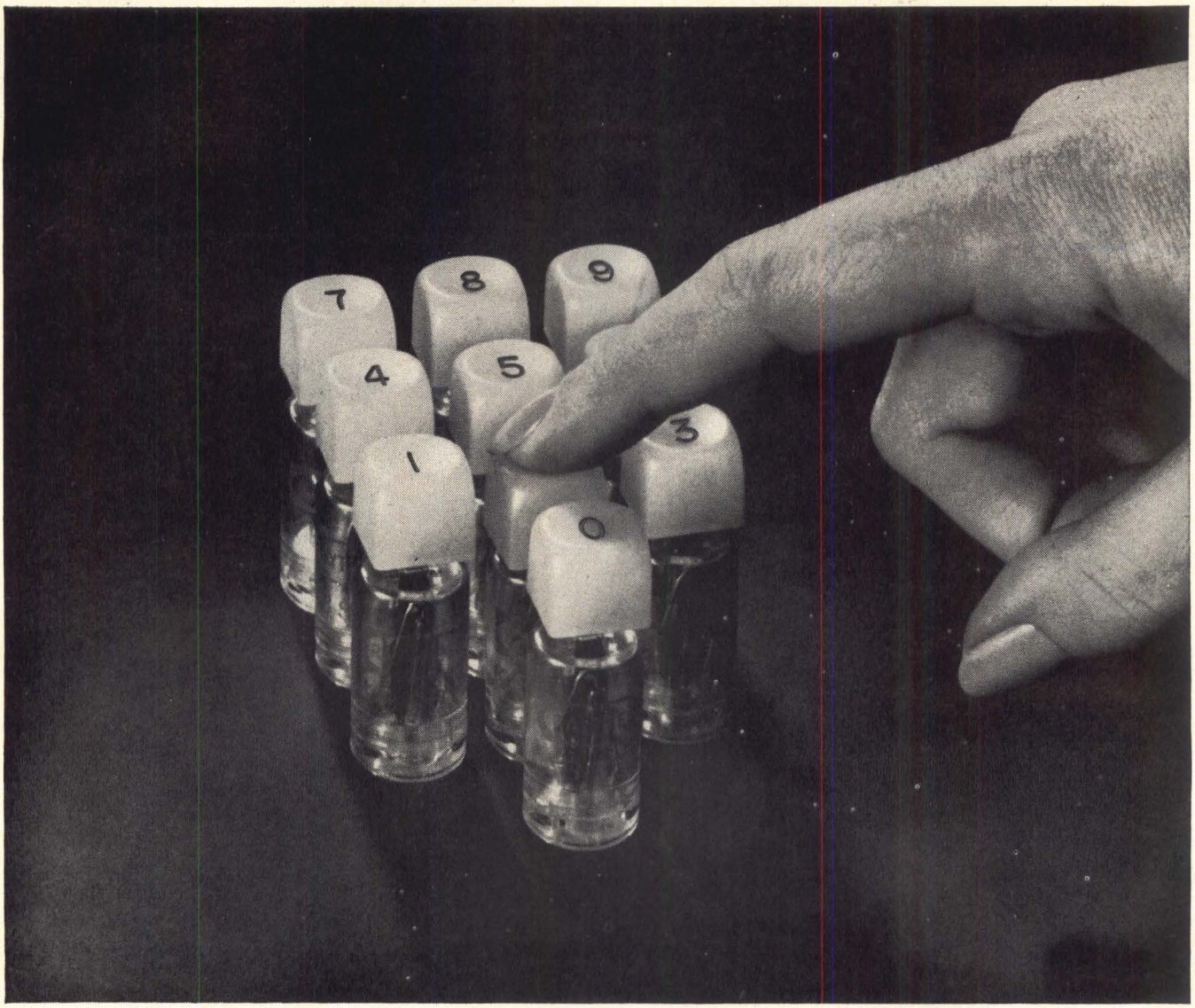
Burroughs Corporation's computer plant in Pasadena runs 200,000 feet of wire a week, makes 120 terminations per minute. With that many connections, at that speed, the right kind of insulation is important—insulation that's not only tough, but absolutely reliable. That's why Burroughs has used wire insulated with Kynar for back planes since 1963.

Why Kynar? A Burroughs engineer answers: "It works better than many others we've tried . . . so why argue with success?" Kynar works for some good solid reasons. It has twice the cut-through resistance of other common fluoroplastics and virtually eliminates cold-flow problems. Kynar runs economically in automatic wire-wrap equipment . . . it feeds, cuts, and strips smoothly. It's unaffected by cleaning solvents, and it won't degrade with age.

Tough arguments? You bet. Tough material . . . that's Kynar. So take a tip from experience. Switch to wire insulated with Kynar. It's available from leading wire manufacturers. For additional information contact: Plastics Department, Pennsalt Chemicals Corporation, 3 Penn Center, Philadelphia, Pa. 19102.

Kynar...the fluoroplastic that's tough! PENNSALT®

CIRCLE NO. 10 ON INQUIRY CARD



These new keyboard switches feature unusually precise action and low-cost mounting. See for yourself—write for samples.

These elegantly styled key switches —designed for handling switching at logic levels—are especially suitable for computers, learning and business machines, and advanced control equipment.

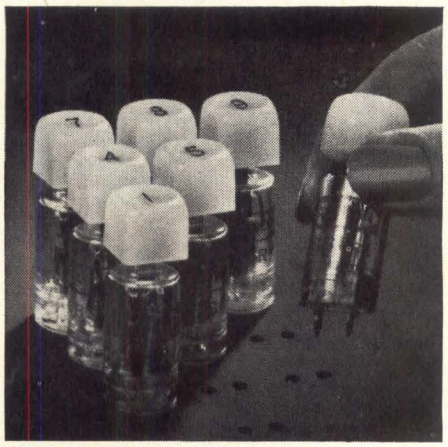
Designed by Raytheon, they have a featherlight touch that is precise and reliable. Just a 3-oz. touch activates the switch. Because of the unique design, this action can be repeated more than 10 million times. Yet the switches cost less than $1 in production quantities.

A wide range of standard- and custom-cap shapes, sizes, colors, and alphanumerics are available. Characters can be hot stamped, engraved or molded through. Bases can be flat or with 10° slope. Characters can be illuminated by backlighting. All switches are made of high-quality materials: stain-resistant caps; polycarbonate body parts; stainless steel springs; beryllium and stainless steel contacts. They are available in single- and double-level wipe-action types, and in dry-reed, hermetically sealed single- and double-level types.

For free samples, write on your letterhead describing your application to: *Raytheon Company, Industrial Components Operation, Dept. 2351-CD, Quincy, Massachusetts 02169.*

RAYTHEON

CIRCLE NO. 11 ON INQUIRY CARD



Simple, low-cost mounting. Raytheon switches plug into .125″ PC board. Contact pins snap in, firmly lock switch in place for soldering. This permits you to use flow soldering techniques—cut keyboard assembly time and costs.

Flexibility.

And we'll give you a good reason to buy our flexible circuits over anyone else's:

We make them with the same kind of precision our regular printed circuits are known for.

We can produce them in quantity to the most stringent specifications—single or multilayer.

We're probably the flexible circuit source you've been looking for.

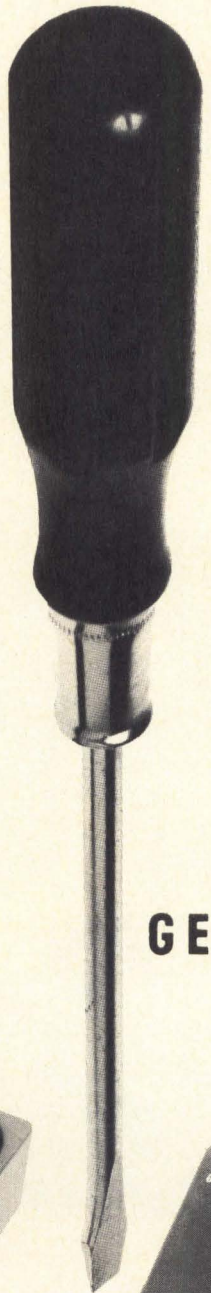
For your copy of "A Designer's Guide to Flexible Circuits," write to Printed Circuits, Lockheed Electronics Company, Data Products Division, 6201 E. Randolph St., Los Angeles, California 90022.

We've added a new wrinkle to our printed circuits.

LOCKHEED ELECTRONICS COMPANY
A Division of
Lockheed Aircraft Corporation

CIRCLE NO. 12 ON INQUIRY CARD

with a screw driver and 15 minutes... you can install a General Electric acoustic data set



Under the newly-filed tariffs, the use of customer owned acoustically-coupled data sets is authorized for use on all telephone company, public switched networks. If the economy of owning your own data transmission equipment is part of your plans for the new year, investigate the many reasons why the General Electric TDM-114 or TDM-115 Series can better satisfy your requirements.

Reliability? Eleven years (100,000 hours) Mean Time Between Failure.

Installation? A screw driver and 15 minutes does it. No adjustment or tune-up required.

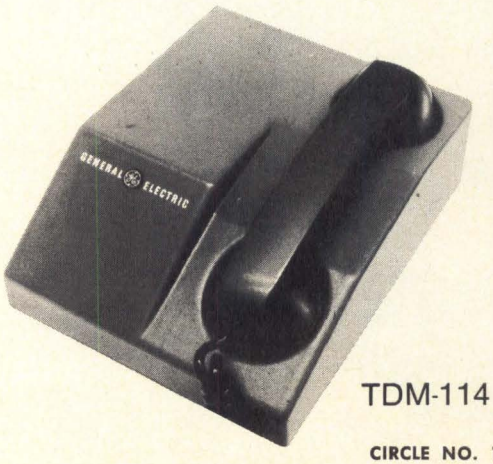
Operation? Fully automatic.

Service? (if ever required) over 750 service facilities located throughout the United States.

Compatibility? Works with Teletype®, Kleinschmidt, Friden, GE, IBM, and other popular serial binary terminals at speeds up to 30 ASCII characters per second.

See for yourself how GE acoustic data sets are performance-proven to better satisfy your data transmission requirements. Complete specifications are yours for the asking. Write to Section 472-07, Fixed Point Communication, Communication Products Department, Lynchburg, Virginia 24502. In Canada, write to Canadian General Electric Company, Ltd., Information Systems and Defence Products Department, 830 Lansdowne Avenue, Toronto 4, Ontario.

GENERAL ELECTRIC



TDM-114

TDM-115

CIRCLE NO. 13 ON INQUIRY CARD

LOW COST, HIGH RELIABILITY... WITH MDS LOW-SPEED LINE PRINTERS

MDS 4320 LOW-SPEED
BUFFERED LINE PRINTER

MDS Series 4000 Low-Speed Line Printers, with print speeds up to 300 lines per minute, are especially designed for business or scientific applications where high speed is not needed.

Low cost, reliability and performance are hallmarks of the MDS Series 4000 Line Printers. Designed for use with the newest compact data processing systems, the Series 4000 reflects the combined skills and engineering talent of MDS and a subsidiary, long recognized as a leading independent producer of highly dependable line printers.

MDS Series 4000 features a rotating drum, on-the-fly, impact printer with long life reliability "built-in." Available in buffered (4320) and unbuffered (4300) console models; or as the MDS 4013 Printer Mechanism unit for integration with your own system.

The 4320 has a ready strobe serial buffer and operates in three modes . . . List Mode . . . Line Edit Mode . . . Edit Mode.

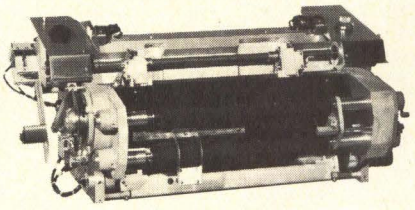
A few of the MDS 4013 features:

- Print hammers use MDS Penetration Control; energy and instant of impact are adjustable to very fine tolerances.
- Tape Control Vertical Format Unit . . . provides 12 channels and 6 or 8 lines per inch.
- Up to six copies can be printed.
- Pin-Type chain drive shuttle paper feeding.
- New Fibre Optics System . . . only 3 light sources.

MDS 4320 and 4300 Console Units incorporate the 4013 print mechanism, power supply, power drive circuit, and I/O interface electronics.

Ask for: Folder-file on MDS Series 4000 Low-Speed Line Printers.

FOR MORE—MEET YOUR MAN FROM MDS



MDS 4013 Low-Speed Line Printer
Mechanism gives long-term, reliable
service—at economical cost.

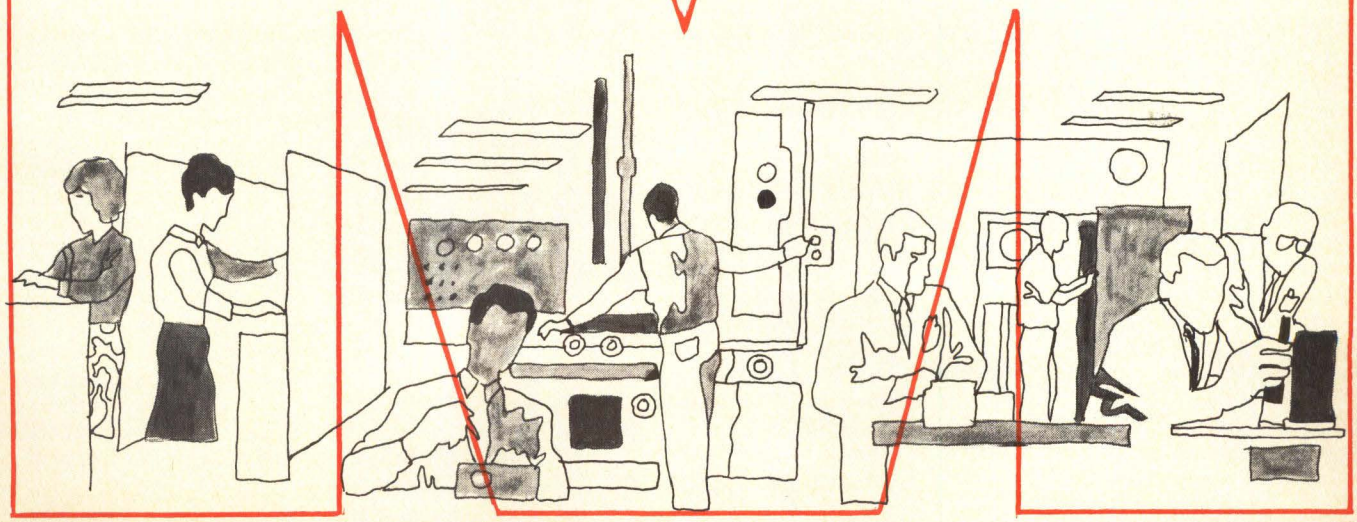
MOHAWK DATA SCIENCES CORPORATION MDS®

OEM MARKETING

305 WEST GRAND AVENUE • MONTVALE, N. J. 07645
Telephone 201/391-7000

Every MDS office is an OEM Marketing office

DIGITAL STRIP PRINTERS • BUFFERED TAPE UNITS
HIGH-SPEED AND LOW-SPEED LINE PRINTERS
CARD PUNCHES AND READERS
PAPER TAPE PUNCHES AND READERS



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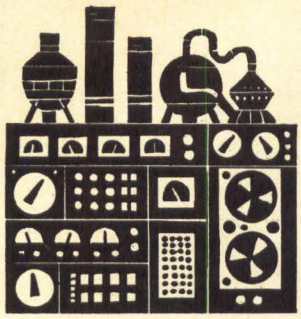

INDUSTRY NEWS

HP ENTERS COMPUTERIZED-CUSTOM TEST SYSTEM BUSINESS – The first computer-controlled custom test system from Hewlett-Packard's newly-formed Systems Division has been delivered to Magnavox Corporation, Fort Wayne, Indiana.

Marking the Palo Alto based instrument company's entry into the custom electronic test systems business, the system will automatically check out thick-film receiver circuits for new Magnavox radios.

The company said the new division has four more computerized systems and about fifty other custom instrument sets currently in its backlog. "Our purpose in going into this business," Division Manager Richard J. Reynolds said, "was to solve the customer problems of getting new computer-controlled test systems working fast, at reasonable cost, with single-source responsibility for the interface between the computer and test instruments. "We felt we could offer fast turn-around and economy by using a building-block approach to the hardware with standard interface cards.

The modular approach, HP explained, began about two years ago when the company embarked on a program to develop new digital computers with ability to interface to many instruments with plug-in cards. New programmable building-block instruments were also developed. The new division will also produce a line of standard computerized automatic test systems with a wide range of options for even faster delivery.

COMPUTER ROOM PACKAGE AVAILABLE FROM A SINGLE SOURCE – A pre-engineered packaged computer room that includes everything but the computer is now available from a single source. Design of the room, and manufacture and installation of all components—raised-floor system, partitions, ceiling, air conditioning, lighting, and even light switches and cover plates—can be included.

The complete computer room package has the design flexibility to be custom engineered in modules to fit the individual needs of the user. From the initial design study and survey of customer facilities to the final on-site assembly, each component is integrated to overcome problems presented by either the computer system itself or the customer's existing facilities. This component tailoring results in accumulated savings for the user. Moreover, an entire room can be remodeled, enlarged, or totally relocated without scrapping components.

Modular design and rigid quality control standards insure the proper matching of all components to provide reliable performance. Components are shipped for fast field assembly with minimum disruption of the customer's operations.

Prebuilt packages for installation by the customer or local contractors are also available. The completed room is guaranteed if installation instructions are followed. Components are completely finished at the factory for immediate installation with little on-site cutting and fitting required. For more information write Westinghouse Architectural Systems Department, 4300 36th Street, Grand Rapids, Mich. 49508.

PHOTO-OPTICS LINKED TO COMPUTER TECHNOLOGY FOR PRECISION MEASUREMENTS – An experimental device for measuring optical microdensity of an image to obtain positional accuracy has been developed by IBM's Boulder, Colo. Product Test Lab. The device links the photo-optical principles of the scanning registration densitometer to the electronic computer.

The system called REGI-B enables precise, accurate measurement of the positions of regularly spaced rows of microminiature images to insure proper registration on a master specimen; for example, a mask used to photo-etch integrated circuit chips. Each image must be positioned precisely to assure reliability of the circuits.

Positional accuracy is difficult to check optically because of variations in density at the edge of an image. REGI-B, however, assures that each image is measured at precisely the same edge point. By recording the distances between these specified points, it determines if an inscribed line is out of registration by as little as one ten-thousandth of an inch.

Optical density is measured by placing a photographic "step guide" on the light table ahead of the specimen. By reflection or direct transmission, a Kohler light source is passed through the specimen to a scanning microscope, which is controlled in the X axis by a variable speed motor and in the Y axis by a stepping motor. The light beam is converted to electrical pulses by a photomultiplier. These pulses, representing optical density, trigger the recording mechanism.

Density measurements are recorded on a strip chart or X-Y recorder. Image registration data are placed on digital tape for statistical analysis on an IBM System/360 computer.

When the master artwork is generated, small holes are punched near its edge at specified intervals. During data analysis, the computer reads the distance between the holes and automatically compensates for any stretch or shrinkage errors.

The tradition breakers.

She's not the only one . . . five years ago TI advanced the state of the magnetic circuit breaker art with a smaller, lighter, simpler mechanism. It went over big. More recently, new TI magnetic circuit breakers show similar design breakthroughs. A 100-amp rating built into a 50-amp frame. A 50-amp rating squeezed into a 25% smaller package. A choice of 20-amp push-button and toggle twins that meet military specifications. A unique magnetic/hydraulic time delay feature. And so on. These and other breaks with tradition make TI the logical choice to solve your circuit protection problems–quickly, economically, precisely. Write TI Control Products Div., Attleboro, Mass. 02703, or tel. (617) 222-2800 Ext. 368

TEXAS INSTRUMENTS
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INDUSTRY NEWS

HONEYWELL ADDS NEW DATA DISPLAY TERMINAL FAMILY – A new family of advanced desk-top terminals for remote on-line entry, retrieval and display of computer information will be marketed by Honeywell's Electronic Data Processing Division, Wellesley Hills, Mass.

The Series 2300 family of six Visual Information Projection (VIP) terminals will replace the current Honeywell VIP line manufactured by the Bunker-Ramco Corp. of Stamford, Conn. The Series 2300 also will be built to Honeywell specifications by Bunker-Ramo.

This series of VIPs may be used in such diverse computer applications as manufacturing production control, marketing data retrieval, library indexing, hospital patient records, stock and commodity market quotations, airline passenger or freight information and other similar management information systems, according to Eric N. Grubinger, group product manager of communications products at Honeywell EDP.

TAPED LECTURE COURSE COVERS BASICS OF PROCESS COMPUTERS – General Electric's Process Computer Department, Phoenix, Ariz. has announced the availability of a unique audio-taped course covering the basics of process computers and how they control industrial processes.

Requiring about four hours, the course consists of a taped lecture with a workbook of more than 100 pages which illustrates the material presented on tape. Quizzes are spotted throughout the book to assure the student understands each segment before he continues to the next.

The course describes the basic components common to any computer (EDP *or* process control), and through a simple analogy, the way they work together to achieve fast, consistent results. The communication devices which enable the computer to "talk" to the process being controlled, and the "languages" it uses in doing so, are also covered, as are the instruments which measure and control process performance.

The course was developed to acquaint plant management, instrumentation and process engineers, operators and others with the fundamentals of process control computers. The price for one complete course, audio tape and workbook pages packaged in an attractive binder, is $125.

SDS OFFERS ON-LINE CIRCUIT DESIGN-ANALYSIS SOFTWARE – Scientific Data Systems Time-Sharing Services is now offering an on-line circuit design-analysis package. This programming system, called CIRC, is offered exclusively to users of SDS Time-Sharing Services.

The system is a general-purpose program, conversationally structured to allow man-machine interaction in a computer-aided design process. CIRC allows a circuit designer, working at a remote input/output teletypewriter terminal in his own office, to analyze proposed design approaches while interacting conversationally with the computer, and thus to arrive at an optimum design in a very short time.

The CIRC-AC program handles both passive and active components. A transistor model, stored within the program, implements a sophisticated two-pole modeling technique that includes the often overlooked "excess phase" characteristic of transistors. This program allows tentative ac circuit designs to be evaluated over an automatically scanned frequency range. It also performs open-loop analyses with proper loading being handled automatically.

PLATED WIRE PRODUCTION CAPABILITY – Electronic Memories, Inc., Hawthorne, Calif., has developed and is producing plated wire and plated wire arrays in limited quantity. The wire and array capability was developed during the past two years under a company-funded research program headed by Dr. Judea Pearl.

The Core Division has been renamed the Magnetic Materials Division to reflect the company's broadened capability in the memory element field.

Richard J. Dadamo, V.P. and G.M. of the Magnetic Materials Division, pointed out that while EM will produce and market plated wire eventually through the system's level, the company will continue to promote and expand its ferrite core memory activity.

The Memory Components Division, presently producing enough plated wire to meet several customers' needs, expects to be in high volume production of plated wire products by mid-year 1969.

The initial plated wire memory plane offered by the company has 64 words of 36 bits and is offered in either bi-polar or uni-polar modes, depending on customer need. The plane's cycle time is 200 nanoseconds, and may be operated over a temperature range of −50° to +100°C.

NEW FIRM TO MARKET PERIPHERAL EQUIPMENT–Tycore Inc. has recently been formed for the design and manufacture of data tape systems and other peripheral computer equipment. The company has completed design and manufacture of two prototype data tape systems. Designated the Series 7500 for 7 channel tape and the Series 9500 for 9 channel tape, both are keyboard-to-tape systems and are aimed at replacing present equipment in the keyboard-to-card punch market.

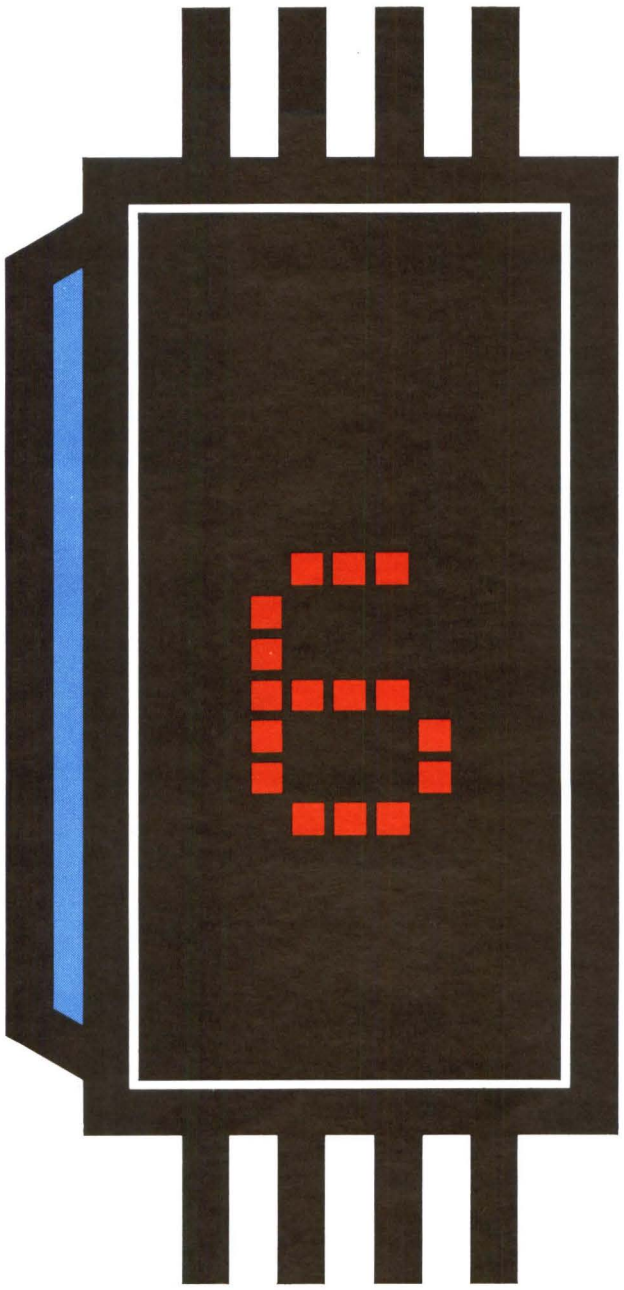
The company occupies 15,000 square feet in a newly completed building at 80 Turnpike Road, Chelmsford, Mass., and is planning to expand into an adjacent 15,000 square feet as soon as production builds up. The first production data tape systems will be ready for shipment in early spring.

CALL FOR PAPERS – The 1969 IEEE Computer Group Conference will be held at the Leamington Hotel, Minneapolis, Minnesota, Tuesday through Thursday, June 17-19, 1969. The purpose of this Conference is to report and explore recent, original developments in "Today's World of Real Time Systems."

Subjects of interest cover the spectrum of real time considerations and include real time systems for process control, message switching, inventory control, time sharing, command and control, biomedical computing. Papers are solicited describing new developments in software, languages, system organization and interface design including peripheral equipment, special purpose systems, system models and analysis, and hardware.

Potential participants are requested to submit for consideration by the Conference Program Committee a 50 word abstract suitable for publication in the *Computer Group News* and a 1000 word illustrated digest suitable for publication in the Conference Digest. The phone number and complete mailing address of the senior author should be identified for possible later questions and revisions. Four copies of the abstract and digest should be submitted by January 10, 1969. Authors will be notified of the Program Committee's decision by March 1, 1969.

All material should be sent to: Donald L. Epley, Technical Program Chairman, 1969 IEEE Computer Group Conference, Department of Electrical Engineering, University of Iowa, Iowa City, Iowa 52240.



Surprise package
(1″ x 1/2″ x 1/10″)

It's a completely new way to display digital information. The Hewlett-Packard solid state numeric display packs everything in one, small unit only 1"x 0.5"x 0.16". Gallium arsenide phosphide diodes and an IC driver/decoder chip deliver bright red numerals—bigger than life, visible for yards.

This new "total package" also gives you the edge on cost. You don't have to buy driver elements, or anything else. No special interfacing is needed. Only four line 8-4-2-1 BCD input and less than five volts to drive it. The modules are available in three-character packages, too.

The Hewlett-Packard solid state numeric display is ideal for instruments requiring smaller, tighter display panels. Or any application demanding either low power or resistance to shock and vibration, without catastrophic failures.

Get more information about the new technology for numeric indicators. Call your local HP field engineer or write Hewlett-Packard, Palo Alto, California 94304; Europe: 1217 Meyrin-Geneva, Switzerland.

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SOLID STATE DEVICES

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DEVELOPMENTS

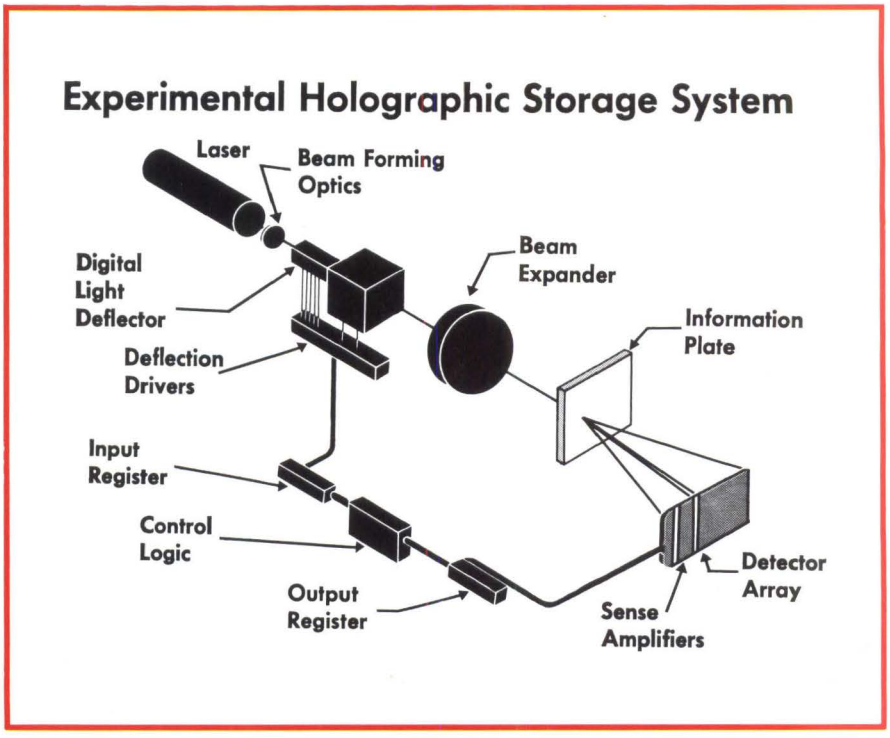
Holographic Memory System Exhibits Rapid Access

An experimental optical memory system that could lead to storage devices a thousand times faster than today's disk and drum storage units has been reported by IBM's Systems Development Division Laboratory, Poughkeepsie, N.Y. In the experimental system, blocks of information are accessed by a laser beam in 10 microseconds, and it could conceivably allow more than 100 million bits of information to be stored on a nine square inch holographic plate. Such a memory could significantly reduce storage costs, increase capacity and provide more reliable and rapid collection of stored data, according to IBM.

The system is described as a holographic, block-transfer, optically accessed store which uses a method of accurately deflecting a beam of light whose position does not change with variations within the deflecting subsystem. In the experimental memory system, the digital light deflector (DLD) consists of alternating electro-optical material (typically KD*P) and birefringent material (calcite). By controlling the voltage across the electro-optical material, the polarization state and hence the position of the emergent light beam is controlled. The DLD accurately positions the light beam to any one of the blocks on the hologram. Each block is recorded with diffused illumination techniques using a photographically prepared mask containing the bits. The block size on the hologram is 2 mm and the beam from the deflector is approximately 0.3 mm, therefore, the beam must be expanded by approximately 6X. This expansion is done by pairs of astronomical doublets. The reconstructed image from the hologram is automatically focused on the detector bank. As the beam is deflected from block to block, the corresponding images remain focused on the detectors. The photodetector array is comprised of photodetector diodes, which consist of a PIN photodiode in series with a blocking diode. Electronic drive circuits, sense amplifiers, and an output register complete the electronics circuitry.

An engineering model was built with several simplified specifications to show the feasibility of the experimental system. The feasibility model used a HeNe 80 mW laser. The deflector output was reduced to four deflectable positions; the beam expanders were eliminated and access to the full information plate diagonal was provided by a set of manually positioned mirrors. The hologram consisted of 3 groups of 4 blocks each with the two end groups separated by approximately 7 inches. Manual mirror positioning provided access to any of the 3 groups, with high-speed electronic access to any of the 4 blocks within a group. The detector array contained 81 detectors arranged in 3 x 3 groups in a square pattern; each group contained 3 x 3 or 9 active detectors. The sensitive area of each element was approximately 0.010″ diameter, with centers at 0.032″. Nine detector chips were bonded to a module, which was then pinned into a mother board. This board also contained the sense amplifiers.

The exposure of the hologram blocks was made using diffuse techniques. A coded mask with a 3 x 3 pattern corresponding to the detector array was used; however, the size encompassed the full bit array. A memory exerciser was fabricated to drive the DLD, and to provide timing points for the readout of the detector array and a set of latch circuits was used to ensure error checking of the information.



The experimental optical memory system developed by IBM's Systems Development Division Laboratory, Poughkeepsie, N.Y., will access information recorded on a holographic plate one thousand times faster than conventional auxiliary storage devices such as disk and drum memories.

Dale Mrazek
National Semiconductor

MOS BRIEF 4

MOS DELAY LINES

Integrated delay lines let digital system designers escape one of nature's small tyrannies—finding a match between system timing and the prefixed delay set by a glass or wire line's length, or a drum's rpm. In contrast, the input-output rates and storage time of an MOS shift register can be controlled individually to mate with any part of the system, be it instrumentation, data link, or computer.

The simplest, smallest, and least power-hungry delay lines are those made with MOS dynamic shift registers. Each silicon chip contains up to 200 storage nodes and the digital equivalents of input transducers and output detectors. All the designer supplies is a few microwatts of power per bit, clock signals, and data. Data can be shifted through the register at rates from near DC to greater than 15 MHz.

Lines that store only a few hundreds or thousands of bits are less expensive to build with MOS. The line in Figure 1a is just the series-connected halves of an MM506 dual 100-bit dynamic register and a few pull-down resistors. A dynamic register is run with a two phase clock, static registers require a single clock. At 700 KHz or less the clock driver (Figure 1b) can drive three or more MM506's or more than a dozen dual 16-bit static registers.

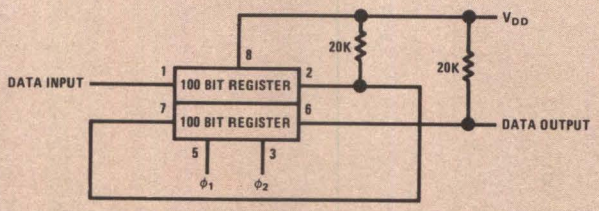


FIGURE 1a. Series-connected Delay Line.

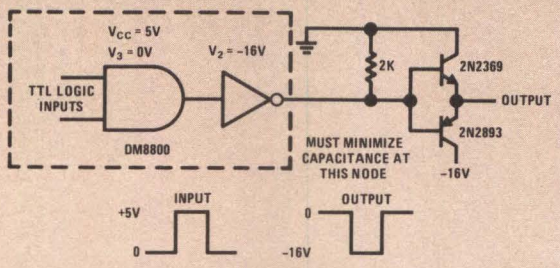
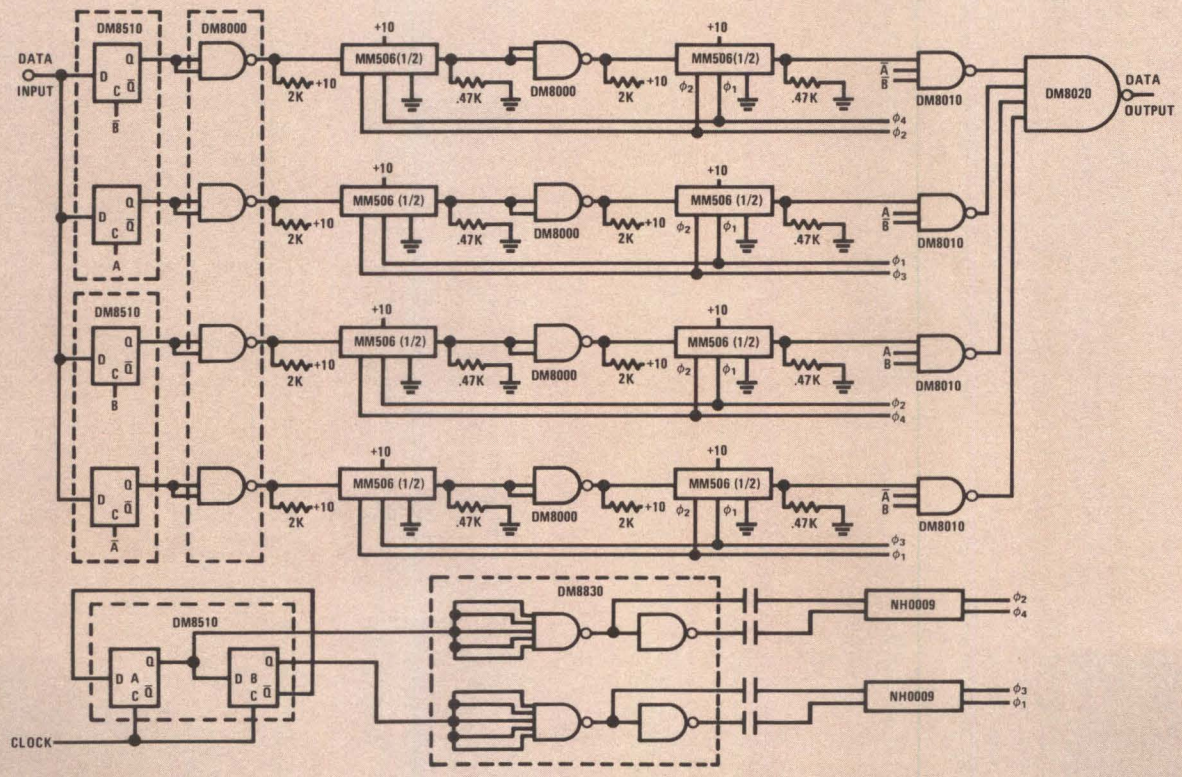


FIGURE 1b. Line Driver.

Delay duration is the product of the clock period and the number of bit-storage nodes in the registers. At 1 MHz, for instance, 200 bits would be delayed 200 microseconds. The longest delay possible in a dynamic register is determined by the minimum operating frequency, which ranges from about 10 to 25 Hz at 25°C to 10 KHz at 125°C. If the designer wants a shift rate in the megahertz



INTEGRATED CIRCUIT PARTS LIST							
3	DM8510	Triple 3-Input NAND Gate	2	DM8000	Quad 2-Input NAND Gate	1	DM8830	Dual Differential Line Driver
			1-1/3	DM8010	Dual D Flip-Flop	2	NH0009	2ϕMOS Clock Driver
			1/2	DM8020	Modulo-n Divider	4	MM506	Dual 100-Bit Dynamic Shift Register

FIGURE 2. High-speed Register Uses TTL Logic to More Than Double MOS Shift Rates.

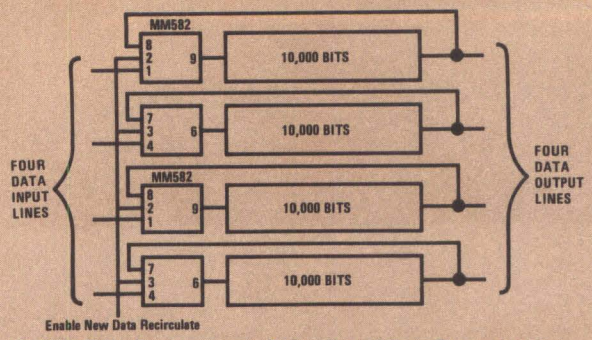


FIGURE 3. Synchronous Delay-line Array Operates as a 60,000-bit Drum Memory.

range, but wants to delay the data much longer than microseconds, he can inhibit the clock between loading and unloading of the register, or recirculate the bits at low frequency within the register while reading in and out at high speed. To overcome a data synchronization problem, data can be shifted in at one rate and out at another.

Dynamic registers would lose data if the clock is stopped indefinitely, since they don't contain latching devices. Static registers do have latches, and can therefore operate at DC dlock rates at any temperature. Their clocks can be stopped, allowing indefinite delays. The price of latching and other special features of static registers is less bit capacity per chip than dynamic registers.

Clock rates much higher than the normal MOS speed limit of 1 to 5 MHz can be achieved by operating registers in parallel or interfacing them with TTL logic. Both methods are combined in the Figure 2 delay line, which has been clocked at 16 MHz. The high-speed clock and data inputs are distributed among the registers so that the upper MM506 transfers and delays bits numbers 1, 5, 9, 13, etc., of the data. The next two MM506 halves handle bits 2, 6, 10, 14, etc. The bits flow through the registers at a 4 MHz rate. When the four bit streams are reassembled in the DM8020 NAND gate, the data rate of 16 MHz is restored.

In an all-MOS system, an MM506 register could be clocked at 1 or 2 MHz. The limit is largely imposed by RC time constants raised by the high impedances of adjoining MOS elements. The register runs at 4 MHz in the Figure 2 configuration because TTL gates are fore and aft of each MM506 half. Thus, each register is driven at its input by a low-impedance source and each output terminates in a low impedance, low level sensor, making the outputs more easily detected. The TTL–MOS interfaces are simply pullup resistors at the register inputs and pull-down resistors at the outputs.

Parallel series of registers also make a fine "drum" memory—that is, a rectangular array of synchronous delay lines (Figure 3). When less than about 200,000 bits of storage are needed, MOS drums are less costly than electromechanical drums. An MOS multiplexer (MM582) does the gating required to write a word into a register, recirculate it and access it upon command. With counter addressing, the contents of a specific register in a series can be read out without disturbing the contents of other registers.

If the data stored in a line is recirculated within several minor loops in each line, the access time will be reduced proportionately. The recirculating loops in Figure 4 were designed to allow the continual shuttling of data from TTL logic into the MOS delay loops, and back out into TTL logic. The loop lengths should be kept to multiples of one another—say 100 or 50 bits—to avoid clocking complications. Here, too, the few additional TTL gates and resistors allow the registers to be clocked at up to 4 MHz.

Since each register in a delay line can operate independently, almost any combination of the basic operating modes in different segments of a line can be used. For instance, assemble a delay line with variable taps, build buffer memories with selectable delays to faciltate time-shared processing of data from several sources, or match low-speed sensor data to relatively high-speed logic circuits. Numerous specialized design-options are also available, such as clock formats that permit asynchronous operation of registers in a line or keep power dissipation well below the normal levels.

Write for data sheets on MOS and TTL devices used in delay lines.

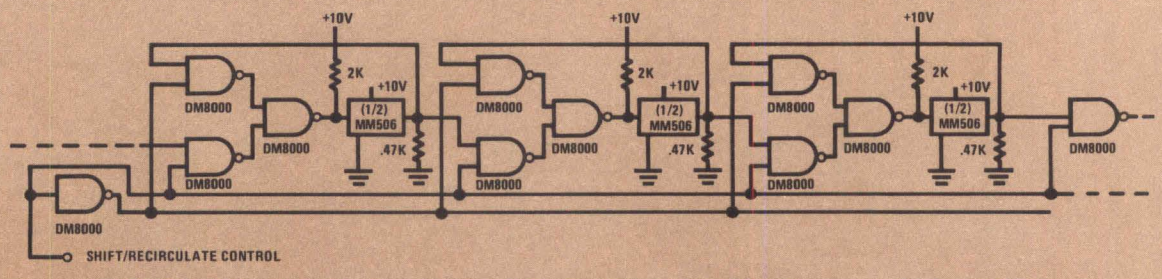


FIGURE 4. Recirculating Loops are Compatible with TTL Logic and Can Operate to 4-MHz Shift Rates.

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DEVELOPMENTS

Video Editing Boosts Picturephone Service

An experimental method of "editing" video signals before transmitting them holds promise of allowing three PICTUREPHONE® calls to be made over some facilities that might otherwise carry only one.

The method, devised by F. W. Mounts of Bell Telephone Laboratories, Murray Hill, N.J., involves transmitting only significant differences that occur from picture-to-picture in a video signal.

In Picturephone communications, in any short period of time, only a small portion of the picture changes—for example, an eyelash flutters, or lips move—but the rest of the picture remains the same. Picturephone service, which the Bell System is developing for commercial use in the 1970's, transmits all information about the picture 30 times each second. Since there is little change in a picture in one-thirtieth of a second—the position of a person's head generally remains the same—the present technique transmits much repeated information. This type of repetition is called "frame-to-frame" redundancy.

White dots in this actual video-telephone picture show areas of significant change during face-to-face communications in one-sixtieth of a second. An experimental technique (called conditional replenishment) developed by Bell Telephone Labs transmits only these changes to update the previous picture.

The new method removes most of this redundancy, and it does so without reducing picture clarity—it is called "conditional replenishment."

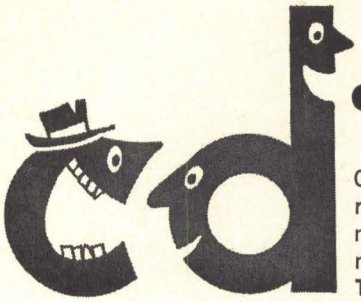
In the conditional replenishment technique, digital frame-to-frame processing is used to continuously store a reference picture and update or replenish only elements that change between frames. Then, only the picture information needed to update the reference picture is transmitted. Received picture information is used to update a similar stored reference picture, which tracks the one at the transmitter.

The new technique does this by expressing video signals as 8-bit numbers, and position of the signals as 7-bit numbers. In order for the receiver to update the picture elements correctly, both these pieces of information must be conveyed to the receiver.

The frame memory consists of delay lines and stores one complete frame of video information encoded as 8-bit pulse code modulation (PMC). A subtractor circuit compares the new information from the camera with the reference picture stored in the frame memory and determines the difference between the stored and new picture.

Each sample period, control logic decides whether a significant difference exists between the signal values. A selector switch strobes the new signal value into the frame memory to update the reference picture if a significant change occurs; otherwise, the signal value stored in the memory is maintained. Each time a reference picture is updated, a buffer stores the value and position of the information needed to update, and it is then read out onto the transmission line at a constant rate on a first-in, first-out basis.

Although the principle of conditional replenishment is applicable to commercial television, it is limited by the amount of motion occuring from frame to frame. Thus, for commercial television, in which movement is usually constant, the technique is impractical.



commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of **T. PAUL BOTHWELL, Contributing Editor.**

Interpretive Simulation

RONALD D. MALCOLM

Interpretive simulation is a particularly desirable method for digital computer simulation. Its advantages are: short implementation time, low memory consumption and ease in handling changes in the original task program.

In the interpretive simulator, the operation performed by each instruction or command of the original computer is emulated by a programmed subroutine. A set of subroutines is written, one for each instruction in the original computer. An interpreter routine, in the simulator, examines each instruction of the task program and selects the corresponding simulator subroutine for execution.

The program (sequence) counter of the simulator does not move through the task program itself. It moves from the interpreter routine to a simulation subroutine and back to the interpreter routine. A register or memory cell, used as a pseudo program counter, is updated by the interpreter and simulation routines to keep track of the current position in the task program. The original task program is thus executed a step at a time with each instruction performed in the same sequence and fashion as by the original computer.

Ronald D. Malcolm, the author of this month's CD Commentary, is a Senior Systems Engineer at Honeywell's Computer Control Division. His responsibilities include design of digital computer base systems, custom computer options, and special purpose digital systems.

The interpreter routine generally uses the task program operation codes to cause reference to a table of simulation subroutine starting addresses, with each code causing entry into a different place in the table. The interpretation is accomplished by adding the operation code to the address table base address to select the appropriate subroutine starting address, and then setting the program counter to this starting address. This operation is similar to "indexed indirect addressing." (Fig. 1).

The address fields of task program instructions are also interpreted and equivalent simulator addresses generated. Memory reference instructions reference equivalent memory locations in the simulator; register reference instructions are caused to reference an area of the simulator memory used to simulate the hardware registers of the original computer. Indexing

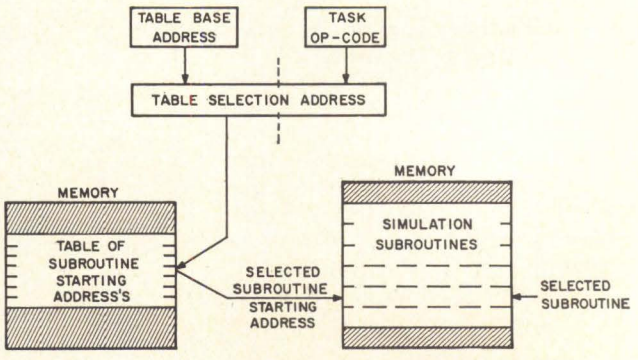


Fig. 1 Operation code interpretation.

DATA COMMUNICATIONS
equipment for on-line, real-time processing

data arrives by jet at 1200 WPM

Teletype announces a new arrival: a high speed electronic terminal that takes data off the line as fast as it comes in. Teletype's new Inktronic® printer ("The Jet Set") prints without pausing for "fill" characters.

In modern data processing and communications, where economy is measured in milliseconds, a machine that can convert data into hard copy at transmission line speeds without lagging is a truly practical terminal—especially for time sharing operations, or high volume computer output.

Add the advantages of low cost and rugged endurance, and you begin to get an idea why we're proud of our new Inktronic RO (receive-only) printer: first terminal in a complete new 1200 wpm line which will include KSR (keyboard send-receive) and ASR (automatic send-receive) sets, with future plans for even higher speeds to completely utilize voice grade channels.

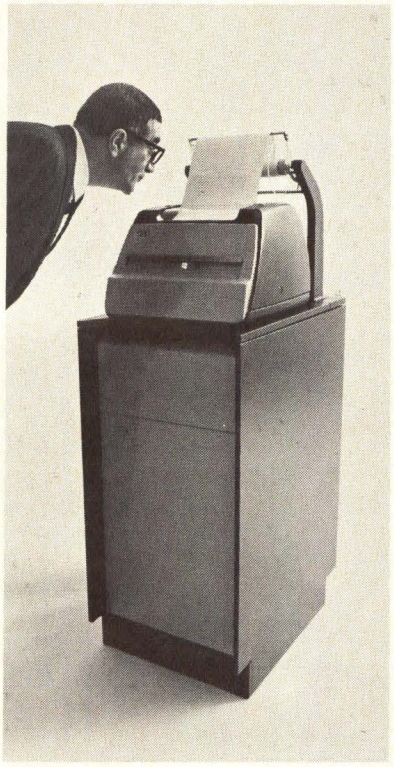
THE PRINTER WITH NO CHA! CHA! CHA!

The Inktronic printer is as different from ordinary machines as jets from props. The electrostatically deflected ink jet printing is continuous (character by character) instead of periodic (line by line). There is no cha-cha-cha printing rhythm. And there is no rhythmic printing noise —just a barely audible undertone accompanied by miles of incredibly unwinding copy.

A copy continuum!

NO BUFFER STORAGE

We didn't cut out the printing



rhythm to keep the data from dancing. As a matter of fact, the Inktronic printer will make data dance all over the page, producing print wherever wanted. Its printing format is unrestricted.

What it doesn't do is store up full lines of characters, including blank fillers, for periodic print-out from buffer storage. The Inktronic printer simply takes the characters as they come off the circuit, and fires instant print through forty electronically controlled jets. It doesn't waste time storing imaginary characters to "fill" empty spaces after partial lines.

By eliminating buffer storage, Teletype R&D engineers have achieved a higher effective speed. They have reduced the time and cost of data print-out. And they have produced a practical data terminal with few moving parts. Actually, only one part moves in the entire ink guidance system. So the "Jet Set" should not need much of the usual maintenance care.

Here, in fact, is an electronic printer that will maintain a 1200 wpm pace month after month without faltering. It's meant for heavy duty use in a variety of ways, including use as an on-line computer terminal; or as a monitor for high speed tape-to-tape systems.

FAST AND ECONOMICAL

The Inktronic printer's speed is combined with convenience and economy features that make it an ideal on-line terminal.

It will print up to 64 alphanumerics for which its transformer core memory is programmed.

It is available with either the 5-level code or U.S.A. Standard Code for Information Interchange (ASCII).

It uses inexpensive ink, and gives you more than 15 miles of fully printed lines to the pint—on regular, inexpensive, 8½ inch wide teletypewriter paper.

Incidentally, the ink is easier to insert then a typing ribbon. And cleaner.

Why not get all the available facts on how you can have data arrive faster by jet? Contact Teletype Corporation (71M), 5555 Touhy Avenue, Skokie, Illinois 60076.

machines that make data move

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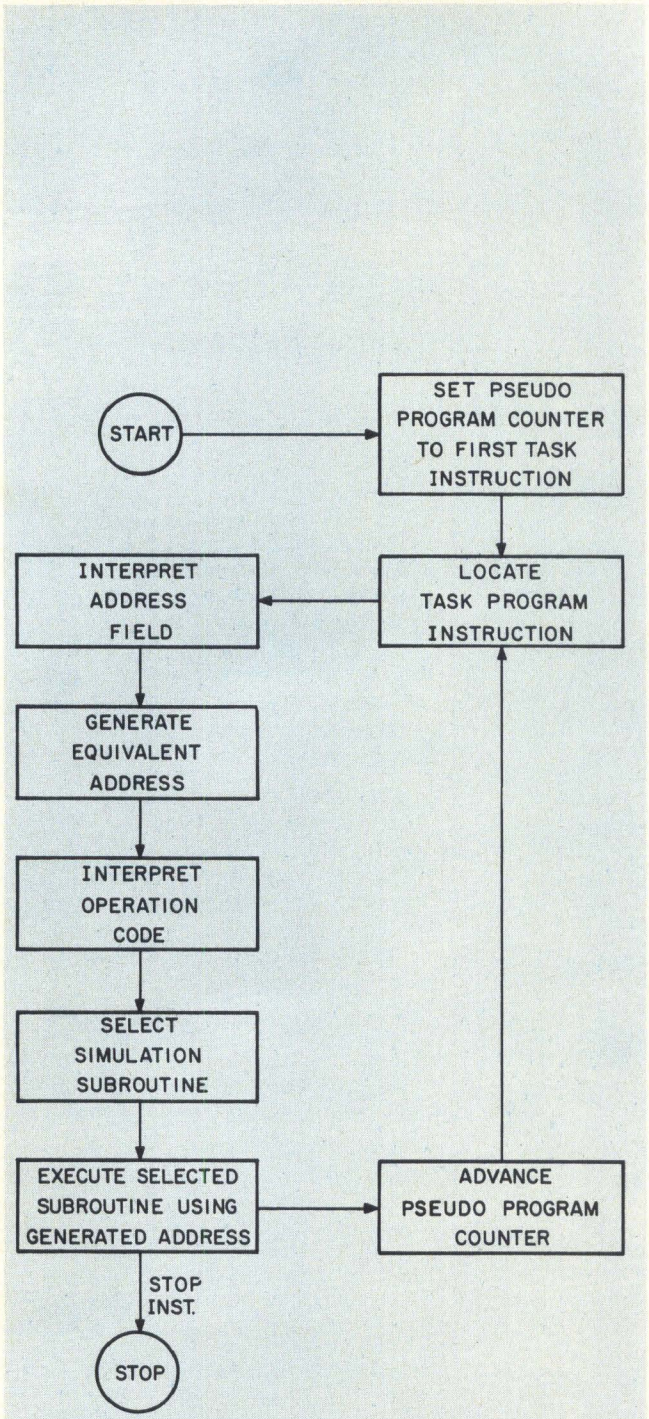

Fig. 2 Simulator operation flow.

and indirect addressing is also simulated by the interpreter routine.

The results of simulated arithmetic computations must be identical to those of the original computer to allow for the modifying of task instructions (i.e., changing address fields of table referencing instructions) by the task program itself (Fig. 2).

Fig. 3 is the layout of a typical simulator memory. The hardware registers of the original computer are simulated in memory locations in the simulator, allowing register access and manipulation when specified by task program instructions. The simulator's peripheral devices may require special routines to correct data formats or simulate block transfers, direct memory channels, etc.; the simulator's interrupt facility may require routines to handle it.

Real-Time Simulation More Difficult

It can be seen that the specification for an interpretive simulator is essentially equivalent to the functional specification of the original computer. This makes the production of the simulator a clearly defined task. Creating a non-real-time simulator by the interpretive method, using a general-purpose computer, poses no particularly difficult problems. Real-time simulation, on the other hand, requires very careful consideration, and certain relationships between the original and simulator computers must exist to allow practical real-time operation.

The real-time simulator must generally be faster than the original, or more powerful, or both. The probability of success is improved if the arithmetic conventions are the same, if the simulator word

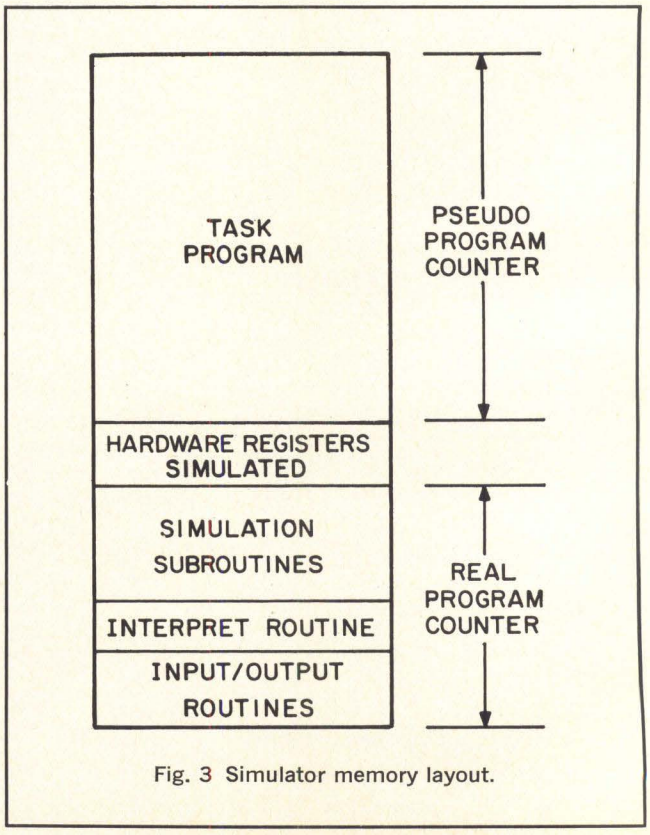

Fig. 3 Simulator memory layout.

DATA COMMUNICATIONS

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For example, the Model 33 ASR (automatic send-receive) set with PBDG (Push Button Data Generator) reduces the time consuming business of typing small amounts of fixed data to the simple act of pressing a button. A button that never makes stenographic errors!

Preparing computer input tapes off-line with this ASR set is a breeze. The various fixed data are entered by pushing appropriate PBDG buttons among a set of twelve. Variable data is typed in from the keyboard. The completed, punched tape is then put into the ASR's reader, and the computer is called. The intricate computer instructions, already programmed into the PBDG, are transmitted by simply pressing a single button.

Smooth, steady, timesaving, 100 wpm tape transmission begins immediately. Both line and computer time are saved.

PBDG sets are available with as many as 96 pushbuttons, for reproducing fixed data in groups of 24 characters per button. They can be used with all other Teletype teletypewriter terminals, as well!

USERS LIKE MODEL 33

The dependability and low cost of Teletype Model 33 ASR (automatic send-receive), KSR (keyboard send-receive) and RO (receive only) sets have commended them to many users and developed many uses. Computer manufacturers use them as input/output terminals. Banks use them to contact investment firms for securities information. Model 33 employs the U.S.A. Standard Code for Information Interchange (ASCII), and can communicate with most computers and other business machines. Manufacturers use them to transmit multicopy forms.

Computer assisted instruction in schools has developed more recent uses. In Chicago, a well-known university conducts a computer service involving problem solving for more than 1,000 students at 16 city and suburban high schools and junior colleges equipped with Teletype Model 33 terminals.

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In addition to value and versatility, Model 33 sets offer a full array of special purpose options.

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Details on these and many other Model 33 product features are available from Teletype. If you are looking for terminals that will adapt to unique systems, contact Teletype Corporation, Dept. 71M, 5555 Touhy Avenue, Skokie, Illinois 60076.

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CIRCLE NO. 19 ON INQUIRY CARD

TELETYPE

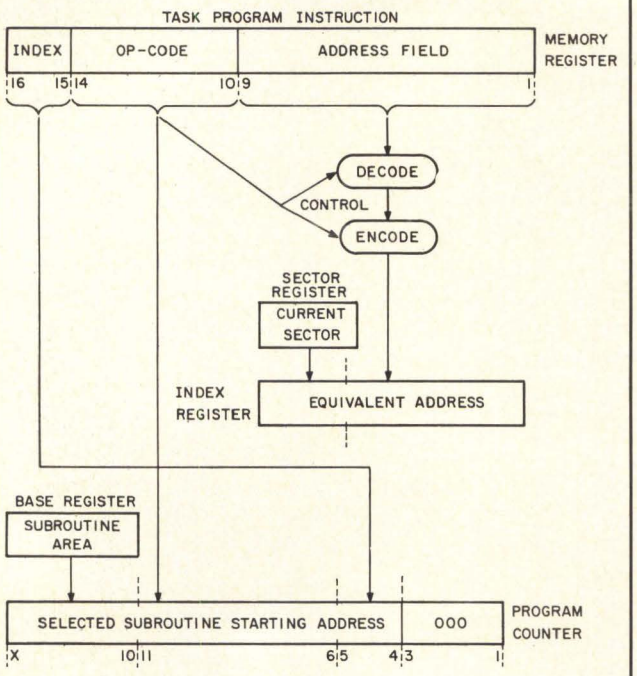

Fig. 4 Special interpret instruction.

length is equal to or greater than that of the original, if the addressing capabilities are similar, and if the input/output structures are similar.

The overhead (time) required for operation code and address field interpretation is the major stumbling block for interpretive simulation in real time. A number of general-purpose computers have "simulate" or "interpret" instructions to help reduce this overhead. An interpret instruction, tailored to a particular interpretation application, can be very effective in reducing the overhead. Special arithmetic and register manipulation instructions tailored to the application may also help increase simulation speed.

The special interpret instruction can be made to interpret both the task operation codes and address fields. The instruction automatically sets the program counter to the first instruction of the desired subroutine, and loads a hardware register (e.g., Index Register) with the generated equivalent address. The operation of such an instruction for an example simulation of a 16-bit computer with a six-bit operation code, nine-bit address field, and two-bit index specifier is shown in Fig. 4. The three low order zero bits in the program counter allow each simulation subroutine eight memory cells (enough for most operation simulations). The few instructions requiring larger subroutines have the remainder of their subroutines located outside of the primary subroutine area.

The special interpret instruction can make an interpret program routine unnecessary altogether by including an automatic increment of the pseudo program counter (index register) each time the interpret instruction is executed.

The simulation commences by loading an index register with the task program start location on the original computer. An interpret instruction is executed using the index register, and an augmenting address field generating a resultant memory address equal to the task program starting location in the simulator memory. This instruction will interpret the first task program instruction and cause the associated simulation subroutine to be executed. The last instruction of each sub-routine is an interpret instruction identical with the one described above. The program counter of the simulator thus moves from one subroutine to another, as controlled by task instruction codes, and the index register (used by the interpret instruction) becomes the task program pseudo program counter.

This type of special interpretive instruction, coupled with tailor-made arithmetic and register manipulate instructions, forms a very efficient simulator at reasonable cost. Even with this capability, the simulator must be inherently faster than the original computer to achieve real-time simulation. Fortunately, most special purpose air-borne or space-borne computers are designed to be relatively slow in order to achieve the high reliability required.

Other methods of simulation may be used in severe real-time applications. The simulator's tasks may be reprogrammed in the language of the simulator computer, or a task program translator used. Reprogramming results in the most efficient simulation, but has the disadvantages of high cost, long implementation time, and difficulty in keeping pace with changes in the original task programs. Program translation, although somewhat faster than interpretive simulation, produces a substantially dilated equivalent task program, consuming a great deal of memory. A translator is very difficult to produce, and may not be practical, in the event the original task program modifies its own instructions (as in moving pointer address fields and updating counting instruction address fields).

Conclusion

Interpretive simulation methods have been used successfully to simulate flight computers for astronaut training, for developing software for computers simultaneously with hardware development, in implementing conversational languages on time-shared computer systems, and for conserving memory space in space-borne computers. Micro-programming (simulation of a non-existent computer) is used in some of the latest computers to allow a computer with a relatively simple basic instruction repertoire to perform more complex programmed instructions by executing subroutines stored in a fast read-only memory. Indications are that future computers will use more of this mode of operation to conserve expensive read/write memory, as the speed and cost of logic circuits and read-only control memories continue to improve.

DATA COMMUNICATIONS

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sorry, no hieroglyphics, but...

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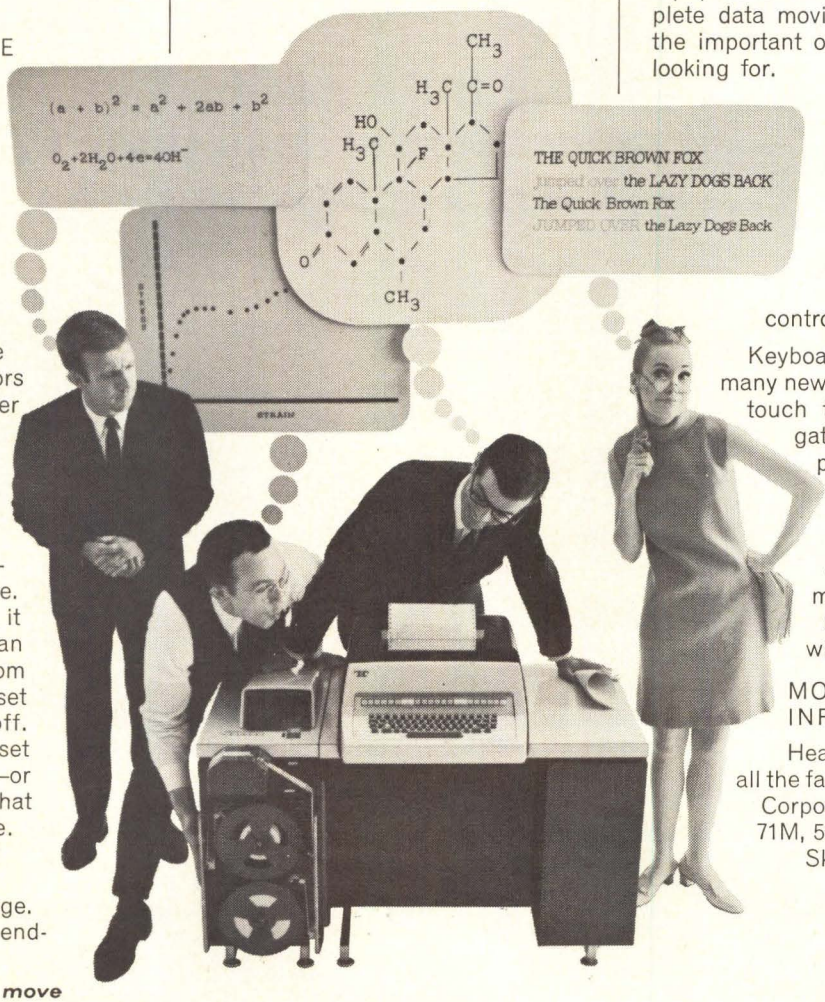
The Model 37 line consists of RO (receive only) and KSR (keyboard send-receive) sets, and the ASR (automatic send-receive) set shown here plus paper tape punches and tape readers housed in modular units compatible with all Model 37 equipment. You will have a complete data moving system with all the important options you've been looking for.



The KSR and ASR sets can be equipped with form feed-out controls that enable an operator to advance multi-copy forms into the printer by remote control. A real timesaver.

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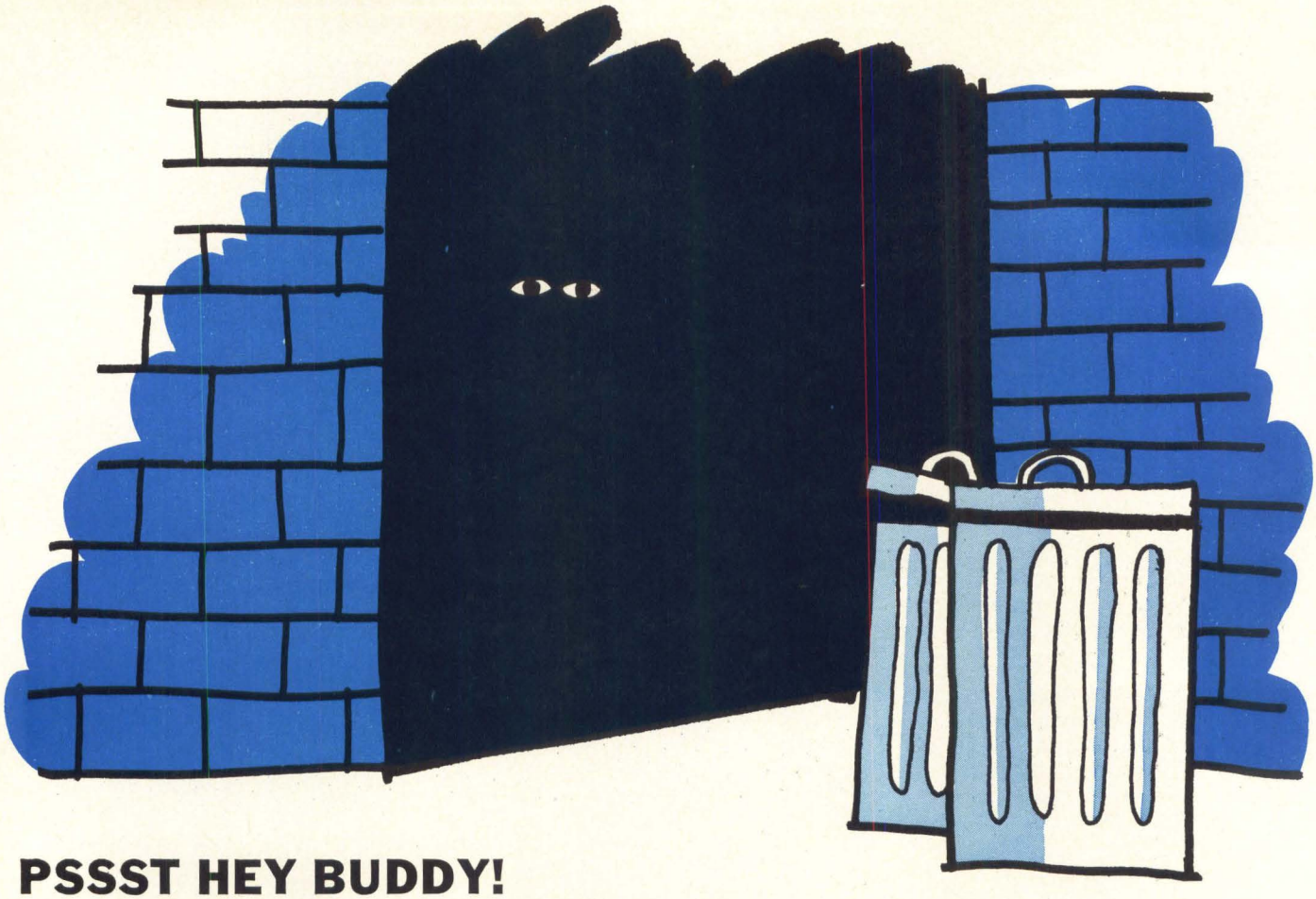

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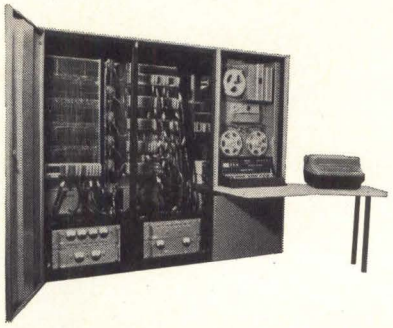

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CIRCLE NO. 21 ON INQUIRY CARD

Total computing system integrity may be evaluated by exercising all instructions, performing sample problems, and comparing with precomputed results. Memory access integrity may be evaluated by the means discussed in this article.

ON-LINE MEMORY INTEGRITY EVALUATION AND IMPROVEMENT

Frank Bujnoski

Honeywell Inc.
Aerospace Div.
St. Petersburg, Fla.

A processor consisting of a finite number of bistable elements may be considered a discrete-state device. At any time when all the bistable elements of such a device are in a stable state, the state of the system may be represented by an "n" dimensional vector (where "n" is the number of bistable elements). The state of such a device typically changes with time in coincidence with a quantized clock. Since "n" may be as high as several hundred, the number of unique states which the device may assume is astronomical. At any quantized clock time when one of the "n" elements is in error, an erroneous state exists.

State of the art Von-Neuman (stored-program) organized machines are organized so that the various discrete states of the machine are sequentially specified by instructions and data words stored in memory. The erroneous discrete states which may occur in stored computational or control program sequences can be catastrophic to the program; for example, an add command may be misinterpreted due to improper memory operation, producing a grossly erroneous state such as an unconditional transfer out of a program routine, thereby effecting loss of program control. Similarly, an add command may be misinterpreted due to improper memory operation as a multiply, an operand address may be misread effecting access to a wrong memory location, or a data word may have a misread bit in one of the more significant bit positions, thus providing grossly erroneous data.

It must also be noted that equally catastrophic results may be effected by improper operation of the control section of the processor; for example, a malfunctioning command decoder may similarly effect misinterpretation of an add command as a multiply or an unconditional transfer, or the memory address register or decoder may improperly command access to an erroneous data address similarly providing grossly erroneous data.

Thus, although control section errors may be just as catastrophic as memory errors, experience indicates that memory is generally the weakest link in the computer system in terms of reliability. Hence, some error detection for memory, such as parity circuitry (which detects one or an odd number of bit errors), or programmed error detection is usually justifiable.

The main consideration when considering the inclusion of some sort of memory error detection is a tradeoff evaluation of the required time and/or space redundancy versus the measure of memory integrity improvement achieved.

MEMORY ORGANIZATION

The ferrite toroidal core memory operated in a coincident-current threshold select mode has become the current standard memory system among both military and commercial computer suppliers.

Classically, in the toroidal core memory, the cores are physically arranged as points in a three dimensional coordinate system. The X and Y coordinates together specify a word address. The Z coordinate specifies which bit of the word the core represents.

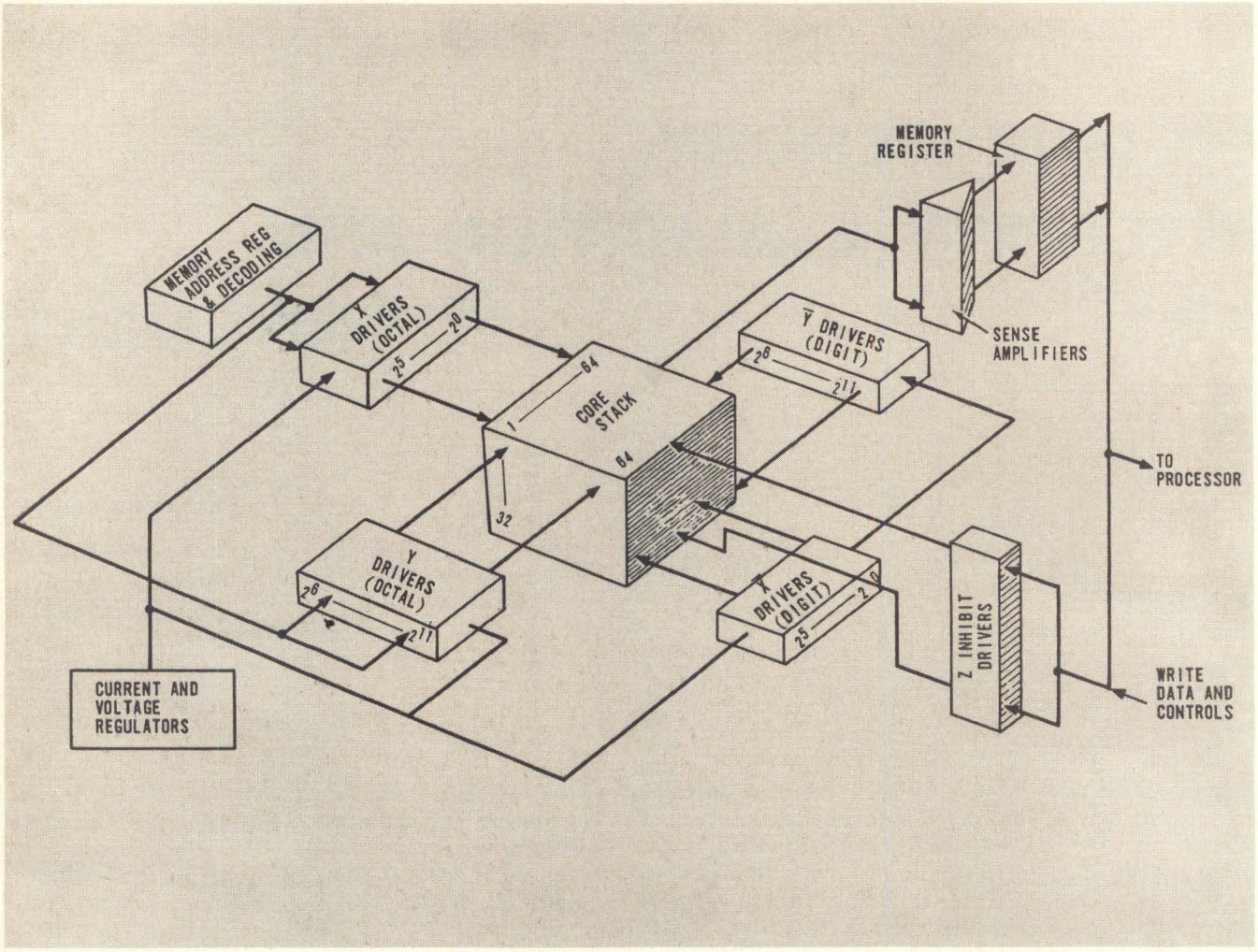

Fig. 1 Toroidal core memory block diagram.

Thus, conventional memories are designed to be extremely symmetrical to conserve electronic components by functional sharing of circuitry. A typical memory organization is shown in Fig. 1.

The number of word drivers for a 4,096 word memory is $4(N)^{1/4}$; in other words, for N = 4,096, 8 octal and 8 digit drivers for both the X and Y addresses will total 32 drivers. Add to this (typically) two diodes for each X and Y coordinate location, which totals 256 diodes, plus one Z inhibit driver and one sense amplifier for each bit of the word; all of which comprise the total electronics complement for a 4,096 word memory module.

A wide variety of less popular memory types with relatively slight organizational differences are also available. These include planar and wire-deposited film, multi-aperture ferrites, solid state semiconductor chip memories, and various "permanent" or read only devices.

HARDWARE PARITY BIT MEMORY CHECKING

The inclusion of a memory parity bit in typical memory organizations requires the addition of a redundant bit per word (or per each n bit byte) plus its associated read, write, inhibit and sense electronics. To this must be added the electronics for checking and generating the parity bit for each memory cycle.

Parity generation and checking is very easily performed in a word serial mode; however, state of the art memories are typically "word parallel", and the time required for parity checking and generation in a serial mode is prohibitive for most applications. Therefore, to preclude prohibitive time delay at present-day memory speeds, parity checking and generation must be performed in a parallel or hybrid serial/parallel mode, resulting in a considerably greater cost in hardware.

Parity bit inclusion penalties are nominally 6 to

15 percent in memory hardware component count and 18 to 20 percent in memory cycle time; for example, a 2 microsecond cycle time memory may become a 2.4 microsecond cycle time memory with 10 percent more components when parity detection is added. Parity bit hardware is essentially space redundancy, though it does require additional time for the parity detection and generation.

PROGRAMMED PARITY MEMORY CHECKING

It must be noted that memory integrity may be checked without the specific inclusion of a parity bit. Programmed read and check sum evaluation of critical instructions and constants prior to routine execution will evaluate parity on a bit-by-bit basis for all words checked. This method will detect persistent (fixed) errors, but could miss intermittent (noise type) memory errors. Intermittent errors may then be detected using output parameter reasonableness checks. This approach is "time redundancy" and does not require additional electronics.

PROGRAMMED MEMORY ELECTRONICS CHECKING

Memories are designed for a high degree of symmetry and functional circuit time sharing. The word selection process may be considered as a square matrix array organization of N elements (where N is the memory word size); thus, a word is uniquely specified by its row (X address) and column (Y address) locations. Refer to Fig. 1

Since memory electronics failure rates are significantly higher than stack failure rates, a measure of memory integrity may easily be determined by checking the memory electronics. For example, reading out eight appropriately selected word addresses (one octal and one digital for both X and Y dimensions) containing selected word formats will evaluate all of the word drivers, many of the diodes, and all sense amplifiers. An automatic rewrite follows each memory read; inhibit drivers (write) are thus checked by rereading the same location. Memory-peculiar worst case word formats are included to detect marginal elements and worst case signal to noise ratios.

Thus, memory electronics can be easily evaluated with relatively few instructions, and gross integrity of the total memory subsystem may be evaluated with less expenditure of time and space redundancy than checking each memory readout cycle.

PROGRAMMED "REASONABLENESS" CHECKS

An additional malfunction detection scheme is the performance of "reasonableness" checks wherein computed routine results are compared with results of previous iterations. If results are not within specified limits, a malfunction (of some type) is assumed to have occurred.

CORRECTIVE ACTION

More important than detecting the malfunction is what to do when a malfunction occurs. Conventional parity checking and checksum evaluations detect, but cannot correct, an error. Once a memory word is read out in error in conventional Destructive Read Out (DRO) type memories, it is automatically rewritten and will be rewritten in error, resulting in a permanent compromise of stored information.

The only recourse then is:

Continue and perform "reasonableness" checks
Routine abort
Program roll-back
Reload the program from bulk memory
Program mode check

In any case, any corrective action must be derived from progammed corrective action.

Reasonableness Checks

For routines which are not critical, reasonableness checks are performed. If the results are within specified limits (indicating the error was not catastrophic) the program may be continued.

Program Reload

When a bulk store is available, all programs should be contained in the bulk store. Upon program memory malfunction, the affected program should be reloaded and verified.

Program Roll-Back

Program roll-back for corrective action must be routine or function oriented since it is impractical from a storage requirement point of view to provide corrective action for each instruction. The roll-back must be to a point where initial conditions are available from sensors, prestored, or reconstitutable. Even an intermittent memory malfunction during access becomes a persistent error since it is immediately rewritten in error. Thus, critical routines or high iteration rate real-time routines (for example, those which perform integration with respect to time) should be stored redundantly so that in the event of malfunction the redundantly stored routine is used to preclude routine malfunction or error buildup with time.

To provide for recovery from error, initial conditions for the routine and failure recovery address must be stored so that in the event of malfunction, the program is automatically interrupted and forced

to the recovery location. Refer to Fig. 2.

The following is an alternate roll-back scheme where programs are stored redundantly and hardware parity detection is provided:

Upon error detection, an interrupt forces entry into a correction routine which stores the program sequence register. This address then provides a pointing address from which the address of the redundantly stored instruction or constant may be derived. The correct word is then read and stored in the malfunction location. The corrected routine is then recycled.

Program Mode Checks

Program mode-controls (mode-switches or stored mode-control words) should be reread after each routine or timed interval to prevent complete loss of control. Thus program hang-up may be precluded by loading a real-time counter with a Δt such that an elapsed time interval greater than the longest routine (Δt) will cause the counter to overflow which interrupts the processor and reinitializes the program.

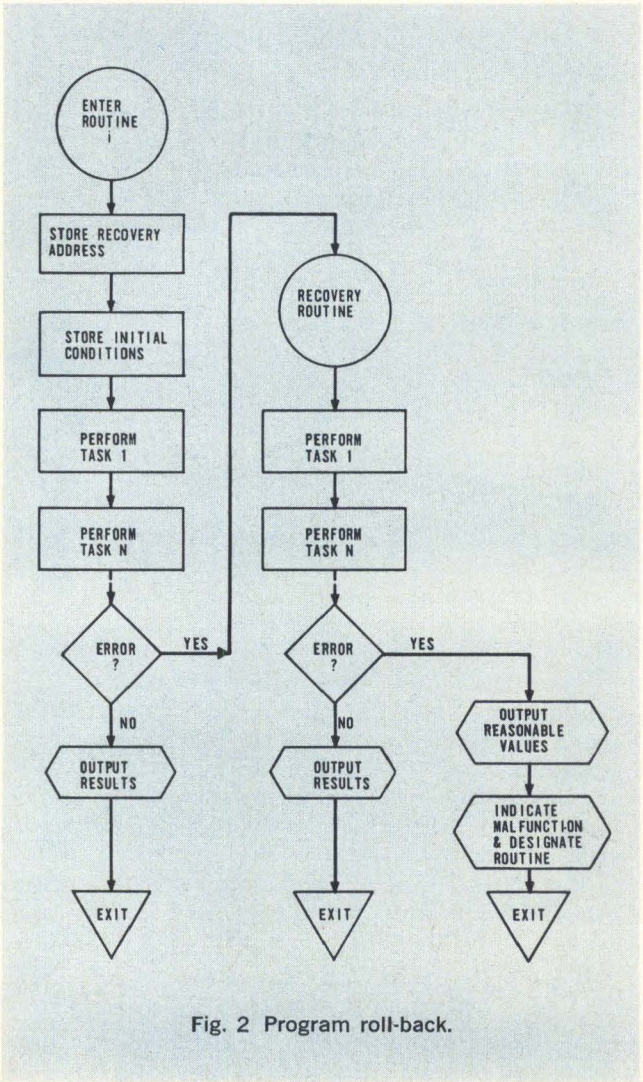

Fig. 2 Program roll-back.

NONDESTRUCTIVE READOUT (NDRO) MEMORIES

In the case of NDRO memories, where transient or intermittent errors can occur without becoming persistent errors, the malfunction circumvention approach is the same with the following possible exceptions.

On the first routine iteration during which a readout error occurs, the program continues and reasonable result values are used. However, an error counter is incremented with a weighted increment for each incorrect pass and decremented for each correct pass. If the counter overflows indicating persistent errors, the redundantly stored routine is used as in the DRO memory case.

The major advantage of NDRO type memories is their greater tolerance of intermittent or transient type errors. Counteracting this to some extent is the fact that NDRO memories are typically linear-select or word-oriented, thereby requiring considerably more electronics and interconnections. This memory organization requires typically $2\sqrt{N}$ word select drivers, N diodes and $X \times Y + Z$ interconnections, compared to $4(N)^{1/4}$ drivers, $2\sqrt{N}$ diodes and $X + Y + Z$ interconnections for the DRO memory case. In addition, magnetic flux changes ($\Delta\phi$) are considerably less, thereby providing lower readout voltages so that more complex sensing and noise rejection circuits are required. Thus, since NDRO memories require substantially more electronics, their composite failure rates are higher, resulting in a lower mean time before failure.

CONCLUSIONS

1. The greatest benefit to be derived from the conventional memory parity bit (space redundancy) is more rapid (less time redundancy) detection of memory malfunctions.

2. Indication of memory malfunction is not sufficient; corrective action (generally programmed) should be provided.

3. In the NDRO memory, when used in whole-valued sampled data calculations, intermittent errors will generally result in a noisy data point. This will be smoothed or totally corrected in subsequent iterations. For the worst case of integration with respect to time, reasonableness checks based on the previous iteration will constrain the error.

4. In present computers wherein most of the memory electronics is implemented via discrete components and the memory stack is implemented via discrete cores, parity checking has been frequently used to detect errors in the readout of memory data. However, with the advent of batch fabricated memories (for example, planar and wire deposited film), integrated circuits, and large scale integrated circuits, the probability of multiple errors is no longer insignificant. Thus, this approach to memory integrity testing will need to be re-evaluated.

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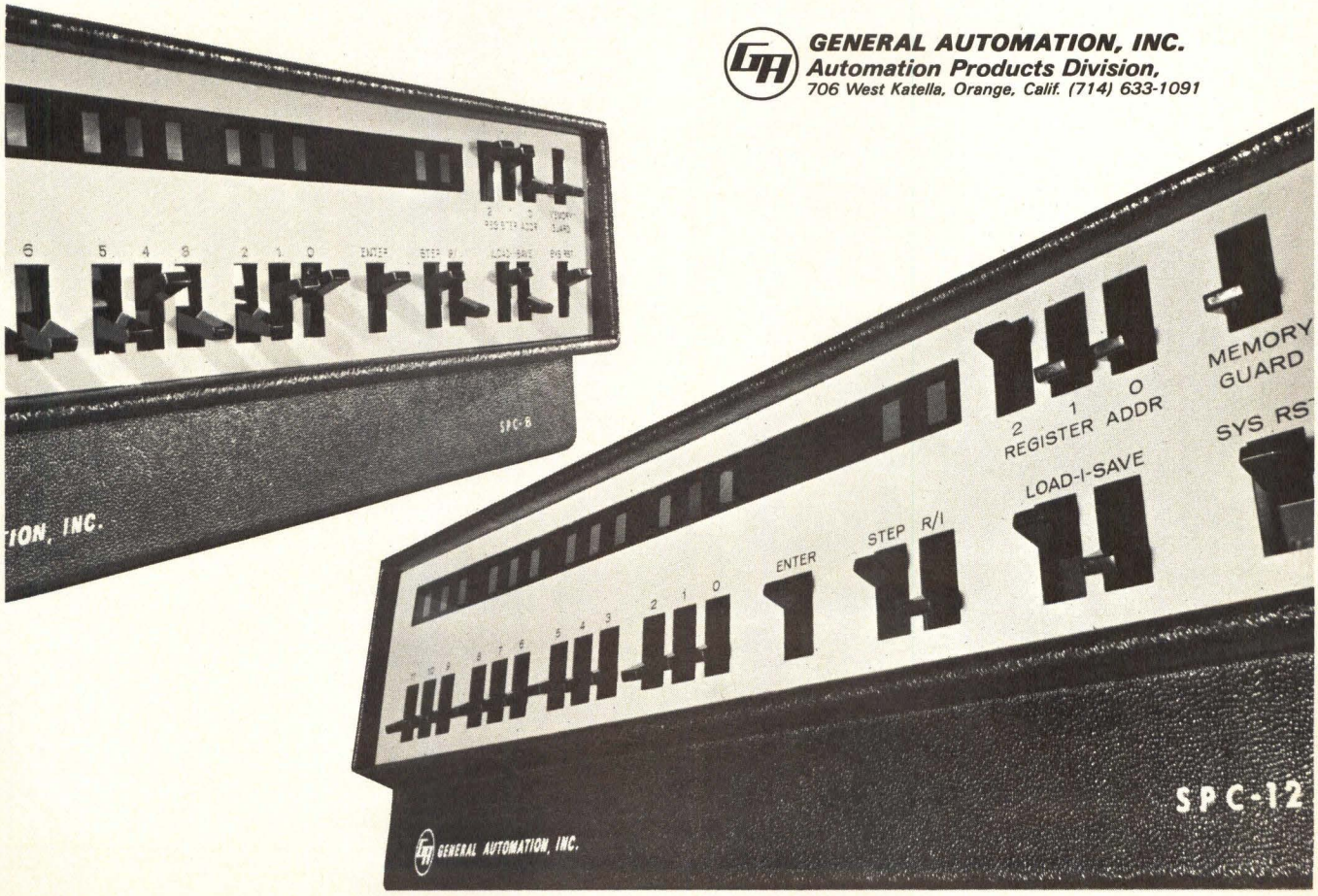

CIRCLE NO. 22 ON INQUIRY CARD

The development of the moving coil motor has significantly advanced servo designs. This has led to many new applications of servomechanisms in computer peripheral equipment.

POLES AND ZEROS IN PERIPHERALS*

Tom Fitzgerald

Honeywell Inc.
EDP Division
Waltham, Mass.

The introduction of the third generation of computers and their associated peripherals has done much to extend the application of servomechanisms. This article provides a review of the design and use of servomechanisms and describes an innovative design technique that Honeywell EDP has used in their peripheral equipment. It also discusses the advantages and the problems peculiar to servomechanisms and the tools and techniques of design. Lastly, new applications made possible by recently developed components such as the moving coil motor are given.

SERVOS

Before discussing components, it is convenient to review the block diagram of a servo (Fig. 1). The basic servo loop consists of an amplifier, motor, detector, and summing network which are connected so that the motor will turn until the detector produces a feedback voltage that cancels the input command. Useful output from the servo is taken from the motor shaft as indicated.

The detector is a transducer producing a voltage (for feedback) from a mechanical input. There are two general categories of detectors in common use: one produces a voltage proportional to position, the other produces a voltage proportional to velocity. The choice of transducer type is determined by the requirements of the application.

In general, the performance of a servo is related to the "stiffness" of the loop. If it has high gain then only a small error signal is needed to drive the motor; the output follows the input closely.

APPLICATION IN PERIPHERALS

Systems like this have been used for years in a great many applications—for controlling reels in tape drives, for regulating motor speeds, for controlling turn-and-bank in aircraft auto pilots, and for controlling temperature in buildings. In peripheral equipments, there is a certain type of motion that seems ideal for implementation by means of a servo. These are essentially start-stop types of motion—the spacing of paper in a line printer, the indexing of a card through a punch station, or the demand feeding of a document or a card. However, electric motors capable of producing the desired accelerations have only recently become available. (As a matter of interest, the time allotted for this type of motion usually is in the range of two to twenty milliseconds.)

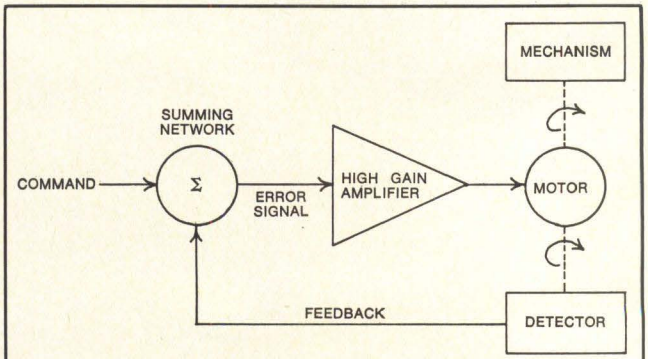

Fig. 1 Block diagram of a servo.

**This article is a reproduction of a paper published in the fall 1968 issue of the Honeywell Computer Journal.*

To achieve the accelerations needed, the earlier designer had a choice of three techniques: brake-and-clutch, hydraulic servos, or mechanical indexing schemes using such components as Genevas.

The most common problem with the brake-and-clutch is the wear of the brake and clutch faces. Many clutch facing materials have been investigated and this wear has been reduced, but for years the author carried a five mil shim in his wallet for resetting brake and clutch gaps. This was usually the first check made when visiting a site with reported difficulty.

Mechanical indexing schemes are possible but require a long development time and close manufacturing control. Such mechanisms typically involve cams or impacting surfaces which are subject to wear; the long development time must include extensive life testing for wear.

Hydraulic servos do not have the difficulties of the above techniques, but these types have to be accompanied by an overhead of pumps, fluid, filters, and plumbing.

MOVING COIL MOTOR

The moving coil motor is a recent innovation[1] which provides the designer with a motor having several times the acceleration of earlier motors (150,000 to 200,000 radians per sec^2 compared to 40,000 radians per sec^2). Fig. 2 and 3 are photographs of two versions of the motor: Fig. 2 is a disk or "printed circuit" motor and Fig. 3 is a model having a cylindrical coil. In each model, the rotor does not contain any iron, resulting in a rotor having a low moment of inertia and low self-inductance.

The magnetic energy stored in the rotor ($\frac{1}{2}$ LI^2) for a given current is therefore less, resulting in smaller inductive kicks during commutation and reduced arcing, leading to longer brush and commutator life. As will be seen later, the lower inductance of the rotor also eases the design of the servo.

VELOCITY SERVOS

The types of applications considered here are typical of position servos. For example, we are interested in moving the paper in a line printer one line or two lines or five lines; in each case the paper is to be moved to a new position. However, in actual practice it has been found that it is simpler to implement the design as a velocity servo. A typical block diagram is given in Fig. 4.

The servo system is as described before. The transducer is a tachometer which produces a dc output voltage proportional to angular velocity with its polarity determined by the direction of rotation. The command signal is derived from a flip-flop which is set by a start signal from the logic. Attached to the motor shaft or a shaft in the mechanism is a position indicator—in this case a disk with slots which permit light to pass through and focus on a photocell. When

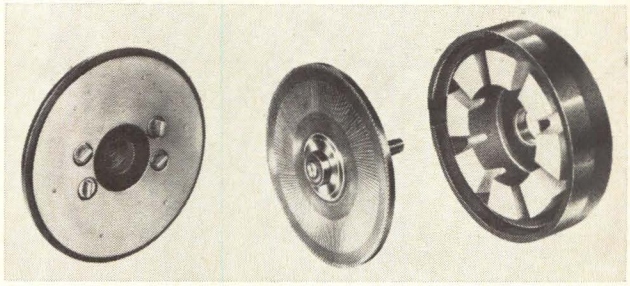

Fig. 2 Moving coil motor (disk).

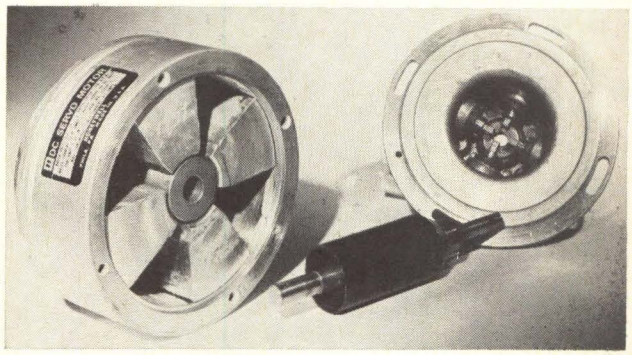

Fig. 3 Moving coil motor (cylindrical).

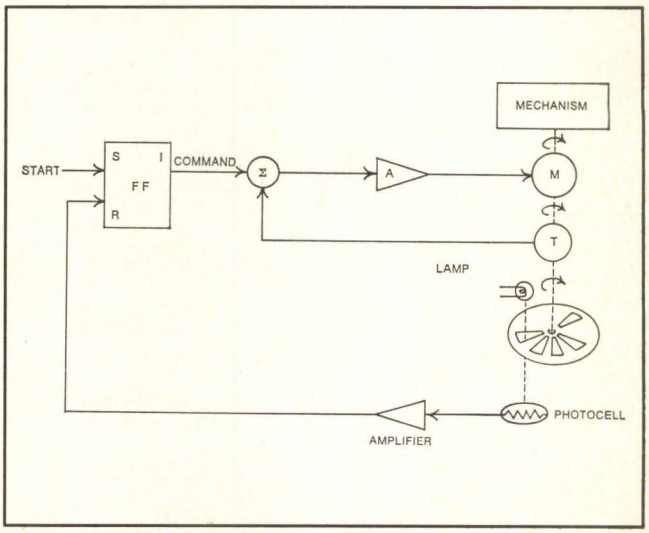

Fig. 4 Block diagram of a velocity feed servo.

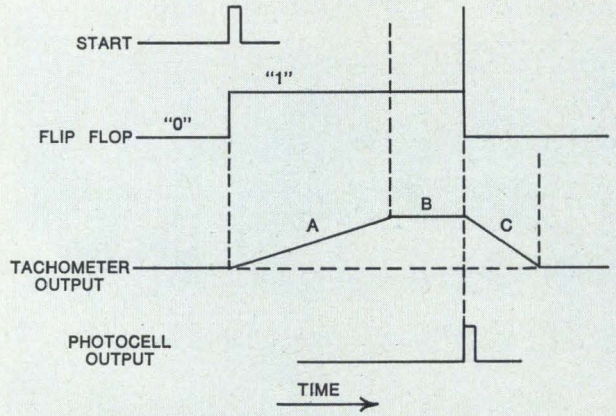

Fig. 5 Waveforms of the velocity servo.

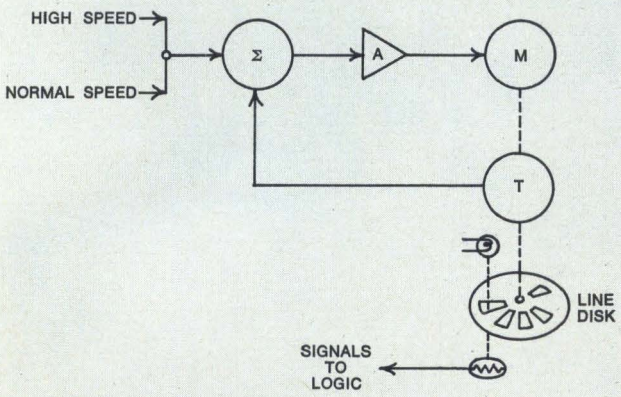

Fig. 6 Multispeed operation of a servo.

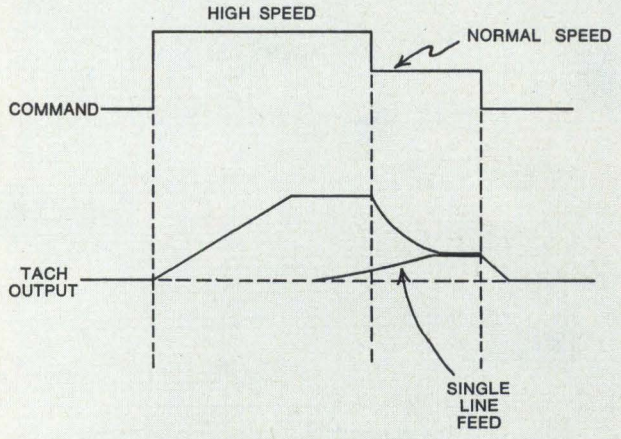

Fig. 7 Waveforms in a multispeed servo.

the system is commanded to start, the motor, mechanism, and disk come up to an angular velocity such that the tachometer output is almost equal to the command input voltage. This speed is maintained until the next slot in the disk comes between the lamp and the photocell, at which time the pulse from the photocell resets the flip-flop removing the command input to the servo. The waveforms are shown in Fig. 5. The tachometer output rises during interval A to a value almost equal to the command from the flip-flop, and then levels out at a constant voltage (and velocity) in region B. (This has another significance to be explained later.) After the stop command is given, the servo decelerates to halt in region C.

The point at which the system comes to rest is then determined by the light slot plus the distance the motor turns during the breaking period—interval C in the diagram. Since the tolerance on the light slot path can be accurately held, the other consideration in the accuracy of positioning is the repeatability of the braking action; the designer must evaluate this in his design.

ADVANTAGES OF A SERVO SYSTEM

Having arrived thus far, it is appropriate to list the advantages which the servo offers the designer as a tool.

1. It offers flexibility. One basic servo design for a card-picking mechanism is used with slight modifications throughout the Honeywell 123/223 Card Reader family (400,600,800, and 1050 cards per minute), and in the H-214 Reader Punch. The modifications for the different designs are accomplished by changing electric components.

2. Because of the feedback action, the response of the system is more uniform with varying loads—such as in different weights of paper forms in a printer, or in different heights of the input deck in a card reader.

3. The servos may be designed to accept standard logic inputs.

4. The response of the servo and, therefore, the motion of the mechanism may be controlled by shaping the command (by means of filters). Thus, we may want a picker knife to contact the card at a low initial velocity and then to accelerate it to a higher velocity.

5. The servo can be designed so that it requires adjustment infrequently or not at all.

6. Perhaps the most significant advantage of the servo in a system design is that it may be designed for multi-speed or bidirectional operation. This capability is not readily accomplished with the other techniques described earlier.

For example, if we want a paper feed to skip several lines, then time can be saved if this can be done at a higher velocity. A two speed paper-feed system is shown in Fig. 6 and the command and velocity waveforms are shown in Fig. 7. The logic is designed to

keep track of the number of lines to go. It should be noted that just before the servo reaches the line on which it is going to stop, the velocity is reduced to normal speed. The servo thus always stops from this speed so that the uniformity of stopping is maintained. The tachometer waveform for a single line feed is shown for comparison.

SERVO DESIGN

In some areas of engineering, a designer can be successful without being highly analytical—but not in servo mechanisms. The design of a servo system to meet tight performance specifications requires a detailed paper analysis.

Since the analysis of a servo is basically one of solving a system that is described by integro-differential equations, the designer uses the techniques developed for the solution of such systems, in particular, the Laplace transform. The Laplace transform reduces the solution of a system of differential equations to an algebraic manipulation of their coefficients. It provides the complete solution for the system—the transient response as well as the steady-state response. Since the transform is covered so well in the modern engineering literature, it will be enough here to sketch two particular methods in which it is used in the analysis and design of servos: the frequency-response analysis and the root-locus methods. Each technique has a particular class of problems for which it is best suited.

Since the servomechanism is a system having negative feedback, one of the major problems is to provide stability, i.e. to keep the system from oscillating. The mechanism of oscillation is easily visualized if we follow a signal around the loop (realizing that at different points of the loop the "signal" may be a voltage, a torque, or a motion). As the signal proceeds around the loop, it experiences delays due to filters, due to amplifier response, due to the inductive time constant of the motor winding, due to torque-to-inertia ratio and so on. If at any one frequency, the delays experienced in proceeding around the loop add up to 180°, and if there is a net power gain around the loop at that frequency, then the servo will oscillate because the negative feedback has become positive and excess power is returned to the starting point. One possible procedure then is to identify the delay producing elements and to control the loop frequency response so that the power gain will be less than one when the delay becomes 180°.

Many workers have developed techniques for the frequency analysis of feedback systems; the most well known is Bode's.[2] Bode's technique makes use of the fact that in most circuitry and mechanical systems, the amplitude of the frequency response is related to the phase response. If one is known, the other can be determined. In this technique the designer manipulates the frequency response although he is equally concerned with the phase response.

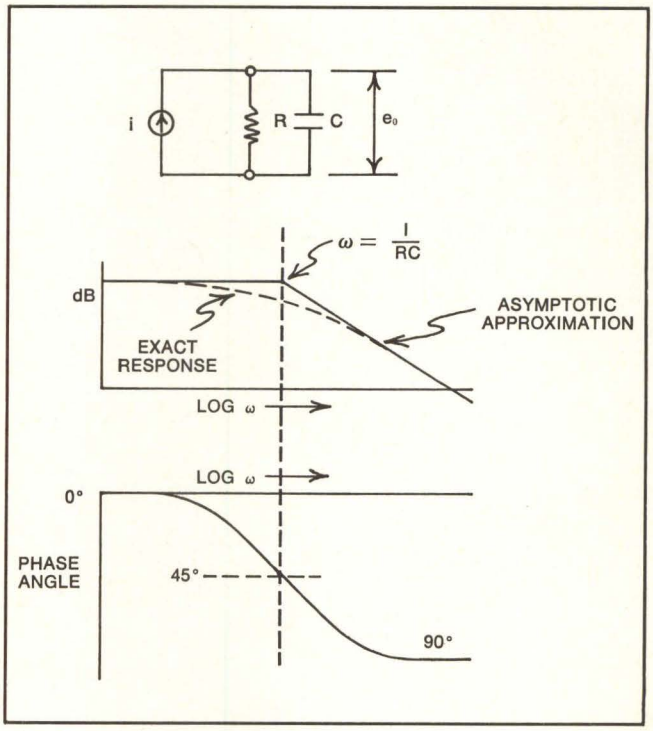

Fig. 8 Frequency and phase characteristics.

Fig. 8 illustrates this principle. A network driven by a current generator is shown; this might well be the equivalent circuit of the collector circuit of a transistor amplifier. If the transistor frequency cutoff is high enough to be neglected, then the output voltage, e_o, is given by

$$\frac{e_o}{i} = \frac{R}{1 + j\omega RC} \qquad \text{(Eq. 1)}$$

When the frequency gets high enough so that $\omega RC > 1$, the high frequency asymptotic approximation of the output voltage becomes

$$\frac{e_o}{i} \approx \frac{1}{j\omega C}$$

If the amplifier power gain (decibels) is plotted versus the logarithm of radian frequency, ω, then the frequency response may be approximated by two straight lines, one horizontal, the other with a slope of minus 6 dB per octave. The breakpoint occurs at:

$$\omega = \frac{1}{RC}$$

The curve shows the exact network response for comparison with the approximation.

At this point we should very simply sketch some of the essentials of Laplace transform theory. Equation 1 is a typical *system function*, i.e. the ratio of the output response of a network to its input stimulus. If the system function ever becomes infinite, then

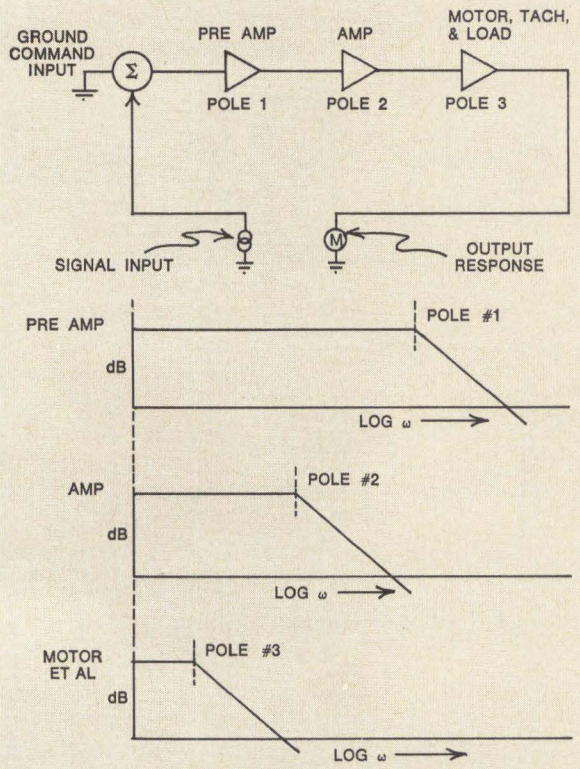

Fig. 9 Frequency analysis of a servo.

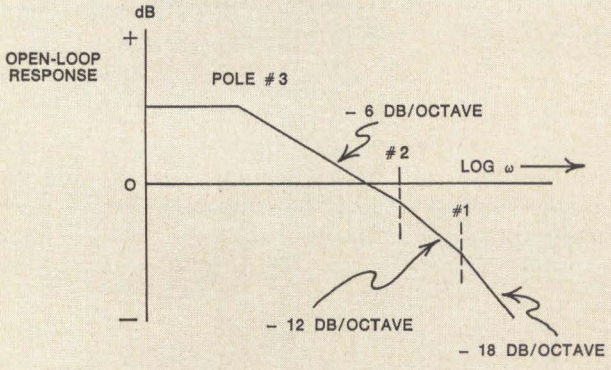

Fig. 10 Composite response of open loop.

we have a situation in which an infinitely large output is produced for no input at all—or, in other words, the system oscillates.

Mathematically, such an infinite system function is produced if the denominator is equal to zero. In Laplace transform theory, the frequency variable jω is replaced by the generalized frequency variable s, which is a complex variable equal to σ + jω. The denominator of Equation 1 then becomes 1 + RCs which can become zero if RCs equals —1. Thus we have an infinite response (a "pole" in the jargon) when the generalized frequency variable, s, has the value $-\frac{1}{RC}$

In Laplace notation we would say that the system function has a pole at:

$$s = -\frac{1}{RC}$$

In brief, the response of any system to an input stimulus is determined by the poles and zeros (values of variable s for which the numerator is zero) of the system function.

Fig. 8 also shows a plot of the phase angle of the response. Comparison of the phase angle and power gain curves indicates that when the frequency response is well down on the roll-off, the phase angle has flattened out at 90 degrees lagging.

If we investigate other networks we find that a slope of minus 12 dB per octave is accompanied by a phase shift of 180 degrees. A rising slope of 6 dB per octave has a phase shift of 90 degrees leading. In general, if the slope of the power gain is measured in units of 6 dB per octave, then each unit will have a phase shift of 90 degrees associated with it, the sign of the phase shift determined by whether the slope is rising or falling.

This particular method of plotting frequency response has other advantages. With cascaded elements, the "Bode" plot for the group may be obtained by adding the plots of the series elements. This technique is illustrated in Fig. 9 in which the design of a servo is tested for stability.

The servo loop is broken (in the designer's mind) and a variable frequency generator is inserted to pump a signal around the loop. The gain around the loop is to be checked to insure that it is less than one when the phase shift reaches 180 degrees. In the example shown, there are three poles, one each for the preamplifier, the amplifier, and the motor-tachometer combination; the designer has determined the Bode plot for each element. The complete open loop response can then be plotted by adding the three plots to obtain the result shown in Fig. 10. It is seen that as the frequency increases past each pole, the roll-off increases another 6 dB per octave (and the phase shift another 90 degrees). The servo will be stable, therefore, if the gain is adjusted so that the frequency response crosses the zero dB axis before the phase shift reaches 180 degrees (12 dB per octave slope).

It becomes obvious now that there are conflicting

requirements. A high gain is needed for a "stiff" servo, but too high a value will affect the stability. Fig. 11 illustrates how the maximum allowable gain of the system is determined by the relationship of the first pole to the other poles. If the second and third poles are further out, then a higher gain may be used since the zero dB axis is still crossed at a slope of 6 dB per octave.

And so the designer becomes a juggler of poles and gain. If he needs a tight servo loop (high gain) then the second and higher poles must be moved out. If this cannot be accomplished, the first pole must be moved to a lower frequency.

It may be evident from the above discussion that the designer normally works with the open loop response since this can be calculated directly from the circuit values; the closed loop response can only be obtained indirectly. Fig. 12 gives a useful approximation in which it is shown that the break-point of the closed loop response occurs at about the frequency of the zero dB crossing of the open loop response.

One significant fact is derived from Fig. 12 and the preceding discussion—the closed loop response is determined more by the location of the second lowest pole than the lowest pole. Thus it is possible to space paper in 17 milliseconds with a motor having a time constant of 50 milliseconds.

ROOT LOCUS TECHNIQUES

Frequency analysis methods are useful for the treatment of designs having simple poles on the real axis; root locus techniques are better suited for systems having complex poles.

This technique is based upon the fact that if the location of the poles and zeros of the open loop response are known, then the loci of the pole positions of the closed loop response are also known. Furthermore, from the performance requirements of the servo, the proper location of the poles and zeros of the closed loop response can be specified. The designer obtains the desired position by juggling the open loop poles and zeros and the loop gain.

To demonstrate: let the open loop response of a servo be expressed as

$$\text{O.L.R.} = KG(s) = \frac{K\,N(s)}{D(s)}$$

where K is the gain constant and G(s) is the frequency dependent portion of the response. G(s) is a fraction in which the numerator and denominator are polynomials in s, with the numerator of lower order than the denominator in practical cases.

The closed loop response is then given by.

$$\text{C.L.R.} = \frac{KG(s)}{1 + KG(s)} = \frac{K\,N(s)}{D(s) + K\,N(s)}$$

The zeros of the closed loop response are the zeros of the open loop response. The poles of the closed loop response are determined by setting

$$D(s) + K\,N(s) = 0$$

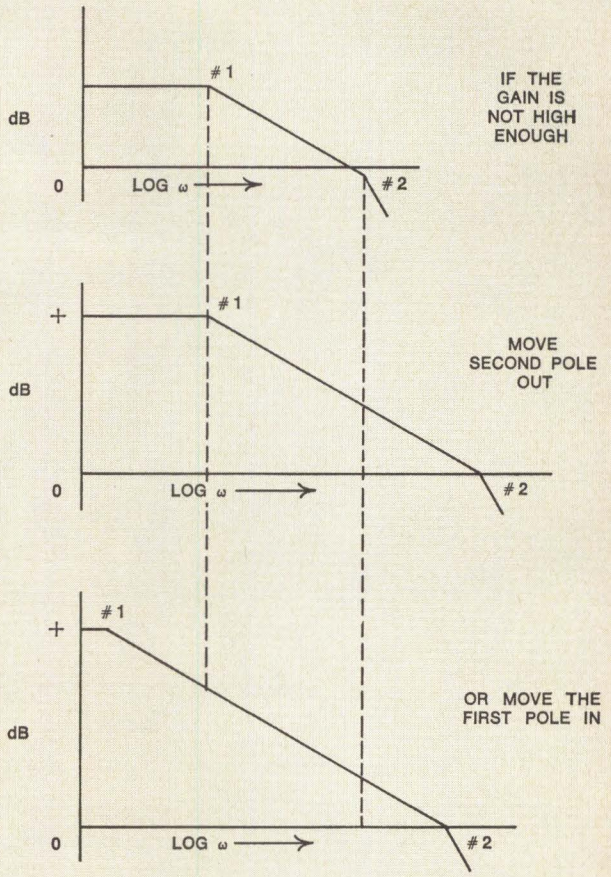

Fig. 11 Effect of pole position on permissible loop gain.

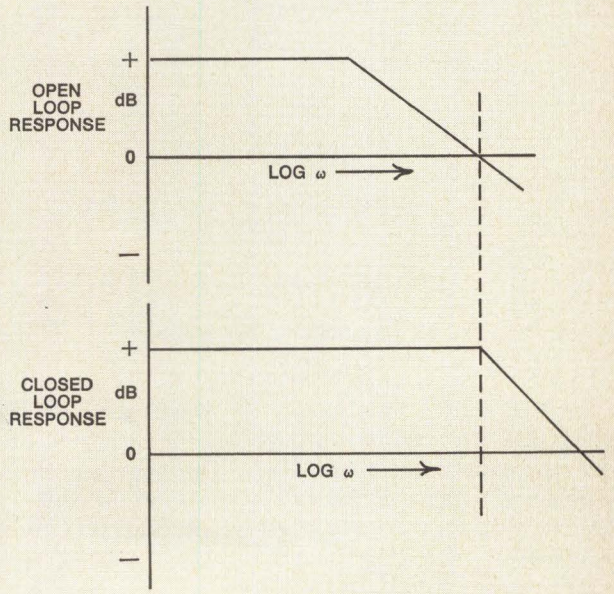

Fig. 12 Approximation of relationship of open loop to closed loop response.

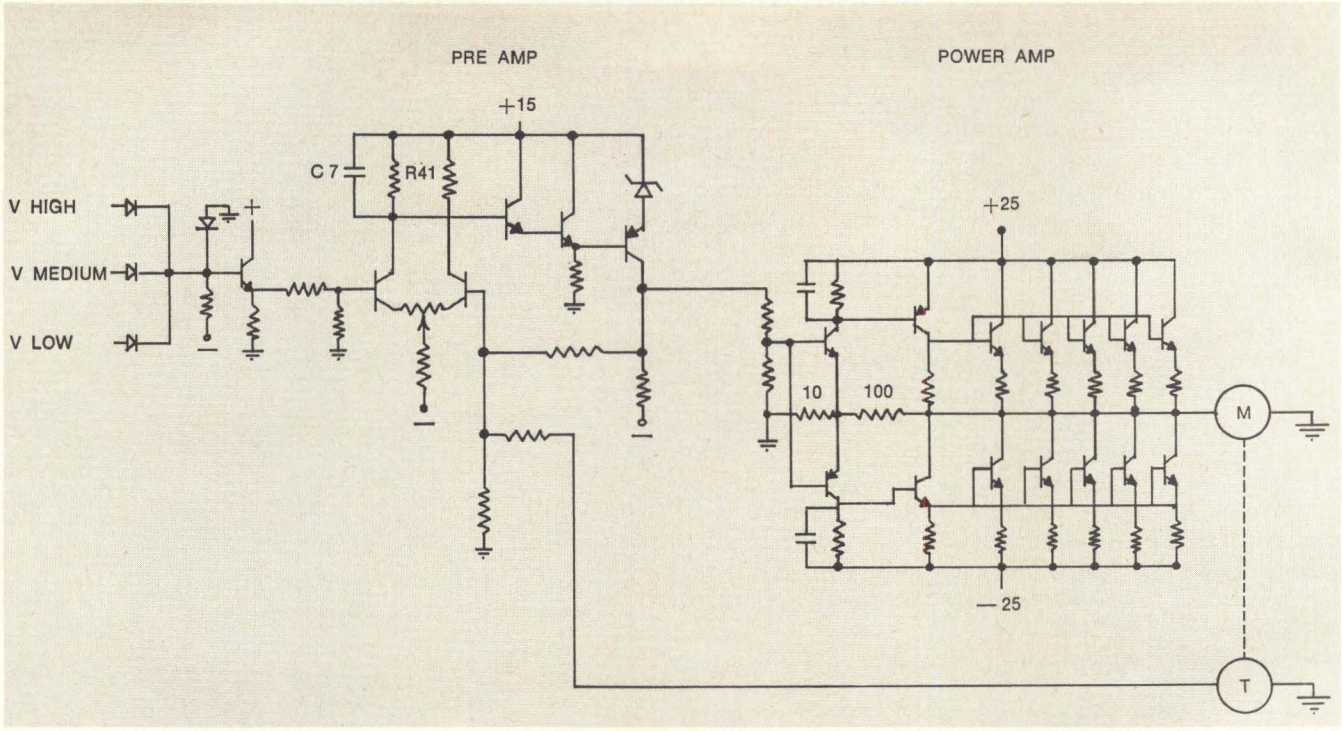

Fig. 14 Paper feed servo.

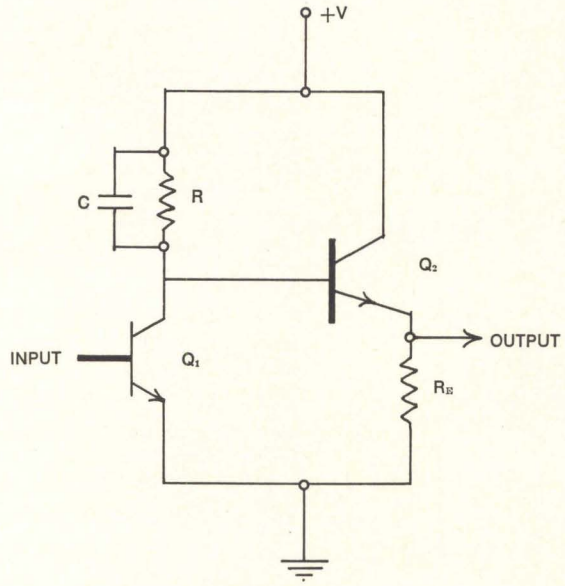

Fig. 13 Determining pole position.

Now it is seen that if the gain, K, is varied the poles will vary. The particular way in which the poles will vary is determined by the original pole and zero configuration of G (s). Tables of graphs of various pole-zero combinations are available for the designer and they are used just as tables of transforms are used.

DESIGN CONSIDERATIONS

As indicated above, the servo designer must be concerned with the loop gain and the positions of the poles (and zeros) of the loop response. Having settled on a configuration, a problem of some concern is that of producing the design in manufacturing, particularly in the light of the variation of transistor parameters. (It is interesting to note that the early work of Bode and others was directed toward the design of amplifiers that would have reproducible specifications in the face of varying tube parameters.) Some of the design techniques are described briefly below.

Because the bandwidth of the transistors is large compared to the "bandwidth" of the motor, practically unlimited gain is available to the designer at no expense other than the cost of the components. However, the gain of transistors is one parameter that has a wide spread for most transistor types; in a typical lot, the ratio of gain of the highest gain transistor to the gain of the lowest gain transistor might be 5 to 1. The designer therefore uses the transistor for raw gain and stabilizes it by using localized feedback. Such feedback might take place within one stage (e.g. by using emitter resistors) or may be taken around several stages. Typically a design may break the "high gain amplifier" shown in Fig. 1 into two amplifiers, a preamplifier and a power amplifier, each amplifier being a negative feedback amplifier for stability of gain. In recent years, the preamplifier function has been taken over by integrated circuit operational amplifiers now on the market.

The general technique for stabilizing the pole (and zero) positions is to use circuit configurations that are independent of the transistor parameters. Thus, in Fig. 13, the pole position is determined by the RC product of the components in the collector circuit of Q_1. The input impedance of Q_2 is in parallel with the collector load; by choosing a low impedance level for R and C, and by obtaining a high input impedance for Q_2 by using an emitter follower configuration, this input impedance may be neglected. The number of such techniques is limited only by the ingenuity of the designers.

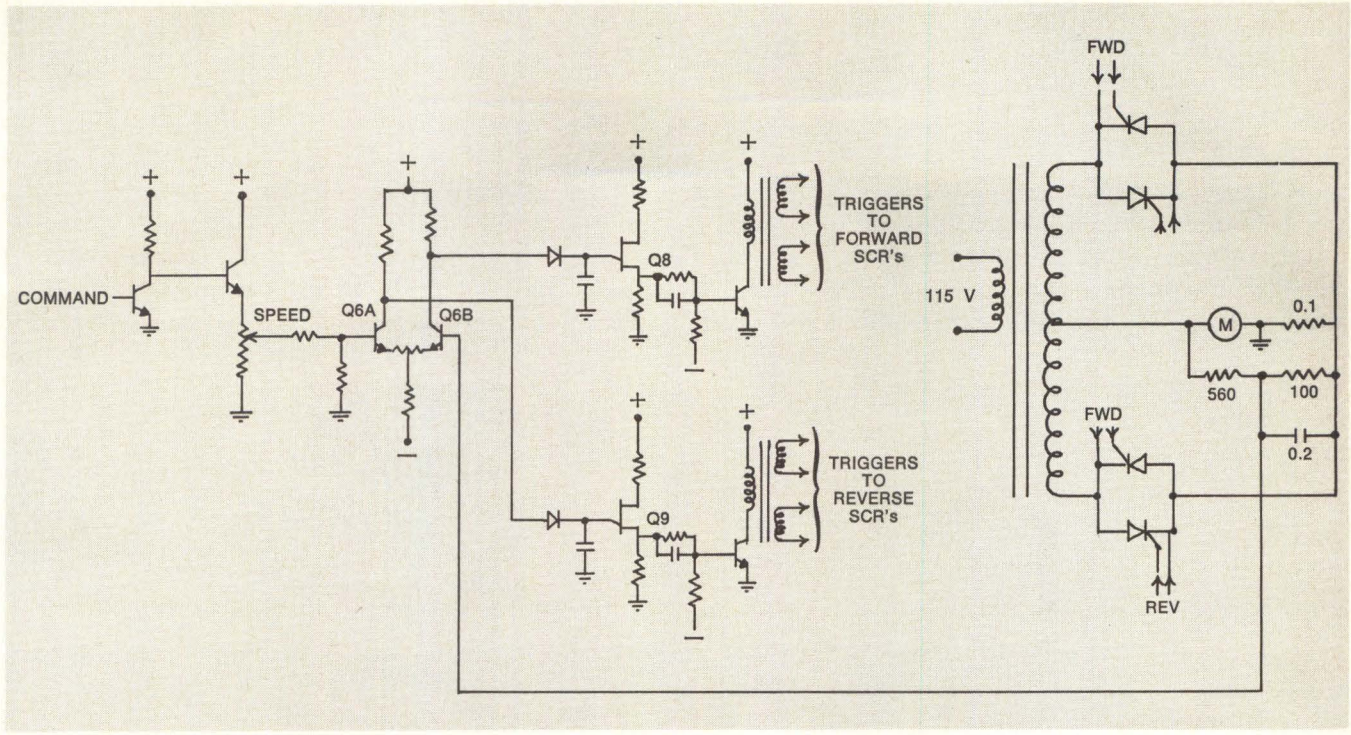

Fig. 15 Picker motor servo.

PAPER FEED SERVO

Fig. 14 shows a simplified schematic of the paper feed servo used in the Type 122 and 222 printers. The salient features that should be noted are:

1. Three input commands produce the three paper feed speeds.
2. Use of a preamplifier with its gain stabilized by negative feed back determined by C7 and R41.
3. A brute force class B power amplifier, each half stabilized independently (by the RC network in the collector of the input stage) since both halves of the amplifier never conduct simultaneously.

Other problems peculiar to such servos which do not show up on the schematic are the problems of bringing the high power from the power supply to the power amplifier and to the motor. Some attention has to be given to the grounds and to the dress of the cables because of the loop inductance and the possibility of feedback to the low power stages.

PICKER MOTOR SERVO

Fig. 15 gives a simplified schematic of the picker motor servo used in the Type 123 and 223 Card Readers and in the 214 Reader Punch. This servo obtains its power gain through the use of silicon controlled rectifiers (SCR's) connected in a full wave configuration. In addition, the tachometer has been eliminated as the velocity transducer; the back emf of the picker motor itself is used to obtain a voltage proportional to velocity.

The differential stage Q6A and Q6B performs the summing function, with the command applied to the base of Q6A and the velocity feedback voltage to the base of Q6B. The output of this stage permits either Q8 or Q9 (the unijunction oscillators) to fire. Each unijunction oscillator fires the appropriate set of SCR's to make the motor accelerate or decelerate.

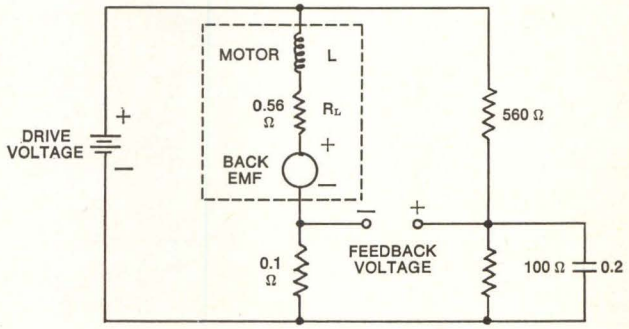

Fig. 16 Elimination of the tachometer.

Fig. 16 illustrates the technique for eliminating the tachometer. A bridge circuit is used so that the drive voltage does not appear at the feedback terminals; however, a voltage proportional to the back emf of the motor is present at the terminals. A capacitor is added to one leg of the bridge to compensate for the rotor inductance.

CONCLUSION

The Honeywell 222 Printer, 223 Card Reader, and 214 Reader Punch were among the first peripherals to use the moving coil motor for rapid start-stop actions. In all applications the motors were used in velocity servomechanisms. The excellent performance of hundreds of these servos in the field has justified the original decision to use these motors.

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2. Bode, H. W., "Network Analysis and Feedback Amplifier Design," D. Van Nostrand Company, Inc., New York, 1948.

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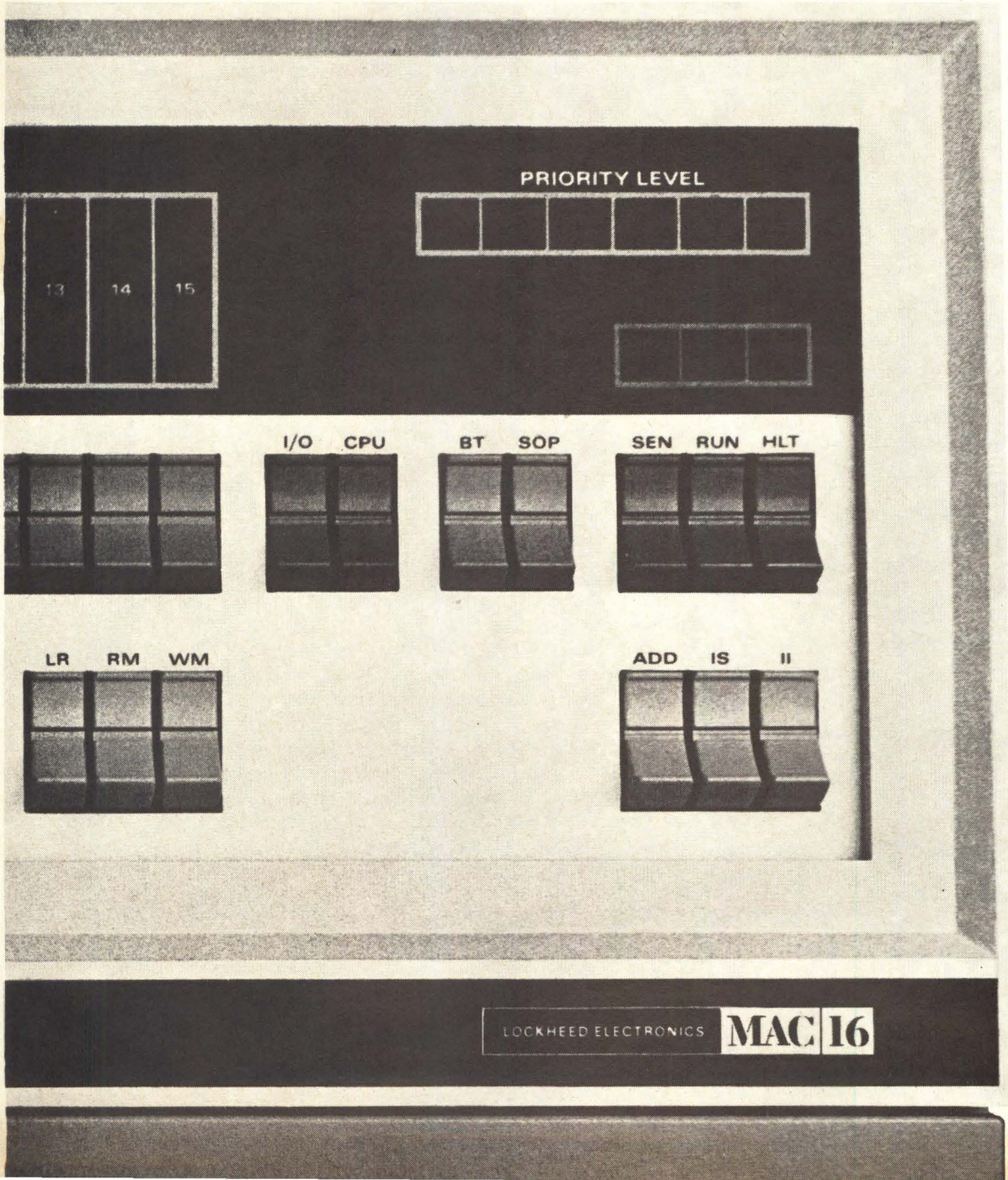


Let MAC do it.

In the May 1968 issue of Computer Design, a design algorithm was developed for the synthesis of sequential machines using Moore's model. In this paper, the Mealy model is used for the synthesis of a sequential machine.

THE SYNTHESIS OF SEQUENTIAL CIRCUITS

M. A. Ettinger

Mark Computer Systems, Inc.
Plainview, N. Y.

In a paper[1] co-authored by myself, a design algorithm was developed which could be used in the synthesis of "any" sequential machine, utilizing any family of microcircuit elements (RTL, DTL, TTL, etc.) with any type memory element (one-shot, T-flip flop, S-R flip flop, J-K flip flop, etc.). This algorithm and some design examples were developed utilizing Moore's sequential machine model[2].

In this paper another model, the Mealy sequential machine model[3], is explained and its similarities and differences are discussed. Furthermore, the method associated with the manner in which the states of the sequential circuit are coded is shown to be one of the most difficult problems associated with synthesis of sequential circuits, greatly affecting the circuit complexity.

For those not immediately familiar with the algorithm which was presented in the reference above [(1)], it is detailed below.

THE ALGORITHM

In general the synthesis (or design) of a sequential circuit consists of the following steps, as shown in the flow diagram of Fig. 1.

Sequential Machine Synthesis Algorithm

1. Translation of the verbal problem into a state diagram.

A pictorial presentation is prepared which contains a number of circles, each of which indicates a state the machine may be in. These circles are numbered from 1 to n, where n indicates the number of possible conditions that may be encountered.

2. Reduction of the number of states and construction of a reduced state diagram.

Since the initial state diagram is merely a translation of the verbal statement of the problem, it does not necessarily yield an economical minimum state representation. A reduced state diagram is obtained by examining whether several states are equivalent to each other and may thus be merged into a single state.

3. Construction of the reduced state table from the reduced state diagram.

Since, from this point on, it is more convenient to work with tabular representations of the state diagram, a table is constructed which consists of one row per state. It indicates the present state number in the first column, the "next state" number in the second or third column (depending upon whether one arrived in that particular next state when the input to the machine was 0 or the input was 1) and the output of the machine corresponding to each state in the last column.

4. Assignment of the states of the memory elements to the internal states of the machine.

We normally number states in a manner that is convenient to us, such as 1, 2, 3 . . . n, but since our storage elements are usually binary devices, we must code the state in binary form; 1 may correspond to 000, 2 may correspond to 001, etc., or any other coding as may be desired as long as enough binary digits

are used to represent the total number of states to be encountered.

5. Selection of the memory element to be used in the synthesis, i.e. relays, S-R flip flops, J-K flip flops, etc.

This selection will depend upon speed considerations, cost or apparent functional suitability.

6. Generation of the excitation table for the particular problem.

Subsequent to the state assignment it is known how many memory elements are required, but it is not known how they are to be interconnected or "excited" to take on the various states in the proper sequence as required by the original statement of the problem. Entries are placed into the excitation table in accordance with the needs of the "present state to next state transition" input requirements of the particular memory element selected.

7. Generation of the memory element input or excitation equations.

The excitation table contains the information which is required to obtain a Karnaugh Map (or equivalent) logic minimization, thus obtaining the excitation equation for each logic element.

8. Generation of output equations.

Since outputs are to be obtained only in particular states, a similar process as in 7 is used to obtain the output equation.

9. Draw circuit configuration.

As shown in step 1 of the algorithm, it is first necessary to translate the verbal problem into a state diagram. In most design problems, the choice of using the Moore model or the Mealy model is left entirely to the discretion of the logic designer. However, an understanding of both methods, coupled with design experience will usually predicate which model to be used.

COMPARISON OF MOORE AND MEALY MODELS

The definition of a sequential machine is now given: A finite sequential machine, M, may be described as a 5-tuple of variables I, S, Z, G, f such that:

1) $I = I_1\ I_2 \ldots\ldots I_n$ is the finite non-empty set of inputs,
2) $S = S_1\ S_2 \ldots\ldots S_n$ is the finite non-empty set of internal states, the secondary states,
3) $Z = Z_1, Z_2 \ldots\ldots Z_n$ is the finite non-empty set of outputs, and
4) g is the next state function which maps $I \times Si$ into $S_i + j$

This four-part definition is identical for either the Moore or Mealy machine. The only difference is their definition in association with the output definition. The output function is defined as:

5a) f is the output function which maps $I \times S$ into Z for the Mealy model, and
5b) f is the output function S into Z for the Moore model.

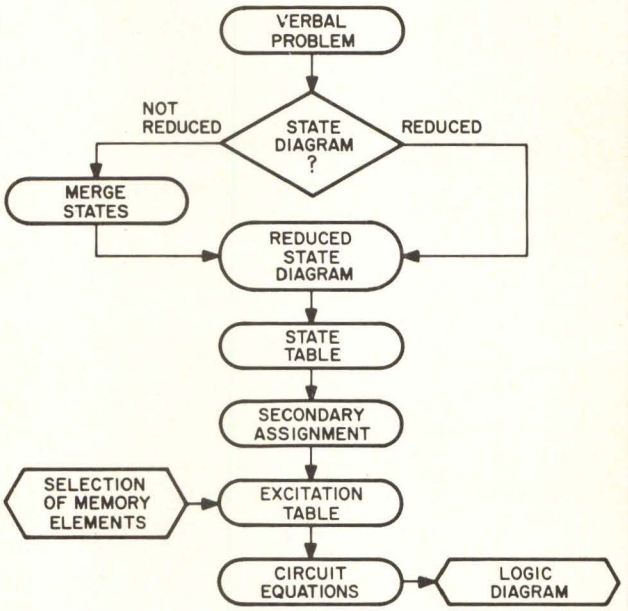
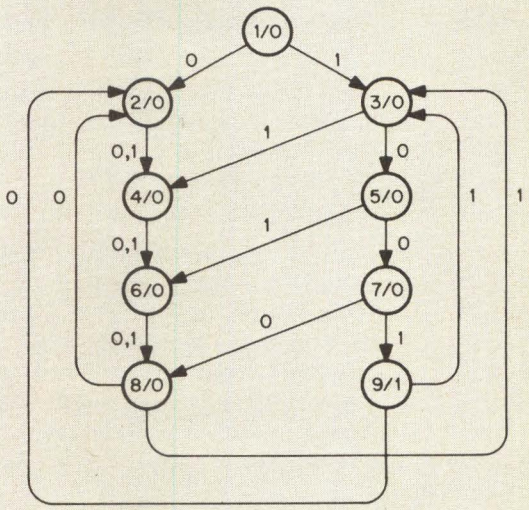


Fig. 1 Sequential Machine Synthesis Algorithm.



(a) State Diagram.

P.S.	N.S 0	N.S 1	Z
1	2	3	0
2	4	4	0
3	5	4	0
4	6	6	0
5	7	6	0
6	8	8	0
7	8	9	0
8	2	3	0
9	2	3	1

(b) State Table.

Fig. 2 Moore Model.

Therefore, we see that we can derive the following output equations:
(1) Z = f (Si, Ii), is the output equation for the Mealy machine, whereas
(2) Z = f (Si) is the output equation for the Moore machine.

Note that the output associated with a Moore model is solely dependent upon the present state of the sequential machine, while the output associated with the Mealy model is a function of both the present input Ii and the present state Si.

In order to examine the differences associated with the two models let us design the following circuit.

Example 1: Construct the state diagram and state table for a sequence detector with the following specifications.

An input sequence 1001 produces an output of 1, while all other sequences give an output of zero. The circuit is to examine all groups of four pulses. Assume the circuit is initially reset.

The Moore model is constructed in Fig. 2.

For the state diagram in Fig. 2, we see that states 8 and 9 are reached after the fourth pulse with state 9 having an associated output of 1. In addition, notice that the fifth pulse starts the examination of the next four pulses. Before we examine the Mealy model, let us draw the input/output timing diagram shown in Fig. 3.

Realize, in addition, that this nine state machine would require four memory elements. The block diagram is shown in Fig. 4.

For the same example we construct the Mealy model as shown in Fig. 5.

The notation used in the Mealy model state diagram is Xi/Zi, denoting that the output is associated with the present input in addition to that of the present state. Similarly, the state table must reflect this, and hence the output column must show the association with the present input as well as the present state.

For this state diagram, realize that the output is coincident with the fourth input pulse. As before, we draw the timing diagram as shown in Fig. 6.

Since the Mealy model contains only seven (7) states, the synthesis of this machine would require three (3) memory elements as shown in Fig. 7.

Although one memory element is saved, notice that the output associated with the Mealy machine occurs

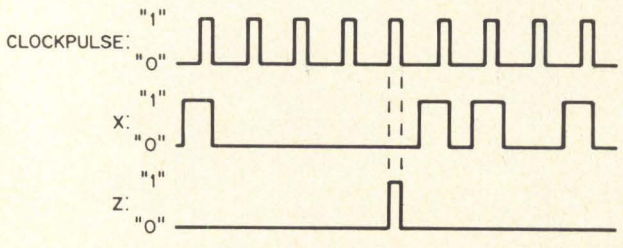


Fig. 3 Timing Diagram—Moore Model.

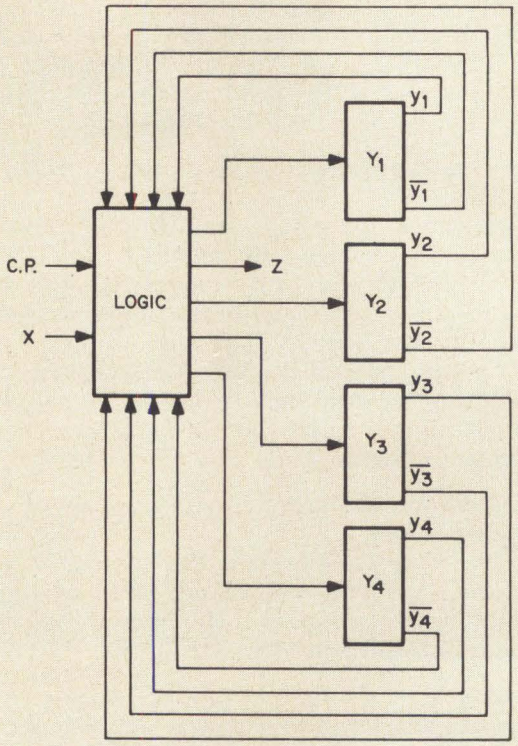
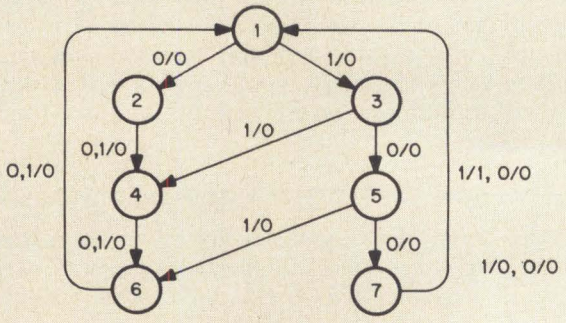


Fig. 4 Block Diagram—Moore Model.



(a) State Diagram.

P.S	N.S		Z	
	0	1	0	1
1	2	3	0	0
2	4	4	0	0
3	5	4	0	0
4	6	6	0	0
5	7	6	0	0
6	1	1	0	0
7	1	1	0	1

(b) State Table.

Fig. 5 Mealy Model.

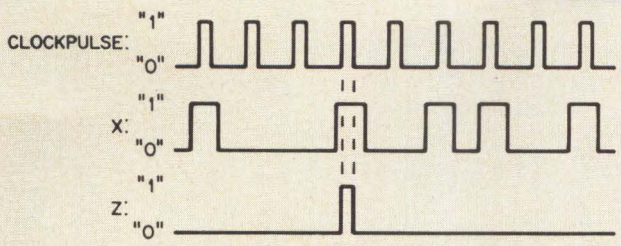


Fig. 6 Timing Diagram—Mealy Model.

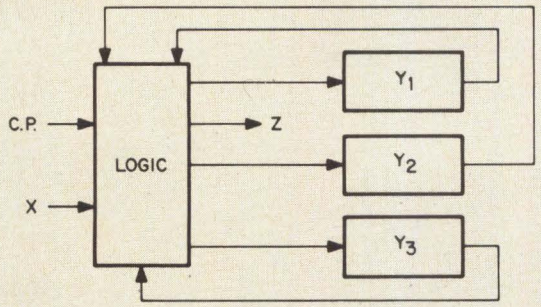


Fig. 7 Block Diagram—Mealy Model.

	N.S		Z	
P.S	0	1	0	1
1	4	3	0	0
2	6	3	0	0
3	5	2	0	0
4	2	5	0	1
5	1	4	0	0
6	3	4	0	0

Fig. 8 Reduced Mealy State Table.

		N.S		Z	
	P.S	0	1	0	1
1→	000	011	010	0	0
2→	001	101	010	0	0
3→	010	100	001	0	0
4→	011	001	100	0	1
5→	100	000	100	0	0
6→	101	010	100	0	0

Fig. 9 Secondary Assignment Table—Assignment #1.

To Change		Required
Qn	Qn+1	Input T
0	0	0
0	1	1
1	1	0
1	0	1

Fig. 10 T-FF Excitation Table.

in coincidence with input pulse number 4. Should the desired output be coincident with input pulse number 5, the Mealy output could be delayed one clockpulse, requiring an additional memory element; therefore, requiring four (4) exactly as in the Moore design.

In general, a Moore machine can always be converted into a Mealy machine and vice versa. A Mealy machine, however, will usually require less states and therefore may be synthesized with a number of memory elements that are less than or equal to the number required for a Moore type synthesis.

Therefore, if the designer has the freedom of choice of selecting the synthesis method to be employed, he usually selects the Mealy method for it might yield a solution requiring fewer memory elements. However, a more important factor which influences the complexity of the circuit is the manner in which the states of the sequential circuit are coded. This is known as the secondary assignment.

SECONDARY ASSIGNMENT

In the design of any sequential circuit, one of the most important steps is the assignment of the binary variable to the states which represent the internal structure of the machine. Since the number of possibilities grow profusely with the number of internal states, it is almost impossible unless, of course, the design engineer has a digital computer at his disposal for each circuit design, to try all possible assignments in order to find the most economical solution.

In order to fully understand the significance of the secondary assignment, consider the following example:

Example 2:

Let us suppose that steps 1 through 3 of the algorithm yielded the reduced Mealy state stable shown in Fig. 8. It is obvious that the six internal states can be coded and assigned in many ways ($8!/2! \approx 2 \times 10^4$). Let us choose just two.

Assignment 1:

Choosing a straight binary coded assignment yields the secondary assignment table of Fig. 9.

As per the algorithm, the next step is to generate the excitation table and the design equations.

Assuming that the choice of memory elements is T-flip flops, and referencing the excitation table for T-flip flops as shown in Fig. 10, we generate the excitation table for the problem as shown in Fig. 11.

P.S.			N.S.						Z	
			X=0			X=1				
y_1	y_2	y_3	T_1	T_2	T_3	T_1	T_2	T_3	X=0	X=1
0	0	0	0	1	1	0	1	0	0	0
0	0	1	1	0	0	0	1	1	0	0
0	1	0	1	1	0	0	1	1	0	0
0	1	1	0	1	0	1	1	1	0	1
1	0	0	1	0	0	0	0	0	0	0
1	0	1	1	1	1	0	0	1	0	0
1	1	0	ø	ø	ø	ø	ø	ø	ø	ø
1	1	1	ø	ø	ø	ø	ø	ø	ø	ø

Fig. 11 Excitation Table—Assignment #1.

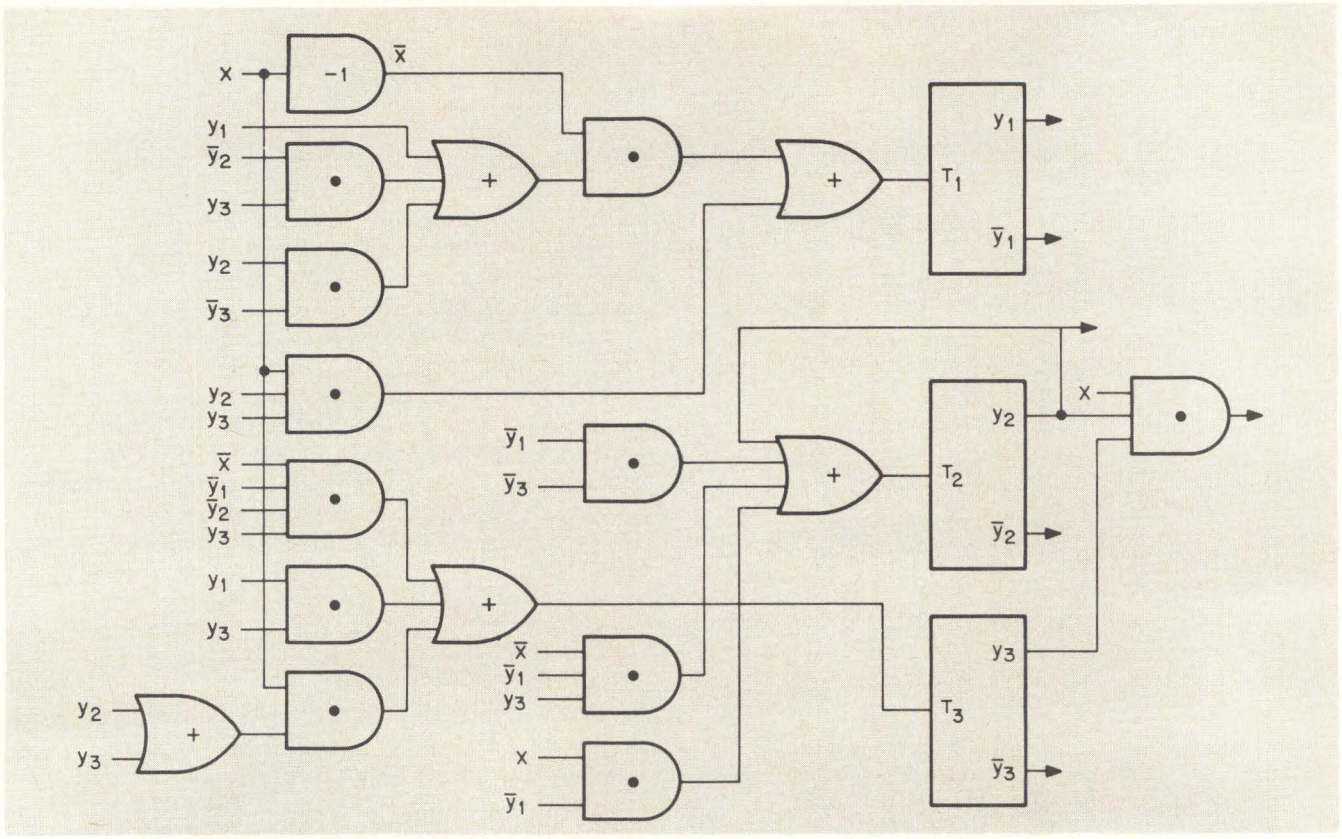


Fig. 12 Circuit Configuration—Assignment #1.

The design excitation equations derived from Fig. 11 are given below:

$$T_1 = \bar{x}(y_1+\bar{y}_2y_3+y_2\bar{y}_3)+\bar{x}y_2y_3$$
$$T_2 = \bar{x}y_1\bar{y}_3+x\bar{y}_1+y_2+\bar{y}_1y_3$$
$$T_3 = \bar{x}y_1y_2\bar{y}_3+x(y_2+y_3)+y_1y_3$$
$$Z = xy_2y_3$$

The circuit is configured in Fig. 12.

Assignment 2:
Now we consider a second assignment, whose selection was not made in an arbitrary manner but through a relatively straight-forward algebraic procedure. The state table is shown in Fig. 13.

Utilizing T-FF's as the memory element again, the excitation table is derived, as shown in Fig. 14.

The excitation equations are derived from Fig. 14 and are given below:

$$T_1 = \bar{X}$$
$$T_2 = \bar{x}y_3xy_2$$
$$T_3 = \bar{y}_2$$
$$Z = xy_1\bar{y}_2\bar{y}_3$$

The circuit is configured in Fig. 15.

Upon comparison of the circuit configurations for assignments 1 and 2, Figs. 12 and 15 respectively, it is seen that assignment #1 yields a much more complicated solution. Assignment #1 is realizable with 10-2 input gates, 6-3 input gates, 2-4 input gates, 1-inverter and 3-T-flip-flops whereas assignment #2

P.S.		N.S.		Z	
		0	1	0	1
1	010	100	000	0	0
2	001	110	000	0	0
3	000	101	001	0	0
4	100	001	101	0	1
5	101	010	100	0	0
6	110	000	100	0	0

Fig. 13 State Table—Assignment #2.

P.S.			N.X.		Z	
			x=0	x=1		
y_1	y_2	y_3	x		x=0	x=1
0	1	0	110	010	0	0
0	0	1	111	001	0	0
0	0	0	101	001	0	0
1	0	0	101	001	0	1
1	0	1	111	001	0	0
1	1	0	110	010	0	0
0	1	1	øøø	øøø	ø	ø
1	1	1	øøø	øøø	ø	ø

Fig. 14 Excitation Table—Assignment #2.

is realizable with 2-2 input gates, 1-4 input gate, 1-inverter and 3-T-flip-flops. Obviously quite a savings in both circuit complexity and—above all—cost!

The question at hand is now—How was assignment #2 obtained? The excitation equations for assignment #1 are fairly complicated; notice that each input excitation equation is "dependent" upon all three flip-flop variables (y_1,y_2,y_3). For assignment #2, however, the excitation equations are relatively simple; notice

that T_1 does not depend on y_2 or y_3 and T_2 and T_3 are not dependent on y.

The method used to obtain this assignment is an algebraic procedure called Partition Theory[4-5].

SECONDARY ASSIGNMENTS UTILIZING PARTITION THEORY

The partition theory method utilized in obtaining a secondary assignment may or may not yield an optimum assignment. The optimum assignment can only be obtained by the exhaustive method of trying each independent assignment. The partition theory method assignment, however, yields excitation equations with minimum self-dependency; that is where the excitation equations are dependent on as few variables as possible. Where this method fails is that a minimum self-dependency equation may not be a minimum solution.

For example, consider an eight state machine which requires three memory elements with dependent variables y_1, y_2 and y_3. Suppose an assignment is made such that T_1 is dependent solely on the input X, and internal variable y_1 in the form

$$T_1 = f(x,y_1) = xy_1 + \bar{x}\bar{y}_1$$

If another assignment could be found which has greater dependency, say T_1 dependent upon x, y_1,y_2 and y_3 in the form

$$T_1 = f(x_1y_1,y_2,y_3) = \bar{x}_1y_1y_2y_3, \text{ then}$$

the latter solution is "more-minimum" even though it has a greater variable dependency.

However, as a general method, the use of partitions in forming a secondary assignment yields a solution in much simpler form than the brute-force approach, as shown by Example 2.

Consider the following definitions:

Definition 1: A partition, denoted by π, on any set, S, is a collection of disjoint subsets of S such that their set union is S. The subsets of π are called the block of π.

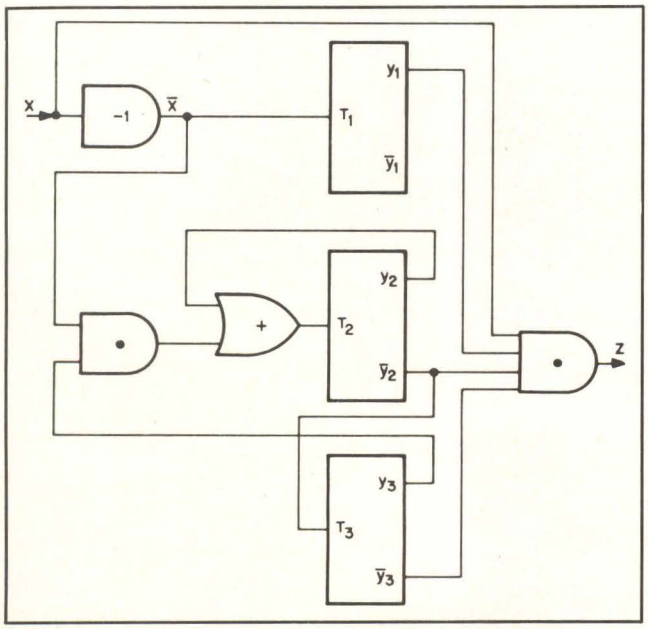


Fig. 15 Circuit Configuration—Assignment #2.

For the state table of Example 2

$$\pi_1 = (\overline{1, 2, 3}; \overline{4, 5, 6}) \quad \text{and}$$
$$\pi_2 = (\overline{1, 6}; \overline{3, 4}; \overline{2, 5}) \quad \text{are partitions on S}$$

In addition, every set S has two trivial partitions, the null partition and the unity partition.

The null partition is $\pi\{\phi\} = (\bar{1};\bar{2};\bar{3};\bar{4};\bar{5};\bar{6})$ whereas the unity partition is $\pi\{I\} = (\overline{1,2,3,4,5,6})$ for Example 2.

Definition 2: A partition π, on a set of states S, of a sequential machine M is said to have substitution property (S.P.) with respect to M if for any two present states S_i and S_j belonging to the same block of π and any input I, the next states $I \otimes S_i$ and $I \otimes S_j$ are again contained in a common block of π. This common block may or may not be the same block containing S_i and S_j.

For Example 2

$\pi_1 = (\overline{1, 2, 3}; \overline{4, 5, 6})$ and $\pi_2 = (\overline{1, 6}; \overline{3, 4}; \overline{2, 5})$ have S.P.

DETERMINATION OF PARTITIONS WITH S.P.

To determine the basic partitions with S.P. for a given machine M:

(1) Start by identifying any two distinct states S_1 and S_2.

(2) Then identify the pairs of states S_{1k}, S_{2k} which S_1 and S_2 go to if we apply the input, K = 1, 2, . . . m.

(3) To this set of states, add those pairs which can be identified by the transitive law: that is, if S_i and S_j are identified and so are S_j and S_k, we have to identify S_i and S_k.

(4) Repeat the process looking up the new identifications induced by the new pairs, and if after R steps, the R+1 step does not yield any new identifications, we have constructed a partition π, on S which has S.P. on machine M.

(5) If there does not exist a non-trivial partition which has S.P., then this process stops after identifying all states of M.

For a machine M with n states, we must try n(n-1)/2 distinct pairs of states to determine that there does not exist a π with S.P. on M.

ALGEBRAIC PROPERTIES OF PARTITIONS

Definition 3: We say π_1, on S is smaller than π_2 or equal to π_2 on S, $\pi_1 \leq \pi_2$, if and only if each block of π_1 is contained in a block of π_2.

For Example 2

$$\pi_1 = \{ \overline{1, 2, 3}; \overline{4, 5, 6} \}$$
$$\pi_2 = \{ \overline{1, 6}; \overline{3, 4}; \overline{2, 5} \}$$
$$\pi_1 > \pi_2$$

Thus the smallest π is one which contains only blocks with single elements ($\pi = 0,1, \ldots m$).

This is the null partition denoted as ϕ.

The largest π is one which contains one block ($\pi = 0, 1, \ldots m$) which is the unity partition denoted as I. In addition to the basic partitions there may exist additional partitions defined below.

Definition 4: The least upper bound (l u b) of a pair of partitions is defined as $\pi_1+\pi_2=\pi_3$ the set-union of all blocks of π_1 and π_2. If π_1 and π_2 have S.P., then so does π_3.

For Example 2

$$\begin{aligned} \pi_1 &= (\overline{1, 2},\ \overline{3; 4},\ \overline{5, 6}), \\ \pi_2 &= (\overline{1, 6};\ \overline{3, 4};\ \overline{2, 5}) \qquad \text{and therefore} \\ \pi_1+\pi_2 &= (\overline{1, 2, 3, 4, 5, 6}) \end{aligned}$$

Definition 5: The greatest lower bound (g l b) of a pair of partitions is defined as $\pi_1 \cdot \pi_2=\pi_3$ the intersection of the blocks of π_1 and π_2. If π_1 and π_2 have S.P., then so does π_3.

For Example 2

$$\begin{aligned} \pi_1 &= (\overline{1, 2, 3};\ \overline{4, 5, 6}), \\ \pi_2 &= (\overline{1, 6};\ \overline{3, 4};\ \overline{2, 5}) \qquad \text{and therefore} \\ \pi_1 \cdot \pi_2 &= (\overline{1}, \overline{2}, \overline{3}, \overline{4}, \overline{5}, \overline{6}) \end{aligned}$$

We now have enough information to find the partitions with S.P. The state table from Example 2 is shown in Fig. 8, and utilizing the above procedures we obtain the following partitions. We start by identifying pairs.

$\overline{1, 2} \rightarrow \overline{3, 4, 6} \rightarrow \overline{4, 5};\ \overline{2, 3} \equiv \overline{2, 3, 4, 5} \rightarrow$
$\overline{1, 2, 5, 6};\ \overline{2, 3, 4, 5} \equiv \overline{1, 2, 3, 4, 5, 6} \equiv \pi\{I\}$

$\overline{1, 3} \rightarrow \overline{4, 5};\ \overline{2, 3} \equiv \overline{1, 2, 3};\ \overline{4, 5} \rightarrow \overline{2, 3};\ \overline{4, 5, 6} \equiv$
$\overline{1, 2, 3};\ \overline{4, 5, 6} \equiv \pi_1$

$\overline{1, 4} \rightarrow \overline{2, 4};\ \overline{3, 5} \equiv \overline{1, 2, 4};\ \overline{3, 5} \rightarrow \overline{2, 4, 6};\ \overline{3, 5} \rightarrow$
$\overline{1, 2, 4, 6};\ \overline{3, 5};\ \overline{1, 5};\ \overline{2, 4} \equiv \overline{1, 2, 3, 4, 5, 6} \equiv \pi\{I\}$

$\overline{1, 5} \rightarrow \overline{1,4};\ \overline{3,4} \equiv \overline{1, 3, 4, 5} \rightarrow \overline{1, 2, 4, 6};\ \overline{2, 3, 4, 5} \equiv$
$\overline{1, 2, 3, 4, 5, 6} \equiv \pi\{I\}$

$\overline{1, 6} \rightarrow \overline{3, 4} \rightarrow \overline{2, 5} \rightarrow \overline{1, 6};\ \overline{3, 4} \equiv \overline{1, 6};\ \overline{2, 5};\ \overline{3, 4} \equiv \pi_2$

$\overline{2, 3} \rightarrow \overline{2, 3};\ \overline{5, 6} \rightarrow \overline{1, 3};\ \overline{4} \equiv \overline{1, 2, 3};\ \overline{4};\ \overline{5, 6} \rightarrow$
$\overline{1, 2, 3};\ \overline{4, 5, 6} = \pi_1$

$\overline{2, 4} \rightarrow \overline{2, 6};\ \overline{3, 5} \rightarrow \overline{3, 6};\ \overline{3, 4};\ \overline{2, 5} \equiv \overline{2, 3, 4, 5, 6} \rightarrow$
$\overline{1, 2, 3, 4, 5, 6} = \pi\{I\}$

$\overline{2, 5} \rightarrow \ldots = \pi_2$
$\overline{2, 6} \rightarrow \ldots = \pi\{I\}$
$\overline{3, 4} \rightarrow \ldots = \pi_2$
$\overline{3, 5} \rightarrow \ldots = \pi\{I\}$
$\overline{3, 6} \rightarrow \ldots = \pi\{I\}$
$\overline{4, 5} \rightarrow \ldots = \pi_1$
$\overline{4, 6} \rightarrow \ldots = \pi_1$
$\overline{5, 6} \rightarrow \ldots = \pi_1$

Therefore, the basic partitions with S.P. are

$$\begin{aligned} &\pi\{I\},\ \pi\{\phi\} \\ &\pi_1 = \{\ \overline{1, 2, 3};\ \overline{4, 5, 6}\ \} \\ &\pi_2 = \{\ \overline{1, 6};\ \overline{2, 5};\ \overline{3, 4}\ \} \end{aligned}$$

As per the requirements specified for determining additional partitions we try

$$\begin{aligned} &\pi_1 + \pi_2 = \pi\{I\} \quad \text{and,} \\ &\pi_1 \cdot \pi_2 = \pi\{\phi\} \end{aligned}$$

Therefore, there exists only two non-trivial partitions with S.P. on this machine.

To utilize the partitions with S.P in the secondary assignment, the following theorem must be satisfied (4).

Theorem 1:
A sequential machine M with n states has a binary variable assignment of length $S = (\log_2 n)$, which can be split into 2 parts, such that the first k variables, lckcs, and s-k variables can be computed independently, if and only if, there exists two non-trivial partitions $\pi 1$ and $\pi 2$ which satisfies that

$$\begin{aligned} &(1) \quad \pi_1 \cdot \pi_2 = \pi\{\phi\} \\ &(2) \quad [\log_2 \#(\pi_1)] + [\log_2 \#(\pi_2)] = S \end{aligned}$$

Where $\# \pi_i$ denotes the number of blocks or subsets in π_i. The proof is contained in (5).

If (1) is satisfied, but not (2) an assignment is still possible by adding additional variables.

For the partitions of Example 2, the conditions of Theorem 1 are:

$$\begin{aligned} &(1) \quad \pi_1 \cdot \pi_2 = \{\overline{1}; \overline{2}; \overline{3}; \overline{4}; \overline{5}; \overline{6}\} : \text{satisfied;} \\ &(2) \quad [\log_2 (\#\pi_1)] = [\log_2 (2)] = 1 \\ &\qquad [\log_2 (\#\pi_2)] = [\log_2 (3)] = 2 \\ &\quad s = [\log_2 m] = [\log_2 (6)] \quad = 3 \\ &\qquad \therefore (2) \text{ is satisfied} \end{aligned}$$

Therefore, the assignment is made such that

a) Y_1 distinguishes the blocks of π_1
b) Y_2 Y_3 distinguishes the blocks of π_2

The assignment is shown in Fig. 16.

Y_1	Y_2	Y_3	Present State
0	1	0	1
0	0	1	2
0	0	0	3
1	0	0	4
1	0	1	5
1	1	0	6

Fig. 16 State Assignment.

An assignment such as this yields the following variable dependency:

$$\begin{aligned} T_1 &= f(x, y_1) \\ T_2 &= f(x, y_2, y_3) \\ T_3 &= f(x, y_2, y_3) \end{aligned}$$

Note that the design excitation equations obtained in Example 2 are less dependent than the functional dependency equations indicate. The functional dependency equations yield the maximum reduced dependent solutions, whereas the design equations may be less dependent.

Consider the following example:

Example 3:
Given the Moore state table of machine M_1 shown in Fig. 17, we first find all partitions with substitution property (S.P.)

P.S.	X 1	X 2	X 3	X 4	X 5	Z
1	2	1	5	8	3	0
2	1	2	6	7	4	0
3	4	3	6	6	1	0
4	3	4	5	5	2	0
5	5	6	3	4	7	0
6	6	5	4	3	8	0
7	7	8	4	2	5	0
8	8	7	3	1	6	1

Fig. 17. State Table Machine M_1.

For machine M, the computation of the partitions with S.P. are shown below:

$\overline{1,2} \rightarrow \overline{1,2}; \overline{5,6}; \overline{7,8}; \overline{3,4} = \pi_1$

$\overline{1,3} \rightarrow \overline{2,4}; \overline{1,3}; \overline{5,6}; \overline{6,8} \rightarrow \overline{1,3}; \overline{2,4}; \overline{5,6,8} \rightarrow \overline{1,2,3,4}; \overline{5,6,7,8} = \pi_2$

$\overline{1,4} \rightarrow \overline{2,3}; \overline{1,4}; \overline{8,5} \rightarrow \overline{7,6} \rightarrow \overline{1,4}; \overline{2,3}; \overline{5,8}; \overline{6,7} = \pi_3$

$\overline{1,5} \rightarrow \overline{2,5}; \overline{1,6}; \overline{3,5}; \overline{7,8} \rightarrow \overline{1,2,3,5}; \overline{4,8} \equiv \pi\{I\}$

$\overline{1,6} \rightarrow \overline{2,6}; \overline{1,5} \ldots = \pi\{I\}$

$\overline{1,7} \rightarrow \overline{2,7}; \overline{1,8}; \overline{4,5}; \overline{2,8}; \overline{3,5} \rightarrow \overline{1,2,7,8}; \overline{3,4,5} \rightarrow \overline{1,2,7,8}; \overline{3,4,5,6} = \pi_4$

$\overline{1,8} \rightarrow \overline{2,8}; \overline{1,7}; \overline{5,3}; \overline{8,1}; \overline{3,6} = \pi_4$

$\overline{2,3} \rightarrow \overline{1,4}; \ldots = \pi_3$
$\overline{2,4} \rightarrow \overline{1,3}, \ldots = \pi_2$
$\overline{2,5} \rightarrow \overline{1,5}; \ldots = \pi\{I\}$
$\overline{2,6} \rightarrow \overline{1,6}; \ldots = \pi\{I\}$
$\overline{2,7} \rightarrow \overline{1,7}; \ldots = \pi_4$
$\overline{2,8} \rightarrow \overline{1,8}; \ldots = \pi_4$
$\overline{3,4} \rightarrow \overline{5,6}; \overline{1,2}; \ldots = \pi_1$
$\overline{3,5} \rightarrow \overline{1,7}, \ldots = \pi_4$
$\overline{3,6} \rightarrow \overline{1,8}, \ldots = \pi_4$
$\overline{3,7} \rightarrow \overline{1,5}, \ldots = \pi\{I\}$
$\overline{3,8} \rightarrow \overline{1,6}; \ldots = \pi\{I\}$
etc.

In this way, we obtain that there are four non-trivial partitions with S.P. on machine M.

$$\pi_1 = \{\overline{1,2}; \overline{3,4}; \overline{5,6}, \overline{7,8}\}$$
$$\pi_2 = \{\overline{1,2,3,4}; \overline{5,6,7,8}\}$$
$$\pi_3 = \{\overline{1,4}; \overline{2,3}; \overline{5,8}; \overline{6,7}\}$$
$$\pi_4 = \{\overline{1,2}; \overline{7,8}; \overline{3,4,5,6}\}$$

Since the sums and products do *not* yield any new partitions, we have thus computed all S.P. partitions on machine M.

The requirements of Theorem 1 are examined.

$\pi_1 \cdot \pi_2 = \pi_1$ $\quad$ $\pi_2 \cdot \pi_3 = \pi_2$
$\pi_1 \cdot \pi_3 = \pi\{\phi\}$ $\quad$ $\pi_2 \cdot \pi_4 = \pi_1$
$\pi_1 \cdot \pi_4 = \pi_1$ $\quad$ $\pi_3 \cdot \pi_4 = \pi\{\phi\}$

Therefore $\{\pi_1, \pi_3\}$ and $\{\pi_3, \pi_4\}$ satisfy requirement 1) of Theorem 1, while only $\{\pi_3, \pi_4\}$ satisfy requirement 2).

The assignment is therefore:

Y_1Y_2 distinguishes blocks of π_3, and
Y_3 distinguishes blocks of π_4.

The assignment is shown in Fig. 18.

Y_1	Y_2	Y_3	Present State
1	0	0	1
0	1	0	2
0	1	1	3
1	0	1	4
0	0	1	5
1	1	1	6
1	1	0	7
0	0	0	8

Fig. 18 Assignment of Machine M_1.

The dependency of this assignment utilizing J-K flip-flops is

$$J_1 = f\ (x, y_1, y_2)$$
$$K_1 = f\ (x, y_1, y_2)$$
$$J_2 = f\ (x, y_1, y_2)$$
$$K_2 = f\ (x, y_1, y_2)$$
$$J_3 = f\ (x, y_3)$$
$$K_3 = f\ (x, y_3)$$

Again this is the maximum reduced self-dependency.

CONCLUSION

The assignments to these examples are by no means unique, nor does the author claim them to be optimum. Reiterating, the secondary assignment is one of the most difficult problems associated with the synthesis of sequential circuits greatly affecting the circuit complexity and, although the partition-theory method does not always yield an optimum solution, it normally allows the logic designer to obtain a less complex circuit.

The variable dependency is always consistent with the memory element selection; that is, no matter what the memory element is, all of its input equations have the same variable dependency.

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APPLICATION NOTE

How to Specify a Special Purpose Core Memory System

Bryan W. Rickard

Electronic Memories, Inc.
Hawthorne, Calif.

This application note provides general information on core memory systems that should be known to anyone contemplating using one. Particular emphasis is given to the practical question: How do you adequately specify a special purpose system?

What To Look For

Naturally, the most economical way to buy a core memory system is to select an off-the-shelf unit, in production, with proven design standards and field reliability data. Thus, the first step in selection of any product is to discuss your requirement with all suitable vendors. Most application or sales engineers are not only well versed about their own company's products, but are also usually quite familiar with competitive types, and are quickly able to analyze your needs and determine whether any existing system can meet it.

If a standard memory system is not available to meet your needs, discuss your requirement with the sales engineer in detail and give him a few days to think it over. He will come back with suggestions and advice for implementing your particular system and will probably save you money and trouble by applying the experience gained by his association with other customers.

Table 1 lists the principal requirements which should be specified when considering a core memory system. You should have some idea of your requirements for each of these particulars when you shop for a memory.

The following paragraphs discuss each item of Table 1 describing the various possibilities and trade-offs.

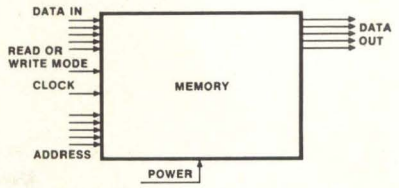
Addressing Mode

The usual internal organization of a core memory is such that a number of cores, comprising one memory "word," are accessed in parallel at every memory cycle. This gives an optimum relationship between magnetics cost and electronics cost.

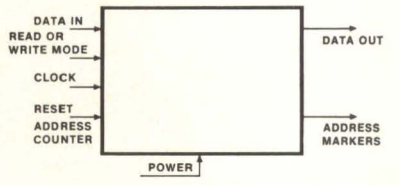
Any one of the total capacity of memory words is equally capable of being accessed and is defined by the address presented to the memory. This organization is known as "random-by-word, parallel-by-bit".

All normal applications of memory systems use the random-access parallel memory shown in Fig. 1a. In special cases the serial memory (Fig. 1b) may offer advantages.

Other addressing modes are possible. For instance, by giving the memory circuits a counting capability, a "serial-by-word, parallel-by-bit" memory may be obtained. This has the advantage that, once started, it will access successive addresses without requiring them to be explicitly defined at the memory address inputs.



(a) Block diagram of a random access parallel-organized memory.



(b) Block diagram of a serial access memory.

Figure 1

TABLE 1

Addressing Mode	Size and Weight
Capacity	NDRO or DRO?
Signal Functions	Workmanship and Design Standards
Speed	Quality Control
Signal Characteristics	Maintainability
Power	Documentation
Environmental Requirements	Warranty and Service
RFI Provisions	Price and Delivery
Testing	

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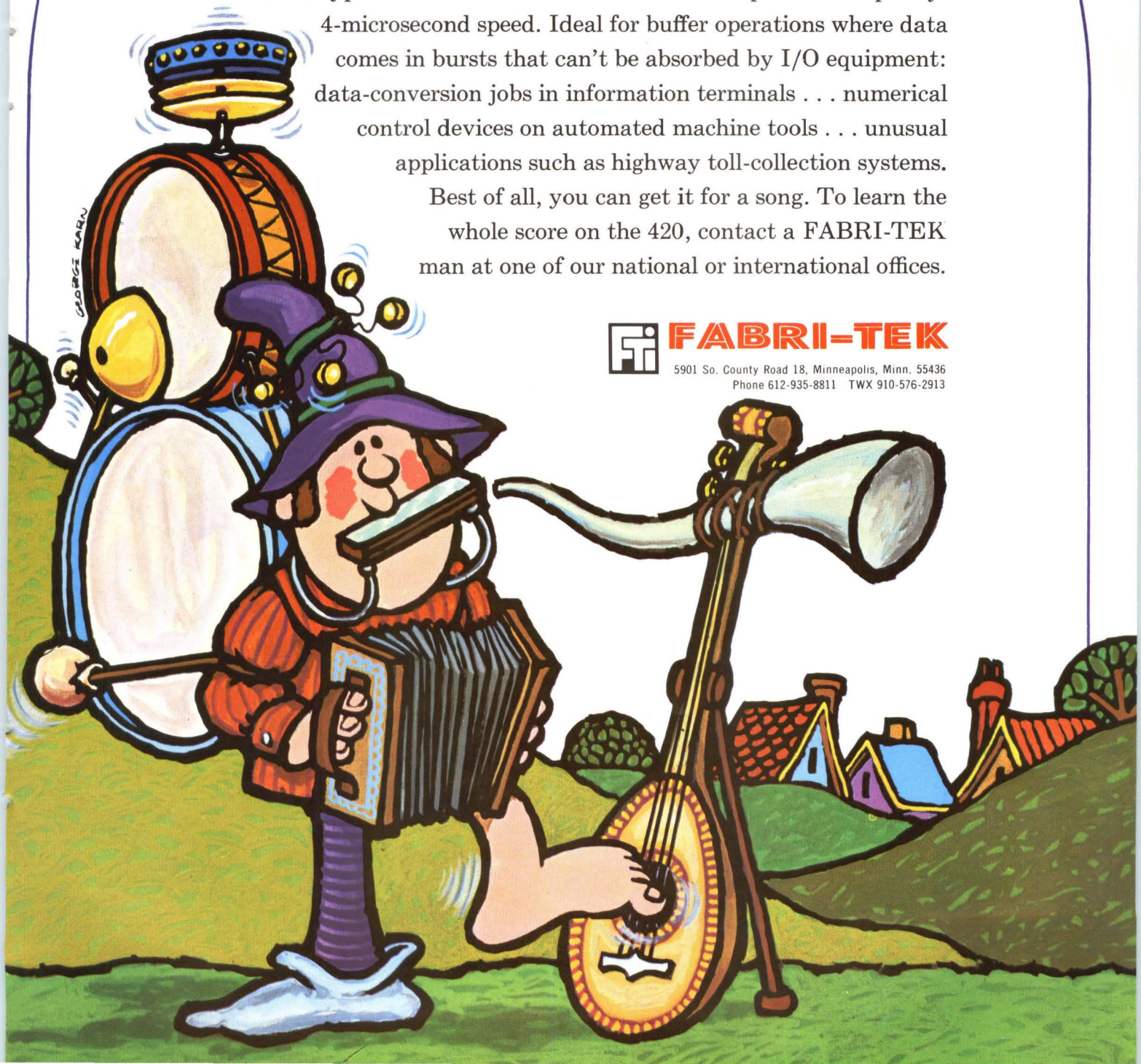

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A fully serial memory is often required for data storage and retrieval where only one information channel is to be processed—this is often the case in space-craft applications. Such a system may be obtained by applying serial/parallel conversion processes to a parallel-organized memory, but an attractive alternate for low-power, high reliability systems is the use of magnetic switching techniques for accessing the core store. In such memories, ferrite core ring switches or current-steering switches perform the triple functions of address decoding, sequencing, and storing.

Consideration of accessing mode leads to the next parameter to be specified, the capacity of the system.

Capacity

Specify the required word length in bits and quantity of words required (for a bit serial memory, just state the total number of bits). Economical word lengths for the average system lie between 16 and 72 bits, with the longer word lengths used where quantity of data handled in a given time is at a premium. Quantity of words is usually in exact 2″, with "N" ranging roughly between 10 and 16.

If your requirements are not within these limits, don't worry—there are many economical ways of implementing special capacity requirements and your sales engineer contact will undoubtedly suggest some of them.

Signal Functions

The function of signals to the memory will depend on your particular requirements. Your first discussion with a sales engineer may change your ideas, but the following signals are typical:

Data Out.—The one function that is common to all memory systems is output of stored data. A serial memory will provide a stream of data on one channel; a parallel memory will put out data on many channels simultaneously.

Data In.—All memories except those used purely for fixed storage require channels for input data, either serial or parallel.

Clocks.—It is conceivable for a memory to be free running, i.e. to read out stored data continuously without external control. Such a memory would be very difficult to interface, so all practical core memories usually operate in response to input clock signals. These may be supplied at regular or irregular rates up to the maximum inherent speed of the memory.

Modes.—If the clock signal is regarded as telling the memory when to perform an operation, the mode signal tells the memory what operation to perform. The two basic modes of memory operation are read and write. Many memory systems have just one mode channel, which is held, say, true for read, and false for write. Another useful mode is split cycle, which is a combination of the two half-cycles whereby useful information is read out by the first pulse, and new information is stored in the same core by the second pulse. This mode is considerably faster than using a normal two-pulse read operation followed by a normal two-pulse write operation, but extra hardware may be required to implement it. Other modes may be devised whereby some specified bits of a parallel word are read-restored while others write new data, or certain address sequences may be accessed in an automatic indirect addressing mode. Such features may be built into a custom memory system and are often offered as options on standard equipment.

Addresses.—In all random-access memories, the user must define the address he wishes to read out of or write into. These are always defined in binary code on "n" channels for a 2″ word memory.

Resets.—In serially accessed memories, the user usually requires to start at a known address. Rather than specifying an address on "n" lines, it is often found satisfactory to reset to a predetermined starting point by means of a single signal on one line. This is easy to mechanize in any serial memory. Further reset lines may select other starting points as required.

Markers.—These are outputs from the memory analogous to resets and may be used instead of or in conjunction with resets. They are again relevant only to serially addressed systems, and indicate on special output channels when particular addresses have been reached.

Miscellaneous.—At the whim of the specifying activity such signals may be generated by the memory as monitor outputs showing physical or electrical conditions within the memory, or alarm signals showing power failure, illegal input conditions, or overheating. Extra inputs may be conceived to put the memory into self-test modes, or to define various degrees of protection against accidental erasure.

Speed

Speed is expressed in terms of cycle time, which is the time taken for a read or write mode operation to be completed. Cycle times of 2 μsec are commonplace and cycle times of less than 1 μsec are available. A parallel memory with long word length naturally allows a large number of bits of data to be processed in one cycle time.

Another speed parameter which may be important is access time, which is the time taken between asking the memory to read out information, and the time the information appears on the output lines. The access time is usually about 1/4 to 1/3 of the cycle time.

Interstate Signal Characteristics

Most off-the-shelf memories are designed with standard integrated circuits at the inputs and outputs, typically DTL or TTL. These will interface directly with the user's own logic circuits, provided the noise immunity and loading rules are not violated.

As with interfacing any two digital systems, it is desirable to keep cable capacitance low in order to preserve rise-times (when high speed is required) and to minimize crosstalk and ringing.

Power

Memories work off three (3) or four (4) levels. Usually +5 V is required for the integrated circuits and about +15 V and −15 V to generate drive currents. Required regulation is about ±5%, including ripple. If you have these voltages available, it is wise to supply them to the memory. The memory will be cheaper, and will not have to contain an internal power supply that the memory manufacturer will have to buy outside anyway. If

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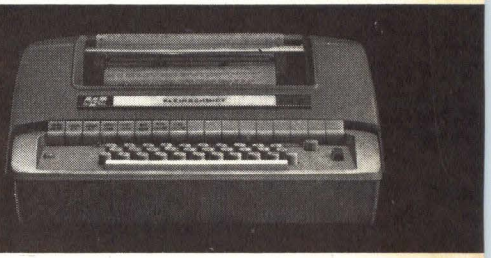

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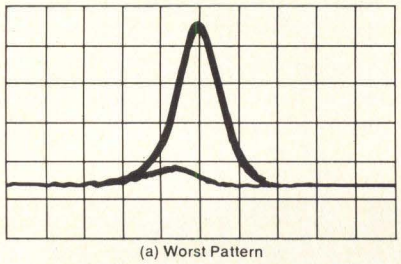
you supply the memory voltages, however, be sure to specify the maximum surge current at turn-on, and the maximum rate of change of current, which the memory may draw under operating conditions. Core memories use short duration current pulses in the order of amperes which can throw a power supply out of regulation if not sufficiently decoupled. However, the decoupling itself can cause difficulty, since very large capacitance across the power lines can trouble a power supply at turn on.

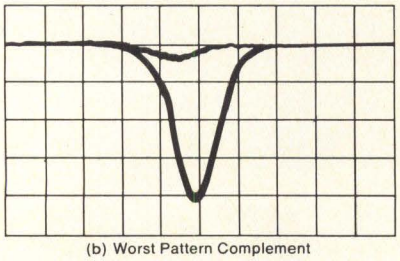
Commercial memory manufacturers usually offer a 110 V 60 Hz power supply as an option. Special power supplies can, of course, be made to allow a memory to work off any power source, ac or dc.

Power consumption is generally low, and by special design may be made extremely low. Spacecraft memories, powered by solar cells, run at fractions of a watt, while even the largest ground-based commercial memory is unlikely to take more than a few kilowatts. Consumption is generally proportional to speed and word length.

If you require any data to be retained in the memory while the power is turned off, it is essential to so specify. The core store itself is not dependent on any source of power for data retention. However, it is a somewhat difficult design problem to assure that the circuits do not spuriously access the store during turn-off and turn-on, thereby garbling some of the data. The memory manufacturer will require an assurance from you that no clock signals will be sent to the memory during power turn-off and turn-on, and you may make life easier for him by supplying him with a signal which you guarantee will be true during this period.



(a) Worst Pattern



(b) Worst Pattern Complement

Figure 2

Environmental Requirements

For use in a laboratory or an office, you should specify correct operation at 5°C to +45°C, and 0 to 95% relative humidity. This is not a difficult specification for any memory to meet.

A mobile system would require a specification on mechanical environment as well. You should investigate your own situation thoroughly before making a final specification.

RFI

If an RFI specification is required for system integration, you should specify that the unit should be immune to the applied disturbances listed below in (A), (B), and (C), and that it should not generate any disturbances in excess of those specified in (D) and (E).

A. Conducted spikes. Specify: amplitude, duration, repetition rate, and power and signal lines on which the interference is to be applied. The repetition rate should be independent of the rate of the clock or other genuine inputs. This interference is to be superimposed on the genuine inputs and monitored at the memory inputs.

B. Conducted rf. Specify amplitude, frequency limits, and points of application.

C. Radiated spikes of rf. This is best specified in terms of the test conditions, which may simply be a wire at a certain distance from the memory which is arranged to carry current spikes and oscillations of the specified characteristics.

D. Conducted output noise. Limits should be placed on high-frequency spikes and oscillations backing up on input signals and power lines, and also on similar noise being superimposed on genuine outputs on the output signal lines.

E. Radiated output noise. Core memories contain high-current loops switching at high speed. They can, therefore, radiate a substantial amount of energy. This may be minimized by good design, both electrical and mechanical, but if RFI could be a problem, specify that the memory be completely enclosed in a conducting box with RFI gasketing at all joints.

Testing

It is impossible to test a memory system under all conditions. Whatever testing you decide you can afford should be carried out under the worst conditions specified. Some severe conditions are listed below. You may not need to operate under all these conditions, but the so-called "worst pattern" check should always be performed.

For testing elaborate non-standard memories it will often be necessary to commission the development of a special purpose test set.

Any test set used should be equipped with means for automatically checking the data read from the memory, and indicating an out-of-spec condition. The test set should also have provision for monitoring input and output waveforms on an oscilloscope, and margining critical input parameters such as power supply voltages, clock widths, amplitudes, and rise times.

Worst Pattern—This is a condition where the stored 1's and 0's are distributed in such a way that all the 1's give rise to a pulse of the same polarity on the sense line. (Fig. 2a). In this case, the zeros look more like 1's than in any other case, and the sense amplifiers have their hardest task distinguishing them. Worst pattern is fairly easy to generate in the test set. The complement (Fig. 2b) must also be checked.

Bit Complement—This is a condition where worst pattern is stored in the memory and then each bit in turn is complemented, checked, and complemented again. In this case, the 1's are at their lowest condition.

Dwelling on One Word—In fast stores, there is a considerable heating effect in the cores. Have the test set continuously access one word (storing all 1's) for several seconds at its maximum operating speed. Then write all zeros and error-check.

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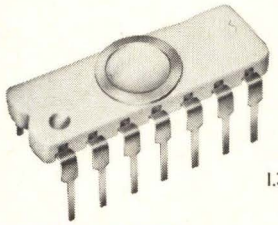

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Always ensure that your specification clearly states just what testing the vendor is required to perform. You should also state explicitly that the memory is required to perform within specification under all applicable conditions; not just under the necessarily small sample of conditions that constitutes the acceptance test.

Size and Weight

You will get a more favorable price and delivery if you specify a standard package which is usually a free-standing rack or a rack-mountable structure. If you have special requirements, a new design can be made. Size and weight considerations, if they are very stringent, as in the case of many aerospace programs, can have a considerable effect on the electrical and magnetic design. It is quite feasible to produce a memory that weighs under a pound, and occupies less than 30 cubic inches.

It is helpful if you specify that the vendor supply at an early date, an outline drawing showing mounting dimensions, overall dimensions, and pin allocation on the connectors. This drawing should then become a contractual document.

NDRO or DRO

Non-destructive readout is an expensive luxury that may not be all that it seems.

NDRO using multi-aperature cores is as vulnerable to erasure due to equipment malfunction as any other type of core store, unless the writing circuits are physically disconnected.

Although the DRO two-beat cycle explained in the section on Addressing Mode may seem an elaborate and risky way of handling data, it depends on magnetic and electronic parameters that are inherently very stable. DRO memory users very soon come to regard their memory as an NDRO blackbox.

There are applications for wired-in programs using core storage but they are generally expensive and inflexible once a design has been committed to manufacture, so it is advisable to specify a straightforward DRO store, and concentrate your attention on more critical factors.

Workmanship and Design Standards

For a commercial operation, the specification "good commercial practice" and the warranty provisions will take care of most requirements if you buy from an established manufacturer. The military requirements are more stringent, and government contractors are usually bound by the terms of their contract to impose strict standards on their vendors. It is normally required that the vendor submit workmanship standards for approval and have his facilities inspected. If a special design is required, it is always advisable to specify ground rules for worst-case design and derating of components. Approval of parts and components is often required for military products, but parts used in memories are so commonplace and so inherently reliable that an approval mill is little more than an academic exercise and should be avoided where possible. Spend the effort on detailed design review and liaison of integration of the memory into your overall system.

Military customers should specify the appropriate MIL-specs but should be prepared to allow deviations in some areas which are not applicable to core memories. For instance, magnet wire soldering and some frame interconnect techniques are not covered by existing government specifications.

Quality Control Requirements

It is desirable to let the vendor think all aspects of the specification will be monitored. The cheapest way of doing this is to let the vendor do it himself. So specify that a quality control plan is to be submitted and that facilities for your own inspectors to carry out on-site audits of the vendor's quality control system are to be provided. You will also save a lot of time and trouble by allowing the vendor, materials review authority. This can be done under sufficient control to prevent abuse of the authority.

Maintainability

A full pluggable system is obviously desirable, especially if a supply of spare circuit modules is available. The memory core stack is not normally divisible into modules, and even separating it from the drive decoding system involves breaking a large number of connections. You may have to specify this as one large replaceable unit in the interests of simplicity. Manufacturers will always be glad to sell you a stock of spare parts.

Documentation

The very minimum of documentation is a certification that the memory meets the requirements of your purchase order and installation and operating instructions—these must be specified.

Further desirable documentation is a technical description (which may come free if you request a proposal), monthly progress reports, and an operating manual. You should specify in some detail just what is to appear in these documents.

More elaborate documentation which is often required for government contracts comprises some or all of the following: Quality control procedures; Part and material specifications; Failure reports on returned material; Test data on the completed memory; Test data on components; Configuration logs; Assembly drawings; Materials review board actions and Design review minutes.

The imaginative procuring officer will doubtless think of more, but an excess of paperwork will prejudice price and delivery.

Warranty and Service

These are usually specified in the contract rather than in the procurement specification, but it is essential to ensure that prompt attention will be given to malfunctioning equipment, and that the manufacturers will accept appropriate financial responsibility.

Price and Delivery

These factors will naturally be roughly proportional to the work required to meet the specification. Therefore, be prepared to relax on aspects of the specifications during negotiations. Sales engineers will know best where the biggest savings are to be made. The most economical approach of all is to buy an existing design exactly as is.

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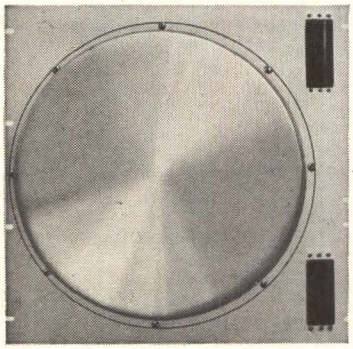

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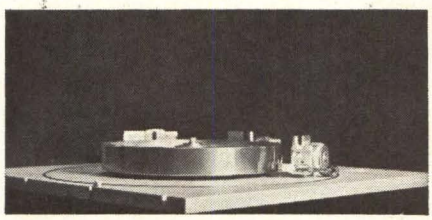

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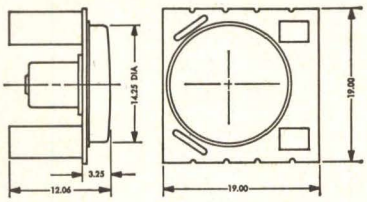

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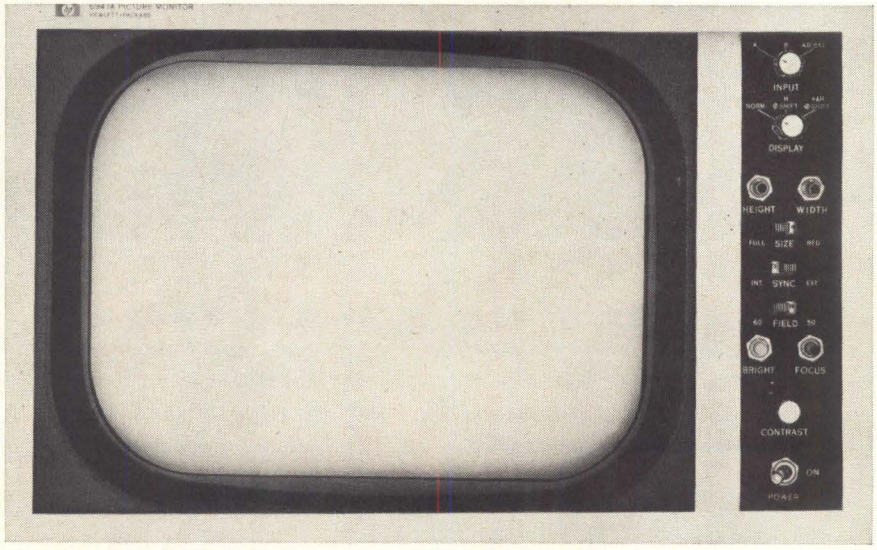

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High-resolution computer-driven graphic displays using TV rasters require performance characteristics even beyond those required for TV microscopy, satellite reproduction, and document transmissions. To satisfy these requirements, the Harrison Division of Hewlett Packard has developed a solid state, 14-inch TV monitor that features a video response extending to 18 MHz with controlled phase response.

Designated the model 6947A, the black-and-white monitor is effectively "transparent" to video signals, reproducing video faithfully without adding anything of its own. Raster linearity is less than 1.5% geometric distortion over the entire display area, and is unaffected by adjustment to the size control. Picture stability during input signal and line voltage variations is assured by the use of fully regulated power supplies (black levels are maintained within 1% during a full change in input signal level).

The 6947A has a video response that is within $\pm\frac{1}{4}$ dB up to 8 MHz Smooth roll-off to -3 dB at 18 MHz and to -20 dB at 40 MHz insures linear phase delay. This monitor displays the difficult-to-reproduce sine^2 T/2 test pulse with less than 3% overshoot.

The monitor accepts either balanced or unbalanced (75Ω) lines with loop-through facility; input impedance (unterminated) is 12Ω. Common-mode rejection for balanced lines is 46 dB up to 2 MHz, dropping at 6 dB/octave to 20 MHz. Video signals of either polarity are accepted because of the balanced input.

For maximum vertical resolution, the monitor achieves unity interlace (equal spacing between raster lines). Rock-solid interlace syncing is obtained by driving both horizontal and vertical sweep generators from a single master oscillator.The oscillator, operating at twice the line frequency, is phase-locked to regenerated incoming sync signals (either stripped from composite video or supplied separately). The output of this oscillator is divided by two to get horizontal sync pulses.

Vertical timing pulses are derived by using the incoming vertical sync pulse as a gate to select a pulse from the master oscillator. The vertical sweep generator thus is locked solidly to the horizontal.

Lock-in range of the sync circuits is so broad that, without any circuit switching, the circuits can lock onto the 50 Hz, 625-line European Sync standards as readily as they do to the 60 Hz, 525-line American Standards (a front panel switch adjusts the raster aspect ratio to accommodate either snyc standard).

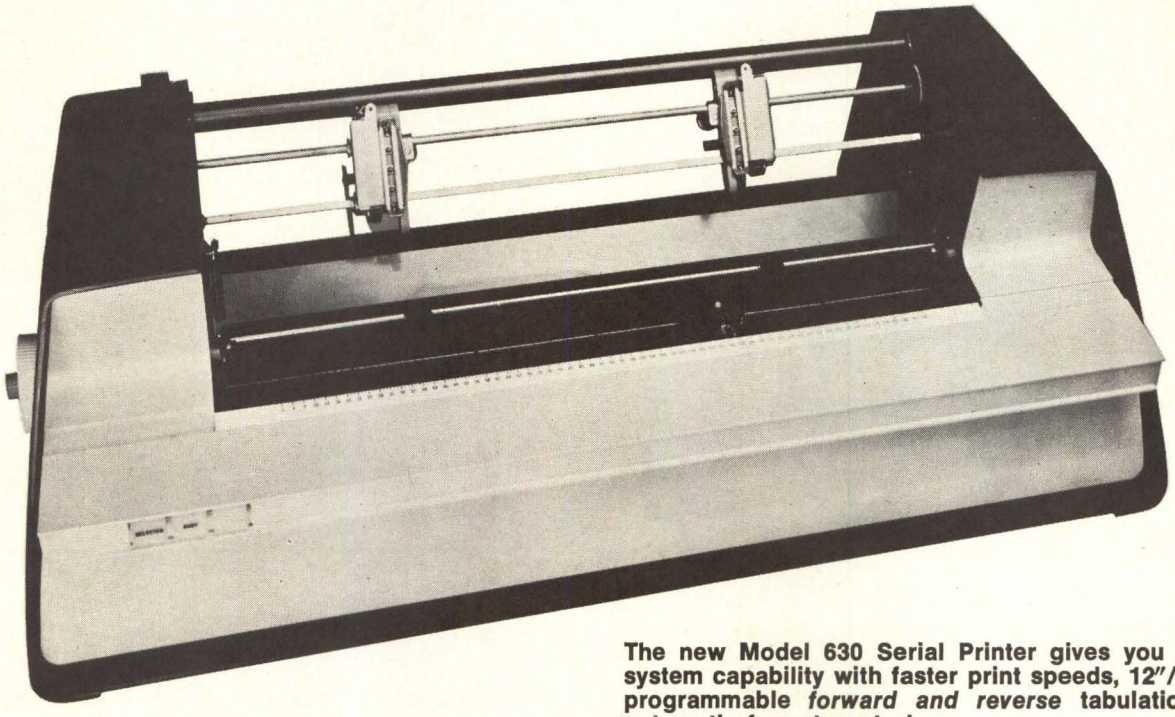
Feedback techniques are used to insure raster linearity. The vertical sweep generator uses a Miller run-down circuit. A current-sensing resistor, in series with the vertical deflection coil, provides a feedback voltage for linearizing the vertical drive amplifier.

A sensing coil is wound with the horizontal deflection coil. Voltage variations induced in the sensing coil by non-linear sweep currents are used as an error signal to correct the horizontal driver output. A small, parabolic waveform is added with the error voltage to compensate for the curvature of the picture tube's faceplate. These feedback techniques maintain raster linearity at such a high level that no manual linearity controls are needed in this monitor.

The Model 6947A costs $1050.

For additional information circle No. 199 on inquiry card.

New printer lets you cut data system design time



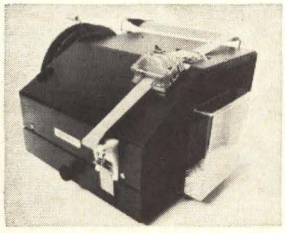
The new Model 630 Serial Printer gives you greater system capability with faster print speeds, 12"/second programmable *forward and reverse* tabulation, and automatic format control.

Now you can get a head start on building a data system for tomorrow's market. That's the idea behind Litton Automated Business Systems' new data system components for original equipment makers — and users who want to put together a system based on their particular needs.

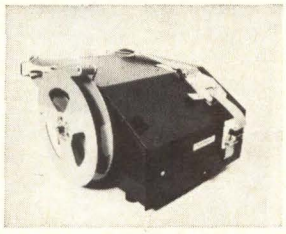
The Model 630 is a completely new and different serial impact printer. It features a moving printwheel that allows faster, more efficient operation. Electronically controlled stepping motors cut down on moving parts — providing high reliability, low maintenance and longer life. Positive detent assures smudge-free printing. The Model 630 can be ordered with tractor feed or split platen. A companion keyboard is also available.

OEM products include reliable 50 cps. paper tape punches and readers in a variety of configurations. Series 500 Tape Punches and Readers give you such advanced design features as small, efficient electromagnets in combination with over-center springs for smooth, trouble-free punching over a long life — reluctance type pick up — bi-directional reader — semi-automatic tape feed.

Companion keyboard



Tape Punch



Tape Reader

Litton Automated Business Systems
OEM Products Division
600 Washington Avenue
Carlstadt, N.J. 07072

Please send me complete information on your new data system components.

Name _____ Title _____

Company _____

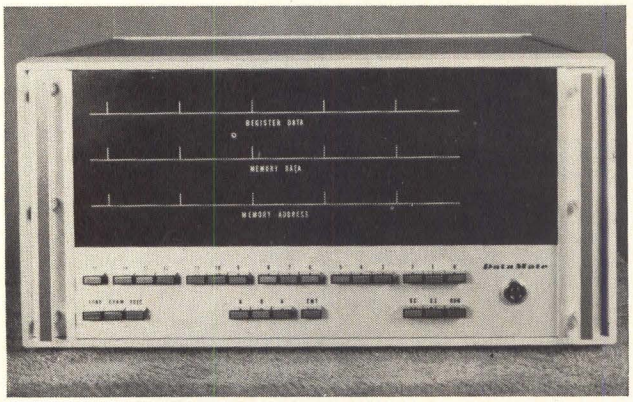
Street _____

City _____ State _____ Zip _____

AUTOMATED BUSINESS SYSTEMS
DIVISION OF LITTON INDUSTRIES

CIRCLE NO. 28 ON INQUIRY CARD

NEW PRODUCTS



DIGITAL COMPUTER

A two's complement, 16 bit arithmetic fully parallel processor, the DataMate 16 has a 4096 word, 1 μs memory modularly expandable to 32,724 words. Built in features include hardware multiply and divide; 8 I/O channels with priority interrupts; hardware index register and power failure protection. A flexible I/O bus accommodates up to 64 peripheral devices. A plug in card is used to interface the processor with the peripherals.

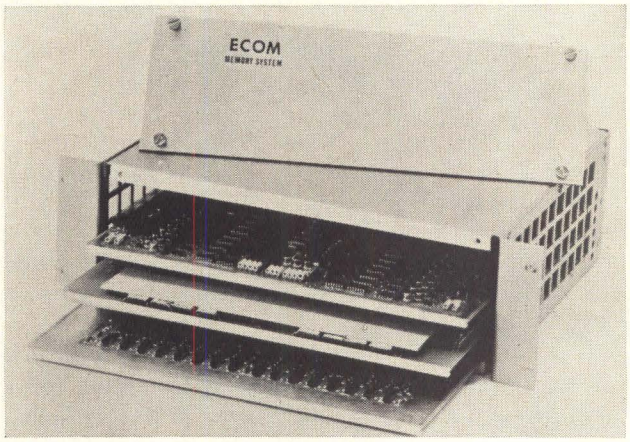
The computer has byte, words, and double word processing capability with multi-level indirect addressing. A throughput rate of 1 million 16 bit words per second makes the computer particularly applicable to systems dedicated to data acquisition, data manipulation, data logging, data analysis and process or instrument control. DataMate Computer Systems, Big Spring, Texas.

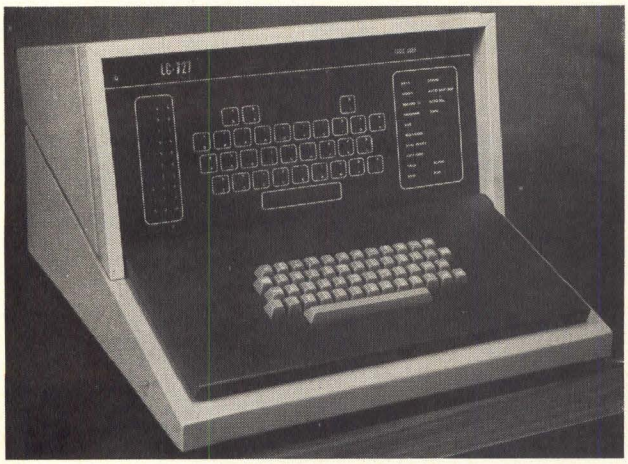
Circle No. 202 on Inquiry Card.

CORE MEMORY SYSTEM

ECOM is available in capacities from 1024 x 8 up to 4096 x 16, with a full cycle speed of 2.50 μs and an access time of .75 μs. The entire ECOM system is contained on three 12″ x 15″ circuit boards. Core arrays and diode switches that make up the magnetics assembly are mounted on one pc board. The timing, decoding, driving and digit circuitry are divided between the remaining two boards. Other features include servo controls on critical voltages; built-in expansion capabilities with party-line to increase the number of words and their length; up to 16 bits in word length. Interface circuits are compatible with all popular logic forms, DTL, T^2L, RTL and discrete circuits. Standard Memories, Inc., Sherman Oaks, Calif.

Circle No. 201 on Inquiry Card.



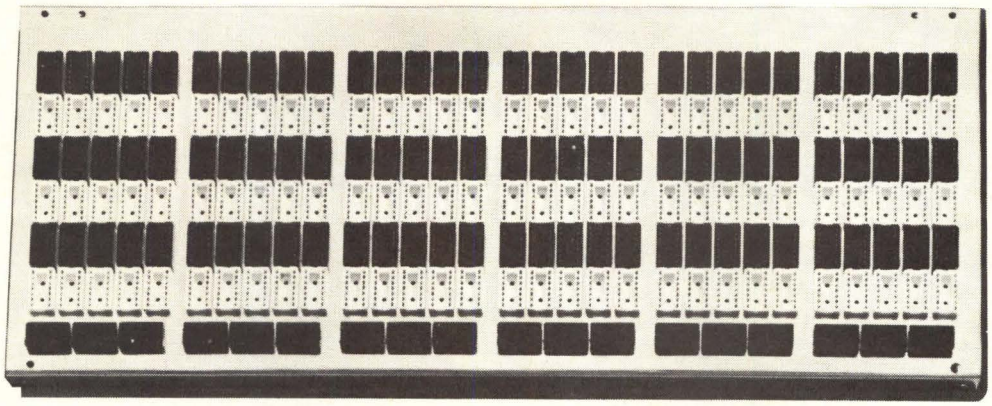


DATA ENTRY SYSTEM

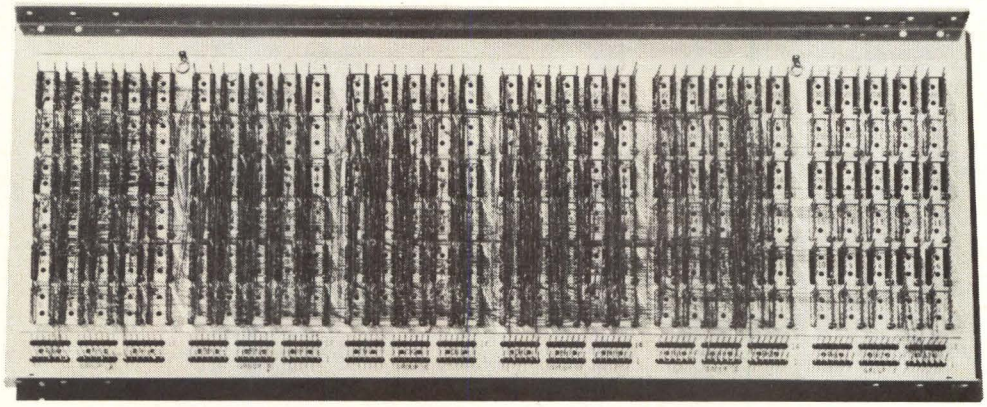
The LC-720 data entry system is capable of accepting simultaneously the data output of up to 120 keyboard operators into its central processor, which employs a small digital computer. The output of the central processor is then recorded on either two IBM/360-compatible magnetic tape recorders or an IBM magnetic disc pack recorder.

Keyboard is a standard 64-character keypunch layout combined with an alpha-numeric display panel that shows the operator in English the program number, the last character entered and column number, and the terminal operating mode. An operating mode provides for simultaneous entry and verification of data by two different operators. In this mode, the data entered by one operator is stored in core memory until it has been verified by a second operator; then it is entered on the tape or disc. Logic Corp., Haddonfield, N.J.

Circle No. 244 on Inquiry Card.



Buy one



We'll wrap it free

Here's our special offer: if you buy our new Modu-Wrap DIP packaging chassis for your next prototype system, we'll do the wire-wrapping free, no matter how many wires are involved. All you need to do is to tell us what your hardware requirements are and pay a small charge for programming our automatic wire-wrapping machines. This offer expires January 31, 1969. And, sorry only one system to a customer.

The reason we're making this unusual offer, is to introduce you to our new Modu-Wrap series 2900/5800 DIP chassis assemblies. They come in two standard widths (2.9" and 5.8") and they're available in any length you want. Furthermore, you can get any combination of 14, 16, or 24 pin sockets; component posts, transistor holders, connectors (.100" cc) or even just the blank panel. In other words, our approach is completely modular and you get packaging that fits your needs exactly. No waste space, no empty sockets.

Because of the modular building block structure of our packaging system, you get what you want without paying extra for set-up, tooling, engineering, and costly hand-writing. Best of all, you don't have to wait 10 weeks to get it. We deliver in three weeks.

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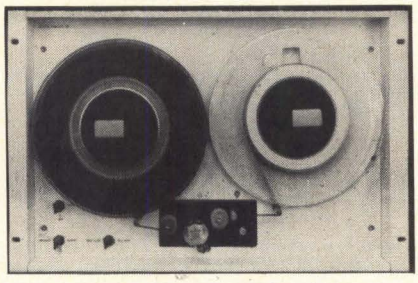
CIRCLE NO. 29 ON INQUIRY CARD

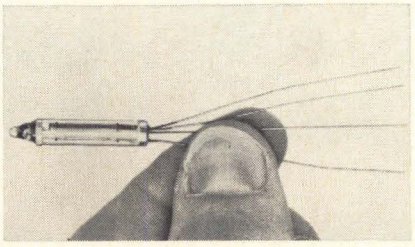
NEW PRODUCTS



INCREMENTAL RECORDER

Model III digital incremental recorder records data in IBM compatible format on 8½" reels containing 1,200 ft. of recording tape. The 19" rack mounted unit features depressed mounting of the drive and reel mechanisms and a straight-line tape path design which provides for untouched tape oxide prior to recording head contact. Other standard features: recording at 200 bpi; 110 steps per second; 7-track format with 9-track option; LCC and IRG gap times automatic at 350 ms maximum. Delta-Corders, Inc., Phoenix, Ariz.

Circle No. 215 on Inquiry Card.



SUBMINIATURE INDICATOR TUBE

Subminiature logic indicator triode Type 6977 operates with either NPN (positive) or PNP (negative) logic circuits and permits grid potentials as high as 12 V when proper biasing is used. When the 6977 is 'ON', it produces a brilliant blue-green bar of light that is visible under high ambient light conditions.

Arrays of 6977 tubes mounted on printed circuit boards are used to monitor flip-flop status in computer registers, in input/output devices and in other logic circuits. The tubes are 0.217" in diameter and may be mounted in direct contact with one another. Amperex Electronic Corp., Semiconductor and Microcircuits Div., Slatersville, R.I.

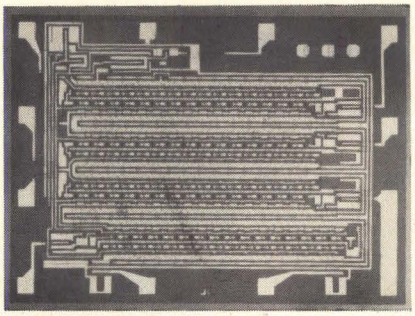
Circle No. 216 on Inquiry Card.

DATA SETS

Two data sets, designated Modem 4400/20H and Modem 4400/20L, transmit two separate high-speed 2000 bit-per second messages at the same time over a single telephone line. Each message stream is transmitted independently, as if two individual phone lines were being used.

EDP users with multi-station communication networks can realize cost savings of up to 50 percent on leased transmission lines by using the dual transmission capability of the data sets. At current line leasing rates, a data processing center in New York with remote terminals in Kansas City and Omaha would save $935.00 per month on line costs. International Communications Corp., Sub. of Milgo Electronic Corp., Miami, Fla.

Circle No. 203 on Inquiry Card.



STATIC SHIFT REGISTERS

Two 64-bit MOS shift registers, each with a single phase clock, provide operation from dc to 1 MHz and consume less than 3 mV of power per bit.

The 3305 quad 16-bit static shift register, which is available in a Dual In-Line package, and the 3306 dual 16-bit/single 32-bit static shift register, which is packaged in a TO-100 container are identical except for their packages and their input-output connections (four for the 3305 and three for the 3306). A minimum noise immunity of 1 volt is guaranteed. All inputs are protected; all outputs are buffered.

If the quad system is organized around BCD, each 16-bit register can store four 4-bit words with no bits unused.

Chief applications for the circuits are as storage registers, delay lines and data buffers used in radar and telemetry systems, computer and memory systems, control systems, calculators, data terminals, and data acquisition systems. Fairchild Semiconductor, Mountain View, Calif.

Circle No. 230 on Inquiry Card.

Good things to remember!

AMC's new M-200 was specifically designed for the new generation of low-cost computers. Compact in size, it is a fast access memory that is also surprisingly low in cost. The M-200 is a head-per-track system featuring a single 12-inch disc that accommodates from 16 to 128 data tracks with storage capacity from 426,000 to 3,400,000 bits. IC logic, disc and belt drive fit into a compact 20x19x7 inches. If you are seeking speed, capacity *and* economy — the M-200 is something to remember!

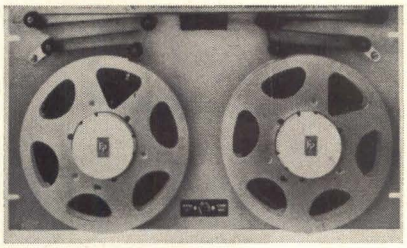
APPLIED MAGNETICS CORPORATION

Amc

75 ROBIN HILL ROAD / GOLETA, CALIFORNIA 93017 / TELEPHONE 805-964-4881

CIRCLE NO. 32 ON INQUIRY CARD

NEW PRODUCTS

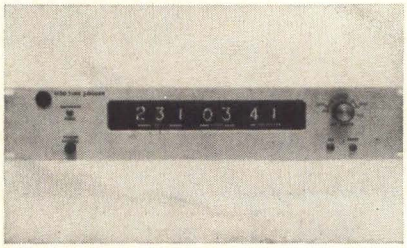


HIGH SPEED TAPE SPOOLER

Type 4030 tape spooler is capable of speeds up to 60 inches per second (reading speed). The unit contains a servo mechanized tape tension system that ensures trouble-free handling of tape at high speeds. A high speed rewind facility permits tape to be rewound at speeds of up to 180 inches per second in either direction.

The 4030 is equipped with 8″ NAB reels, which store up to 800 feet of 0.0045″ paper tape. To facilitate tape loading, each servo arm can be latched at its outer extremity. Ferranti-Packard Electric, Ltd., Electronics Div., Toronto, Ontario, Canada.

Circle No. 222 on Inquiry Card.



TIME LOGGER

A time code generator/reader, Model 1130, supplies a time code to up to 50 continuously operating communication recorders, and searches for desired information in either direction at rewind speeds to 1000 ips.

A 3600-foot tape (sufficient for 24 hours at ½ ips) can be rewound at maximum speed from end to start in less than 2½ minutes at 300 ips.

Time resetting is accomplished by convenient front panel controls. Silicon integrated circuits and transistors are used throughout.

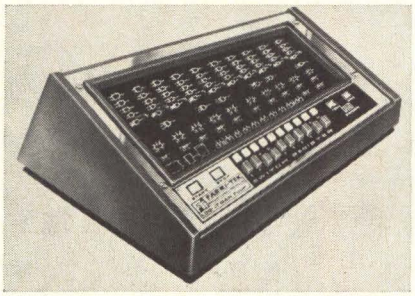
The 1130 operates on 100-130 volts, 60 Hz, and measures 3½″h x 19″w x 6″d. Weight, 20 lbs. Electronic Engineering Company of California, Instruments Div., Santa Ana, Calif.

Circle No. 232 on Inquiry Card.

AC DIGITAL PANEL METER

The DT-342 is available in three ranges: 0 to 750 V rms; 200 V rms; and 20 V rms. Accuracy is 0.2% ± 2 digits on the 0 to 750 V and 2 to 200 V scales, and 0.5% ± 2 digits on the 2 to 20 V scale. The frequency response of the instrument is 45 Hz to 10 kHz, with an input impedance of 1 Megohm. In mechanical dimensions and weight it is directly equivalent to the DT-340 (2.4″ high x 5.2″ wide x 7.5″ deep, weight less than 20 ozs.) The case is constructed from high-impact, aborbent cycolac plastic; the unit is self-insulating and hermetically sealed. Data Technology Corp., Palo Alto, Calif.

Circle No. 241 on Inquiry Card.



DIGITAL LOGIC TRAINER

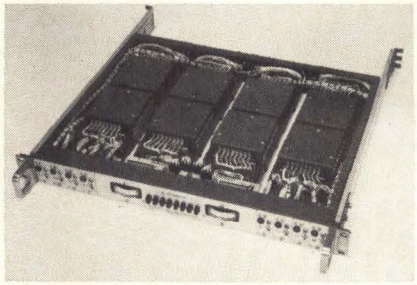
A digital logic trainer, the Logi-Tran Four, gives students reinforced understanding of digital logic classroom theory by enabling them to explore all digital logic functions by a hands-on interconnection of logic elements.

The Logi-Tran Four has a unique interface capability for use with Fabri-Tek's Bi-Tran Six digital computer trainer. Logic functions are clearly marked on an extremely heavy-duty printed circuit card. Socket mounted integrated circuits facilitate service/maintenance training. A coordinate numbering system aids element identification.

The Logi-Tran Four measures 7″ high, 19″ wide and 15″ deep. Educational Products Div., Fabri-Tek Inc., Edina, Minn.

Circle No. 231 on Inquiry Card.

NEW PRODUCTS



IC POWER SYSTEM

The systems consists of a thin-line rack adapter which can accommodate up to 8 miniaturized power modules, 8 overvoltage protectors, 8 individual power control panels, a metering panel with two meters, fuses and selector switch, 4 connecting cables (no soldering) and 2 chassis slides.

The power supplies, a series of power modules trade named COM-PAK MARK II™, as well as all system accessories are standard, off-the-shelf models which can be supplied fully wired and assembled ready to plug into a customer's system, or may be ordered unassembled with individual components and accessories specified and assembled by the customer.

COM-PAK MARK II power supplies can be mounted on any of five mounting surfaces.

Dual output system power supplies are provided with these features: independent operation, remote sensing, remote programming and series/parallel (master/slave) operation. Lambda Electronics Corp., Melville, N.Y.

Circle No. 228 on Inquiry Card.

TAPE DRIVES

Three 60KHz magnetic tape drives, the 7-channel TU79 and TU30 units and the 9-channel TU30A, all IBM compatible, are controlled by the TM10 control which can handle up to eight drives in any combination. The new tape units operate at 75 ips and feature a recording density of 800 bpi for the TU30A and 200, 556 or 800 bpi for the TU30 and TU79.

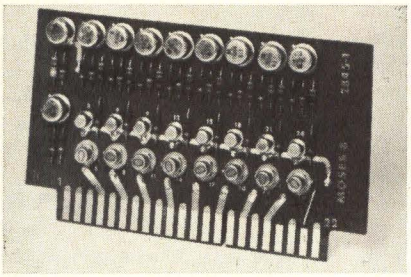
The tape drives bring to five the number of such units available with the PDP-10. The others are 7- and 9-channel 36KHz drives, Type TU20 and TU20A. Digital Equipment Corp., Maynard, Mass.

Circle No. 208 on Inquiry Card.

PRECISION WW POT

A 7/8" diameter, 10-turn precision wirewound potentiometer, the LD09, is designed to meet requirements of MIL-R-12934. Available in resistance values from 100 ohms to 200 K, the LD09 provides independent linearity of ±0.2%. The unit is 1½" long and is available in either servo or bushing mounting with single or dual sections. When required, 10-inch-per-pound stop torque can be achieved. Litton Industries, Potentiometer Div., Mt. Vernon, N.Y.

Circle No. 207 on Inquiry Card.



ELECTRONIC SWITCH

Model MOSES-8, an 8-channel switch, has an input analog voltage range of ±10V (with +15V and −28V supplies) and ±5V (with ±15V supplies). Other features include switching time, 0.1 μs; switch impedance 100 MΩ open, 300Ω closed; and capacitive coupling, 2.5 pF max. Operating temperature range is 0° C to +70° C. Power requirements are +15V at 25 mA and −15V at 50 mA or −28V at 100 mA. Pastoriza Electronics, Inc., Newton Upper Falls, Mass.

Circle No. 234 on Inquiry Card.

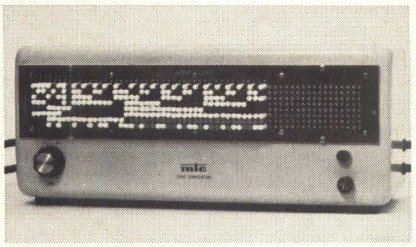
CAPTION MODULES

Caption modules can be used independently as message modules or in conjunction with manufacturer's numeric readout modules.

Anything that may be put on film can be shown, including numbers, letters, words, symbols and special characters. Up to 6 messages per module may be displayed, in any combination, individually, or simultaneously by lighting the corresponding lamp or lamps. When not illuminated, the captions can be either hidden or visible, depending on the use of non-glare or polished viewing screens. Dialight Corp., Brooklyn, N.Y.

Circle No. 214 on Inquiry Card.

NEW PRODUCTS



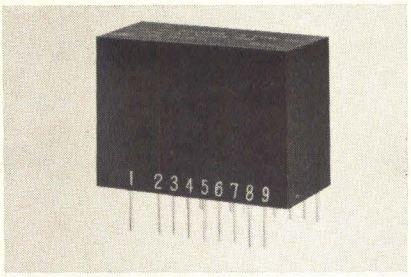
CODE CONVERTERS

Converters allow translation of any 5, 6, 7 or 8 level input code to any desired output code. Versions can be provided with hard-wired input and output code formats for specific applications, or for maximum versatility, with uncommitted diode-pin plugboard input and/or output circuits.

The units will I/O interface between paper tape or card readers, punches. typewriters, magnetic tape decks, optical readers, computers, etc., in any combination, for one-way or two-way code conversion.

Conversion speed is greater than 10,000 codes/sec and essentially depends on the speed of I/O devices and voltage levels. A built-in power supply for 115 Vac operation is standard. Measurement Technology Corp., Canoga Park, Calif.

Circle No. 226 on Inquiry Card.



DECODER/DRIVER

Series D 4-line to 7-line decoder-driver module has signal inputs in the 1, 2, 4, 8 BCD format at logic levels compatible with DTL and TTL systems. Five volts d.c. is required for operation while isolated lamp inputs permit use of lamp voltages up to 20V in the incandescent version and 80 V in the neon version. The device measures 1.3 x .6 x .8" with pins on .1" centers. Operating temperature range is 0° to 70°C. The Mesa Co., Inc., Bristol, Pa.

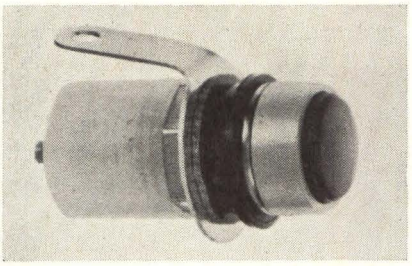
Circle No. 225 on Inquiry Card.

COMPUTER TERMINAL

The portable Model 1021 conversational terminal is compatible with any computer using extended BCD interchange code, and with the IBM 2740 series terminals. No change in software is required.

The Model 1021 has the following capabilities: reverse index which permits reverse document travel toward top margin; interrupt key which signals the CPU to momentarily stop the feedback and take new instructions; and vertical parity check which checks if the transmitting or receiving code is in error. In addition, a non-print non-escape feature ensures against piracy of user's name, job code, or account number by non-printing while transmitting the data, and the interchangeable typing spheres permits print-out in various typefonts appropriate to the specific application. DURA, Div. Intercontinental Systems, Inc., Palo Alto, Calif.

Circle No. 237 on Inquiry Card.



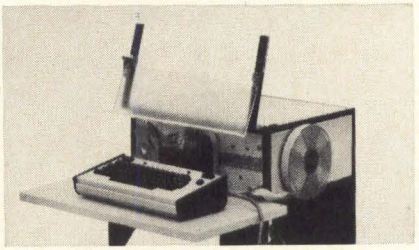
INDICATOR LIGHT

Designed for rear relamping, Model 107 series ultra-miniature indicator light mounts in a 7/32" diameter hole for the standard models or in a 7/64" diameter hole for the insulated model SI. Available with a single terminal, or with two terminals by using insulating hardware, the Model 107 series uses the T-1 midget flange based lamp.

The light is available in six lens styles and in five lens colors—both translucent and transparent. The Sloan Co., Sun Valley, Calif.

Circle No. 240 on Inquiry Card.

NEW PRODUCTS

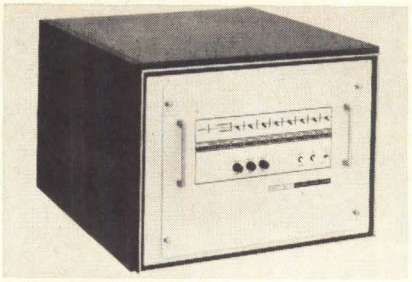


PAPER TAPE KEYPUNCH

CPP 600 machines can be supplied with any required keyboard layout and paper tape coding, including BCD, ASCII, and six-channel teletypsetting codes.

Keyboard is entirely electronic. A pulse key switch allows a second key to be depressed and cause punching before the first key has been released, yet electronic lock-out prevents double punching or garbled punching on simultaneous depression of two keys. A keyboard display continuously shows the last previous code punched and a large clear plastic, hinged media holder is provided for source documents. Logic is entirely integrated circuits mounted on removable printed circuit cards. Computer Products, Inc., Seattle, Wash.

Circle No. 219 on Inquiry Card.



SMALL MASS STORE

The Small Mass Store (SMS) is available for DDP-516 computers in four capacities ranging from 24,576 to 196,608 words. The SMS offers an average access time of 8.7 ms and a data transfer rate of 30,000 16 bit words per second.

The option consists of the device and a controller. The device may be housed in its own table-top cabinet or can be rack-mounted in a 72-inch cabinet with the DDP-516. The controller is installed in the computer's option drawer.

The fixed-head SMS records data on a word (16-bit) basis with each word containing a parity bit. The SMS can be connected to the computer through the I/O bus, direct multiplex control unit or direct memory access unit. Data transfers are word buffered. Honeywell, Inc., Computer Control Div., Framingham, Mass.

Circle No. 218 on Inquiry Card.

DISC MEMORY SYSTEM

Series 8000 disc memory system has an average access time of 8 milliseconds and a maximum track capacity of 6250 bits.

Each memory system includes head address, decode and selection systems, bit and sector clocking, and complete "functionally packaged" integrated circuit boards; one for the entire read function, another for the write.

The system is capable of operation in either a vertical or a horizontal position. When mounted in a horizontal plane the disc assembly requires 10½" of panel space.

Compatible with most integrated circuits, all logic interfacing is accomplished at positive levels through a single connector. Weight of the system is 10 lbs. Information Storage, Inc., Detroit, Mich.

Circle No. 213 on Inquiry Card.

COMPUTER WIRE

A line of computer wire with an extremely high insulation cut-through resistance is specifically designed for automatic wire wrap applications. The Vylar™ wire is available in AWG sizes ranging from 20 to 32 and has a continuous operating temperature rating to 105°C. It is available as single conductor, twisted pairs or twisted shielded pairs.

The wire is normally constructed with a silver plated, oxygen free, high conductivity #30 solid copper conductor, with a helically wrapped film of biaxially oriented Mylar polyester laminate with a flame retardant additive. The stripping forces vary with size, ranging from ½ lb. for AWG 32 wire to 1 lb. for AWG 20 wire. Insulation thicknesses available range from .00325 to .00650", ±.0005". Berkshire Technical Products, Inc., Reading, Pa.

Circle No. 209 on Inquiry Card.

PLASTIC TRANSISTORS

Differential amplifiers with PNP polarity, the TD-400 family, feature a typical base-to-emitter voltage match within 2.5 mV and will track within 6 μV/°C. Minimum β is 120 at 100μa.

Complementary dual transistors, the TD-600 series, are specified for low-level applications such as single-pole double-throw switching. These units feature low noise (2 dB maximum) and high gain. In addition, the Type TD-602 features a minimum gain-bandwidth product of 200 MHz. Sprague Electric Co., North Adams, Mass.

Circle No. 204 on Inquiry Card.

DATA ACQUISITION INSTRUMENT

The Multiverter(R) Mark III includes a 15 bit analog-to-digital converter and provides continuous throughput at rates exceeding 100 kHz. Up to 128 input channels can be accommodated by a single unit

Multiverter instruments are a family of devices combining a multiple channel multiplexer, a sample-and-hold amplifier of high accuracy, and a high resolution analog-to-digital converter in a single drawer. Raytheon Co., Computer Operation, Santa Ana, Calif.

Circle No. 211 on Inquiry Card.

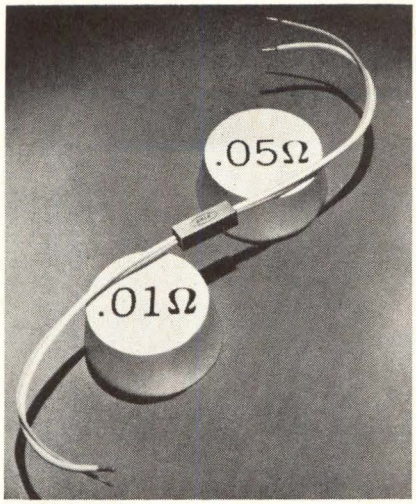
CONVERTER MODULE

A 10 bit digital-to-analog converter module, Model DT24, has 0.1% accuracy and high drive capability for driving remote loads through cable.

Output range of the DT24 is −10 V to +10 V full scale, with current of ±20 mA. For a change in output from minus to plus full scale, settling time to within 10 mV of full scale is 60 μs. Either two's complement or one's complement digital input is accepted. The module includes a conversion ladder and operational amplifier.

The DT24 is mounted on one standard SDS circuit card and fits into the same mounting cases as the T Series digital logic modules. Scientific Data Systems, El Segundo, Calif.

Circle No. 212 on Inquiry Card.

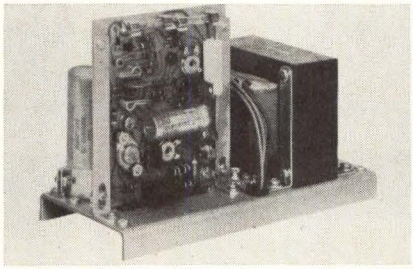


PRECISION WW RESISTORS

Rated at 5 W (continuous), the SPR type resistors have a resistance range of .01 to .05 ohm; tolerances from .1% to 5%, depending on resistance range; temperature coefficients of ±20 ppm (from +25°C to +250°C) and ±40 ppm (from +25°C to −55°C). Load life stability is rated at ±0.1% max. ΔR per 1,000 hours at 5 W continuous power. Typical ΔR is ±.05%. Inductance is 15 nh max. from .5 to 500 kHz.

The SPR-367 is housed in a rectangular ceramic case 7/8" l x 21/64" w x 5/16" h; the SPR-383 is housed in a rectangular gold anodized aluminum case 1" l x 5/16" w x 5/16" h. Dale Electronics, Inc., Columbus, Neb.

Circle No. 220 on Inquiry Card.

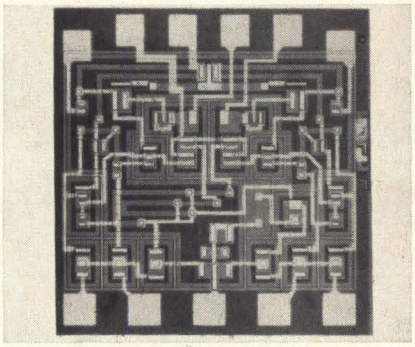


POWER SUPPLY

A dual output power supply, Model No. D-OEM-1, provides 24 volts at 2 A for relays and other dc loads and 5 volts at 1 A for integrated circuit loads. Overvoltage protection is provided. Dimensions are 8.3"L x 5.7"H x 4.0"W and it weighs 9 lbs. Wanlass Electric Co., Santa Ana, Calif.

Circle No. 224 on Inquiry Card.

NEW PRODUCTS

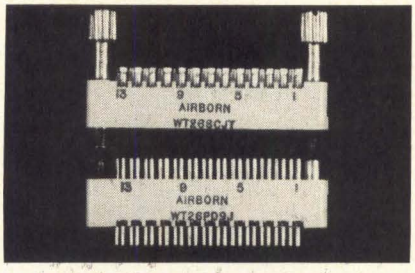


DIFFERENTIAL COMPARATORS

Series TDC 4711 and 5711 monolithic dual differential comparators guarantee a minimum sink current of 5.0 mA, permitting the circuit designer to directly drive up to four TTL input loads. Pin configuration is the same as the standard TDC 1711. Types TDC 6711 and 7711 offer two individually controlled and independent differential comparator circuits, each with its own strobe and output. The two circuits can be used separately, or the two outputs can be OR'ed. TDC 8711 and 9711 combine the features of high sink current and independent outputs.

The comparators, standard or high sink current, are supplied in ceramic dual-in-line or flat packages. Single output comparators come in 10 lead TO-5, dual-in-line or flat package. Transitron Electronic Corp., Wakefield, Mass.

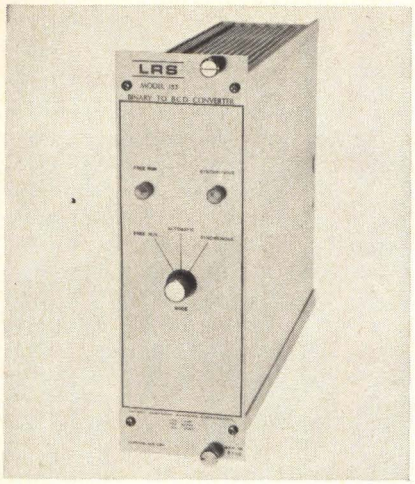
Circle No. 233 on Inquiry Card.



SUBMINIATURE CONNECTORS

WTA Series of subminiature rectangular connectors feature dual contact rows, offset .050", jackscrew set, .030" diameter pins, cross-slotted sockets, and dip solder or solder cup terminals. Moldings are class-filled diallyl phthalate. Sizes range from 10 to 70 contacts with .100" centers. Airborn, Inc., Dallas, Texas.

Circle No. 223 on Inquiry Card.

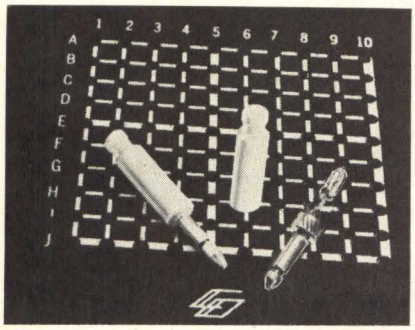


BINARY TO BCD CONVERTER

Model 153 Binary-to-BCD Converter accepts up to 24 bits of binary data from a parallel line input and decodes it into up to 8 decades of binary coded decimal.

Compact integrated circuit design provides exceptional reliability and accuracy at a speed fast enough to lead virtually any data recorder. The unit's 100 μs full scale conversion time allows efficient decoding of a large number of binary channels for decimal readout on a parallel printer, punch paper tape recorder, or typewriter. LeCroy Research Systems Corp., West Nyack, N.Y.

Circle No. 242 on Inquiry Card.



LITED PINS

A Co-Ax Lited Pin permits insertion of bulbs into 2 thru 6 level matrix programming boards. A rugged .106" diameter teflon insulated pin provides high bending resistance. Bulbs up to sizes T1¼", incandescent or neon, can be used according to customer specifications. Handles of these new lited pins are available in several colors to facilitate their use in various programs. Co-ord Switch LUC Industries, Inc.

Circle No. 217 on Inquiry Card.

MAG TAPE ENCODERS

Series 1000 Encoder is offered in both 7-track and 9-track encoding models. The Series 1070 encodes 7-track magnetic tape at 556 bpi with a ¾" record gap; Series 1090 encodes 9-track tape at 800 bpi with a 0.6" record gap.

Both 7- and 9-track models are offered in three keyboard configurations. The full configuration consists of a basic keyboard (which generates 102 codes), a function control panel (60 codes) and an auxiliary keyboard (94 codes). These, in combination on Models 1073 and 1093, provide the full 256-character encoding capability. Keymatic Data Systems Corp., Bay Shore, N.Y.

Circle No. 236 on Inquiry Card.

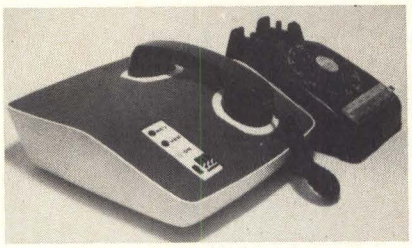
DUAL-IN-LINE SOCKETS

The 039 Series of dual-in-line sockets for MSI and LSI packages feature entrances designed to protect and hold the taper of the D.I.P. leads by not interfering with their outward spread—socket contacts wipe against the side of the lead. The 039 Series polysulfone sockets have one-piece contact/terminals stamped from full spring temper beryllium copper alloy, hard gold over nickel plating, with tab type terminals for wave or hand soldering, and are available in two models—one with flanges for chassis mounting, one without; for use on p.c. boards. The sockets accept all MSI and LSI devices with 0.600" spacing between rows, 0.100" spacing between leads, and lead lengths of at least 0.115".

Typical contact resistance is 0.010 ohms; insulation resistance is 10^{16} ohms; and interlead capacitance is 4 pF at 1 MHz. Max. current is 1.0 A and voltage breakdown is at 2200 V. Typical operating life is from 20,000 to 50,000 insertions. Barnes Corp., Lansdowne, Pa.

Circle No. 205 on Inquiry Card

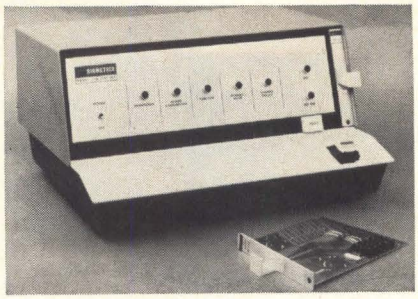
NEW PRODUCTS



ACOUSTIC COUPLER

Model 103AC is designed to provide data communications over the dial network using a standard voice handset. Logic level inputs are converted to bit serial tones for transmission. The phone line transmission is compatible with the Western Electric 103A. Unit is available with transmit or receive options for asynchronous data up to 300 bits/sec. The unit measures 10½" x 11½" x 3¾" and weighs approximately 5 lbs. Digi-Data Corp., Bladensburg, Md.

Circle No. 239 on Inquiry Card.



DIGITAL IC TESTERS

The Model 1110 features a programmable program card technique which allows forcing function and limit detection levels to be adjusted simply to less than 1% accuracy. An internal voltage reference source and rear panel test points can be used to establish better than 0.25% accuracy for all programmable test conditions. A single plug-in quick calibration card can also be used for on line go-no-go tester calibration assurance.

The 1110 tests virtually all digital IC's including complex function types in any package configuration up to 16 leads, at rates up to 10,000 per day Signetics Corp., Sunnyvale, Calif.

Circle No. 235 on Inquiry Card.

SILICON POWER TRANSISTORS

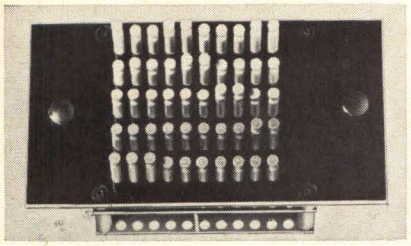
A family of single-diffused, intermediate frequency NPN silicon power transistors with current ranges from 3.0 A to 30 A feature capability to resist second breakdown, moderate frequency (not susceptible to spurious oscillations) and power cut-off frequency beyond audio range. Vce_o (sus) ranges from 40-140 V. The family is packaged in either the TO-66 or the TO-3 configuration. Solitron Devices, Inc., Riviera Beach, Fla.

Circle No. 206 on Inquiry Card.

SWITCHING-TRANSISTORS

A line of switching transistors feature minimum current gains of 40-100 (at 1 A). Minimum $BVce_o$ (sus) ranges from 80-100 V and $BVce_r$ (sus) from 120-150 V. Collector saturation voltage at 1 A is 0.25 V max; at 5 A, it is 1 V max. Maximum turn-off time ranges from 450-550 ns. Transistors are available in both pancake and stud-adapter TO-5 packages. Solid States Products, Salem, Mass.

Circle No. 210 on Inquiry Card.



PROGRAM BOARD

A captive-pin matrix programmer featuring 10 x 5 modular design and snap-in mounting can be used for rapid reset programming applications, and is constructed to mount in a standard 19″ relay rack.

The program board features vertically-bussed upper deck and individual lower deck contacts—a design suitable for providing diode isolation. Contacts are all silver plated for low contact resistance over thousands of insertions. Six similar modules can be stacked horizontally to provide a 10 x 30 program. Sealectro Corp., Programming Devices Div., Mamaroneck, N.Y.

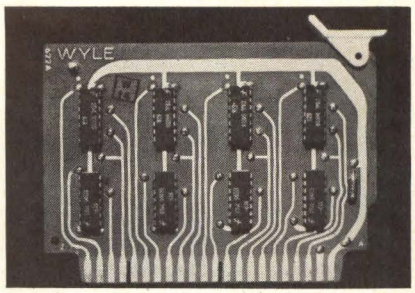
Circle No. 238 on Inquiry Card.

CONTINUOUS TAPE RECORDER

An IBM-compatible tape deck, Model 70C, is designed for a maximum speed of 25 ips continuous operation, and is available at speeds of 5, 12½, and 18¾ ips. The recorder will accept up to 20 commands per second and has the optional capability of search forward/reverse at 75 ips.

The Model 70C is available in either a 7- or 9-track configuration. All the controls and write electronics are standard features. LRCC and CRCC generation, read electronics, and gap insertion are optionally available. Cipher Data Products, Inc., San Diego, Calif.

Circle No. 243 on Inquiry Card.



FLIP-FLOP CARDS

The MGF-8 flip-flop card provides eight independent gated RS flip-flops, with each flip-flop having a single set and single reset input, gated with a transfer input. The card has all inputs and outputs brought out to the connector.

Designed for general-purpose and parallel load storage element applications the MGF-8 provides: frequency, dc to 5 MHz; input loading, DC1 and DC0, 1 unit load, transfer, 2 unit loads; and noise rejection, 750 mV typical at logic 0, 1 V typical at logic 1. Wyle Laboratories, Systems Division, El Segundo, Calif.

Circle No. 227 on Inquiry Card.

LITERATURE

Multiplexer

A booklet describes multiplexing techniques and capabilities of the TC-100 Concentrator, a general purpose EDP communications multiplexer. Tel-Tech Corp., Silver Spring, Md.

Circle No. 317 on Inquiry Card

Dual Inline Packaging

Dual inline packaging, a new concept in high density packaging of dual inline integrated circuit modules, is described in a 20-page designer's catalog. Scanbe Mfg. Corp., Monterey Park, Calif.

Circle No. 302 on Inquiry Card

Wirewound Resistors

Precision wirewound resistors for governmental and commercial applications are discussed in 44-page illustrated, Pub. LA-194, including specifications. Shallcross, Selma, N.C.

Circle No. 314 on Inquiry Card

Sub-Miniature Indicator Lights

Two terminal sub-miniature indicator lights, designed for mounting in $^{15}/_{32}$", $^{1}/_{2}$" and $^{17}/_{32}$" clearance hole are described in this twelve page, two color catalog. Dialight Corp., Brooklyn, N.Y.

Circle No. 300 on Inquiry Card

Flat Ribbon Cable

This data sheet details the advantages and specifications of VERIL-OCAP® low capacitance round conductor flat ribbon cable. Spectra-Strip Corp., Garden Grove, Calif.

Circle No. 316 on Inquiry Card

Data Communication Systems

A 24-page brochure includes information on data communication systems, designed for military tactical use. Canoga Electronics Corp., Electronic Systems Div, Chatsworth Calif.

Circle No. 315 on Inquiry Card

Fluidic Flip/Flop Amplifier

A product specification sheet for a fluidic flip/flop amplifier describes the 4NF2 as a bistable element that may be used on almost any type of fluidic system powered by gas or air. Micro Switch, Div of Honeywell, Inc., Freeport, Ill.

Circle No. 301 on Inquiry Card

Hardware Components

This catalog describes and illustrates a complete line of sockets, carriers, contactors, and breadboards for integrated circuits, M.S.I. and L.S.I. devices, transistors, relays and operational amplifiers. Barnes Corp., Lansdowne, Pa.

Circle No. 305 on Inquiry Card

Capacitors

These engineering bulletins cover Type 164D solid-electrolyte RED TOP® TANTALEX capacitors and Type 151D non-polarized hermetically-sealed TANTALEX capacitors. Sprague Electric Co., North Adams, Mass.

Circle No. 308 on Inquiry Card

Power Supplies

Catalog No. 691 gives complete electrical and mechanical specifications, and prices, of thousands of power supplies, including regulated ac-dc, regulated dc-dc, unregulated ac-dc, dc-ac. Technipower, Inc., Ridgefield, Conn.

Circle No. 310 on Inquiry Card

Desk Top Modem

This 2-page technical bulletin illustrates and describes a solid-state modem which receives and transmits digital data over voice-grade telephone lines at 2400 bits a second. Ultronic Systems Corp., Moorestown, N.J.

Circle No. 321 on Inquiry Card

Time Sharing Computer System

A four-page folder describes how the 940 Time-Sharing Computer System is being used by 300 to 400 personnel at TRW Systems Group, Redondo Beach, California. Scientific Data Systems, El Segundo, Calif.

Circle No. 318 on Inquiry Card

Core Memory Systems

Bulletin TB503 describes ECOM, first in a series of economical core memory systems, designed for service in general system applications requiring high-speed, random access to moderate amounts of digital data. Standard Memories, Inc., Sherman Oaks, Calif.

Circle No. 306 on Inquiry Card

Read-Only Memory

The 4-page Bulletin 1000B contains system specifications, timing diagram, block diagram, principles of operation and a discussion of the Read-Only Memory State-of-the-Art using the braid transformer principle. Memory Technology Inc., Waltham, Mass.

Circle No. 320 on Inquiry Card

Digital Tape Memories

This case history G293 describes the use of Model TM-7 digital tape memories by the Laboratory for Electronics and Nucleonics (LABEN), Milan, Italy, to prepare space-telemetry data for computer processing. Ampex Corp., Redwood City, Calif.

Circle No. 313 on Inquiry Card

You probably aren't our kind of engineer.

No offense intended. We just know what we want.

We're computer memory specialists. If you know our products, you know we're good.

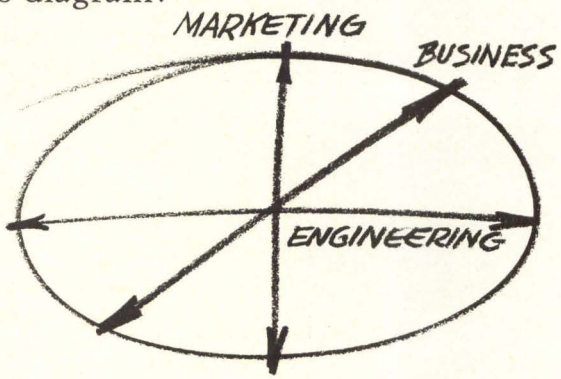
Not surprisingly, we're growing fast.

So we need engineers. Good minds. Good technical backgrounds. But that's not all.

You see, back when we were small we learned an important lesson. Each of our engineers had to get involved in everything: research, design, costing, marketing, production – you name it. Being involved, they became committed. And worked better for it.

That's how we got our reputation for doing what we do better than anyone else. We intend to keep it.

That's why we take such a close look at all applicants for our engineering positions. We'll talk to you about interests and aspirations and experience. And, at some point along the line, we'll draw this diagram:



It's the essence of what we mean by our kind of engineer. An interest in and understanding of all aspects of our company's activities. You could call it balance. Whatever it is, it works for us.

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We make memory systems and stacks and planes and printed circuits. We're looking to the future with research in plated wire and films. And we're in the process of introducing a brand new product: MAC 16, a compact, inexpensive Multi-Application Computer. Our division is going to keep right on growing. And we'll need even more of our kind of engineers.

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LOCKHEED ELECTRONICS COMPANY

Data Products Division of Lockheed Aircraft Corporation

CIRCLE NO. 900 ON INQUIRY CARD

Data Set

A data set that transmits/receives asynchronous serial digital data over direct distance dialing (DDD) networks at rates from 0 to 120C bps is described in Bulletin 5305. Sangamo Electric Co., Springfield, Ill.

Circle No. 307 on Inquiry Card

Control Module Handbook

The 1969 edition of the Control Handbook contains useful information on the latest techniques and products available for implementing faster, cheaper and more reliable solid state electronic control systems. Digital Equipment Corp., Maynard, Mass.

Circle No. 311 on Inquiry Card

Subminiature Rotary Switches

A line of one-half diameter subminiature rotary switches—designed for applications where extreme compact size is essential—is described in a new two-color technical bulletin. Oak Mfg. Co., Div of Oak Electro/Netics Corp., Crystal Lake, Ill.

Circle No. 304 on Inquiry Card

General-Purpose Relays

Cataloged in a 4-page bulletin on the general-purpose Series 68 relay are more than a thousand possible combinations of such electrical and physical features as contact arrangement, contact material, coil voltage, terminals, mounting styles, and enclosures. Sigma Instruments, Inc., Braintree, Mass.

Circle No. 303 on Inquiry Card

Capability Brochure

A 4-page brochure describes in detail many of the technical operations and varied services available from the Magnetics Operations group. Also included is a section on a line of standard power supplies. Bourns, Inc., Magnetics Operations, Trimpot Products Div., Romoland, Calif.

Circle No. 309 on Inquiry Card

the Honeywell man. he's an enthusiast!

At work, or play, he's committed to meeting a challenge. He doesn't go for half-way measures — whether tackling the ski trails of nearby Maine, New Hampshire or Vermont, continuing his education in Boston, or designing and developing highly sophisticated computer systems.

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CIRCLE NO. 901 ON INQUIRY CARD

COMPUTER DESIGN INDEX 1967 & 1968

An up-to-date listing of feature articles that have been published in Computer Design since January 1967.

Logic Designers:

Help IBM develop large-scale data processing systems.

We need logic designers to develop the hardware for large-scale scientific systems, designed to solve complex problems having extremely large computational loads. Loads that are found in such areas as weather forecasting, radiation burst effects, or signal processing.

Imaginative new concepts.

Advanced concepts in system architecture are being explored to achieve exceptionally high data processing rates.

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If you qualify, you could get in on the ground floor of important advances in large-scale computation.

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This development program is just one of the many we have at IBM's Federal Systems Division, located near Washington, D.C.

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It has been these kinds of advanced programs that have kept IBM a leader in the information processing industry.

Call or write.

Learn more details. Call Jim Dunn at (301) 921-7724 any weekday between 9 and 4:30. Or, if you prefer, send a brief letter or resume to him at IBM Corporation, Federal Systems Division Headquarters, Dept. BM-1039, 18100 Frederick Pike, Gaithersburg, Maryland 20760.

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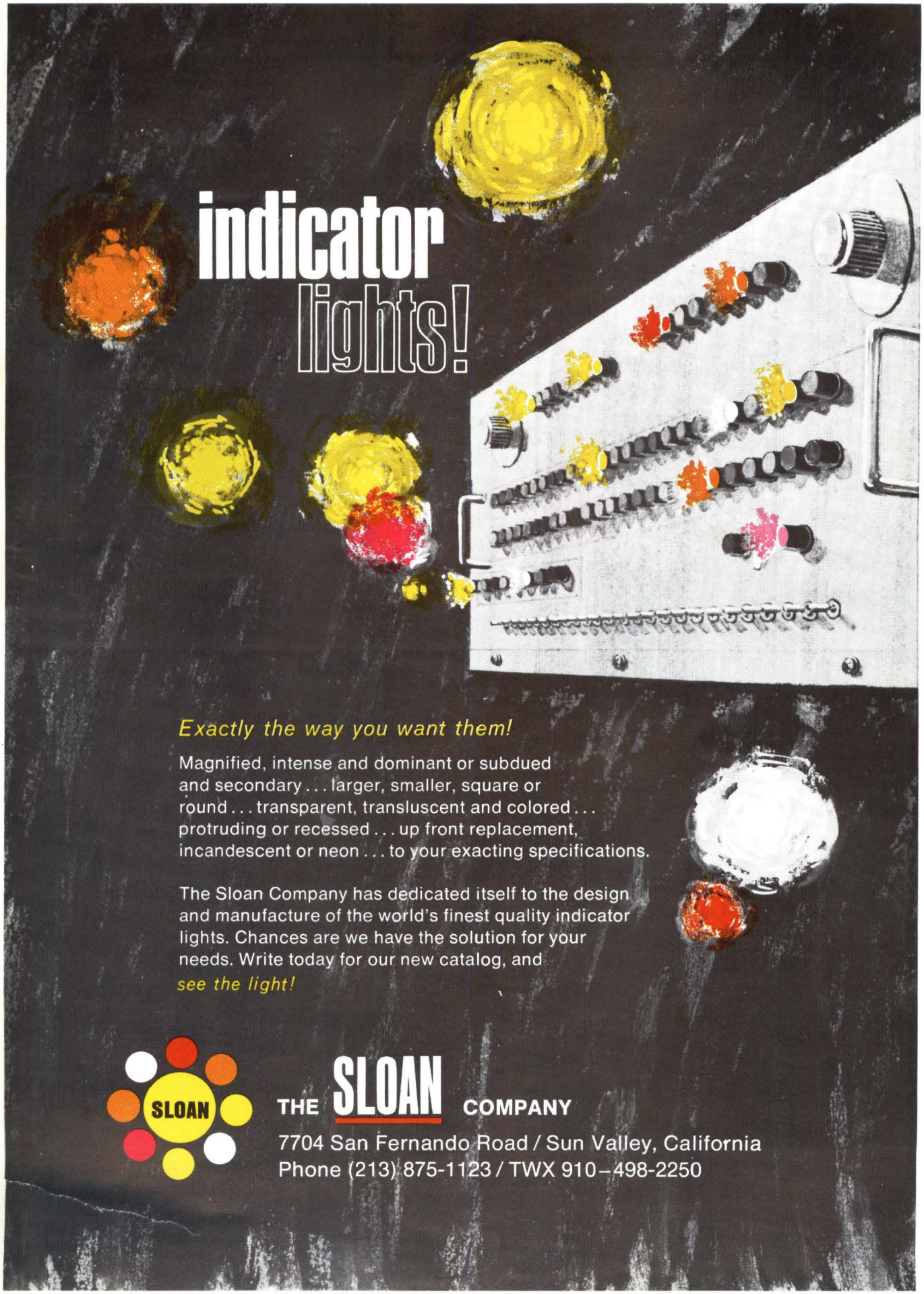

CIRCLE NO. 53 ON INQUIRY CARD

It's one thing to make a low cost digital tape unit, it's something else to make a low cost digital tape unit without compromise. Tally did.

From bare bones to full dress, Tally's new low price Series 4000 computer compatible digital tape units were built from the ground up with no compromises in design.

Series 4000 digital tape units are available and in production now. You can order the transport only with servo and capstan electronics. Or you can order the full dress version with read/write data electronics and complete interface logic.

Performance? Just Check All these Key Features.

- High speed rewind with servo controlled tape tension (another no compromise) takes 1½ minutes for a full 10½ inch reel of tape.
- Compact design handles full 10½ inch reels yet uses only 26½ inch panel space in a standard 19 inch rack. Hinged transport for easy access and front-end service.

- DTL logic or 7 and [illegible] formats. Special read only version can handle both formats without head change.
- Tape deck constructed from a rugged temperature stabilized precision casting. (Unique in the low cost field.)
- No periodic mechanical adjustments. (Another no compromise design feature.)
- Low mechanism forces and single capstan drive handle tape gently for long tape life.

Simply write or call our man Tom Tracy for more data. Tally Corporation, 1310 Mercer Street, Seattle, Washington 98109. Phone: (206) 624-0760. In the U.K. and Europe, address Talley Limited, 6a George Street, Croydon, Surrey, England. Phone: (01) 686-6836.

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