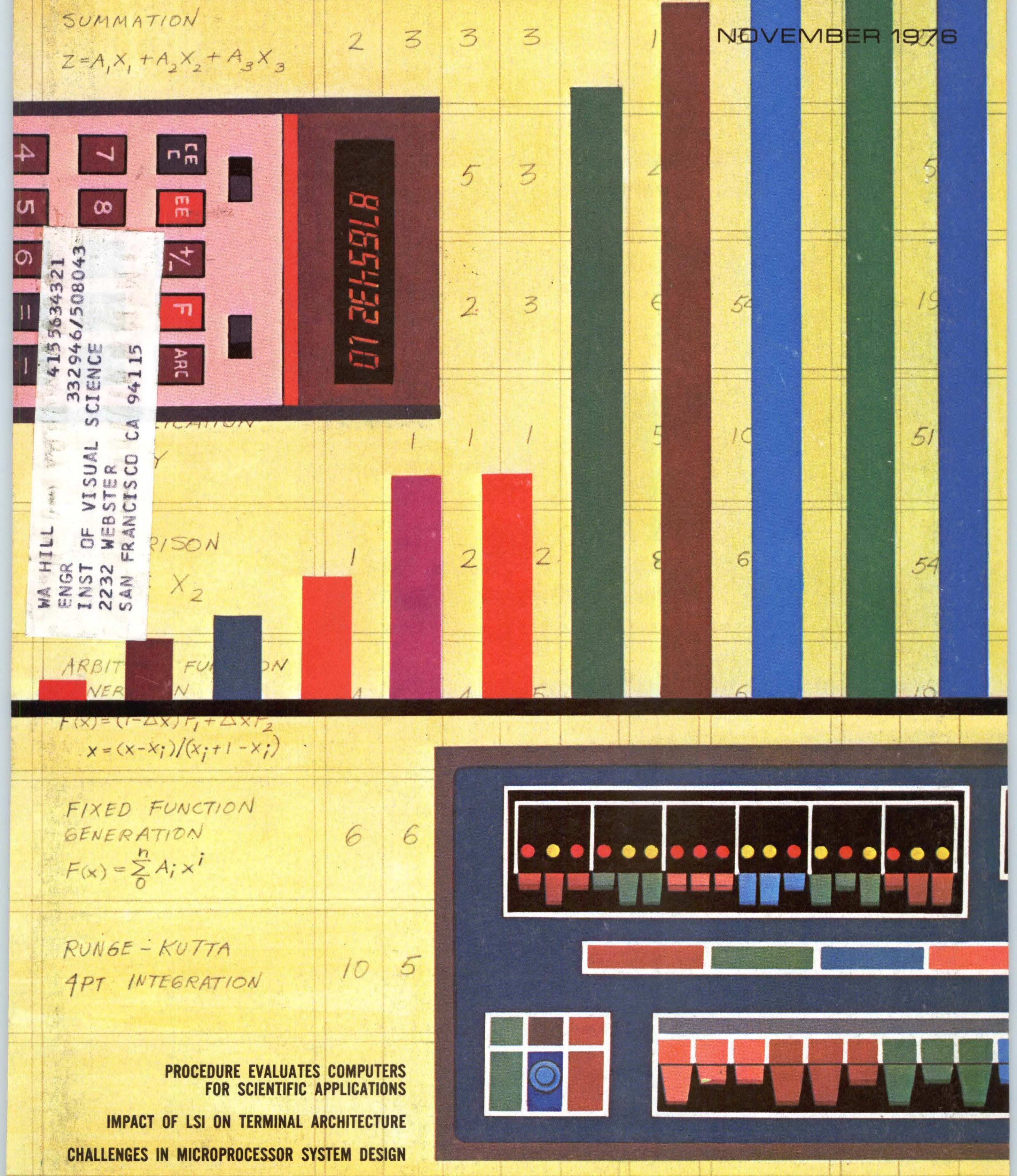
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

NOVEMBER 1976



PROCEDURE EVALUATES COMPUTERS FOR SCIENTIFIC APPLICATIONS

IMPACT OF LSI ON TERMINAL ARCHITECTURE

CHALLENGES IN MICROPROCESSOR SYSTEM DESIGN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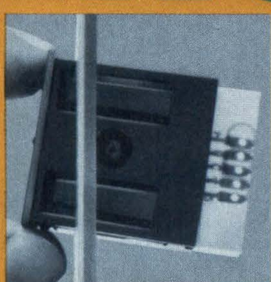

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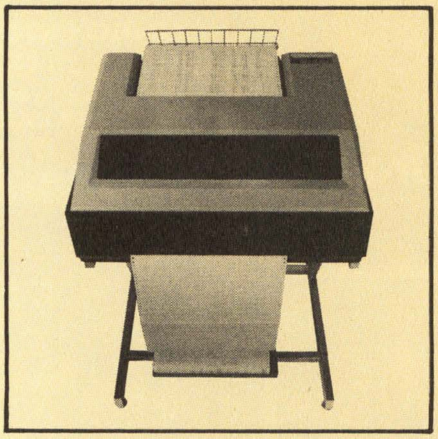

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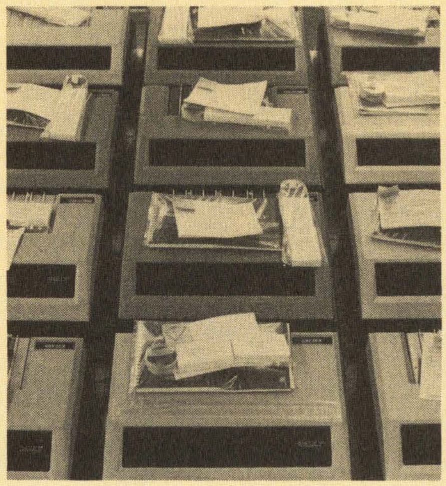

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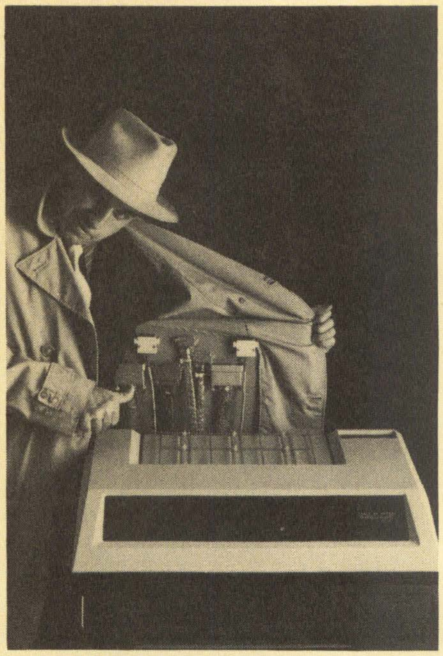

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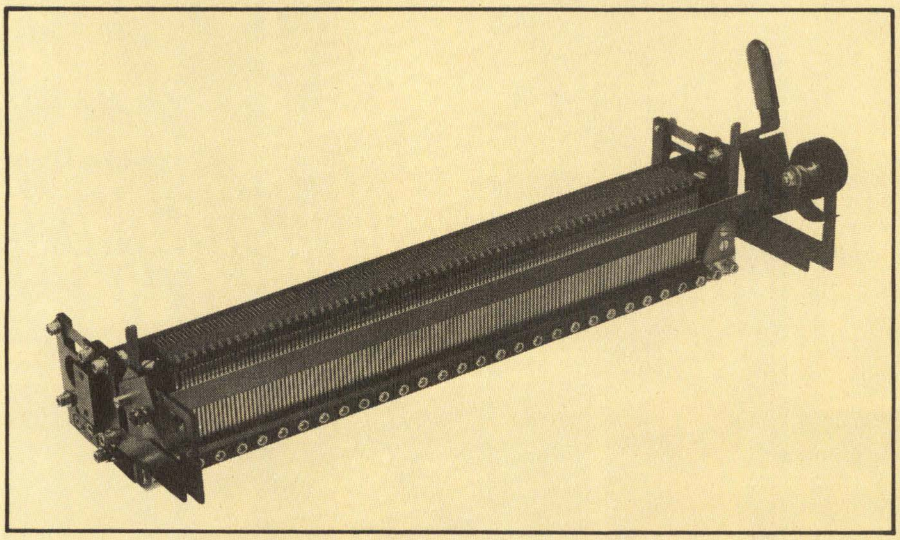

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THE
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OF DIGITAL
ELECTRONICS

COMPUTER DESIGN

NOVEMBER 1976 • VOLUME 15 • NUMBER 11

FOR A FREE SUBSCRIPTION, FILL OUT QUALIFICATION FORM STARTING ON PAGE 189

DEPARTMENTS

6 CALENDAR
10 LETTERS TO THE EDITOR
14 COMMUNICATION CHANNEL
27 DIGITAL TECHNOLOGY REVIEW
50 DIGITAL CONTROL AND AUTOMATION SYSTEMS
134 AROUND THE IC LOOP
142 MICRO PROCESSOR/ COMPUTER DATA STACK
162 PRODUCTS
183 LITERATURE
184 GUIDE TO PRODUCT INFORMATION
188 ADVERTISERS' INDEX
Qualification Form and Reader Service Cards pages 189-196

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FEATURES

74 INTERNATIONAL ELECTRON DEVICES MEETING

1976 IEEE IEDM will present 26 technical sessions stressing solid-state devices, device technology, energy conversion devices and quantum electronics, image transducers and optoelectronic devices, and integrated electronics

93 PROCEDURE EVALUATES COMPUTERS FOR SCIENTIFIC APPLICATIONS

by Louis Wolin

Based on a scientific mix, technique can be used to evaluate computer systems, selecting an optimum system and calculating an approximate required solution time for a given problem

103 IMPACT OF LSI ON TERMINAL ARCHITECTURE

by Peter G. Cook and Thomas B. Cheek

LSI technology offers the opportunity to reduce cost and increase reliability of terminals, and holds promise of a real breakthrough in product design if engineers watch for opportunities

109 CHALLENGES IN MICROPROCESSOR SYSTEM DESIGN

by Tom Jones and Peter Thomas

By treating a microcomputer system as if it were a small minicomputer, specifically designed for an entire line of products, manufacturers can take full advantage of today's microprocessor technology

120 LOW POWER COMPUTERS: A MAKE OR BUY DECISION

by Jerry Washburn

Many advantages exist for buying traditional low power minicomputers rather than building computers using microprocessor chips and other ICs

160 SMALL BUT VERY FAST MINICOMPUTER OFFERS LARGE-MACHINE PERFORMANCE

Smallest member of computer family meets computational and data collection requirements of scientific and data communications applications

STAFF

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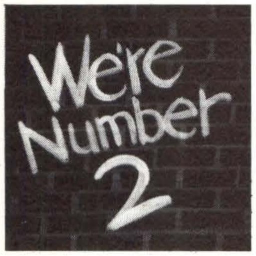
While other mini-makers have been pushing & shoving...

one company has quietly become number 2*.



They've quietly shipped over 9,000 computers. In fact, over 400 of their minis are going to OEM's every month.

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*In the number of minicomputers currently being shipped to Original Equipment Manufacturers.

CALENDAR

CONFERENCES

NOV 18, JAN 18, and FEB 14—1976/77 Invitational Computer Conferences, Dallas, Tex; Orange County, Calif; and Fort Lauderdale, Fla. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 204, Newport Beach, CA 92660. Tel: (714) 644-6037

NOV 23-25—COMPEC-UK (Computer Peripheral, Small Computer, and Systems Exhibition), Wembley Conf Centre, Wembley, Middlesex, England. INFORMATION: Trident Conferences and Exhibitions Ltd, Abbey Mead House, 23a Plymouth Rd, Tavistock, Devon PL19 8AU England

NOV 23-27—Conf-Exhibition of Automation and Instrumentation, Milan, Italy. INFORMATION: Federation of Scientific and Technical Associations, Piazzale Rodolfo Morandi, 2 (Piazza Cavour)-20121 Milano, Italy

NOV 25-DEC 1—electronica 76 (7th Internat'l Trade Fair for Components and Production Facilities), Munich Fairgrounds, Munich, Germany. INFORMATION: Münchener Messe- u. Ausstellungsgesellschaft mbH, München 12, Postfach 12 10 09, Messegelände, Germany

NOV 29-DEC 1—Nat'l Telecommunications Conf, Fairmont Hotel, Dallas, Tex. INFORMATION: J. H. Tilley, Gen'l Chm, Collins Radio Group, 1200 N Alma Rd, Richardson, TX 75080

DEC 6-8—Winter Simulation Conf, Nat'l Bureau of Stds, Gaithersburg, Md. INFORMATION: Dr Harold J. Highland, Chm, Data Processing Dept, State U Technical College, Farmingdale, NY 11735. Tel: (516) 420-2190

DEC 6-8—IEEE International Electron Devices Meeting, Washington Hilton Hotel, Washington, DC. INFORMATION: C. Neil Berglund, Bell-Northern Research, POB 3511, Station C, Ottawa, Ontario K1Y 4H7 Canada

DEC 6-9—Digital Equipment Computer Users Society (DECUS) Sym, MGM Grand Hotel, Las Vegas, Nev. INFORMATION: David Simler, DECUS, Maynard, MA 01754. Tel: (617) 481-9511, X6973

JAN 10-14—Data Communications Equipment Exhibition, U.S. Trade Center, London, England. INFORMATION: Anita F. Brownstein, Dept of Commerce, OIM, United Kingdom, Washington, DC 20230. Tel: (202) 377-4443

JAN 31-FEB 2—5th Annual ACM Computer Science Conf, Atlanta, Ga. INFORMATION: Vladimir Slamecka, Director, School of Information and Computer Science, Georgia Institute of Technology, Atlanta, GA 30332

FEB 7-9—WINCON (Aerospace and Electronic Systems Winter Convention), North Hollywood, Calif. INFORMATION: H. S. Abrams, Litton Systems, Inc, G&CS Div, 5500 Canoga Ave, Woodland Hills, CA 91364

FEB 16-18—IEEE Internat'l Solid State Circuits Conf, Philadelphia, Pa. INFORMATION: Lewis Winner, 152 W 42nd St, New York, NY 10036. Tel: (212) 279-3125

FEB 24-25—Sym on Design Automation and Microprocessors, Palo Alto, Calif. INFORMATION: W. M. vanCleemput, Gen'l Chm, Digital Systems Laboratory, Stanford University, Stanford, CA 94305. Tel: (415) 497-1270

FEB 28-MAR 3—COMPCON '77 Spring, Jack Tar Hotel, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

MAR 9-11—DATACOMM 77, Washington, DC. INFORMATION: Carol Iredale, DATACOMM 77, 60 Austin St, Newtonville, MA 02160. Tel: (617) 964-4550

MAR 21-23—IECI '77 Conf (Industrial Electronics and Control Instrumentation), Philadelphia, Pa. INFORMATION: W. W. Koepsel, Program Chm, IECI '77, Dept of Electrical Engineering, Kansas State U, Manhattan, KS 66506. Tel: (913) 532-5600

MAR 23-25—Fourth Annual Computer Architecture Sym, College Park, Md. INFORMATION: Dr Bruce Wald, Superintendent, Communications Science Div, Naval Research Laboratory, 4555 Overlook Ave, Washington, DC 20390

MAR 29-31—Computer Systems and Technology Conf, U of Sussex, England. INFORMATION: Conf Dept, Institution of Electronic and Radio Engineers, 8-9 Bedford Sq, London WC1B 3RG England

SEMINARS

NOV 22-24 and DEC 15-17—Intelligent Terminals; DEC 8-10 and FEB 2-4—Applied Network Engineering; and DEC 13-15 and JAN 24-26—Microprocessors and Microcomputers, San Francisco, Calif, New York, NY; Washington, DC, San Francisco, Calif; and Arlington, Va, Houston, Tex. INFORMATION: Institute for Advanced Technology, Control Data Corp, 6003 Executive Blvd, Rockville, MD 20852

NOV 29-DEC 1—Input/Output Systems Seminar, City Squire Motor Inn, New York, NY. INFORMATION: Input/Output Systems Association, PO Box 1333, Stamford, CT 06904. Tel: (203) 323-3143

DEC 6-8 and JAN 24-26—Data Entry Management and Supervision, Cherry Hill Inn, Cherry Hill, NJ. INFORMATION: Management Information Corp, 140 Barclay Center, Cherry Hill, NJ 08034 Tel: (609) 428-1020

DEC 6-8—Minicomputers; Project Management for Computer Systems; and Data Communications; and DEC 13-15—Systems Analysis and Design, New York, NY; Miami Beach, Fla; and New York, NY; and Houston, Tex. INFORMATION: Heidi E. Kaplan, Information Services Mgr, Dept 14NR, New York Management Ctr, 360 Lexington Ave, New York, NY 10017. Tel: (212) 953-7262

SHORT COURSES

DEC 1-3—Introduction to Microprocessor Based Systems Design, State U of New York at Stony Brook, Long Island, NY. INFORMATION: Kenneth Short, Dept of Electrical Engineering, SUNY at Stony Brook, Stony Brook, NY 11794. Tel: (516) 246-5985

DEC 1-3—Advances in Computer Graphics, DEC 6-9—Commercial Automatic Testing Systems, Sheraton Motor Inn, East Brunswick, NJ. INFORMATION: Registrar, The Center for Professional Advancement, Ramada Inn, Route 18, East Brunswick, NJ 08816

DEC 3—Microprocessor for Management, DEC 7-10—Basic Technology, and DEC 16-17—Integrated Circuits Failure Mode, Scottsdale, Ariz; Scottsdale, Ariz; and Phoenix, Ariz. INFORMATION: Integrated Circuit Engineering Corp, 6710 E Camelback Rd, Suite 211, Scottsdale, AZ 85251. Tel: (602) 945-4564

DEC 6-10—Digital Signal Processing, DEC 13-17—ECM and ECCM for Digital Communications, and Modern Digital Communications, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education Program, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

DEC 6-10 and DEC 14-16—Designing with Microprocessors, Monterey, Calif and St. Louis, Mo. INFORMATION: Edwin Lee, Pro-Log Corp, 2411 Garden Rd, Monterey, CA 93940. Tel: (408) 372-4593

DEC 13-17—Mini Computer Systems, Milwaukee, Wis. INFORMATION: John T. Snedeker, Dept of Engineering, U of Wisconsin-Extension, 929 N Sixth St, Milwaukee, WI 53203. Tel: (414) 224-4193

DEC 14-16—Applications of Modular Microelectronics and Microprocessors, Biscayne College, Miami, Fla. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

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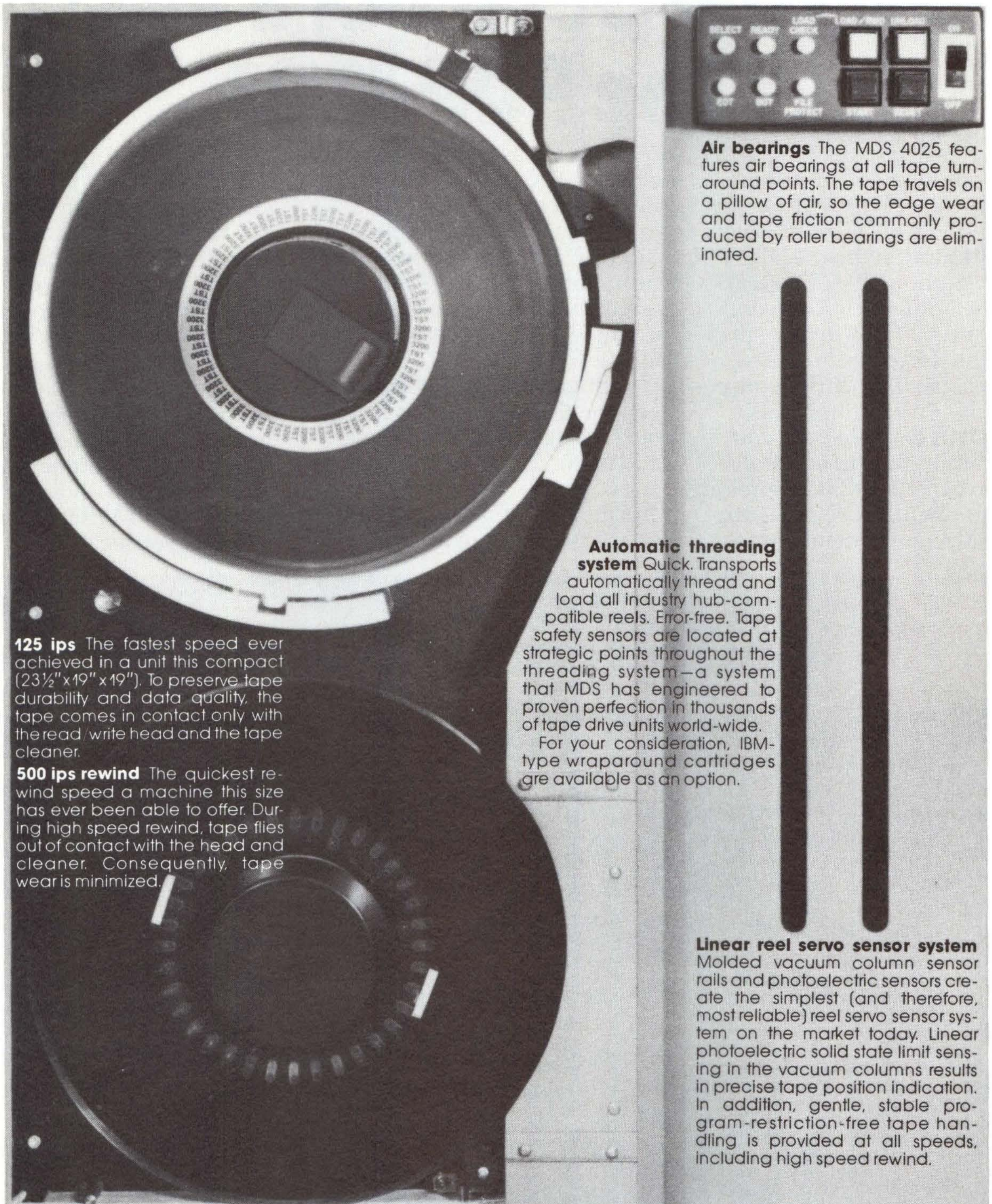

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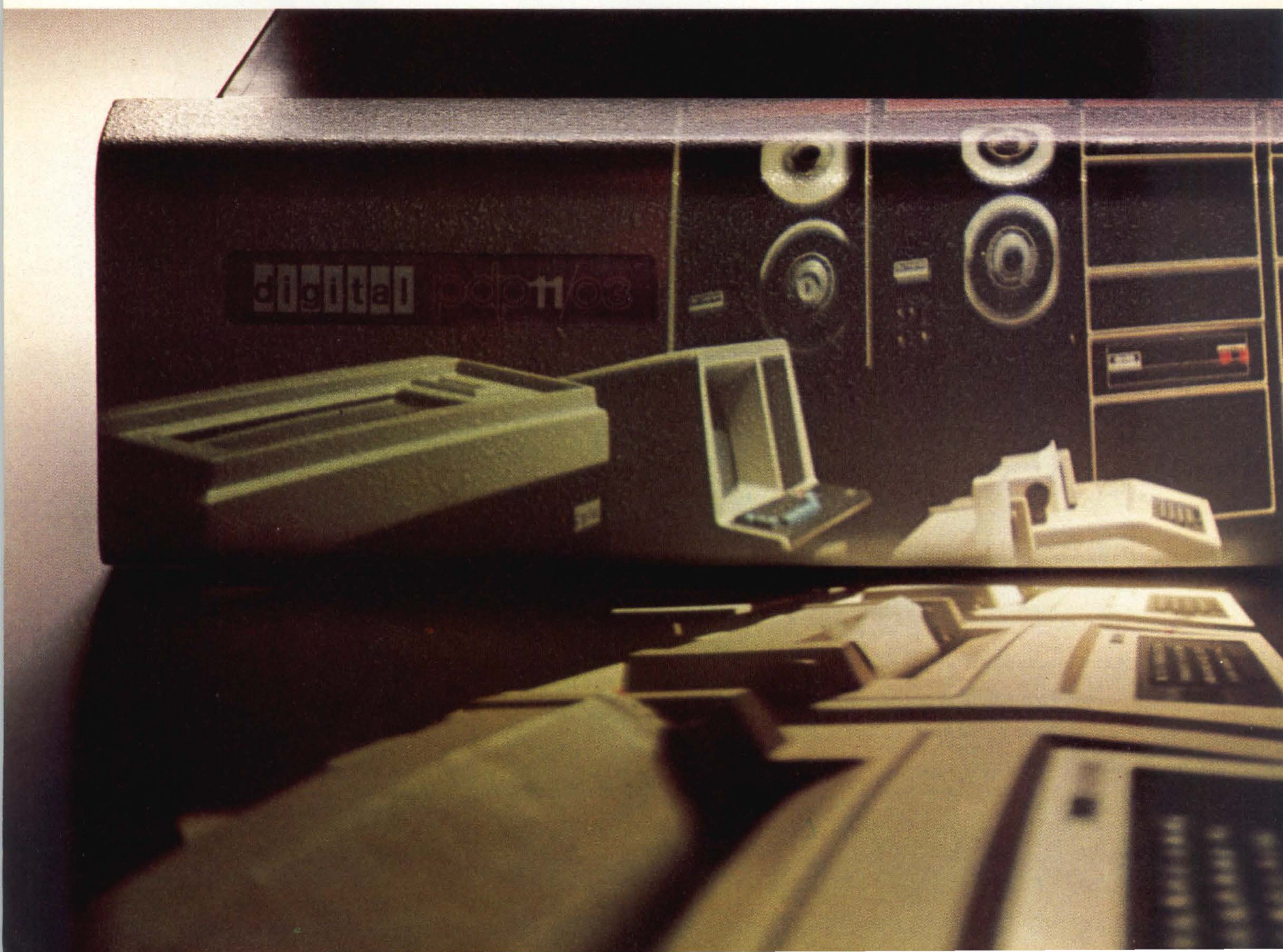

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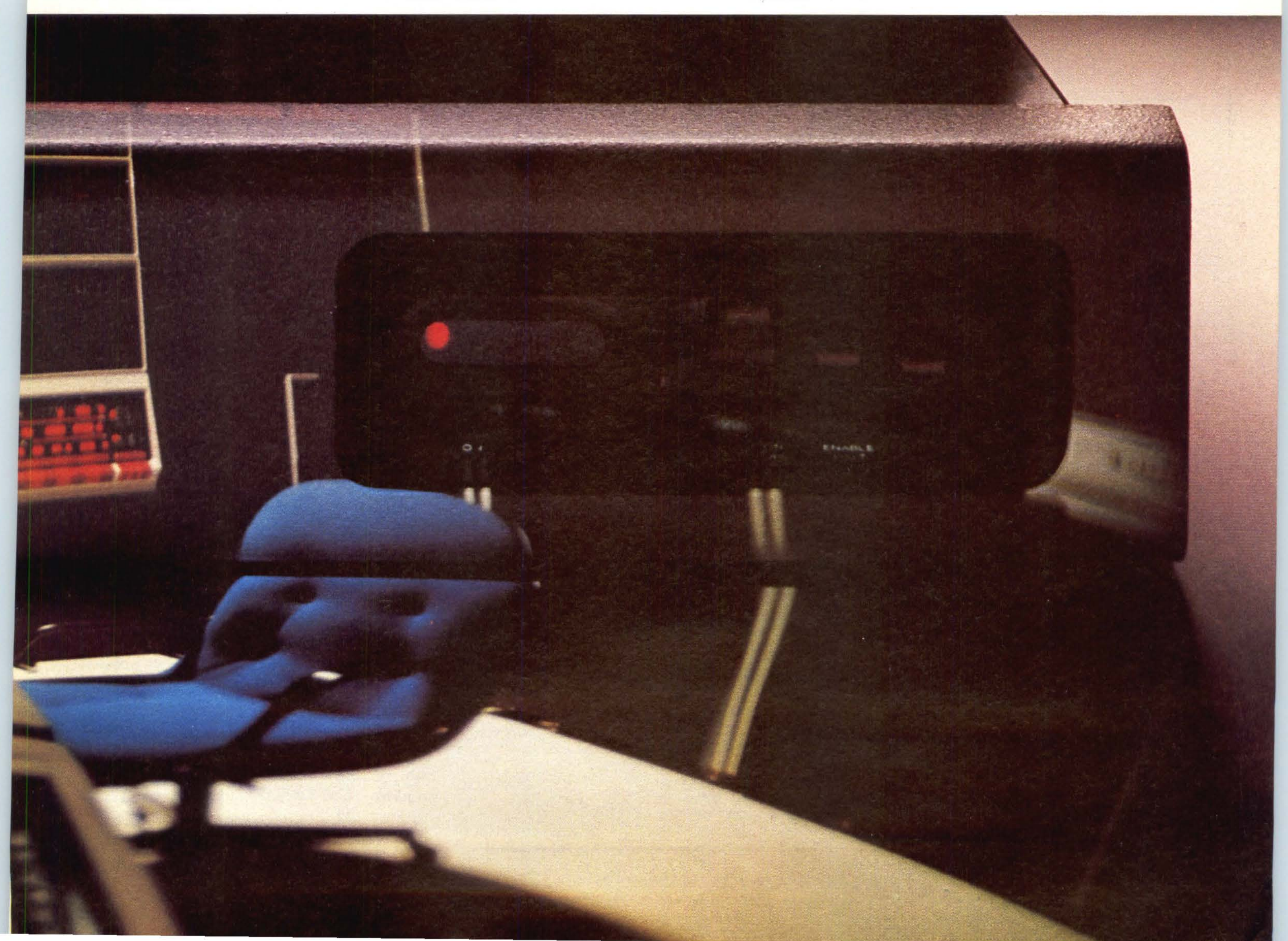


LETTERS TO THE EDITOR

To the Editor:

We are writing in regard to John Buckley's "Communication Channel" on "Computerized PBX Systems" in the May 1976 issue of *Computer Design*, pp 14, 19.

The IBM 3750 is mentioned as being recently introduced into the U.S. markets. We would be interested to learn of actual U.S. installations, since we understood previously that only overseas sales were being made by IBM.

Martin W. Fletcher
ComQuest Corp
Palo Alto, Calif

The Author Replies:

In response to your inquiry, you are correct in stating that IBM has only marketed the 3750 in overseas locations. While the 3750 has not been actively presented to the U.S. market, it has been selectively discussed in the context of a market study. Descriptive literature and manuals are available in the U.S.; however, they are written in terms applicable to the overseas communications environment. We also understand that there are 3750s installed in the U.S. at some IBM facilities. While there are a number of reasons for IBM's lack of direct 3750 U.S. marketing efforts, one of the more valid is the fact that the next generation 3750 is presently being developed by IBM in France under the project name "Rosebud."

Admittedly, the May column tended to imply that the 3750 was more active in the U.S. market. We can realistically anticipate, however, that IBM will agressively enter this market at some time in the near future.

John E. Buckley
Telecommunications
Management Corp
Cornwells Heights, Pa

Correction

An error was made in compiling the table showing the increase in word length caused by error correcting and detecting codes, appearing on p 180 of the article, "Automatic Error Correction in Memory Systems," by Bryan Rickard, *Computer Design*, May 1976. In the last six rows, the number of extra bits shown was incorrect in both columns; consequently, the percentage increase also was incorrect. The complete corrected table follows.

**Increase in Word Length
With Error Detection and Correction**

	Single-Error Correction		Single-Error Correction and Double-Error Detection	
Data Word Length	Extra Bits	Increase (%)	Extra Bits	Increase (%)
4	3	75.0	4	100.0
8	4	50.0	5	62.5
10	4	40.0	5	50.0
12	5	41.7	6	50.0
16	5	31.25	6	37.5
18	5	27.8	6	33.3
20	5	25.0	6	30.0
24	5	20.8	6	25.0
32	6	18.75	7	21.9
48	6	12.5	7	14.6
60	7	11.7	8	13.3
64	7	10.9	8	12.5
72	7	9.7	8	11.1
96	7	7.3	8	8.3

To the Editor:

While we appreciate the attention given to us in the "Communication Channel" column entitled "Satellite Business Systems" by John E. Buckley, *Computer Design*, June 1976, pp 10, 14, we would like to call attention to several inaccuracies in the article which should be corrected.

The estimated average cost of SBS earth stations to be supplied during the 1980-85 time frame is approximately $350,000, as our filings with the Federal Communications Commission show. Mr Buckley's estimate of $2000 is totally unrealistic for the kinds of stations SBS will utilize—each with a high power 14-GHz transmitter, a 12-GHz receiver with low noise amplifier, TDMA burst modulator/demodulator, and a satellite communications controller—all designed for reliable unattended operation.

While SBS will offer switched telecommunications services, they will be private network offerings to large industrial and governmental users. SBS services will not be analogous to direct distance dial service or to the Execunet service, and there is no intent to provide such services in the future.

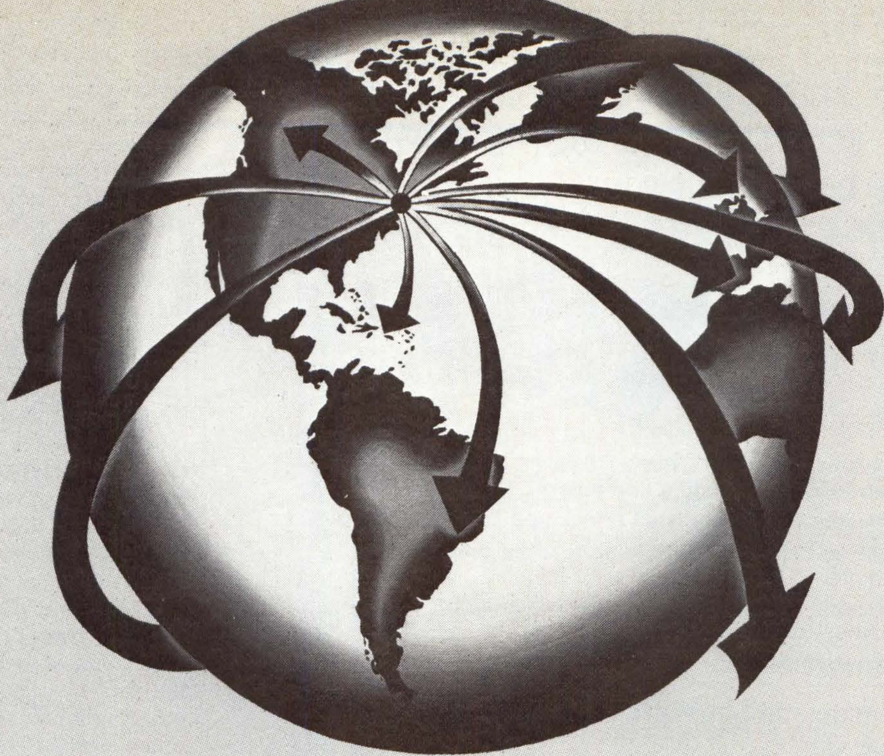
SBS's private network common carrier services are not the "closed" system service that the article postulates. The SBS system, as our filings emphasize, will include industry-standard interfaces and network accessibility without regard to the source of the customer's data processing equipment, and the service will be provided under tariffs which are nondiscriminatory.

Larry Weekley
Satellite Business Systems
Washington, DC

The Author Replies:

Many thanks for the acknowledgement of the June column. I regret that it appeared to reflect "inaccuracies" from your perspective. Perhaps the following additional views will resolve these concerns.

The primary earth stations for the SBS systems will indeed incur costs greater than $2000. One of the unique advantages of the SBS systems is that because of its frequency



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selection, an earth station of a few channel capacity is economically practical. Such low capacity earth stations could be placed at locations other than the primary earth stations. This ability would preclude the absolute necessity to always use land lines from a customer location to the primary earth station. The possible future cost of $2000 was intended to indicate a per channel cost objective that could be realistically obtained.

As your letter states, SBS will offer switched telecommunications services, which my column indicated. Regardless of the scope of access to such services, switched telecommunications services are analogous to direct distance dial service or to the Execunet service in that charges are only applicable for the time a channel was in use, and a specific channel is shared among a number of users over a period of time. The only difference between the statements in the column and your letter is the concept of how many users can have access to these switched services. This does not appear to be a valid component of a switched service definition. The column stated that once the SBS network is established, switched services can be expected. This projection is confirmed by your letter.

With respect to the third point of your letter, I suggest that you are overreacting to the concern stated in the column. It does not state that the SBS services will be a closed system service. It does state that a closed system may be able to be created. I am certain that the SBS tariff filings will express a nondiscriminatory intent. Such expressions, however, do not totally dispel the potential for such "closed" system concerns. Only historical experience with SBS after future operation will be able to effectively negate such concerns.

John E. Buckley
Telecommunications
Management Corp
Cornwells Heights, Pa

Letters to the Editor should be addressed:

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Professional Building
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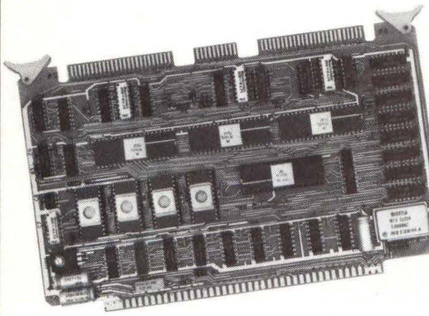
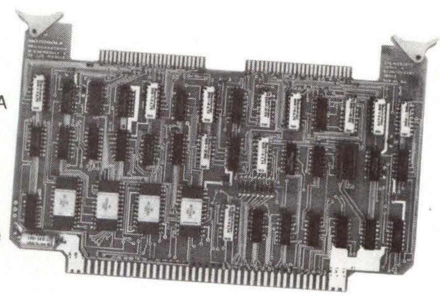
MOTOROLA introduces

micromodules...





Micromodule Family

Monoboard Microcomputers

M68MM01	Monoboard Microcomputer 1
M68MM01A	Monoboard Microcomputer 1A

Micromodule CPU

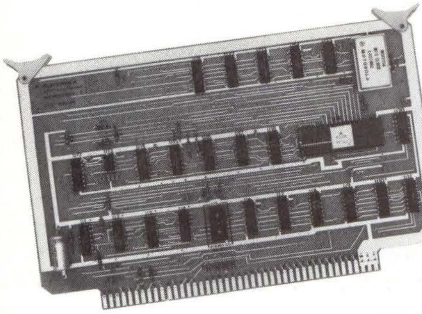
M68MM02	CPU Module

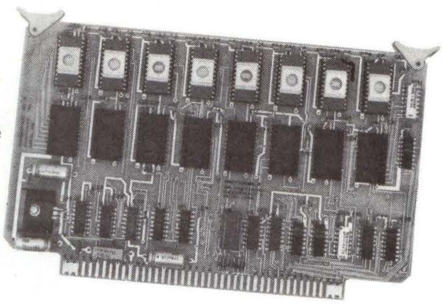
Micromodule System Expanders

M68MM03	32/32 Input/Output Module
M68MM04	8K/16K AROM/ROM Module
M68MM05A	8-Channel Differential 12-Bit A/D Module
M68MM05B	16-Channel Single-Ended 12-Bit A/D Module
M68MM05C	Quad 12-Bit D/A Module
M68MM06	2K RAM Module
M68MM07	Priority CPU Module
M68MM08	Microbug Module
M68MM09	CMOS/RAM Battery Module
M68MM10	Programmable Timer Module
M68MM12	GPIB Module
M68MM13	Ref State Detector Module

Applicable EXORciser Modules

- ACIA Module
- EROM/RAM Module
- 8K RAM Module
- 16K RAM Module
- Systems Analyzer





the flexible M6800 microcomputer alternative

Looking for a fast, low cost, microcomputer hardware design? Trying to avoid the costs of designing and building your own microcomputer system for relatively low-use rates? Looking for ways to build a custom computer with standard boards without big working capital requirements, increased labor force, big inventories, and a drain on cash flow?

Motorola's new M6800-based Micromodule* Family has the answers. You now have the choice you didn't have before. Take the single-board approach, or reach into our assortment of mix-'n-match module options and build your own customized system with standard boards.

Micromodules 1 and 1A are M6800-based 8-bit single-board microcomputers, Monoboard Microcomputers. MM 1 features all parallel I/O. MM 1A has both serial and parallel I/O.

Micromodule 2 is the M6800-based CPU module, the heart of the Micromodule Family's modular microcomputer concept. Use it with your choice of I/O, RAM, AROM/ROM, A/D, D/A, Programmable Timer and other Micromodule options.

Orders may be entered now for Micromodules 1, 1A, 2, 3 and 4, and ten additional Micromodules are already defined for this new microcomputer concept. As an example of the cost savings inherent in the concept, a single Micromodule 1, the M68MM01, sells for $485.00, and drops to $275.00 in 100 lots.

The total resources of Motorola's system development tools including the EXORciser*, EXORdisk*, and a full complement of software back up the Micromodule Family. The family also offers card cages, rack-mount chassis, and power supplies. Remember, too, that Micromodules and EXORciser modules are bus compatible.

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CIRCLE 10 ON INQUIRY CARD

by John E. Buckley
Telecommunications Management Corp
Cornwells Heights, Pa.

Dynamic Multiplexing Applications

Accessibility of information systems today is constantly being extended. System designers continue striving for a direct system interface that will provide closer access to the primary source data of a given application. Evolution of data communications terminals has been characterized by more lower speed, applications-oriented terminal devices. In order to improve the timeliness of source data as well as to increase the availability of existing data base information, the trend toward specialized terminals and low cost low speed terminals has continued.

Early online data communications systems used batch transmissions or remote job entry (RJE) terminals to develop and access a data base system. The primary system characteristic in need of improvement was the time-consuming task of manually collecting and preparing the required source data for system entry as well as the complexity of accessing that processed source data. Development of an interactive system capability has allowed the application of lower speed data communications terminals, permitting actual source data to be entered in a more timely manner. Most important has been the companion capability of enabling remote low speed terminals to interrogate and manipulate a centralized data base in order to obtain the desired information.

The increased number of low speed interactive terminals was paralleled with their increased geographical distribution. While the cost per remote terminal significantly decreased, the cost of centralized system access increased, if traditional network access methods were maintained. Batch or RJE terminals typically accumulated a large volume of data prior to system access. Access could then be established by means of a dial or switched connection. After the high speed exchange of data with the central processing site, the transmission connection could be disconnected, terminating any communications cost such as toll charges or measured WATS charges. If the terminal had a predictably large data volume and/or generated a number of batch data transmissions over an extended period of time, a leased line could be cost-justified. Such a line would be permanently installed between the terminal and the central processing site.

As lower speed data terminals were applied, data were not accumulated in any significant volume at remote locations. As each piece of source data became available it was to be directly entered to the centralized data base. With the same degree of urgency, immediate access was required when the need for data base information occurred. A number of truly interactive applications require availability of centralized information at the remote terminal location before new source data can be entered. This dual requirement intensifies the need for constant access to the central processing site.

In the United States, the primary communications channel in use is the voice grade channel. With a nominal bandwidth of 4 kHz, this channel is the vehicle for virtually all communications systems. Use of a batch or RJE terminal can easily fill the capacity of such channels during data transmission. A low speed interactive terminal operating at 150 bits/s or less does not begin to challenge the ultimate capacity of a voice grade channel. The solution to resolving the direct access, yet lowering cost access requirements of interactive applications, is to allow a number of low speed terminals within the same geographical area to share a common voice grade channel to the centralized computer site. This sharing must create the illusion at each remote terminal that a direct, dedicated connection exists to the centralized computer site without the awareness or participation of any other low speed terminals. This is done through multiplexing.

Multiplexing of digital data has been accomplished by allocating either the frequency spectrum or the time availability of the voice grade channel among the connected low speed terminals. Allocation of the frequency spectrum is known as frequency division multiplexing (FDM), while allocation of the time availability is known as time division multiplexing (TDM). FDM is also correctly referred to as space division multiplexing. With either technique, a fixed assignment of a portion of the frequency spectrum or the time availability of the shared voice grade channel is made to each of the connected low speed terminals. More information on these methods is contained in the May 1971 issue of *Computer Design*, "Communications

Introducing The compact 1 from number 1:

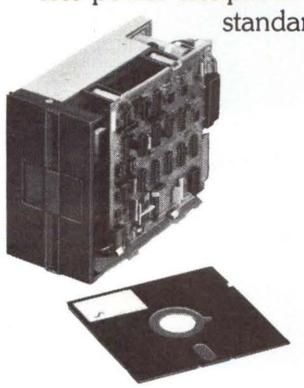
The minifloppy™ from Shugart

Give your system the performance of a floppy at a cassette price. Gain the random accessibility, mechanical reliability and data integrity of a flexible disk in a more affordable size. Go minifloppy.

This little half-pint is half the size, half the cost of a standard floppy but Shugart packs a lot of proven technology into that itty-bitty box (3.25″ x 5.75″ x 8.0″).

The same proprietary glass bonded ferrite/ceramic read/write head and recording technology used in 40,000 standard-sized Shugart floppy drives give the SA400 minifloppy dependable data integrity—$1/10^8$ soft errors, $1/10^{11}$ hard errors. You'll be hard pressed to find that integrity in any cassette. You won't get 110 K byte storage capacity at 125 K bit/second data transfer rates either.

Special minifloppy drive features include direct drive stepping motor actuator, DC servo-controlled spindle drive, and less power dissipation than any standard floppy.



The minidiskette media is just like the standard flexible disk, only smaller. Available in hard or soft sectored formats from several media sources, it shares the same oxide formulation, technology and technique of manufacture. Protective jacket is just 5.25″ square.

The Shugart minifloppy drive keeps data safe, too. Positive media interlock prevents minidiskette damage. Our standard write protect circuitry prevents loss of recorded information.

Low power consumption of only 15 watts in continuous duty and 7.5 watts in standby produces low heat and eliminates noisy fans.

Whether you build word processing equipment or an entry level microprocessor system, an intelligent calculator or a hobby computer, the Shugart minifloppy drive can help you bridge the price/performance gap between cassette and standard flexible disk.

The gap is gone. So put the minifloppy drive to work in your system before your competitor does. Write, call or run to Shugart for complete OEM information.

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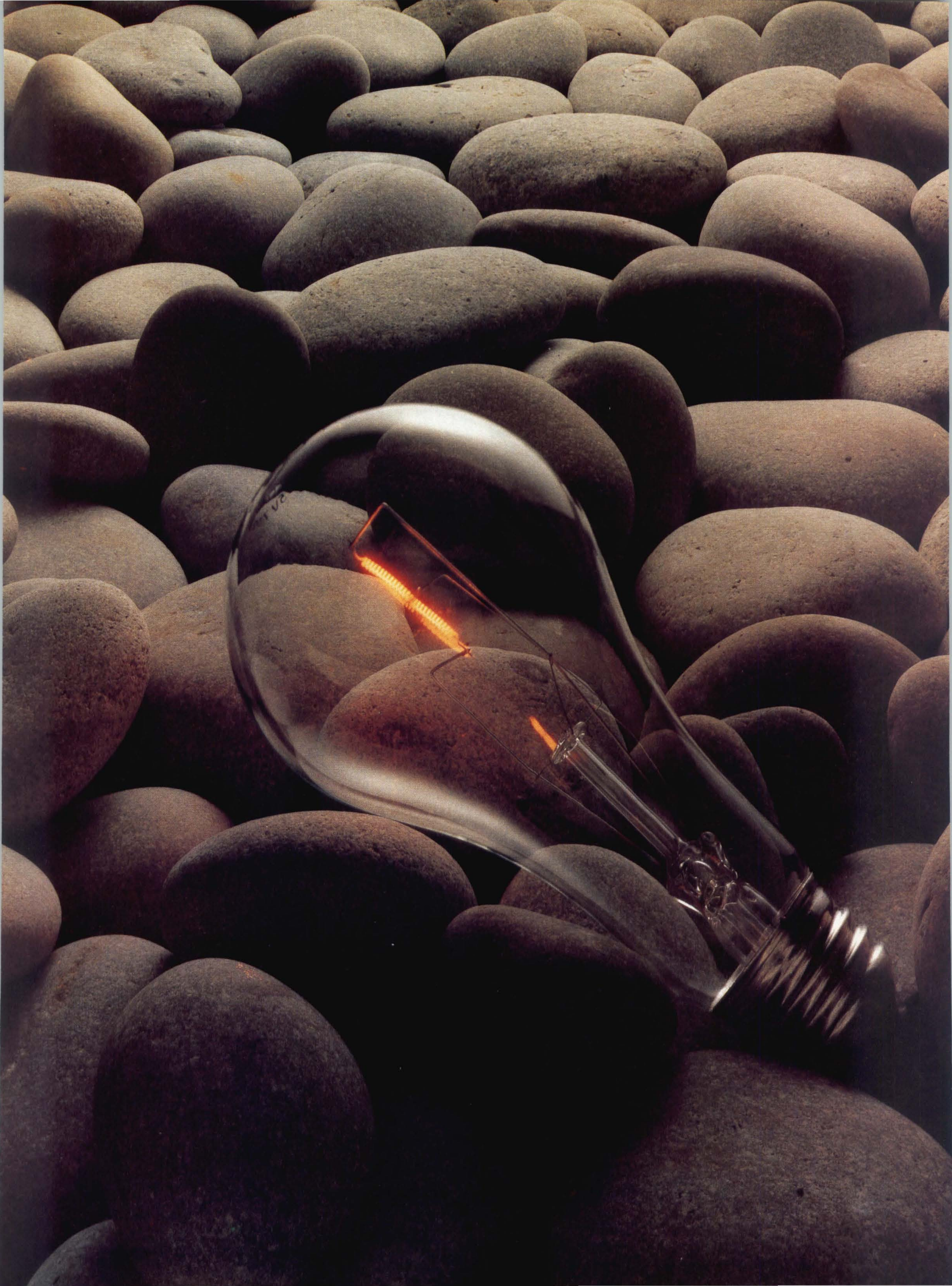

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The SEL 32/35 is the strongest price-performer of any 32-bit single or multiple-CPU system available today. These computers can be configured from 64K bytes to 512K bytes of 900 nsec memory. Resembling its more powerful brothers, the SEL 32/35 is a complete package, including central processor with floating-point arithmetic, memory, chassis, power supplies, and cabinet.

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Channel," "Digital Multiplexer Fundamentals," pp 14, 17. (The author will forward a copy of this article to readers who send a self-addressed, stamped envelope with their request.)

Capacity of fixed multiplexing methods can easily be calculated by the following methods. With FDM, the effective bandwidth of the voice grade channel is an aggregate of the bandwidth required by each of the low speed terminals. If each of the terminals operates at 150 bits/s, each will require a bandwidth of at least 200 Hz. The *effective* bandwidth of a voice grade channel is typically 2400 Hz. This means that a total of 12 such terminals can jointly use the common voice grade channel. With TDM, the capacity of the common voice grade channel is a multiple of the highest data rate of the low speed terminals. If the voice grade channel is operating at 4800 bits/s and the terminals at 150 bits/s, approximately 32 terminals can jointly use the common channel.

With these traditional multiplexing methods the assignment of a low speed terminal to a specific portion of the common frequency spectrum or to a defined time interval within the data bit stream being clocked on the common voice grade channel is fixed or static. Even when the associated low speed terminal is not generating a data character, the assigned, yet unused frequency spectrum or time slot may not be reassigned to any other terminal's data.

Examination of typical interactive low speed terminal operational characteristics indicates that most of these terminals are direct keyboard or manual entry. Physical depression of a key results in a coded byte being generated to the communications line of the character represented by the depressed key. If a key is not being depressed, the associated input communications line is idle, which occurs 70 to 80% of its available time. It seems logical that if this time could be assigned to other input data sources, the capacity of the shared voice grade line would be significantly increased. Thus, reallocation of idle input time is the basis for the dynamic multiplexer.

Limited to TDM, the dynamic multiplexer maintains an awareness of the activity level of each associated low speed terminal. When a character is being generated from a terminal, a time slot on the common voice grade line is assigned for transmission to the central processing site. During the subsequent frame transmission, that same time slot will be used to transmit a character for another low speed terminal. The term statistical or pause multiplexing describes this same technique of dynamic multiplexing.

In theory, such a dynamic allocation of available time slots can significantly increase the capacity of the common voice grade channel over the absolute limits of static TDM. In practice, the advantage of increased capacity is coupled with two disadvantages—data entry contention and data byte identification.

It is highly probable that more characters than available time slots will be generated simultaneously by the terminals. If the common voice grade channel is operating at 4800 bits/s and the low speed terminals at 150 bits/s, only 32 time slots exist within a single frame. If 33 characters are generated simultaneously, one of them must wait for the following frame. This wait means that data queues or storage must be assigned to each input low speed terminal. Occasional contention conditions can then be compensated for by storing the delayed characters until later frames. Probability of manual data entry indicates that terminals which generated characters for the first frame will not have generated characters by the time the second frame must be transmitted.

The key to successful static time division is that each time slot is fixed to each low speed terminal's input. The first time slot of the frame is always from terminal 1, the second is always from terminal 2, etc. Since the source of the data content of each time slot changes with dynamic multiplexing, some means of constantly identifying the source of the time slot's data must be established. Two methods are used. The first is to assign an address byte with each time slot to identify the data content's low speed terminal source. As the number of terminals increases, size of the address field with each time slot must also increase. It is quite easy to begin to limit the capacity of such a system by the number of bits required for identification rather than data.

The second method is to affix to each frame a polynomial that, when modified and expanded by the previous polynomial and/or constants stored in the multiplexer, will map the input activity of each low speed terminal represented by that frame. This method is most frequently used with high capacity multiplexers. A possible disadvantage is that it is undesirable to directly interface the common multiplexed voice grade channel to the central computer. A companion multiplexer is required at the computer site for processing the polynomial and demultiplexing into individual low speed interfaces.

So far, we have only discussed dynamic multiplexing with respect to manual data entry. If low speed terminals use automatic data entry by means of remote terminal storage, the advantages will be sharply impacted. Use of paper tape, cassettes, etc to accumulate manually entered data prior to transmission will result in a burst of data characters that can exceed the limited data storage queues in the multiplexer. If each terminal is capable of generating 50 contiguous characters at 150 bits/s each time transmission is initiated, the incident of lost characters due to exceeding the limits of the input queue may be quite high. Future plans to perhaps implement such automatic transmission terminals should be considered carefully with any decision to implement dynamic multiplexers.

This concern for burst transmission must also be evaluated with respect to output data transmission. In response to an inquiry, the central computer attempts to transmit contiguous characters at the established low speed data rate. The computer must be programmed to recognize a full queue condition in the multiplexer and hold further output data character transfer to that low speed channel. Such recognition is naturally contingent upon the central site multiplexer providing the computer with some indication of when a full queue condition occurs. The decision to implement dynamic multiplexers must, therefore, also include an evaluation of the increased interface controls as well as processing overhead at the central computer site.

As with any device or technique, there are corresponding advantages and disadvantages. Both must be identified and evaluated in view of the capabilities and requirements of each specific application and system.

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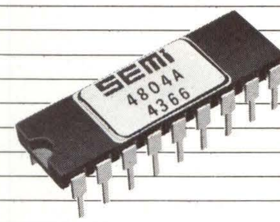

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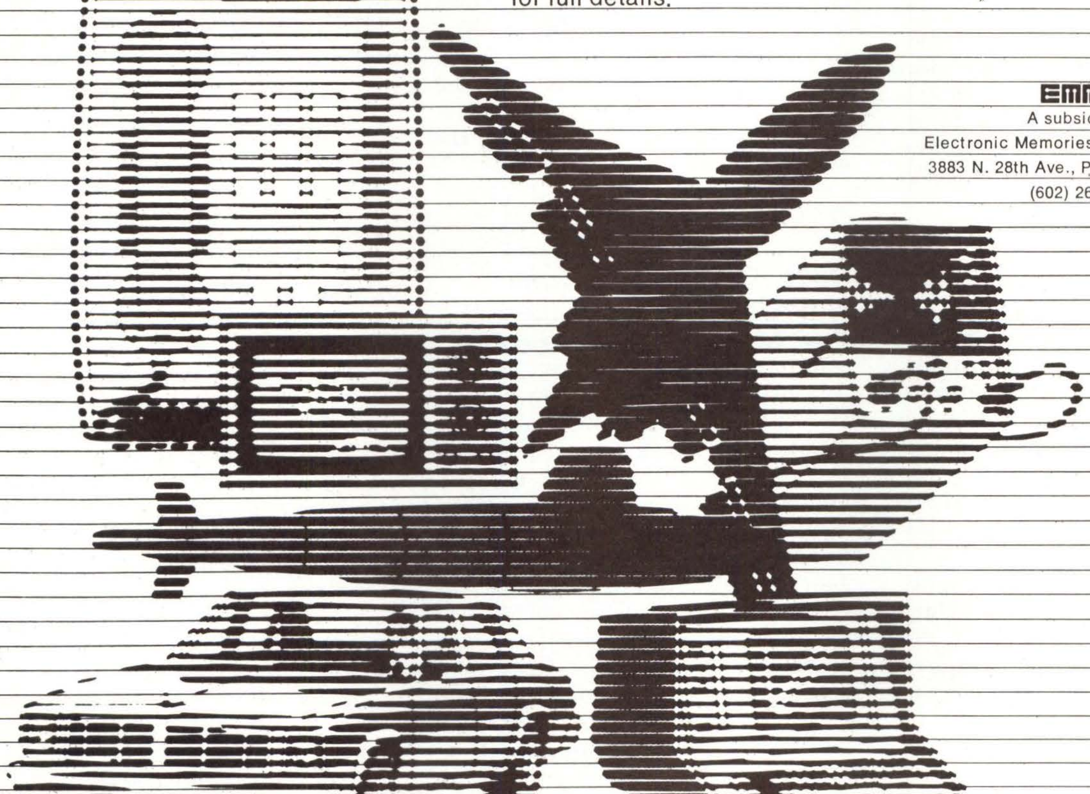

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Early Approval By FCC Requested for Domestic Communications Satellite

In response to petitions opposing its entry into the field, Satellite Business Systems (SBS) of Washington, DC has requested the FCC to approve—without further proceedings—its applications for a domestic satellite communications system. The company, a partnership formed by subsidiaries of COMSAT General Corp, IBM, and the Aetna Casualty and Surety Co, claims that its system proposals fully meet the broad domestic satellite policies established by the FCC. "Meticulous attention" was supposedly paid to conformance with the particular standards and conditions of the balanced CML entry option set forth in the Commission's CML decision of Feb 1975.

Applications were filed with the FCC in Dec 1975 for authority for SBS to construct a domestic satellite system to operate at the higher 12/14-GHz frequencies. This would reportedly provide customers with their own all-digital, switched private communications networks and with end-to-end voice, data, and image services among small satellite earth stations located on their premises. A favorable decision was requested by late 1976 so that the system could begin operation in 1979.

Claims for the proposed system include system concepts and communications techniques that would promote the public interest by serving important private network communications requirements and fostering a pro-competitive environment. Systems applications are said to be "developed fully within the context of the Commission's efforts to infuse competition into the provision of specialized or private line communications services."

The company said that its applications "provide copious detail which equals or exceeds the quantity of information the Commission required in granting initial authorizations to the carriers already providing domestic satellite services. In addition, further particulars are being provided in this response to assure that the Commission has before it all of the relevant information necessary to support a finding that grant of the applications will advance the public interest."

An evidentiary hearing "would not yield additional information of a substantial or material nature," according to SBS. "Instead, such a hearing would increase the risks the company must already face in entering the field, and would effectively advance the carriers' private interests, by postponing, and perhaps aborting, the advent of a vigorous competitor. An evidentiary hearing would certainly frustrate the FCC's public interest goals and radically depart from the procedural standards which the Commission has adopted and applied consistently in the past with respect to domestic satellite applications for competitive services."

SBS also noted that "although the Department of Justice had joined the carriers in calling for an evidentiary hearing on antitrust questions, the Justice Department has not previously interposed objections to consortium arrangements such as SBS in the domestic satellite field which might be considered to have antitrust implications. Instead, the Justice Department has wisely encouraged the Commission to permit entry by any qualified applicant, and it has recognized the dampening effect which lengthy evidentiary hearings are likely to have. To insist upon a hearing to determine unascertainable future facts would be contrary to the public interest and to the goals of the antitrust laws."

Data Communications Newsletter Introduced For Management Readers

A monthly newsletter "designed to take the myth out of data communications" was scheduled to begin publication in October as an information aid for business executives. *Datacomm Awareness Report,* published by Management Information Corp, 140 Barclay Center, Cherry Hill, NJ 08034, at $70 per year, is intended "to give the reader, over a period of time, a well-rounded basic education on data communications; and to each month brief the reader on what is happening in the data communications field that may affect his business. This newsletter will also serve as a vehicle to bring data communications users together so that they may share their ideas and problems."

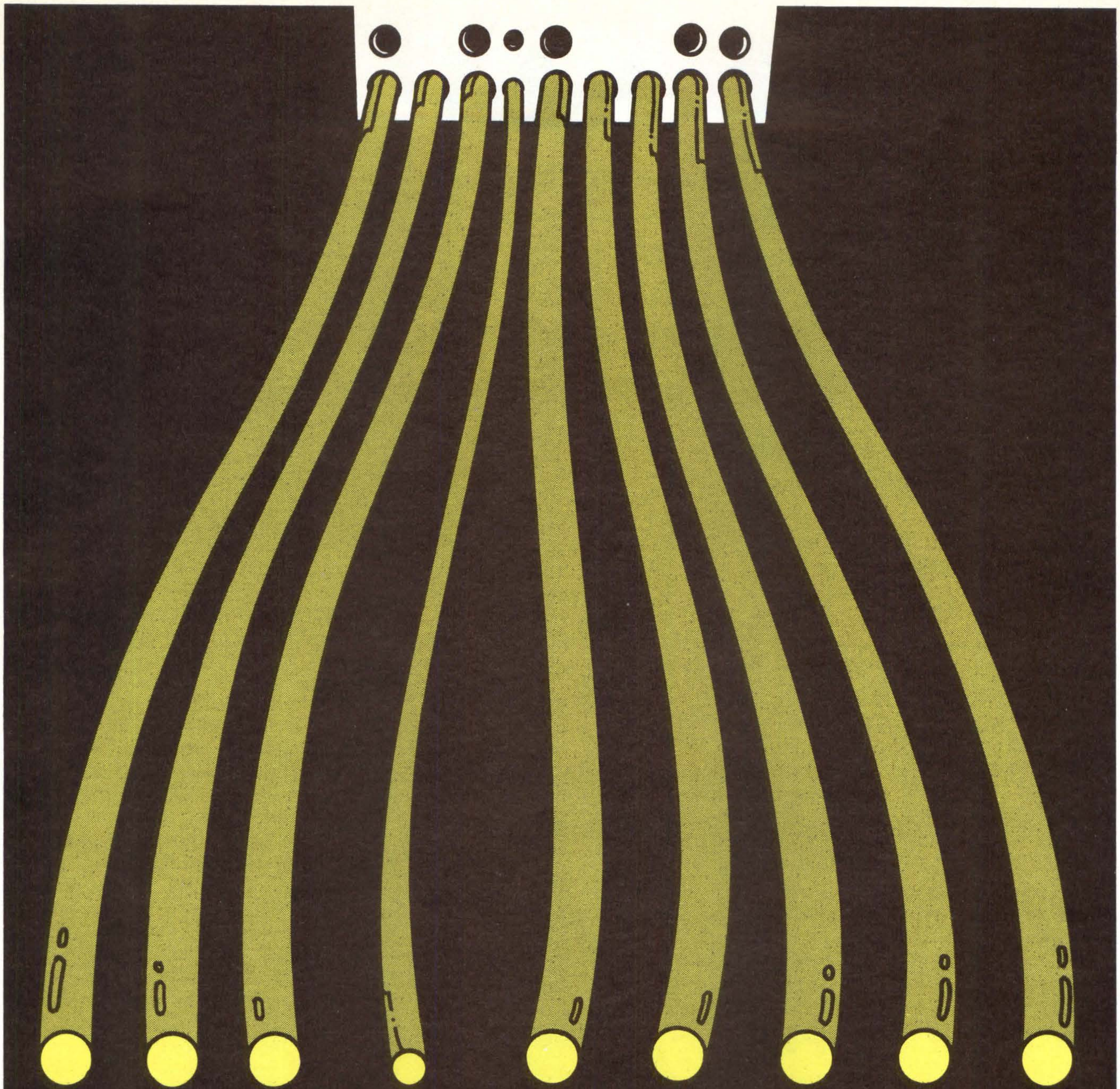
Fully involved with data communications, each issue will include commentaries on current items of significance, important news and interpretation as to how it may affect users, products and services of interest to users, tutorials on data communications basics written for the non-technical-oriented, analytical reports on one or two data communications products or services, application case histories describing how users in various businesses and industry sectors successfully applied equipment or services to solve their problems (or how they failed to do so and why), and an "Ask-the-Expert" section for specific questions related to user installations.

Charter Rates Reduced For Subscribers to Data Communications Report

Reduced charter rates have been announced for subscribers to *Datapro Reports on Data Communications,* a monthly updated information service for persons responsible for data communications oriented systems and networks. The service will contain comprehensive, in-depth information on the complete spectrum of data communications products, services, and techniques and will include three looseleaf volumes of reports; monthly report supplements; *Datalink,* a monthly data communications newsletter; and the firm's telephone inquiry service. Charter subscriptions from Datapro Research Corp, 1805 Underwood Blvd, Delran, NJ 08075 are $390, a $40 reduction from the regular rate of $430.

Designed to provide users and vendors with current, highly concentrated, and objectively prepared information to help them in planning, designing, and costing communications systems and networks; and to assist them in evaluating and selecting data communications equipment, software, and services, the service also includes operational and management guidelines to aid in measuring and optimizing installed systems.

Major information categories are: glossary; concepts; standards; management/system guidelines; computer vendor systems; processors; software; terminals; programmable terminals; batch terminals; display terminals; teleprinter terminals; transmission facilities; modems; multiplexers; test, monitor, and control equipment; special equipment and services; remote computing services; and telephone systems.

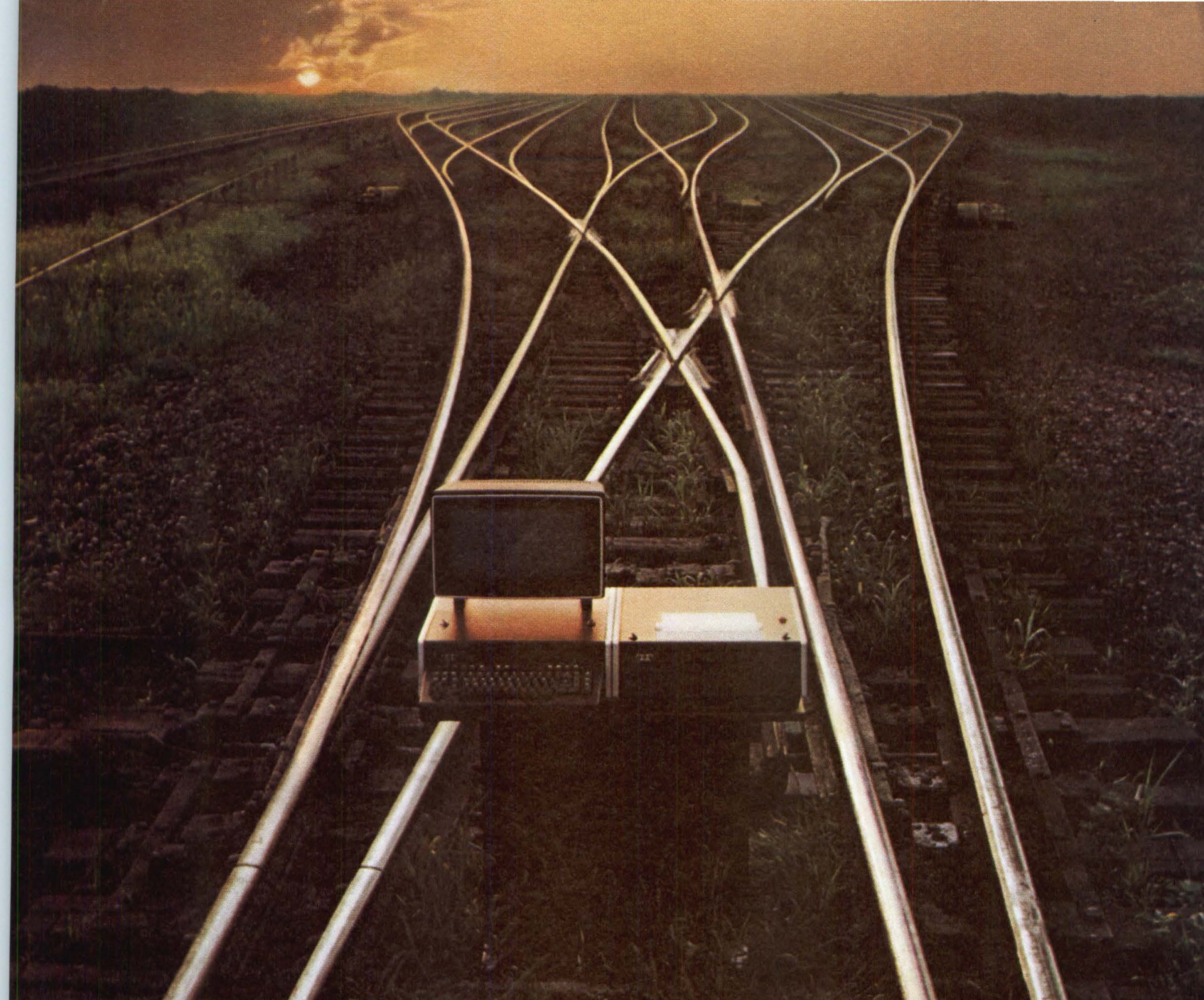


High Capacity Cable Expands Transatlantic Data Communications

Built to keep pace with the increasing volume of voice and data communications between the U.S. and Europe, a transatlantic telecommunications cable system dedicated on Sept 1 carries the equivalent of 4000 telephone conversations at one time. The 17-nation TAT-6 facility, which spans the 3402 nautical miles between Green Hill, RI and St. Hilaire de Riez, France, has the largest capacity of any undersea cable now in service. Increased capacity resulted from improved transmission capability and advances in repeater design that permit the use of much higher frequencies than earlier systems.

TAT-6 was developed jointly by the British Post Office, the French Secretariat of Posts and Telecommunications, and the American Telephone and Telegraph Co (AT&T). International partners include AT&T, ITT World Communications, Inc; RCA Global Communications; Inc; Western Union International, Inc; and telecommunications entities in Austria, Belgium, Denmark, France, Finland, Germany, Greece, Ireland, Italy, The Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom. About 20 other nations throughout Europe, the Middle East, and Asia will have circuits in the facility to serve their communications needs.

Bell Laboratories was responsible for the overall system design including specific design and development of equalizers and repeaters that amplify and control communications signals as they move along the undersea path and precision power supplies to energize these components from the terminal stations. Because the system operates at extremely high frequencies, the strength of the signal diminishes more rapidly than in previous cables. Therefore, repeaters must be placed every 5.1 nautical mi, compared to every 10 nautical mi for the next most recent Bell Labs-designed transatlantic system. Each repeater, built by Western Electric in Clark, NJ, will boost the signal power it receives as much as 10,000 times to compensate for transmission losses along the way. It must withstand water pressure at ocean depths of more than 3 mi during its 25-yr design life span. □



When it comes to flexibility, the model 40 gives you a lot of ways to go.

When we designed the model 40 system, we included a long list of features and options to give it the flexibility for practically any data transmission requirement. Whatever your industry or application.

First, there's a variety of speeds ranging from 110 to 4800 bps, along with a choice of interfaces, half/full duplex operation and character and batch mode transmission. The model 40 system also has a number of on-line controls, even/odd parity generation and a destructive scrolling feature that permits continuous bottom line reception with no loss of data until memory overflow.

Flexibility features don't stop there, either. There's an expandable memory with line and page scrolling, protected format with variable field transmission, plus many other features and options to select from. And since the entire system is modular, it can be custom-tailored to fit your needs.

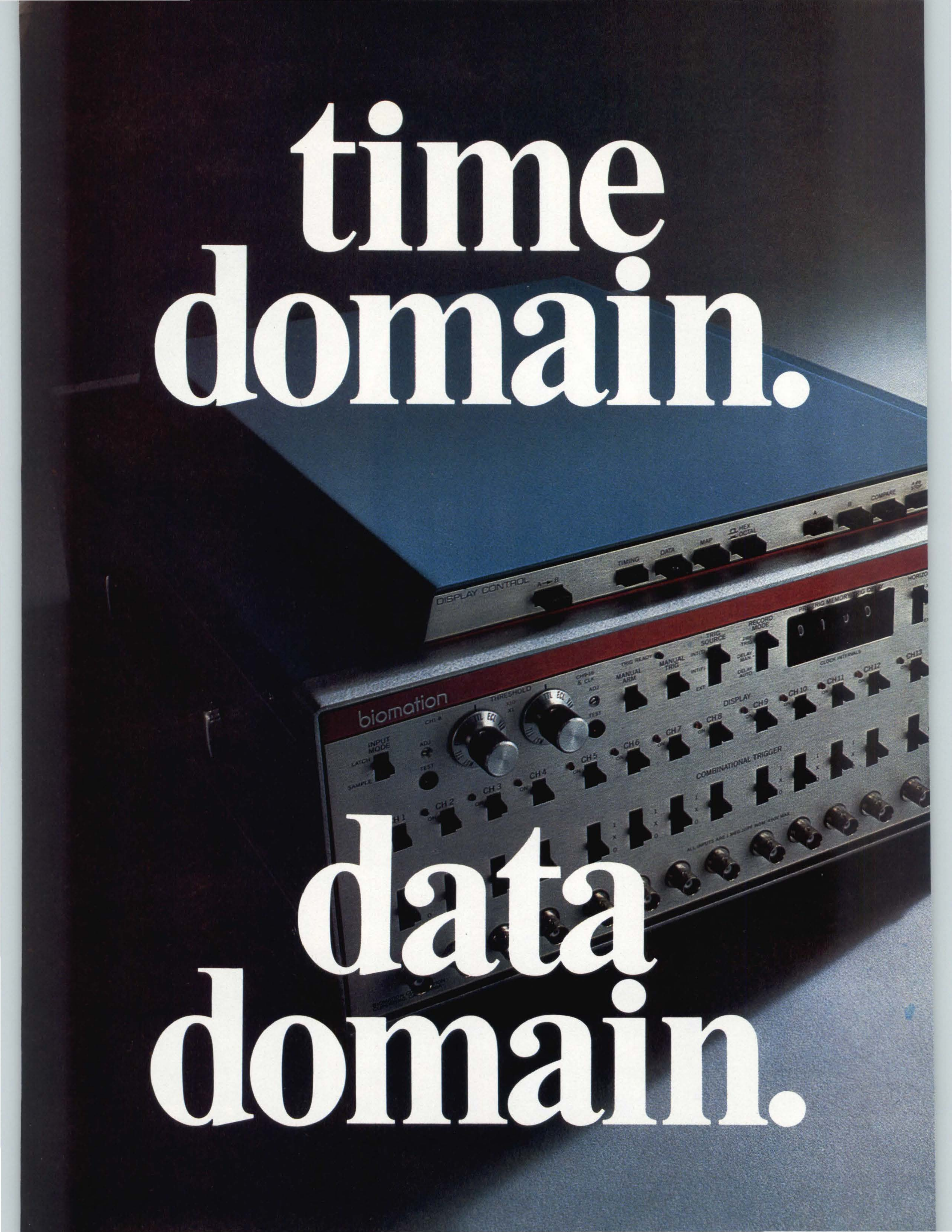
These are just some of the many reasons why the model 40 has the flexibility to fit just about any system. But the model 40's strongest suit is economy. Because on a cost/performance basis, nothing even comes close. And delivery is a lot sooner than expected.

For complete information, please contact our Sales Headquarters at: 5555 Touhy Ave., Skokie, Ill. 60076. Or call Terminal Central at: (312) 982-2000.

TELETYPE

The Teletype model 40 system. Nothing even comes close.

CIRCLE 17 ON INQUIRY CARD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When your job is to interface, integrate and program a complex new digital logic system, you want as much information as you can get.

That's why we're providing a new set of tools which let you display timing information as well as logic word content—in the language of your choice.

Our new 1650-D logic analyzer gives you 16 channels at 50MHz. Our 851-D gives you 8 channels at the same speed.

Accessories can now give you a logic state (1's and 0's) display of any 16 stored words; hex or octal translation; and a vector map of memory contents. The 8 and 16-channel logic analyzers feature:

- Pretrigger and delayed trigger recording
- Trigger point can be easily identified
- Latch record mode for fast pulse capture
- Combinational triggering (true *or* false)
- Movable display cursor that stays with the data when you switch display modes
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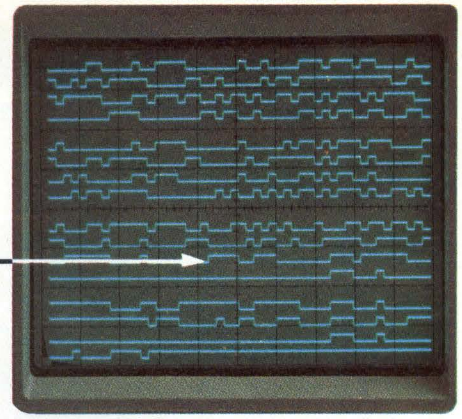
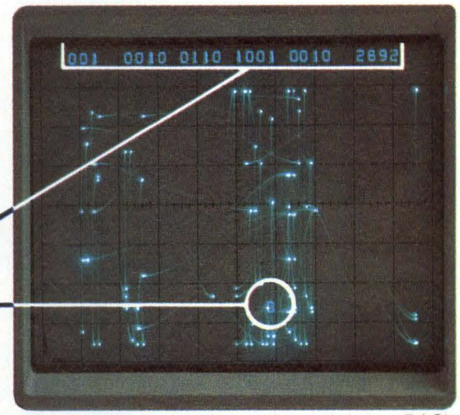
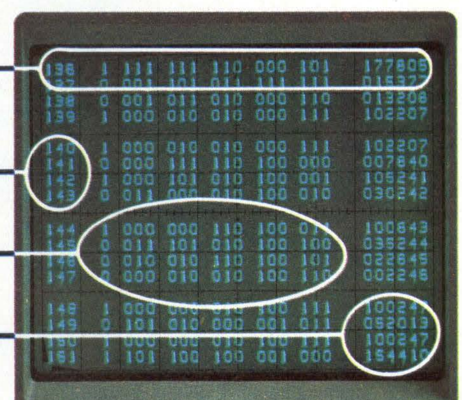
These are complex instruments and we can't give you all significant details here. But please write, call, or use the reader service card. We want to get this useful information into your hands. Biomation, 10411 Bubb Road, Cupertino, CA 95014, (408) 255-9500. TWX: 910-338-0226.



Biomation's new 1650-D produces a repetitive display output reconstructing precisely 500 bits per line for a 16-line timing diagram on a conventional oscilloscope or CRT display. Separate selection of individual channel outputs allows viewing of 1, 2 ... 16 channels at one time with automatic vertical expansion.



Map—each word in memory is transformed via two DAC's to form a unique dot which characterizes that word. All 512 words of the 1650's memory can be accessed for mapping. The cursor word is circled in the map as well as displayed at the top of the screen in alphanumeric form. The cursor may be moved to any of the points in the map for positive identification of that word. In addition, a map of only 16 words may be selected.



Logic state—provides memory address location, binary output of the 16 channels and selectable octal or hexidecimal translation. 16 words are displayed at one time with the cursor address location at the top of the screen. Movement of the cursor control allows accessing any 16 words of the entire 512 words stored in the 1650-D. The display control memory can store 16 words while a different set of 16 is selected from the 1650's main memory (or a new recording is made). These two sets of 16 words can then be overlayed on the CRT. *Any differences will blink* and be easily identified.

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CIRCLE 18 ON INQUIRY CARD

TURNKEY 620 SYSTEMS FROM NEFF USING THE HP 9825 CALCULATOR..

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You're involved in a scientific, engineering, or industrial project that could use a high performance, low cost data acquisition system. But you know that system integration and software costs of most systems actually exceed the hardware. And your need is now, so you want a system that will take data immediately with minimum user training.

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620S is a sophisticated data acquisition system with amplifier-per-channel or differential multiplexer analog signal processing and using the H.P. 9825 computing calculator for system control, data analysis and recording.

Neff systems are known for high performance and the 620S is no exception. Consider 0.1% accuracy with 50kHz channel scanning rate, fullscale input sensitivities from 5 millivolts to 10 volts, up to 256 channels or 2048 channels fully expanded, and 120dB rejection of common mode voltages up to 300 volts. Selectable data filters, simultaneous sample and hold and input signal conditioning are but a few of the many available features.

The Hewlett-Packard 9825 calculator provides the 620S computer performance with the operating convenience of a calculator. Programming is simple with HPL, an easy to learn, high level language designed for scientists and engineers. Standard features include a live-keyboard, alpha numeric printer and cassette recorder. Up to 24K memory is available. Plug-in peripherals include floppy disk, line printer, x-y plotter, and tape punch. It also attaches to H.P. Interface Buss.

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CIRCLE 19 ON INQUIRY CARD

Small Computer Systems Offer Fast Processor To Speed Program Execution

A family of small computer systems, 1000 Systems provide the high performance needed to meet demanding computation, instrumentation, and operations management applications. Priced typically about 9% below presently available equipment, the systems offer a sprint-speed processor, complete data base management software, and networking software. A disc-based real-time executive operating system allows multiprogramming, batch spool monitoring, and multilingual operations; the system supports four or more terminals concurrently.

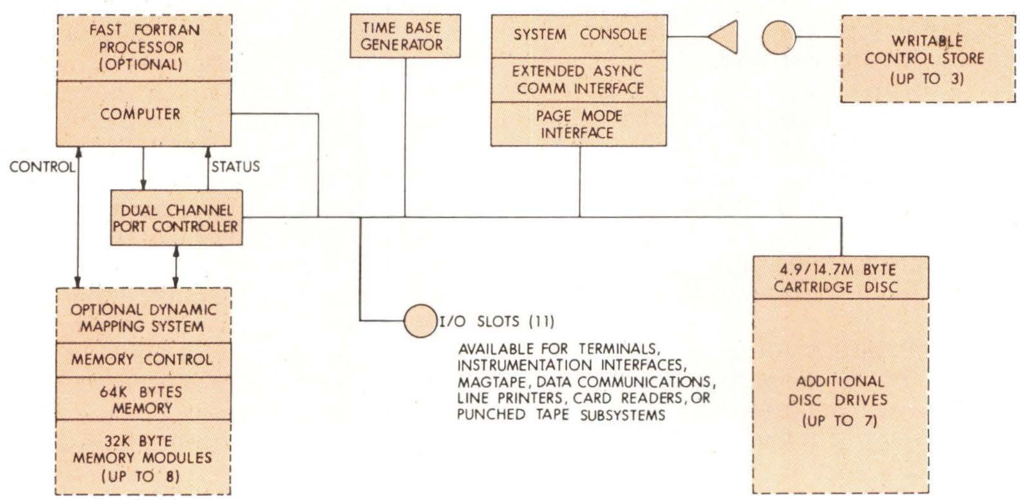
Developed by Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304, the systems are available in desk style or cabinet models, and are programmable in BASIC, FORTRAN, ALGOL, and HP assembly languages. The system processor achieves 60 to 100% faster execution of programs using the concept of dynamic microcycle timing. Instead of allowing time for the slowest operations, the control processor is capable of recognizing the need for and allotting 280 ns to the occasional slower function, while completing most operations within 175 ns. Memory cycle time is reduced to 550 ns.

Three features permit the user to increase the processor's power at will. A control processor address space of 8.5K 24-bit words is provided for the user's microprogrammed subroutines—enough to completely reconfigure the machine. A complete set of microprogramming software is offered to help in utilizing this feature; the set includes microassembler, microeditor, loader, and debug utilities. In addition, the processor enables routines to be transferred from disc or other source directly into control store under software control; this makes the control processor available as a dynamic resource under operating system control.

Standard on large systems (optional on others) IMAGE/1000 data base management software is augmented with QUERY, an English-like inquiry procedure which requires no programming experience. QUERY allows the user to easily obtain information from his data base and to generate reports in whatever form is desired.

Standard system console is the 9600-baud model 2645 CRT terminal, which is equipped with two built-in minicartridge drives. Programmers on multiple terminals can plug-in, modify, and walk away with their programs stored on the convenient cartridges. System software is provided on the cartridges, eliminating inconvenient storage of paper tapes.

Appropriate as the main computation resource in an engineering design facility, the desk-styled model 30 consists of computer with 64K bytes of semiconductor main memory, a 15M-byte cartridge disc subsystem with 25-ms average access time, and RTE II real-time executive operating system software. Up to four termi-



Hewlett-Packard's 1000 Systems are based on a processor that is capable of executing an add instruction in 1.12 μs. Both desk-mounted and cabinet models allow flexible configuration for use in computation, instrumentation, or operations management applications

Universal One

The Microprocessor Development System for the 8080, 2650, and 6800.

It's universal. Millennium's Universal One System interfaces to the most commonly used microprocessors today and others in the near future.

And, it's universally accepted. It's so well accepted that design engineers call it a hardware development aid. It's so powerful, application programmers call it a complete software development system. And project managers? They know it as a great time and money saver and don't worry about what it's called.

Can the project manager be right?

The ability to interface with the different microprocessors of today and the new microprocessors of the future is the key benefit of Universal One. Universal One will never be obsolete and therefore provides the greatest *Return On Investment* of any microprocessor development system available today.

The universality of the system is based on Universal One's innovative multiple CPU architecture. One CPU, the Master CPU, is the controlling element of the system and executes all application *independent* functions; file management, text editing, system utilities, system I/O and software debugging.

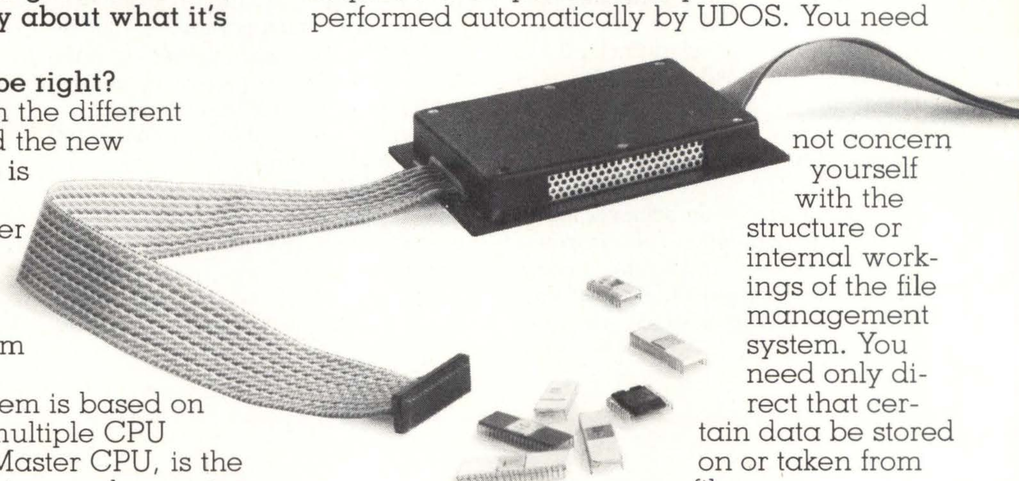
The second CPU, the slave, which is controlled by the master, executes those functions that are application *dependent;* the microprocessor Assembler, in-circuit testing, user application programs, and user I/O. Additional microprocessor slaves are readily added by interfacing the new slave to the system bus and integrating it into the system software.

By meeting all the staff's needs, Universal One cuts costs. It's not necessary to have special test fixtures for design engineers and software development systems for programmers. Universal One saves on personnel training expenses since only one system interface need be learned.

Can the programmer be right?

Universal One's software capabilities rival those found on many powerful minicomputer systems. *U*niversal *D*isk *O*perating *S*ystem (UDOS) was developed specifically for and tailored to the multiple CPU architecture. The operating system is executed by the Master CPU in its own totally protected Master memory to prevent disruptions by application programs.

UDOS is floppy disk file oriented. The system was designed specifically for the characteristics and peculiarities of a floppy disk and as such makes maximum use of it's benefits. Many file management functions, normally required to be performed by the user, are performed automatically by UDOS. You need not concern yourself with the structure or internal workings of the file management system. You need only direct that certain data be stored on or taken from a file.

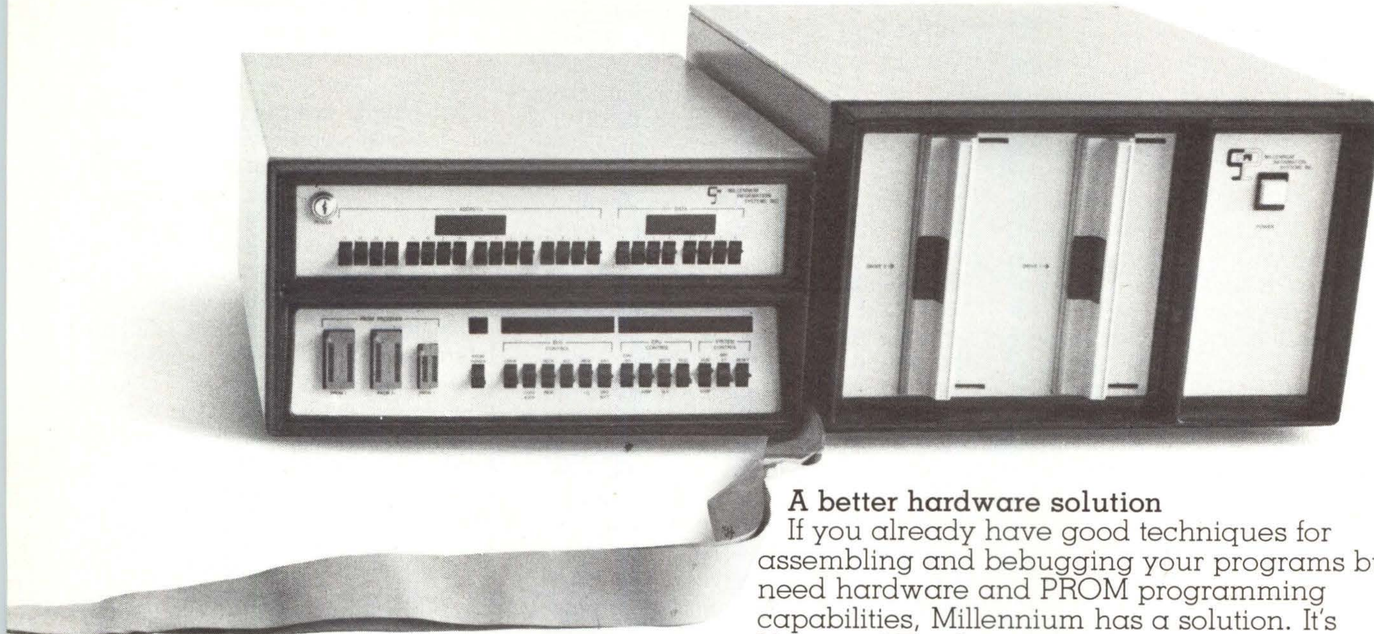


μBASIC™, Millennium's proprietary high level compiler, is a flexible version of BASIC tailored for microprocessor development applications. Unlike interpretive systems the final output of μBASIC is the object code for the microprocessor. μBASIC can also be intermixed with Assembly for memory space reduction and faster program execution.

With Universal One's dynamic trace capability, the activity of a program is traced, instruction by instruction. For break-point analysis two hardware registers provide a break and display of the breakpoint address and contents on memory fetch only, memory write only or on memory read/write access.

Universal One contains a powerful text editor which is file oriented and has macro and iteration capabilities for combining commands.

Millennium provides comprehensive diagnostics which not only test the system's processors, memory & I/O but also check peripheral devices and interrupt logic.



A better hardware solution

If you already have good techniques for assembling and bebugging your programs but need hardware and PROM programming capabilities, Millennium has a solution. It's Universal Emulator, an advanced product that provides all the hardware emulation and PROM programming capabilities of Universal One at a lower price. And, it can be upgraded to the Universal One in the field at any time.

Can the design engineer be right?

Universal One provides two modes of development system emulation for saving time during initial hardware debug and during hardware/software integration. In the first mode, Universal One emulates the prototype's microprocessor and its memory, while I/O functions are controlled by the user hardware. In the second mode, the prototype uses its own memory and I/O. Universal One's two-stage emulation eases the transition from initial test to full prototype implementation.

The front panel PROM sockets accommodate the most commonly used PROMs, the *2708, the 1702A MOS erasable and 82S115 family of bipolar PROMs. Others will be added in the future.

Can they all be right?

Obviously yes! Universal One has the capabilities to get development projects completed on time and within budget. And, Universal One will be just as valuable in the future as it is today. The universal architecture assures the product will never be obsolete.

Universal One's powerful operating system is easy to use so personnel get the most out of it whether they are inexperienced or advanced programmers. μBASIC saves vast amounts of software development and maintenance time.

Last but not least, development system emulation simplifies hardware and software integration. Put it all together, it's the Universal One for 8080s, 2650s, *6800s, application programmers and design engineers.

* Available January, 1977

You can be right, too!

Universal One and Universal Emulator are available for immediate delivery. A complete Universal One System with a single slave and dual flexible disc is $8,900. Additional slaves are $1,250. A single slave Universal Emulator is $4,500. For a prompt direct reply, return the coupon.

I'm tired of doing it the hard way. Show me a better way. My need is ___ Immediate ___ Within the next six months ___ for information only.

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nals can be active concurrently, while the processor executes other programs.

The larger model 80 uses a computer with 128K-byte semiconductor main memory, the same CRT console and disc equipment as the model 30, 200 line/min. line printer, and a 1600-bit/in. tape drive. Suitable for use in operations management, the system uses RTE-III operating system and IMAGE/1000 data base management software with QUERY. With networking software, it can deliver edited, up-to-date reports to other data centers.

Circle 140 on Inquiry Card

Small Diskette Drives Provide Large Diskette Speed/Reliability

Designed to fit into many applications where conventional diskette drives are physically inappropriate, the series 50 family Mini-Diskette Drives (MDD) require the space of a cassette tape unit yet provide electrical and mechanical parameters which allow their incorporation into a larger system or subsystem. Developed by General Systems International, Inc, 1440 Allec St, Anaheim, CA 92805, the drive consists of read/write and control electronics, drive mechanism, read/write head, track positioning mechanism, and the removable diskette.

Three members of the family—MDD 50, 51, and 52—provide capacities for 100K, 200K, and 400K bytes/disc unformatted or 65.5K, 131K, and 232K bytes/disc formatted with transfer rates of 125K, 250K, and 500K bits/s, respectively. Recording is FM on the model 50, MFM on the 51 and 52. The electronic interface is arranged to be a subset of the GSI 110 industry compatible interface. This together with the track/sector configuration allows easy incorporation into developments where large diskette drives have previously been used. Elimination of ac power requirements makes the device insensitive to variations in the U.S., European, and Asian power sources.

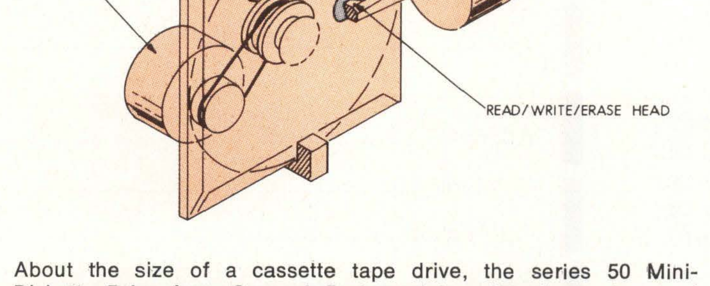
Basic electronics are packaged on one PCB, which contains index/sector detector circuits, head position actuator driver, head load actuator driver, read/write amplifier and transition detector, write protect, and drive select circuits.

A programmable dc drive motor rotates the spindle at 300 or 600 rpm through a belt driven system. The minidiskette is positioned by a registration recess on the face of the spindle. A centering cone that moves in conjunction with the front latch fixes the diskette to the spindle.

Read/write head is positioned with an electrical stepping motor and lead screw. The single element ceramic read/write head has tunnel erase elements to provide erased areas between data tracks preventing normal interchange tolerances between media and drives from degrading the signal/noise ratio, insuring diskette interchangeability. The head is mounted on a carriage on the head position actuator lead screw; the diskette is held perpendicular to the head by a platen, and is loaded against the head with a load pad actuated by the head load solenoid. Contact with the diskette occurs only during data transfer operations, and the head surface is designed to obtain maximum signal transfer with the magnetic surface with minimum wear.

Recording medium is a small flexible disc (Mini-Diskette, specification 100106) permanently housed in an envelope with the apertures necessary for drive spindle, head, and sector hole access. The envelope measures 5¼-in. sq but otherwise is conceptually similar to the IBM diskette.

Circle 141 on Inquiry Card



About the size of a cassette tape drive, the series 50 Mini-Diskette Drive from General Systems International can be used in subsystems developed for conventional diskette units. An electrical stepper motor and lead screw serves to position the read/write head. Head makes contact with the recording surface only during data transfer operations

Disc Storage Subsystem Fills System/370 Storage Needs Economically

The 3650 direct access disc storage subsystem, for attachment to System/370 computers, models 135 through 168, offers full 3350 compatibility plus enhanced software features, improved configuration flexibility, and lower cost/byte for large storage capacity. Developed by Memorex Corp, San Tomas at Central Expressway, Santa Clara, CA 95052, the subsystem uses advanced Data Mark™ 70 and 70F data modules, which incorporate media, read/write heads, and associated circuitry in a removable, self-contained unit, and features optional OS and DOS/VS native mode support.

Instead of the six recording surfaces with 300-track/in. density used by Data Mark units, the 3650 storage module contains 15 recording surfaces with 480 tracks/in. Higher densities make head-to-track align-

Now, Intel delivers memory for PDP-11/04 and PDP-11/34.

Intel is now shipping high speed, low cost memory for two of the hottest new minicomputers, DEC's PDP-11/04 and PDP-11/34.

That means you can get 30-day delivery and 30 to 50% savings by specifying Intel, the largest independent manufacturer of semiconductor memory.

We can give you add-in memory and add-on memory, both totally compatible with PDP-11 hardware and software. Our in-4711 is an add-in memory for the PDP-11 family and slides into an available memory slot, without modifications. For add-on memory capacity, simply attach the in-4011 memory system. You can add memory in 16K x 16 bit increments, up to 128K words.

Built with the proven Intel 2107B 4K RAM, the in-4711 memory is fully transparent to the CPU, with greater processing speed. For maximum throughput you can interleave two memories.

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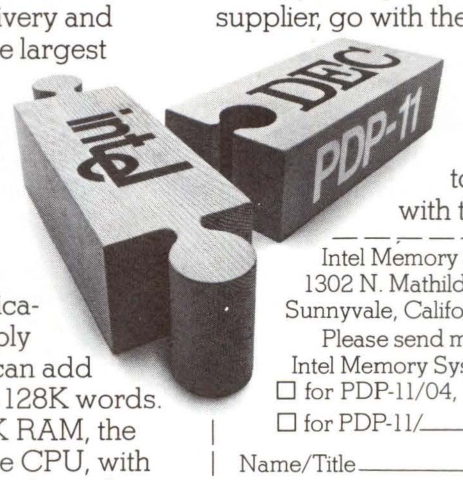
If you've picked DEC to be your computer supplier, go with the best for memory, too. Intel delivers a complete line of add-in and add-on memory for the entire PDP-11 family.



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ment particularly critical, especially where maximum reliability and data integrity are required. To meet these parameters an advanced head-disc assembly (HDA) has been developed.

Significant features standard on 3650 modules include rotational position sensing and write format release. The storage modules are capable of reading and writing in 3650 native mode (317.5M bytes), 3670 compatibility mode (two times 100M bytes), and 3675 compatibility mode (200M bytes) formats. These may be specified on a drive by drive basis. Mode changes are facilitated by the HDA which contains disc, access arm read/write heads, spindle, and voice coil bobbin.

The subsystem consists of 3650 direct access storage module, 3653 storage module and controller, 3654 storage module and alternate controller, and 3674 storage control unit. The 3650 dual-spindle storage module provides storage capacity of 635M bytes, or 317.5M bytes/spindle, with a data transfer rate of 1.198M bytes/s. An optional fixed head allows zero seek time for 1.14M bytes of the total capacity.

A typical system configuration consists of one 3653 storage module and controller and up to three 3650 storage modules, providing a maximum capacity of 2.54G bytes. Substituting the 3654 storage module and alternate controller for one of the 3650s provides maximum availability.

The 3674 storage control unit (SCU) is a microprogrammed controller with read/write monolithic memory; the controller's program is loaded during the power-on sequence from a disc cartridge located internally. The easily interchangeable cartridge allows program updates to be made by merely replacing the disc. From one to four 3653s and from one to twelve 3650 modules can be attached. Thus one SCU can control up to four strings of drives with eight drives/string. Direct attachment of the subsystem to the System/370 CPU's integrated storage control is achieved through the 3653; channel attachment via the 3674 SCU or the IBM 3830-2 SCU.

The unit uses standard OS/VS and DOS/VS (3670 compatibility only) support with no host software changes other than IBM system generation requirements for equivalent 3350 support. Initial customer deliveries are scheduled to begin in second quarter 1977. The 3350 disc drives and head-drive assemblies will be offered only as a package.

Circle 142 on Inquiry Card

Word Processing System Incorporates Video Display, Text Editing Facilities

The WP5000 family of word processing systems are keynoted by operational simplicity. While providing video display, automatic printing, and text editing and revision facilities, N. V. Philips Gloeilampenfabrieken, Eindhoven, The Netherlands organized the system around the operator—it provides instant feedback by indicating on the video screen all operations entered on the keyboard.

To produce typewritten documents, the operator enters text from the keyboard; text is stored in an electronic memory and simultaneously appears on the visual display unit (VDU). The operator modifies text appearing on the VDU if necessary, and at the touch of a key causes the high speed printer to provide finished text. Texts can be recorded on magnetic tape or flexible disc and reproduced on screen or printer.

Three versions of the system all have VDU combined with keyboard, high speed printer, and pedestal unit housing system data storage and processor electronics. "A" version uses magnetic cards for text storage; "B" stores up to 128 pages of text on a single floppy disc; and the "C" version provides two floppy disc units. Printer is a 45-char/s interchangeable "daisy wheel" type which prints at 450 words/min.; a 55-char/s unit is optional. Video display holds up to 61 lines of text (125 char/line).

Circle 150 on Inquiry Card

Redundant Computer Configuration Will Control Space Shuttle

NASA's space shuttle orbiter, being readied for flight, will have an Orbiter Avionics Data Processing System onboard for guidance, navigation, control, and performance monitoring. The system, developed under contract to Rockwell International Corp's Space Div by International Business Machines Corp's Federal Systems Div, 10215 Fernwood Rd, Bethesda, MD 20034, will also collect and analyze data from hundreds of onboard sensors and display information in real-time to the shuttle's flight crew. System components include onboard computers, interface equipment, displays, and mass memories.

Five computers, arranged in a redundant configuration, will allow a mission to continue even if multiple failures are experienced. In this "digital fly-by-wire" configuration, the vehicle is controlled by electrical signals developed by a digital computer and sent to mechanical actuators. The computers are modified versions of the AP-101 model, part of the Advanced System/4 Pi avionics computer series.

Input/output processors act as the interface between the AP-101 and other Orbiter systems. These units perform detail management and buffering of I/O data for the computers. Mass memory units support the computers and displays by providing storage for computer programs and display formats. Multifunction CRT display subsystems provide the interface between the flight crew and the data processing system.

Circle 143 on Inquiry Card

Computer Graphics System Produces Shaded Images in Real Time

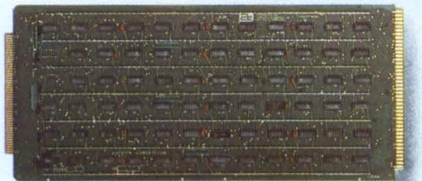
An advanced computer graphics system has demonstrated the capability to produce either vectored or shaded real-time images of dynamic 3-dimensional environments. A graphics extended ALGOL compiler implemented on the system at Case Western Reserve University, Cleveland, OH 44106, allows the user to deal with the system at a high level. Images can easily be produced, turned in any direction and colored, and then recorded on film.

Objects can be described to the computer mathematically, a set of points can be entered from the keyboard, or a data tablet with two special pens can be used to draw designs. Three-dimensional environments are specified using planar polygons as the primitive structure. The system conceives all drawings in basic units of polygons. It turns or cuts polygons to form any shape, creating images having up to 1000 polygon edges in real-time (30 images/s) for animated sequences. Im-

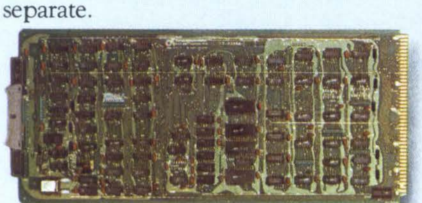
(Continued on p 41)


When you're buying
low-cost computers,
it pays to look
beneath the surface.

The computeriz

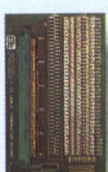


Paper Peripheral Controller. Model 14223-00. Single device controller for paper tape reader, paper tape punch, line printer or card reader. Cabling separate.

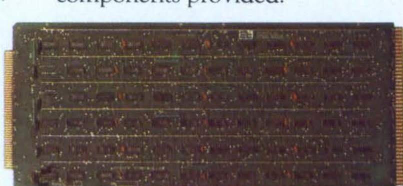


Floppy Disk Controller. Model 14566-01. Provides interfaces for one to four IBM-compatible standard floppy disks, or equivalent. Cabling separate.

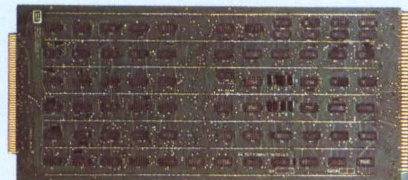
Piggyback Teletype Interface. Model 12635-01. For LSI-3/05 processor. On-board mounting provides bit-serial interface. (For byte-serial interface, use Distributed I/O System with Current-Loop Serial Intelligent Cable.)



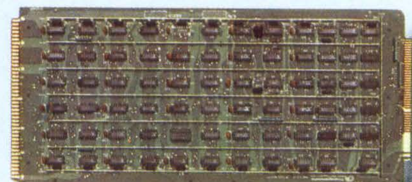
I/O Terminator Module. Model 14511-00. Convenient means for terminating user-designed I/O cables. Plugs onto rear of I/O cards (uses 100 pin connector) with rigid termination. Pads for mounting termination components provided.



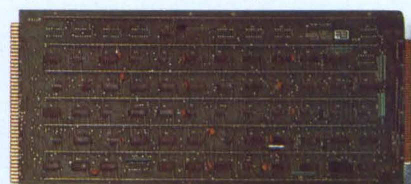
Utility I/O Interface Module. Model 14223-00. General purpose interface with 8 or 12-bit output transfers with 4 control bits in parallel.



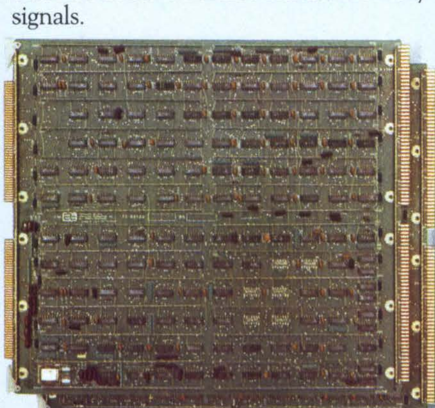
64-bit Input Module. Model 13219-00. Provides 64, 32, 16 or 8-bit inputs with individual strobes.



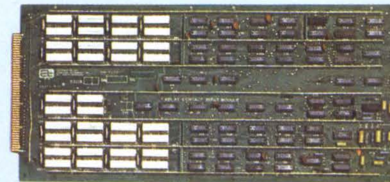
16-bit Digital Input/Output Module. Model 13213-00. Provides input and output registers which may be used as one 16-bit or two 8-bit registers. DTL/TTL compatible.



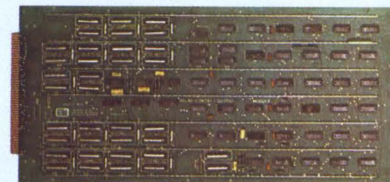
I/O Driver Module. Model 13222-00. Units drive the computer I/O bus up to 25 feet, buffer internal I/O bus from external noise. Does not include memory signals.



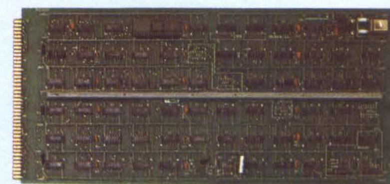
Moving Head Disk Controller. Model 14530-XX. Provides interfaces for one to four standard moving head disk drives, or equivalent. 1500 or 2400 RPM. Cabling separate.



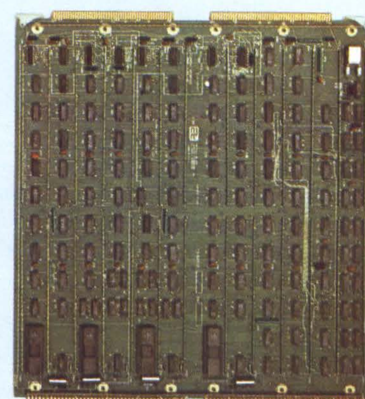
32-bit Relay Input Module. Model 13215-00. Operates as one 32-b two 16-bit, or four 8-bit inputs.



32-bit Relay Output Module. Model 13214-20. Operates as one 32-b two 16-bit, or four 8-bit outputs.

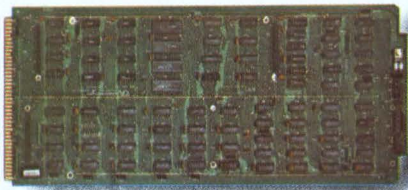


Asynchronous Modem Controlle Model 14535-0X. For one asynchronou line (point-to-point, multipoint, or dire dial). Fully programmable for mode, character size, parity, echoplex, diagno loop-back, special character detect, variable stop bits. Send/receive speed individually selectable with jumpers— to 9600 baud. Available as EIA Interfa with full Data Set Controls or as Curre Loop Interface.

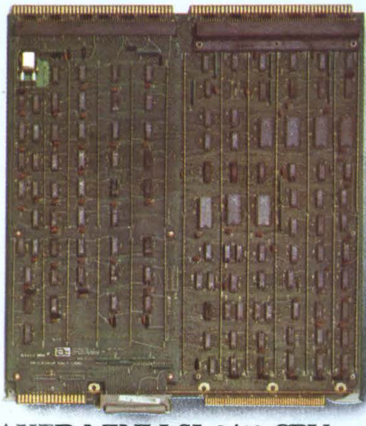


Asynchronous Modem Multiplex Model 14512-XX. As above, but for tw or four independent asynchronous line Multiple vectored interrupts for each li

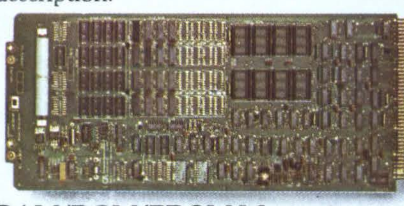
NOTE: Products shown are representative only. For information on products, accessories



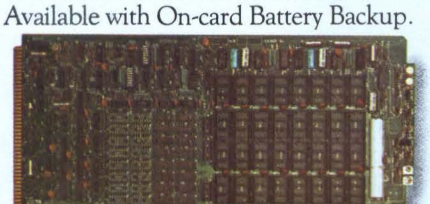
NAKED MILLI LSI-3/05 CPU, Type 0. Model 10300-00. Small low-cost processor offers exceptional power and features. 95 instructions, Power Fail Restart, vectored priority interrupts and 16-bit DMA port.



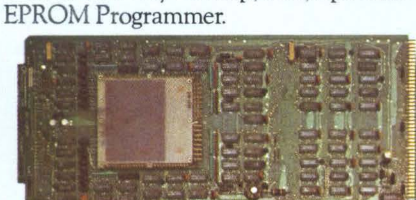
NAKED MINI LSI-2/10 CPU. Model 10600-00. 16-bit minicomputer processor offers twice the speed of LSI-3/05 processors. Includes Power Fail Restart option. See ALPHA LSI-2/10 description.



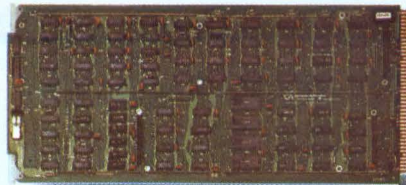
RAM/ROM/PROM Memories. Model 11650-XX. Includes semiconductor RAM in choice of 256, 1K or 2K words; sockets for 8K words of ROM and sockets for 2K words of PROM. Available with On-card Battery Backup.



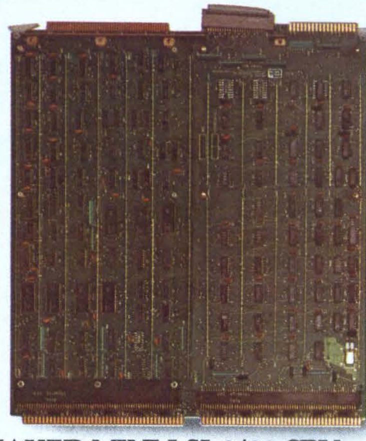
RAM/EPROM Memories. Model 11530-XX. Includes semiconductor RAM in choice of 1K or 2K words and sockets for 4K words of ultra-violet Erasable Programmable ROM. Available with On-card Battery Backup; also, optional EPROM Programmer.



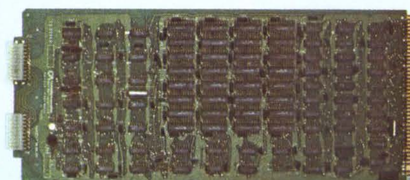
Half-card Core Memory. Model 11671-XX. 4K words. For either NAKED MILLI/ALPHA LSI-3/05 or NAKED MINI/ALPHA LSI-2 Series Computers.



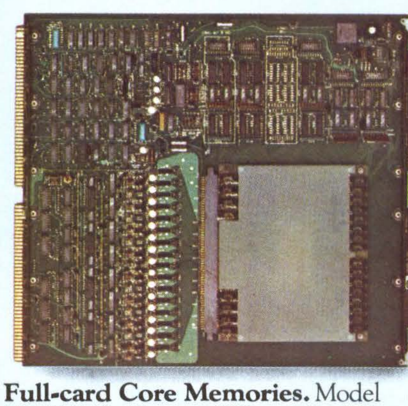
NAKED MILLI LSI-3/05 CPU, Type 1. Model 10300-01. Same as Type 0 at left, but also includes Real-Time Clock and AutoLoad capability.



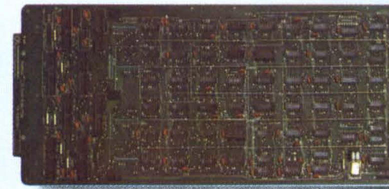
NAKED MINI LSI-2/20 CPU. Model 10400-00. Designed for high-performance applications. Twice the performance of the LSI-2/10 for only a nominal increase in cost. Also includes Power Fail Restart.



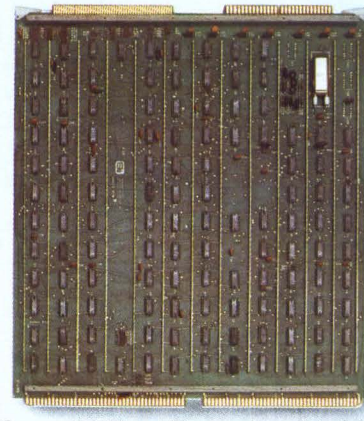
RAM-only Memories. Model 11642-XX. Choice of 4K or 8K words. Available with Battery Pack.



Full-card Core Memories. Model 115X0-XX. Choice of 8K words of Core 980 Memory or 16K words of Core 1200 Memory. For Standard or Jumbo Chassis only.



I/O Distributor. Model 14629-XX. In conjunction with Intelligent Cables (see text), the I/O Distributor provides up to eight interfaces—serial or paralle in any mix. Small version accommodat four interfaces. A DMA version allows data transfer rates up to 250K bytes per second.



Magnetic Tape Controller. Model 14224-00. Provides interfaces for one t four 9-track standard tape units, or equivalent. Cabling separate.

Intelligent Cables. Model 14631-XX. A broad assortment of models offers lo off-the-shelf interface for most standar and special user devices: Line Printer, C Reader, Paper Tape Reader, Paper Tap Punch, Current Loop, CRT, Modem, et General Purpose and Custom Program versions.

16-channel Priority Interrupt Module. Model 13220-00. 16 interrupts with acknowledgement lines.

ComputerAutomation cuts the cost of computerizing.

Knowing what the OEM needs...understanding the OEM predicament. That's what sets ComputerAutomation apart. It's the reason we ship over 100 computers per week—the second highest shipping rate in the industry.

Guaranteed savings.

OEM's buy our computers because they're the most reliable machines made.

Every IC, subassembly, memory subsystem and completed computer is temperature, shock and vibration tested.

That's why ComputerAutomation can offer the only one-year warranty in the industry—when we send a computer out, we know it's not coming back for a long time.

We deliver.

In an industry where one delinquent diode can (and sooner or later will) shut down an entire assembly line, that's saying a lot.

It especially says a lot to OEM's who know they're at the mercy of their sole source computer supplier. One thing you can't do is stick somebody else's machine in that slot.

So here's a thought you might want to stick in the back of your mind for future use:

ComputerAutomation delivers on time.

The reason is that we deliver from inventory—usually a comfortable 30-day cushion of computers sitting around getting more reliable by the minute because they're kept under power and constant test scrutiny.

A lot more trouble for us, but a lot less worry for you. And it does tend to prove our point.

We understand the problem.

From the people who brought you the NAKED MINI.®

The people who brought you the first solution to high-cost computers.

And the most recent solution as well.

And all the solutions in between. Including low-cost memory. And the Distributed I/O System.

Plus on-time delivery. And the only full-year warranty in the business.

The total solution to computerization.

So if you can't spare the time and money to re-invent the wheel, there's a simple solution...from the people who came up with all the other solutions.

Temperature chambers stress computers to isolate marginal components. Computers are continuously tested during 72-hour burn-in at 50°C. Any error starts the test over from the beginning. To further stress the computer, power is cycled on and off approximately 2000 times during test.

Computers awaiting shipment idle away the hours under test. Reliability benefits from the additional component aging.

ComputerAutomation
Naked Mini® Division

ComputerAutomation, Naked Mini Division, 18651 Von Karman, Irvine, California 92713/Eastern Regional Office, 79 North Franklin Turnpike, Ramsey, New Jersey 07446, (201) 825-0990/Midwestern Regional Office, 2621 Greenleaf Avenue, Elk Grove Village, Illinois 60007, (312) 956-6400/ Western Regional Office, 18651 Von Karman, Irvine, California 92713, (714) 833-8830/Europe, CAI Ltd., Hertford House, Denham Way, Maple Cross, Rickmansworth, Hertfordshire, WD3, 2XD, England, Telephone Rickmansworth 71211.

LITHO IN U.S.A.

The computeri

The cost of an OEM computer can be a lot different than the price on the P.O.

In fact, everything considered, the purchase price could be as little as ten percent of the costs incurred over the life of the computer.

To be brutally blunt, it all depends on whose hardware you buy. That's because the cost of computerizing goes way up with most machines.

The cost of hardware integration, for example.

The cost of developing interface electronics.

The cost of developing software.

The cost to maintain the machine once it's out in the field.

Any one of which could seriously impact the profitability of your product. Given that possibility, here's what you need to know to protect those profits.

Engineering Costs.

Prototyping and systems integration is a high-cost area where, traditionally, the OEM has been left to his own devices, so to speak.

ComputerAutomation doesn't work that way. We've accumulated enormous experience in systems integration because we get involved in our customer's projects.

What's more, we've put together a program for sharing that experience with our customers... free, of course. Part of it includes extraordinarily comprehensive documentation provided on an on-going basis. But more importantly, it's a people-to-people program that even provides on-board support personnel when they're needed.

Programming Costs.

No other endeavor consumes time and money quite like programming. For the OEM who's usually racing to release a new product ASAP, even a minor programming effort can be a major setback.

The solution is to concentrate on the applications end of it and not re-invent software that's already on somebody's shelf—ours. ComputerAutomation has an enormous library of powerful software that will cost you next-to-nothing. Everything from humble assemblers to high-powered compilers in BASIC and FORTRAN IV.

The powerful instruction set that comes with our computers will spare you countless hours of programming effort, too, because it's designed with that objective in mind.

Remember, too, that all our computers are buss compatible. Which means you won't have to start programming all over again when you switch to another computer in our LSI Family.

Interface Costs.

Many times an OEM is forced to invent his own interface... usually a very expensive proposition... because the supplier he's

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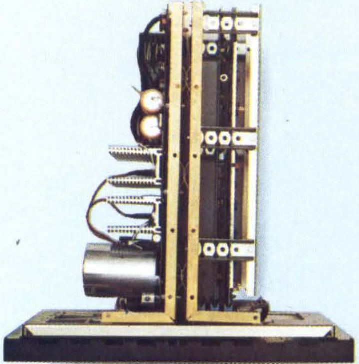
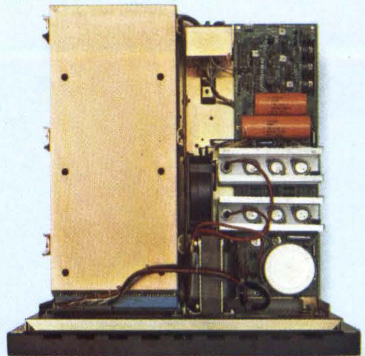
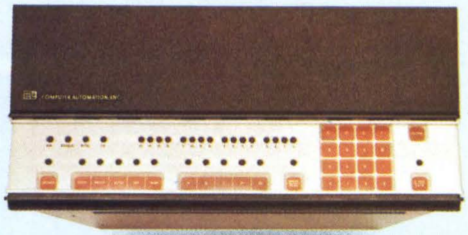




ALPHA LSI-3/05, NAKED MILLI Series. Model 10373-XX. Includes LSI-3/05 CPU (Type 1), with LSI Family compatibility, three half-card chassis, 10-Amp power supply and Operator's Console. This small, low-cost computer offers exceptional power and features, including 95 instructions, Power Fail Restart, vectored priority interrupts, Real-Time Clock, AutoLoad capability and 16-bit DMA port. Full memory options.

ALPHA LSI-3/05 B, NAKED MILLI Series. Model 10375-XX. Includes LSI-3/05 CPU (Type 1) described at left, plus 5 half-card chassis with fan, 15-Amp power supply and Operator's Console. Full memory options.



ALPHA LSI-3/05 C, NAKED MILLI Series. Model 10376-XX. Same as LSI-3/05 B configuration with addition of Programmer's Console.

ALPHA LSI-3/05 D, NAKED MILLI Series. Model 10356-XX. Includes LSI-3/05 CPU (Type 1) as above, standard five full-slot processor chassis, 25-Amp power supply and Operator's Console. Core memory in either 4K, 8K or 16K word sizes.

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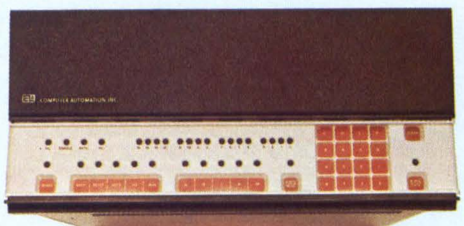

ALPHA LSI-3/05 E, NAKED MILLI Series. Model 10366-XX. Same as LSI-3/05 D configuration with addition of Programmer's Console. Either RAM-only or Core Memory in 4K, 8K, or 16K sizes.

ALPHA LSI-2/10 T, NAKED MINI Series. Model 1074X-XX. A 16-bit minicomputer offering twice the speed of our LSI-3/05 computers. CPU provides 188 major instructions, including multiple stack handling, hardware multiply/divide, memory scan, and extensive byte capability. Five vectored priority interrupts are expandable to 256; two direct memory channels may be increased to 64. Direct Memory Access is standard. Includes Power Fail Restart. Also includes chassis with power supply and Operator's Console. Available in either 5-card or 9-card (Jumbo) versions. 4K or 8K Core 980 Memory or 16K Core 1200 Memory. Memory modules may be added up to 256K words using Memory Bank Control.

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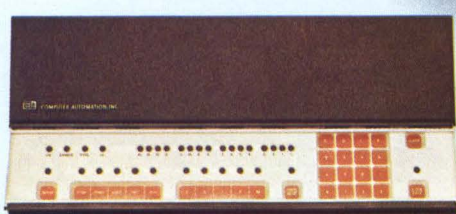
ALPHA LSI-2/20 T, NAKED MINI Series. Model 1055X-XX. Same as LSI-2/10 configuration except with high performance LSI-2/20 CPU offering twice the speed of the LSI-2/10.



ALPHA LSI-2/20 G, NAKED MINI Series. Model 1055X-XX. Same as LSI-2/10 G configuration except with high performance LSI-2/20 CPU, as above.

ALPHA LSI-2/10 G, NAKED MINI Series. Model 1074X-XX. Same as LSI-2/10 T configuration with addition of Programmer's Console.

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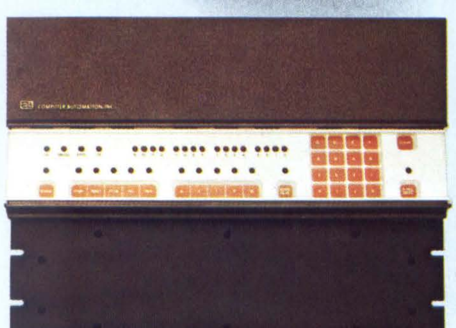

Variables, Teletype or EIA CRT interface, Real-
and AutoLoad ROM Set. Full Memory options.

Software and Documentation Packages. Advanced software and documentation packages, including BASIC, FORTRAN IV, Real-Time Executive and Operating System are available. Plus a complete inventory of diagnostics, editors, assemblers.

zation problem.

picked doesn't offer all the interface he needs.

Or, in some cases, the supplier's interface solution is so expensive it forces the OEM to go his own way.

So, at a time when he needs to concentrate all his energies on his own product development, the OEM finds himself committing substantial resources to a peripheral project. One that can be deceptively time-consuming and costly.

Suddenly the designers are coming in, more test equipment is being designed/built/ordered, ditto for new jigs and test fixturing, the documentation hassle is getting under way, and the dollar and time costs start really piling up.

ComputerAutomation is the only computer company that has solved that problem. You can see it here in the picture. Our exclusive Distributed I/O System. Probably the closest thing to a universal interface you'll ever come across.

The Distributed I/O System only works with our computers, but it works with *all* our computers.

The way it works is this: one half-card I/O Distributor handles the commonalities for up to eight interfaces. (There's a four interface version, too.) The actual interface is accomplished by an Intelligent Cable—so-called because of the microcoded PicoProcessor molded into the cable.

This system offers amazing versatility: any and all kinds of interface can be mixed in any combination—serial, parallel or whatever. And not just standard peripherals, either. The Distributed I/O System accommodates special purpose black box kinds of things, too. There's even a version you can custom microcode yourself.

The cost? Typically under $200 per interface in OEM quantities of 100.

Maintenance Costs.

The cost of keeping a computer in service over the long haul can be enormous. The proof of which is the huge service revenues reported by some computer companies. (Up to $2,000 per year per computer!)

ComputerAutomation's service revenues, by comparison, are minuscule. The reason is that our equipment is so reliable that breakdowns are few and far between. And when there is a malfunction, the fix is almost always a matter of plugging in a spare board and sending the bad board back to us. No tricky fine-tuning to worry about and no high-priced junior technician in there messing around with your customer's equipment.

The Computerization Solution.

The computerization problem obviously goes far beyond computers. So it makes sense that the solution is not only a computer solution, but a systems solution as well.

To find that solution you have to look at the big picture...which we invite you to do by turning the page.

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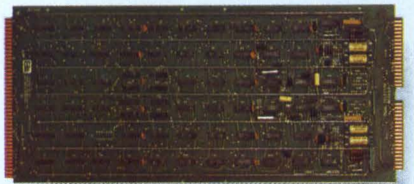
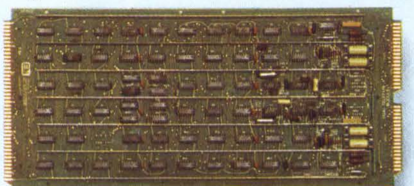
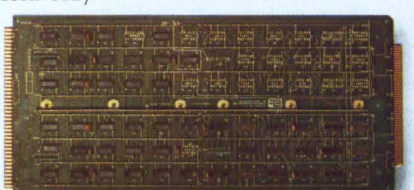


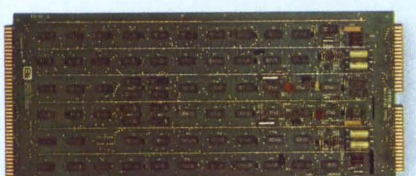
Dual TTY Interface. Model 14236-21. For two modified ASR-33 Teletypes. 20 mA Current loop, 110 baud, two half-duplex channels. Has circuit for programmed motor on/off.



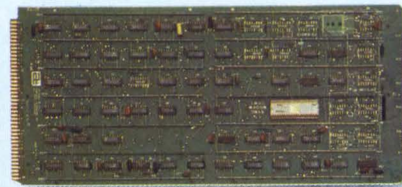
EIA RS232 Interface. Model 14236-5X. For one CRT at baud rates from 110 to 9600. Half-duplex operations only.



Automatic Calling Unit (ACU) Multiplexer. Model 13523-0X. Provides interfaces for one to four Model 801 ACU's, or equivalent. Simultaneous operations, full digit buffering and sense date-line busy. Four vectored interrupts per ACU. Available for either two or four ACU's.

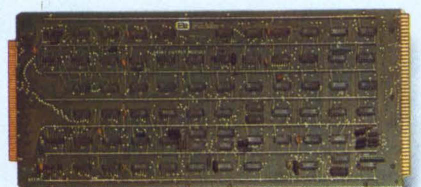


Dual CRT Interface. Model 14236-1X. For two CRT's or leased line modems. EIA RS232 interface with two half-duplex channels, each with one output control line and one input status line. Baud rates from 110 to 9600.



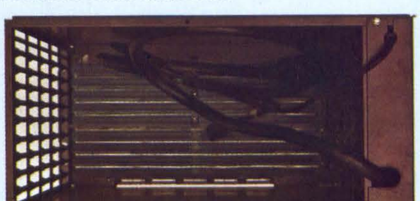
Synchronous Modem Controller. Model 14513-00. Double buffered, half or full-duplex interface for synchronous communications line (point-to-point, multipoint, or direct dial). EIA RS232C/CCITT compatible, programmable synchronous character, and one special character detect. Odd, even or no parity and 5-8 bit frame size program selectable. Transfer to 9600 baud.

Model 14513-01 provides internal clock with strappable options for 1200, 2400, 3600, 4800, 7200 or 9600 baud operation and full Data Set Controls.



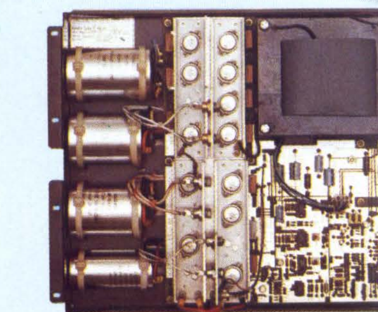
64-bit Output Module. Model 13216-00. Provides output for use as 64-bit word or multiples of 32, 16, or 8-bits with individual strobes.

Processor Chassis. Model 12034-00/20500-01. Full-card chassis. Available in 5-slot and 9-slot versions. Includes motherboard and fans.

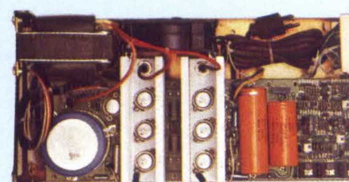


Card Expansion Modules. Model 12098-00/12099-00. Five and nine-slot versions include chassis, blank panel with expansion buffer controller, interconnecting cables and power supply.

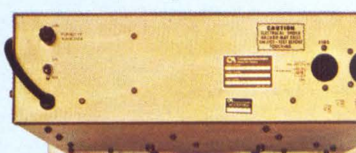
Card Cage, LSI-3/05. Model 12095-0X. Available in either 3-card or 5-card versions. Includes motherboard, card guides, and retaining hardware.



Standard Power Supply. Model 12044-00. Supplies +5V @ 25 Amp
+12V @ 4 Amps and −12V @ 9 Ar



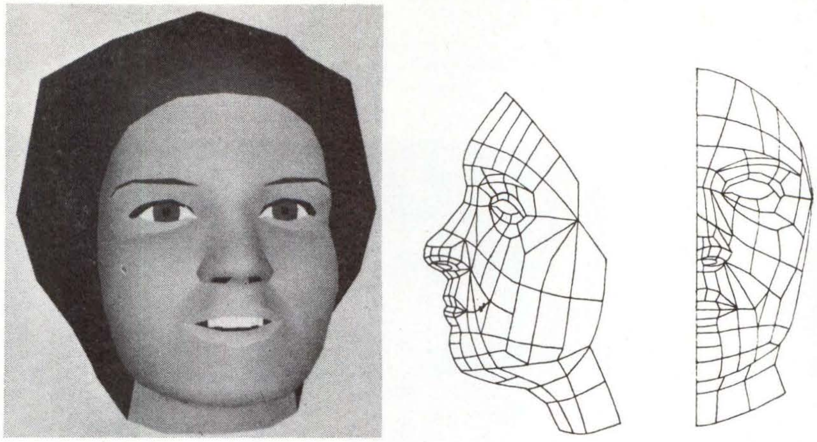
Power supplies for LSI-3/05. Model 12046-0X. Open frame powe
supplies mount in any plane. Supply
+5V @ 10 Amps, +12V @ 0.8 Am
−12V @ 0.8 Amps; +12V @ 1 Am
−12V @ 1.5 Amps. With fan.



Jumbo Power Supply. Model 20441-00. Supplies +5V @ 36 Amp
+12V @ 5.6 Amps, −12V @ 10.7 Ar

MegaByters. Model 109 Series. High-speed 16-bit systems for real-time, communications and business applications. Features include LSI Family compatibility; four standard input-output modes, including Direct Memory Access; vectored priority interrupts; and a comprehensive set of 224 instructions. Includes Jumbo Chassis, Jumbo Power Supply, Programmer's Console, Power Fail Restart, Basic
Time Clock, AutoLoad

test equipment or options not covered, please contact the factory or your regional sales representative.



Shaded real-time images of dynamic 3-dimensional environments can be produced using Case-Western's computer graphics system. Conceiving of all drawings in basic units of polygons (see diagram), the system creates shaded images such as that shown in the photo. Animated sequences of images having up to 1000 polygon edges can be produced in real-time; more complex images with up to 4000 polygon edges are produced at slower rates

ages having up to 4000 polygon edges can be produced at slower rates. Colored filters are used to record the finished product on 35-mm film or as 4 x 5" stills.

Most of the graphics work is produced on hardware designed by Evans & Sutherland, Salt Lake City, Utah. A PDP-11/40 is the controlling processor, handling I/O for itself and the channel control processor. The two processors share a common memory, communicating via memory and the Unibus™. Channel control processor and associated graphics hardware appear as a peripheral to the -11/40.

A high speed 4 x 4 array multiplier, the matrix multiplier performs rotations, translations, scaling, and perspective transformations. Accepting input from the channel controller, the unit feeds information to the shaded graphics pipeline, vector graphics pipeline, or back to the channel controller.

The shaded graphics pipeline consists of polygon clipping/divider, Y-sort memory, visible surface processor, and shaded-raster generator. Within these components data are manipulated with hardware-implemented algorithms to produce the shaded raster-scanned images that are similar to TV images. The vector graphics pipeline contains hardware which interprets data and commands from the matrix multiplier and channel controller to produce dynamic vector images, eliminating vectors outside the field of view, performing perspective division, and producing X-Y deflection signals to draw the specified vector. Output from either pipeline goes to two black/white display monitors and/or to a film recording unit.

User interaction with the system is provided through a user terminal—consisting of keyboard and alphanumeric display and a large dual-pen data tablet. Storage for system software, user programs, and data files is provided by a 10M byte disc. A communications link allows the graphics system to communicate with a PDP-11/45 and with a text editing file storage system, which provide services such as magnetic tape drives and mass storage, not available on the graphics system.

Some of the projects attempted on the system include a motion picture illustrating stresses on a supersonic aircraft in flight, illustration of fluid flows, visualization of automobile traffic patterns, and illustration of the molecular bonding of chemicals.

Circle 144 on Inquiry Card

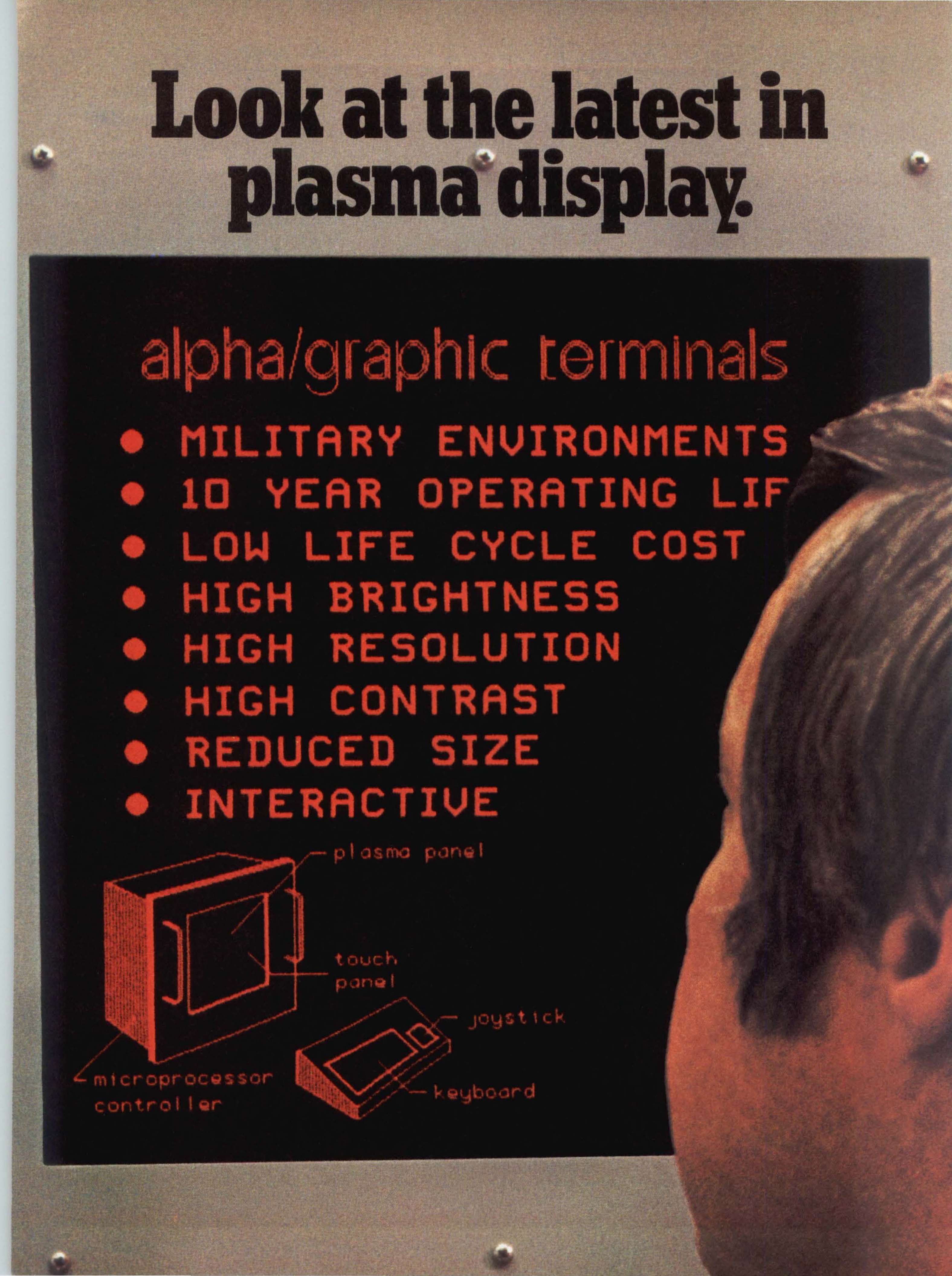
Semiconductor Laser Solves Problems of Videodisc Pickup Systems

High operating costs and difficult adjustment and maintenance associated with conventional optical videodisc pickup systems have been overcome using a semiconductor laser pickup. Developed by Hitachi Ltd, Central Research Laboratory, Tokyo, Japan, the pickup is directly compatible with conventional HeNe systems but easier to adjust and maintain, requires a smaller power supply, and is one-twentieth the size and volume.

Developed for Philips type videodiscs, the pickup uses a buried heterostructure injection laser for the light source. In the optical system a laser beam is focused as a microspot on the videodisc, and the reflected beam is detected by a photosensor. Conventional systems employ a large HeNe (helium neon) laser as the light source and a complex composition of mirrors and lenses for reproduction, resulting in high operating costs and difficult adjustment and maintenance. By using a semiconductor laser as light source and by bringing into one axis the laser beams for detection of video and servo signals, the optical system has been significantly simplified. Testing conducted with the laser pickup functioning at an output power of 0.5 mW has resulted in images with 40 dB signal/noise ratio—equivalent to the level used for ordinary color TV.

The ultra-small-size semiconductor laser which serves as light source has a 1 micron (1/1000 mm^2) radiant surface. Active region is made of filamentary GaAs buried completely in GaAlAs, a substance which causes no optical loss in the lasing. This buried heterostructure, achieved by using a successive liquid-phase-epitaxial growth technique, provides added advantages of reduced operating current and device size. Threshold current of this laser at room temperature is a minimum of 17 mA in dc and 15 mA in pulsed operation, or about an order of magnitude lower than those of conventional devices. The filamentary active region allows superior thermal characteristics to be obtained and allows continuous operation at room temperature even with heat dissipation through the GaAs substrate. Low operating current makes a large heat sink unnecessary and permits the device to have a volume of less than 1 cm^3.

Used in the optical pickup, the laser has an inherently small radiant surface, and gives steady spot



Look at the latest in plasma display.
alpha/graphic terminals
• MILITARY ENVIRONMENTS
• 10 YEAR OPERATING LIF
• LOW LIFE CYCLE COST
• HIGH BRIGHTNESS
• HIGH RESOLUTION
• HIGH CONTRAST
• REDUCED SIZE
• INTERACTIVE
plasma panel
touch panel
joystick
microprocessor controller
keyboard

Developed by Hitachi, the optical pickup system for Philips type videodisc systems uses a semiconductor laser to greatly reduce both size and operating costs. One-twentieth the size of a conventional pickup, the unit's optical system has been simplified by bringing into one axis the laser beams for detection of video and servo signals, thus reducing the difficulty of adjustment and maintenance

radiation at an operating current of approximately 10 mA. The diameter of the microspot has been reduced to less than 2 microns, necessary for reproduction on the videodisc and to secure output power of more than 0.5 mW.

Rather than a separate laser beam system necessary for conventional detection of the autofocusing, tracking, and image signals, the pickup detects all signals with a single beam. Using a single beam simplifies composition, improves light utilization efficiency, and allows easy adjustment. Quality of the reproduced signal is also improved because mutual interference between autofocusing and tracking signals is compensated for electrically.

Circle 145 on Inquiry Card

Commercial Computer Doubles Memory Capacity, Uses High Density Modules

Distributed processing, commercially oriented minicomputers, and data base capability on minicomputers have been identified as existing needs by commercial computer users. The Eclipse C/330 computer and IDEA software, introduced by Data General Corp, Southboro, MA 01772, respond to these needs and provide easier implementation and use of minicomputer systems by data processing managers who must distribute processing capability to both decentralized and relatively unsophisticated users.

The C/330 incorporates 64K-byte semiconductor and 32K-byte core single board memory modules, and uses a memory allocation and protection (MAP) unit to attain main memory capacity of 512K bytes with hardware protection of user programs in dual programming applications. Dense memory results in fewer connections and interfaces, increasing system reliability; while the MAP's large memory capacity offers advantages to multiterminal interactive data entry/access (IDEA) system users.

Microprogrammed architecture of the C/330 processor includes a comprehensive instruction set tailored for data handling. Capabilities include word, byte, and bit addressing, character string move and compare, and code translation. A special edit command provides the ability to convert from packed or unpacked decimal to ASCII and to perform formatting functions such as leading zero suppression and punctuation control. Both 16- and 32-bit instructions are provided. The instruction set optimizes operating system and high level language performance by replacing software routines with a single instruction.

Operating system interrupt servicing is performed in high speed hardware, providing the fast response important to multiterminal or communications environments. A single instruction identifies the interrupt source, saves the machine state, switches from user to system stack, and alters the priority structure. Packed and unpacked decimal numeric data are handled by the extended arithmetic processor which operates in parallel with the CPU, and performs single and double precision floating arithmetic.

Core and semiconductor memory modules may be mixed in the computer, and modules may be interleaved up to eight ways to reduce effective cycle time. Both 32K-byte core and 64K-byte semiconductor modules are available as single boards for high density. Speed of the 64K n-MOS has been increased to 500 ns for read cycles, compared to the 700-ns read cycle time for previous 16K modules; write cycle is 700 ns. Memory error checking and correction is standard, detecting and correcting all single-bit main memory errors and detecting most multiple bit errors. The 32K core modules have an 800-ns full cycle time, achieved using a split sense memory technique to reduce the traditional 1-μs speed.

IDEA software (which includes an easy to use English-like language) consists of a screen-format generator for freeform format design, a compiler for specifying field processing, and an online multiterminal monitor that controls up to 16 terminals. A user-transparent interface provides access to the INFOS data management system, giving users multilevel keyed access to data base files for record retrieval, display, and updating.

Circle 146 on Inquiry Card

Extended BASIC Language Allows Software Control of Real-Time Processes

Controller BASIC, an extended version of standard BASIC that was developed for controlling real-time processes, provides transfer of data, commands, and status information to and from I/O devices not commonly associated with the BASIC language. A WHEN statement allows the user to develop programmed routines that accept and service randomly-timed interrupts.

The language provides a full range of arithmetic and trigonometric functions, multidimensional arrays, matrices, string, and relational operations. Extended features include the WHEN statement, which enables the user to synchronize an external event to his program. When this event occurs, the program branches to a specified statement number where sequential execution resumes.

Extended I/O statements allow the user to specify a unit number or mnemonic to identify a logical I/O device. The CALL statement allows users to call and pass parameters to assembly language subroutines. Users can set and read the date and time of day through the TIME statement.

Controller BASIC requires 8K of memory and is executed under the company's Real-Time Executive. Software and documentation are available from Computer Automation, 18651 Von Karman, Irvine, CA 92713 for a one-time charge of $400.

Circle 147 on Inquiry Card

Compare the new Sanders Graphic 7 with other interactive terminals.

You'll draw a graphic conclusion.

Sanders' new Graphic 7 is an intelligent terminal with all necessary hardware and software as standard —not cost-you-extra—features.

But the Graphic 7 doesn't just save you money when you buy it. It also saves you money after you buy it.

Simply wheel your Graphic 7 through the door and plug it in. No installation problems.

Your programmer won't have to spend much time with your Graphic 7. It comes pre-programmed.

And your operators will be able to handle your Graphic 7 after a 10-minute briefing, because it works with a one-button initialize.

Application programs? Our Fortran-based graphic support package can reside in any host that supports Fortran.

And with the intelligence at the terminal, there's minimum impact on the host. You can do more work faster.

Sanders experience? Our graphic terminal systems are used in computerized production projects. Tire-tread design. Avionics defense systems. Flight training. Land-use management. Air traffic control. And dozens of other areas.

Compatible, fully equipped, low priced. What other graphic conclusion can you draw than the new Sanders Graphic 7? Send for specs and specific applications. Sanders Associates, Graphic Systems Marketing, South Nashua, NH 03060. 603-885-5280.

SA ®
SANDERS ASSOCIATES, INC.

CIRCLE 24 ON INQUIRY CARD

100-kVA UPS Protects Computer and Itself With Individual Module Control

An uninterruptible power system that is capable of protecting itself, as well as the computer it powers, the UPS is designed for applications of 100 kVA and up. Features include individual module control with multimodule communication, automatic "start" and "stop" operation, solid-state metering and annunciation, increased brownout protection, extended battery life, and flexible system configuration.

Power modules in the unit, manufactured by General Electric Co's General Purpose Control Dept, PO Box 2913, Bloomington, IL 61701, consist of rectifier, battery, and static inverter. During normal operation, incoming ac power is converted to dc, which powers the inverter. The battery is "floated" on the dc bus to provide dc power to the inverter in the event that incoming ac power from the utility is lost. The inverter section reconverts dc power to smooth ac power to support the critical computer load.

Each system contains sufficient power modules to serve the critical load. A redundant system contains one power module more than the base load requires. A solid-state bypass transfer automatically switches the computer to an available alternate power source to prevent power interruption in the event the UPS has a system failure.

Multimodule systems are designed with intermodule datalink communication to assure coordinated individual control operation. Control communication between modules is accomplished by two independent datalinks. An internal monitor and output detector are separate and distinct from each other. Each is redundant of the other, eliminating any possible common mode control failures, and providing sustained power output even if one datalink is lost.

Operator controls on the system consist merely of "start" and "stop." Operational control with self-protection for each module is completely automatic with the Logicenter. A self-diagnosing, completely solid-state annunciator in each module produces a time-stamped hard copy printout of status and sequential events in the automatic system operation. Indications are provided for more than 220 monitored items and solid-state instrumentation; a digital display is provided for the instrumentation. Each power module has built-in "early warning" detectors. Triggered by a module malfunction, the system prevents disturbance to the critical computer load while minimizing damage within the module. Detectors are simultaneously linked to the sequential, self-diagnosing annunciator.

A duplicate module control panel including the printer and display can be remotely located, permitting complete control from a remote station.

Circle 148 on Inquiry Card

Plug-In Display Formatter Extends Logic Analyzer's Capabilities

The DF1 display formatter is a 7000-series plug-in module dedicated to use with the 7D01 logic analyzer. The combination provides displays in timing diagram, binary, octal, and hexadecimal state table, and mapping formats to save troubleshooting time in debugging either hardware or software. Tektronix, Inc, PO Box 500, Beaverton, OR 97077 designed in the hexadecimal format and exclusive-OR capabilities to make the unit an effective tool for analysis of microprocessor software.

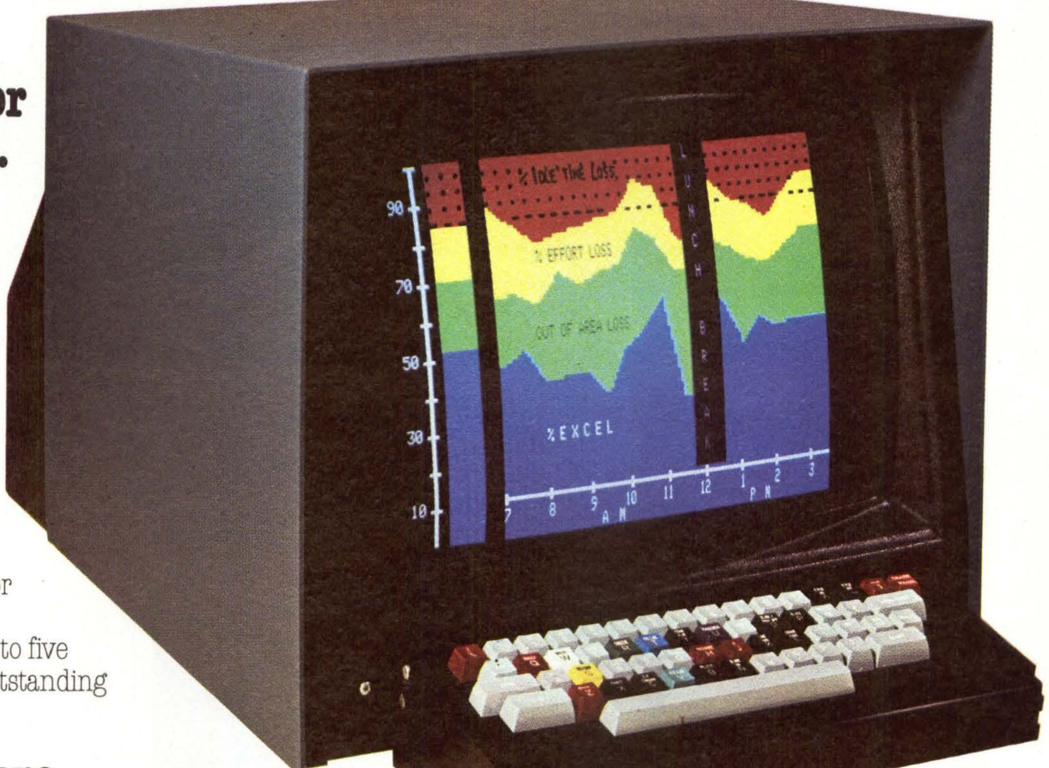
In timing diagram mode, the 7D01 provides its standard display, while the DF1 generates a CRT readout in binary, octal, or hexadecimal of individual words as selected by the analyzer's cursor control.

Mapping displays can be generated from binary, octal, or hex configurations. The location of a digital word representing a word identification marker, advanced in manual or slow mode of operation, is spelled out in binary, octal, or decimal format each time the position of the marker and that of a mapped point coincide. In either slow or fast automatic operation the relative length of time spent at any word location indicates the number of times that the word appears in the analyzer's memory, while the sequence of positions reveals the sequence of individual words.

(Continued on p 48)

The Intecolor® 8001

It's an 8-Color Intelligent CRT for $1995.*
Or a Micro Computer for an additional $1495.
The choice is yours.



A $1995 8-Color CRT. Complete.

When we say complete, we mean complete. The **Intecolor** 8001 has 8080 CPU, 4K RAM Refresh, Selectable Baud Rate to 9600, Keyboard, RS232 I/O, and ASCII Character Set. All in one package. It's a complete stand-alone system which features our unique **Intecolor** 8001 NINE SECTOR CONVERGENCE SYSTEM for minimum set-up time and exceptional stability. Three to five minutes is all it takes for outstanding color registration.

The $1495 Micro Computer Package.

You just give us the word and we'll convert the **Intecolor** 8001 into a stand-alone micro computer with BASIC, Roll, Insert/Delete, Additional 8K RAM Work Space, Graphics Mode with 160X192 Elements, Background Color, Lower Case ASCII, 48 Line X 80 Characters/Line, and 2X Character Height. Plus additional features which make your **Intecolor** personal computer the best buy in the industry.

Which System Is Right For You?

The **Intecolor** 8001 CRT is a smart, inexpensive way to upgrade the CRT's in your present system from black and white to color. And color has definite sales advantages. Like more efficient man-machine interaction and significant error reductions in data entry and recognition. The **Intecolor** 8001 CRT can also be used or marketed as a complete stand-alone micro computer system with computation or control capabilities. It might even replace your whole system!

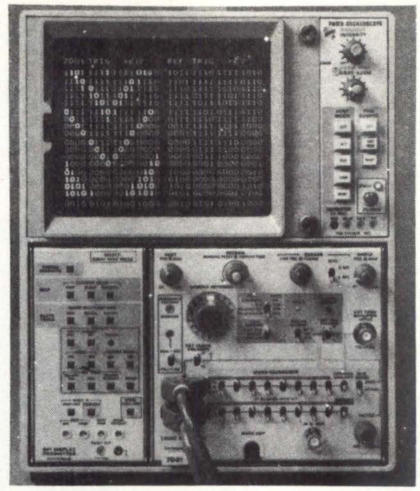
Whatever your needs, market or application — Process Control, Medical, Credit Checking, Order Entry, Financial Analysis, Research and Development, or for your own personal computer — you won't find a more usable terminal, color or black and white.

Write Or Call For More Information

We know you're going to have some more questions, and we've got the answers. We think we've come up with a CRT and computer package that's hard to beat. And one thing for sure. The **Intecolor** 8001 is by far your best buy today in a color CRT micro computer or intelligent terminal. Make us prove it to you with a demonstration by one of our authorized representatives. Or call us direct and talk to an applications engineer.

Intelligent Systems Corp.®
5965 Peachtree Corners East
Norcross, Georgia 30071
Telephone (404) 449-5961

*Quantity 100 Price.
Unit Price $2,495. Domestic USA Prices



A plug-in module for Tektronix' 7D01 logic analyzer, the DF1 display formatter provides mapping displays in binary, octal, or hexadecimal configurations. Side-by-side comparison of stored reference data against new data in exclusive-OR mode provides an intensified display of new data that differ from those in the reference table

In state table mode, standard display consists of a table of 16 lines of 16-bit words, in binary, octal, or hexadecimal. The interval between the cursor-selected word and the triggering word is displayed in alphanumeric characters at the top of the CRT screen. When the trigger word appears in the table it flashes intermittently for quick identification. Display is advanced line for line with fine cursor control, table by table with the coarse control.

Side by side comparisons of reference vs "new" data can be made. Data from the circuit under test are displayed on the left half of the screen (7D01 display); data transferred to the DF1 from an earlier 7D01 display are shown on the right hand side (reference display). An exclusive-OR mode intensifies data on the 7D01 display which differ from that of the reference table to permit easy identification. Comparisons can be made table by table or column by column. Reference data in DF1 memory can be compared line by line or table by table with new data; the new data window can be advanced to provide comparison of two data sets offset by a specific number of words, or new memory can be searched for each occurrence of a key word in reference memory.

Circle 149 on Inquiry Card

← CIRCLE 26 ON INQUIRY CARD

From those wonderful folks who brought you the best high-priced testers.

The best low-priced tester.

Introducing the GR 1795 logic circuit tester. The first tester to give you the full diagnostic capability of our GR 1792 series of testers. For about one-third the cost.

This means that for the price of a pretty ordinary tester, you can now get one that will run our powerful CAPS Computer-Aided Programming Software.

So you get all the trouble-shooting speed and accuracy of our big systems.

You get our latest look-ahead probe with pulse-catching capability and automatic programming for different logic families.

And you get a diagnostic clip, fast floppy disc storage, and the same device adapter we use on our big machines.

So what don't you get with the 1795?

Simple. You don't get CAPS simulation and programming capability.

For set-up, you have to program on either an existing 1792 or a separate GR 1797 Programming Station, or use our Programming Service.

Or, you can buy our alternate model GR 1795-LTM.

Instead of CAPS, the LTM uses our new Learner/Tester Mode for set-up and trouble-shooting. It's far more accurate than other schematic/operator-guided probing techniques since it stores full data per node instead of making transition counts. And, it allows you to move up to full CAPS diagnostics at any time.

Now that this kind of performance is available in a low-cost system, big-time testing capability can come to a lot of places it's never been before. Like service depots, to reduce board float. Or small companies on small budgets. Or large companies with multi-station applications.

The new GR 1795 and GR 1795-LTM.

The first low-cost testers that are as good as a GR tester.

GenRad, Inc., Test Systems Division, 300 Baker Avenue, Concord, Mass. 01742, 617-369-8770.

GenRad

The difference in software is the difference in testers.

CIRCLE 27 ON INQUIRY CARD

Television Network Automated by Minicomputer-Controlled Channels

Viewers of televised musical spectaculars or dramatic extravaganzas regularly are awed by the extensive and complicated audio and video effects that often make the human talent on display seem of secondary importance. Yet these viewers rarely consider the even more awesome problems of getting those programs on the air—coordinating video and audio, inserting commercials, cuing special events, starting and stopping one program, and starting the next—without either blanks or overlaps.

The editors for a program may have days or weeks to cut and merge tapes before finalizing the program; the engineers putting that program over the network are working in real time. They can't back up and start over if they make a mistake.

Of course, the viewers—as the customers for the network's programs—should not be expected to consider those problems. They have every right to anticipate a perfect sequence of programming—and certainly the sponsors of the programs demand a smooth and uneventful continuance that will not detract from the impact of their commercials upon the viewers.

Commonly, the hub of all activity related to airing television programs is a television center or central.[1,2] At NBC's New York City plant, for instance, the TV central coordinates several relatively independent areas such as production studios, telecine equipment, video tape machines, and audio/video master controls and circuits to assure proper release of audio and video signals to both the local NBC station (WNBC-TV) and the NBC television network.

Chief element of this coordination is "switching central," which in turn depends on a master grid or audio/video routing switcher. Provisions are included for 10 simultaneous output channels, six of which have so far been implemented. Each of these six channels is controlled by a 16-bit General Automation, Inc SPC 16/45 minicomputer with 32K words of core memory, supplemented by 2.5M words of disc memory. In addition, two "keyboard" computers, substantially identical to the online "channel" computers, are included for addressing the channel computers to load or retrieve data. System design was conceived and executed by NBC Engineering. Portions of the system were then subcontracted for manufacture according to "black box" specifications. The routing switcher, for example, was built by General Dynamics, San Diego, Calif. Software was developed and executed by a 5-man team of programmers attached to RCA Laboratories, Princeton, NJ.

Most daily programming requirements are handled by one channel for the local station and one for the network. The remaining four active channels serve for special network services, to backup the local or network channels, to automatically preview programs for clients, or as automated pre-assembly facilities.

Master Grid

In its current organization, the master grid—an audio/video routing switcher—can switch 100 video inputs and 300 associated audio inputs into 320 possible users.[3] Four different audio sources can complement each video source (although only three have so far been implemented).

Within the structure of each of the six channels, the respective minicomputer requires supporting equipment in order to perform its job. Since all station/network events are based on time, very precise time information must be input to the CPU. As shown in Fig. 1, in order to initiate computer procedures a time code is fed into a time code reader by a plant precision time generator. This code, originally intended

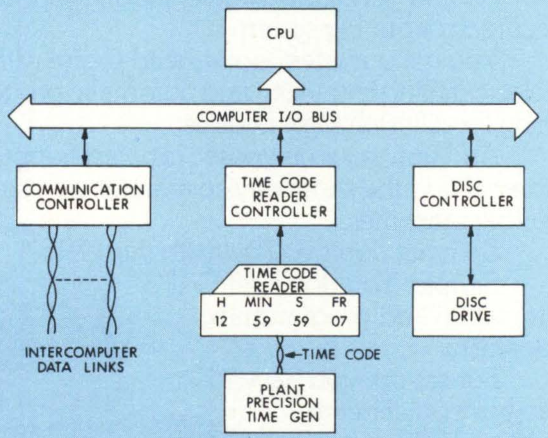


Fig. 1 Primary software interface.[3] A time code, which serves as precision time standard throughout broadcast plant, is fed to channel computer as parallel BCD input. Frame timing is approximately 30/s. Disc contains two full days of program instructions for channel

(Continued on p 59)

INNOVATIONS FROM

Advertisement

HEWLETT-PACKARD

COMPUTER ADVANCES

The introduction of the affordable computer power center, the Hewlett-Packard 1000 Computer System is one of those fortunate occasions where a number of computer advances arrive concurrently and are able to be utilized within a single new computer system. Significant contributions within the HP 1000 computer system include a fast new processor, and a fast and flexible new CRT terminal as the convenient machine/human interface to HP's new IMAGE/1000 data base management software. Plus, the system's contemporary and attractive desk styling is a welcome addition to office environments.

Beyond these new capabilities, the HP 1000 builds on previous contributions such as HP's complete computer network software, the Hewlett-Packard Interface Bus for control of automated instrument systems, HP's efficient and proven Real Time operating systems, and the fastest cartridge disc memory on the market.

The effect is an exceptionally fast and powerful small computer system that both OEM's and end users with computer experience can easily use as a tool to implement a wide range of applications. The HP 1000 is well suited to computation, instrumentation, and operations management applications that demand high performance. Because its increased performance is priced five to ten per cent below previous HP small computer systems, the HP 1000 sets a new price/performance standard in its class.

FROM PRODUCT DESIGN TO CUSTOMER DELIVERY THE HP 1000 IS YOUR PARTNER IN PRODUCTIVITY

"RIGHT NOW" ANSWERS TO "RIGHT NOW" QUESTIONS

The combination of an HP 1000 and IMAGE/1000, Hewlett-Packard's new data base management software, provides a new entry level for data base management applications. For under $65,000 Hewlett-Packard provides a complete set of tools that allows better management of manufacturing and design information. IMAGE/1000 assists in organizing a company's individual data files into a single data base so that relevant information is available to those who need it, when they need it. IMAGE/1000 utilizes a logical and easy-to-understand structure that makes the construction of a data base a straight-forward task. IMAGE automatically links together related information and reduces redundant data. Users can have multi-terminal, multi-program access to the data base for concurrent and interactive retrieval and reporting of information.

Using IMAGE/1000 doesn't require programming skills. Non-technical people can access the data base with QUERY, a "free form" inquiry language. By merely typing simple, English-like commands on a terminal, an authorized operator can retrieve, enter, modify or delete data.

With QUERY, a user can quickly find any record in the data base by a "key value", such as a name, customer account or part number. There's no need to know the address of the data, or to search sequentially through records.

QUERY is especially useful in generating impromptu reports and getting answers to one-time, "What if?" questions. For example, "What if there were a change in the styling of a product's design?" "How would material requirements and lead and delivery times be affected?" Access to an IMAGE data base can provide immediate answers to such questions. Special formatting features such as forms, titles, page and column headings, data sorting by categories, subtotals, totals and averages all contribute to readable, understandable reports.

You can receive more information on IMAGE, by circling A on the reply card.

HEWLETT-PACKARD COMPUTER ADVANCES

THE VERSATILE HP 1000

A new sprint speed computer is the nucleus of each HP 1000 System. It provides the important performance necessary for multi-programming, multi-user application environments. The new processor executes most instructions 60%-100% faster and performs floating point operations 250% faster than its predecessor.

Processor growth power is built into each HP 1000 in a number of ways. First, a variety of peripheral and software options enable users to upgrade from the smallest HP 1000 model to the largest as their requirements expand. Next, fast, low cost, semi-conductor, main memory capacity of up to 608k bytes is twice that of comparable systems. And the HP 1000's new processor uses a very high performance control processor, or "computer within a computer," that enables a user to increase computational horsepower almost at will. A simple terminal oriented language and editor can be used to create and load small routines, or even entire applications or operating systems into the control processor's large address space for faster execution. One HP implementation of this concept increases FORTRAN performance from 2 to 20 times over the non-microcoded execution. The HP 1000 is a computer that strenuously resists being obsoleted by demands for more processing speed.

Advanced interactive display. The System 1000 also takes advantage of the innovations in the fast new 9600 baud, high resolution screened HP 2645 Display Station. Pocket sized mini-cartridges can be used for convenient storage of programs close to your heart, or for real time logging of data entry transactions on the dual cartridges.

The 2645's "Soft Keys" can be programmed to automatically enter multiple keystroke sequences. With a single stroke of a user defined "Soft Key," you can load or compile a program, query a data base, or monitor the status of multiple tasks.

Multi-talented operating software. The HP 1000 System has a voracious appetite for many different applications because its power can be applied in many ways. The HP 1000 operating system orchestrates interactive program development from multiple terminals concurrently with batch processing. Multi-lingual programming—in FORTRAN, ALGOL, HP Assembly and Multi-User Real-Time BASIC—allows users to communicate with the system in the language that best suits their requirements.

Rapid access disc. The performance demands of disc active applications, such as data base management and multi-terminal applications, are met with latest track-follower disc technology and the micro-processor based control unit of the system's HP 7905 Disc. The HP 1000's disc storage capacity of up to 120m bytes allows the construction of a data base large enough to serve most small to medium-sized organizations.

Standard Instrument Connections. Thanks to the Hewlett-Packard Interface Bus (HP-IB*) the HP 1000 can be put to work in nearly any kind of automated electronic or electrical testing measurement and control application. With an HP-IB interface kit, the HP 1000 can control multiple clusters of instruments, each consisting of up to 14 HP-IB compatible instruments. More than one hundred HP-IB interfaceable measurement and test instruments are now available from Hewlett-Packard and other instrument manufacturers.

And Network Connections. If you use more than one computer within your organization, linking these "islands of automation" can give you more complete control of your operations and significantly greater flexibility in collecting and managing information.

This well-balanced combination of HP 1000 computer system power, and IMAGE/1000 make dynamic, user-oriented information handling a reality at an exceptionally low cost. An HP 1000 data base management system can be dedicated to a single department or to an entire company. Or several such systems can be linked in network, allowing each local data base to be shared by users throughout the network. Prices for complete data base management systems from Hewlett-Packard start at $61,200.*

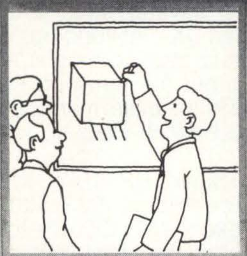
Four basic HP 1000 system models priced from $33,500** to $62,200,** make the HP 1000 the lowest cost member of the Hewlett-Packard family of major computer systems. HP 1000, an ideal starter system for experienced OEM's and end users, is followed by the HP 2000 Timesharing and the powerful multi-programming, multi-lingual HP 3000 Series II.

If you would like more information on how the affordable HP 1000 can be dedicated to a demanding application or distributed throughout an entire network to perform where the work is, circle B on the reply card.

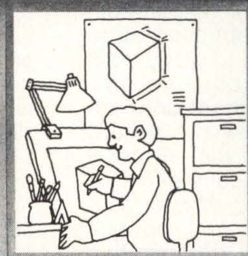
*The Hewlett-Packard Interface Bus. (HP-IB) is HP's implementation of IEEE Standard 488 and identical ANSI Standard MC1.1, "Digital Interface for Programmable Instrumentation".
**Domestic prices FOB California

The 2645's "Soft Keys" can be programmed to automatically enter multiple keystroke sequences. Circle C for more information on the HP 2645.

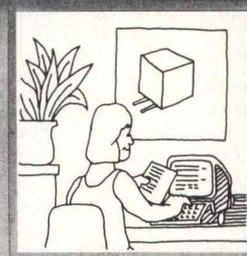
THE HP 1000 IN MANUFACTURING: HELP IMPROVE PRODUCTS,



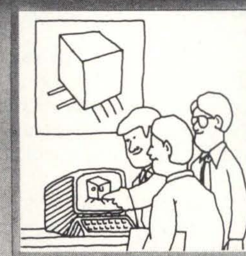
Unique HP 1000 Computer Systems can help turn design concepts into profitable products. Powerful yet affordable, HP 1000's can automate phases of the manufacturing cycle, shorten development schedules, optimize product design, increase productivity, and control manufacturing operations.



Optimize Product Design. For quick solutions to complex design problems, HP 1000 Systems include a new CPU 60% to100% faster than its predecessors. It easily handles "computation heavy" tasks such as array manipulation, numerical integration and differentiation. Programming choices are FORTRAN, BASIC & ASSEMBLY.

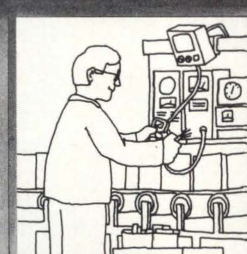


Perform Simulations. Raw speed also makes HP 1000 Systems ideal for other computational tasks such as design simulation, modeling and life testing. Special purpose or frequently used routines can be microprogrammed for even faster execution—at cycle times as short as 175 nanoseconds.



Computer-Aid Designs (CAD). With large main memory to 608 k bytes and fast disc swaps (average time: 100 milliseconds), the HP 1000 can handle the extremely long programs often found in CAD applications such as three-dimensional projections of mechanical parts and automated drafting systems.

Automate Materials Handling. Easy interface with sensors, transducers and electrical contacts makes the HP 1000 a logical choice for control of automated material handling equipment. Multiple terminals can be placed at strategic locations—receiving, incoming inspection, stockroom—to guide flow of material.

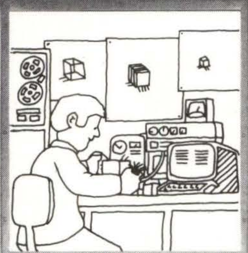


Automate QC Test Stations. Automating QC test stations is a simple procedure with HP 1000 Systems. Multiple clusters of up to 14 HP-IB instruments can be assembled for concurrent testing of component, subassembly, or finished-products. New test stations can be added concurrently with other system activities and test operations.

Collect Factory Data. Each HP 1000 can support up to 56 low-cost data collection terminals. Dispersed terminals can collect up-to-date information about production status, material location, labor costs and machine utilization for a manufacturing data base maintained by IMAGE.

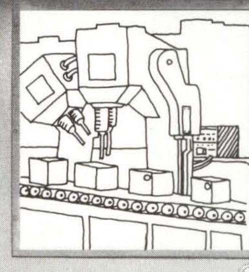
*The Hewlett-Packard interface bus (HP-IB) is HP's implementation of IEEE Standard 488-1975. "Digital interface for programmable instrumentation."

A MULTI-TALENTED TOOL THAT CAN PRODUCTIVITY & PROFITS.

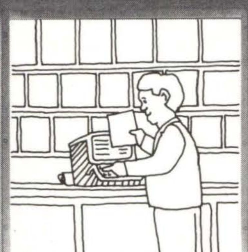


Computerize Bill-of-Materials. Using an HP 1000 to build and modify bills-of-material makes it easy to compute material costs, respond to change orders and produce accurate kit-pull instructions. With IMAGE/1000, engineers can quickly locate part numbers for a particular component and determine which stocked parts meet design requirements.

Automate Prototype Testing. Full, automatic testing of design prototypes can spot design flaws before they become production fiascos. An HP 1000 with HP-IB* Interface Kits let engineers set up specialized test stations quickly. Programming test procedures are simple BASIC "PRINT" or FORTRAN "WRITE" statements.



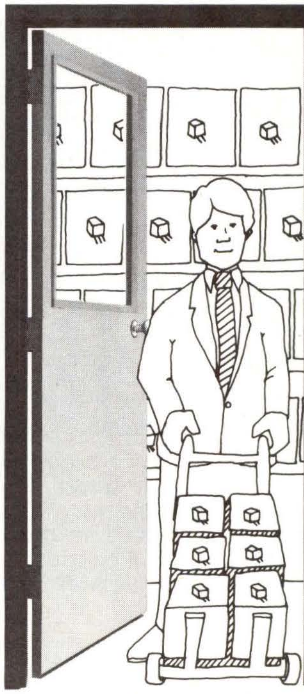
Computer-Aid Manufacturing (CAM). HP's broad line of analog and digital subsystems gives HP 1000 users tools needed for control of production processes. RTE operating software's priority scheduled program execution, performs critical tasks immediately. Networking capability lets each HP 1000 direct satellite measurement/control computer systems.



Plan Material Requirements. IMAGE/1000 also provides the power for a full material requirement planning system. Once bills-of-material and inventory level have been stored in a data base, the HP 1000 can compute net material requirements from a production schedule, interactively from an HP 2645 or in batch mode.

Process Customer Orders. An HP 1000 with IMAGE/1000 provides a common integrated database, making current information available to all departments for control of customer orders. Using QUERY, an English-like inquiry language, clerks can quickly locate open orders, input changes or add new information.

Generate Management Reports. QUERY also makes it easy to generate special management reports on customer order or production status. No special programming skills are needed to extract information from an interrelated IMAGE data base.



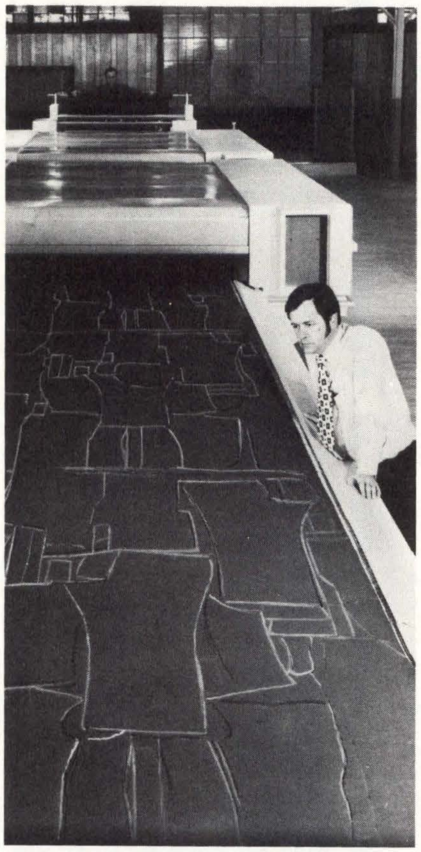
To find out more about how HP 1000 Computer Systems can improve products, productivity and profits, circle B on the attached reply card.

"A MINI IS NOT JUST A SMALL BIG COMPUTER"

Hughes Aircraft Company's Industrial Products Division, Carlsbad, California, realizes, as production control expert George W. Plossl wrote, "manufacturing control is the last frontier for profits." Large dollar savings can result from small improvements in manufacturing control. For that reason Industrial Products Division installed a Hewlett-Packard 21MX minicomputer with IMAGE Data Base Management software to handle manufacturing information control.

Jack McNamee, data processing manager for the Division, says, "we confined our search for computerized control to on-line, interactive systems that are user oriented, and that require a minimal data processing staff and no programmers. To ensure that the information was timely and immediately available, we want CRT display terminals strategically placed throughout the plant. We wanted as few printed reports as possible.

"We researched carefully," McNamee says, "and found that the Hewlett-Packard 21MX minicomputer offered the advantages of low cost, short delivery time, reliability, prompt service and easy upgrading."



Manufacturers of a broad line of automated Lasercutters designed for the apparel industry, Hughes Aircraft Co. saves time and cost since installing a Hewlett-Packard minicomputer and ASK manufacturing software.

In the search for a company to provide the needed software, McNamee found ASK Computer Services, Inc., in Los Altos, California. ASK specializes in computerized manufacturing management systems and their MANMAN (MANufacturing MANagement) software runs on the HP 21MX with IMAGE. MANMAN is an on-line, interactive, multi-user program providing inventory control, bill of materials processing, purchasing and receiving, work in process, and material requirements planning.

According to Sandra Kurtzig, president of ASK, "The 21MX and IMAGE represent the latest technology in data base management at a price that allows a company to dedicate a computer resource to a specific application. Not many people are aware just how powerful a minicomputer is. The 21MX, with 64K to 608K bytes of memory, disc storage, and speed, is ideally suited for manufacturing management applications. A mini is not just a small 'big' computer, but a unique tool all by itself."

As the Hughes division put the MANMAN system on the line, McNamee found that it disciplined the manufacturing environment. The software system has built-in edits to automatically check for errors and to assist in maintaining data integrity. For example, these edits eliminate duplicate entries into the data base and immediately reject transactions against invalid parts, assemblies, purchase orders, etc. As a result, accurate entries must be made.

The system's user orientation simplifies data entry. For instance, when parts are withdrawn from stock for work orders, a clerk need only enter the work order number. The computer will automatically make the necessary on-hand inventory adjustments for all parts on the current bill of materials for that work order. The IMAGE/QUERY system can pull information not ordinarily compiled. For example, finding all vendors of a particular part or all customers for a piece of equipment.

When the system was first installed, the plan was to fully implement MANMAN for each of the Division's five product lines one at a time. The first task was to provide complete inventory control for the production equipment line. Because of the immediate visibility into the inventory of that line, and the resulting financial control, management requested that inventory for all product lines be computerized before implementing the additional system functions. Currently, the entire MANMAN software package is in use.

The savings so far in manpower alone have been substantial. Prior to computerization, it took three full-time people to enter stock room transactions. Because of paper work back logs, it sometimes took up to three weeks for transactions to be posted. With MANMAN on the HP 21MX, it now takes only one person two to three hours a day to enter stock transactions and inventory is always current. The computerized system has eliminated redundant record keeping, reduced stock record keeping time by 90 percent, and maintained a cyclic inventory based on usage dollars throughout the year (eliminating overtime for inventories). The accounting department, which used to receive bundles of transaction slips for balancing and entry into the general ledger, now receives a complete and balanced register at the end of each day.

Says McNamee. "We certainly have a more disciplined production system now, and tremendously more accurate records. I know that we have a better handle on expense control and we expect improvement in customer order delivery. The computer handles the manual tasks and frees our people to concentrate on their other responsibilities."

McNamee is pleased with both IMAGE on the 21MX and MANMAN. "ASK has integrated the latest in functional technology with the latest in systems technology. The combination of Hewlett-Packard and ASK software gave us immediate implementation and operational leverage without a long development cycle. We can concentrate on manufacturing, our specialty, rather than on computers and programming."

For more information on how diverse organizations are using HP's wide ranging computer products, circle D on the reply card.

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for use in video tape editing, presents time signals in hours, minutes, seconds, and TV frames (approximately 30/s) and is used as a precision time standard throughout the plant.

Each of 320 outputs contains a data code which identifies the input connected to it. Certain outputs are tested by the channel computer to verify that the selected inputs are energized. If verification does not occur, the switching central operator is alerted.

Each channel computer is tied to the keyboard computers via the communications controller and intercomputer data links. These links provide access for the operator in switching central when he wants to make a programming change for a channel. All changes are fed in by the operator through the keyboard processors.

All of the daily program for an individual channel is on disc. Data loaded via the communications controller are stored on the disc (one per computer); and as the day progresses, a core-based operating system processes pieces of those data and manipulates them to make the proper sequences of events occur.

Actually, two days of events, including two alternate sequences, can be stored on disc. CPU core memory contains only a copy of the next 20 events. As each event goes on the air, a new event moves from disc to core. The channel computer can continue to operate, however, even if its disc fails. Its core-resident software system relays a take-over request to one of the keyboard computers which then automatically replenishes the core event file as events are transmitted.

Interfaces required for man-machine relationships between the switching central operator and the channel computers are illustrated briefly in Fig. 2. The data display terminal, a CRT, shows the operator what is being transmitted over a particular channel—the current program—and also what events are scheduled during the next time period.

If changes are required that are too time critical for routine channel access via the keyboard computer, the operator can access the channel computer through the manual function/tally (indicator light) panel to control the channel computer in real time. In addition, this panel can be used to perform routine checks of computer operation.

A separate panel allows the operator to input news bulletins and special events or for emergencies which require bypassing the computer system. When the operator assumes manual control he can select and switch onto the channel any of 100 sources that feed the master grid.

One monitor housing display shows exactly what is being transmitted over a channel as the current program. A second monitor can be used to view the backup or "protection" tape or to preview the program that will be transmitted during the next time period.

Audio/video transition and effects are controlled by the channel computer: cross-fades and audio-over and

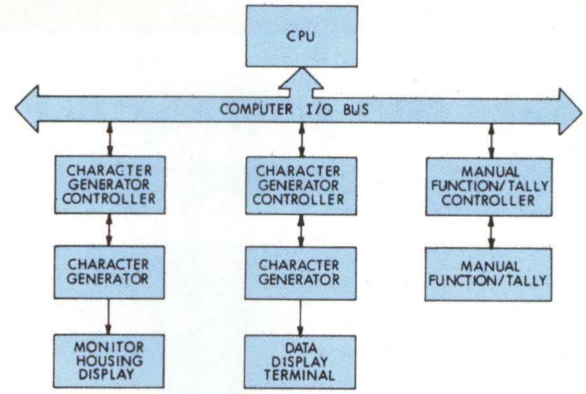

Fig. 2 Operator-oriented interfaces.[3] Data display CRT and video monitors provide visual indications of current and upcoming events on particular channel. Panel permits operator to manually override or modify computer control

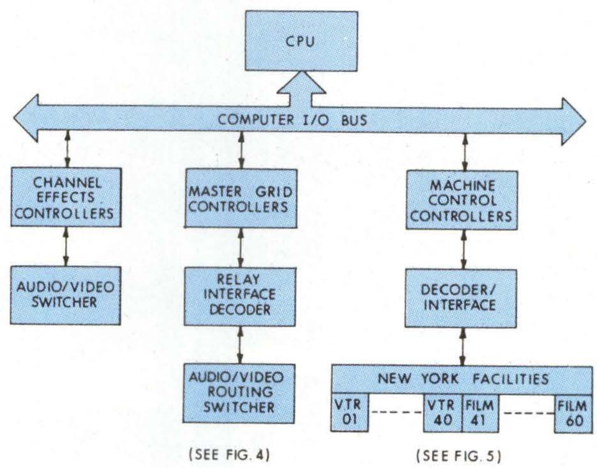

Fig. 3 Audio/video program interfaces.[3] Channel computer controls transitions and effects from both audio and video devices. It accesses each device five minutes in advance and maintains sole control of device until no longer needed

audio-level selections, and video dissolves and inserts (Fig. 3). The channel computers constantly check five minutes in advance to gain control of the devices or facilities required for the next program segment. Channel computers have access to a large number of devices such as video cartridges or tape recorders, and any device can be accessed by any computer. However, once a device is acquired by a computer it remains totally under the control of that computer


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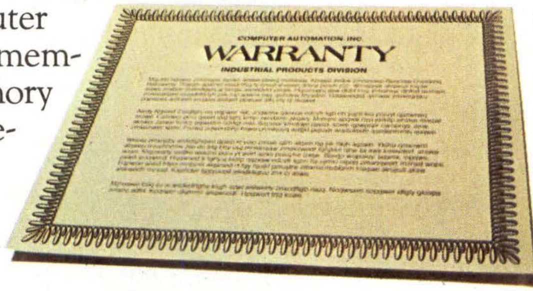

Next, there's Guided Fault Isolation (GFI) with both a single point probe and our new Clever Clip,™ which can handle IC's up to 24 pins. This not only makes testing faster, but also minimizes the chance for error because the operator has less to do. There's even a special readout that tells you if the clip isn't making proper contact with the pins.

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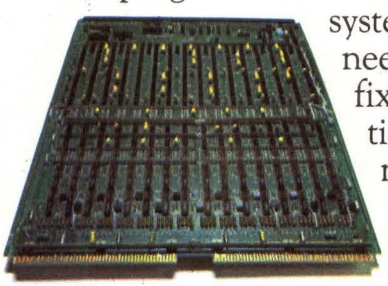

And since our entire system is modular, you can add pin electronics up to 767 pins as your boards become larger and more complex. You can add additional memory as your test routines become larger. You can add new logic families. Or you can convert your CAPABLE into a complete analog test system. All as you need it.

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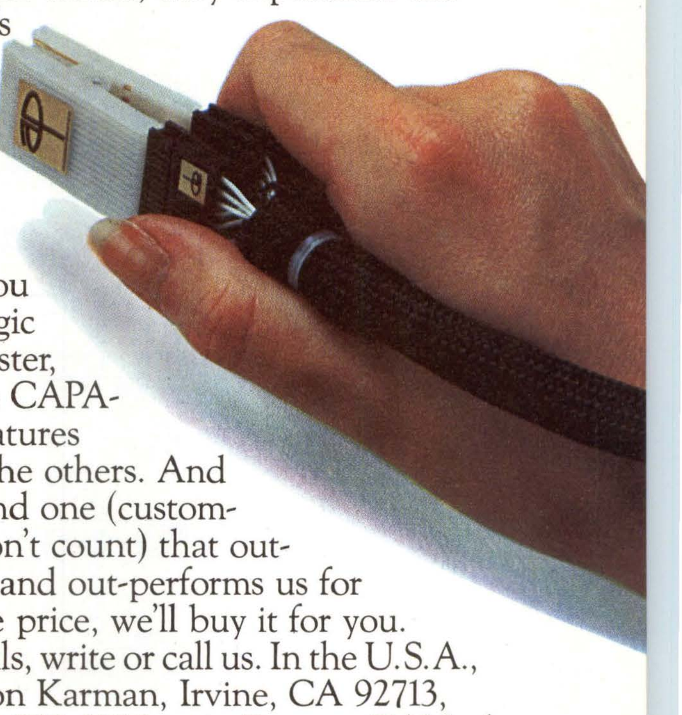

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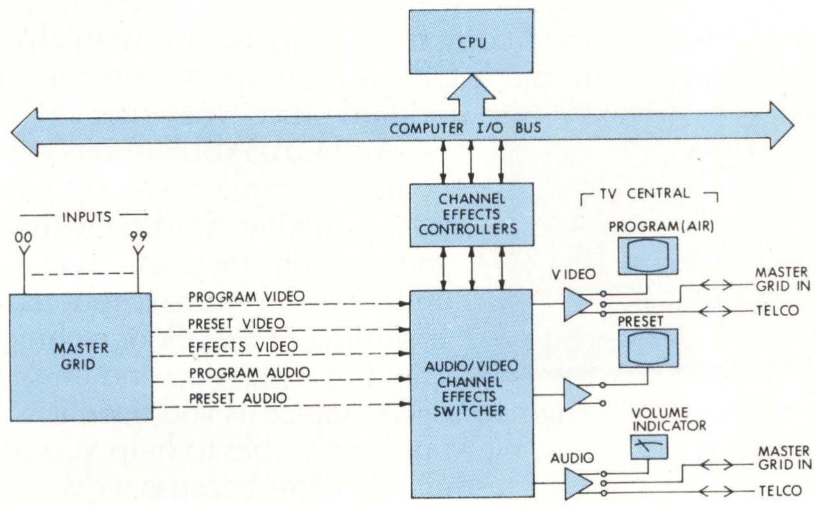

Fig. 4 Audio/video channel effects-switcher interface[3] (expansion of left column of Fig. 3). Master grid has access to 100 audio and video devices

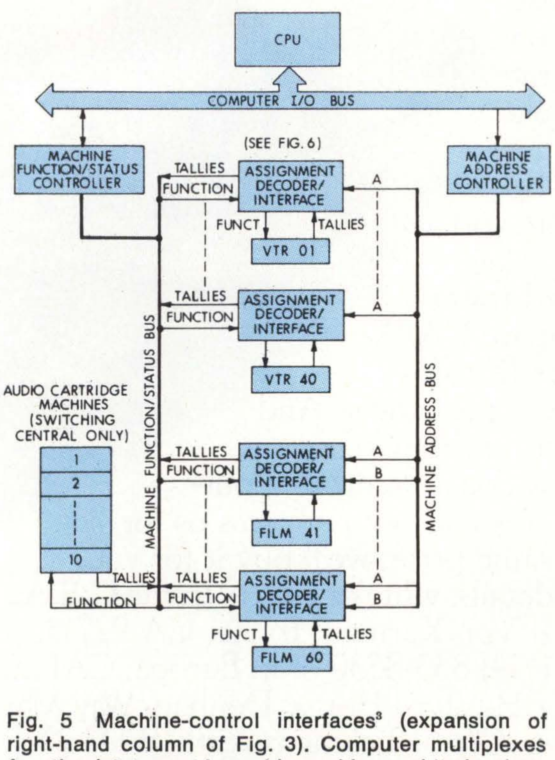

Fig. 5 Machine-control interfaces[3] (expansion of right-hand column of Fig. 3). Computer multiplexes function/status and machine address signals along respective buses to proper assignment decoder/ interface

and cannot be accessed by one of the other computers until released.

Rolling devices start five seconds before they are switched on the air. Ten seconds prior to that a preset monitor switches on to permit an operator preview of what will be transmitted. The computer will automatically switch on a "protect" device if the originally specified device fails.

As more clearly shown in Fig. 4, an expanded presentation of the center column of Fig. 3, the master grid accepts inputs from 100 available audio and video devices and feeds items such as program, effects, and preset video and program and preset audio to the channel effects switcher along five buses. This switcher is supported by the channel effects controllers which in turn are controlled by the channel computer via the I/O bus. Outputs of the channel effects switcher are re-entered into the master grid for monitoring and then fed to the telephone line for distribution. As discussed previously, monitors show both on-the-air and preset (preview) video. A volume indicator, a specially designed voltmeter, reads both rms and peak values of audio signals.

Fig. 5, an expanded version of the right-hand column in Fig. 3, shows the interfaces involved in machine control. Both machine function/status and machine address controllers are multiplexed by the computer along their respective buses to the assignment decoders/interfaces. Each controllable device is assigned a unique address line that causes its decoder/interface to come under computer control when activated by a computer.

Four commands from the channel computer will be accepted by the interface system; the feedback

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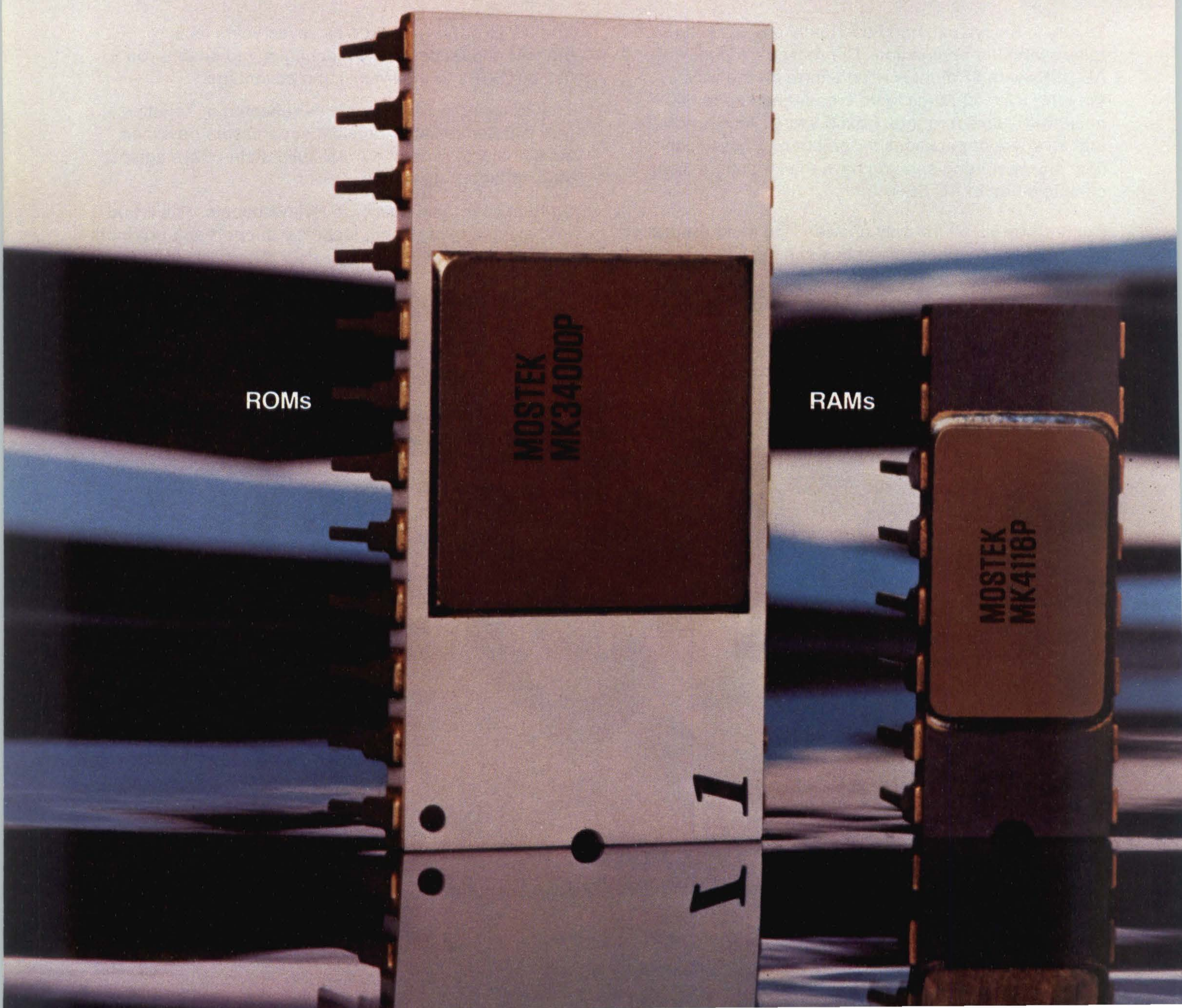

Random Access Memories

Description	Part No.	Access Time
256-Bit Static	MK 4006P—6	400ns
	MK 4008P—6	500ns
1K Dynamic	MK 4007P(N)	525ns
	MK 4007P—4(N)	525ns
1K Static	MK 4102P	$1\mu s$
	MK 4102P—1	450ns
	MK 4102P—6	275ns
	MK 4102P—8	250ns
4K Dynamic	MK 4096P—6(N)	250ns
	MK 4096P—11(N)	350ns
	MK 4096P—15(N)	350ns
	MK 4096P—16(N)	350ns
	MK 4200P—11(N)	350ns
	MK 4200P—16(N)	300ns
	MK 4027P—2	150ns
	MK 4027P—3	200ns
	MK 4027P—4	250ns
4K Static	MK 4104P*	200ns
16K Dynamic	MK 4116P—2	150ns
	MK 4116P—3	200ns

Read Only Memories

2K ROM	MK 2400P	550ns
4K ROM	MK 2500/2600P	400ns
8K ROM	MK 30000P	450ns
16K ROM	MK 28000P(N)	600ns
	MK 31000P	550ns
	MK 34000P	350ns

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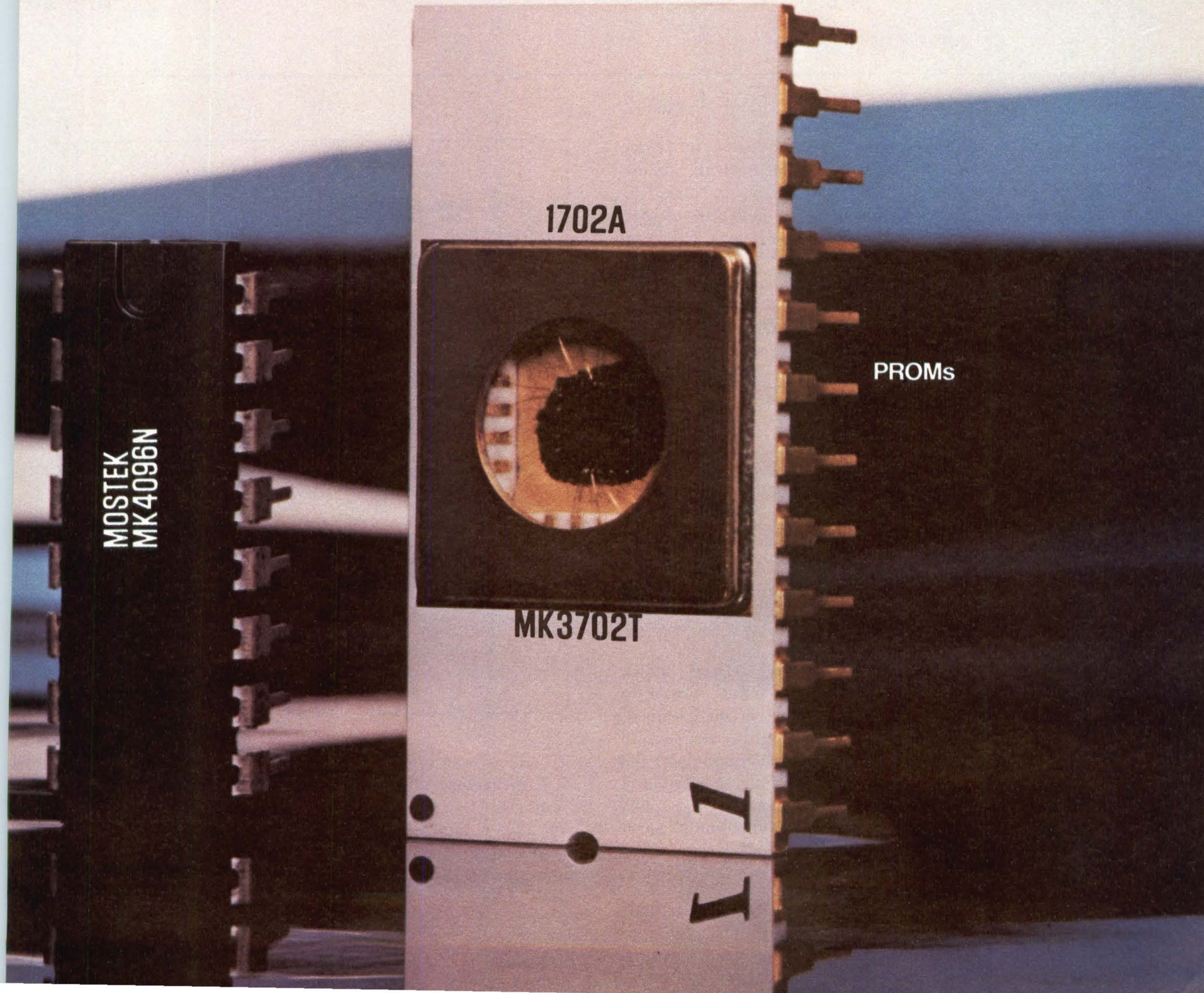


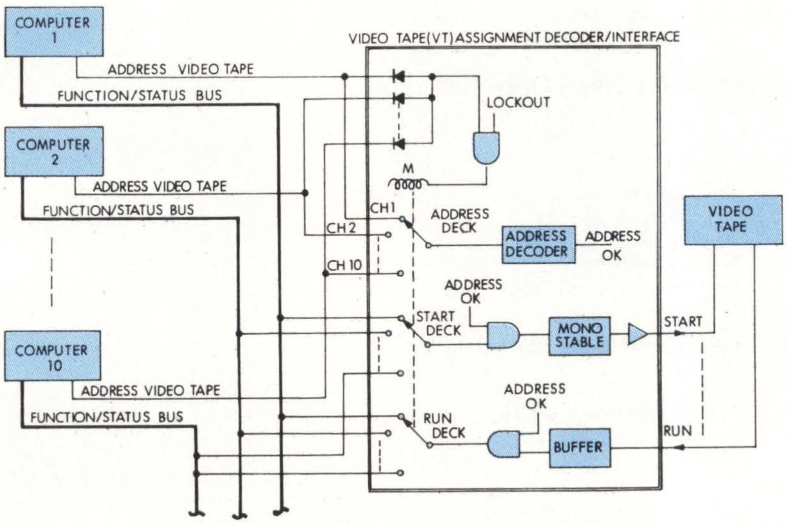


Fig. 6 Function/status switcher[3] (expansion of assignment decoder/interface of Fig. 5). Three relays decode incoming addresses; fourth prevents accidental command from reaching system

consists of three tallies plus a 1-bit address for video tape machines and a 2-bit address for telecine chains. The assignment decoder/interface, shown in more detail in Fig. 6, is made up of a 12-pole, 10-position stepping switch and associated control relays for homing, lockout (interlock logic), release of lockout, and manual stepping. Once a channel computer gains access to a device, its system locks out any other request for control until a release command is issued to indicate that the computer no longer needs the device.

Audio Multiplex

Each video channel is complemented by four audio channels which are encoded into 12-bit pulse-code modulation (PCM) digital signals and then biphase modulated on a 24-MHz subcarrier (Fig. 7). The resulting rf envelope is mixed with the baseband video signal and routed through the switching system as a multiplexed signal.[4] Each video signal occupies a full 10-MHz bandwidth while combined audio signals are within a 12-MHz band that is centered at the 24-MHz subcarrier.

The four analog-to-digital converters (ADCs) shown in Fig. 7 sample and convert audio input signals to separate 12-bit PCM codes. Each code is then sequentially loaded into a parallel-to-serial shift register to make up the digital train which will modulate the biphase modulator. Sync, address, data, parity, and zero bits are added to each audio sample of 12 bits within the shift register to form one 20-bit audio word. The bit patterns for four successive audio words are shown in Fig. 8. In operation, these four audio words are formed 75,000 times a second (6 million bits/s).

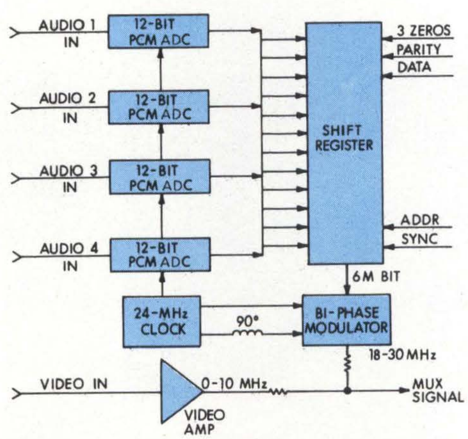
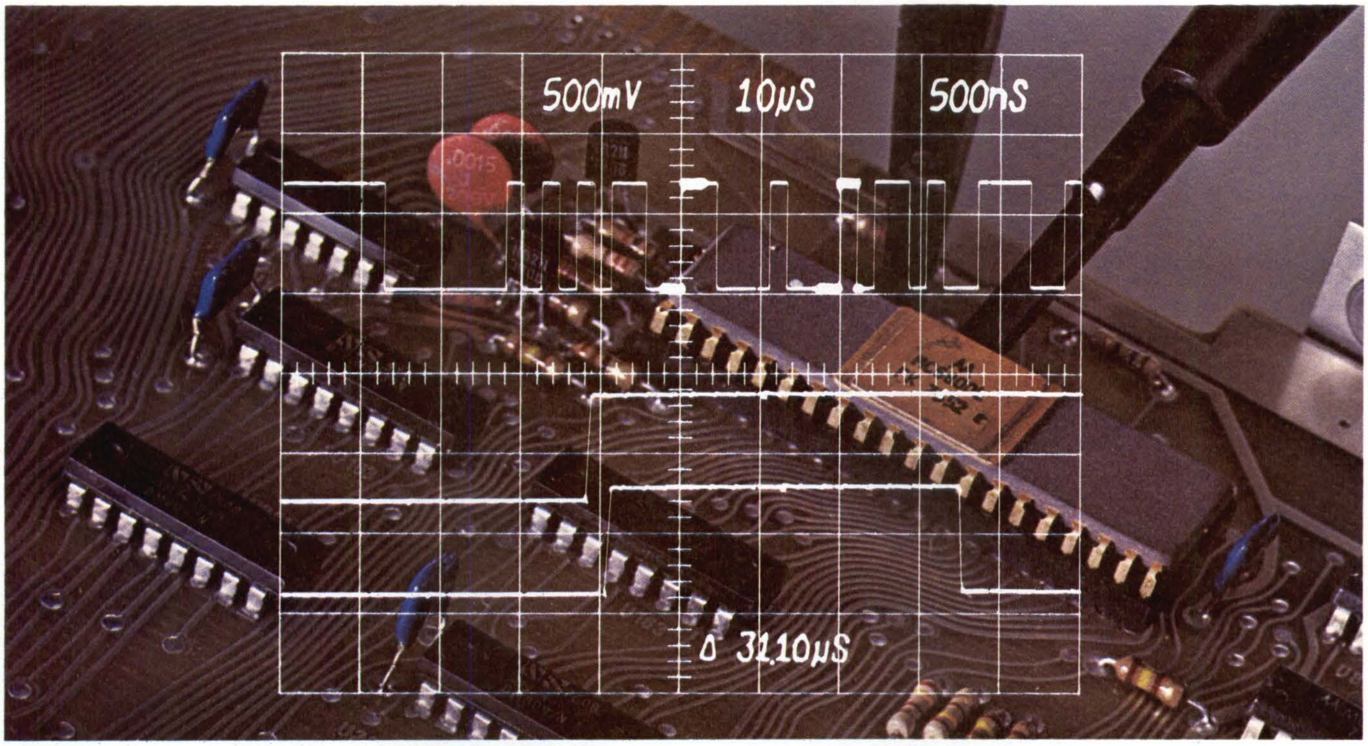


Fig. 7 Multiplexing scheme.[4] Signals from four audio channels and one video channel are encoded by analog-to-digital converters (ADCs) and transmitted through switching system within rf envelope as multiplexed signal

An envelope of rf energy from 18 to 30 MHz is produced by a biphase modulator operating at the 24-MHz primary clock frequency. When this envelope is added to the video signal the combined signal is multiplied to supply 320 discrete crosspoints, one for each of the 320 switcher outputs.

(Continued on p 70)

For your pulse and digital timing measurements



The instrument shown includes a 7904 mainframe configured for pulse and digital measurements. Our △ time plug-ins, the 7B80 and 7B85 time bases, give you differential time measurements with sweep rates to 1 ns/div. The 7A19 provides one vertical channel with a rise time of 0.8 ns and the 7A26 provides dual channels with rise times of 1.8 ns.

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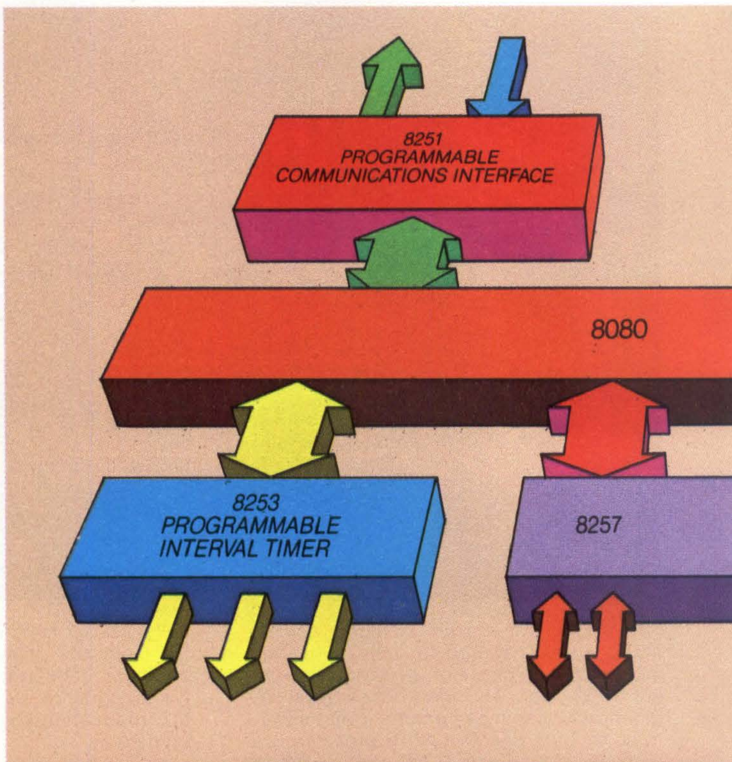

Now you can get microcomputer based products out of the lab and into production faster than ever before. Intel® 8080 programmable LSI peripherals give you the competitive advantage by helping you reduce design time, component count and manufacturing and inventory costs. Most of all they'll help you get to market first.

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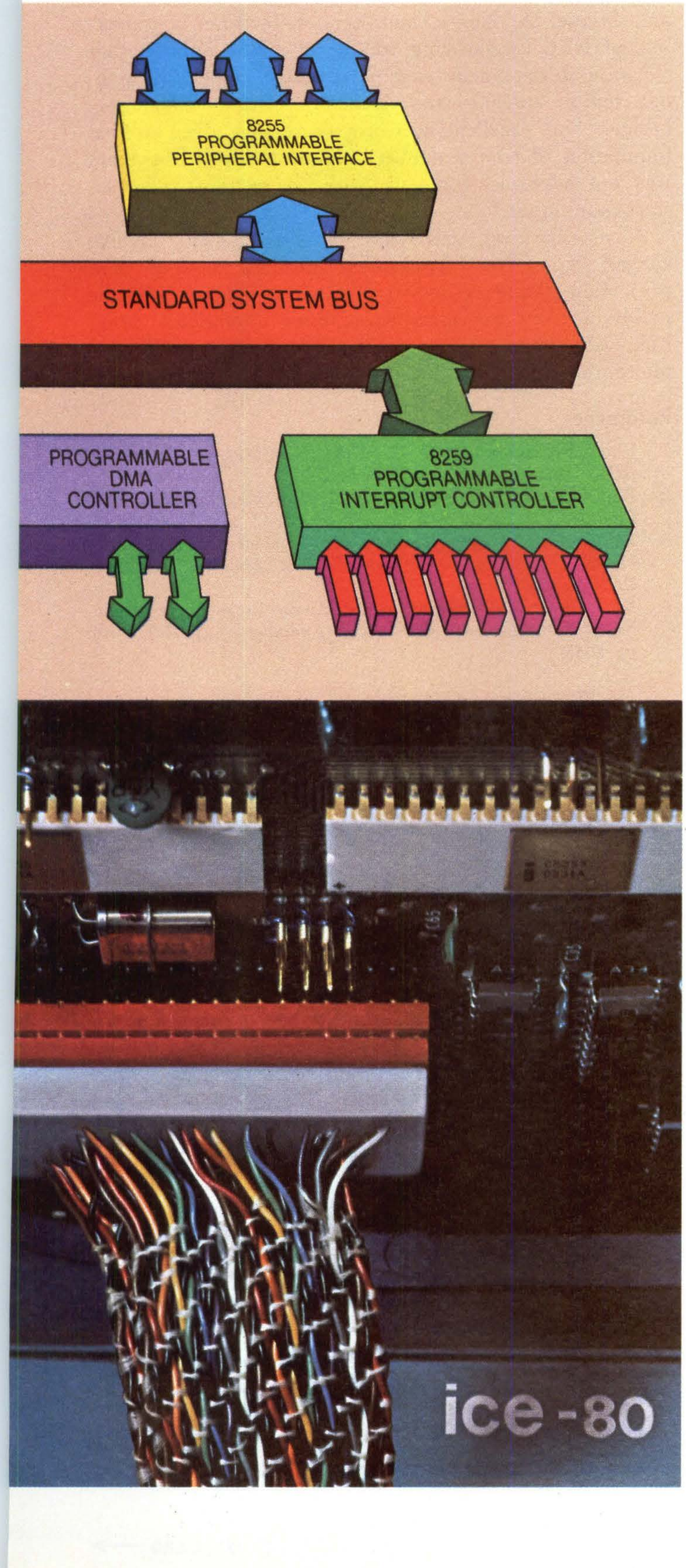

munication protocols, including IBM Bi-Sync. For "parallel I/O," each 8255 Programmable Peripheral Interface gives you 24 versatile I/O lines to interface relays, motor drives, printers, keyboard/display and other parallel equipment.

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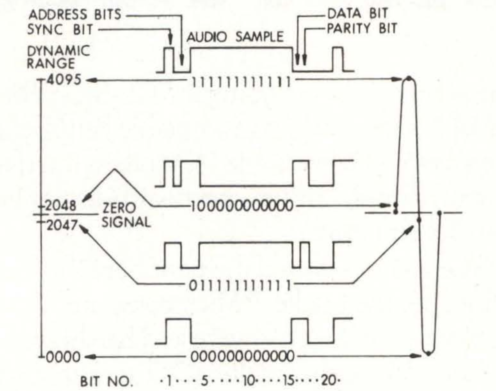

Fig. 8 Bit pattern for four audio words.[4] Such groups of words are formed 75,000 times/s

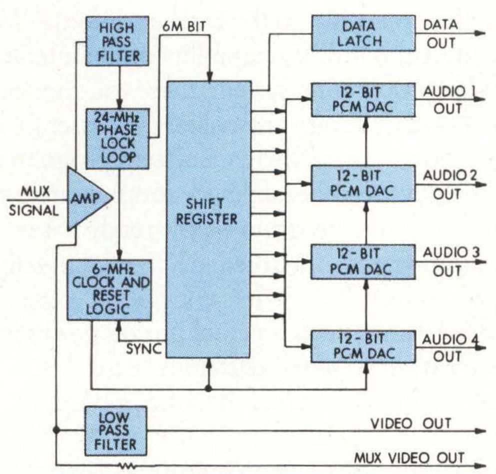

Fig. 9 Audio/video processing after switching.[4] Multiplexed components are separated into two parts by high and low pass filters. Digital-to-analog converters (DACs) return pulse-code modulated (PCM) digital signals to analog form

Filter circuits separate multiplexed components into two parts after switching and routing (Fig. 9). All energy below 10 MHz is routed through a low pass filter to the video output port, while a high pass filter allows the rf envelope from the biphase modulator to reach the 24-MHz phase lock loop. Digital-to-analog converter (DAC) outputs are band limited to 15 kHz and become the four system audio outputs.

Current and Future

When the switching central first went into automatic operation in October 1974, it was online for only four hours each morning to determine what problems existed. Then the system was switched back to manual for the remainder of the day for debugging.

In January 1975, operation was extended to 1 pm, in March it ran to 4:30, and by August—less than one year after initiation—it was on a full 24-hour schedule. The early operating periods were chosen for the beginning of the day in order to fully debug the system before it was used in prime time periods.

Robert J. Butler, director of technical development, and Miguel A. Negri, manager of facilities engineering, of NBC Engineering concurred in the opinion that software development was particularly successful without major hitches—and basically within schedule—because "an excellent software team was given a firm foundation of technical operating procedures. The team was not asked to come up with a program and then start changing it."

A new project, currently in design, will involve control from New York City headquarters of film projection facilities in New Jersey. Control will be maintained by microcomputers over a communication link. Although not yet implemented, RCA COSMAC microprocessors will be the controlling elements.

References

1. F. L. Flemming, "NBC Television Central—An Overview," *RCA Engineer*, Apr/May 1976, pp 2-4
2. R. Edmondson and R. Post, "NBC Switching Central," *RCA Engineer*, Apr/May 1976, pp 7-17
3. M. A. Negri, "Hardware Interface Considerations for Multi-Channel Television Automation," *RCA Engineer*, Apr/May 1976, pp 18-23
4. R. J. Butler, "PCM-Multiplexed Audio In A Large Audio-Video Routing Switcher," *RCA Engineer*, Apr/May 1976, pp 42-45

DC&AS BRIEF

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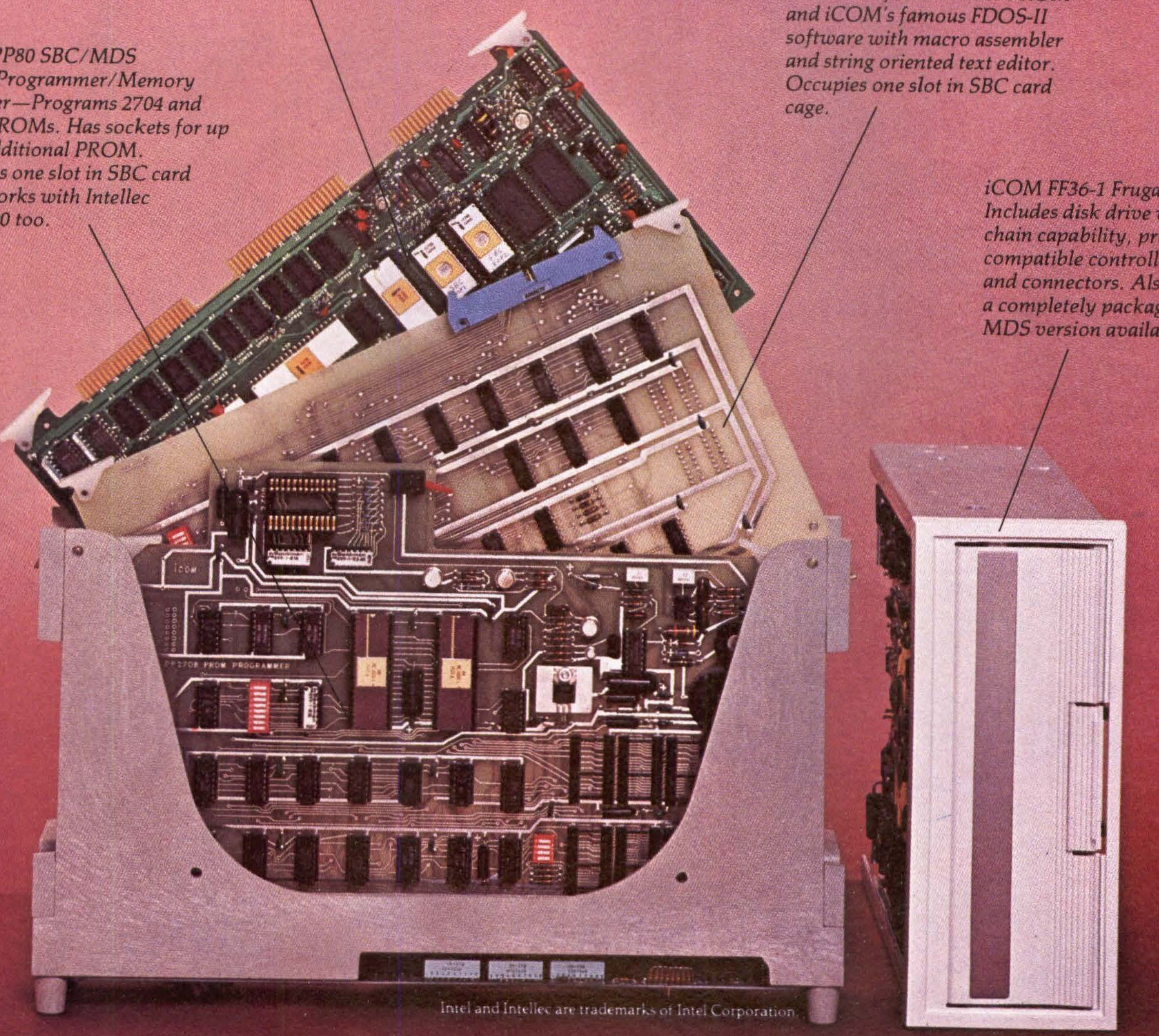

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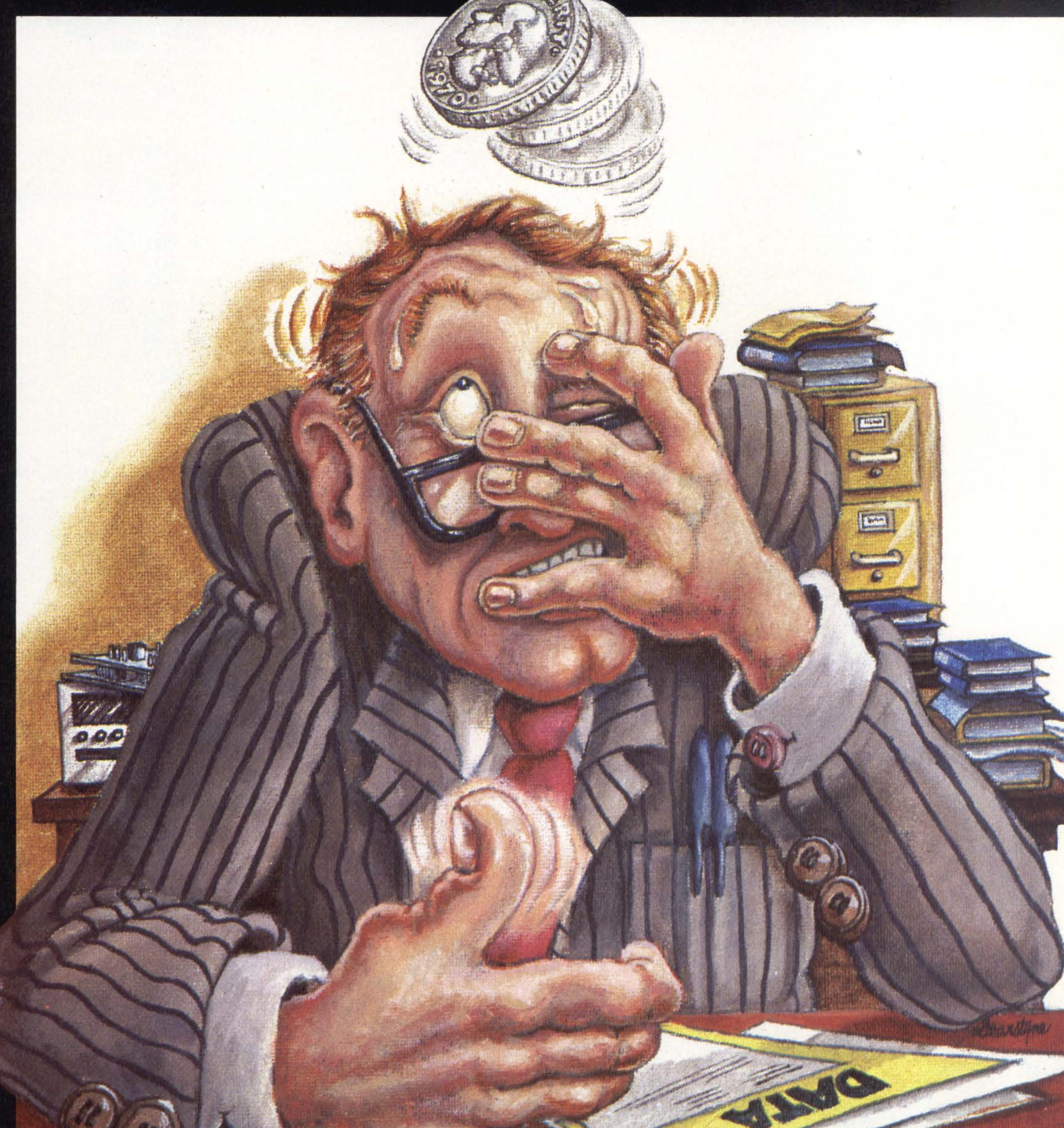
“Nervous Nellie” Nelson choosing his



used to sweat bullets mini memories

Nelson "Nervous Nellie" Nelson.

To avoid undue confusion, had the same first and last names.

Always wore a belt and suspenders at the same time.

Owned several shares of Amalgamated Safety Pin.

Hated to make decisions. Especially when choosing minicomputer memories.

"Nervous" was *sure* he didn't like the high prices of the mini manufacturers.

Yet he was afraid to buy from a lower-priced independent because he wasn't sure what he would be getting.

One day, while shopping for a security blanket, "Nervous Nellie" spotted the following message monogrammed on the label:

"Plessey Microsystems is the largest independent supplier of minicomputer add-on memories there is, and they are part of an international billion dollar corporation. Plessey's low prices are complemented by the high quality and reliability of their products and the comprehensiveness of their support services.

"Plessey Microsystems.

"P.S.: Do not remove this Plessey pitch under penalty of law."

"Hmmm," noticed Nervous. "Billion dollar corporation. Largest independent mini memory supplier. Low prices. Reliable products."

He was certain he sort of liked that.

With a newfound surge of self-confidence, he placed a person-to-Plessey call and reassured himself that Plessey Microsystems was everything the label said they were. And more.

From then on, Nelson Nelson bought all his mini peripherals from Plessey.

And threw away his suspenders.

You, too, can find out how add-on core memories, single and dual disc drives and punched tape readers from Plessey Microsystems can expand your mini at low prices without your having to sweat about the results.

Just call and we'll be glad to tell you more about our products.

The Pacifiers

Plessey disc drive systems store up to four times the data in one quarter of the space at a much lower cost than drives from the mini manufacturers.

They are software, hardware, and media compatible with DEC and Data General minicomputers and they are available in a variety of types and sizes for doing your job your way.

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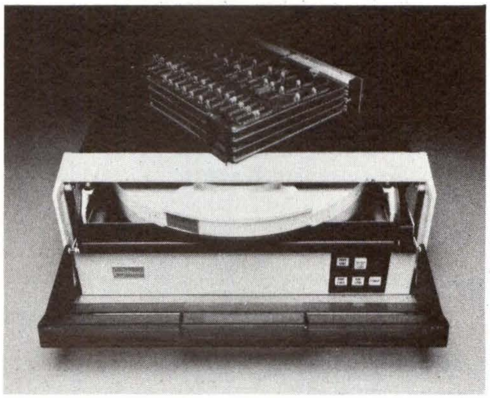

CIRCLE 34 ON INQUIRY CARD

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December 6-8
Washington Hilton Hotel
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International Electron Devices Meeting

Emphasis will be placed on new and significant aspects of research, development, design, and manufacture of electron devices at the 1976 IEDM, which is sponsored by the IEEE Electron Devices Group. Particular subjects to be accentuated are principles, structures, materials, and technology of *solid-state devices;* characterization and developments of materials and devices involved in *device technology; energy conversion devices and quantum electronics*—specifically lasers and semiconductor light sources; radiation detectors, LCDs, LEDs, gas-discharge displays, and modulators involved with *image transducers and optoelectronic devices;* and devices and circuits—MOS, CCD, and magnetic bubbles, and digital circuits for logic and memory—concerned with *integrated electronics.*

The 3-day annual technical meeting will begin at 10 am on Monday with a General Session of invited papers to be chaired by the Technical Program Chairman, Dr Josef Berger, Hewlett-Packard Company. This year's General Chairman is Dr C. Neil Berglund, Bell-Northern Research, Canada.

A luncheon will be held at noon on Tuesday, Dec 7, with guest speaker W. J. Sanders, president of Advanced Micro Devices, Sunnyvale, Calif, discussing the "Trends and Outlooks for the Semiconductor Industry." Other scheduled special events are a cocktail party from 6 to 7 pm Monday, Dec 6 (open bar), and a tour of the National Bureau of Standards on Tuesday evening.

Registration fees at the Conference are $32 for IEEE members, $41 for nonmembers, and $16 for students or unemployed IEEE members. These fees include a copy of the *Technical Digest.* Additional copies will be available for $12 at the meeting; after the meeting, the price is $15 for members, and $20 for nonmembers. Tickets for the luncheon are $12; $5 for the cocktail hour; and $3 for the tour.

Only those sessions of particular interest to readers of *Computer Design* are covered in the following excerpts. Closing times listed for each session are approximate. Information is limited to that available at press time.

TECHNICAL PROGRAM EXCERPTS

Monday Morning

General Session 10 am Ballroom Ctr

Invited Papers

Organizer/Chairman: Josef Berger

"An Experimental Optical Fiber Communications System: Devices and Performance," M. DiDomenico, Jr, Bell Laboratories

"New Directions in Non-Planar Semiconductor Device Technology," H. C. Nathanson, Westinghouse Research Laboratories

"Progress in Low Cost Solar Cells," P. Rappaport, RCA, David Sarnoff Research Center

Monday Afternoon

Session 2 2-5 pm Ballroom Ctr

Integrated Electronics—CCDs and Other Dynamic MOS

Organizer: D. D. Buss

Chairman: J. F. Skalski

"A New Multiplexed Electrode-Per-Bit Structure for CCD Memory," S. Kohyama, H. Hatano, T. Tanaka, and N. Kubota, Tokyo Shibaura Electric Co, Japan

"Merged Charge Memory (MCM)—A New Random Access Cell," H. S. Lee and W. D. Pricer, IBM

"Charge Coupled Devices in Digital LSI," R. A. Allen, R. J. Handy, and J. F. Sandor, TRW Systems

"An Electrically Programmable Transversal Filter," Y. A. Haque and M. A. Copeland, Carleton University, Ottawa

"Antialiasing Inputs for Charge Coupled Devices," C. H. Sequin, Bell Laboratories

"Coplanar Al-Al_2O_3-Al Gate CCD," T. Ohzone, S. Horiuchi, H. Kadota, and K. Kagawa, Central Research Laboratories, Matsushita Electric Ind Co, Japan

Session 3 2-5 pm Ballroom W

Device Technology—Bipolar Process Technology

Organizer: R. K. Watts

Chairman: J. B. Kruger

"Bipolar Linear Integrated Circuit Reliability," G. F. Foxhall, Bell Laboratories

"Reduction of Emitter-Collector Leakages by Ion Implantation," K. D. Beyer, G. Das, M. R. Poponiak, and T. H. Yeh, IBM System Products Div

"A Compatible Bipolar and JFET Process," A. Wang and C. Dell'Oca, Hewlett-Packard Laboratories

"High Performance ECL Gates Made by SEL Method," A. Hayasaka, T. Kaji, Y. Honma, and S. Harada, Hitachi, Japan

"Measurement of Minority-Carrier Lifetime and Surface Recombination Velocity with a High Spatial Resolution," M. Watanabe,

Card on pages 75 & 76 does not appear in certain regional copies

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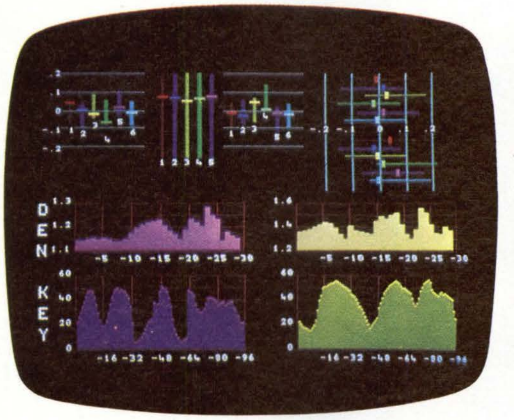

Process Control: Color printing press.

Medical Imaging: Nuclear heart study.

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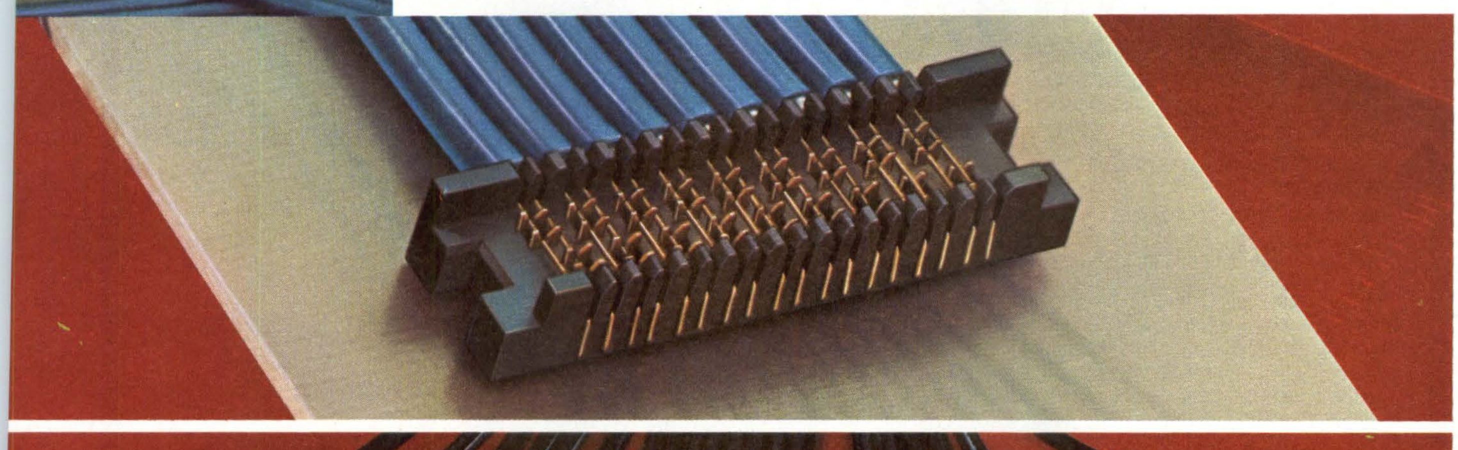

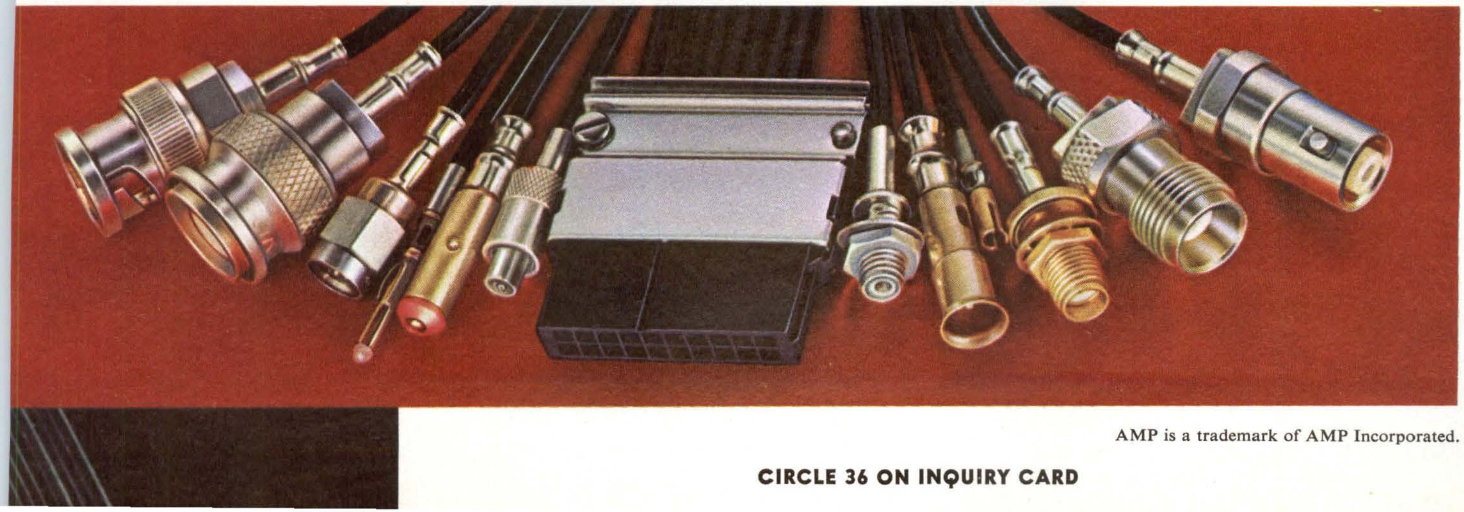

G. Actor, and H. C. Gatos, Massachusetts Institute of Technology

"A Junction Isolation Technology for Integrating Silicon Controlled Rectifiers in Crosspoint Switching Circuits," A. R. Hartman, P. W. Shackle, and R. L. Pritchett, Bell Laboratories

Session 6 — 2-5 pm — Jefferson Room

Energy Conversion—Semiconductor Lasers

Organizer: G. B. Stringfellow

Chairman: J. K. Butler

"Status of Distributed Feedback Lasers," W. Streifer, D. R. Scifres, and R. D. Burnham, Xerox Palo Alto Research Center

"(Al,Ga)As, GaAs Double Heterostructure Lasers Prepared by a New Liquid Phase Epitaxial Growth Technique," Y. Horikoshi, The Musashino Electrical Communication Laboratory, Japan

"Diode Sources for 1.0 to 1.2 μm Emission," C. J. Nuese, RCA Laboratories

"Visible CW (AlGa)As Heterojunction Laser Diodes," I. Ladany and H. Kressel, RCA Laboratories

"Single Heterostructure Tunable Diode Lasers Formed by Compositional Interdiffusion," K. J. Linden, J. F. Butler, and K. W. Nill, Laser Analytics, Inc

"Modulation Characteristics of CW Laser Diodes," T. L. Paoli, Bell Laboratories

Tuesday Morning

Session 8 — 9-12 am — Ballroom Ctr

Integrated Electronics—Static MOS Memory and Logic

Organizer: S. Rosenbaum

Chairman: M. Copeland

"Operation and Characterization of n-Channel EPROM Cells," J. Barnes, J. Linden, and J. Edwards, Advanced Product Development, American Microsystems, Inc

"Endurance of Thin-Oxide Nonvolatile MNOS Memory Transistors," M. H. White, J. W. Dzimianski, and M. C. Peckerar, Westinghouse Electric Corp, Advanced Technology Labs

"A Cross-Point MNOS Capacitor Memory," A. S. Chawla and H. C. Lin, University of Maryland

"Back-Gate-Input MOS—A New Low-Power Logic Concept," S. Asai, T. Masuhara, and T. Nakamura, Central Research Laboratory, Hitachi, Ltd, Japan

"C²L: A New High Speed, High Density Bulk CMOS Technology," A. Dingwall and R. Stricker, RCA Corp, Solid State Technology Center

"Frequency Dependent Propagation Delay in Silicon-On-Sapphire Digital Integrated Circuits," S. Sheffield Eaton, RCA; and B. Lalevic, Rutgers University

Session 10 — 9-12 am — Georgetown Room

Electro-Optical Devices—Optical Modulators, Couplers, and Signal Processors

Organizer: C. H. Sequin

Chairman: B. G. Streetman

"Intergrated-Optics Components: Modulators," E. Conwell, Xerox Webster Research Center

"Coupling Components for Single Optical Fibers," M. K. Barnoski, Hughes Research Laboratories

"Electro-Optic Multimode Multiplexer," R. A. Soref and A. R. Nelson, Sperry Research Center

"Resolution of Spatial Phase Modulators: Measurement Techniques," C. Warde, Massachusetts Institute of Technology

"50 Channel Optical Modulator with Integrated CCD Addressing," D. J. Bartelink and G. Sitts, Xerox Palo Alto Research Center

"Electro-Optical Processing of Signals and Images Using CCDs," D. Roy and M. A. Copeland, Carleton University, Ottawa

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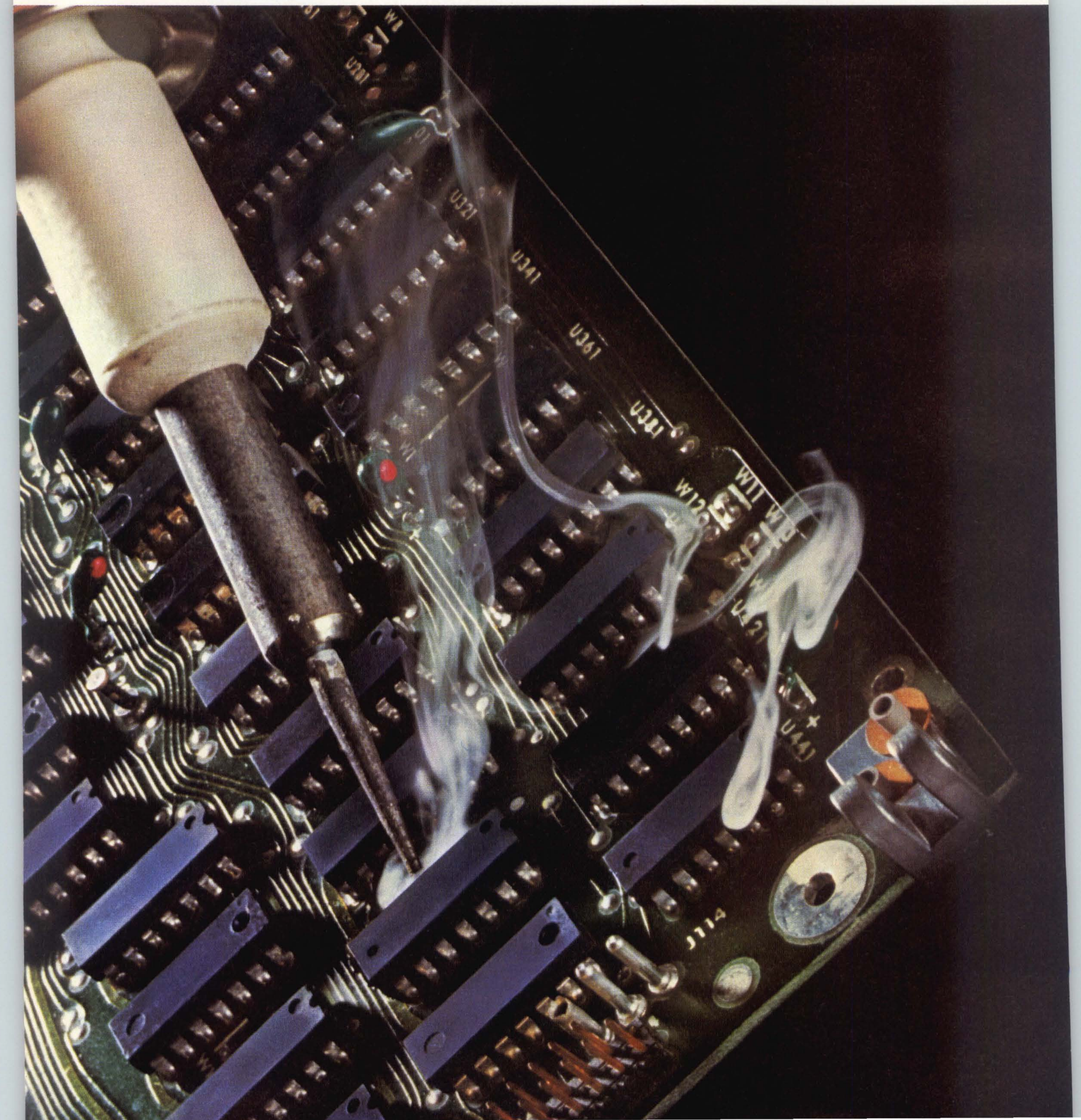

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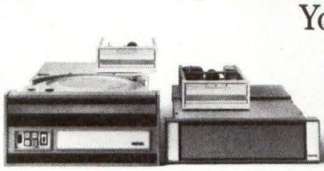

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Session 12 9 am-12:30 pm Lincoln Room W

Solid-State Devices—Novel Devices and Techniques

Organizer/Chairman: D. Hendricks

"Gallium Antimonide Planar Tunnel Diode," S. Kang and W. Ko, Case Western Reserve University

"A Silicon Bipolar-Carrier-Domain Magneto-Current-Generator," Jim Smith, Tektronix Labs

"Schottky Diode Magnetic Sensor of High Sensitiveness," G. Kamarinos and P. Viktorovitch, Institut National Poly Technique, France

"Thermosensor—A New Temperature-Sensitive Switching Device," J. Nakata, T. Sogo, K. Yamanaka, T. Kameda, and Y. Mihashi, Mitsubishi Electric Corp, Japan

"Metal-Oxide Devices for Rapid High Current Switching," G. Gaule, P. La Plante, S. Levy, and S. Schneider, U.S. Army Electronics Technology and Devices Laboratory

"Investigation of the Sapphire-Silicon Interface by Transient Current Analysis," K. Lehovec and R. Miller, University of Southern California

"The Utilization of Charge Pumping Techniques to Evaluate the Energy and Spatial Distribution of Surface States of an MOS Transistor," W. V. Backensto, Hughes Aircraft Co; and C. R. Viswanathan, University of California, Los Angeles

Tuesday Afternoon

Session 13 2:30-5:30 pm Ballroom Ctr

Integrated Electronics—I^2L Technology and Modeling

Organizer: J. G. Fossum

Chairman: J. Saltich

"Physics of and Models for I^2L," F. M. Klaassen, Philips Research Laboratories, The Netherlands

"The Schottky I^2L Technology and its Application in a 24 x 9 Sequential Access Memory," F. W. Hewlett, Jr and W. D. Ryden, Bell Laboratories

"A New High Speed I^2L Technology—Up-Diffused," B. B. Roesner and D. J. McGreivy, Hughes Aircraft Co

"Modular Bipolar Analysis," J. L. Dunkley, Tektronix, Inc; S. D. Kang, Texas Instruments Inc; and P. A. Nygaard, Hughes Aircraft Co

"Base Current of I^2L Gates at Low Current Levels," W. Mattheus, R. Mertens, and J. Stulting, Labo Fysica en Elektronica van de Halfgeleiders, Belgium

"An Analytic Model for the Design and Optimization of Ion Implanted I^2L Devices," S. A. Evans, Texas Instruments Inc

Session 14 2:30-5:30 pm Ballroom E

Device Technology—MOS Reliability, Performance, and Characterization

Organizer/Chairman: D. Farrington

"Failure Modes and Reliability of Dynamic RAMs," C. R. Barrett and R. C. Smith, Intel Corp

"Anomalous Electrical Gate Conduction in Self-Aligned MOS Structures," W. E. Ham, RCA Laboratories; and S. Eaton, RCA Solid State Division

"The Relative Performance and Merits of CMOS Technologies," A. Aitken, A. P. T. MacArthur, R. Abbott, and J. D. Morris, Bell-Northern Research, Canada

"CMOS Process for High-Performance Analog LSI," W. C. Black, Jr, R. H. McCharles, and D. A. Hodges, University of California, Berkeley

"Relationships of Residual Defects and Excess Noise in Ion-Implanted MOSFETs," K. L. Wang, General Electric Co

"Surface Characterization of Ion-Implanted $Si\text{-}SiO_2$ Structures," K. L. Wang and P. V. Gray, General Electric Co

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Session 15 2:30-5:30 pm Georgetown Room

Solid-State Devices—Microwave Transistors and Integrated Circuits

Organizer: C. P. Snapp

Chairman: W. R. Wisseman

"Developments in GaAs FETs and ICs," R. Zuleeg, McDonnell Douglas Astronautics Co

"Gunn Domain Formation in the Saturated Current Region of GaAs MESFETs," R. W. H. Englemann and C. A. Liechti, Hewlett-Packard Laboratories

"Noise in Ungated GaAs FETs," J. Graffeuil, J. C. Martin, and G. Blasquez, Laboratoire D'Automatique et D'Analyze des Systemes du Centre National de la Recherche Scientifique, France

"A Microwave PNP Bipolar Silicon Power Transistor," K. B. Verma, M. Siegel, and R. Wood, Tektronix, Inc

"The Effects of Neutral Capacitance on the Frequency Response of Microwave Transistors," A. Wang, Hewlett-Packard Laboratories

"Interface State Density in Au and Al nGaAs Schottky Diodes," J. M. Borrego, R. J. Gutmann, and S. Ashok, Rensselaer Polytechnic Institute

Session 17 2:30-6:15 pm Lincoln Room W

Electro-Optical Devices—Detectors and Pickup Systems

Organizer/Chairman: B. F. Williams

"Acoustic Imaging Devices for Nondestructive Testing," G. S. Kino, Stanford University

"Integrated Filter Arrays on CCDs for Color Imaging," A. T. Brault, W. A. Light, T. W. Martin, L. P. Dillon, and E. Garcia, Eastman Kodak Co

"Recent Digicon Developments," J. P. Choisser, Electronic Vision Co

"Position Sensitive Photodetectors with High Linearity," G. Petersson and L. Lindholm, Chalmers University of Technology, Sweden

"Epitaxial Silicon n^+-p-π-p^+ Avalanche Photodiodes for Optical Fiber Communications at 800 to 900 Nanometers," H. Melchior and A. R. Hartman, Bell Laboratories

"Very High Speed High Efficiency Silicon Avalanche Photodiodes," J. Muller and A. Ataman, Institut fur Hochfrequenztechnik, Technische Universitat Braunschweig, West Germany

"$GaAs_{1-x}Sb_x$ 1.06 μm Avalanche Photodiodes," F. W. Scholl, K. Nakano, and R. C. Eden, Rockwell International Science Center

"Photosensors on $GaAs_xP_{1-x}$," R. K. Ahrenkiel, F. Moser, T. J. Coburn, and S. L. Lyu, Eastman Kodak Co; and K. V. Vaidyanathan, P. K. Chatterjee, W. V. McLevige, and B. G. Streetman, University of Illinois

Wednesday Morning

Session 22 9-12 am Lincoln Room W

Electro-Optical Devices—Infrared Detectors

Organizer/Chairman: M. Y. Pines

"On-Chip Signal Processing to Overcome IR Detector Nonuniformities," R. E. Eck, Santa Barbara Research Center

"Advances in 2-5 Micrometer (Hg,Cd)Te Photodiodes," T. J. Tredwell, Honeywell Radiation Center

"Epitaxial Heterojunction $InAs_xSb_{1-x}$-InSb Photodiodes," D. H. Pommerrenig, M. Kinoshita, A. Mantzouranis, and T. Oishi, Hamamatsu Corp

"InSb CID Infrared Imaging Devices," J. C. Kim, W. E. Davern, and D. Colangelo, General Electric Co

"Temperature Noise-Limited Pyroelectric Detectors," S. E. Stokowski and N. E. Byer, Martin-Marietta Laboratories

"TGFB and DTGFB Pyroelectric Vidicons," E. H. Stupp and B. Singer, Philips Laboratories; and T. Conklin, Amperex Electronic Corp

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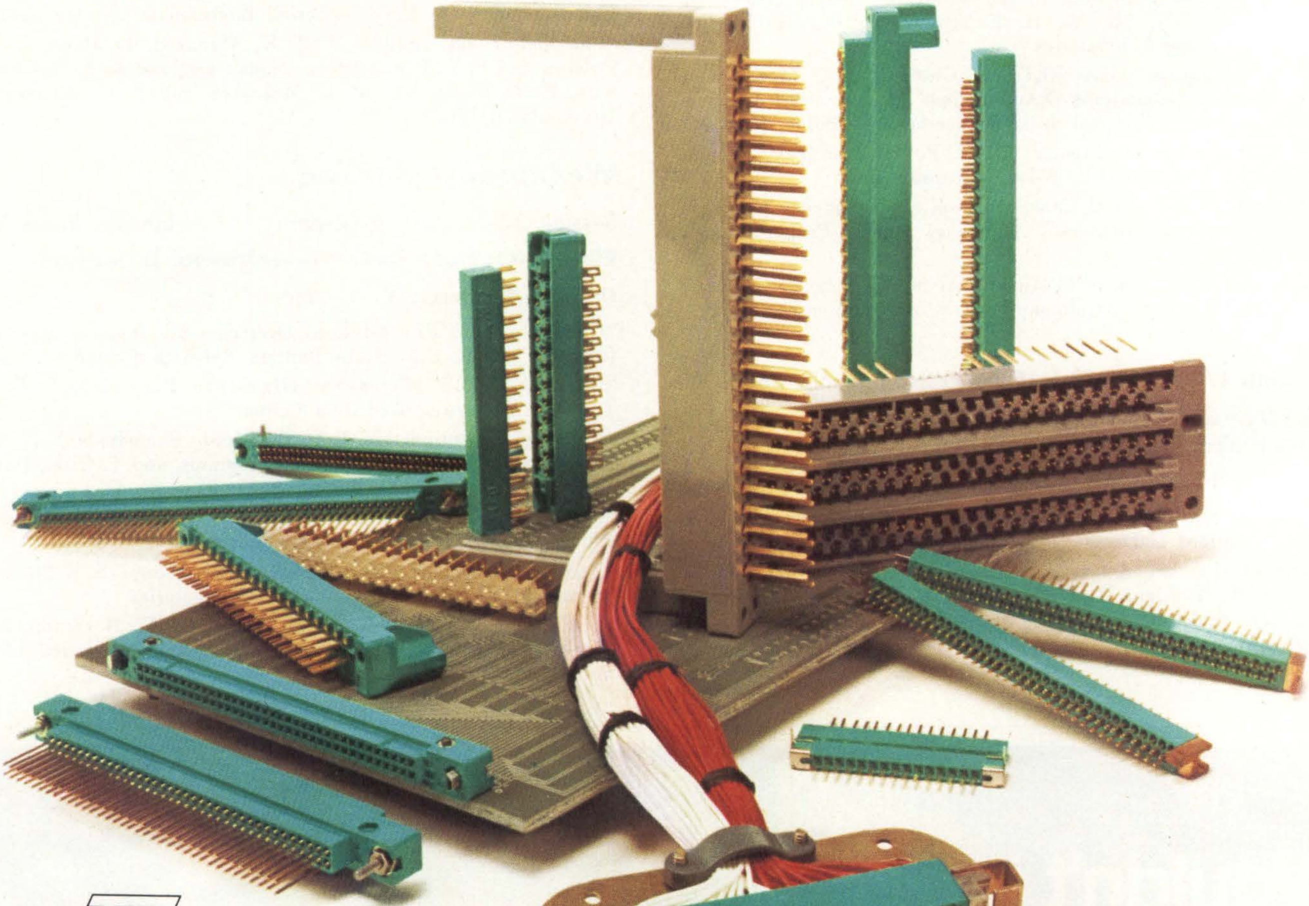

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Wednesday Afternoon

Session 23 2-5:30 pm **Ballroom W**

Solid-State Devices—Short Channel FETs and MOS Type Devices

Organizer: P. J. Salsbury

Chairman: H. C. Nathanson

"Minimization of Gate-Drain Overlap Capacitance in VMOS Structures," I. S. Bhatti, T. J. Rodgers, and J. R. Edwards, American Microsystems, Inc

"Characterization and Modeling of Simultaneously Fabricated DMOS and VMOS Transistors," D. C. D'Avanzo, S. R. Combs, and R. W. Dutton, Stanford University

"Modeling of V-Channel MOS Transistors," B. K. Ahuja and A. R. Boothroyd, Carleton University, Ottawa

"Double-Implanted V MOS," P. Ou-Yang, State University of New York at Stony Brook

"Hot Electron Emission from a Semiconductor Under Low-Level Avalanche Conditions," R. R. Troutman, IBM Corp

"Narrow Channel Effects in Insulated Gate Field Effect Transistors," W. P. Noble and P. E. Cottrell, IBM Corp

"Temperature-Stable MOSFET Reference Voltage Source," W. J. Butler and C. W. Eichelberger, General Electric Co

Session 24 2-5 pm **Ballroom E**

Device Technology—Process Technology II

Organizer/Chairman: R. Edwards

"MOSFETs with Polysilicon Gates Self-Aligned to the Field Isolation and to the Source/Drain Regions," V. L. Rideout and V. J. Silvestri, IBM Watson Research Center

"A Metallization Providing Two Levels of Interconnect for Beam Leaded Silicon Integrated Circuits," W. D. Ryden, E. F. Labuda, and W. van Gelder, Bell Laboratories

"Dielectric Isolation Using Shallow Oxide and Polycrystalline Silicon," J. I. Raffel and S. E. Bernacki, Massachusetts Institute of Technology Lincoln Laboratory

"Preparation of Semiconductor Devices by Ionized-Cluster Beam Deposition and Epitaxy," T. Takagi, I. Yamada, and A. Sasaki, Kyoto University, Japan

"Correlation of Fabrication Process and Electrical Device Parameter Variations," R. W. Dutton, D. A. Divekar, A. G. Gonzales, and S. E. Hansen, Stanford University

"Laser Vaporization of Metal Films—Effect of Optical Interference in Underlying Dielectric Layers," J. C. North, Bell Laboratories

Session 25 2-5:30 pm **Georgetown Room**

Electro-Optical Devices—Displays and LEDs

Organizer: H. Kressel

Chairman: G. B. Stringfellow

"Phenomena Useful for Displays," J. I. Pankove, RCA Laboratories

"The Liquid Crystal Light Valve—A New Display Device," A. D. Jacobson, J. Brinberg, W. P. Bleha, J. D. Margerum, L. J. Miller, and L. M. Fraas, Hughes Research Laboratories

"A Photoconductivity Controlled Liquid Crystal Light Valve," M. H. Wu and N. H. Farhat, The Moore School of Electrical Engineering

"Matrix Display Using Twisted Nematic Liquid Crystal Dynamically Addressed," M. Goscianski and J. Donjon, Laboratoire d'Electronique et de Physique Appliquee, France

"The Fabrication and Performance of LEDs and Detectors from the Ga/In/As Alloy System," A. W. Mabbitt and K. Ahmad, The Plessey Co Ltd, England

"The Design of Optimum High Radiance Double Heterojunction (Al,Ga)As LEDs for Fiber-Optical Communication Systems," J. Zucker and R. B. Lauer, GTE Laboratories

"Increase in Luminous Efficiency With Thinned LEDs," F. Porret, Centre Electronique Horloger S.A., Switzerland □

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μPD2102AL	1K STATIC RAM
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μPD2308	8K Mask ROM
μPD369	UART
μPD758	Seiko Printer Controller
μPB8212	I/O Port
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It is often difficult to estimate quantitatively in advance which computer or compiler would be adequate or cost-effective to solve scientific and engineering research and development problems. This technique simplifies such estimations

Procedure Evaluates Computers For Scientific Applications

Louis Wolin

U. S. Army Materiel Development and Readiness Command
Alexandria, Virginia

To the research scientist and engineer, comparing the performance of various computers is of the highest priority. While he usually does not care about the capability or cleverness of the processing system, he does need to know if a given computer or compiler can solve the problem in a reasonable time and meet mission requirements within cost constraints. From the point-of-view of management, number of runs and cost per run per unit time are significant when new equipment is procured or existing equipment is replaced or augmented. Once management has purchased a particular system, the scientist is limited by maximum capabilities of both the hardware and software operating systems.

In developing a technique for making such comparisons, the U.S. Army Materiel Development and Readiness Command (DARCOM) focused its attention on problems in which the heavy workload is performed by the central processor, while the peripheral workload and input/output (I/O) processing are relatively low. These conditions are typical of real problems in radar, signal processing, missiles, energy, medicine, and other fields, where the high processing workload results from the requirement for computation in real-time, or the extreme complexity of the simulation. In developing this model or applying the technique, design criteria were:

(1) Job or application dependence rather than computer dependence

(2) Present and future scientific computation capabilities to be represented in quantitative terms

Basic Relationships

A processor that satisfies the requirements for a particular line of scientific computation must operate within these guidelines:

$$R_p = O \times P \times S$$

$$B = O_{max}/R_p$$

$$T = N/B$$

where

R_p = Problem requirements in operations per cycle at the highest problem frequency

O = Number of operations per pass through the equations

P = Number of passes per sample

S = Number of samples per problem cycle

B = Processor-limited problem bandwidth

O_{max} = Maximum operations per second of processor

T = Computation time in seconds

N = Problem length in number of cycles of highest frequency

(3) No system to be favored over another

(4) Realism

(5) Testing capability against existing computing systems, as a function of cost per run per unit time

(6) The technique should be tailored to user requirements.

A survey of various Army laboratories showed that problems with over 50 nonlinear simultaneous differential equations were considered overly expensive to solve by digital techniques because of excessive computation time. Reasonable computation for research and development required the solution of no more than 30 to 50 of these equations, with frequency requirements from 1 to 500 Hz.

General Theoretical Considerations

To meet real-time needs and make simulation problems cost-effective under large computational loads, computation speed is an important parameter—particularly in semiphysical simulations, or when system hardware is included in the simulation. The fastest digital machines available today do not meet the frequency requirements of many scientific applications. When the bandwidth of the application problem to be solved is very high, the number of operations per unit time required for each state variable increases as a function of the highest frequency. Since the maximum speed of any processor is limited, computation time must increase to meet the problem's dynamic accuracy requirements. Thus problem bandwidth is very important in the solution of scientific problems, both in real-time and non-real-time simulation; however, it has been neglected by many users and computer manufacturers.

For purposes of this article, problem bandwidth is defined as the highest frequency in hertz present in the problem dynamics, which are represented by a set of differential equations. In nature, these equations are usually nonlinear, but for purposes of analysis, they can usually be approximated by a set of linear differential equations, by considering small perturbations about a reference or equilibrium solution. Roots of these linear equations at any instant, if real, represent exponential dynamic behavior; if complex, they represent oscillations. Both types of roots have units of frequency—that of the corresponding transient oscillation, or of the reciprocal time constant of the corresponding exponential transient. The root with the largest magnitude defines the highest problem frequency, and therefore the bandwidth.

For example, in an aircraft problem with six degrees of freedom, the highest problem frequency typically is approximately 1 Hz, the frequency of the short-period motion. If control-surface dynamics are included in the equations, frequency increases to about 10 Hz, taking into account, for example, helicopter blade dynamics. For a process control plant, the highest frequency may correspond to a time constant of 0.1 s, so that the highest problem frequency (and hence the problem bandwidth) is

$$\frac{1}{0.1} = 10 \text{ radians/s or } \frac{10}{2\pi} = 1.59 \text{ Hz}$$

In digital simulation, where nonlinear differential equations representing the problem dynamics are integrated numerically, accuracy of the result is very sensitive to integration step size. If the latter is too large, accuracy deteriorates and the solution may show instability when the simulated system is actually very stable; if it is too small, the computer word length may impose dynamic range problems (round off errors). If the same integration step size is used throughout the problem (as is usually the case), typically the number of integration steps per cycle of the highest problem frequency lies between 10 and 100, depending on the integration algorithm used.

At each integration step, all algebraic, transcendental, and logical operations needed to evaluate the rate-of-change of each state variable over that step must be computed at least once. Thus, every time the problem bandwidth is doubled, the number of required digital operations per second is doubled if the computation must proceed in real-time; or, if the digital computer was already operating at maximum speed, overall problem solution time is doubled, and real-time operation is lost. Thus problem bandwidth, as defined, can set speed requirements for real-time digital simulation. Conversely, for a given digital computer in non-real-time, bandwidth determines time required for the simulation run and hence the cost per run.

However, for some types of simulation, problem bandwidth alone may not set speed requirements. One or more time-varying input variable to the simulation may have significant power content at frequencies above the problem bandwidth. For example, if the simulation consists of low pass filtering of input data, filter cutoff is the highest problem frequency. If integrator step size is based on this frequency, resulting sample frequency for the input data may be inadequate for certain power frequencies. According to a well-known theorem, sampling frequency must be at least twice the highest problem frequency; otherwise, frequencies in the input signal that are more than one-half the input sample frequency are converted erroneously into frequencies less than one-half the sample frequency. This effect, known as "aliasing," can cause large errors if not recognized and corrected. Correction requires either a higher input sample rate or prefiltering the input signals; the higher rate requires either higher digital processor speeds or more processor time.

Despite these considerations, the proposed technique is based strictly on the problem bandwidth. The quantitative method of comparing computer systems described here does not assume that one system is superior to the other. It shows how to predict in advance which computer is more cost-effective or more likely to solve the required application according to design specifications. In comparing computers, the physics of the problem and the input and output signals must be considered.

TABLE 1

Typical Scientific Problems

Organization	Applications	Millions of Operations/s	Number of Differential Equations	Bandwidth (Hz)	Computer Time Analog	Computer Time Digital
AEC	Reactor core dynamics	80	200	50	10 min. (EAI 8900)	200 min. (IBM 360/75)
Army	Gun stabilization/ control (500 runs/ vehicle)	10	50	200	0.83 min. (EAI 231R)	20 min. (IBM 360/44)
Army	Cross country vehicle (20 runs/ vehicle)	4	30	500	1 min. (EAI 231R)	15 min. (IBM 360/44)
Army	Helicopter flight simulation (500 runs/aircraft)	43	250	50	—	1 hr (IBM 360/65)
Hughes Aircraft	Air-to-air homing missiles (400 runs/day)	36	60	1000	20 s (EAI 680)	600 s (Sigma 8)
Navy	Real-time torpedo launch simulation	1	10	10	10 min. (EAI 8800)	—
Beech Aircraft	Missile dynamics	1	35	20	1 min. (EAI 600)	12 min. (Cyber 72)
U of Michigan	Electrohydraulic control system	10	8	60	1.5 min. (AD/1130)	1012 min. (IBM 1130)
Army/Martin-Marietta	Missile trajectory (100,000 runs/missile)	8	53	50	100 s (EAI 8800)	334 s (IBM 370/168)
Air Force/ Martin-Marietta	Missile trajectory (4000 runs/missile)	8	—	50	5 min. (EAI 8800)	200 min. (EAI 8400)
Army/Martin-Marietta	Missile stability and control (90,000 runs/missile)	2	31	60	10 s (EAI 8800)	100 s (EAI 8400)
DCA/Martin-Marietta	Communication receiver simulation (10,000 runs)	150	32	45	5 min. (EAI 8800)	246 min. (U 1108)
Martin-Marietta	Voice intelligibility study (900 runs)	64	46	35	22 min. (EAI 8800)	702 min. (Xerox)
Martin-Marietta	Economic system model (100 runs)	230	14	5	0.02 s (EAI 8800)	2 s (IBM 370/168)
Martin-Marietta	Autovon model (18 runs)	10	—	50	1.1 min. (EAI 8800(3))	360 min. (IBM 370/155)
Toyota	Automobile dynamics (1000 runs/design)	7	29	10	5 s (EAI 600)	5400 s (IBM 360/65)

Scientific Mix to Compare Computers

One technique for comparing computer performance is the use of a scientific mix of instructions. It is based on the assumption that a quantitative measure may be derived from the mathematical representation of the system to be simulated and the performance characteristics of the computer, and used as an estimate of computation time to perform the simulation. It assumes that mathematical equations for the simulation are known and will be evaluated by a digital computer that operates in accordance with advertised or measured performance specifications. These mathematical equations are translated into a total count of digital computer operations per second, which is then used to obtain total computation time. To reflect the experi-

TABLE 2

WSP Scientific Mix

Mathematical Function	Add	Mult	Load	Store	Compare	Normalized Digital Operations Per Function	Total Functions Per Mix	Total Normalized Digital Operations/ WSP Mix
Weights	1	3	1	1	1			
Summation $Z = A_1X_1 + A_2X_2 + A_3X_3$	2	3	3	3		17	136	2312
Multiplication $Z = XY$		1	1	1		5	102	510
Comparison $X_1 \geq X_2$	1		2	2	3	8	68	544
Arbitrary Function Generation $F(x) = (1-\Delta x)F_1 + \Delta xF_2$, $x = (x-x_i)/(x_{i+1} - x_i)$	4	3	4	5	3*	28	68	1904
Fixed Function Generation $F(x) = \sum_{0}^{n} A_i x^i$	6	6	1	1		26	68	1768
Runge-Kutta 4-pt Integration	10	5	11	11	3**	60	102	1530***
							TOTAL	8568

*Plus 10% overhead
**Plus 20% overhead
*** 25% of 60 x 102

mental nature of the simulations conducted by the U.S. Army Laboratories, arbitrary and fixed function generators were included in the mix. Finally, all or part of the estimate was validated by actually running the problem on the computer system and comparing estimated and actual times.

The method is problem-dependent rather than computer-dependent since the engineer or scientist reduces the equations directly to operations per second. For example, the equation $w = xy/z$ requires one multiplication, one division, three stores, and one load to be evaluated on a digital computer. Although various computers may solve the problem differently, the mix serves as a baseline for comparing them, because it depends upon basic mathematical operations and the computer characteristics in performing these operations. The mix is intended to be used both in applications that tax present large computers, and in systems of minicomputers.

This measure of performance is useful when new computer systems are selected and evaluated, or when existing systems are replaced or augmented. It can also project future requirements by predicting which problems require too much time to be solved effectively on present-day large digital computers. For example, the U.S. Army Air Mobility Research and Development Laboratories encounter very large problems in the simulation of helicopters, while analyzing competitive designs. Simulation of these applications requires approximately 250 first-order simultaneous nonlinear differential equations and requires up to four hours on an IBM 360/65 to evaluate a few minutes of real-time performance. Other large problems are equally time-consuming (Table 1).

The technique is best explained by a specific example (Table 2), which is based on a representative simulation of a large missile. Developed by DARCOM, it is called the Wolin-Saucier-Peak (WSP) Scientific Mix. It includes 102 simultaneous nonlinear first-order differential equations. Evaluation of these equations requires summation, multiplication, Boolean comparison, arbitrary function generation, and single fixed function generation in terms of a power series. These five operations, along with the fourth-order Runge-Kutta integration algorithm by which each first-order equation is integrated over one time step, are listed in the first column of Table 2. In the next column, these mathematical operations are reduced to equiva-

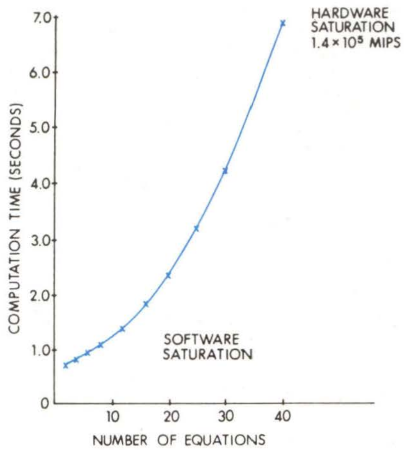

Fig. 1 Validation. Computation time for various sets of simultaneous differential equations was predicted according to the technique to lie along this curve. Observed time was very nearly the same; it lay, in fact slightly above this curve as a result of software inefficiencies

lent digital operations. For example, the summation function $A_1X_1 + A_2X_2 + A_3X_3$ requires a minimum of two additions, three multiplications, three loads, and three stores to evaluate. Each of these operations has a weighting factor, normalized with respect to the execution time of an add operation for the specified computer. With these weighting factors, differences in digital computers can be adjusted. In this example, weighting factors are all 1 except for multiplication, which is assumed to require the equivalent of three additions to execute. Sum of the digital operations, each multiplied by its weighting factor, is the number of static digital operations for the corresponding mathematical operation; this number, for a summation, is 17 (third column). Missile simulation requires 136 of these summations (fourth column), so that the total count of normalized operations is the product of the number of digital operations per function and the number of times the function occurs in the simulation. This is 17 x 136 for the summation, or 2312 (fifth column).

Similarly, total normalized digital operations are calculated for the other functions in the simulation. The result in column 5 is the total number of digital operations required to evaluate the corresponding mathematical function in column 1 at a single value of the independent variable—that is, for a single sample representing a brief interval of time. However, for the Runge-Kutta integration, the table entry is the previously mentioned product divided by four, because four passes are necessary at each sample point. These passes represent, in effect, a partial evaluation at the next three sample points as well as the present one, because the algorithm is recursive. Taking this into account, the total of all entries in column 5 is 8568, the number of digital operations required to run the whole simulation for a single value of the independent variable—that is, for a single sample.

Because four passes are made per sample, and because 20 samples are made for each cycle of the problem frequency, which is 1 kHz, the number of equivalent digital operations per second of missile time (not necessarily per second of real-time) is 4 x 8568 x 20 x 1000 = 685,440,000. However, if the mix assumes a problem frequency of 10 Hz, the simulation is slowed down by a factor of 100 from this rate, or 6,854,400 operations/s. Thus the simulation runs at 1/100 real-time.

Empirical relationships can be developed from experience relating the number of operations per second to number of simultaneous differential equations and bandwidth of the highest frequency. If all other parameters are fixed, and only the frequency varies, number of operations per second is proportional to bandwidth. Such an estimate does not take into consideration software efficiency or computer overhead; however, as a figure of merit it estimates the best performance possible.

Validation of the Technique

The technique can optimize the selection of a computer for any given computation requirements, either to choose new computing systems to meet present or future needs, or to predict in advance the most cost-effective technique or fastest computation time for large and small scientific problems.

Martin-Marietta Corp verified the technique by utilizing experience gained over many years in simulating missiles. In applying the technique with debugged production programs repeated many times, Martin-Marietta was requested to answer two questions without imposing an additional workload on its facility.

(1) Given two computers, the IBM 370/168 and the EAI 8400, can the computation time of each be predicted in advance? Predicted execution times on both computers were within 10% of actual computation time.

(2) Given a large computer, such as the IBM 370/168, and a choice of several compilers written to run in various memory capacities, which compiler is best suited for a program to solve the equation of motion of a rigid body in a single plane? Although these

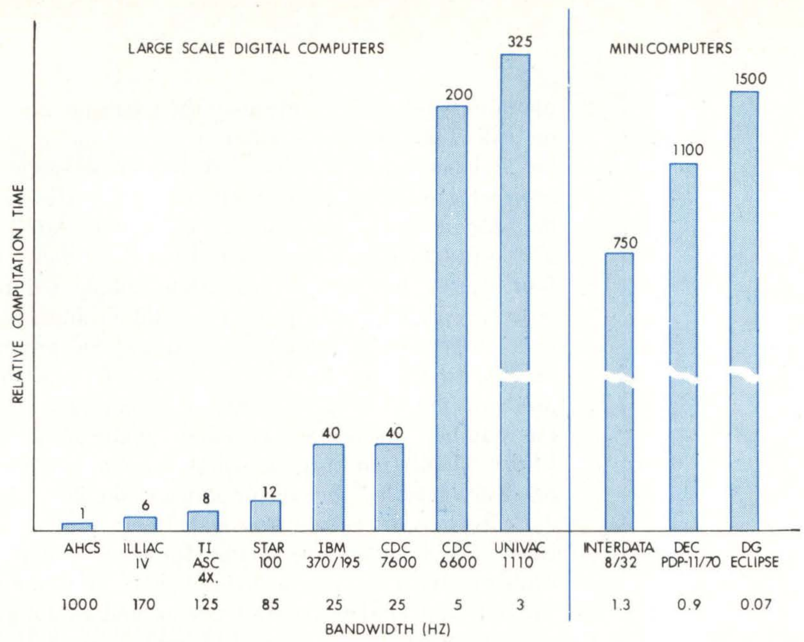

Fig. 2 Comparison based on computer speed. Using a proposed hybrid design as a standard, and executing a particular problem that required 600,000 operations per problem cycle, various commercially available systems were found to require these relative computation times. Standard design could execute 100,000 operations/s and simulate a 1-kHz system in real-time; numbers across bottom of chart show relative real-time speeds of other computers evaluated

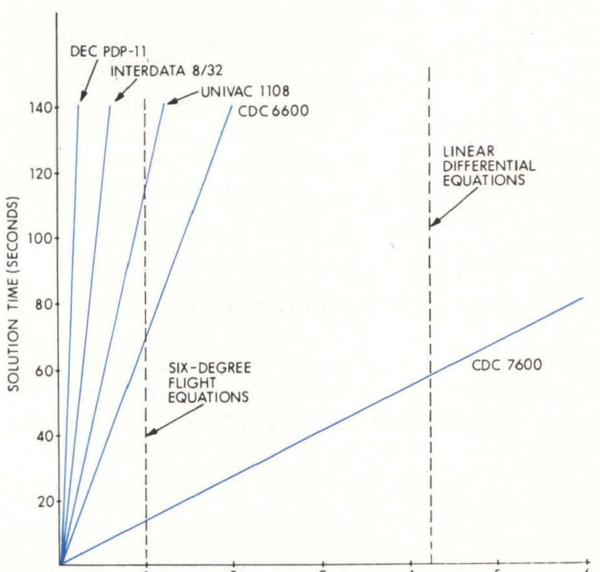

Fig. 3 Comparison based on problem size. Time required to solve a problem is proportional to problem complexity measured in the number of operations per second that would be required to solve it in real-time. Relationship applies even to parallel-processor systems, but is clearly impractical for small computers. Proposed hybrid design, standard for the comparison, would be represented by a horizontal line just above the axis; increasing complexity calls for more hybrid modules that keep the solution time constant

results were less definitive than the first, because all compilers ran in about the same time, within 4%, predicted compilation time was reasonably close to the time actually required.

Further validation of the method was provided by the University of Massachusetts, in predicting the computation time to solve linear simultaneous differential equations on a Control Data Corp CYBER 74 computer using CSSL/RSSL software. In this test, the highest frequency was 1 kHz, and the Runge-Kutta algorithm was used with each equation over one time step. Eight simultaneous differential equations were solved in 1 s, and 40 equations in approximately 7 s (Fig. 1). Observed computation times were slightly longer than predicted because of inefficiencies in the RSSL software.

Various government and industrial laboratories have further verified the technique on digital and hybrid computers.

Applying the Technique

Another representative missile simulation like the one used earlier required roughly 30,000 digital operations per integration step. Assuming, as before, 20 steps/cycle of the highest problem frequency, this comes out to 600,000 digital operations/cycle of the highest problem frequency. A proposed large hybrid system could handle problem frequencies of up to 1 kHz without significant accuracy deterioration. This is its bandwidth, corresponding to 1000 x 600,000 = 600M operations/s.

Another way of comparing computers is to constrain them to real-time operations. This approach assumes that they run at the maximum possible speed consistent with acceptable accuracy, since this yields the lowest cost per solution. For various digital computers (Fig. 2) the range of problem bandwidths varies from

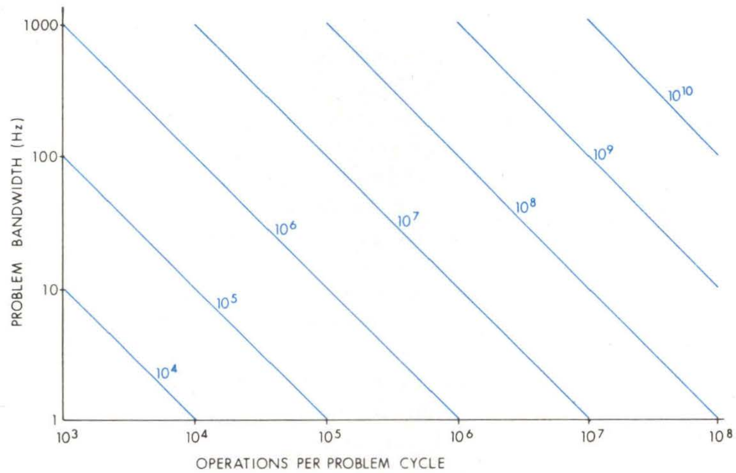

Fig. 4 Nomograph 1. Operations per problem cycle (horizontal axis) and number of problem cycles per second (vertical axis) determine the number of operations per second (curve and figures in color) required of the processor that will solve the problem

less than 1 Hz for some minicomputers to roughly 170 Hz for today's largest computers when applied to simulations that require 600M operations/s. For the proposed hybrid system just mentioned, maximum problem frequency content may fall anywhere between 10 Hz and 1 kHz. For digital computers the maximum practical interval of numerical integration corresponds, as in the example cited, to about 20 steps/cycle of the highest problem frequency.

Maximum number of operations per second for a number of scientific digital computers was estimated and verified by consulting with various laboratories and computer manufacturers throughout the country. In each case dividing this number by 600,000 gives the actual maximum problem frequency which the given computer can handle and still solve the missile simulation problem. This is defined as the computer bandwidth.

Since digital computers operate serially, problem solution time grows linearly with problem size (Fig. 3). Even in the case of digital computers using a number of parallel processors, such as ILLIAC IV, maximum number of operations per second is achieved when all processors operate simultaneously at full speed, so that the linear relationship holds.

Computer Selection

The technique is based essentially on two nomographs (Figs. 4 and 5). Using the first, the computer with the required maximum operations per second can be selected from the problem requirement in operations per problem cycle (abscissa) and problem bandwidth (ordinate). Since operations per second equals operations per cycle multiplied by cycles per second, the curves in Fig. 4 are hyperbolas of the form $xy = k$; they appear as straight lines because the scales on

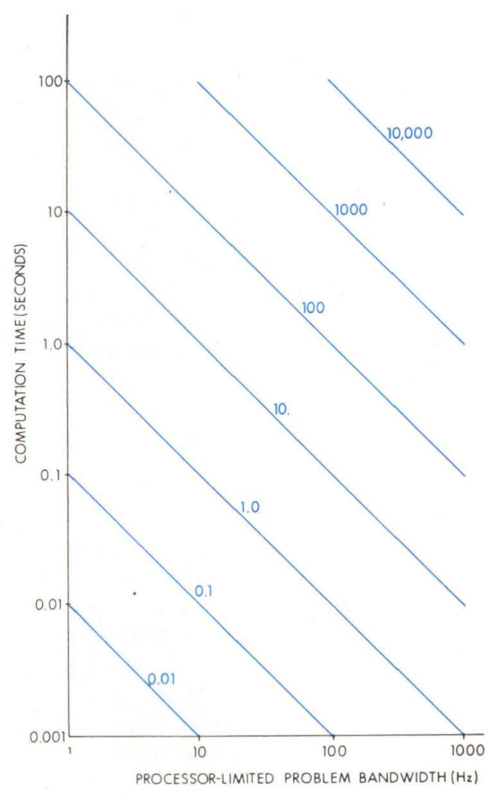

Fig. 5 Nomograph 2. Number determined in Fig. 4, divided by problem requirements in operations per cycle, gives the processor-limited problem bandwidth, shown along the horizontal axis. This number, and the actual problem bandwidth (curves and figures in color) provide an estimate of the length of time required to solve the problem

TABLE 3

Typical Computer Speeds

Computer	Max Operations/s (x 10^6)
ILLIAC IV	100
Texas Instruments (ASC 4^x)	75
CDC STAR-100	15
IBM 370/195	15
CDC 7600	15
CRAY	80
CDC 6600	3
UNIVAC 1110	1.85
Interdata 8/32	0.8
DEC PDP-11/70	0.55

both axes are logarithmic. The second nomograph (Fig. 5) relates computation time in seconds to the number of problem cycles at the highest problem frequency and the processor bandwidth in hertz. These curves are also hyperbolas, generated from a different basis but the same relationship as those in Fig. 4. This technique is particularly useful and has a high probability of success when problems or simulations can be expressed quantitatively by equations or number of equivalent computer operations. Its validity depends upon problem definition, accuracy required, and problem bandwidth. Corrections to the predicted results can be made easily by running a scaled-down version of the problem on various computers.

Illustration of Technique

A practical problem illustrates the method. Assume that a simulation requires 10^5 operations/problem cycle as determined by the maximum number of equations or operations required. For this problem, the best computer can be found from Fig. 4, assuming that the problem bandwidth is 10 Hz. At the point 10^5 (problem requirement) on the abscissa draw a vertical line. At the point 10 Hz (problem bandwidth) on the ordinate draw a horizontal line. The two lines meet on the diagonal line labeled 10^6. This means that a computer capable of 10^6 operations/s is required. At least two computers meet this requirement (Table 3) and are therefore candidates for the job; they are a CDC 6600 or a UNIVAC 1110.

When a computer has been selected, computation time for solving the problem can be predicted from Fig. 5. It depends on the processor-limited problem bandwidth—that is, the highest problem frequency that a given processor can handle in real-time, which may not be the same as the actual problem bandwidth. This processor-limited problem bandwidth is the quotient of the maximum processor operations per second, as determined from Fig. 4, divided by the problem requirements in operations per cycle. For example, from the nomograph, a machine with a processor-limited problem bandwidth of 10 Hz requires 1 s to run a program with an actual problem bandwidth of 10 Hz. Similarly, if another machine with a processor-limited problem bandwidth of 1 Hz were selected, computation time for the same problem would be 10 s. Since maximum capability of most computers can be expressed in operations per second, a family of curves like those in Fig. 4 but with different slopes and intercepts can be developed for new computers when theoretical and measured data become available. From such curves, a processor can be selected to give the optimum computation time and the minimum cost—keeping in mind the assumptions that the computer is not saturated when processing the problem and that architecture, software, operating system, and compiler are performing in accordance with known specifications.

Conclusions

For problems requiring 600,000 operations/cycle of the highest frequency, effective bandwidth of present-day large-scale digital computers is less than 170 Hz. However, from a survey of the scientific applications of various laboratories, there are real-time requirements for computers which can process problem bandwidths of at least 10 kHz and approach a performance capability of 600 x 10^6 operations/s—three orders of magnitude faster than available computers. The technique described here is useful in predicting the optimum computer system and an approximate required solution time for a given problem, and in selecting a computer system to meet present or future computational needs for scientific applications.

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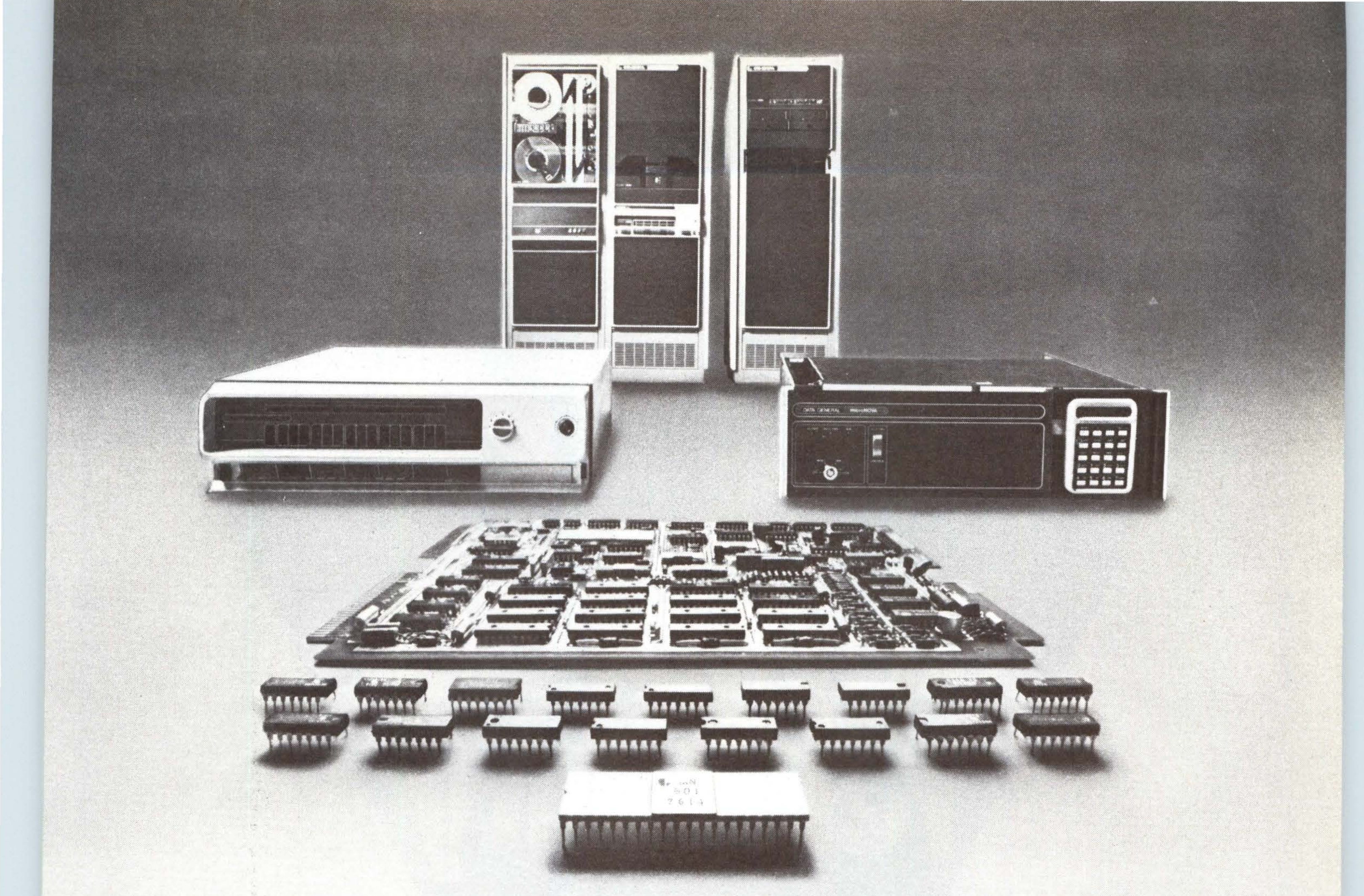
Louis Wolin, currently an operational research analyst, has worked in digital communications, digital and analog computers, and simulation. He holds a BS in mathematics and physics and an MS in education from the College of the City of New York, a BS in electrical engineering from Ohio State University, and an MS in electrical engineering from the University of Pennsylvania.



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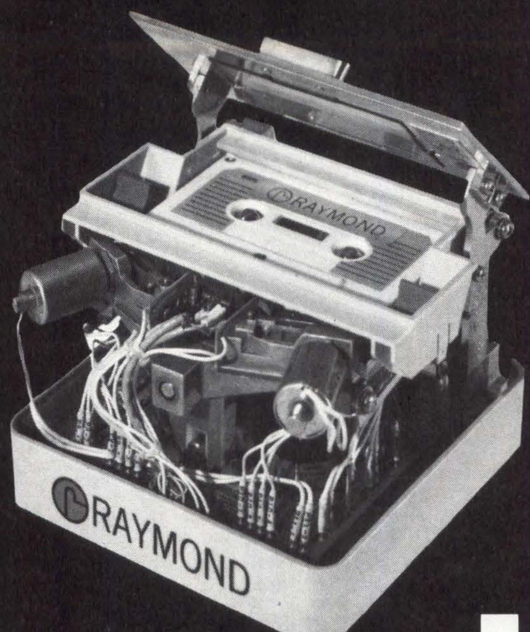

As large-scale integrated circuits add more and more capability, their usefulness to terminal designers increases, resulting in more articulate or cheaper terminals or both

Impact of LSI On Terminal Architecture

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Designers have a responsibility to assess the value of arising technologies and to propose *revolutionary* products which satisfy user needs rather than user desires. This obligation contrasts sharply with the way most terminal designs are created—winding up at the engineer's bench after a series of customer inputs have been filtered by the marketing department. Marketeers usually want *evolutionary* products that are extensions of the existing product line: a little faster, cheaper, and with a few new functions.

Large-scale integrated (LSI) circuit technology offers promise of a breakthrough in product design, and deserves careful consideration in planning its introduction into terminal designs. It offers some universal advantages, independent of the details of its use. One of these is reduced lifetime cost, resulting largely from reduced downtime and faster maintenance. A lower component count and accompanying reduction in circuit boards, connectors, and cables present less opportunity for failure.

Another advantage is the opportunity for built-in reliability. Lower cost per function permits redundancy and error correction, reducing failure incidence. Addition of diagnostic facilities also promises lower cost to repair. Fewer failures and faster repairs increase the system's availability to the user throughout its life. LSI also reduces power dissipation. Smaller power supplies, less heat, and fewer fans promise smaller, quieter, and lighter terminals.

Unfortunately, LSI does not have much effect on purchase price reductions, which are more limited by packaging, mechanical considerations, software, and marketing costs than by semiconductor devices.

LSI Functions and User Needs

LSI also has advantages in specific terminal functions, which include data input from keyboard or digitizer; display on cathode-ray tube (CRT) or printer; secondary storage on cassette or diskette; communication with mainframes or other terminals; and data manipulation. Onto this set of terminal functions must be mapped a series of requirements that represents the set of user needs, which includes data entry, data retrieval, editing, display, and computation. The degree of fit between these two sets determines the effectiveness of the terminal in a particular application.

Prime concern of the design engineer is how to implement the functions most effectively; however, for the user terminal functions are but a means to an end. He is relatively indifferent to their implementation. The designer must not lose sight of the user forest as he looks at the functional trees.

When implementing the desired feature set, the designer must choose between the flexibility of a general-purpose device and the performance of a specialized device. LSI microprocessors offer the advantage of changing the feature set without modifying the hardware. This permits a terminal to be designed for usefulness in more than one application by changing the control program. The result amortizes hardware engineering expense over a larger volume and achieves economy of scale in manufacturing. For example, a single alphanumeric CRT and associated hardware might be applied both to a data retrieval application and to another application utilizing "fill-in" from displays.

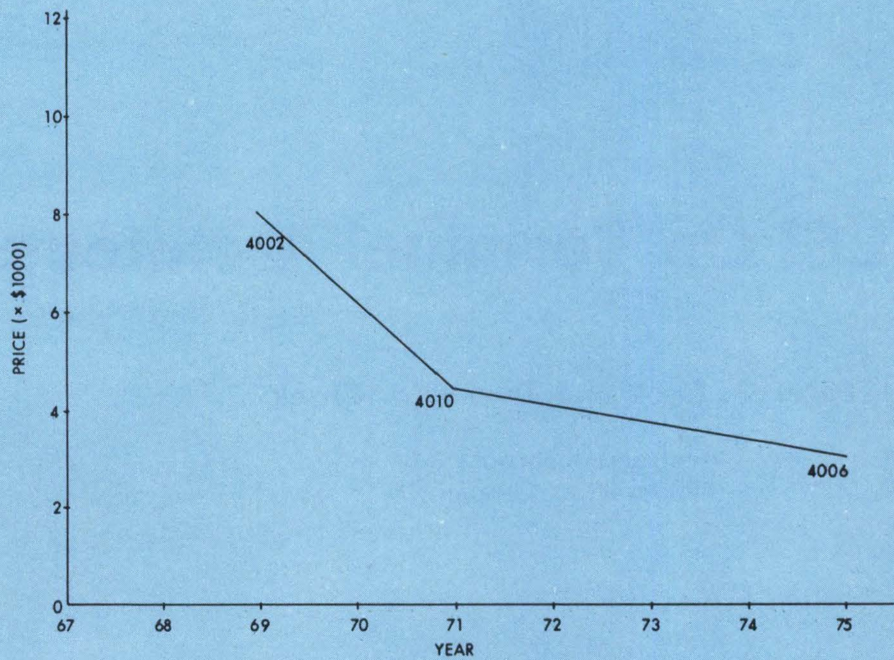

Fig. 1 Technology and cost. One way to take advantage of improved technology is to maintain performance and reduce prices. While retaining the same capacity for data, prices of Tektronix 4002, 4010, and 4006 graphic terminals have dropped successively lower through the years

Unfortunately, circuits as complex as a microprocessor are most easily implemented in metal-oxide semiconductor (MOS) and related technologies, which are relatively slow. Some terminal functions, such as error checking of high speed communication lines, may exceed the capability of many processors. To stay with the general-purpose approach requires use of a faster but more expensive microprocessor, perhaps a bipolar implementation. Use of multiple microprocessors is an alternative, but brings problems of multiprocessor architecture. On the other hand, the special-purpose approach requires random logic to implement the precise function set required. If properly done, this last approach optimizes performance.

A feasible intermediate approach uses a microprocessor at the heart of the system, and surrounds it with specialized medium-scale integrated (MSI) or LSI circuits for repetitive functions or those working with special signal levels. As needs have been defined, a number of special-purpose devices have appeared. Semiconductor distributors stock many of the common terminal functions. These include: universal asynchronous receiver-transmitters (UARTs), keyboard scanners, character generators, power supply regulators, and digital-to-analog converters. Some special functions may be implemented with standard microprocessors dedicated to one task. This avoids the problems of generalized multiprocessor systems.

Networking

The most far-reaching consequence of LSI's effect on terminals is in how they will be used in networks. The typical computer network consists of a large central computer, a variety of local high performance peripherals, such as printers and mass storage units, and a large number of remote terminals connected by telephone lines. The network exists primarily to allow remote terminal users to access the computer's processing power, and to share the central data base and the system peripheral devices. However, such networks, in attempting to provide "real-time" response, incur a high system overhead that raises costs and lowers performance. They are also subject to relatively high communications costs, which do not appear to be falling as fast as other system costs.

If present trends continue, future terminal processing power and memory capacity will be adequate for many processing tasks now being imposed on the host

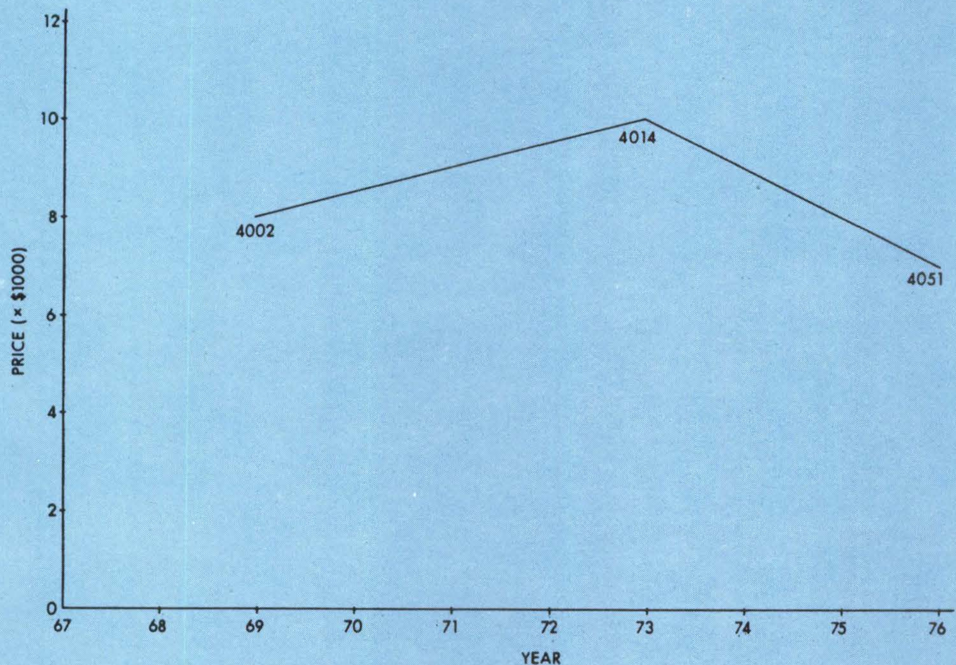

Fig. 2 Technology and performance. Another way to use technology is to increase performance and maintain a steady price. Thus terminal art has progressed from the early 4002 to the large screen 4014; and then to the 4051, which includes its own computer and cartridge tape drive

computer. This is particularly true of input and editing tasks. As a result, the host computer system can be optimized to run larger programs with less concern for real-time response, and will, therefore, suffer less from overhead. At the same time, the terminal user will have improved response, since much processing will be local; and communication costs will be lower, as fewer messages are transmitted back and forth.

However, since the need for shared data bases, shared specialized peripherals, and backup computation power will continue, networks will continue to exist. Paradoxically, instead of terminals supplying data and programs to the host computer, it may be more common for the host to feed data and programs to be run on the terminal.

This process will not occur overnight, but the trend should be steady.

LSI and Computation

Microprocessors are falling even faster in price than memory chips, while architectures, speeds, and instruction sets are becoming more powerful. Machines, which began modestly as 4-bit "number gummers," are now available with 8-, 12-, or 16-bit words, and some are real "number crunchers." Introduction of bipolar processor chip sets has opened yet another dimension of speed and flexibility.

At first thought, it would appear that terminal computation would not require very high performance. This would be true if LSI were used merely to implement the traditional terminal functions. However, between designers' imagination and customer wishes, terminal processing requirements can be demanding. Even now, many applications require 8K, 16K, or even 32K bytes of control memory. Although the typical data word is a 7- or 8-bit character, any operation requiring much data translation on the display screen will require manipulation of 16-bit address pointers and, therefore, 16-bit arithmetic. Meanwhile, graphic terminals have almost unbounded needs for computation. While simple 2-dimensional images require little processing, such tasks as clipping a picture to fit on the screen, or performing real-time 3D rotation, can put severe demands on a system.

Some important issues have not yet been resolved. For example, how much programming power will the individual user want? and what will be the division of responsibilities between vendor and customer?

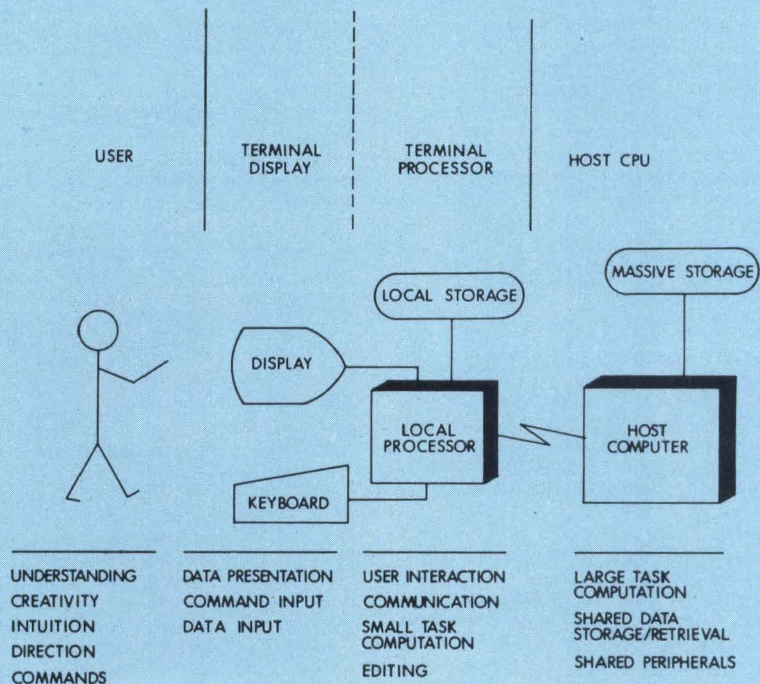

Fig. 3 Division of system tasks. Each level in any terminal application can be dedicated to the particular things it does most economically

Data Input

The standard typewriter keyboard is likely to remain the most common data entry device for some time. LSI has its impact here by allowing keyboards to be configured in unlimited ways. Traditionally, each key on a keyboard is assigned a specific code, which is transmitted to the computer when the key is depressed. With LSI, these key codes can initiate separate control routines, which, for example, might alter key codes according to some algorithm. By this means, key-cap positions could be moved freely; changing the "mapping table" would make the proper key codes follow the keys.

Similarly, normal and shifted key codes can be freely paired rather than restricted by coding conventions. Individual keys can be tagged to repeat their codes as long as they are held down, while others are nonrepeating. LSI scanning techniques also make protection against "N-key roll-over" easy—that is, avoiding incorrect signals when two or more keys are depressed simultaneously. Finally, special function keys can be programmed to perform whole sequences of operations and even reprogrammed by different users for different functions. This flexibility means that the keyboard can be more readily tailored to the user's needs and thus should allow faster and more accurate data entry.

As has been well recognized, errors are most effectively corrected at the source. Local software can apply a variety of tests to data input, verifying consistency, range, and so on. When the terminal itself performs these checks, it avoids burdening the host computer and communication lines.

Data Display

Certainly during the next five years the CRT will be the dominant display component for terminals. LSI will help improve performance and lower costs of CRT-based terminals by taking over or aiding timing generation, picture geometry correction, digital-to-analog signal conversion, and other functions. Generally, these functions will be implemented using analog and combined analog/digital LSI devices. Although the term LSI often implies a monolithic structure, some of these combined devices will be hybrids built with thin-film technology. In some terminals LSI will be used to build units with larger CRTs of higher resolution, which therefore can show larger numbers of characters that are more legible and more attractive.

With low cost semiconductor memory, inexpensive graphic terminals using refreshed CRTs will be feasible. However, technology improvements will also make storage CRTs and plasma panels cheaper, and these devices will compete extensively in some applications.

For several important segments of the graphic terminal market—such as computer aided design, which requires large and complex displays—the storage CRT will reign supreme. For screens more than 30 cm across and images with over 20,000 vectors, the storage CRT has not only a very large equivalent memory space, but also image addressability, small spot size, and resolution much higher than all but the most expensive refresh CRTs.

LSI will eventually solve addressing, memory, and driving problems in emerging display technologies, such as liquid crystals, by incorporating the LSI circuits directly into the display unit. However, much work remains to make such devices economically practical. In particular, in the short run magnetic bubble memories, charge-coupled devices (CCD), and electron-beam-addressable memories appear to be inferior to MOS random-access memory (RAM) both in performance characteristics and potential low system cost for general-purpose terminal usage. In terminal applications, the organizational flexibility of MOS RAM makes it much more attractive than serial memory approaches or techniques requiring complex support circuits.

LSI and Communications

One of the major reasons for incorporating intelligence in terminals is to reduce communication cost. The word "intelligence" implies more complete message correction and verification before transmission, which reduces the need for repeated data transfers and improves transmission accuracy. The term also includes methods of polling, delayed data transmission, and elaborate networking techniques, permitting more efficient allocation of communication resources.

Special-purpose LSI is especially important in communication because the signal levels of some channels differ from standard logic levels. Also, because some communications tasks require very specialized processing, optimized circuit architecture is needed for efficient performance.

LSI and Peripherals

The impact of LSI on peripheral equipment for terminals has been pronounced. One of the characteristics of the market is that terminals are usually bought to match the terminal as closely as possible to the job. This means that the typical user buys units without much excess capability. As the need arises for peripheral devices, such as magnetic memories or printers, the original system can be very difficult to expand. However, by building LSI processors and memory into each peripheral device, the control burden imposed on the terminal is much lighter. Transferring data in blocks can reduce timing constraints. In addition, some specialized data manipulation tasks such as format conversion and signal amplification can be assigned to LSI chips specifically designed for them.

Summary

LSI technology offers an opportunity to reduce cost and increase reliability in terminals. The engineer will have to trade-off the flexibility of a general-purpose approach against the performance of special-purpose modules. Sales volume and application needs weigh heavily in the decision. Designers must also watch for opportunities for a real breakthrough. A reduction of terminal selling price by a factor of 10 would benefit the entire computer industry.

Presently engineering manager for the Information Display Systems Div of Tektronix, Peter G. Cook has been involved in data processing management, software development, and terminal design. He received a BA degree in physics from Williams College, and has done graduate work at Syracuse University and North Carolina State University.

Thomas B. Cheek is a senior engineer with the Information Display Group of Tektronix. His experience in design of low cost, high performance graphic display systems includes early work on direct-view storage, raster-scan, and calligraphic-refreshed CRTs. He holds BSEE and MSEE degrees from Massachusetts Institute of Technology.

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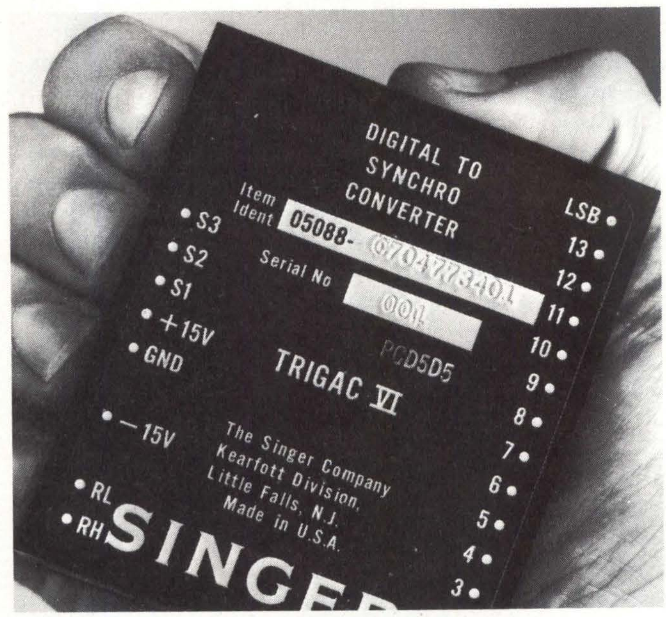

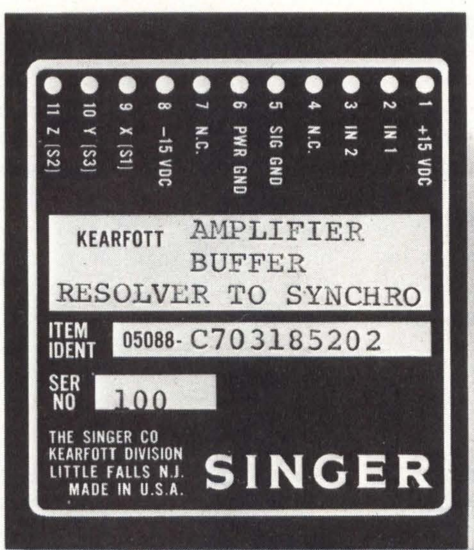

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Getting the most out of microprocessors in any application requires the system to be designed for a broad range of applications, with flexibility and versatility built in

Challenges in Microprocessor System Design

Tom Jones and Peter Thomas

Intel Corporation
Memory Systems Division
Sunnyvale, California

Today's electronics industry enjoys a sense of freedom and growth unimagined only a few years ago. The advent of the microprocessor has enabled manufacturers in the industry to use relatively simple, but powerful, microprocessor cards containing no more than 10 to 20 large-scale integrated circuits, not only for one particular product, but for entire lines of products. Product design has thus become largely a matter of system reconfiguration, which has, in turn, become a matter of redesigning system software and shuffling peripheral subsystems, much the same as with minicomputers.

Although these generalized microprocessor cards could well revolutionize product design, because of the ease with which the resulting product can be modified, designing microcomputer systems that allow flexibility and versatility is subject to numerous considerations. Design of generalized microcomputer systems involves many facets of microcomputer hardware design, and poses numerous questions that should be faced by any designer embarking on such a design.

Equipment manufacturers have discovered the impressive cost-effectiveness of microcomputers. Today, manufacturers are finding that the utilization of generalized microcomputers, rather than specialized logic controllers, can have a direct bearing on their profitability. These boards bring about reduced costs of development, production control, manufacturing, and field maintenance for diverse end-products.

Microcomputer Development

Two previous difficulties in adapting microcomputer systems have been generation of microcomputer software and integration and debugging of this software with the microcomputer hardware. However, modern microcomputer development systems, especially adapted to perform these tasks, have essentially removed those difficulties. They are effective because they can control multiple development resources and allow users to simultaneously develop and debug software and hardware from the beginning of the design cycle.

These development systems support numerous peripheral devices, which make system software generation quick and efficient, and allow software and hardware system testing and debugging to be carried out. Because of their architecture, most modern microcomputer development systems check out integrated software and hardware with either complete hardware emulation or selective in-circuit emulation.

Today's microcomputer designers are at the confluence of two traditionally separate technologies. Neither hardware nor software design can be carried out without full knowledge of the capabilities and constraints of the other discipline. Using currently available development tools, digital designers can do most of their design tasks in software. Thus, reconfiguring a microcomputer system is totally a matter of reprogramming, as long as the microcomputer hardware has been designed to allow for the required changes.

Hardware Considerations

Now that the microprocessor has made the transition from laboratory novelty to production line workhorse, microcomputer system design techniques are known and widely used. Slight variations to these techniques can improve versatility of the microprocessor unit (MPU) hardware and thereby increase the hardware's utilization.

First step in "designing out" obsolescence of a new microcomputer system is not merely to concentrate on the primary system, but also to consider any possible options to be offered with it. In addition to these primary and secondary considerations, designers should keep in mind potential uses for their MPU in future products. Knowing future requirements in general, the design team will know in which areas the microcomputer hardware will probably change. This information also will serve as an important constraint when selecting the microprocessor family.

The list of parameters on which the selection of a microprocessor family is based may be quite lengthy, and may differ for each application. However, one of the most important characteristics on which the selection should be based is the ease of expansion of memory and input/output (I/O) ports. Another important factor is that the components making up the microprocessor family should be reconfigurable on the board with only software modifications.

Regardless of which microprocessor family is chosen, the design team will want to develop a prototype quickly. They have two choices: to develop a prototype that approximates the final system, or to procure a standard microcomputer board that uses the selected microprocessor family. Either way, they can use a microcomputer development system to refine both software and hardware systems. For both they must determine required memory size, number of I/O ports, need for handling interrupts, number of interrupt levels, and amount of special circuitry to be incorporated on the MPU card.

Determining the memory size is of foremost importance. While an exact size can be determined only after extensive software development, in the majority of microprocessor applications a reasonable approximation of memory requirements is obtainable from a cursory analysis of the control, numerical, I/O, and data manipulation tasks to be performed by the microcomputer.

I/O requirements are determined by the number of peripheral devices to be used and the various control and data signals associated with each device. Specifications should include number of I/O lines, type of communication on each (eg, synchronous or asynchronous communication, parallel or serial data words), number of status flags, and data rates on each I/O line.

An adjunct of I/O requirements is the processor interrupt system. Interrupts, of course, are closely linked to the communication environment of the processor, and in most applications, the answer is fairly obvious. Not so obvious, however, is the required number of interrupt levels and the arbitration of interrupt priorities. Here again, a number of microprocessor families include a peripheral circuit which provides priority arbitration and vector generation. These flexible components allow the details of interrupt handling to be performed in software, instead of hardware.

Prototype specification is completed with the definition of any special circuitry required on a microprocessor card, which may include analog-to-digital converters, voltage translators, current buffers, and other equipment.

Once the prototype has been specified and built, and with the aid of a modern microcomputer development system, the software development team has all the diagnostic tools required to completely check out the microcomputer software and hardware system simultaneously. While this checkout is in progress, designers can begin detailed definition of the system hardware. At this point they must decide whether to use a generalized microcomputer card or a special-purpose logic module. Close attention must be given to future system expansion, production testing, field maintenance, final system partitioning, packaging techniques, board size, bus structure, and system voltage. A number of hardware trade-offs must be made at this time, each directly affecting the future usefulness and flexibility of the MPU card.

Generalized MPU Design Example

Trade-offs to be made in a microprocessor design can be illustrated through an example. The task is to develop a controller. Immediate design requirements comprise one serial asynchronous interface of 110, 300, or 1200 baud; input for seven status lines; output for 21 lines to an impact printer; output to 37 other control lines; enough read/write memory to satisfy the requirements of operating system software, plus a buffer for about 4K 8-bit words of data; read-only memory (ROM) for program storage, the actual size of which is to be determined during development; and service requirements for six interrupts. In addition, marketing requirements call for several future expansion options, including field-replaceable programs, field expansion of read/write memory, portable nonvolatile storage (probably either cartridge tape or flexible disc, but possibly a newer technology), and one additional communication interface for 9600-baud synchronous data transmission.

Analysis of the major present and future system requirements indicates that system controller and processor cycle time will be challenged primarily when the 9600-baud interface is attached. However, since 1-ms intervals are available between transfers of parallel 8-bit words into the interface, a high speed microprocessor is not required. Future field upgrade of the system calls for a modular system, a characteristic that is present in various microprocessor families.

Analysis also shows that a standard universal synchronous/asynchronous receiver/transmitter (USART) in the communication interface is desirable, because it eliminates the need for software-generated timing loops—not to mention word formatting and deformat-

System Component Examples

Card Type	Quantity	Components	I/O Lines*
CPU	1	8080A microprocessor	50
	1	8224 clock generator	
	1	8228 data bus driver, bidirectional	
	1	8214 priority interrupt control	
	4	8216 quad bus driver	
	1	8212 8-bit 3-state latch	
	1	8205 1-of-8 binary decoder	
	1 or 2	8316A 16K-bit masked ROM	
	2 or 4	8708 erasable 8K p/ROM	
	4	8111-1 static memory 256 x 4	
Memory Control	1	8222 refresh control	40
	1	8205 1-of-8 binary decoder	
		various logic ICs (TTL)	
Memory Module	16	2107B dynamic 4K x 1 RAM	40
	2	8212 8-bit 3-state latch	
	2	8216 quad bus driver	
	1	8245 quad MOS clock driver	
General-Purpose Input/Output	2	8255 programmable I/O device	70
	12	8216 quad bus driver	
	1	8205 1-of-8 binary decoder	
Impact Printer Control	2	8255 programmable I/O device	60
		solenoid drivers	
		various logic ICs (TTL)	
Communication Interface	2	8251 USART	40
	1	8205 1-of-8 binary decoder	
		various logic ICs (TTL)	
Mass Storage Controller	20 to 30	small and medium ICs	40
	1	8255 programmable I/O device	

*Not including power

ting, which would be difficult at 9600 baud under software control. I/O flexibility can be improved with the use of reprogrammable I/O circuits such as the MCS-80 8255. A number of I/O lines are provided from each IC package with simple interface to the system central processor unit (CPU) bus. Program control of the I/O configuration is important in a modular/expandable system.

Other Considerations

Another consideration at this time is whether to concentrate on the use of static or dynamic random access memory (RAM). Trade-offs include packaging density, power requirements during active and standby modes, reliability, ease of interface, and cost. Static memory is generally more expensive (cost per bit) than dynamic memory, and also tends to lag behind dynamic memory in packaging density. Interface design of the memory to the processor is generally easier with static memory.

Additional analysis of system requirements and how they fit various microprocessor families, leads to a decision to use a specific type or family of microprocessor. However, before beginning the detailed system design, other decisions must be made to determine the best long-term design approach. These include establishing present and future packaging constraints for the system, determining how many customers will eventually upgrade their systems—especially in preference to buying additional new systems, defining the company's field repair policy to fit multi-board and/or single-board designs, deciding whether various customers' requirements are different enough for modularity to increase sales, or similar enough for single-board design to pay off, and, finally, planning additional controller designs that might use the same CPU board, but different I/O and memory configurations.

For the present example, modularity was considered very important. Requirements for read/write memory vary in 8K-byte increments between different customers. I/O options vary from a minimum of 16 to a maximum of 96 lines. A field repair organization is already established to handle either the single- or multi-board configuration.

The decision to direct the design toward a multi-board modular system is followed by definition of system modules. Trade-offs for packaging are critical, and must be coordinated between the mechanical and electrical design teams, requiring a series of decisions.

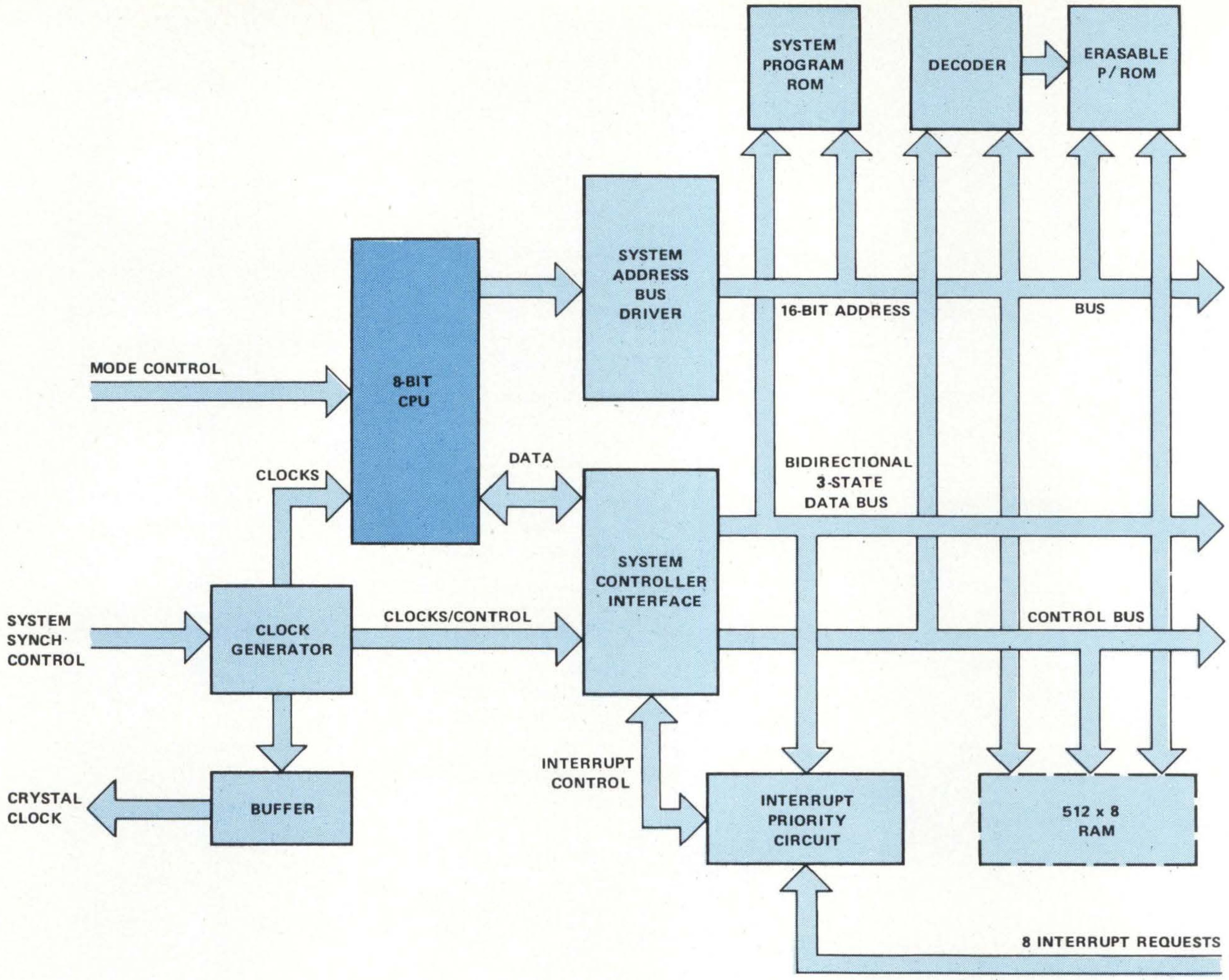

Fig. 1 CPU card. CPU clock and buffer requirements are included along with vectored interrupt and program memory. CPU mode control and system sync control as well as data, control, and address buses are available at the edge connector

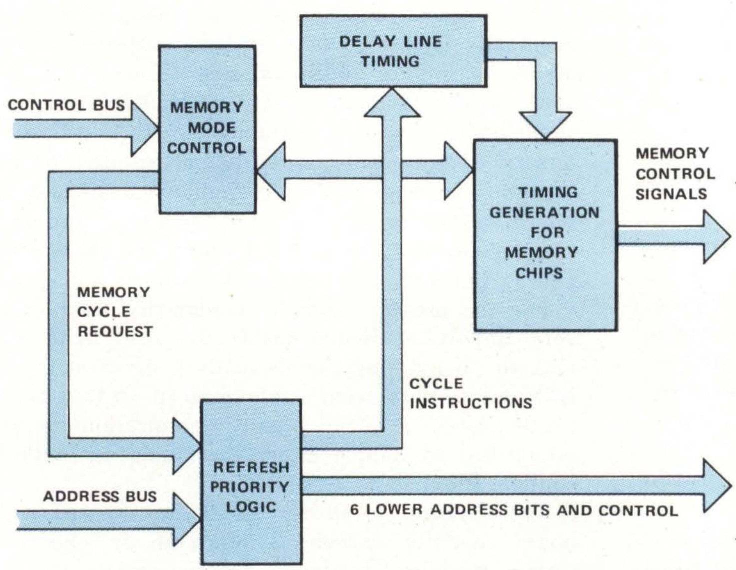

Fig. 2 Memory control card. With use of a dynamic read/write memory, refresh cycle control and priority are placed on this card, which also carries timing for read and write cycles for all dynamic memory cards

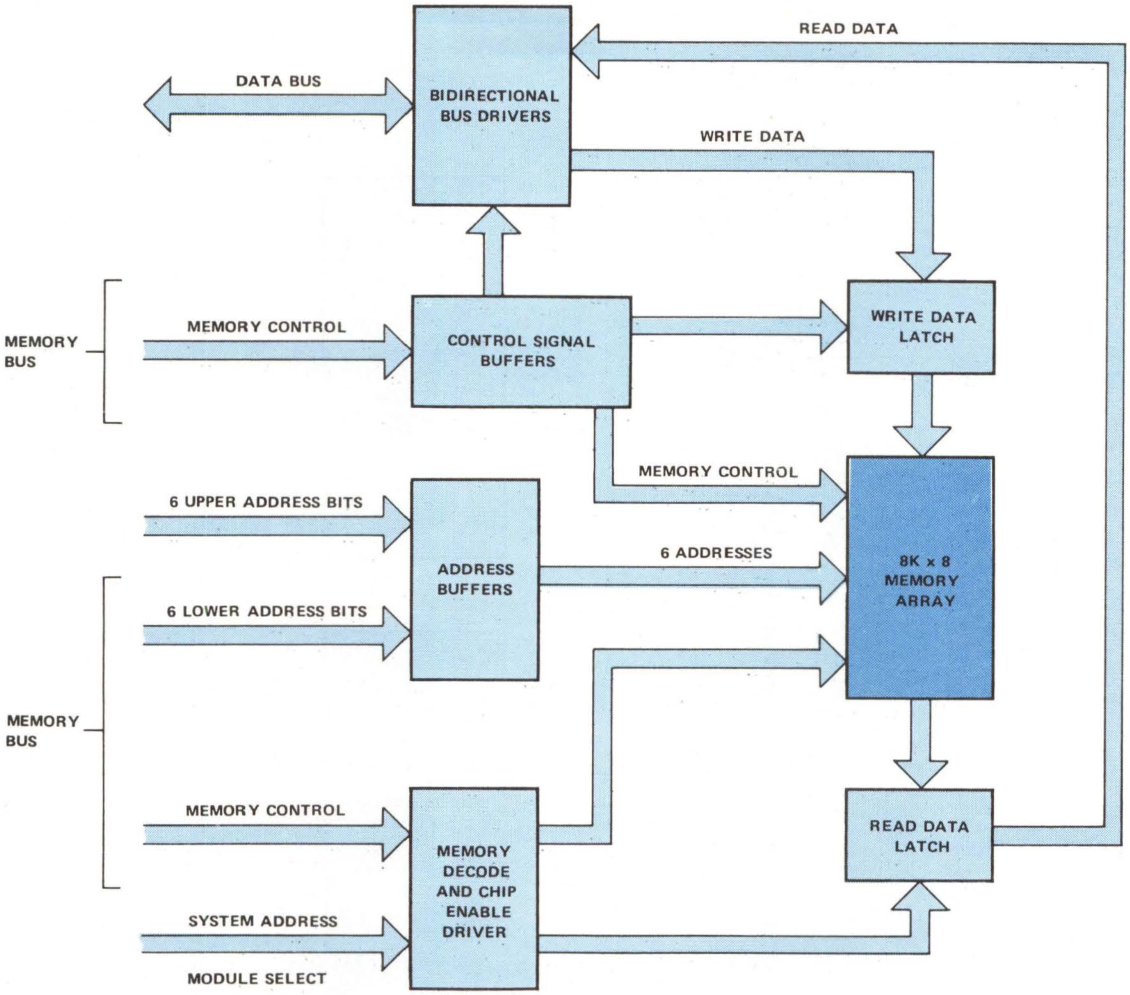

Fig. 3 Memory modules. Addressing and control of all modules requires only two buses. Memory and system module selection take place either through wiring on the backplane or switch selection on the card

First, mechanical engineers tentatively define the envelope available for mounting printed circuit (PC) boards. Electronic engineers then decide on tentative module configurations and the amount of board space they will need. Contributing to this decision are the total list of options, perhaps grouping the options as specific packages, and determining whether the options require similar amounts of board space. An important consideration is allowing for future field installation of options—deciding, for example, whether field installation of options requires wiring as well as adding components, which complicates the installation, or whether it should require only new components in prewired spaces. Options should be set up to minimize the number of PC boards in the system, while keeping the configuration on each board as unspecialized as possible.

Then, with module configurations and board space in mind, mechanical and electrical design engineers agree on definite board size and connector types for the system. Finally, design engineers start designing the board. All engineers must agree on the backplane connections prior to actual board layout.

Organizing the System

For the generalized example, the card configurations described in the Table are one approach to the system. Block diagrams of the card designs (Figs. 1 through 6) show the function of each in the system.

Each card has specific features that are important to the design flexibility and modularity. For example, on the CPU card (Fig. 1) all control, data, and address buses are accessible at the connector, allowing

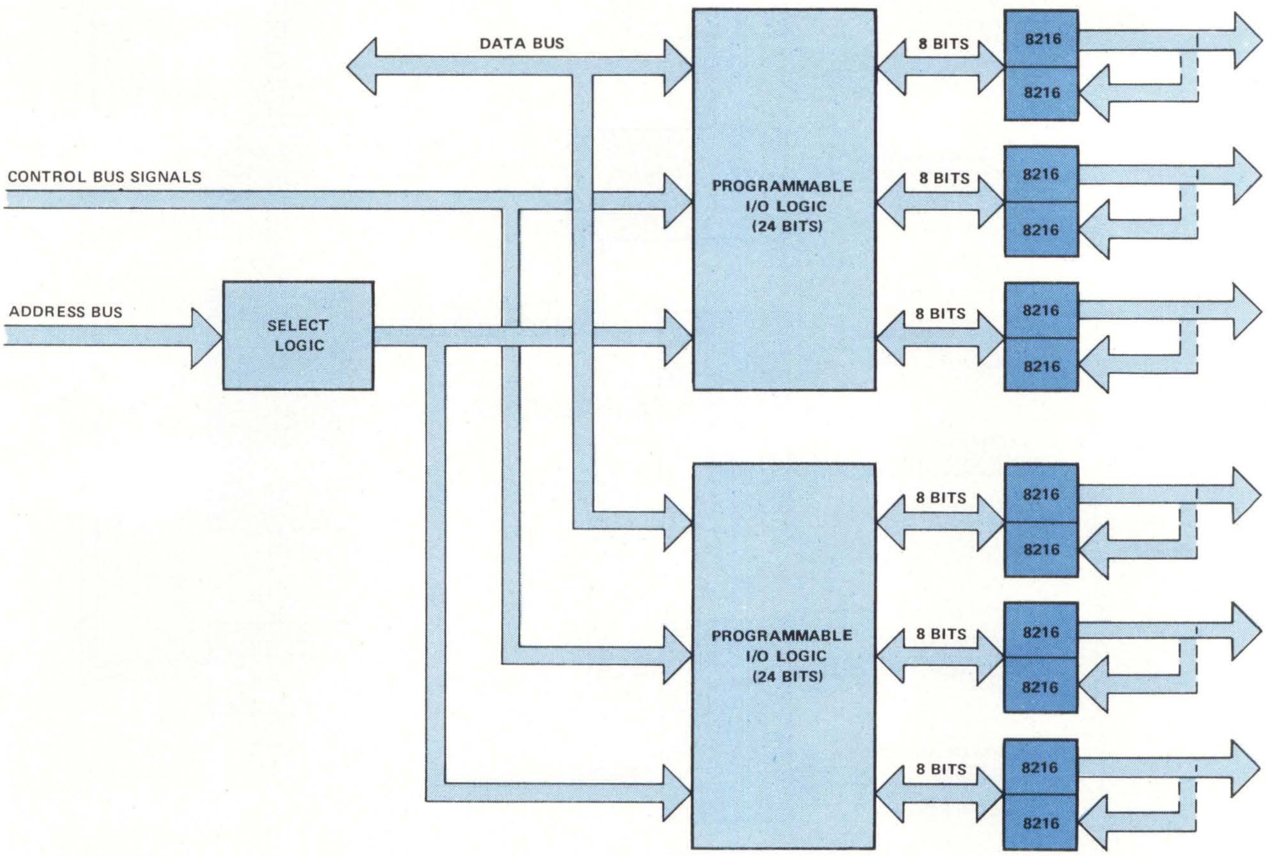

Fig. 4 I/O module. Through use of programmable I/O ports, card can be configured for almost any application. Program-controlled bus transceivers in sockets, which can be replaced by jumper modules for some applications, have adequate drive capability for any system requirement

full use of the CPU in other designs. All memory ICs are mounted in IC sockets, for easy expansion or removal. The optional 256 or 512 words of static read/write memory on the CPU card could replace the main memory and its controls in some system designs. Also, if the CPU card were used as a built-in diagnostic subsystem to test other system cards, static memory could store control and status information.

Memory modularity allows up to eight 8K-byte modules to be used in a system. To minimize total active system power and attain lowest costs, a dynamic memory using 4K RAMs was selected. Centralization of all control and timing for the memory modules is on the memory control card (Fig. 2). The control card provides an interface between processor and memory cards, centralizing refresh priority logic and generating timing for all memory cycles. Control signals and least significant address lines from the control card are on a separate bus, permitting ease of future modification of the memory system. The single control card makes it easier to use the memory cards with a different processor; only the control card interface to the processor needs to be redefined.

All memory cards (Fig. 3) are identical. They use 13 address lines to locate the specific word out of 8K words; the lower 12 of these are divided into two groups of six with the lower six multiplexed with the refresh addresses on the control module. The other line specifies one of the half arrays of each module. Card selects are decoded on each memory

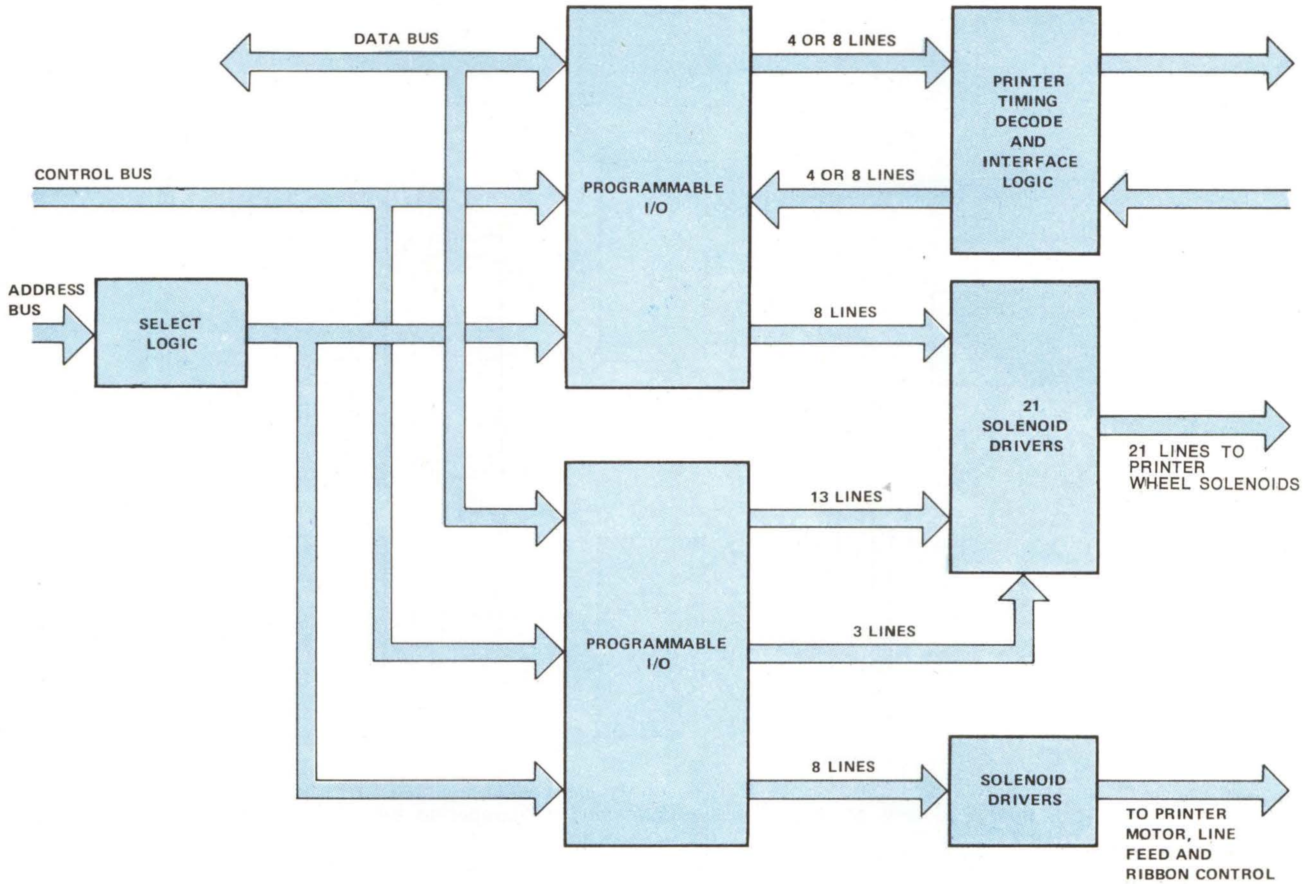

Fig. 5 Impact printer control card. Printer control is primarily through software. However, solenoid drivers for some functions, and timing and control interface conversion, require logic circuits

with the use of small dual inline packaged (DIP) switches and address-compare logic.

The I/O card (Fig. 4), using programmable large-scale integration (LSI) with program- or jumper-selectable drivers, has many different configurations. Output drivers are mounted in sockets. If the system requires buffered I/O ports, type 8216 bidirectional drivers are plugged in as shown in the diagram, and the appropriate input or output buffer drive direction is selected with wire jumpers. If system I/O requires strobed I/O ports or controlled bidirectional ports, the 8216 bidirectional buffers are replaced as necessary by headers that connect the I/O signals directly to the programmable logic. This design approach provides maximum flexibility of the I/O module in any system environment.

The impact printer control module (Fig. 5) puts most of its control in software, reducing hardware requirements and giving more flexibility to use the same interface with different printers.

The communication interface (Fig. 6) has sockets for the two USARTs, thereby allowing easy field expansion of the system. Selection of transmission speed and synchronous or asynchronous mode for each USART is made through system software. One USART is permanently wired to an RS-232 interface; the other can be connected to either an RS-232 or a current-loop interface, selected by jumper.

The system also has room for a mass storage card, undefined until later, which would have access to the common data address and control buses from the CPU

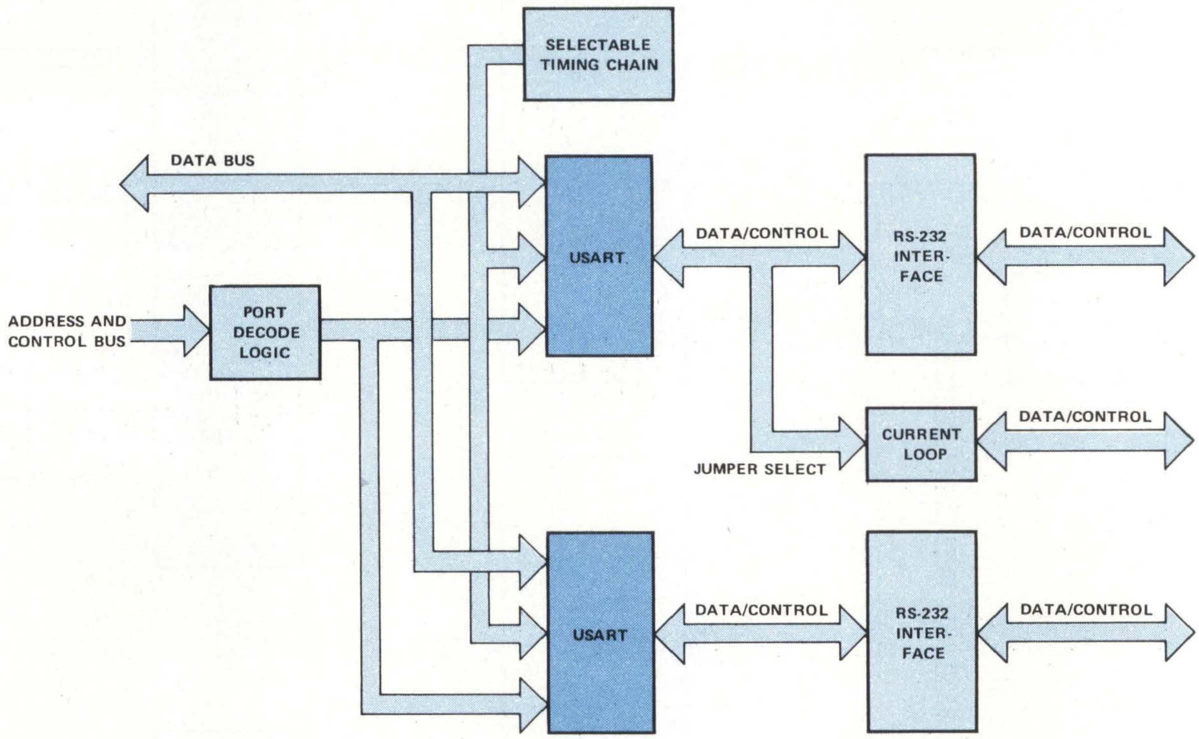

Fig. 6 Communication interface card. Both USART chips are socket-mounted to reduce cost in applications requiring only one interface. One of them can be connected by jumper to either a current loop or RS-232 interface

and would use programmable I/O logic in LSI and discrete form.

Buses Are the Key

After the design has progressed to a block diagram level, the approach to testing the modules and servicing the controller should be determined. Test capability of circuit cards or modules is strongly enhanced by the common data, address, and control buses linking all modules (Fig. 7). Through the buses, any CPU card or controller has access to any other card in the system. Thus, for production testing, cards can be individually checked for performance, using a special test control CPU or automated test equipment. Common bus organization also simplifies field testing and repair of the processor and its modules. Since all internal board communication is carried over these buses, controlling and monitoring the internal functions of the various system modules is easy. This, in turn, provides a simple technique for exercising submodules and detecting component level discrepancies.

Final system tests that put all of the logic together for a performance check are important. However, they should be made only after each individual module has been fully checked, including temperature burn-in and worst-case voltage margin testing, and a mechanical check. Pretested modules assembled as a system greatly reduce the number of failures when power is applied to the total system.

There are two approaches to field maintenance of the system (Fig. 8). One approach includes diagnostics as part of the system program and allows the end user to check his own system. The other uses an external program and test equipment attached to the controller buses, for checking by service personnel. The latter approach allows the field serviceman to reconfigure the system ROM card for a different ad-

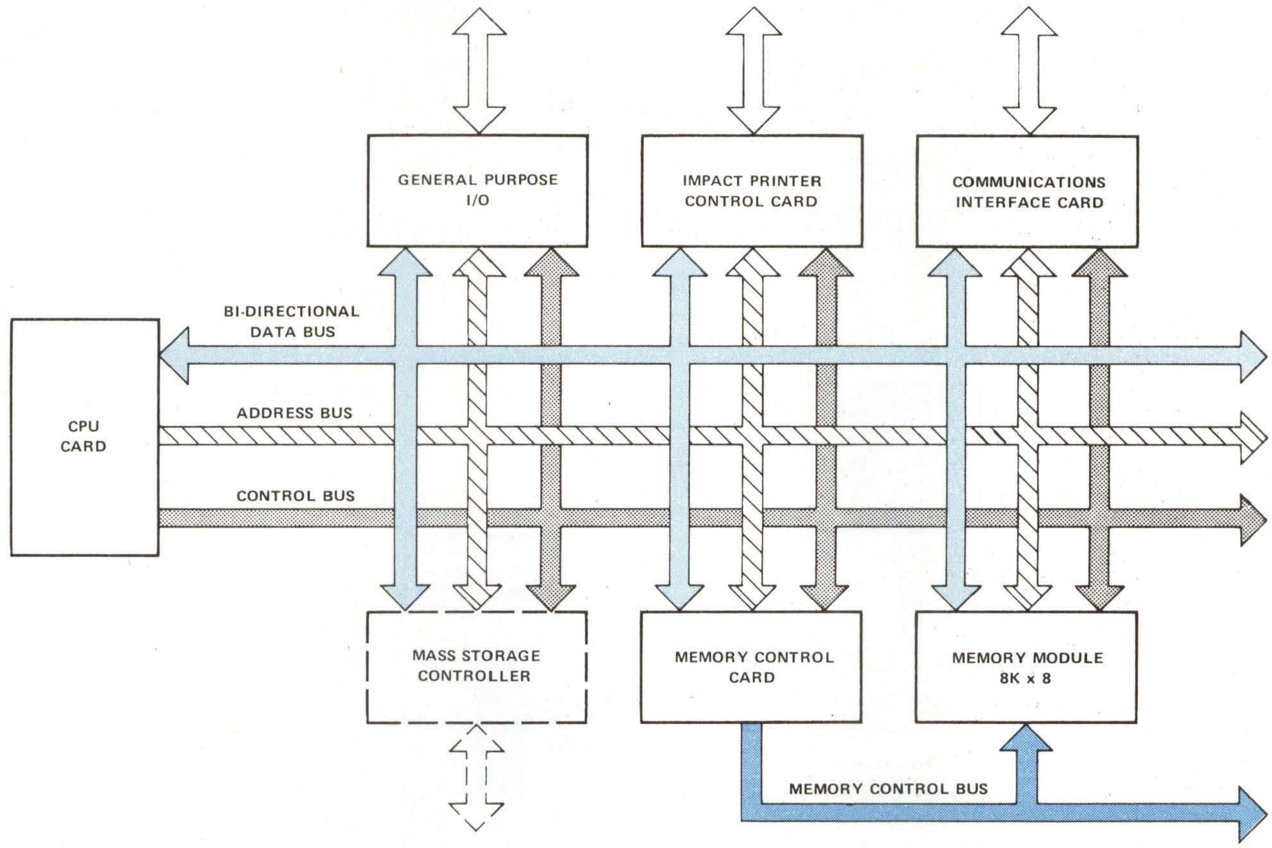

Fig. 7 System configuration. Data, control, and address buses are common to all system cards; memory control bus is separate

dress space or even remove the ROMs from the controller and plug in diagnostic programmable ROMs (p/ROMs) to analyze the system.

Physical attachment of the test equipment to the buses can be made at a connection on the CPU card or through a system bus connector. All power and control for the diagnostic tester would come from the controller chassis through this connection.

System analysis can proceed without any address reconfiguration if system software includes a means of sensing the remote test interface. For example, via power-on or a fixed interrupt, the software could check for the presence of a test program at a fixed address. If present, the test program would take control of the system. One advantage of this approach is that the diagnostic can use system subroutines in ROM to exercise various peripheral devices.

The printer and any other external display device could ordinarily be used as a diagnostic tool. Since a system failure could prevent use of these peripherals, one additional diagnostic display is required—for example, display of the diagnostic program address. After detecting a system failure, the diagnostic routine would display its current address on the tester control panel indicators and jump to a specific HALT instruction in the program. The address at which the machine halts would correlate to a specific failure.

Summary

Microcomputer design is a complex process that requires concentrated, directed effort on the part of software and hardware design engineers, project management, and marketing personnel. Careful thought and consideration must be given to all aspects of future product utilization. Decisions are made throughout the development program that affect production costs, pack-

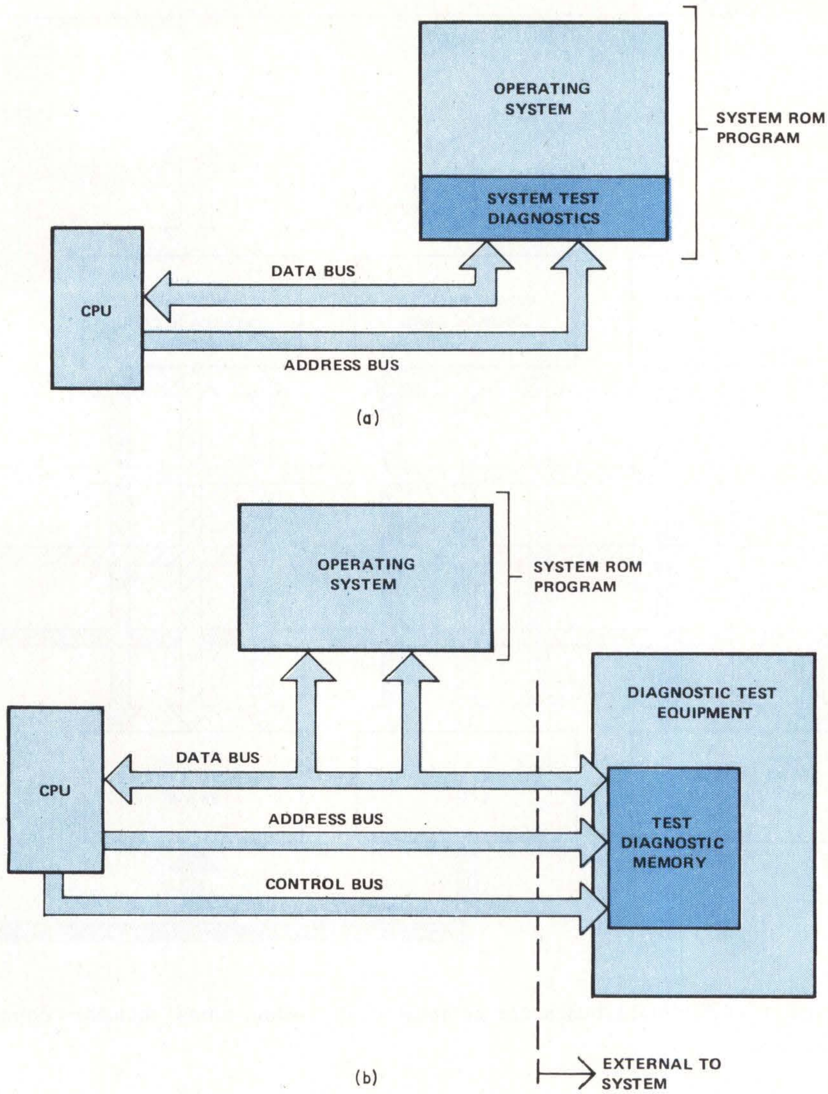

Fig. 8 Two approaches to diagnostics. Diagnostic programs can be included with the system program in a read-only memory (a) or, alternatively, can be stored in the field service equipment memory (b), which is connected to the system buses for testing

aging, customer options, modularity, field maintainability, performance, and future system expansion. With complete and detailed planning, a manufacturer can design hardware obsolescence out of his products. By treating a microcomputer system as though it were a small minicomputer, specifically designed for an entire line of products, equipment manufacturers can take full advantage of today's microprocessor technology.

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Manager of custom systems engineering, Peter Thomas holds a BSEE from Utah State University and an MSCS from the University of Santa Clara. At Intel's Memory Systems Div his experience includes product development of custom memory boards, memory systems, and custom microprocessor systems.

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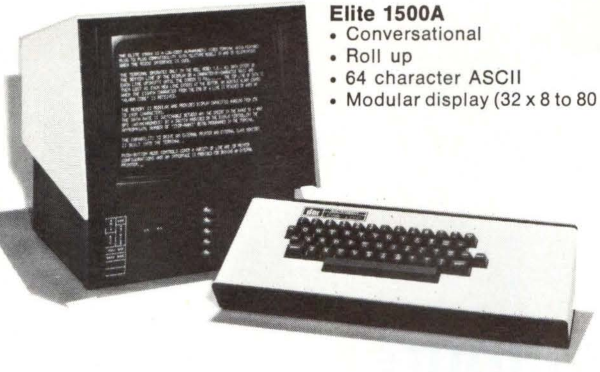

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- Roll up
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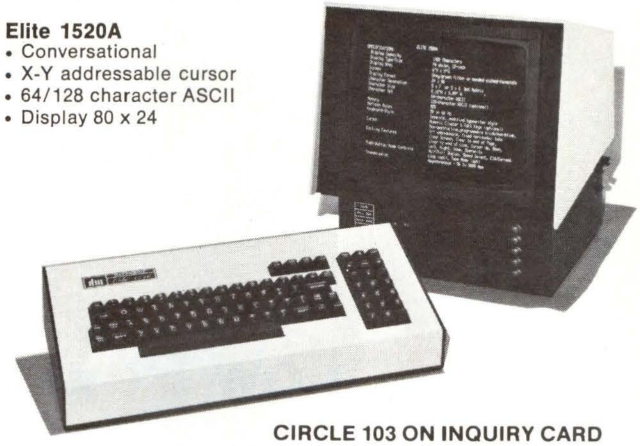
- Modular display (32 x 8 to 80 x 24)

CIRCLE 102 ON INQUIRY CARD

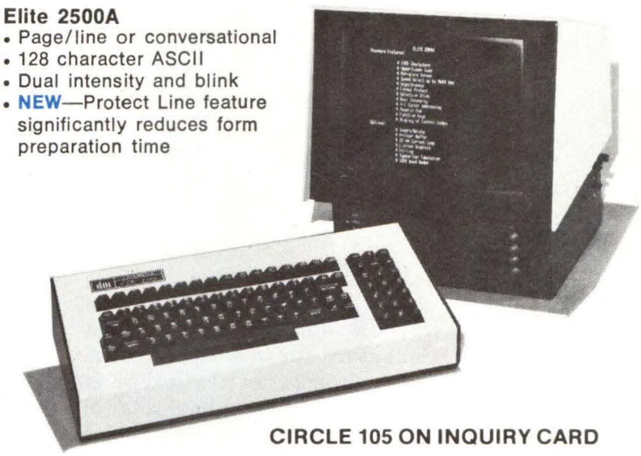


Elite 1520A
- Conversational
- X-Y addressable cursor
- 64/128 character ASCII
- Display 80 x 24

CIRCLE 103 ON INQUIRY CARD

Elite 1520APL/ASCII
- Conversational
- 128 character APL/ASCII
- Bit-paired or typewriter-paired
- Display 80 x 24

CIRCLE 104 ON INQUIRY CARD



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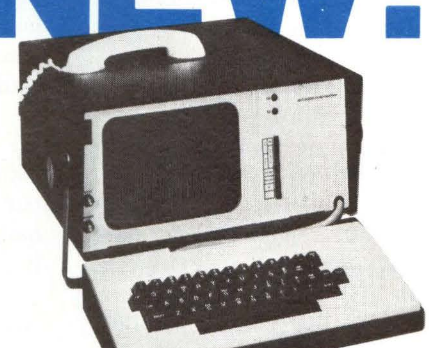

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APPLICATION NOTE

Low Power Computers: A Make or Buy Decision

Jerry Washburn

Computer Automation, Incorporated
Irvine, California

Although microprocessors are justifiably an increasingly popular type of component for use in many systems, many reasons for using a standard low power minicomputer of traditional design are discussed from the viewpoint of a minicomputer manufacturer

Engineers who work for companies in the OEM market* often must decide whether to build or buy low power computers—sometimes called microcomputers, millicomputers, or minicomputers—for the systems they design. Should they solve the dilemma by building computers with microprocessor chips and other integrated circuits, or should they buy standard low power computers?

Building low power computers always seems attractive; it's easy now, with over 25 microprocessor chip sets on the market. Semiconductor manufacturers claim that users can satisfy their computer requirements at the lowest possible price by selecting, configuring, and assembling microprocessor chip sets.

In many applications, the do-it-yourself microprocessor chip set or kit approach does indeed provide a workable low power computer for the system. However, when all the factors that affect a rational decision are examined, computers implemented from do-it-yourself microprocessor chip kits often turn out to cost more than mass-produced computers from bona fide minicomputer OEMs. Unless the application calls for a very large number of computers with minimum performance to work with equipment, the requirements of which are unlikely to evolve, microprocessor chips do not usually offer the better way to go. Designing the system to use microprocessors may be more fun for the engineer, but not for the general manager (Fig. 1).

Microprocessor chips generally are suitable for high volume applications requiring small physical size, for which limited performance is adequate. They provide excellent solutions to design problems posed by auto fuel systems, clocks, calculators, cash registers, small test equipment, and many other consumer-related products.

Although the cost of microprocessor chips is attractive, other costs must be considered, too. These expenses include such items as software development, supporting system hardware components (Table 1), testing, sustaining costs, and associated risks. In building a low power computer, what the system designer may not know at the start of the project *can* hurt him, because the price of the hardware is just the starting point for the total cost.

Before building a computer, the system designer must first determine

*Ed. Note—Mr Washburn's discussion of an important design decision principally concerns OEMs—an abbreviation that most readers recognize as standing for Original Equipment Manufacturer. The term correctly describes the seller of an item traded in large quantities for incorporation in a customer's product. It does not describe the buyer of such an item—even though the abbreviation is often used incorrectly in that sense. Thus, Mr Washburn's employer is an OEM to many of its customers, such as process-control system houses, makers of data acquisition systems, and builders of communication networks. This article has been edited with this definition in mind.—WBR

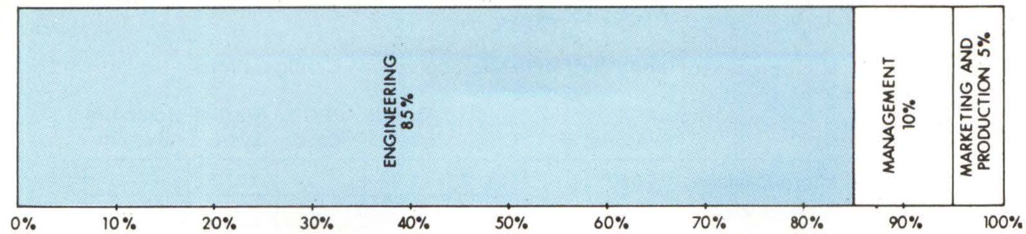


Fig. 1 Impetus. Customer survey showed that the major motivation for using microprocessors comes from the engineering department, rather than from top management or other departments

how much computer power is needed. Once that decision is made, the design team usually must acquire specialists in software, firmware, CPU, memory, and interfacing. Extra personnel for drafting, testing, documentation, maintenance, diagnostics, inspection, and supervision for the computer portion of the system are also required. These requirements invariably get bigger as the product functions and capabilities evolve or change.

The Processor

Microprocessor architecture usually limits do-it-yourself computers to a basic repertoire of 50 to 75 primitive instructions. Since microprocessors generally are not I/O-oriented, they provide I/O only through registers. On the other hand, computers from minicomputer manufacturers provide programmed I/O through both registers and memory, plus automatic I/O instructions and a standard direct memory access port.

Microprocessor chip interrupt capabilities are minimal; most minicomputers provide system-oriented interrupt structures. (Interrupts are signals generated by internal and external sources, such as peripherals, to take the processor away from the task it is performing and direct it to handle other systems events.) Minicomputers usually offer a wide variety of interrupts, enables, disables, and a nesting capability for processing several sequential interrupts. This multiplicity of fully implemented, vectored priority interrupts is hardly comparable to the one partially implemented interrupt level that micros typically furnish.

Instruction cycle time is the typical rule-of-thumb measurement of a processor's macroinstruction speed. Microprocessor cycle times are longer and the chips use many cycles to perform useful operations, because semiconductor manufacturers have had to make compromises in chip geometry, number of pins, and cost versus performance. Fewer of these limitations constrain minicomputer makers, who thus can make tradeoffs that shorten instruction executing times by factors of two to eight relative to the microprocessor.

Minis often have very powerful macroinstructions that would require implementing with many subroutines in microprocessor chip sets, whereas 4- and 8-bit microprocessors generally perform arithmetic instructions slowly because of limited word size. These microprocessors make up the majority of available types; only a few have 16 bits. Word size also affects instruction power and speed, because shorter words can call up fewer operations than longer words. A substantial proportion of operations by micros therefore requires multiple-word instructions.

Minicomputers not only offer higher processing speed than microprocessor chip sets, but also use memory more efficiently. For example, minicomputers have powerful user-level instructions that get more done in a single instruction cycle than a microcomputer can hope to achieve. In many cases these macroinstructions are possible because the minicomputer's control store has long words with which to specify many steps in a complex sequence—whereas most microcomputers, if they have control stores at all, have control words no longer than the data words. These are two ways to achieve high memory efficiency, which is very advantageous, because memory often costs many times more than the CPU itself.

TABLE 1

Typical CPU Cost Breakdown

Components	Percentage
1. Control ROM	30
2. File/ALU Functions	20
3. Bus Functions	20
4. Miscellaneous/Hardware	30
TOTAL	100

Occasionally, the potential chip user selects a microprocessor that does not work in his system, because of incomplete evaluation or increased performance requirements. This realization may come too late for him to recoup his development costs. The minicomputer manufacturer minimizes this risk by providing a complete line of mutually compatible processors, arranged in steps of increasing capability or power; few micro makers have this capability.

Software

Minicomputer manufacturers offer a complete line of time-tested, high level language software packages that generally include several assemblers, loaders, various subroutines and utilities, editors, and diagnostic programs. They also supply a user's manual and documentation.

TABLE 2

Microprocessor and Mini/Milli/Microcomputer Configurations

Manufacturer	Model #	Chip	Chip Set	PC Card	Partial System	Complete System
Advanced Micro Devices	9080	■				
American Micro-Systems	9209	■	■			
Computer Automation	LSI-3/05			■	■	■
Digital Equipment Corp	MPS			■		
	LSI-11			■	■	■
Electronic Arrays		■				
Fabri-Tek	MP-12			■	■	
Fairchild Semiconductor	F-8	■				
General Automation	Solution 16			■	■	■
General Instruments	CP1600	■				
Intel	3000	■				
	8008	■	■	■		
	8080	■	■	■		
Intersil	IM6100	■				
Monolithic Memories	6701	■				
Mostek	5065	■	■			
Motorola	M6800	■	■	■		
National Semiconductor	IMP 8		■	■	■	
	IMP 16		■	■	■	
RCA	COSMAC	■	■			
Rockwell International	PPS-8	■	■			
Signetics	2650	■				
Teledyne Systems	TDY52		■	■		
Texas Instruments	9900 Series	■	■	■	■	■
Western Digital	MPS1600	■				

Most micro users, on the other hand, are obliged to develop programs in assembly language with the help of a read-only memory assembler card or on a large computer. Their programs can be tested on the microprocessor itself or simulated on larger computers. However the testing of programs on micros themselves is often difficult because some of them are unable to operate in single steps and do not offer access to internal registers.

Simulating microprocessor software operation on large computers does not necessarily offer the best solution, either. Large, very expensive-to-use computers or timesharing computer networks cannot effectively simulate the input and output required to debug the real-time parts of a microprocessor application program. In many cases, the system designer must develop his own prototyping aids or purchase expensive development equipment. In fact, many designers are beginning to use minicomputers for microprocessor simulation. If a designer has to use another computer to support his macroinstructions, he might as well use that computer to complete the total job.

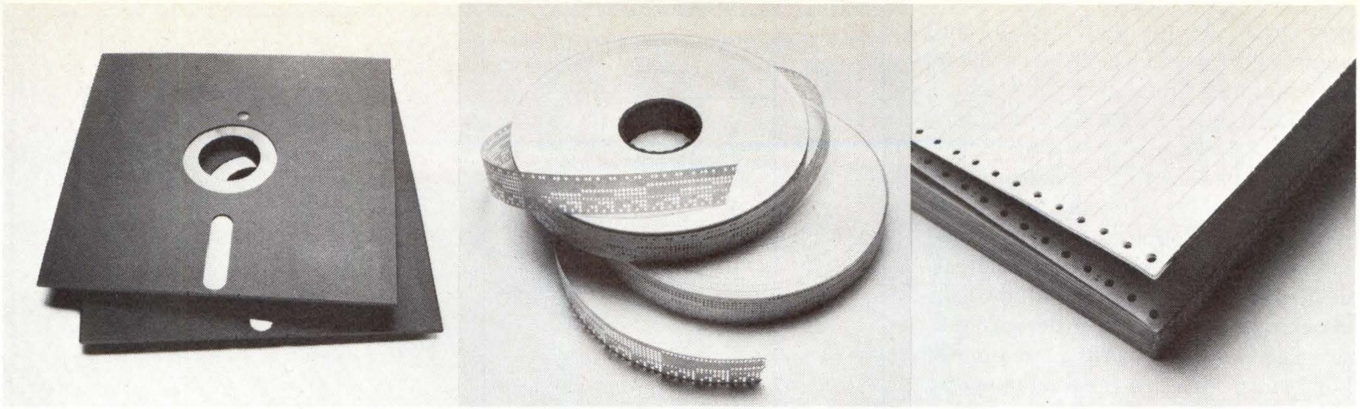
OEMs offer batch operating systems with real-time operating systems and BASIC and FORTRAN languages, whereas chip manufacturers usually offer nothing comparable. In some cases, modified subsets of high level languages are available for micros, but most of these are limited and inefficient. The comprehensive library of software available from minicomputer houses greatly reduces the time required to develop the programming for a product. At the same time, superior programmability of minicomputers makes software generation faster and easier.

System Hardware

Semiconductor manufacturers do not offer the potential low end computer user a full line of off-the-shelf system components. Of 25 suppliers of mini, milli, and micro equipment and configurations (Table 2), less than 50% sell their microprocessor assembled on a printed circuit board and only 25% offer supporting system components, such as memory and teleprinter interfaces, to support their chip sets.

Only OEM minicomputer companies market a full line of selectable supporting system components, including chassis, power supplies, panels, core and semiconductor memories, peripherals, and interfaces. Computer Automation, for example, offers off-the-shelf interfaces for numerous specific devices and many types of general purpose interfaces. Just recently, the company introduced a universal distributed I/O system for interfacing peripherals at a price of well under $200 in quantities of 100. That price includes peripheral cables and connectors.

By contrast, the chip manufacturer generally markets only a teleprinter interface. Consequently, the



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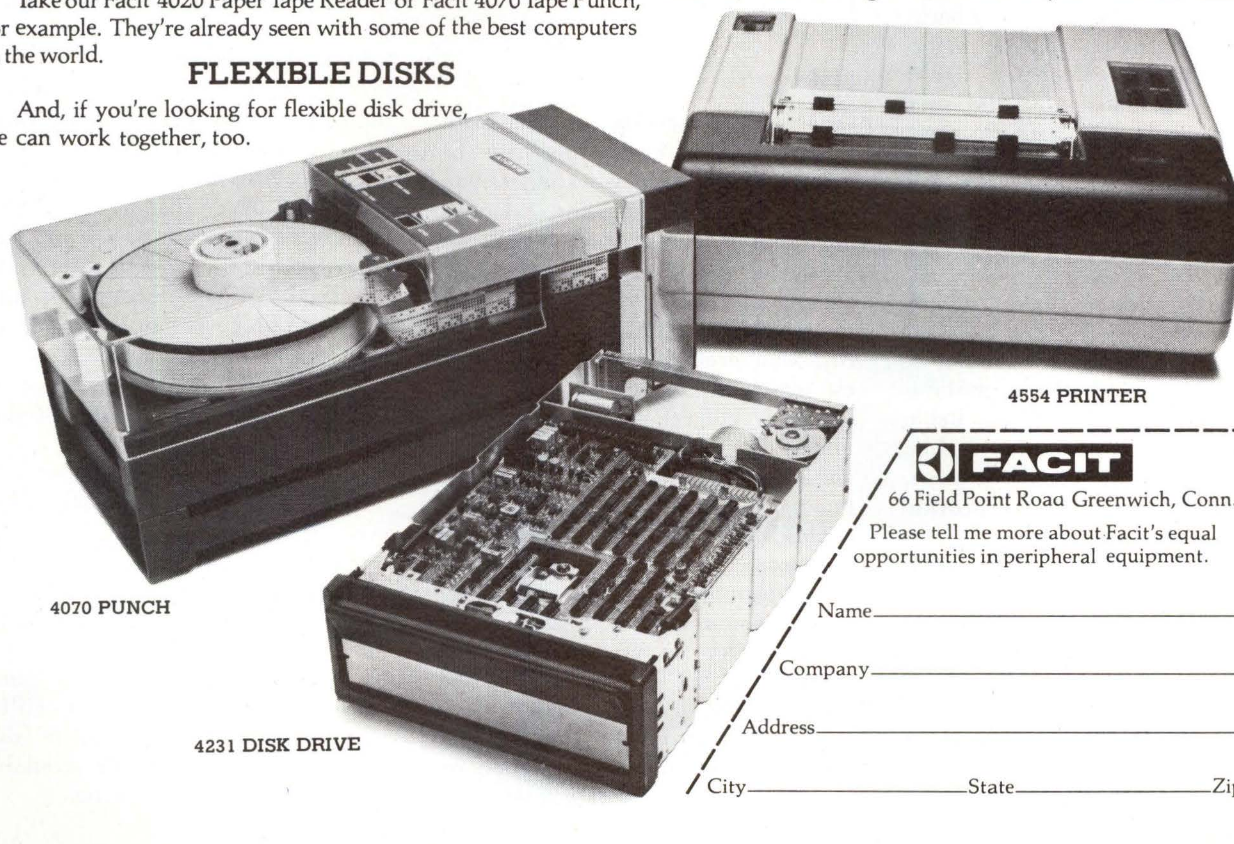

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City__________ State__________ Zip__________ user must design, build, test, and manufacture interfaces to mate other I/O equipment to a special I/O chip, and incorporate it into the computer.

Alternatively, the user can invent his own interface to the microprocessor. However, because this approach requires completing the CPU interface definition before the peripheral device interface design is started, attaching gadgets to the microprocessor chip set can take a distressingly long time. With a general-purpose minicomputer interface, on the other hand, hooking up an I/O device often consists of merely wiring up an interconnecting cable.

Product Development

Development of a product generally occurs in two phases: assembling and testing a prototype, and manufacturing the finished design. During both of these phases, development costs of kit machines can skyrocket, because of the things that the semiconductor manufacturer can't pack into the kit—such as documentation and testing. The hidden cost of software, documentation, and development far outweighs the savings accrued from the low microprocessor price.

The premanufactured minicomputer frees the designer from tasks that can erode his budget. Such tasks as interfacing a memory to the processor or designing battery-backup for the memory can be nightmarish. The minicomputer OEM solves these problems for the user by making available a large selection of memories in a variety of types, speeds, and sizes.

Continuing Costs

When using microprocessor chips, the designer must also add product continuation costs to the total. These added costs include testing, sustaining, engineering, and the inevitable repair of failed products. Unlike many minicomputer manufacturers, some chip suppliers do not provide warranties on components.

Microprocessor chip testing is difficult and expensive. Since the chip manufacturer must minimize test time to sell his product for a profit, he must avoid exhaustive, time-consuming tests; otherwise no one could afford to use a microprocessor. Cost of exhaustive testing is very high, because a typical microprocessor

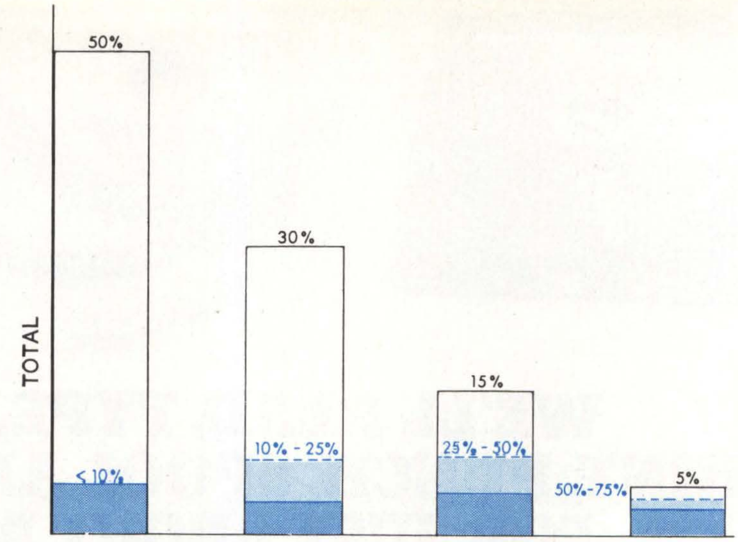

Fig. 2 Diminishing returns. Relation of potential microprocessor applications to microprocessor cost as a proportion of total product cost shows that in most applications microprocessors (blue) represent a very small part of the total cost—whereas using a low power computer is much less risky. For example, in 50% of potential applications, the microprocessor represents only 10% of the total product cost

chip set contains 12,000 to 15,000 active elements. This complexity can allow microprocessors to run perfectly on many possible programs, only to malfunction when run on another program. Therefore, the potential user must be prepared to test microprocessor chips.

Risks

Developing a specific product with a microprocessor chip set can be risky business for reasons other than those already noted. For example, the chip or chips selected may be available from only one source, placing the user at the mercy of the supplier and of his good fortune. Although probably few, if any, honest semiconductor makers would deliberately cut off a customer except under dire economic circumstances, all of them are subject to fires, floods, or other catastrophes that could leave a user in a very embarrassing position. Currently only one or two microprocessor chips have multiple sources, but cross-licensing is beginning to appear. Generally, where quantities are involved the best policy is not to gamble, but to stay with a microprocessor chip or chip set that has alternative suppliers. On the other hand, remember that even though two manufacturers offer identically specified parts, their microprocessors may contain idiosyncrasies that can be incompatible in some applications.

Time is one risk that the project manager or system designer must carefully consider. Overrun development schedules can be costly in development charges and potential loss of profit caused by amortizing the extra development expense. Product development with microprocessor chips can take as much as six months to a year longer than it would with standard minicomputer products from an OEM. Manufacturers who use small OEM computers in their systems usually get to market faster than those who use microchips and can beat their competitors, thus increasing their chances for product success (Fig. 2).

Generally, the user does better by buying from a minicomputer OEM, even if cost trade-offs show little or no benefits. A minicomputer that is easy to work with gives the designer a benefit that means much more than money. It gives the system manufacturer peace of mind, because the software tools, CPUs, and system hardware are all reliable, field proven, and readily available. All it takes is smart buying. □

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An Economical Diskette Drive Subsystem

A complete subsystem including a single diskette drive (Model 70), the Model 1070 controller with interface and a controller-to-disk-drive cable is available in single units for $1,195. For double capacity, a dual diskette drive (Model 270) subsystem is available for $1,495. OEM discounts available.

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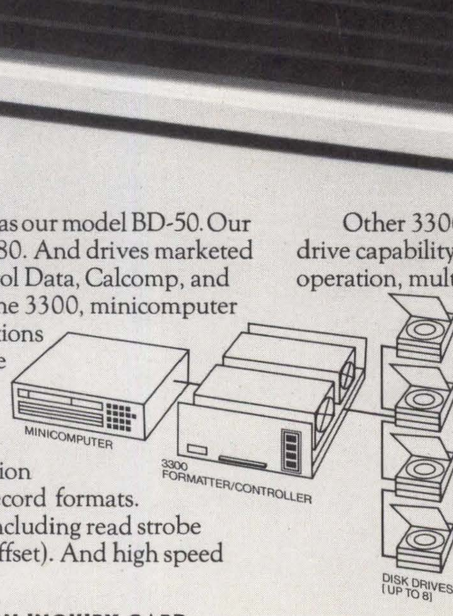

Other 3300 features include multiple drive capability (up to 8), seek overlap operation, multi-record transfers, internal data encoding and decoding, alternate track sparing, and FIFO buffering. Plus additional performance characteristics to facilitate maintenance and configuration flexibility.

Many optional features are available. Including dual port con-

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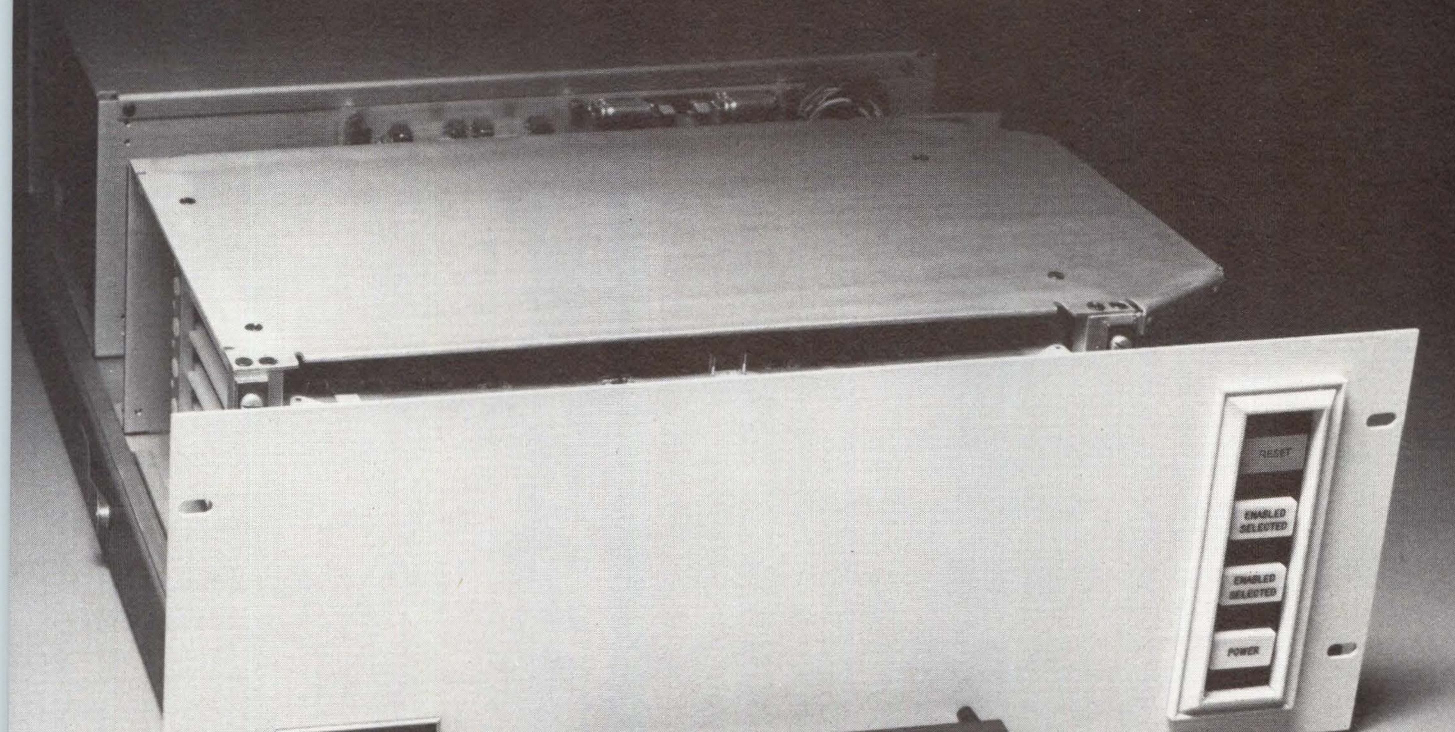
better disk drive.
ter/controller to match.



figuration. (The 3300 automatically resolves disk contention and file reservation from multiple CPUs.) And a multiple-drive power sequence module.

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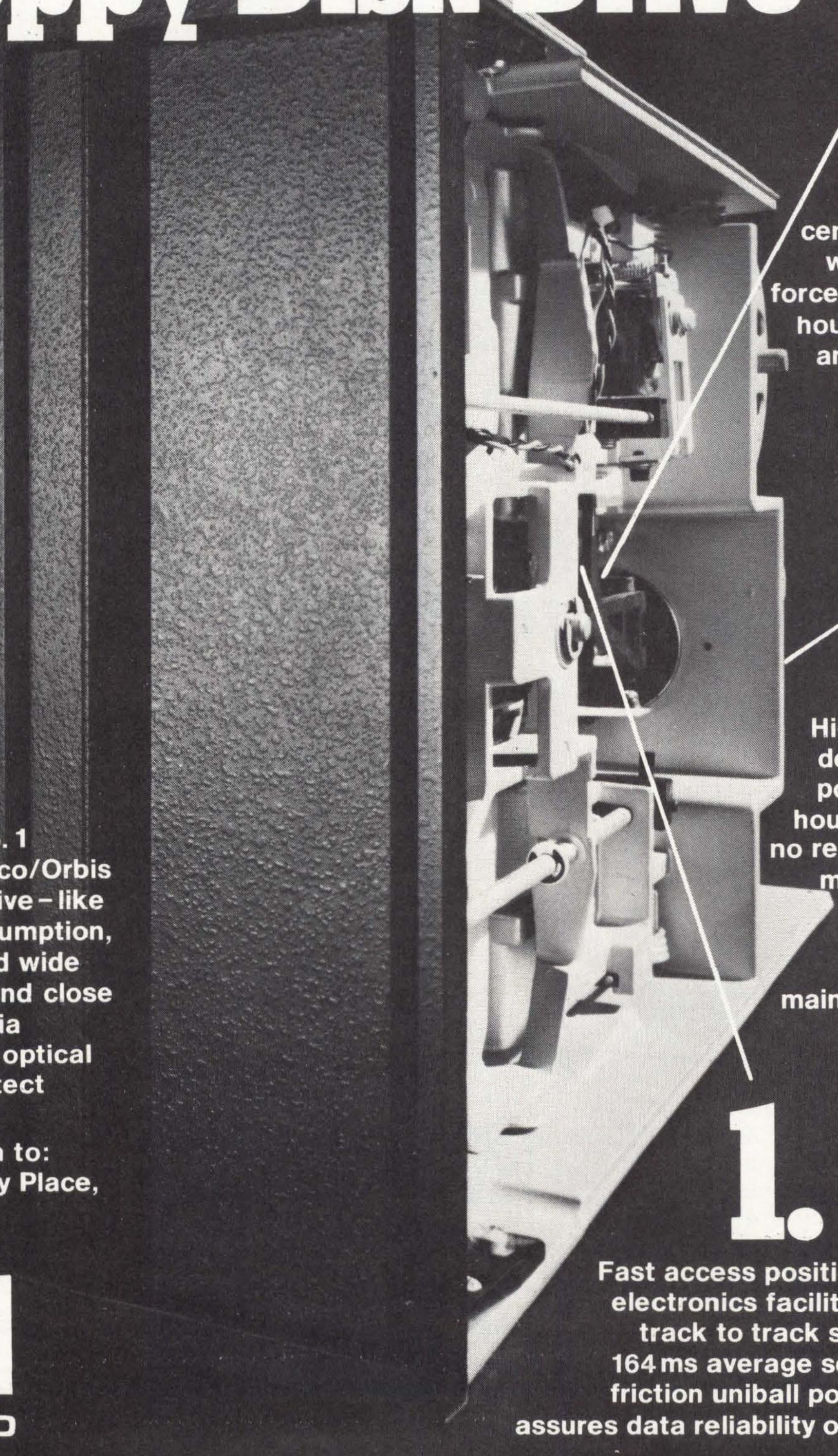

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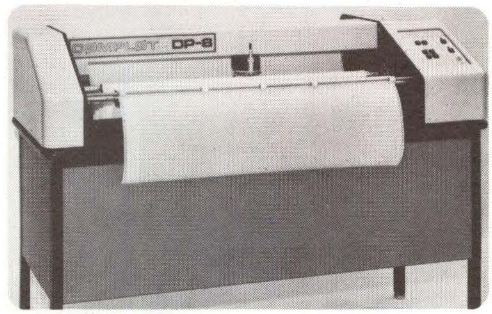

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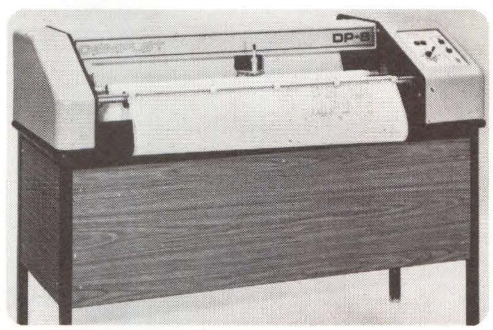

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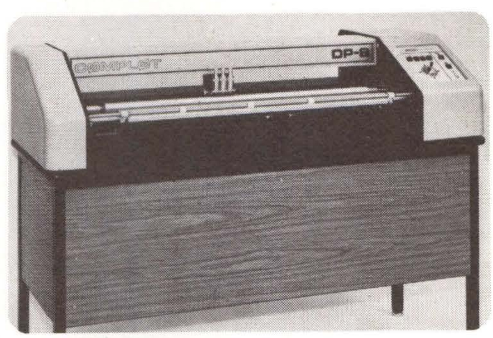

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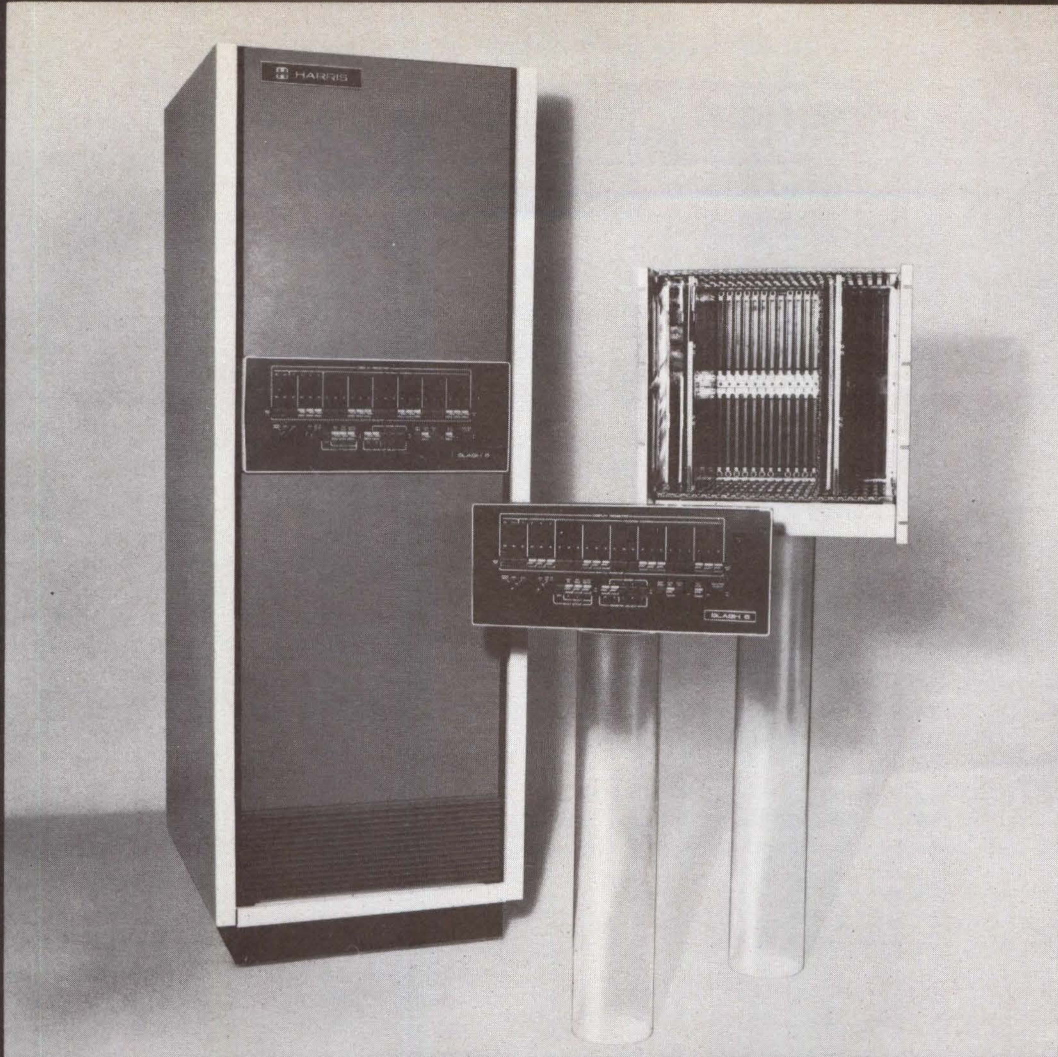

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CIRCLE 54 ON INQUIRY CARD

The Changing World of Advanced LSI

Computer Design
Editorial Staff

Technological growth has rarely been as dramatic as in the development of semiconductors, and particularly of integrated circuits. Even the introduction and acceptance of the transistor itself seem minor compared to the impact of small-, medium-, and now large-scale integration.

Since the early 1960s, developments in semiconductor design and manufacturing technology have resulted in a doubling of the number of components per chip every year as well as spectacular increases in speed, concurrent with increasing chip densities and reduced power requirements. Per-chip prices, however, have remained relatively uniform, resulting in the equivalent reduction of per-component, or per-bit, prices by a factor of two per year.

This dramatic technological growth is particularly significant to the designers of digital equipment. In the present and near future it means major equipment simplification as well as increased sophistication. Possibly even more important, it means substantially lower per-function costs. Products that were previously technically impractical or commercially unsound are now being introduced or are rumored. Even if the past trend of rapid development were to slow, the technological impact will remain. For instance, one forecast calls for the mid-1980s debut of a desk-size computer, equivalent in power to a mid-range System/370, with 1M byte of semiconductor memory—priced at \$2500 to \$5000.

As spectacular as this may seem, the effects over the somewhat longer term may be even more important. In addition to expected miniaturization, digital equipment will come to depend less and less on electromechanical mass storage. Disc and tape storage, although not fully replaced, will be secondary to such devices as high density read-only memory, charge-coupled devices, and bubble memory.

Miniaturization and cost advantages of electronic portions of a system may in some cases be offset by the bulk and expense of mechanical and electromechanical components. For instance, evolution of the computer has been characterized by a tendency to maintain size and cost balance among the system's three elements: processor, memory, and power supply—with technological effort necessarily focused on the element that lagged the others and therefore "didn't fit." Therefore, recent major cost and size reductions in central processing unit and memory which brought about the microcomputer caused emphasis to be placed on the power supply. Solutions, in such forms as switching regulated supplies, have been provided—as in the past —by new developments in semiconductors. Similarly, other advances brought about by advanced semiconductor technology and use of large-scale integration should bring at least some of the input/output devices into line with the rest of the computer system.

Impact of large-scale integration has been evidenced in such areas as information sensing, where "real-world" data enter the digital system through analog-to-digital converters, which are now available as inexpensive yet fast monolithic integrated circuits. As the next step in the integration process, these converters and associated devices are being designed directly into the processor chips, substantially reducing the complexity and cost of the interface.

Recent and Near Future Developments in LSI Devices

- Programmable digital *frequency synthesizer* using IIL and Schottky technology to replace discrete component telecommunications equipment
- Ion implantation bipolar chip containing most of the components of an integrated *switching regulator*
- Bipolar *microprogram sequencer* with highly versatile control features
- *A-D converter* combining digital and linear CMOS, minimizing external circuitry, interfacing directly with TTL or CMOS logic, and especially suited for microprocessor controlled bus-oriented systems
- 4-decade IIL LSI *programmable counter* using one-third the power of a competitive CMOS counter and operating at more than 60% higher frequency
- *Interrupt controller* with eight levels of requests, and expandable to configurations of up to 64 levels
- 8-bit I/O port
- 1-of-8 decoder
- Priority interrupt control unit
- 4-bit bidirectional bus driver
- Programmable interval timer
- DMA controller
- General-purpose software programmable I/O chip
- General-purpose keyboard/display, floppy disc controllers
- Solid-state crossbar switch
- Digital dialer chips for telephone application
- LSI multiply/divide unit
- Synchronous data link controller
- Programmable communications interface
- Programmable I/O port

Impact of Large-Scale Integration

To a large degree, the continuing interest in further development of large-scale integration (LSI) techniques is a direct consequence of successes thus far. Clearly, the microprocessor with its wide potential in present and new applications cannot be fully exploited if large numbers of additional integrated circuits (ICs) are required, for example in system interfaces. Thus, the trend is toward increasing microprocessor sophistication, adding to the central processor unit (CPU) chip many functions which in earlier units had been relegated to external ICs.

The substantial increase in the variety of LSI devices used with microprocessors has enhanced the system simplification made possible by the microprocessor itself. Markets for microprocessors have provided the economic motivation for the development of many of these chips; high volume applications that were not feasible prior to the advent of microprocessors are stimulating LSI developments which would have been uneconomical only a year or two ago.

Microprocessors as generally available components are only about two or three years old, and much of their supporting LSI has been developed even more recently. However, a survey conducted early in 1976 showed that LSI devices—in addition to expected read-only memory (ROM), random-access memory (RAM), and programmable ROM (p/ROM)—were already in extensive use.* In addition, a number of LSI devices have since become available or are soon to be introduced (see "Recent and Near Future Developments in LSI Devices").

Developments in LSI Technology

Inventiveness of semiconductor design and manufacturing engineers has continually extended technological performance beyond that predicted by even the most knowledgeable forecasters—basically because no allowance can be made for "breakthroughs." As an example, after two to three years of evaluation, bipolar integrated injection logic (IIL) is emerging as a serious and exciting entry in the LSI race. It is presently regarded as a competitor of complementary metal-oxide semiconductor (CMOS) but not to MOS in general. Although many of IIL's performance advantages have been diluted by continuing spectacular improvements in the speed and power consumption of CMOS, the special ability of IIL to combine low cost digital and linear functions on the same chip is a major asset in meeting increasingly complex LSI interface requirements. Among the linear functions that have been combined in this way are operational amplifiers, sample-and-hold circuits, and A-D and D-A converters.

Other IIL advantages are exceptionally low power dissipation for its propagation delay, compatibility with other bipolar devices, and suitability over the wide temperature ranges of military applications.

Currently, IC manufacturers are developing families of IIL digital products, including high speed 4K-bit memories and microprocessors for use where high performance is desired, even at a modest cost premium. A large variety of specialized IIL devices is expected to become available during the next year, and a fast 64K-bit memory may eventually be developed.

There is also encouraging progress in other exciting technologies. For example, the V-MOS fabrication technique, recently applied in high power junction transistors, offers the possibility of a low nanosecond cycle time memory. Both V-MOS and (double diffused) D-MOS with their high density potential have important implications for the future, such as in 64K-bit memories. Recent developments increase densities by factors of two to four, as well as provide performance advantages, by using 2-level memory structures.

Low Cost Applications

While advanced LSI devices have extended the achievable levels of complexity and sophistication as well as the performance of practical digital systems, parallel developments have occurred in simpler application areas. Manufacturers are now developing and offering basic microprocessor devices in which computer power is traded off against low cost and ease of application. Such devices are ideal for the many uses where quantities are large and unit cost savings are therefore important, and where most microprocessor offerings have substantial excess capability.

Interfacing and control represent typical generic areas for such bottom-of-the-line devices. A typical device might be a single chip standalone controller including CPU, p/ROM, RAM, and I/O, thus greatly reducing the need for additional ICs, simplifying interconnection, increasing reliability, and lowering cost. Combining analog with digital electronics on the chip will further extend this trend.

Future developments may permit use of smaller chips for these less sophisticated applications, improving production yields, and further lowering costs. Plastic packages will accelerate cost reduction, expanding LSI usage to extremely high volume and relatively unsophisticated and highly competitive consumer applications.

Where production requirements exceed many tens of thousands, and delays and expenses of development and tooling can be justified, special LSI devices can optimize chip characteristics for the application. Standard chips are now available incorporating basic semiconductor components, with specific interconnects added to order. Mask programmable "universal" chips are often a fast and satisfactory route to an optimum design. Some manufacturers are increasing the use of computer-aided design to reduce the cost and delivery time of special LSI ICs.

Conclusions

That IC devices have been accepted is indisputable. WEMA recently released figures which showed that U.S.-based semiconductor manufacturers shipped $156 million worth of IC devices worldwide during July 1976. U.S.-industry IC shipments for the first seven months of the year totaled more than $1 billion.

Continuing advances in LSI technology and chip design are so spectacular that the revolution in digital system design brought about by the microprocessor may be said to be barely under way. "Keeping up" must necessarily be a major continuing effort of the digital equipment designer.

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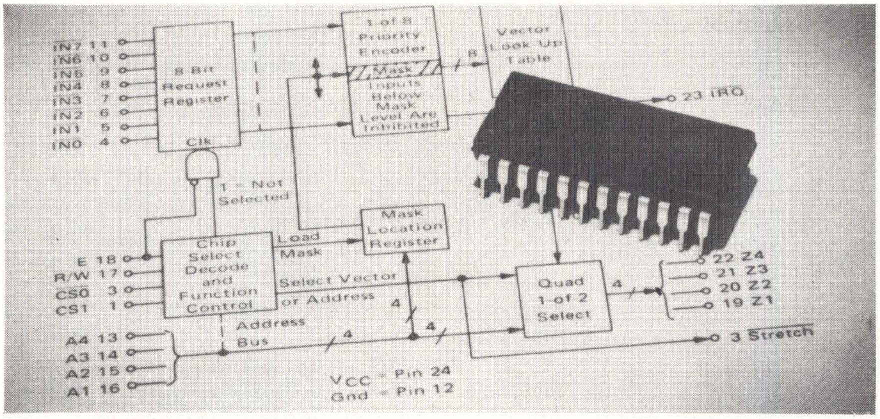
*As part of a survey on the impact of microprocessors, conducted jointly by Computer Design Publishing Corp and International Data Corp, respondents were asked what LSI devices they were using other than microprocessors and semiconductor memories. The largest single category mentioned was universal asynchronous receiver/transmitters (21%). Other data communications devices included universal synchronous and synchronous/asynchronous receiver/transmitters and a number of communications interface adapters.

Additional predominant interfaces included programmable interface adapters, I/O chips and ports, A-D and D-A converters, multiplexers, and encoder/decoders. Memories other than RAMs, ROMs, and p/ROMs included FIFO/LIFO, programmable and field programmable logic arrays, character generators, and shift registers.

Bipolar LSI Circuit Eases System Interrupt Control



Block diagram of Motorola MC8507/MC6828 priority interrupt controller (PIC). Although optimized for the M6800 microprocessor system, it may be used in non-M6800 processor applications

Prioritized control on interrupt inputs to a microprocessor system can be attained by the priority interrupt controller (PIC), a bipolar LSI circuit optimized for the M6800 microprocessor system. Basically, the MC8507/MC6828, from Motorola Semiconductor Products Inc, PO Box 20294, Phoenix, AZ 85036, eliminates the software interrupt polling routine in systems containing multiples of eight I/O devices. Functionally, it can change the interrupt vector, reserved in memory for hardware interrupts, into one-of-eight alternate vectors assigned to the I/O service routines.

The PIC modifies low order bytes of the reserved interrupt address. Second, third, fourth, and fifth least significant bits (LSBs) of the system address bus are used as inputs; a bit pattern of 1100 (fifth LSB to second LSB, respectively) is required to initiate the vector translation.

Interrupt output of each I/O device is normally connected to one of eight prioritized latching inputs on the PIC. When enabled, each interrupt will cause a unique bit pattern to be generated and substituted for the fifth through second LSB of the original interrupt vector. These eight alternate vectors are used to start the interrupt subroutines for the I/O devices.

A mask, which is programmed via the fifth through second LSBs of the address bus, can be used to inhibit any or all of the interrupts at the eight inputs. An interrupt input on an uninhibited line will generate an interrupt ($\overline{IRQ}$) output from the PIC. When this $\overline{IRQ}$ signal is accepted by an MC6800 MPU, bit pattern 1100 (fifth through second LSBs, respectively) will be put on the address bus. This allows the PIC to begin substituting the alternate vector, assigned to that PIC interrupt input, for the original vector.

Inhibited interrupts to the PIC will generate $\overline{IRQ}$s when the mask is reprogrammed to an inhibit level that is lower than the priority level of the unserviced interrupt.

An output from the PIC, called the $\overline{STRETCH}$ signal, is available to lengthen a system clock cycle ($\phi 2$ in an M6800 system) when accessing slow memories. When unselected, the PIC is transparent on the address bus and will not affect the reserved interrupt vector.

PIC is currently offered from stock in a plastic 24-pin DIP at $7.50 in quantities of 100 to 999. A ceramic version will be offered in the near future.

Circle 350 on Inquiry Card

CMOS Circuits Offer Improved Design and Utility

Additions to its Isoplanar family of CMOS circuits have been announced by Fairchild Camera and Instrument Corp's Digital Products Div, 464 Ellis St, Mountain View, CA 94042. One, the 4528 dual retriggerable, resettable monostable multivibrator, offers a typical device-to-device output pulse width variation of ±3% at V_{DD} = 15 V; and ±1% typical output pulse width variation over the commercial temperature range with V_{DD} = 15 V. Propagation delays are independent of the timing capacitor, and the device will not retrigger while the timing capacitor is discharging in response to an initial trigger input.

A second device, the 4511, is a BCD-to-7-segment latch/decoder/driver which is claimed to offer significant improvement in ac performance for additional multiplexing flexibility, and improved output drive capabilities for added application utility. Both devices meet or exceed all limits of the industry standard "B" series CMOS specifications, and are available from stock in plastic or ceramic packages in both military and commercial temperature ranges.

Other added devices, which also meet or exceed the "B" series specifications, are the 4006 18-stage shift register, 4041 quad true/complement buffer, 4043 quad NOR R/S 3-state latch, 4044 quad NAND R/S 3-state latch, 4510 BCD up/down counter, and 4516 binary up/down counter.

Circle 351 on Inquiry Card

3-Digit CMOS DVM IC Competes Economically With Analog Panel Meters

Self-contained construction of the LD130, claimed to be the first 3-digit monolithic digital voltmeter integrated circuit, reduces the cost of building meters into products to approximately $15 to $20, making the device economically competitive with analog meters. Whereas, in the past, complex circuitry and precision components had to be added to such DVM ICs to attain accuracies of 1 to 3%, a built-in temperature drift correction function in this IC maintains a typical accuracy of ±0.1% ±1 count.

The single-chip CMOS device operates as a self-contained analog-to-BCD converter, with its digit-strobed BCD outputs directly driving standard CMOS display decoder/driver units. It avoids the usual maximum 200 count limitation of 2½-digit monolithic DVMs by using the same three elements for a maximum count of 999. An autopolarity function increases the range to ±999 and automatically switches the ± sign. Auto-

The REMEX RFD 1000—Because It's Versatile. Double or single density with capacity up to 6.4 Mbits...IBM standard or 32 hole hard sectored media without drive modification...IBM compatible or expanded hard and soft sectored formats for application flexibility...Unit select daisy chain capability for maximum controller efficiency...Selectable DC negative voltage for system compatibility...Individual drive housing or two drives horizontally side by side in a 19 inch rack configuration.

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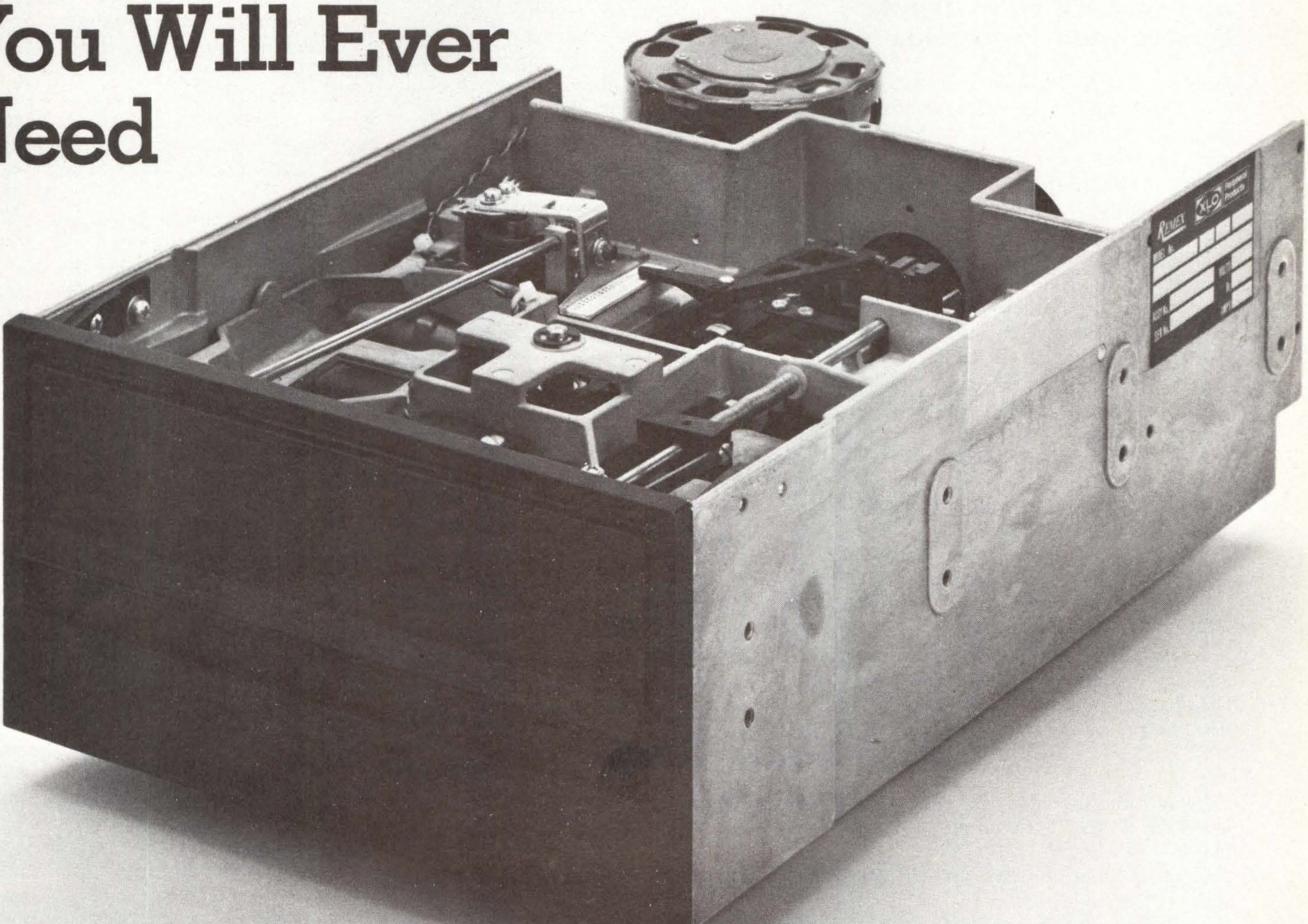

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range functions provide six decades of operation and the control can be used to switch range-scaling components and display decimal point.

Power dissipation is 26 mW typ. Since separate active analog requirements are not needed, a single or split 10-V power supply can be used; eg, a ±5-V supply is adequate for battery powered instruments. Type of voltage reference is optional: a standard zener diode fixed reference or a low power current source driving a potentiometer.

Fabrication is in an 18-pin DIP. Pricing in quantities of 100 to 999 is $8.75 each from Siliconix, 2201 Laurelwood Rd, Santa Clara, CA 95054. Delivery is from stock.

Circle 352 on Inquiry Card

Analog MUX Have Input Overvoltage Protection

Single-ended 8-channel and 4-channel differential I/O CMOS analog multiplexers, respectively, the MPC8S and MPC4D feature self-contained binary channel address decoding and are compatible with DTL, TTL, or CMOS input levels. Transfer accuracies of better than 0.01% can be achieved at sampling rates up to 200 kHz from signal sources of up to ±10-V amplitude. The user can individually enable an 8- or 4-channel group to ease channel expansion in either single-mode or multi-tiered matrix configurations.

Digital and analog inputs are failure protected by channel interaction during overvoltage conditions as well as in the event of power loss. Operating power dissipation at 100 kHz is 15 mW (7.5 mW standby).

Both units are accuracy-compatible with 12-bit systems and have typical access times of 500 ns. Break-before-make switching protects input sources. Off-channel isolation is typically 65 dB. Supply range is ±5 to ±20 V; I/O range is equal to supply voltage.

They are specified for operation over the 0 to 75°C range and are housed in 16-pin DIPs (pin- and package-compatible with the 508/509 series). Available from stock from Burr-Brown, PO Box 11400, Tucson, AZ 85734, the devices are priced at $14.00 for 1 to 24, $12.20 for 25 to 99, and $10.00 for 100 or more.

Circle 353 on Inquiry Card

Mil-Range FPLAs Offer Improved I/O Abilities

Full military temperature range versions of field programmable logic arrays (FPLAs), from Signetics, 811 E Arques Ave, Sunnyvale, CA 94086, are claimed to offer the best performance now available over the −55 to 125°C range. Key specifications include 600-mW typical power dissipation and 80-ns maximum access time. S82S100 has a 3-state output and S82S101 is an open collector version.

The Schottky-TTL arrays, based on nichrome fuse technology, are collections of AND and OR logic gates whose internal and external input connections can be arbitrarily programmed by the user. They feature a single 5-V supply operation, and differ in organization from any other FPLAs now on the market.

They are organized with 16 inputs and eight outputs, whereas other devices typically have 14 inputs. This I/O configuration allows direct manipulations of two data bytes and provides the capability to scan an address field 65,536 words deep.

Although the organization also includes 48 product terms, the number used or shared among the outputs does not affect speed or power dissipation. By contrast, competitive FPLAs typically dissipate 4 mW more power for each product term used. In addition, a chip-enable input eases the expansion of inputs and product terms and permits application of the 3-state device to bus-organized systems.

Both devices are available from stock as full military temperature and MIL-STD-883B processed units in 28-pin ceramic DIPs. In quantities of 100 up, prices are $48 for the S82S100 and $54.25 for the S82S101.

Circle 354 on Inquiry Card

64-Bit Multiplier IC Meets Requirements of High Speed Processing

Complete 8- by 8-bit parallel multiplication can typically be performed in 130 ns by the MPY-8, a monolithic LSI circuit developed by the Electronic Systems Div of TRW Inc, 1 Space Park, Redondo Beach, CA 90278. The monolithic multiplier circuit includes more than 4500 components on a single 190-mil square silicon chip. Two 8-bit words can be multiplied to generate a double precision product for military and commercial high speed processing applications and for instrumentation.

Inputs and outputs are fully TTL-compatible. Outputs have 3-state control. A single 5-V power supply is used. Emitter-follower logic (EFL) is used internally in the multiplier to achieve high speed and very low power consumption. Non-inverting EFL AND-OR gates eliminate delay times in other logics requiring signal inversion. Multiplication is carried out by an array of full adder cells using the successive add algorithm.

Organization is as a 4-port device in a 40-lead ceramic DIP. Four independent D-type registers are used for input loading and storage of the output product. Input registers have separate single-phase clock controls, and output registers have a common clock control. If desired, a single 8-bit bus can be used for both loading and transmitting the product using a sequential mode on the control signals.

The multiplier is a 2's complement machine with the sign bit occupying the most significant bit position. Speed/power product for the bulk of the logic is under 3 pJ. Typical power consumption is 1.8 W (over 900 equivalent gates).

Samples are available 30 days from receipt of order. Current prices for sample quantities are $100 for 1 to 24 devices and $85 for 25 to 99 devices.

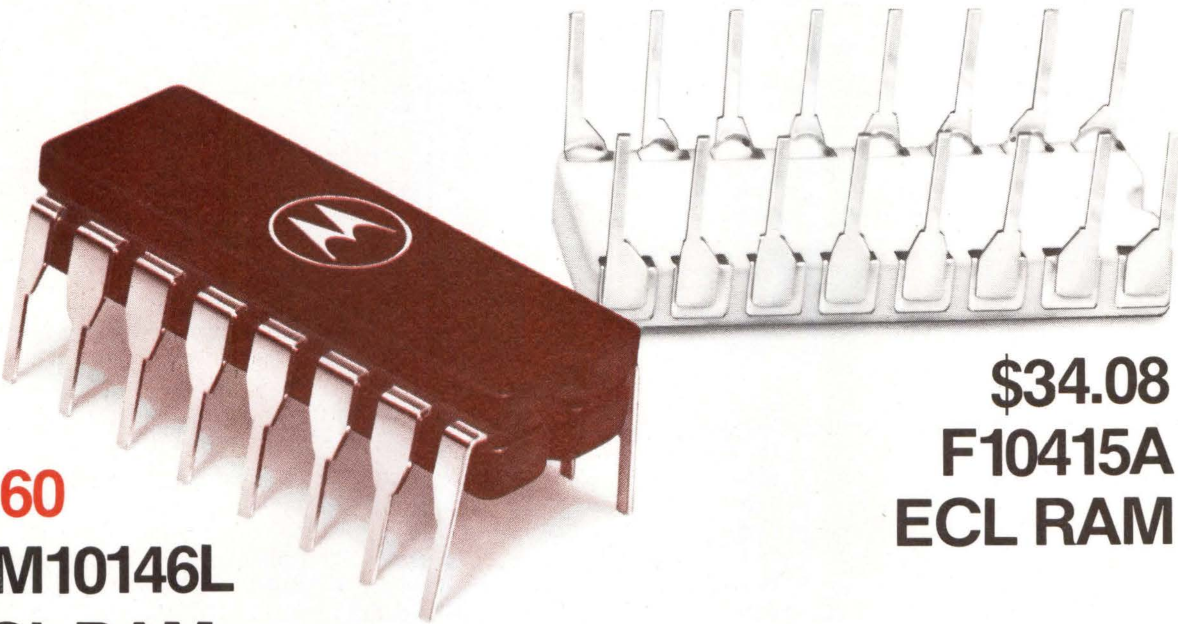
Circle 355 on Inquiry Card

Linear ICs Meet Interface Requirements

Five interface circuits—four dual memory drivers (55/75326 and 55/75327) and a dual line driver (75150)—have been announced by the Linear Integrated Circuits Div of Fairchild Camera and Instrument Corp, 464 Ellis St, Mountain View, CA 94042. Several packaging or temperature-range versions of each are available.

All of the dual memory devices can sink up to 600 mA. 55/75326 versions operate from single 5-V supplies. Output-transistor base current can be increased by connecting an external resistor. Each output collector is protected from voltage surges during inductive switching by

Your 1K ECL RAM struggle is over.



$15.60
MCM10146L
MECL RAM

$34.08
F10415A
ECL RAM

Now Fairchild's begins.

It's no effort to get 1K ECL RAMs anymore.

Now that you can get them from a production house that *thinks* like a production house. Motorola.

Many of you waited for us to introduce this part so you could have ensured deliverability and producibility. Well, you've got 'em.

Together with an unbelievably low price... neck-and-neck even with pricing for F-troop's fastest T^2L RAM. Look it up. That's gonna surprise a lot of people. Including the former first source.

Our producibility is so good we can sell it for less. And we knew once you saw our unit you'd choose it over theirs. For obvious reasons.

It's what you've been battling for all along.

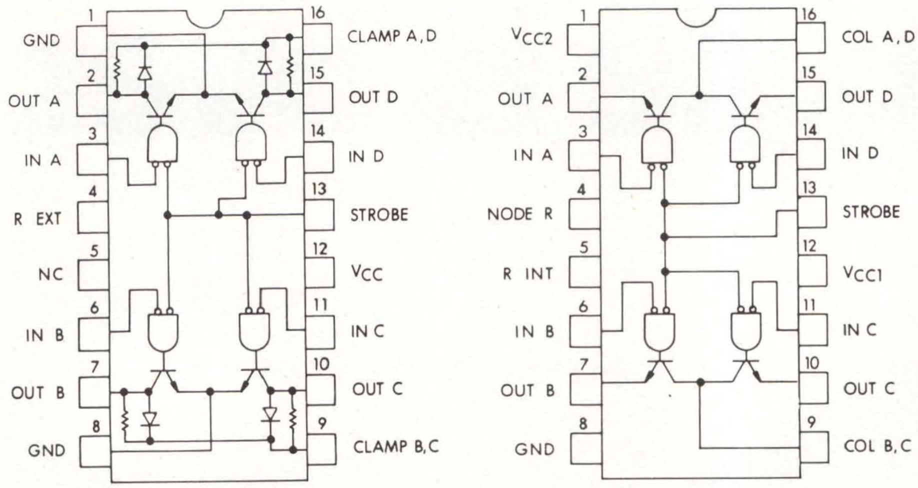
Send for complete data from Motorola Semiconductor Products, Inc., Box 20912, Phoenix, AZ 85036. Or check with your in-plant data center or your authorized distributor.

Maybe we took longer. But we fought to make it available and cheaper, and that's what counts in the real world.

Doesn't it Fairchild?

MOTOROLA Semiconductors
—*still* the production house

MECL is a trademark of Motorola Inc.
All prices 100—999, latest available.



Schematic diagrams of Fairchild dual memory drivers. 75326 (left) sinks up to 600 mA and operates from single 5-V supply; 75327 (right) sinks or sources up to 600 mA and operates from 5- and 4.5- to 24-V supplies

a clamp diode in parallel with an internal pull-up resistor.

55/75327 memory switches can function as either sink or source drivers at up to 600 mA, and operate from two supplies: one 5 V and the other 4.5 to 24 V. An internal base-drive resistor on the chip can be used by connecting two pins externally.

Devices are available in either ceramic DIP or military flatpack for the military temperature range. For the commercial market they are available in both ceramic and plastic DIPs, priced at $3.14 and $2.62, respectively, in quantities of 100.

The 75150 dual line driver satisfies interface requirements between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. It permits a transmission rate of 20,000 bits/s with a full 2500-pF load.

Logic input is compatible with most TTL and DTL families. Operation is from 12- and −12-V power supplies. The device is a pin-for-pin replacement for the SN75150 and is available from stock in ceramic or plastic DIP and ceramic or plastic mini-DIPs. Pricing in 100 quantities is $2.07 in ceramic and $1.72 in plastic DIPs and $2.00 in ceramic and $1.67 in plastic mini-DIPs.

Circle 356 on Inquiry Card

Bipolar RAMs Meet High Speed/Low Power Scratchpad Requirements

Low power 64-bit bipolar memories with full military capabilities, the DM-74LS289 and DM74LS189 random-access memories, with open collector and Tri-State[R] outputs, respectively, are replacements for the older DM5489D and DM7599D. Although they require only 25-mA max input power, they maintain the 35-ns speed of the older devices. Available from National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051, these devices can be applied to scratchpad applications which require the high speed of TTL plus the low power of Schottky technology.

Both RAMs are fully decoded and feature a chip-enable input to simplify the decoding needed to achieve the desired system organization. They are available from stock, priced at $3.73 each (in lots of 100) for commercial parts, and $8.00 each for the military temperature range.

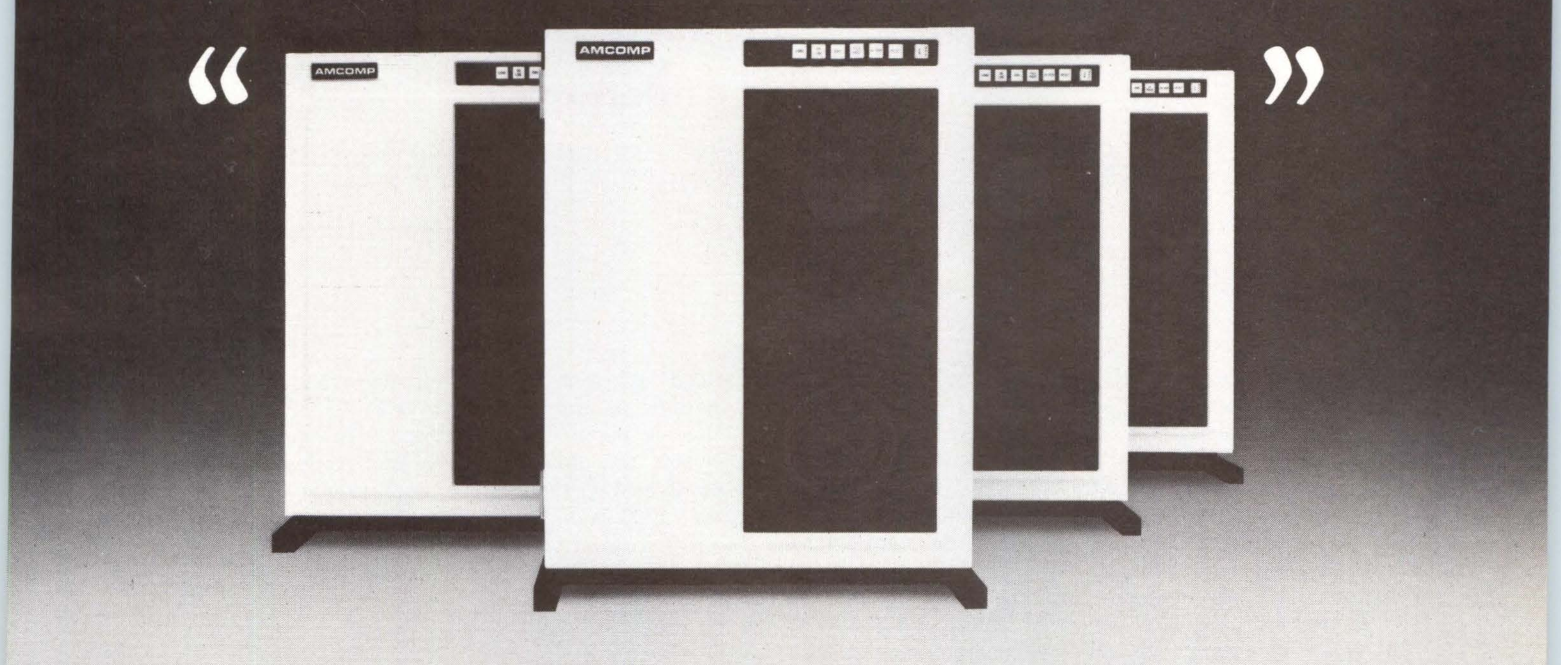
Custom MSI Circuits Ease Design Problems For Low Volume Needs

Two-week delivery (after receipt of customer's masks) is promised for low volume supplies of custom medium scale integrated CMOS circuits by Mosfet*Micro*Labs of Penn Centre Plaza, Quakertown, PA 18951. Using company supplied layout rules and test circuits, the customer designs standard elements on one chip such that the metal pattern can be interconnected in different circuit configurations by changing only the metal mask. The company then fabricates CMOS wafers to meet test transistor requirements from the mask sets. Circuit testing is performed by matching electrical results of probed chips with breadboarded ICs.

An oxide/nitride gate dielectric is claimed to provide much improved stability. Allowing a maximum change in flat band voltage of 0.5 V at conditions of 250°C at ±30 V (cooled to room temperature) the devices nominally change less than one-tenth this value. A planar oxide process virtually eliminates metal discontinuity over stepped oxides. After field testing of the custom part, the layout can be improved to optimize yield if high volume needs develop. □

Circle 357 on Inquiry Card

Our commitment to the tape drive market can be summed up this way:



We make four basic tape drives. One of them is just the one you want.

Because the options we've engineered for our basic four effectively give you a choice of over 400 configurations.

Speeds from 12.5 to 125 ips. Tension arm or vacuum column. A variety of electronics options. And more.

Yet with all the differences from drive to drive, there are a number of things the same in every drive.

Simple one-hand loading, dynamic braking, linear sensors and servos, and other engineering advantages.

A near 80% parts commonality. Which makes your spares stocking, training, and servicing a lot easier. An industry-unsurpassed commitment to quality—given meaning by our industry-unsurpassed 13 month warranty. And backed by 24 hour a day, 7 days a week field service.

AMCOMP Tape Drives. Giving you exactly what you want rather than selling you just what we have.

To find out more about the tape drives, or other products and services we have, please contact your nearest AMCOMP office, or AMCOMP, INC., 686 West Maude Avenue, Sunnyvale, CA 94086, phone (408) 732-7330.

AMCOMP. Our strength is our commitment. And our commitment is strong.

AMCOMP

Microcomputer Interfacing: Microcomputer Interrupts

David G. Larsen
Virginia Polytechnic Institute & State University

Jonathan A. Titus
Tychon, Inc

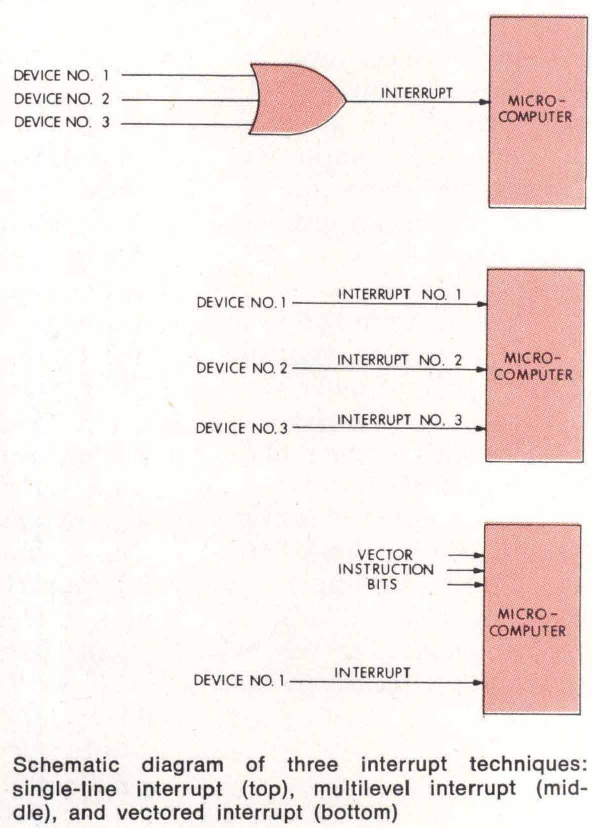
Peter R. Rony
Virginia Polytechnic Institute & State University

This month's column is the first of several that will focus upon the concept of an interrupt. When used in the context of a computer, an interrupt can be defined as the suspension of normal program execution in order to handle a sudden request for service, ie, assistance, by the computer. At the completion of interrupt service, the computer resumes the program from the point where it was interrupted.[1] This specific use of interrupt is consistent with the general meaning of the term: to stop a process in such a way that it can be resumed.

A given computer typically will communicate with a variety of external I/O "devices." If it is a minicomputer, it may communicate with a teletypewriter or alphanumeric keyboard, CRT display, printer, floppy disc, and perhaps one or more laboratory instruments. If it is a microcomputer, it may communicate with smaller devices—motors, solid-state relays, pushbutton switches, display lights—within a larger machine or instrument. When used as a replacement for discrete logic devices in a complex digital circuit, a microcomputer may communicate with other TTL integrated circuit (IC) chips such as latches, flip-flops, and 3-state buffers.

When communicating with external I/O devices,[2] microcomputers can operate in two general modes, polled and interrupt. Polling is the periodic interrogation of each I/O device that shares a communications link to a microcomputer to determine whether it requires servicing. A microcomputer sends a poll that has the effect of asking the selected device, "Do you have anything to transmit?" "Are you ready to receive data?" and similar questions. When a microcomputer services a polled device, it simply exchanges digital information with the device in a manner that is prescribed by software in a subprogram or subroutine called a software driver.

In polled operation, the microcomputer sequences through the devices tied to the microcomputer looking for individual devices that need servicing. When it finds a device that requires service, it stops sequencing, calls a software driver, and services the device. Once it is finished, the microcomputer continues checking the devices. Polled operation is most useful with relatively slow devices that do not require frequent service, do not need attention from the microcomputer for excessive periods of time, and can wait to be serviced. Advantage is taken of the difference in operating speeds between the microcomputer and the I/O device. Most common I/O devices are much slower than microcomputers. For example, in 100 ms (teletypewriter response



Schematic diagram of three interrupt techniques: single-line interrupt (top), multilevel interrupt (middle), and vectored interrupt (bottom) time) an 8080A-based microcomputer can execute approximately 20,000 instructions when operated at a clock rate of 2 MHz. Although a microcomputer may appear to be doing several things simultaneously, this is only an illusion since it can manipulate data much faster than most I/O devices can respond to changes in data. A single computer can perform only one task at a time.

In interrupt operation, the microcomputer juggles the demands of the external I/O devices. There is a distinction between slow devices that require infrequent servicing and high speed devices that demand almost constant attention from the microcomputer. The most appropriate description for interrupt operated systems is that they are asynchronous, ie, they lack a common synchronizing signal and therefore give rise to generally unexpected or unpredictable program execution within the microcomputer. In an asynchronous device the speed of operation is not related to any frequency in the system to which it is connected.[3] Use of asynchronous devices is the rule rather than the exception.

Priority can exist in interrupt operation; all I/O devices can be ordered in importance so that some devices take precedence over others. In contrast, there is usually no priority in polled operation; once a device is serviced, it waits its turn until all others are sequenced and, if necessary, also serviced. Time between the interrupt request by a device and the first instruction byte of the software that services it is known as the interrupt response time. For a high speed device that has high priority, the response time can be very short, less than a millisecond. For a low speed device that has low priority, the response time is variable, since it depends upon the demands placed upon the microcomputer by all higher priority devices.

Three commonly used microcomputer interrupt techniques are the single-line interrupt, multilevel interrupt, and vectored interrupt (see Figure). In the single-line interrupt technique, multiple devices must be OR connected to a single interrupt line to the microcomputer. Once an interrupt signal is received, all interrupt devices are polled to determine which one caused the interrupt. Software priorities may be assigned to the various interrupting devices, so that the first device polled that needs service is the one that receives the attention of the microcomputer. A common term used for the part of a program that polls interrupt devices is flag checking routine. (The concept of a flag will be discussed in a future column.) At the moment, consider a flag to be a single-bit memory that indicates when an operation has been completed or when a condition has been attained.

In the multilevel interrupt technique, there exist several interrupt lines to the microcomputer, each line being tied to a separate I/O device flag. The microcomputer need not poll the devices to determine which one caused the interrupt. This is done internally within the microprocessor chip. Depending upon the nature of the microprocessor chip, this can be a very fast interrupt technique, but it is somewhat difficult to expand.

A vectored interrupt causes a direct branch by the microcomputer to the part of the program that services the interrupt. This interrupt technique requires external IC chips to supply the memory address of the interrupt service routine as well as to set the priority. With the 8080A microprocessor chip, eight different service routine addresses can be readily specified, although one of these addresses coincides with the reset address for the microprocessor, location zero. The Intel 8259 programmable interrupt controller, which became available commercially in July 1976, should be considered by those who are interested in vectored interrupts.

Use of interrupts should be considered very carefully. More complicated software is invariably required. For example, the status of the microprocessor chip generally has to be saved at the time that the interrupt occurs. This means that contents of the accumulator, flags, and registers must be placed in a specified region of memory from which they can be retrieved at a later time, after the interrupting device has been serviced. Pay attention to priorities: devices that require high priority and need immediate servicing should be given the highest priority; other devices, such as teletypewriters, should be low priority. Also, if too much is attempted with an interrupt system, the microcomputer may become "interrupt bound," which means that it is working only on interrupt tasks and not on the main task. It should be working on the main task and only infrequently servicing interrupt requests.

Finally, we would like to provide an example of an interrupt system. Assume that the microcomputer is performing mathematical computations on 7-bit ASCII numbers that are entered via a UART chip[4] connected to a teletypewriter operated at 110 baud, or 10 ASCII numbers per second. Data exchange between the microcomputer and the UART can be performed in 20 to 30 μs, which leaves 99.97 ms for the microcomputer to do other things. With the Intel floating point package, for example, each floating point multiplication or division can be performed in 2 to 5 ms with an 8080A-based microcomputer operating at 2 MHz. Sixteen-bit binary multiplications and divisions can be performed even faster. Therefore, it is appropriate to consider that the main task of the microcomputer is to perform such computations, and that it can devote 0.05 to 0.10% of the time to servicing the interrupting teletypewriter. Less attractive alternatives are for the microcomputer either to poll the UART or to wait for a change of state of the UART data ready or transmitter buffer empty flags.

Interrupts also are effective for use with devices that provide data to a microcomputer but which have no buffer of their own to store it. Existing data must be removed from the device and stored in the microcomputer quickly before a new data word can be generated by the device. One example of such a device is an analog-to-digital converter in which conversions are clocked by an external clock at repetitive time intervals.

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2. D. G. Larsen, P. R. Rony, and J. A. Titus, "Microcomputer interfacing: Microcomputer I/O devices," *American Laboratory,* Nov 1975, p 100
3. Rudolf F. Graf, *Modern Dictionary of Electronics,* Howard W. Sams & Co, Inc, Indianapolis, Ind, 1972
4. D. G. Larsen and P. R. Rony, "Computer interfacing: The universal asynchronous receiver/transmitter (UART)," *American Laboratory,* Feb 1975, p 113

This article is based, with permission, on a column appearing in *American Laboratory* magazine.

Single Board Computer Features Full Multiprocessor Capability

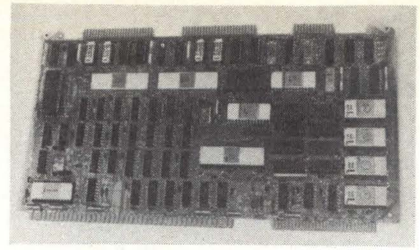
SBC 80/20 is a second generation complete OEM single-board computer containing CPU, memory, and programmable parallel and serial I/O. The system includes a variety of high performance circuits—multimaster control logic, programmable interval timer, and programmable priority interrupt controller. It can operate as a standalone, 8-bit general-purpose computer, or in a multiprocessor system containing up to 16 master subsystems.

Basic subsystems similar to those of the SBC 80/10 (see *Computer Design*, Mar 1976, pp 116, 118) are included in addition to major enhancements. The resident multimaster bus control logic allows four 80/20s to share the system bus. An optional priority network extends the number to 16. Bus controller has its own clock, allowing controllers of different speeds to operate as bus masters; asynchronous data transfers permit masters to operate at their own speeds. Master-slave capabilities can be used for DMA as well as multiprocessing.

Maximum design flexibility is provided by the use of programmable LSI devices for I/O interfacing and peripherals control, which allow system operating configurations to be customized with software. The addition of LSI peripherals increases the onboard intelligence to handle system tasks and to control external peripherals, thereby reducing CPU real-time loading and increasing throughput and real-time responses.

Since each system contains its own local memory and I/O, much of the processing occurs onboard without reference to the system bus. Several computers together can simultaneously execute programs without speed reductions due to heavy bus loading. Interprocessor communication, when necessary, occurs via global memory and the system bus.

Measuring 6.75 x 12", the board has a CPU with system clock, controller, and bus expansion drivers; 2K bytes of read/write data memory in static RAMs; sockets for up to 4K bytes of EPROM or ROM; 48 programmable parallel I/O lines with sockets for interchangeable quad line drivers and line terminators; programmable synchronous/asynchronous serial data I/O with

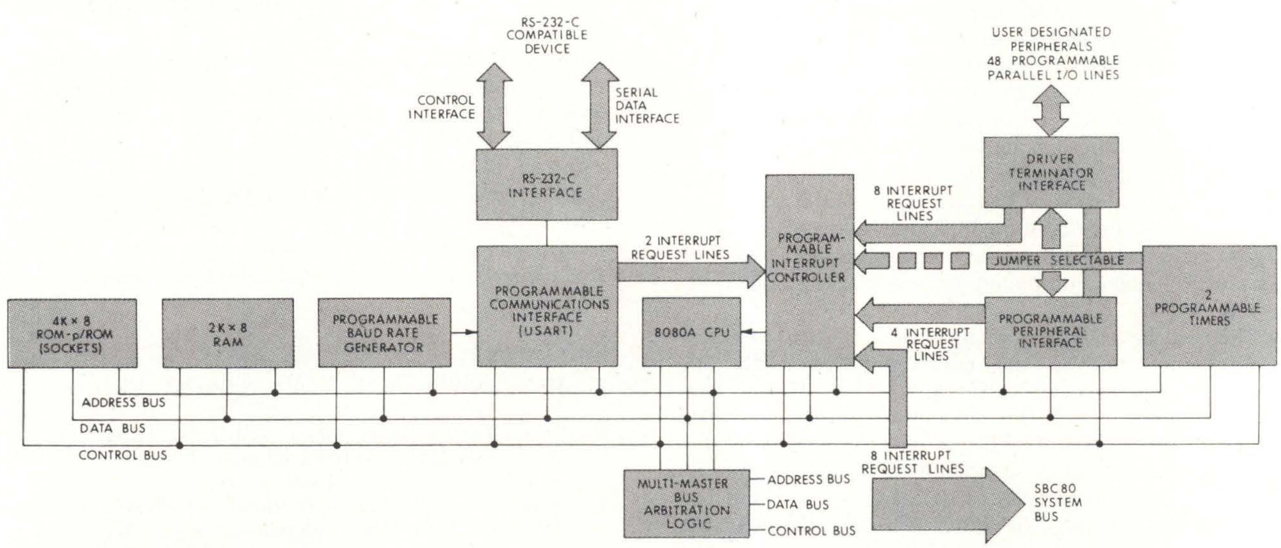


SBC 80/20 is second generation single board computer complete on 6¾ x 12" PC card. Featuring multiprocessing capability, card contains CPU, memory, and programmable LSI devices for I/O interfacing and peripherals control

RS-232-C compatible interface and fully software-selectable baud rate generation; 8-level programmable interrupt control; two programmable interval timers/event counters based in 16-bit binary/BCD counters; auxiliary power bus and memory protect control logic for battery backup data memory; and compatibility with the full line of optional memory and I/O expansion boards.

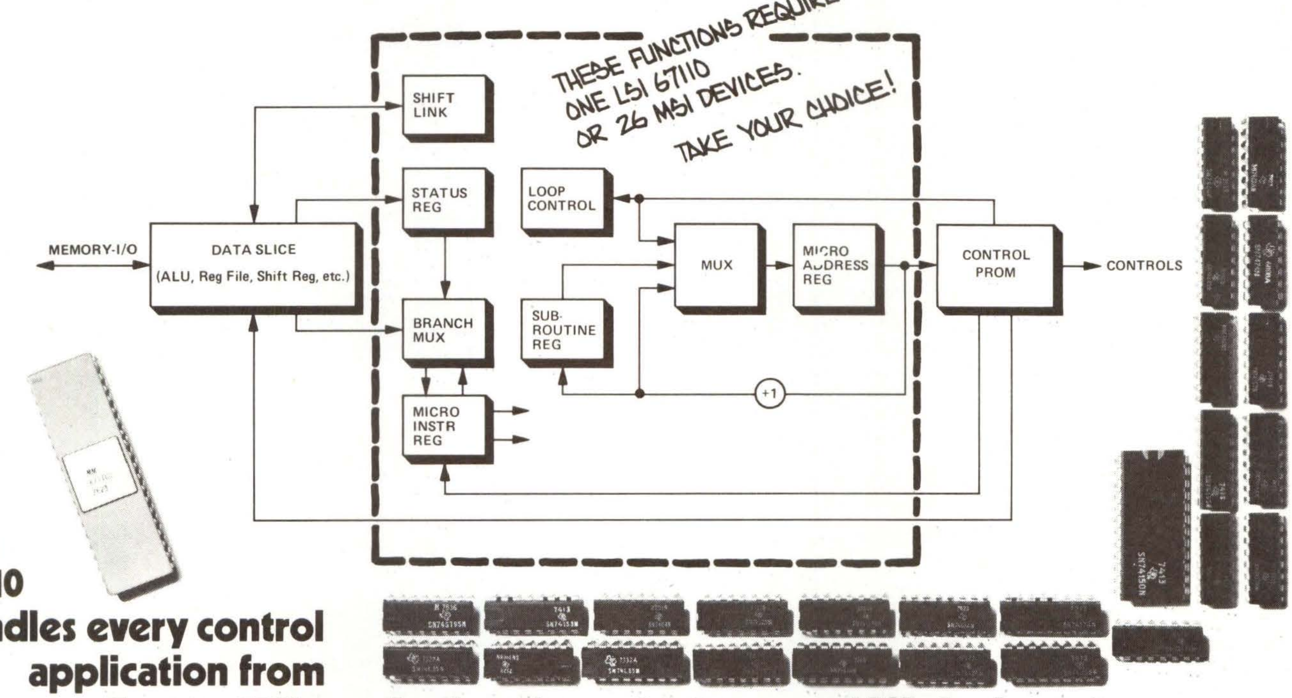
The 8080A 8-bit parallel n-channel MOS CPU has 8-bit general-purpose registers, accumulator, 16-bit program counter for up to 64K bytes of memory, and 16-bit stack point and manipulation instructions. Instruction execution time is 1.86 μs.

A programmable interval timer eliminates most problems associated with monitoring and managing I/O servicing and external events and



Block diagram of SBC 80/20 single board computer. Card contains multi-master bus arbitration logic, two programmable timers, and programmable interrupt controller. Multiple systems can be interconnected as a multiprocessor or distributed processing system

The Only Bipolar Microprogram Controller



The 67110 Handles every control application from discs to CPUs.

And replaces 26 or more MSI devices.

Applications

CPU
Process Control
Disc Control
High Speed Printer Control
CRT Controller
Signal Processing Control

DEVICE	TEMPERA-TURE	100 QUANTITY PRICE
67110J	Commerical	$25.00
57110D	Military	$55.00

Features

- Works with any bit slice microprocessor such as MMI 6701, 2901, 3002.
- Works as a stand alone non-arithmetic controller
- Directly addresses 512 words of microprogram storage
- On-chip five bit loop counter for program looping routines
- Data shift linkage for arithmetic and logic shifting with 4 bit slices
- Microsubroutine and four way branch capabilities
- Very High Speed — 33 MHz

Information

For more information about this revolutionary microprogram controller and about other members of our growing family of LSI logic devices that will eventually replace all MSI logic, call, TWX or write:

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rates. One of the three 16-bit timer/counters within the timer operates as a programmable baud rate generator; the other two can function independently. Timing range is approximately 2 μs to over 60 ms, which can be extended to 1.1 h by cascading the two timers.

A programmable interrupt controller handles vectoring control of up to eight priority interrupt levels for the CPU. It generates interrupt vectors and resolves priorities, changing them as needed. Four modes which can also be changed dynamically are the fully nested, autorotating, polled mode, and software assigned priority levels with masking of individual levels.

Manufactured by Intel Corp, Microcomputer Div, 3065 Bowers Ave, Santa Clara, CA 95051, the SBC 80/20 and associated products are available from stock. Price ranges from $895 for a single unit to $520 in quantities of 100; OEM discounts apply to quantities over 10.

System programming, which is the only development task associated with using the computer, can be done directly with the Intellec[R] Microcomputer Development, ICE-80 In-Circuit Emulator, and resident software. An Intellec resident software package, which uses the company's PL/M high level language or assembly language, is also being introduced. It includes PL/M resident compiler, and ISIS-II diskette operating system containing DOS system, text editor, macroassembler, and linker, loader, and library manager.

Circle 170 on Inquiry Card

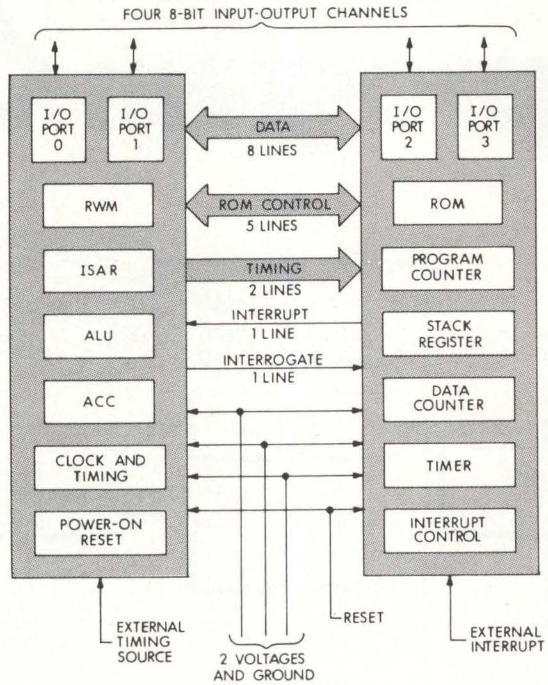


Fig. 1 2-chip microcomputer. Diagrams of the Fairchild 3850 (left) and 3851 (right) show major functional parts of simple computer

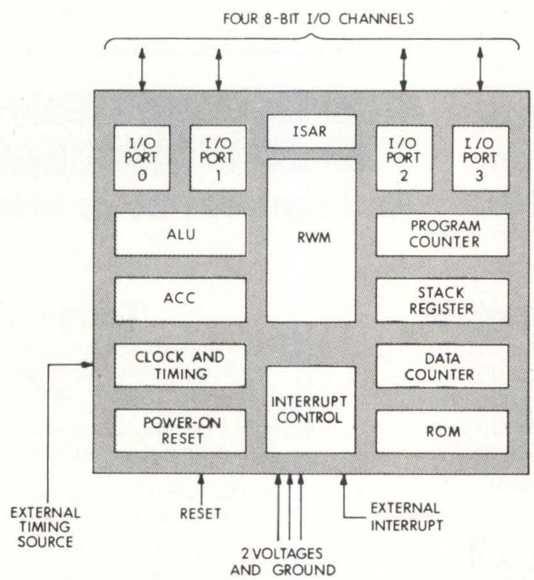


Fig. 2 1-chip microcomputer. All functions executed by 2-chip F8, with the exception of smaller counters, have been integrated on single chip

n-MOS Technology Combines 2-Chip F8 Into 1-Chip Version

Fabricating what is claimed to be the first true computer-on-a-chip, Fairchild Camera and Instrument Co, Systems Technology Div, 1725 Technology Dr, San Jose, CA 95110, has announced a 1-chip version of the F8. Describing the device in a paper presented at the IEEE Computer Conference (Compcon) in September, Thomas A. Longo, the company's vice president and technical director, points out that this device, as well as the 2-chip F8, is different from the majority of microprocessors. Other units consist of a computer system's CPU, reduced to fit on one or a few ICs, and require numerous external circuits to function.

In its most elementary form, the original F8 family consisted of a processing unit (part number 3850) and a program storage unit (part number 3851). The 2-chip F8, however, did not fit many applications in which space was at a premium. Many of the 40 pins on each of the two packages were devoted to signals between chips, not to or from the outside. Furthermore, due to partitioning of functions between chips, some functions had to be duplicated.

In order to meet these conditions, the company decided to merge the two chips into one, which resulted in the type 3859. In the original F8, one chip had an ALU, two I/O

ports, a 64-byte R/W memory, and clock, and the other had two more I/O ports, a 1K-byte ROM, timer, and interrupt circuitry. The new version puts all of these on one chip. Due to limited space, there are three registers of 10 bits each—a program counter, data counter, and stack register—rather than 16 bits as in the 2-chip version. At 16 bits, the program and data counters can identify items stored in up to 65K of memory; at 10 bits, they are limited to 1K, which is adequate for the unit's intended applications. The elimination of unnecessary and duplicated functions reduces the logic transistor count by about 7.5%; the area of the transistors on the chip is reduced about one-quarter. Power dissipation and cycle time have also been reduced.

The key to achieving this capability on a single chip is the n-MOS Isoplanar fabrication process which was also used in the 2-chip F8. In the process, the active area of each transistor is slightly higher than the surrounding chip surface, reducing the height of the "steps" over which the upper metallization layer must make contact with the semiconductor substrate; in addition, these steps are given rounded edges by a reflowing technique, reducing the probability of metal cracking, and therefore device failure during subsequent fabrication steps or in the field. By this means, the number of transistors per chip increased from about 9500 in the 2-chip F8 to over 18,000 in the 1-chip version.

Shipments of the 1-chip F8 will begin shortly after the first of the year; the 2-chip version remains in production for more complex applications.

At Compcon, Longo predicted that by 1978 single IC chips would be in production with as many as 30,000 transistors. He also hinted that a 1-chip microcomputer with a 2K-byte ROM, capable of running programs twice as long as either present F8 version can, might appear next spring. Details, of course, remain speculative.

Meanwhile, according to some reports, the Microsystems Div of Motorola, Inc, Austin, Tex, and Intel Corp, Santa Clara, Calif, were working on 1-chip microcomputers of their own, but were not quite ready to talk about them by the time of Compcon.

Circle 171 on Inquiry Card

Analyzer/Controller Is Compatible With 6800 µProcessor Systems

Both the functions and conveniences of a sophisticated minicomputer console, as well as those features oriented toward development of microprocessor systems, are contained in the 6800 microprocessor analyzer (model MPA AO 6800). Designed to meet all microprocessor system problems from development to field service, the development and debugging tool provides extensive capabilities previously unavailable.

Standard functions include setting and examining registers (A and B accumulators, index, stack pointer, condition codes, and program counter), examining and depositing in memory (65K), hardware breakpoint and monitor, run/halt, and single step. Displays are provided for system status, analyzer status, address bus, and data bus, with an optional hexadecimal display for both address and data.

Special control functions also are furnished. An execute control allows the insertion of instructions independent of normal program flow, and an optional sequence recorder stores the addresses of up to 128 instructions, and can display the program sequence forward or backward.

Manufactured by A O Systems, Inc, 1736 Front St, Yorktown Heights, NY 10598, the instrument can be connected to any 6800 microprocessor system without placing constraints on the system hardware or software design. Accessories enabling portability include a DIP clip buffer probe that attaches directly to the microprocessor chip, and a field service case with power supply and cables.

Circle 172 on Inquiry Card

Resident Compiler Simplifies Programming of the 8080 µComputer

FORT/ /80, a resident FORTRAN compiler designed to run on any 8080 system, complies subset ANSI FORTRAN IV, producing 8080 machine object code. The code can then be loaded into p/ROM-ROM or executed directly on the 8080; this allows users to program problems in FORTRAN directly on their in-house development systems. Although the code generated by the compiler is efficient compared with assembly language code, the facility exists to link inline machine code into a FORTRAN program. This allows critical segments to be directly coded for optimal throughput.

Since the need for timesharing services is eliminated, this high level language software tool reduces software development, debugging, and documentation costs. In addition, software maintenance and upgrading can be accomplished easily. A library of subroutines and functions is available which allows the user to utilize supplied functions rather than rewrite his own.

Occupying less than 12K of memory, the compiler requires only 16K (compiler and workspace) for operation. Unified Technologies Inc, 4800 Dundas St W, Suite 209, Islington, Ontario M9A 1B1 Canada is providing a single- and double-byte integer arithmetic; an optional IBM-standard floating-point package will be available in the fourth quarter of 1976.

Circle 173 on Inquiry Card

Standalone System Offers Built-in I/O Peripherals

A fully configured, portable microcomputer, DE68 is a standalone system equipped with built-in I/O support peripherals which allow it to offer more than just an interface to an external CRT terminal or teletypewriter. Microperipherals include a 96-character keyboard, miniature cassette tape system to store up to 100K bytes of program or data per cassette, and 20-column alphanumeric display to operate system interactive communication.

Announced by Digital Electronics Corp, 415 Peterson St, Oakland, CA 94601, the system is structured around the 6800 microprocessor. In addition

CORTRON IS WRITING THE SOLID STATE KEYBOARD SUCCESS STORY

A new name in keyboards, CORTRON actually has a history dating back to 1968, when Illinois Tool Works Inc. made news with the introduction of its first solid state keyboard through its Licon Division. ITW has emerged as a major producer of solid state keyboard products and has supplied thousands upon thousands of custom-designed keyboards to meet specific customer requirements.

CORTRON DIVISION FORMED BY ITW

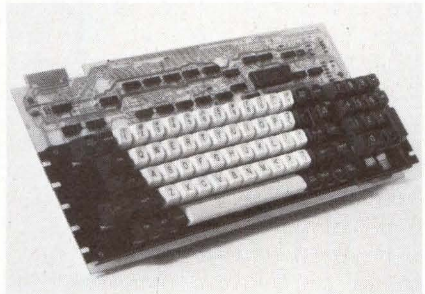
With a strong market demand and a promising future for keyboard products, ITW formed a new division, CORTRON, to handle full responsibilities for electronic keyboards and key switches. Following a proven ITW strategy, CORTRON concentrates a special division team of experienced Licon design, manufacturing and marketing people on this new major business opportunity.

KEYBOARD MARKET DIVERSIFIED

Typical applications for CORTRON™ Keyboards include data and word processing, computerized accounting, production and inventory control systems, retail point-of-sale and remote banking terminals, airline reservation and seat assignment stations, typesetting and text editing systems. And new applications are continually surfacing.

PROVEN PRODUCT RELIABILITY

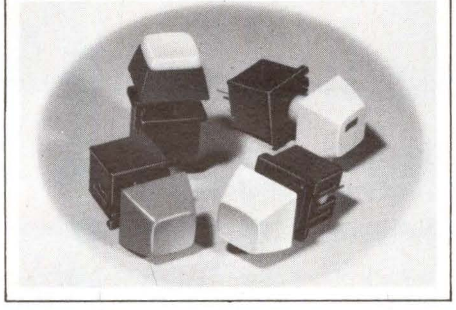
The CORTRON Division offers proven keyboard products with an established reputation for excellence and reliability. The



CORTRON Series 555 Solid State Keyboard is a sophisticated electronic device. Its high reliability protects against costly service calls and the hardship of downtime. The low profile alpha numeric keyboard has the human engineered "feel" required by your marketplace. This promotes speed, accuracy and greater operator productivity.

CORTRON KEY SWITCH MAKES THE DIFFERENCE

The CORTRON Contactless Key Switch is the heart of the solid state keyboard. The CORTRON



Key Switch is respected throughout the industry for its ultra reliable 100 million cycle life rating. Utilizing a ferrite core switching technology, the key switch is mechanically simple with only four basic parts.

CORTRON RESPONDS TO CUSTOMER NEEDS

Since keyboard products are CORTRON's only business, the ITW Division is highly responsive to individual customer needs and requirements. CORTRON offers expert application engineering assistance, and has the high volume keyboard production capability so essential to large customer demands. Further, the division is backed by the resources of ITW, a worldwide corporation. Whether you want to buy keyboards or build them, CORTRON can supply the key elements necessary to success. For complete details, contact CORTRON, A Division of Illinois Tool Works Inc., 6601 West Irving Park Road, Chicago, Illinois 60634. Phone: (312) 282-4040. TWX: 910-221-0275.

CORTRON is writing the solid state keyboard success story.

TO BE CONTINUED . . .

CORTRON
A DIVISION OF ILLINOIS TOOL WORKS INC

THE KEYBOARD PROFESSIONALS

CIRCLE 59 ON INQUIRY CARD

to the standard 1K bytes of read/write memory (expandable to 4K, 8K, or 32K), the computer features DEbug—a 5.5K-byte p/ROM operating system. DEbug firmware includes a mnemonic translator which allows software to be written and debugged entirely in the assembly language mnemonics of the 6800 microprocessor. Selectable memory entry/display modes allow communication in assembly mnemonics, hexadecimal notation, or ASCII characters. The command set simplifies software development. Commands include memory examine and change, search, move memory block, and tape commands; others permit setting multiple breakpoints, software single step, and tracing 6800 MPU register activity.

Computer is packaged in an attache-style carrying case. Bus lines are available on a single edge connector for direct I/O expansion as needed. Programmed, interrupt-initiated, and DMA data transfers are possible. An optional Micro-Printer provides built-in hardcopy output capability. An educational package includes a teaching module and manual for microcomputer training.

Circle 174 on Inquiry Card

Add-On Modules Are Available for Learning System

Three preassembled, add-on modules—controller, memory, and input/output—have been announced by Texas Instruments Inc, PO Box 5012, Dallas, TX 75222 for the Microprogrammer Learning Module (see *Computer Design*, Mar 1976, p 124). These self-contained units complete the user-paced system for understanding microprocessors. Users progress in a logical sequence from micro to macro level programming to the operation of a fully automated digital system with the modules, each of which has an instruction manual, battery, charger, cables, and connectors.

In the LCM-1002 controller module a 256 x 20 p/ROM (five chips) is used to store macroinstructions, each containing eight or 16 microinstructions. The module also has a memory data register, instruction register, and program counter. Interfacing the controller with a read/write memory presents assembly-level language ideas. Single step manual or automatic clock, macroinstruction load, a program counter load, and a memory data register clear are accessible by pushbutton or toggle switches.

The standalone R/W static RAM, organized as 1024 words of 12 bits each, stores macroinstructions. A 12-bit instruction word provides an operation code and an operand address; the 1024 words may include instructions, constants, or variable data. Switches are provided on the LCM-1003 memory module for manual loading. An address counter then automatically increments the address, facilitating both initial loading and the insertion of blocks of data at individual locations in memory. VLED indicators are used to observe address and content of each selected location. Multiplexers are used for either address and data bus isolation of the memory during manual loading, or direct operation from a remote device.

Designed to accomplish I/O interfacing to the microprocessor, the LCM-1004 I/O module is the final step in the microsystem development. Four 4-bit input ports and four 4-bit output ports with latches provide temporary data storage within the system, allowing synchronization of the user's program with outside data. Ports may be operated independently or in combinations of two, three, or four ports. Up to three I/O modules may be used for system expansion.

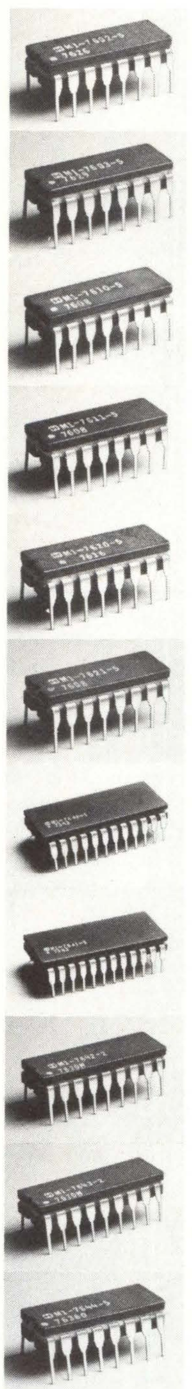
As an additional aid, a 390-page book, "Software Design for Microprocessors," is available, designed to give the reader an understanding of the basics of microprocessor machine code and assembly language, and of fundamental hardware/software relationships.

Circle 175 on Inquiry Card

Bipolar Microprocessor Is Optimized For Control Operations

A high speed monolithic microprocessor with a fixed instruction set, the model 8X300 employs bipolar Schottky technology and a partitioned bus

Why Do More Top Designers Insist On Working With Harris Generic PROMs?



The compatibility and depth of our Generic PROM family simplifies selection, application, and production. But that's only the beginning. Here are a few specific reasons for choosing Harris.

✓ Identical programming specifications means that one programmer programs the entire family.

✓ Single pulse one millisecond per bit programming achieves fast programming and superior reliability.

✓ Industry's highest programming yield increases production efficiency, regardless of PROM size.

✓ Access times are guaranteed over full temperature and voltage ranges and any random addressing sequence.

✓ Harris is the only JAN-38510 QPL-1 approved PROM supplier.

✓ Proven Nicrome fuse design and Schottky technology.

✓ Complete family availability from prototype quantities to production volumes.

Now See How The 1Kx4 PROM Can Improve Your System.

✓ High-density 16 or 18 pin packages greatly reduce board area.

✓ HM-7644 (16 pin, no enables) provides direct upgrade for systems using 1K or 2K PROMs and having less than 1024 words.

✓ HM-7642/43 (18 pin, 2 enables) extends high density packaging to large memory configurations.

✓ Low power per bit: (Icc$<$140 ma or $<$180 μW/bit).

For a quick look at our PROM family check the chart. And for complete details call your nearby sales location or write to Harris Semiconductor, P.O. Box 883, Melbourne, Florida 32901.

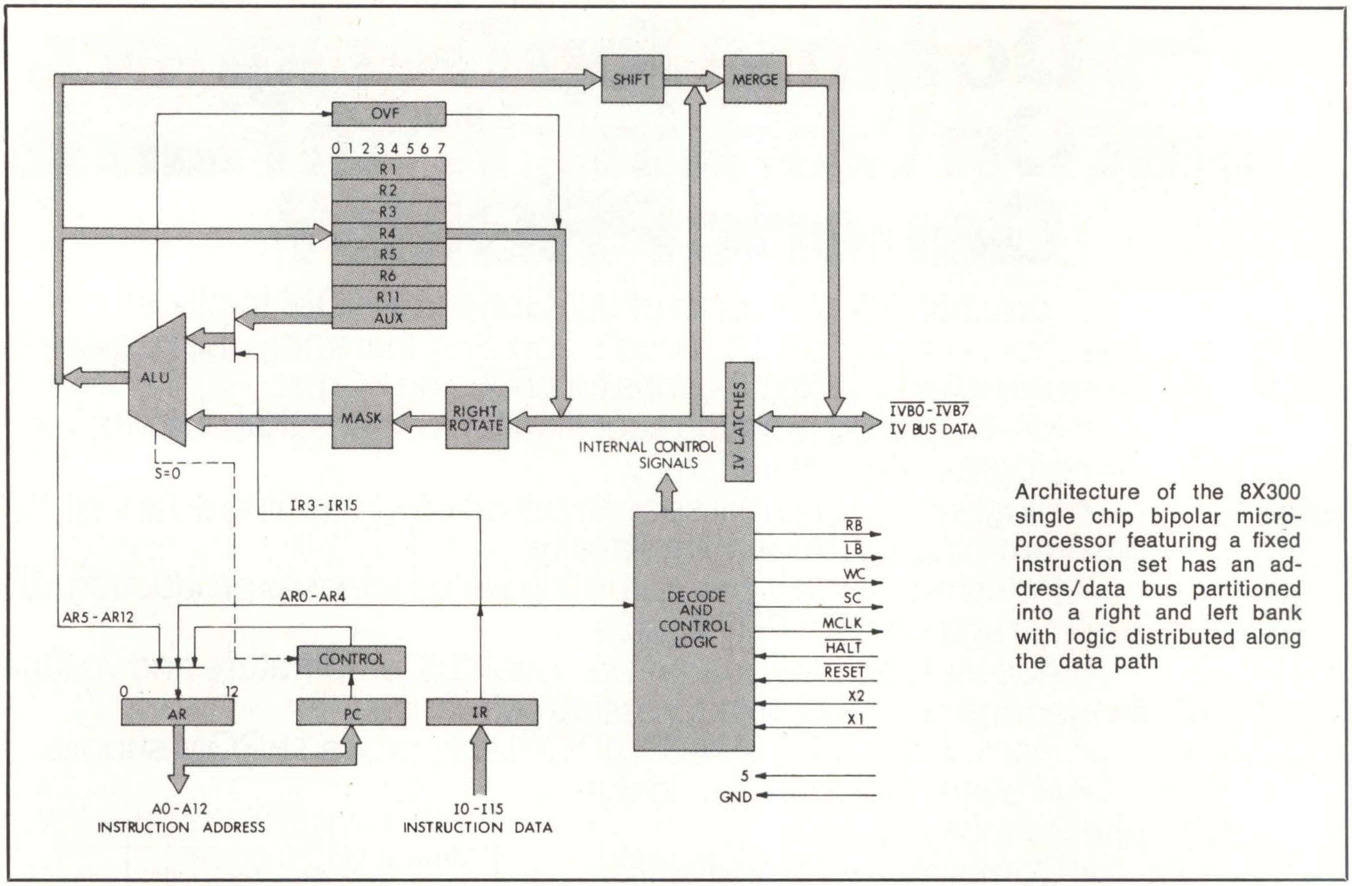
Device #	No. of Bits	Organi-zation	No. of Pins	Max. Access Time* Com.	Max. Access Time* Mil.
HM-7602 (open coll)	256	32x8	16	40ns	50ns
HM-7603 (three state)	256	32x8	16	40ns	50ns
HM-7610 (open coll)	1024	256x4	16	60ns	75ns
HM-7611 (three state)	1024	256x4	16	60ns	75ns
HM-7620 (open coll)	2048	512x4	16	70ns	85ns
HM-7621 (three state)	2048	512x4	16	70ns	85ns
HM-7640 (open coll)	4096	512x8	24	70ns	85ns
HM-7641 (three state)	4096	512x8	24	70ns	85ns
HM-7642 (open coll)	4096	1024x4	18	70ns	85ns
HM-7643 (three state)	4096	1024x4	18	70ns	85ns
HM-7644 (active pullup)	4096	1024x4	16	70ns	85ns

*Access time guaranteed over full temperature and voltage range.
Industrial (T_A = 0°C to 70°C, V_{CC} ±5%)
Military (T_A = −55°C to 125°C, V_{CC} ± 10%)

Proven PROM Capability

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

CIRCLE 60 ON INQUIRY CARD



Architecture of the 8X300 single chip bipolar microprocessor featuring a fixed instruction set has an address/data bus partitioned into a right and left bank with logic distributed along the data path

structure, to increase operational simplicity and system efficiency. Designers need only interface the device to selected program storage and I/O devices, and clock mode.

The single-chip processor features a dual-purpose address/data bus partitioned into a right and left bank, with logic distributed along the data path. This and the double operand instruction set, along with eight 8-bit working registers; separate instruction address, instruction, and I/O data buses; on-chip oscillator; and dedicated program counter enable 8-bit parallel data to be accessed and processed in one 250-ns cycle.

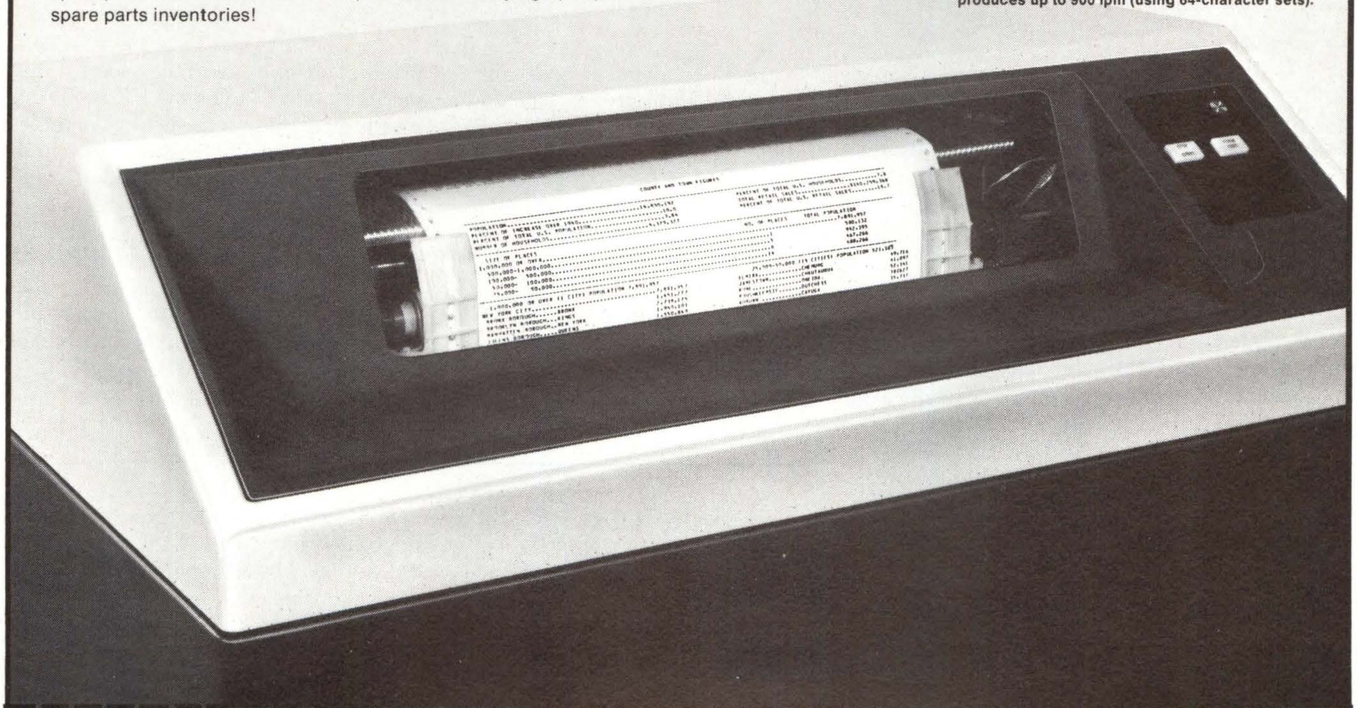
According to Signetics, 811 E Arques Ave, Sunnyvale, CA 94086, industry-standard peripheral circuits, assembler, and prototyping system provide support for the microprocessor. Peripheral circuits include both synchronous (8T32/8T33) and asynchronous (8T35/8T36) I/O ports, and the 8T39 bus extender. These circuits are field programmable so that the user can set the addressing of the microprocessor. Program storage is provided by a variety of p/ROMs; working storage is provided by RAMs.

Circle 176 on Inquiry Card

System Features Dual Audio Cassette and Video Terminal Interface

Key features of the Jupiter IIC, a low cost complete microprocessor-based computer system with 8K RAM and 3K ROM, offered by WaveMate Computers and Systems, 1015 W 190th St, Gardena, CA 90248, are video terminal interface and keyboard, and the dual audio cassette interface. I/O capability of the unit's M6800 microprocessor is extended with an 8-level prioritized and maskable interrupt system, and single cycle and block DMA transfer modes. Wirewrap modules allow custom tailoring of system logic; plug-in modules provide sockets for 8- to 64-pin ICs.

The video terminal interface converts any black and white TV set into a monitor or CRT terminal. Features of the interface and key-

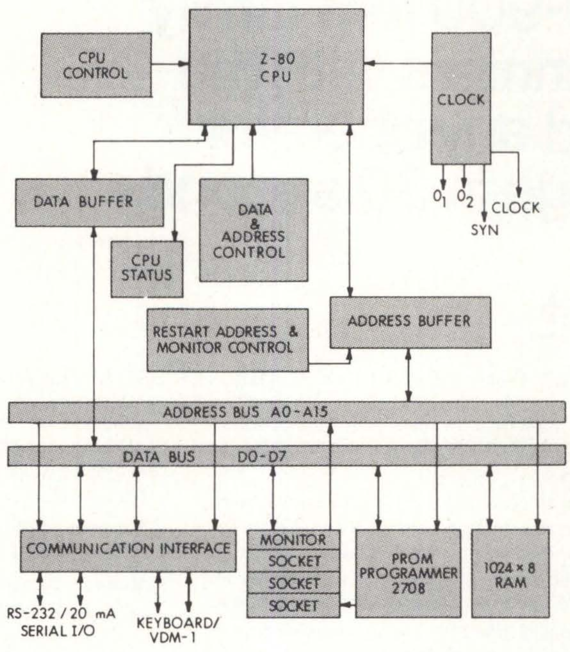


board include upper and lower case character sets (including the Greek alphabet), and dot graphics. A dual port memory allows display refreshing without the use of CPU cycles, providing minimum CPU loading and high display resolution due to ANSI standard sync and video signals. Basic interface displays 16 lines with 64 char/line, expandable to 32 lines with 64 char/line.

The dual audio cassette interface serving as a complete paper tape replacement interfaces two portable audio cassette units to the system, and provides start/stop motor controls. It operates at 600 and 1200 baud. Sophisticated error recovery circuitry gives data reliability.

A monitor/debugger package includes an interrupt handling system and I/O monitor call instructions. Systems are also supplied with a programmable macro editor, expanded assembler, and proposed ANSI standard BASIC. In kit form the system costs $2200; assembled and tested, it costs $3200, which includes two audio cassette units and a 12" black and white TV set.

Circle 177 on Inquiry Card



Single PC board 80AI microcomputer combines functions of CPU, RAM, ROM, and SIO boards

Single Board Computer Combines Functions of Four Boards in One

The 80AI is a low cost expandable single board microcomputer which contains all components needed to build either a system compatible with Altair™ and IMSAI backplanes, or a standalone microcomputer. The single PC board combines all of the functions of Altair's CPU, RAM, ROM, and SIO boards. With the addition of power and a terminal, the microcomputer is ready to use after assembly.

Based on the Zilog Z-80 microprocessor (see *Computer Design*, Feb 1976, p 132), the system from Quay Corp, PO Box 386, Freehold, NJ 07728 runs on a 2.5-MHz clock. This enables both Altair 8800 or Intel 8080 software to be run. Maximum flexibility can be obtained from an 8080-compatible 2-phase clock and sync signal synthesized in the kit.

With the Z-80 instruction set more powerful software can be developed. There are 158 instructions including 78 8080A, block transfer, and block search instructions. The system also includes two index registers (17 internal registers), three interrupt, an 8080A, 6800-type, and Z-80 vectored modes.

Memory is supplied onboard. The monitor is supplied on a ROM, and a 1024 x 8 dynamic RAM is provided for user programming. Sockets can hold up to four 1024 x 8 EPROMs for program storage development.

Three communication support circuits are standard: RS-232-C, teleprinter 20-mA current loop, and parallel ASCII keyboard. The ROM-resident monitor with listings samples three communication interfaces, eliminating user strapping. Serial baud rates from 110 to 2400 with one or two stop bits are supported. The kit also includes a parallel port, EPROM programmer, documentation package, PC board, and 40- and 24-pin sockets—for $450. Factory assembled and tested the system costs $600.

Circle 178 on Inquiry Card

Programmable CPU Module Is Available for Microcomputer

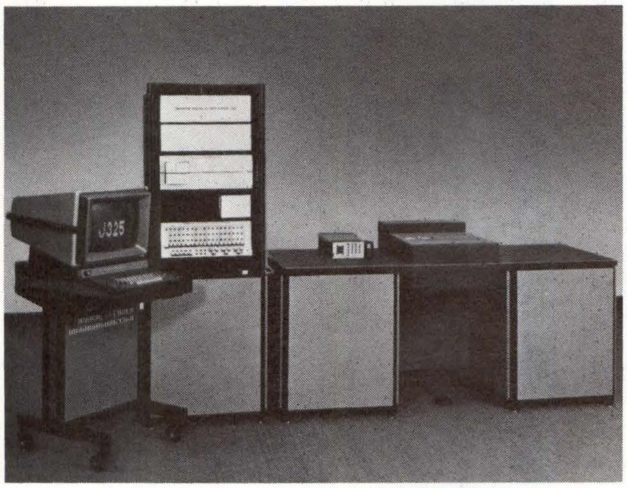
Designed for the company's System 8 series of 8-bit bipolar microcomputers, the M-8Z is a single board (4.5 x 4.5") microprogrammable CPU. Available from the Electronic Products Div of the Warner & Swasey Co, 7413 Washington Ave S, Edina, MN 55435, the CPU allows the user to select his own instruction set, either emulating another 8-bit computer instruction set, or defining his own set.

With a micro-cycle time of 250 ns, the CPU interfaces with all System 8 modules, which include a programmer's console so that the user can microcode standard console functions or define his own to fit the exact application. Applications include high speed execution of special-purpose algorithms, or dedicated OEM applications with unusual instruction set requirements.

Module comes with a microassembler program (written in FORTRAN) available on Dialcom timesharing, and microprogramming manual.

Circle 179 on Inquiry Card

THE J325 IC TEST SYSTEM. THERE'S A SPECIAL PREMIUM IN EACH ONE.



The premium is productivity.

To squeeze every last bit out of the J325 digital IC test system, we combined a single mainframe with two optimized test stations, one for ECL, TTL, and DTL, the other for CMOS and static MOS.

The CMOS/MOS station gives you low current and differential voltage measurements, programmable clock phases, and comparator strobe delays. The ECL/TTL station provides solid-state switching, low noise, one millivolt resolution, and subnanosecond time measurements with the optional S357 add-on. The system can handle up to four of these stations in whatever combination is most productive for you.

The J325 really shines on the production line, but it also delivers excellent service in incoming inspection, device evaluation, and QC. To help make your operation even more productive, the system feeds back Schmoo plots, distribution analyses, summary sheets, wafer maps, and full datalogging of all tests.

We back up the J325's productivity with our unique 10-year circuit module warranty and a global service program supported by local parts stocking centers. We also provide all software, interfaces to probers and handlers, and ongoing applications support.

System design will always be a question of trade-offs. At Teradyne, we'll always take the alternatives that give our systems the greatest productivity. And we'll continue to build them in a way that guarantees they'll remain productive for as long as they're needed. Productivity is something you can't have too much of.

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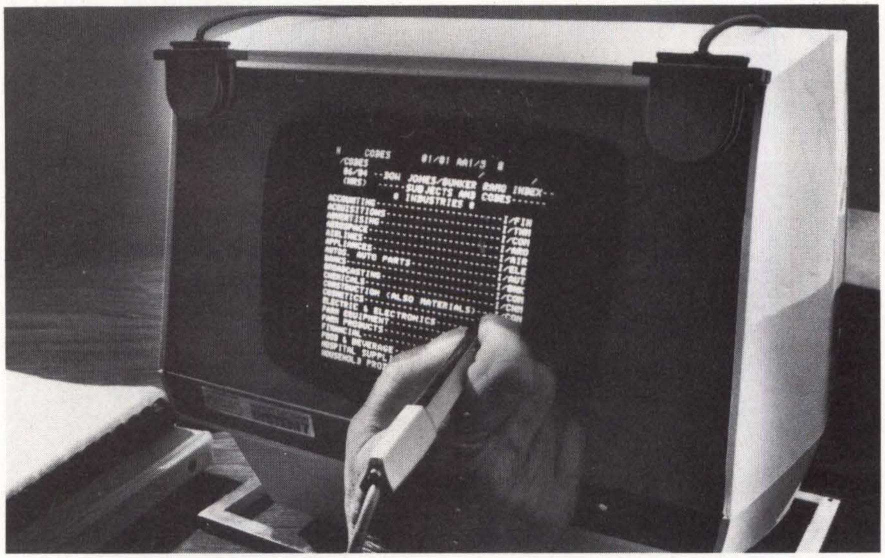
Microprocessor-Based Controller is Minicomputer Compatible

The 1000 series microprocessor-based controller, designed around the 2900 low power Schottky, 4-bit slice microprocessor, allows direct plug compatible interconnection between the company's memory peripherals and Digital Equipment Corp, Data General, or Hewlett-Packard minicomputers. Xebec Systems Inc, 2985 Kifer Rd, Santa Clara, CA 95051, claims the controller's 150-ns cycle time makes it the fastest on the market. The speed allows such special features as ECC to be incorporated while maintaining plug compatibility.

An additional feature is that the controller is also program transparent. The p/ROM layout for each computer/peripheral combination permits total hardware and software compatibility. The controller is available in systems with 5 to 1200M bytes of disc storage, 12.5- to 125-in./s mag tape, and Persci double-density floppy discs.

Circle 180 on Inquiry Card



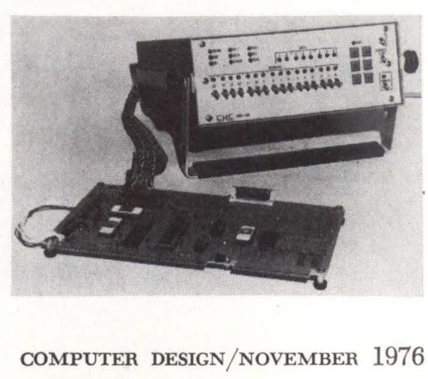
Standalone In-Circuit Emulator Debugs 8080 Systems

Connecting to the host system by a 40-pin connector that plugs into the socket usually occupied by the user's 8080, the portable standalone MAS-80 microcomputer analyzer system debugs 8080 systems. The in-circuit emulator displays all important 8080 signals.

Unit requires no development system or teleprinter to operate and supplies all dc power for ICs and 8080, allowing users to monitor and control any 8080 project. An add-match feature causes the 8080 to wait or provide a sync pulse when switch-selected address is reached. Data bus indicator has three switch-selected options to monitor the bus during all cycles while the system is running.

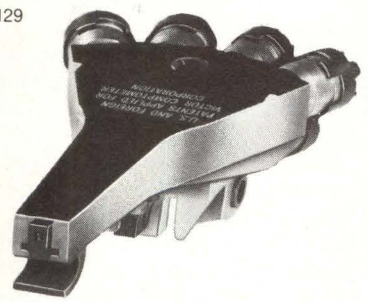
Module contains its own 8080, which is protected from damage by buffer circuits. High quality components are used in the front panel to reduce finger fatigue. Small debug machine programs can be entered in the user's RAM; debugging is further enhanced by a continuous deposit feature, and by using the control panel's single-step mode.

Internal 5-V supply provides power; input voltage is 117 Vac. The system, available from California Micro Computer, 9323 Warbler Ave, Fountain Valley, CA 92708, supplies



Victor's high-speed matrix printer can fit into your systems design.

129



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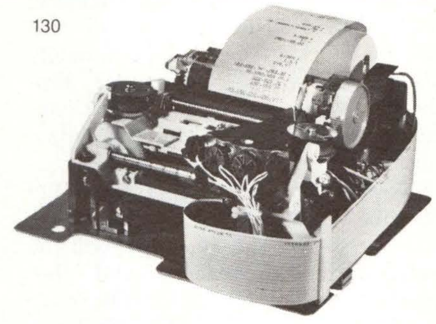

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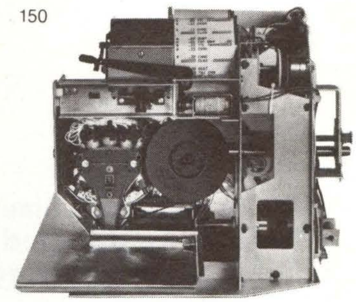
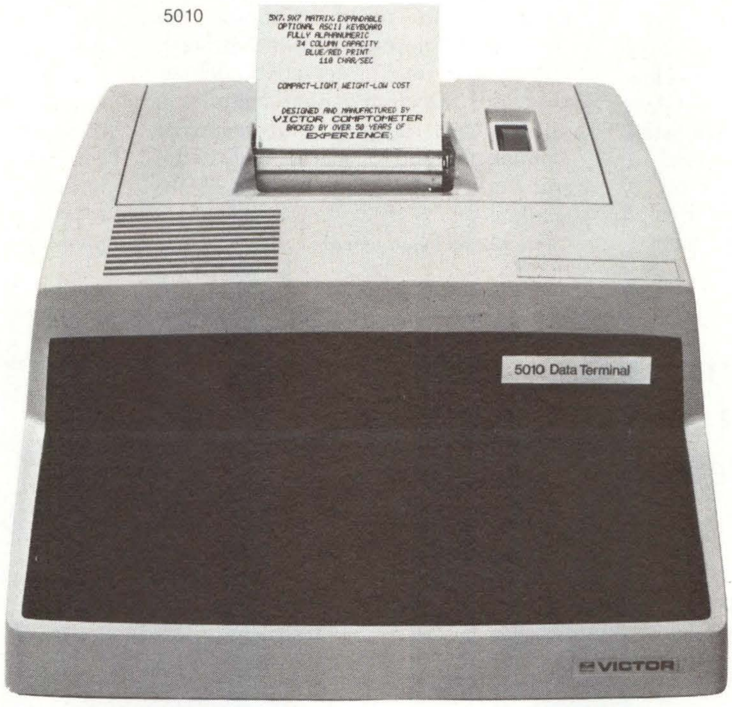


5010



If you're starting from scratch in designing your own print mechanism, the Victor Model 129 matrix print head will optimize your price-performance ratio.

You can enjoy this popular and reliable device already built into the Victor Matrix Printing Mechanism 130 (which can be integrated readily into all types of data generating devices).

It's also available in the Multi-Position Printing Mechanism 150 that can print three documents simultaneously.

You'll find Victor terminals meet your needs, too.

The 5010 allows interfacing with RS232C, 8-bit parallel or TTY current loop. With Intel MCS-40, you have a data terminal with a mind of its own.

The 5005 terminal comes complete with a matrix printing mechanism, integrated power supply, and driver circuitry.

So, to see how Victor components can fit into your program, just send the coupon.

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Chicago, Illinois 60618

Yes, I'd like detailed specs on Victor components.

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THE VICTORS

CIRCLE 63 ON INQUIRY CARD

dc power for its 65 SSI, MSI circuits, and the 8080.

Controls include data-address select, start-stop, reset, load add, step, enter data, exam, sync address stop, and delay switches; run and power indicators; sync pulse test point; 16 LED address indicators; and 8 LED data indicators.

Circle 181 on Inquiry Card

Savings in Memory Size and Time Are Obtained With Multilevel Language

MicroFORTH™, a multilevel microprocessor language, offers large reductions in application development time, program execution time, and memory requirement. The developers, Forth Inc, 815 Manhattan Ave, Manhattan Beach, CA 90266, state that execution times have been reduced by as much as a factor of 10, compared with those of other high level languages (PLM and BASIC). For an application requiring 2K bytes coded in assembly language, the language can reduce the memory requirement to 1K or less.

The language runs on a microprocessor development system with a minimum of 6K bytes of memory, diskette, and terminal. In an 8K configuration, this leaves approximately 2K for customers' applications. Programs written in microFORTH are transferrable among most manufacturers' microprocessor systems.

Now offered on the Intel MDS 800 and the RCA CDP 1800 development systems, the package will be available for the EXORciser and other systems by late fall 1976. The standard package, selling for $1000, includes a compact disc operating system, powerful macro-assembler, the company's compiler and interpreters, text editor, and interactive debugging aids. Documentation includes a self-teaching primer and technical manual. Extended math, BCD I/O, and other optional functions are available.

Circle 182 on Inquiry Card

Second Sourcing of 2900 4-bit µProcessor Slice Family Is Arranged

Motorola Semiconductor Products, Inc, PO Box 20294, Phoenix, AZ 85036, has elected to second-source the 2900 series of Schottky-TTL processor components originated by Advanced Micro Devices, Inc of Sunnyvale, Calif. Mask sets have been purchased for the 4-bit microprocessor slice (MC2901), microprogram sequencer (MC2909), and one-by-two-port register (MC2918).

Samples will be available in the fourth quarter of 1976, with quantity production slated for first quarter, 1977. Availability of the MC2911 sequencer, a mask option version of the 2909, will closely follow that time schedule.

Future products for the family, notably single- and dual-port bus transceivers and a priority interrupt controller for system hardware interrupts, are also included in the agreement. These products are scheduled for introduction in 1977. □

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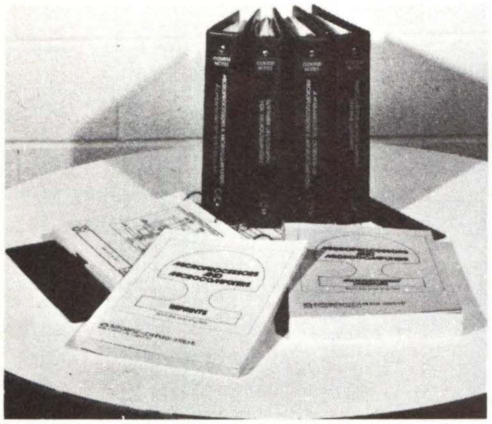

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201: MILITARY AND AEROSPACE MICROPROCESSOR SYSTEMS (420 PAGES)
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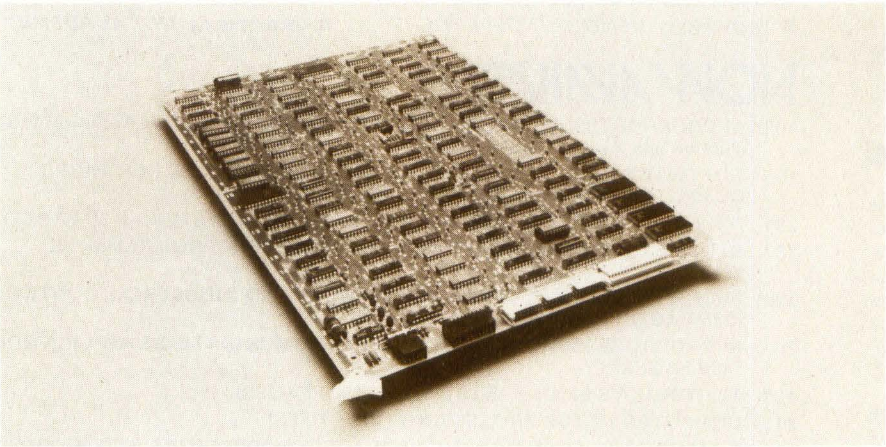
PRODUCT FEATURE

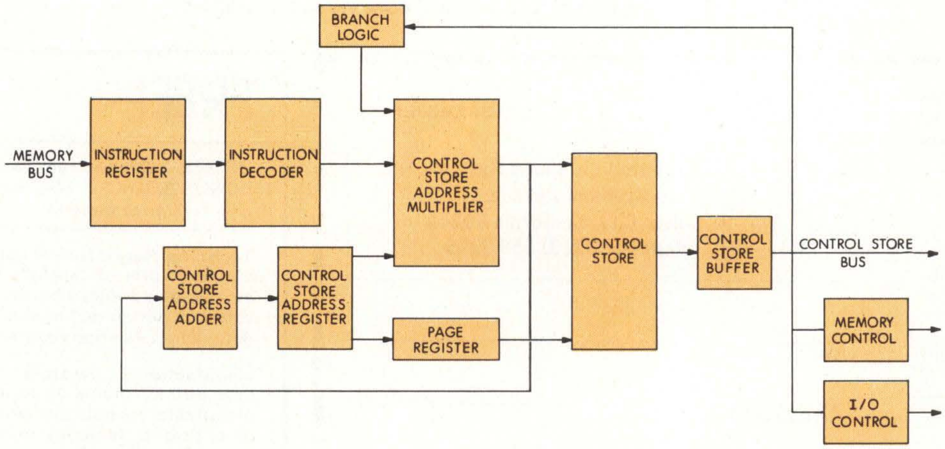
Small But Very Fast Minicomputer Offers Large-Machine Performance



High speed arithmetic capability, exceptional communications performance, and the ability to work with high level languages are claimed as key features of Varian Data Machine's V77-200 computer, the smallest member of the V77 family. Designed to function as either a standalone processor in a laboratory environment, handling a heavy volume of scientific calculations, or as part of a multiple-computer distributed processing network with larger members of the family, this computer is as powerful as many large scale minicomputers. Although its architectural scheme is characteristic of upper-end minicomputers, including the ability to run a multitasking operating system, it provides a high performance/price ratio.

Characteristics and Capabilities

The V77-200 has fully microprogrammed architecture, an 8-register central processing unit (CPU), and a 32-bit arithmetic capability which permits handling of 8-, 16-, or 32-bit data, working with a set of 187 instructions. Many of the instructions incorporate multiple operands, using combinations of 16- and 32-bit word lengths for effective memory use and efficient memory addressing. Byte manipulation instructions are also incorporated to support byte-



Control loop block diagram for the V77-200 minicomputer oriented operations such as data communications. The instruction set is implemented by microinstructions stored in a block of 16K bits (512 words x 32 bits) of read-only memory (ROM) devices.

One feature that separates it from low-end OEM processors is the speed of its arithmetic functions. Signed multiplication functions, for instance, are performed in 4.9 μs and divide functions in 8 μs. The company states that medium-scale integration (MSI) was chosen for the circuitry in preference to large-scale integration (LSI) in order to obtain the high performance of MSI, even though it meant trading off the low cost of LSI.

Throughput speed is 165 ns per microinstruction. In addition, each microinstruction contains multiple fields which are coded to select the next microinstruction address while concurrently performing functions such as shifting or manipulating bytes in a selected register, performing logical or arithmetic functions in the address, or starting a memory cycle or I/O operation. The microcode also includes an automatic bootstrap loader for implementing multiple devices.

Need for a programmer's console is eliminated by virtual console logic which permits an operator to control the computer from a teletypewriter or CRT terminal keyboard. This logic is a combination of firmware (ROM) in the control store and programming in main memory.

An optional data communications multiplexer (DCM) halfboard plugs into the computer chassis and transfers into memory via a direct memory access (DMA) channel. Data communications capabilities are supported by a DCM and associated line adapter which provide a virtually universal data communications hardware interface. A single DCM can serve as an interface for large numbers of synchronous and asynchronous terminals and communications lines, permitting concurrent execution of a variable number of real-time and background tasks. Data are transferred through the system by the DCM at rates exceeding 60K bytes/s.

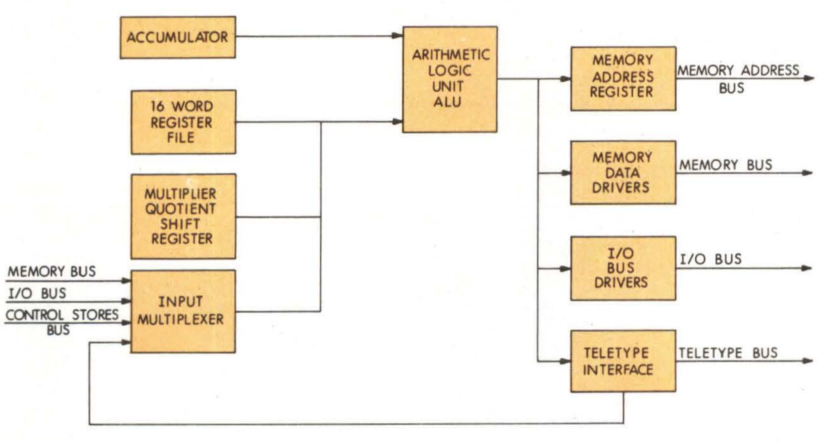
I/O structure features DMA for high speed devices and programmed I/O for devices of lower speeds. A dual bus architecture enables the processor to communicate with I/O devices without tying up the bus to memory; the I/O end of the bus accommodates programmed I/O, interrupts, and DMA while the other provides a direct channel to memory. Standard programmed I/O uses separate program instructions for each character or word transfer. DMA uses a cycle-stealing sequence to transfer blocks of data at rates to 330,000 words/s.

Up to 64 external vectored interrupts are supported. External interrupts are driven by the I/O bus with interrupt addresses determined externally. A number of internal interrupts, with fixed vectors and priorities, are generated by CPU hardware and do not affect the I/O bus. Interrupt servicing can simply identify a device and vector to a device handler or perform functions such as saving machine state, switching stacks, updating priority, and enabling an interrupt before branching to the device handler.

Although the smallest member of the V77 family, the -200 is physically and electrically compatible with the other family members of superior processing power. For instance, its dual bus scheme enables it to function either in a distributed processing environment with multiple combinations of the same type processor or with a larger computer on a shared-memory basis.

All are supported by the company's multiprogramming VORTEX operating system as well as the library of programs and languages for all V70 series machines. Included are FORTRAN IV, HASP/RJE, and VTAM telecommunications software. The last consists of a collection of processing modules that provide a network definition language, operator network control, storage management, and interrupt servicing.

Other standard features include an integral teleprinter/CRT controller, real-time clock, and automatic program loaders. Options include operator's console, power fail/restart, integral power supply, system chassis, and 660-ns memory board with 8K, 16K, or 32K words capacity.



Data loop block diagram for the V77-200 minicomputer

Price and Delivery

Single unit price for the V77-200 minicomputer is $1100 for the processor board alone or $5100 for a chassis mounted computer including 16K memory and all features required to run an operating system. OEM discounts are available. Deliveries are scheduled to begin in January 1977. Varian Data Machines, 2722 Michelson Dr, Irvine, CA 92664. Tel: (714) 833-2400.

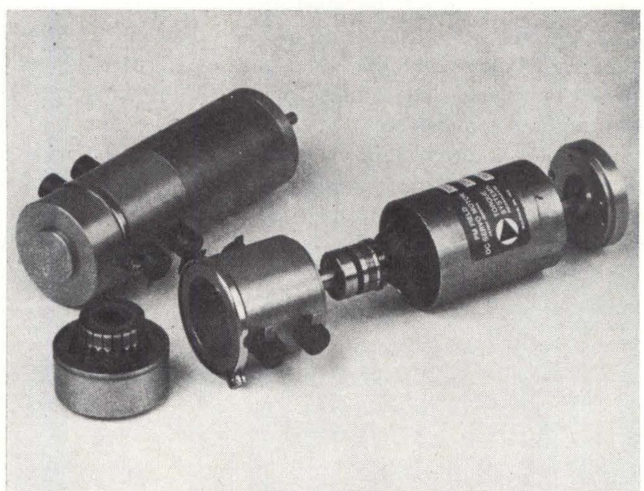
For additional information circle 199 on inquiry card.

Numeric Data Entry Terminals Are Readily Dedicated to User's Applications

Operators with little or no experience with computers are the intended users of the first of a series of numeric data terminals for industrial and commercial applications. HP 3070A is designed for optimum performance with the HP 1000 computer system as well as with HP 2100 and 21 MX computers; the 3071A is for use with computers of most other manufacturers. Both have numeric-only keypads for entering data and bright, 16-digit numeric displays. Keys and LED indicators can be specially labeled to customize the terminals for the user's specific computer programs. Terminals can be used to link HPIB-compatible instruments to the computer system, enabling the computer to control instruments up to 1.24 miles distant. As many as 56 terminals can also be connected to a computer system via a single twisted pair cable. Weight is 10.3 lb, dimensions are 10.9 x 4.6 x 15.7". Their ability to interface a wide range of instruments to a remote computer adapts them to electronic manufacturing and test installations. **Hewlett-Packard Co,** 1501 Page Mill Rd, Palo Alto, CA 94304.

Circle 200 on Inquiry Card

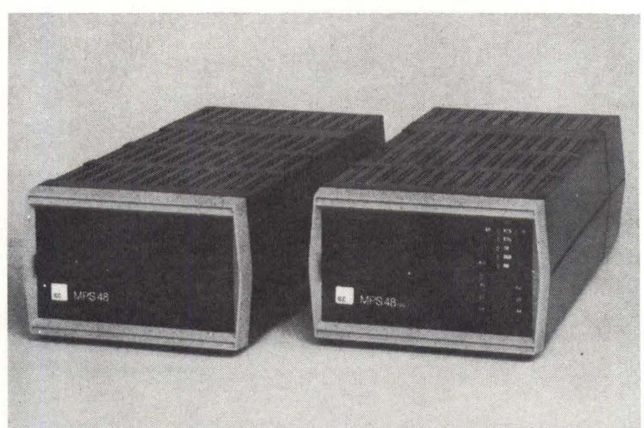
DC Servomotor Improves Control of Instantaneous Speed Variations



Although specifically designed for use as capstan or reel drivers in tape drive and tape transport systems up to 50 in./s, 2000 and 2100 series dc permanent magnet servomotors also meet the requirements of line or character printers for paper feed and carriage drive systems. Integral tachometers reduce ripple to 2% pk-pk without external filtering. Use of an alnico field improves tempco to 0.015%/°C, eliminating the need for compensation networks and the resulting high impedance outputs. Unique bearing construction results in better seating of brush at higher speeds and longer brush life. Larger bearings also yield greater radial and axial load ratings and provide longer bearing life. Design of the brushholder makes it virtually immune from typical breakage problems. Large shaft diameters allow high mechanical resonant frequency between motor and tachometer, as well as heat radiation qualities of the casing, to provide lower thermal resistance and increased life expectancy. **Torque Systems Inc,** 225 Crescent St, Waltham, MA 02154.

Circle 201 on Inquiry Card

Microprocessor-Based Modems Reduce Line Equalization Times



MPS 48 and 48 Dial, 4800-bit/s modems featuring microprocessor technology, are designed to reduce line equalization time for greater transmission efficiency. Operating at full data rate, they equalize dial-up lines and dedicated point-to-point or multidrop lines in 26 ms, as opposed to at least 50-ms clear-to-send time generally required by conventional 4800-bit/s modems to achieve equalization. Remote test features available for use in either point-to-point or multidrop networks allow the user to isolate system faults from the central site without involving personnel at remote sites. The modems are tolerant of widely varying line conditions and operate with significantly low error rates in both dial-up and multidrop polling systems. They measure 5⅕ x 8 x 19"; two can fit side by side in a standard 19" rack. **International Communications Corp,** 8600 NW 41st St, Miami, FL 33166.

Circle 202 on Inquiry Card

The fastest microcomputer known to man

Want to see it again?

Just call Plessey and ask to see the 16-bit MIPROC 16, the first microcomputer fast enough for your real-time systems.

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PRODUCTS

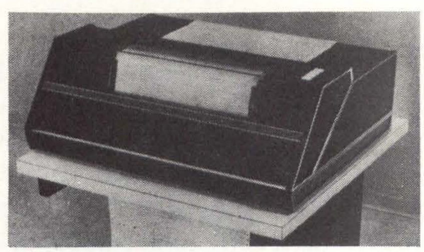
DIGITAL CASSETTE

Certified digital cassette features mag tape with a new oxide to achieve higher signal output, increased environmental stability, and improved wear characteristics. Signal output of the Scotch brand No. 834 cassette exceeds NBS reference and std tapes by 20%. Magnetic coating, which does not soften at high temp or become brittle at low temp, improves environmental stability, resulting in consistent head-to-tape contact. Improved coating wearability provides no appreciable signal loss, or change in signal uniformity. **3M Co, Data Recording Products Div,** PO Box 33600, St. Paul, MN 55133.
Circle 203 on Inquiry Card

LIGHTED PUSHBUTTON SWITCHES

Offering a series of five colored pushbuttons (opaque or translucent backgrounds), seven colored screens, and four colored filters, PLI pushbuttons are designed for use with the company's "Push-Lite" lighted switches and indicators which feature leaf-spring switching, front of panel mounting and relamping, momentary and push-lock/push-release actuation, and twin and single lamp illumination. A variety of legend options are available. **Switchcraft, Inc,** 5555 N Elston Ave, Chicago, IL 60630.
Circle 204 on Inquiry Card

IMPACT LINE PRINTER



Operating at 300 to 500 lines/min., the model 200 is available in both 80 and 132 col widths. Tractor feed is used for continuous forms operation. The printer uses a fully formed char font on a horizontal type carrier, which is operator removable and replaceable for multiple font changeover. A hammer per position produces 64- and 96-char ASCII sets. Mechanism contains two full line buffers and is available with most popular interfaces. An automatic motor turn-off feature is included. **Data Test Corp,** 2450 Whitman Rd, Concord, CA 94518.
Circle 205 on Inquiry Card


120 VAC
INTERNATIONAL RECTIFIER
IOR CRYDOM DIVISION
SOLID STATE RELAY
D1210
PATENT NO. 3,723,769
3-32 VDC
2 AMP SERIES 2
FOR HEATSINK OR PANEL MOUNT
Two models, S218 (120 Vac) and S228 (240 Vac), feature standard 0.187" terminals for push-on connectors or bare-wire solder connection, positioned to provide maximum isolation between signal and power circuits. Offset positioning of the terminals permits side-by-side gang mounting for high packaging density. Occupying less than 1.0 cubic inch, they provide a full 8 ampere (rms) current rating and a high surge current capacity suitable for control of the toughest loads. The S218 units are $5.90 in 1,000-piece lots.
the originators
of the photo-isolated
solid-state power relays
that have become the
industry standard . . .
CRYDOM
S218
A QUANTUM STEP
IN SIZE
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REDUCTION!
TWO NEW CRYDOM
CHALLENGER
SOLID-STATE RELAYS!
The new Crydom Series 2 and 3 SSRs combine small size and low price, challenging all comparably rated SSRs, hybrid relays, and in-house designs on a size/cost/performance basis. They provide photo isolation, zero voltage switching, high current rating and rugged packaging — first established by the original Crydom Series 1, now the world's leading SSR design. Designed for UL/CSA approval, they offer the advantages of long life, RFI-free switching, logic level control, and excellent electrical and mechanical isolation of signal and power circuits.
The application of SSRs is no longer limited by size and cost. Crydom Challengers have knocked down these barriers. SSR control of motors, heaters, lamps, transformers, solenoids, valves and contactors now becomes practical in many new applications.
Think about it for your product . . . and join the Challengers!
IOR
INTERNATIONAL RECTIFIER
CRYDOM SOLID STATE RELAY
S312
2 AMP SERIES 3 FOR PC BOARD MOUNT
Two models, S312 (120 Vac) and S322 (240 Vac), provide a higher power handling capability than any SSR of equal size. Occupying less than 0.4 cubic inch, Series 3 SSRs achieve a full 2 ampere free-air rating in a 40° ambient. A low 3/8" profile allows 1/2" spacing of rack mounted printed-circuit boards. The S312 units are $4.90 in 1000-piece lots.
INTERNATIONAL RECTIFIER
IOR CRYDOM DIVISION
1521 Grand Avenue, El Segundo, CA 90245 (213) 322-4987
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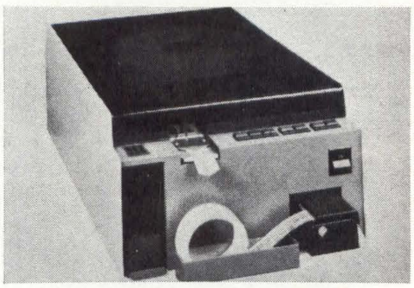
. . . the pacesetters!

PRODUCTS

OCR WAND

Automatically entering human-readable source data into distributed data processing terminals such as the IBM 3270, the class P130 OCR wand reads machine-printed, human-readable alphanumeric characters produced either in the OCR-A or OCR-B (subset 1, ECMA 71) type font. All output is computer compatible. The wand is connected between an intelligent terminal and its keyboard, enabling existing communications links between the keyboard and terminal to be maintained. Data are read and input at speeds of 30 to 130 char/s. **Recognition Equipment Inc,** PO Box 22307, Dallas, TX 75222.
Circle 206 on Inquiry Card

PAPER TAPE READER/PUNCH



A quiet (58 dB) combination which attaches to any terminal through the RS-232 or current loop connector, SRP-300 may be remotely controlled from the line or terminal through std DC1-DC4 codes. Full/half duplex, line/local, search/edit control, back space, tape feed, and selectable baud rates are all standard. Compact (12" wide) unit features MODUPERF tape punch mechanism which cuts all paper, Mylar, rolled, and folded tapes without re-adjustment or modification. **Data Specialties, Inc,** 3455 Commercial, Northbrook, IL 60062.
Circle 207 on Inquiry Card

900-LINE/MIN. PRINTER FOR SYSTEM/3

The 6609 System/3 printer, designed for use with IBM System/3 model 8, 10, 12, and 15 computers, is available as a direct replacement for all IBM 5203 and 1403 printer models currently used with System/3 computers. Featuring 900-line/min. performance, the units operate under std system software and require no change to user programs. They deliver clear, readable characters on single through 6-part forms. Rated speeds are attained when printing a full 63-char set over a 132-column print line. **Decision Data Computer Corp,** 100 Witmer Rd, Horsham, PA 19044.
Circle 208 on Inquiry Card

PRODUCTS

FREQUENCY-TO-VOLTAGE CONVERTER

The 9001 family is offered in std input frequency ranges of 100, 20, and 10 kHz, with all units factory pretrimmed within 0.4% (max) of full scale. Self-contained modules require only a single 15-V supply. Typical linearity is within 0.01%, and peak ripple is <25 mV typ. Gain TC is held within 100 ppm/°C (max). Designed to accept ragged input waveforms without pulse-shaping, units have an internal timing section that makes them insensitive to variations in input waveform duty cycle. **Dynamic Measurements Corp,** 6 Lowell Ave, Winchester, MA 01890.
Circle 209 on Inquiry Card

p/ROM PROGRAMMER

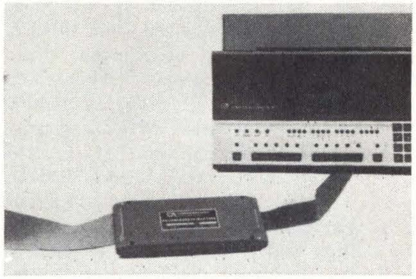
Consisting of M920 master control unit and a plug-in p/ROM personality module, series 92 uses interchangeable personality modules (same as series 90) to program all major MOS or bipolar p/ROMs. A built-in 20-mA current loop allows operation with teleprinter or with any terminal, computer, or microprocessor development system having this interface. The unit can be commanded to program, list, duplicate, or verify p/ROMs; or can be used as a standalone p/ROM duplicator. **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940.
Circle 210 on Inquiry Card

GAS DISCHARGE PANEL DISPLAYS

Displaying between 19 and 96 characters depending on desired character format, series C4101 has 17 horizontal rows x 192 columns which easily adapt for displays of graphs, signatures, and waveforms. Panel can be programmed to display 19 8 x 12 char nearly ½" high, or 96 5 x 5 char (each 0.27" high) in three rows of 32 each. Single SELF-SCAN[R] unit, with anode and cathode drive electronics, measures 12 x 2 x 1", requires max of 23 connections, and weighs 10 oz. **Burroughs Corp, Electronic Components Div,** PO Box 1226, Plainfield, NJ 07061.
Circle 211 on Inquiry Card

PRODUCTS

MAG TAPE INTELLIGENT CABLE



Driving up to four PE or NRZ tape units, the parallel interface intelligent cable is used in conjunction with a distributed I/O system and external tape formatter. In the 6′ cable is a Picoprocessor, a self-contained, microprogrammed processor that supports std magnetic tape drive control functions, such as data transfer, device protocol, device status monitoring, and interrupt generation. The processor mounts to any flat surface. The formatter is compatible with std tape speeds (75 in./s max), densities from 200 to 1600 char/in., and seven or nine tracks. **Computer Automation, Inc,** 18651 Von Karman, Irvine, CA 92713.
Circle 212 on Inquiry Card

40-PIN IC TEST CLIPS

Proto-Clip™ 40 is compatible with 0.6″ center ICs up to 40 pins. Test clip offers a narrow throat for bringing IC leads up from high density PC boards—practically eliminating accidental shorts while testing live circuits. It can be used to inject signals and wire unused circuits into other boards. Scope probes and test leads lock onto the gripping contact teeth. Noncorrosive nickel/silver contacts provide simultaneous wiping action, and low resistance connections to IC leads. **Continental Specialties Corp,** 44 Kendall St, PO Box 1942, New Haven, CT 06509.
Circle 213 on Inquiry Card

MICROPROCESSOR-CONTROLLED DIGITAL CASSETTE RECORDER

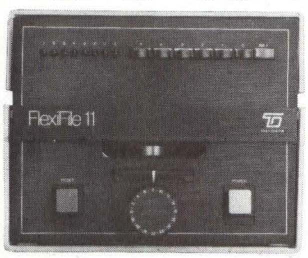
Factory dedicated to a specific instrument the dcr/10 comes complete with proper interface cable. Processor edits data to produce consistent blocked records for computer analysis. Firmware control allows units to accommodate serial or 8-bit parallel data at any baud rate, as well as any code conversion required. Tapes may be read directly by a computer's cassette system. Models currently available include TI Silent 733 ASR, Wang 2200 series, and Digital Equipment Corp with DECassette. **William Palmer Industries,** 1627 Pontius Ave, Los Angeles, CA 90025.
Circle 214 on Inquiry Card

SOLID-STATE IMAGE SENSORS

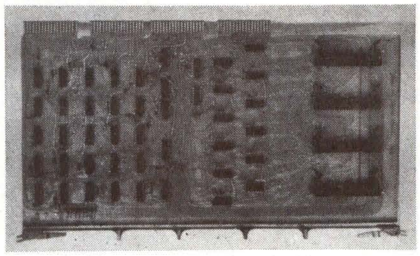
Line scanners are available with 15-μm (H series) and 25-μm (G series) element-to-element spacing. G series is offered in 128, 256, 512, 768, and 1024 element configurations and contains onchip monolithic drivers and video amps. Instead of multiphase clocks, it accepts single phase TTL drive, simplifying required peripheral circuits. Cascaded devices readily drive one another for high resolution applications requiring multiples of 1024 elements. H series is available in 1024 and 1723 element formats for single chip facsimile and OCR use. **Reticon Corp,** 910 Benicia Ave, Sunnyvale, CA 94086.
Circle 215 on Inquiry Card

PC BOARD SOLID-STATE RELAYS

Miniature solid-state relays require a 1.27 sq in. area, switch up to 3 A at 120 or 240 Vac, and are available with 3 to 8, 8 to 18, and 18 to 32 Vdc inputs to minimize input current and op temp. Capable of being driven directly by TTL logic, the units offer zero crossover switching, photo-isolation between input and output, total epoxy encapsulation, IC compatibility, long life, and immunity to shock and vibration. **Elec-Trol, Inc,** 26477 N Golden Valley Rd, Saugus, CA 91350.
Circle 216 on Inquiry Card



8-WORD PLUG-IN INTERFACE FOR PDP-8A



To meet the need for increased input capacity (96 bits) in the PDP-8A, the 8-word interface allows direct input from a number of external data sources or peripherals. IOT codes for the group of input words and associated interrupt/skip/clear functions are jumper selectable for max software flexibility. Two words and two interrupts are arranged in each of four input connectors. Model 8W can be used with the std DEC instruction set to interface the company's model 400 high speed tape reader to the PDP-8A. **Forte Technology Inc,** 15 Strathmore Rd, Natick, MA 01760.

Circle 217 on Inquiry Card

COMPUTER/PERIPHERAL INTERFACE UNIT

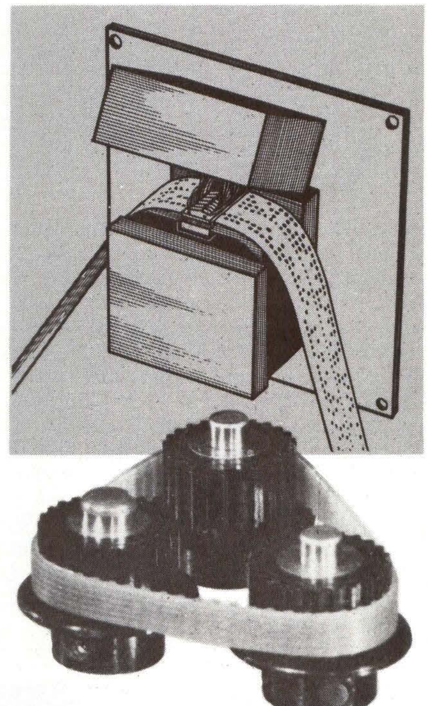
A coaxial cable interface unit, model CCI-4000 is designed for computer to computer and computer to peripheral communication at any bit rate up to 1M baud. Two or more computers can be connected to a single coaxial cable. Computer/peripheral connections can also be provided by the addition of plug-in peripheral point boards. Peripherals may be intermixed and operated at different speeds. Transmission distance can be as high as 40K ft, without repeaters, on low loss coaxial cable. **Computrol Corp,** Berkshire Industrial Pk, Bethel, CT 06801.

Circle 218 on Inquiry Card

HIGH SLEW RATE OPERATIONAL AMPLIFIERS

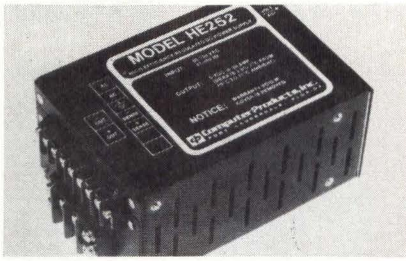
Models A970 and A975 operational amplifiers are wideband and feature high slew rate. In addition to low bias current, high input impedance, and high CMRR, they are packaged in TO-99 cases. Specs include slew rate of 80 V/μs for the A975; and gain bandwidth of 100 MHz, and an open loop gain of 95 dB for the A970. Both have input impedance of >100 MΩ. Devices operate over a temperature range of 0 to 70°C. **Hybrid Systems Corp,** Crosby Dr, Bedford, MA 01730.

Circle 219 on Inquiry Card



PRODUCTS

HIGH EFFICIENCY POWER SUPPLY



Model HE252 achieves 75% efficiency and is contained in a 6.5 x 4.5 x 3.2" package weighing 3.25 lb. Cool operating unit is designed with the "footprint" and mounting hole configuration of Lambda's B package size supplies. Output is 5 V, 20 A at 45°C; input is 90 to 130 Vac (180 to 260 Vac, model HE252E) at 47 to 450 Hz. Line and load regulation is ±0.1% max for a 10% change in line from no load to full load. Other specs include 50-mV pk-pk max ripple and noise; and 0.01%/°C tempco typical. **Computer Products,** 1400 NW 70th St, PO Box 23849, Fort Lauderdale, FL 33307.
Circle 220 on Inquiry Card

IEEE-BUS-COMPATIBLE MAGNETIC TAPE FORMATTER

Model 1015A allows the user to add any industry std magnetic tape drive to the general-purpose interface bus (IEEE 488-1975). It provides asynchronous data transfer to and from synchronous tape recorders. Features include read-after-write error checking with automatic correction, rapid recording rates, and no loss of data during interrecord gaps. A dedicated Z-80 microprocessor manages both bus interface and memory management functions. Formatter is available in 7-track (200, 556, or 800 char/in. NRZI), 9-track (800 char/in.), or 9-track 1600 char/in. PE. **Dylon Corp,** 7854 Ronson Rd, San Diego, CA 92111.
Circle 221 on Inquiry Card

SOLID-STATE RELAYS

Challenger series units offer power ratings to 8 A, and feature zero voltage turn-on, internal snubbers for the Triac, half-cycle response, and firm bistable turn-on action. In addition, they accept spade-type quick-connect terminals. Series 2, a panel mount version, is transfer molded with overall dimensions of 1.75 x 0.81 x 0.60". Load current rating is 8 A rms when mounted on a heat sink. Series 3, a PC mount version, is ⅜" high and is rated for 2 A rms. **International Rectifier Corp, Crydom Div,** 1521 Grand Ave, El Segundo, CA 90245.
Circle 222 on Inquiry Card

SYNCHRONOUS MULTIPLEXER

Timeline 290 Miniplexer, a synchronous time division multiplexer, will split a 2400-, 4800- or 9600-bit/s facility, DDS or conventional, into two, three, or four separate channels. Users of Bell 209 data sets can switch to DDS without losing bandsplitting benefits. Inputs may be a mix of DDS and conventional at speeds of 600, 1200, 2400, 4800, and 7200 bits/s. Input speeds are switch selectable and LED indicators display mode of operation. A switch for each channel sets it in local loop or test mode. **Infotron Systems Corp,** 7300 N Crescent Blvd, Pennsauken, NJ 08110.
Circle 223 on Inquiry Card

HIGH TEMPERATURE PC CARD BUS

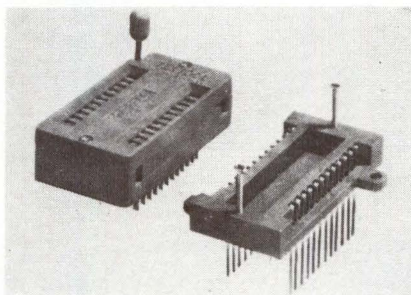
E series model B10200/B10300 is capable of withstanding high temperatures and extended dwell times in wave soldering. Utilizing Nomex and Kapton, combined with a special thermosetting adhesive system, the parts (both vertical and flat DIP bus) withstand soldering temperatures up to 520°F and solder wave dwell of up to 30 s with no danger of delamination or deterioration. Buses are available in single- and multi-layer types. Radius pin tips are provided for easy insertion. **Bussco Engineering Inc,** 119 Standard St, El Segundo, CA 90245.
Circle 224 on Inquiry Card

PRODUCTS

SPDT SUBMINIATURE SLIDE SWITCH

With a PC mounting terminal, model 1101CQ features a low profile slide actuator measuring 0.152 in.^{2} (3.86 mm) x 0.200" H (5.08 mm). Switch body measures 0.500 (12.7 mm) x 0.260 (6.60 mm) x 0.250" (6.35 mm). Actuator sits atop field proven internal mechanism. With spring-loaded teflon contact follower, slide retains same terminal sealing and options available with toggle switches. Contact rating is 6 A with resistive load at 120 Vac or 28 Vdc; 3 A with resistive load at 250 Vac. **C&K Components, Inc,** 103 Morse St, Watertown, MA 02172.
Circle 225 on Inquiry Card

DIP SOCKET/RECEPTACLE



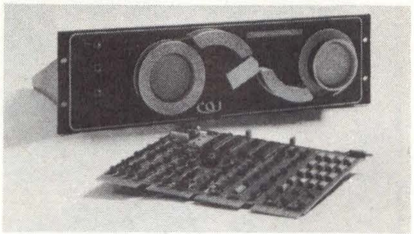
ZIP DIP II socket/receptacle series features enlarged entry for use with a wider range of devices, and a flat top plate for easier entry and extraction. Contacts are on even 100-mil spacing (300-400-600 mil) for convenient mounting on std hardware. A built-in "stop" insures that the socket handle cannot be easily overstressed. Top mounted assembly screws facilitate replacement of damaged or worn internal parts. Virtually eliminating mechanical rejects, device has a typ life of 25,000 to 50,000 insertions. **Textool Products, Inc,** 1410 W Pioneer Dr, Irving, TX 75061.
Circle 226 on Inquiry Card

PC CARD GUIDE/HEAT SINK

Series 1000 metal (phosphor bronze, beryllium copper, or stainless steel) PC card guide, when assembled into an aluminum heat sink guide bar (GBH-1000), offers exceptional heat dissipation. Spring-finger action of the card guide firmly presses one edge of the PC card into contact with the guide bar over its entire length, providing an extremely large contact area for effective heat transfer. Guide bar and card assembly can be mounted with mounting clips at each end or epoxied or riveted directly to the chassis. **Unitrack Div, Calabro Plastics, Inc,** 8738 W Chester Pike, Upper Darby, PA 19082.
Circle 227 on Inquiry Card

PRODUCTS

LSI-11 COMPATIBLE MAGNETIC TAPE SYSTEM

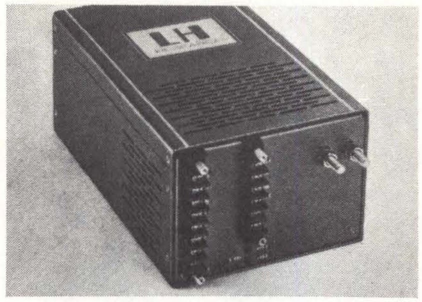


CO-3000LSI LINC tape is DECtape[R] compatible and offers media interchangeability with any computer equipped with DECtape. With capacity for 148K 16-bit words in blocks of 256, the unit offers direct access storage suitable for tough industrial environments. A tape driver for DEC's RT-11 operating system supports MACRO, EDIT, LINKER, FORTRAN IV, and BASIC. The system can be used in real-time systems for overlays and data acquisition. Controller occupies a quad slot in the LSI-11 and contains a FIFO buffer and optional ROM bootstrap. **Computer Operations, Inc,** 9700-B George Palmer Hwy, Lanham, MD 20801.
Circle 228 on Inquiry Card

OPTICAL COUPLER

TTL compatible with a specified 1 through 10 unit lead saturated output capability, the MCT210 has a specified min CTR of 50% saturated, and 150% unsaturated over a temp range of 0 to 70°C. The device incorporates a GaAs diode emitter coupled to an npn silicon planar phototransistor. Saturated output voltage (V_{OL}) collector to emitter is 0.2 V typ (specified max of 0.4 V) with collector current of 16 mA and input current of 32 mA. Saturated switching times are 2.5-μs typ rise time, and 2.5-μs fall time. **Monsanto Commercial Products Co, Electronics Div,** 3400 Hillview Ave, Palo Alto, CA 94304.
Circle 229 on Inquiry Card

5-OUTPUT SWITCHING POWER SUPPLY

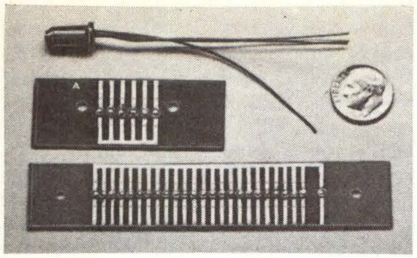


Producing up to 750 W of power in a 5.10 x 7 x 12.75" package, model MM-450 is up to 80% efficient and features 1% pk-pk or 50-mV pk-pk ripple and noise on output, line regulation of 0.4% over the entire input range, and load regulation of 0.4% from no-load to full-load. Response time is 200 μs to 1% after 25% load change. Primary output is 5 V at 150 A; the four other outputs can be 5 V at 5 A, 12 V at 5 A, 15 V at 5 A, 18 V at 4 A, or 24 V at 3 A to a total max of 750 W. **LH Research, Inc,** 1821 Langley Ave, Irvine, CA 92714.
Circle 230 on Inquiry Card

SYNCHRO-TO-RESOLVER CONVERTER

The 60-Hz unit (part number 52448) converts 90-V line-to-line synchro information to 6-V sine and cosine information. Nominal dimensions are 1 x 1⅝ x 11/16", providing close board to board spacing in multiboard systems and in potted modules; 0.040" diameter pins are provided for mounting. Basic accuracy of 1 arc min. is achieved by accurate magnetic transformation ratio, and is independent of temperature or age. With isolation from high common mode synchro bus voltage and transients, no synchro bus grounding is required. **Magnetico, Inc,** 182 Morris Ave, Holtsville, NY 11742.
Circle 231 on Inquiry Card

MARK-SENSOR ARRAYS

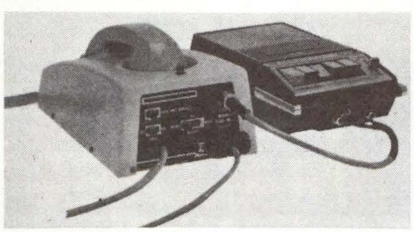


The CYCLOPS single channel device has a microminiature GaS emitter and Si detector in one integral package. Field of vision is zero and there is no focal point or blind spot as with conventional configurations. Used to detect paper or card edges, holes, pencil marks, patterns, applications include industrial processing and control, computer card reading, and shaft or position encoders. A 6-channel custom array on 0.125" centers, and a 22-channel array on 0.1" centers are also available. **Ultra Sensors, Inc,** 2400 W 102nd St, Suite 313, Minneapolis, MN 55431.
Circle 232 on Inquiry Card

DYNAMIC GRAPHIC DISPLAY

For use with any 16-bit minicomputer, QVEC refreshed graphic display system comprises display generator, 17 or 21" display screen, and computer interface. Display generator produces dots, lines, or characters on an X-Y coordinate matrix of 1024 x 1024 points. Hard copy can be obtained by using a std X-Y analog plotter connected to the generator's plotter output. Data are stored in the user's computer memory and are automatically output periodically by the DMA interface without program intervention. **Sigma Electronic Systems Ltd,** Church St, Warnham, Horsham, Sussex, RH12 3QW England.
Circle 233 on Inquiry Card

ACOUSTIC COUPLER

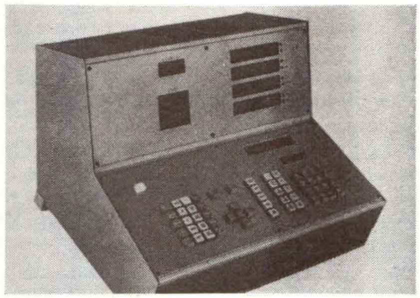


Model 302C provides for data transfer between a remote computer, a local terminal, and an ordinary audio mag tape cassette unit. Unit is a 300-baud acoustically coupled modem providing carrier indicator, full/half-duplex, and mag tape unit interface. Data are recorded and retrieved in the form of records and blocks as determined by an operator selectable switch which may be set to retrieve all data without marker interruptions. At 300 baud, the recorder stores up to 150K characters on ordinary cassettes. **ComData Corp,** 8115 Monticello, Skokie, IL 60076.
Circle 234 on Inquiry Card

REMOTE DATA ENTRY KEYSTATION

Remote keystation capability for the CMC 1800 allows operators at remote sites to enter, verify, correct, and update data via telephone lines under control of a central supervisor. A keypunch-style keyboard (1155) or a typewriter-style keyboard with numeric pad (1156) are independently movable; both models use standard CMC software. Data transmission to and from remote stations is asynchronous, full-duplex, on 2- or 4-wire systems. **Pertec Computer Corp, CMC Div,** 2500 Walnut Ave, Marina del Rey, CA 90291.
Circle 235 on Inquiry Card

AUTOMATIC POSITIONING SYSTEM CONTROLLER



Using a microprocessor for positioning up to four axes for combinations of linear or circular motion, Anomatic™ controllers feature the use of a 12-V CMOS bus, which interconnects the microprocessor to all I/O devices. All logic and controls are CMOS; microprocessor, p/ROM, and ROM, located in one section of a card, are TTL. Noise immunity is 4.8 V throughout. System contains built-in p/ROM programmer to provide nonvolatile memory, and can be programmed from internal memory, paper tape, cassettes, or mag cards. **Anorad Corp,** 115 Plant Ave, Smithtown, NY 11787.
Circle 268 on Inquiry Card

FLOATING POINT ARRAY FOR H-P 2100

Computational capability of Hewlett-Packard's 2100 series can be greatly expanded by the addition of this programmable array processing peripheral which increases the system's processing speeds by as much as several orders of magnitude without sacrificing accuracy or precision. Ability to efficiently handle a wide range of algorithms is gained; multiprocessor architecture offers enhanced speed and the advantage of optimized throughput by overlapping of input, output, arithmetic, and executive operations. **CSP Inc,** 209 Middlesex Tpk, Burlington, MA 01803.
Circle 269 on Inquiry Card

DIGITAL CASSETTES

Abraxas V cassettes feature selection of write enable-write inhibit, optional BOT/EOT marker holes, and interlocking tongue and groove case construction to eliminate contamination. Model V-F is a general-purpose unit designed to function on tape drives with built-in guidance systems; model V-C provides its own tape control. V-W is made for word processing equipment, automatic text editing typewriters, and computer-aided word processors; and the V-I is designed for Wang programmable calculators. **CFI Memories, Inc,** 305 Crescent Way, Anaheim, CA 92801.
Circle 236 on Inquiry Card

FLOPPY DISC SEND/RECEIVE TERMINAL

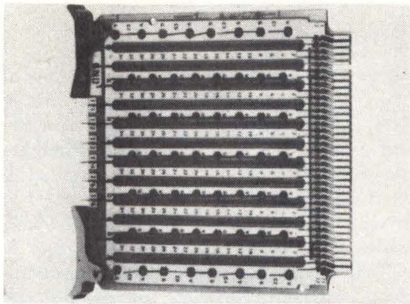
A 2-way batch terminal with complete editing and data search capability, disc storage for over 311K char, and full RS-232 interface compatibility, the RDS/FDSR is plug-compatible with existing RS-232 data terminals. Over 2400 addressable lines of 128 char can be accessed from the terminal within 0.3 s or from asynchronous CRT or keyboard/printer terminal. **Randal Data Systems Inc,** 365 Maple Ave, Torrance, CA 90503.
Circle 270 on Inquiry Card

DUAL OUTPUT LIGHT PEN

Solid-state assembly of the 120-1 utilizes optoelectronic and hybrid circuitry to provide TTL-compatible "light pen switch" and "light pen hit" outputs. A switch signal is generated whenever the tip of the pen is pressed against the CRT faceplate; hit occurs when an unblanketed spot on the faceplate is under the pen tip. Signals are transmitted through the light pen cable to control logic of the terminal subsystem. The IBM-compatible unit features fast signal response time, excellent resolution, and high ambient light rejection. **HEI, Inc,** Jonathan Industrial Ctr, Chaska, MN 55318.
Circle 271 on Inquiry Card

PRODUCTS

SMALL WIREWRAP IC BOARDS



IC pluggable packaging assemblies measure as little as 4.86 x 4.38" and contain as many as 12, 18, or 24 IC positions. A universal version consists of 12 columns of 35 socket/terminals on 0.100" centers; a high density version has from 16 to 20 universal columns and 12 test terminals. Card-edge connector is std on all versions. Series ECM 72 has 14 or 16 socket/terminals per IC position, with or without voltage and ground sockets. Wirewrap posts can be provided for 1-, 2-, or 3-level wrapping. **Garry Manufacturing Co,** 1010 Jersey Ave, New Brunswick, NJ 08902.
Circle 237 on Inquiry Card

ENDLESS LOOP TAPE TRANSPORT

Model A5 uses std NAB A size cartridge and has a self-governed dc motor that maintains exact speed over a 10- to 16-V range. Electrically controlled for remote operation, the fail safe design protects tape and transport in case of power interruption. Industrial 4-point mounts for both heads provide separate zenith, height, and azimuth adjustments. High traction, self-aligning pinch roller contains instrument ball bearing, eliminating tape edge wear. Front panel permits easy cartridge loading. **Amilon Corp,** 49-12 30th Ave, Woodside, NY 11377.
Circle 238 on Inquiry Card

INTELLIGENT MODEM

The model 4910 provides dial-up capability for timesharing terminals through DDD at 10, 20, or 30 char/s transmission speeds, access to the TWX network, direct hook-up for a local computer communications front-end, or access to the TWX/DDD networks for multiple add-on terminals through a special RS-232-C interface. Switch-selectable printing speeds are 10, 20, and 30 char/s, 80 or 132 print positions. Single or dual magnetic tape cassettes and 1200-baud tape transmission are provided. **Omnitec Corp,** 2405 S 20th St, Phoenix, AZ 85034.
Circle 239 on Inquiry Card

132-COLUMN LINE PRINTERS

Using the rotating belt technique, two models impact-print u/lc text. Speed depends on the number of printable char/line. Model 9212 prints 120 to 240 lines/min.; model 9214 prints 230 to 240 lines/min. Operator controls and indicator lamps are straightforward and easily understood. Ample use of sound-deadening material keeps noise to a minimum. Std sprocket-fed paper can be fed directly from the shipping carton and the finished printout stacked in a tray for easy removal. **Datapoint Corp,** 9725 Datapoint Dr, San Antonio, TX 78284.
Circle 240 on Inquiry Card

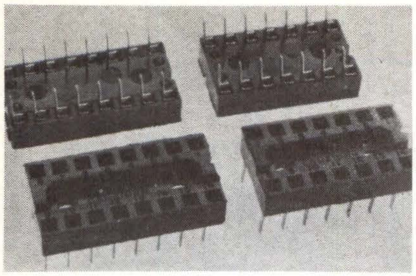
DATA TABLET/GRAPHIC CALCULATOR INTERFACES

Capable of interfacing the company's products to the Tektronix 4051 graphic calculator, interfaces are available for both series of data tablets. Interface for the HW series is housed in a separate box while the microprocessor-controlled digitizer ID series is contained on a card internal to the electronics controller. Interface enables the transfer of X-Y coordinate values from the tablet to the calculator. All status bits, control functions, and handshaking signals are also transmitted. **Summagraphics Corp,** Box 781, Fairfield, CT 06430.
Circle 241 on Inquiry Card

CIRCLE 75 ON INQUIRY CARD

CIRCLE 76 ON INQUIRY CARD

LOW PROFILE SOLDER-TAB SOCKETS

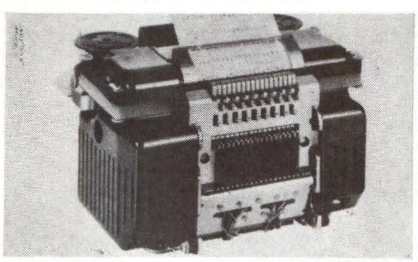


With a profile of only 0.156″ above the board, the 14- and 16-pin sockets feature good lead-in for IC leads as well as closed-entry for protection of contact springs. Contact spring compliance is achieved without compromise in the normal force on component leads. Design includes inverted contacts which apply pressure to the flat sides of the DIP lead, and a molded lead-in funnel which guides the DIP into the contact area and protects against contact damage. Housings are glass-reinforced nylon. **Cambridge Thermionic Corp,** 445 Concord Ave, Cambridge, MA 02138.
Circle 242 on Inquiry Card

BIT ERROR RATE TESTER

Complete end-to-end performance testing of communication links, tape recorders, bit synchronizers, or any PCM system having a bit rate within the 1- to 5M-bit/s range is provided by the model 721. Two basic data patterns generated are a 16-bit word, with each bit front panel selectable; and a 2047-bit pseudo-random word. Frame length is selectable from 1 to 512 words/frame, in increments of powers of two. A bit-blanking function is provided for bit synchronizer flywheeling or coasting measurement. **EMR-Telemetry,** PO Box 3041, Sarasota, FL 33578.
Circle 243 on Inquiry Card

DIGITAL IMPACT PRINTER



Model 102 digital impact printing mechanism is a parallel-entry 18-col printer with std 13-char font that can also be customized. Print speed is 2.7 lines/s, in black and red, on 2½″-wide std paper (pressure sensitive may be used). Driven by a Shinshu Seiki transistorized brushless constant-speed dc motor requiring low operating power (15 Vdc, 490 mA max), printer is guaranteed for MTBF of 5M lines of continuous operation. Printer measures 3⅜ x 5¾ x 4⅞″. **C. Itoh Electronics, Inc, Systems and Components Div,** 280 Park Ave, New York, NY 10017.
Circle 244 on Inquiry Card

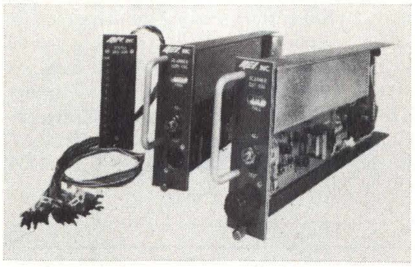
PDP-11/70 PLUG-COMPATIBLE CORE MEMORY

The ARM-1170, a transparent alternative to or replacement for MJ11 memories used in PDP-11/70 computers, is available in 128K-byte (32K words of 36 bits each) increments and is capable of expanding the computers to their max 4M-byte capacity within the two system cabinets. Throughput enhancement is provided by 2- or 4-way internal interleaving. 4-way interleaving gives an effective cycle time of 350 ns, compared with 800 ns for the basic memory or 1000 ns for DEC memory. **Ampex Corp, Memory Products Div,** 200 N Nash St, El Segundo, CA 90245.
Circle 245 on Inquiry Card

PROCESSOR STORAGE SYSTEM

Multimemory/168 for IBM 370/168 computer installations is designed for memory capacities of up to 8M bytes on a single processor and 16M bytes on a multiprocessor. It is completely compatible and attachable to all IBM 168 models. A maintenance deferral system allows the operator to detect memory failure via lighted display on the system's panel, and correct the failed memory block by flipping a switch to automatically remove the block from the system and restore address continuity. **Electronic Memories and Magnetics Corp, Systems Equipment Div,** 3216 W El Segundo Blvd, Hawthorne, CA 90250.
Circle 246 on Inquiry Card

DIGITAL SCANNER SYSTEM

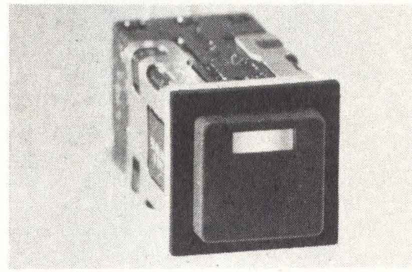


Featuring time and frequency division multiplexing in each compact transmitter and receiver module, QSS-1130 is an all solid-state system that permits transmission and reception of up to 11 discrete data points at speeds up to 30 bits/s as std, or control in some applications. System consists of a QST-1130 scanner transmitter, QSR-1130 scanner receiver, optional QSD-1130 status display unit, and optional (separately mounted) QSK-1130 relay output. Combination QSKD-1130 relay and status display unit is also available. System uses CMOS digital logic. **QEI, Inc,** 60 Fadem Rd, Springfield, NJ 07081.
Circle 247 on Inquiry Card

INCREMENTAL-DIGITAL POSITIONING CONTROL

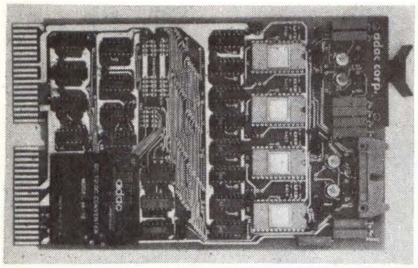
CSR servo translator is a high response, closed loop system that accepts digital positioning commands in the form of a serial pulse train. Each pulse causes the motor to move one step in either a clockwise or counterclockwise direction. Rate at which pulses are received determines motor speed. Features include absolute digital translator subtractor circuitry and a patented pulse-width modulated driver for controlling high response, permanent magnet motors. Torques are provided up to 300 in.-lb. **Control Systems Research, Inc,** CSR Bldg, 632 Fort Duquesne Blvd, Pittsburgh, PA 15222.
Circle 248 on Inquiry Card

LED PUSHBUTTON SWITCHES



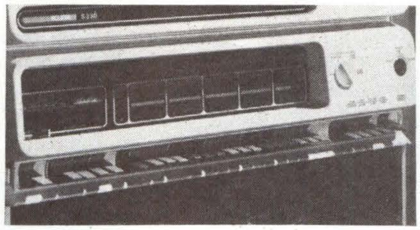
A funnel-shaped reflector at the base of the diode helps beam red, yellow, and green lights to the front display surface of the pushbutton/indicator. The 5-, 10-, and 15-Vdc switches have an internal resistor to maintain current at a nominal 20 mA. They are available with momentary or 2-level alternate action (push on/push off) and with three types of IC functions: 5-V sink, 5-V source, and 6- to 16-V regulated sink. Rectangular bar type LED lighting is offered in 1- and 2-pole form C control arrangements. **Micro Switch, a div of Honeywell,** 11 W Spring St, Freeport, IL 61032.
Circle 249 on Inquiry Card

LSI-11 COMPATIBLE D-A SYSTEM



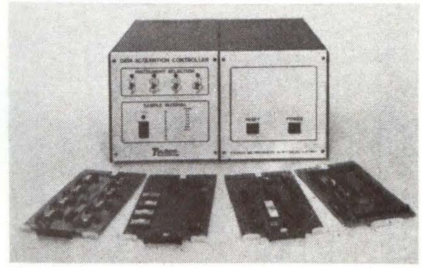
Model 600-LSI-11D is a digital to analog system compatible with the DEC LSI-11 and PDP-11/03 microcomputers. Basic system configuration, contained on a single 5 x 8½" PC board, consists of bus interface, dc-dc power converter, scope control, and one, two, three, or four 12-bit DACs. Scope control permits visual display of data without extraneous data, such as normally occurs during DAC updating intervals. Cable and documentation are also included. A third wire sense lead from each DAC is optional. **ADAC Corp,** 15 Cummings Pk, Woburn, MA 01801.
Circle 250 on Inquiry Card

SCIENTIFIC COMPUTER



For scientific, instrumentation, and computational applications, Eclipse[R] S/230 features main memory capacity of up to 512K bytes of high speed semiconductor, core, or mixed memories; full memory mapping and protection; and an expanded data channel memory space. The 16-slot computer also has a 16-bit microprogrammed architecture with optional writable control store. This consists of 256 56-bit words of user-programmable RAM for writing specialized instructions, optional high speed single- and double-precision floating point processor, and comprehensive instruction set. **Data General Corp,** Southboro, MA 01772.
Circle 251 on Inquiry Card

DATA ACQUISITION CONTROLLER

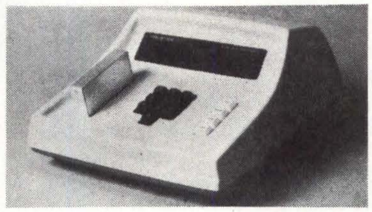


Microcomputer-based data collection and control system has both analog and digital inputs and outputs. Analog and digital input may be used for local control or stored and then sent serially to a remote site or computer. Front panel controls of the modular unit are software activated as needed. Functions are also defined in software so that changes need be made only in p/ROM, not in hardware. Additional modules include cassette, printer, and terminal interfaces, and solid-state relay controller. **Tychon, Inc,** PO Box 242, Blacksburg, VA 24060.
Circle 252 on Inquiry Card

PRODUCTS

EROM STORAGE AUTOPROGRAMMER

Model 583 will store, on interchangeable EROM cartridges, a sequence of programming commands which will automatically control the output of the company's programmable generators. Particularly useful in systems applications involving repetitive tests, the instrument stores a sequence of up to 99 separate tests on each EROM cartridge: each can be called up as required. Test cycling can be either automatic or manual. Autoprogrammer will automatically sequence through up to 100 tests (addresses 00 through 99) displaying the current test address. By programming a stop command, processing can be halted at any given address within a test. Processing can then be manually continued by control panel key. EROM cartridges can be programmed using an EROM programmer or can be custom programmed. **Wavetek,** 9045 Balboa Ave, San Diego, CA 92123.



Circle 253 on Inquiry Card

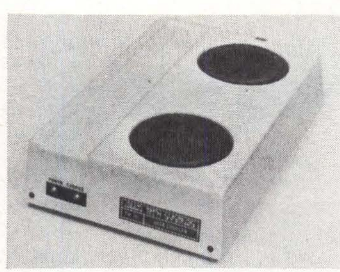
INDUSTRIAL APPLICATION MINICOMPUTER

The P851M MicroMini uses LOCMOS LSI technology, which combines LSI performance with improved noise immunity and low power consumption. The unit can be used as a micro or minicomputer to match application needs. Application software can be developed on any member of the P800M family. The general purpose bus expands to accommodate std I/O controllers and an I/O processor to ensure fast data transfer and direct memory access facility. Interface cards for digital and analog I/O mount directly in the CPU chassis. Static memories are available with from 0.5K to 2K words; dynamic memories with 4K or 8K words. Storing user applications programs, REPROMs are available in modules of 1K, 2K, or 4K words; they can be combined with RAM modules. A built-in panel gives diagnostic capability for maintenance. **Philips Data Systems,** PO Box 523, Eindhoven, The Netherlands.

Circle 254 on Inquiry Card

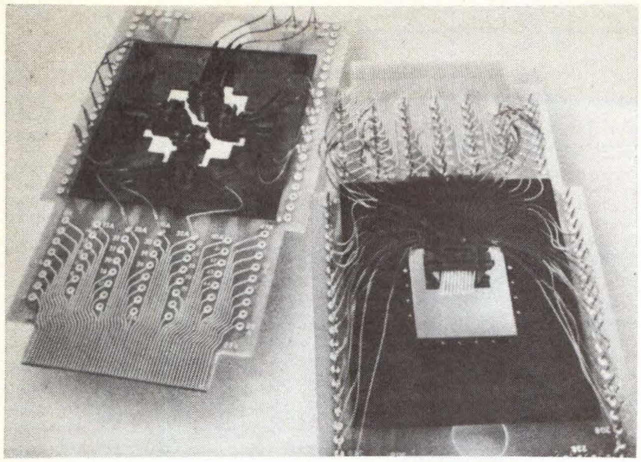
300-BIT/S ACOUSTIC COUPLER

Model FM30 transmits and receives asynchronous serial digital data at up to 300 bits/s, full- or half-duplex on DDD networks. An acoustically coupled data modem, the device permits data communication through the handset of an ordinary telephone, making it easier for timesharing users to cope with changing systems requirements, and providing mobility and portability to terminal usage. The unit is compatible with WE series 103 and 113 A/B data sets and with EIA RS-232-B/C, 20-mA current loop and TTL interfaces. Transmit frequencies are crystal controlled; the receiver uses active filters and digital detector. Sensitivity is −40 dBm. Frequency stability is ±0.1%, and transmit level is −16 dBm. Power requirements are 115 Vac, 60 Hz. **Multi-Tech Systems, Inc,** 3406 University Ave SE, Minneapolis, MN 55414.



Circle 255 on Inquiry Card

FIXED-POINT PROBE CARD ASSEMBLY SYSTEM



The Para-Probe™ system permits simple assembly of fixed point probe cards from a kit of components. A patented double cantilevered probe block eliminates pad scrub while retaining wipe action to remove surface oxides for virtually zero point-to-pad contact resistance. Probe blades are replaceable, probe cards rebuildable, and components reuseable. The parallel method of construction allows high probe densities, making it possible to build cards with multiple interlocking parallel base blocks and forming a single module with an infinite number of probes in a straight line. Base blocks can also be mounted at 45-deg to dice side for contacting corner pads. Center-to-center spacing of 0.004" can be achieved. **Alignment Enterprises,** Dept 100, 9537 Telstar Ave, Suite 132, El Monte, CA 91732.
Circle 256 on Inquiry Card

16-CHANNEL ANALOG MULTIPLEXER

Model 4550 contains digital input buffers, decoder logic, analog switches, and an output buffer amplifier in a single package. It switches one of 16 inputs (switching action is break-before-make) to a common output depending on the state of the four address lines and the enable input. The unit can accept an input voltage range to ±10 V with an accuracy of ±0.01%, and has a max input overvoltage of ±35 V. Digital inputs are buffered with Schmitt trigger logic and have an overvoltage capability of ±19 V. Output settling time for a 20-V step to ±1 mV is 3 μs max (including 1-μs switching time). The number of input channels may be expanded by tying additional multiplexers together by connecting the op amp input terminals. **Teledyne Philbrick,** Allied Dr at Rt 128, Dedham, MA 02026.
Circle 257 on Inquiry Card

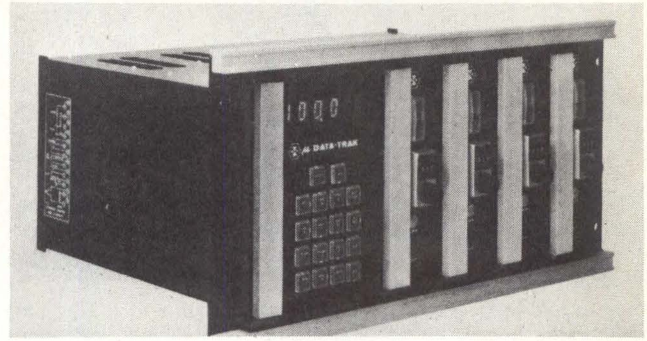
MULTI-OUTPUT SWITCHING POWER SUPPLY

A 4-output, 400/475-W supply, the model 674/675 is designed specifically for microprocessors, small computers, or add-on memories. Features include a main output for logic, a second for memory, and two for accessory power needs. Measuring 5 x 8 x 14.33", and weighing 15 lb, the unit has >60% efficiency, and a MTBF of >30,000 h. Outputs are: rail 1—2 or 5 Vdc out at 50/70 A (674/675 respectively); rail 2—≤12 Vdc at 10/8 A, or >12 at 120/96 W; rail 3 and 4—≤15 at 4/4 A, or >15 at 60/60 W (no second rail). Input is strappable to 102 to 130/188 to 256 Vac, 45 to 63 Hz, single phase. Dynamic regulation is 1% for each 10% of load current step. Output ripple and noise are 20 mV rms typ, 50 mV pk-pk. **Trio Laboratories, Inc,** 80 Dupont St, Plainview, NY 11803.

Circle 258 on Inquiry Card

PRODUCTS

MICROPROCESSOR-CONTROLLED PROCESS PROGRAMMER

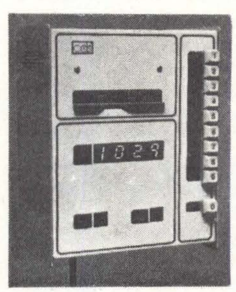


Model 5600 μ-DATA TRAK reduces programming costs and increases flexibility for industrial process programmers by providing one or two analog set point programs for process manipulation vs time, plus seven programmable on/off event functions. Programs are generated by best-fit straightline segments of a desired profile, stored and retrieved using digital and microprocessor techniques. Capacity for up to 40 line segments is available with process resolution to one part in 1000. Programming entry into the micro's memory is via a keyboard on the front panel. Sixteen pushbuttons allow the operator to select 28 functions. Front panel display is 0.47" tall incandescent digits plus sign. The device provides programmed output voltage of 0 to 5 V into 500 Ω and output current of 4 to 20 mA into 500 Ω. **Research, Inc,** PO Box 24064, Minneapolis, MN 55424.
Circle 259 on Inquiry Card

PUSHBUTTON SWITCHES

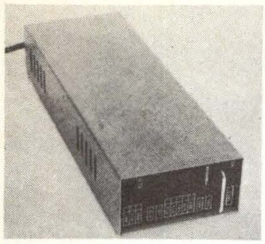
Using a pair of formed wires for actuation, contact, and termination, spst switch eliminates the snap-acting leaf spring and provides low bounce characteristics with high current-carrying capacity and long mechanical life. The two formed wires handle three functions: tactile feel and spring return, surfaces for electrical contact, and termination areas for solder or wirewrap connection. Most applications require no buffering; minimum buffering is needed for TTL and MOS circuitry. Contact surfaces move against each other, and are wiped electrically clean during each make/break cycle. Designed for direct-strip or matrix mounting on PC boards, the switch has a nom switch life of >10 million cycles carrying a 12-V, 0.4-A load. **RTC Inc,** 343 E Fillmore, St. Paul, MN 55107.
Circle 260 on Inquiry Card

DATA COLLECTION TERMINAL



A microprocessor-based data collection terminal, the Smart Clock interfaces with virtually any type of processor. The terminal, which can operate in either a real-time/online or standalone mode, reads up to 16 digits of Hollerith code from plastic ID badges and IBM cards, and will also accept numeric information via 10 pushbuttons. The unit contains up to 1.7K of factory-programmed ROM and up to 14K of data capacity. An internal battery insures nonvolatility in the event of power failure. Up to 64 terminals can be connected on the same interface line. Data are relayed to the host processor in ASCII form through either an RS-232-C, 20-mA current loop or built-in 600-baud modem interface. **Coastal Data Services, Inc,** 1592 NW 159th St, Miami, FL 33169.
Circle 261 on Inquiry Card

SYNCHRONOUS LINE DRIVER

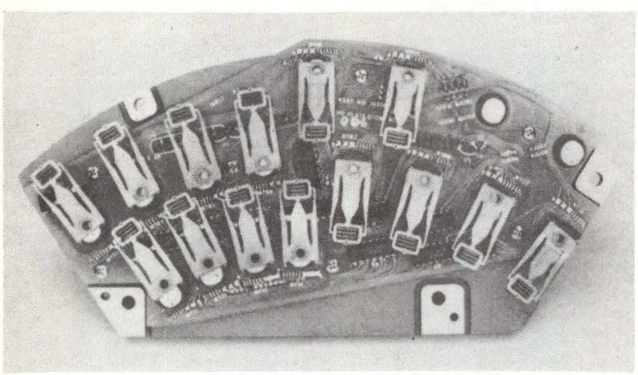


Providing synchronous data transmission rates which allow full utilization of terminals, CPU ports, and data transmission lines, the SLD operates over common loaded multigauge cable at baud rates of >4800 bits/s. Over nonloaded cable, speeds of >19,200 bits/s are possible. All data rates are switch-selectable. Transmission distance ranges up to 25 mi. Each unit incorporates complete diagnostic capabilities including local and remote loopbacks, nine diagnostic LED indicators, and a pseudorandom word generator for self testing. Digitally generated sinewave output allows the device to conform to Bell spec 43401. A crystal oscillator is used for both signal generation and system timing. The units perform equally well in half- or full-duplex mode as well as in a polled environment. **Prentice Electronics,** 795 San Antonio Rd, Palo Alto, CA 94303.
Circle 262 on Inquiry Card

INTELLIGENT PRINTING TERMINALS

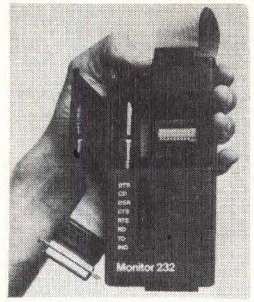
The Carousel line features a power front-forms insertion device, which automatically feeds ledger cards, single sheets, and bottom-glued multipart forms into the platen. An additional accessory enables the device to handle multipart forms which are not bottom-glued, even when the sheets are of varying length. Model 320, a complete computer I/O printing terminal, includes a 120-char/s paper tape reader and plotting capability, and can replace an ASR Teletype[R], high speed printer, and plotter with a single unit. The 350 has a split platen and can accommodate two paper-handling devices simultaneously. The 310 provides a single platen, enables 4800-point/in.^{2} plotting capability, and accepts any forms-handling device. **Perkin-Elmer Data Systems, Terminals Div,** Randolph Pk W, Rt 10 and Emery Ave, Randolph, NJ 07801.
Circle 263 on Inquiry Card

DISC MEMORY READ/WRITE FLYING HEAD ASSEMBLY



The FH 140 assembly incorporates a Winchester-type digital data transducer for use in fixed head-per-track or hybrid (moving plus fixed head) disc systems. Available with both 3-track (model 143) and 5-track (145) gimbal subassemblies, units provide 42 or 70 tracks, respectively. Standard are Winchester-type ferrite sliders with 9.5-mil track widths on 60-mil centers, which provide 67-track/in. density. Design operates on both oxide and nickel-cobalt discs under contact start/stop conditions. When coupled with the assembly, Winchester-type discs provide for a straightforward head/disc interface which can be designed into a complete disc system. The assembly can also be used in existing moving arm drive systems with only nominal design changes. **National Micronetics, Pacific Div,** 5600 Kearny Mesa Rd, San Diego, CA 92111.
Circle 264 on Inquiry Card

HAND-HELD DATA COMMUNICATIONS SYSTEM

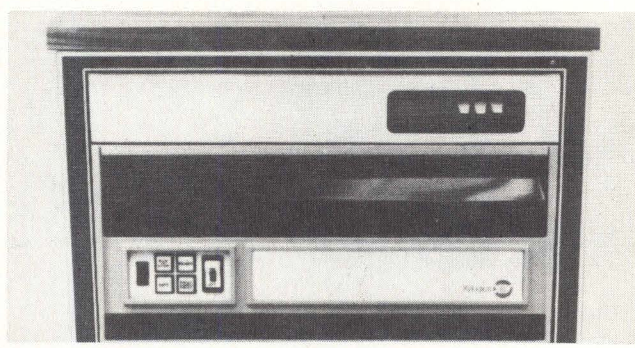


Designed to monitor data communications systems to EIA spec RS-232-C, the 232 provides a simple yet effective method of checking system operation and enables problems to be identified and located quickly when breakdowns occur. The lightweight, self-contained, and rugged unit can be conveniently carried for use in testing and servicing applications, or left permanently connected to a circuit for continuous monitoring. It indicates the condition of the data communications system under test, permits direct access to individual signal lines, and allows operation of the system terminal in echo mode. Continuous displays of DRT, CD, DSR, CTS, RTS, RD, TD, and Test Indicator are given on eight LEDs. Pin connections are available for oscilloscope monitoring. **Goodwood Data Systems,** Box 768, Ogdensburg, NY 13669.
Circle 265 on Inquiry Card

DIGITAL LOGIC BOARD TEST SYSTEM

Featuring a guided clip/probe, the MAGICLIP system is an optional hardware/software package for the 6500 test/programming station. Hardware consists of a 16-pin IC clip and a single-tip probe. Either can be used for troubleshooting; both are cable-connected to circuitry in the 6500 test head. In troubleshooting mode, diagnostic information (ie, clip or probe placement) is retrieved from the data base stored in the 6500. After plugging in the board to be tested and entering a few simple instructions via the keyboard, the operator is told automatically by the system where to place the clip to trace a failure, and the precise cause of failure is reported. In addition to information displayed on the CRT, a printer-generated hardcopy contains full diagnostics plus board serial number. **Mirco Inc, Systems Div,** 10888 N 19th Ave, Phoenix, AZ 85029.
Circle 266 on Inquiry Card

DISC SUBSYSTEM



Integrating large storage disc capacity and fast access time of cartridge discs with capabilities of DEC's LSI-11 CPU, the Phoenix 145 system is an alternative to DEC's 11V03. LSI-11 architecture is directly interfaced to the Phoenix 45 disc controller, eliminating the need for a Q bus/Unibus adapter. Packaged in a rack-mountable chassis with an operator's control panel and a 9-slot backplane, the system can be configured to support up to 20M bytes of disc capacity, four terminals, line printer, and a 28K-word LSI-11 processor. Housed in a 30″ standalone cabinet are the chassis, controller, and 5M-byte disc drive. Controller features include sector address verification, multiple sector transfers, write protect to the sector level, and self-test capability. **Xylogic OEM Components Group, Inc,** 42 Third Ave, Burlington, MA 01803.
Circle 267 on Inquiry Card

LITERATURE

Standard Circular Connectors

In-depth descriptions, specs, and applications of MIL-C-5015 MS std connectors are supplied in brochure featuring charts and drawings. **ITT Cannon Electric,** Santa Ana, Calif.
Circle 300 on Inquiry Card

Disc Cartridge Requirements

Mag media and disc cartridge requirements for D36XX disc drives are discussed in application notes, along with disc storage capacity, storage and handling procedures, and electrical signal characteristics. **Pertec Corp, Peripheral Equipment Div,** Chatsworth, Calif.
Circle 301 on Inquiry Card

Miniperipherals

Illustrated catalog describes uses and features of line of memory, disc, and paper tape peripherals for DEC, Data General, and Interdata minicomputers. **Plessey Microsystems,** Irvine, Calif.
Circle 302 on Inquiry Card

Switches

Detailed descriptions and specs on miniature switch items are listed in catalog featuring subminiatures, miniature 250-V, and line of miniature oil-tight controls. **Alco Electronic Products, Inc,** North Andover, Mass.
Circle 303 on Inquiry Card

Semiconductors

Complete with charts and diagrams, updated condensed catalog consists of latest product listings and technical specs on ICs, interface circuits, MIL devices, and discrete components. **ITT Semiconductor,** Woburn, Mass.
Circle 304 on Inquiry Card

Microprocessor

Brochure on the EA9002 8-bit microprocessor features functional descriptions, timing diagrams, definitions, applications, instruction formats, and two block diagram systems configurations. **Electronic Arrays, Inc,** Mountain View, Calif.
Circle 305 on Inquiry Card

Bipolar Transistors

Modeling the Bipolar Transistor gives circuit designers information on model selection and describes equipment and techniques for parameter measurements. Price is $8. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.

A-D and D-A Converters

Two applications bulletins detail A-D and D-A parameters to improve user understanding of parameter definitions, specs, test methods, and error calculations through diagrams and tables. **Teledyne Philbrick,** Dedham, Mass.
Circle 306 on Inquiry Card

Time Division Multiplexer

Technical information and features of the TDM 1203, which uses LSI technology to provide reliability and minimize power, are contained in bulletin. **General DataComm Industries, Inc,** Wilton, Conn.
Circle 307 on Inquiry Card

Control Panels

Illustrated layout design guide considers operator requirements, environmental considerations, manual controls, visual displays, and maintainability, as well as color, coding, and illumination. **Micro Switch, a div of Honeywell,** Freeport, Ill.
Circle 308 on Inquiry Card

Data Communication Service

Brochure packet describing the data comm service includes summary information, specs, and characteristics, plus operational and management guidelines. **Datapro Research Corp,** Delran, NJ.
Circle 309 on Inquiry Card

Miniprocessor Components

Designed for OEM customers, the 21MX-K series is covered in two brochures providing a summary of applications and hardware specs. **Hewlett-Packard Co,** Palo Alto, Calif.
Circle 310 on Inquiry Card

Display and Recording Devices

Sectionalized by product categories of CRTs, display storage tubes, and flat panel display, illustrated catalog contains spec tables, diagrams, and applications information. **Westinghouse Electric Corp,** Pittsburgh, Pa.
Circle 311 on Inquiry Card

IEEE Standards

Catalog lists over 350 publications and provides a subject index to standards covering test methods, units, definitions, graphic symbols, and application methods. **Institute of Electrical and Electronics Engineers, Inc,** New York, NY.
Circle 312 on Inquiry Card

Computer Power Center

Brochure includes operation, application, and installation details of center which provides flexible power distribution for computer installations. **Computer Power Systems Corp,** Costa Mesa, Calif.
Circle 313 on Inquiry Card

Programmable Rotary Encoded Logic Switch

Brochure provides features, options, specs, and dimensional drawings of the P/rel 700 which achieves up to 60 detent positions. **Standard Grigsby, Inc,** Aurora, Ill.
Circle 314 on Inquiry Card

Incandescent Displays

Short-form catalog provides a chart of complete specs for Pinlite[R] displays, connectors, decoder/drives, lamps, and assemblies. **Refac Electronics Corp,** Winsted, Conn.
Circle 315 on Inquiry Card

Solid-State Relays

Highlights of short-form catalog include features, electrical specs, spec notes, thermal ratings, and dimensions of SSRs. **Opto 22,** Huntington Beach, Calif.
Circle 316 on Inquiry Card

Indicator Lights

Design considerations and specs of several indicator light series containing solid-state, neon, and incandescent lamps are supplied in OEM selection guide. **Industrial Devices, Inc,** Edgewater, NJ.
Circle 317 on Inquiry Card

Power Supply Efficiency

Providing guidelines for effective thermal management, technical article offers semigraphical methods for estimating heat rise and reliability of power supplies. **Semiconductor Circuits, Inc,** Haverhill, Mass.
Circle 318 on Inquiry Card

Rotary Switches and Stepping Drum Programmers

Descriptions and photographs of rotary and impact switches and switch products, as well as application ideas, are highlighted in bulletin. **Cole Instrument Corp,** Costa Mesa, Calif.
Circle 319 on Inquiry Card

Programmed Logic

Presenting sample programs and applications of programmed logic, 56-page plan book deals primarily with design and documentation of 4004 and 4040 microprocessor systems. Copies are $5 from **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940.

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

PAGE

HARDWARE

BUSES

Bus Bars
Bussco Engineering 170, 177

CONNECTORS AND INTERCONNECTION SYSTEMS

Connectors
Elco 88

HEAT SINKS

PC Card Guide/Heat Sink
Unitrack/Calabro Plastics 171

MOUNTING HARDWARE

PC Card Guide/Heat Sink
Unitrack/Calabro Plastics 171

PANELS AND BACKPLANES

Logic Panels
Excel 80

Wirewrap IC Boards
Garry Manufacturing 174

Wirewrapping Equipment
OK Machine & Tool 170

PARTS

Gear Tooth Endless Belts
Fenner America 169

SHIELDING

Shielding Components
Instrument Specialties 182

SOCKETS

Sockets
Electronic Molding 180

Breadboarding Sockets
Continental Specialties 4

Solder-Tab Sockets
Cambridge Thermionic 175

DIP Socket/Receptacle
Textool Products 171

WIRE AND CABLE

Wire and Cable
Belden/Electronic 172
Blake Wire & Cable 186

Flat Ribbon Cable Assemblies
AMP 78

COMPONENTS AND ASSEMBLIES

MAGNETIC COMPONENTS

Disc Memory Head Assembly
National Micronetics/Pacific 181

MOTORS; ROTATIVE COMPONENTS

Miniature DC Motors
North American Philips Controls 158

Miniature DC Servomotor
Portescap U.S. 147

DC Servomotor
Torque Systems 162

PHOTODEVICE ASSEMBLIES

Optical Coupler
Monsanto Commercial Products/Electronics 172

Solid-State Image Sensors
Reticon 168

PAGE

Mark-Sensor Arrays
Ultra Sensors 173

POWER SOURCES, REGULATORS, AND PROTECTORS

Power Supplies
Computer Products 170
Technipower/Benrus 22

Switching Power Supplies
Control Data/Magnetic Components 182
LH Research 172
Trio Laboratories 179

Flexible Disc Power Supplies
Power-One 12

RELAYS

Solid-State Relays
International Rectifier/Crydom 165, 170
Teledyne Relays 63

PC Board Solid-State Relays
ElecTrol 168

SEMICONDUCTOR DEVICES

Silicon Rectifiers
Electronic Devices 158

SWITCHES

Thumbwheel Switch
EECO ....Cover II

Rocker Switches
Cutler-Hammer/Specialty Products 86

DIP Rocker Switches
Grayhill 171

Miniature Toggle Switch
Alco Electronic Products 174

Subminiature Slide Switch
C&K Components 171

Pushbutton Switches
RTC 180

Lighted Pushbutton Switches
Switchcraft 164

LED Pushbutton Switches
Micro Switch/Honeywell 176

THERMAL COMPONENTS

Thermostats
Elmwood Sensors 179

CIRCUITS

CIRCUIT CARDS AND MODULES

Add-On Core Memory Boards
Ampex/Memory Products 175

Semiconductor Memory Boards
Intel Memory Systems 31

Microcomputer Modules
Motorola Semiconductor Products 13

Microcomputer Programmable CPU Module
Electronic Products/Warner & Swasey ..154

Single Board Microcomputer
Quay 154

Microprocessor Learning System Modules
Texas Instruments 150

D-A Converter System
ADAC 177

Digital-Synchro Converter Module
Singer/Kearfott 108

PAGE

F-V Converter Module
Dynamic Measurements 167

DIGITAL AND INTERFACE INTEGRATED CIRCUITS

CMOS Circuits
Fairchild Camera and Instrument/Digital Products 136

Custom MSI Circuits
Mosfet*Micro*Labs 140

64-Bit LSI Multiplier
TRW/Electronic Systems 138

Mil-Range FPLAs
Signetics 138

Static RAM
EMM Semi/Electronic Memories & Magnetics 19

Bipolar RAMs
National Semiconductor 140

1K ECL RAM
Motorola Semiconductor Products 139

16K RAM
Mostek 64

p/ROMs
Harris Semiconductor 150

Computer-On-A-Chip
Fairchild Camera and Instrument/Systems Technology 146

Microprocessors
Data General 101
Signetics 150

Microprocessor Slice Family
Motorola Semiconductor Products 158

Microprocessor Peripheral ICs
Intel 68
NEC Microcomputers 90

Bipolar Microprogram Controller
Monolithic Memories 145

Bipolar LSI Interrupt Controller
Motorola Semiconductor Products 136

CMOS DVM IC
Siliconix 136

LINEAR INTEGRATED CIRCUITS

Interface ICs
Fairchild Camera and Instrument/Linear Integrated Circuits 138

Operational Amplifiers
Hybrid Systems 169

Synchro-to-Resolver Converter
Magnetico 172

Analog MUX
Burr-Brown 138

OTHER CIRCUITS

Probe Card Assembly System
Alignment Enterprises 179

MEMORY/STORAGE EQUIPMENT

FLEXIBLE DISC UNITS

Flexible Disc Drives
Ex-Cell-O/Remex 137
Facit 123
Wangco 128

Flexible Disc Systems
iCOM 71
PerSci 125
Shugart Associates 15
Tri-Data 169

Flexible Disc Send/Receive Terminal
Randal Data Systems 173

PAGE

MAGNETIC CORE MEMORIES

Add-On Core Memory
Ampex/Memory Products 175

MAGNETIC DISC AND DRUM UNITS
(See also Flexible Disc Units)

Disc Drives
Diablo Systems ....Cover IV
Pertec/Peripheral Equipment 82

Storage Module Disc Drives
Microdata 167

Disc Systems
Plessey Microsystems 72

Disc Subsystem
Xylogic OEM Components Group 182

Disc Drive Formatter/Controller
Ball Computer Products 126

Microprocessor-Based Disc Controller
Xebec Systems 156

MAGNETIC TAPE UNITS

Tape Drives
AMCOMP 151
Mohawk Data Sciences 7

Cartridge Tape Drives
Microdata 166

Endless Loop Cartridge Tape Transport
Amilon 174

Cartridge Tape System
Applied Data Communications 164

Magnetic Tape System
Computer Operations 172

Tape Recorders
Kennedy 1

Cassette Recorder
Raymond Engineering 102

Intelligent Cassette Recorder
William Palmer Industries 168

Magnetic Tape Formatter
Dylon 170

Mag Tape Intelligent Cable
Computer Automation 168

Digital Cassettes
CFI Memories 173
3M/Data Recording Products 164

ROM/RAM PROGRAMMERS AND SIMULATORS

p/ROM Programmers
iCOM 71
Pro-Log 167

EP/ROM Programmer
Associated Electronics 176

EROM Storage Autoprogrammer
Wavetek 178

SEMICONDUCTOR MEMORIES

Static RAM
EMM Semi/Electronic Memories & Magnetics 19

Bipolar RAMs
National Semiconductor 140

16K RAM
Mostek 64

1K ECL RAM
Motorola Semiconductor Products 139

p/ROMs
Harris Semiconductor 150

Semiconductor Memory Systems
Intel Memory Systems.... 31
Electronic Memories & Magnetics/ Systems Equipment 175

INPUT/OUTPUT AND RELATED EQUIPMENT

BADGE READERS

Data Collection Terminal
Coastal Data Services 180

PAGE

CHARACTER RECOGNITION EQUIPMENT

OCR Wand
Recognition Equipment 166

DATA ENTRY EQUIPMENT

Dual Output Light Pen
HEI 173

DATA TERMINALS
(See also Graphic Equipment)

Data Terminals
Teletype 23
Texas Instruments/Digital Systems 92

Flexible Disc Send/Receive Terminal
Randal Data Systems 173

CRT Display Terminals
Datamedia 119
Research 48

Intelligent CRT Display Terminal
Hewlett-Packard 51-58

Intelligent CRT Color Display Terminal
Intelligent Systems 46

Plasma Display Terminals
Interstate Electronics 42

CRT Display System
Documation 132

DISPLAY EQUIPMENT
(See also Data Terminals and Graphic Equipment)

Gas Discharge Panel Displays
Burroughs/Electronic Components 167

GRAPHIC EQUIPMENT

Graphic Display
Sigma Electronic Systems 173

Graphic Display Terminal
Sanders Data Systems 45

Color Graphic Display Systems
Ramtek 77

Sonic Digitizer
Science Accessories 156

Data Tablet/Graphic Calculator Interfaces
Summagraphics 174

INTERFACE EQUIPMENT; CONTROLLERS

8-Word Plug-In Interface
Forte Technology 169

Universal Controller
Austron 174

Computer/Peripheral Interface
Computrol 169

Microprocessor-Based Memory Controller
Xebec Systems 156

Mag Tape Intelligent Cable
Computer Automation 168

Magnetic Tape Formatter
Dylon 170

Disc Drive Formatter/Controller
Ball Computer Products 126

Disc and Tape Drive Controllers
Western Peripherals 12

Data Tablet/Graphic Calculator Interfaces
Summagraphics 174

KEYBOARD EQUIPMENT

Keyboards
Cortron/Illinois Tool Works 149

Remote Data Entry Keystation
Pertec Computer/CMC 173

Numeric Data Entry Terminals
Hewlett-Packard 162

PLOTTING EQUIPMENT

Digital Plotters
Houston Instrument/Bausch & Lomb 129

PRINTER/PLOTTERS

Electrostatic Printer/Plotter
Gould/Instrument Systems 84

PAGE

PRINTING EQUIPMENT

Printers
Facit 123

Intelligent Printers
Perkin-Elmer Data Systems/Terminal 181

Line Printers
Control Data 153
Datapoint 174
Tally 2
Wang Laboratories 164

Impact Line Printer
Data Test 164

900-Line/Min Printer
Decision Data Computer 166

Thermal Printer
NCR/Terminal Systems 130

Digital Printers
C. Itoh Electronics/Systems and Components 175
Victor Comptometer/ Systems Components 157

PUNCHED TAPE EQUIPMENT

Paper Tape Equipment
Facit 123

Paper Tape Reader
Decitek/Jamesbury 21

Paper Tape Reader/Punches
Epson America 178
Data Specialties 166
Sweda International/OEM Products 181

COMPUTERS AND COMPUTER SYSTEMS

AUTOMATIC TEST SYSTEMS

Automatic IC Test System
Teradyne 155

Automatic Logic Board Testers
Computer Automation 60
GenRad 49
Mirco/Systems 182

COMPUTER AUXILIARY UNITS

Floating Point Array for H-P 2100
CSP 173

Portable Program Loader
Computer Operations 22

CONTROL PROCESSORS

Industrial Application Minicomputer
Philips Data Systems 178

MICROCOMPUTERS AND MICROPROCESSORS

Microcomputers
IMS Associates 168
Data General 101
Digital Equipment 8
Plessey Microsystems 163

Microcomputer Modules
Motorola Semiconductor Products 13

Microcomputer Programmable CPU Module
Electronic Products/Warner & Swasey ..154

Single Board Microcomputer
Quay 154

Portable Microcomputer
Digital Electronics 148

Microcomputer System
Wavemate Computers and Systems 152

In-Circuit Microcomputer Emulator
California Micro Computer 156

Microcomputer Resident Compiler
Unified Technologies 148

Single Board Multiprocessor
Intel/Microcomputer 144

Computer-On-A-Chip
Fairchild Camera and Instrument/ Systems Technology 146

GUIDE TO PRODUCT INFORMATION

PAGE

Bipolar Microprocessor
Signetics 150
Microprocessor Slice Family
Motorola Semiconductor Products 158
Microprocessor Peripheral ICs
Intel **68**
NEC Microcomputers **90**
Bipolar LSI Interrupt Controller
Motorola Semiconductor Products 136
Bipolar Microprogram Controller
Monolithic Memories **145**
Intelligent Process Programmer
Research 180
Microprocessor Development System
Millenium Information Systems **28**
Microprocessor Learning System Modules
Texas Instruments 150
Microprocessor Analyzer
A O Systems 148
Multilevel Microprocessor Language
Forth 158, **187**

MINICOMPUTERS; SMALL- AND MEDIUM-SCALE COMPUTERS

Computers
Data General **11**
Minicomputers
Computer Automation **33-40**
Data General **101**
Digital Computer Controls **5**
Harris Computer Systems **133**
Systems Engineering Laboratories **16**
Varian Data Machines 160
Industrial Application Minicomputer
Philips Data Systems 178
Scientific Computer
Data General 177
Minicomputer System
Hewlett-Packard **51-58**

MULTIPROCESSORS

Single Board Multiprocessor
Intel/Microcomputer 144

DATA COMMUNICATIONS EQUIPMENT

COMMUNICATIONS COUPLERS

Acoustic Coupler
ComData 173
300-Bit/s Acoustic Coupler
Multi-Tech Systems 178

COMMUNICATIONS MULTIPLEXERS

Synchronous Multiplexer
Infotron Systems 170

DATA COMMUNICATIONS TEST EQUIPMENT

Bit Error Rate Tester
EMR-Telemetry 175
Hand-Held Data Communications Monitor
Goodwood Data Systems 182

DATA TRANSMISSION EQUIPMENT

Synchronous Line Driver
Prentice Electronics 181

MODEMS; DATA SETS

Intelligent Modem
Omnitec 174
Microprocessor-Based Modems
International Communications 162

DATA ACQUISITION AND CONTROL EQUIPMENT

A-D AND D-A CONVERTERS

D-A Converter System
ADAC 177

ANALOG MULTIPLEXERS

16-Channel Analog Multiplexer
Teledyne Philbrick 179

ANGLE AND POSITION ENCODERS

Position Encoders
BEI Electronics **176**

PAGE

DATA ACQUISITION SYSTEMS

Data Acquisition Systems
Neff Instrument **26**

DATA TRANSFER AND INTERFACE EQUIPMENT

Process Computer I/O Interface
Computer Products ....**Cover III**

MONITORING AND CONTROL EQUIPMENT

Industrial Application Minicomputer
Philips Data Systems 178
Data Acquisition Controller
Tychon 177
Automatic Positioning System Controller
Anorad 173
Incremental-Digital Positioning Control
Control Systems Research 176
Intelligent Process Programmer
Research 180

SCANNERS

Digital Scanner System
QEI 176

SYNCHRO-DIGITAL AND DIGITAL-SYNCHRO CONVERTERS

Digital-Synchro Converter
Singer/Kearfott **108**

TEST AND MEASUREMENT EQUIPMENT; INSTRUMENTATION

DIGITAL EQUIPMENT TESTERS; INSTRUMENTATION

IC Test System
Teradyne **155**
Automatic Logic Tester
GenRad **49**
Logic Board Tester
Computer Automation **60**
Logic Board Test System
Mirco/Systems 182
Logic Analyzers
Biomation **24**
Logic State Analyzer
Hewlett-Packard **81**
Microprocessor Analyzer
A O Systems 148
In-Circuit Microcomputer Emulator
California Micro Computer 156

OSCILLOSCOPES

Digital Delay Oscilloscopes
Philips Test & Measuring Instruments **131**
Digital Timing Oscilloscope
Tektronix **67**

OTHER TEST AND MEASUREMENT EQUIPMENT

Probe Card Assembly System
Alignment Enterprises 179
40-Pin IC Test Clips
Continental Specialties 168

SIGNAL AND CODE CONVERTERS

F-V Converter Module
Dynamic Measurements 167

OTHER PRODUCTS; SERVICES

EDUCATION

Seminars
Integrated Computer Systems **159**

EMPLOYMENT OPPORTUNITIES

Employment Opportunity
NCR/Terminal Systems **187**

MARKET REPORTS

Microprocessor/Microcomputer Market Survey
Computer Design/Market Research **171**

SOFTWARE

Multilevel Microprocessor Language
Forth 158, **187**
Microcomputer Resident Compiler
Unified Technologies 148

ADVERTISERS' INDEX

Alco Electronic Products, Inc. 174
AMCOMP, Inc. 151
AMP, Inc. 78, 79
Applied Data Communications 164
Associated Electronics 176
Austron 174

Ball Computer Products, Inc. 126, 127
BEI Electronics, Inc.,
Controls and Instrumentation Div. 176
Belden Corp. 172
Biomation Corp. 24, 25
Blake Wire and Cable Corp. 186
Bussco Engineering 177

Computer Automation, Inc. 33-40, 60, 61
Computer Design Publishing Corp. .... i, ii*, 171
Computer Operations, Inc. 22
Computer Products, Inc. .... Cover III
Continental Specialties Corp. 4
Control Data Corp. 153
Cortron,
a division of Illinois Tool Works, Inc. 149
Cutler Hammer,
Specialty Products Div. 86

Data General Corp. 11, 101
Datamedia Corp. 119
Decitek,
div. of Jamesbury Corp. 21
Diablo Systems, Inc. .... Cover IV
Digital Computer Controls, Inc. 5
Digital Equipment Corp. 8, 9
Documation, Inc. 132

EECO .... Cover II
Elco Corp. 88
Electronic Devices 158
EMM SEMI,
a subsidiary of Electronic Memories & Magnetics Corp. 19
Electronic Molding Corp. 180
Elmwood Sensors, Inc. 179
Epson America, Inc. 178
Excel Corp. 80
Ex-Cell-O Corp.,
Remex Div. 137

Facit 123
Fenner America 169
Forth, Inc. 187

GenRad, Inc. 49
Gould, Inc. 84
Grayhill, Inc. 171

Harris Corp.,
Computer Systems Div. 133
Semiconductor Div. 150, 151
Hewlett Packard Corp. 51-58, 81
Houston Instrument,
Div. of Bausch & Lomb, Inc. 129
E. F. Hutton & Co., Inc. 175

iCom, Inc. 71
IMS Associates, Inc. 168
Instrument Specialties Co., Inc. 182
Integrated Computer Systems, Inc. 159
Intelligent Systems Corp. 46, 47
Intel Corp. 68, 69
Intel Memory Systems 31

International Rectifier Corp.,
Crydom Controls Div. 165
Interstate Electronics Corp. 42, 43

Kennedy Co. 1

Magnetic Components Group,
Control Data Corp. 182
Microdata Corp. 166, 167
Millenium Information Systems 28, 29
Mohawk Data Sciences Corp. 7
Monolithic Memories, Inc. 145
Mostek 64, 65
Motorola Semiconductor Products, Inc. 13, 139

NCR,
Terminal Systems Div. 130, 187
NEC Microcomputers, Inc. 90, 91
Neff Instruments Corp. 26
North American Philips Controls Corp. 158

OK Machine & Tool Corp. 170

PerSci, Inc. 125
Pertec Corp.,
Peripheral Equipment Div. 82, 83
Philips Test & Measuring Instruments 131
Plessey Microsystems 72, 73
Portescap U.S. 147
Power-One, Inc. 12

Ramtek Corp. 75, 76,**77
Raymond Engineering Co. 102
Research, Inc. 48

Sanders Associates,
Federal Systems Group, Military Data Systems Div. 45
Science Accessories Corp. 156
Shugart Associates 15
Singer Co.,
Kearfott Div. 108
Sweda International,
OEM Products Div. 181
Systems Engineering Labs 16, 17

Tally Corp. 2
Technipower,
Division of Benrus Corp. 22
Tektronix, Inc. 67
Teledyne Relays 63
Teletype Corp. 23
Teradyne, Inc. 155
TEXAS INSTRUMENTS INCORPORATED,
Digital Systems Div. 92
Tri-Data Corp. 169

United Technologies,
Norden Div. 85, 87, 89

Victor Comptometer 157

Wang Laboratories, Inc. 164
Wangco, Inc. 128
Western Peripherals, Inc. 12

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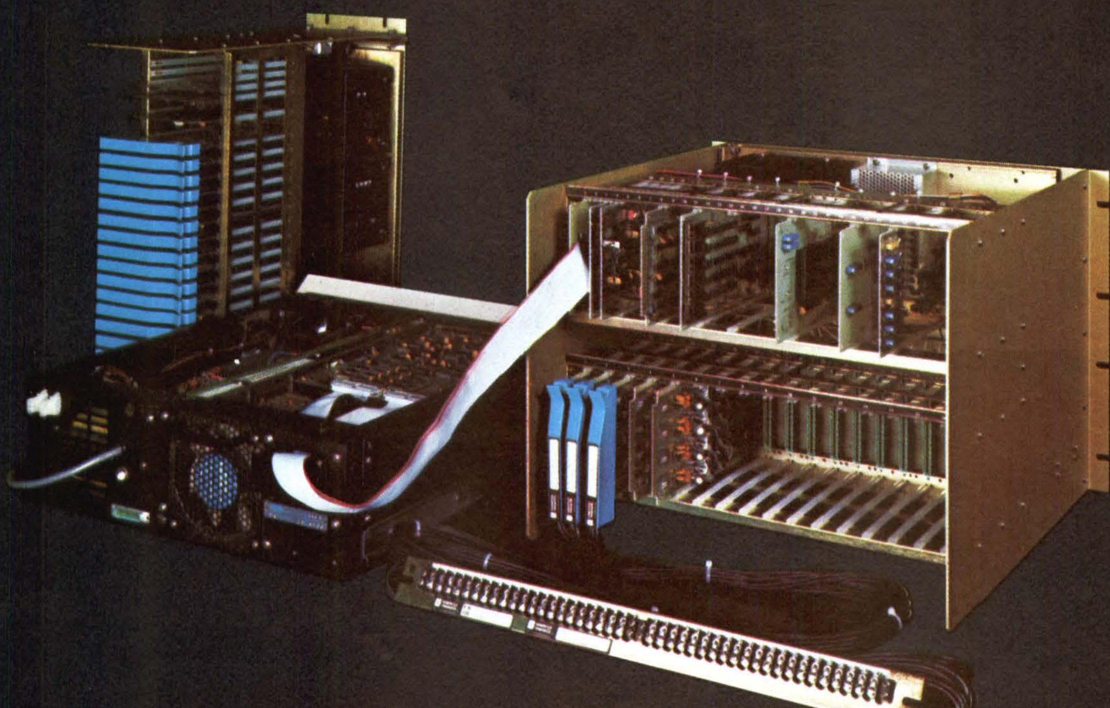

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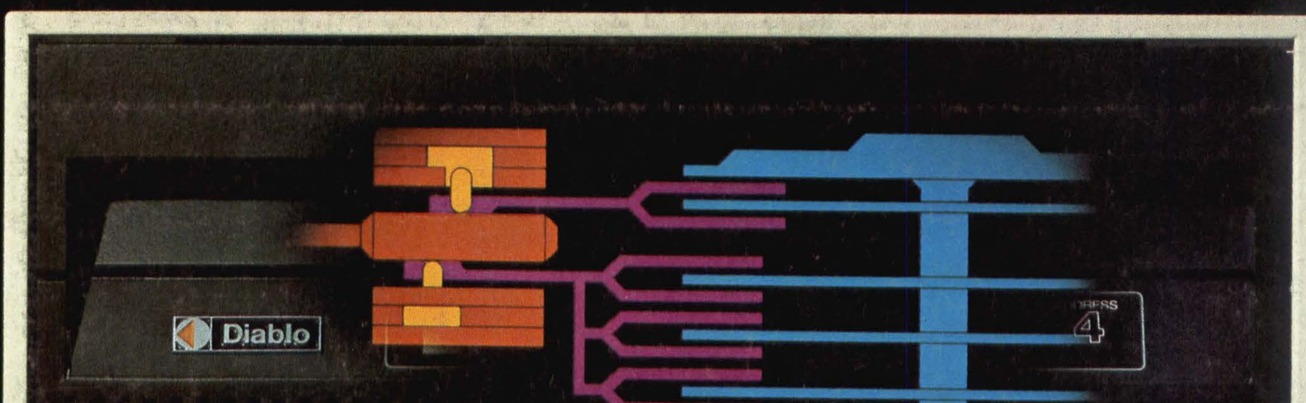

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