COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

NOVEMBER 1977

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THE MAGAZINE OF DIGITAL ELECTRONICS

COMPUTER DESIGN

NOVEMBER 1977 • VOLUME 16 • NUMBER 11

FEATURES

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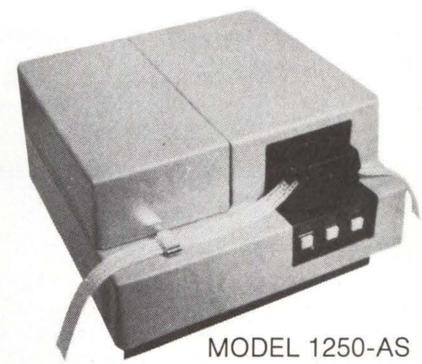

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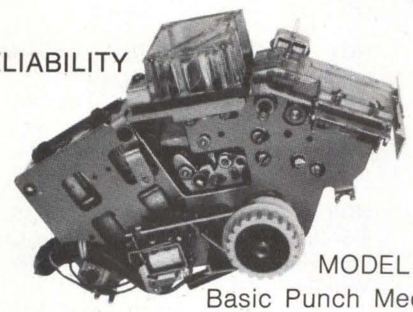

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CALENDAR

CONFERENCES

NOV 14-16—Distributed Data Processing Conf, Ramada O'Hare Inn, Chicago, Ill. INFORMATION: American Institute of Industrial Engineers (AIIE), Dept PR, PO Box 3727, Santa Monica, CA 90403. Tel: (213) 450-0500

NOV 15-17—6th Annual Meeting of Members of Computer-Aided Manufacturing—Internat'l (CAM-I), Americana Inn, Arlington, Tex. INFORMATION: C. H. Link, Exec Secretary and Gen'l Mgr, CAM-I, 611 Ryan Plaza Dr, Suite 1107, Arlington, TX 76011. Tel: (817) 265-5328

NOV 17 and JAN 19—Invitational Computer Conf, Houston Oaks, Houston, Tex; South Coast Plaza Hotel, Orange County, Calif. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: (714) 644-6037

NOV 28—NBS and IEEE Personal Computing Conf, Nat'l Bureau of Stds, Gaithersburg, Md. INFORMATION: Paul Meissner, A219 Technology Bldg, Nat'l Bureau of Stds, Washington, DC 20234. Tel: (301) 921-3427

DEC 5-7—IEEE Internat'l Electron Devices Meeting, Washington Hilton Hotel, Washington, DC. INFORMATION: Susan Hinman, Courtesy Assoc, 1629 K St, NW, Washington, DC 20006. Tel: (202) 296-8100

DEC 5-7—Nat'l Telecommunications Conf (NTC), Marriott Hotel, Los Angeles, Calif. INFORMATION: NTC '77, PO Box 1250, Pasadena, CA 91109. Tel: (213) 354-2759

DEC 5-7—Winter Simulation Conf, Nat'l Bureau of Stds, Gaithersburg, Md. INFORMATION: Paul F. Roth, B250 Technology Bldg, Nat'l Bureau of Stds, Washington, DC 20234. Tel: (301) 921-3545

DEC 6-8—Mini/Micro Computer Conf, Anaheim Conv Ctr, Anaheim, Calif. INFORMATION: Robert D. Rankin, 5544 E LaPalma Ave, Anaheim, CA 92807. Tel: (714) 528-2400

DEC 15—Computer Networks Sym, Gaithersburg, Md. INFORMATION: Computer Networks, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

JAN 19-21—U.S./Southeast Asia Telecommunications Conf, Singapore. INFORMATION: John Sodolski, Electronic Industries Assoc, Communications Div, Washington, DC 20006. Tel: (202) 457-4934

JAN 24-26—Reliability and Maintainability, Biltmore, Los Angeles, Calif. INFORMATION: D. F. Barber, PO Box 1401, Branch PO, Griffiss AFB, NY 13441

FEB 7-10—World Fair for Tech Exchange, Georgia World Congress Ctr, Atlanta, Ga. INFORMATION: Dr Dvorkovitz & Associates, PO Box 1748, Ormond Beach, FL 32074. Tel: (904) 677-7033

FEB 13-15—Aerospace and Electronic Systems Winter Conv (WINCON), Los Angeles, Calif. INFORMATION: Max Weiss, Aerospace Corp, PO Box 92957, Los Angeles, CA 90009. Tel: (213) 648-5000

FEB 15-17—IEEE Internat'l Solid-State Circuits Conf (ISSCC), San Francisco Hilton, San Francisco, Calif. INFORMATION: Lewis Winner, 152 W 42nd St, New York, NY 10036. Tel: (212) 279-3125

FEB 21-23—Datacom '78, Sheraton Park Hotel, Washington, DC. INFORMATION: Ed Bride, The Conference Co, 60 Austin St, Newtonville, MA 02160. Tel: (617) 964-4550

FEB 28-MAR 2—COMPCON Spring '78, San Francisco, Calif. INFORMATION: COMPCON Spring '78, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

MAR 1-3—Control of Power Systems Conf and Exposition, Lincoln Plaza Hotel, Oklahoma City, Okla. INFORMATION: Dr M. E. Council, OG & E Prof, School of Electrical Engineering and Computing Sciences, U of Oklahoma, Norman, OK 73019. Tel: (405) 325-4721

MAR 5-8—TAPPI Internat'l Pulp and Paper Industry Exhibit, Conrad Hilton Hotel, Chicago, Ill. INFORMATION: Wayne Gross, c/o TAPPI, 1 Dunwoody Pk, Atlanta, GA 30341. Tel: (404) 394-6130

MAR 14-17—Printemps Informatique, U.S. Trade Ctr, Paris, France. INFORMATION: Helen Burroughs, U.S. Dept of Commerce, Office of Internat'l Mktg, France/Benelux, Rm 6318, Washington, DC 20230. Tel: (202) 377-4941

MAR 20-22—Industrial Electronics Control Instrumentation (IECI) Conf, Sheraton Hotel, Philadelphia, Pa. INFORMATION: Dr S. J. Vahaviolos, Engineering Research Ctr, Western Electric, PO Box 900, Princeton, NJ 08540

MAR 22-24—Internat'l Topical Conf on the Physics of SiO_2 and Its Interfaces, IBM Thomas J. Watson Research Ctr, Yorktown Heights, NY. INFORMATION: Dr Sokrates T. Pantelides, Conf Chm, IBM Thomas J. Watson Research Ctr, PO Box 218, Yorktown Heights, NY 10598. Tel: (914) 945-3000, (914) 945-1207

MAY 9-12—Internat'l Magnetics (INTERMAG) Conf, Palazzo Dei Congressi, Florence, Italy. INFORMATION: E. Della Torre, Dept of Electrical Engineering, McMaster U, Hamilton, Ontario L8S4L7, Canada

SEMINARS

NOV 21-22 and DEC 12-13—Data Communications: Advanced Concepts and Systems; DEC 7-9—Data Communications: An Introduction to Concepts and Systems; DEC 12-13—Minicomputers and Microcomputers: Selection and Usage Guidelines, San Francisco, Calif; New York, NY; and Washington, DC. INFORMATION: Peggy Quinn, Datapro Research Corp, 1805 Underwood Blvd, Delran, NJ 08075. Tel: (609) 764-0100, (800) 257-9406

JAN 30-FEB 1—Automated Testing For Electronics Manufacturing, Los Angeles Marriott, Los Angeles, Calif. INFORMATION: Sheila Goggin, ATE Seminar/Exhibit Coordinator, 167 Corey Rd, Brookline, MA 02146. Tel: (617) 232-2668

FEB 2-3—4th Joint College Curricula Workshop in Computer Science & Engineering, Orlando, Fla. INFORMATION: Dr David Rine, Info Science Program, Western Ill U, Macomb, IL 61455

SHORT COURSES

NOV 21-23, NOV 28-DEC 2, and DEC 14-16—Data Comm Systems and Networks; Structured Programming; and Minicomputers, Microcomputers, and Microprocessors for Non-Electrical Engineers, George Washington U, Washington, DC. INFORMATION: Martha Augustin, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

NOV 28-DEC 1 and DEC 12-15—Microprocessor Training Courses, San Jose, Calif. INFORMATION: John Hatch, Fairchild Camera and Instrument Corp, Instrumentation and Systems Group, 1725 Technology Dr, San Jose, CA 95110. Tel: (415) 962-3617

NOV 28-DEC 2, DEC 6-8, DEC 12-16, JAN 3-5—Hands-On Microprocessor Short Courses with Free Take-Home Microcomputer, and Workshop, Boston, Mass; Detroit, Mich; Chicago, Ill; and Mayaguez, Puerto Rico. INFORMATION: Jerilyn Williams, Wintek Corp, 902 N 9th St, Lafayette, IN 47904. Tel: (317) 742-6802

DEC 5-9—Design and Prediction of Sonar Systems, The Royal Inn of Point Loma, 4875 N Harbor Dr, San Diego, Calif. INFORMATION: Continuing Engineering Education Program, George Washington U, Washington, DC 20052. Tel: (202) 676-6106, or (800) 424-9773

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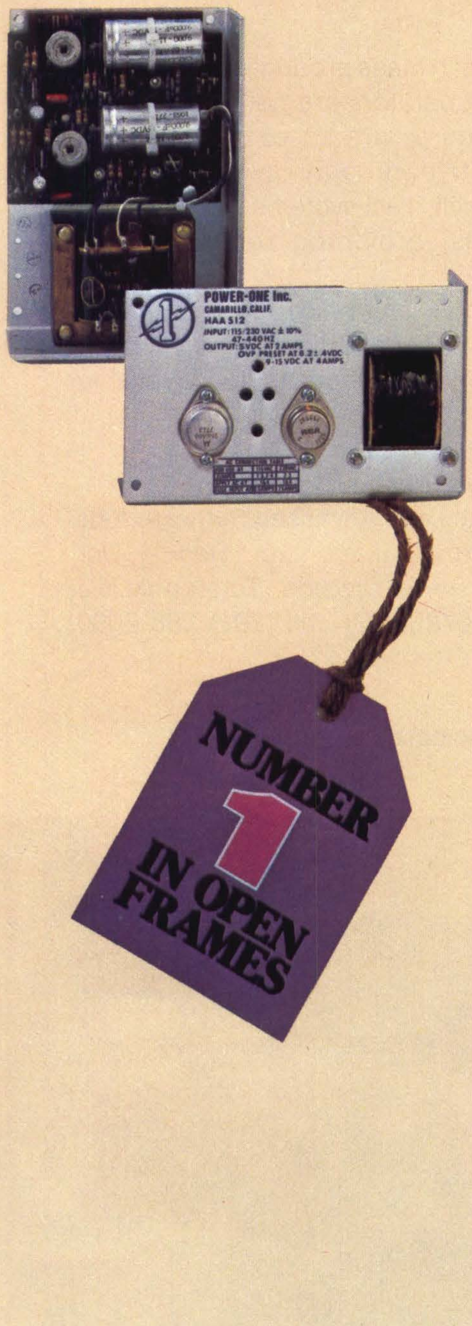

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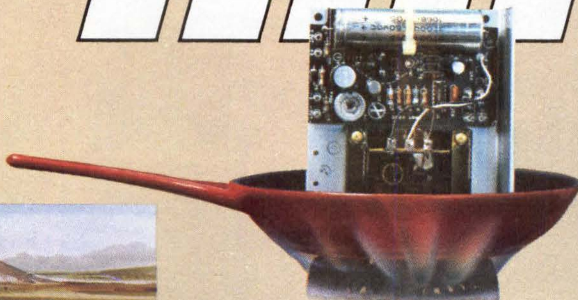

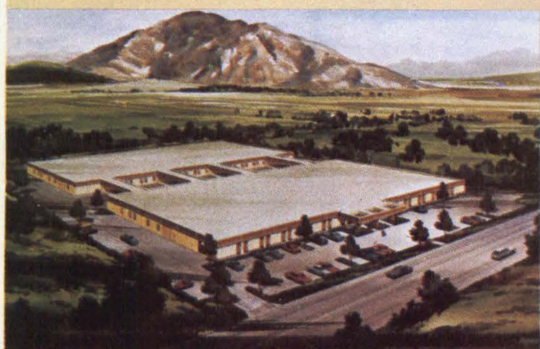

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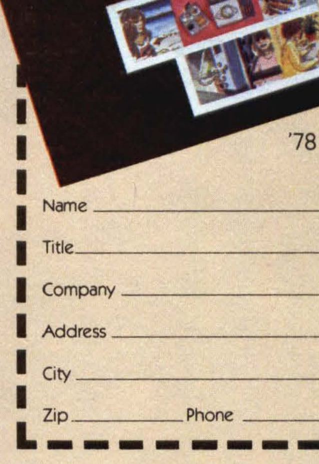

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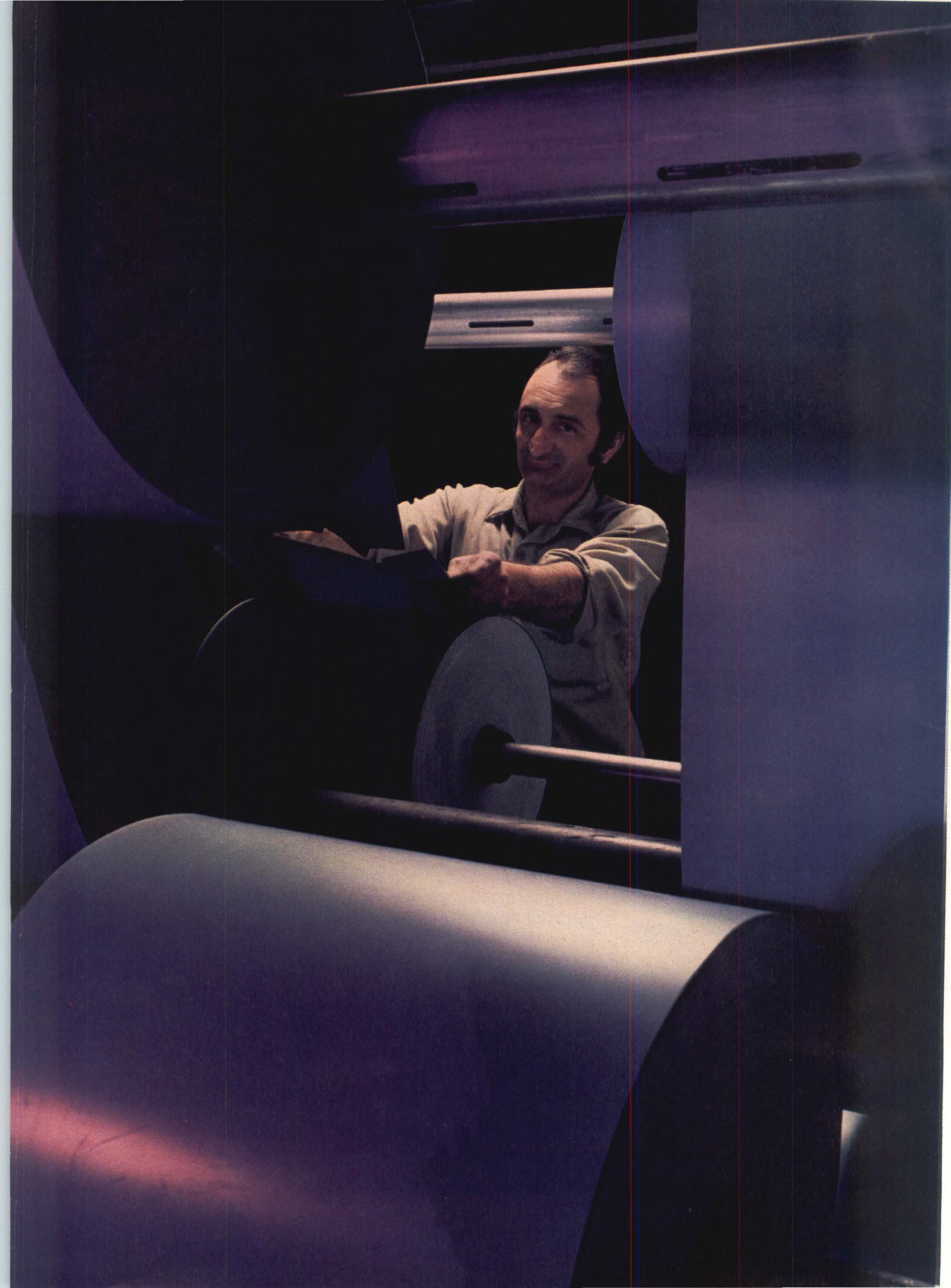


The LSI-11 microcomputer is really getting the plastics business rolling.

There's a new computerized extrusion process control system for plastic sheet and film that improves material uniformity by up to 75%. It also decreases usage of expensive resins by up to 10%, while automatically maintaining close produce tolerances. Yet it's one of the most effective extruder control systems you can buy.

It's called the Measurex 2000/25.

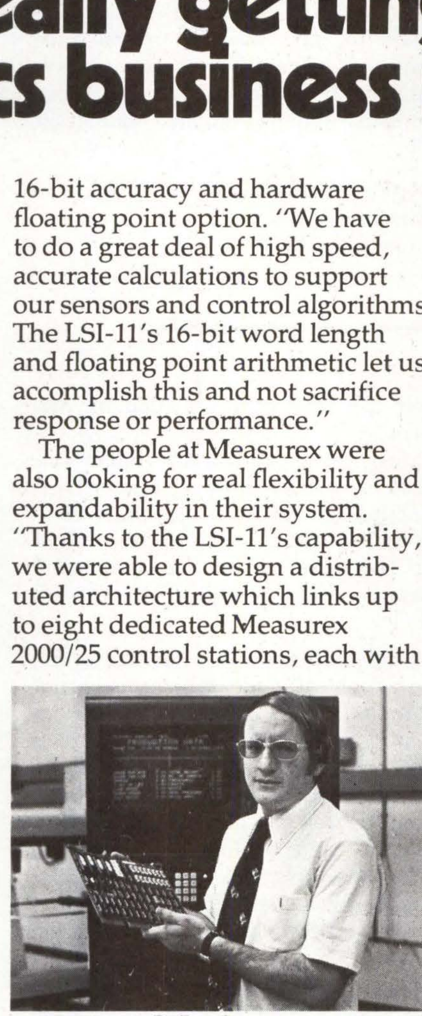
And it's run by an LSI-11—the highest performance, most software-supported microcomputer you can buy.

For Measurex Project Manager Dave Stepner, anything less than the LSI-11 simply wouldn't have been enough.

"We were looking to develop the most cost effective, full state-of-the-art system on the market," says Dave. "With the LSI-11, we got the computer power and 16-bit accuracy we needed, plus packaging flexibility."

What Dave Stepner liked most about the LSI-11 compared to other microcomputers, was its full 16-bit accuracy and hardware floating point option. "We have to do a great deal of high speed, accurate calculations to support our sensors and control algorithms. The LSI-11's 16-bit word length and floating point arithmetic let us accomplish this and not sacrifice response or performance."

The people at Measurex were also looking for real flexibility and expandability in their system. "Thanks to the LSI-11's capability, we were able to design a distributed architecture which links up to eight dedicated Measurex 2000/25 control stations, each with its own LSI-11, to a central intelligent data terminal for management reporting. And because of the LSI-11's low cost and single-board packaging, we can provide customers with a spare computer on site."



Dr. Dave Stepner,
2000/25 Project Manager, Measurex Corp., Cupertino, CA.

Dave Stepner concludes: "The LSI-11 really has everything going for it. The instruction set allows for very efficient coding—the technology has been tested and proven—and, of course, Digital has a mass production and delivery capability well matched to our needs."

Why not do like Measurex's Dave Stepner and get in touch.

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LETTERS TO THE EDITOR

To the Editor:

On page 120 of the July 1977 issue of *Computer Design* (Microprocessor/Computer Data Stack), the article on the Relational Memory Systems microprocessor development system . . . refers to the machine as "the only available alternative to the Zilog ICE on the market." This is definitely not so.

The Tektronix 8002 μProcessor Lab offers full support for the Z-80 including in-circuit emulation, (as well as for) . . . the 8080, the 6800, and the 16-bit TMS 9900. This disc-operating-system-based unit offers full development capability including program input and editing, program assembly, in-circuit emulation, both software and hardware debugging capability, and built-in p/ROM programming capability. A second system, the 8001, is offered for those interested in in-circuit emulation only.

Joseph G. McCarthy
Tektronix, Inc
Beaverton, Ore

To the Editor:

The article ("Solving Mass-Produced ROM Programming Problems With Base Registers," pp 99-105) by John A. Carroll in the August issue of *Computer Design* was very interesting. It suggested that the addition of base registers to a microcomputer's instruction set architecture would permit the use of mass produced ROMs for many commonly used software modules. The article made a number of valid points which I have not seen previously discussed in the literature, most significant being that the motivation for his architecture suggestions was the desire to encourage the use of low cost, mass produced ROM modules.

In our business, which includes the design and manufacture of digital microcomputers for the aerospace market based on bit slice microprocessors, the use of ROM memory can be very beneficial. Not only is it low cost (if mass produced in volume), but it is very reliable, low power, very modular (unlike core), and highly resistant to corruption by radiation.

Consequently, we have given considerable thought to the characteristics of computer architecture which facilitate the use of ROM and which make ROM modules reusable for several applications. This interaction is largely ignored in the literature and therefore in the design of microcomputer architectures, so we welcome the treatment provided by Mr. Carroll.

Since we have come to similar conclusions in designing a standard instruction set for our aerospace computer products, your readers might find the following comments a useful extension and clarification of his article.

(1) His attempt to facilitate the generation of code which need not be modified when it is moved, or relocated, in memory is referred to as the generation of "position independent code" in the more formal computer science literature. It is possible to find technical articles on techniques for generation of position independent code whose motivation is invariably the implementation of dynamic relocation in read/write memory (eg, for a timesharing system) rather than the implementation of position-independent ROM modules. The fact that these two problems are equivalent is important to realize.

(2) A powerful technique for the generation of position independent code was not mentioned in the article. This involves the use of the program counter (PC) as an address modifier or base register. If all jump addresses within the ROM module are computed relative to the PC (ie, using the PC as a base register), they become inherently position-independent without requiring the dedication of a hardware base register. In our SKC family of computers, all short jump instructions are executed relative to the PC in part for this reason.

(3) Another way to employ the PC as a base register is via the implementation of instructions with an Immediate Operand capability. That is, the operand for the instruction immediately follows the instruction in (ROM) memory. As a result, it is usually not necessary to set up a region of (ROM) memory for local constant data. The use of a local constant region would have implied the use of another hardware base register. In our new SKC3121 computer, all memory reference instructions have an immediate operand option for this reason.

(4) The link table mentioned in Mr. Carroll's article is a very useful ingredient in designing a modular program in ROM. However, for maximum utility, the jump instruction set must be tailored to facilitate the use of the link table. For example, an indirect subroutine jump instruction was implemented in our standard aerospace instruction set specifically to facilitate the use of a link table for intermodule communication. Without this facility, inefficiency would be introduced in transfers between modules via the link table.

In short, the use of base registers for operand address modification was only the first step in the synthesis of an instruction set architecture which was well suited to the widespread use of ROM for aerospace applications. We hope the issue receives continued treatment in the literature. Perhaps Mr. Carroll's article will serve as a catalyst toward that end.

Austin J. Maher
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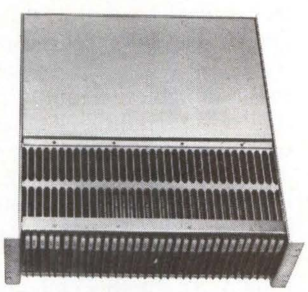

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by **John E. Buckley**
Telecommunications Management Corp
Cornwells Heights, Pa.

Office Automation

The field of office automation is rapidly evolving toward the merger of data processing and telephone communications systems. Identified by such nomenclature as office of the future, computerized office, paperless office, and word processing, the basic concept addresses the ability to collect fragmented source data within an office environment and to build centralized data files for demand retrieval or subsequent data processing. While the data processing capability has been viable for several years, the constraint has been data communications capabilities and, particularly, economies.

Ironically, most larger offices have had both data processing and telecommunications resources for some time. These two areas, however, have functioned in isolated and limited environments. Until recently, the telephone system as a means of passive communications could at best function as the network access vehicle between data origination locations (ie, individual telephone extensions) and a centralized data processing system. Introduction of computerized telephone systems (CBXS) changed the telephone system's role to that of an active data control device.

Examination of this emerging area of office automation makes it possible to speculate on the probable applications and requirements that can be expected to become commonplace over the next few years. The concept of management information systems (MIS) has been constantly defined and redefined to offer a timely definition that suits changing applications. However, an examination of the economics involved in primary data source collection has shown the limitations of these MIS applications. For example, a basic application of employee time reporting could ideally be accomplished by installing a data terminal at each employee's desk. Employee and project identification could then be entered each time activities on the project are begun and ended. The value of collecting such data is self-evident; timely and accurate project cost accounting, prompt client or customer billing, and employee efficiency and effectiveness tracking, among others, are obtained. The cost, however, of such a distributed data entry system has been impractical, resulting in the preservation of manually prepared time reports, which are manually collected, sent to a centralized data preparation location, converted to computer-compatible form, and then processed by computer.

Due to the tediousness of the steps to be performed, time reporting is at best a weekly event, producing data reports that lag the actual activities by two or more weeks. With a standard pushbutton telephone set, the CBX collects source data from the primary source as it occurs, requiring the employee to enter minimum data. The project number (entered by the employee) and extension number, date, and time (automatically controlled) are stored on a peripheral disc subsystem. Upon termination of a project, the CBX accesses the stored data, and prepares and stores a complete elapsed time record for later retrieval.

It should not be misinterpreted that the CBX is going to replace the traditional data processing center. Rather than compete with an existing data processing facility, the CBX will complement the data applications to be processed on existing computer equipment. At the present time the necessary basic components of the CBX exist and are operational for automatic incremental data collection and dissemination. The availability of new tools and techniques, together with the rethinking of basic premises of present office data flow techniques must be utilized in order to conceive a system that will meet future applications.

The CBX is not a telephone system controlled by a programmable computer; it is a computer system, similar to traditional message switching systems, that can switch digitized voice bytes to specified addresses. The conceptual development of office automation applications must be formulated with this in mind. Admittedly, the primary addressing function of a CBX is the number the call originator has entered to be called, which usually is another telephone extension on the CBX or an outside trunk to the public telephone network. While the actual data to be switched is analog voice, the digitization of that voice signal coupled with time division multiplex switching completes the parallel between this and the message switching systems.

CBX systems are capable of decoding multifrequency signals generated by a pushbutton telephone set. These same types of signals can also be generated and received by such interactive terminals as keyboard/CRT or keyboard/printer terminals. Outputs from a CBX that are presently intended for trunk circuits to the public telephone network can also be used to interface to disc subsystems, mini or microcomputer systems, and data processing centers. Based on the data content entered from a pushbutton telephone or interactive data terminal, the CBX can select the proper output of the subsequent data entries. The actual processing of the data content can be performed prior to its delivery, so that the CBX, in effect, is functioning as an input/output processor within a data application.

Primary value of the CBX in an office automation environment is not to duplicate existing functions, but rather to provide added dimensions of incremental data

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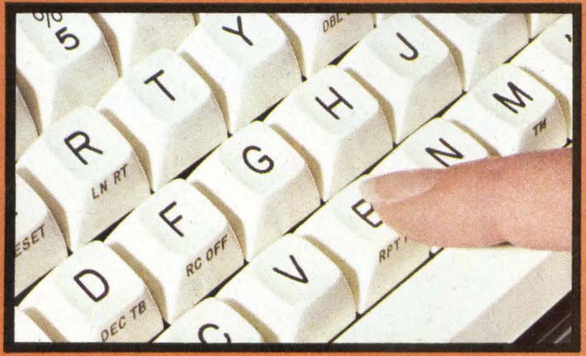
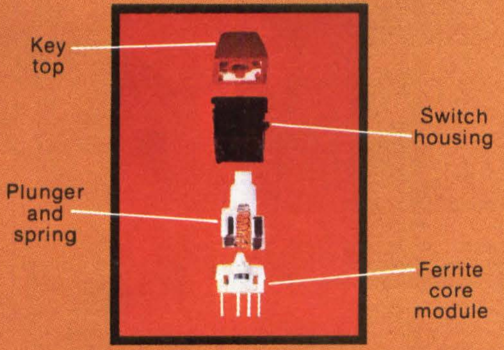


Get your hands on a CORTRON Solid State Keyboard, and you'll soon find out why you can't judge all keyboards on initial price alone.

It's after installation that cost efficiency becomes most important. In life expectancy, ability to endure extreme environments, high speed operation without "misses," accuracy, downtime caused by beverage spillages, reliability, serviceability and human engineered features. That's where a CORTRON Solid State Keyboard really pays off.



Unique contactless key switch makes the difference. Utilizing ferrite core switching technology, the CORTRON Key Switch is mechanically simple (only 4 basic parts!) and has an ultra reliable 100 million cycle life test rating. CORTRON Keyboard Professionals can translate what this can mean to you in cost efficiency terms of MTBF (mean time before failure). CORTRON has actual customer experience of MTBF in excess of 40,000 hours.

They'll also explain other advantages you'll gain over competitive technologies such as Hall effect, reed switch, and capacitive switching. All in all, you'll find the CORTRON Key Switch offers unusual built-in protection against costly service calls and the hardship of downtime.

"Human engineered" keytops and key placement options give CORTRON low profile alpha numeric keyboards the familiar "typewriter feel" that promotes operator productivity and efficiency.

Nothing left to chance. CORTRON solid state keyboard materials, components, subassemblies, and final assembly are 100% inspected and tested to assure your specifications are met with plenty of room to spare.

These are just a few of the cost efficiency benefits CORTRON offers you and your customers.

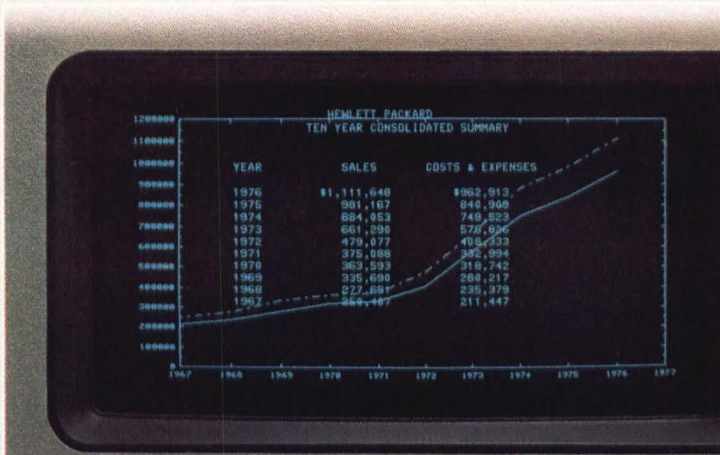
Cost efficiency you can put your finger on. For a greater insight into the cost efficiencies attainable with a CORTRON Solid State Keyboard, write or call for details: CORTRON, A Division of Illinois Tool Works Inc., 6601 West Irving Park Road, Chicago, Illinois 60634. Phone (312) 282-4040. TWX 910-221-0275.

CORTRON
A DIVISION OF ILLINOIS TOOL WORKS INC

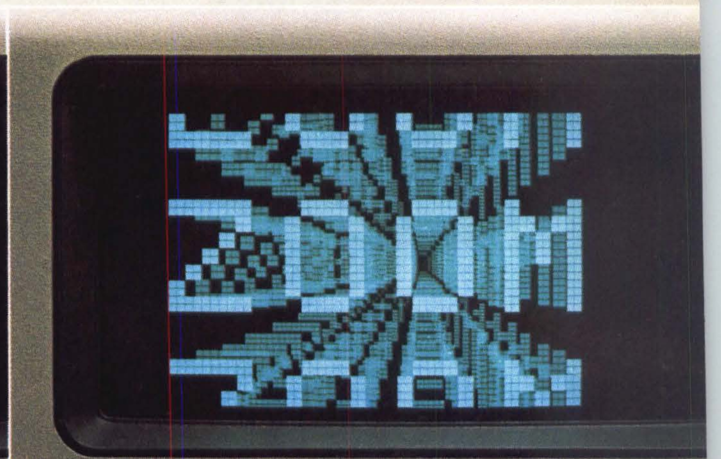
THE KEYBOARD PROFESSIONALS

CIRCLE 10 ON INQUIRY CARD

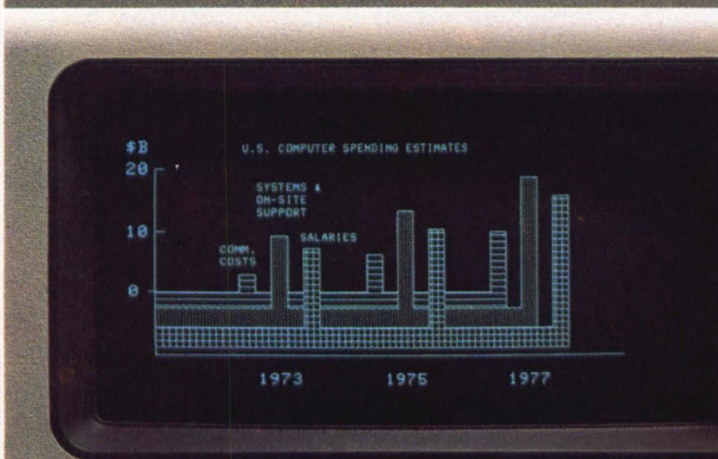
Hewlett-Packard brings a bright new look to low-cost graphics.



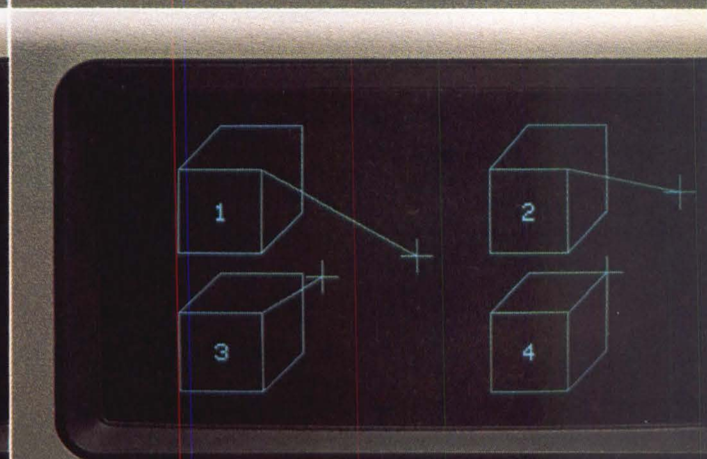
Auto-Plot



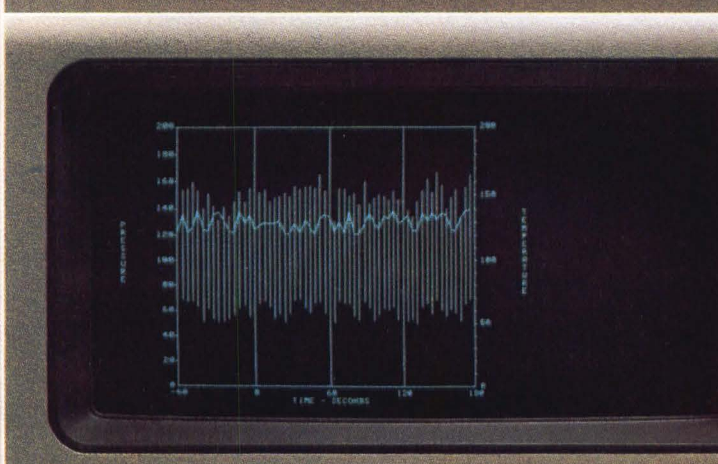
Zoom



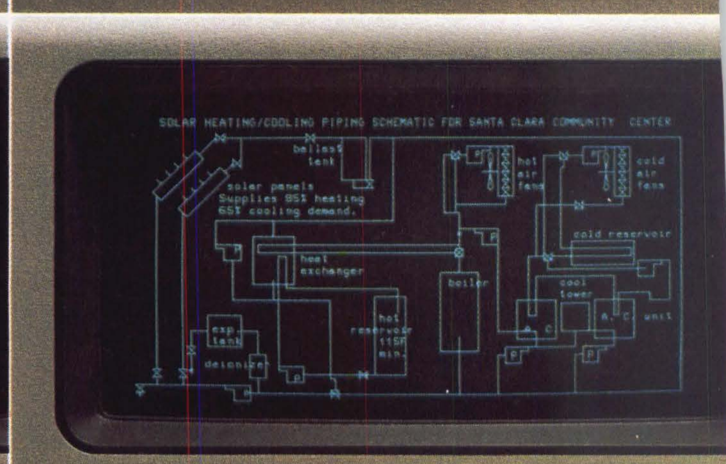
Area shading



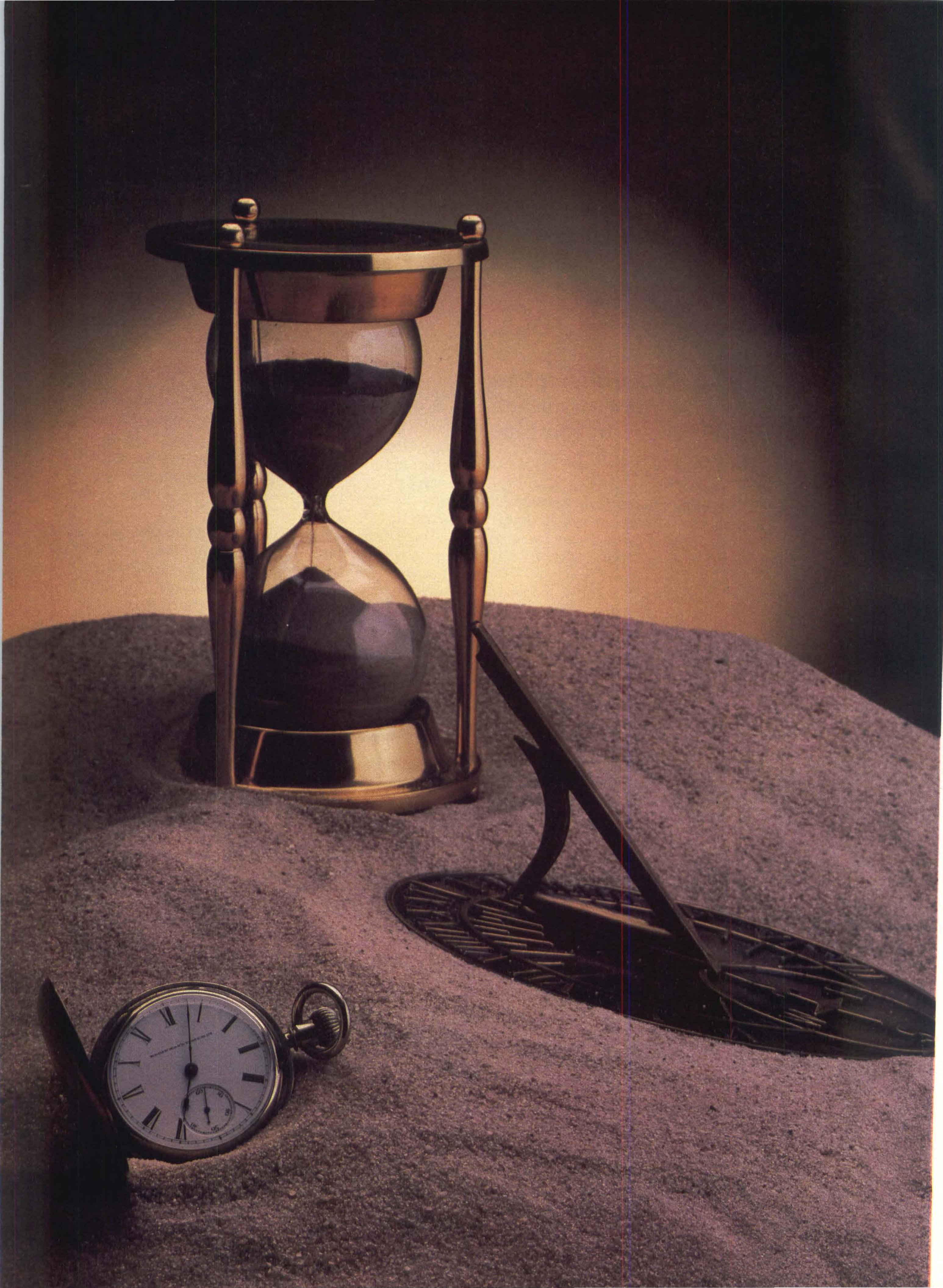
Rubber-band line



Typical application: scientific plotting.



Typical application: process flow diagram



Real-time problems? Systems has timely solutions.

Systems Engineering Laboratories has dedicated its 16 year corporate life to solving challenging real-time problems. The experience gained in solving these problems is what led us to pioneer the development of true 32-bit computer systems.

Look into the operating systems, the languages, the data base system, the real-time device handlers and terminal systems, and you will see that we build for the real-time environment. That's our business.

Choose from a well-bred family of computing systems: The SEL 32/35, the SEL 32/55, or the SEL 32/75. Unlike other so-called "32-bit minis" that are only bridge-the-gap systems developed from essentially 16-bit architecture, all SEL 32 systems are true 32-bit machines. This results in richer instruction sets, more precision in data representation and larger, directly-addressable memory. All are available with throughput rates in excess of 26 million bytes/second.

Systems computers fit the term "minicomputer" in price alone. If your application is performance-sensitive, we'll save you money. If you're budget-sensitive, we'll give you more performance for your dollar.

The SEL 32/35 can be configured from 64K bytes to 512K bytes of 900 nsec memory. Resembling its more powerful brothers, the SEL 32/35 is a complete package, including control processor with floating-point arithmetic, memory, chassis, power supplies and cabinet.

The SEL 32/55 is offered in a variety of both single and multiple CPU configurations, with from 32K bytes to 1 million bytes of 600 nsec memory.

The SEL 32/75, with up to 16 million bytes of main memory, has a concept so new, we had to coin a special term to describe one of its main features: Regional Processing Units. Working independently, these RPU's contain sufficient control and buffer storage areas to process an I/O region and transfer the resultant data directly to main memory. Computer system throughput is further enhanced by High-Speed Floating- Point Hardware and Writeable Control Storage.

Just circle our number on the Reader Service Card, or call us today. We'll send you the powerful story of the SEL 32 family.

SYSTEMS
ENGINEERING LABORATORIES

☐ CALL ME
☐ SEND ME MORE INFORMATION
☐ I HAVE PRESENT NEED FOR SYSTEM
NAME ____________
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SYSTEMS Engineering Laboratories
6901 West Sunrise Boulevard, Fort Lauderdale, Florida 33313
(305) 587 2900

CIRCLE 12 ON INQUIRY CARD

collection and dissemination on a real-time basis. This aspect is further enhanced since many of these envisioned applications would utilize standard pushbutton telephone sets for data input.

This telephone set also could be used as an audio output device if the CBX is equipped with a voice answer-back peripheral. In a retrieval application an authorized department manager can ask for the total time accumulated on a specific project. The CBX searches the data file for the project number, accumulates the total, and transmits it to the manager by means of the audio response unit.

Through the use of specialized telephone sets, more automated data collection and coordination applications can be implemented. In a manufacturing production environment, existing card dialer pushbutton telephones (also used to make normal phone calls) can be effective data input terminals; an electronic assembly application could have such telephones at the parts receiving and testing area. When a shipment of electronic components are received, a dialing card for the parts lot number can be prepared and read into the CBX, with the quantity entered by the employee. Following receiving inspection and test, the card is again read and the employee enters the accepted quantity. When components are transferred from parts inventory to assembly, the application cards identify the part lots and an assembly card can be prepared and entered for this assembly lot. The assembly personnel would enter the card when actual assembly was initiated and completed. At manufacturing quality control, the same card would be entered along with the quantity of accepted assembly units. The compilation of these incremental source data inputs results in a comprehensive and dynamic manufacturing reporting and inventory system, and an effective employee performance tracking system.

The office automation possibilities of a CBX considered as a computer system that switches audio calls are extensive. Specialized systems are already marketed for office environmental control; the CBX, however, could receive input from environmental transducers connected in lieu of telephone instruments. In another case, access and personnel sensors in a building could track movements throughout the building during nonworking hours; when programmed thresholds or conditions are detected, security personnel are notified or certain specified areas are secured.

The CBX has been a viable system in the marketplace for only two years, with initial growth focusing exclusively on voice telephone applications. With the continued addition of specialized or traditional data terminals, the CBX can become an office automation system.

The operating telephone companies of the Bell Telephone System currently are one of the largest vendors of computerized telephone systems. Under the Consent Decree in force from the federal government on AT&T, as well as the Computer Communications ruling from the FCC, AT&T is prohibited from providing such office automation applications. As the realization of these CBX capabilities becomes evident to potential users, the demand for such applications may stimulate AT&T to try to reverse or modify their present legal and regulatory restrictions. The outcome of negotiations and compromises that would be necessary to achieve this objective, combined with the introduction of computerized telephone systems for more advanced requirements, can be expected to radically change the present telecommunications and data processing environments.

Get Smart.

ADDS *Regent* • Smart for the price of Dumb.

Time was, if a man bought a Dumb terminal, he was considered pretty smart. Times change.

ADDS Regent family of Smart terminals is making Dumb look dumb.

For under $1000 our Regent 100 has features no smart man can resist.*

You get cursor controls for operational simplicity and extensive remote commands that make it easy to control the Regent from the computer. Optional function keys customize Regent to your specific application.

You get a Status Line that provides current information on the terminal's operating status. And, you get visual highlights such as blinking, zero intensity, half intensity, underline and reverse video.

You also get self diagnostics.

In other words, you get Smart. Or Smarter: Our Regent 200 has everything our 100 has plus buffered transmission, auxiliary port and editing options.

You can't get a whole lot more.

Get Smart. Get ADDS.

Quality, Reliability and Integrity. It all adds up to ADDS.

*In moderate quantity.

ADDS *Applied Digital Data Systems Inc.*
100 Marcus Blvd., Hauppauge, New York 11787 516-231-5400
Dept. 250

*Name*__________

*Firm*__________ *Title*__________

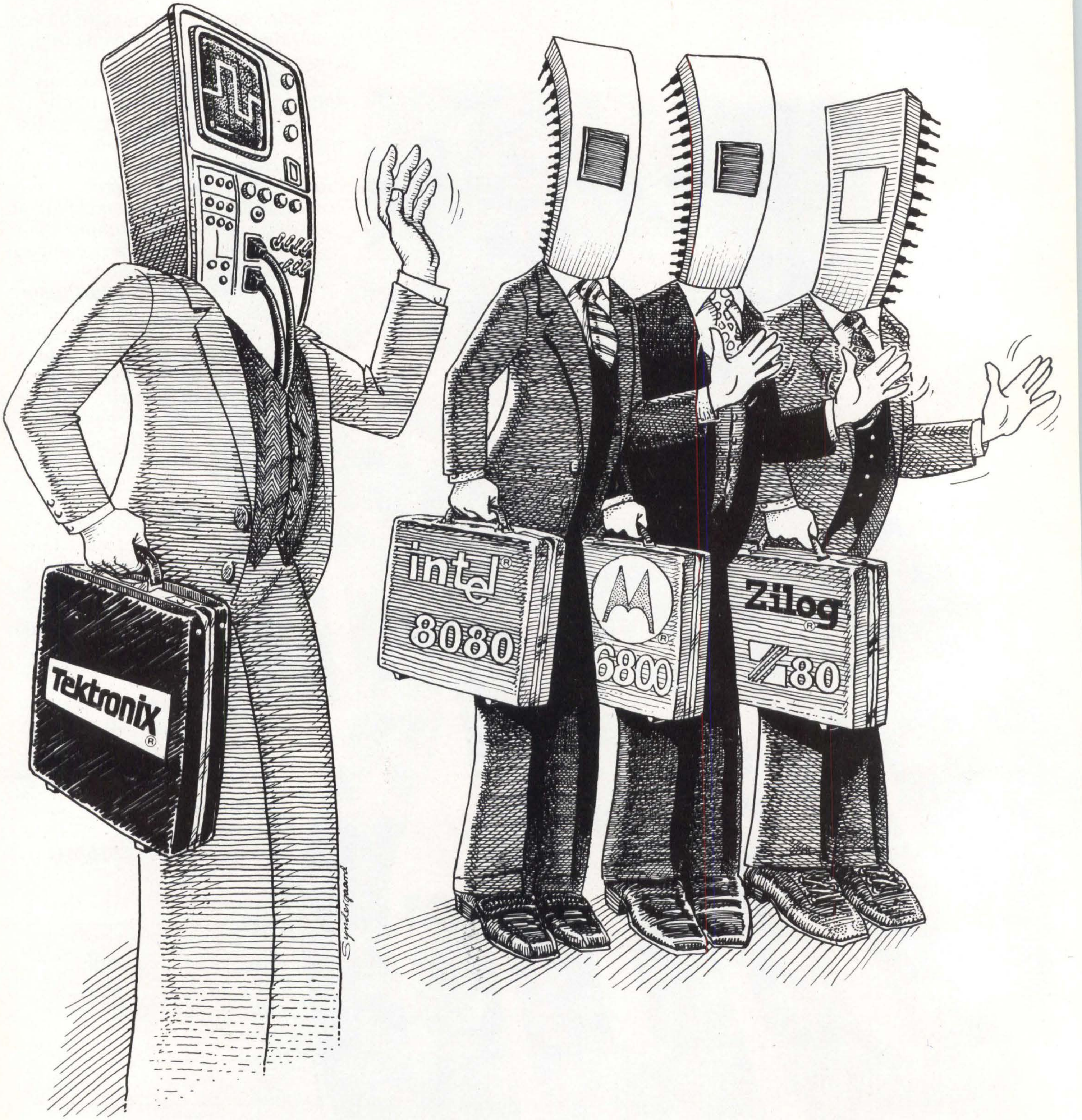
*Address*__________

*City*__________ *State*__________

*Phone*__________

CIRCLE 14 ON INQUIRY CARD

Are you rushing into microprocessor-based development with old friends?



You have a new friend.

You don't have to pay a big name price for a universal product development lab. And, don't let your fondness for a certain chip lead you to a convenient but confining marriage. The inevitable divorce will be costly and time consuming. If you want to develop products happily hereafter, move in with Futuredata.

Futuredata systems are universal.

We can move you into multiple-microprocessor-based product development at half the cost. With the largest selection of powerful hardware, software and economical peripherals around. With high speed disk or low cost tape operating systems. With in-circuit emulators for 8080, 6800, and Z-80. With the universal microcomputer that tackles every job.

Only Futuredata can move you in for $3850.*

No other microcomputer can match the cost/performance standards set by our MICROSYSTEM/20 & 30 disk-based systems and our MICROSYSTEM/10 & 15 tape-based systems. Each of these are complete development systems with up to 56K memory, 960 character CRT, ASCII keyboard, two RS-232 serial ports, 8-bit parallel I/O, real-time clock, bootstrap in PROM, 8-level vectored interrupts and complete disk and tape operating systems with monitor, debugger, editor, assembler and utility.

*Domestic U.S.A. prices

The most complete spectrum of economical systems.

Move in with our Dual 5″ Mini Floppy Disk System, our Dual 8″ Standard Floppy Disk System, our unique QUICKRUN™ 32K Tape Operating System or our new Universal Dual Development System. No matter which you choose, the savings will be significant.

Only Futuredata has QUICKRUN.™

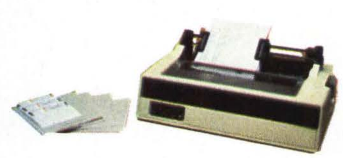
MICROSYSTEM/15 has the only co-resident assembly and interactive debugging system in the industry. With editor, assembler and debugger/monitor all in memory, things happen fast. Assembly of a 1000 statement program takes a mere 15 seconds. At $5275,* it's the most cost-effective development tool around.

Now the first Universal Dual Development System.

Futuredata has combined two separate memory/processor systems in one host computer. Mix or match processors, disk or tape operating systems in each half. Put two development engineers to work at full speed, simultaneously. You get two complete systems in one and save nearly $2000.

In-circuit emulation and higher-level language.

We have in-circuit MICROEMULATORS™ for 8080, 6800, Z-80, Extended BASIC, line printers, EPROM programmers, hardware, software, documentation and a rock-solid record for reliability. So, let's be friends!



30-day "Get Acquainted" offer.

Try one of our development systems for 30 days at no risk. For more information, write or call Futuredata today.

Move into product development with a new friend...

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SEE US AT MINI/MICRO '77, BOOTH #608.

CIRCLE 15 ON INQUIRY CARD

Automated Switching Expedites Data Transfers On All Types of Networks

For multicomputer data networks, the Multitran M3000 series digital network management switch system permits operators of asynchronous terminals to selectively access diverse computer resources. These resources may be application or speed dependent ports on a single computer, or multiple computers located at a single facility or in widely dispersed locations.

The device's function is to dynamically switch data between two channels at high speed with almost no delay. Maximum configuration of an asynchronous switch accommodates a bandwidth of about 60k char/s.

Installed by Computer Transmission Corp, El Segundo, CA 90245 in several applications, the switch replaced telephone data network systems that were so congested that voice communications became degraded. The unit, containing the company's Directran[R] data set, a modem located at the terminal and at the switch, frees the telephone system for voice grade transmission.
Circle 400 on Inquiry Card

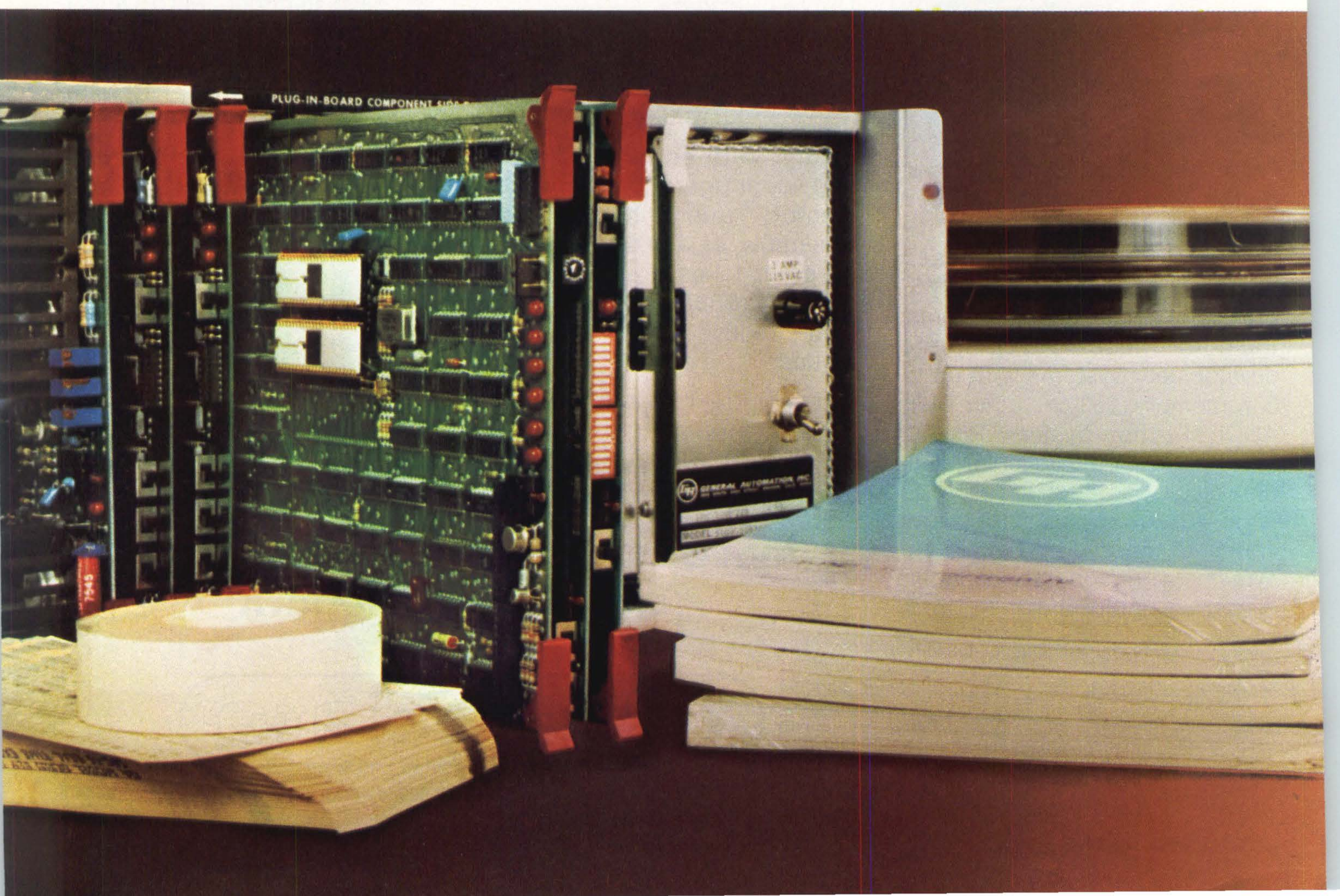
Wideband Communications Are Predicted to Impact Leisure and Business

Communications satellites and fiber optic technologies will soon be combined to provide universal, inexpensive, wideband communications which will change people's working and leisure lives, according to the "Impact of Wideband Communications" report available from International Resource Development Inc, 125 Elm St, New Canaan, CT 06840. While previously too expensive for all but major communications users, a proliferation of wideband telecommunications will have a major effect on the economics of teleconferencing, electronic mail, and data communications.

These effects are expected to be reflected in some substitution of teleconferencing for airline travel, some changes in the way paper is used for business correspondence and forms, and development of new types of office equipment.
Circle 401 on Inquiry Card

Tremendous Increase In Facsimile Use Is Forecast

Increased communications speed, lower equipment and line costs, versatility, interfaces to other systems, and postal service cost increases are



the factors which are most likely to place facsimile technology into many offices during the next few years, and conceivably into the home. Predicting these developments, Dal Berry, president of Graphic Systems, Inc, Corporate Dr, Commerce Park, Danbury, CT 06810 foresees interfaces between facsimile units and copiers for faster and cheaper distribution. Data compression transmission techniques and communications networks using satellites and fiber optic cables will play a significant role in reducing communications costs.

Future information processing networks must be able to handle communications in the forms of words, numbers, voice, and graphics; facsimile can handle more of these than any other technology. As the number of compatible facsimile units increases, the emphasis will shift from intra to intercompany communication. According to Quantum Science Corp, facsimile shipments are expected to reach $700M by 1980.

U.S. Packet Network Implements Standard X.25 Interface

Synchronous data communications service for computers and other programmable devices equipped with a standard X.25 interface is being implemented in the U.S. by Telenet Communications Corp, 1050 17th St, NW, Washington, DC 20036. The added capability for users of the company's public packet network and other compatible packet networks worldwide permit a computer to handle up to 4095 logical connections simultaneously over a single network access line. Each connection is switchable on demand and individually flow-controlled, so that devices of dissimilar speeds can communicate without loss of data or congestion.

The service will be made available in Boston, Chicago, Dallas, Los Angeles, New York, San Francisco, and Washington, DC. By the first quarter of 1978 a total of 22 cities should be included. International expansion is also being planned.

Agreement Upgrades and Expands Switching System

A five-year agreement signed by Collins Commercial Telecommunications Group of Rockwell International, Dallas, TX 75207 and Securities Industry Automation Corp (SIAC) provides expansion and upgrading of SIAC's existing Rockwell-Collins front end/message switching system. Two separate 2-processor C-Systems front-ending a Univac host processor, manufactured by the Collins Communications Switching Systems Div in Dallas, are to be installed to form the Automated Bonds System and Common Message Switch at SIAC's computer center in New York City. □

Our new mini/micro computer printers... "the easy ones."

Features:

- Three popular ASCII input configurations
- Forty characters per line
- Internal data storage
- Double-width character selection
- Power line filter
- Optional tally-roll and/or fast paper feed

EASY TO INTERFACE
The new DP-1000 Series Printer family fits right into most mini-micro computer and modem applications – thanks to three popular ASCII formats available in four different basic models.

Standard Baud rates from 110 to 2400 Baud, and internal storage of up to 104 characters (more optionally) with "hand-shake" control signals, let you pick from a variety of off-the-shelf configurations to fit your specific application.

EASY TO USE
A time-proven, dot matrix impact printing element can print 64 alpha-numeric and special symbols in 40 characters/line at 50 CPS on single or multiple-copy paper rolls. Options such as Tally Roll take-up and Fast Paper Feed, make the printers easy to fit point-of-sale and related fields.

Combining form and function, the modern package blends with virtually any surroundings, while its flip-top design allows convenient access for paper replacement and servicing.

EASY ON BUDGETS
Best of all, single-unit prices for the DP-1000 Series start at under $700, with substantial Dealer and OEM quantity discounts.

Want to see a demonstration in your office, or more details? That's easy too. Just contact Ken Mathews at Anadex; 9825 DeSoto Avenue; Chatsworth, CA 91311; Telephone (213) 998-8010; TWX 910-494-2761.

Anadex

"See us at Mini/Micro Show, Booth 307."

16-Bit Minicomputer Addresses 256k Bytes, Has Mainframe Features

Model 8/16E processor, a 16-bit computer system capable of addressing 256k bytes of semiconductor memory, provides performance capabilities and economy. Suited for use in scientific computation, process control, and data communications, the systems include an enhanced OS/16 MT2 operating system and extended FORTRAN IV software packages.

The 8/16E processor was designed by Interdata, Inc, a unit of Perkin-Elmer Data Systems, 2 Crescent Pl, Oceanport, NJ 07757, to provide big machine features such as 16 general-purpose registers, an IBM-like instruction set, list processing instructions, dual I/O bus architecture, and 255 automatic I/O channels. Integral memory management hardware permits up to 256k bytes of memory to be addressed. Available in 32k-byte increments, memory has an 275-ns access time and a 750-ns cycle time.

Processor architecture, similar to that of the 360/370 line, includes 16 general-purpose registers which reduce overhead, cut execution time, and simplify program development. Supervisor mode when enabled causes I/O and most status switching instructions to become privileged instructions.

Integral memory mapping hardware permits expansion of physical memory from 64k bytes to 256k bytes. Program mapping is performed by implementing additional bits in the program status word. Load program status, load program status register, set map, and set map register instructions control these additional bits, and also serve to minimize the associated overhead incurred by user programs.

Selected blocks of memory can be allocated as write protected, read/write protected, or instruction execution protected through the memory protect controller. Memory can be partitioned into a maximum of 64 blocks with individual protection for each block. The controller also provides two loadable maps for data security and integrity.

In the 156-instruction set are several classes intended to increase memory utilization efficiency. The set provides both 16- and 32-bit formats and permits operation between two general registers; or between a general register and a memory location, a 16-bit data constant carried in the primary instruction word, or a 4-bit data constant.

Dual bus structure of the I/O system permits high speed devices to operate at a maximum of 2,666,000 bytes/s over the optional extended memory selector channel. Operation of selector or multiplexer channel can be 8 or 16 bits parallel. Either channel operates on a request-response basis for reliable device controller design.

OS/16 MT2 is a real-time, multitasking operating system which provides an event-driven environment for user application programs. It manages system resources, including access to the processor, with up to 255 levels of priority defined by the user. In addition, it provides intertask communication and control facilities, including task common and reentrant libraries, which allow users to create structured event-driven systems such as those needed by transaction processing systems.

Extended FORTRAN IV enables users to access the power of processors efficiently and with a minimum of systems resources. Operating in as little as 21k-bytes memory, the compiler directly generates object code, minimizing program development time, effort, and cost. Exceeding requirements of ANSI standard (X3.9—1966) FORTRAN, the software provides extensions such as mixed mode arithmetic, ENCODE/DECODE, and Integer *2. A special Reentrant Runtime Library results in greater speed, and accuracy which is better than five decimal digits for REAL function and better than 14 decimal digits for double-precision function.

Circle 410 on Inquiry Card

Fiber-Optic Kit Allows Engineering Evaluation of Complete Interconnection System

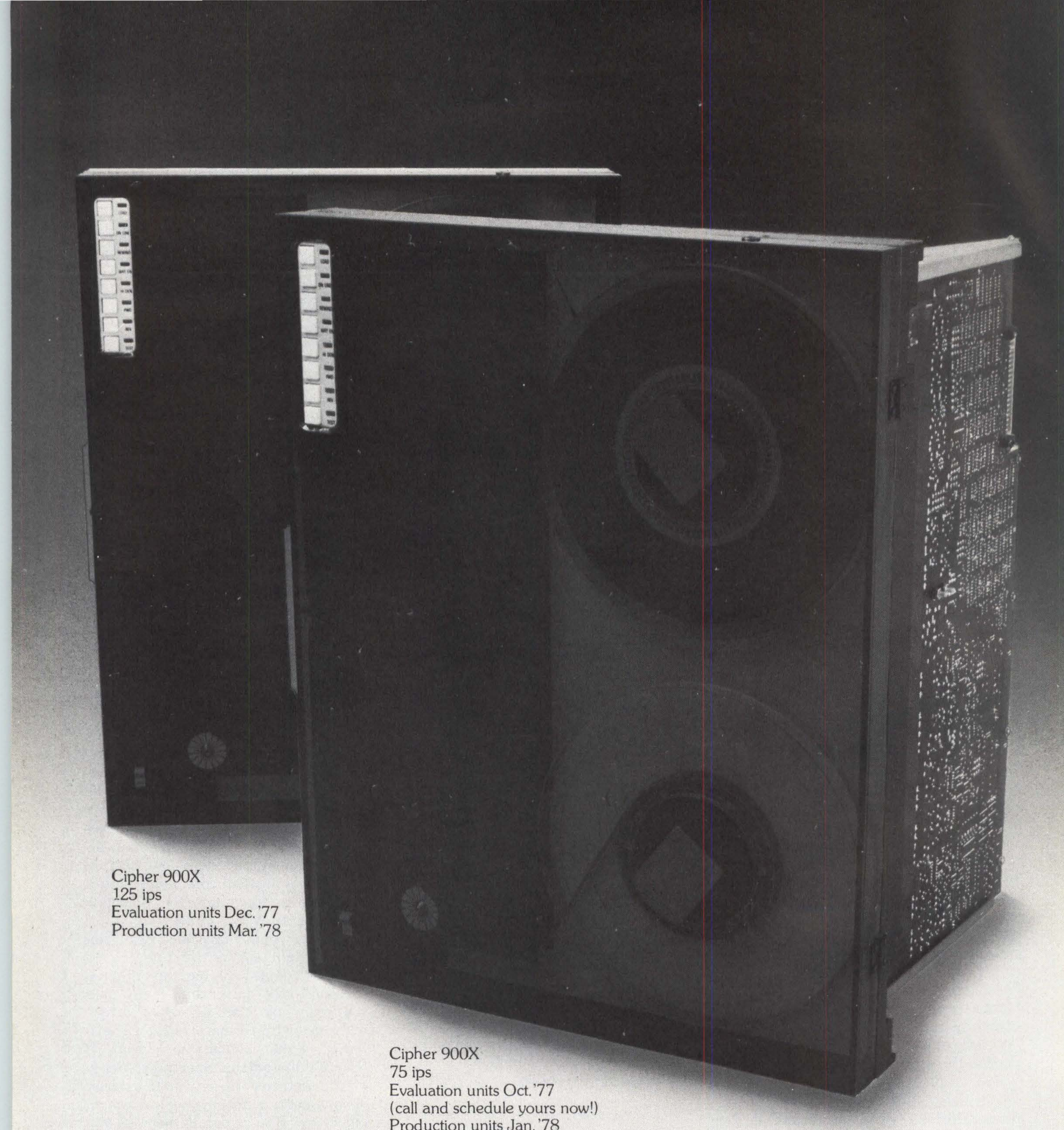
A fiber-optic evaluation kit, designed by systems engineers familiar with applications requiring complete TTL electronics, offers a complete interconnect system, rather than connectors only. The system, designed for OEM use as well as laboratory experimentation, allows engineering evaluation of fiber-optic interconnection. It operates from dc to 5M bits/s over the 0 to 55°C temperature range without drifts or inadvertent comparator switching.

Fiber-optic evaluation kit developed by Augat provides a complete interconnection system which allows engineers to evaluate the technology for applications requiring TTL electronics

The kit, developed by Augat, Inc, Interconnection Products Div, 33 Perry Ave, PO Box 779, Attleboro, MA 02703, contains emitter assembly, 5-m fiber-optic cable assembly, temperature referenced photodetector assembly, TTL-compatible preamplifier and TTL-compatible emitter driver. A second kit is available without preamplifier and driver for applications not requiring the electronics package. Both include a comprehensive application engineering instruction manual containing circuit diagrams for operation to 5M bits/s digital or 10 MHz analog.

Emitter transforms electrical signals to light signals through an IR-emitting diode. It has an 880-nm spectral peak and exhibits rise and fall times of <50 ns when driven with ICs or transistors. Detector transforms light signal to electrical through photodiode. Spectral response of the detector closely matches that of the emitter for maximum system efficiency. Rise and fall times of the detector are <35 ns when properly biased and loaded by receiver circuitry described in the instruction manual. Interconnection of the emitter and detector assemblies is accomplished with a 5-m fiber-optic cable—a 180-fiber bundle with 0.045" (0.114-cm) bundle diameter, jacketed with black Hytrel[R] for strength and crush resistance.

Emitter driver provides a complete TTL-compatible fiber-optic



Cipher 900X
125 ips
Evaluation units Dec. '77
Production units Mar. '78

Cipher 900X
75 ips
Evaluation units Oct. '77
(call and schedule yours now!)
Production units Jan. '78

Cipher delivers a quiet blow to the competition.

Quiet as a whisper, the 75 and 125 ips Cipher vacuum tape transports simply obsolete every other vacuum drive on the market today.

By design and construction, the Cipher 900X vacuum tape drives are simply the best, most reliable tape transports on the market today. Bar none.

It starts with complete microprocessor control of all of the transport's functions, including complete self-test/diagnostics and a full measure of protection for the tape and an extraordinary reduction of maintenance problems.

In conjunction with our switched linear servo electronics, the microprocessor maintains total servo control during critical load and unload or power fail sequences. It's the smoothest tape handling you've ever seen; there is no possibility of tape damage even if a power failure should occur during high speed rewind.

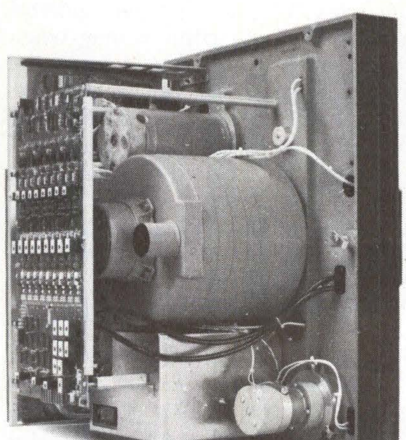
Power wise. The Cipher 900X series is the lowest power user of all vacuum tape transports. Averaging 300 to 350 Watts with a worst case 450 Watts Continuous Power Dissipation, the 900X series uses roughly half the 650 to over 1,000 Watts used by other vacuum tape transports.

You won't believe the quiet. Thanks to the Cipher 900X's multistage low speed vacuum pump, we use a much smaller motor. At 3400 rpms, our motor is substantially quieter than the competition's 10,000 rpm motors. A whisper instead of a high-pitched whine. And we've reduced more than noise. We've also knocked out 50% of the maintenance requirements found in traditional vacuum tape drives by eliminating belt drives.

No relays. Because the Cipher 900X incorporates opto-isolators to drive the blower motor and switch the high voltage AC components at the zero crossing line, transient generated line RFI is minimized. Power usage is drastically reduced. So is maintenance.

No incandescents. Light Emitting Diodes are used in place of incandescents in the 900X. With the field-proven reliability of solid state electronics, the unpredictable behavior of incandescents is eliminated.

Improved tape path. Only the long life sapphire cleaner and the chrome head (guaranteed for 5,000 working hours) come in contact with the tape. Air entering the tape path is filtered and the tape path itself is under a low positive pressure to prevent accidental ingestion of particular contaminants. No guesswork loading, since servos and transducers under control of the microprocessor automatically feed the column during load and unload. Servo controlled shutdown power fails protect the tape since, in the event of a brown out or failure, energy stored in the servos is utilized to effect a controlled power down.



Easiest to maintain and repair. Our exclusive Optical Sensing File Protect replaces troublesome switches, solenoids and trouble-prone mechanisms. And because the Cipher 900X has internally generated sequences of diagnostic and alignment tests, the MTTR is cut a good 30% by immediately locating the problem area. All mechanical and electronic assemblies in the 900X are modular. No special tools or fixtures are required; all critical tolerances are machined in.

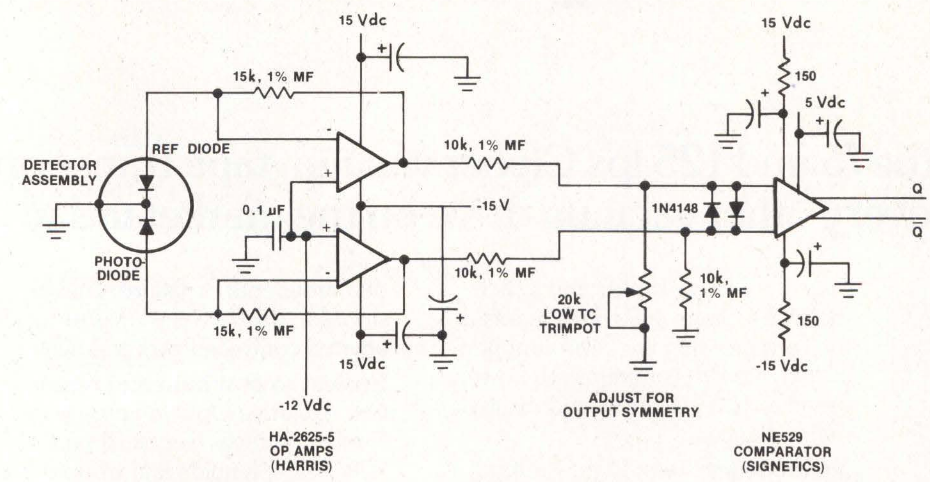
The only thing missing are the problems: No belts, no hoses, no relays, no solenoids, no incandescents, no cooling fans, no power surges, no contaminants, no noise problems, no maintenance problems, no special tools or fixtures, no false EOT/BOT detection, no tape problems—no load snap, no whip, no shredding, no special precautions, no guesswork, and best of all—no price premium. None.

With design simplicity and the use of advanced solid state electronic components, the Cipher 900X series provides unparalleled performance, reliability and serviceability. At low cost. And quietly, too.

For further information and specifications, contact Cipher Data Products, 5630 Kearny Mesa Road, San Diego, California 92111. Headquarters: (714) 279-6550. TWX: 910-335-1251. Eastern Region: (617) 449-3182. Central Region: (312) 296-7250. Or contact your Cipher representative.

See us at Mini/Micro '77 Booth #501/502

Cipher Data Products



Detector in Augat's fiber-optic kit has rise and fall times of <35 ns when biased and loaded using receiver circuitry such as that illustrated

transmitter when used with the emitter assembly, a 5-V power supply, and an optional filter capacitor. Preamplifier provides a complete TTL-compatible fiber-optic receiver when used with the detector assembly, trim pot, and power supply. Both driver and preamplifier are contained in a 24-pin DIP.

All connectors utilize a waveguide beyond cutoff design and are of gold-plated brass construction to ensure retention of the integrity of shielded enclosures. Teflon sockets and low-profile, right-angle brackets are included for PC board, chassis, panel, or bulkhead mounting and connection of the emitter and detector assemblies.

Other standard accessories (not in kit) include cable splice for inline or bulkhead use, O-ring set for hermetically sealing emitter and detector assemblies, and fiber-optic cables of various standard lengths. Kit 698-OK-001 (without electronics) is priced at $99.50 in any quantity; 698-OK-002 (with preamp and driver) sells for $190 in any quantity.

Circle 411 on Inquiry Card

Printer/Printer Terminal uProcessor Controlled For Optimum Throughput

First members of a family of 180-char/s dot matrix serial printers, introduced by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, are the 2631A printer and 2635A printing terminal. Operating under control of an sos microprocessor, both units offer as standard three different ways to print, fast replacement cartridge ribbon, automatic underlining, and smart bidirectional printing.

Bidirectional printing path is controlled by a "smart printing" algorithm. Leading and trailing spaces are detected and ignored; the head moves directly to the next material to be printed. Looking ahead in the data stream, the printer detects spaces imbedded within a line; when 10 or more spaces are found, the printhead speeds to the next printable character at an accelerated 45-in (114-cm)/s rate. Horizontal tabs, a standard feature on both units, also initiate this fast movement. With throughput thus optimized, apparent print rate often exceeds nominal specifications.

There are three standard print modes: normal, expanded, and compressed. In normal mode, 10 char/in (4/cm), 136 columns can be printed on 14" (36-cm) paper. A 5-char/in (2/cm) expanded mode is useful for bold face and highlighting. In compressed mode, 136 columns can be printed on 8.5" (21.6-cm) paper, or 227 columns on 14" (36-cm) paper. Underlining can be simultaneous with printing, and characters may be overstruck. A display functions feature causes control functions to be printed; this is a useful tool for program development.

Vertical line spacing is variable under program control; choices are 1, 2, 3, 4, 6, 8, or 12 lines/in (12 lines/in is used to print subscripts and superscripts). A switch on the 2631A can select 6 or 8 lines/in; any choice may be made via the keyboard on the 2635A.

The long-life printhead needs no alignment, and is therefore easily replaced by the user. The ribbon, good for more than 10M char, is contained in an easily replaced cartridge. Self-test can be initiated by the operator or by a program, to verify proper operation. Standard equipment is the USASCII 128-char set. Each character is formed by dots in a matrix of seven columns and nine rows. Both units can accommodate one additional 128-char set.

Standard interface for the 2631A is an 8-bit differential line driver configuration compatible with the company's line printers. The 2635A features an EIA RS-232-C interface as std. Optional interfaces include EIA RS-232-C with 202-type modem control, and current loop; for the 2631A, HP-IB and 8-bit TTL parallel are also offered.

The microprocessor in both products is a company-designed 16-bit silicon-on-sapphire (sos) device designed specifically to provide a broad

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All the Data I/O programmers save lab time and slash your development expense. These are portable, rugged, human-engineered and easy to use units. They're ideal for field service. Both the Model V and Model IX offer a direct display readout of PROM or RAM data at any address and offer unlimited data editing capabilities. Operation is totally automatic, and you can enter data manually through the keyboard or load it automatically from a preprogrammed master PROM. There are built-in error checking routines to insure accurate and correct data transfers, and serial or parallel I/O are standard. These unique PROM programmers and their personality cards are available now.

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CIRCLE 18 ON INQUIRY CARD

range of I/O and program control capabilities and to optimize controller type applications.* A 34-mm² chip, containing approximately 9600 transistors, executes 34 basic classes of 16-bit instructions tailored for I/O processing. The instruction set allows direct access to 16 registers, eight of which are located in the processor chip itself.

Control capabilities are implemented via decision-making mechanisms such as computed branch and condition code interrogation. Also available are stacked subroutine linkages, direct addressing to 64k words of memory, indexed and indirect addressing modes, and immediate operands. At a worst case 150-ns minor cycle time, instruction speeds range from 0.6 to 1.8 μs with a mean of 1.05 μs.

The chip features fully static and synchronous operation with a single-phase clock. This eases system clock requirements, and aids testing and system debugging by allowing single minor cycling, or single instruction cycling. It can use a single 12-V power supply and dissipates 0.5 W at its full rated speed.

Separate asynchronous I/O and memory handshakes permit memory and I/O operating at different speeds to be mixed. Separation of data, address, and control buses simplifies decoding and increases bandwidth. Both data and address paths are 16-bit bidirectional 3-state buses, permitting simple, fast interface to the processor, thus minimizing system overhead.

Circle 412 on Inquiry Card

Image Display Device Produces 3-D Illusions From Computer Data

An image display device that may bring improved accuracy to air traffic control, mapping of underground ore deposits, and analysis of data from medical scanners has been developed at the University of Utah, Salt Lake City, UT 84112. The 3-D virtual image display device, developed by the Advanced Imaging Methods Laboratory, uses a special optical system and a television screen to produce a realistic 3-D illusion. Such an image can be created from any type of data that can be fed into a computer, including 3-dimensional graphs, brain scanner images, X-rays, maps, and drawings.

Prototype image display system at University of Utah creates realistic 3-D illusions by projecting onto a television screen a series of 2-dimensional images formed from computer stored data. Special optical system spreads the images behind the screen to achieve 3-D illusion

"The special optical system takes a series of 2-dimensional images stored in the computer, and projects them, one behind another using a television screen," says Dr Steven A. Johnson, research associate professor in bioengineering and associate consultant at the Mayo Clinic. "It does not require special glasses like the old 3-D movies, and several people can look at the image at the same time. A person can also move his head and see around the side of the image.

A laboratory prototype of the device, constructed by Johnson and Dr Brent S. Baxter, assistant professor of radiology, has been used to display 3-D images of X-ray brain scans and simple geometric forms. With this device, the scientists hope to be able to view a 3-D image of the contents of the skull which will emphasize lesions and other highlighted structures. This would not only provide advantages in diagnosis, but would give the surgeon a better feel for the location and size of the problem he is trying to correct.

If the prototype achieves the kind of results that are expected, the scientists plan to design a second one which will connect directly with the scanner's computer memory. Although it is now possible to produce only black and white images, there is no reason that color images cannot be achieved.

Circle 413 on Inquiry Card

8080-Based Controller Supports Terminal Cluster Plus Communications

Offering the computing power of larger systems, the SPD 15/25 cluster controller has a price/performance ratio that is acceptable to smaller installations. Incoterm Corp, 65 Walnut St, Wellesley Hills, MA 02181 accomplished this by basing the terminal processing unit on the industry standard 8080A microprocessor.

The SPD 15/25 is a programmable controller for attaching display terminal clusters and online communication to a central computer. Its terminal processing unit (TPU) operates compatibly with the communications protocol of a variety of mainframe computers; it can support up to two 1920-char displays or four 960-char displays, as well as a full line of printers. Multiplexing TPUs enables them to share a single modem and provide extra display positions if required.

In addition to a fully programmable interrupt system, arithmetic/logical processor, and a real-time clock in the controller, the internal TPU has a refresh subsystem with 4k bytes of directly addressable RAM for screen data. A controller can contain up to 64k bytes of addressable memory made up of RAM, EPROM, or core.

A built-in communication controller operates in full- or half-duplex mode with synchronous or asynchronous protocols at speeds from 75 to 9600 bits/s. Support for all standard

*For a more complete technical description of the microprocessor, see "A CMOS/SOS 16-Bit Parallel μCPU," Lam-Giang Dang, et al, *Proceedings of the 1977 IEEE International Solid-State Circuits Conf*, pp 134, 135, 245.

TALLY 1200 BAUD PRINTER TERMINAL

Key into Tally. . . the most flexible printer

EVERYTHING YOU COULD ASK FOR IN A PRINTER TERMINAL

The Tally T-1612—loaded with functions and features, yet simple enough for anyone to master. Your operator will like Tally best. Here's why. It's quiet. Easy to operate. And very flexible. You can load control functions from your user program or directly from the keyboard. In fact, you get 42 operator programmable keyboard functions. Even unique ones like double width character printing. With Tally, you can mix and mingle 6 different type fonts by simple keyboard programming. And, of course, Tally superb print quality is a built-in bonus.

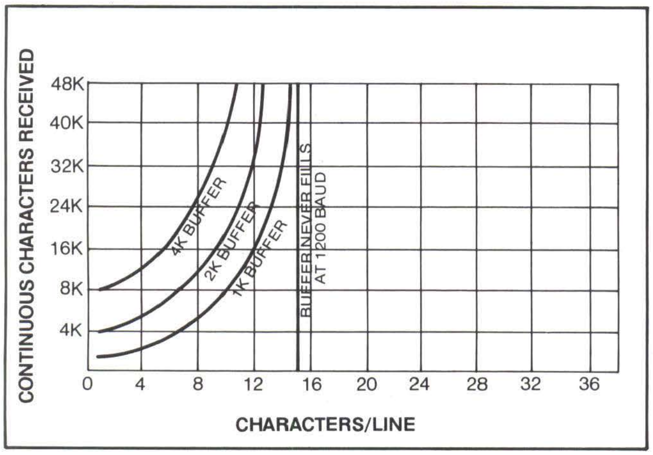
Boasting a 1 k buffer to sustain a full 1200 Baud printing rate, the T-1612 communicates comfortably at 300, 600, 1200, 2400, 4800 or 9600 Baud. Available in KSR or RO versions, use the Tally T-1612 for both communications and interactive computer console applications. The unit is fully compatible with all major time sharing services.

Convenience. The T-1612 is very operator friendly. And very quiet to the ear. For format programming or interactive communications, your front panel and keyboard controls are clearly labeled and easily accessible. With push button convenience you can select a vast variety of functions or operating modes. The machine can be as simple or as versatile as your needs dictate.

In keeping with easy operation, even forms handling duties are selectable through the keyboard. Select the appropriate keys and set up horizontal tab, vertical tab, top of form, forms length, top and bottom margin, and right and left margin.

Optimized operation. The T-1612 printer terminal is smart, too. Tally uses microprocessor electronics to deliver optimum printer throughput and cut down wasted motion. For bonus throughput, printing is bi-directional. The print head always looks ahead for the shortest path to the next print position. While searching, the head moves at an accelerated rate. This "optimized bi-directional" printing doubles or triples throughput over the printer's rated 160 characters per second without taxing the print head. So important for keeping pace with higher Baud rates.

Outstanding short line capability



HERE'S WHAT YOU GET WITH TALLY

Tabletop or pedestal mount.
160 cps bi-directional optimized printing.
300, 600, 1200, 4800, 9600 Baud operation.
Full-duplex or half-duplex.
ETX, EOT or Reverse Channel HDX protocols.
XON/XOFF FDX protocol.
Up to 218 columns (16.5 cpi).
128 ASCII character set.
ANSI keyboard with multi-key rollover.
Self-test.
Parity selection.
Paperout switch.
EIA interface.
1 k of buffer.
Automatic new line.
Automatic line feed.
20 character answerback.

OPTIONAL FEATURES

Bottom paper feed.
Alternate character set.
14 key numeric pad.
TTL interface.
20 ma/60 ma current loop interface.
75/1200, 150/1200 split Baud rates.
2 k or 4 k buffer.
APL code.

EASY TO USE, EASY TO LIKE

The Tally printer terminal has all the functions you want for optimum interactive data communications. The highly versatile keyboard uses a standard ANSI pattern for typewriter-like operation. A 14 key numeric pad adjacent to the standard keyboard is optional.

POWERFUL YET SIMPLE

Lots of features. Tally has the multi-key rollover feature if two keys are struck simultaneously. And 20 character answerback capability. (The message is stored in memory, and can be reprogrammed from the keyboard.) The standard printer terminal offers a full 128 ASCII code set. For the reduced set of 70 codes for compatibility with other ASCII equipment, simply set the All Caps locking key.

Other standard T-1612 features include end of line warning when keying data and automatic paperout detection. A convenience feature you'll appreciate is the view key for a clear look at the last characters printed.

Options you'll like include alternate character set and a programmable configuration that returns the printer to a specified condition upon power up.

Forms flexible. The Tally printer terminal is easy to like when it comes to forms handling. The flip-up tractor assembly affords easy access to the sprocket wheels for paper loading. Dual tractors are used to hold the paper securely for precise print registration. And the tractors adjust from either end of the carriage to accommodate various width forms from 4 inches to 15 inches. Up to six-part forms can be printed. Forms thickness control is standard. Optionally, the bottom load feature allows paper to enter the printer from either the bottom or back of the machine. Additionally, for clean, fast, and easy ribbon changing, the printer terminal offers a convenient snap-in cartridge. A large, easy to read column indicator is standard. At a glance, you quickly see the exact column you are on.

Tally T-1612 Printer Terminal

EIA/CCITT INTERFACE

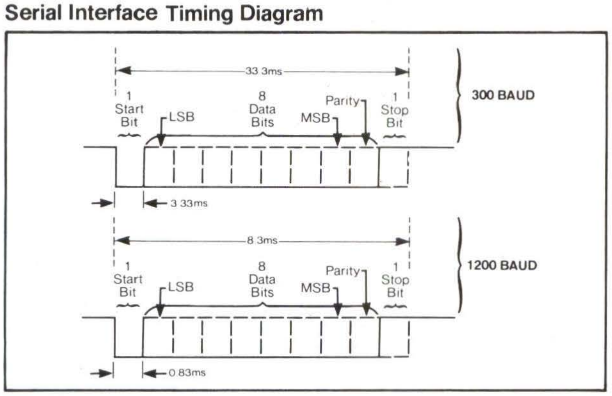
The Tally T-1612 features a standard EIA RS-232 C/CCITT recommendation V.24 serial interface. A nine-foot cable terminated with a standard 25-pin EIA connector is supplied. Pin connections are listed below.

Pin No.	EIA Circuit Designations	Circuit Descriptions
2	BA	Transmitted Data
3	BB	Received Data
4	CA	Request to Send
5	CB	Clear to Send
6	CC	Data Set Ready
8	CF	Rec. Line Signal Det (RLSD)
19	SCA	Sec. Request to Send
20	CD	Data Terminal Ready
22	CE	Ring Indicator
12	SCF	Speed Indicator (212 Series) Secondary RLSD (202 Series)
1	AA	Protective Ground
7	AB	Signal Ground

PARITY

Even parity or odd parity, with or without parity error printout can be selected by the user.

Serial Interface Timing Diagram



SPECIFICATIONS

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

OPERATION

Print speed
160 characters per second bi-directional optimized

Vertical slew
8.5 inches per second

Single line advance
50 ms

Full carriage return
350 ms

PRINTING FORMAT

Number of columns
132 (programmable for 80 column format)

Character set
96 character USASCII

Character style
Dot matrix, 7 × 7 half-space

Character size
0.080" wide × 0.106" high

Line spacing
6 and 8 lines per inch

Characters per inch
10, 12 and 16.5 cpi

Double width character
Standard

ELECTRICAL

Power
200 watts

Line voltages
105-140 VAC, 60 Hz±2%
90-110 VAC, 50 Hz±2%
187-264 VAC, 50 Hz±2%

PHYSICAL

Width
25.5"

Height
8.5"

Depth
27"

Weight
68.5 lb.

FORMS CONTROL

Feed mechanism
Sprocket feed adjustable from 4" to 15"

Paper out
Audio alarm sounds 3" from bottom of form

FORMS SPECIFICATIONS

Type
Continuous fanfold, edge perforated

Width
Variable from 4" to 15"

Copies
Original plus five

Weight
15 lb. single part, 12 lb. with 7 lb. carbon multipart

Thickness
0.003" to 0.020"

ENVIRONMENTAL

Operating temperature
50 to 100°F (10 to 38°C)

Operating humidity
10 to 90% RH noncondensing

NOISE LEVEL
55 dBa

COMMUNICATIONS

Code
USASCII

Bit structure
300 to 9600 Baud. 1 start 7 data, 1 parity, 1 stop

Parity structure
Input and output parity. Odd, even and no parity. A received character with incorrect parity will cause a specific character to be printed.

HOW TO ORDER

The Tally T-1612 brings unmatched price/performance to your interactive printing needs. Tally printers are renowned for reliability, simplicity and low cost of ownership. Tally's own nationwide field service organization with resident offices throughout the United States provides backup support for every installation. Worldwide service is available through Tally subsidiaries and distributors.

Call the Tally sales office nearest you for any assistance you require.

TALLY

TALLY CORPORATION
CORPORATE HEADQUARTERS
8301 South 180th Street
Kent, Washington 98031
Telephone: 206-251-5500
Telex: 320-200
Cable Address: Tally, Seattle, WA

TALLY LIMITED, Reading, England, (0734) 580 141
TALLY GmbH, Frankfurt, Germany, 0611-417191
TALLY GESmbH, Vienna, Austria, (0 22 2) 67 26 47
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LITHO IN USA

terminal that you can lay your hands on..

A HANDY CONTROL PANEL

For operator convenience, numerous control functions are located on the front face of the printer for easy accessibility. Also, the critical communications controls have been moved off the keyboard onto the front panel to avoid an erroneous key strike causing lost data. Functions controlled by this panel include power, Baud rate selection, local or off-line operation, half- or full-duplex, automatic line feed, automatic new line and paperout detection.

With the automatic new line (ANL) feature, a line feed is automatically performed when the print head reaches the right margin. This prevents data loss when the data input format does not match the printer format. The automatic line feed (ALF) function, when depressed, creates a line feed whenever the carriage return on the main keyboard is struck or a carriage return is received on the communications line.

PUSH BUTTON CONVENIENCE

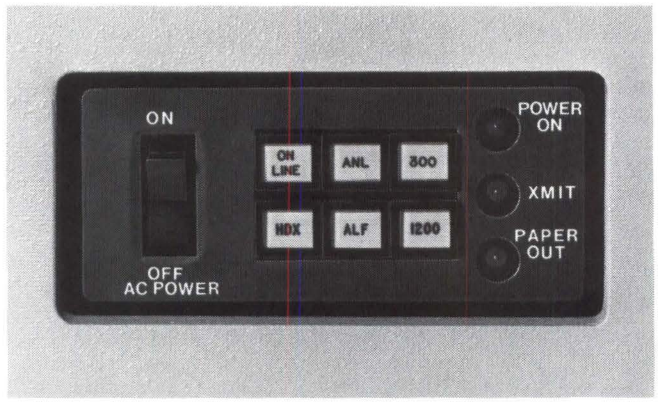
Unlike many terminals, the half-duplex switch is not just a "local copy" switch. It indicates to the microprocessor whether or not it should respond to line turnaround indicators.

The two Baud rate switches allow any of three Baud rates to be selected. 300, 1200, or (if both switches are in the out position) 600 to 9600 as selected on a rotary switch on the rear of the printer.

The power light indicates the application of AC power. The XMIT light indicates that clear to send (CB) is high and informs the operator that his input can be transmitted.

The paperout light indicates that the terminal is out of paper or that a test mode is in process.

MORE FUNCTIONS, MORE FEATURES



CONTROL PANEL

. 42 keyboard programmable functions!

KEYBOARD PROGRAMMING

APPLICATIONS ADAPTABLE

AS FLEXIBLE OR AS SIMPLE AS YOU NEED

Via the keyboard, the operator can select 42 distinct control functions. Also, since the printer can be formatted by incoming data, the operator is not required to make any set-ups on the printer. However, the operator can change the format at any time from the keyboard.

Following is a complete listing of the available functions.

42 Programmable Functions

Formatting.
- Set horizontal tab wherever print head is positioned.
- Set horizontal tabs by address.
- Clear all horizontal tabs.
- Clear a single horizontal tab.
- Set vertical tab wherever form is positioned.
- Set vertical tabs by address.
- Clear all vertical tabs.
- Clear a single vertical tab.
- Set left margin.
- Set right margin.
- Set form length.
- Set top margin by address.
- Set bottom margin by address.
- Set top margin on line where form is positioned.
- Set bottom margin on line where form is positioned.
- Clear bottom of form skip.
- Set LED indicator to show vertical line number.
- Set LED indicator to show horizontal column number.
- Select 6 lines per inch.
- Select 8 lines per inch.
- Select 10 characters per inch.
- Select 12 characters per inch.
- Select 16.5 characters per inch.
- Select standard sized characters.
- Select double width characters.

I/O functions.
- Select local mode.
- Select modem mode.
- Select EOT, ETX or CR line turnaround protocol.
- Select DELETE as a pad character.
- Select DELETE as print buffer erase.
- Enter XON/XOFF.
- Exit XON/XOFF.
- Reprogram HERE IS message.
- Erase the data buffer.
- Select attended operation.
- Select unattended operation.

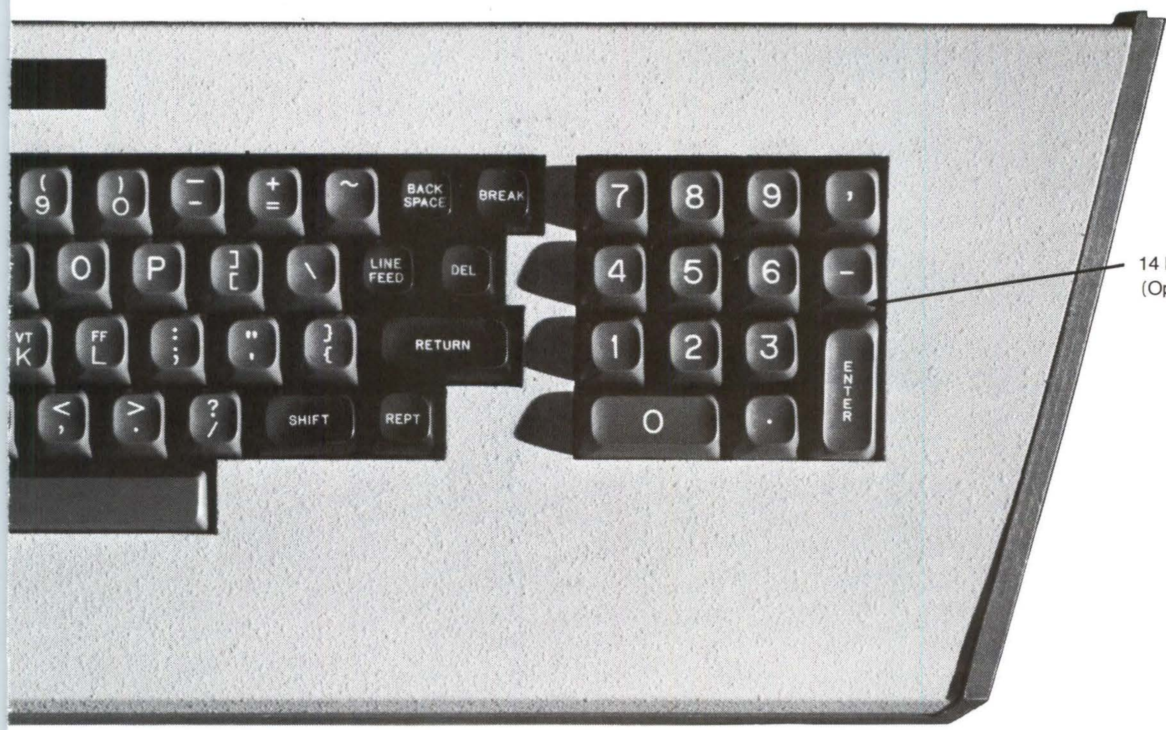
Special functions.
- Select keyboard control.
- Select keyboard and host control.
- Select Special Self-Test mode.
- Select Self-Test mode.
- Clear existing format and reset printer to factory set condition.
- Set customer programmed configuration.

READY TO PLUG IN

For communications compatibility with your system, you can choose from three serial interface configurations—EIA, TTL or 20/60 ma current loop. The printer terminal comes ready to interface to other RS-232 equipped serial devices for local operation or with modem data sets for data communications. The EIA interface is compatible with CCITT recommendation V.24. It is compatible with 103, 113, 202 and 212A Bell modems and the Vadic 3400 modem. The current loop option is a simple internal change-out cable assembly. No special tools are required.

Parity selection is switch controlled by the operator. Optional 75/1200 and 150/1200 split Baud rates are available.

Half-duplex protocols can be selected by the user to operate EOT, ETX or Reverse Channel.



14 KEY NUMERIC PAD (Optional)

PUT A CHANGE OF PACE

IN YOUR PRINTOUT

THE TALLY PRINTER TERMINAL

HAS SIX DIFFERENT

CHARACTER CONFIGURATIONS TO SAVE PAPER

OR DRESS UP YOUR FORMS

BY ENHANCING READABILITY

10, 12, AND 16.5 CHARACTER PER INCH SPACING

IS OPERATOR PROGRAMABLE THROUGH THE KEYBOARD. AND EACH CPI

FORMAT CAN BE SELECTED TO PRINT DOUBLE WIDTH!!

WITH CONDENSED PRINTING, YOU CAN GET 132 COLUMNS ON NARROW PAPER AND 218 COLUMNS ON STANDARD PAPER.

ACTUAL PRINTOUT HAS BEEN REPRODUCED TO SHOW YOU THE POSSIBILITIES--

AND TO POINT OUT TALLY'S OUTSTANDING PRINT QUALITY

A 7X7 HALF SPACE MATRIX FONT DELIVERS CLEAN, CRISP CHARACTERS WITH

HIGH LEGIBILITY FOR

EASY READABILITY.

THE PRINTER FEATURES DUAL TRACTOR ENGAGEMENT ABOVE AND BELOW

THE PRINT LINE TO HOLD THE PAPER PRECISELY IN PLACE AND DELIVER

FAST PAPER ADVANCEMENT. REGISTRATION NEVER WAVERS.

TALLY
TALLY
TALLY
TALLY
TALLY
TALLY

WITH SO MUCH FLEXIBILITY AT YOUR FINGERTIPS, ITS EASY TO SEE

THAT YOUR BEST BUY IS THE TALLY T-1612 PRINTER TERMINAL.

communications line codes is provided, including ASCII, EBCDIC, and Baudot. The controller also provides 15 levels of priority interrupts and interfaces to control various peripheral devices.

Circle 414 on Inquiry Card

Disc-Based Systems Added to Commercial Minicomputer Line

Three additional models in the DS 990 family of disc-based minicomputer systems offer extensive file management capabilities that support multiple interactive users in a multilanguage environment. Based on the model 990/10 processor and the enhanced DX10 operating system, Texas Instruments Inc, Digital Systems Div, PO Box 1444, Houston, TX 77001 has emphasized systems-level design and support in the models 4, 6, and 8.

Model 4 serves as a small multistation full-function software development system or a medium-scale application system. It includes a 128k-byte processor, 1920-char model 911 video display terminal, 5M-byte fixed disc, and 5M-byte removable cartridge disc drive. Model 6, which offers more disc capability for larger data base applications, includes 128k-byte processor, 911 terminal, and two 25M-byte removable pack disc drives. Model 8 accommodates even larger data bases with two 50M-byte disc drives.

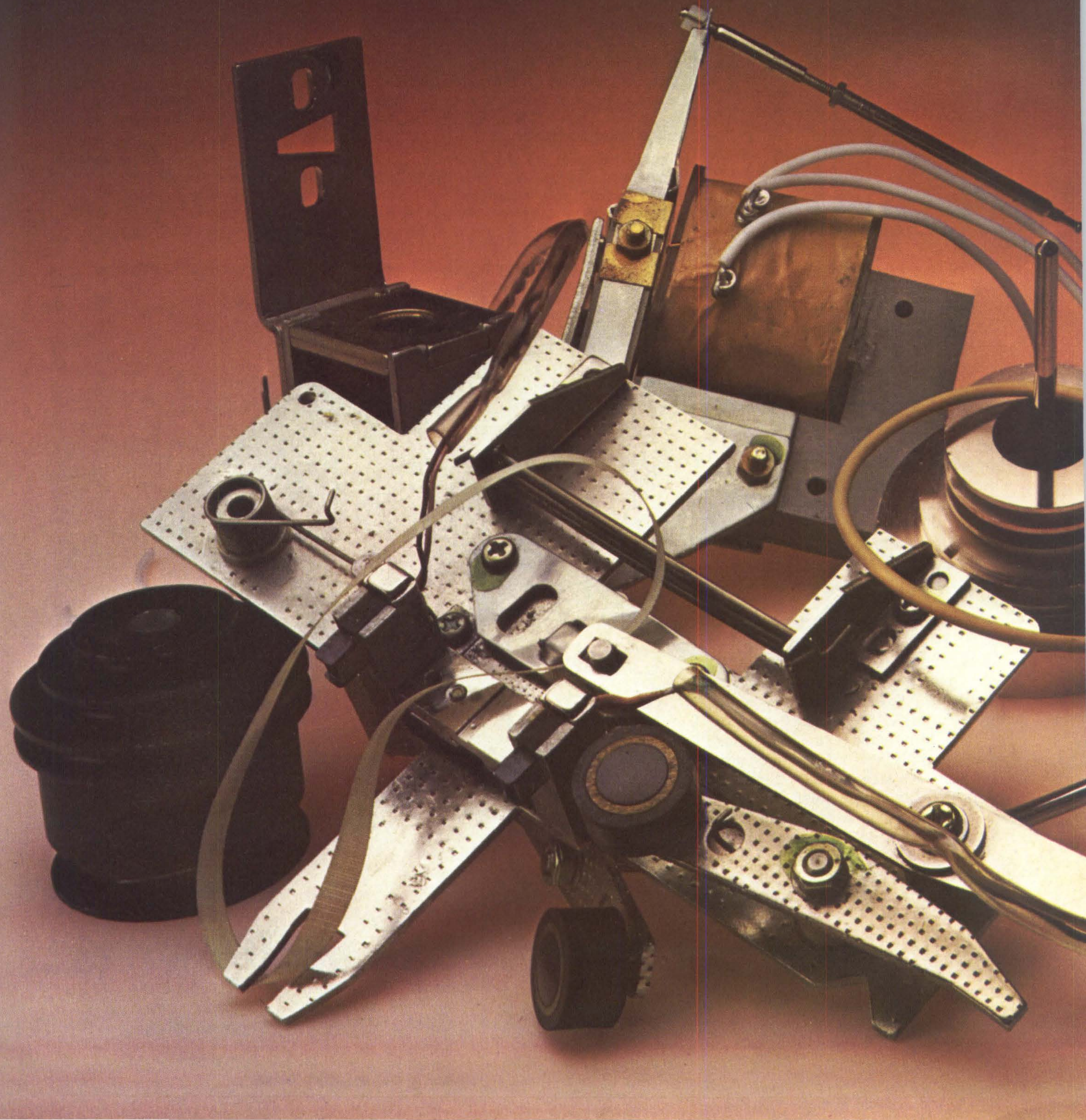
The systems offer software support and utilities for business applications, including COBOL, Sort/Merge, BASIC, and Business BASIC. FORTRAN IV with ISA extension is also available. The DX10 operating system contains file management features including multikey indexed file support. Software development facilities include a macroassembler, interactive source editor, and overlay supported link editor.

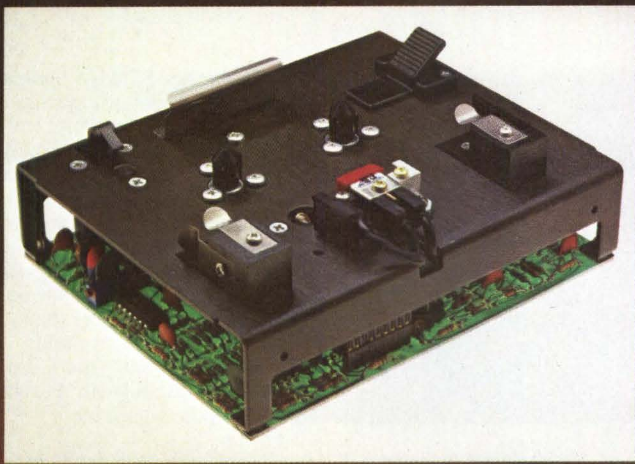
Standard options for the system include additional memory up to 2048k bytes, and additional 911 terminals and disc drives as well as diskette units. Model 810 impact printer, 2230 and 2260 printers, 979A 9-track magnetic tape drive, and communications options are also available.

Circle 415 on Inquiry Card

We looked at all the things you hate about cassettes.

And threw them out.



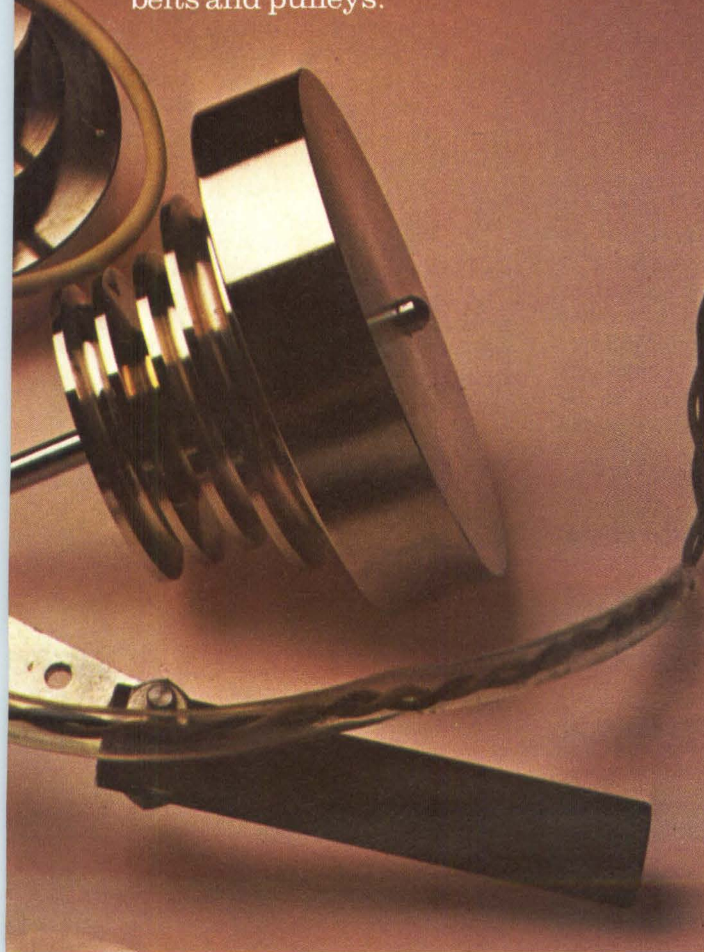


The remarkably simple MFE cassette drives make cassettes a viable, reliable storage medium.

Those innocent-looking little pieces of plastic and metal are responsible for just about all the problems you've come to expect from cassettes.

That's why we don't use them.

No finicky solenoids and clutches. No whirling pinch rollers, capstans, belts and pulleys.



MFE cassette drives have only two moving parts. Which means there's practically nothing to go wrong. The result is an impressive 15,000 hour MTBF.

Data Integrity. Our revolutionary tape transport system also greatly improves data integrity. Patented servo-controlled reel-to-reel tape handling results in a constant tape speed within ±1% and a low bit-to-bit jitter of ±3%.

We even include a RAW head as a standard feature. Because read-after-write checking is the best way to guarantee data integrity.

Here are a few more reasons MFE cassette drives will change your thinking about cassettes:

Widest speed range. Continuously variable tape speed from 2-120 ips.

Highest data transfer rate. Up to 32K bps ANSI/ECMA compatible.

More options. Both serial and parallel I/O.

Low power requirements. Only ±5V at 5W total power consumption.

We even have a model that's qualified for hostile environments. It operates at temperatures from −40°C to +70°C.

The MFE 250B cassette drive. If you hate cassettes because they're cranky and unreliable, you need another reason.

For details, contact MFE, Keewaydin Drive, Salem, New Hampshire 03079, Tel. 603-893-1921/TWX 710-366-1887/ TELEX 94-7477.

Europe: MFE Products SA, Vevey, Switzerland, Tel. 021 52.80.40/TELEX 26238.

MFE

CIRCLE 20 ON INQUIRY CARD

Modular Automatic Test Equipment System May Produce Savings

A modular automatic test equipment system (MATE) for use in maintenance of aircraft is expected to provide significant savings in equipment, maintenance, and operating costs. Requests for proposals for studies, analysis, and hardware for the system have been issued by the United States Air Force, Aeronautical Systems Div at Wright-Patterson AFB, Ohio.

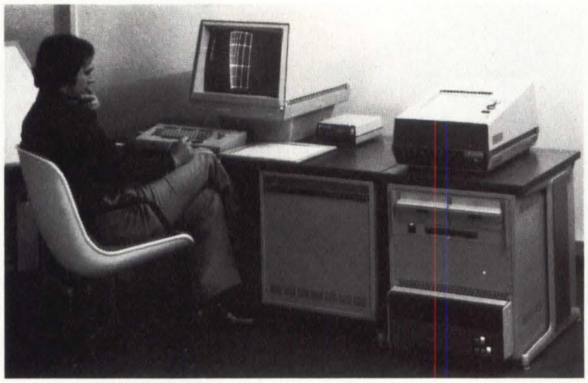
The system, intended for use in future maintenance work with all types of aircraft, is the first development of automated test equipment to be independent of a specific aircraft. Currently, separate test equipment is developed and purchased for each aircraft at each level of maintenance—field, organizational, and depot.

Under the MATE program, interchangeable or modular parts (hardware and software) to a single system would be procurred. This one system would then be used to perform maintenance checks on all types of aircraft at any level of maintenance. The pieces used in assembling the system would depend on the aircraft and avionics system to be tested. Plans are to test radar, radio, inertial navigation, and electronic countermeasures equipment using the system.

System Reduces Cost of Building Models for Finite Element Analysis

A standalone finite element modeling system, FEM 181 promises to significantly reduce the cost of building models for finite element analysis by cutting the time required by up to 70% and eliminating timeshare costs. The integrated, interactive graphic system allows models to be created fast and accurately. Since models are created offline, host-computer timeshare costs are nonexistent. A universal bulk data formatter provides compatibility with existing analysis systems as well as proprietary analysis programs.

Tektronix, Inc, Information Display Group, PO Box 500, Beaverton, OR 97077 formulated the basic system with a 19" (48-cm) combination storage/refresh CRT display, terminal keyboard, 10M-byte disc unit, hardcopy unit, and finite element modeling software. An 11 x 11" (27.9 x 27.9-cm) tablet is optional.



Tektronix' FEM181 finite element modeling system includes 19" (48-cm) combination storage-refresh CRT display, terminal keyboard, 30 x 40" (76 x 101.6 cm) graphic tablet, disc memory, hardcopy unit, and finite element modeling software. Models created using this standalone system can be verified, formatted for analysis, and then transferred in bulk to the host analysis computer

Operating independently of the host computer, the system allows the structural analyst to create a model, verify its accuracy, and format the model data into a form compatible with the host analysis system's input requirements. Formatted data can then be transferred in bulk to the host computer.

Initial coordinate data can be entered from keyboard, graphic tablet, or down loaded from the host computer. A 30 x 40" (76 x 101-cm) graphic tablet is available, allowing nodes to be digitized directly from engineering drawings. The data loader module permits the data base for an existing model to be transferred from the host to disc memory, and then examined and edited with modeling system software.

The model is shown in three dimensions on the display screen as it is created. When defining node coordinates and elements, the analyst has virtually instantaneous interaction with the display. Copy commands in the system allow a model to be built quickly when only a few initial nodes have been defined.

Verification and inspection of the model is facilitated using system features which allow 3-dimensional rotations, erase and redisplay in a new orientation, and zoom in on specific sections. Z-plane clipping omits the front or rear portion of a model to eliminate confusion.

When an accurate model has been achieved, the bulk data formatter module is used to compile and format the node, element, and property data for processing by the host finite element analysis system in whatever card image format is required. Model data and other system data are then transferred in bulk to the host system for analysis.

Circle 416 on Inquiry Card

Mark Sense Cards Primary Input Medium for Instructional Computer

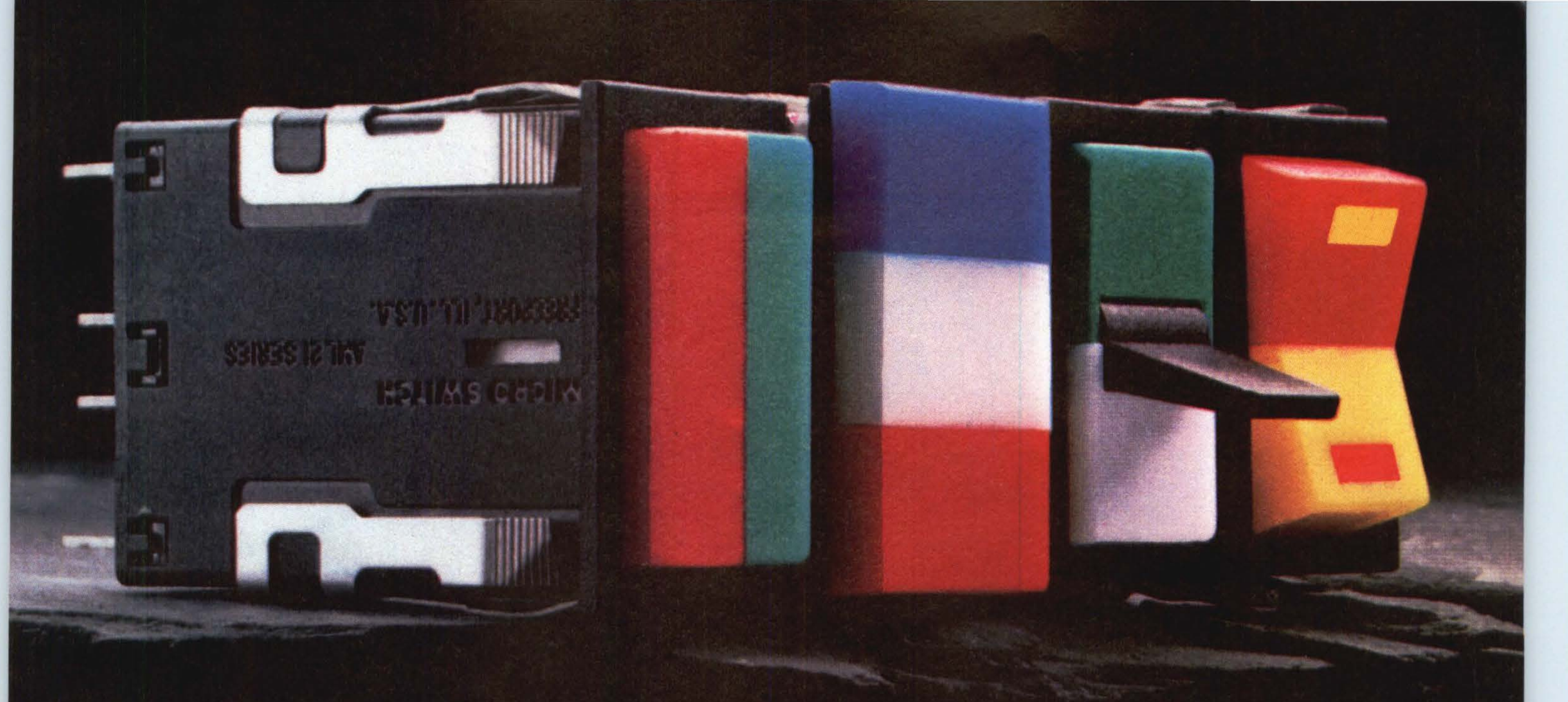
A compact batch-processing system that uses mark sense cards as its primary input medium to extend computer access to large numbers of students, MSB-11 (Mark Sense Batch-11) supports both BASIC and FORTRAN IV programming languages. The system is available from Digital Equipment Corp, Education Products Group, Maynard, MA 01754 at a cost approximately the same as a 5-user timesharing system.

The PDP-11/04 based system with 32k bytes of semiconductor memory and a dual floppy unit for program and data storage is housed in a 4-ft (1.2-m) high cabinet. Input/output devices include an 180-char/s line printer, LA36 DECwriter II console terminal, and the CMS-11K mark sense card reader.

The desktop 250-card/min reader enables the system to accept 40-col punched or marked cards coded in BASIC or FORTRAN IV. Programs are processed in a single batch stream and are stored on the 512k-byte disc unit, or are printed out on the LA180 matrix printer.

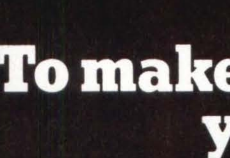
Price of the MSB-11 with a subset of the RT-11 operating system and the BASIC language is $21,460. With a minimum expansion, the system can be configured for scheduled use as either a timesharing or batch system.

Circle 417 on Inquiry Card



To make a complete line of pushbutton controls, you need more than pushbuttons.

Pushbuttons from MICRO SWITCH's AML (Advanced Manual Line) have always been attractive to designers. Because they look so good.



And because they're so easy to mount and wire.

But now, the AML series is even more appealing. Because now there's a variety of rocker and paddle switches to choose from, including dual lamp and dual color. Which means now you can perform just about any function with a harmonious display. You don't have to compromise.

AML controls also look appealing to the people who have to do the wiring. All are designed with the same depth for single level termination, regardless of switch or terminal type.

There's easy snap-in mounting from the front, PC board mounting or subpanel mounting using individual, strip or matrix hardware.

Which means mounting is simpler. Wiring is simpler. Engineering time is reduced. And total installed cost is lower.

Plus, they offer solid state, electronic control or power switching in the same size housing. All AML devices are designed to meet international, UL and CSA standards.

Displays include split screen, hidden color, and a unique three-segment lens cap indicator. The choice of lamps includes T-1¾ wedge base, neon and LED.

AML has it all —pushbuttons, indicators, and now, paddles and rockers. But to see how good-looking AML really is, contact us for a personal demonstration.

MICRO SWITCH will provide you with field engineers for application assistance and a network of authorized distributors for local availability. Write us for details or call 815/235-6600.

MICRO SWITCH products are available worldwide through Honeywell International.

MICRO SWITCH

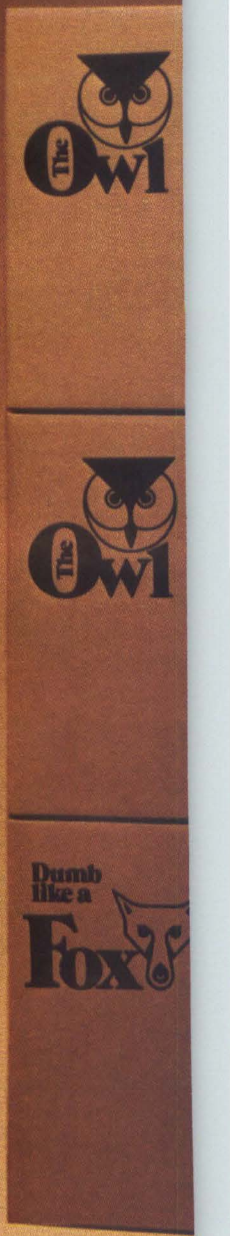
FREEPORT, ILLINOIS 61032

A DIVISION OF HONEYWELL

Circle 21 for data.

In 7 months, I placed 5000 foxes and owls in good homes.

–Jim Folts, Vice President, Terminals Division



Seven months ago, Perkin-Elmer introduced two new CRT terminals. The Model 1100, a very simple terminal that's dumb-like-a-fox for $907.* And the Model 1200, a smart editing terminal known as The Owl for $1383.*

Right away, the big wheels in the terminals business gave us plenty of encouragement. "Who needs another inexpensive CRT?" they said.

"Every OEM and system builder who knows true value," we said.

And, sure enough, smart OEMs and system builders ordered 5000 Perkin-Elmer terminals and really started sales rolling.

Now it's Pussycats.

But, that's only the beginning.

This month we're unleashing a new thermal printer called The Pussycat–a 100 cps CRT page printer that should make hard copy a lot more affordable and send our competition running for cover. Especially when they hear we're tooling up for thousands of Pussycats the first year. Turn the page for a closer look. Then call your nearest Perkin-Elmer Data Systems office.

And while you're at it, get more information on the rest of our menagerie. The Model 1100 Terminal that's dumb-like-a-fox and The Owl, our Model 1200 Editing Terminal.

Perkin-Elmer products. You'll become attached to them in no time.

PERKIN-ELMER DATA SYSTEMS | TERMINALS DIVISION

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(214) 234-8880	Dallas, TX	539-2260	Paris, France
(714) 544-9093	Los Angeles, CA	753-34511	Slough, Berkshire, UK
(201) 229-4040	Oceanport, NJ	089-753081	Germany
(408) 249-5540	San Francisco, CA	2200949	Singapore
		031/450/160	Frolunda, Sweden

*Quantity 75.

CIRCLE 22 ON INQUIRY CARD


Dumb like a Fox
The Owl
Dumb like a Fox
The Owl

Display Terminal Saves Time and Minimizes Text Processing Errors

A microprogrammed video display terminal, the Delta 4300E incorporates 4k-char memory and offers flexibility in manipulating data on the screen and in memory. Delta Data Systems Corp, Woodhaven Industrial Pk, Cornwells Heights, PA 19020 designed the terminal specifically to add convenience and minimize errors in text processing applications.

Text manipulation features include automatic word wrap, ragged right sentence and paragraph justification, and automatic justification of new insertions. Automatic search modes are search for word or word string, search and replace word or word string, search and replace upon request, and search and delete word or word string.

Operator errors are minimized by ability to move/copy/delete any defined text from memory, automatic carriage return, and a memory preservation feature which prevents loss of data by signaling when a character is added to a full memory.

Display provides a full 128 char u/lc character set, scroll up or down, full tab/clear control, end of data tab, and protected text control. A paging feature permits display of all characters in memory, and permits the user to recover information that has been rolled off the screen.

Communication speeds up to 9600 baud are possible. An optional serial printer port allows hardcopy records of material on the screen to be obtained.

Circle 418 on Inquiry Card

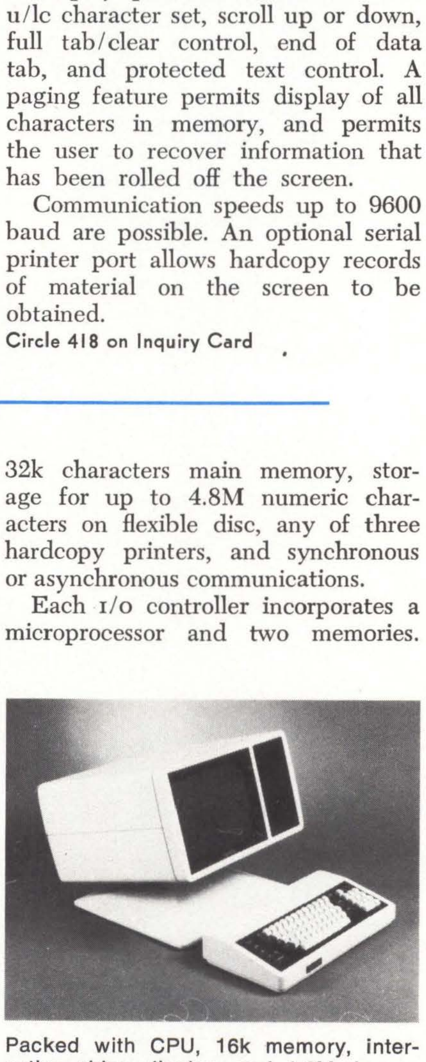
Compact Business System Incorporates Disc Unit And Video Display

Incorporating flexible disc media and expanded memory into a compact, dual-component system, the model 210 business computer serves as a standalone computer for entry level use or as a host or satellite processor in a distributed computing network. The system was designed by Qantel Corp, 3525 Breakwater Ave, Hayward, CA 94545 to perform all computing functions of larger units and for 100% compatibility with software for the company's larger systems.

In basic configuration the unit includes CPU, 16k bytes of user-dedicated main memory, interactive video display, and a flexible disc drive with storage capacity for 1.2M alphanumeric or 2.4M numeric characters of data. Expansion space is provided to accommodate communications, increased memory and storage, and additional plug-in I/O devices. All this hardware is packaged in the video component. The separate keyboard incorporates alpha and numeric pads and connects to the main computer with a 4′ (1.2-m) cable.

System expansion is accomplished by addition of plug-in circuit boards. Fully expanded, the system supports 32k characters main memory, storage for up to 4.8M numeric characters on flexible disc, any of three hardcopy printers, and synchronous or asynchronous communications.

Each I/O controller incorporates a microprocessor and two memories.



Packed with CPU, 16k memory, interactive video display, and 1.2M-character capacity floppy disc, Qantel's model 210 serves as standalone or satellite processor

This, in addition to increasing computer power, enhances efficiency by enabling the main computer to perform multiple jobs simultaneously. An operator can enter data at the terminal in foreground mode while printing reports in background mode.

Circle 419 on Inquiry Card

Storage Capacity and Communications Added to File Management System

Enhancements to the System 5000 quadruple disc storage capacity and add remote batch communications capability to permit its use in distributed computing networks. Disc units introduced by Inforex, Inc, 21 North Ave, Burlington, MA 01803 for use with the system are the 62M-byte model 5303 and the 235M-byte 5304. Up to four drives of either density can attach to a terminal control unit, providing maximum capacities of 940M bytes. Under software release 506, System 5000 display terminals can communicate with IBM 2780/3780 equipment or other equipment capable of emulating either IBM remote batch protocol.

In addition to remote batch communications capability, the software features dynamic disc allocation, and permits users to build index sequential, as well as simple sequential, files. With system enhancements, a user can access any of the 11M records within 80-char record files in less than 3 s. Release 506 allows files stored on disc in the System 5000 to be transmitted at speeds of up to 9600 bits/s, with a single keystroke command, to a mainframe or any device supporting 2780/3780 protocol.

Hardware enhancements for use with the software include a microprocessor-based binary synchronous communications adapter, which offloads communications tasks from the control unit; and a memory expansion unit, which permits remote batch communication to occur concurrently with online file management.

The adapter handles all communications-related tasks, maintaining throughput during file management by relieving the control unit of the communications burden. Throughput is increased by permitting concurrent communications and online file management. The memory expander feature, which adds 64k words of main memory to the terminal control unit, improves terminal response times in large configurations, especially where a number of procedural steps are performed on each record.

Circle 420 on Inquiry Card

Smile, when you say pussycat!

Pussycat. Perkin-Elmer's $795,* 100 cps CRT Page Printer.

Pussycat. That's what we call our new 100 cps thermal printer, The Model 650 CRT Page Printer.

Pussycat. People who make 30 cps printers will think it's an incredibly funny name. Until they realize our meek little Model 650 is half the price of their machines, three times faster, and a whole lot quieter and easier to maintain.

In quantity 75, the Model 650 is only $795 each. Which means you can buy a CRT and a Pussycat printer for what you're now paying for a printing terminal alone.

The Model 650 is fast. It prints an entire screen full of characters in 20 seconds. And, because it's the only printer in its class with a full-screen buffer, the Model 650 can free the CRT in 2 seconds or less. So the operator can go back to work while the printer is printing.

The Model 650 connects to any CRT terminal with an RS232 port – a Perkin-Elmer terminal or, perish the thought, someone else's. No need to replace existing hardware or software.

And no need to worry about noise or maintenance. The Model 650 has only one moving part – the platen.

Check out The Pussycat from Perkin-Elmer. It's a great little printer at a very reasonable price.

And, if you're one of our competitors…Smile, when you say pussycat!

*Quantity 75.

CIRCLE 23 ON INQUIRY CARD

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Before the board meets
to discuss rising
service costs,
call Tektronix
TEKTRONIX
TEKTRONIX 851 DIGITAL TESTER
CHANNEL A
CHANNEL B
CHANNEL C
FUNCTION
RANGE
SLOPE
POS
NEG
POWER
DMM

Our new 851 Digital Tester can give you the leverage to control those costs.

Managing a service organization is no bed of roses. It's big business. And it's continually getting more costly. Customer engineers, spare parts inventories, training, designing for serviceability, documentation, and instrumentation all contribute to these spiraling costs. Because service is so important to the success of a company, you need to identify those elements which have the greatest leverage for your service organization.

Consider instrumentation.

Typically it is less than 5% of your overall service budget. Yet the right test instrument can have a tremendous impact on the other 95%... training, salaries, inventory requirements, travel and backup.

That's why we built the new 851 Digital Tester. It's a synergistic, new service instrument that combines the functions of many instruments in one portable package.

We know that the task of servicing digital equipment is threatening to outrun existing service resources. Your first-line customer engineers are being required to make more intricate measurements on increasingly complex systems.

With the new 851, your first-line customer engineer will be able to solve more problems in less time on the first call. That's because he can rely on the measurement and interpretation capabilities of the 851 to perform complicated tests in the field. Not only does this save you the expense of calling in the back-up engineer, but it also gives your first-line engineer the satisfaction of solving more problems on the first call.

A new concept in service instruments.

Your inventory of service instruments probably includes oscilloscopes, DMM's, counters, timers, logic probes, thermometers, and some special purpose test equipment.

A bench full of test equipment is a great resource for your customer engineer to rely on... as long as he doesn't have to travel much.

But imagine a self-contained service instrument that weighs only 13 pounds and makes most of those same measurements.

That's our new 851 Digital Tester.

The power of the 851 lies in the fact that even though this one instrument makes the measurements of a variety of test gear, it is also easy to use.

With just one turn of the knob you can dial 22 different functions to make a wide range of system measurements and tests.

851 Digital Tester Functions

MEASUREMENTS		SIGNAL ANALYSIS	SELF TEST
VOLTAGE PEAK (25 ns to 25 ms) AC DC POWER LINE INPUT LOGIC THRESHOLDS **RESISTANCE (0.1Ω to 50 MΩ)**	**TEMPERATURE** **TIME (20 ns to 10 s)** PERIOD FREQUENCY PULSE WIDTH INTERVAL COINCIDENCE TRANSITION	**LOGIC STATE INDICATORS** HI, LO, INVALID, ACTIVE **% DUTY FACTOR** **COUNTING** FREQUENCY RATIO EVENTS BETWEEN START AND STOP PULSES TRANSITIONS BETWEEN START AND STOP PULSES TOTALIZE	**TEST SIGNAL** EXERCISE FUNCTIONS ADJUST PROBE **READOUT TEST**

It's easy. Just dial a function, probe the circuit being examined, and read the results directly from the autoranging LED display.

And what about product support? With Tektronix, it's worldwide.

Wherever in the world your service organization goes, Tektronix is with you all the way. Service personnel at 46 Tektronix Service Centers in the U.S. as well as service personnel in 50 other countries back our products.

Put the 851 to work in your digital service environment.

The measurement capabilities of the 851 make it particularly useful for sevicing computer peripherals, small business systems, and industrial control equipment.

We had you in mind when we designed the 851 Digital Tester.

Detailed specifications, application notes and a color brochure are available for your information. Please contact your Tektronix Field Engineer. Or write Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077. In Europe write Tektronix Limited, P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

New concepts in digital service

Tektronix
COMMITTED TO EXCELLENCE

For technical data, circle 24 on Inquiry Card.
For a demonstration, circle 25 on Inquiry Card.

High Density, 28-Track Digital Tape Recorder Offers High Throughput

A 28-track, high density, digital magnetic tape recorder, the HI-D™ system offers a wide dynamic range at high throughput rates with high tape packing densities and data capacities, meeting demands for increased resolution and the need to store increasingly large quantities of information. By recording data in digital form, the need to translate from analog to digital for subsequent data processing is eliminated, increasing the usefulness for real-time uses.

General specifications of the HI-D system, introduced by Bell & Howell Co, Datatape Div, 300 Sierra Madre Villa Ave, Pasadena, CA 91109, include parallel entry and exit of data at data rates to 92M bits/s; TTL-compatible, single-ended or differential input and output of data and coincident clock; and the ability to handle long strings of 0s or 1s. Parallel E-NRZ™ (enhanced non-return to zero) electronics are capable of handling digital data at up to 3.3M bits/s per channel. A minimum of four channels and a maximum of seven or 14 channels on 0.5" (1.27-cm) tape and 14 or 28 channels on 1" (2.54-cm) tape can be accommodated.

The enhanced NRZ recording scheme is a variation of the basic non-return to zero code that is particularly useful for high density recording. E-NRZ takes advantage of the basic code's high packing density capability and overcomes the low frequency limitation by insuring a data level transition using data enhancement techniques. Incoming data are first compressed in time base, then the enhancement bit is inserted. When data are reproduced, the enhancement bit is removed and the original data stream is reconstructed.

Using the E-NRZ technique with a tape speed of 120 in/s (305 cm/s), a nominal input/output data rate of 3300k bits/s per track is achieved with a bit error rate of 1 in 10^6 for 28-track operation. Recording with tape speed of 1.875 in (4.76 cm)/s and 51.5k bits/s I/O data rate per track results in a bit error rate of 1 in 10^5 for 28-track operation.

The system encoder provides an input rise/fall time of 100-ns maximum. The E-NRZ data are augmented by a 40-bit deskewing sync word used to align the output skewing buffers, which consist of four TMS 3120 shift registers with storage capacity for 1280 bits (1120 data bits and 160 enhancement bits). Data rate is automatic with tape speed selection for data rate ranges specified for 1.875 to 120 in (4.76 to 304.8 cm)/s.

Reproduce/bit sync/decoder provides amplitude and phase equalization, synchronizes and regenerates the clock from data, and decodes data to remove parity bit, deskew sync information, and bit inversion to restore data. For setup, troubleshooting, and verification of system performance during operation, record level, reproduce level, bit error rate, and data rate monitor outputs are wired from the decoder to a multipin connector on the back of the amplifier mounting assembly. □

Circle 421 on Inquiry Card

From a single CPU board

to a half million word super computer

That's the selection you get from ROLM's AN/UYK-19 family. It's the most complete line of Mil-Spec computers in the industry. And every piece is backed by extensive, updated, upward compatible software.

Delivery? 30 days or less because they're all standard products in continuous production. Plus they follow a modular concept for interchangeability, compatibility and upgrading.

Rolm completes the package with full nomenclature and an integrated line of both military and commercial peripherals.

In just seven years we've been able to put together a family plan that lowers your programing costs, reduces hardware costs, cuts out your risk and gives you quicker reaction time.

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CIRCLE 28 ON INQUIRY CARD

TOUGH COMPETITION:

The complete 125 ips package—beats anything in its class now moving tape.

Strong words. For strong capabilities, wrapped up in a strong new look. A totally new design in vacuum column drives houses the first *complete* high-speed package in the field.

The T1000 Series from Pertec.

No more compromising. No more shopping around. We've got it all. Together. Just for starters: 125 ips. Plus GCR. Plus auto-thread and auto-load.

You'll find everything you need to feed your powerful mini systems, in a T1000 configuration. These are not only our most advanced, most flexible tape transports produced today—they're built by Pertec to fit tomorrow's data processing applications to a T.

Ask for 6250 bpi GCR. In addition to dual NRZI/PE modes available, T1000 drives offer OEMs the only Group-Coded Recording at 125 ips—*with* a vacuum capstan to protect high-speed operations with a friction-free instant grip, for safer fast starts and stops.

Ask for operational convenience. T1000 makes life easier for your customers: *with* cartridge auto-load, automatic threading, and automatic load point seek. *With* a built-in daisy-chain capability. *With* front access to all electronics to simplify maintenance.

Ask for internal data formatting. Intelligence can be built into T1000 NRZI/PE configurations (as well as our tension-arm 7″ reel FT7000 and 10½″ reel FT8000, and our 37.5-to-75 ips FT9000 vacuum column series). Pertec is now installing our Microformatter inside these units, on order, to simplify interfacing, and reduce system costs.

Now complete the picture: ask for Pertec. Making it still tougher on the competition, our broad line of tape transports covers the full spectrum of OEM requirements. With the same total commitment backing T1000: Pertec, the world's largest independent manufacturer of peripheral equipment, backs *all* its products with the international sales, support and service operations of Pertec Computer Corporation.

There's a Pertec service office near you... and your customer. With emergency assistance on-call, on a 24-hour 7-day basis, through our toll-free 800 line.

☐ Please send complete details on the Pertec T1000 Tape Transport Series.
☐ Send pricing information as indicated on the RFQ below (no obligation or cost).

Request for Quote

T1000 Model #	Data Format	Data Density (bpi)	Tape Velocity (ips)	Quantity Required	Date Wanted	Send Specs Only
T1640-98	PE/NRZI	1600/800	75-125			
T1940-96	GCR/PE	6250/1600	75-125			
FT1640-98 w/internal formatter	PE/NRZI	1600/800	75/125			

Name____________________

Title__________ Phone__________ Ext______

Please attach coupon/RFQ to company letterhead and return to Pertec, 9600 Irondale Avenue, Chatsworth, CA 91311.

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PCC PERTEC

a division of Pertec Computer Corporation

CIRCLE 29 ON INQUIRY CARD

Brooklyn Firefighting Units Respond to Computer-Aided Dispatching System

Four hundred and fifty thousand alarms a year—an average of nearly one alarm each minute. When those figures relate to incidents reported to the fire department in a major city, the problem of apparatus distribution becomes gargantuan and seemingly almost totally unwieldy—particularly if nearly half of the alarms are false, tying up equipment that is needed elsewhere.

New York City's fire department—more commonly designated FDNY—consists of over 350 pieces of apparatus and more than 10,000 firefighters. Until recently, deployment and control of all equipment and personnel in all five of New York City's boroughs was handled manually by human dispatchers.

Under this "manual" system, a fire alarm for a particular borough—usually reported by street alarm box or telephone—is transmitted to a central communications office in that borough, where a dispatcher decides how many and which units to send in response. The dispatcher must assume all alarms to be "real"; even an alarm that the dispatcher believes to be false requires a response of at least two pieces of equipment: one engine or pumper and one ladder. In addition, these "real" alarms do not all concern serious or structural fires. The problem being reported may be a rubbish can fire, a person stranded on an elevator, smoke in a vent, or food burning on a stove.

The dispatcher must know the availability of backup apparatus in case a working fire requires additional firefighting units. No section of the city can be left unprotected. If an area is stripped of fire protection, equipment must be reassigned from another area as cover.

The variety of demands for fire department service and the rapidly increasing rates of alarm activity—30,000 in 1925; 60,000 in 1945; 130,000 in 1965; 300,000, in 1973; 400,000 in 1975; and 450,000 in 1976—forced FDNY to reassess its policies. It had become apparent that present procedures for response and deployment would soon become inadequate, that more sophisticated methods were required for predicting alarm incidents and for assigning units to each alarm.

Brooklyn MICS: The First Step

In February of this year, the borough of Brooklyn—in itself the fourth largest city in the United States—placed online a Management Information and Control System (MICS) that provides computer assistance to that borough's fire department communications facility. Only the Brooklyn MICS is computer assisted; all other boroughs perform their respective dispatching functions manually.

MICS is capable of handling three alarms each minute with 1-s CRT response time—almost four times the 1976 incidence rate. A complete cycle including receipt of alarm, selection of equipment, and relay of alarm and assignments to the watch desk is performed in 40 s or less.

The Brooklyn MICS, contracted for with Bradford National Corp, 1700 Broadway, New York City in March 1975, was built and installed in 18 months and placed online five months later. It is a dual computer system with dual microprocessor backup in the most critical area.

Two Digital Equipment Corp PDP-11/45 computers are chief components of the assignment and dispatch system. One computer is constantly online to a dual access disc subsystem and, via a line switch, to a display/fallback system as well as various input/output systems (Fig 1).

The computers constantly maintain a channel-to-channel link for interprocessor communications. If the online computer fails, the standby unit immediately assumes its duties with full access to all system components.

Similarly, a pair of Intel 8080 microprocessor-based controllers—included in the critical status recording subsystem as backup for the larger computers if both of those units fail—have online and standby duties. In the very unlikely event that all four processors fail, the status recording subsystem reverts to manual operation.

The online PDP-11/45 processes alarms received from the old mechanical street boxes, from newer electronic street boxes that permit voice communication as well as transmission of digital signals, and via direct telephone contact. Based on company availability and programmed rules, the computer determines the quickest and most suitable response to each alarm and displays each proposed unit dispatch assignment on a CRT terminal for the dispatcher's approval or modification according to personal knowledge of the situation. Once the dispatcher agrees with the computer's choice, he validates the assignment by pressing a button which allows the computer to send a message

The new Fluke 3041A programming station with the 3040A Logictester™ for μP boards you haven't even designed yet!

Check one: Fluke's ☐#1 ☐#3 in digital board testers.

Correct on both counts.

More Fluke logic test systems are in production and service applications than anyone's. And more are shipped each month. Two ways of saying we're #1.

And, our customers spent less getting us there than they could have with anyone else. That makes us #3 on average cost.

But low front-end cost is only the start. You'll get lower programming, training and start-up costs than you thought possible. The highest test rates in the business, too, because boards run at rated speeds, including dynamic μP boards at multi-MHz rates.

More importantly, you'll test with confidence. If your board passes our tester, it'll work in your system. It's that simple. And reliable; more Fluke systems sold prove it.

The heart of our 3040A is a new merged sequence technique which lets you mix your test codes with automatically-generated sequences. And the best simulator around: your own known-good board. And dynamic LSI/fault isolation, automatic, manual or both!

Fluke hasn't forgotten about the bad boards either. After the tester nails the bad ones, we automate the troubleshooting. Our Autotrack™ computer-guided troubleshooting leads the operator to the fault. With the new 3041A programming station, you describe the board onto a floppy disk and the 3040A does the rest.

The **3040A**, with up to 240-pin capability, is $60,000 to $95,000*, depending on option configuration.

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Call (415) 965-0350, collect. Ask for the complete story on our high-ranking Logictester™ family, or the location of the closest Fluke office. Or, write: Fluke Trendar, a subsidiary of John Fluke Mfg. Co., Inc., 630 Clyde Ave., Mountain View, CA 94043.

In Europe, write: Fluke (Nederland) B.V., P.O. Box 5053, Tilburg, The Netherlands. Phone: (013) 673-973. Telex: 52237.

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ComputerAutomation's NAKED MINI® 4/10 is the most exciting spread we've ever dished up: a high-speed, versatile, 16-bit processor, up to 4K words of RAM/PROM memory, and four distributed I/O channels. All on a single board. And this powerful, multi-register minicomputer sells for micro prices.

Value, however, is a lot of things. Such as performance, versatility, and a faster, lower cost way of getting a product to market. For the 4/10, your real savings just begin to start with the sale price. Its large instruction set (including multiply/divide as standard) pays off with exceptional programming versatility, faster development, less memory used. Options include floating-point instructions and double-register shifts.

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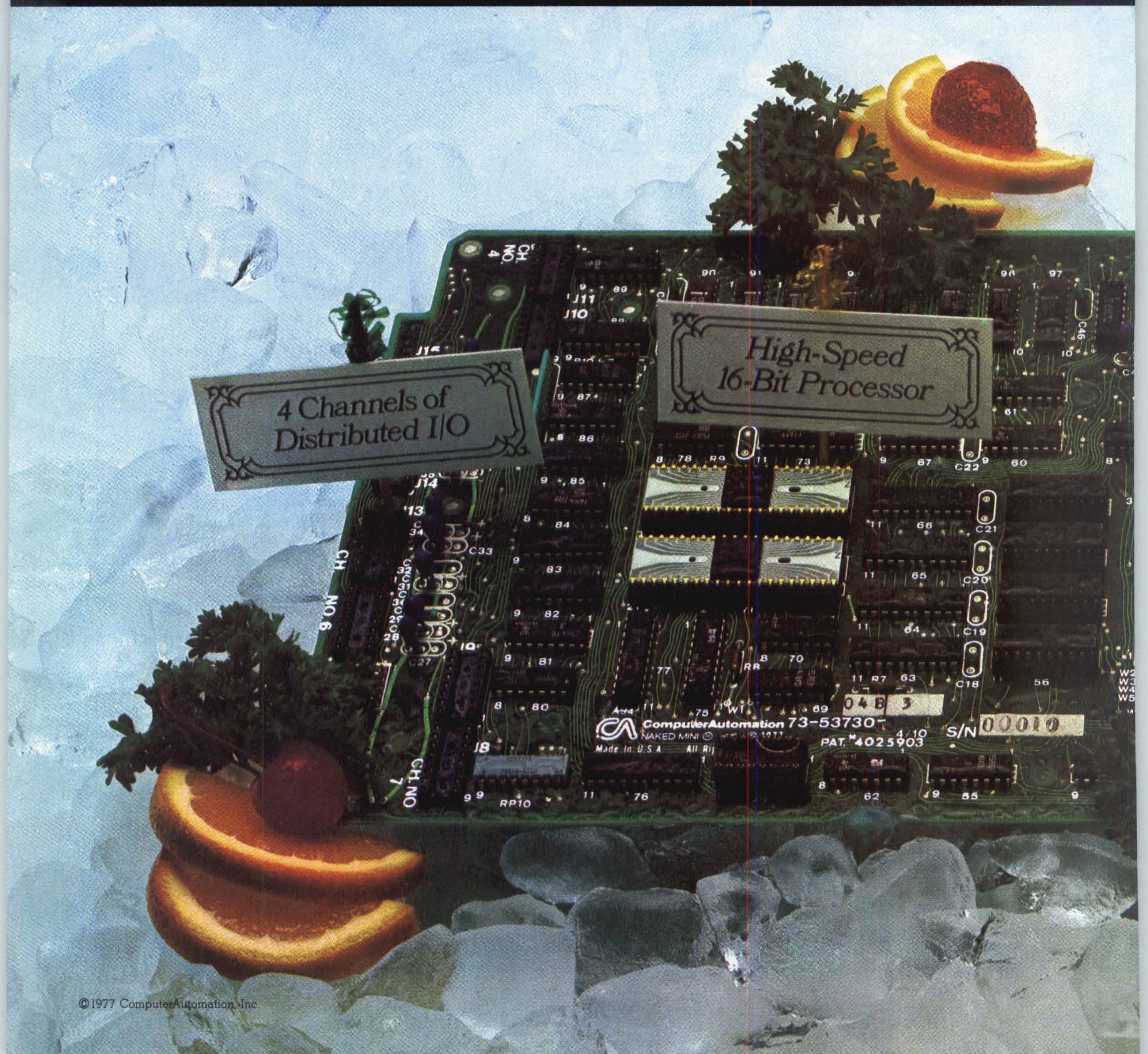

The 4/10 has 64K-word addressing and a MAXI-BUS that allows interfacing with the wide variety of interchangeable memories and I/O controllers in the NAKED MINI 4 family.

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to the firehouse. When the hardcopy record appears on the firehouse teleprinter, a fireman hits an acknowledgement button on a response panel. If this acknowledgement is not received within 20 s, the dispatcher transmits a voice message as backup.

Even after an alarm has been answered, the computer monitors the status of all assignments, including requests for additional units for major fires. It also determines if adjustments and reassignments are necessary to protect an area of the borough from which firefighting units have been depleted—and recommends the relocations to be made. Finally, the dual computer system provides management information reports of all activities processed by the system.

Operational Modes (Fig 2)

Alarm Receipt: This mode supports three methods of receiving alarms: mechanical street boxes, electronic street boxes, and telephone. Coded alarms originating

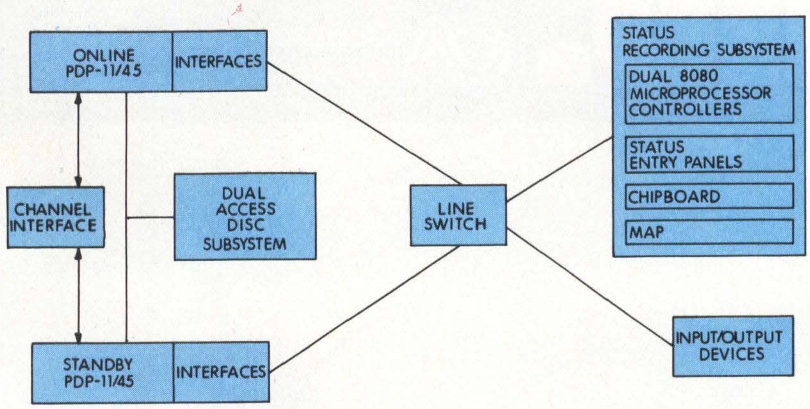

Fig 1 Basic configuration of Brooklyn MICS. Control computer is backed up by identical standby unit, both of which have access to dual disc subsystem. Online and standby microprocessor controllers serve as dual backup to two larger processors. If all four fail, system is operated manually

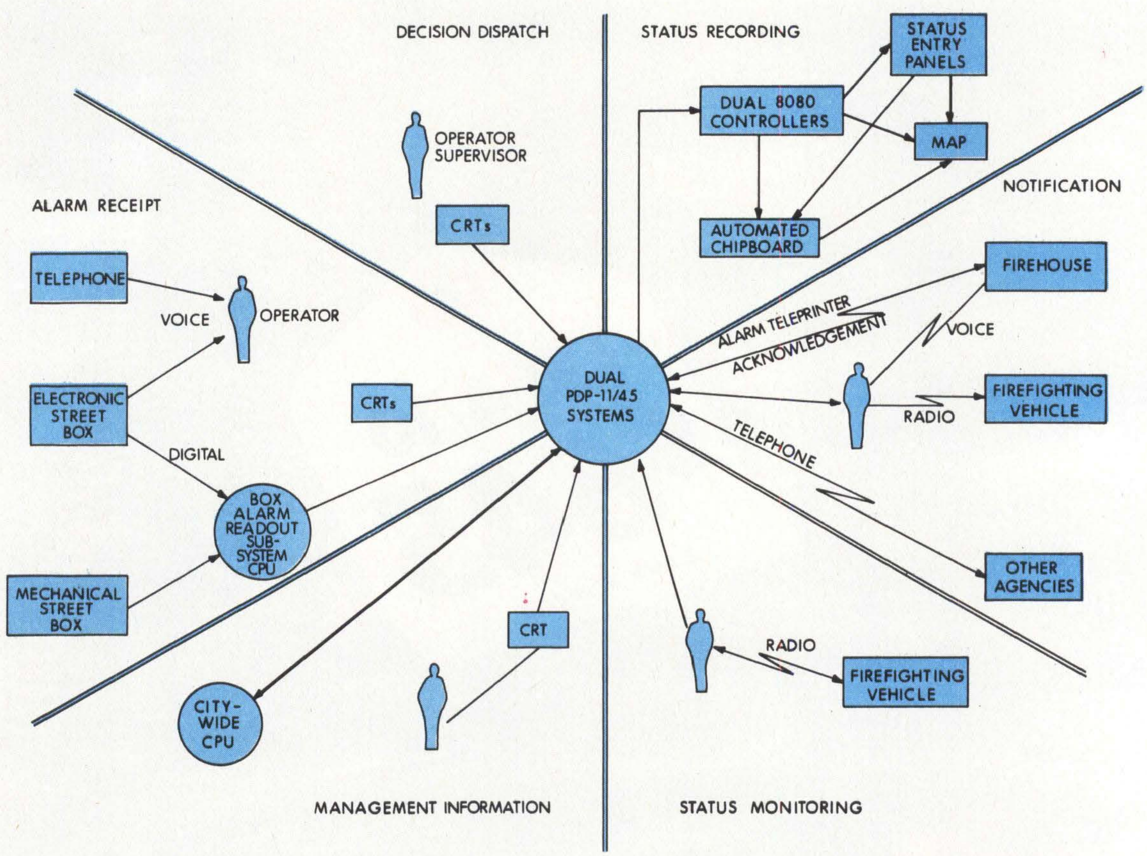

Fig 2 MICS modes of operation. All five modes are assisted by computer recommendations but operator or supervisor makes final decision. Box alarm readout system and city-wide deployment CPUs are not actually part of MICS but function with it

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Today, Teradyne has an installed base of well over 100 J380-series memory test systems working for more than 20 companies. At probe, at final test, and at incoming inspection. That's a larger dollar base than our two nearest competitors combined.

Four years of experience have made us the most capable source of memory test equipment in the world.

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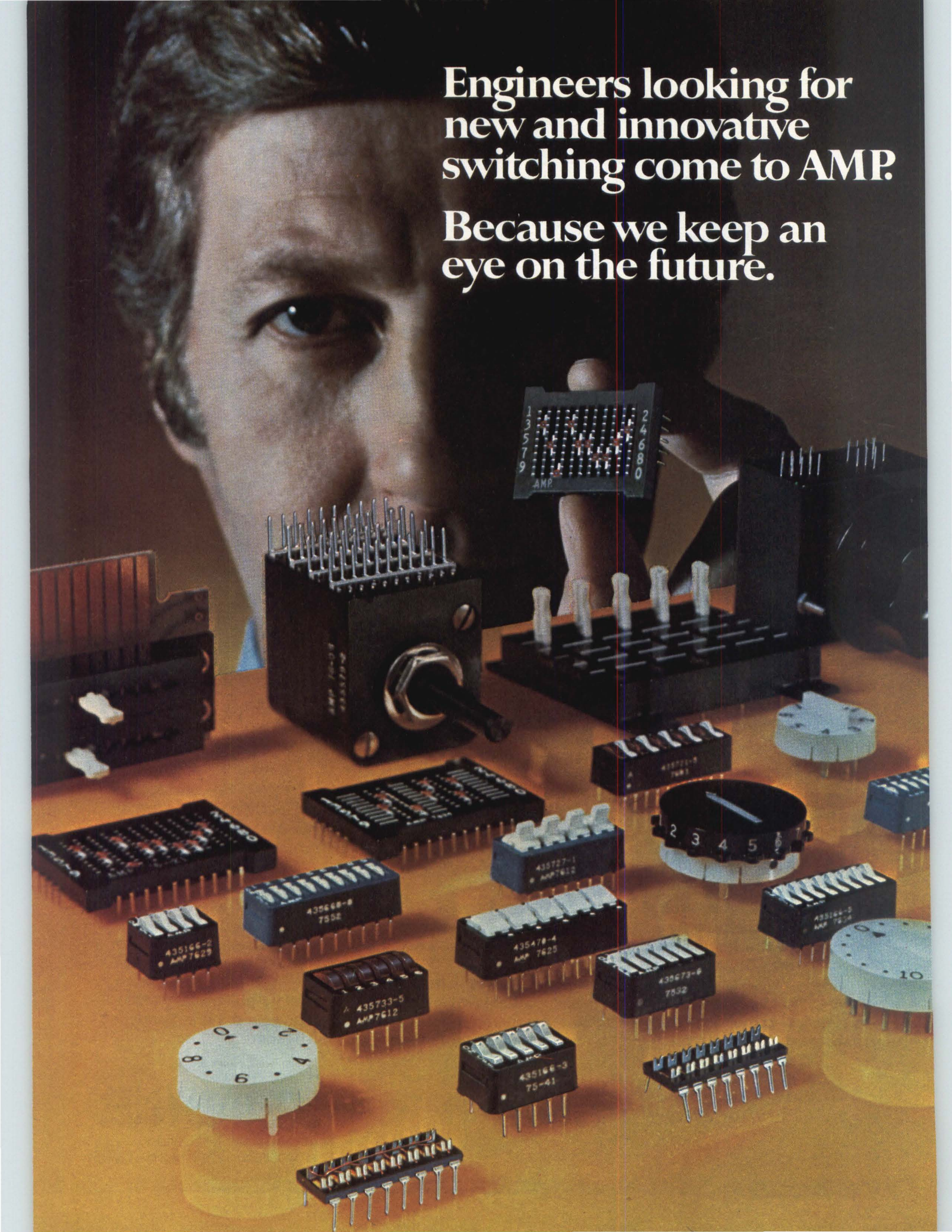
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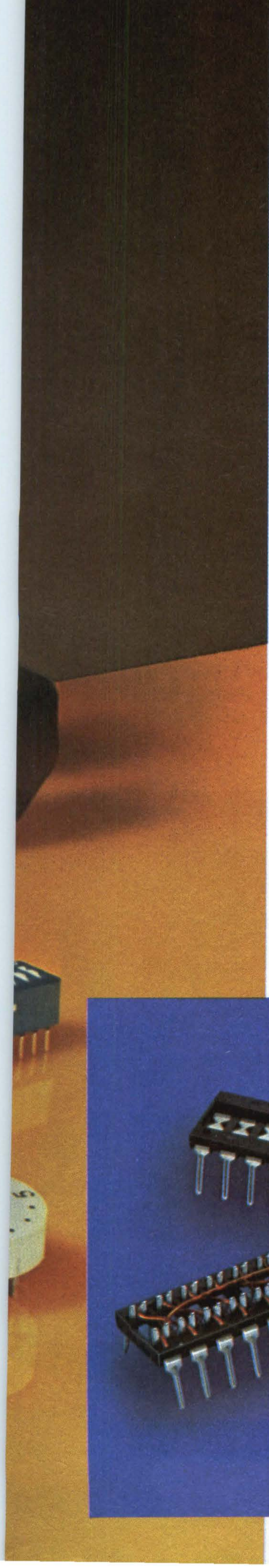

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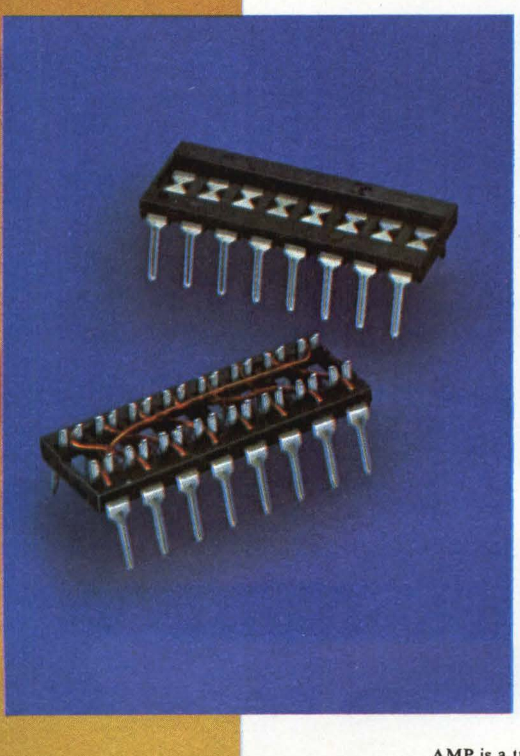

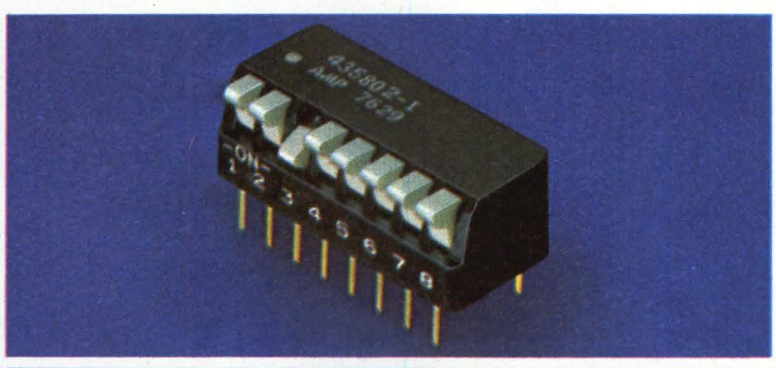

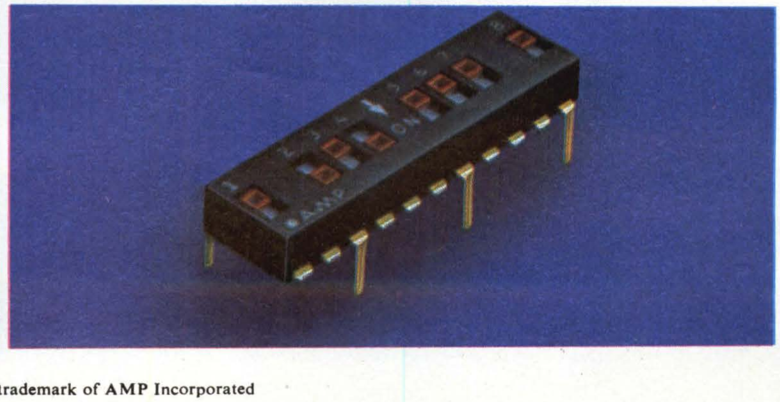

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from mechanical street boxes are multiplexed through a box alarm readout subsystem (BARS) where they are converted to digital information and processed automatically by a separate computer. Alarm data (30 bits/alarm) are transmitted to the MICS computer via a standard RS-232-C communications interface at 600 baud.

A different type of electronic street box, used in a new emergency reporting subsystem (ERS), permits a voice alarm to be presented directly to the alarm receipt operator while a digitally-encoded alarm is sent to the BARS central processing unit (CPU) via a modem interface. Each digital alarm consists of 40 bits of information including parity and is transmitted at a nominal rate of 600 baud.

ERS voice alarms and those received via telephone are switched to alarm receipt operators who obtain the pertinent information and enter it into MICS through a CRT terminal. Telephone alarm information is processed by a phonetic address translation program that provides phonetically equivalent alternatives to eliminate the need for correct spellings.

Each alarm is checked by the computer against alarms in process to determine if it is unique or if it has already been received from another source. When an alarm is found to be unique, MICS enters the decision dispatch mode. Under special conditions, an emergency control procedure can be set up to funnel all related alarms for a designated area to a special command post that operates in an independent mode.

Decision Dispatch: For every alarm received, MICS must determine how many and which firefighting units should be sent. Since MICS assists rather than controls, this determination is displayed for review and approval of an operator or supervisor before any further action is taken. Units can be added to or deleted from the recommended response or any of several other actions can be substituted.

In most cases, the decision dispatcher will handle the decision. However, a supervisor can assume control in case of unusual alarms or when coordinated actions are needed to handle special equipment. The supervisor also interacts with the computer to relocate units if an area becomes unprotected or resources have been reduced below an acceptable level.

Status Recording: This mode provides both a visual aid and automated backup. A "chipboard" maintains a record of all current incidents in Brooklyn, keeps track of the status of 100 firefighting companies normally assigned to and housed in Brooklyn, and stores domino-like chips representing the Brooklyn companies plus 45 fire companies housed outside of Brooklyn but commonly used at Brooklyn incidents. In addition, a geographic display (an illuminated map) is used to keep track of the status of the engine and ladder companies in order to assure that minimum coverage is maintained at each area.

Status entry panels are located at alarm notification workstations. Each panel is actually a specially-designed keyboard for updating unit and incident data.

During automatic or prime mode of operation, the online microprocessor controller maintains control of chipboard, map, and status entry panels as a peripheral to the computer. If both PDP-11/45s fail, the microprocessor controllers assume full control of the status recording subsystem.

If both computers and both controllers fail, the displays are updated in manual operation directly by the status entry panels. In that situation the system supervisor determines the availability of a company by the state of the associated light. The supervisor then removes the plastic chips for operational units and sets up a visual display manually.

Notification: At this point in the cycle, the units chosen to respond to an alarm might be in the firehouse or might be at the site of an earlier alarm. If the unit is at the firehouse, the alarm order is transmitted by the teleprinter; if the unit is at another location, the order is sent by radio. In both cases, a hardcopy record is printed on the firehouse teleprinter.

To complete this phase, an acknowledgement must be sent by the selected unit. Each firehouse in Brooklyn contains a microprocessor-controlled response panel which also functions as controller for the alarm teleprinter. Acknowledgement messages are transmitted by pressing panel buttons.

Notification also involves contact with other FDNY commands; eg, second alarms are sent city wide. In addition, certain situations might prompt the operator to notify police, ambulance, or even sanitation departments.

Status Monitoring: The status of both units and alarm incidents are monitored by MICS to provide accurate real-time knowledge of the availability and location of all firefighting units. Units report by radio when they complete their work and are leaving a scene, and again when they arrive back at the firehouse, or at another scene when ordered to relocate.

MICS acknowledges all unit reports and updates availability status records. An automatic monitoring function alerts the radio dispatcher if a unit fails to report within a preset length of time.

Management Information: A variety of functions performed in this mode support the actual dispatching process. These include data recording, which frees dispatchers from preparing routine paperwork and captures data to be reported to management; activity reporting, which provides statistical summaries of unit and department activities; and inquiry/retrieval, which allows access to information on incidents less than 72 hours old.

In addition, this mode provides performance monitoring of critical parameters, and load generation to measure response rates and gather data on city wide deployment. It also programs time scheduled events, supports dispatcher training, and controls operation of printing terminals for administrative message switching.

(*Continued on p* 58)

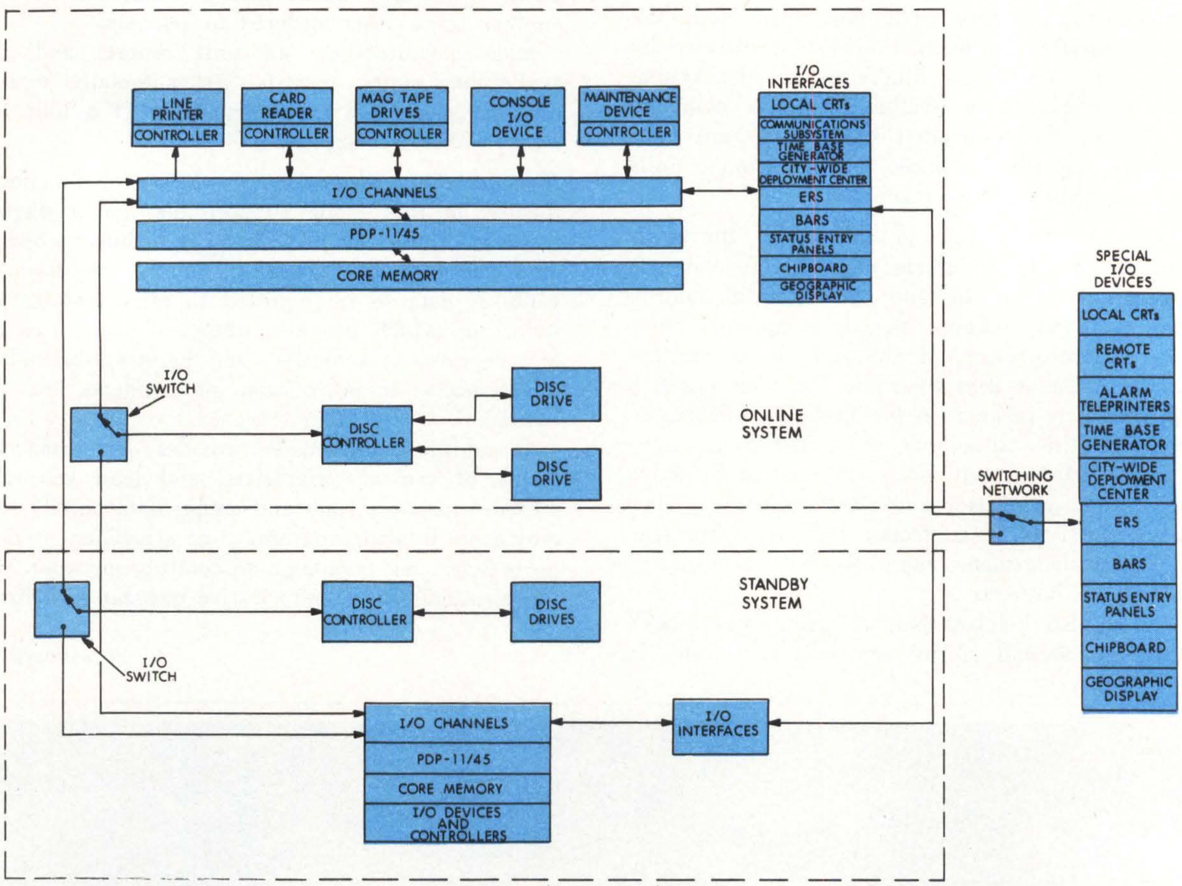


Fig 3 Brooklyn MICS detailed hardware configuration. Online and standby systems are fully redundant. They access dual disc drive subsystem and special input/output devices via switching network

Hardware

The two PDP-11/45 minicomputers (Fig 3) are configured with 96k words of core memory as well as three 88M-byte discs, two tape drives on each system, line printers, card reader, CRT terminals, special duty terminals for central office operations, and a microprocessor-controlled alarm teleprinter in each fire station. Status recording subsystem 8080-based controllers contain 8k bytes of read-only memory and 2k bytes of random-access memory that enable control of devices which show unit and incident status and location changes.

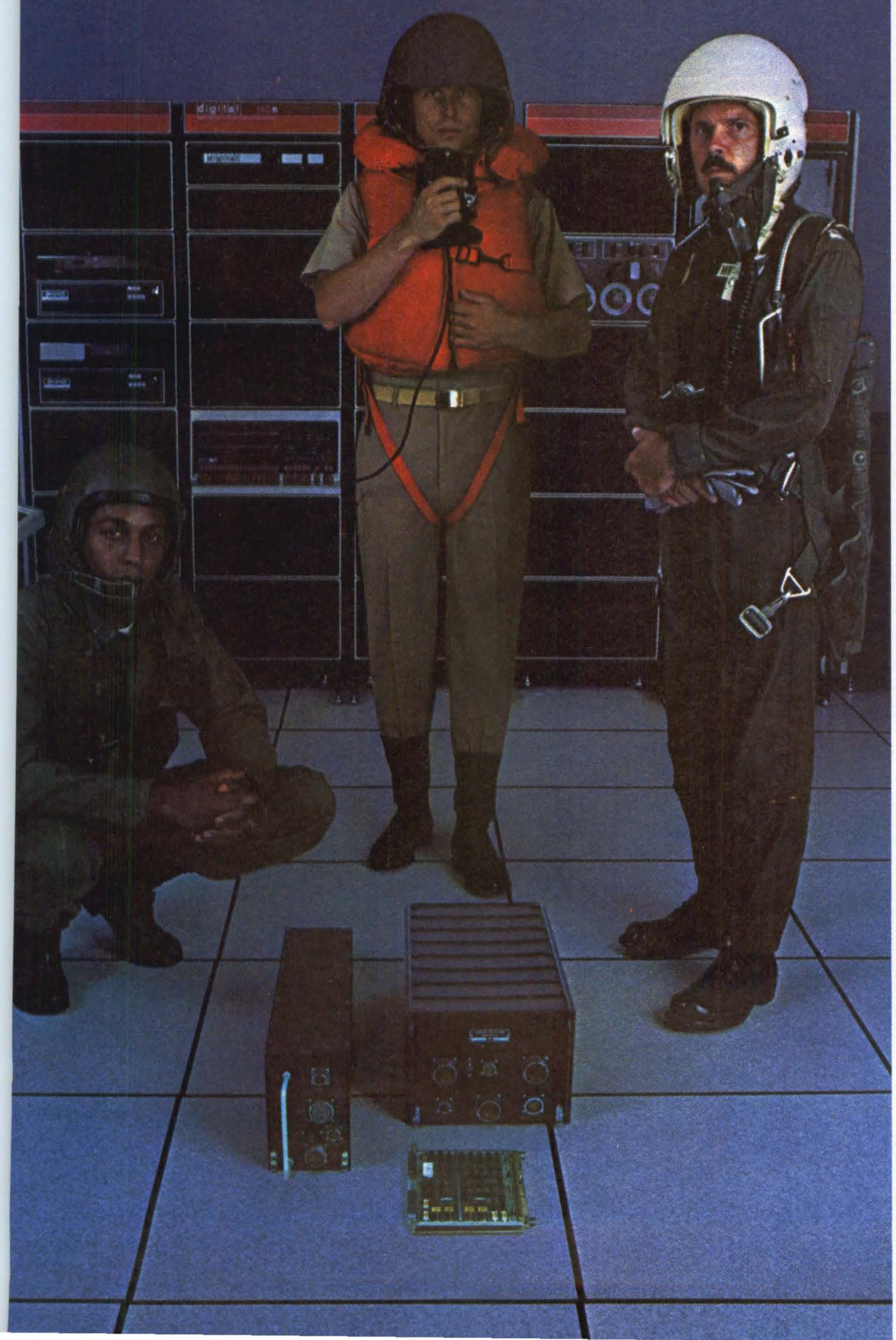
Communication is maintained via FDNY's own communications lines. Therefore, even a major fire at a telephone company switching center is unlikely to seriously affect the fire alarm system. A communications multiplexer subsystem capable of handling 64 asynchronous telecommunications lines is maintained for MICS.

An input/output (I/O) switch enables access to the dual disc subsystem by either the online or standby computer so that either or both disc subsystems can be connected to either computer. This switch also controls part of an I/O bus, allowing other devices to be accessed by the computers.

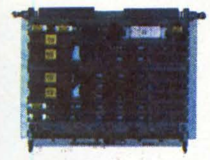
Primary access to MICS is via 16 CRT terminals located at alarm receipt, decision dispatch, and management points. In addition, 100 teleprinters are distributed among the borough firehouses and three more are situated at locations in the central office and at headquarters. These provide a hardcopy record of all alarms and equipment dispatch orders. Both firehouse alarm teleprinter/response panels and CRTs are specially designed units supplied by Megadata Computer and Communications Corp.

(Continued on p 62)

Now Norden gives the PDP-11/34M a little brother: the LSI-11M.



New militarized micro-computer uses same software as commercial LSI-11.



The LSI-11M is a full-scale, 16-bit micro-computer and the smallest computer in the PDP-11M line. Part of a new family of fully-militarized computers, it uses exactly the same software as the commercial LSI-11.

Combining Norden's experience in military electronics with DIGITAL architecture and DIGITAL software, the LSI-11M offers exceptional price/performance. This is a direct result of a rich repertoire of over 400 instructions and a low hardware cost.

Familiar features plus militarized peripherals.

Available without chassis, the LSI-11M comes as a 6 x 8.2 x 1" CPU module. This module is available with 4K words of resident semiconductor memory. Further memory options in the form of 4K PROM and 16K and 32K core modules are offered. Peripheral and I/O connections are accomplished thru fully militarized serial and parallel I/O modules. The LSI-11M also has a real-time operating system (RT-11).

For more information, call or write Director of Marketing, Computer Products Center, Norden Division, United Technologies Corporation, Norwalk, Connecticut 06856; Telephone (800) 243-5840 toll-free, or call (203) 838-4471.

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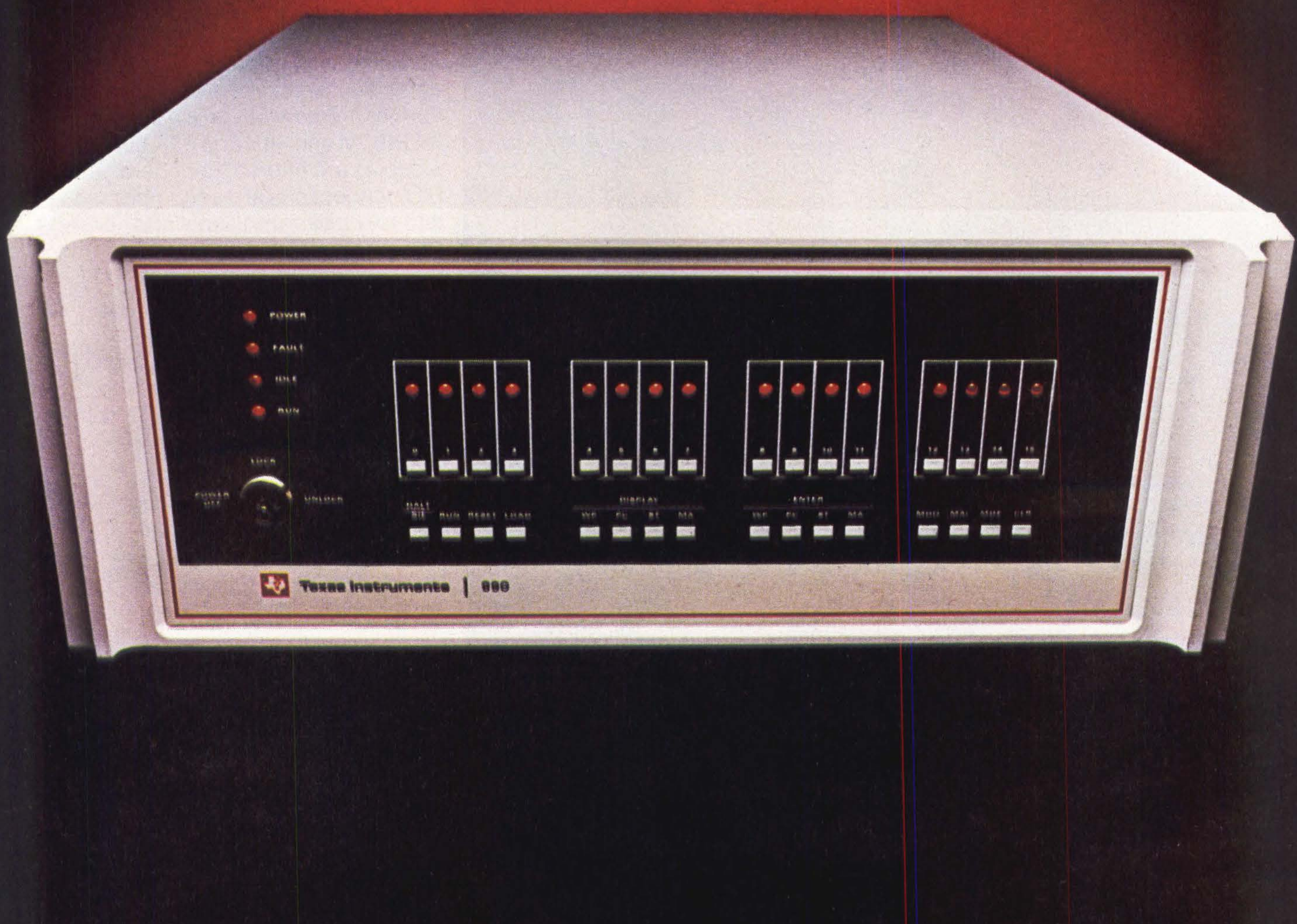

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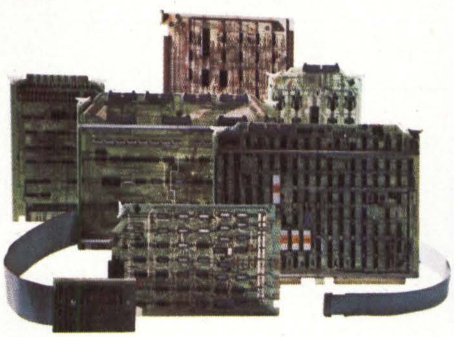

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Built for system flexibility.

In small or large configurations, the 990/10 design provides surprising flexibility for a small investment.

The CRU, with up to 4096 I/O lines, reduces interfacing costs by keeping controller complexity to a minimum. The TILINE* asynchronous high-speed data bus can support both high- and low-speed devices and takes advantage of design simplicity for simultaneous data transfer between peripherals, the CPU and memory.

Model 911 Video Display Terminal

With the 990/10, you get a powerful instruction set with an extended operating feature that allows hardware to take over operations that software would normally execute. An optional mapping feature provides memory protection and memory expansion to 2 million bytes. And, optional error-correcting memory corrects single-bit errors for increased system reliability.

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With common higher level languages, FORTRAN IV, COBOL and Multiuser BASIC, plus the 990/10 assembly language, you have all the tools you need for an efficient application program.

Both the disk-based and memory resident operating systems give you modularity and flexibility for system generation to meet application demands. We offer program development aids for creating and testing software, and communications software to support synchronous or asynchronous data transmission.

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CIRCLE 36 ON INQUIRY CARD

Accurate time of day information is provided to the MICS computer by a time base generator. Time is expressed in hours, minutes, seconds, and milliseconds for inclusion in reports.

In the near future, a solid-state uninterruptible power supply (UPS) that will be able to support all MICS equipment for up to 20 minutes will be added to the system. It will be for use during the transient periods that would be required for the central office dual motor-generator sets to come up to speed to supply power if commercial supplies failed.

Software

A control program consisting of system, application, and data management continually coordinates all supervisory functions and monitors, schedules, and controls the execution of MICS programs. It includes the monitoring of all system operations that are program controllable to check hardware operation and performance.

System management is concerned with status, performance, and effectiveness of the overall system. It controls and monitors both the system and interjob processing flow. Events or requests are handled on a

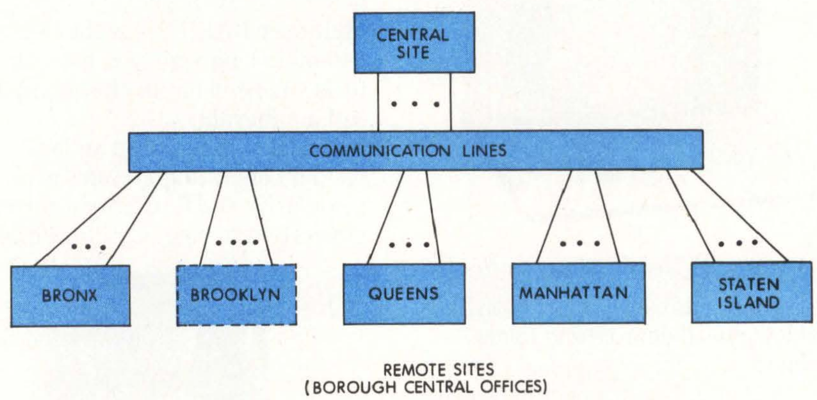

Fig 4 Overall configuration of recently approved centralized MICS for all of New York City. All data processing functions for five borroughs of New York City will be performed at central site. However, each remote site or borough central office will control its own alarm receipt and dispatch functions. Initially Brooklyn MICS will remain in its present state although it will be part of overall system. Later it will be reconfigured to be same as other four central offices

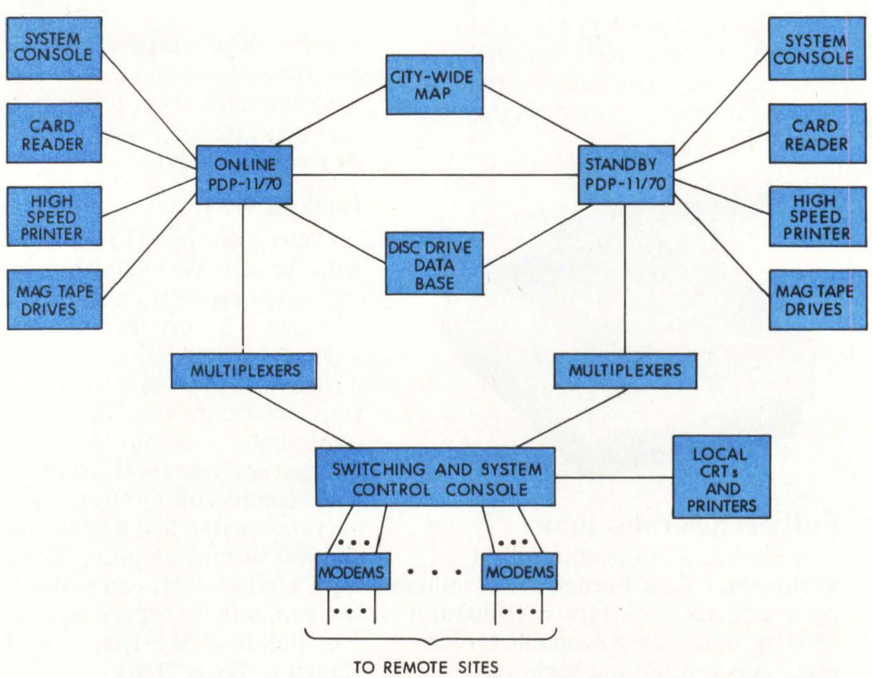

Fig 5 FDNY central site configuration. Dual computers will be redundant but standby unit will be available for other processing duties. Central site concept eliminates need for duplicating some of data processing hardware at each remote site

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priority basis depending on relative importance. Application management controls supervisory application processing needs of the program modules, while data management controls the transfer of information between main storage and external devices.

City-Wide MICS: The Next Step

Approval of a FDNY proposal to expand the Management Information and Control System (MICS) to cover all five boroughs of New York City was received in August of this year, just six months after the Brooklyn computer-aided dispatching system went online. This multi-borough MICS will concentrate data processing at one site that will be in constant contact via 9600-baud communication lines with central offices in all five boroughs (Fig 4).

The new system will necessarily be even more sophisticated than that now in use in Brooklyn. However, the present borough MICS will be compatible with the new centralized system and in time will be converted to include the same equipment.

This centralized approach, according to John Mohan, director of the FDNY Bureau of Information and Computer Services, and Irwin Steinberg, deputy director, will result in a savings of \$2 million—about 20%—over the cost of four separate systems. In addition, data processing requirements will be more easily administrated, operated, and supported by only a single group of specialists. There will also be less total equipment and less disruption of services.

The central data processing function will be controlled by dual Digital Equipment Corp PDP-11/70 computers, one online and the other on standby (Fig 5). The latter computer, however, will be available for other communication or batch work until required to go online.

Each processor will be supported by high speed magnetic tape drives, high speed line printer, card reader, system console, synchronous multiplexer for communication with borough central offices and firehouses, and asynchronous multiplexer for local CRTs and printers. Four dual access 176M-character disc drives will permit programs, static files, and dynamic files to be separated.

Communication with borough central offices (remote sites) will be maintained via three synchronous, full duplex channels. Any one of these lines will be sufficient to maintain central to remote communication with minimum degradation; however, an additional "hot line" will be provided between central and remote sites as backup.

All software support and maintenance will be performed at a single location. The central site processor will contain all application and communication software required for borough central office interface.

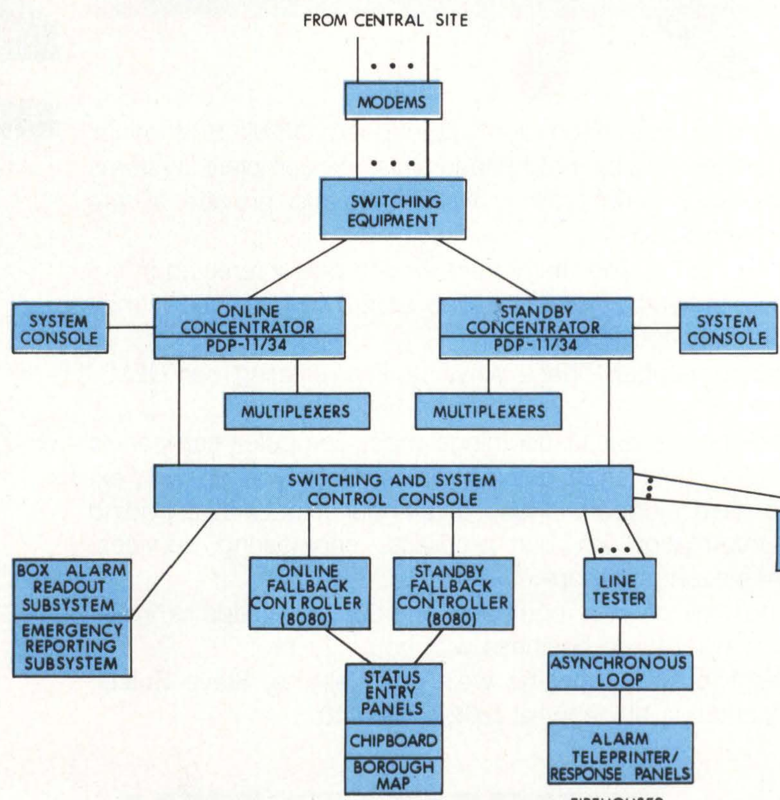

Fig 6 Borough central office or remote site configuration. Redundant concentrators control message traffic via switching and system control console. Microprocessor controllers are backup as in Brooklyn MICS

(Continued on p 68)

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Unlike logic analyzers, the μScope 820 console provides a genuine solution for test and service personnel. It provides the same inside look at system operation that you get with a logic analyzer. But the μScope 820 goes far beyond the mere collection of data. Its internal microprocessor system can actually analyze the data it collects. It does that with diagnostic programs you design specifically for your end product.

Rather than passively watching system operation, the μScope 820 console lets you execute application programs or diagnostics you develop, in real time or single steps. And it provides full breakpoint capability and a large trace memory.

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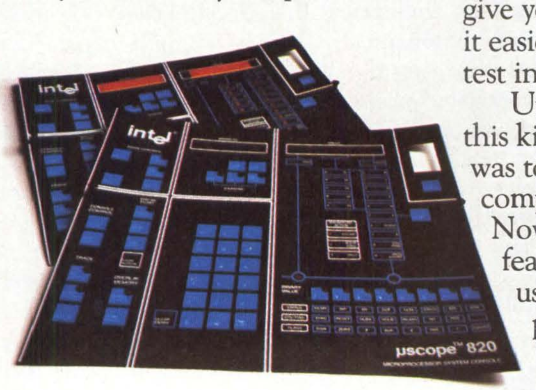

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Circle 39 for technical information.
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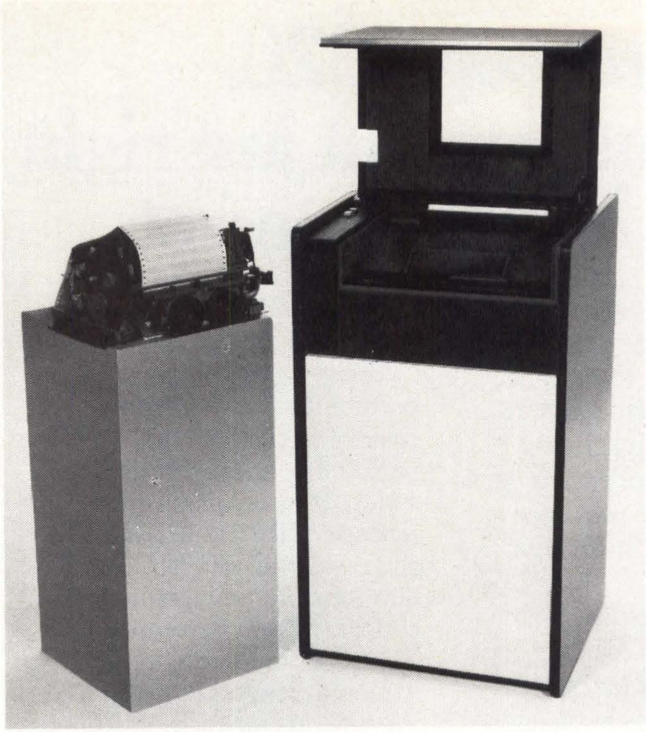

Local CRTs and printers at the central site will also serve in general system monitoring and other functions.

Alarm receipt and dispatch functions will remain within each borough. Two concentrators—using Digital Equipment Corp PDP-11/34 computers—at each remote site will control message traffic to and from the central site (Fig 6). One computer will always be online, the other on standby. A switching and system control console will determine which concentrator is active and direct traffic to it. However, control and operation of the concentrator and switching equipment, as well as all system maintenance, will be initiated from the central site.

The remote concentrators will automatically provide information to the central site CPU on component failures. Therefore maintenance will be initiated without action from remote site personnel.

Standardization will be maintained on all remote site installations. Equipment interfaces and equipment will be identical for each site.

The centralized system will also be designed and implemented by Bradford National Corp, under the direction of project manager Ronald Scherma. Four phases proposed are system design, central site implementation, simultaneous remote site implementation, and interconnection of central and remote sites and the firehouse teleprinter network. A time schedule of 36 months is predicted for completion of all four phases.

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DC&AS BRIEFS

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In a direct computer control (DCC) system offered by Ragen Precision Industries, Inc, N Arlington, NJ, multiple stations automatically supply components to be inserted by an operator who is directed by a precision digitally controlled projector that beams an arrow onto the board, indicating the location, orientation, and polarity of the component. Computer-stored programs, which replace use of punched tapes, are stored, cataloged, and edited and are assignable to equipment stations. Up to seven elements can be included in a system: a processor which is a programmable logical control unit; a disc drive which stores station operating commands and data; and—at each station—operator controls, a digitally controlled articulated projector, an automatic component delivery system, a numerical operation number readout, and auxiliary signal light logic. □

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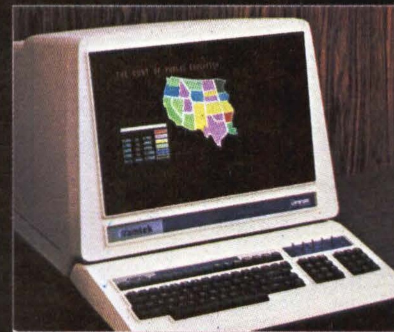

Here's great resolution and a bright, flicker-free display on a matrix of 512 elements by 256 lines in a terminal that's easy to program to your requirements.

No longer do you have to put up with poor resolution in economy-priced terminals. Ramtek gives you a combination of true graphics—such as vectors, conics, plots and bar charts—and high-speed alphanumerics with a high-resolution industrial-quality monitor. You can choose two sets of 8 colors for both graphics and alphanumerics. Dual and split screen capability too, with all the price/performance benefits of raster scan technology. And the independent alphanumeric refresh offers you single-character addressability within a visible matrix of 25 rows of 80 characters that are bright, crisp, sharp, and well defined. The refresh memory also allows selective erase, modification, and update.

The MICROGRAPHIC terminal is controlled by a powerful Z-80 microprocessor with up to 28K bytes of PROM and 16K bytes of RAM. Ramtek's control software gives you TTY compatibility and high-level graphic functions commanded by ASCII text strings. Choose from an extensive list of options such as additional serial I/O ports, alphanumeric overlays, programmable fonts, and packaged software.

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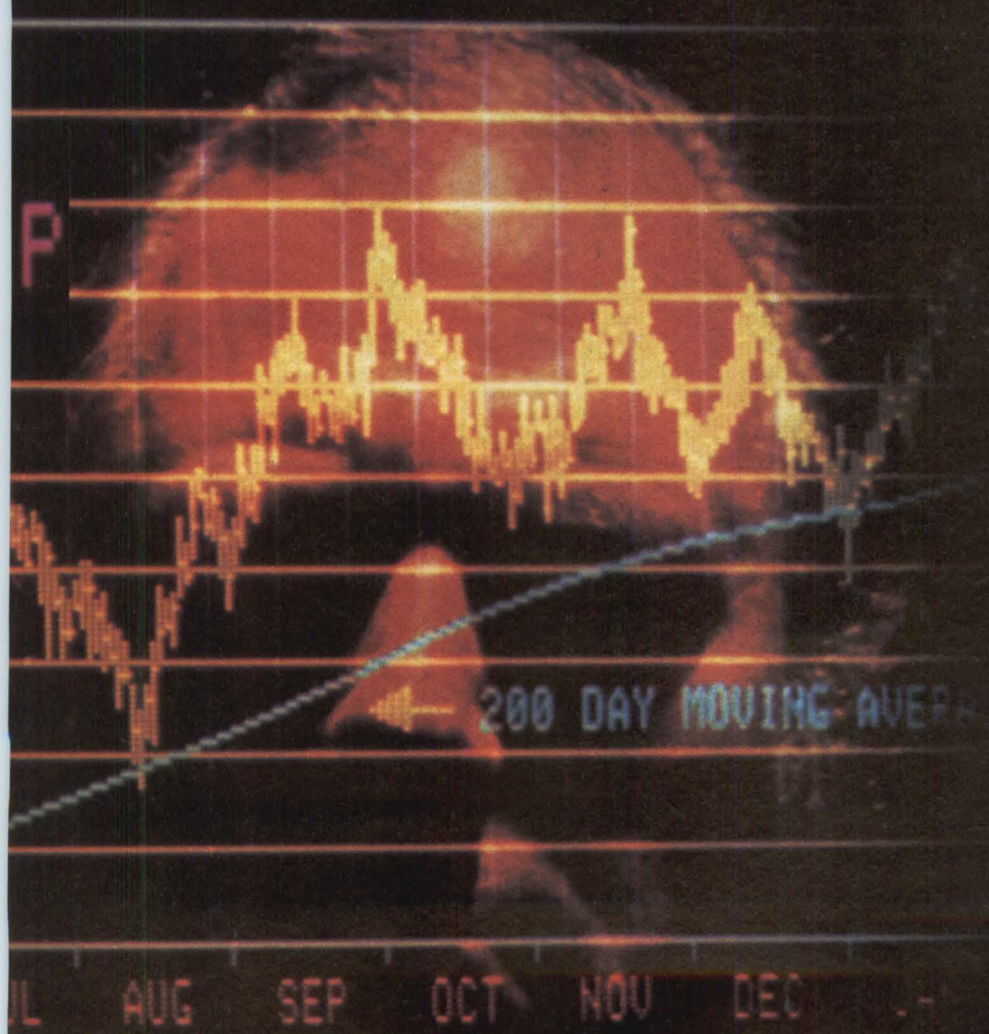

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CONFERENCE SESSIONS

TUESDAY

MORNING

Small Business Systems
Organizer: Don Schnitter, Basic Four Corp.

Trends in CRT Terminals
Organizer: To be announced

AFTERNOON

Small Disk Memory Trends
Organizer: Henry T. Meyer, CalComp

Buyer Be Aware: How Reliable and Flexible will Future Systems Be?
Organizer: Edward J. Bride, The Conference Co.

Low Cost Microcomputers in Business Applications
Organizer: Adam Osborne, Osborne & Assoc.

WEDNESDAY

Trends in Printer Development
Organizer: Neil Kleinman, International Data Corp.

Intelligent Applications of Minis in the Small Business Environment
Organizer: John Kirkley, Datamation Magazine

Criteria Used in Selecting & Evaluating a Minicomputer
Organizer: Joe Baker, Robert W. Baird Co.

How to Keep an On-Line System from Crashing
Organizer: Neil Kelley, Infosystems Magazine

Application of Microcomputers to Military Avionics
Organizer: Joe Genna, Delco Electronics

Trends in Mini/Micro Software
Organizer: Joe DeVita, Computer Automation

THURSDAY

OEM Peripherals in End-User Systems: The Current View
Organizer: George King, Benwill Pub. Co.

Distributed Data Processing
Organizer: Roger Billings, Billings Computer

Getting Into the Microcomputer Business
Organizer: Robert S. Jones, Interface Age Mag.

Computer Law
Organizer: Richard L. Bernocchi, Irell & Manella

Transaction Processing with Networks
Organizer: Elton Sherman, General Automation

NOTES:

1. **Morning Session — 9:30 - 12:00 noon**
   Afternoon Session — 1:30 - 4:00 p.m.
2. **All Sessions will be held in the Anaheim Convention Center**
3. **Monday, December 5 is IEEE Career Day. Contact: Vincent J. Giardina (201) 981-0060**

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Available digital processing technologies and key design tradeoffs are discussed for the rapidly emerging field of computer voice response systems. These techniques are implemented to develop an operational application

Design Guidelines for a Computer Voice Response System

Paul Thordarson*

Input-Output Computer Services, Incorporated
Cambridge, Massachusetts

The field of computer voice response systems has been developing rapidly in response to the need to structure future computers to communicate in a manner that is natural for the user. For instance, upon suitable user interrogation, computer-driven peripherals could respond directly in spoken words—the ultimate in machine-to-man communication. The input device needed to access such a computerized system, the ordinary dial or touch-type telephone, is already installed in millions of homes and businesses for immediate use by "trained" users. Even today, one can enter a 7-digit number and listen to voice recordings of the latest weather report, stock report, or time of day. These systems communicate by voice in one direction—from machine to user—upon coded keypad entry.

To enable designers to choose the best method for structuring machine-to-person voice communications, techniques and implementation considerations pertinent to such a system are discussed. First, various technologies available to make a computer "speak" are described. Second, some design tradeoffs to be considered in developing a voice response system are analyzed. Finally, an operational implementation of a computer voice response system for a real-world application—an automated weather bureau for the general aviation public—is presented.

Voice Response Technology

Computer voice response (CVR) systems consist of a data base containing a collection of individual words or phrases (a vocabulary) and some means of assembling these words or phrases into meaningful responses (Fig 1**). The exact format of the vocabulary varies substantially among the existing technologies. In general, the more compact the representation for speech, the more complex the recording and reproduction processes become.

Current technology available for CVR systems can be classified under two very broad categories: waveform coding and analysis/synthesis. Waveform coding represents a signal by recording its amplitude while it varies in time. Analysis/synthesis records a set of parameters, such as frequency content, derived from the waveform. Both systems vary greatly in complexity and performance, so that design tradeoffs can be highly involved.

Waveform Coding Systems

Waveform coding systems produce voice output using recordings of human speech. A vocabulary of individual words and phrases is recorded and entered into the computer. Typically, each word is entered as an individual file or record in a large data base. Entire sentences are "spoken" by retrieving required individual words and phrases from the vocabulary and

*Mr Thordarson is currently employed by Digital Equipment Corp, Maynard, Mass.

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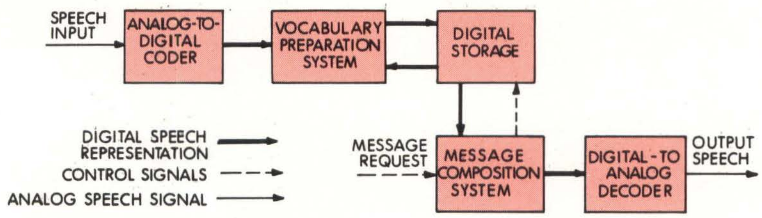


Fig 1 All-digital voice response system. This system requires analog-to-digital coder for obtaining digital representation of speech signal. Similarly, appropriate digital-to-analog decoder converts digital representation to analog signal. Vocabulary, in digital format, is first processed and then stored in digital memory. Access to vocabulary entries is performed by message composition system for correct sequence and presentation to output decoder (Courtesy of IEEE)

reproducing them in the proper sequence. Although both analog and digital techniques can be used for recording the speech, this article concentrates on digital recording techniques because they are more easily adapted to conventional computer hardware.

Digital waveform coding requires that the amplitude of the speech signal be sampled. Sampling is done using an analog-to-digital converter (ADC) which measures the signal amplitude at regular time intervals and produces a series of binary numbers representing that signal amplitude at each interval. For a sampled waveform, the highest frequency in the waveform which can be reproduced qualitatively is called the Nyquist frequency, which is equal to one-half of the frequency or rate of sampling. Experiments show that acceptable quality speech can be reproduced with a signal bandwidth of 3 kHz, thereby requiring a sampling rate of 6 kHz or greater.

Digital recording and reproduction of speech requires the circuit devices as shown in Fig 2. The input speech signal is first filtered to remove all frequencies in the signal above the Nyquist frequency (in this example 3 kHz), then sampled using a sampler and encoder—an ADC. A digital representation of the signal amplitude is produced every 166.7 μs (for a 6-kHz sampling rate); this representation is stored on the vocabulary storage medium, such as a disc, for later reproduction.

The reverse of the recording process, the reproduction process consists of first reading the digital representation of the waveform from the vocabulary storage medium. The retrieval component is a simple hardware device or retrieval software running on a general-purpose computer. Retrieved digital samples are converted to an analog waveform by a decoder, such as a digital-to-analog converter (DAC). This decoder

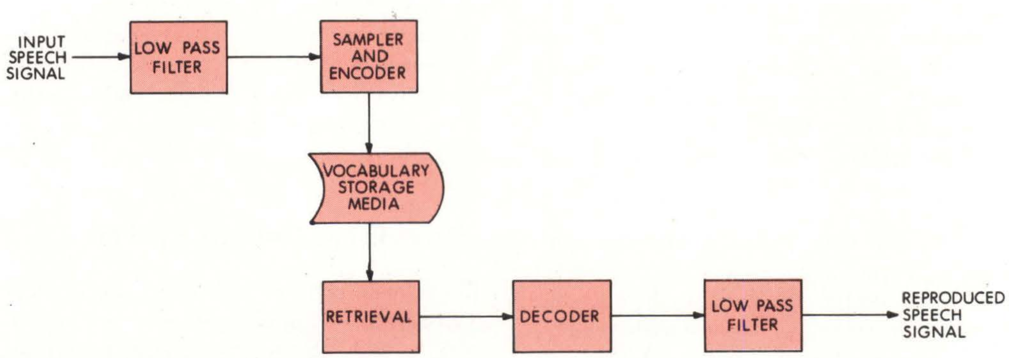


Fig 2 Digital recorder/reproducer. Speech signal is first filtered to remove high frequency components unnecessary for quality speech reproduction; cutoff frequency of filter is 3 kHz. Filtered signal is then sampled at rate at least twice cutoff frequency (6 kHz), and samples are stored on digital storage medium such as magnetic disc. Speech is reproduced by retrieving speech samples and decoding them by applying function which is inverse of the encoder function. Resulting signal is filtered to remove distortion introduced by sampling process, giving reproduction of original signal

applies the inverse of the encoder function to the samples to reproduce the original waveform. Finally, the reproduced waveform is again filtered by a 3-kHz lowpass filter to remove all harmonic components introduced by the sampling process.

All techniques for waveform coding resemble the system shown in Fig 2. Most systems use a sampling rate between 6 and 8 kHz. However, the number of bits recorded in the encoded speech samples varies greatly between systems. The waveform coding techniques to be reviewed here vary in bit rates from 10k to over 60k bits/s, and result in a factor of 6 change in the amount of data stored for any given spoken word. Therefore, the choice of encoding technique directly affects the size and throughput required of the storage medium. For example, the size and throughput required of the vocabulary storage medium are both six times greater at 60k bits/s than at 10k bits/s. However, encoding techniques which offer lower data rates require more complex encoding equipment. Choice of technique depends on whether the vocabulary is small, with encoding/decoding equipment representing most of the cost, or large, with vocabulary storage medium representing the largest part of the cost.

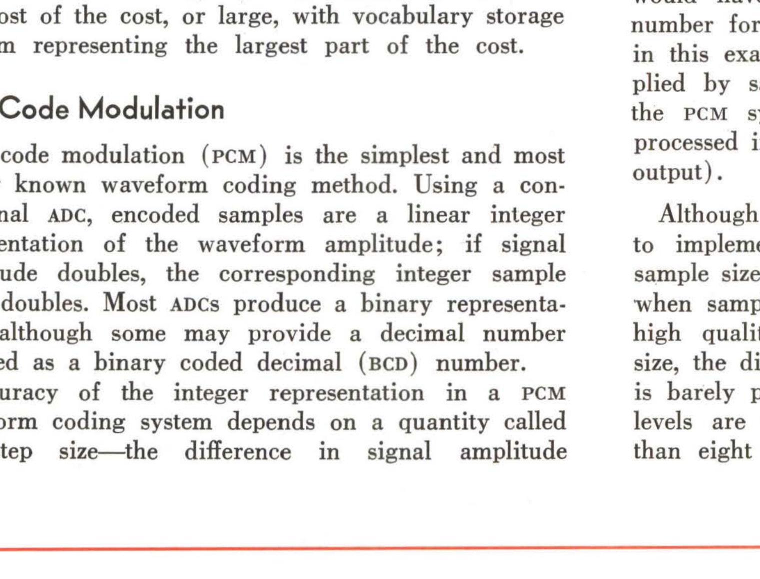
Pulse Code Modulation

Pulse code modulation (PCM) is the simplest and most widely known waveform coding method. Using a conventional ADC, encoded samples are a linear integer representation of the waveform amplitude; if signal amplitude doubles, the corresponding integer sample value doubles. Most ADCs produce a binary representation, although some may provide a decimal number encoded as a binary coded decimal (BCD) number.

Accuracy of the integer representation in a PCM waveform coding system depends on a quantity called the step size—the difference in signal amplitude represented by two successive integer sample values. For example, if in a PCM encoder the integer 14 represents a signal amplitude of 14 mV and the integer 15 represents a signal amplitude of 15 mV, step size for this encoder is 1 mV. Fig 3 illustrates a waveform and the encoded samples produced by a PCM encoder with a 1-mV step size and a sampling rate of 1 kHz. Sample values are shown as decimal integers; actual representation is binary.

Step size determines the smallest variation in the input signal which will produce a variation in the encoded samples. The smaller the step size, the more accurate the signal reproduction will be. Smaller step sizes, however, require a larger number of steps (ie, larger "greatest possible integer value" for an encoded sample) to ensure that the entire range of input signal values can be encoded. The largest possible value for the integer determines the number of digits (bits) in the binary value of that integer. For example, if an encoder with a 1-mV step size is used to encode signals which could vary from −1 to +1 V, encoded samples would have 2000 possible values. Since the binary number for decimal 2000 is 11 bits long, sample size in this example would be 11 bits. Sample size multiplied by sampling rate gives required data rate for the PCM system (ie, the number of bits which are processed in a unit of time in order to maintain voice output).

Although PCM systems are the simplest CVR systems to implement, their data rates are the highest. A sample size of at least 11 bits (data rate of 66k bits/s when sampling rate is 6 kHz) is required to achieve high quality speech reproduction. With this sample size, the distortion introduced by the sampling process is barely perceptible to the listener. Higher distortion levels are tolerable; however, a sample size of less than eight bits (data rate of 48k bits/s) will intro-



SAMPLE TIME (ms)	ENCODER OUTPUT
1	-83
2	-121
3	-53
4	28
5	75
6	165
7	112
8	50
9	-110
10	-62

Fig 3 Waveform encoded using pulse code modulation. Waveform is sampled by PCM encoder every millisecond (1-kHz sampling rate) using step size of 1 mV. Sample time and corresponding integer value of encoder output are listed in table. Integer corresponds exactly to signal amplitude in millivolts

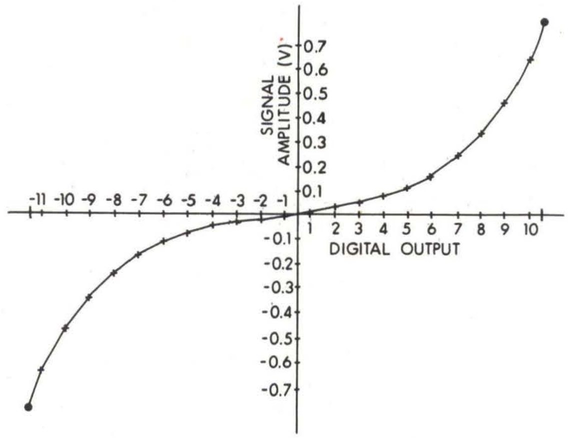


Fig 4 Log PCM transfer characteristic. Response sensitivity of human ear is logarithmic; therefore, its "incremental" sensitivity is lower at larger amplitudes. Log PCM takes advantage of this characteristic by providing small step size at low signal amplitudes, and large step size at high amplitudes, thus increasing encoder resolution at amplitudes where ear's sensitivity is greater

duce more distortion than is acceptable by the majority of listeners.

A decrease in data rate can be achieved by using a variation on PCM called log PCM. In log PCM, step size is not constant over the entire range of signal amplitudes to be encoded. Rather, it increases as the signal amplitude increases. The transfer function (signal amplitude vs encoded sample value) for a log PCM encoder is shown in Fig 4. Note that encoded sample values are proportional to the log of signal amplitude. This encoding method is effective in reducing the data rate because the human ear's response to signal amplitude is also logarithmic. Sample size in log PCM should be seven bits or greater to achieve high quality speech reproduction.

Differential Coding

Data required to encode speech waveforms can be reduced by taking advantage of some inherent audio properties. One known property is that the greatest amount of signal energy in a speech waveform lies below the Nyquist frequency. This causes successive speech samples to exhibit a high degree of correlation. (The amount by which a signal changes between successive samples is likely to be less than the largest possible value the signal can have.) Because of this correlation, a smaller sample size is required to encode

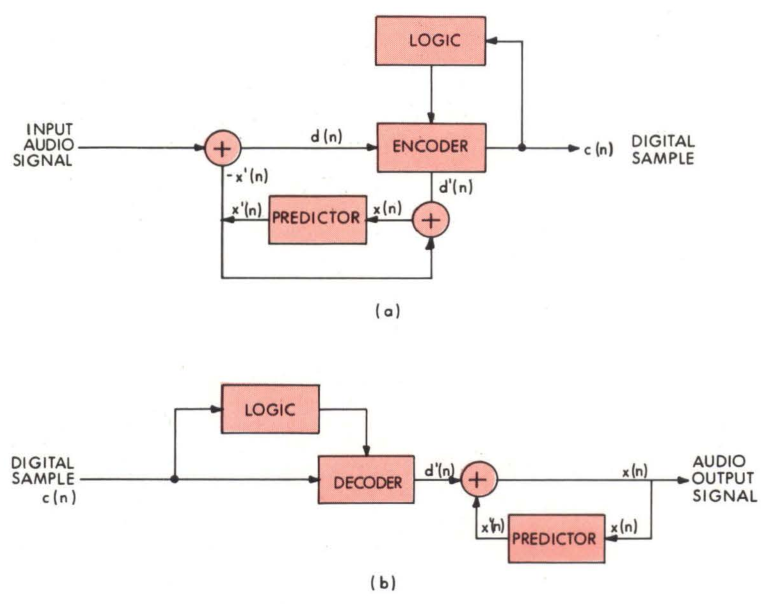


Fig 5 Differential encoder and decoder. Encoder (a) produces difference signal d(n) by subtracting predictor output x'(n) from incoming audio signal. d(n) is encoded to produce digital sample value c(n) which is stored on vocabulary storage medium. Encoder also produces d'(n), which is d(n) rounded to nearest step size. d'(n) is summed with predictor output to produce x(n). Predictor uses x(n) to produce next value of x'(n). Optional logic component uses all previous c(n) values to adjust step size of encoder. Decoder (b) takes encoded samples and decodes them to produce difference signal d'(n). Logic component adjusts step size of decoder based on all previous values of c(n). Difference signal is summed with predictor output x'(n) to produce x(n), which is used for both audio output and for predictor input which is used to produce next value of x'(n)

a waveform if the difference between successive samples is recorded than if the exact value of the signal is recorded for each sample.

Fig 5 shows a generalized differential encoder and decoder. Encoding begins by computing the difference between the input signal voltage and the predictor voltage x′ (n). This difference is the signal d(n). The encoder converts d(n) to the digital sample c(n), which is recorded on the vocabulary storage medium; conversion occurs at the sampling rate. The encoder also produces the signal d′(n), which is d(n) rounded to the nearest step-size value. For example, if the step size is currently 1 mV, a value of 14.5 mV for d(n) would give a value of 14 mV for d′ (n). This is added to the predictor output voltage to produce the signal x(n), which is used by the predictor to calculate the next value of x′ (n). While the predictor can be a complex function, in most cases it is just a holding circuit whose transfer function is $x'(n + 1) = ax(n)$. The term "a" is a constant whose value is close to, but less than, 1. It represents any leakage or loss which may be present in the holding circuit. The logic component is present in some encoding methods and is used to adjust the step size of the encoder based on previous values of the digital samples c(n).

On decode the reverse of the above process occurs. Digital samples are retrieved from the vocabulary storage medium and are decoded to produce the difference signal d′ (n). This signal will be the same as the corresponding signal d′ (n) in the encoder. The logic component dynamically adjusts the step size based on previous values of c(n). Signal d′ (n) is added to the predictor output x′ (n) to produce x(n). Audio output signal x(n) is the reproduction of the signal encoded, and is also the input to the predictor which is used to compute the next value of x′ (n).

The simplest technique using differential coding is delta modulation (DM). In delta modulation, a signal is encoded using a 1-bit sample size. If input voltage is greater than the predictor value, a logic 1 is produced for the encoded signal value, and the predictor voltage is incremented; if less, a logic 0 is produced and the predictor is decremented. Sampling rates for DM are generally much higher than PCM encoding to improve sample-to-sample correlation and, therefore, the quality of the signal achieved with the 1-bit sample size.

The signal-to-noise (S/N) ratio of DM can be improved by adjusting the step size of the quantizer (ie, encoder). This improvement is achieved because the difference samples recorded in a differential encoding scheme also show some degree of correlation. That is, if difference sample "n" is large, it is very likely that difference sample "n + 1" will also be large. Therefore, it is possible to vary the amount the predictor voltage is incremented or decremented at each sampling interval in order to more accurately track the signal voltage. This encoding method is called adaptive delta modulation (ADM).

Data rates for the encoded speech signal can vary considerably in ADM and DM systems. The rate depends on the desired S/N ratio and, in the case of ADM, the sophistication of the algorithm used to vary the step size. One system implemented using an ADM algorithm was able to produce acceptable quality speech with a data rate of only 10k bits/s. The algorithm for controlling the step size, however, was complex and costly to incorporate.

A multibit quantizer permits sampling closer to the Nyquist rate. Using the encoder design for DM with a multibit encoder yields differential pulse code modulation (DPCM). If step size is allowed to vary as in ADM, the encoding method is called adaptive differential pulse code modulation (ADPCM). ADPCM has been found to produce quality speech using adaption algorithms which are simple and inexpensive to implement. Typical sample sizes are three or four bits, giving a data rate of 18k to 24k bits/s, respectively.

Various encoding techniques are compared in Fig 6*. The chart shows S/N ratio versus data rate in kilobits/second for three encoding methods: log pulse code modulation, adaptive delta modulation, and adaptive differential pulse code modulation.

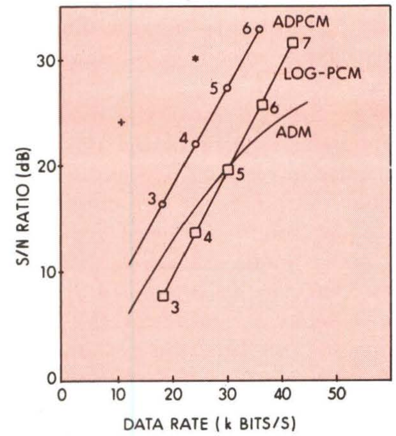


Fig 6 Comparison of signal-to-noise (S/N) ratio to data rate for several encoding methods. Note that ADPCM gives S/N improvement of almost 10 dB over log PCM for corresponding data rates. Two random data points represent S/N ratio as perceived in listening tests rather than with signal measuring hardware. Point labeled "*" represents ADPCM with a 4-bit sample size (24k bits/s) and "+" represents 10k bits/s ADM. Note that S/N ratio of ADM as perceived in listening tests is almost 20 dB better than its value obtained with signal measuring hardware (Courtesy of IEEE)

*From Rabiner and Schafer, Copyright 1976 by IEEE.

In itself the S/N ratio is not the final indicator of speech quality. Each encoding scheme introduces its own particular type of distortion. While contributing to a decrease in the S/N ratio, the distortion may not reduce the understandability of the reproduced speech. For example, noise introduced in reproduction of sounds like "th" would detract from the objective S/N ratio; however, since the sound produced for "th" resembles white noise, many kinds of noise introduced by the encoding algorithm can go unnoticed. Two data points in Fig 6 show relative quality of the speech as perceived by listeners for 4-bit ADPCM (the point labeled "*") and for the 10k-bit/s ADM system cited earlier ("+").

Analysis/Synthesis Systems

Waveform coding methods deal with time sampling of audio waveforms. Modest data rate improvements can be achieved by using some statistical properties of typical waveforms. Much greater reduction in bandwidth can be achieved by encoding speech with parameters based on a model for human speech production—the analysis/synthesis methods. While the possible parameters which can be encoded are many, an example coding scheme based on a particular set of parameters provides a basis for understanding the general concepts.

Every spoken language consists of a set of fundamental sounds called phonemes. These fundamental sounds are strung together to form consonant and vowel sounds which make up the spoken language. For example, the vowel sound "i" as in "bite" is produced by the phonemes "ah" and "ee." Most languages consist of less than 200 phonemes, with the number in common usage ranging from 50 to 60. Slight variations can be given to each phoneme by changing the stress (eg, angry, calm, or happy) and duration (how long the particular phoneme takes to pronounce). Stress does not vary by much at the phoneme level; limiting the stress to four different values is adequate to cover most speech. Duration for most phonemes is covered by a range of 25 to 100 ms. Using 15-ms steps from 15 to 240 ms (16 steps) is sufficient to satisfy duration range requirements.

A data rate can now be determined for this encoding method. Each encoded value contains three parameters: the encoded phoneme, its stress, and its duration. Since the number of phonemes is less than 200, the phoneme is encoded as an 8-bit integer. Stress, which can be one of four possible values, is encoded as a 2-bit number. Duration can have one of 16 possible values, thus requiring a 4-bit integer. This method gives a total of 14 bits for each encoded value or sample. Since phonemes are typically greater than 25 ms in duration, the number of samples per second will be 40 or less, giving a maximum data rate of 560 bits/s for an analysis/synthesis system that uses phonemes as the encoding parameter. Although bit rates can vary according to the parameters selected for the waveform encoding, it is clear that they are at least an order of magnitude less than their waveform coding counterparts.

Analysis/synthesis systems also offer a great deal of flexibility. A given word in any language can vary considerably in sound, depending on the context, that is, whether it occurs at the beginning or end of a sentence, and whether the sentence is a question or a statement. In waveform coding methods, either one recording of a word must be used in all contexts, affecting the naturalness of the speech, or many different recordings of a word must be used, requiring more storage. In analysis/synthesis methods it is possible to adjust the parameters, such as stress, to fit the context the word is spoken in.

While analysis/synthesis methods offer promise for both low bit rates and high flexibility, they suffer from some serious limitations. First, most equipment is more expensive than for waveform coding techniques. Second, while the speech quality is acceptable, its "unnatural" or "inhuman" sound may negatively affect understandability since listeners may pay more attention to the sound of the speech than to what is being said. Finally, methods for taking advantage of the inherent flexibility are still in the laboratory phase. Therefore, waveform coding techniques will continue to dominate the commercial market for at least the near future.

System Selection

The decision to buy or design a system for a particular application is made by examining the application in terms of the following requirements: vocabulary size, expected number of users, mode of interaction, and how the computer voice response system fits with existing applications (system structure).

Vocabulary Size

Vocabulary size is the most important variable in a CVR system. Its size determines the amount of storage required, and affects the decision of which waveform coding technique to use. A small vocabulary will indicate that a simple waveform coding technique, such as PCM, should be used since encoding and decoding hardware will represent most of the system cost. If a large vocabulary is chosen, a more complex system, such as ADM or ADPCM, can be used since the interface cost may be recovered through savings in storage requirements.

Vocabulary requirements for a given application can vary greatly; however, a minimum set of words and phrases exists which will handle the job. Any additional vocabulary usually is added merely to make a system more convenient to use. The upper limit on size will be determined by evaluating the system user and how much inconvenience he will tolerate.

Minimum vocabulary size is relatively easy to determine. For example, consider an inventory control system which accepts orders for particular items by part number and updates the available inventory for that item. A minimum vocabulary might contain 10 digits (0 to 9) to record part numbers, quantities, and prices; and several phrases to guide the user through the dialogue, such as "enter part number," "enter quantity," or "the price for the selected item is." Ten such phrases should be adequate. The resulting vocabulary would contain the 10 digits (0 to 9) and the 10 phrases. Digits require roughly 0.67 s each to speak, while the phrases may average about 2 s each. Thus, 10 x 0.67 or 6.7 s of speech are required for the 10 digits, and 2 x 10 or 20 s of speech for the 10 phrases, making the entire vocabulary requirement equal to 26.7 s of speech. Even when using PCM at 60k bits/s, total vocabulary storage requirement is only 200k bytes—a fraction of the storage on even the smallest disc systems currently available.

Maximum limit on vocabulary size is somewhat harder to determine, since the vocabulary for the example system could be increased for convenience without adding any new capabilities. For example, several phrases could be added to the vocabulary to ease the handling of incorrectly entered data. Actual part names, such as "size 14 rubber grommet," could be added to the vocabulary to give additional confirmation that the data are correctly entered. Including the entire alphabet allows spelling of abbreviations. For an inventory of 500 items, the additional vocabulary consists of about 10 extra phrases or 2 x 10 s, the 26 letters of the alphabet or 26 x 0.67 s, and 500 part names at about 2 s each for 500 x 2 s. The total vocabulary size in seconds of speech, including the 26.7 s from the minimum vocabulary, would be 1064 s. At 60k bits/s, the vocabulary would require approximately 7.98M bytes. Changing to ADPCM at 24k bits/s would lower this requirement to 3.19M bytes, a savings of 4.79M bytes. Additional cost of ADPCM decoding hardware would be made up if the saving in storage avoids the purchase of an additional disc drive.

Number of Users

A CVR system might be expected to support a number of users simultaneously. The number of users affects the throughput required from the vocabulary storage medium and total cost of decoding hardware. By determining the throughput required for voice response, the decision to use the unused capacity of existing system storage or a dedicated storage device can be made. Hardware costs for the decoders are easier to determine, since the cost is proportional to the number of decoders.

The number of simultaneous users to support is more difficult to determine than the vocabulary size. While most of the considerations are specific to each application, some general ones are outlined below. System usage can be divided into periods of time which are called "user sessions." Each session begins when a user gains access to the system and ends when the desired operations have been completed. In an inventory control system, for example, a session consists of a salesman accessing the system by typing a code or password and then entering and verifying several transactions.

Based on the particular application, the length of a typical user session is estimated. This estimation, coupled with the maximum number of user sessions that can be expected within a given period of time, determines the average number of sessions that might be active. Probability shows that the number of sessions concurrently active can exceed this average, since a session can begin at any random time a user gains access to the system. The exact number of users a system is designed to support must be based on expected average use and a factor to handle times when the load exceeds the average. In general, the concept is to attempt to guarantee that x% of all users will find the system available on their first attempt to access it. The exact value assigned to "x" depends on how costly waiting can be. In any system where the general public is the principal user, x must be close to 100 since excessive waiting time can mean lost customers.

Mode of Interaction

CVR systems can offer many modes of interaction. Level of interaction can vary from almost none, such as a single voice output for reporting status or emergency situations, to very heavy, as in the inventory control system.

Interaction can be classified as being in transaction mode or in batch mode. In transaction type interactions, the entire session consists of short user requests followed by short answers from the system, or the reverse. The amount of voice output occurring between user inputs will be on the order of a few seconds. The inventory control system represents a transaction mode interaction.

Batch type interaction involves a brief dialogue between the machine and user to determine what response is required. At the end of the dialogue, the system performs an information-search action, and then usually provides a long verbal report to which the user listens. The only interaction during this period may be special functions to permit pauses in output to give the user time to digest the information, or to skip information which may not be of interest. An example of batch mode interaction is a medical history system. Initial dialogue would determine the patient, data desired, and beginning and end dates for the data. After this brief dialogue, data reports would be given with no further interaction on the user's part.

Also related to mode of interaction are the physical devices used for the interaction. At one extreme, all users would have terminals specially designed to precisely fit the dialogue. At the other extreme, users would access the system using ordinary dial or touch-type telephones. In the latter case, dialogue would have to be specially tailored to the limitations of using an ordinary telephone as an interactive data entry terminal.

Use of telephones also poses data entry problems since the interaction must be structured to the telephone, rather than the reverse. Among the factors to be considered are problems imposed by a restricted character set, user frustration caused by excessively complex dialogues, and excessive amounts of user input before positive or negative feedback is obtained from the system. Unfortunately, since these user areas are very subjective and human-oriented, definite system recommendations beyond practical experience can not be made. While these factors have little effect on the overall design of a system, they do have a strong effect on user acceptance of the system.

System Structure

The above considerations define a CVR system as it appears to the user. The designer must also consider how the CVR system must interface to existing applications, both hardware and software. To do this, all demands placed on a system must be examined to determine the impact of adding voice response.

First to be examined is the number of decoder interfaces or voice channels required. This number is determined by number of users and mode of interaction. If batch interaction is planned, it is very likely that all users may require voice output at the same time. Therefore, number of channels will equal number of users. However, if the mode is transaction, and the length of a typical response from the system is comparable with the delay which can be tolerated by the user, a channel may be multiplexed over several users. A channel is assigned to a particular user for the duration of a response from the system; when the response is completed, the channel is free to be assigned to another user. Number of channels required is determined by considering the length of a typical response versus the time between responses, and the maximum tolerable delay. Exactly how these factors combine depends on the particular application; specific guidelines beyond practical knowledge are not conclusively adaptable. It should also be noted that multiplexing a hardware channel over more than one user requires sophisticated software techniques. Therefore, the expected cost of developing and supporting the software in this case is a major consideration in determining the feasibility of such an approach.

Next item to be examined is the vocabulary storage medium. Amount of storage required is determined directly by vocabulary size and encoding technique. Performance required from the storage is the product of the number of channels times the data rate for the encoding technique employed. This product value gives total throughput required from the storage medium. Throughput for a given medium is a function of its access time and the method used for buffering the device. Again, exact throughput is determined by the particular configuration, and specific guidelines cannot be readily derived.

After these factors have been established, the choice must be made between two basic approaches. First, the designer can add all required peripherals and software to an existing system by utilizing "excess" throughput available in the system. The second approach is to design a voice response "frontend" processor to handle all user input and voice output. The host computer is required only to retrieve information needed by the frontend processor.

Response time is a major item which must also be considered. A user can tolerate a minor amount of delay between making a request for information and the time when it is obtained. However, once the response begins, it must continue without interruption, because otherwise pauses can occur in mid-sentence or even in mid-word. This means that all input/output (I/O) operations required by the CVR system, such as disc accesses, must be given higher priority than other access requests; this could adversely affect response time of the application.

In general, using a frontend processor has the advantage of better response time and greater future expandability. Its major disadvantage is cost. The proper choice lies in carefully applying the above considerations to the particular application.

Automated Weather Information System

An automated weather information system has been developed by Input Output Computer Services, which typifies the implementation of a CVR system. This system is designed to serve as part of a Dept of Transportation development effort called the Flight Service Station Automation (FSSA) Program. Normally, general aviation users, such as private pilots, obtain weather information required to plan a flight by calling a Flight Service Station (FSS) attendant who must first access available weather information (eg, maps and reports) and then vocally provide the caller with the needed information. The FSSA program was initiated to curb projected future manpower requirements and associated costs for FSSs by using a CVR system to provide an interactive weather information system. Users would obtain the latest weather reports using a touch-type telephone as a data entry device. After keying in flight locations and other information required to obtain a report, the automated system would return with the desired weather report.

Vocabulary Size

The FSSA system needed a vocabulary size sufficient to adequately describe aviation weather. It had to include names of reporting stations and airports, cloud types, wind conditions, numeric entries, and words and phrases required to convey this information in common English language. In addition, the user-computer dialogue was to be guided by a series of instructions from the computer, all of which were to be stored as single phrases rather than individual words. These requirements resulted in a vocabulary size of 3500 to 4000 items. Most were individual words averaging a duration of about two-thirds of a second each.

Number of Users

The FSSA system was designed to support up to ten simultaneous users. This number was chosen arbitrarily, since the system was intended to prove the feasibility of a multiuser voice response system. Usage statistics, which would be collected online during system test would be used to more accurately determine the number of users for future systems.

Mode of Interaction

Users interact with the FSSA system using touch-type telephones as data terminals with their keypads serving as data entry devices. Alphanumeric data are entered using a special entry protocol which requires two keystrokes to define a single character. Input editing functions, such as "cancel last input," are also available.

A user session with the system consists of the dialogue to determine what information should be retrieved and the retrieval during which the weather information is presented to the user. Dialogue begins with a request for location codes—3-character abbreviations for weather reporting stations and airports. These codes entered by the user are typically points of departure and destination for a flight, as well as selected locations along the route of flight. Location codes are entered one at a time with a confirmation after each code, followed by a selection of the type of weather information required. In all, nine types of reports, such as surface observations, winds aloft, and weather warnings, are available. For some weather reports, only this information is required, and the dialogue would end. Other reports, however, require additional information; for example, winds aloft requires an altitude and a time, which would be requested at this time.

Weather reports are presented during the retrieval phase. At this time, the only interaction between user and CVR system is a set of special function commands. These commands are used to customize the presentation of data to the user's needs. Available functions include skipping reports, rereading reports, pausing, and ending the retrieval phase.

This mode of interaction is of the batch type described previously. Dialogue occurs at the beginning to select information to be presented, followed by the actual presentation when the user does little except listen. In this particular system, a brief dialogue could easily cause 15 min or more of a report to be presented for one user.

System Structure

First step in determining system structure was to choose the method of voice output and then to determine the demands for system resources that this selection would make. A study of technology available for CVR led to the selection of waveform coding over analysis/synthesis. Analysis/synthesis techniques, while holding future promise, cannot presently compete with the waveform coding technique for simplicity and speech quality.

Choice of the particular waveform coding technique was based to some extent on vocabulary size requirements. As mentioned, the vocabulary consisted of about 4000 words and phrases, each 0.67 s in duration. At a 6-kHz sampling rate, this results in about 4000 samples/word, or a total of 16M samples for the entire vocabulary. Selection of a coding technique with a small sample size was desirable, since a reduction of just 1 bit/sample would save 2M bytes of vocabulary storage. In addition, reduction of sample size decreased the throughput requirements for the vocabulary storage medium, which also lowered cost.

The waveform coding technique chosen was adaptive differential pulse code modulation (ADPCM) with a 4-bit sample size. ADPCM offered a data rate that was relatively low (24k bits/s), and a decoder interface which was simple to construct. Simplicity refers to the fact that the interface to the computer's I/O bus accounted for a sizable portion of the total cost of the decoder interface. Since the I/O bus interface was required regardless of the particular decoding method used, changing to a method simpler than ADPCM would not substantially reduce the cost of the interface.

Data rate for ADPCM could now be used to determine required performance for the vocabulary store. First, since the FSSA used a batch mode of interaction, it was not feasible to multiplex ADPCM interfaces over many voice channels. Therefore 10 interfaces would be used, giving a composite data rate of 240k bits/s for all 10 channels. This data rate, however, had to be combined with other factors such as available core buffer size and the likelihood of reading only partial disc blocks (a spoken word rarely occupies an integral number of blocks). The calculations were highly complex and are beyond the scope of this discussion.

Remaining functions (touch-type telephone signal decoding and message handling) required special interfaces and software, but had little impact on overall performance requirements. System structure was then dictated by the voice response requirements. Therefore,

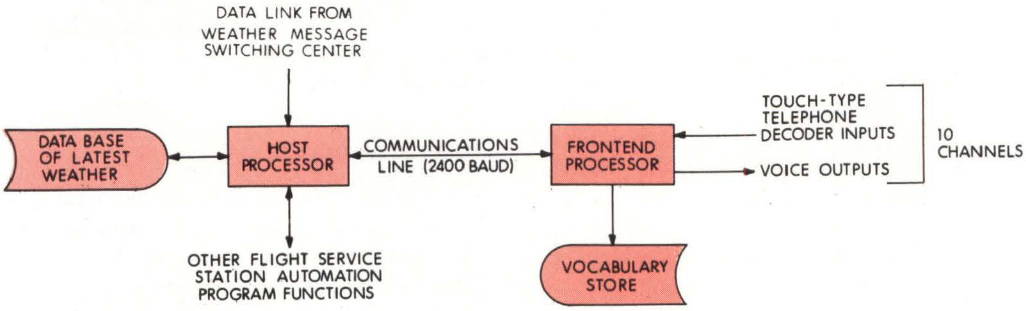


Fig 7 10-user computer voice response system. Host computer receives latest weather information from network link to national Weather Message Switching Center. Host maintains this information in data base used by many applications programs, including graphics displays, terminal printers, and voice response system. Frontend processor "fields" user requests for weather information and retrieves this information from host via communications line. Output data are then "spoken" using vocabulary of weather terms resident in frontend processor

a dedicated frontend processor was chosen to ensure the response time critical for voice output without substantially impacting response time for other applications. This resulted in a system with a voice response frontend computer handling all user-machine dialogue functions attached to a host computer. The host maintained the data base of current weather information, and handled the selective retrieval of that information (Fig 7). This configuration relieves the host of much of the work of supporting the voice response system, freeing it for other applications.

Conclusions

Computer voice response offers the system designer a means of making a complex machine system available to many unskilled users. The required data entry terminal (an ordinary telephone) is commonly available. While limited by human speech's serial presentation and lack of hard copy, the automated weather information system implementation shows that highly technical applications can be developed and put online quickly for users with no computer training.

While this discussion has presented some general guidelines for designing a CVR system, specific use of the guidelines is highly application dependent. Many issues are, therefore, addressed in only general terms. The automated weather information system serves to illustrate how the guidelines might be implemented in a real-world situation.

Computer voice response holds a promising future for many applications where the principal user is the nontechnical public. Waveform coding systems will continue to dominate applications which require immediate acceptance by the user. Analysis/synthesis systems require further advancement before they achieve their full potential.

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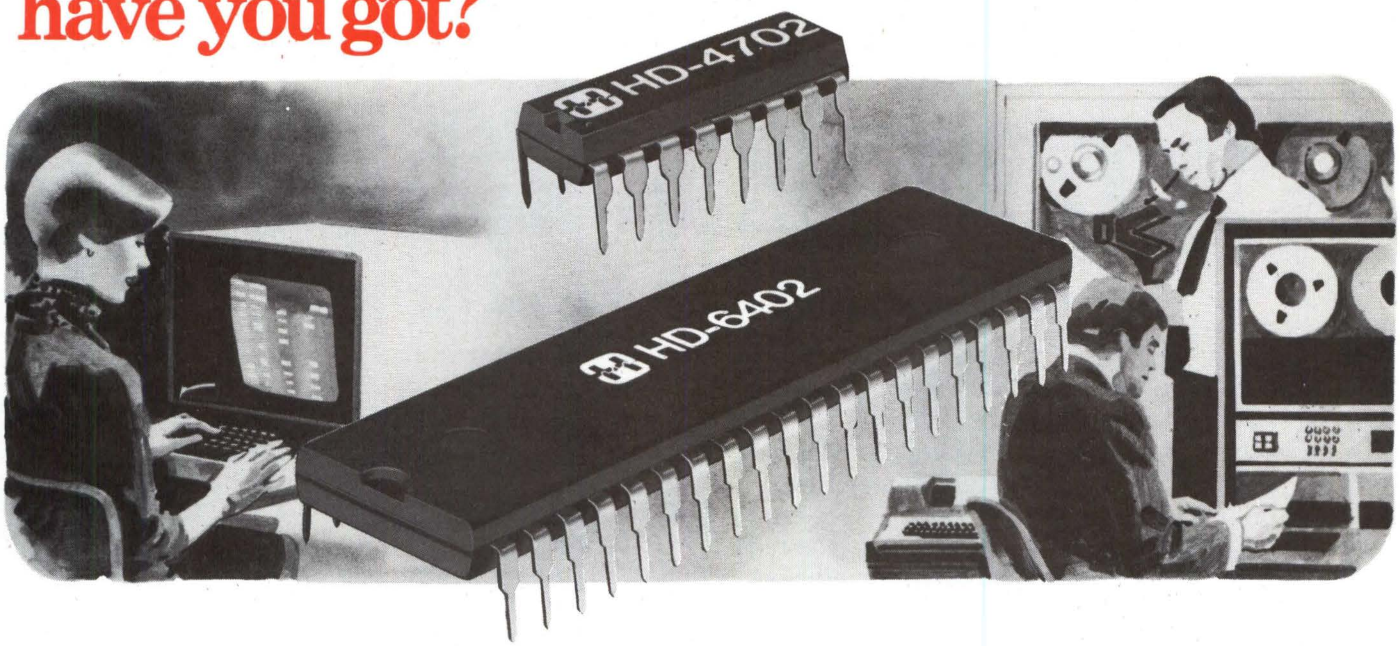

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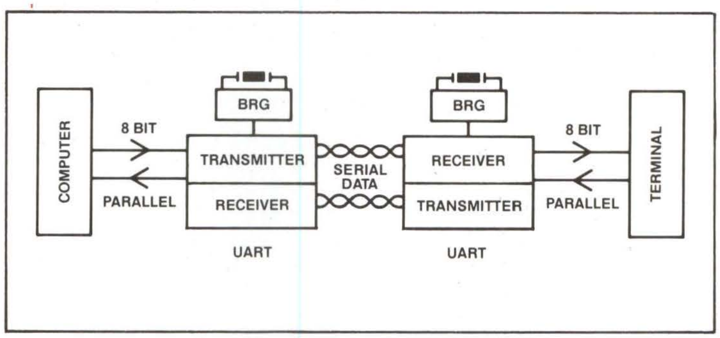

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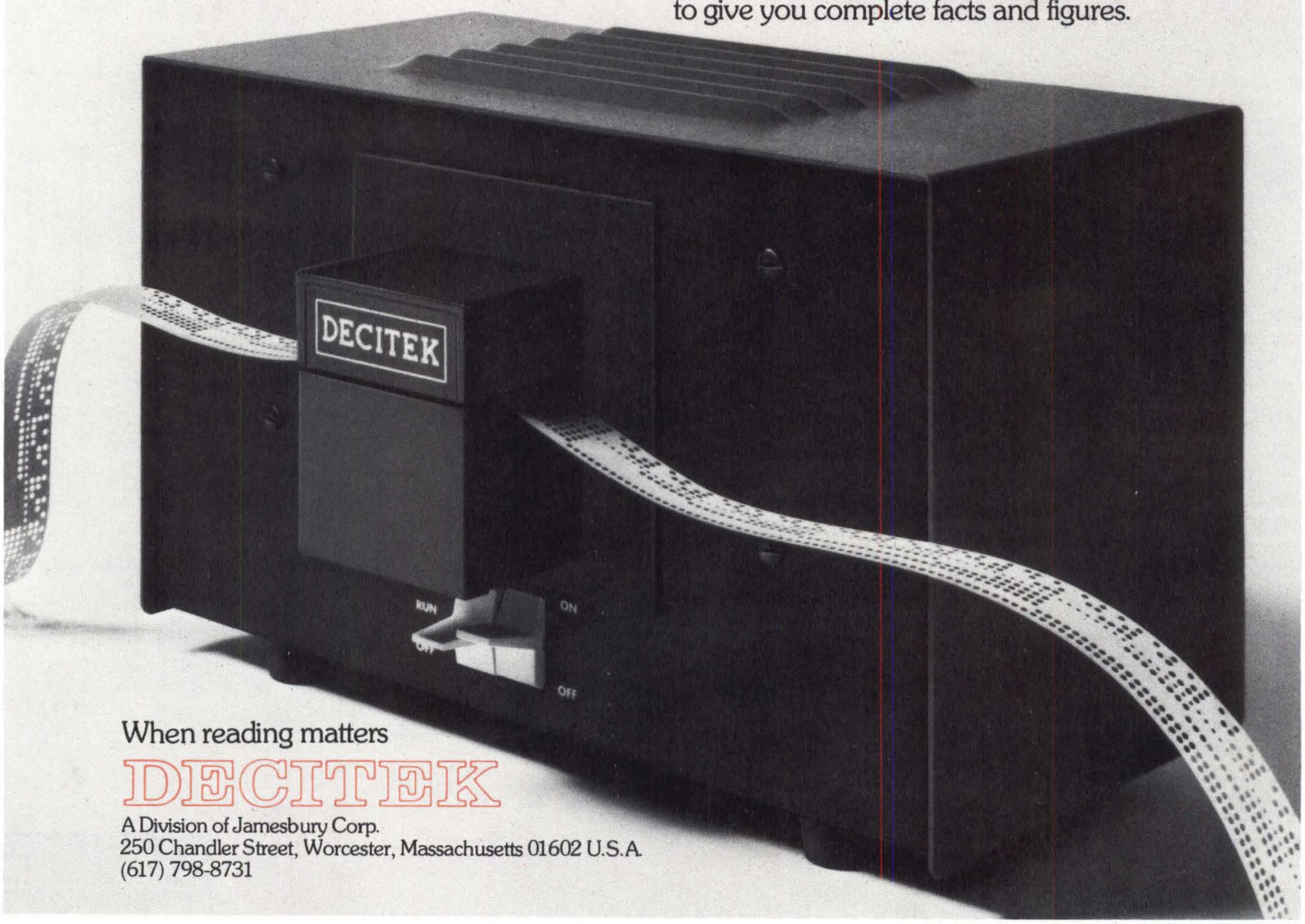

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Multiserver queuing models, coded for a handheld calculator, permit the evaluation of computer system performance, using powerful decision-making simulations to evaluate equipment, judge prospective reconfigurations, and modify existing operations

Computer Queuing Analysis On a Handheld Calculator

Ronald Zussman

Securities Industry Automation Corporation
New York, New York

Queuing theory can be practically applied to estimating computer performance and locating system bottlenecks. This is demonstrated by a generalized multiserver queuing model coded to run on the Texas Instruments SR-52 handheld calculator. The model is interactive so that effects of prospective design changes can be evaluated immediately, allowing an analyst to make the iterative design decisions required to optimize system effectiveness. Having the model preprogrammed for a portable calculator further increases its availability and convenience.

Where a complicated problem can be separated into a number of basic queuing situations, it is often possible to use this calculator model instead of an exten-

Multiserver Queuing Equations

Input Parameters

Average arrival rate:	λ
Average service rate:	u
Number of servers:	s

Performance Attributes

Facility utilization: $U = \lambda/us$

Probability of finding no items* in the system:

$$P(0) = 1/\left(\left(\sum_{N=0}^{s-1} (\lambda/u)^N/N!\right) + (\lambda/u)^s/(s!(1-U))\right)$$

Probability of finding n items* in the system:

$$P(n) = P(0)\ (\lambda/u)^n\ (1/n!) \qquad ,n < s$$

$$P(n) = P(0)\ (\lambda/u)^n\ (1/(s!\ s^{n-s})) \qquad ,n \geq s$$

Probability of finding all servers busy (ie, that $\geq$ s items are in the system):

$$B = \sum_{n=s}^{\infty} P(n) = (\lambda/u)^s\ P(0)/(s!(1-U))$$

Average waiting time in the queue:

$$TW = B/(su(1-U))$$

Average system response time (ie, total time an item spends in the system):

$$T = TW + 1/u$$

Standard deviation of system response time:

$$\sigma(T) = \sqrt{B(2-B) + s^2\ (1-U)^2}\ /(su(1-U))$$

$$\sigma(T) = \sqrt{B(2-B) + s^2\ (1-U)^2}\ TW/B$$

Probability of waiting time in the queue exceeding t:

$$P(TW>t) = B\ e^{-su(1-U)t}$$

Average number of items in the queue:

$$\overline{Q} = \lambda(TW)$$

Average number of items in the system:

$$\overline{N} = \lambda(T)$$

*Items in the system either reside in the queue or are being processed by one of the servers.

TABLE 1

SR-52 User Instructions for Multiserver Queuing Model

Step	Procedure	Enter	Press	Display
1.0	Load program card (sides A and B)			
2.0	Input parameters:			
2.1	Average arrival rate	λ	STO 0 1	
2.2	Average service rate	u	STO 0 2	
2.3	Number of servers	s	STO 0 3	
3.0	Calculate P(0) before proceeding to Step 4			
3.1	Probability that 0 items are in the system*		P(0)	Probability
3.2	Facility utilization of each individual server		U	Utilization
4.0	Request the following in any order			
4.1	Probability that n items are in system*	n	P(n)	Probability
4.2	Probability of finding all servers busy (Probability that ≥s items are in system)		B	Probability
4.3	Average waiting time in queue		TW	Time
4.4	Probability that waiting time in queue >t	t	P(TW>t)	Probability
4.5	Average system response time* (Total time item spends in system)		T	Time
	Standard deviation of system response time		RUN	σ(T)
4.6	Average number of items in queue		$\bar{Q}$	Number
4.7	Average number of items in system*		$\bar{N}$	Number

*Items are in system when they reside in queue or are being processed by one of servers

sive and expensive real simulation. Although the discussion concentrates upon computer central site queuing, this model also has wide application in communication systems and industrial engineering.

Assumptions

Several simplifying and yet conservative assumptions are used to derive the analytic equations listed as "Multiserver Queuing Equations." Random arrival and random service are assumed. All servers are considered identical, with the same capacity and equal loading. Dispatching is first-in first-out (FIFO). No input traffic is lost because all arrivals are queued until they can be serviced.

Mathematically, the input traffic rate is assumed Poissonian in nature, with interarrival times following an exponential distribution. These distributions are characterized as memoryless and their arrivals as random. For this type input, arrival probability is constant and traffic load is independent of time. This means that different input rates must be modeled individually. Another attribute of the Poisson distribution is nonzero interarrival time, which rules out the occurrence of simultaneous inputs. Lastly, arrivals are independent of past events and have no influence on future inputs.

The model assumes exponential service times, which are mutually independent, identically distributed, random variables. Service time specifications parallel those for input traffic, as stated previously. Exponentially distributed interarrival and service times are Erlang 1 distributions, a special case of the gamma function. Time periods are so widely fluctuating and random that the standard deviation equals the mean.

$$(\text{mean} \div \text{standard deviation})^2 = \text{Erlang } 1$$

Their coefficient of variation is also 1.

$$\text{coefficient of variation} = (\text{standard deviation} \div \text{mean}) = 1$$

Modeling with exponential distributions is a standard conservative approach. In contrast, simulations using constant arrivals and service times predict best-case performance with minimal queuing. Constant distributions are Erlang infinity with standard deviations of zero.

TABLE 2

SR-52 Coding Form For Multiserver Queuing Model

Loc	Code	Key	Comments	Loc	Code	Key	Comments	Loc	Code	Key	Comments
000	46	LBL	RCL	075	55	÷		150	95	=	
	19	D′			42	STO			22	INV	
	42	STO			00	0			23	ln x	
	01	1			06	6			65	X	
	09	9			05	5			46	LBL	B
005	36	IND		080	19	D′		155	17	B′	
	43	RCL			55	÷			06	6	
	01	1			03	3			19	D′	
	09	9			19	D′			65	X	
	56	rtn			29	x!			07	7	
010	46	LBL	U	085	85	+		160	19	D′	
	16	A′			07	7			55	÷	
	01	1			19	D′			03	3	
	42	STO			95	=			19	D′	
	00	0			20	1/x			29	x!	
015	05	5		090	42	STO		165	55	÷	
	01	1			00	0			05	5	
	19	D′			07	7			19	D′	
	55	÷			56	rtn			95	=	
	02	2			46	LBL	P(n)		56	rtn	
020	19	D′		095	12	B		170	02	2	σ(T)
	55	÷			90	if zro			75	—	
	42	STO			11	A			17	B′	
	00	0			42	STO			65	X	
	04	4			00	0			17	B′	
025	03	3		100	00	0		175	85	+	
	19	D′			75	—			03	3	
	95	=			03	3			19	D′	
	22	INV			19	D′			40	x^2	
	44	SUM			95	=			65	x	
030	00	0		105	80	if pos		180	05	5	
	05	5			87	1′			19	D′	
	56	rtn			00	0			40	x^2	
	46	LBL	P(0)		19	D′			95	=	
	11	A			29	x!			30	$\sqrt{x}$	
035	16	A′		110	41	GTO		185	55	÷	
	03	3			46	LBL			53	(	
	19	D′			87	1′			17	B′	
	75	—			48	EXC			65	X	
	01	1			00	0			41	GTO	
040	42	STO		115	03	3		190	13	C	
	00	0			45	y^x			46	LBL	$\bar{N}$
	07	7			48	EXC			10	E′	
	95	=			00	0			01	1	
	90	if zro			03	3			19	D′	
045	00	0		120	65	X		195	65	X	
	07	7			03	3			53	(	
	00	0			19	D′			46	LBL	T
	42	STO			29	x!			14	D	
	00	0			46	LBL			02	2	
050	00	0		125	46	LBL		200	19	D′	
	04	4			55	÷			20	1/x	
	19	D′			07	7			85	+	
	45	y^x			19	D′			46	LBL	TW
	43	RCL			55	÷			13	C	
055	00	0		130	04	4		205	02	2	
	00	0			19	D′			19	D′	
	55	÷			45	y^x			20	1/x	
	43	RCL			00	0			55	÷	
	00	0			19	D′			03	3	
060	00	0		135	95	=		210	19	D′	
	29	x!			20	1/x			55	÷	
	95	=			81	HLT			05	5	
	44	SUM			46	LBL	P(TW>t)		19	D′	
	00	0			18	C′			65	X	
065	07	7		140	65	X		215	41	GTO	
	58	dsz			03	3			17	B′	
	00	0			19	D′			46	LBL	$\bar{Q}$
	05	5			65	X			15	E	
	01	1			02	2			01	1	
070	04	4		145	19	D′		220	19	D′	
	19	D′			65	X			65	X	
	45	y^x			05	5			41	GTO	
	03	3			19	D′			13	C	
	19	D′			94	+/−					

Labels: A = P(0), B = P(n), C = TW, D = T, σ(T), E = $\bar{Q}$, A′ = U, B′ = B, C′ = P(TW>t), D′ = RCL, E′ = $\bar{N}$

Registers: 00 = dsz, n; 01 = λ; 02 = u; 03 = s; 04 = λ/u; 05 = 1-U; 06 = $(\lambda/u)^s$; 07 = P(0)

The model delivers realistic results, even when actual distributions deviate from exponential. Practical job scheduling algorithms introduce even greater randomness than the FIFO discipline assumed in the model. Empirical measurements indicate that although coefficients of variation may exceed 1 at the central processing unit (CPU), they are usually less than 1 for the input/output (I/O) peripherals. Fortunately, these departures from exponential distributions have opposite effects on computer system performance and tend to negate one another.

Validity of predicted results depends on the accuracy of a model's input data as well as on the adaptability of the model to the system being simulated. Determining input data using a monitor is the most accurate approach. Using a hardware monitor to measure input parameters and the same monitor to validate the model's predictions, such queuing models for IBM and Univac mainframes have proven correct to within 5%. More typically, performance can be predicted to an accuracy of 10% either way of observed values.

The Model

Challenges encountered in programming this model for the SR-52 calculator included the problems of trying to fit the code within 224 instruction steps, minimize calculator execution time, and provide convenient user operation. The resultant program, listed in Tables 1 and 2, is an optimal tradeoff between these three sometimes conflicting objectives.

Subroutines were used extensively to enable the code to fit into 224 program steps. However, as subroutines take more time to execute than inline code, they were avoided in iterative loops. To further speed execution, frequently used labels were placed in low address locations and absolute addressing was used wherever possible.

Ten user-defined functions can be executed by pressing the top row of keys on the SR-52 calculator. To provide maximum user convenience, these user-function keys are named and referenced as follows:

Key	Name	Key	Name
A	P(O)	A′	U
B	P(n)	B′	B
C	TW	C′	P(TW > t)
D	T, σT	D′	$\overline{-}$
E	$\overline{Q}$	E′	$\overline{N}$

With minor modifications this program is upward-compatible to TI-58 and -59 calculators, which use the same algebraic hierarchy and have the same number of user label keys as the SR-52. Using their additional program step capacity and companion PC-100A printer, the code can be expanded to print out alphanumeric messages for prompting and headings or to plot results.

Readers without access to TI calculators can use the multiserver model, by reprogramming the "Multiserver Queuing Equations" for whatever calculator is available.

The model requires input parameters λ, u, and s, which reflect characteristics of both workload and service facilities. As a preliminary step, these variables are stored in the calculator's memory registers. Then, as indicated in Table 1, "User Instructions," the simulation is run (Step 3.1) and any of the ten performance attributes listed in "Multiserver Queuing Equations" can be displayed.

Central Processor Simulation

Seven practical examples are given in Tables 3 and 4 to illustrate the technique for modeling CPU configurations. In Table 3, the three input parameters necessary for modeling are determined. In Table 4, the simulation results are listed.

One measure of processor speed is the time it takes to execute instructions. Average instruction execution time (AIET) depends on both the hardware and the software application. Scientific, business, and control system users have different AIETs on the same computer. To measure this value empirically, connect a counter to the instruction fetch strobe signal, then divide CPU active time by this instruction strobe count. The CPU in Table 3 has a given AIET of 1.072 μs. The reciprocal of AIET is the maximum number of instructions that can be executed by the processor in a unit time period. For modern full-scale computers, this number is so large that it is usually quoted in terms of millions of instructions per second (MIPS), which is the instruction execution rate for a saturated CPU running at 100% utilization. In this example, it is equal to 0.932836.

Before CPU service rate can be computed, the average number of instructions processed for each transaction or job must be established. Transactions are studied in real-time systems, while jobs are used for batch. If the system under investigation is still in the planning or design stage, the only way to proceed is to use a combination of time-consuming instruction counts (if code actually exists) and/or judicious estimating; this means tracing execution paths and actually counting or estimating the number of lines of code. The level of preliminary work done here will establish your confidence level in the simulation results. If the system is already operational, an exact count can be determined via a software accounting package, software monitor, or hardware monitor. Make certain that the final count includes instructions in the application code and a proportion of the operating system, utilities, and I/O handler overhead. In Table 3, the average number of instructions executed for each transaction is specified at 67,500.

CPU service rate is MIPS divided by the instruction-per-transaction overhead, then multiplied by 10^6 to keep units in line. In the previous example

$$\text{CPU service rate} = (0.932836 \div 67{,}500) \times 10^6$$
$$= 13.82 \text{ transactions/s}$$

Thus maximum CPU throughput is 13.82 transactions/s. At higher rates, queues continuously build, eventually outgrowing their buffers. Batch systems have their service rates quoted in jobs per second.

Two other parameters needed are number of servers and input transaction (or job) arrival rate. Number of servers (s) is taken equal to the level of multiprocessing. In uniprocessor configurations s = 1. For multiprocessors, where s is greater than 1, the model uses the actual overall arrival rate. In multiple uniprocessor configurations, only one CPU is modeled and input transactions are assumed to be uniformly distributed to all pro-

TABLE 3

Determining Input Parameters For Modeling CPU Configurations

Configuration	Total No. CPUs	Transaction Arrival Rate (per second)	CPU Service Rate (per second)	Model Input Parameters λ	u	s
2-CPU multiprocessor	2	25.00	13.82	25.00	13.82	2
3-CPU multiprocessor	3	25.00	13.82	25.00	13.82	3
4-CPU multiprocessor	4	25.00	13.82	25.00	13.82	4
2 uniprocessors	2	25.00	13.82	12.50	13.82	1
3 uniprocessors	3	25.00	13.82	8.33	13.82	1
4 uniprocessors	4	25.00	13.82	6.25	13.82	1
1 CPU (100% faster)	1	25.00	27.64	25.00	27.64	1

AIET = 1.072 μs

$$\text{MIPS} = \frac{10^{-6}}{\text{AIET}} = \frac{1}{1.072} = 0.932836$$

Average number of instructions-executed-per-transaction = 67,500
(Includes application + operating system + utilities + I/O handler)

CPU service rate = MIPS x 10^6 ÷ (instructions/transaction)

$$= \frac{932{,}836}{67{,}500} = 13.82 \text{ transactions/s}$$

TABLE 4

Queue Statistics (for CPU Configuration in Table 3)

Simulation Results

Configuration	U	P(0)	P(1)	P(2)	B	TW	P(TW>.1)	T	σ(T)	$\bar{Q}$	$\bar{N}$
2-CPU multiprocessor	0.9045	0.0502	0.0907	0.0821	0.8591	0.3254	0.6598	0.3978	0.3819	8.1356	9.9446
3-CPU multiprocessor	0.6030	0.1443	0.2610	0.2361	0.3586	0.0218	0.0691	0.0941	0.0861	0.5446	2.3536
4-CPU multiprocessor	0.4522	0.1601	0.2896	0.2619	0.1304	0.0043	0.0063	0.0767	0.0742	0.1077	1.9166
2 uniprocessors	0.9045	0.0955	0.0864	0.0781	0.9045	0.6852	0.7926	0.7576	0.7576	8.5652	9.4697
3 uniprocessors	0.6027	0.3973	0.2394	0.1443	0.6027	0.1098	0.3481	0.1821	0.1821	0.9146	1.5173
4 uniprocessors	0.4522	0.5478	0.2477	0.1120	0.4522	0.0597	0.2121	0.1321	0.1321	0.3734	0.8256
1 CPU (100% faster)	0.9045	0.0955	0.0864	0.0781	0.9045	0.3426	0.6946	0.3788	0.3788	8.5662	9.4697

cessors. Therefore, arrival rate to the one modeled CPU is the overall arrival rate divided by the number of uniprocessors.

Computers often process several distinct classes of input simultaneously. When this occurs, these different classes may be combined and modeled as one representative type of input. The example in Table 5 shows how to merge three transaction types: inquiries, orders, and reports. Total arrival rate is a summation of individual arrivals:

17.0 + 20.0 + 4.5 = 41.5 transactions/s

The equivalent instructions-executed-per-merged transaction is weighted average, based upon relative arrival frequency and instructions-executed-per transaction:

(0.41 x 1500) + (0.48 x 6700) + (0.11 x 74,000)
= 11,971 instructions/transaction

As previously discussed, CPU service rate is computed by multiplying the given 0.500000 MIPS rate by 10^6 and then dividing this product by 11,971 instructions/transaction, yielding a result of 41.8 transactions/s.

Once input parameters are known for the merged transaction, a calculator simulation can be run to determine queue statistics.

When facility utilization exceeds 80%, both queue size and waiting time increase exponentially. The processor of Table 5 has a utilization just below 100% (U = 0.9928). This is too busy for satisfactory performance. Almost all of the 138.3333 transactions in the system ($\bar{N}$) are immobilized in the queue. Simula-

TABLE 5

Merging Transaction Types Into One Equivalent Transaction

MIPS = 0.500000

Three Transaction Types	Arrival Rate (per second)	Relative Arrival Frequency	Instructions Executed per Transaction	CPU Service Rate (per second)	CPU Utilization U
Inquiry	17.0	0.41	1,500	333.3	0.05
Order	20.0	0.48	6,700	74.6	0.27
Report	4.5	0.11	74,000	6.8	0.66
Totals	41.5	1.00			0.98

One Equivalent Transaction

Arrival rate = 41.5 transactions/s

Instructions/transaction = (0.41 x 1500) + (0.48 x 6700) + (0.11 x 74,000) = 11,971

CPU service rate = 500,000 ÷ 11,971 = 41.8 transactions/s

Model Input Parameters			Simulation Results				
λ	u	s	U	TW	T	$\bar{Q}$	$\bar{N}$
41.5	41.8	1	0.9928	3.3094	3.3333	137.3405	138.3333

tion predicts 137.3405 transactions queued ($\bar{Q}$), each waiting for an average of 3.3094 s (TW). Overall response time (T) is 3.3333 s. Therefore, only 3.3333 − 3.3094 = 0.0239 s are actually consumed for processing. Most of the response time (3.3094 ÷ 3.3333 = 99.28%) is spent waiting; only 0.72% is used in obtaining actual service.

While it is cost-effective to make good use of hardware, always consider the tradeoffs of adequate response time and realistic buffer size. No system can be expected

TABLE 6

Modeling Preemptive Priority Queue Disciplines

Three Transaction Types	Priority Level	Arrival Rate (per second) λ	Instructions Executed per Transaction	MIPS (for Subdivided Models)	CPU Service Rate (per second) u	U Subdivided Models
Inquiry	high	17.0	1500	0.500000	333.3	0.05
Order	medium	20.0	6700	(1-0.05) (0.500000) = 0.475000	70.9	0.28
Report	low	4.5	74,000	(1-0.05) (1-0.28) (0.500000) = 0.342000	4.6	0.98

Subdivided Models

Three Transaction Types	Model Input Parameters			Simulation Results					
	λ	u	s	U	TW	T	Throughput 1/T	$\bar{Q}$	$\bar{N}$
Inquiry	17.0	333.3	1	0.0510	0.0002	0.0032	316.3000	0.0027	0.0537
Order	20.0	70.9	1	0.2821	0.0055	0.0196	50.9000	0.1108	0.3929
Report	4.5	4.6	1	0.9783	9.7826	10.0000	0.1000	44.0217	45.0000

to operate safely with a facility utilization above 80% anywhere in the processing chain (CPU or channels). At high utilizations, any small increase in arrival rate or deviation of distribution may result in severely degraded performance. Data can be lost because of overflowing buffers or the system can be brought down entirely.

Until now, different transaction types have been implicitly assumed to be at the same priority level. However, modeling need not be so restricted. Table 6 develops the concept of job stream priorities. The approach is to subdivide one computer into a number of separate pseudomachines, one processing each transaction type, and each with its own MIPS rate. These pseudomachines are modeled independently to determine performance characteristics for the various classes of input.

Since Table 6 considers three transaction types, three pseudocomputers are modeled. Inquiries receive precedence and are given the full benefit of the 0.500000 MIPS. CPU service rates, for the pseudoprocessors, are calculated by multiplying their respective MIPS by 10^6 and then dividing by instructions per transaction. For inquiries, this service rate calculation is

$0.500000 \times 10^6 \div 1500 = 333.3$ inquiries/s(u)

Once λ, u, and s are determined for the pseudoprocessors, the model can be run to display their queue statistics. Such simulation indicates that the inquiry processing pseudocomputer is only 5% utilized (U). Table 6 also lists waiting time (TW), response time (T), throughput (1/T), and queue length ($\bar{Q}$, $\bar{N}$) statistics.

Order processing ranks second, having preemptive priority over reports. The MIPS available to orders (0.475000) is computed by multiplying the original MIPS rate (0.500000) by the inverse of CPU utilization for the inquiry pseudoprocessor:

(0.500000) x (1− inquiry CPU utilization)

$= (0.500000) \times (1 - 0.05) = 0.475000$ instructions/s

The third pseudocomputer, for reports, gets whatever MIPS is left over (0.342000). This computation is analogous to the one for orders.

(0.475000) x (1 − order CPU utilization)

$= (0.475000) \times (1 - 0.28) = 0.342000$ instructions/s

Resulting queue statistics, in Table 6, are valid performance indicators for the three transaction types. However, utilization of the actual processor remains to be resolved. The percentage of real CPU utilization, contributed by each input class, is calculated by multiplying arrival rate by instructions per transaction and then dividing by the product of the overall 0.500000 MIPS rate times 10^6.

		CPU Utilization
Inquiry:	$(17.0 \times 1500) \div (0.500000 \times 10^6)$ =	5.1%
Order:	$(20.0 \times 6700) \div (0.500000 \times 10^6)$ =	26.8%
Report:	$(4.5 \times 74{,}000) \div (0.500000 \times 10^6)$ =	66.6%
	Total	98.5%

Combined CPU utilization for inquiry and order processing is only 5.1% + 26.8% = 31.9%. This indicates that inquiries and orders are processed more expeditiously than in the single priority system of Table 5. Report processing, having lowest priority, is degraded the most. Average report queue length ($\bar{Q}$) is 44.0217, and mean response time (T) is 10.0000 s.

Subdividing one computer into a number of pseudoprocessors assumes smooth and homogeneous CPU execution for transactions of all priority levels. However, in practice, CPU activity occurs in bursts interspersed with idle periods. Modeling errors will be small so long as either (1) instruction overhead for high priority transactions is shorter than for those of lower priority and/or (2) high priority transactions only lightly load the system. The degree to which these two assumptions are met determines result accuracy.

In Table 6, errors caused by our homogeneous processing assumption are less than 5%. Conditions ensuring accurate results are:

Instructions Per Transaction	Inquiry < Order < Report
	1500 < 6700 < 74,000
CPU Utilization	Inquiry + Order = 31.9%

Similar stipulations can be expanded to any number of priority classes. Generally, high priority transactions and jobs have shorter instruction execution paths than those of lower priority. In practice, preemptive priority queue modeling is applicable and its results are realistic. Case histories have been documented in which such pseudoprocessor analytic models were as accurate as discrete simulation packages which had run and accumulated statistics for many thousands of transactions.

Disc and Drum Channel Simulation

Five examples of channel configurations are given in Tables 7 and 8. Table 7 develops the three input parameters (λ, u, s) needed for modeling. Queue statistics resulting from these simulations are listed in Table 8.

Throughput capacities for three types of drums are computed in the upper half of Table 7. All quoted times and rates represent averages. Access time includes seeking and rotational delay. Drum seek times are always zero because heads are fixed and stationary. Average rotational delay (latency) is the time consumed by one-half a disc or drum revolution. Data transfer time depends on the physical characteristics of the device, r/min, and bit-packing density, as well as on blocking size. Adding access to data transfer time results in I/O service time. The reciprocal of service time is service rate u, the maximum possible number of device I/O operations per second.

When different classes of transactions reference the same I/O device, the relative frequency of their accesses is used to compute a weighted average block size. This is done by multiplying the block size of each transaction

TABLE 7

Modeling Channel Configurations

Drum Type	Access Time(s)	+ Transfer Time/Byte(s)	x Bytes/Transfer	= Service Time per I/O(s)	Service Rate(/s)
	Channel Characteristics				
A	0.01700	4.25×10^{-6}	560	0.019380	51.60
B	0.00425	4.25×10^{-6}	2048	0.012954	77.20
C	0.09200	7.00×10^{-6}	384	0.094688	10.56

Example	Drum Type	Channel Configurations Description	Total No. Channels	I/O Rate/s	Model Input Parameters λ	u	s
1	A	1 single channel	1	22.20	22.20	51.60	1
2	B	2 single channels	2	150.00	75.00	77.20	1
3	B	1 dual channel	2	150.00	150.00	77.20	2
4	C	4 single channels	4	4.32	1.08	10.56	1
5	C	2 dual channels	4	4.32	2.16	10.56	2

TABLE 8

Queue Statistics (for Channel Configurations in Table 7)

Example	Model Input Parameters λ	u	s	Simulation Results U	P(0)	P(1)	P(2)	B	TW	P(TW>0.1)	T	σ(T)	$\bar{Q}$	$\bar{N}$
1	22.20	51.60	1	0.4302	0.5698	0.2451	0.1055	0.4302	0.0146	0.0227	0.0340	0.0340	0.3249	0.7551
2	75.00	77.20	1	0.9715	0.0285	0.0277	0.0269	0.9715	0.4416	0.7796	0.4545	0.4545	33.1194	34.0909
3	150.00	77.20	2	0.9715	0.0145	0.0281	0.0273	0.9575	0.2176	0.6166	0.2306	0.2274	32.6407	34.5837
4	1.08	10.56	1	0.1023	0.8977	0.0918	0.0094	0.1023	0.0108	0.0396	0.1055	0.1055	0.0117	0.1139
5	2.16	10.56	2	0.1023	0.8144	0.1666	0.0170	0.0190	0.0010	0.0028	0.0957	0.0952	0.0022	0.2067

type by the percent of accesses attributable to that transaction type. Summing all these products gives the weighted average block size. Then, device service rate is calculated as shown in Table 7. Multiplying average block size by the transfer time per byte and adding access time gives the service time per I/O, the reciprocal of which is service rate (u).

Peripherals having the most influence on system performance are mass data storage discs and drums. Channel configurations interface sets of these I/O devices to the CPU. A one-path interconnection is interpreted as a "single" channel; two access paths represent a "dual" channel, where any two peripherals in the set can be accessed simultaneously.

Drum channel queuing is more pronounced than queuing at the device level; so rather than model individual peripherals, aggregate channel activity is considered. A channel is in use for the total busy time of all drums accessed through it. The underlying supposition is that both a drum and its channel are seized and released simultaneously. Queues form when all channel access paths to a device are in use. "Single" channels are represented by one queue and one server. A "dual" channel is modeled as two servers replenished from one queue.

Channel service rate is determined by the peripherals interfaced, and equates directly to drum service rate in Table 7 because all drums on each channel have identical specifications. In practice, there may be cases where the same channel is used by several different types of drums. Channel service rate is then an average of drum service rates, weighted according to frequency of drum accesses. This is calculated by multiplying the service rate of each drum on the channel by the percent of channel accesses attributable to that drum. Channel service rate is the sum of these products.

Selector channels handling command-chained channel programs are busy during the total time that their discs

TABLE 9

Determining Optimum Multiprogramming Level For Computer System

Model Entire Multiserver CPU (where each initiator is a server)						Drum Type B on One Dual Channel					Total System	
Number of Initiators N	λ	u	s	U	Response Time T_1	λ	u	s	U	Response Time T_2	Response Time $T=T_1+T_2$	Message Throughput $N \div T$
1	3	40.00	1	0.0750	0.0270	1.5	77.20	2	0.0097	0.0130	0.0400	25.03
2	6	20.00	2	0.1500	0.0512	3.0	77.20	2	0.0194	0.0130	0.0642	31.17
3	9	13.33	3	0.2250	0.0761	4.5	77.20	2	0.0291	0.0130	0.0891	33.68
4	12	10.00	4	0.3000	0.1013	6.0	77.20	2	0.0389	0.0130	0.1143	35.00
5	15	8.00	5	0.3750	0.1269	7.5	77.20	2	0.0486	0.0130	0.1399	35.74
6	18	6.67	6	0.4500	0.1530	9.0	77.20	2	0.0583	0.0130	0.1660	36.15
7	21	5.71	7	0.5250	0.1800	10.5	77.20	2	0.0680	0.0130	0.1930	36.27
8	24	5.00	8	0.6000	0.2087	12.0	77.20	2	0.0777	0.0130	0.2217	36.08
9	27	4.44	9	0.6750	0.2410	13.5	77.20	2	0.0874	0.0131	0.2541	35.43
10	30	4.00	10	0.7500	0.2807	15.0	77.20	2	0.0972	0.0131	0.2938	34.04
11	33	3.64	11	0.8250	0.3389	16.5	77.20	2	0.1069	0.0131	0.3520	31.25
12	36	3.33	12	0.9000	0.4600	18.0	77.20	2	0.1166	0.0131	0.4731	27.48
13	39	3.08	13	0.9750	1.2227	19.5	77.20	2	0.1263	0.0132	1.2359	10.52
14	42	2.86	14	1.0500	—	21.0	77.20	2	0.1360	0.0132	—	—

and drums are active; this includes seek (arm movement), latency (rotational delay), and data transfer times. Access time is the sum of seek and latency. Drums, having fixed heads, always have a seek time of zero. Once access time is established, channel calculations are made as in Table 7.

If one disc channel program initiates a standalone seek and a second channel program initiates a data transfer operation (after the seek is complete), the selector channel is freed during the seek operation and its access time is equal only to latency. The tradeoff is the additional overhead caused by the extra interrupt and I/O supervisor processing which needs to be added to the CPU model.

Block-multiplexer channels are more efficient because they automatically disconnect during seeks, even with only one command-chained channel program. Utilization of a disc block-multiplexer channel can be as low as one-half or one-third of the combined utilizations of its individual discs. Disc block-multiplexer channels are modeled by proceeding as indicated in Table 7 without adding disc seek time into access time. Block-multiplexer channels with "rotational position sensing" are also free during latency and their access time is therefore zero.

Rules for representing channel arrival rates (λ) and number of servers (s) are similar to those for CPUs. Single channels are modeled as one server. λ is the total I/O arrival rate divided by the number of single channels. Only one of the single channels in the group is actually simulated, with its results applying to all. A dual channel is modeled as two servers fed from one queue; dividing the total I/O arrival rate by the number of dual channels computes to λ. Table 7 provides additional details.

The model assumes an absence of dual channel device lockouts, attempting to simultaneously use one peripheral device via each of the two access paths. One request is blocked until completion of the other. With a number of I/O devices on each channel and an even distribution of files, the probability of device lockout is small. Instances of high probability are best represented by the single channel model.

Central Site Modeling

When transation flow can be approximated by sequential queues, CPU and channel models can be consolidated. Total central site response time is estimated by summing response times for processor and each appropriate channel.

Table 9 shows how to determine the optimum number of initiators. This example is a CPU and drum channel system with two queues in series. Total transaction response time (T) is computed by adding together computer (T_1) and drum channel (T_2) response times. Dividing the number of initiators (N) by this total response time (T) approximates a theoretical system throughput capacity.

The processor is multiprogrammed with initiators modeled as individual servers. Total CPU service rate remains fixed at 40.00 transactions/s. Number of initiators corresponds to level of multiprogramming. An increasing number of servers is balanced by a diminished processing power allocated per server. Each initiator is consigned a service rate (u) of $40.00 \div N$.

The goal is maximizing real transaction throughput for the system. This corresponds to the maximum transaction arrival rate (λ) which can be handled. The last column in Table 9 lists a theoretical system throughput capacity ($N \div T$). Optimal real system throughput is the highest transaction arrival rate which satisfies the relationship $\lambda \leq (N \div T)$. In Table 9 the best choice for N is 10 ($\lambda = 30$ and $N \div T = 34.04$); at this point, the CPU arrival rate and theoretical system throughput capacity curves effectively intersect. Higher traffic rates cannot be supported by the system and will result in queue backup and overflow. For example, at $N = 11$, arrival rate (λ) of 33 transactions/s is higher than the theoretical system throughput capacity ($N \div T$) of 31.25 transactions/s.

Total system throughput depends on both processor and drum I/O. As the number of initiators is increased, the CPU saturates much more rapidly than the channel. At $N = 11$, CPU utilization has already reached 82.5% while channel utilization is only 10.69%. The computer determines the level of multiprogramming, and its utilization controls the shape of the theoretical system throughput capacity curve. Drum hardware characteristics establish a lower bound ($T_2 = 13$ ms) on system response time.

Summary

The generalized computer system simulation package presented can evaluate any level of multiprogramming and multiprocessing with any combination of interactive and batch workloads. Elaborate queuing formulas have been reduced to a simple technique for efficiently evaluating complex systems on a programmable calculator.

A wide range of problems facing manufacturers of mainframes and peripherals as well as end-users can be addressed. The impact of hardware configuration changes and software modifications on performance can be anticipated. The effect of totally new hardware, improvements to existing machines, and the interplay of components can be assessed. The consequences that projected increases in a system's online workload will have on response times, batch throughput, and turnaround times can be predicted. Bottlenecks that are likely to arise as workload increases can be located.

Before using the model, the computer designer merely characterizes system resource demands and capabilities with a small set of easily researched parameters, determined by some combination of monitor measurements, estimates, or design specifications. Pressing a few calculator keys simulates the effect of job contention for processor and I/O, predicting the performance of any computer system. With such a queuing model, the programmable calculator becomes a convenient and indispensable tool for predicting and optimizing system performance.

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Ronald Zussman, currently senior consultant and project leader of computer measurement and evaluation at SIAC, has experience that includes development of interactive models of shipboard computer systems and a prototype of an automated trading post. He holds BSEE, MSEE, and professional EE degrees from Pratt Institute, New York University, and Columbia University, respectively.

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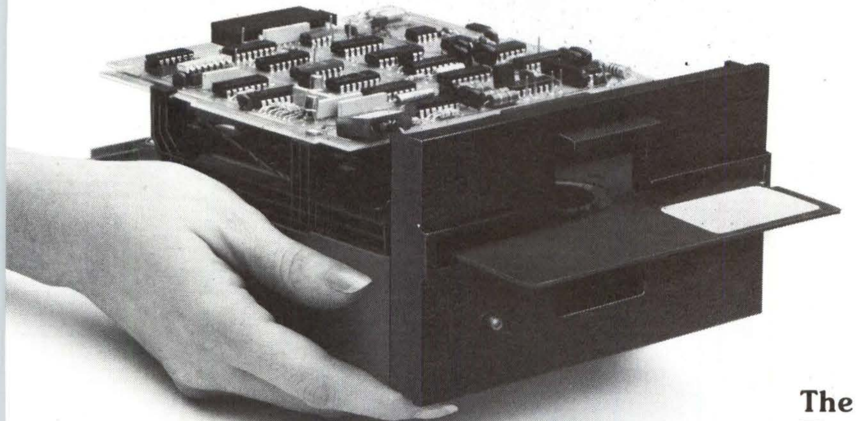

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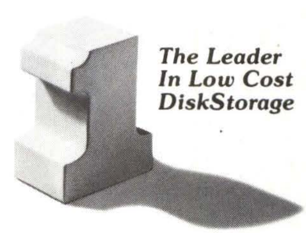

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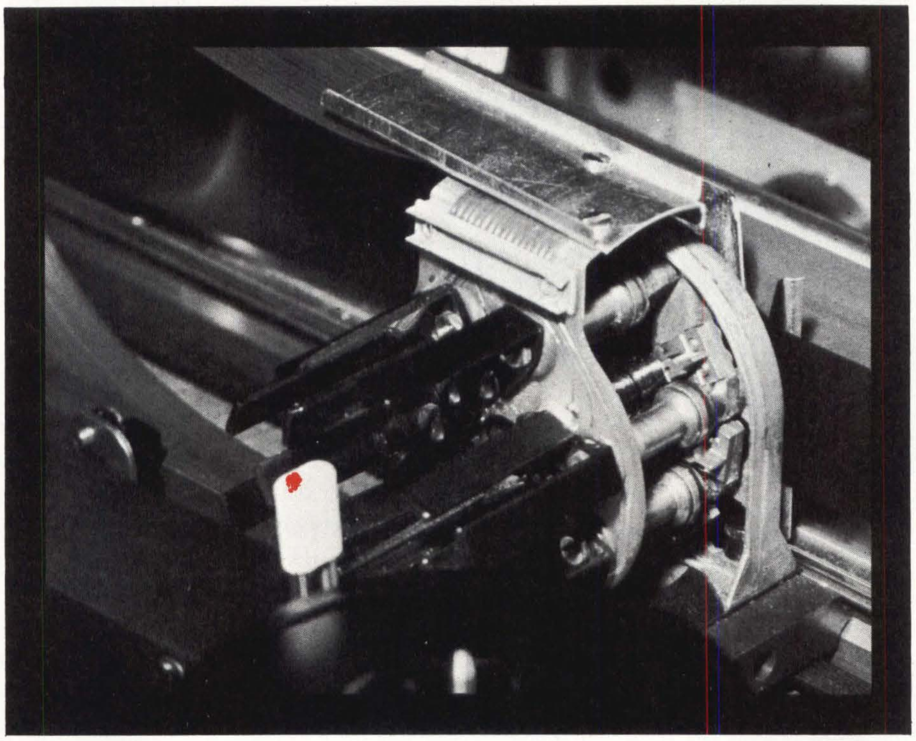

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Various magnetic tape transport speeds, track configurations, and read/write densities are automatically software-controlled by a universal buffered tape formatter that incorporates a high speed oriented microcomputer and offers IEEE-488 interface compatibility

Magnetic Tape Formatter Design Reduces Hardware/Software Requirements

A. Scott McPhillips

Information Development & Applications, Incorporated
Beltsville, Maryland

A universal buffered tape formatter resolves the recurring disadvantages of demand-designing tape interfaces, resulting in lower cost, increased adaptability and reliability, and expanded capability. Incorporating a microprocessor, which provides significant economies by greatly simplifying interface hardware and tape handling software, the formatter is plug-compatible with most existing devices that interface to magnetic tape.

Interfacing this buffered formatter to a data or instrumentation system is simplified since the formatter is compatible with the IEEE-488 standard interface. This general-purpose interface bus (GPIB) is now available on many minicomputers, programmable calculators, instruments, and other data handling devices. Thus, the buffered formatter is automatically plug-compatible with a majority of the existing devices that must be interfaced to magnetic tape. For noncompatible data devices, it is easier and less expensive to add a GPIB interface than to add a conventional tape interface. In addition, the GPIB interface provides device-compatibility to present as well as future data processing systems and instruments.

The industry's highly standardized tension-arm magnetic tape transports are available in several speeds, track configurations, and recording densities. This diversity of timing and format requirements causes present tape formatters to be complex and expensive. A typical formatter designed with transistor-transistor logic (TTL) requires 125 integrated circuits (ICs) to handle standard tape densities through 800 bits/in and another 125 ICs if it is to handle 1600-bit/in tapes as well. In contrast, the microprocessor-based buffered formatter (Fig 1) uses 80 chips to duplicate all functions of an 800-bit/in formatter. Provisions are also made for adding an optional 50-chip board to convert to 1600-bit/in operation.

In addition to this factor-of-two parts reduction, the microcomputer approach provides even more significant economies by greatly simplifying the interface hardware and tape handling software in the data system that controls the formatter. The microcomputer buffer memory allows incremental writing and reading. This removes all timing constraints on the external system and often avoids the need for a direct memory access (DMA) controller. The GPIB interface is already available in many systems, avoiding the need for any custom interface design. The microcomputer can be directed to search a tape to find a desired data block or file, freeing the system processor of this time-consuming task. Most important, microcomputer software can automatically handle all error detection and recovery procedures, completely relieving system software of these details.

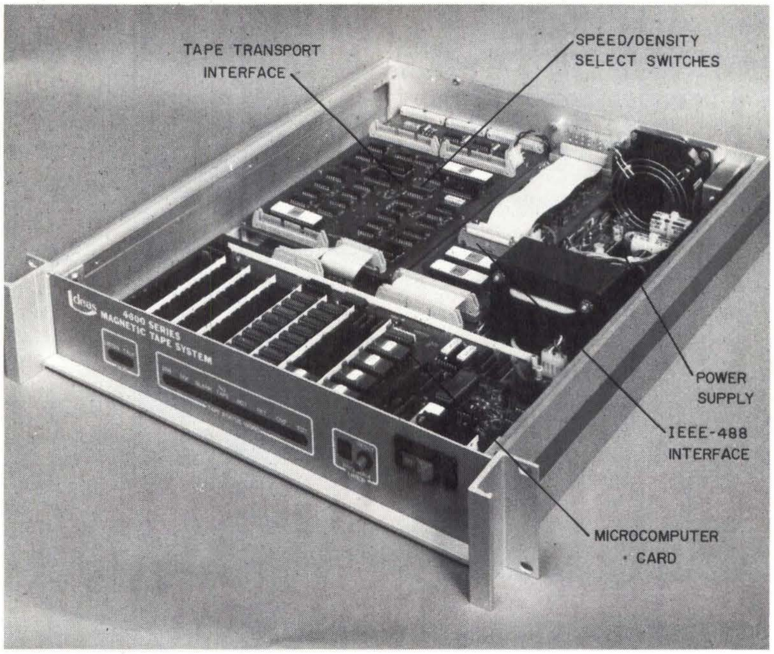

Fig 1 Buffered magnetic tape formatter. Microprocessor performs tape timing, data buffering, and formatting. Parts count is only about half that of conventional unbuffered formatters, even though system includes such extra capabilities as tape searching and automatic error correction. Wide card in front contains microcomputer and buffer memory expansion sockets. Tape interface board (rear left) includes "poor man's DMA" controller. Other boards are IEEE-488 interface and power supply

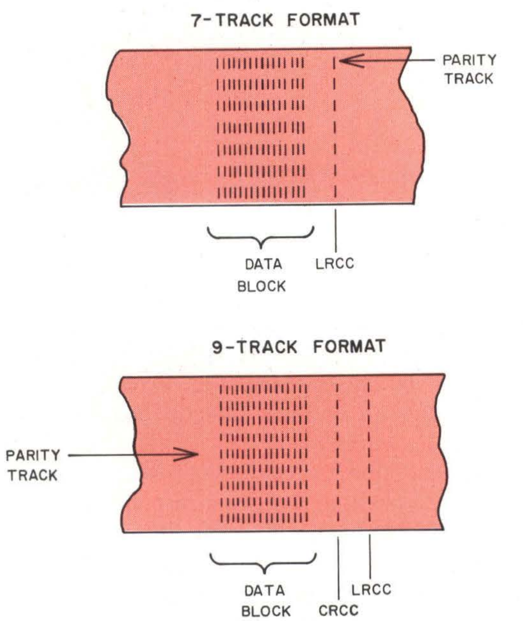

Fig 2 Industry standard 7- and 9-track magnetic tape formats add error detection codes to each data block. Individual data characters are protected with parity bit, and longitudinal redundancy check character (LRCC) code is used to check parity along each track. 9-track format also includes cyclic redundancy check character (CRCC) error correction code that permits automatic correction of most errors

Error Detection

Errors are detected in magnetic tape systems by recording two or three types of check bits with each data block (Fig 2). While a block is being written, it is simultaneously read back by a separate tape head and all error detection codes are checked. If a recording (write) error occurs, the formatter automatically backspaces, erases the small region of tape that contains the error, and then rewrites the block from its buffer memory. If a read error occurs, the formatter software goes into a 2-phase process designed to recover the original data if at all possible. First, the data block containing the error is reread several times while varying the sensitivity of the tape transport read amplifier. If the error is "soft" (temporary), perhaps caused by a speck of dust or slightly deformed tape, it can often be read correctly after a few tries. A "hard" (permanent) error will persist through any number of rereads and calls for the second phase of the error recovery software to be invoked.

This error correction phase makes use of the cyclic redundancy check character (CRCC) recorded with each data block. CRCC is an error detection and correction code designed to correct any number of errors—provided that all errors occur in the same track on the tape. Stray dust or tape particles tend to be much smaller than the distance between tape tracks so that single-track errors are by far the most prevalent. Therefore, most hard errors can be detected and corrected using the CRCC.

The longitudinal redundancy check character (LRCC) consists of parity bits that make the total number of 1s in each track even. This assures that all tracks will erase with the same magnetic polarity in the

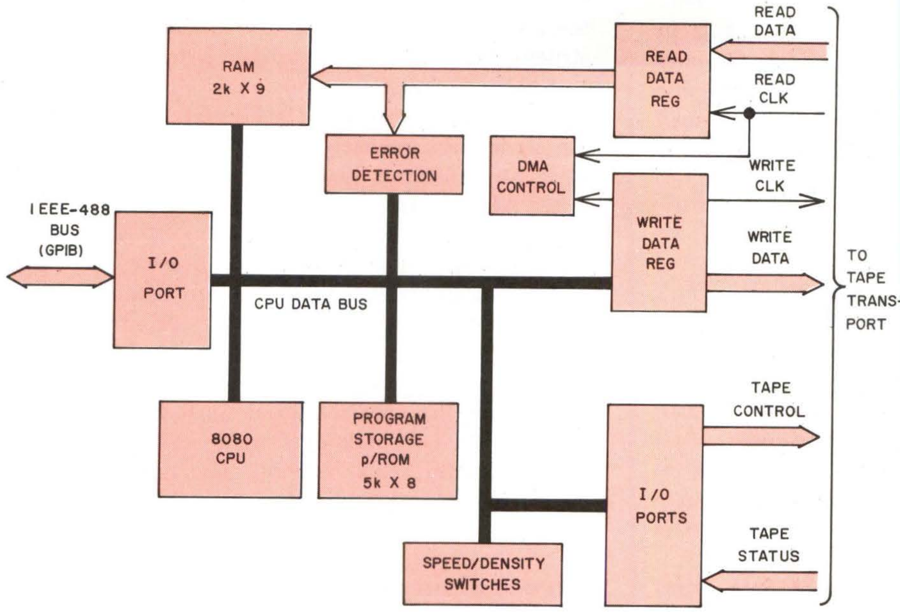

Fig 3 Organization of buffered tape formatter. Formatter uses microprocessor to interface industry standard tape drive to IEEE-488 bus. Software handles all tape formatting, timing, and error recovery procedures plus bus handshake protocol. Processor accepts incremental data from bus and stores it in RAM. When complete data block is received, required check characters are added and block is recorded synchronously on tape. Error detection circuitry continuously monitors data received from tape, providing read-while-write data checking while software concentrates on write timing

interblock gaps. The older 7-track format also uses the LRCC to detect multiple-bit errors that might produce acceptable character parity. Although the LRCC provides reliable error detection, it is not sophisticated enough to support automatic error correction; thus 7-track systems will suffer from a higher rate of uncorrectable errors.

Error detection and correction using rewrites, rereads, amplifier threshold adjustments, and the CRCC code are all well-known and widely used techniques on tape controllers designed for use with large mainframes. Rarely, if ever, however, have all of these capabilities been included in a small formatter designed for offline use. Without the microcomputer, these capabilities would be prohibitively expensive in small data systems.

Software Replaces Hardware

The block diagram in Fig 3 shows the organization of the formatter. All timing, counting, and delay generation circuitry typical of present formatters is absent—replaced with a microprocessor and associated memories to form an integral microcomputer. Even the GPIB interface is composed of little more than input/output (I/O) ports and line drivers, plus software that performs bus handshake and control tasks. The interface between the microprocessor and tape transport is not as simple, but still relies on software as much as possible to eliminate hardware.

While the microprocessor is busy recording data, special parity and CRCC checking circuits simultaneously monitor the read data output of the transport for tape errors. After a data block is written, the microcomputer checks this hardware to determine whether any errors occurred during the write cycle. Other than this hardware assistance, all tape timing, coding, reading, and writing are handled by software that adapts to the format and tape speed required for the tape transport in use.

Data bytes received from the GPIB are stored in random-access memory (RAM) until a complete tape block is received. Software then adds the required parity bits and check characters, creating an exact image in RAM of the block as it is to appear on magnetic tape.

When the RAM image is ready, the microcomputer becomes a tape formatter for the few milliseconds needed to record the data block on magnetic tape. Software first starts the tape in motion, and then generates a prerecord time delay that allows the tape to reach rated speed. This delay interval and all other tape timing depends on tape speed, tape format, and operation cycle (read, write, backspace, edit, etc) in process. More than 100 time delays are stored in program tables to handle various operations that can occur at four standard speeds (12.5, 25, 37.5, and 45 in/s) and in three formats (7-track NRZI,* 9-track NRZI, and 9-track phase-encoded).

When the tape reaches rated speed, actual recording occurs. Software outputs the tape block image from RAM one byte at a time at a rate appropriate for tape speed and desired recording density. These parameters are selected by setting speed/density switches that are sampled by the software when the system is turned on or reset. Four tape speeds and four standard densities (200, 556, 800, and 1600 bits/in) are accommodated,

*Nonreturn to zero inverted

introducing a total of 16 possible recording frequencies. Each of these required frequencies is generated by a software timing loop that outputs one byte each time around. While the lower speeds and densities are easily handled, the transfer rate for 45 in/s at 1600 bits/in is 72k bytes/s (about 13.9 μs/byte), which initially appears to be beyond the capabilities of available microprocessors. Therefore, a technique was developed to output 72k bytes/s using a conventional metal-oxide semiconductor (MOS) microprocessor.

Speeding up a Microprocessor

The 8080 microprocessor was selected for the investigation into speedup techniques because its interface signals and architecture offer several options instead of forcing a standardized design. Fig 4 shows a first attempt to output tape data with a fast 8080 software loop. This loop executes in 46 clock cycles, which takes 23 μs with the 8080. Unfortunately, this loop time is almost twice the required 13.9 μs/byte.

The usual design solution to this type of data transfer problem is to incorporate a DMA interface and allow external hardware to pull data from RAM at whatever rate is needed. While this approach is quite feasible for handling the 13.9-μs transfer rate, it would be cumbersome in this application because 16 different transfer rates are required at various speeds and densities. A DMA controller that must operate at any one of 16 unrelated frequencies is just the kind of complex timing circuitry originally slated for elimination with software.

This impasse was overcome by combining hardware and software to implement a "poor man's DMA." Key to this technique is to improve the microcomputer transfer rate by eliminating an inherently wasteful processing sequence. As with most small computers, the 8080 can output data only from its accumulator. If the needed data are in RAM, they must first be read into the accumulator, then output. This is evident in the program of Fig. 4. The MOV A,M instruction loads the accumulator from memory so that the OUT TAPE instruction can then output the data byte.

Adding a single NAND gate eliminated the need for this double transfer (Fig 5). This gate allows the write data register to receive the data byte at the same time that the 8080 reads it. A spare 8080 address line, A15, enables the gate. Whenever the microprocessor reads memory with the A15 address bit set, the data read are transferred directly from memory to the output latch. This technique eliminates the need for an output instruction in the program loop, thus saving 5 μs for every transferred byte. The only penalty is that with the A15 address line dedicated to controlling the special output port, the microprocessor can address only 32k of storage instead of the normal 64k. However, 32k is still far more storage than required.

Streamlining the Software

Eliminating the OUT instruction reduces the loop execution time to 18 μs, still short of the 13.9-μs goal. The final speedup is achieved by reworking the loop program to take advantage of the fact that the accumulator is no longer needed as a transfer station for output data. The program listed in Fig 6 has only four instructions in the output loop and, with the help of the added NAND gate and some advance data preparation, it outputs 1 byte every 13 μs. With this program, the required output rate (13.9 μs) can be achieved exactly by using a slightly lower than normal crystal frequency in the 8080 clock oscillator.

In the revised loop program, the first difference from the original program is that the memory pointer

```
                                                         Timing
        LXI   H,BUFSTART      ; POINT AT FIRST BYTE
        LXI   D,BYTECOUNT     ; LOAD LOOP COUNT
LOOP:
        MOV   A,M             ; FETCH BYTE FROM RAM        7
        OUT   TAPE            ; OUTPUT IT                 10
        INX   H               ; POINT AT NEXT BYTE         5
        DCX   D               ; DECREMENT LOOP COUNT       5
        MOV   A,D             ; SEE IF LOOP COUNT = 0      5
        ORA   E               ;                            4
        JNZ   LOOP            ; JUMP BACK IF NOT          10
                                                          46 clock cycles
                                                         (23 μs)
```

Fig 4 Simple 8080 programmed output loop. After fetching and outputting data byte, program must update two registers (H and D) and then test for 0 in double-precision loop counter. Timing measurements show that loop consumes 23 μs/byte—too slow for design requirements register is initially loaded with BUFSTART + A15. This register is loaded with the address of the first byte to be transferred, as before, except that address bit A15 is also set. Any memory access using this pointer will now output data.

The first instruction within the transfer loop, MOV B,M, reads memory using the pointer, and this outputs a byte to the special port. This instruction has been changed from the original MOV A,M to shunt the byte into otherwise unneeded register B, which frees the accumulator for more profitable work. The data byte is not needed in any register—it is merely read to make it available to the external latch. Because the instruction set requires a destination for any read instruction, the 8080 reads the byte into a surplus register.

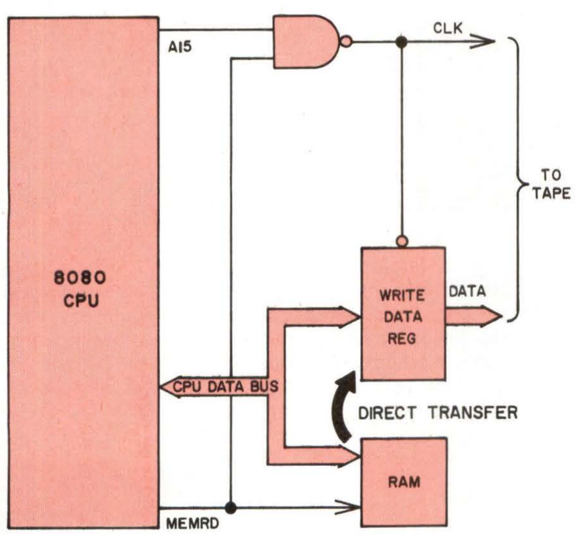

Fig 5 Poor man's DMA. Adding one NAND gate to 8080 microcomputer system provides poor man's DMA. NAND gate forces a direct memory-to-output data transfer to occur whenever program reads RAM with address bit A15 set, eliminating need for several instructions and doubling the processor's output transfer rate

With this novel programming technique, the accumulator is not used while outputting data. Instead, it is devoted to streamlining the loop exit-condition checking. The accumulator is eight bits wide with a capability to count up to 256. Unfortunately, the tape formatter may be called upon to record blocks of several thousand bytes, so the accumulator cannot be utilized as a simple loop counter.

Nevertheless, loop termination testing can be done with only one instruction, CMP H, if data to be recorded are placed properly in memory. This instruction compares the number in the accumulator with the number in the H register, and sets flags that control the succeeding conditional jump. The H register contains half of the memory pointer—the most significant eight bits. Thus, the program compares an 8-bit value called HLIMIT + A15 (held in the accumulator) with the most significant eight bits of the memory pointer. The loop can terminate only when the most significant half of the pointer changes. This change occurs at addresses that are multiples of 256. To detect the end of the loop properly, the memory image of the block to be recorded must end exactly at one of these boundaries. Since there is no restriction on where the block can start, blocks of any size can still be accommodated. The only advance preparation needed is to assure that the block is properly positioned in RAM before the write loop is executed.

This extremely short program loop, and the gate circuit that made it possible, increased the programmed output transfer rate from 38.4k to 76.9k bytes/s. In

```
                                                      Timing
        LXI   H,BUFSTART+A15   ; POINT AT FIRST BYTE
        LDA   HLIMIT           ; PUT HLIMIT IN A
LOOP:
        MOV   B,M              ; HARDWARE GRABS BYTE     7
        INX   H                ; POINT AT NEXT BYTE      5
        CMP   H                ; SEE IF H = HLIMIT       4
        JNX   LOOP             ; JUMP BACK IF NOT       10
                                                        26 clock cycles
                                                       (13 µs)
```

Fig. 6 Final output program. 4-instruction loop outputs one byte every 13 μs, exceeding timing goal. First instruction in loop triggers direct memory-to-output transfer. INX H updates memory address register. Since accumulator is no longer needed for output, it is used to simplify loop control to just two instructions the buffered formatter design, this rate is set to the desired 72k bytes/s by slowing down the 8080 clock. The other 15 required transfer rates are provided by other software loops with built-in time delay instructions. Although the buffered formatter is intended only for tape speeds of up to 45 in/s, incorporating double-speed 8080 components and doubling the clock frequency will extend formatter capability to 90 in/s.

Reading is Easier

Reading tape data into RAM is accomplished with an input version of "poor man's DMA." Problems here are that the number of characters to be read is unknown (almost any block size may be encountered) and timing of the external read data clock is subject to tape speed inaccuracies and jitter. Even though a very simple software loop can be used to input data and increment to the next RAM address, hardware must be provided to synchronize the software to the external clock and to escape from the loop when a complete block has been read.

To synchronize with the external tape clock, use is made of the 8080 READY interface line. While this signal is low, the 8080 pauses during the memory access portion of a machine cycle. The circuitry illustrated in Fig 7 detects the moment when the software loop is writing to RAM, again using address line A15 to activate a direct memory transfer. In this case, however, the DMA circuitry also "freezes" the microprocessor until the next byte of data is clocked in from the tape transport. Once the byte has been received, the READY signal is set high again, permitting the software to continue in its loop, incrementing the memory address register, and restarting the cycle. This process will continue indefinitely, with the software stuck in a never-ending input loop, until the MPD (missing pulse detector) circuit detects the end of a data block. This occurrence interrupts the 8080, providing an escape from the loop so that normal processing can resume. Trigger time of the MPD is controlled from a few microcomputer output bits that are initialized at power-on for the transfer rate in use, again using software and programmable read-only memory tables to avoid the use of complex timing hardware.

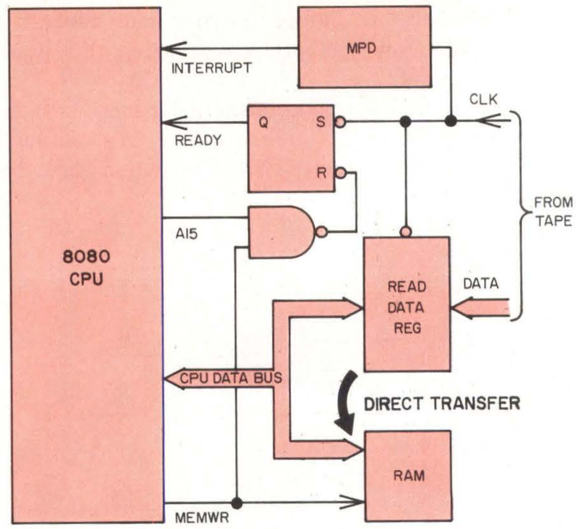

Fig 7 Input version of poor man's DMA. Tape data are read directly into RAM while small software loop provides sequential addresses. Ready flip-flop synchronizes program to external clock by stopping processor until next tape character arrives. MPD (missing pulse detector) senses end of data block and terminates loop by interrupting microprocessor

Conclusions

This microprocessor-based formatter design originally appeared to be impractical because low cost MOS microprocessors were apparently too slow to handle 45-in/s magnetic tape data. Undoubtedly, a smart formatter might have been developed by adding a microprocessor to a conventional formatter, but this would be an expensive solution. Instead, a microprocessor's capabilities were stretched, using a synergistic blend of hardware and software to double its speed. This made it possible to replace most of the circuitry found in present formatters with a microcomputer. Once this was accomplished, several advanced capabilities could be added by merely including more software.

The result is a tape formatter that uses fewer components than its TTL-based predecessors while providing new capabilities. The microprocessor inherently provides data buffering, and this is exploited to full advantage by adding a software-controlled interface compatible with the IEEE-488 standard. Additional software makes it possible to handle tape transports at all common speeds and densities without changing any components, to search a tape for a desired file or block, and to automatically reread, rewrite, or correct tape errors. If these kinds of capabilities were implemented with TTL, the resulting design would be prohibitively expensive. With a microcomputer, however, these features are attained by adding only a couple of program storage memories to the hardware cost.

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OEM User's Manual for Tape Transports, Pertec Corp, Chatsworth, Calif, 1973

A. Scott McPhillips is a microprocessor design consultant at IDEAS. His experience includes the application of microprocessors to numerous tasks, and the design of magnetic tape transports and formatters. He holds a BSEE degree from the University of Maryland.

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APPLICATION NOTE

Pattern Sensitivity Techniques for Testing CCD Memories

Ivan D. Vancov*

Bulgarian Academy of Sciences
Sofia, Bulgaria

Use of RAM test programs with serial shift CCD memories requires time-consuming and expensive measurements. By analyzing parameter and pattern sensitivities, simplified but sufficiently thorough tests for these memories have been developed that reduce safe testing from hours to minutes, while resulting in significant cost savings

Recent appearance of charge-coupled device memories on the market has brought about an increasing range of information storage applications. As with other semiconductor memory types, sensitive operating parameters and data patterns must be thoroughly checked using timely, cost-effective test procedures. The former refers to such critical parameters as shift period and drain supply voltage and the latter to the applied test patterns of various combinations of logic 1s and 0s. A number of standard memory test programs, such as MARCH (write and read/write forward and backward), WAKPAT (walking pattern or ripple), GALPAT (galloping 1s and 0s), and others,[1,2] were developed mainly for testing random-access memory devices and systems.

These common tests have proved to be highly effective. For their program execution, however, a specialized high speed test system such as the Macrodata MD-104 or MD-154 is required, which usually is not available to memory users. Furthermore, the realization of these memory test programs by a commercial minicomputer is a time-consuming procedure due to the slow operation of the program interface channel, especially for a charge-coupled device (CCD) memory with a minimum size of 16k. For example, a checkout of the Intel 2416 CCD memory[3] by a single WAKPAT test pattern using a Multi-20 minicomputer (manufactured by Intertechnique, France) takes about six hours. Consequently, by exploiting the device's internal organization, simpler and more conclusive parameter and pattern test programs have been successfully derived to save both cost and time.

Memory Device Organization

A synchronously clocked 16,384-bit CCD memory, the Intel 2416 is organized as 64 parallel, independent, recirculating shift registers (SRs) of 256 bits each with a refresh amplifier at each end. Shifts of 1 bit are initiated simultaneously within all 64 SRs by exercising the 4-phase clock signals. During the time between each shift, any one of the 64 SRs can be accessed for an input/output (I/O)

*The work described was performed by the author at the Laboratoire d'Electronique et de Technologie de l'Informatique du Centre d'Étude Nucléaire de Grenoble, France.

TABLE 1

Lowest Drain Supply Voltage Values for Normal CCD Operation

Test Program \ t_{SP} (μs)	0.65	0.70	0.75	0.8	0.9	1.0	1.2	1.4	1.6	9.0	20
1. Write All 0s	11.1	9.6	9.5	9.5	9.3	9.3	9.2	9.0	8.9	8.9	9.0
2. Write All 1s	11.6	9.7	9.0	8.9	8.8	8.7	8.5	8.3	8.3	8.2	8.3
3. 0 Between 1s	11.5	10.7	10.3	9.9	9.6	9.5	9.4	9.3	9.2	8.9	9.0
4. 1 Between 0s	11.1	9.8	9.2	8.9	8.8	8.7	8.6	8.5	8.5	8.2	8.3
5. 00110011 . . .	—	9.8	9.5	9.4	9.3	9.2	9.1	9.0	9.0	9.0	9.1
6. 010101 . . .	—	10.5	10.1	9.7	9.4	9.3	9.2	9.1	9.0	9.2	9.3
7. 0101 . . ./1010 . . . /0101 . . .	—	10.9	10.3	9.9	9.7	9.5	9.4	9.3	9.2	9.3	9.4

operation by applying an appropriate 6-bit address input through the 1-of-64 decoder. Information stored in any (no matter which) bit location is constantly circulating through each SR, ie, each recorded logic 0 or 1 level is incremented through each of the 256 bit locations of its particular SR. Therefore, the device organization combines serial and random address memory functions for the 64 SRs.

Test Program Development

Upon examination of the memory's internal structure, it is reasonable to assume that there is no outstanding advantage in checking all 64 x 256 or 16,384 bit locations of the device using a separate test word, as was done in the previously mentioned test programs. It should be sufficient to write the test information into one bit location of each SR, and then test the remaining SR bit locations by 255 shifts.

In a multibit memory system at least one separate 2416 device must be used for each bit because only one SR from the chip is accessible for an I/O operation at the same time. Interactions between these separate devices, ie, between the different bits of the memory system, are not probable. Thus, all memory system bits can be tested independently, by the same information pattern; ie, the test words could contain the same logic level in all memory bits, such as 0000...0 or 1111...1.

Test Programs

Using previously developed SR test patterns[2] and taking into account the unique properties of CCD memories, the following test programs were devised.

1. *Write All 0s or 1s.* All logic 0s or all logic 1s are written into every bit location of the memory. Each location is read out and verified, in turn, for correctness. This is an absolute minimum test necessary in order to check every SR as well as addressing.

2. *0 Between 1s or 1 Between 0s.* This modification to the Walking Pattern Shift Register Test (SRWALK) is realized by initially writing all 1s throughout the memory. A logic 0 is then written into one bit location of SR-n, where n is any one of 64 SRs. Next, while reading and checking for information destruction, SR-n is shifted 256 times. The 0 bit location, surrounded on all sides by 1s, is incremented through all 256 SR locations (cells) until it returns to its starting location. This tests for worst case charge interactions between neighboring cells of a CCD. Next, a logic 1 is rewritten in place of the 0 bit. In SR-n + 1, a logic 0 is then written into the same bit location as described for SR-n; SR-n + 1 is likewise incremented, read, and checked using the same shifting technique. After rewriting logic 1, the succeeding SR is tested until all 64 SRs have been checked out. Similarly, the 1 between 0s test program can be carried out by first writing all 0s throughout the memory and then using a single logic 1 as the check bit.

3. *001100110011....0011 Test.* This program, based on the alternating word pattern shift register test (ALTWOR), is recommended as a test for device sensitivity to a sequence of all possible information transitions—such as 0 to 0, 0 to 1, 1 to 1, and 1 to 0. A 001100110011....0011 test pattern is written into each SR of the CCD, and all addresses are read, in turn, to verify correctness.

4. *01010101....01 Test.* Alternate 0s and 1s are written into ascending bit locations of each SR, starting with logic 0. Each bit location is then read out and checked for information destruction, to test for sensitivity to the successive 0 to 1 and 1 to 0 transitions.

5. *0101.../1010.../0101.../1010... Test.* To stress the interaction between neighboring cells of different SRs, this checkerboard test pattern is used. Alternate 0s and 1s are written into all bit locations of the first SR, starting with logic 0. The same sequence, starting with logic 1, is written into the second SR. Logic 0 is the first level of the sequence in the third SR, while logic 1 starts SR-4, and so on. The device is read out and checked for information correctness in ascending bit locations.

TABLE 2

Drain Supply Voltage Values of Eight Devices Tested by Five Programs for Two Shift Periods

t_{SP} (μs)	1.0								1.5							
Test Program \ Memory Device	a	b	c	d	e	f	g	h	a	b	c	d	e	f	g	h
1. 0 Between 1s	9.3	8.5	8.4	8.2	8.7	9.4	8.8	8.9	9.3	8.3	8.2	8.2	8.4	9.3	8.8	8.7
2. 1 Between 0s	9.3	8.9	8.4	8.2	8.9	9.5	8.8	8.7	8.9	8.5	8.2	8.3	8.5	9.3	8.8	8.7
3. 00110011...	9.3	8.4	8.3	8.2	8.6	9.5	8.8	8.8	9.3	8.4	8.2	8.3	8.5	9.3	8.9	8.7
4. 010101...	9.3	8.9	8.7	8.3	9.0	9.5	9.0	9.0	9.3	8.6	8.2	8.3	8.6	9.4	9.0	8.7
5. 0101.../1010.../0101...	9.3	9.0	8.8	8.4	9.2	9.6	9.1	9.3	9.3	8.6	8.2	8.3	8.6	9.4	9.0	8.7

TABLE 3

Results of Testing Same Eight CCDs Organized as Two 16k, 4-Bit and Two 64k, 1-Bit Memories

t_{SP} (μs)	1.0				1.5			
Memory Organization	16k, 4 Bits		64k, 1 Bit		16k, 4 Bits		64k, 1 Bit	
Test Program \ Memory Devices	a-d	e-h	a-d	e-h	a-d	e-h	a-d	e-h
1. 0 Between 1s	9.3	9.4	9.3	9.4	9.3	9.3	9.3	9.3
2. 1 Between 0s	9.3	9.5	9.3	9.5	8.9	9.3	8.9	9.3
3. 00110011...	9.3	9.5	9.3	9.5	9.3	9.3	9.3	9.3
4. 010101...	9.3	9.5	9.3	9.5	9.3	9.4	9.3	9.4
5. 0101.../1010.../0101...	9.3	9.6	9.3	9.6	9.3	9.4	9.3	9.4

Test Results

These test programs have been implemented by a Multi-20 minicomputer, using its program interface channel and a computer program for peripheral testing. The longest test program (No. 5: 0101.../1010.../0101...) at a shift cycle time of 9 μs takes about 2 min for a 16k memory. For all test patterns, the effective limits of the drain supply voltage (V_{DD}) and shift cycle time, chosen as the most sensitive device parameters, were measured. A concurrent investigation of the influence of the V_{BB} supply voltage has disclosed that its value is not critical—the memory operated successfully under test for V_{BB} variations from 1 to 5 V.

Lowest values of drain supply voltage (V_{DDL})** at which a single 2416 device continues to operate normally are listed in Table 1. These values were obtained by running seven test programs at 11 shift periods (t_{SP}). As listed, no large variations in V_{DDL} exist in the shift period range of 1 to 20 μs. For t_{SP} values less than 1 μs, a significant increase in V_{DDL} with a decrease in shift period is observed. These results show that in the manufacturer's guaranteed range of shift period—0.75 to 9.0 μs—the device operates with a reasonable margin of change in V_{DDL}—1.7 V minimum (12.0 − 10.3) at a t_{SP} of 0.75 μs. A comparison with results from random-access memory (RAM) testing demonstrates that better stability exists for a CCD memory: V_{DDL} values for a 4k RAM[1] are 11 V for the MARCH test program and 11.9 V for the GALPAT pattern, while a V_{DDL} value of 10.3 V at 0.75 μs is obtained for the CCD memory in the worst case. The nominal value of V_{DD} for both memories is 12 V.

Table 2 gives the V_{DDL} values for eight 2416 devices at two shift periods. A comparison of the results of any two devices demonstrates no correlation in their patttern sensitivity—V_{DDL} increases in value for the same device in all test programs. It can also be seen that for some devices the pattern 0 between 1s gives higher V_{DDL} values than the pattern 1 between 0s; however, for others this effect is reversed. Most likely, for this reason, the test programs 010101... and 0101.../1010.../0101... give the maximum V_{DDL} values, since the two configurations 0 between 1s and 1 between 0s are repeated successively in these test patterns.

**Investigations show that up to the absolute maximum V_{DD} value (14 V) as prescribed by the manufacturer, there are no upper limiting values of V_{DD} under all test conditions.

Data in Table 3 were obtained by testing the same eight devices, this time divided into two groups of four (a through d and e through h). Each group was organized either as a 16k, 4-bit memory or as a 64k, 1-bit memory. A comparison of data in Table 3 with those in Table 2 shows that memories formed by devices a through d have the same V_{DDL} values as those of device a when tested separately. The same result is observed for memories formed by the second group of devices e through h, whose V_{DDL} values coincide with those of device f. Note that V_{DDL} values of devices a and f are the highest for each group; therefore, these devices determine the limit of the V_{DD} decrease for corresponding memories. Lack of change in the V_{DDL} values, when a CCD (a and f in this case) is tested separately or included in a memory system, confirms the stipulated absence of information interaction between separate bits of the memory system (the 16k, 4-bit case). Also, no interaction between the four devices forming one bit of the 64k memory system could be observed.

For comparison, the second 16k, 4-bit memory (including devices e through h) was tested by a WAKPAT program at a t_{SP} of 1 μs. The background pattern was 1010, and a complement test word was written successively in all locations, with reading and information checks of all other addresses after each new writing. The V_{DDL} value obtained—9.5 V—is equivalent to the results for the same memory when tested by 1 between 0s, 00110011..., and 010101... programs, and is below the V_{DDL} value obtained by the 0101.../1010.../0101... program (Table 3). This fact shows that simplification of CCD test programs has not decreased test efficiency.

Conclusions

The acquired results show that CCD memories, like other memory types, have pattern sensitivity over a valid range of operation, and careful testing is inevitably required. For this purpose, the proposed test programs are highly effective. By exploiting the internal CCD structure, sensitive test programs ensure sufficient testing in minimum time and can be realized economically by a standard minicomputer. For a basic evaluation at the component level, a full testing by all patterns is advisable, while for an SR memory system, the rather unsophisticated pattern of 0101.../1010.../0101... is recommended as a safe test.

Acknowledgements

The author is indebted to Messrs R. Gariod, C. Axelrad, and J. L. Lecomte who made this work possible and is thankful for the valuable advice and counseling offered by Messrs L. Chabanas and B. Thevenin.

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TECH BRIEF

Binary/BCD-to-ASCII Data Converter

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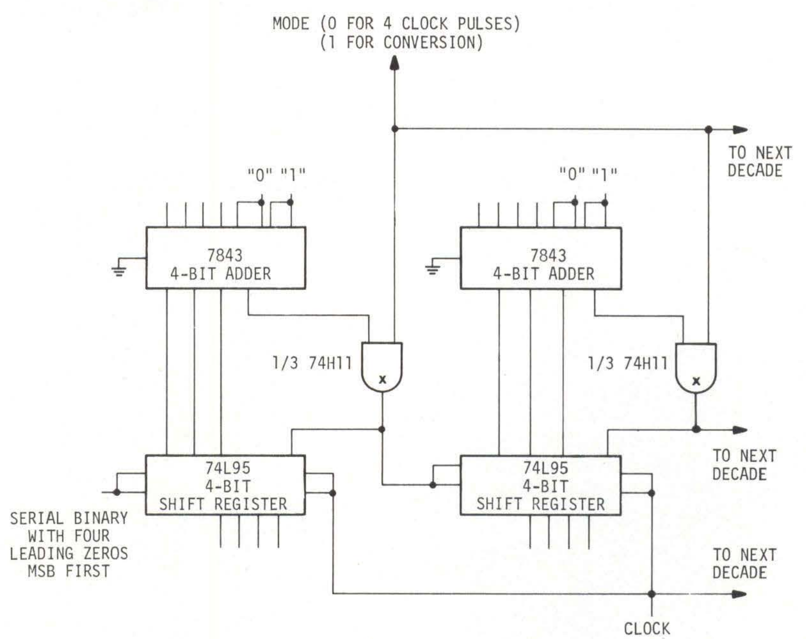
A digital data converter inputs multiple precision binary words, converts the data to multiple precision BCD data, and routes these data back to the computer. The converter accepts two computer words from a 16-bit minicomputer (32 bits total) and converts them to 80 bits of BCD standardized (ASCII) data. Compared to previous data converters, this method reduces the required computer software, time, and memory.

The converter can readily change its conversion base. Unlike prior converters which use a ROM dedicated to base 10 only, the converter base can be readily changed without the need for a new gate structure for each base changeover.

Each decade of the converter, as partially illustrated, consists of a 7483 4-bit adder, a 74L95 4-bit parallel-in/parallel-out right shift register, and one-third of a 74H11 AND gate. The 7483 continually adds three to the contents of its associated shift register. If the contents are four or less, the most significant output bit is zero. If the contents are five or more, this bit is one.

The bit state controls the mode of the associated register. If the bit is one, then the sum of three plus the contents of the register is replaced but shifted one bit to the right. The least significant bit is either shifted in serially or loaded in parallel.

Support software has optional leading zero suppression and stores the results where desired, requiring approximately 100 locations of memory depending on the computer which is interfaced to this converter. Actual conversion time for 32 bits is 72 μs, and the range is zero to (2^{32}-1). Master clock frequency is 500 kHz; conversion time is 36 pulses of this clock. If clock frequency is increased, conversion times (using faster registers) as low as 10 μs are possible. Time to execute one complete passthrough, and software for a 32-bit conversion and zero suppression is about 240 μs.



Two decades of data converter are shown to indicate how 7483 controls shift register in such a way as to be parallel loaded or shifted one place to the right

Note

This work was done by Anthony J. Miller of Goddard Space Flight Center. For further information, write to: Donald S. Friedman, Technical Utilization Officer, Goddard Space Flight Center, Code 704.1, Greenbelt, MD 20771.

Patent Status

This invention is owned by NASA, and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to the Patent Counsel, John O. Tresansky, Goddard Space Flight Center, Mail Code: 204, Greenbelt, MD 20771. Refer to GSC-12044.

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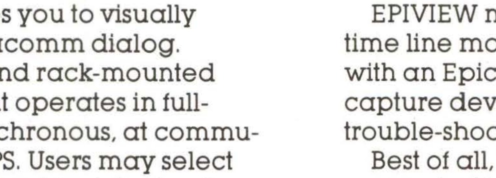

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TECH BRIEF

Microprogramming for Real-Time Data Acquisition

Microprogrammed firmware asynchronously handles transmit and receive functions

A microprogramming (firmware) technique has a polling interval of 100 μs and satisfies the following requirements. It allows full data bus duplex operation; measurement data can be obtained by polling various hardware interface modules on a 1M bit data bus; polling functions are transparent to software operations; polling is accomplished on a cyclic basis with a fixed interval between polls; verification of the proper response is performed as part of the receive function; the transmit function is able to interrupt the receive function; and "off-the-shelf" processors are utilized.

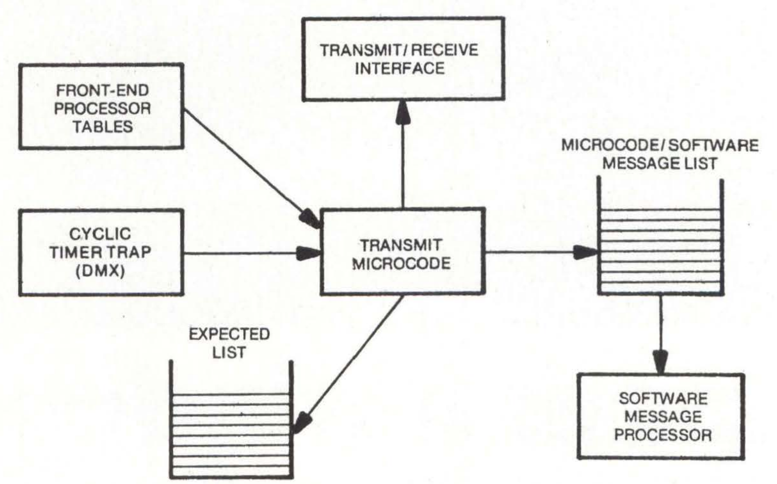


Fig 1 Transmit microcode trap logic is conditioned by a preset clock. A measurement request or issuance of a command is controlled by a set of software-initialized polling tables

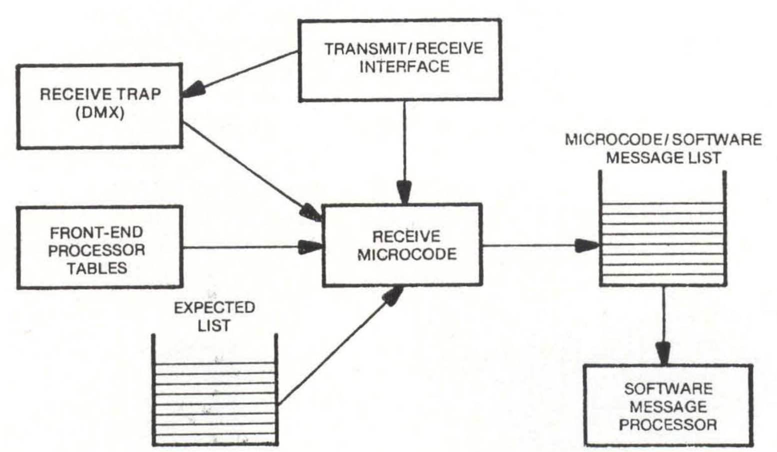


Fig 2 Receive microcode trap logic is conditioned by the transmit/receive hardware when a response is returned on the data bus

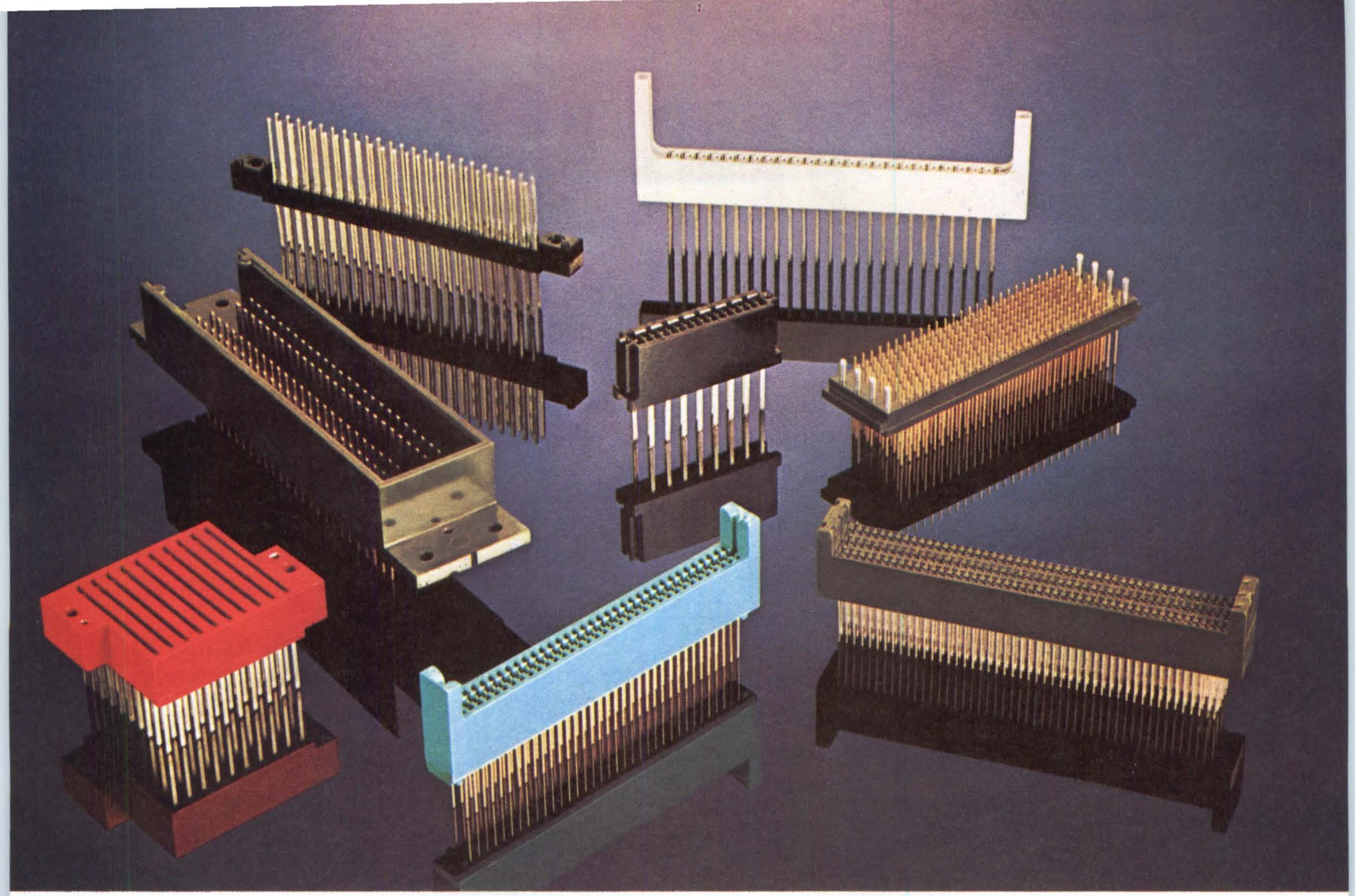
The firmware package is a trap-initiated microprogramming technique that asynchronously handles a transmit-and-receive (T/R) function as shown in Figs 1 and 2. In addition, microcode traps used to perform the assigned tasks require expansion of the computer direct-memory-exchange (DMX) trap capability to include recognition of a user-implemented trap. This technique may be implemented on any computer system having a user-writable control store and microcode trap logic.

The data bus is controlled by a transmitter/receiver which interfaces with the processor in control. Transmit microcode trap logic, as shown in Fig 1, is conditioned by a preset clock. Operations performed on the bus may be a request for a measurement or the issuance of a command. The sequence of these operations is controlled by a set of software-initialized polling tables. Multiple tables provide for a change of sampling rates.

The receive microcode trap logic, as shown in Fig 2, is conditioned by the T/R hardware when a response is returned on the bus. An input sequence acquires the data and performs certain validity checks. Any resultant errors from these operations are reported to software. Some of the errors, considered catastrophic, cause the microcode to inhibit all further operations on the bus.

Note

This work was done by Frank J. Patella of IBM Corp for Kennedy Space Center. For further information, write to: Raymond J. Cerrato, Technical Utilization Officer, John F. Kennedy Space Center, Code SA-RTP, Kennedy Space Center, FL 32899. (KSC-11027).



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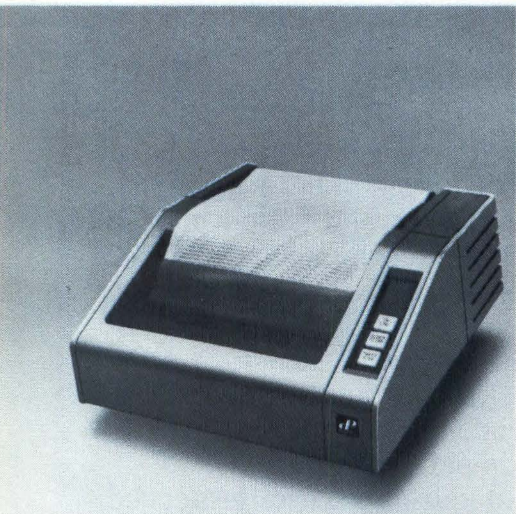
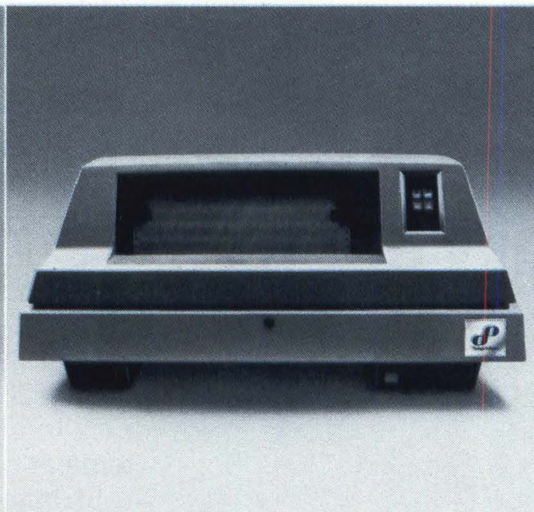


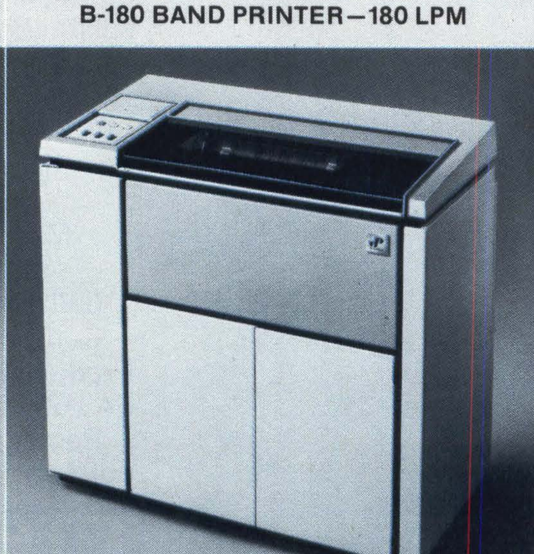
T-80 THERMAL PRINTER—80 CPS



B-180 BAND PRINTER—180 LPM

M-200 MATRIX PRINTER—200 LPM

2290 LINE PRINTER—900 LPM



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CIRCLE 53 ON INQUIRY CARD

DESIGN NOTE

Two-Step Procedure Improves CRC Mechanism

Patrick J. Fortune

Argonne National Laboratory
Argonne, Illinois

A 2-step technique modifies conventional CRC error detection schemes to overcome the issues involved with erroneous leading or trailing 0 bits in bit-oriented protocols by setting the CRC shift register to all 1s and then transmitting the inverted remainder as check bits

Conventional usage of a cyclic redundancy check code to detect transmission errors in a data stream corresponds to appending check bits after each data block at the transmitter and comparing them to the computed bits using the data as detected at the receiver. That is, consider that N bits in a data message represent coefficients (0 or 1) of a polynomial of $N - 1$ degree, $D(x)$, and that the remainder (the check bits) which results when $D(x)$ is divided modulo-2 by a generator polynomial, $P_n(x)$ of degree n, is appended to the data. Hence, the actual transmitted message is

$$M(x) = x^n D(x) + R_{n-1}(x) \quad (1)$$

where $R_{n-1}(x)$ is defined by

$$x^n D(x)/P(x) = Q(x) + R_{n-1}(x)/P_n(x) \quad (2)$$

or

$$M(x) = Q(x)\ P_n(x) \quad (3)$$

and the division is understood to be modulo-2, equivalent to the Exclusive-OR function. The same operations are performed at the receiver, and since modulo-2 arithmetic is used (so that the results of addition and subtraction are the same), the remainder generated will be zero (by equation 3) if no detectable errors have occurred in transmission.

The indicated operations can be performed by hardware, software, or a combination of the two. Techniques used to carry out the division must, of course, be combined with techniques to determine where the data bits of a message begin and end, so that the division operation can be started and stopped appropriately. A hardware technique to determine $R(x)$ given $D(x)$ and $P_n(x)$ using a feedback shift register has been discussed.[1]

In essence this technique amounts to shifting bits out of a shift register which contains the remainder, Exclusive-ORing the bit shifted out with the next data bit, and Exclusive-ORing the result back in at the positions corresponding to the 1 bits in the generating polynomial. A diagram of the shift register approach for generating polynomial $P_5(x) = x^5 + x^2 + 1$ is shown in Fig 1. As noted in Ref 1, application of this technique as outlined can lead to problems when used with recently popular bit-oriented protocols, such as SDLC (synchronous data link control), HDLC (high level data link control), and ADCCP (advanced data communication control procedures). In particular,

(a) if in the shift register implementation alluded to above the contents of the register which contains the remainder are preset to zero, erroneous leading 0 bits will not be detected;

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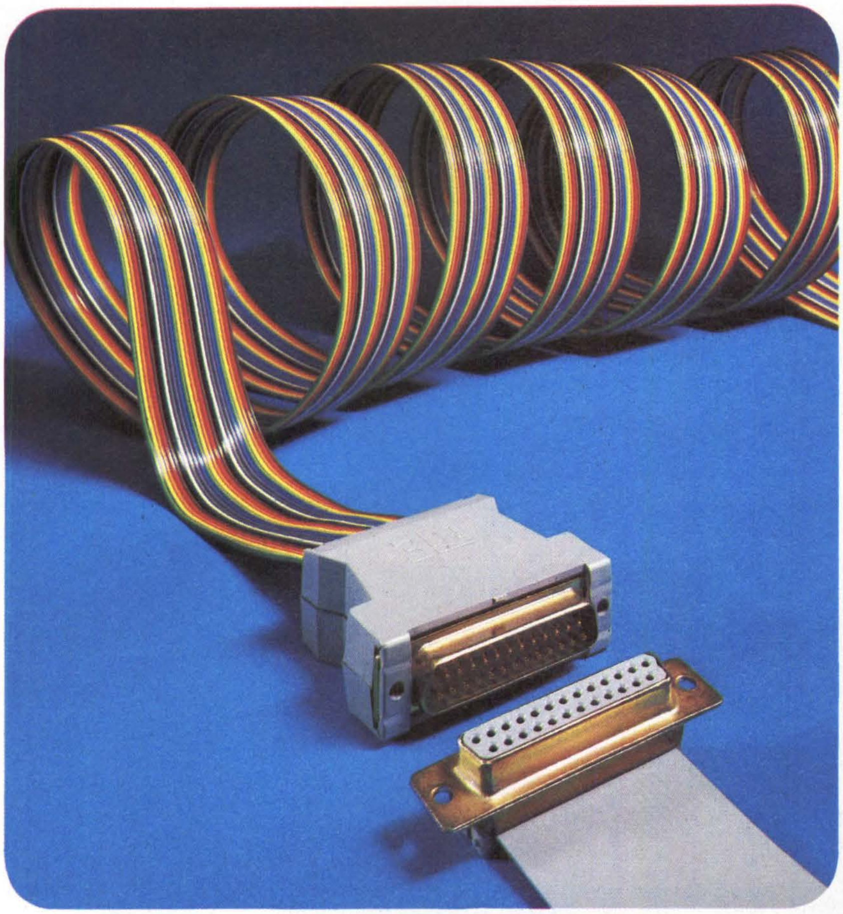

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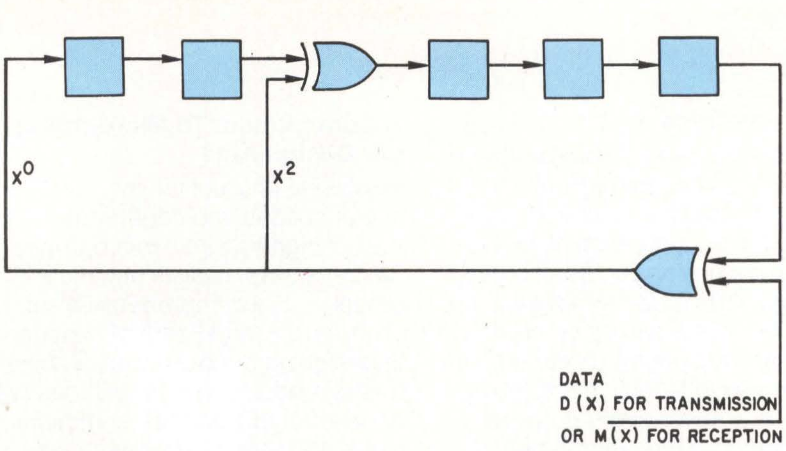

Fig 1 Linear feedback shift register for implementing division by $P_5(x) = x^5 + x^2 + 1$. When data block to be transmitted passes through this shift register, it is effectively divided by the polynomial, producing either string of redundant check bits for end of message or indication of errors picked up during message transmission

(b) if the final state of the register is also zero (essentially because of equation 3), the erroneous trailing 0 bits will not be detected.

Appropriate solutions to these problems have been proposed.[1] One such solution will be discussed and clarified, indicating its implications regarding the design and implementation of error checking hardware to be used with the above protocols.

2-Step Technique

The sources of the above problems can be eliminated by using a 2-step implementation prescribed by the SDLC, HDLC, and ADCCP protocols. First, the contents of the shift register are preset to an all 1s state prior to computation of the cyclic redundancy check (CRC) bits; this permits the detection of erroneous leading 0s. Second, the CRC bits are inverted (ie, complemented) prior to transmission to permit the detection of erroneous trailing 0s. The second step results in a unique nonzero final state of the shift register at the receiver if no errors have occurred in transmission. This final state's specific form depends only on the generating polynomial. The issues involved in selecting a particular CRC polynomial include the maximum size of the transmitted data block, the probabilities of both random bit errors and burst errors in the communication channel, the rate of undetected errors which can be tolerated by the users, and the overhead incurred by transmitting the CRC bits along with the data bits. The determination of the error detecting properties of a given $P_n(x)$ is a nontrivial problem and is discussed by Peterson and Brown.[2]

To illustrate the 2-step procedure, consider a transmission in which the data bits are 00111011 and the generating polynomial is 100101. These data and CRC bits correspond to the polynomials $D(x) = x^5 + x^4 + x^3 + x + 1$ and $P_5(x) = x^5 + x^2 + 1$, respectively. The first step in computing the CRC bits, using equations 1 and 2, amounts to forming the quotient $x^5D(x)/P_5(x)$. The $x^5D(x)$ term is represented by the bits 0011101100000, as multiplication by x^5 amounts to appending five 0 bits to the right of the data bits. Now, to eliminate the problem associated with erroneous leading 0s, the procedure given by equations 1 and 2 has been modified by requiring that the shift register in Fig 1 be preset to an all 1s state. In terms of the data polynomial, this is equivalent to carrying out the modulo-2 addition of the polynomial $F(x) = x^8 (x^4 + x^3 + x^2 + x + 1)$ to $x^5D(x)$; in terms of the actual data bits, this amounts to Exclusive-ORing the first five bits of $x^5D(x)$ with the five bits 11111. Thus, computation of the CRC bits requires dividing the sum $F(x) + x^5D(x)$ by $P_5(x)$ using modulo-2 arithmetic.

In general, the generating polynomial is not a factor of the dividend; therefore, the division will not come out even, ie, there will be a remainder. It is this remainder, then, that is complemented and used to replace the five added 0s in $x^5D(x)$, thereby forming the final transmitted message. In the case at hand, the results are

TABLE 1

Shift Register States in CRC Procedure Used in Bit-Oriented Protocols

	Shift Register State		Data Message Bits	
Nonzero Initial State	11111			
	11011		0	
	11001		0	
	01100		1	
	10010	D(x)	1	M(x)
	11101		1	
	11010		0	
	11001		1	
Remainder—complemented and sent as CRC bits	01100		1	
	10010		1	
	11101	Inverted CRC Bits	1	
	11010		0	
	01101		0	
Unique nonzero final state	00110		1	

Note: CRC bits (11001) are inverted remainder bits which are concatenated to the data bits to form transmitted message M(x).

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MC68A00L	Microprocessor	Introduced
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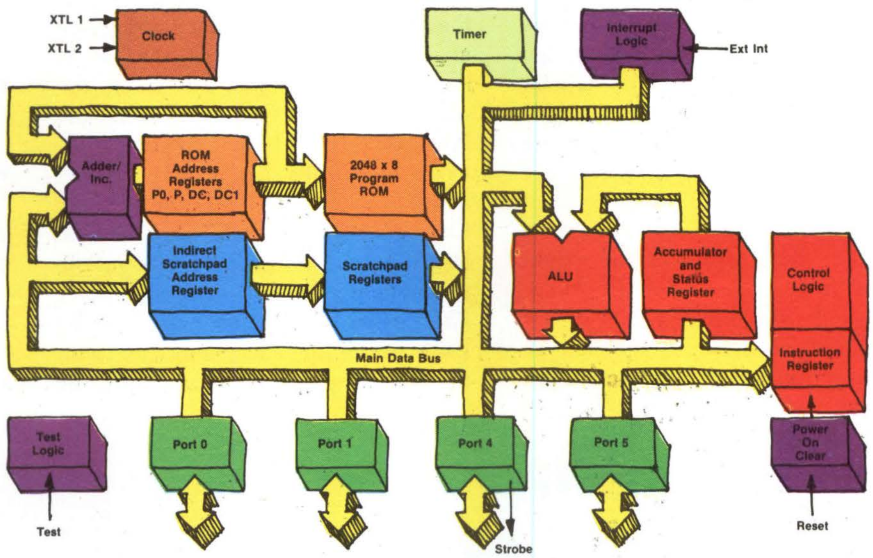

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$$\frac{1100001100000}{100101} = 0000011011110 + \frac{00110}{100101}$$

so that $\overline{R} = 11001$ and the transmitted message is 0011101111001.

This message is again divided by 100101 at the receiver and if no errors have occurred in transmission, the final result after division will be the unique nonzero remainder noted above. The states of the shift register at the receiver for this same example using the hardware of Fig 1 are presented in Table 1. The remainder (in the shift register) at the end of the data bits is 01100, with most significant bit (MSB) on the right so that it corresponds to $0(x^4) + 1(x^3) + 1(x^2) + 0(x) + 0(1) = x^3 + x^2$. Thus, the complement, 10011 is transmitted right-most bit first. Also, note that the final shift register state contains the result 00110 (x^0 through x^4), which represents the unique nonzero remainder.

This approach to the elimination of erroneous leading and trailing 0s can be clarified by using the following "longhand" technique to carry out the CRC computation that takes place at the receiver. Assume that it is known where the CRC bits start; the objective is to divide the 13 message bits (0011101111001) by the fifth-order generating polynomial (100101) one character at a time. Character size is defined to be one less than the number of bits in the polynomial; in this case, character size is five bits. Division is done by Exclusive-ORing each character with the previous remainder, padding the result with on all-0 character, and then Exclusive-ORing the result with the generator polynomial. If at the end of the data bits, less than a full character is left, the number of 0s padded is equal to the number of bits in the last group of data bits; then, the division is completed until the number of significant bits in the remainder is less than the number in the generating polynomial. To illustrate this technique, the results of the various steps, using the same message that was used in the first example, are presented in Table 2. The final nonzero result 0110 has its MSB on the left so that it corresponds to $0(x^4) + 1(x^3) + 1(x^2) + 0(x) + 0(1) = x^3 + x^2$. The final nonzero result 01100 (x^4 through x^0) in both tables is the same using either technique. This must be so, since the shift

TABLE 2

Longhand Generation of Final Remainder
Using Eight Data Bits and CRC Polynomial $P_5(x)$

"Initial" remainder	11111
First character (first five data bits) plus padding (five 0s)	0011100000
	1100000000
$P_5(x) = 100101$	100101
	101010000
	100101
	1111000
	100101
	110010
	100101
Remainder after first character division	10111 (number of bits < divisor)
Second character (last three data bits) plus padding (five 0s)	01100000
	11011000
$P_5(x) = 100101$	100101
	1001100
	100101
Remainder R after second character division	00110 (number of bits < divisor)
Check character (five bits) plus padding (five 0s)	1100100000
$R + \overline{R}$ plus padding = reference polynomial	1111100000
$P_5(x) = 100101$	100101
	110110000
	100101
	10011000
	100101
Final nonzero result	01100 (number of bits < divisor)

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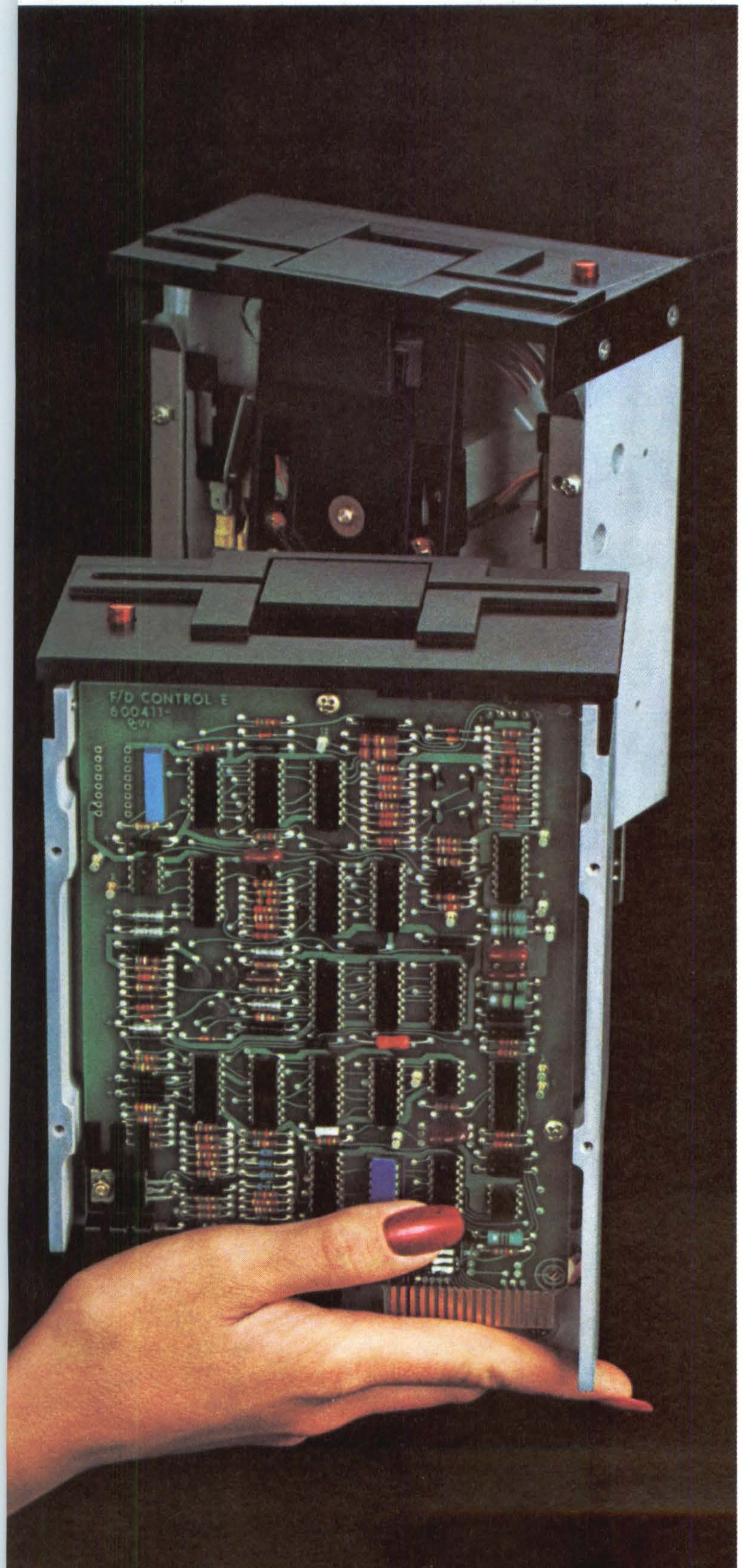

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TABLE 3

Representative CRC Polynomials and Final Results When Used With CRC Character Generation Schemes (Tables 1 and 2)

Generating Polynomial	Unique Nonzero Final Result
A) $x^{11} + x^{10} + x^6 + x^5 + x^4 + x^2 + 1$	$x^{10} + x^9 + x^8 + x^7 + x^6 + x^5 + x^4 + x^3 + x^2 + x + 1$ 11111111111
B) $x^{16} + x^{12} + x^5 + 1$	$x^{12} + x^{11} + x^{10} + x^8 + x^3 + x^2 + x + 1$ 0001110100001111
C) $x^{22} + x^{13} + x^2 + 1$	$x^{17} + x^{16} + x^{15} + x^{14} + x^{13} + x^6 + x^5 + x^4 + x^3 + x^2 + 1$ 0000111110000001111101

Note: Desirable error detecting capabilities of A and C may be found in Ref 1. B represents generating polynomial used in SDLC, HDLC, and ADCCP bit-oriented protocols.

register and longhand approaches correspond to the same division process.

It is clear from the second example that the result of Exclusive-ORing the remainder (R) at the end of the data in the absence of errors (see Eq 1) with the CRC bits is then $R + \bar{R}$, which represents a character of all 1s. Padding with zeroes and continued division is then equivalent to dividing a reference polynomial (the result of concatenating a character of all 1s with a character of all 0s) by the generating polynomial. This is seen explicitly in Table 2 in the step following the receipt of the remainder character, where $R + \bar{R}$ plus padding equals 1111100000. Since the result will always be of this form if no errors have occurred in transmission (but will have different lengths depending on the length of $P_n(x)$), the final contents of the shift register or the final result of completing the division will be a unique bit string. The specific bit string for a given $P_n(x)$ is then easily determined by dividing the reference polynomial by $P_n(x)$. The results of this operation for three different choices of $P_n(x)$ are presented in Table 3.

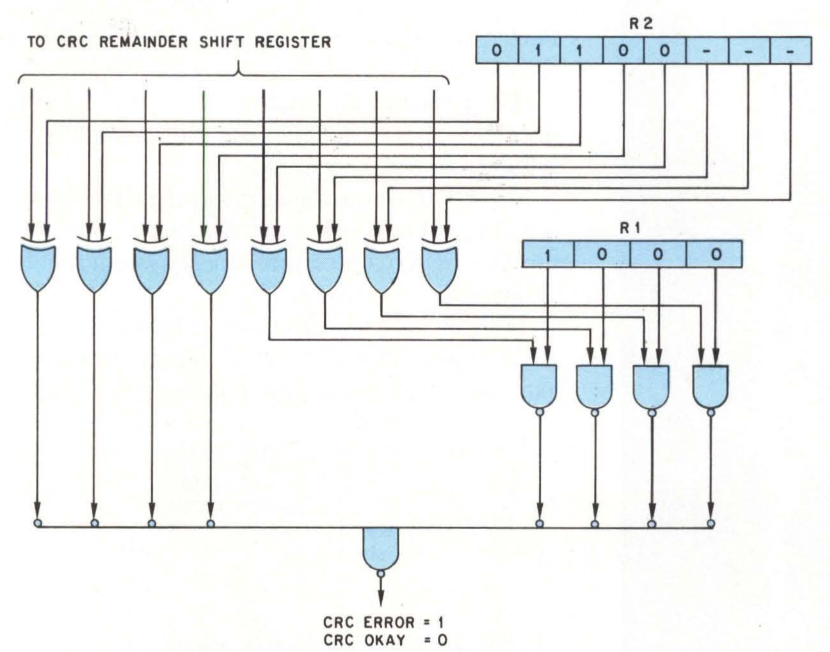

Fig 2 Diagram, comparing final result of CRC for several different polynomials containing at least four and at most eight bits, uses polynomial $P_5(x) = x^5 + x^2 + 1$. R2 contains bit pattern to be matched; R1 contains mask bits for unused bits in R2

This longhand approach represents a possible method for implementing CRC checking in software, especially when an integral number of characters is always transmitted. Note that in this case, the result of Exclusive-ORing R with $\bar{R}$ is sufficient to detect error conditions, and the division does not have to be continued. That is, in the absence of errors, $R + \bar{R}$ is equal to a character of all 1s. Thus, when a message delimiting (flag) character is received, $R + \bar{R}$ can be formed and compared with the all 1s state. Then, the problem with erroneous trailing 0s is eliminated without the need to continue the division process beyond this point. This can represent a significant computational savings. It is clear, however, that a mechanism

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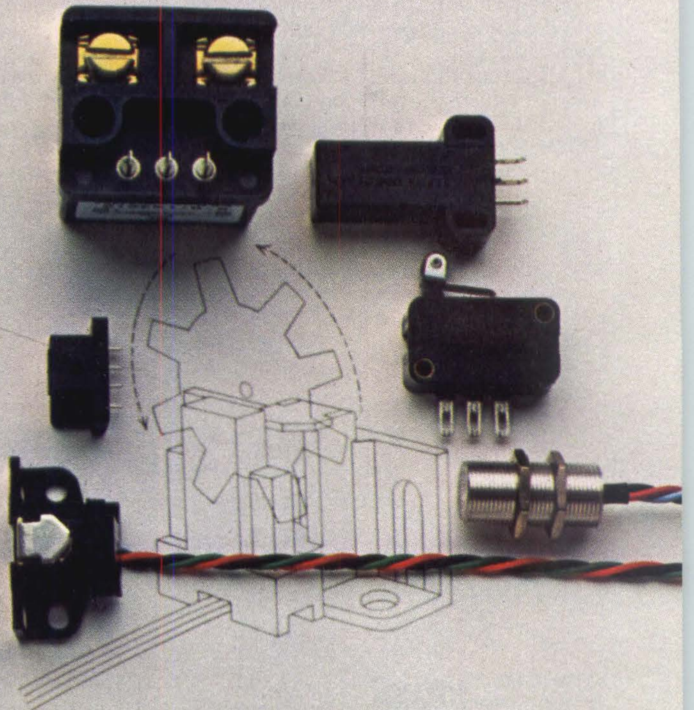

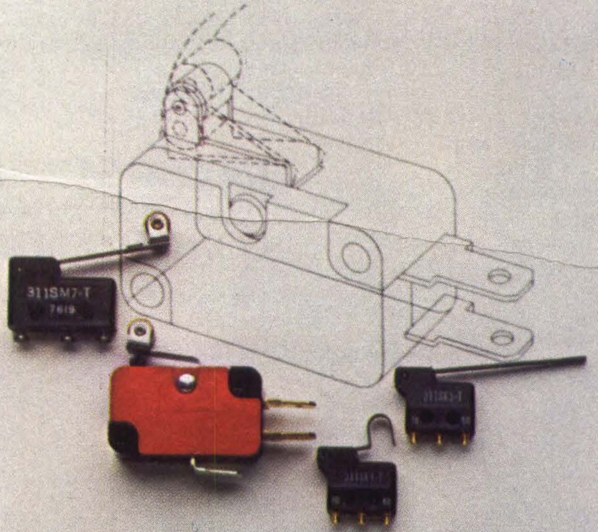

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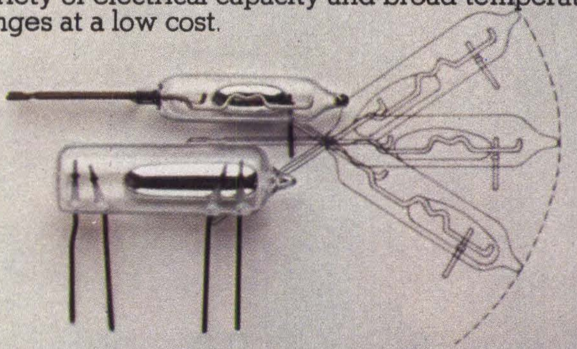

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that looks ahead for the CRC character must be employed in this case.

Hardware Considerations

In the design of ICs using the shift register approach, it follows that for bit-oriented protocols the ability to compare the final remainder with the contents of an additional register should also be included. Since the length of the various generating polynomials may be different, the use of another register (R2) to mask out the unwanted bits is implied. A possible approach is illustrated in Fig 2. Here, the contents of R1 are set up so that a logic 0 is loaded in those positions that correspond to bits in the CRC remainder shift register that can be ignored. For example, if a given line adapter were to be used with 16- and 24-degree polynomials, the equivalents of two 24-bit and one 16-bit shift registers would be employed. The contents of R1 would be all 1s for the 24-bit case, and would consist of eight 0s and eight 1s in the 16-bit case. The contents of R2 would be set in accordance with the specific polynomial as described above.

Conclusions

The discussion has presented a well-known mechanism used to eliminate problems relating to erroneous leading and trailing 0s in bit-oriented protocols; it consists of presetting the contents of a CRC shift register to an all 1s state and transmitting the inverted remainder as the CRC bits. Also described are hardware and software techniques to handle CRC computations, and features of ICs to be used in line controllers. Through elucidation of the basis of the method, a simple manuever is formulated for users/designers to determine the specific form of the final remainder at the receiver for any polynomial, without having to proceed through the various shift register states one bit at a time.

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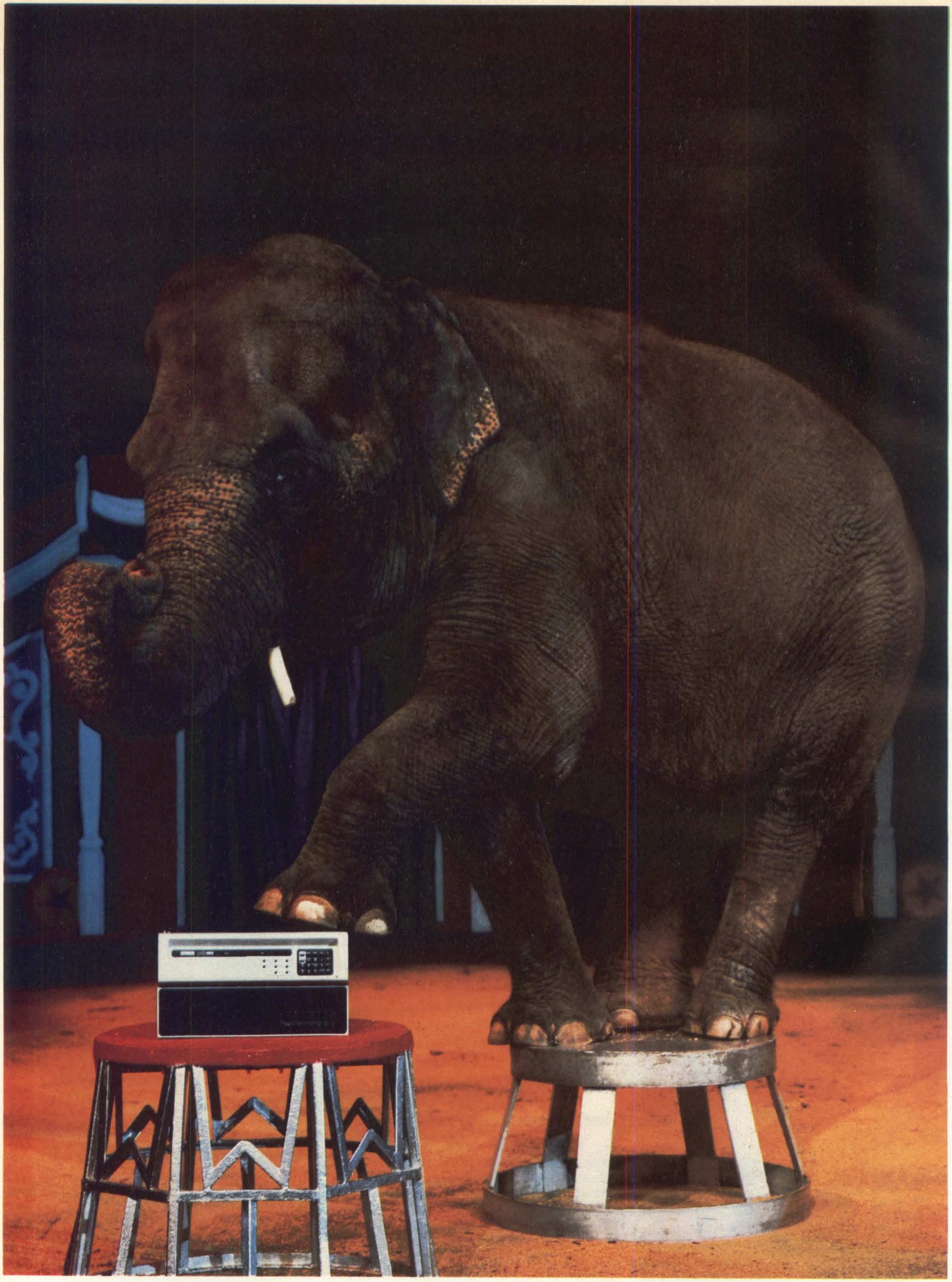
1. H. C. McKee, "Improved CRC Technique Detects Erroneous Leading and Trailing 0's in Transmitted Data Blocks," *Computer Design*, Oct 1975, pp 102-106
2. W. W. Peterson and D. T. Brown, "Cyclic Codes in Error Detection," *Proceedings of the IRE*, Jan 1961, pp 228-235



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Microcomputer Interfacing: Preparing Your Programs

Jonathan A. Titus
Christopher Titus
Tychon, Inc

David G. Larsen
Peter R. Rony
Virginia Polytechnic Institute & State University

One of the difficulties facing many microcomputer users is the preparation of software for their particular applications. Software examples contained in past columns were short enough to assemble by hand, ie, each mnemonic was translated into its octal, hexadecimal, or binary equivalent. Usually listed in sequential order on the rough draft, addresses for jumps, calls, and input/output devices can easily be added or changed since the computer programs are short. Unfortunately not all software preparation is this easy. Many application programs contain thousands of steps. This month's column initiates a discussion of microcomputer program development aids which are available.

The clear, concise statement of the problem and how it is to be solved is one of the largest problems in software development. All of the desired results, inputs, outputs, and complete program flow—including all decision-making steps—must be considered before programming is started. While outline or block diagram form is acceptable, a flowchart often proves to be much easier to follow (see Figure).

The next step is to make a decision: Is the program short enough to be easily translated by hand? In many cases, particularly where the programs are simple, hand assembly makes sense. In other cases software development aids called editors and assemblers are faster and more efficient (see Glossary of Terms).

To understand how editors and assemblers work, consider the analogous example of writing a manuscript. The first step is to outline the subject to ensure that it is well covered in the allotted space. The editing process requires the copy to be corrected and typed, perhaps several times; illustrations and examples are formulated and drawn separately. When the article is composed or assembled, direct references to tables and figures (eg, Table 5) are easier to follow.

Computer software is developed in much the same way. An editor program is used on either a microcomputer or timesharing system to edit individual program steps, which includes correcting, changing, inserting, and deleting steps. Since most editors can be used to perform many functions, the editor program generally is unaware that a computer program is being written. When an editor is used to prepare a program in mnemonic form, symbolic addresses are often assigned to software tasks within the program. In this way the actual value of the addresses for subprograms or subroutines is not needed; for example, the program may refer to the letters LOOP as the starting address of a time delay loop. This use of symbolic addresses for program steps allows a program to be changed without regard to the actual numeric values of addresses.

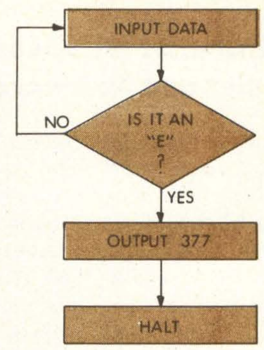
The assembler program must be such that it accepts information from the editor and generates an output in computer-compatible form. The assembler, which functions by performing one step at a time, contains a table

Glossary of Terms for Software Preparation

Editor	A program allowing such edit functions as addition of a line or character, insertion, or deletion to permit altering of a program. Input data can be anything from programs or reports to raw instrument data.
Assembler	The program that converts assembly language code into machine code, accepting mnemonics and symbolic addresses instead of actual binary values for addresses, instructions, and data.
Monitor	Controlling the operation of the various programs available, the monitor can access the editor, assembler, or other programs.
Debugger	A program which allows the user to observe the program flow and results of the program's operation in a step-by-step mode. It may be used to change data or instructions, alter registers, etc.
Breakpoint	This special instruction may be inserted in a program to break off the normal program control and return control to a debug-type program. When a breakpoint is executed, the debug program indicates what the computer was doing at that point.
Cross Assembler	A type of assembler program which generates binary code of a program for a computer other than the model it is being used with; eg, an 8080 cross assembler might operate on a PDP-8 minicomputer.

Software Listing of Typical Assembler Output

```
                                 *003 000
003 000 061      START,          LXISP        /Symbolic address of START
003 001 377                      377
003 002 003                      003
003 003 333      LOOP,           IN           /Input data from port 5
003 004 005                      005
003 005 376                      CPI          /Compare it to 026
003 006 026                      026
003 007 312                      JZ           /If it matches, go to DETECT
003 010 015                      DETECT
003 011 003                      0
003 012 303                      JMP          /If it doesn't match, go to
003 013 003                      LOOP         /LOOP and check again
003 014 003                      0
003 015 171      DETECT,         MOVAC
003 016 323                      OUT
003 017 007                      007
003 020 166                      HLT
```



Typical flowchart with input, output, and decision-making steps

of mnemonics and their equivalent values. For example, an 8080 assembler would translate an MVIA instruction into 076 octal. The assembler also assigns real, 16-bit addresses to symbolic addresses, such as LOOP. The user must be sure to have a program step for each symbolic address and must assign an address if a symbol is used. The same "name" cannot be assigned to more than one address. Most assemblers recognize a redefined or undefined symbol and produce an error message indicating what needs to be corrected.

Final assembler output is in punched paper tape, cassette, or disc form ready to run on the system. Most assemblers also produce a listing of the program showing the address of each step, the data in each successive location, a symbolic address name, and the mnemonic plus any comments. A typical assembler output is shown in the Software Listing.

After a program is assembled, it probably will have to be debugged in order for it to operate properly. Program checkout and debugging can be a painful process without additional software tools. Computer control panels are often useful, but reading binary codes can become tedious and many computers do not have external controls and readouts. As an alternative, debugging programs are available for most microcomputers to allow the user to change instructions, list blocks of data or instructions, and single-step through a program.

Many debug programs feature the ability to establish a breakpoint in the software being tested. When the computer reaches a breakpoint, the instruction at that address is executed and an output device such as a teletypewriter lists the contents of important, internal CPU registers. Breakpoints are very useful since they indicate not only that the computer reached a certain point in the software, but also what the computer was doing when it got there. If a breakpoint is set in the normal program flow and is not reached, there is obviously something wrong with the program. In this case, the breakpoint would be moved closer and closer to the start of the program until the error is found. The error then may be corrected by using the debug program to change an instruction, data, etc.

Once the program is operating correctly, the debug program should be able to retain it on paper tape, cassette, or other medium, and also should be able to read such programs back into memory. In any case, when errors are found the software should probably be re-edited and re-assembled to produce a complete, error-free, documented listing.

Since most programs contain errors, it is valuable to have a permanent debug program with the computer, preferably stored in read-only memory (ROM) or programmable ROM (p/ROM). This is advisable since "run away" programs being tested might alter the debug software, necessitating its reloading. Many debug or monitor programs are available; Intel Corp's Insite software library lists at least four. Editor/assembler programs also may be resident in p/ROM. The low cost of both read/write memory and p/ROM chips suggests that many users will keep standard system programs such as editors, assemblers, and debug resident in their system. The alternative is a paper tape, cassette, or disc-based software package which must be read into memory before each use.

Cross assemblers also are available to generate an assembled program, but for some other computer. For example, a PDP-11 might be able to cross assemble 8080 microcomputer programs. Cross assemblers can be powerful since some also incorporate simulation programs to test the program.

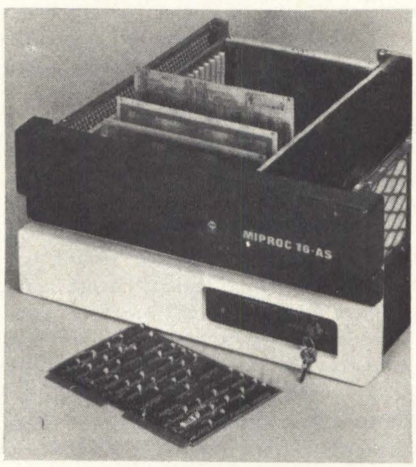
For testing programs we use DBUG, an 8080 interactive debugger written by C. A. Titus (E&L Instruments, Inc, Derby, Conn, 1977); the assembler output shown in the program example is that produced by the Tychon editor/assembler (TEA). Both are resident in our 8080 system on p/ROM chips.

This article is based, with permission, on a column appearing in *American Laboratory* magazine.

Expansion of Microcomputer Family With System Modules and Software Is Aimed At OEM Applications

A range of high performance system modules and additional software have been specifically designed by Plessey Microsystems, Microcomputer Products, 1641 Kaiser Ave, Irvine, CA 92714 to enable fast realization of high performance OEM computing systems. Designated Miproc 16-AS (application system), the family consists of the standard 350-ns instruction time Miproc-16 CPU card supported by processor, memory, and interface modules, which are plugged into a 13-card bay with integral power supply.

The card bay modules can be enclosed in a 19" (48-cm) rack-mounting chassis unit. It accommodates one or two card bay modules and has fan units and an operator's panel. The chassis can hold two card bay modules organized as independent systems, or the second card bay can be used as an extension of the first. A 3-bay version is available for multiprocessor configurations.



Enhancing its Miproc-16 microcomputer, Plessey has added processor, memory, and interface modules for OEM systems applications. Modules are plugged into 13-slot card bay with power supply; chassis unit can hold up to three card bay modules

Processor modules include the CPU, an optional index register/interrupt module, and optional hardware multiply peripheral for higher speed applications. Also available is a combined power monitor and real-time clock module which monitors both ac and dc power rails.

A high speed 2k bipolar RAM, high speed 8k bipolar p/ROM, and applications memory providing 4k p/ROM and 256-word RAM comprise the memory cards. Also included is a 2k CMOS RAM with integral battery to provide nonvolatile alterable peripheral storage. Interface cards include programmable serial line interface, 2-channel 16-bit parallel bidirectional I/O card, and 6-channel parallel input, as well as output, cards.

The PL-Miproc language, which resembles ALGOL in structure, is suited to structured programming; it reduces the time required to develop application software. The cross-compiler runs on DEC's PDP-11 computers under the RT-11 operating system. Compiled code is in the proper format to be loaded into the Miproc-16 prototyping system.

As an aid to program development at the testing and debugging stage, the Monitor module consists of a set of three cards that are housed either in the 16-AS chassis or the Miproc-PK real-time prototyping kit. It provides a facility to interrogate, inspect, and update program and data memories in the system via a teletypewriter or compatible device; programs are run in near real-time conditions. Using the Miproc processor to help diagnose errors, the monitor features multiple trace, multiple trap, and backward trace.

Circle 170 on Inquiry Card

Increased Functions of µComputer Family Support Added Applications

The MN1400 series of three microcomputers (models MN1400, 1402, and 1498) and an evaluator chip (1499) which can perform tests on the series offer more onchip functions to fill the application gap between 4- and 8-bit units. Built by Panasonic Electronic Components, One Panasonic Way, Secaucus, NJ 07094 with n-channel E/D MOS process, the chips incorporate functions previously included in auxiliary circuitry—an 8-bit presettable counter/timer, clock generator, 1024 x 8-bit instruction ROM (1400 model), 64 x 4-bit RAM with four directly addressable words, ALU, two 4-bit parallel input ports, 4-bit parallel output port, and 8-bit PLA decoded output port.

Other user-oriented features are two sense input lines, counter select input line, power-on reset input line, and 12 discrete output lines. With single power supply operation (4.5 to 6.0 Vdc), the units have a 10-ms instruction cycle time, 75 instructions, and subroutine nesting to two levels. Models are available in 28-, 40-, or 64-pin DIPs.

Circle 171 on Inquiry Card

Development System Stores 300k Bytes on Floppy Disc

A compact program development system, the Z80-PDS provides complete support for developing and debugging Z80 microcomputer programs. The standard system, expandable via options, includes a floppy disc drive with up to 300k bytes of online data storage, internal memory of 3k bytes of p/ROM and 16k bytes of RAM, and serial I/O with RS-232 or strappable current loop interface.

Zilog, Inc, 10460 Bubb Rd, Cupertino, CA 95014 also supplies software which includes disc resident operating system, editor, assembler, debugger, and file handling utilities. Consisting of a card enclosure and disc unit, the system sells for $2850 in single quantities.

Circle 172 on Inquiry Card

Digital Output Boards Are Compatible With 6800 Microcomputers

Memory mapped, plug-compatible 16- or 32-channel isolated digital output systems, MP701 and MP702, respectively, are available for Motorola Micromodule and EXORciser[R] microcomputer systems. Introduced by Burr-Brown, International Airport Industrial Pk, Tucson, AZ 85734, the systems contain all necessary control and timing circuitry, and include

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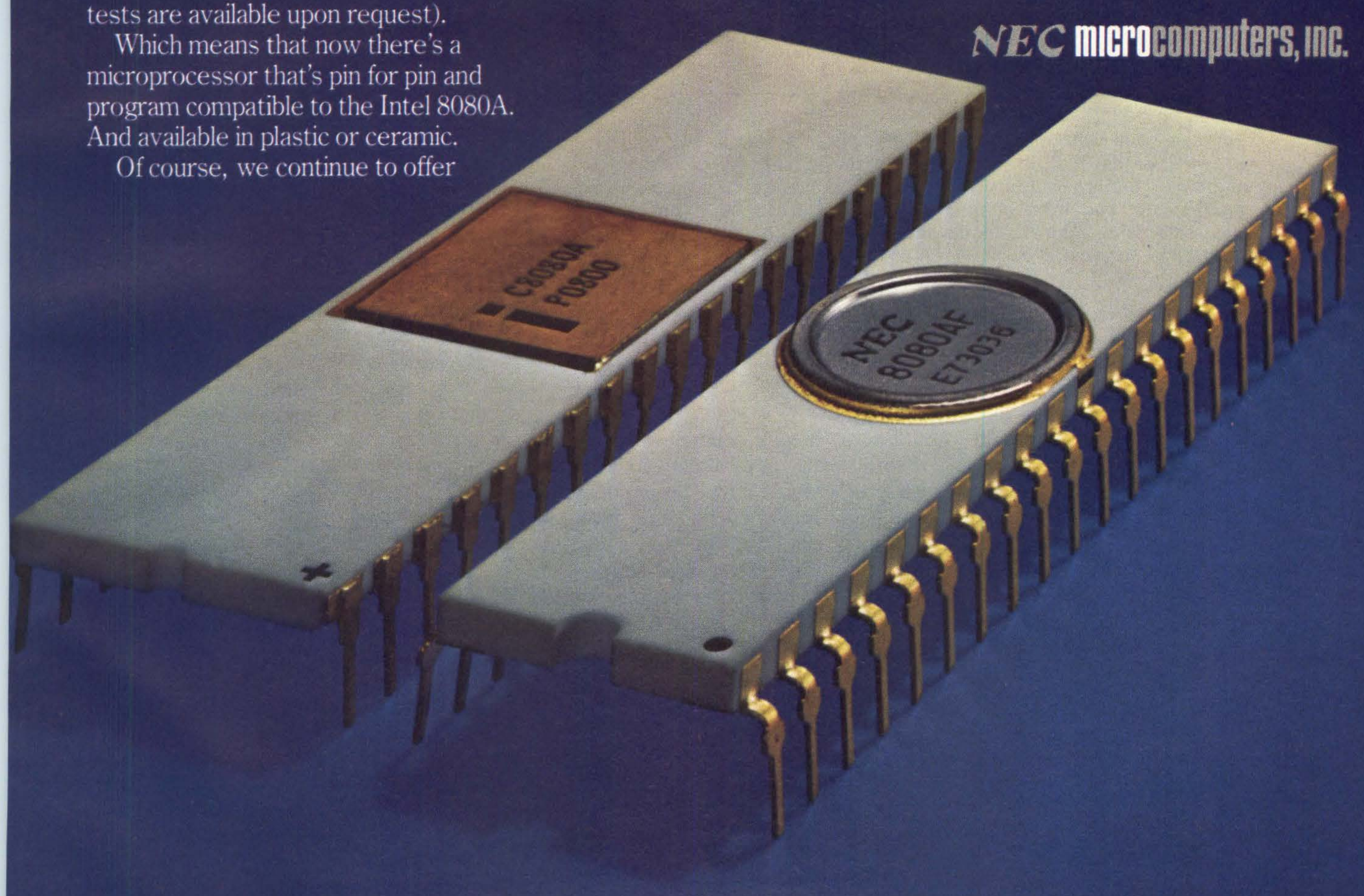

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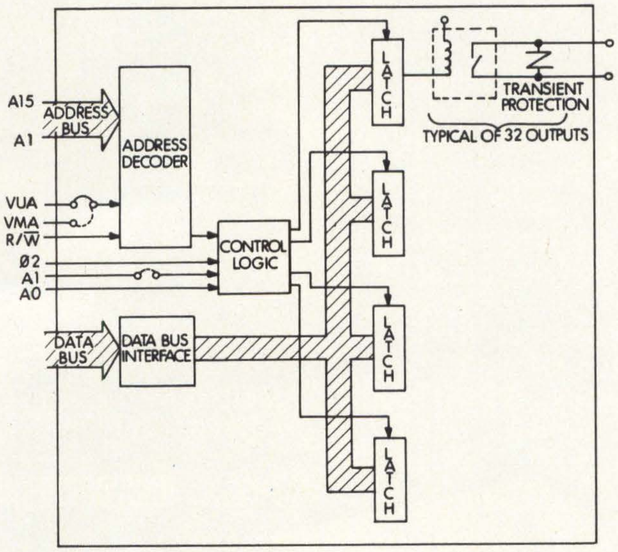


For use with Motorola 6800 microcomputer systems, Burr-Brown's digital output microperipherals (either 16 or 32 channels) feature outputs isolated from computer bus up to 600 Vdc, and from channel to channel up to 300 Vdc. User-selectable address block occupied by each board can be placed anywhere in memory

contact-closure outputs rated at 28 V and 0.5 A (resistive load).

Mechanically and electrically compatible with Motorola systems, the units operate from the microcomputer's 5-Vdc supply. For ease of programming, the units are treated as memory by the CPU. Eight output channels occupy one memory location.

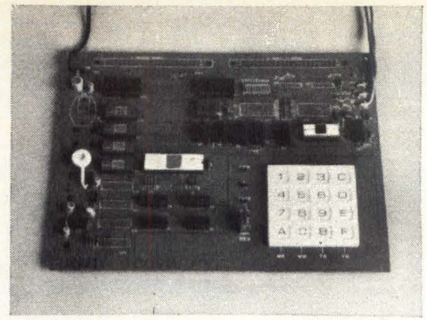
Each output channel is implemented with a protected reed relay, used to provide low "on-impedance," and high output current and isolation. Outputs are capable of switching inductive loads. Transient suppressors are used across each output switch to protect open contacts from voltage surges.

Circle 173 on Inquiry Card

Video Interface Processor Combines Low Cost With Expandability

With the Cosmac VIP video interface processor kit, a hobbyist can assemble a microcomputer with which to create and play video games, generate graphics, and develop microprocessor control functions. Priced at $275, the kit offers an operating system in 4k bits of ROM. Components include the CDP1802 microprocessor (see *Computer Design*, Apr 1976, pp 132, 134), a 2048-byte RAM which uses 4k-bit static RAMS, single-chip graphic video display interface, built-in hexadecimal keyboard, 100-byte/s audio tape cassette interface, and wall plug regulated power supply all on a single 8.5 x 11" (21.6 x 28-cm) PC card.

Output directly interfaces with a monochrome CRT display or, when used with an FCC-approved modulator, a TV receiver. The 512-byte ROM operating system simplifies such tasks as loading programs into RAM via the keyboard, recording RAM contents on cassette tapes, examining memory and registers, and displaying memory bytes in hexadecimal format on a CRT.



Complete 4k-bit ROM computer on one PC card, RCA Solid State Div's Cosmac video interface processor is based on CDP1802 microprocessor. Expandable hobby kit is useful for video games, graphics, and microprocessor control functions

Chip-8 interpretive programming language has 31 instructions in a 2-byte format; it is capable of providing 16 1-byte variables and permitting subroutine nesting. Programs can be stored on cassette tapes.

RCA Solid State Div, Box 3200, Somerville, NJ 08876 has designed the processor for future expandability, both on the PC card and through connectors. RAM capacity can be doubled on the card to 4096 bytes by adding four 4k-bit devices. A 44-pin connector socket accepts added devices for up to 32k bytes of memory, as well as other circuitry. Parallel I/O expansion to 19 lines is possible.

Circle 174 on Inquiry Card

Development System Aids Design of 16-Bit Microprocessor Systems

Fully assembled on a PC board, the PACE low cost development system (LCDS) allows engineers to develop, test, and debug PACE hardware and software designs. To simplify program checkout, the unit operates in single-step or continuous mode with breakpoints. It also permits memory and register contents to be viewed, printed, and modified.

Contained on the card are a 16-bit PACE microprocessor, 1k words of RAM, sockets for 1k words of P/ROM, 20-key dual-function keyboard, 6-digit LED display, system timing element, I/O buffers, and bidirectional transceiver elements. A 20-mA current loop or RS-232 port is available.

Satisfy Your 8080 Microcomputer Design, Test and Service Needs

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MUPRO FEATURES	YOUR BENEFITS
Real-Time Execution from emulator or users' system memory	More thorough and flexible system test capability
Multi-User/Multi-Task Disk Operating System (MUTE)	More efficient use of software personnel permits simultaneous use by up to four programmers
Block Structured Assembly Language (BSAL) and user oriented software packages	Saves software development and maintenance time while retaining the size, speed and flexibility of assembly language programs
Transparent Control/Display Console	Provides total use of microprocessor. No memory, I/O or interrupt restrictions
Compact and ruggedized system packaging	Single system provides total solution to development, test and field service needs

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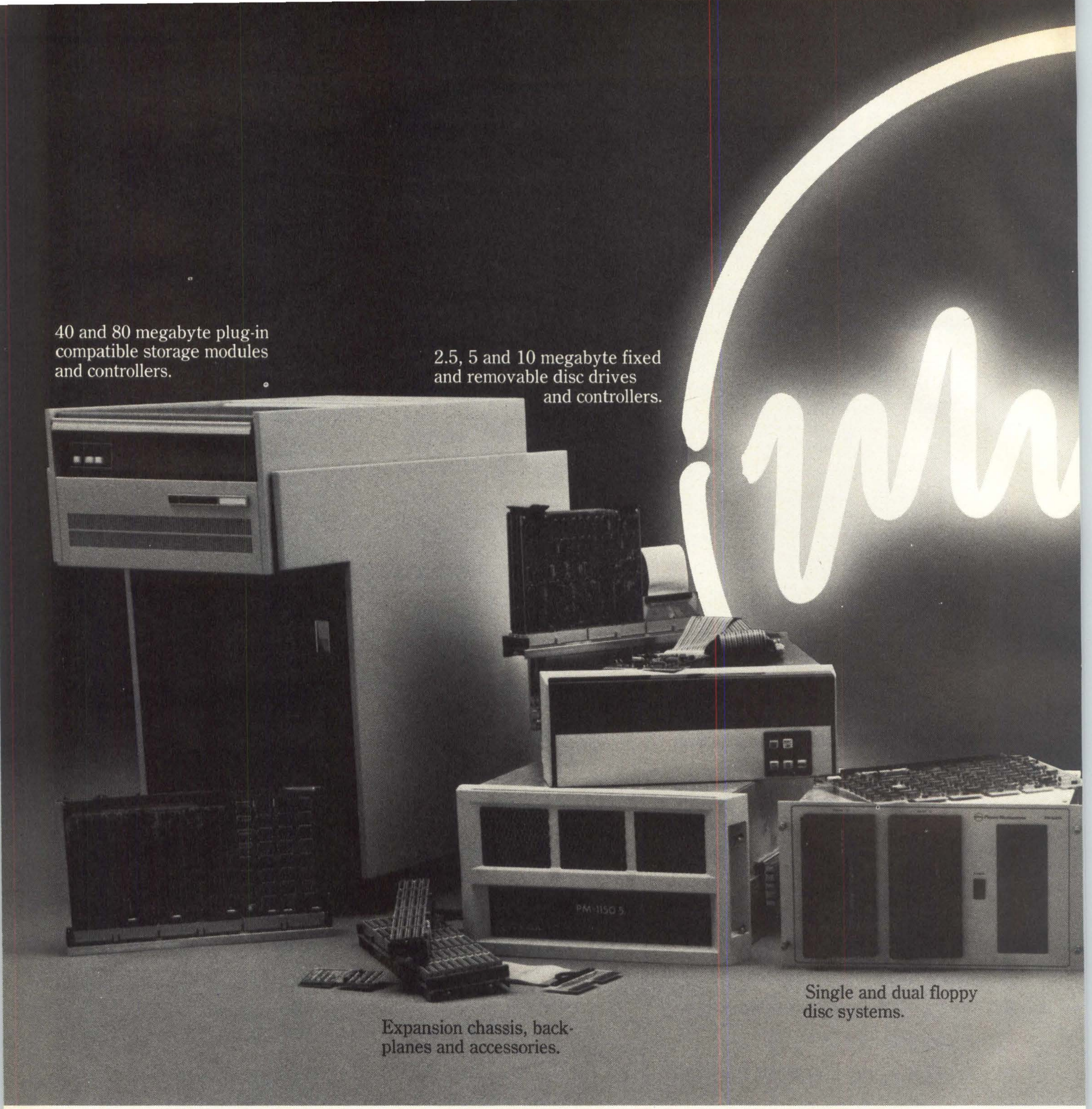
Circle 62 for demo and technical data

Circle 153 for technical data



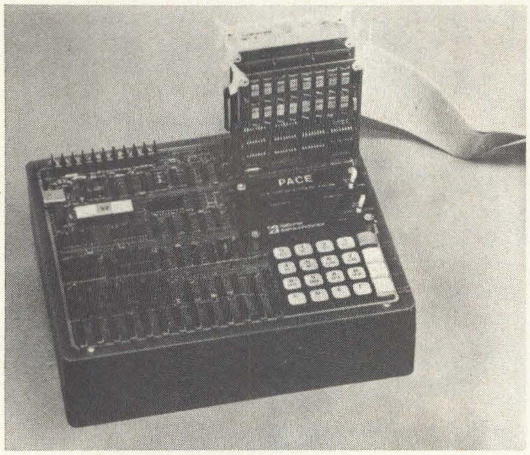
Everything you need to

know about DEC peripherals:

Plessey offers a complete line of DEC compatible products. Reliability, quick delivery and substantial cost savings are some of the reasons to make Plessey your supplier. For complete price and delivery information, please contact the nearest listed sales office.

Plessey Microsystems

Copenhagen (01) 12.48.03/Helsinki (080) 542.077/Paris (01) 727-4349/Munich (089) 351-6021/Neuss (Düsseldorf) (02101) 44.091/W. Berlin (030) 24.72.12/Milan (02) 688-2324/ Turin (011) 61.63.33/Zeist (Utrecht) (03404) 21.344/Oslo (02) 15.00.90/Madrid (01) 252-37.22/Stockholm (08) 23.55.40/Geneva (022) 82.55.30/Zurich (01) 50.36.55/Towcester (Northants) (0327) 50.312/Tolworth (01) 330.4100. SERVICE CENTERS UNDERLINED



Users are able to develop, test, and debug designs at low cost with National Semiconductor's PACE development system. Code for building application routines is entered through keyboards or external terminal. Firmware, resident in onboard p/ROMs, provides system monitoring capabilities and controls subroutines for I/O devices

National Semiconductor Corp's Microcomputer Group, 2900 Semiconductor Dr, Santa Clara, CA 95051 has designed the system so that its microprocessor can be isolated from the system bus, allowing an external PACE to use the LCDS memory and peripherals. Three sockets allow for added memory or extension of the interface bus. Unit costs $585. An IPC-16C/011 card supplies 1k x 16 bits of RAM, and the /012B card has sockets for up to 2k x 16 bits of ROM or p/ROM.

The 80-character, 24-line video output device features a character set with upper/lower case characters, punctuation, and underline. Characters can blink at a user-selectable rate, and can be made to appear brighter or in reverse field. Custom character sets are available.

Forms overlays, charts, graphs, or order entry forms can be generated on the screen. Continuous gray scale elements are displayed in any of nine levels in any of 1920 positions on the screen.

The 2-board, S-100 based system occupies 2k of RAM address space and two I/O ports. Timed screen updates occur only during retrace when the screen is totally blanked.

Software support includes machine language code with fully commented source listings, and a BASIC software package. A link program is provided in BASIC. Assembly language drivers allow the system to be customized. Kit price is $285.

Circle 176 on Inquiry Card

Upgraded Single Card 8080A-Based System Doubles Memory Capacity

The PLS-888 programmed logic system offers 1k of RAM, and sockets for an added 1k of RAM and 8k of TMS-2716 p/ROM. The 4.5 x 6.5" (11.43 x 16.51-cm) card includes an 8080A microprocessor, crystal clock, built-in power-on reset, 16 lines of TTL input, and 24 lines of TTL output. Pro-Log Corp, 2411 Garden Rd, Monterey, CA 93940 has designed the card to be plug-compatible with its PLS-881 4k ROM card.

Circle 175 on Inquiry Card

Disc and Video Display Systems Are Compatible With S-100 Bus Devices

The MSDD-100 disc and MSDV-100 video display systems are intended for hobby and small business applications using the S-100 bus. A Shugart SA-400 minifloppy™ drive and LSI controller are utilized by the low power, single card floppy disc system. Up to three drives, supported by the synchronous controller, provide all disc timing functions so that no software timing loops are required. Three modes of programmed I/O (no DMA) are a simple command I/O, standard interrupt, and switch-selectable facility to vector the processor to any Restart location upon generation of an interrupt.

The drive has 89,600-byte maximum data capacity and 35 tracks. Average access time is 600 ms (random R/W). Power requirements are 8 V, 200 mA max; 15 V, 20 mA max; and −15 V, 10 mA max.

Software provided by Micro Systems Development, Inc, 2765 S Colorado Blvd, Denver, CO 80222 includes two diskettes—for user programs and files, and for an array of system programs. An 8080 monitor permits formatting of diskettes and diagnostic checks. A bootstrap loader, memory-to-disc routines, and disc I/O routines are provided. Mits BASIC software can be run with the system via a link; a BASIC program is also included. Price is $499.

High Speed Verifier and Library Upgrade Logic Simulation Software

Upgrading of the Logcap logic simulation software system, which simulates an entire microcomputer system down to the gate level, has been accomplished with the addition of a high speed fault verifier along with a full set of user commands, and a proprietary library including the Advanced Micro Devices 2901 bipolar microprocessor. The fault verifier analyzes up to 1k faults at one time.

Logcap, jointly owned by Ungermann Associates, 832 Nash Rd, Los Altos, CA 94022 and RRC International, Inc, Troy, NY 12181, can verify stuck-at-one and stuck-at-zero faults on inputs and outputs to any node. Addition of the Am 2901 to the library helps define that logic element and assures correct representation of the circuit.

Circle 177 on Inquiry Card

The complete $655 line printer.

It's ready to plug in, has an 80-column format, a remarkable MTBF and is 14 times faster than a teletype!

Breaking the hardcopy barrier

It's finally happened! The Axiom EX-800 provides full performance hardcopy at a price compatible with today's low cost micros. This little 80-column machine zips along at 160 characters per second (14 times faster than a teletype)—at a breakthrough single quantity price of $655 for a complete printer.

When we say complete we mean it

The EX-800 is a stand-alone unit with case, power supply, 96 character ASCII generator and interface, paper roll holder, infra-red low paper detector, bell, and multi-line asynchronous input buffer. You won't find these standard features on any other printer, regardless of price!

Our only option

Our printer is so complete, that we offer only one option. A serial interface (RS 232C or current loop) good for 16 baud rates from 50 to 19,200 and thoughtfully provided with a switch for either Centronics or Tally compatibility. Might we call it a Tally-whacker? At $85.00 it certainly should be!

Built-in LSI microprocessor

The heart of the EX-800 is a printed circuit card, containing a custom LSI chip made by Intel to Axiom specifications, which controls all printer functions. Microprocessor power means flexibility. Such as the built-in self test routine and variable character size. It also means reliability. Several industry surveys have shown LSI to be many times more reliable than equivalent conventional circuitry.

THIS LIFE-SIZE SAMPLE SHOWS THE 80-COLUMN PRINTOUT FROM AXIOM'S EX-800 PRINTER

There are 3 character sizes (upper and lower case) which can be MIXED.

This can have the same effect as UNDERLINING or changing COLOR.

The advantages of electrosensitive printing

The EX-800 can print 80, 40, or 20 characters across the five inch wide electrosensitive paper. Under software control, single characters or words may be printed larger for emphasis. The permanence of the hardcopy is archival, because once the aluminum coating has been removed, there is no way to put it back. It's unaffected by sunlight, moisture or heat. Although the printer doesn't provide multiple copies, excellent quality photocopies can be made from the high contrast printout. Also, the paper is inexpensive and readily available, costing about 1¢ for an 8½ x 11" equivalent.

Light, small, quiet, reliable, and versatile

Our EX-800 weighs in at 12 pounds, is just 9½ inches wide, 4 inches high, and 11 inches deep, and is delightfully quiet which makes it ideal for office and other low noise environments. The simple print mechanism is virtually maintenance free. In fact, tests show an incredible MTBF, many times greater than impact printers. This versatile printer is the ideal mate for micros, minis, CRTs, instruments and systems.

Just unbox and plug it in

That's all you have to do to the Axiom EX-800 — apart from pay for it, and at $655 that's almost a pleasure.

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Glendale, CA 91202

- ☐ Urgent. Please phone me at ext ____
- ☐ Have rep contact me
- ☐ I'd like to have a demonstration
- ☐ Send lit including sample of printout

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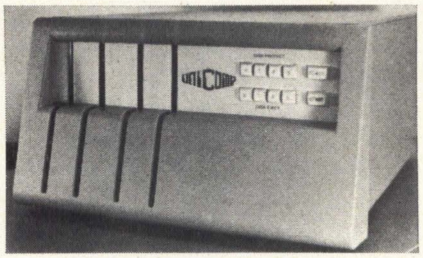
CIRCLE 64 ON INQUIRY CARD

MICRO PROCESSOR / COMPUTER DATA STACK

Fully Integrated 16-Bit μComputer System Delivers Power of LSI-11

The SS-11/15 is a cost-effective, dual or quad disc-based system packaged in a 10.5" (26.7-cm) rack or table-



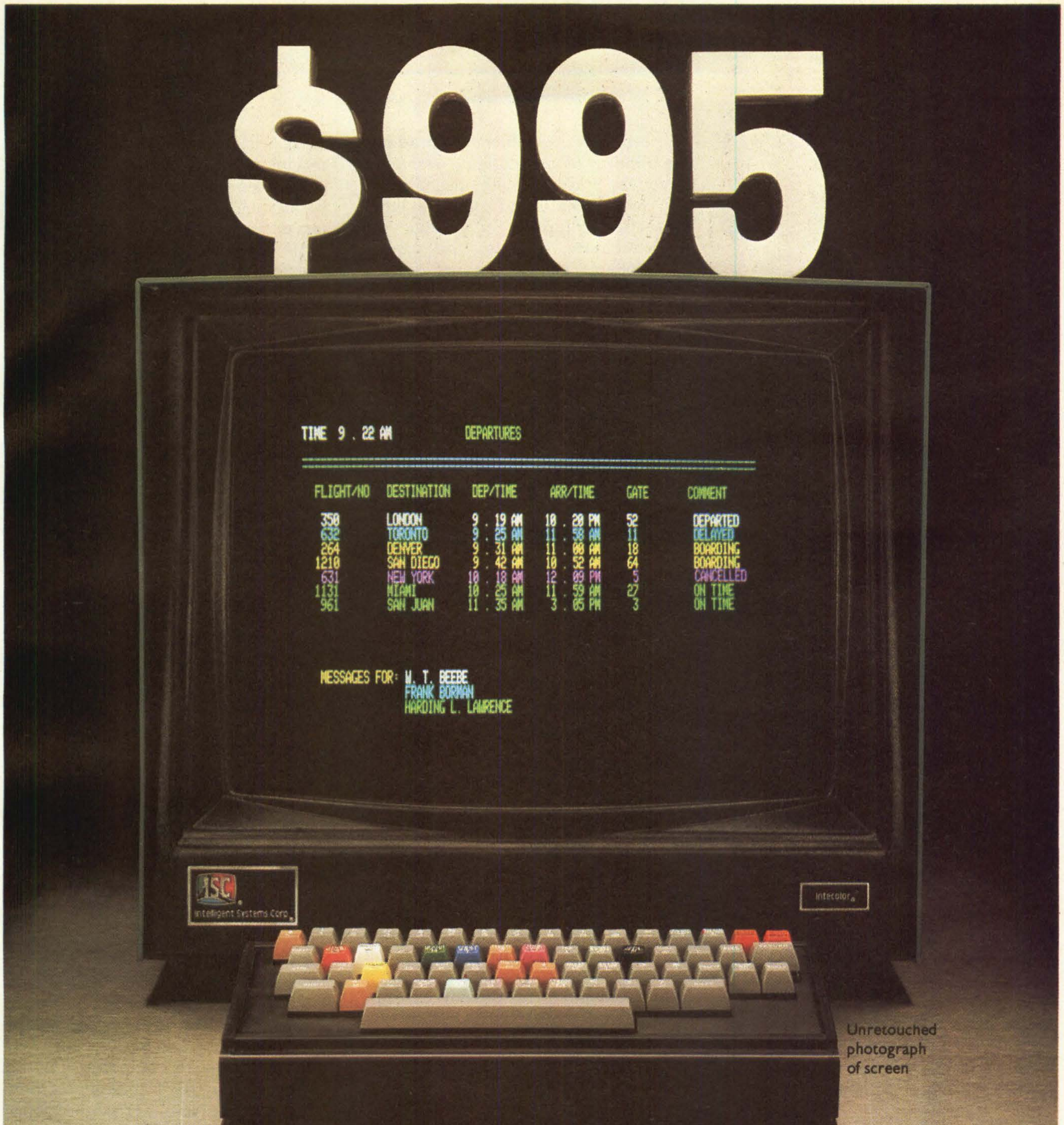
top mounting enclosure. Hardware includes a 15-quad slot backplane, integral switching mode power supply, an LSI-11 CPU with EIS/FIS MICROM, 20k- to 28k-word RAM, console interface, diagnostic/bootstrap p/ROM, bus terminator, console switch register, distributed refresh controller, and front panel controls/displays. Compatible with operating system software such as RT-11 and RSX-11/S, the system from Unicomp, Inc, 8950 Westpark, Suite 312, Houston, TX 77063 features an array of source languages including Multi-User BASIC, FORTRAN IV, and Macro-11.

Circle 178 on Inquiry Card

Packaged Microcomputer System Offers APL Capabilities

The APL/X3 microcomputer system consists of the DEC LSI-11™ CPU packaged in a 16-slot backplane with 28k words of MOS memory, extended instruction set, and floating point arithmetic. General Robotics Corp, 57 N Main St, Hartford, WI 53027 has fabricated the system with a 10M-byte cartridge disc (one fixed, one removable platter), APL CRT with 24 lines of 80 char, and an APL printer with 132 columns and speed of 60 char/s. Software is DEC RT-11™ and APL/RT-11™ with licenses.

Circle 179 on Inquiry Card



Unretouched photograph of screen

Get the jump on your competition without outspending your competition. We're Intelligent Systems Corporation, and we've just lowered the price of our Intecolor 8001 to $995. So now you can upgrade the terminals in the systems you're marketing to color at black and white prices.

The fact is that the Intecolor 8001 has the best price-performance ratio of any intelligent data entry terminal on the market—color or black and white. And that can really add some punch to your sales story. So can color, not because it looks better, but because it communicates better than black and white.

And if you're marketing your systems by promoting the stand-alone capabilities of your terminals, we've got a list of options that'll give you just about any degree of sophistication you want. Including disk storage devices, bi-directional desk-top line printers and a brand new 2708/2716 PROM programmer.

Contact the ISC rep nearest you. We guarantee delivery of your Intecolor 8001 evaluation unit for $995 (cash-with-order) within 30 days or your money back. Or if you've seen the Intecolor 8001 in action and you're already sold on the price and performance, we'll give you the same $995 price for orders of 100 units or more. Get the jump on your competition without outspending your competition. Get the Intecolor 8001.

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CIRCLE 66 ON INQUIRY CARD

TV Course Aimed At Industry Teaches 6800 Microprocessor

A TV microprocessor course consists of 30 half-hour color video cassette sessions—15 introductory and 15 laboratory sessions each cover a particular portion of the 6800 microprocessor system. Based upon the Micro-68 training computer, it was produced for industry by Electronic Product Associates, Inc, 1157 Vega St, San Diego, CA 92110 in conjunction with Colorado State University. Documentation includes a study guide, Micro-68 lab and user's manuals, 6800 programming and system design reference manual, and "Understanding Microprocessors" textbook.

Circle 180 on Inquiry Card

Cassette Interface For µProcessor Programs Operates at 2400 Baud

The Wince cassette interface enables microprocessor programs and data to be loaded and dumped from an audio cassette eight times faster than standard 300 baud. Announced by Wintek Corp, 902 N 9th St, Lafayette, IN 47904, the device interfaces directly to the Motorola 6850 ACIA. The 2.5 x 5" (6.35 x 12.7-cm) module also supports 300-baud Kansas City standard operation and contains an RS-232 interface for standard baud rates from 150 to 9600.

Circle 181 on Inquiry Card

F8 Macro Cross Assembler on Diskette Improves Software Development

An assembler for the F8 microprocessor operates on any Intel MDS-800 development system capable of supporting the ISIS-II operating system. Source programs are compatible between this assembler and those available with the F8 Formulator and from several timesharing networks.

Xener Corp, Suite 211, 6641 Backlick Rd, Springfield, VA 22150 has supplied the assembler with added capabilities of conditional assembly directives and complete macro facility with local and global label generation. Supplied on a single- or double-density diskette, the assembler offers utilization of system peripherals to print listings and enter data into ROMS. Error codes for source program errors are printed on the assembly listing.

Circle 182 on Inquiry Card

Board Brings Debugging and Real-Time Processing To 8080 Systems

Added capabilities of debugging hardware and software, providing timing functions for real-time processing, and implementing timesharing for Altair/Imsai microcomputers is available from the plug-compatible Better Bug Trap (BBT) PC board. Combining the ability to detect addresses with the generation of time intervals, the board provides software programmable functions that operate transparently to applications programs.

Central features are four hardware breakpoint address registers for inserting instructions at up to four ROM locations and a 16-bit clock counter running at 1/256 the system clock rate which can be read as a memory location for timing or as a random number. Breakpoint capability enables the device to stop the processor at an address or generate an interrupt. A real-time clock, interval timer, automatic single-step function, or watchdog timer are possible. The BBT also generates and services its own interrupts.

No modification of programs for timesharing applications is necessary; a simple software routine is included with the BBT so that the system can switch from executing one program to the other rapidly and efficiently. Addressed as if it were 16 bytes in memory, the BBT is commanded from software or front panel.

Micronics, Inc, PO Box 3514, Greenville, NC 27834 includes a standard software package (IBB) with interactive terminal commands, extensive error checking, and commands to set all BBT functions and registers. It also sets and maintains a time-of-day clock. It is supplied as an 8080 assembly language source listing. Assembled and tested, the BBT costs $160 including documentation package and routine IBB.

Circle 183 on Inquiry Card

Formatting Program Offers Capability of Word Processing

Designed for 8080 microcomputers using iCOM floppy discs, the text formatting program comes in hexadecimal ASCII object format on a data diskette ready to run under iCOM's FDOS (II or III). Program input is created under the system's text editor and contains formatting commands and text. Formatted output is written back onto a diskette. Input and output file names of the program from Ortronics, 4753 Irvine Ave, North Hollywood, CA 91602 are specified in a RUNGO command to FDOS.

Circle 184 on Inquiry Card

Multiprocessing Disystem Series for Control Features Floppy Disc

Available as a complete turnkey system or as individual components from Systemathica Consulting Group Ltd, 4732 Wallingford St, Pittsburgh, PA 15213, the 8080-based multiprocessing disystem series consists of a single-board computer; system controller board; a multiplexer supporting two, four, or eight floppy disc drives; and 64k memory subsystems. The computer features 4k static RAM, 4k ROM, two TTY or RS-232 serial ports, six 8-bit parallel ports, buffered bus lines, and memory addressing up to 64k.

A communication and arbitration module, memory cross-access unit, and intelligent multidrive floppy disc controller unit comprise the controller board. Subsystems are a buffered memory decoding motherboard and 16k 8-bit or 8k 16-bit word static RAM boards. Compatible with other 8080 systems, the components are available in various standard configurations. □

Circle 185 on Inquiry Card

Charge-Transfer Devices — Part 1: The Technologies

Eric R. Garen

Integrated Computer Systems, Inc
Culver City, California

Charge-transfer devices have been one of the most rapidly advancing large-scale integration technologies in recent years. While the most publicized of these devices have been charge-coupled device digital memories, the technology and its implications are far more extensive. For example, charge-transfer devices are also finding widespread application in analog signal processing, digital logic, and solid-state image sensing. In this first in a series of three columns, the basic charge-transfer device technologies are described and compared. The next column will describe the history and current status of charge-coupled device memories, and the third will be devoted to signal processing and imaging devices and applications.

To accomplish these diverse tasks, several subsets of charge-transfer device (CTD) technology have been devised to handle analog as well as digital information. The first of these is the charge-coupled device (CCD) itself. A CCD is functionally a shift-register memory for either analog or digital information in which the data are represented as stored charges. The charges in a CCD are stored in a linear array of "potential wells," with the potential of each well controlled by a voltage applied to an isolated metal-oxide semiconductor (MOS) capacitor above the well. By applying a "traveling voltage wave" to this linear array of capacitors, any charges within the wells are pushed along from well to well (Fig 1).*

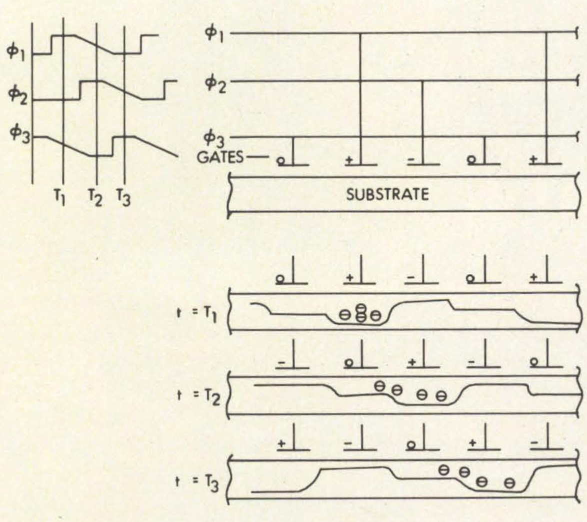


Fig 1 Shift control in a linear array of closely spaced MOS capacitors. Three-phase voltage (upper left) applied to series of cells (upper right) causes accumulated charge to move from cell to cell (lower right)

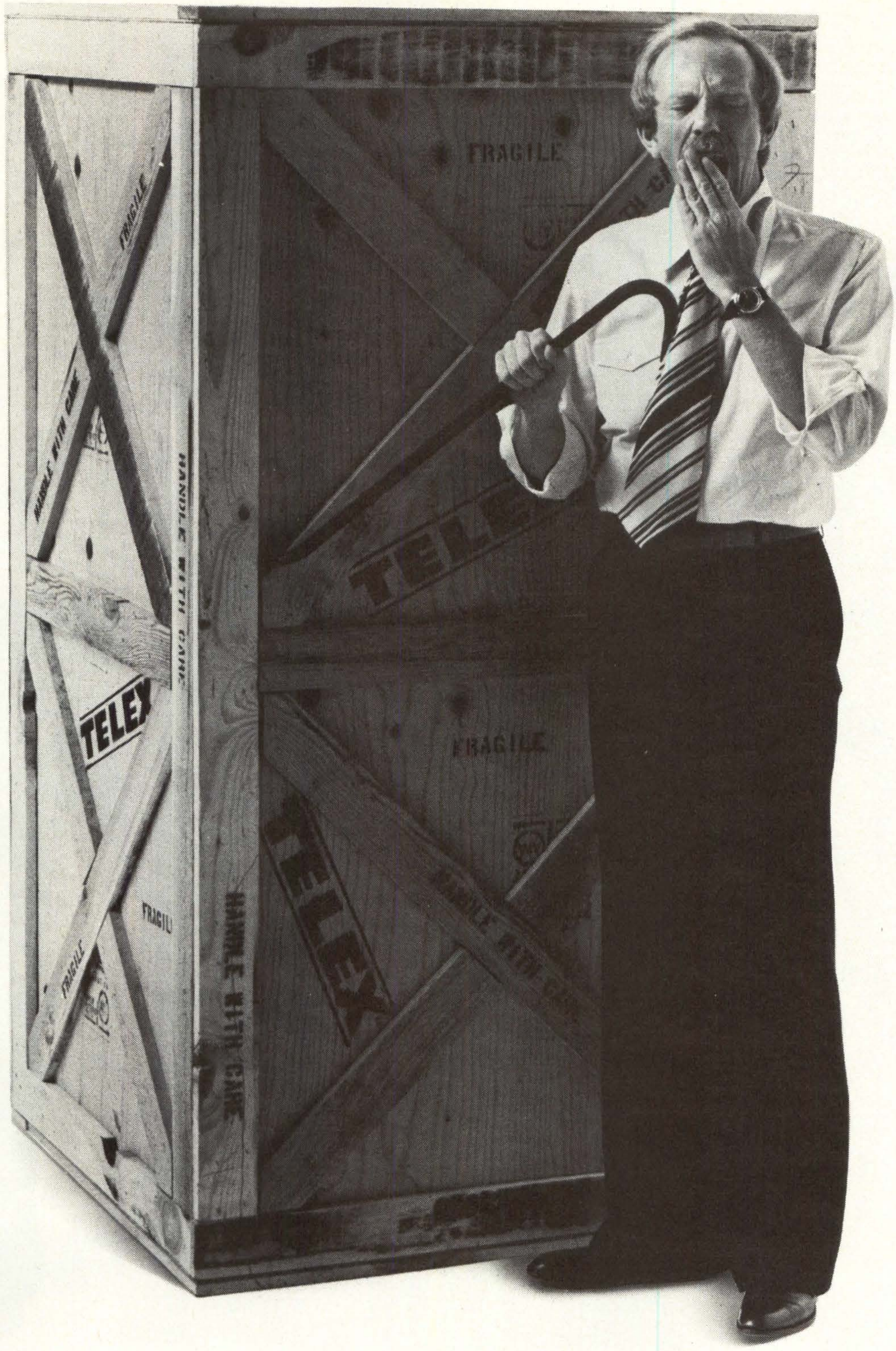
For a digital memory, the potential wells are either uncharged or fully charged to represent 0 and 1. To implement an analog memory, the charge is varied linearly in proportion to the sampled input voltage. Thus, analog delay lines as well as digital memories are implementable with CCD technology. Furthermore, as will be detailed in part 3 of this series of columns, analog CCD shift registers can be integrated on the same chip with other electronics to build image sensing arrays and other complex integrated devices.

Related in function, but differing in principle of operation, are bucket-brigade devices (BBDS). The essential difference in performance between CCDS and BBDS is that CCDS are faster and transfer virtually all electrons from cell to cell, while BBDS may lose a small fraction of the number of electrons present, typically 0.1%.

BBDS transfer stored charges from one physical capacitor to another by opening and closing a sequence of field-effect transistor (FET) switches which separate the capacitors (Fig 2). The input to the BBD is an n-channel MOS transistor switch. When energized by clock ϕ_1, it connects the analog input signal to input capacitor C_s. This charge is then transferred from C_s to the first stage capacitor by clock ϕ_2, which energizes the transistor switch between C_s and C_1. Clock ϕ_2 also provides a positive bias to C_1, thus "pulling" electrons away from C_s. Similarly, clock ϕ_2 then transfers the charge sample from C_1 to C_2, etc. Thus two capacitor stages are required for each charge sample and the samples are passed on clock ϕ_1 from odd to even stages, and on ϕ_2 from even to odd.

In practice, not quite all of the charge is transferred in such devices and this is often the factor which limits the signal-to-noise (S/N) ratio. Because of this, in practical applications typical S/N ratios are between 40 and 50 dB (ie, between 7- and 8-bit accuracy) even though the BBDS may be rated closer to 70 dB (12 bits). It now appears that CCD technology will largely replace BBDS because of an approximately 20-dB improvement in S/N ratio over BBD as well as simpler, more compact, and therefore less expensive structures. Part 3 of this series of columns will

*H. R. Crouch, J. B. Cornett, Jr, and R. S. Eward, "CCDs in Memory Systems Move Into Sight," *Computer Design*, Sept 1976, pp 75-80



Announcing another new 6250 bpi tape transport...

For minis!

Engineering breakthroughs enable Telex to bring big computer storage and reliability to OEMs at a fraction of the size and cost.

The long-awaited 6250 bit-per-inch (bpi) tape drive for minicomputers is here.

The Telex Model 6250.

It offers minicomputer users nearly four times the tape capacity of the previous 1600 bpi drives. Yet it takes up only one-fourth the space and costs only about half as much as the worldwide accepted, big box 6250 bpi units Telex has supplied to IBM users for years.

The four-to-one size reduction wasn't easy.

It took three years and a whole new standard of design to pack all that technology in a 19-inch frame. Parts innovations. Creative placement of needed elements. New materials. All have led to a remarkable achievement in simplicity and reliability.

The machine meets all the stringent requirements of true high density, 0.3-inch inter-record gap recording in both read and write operations.

In addition, the drive:

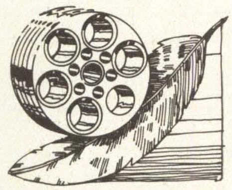
- Handles all three standard data formats—NRZI, PE and the new GCR.

- Runs reliably at speeds to 125 inches per second (models are also available at 45, 75 and 100 ips).
- Transfers data at the high speed of 781 kB per second (so off-loading can be done at nearly disk speeds).

- Rewinds a full 2400-foot tape reel in less than a minute. (That's 500 inches per second!)
- Reduces the complexity and cost of field maintenance (all work is done from the front).

Remarkable new capstan weighs only 1.9 grams.

To feel this Supr-Lite™ capstan is to believe its engineering achievement.



Not only does its lack of weight reduce inertia, it lets us use a smaller motor. Heat is reduced. Cooling blowers and hoses are eliminated.

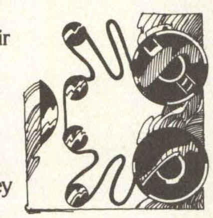
Capstan walls are only 1/1000-inch thick, yet its unique manufacturing process* assures strength, absolute roundness (and users a more consistent data rate).

Telex tape path gets you up to speed in a hurry.

Perhaps the most dramatic example of how Telex miniaturized the 6250 is its tape path*. The path is very compact, yet it retains four vacuum columns (just like big brother).

It brings new efficiencies in tape dynamics and reduces the length of tape required between head and primary vacuum columns.

Combined with our new capstan, friction and mass are cut down so much that the unit runs tape full speed forward to full speed reverse in a mere 0.13 inches (a new record).



Special vacuum buffers and fixed air bearings gently handle tape at the high program rates possible with short inter-record gap operation. They eliminate long spans of unsupported tape, thus avoiding harmful tape oscillations that can restrict programming.

And we're so confident of tape servo reliability that we covered up the tape path with the operator's panel (further reducing space requirements).

New controller/formatter handles up to eight drives.

It includes the same proven logic design as our big controller, only miniaturized to fit a 10 ½-inch-high, rack-mounted box. And it's flexible enough to intermix all four tape speeds and all three densities—800, 1600 and 6250 bpi—in the same subsystem.

A built-in microprocessor handles extensive diagnostic routines.

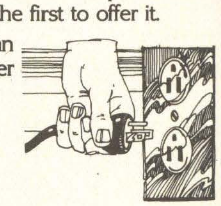
When maintenance is required—on either controller or drive—the machine helps the technician quickly isolate faults down to board level for simple replacement. Given on-hand parts, a disabled machine should take less than an hour to fix. And all maintenance is done from the front.

Plug it in and go, it's that simple.

A common wall socket is all that's needed. And no special air conditioning. You can even operate it from a truck.

Design innovations with a goal of simplicity have enabled Telex to bring OEM's this remarkable new tape transport and controller. Large minicomputer users need this 6250 bpi mass storage capacity. Models are available now in dual density 800/1600 bpi. Full 1600/6250 bpi units will ship in the first quarter of 1978. Be the first to offer it.

Write or call Mr. Dan O'Neill, Telex Computer Products, Inc., 6422 E. 41st Street, Tulsa, Oklahoma 74135. Telephone: (918) 627-1111.



* patent pending

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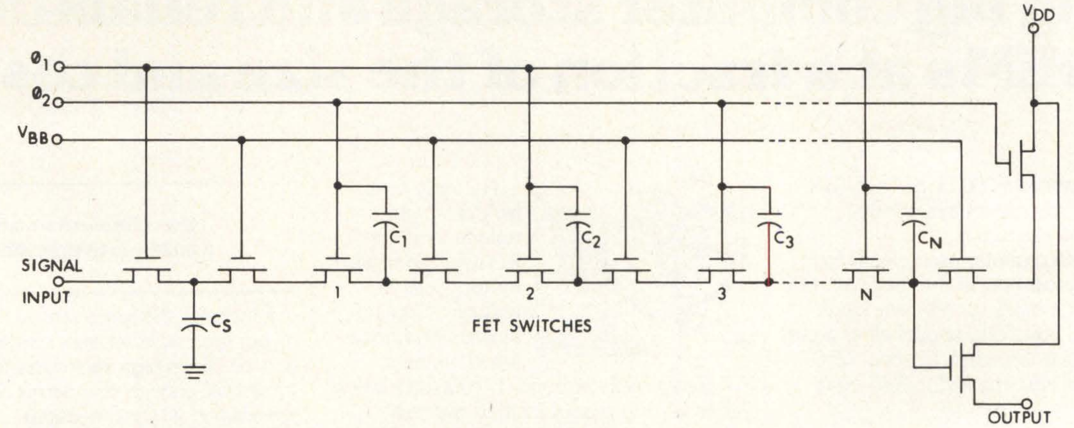

Fig 2 Typical BBD structure. Input signals charge C_S during ϕ_1, after which ϕ_2 clock transfers charge to C_1 by energizing FET switch 1 and "pulling up" C_1 to attract minority carriers away from C_S. Next, ϕ_1 clock transfers this charge to C_2. This continues until the charge reaches final storage cell C_N which controls the output switch and is discharged on ϕ_2 through V_{DD}

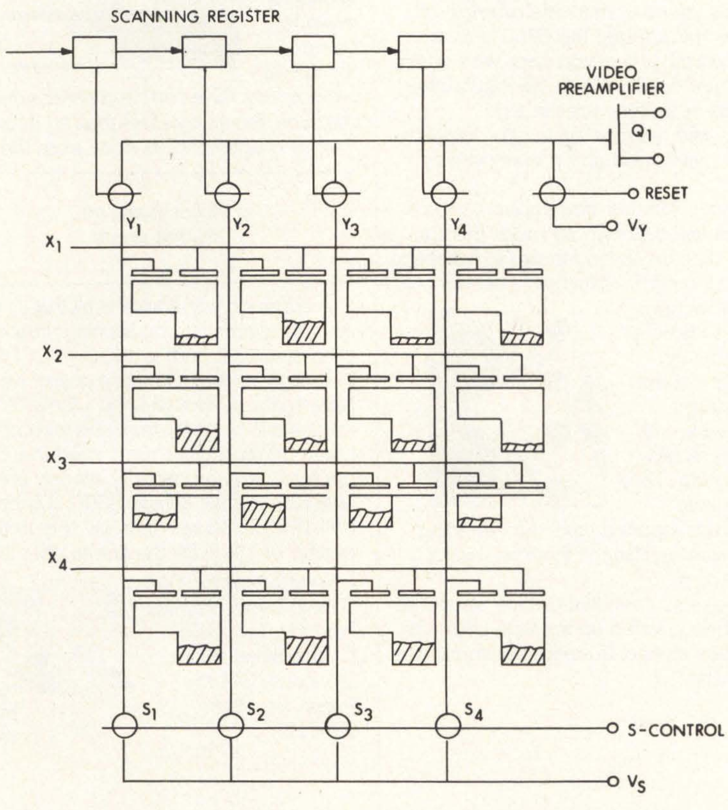

Fig 3 Example of 4 x 4 CID imaging array. Each cell consists of two capacitors, one attached to row control line (X), other to column control (S). Initially, all charges are stored under row electrodes. Readout is accomplished by precharging column electrodes to V_S, and then removing row voltage. As shown in X_3 row, charges then transfer to column electrodes. Column voltages can then be sequentially connected through selection switches Y_1 through Y_4 to video preamplifier Q_1

discuss how BBD delay lines, nevertheless, have already found widespread usage in analog (especially acoustic) processing.

A third basic charge transfer mechanism is charge injection which has been applied to image sensing devices. In charge-injection devices (CIDS), the charge is stored in an X-Y addressable array of potential wells. For image arrays, the charge for each of the cells is generated by an associated photodiode. In early CIDS, readout of the array was accomplished by addressing a single cell and injecting the stored charge into the substrate. The resulting displacement current was detected and amplified to create an output voltage. Thus, the "detection" or readout mechanism was directly achieved by the injection process which simultaneously cleared each cell (ie, destructive readout).

(*Continued on p* 152)

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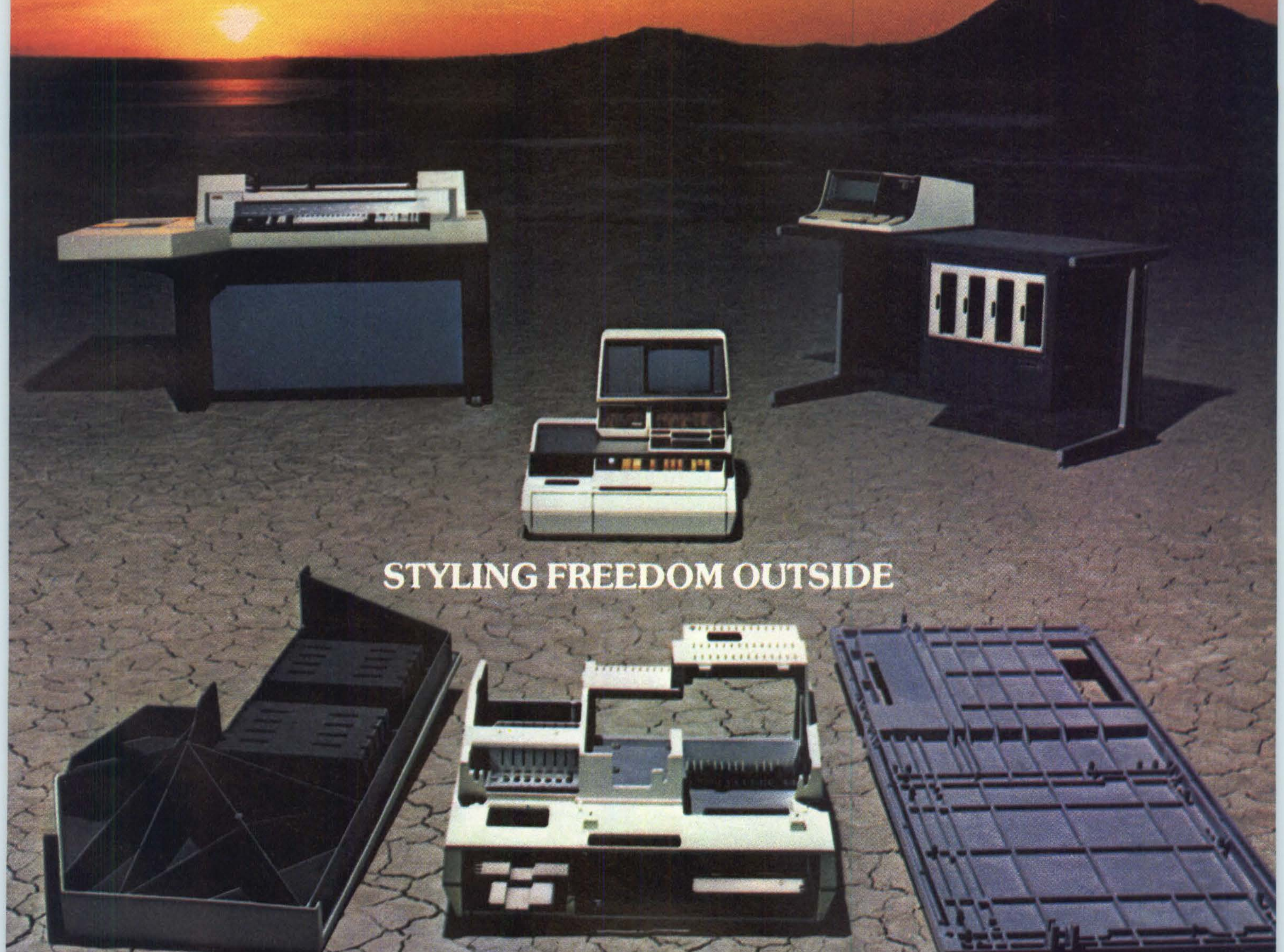

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WHAT THE WORLD IS COMING TO: GE ENGINEERING STRUCTURAL FOAM
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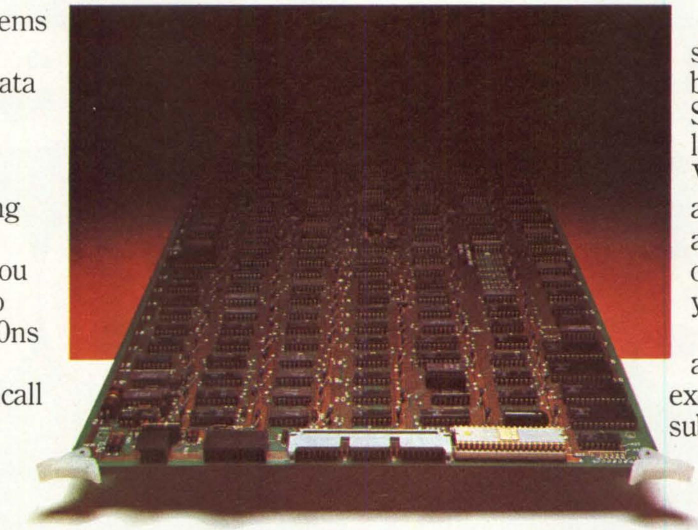
GENERAL ELECTRIC

More recently, this technology has been advanced by the General Electric Research and Development Laboratories by separating the functions of detection and injection, making nondestructive readout possible. Fig 3 shows the basic structure of a 4 x 4 array of storage cells, and also shows an example of signal-charge stored beneath each capacitor. Initially, all charges are stored beneath the "row" capacitor of each storage cell. To read the cells, the column capacitors are first "cleared" by applying the reference voltage, V_s, to the column lines, which are then allowed to float. Voltage is then removed from the capacitors in the row selected for readout (X_3), causing signal charges at each cell in that row to transfer from the potential well beneath the row electrode to the well beneath the column electrode. The resulting change in voltage caused on each of the floating column lines is then sequentially detected and amplified.

Following this line readout operation, all charges on the selected line can be injected (cleared) simultaneously by driving all column voltages to zero. Alternatively, for nondestructive readout the injection operation is not performed. Instead the row voltage is simply reapplied, thus attracting the signal charges back to the row capacitor. Using this interesting technology, General Electric has developed a 244 x 248 element imaging array and has applied it in a low cost camera system (to be described in part 3 of this series).

These three different charge-transfer technologies—CCD, BBD, and CID—make possible an extremely wide range of devices that are now finding applications throughout the electronics industry. History, current status, and applications of the devices will be discussed in the next two columns.

Sperry Univac's new mainframe-on-a-board: What you do with it is your business.



Whether your systems business is scientific, instrument control, or data communications, know this:

Our new V77-200 delivers more computing power than any other computer-on-a-board you can buy. Handling up to 32K/16-bit words of 660ns MOS memory.

Reason enough to call it the world's first mainframe-on-a-board. But there's more.

Because our new V77-200 comes loaded with "big machine" features. Like 8 programmable registers with byte, word and double word manipulation. Up to 32-bits of arithmetic precision. A powerful set of 187 instructions. Hardware multiply/divide. Direct memory access. Programed I/O. Multi-device automatic program loaders. A real-time clock. And a teletype/CRT controller. All standard. And all on a single 10.8″ x 17″ board.

There's even Virtual Console Logic that eliminates the need for a programmer's console by allowing you to control the V77-200 from a teletype or CRT keyboard.

You get "big machine" performance, too. Example: a microinstruction cycle time of 165ns that allows multiplication functions to be handled in just 4.9 microseconds—divide in just 8.

Plus your choice of OEM-tailored options. Like a variety of connector planes and general purpose interface boards for custom I/O designs. Three different 660ns memory boards (in 8K, 16K, and 32K-word modules). An operator's console. Power-fail detect and data save. Memory parity. Hardware for up to 64 priority vectored interrupts. An integral or modular power supply. And a system chassis. All the "unbundled" pieces you need for quick and easy system integrations.

The new V77-200 also saves you time and money by allowing you to use Sperry Univac's well-established floppy or disk-based VORTEX real-time operating system. In effect, allowing you to concentrate on the development of your application software.

And giving you access to Sperry Univac's extensive library of software subsystems, language processors, and system utilities.

Best of all, the world's first mainframe-on-a-board has a base price of just $1200. Plus a discount plan designed to give even modest-volume OEM buyers a big break. And you can take delivery in a matter of days—not months.

No matter how you configure it, the new V77-200 is the most economical Sperry Univac yet. Delivering the kind of price/performance value that just makes good sense. No matter what business your systems are in.

For more information on the world's first mainframe-on-a-board, please contact: Sperry Univac Mini-Computer Operations, 2722 Michelson Drive, P.O. Box C-19504, Irvine, California 92713, Telephone (714) 833-2400.

SPERRY UNIVAC

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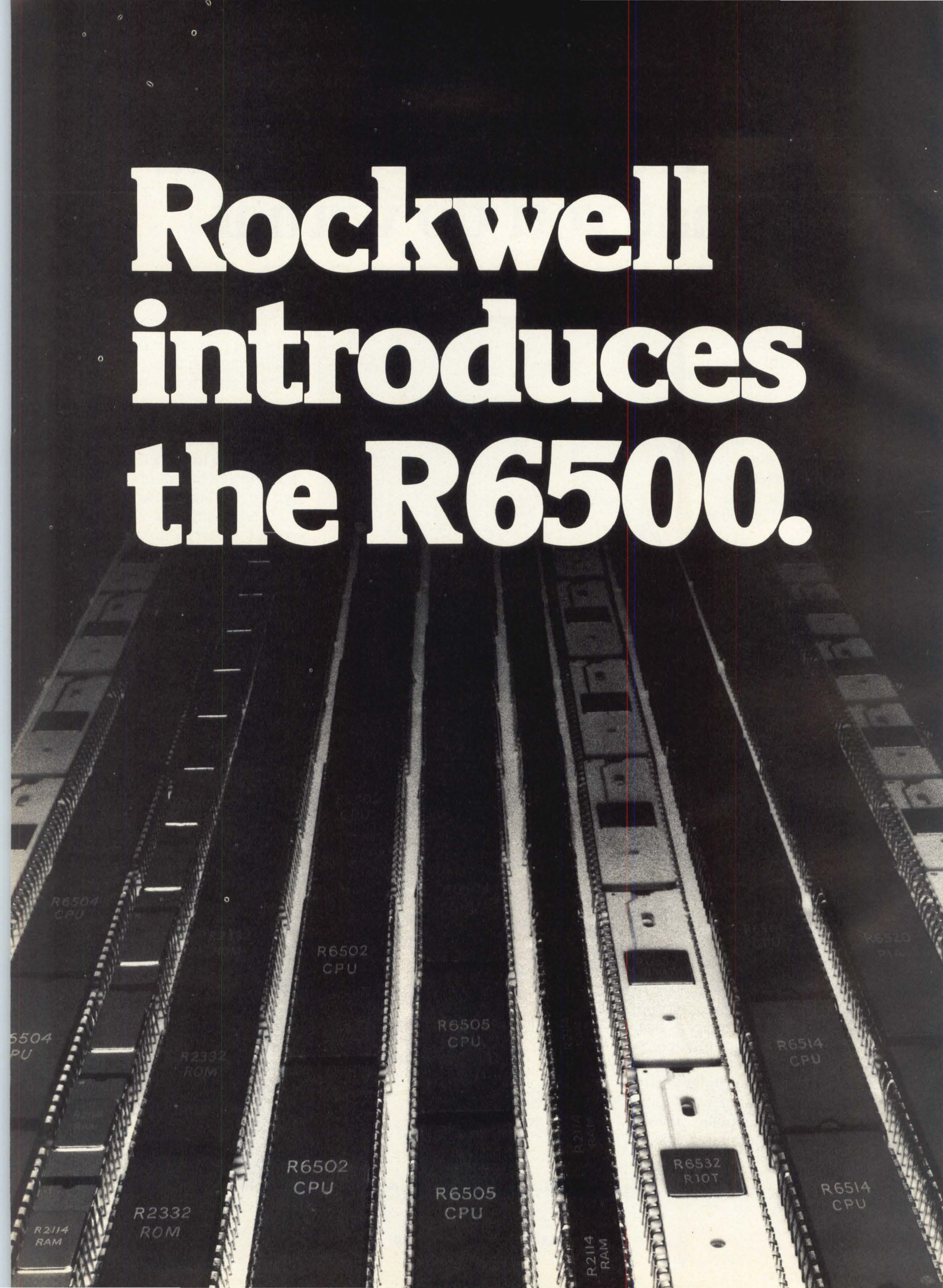
CIRCLE 71 ON INQUIRY CARD


Rockwell introduces the R6500.
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R6502 CPU
R6505 CPU
R2332 ROM
R6514 CPU
R6502 CPU
R6532 RIOT
R6505 CPU
R6514 CPU
R2332 ROM
R2114 RAM
R2114 RAM

R6500: the third generation microprocessor system

Now you can move up to the proven 2 MHz performance of an NMOS 8-bit microprocessor, the R6500 from Rockwell.

Third-generation R6500 architecture and instructions with 13 powerful addressing modes make it easier for you to design more functions in, more cost out. And the R6500 is design-compatible with systems you may now be using.

R6500 economics are on your side

Smaller R6500 chips and single 5V power supply keep costs down as performance goes up. To get the right fit, choose from 10 software-compatible CPUs, eight versatile I/Os, ROMs, RAMs, and memory-I/O-timer circuits.

R6500 CPU Options

	40-Pin DIP		28-Pin DIP				
	R6502	R6512	R6503 R6513	R6504 R6514	R6505 R6515	R6506	R6507
Memory Address Space	65K	65K	4K	8K	4K	4K	8K
Interrupts — Maskable — Non-Maskable	Yes Yes	Yes Yes	Yes Yes	Yes No	Yes No	Yes No	No No
SYNC — Output indicates op code fetch cycle	Yes	Yes	No	No	No	No	No
RDY — Single step and slow memory synchronization	Yes	Yes	No	No	Yes	No	Yes
$\emptyset_1$ Clock Output	Yes	Yes	No	No	No	Yes	No
DBE — Extended Data Bus Hold Time	No	Yes	No	No	No	No	No

I/O Devices

PART #	NOMENCLATURE	DESCRIPTION
R6520	Peripheral Interface Adapter	2, 8-bit bidirectional I/O ports; 4 peripheral control/interrupt lines.
R6522	Versatile Interface Adapter	PIA functions plus 2, 16-bit programmable interval timers/counters.
R6530	ROM-RAM-I/O-Timer	1024 x 8 ROM, 64 x 8 static RAM; 2, 8-bit bidirectional data I/O ports; 2 programmable data direction registers; 8-bit interval timer.
R6532	RAM-I/O-Timer	128 x 8 RAM; 2, 8-bit bidirectional data ports; 2 programmable data direction registers; 8-bit interval timer.

PLUS ROMS, RAMS...AND MORE ON THE WAY

Rockwell adds solid development support

For fast and efficient system design, Rockwell offers SYSTEM-65 — one of the smartest and lowest-cost, disk-operating, complete development systems available. It's equipped with two mini-floppies, resident two-pass assembler, text editor and monitor/debug package.

KIM-1, TIM, timeshare, complete documentation, plus extensive applications engineering are also available.

Rockwell is delivering in volume now

R6500 circuits are already being produced in quantity with Rockwell's N-channel, silicon-gate, depletion load process.

R6500 devices and SYSTEM 65 development microcomputers are now available at your local Hamilton-Avnet or Schweber distributor.

And new chips are in design. The first, a fully static 32K ROM, is now in production.

For your R6500 brochure write: D-727-A, Marketing Services, Microelectronic Devices, Rockwell International, P.O. Box 3669, Anaheim, CA 92803, U.S.A. or phone (714) 632-3729.

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...where science gets down to business

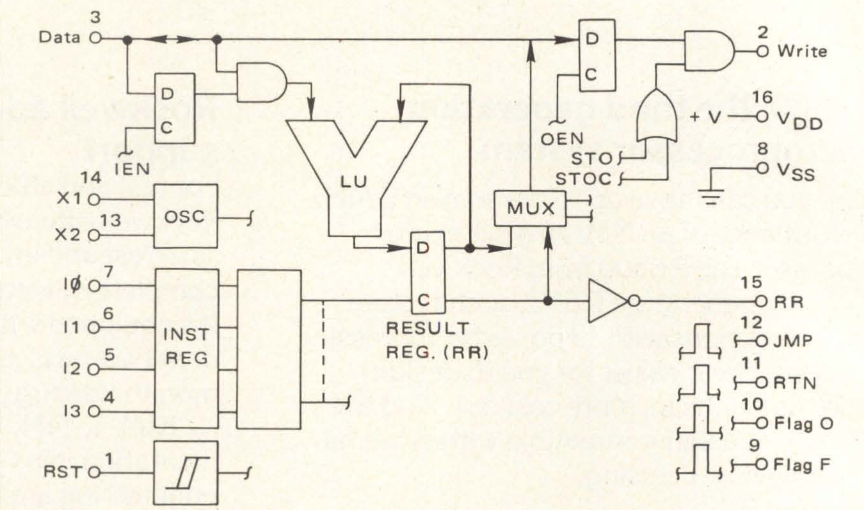
Universal Controller Interfaces Printer to Mini/Microcomputers

Control of and interface to any standard impact, thermal, or electrostatic 5 x 7 dot-matrix printer having a print speed up to 200 char/s is now possible with the model CY 480 universal printer controller. The controller interfaces between a printer and any microcomputer or minicomputer system through standard 8-bit ports, accepts either RS-232-C (serial) or parallel ASCII from the host system data channel, and has ready lines for full asynchronous communications with handshaking.

Features of the controller, which is a product of Cybernetic Micro Systems, 2460 Embarcadero Way, Palo Alto, CA 94303, include a dot-matrix character generator and optional foreign language character generator, full 96-char ASCII font, and 48-char buffer expandable to 96 characters. In addition, the low power device provides a forward or backward printing command at 8, 10, or 12 char/in density, and feeds paper in an up or down direction, handles 2-color ribbons, and allows variable horizontal and vertical spacing in graphics mode. Moreover, images can be displayed in true as well as mirrored form using the forward/backward and up/down print capability in graphics mode. The controller comes in a 40-pin DIP, and operates from a single 5-V supply.

Circle 360 on Inquiry Card

Control Unit Offers Alternative to Combinatorial Logic



Instructions to Motorola MC14500B industrial control unit (ICU) enter via pins 4 through 7, while 1-bit data move into ICU via data bus, route through logical unit, and leave via multiplexer

The MC14500B industrial control unit (ICU), a single-bit CMOS processor for systems requiring decisions based on successive 1-bit data, when used in a system with program counter forms a stored program that replaces combinatorial logic. A repertoire of 16 instructions, 11 of which perform control functions within or external to the ICU, enable the device to perform several logic operations on data occurring on a 1-bit bidirectional bus and on data in a 1-bit accumulating result register. By operating on inputs and outputs one at a time and by using a looping (rather than jumping) program flow, an ICU-based system can control decision making electronic and electromechanical devices in microprogram-control sequencers; serial bit-stream communications; telephone dialing systems; and peripherals such as printers, keyboards, discs, and controllers.

Logical operations executed by the device include AND, OR, exclusive-OR, complement, complement OR, and complement AND. Data can be routed unchanged through the device as well. All logical operations occur in a logic unit (LU) on the ICU (see Figure). Operands enter the LU from the data bus and from the result register (RR) which also holds the output from the LU after a logical operation completes. True and complement outputs of the RR are routed to a multiplexer which, under program control, directs one of the two RR outputs to the data bus. Besides its logic operation capability, the ICU can generate a write level, an O flag, an F flag, a jump indication, and a return indication.

The ICU, produced by Motorola Semiconductor Products Inc, 3501 Ed Bluestein Blvd, Austin, TX 78721, contains its own oscillator circuit. It operates from dc to mHz with V_{DD} set at 5 V and executes one instruction per clock cycle. The four instruction inputs to the device are TTL-compatible, while its output lines can drive one low power Schottky load or two low power TTL loads. Other features include a typical noise immunity of 45% over a 3-Vdc to 18-Vdc V_{DD} range and a low current drain—quiescent current drain is typically 5.0 μAdc with V_{DD} = 5 V.

Circle 361 on Inquiry Card

CMOS A-D Converter Provides BCD Output

Latched, non-multiplexed, parallel BCD from the 8750 3½-digit CMOS analog-to-digital converter enables application in LCDs and gas discharge displays. Moreover, its typical power dissipation of only 20 mW, which results in a 2-mA drain on its ±5-V supply, permits the monolithic converter to serve also for battery-powered operation. It offers monotonic operation—it uses no missing codes—as well as high linearity, noise immunity, and 3½-digit resolution with ±0.025% error.

During A-D conversion (see Figure), the analog input current to the converter, I_{IN}, flows into an integrator comprising resistor R_{IN} and capacitor C_{INT}, at the input of an operational amplifier. Concurrently, a reference current, I_{REF}, which is opposite in

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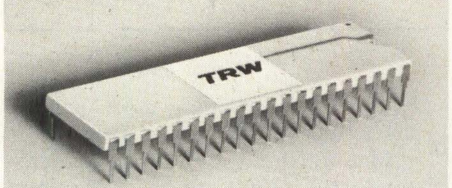
8 x 8 bits



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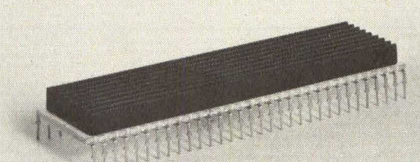
MPY-12AJ
150 ns
12 x 12 bits



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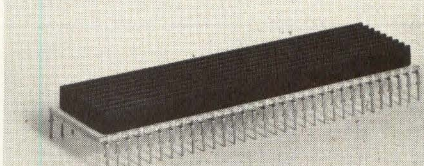
MPY-16AJ
160 ns
16 x 16 bits



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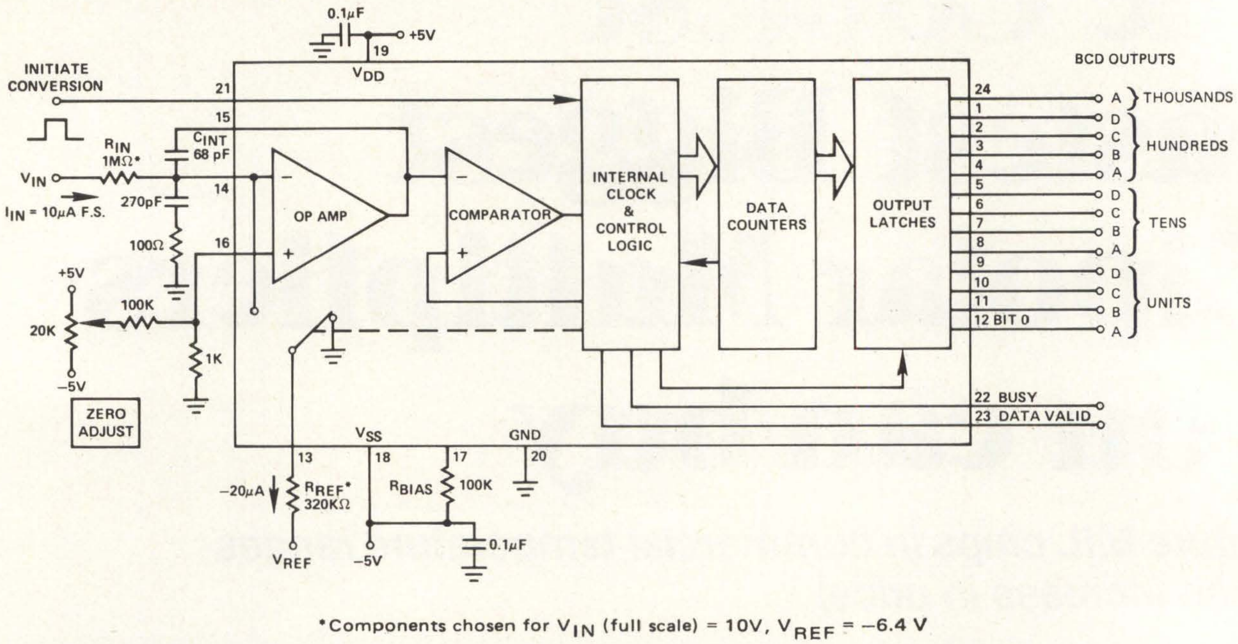


Teledyne 8750 conversion technique switches number of current pulses needed to zero analog current at input of op amp and thus, by counting number of pulses used, determines digital equivalent of incoming analog

polarity to I_{IN}, is switched into the integrator by converter internal clock and control logic and integrated with I_{IN}. I_{REF} is switched for one clock period into the integrator just frequently enough to maintain the input to the op amp at zero.

The total number of I_{REF} pulses needed to maintain the op amp input at zero is counted by one of two converter counters, a data counter, and the resulting BCD count for a given analog input is read into the output latches. After the conversion process is started by the initiate conversion input, the second of the two counters, a clock counter, counts a prescribed number of pulses defining the conversion time of the device and, then, initiates an end-of-conversion sequence in the converter.

A positive signal generated internal to the converter strobes the initiate conversion input to start an A-D conversion. At this time, the busy line latches high, the counters are reset, and the integrator is discharged. A-D conversion begins immediately afterwards and continues until the clock counter initiates the end-of-conversion sequence or the data counter overflows. During the end-of-conversion sequence, the valid output falls to a low for approximately 10 μs, during which time the latched BCD output changes to reflect the output resulting from the conversion just performed.

In normal operation, the initiate conversion input is a 500-ns (typ) pulse which enables the converter to function. By applying a constant high on this input the converter can operate in a freerunning mode producing a typical 100 conversions/s.

Manufactured by Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94043, the converter affords a maximum differential nonlinearity of 0.025% with temperature drift of typically ±2.5 ppm/°C, a gain variance of ±2% of normal and a gain temperature drift of ±25 ppm/°C. Furthermore, the device provides a zero offset of typically ±10 mV with $I_{IN} = 0$, a zero temperature drift of ±30 μV/°C, and a conversion time of 10 ms. It is available in plastic DIP for operation over the 0 to 70°C temperature range and in ceramic DIP for operation over the −40 to 85°C range.

Circle 362 on Inquiry Card

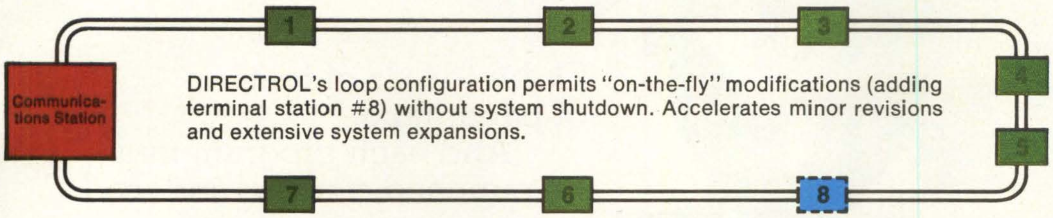
Companding DAC Meets Bell μ-255 Law

Companding digital-to-analog conversion designed for telecommunication applications is now also available with the Am6072 DAC produced by Advanced Micro Devices Inc, 901 Thompson Place, Sunnyvale, CA 94086. A pin-for-pin replacement for the Precision Monolithics, Inc DAC-86, the device complies with the Bell System u-255 companding law by using 15 linear chords, each defined by a sign bit and three chord select input bits, and, within each chord, 16 uniformly spaced linear steps, each defined by four step select bits. Thus a 72-dB dynamic range, equivalent to that of a 12-bit linear converter, is achieved using only eight bits. The DAC is available in commercial and military temperature range units.

Circle 363 on Inquiry Card

New DIRECTROL™ Multiplexer. Signaling new directions for industrial control.

Cutler-Hammer's new DIRECTROL . . . finally, here's a multiplexer that's practical for industrial control application. DIRECTROL achieves startling advantages in project simplification, system productivity and plant versatility.

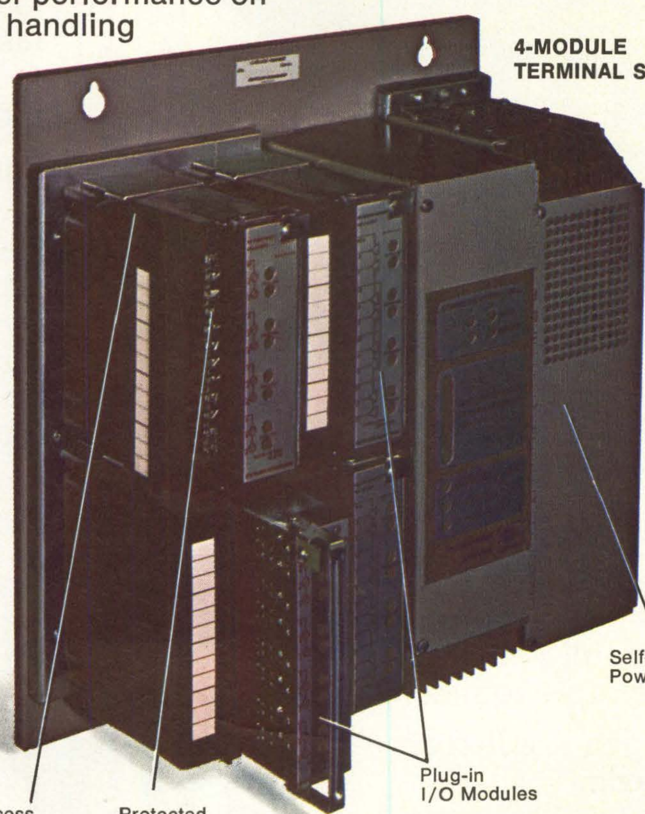


Project simplification. DIRECTROL is designed and applied in a conventional control manner. But unlike the conventional, it substantially reduces wiring costs and project complexity—easily adapting to unanticipated requirements. For the first time, DIRECTROL offers control multiplexing in easy-to-apply, easy-to-order, easy-to-install modules.

System productivity. DIRECTROL's innovative approach provides high-yield features like monitoring of multiplexer performance on every signal scan, high security data handling routines, self-diagnostic/self-correcting characteristics, integral high noise immunity and multiple redundancy options to name only a few. Plus the unique ability to add new stations "on the fly" without affecting system operation.

Plant versatility. DIRECTROL's 4,096 signal capacity and 5,000 foot distance between stations combine with "stand-alone" independence or computer compatibility to add dramatic equipment selection flexibility for future needs.

Why not set a new course for your industrial control requirements? Write Milwaukee, Wisconsin 53201 for descriptive brochure.



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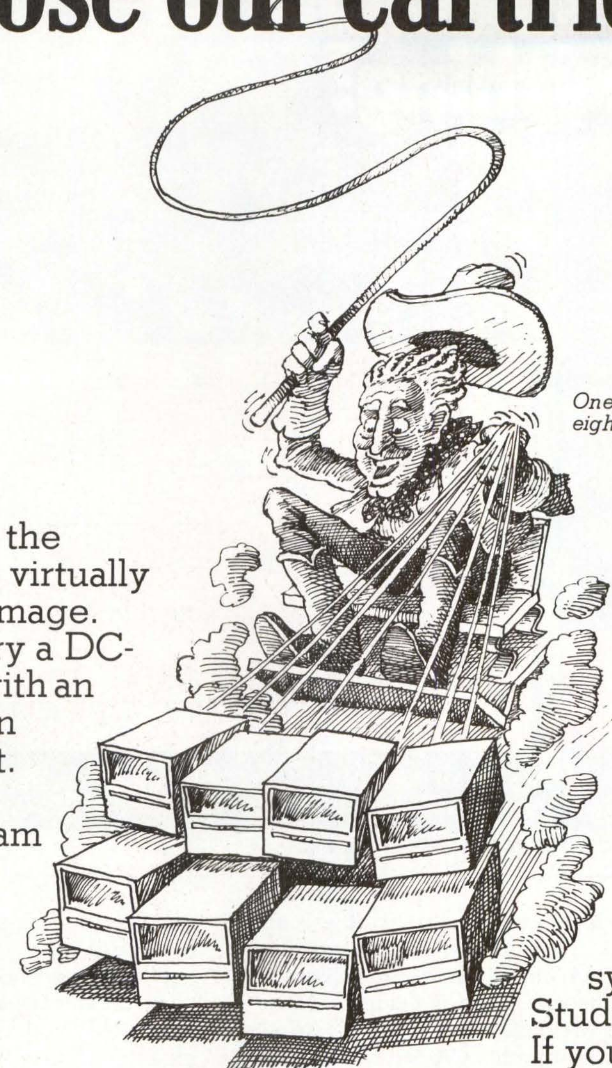
to choose our cartridge drive?



One formatter can control eight drives at once.

protected inside the cartridges, so it's virtually impossible to damage.

You can carry a DC-100A cartridge with an entire program in your shirt pocket.

Even if you drop it, the program will survive unscathed.

Remember that the next time you drop a stack of cards.

Don't take our word for it. Ask your computer.

If you'll send us the coupon, we'll send you the specifications for all three of our drive systems.

Ask your computer to compare them with any other type of drive system.

We'll bet your computer will prefer ours.

Maybe it'll choose our famous DCD-3 drive. It's people-proof, jam-proof and wear-resistant.

Or maybe your computer will decide upon our DCS-3000 series, an ANSI-formatted system that allows one formatter to control up to eight drives.

The DCS-3000 is extremely easy to integrate into your system. Only one cable to the user's logic is required.

But if you require compact size, your computer will probably choose our unique DCD-1. It offers many of the features of our bigger systems, yet it will fit inside a five-inch cube.

The cartridge alone measures just 2.4 x 3.2 x .5 inches.

See for yourself.

Send us the coupon. There's much more we can tell you about our drive systems.

Study the information carefully.

If your computer isn't smart enough to choose our drive systems, we'll bet you will be.

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CIRCLE 75 ON INQUIRY CARD

AROUND THE IC LOOP

Multiplier Offers 100 ns/ 1 W Speed/Power Product

Multiplication of two 8-bit signed 2's complement, unsigned uncomplemented, or a combination of both operands is possible with the 57558/ 67558 8 x 8 combinatorial multiplier which accepts rounded operands and provides a 16-bit product and an inverted most significant bit output. Having the most significant bit in both true and complement form enables signed product expansion. In addition, the outputs of the device are 3-state, thus allowing the multiplier to serve in pipelined systems.

The device, which multiplies at 100 ns while dissipating only 1 W, serves such digital signal processing functions as fast Fourier transform and speech and signal processing. Other applications include calculations in computer-aided tomography (brain and body scanning) and fast floating-point processors.

Multiplier specifications include a minimum high level and maximum low level input voltage of 2 and 0.8 V, respectively, a maximum low and high level output current of −2 and 8 mA, respectively, and a maximum −10-mA output short circuit current. The device, which is made by Monolithic Memories Inc, 1165 E Arques Ave, Sunnyvale, CA 94086 and second sourced by ITT Semiconductors, operates over a temperature range of 0 to 70°C with a supply voltage in the range of 4.5 to 5.5 V.
Circle 364 on Inquiry Card

Low Power EPROM Operates From Single Supply

Fast access time, rapid and simple programming, and single 5-V supply requirement are key features of the 2758 1k x 8 UV-erasable programmable read-only memory. Low power dissipation derives from the 525-mW maximum active power requirement falling 75% to a low 132 mW when memory is placed in a standby state. Unaffected by the standby state is the memory's fast 450-ns maximum access time. Programming speed complements the operating speed: 1024 bytes can be programmed in less than a minute, claimed to be twice as fast as for other EPROMS; a single byte can be programmed in 50 ms, 10 bytes in 0.5/s.

Non-dependence on multiple supplies permits it to serve in systems structured around single-supply, single-chip microcomputers. Also, the memory can operate off an MOS or TTL supply.

The EPROM contains ten address lines, eight data outputs, and chip select ($\overline{CS}$), power down/program (PD/PGM), and select reference input level (A_R) inputs. All are TTL-compatible during both read and program operations. Also, the output lines are 3-state, thus allowing OR-ties with the output lines of other EPROMS. The high impedance state emerges when the $\overline{CS}$ input deselects the memory.

During read, data are available 450 ns after the address on the address line stabilizes and $\overline{CS}$ is in the low (enable) state. When $\overline{CS}$ goes high, disabling the EPROM, a logic high level on PD/PGM selects the power down mode. It is possible for the $\overline{CS}$ and PD/PGM lines to be driven by the same level. Finally, the A_R input contains low voltage level for reference during all memory operations.

This EPROM is made by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 and is compatible with other company EPROMS and masked ROMS.
Circle 365 on Inquiry Card

Now you can expect even more from Lear Siegler.

Printers.

Introducing Lear Siegler's new 200 series printer.

Our revolutionary Ballistic™ printer head design makes us unique among printer manufacturers. Unlike other matrix printers, there are no solenoids, and thus no moving cores attached to the wires. The Ballistic™ head uses small "swatters" that ballistically propel the matrix wires. This simplified system has eliminated clogging with inks, dust and paper fibers – so the Ballistic™ head requires no preventive maintenance. If you have a requirement that calls for continuous printing, and the cost of service is important to you, our 200 series printers will give you the lowest cost of ownership.

Lear Siegler's new 200 series printers are designed to have at least 10 times better reliability than presently existing printers. Remarkably, the Ballistic™ heads are capable of printing up to 1 billion characters before needing a replacement. And with a fully-buffered input for bi-directional printing, you can print an original and 5 copies at 180 cps. With no head adjustment.

Compare this with the up-to-now-best printer's head, which needs constant adjustment, and lasts only for about 100 million characters. If you were lucky. And many times you weren't.

So if you're tired of depending on luck, and need non-stop output, you owe it to yourself to look into our new printers.

You'll like what you see.

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CIRCLE 77 ON INQUIRY CARD

Low Power p/ROM Offers 96% Programmability

Key characteristics of the MB7055/7060 1024 x 8 electrically field programmable read-only memory made by Fujitsu America Inc, 2945 Oakmead Village Ct, Santa Clara, CA 95051 include 150-ns typical access time and 0.044-mW/bit power dissipation. Moreover, inputs and outputs to the device, including a chip enable input which affords typical 60-ns and maximum 150-ns access times, are fully DTL/TTL-compatible. Such features as these make the device an enhanced replacement for such parts as the earlier Intel 2708 and the Fujitsu MB 8518.

Programming the p/ROM, which involves the avalanche induced migration technology, is available through Data I/O and Pro-Log offices. 96% programmability is achieved using special circuitry that permits post-packaging tests for ac, dc, and programming parameters. The devices are available in 24-pin ceramic DIPS.
Circle 366 on Inquiry Card

Design Kit Facilitates Custom IC Design

For the electronic engineer without previous experience in IC design, all necessary information to design linear or digital custom circuits is available in the Mo-K design kit from Interdesign, Inc, 1255 Reamwood Ave, Sunnyvale, CA 94086. An updated and expanded version of the company's Monochip design kit, this package contains an overview of IC design on a 30-minute audio cassette; a 212-page handbook containing sections on component parameters, computer analysis, predesigned functional blocks, IC layout, and chip selection; and several design tools and 20 DIP parts for breadboarding. Included in the $59 kit price are free layout sheets, consultation from the company's IC design group, and monthly application note updates.
Circle 367 on Inquiry Card

Monolithic Voltage Controlled Filter

Specifications for the SSM2040 voltage controlled filter (VCF) include better than 75-dB signal/noise levels, 0.1% distortion levels, and a guaranteed control rejection characteristic over its 10,000:1 sweep range. Elements of the filter include an exponential generator, four 3080-like voltage controlled amplifiers, and four high impedance buffers that offer four flexible tracking filter sections. The VCF can serve in any type of active filter including lowpass, bandpass, highpass, allpass, notch, biquad, and state variable. Other applications include parametric equalizers and tracking filters. The device is offered by Solid State Music, 2102A Walsh Ave, Santa Clara, CA 95050.
Circle 368 on Inquiry Card

Op Amps Feature Low Power Dissipation

Four internally compensated op amps, ULN4136A through ULN4436A, offering such capability as 300-V/mV typical open loop voltage gain, 90-dB typical common mode rejection, 120-dB typical channel separation, and 2-MΩ input resistance, meet or exceed industry standard μA741 amplifier specifications. They can directly replace LM124, LM148, and MC3404 series devices. The amplifiers, which serve in such applications as active filters and multichannel amplifiers, also offer continuous output short circuit protection and come in low power models that dissipate typically 60 mW of power. Total power consumption is 625 mW.

The devices, manufactured by Sprague Electric Co, 555 Marshall St, North Adams, MA 01247, feature monolithic construction to allow very close thermal tracking, 1-mV typical input offset voltage, 30-nA typical input bias current, 0.6-V/μV slew rate, input voltage range of ±14 V typical, and operating temperature range of 0 to 70°C. They are available in 14-lead DIPS conforming to JEDEC outline TO-116 as well as in 88-mil square chips for use in hybrid circuit devices.
Circle 369 on Inquiry Card

Op Amps Feature Lower Offset Voltages

Two op amps introduced by Precision Monolithics Inc, 1500 Space Park Dr, Santa Clara, CA 95050, the OP-08 and OP-12, are improved replacements for the LM108/308-type amplifiers. Both offer three times lower offset voltage (350 μV worst case over −55 to 125°C compared to 900 μV for the part it replaces) and two times lower offset voltage drift (2.5 μV/°C). Each drives a 2-kΩ load. Both devices serve in low power airborne controls and battery-powered applications, as well as 4- to 20-mA industrial control current loops.

A third op amp, the OP-11, is a precision quad device which offers an input offset voltage as low as 500 μV and replaces the LM148/HA4741-type amplifier. Guaranteed matched common mode rejection ratio of 94 dB minimum and offset voltage of 750 μV maximum enables it to serve in instrumentation amplifiers.

Because each amplifier affords symmetrical slew rates in positive- and negative-going directions, it can be used in audio systems as well. Other applications for the amplifiers, each of which offers low noise, low drift, and long term stability, include active filters and those requiring minimum space and low cost.

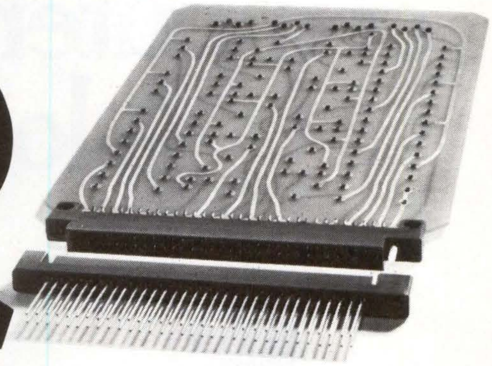
Each op amp is available in both military and commercial versions with each version having a number of models to meet varying operating requirements.
Circle 370 on Inquiry Card

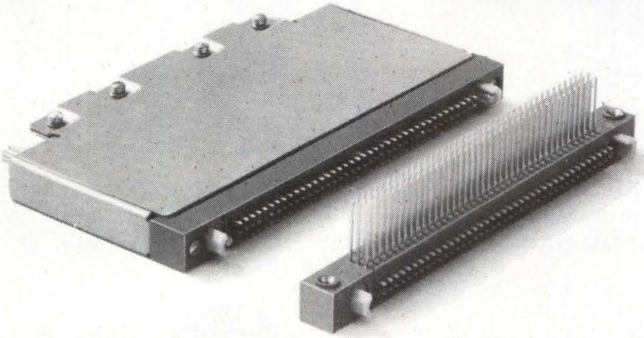
Op Amp Offers High Slew Rate

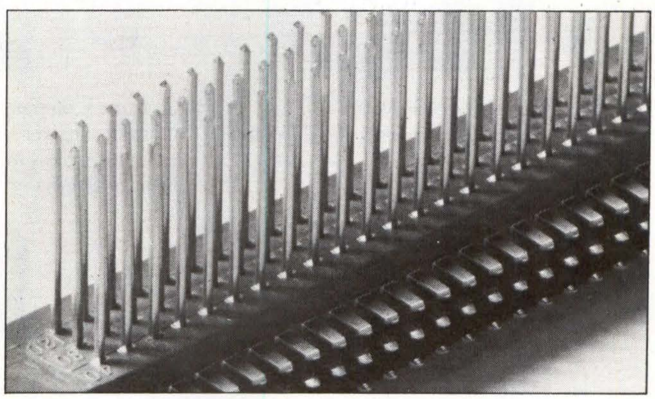
Typical and guaranteed minimum slew rates of 60 and 40 V/μV, respectively, are characteristics of the SE/NE538 op amp which also offers a 2-mV input offset voltage, a 60-mA input bias current, and a 90-dB common mode rejection ratio over the −55 to 125°C temperature range. In addition, the device is internally compensated for gains of five or greater with a gain bandwidth product of 6 MHz and has an improved input structure that makes possible both upgrading of system speed performance and minimizing of errors.

The op amp accepts input signals in the range of ±13 V across a typical input resistance of 6 MΩ, provides a large signal voltage gain of 200 V/mV with a 2-kΩ load resistor and a ±10-V supply, and offers a 100-Ω output resistance and an output voltage swing of ±14 V. A product of Signetics, 811 E Arques Ave, Sunnyvale, CA 94086, the device can be used in digital-to-analog and analog-to-digital applications and in telecommunications and test and medical instrumentation. Because of features such as 2.2-mA typical power supply current and wide bandwidth, the amplifier can replace the LM318 amplifier in applications where required gain is greater than +5 or —4. □
Circle 371 on Inquiry Card

How to get a lot more into a lot less.







First, with 3 rows of contacts on .100 centers, Viking's unique Nordic 2-piece P/C board connectors and I/O I.C. panel plugs get a lot more contacts into a lot less space.

Second, our unusual polarizing system lets you key each mating pair to prevent cross mating with adjacent connectors of the same type. You can stack a series of Nordic connectors next to one another in cramped space and not worry that they might be cross mated.

Our full line includes 64 and 82 contact models as well as the 120. Contacts on I/O connectors are crimp, snap-in, removable, gold plated and use MIL-T- 22520 tools.

Diallyl Phthalate is the insulator in most models. And all connectors are designed to meet conditions of MIL-C-55302.

If you need them right now, our distributors have most models in stock. For details, use the coupon and get our latest catalog.

O.K. Send me:

☐ Your latest catalog with details on the two-piece PC connectors ...and your nearest rep. I have some questions for him.

Name: __________

Position: __________

Company: __________

Address: __________

City: ______ State: ______ Zip: ______

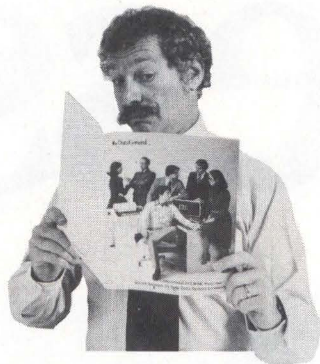
Viking CONNECTORS

Viking Industries, Inc., 21001 Nordhoff Street, Chatsworth, CA 91311

CIRCLE 78 ON INQUIRY CARD

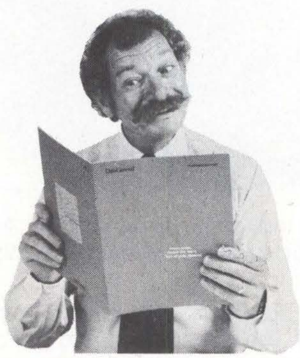
A little knowledge about computers can be expensive. A lot can be free.

1. The inside story on how our full PRODUCT LINE makes the difference to you.
Reader Service # 301



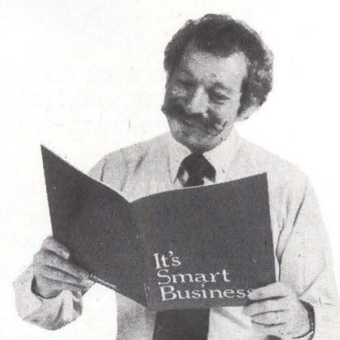
2. How Commercial ECLIPSE Systems answer the diverse demands business makes today on a data system.
Reader Service # 302

3. The secret of having computer power where your business needs it. Our book on CS/40 SMALL BUSINESS SYSTEMS tells.
Reader Service # 303

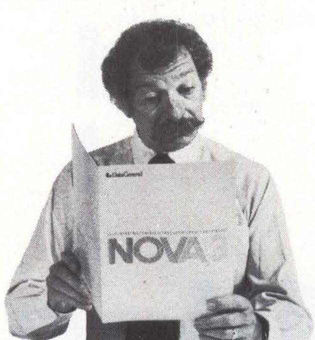


4. Describes seven important SUPPORT SERVICES that get systems up and running, then keep them there.
Reader Service # 304

5. Find out how our Real-Time Disc Operating System SOFTWARE can get you on-line fast, and keep you there.
Reader Service # 305



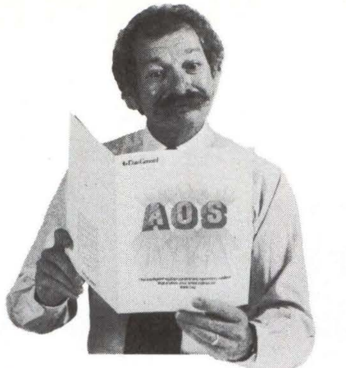
6. IT'S SMART BUSINESS to know how our way of doing business benefits our customers.
Reader Service # 306



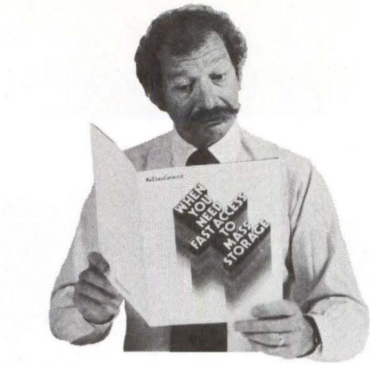
7. How OEM's solve the dilemma of keeping their system costs down with our NOVA 3 COMPUTER FAMILY.
Reader Service # 307

8. What you need to know about getting everything for a DATA ACQUISITION and CONTROL system from one place.
Reader Service # 308

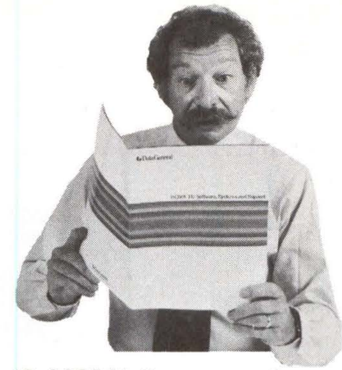
9. The last word in microprocessor-based microNOVA systems with full 16-bit NOVA architecture.
Reader Service # 309



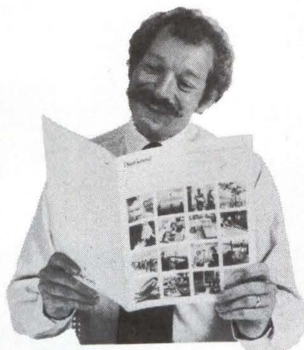
10. The amazing story behind our unique heuristic MULTI-PROGRAMMING operating system.
Reader Service # 310



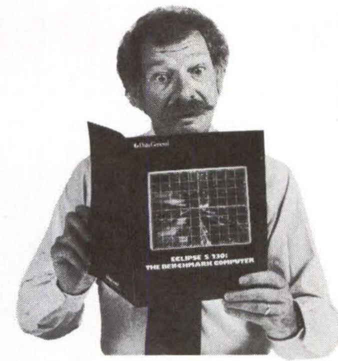
11. What to do when you need fast, fast access to MASS STORAGE.
Reader Service # 311



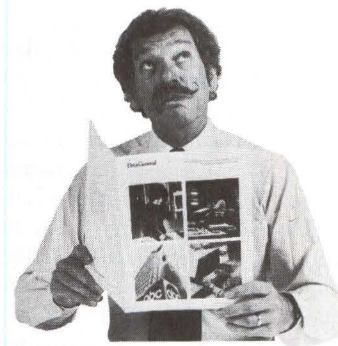
12. NOVA 3 systems, software and support let you customize a system to your application.
Reader Service # 312



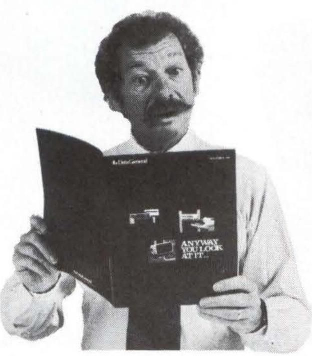
13. A wealth of information about how our computers are being used in actual APPLICATIONS.
Reader Service # 313



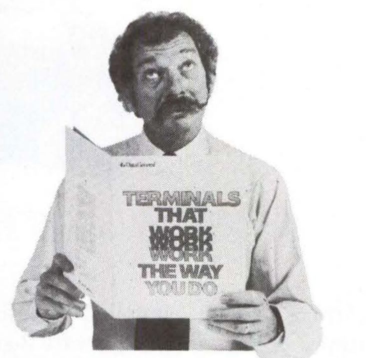
14. Wonder what sets the benchmark for big performance computer systems? Wonder no more, it's ECLIPSE S/230.
Reader Service # 314



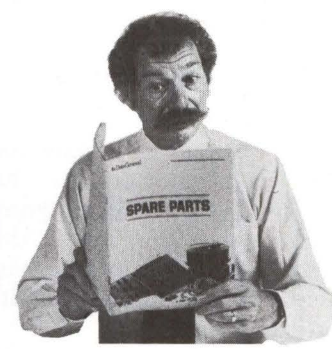
15. Is there a sensible way to use computers in DATA COMMUNICATIONS? The message comes through clear.
Reader Service # 315



16. What's the most you can expect to get from a mid-range mini today? What you get with an ECLIPSE S/130 – the standard setter.
Reader Service # 316



17. You want terminals that work the same way you do? You want the facts on our DASHER TERMINALS.
Reader Service # 317



18. Our whole SPARE PARTS catalog. They're too important to be kept a mystery.
Reader Service # 318

19. 1976 was a very good year. Our ANNUAL REPORT could be good for you.
Reader Service # 319

Mail to: Data General, Westboro, MA 01581 CD-11

☐ Yes, I'd like to pick your brains. Please send me the brochures I have circled.

☐ I'm in a hurry. Have your sales representative bring in the brochures I have circled.

Brochure numbers: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

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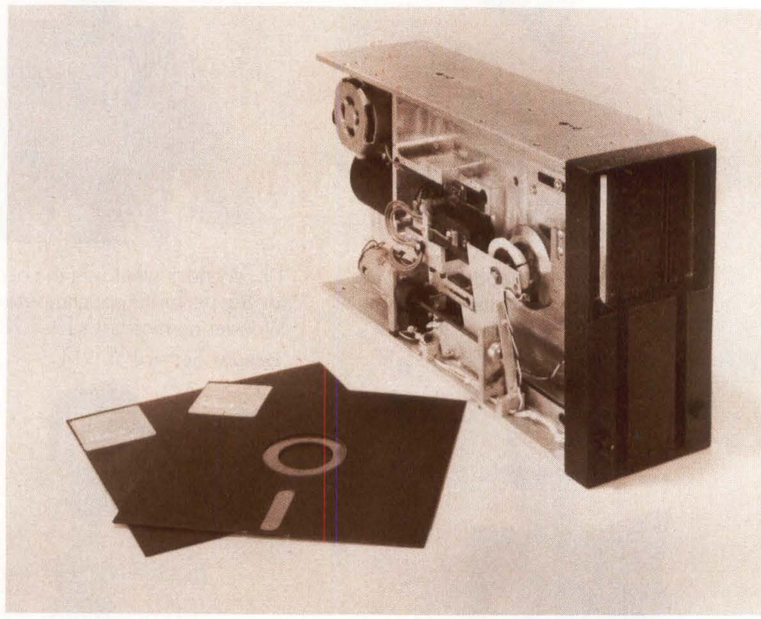
Data General, Westboro, MA 01581, (617) 366-8911. Data General (Canada) Ltd., Ontario. Data General, Europe, 15 Rue Le Sueur, Paris 75116, France, 50-006-06. Data General Australia, Melbourne (03) 82-1361.

Data General
It's smart business.

PRODUCT FEATURE

Diskette Drive Provides 4-Sided, Double-Density Capability

Although it retains the same physical outline as the company's standard dual diskette drives, the model 299 diskette drive introduced by PerSci, Inc has a maximum unformatted capacity of 25.6M bits. Fundamentally it is an enhanced version of the model 270/272/277 drives with the capability to read and record single or double density on present diskettes or on both sides of 2-sided diskettes. Four read/write heads are provided, one for each diskette surface. Two index sensors distinguish between single- and double-sided diskettes. Unlike earlier models, ac spindle motor power must be supplied.



Operating Characteristics

The electrical interface between drive and host system is maintained through three connectors. One handles all signals for the drive, the second provides dc power, and the third supplies ac power and frame ground. All of the lines in the signal interface are TTL.

Diskette select I/O lines, when activated to a logical 0 level, enable the various multiplexed signal I/O lines. Only the diskette or read/write head dedicated to the active select line will respond to the input lines and gate output lines. Normal, factory-installed connections establish individual diskette select input lines that activate the interface signals for each diskette and each side.

Options

A number of customer-installable options are available. These include multiplexing either four or eight 2-sided diskettes (two or four drives) using the four diskette select I/O lines as well as a side select I/O line. The side select signal line, not used in normal, factory-supplied configurations, defines which side of a 2-sided diskette is used for data transfer.

Standard connections allow head loading to occur when the diskette is selected if the diskette is present. However, an option that is useful in copying between diskettes allows loading of the heads independent of the state of the diskette select I/O lines if the diskette is present. A logical 0 activates the head load circuitry for the selected diskette. Heads will be loaded and stable, and data transfer may be initiated 35 ms after application of head load or side select signals.

In standard configurations, the manual eject inhibit I/O line is not connected. An option, however, allows this line, when activated to a logical 0 level, to inhibit operation of the unit's manual diskette ejection pushbutton as an OR function with the head load line. It also causes an LED to turn on for the selected diskette as an OR function with the diskette select line.

The remote eject I/O line is also not normally connected. Still another option allows this line, when activated, to energize a circuit that ejects the selected diskette. A 1-μs pulse to the logical 0 level activates the ejection circuit.

Summary of Specifications

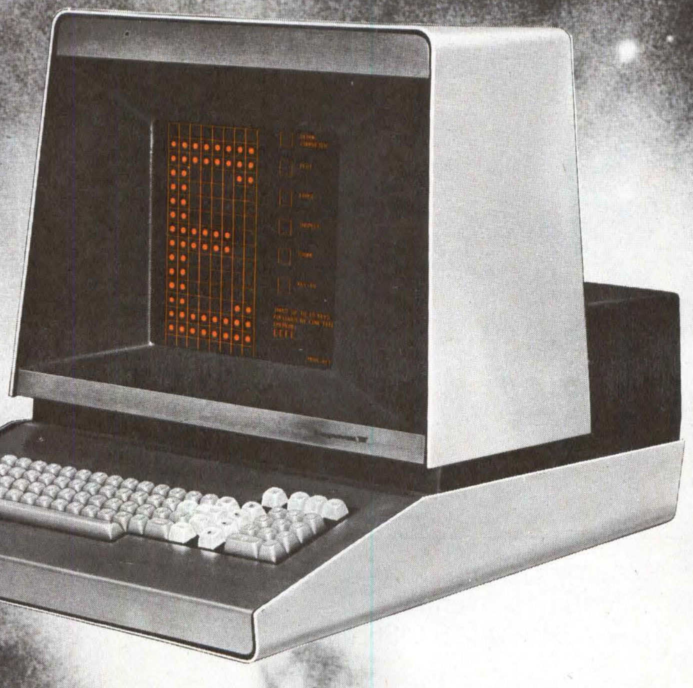
Unformatted capacities for single and double densities, respectively, are 12.8M and 25.6M bits/drive, 6.4M and 12.8M bits/diskette, and 41.7k and 83.4k bits/track. IBM format capacities in single density are 8.0M bits/drive, 4.0M bits/diskette, and

ORION-60

A New Intelligence in the Nebula

Are you seeking a bright, high-contrast display – without jitter and distortion; one that combines unlimited vector length without flicker – with full alphanumeric capability, dynamic motion, and selective edit/erase?

If so, your answer is the ORION-60 graphics display terminal from Magnavox Display Systems – the pioneer producer of plasma display terminals.



Now, because of its modular design, the ORION-60 can be upgraded to a standalone, intelligent graphic configuration. The terminal, starting at $5995, may be converted to full standalone operation with many flexible options including: resident BASIC with graphics extensions, up to 56K bytes of user memory space, floppy disc for local mass storage, communication with external host via RS-232 interface, touch panel permitting user data entry by pointing at the screen with the finger, and optical rear projection using an integral 35mm computer-addressable random access projector.

FOR A DEMONSTRATION OF THE STANDALONE ORION-60 WRITE OR CALL US AT

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Magnavox
DISPLAY SYSTEMS

Intel delivers PDP-11 memory for people who can't afford to wait.

When you're in a hurry for more semiconductor memory for your PDP-11, call Intel. We deliver memory for the full PDP-11 line. And because we're the largest manufacturer of semiconductor memory in the world, delivery is when you want it.

Why wait? Since you've chosen the leader to supply your minicomputer, it makes sense to go to the leader for memory, too. That's us.

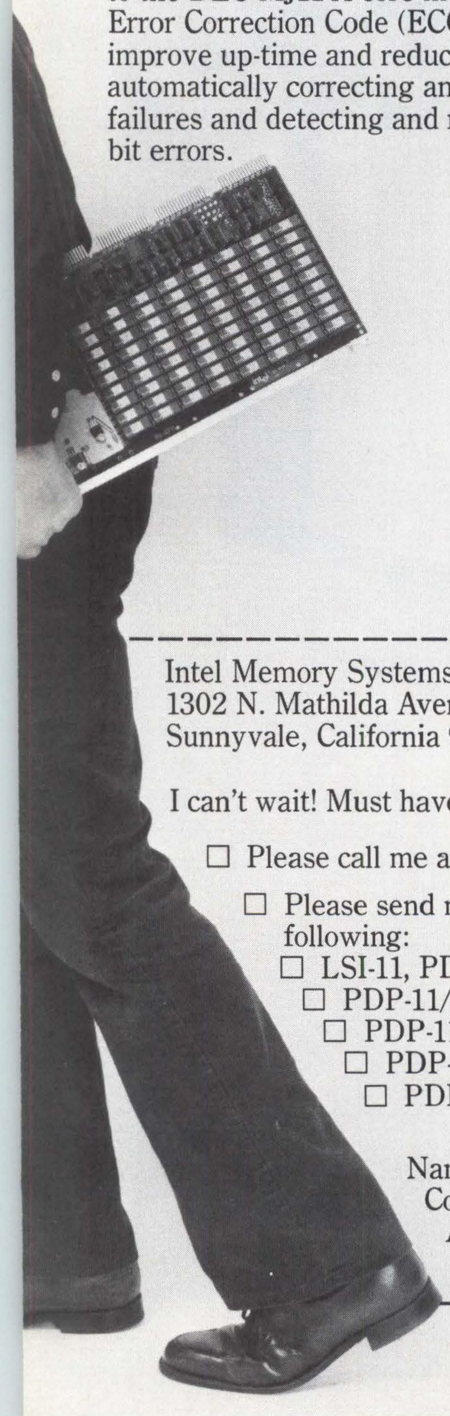
Intel memory systems save you more than time. Our in-1670 add-on memory for the PDP-11/70 is one example. It gives you four times the capacity in the same frame compared to the DEC MJ11-A core memory. And built in Error Correction Code (ECC) and Error Logging improve up-time and reduce maintenance time by automatically correcting and recording single-bit failures and detecting and recording double-bit errors.

For PDP-11 add-in memory go with our in-4711 plug in boards. You'll get memory that's even faster than DEC's. 16K words per hex-wide board. With or without parity. To further expand PDP-11 memory and reduce UNIBUS™ loading choose our in-4011 add-on. With memory management you can expand to 128K words in 16K increments. And since the in-4011 requires only one UNIBUS load, you get added system flexibility.

Get more memory for your LSI-11 and PDP-11/03 in less space with our in-1611 add-in memory. You get up to 32K words, in 8K increments, on a single, two-wide, board. That's up to eight times the memory you get with a DEC board.

When you can't afford to wait call us at 800-538-8476. In California and Canada, call 408-734-8102, x575. We'll save you time, and much more.

intel delivers.



CD-11

Intel Memory Systems
1302 N. Mathilda Avenue
Sunnyvale, California 94086

I can't wait! Must have delivery in ☐ 5 Days ☐ 30 Days ☐ _____ Days

☐ Please call me at _____/__________________ Ext. __________

☐ Please send me information on semiconductor memory for the following:

☐ LSI-11, PDP-11/03 ☐ PDP-11/40
☐ PDP-11/04 ☐ PDP-11/45
☐ PDP-11/05 ☐ PDP-11/55
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☐ PDP-11/35

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UNIBUS is a trademark of Digital Equipment Corp. Maynard, Mass.

26.6k bits/track; this format is not applicable in double density.

Transfer rates are 250k bits/s single density and 500k bits/s double. Average latency is 83 ms and head load time is 35 ms for both densities. Seek times are also the same for both: 10 ms track to track and 100 ms for 76 tracks. There is no settling time after speed.

For both densities rotational speed is 360 r/min, flux density is 6816 fc/in, and track density is 48/in. Recording densities are 3408 bits/in single density and 6816 bits/in double. Encoding methods are FM for single density, M^2FM for double.

Single-sided, soft-sectored media are IBM Diskette I or equivalent for both single density and ID or equivalent for double; single-sided, hard-sectored media are Dysan 101 or equivalent for single density and 101D or equivalent for double. Two-sided, soft-sectored media are IBM Diskette II or equivalent for single density, IID or equivalent for double; two-sided, hard-sectored are Dysan 101/2 or equivalent for single density, 101/2D or equivalent for double.

Environmental limits are 40 to 115°F (5 to 45°C) at 20 to 80% relative humidity. Ac power requirements at 50/60 Hz ±0.5 Hz are 90 to 127 V at 0.4 A typ or 180 to 253 V at 0.2 A typ; dc requirements are 24 V ±5%, 1.2 A typ; 5 V ±5%, 1.9 A typ; and −5 V ±5%, 0.15 A typ (option −7 to −16 V). The unit measures 4.38 x 8.72 x 15.00" (11.13 x 22.15 x 38.1 cm) and weighs 22 lb (10 kg).

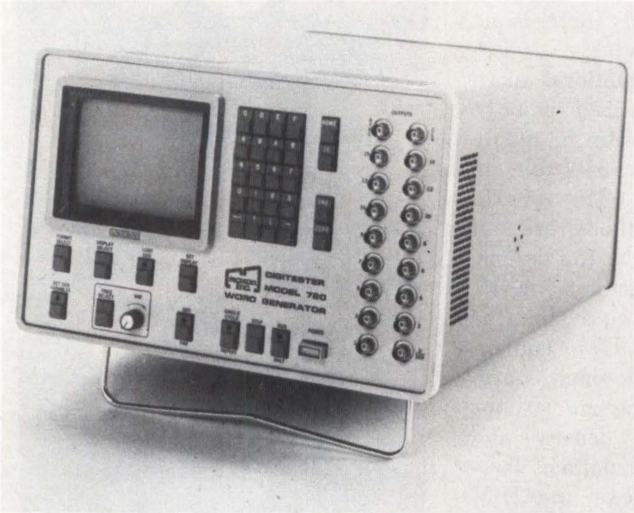
Reliability predictions include MTBF of 6000 h under typical usage, component life of 15,000 h, and media life of 3.5 x 10^6 passes/track and >30,000 insertions. Error rates are 1 per 10^9 bits soft read, 1 per 10^{12} bits hard read, and 1 per 10^6 seeks. MTTR is claimed to be 30 min.

Price and Delivery

Single unit price for the model 299 diskette drive without options is $1425. OEM discounts are available. Production deliveries will begin in February. PerSci, Inc, 12210 Nebraska Ave, West Los Angeles, CA 90025. Tel: (213) 820-3764.

For additional information circle 199 on inquiry card.

PRODUCTS



Smart Data Generator Offers Keyboard Entry and CRT Display in a Variety of Formats

Data generator features a hexadecimal keypad and scratchpad memory that directs the integral CRT display in hexadecimal, octal, binary, and timing formats to show programming of 1024 serial bits or 64-word, 16-bit parallel channels as they are formulated for loading into a transmit memory. To test microprocessors, IC development, computer simulation, and related applications, the self-contained model 720 includes all data generation, display and interface electronics. In operation, the unit generates an algorithmic pattern to pinpoint faults in hardware and software. Output data rates to 20 MHz are generated internally or fed in from an external source. Choice of 1-bit, 1-word, start-stop bits, or continuous run at true pos and neg, TTL levels is offered. Options provide interface and handshaking with other systems and controllers. **Moxon, Inc,** 2222 Michelson Dr, Irvine, CA 92715.

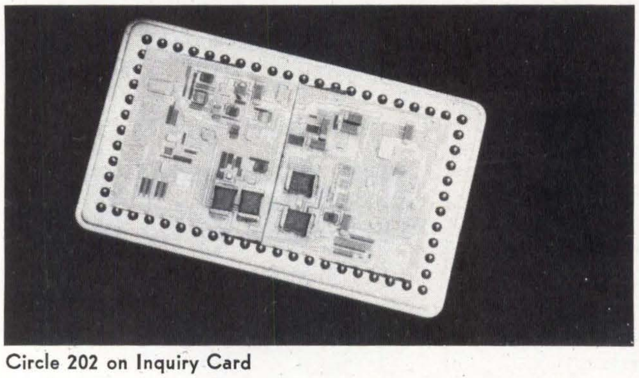
Circle 200 on Inquiry Card

Desktop Multifunction Workstation Is Integrated Microcomputer Terminal System

Benchmark results for the Microterm II Z80 microcomputer-based CRT terminal workstation, designed to measure efficiency of the BASIC interpreter in conjunction with the systems architecture, and to test the speed of completing large numbers of memory accesses and arithmetic speed of the processor, were superior to those of 21 other microcomputers. Designed around two 4-MHz Z80s with up to 48k bytes of RAM storage, the system features minimized access and wait times and can handle simultaneous functions. The desktop unit has a 24 x 80-char, 12" (30-cm) CRT; 2200-char/s nonimpact printer; and single or dual minidiskettes. Internal and external printers, dual diskettes, and memory expansion beyond 16k bytes are optional. Applications software to run with the interactive disc operating system can be programmed in extended BASIC or Z80 assembly language and debugged from the keyboard. **Digi-Log Systems, Inc,** Babylon Rd, Horsham, PA 19044.

Circle 201 on Inquiry Card

Complete 12-Bit Data Acquisition Systems Are Fabricated With Thin-Film Hybrid Technology



Circle 202 on Inquiry Card

Complex hybrid data acquisition systems are available with 16-channel single-ended (HDAS-16) or 8-channel differential (HDAS-8) inputs. Featuring a throughput rate of 50-kHz at 12 bits resolution, the devices incorporate a CMOS multiplexer, programmable gain instrumentation amplifier for gains of 1 to 1k, sample-hold, 12-bit A-D converter, 10-V buffered reference, address register, and digital control logic in a 2.3 x 1.4 x 0.24" (58.4 x 35.6 x 6.1-mm) 62-pin package. Performance equals that of larger, modular systems. Specs include 100-MΩ resistance, 200-pA max input bias current, and 10-μV/°C X gain offset drift. Acquisition and conversion times are 9 μs. Three modes of operation are free-running sequential, triggered sequential, and random addressing. A hermetically sealed, full military temp range model, operating over −55 to 125°C, is available. **Datel Systems, Inc,** 1020 Turnpike St, Canton, MA 02021.

HP9830A/B and Infotek...

made for each other.

If you use the HP9830A/B, you know that it has great potential.
Now you can extract the full measure of 9830 capabilities with Infotek's Memory, ROMs and Peripherals.

Memory. The EM-30, 32,192 byte memory for the '30, pioneered by Infotek, is one of the most significant contributions to increasing the '30's power.

EM-30B, in conjunction with Infotek's Mass Memory II ROM multiplies the speed of the 9880B Mass Memory System by avoiding redundant disc operations. A must for the 9880B user!

Fast Basic ROMs. The Fast Basic ROM series provides 54 statements, functions and commands. With these ROMs your '30 acquires versatility and speed superior to any other desk top computer. Here's just a few examples of Fast Basic Power.

- *** Dimension arrays any size you like. Sort or search any array that will fit in your memory!**
- Move information in or out at 10K bytes per second . . . fabulous for instrumentation and control applications.
- Interrogate and amend variables without halting the program, just like a live keyboard.
- Suspend any program including mass memory operations to cassette or floppy for future completion.
- Interrupt capability — a peripheral can now demand service, branch or initiate program execution.
- Edit program test and super-secure both program and data files.

If this is the kind of added capability that you can use in your '30 then read on, there's more!

The FD-30 Series Floppy Discs. Each of the FD-30s stores 305K bytes. Organize this information any way you like up to 2387 files. Best of all, you can talk to the FD-30s without any software changes because the FD-30 series obeys *every* 9830 cassette instruction.

The series consists of the FD-30A single disc unit, FD-30S slave drive, FD-30M multiple disc drive which contains a master and up to three slave drives, and the FD-30SR slave drive system which will accommodate one to four drives.

A single master will support up to seven slaves and only one I/O slot is used.

Peripherals. Infotek has applied the same level of ingenuity reflected in the ROMs and floppys to the development of extremely high quality and reliable peripherals tailored to the needs of the 9830A/B. Now available are:

- LP-30, a 200 line per minute matrix printer
- CP-30, a 45 character per second character printer/plotter
- PS-30, a paper tape punch/reader
- TC-30 and RT-30 time clocks
- RS-30, a 9600 BAUD RS 232-C interface with 7 quartz reference rates.
- FI-30, a 10K byte/sec TTL I/O

Contact us now for the name of your local Infotek representative. Discover why more than a thousand 9830 users working with Infotek enhancements believe that the 9830 and Infotek are made for each other.
World-wide service and distribution centers back up Infotek's liberal warranty and service commitment.
At Infotek we're dedicated to making good computers better.

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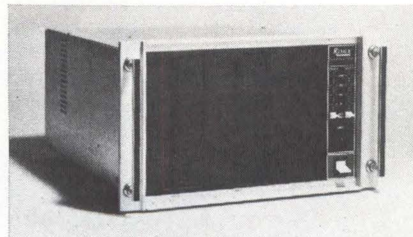
The 9830A/B is a product of Hewlett-Packard Company.

CIRCLE 82 ON INQUIRY CARD

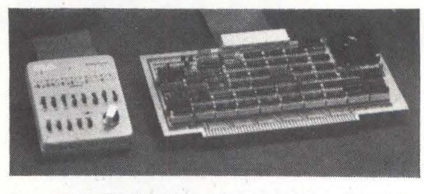
PRODUCTS

FLEXIBLE DISC SYSTEM



An integrated hardware/software unit, disc system connects directly to the PDP-11 Unibus; software modules allow it to operate in an RT-11 environment, using either std DEC RX-01 26-sector format or a 16-sector format which increases storage capacity by 25%. Up to four flexible disc drives can be included in the -11 installation. A single rackmounted unit contains controller/formatter circuitry, power supply, disc storage bin, and space for two drives. **Ex-Cell-O Corp, Remex Div,** 1733 Alton St, PO Box C-19533, Irvine, CA 92713.
Circle 203 on Inquiry Card

S-100 BUS-COMPATIBLE LOGIC ANALYZER BOARD



Specifically designed to support troubleshooting on the S-100 bus, the model 150 Bus Grabber can monitor, analyze, and display the 16-bit address bus; 8-bit data bus; and MPU control, status, and interrupts without disassembly of the computer. 56 bus signals are monitored simply by plugging the PC board into any available computer slot. Eight additional user-defined signals are available for monitoring other points or ICs inside the computer. **Paratronics, Inc,** 800 Charcot Ave, San Jose, CA 95131.
Circle 204 on Inquiry Card

COLOR GRAPHICS TERMINAL

An intelligent color graphics terminal uses a permanently converged CRT, optimized for digital color displays. Configured as a standalone terminal or rackmount unit with detached keyboard, it features std ASCII alphanumerics, bar graphics, reverse video, blink, and up to 800 special symbol graphics, 512 of which are microprogrammable. Individual foreground/background selection in any of eight colors is made on a char-by-char basis. **Industrial Data Terminals Corp,** 1550 W Henderson Rd, Columbus, OH 43220.
Circle 205 on Inquiry Card

When we installed our first minicomputer disk system, we talked a lot about RELIABILITY.

4000 systems later, our customers tell the story.

Reliability. We do more than just talk about it. We deliver it. That's one of the main reasons we're now the world's largest independent supplier of minicomputer disk storage systems.

We've delivered more than 4,000 systems since we installed our first one in 1971. That's strong evidence of hardware reliability and product acceptance.

There's a lot more to the story. Behind our reliable hardware is a reliable company that keeps delivery commitments, provides total software support and responds quickly to customer service requirements. Ask our customers.

We make good disk drives work better through *Extended Emulation.*™ This powerful approach adapts software to emulate the CPU manufacturer's operating systems—while still taking full advantage of the unmatched performance offered by our disk system. Whether you need disk storage for mini or micro, you need to know about the important benefits *Extended Emulation* can provide.

The diverse applications for our disk systems are regularly described in our quarterly newsletter, *The Bit*. If you'd like to be on our complimentary mailing list, use the coupon today. We'll send you the current issue. And if you need product data, or help with a specific application, contact the System Industries sales/service office nearest you.

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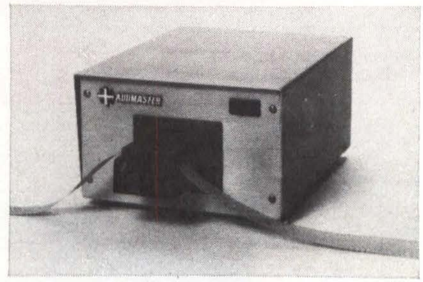
Germany, Dusseldorf: 0211-400606. **Sweden, Stockholm:** 08-236-640.
United Kingdom, Woking: (4862) 70725.

CIRCLE 84 ON INQUIRY CARD

PRODUCTS

STANDALONE PAPER TAPE READER



Having greater capacity than earlier models, model 612 has the ability to read 5- to 8-level tape and transmit 7 to 11 frames/char at 50 to 9600 baud. The standalone paper tape reader also features starting and stopping on char at all speeds; choice of manual control or X-on, X-off; 90- to 260-V, 50- to 60-Hz power; and even, odd, or no parity. RS-232, current loop, or parallel outputs are available. **Addmaster Corp,** 416 Junipero Serra Dr, San Gabriel, CA 91776.
Circle 206 on Inquiry Card

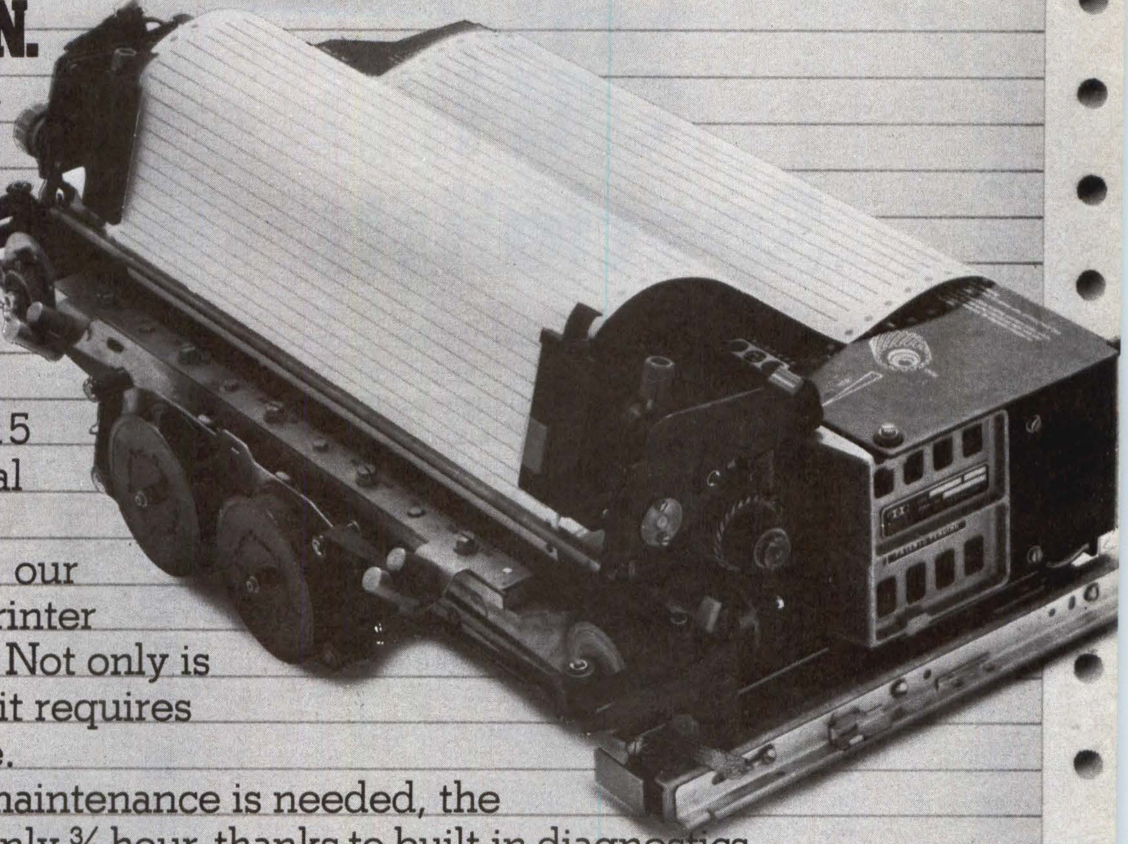
SELECTOR CHANNEL EMULATION UNIT

High performance IBM (or IBM plug-compatible) peripheral devices attach to a medium-scale minicomputer system with the SCEU emulation unit for increased performance. Unit generates protocol sequences required by the IBM PCU in response to operational commands of the minicomputer CPU. It also converts IBM selector channel's 8-bit data path into 16- or 32-bit word-path size for host CPU. Up to 255 device control units are supported at combined data transmission rates of >2.4M bytes/s. **Information Products Systems, Inc,** 6565 Rookin, Houston, TX 77074.
Circle 207 on Inquiry Card

PRESSURE-SENSITIVE POSITION SENSOR

A finger, ballpoint pen, or similar stylus can be used to select or determine positions on an underlying image with the E270 transparent position sensor which is a plate glass substrate coated with semiconductive metal oxide. An electrically isolated plastic cover sheet with a transparent conductive coating is placed over the substrate. Pressure applied to the cover sheet makes contact between the two. X and Y coordinates are converted from analog to digital by an ADC. **Elographics, Inc,** 1976 Oak Ridge Tpk, Oak Ridge, TN 37830.
Circle 208 on Inquiry Card

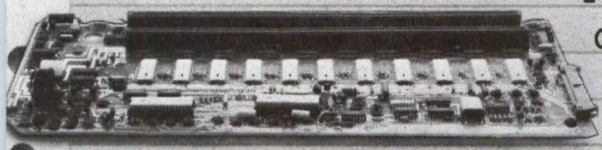
AT UNDER $2000, THE MODEL 40 OEM PRINTER NOT ONLY COSTS LESS TO BUY–IT ALSO COSTS LESS TO OWN.



It costs less to buy because for less than $2000 you get a 300 lpm printer that's completely operational. All you furnish are 115 VAC and the serial signal source.

Once on-line, our model 40 OEM printer costs less to own. Not only is it highly reliable, it requires little maintenance.

Even when maintenance is needed, the MTTR averages only ¾ hour, thanks to built-in diagnostics that help pinpoint trouble quickly. And with only seven modular mechanical assemblies and one CMOS logic card, repairs are simple.



This modularity and diagnostic capability also cut the cost of training service personnel.

To reduce your logistics problems and spare parts inventory, there's an 80% parts commonality between all model 40 printers. Plus Teletype offers an exchange repair service that can save you up to 50%.

For more information about our model 40 OEM printers, send in the coupon. Or call 312/982-2000.

TELETYPE®

THE TELETYPE® MODEL 40 OEM PRINTER.
NOTHING EVEN COMES CLOSE.

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5555 Touhy Ave.
Skokie, IL 60076

Please send me additional information about the model 40 OEM printers.

Name________________

Title________________

Company________________

Address________________ Phone________

City________________ State________ Zip________

CIRCLE 86 ON INQUIRY CARD

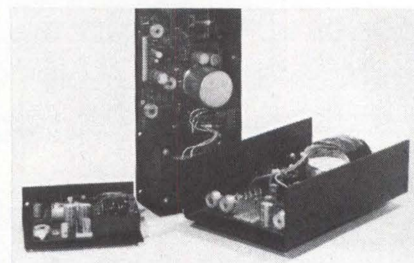
PRODUCTS

RS-232 TO CURRENT LOOP/ TTL ADAPTER

ADApter has two circuits—one converts RS-232 signal to a 20-mA current loop signal, and the other converts 20-mA current loop signal to RS-232 signal. Device permits teletypewriter ports to be used to drive an RS-232 terminal, or vice versa, without modification of the port; it can also be paralleled to drive a teleprinter or RS-232 printer while using the computer's regular terminal. Device does not alter baud rate and uses std power supplies with low current requirements. **Connecticut Microcomputer,** Pocono Rd, Brookfield, CT 06804.

Circle 209 on Inquiry Card

FLOPPY DISC DRIVE POWER SUPPLIES



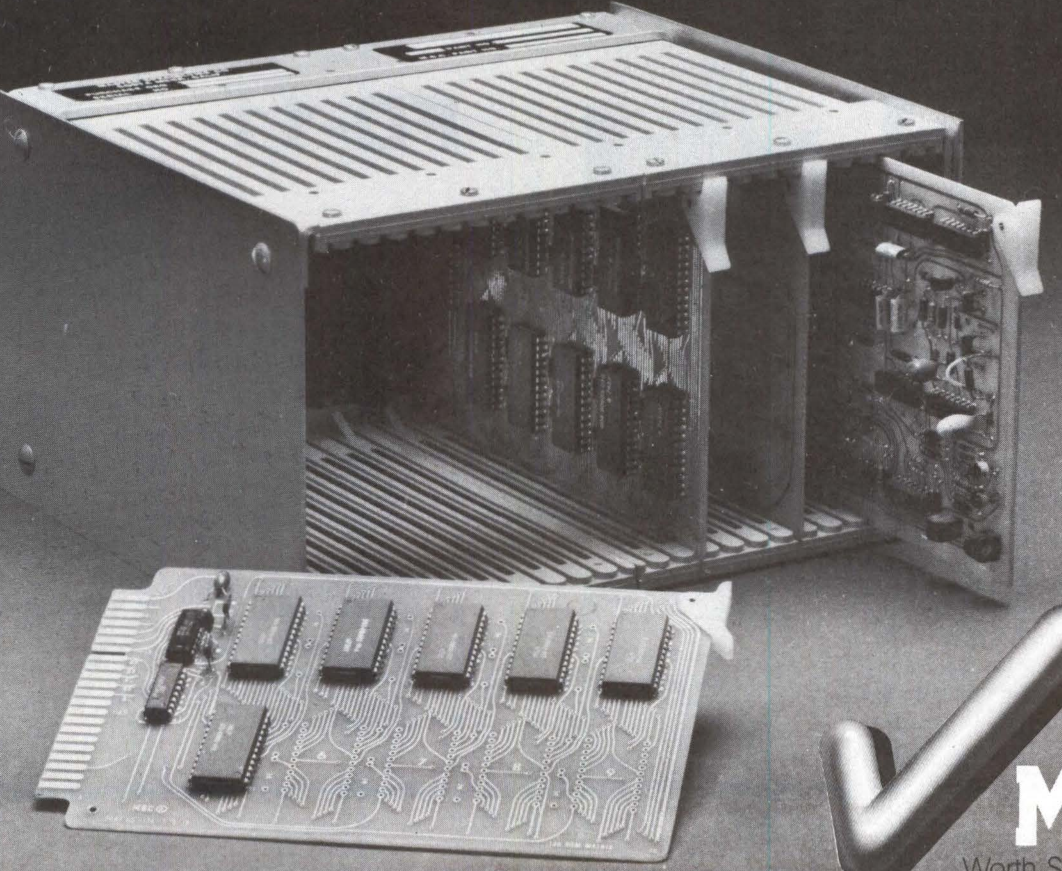
Open frame power supplies designed for ac-powered floppy disc drives include the 2BXFD, which is aimed at systems incorporating the Shugart Mini Floppy (or equivalent) drive; 2PFD and 2QXFD supplies are intended to operate single and dual floppy disc drives. All outputs are adjustable and regulated to ±0.15% for line or load variations with 10-mV pk-pk ripple except for the two low power (0.5/0.6 A) 5-V outputs that have a total tolerance of ±3%. **Alpha Power, Inc,** 20536 Plummer St, Chatsworth, CA 91311.

Circle 210 on Inquiry Card

MICROHYBRID 2-QUADRANT DIVIDERS

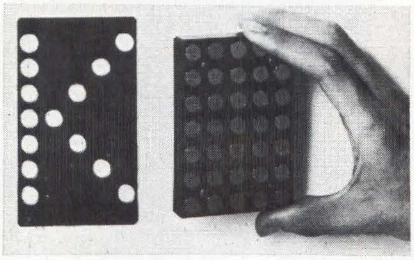
A transconductance dividing element, stable reference, output amp with specified accuracy internally trimmed for feedthrough output zero and gain trim comprise the 500 series of microhybrid dividers. For microprocessor-based systems, 503 through 506 divide in two quadrants with a transfer function of −10X/Y. For 0 to 70°C operation, they are specified for dividing errors of 1, 0.5, 0.25, and 0.10% at 25°C. Output provides ±10 V at 5 mA, and is short-circuit protected. **SGR Corp,** Neponset Valley Industrial Pk, PO Box 391, Canton, MA 02021.

Circle 211 on Inquiry Card



PRODUCTS

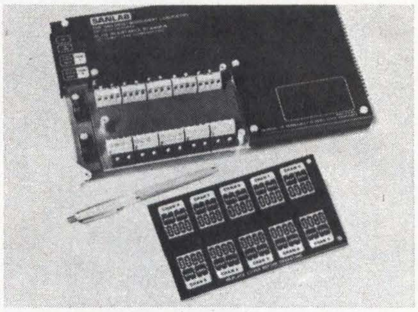
LARGE LED ALPHANUMERIC DISPLAY



For use in illuminated displays, the "Datablox" alphanumeric LED matrix display provides alphanumeric digits 4 x 3" (10 x 7.6 cm) and uses 35 (5 x 7 matrix) high intensity LEDs mounted in individual reflectors. With wide angle viewing, digits can be read at distances of 200 ft (61 m) in normal office lighting conditions. Features include low power, long life, and ruggedness. Compatible with solid-state drive, they can generate the full 64-char ASCII set. **Chicago Miniature Lamp Works, General Instrument Corp,** 4433 N Ravenswood Ave, Chicago, IL 60640.
Circle 212 on Inquiry Card

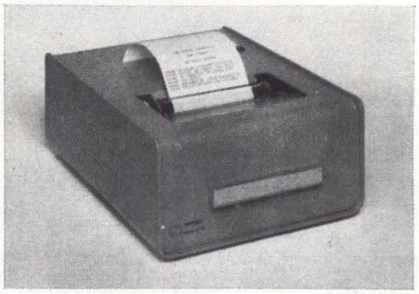
10-CHANNEL RTD SCANNER

A modular scanner in a card-mounted, shielded package, the SL115 connects 10 platinum resistance thermometers directly to a user's high level A-D converter, and excites, lead compensates, continuity tests, linearizes, amplifies, and filters the signals. Remote calibration features give online calibration of the scanner at the ice point. Control logic is DTL/TTL/CMOS-compatible. The unit gives output sensitivities from 1 to 100 mV/°C. **San Diego Instrument Laboratory,** 7968 Engineer Rd, San Diego, CA 92111.



Circle 213 on Inquiry Card

IMPACT DOT MATRIX PRINTER



As a standalone unit, the model SP-302 5 x 7 impact dot matrix, 40-col intelligent printer features a microprocessor controller that allows double width printing and double and triple space format; tab functions are also std for simple software control from a host device or computer. Unit prints 50 char/s and has multiple copy capability. Inputs include RS-232 and a 20-mA current loop. Input baud rate of 110 is std; other rates can be internally set. **Syntest Corp,** 169 Millham St, Marlboro, MA 01752.
Circle 214 on Inquiry Card

The CRT terminal for the systems designer

You can change it to fit your system—instead of vice versa.

New microtechnology, new systems, new applications. It's all changing quickly. Our challenge: design a CRT terminal flexible enough to keep up with your ideas —one to help you make the most of your latest system, not compromise it.

The 480/25 is the result.

Need an intelligent CRT terminal?

O.K. The 480/25 is an addressable/pollable intelligent CRT terminal that can accommodate a variety of protocols. It offers local editing, protected field formats, block transmission, and more.

It can save time; no time-fill characters needed, even at 9600 bits per second.

It offers cursor positioning by—and reporting to—the host computer. And, of course, it can store forms locally and automatically check formats.

Need a cluster controller or a microcomputer?

Fine. One 480/25 can control a series of terminals and also communicate with a host computer. Or, you can add a disc, a printer, and expanded memory to a 480/25—and you've created a true microcomputer with integrated CRT and keyboard.

Etc., etc., etc.

The fact is, combine your software and the right peripherals and you can have 480/25 doing all kinds of handsprings for you. So instead of clamping a lid on your system, it can spring loose some great ideas.

Get the details.

It's easy, just ask.
Call (213) 966-3511. Or write.
CONRAC, 600 N. Rimsdale Avenue,
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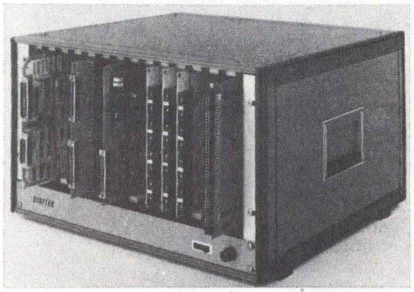
PRODUCTS

PROCESS CONTROL SYSTEM



A flexible, microprocessor-based system, which includes a complete software package for supporting up to 16 control loops and 16 additional inputs with alarm limits, controls such parameters as temp, pressure, and flow rate, and provides monitoring and control of variable high or low analog conditions. System interfaces easily to peripherals such as CRT terminals, printers, and floppy disc drives. Programming is done in BASIC with some subroutines written in assembly language. **Digitek, Inc,** 5950 6th Ave, S Suite 101, Seattle, WA 98108.
Circle 215 on Inquiry Card

PROCESS MINICOMPUTER SYSTEM PERIPHERALS AND CPUs

A wide range of products for the 300 process computer systems include five peripherals and three CPUs based on the 330 model. The 330-R10, R20, and R30 minicomputers and the 340-R40 multiprocessor system are CPU units whose quantitative specs vary. They have identical instruction set, including bit, byte, field, 32-bit fixed-point and 64-bit floating-point instructions; powerful autonomous I/O processors; and same interface structure for peripherals. **Siemens AG,** Postfach 3240, D-8520 Erlangen 2, Federal Republic of Germany.
Circle 216 on Inquiry Card

AC LINE REGULATOR

OEM-3150 line regulators use the company's patented multiprimary switching regulator circuit which operates at 99% efficiency and generates no noise or distortion. Response time for worst case, complete correction is 0.5 cycle, and regulators are insensitive to frequency and power factor changes. The package has been optimized for easy installation. Dimensions are 4.5 x 4.8 x 8" (11.4 x 12.1 x 20.3 cm) and a 1.5-kVA regulator weighs 12 lb (5.4 kg). **Power-Matic, Inc,** 8076 Engineer Rd, San Diego, CA 92111.
Circle 217 on Inquiry Card

PHOTOELECTRIC SCANNER

A solid-state chip for self-contained reflective scanning combines miniaturized LED and phototransistor elements in a 0.375" (0.95-cm) diam unit. Operating with the company's "M" series modulated amps, LP-400 has a 0.5 to 3" (1.3 to 7.6-cm) adjustable range to detect objects as small as 0.010" (0.025 cm) in diam. Response time is 1 ms. Due to wide field of view and adjustable amp sensitivity, it is easy to set up and keep aligned. **Banner Engineering Corp,** 9714 10th Ave N, Minneapolis, MN 55441.
Circle 218 on Inquiry Card

0.5" PLANAR GAS DISCHARGE DISPLAY

Accommodating up to 16 char in a package measuring 1.55 x 8.90" (39.4 x 226.1 mm), SP-451 is based on 14-segment design. Messages consist of numerals, letters, and special symbols to satisfy POS and instrumentation displays. Character size, variety, brightness, and 130-deg viewing angle provide readability in bright, dark, or otherwise difficult conditions. Designed for edgeboard mounting, the display requires only 0.8" (2.0 cm) mounting depth, including tubulation. **Beckman Instruments, Inc,** 2500 Harbor Blvd, Box 3100, Fullerton, CA 92634.
Circle 219 on Inquiry Card

CIRCLE 92 ON INQUIRY CARD

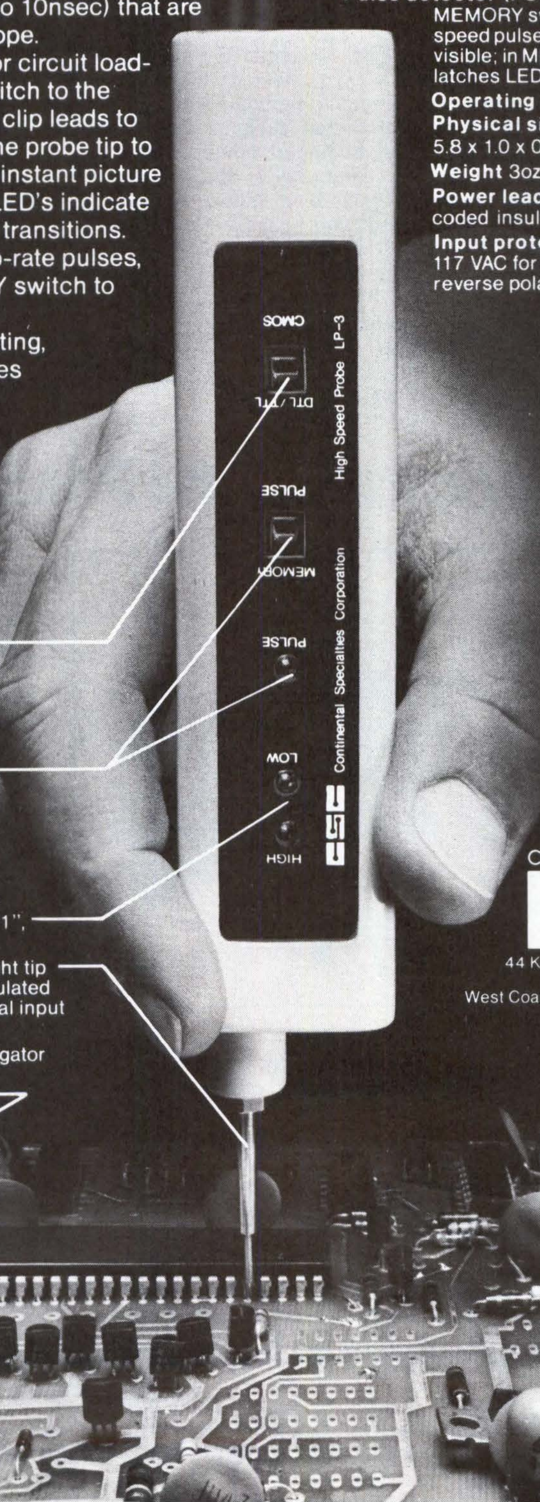
10 nsec. $69.95

Meet CSC's LP-3. The multi-family logic probe that's as fast as a high-speed memory scope. At about 1/100th the price.

You won't want to be without this compact, enormously versatile test and troubleshooting tool that does the work of a level detector, pulse detector, pulse stretcher and memory probe. It gives you instant, positive indications of circuit conditions—capturing one-shot and low-rep-rate pulses (down to 10nsec) that are barely visible, even on a fast scope.

Easy to use. No sync, polarity or circuit loading to worry about: just set a switch to the proper logic family, connect two clip leads to the circuit's supply and touch the probe tip to the node under test. You get an instant picture of circuit conditions: Separate LED's indicate logic "1", logic "0" and all pulse transitions. To store single-shot and low-rep-rate pulses, simply set the PULSE/MEMORY switch to MEMORY.

At $69.95, LP-3 simplifies testing, debugging and servicing all types of digital circuits, with pulses as fast as 10nsec. See your CSC dealer today. Or call 203-624-3103 (East Coast) or 415-421-8872 (West Coast) for the name of your local stocking distributor and a full-line catalog.



Logic Family Switch—TTL/DTL or CMOS matches Logic "1" and "0" levels; CMOS position also compatible with HTL, HiNIL and MOS logic.

PULSE/MEMORY Switch & LED—PULSE position detects and stretches pulses as narrow as 10 nanoseconds to 1/10 sec.; MEMORY stores single-shot and low-rep-rate events indefinitely; HI/LO LED's remain active.

HI/LO LED's—Display level (HI-logic "1", LO-logic "0") of signal activity.

Interchangeable probe tips—Straight tip supplied; optional alligator clip and insulated quick-connecting clip available. Optional input ground lead.

Plug-in leads—24" supplied, with alligator clips. Virtually any length leads may be connected via phono jack.

*Manufacturer's Recommended Resale

Specifications

Input impedance 500,000Ω

Thresholds (switch selectable)	**DTL/TTL**	**HTL/CMOS**
logic 1 thresholds (HI-LED)	2.25V ± .10V	70% Vcc ± 10%
logic 0 thresholds (LO-LED)	0.80V ± .05V	30% Vcc ± 10%

Min. detectable pulse width 10nsec. guaranteed

Pulse detector (PULSE LED) in PULSE position of PULSE/MEMORY switch, 1/10-sec. pulse stretcher makes high-speed pulse train or single events (+ or − transitions) visible; in MEMORY position, first transition lights and latches LED

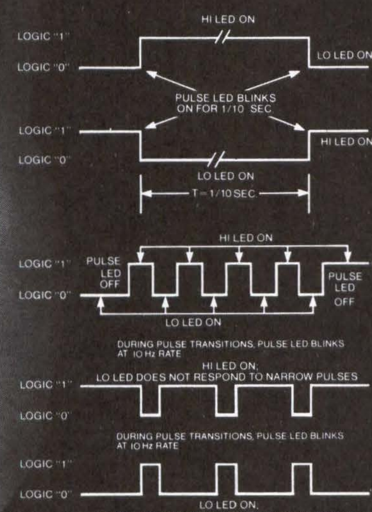
Operating temperature 0-50°C

Physical size (l x w x d) 5.8 x 1.0 x 0.7" (147 x 25.4 x 17.8mm)

Weight 3oz. (.085Kg)

Power leads removable 24" (610mm) with color-coded insulated clips; others available*

Input protection overload, ± 25V continuous; 117 VAC for less than 10 sec.; reverse polarity, 50V



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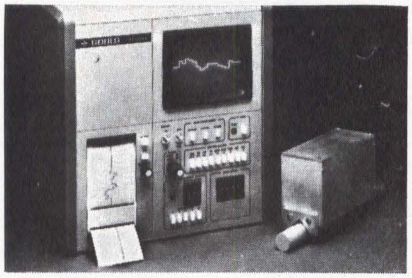
CIRCLE 93 ON INQUIRY CARD

PRODUCTS

MULTIPOINT, NONCONTACT GAUGING SYSTEM



Electronically scanning production parts and instantly displaying their critical dimensions, the microprocessor-based speedgage system reduces time and cost. A part is scanned in <2.5 s by an array of up to 240 noncontact capacitive-type sensing probes, and compared with dimensions stored in an internal memory. Errors then appear as a step trace on the CRT screen. Nine pushbutton-selected vertical sensitivities range from 20 μin (0.5μm)/div to 10,000 μin (250μm)/div. **Gould Inc, Instrument Systems Div,** 3631 Perkins Ave, Cleveland, OH 44114.

Circle 220 on Inquiry Card

SINGLE STATION PC SWITCH

Designed to provide a gating function on a PC board, stackable design for multifunction switching features a low 0.028" (0.07-cm) profile, large, sturdy lever wheel for positive wiping action, and large, easily read characters. Housing is black thermoplastic polyester, 30% glass-filled. Base is black, type 6/6 nylon, 30% glass-filled. Mechanical performance is rated at 2000 switching operations for each spst station; electrical performance is rated 50 Vdc at 100 mA, nonswitching. **Stanford Applied Engineering, Inc,** 340 Martin Ave, Santa Clara, CA 95050.

Circle 221 on Inquiry Card

RAM BOARD IN SEMIKIT FORM

Offered fully assembled and wave soldered with pretested ICs, semikit memory modules eliminate common kit-building problems such as bad solder joints, heat damaged components, and faulty ICs. Features of the 16KRA include a 16,384-byte memory, invisible refresh, and worst-case access time of 400 ns. Each 4096-word block is independently addressable for max system flexibility. Power is typ 5 W; backup power connection is built-in. **Processor Technology Corp,** 6200 Hollis St, Emeryville, CA 98608.

Circle 222 on Inquiry Card

MINICOMPUTER EXTENDED MEMORY UNIT

A solid-state, plug replacement unit for DEC RF/RS-11, the EMU™ requires 2.1-μs access time to set up control registers and initiate transfer of information to and from main memory. Information is transferred at a 1-μs data rate. Design utilizes interchangeable memory modules, each consisting of 64k x 9 bits of 16k RAM. Dual port UNIBUS® interface allows access by two processors and incorporates card interchangeability. **Monolithic Systems Corp,** 14 Inverness Dr, Englewood, CO 80110.

Circle 223 on Inquiry Card

WIREWRAP PCBs

For users who want to build their own LSI-11 type I/O and memory systems, board, uncommitted and designed for insertion of wirewrap pins, accommodates approx 130 std 14- and 16-pin DIPs, plus necessary passive components. Featuring ±12 V on ground, board is fully grounded on one side with grounded shield at circuit size. Half-size version (WW-11.5) measures 5.255 x 8.4" (13.272 x 21.3 cm), while full-size version (WW-11) measures 10.450 x 8.4" (26.54 x 21.3 cm). **Artec Electronics, Inc,** 605 Old County Rd, San Carlos, CA 94070.

Circle 224 on Inquiry Card

If you're this kind of systems OEM,

You're building complex turnkey projects.

You need more than "iron".

You know that your best buy is not a mixed bag of bottom-priced components, but a proved system, with all essential support, from a supplier who becomes your working partner.

we're your kind of computer systems source.

We're different. Instead of selling you black boxes, we supply complete computer systems. We've been doing this for seven years.

We have a state-of-the-art line of standard processors, memories, I/O devices, terminals and other peripherals. Plus proved system operating software that speeds your application programming. Advanced network and transaction software. And we'll quote special hardware and software where needed.

You'll like our systems engineering help, because we understand system problems. And we don't love you and leave you, but supply full support — field service, documentation, personnel training, even sales support.

What you get from MODCOMP is a fully checked-out system, factory burned-in, ready to bring on-line quickly and efficiently.

Get the full MODCOMP OEM story, by asking for the brochure, "Power Tools For Building OEM Systems". Modular Computer Systems Inc., 1650 W. McNab Road, Fort Lauderdale, Fla. 33309. (305) 974-1380.

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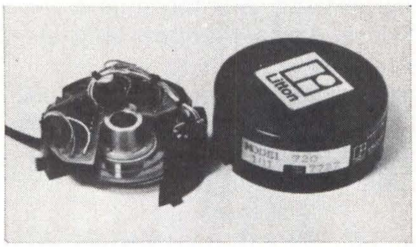
CIRCLE 98 ON INQUIRY CARD

Two Modcomp IV and four Modcomp II processors are the center of a new digital traffic control system for the city of Baltimore, engineered by TRW Inc. The TRW system has the capacity to control signals at 1200 key intersections in the city, and also provide surveillance of a five-mile section of the Jones Falls Expressway.

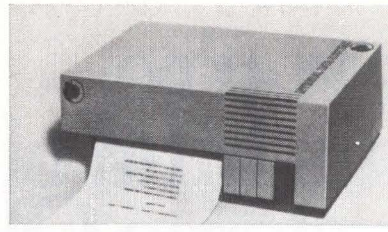
MODULAR OPTICAL ENCODER



Model 720 is a kit that consists of easily installed photohead and disc assembly. It provides a means of sensing rotary speed or angular position in applications where space is at a premium and little inertia and no additional torque can be added to the system. Features include solid-state LED sources, phototransistor sensors, optical quality glass commutator disc, and direct DTL, TTL, CMOS, and discrete component compatibility. Std resolutions range from 24 through 2540 cycles. Voltage options are 5, 12, 15, and 24 V. **Litton Systems, Inc, Encoder Div,** 20745 Nordhoff St, Chatsworth, CA 91311.

Circle 225 on Inquiry Card

DOT MATRIX IMPACT PRINTER



Ready-to-use, tabletop dot matrix impact printer for mini or microcomputer systems prints up to 120 char/s with 80 to 132 char/line. Features include an RS-232 and current loop serial interface and enhanced mode (double width) char. Multiple copy capability on both fanfold and roll paper is std. Serial baud rates of 110 to 1200 bits/s are selectable; parallel interface capability is also provided. A 5 x 7 dot matrix is used to print std 64-char ASCII set. **Integral Data Systems, Inc,** 5 Bridge St, Watertown, MA 02172.

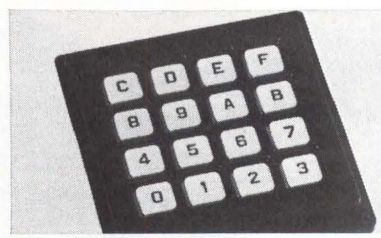
Circle 226 on Inquiry Card

SC/MP BIPOLAR p/ROM CARD

Designed to be bus- and card-size compatible with the National ISP or the company's PDC family of cards, PDC-311 replaces complex erasable p/ROMS with multiple-sourced, simple to program bipolar p/ROMs. The card uses std open-collector or 3-state 256 x 4 or 512 x 4 bipolar p/ROMs, with 2k of memory from 256 x 4 p/ROM and 4k from 512 x 4 p/ROMs. It has full 65k address decoding and is complete with p/ROM sockets. A 5-V supply is required. **MilerTronics, Div of George Miler Inc,** 303 Airport Rd, Greenville, SC 29607.

Circle 227 on Inquiry Card

12- OR 16-BUTTON KEYBOARD FAMILY

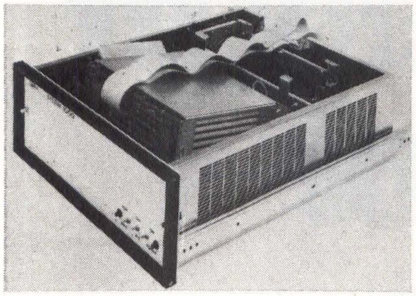


A choice of 12- or 16-button arrays plus circuitry, mounting means, and legending is offered by this keyboard family. Circuitry options include matrix coding, single pole/common bus switching, 2-out-of-7 or 2-out-of-8 code. Either 3 x 4 or 4 x 4 array is available with post mounting or screw type flange mount. Std keyboard arrangements have molded-in legends, hot-stamped legends to customer order, and snap-on caps for self-legending of prototypes. **Grayhill, Inc,** 561 Hillgrove Ave, La Grange, IL 60525.

Circle 228 on Inquiry Card

PRODUCTS

MODULAR DATA ACQUISITION SYSTEM



Data acquisition 1000 system series for industrial and scientific applications consists of a rack drawer, card cage/backplane assembly which holds up to 11 8.5 x 10" (21.6 x 25.4 cm) or 22 8.5 x 5" (21.6 x 12.7 cm) or any mixture of DEC LSI-11 bus-compatible PC cards. Standalone system has LSI-11 microcomputer and min 4k RAM for up to 700 high level analog input channels, 128 low level analog input channels, or up to 700 digital I/O functions. **Adac Corp,** 15 Cummings Pk, Woburn, MA 01801.
Circle 229 on Inquiry Card

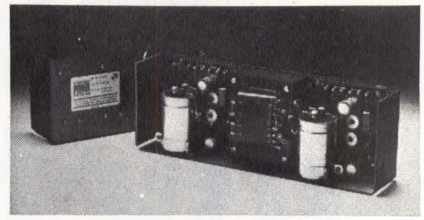
ADVANCED FAULT RESOLUTION CAPABILITY

Advanced fault resolution (AFR) option for Capable 4000 logic testers finds both component and production defects in microprocessor circuits and also indicates exactly which component to replace or etch to repair. Step-by-step instructions on a video display terminal tell the operator where to place a current sensing probe. At the same time, the tester injects a controlled current pulse into the signal bus; the package controls both current pulse and current sensor. **Computer Automation, Inc, Industrial Products Div,** 18651 Von Karman, Irvine, CA 92713.
Circle 230 on Inquiry Card

DISKETTE WRITE PROTECT OPTION

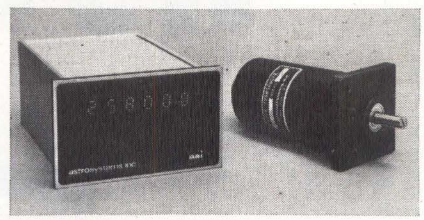
A write protect option available on the 9512 micro-disc allows the user to protect data files stored on any diskette via a small hole punched in the diskette jacket. A sensor and associated circuitry within the 9512 inhibit activation of the write mode when this hole is open. To re-enable recording on a protected diskette, the hole can be covered with black opaque tape such as electrical tape. **Techtran Industries, Inc,** 200 Commerce Dr, Rochester, NY 14623.
Circle 231 on Inquiry Card

MULTIPLE-OUTPUT DC POWER SUPPLIES



SPS-D and -T models provide power for memories, floppy discs, op amps, microprocessor circuitry, logic, and transistorized circuitry. Std adjustable voltages range from ±5 to ±28 Vdc (±10%). Currents are available from 1.0 to 12 A. Features include complete isolation between outputs, 115/230 Vac, 47- to 440-Hz input, temp compensated circuitry, output voltage adjust, and current limit short-circuit protection. Line and load regulation is ±0.1; ripple is 0.1%; response time is 50 μs. **Standard Power, Inc,** 1400 S Village Way, Santa Ana, CA 92705.
Circle 232 on Inquiry Card

HIGH RESOLUTION SHAFT ENCODER



Providing 1M count capacity with 6-decade BCD or 22-bit binary resolution, encoder consists of ruggedized NEMA 12 electromagnetic transducer and solid-state electronic converter connected by six wires. Also available is a 1.1" (2.8 cm) diam transducer. A 1-line instant reset sets all decades or bits to zero; preset control is provided. For BCD units, resolution/turn is 3 decades or 1k counts with total capacity of 1k turns; for binary units, counts/turn is 10 bits with a total of 4096 turns. **Astrosystems, Inc,** 6 Nevada Dr, Lake Success, NY 11040.
Circle 233 on Inquiry Card

VARIABLE DELAY LINE

Minitrim variable delay line, for precise delay adjustments, provides max delays from 10 through 300 ns, attenuation of <0.5 dB, and resolution of <1 ns. Std features include precious metal bifurcated contacts, O-ring seal, stainless steel shaft, epoxy fiberglass case, 2-point terminal embedment, and internal PC board. Units are 0.35" (0.89 cm) high x 0.70" (1.78 cm) wide and either 2.25 or 4.00" (5.7 or 10 cm) long; TD/TR ratios are 4:1 and 7:1, respectively. **Kappa Networks, Inc,** 165 Roosevelt Ave, Carteret, NJ 07008.
Circle 234 on Inquiry Card

What price boredom?

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Because we've reduced prices on our open frame power supplies to an all-time low. Thanks to new manufacturing facilities. The latest engineering advances. And an insane desire to increase our sales.

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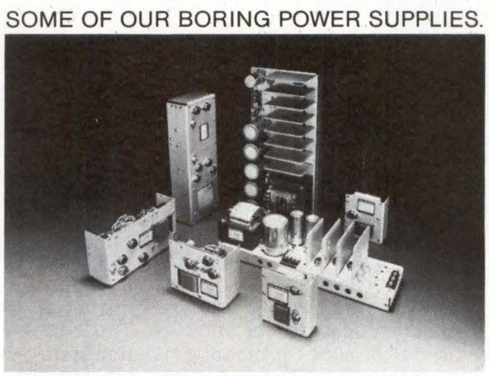
SOME OF OUR BORING POWER SUPPLIES.



acdc electronics

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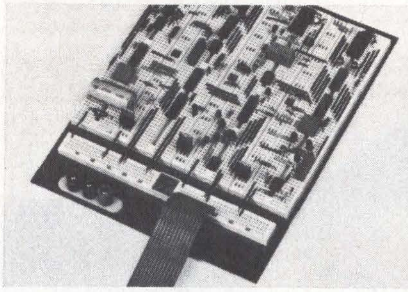
PRODUCTS

MULTILEVEL BREADBOARD



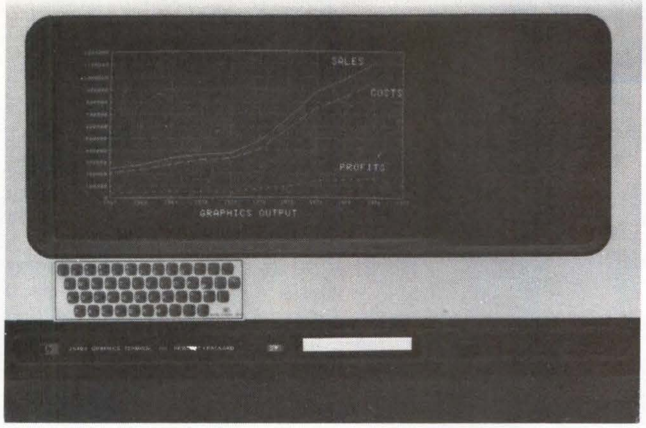
Offering a distribution system consisting of three distribution strips, two levels of PCs, and three front-mounted binding posts, Breadboard II has been expanded to replace the earlier version. With 3208 solderless plug-in tie-points on a universal 0.1 x 0.1" (0.254 x 0.254-cm) matrix, the board accepts all DIPs and components with leads up to 0.032" (0.08 cm) diam. The matrix is comprised of 2776 tie-points while the distribution matrix provides 432. **A P Products, Inc,** 72 Corwin Dr, Box 110, Painesville, OH 44077.
Circle 235 on Inquiry Card

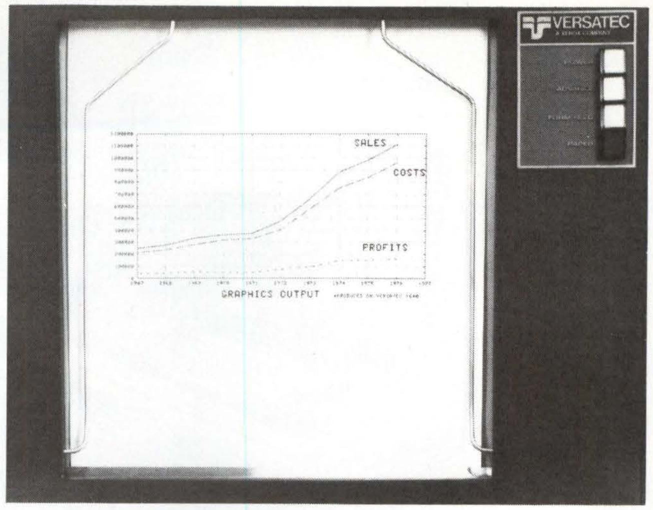
MILITARIZED BACKPANEL SYSTEM

A militarized version of the Fabri[R]-Pak backpanel system for severe environment and high speed applications features "tuning fork" connector patterns, press-fitted into a PC backpanel, and covered with an insulated housing to receive blade-type contacts. It eliminates wirewrapping, provides vibration-resistance, and allows discrete circuitry on the board. Capacitance is provided through ground and power planes. Individual contacts are removable. **National Connector Div, Fabri-Tek Inc,** 9210 Science Ctr Dr, Minneapolis, MN 55428.
Circle 236 on Inquiry Card

LINE CONTROLLER

Remote terminal costs in communications networks are reduced by up to 50% with the terminal line controller model TLC. Designed for IBM, Burroughs, Univac, and Honeywell computer systems, 2740 MOD II protocol emulator permits use of nonintelligent RS-232-C ASCII terminals without modification of host software. The controller provides protocol emulation, buffering, and addressing. Data communications is asynchronous at speeds from 150 to 1800 bits/s. **C. D. Johnson & Associates Ltd,** 56 Sparks St, Suite 100, Ottawa, Ontario K1P 5A9, Canada.
Circle 237 on Inquiry Card





Hewlett-Packard Versatec

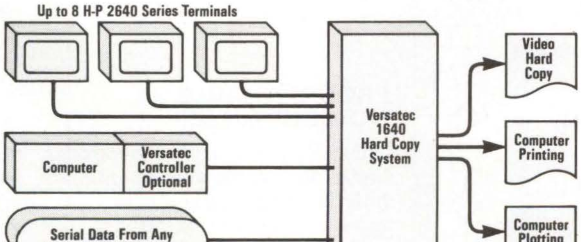
Immortality for two cents.

Now that your HP 2640 series terminal has that picture on-screen, don't lose it. Not when you can immortalize that image for only two cents a copy.

The Versatec 1640 hard copy system is designed specifically for HP terminals. Just plug it in.

One system serves up to eight terminals. It delivers ready-to-use copies in just ten seconds. And most important, it provides the best copy quality at the lowest copy cost.

The best copy lasts. No fade. No deterioration. True archival quality at one-fourth the cost of dry silver paper.



You can store paper at room temperature. Make up to 1000 fanfold copies without a refill, or use an interchangeable continuous roll. Another nice advantage. You can write on this paper in pen or pencil without a slip or a smudge.

Need more justification? Optional controllers let you print and plot directly from any popular computer. Print 1000 LPM or plot three square feet per minute. Then, upon request, make any number of copies from your HP terminals. That's utilization!

Archival quality. Lower cost per copy. And maximum machine utilization. All from the one complete hard copy system for HP display terminals—The Versatec 1640.

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☐ Other displays and video sources ____________ (manufacturer and model)

☐ Send samples

name ____________ telephone ____________

organization ____________

address ____________

city, state & zip ____________

CIRCLE 105 ON INQUIRY CARD

PRODUCTS

SEND/RECEIVE OPTION FOR HIGH SPEED TAPE UNITS

Data communications diagnostics are aided by the send/receive option for the T-511 portable high speed tape unit. All traffic is recorded on both sides of a data link for later replay and analysis. Data recorded on tape by the Datascope D-601 or a tape unit may be transmitted between two high speed tape units equipped with the option; data are sent in simplex operation (not simultaneously). Information on the tape cartridge is read by the tape unit in blocks, and presented to the modem in EIA levels. **Spectron Corp,** 344 New Albany Rd, Moorestown, NJ 08057.
Circle 238 on Inquiry Card

OFFLINE RECORDER

ANSI-compatible cassette recording system model 2146 is a write-only recorder that records offline and plays back directly on Texas Instruments "Silent 700" terminals. Operating at remote sites and times to free up a terminal, it accepts serial data at five selectable rates up to 1200 baud and records in ANSI/ECMA format. It also accepts parallel data. Std Philips cassettes are used and may also be read back on the company's 3765-8 recorder. **Memodyne Corp,** 385 Elliott St, Newton, MA 02164.
Circle 239 on Inquiry Card

PROGRAMMABLE I/O CONTROLLER

PIO4800, a 6-port PIO controller, interfaces the computer to printers, keyboards, or other parallel devices with or without handshaking strobes. It may be operated with or without interrupts, in either isolated I/O or memory-mapped mode. Data transfer is parallel; a single input or output is accomplished by executing one processor instruction. Compatible with the S-100 bus, the 5 x 10" (12.7 x 25.4-cm) PC board contains two channels with three different modes of each channel. **I O R,** Box 28823, Dallas, TX 75228.
Circle 240 on Inquiry Card

PRODUCTS

PUSHBUTTON SWITCH ASSEMBLY

An interlocking/momentary pushbutton switch assembly with master-on control module has applications in the instrumentation and controls market. Engaging the master-on module interlocks all switches, while disengaging reverts the switches to momentary contact mode. Features include lighted or nonlighted assemblies, and multiple switch configurations. Devices are available for use in an interlock assembly with lockout. **Centralab Electronics Div, Globe-Union Inc,** PO Box 858, Hwy 20 W, Fort Dodge, IA 50501.

Circle 241 on Inquiry Card

CONTINUOUS CURVE PLOTTER

The Spectra-Sensor adds plotting capability to ACS-500 or 600 color control systems. Its buffer memory enables it to execute its plot routine while the scanning portion of the ACS system simultaneously measures the next sample. Total time for std and batch measurements is 45 s max. An electrostatic paper hold-down feature facilitates paper changing and accommodates many paper sizes and weights. Plotter is accurate to 0.005" (0.127 cm). **Applied Color Systems, Inc,** PO Box 5800, U.S. Hwy No 1, Princeton, NJ 08540.

Circle 242 on Inquiry Card

TTY AUXILIARY EQUIPMENT ADAPTER

For use with model 33 Teletype[R] terminals, adapter facilitates expansion by providing an auxiliary I/O port which permits disc/tape cassette unit, X-Y plotter, punched card reader, or other auxiliary terminal device to function as an integral part of the teleprinter. Mode of online communications is determined by the external signal line wiring. **United Data Services Co, Inc,** 3024 N 33rd Dr, Phoenix, AZ 85017.

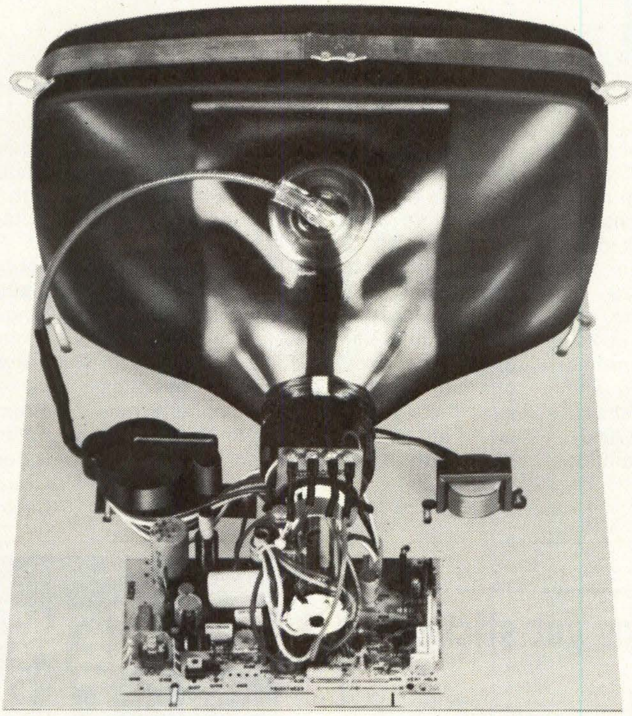
Circle 243 on Inquiry Card

20-MHz DUAL TRACE SCOPE

A 20-MHz dual channel, dual trace oscilloscope, model LBO-508 has a 10-mV/cm sensitivity and features add and subtract modes on CH-1 and CH-2 to facilitate rapid checkout for industrial, laboratory, and service applications. The scope automatically triggers from CH-1 or 2 to eliminate adjusting of trigger level at every setting. It triggers on the smallest signal levels, and has a bright, stable display at all sweep speeds. Rise time is 17.5 ns. **Leader Instruments Corp,** 151 Dupont St, Plain-View, NY 11803.

Circle 244 on Inquiry Card

When you're big on quality but short on space Ball measures up.



Our ready-to-run monitor-pack helps you save dollars as well as room in custom terminal installations.

If you haven't got the room for a full size chassis, or if you just plain insist on adding Ball performance to your own electronics, size up our flexible TVX-Series monitors.

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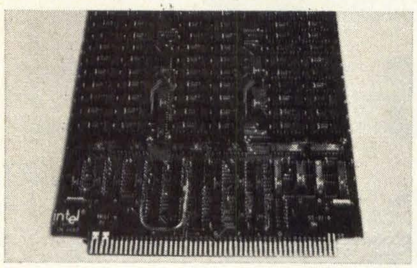
Ball Electronic Display Division

CIRCLE 110 ON INQUIRY CARD

FLEXIBLE, STATIC SEMICONDUCTOR MEMORY



The in-7000 offers from 16k to 256k words of memory capacity and word sizes from 6 to 96 bits. The system uses only a single 5-V power supply, needs no refresh, and comes as a basic card or in a chassis. Available in four 16k configurations—16k x 12, 16, 20, or 24 bits, card may be changed to the corresponding 32k x 6-, 8-, 10-, or 12-bit configuration by merely operating the byte control input line. Read and write cycle times are 250 ns (7000 version), 350 ns (7001), and 500 ns (7002). **Intel Memory Systems,** 1302 N Mathilda Ave, Sunnyvale, CA 94086.
Circle 245 on Inquiry Card

HALL-EFFECT ELECTRONIC SWITCH

Serving as a replacement for mechanical switches for a higher degree of system reliability, the TL170 is a bipolar magnetically-activated electronic switch that uses the Hall effect for sensing a magnetic field. It performs electrical switching with hysteresis. Each circuit, offered in a 3-pin TO-92 SILECT™ plastic package, consists of a silicon Hall sensor, signal conditioning and hysteresis function, and an output stage integrated onto a monolithic chip. **Texas Instruments, Inc,** PO Box 5012, Dallas, TX 75222.
Circle 246 on Inquiry Card

TWX-DDD DATA MODEM

Combining a TWX and DDD modem with touch-tone or rotary dialing, modem interfaces to any 0- to 300-baud data terminal or computer. A 20-mA current loop and RS-232-C interface are std; outputs from both interfaces may be used simultaneously. Active filters, CMOS logic, and MSI ICs are employed in the unit. Also featured is automatic answer on TWX or DDD lines without operator intervention. Device operates over the TWX and DDD telephone network at data rates up to 300 baud. **Westwood Associates, Inc,** Bloomfield, NJ 07003.
Circle 247 on Inquiry Card

MINIATURE DIP SOLID-STATE RELAY

Packaged in a low profile hermetically sealed DIP enclosure, model 682-1 is optically coupled and utilizes thick-film hybrid microcircuit construction. Input voltage range is 3 to 16 Vdc with TTL and HiNIL compatibility. Output rating is 1 A/250 V rms, with synchronous zero voltage turnon to minimize emi. Designed to meet requirements of MIL-R-28750/9, relay has an operating amb temp range of −55 to 110°C. **Teledyne Relays,** 3155 W El Segundo Blvd, Hawthorne, CA 90250.
Circle 248 on Inquiry Card

MINIATURE 100-LED COLUMN DISPLAY

Model MC-100 miniature LED column display consists of a line of 100 LEDs with lit length proportional to the input voltage. The compact unit requires ±5-V power supply and is TTL-compatible. Four terminal pins are voltage input, 5 V, −5 V, and ground. Input range is 0 to 2.5 V for zero to full scale reading. Resolution and accuracy are better than 1%. Unit is free from flicker and resistant to mechanical stresses and vibration. Available color options are red, green, yellow, or infrared. **Digital Components Corp,** 19 Grant St, Linden, NJ 07036.
Circle 249 on Inquiry Card

CIRCLE 111 ON INQUIRY CARD

CIRCLE 112 ON INQUIRY CARD

A software development breakthrough.

FORTRAN compiler and relocatable macro assembler in a new custom software system for micros.

Now it's easier than ever to create smooth running custom software for PCS SuperPac 8080 A-*based microcomputers. And it takes less time, too. With SPDS. The SuperPac development system.

SPDS has resident software you'd expect to find only in minis. Like a FORTRAN compiler option for fast, easy programming in a language your programmers already know (look for BASIC soon). A cross-reference generator that lists constants, labels and addresses and really saves time when you're moving segments around. A relocatable assembler with full macro capability. And an up-down loader for directly loading software into a target system up to 1,000 feet away and calling it back to the development system whenever you need it.

Choose the hardware tools you need. A desk console and dual floppy are standard. From there it's up to you. EPROM programmer, CRT terminal, choice of two line printers and paper tape reader are optional.

SPDS for SuperPac microcomputers. It's a software development breakthrough. From Process Computer Systems, of course. The full service microcomputer manufacturer.

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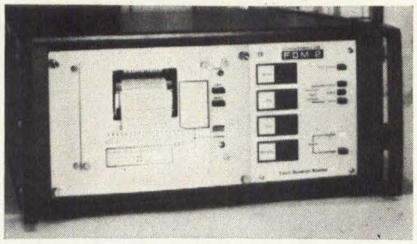
CIRCLE 113 ON INQUIRY CARD

PRODUCTS

POWER LINE DISTURBANCE MONITOR



Model FDM-2 monitors voltage and frequency on single- or 3-phase power lines and prints out exact time and duration of a fault, as well as other information. Features include battery standby, adjustable thresholds, testpoints for oscilloscope display, and alarm. Front panel contains optional digital clock display, nominal line voltage selector, and self-check button. Rear panel contains alarm buzzer, Delta/Wye selection, testpoints, instrument power on-off, and power input connector. **Consultronics Ltd,** 38 Le Page Ct, Downsview, Ontario M3J 1Z9, Canada.
Circle 250 on Inquiry Card

LIGHTED PUSHBUTTON SWITCHES

The A3P series of compact lighted pushbutton switches offers mechanical contacts or solid-state outputs in momentary or alternate action formats. Devices with dimensions of <2" (5 cm) have a service life rated at 5M mechanical operations (min). Interchangeable lens panels permit choice of color. A clear lens cover permits field changes of legends. Solid-state contacts use a Hall-effect IC to produce an output of 50 mA at 5 Vdc in either pulse or continuous operation. **Omron Electronics, Inc, Control Components Div,** 233 S Wacker Dr, Chicago, IL 60606.
Circle 251 on Inquiry Card

ROTARY/PUSHBUTTON SWITCH

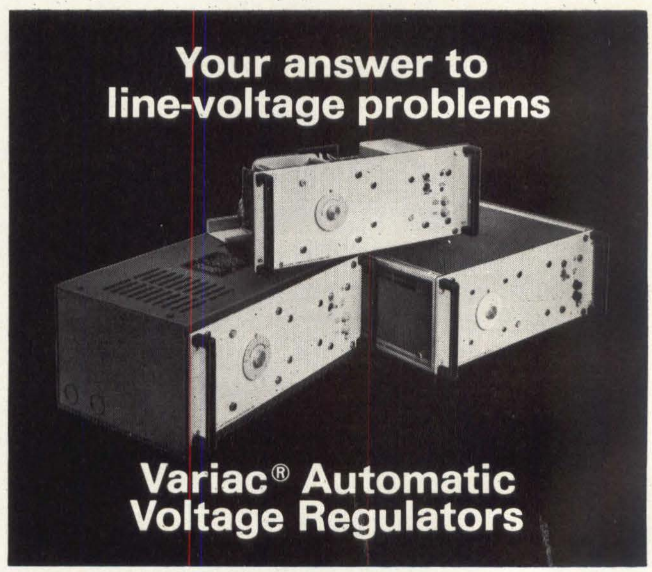
Three Blue Line rotary/pushbutton switches are assembled from modules called "stages," which each contain two isolated double-break silver-alloy, cam operated contacts. The D10 is designed for motor control, instrumentation, and std rated control circuits. Virtually corrosion resistant cross wire contacts of the D11 gear it for dry circuitry down to 30 mV. D12, designed for reliability in low voltage circuits, has a higher interrupting capacity than the D11. **American Solenoid Co, Inc,** 245 E Inman Ave, Rahway, NJ 07060.
Circle 252 on Inquiry Card

BIDIRECTIONAL INTERFACE MODULE

The model 417 bidirectional interface module offers Data General computer users compatibility with instruments operating on the IEEE-488/1975 std digital interface for programmable instrumentation. Occupying one I/O slot in computer or expansion chassis, it communicates with the CPU using std Busy/Done logic. Hardware includes interrupt transfer to and from CPU, 3-wire handshake, and parallel and serial poll. An IEEE-488 cable and software are included. **RBI Systems,** 13123 Valleywood Dr, Wheaton, MD 20906.
Circle 253 on Inquiry Card

PUSHBUTTON THUMBWHEEL SWITCH

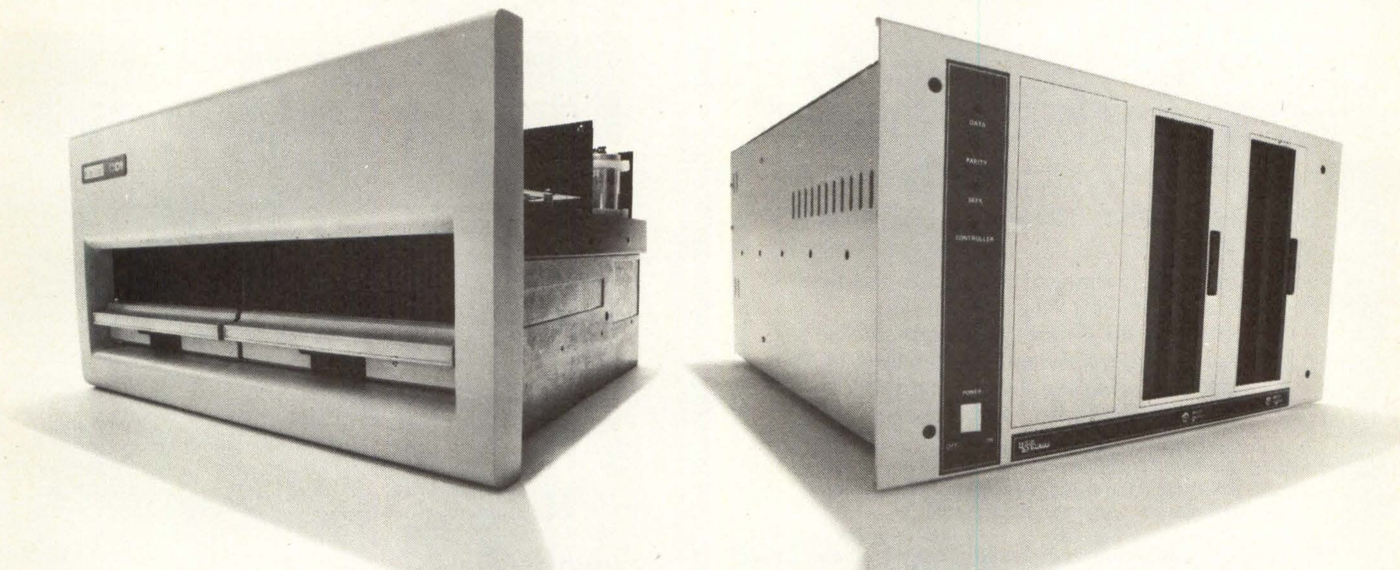
The T56 series bidirectional pushbutton thumbwheel is available in six codes—decimal, BCD, BCD plus complement and 1 common, BCD complement only, BCD with diode provision, and single-pole repeating. Wheel indexing is controlled by two plungers. A transparent plastic window covers the legend opening. Operating force is 400 g, and contact resistance is 0.1 Ω max. It is intended for use in logic level circuits with a rating not to exceed 50 V, 0.1 A. **Cherry Electrical Products Corp,** 3600 Sunset Ave, Waukegan, IL 60085.
Circle 254 on Inquiry Card



Now you have a choice of DEC®-compatible floppy disk systems.

The DEC RX01.
It costs ~~$4,095.~~ $4,300.
You can wait months for it.

The DSD 210.
It costs $3,295.
You can have it in weeks.



YES	PDP®-8, PDP®-11, LSI-11 plug compatible	YES
YES	Software compatible with all DEC operating systems	YES
YES	IBM 3740 Format	YES
NO	Write protect switches	**YES**
YES	Automatic head unload	YES
YES	Ceramic read/write head	YES
YES	Holds 256,256 bytes per diskette	YES
NO	Diskette formatting capability	**YES**
1 OR 2	Drives per controller	**1, 2, OR 3**
NO	Interchangeable 50/60 Hz operation	**YES**
YES	Digital phase-lock-loop data separation circuit	YES
NO	Front panel activity LED lights	**YES**
NO	Front panel system status indicators	**YES**
PARTIAL	Modular construction	**COMPLETE**
MINIMAL	Self-testing microcode	**EXTENSIVE**
NO	Field-proven Shugart drives	**YES**

Our DSD 210 floppy disk system is 100% hardware, instruction set, and media compatible with all DEC PDP-8, PDP-11 and LSI-11 systems. It costs $1,000 less than DEC's RX01, has a far shorter delivery time, and has more useful features.

Data Systems

For an expanded comparison and complete technical details, phone or write Data Systems Design, Inc., 3130 Coronado Drive, Santa Clara, CA 95051, 408/249-9353.

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COURSE 111: One Day—MONDAY

Microprocessor Project Management

From design through manufacture, QA and field service

MICROPROCESSORS: HOW CAN YOU GO WRONG???
WHAT ABOUT . . . ?

Underestimating software costs and time?
Inadequate software documentation?
Selecting the wrong microprocessor?
Software development equipment($14000!)?
Manufacturing problems? Hardware/software testing? Reliability? Obsolescence? . . .

A microprocessor project is different from anything you've managed before. This one efficient day of organized, expert guidance will save you literally months of wasted time, re-invented wheels, and costly oversights.

This unique course synthesizes the experience of hundreds of project managers (who learned the hard way) into a practical field-proven methodology for managing all phases of a microprocessor application. The course emphasizes high-risk, high-cost and time-critical problems unique to microprocessors. Concrete real-world case studies illustrate the methods presented, and these step-by-step methods can be immediately applied to your own project.

This course will benefit every manager and engineer concerned with microprocessors. Teams from engineering, manufacturing, QA, and field service are encouraged to attend (team discounts available).

KEY TOPICS

1. **Fundamental concepts, definitions and jargon.**
2. **Avoiding pitfalls and "technical tunnel-vision."**
3. **Planning and specifying the project — the PERT/flowchart.**
4. **How to select personnel and evaluate performance.**
5. **How to select the right microprocessor — what's really important?**
6. **Software development and test equipment — what's really needed?**
7. **How to estimate overall project costs and schedule.**
8. **How to manage software design and development.**
9. **Software documentation — a practical methodology.**
10. **Verifying that the software works.**
11. **Manufacturing, testing and QA — both software and hardware.**
12. **Component & product reliability — planning μP field service.**
13. **How to prepare for the future today . . . and avoid obsolescence tomorrow.**

SPECIAL LATE-AFTERNOON WORKSHOP
A unique opportunity to discuss your application-oriented problems in a productive shirtsleeves atmosphere. Immediately after Course 111 from 4:30 until 6:00pm with snacks and refreshments.

COURSE 102s: One Day—TUESDAY

Microprocessors and Microcomputers:

A Comprehensive Technical Introduction and Survey

This course provides a comprehensive unbiased introduction to microcomputer hardware/software development and integration. The course emphasizes the factors affecting key design and development decisions including: processor selection, I/O and software design, software implementation steps, development and test equipment, and most important pitfalls to be avoided when getting started. Throughout the course, applications examples provide concrete illustrations of concepts presented and are drawn from the following application areas: military, communications, consumer, instrumentation, industrial control, and biomedical systems.

This course is *vital* (1) to all engineers and managers who want a quick, unbiased, cost-effective introduction to microprocessors (2) to those engineers attending this as the first day of the "Engineering Design" series (Course 102s, 125A and 136) and (3) to managers attending this course as the second day of "Project Management" series (Course 111 and 102s).

COURSE OUTLINE

1. **INTRODUCTION**
   • What is a microprocessor (μp)? a microcomputer (μc)? • Identifying suitable and unsuitable applications
2. **FUNDAMENTAL MICROCOMPUTER CONCEPTS**
   • Terminology • Software (SW) — how it works; how it's develope • Hardware (HW) — Basic μc configurations • The μc design cycl
3. **THE HARDWARE**
   • μp architectures (4, 8, 16-Bit and slices) • Memory systems design — ROM, PROM, RAM, CORE • Input/output organization (programmable I/O, interrupts, DMA) • Build or buy?
4. **INTERFACING TO THE EXTERNAL WORLD**
   • I/O port design • Programmable LSI I/O chips • Interfacing to: analog devices, keyboards, displays, cassettes, etc.
5. **SOFTWARE DESIGN & IMPLEMENTATION**
   • Four implementation methods • Editors, assemblers, compilers • Assembly vs. high level languages (FORTRAN, BASIC, PL/M)
6. **INTEGRATING AND TESTING THE HW AND SW**
   • What really useful tools are available? • What tools should you build yourself? • Isolating and fixing HW and SW bugs
7. **TECHNICAL SURVEY OF μP'S AND μC'S**
   • Intel, Fairchild, Motorola, National, Rockwell, Signetics, Texas Instruments, Zilog, and others including the new LSI minicomputers • Board-level μc systems — PROLOG, PCS, CONTROL LOGIC, WARNER/SWASEY, and others
   • A systematic, application-oriented approach to selecting the right microprocessor family.
8. **UTILIZING DEVELOPMENT AND TEST EQUIPMENT**
   • Logic analyzers • SW simulators • Specialized μc debugging equipment • μc development systems • Peripherals to buy
9. **HOW TO GET STARTED**
   • What equipment to buy first • Pitfalls to avoid • Good information sources

R EDUCATION

)	DENVER February 13-17	BOSTON March 6-10

Design Series

COURSE 125A: Two Days — WEDNESDAY & THURSDAY

Hands-On Microcomputer Programming Workshop (for the beginner)

LEARN-BY-DOING
EACH STUDENT RECEIVES A COMPLETE 8080 MICROCOMPUTER SYSTEM FOR HIS PERSONAL USE THROUGHOUT THE COURSE.

This highly efficient, intensive short-course combines expert teachers and detailed course materials with unique opportunity to learn by *immediately* implementing on *your personal microcomputer* each new programming concept as it is developed by the instructor.

COURSE OUTLINE [with exercises in brackets]

1. **INTRODUCTION TO THE ICS 8080 μC TRAINING SYSTEM**
   • Hardware configuration • How to use the keyboard/display and built-in commands • [Loading and executing a simple program]
2. **SOFTWARE FUNDAMENTALS AND BASIC TECHNIQUES**
   • CPU Register Instructions [Counting] • Memory Instructions [Storing & Retrieving Data] • Basic I/O [Controlling LED segments] • Jumps and Loops [Time delay program] • Bit Testing [Binary Decoding] • Subroutines & Stacks [Keyboard Input]
3. **ADVANCED PROGRAMMING TECHNIQUES**
   • Arithmetic [A multi-precision calculator] • Data Organization [Table Look-up] • Block I/O Transfers [Real-Time I/O] • Controller Programs [Traffic Control]
4. **PROGRAM DESIGN METHODOLOGY**
   • Systems analysis • Specifying the program • Design approaches (top-down, structured programming, modular design)

OPTIONS: KEEP THE MICROCOMPUTER SYSTEM
Course 125B: Includes 125A PLUS attendee receives a microcomputer & a 650-page Self-Study Text to take home.
Course 125C: Includes 125A PLUS microcomputer to take home.

COURSE 136: One Day — FRIDAY

NEW! NEW! NEW!

Hands-On Interfacing Workshop

(Limited to current or former attendees of Course 125.)

Utilizing the ICS training microcomputers and additional Interfacing hardware, students will learn both software and hardware for interfacing to the real-world.

In-Class Projects include:
1. Real-Time Interrupt programming (w/Intel 8253 timer)
2. A/D Conversion — A Digital Thermometer
3. DC Motor Control (Open and closed loop)
4. Other (student-option) Interfacing projects

CIRCLE 117 ON INQUIRY CARD

COURSE ENROLLMENT FORM

COURSE HOURS:
Registration: 8:15am
Course Lecture: 9:00am—4:30pm
Special Events: 4:30—6:00pm

In addition to the extensive hands-on exercises of Course 125A and 136, informal microcomputer hardware activities are organized at every course for valuable hands-on experience.

COURSE FEE:
Management Series: (2 days: 111 + 102s)—**$390**
3-day Design Series: (102s + 125A)—**$495***
4-day Design Series: (102s + 125A + 136)—**$595***
Complete Series: (111 + 102s + 125A + 136)—**$695***
Individual Courses: 111 or 102s or 136 —**$195**; 125A—**$395***
*Option 125B—add **$445**; Option 125C—add **$350**

Course Fee Includes: lectures, lecture-coordinated notes, extensive reference materials, luncheon & coffee breaks.
Team/Group Discounts: 10% reduction for three or more participants from the same organization, if invoiced at the same time.

TO ENROLL:
Please fill out, detach and return coupon. A confirmation with complete course details will be forwarded to you.

MAIL TO: **Integrated Computer Systems, Inc.
4445 Overland Avenue
P.O. Box 2368
Culver City, California 90230**

For immediate confirmation, CALL: **(213) 559-9265**

☐ PLEASE ENROLL ME in the following courses:

2 Day Project Management Series (111, 102s) — 3 or 4 Day Engineering Design Series (102s, 125A, 136)

COURSE	111	102s	125A	136
CHICAGO	☐ Dec 5	☐ Dec 6	☐ Dec 7-8	☐ Dec 9
WASHINGTON D.C.	☐ Dec 12	☐ Dec 13	☐ Dec 14-15	☐ Dec 16
LOS ANGELES	☐ Jan 16	☐ Jan 17	☐ Jan 18-19	☐ Jan 20
HOUSTON	☐ Jan 23	☐ Jan 24	☐ Jan 25-26	☐ Jan 27
DETROIT	☐ Feb 6	☐ Feb 7	☐ Feb 8-9	☐ Feb 10
DENVER	☐ Feb 13	☐ Feb 14	☐ Feb 15-16	☐ Feb 17
BOSTON	☐ March 6	☐ March 7	☐ March 8-9	☐ March 10

NAME ____________________
JOB TITLE ____________________
COMPANY ____________________
MAILSTOP ____________________
ADDRESS ____________________
CITY ____________________
STATE ____________ ZIP CODE ________
TELEPHONE (____) ____________ Ext ________

PAYMENT: Please indicate method of payment.
☐ Check/M.O. enclosed ☐ P.O. included ☐ Please invoice me

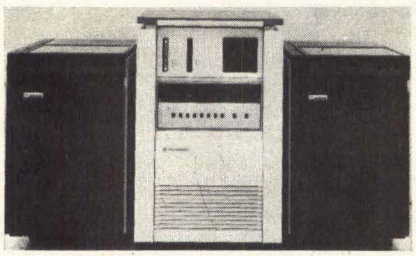
☐ Please put me on your mailing list to receive future Course Schedules.
☐ Please send information on ICS Self-Study Courses.
☐ Please contact me with regard to On-Site Courses.

PRODUCTS

STATIC ELIMINATOR BRUSH

Static charges which build up as a result of paper movement in a computer printer are controlled and eliminated by the static eliminator brush. The self-energized, induction-type device collects all static charges and bleeds them directly to ground to prevent static-caused paperjams. It does not have to be renewed, poses no health hazard for personnel, and is mechanically safe as it cannot damage the computer or moving paper. **Texwipe Co,** Hillsdale, NJ 07642.
Circle 255 on Inquiry Card

DISC AND MAG TAPE CARTRIDGE DRIVES



First of two components for model 4000 series interactive timesharing systems, the 4460 disc drive replaces the 7.5M-byte drive previously incorporated in the 4000/15 and provides 10M bytes of nonremovable formatted storage. The 4560 mag tape cartridge drive provides 10M bytes of storage on a compact 3M-type cartridge, using a recording density of 6400 bits/in. Cartridge drive allows programmatic backup of disc data to tape, and recovery of tape data to disc unit. **Basic Timesharing Inc,** 870 W Maude Ave, Sunnyvale, CA 94086.
Circle 256 on Inquiry Card

BELL-COMPATIBLE ACOUSTIC COUPLER/MODEM

AJ 1245, a Bell-compatible 103 and 202 mode coupler and modem in one unit, is designed to optimize the transfer of low and medium speed data over normal voice grade telephone lines using an ordinary telephone handset. It interfaces with any EIA terminal and communicates acoustically at 0 to 450 baud in 103 mode and 0 to 1200 baud in 202 mode. The coupler automatically adjusts baud rate and interface protocol so that the user may switch select between these two modes. **Anderson Jacobson, Inc,** 521 Charcot Ave, San Jose, CA 95131.
Circle 257 on Inquiry Card

I/O BUS INTERFACE LINE PRINTER CONTROLLER

Capable of driving three printers simultaneously, the S-10 controller is designed for DECsystem-10 to operate with printers from 600 to 1500 lines/min. The 5.25" (13.34-cm) high unit can be installed in unused space in the computer. No special programming is necessary. Compatible with KA, KI, and KL processors, the controller is also software compatible with all operating systems. Power supply, mounting brackets, printer cables, and operations and maintenance guide are included. **Southern Systems, Inc,** Fort Lauderdale, FL 33308.
Circle 258 on Inquiry Card

1⅛" DIAMETER FAN

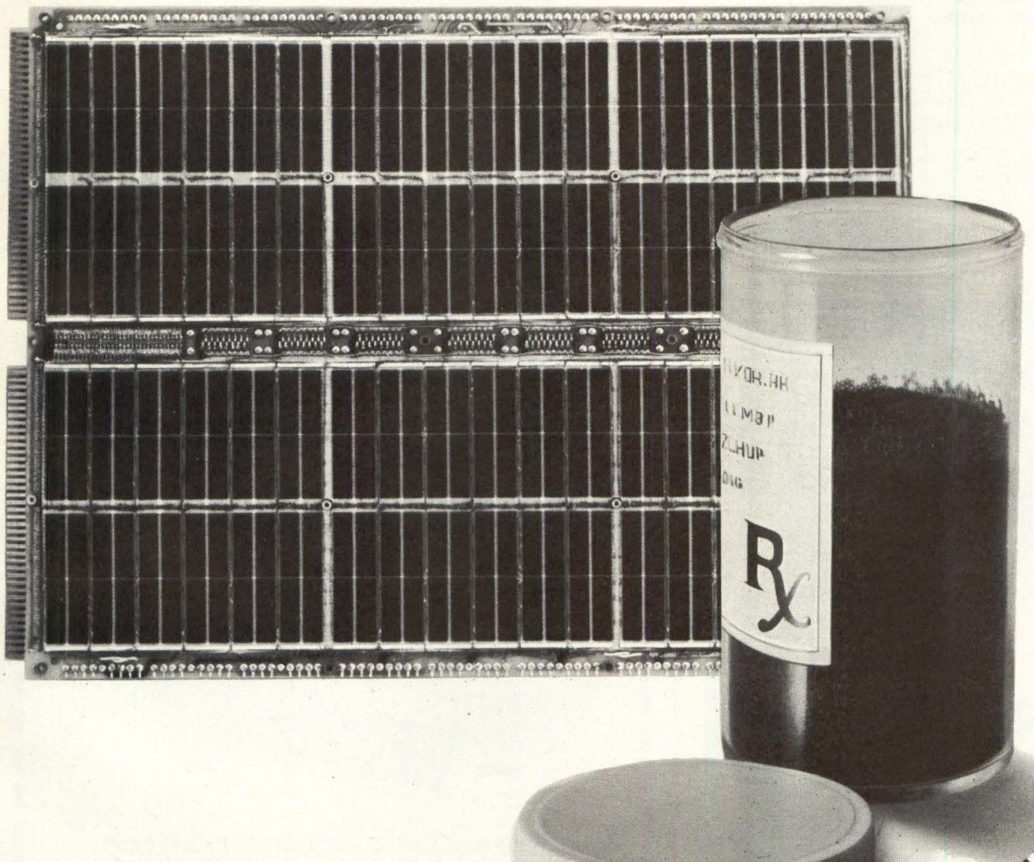
Minimax™ 9-frame cooling fan for high density electronic packages measures 1.125" (28.57 mm) diam and approx 1.5" (38.1 mm) thick, with a capacity of 12 ft^3/min (0.34 m^3/min) at free delivery. Impeller and correctional vanes are of airfoil construction for max aerodynamic efficiency and min noise level. It is applicable to small air moving devices capable of delivering required air flows at high back pressures. It operates in amb temps from −55 to 100°C. **Rotron, Inc, an EG&G Co, Custom Products Div,** Woodstock, NY 12498.
Circle 259 on Inquiry Card

Suffering from temporary loss of memory?

Try the Fabri-Tek core remedy.

If you're like some people who've been on a straight semiconductor memory diet, you've probably been experiencing severe complications. Loss of memory when power is removed. "Soft" random errors that can't be diagnosed. Temperature sensitivity. Added cost and complexity of error detection and correction schemes and battery back up.

For no added cost, core memories provide greater reliability, maintainability, non-volatility and 20 years of proven technology. They're relied upon in process control and a lot of other demanding applications where a failure could be catastrophic. Take our Model 698: 64K bytes of 650 nsec cycle time and 250 nsec access time. You can build a system up to 512K bytes. (Micro 3000 compatible, too). Maybe its time you kicked the semiconductor habit. We're ready to help.



FABRI-TEK INC.
COMPUTER SYSTEMS

5901 South County Road 18 • Minneapolis, MN 55436 • (612) 935-8811

Boston, MA (617) 969-5077	Hawthorne, CA (213) 973-0484	Dallas, TX (214) 234-8438	United Kingdom Maidenhead 37321-4
Chicago, IL (312) 437-4116	San Jose, CA (408) 246-8391	Houston, TX (713) 467-4373	

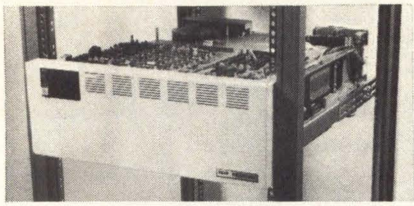
TELL ME MORE

☐ Model 698-32K X18 System ☐ Model 696-16K X18 System
☐ Bulk Core Systems ☐ 30-90 day requirement ☐ Future requirement
☐ Special memory needs ☐ Have salesman call ☐ Send literature

Name and Title
Company
Address
City, State, Zip
Phone

PRODUCTS

SMALL COMPUTER HARD DISC



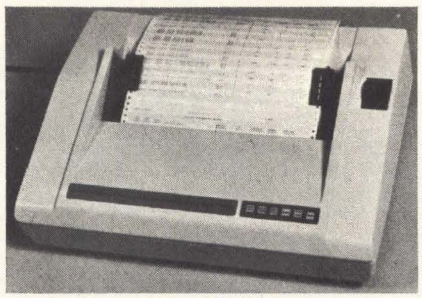
A hard disc for small computers, the C-D74 provides a 35-ms avg access time to any of 74M bytes of information. With 12 tracks on a cylinder without reseeking, the disc can access any of 220k bytes of information in 5 ms. Winchester technology allows the drive to run 24 h/day without disc wear. Unit has a 10-ms single-track seek and data transfer rate of 7.3M bits/s. A nonremovable, sealed chamber drive features a rotary arm positioner. **Ohio Scientific,** Hiram, OH 44234.
Circle 260 on Inquiry Card

TIME DIVISION MULTIPLEXER

A bit-leaved time division multiplexer meets requirements of both national and international Telex, as well as national data networks. For Telex operations, the B101 provides typ configurations of 46 channels operating at 50 to 300 baud. A universal card interfaces with terminals or Telex exchanges, using any char code. It can handle three independent high speed lines, and provides aggregate rates from 1.2k to 9.6k bits/s. In data networks, the unit operates as fast as 64k bits/s over the three independent lines. **Timeplex, Inc,** 100 Commerce Way, Hackensack, NJ 07601.
Circle 261 on Inquiry Card

INTELLIGENT MULTIPURPOSE PRINTER

For applications requiring both printing and computing capabilities, the IPS-7200[R] microcomputer-based intelligent printing system generates variable-sized



char without requiring host computer programming. It can function as a label printer, general-purpose output printer, or programmable microcomputer. Combining a 120-char/s serial printer and 8-bit microcomputer system, the unit includes an RS-232-C asynchronous communications interface; a 20-mA current loop interface is optional. **Dataroyal, Inc,** 235 Main Dunstable Rd, Nashua, NH 03060.
Circle 262 on Inquiry Card

WIREWRAPPABLE INTERFACE BOARDS

Series CIP4 and CIP4/11 wirewrappable boards for interfacing with DEC LSI-11 microprocessor and PDP-8/11 minicomputers plug directly into, and are bus-compatible with, std DEC Omnibus and Q-Bus systems. Boards provide 32 col of 60 low profile socket terminals/col, with alternate rows of committed ground and voltage wirewrappable terminals. Up to 110 16-position IC chips or an equivalent mix of 14-, 16-, 18-, 22-, 24-, 28-, 36-, or 40-position IC chips are accommodated. Boards are available in dual, quad, and hex sizes. **Garry Manufacturing Co,** 1010 Jersey Ave, New Brunswick, NJ 08902.
Circle 263 on Inquiry Card

 CIRCLE 122 ON INQUIRY CARD

CIRCLE 123 ON INQUIRY CARD

Our first SBC 80 compatible systems for 1977!

Visit us in Booth 121-123, Mini/Micro 77 December 6-8, Anaheim, CA

4K to 64K RAM Up to 8K EPROM on one board

Now you can have RAM and EPROM on the same board and buy as much or as little memory as you need. And because our memories use 16 pin memory element sockets you can change your memory when you change your mind.

Speaking of changing your mind, when you want to change address locations of either RAM or EPROM, it's done with two, on-board switches—providing 16 possible start locations for each memory.

Compare these features with our much improved read, write and refresh cycle times and you'll choose MSC first.

16K RAM Version

Up to 16K × 8 of RAM and up to 8K × 8 of EPROM on the same board.

RAM expandable in 4K × 8 increments and EPROM expandable in 1K × 8 or 2K × 8 increments.

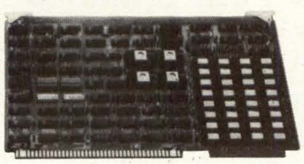
On-board DIP switches to select any of 16 address start locations for RAM and 16 address start locations for EPROM.

Cycle times:
Read, 350 nsec.
Write, 500 nsec.
Refresh, 500 nsec.

Totally SBC 80 and Intellec MDS hardware and software compatible.

Limited one year warranty on parts and labor.

Delivery 30 days ARO.



MSC 4602

64K RAM Version

Up to 64K × 8 of RAM and up to 8K × 8 of EPROM on the same board.

RAM expandable in 16K × 8 increments and EPROM expandable in 1K × 8 or 2K × 8 increments.

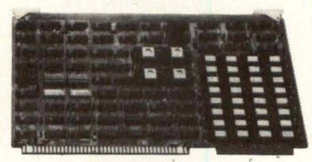
On-board DIP switches to select any of 16 address start locations for RAM and 16 address start locations for EPROM.

Cycle times:
Read, 350 nsec.
Write, 500 nsec.
Refresh, 500 nsec.

Totally SBC 80 and Intellec MDS hardware and software compatible.

Limited one year warranty on parts and labor.

Delivery 30 days ARO.



MSC 4502

Beginning firsts

Beginning with compatible memories, Monolithic Systems will continue to introduce SBC 80 systems with features which are firsts.

First to take advantage of the latest technology. And first in reliability, value and delivery.

You can be among the first, when you call us for SBC 80 compatible systems.

SBC 80 compatible systems... from the first.

Monolithic Systems corp.

14 Inverness Drive East
Englewood, CO 80110
303/770-7400

Intellec is a registered trademark of Intel Corporation.

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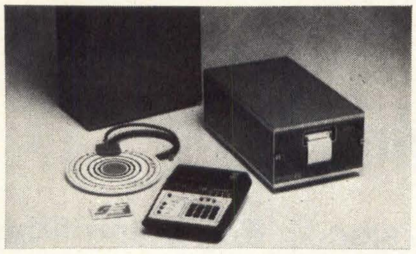
PRODUCTS

PROXIMITY-OPERATED ACCESS CONTROL SYSTEM



Model 414 operates by proximity; credit-card-sized command key cards activate access doors when held within 4" (10 cm) of a concealed sensor. The system controls access for up to eight locations; it includes electronic control unit, sensors, system programmer, command keys, and optional printer. Program unit has memory capacity for more than 1000 individual key codes. System can be reprogrammed to prevent use of lost key card. System printer can log all accesses. **Schlage Electronics,** 1135 E Arques Ave, Sunnyvale, CA 94086.
Circle 264 on Inquiry Card

THUMBWHEEL SWITCHES

Suited to programming of data processing, numerical machine control, and manufacturing process control systems requiring readily-altered digital input information, the Metal-Mite thumbwheel switches feature one to 20 stations; 8-, 10-, 12-, and 16-position modules; and large, easy-to-read thumbwheel nomenclature. Typ codes offered are decimal, BCD, octal, BCO, and hexadecimal. Four types of rear mounting are switch modules only, without bezel, with bezel, and with escutcheon. **Switchcraft, Inc,** 5555 N Elston Ave, Chicago, IL 60630.
Circle 265 on Inquiry Card

REAL-TIME DIGITAL LOGIC ANALYZER

Model RK 778 8-channel logic timing display works with any triggered oscilloscope to catch and display on all channels pos or neg going glitches <13 ns. Glitch width display control is adjustable. Eight channels of input are sampled by internal adjustable or external clock. It can be used in an alternate mode self-triggered. Features include 8-channel combinatorial trigger for jitter-free display, Schottky buffered inputs, and regulated supply. **Kenmark Development Group, Inc,** 6 Meadowlark Dr, East Northport, NY 11731.
Circle 266 on Inquiry Card

BASIC I/O DRIVER

I/O driver controls up to four cassette recorders, allowing BASIC programs to read records from and write records to cassette tape under program control. Patched to/from BASIC, the driver handles all I/O to either cassette operating system or console. The controller, which plugs into a single Tarbell interface board, is available as a 4- or 2-port kit. Software includes cassette operating system, BASIC I/O driver and listing, and assembler with patches to assemble large programs from tape. **Ro-Che Systems,** 7101 Mammoth Ave, Van Nuys, CA 91405.
Circle 267 on Inquiry Card

DC RECORDER WITH EDGE PRINTER

For use in portable systems to be powered from 12 Vdc and for systems where electronic isolation from line power is required, the M1-50 DCM recorder module has a 50-mm chart width, power consumption of <8 W, and four chart speeds of 5, 10, 25, and 50 mm/s std. Frequency response is dc to 110 Hz at 10 mm pk-pk. It is available as a mechanical recorder or with electronics, and can be equipped with optional alphanumeric edge printer with a 5 x 7 dot matrix. **MFE,** Keewaydin Dr, Salem, NH 03079.
Circle 268 on Inquiry Card

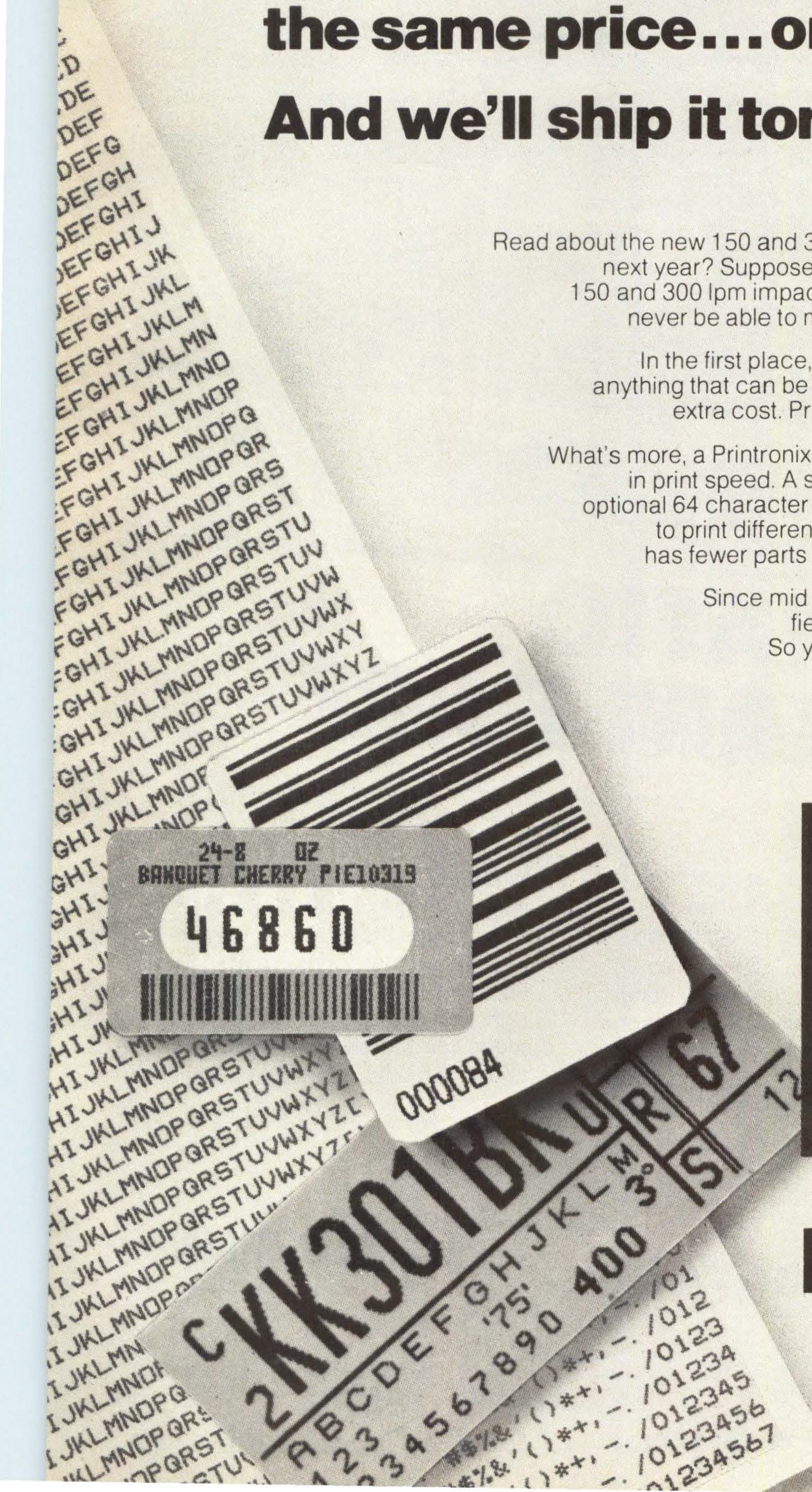
CIRCLE 126 ON INQUIRY CARD

CIRCLE 127 ON INQUIRY CARD

If you wait until 1978, you'll see some new 150 and 300 lpm band printers.

If you order a field-proven Printronix impact matrix line printer today, you'll get unbeatable print quality plus full plotting capability for the same price...or less.

And we'll ship it tomorrow.



Read about the new 150 and 300 lpm band printers scheduled for delivery sometime next year? Supposedly, they'll be in the same low price range as Printronix 150 and 300 lpm impact matrix line printers. But good as they might be, they'll never be able to match the utility and value of Printronix Printer/Plotters.

In the first place, you can't plot with a band printer. A Printronix can plot anything that can be displayed on a CRT. You get this extra capability at no extra cost. Printing and plotting for the same price as a band printer.

What's more, a Printronix gives you a 160 character capacity with no slowdown in print speed. A standard 96 character ASCII set plus your choice of an optional 64 character computer selectable set. No time lost changing bands to print different languages or character styles. And since a Printronix has fewer parts than a band printer, you can count on higher reliability.

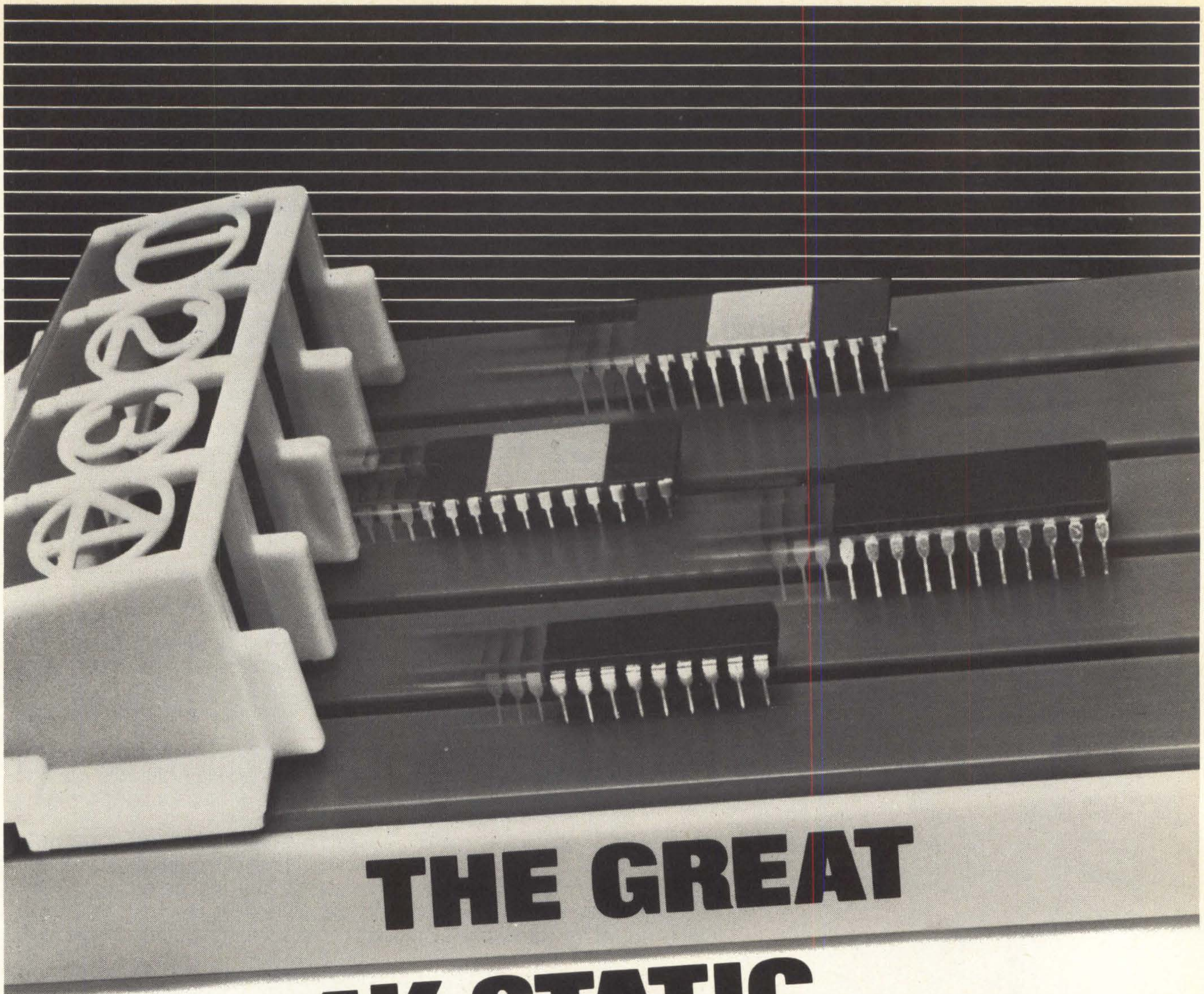
Since mid 1975, we have shipped more than 3,000 units. They're field proven. And we are tripling our production capacity. So you won't have to wait 6 to 9 months to get the best buy in printers. Order one today and we'll ship it tomorrow!

Printronix, Inc., 17421 Derian, Irvine, California 92714
Call us at (714) 549-8272

CIRCLE 128 ON INQUIRY CARD

PRINTRONIX...

Your chance to beat the band.



THE GREAT 4K STATIC RAM RACE

In a world of claims and counter-claims, one thing is clear. EMM SEMI is still in the lead. Of course, we not only had a healthy head start, but we field a whole family of 4K static RAMs.

We *delivered* the industry's first 4K static RAM in 1975, a full year and a half before anyone else. We are now delivering 7 basic static RAM types with many versions of each, and producing them at a greater monthly rate than our nearest competitors combined.

By now we have more 4K static RAMs operating in a wider range of customer equipment than anyone else in the semiconductor memory business — from 10 Megabyte IBM add-on memory systems to hobbyist microprocessor kits.

Whatever your application, from mass storage to telecommunications, from medical electronics to toys and games, chances are there's an EMM SEMI static RAM just right for you. Please call or write today for full details — and ask about our byte oriented RAMs, too.

Memory at work **EMM SEMI, Inc.**

a subsidiary of Electronic Memories & Magnetics Corporation • 3883 N. 28th Avenue, Phoenix, Arizona 85107 • (602) 263-0202

AUTOMATIC µP-BASED RLC TESTER

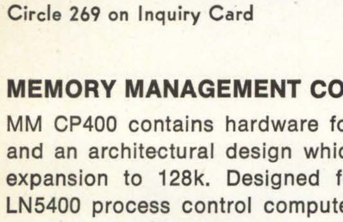
An automatic impedance component tester with keyboard control and internal microprocessor, the 1658 Digibridge™ measures R, L, C, D, and Q of resistors, capacitors, coils, and other components at a selectable frequency of 1 kHz or 120 Hz. Basic accuracy is 0.1%. No calibration is required. Ten limit comparison bins are available for sorting; either symmetrical or asymmetrical limits can be entered through the keyboard. Three different test speeds up to 7 measurements/s are selectable. Test modes are continuous for repetitive measurements, single, and average. Providing a running average of 10 successive measurements, average mode smooths noise or slight variations due to unstable components from one measurement to another. **GenRad, Inc,** 300 Baker Ave, Concord, MA 01742.
Circle 269 on Inquiry Card

MEMORY MANAGEMENT CONTROL PROCESSOR

MM CP400 contains hardware for dynamic memory mapping and an architectural design which offers convenient memory expansion to 128k. Designed for use with the company's LN5400 process control computer systems, the equipment is based on the the CP400 control processor. Features include dual processing units, CPU and IOP; control storage to support high speed operation of CPU and IOP; modular architecture; general-purpose registers, real-time clocks, and direct I/O interface; and programmer's control panel. The IOP processor's high data transfer rate permits large quantities of data to be processed and transmitted without taking time away from real-time control. **Leeds & Northrup Co, Systems Group,** Dickerson Rd, North Wales, PA 19454.
Circle 270 on Inquiry Card

MINI/MICROCOMPUTER STANDALONE PRINTER

Suited for terminal applications or as standalone printers, DP-1000 series digital printers feature a dot-matrix impact printing element capable of producing 64 alphanumeric and special symbols in 40-char lines at 1.25 lines/s on std single or multiple-copy paper rolls. Three basic ASCII configurations, conforming generally to EIA RS-232-C, allow interfacing to most minicomputers, modems, and the current drive mode of Teletype® printers. Std baud rates from 110 to 2400 are available. All models have internal storage. Single or double-width characters may be selected via an external control line, allowing either 6 or 12 char/in (2.4 or 4.7/cm) to be intermixed on a line. **Anadex,** 9825 DeSoto Ave, Chatsworth, CA 91311.



Circle 271 on Inquiry Card

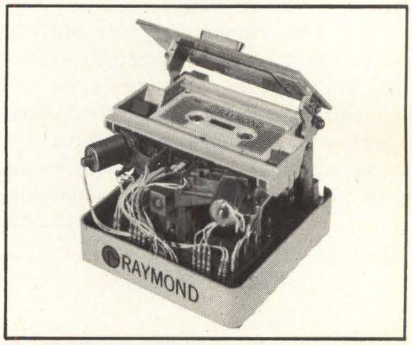
Raymond

will ship over 10,000 small digital tape drives this year. To more than 100 customers!

We manufacture:

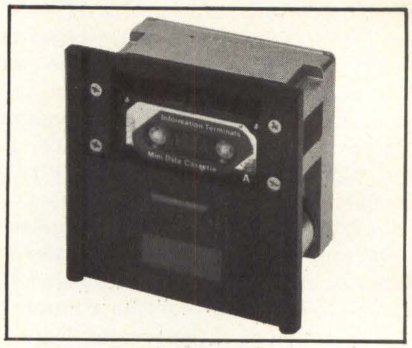
Model 6406 Raycorder

for Philips cassettes — the industry standard for more than 6 years.



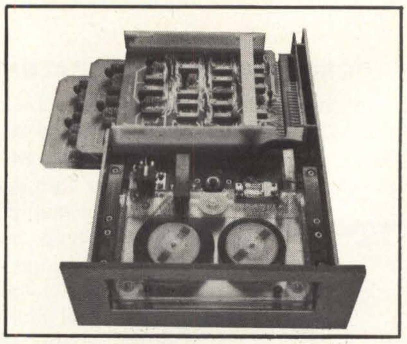
Model 6409 Mini-Raycorder

for ANSI X3B5/77-22 Mini-Data cassettes — the first in the industry. Now added features make it even better — the runaway leader in its class.



Model 6413 Cartridge Raycorder

for $\frac{1}{4}$-inch data cartridges. A new offering this year from Raymond — a new package with a proven track record.



Shouldn't you be buying the best? From the small tape drive experts —

Raycorder Products Division
Raymond Engineering Inc.
217 Smith Street, Middletown, Connecticut 06457, (203) 632-1000
a subsidiary of Raymond Precision Industries

PRODUCTS

POCKET-SIZED PROGRAMMABLE CALCULATOR WITH BUILT-IN PRINTER

Keystroke programmable HP-19C features 98 fully merged program steps, continuous memory, full editing and programming functions, 30 data storage registers, and a quiet thermal printer. Editing and programming functions include backstep, insert/delete, single step, pause, and a total of 10 decision tests. The printer records the contents of program memory, data storage, and operational registers; and is useful in program debugging. User may select from three operating modes—manual: printer operates only when print x key or list function is operated; normal: all entered data and functions are recorded; and trace: step number, function, each step of executing program, and results of manual calculation are printed. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304.

Circle 272 on Inquiry Card

10-CHANNEL PROBE POD LOGIC ANALYZER ACCESSORY

A high performance active probe pod which detects combinational triggers from up to 36 signals when used with the company's logic analyzers, the 10-TC is particularly useful for troubleshooting microprocessor-based circuits. Ultraminiature clips can be connected to IC pins without the need for DIP clips; leads between pod and clips are light, flexible, and color-coded. By connecting the pod between analyzer and circuit, high input impedance, combinational trigger with qualifiers, clock qualifying, and independent threshold detection are combined. Power is provided by the analyzer. Device may be used to form a convenient signal interface or to expand combinational trigger capability up to 36 channels. **Biomation,** 10411 Bubb Rd, Cupertino, CA 95014.

Circle 273 on Inquiry Card

FULL FEATURE PROGRAMMABLE CONTROLLER

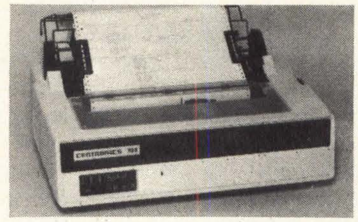
The 484 includes typical capabilities of relay logic, timing, and counting, and provides 1.0-, 0.1-, and 0.01-s time base timers. Other features are full arithmetic capability (including add, subtract, multiply/divide), internal coils, 16-bit binary registers, ability to generate reports to hierarchical computers, and two built-in 128-step sequencers which enable the unit to be used where drum-type programmers or stepping switches have previously been used. I/O expansion is possible in increments of four points from 8 to 512 I/O points. The expanded version has a memory capacity of 4096 words. The controller's 5" CRT multinode panel can display up to 77 circuit contacts at a time; up to seven complete ladder diagram rungs can be shown at once. **Gould Inc, Modicon Div,** PO Box 83, SVS, Andover, MA 01810.

Circle 274 on Inquiry Card

PRODUCTS

120-CHAR/S SERIAL DOT MATRIX PRINTER

A 132-col bidirectional, logic-seeking, impact printer, model 702 features a standard 7 x 7 dot matrix pattern (5 x 7, 9 x 7, 7 x 9, and 9 x 9 are options), and prints at 120 char/s. Printed data format consists of 10 char/in horizontally and operator selectable 6 or 8/in vertical spacing with either a 2-, 8-, or 12-channel electronic vertical format unit. Forms handling is tractor feed for rear or bottom feed forms. Paper widths range from 4" (102 mm) to 17.3" (439 mm). The system uses a cartridge containing a continuous ribbon 0.56" (14 mm) wide, 10 yd (9.1 m) long; a mobius loop allows printing on upper and lower portion on alternate passes. Data input is 7- or 8-bit ASCII parallel. **Centronics Data Computer Corp,** Hudson, NH 03051.



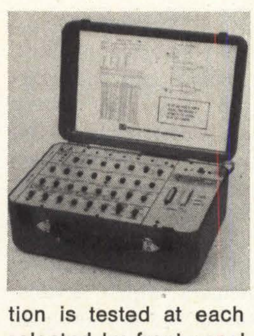
Circle 275 on Inquiry Card

CALCULATOR CONTROLLED PROCESS MONITORING SYSTEM

The Digitrend 240 scans and measures up to 1000 points of thermocouples, RTDs, voltages, or process transmitter signals. Each point is automatically digitized, linearized, and converted into engineering units for printing, recording, or passing on to the calculator. Four alarm setpoints may be individually set for each point. With the HP 9825A calculator as control terminal for the monitor, averages, integrals, trends, projections, deviations, and other calculations may be made using measured data. The monitor's control terminal interface is directly compatible with the calculator's RS-232-C interface module. Operation at 1200 baud allows low level analog multiplexing and digitizing rates up to approximately 10 points/s. Calculator keyboard allows entry of monitor commands such as function assignments, setpoint values, and operational commands. **Doric Scientific Div, Emerson Electric Co,** 3883 Ruffin Rd, San Diego, CA 92123.

Circle 276 on Inquiry Card

OFFLINE TERMINAL TESTER



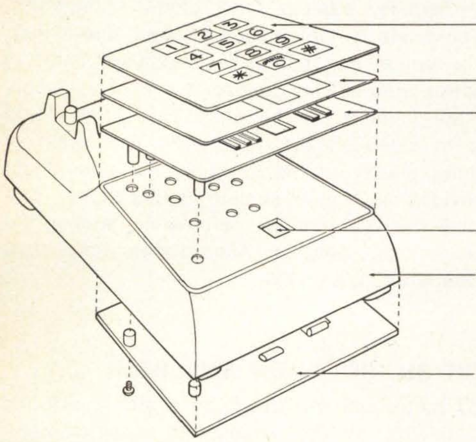
A full-duplex unit that offers split-speed capability (ie, both character generator and receiver can operate at different speeds), the PMK04 can be carried to remote locations for testing a single asynchronous ASCII terminal or can be used at large installations. In testing, the unit exercises all printer/display functions at all transmit/receive speeds; in troubleshooting a fault, each function is tested at each speed until the fault is found. Data selected by front-panel switches are generated, converted to serial data format, parity added if selected, and transmitted to the serial terminal, via EIA voltage levels or the 20-mA DEC-compatible current loop. Characters can be received from the terminal keyboard, parity checked, the ASCII code displayed on the front-panel indicator, and then echoed back to the terminal. **Atlantic Research Corp,** 5390 Cherokee Ave, Alexandria, VA 22314.

Circle 277 on Inquiry Card

GRAPHICS AND IMAGING VIDEO PROCESSOR

Self-contained on a 15 x 15" (38 x 38-cm) PC board that fits into any std Data General Nova or Eclipse computer, the 200-D generates raster-scanned, refresh, graphics, and imaging displays up to 512 x 512 pixels in B/W monochrome or 256 x 256 pixels in 16-level gray scale or color. A writable control store enables all image processing and data formatting routines to be modified under program control from the host computer. This allows instantaneous reallocation of refresh memory between the size of display and levels of intensity displayed. The unit incorporates a high speed bipolar video microprocessor with a cycle time of 100 ns; either the host computer or processor-resident 32k bytes of memory is used to refresh the display. **Lexidata Corp,** 215 Middlesex Tpk, Burlington, MA 01803.
Circle 278 on Inquiry Card

TOUCH SENSITIVE KEYBOARD SWITCHING SYSTEM



Using thick-film techniques to provide a flat, sealed data entry surface for such equipment as electronic POS terminals and scales, the TIP™ (touch-in-panel) system replaces traditional pushbutton switches with a smooth Mylar surface. The entire switching assembly is sealed. Assembly consists of panel, with keyboard printed on the top and contact surface on the reverse side. A circuit isolation mask is sandwiched between the Mylar and a substrate circuit carrier. This subassembly is laid on the end product's housing so that depressing an imprinted button on the Mylar forces the contact material on the back to touch the substrate, making an electrical connection through metal pins to the logic board. **Oak Industries Inc, Switch Div,** Crystal Lake, IL 60014.
Circle 279 on Inquiry Card

PDP-11/70 COMPATIBLE DISC SYSTEM

The DD70 series consists of the Computroller V, an intelligent microprocessor-based disc controller; 4-board PDP-11/70 interface, which plugs into the computer in place of the DEC RH70 Massbus[R] controller; and a choice of disc drives ranging in capacity from 80M to 300M bytes/spindle. Controller interfaces directly to the computer and communicates directly with its cache bus controller. Replacing DEC RP04 and RP06 drives, the system uses a microprocessor-based emulation package, and is software transparent to all std DEC operating systems. The disc system supports RSTS RSX11D, RSX11M, Mumps, Unix, and DOS operating systems. Error correction is provided for both header and data fields, and transfer rates of up to 1209k bytes/s are supported. **Diva, Inc,** 607 Industrial Way W, Eatontown, NJ 07724.
Circle 280 on Inquiry Card

PRODUCTS

DIGITIZER INPUT FOR HANDHELD PROGRAMMABLE CALCULATOR

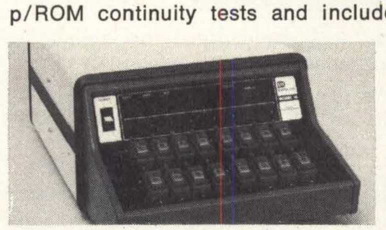
A non-keyboard entry device, SAC® GP-352 consists of a basic Graf/Pen™ TP-3 sonic digitizer, SR-52 calculator, and necessary interface, cabling, and plug-in connector. The system can calculate variables such as area, line length, and volume. In a typical application, a navigation chart is put within the active area of the digitizer's sensor assembly and two points are located on the chart with a handheld stylus or cursor to establish the orientation and scale of the chart. Touching points on the chart with the handheld input device provides automatic scaling and storage. Calculator will display the last position calculation and/or the total of all calculations. **Science Accessories Corp,** 970 Kings Hwy W, Southport, CT 06490.
Circle 281 on Inquiry Card

DATA ACQUISITION ISOLATION AMPLIFIER

Up to eight 286J amps can be driven by a single external synchronizing oscillator; multiple oscillators allow configurations of virtually limitless numbers. An internal isolated dual 15-Vdc at 15-mA supply provides power for external transducers and signal conditioning devices. For industrial data acquisition applications, it provides total ground loop isolation and protection from common-mode voltages of ±2500-V, continuous, or a max ±6500-V pk, 10-ms pulse. Nonlinearity of ±0.05% at 10-V pk-pk output makes the device suitable for systems requiring 10-bit accuracy. Input voltage drift is ±10 μV/°C; gain stability is 0.001%/1000 h and 0.01%/°C. **Analog Devices, Inc,** Rte 1 Industrial Pk, PO Box 280, Norwood, MA 02062.
Circle 282 on Inquiry Card

HIGH OUTPUT p/ROM PROGRAMMER

Delivering programming rates approaching 1M bytes/h, model 16 simultaneously programs 16 EPROMs, and includes a built-in calibration mode. In addition, it provides fault-finding p/ROM continuity tests and includes automatic pretests of programmer voltages. Automatic checksum sequences are used to test data integrity. The unit includes RS-232-C serial I/O with selectable baud rates, and features an interactive display for ease of operation. Both 2708 and 2716 type EPROMs can be programmed. To change programmer personality, simply replace the socket adapter on the programmer's front panel. A 2k-byte x 8-bit expandable RAM is std, along with RS-232-C serial I/O. **Data I/O Corp,** PO Box 308, Issaquah, WA 98027.



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LITERATURE

Flat Cables

Providing data on advantages of flat cable systems and on types of flat cables and terminations available, design guide helps identify potential applications. **Institute of Printed Circuits,** Evanston, Ill.
Circle 330 on Inquiry Card

Floppy Discs

Outlining the storage and handling of floppy discs, pamphlet reviews problems encountered with floppys and offers suggestions on how to prevent loss of data. **Advance Access Group,** Westchester, Ill.
Circle 331 on Inquiry Card

AC and DC Motors

Handbook is devoted to technical information and illustrations, with dimensional drawings and connection diagrams of ac motors, plus dc motors for aerospace military and high performance uses. **IMC Magnetics Corp,** Westbury, NY.
Circle 332 on Inquiry Card

Electronic Products

Catalog describes 400 electronic products in kit form, including personal computing systems, software, and peripherals, as well as a variety of assembled products. **Heath Co,** Benton Harbor, Mich.
Circle 333 on Inquiry Card

Printers/Plotters

Brochure covering line of electrostatic printers, plotters, and printer/plotters has 10 sections documenting applications, throughput, interfacing, and software. **Versatec, a Xerox Co,** Santa Clara, Calif.
Circle 334 on Inquiry Card

Uninterruptible Power Systems

Explaining problems and solutions encountered with computer systems involving power deviations, bulletin presents building block approach using static line voltage regulators, static automatic transfer switches, and UPS. **Cyberex, Inc,** Mentor, Ohio.
Circle 335 on Inquiry Card

Minicomputer Breadboards

32-page catalog describing general-purpose breadboards, connectors, and racks also shows minicomputer interface boards which are compatible with other hardware systems. **Douglas Electronics, Inc,** San Leandro, Calif.
Circle 336 on Inquiry Card

Miniature Circular Connectors

Focusing on 3-point bayonet type connectors of the KPT, KPTM, and KPSE line designed to MIL-C-26482, brochure contains drawings, photos, and data on materials and dimensions, and electrical data charts. **ITT Corp, Cannon Electric Div,** Santa Ana, Calif.
Circle 337 on Inquiry Card

Solid-State Lightpens

Catalog contains specs and definitions of specification terminology to aid designer in selecting units according to application needs. **Information Control Corp,** Los Angeles, Calif.
Circle 338 on Inquiry Card

Inductive Proximity Controls

Discussion of proximity sensing, applications, electrical specs, and information on mounting brackets, conduit fittings, and interfacing are highlighted in catalog covering line of solid-state proximity sensors, switches, and control systems. **Turck Multiprox, Inc,** Minneapolis, Minn.
Circle 339 on Inquiry Card

Sealed Component Sockets

Data sheet gives specs, diagrams, and features for NC machine insertable component sockets with silicone rubber seal. **AMP, Inc,** Harrisburg, Pa.
Circle 340 on Inquiry Card

Flat Cable Connectors

PCB, female socket, header, DIP, and card edge connectors for ribbon cable applications along with Cee Wee™ connectors are featured in catalog comprised of selection guide, assembly instructions, dimensional drawings, and specs. **CW Industries, Inc,** Warminster, Pa.
Circle 341 on Inquiry Card

Universal Data Converter

In addition to complete applications data, bulletin provides specs, systems diagram, features, and operation characteristics of DC-6 parallel-to-serial universal data converter. **Science Accessories Corp,** Southport, Conn.
Circle 342 on Inquiry Card

Terminals

Photos illustrate color brochure consisting of specs and features of the Dasher™ 60- and 30-char/s printers and display terminals. **Data General,** Westboro, Mass.
Circle 343 on Inquiry Card

LITERATURE

Micro/Minicomputers

Highlighting software, system packages, and applications, *PDP-11 Variations On A Theme* presents an overview of the computer family from entry level microprocessors to the "supermini" PDP-11/70. **Digital Equipment Corp,** Maynard, Mass.
Circle 344 on Inquiry Card

A-D, D-A Peripherals

Depicting electrical and mechanical parameters and programming considerations on the SineTrac 800 series, brochure includes block diagrams, details of diagnostic test programs, and programming methods. **Datel Systems, Inc,** Canton, Mass.
Circle 345 on Inquiry Card

Low Profile Switch Modules

Listing features, applications, operating characteristics, and specs, product sheet also provides force displacement curves for current sinking, pulsed, logic scan, and LED modules. **Micro Switch,** div of Honeywell, Freeport, Ill.
Circle 346 on Inquiry Card

Capacitors

Specs, temp characteristic graphs, and dimensional diagrams constitute catalog listing of miniature aluminum electrolytic, metallized polyester film, mylar, ceramic, and tantalum capacitors. **TransCap,** El Cajon, Calif.
Circle 347 on Inquiry Card

ATLAS Syntax Standard

Standard delineates the syntactic structure of the ATLAS test language in Backus Naur format, and offers a formal definition. IEEE Std 416A-1976 is available for $10 ($9 for members) plus $2 for shipping from **IEEE Service Ctr,** 445 Hoes Lane, Piscataway, NJ 08854.

Small Business Computers

All About Small Business Computers serves as a selection guide with comparison charts and detailed specs covering assorted computer systems. Price is $12/copy. **Datapro Research Corp,** 1805 Underwood Blvd, Delran, NJ 08075.

µC Programming and Interfacing

Bugbooks V and VI introduce the basics of 8080A microcomputer programming and instructions, and integrate the concepts into a treatment of 8080A interfacing with lab experiments and text review. Price is $9.50/book. **E & L Instruments, Inc,** 61 First St, Derby, CT 06418.

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

PAGE

 CIRCLE 140 ON INQUIRY CARD

GUIDE TO PRODUCT INFORMATION

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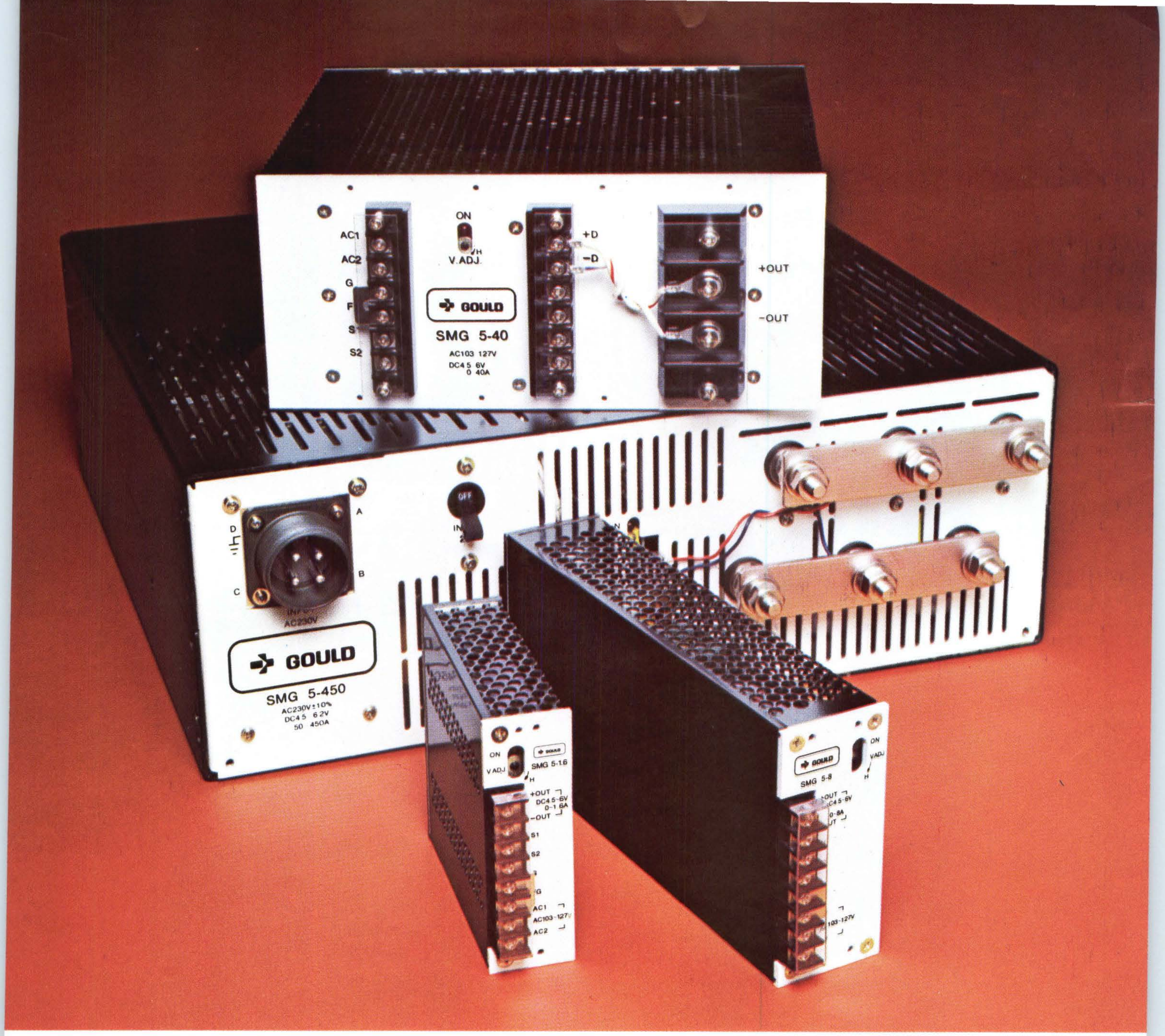

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