COMPUTER DESIGN

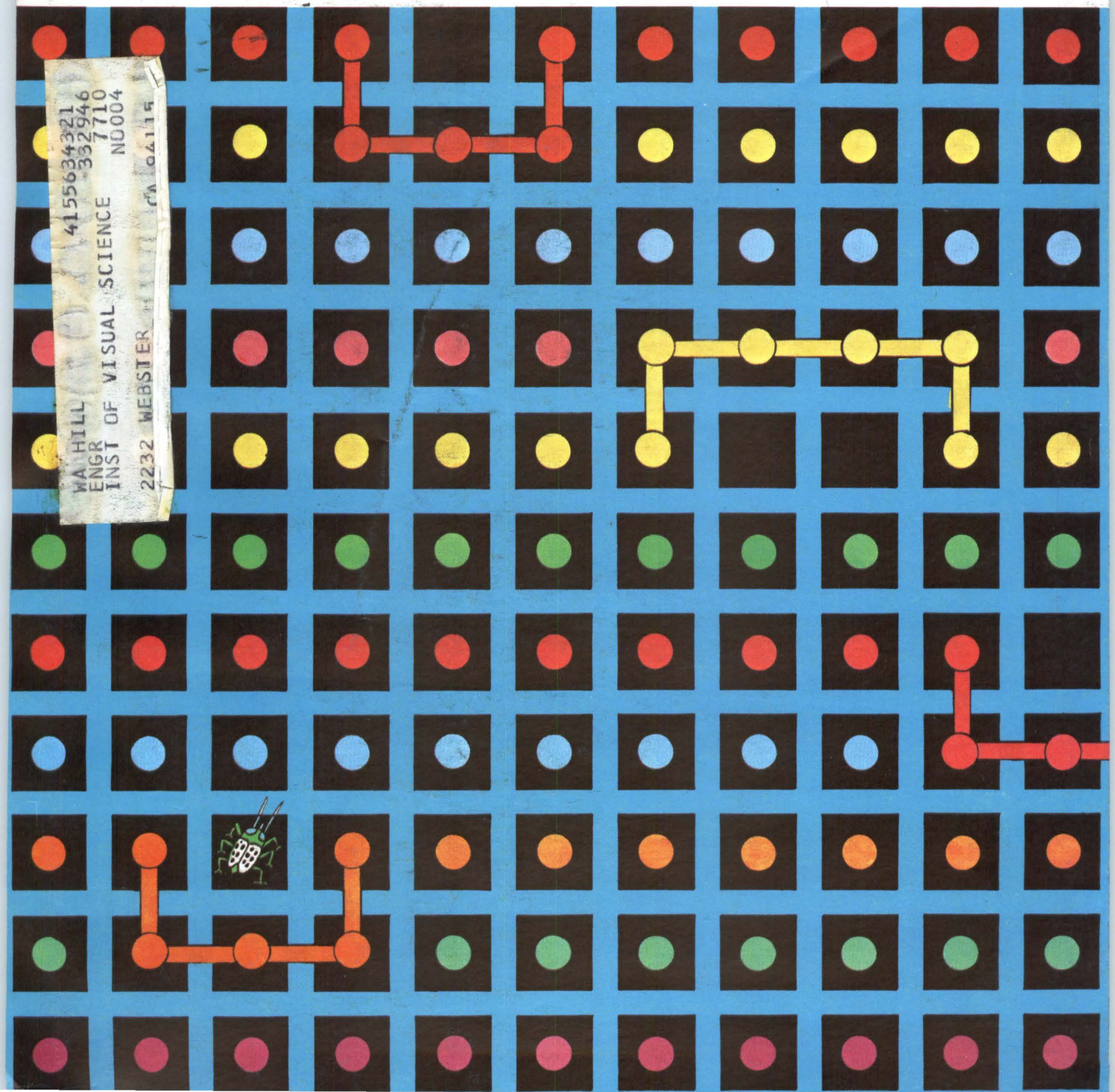
THE MAGAZINE OF DIGITAL ELECTRONICS

NOVEMBER 1978

BREAKPOINT DESIGN FOR DEBUGGING MICROPROCESSOR SOFTWARE

SIMPLE HARDWARE APPROACH TO ERROR DETECTION AND CORRECTION

MULTIPLE PROCESSOR MINICOMPUTER SYSTEMS—PART 2: Implementation



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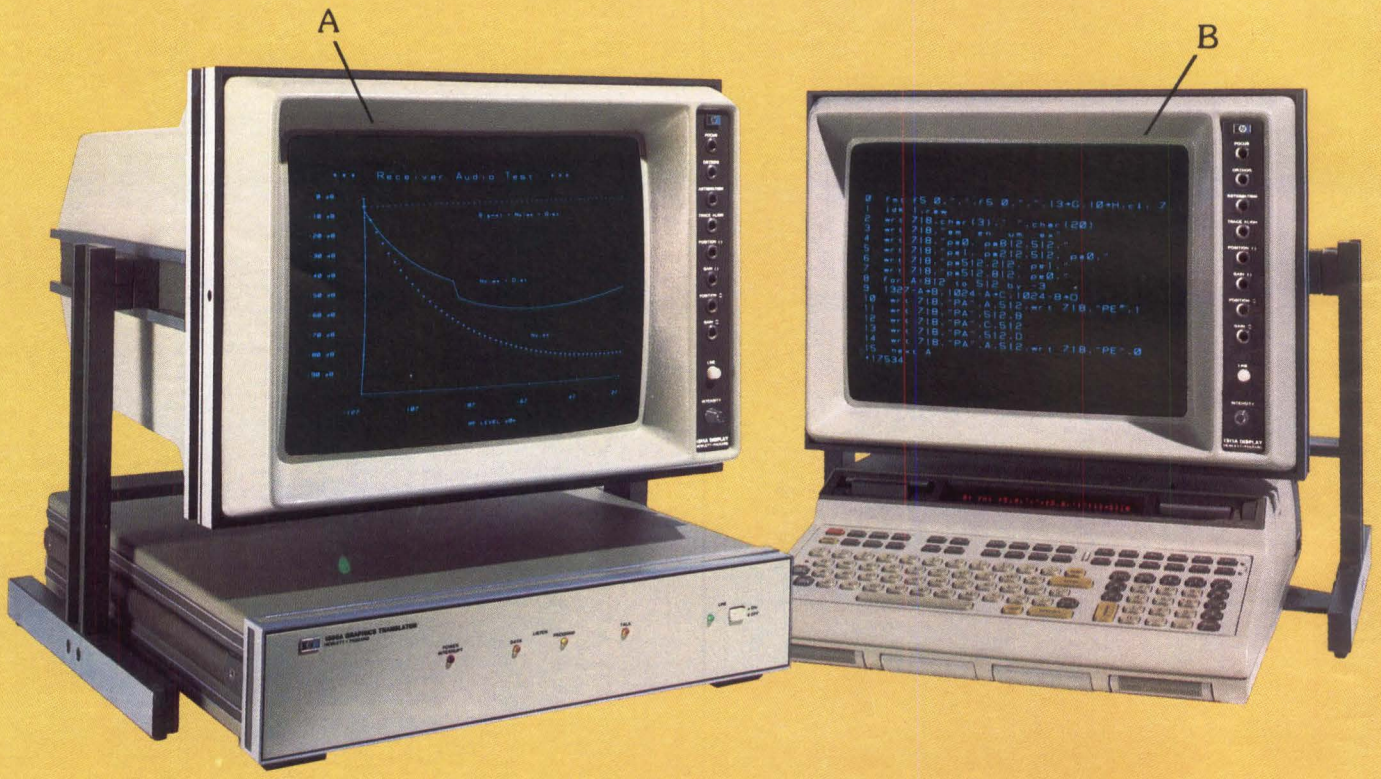
Here's the fastest HP-IB* graphic peripheral available today... and it programs like a plotter.



With the HP 1350A Graphics Translator and one or more HP electrostatic CRT displays, there's no faster way of seeing your system's output. You can get a quick reading - then plot if hard copy is needed.

Because it's HP-IB* compatible, the 1350A is easy to add to your system. It lets you present different information simultaneously on up to four CRT displays.

And, it makes writing a program for a CRT display as easy as programming a plotter. An optional binary cassette tape for the HP 9825 Desktop Computer simplifies programming and lets you use the same routines on both CRT's and plotters.

The 1350A lets you update the display selectively. For example, in an application such as sequential testing, you can view multiple data plots (A) on a CRT and update only a portion of the display for rapid comparative measurements. It also provides convenient operator interaction. You can display program listings (B), normal and expanded displays, or a cursor and its coordinates.

Ideal for use with HP Data Acquisition and Network Analysis Systems, the 1350A Graphics Translator, priced at $3,450**, is a useful tool anywhere a fast, high-resolution graphic presentation of information is needed. Write for Application Note 271-1, or call your local HP field engineer for complete details.

*HP's implementation of IEEE Standard 488-1975
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088/12

CIRCLE 1 ON INQUIRY CARD

Models 9100/9300 Vacuum Column Tape Transports . . .

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Kennedy's vacuum column digital tape transports weren't designed yesterday to grab a piece of a growing market. In fact, they virtually founded the vacuum column market. They were the first to have such features as a capacitive tape-location detector for improved tape life; air bearings and hardcoated read-after-write heads to reduce tape wear and improve data integrity.

Model 9100 (75 ips) and 9300 (125 ips) offer crystal controlled timing, read-after-write shortened skew gate, front-accessible test panel, quick release hubs and simplified tape loading.

Data densities are 200/556 cpi or 556/800 on 7-track units and 800 cpi, 1600 cpi or 800/1600 cpi on 9-track transports. The format is NRZ1/PE.

Models 9100/9300 offer more features, more performance, and most important, more time-in-the-field than any competitive units.

Why do we think so? Simple. Our figures show that we are about 3000 satisfied users ahead at this point.

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CIRCLE 2 ON INQUIRY CARD

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THE TALLY PRINTER TERMINAL

Control 42 functions via the keyboard or the program

The Tally T-1612 Printer Terminal is designed for the user. It's loaded with functions and features. In addition to 42 programmable functions, which are available through the keyboard or through the user program, you get features like outstanding print quality, optimized bi-directional printing at 160 cps for bonus throughput, quiet operation for office use, lots of forms control conveniences, table top or pedestal mount and outstanding reliability that translates into low cost of ownership. And plenty more.

Unique features include six selectable type fonts in upper and lower case, LED column/line indicator, non-destructive memory providing pre-selected configuration on power up and 1k buffer standard (up to 4k optionally).

The Tally T-1612 is also available as a Receive Only printer. Both versions sustain a full 1200 Baud transmission rate. Or you can select 300, 600, 2400, 4800 or 9600 Baud operation.

Tally Corporation, 8301 S. 180th St. Kent, WA 98031. Phone (206) 251-5500.

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COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

NOVEMBER 1978

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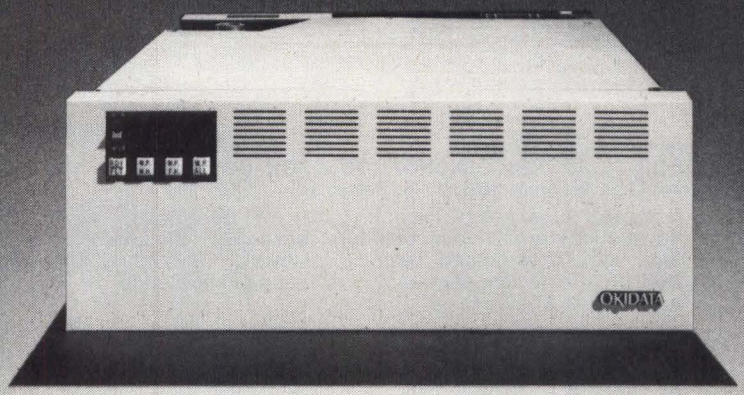
Okidata Sells Disc Drives That Sell Minisystems



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Seven 3300 Series models, from 13 to 80 megabytes, fit in just 7 inches of rack space, complete with power supply and the finest air filtration system in the industry.

The 3300 combines moving head storage with over two megabytes of fixed head to satisfy the full range of business, communications and distributed processing applications—with one form factor and one set of systems programs.

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Editorial & Executive Offices
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Tel. (617) 486-8944
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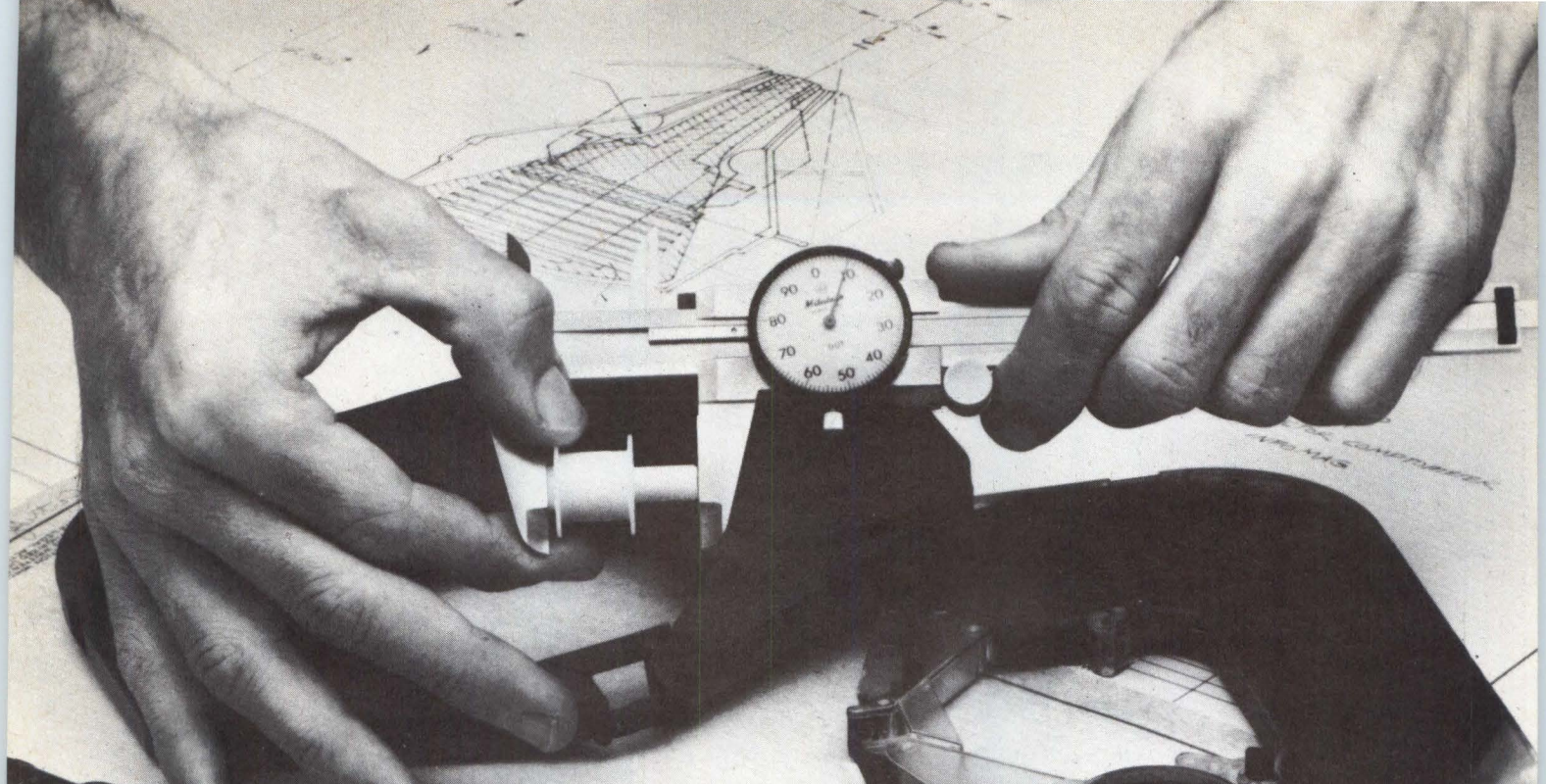

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Data Packaging Corp.

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We deliver performance.

CIRCLE 5 ON INQUIRY CARD

THE PARTS THAT SET US APART

Look at us part by part. There has never been a vacuum column transport like Cipher Data Product's 900X—the first vacuum column tape drive with complete microprocessor control—available in 75 ips or 125 ips.

Forget all the old problems with vacuum column tape drives—the heat, the noise, the inefficient tape control, the belts, hoses, relays, solenoids, cooling fans, incandescents, energy drain, oversize and high cost—because the Cipher Data Products 900X drives don't have any of them. The 900X Series is a completely new design concept in digital tape technology.

Part I—The Z-80 Microprocessor

The intelligence of the Z-80 microprocessor brings major performance enhancements to the 900X while increasing reliability through reduction in both the complexity and number of components. For the first time, total control of tape is a reality in a vacuum column tape drive. There is no snap, whip or loose tape during critical load and unload. There is no possibility of tape damage in the event of power failure in any mode. And, because exact tape position is sensed and controlled by the microprocessor, maximum possible speed is maintained throughout the rewind operation.

Built-in diagnostics and service aids, unique to the Series 900X drives, are made possible by Z-80 intelligence. Decision making logic in ROM is automatically tested during power up and, if not successful, the drive shuts down with fault indications clearly given on the front panel. Possible damage to tape or machine is avoided and, since fault areas are readily identified, repair and maintenance time are minimized.

Part II—Dual Density Databoard

With the 900X Series, Cipher Data Products introduces a state-of-the-art databoard on only one card that handles dual density, NRZ or PE only and is 100% industry compatible. To the user, this multi-function board significantly reduces spares cost.

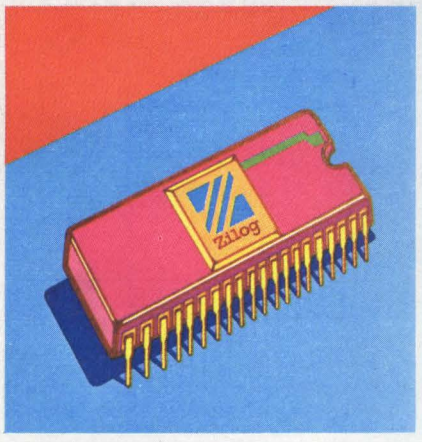
Most important, in comparison with competitive units, this new databoard provides increased reliability—with a 40% reduction in total parts count, improved PE resolutions, low noise generation and pickup, a 50% lower power consumption, and the elimination of troublesome write deskew alignments. In addition, self test through special diagnostic and alignment modes can be accomplished without the use of external equipment.

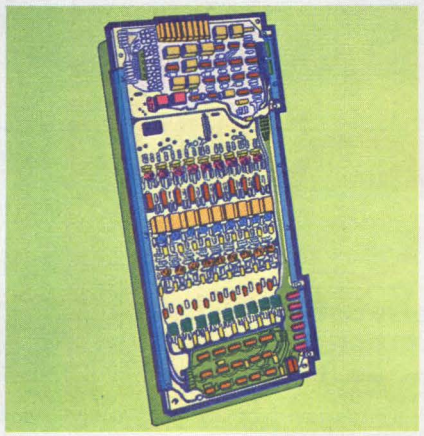
Part III—The Beltless Direct Drive

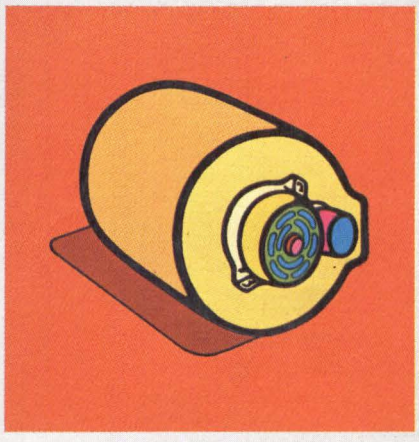
Compare Cipher Data Product's 3400 rpm direct drive motor to the belt driven 10,000 rpm motors in most competitive drives. The 900X drive operates on only 300 watts (nominal) of power in large part due both to the use of the direct drive motor and to a highly efficient, low power, multistage centrifugal pump, contrasted to the multiple pumps required by other drives. Only one blower on the 900X means quiet, whisper-like operation and no hose connections to cause maintenance problems. And, the Cipher drive can be operated on either 50 Hz or 60 Hz without frustrating belt change.

Now look at all the other parts—like the switched linear servo system, optical file protect, LED light sources, hard chromed face read/write head, sapphire tape cleaner and modulated tape sensor system. The Series 900X vacuum column tape drive is far ahead of the market in design while still fully compatible with today's industry standards.

Do your part. Call for full information and OEM quantity price competitive quotes. Cipher Data Products, Inc., 5630 Kearny Mesa Road, San Diego, California 92111. (714) 279-6550.







Cipher
Data Products

CIRCLE 6 ON INQUIRY CARD

The EMR is dead... Long live Motorola

The SPST electromechanical relay (EMR) is dead – killed by contact arcing, mechanical wearout and incompatibility with modern circuitry.

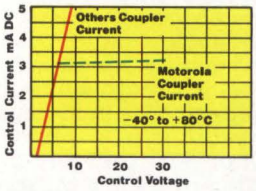
We know – and you know – where multiple-pole, higher current contactor applications are required, it'll still be around.

But for the bulk of logic level designs where you need the advantages of solid-state reliability, convenience, versatility, standard packages, multiple sourcing and low cost... solid-state relays are the *only* way to go!

Now Motorola presents a new, broad line of SSRs and I/O modules vastly superior to the century-old EMR and affording significant advances even over similar contemporaries. Advances that spell quality throughout.

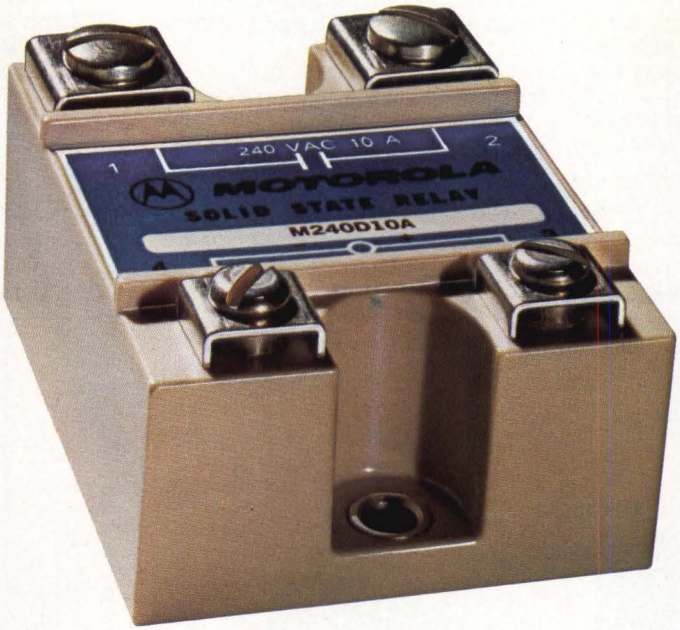
- Like better input characteristics for optimized opto coupler life. The more current, the shorter the coupler's life expectancy. Our SSRs limit coupler current and hold it to a minimum. The result is a longer-lasting SSR with constant performance over time.
- Like use of the finest, in-house manufactured semiconductors from the world's technology-in-volume producer. Nobody can beat that kind of QC.
- Like extended design goals with design performance verified by Mil-type testing. Quality and care in manufacture mean a better product from us now and a better one for you down the road.
- Like complete, void-free, vibration-resistant potting that's withstood millions of hours of under-the-hood environments.

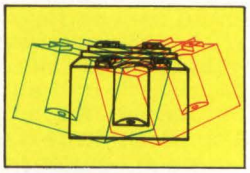
For Power Designs



Positive control over temperature

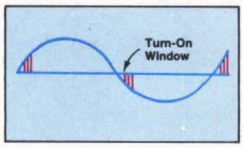
We guarantee the control points of the output switch over the full spec'd temp range. You can count on it from 3-32 V over a −40° to +80°C range. And the highest voltage doesn't shorten life of the optical isolator. Our design goal is reliable operation for 10 years.





Shock & vibration-resistance

Completely potted units have shown ability to withstand MIL-spec type testing for accelerated impact, vibration, salt spray, thermal cycling life, etc. We make 'em rugged for rugged environments.

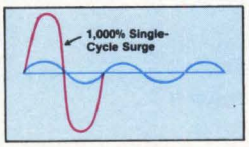


Zero voltage switching

Closures can occur only near the zero-crossing point of line voltage, minimizing noise generation which could interfere with other electronics. The electrical environment therefore remains clean.

Reverse polarity protection

Additional features like reverse polarity protection obviate damage from error in installation and subsequent equipment malfunction.



High peak surge ratings

1000% single cycle surge ratings protect against current abuse. Conservatively-rated components and thermal design contribute to longer service life.

Transient immunity

Motorola SSR components are 100% overrated for high voltage conditions. Each is internally protected against high line, random noise, spikes and conditions typically found in harsh industrial environments.

solid-state relays!

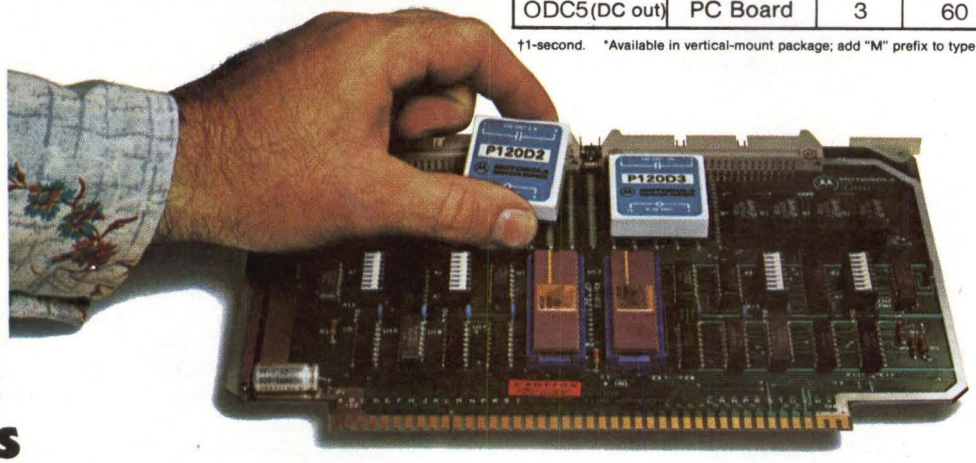
- Like compatibility with microprocessors, integrated circuits and other solid-state relay control circuits.
- Like standardized packaging and footprints available from multiple industry sources.
- Like technical field assistance from our nationwide applications engineers and reps and stocking from authorized distributors.

That's why our relays and modules are so good. And that's why they'll last a long time.

For more information on any of these new Motorola solid-state units, contact Motorola Subsystem Products, P.O. Box 20912, Phoenix, AZ 85036 (602) 244-3103. Viva Motorola Solid-State Relays!

Switch	Type Mounting	Output Current A	Line Voltage V	Peak Surge# A
M120D05A	Chassis	5	120	50
M120D10A	Chassis	10	120	100
M240D05A	Chassis	5	240	50
M240D10A	Chassis	10	240	100
P120D2*	PC Board	2	120	20
P120D3*	PC Board	3	120	55
P240D2*	PC Board	2	240	20
P240D3*	PC Board	3	240	55
IAC5 (AC in)	PC Board	—	95-130	—
IDC5 (DC in)	PC Board	—	10-32	—
OAC5 (AC out)	PC Board	3	12-140	55
ODC5 (DC out)	PC Board	3	60	5†

†1-second. *Available in vertical-mount package; add "M" prefix to type number. #Single-Cycle.

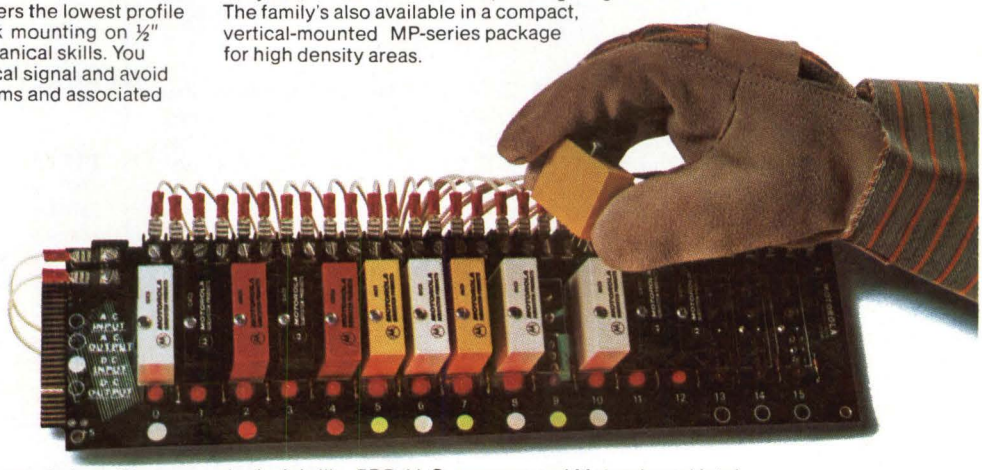


For PC Boards

Fit-anywhere, go-anywhere horizontal- or vertical-mounted convenience and economy are yours with the P/MP-series 2 & 3A, 120 & 240 V relays.

Measuring only ⅜" thick, P-series offers the lowest profile solid-state unit of its kind for card rack mounting on ½" centers. No wire terminations. No mechanical skills. You treat system loads like any other electrical signal and avoid connector-wire, board-mounting problems and associated labor costs.

1,500 V photo isolation, zero-voltage turn on, built-in snubber network, 100% testing at rated load, I/C compatibility and a −40° to +100°C operating range are standard. The family's also available in a compact, vertical-mounted MP-series package for high density areas.



For I/O Systems

In a costly electronic control system, it's easy to invest two-thirds to three-fourths of total cost in just interface and wiring. We've now solved that and given you the convenience and versatility to revolutionize your I/O control system.

Because each Motorola I/O module contains signal conditioning, isolation, logic interface, power handling and status indication drive in one compact, compatible package that interfaces with all 5 V logic families and standard MPU I/O requirements. At a *fraction* of the cost of other systems.

The color-codable board's standard, too... with or without the modules. You can interface the entire system with standard minis like PDP-11, Supernova and Motorola and Intel micros... install them in standard NEMA enclosures... and remove or replace modules without disturbing field wiring. The package is rapidly becoming the industry standard, too... and that makes it comfortable.

Motorola I/O Modules. Easy. Quick. Reliable.

MOTOROLA INC.

CIRCLE 7 ON INQUIRY CARD

CALENDAR

CONFERENCES

DEC 4-6—Conf of the Assoc for Computing Machinery, Sheraton-Park Hotel, Washington, DC. INFORMATION: Dr Richard Austing, Dept of Computer Science, U of Maryland, College Park, MD 20742. Tel: (301) 454-2004

DEC 4-6—Internat'l Electron Devices Meeting, Washington Hilton Hotel, Washington, DC. INFORMATION: Susan Henman, Courtesy Assoc, 1629 K St NW, Washington, DC 20006. Tel: (202) 296-8100

DEC 5-7—Design Engineering Conf/West, Convention Ctr, Anaheim, Calif. INFORMATION: Clapp & Poliak, Inc, 245 Park Ave, New York, NY 10017

DEC 12-14—Midcon, Dallas Convention Ctr and Dallas Hyctt Regency, Dallas, Tex. INFORMATION: William C. Weber, Jr, General Mgr, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965

DEC 13—Computer Networking Sym, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: Computer Networking, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

JAN 16, FEB 8—Invitational Computer Conf, Orange County, Calif; Ft Lauderdale, Fla. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: (714) 644-6037

JAN 22-26—Computers and Peripheral Trade Show, London, England. INFORMATION: E. Belden, U.S. Dept of Commerce, Bureau Export Div, Washington, DC 20230

JAN 24-27—Internat'l Microcomputers/Minicomputers/Microprocessors (IMMM), Harumi Exhibition Ctr, Tokyo, Japan. INFORMATION: Industrial and Scientific Conf Management, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

JAN 30-FEB 1—Communication Networks, Sheraton-Park Hotel, Washington, DC. INFORMATION: Ed Halsted, The Conference Co, 60 Austin St, Newton, MA 02160. Tel: (617) 964-4550

FEB 6-8—Sym on Modeling and Performance Evaluation of Computer Systems, Technische Universität Wien, Austria. INFORMATION: Dr A. Butrimenko, Internat'l Institute for Applied Systems Analysis, A-2361 Laxenburg, Austria

FEB 12-16—Computers and Peripheral Equipment Exhibition, U.S. Trade Ctr, Sao Paulo, Brazil. INFORMATION: Industry and Trade Administration, Rm 4039, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-5427

FEB 14-16—European Conf on Parallel and Distributed Processing, Toulouse, France. INFORMATION: C. Girault, Institut de Programmation, 4 Place Jussieu, 75230 Paris Cedex 05, France

FEB 14-16—IEEE Internat'l Solid State Circuits Conf (ISSCC), Philadelphia, Pa. INFORMATION: Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: (305) 446-8193

FEB 26-MAR 1—COMPCON Spring, San Francisco, Calif. INFORMATION: COMPCON Spring 79, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

FEB 26-MAR 2—INTELCOM, Dallas Convention Ctr, Dallas, Tex. INFORMATION: M. Raftery, Mgr of Promotion, Horizon House Internat'l, 610 Washington St, Dedham, MA 02026. Tel: (617) 326-8220

FEB 27-MAR 2—NEPCON WEST, Anaheim Convention Ctr, Anaheim, Calif. INFORMATION: Industrial and Scientific Conf Management, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

FEB 28-MAR 2—Internat'l Computer Expo, Tokyo Internat'l Trade Ctr, Tokyo, Japan. INFORMATION: Golden Gate Enterprises, Inc, 1307 S Mary Ave, Suite 210, Sunnyvale, CA 94087. Tel: (408) 735-1122

MAR 4-8—Business Systems Exhibition, U.S. Trade Ctr, Tehran, Iran. INFORMATION: Susan Blackman, Project Mgr, Commerce Action Group for the Near East (CAGNE), Rm 6015B, Washington, DC 20230. Tel: (202) 377-2952

MAR 6-8—Optical Fiber Communication, Shoreham Americana Hotel, Washington, DC. INFORMATION: Optical Society of America, 2000 L St, NW, Suite 620, Washington, DC 20036. Tel: (202) 293-1420

MAR 19-21—IECI Conf and Exhibit on Industrial and Control Applications of Microprocessors, Philadelphia, Pa. INFORMATION: S. J. Vahaviolos, Physical Acoustics Corp, PO Box 3135, Princeton, NJ 08540. Tel: (609) 799-8266

SEMINARS

DEC 4-5—Microcomputers: Operating Principles, Hardware, and Software, and DEC 6-8—Microcomputer Hardware and System Design; DEC 4-8—PASCAL Programming for Mini and Microcomputers, and DEC 7-9—Bit-Slice Microcomputer and Digital System Design; and JAN 11-13—Software Engineering for Mini/Microcomputer Systems, Dallas, Tex; Woburn, Mass; and Los Angeles, Calif. INFORMATION: Prof Donald D. French, Institute for Advanced Professional Studies, One Gateway Ctr, Newton, MA 02158. Tel: (617) 964-1412

DEC 18-20—Software Testing and Test Documentation Workshop, Bahia Mar Hotel, Ft Lauderdale, Fla. INFORMATION: Dr Edward F. Miller Jr, Software Research Associates, PO Box 2432, San Francisco, CA 94126

JAN 10-11, MAR 27-28—Professional Calculator Seminar, Ambassador Motor Hotel, Minneapolis, Minn. INFORMATION: Nortronics Education Div, 8101 Tenth Ave N, Minneapolis, MN 55427. Tel: (612) 545-0401, X295

JAN 23-25—ATE Seminar/Exhibit, Los Angeles Marriott Hotel, Los Angeles, Calif. INFORMATION: ATE Seminar/Exhibit, Circuits Manufacturing Magazine, 1050 Commonwealth Ave, Boston, MA 02215. Tel: (617) 232-5470

SHORT COURSES

DEC 4-8, DEC 11-15, JAN 15-19, JAN 22-26, and JAN 29-FEB 2—Microprocessor/Computer Short Courses, Washington, DC; Atlanta, Ga; Los Angeles, Calif; Denver, Colo; and Dallas, Tex. INFORMATION: Kim D. Sanson, Program Mgr, Integrated Computer Systems, Inc, 3304 Pico Blvd, PO Box 5339, Santa Monica, CA 90405. Tel: (213) 450-2060

DEC 11-15—Modern Digital Communications; JAN 8-12—Structured Programming and Software Engineering; JAN 22-23—Minicomputer Technology; and JAN 24-26—Design and Selection of Minicomputers, George Washington U, Washington, DC. INFORMATION: Martha Augustin, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

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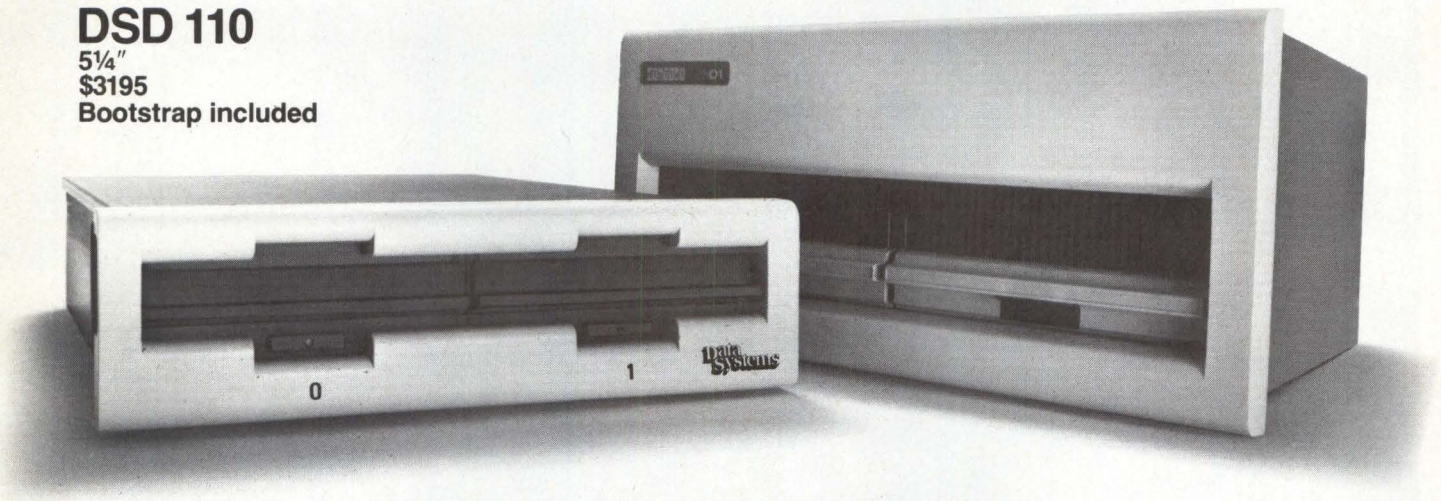

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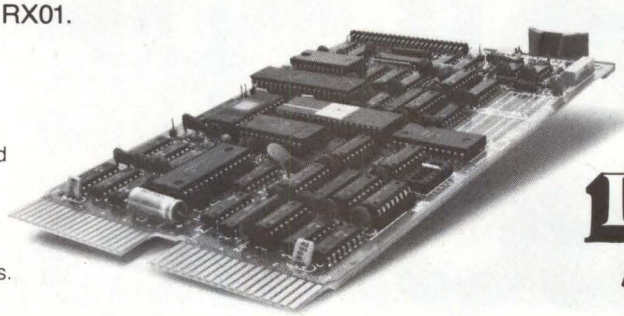

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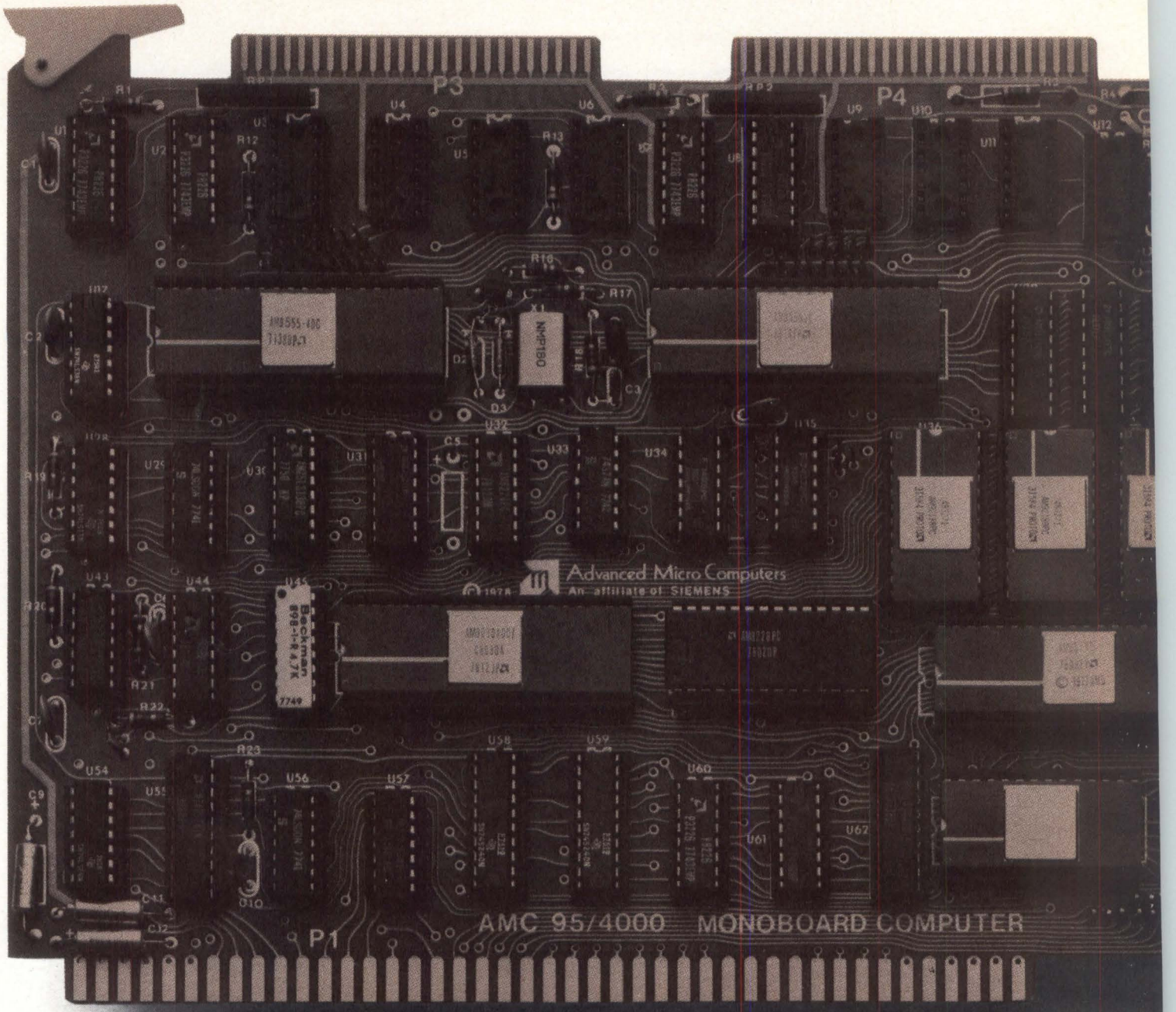
CIRCLE 8 ON INQUIRY CARD



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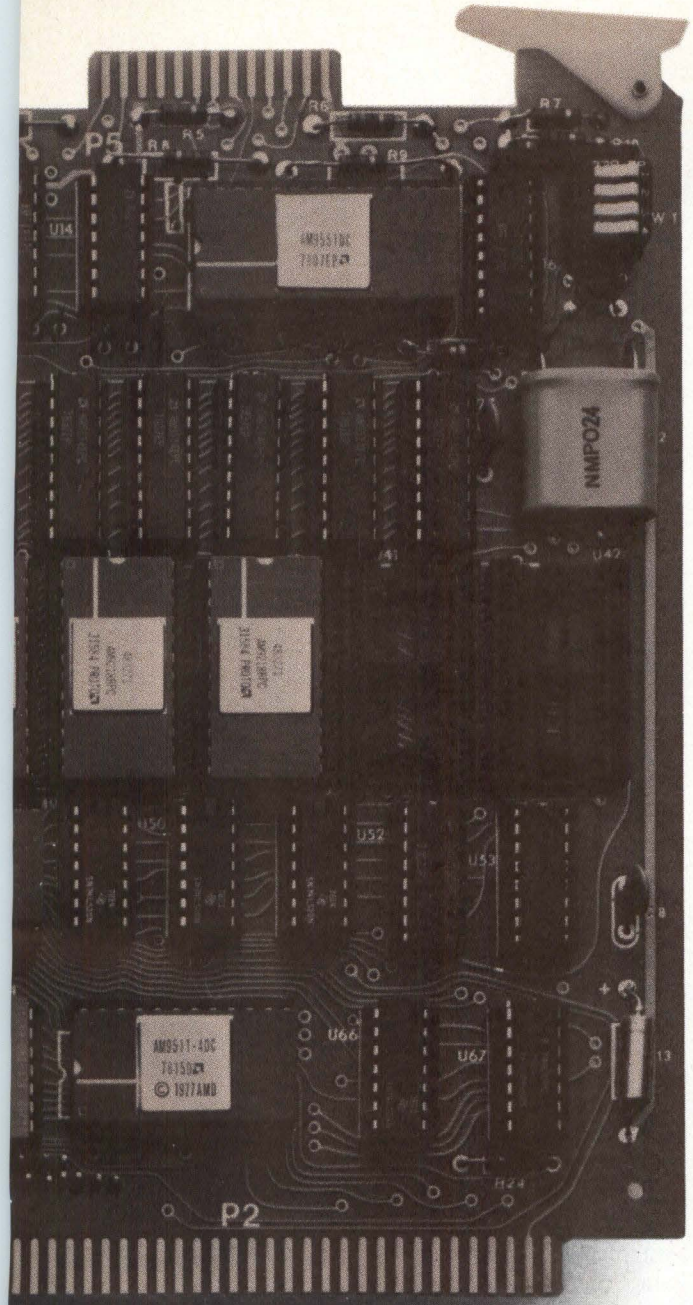

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CIRCLE 9 ON INQUIRY CARD

COMMUNICATIONS ACT of 1978

John E. Buckley
Telecommunications Management Corporation
Cornwells Heights, Pennsylvania

The year 1978 has been marked by a new attempt to replace the original Communications Act of 1934. It was under that legislation of over 40 years ago that the Federal Communications Commission (FCC) was formed, and the concept of franchised communications monopolies, ie, AT&T, was defined and implemented. Much of the confusion and turmoil characterizing today's evolving world of telecommunications regulation is the result of continuing attempts to interpret and apply the provisions of that 1934 statute to the demands and needs of the telecommunications community of 1978. It is universally agreed that there is a necessity to rewrite that Communications Act to be reflective of today's requirements, and supportive of communications developments in the foreseeable future.

During 1976 a Bell System sponsored legislation entitled the Consumer Communications Act of 1976 was introduced to the United States Congress. It was blatantly structured to prohibit competition in all aspects of communications services and equipment while at the same time granting antitrust immunity to AT&T. During an election year it was obvious that some legislators would automatically add their endorsements because of the vote-stimulating title of the proposed Act. It was only after a major information campaign by independent communications equipment manufacturers and by the specialized communications common carriers that the U.S. Congress acted to defeat that effort.

In June of 1978, Congressmen Van Deerlin and Frey introduced a rewrite of the 1934 Communications Act. This effort was not initiated by any special interest group. It was a genuine attempt to realign a generally outmoded legislative Act in order to meet all legitimate needs of the participants in today's communications environment.

This proposed Communications Act of 1978 would replace the present FCC with a new Communication Regulatory Commission. One of the primary tasks of this body would be to define and establish the guidelines under which services would be classified as either competitive or non-competitive. Its jurisdiction would be only over interstate telecommunications services. This classification authority would permit the allocation of competitive and monopoly markets.

As the new Act is presently drafted, the Commission is apparently provided a broad and loosely defined authority to define and classify. Many competitive communications organizations have expressed concern that, under the draft provisions, the new Commission could broaden the existence of regulation rather than encourage a growing competitive environment.

The Act specifies the objectives or guidelines for the new Commission. As with the Communications Act of 1934, the promotion and support of a nationwide telecommunication service at affordable rates is cited as a major goal. The Act also declares that the Commission is to place maximum "feasible" reliance on competitive marketplace forces. As such, it is guided to rely on the ensuing competition to bring the desired efficiencies, innovations, and economies to the consumer. These same competitive factors are to be expected to determine the variety, quality, and cost of telecommunications services. The new Commission is also instructed to establish and encourage full and fair competitive conditions, and to prevent practices that would allow or cause the limitation or exclusion of competition in the provision of telecommunications services. The only reference to the use of regulation in these guidelines is in cases where competitive marketplace forces are deficient.

The tone of the Act appears pro-competition and advocates minimal application of regulation on almost an exception basis. There appear to be concerns however, that certain oversights and omissions will encourage even greater confusion and restrictions than presently exist under the original Communications Act of 1934.

(*Continued on p* 19)

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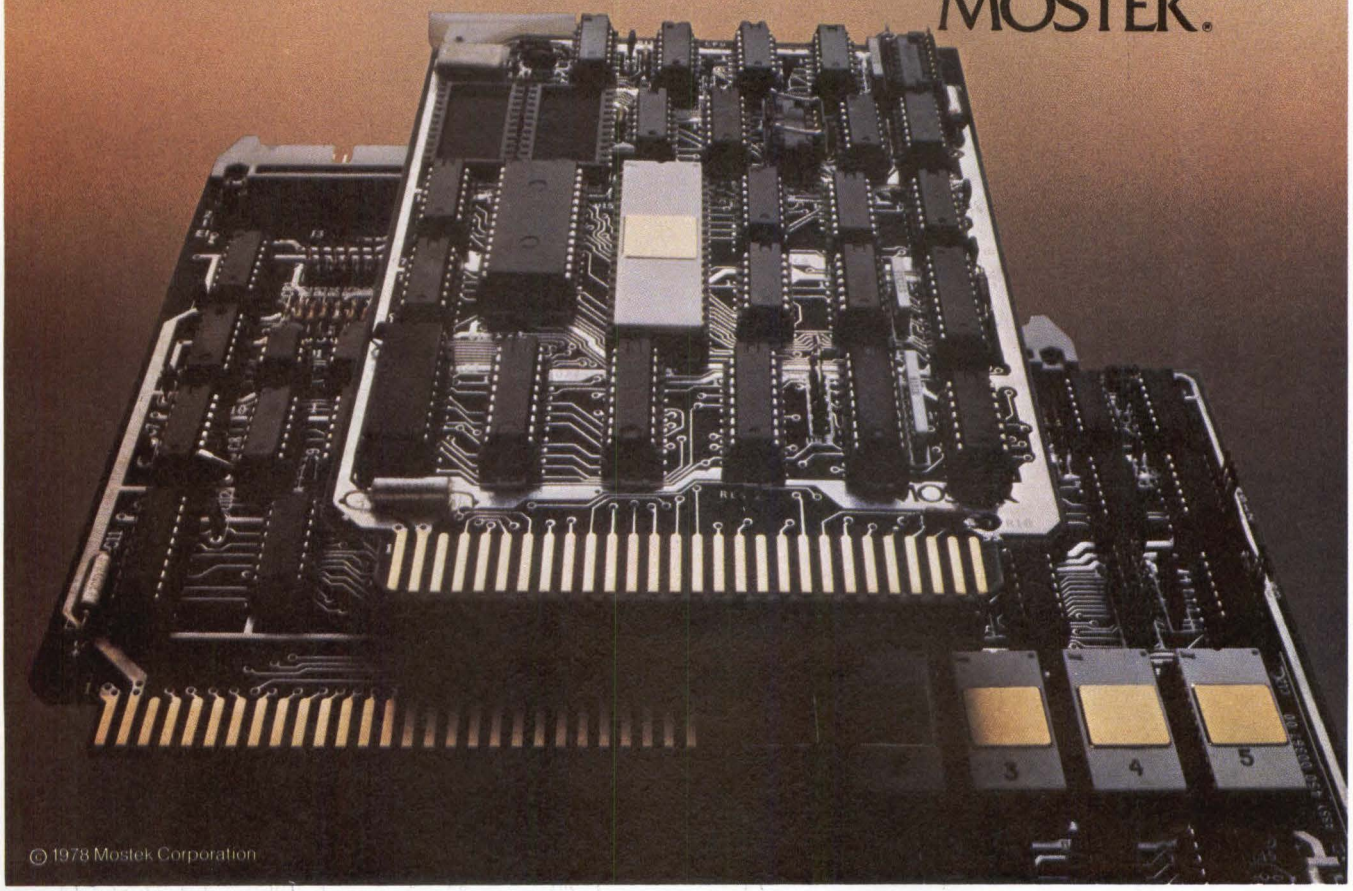

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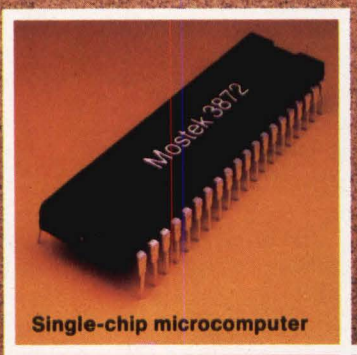


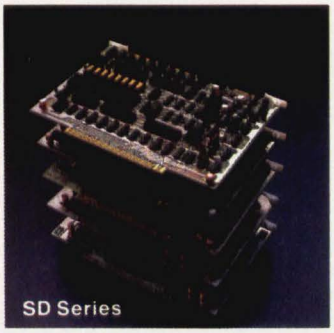
Single-chip microcomputer

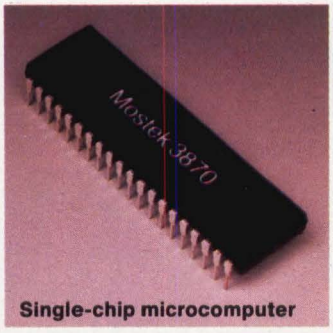
Z80 Combo Chip

3870 FAMILY

AID-80F software

Z80

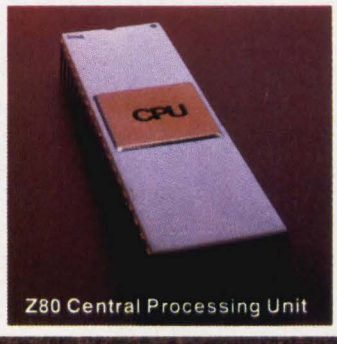

SD Series



Single-chip microcomputer

CRT and line printer

Single-chip microcomputer



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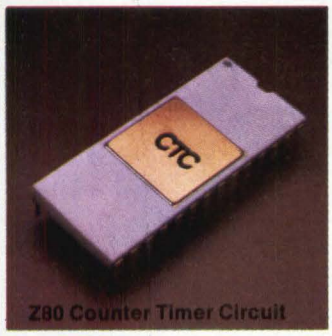
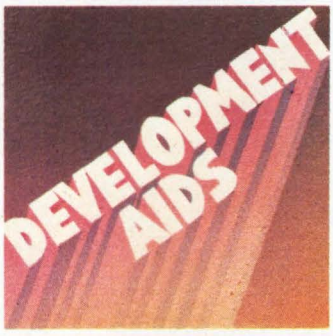
MD Series

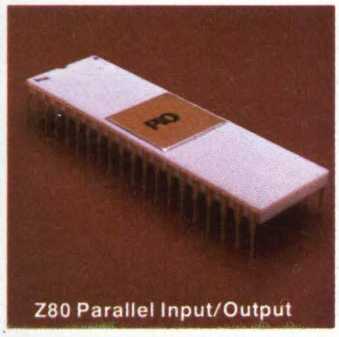
AID-80F



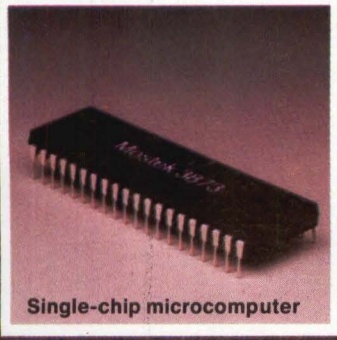
Z80 Counter Timer Circuit

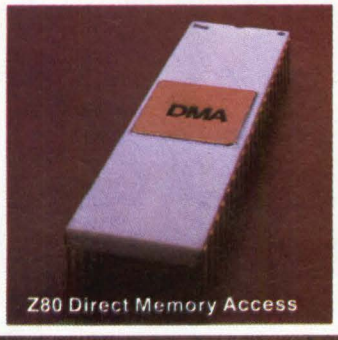


Software development boards

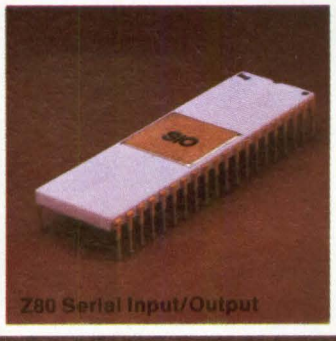


Z80 Parallel Input/Output

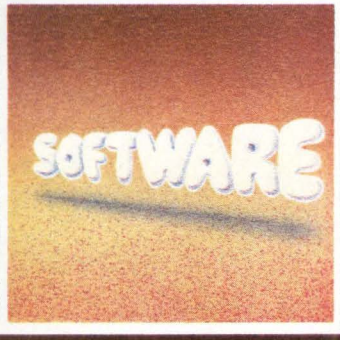

Single-chip microcomputer

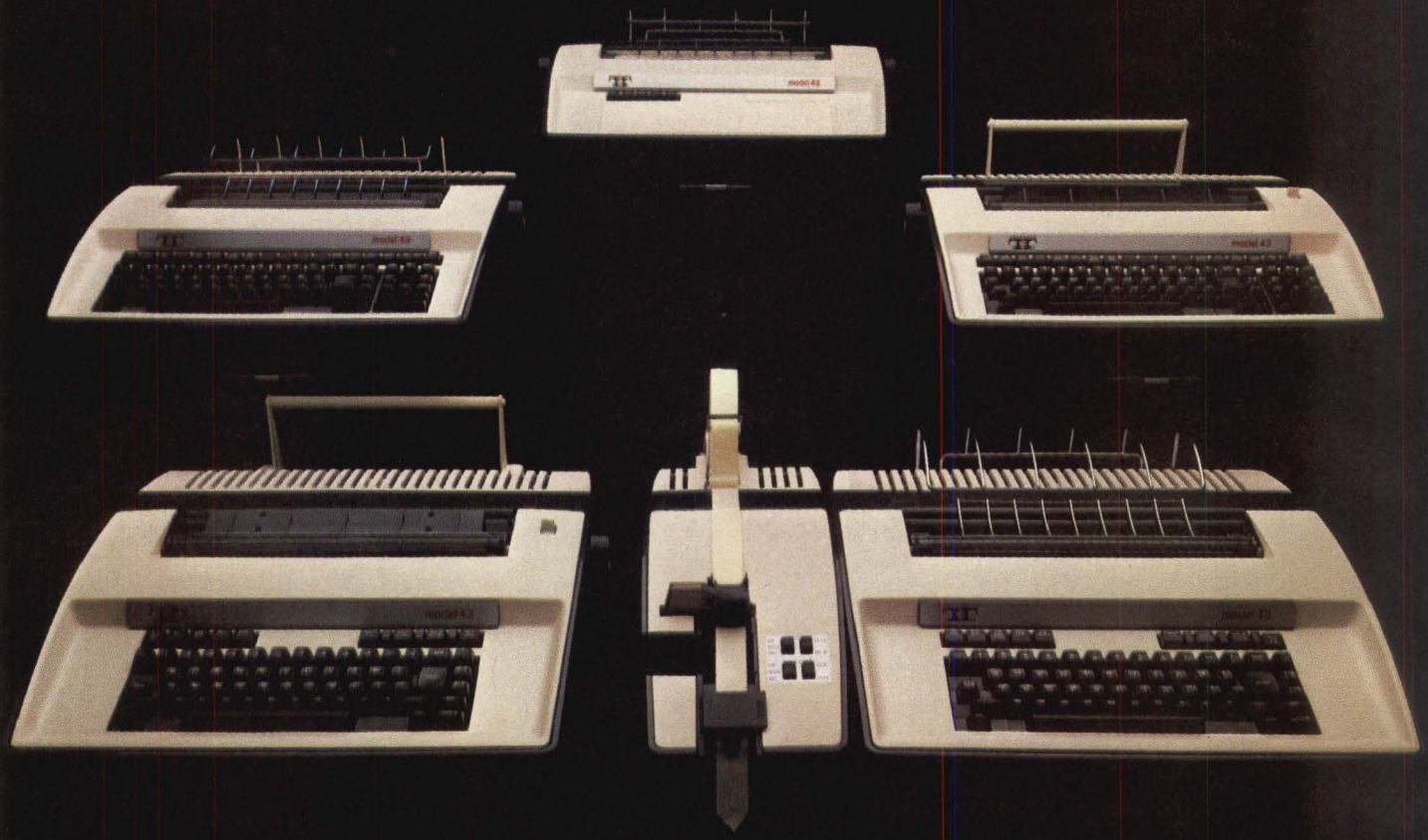


Z80 Direct Memory Access



Z80 Serial Input/Output





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CIRCLE 12 ON INQUIRY CARD

First of these concerns is that many of the basic legal precedents that have been achieved during the years since the Carterfone decision will be abandoned. There is no provision in the proposed legislation that assures that the principles of these past decisions, as adopted by the FCC or decreed by the courts, will continue to be recognized as being valid. There is a provision that all orders, rules, regulations, and grants of the present FCC that are not contrary to the proposed law would remain in effect until modified or repealed by the new Commission. The concern of this minimal assurance is that many settled principles could all be reopened to challenge, debate and redecision by the Commission.

A second concern is that the proposed legislation does not define clearly which telecommunications services or facilities are interstate and intrastate. The Act does state that the Commission has no authority "with respect to any intrastate telecommunications facility, or the provision of any service through the use of such facility." Without an interstate/intrastate definition, the above excerpt from the language of the proposed Act is subject to wide interpretation. The Act totally fails to address or resolve the question of predominate jurisdiction if a telecommunications facility is used for both interstate and intrastate telecommunications services. After many long judicial actions, such as in the North Carolina Utilities Commission vs FCC Decision of 1977, this jurisdictional question was finally resolved. The proposed legislation inadvertently reopens the question in an atmosphere of what appears to be more stringent language prohibiting the exercise of federal authority. While there are emphatic definitions of competitive standards, the Commission and any judicial decisions may be precluded if the telecommunications facilities or services are defined as under exclusive state authority. It is an expressed concern that customer-provided telecommunications equipment is not defined as interstate or intrastate within the language of the new bill. If it is interstate it may be classified as competitive or regulated by the Commission. If it is intrastate, each one of the 50 state public utilities commissions or equivalent agencies will decree the future viability of customer-owned telecommunications equipment within that state.

A third weakness identified in the proposed legislation is the absence of any provision for the enforcement of antitrust laws. Current decisions of the U.S. Supreme Court indicate a probability that the competitive standards contained in the Act may be accepted as substitutes for the antitrust laws. As such, the communications common carriers will be provided with implied immunity from liability under the antitrust laws. It may be properly suggested that the provisions of the bill attempt to preempt the antitrust laws with the proposed regulation.

Specifically, AT&T would be released from the constraints of its 1956 Consent Decree. It would permit communications common carriers to establish separate companies to provide telecommunications services and equipment incidental to telecommunications. AT&T and its operating companies would be free to enter into the computer and data processing equipment and service industries. These events would result in new organizations that would be easily capable of overshadowing presently established entities in those industries. The actual language of the bill with respect to this capability states that "notwithstanding any other provision of law, or any judicial determination or decree, any carrier can hold shares in, or acquire separate companies to engage in activities, provide services, or offer products which are in telecommunications or incidental to telecommunications."

It is expected that the separate corporation concept will automatically prevent cross-subsidization even though other provisions provide clear opportunities for predatory pricing. The Act appears to substitute the new Commission's authority for the Sherman and Clayton Acts as well as for federal government antitrust action as the determinant whether an activity, service or product constitutes telecommunications or is incidental to telecommunications.

It seems, therefore, that the proposed legislation is an attempt to respond to the growing competitive trend in the various telecommunications service and product industries. At present these emerging marketplaces are being constrained by traditional regulation provisions and requirements. The proposed Communications Act of 1978, however, appears to represent a swing to the other extreme of the regulation spectrum. If all participants could be expected to respond in an objective manner, with the common good as the accepted goal, such broad and almost trusting provisions would be feasible. In view of the realities, and of recent history in this arena, however, a more definitive and hence restrictive legislative posture is warranted. Existing giants in this telecommunications industry must be restrained and channeled through decreasing regulation until the many embryonic entities have been established as viable competitive factors in this marketplace.

During August and September 1978, the House of Representatives' Subcommittee on Communications held a series of hearings on the Communications Act of 1978 (H.R. 13015). A new draft of the legislation should be expected during the fourth quarter of calendar 1978. It is important that all members of the telecommunications industry take an active and visible role in the shaping of this legislation. It will determine the nature of the telecommunications industry in this country for the rest of this century and well into the next.

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Experimental Integrated Optical Device Promises Variety of Applications

Many signal processing applications in future lightwave communications and data processing systems may be served by an integrated optical device recently devised by scientists at Bell Laboratories, Murray Hill, NJ 07974. Its properties suggest use as a logic element in optical memories, a pulse shaper and limiter, an optical switch, a differential amplifier, and an "optical triode." It operates over a broad band of wavelengths at very low optical power, requiring only 1 pJ of light energy for the switching function.

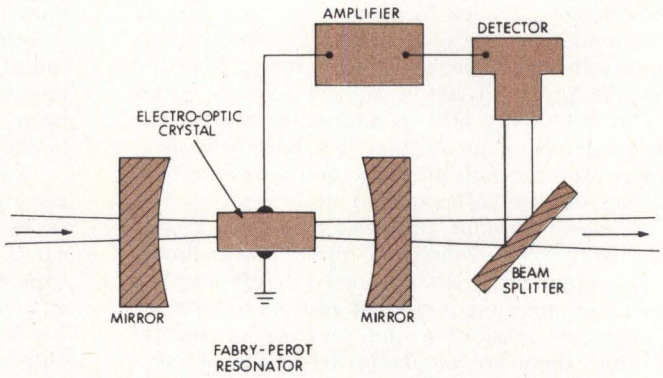
Nonlinearity is produced in the device, an optical waveguide version of a nonlinear Fabry-Perot resonator, by using the output of a photodetector, which samples the transmitted light, to drive an electro-optic lithium niobate (LiNb) element in the resonator. The unit's versatility is due to several properties: it accepts electrical or optical inputs; its nonlinearity may be modified using a nonlinear circuit; it can accept multiple inputs for optical logic operations such as AND or OR gates; and it enables multilevel operation, allowing more complex optical logic functions and A-D conversion of optical signals. It is expected that in the near future the electro-optic element can be driven with as little as 0.1 V, easily obtainable from a photovoltaic device without the need for amplification or for bias voltage.

Several modes of operation are possible with the device. The resonator can be tuned to produce an "S" shaped transmission characteristic, or one exhibiting optical hysteresis. Depending on the resonator tuning and the amount of feedback, the device can then be made to function as an optical memory element, complex logic element, optical limiter or optical triode.

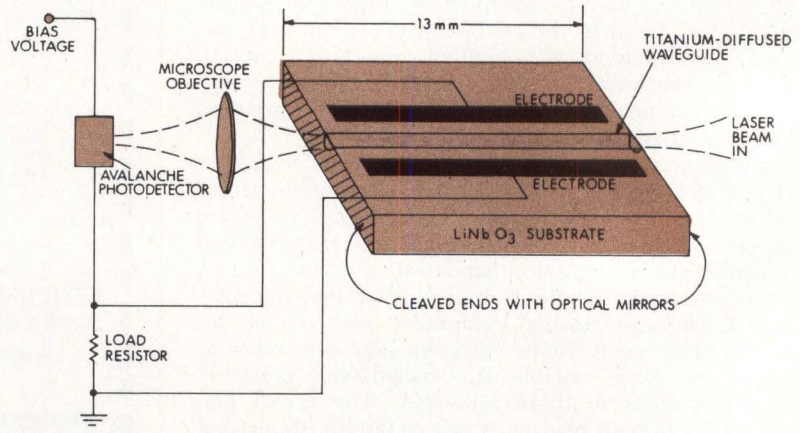
For complex multilevel logic operations, or A-D conversion of optical signals, high gain is required in the feedback loop. In this configuration, as many as 15 equally spaced levels of transmission are possible.

With less feedback and with the resonator tuned for transmission characterized by optical hysteresis, the device can function as a memory element. In this mode, switching between the two stable states—high transmission or low transmission—is accomplished either by an input light beam, or by applying an electrical pulse directly to the modulator electrodes.

After switching to the high transmission state, the output power remains almost constant over a wide range of input powers. In this mode, the device functions as an optical limiter. Output power rises steeply



Basic operation of experimental optical device. Incoming light is reflected back and forth between mirrors forming Fabry-Perot resonator. Beam splitter sends part of transmitted light to detector, whose output creates electric field between electrodes on electro-optic crystal. This field, varying with light intensity, modulates crystal's refractive index, producing nonlinear transmission characteristics



Integrated version. Device is fabricated using standard IC processing techniques. Titanium ions are diffused into electro-optic substrate of lithium niobate material to form 4-μm wide optical waveguide. Fabry-Perot resonator is formed with dielectric mirrors expoxied onto cleaved ends of substrate material

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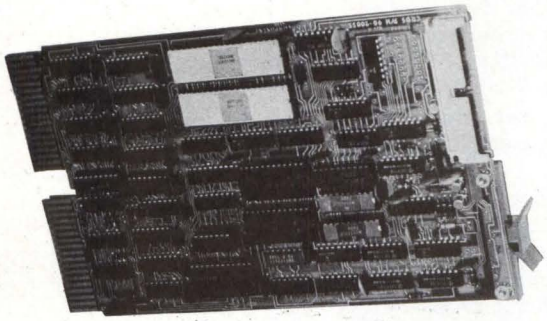

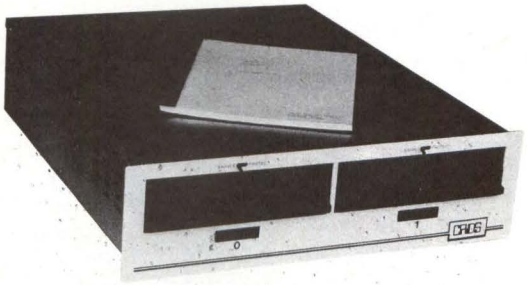

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CIRCLE 14 ON INQUIRY CARD

to a maximum point and then levels out, with little increase in output power as the input power is increased. Output power varies less than 4% for a 15:1 variation in input power.

As an optical triode, the resonator is tuned to produce the "S" type transmission characteristic, and optical power transmitted through the waveguide changes rapidly as a function of incident light. This means that a small additional light signal at the detector produces a large change in transmitted light power. In an experiment with a low level control light beam, a sevenfold gain was measured.

Researchers at the laboratories are looking to longer wavelength light to eliminate unwanted refractive index changes due to photorefractive effects in the LiNb. They expect the fully integrated version to operate with a response time of several ns, and to switch with only a few picojoules of optical energy.

Nationwide Network Service Available for 1200-Bit/s Data Terminals

Nationwide packet network data communications service for terminals operating at 1200 bits/s is being provided by Telenet Communications Corp, 8330 Old Courthouse Rd, Vienna, VA 22180. The expanded public dial-in facilities support the new Bell 212 and Vadic 3400 full-duplex modems, and is available locally in selected major cities, as well as nationally through a central WATS number.

Cities in which public 1200-bit/s service is available include Atlanta, Boston, Chicago, Dallas, Detroit, Honolulu, Houston, Los Angeles, Newark, New York, Philadelphia, San Francisco, and Washington. According to the company, expansion of the service is due to a survey among the more than 225 organizations using the network for computer communications. Results showed a growing preference for the 1200-bit/s rate because of higher throughput and lower costs compared with lower speed terminals, both for data processing and communications.

Laboratory Lasers/LEDs Show High Performance As Optical Transmitters

In the laboratories of Siemens AG, Postfach 103, D-8000 Munich 1, Federal Republic of Germany, both semiconductor lasers and light-emitting diodes (LEDS) have been developed for use as optical transmitters over optical fiber transmission lines. In this application adequate optical power, long service life, and only slight variation of optical parameters are essential properties.

The researchers have found that semiconductor lasers have two basic advantages: they launch a larger optical power into the fiber, and can be modulated with higher frequencies. This only holds true, however, if the lasers are designed as optical semiconductor resonators, so that only the fundamental mode is excited. Stripe-geometry lasers with narrow stripe width fulfill this requirement. At stripe widths of 6 μm, the research laboratory devices provide cw optical output powers of 6 mW.

With LEDS, an optical power of 4 mW at diode current of 100 mA has thus far been achieved. Emission wavelengths of between 800 and 900 nm can be realized by selection of a suitable crystal composition.

The stripe-geometry lasers are GaAs/GaAlAs double heterostructure laser diodes with stripe widths between 6 and 13 μm. They have alumina anti-reflection coatings that permit a high mirror load of 1-mW optical output power per 1-μm stripe width.

On selected samples, threshold current rose by only 3% in the course of 1000 h at 80 °C amb temp. Extrapolation of these data shows that at room temp, such diodes should expect a service life of 100,000 h. This calculation is based on an activating energy of 0.7 eV and a 10% max permitted threshold current rise. How much the other operating parameters will change over such a period remains to be seen.

In early experimental applications a laboratory PCM transmission system showed a pulse amplitude variation of only ±3% at a transmission rate of 560M bits/s, and at the Heinrich Herz Institute for Telecommunications in Berlin, the diodes displayed good modulation performance at 1.2G bits/s.

Circle 400 on Inquiry Card

Modules Offer Interactive Communications for Distributed Systems

3270 display station emulator, intelligent 3270 network interface, and 3270 batch utilities package, allow users of System 21 family of distributed data processing systems choice between designing applications for interactive inquiry into a remote host system, batch transmission to the host, or a combination of local processing with interactive inquiry against local or remote files. With the new capabilities, asynchronous communications are enabled on all three series 21 models, while the 21/40 or 21/50 can also emulate terminals in the IBM 3270 family, according to Mohawk Data Sciences Corp, 1599 Littleton Rd, Parsippany, NJ 07054.

Basic asynchronous emulator, available first quarter 1979, allows operator stations to function as nonintelligent conversational terminals, transmitting data to or receiving data from a mainframe char at a time or in batch mode via diskette or disc. An enhanced version of the emulator, (initial delivery third quarter 1979) adds data formatting, operator prompting, and variety of CRT display functions, supported by MOBOL (Mohawk Business-Oriented Language) routines. MOBOL programs can interact with host processor programs for direct data input and information retrieval. Batch utilities package, also available in third quarter 1979, allows system users to transmit data to host via 3270 protocol with minimum operator intervention. □

Circle 401 on Inquiry Card

Planned planar-hood info.

See page 81

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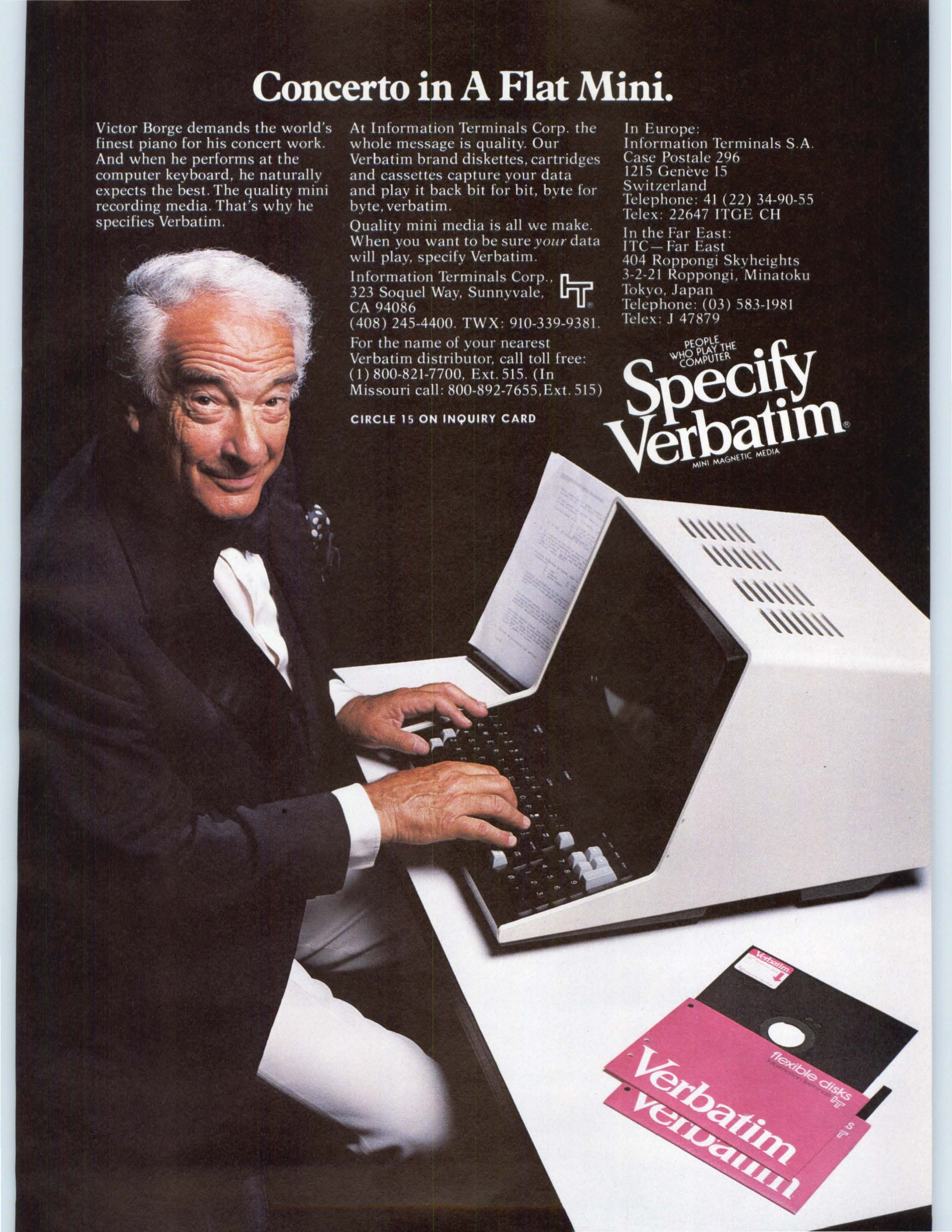
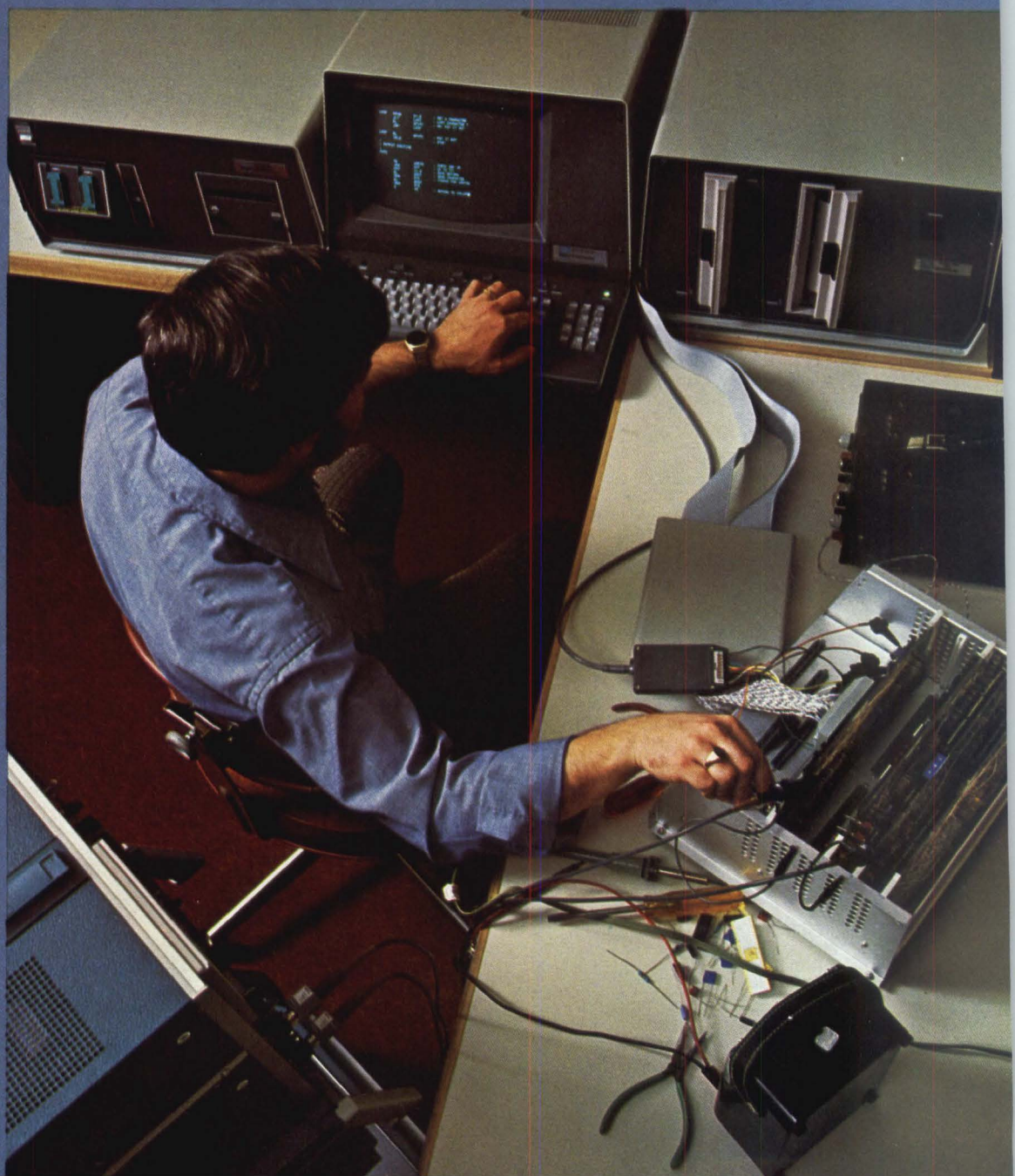


Ever try to find a once-a-week glitch among half a million operations per second?



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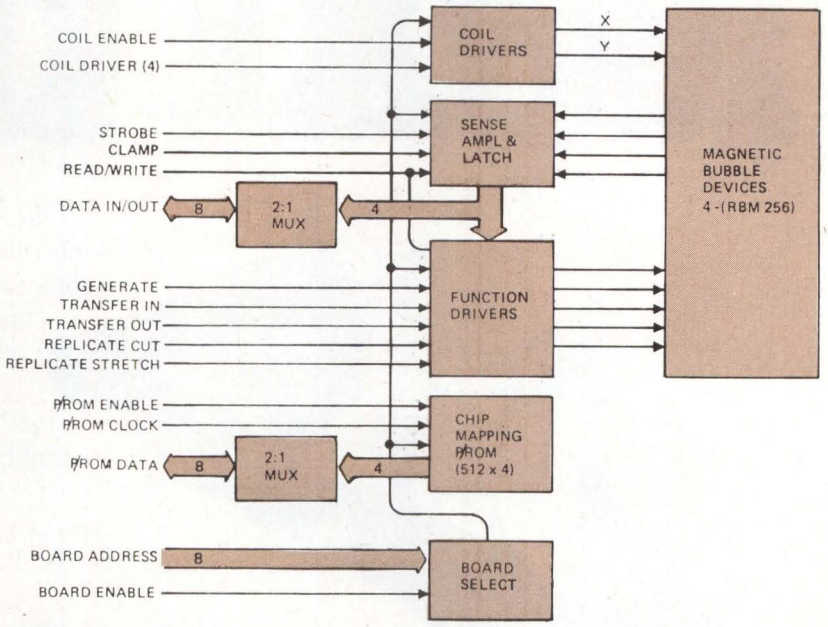
CIRCLE 18 ON INQUIRY CARD

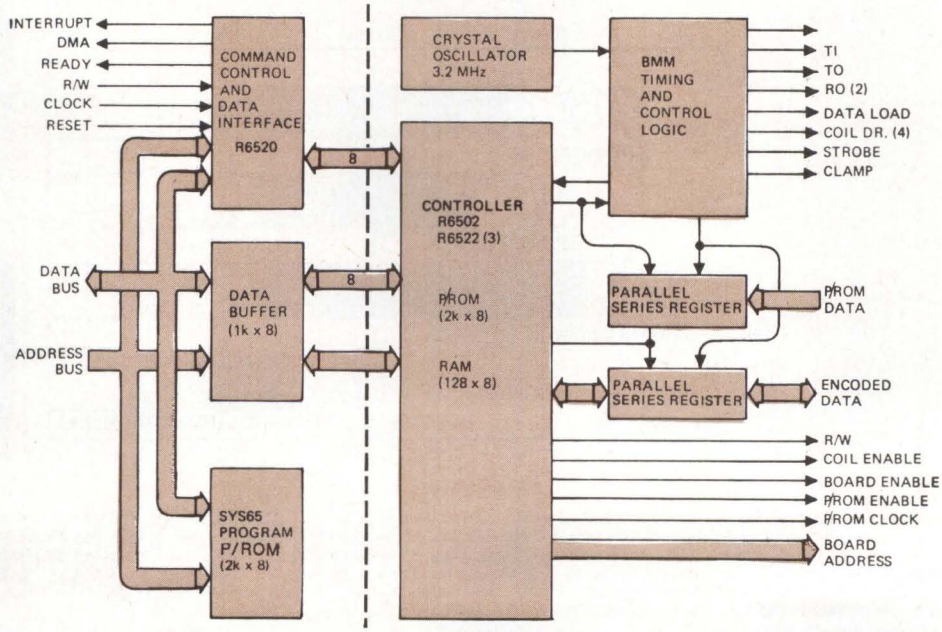
Bubble Domain Memory Devices and Subsystems Based on 256k-Bit Chip

RBM256, a mass-produced binary organized device capable of storing 256k bits of data, is the basis of bubble memory devices and subsystems introduced by Rockwell International, Electronic Devices Div, 3310 Miraloma Ave, Anaheim, CA 92803. RLM658, a linear module, contains four RBM256 devices, thus forming a 1M-bit system on a board. Programmable control module RCM650 controls from 1 to 16 of the linear modules and enables storage capacities of from 128k to 2M bytes. Also available is a development system made up of two linear modules, a programmable control module, and a System 65.

Composed of 282 loops, each containing 1025 bubble positions, the RBM256 operates with a 260-bit data block, thus using only 260 of the available 282 loops. Binary data are stored in 256 loops and the remaining four hold system housekeeping bits. In a typical application where eight RBM256 devices are used in parallel, extra bits may be used to provide a 16-bit block address header and a 16-bit CRCC word suffix. The device transfers data at 150 kHz, taking less



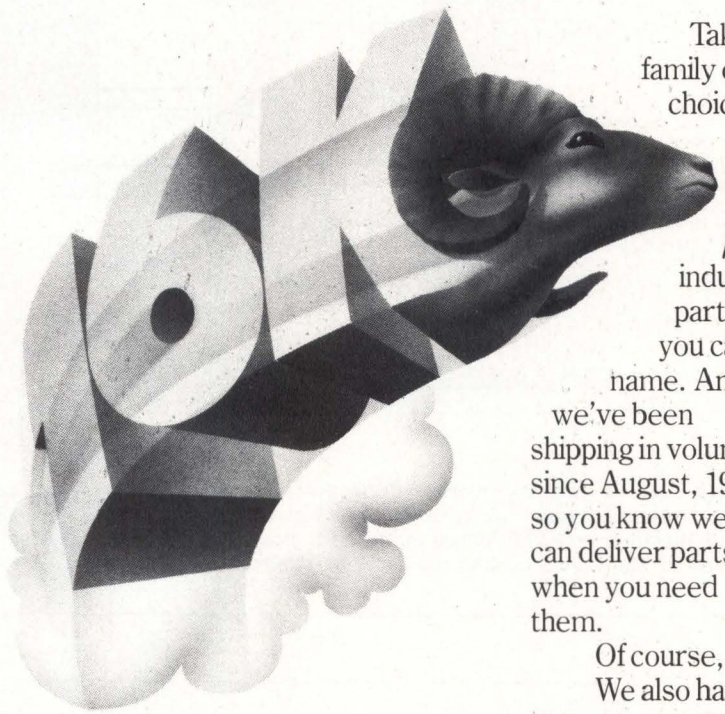
Linear bubble memory module from Rockwell packages storage devices with sense channels, coil drivers, and operator logic needed for support. Chip mapping P/ROM retains good/bad loop maps, used by system controller to skew and deskew block data streams



Controller module supports up to 16 of Rockwell's linear bubble memory modules, forming cost-effective subsystem. Circuits to left of dashed line provide System 65 compatibility, those on right service bubble memory devices

Who do you think of for high-performance 16K RAMs?

Next time,



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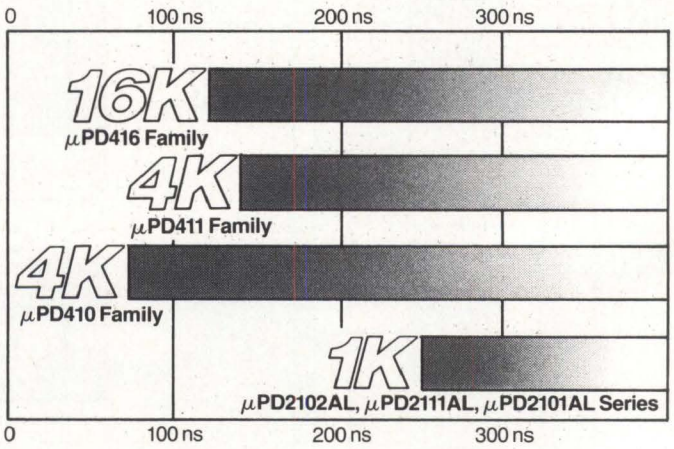
μPD416-3	150 ns	375 ns	35 mA	1.5 mA
μPD416-2	200 ns	375 ns	35 mA	1.5 mA
μPD416-1	250 ns	430 ns	35 mA	1.5 mA
μPD416	300 ns	510 ns	35 mA	1.5 mA
$t_a = 0°C$ to $+70°C$				

Of course, 16K RAMs are just part of our story. We also have a broad selection of other memory components, led by our industry standard



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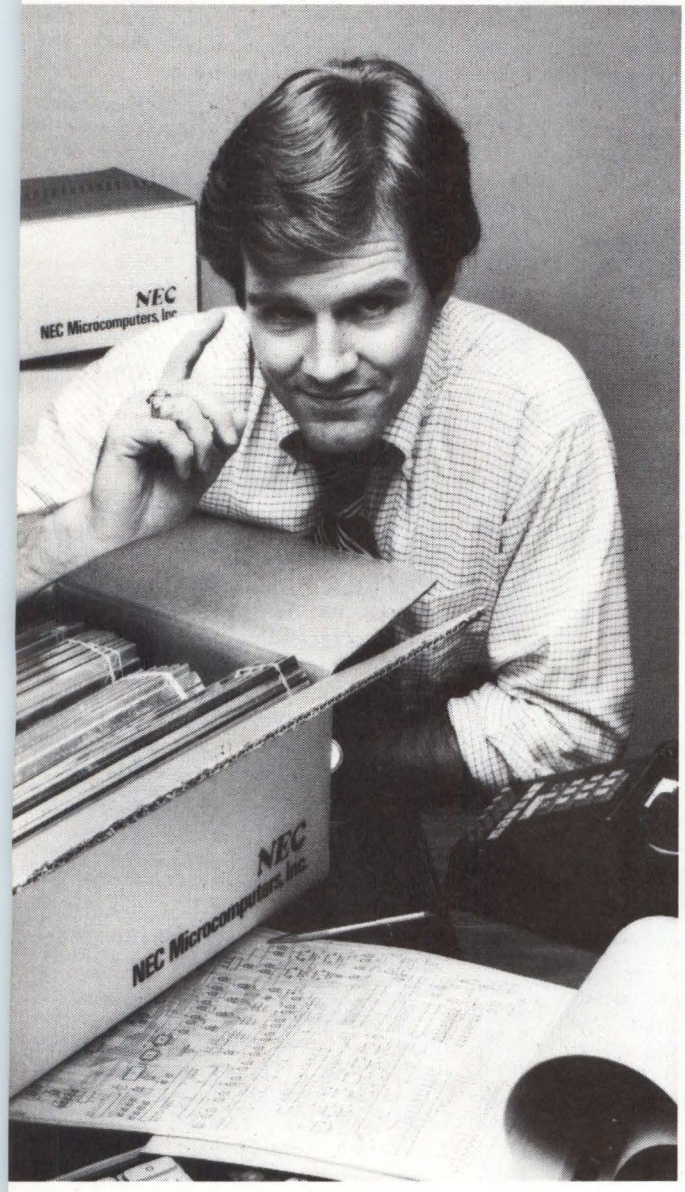

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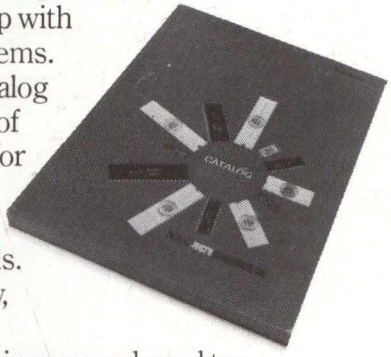

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CD-2-1

than 4 ms to access the first bit of a block. Throughput is preserved during read operations with the device's replicate/read block architecture in which bubbles read at the detectors are actually duplicates of the loop-resident bubbles.

Packaged in an 18-pin, molded plastic DIP, the RBM256 occupies only 1.2 x 1.2" (3.05 x 3.05 cm). It consumes 820 mW of power, and offers −10 to 70 °C case temperature operation.

A prepackaged linear module that provides 1M bits of storage using four parallel RBM256 devices, the RLM658 operates at 100k bytes/s and, when used in conjunction with an appropriate controller, is compatible with the company's System 65 and many 6800 microcomputer development systems. The RLM658 is designed to be used in combinations of two to 16 modules in a byte oriented system environment, providing from 256k to 2M bytes of storage.

To implement a bubble memory subsystem based on linear bubble memory modules, controller circuitry is required. The RCM650 complements the 1M-byte RLM658 linear module in System 65 applications, providing byte-parallel operation in 256-byte blocks. It is totally software compatible with System 65 and the 6502 microprocessor, and can control from 1 to 16 RLM658 modules.

The RCM650 bubble memory controller and the RLM658 linear module are designed to form a cost-effective subsystem. The RCM650 controller supports up to 16 RLM658 modules, allowing system capacity to be expanded up to 2M bytes.

A 256k-byte bubble memory subsystem option (one RCM650 controller and two RLM658 linear storage modules) installed in a System 65 microcomputer development system, allows users to begin developing applications for the bubble memory devices. A powerful microcomputer development system based on the R6502 CPU, it comes standard with two minifloppy disc drives and 16k bytes of static RAM (both totally user-dedicated), plus ROM-resident debug, monitor, symbolic text editor, and 2-pass assembler programs. It includes vacant slots for adding additional memory and I/O modules; an auxiliary card cage permits expansion to the full 2M-byte bubble memory subsystem capability.

Low quantity price for the 256k-bit device is $500 each; linear module is priced at $2500; and programmable control module at $1000. Development system cost is $11,400. Delivery is said to be 60 to 90 days.

Circle 180 on Inquiry Card

Logic Analyzer Solves Problems of High Speed Logic Circuit Probing

Matching high performance timing mode analysis with a comprehensive set of display and decoding capabilities for data domain analysis, the K100-D is claimed to set a standard for troubleshooting at the digital design level. Integrated in the 100-MHz, 16-input channel logic analyzer developed by the Biomation Div of Gould Inc, 4600 Old Ironsides Dr, Santa Clara, CA 95050 are a microprocessor (MC6800) controlled subsystem, CRT display, and full user oriented keyboard for specifying complicated triggering and recording sequences.

Access to the control subsystem is via the front panel keyboard and four front panel switches. Input is via probe sets that feature two 10-input connections at the instrument, and custom hybrid circuits for each active probe. Designed with a limited

Biomation's K100-D logic analyzer provides access to its microprocessor based control subsystem through front panel keyboard and four front panel switches. Menu displayed on integral CRT eases user comprehension of unit's functional capabilities

number of functions per key and a related display menu that speeds the user's comprehension of its function capabilities, the keyboard permits the user to move rapidly into full utilization of the unit's performance characteristics.

The unit's memory is 16 bits wide by 1024 words long, and data clocking into memory can be achieved at rates up to 100 MHz (giving 10-ns time resolution) by way of the internal clock. When an external qualified clock is used, information is clocked at up to 50 MHz. These clock rates make the instrument adequate not only for TTL and ECL circuits, but also provide better timing resolution for measuring critical operating parameters of current and future microprocessors. In addition, with the appropriate accessory, the analyzer can synchronously record from 32 channels without compromising basic performance. The full 16-channel, 100-MHz capability can be used by merely interchanging the 32-channel adapter with the high performance probes.

To reduce the difficulties encountered with reflections and ringing, changing input capacitance, and crosstalk when attempting to get input signals down to 10 ns, probes for use on the K100-D combine features of active pod and individual probes rather than using active probe pods on a multiconductor cable. This approach processes signals close to the user's circuitry to preserve the signals' information content. The probe's hybrid circuit provides buffering for a 1-MΩ input impedance, and threshold detection right at the probe tip. The probe assembly is made up of groups of 10 probes each, all terminated in a common conductor. Plugging in two 10-probe connectors joins 20 probes to the instrument. With individual active probes it adds ability to probe physically distant circuit points.

High performance is augmented by a versatile control subsystem that allows the designer to easily set and access all recording and display parameters. To initiate a recording sequence, the status display is consulted on the CRT screen. Access to a particular field is gained by pressing the corresponding key, then entering the desired parameter. Various decisions can be made about clocking, delay sequence, logic polarity, 2-level trigger, threshold, input mode, arm mode, and trigger. Because there are buttons on each parameter field, parameters can be selected in any sequence desired.

All recording sequences can be monitored, and information analyzed, by way of a comprehensive set of display prompters. There are four separate display modes for data domain, and a timing domain display. All 16 channels of data can be viewed simultaneously. Data domain outputs can be presented in binary, hexadeci-

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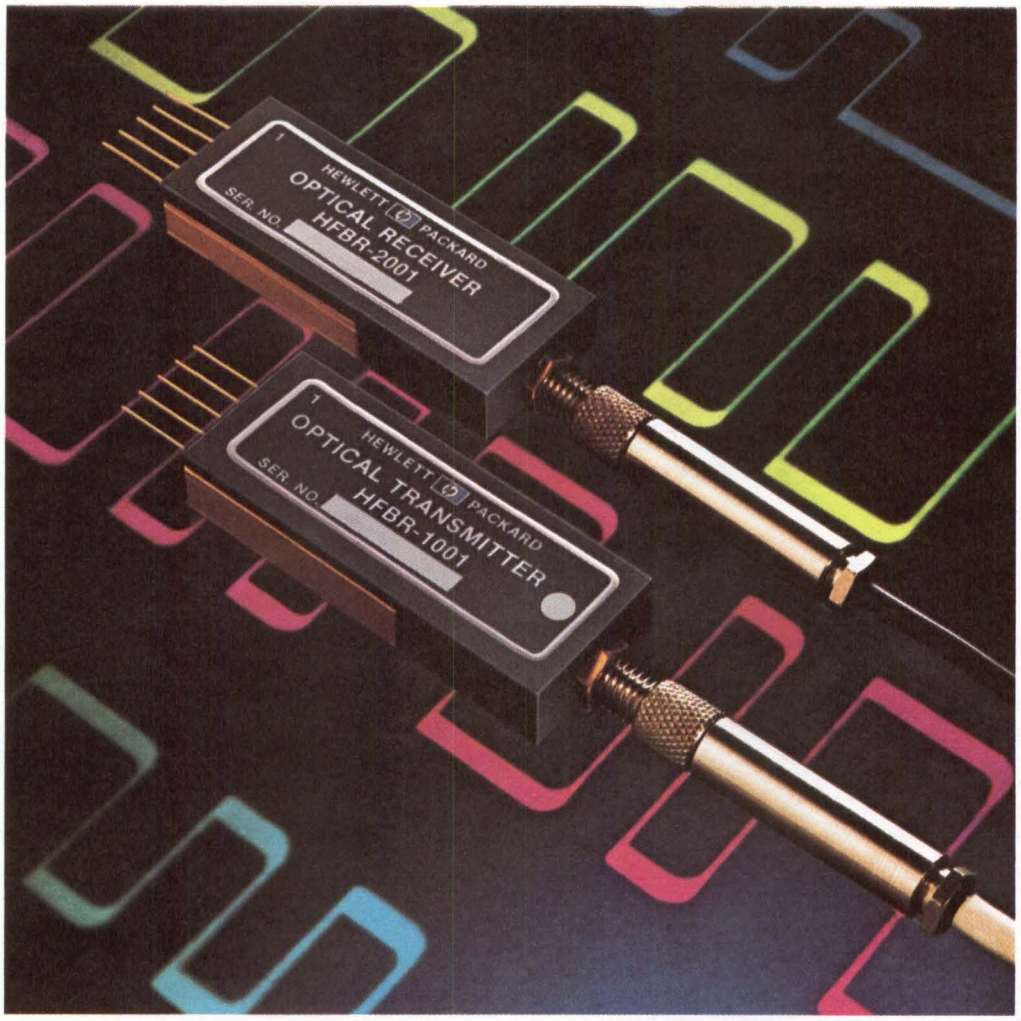


The Data Link of the future is available from HP today.

HP's new Fiber Optic System guarantees error free ($P_e < 10^{-9}$) data transmission from DC to 10Mb/s NRZ over distances up to 100 metres. This system is immune to electromagnetic interference, radiates no external signal and provides total electrical isolation between terminals.

TTL compatible, our system includes a PC board mountable transmitter and receiver which operate from a single 5V power supply. Our low loss, single fiber connector/cable assemblies are available in five standard lengths from 10 to 100 metres.

Applications include large computer installations, distributed processing, power plants, process controls and remote instrumentation.

Prices start at $570 for the HFBR-0010, 10 Metre System.

For more information or immediate off-the-shelf delivery, call any franchised HP distributor. In the U.S. contact Hall-Mark, Hamilton/Avnet, Pioneer Standard, Schweber, Wilshire or the Wyle Distribution Group (Liberty/Elmar). In Canada, call Hamilton/Avnet or Zentronics, Ltd.

*U.S. Domestic Price Only.

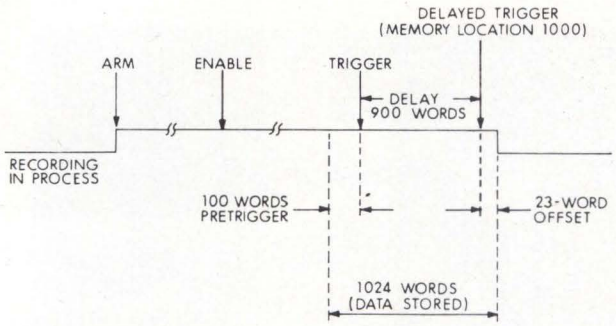
01806

HEWLETT hp PACKARD

1507 Page Mill Road, Palo Alto, California 94304

For assistance call: Washington (301) 948-6370, Chicago (312) 255-9800, Atlanta (404) 955-1500, Los Angeles (213) 877-1282

CIRCLE 19 ON INQUIRY CARD



Three events in sequence are required to complete recording using K100-D logic analyzer. Arm initiates storage of data into memory; trigger controls what is stored. However, enable must be detected before trigger can be recognized. 23-word offset simplifies set up by reconciling difference between 1000 decimal and 1000 binary (1024)

mal, or octal form, as well as a special mode. In special mode, information display can be split to view, for example, 8-bit data bytes in hexadecimal, plus 8 bits in hexadecimal. Other combinations include one which decodes information in binary and ASCII code. Sequence comparison capability allows users to compare 1 word, or up to 1024 words between the two memories.

The K100-D is available on a 90-day ARO schedule. Price is $8800 including two probe sets.

Circle 181 on Inquiry Card

Disc Storage System Doubles Capacity of 3350 Units

An enhanced Winchester technology disc storage subsystem provides 1.27G bytes of data storage capacity in each 2-spindle cabinet. To effectively double the storage capacity of competitive units, Control Data Corp, Box O, Minneapolis, MN 55440 increased the number of data surfaces and recording heads in each sealed data module by one-third and packed a greater number of data tracks on each surface, increasing track density on each data surface to 662 tracks/in. This increased density also improves performance by reducing average access time for 317.5M bytes to 19 ms.

The fixed media device replaces two IBM 3350 units in storage capacity using a two logical volume/spindle concept. It is totally functionally compatible with that unit and completely transparent to all software operating systems that support the 3350. Disc units are connected to the 38302 universal storage controller which also operates IBM compatible 100M- and 200M-byte drives. Use of the controller allows drives of various capacities to be intermixed in each string for configuration flexibility. The unit also attaches to an IBM storage control unit.

The 33502 incorporates the field proven dynamic dual access option to provide an additional level of redundancy as well as improved throughput that results from minimized contention and maximum data availability. Dual access is accomplished by allowing a second unit to access each disc drive. With dual access, data can be written or read simultaneously from two different spindles in the same drive string, through a second storage control unit. In large configurations dual access can be combined with string switch. String switch allows a second storage control unit to gain access to a string of drives, while still limiting data transfer to a single spindle at a time.

Available in six different models, some representative prices for the 33502 are $59,600 for model A2 that includes two drives and data modules, and control adapter unit. With 3.4M bytes of optional fixed head storage (model A2F) price is $72,350. Models B2 and B2F attach to A2 units and are priced at $50,256 and $63,000, respectively. C2 and C2F include a backup control adapter unit and are priced the same as A2 models.

Circle 182 on Inquiry Card

Data Acquisition Unit Offers Continuous Input Without Bandwidth Limits

A data acquisition peripheral for the PDP-11 series computer, the MIP-3/A (micro input processor/analog) is an intelligent analog-to-digital converter. It consists of a Unibus™ interface, data acquisition subsystem, expandable buffer memory, and a sophisticated input processor, and features 16 to 64 single ended channels that can handle 12 bits at 100-kHz throughput rates.

The unit, designed by Computer Design and Applications Inc, 377 Elliot St, Newton, MA 02164, addresses two problems associated with currently available A-D systems: that of continuous data acquisition and the limiting effect of bus bandwidth. In a programmed I/O A-D system, the host processor spends much of its time servicing the A-D unit, thereby limiting the bandwidth available for processing and acquisition. A DMA A-D solves the main acquisition problem but still requires fast CPU response whenever a buffer is filled, placing a severe bandwidth limitation on the system.

The micro input processor resolves this problem by assuming that data are double buffered and by issuing two sets of control parameters, making the second buffer's parameters available as soon as the first buffer is filled. By so doing, the host response time becomes the time spent filling an entire buffer rather than a single sample interval. The problem of bus bandwidth is resolved by placing a dual port memory in the unit.

The data acquisition subsystem is a packaged module which includes an input multiplexer, sample/hold amplifier, and 12-bit high speed A-D con-

CIRCLE 20 ON INQUIRY CARD →

SAMPLE: EASILY REMOVED
FOR YOUR FILES

Ball

The BD Series.

The first disk drive family you'll want to label as your own.

Everything an OEM will ever need in disk drives.

Ball Computer's BD series of disk drives sets new standards for reliability, accessibility and maintainability for the OEM. The BD series, which includes storage module units of 50 megabyte (BD-50) and 80 megabyte (BD-80) capacities, satisfies the OEM requirement for large capacity disk files to interface with small and medium size computers in applications where trouble free performance is critical. Available in either rack mount or console mount configurations, the BD series combines, proven drive technology with features that insure superior reliability and maintainability.

Easy Maintenance

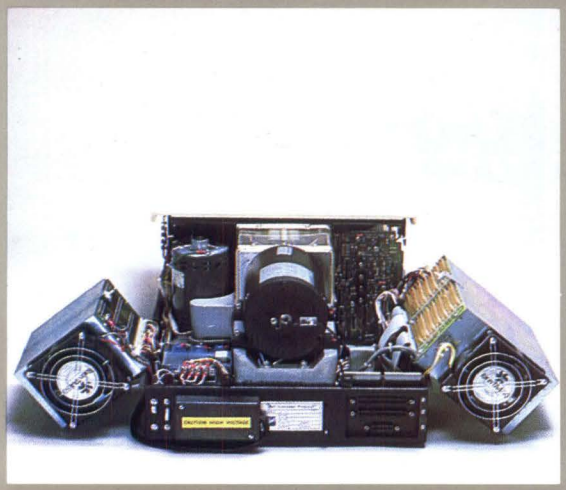
The BD series of disk drives is designed to speed preventive maintenance, simplify trouble-shooting and repair in the field. The drives incorporate a removable 3330-type short stack disk pack. Deck plate, logic and power chassis are hinged and can be "butterflied" out from the top and sides for instant servicing, cleaning and adjustments. The drives are fully modular using separate chassis for actuator and motor control mechanisms, power supply and logic. All electronic circuitry is on plug-in boards, arranged in functional groupings and provided with built-in test points. All critical parts, including voice coils and heads, are standard assemblies available from multiple sources, and field proven in thousands of installations.

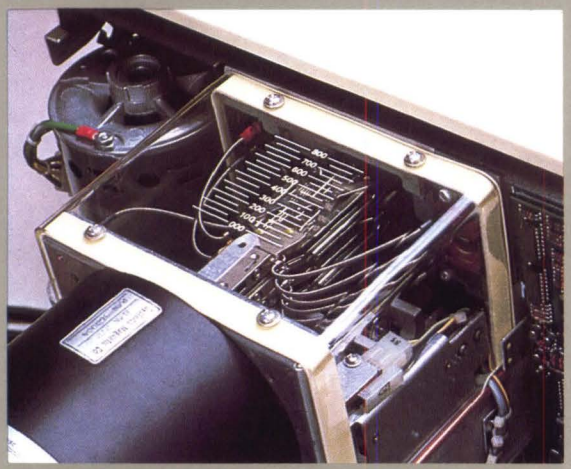
High Data Reliability

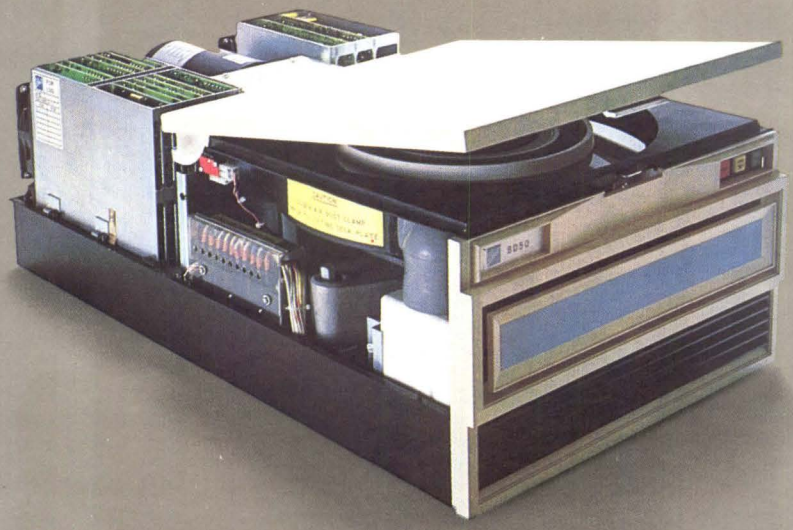
To provide the highest possible data reliability, protective features are incorporated in all critical areas. All moving parts in the actuator and disk pack well are sealed in a "clean room" environment. This environment extends from the disk pack shroud along the entire length of the carriage and ways. Protecting both the disk pack shroud and actuator prevents possible contamination of the disk surfaces during periods when the heads are retracted and power is shut down. This eliminates, most of the reasons for loss of data; dust and dirt accumulation on precision mechanisms and the disk surfaces. Moreover, the use of a constant voltage power supply reduces premature component failures and susceptibility to recording errors resulting from line-power variations.

Self-Diagnostic

When a BD disk drive repaired, it tells you v the operator in locati system when it is in ne series disk drives feat diode (LED) displays to isolate the failure r interface, read, write When the system det internal latches moni light the easily obser on the chassis next to circuits. The operator from the front panel b only be over-ridden b cover and pressing th next to the LED indic







Operation

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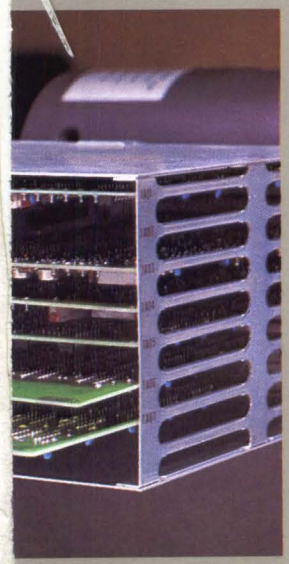
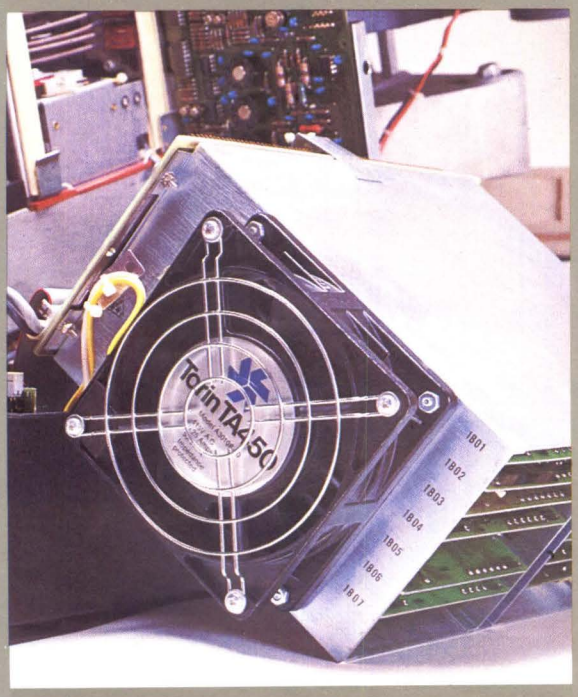


Highly Reliable

For increased reliability, the industry's first triple cooling system in a compact design has been incorporated into each BD Series unit. One fan cools the logic chassis to eliminate hot spots in the circuitry that cause premature component failures. Another fan cools the power supply and servo drivers. The third circulates cool, clean air through the absolute filter to the disk pack shroud and all moving parts. As a result, Ball's unique cooling system design greatly reduces device failures.



...And More

The list of features from Ball is almost endless. For example, the absolute air filter can be easily accessed by raising the deck plate to the maintenance position. The filter is mounted in a frame and can be lifted out by merely loosening a single locking bolt—a simple five minute operation.

Additional features include:

- a track following servo system with no external reference required;
- field upgrade capability from 50 to 80 megabytes;
- interface compatibility with the CalComp Trident TD-50/80, CDC 9760/62, or Ampex 940/980; and
- static discharge immunity up to 4 kilovolts.

Other disk drives may have some of the features you need, but only the Ball BD series has all of them.

Specifications

BD-50

STORAGE CHARACTERISTICS

Read/Write Surfaces	5
Tracks per Surface	815
Tracks per Inch	370
Recording Method	MFM, BIT SERIAL
Data Transfer Rate (at 3600 RPM)	806 Kbytes/sec.
Bits per Track (maximum including header and gaps)	107,520
Bytes per Track	13,440
Bytes per Pack (unformatted)	54.7×10^6

BD-80

STORAGE CHARACTERISTICS

Read/Write Surfaces	5
Tracks per Surface	815
Tracks per Inch	370
Recording Method	MFM, BIT SERIAL
Data Transfer Rate (at 3600 RPM)	1.2 megabytes/second
Bits per Track (maximum including header and gaps)	161,280
Bytes per Track	20,160
Bytes per Pack (unformatted)	82.1×10^6

BD SERIES (Applies to both BD-50 and BD-80)

PERFORMANCE CHARACTERISTICS

Positioning Technique	Continuous track following servo controlled linear motor
Access Time (maximums)	
Track to track (adjacent)	5 milliseconds
Maximum tracks (0 to 814)	55 milliseconds
Average access time	30 milliseconds
Pack Rotational Speed	3600 RPM ±3%
Latency Time	16.7 milliseconds
Start Time	20 seconds
Stop Time	20 seconds

POWER REQUIREMENTS

AC Power Voltage	115(±17)VAC, 60(±.6)Hz, 1 phase 220(±35)VAC, 50(±.5)Hz, 1 phase
Running Current	7.5 AMP (115VAC @60Hz) (Seeking)
Starting Current	22.5 AMP (115VAC @60Hz) (For 10 seconds)
Standby Current	2.5 AMP (115VAC @60Hz)

PHYSICAL CHARACTERISTICS

Height	10.5 inches (26.7 cm)
Width	17.5 inches (44.5 cm)
Depth	31.5 inches (80.0 cm)
Weight	180 pounds (81.6 kg)

ENVIRONMENTAL LIMITS

Operating:	
Temperature	60°F to 90°F (15.4°C to 31.9°C), with a maximum gradient of 12°F (6.6°C) per hour
Humidity	10% to 80% noncondensing
Non-operating:	
Temperature	−40°F to +150°F (−39.6°C to 64.9°C), with a maximum gradient of 36°F (20°C) per hour
Humidity	5% to 95% noncondensing

ADDITIONAL STANDARD FEATURES

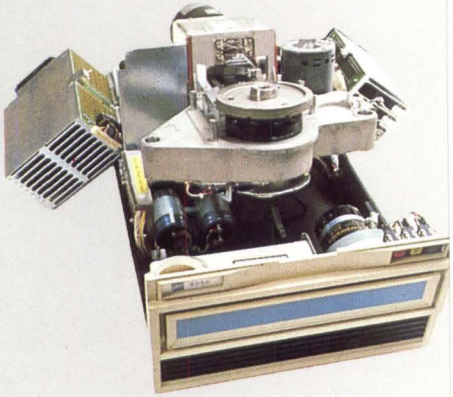
Address Mark Detection
Variable Sector Sizes
Sector Address/Cylinder Address Read Commands
Uniform cooling with individual fans per electronic chassis

OPTIONS

Rack or Pedestal Mounting	
NRZ Data Interface	
Signal Cables	7, 10, 15 or 25 feet (2.13, 3.05, 4.57 or 7.62 meters)
Read/Write Cables	7, 10, 15 or 25 feet (2.13, 3.05, 4.57 or 7.62 meters)

ALSO AVAILABLE

Ball Comprehensive Controllers with error correction, variable record length and multiple drive capability
CPU Interfaces for various minicomputers



Computer Products Division

860 East Arques Avenue, Sunnyvale, California 94086
(408) 733-6700

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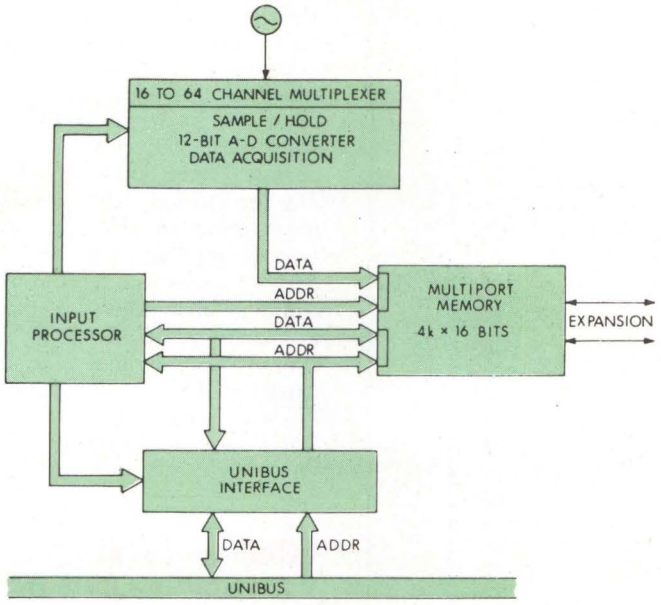


MIP-3/A, intelligent data acquisition peripheral, provides continuous data acquisition without bandwidth penalty. Developed by Computer Design and Applications, unit's 16 to 64 single-ended channels can handle 12-bit input at 100-kHz rates

verter. Maximum throughput rate is 100 kHz.

Buffer memory is implemented with high speed static MOS RAM. It is dual port memory which may be accessed by a Unibus master and is also accessible by the ADC in conjunction with the input processor. Any size window of any port of memory may be placed anywhere on the Unibus by setting appropriate switches. Basic memory size is 4096 16-bit words; this is expandable to a maximum of 65,536 words with the addition of MIP-3/ME memory expander cards. When not in use for A-D acquisition, the memory behaves as normal system memory and may be used for running operating systems, program development, or FORTRAN programs.

Input processor controls the data acquisition subsystem and provides memory addresses for writing A-D data into the buffer. It may also request interrupts from the host CPU. A microprogrammed device, the input processor is controlled by a set of registers located in the I/O page of the PDP-11 address space.

The PDP-11 system communicates with the -3/A by reading and writing either the buffer memory for data or the device register block for control information. The -3/A communicates with the -11 processor by initiating interrupts. Since the -3/A is a microprogrammed machine, the format of the DRB and actual operation of the machine are a function of the microprogram contained in onboard P/ROMS. A standard unit is configured as a multichannel double buffered data acquisition system.

While the -3/A has 16 channels standard, it expands to 64 single-ended or 32 differential channels with addition of an MIP/AE channel expander which mounts on the -3/A. Memory expansion units MIP-3/ME cards each contain an additional 16k x 16 bits of MOS memory. Up to four can be added to the -3/A.

The -3/A occupies one hex SPC slot in a PDP-11 system unit. The necessary −5-V power is supplied by the host. An onboard dc-dc converter provides voltages for the analog circuits.

Circle 183 on Inquiry Card

CCD-Based Disc Replacement Stores 11.2M to 45M Bytes

Faster, better performing, and less expensive than fixed head systems, the 4305 solid-state disc is based on a 65k-bit, CCD device, and ranges from 11.2M to 45M bytes in capacity. In developing the unit, Storage Technology Corp, 2270 S 88th St, Louisville, CO 80027 designed in plug compatibility with large IBM systems and provided the ability to emulate the 2305 fixed head disc subsystems.

Device access time is 0.7 ms; max access is 1.4 ms. Transfer rate is selectable at 1M or 1.5M bytes/s. Variable transfer rate allows the device to be shared between multiple CPUS having different channel speeds. Optional features include dual ports, 2-channel switch, and 3M-byte transfer rates.

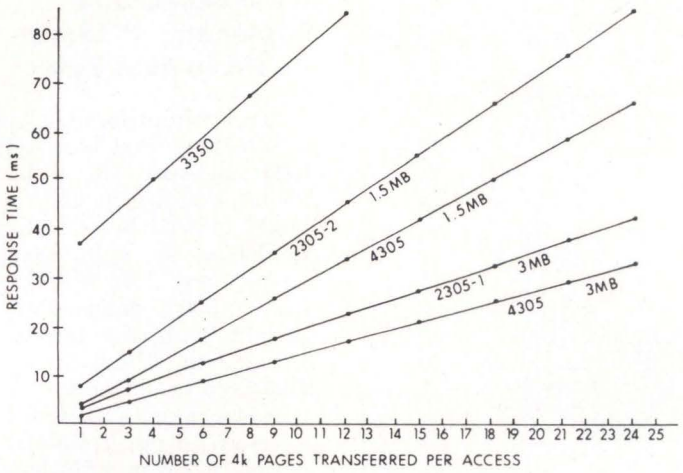
Storage modules consist of 12M bytes of CCD memory packaged on 12 PC boards and organized as 72 rows and 24 columns. Each CCD is organized as 16 serial shift registers (loops), each containing 4096 bits.

During a single clock cycle one bit can be read out or written into each of the 16 loops. All loops are continuously and synchronously recirculating. A bit cycles through a loop in 1.4 ms; providing an average access time of 0.7 ms.

To read data, one loop from each of the 72 devices in a column is selected and one bit is read, obtaining 64 data bits, and 8 parity bits. Each of the 16 loops is read in sequence. When each loop within the CCDS in that column has been read, reading shifts to another column.

Physically the unit consists of two frames; the control unit and the storage unit. Control unit can contain two storage control units, dc power supply, floppy disc reader for microcode, and microprocessor; the storage frame holds up to four memory arrays, each with its own dc power supply and operator panel, main ac power supply, and blower. This packaging offers performance and availability through duplexing. Concurrent access to any two CCD modules is provided. The controller interfaces to the channel, interprets channel commands, translates to physical logical address, and transfers data to the CPU.

Specifically designed to be used for paging, primarily in large configura-



Device paging performance tests made to compare Storage Technology's CCD based solid-state disc to comparable disc subsystems found 1.5M-byte/s 4304 to be almost three times faster than 3350; and 3M-byte/s 4305 to be that much faster than 2305-2. Tests were made transferring 12 4k pages/request

tions running MVS and MV operating systems, the memory provides the performance necessary to achieve increased throughput. Dual port capability provides availability and reliability. If one controller is lost, the array can be accessed through the other path. With two paths, the subsystem has twice the data transfer capability.

The unit's electronic, modular structure serves to ease field service as well as facilitate upgrades. Diagnostic capability built into the system verifies the operation of error-correction circuits and memory function. A read/write floppy disc is built into the unit to allow engineering changes to be made easily in the field.

Circle 184 on Inquiry Card

System 370 Compatible Processors Benefit From Microcode

Basic design philosophy behind the IBM 370 compatible processors developed by Cambridge Memories, Inc, 360 Second Ave, Waltham, MA 02154 is to minimize hardware circuits and maximize the use of micro code. From this are derived time savings in debugging and redesigning circuits, and greater flexibility particularly an ability to react to IBM software changes.

Spanning the range from System 370/115 through 370/135, the models 1, 2, and 3 are claimed to offer 10 to 15% higher performance than equivalent IBM systems and have peripheral and software capability of the 370/138. Based on the design of the Omega 480-1 manufactured by IPL Systems, Inc for Control Data Corp, the processors are planned to be approximately the same size as comparable IBM units and to support IBM or compatible peripherals available on small and medium scale /370 systems.

Hardware within the processors incorporates ECL and current generation TTL circuits. Multilayer printed circuit techniques reduce mechanical connections and enhance reliability.

The amount of dedicated hardware is further reduced by overlapped instruction processing and use of shared circuits operating at high speeds. The basic machine is a microprogram controlled processor with an architecture highly dependent on writable control storage.

The CPUs are available with byte multiplexer, burst mode selector, and block multiplexer channels. All IBM and IBM compatible peripherals except those requiring direct control or external signal features are supported. Noncompatible devices can be supported if their controllers attach to a standard IBM channel.

DOS/VS, VS-1, VS-2, and VM operating systems require only a minor change to the EREP module responsible for etching and recording system error layout data. In addition, all user written application programs will run on the processors.

Initial deliveries are planned for first quarter 1979; volume shipments should begin in mid-year. Prices are expected to be approximately 20% lower than IBM prices.

Circle 185 on Inquiry Card

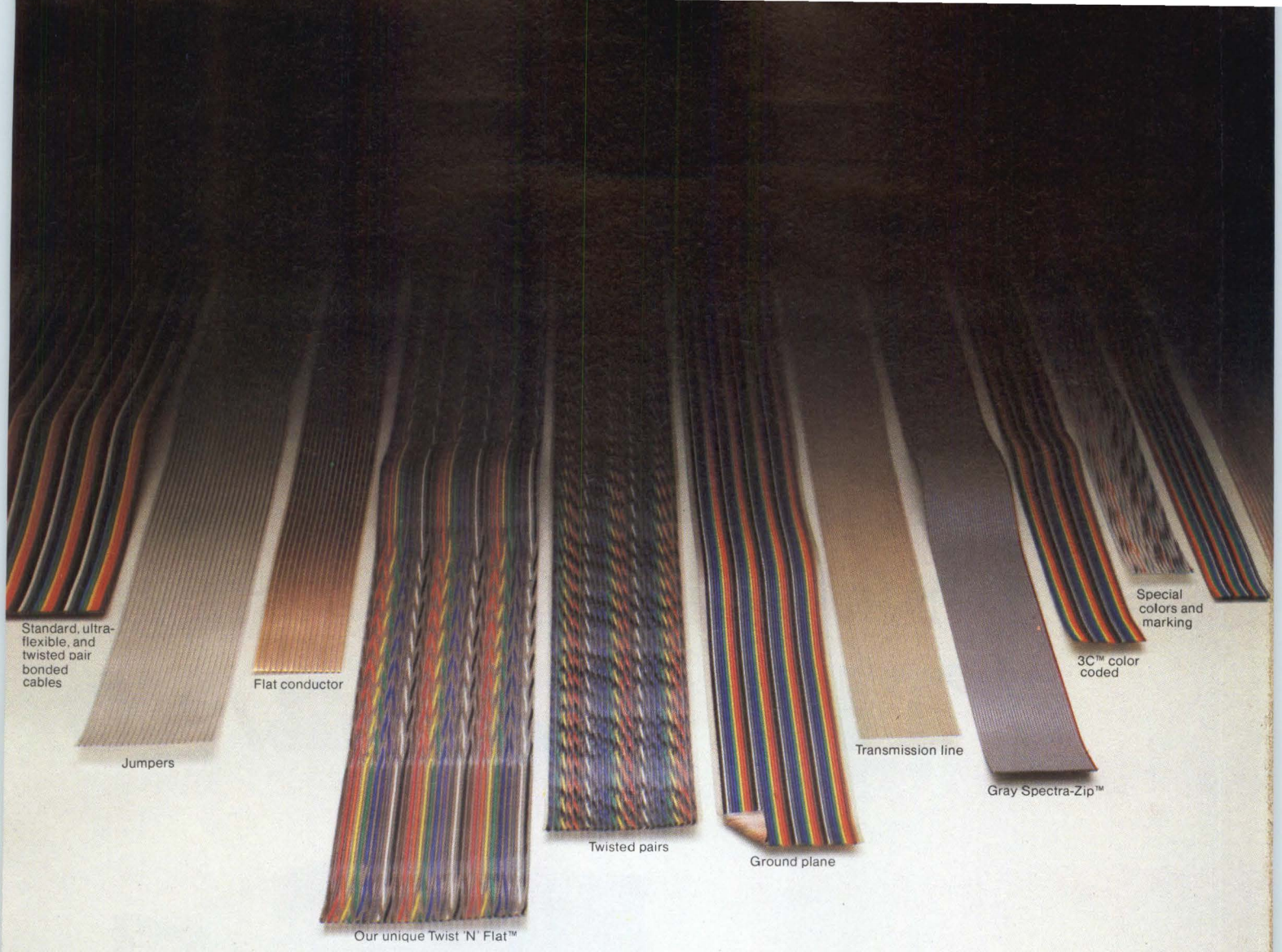
Intelligent I/O System Functions as Remote Sensory Center

IOS2000 uses a preprogrammed onboard microprocessor to handle all forms of analog and digital input and output, acting as a remote sensory center for industrial control and measurement systems. Incorporated in the design of the intelligent I/O system by Burr-Brown Research Corp, International Airport Industrial Pk, Tucson, AZ 85734 are calibration adjustments, signal conditioning and linearization functions, independent ROMs for application programs, and self-checking diagnostic programs.

Remotely located, the unit handles all forms of I/O, collecting and conditioning sensor inputs, sending them to the CPU already digitized and preprocessed. In a closed loop installation, the system responds to CPU commands and generates contact closure outputs to turn on lights and motors, and generates analog output voltages and currents to modulate valves, establish setpoints, and perform similar functions.

Major functions include an A-D converter card that performs automatic zero, automatic ranging, system calibration, and base line offset. I/O cards have onboard P/ROM instructions tailored for linearization and units conversion.

Up to 15 I/O systems can be connected to one serial asynchronous communications line. In a standalone configuration, an H-P 9845 or 9825



When it comes to flat, we've been around.

We make more different kinds of planar cables for more different kinds of interconnect systems than anyone on the planet Earth. And, in this world of planar-come-lately's, Spectra-Strip has been around since the cable world turned flat.

For all your interconnect needs from planar cables to IDC connectors to complete custom assemblies, just check us out. We'll take total responsibility for solving your interconnect problems, and you won't need to call anyone else.

For the name and number of our nearest distributor or rep, write Spectra-Strip, an Eltra Company, 7100 Lampson Avenue, Garden Grove, CA 92642. Or call (714) 892-3361 today.

When you're down to the wire

CIRCLE 21 ON INQUIRY CARD

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New Developments from SYSTEMS...

The SEL 32/30

Until now, you've either had to forego 16-bit pricing to get 32-bit performance, or you've had to give up 32-bit performance just to keep the budget in line.

No longer. Now you can invest in a full-blown 32-bit computer and pay no more than you would for a 16-bit computer. And not have to worry about insufficient power for future needs.

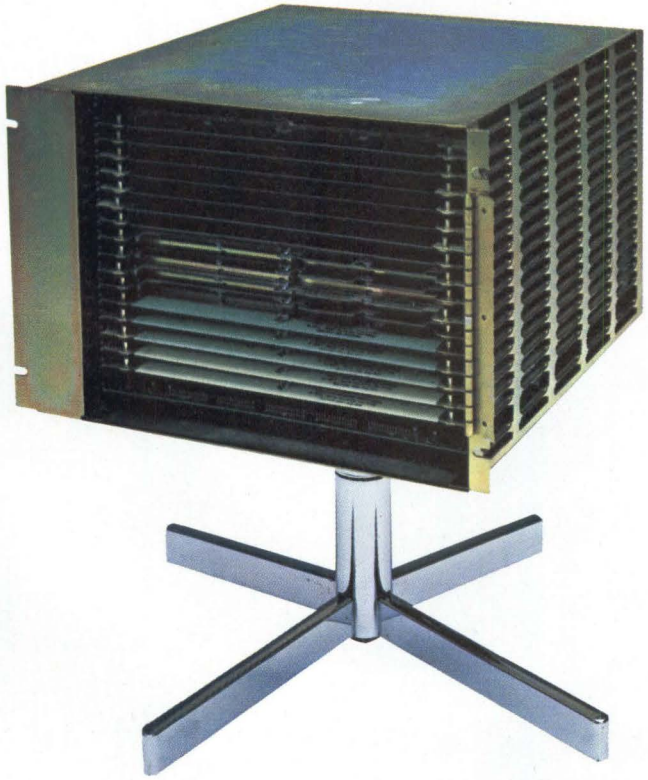
The SEL 32/30 is the smallest of the SYSTEMS hierarchy of 32-bit computers. But don't let its small size fool you. This MAXIBOX is big in performance and throughput, ideally suited for scientific or process control applications such as telemetry, simulation, industrial or laboratory automation. And it costs you no more than a 16-bit computer.

The SEL 32/30 is value-engineered for the OEM. It is a single chassis, fully integrated system that is upward compatible with the entire SEL family of 32-bit computers. So even if you start with a minimal investment, it will continue to pay off as your customers' applications expand.

If power and performance are what you need, and budget is a definite consideration, talk to us. We'll make sure that when you invest in a SEL 32/30 MAXIBOX, more dollars will flow to your bottom line.

Call us. We're easy to talk to.
(305) 587-2900
6901 West Sunrise Boulevard
Ft. Lauderdale, Florida 33313.

MOS MAXIBOX.™



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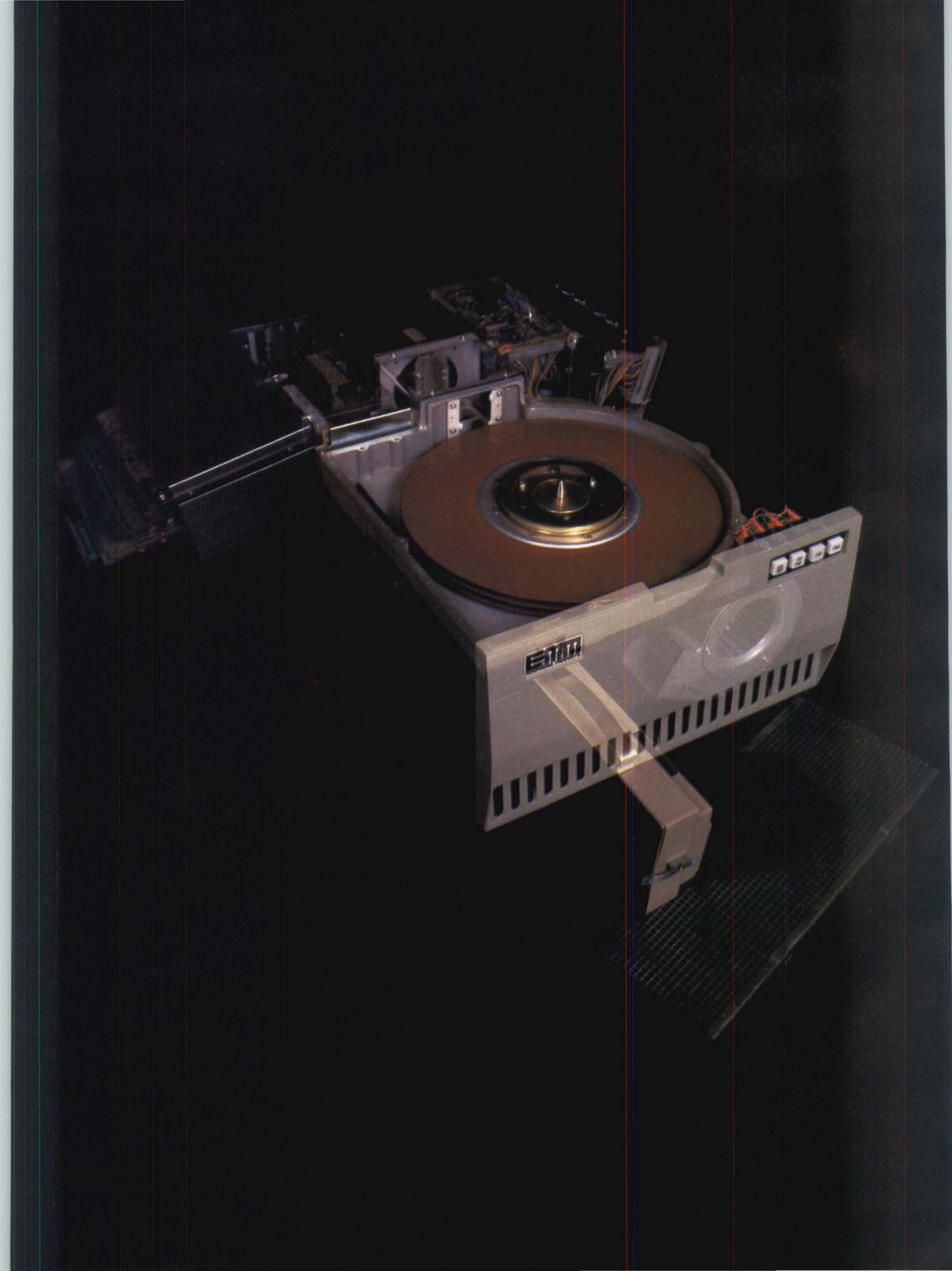

EMI

THE 74 MEGABYTE DISK DRIVE OEMS HAVE BEEN WAITING FOR

Introducing EMM's Model 312 disk drive. The one you've been waiting for. Up to 74 megabytes in a single top loading disk drive. Featuring removable and fixed disks allowing its own backup. Now you have a smart alternative to all-fixed Winchester technology and all-removable storage module type drives. With design features and a price an OEM can appreciate. Like design simplicity for easy maintenance, and improved reliability. Storage flexibility. A down-to-earth price per megabyte. Cartridge drive interface. High performance. Zero warm-up. And, delivery you can count on. Take a look at how our new 312 disk drive can make a difference for you.

Proven Reliability—With thousands of disk drives operating day-in and day-out, we have an outstanding track record for reliability. Our new 312 features such innovations as a dual servo track-following system to eliminate temperature related problems. One dedicated servo surface for the fixed disk and one for the removable cartridge. Superior design features give an MTBF of 4500 hours.

Interface—Our drive is easy to interface with your system. It has a modified cartridge drive interface.

Storage Flexibility—You have the choice of one removable cartridge, and one, two or three fixed disks: 25–74 megabytes that are field upgradable. Daisy chain four drives and you get an incredible 296 megabytes on a single system. So you can keep pace with your customer's expanding storage needs.

Maintenance Simplicity—Our new 312 disk drive is easy to service with snap-on front panel and covers for easy access. A pop-out filter that can be replaced without tools in less than 5 minutes. A flip-out card cage and power supply that is easily removed without tools. No mechanical adjustments and only one head alignment required. Only five adjustments in the electronics. Built in servo track writing capability allows easy replacement or addition of fixed disks in the field.

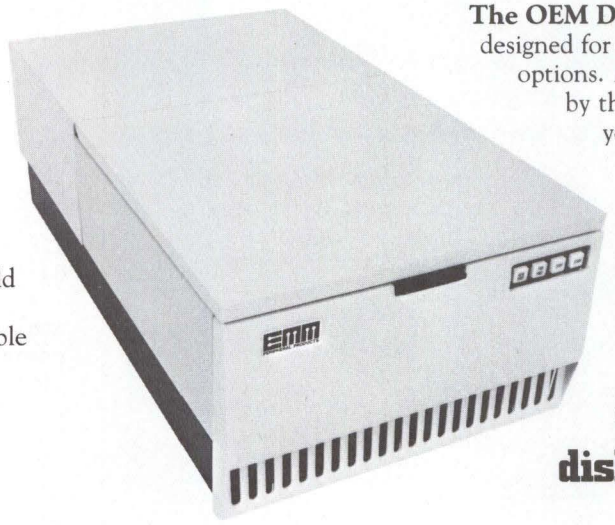
High Performance—Our 312 delivers the best of 3330 technology. Track densities of 370 tpi and recording density of 4545 bpi.

Zero Warm-up—Put a cold cartridge on a hot 312 drive and it's immediately usable. This helps your customer achieve higher system efficiency.

Down-to-Earth Price—You get about 7 times more capacity than a 10 megabyte drive at only 1.5 times the price. It drops your cost per megabyte right down-to-earth.

The OEM Designed Drive—The 312 is designed for OEMs. With select OEM options. And, the 312 is backed by the type of technical support you've come to expect from EMM. It's what you've been waiting for.

To see how our new 312 disk drive can make a difference for you, contact your nearest EMM sales office.



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CIRCLE 23 ON INQUIRY CARD

intelligent terminal serves as controller. All functions are contained on card modules that plug in to a passive card cage. The system is partitioned into five card groups: communications, microcomputer, power supply, A-D converter, and I/O cards. Memory for specific functions is contained on the function card; adding cards adds memory as the system grows.

Full capacity of the largest enclosure is 256 digital points or 128 analog channels in any combination. Up to three card files can be clustered to operate from a single processor, communication, and A-D card set. This card set has capacity for 48 I/O card slots (768 digital points or 384 analog channels) or a combination.

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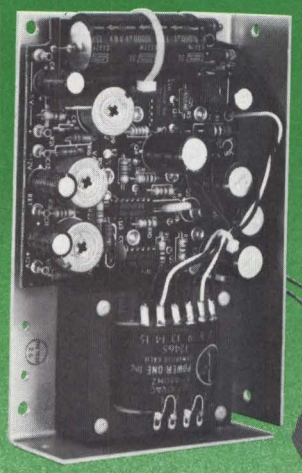

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Memory Analyzer Display Visually Identifies Cell Address and Contents

Immediate visual identification of address and data within a memory device under test are obtained using the memory analyzer display unit introduced by the Xincom Div of Fairchild Camera and Instrument Corp, 20450 Plummer St, Chatsworth, CA 91311. Designed to assist in characterizing semiconductor memories up to 64k, the portable standalone unit interfaces to any Xincom III tester equipped with dynamic error logging unit (DELU), providing a matrix display of test results on a CRT within 200 ns after test completion.

The unit obtains test results by interrogating the dynamic error logging unit and storing the received data. A video image of DELU memory is displayed constantly as a matrix of variable intensity dots on a screen. The screen is arranged in a matrix of 256 x 256 dot locations, each depicting an addressed data bit within memory. A bright dot represents a 1; a dim dot indicates a 0; and the absence of dots denotes a communication error. Dot formats are selected from 1k, 4k, 16k, or 64k memory sizes; ie, a 16k matrix will measure 128 x 128 dots; 4k memories show 64 x 64 dots.

A movable cursor within the matrix marks the desired memory cell. The cursor is controlled by a front panel joystick, a proportional speed vector control with a 15% center dead zone. For close observation of bit cells, sector zoom is provided. This allows a minimum 1k sector with a 32 x 32 dot matrix to be magnified to full screen matrix size.

Operational tests and maintenance diagnostics are provided by a self-test subsystem built into the unit. Tests include all 1s, all 0s, all errors, alternating 1s and 0s, and a cross-hatch pattern for display symmetry check and adjustment. Patterns may be displayed even when a test is in progress.

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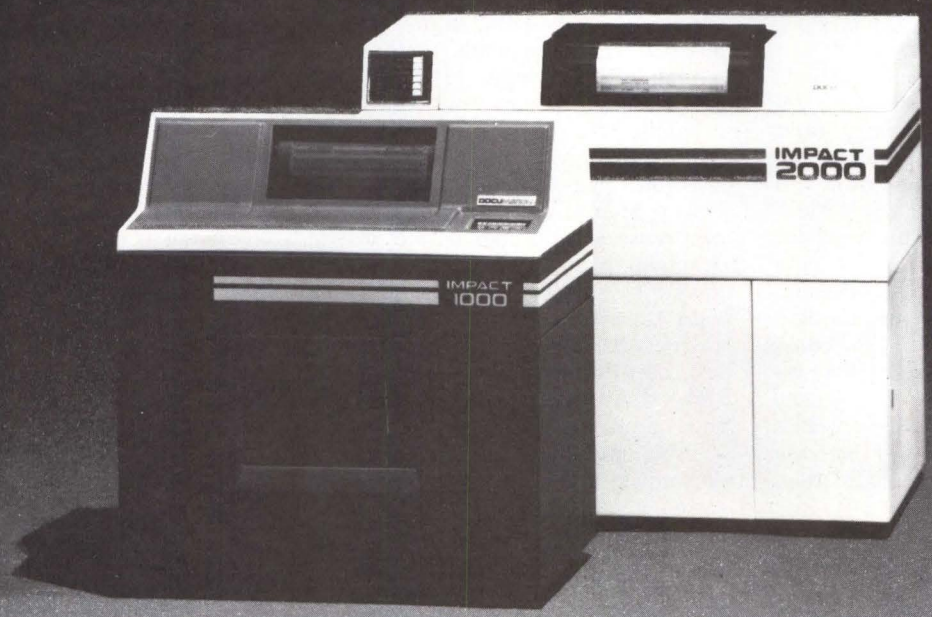

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CIRCLE 25 ON INQUIRY CARD

SOFTWARE

Data Entry Software Offers Performance Oriented Features

Source data entry software permits minimally trained personnel to develop and execute data entry tasks on distributed processing systems. Designed to provide data conversion and editing capabilities on PTS/1200™ MARK-I and MARK-II systems, used for 3270 type interactive tasks, remote batch processing, local processing, and report printing functions in a data communications network, the package introduced by Raytheon Data Systems Co, 1415 Boston-Providence Tpk, Norwood, MA 02062 provides seven major capabilities to increase performance in data entry, validation, and editing functions.

To make use of the package, operators establish dialog through keyboards with the software routine located in system controller. The dialog permits formats to be established, modified, or recalled for use in tasks. A menu of 20 aids accessible during conversion and entry assure a high level of accuracy while maintaining a high rate of entry.

Automatic cursor positioning, for example, allows the system to move the cursor only to those fields within a record that require data. A table lookup feature calls data from tables of prestored information and inserts it automatically into specific fields, reducing keystrokes and assuring higher data transcription accuracy. Reasonableness tests, including range checking, user-definable field comparisons, and validity testing, are used to further ensure accuracy.

Productivity enhancement features encompass alpha only, numeric only, mixed entry, must enter, must complete, right/left justify, character file, check digit generate, check digit check, and branch instructions. System arithmetics include add, subtract, multiply, and divide, and ability to perform line by line and record by record computation and cross footing.

Specialized subroutines can be programmed in MACROL. Data entry capability runs concurrently with interactive and batch jobs on large systems or with a single batch application on smaller systems. On large systems it operates concurrently with combinations of inquiry/response, interactive or batch transmissions, remote batch processing, and local printing.

Circle 188 on Inquiry Card

Enhanced BASIC Reduces Training Time, Eases Problem Solution

BASICPLUS contains enhancements to ease both the learning process and problem solution. The language, available from Datapoint Corp, Data Processing Div, 9725 Datapoint Dr, San Antonio, TX 78284, provides for larger size names, more efficient use of memory, and full interchangeability between its record files and those created with other languages.

The language handles complex programming details automatically, allowing novices to print answers without specifying the exact form, or do arithmetic on all entries in several columns with simple instructions. Advanced features provide string manipulation instructions and complex mathematical routines.

Enhancements include acceptance of 78-char variable names, and multiple statements per line. Chaining and keyboard-controlled execution of programs, automatic configuration of printers, and disc input and output in standard file format are all supported.

Upward compatible with the company's previous versions of BASIC, the language includes many features of the proposed ANSI standard BASIC, including numeric functions, relational operators, logical constants, and matrix operations with determinants and transformations. To execute it requires 48k bytes of memory. □

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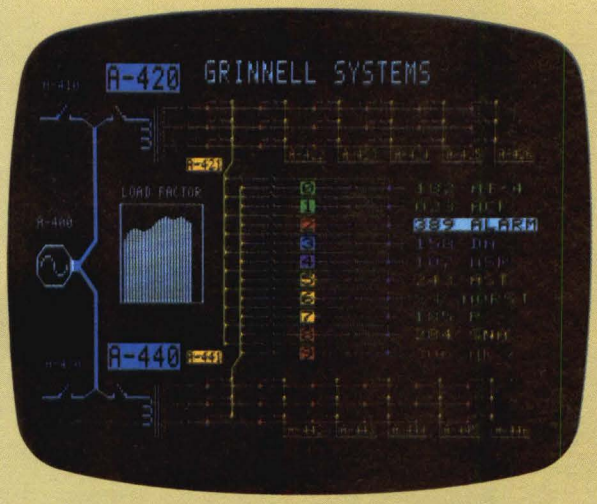

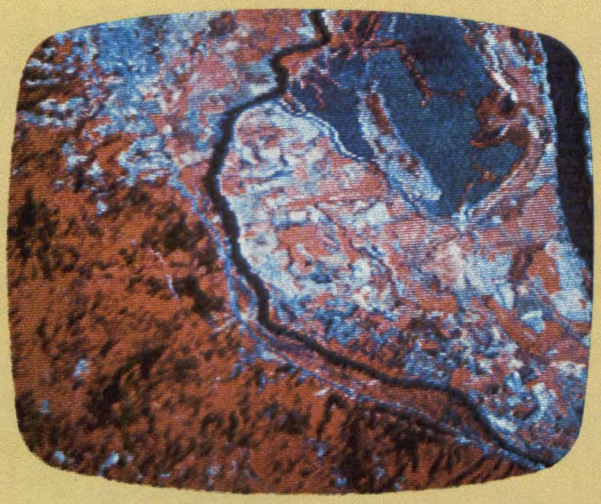

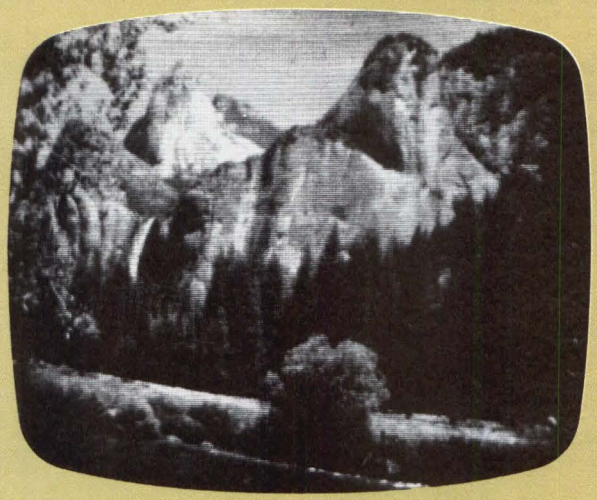

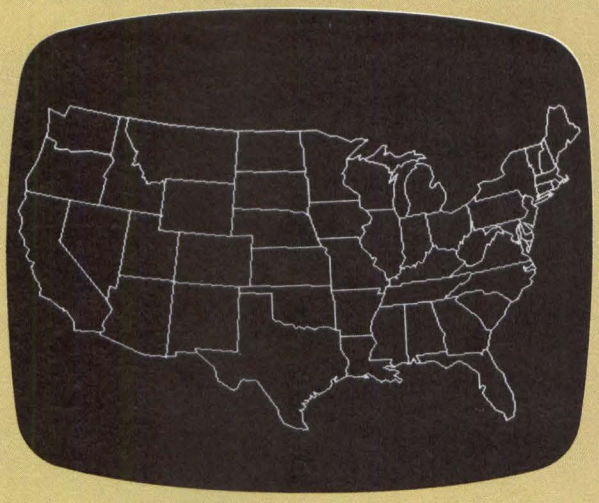

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In Portland, Oregon, Sperry Univac minis help the Police Bureau come to the rescue hundreds of times a day.

Because Boeing Computer Services has computerized all of Portland's emergency services with Sperry Univac Series 77 minis.

Now when a citizen reports a crime, our minis verify the address. Examine the surrounding area for similar calls, hazards, and temporary situations (such as streets under repair). And suggest which units should respond to the call.

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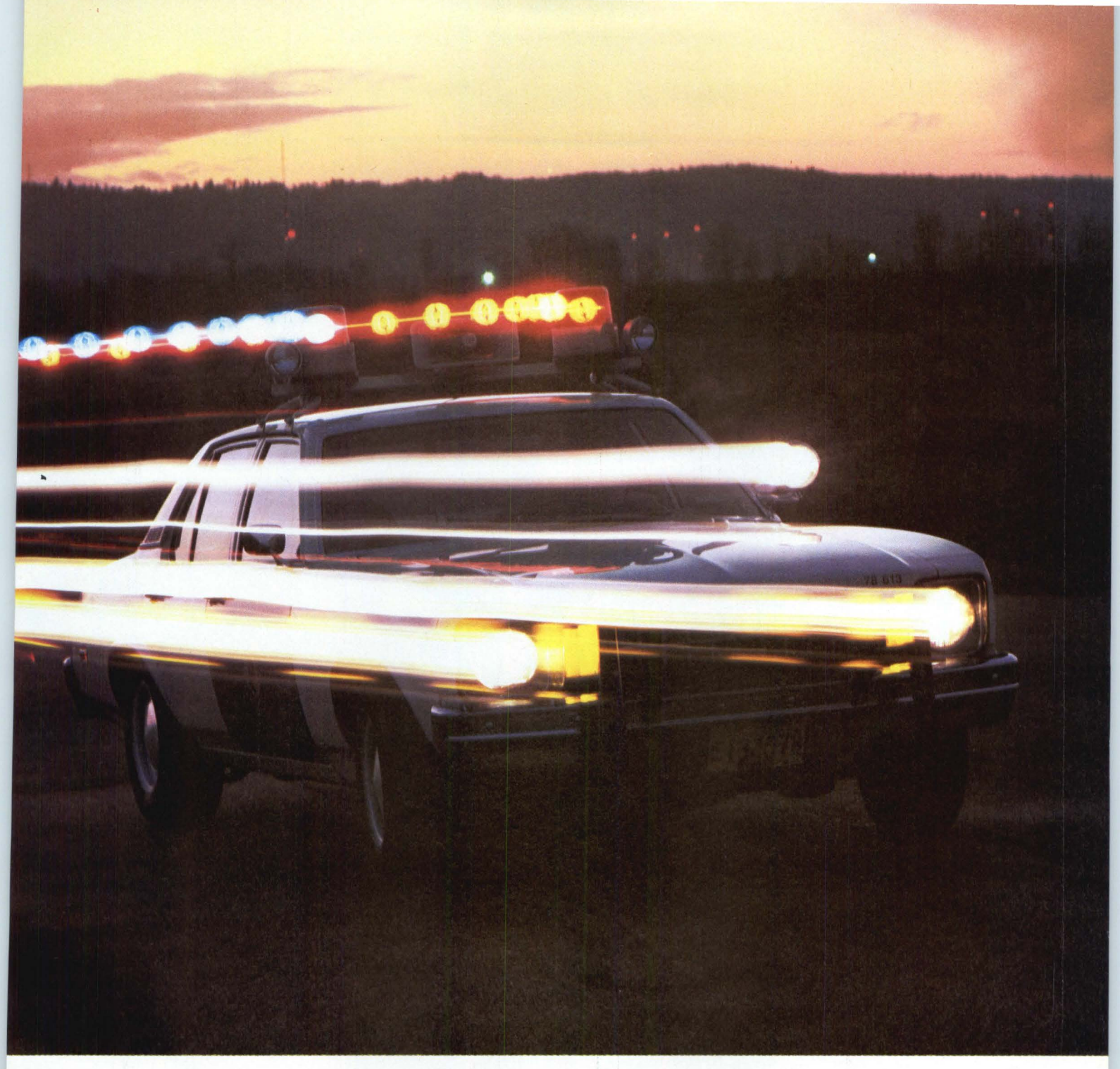

alarming things in Portland.

ing, scientific, instrument control, or data communications.

For more information, write to us at Sperry Univac Mini-Computer Operations, 2722 Michelson Drive, Irvine, California 92713. Or call (714) 833-2400, Ext. 536.

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CIRCLE 27 ON INQUIRY CARD

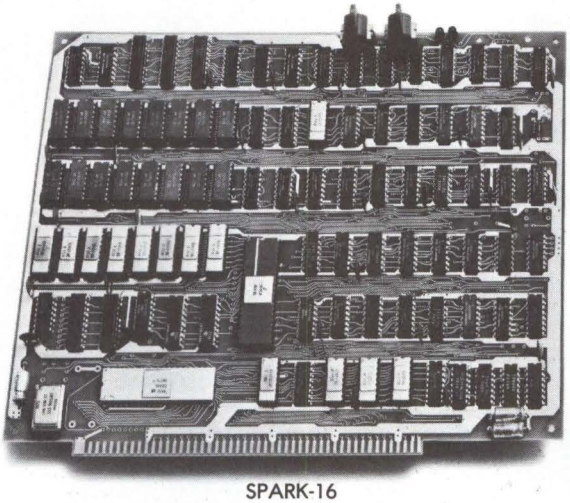
MICRO

Introducing SPARK-16: The MICROFLAME family has given birth to a microcomputer.

Fairchild recently introduced 9440 MICROFLAME™ CPU — the world's first 16-bit bipolar microprocessor that executes an instruction set with minicomputer performance.

Now we're introducing the SPARK-16™ microcomputer designed to demonstrate the capabilities of the 9440 MICROFLAME CPU or to be used as a stand-alone microcomputer for applications requiring 4 K words of RAM (expandable to 8 K words soon, and more later) and 2 K words of ROM.

Major applications for the 9440 MICROFLAME CPU and SPARK-16 board include OEM data processing in a variety of computing control and instrumentation environments; telecommunications PBX switching installations; distributed intelligence, distributed multiprocessing and front-end (terminal) processing.



SPARK-16

Where there's flame there's fire.

Fairchild is also introducing its FIRE™ (Fairchild Integrated Realtime Executive) software package. Available now for use with the 9440 MICROFLAME CPU or the SPARK-16 microcomputer are FIRE-LOAD (bootstrap and binary loader), FIREBUG (interactive entry and debugging program), FIRE-EDIT, FIRE-DIAGNOSTICS, FIRE-SYMBUG, BABY BASIC, FIRE-BASIC, FIRE-MACRO (a stand-alone macro-assembler) and FIRE-RLOAD (stand-alone linking loader). These are fully supported and documented.

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A spark of genius.

The SPARK-16 pc board is loaded with features including the 16-bit 9440 MICROFLAME CPU, 4 K words of RAM, (expandable soon), 2 K words of Autoload PROM, memory control with DMA capability, interface logic for a Teletype or RS232C, 100-pin connector with 9440 Bus, connector for TTY/RS232C, control switches (Autoload, Continue, Halt and Reset) and display. BABY BASIC and FIREBUG are available in PROMs. The SPARK-16 board requires only a single 5 V, 4.0A power supply and a TTY or CRT terminal. The single board price is $995.00.

Only the beginning.

More sophisticated FIRE software, board level hardware and LSI support circuits are on the way. Before year-end the software will include an interactive disk operating system (for hard and floppy disks) and shortly thereafter a FORTRAN 77 and PASCAL. New LSI circuits will include a 16K TTL dynamic RAM; a memory control with control, refresh and DMA capabilities; and an I/O bus controller.

For 9440 parts and SPARK-16 boards, contact your Fairchild representative or sales office. For a MICROFLAME brochure and data sheets, call or write Fairchild Camera and Instrument Corporation, MICROFLAME, P.O. Box 880A, Mountain View, California 94042. Tel: (415) 962-4626. TWX: 910-379-6435.

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DIGITAL CONTROL AND AUTOMATION SYSTEMS

Digital Control at WESCON

Nearly every technical conference today includes sessions or papers on digital electronics—and, in turn, nearly every electronics conference includes sessions on data acquisition and/or control. The 1978 Western Electronic Show and Convention (WESCON) was no exception.

The first session on the professional program was "Industrial Control Systems Using Mini/Microcomputers." Paper subjects included developing computer control algorithms, acquiring data on high temperature operation, designing a computer numerical control system, and developing a realtime language interpreter. Although the range of subject matter is wide, each is more or less typical of the presentations given at conferences of this type.

Development of Feedback Control Algorithm

Key objective in controlling the effects of external disturbances in a computer control system is to restore all disturbed outputs to balanced states in the minimum number of sampling times—to control disturbances in a "deadbeat" manner. Even though the disturbance may still exist in the feedback loop there will be no change or ripple in the output. That balance must be retained in spite of changes in either setpoints or loads.

The computer must be assumed to be an integral part of the feedback control system. System responses are sampled by the computer at predetermined intervals and findings are compared to stored prescribed values. Any deviation from set behavior patterns results in corrective action initiated by the computer's control algorithm.

Such algorithms generally are designed from both process and desired performance specifications. They deal with control of setpoint changes as well as disturbances that enter control loops.

A paper presented concerns development and implementation of control algorithms that result in deadbeat response to either reference or noise inputs.[1] One objective was to design algorithms for control loops (Fig 1) that would offset both setpoint and load changes. Such algorithms would "drive a system from an arbitrary initial state to a desired final state in the minimum number of sampling times and in such a way that after the output matches the input for the first time, the two signals are equal everywhere, not just at the sampling instants." In addition, "the restored system output will not change, or ripple, . . . , even though the disturbance may still be present in the loop."

In a typical system, N + 1 sampling times would be needed to offset a load disturbance (to "deadbeat" its effect and restore the signal). For example, in a first-order system, "the controller becomes aware of the noise one sampling time after the noise enters the control loop. It takes the controller an additional sampling time to prescribe the appropriate action in the manipulation to offset the disturbance. For a second-order system, the noise is also detected in the second sampling interval, and it takes two sampling times to offset it, that is, a total of three sampling times since the noise entered the loop."

Although, for a setpoint change, the point in time that a disturbance enters the loop can be controlled,

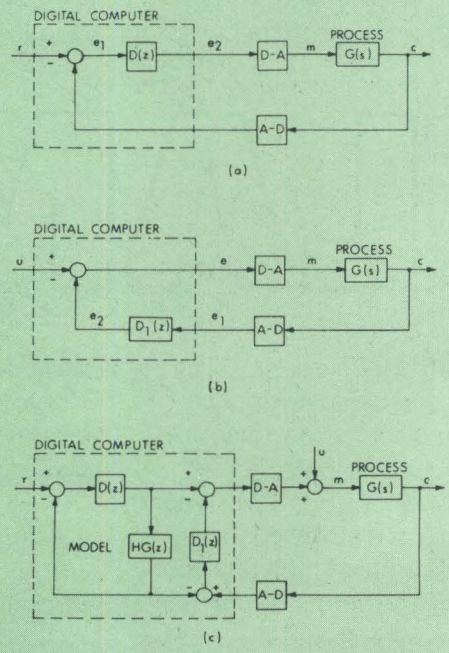

Fig 1 Control loops for deadbeat response.[1] Loop for setpoint changes (a) and that for load changes (b) are superimposed to provide loop for both types of changes (a) that works with or without external disturbances. D(z) and $D_1(z)$ are transfer functions for setpoint and load controllers, respectively. HG(z) represents pulse transfer function or mathematical model of controlled system

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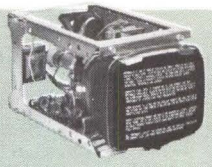

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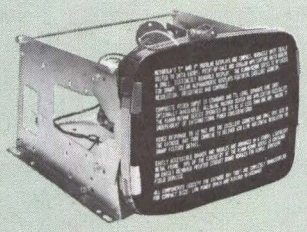
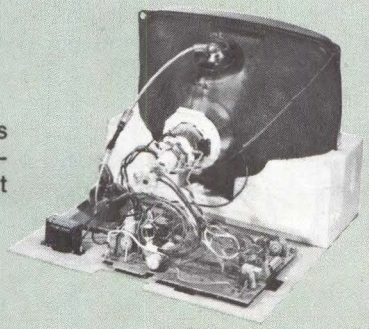
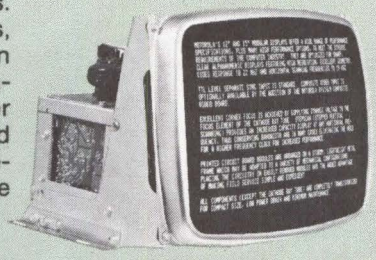
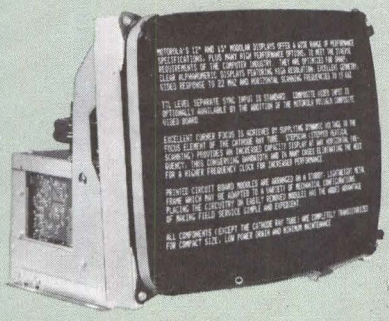




M3500 series 12-inch display modules in chassis or kit form (shown). Cost saving, plus no metal boundaries to inhibit your own layout.



MD3000 series 12-inch display modules. Between the MD3000 and M3500 series, you can have your 12-inch display in any of several ways: chassis or kit, separate sync TTL level, composite video or direct drive inputs, choice of standard EIA phosphors, choice of scan frequencies, with or without anti-reflective faceplate.



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The M4408 15-inch module displays a full page horizontally (132 x 46) or vertically (96 x 66, shown). High character density and low cost, too—raster scan technique with standard TTL logic interface gives you economy twice: once in purchase price and again in design costs. A technology leader.

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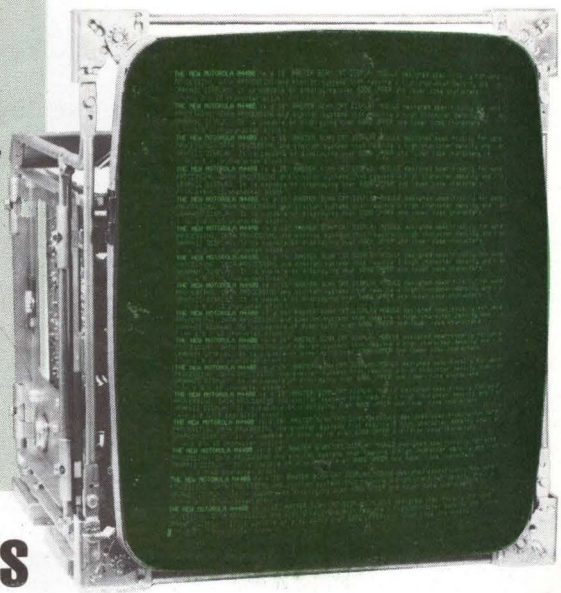

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that is not true for load changes since they are influenced by outside factors. However, resultant effects on overall performance of the loop are not considered important.

This approach is general and can be expanded to cover multiple input/output systems. In the example discussed here, a system was simulated on an analog computer and controlled by a digital minicomputer with 11-bit plus sign D-A and 10-bit plus sign A-D converters.

Acquisition of Temperature Data on Turbine Blades

Although turbine engine performance improves as inlet temperatures rise, the higher temperatures often require better blade cooling techniques. Since temperatures to be measured are high and access to the moving blades is difficult, a method was devised to make the measurements by use of infrared pyrometers and fiber optics.[2] This method involves a complete IR pyrometer system that can gather hundreds of very accurate temperature measurements from high speed rotating blades.

Access to the blades is achieved via a 1.5′ (0.46-m) borescope and a coherent bundle of optical fibers. As the turbine blades rotate, individual fibers carry radiant energy along a radius of the blades.

IR emissions from the turbine blades are focused selectively by a microscope assembly, fiber by fiber, onto detectors. Each detector and associated amplifier produced a voltage proportional to the energy emitted by the selected position on the blade.

Voltages are digitized at rates of up to 2 MHz and then stored. Once 200 successive data points have been developed, a recorder transmits a block of data to a computer system.

Fig 2 is a block diagram of the hardwired logic package used to relieve the computer of the more time-critical functions. This package accepts basic commands from the control computer and executes the desired functions. The logic package also provides digitized data to the computer through an 8-bit data bus,

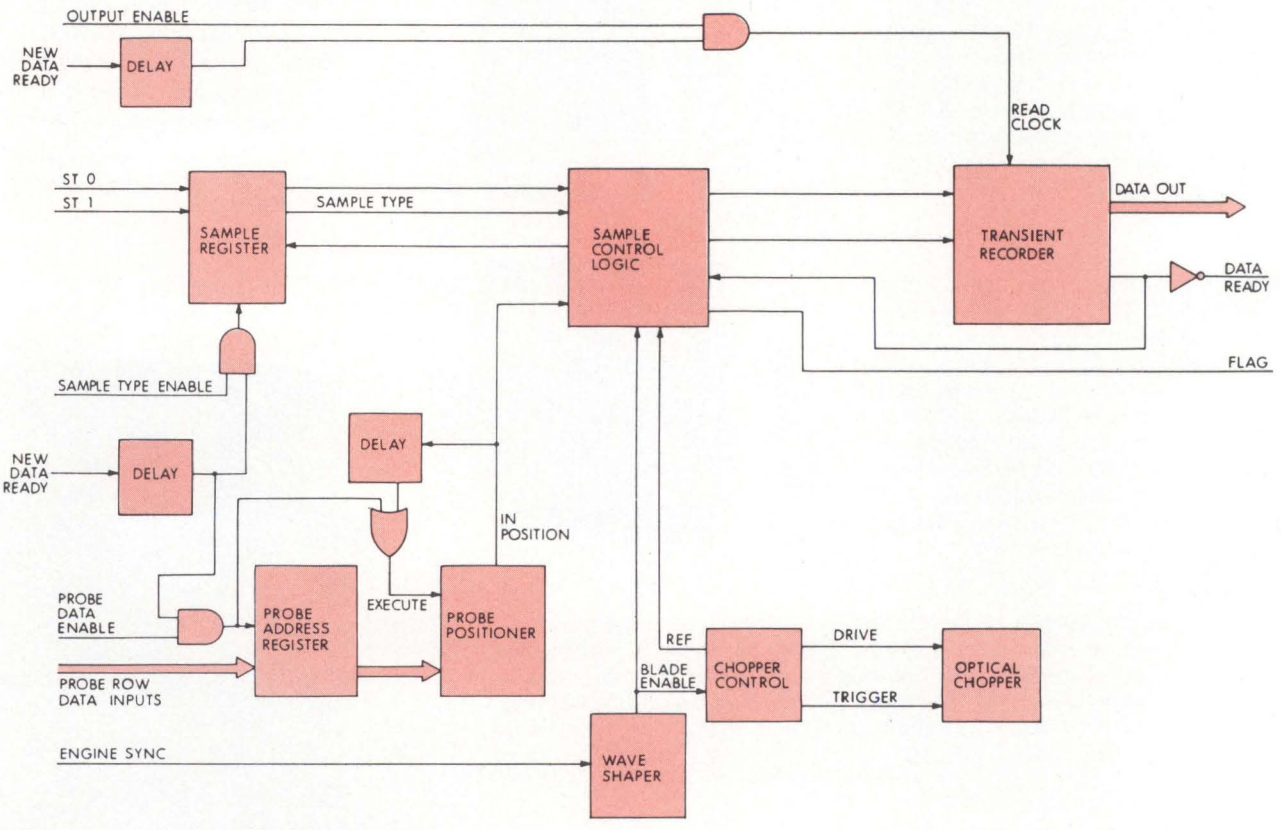

Fig 2 Hardwired logic unit for measurement of turbine blade temperature.[2] Many logic operations necessary for high speed acquisition operations are too demanding for conventional microprocessor control. Communications link was implemented by minicomputer

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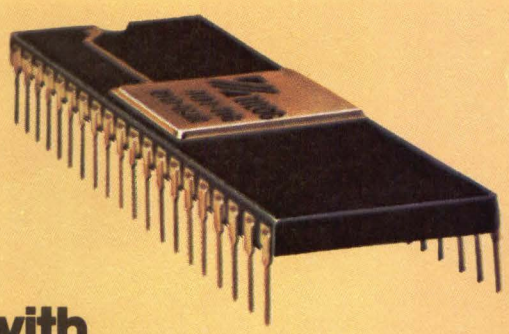

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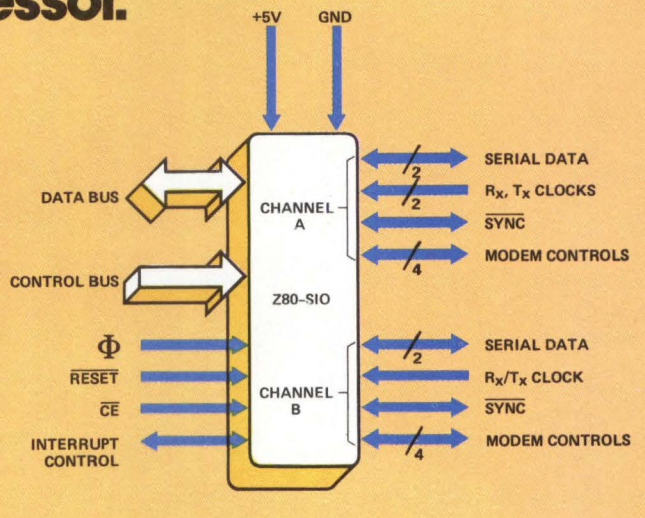

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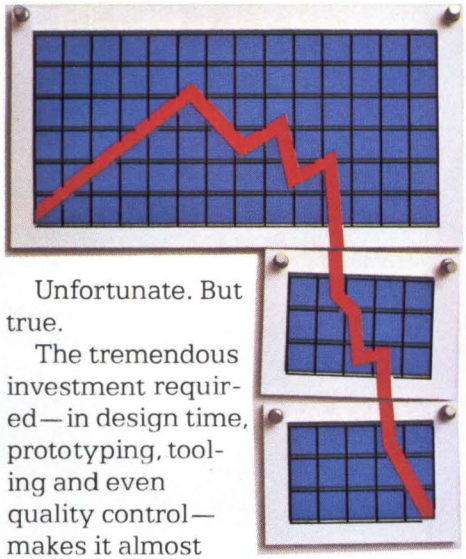

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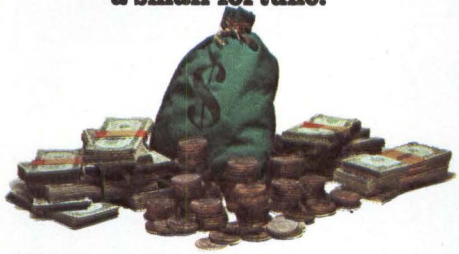

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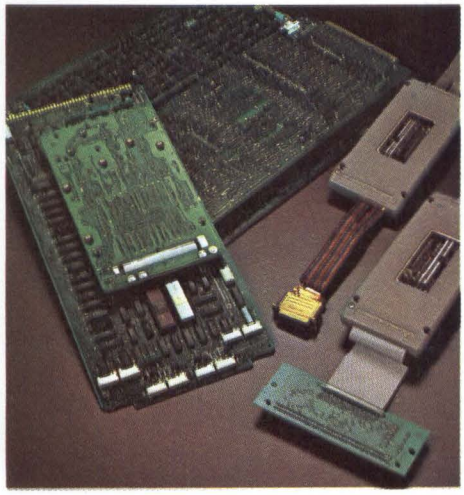

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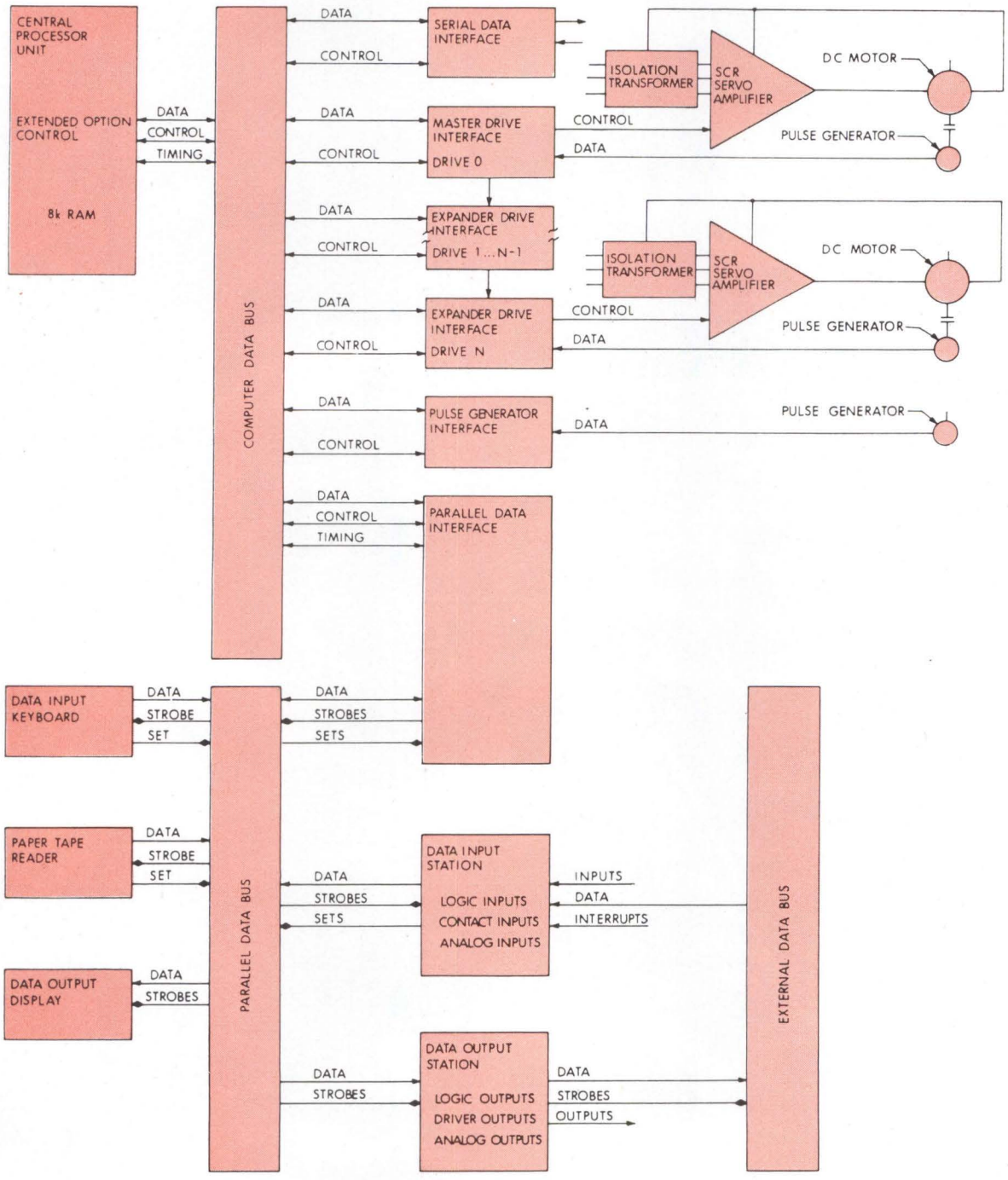

Fig 3 Block diagram of CNC hardware.[3] Microprocessor-based system offers advantages of programmable controller with power and flexibility of general purpose minicomputer yet eliminates most of disadvantages

(*Continued on p 62*)

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and supplies operation-complete information through two flag bits.

Positioning of the optical fibers is initiated by loading a 13-bit fiber address on the probe row data inputs, setting the probe data enable input, and pulsing the new data read line. This loads the fiber address into the probe address register and initiates the operation of the probe positioner. Positioning will continue until the in-position signal goes true.

Sample type selection (light or dark) begins with the loading of a 2-bit sample code onto ST0 and ST1. The sample type enable line is held true, and a new data ready is pulsed. This sequence loads the sample register that is used by the sample control logic in the subsequent sampling operation.

The next trigger signal from the phototransistor assembly initiates operation of the transient recorder, the recorder buffer is filled from the digitized detector output, and a completion flag is set. A flag to the computer indicates that the buffer has been filled.

Microcomputer hardware for this system consisted of an IMSAI I-8080, made up of an Intel 8080 microprocessor, 8k of P/ROM, 8k of RAM, two asynchronous RS-232 ports, and 32 bits of TTL-level digital I/O. The console was a Teletype ASR-33 terminal.

The 8k P/ROM stored IMSAI BASIC 1.4 and the 8k RAM stored program and data. One port was dedicated to the console device, while the other transmited serial data to a remote Interdata 7/32 computer. The parallel ports were dedicated as necessary to interface with the hardwired logic unit.

A general purpose version of BASIC was configured into the system. To support assembler routines, an additional 4k of RAM was added, along with another 1k bytes of P/ROM. Since the input data are supplied as 8-bit integers, it was possible to perform all averaging in fixed point. This greatly increased the speed of the system.

Design of a CNC System

Because programmable controllers lack range and power for complex tasks and general purpose minicomputers are generally relatively difficult to interface and program, a microprocessor-based system was developed to provide computer numeric control for a dc servo.[3] System IV CNC is based on an IM6100 single-chip, 12-bit microprocessor that recognizes the PDP-8 instruction set. CMOS circuits operate successfully in noisy, high temperature environments and dissipate little power.

A typical CNC unit (Fig 3) consists of central processing unit (CPU), extended option control (EOC), random-access memory (RAM), parallel data interface (PDI), data input keyboard (DIK), data output display (DOD), paper tape reader (PTR), cable extender module (CEM), and computer power supply (CPS). CPU, EOC, and RAM are on a single module that plugs into the computer data bus (CDB). PDI and CEM also plug into the CDB. Up to nine additional modules, including RAM, serial data interface (SDI), master drive interface (MDI), expander drive interface (EDI), and pulse generator interface (PGI) units can be plugged into the CDB. Keyboard, display, and reader communicate with the CPU through a parallel data bus (PDB) controlled by the PDI module. Up to 21 additional input and output modules can be plugged into the parallel bus in reserved areas called data input station (DIS) and data output station (DOS). The external data bus (EDB) is used to expand the parallel data I/O capacity as well as provide for remote operation of parallel data devices.

The microprocessor has six 12-bit registers, an arithmetic and logic unit (ALU), and associated gating, timing, and control circuits on a 40-pin dual-inline package that plugs into a large module with 4k or 8k words of RAM. Main software elements include RTS-11 realtime operating system, application program, and diagnostic programs. The RTS-11 package consists of standard software modules used in various systems to simplify the programming effort. The application program is unique for each system and is used to tailor the standard software and hardware products to a specified set of requirements, while a diagnostic program includes online as well as offline procedures used to locate hardware malfunctions.

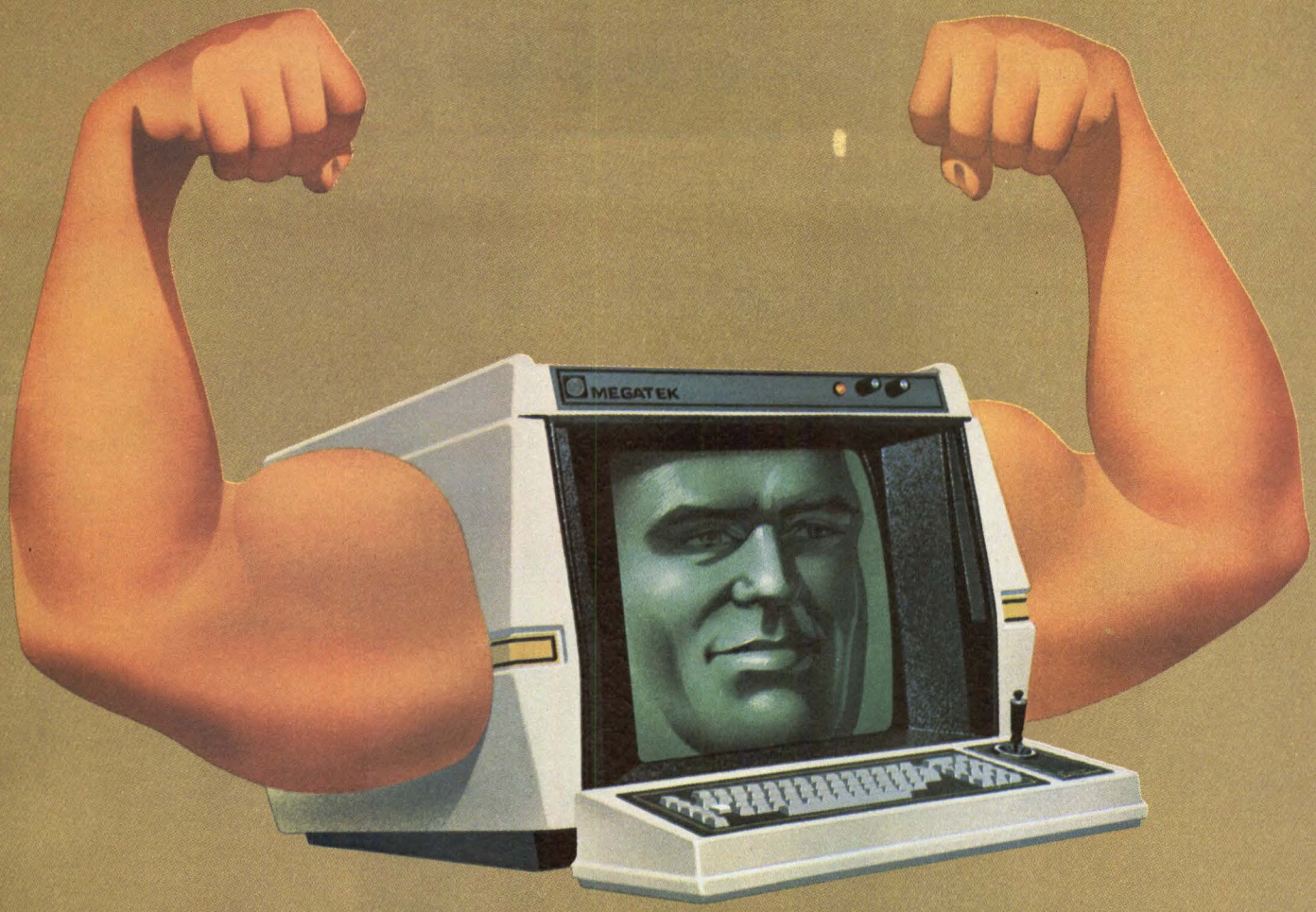
Development of a Realtime Language Interpreter

A version of BASIC designed specifically for data acquisition and control application has been developed for the MicroPac 80/A and the I-8080 microcomputers.[4] Such high level languages as FORTRAN, although in general applicable to process control, have peripheral requirements that are too costly for microcomputer systems. However, BASIC offers a high level language that is economical for use with microcomputers.

To speed up development of a realtime BASIC interpreter, an attempt was made to use an existing BASIC interpreter as the basis of the realtime version to be developed. A variety of BASIC interpreters are available for use on 8080-based microcomputer systems. The MicroPac utilizes a ROM monitor occupying the low 2k of memory. This configuration ruled out the use of several interpreters which utilize restarts as abbreviated calls to frequently used routines. Other interpreters were protected by copyright. The version of the interpreter selected as a nucleus for this project was the Lawrence Livermore Laboratories BASIC, which was developed by the University of Idaho.

The resultant realtime interpreter has been adapted to several 8080-based microcomputer systems. Because it is independent of low memory, it avoids potential conflicts with operating systems (such as CP/M) that may be required. In addition, the format and implementation of the process I/O instructions lend themselves to easy modification for use with byte oriented I/O structures. For example, both the DOT and DIN verbs operate on two 8-bit bytes in the MicroPac version of the interpreter.

(*Continued on p 66*)



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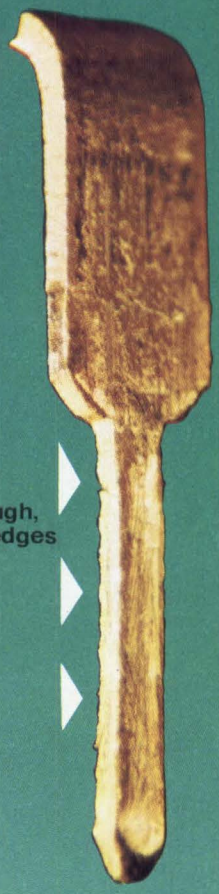

Note rough, jagged edges always present.

Arrows indicate scars and abrasions made by rough edge of lead frame.

22X magnification, unretouched.

Arrows indicate contact surface still smooth, clean, free from abrasions.

22X magnification, unretouched.

Your IC lead frames look like this at 30X enlargement (unretouched). Because they are punched out of metal, the edges are rough, jagged and irregular. In contrast, the flat sides of the lead frame are smooth, even and perfectly plated.

THEIRS

An ordinary edge-bearing socket contact after 5 insertions of DIP lead frame. Contact has been spread apart to show inside faces of contact. Notice how the contact has scars and abrasions from *rough, irregular edge of IC lead frame.* Electrical contact is degraded and resistance is increased. Reliability is obviously reduced.

Lead frame in place in an ordinary edge-bearing contact.

OURS

ROBINSON-NUGENT "side-wipe" socket contact after 5 insertions of DIP lead frame. Contact has been spread apart to show inside faces of contact. See how the RN contact—because it mates with the *smooth, flat side of the IC lead frame*—retains its surface integrity. This 100% greater lead frame contact results in continued high reliability.

Lead frame in place in RN "side-wipe" contact.

expose 'junk' socket problems

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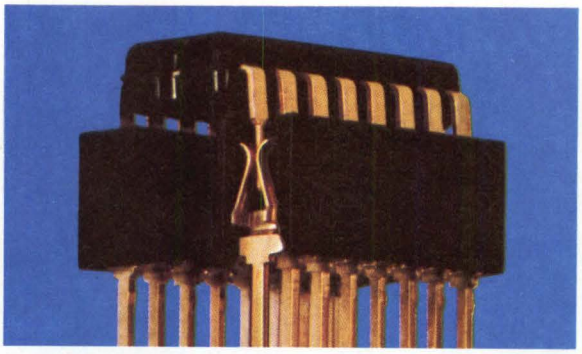

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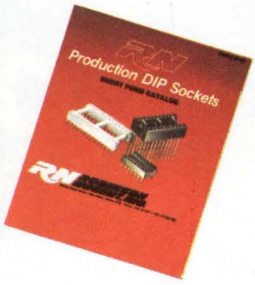

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Realtime BASIC for use on the I-8080 microcomputer series runs under the IMDOS operating system. Notable changes include the origin for the various program modules, the device dependent I/O section, and the structure (syntax) of the process I/O commands.

References

1. G. A. Perdikaris, "Computer Control for Deadbeat Response," WESCON/78 paper 1/1
2. R. Trauth *et al*, "Turbine Blade Temperature Acquisition Using an Infrared Pyrometer and Microcomputer," WESCON/78 paper 1/2
3. G. A. Perdikaris *et al*, "A Microprocessor-based System for dc Servo Control," WESCON/78 paper 1/3
4. D. A. Border *et al*, "An Adaptation of BASIC for Realtime Microprocessor Applications," WESCON/78 paper 1/4

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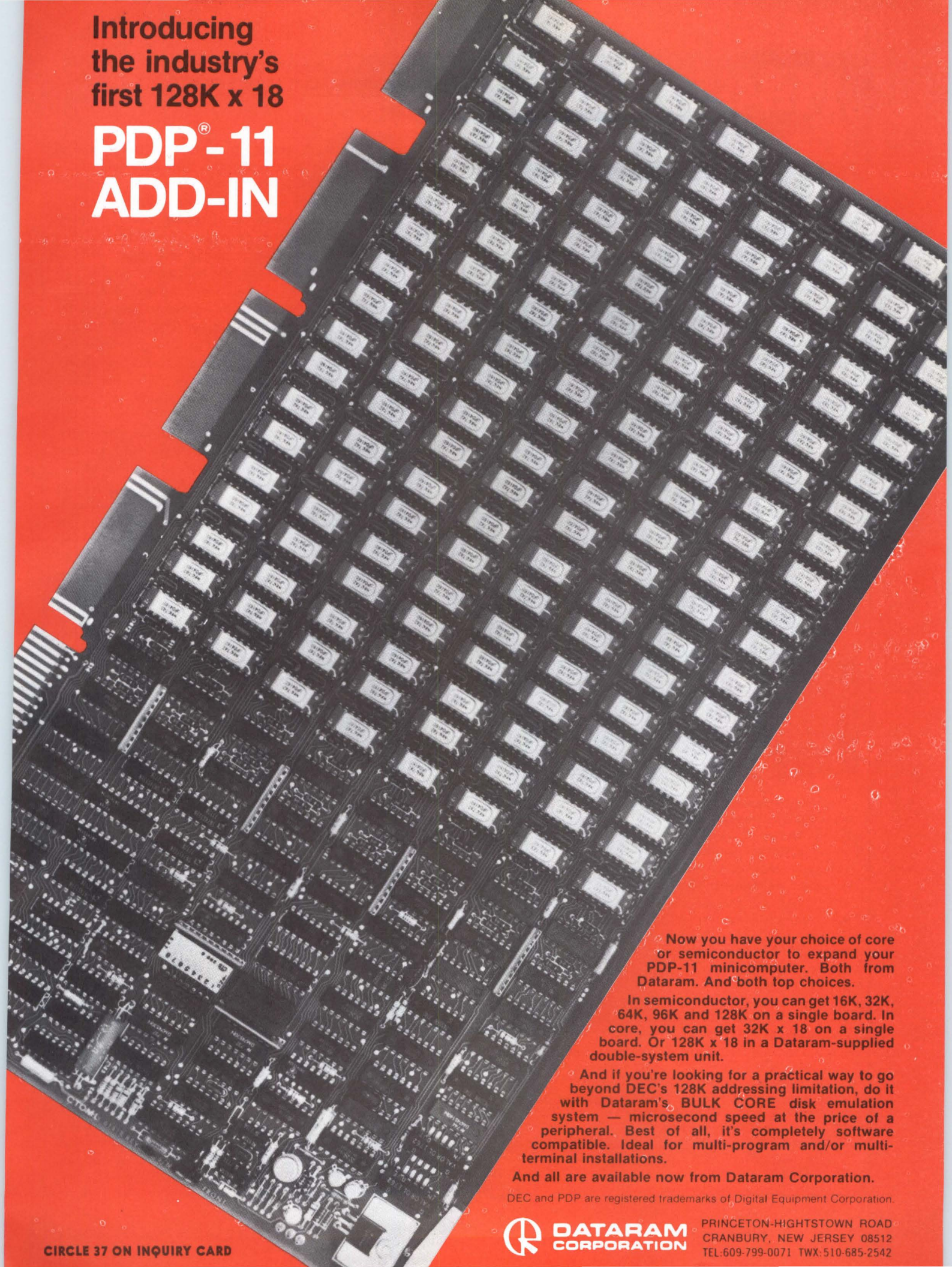

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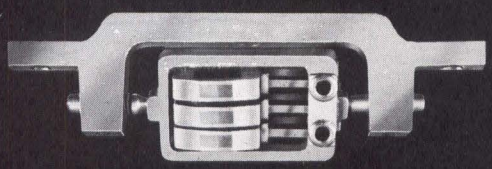

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or new scenarios. A ground plane map display of the defense and offense as it is input is also provided.

Once the user has selected both offense and defense scenarios, he inititates simulated tactical engagement on the display unit to determine optimum flight profiles that will provide maximum protection to the attack aircraft, effectiveness of radar jamming and flight profiles of jamming aircraft, primary and secondary targets for the missile aircraft as a function of time along the attack and escape routes, results of radar jamming to support the attack aircraft during penetration of air defenses, and results of chaff use. All profiles are displayed on the terminal in terms of the probability of abort, which is the likelihood that an aircraft will suffer damage from enemy action to the extent that it cannot complete its assigned mission.

If a user attempts a tactic that would be physically impossible, the program detects the error and notifies the user. For example, if the user tries to overextend his offensive capabilities by employing one missile aircraft against two different defending radars, and the aircraft could not launch a missile against both sites within the timeframe specified (based on the aircraft's maximum airspeed), the program displays a warning such as "excessive airspeed required." The user must then change his offensive scenario.

Set up, follow through, and results of the procedure are displayed on a model 6200A Colorgraphics terminal manufactured by Ramtek Corp, 585 N Mary, Sunnyvale, CA 94086. Data are presented in color, and curves of graphic displays are automatically shaded for improved readability. Use of this portable terminal and a digitizer allows an air strike commander full interaction with the program for both simulation and analysis. Although not designed to meet military specifications, the terminal has been operated in rugged environments without any problems.

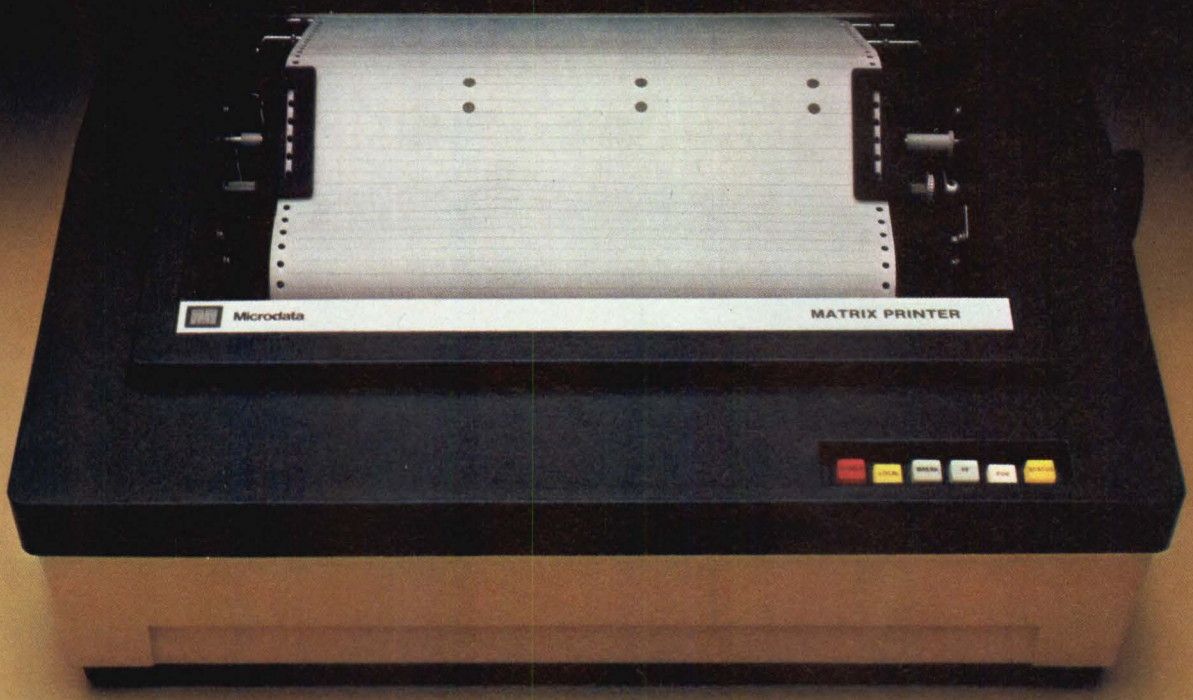
The system can be used also to train pilots by giving them a chance to develop their own tactics and test the effectiveness of those tactics on the computer. As new ECM equipment are developed and improved, each can be tested on the program. Research and development teams also use it to postulate the performance capabilities of air defense systems.

The high resolution terminal provides a flicker-free picture with sharp character and edge definition because the display is refreshed at twice the rate of a home TV set. Graphics resolution is 512 elements by 256 lines. An independent, high speed alphanumeric refresh display offers a visible matrix of 25 rows by 80 characters.

A microprocessor in the terminal is backed up by as much as 28k bytes of P/ROM and 16k bytes of RAM, plus 48k bytes of RAM for refresh. Manufacturer furnished software provides high level graphics functions (vectors, conics, plots, bar charts). ASCII test-strings can be easily transmitted via communication link from the host computer. Further control software can be developed also by the user.

Circle 405 on Inquiry Card

THIS IS THE ONLY DECENT LOW COST 165 CPS MATRIX PRINTER YOU CAN GET IN VOLUME RIGHT NOW.



Other people make them, of course. But you can't get them in volume. Unless you're willing to wait a very long time. And in this business a printer you can't get is about as useful as all those wonderful products that haven't been invented yet.

Even if you did have a wide variety to choose from, you'd probably choose our Matrix printer anyway. Microprocessor control makes it efficient, fast and reliable. And it's programmable from your computer or optional keyboard.

Bidirectional printing and paper feed gives you true graphics capabilities. Special character sets, including foreign language alphabets, provide incredible flexibility. And when you add the optional keyboard, it becomes a remote communications terminal.

Matrix is compatible with all industry standard RS-232-C or parallel interfaces, so you can plug it in just about anywhere.

If you need a good matrix printer in volume and you can't wait forever, contact one of our local sales offices or the Director of OEM Sales, Microdata Corporation, 17481 Red Hill Avenue, P.O. Box 19501, Irvine, CA 92713. Telephone: 714/540-6730. TWX: 910-595-1764.

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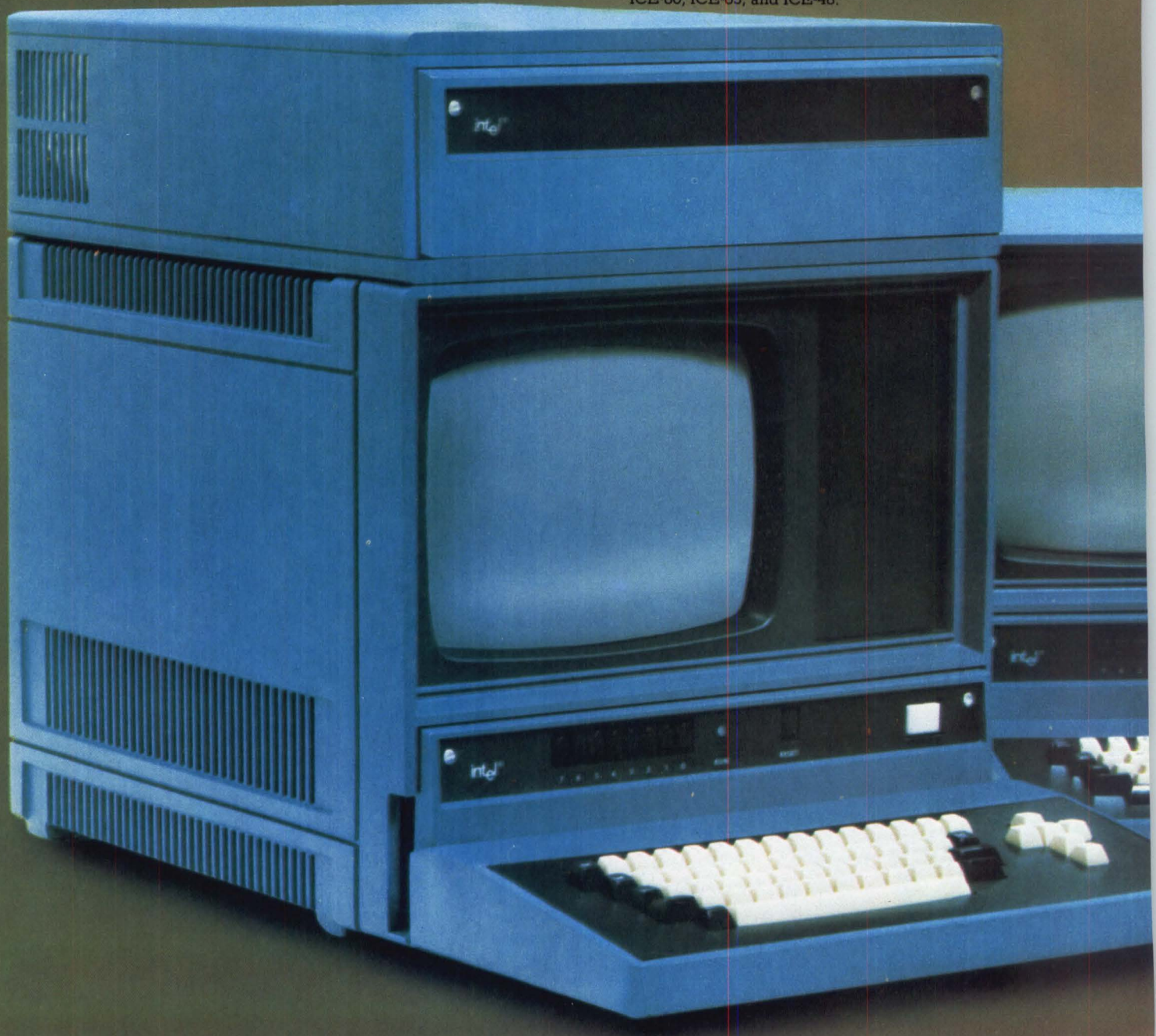
Intel's amazing new generation
Intellec® Series II
Microcomputer Development Systems
. . . everything you'll ever need to
develop a microcomputer-based product.

The Intellec Models 210, 220 and 230 are the first fully integrated, packaged tools for developing and testing your microcomputer-based products. They'll each fit easily on your lab bench to help cut months from your design cycle.

You can rent the newest generation microcomputer development systems today from REI and start taking advantage immediately of the fast, flexible and cost-efficient Intellec systems. Each can help you build a more reliable product. And because these new Intellec systems are so compact, they use less of your valuable laboratory bench space than any other microcomputer development aid on the market.

Model 230 is the most powerful member of the Intellec Series II family, providing you two double-density floppy diskettes with over 1-million bytes of on-line data storage, 64K bytes of RAM and an integral CRT.

The compact Model 230 also gives you a detachable, typewriter-style keyboard with upper and lower case characters and cursor controls. Its powerful ISIS-II Diskette Operating System has relocatable and linkable software and allows the use of two high-level programming languages, PL/M-80 and FORTRAN 80, plus the microcomputer industry's most comprehensive line of macro assemblers. The system has over 1-million bytes of on-line diskette storage and will support up to 2½-million total bytes. The System Monitor (in ROM memory) provides a Self-Test system diagnostic, and interfaces for a printer, paper tape reader/punch and universal PROM programmer are also provided. Model 230 gives you access to all the tools needed for your development work, including software editors, assemblers, compilers and debuggers, plus Intel's famous In-Circuit Emulators — ICE-80, ICE-85, and ICE-48.



...NOW...

For medium-scale system development, you can rent the Model 220. Now.

The Intellec Model 220 is also a complete packaged development system. It has an interactive, 2,000 character CRT with typewriter-style keyboard and a full-sized 256K byte floppy diskette drive and 6-slot MULTIBUS card cage in one compact unit. Model 220 gives you 32K bytes of RAM program memory and 4K bytes of ROM. The ISIS-II Diskette Operating System has a relocating 8080/8085 assembler, and the new system interfaces directly to the ICE In-Circuit Emulators.

The Intellec Model 210 rents for the lowest price of any packaged, full support development system available—anywhere.

Model 210 gives you the minimum system required for the rapid, efficient development of microcomputer software. It has a ROM-based editor/assembler combination which allows the development of small 8080 or 8085 programs completely in RAM memory, which minimizes your use of paper tape. Plus, you can also rent a ROM assembler/editor for Intel's family of MCS-48 single-chip microcomputers. The compact Model 210 has 32K bytes of RAM, 24K bytes of ROM and its own microprocessor. Self-test diagnostics capability is built-in. And it's easy to get started, too. All you have to do is interface the Intellec 210 to your terminal.

You can extend the powerful resources of an Intellec Series II system into your own prototype for fast and efficient software debug in your product's final hardware environment. Just put your product on ICE . . . ICE-80, ICE-85, or ICE-48, all off-the-shelf at REI.

To emulate your own CPU or your entire prototype system in real-time or single-step mode, simply rent the appropriate In-Circuit Emulator module to match your system's microprocessor. And you can begin software debugging as soon as your prototype has a processor socket and bus structure.

Capability-enhancing peripherals are available for short-term rental, too.

You can add to the already extensive capabilities of the Intellec Series II system with a variety of immediately available peripherals. These include two Intellec Printers, two diskette-based peripherals (one single-density with ½-million bytes of storage, the other double-density with 1-million bytes of storage). You can also choose a high-speed paper tape reader and a universal PROM programmer . . . all of which are for rent today from REI.

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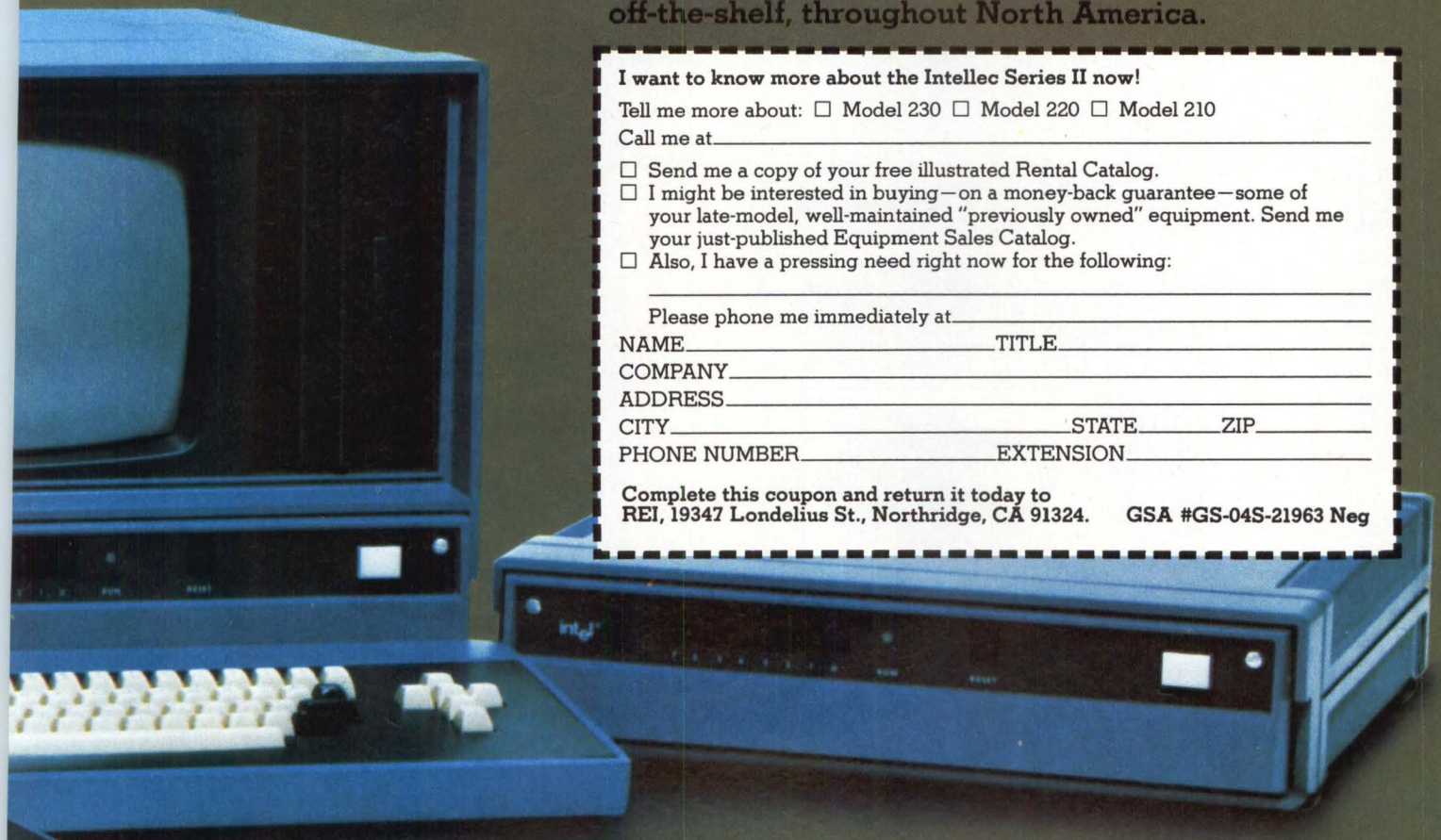

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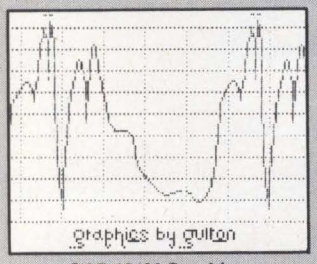
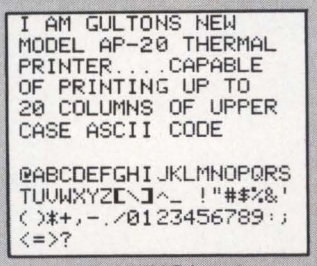
CIRCLE 40 ON INQUIRY CARD

New Fixed Head Digital Thermal Printers & Mechanisms

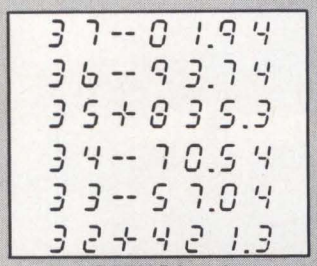
Complete printers with case, interface and drive electronics or stripped down mechanisms.



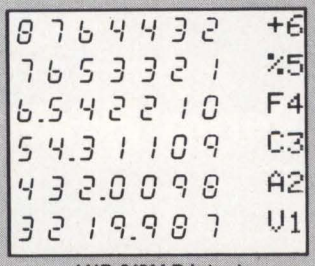
GAP-101M Graphics.
100 million dot line MTBF.



AP-20/20M Printout.
20 million character lines MTBF.



NP-7/7M Printout.
10 million character lines MTBF.



ANP-9/9M Printout.
10 million character lines MTBF.

Gulton's fixed head printers give you printouts like these with the quietness of non-impact thermal printing and the reliability of solid state switching.

You get these advantages, 1) only one moving part—the paper drive, 2) independence from ink supplies and ribbon mechanisms, 3) high character quality and 4) extremely high reliability.

Compare the advantages of Gulton's fixed head printing technique to the drawbacks of other printing methods: the noise created by the hammer and drum technique, the unreliability of the moving head wire matrix technique with its routine solenoid failure, or the electrosensitive technique with its RFI and contamination problems.

Complete Printers/Mechanisms

- AP-20/AP-20M alphanumeric printer with exclusive overlapping dots for exceptional character definition . . . 20 columns of 5×7 characters at up to 2.5 lines/sec.
- NP-7/NP-7M has seven columns of exceptional character quality 7 segment numbers at up to 4 lines/sec.
- ANP-9/ANP-9M is same as NP-7/NP-7M, but has two additional dot matrix I.D columns, up to 2.5 lines/sec.
- GAP-101M is for simultaneous analog, alphanumeric (10 columns 7×9 or 14 columns 5×7) and grid pattern printing. Up to 30 overlapping dot lines/sec. for exceptional graphics and character definition.

AP-20M Mechanism

NP-7 Numeric Printer

Write or call now for detailed catalogs.

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CIRCLE 41 ON INQUIRY CARD

DC&AS BRIEFS

Microcomputer Allows Direct Drive of Vacuum Fluorescent Displays

A single-chip microcomputer that is particularly suited for use as a controller in process and industrial controls, the S2000A allows 26-V direct drive of vacuum fluorescent displays and provides access to all registers and memory for debug and test. Introduced by American Microsystems Inc, 3800 Homestead Rd, Santa Clara, CA 95051, the microcomputer includes 1k bytes of ROM and 256 bits of RAM, as well as 7-segment display decoders, onchip. It provides for eight inputs and eight bidirectional 3-state lines.

Instruction execution cycle time is 4.5 μs. Of 51 1-byte instructions, 49 are executable in a single cycle. Chip architecture provides a 3-level subroutine stack. All registers, as well as ROM and RAM, are accessible for debug and test.

Software and hardware support includes a development center with two floppy disc subsystems, CRT terminal, and printer, with full capability for text editing, macro assembly, simulation, realtime debugging, and P/ROM programming. Other support available includes an EPROM emulator, a software controlled logic analyzer, and field and factory application engineering support.
Circle 406 on Inquiry Card

CNC Systems Handle Multi-Axis Machine Tools

Two low price computer numerical control systems for machine tools have been introduced by the Bendix Corp Industrial Group, Southfield, MI 48076. System 5M can be supplied as either a standalone controller or three or more separate modules for incorporating into the customer's enclosure. This system can handle nearly any task on standard type NC machine tools having up to four axes of control and is designed for machine tools selling in the under $100,000 market. Standard features include universal displays, diagnostics, industrial microprocessor, programmable interface, tool compensations, software travel limits, and interface interrogation from the MDI (manual data input) keyboard. Standard software is provided with the unit's softwired programmable interface. Optional features include a CRT display, part program edit, helical interpolation, lead screw error compensation, macro programs, and special customer-prepared canned cycles. Greater memory and interface capacity can be added.

System 5A complements the 5M by extending CNC to four axes of control and more. It features a floppy disc memory module plus an advanced editor, tool nose radius compensation, and industrial microprocessor.
Circle 407 on Inquiry Card

The quarter billion keyboard. Our unique "Golden Touch" capacitive keyboard is rated at 250,000,000 MCBF per keyswitch. That's at least double anybody else's rating. New patented features make the "Golden Touch" exceptionally resistant to moisture, dust and electrical noise. We guarantee a 1% AQL and give a two-year warranty. Every "Golden Touch" we produce is designed precisely to *your* specifications... because we sell only to volume OEM manufacturers. So *you* name whatever options, circuitry, configuration and legends *you* want. All this at competition-beating prices.

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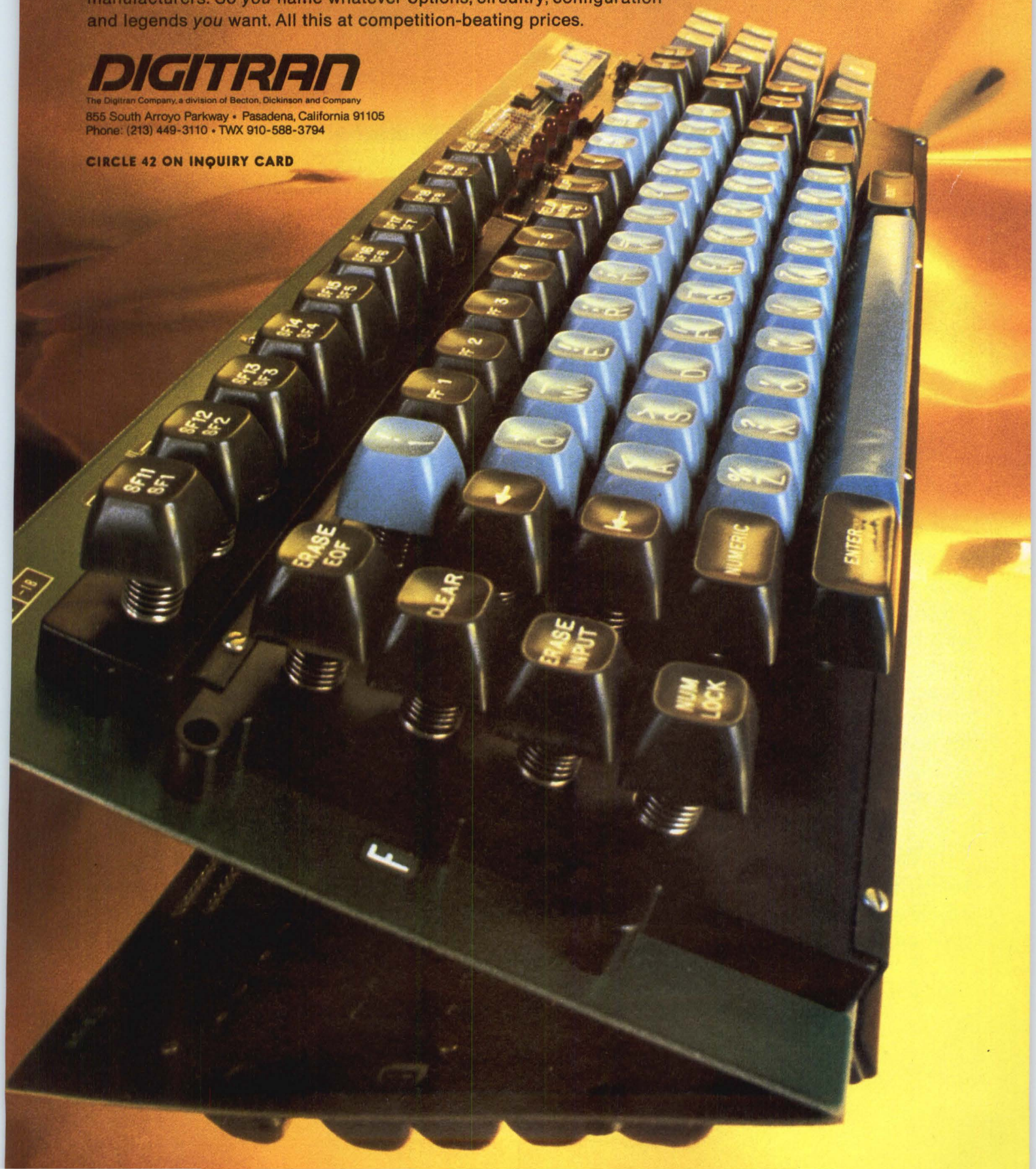
CIRCLE 42 ON INQUIRY CARD



From CPU to software, It's the beginning of a new

Intel's new 16-bit microcomputer is here. It's the 8086, designed to deliver ten times the processing power of our 8080.

More important, right now you can get CPU, memory, peripherals, software, development tools and design assistance. We've made MCS-86™ the most comprehensive microcomputer system ever introduced.

Our challenge was to build the most advanced 16-bit microcomputer. And to give 8080 and 8085 users a direct upgrade path. We accomplished it. The 8086 is the world's most advanced microprocessor. Yet it's a direct evolution of our 8-bit 8080 and 8085. It's software-compatible with both, supporting all their instructions in addition to its own advanced instructions. And the 8086 utilizes readily available Intel microcomputer peripheral chips and low cost, standard MOS memory.

8086 is an architectural triumph, etched in HMOS. The standard 8086 delivers 5 MHz speed. And it delivers direct addressability to a full megabyte of memory, with both 8-bit and 16-bit signed or unsigned multiply and divide in hardware. It gives you efficient byte-string operations and improved bit manipulation. Plus it provides capabilities never before supported by a microprocessor, such as dynamic relocation, reentrant code, position-independent programs and instruction look-ahead.

All in all, 8086 sets a new standard for microcomputer processing capabilities.

We designed MCS-86 for design flexibility. It can operate on a full set of 16-bit registers, or on an 8-bit subset which corresponds to the 8080 register set. That makes MCS-86 adaptable to traditional 8-bit applications as well as larger, more complex applications.

A minimum MCS-86 configuration includes only the CPU, the 8284 Clock Generator, two 8282 Octal Latches, 2K bytes of 2142 RAM and 4K bytes of 2716 EPROM.

MCS-86™ is here today. era in microcomputers.

For easy expansion, add our 8288 Bus Controller, which generates Multibus™ timing signals. And, using our 8286/8287 Octal Transceivers, MCS-86 interfaces with larger, buffered systems.

Get started with software now using our Intellec® development system and PL/M 86, an expanded version of our popular PL/M high level language. And, with the ASM 86 assembler, you can write assembly language programs for your MCS-86 designs and translate your existing 8080 and 8085 software to run on 8086. Both PL/M 86 and ASM 86 operate under ISIS-II, Intellec's advanced operating system.

MCS-86 components are available today. Order your MCS-86 Prototype Kit from your local Intel distributor. The kit includes all the essential components to begin your evaluation of this new era in microcomputers. Or, for more information, contact your local Intel sales office or write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.

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Japan: Intel Japan, K.K., Flower Hill-Shinmachi East Bldg. 1-23-9, Shinmachi, Setagaya-ku, Tokyo 154. Telex 781-28426.

CIRCLE 43 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS

Computer Hierarchy Handles Data Acquisition In Multiple Factory Complex

A data acquisition software package for its series 300 process computer system has been developed by Siemens AG, Postfach 103, D-8000, Munich 1, Federal Republic of Germany. The Seda 300 enables acquisition of data on processing operations in several production areas on a hierarchical network. (This system is not marketed in the U.S.)

In conjunction with a major metal-working company, a distributed processing network is being developed using both 330 and 4004/151 computer systems. Seven plants with all different production programs and all widely scattered throughout the Federal Republic will be controlled from a single computer center.

Online acquisition of production data will be maintained in real time at the individual factories by 330 computers using visual display units and terminals. Two 4004/151 computers at the highest level of the hierarchy will be in constant contact with the smaller computers and will process all data.

Circle 408 on Inquiry Card

Industrial Emission Monitor Separates and Collects Respirable and Nonrespirable Particles

When federal and state environmental monitoring agencies finally establish particulate emission regulations for industrial firms, a microprocessor-based system introduced by Beckman Instruments, Inc, Process Instruments Div, 2500 Harbor Blvd, Fullerton, CA 92634 will be available to determine if those regulations are being met. The Samplair™ automated dichotomous particulate sampling system separates fine and coarse ambient aerosol particles and then collects each for study. (Particles of less than 2.5 μm can enter the lungs of humans; they are considered to be small. Those between 2.5 and 15 μm normally would be ejected by coughing and sneezing and are considered to be large.)

The system can be programmed to change sample filters automatically up to 36 times at predetermined intervals of minutes, hours, or days, or whenever the filters reach overflow conditions. Dichotomous sampling —simultaneous separation and collection of fine and coarse atmospheric particles—is done with an impactor operating at a total sample flow rate of approximately 16.7 liters/min (15.2 qt dry measure), or 1 m^3/h. About 90% of the flow goes through the impactor's fine particle channel; the rest goes through the coarse.

Filter insertion and retraction times, filter overload, and filter rupture are recorded automatically on the system's printer. If power fails, a built-in battery will maintain the timekeeping function for 30 min. The system is housed in a tamper- and weatherproof case that permits operation at temperatures from −40 to 50 °C (−40 to 122 °F) in 0 to 100% relative humidity, and at wind velocities of up to 20 km (12.5 mi)/h.

Circle 409 on Inquiry Card

Traffic Control System Matches Microprocessor Capabilities

Features of microprocessor systems are said to be equaled by a solid-state traffic control system that responds to traffic on a cycle to cycle basis. The standalone TRAC (traffic responsive arterial coordination) system can be used with most existing control equipment. Plug-in printed circuit assemblies use CMOS ICs and LED indicators. No program generation is necessary on this system designed by Tesco, 530 N Henry St, Alexandria, VA 22314.

A master controller coordinates a group of secondary controllers at arterial intersections. Only travel time in seconds is set at the secondaries; the onsite master handles cycle length, offsets, direction, and average flows.

Traffic entering the system is compared by the master to that in the system at a given time, and cycle and speed are automatically modified to alleviate congestion. A multiconductor cable or a pair of wires connect the secondaries to the master. The master receives data from detectors at each end of the system, determines automatically which lanes have heavier traffic and by how much, and assigns each vehicle an appropriate headway. The number of vehicles and their headways then establish how many vehicles may enter each artery. The quantity can be increased in 1-s intervals up to 240 on a cycle by cycle basis without noticeably affecting the constant system speed. Interval timing on any standard solid state controller ranges up to 99 in 1-s increments.

Circle 410 on Inquiry Card

High Level Language Interpreter Reduces Programming Time for Process Control Systems

A BASIC interpreter designed specifically for 8080 compatible microcomputer systems for process control, automatic testing, and data acquisition is said to reduce programming time by up to 90%. XYBASIC is a high level language announced by Mark Williams Co, 1430 W Wrightwood Ave, Chicago, IL 60614 for use with systems based on 8080, Z80, 8086, and 8085 microprocessors and reportedly provides control, use of read-only memory, and capability for customizing input/output features. The 7k-byte interpreter with built-in editor allows programs to be entered directly into memory. As little as 5 s are needed for loading into a microcomputer or development system.

Control features include software interrupt capability that allows the system to monitor external devices and execute a program at the same time. It checks automatically to see if the specified condition is met before executing each program statement. In addition, a delay command builds realtime delay into the program without adding a realtime clock. Other control features include commands to examine and modify any location in the computer's memory, to input or output at the machine level, and to look at any individual bit on any port. A number of bit manipulation commands are included, and a run-time/compiler package produces standalone systems that execute without special operator startup commands. This package compresses the code, allows programs to run anywhere in memory, and increases execution speed. □

Circle 411 on Inquiry Card

Our Wildest Card Yet

A programmable 16-line multiplexer that beats everything in its class

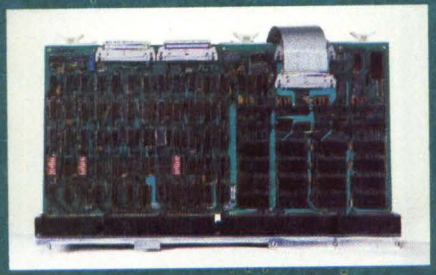
PDP-11 users, we have another winner for you. This time it's DMAX/16™, our new programmable multiplexer for connecting your PDP-11 to 16 asynchronous serial communications lines. DMAX/16 makes the most of the 11's DMA capabilities to establish computer overhead at a level far below that of competitive units like the DJ11 and DZ11. It also offers software compatibility with the DH11... in one-fourth the space!

Now, for the first time, you don't need an expansion box or special back planes. DMAX/16 consists of two hex boards which install easily into standard SPC slots units and connect to the current loop or EIA/RS-232 panel by separate flat-ribbon cable. As many as 16 can be placed on a single PDP-11 for a total of up to 256 lines. A DMUX/16™ option allows modem control for 16 channels.

DMAX/16 provides complete program control of the lines, each of which operates with several individually programmable parameters, such as character length and number of stop bits. Parity generation and detection are odd, even or none. The operating mode is half duplex or full duplex. Fifteen software programmable baud rates: 0 to 9600 baud – plus 19,200 baud – and an external baud rate. Breaks may be generated or detected on each line and the unit can echo received characters without software intervention.

Play the wild card now. You'll get top performance and a competitive price advantage of at least $1000 along with delivery from stock as usual. Write for details and find out why we consider ourselves the leader among manufacturers of DEC enhancements.

Able Computer Technology, Incorporated,
1751 Langley Avenue, Irvine, California 92714.
(714) 979-7030. TWX 910-595-1729



Able, the computer experts

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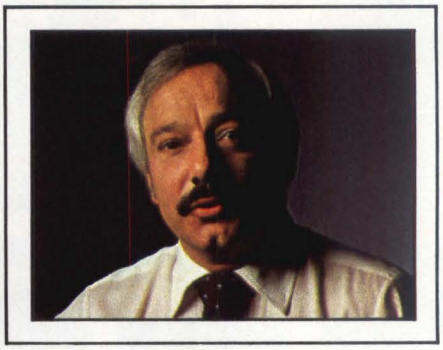
CIRCLE 44 ON INQUIRY CARD

"Any minicomputer memory can make a mistake. The trick is to make a system that corrects mistakes. And that's what makes ours so remarkable."

Bill LeDuc
Product Manager

3



NS D/3 Add-In Memory

"Of all the places I've seen, National Semiconductor has really got things figured. As a second source for minicomputer memory, we can take what's good about a product, design in some useful new wrinkles and make it even better.

Take Data General's Nova 3 memory. Basically, it's a fine system. But it won't correct soft errors. So we created a system that will—the NS D/3 add-in memory, with optional ECC capability that corrects any single-bit soft error. And identifies any double-bit error. A customer can now get ten times the mean time between failure that he can with Data General's system.

We also hit on a way to make the NS D/3 four times denser than Data General's memory. So it uses less power. And space in the chassis is freed up so smaller system packaging is possible.

Control from silicon to systems.

You can't test reliability into a product. By test time, reliability either is or isn't there. What testing does is help us screen out the marginal components before our boards wind up in somebody's system.

So we test. From components to the finished product — from silicon to systems. We run final systems through *three* characterization tests at three stages — over seventy-two hours. We even retest components from our own Components Division. I don't take anything for granted.

We're actually one of the few outfits in memory on both a components and systems level. This gives us a better understanding of the total product — especially in custom systems, where an intimate knowledge is a huge benefit in building memory to customer specs.

I'd say National now makes over 90% of the components in a typical finished memory system. Which is why our systems check out so successfully first time through a test.

With this kind of control we can and do offer a full one year warranty on our NS D/3. Sure, we provide error correction circuitry. But we try like crazy to make sure a customer doesn't need it.

Planned non-obsolescence.

Our customers have enough to do without worrying about memory systems. So we worry for them.

We have a whole group of people who do nothing but create and innovate with state-of-the-art technology. They're the reason our card level products now range from 4K to 128K and up.

National's committed to the memory business. When you deal with us, you don't just get memory chips, you get your own engineering department, your own support people. We even have a quality assurance group that answers directly to top management. That's unusual.

Our people are good. They're creative, open and they live and breathe memory systems. And we're looking for more of them all the time.

If you'd like to know about what we can do for you, write me personally: Bill LeDuc, Product Manager, Memory Systems, National Semiconductor Corporation, Drawer 15, 2900 Semiconductor Drive, Santa Clara, California 95051. Or call 800-538-1866 — 800-672-1811 in California."

Computer Products Group
≈ National Semiconductor Corporation

A thorough examination will be given microprocessors in the 35 professional program sessions scheduled for Midcon/78 in Dallas. Also to undergo close scrutiny during the 3-day program are solid-state memories, bubble and CCD memories, telecommunications, and speech synthesis. All technical sessions and exhibits will be at the Dallas Convention Center.

A Keynote Luncheon scheduled for 12:00 noon on Monday, December 11, will mark the formal opening of the Conference. An address given by Pasquale Pistorio, executive vice president of Motorola Semiconductor, will highlight the Luncheon; in his address Mr Pistorio is expected to discuss development of the worldwide electronics market and its effect on the U.S. industry.

Scheduled for Monday and Tuesday at the Hyatt Regency Hotel, a hands-on tutorial seminar on microprocessor applications will include direct experiments with computer programs. Participants will be introduced through experimentation to programming principles, keyboard control, data acquisition, and interrupts and input principles.

Mariachi music, margaritas, and nachos will set the tone for "Viva La Reunion," the tradi'ional All-Industry Reception, Tuesday evening from 6:30 to 8:30 pm, in the Hyatt Regency's Reunion Ballroom. This Mexican style holiday will allow conference attendees to renew old acquaintances and make new ones.

Occupying East and West Halls of the Dallas Convention Center, exhibits will offer attendees an opportunity to view the lastest offerings of mini and microcomputers, instrumentation and control systems, production, packaging, and test equipment, components, microelectronics, and electro-optics. A special exhibit saluting the microprocessor and its effect on the industry will consist of 21 applications in 7 categories. Each displayed product will be chosen by a panel of judges, which will also select one product in each category for an award of excellence and merit. The Midcon Film Theater will operate between 10 am and 4 pm each day, presenting technical and scientific films selected by a panel of judges.

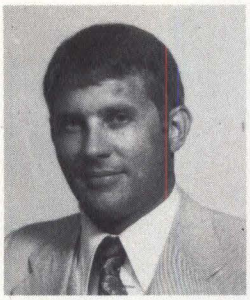
To ease traffic and parking problems free shuttle buses will operate between downtown hotels and the convention center, running at 15-min intervals from 30 min before the show until 30 min after closing each day. Surtrans buses will provide regular service between major hotels and the airport; fee is $4.

Midcon is cosponsored by regional sections and local chapters of the Institute of Electrical and Electronic Engineers and the Electronic Representatives Association. Further information may be obtained from Midcon/78, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965.

To be held at 10 am and 2 pm each day, professional program sessions will cover technical topics including state of the art presentations on both hardware and software applications for microprocessors. Energy systems, communications satellites, fiber optics, and custom LSI are other topics to be considered. Only sessions of particular interest to *Computer Design* readers are covered in the following pages. Information is necessarily limited to that available at press time.

Midcon/78

Electronic Show and Convention
Dallas Convention Center/December 12-14



Dr John L. Fike
Program Chairman

Pasquale Pistorio
Keynote Speaker

Professional Program Excerpts

Tuesday Morning

Session 1 **10 am-12:30 pm**

Single-Chip Microcomputers— Distributed and Multiprocessing Techniques

Organizer/Chairman: Jim Vittera, Mostek Corp

Now that first generation 8-bit single chip microcomputers have been available for over a year, it is appropriate to explore their future. This session attempts to determine the architectural evolution of these original devices and to investigate the implementation of large computer concepts such as multiprocessing and distributed processing as they apply to single chip microcomputers.

"Multi-Microcomputer and Distributed Architecture Systems with the M6801 Single-Chip Microcomputer," Mike Wiles and Fuad Musa, Motorola Inc

"A Distributed Processing Application Using Single-Chip Microcomputers," Don Phillips, Intel Corp

"Using the TMS 9940 in a Multiple Processor Environment," John D. Bryant, Texas Instruments

"Distributed Processing Using 3870 Single-Chip Microcomputers," Bob Burckle, Mostek Corp

Session 2 **10 am-12:30 pm**

Minicomputer Software Productivity

Organizer/Chairman: Andrew A. Allison, Intersil Inc

Advances in semiconductor technology during the last 8 yrs have drastically reduced the cost of computer components. Improvements in software productivity, however, have been modest. In addition, the extensive use of read-only memory within microcomputers adds to the high cost of software maintenance. An experienced user, two manufacturers, and an independent software vendor address the problem.

"Learning to Live with the Microprocessor," Burt Masnick, Hazeltine Corp

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When you're down to the wire

CIRCLE 45 ON INQUIRY CARD

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"Only one DIP socket gives you all the best features. And more.

New DIPLOMATE— from AMP."

The new low profile Diplomate combines the best engineering features with AMP's own exclusive contact design innovations. Here are some of its outstanding advantages:

1. Metal-to-metal-to-metal contacts with dual side-wiping action ensure low contact resistance and excellent electrical reliability.
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3. Exclusive tapered lead-in ramps in large target area make IC insertion faster and easier. Diplomate pc board insertion is also easy and compatible with virtually any automatic insertion equipment.
4. Anti-overstress contact design preserves contact spring integrity for continuous, long-term reliability.

New Diplomate sockets help you get the most from your designs in many other ways:

- Higher densities. Low profile packages are stackable end-to-end for more circuits in less space.
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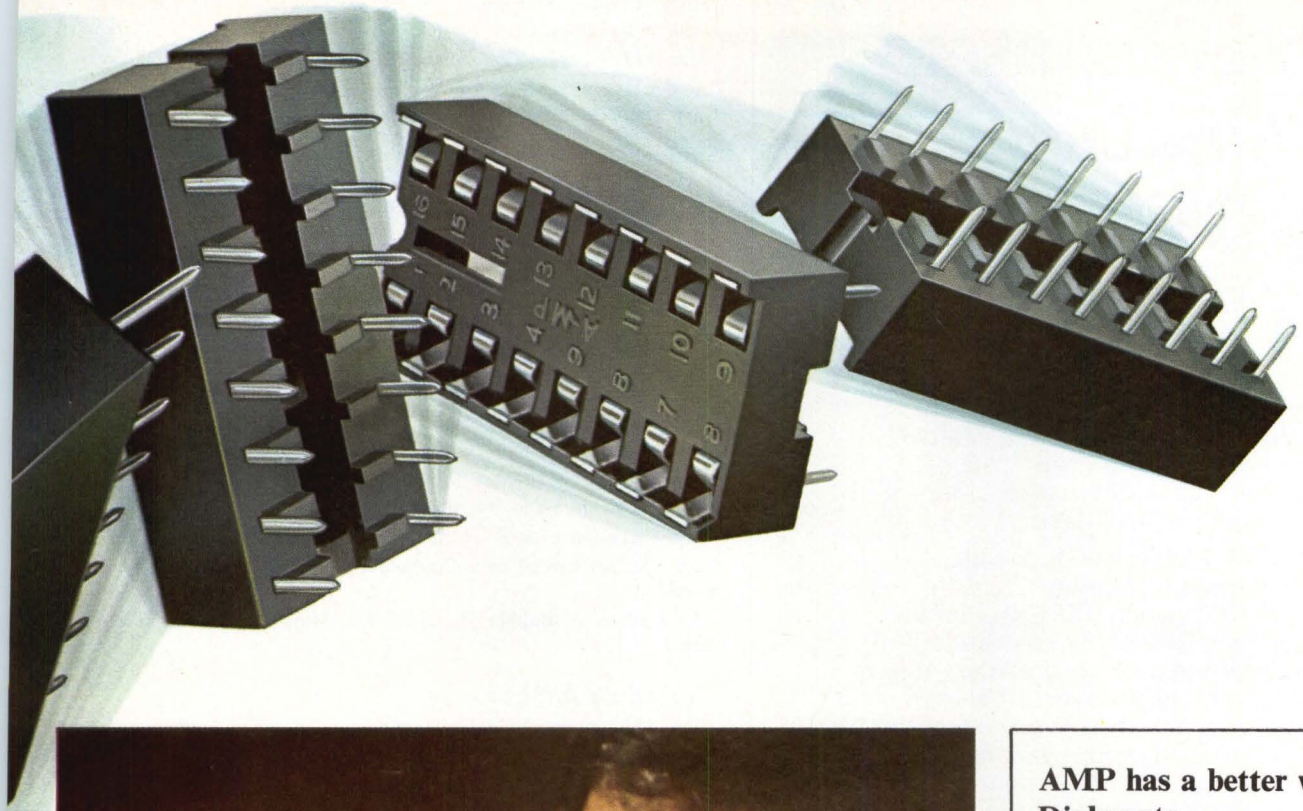
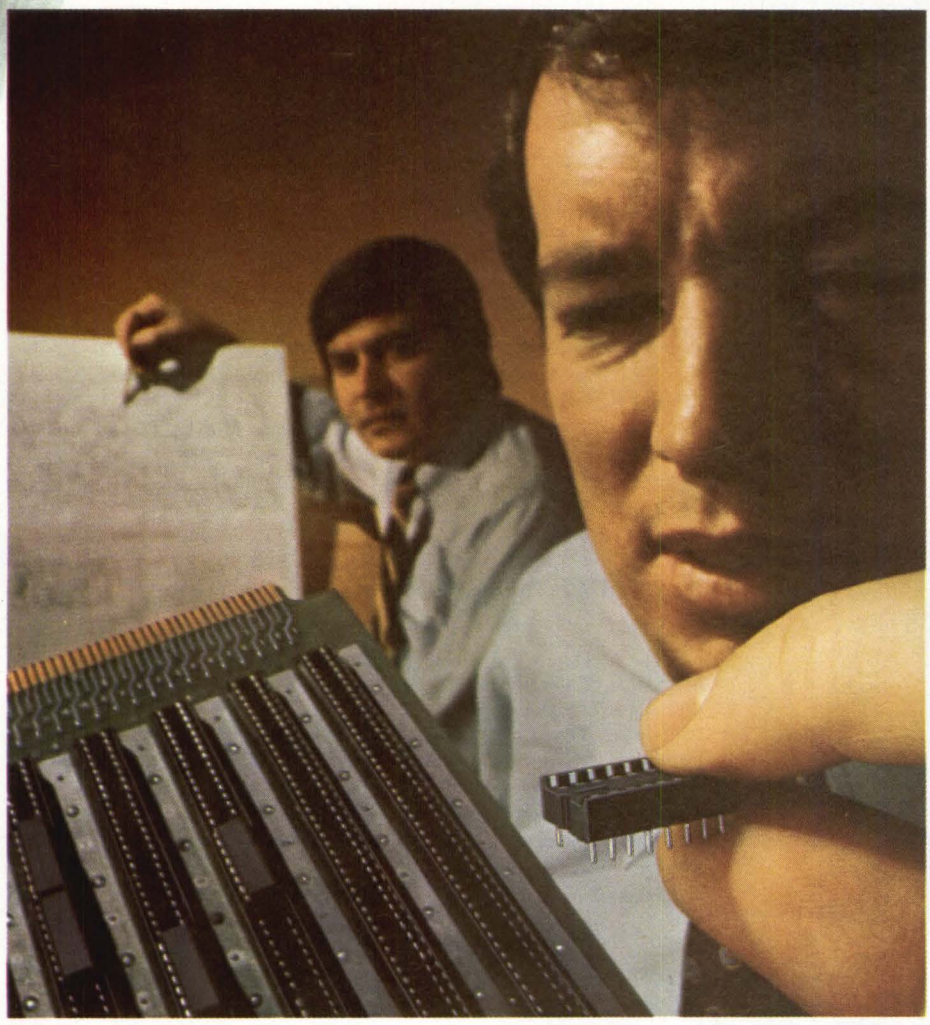
- Full variety of sizes. Complete family of sizes available ranging from 8 to 40 positions.
- Complete technical support. Solid engineering aid is yours for the asking from AMP. And it's available worldwide.

There are more reasons why new Diplomate is the better way, including its competitive prices. For more information, just call Customer Service at (717) 564-0100. Or write AMP Incorporated, Harrisburg, PA 17105.





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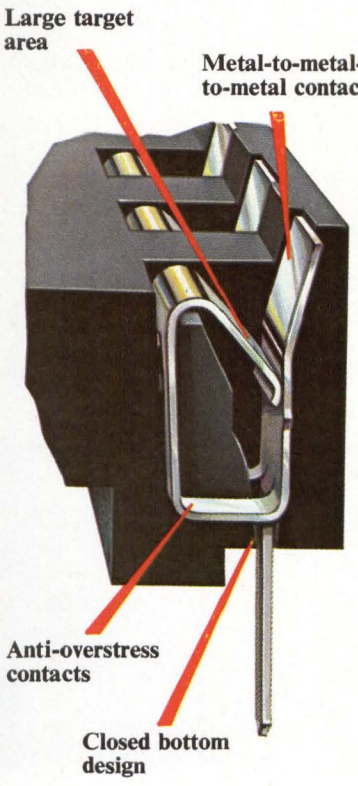

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"High Level Language Productivity/Maintainability Benefits," Stephen M. Hicks, Forth Inc

"Standard Software Components," Joseph P. Harakal, Intel Corp

"A CPU Architectural Approach to Software Productivity," R. Gary Daniels and Gary Summers, Motorola ICD

Session 3 **10 am-12:30 pm**

Technology Advances in Solid State Memory and Their Products

Organizer/Chairman: Sam Young, Mostek Corp

Although integrated circuit memories have been targeted at displacing core in mainframe applications, cost and product breakthroughs during the past several years have opened new markets. This session will discuss the major technologies, their products, and applications available today and in the near future.

"The Impact of VMOS on Semiconductor Memories," Chris Peterson, AMI

"Applications of Bipolar Isoplanar Memories," Bruce Threewitt, Fairchild Camera and Instrument

"The Evolution of MOS Technology," Sam Young, Mostek Corp

"CCD—A Lab Circuit or a Production Part," Milt Gosney, Mostek Corp

"An Update on Bubble Memory," Bill Mavity, Rockwell International

Tuesday Afternoon

Session 7 **2-4:30 pm**

Microprocessor Architectural Trends

Organizer/Chairman: Michael Smolin, National Semiconductor Corp

Papers address new trends in advanced 16-bit microprocessor characteristics—architecture and its ramifications in language, I/O structure, and peripheral utilization. Presentations will be followed by a panel discussion and questions from the audience.

"Advanced Microprocessor Trends," Michael Smolin, National Semiconductor Corp

"The Architecture of Peripheral Intercommunications," Art Gruszynski, American Microsystems Inc

"Distributed Processing with 16-Bit Microprocessors," Dane Elliott and Bert Hill, Intel Corp

"The 16-Bit One-Chip Computer," Tom Miller, Texas Instruments

"Z8000—A New Generation 16-Bit Microprocessor," Ken McKenzie, Zilog Inc

Session 8 **2-4:30 pm**

What's Happening to Personal Computers?

Organizer/Chairman: Narpat Bhandari, Signetics Corp

The explosive growth of computers for personal use has just begun. What seems to have started for a hobby market now becomes a major consumer product. To update current and future trends in personal computing, several currently available computers such as Apple-II, Commodore PET, Radio Shack TRS-80, and Videobrain will be described with users in mind and the personal computer of 1980 will be discussed.

"The Consumer Microcomputer—Appliance of the 80s," Phil Roybal, Apple Computer Inc

"Timeshare at Home," David H. Chung, Umtech Inc

"The Personal Computer: Lab and Office Now; Kitchen Table Later," Charles I. Peddle, Commodore Business Machines

(Paper title to be announced), John Roach, Radio Shack

(Paper title to be announced), L. Hazan, Signetics

"A Personal Computing Survey," Carl T. Helmers, *Byte* Publications

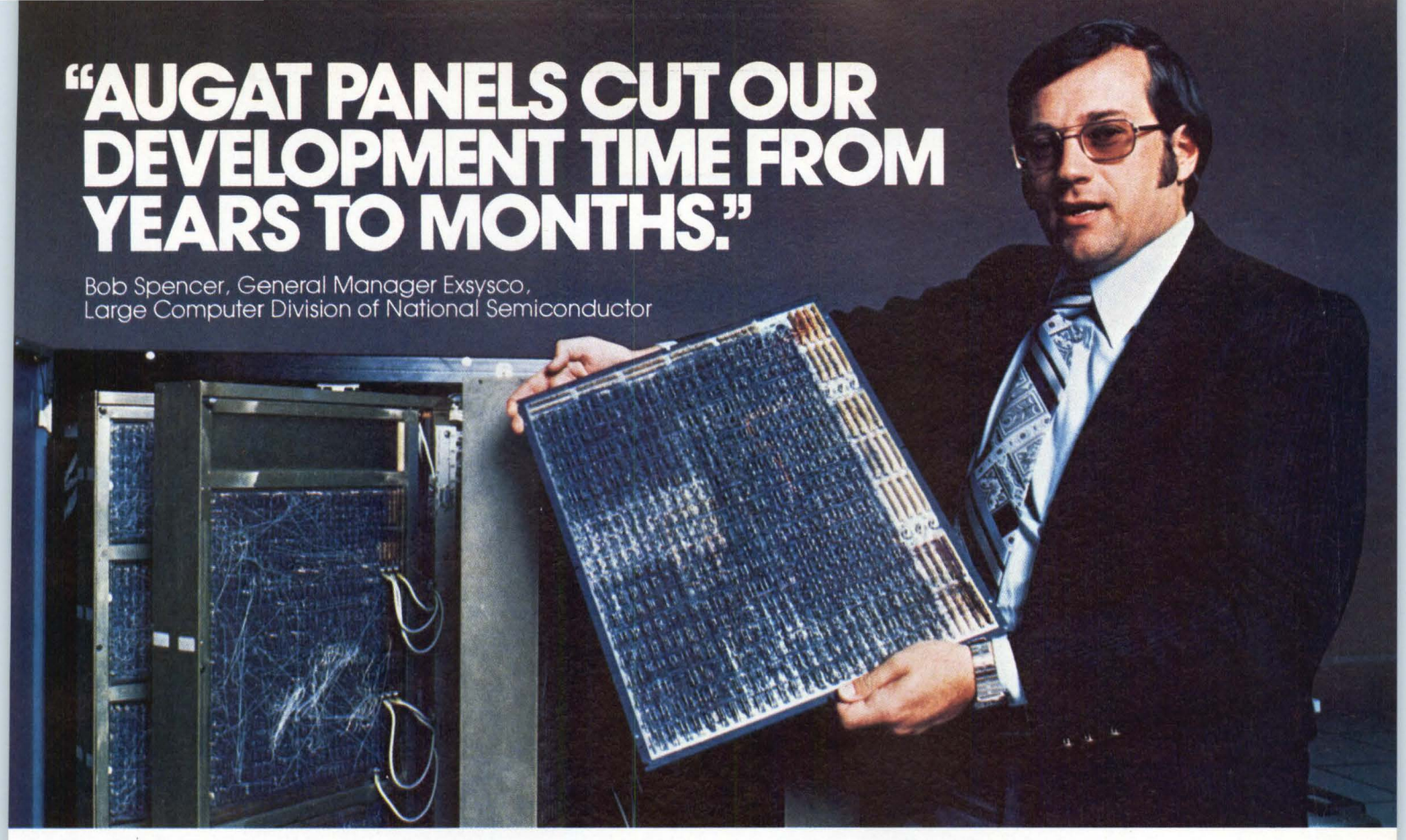
Session 9 **2-4:30 pm**

Bubble and CCD Memory Applications

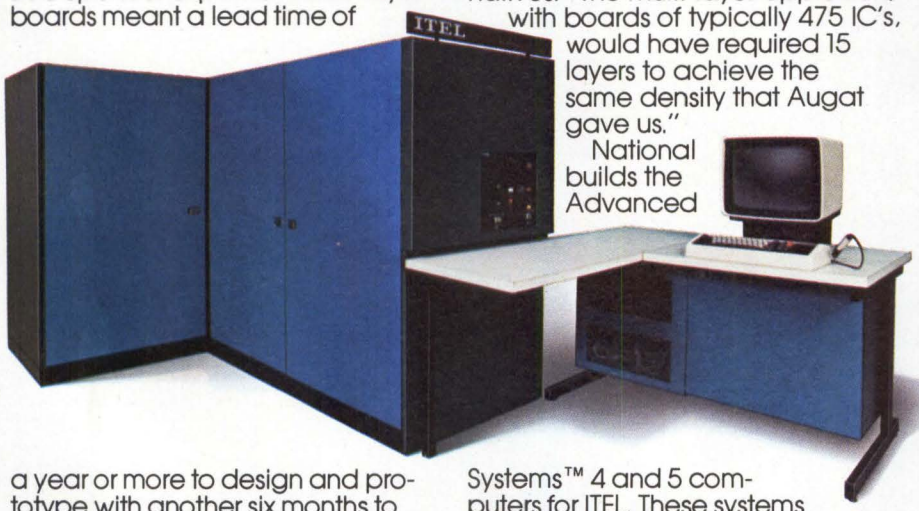
Organizer/Chairman: J. Egil Juliussen, Texas Instruments

"AUGAT PANELS CUT OUR DEVELOPMENT TIME FROM YEARS TO MONTHS."

Bob Spencer, General Manager Exsysco,
Large Computer Division of National Semiconductor



The dynamics of the computer industry demands that manufacturers capitalize on opportunities during the limited lifespan of the "current" technology. That's why initial development time is crucial. One sure way to cut that time is with Augat Wire-Wrap* panels. Bob Spencer explains: "Multi-layer boards meant a lead time of a year or more to design and prototype with another six months to get into production. With Augat boards, we reduced this cycle to a few months and started production the day we approved the prototype. Augat also gave us a flexibility to make circuit changes during the development cycle without causing delays."

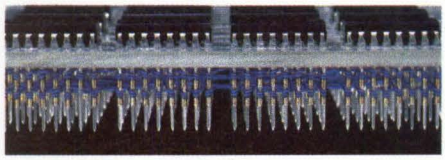


Time isn't the only consideration—cost is also critical. "The expense to design and develop dozens of different, large multi-layer boards can easily run into the hundreds of thousands of dollars, not to mention staffing and equipment. The Augat approach drastically reduced these costs allowing us to concentrate our resources on other critical design elements."

Packaging density is also vital in evaluating interconnection alternatives. "The multi-layer approach, with boards of typically 475 IC's, would have required 15 layers to achieve the same density that Augat gave us."

National builds the Advanced Systems™ 4 and 5 computers for ITEL. These systems must offer high reliability. "As the temperature inside a computer goes up, the reliability goes down. Augat boards reduce the temperature problem because Wire-Wrap pins are excellent radiators."

The benefits also carry into the field. "Thanks to Augat boards, service engineers can make any required changes using simple tools. And because the boards are designed with sockets, we make repairs or upgrade systems quickly by pulling the old chips and plugging in new ones. We also eliminated the cost and logistics of stocking hundreds of different, completed PC boards. Now we simply stock IC's."



How would Bob Spencer rate the performance of Augat Wire-Wrap panels? "Excellent! Our system uses high speed ECL throughout. Augat's patented logic panel, combined with unique automatic wiring from Augat's Datatex subsidiary, performs with no noise or transmission problems."

Throughout the computer industry, you'll find Augat boards at work in all kinds of logic applications delivering high speed performance and system flexibility at dramatic cost and time savings.

For further information, call Len Doucet at 617-222-2202. Or write Augat, Inc., 33 Perry Avenue, Attleboro, Massachusetts 02703.

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Augat interconnection products, Isotronics microcircuit packaging, and Alco subminiature switches.

CIRCLE 48 ON INQUIRY CARD

We'd like to show you around the MSC 8001 Z80/MULTIBUS Single Board Computer

Take the MULTIBUS.™ The MSC 8001 is fully hardware and software compatible with the industry standard SBC 80™ MULTIBUS. Use with any of the wide variety of SBC 80 compatible components to shorten product development cycles. No need to spend extra time and money on basic software development, either. The 8080's software will work just fine.

See the Z80™ perform. Our star attraction is the Z80 CPU, with its expanded instruction set and high speed program execution. The built in eight levels of priority interrupt are at your disposal and more! The Z80 has a non-maskable interrupt you can use to implement power-fail recognition or to assist in debugging.

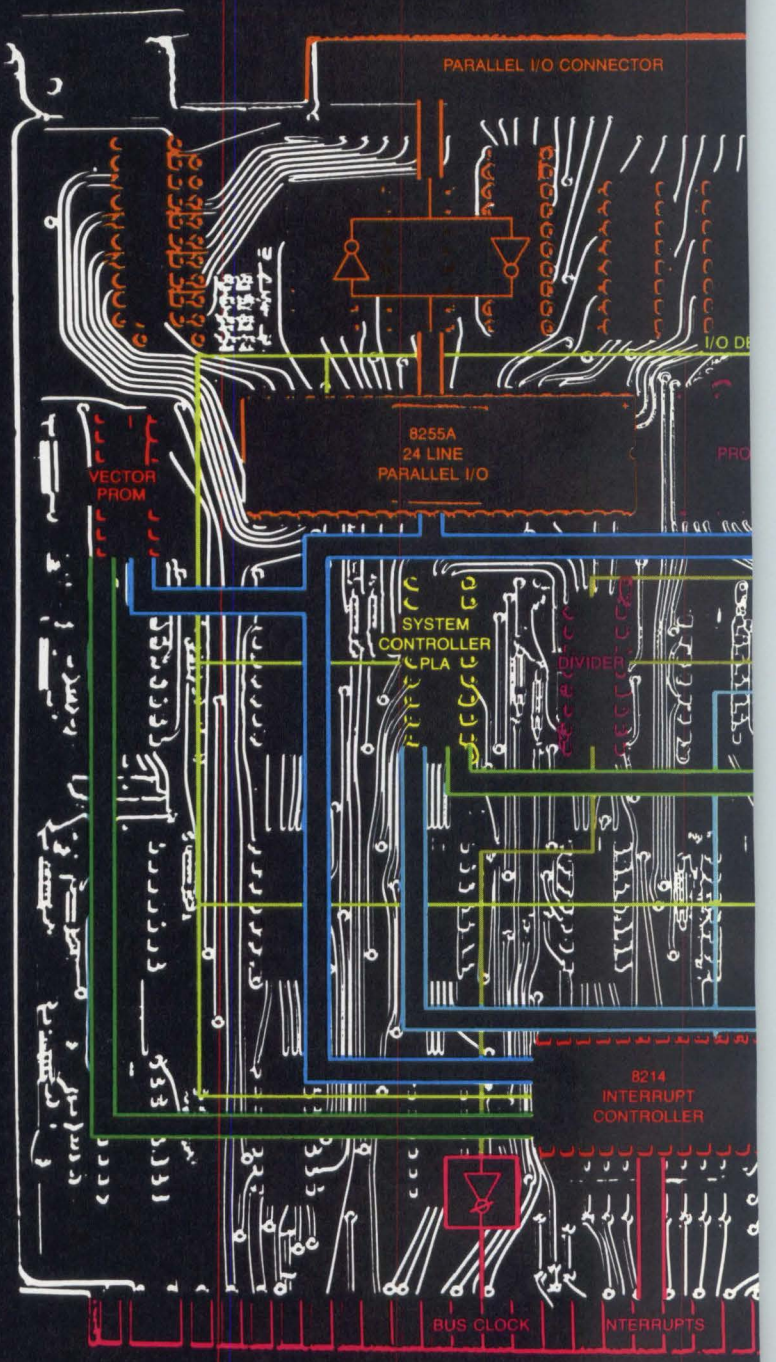
Remembering the way. Our memory gives you up to 8K RAM and up to 16K ROM on board! The need for costly additional memory has now been eliminated in many applications.

Mix and match. You can install identical or completely different 8 bit EPROMs, ROMs or PROMs. Now store commonly used sub-routines in ROMs in one or two sockets, and your own applications programs in EPROMs in the others. Using 4K elements you can have up to 16K bytes.

Got a transfer? During Direct Memory Access transfers, the MULTIBUS can access all of our on-board memory. Use the RAM for intermediate storage for a high speed video display or floppy disk controller.

Along the serial way. Programmable serial I/O interfacing for asynchronous and synchronous terminal devices is provided by the MSC 8001. Whether you require TTL, or optically isolated 20mA current loop, it's all on the board. With us you won't need any external converters to handle your Teletype. ®

Parallel ins and outs. Two programmable ports offer 48 lines of parallel I/O. Inverted and upright signals can be generated and sensed. All of our I/O lines are buffered inbound and outbound for safety and reliability.



Powering up. The MSC 8001 will operate on a single +5 VDC power source in most system applications.

Going further. Our complete 16 page, full color tour guide to the MSC 8001 Single Board Computer is available by contacting Monolithic Systems Corp., 14 Inverness Drive East, Englewood, CO 80110. 303/770-7400. Telex: 45-4498

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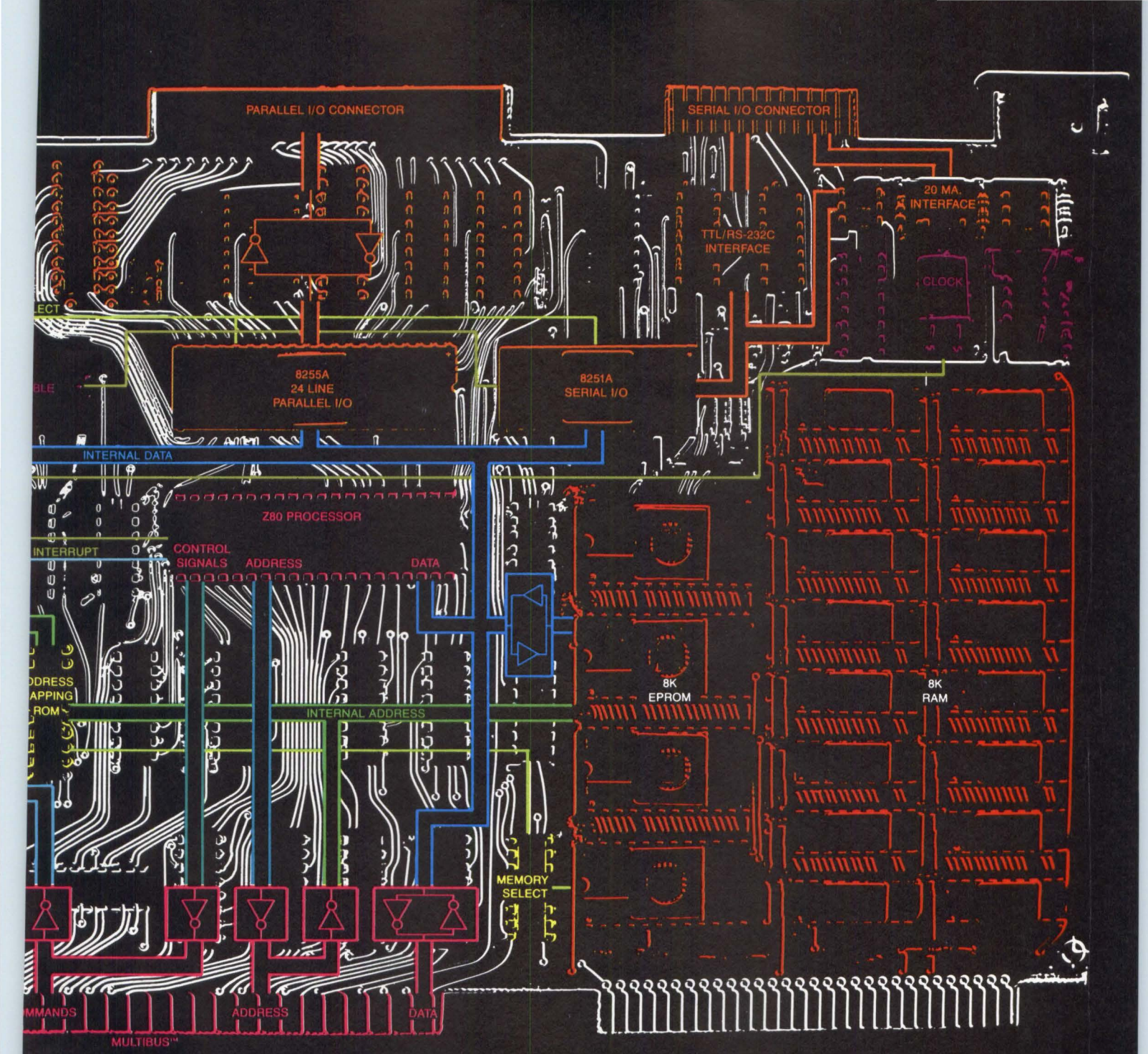

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CIRCLE 49 ON INQUIRY CARD

Bubble and CCD memory products are beginning to appear. This session presents overview of today's CCD and bubble memory status and discusses typical applications—from portable terminals to floppy disc and fixed-head disc replacements.

"Bubble and CCD Memory Status," J. Egil Juliussen and Dave Rosendahl, Texas Instruments

"Bubble Memories as a Floppy Disc Replacement," Richard Clewett, Data Systems Design Inc

"Charge-Coupled Memory Devices in IBM Compatible Peripherals," Tim Trueblood, Storage Technology Corp

"Application of Bubble Memories to Portable Terminals," J. Steven Flannigan, Texas Instruments

Session 10 **2-4:30 pm**

Machinery and Process Control Systems

Organizer/Chairman: George W. Zobrist, The University of Toledo

Presenting various industrial applications where the mini/microcomputer was successfully used as the controlling element, papers given reflect important industrial applications and the trend of using mini/microcomputers and microprocessors as the controller.

"Simulation for Digital Process Control Using CSMP," George Perdikaris, University of Wisconsin-Parkside

"Microprocessor Revitalizes Automatic Drill Press," Ron Becker, Sacramento State College

"A Table Driven Acquisition and Control System for Minicomputer Application," Gary C. Border, Digital Automation Associates

"Software Architecture of a RealTime Process Control Computer," George Perdikaris, University of Wisconsin-Parkside

Wednesday Morning

Session 13 **10 am-12:30 pm**

Designing with OEM Microcomputer Boards

Organizer/Chairman: Jerry Winfield, Mostek Corp

OEM microcomputer boards have become increasing popular over the past few years and are predicted to reach $68 million in sales in 1978. This session examines the advantages of using OEM microcomputers and how an engineer would go about designing an OEM microcomputer into his system. Types of development aids available and how they can be utilized to develop software and debug system hardware will also be covered.

"Evolution of Single Board Computers," Les Soltesz, Intel Corp

(Paper title to be announced), Bill Crawford, Motorola Inc

"The Engineering Design Application to Apply OEM Microcomputer Boards," Matt Biewer, Pro-Log Corp

(Paper title to be announced), Jim Vittera, Mostek Corp

Session 14 **10 am-12:30 pm**

Innovations in Microprocessor Software Development

Organizer/Chairman: Dennis J. Frailey, Texas Instruments

Focusing on innovative approaches to microprocessor software development, session discusses novel ways of supporting high level languages in a limited resource environment and new approaches to software development aimed at the naive user who doesn't want to learn programming.

"A Portable Cobol Compiler for Microprocessors," Keith Clark, Computer Analysts and Programmers Ltd

"Program Development for Ordered Processes," Richard A. Martin and Joseph H. Binkley, Indiana University

"The TI Microprocessor Pascal System," Larry Kroeker, George Ligler, Wendell Merritt, and Larry Spry, Texas Instruments

(Paper title to be announced), Dennis J. Frailey and R. Morrow, Texas Instruments

Session 16 **10 am-12:30 pm**

Speech Recognition Synthesis

Organizer/Chairman: George R. Doddington, Texas Instruments

Revolutions in computer technology are bringing us closer to speech communications with computers. State-of-the-art capabil-

The Big Business Language

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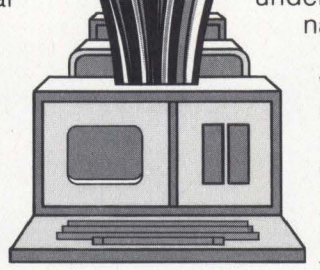

MicroCobol is more than a language . . . it's a total business data processing capability for mini and microprocessor users. It gives programmers structured programming capabilities and interactive symbolic debugging facilities. And much more . . . like complete screen formatting, and multiple-terminal utilization.

MicroCobol is completely PORTABLE, providing the ability to run programs on an expanding range of processors (8080/85, 6800, and Z80 architectures, DEC PDP-11 and IBM Series/1). And programs can be switched back and forth between different machines . . . . . WITHOUT REPROGRAMMING, OR EVEN RECOMPILING.

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MicroCobol is complete and ready for you. It's backed by the CAP-CPP Group's more than 16 years experience in computers and 2,000 man-years of COBOL experience. Call or write for more information.

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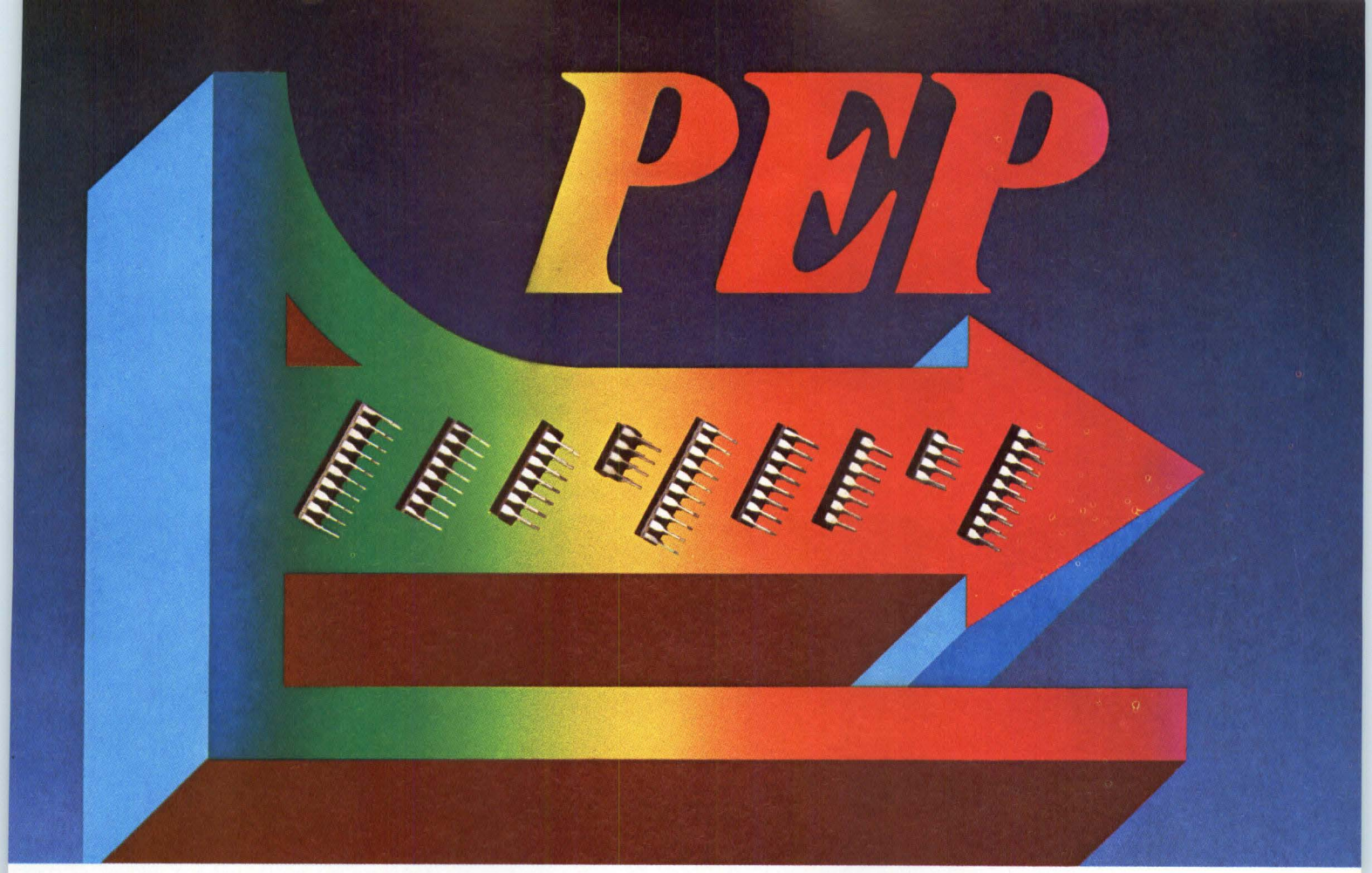

Beat the odds on early-life failures with PEP. And get the tightest AQL's in the industry. From the quality leader. Texas Instruments.

Lower your total system cost. Decrease field service. Decrease incoming test costs.

PEP, the Product Enhancement Program from Texas Instruments, provides off-the-shelf IC's with enhanced quality and higher reliability. With PEP you:

- Reduce or eliminate incoming IC inspection
- Improve yields through assembly
- Reduce field returns and service

PEP 3 and 4 provide 100% burn-in to accelerate the integrated circuit through early operational life, when IC failure rates are the highest, to the period where the failure rate typically reaches less than 0.0005% per 1000 hrs... a typical IC MTBF of 23 years for a system containing 1000 PEP ICs.

PEP processing is offered on Linear, Bipolar Memory and Bipolar Microprocessor, as well as all TTL families including Low Power Schottky (74LS), Schottky (74S), and Standard TTL (74)... in either plastic or ceramic DIP.

The new *PEP* now offers in all popular TTL families:

- 100% high temperature functional, continuity, and parametric testing
- Industry's tightest AQL (0.1% AQL cumulative for parametric, functional, and continuity)
- 2% burn-in PDA on PEP 3 (Plastic) and PEP 4 (Ceramic)

TEST	CONDITION	GUARANTEED AQL %					
		BIPOLAR LOGIC		BIPOLAR MEMORY		LINEAR	
		PEP 1, PEP 3	PEP 4	PEP 1, PEP 3	PEP 4	PEP 1, PEP 3	PEP 4
Continuity	100°C	0.015	0.015	0.015	0.015	0.015	0.015
Functional	0°C to 70°C	0.10	0.10	0.25	0.25	0.10	0.10
DC Parametric	0°C to 70°C			0.65	0.65	0.25 (Note 1)	0.25 (Note 1)
AC Parametric	25°C (Note 2)	0.65	0.65	1.00	1.00	1.00	1.00
Fine Leak	1 x 10^{-6} Leak Rate	NA	0.65	NA	0.65	NA	0.65
Gross Leak	Step C-1	NA	0.40	NA	0.40	NA	0.40
Mechanical Defects	Critical	0.10	0.10	0.10	0.10	0.10	0.10
(Note 3)	Major	1.00	1.00	1.00	1.00	1.00	1.00

Notes:
(1) For linear devices, a 0.25% AQL at 25°C and a 0.65% AQL at 70°C apply.
(2) Sampled and guaranteed.
(3) Critical mechanical defects are those which affect device functionally. Major defects include problems not affecting functionality.

For the complete story on updated PEP processing, and a copy of the new PEP brochure, contact your local TI field sales office or authorized TI distributor. Or, write Texas Instruments Incorporated, P.O. Box 225012, M/S 308, Dallas, Texas 75265.

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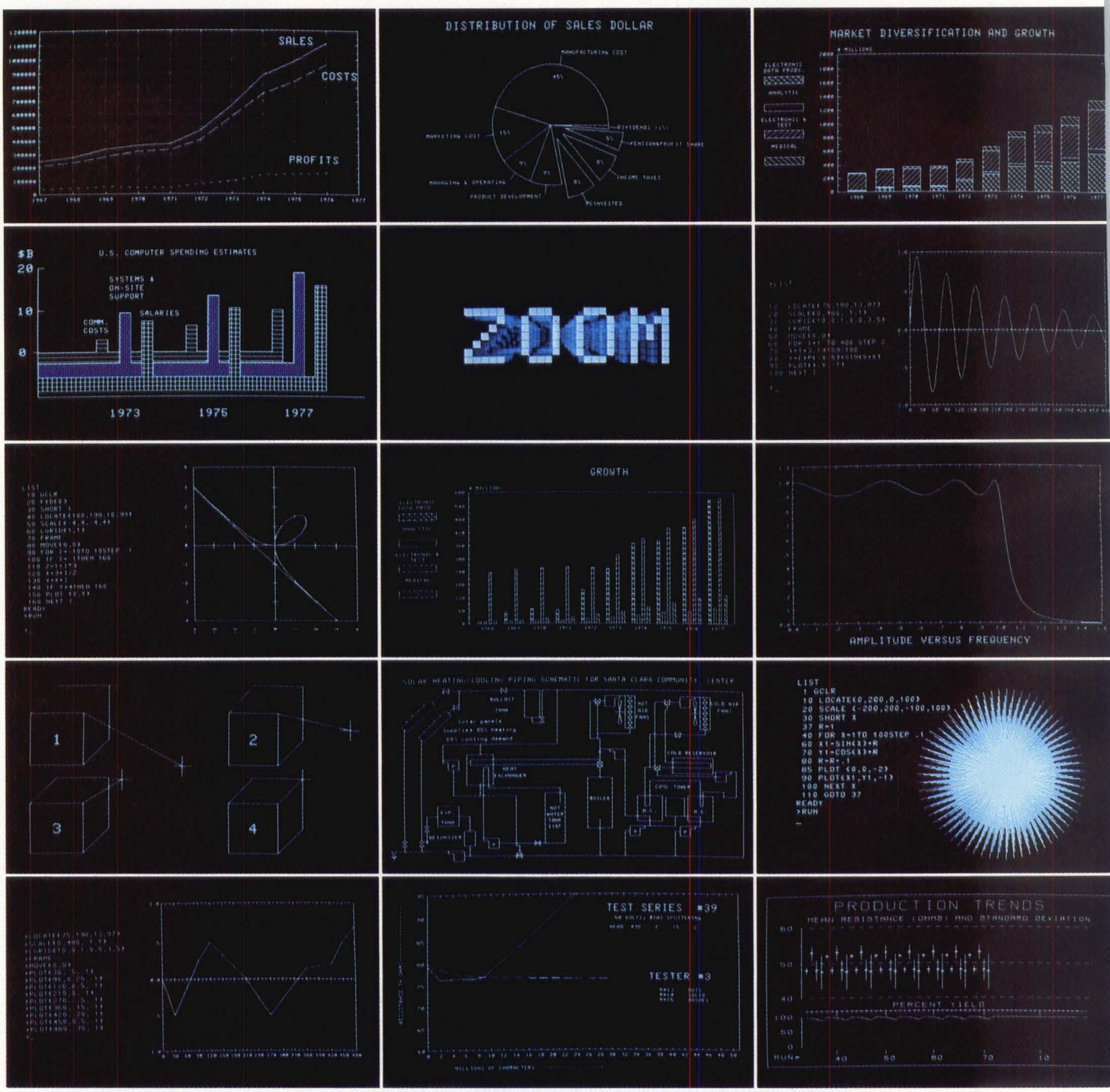
CIRCLE 51 ON INQUIRY CARD

Graphics. Without



graphics software.

You just lost your last excuse for sticking with alphanumerics. Because with HP's new 2647A Intelligent Graphics Terminal, you get graphics without digging into your CPU's software.

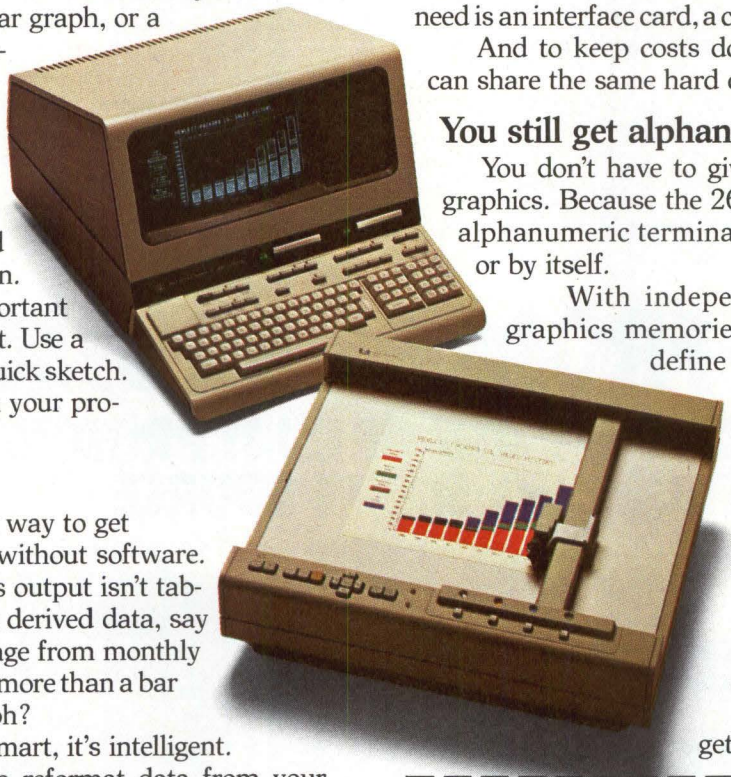
A picture's worth a thousand numbers.

On an alphanumeric terminal, your data's just a screen full of numbers. But with the 2647A you can plot tabular data as a bar graph, or a pie chart, or a linear or logarithmic line graph. Quickly, with just a few keystrokes.

Now you can really see your data, not just look at it.

What's more, with the 2647A you can zoom in and out. Pan right, left, up, down. Selectively erase. Shade important areas to make them stand out. Use a rubber-band line to make a quick sketch.

Without any help from your programming department.



It's more than smart.

The 2647A's the smart way to get graphics from tabular data without software.

But what if your CPU's output isn't tabular? Or if you'd like to plot derived data, say a three-month moving average from monthly sales figures? Or if you need more than a bar graph, pie chart or line graph?

The 2647A's not just smart, it's intelligent.

You can program it to reformat data from your CPU, or to compute more data, in easy-to-write BASIC. And you can program it in AGL, our high-level graphics language extension of BASIC. Its powerful commands, such as FRAME, AXES, LABEL, LOCATE and PLOT, put sophisticated graphics at your fingertips.

Either way, your program runs on the 2647A without any help from your CPU.

Hard copy's easy.

How do you get graphics into your briefcase?

The 2647A makes graphics as portable as alphanumerics. It interfaces easily with our 9872A Four-Color Plotter (which can even make overhead transparencies), and with our 7245A Thermal Plotter-Printer. All you need is an interface card, a cable and the peripheral itself.

And to keep costs down, more than one 2647A can share the same hard copy peripheral.

You still get alphanumerics.

You don't have to give up alphanumerics to get graphics. Because the 2647A's also a programmable alphanumeric terminal for interactive use on-line or by itself.

With independent alphanumeric and graphics memories. Eight soft keys you can define to do several steps with a single keystroke. A bright, easy-to-use, high resolution display. And built-in dual cartridge tape drives for 220K bytes of mass storage.

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CIRCLE 52 ON INQUIRY CARD

ities and limitations of speech synthesis technology are explored and future applications are forecast in this session. Tradeoffs among the basic parameters of data rate, quality, cost, and flexibility will be discussed.

"Speech Synthesis Technology Overview," Ron Schaefer, Georgia Tech

"Industrial Voice Response Systems," Mark Medress, Sperry Univac

"Low Cost Speech Synthesis," Richard Wiggings, Texas Instruments

"Phoneme-based Speech Synthesis," Richard T. Gagnon, R. T. Gagnon Associates

"Speech Synthesis from Text," Jonathan Allen, MIT

Session 17 **10 am-12:30 pm**

Telecommunication Networks

Organizer/Chairman: Roshan Lal Sharma, Rockwell International

This session deals with the design and analysis of telecommunications systems and networks employing digital switching and transmission techniques. Modeling techniques and analytical and simulation design aids will be emphasized.

"Design Considerations for a General-Purpose Switched Digital Network," R. Pederson, Arthur A. Collins Associates

"Queuing and Time-of-Day Routing in Multipoint Switched Voice Networks," James Jewett, Vanderbilt University

"Simulation of Voice Telecommunication Networks," A. Kumar and P. Lindsley III, Compucon Inc

"Design of Multicenter Telecommunication Networks," Paul De Sousa, Rockwell International

Wednesday Afternoon

Session 19 **2-4:30 pm**

Interfacing Microprocessors to the Outside World

Organizer/Chairman: Rob Walker, Intel Corp

As the cost of microprocessors and memory continues to decline, the interface between microprocessors and the outside world becomes increasingly important. Microprocessors with on-chip A-D converters, microprocessor peripherals, buses, and multiprocessing will be covered.

"Microcomputer with Onboard A-D Converter," Jeff Miller, Intel Corp

"Microprocessor Peripherals," Art Hamilton, National Semiconductor Corp

"Microcomputer Bus Structures," Carol Ogdin, Software Technique Inc

"Interconnective Microcomputers," Joe Barthmaier, Intel Corp

Session 20 **2-4:30 pm**

Microprocessor Software/Firmware Project Management—From Design to Field Maintenance

Organizer/Chairman: Bill Lowery, Tektronix, Inc

This session discusses and shares knowledge accumulated to date on problems and solutions encountered in microprocessor-based systems designs. Though still evolving, many new management techniques have already been formulated for dealing with the rather formidable obstacles that lie in the path of successful microprocessor software project completion.

(Paper title to be announced), Doug Bingham, Tektronix Inc

"Management Tools for Efficient Software Development," Michael Rooney, Boston System Office

"The Benefits of Software Engineering Methodology in Systems Software Project Management," Hugo Fray and/or John Fluke Jr, John Fluke Mfg Co

"Managing Hardware/Software Design," James Beetem, Hewlett-Packard, General Systems Div

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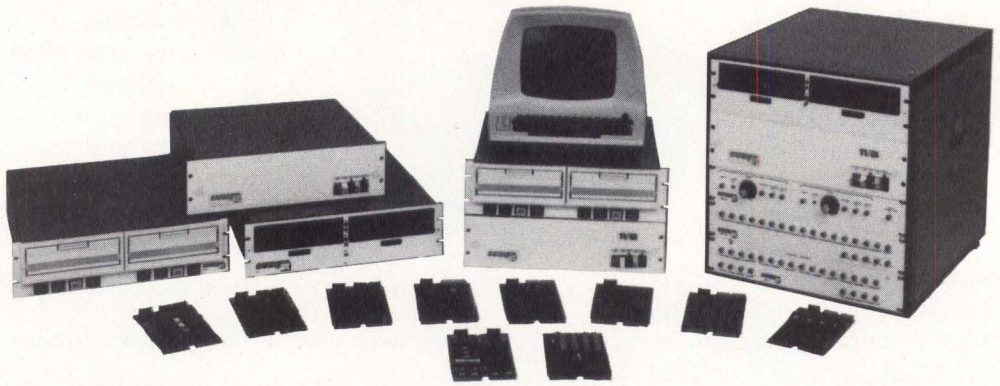

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CIRCLE 54 ON INQUIRY CARD

Motorola M6800

M6800 FAMILY DATA COMMUNICATIONS MICROCOMPONENTS NOW AVAILABLE

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MC6862	2400 bps MODULATOR
MC6850	ACIA (Async)
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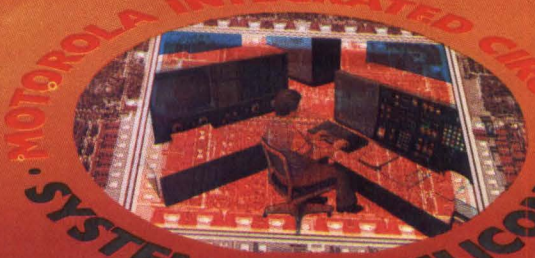

communicates...

Cost effective communications capability has been a primary M6800 consideration from the start.

When the M6800 Family's design concept was finalized, one of the features that raised it above the ordinary new microprocessors of the day, that made it unique, was its orientation toward data communications.

The MC6850 Asynchronous Communications Interface Adapter and the MC6852 Synchronous Serial Data Adapter were part of the original M6800 Family. A MODEM, the MC6860, was the first addition to the basic family. Later, the MC6862 2400 bps MODULATOR was added.

Data communications is now, more than ever, one of the special provinces of the M6800 Family. Powerful new family LSI functions keep expanding its capabilities. Functions like the Advanced Data Link Controller, MC6854, which is available now, and the MC6851 Universal Communications Interface Adapter scheduled for availability in the first half of 1979.

Advanced Data Link Controller implements all major bit-oriented protocols - on chip.

The MC6854 ADLC is Motorola's new 28-pin MPU/data communications link dedicated to doing its bit-sync job better than any 40-pin general purpose device can, and doing it less expensively.

It's available off-the-shelf now for $16.95 (plastic) in 100-up quantities. Because the MC6854 maximizes effectiveness of its specific function, software overhead and associated costs are minimized.

In addition to SDLC, the bit-oriented protocol implemented by most devices, the MC6854 also handles ADCCP and HDLC on chip, without any sacrifice of its complete MODEM controls (RTS, DCD, CTS, DTR), DMA capability, or loopback self-test. The ADLC implements NRZ and NRZI, and also provides complete on-chip loop control. Quad buffers, instead of the usual pair, allow two-byte transfers.

Three speed variations, 1 MHz, 1.5 MHz, and 2.0 MHz, are now available, and the 1.0 MHz MC6854 is offered in your choice of 0 to +70, −40 to +85, or −55 to +125 degrees C.

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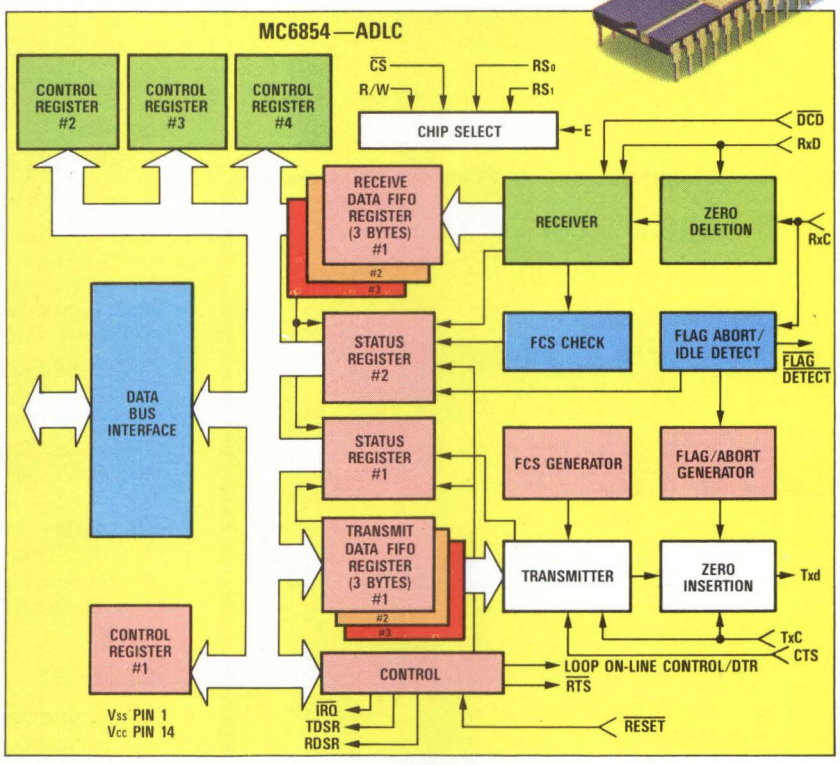

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CIRCLE 55 ON INQUIRY CARD

Session 23 2-4:30 pm

Electronic/Digital Telephone Switching

Organizer/Chairman: Narindra N. Lakhanpal, Rockwell/Collins

Applications oriented session presents both problems and opportunities that are emerging as the interest in electronic switching continues to grow in the marketplace.

"Application of Microcomputers to Telecommunications," J. Gordon Pearce, Stromberg Carlson

"Network Synthesis of Tactical Military Switching System," Yau-Wu Tang, The Mitre Corp

"Control Parameters for Switching Systems," W. V. Tyrlick, Martin Marietta Corp

"Digital Voice Conferencing," D. C. Nicholas, Rockwell/Collins

"Concerns Regarding Digital Evolution," Phillip B. Harris, Bell Northern Research Inc

Thursday Morning

Session 25 10 am-12:30 pm

Testing New Generation LSI Devices

Organizer/Chairman: Dave Huffman, Mostek Corp

High density, high performance MOS/LSI memories now appearing on the market are aimed at a very cost-sensitive portion of the applications spectrum, while others are aimed at high performance applications. These memories present unique test problems to the semiconductor manufacturer, test equipment manufacturer, and the user.

"Design and Testing of New Generation LSI Memories," Dennis Segers, Mostek Corp

(Paper title to be announced), Garry Gillette, Teradyne

(Paper title and speaker to be announced)

Panelist: Norm Hartdegen, Mostek Corp

Session 26 10 am-12:30 pm

Computer Applications in Medicine

Organizer/Chairman: A. R. Potvin, University of Texas

Micro- and minicomputer technology is finding widespread application in the medical environment. In this session, medical researchers review current applications in neurology, neurosurgery, radiology, psychiatry, and internal medicine.

"Radionuclide Cardiology Using Dedicated Minicomputers," Ernest M. Stokely, Southwestern Medical School

"Use of Microprocessors for Medical Monitoring in Sleep Research," Stephen A. Underwood, University of Texas at Arlington

"Automation of a Comprehensive Neurofunction Laboratory," A. R. Potvin, University of Texas at Arlington

"An Overview of Computerized Tomography," El Olson, E.M.I. Medical Inc

Session 29 10 am-12:30 pm

LSI Technology in Telecommunications Systems

Organizer/Chairman: Joe Jarrett, Mostek Corp

Exploring the increasing use of LSI in telecommunications systems from both a technology and applications viewpoint, session presents solution to several unique problems inherent in these systems. Both custom and standard product LSI in several different process technologies will be investigated.

"Application of LSI in Stored Program Telecommunications System," John Tinney, Danray Inc

"CMOS Technology for Single-Chip Implementation of a Per-Line Codec," Kul Ohri, Mostek Corp

"LSI DTMF Receivers," Mod Hammad, Mitel Inc

"LSI Channel Bank Applications," Toney Warren, Collins Radio Group, Rockwell International

Thursday Afternoon

Session 31 2-4:30 pm

Debugging Microprocessors in Real Time

Organizer/Chairman: Erin Greene, Tektronix, Inc

How do you debug microprocessor devices you can't stop or interfere with? Each member of the session panel will expound on the realtime issue, including realtime tracing, how the realtime instrument is made, how it works, and what it offers over and above slow traces.

"General-Purpose Logic Analyzer and Accessories Solve Microprocessor Problems in both Hardware and Software," Ed Jacklitch, Biomation Division, Gould Inc

"The Logic Analyzer: A Key Element in the Design, Production and Service of Digital Systems," John Marshall, Hewlett-Packard Co

"Debugging Realtime Systems Requires Powerful Tools," Bob Francis, Tektronix Inc

"Complexities of Capturing and Analyzing Logic Data in a Realtime Environment," Barry Price and Bruce Barlow, Texas Instruments

Session 32 2-4:30 pm

Microprocessors Improve Test Instrument Performance

Organizer/Chairman: Frank J. Burge, Regis McKenna, Inc

Microprocessor based instruments are now providing test capabilities not previously available. This session describes some of these instruments and their applications, and also addresses the need for software standardization.

"Instrument Standardization," John Fluke, Jr, John Fluke Manufacturing Co

(Paper title to be announced), Dick Kinnard, Tektronix, Inc

"Hewlett-Packard's Synthesizer/Function Generator," Doug Garde, Hewlett-Packard Co

"Production Test of Digital Products," Roy Tottingham, Gould Inc/Biomation Div □

CIRCLE 56 ON INQUIRY CARD

CIRCLE 57 ON INQUIRY CARD→

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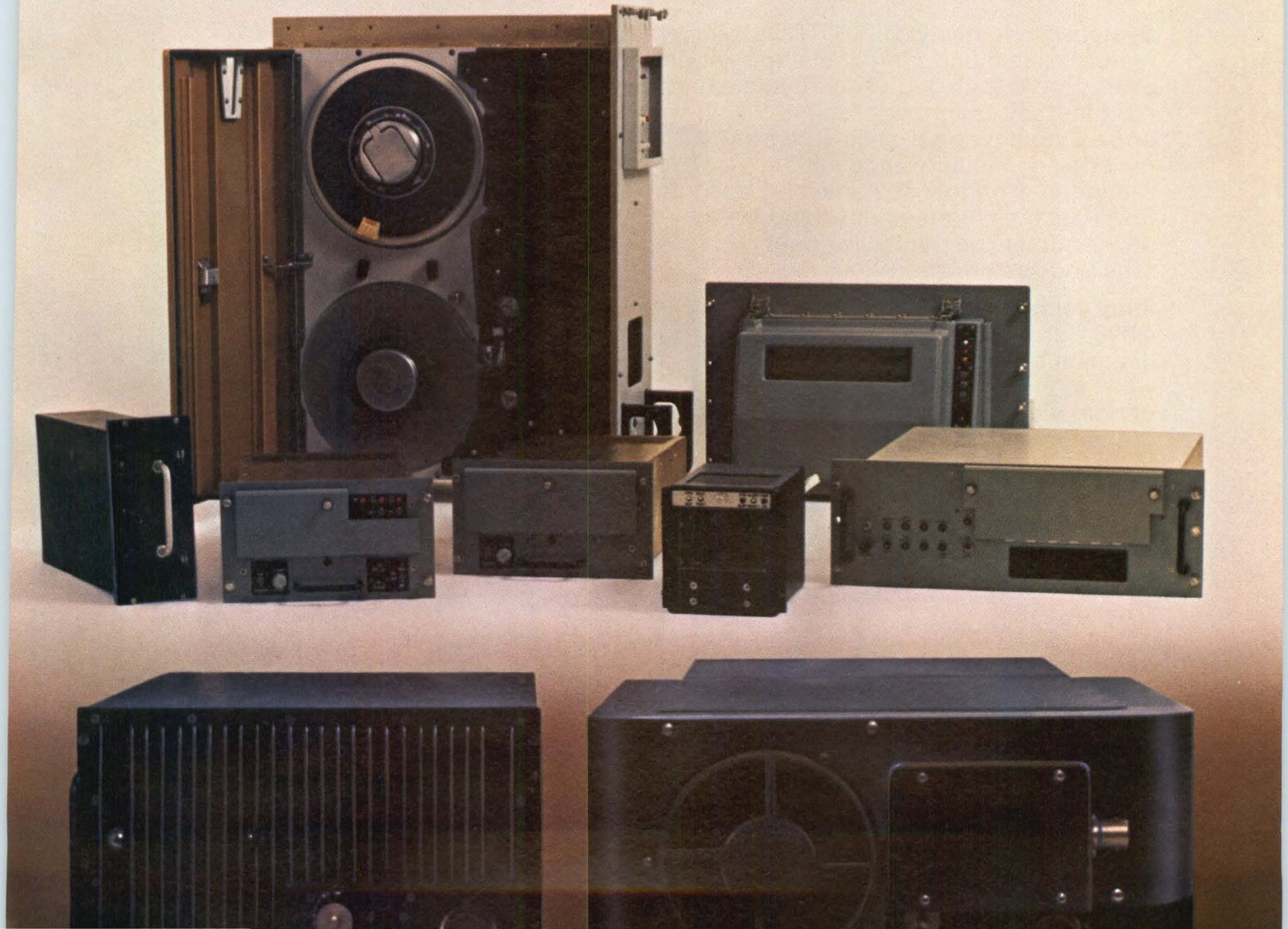
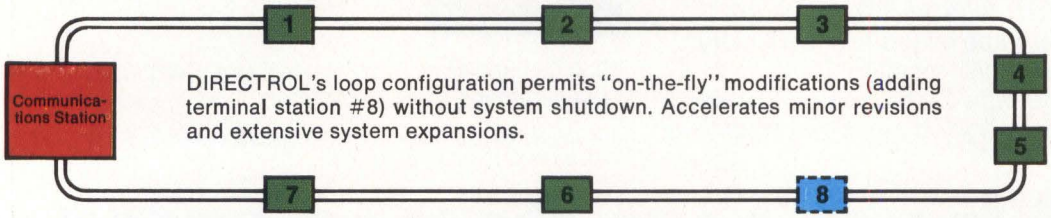
ROLM backs up its processors with Mil-Spec peripherals



New DIRECTROL™ Multiplexer. Signaling new directions for industrial control.

Cutler-Hammer's new DIRECTROL . . . finally, here's a multiplexer that's practical for industrial control application. DIRECTROL achieves startling advantages in project simplification, system productivity and plant versatility.



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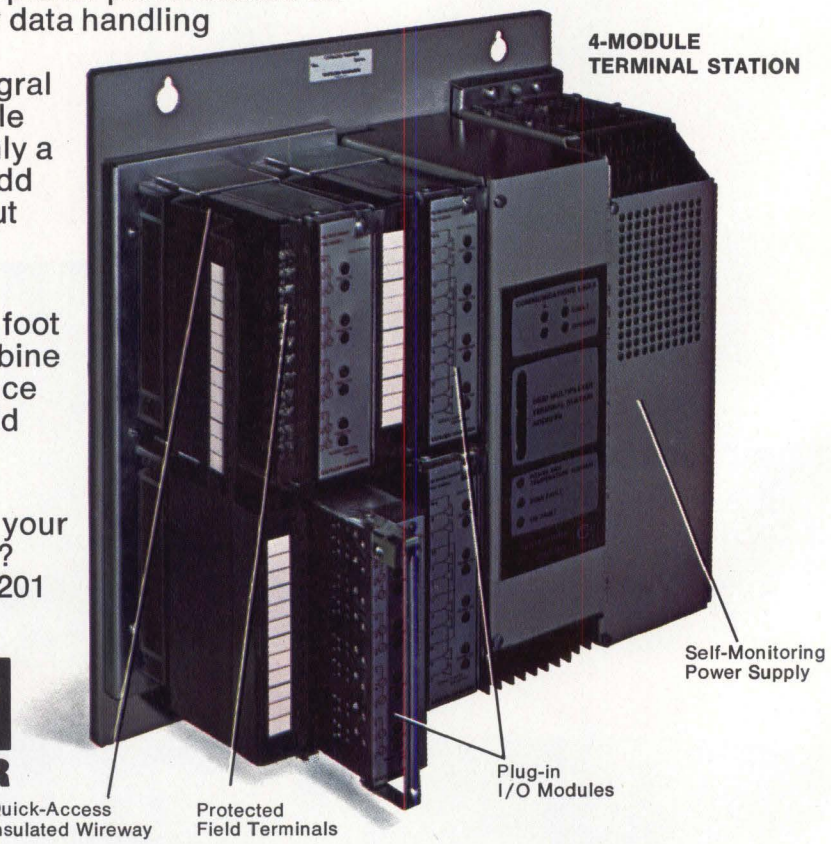

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CIRCLE 58 ON INQUIRY CARD

BREAKPOINT DESIGN FOR DEBUGGING MICROPROCESSOR SOFTWARE

Software techniques for implementing breakpoints to assist in microprocessor program checkout within the framework of a debug monitor demonstrate the attributes and limitations of interrupting program operation to allow designers to examine and modify data or code before returning to program execution

T. P. Hughes Consultant, South Orange, New Jersey
D. H. Sawin III Foxboro Company, Foxboro, Massachusetts

A useful method for controlling the execution of code under test is a software "breakpoint," a specific point in a program that requests interruption to grant the designer the opportunity to check, correct, or modify the program before continuing execution. A breakpoint returns control of the system to the debug monitor when a specified program location is addressed on an instruction fetch cycle of the central processing unit. With the debug monitor in control, the designer can check that the program has produced the expected results by displaying data stored in memory or central processing unit registers, or by obtaining the desired sequence at an input/output port (eg, a character output to a cathode-ray tube or printer terminal).

Breakpoint capability may be implemented by front panel controls, by other specially-designed hardware, or by software alone; the latter is commonly done with teleprinter or cathode-ray tube (CRT) based monitors, where no front panel or additional hardware is utilized. Frequently, the documentation supplied with available monitors is incomplete with respect to the exact design of the breakpoint, especially its interaction with the rest of the monitor and the designer's application program.

Debug Monitor Operation

To fully comprehend the significance of breakpoints it is helpful to summarize the operation of a debug monitor, since both are intimately interwoven. As a standard software item utilized in the development of microprocessor systems, a debug monitor permits the designer to search out and correct errors in software routines. The debug monitor itself is an interactive software program that resides mostly in programmable read-only memory (P/ROM) but also requires a small amount of random-access memory (RAM), or other read/write (R/W) memory, to operate. Capability and ease of use of a monitor are related directly to its memory size. A primitive monitor might occupy 256 bytes of P/ROM and provide rudimentary debugging capabilities; larger versions occupy 1k to 3k bytes and provide powerful debugging tools. A monitor

should at least provide for loading memory with an application program to test, for displaying and modifying the contents of memory and central processing unit (CPU) registers, and for executing and testing programs in a controlled manner.

When a new application program is debugged, the monitor and application program share the same processor in an orderly manner, but they occupy separate areas of memory space. The design of a debug monitor involves trading off two directly opposing objectives. First, the monitor should maintain some control to reliably assist in checking out the application program. Second, the application program should run in as natural a state as possible, in complete control of system resources, as if the monitor were not present. An acceptable monitor design achieves a balance between these objectives.

If special hardware is not used, the monitor must start at location 0 in 8080A memory space, since this is where the processor begins execution at power-up/reset. (While the breakpoint principles discussed apply to the 8080A microprocessor, they can be extended to other microprocessors of various architectures.) Fig 1 illustrates the two segments of memory space that monitors use. One segment is read-only memory (ROM) containing the actual monitor program, and the second is R/W memory containing the monitor's data base and stack.

Application program workspace is most often all R/W memory during debugging phases, even though most application programs will finally have separate program and data segments, just as the monitor does. The designer loads new or untested programs into the application program workspace, either directly in machine language using a display/alter memory command or indirectly through an auxiliary storage medium such as paper tape. The tape contains a machine language program that has been produced by an assembler or compiler and is in a format compatible with a load paper tape routine invoked with a monitor command.

Many microprocessors, the 8080A included, utilize special memory locations which are forced by the hardware to begin execution in response to an external interrupt. These special locations are called interrupt traps (see Fig 2). Contained in the monitor program segment, these locations are programmed with jumps to the lowest locations in the application program workspace to facilitate and standardize the debugging of realtime programs. An execution time penalty of one jump instruction is associated with this procedure. This delay of one instruction time normally is not important to application program performance. For example, in Fig 2, the three locations 0008_{16} to $000A_{16}$ are programmed with a jump to 2008_{16}, thus indirectly vectoring the interrupt for trap 0008_{16} into the application program workspace. Similar jumps are programmed for other interrupt locations, while a power-up/reset vectors the processor into the monitor. This use of the reset trap can be avoided by special purpose hardware, which allows the application program to use it after some initialization. Experience has shown that the reset trap is almost never used in a system for runtime interrupt handling; thus, this theoretical shortcoming is rarely a practical problem.

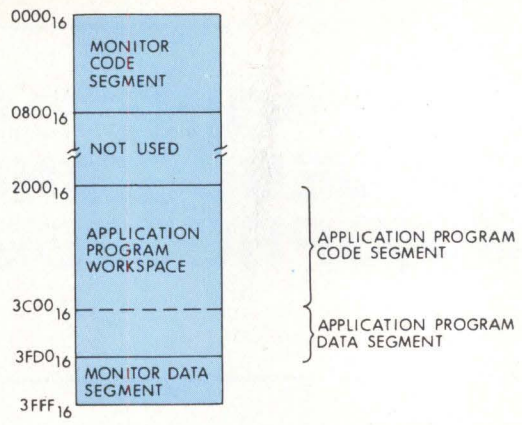

Fig 1 Memory map for debug monitor and application program. Monitor consists of two memory segments, one in P/ROM containing monitor program, and second much smaller segment in RAM containing monitor variable tables and monitor stack area. Remaining memory space is available for application program. In this example, fixed 8k-byte block of RAM is used (2000 to $3FFF_{16}$), almost all of which is available as workspace. Last 48 bytes (3FD0 to $3FFF_{16}$) are reserved for monitor data segment. Application program being debugged consists of 7k bytes of code (2000 to $3BFF_{16}$) and slightly less than 1k bytes of R/W memory (3C00 to $3FCF_{16}$)

Assume that the system being designed can accommodate the monitor and monitor input/output (I/O) port, which usually is a simple serial interface to a terminal device. The terminal device then replaces the traditional computer front panel. When the application software (running in the application workspace R/W memory) is completely debugged under monitor control, the monitor portion is removed from the system by eliminating the monitor P/ROMs; it is

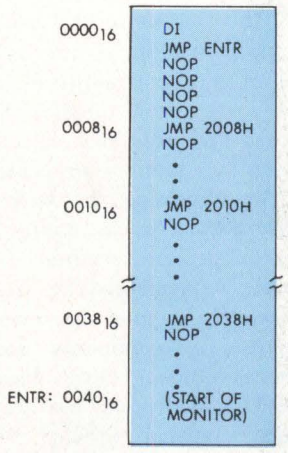

Fig 2 8080A interrupt trap locations. These locations are in lowest part of monitor code segment. Restart trap actuated at power-up/reset vectors control into monitor. Remaining interrupt traps vector control into lowest part of application program workspace; however, monitors often reserve one trap location for breakpoint processing, in which case jump is to monitor breakpoint processing routine located in monitor code segment

replaced by the application software, which has been relocated in memory to location 0000_{16} and is now in ROM. Fig 3 illustrates the new memory map with the monitor removed. Interrupt traps are now properly located in the memory image, and the level of indirection (Fig 2) caused by the interjection of the monitor into the system is removed. When power is applied now, the relocated application software (often referred to as operational firmware) receives control and hopefully runs the system correctly. If not, the designer can retreat to the monitor configuration and attempt to resolve the problem.

When power is applied to the system with the monitor present, a start-up message is normally delivered to the command terminal followed by a prompt character (typically a question mark or period). The command terminal is ready to accept a command. A monitor command usually consists of a single letter, which identifies the command type, followed by any command operands. The entire line of input is usually ended with a carriage return. Basic operating sequence of the monitor is shown in Fig 4. Type 1 commands consist of utility functions, such as display/alter memory and load paper tape, and do not involve execution of the application program. Type 2 commands involve execution of the application program; return from their operation to the monitor may be via a reset or breakpoint.

The monitor's command processing state is its active state. Commands are processed one at a time as they are entered by the designer. Since a monitor usually operates with all interrupts disabled, it is completely in charge of the system. This may not be the case if direct memory access (DMA) transfers are possible, but this complication is beyond the scope of the article. Interrupts are enabled before the monitor passes control of the processor to the application program. This allows realtime programs to operate properly.

When the designer enters an execute command, the monitor enters its passive state and restores the CPU registers to their application program values, enables interrupts, and jumps to the specified start address. Fig 5 illustrates the monitor's data base, showing the tables in which it stores the application program information. Once the application program has control of the system, the monitor remains in its passive state until a breakpoint is encountered or until the system is reset.

While the application program is running, the monitor's data tables are vulnerable to bugs in this program. However, if the monitor is designed defensively, only a few bytes of the monitor tables are critically

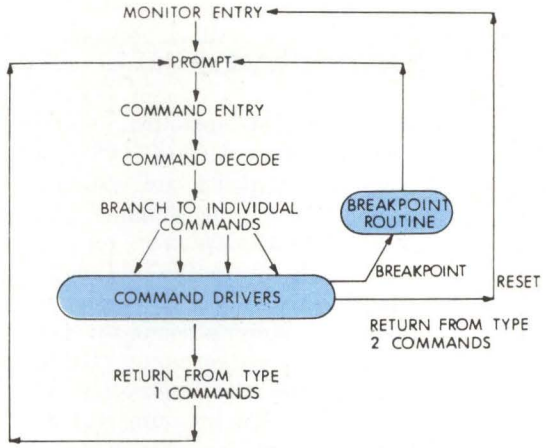

Fig 4 Monitor operation. Upon start-up, prompt is issued to designer, signifying that system is ready for command entry. Command is entered by designer and subsequently decoded by monitor. Once command-directed monitor action has been completed, monitor issues another prompt character and process starts anew

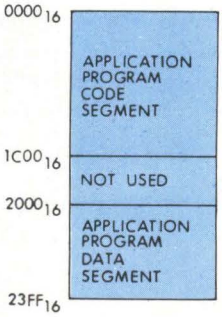

Fig 3 Memory map with debug monitor removed and operational firmware in control. Operational firmware receives complete system control on power-up/reset. This application program, which occupied locations 2000 to $3BFF_{16}$ during debugging, has been reassembled with origin of 0, and resultant code placed in P/ROM. Code segment now occupies memory space 0 to $1BFF_{16}$. Application program data segment has also been relocated in reassembly and now occupies locations 2000 to $23FF_{16}$

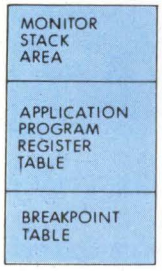

Fig 5 Monitor data segment. Monitor R/W memory is usually divided into three divisions shown: first for monitor stack when monitor is active, second for storing application program CPU register contents when monitor is activated through breakpoint, and third for breakpoint information

important. The monitor code itself is programmed into P/ROM and cannot be overwritten by an application program.

As an example of monitor operation, consider the display/alter register command that most monitors possess. Present register contents are stored in the monitor register table. When the designer changes a register value with the display/alter register command, the monitor simply overwrites old data in the table with new data. Later, when the designer enters an execute command, the monitor loads the CPU registers with the values stored in the monitor table before executing (ie, jumping to) the application program. Similarly, when the application program returns to the monitor via a breakpoint, the monitor stores the CPU registers into the RAM table before it uses them. Thus, the monitor maintains the application program state of the CPU by saving and restoring all registers on every entry to and exit from the monitor, respectively.

Where the Breakpoint Fits In

Breakpoints are incorporated in a debug monitor to return control of the system to the breakpoint routine, which can then "freeze" the state of the application program by disabling interrupts and saving the contents of the CPU registers. It should save the registers as reliably as possible, even if the application program has gone awry. Similarly, the mechanism by which the software breakpoint is implemented should have only minimal impact on application program capabilities.

Monitors generally use one of eight 8080A restart instructions (RST 0 to RST 7) to implement the software breakpoint. The RST N instruction is a 1-byte subroutine CALL to location 8*N and results in a CALL to one of the interrupt trap locations (0_{16}, 8_{16}, 10_{16}, . . . 30_{16}, 38_{16}). For example, the Intellec® 8 MOD 80 monitor uses RST 1, while the Intel MDS monitor uses RST 0. Since the RST N instruction is reserved for monitor use, the designer cannot debug a realtime program that uses interrupt level N.

When the designer requests a breakpoint to be set, the breakpoint routine in the monitor saves the present content of the breakpoint location in the breakpoint buffer (one byte), along with the address of the location (two bytes). Then, the restart instruction is stored by overwriting the breakpoint location. When this location is executed, an effective 1-byte CALL to the breakpoint routine in the monitor occurs, and the breakpoint routine receives control. If the breakpoint location is not executed, the designer must toggle the 8080A RESET line to obtain control. On reset, most monitors (including the two Intel monitors) do not restore any breakpoints that have been set because they initialize the monitor breakpoint table in RAM just as they do on power-up. Thus, the designer is left with one or more RST N instructions in the program and must restore these locations with the display/alter memory command before continuing, unless of course the program is reloaded.

Breakpoints may also be implemented with CALL or JMP instructions. However, since these 8080A instructions are three bytes long, difficulties are introduced that do not occur with 1-byte restart instructions. For example, if a designer requests a breakpoint at location J, the monitor sets it by writing the 3-byte instruction (either CALL or JMP) into locations J, J+1, and J+2. Under these conditions, any reference to location J+1 or J+2 will not produce the expected results and may, in fact, introduce errors into the application program, as illustrated in the following 8080A code. If the designer should execute a CALL to SUB1 (Subroutine 1) before the breakpoint at J is encountered, incorrect code will be executed (the instructions shown in SUB1 have no particular meaning other than to illustrate this point).

```
                    .
                    .
                    .
J                   RET
J+1       SUB1:     INX  H
J+2                 INR  A
                    .
                    .
                    .
                    RET
```

Consequently, restart instructions are almost always used to implement software breakpoints for the 8080A.

Regardless of the breakpoint instruction chosen, two limitations are inherent in the software breakpoint approach. First, breakpoints may be set only in R/W memory. An attempt to set a breakpoint in P/ROM will be unsuccessful. No harm will come of the attempt, however, either when the breakpoint is set or cleared, except that the designer will be wasting the capability. A hardware implementation uses the address lines of the CPU, which are compared to a breakpoint register set by the designer (eg, through front panel switches). When a match occurs during an opcode fetch cycle of the CPU, the breakpoint is activated. The type of memory at the breakpoint address is irrelevant.

The second software limitation is that breakpoints must be set at the first byte of an instruction. Setting a breakpoint at the second or third byte of a multibyte instruction not only will cause the breakpoint to be missed, but also will probably cause erroneous code to be executed. This can be a significant problem with variable-length instruction processors, such as the 8080A.

This latter limitation also applies to the hardware breakpoint. However, memory is not overwritten in

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the hardware implementation, so there is no possibility of executing incorrect code. The worst that can happen is that the breakpoint condition will not occur.

Breakpoint Implementation Using RST 0

Based upon the previous background information, the design approach chosen implements the breakpoint with the RST 0 instruction of the 8080A. This technique gives the designer almost full use of the interrupt capability of the 8080A, as the remaining seven restart instructions (RST 1 to RST 7) may be used by the application program for hardware generated interrupts. Experience reveals that most 8080A systems only use the level 0 interrupt for system initialization; therefore, application program capabilities are only minimally affected by this decision.

The designer supplies the breakpoint address as an optional operand in the monitor execute command. The allowed forms of this command are described below, where G designates the execute command, X and Y represent hexadecimal memory addresses, and <CR> represents a carriage return, signaling the end of the command string to the monitor. Square brackets delimit the optional breakpoint part of the command string; they are not entered by the designer.

GX [,Y] <CR>	Execute program starting at location X [with an optional breakpoint set at location Y]
G [,Y] <CR>	Execute program starting at current program counter [with an optional breakpoint set at location Y]

The syntax of this command is similar to the GO command in the Intellec 8 MOD 80 monitor.

The G command jumps to the designer program with all interrupts enabled. It is convenient to use a second command P (perform designer program) whose syntax and operation are identical to the G command except that the monitor jumps to the designer program with all interrupts disabled. Ideally, the monitor should also be able to jump to the designer program with the interrupt enable flip-flop set to the same state as it was on the last entry to the monitor. This is impossible with the 8080A (unless external logic is used), as there is no instruction to read the interrupt enable flip-flop in the CPU. This capability has been incorporated into the 8085 processor with the introduction of the read interrupt mask instruction (RIM).

The optional breakpoint at Y remains set until the monitor becomes active again (ie, until the breakpoint is executed or until the RESET line is toggled). Then, after disabling interrupts and saving registers, the monitor restores the original contents of the breakpoint location. Because the breakpoint is in effect only when the application program is running, it is referred to as a "runtime" breakpoint.

Permanent breakpoints have also been implemented, and they are set and cleared by additional monitor commands. Their advantages over runtime breakpoints are that the designer only has to set them once and they remain in effect until cleared. This avoids entering a breakpoint address each time a G or P command is given. However, permanent breakpoints do introduce reliability problems that do not occur with runtime breakpoints. Problems arise when the monitor is active, and the designer inadvertently overwrites the permanent breakpoints by performing other monitor commands, such as load paper tape or display/alter memory. The chosen design, and most permanent breakpoint designs, make no attempt to protect these locations, depending instead on the skill of the designer. Protecting them against all monitor commands that write into memory would necessitate substantial software overhead. No immediate problem arises if a breakpoint is overwritten, except possibly that no breakpoint will occur. However, when the designer later clears the overwritten breakpoint, errors are probable because the monitor will restore the breakpoint location to the value the monitor had originally saved in the monitor RAM table.

Protection against this situation may be built into the clear breakpoint monitor routine. If the monitor clears a breakpoint and finds that the breakpoint location no longer contains an RST 0 instruction, then it does not restore the location to its original value. In addition, the monitor outputs a special character ('*') to the command terminal to inform the designer.

The chosen design provides one runtime breakpoint and three permanent breakpoints. Both Intel monitors provide for two runtime breakpoints, whereas some other monitor designs provide for a single permanent breakpoint. As already mentioned, the main advantage of the permanent breakpoints is that they do not need to be entered each time a G or P command is given. The main advantage of runtime breakpoints is that they allow the designer to continue execution from the point at which a runtime breakpoint occurs; entering a G or P command without a start address after a runtime breakpoint is encountered acts as a continue command. It is not possible to continue execution when a permanent breakpoint is encountered without first clearing it with the clear breakpoint command. If it is not cleared, the continue command will cause the restart instruction to be executed again, and control will pass back immediately to the monitor breakpoint routine.

Format of the breakpoint table in monitor RAM is shown in Fig 6. The first three bytes are reserved for the single runtime breakpoint and the remaining nine bytes for the three permanent breakpoints. Conventionally, a breakpoint address of 0 indicates that no breakpoint is set; thus, the monitor does not accept such an address. This is not a limitation because location 0 is in monitor P/ROM, where a breakpoint will not work anyway.

When the designer enters a permanent breakpoint command consisting of the letter B followed by one

to three addresses, the addresses are stored as they are entered into the first available permanent breakpoint entry, and the byte at the breakpoint address is stored in the third byte of the entry. If three permanent breakpoints are already set, no further permanent ones can be accommodated, and an attempt to set a fourth results in termination of the command with the error character ('?') output to the command terminal.

To ensure proper restoration of the permanent locations, more than one permanent breakpoint cannot be allowed at the same location. Otherwise, by certain sequences of setting and clearing permanent breakpoints, it is possible to restore a breakpoint location incorrectly. The monitor will not accept a permanent breakpoint request if the address already appears in the breakpoint table.

Breakpoint Processing

A software flowchart (Fig 7) shows monitor processing on power-up, reset, or when a breakpoint is encountered. When the system is powered up, no start-up message is output since the monitor cannot distinguish a power-up entry from a reset or breakpoint entry. The reset or breakpoint message is output to the command terminal, but both are meaningless since the designer has not loaded memory with a program to test.

Since memory presumably powers up in a random pattern, the three addresses in the permanent breakpoint table contain random addresses. The designer should zero the permanent breakpoint addresses before loading a program; this avoids the possibility of overwriting the program by clearing the permanent breakpoints at a later time. This can be done by entering the single command C<CR>, which clears all permanent breakpoints. The table can also be zeroed using the display/alter memory command or a fill memory command, provided the designer knows its location. It is not necessary to clear the runtime breakpoint since this is always done automatically by the monitor.

Requiring the designer to clear permanent breakpoints at power-up is inconvenient and a possible source of error. This is compensated for by the usefulness of the permanent breakpoints and their transparency to future resets, which require the designer to manually restore any existing breakpoints in other monitors.

Note in Fig 7 that if the runtime breakpoint location no longer contains an RST 0 instruction, a special character '*' is output and the breakpoint location is not restored. Thus, if the designer has overwritten the breakpoint address in the monitor table, the monitor is prevented from inserting the saved byte into an incorrect address. The other error possibility is that the designer has overwritten the restart instruction in the program. In either case, the designer is informed of a problem by the appearance of the special character. The end result is that the monitor is less likely to compound errors if the application program has bugs. A similar situation can arise when the designer clears a permanent breakpoint with the C command. A similar check is made, and the special character is again output to indicate an error condition.

The four bytes containing the saved contents of the breakpoint locations are also vulnerable. The monitor provides virtually no protection if these locations are overwritten by the application program. Assuming the breakpoint address is not destroyed and the breakpoint

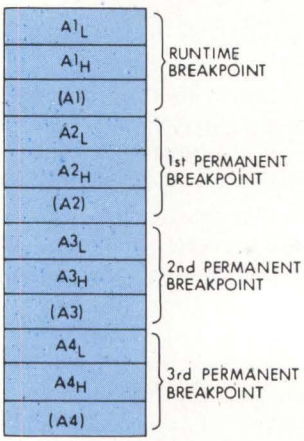

Fig 6 Monitor breakpoint table. Table consists of three bytes for each possible breakpoint. First three bytes are reserved for single runtime breakpoint. Remaining nine bytes are for three permanent breakpoints. First two bytes of each entry contain address of breakpoint. Third byte contains normal content of breakpoint location, which is saved before RST 0 instruction is stored. Address of 0 indicates that no breakpoint is set in this entry; monitor does not permit designer to set breakpoint at location 0

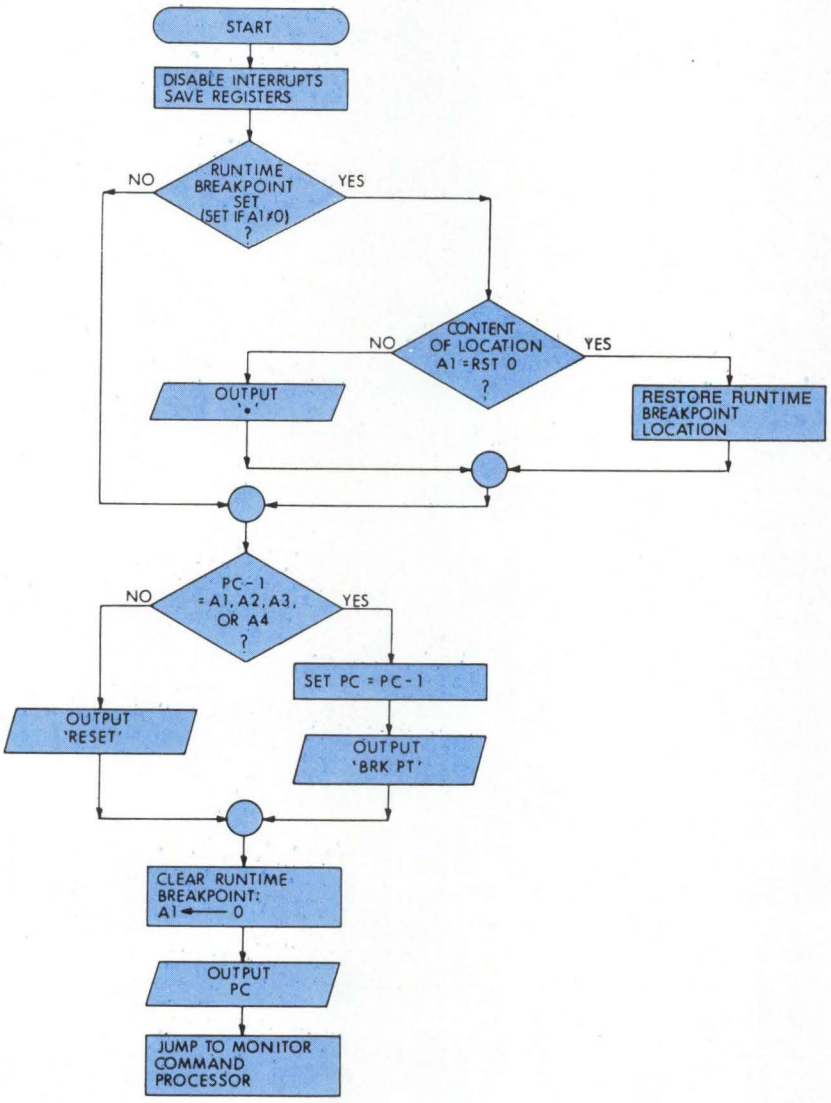

Fig 7 Monitor software flowchart. Monitor processing begins on power-up, reset, or when breakpoint location (A1 through A4) is executed. Monitor assumes that designer executed breakpoint location or toggled RESET line

location still contains an RST 0 instruction, the monitor will obediently insert the incorrect byte into the application program when any breakpoint occurs or when the system is reset in the case of the runtime breakpoint, or when a breakpoint is cleared with the C command in the case of permanent breakpoints.

In Fig 7, the basic assumption of the breakpoint processing routine is that the application program has just executed a breakpoint location or that the designer has manually reset the system. If the program executes a breakpoint location containing an RST 0 instruction, the processor pushes the address of the next instruction onto the application program stack and effectively jumps to location 0. The stack is a block of R/W memory set aside by the application program for temporary last in, first out storage of data and for subroutine linkage. The current location in the stack is determined by the content of a 16-bit CPU register—the stack pointer (SP)—which can be loaded and modified by several 8080A instructions.

The breakpoint processing routine outlined in Fig 7 receives control and eventually pops the program

Program Listing of 8080A Code To Save Application Program Registers

```
        ORG     0
        DI                      ;"FREEZE" SYSTEM
        JMP     ENTR            ;J OVER INTERRUPT VECTOR TABLE
         (INTERRUPT VECTORS TO WORKSPACE GO HERE)
        ORG     40H             ;START CODE AFTER LAST TRAP
ENTR:
        SHLD    APHL            ;SAVE HL
        POP     H               ;GET PC FROM STACK
        SHLD    APPC            ;SAVE PC
        LXI     H,0             ;SET HL=SP
        JC      ENTR1           ;    J IF CY FLAG SET
        DAD     SP              ;    HL=SP, CY=0
        JMP     ENTR2           ;    CONTINUE
ENTR1:
        DAD     SP              ;    HL=SP, CY=0
        STC                     ;    SET CY=1 AGAIN
ENTR2:
        SHLD    APSP            ;SAVE SP
        LXI     SP,APPSW+1      ;SET MONITOR SP
        PUSH    PSW             ;SAVE REMAINING REGISTERS
        PUSH    B
        PUSH    D
          .
          .
          .
        ORG     (ADDRESS OF REGISTER TABLE IN MONITOR RAM)
APDE:   DS      2               ;STORAGE FOR E AND D REGS
APBC:   DS      2               ;STORAGE FOR C AND B REGS
APPSW:  DS      2               ;STORAGE FOR A REG AND FLAGS
APHL:   DS      2               ;STORAGE FOR L AND H REGS
APPC:   DS      2               ;STORAGE FOR PC(L) AND PC(H)
APSP:   DS      2               ;STORAGE FOR SP(L) AND SP(H)
```

counter (PC) of the application program from the stack. If PC-1 equals a breakpoint address, the breakpoint routine concludes that the designer has executed a breakpoint location. If not, it assumes that the system has been reset.

If the application program SP is not pointing to R/W memory when the restart instruction is executed (because of some error in the program or because the designer forgot to initialize the SP before entering the execute command), then the breakpoint routine will pop a meaningless PC, and will assume a reset has occurred. The monitor cannot protect itself from this occurrence because the use of the restart instruction for breakpoint implementation assumes that the SP points to R/W memory.

The processing required to freeze the system and save the CPU registers when the breakpoint routine is entered is contained in the first process box of Fig 7; the 8080A code that accomplishes this processing is shown in the Program Listing. The designer's stack is not used as temporary scratchpad in saving the registers. Both Intel monitors save the CPU registers

by pushing them, at least temporarily, onto the designer's stack. Therefore, neither monitor can be certain of correctly saving the registers because the designer's SP may be set improperly. The present design can guarantee saving all the registers correctly (except the PC, which must be retrieved from the stack), even if the designer's SP does not point to R/W memory.

In the Listing, the entire set of application program registers is saved in the monitor register table without utilizing the application program stack. HL register pair is saved first, followed by PC, which is popped from the stack. SP is saved next and, since the DAD SP instruction clears the carry flag (CY) in this program, a branch to ENTR1 is necessary if CY is set. SP is then reloaded, and the remaining registers are saved. Once this occurs, SP is properly positioned at the beginning of the monitor stack area, as shown in Fig 5.

Similar considerations are used in implementing the G and P commands. The Intel monitors implement the G command by executing a group of instructions set up in the monitor R/W data segment, which restores the application program register values to the CPU, and jumps to the selected start address. However, these instructions are set up in the monitor data segment only at power-up/reset and may be overwritten by an errant program without the designer realizing it. In the present design, the registers are restored by instructions in the code segment that cannot be overwritten. A jump instruction is set up in the monitor data segment each time a G or P command is entered. This guarantees that the designer's register values will be restored properly to the CPU and that the designer will at least reach the desired start address in the program under test. For the G command, instructions to enable interrupts and jump to the specified address are set up in a 4-byte buffer in the monitor data segment, and are the last instructions executed by the monitor before the application program takes over.

```
EI          ; Enable interrupts
JMP  X      ; Jump to address X
```

where X is the specified start address. The P command sets up the same jump instruction but prefaces it with a disable interrupts (DI) instruction instead of an enable interrupts (EI) instruction.

If the monitor I/O port(s) use programmable chips (such as the 8251 universal synchronous/asynchronous receiver/transmitter for the command terminal interface), it is desirable to initialize and program them immediately after saving the application program CPU registers. (Ideally, none of the I/O ports should be shared by the application program.) Initializing the chips on every monitor entry will guarantee that the port(s) will operate correctly even if the application program has inadvertently reprogrammed them by executing erroneous code.

The idea of reinitializing the monitor I/O port(s) on every entry illustrates an important point in designing debug software; namely, always assume that errors exist in the program. Allow the monitor to refresh its proper state as frequently as possible to assure reliable operation despite the potentially unfriendly intrusion of an untested program.

Summary

This software breakpoint design approach serves the 8080A microprocessor operating within the structure of a debug monitor. Breakpoints are implemented with the RST 0 instruction, allowing the seven remaining interrupt levels to be used by the program under test. The design is therefore well suited to debugging and testing complex interrupt driven, realtime software. Shortcomings and reliability problems associated with the interaction between the software under test and breakpoint processing are discussed, as are suggestions of mechanisms for minimizing errors and notifying the designer of problems.

Although the present design is directed to the 8080A, the general problems encountered are common to many microprocessors. The design adopted in other cases depends heavily on the architecture of the particular microprocessor. From the designer's point of view, the most important objectives to be achieved in a breakpoint design are reliability and minimal use of the processor resources.

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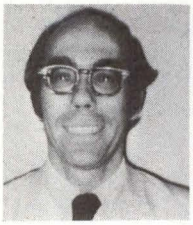
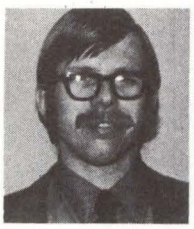


Thomas P. Hughes is a consultant specializing in microprocessor applications and systems, and realtime software development. He previously was a senior microprocessor systems specialist. He has received BA, MS, and PhD degrees in physical chemistry from Rutgers University.



Serving as a research engineer with Corporate Research of Foxboro Co, Dwight H. Sawin III has previous experience as a design engineer with the U.S. Army Computer Techniques and Development Team of the Center for Tactical Computer Sciences. He holds BSEE and PhD degrees in electrical engineering from the University of Idaho.

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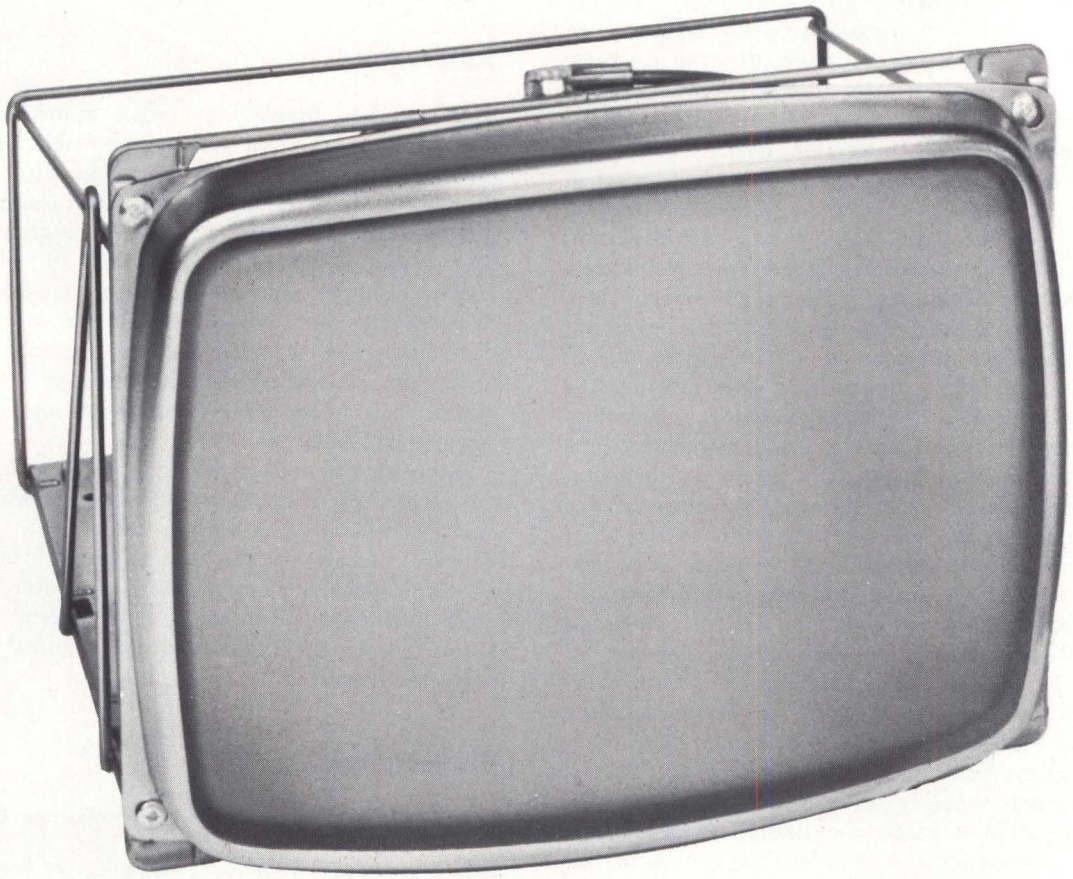

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SIMPLE HARDWARE APPROACH TO ERROR DETECTION AND CORRECTION

For reliable data transmission/reception, decimal checksum and modulus arithmetic techniques are derived that pinpoint location of single- and double-error bits. Simple hardware circuits have been designed to correct such errors automatically, at low cost and at low complexity in system integration

Richard C. Montgomery Honeywell, Inc, Denver, Colorado*

Single- and double-error correction codes can be developed for reliable data communication through a simplified approach that relies on hardware rather than on mathematical terms. A number of texts[1,2] have presented the fundamental properties of digital error detection and correction codes in mathematical terms, but little material has been provided dealing with specific hardware implementation.

To establish a background for a discussion of a simple method for developing and implementing such codes in hardw re, assume that a transmitter (T) emits groups of 15 binary bits (Fig 1). Assume also that if the bits are used to imply a number, position 1 is the least significant bit (LSB), position 15 the most significant bit (MSB), weighting is as indicated, and the bits are transmitted serially with bit 15 first. Of these bits, some are data taken from a random source, and some are error-control that are inserted as desired.

A receiver (R), which receives the 15-bit groups, has the task of detecting errors that might have occurred while transferring the groups from transmitter to receiver. If all 15 bits are derived from a random data source, there is no method for determining whether an error has occurred. Therefore, it must be ascertained how many error-control bits to insert and how to use them.

A simple method is to utilize bit 1 as a parity bit. Thus, bit 1 is adjusted so that the total number of 1s in the 15-bit group is odd, resulting in 14 data bits in bit positions 2 through 15, and an odd parity bit in position 1. At the receiver, the 15 bits are examined (either serially, one at a time, or in parallel, all at once) to gain information about possible errors. If no errors occur in transmission, there will be an odd number of 1s in the 15-bit sequence. If an odd number of errors occur (1, 3, 5, . . . , 15), the number of 1s in the received sequence will be even. If an even number

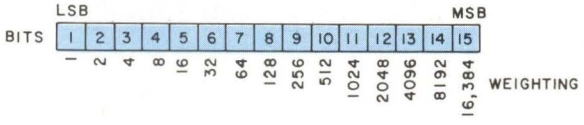


Fig 1 Format of assumed data stream for serial data transmission. MSB is transmitted first, followed by remaining bits

*Mr Montgomery is currently employed at EMR Telemetry, Sarasota, Florida.

of errors occur, the received sequence will contain an odd number of 1s, the same as if no errors occur.

In any case, although this parity method can detect errors, it cannot correct them. The parity bit may show that one of the 15 bits is in error, but it is of no help in identifying that bit. Therefore, to implement codes capable of correcting errors, the first goal is to correct a single-error bit. Simply stated, when the 15-bit block has been processed by the receiver, there should be a pointer, made up of several bits, that directly picks out which bit, if any, is in error.

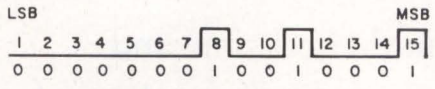


Fig 2 Typical serial data format. Bits 15 (MSB), 11, and 8 are logic 1; remaining bits are logic 0

Decimal Checksum

To examine this method, analyze the following possible solution. Circuitry could be added to the transmitter to determine the number of each bit transmitted (in 1 through 15 notation) and, if a particular bit is a 1 (ON or activated), add the position number of that bit to a checksum (called $R(X)_T$). For example, in Fig 2, 1s are located in bit positions 15, 11, and 8. Thus, the checksum is $R(X)_T = 15 + 11 + 8 = 34$.

If sufficient space exists in the 15-bit sequence, this checksum can be transmitted along with the data (ie, some bits are data and some are checksum). When this sequence is received, a second checksum, $R(X)_R$, is computed and compared to the checksum transmitted. If the message is received with no errors, $R(X)_R = 15 + 11 + 8 = 34$, and $|R(X)_T - R(X)_R| = |34 - 34| = 0$ (no errors). Suppose, however, that a single error occurs and causes a 1 to appear in bit position 13. In this case $R(X)_R = [15 + 13 + 11] + 8 = 47$, and $|R(X)_T - R(X)_R| = |34 - 47| = 13$, indicating that bit 13, as received, is incorrect. Similarly, if a single error occurs and causes bit 8 to be a 0, $R(X)_R = 15 + 11 = 26$, and $|R(X)_T - R(X)_R| = |34 - 26| = 8$, indicating that bit 8, as received, is incorrect.

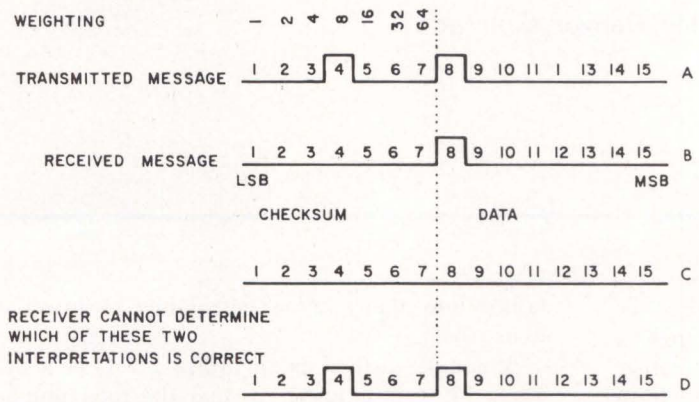


Fig 3 Simple decimal checksum. In this technique, some errors may not be isolated. If message sequence A is transmitted, and an error causes sequence B to be received, receiver cannot determine whether bit 8 was added (C) or bit 4 was deleted (D)

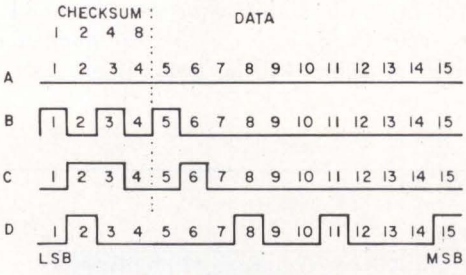


Fig 4 Modulo-16 arithmetic. When this method is used for checksum generation, only four positions are required for checksum; A, B, and C show checksum which would result from certain data bit patterns. D shows that modulo-16 sum of 15 + 11 + 8 = 2, as discussed in text

While this method could be implemented, it has two disadvantages. First, the checksum expressed as a binary number can be large, thus unnecessarily occupying many of the 15 bits being used. Second, if single errors occur in the checksum, they may be interpreted incorrectly (Fig 3).

Modulus Arithmetic

To correct the first disadvantage (too many bits for

the checksum), consider the following example. Position numbers of bits 1 through 15 require only four binary bits for definition, that is, 0001 through 1111. Thus, when the transmitter adds up the checksum, made up of four bits, it could discard the portion of any sum that results in a number larger than 15, ie, number 16. Using this technique, the example of Fig 2 yields

$(15 + 11) = 26 \rightarrow 26 - 16 = 10;$

$(10 + 8) = 18 \rightarrow 18 - 16 = 2.$

Thus, the transmitted checksum is $R(X)_T = 2 = 0010$. This method of adding is called modulo-16 addition.

Continuing with the same data (Fig 2), suppose an error occurs and causes a 1 to appear in bit position 13. The receiver computes its checksum as

$(15 + 13) = 28 \rightarrow 28 - 16 = 12;$

$(12 + 11) = 23 \rightarrow 23 - 16 = 7;$

$(7 + 8) = 15;$ or $\leftarrow R(X)_R = 15.$

As before, $|R(X)_T - R(X)_R| = |2 - 15| = 13$, pointing to the error at bit position 13. Testing shows that this approach is valid, so that 15-bit sequences (Fig 4) can be used to correct single data errors, using 11 data bits and 4 checksum bits.

Modulo-2 Arithmetic

While modulo-16 addition is not particularly difficult to implement in hardware, a simpler arithmetic, called modulo-2, works equally well. The truth table for modulo-2 arithmetic, along with a modulo-2 adder, is shown in Fig 5. Returning to the data sequence of Fig 2, modulo-2 arithmetic provides

```
 15 = 1 1 1 1
+11 = 1 0 1 1
     0 1 0 0    Modulo-2
 +8 = 1 0 0 0
R(X)T = 1 1 0 0  Modulo-2
```

If an error occurs and causes bit position 8 to be a 0,

```
 15 = 1 1 1 1                R(X)T = 1 1 0 0
+11 = 1 0 1 1               −R(X)R = 0 1 0 0
R(X)R = 0 1 0 0  Modulo-2           1 0 0 0 = 8
```

Position Renumbering

The second disadvantage concerns errors that occur in the checksum. In the sequence shown in Fig 3, if the 1 in bit position 4 is erased, the receiver cannot determine whether the error is in bit position 4 or in bit position 8. The problem is that there are bit positions in the data sequence that can change the checksum by only one bit when they are added or deleted, as follows:

Checksum Weighting	Checksum Bits 1 2 3 4	
1	1 0 0 0	Error Positions (1)
2	0 1 0 0	
4	0 0 1 0	
8	0 0 0 1	

This situation is not a problem with checksum bit positions 1 or 2 because they point to themselves. The problem occurs when an error appears in bit position 3, giving $|R(X)_T - R(X)_R| = 4$, or an error in bit position 4 gives $|R(X)_T - R(X)_R| = 8$.

This problem can be solved by renumbering the bit positions. In Fig 1, the bits are numbered 1 to 15 in sequence from left to right. Consider the numbering scheme shown in A of Fig 6, called bit location numbers. A shows that if an error occurs in bit location 4, the checksum changes by 4. The remaining data-bit positions can be numbered as desired, as long as 1, 2, 4, and 8 are not used. B shows the chosen numbering method. Other numbering methods would also work.[3,4]

Checksum Generation

Having overcome both disadvantages, hardware implementation is considered. In Fig 7, assume that the

A	B	C = A + B	C = A−B OR B−A
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

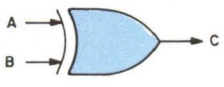


Fig 5 Modulo-2 arithmetic. One reason why modulo-2 arithmetic is more convenient is because addition and subtraction look the same. Modulo-2 addition or subtraction is equivalent of exclusive-OR of two signals, as shown in truth table and gate

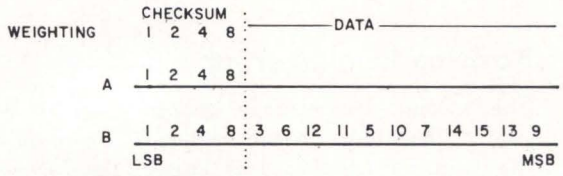


Fig 6 Renumbering bit positions. Scheme resolves ambiguities of Fig 2, and provides workable error detection and correction code. Bits have been renumbered so that location numbers of checksum bits correspond to their binary weights, as in A. Data locations can be numbered as desired, as long as 1, 2, 4, and 8 are not used

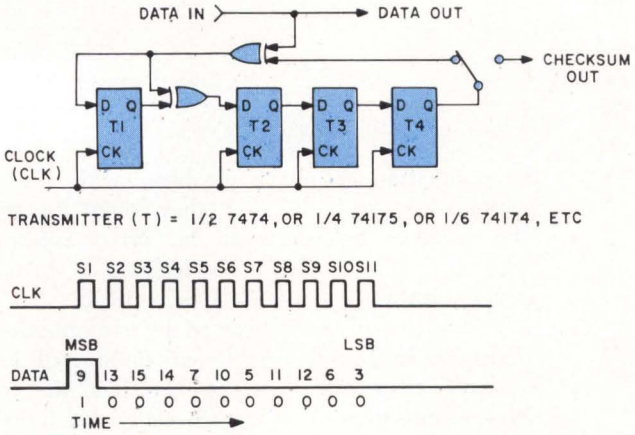


Fig 7 Transmitter checksum hardware circuit. This circuit generates checksum corresponding to bit location numbers of Fig 6. If T1 to T4 are initially 0, and a bit is shifted in at S1, followed by 0s at S2 to S11, the content of T1 to T4 will be 1001_2, or 9_{10}, the location number of the MSB

four transmitter flip-flops (T1 to T4) are initially set to 0, and that the data sequence contains a 1 in the MSB, followed by ten 0s. In this case, the following sequence occurs:

Clock	Data	(MSB) T_4 T_3 T_2 T_1 (LSB) 0 0 0 0	Decimal No.
S1	1	0 0 1 1	3
S2	0	0 1 1 0	6
S3	0	1 1 0 0	12
S4	0	1 0 1 1	11
S5	0	0 1 0 1	5
S6	0	1 0 1 0	10
S7	0	0 1 1 1	7
S8	0	1 1 1 0	14
S9	0	1 1 1 1	15
S10	0	1 1 0 1	13
S11	0	1 0 0 1	9

Treating this transmitter sequence as 4-bit binary numbers (with T_1 = LSB and T_4 = MSB), the same bit location numbers evolve as used for the data positions of B in Fig 6, that is, 3, 6, 12, 11, 5, 10, 7, 14, 15, 13, and 9. Furthermore, if a 0 appears in the data MSB, a 1 in the next bit (MSB-1), and then nine 0s, the sequence ends at 13 (S10). Similarly, correct results occur if a 1 appears in any single data-bit position.

Now, consider the transmitter data sequence that occurs with 1s in the two MSB positions (9 and 13) and 0s in the remaining positions, as follows:

Clock	Data	(MSB) T_4 T_3 T_2 T_1 (LSB) 0 0 0 0	Decimal No.
S1	1	0 0 1 1	3
S2	1	0 1 0 1	5
S3	0	1 0 1 0	10
S4	0	0 1 1 1	7
S5	0	1 1 1 0	14
S6	0	1 1 1 1	15
S7	0	1 1 0 1	13
S8	0	1 0 0 1	9
S9	0	0 0 0 1	1
S10	0	0 0 1 0	2
S11	0	0 1 0 0	4

Thus, the content of T_1 through T_4 corresponds to the checksum expected if the bit location numbers of the two MSBs are added (modulo-2)

1 1 0 1 = 13 (MSB-1 Location)

+1 0 0 1 = 9 (MSB Location)

0 1 0 0 = 4 (Modulo-2) = S11

Furthermore, if the two 1s in the transmitter data sequence had occurred one clock time later, the final result (S10) would have corresponded to the proper modulo-2 sum.

15 = 1 1 1 1 (MSB-2 Location)

13 = 1 1 0 1 (MSB-1 Location)

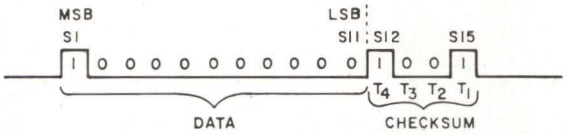
2 = 0 0 1 0 = S10 (Modulo-2)

Thus, the hardware of Fig 7 not only counts in the sequence desired, but also performs correct modulo-2 addition. For any 11-bit data sequence, the hardware of Fig 7 generates the proper checksum required for error detection and correction at the receiver.

Single-Error Detection

The checksum can be used by the receiver to detect and/or correct errors with the receiver circuit shown in Fig 8. It is almost identical to the circuit used at the transmitter, the difference being that the data are applied at the least significant position. Also, the receiver handles a 15-bit sequence, consisting of 11 data bits and 4 checksum bits.

Operation of the receiver can be examined by assuming that a message, consisting of the MSB data bit and its proper checksum, is transmitted correctly. The selected transmitted message then appears on an oscilloscope as



The sequence in the receiver register (R_1 to R_4), initially assumed to be zero, would be

Clock	Data	Checksum (MSB) R_4 R_3 R_2 R_1 (LSB)	Decimal No.
		0 0 0 0	
S1	1	0 0 0 1	1
S2	0	0 0 1 0	2
S3	0	0 1 0 0	4
S4	0	1 0 0 0	8
S5	0	0 0 1 1	3
S6	0	0 1 1 0	6
S7	0	1 1 0 0	12
S8	0	1 0 1 1	11
S9	0	0 1 0 1	5
S10	0	1 0 1 0	10
S11	0	0 1 1 1	7
S12	1	1 1 1 1	15
S13	0	1 1 0 1	13
S14	0	1 0 0 1	9
S15	1	0 0 0 0	0

At clock pulse S15, the receiver register contains decimal number zero (0000_2). Thus, the receiver register has calculated the checksum of the 11 data bits, and subtracted from it the four transmitted checksum bits. The zero at S15 indicates that no error occurred in the transmitted sequence.

Suppose that the same sequence is transmitted, but that an error (E1) occurs, causing the following sequence to be received:

Clock	Data	Checksum (MSB) R_4 R_3 R_2 R_1 (LSB)	Decimal No.
		0 0 0 0	
S1	1	0 0 0 1	1
S2	0	0 0 1 0	2
S3	0	0 1 0 0	4
S4	E1	1 0 0 1	9
S5	0	0 0 0 1	1
S6	0	0 0 1 0	2
S7	0	0 1 0 0	4
S8	0	1 0 0 0	8
S9	0	0 0 1 1	3
S10	0	0 1 1 0	6
S11	0	1 1 0 0	12
S12	1	1 0 1 0	10
S13	0	0 1 1 1	7
S14	0	1 1 1 1	15
S15	1	1 1 1 0	14

At clock pulse S15, the receiver register contains 1110_2, which is 14_{10}. Referring to Fig 8, 14 is the location number of the bit that occurs at S4. Checking confirms that if any single error occurs in any properly encoded sequence, the receiver register contains the appropriate error-location number at S15 (using the notation of Fig 8). Thus, the following is true at S15:

a. No errors: R_4 through R_1 = 0000,

b. 1 error: R_4 through R_1 = bit location number in Fig 8 notation,

c. 2 errors: R_4 through $R_1 \neq$ 0000, never 0,

d. 3 to 15 errors: R_4 through R_1 = Not 0 $\left(\frac{(2^4 - 1)}{2^4}\right.$ or 94% of the time$\left.\right)$, = 0 (1/2^4 or 6% of the time).

Finally, if R_1 through R_4 are used for error detection only, they will detect all single and double errors, and approximately 94% of all multiple (3 to 15) errors.

Single-Error Correction

If the MSB of the data is in error, R_4 through R_1 (Fig 8) produce 1001_2 or 9_{10} at S15. Also, if the bit after the MSB is in error, R_4 through R_1 are equal to 1101_2 or 13_{10}. Then, if the receiver register is right-shifted once, with a zero input (0000), 1101_2 becomes 1001_2. This behavior is consistent, and provides the basis for Fig 9.

The circuit of Fig 9 operates as follows. Incoming data are entered into a 15-bit shift register (A). Gate (B) is provided so that 15 bits of the received sequence can be shifted into (C), followed by 0s. During the time that the received sequence is being processed by (C), the checksum is formed as previously discussed (Fig 8 and examples). When the last bit of the trans-

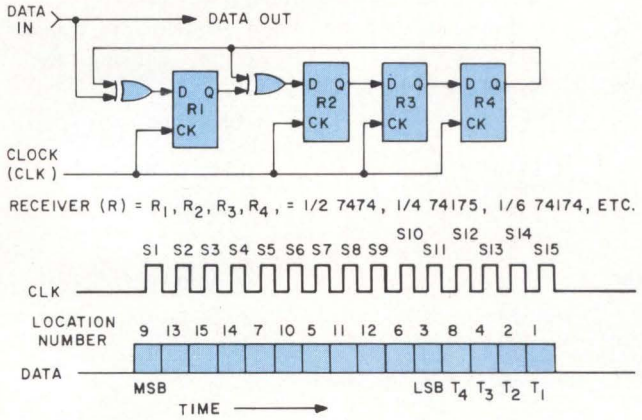


Fig 8 Receiver circuit for single error detection. Circuit processes data produced by transmitter of Fig 7, and produces $|R(X)_T - R(X)_R|$ error-location pointer. Fifteen bits, made up of 11 data bits followed by 4 checksum bits, are shifted into the register, resulting in 0 if no error occurred, or an error location number

mitted checksum is in (C), the MSB of the received sequence is at the output of (A). If the data are error-free, R_4 through R_1 are 0_{10} (0000_2), and no correction occurs. If any single bit (X) is in error, R_4 through R_1 are 1001_2 or 9_{10} when (X) arrives at the output of (A); then, (D) and (E) cause (X) to be corrected. In a real system, it is best to disable (D) during the time that data are being entered into (C), because the pattern 1001_2 might legitimately occur during computation.

The circuitry of Fig 9 is usually the simplest method of correcting single errors. Even if the data stream is continuous (so that one 15-bit block is being processed while the previous 15-bit block is being corrected), it is only necessary to duplicate (C) and to provide correct gating signals.

Other Checksum Generators

As previously described, B in Fig 6 is not the only numbering sequence that will work. Published lists exist that can be translated into the required feedback connections, with registers similar to Figs 7 and 8, to generate other sequences.[3] These lists commonly use the following notation: Fig 7 would be referred to as $X^4 + X + 1$; that is, X^4 (the output of T^4) is added (modulo-2) to X (the input of T_2) and 1 (the data input of T_1).

In Peterson's notation,[3,4] $X^4 + X + 1$ could also be written as 23_8, representing $(010)\,(011) = 0X^5 + 1X^4 + 0X^3 + 0X^2 + 1X + 1 = X^4 + X + 1$. One register connection, which will generate a workable sequence, is the reciprocal of $X^4 + X + 1$, which is

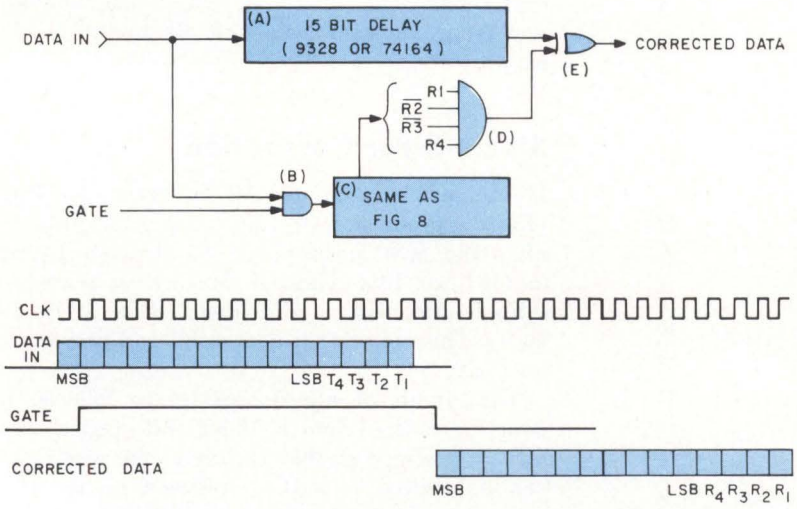


Fig 9 Single-error correction circuit. Circuit processes data produced by transmitter of Fig 7 and uses error-location pointer to correct an error. Fifteen bits of data are shifted simultaneously into A and C; the checksum $|R(X)_T - R(X)_R|$ is computed in C. If a single error occurs, the erroneous bit will appear at output of A at the same time that $R_1R_2R_3R_4 = 1001$. Gate D detects the 1001, and causes E to invert (correct) erroneous bit

$$\frac{X^4}{X^4} + \frac{X^4}{X} + \frac{X^4}{1} = 1 + X^3 + X^4 = X^4 + X^3 + 1,$$

or in Peterson's notation 31_8. Of these two choices, 23_8 or 31_8, only one would be listed by Peterson.

Double-Error Correcting Checksums

Referring to Fig 6, single-error correction works because the checksum is able to point to 0 for no errors, or to 1 of 15 specific, single-bit errors. A double-error correcting checksum must still be able to point to 0 if no errors occur, and to the 15 possible single-bit errors. Also, a double-error correcting checksum must be able to point out 14 errors that involve the MSB and 1 other bit, 13 errors that involve the next MSB and another bit, etc. In total, it must be able to locate 15 + 14 + 13 + 12 + 11 + 10 + 9 + 8 + 7 + 6 + 5 + 4 + 3 + 2 + 1 = 120 single or double errors plus the error-free condition. The smallest integer N for which $2^N - 1$ is greater than 120 is N = 7. Although it is possible to construct sequences of seven checksum bits and eight data bits with some double-error correcting capability, it is not attempted here because no such sequence corrects all double errors. This article explores, instead, the possibility of constructing a sequence of eight checksum bits and seven data bits with double-error correction capability. In previous examples, when the receiver completed its calculations, the checksum register contained the location, in format B of Fig 6, of the erroneous bit (or 0 for no error). Since similar construction is used for double-error correction, the checksum ends up with

a. 0 for no errors,

b. bit location of the error for 1 error, or

c. modulo-2 sum of the locations of two errors.

This requires that (a) the checksum associated with any one of the 15 single-error locations points to that location, and (b) the modulo-2 sum of any two single-error checksums points to a unique pair (and not to any single-error position). In the single-error correcting example, the checksums are arranged so that changing any single data bit causes at least two checksum bits to change. In fact, the numbering is changed to that of B in Fig 6 to accomplish this. This property is referred to as "minimum distance," and the coding used has a minimum distance of 3; that is, 1 (data bit) plus at least 2 (checksum bits) equals at least 3 (minimum distance). A double-error correcting checksum requires a minimum distance of 5. That is, changing one data bit must cause at least four checksum bits to change.

The particular checksum generator chosen is (in Peterson's notation[3,4]) 721_8, or $X^8 + X^7 + X^6 + X^4 + 1$ (Fig 10). This generator is the modulo-2 product of generators 23_8 $(X^4 + X + 1)$ and 37_8 $(X^4 + X^3 + X^2 + X + 1)$. This generator meets the requirements, stated in proper terms, because the polynomial $(X^8 + X^7 + X^6 + X^4 + 1)$ has four consecutive roots, guaranteeing a minimum distance of five units.[5]

If a 1 followed by six 0s of data is shifted into this register, the resulting states are

Data		Checksum (MSB) T_8	T_7	T_6	T_5	T_4	T_3	T_2	T_1 (LSB)	Decimal No.
		0	0	0	0	0	0	0	0	
9	1	1	1	0	1	0	0	0	1	209
10	0	0	1	1	1	0	0	1	1	115
11	0	1	1	1	0	0	1	1	0	230
12	0	0	0	0	1	1	1	0	1	29
13	0	0	0	1	1	1	0	1	0	58
14	0	0	1	1	1	0	1	0	0	116
15	0	1	1	1	0	1	0	0	0	232

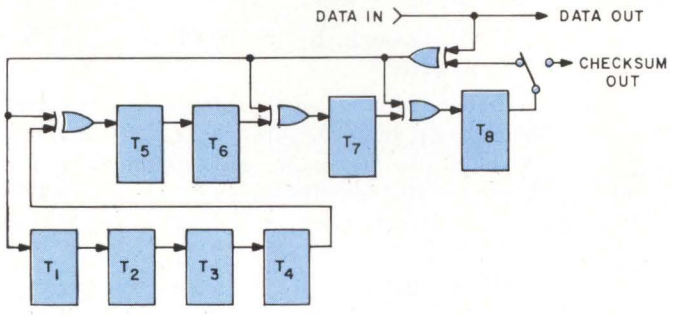


Fig 10 Double-error transmitter circuit. This generates 15-bit sequences with an 8-bit double-error correcting checksum. The checksum corresponds to the polynomial $X^8 + X^7 + X^6 + X^4 + 1$, which is product of $X^4 + X + 1$ and $X^4 + X^3 + X^2 + X + 1$. If seven data bits are shifted in, the resulting state of T1 to T8 will be the eight checksum bits

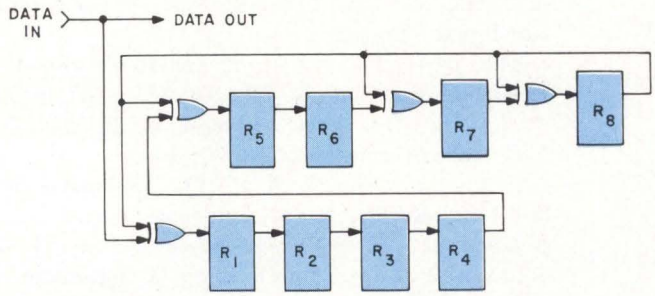
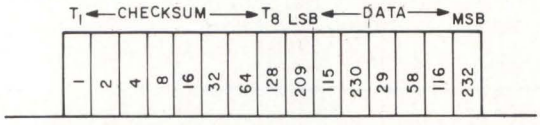


Fig 11 Double-error receiver pointer circuit. Register processes data produced by transmitter of Fig 10, and provides error-location pointer capable of correcting double errors. 15-bit sequence, consisting of 7 data bits followed by 8 checksum bits, is shifted in; result can point to any combination of one or two errors

In the notation of Fig 6, the location numbers of the sequence generated by Fig 10 are



No two location numbers are the same, thereby ensuring that single errors can be corrected. Note that the modulo-2 sum of any two location numbers does not equal the sum of any other pair of location numbers or any single location number, thus ensuring double-error correction.

One-Step Lookup

The checksum generator used at the receiver is shown in Fig 11. Observe its similarity to Fig 8 and Fig 10. If seven bits of data followed by eight bits of checksum (generated by Fig 10) are shifted through Fig 11, the result is

a. 0 if no errors occur,

b. 1 of the 15-bit location numbers if a single error occurs,

c. 1 of the 105 pair pointers if a double error occurs, or

d. 1 of the 135 (256 - 121) pointers to uncorrectable (?) multiple errors, but not 0 unless five or more errors occur.

The correction circuitry is shown in Fig 12. When the 15th bit of the received sequence has been shifted into (A) and (D), R_1 through R_8 contain the 8-bit checksum. This checksum is used to address P/ROM(B). The output of (B) (ie, data D_1 to D_8 at address R_1 through R_8) is routed to decoders (C1) and (C2). Decoder (C1) points to one of the erroneous bits in (D), if there are any. Decoder (C2) points to the other erroneous bit in (D), if there is another. Thus, the data are corrected immediately.

The only difficult aspect of Fig 12 is the programming of the P/ROM. This may be done as follows:

e. If R_8 through R_1 = 00000000, then D_8 through D_1 = no error

f. If one of the single errors is indicated by R_8 through R_1, then D_4 through D_1 = 0 and D_8 through D_5 point to the error. For example, if R_8 through R_1 = 11101000, D_4 through D_1 = 0000 and D_8 through D_5 = 1111, indicating a single error at bit position 15 (the MSB).

g. If R_8 through R_1 indicates an error pair, D_4 through D_1 points to one error, and D_8 through D_5 points to the second error. For example if R_8 through R_1 = 10100101, D_4 through D_1 = 1001 and D_8 through D_5 =1110, indicating two errors at bit positions 9 and 14.

Since it is not usually necessary to correct errors in

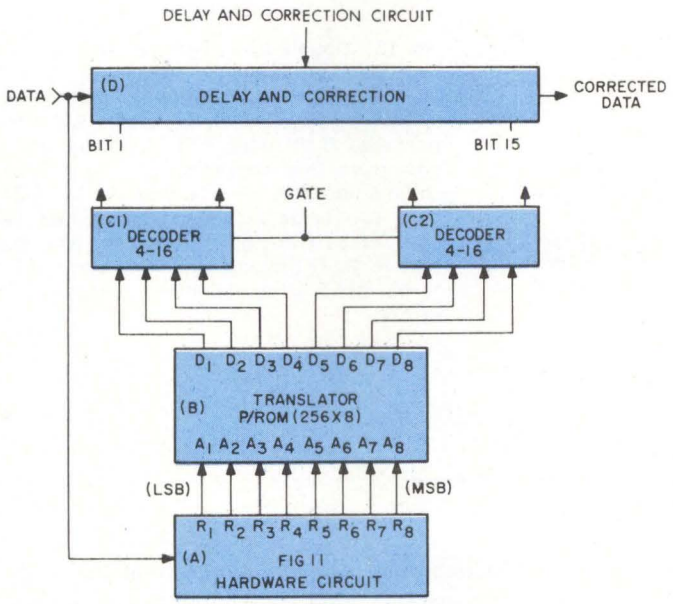


Fig 12 Double-error receiver correcting circuit. This processes data from Fig 10, and uses a P/ROM to translate checksum into bit location of up to two errors. Both errors can be corrected immediately. A 15-bit sequence, 7 data bits and 8 checksum bits, is shifted simultaneously into D and A. Checksum is used to address P/ROM B, whose outputs point to zero, one, or two errors associated with the checksum. One error is corrected via C1, the other via C2, when enabled by the GATE signal

the checksum bits, it may be necessary only to program 85 of the P/ROM locations:

h. 1 place for no errors,

i. 7 places for single-data errors,

j. 21 places for double-data errors, and

k. 56 places for one data and one checksum error.

The remaining P/ROM locations must point to some harmless place, such as the no-error location. The bulk of the double-error correcting receiver circuit could be constructed from the following:

l. four 8504s (presettable polynomial generator) for (D) delay and correction,

m. five 7404s (hex inverter) and two 74154s (4-line to 16-line decoder/demultiplexer) for (C1) and (C2) decoders,

n. one 74S471 (P/ROM) for (B) or 82S114 (P/ROM), and

o. two 74175s (quad, D-Type, flip-flop) and one 7486 (quad, 2-input, Exclusive-OR) for (A) or two 8504s (presettable polynomial generator).

Programming of the P/ROM can be hand-calculated or done on a computer.

The construction shown in Fig 12 is reasonably cost effective for 15-bit sequences. A similar construction could be extended to longer sequences, for example, a 21-bit data with a 10-bit checksum sequence, etc. A similar construction also works for triple (or higher) error-correcting codes. In either case, there is a practical limit because of the size of the required P/ROM.

Two-Step Lookup

Consider a different construction that requires less P/ROM, but more circuitry. As previously mentioned, the checksum generator of Figs 10 and 11 is the modulo-2 product of two smaller generators. The receiver version of these generators is shown in Fig 13. It can be verified that any error-free sequence encoded per Fig 10 results in R_{11} through R_{14} = 0000, and R_{21} through R_{24} = 0000, if received error-free.

If a single error occurs, the content of R_{11}-R_{14}, after the 15 bits are shifted in, will be the same error location numbers that were generated by Fig 8. This same single error will generate an error location number in R_{21}-R_{24}, different from that in R_{11}-R_{14}. A table can be generated which shows the error checksum in R_{11}-R_{14} and R_{21}-R_{24}, for each of the 15 possible error locations. If, for example, the MSB is in error, R_{11}-R_{14} = 1001 and R_{21}-R_{24} = 1111.

If a double error occurs, the content of R_{11}-R_{14} and R_{21}-R_{24}, after the 15 bits have been shifted in, will be the modulo-2 sums of the error location numbers

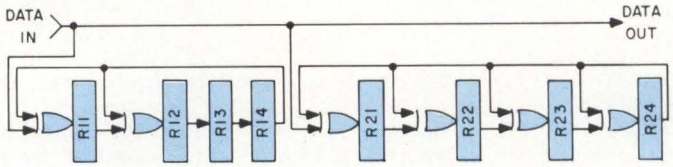


Fig 13 Double-error receiver pointer circuit. Data produced by transmitter of Fig 10 can be processed through pair of receiver registers which generate two error pointers. If 7 data bits, followed by 8 checksum bits generated by Fig 10, are shifted into R11 to R14 and R21 to R24, then two error location pointers will result. These two pointers (R11 to R14 and R21 to R24) provide sufficient information to correct any combination of one or two errors

of the two individual errors. If, for example, the MSB and the MSB-1 are in error,

$$\begin{array}{rr} R_{11}\text{-}R_{14} = & 1001 \\ & +1011 \\ \hline & 0010 \end{array} \qquad \begin{array}{rr} R_{21}\text{-}R_{24} = & 1111 \\ & +0001 \\ \hline & 1110 \end{array}$$

The key point is that no combination of one or two errors other than MSB and MSB-1 will cause R_{11}-R_{14} = 0010 and R_{21}-R_{24} = 1110 simultaneously.

Error correction can be done as follows: A 15-bit sequence, 7 data bits followed by 8 checksum bits, is shifted into a 15-bit delay register and simultaneously into R_{11}-R_{14} and R_{21}-R_{24}. R_{11}-R_{14} are used to address a P/ROM, whose outputs D_1-D_4 are the values expected in R_{21}-R_{24} if an error occurred in the MSB and another bit. If D_1-D_4 = R_{21}-R_{24}, the MSB is corrected as it leaves the delay register. If D_1-D_4 = R_{21}-R_{24}, R_{11}-R_{14} and R_{21}-R_{24} are shifted (with 0 input) and the check for D_1-D_4 = R_{21}-R_{24} is repeated.

It can be verified that the following will occur

No Error: R_{11}-R_{14} = 0000 R_{21}-R_{24} = 0000

One error: D_1-D_4 = R_{21}-R_{24} once during 15 shifts, correcting the single error as it leaves the delay register.

Two errors: D_1-D_4 = R_{21}-R_{24} twice during 15 shifts, correcting each of the two errors as they leave the delay register.

Summary

Presenting single- and double-error correction codes as a form of arithmetic, rather than algebra, may simplify the use and understanding of these codes. The checksum methods discussed allow analysis of both random and burst-error correction codes. The most important consideration is that the receiver checksum generator used must produce a unique checksum associated only with the error to be corrected. As the cost of memory elements decreases, the 1- and 2-step multiple-error correction decoders described become increasingly effective when compared to traditional methods. The hardware techniques described can be used with a wide variety of error correction block lengths, and are applicable to single-, double-, and multiple-error correction procedures.

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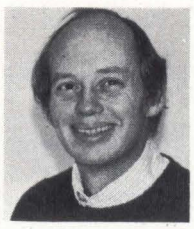

Richard C. Montgomery has been involved in design of data encoding/decoding electronics for magnetic tape recording of high rate data streams, as well as in design of mini- and microcomputer based digital control and data analysis systems. He has a BS degree in physics from California Institute of Technology.

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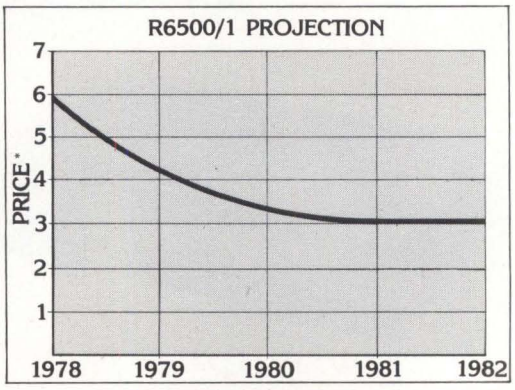

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MULTIPLE PROCESSOR MINICOMPUTER SYSTEMS— PART 2: IMPLEMENTATION

Cost-effective MPS design can be assured through application of systematic design methodology that allows alternative architectures to be compared

Burt H. Liebowitz International Computing Company, Bethesda, Maryland

Part 1 of this 2-part article, published in October, provided a comprehensive overview of distributed processing design concepts by comparing mainframes and multiple processor systems as to advantages and disadvantages, cost-effectiveness, and technical aspects, and presented a systematic approach to the resolution of issues essential to successful design of such systems. Emphasizing these basic principles, Part 2 concludes the discussion by applying the MPS design guidelines to resolve realtime computational system situations.

The process of designing a multiple processor system encompasses successive major tasks. The first involves the development of a detailed functional requirements specification (Table 1). After this specification is available, a conventional engineering approach is applied to develop a uniprocessor design in terms of a standard computer. For example, a computer X times as powerful as the standard computer with Y words of main memory and a certain file structure will satisfy system requirements. This model provides a starting point for the distributed system design. Then, several architectures using X or more standard computers are developed and compared. Finally, the most promising architecture is selected and refined against the requirements. In a multisite structure, the architecture is evaluated against several traffic models, representing the range of site characteristics.

Standard Computer

The standard computer represents an available and thoroughly understood computer that is *a priori* determined to be a viable candidate for the multiple processor system (MPS) design solution. For example, in a recent effort, the Varian L-100, a 16-bit minicomputer with a 1-μs memory cycle time, was selected as the standard computer. A specially developed algorithm then allowed other computers to be compared with the

TABLE 1

MPS Functional Requirements Specification

- Purpose
- Functions
- Data Flow
- Outputs
- Data Base Requirements
- Performance Requirements (transaction rates, and response times)
- External Interfaces
- Reliability Requirements
- Growth Requirements
- Site Requirements (for a multisite system)
- Design Constraints
- Test Requirements

L-100. Although the algorithm provided only an approximate comparison, it proved invaluable in achieving first cut designs.

If the standard computer is chosen appropriately, the system solution will require a computer with significantly more power for the most demanding traffic case. If the standard is powerful enough to handle the most demanding case, a computer with less power should be chosen as the processor, or a uniprocessor solution should be considered.

Traffic Model

Next, a traffic model that relates the realtime processing requirements by major functions to the computing capabilities of the standard computer is developed. Each realtime function is analyzed to determine milliseconds of computing time per call. These estimates are based on sample programs written for key algorithms or analysis of existing similar systems.

The functions identified depend on the application. A typical breakout is among communications, applications, and file handling. Applications represent the major transactions of the system. In a banking system, this might be savings inquiries, deposits, withdrawals, etc. In the system example described here, the functions are all communications oriented: terminal processing, host processing, and trunk line processing.

After all major functions have been identified and calibrated, the rates at which the functions will be exercised must be quantified. If the system operates in a multisite environment, the rates for at least a representative range of sites must be identified.

Processor Model

A processor model is developed by analyzing the following functions.

Central Processor Utilization—Percentage of a standard computer required to process this function under peak load. This value does not include operating system overhead.

Online Memory Utilization—Online memory is measured in 8-bit bytes; it has three components: program size, table size, and buffer size (for storage of data in process).

File Utilization—Amount of time per second that the function uses an online file during peak load. This value is the product of accesses per function call, function calls per second, and service time per access.

Interfunction Communications—This function measures the amount of data in bits and number of messages sent per second to all other functions.

Central processor unit (CPU) utilization per function can be calculated by several methods. One approach is to write or flowchart a test program and, from that, estimate the number of instructions executed per call in terms of the standard computer. This estimate is multiplied by the number of times the function is executed per second and is divided by the instruction processing rate per second of the standard computer. For example, assume that a function executes 10 times/s and requires 5000 instructions/call. If the standard computer processes 350,000 instructions/s, CPU utilization is $(10)(5000)/(350{,}000) = 0.143$.

A second approach is to measure CPU utilization per call by executing a similar function on an existing processor (which may differ from the standard). Extrapolation is then performed to account for differences in the actual function and the actual processor. Both activities are presently more of an art than a science. Processor comparisons can be made by use of elaborate benchmarks or by hand calculations of the comparative running times of simple, but representative, programs. Functional comparison is usually made empirically, based on knowledge and experience.

Program size per function for online memory utilization can be estimated by comparing existing or similar programs or by roughly flowcharting the function. Separate estimates should be made for core- and disc-resident codes. Size of supporting tables can be estimated by comparison with previous efforts. Number of supporting buffers depends upon buffer size, message size, message arrival rate, and the average time a message is resident in the system.[1,2]

Data base accesses for file utilization are determined by estimating how many data records are required per function call, and what types of operations are necessary. For example, a read or write operation is one access; an update consists of two—one read and one write; and create record may take several accesses. In addition a factor must be calculated to account for indexing accesses; ie, those accesses required to find the desired record.

Service time for each access is the sum of the average seek time, rotational delay, and data transfer time. To be conservative, assume that all accesses require a new seek (for moving head systems). Overall disc utilization per function is given by the product of the number of accesses for the function and the average service time for each access.

Estimates of interfunction communications provide a basis for assessing the impact of placing different functions in different processors. The number of messages sent and received can create a significant interrupt load. The total bit rate of information sent and received determines what type of interprocessor communications network (ICN) is required.

First-Cut Centralized Design

CPU requirements for the centralized computer model follow directly from the previous analysis. For example, if the total realtime load is 5.7 s of CPU time/s of real time, a computer having at least six times the processing power of the standard is required, exclusive of background loads or executive overhead.

The next analysis involves memory size. Program size, table size, and buffer requirements must be totaled for each function. This process results in separate estimates for total main memory requirements and disc resident storage.

The final analysis results in a design for the data base files. These files must be sized and organized, and access methods must be determined. Realtime

factors relating to response time must be considered to ensure that the required access rates can be handled. Queuing theory calculations are then applied to ensure that the resulting first-cut design can support the system's response time requirements.

First-Cut Distributed Design

Centralized analysis provides a starting point for the distributed system design. Since power of the central computer is now known, it is possible to make a first estimate of how many standard processors are required in the MPS approach. The next step is to validate whether the class of computer represented by the standard computer is the proper choice for the MPS processor. The standard computer may prove either too powerful or not powerful enough. In either case, another standard that is more suitable to system operation should be selected and examined.

A major task of the distributed design process is assignment of functions to processors. To minimize cost, the goal is to create a balanced load between processors, and to balance memory size between processors. After a reasonable assignment of functions is made, interprocessor data flow must be analyzed. This flow creates two potential overhead problems: message interrupts in the processors and contention for the interprocessor communications network (ICN).

Loading on the ICN must be determined so that design criteria can be developed. Bandwidth of the ICN must be adequate to absorb peaks and to minimize transmission delays. Also, the ICN must contain redundancy to allow the system to function despite a single-point failure. ICN overhead may make it necessary to reassess the number of processors required for the job, reassign functions to reduce the load, or add processors to regain computing power that is lost because of communications overhead.

After functions have been reassigned, memory size for each processor can be estimated. Memory mapping must be explored to provide sufficient main memory size. If mapping is needed, system processing capability may degrade by as much as 5% to 20%, requiring additional processors to compensate for this loss of performance.

The next task is to determine how to handle the data base; ie, whether to have a single processor support file requests or to distribute that function over several processors.

Deciding how many spare processors are necessary to provide the redundancy necessary to satisfy availability requirements is the final task. This determination can be made with the aid of relatively simple reliability equations,[3] and consideration of the practical problems of error detection, fault isolation, and switchover. All of these tasks should be performed for each candidate architecture that is judged promising for the system application.

Analysis and Selection of a Detailed Design

Candidate architectures must be analyzed with respect to the following factors: cost-effectiveness, availability, reliability, response time, special hardware, development risks, software availability, modularity, and expandability. Several alternative methods exist for these determinations. One approach is to set acceptable levels in each performance category; the selected architecture meets all performance levels at the lowest cost. Another approach is to assign weights to each performance factor, as well as a weight for cost; the selected architecture is the one that aggregates the highest value.

A significant result of this analysis phase is development of the evaluation criteria. This task is difficult because it involves a combination of subjective and quantitative factors. However, extensive analytic tools, such as computer simulations, are not needed. Field experience has confirmed that simple reliability theory, queuing theory, and basic computing knowledge are sufficient to analyze MPS designs at this stage.[1,4,5]

Finally, the selected architecture is subjected to a detailed design review to detect flaws. If suspect, more detailed analysis studies are performed to validate the chosen design. This task may result in redistribution of functions to processors or change in the number of processors used. If changes are major, one or more of the other candidate architectures should be re-evaluated.

System Design Example

The MPS design methodology is illustrated using the configuration of a store and forward packet switch as

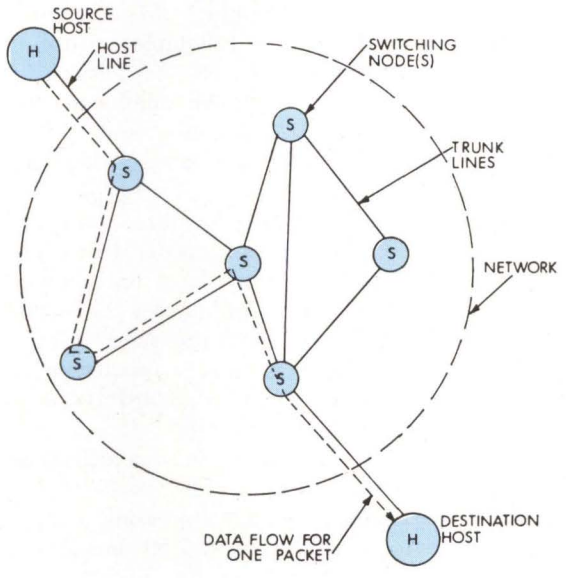

Fig 1 Packet switching network. This network type provides high speed, low delay mechanism for transmitting messages between host processors. Packets comprising message are transmitted independently across network, with successive packets taking different paths. Data enter network over host line. Messages may be in any code or format, with switches converting data to conform to network protocols

a system example.[2] The example is simplified for the purpose of clarity. Primarily, a packet switch transmits messages from an entry point to a destination point in a network (Fig 1). Each message is broken into subunits called packets, and each packet is transmitted independently through the network. Nodes (or switches) reassemble the packets in correct order to ensure proper delivery to their destination. Messages can be originated by terminal or host computers. Each switch processes data on three types of lines: trunk lines that interconnect switches, host lines that connect hosts to switches, and terminal lines that connect terminals to switches.

Detailed process flow for a particular switch (Fig 2) may be hard to define; trunk, host, and terminal requirements may be known only in the aggregate. However, field experience has shown that aggregate flow suffices for further analysis.[2] In Fig 2, N, H, and T represent the total full-duplex trunk, host, and terminal traffic flows, respectively, at a switch. For this example, assume that functional requirements of the system are those given in Table 2, and that traffic rates for the largest and smallest switches are as listed in Table 3. Assume that stated availability for a switch is 0.995; ie, the switch must be operational for 995 out of every 1000 h, and that the switch is to operate 7 days/wk, 24 h/day.

Basic System Requirements

Sizing information is provided for the packet switch in terms of an unidentified standard computer with a 1- to 2-μs instruction time.[2] Since the L-100 is in this class, it is assumed to be the standard computer for this example. For a packet size of 1000 bits and an average message size of 8000 bits,* this standard computer can support 475k-bit/s full-duplex trunk traffic, 160k-bit/s full-duplex host traffic, or 26k-bit/s full-duplex terminal traffic. Using these numbers, core size estimates based on field experience and established traffic rates (Table 3) yield the packet switch processing model defined in Table 4.

CPU utilization is calculated in three parts—trunk, host, and terminal processing. Consider trunk processing. From Table 3, if all trunk lines are transmitting data at full capacity, total full-duplex bandwidth is 1400k bits/s. Since the standard processor will process 475k bits/s of full-duplex traffic, a processor almost three times as powerful as the standard is needed to handle the load (1400/475 = 2.95). If a distributed system is implemented, at least three standard processors are required to handle the trunk load.

Similarly, host and terminal processing capabilities are determined to be 250/160 = 1.50 and 240/26 = 9.23, respectively. Because there are no external files in this packet switch, the processing model does not reflect disc accesses.

This system design assumes a 10% overhead for common (executive) processing. Table 4 indicates that a single processor with 15.05 times the power of the standard and 351.4k bytes of main memory can handle the processing load generated by all lines transmitting data at 100% capacity at a large switch. Data for the smallest switch (node) indicate that a processor 2.64 times as powerful as the standard with main memory of 146k bytes can support full line load input.

These results indicate a potential problem with a uniprocessor approach. The selected processor must possess a wide dynamic range that reasonably fits at both ends of the large to small switching spectrum, demanding a maximum processing capability of ap-

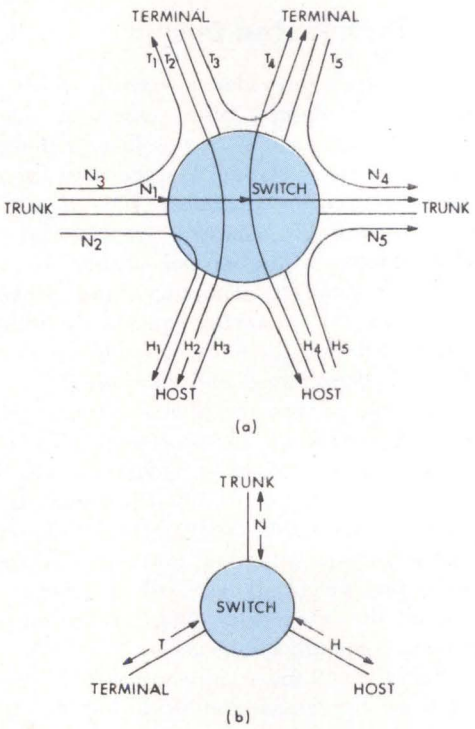

Fig 2 Switch data flow. Switch (a) supports variety of individual data flows. Data arriving on trunk may flow to another trunk (N_1), to local host (N_2), or to local terminal (N_3). Similar 3-way split exists for locally generated terminal traffic (T_2, T_3, and T_5), and locally generated host traffic (H_3, H_4, and H_5). In aggregate flow model (b) trunk flow (N) is associated with data arriving on one trunk line and exiting on another; associated processing is primarily involved with packet routing. Host flow (H) is associated with processing of packets to and from hosts, and terminal flow (T) with processing packets to and from terminals

*Details that justify these numbers are omitted for simplicity. Readers who are interested in packet switching applications should consult Ref 2.

proximately 6 x 10^6 instructions/s.** This analysis implies a single centralized processor in the UNIVAC 1100 category. In addition, because of reliability, two processors are needed at each site.

Distributed System Approaches

Two MPS approaches depicted in Fig 3 are explored: dedicated function and traffic sharing. In the former, subsets of functions are allotted to particular processors, which are dedicated to these functions. In the latter, each processor handles all functions, but system traffic is divided between processors. Each approach is analyzed for both a large and a small switch.

TABLE 2

Packet Switch System Functions

Trunk (N) Processing—Receive packet on trunk line; determine its destination; ie, host, terminal, or trunk line; and ship packet to destination

Host (H) Processing—Receive input data from host; format in packet; and transmit to trunk processing; or receive host data from trunk processing; format for transmission to host; and transmit to host

Terminal (T) Processing—Receive characters from terminal, format into host protocol, perform host processing, and transmit to trunk processors; or receive data from trunk processing, perform host processing, format for terminal, and transmit to terminal

Common Functions—Executive, input/output, and support functions, common to all functions, include error checking and routing table updates

TABLE 3

Packet Switch Traffic Rates

Type	Rate (kilobits/s)	No. of Lines	Total Traffic (kilobits/s)
Largest Switch			
Trunk (N)	56	25	1400*
Host (H)	9.6	25	240
Terminal (T)	4.8	50	240
			1880
Smallest Switch			
Trunk (N)	56	10	560
Host (H)	9.6	5	48
Terminal (T)	4.8	5	24
			632

*For full-duplex traffic, 1400 means 1400k bits/s into processor and 1400k bits/s out of processor. All traffic rates in this example are full duplex.

Dedicated Function Approach/Large Switch

A number of processors are dedicated to trunk processing, others to host processing, and still others to terminal processing. These processors are connected to the appropriate communication lines and to each other; spares are included for reliability. Data arriving on a trunk, host, or terminal line are routed by trunk, terminal, or host processor, respectively, for output to a destination. Each processor has sufficient routing information to control these data transfers. If a processor fails, it is replaced by a spare processor (SP in Fig 3). One processor can be designated as the control processor and supplied with a local file containing a copy of all programs.

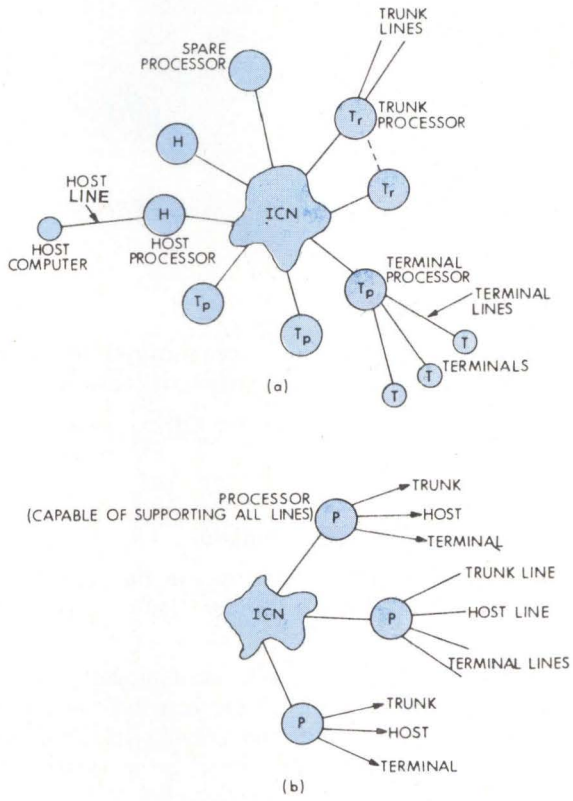

Fig 3 MPS distributed architectures. In dedicated function MPS (a), all processors are dedicated to specific functions; none is capable of supporting all functions. Processors communicate with each other via interprocessor communications network (ICN). Spare processor (SP) backs up failed processor. In traffic sharing MPS (b), each processor can support all functions for portion of traffic. Subset of trunk, host, and terminal lines is attached to each processor

**The standard processor is capable of 10^6 machine cycles/s. Assuming 2.5 cycles/instruction, the processor can support 400k instructions/s. The required processor must be 15 times as powerful; hence, it must be capable of processing 6 x 10^6 instructions/s.

TABLE 4

Packet Switch Processing Models

Processing Function	Basic Processing CPU Utilization (Computed to Standard)	Program (P) Size (kilobytes)	Table (T) Size (kilobytes)	Buffer (B) Size (kilobytes)	Total Memory (kilobytes)
Largest Switch					
Trunk (N)	2.95	8	2.8	28	38.8
Host (H)	1.50	24	14.6	64	102.6
Terminal (T)	9.23	30	14.0	123	163
Common	(10% of processing or 1.37)	40	2.0	0	42
	15.05	102	34.4	215	351.4
Smallest Switch					
Trunk (N)	1.18	8	1	11	20
Host (H)	0.30	24	3	13	40
Terminal (T)	0.92	30	2	12	44
Common	(10% or 0.24)	40	2	0	42
	2.64	102	8	36	146

Trunk Processing

How many trunk processors are required to support the throughput of the large switch is determined by

$$NP = \frac{(BP) \times (HF) \times (EO) \times (MF) + I/O}{MU} \quad (1)$$

where

NP = Number of processors required

BP = Basic processing required for the function as determined from Table 4 (for trunk processing, BP = 2.95)

HF = "Hopping" factor which accommodates the fact that each packet originating on a trunk line could appear in two processors: one serving its input line, the other serving its output line. In a system with many processors, this factor approaches 2.0

EO = Executive overhead; for a packet switch with a tightly written executive, this number is assumed to be 1.1, ie, 10% overhead

MF = Mapping factor which accounts for memory cycles lost if a memory map is used. In this example, a factor of 1.1 is used if main memory requirements for a processor exceed 64k bytes. If not, a factor of 1.0 is used

I/O = I/O load factor which accounts for loss of memory cycles due to I/O transfers, including cycle stealing and interrupt processing

MU = Memory utilization factor to accommodate maximum allowable CPU utilization under full load. In this system example, 0.9 is used; ie, CPU must be less than 90% utilized at full line utilization.

All equation factors are known except for I/O. In this system example, I/O is caused entirely by packet transfers. Each packet that enters or leaves a processor creates one interrupt and causes cycle stealing. Assuming that 100 cycles are used by the interrupt, that each packet is 1000 bits in length, and that one memory cycle is lost for each 16-bit word, 63 cycles are lost due to direct memory accesses, for a total of 163 cycles. To be conservative, this number is rounded up to 200 cycles/packet transfer. Since the standard computer provides 10^6 cycles/s, each packet transfer requires 0.0002 standard processors.

Based on known factors Eq (1) can be reduced to

$$NP = \frac{(BP)\ (2)\ (1.1)\ (MF) + (MF) + PS\ (0.0002)}{0.9} \quad (2)$$

where

PS = Number of packets per second in and out of the trunk processors calculated from trunk traffic data (Table 3). Total input trunk rate is 1400k bits/s, which represents 1400 packets/s entering the system. Each packet enters one processor via a communications line, exits that processor on the ICN, enters another trunk processor, and exits that processor via a communications line. Therefore, PS is four times the packet entry rate, giving a total of 5600 packets/s.

To determine MF in Eq (1), memory size (MS) requirements for each trunk processor must be calculated using the following equation:

$$MS = CP + CT + FP + \frac{HF(FT + FB)}{NP} \quad (3)$$

where

MS = Memory size of processor in kilobytes

CP = Size of common program in kilobytes

CT = Size of common tables in kilobytes

FP = Size of functional program in kilobytes

FB = Size of buffers for function in kilobytes

FT = Size of tables for function in kilobytes

NP = Number of functional processors

HF = Hopping factor

Eq (3) reduces the buffer and table storage per processor by a factor NP to account for the distribution of load across NP processors. All factors except NP can be obtained from Table 4. To find NP, calculate Eq (2) assuming that MF = 1; ie, no memory mapping required. This gives

$$NP = \frac{(2.95)\ (2)\ (1.1)\ (1)\ +\ 5600\ (0.0002)}{0.9} = 8.46 \qquad (4)$$

Therefore, nine trunk processors are required, excluding the potential for memory mapping, and memory requirements can be determined from Eq (3).

$$MS = 40 + 2 + 8 + \frac{2(2.8 + 28)}{9} = 56.8\text{k bytes}$$

To ensure a margin for growth, 10% spare memory capacity is provided for host processing and for all subsequent memory calculations. 56.8 (1.1) = 62.48k bytes. Memory is assigned in 32k-byte increments; therefore, a 64k-byte processor is adequate. Since MF = 1, the previous calculation of NP is correct. Consequently, nine 64k-byte processors will support trunk processing.

Host Processing

The number and memory size of host processors are determined in a similar manner. Eq (1) is used as the basis for calculating the number of host processors with some modifications. It is assumed that each host packet will be processed only once by a host processor, ie, there will be no host to host traffic within a switch. Therefore, HF = 1.0 for host processing. From Table 4, BP is 1.50.

Each packet creates two interrupts: one when it enters the host processor and one when it leaves. Each interrupt takes 200 cycles of CPU time as is the case for trunk processing. Therefore, each packet transfer utilizes 0.0002 standard processors. The number of packets in and out is twice the full-duplex traffic rate divided by the packet size (1000 bits). Full-duplex host traffic is 240k bits/s (Table 3). Therefore,

$$I/O = \frac{2(0.0002)\ (2)\ (240 \times 10^3)}{1000} = 0.192 \qquad (5)$$

Inspection of Table 4 shows that the combination of host and common programs sizes exclusive of buffers and tables requires 64k bytes. Hence, processors greater than 64k bytes will be required, and, an MF of 1.1 is used. Substituting all factors into Eq (1) gives

$$NP = \frac{(1.5)\ (1)\ (1.1)\ (1.1)\ +\ 0.192}{0.9} = 2.23 \qquad (6)$$

revealing the need for three host processors.

Memory size can be calculated from Eq (3), using the factors given in Table 4 for common and host processing, resulting in

$$MS = 40 + 2 + 24 + \frac{(14.6 + 64)}{3} = 92.2\text{k bytes} \qquad (7)$$

To provide room for growth, a 128k-byte host processor is recommended since processor sizes are allocated in terms of 32k-byte increments.

Terminal Processing

Eq (1) is also used to determine the number of terminal processors. From Table 4, BP = 9.23. HF = 1.0 because a terminal packet is processed by only one terminal processor. The I/O factor is calculated in a manner similar to that described for host processing. Each packet in and out of a terminal processor creates two packet transfers, each utilizing 0.0002 standard processors. Since the full-duplex terminal load is 240k bits/s (Table 3) and each packet is 1000 bits, I/O = 0.192, as shown in Eq (5).

Processors with memories greater than 64k bytes will be required, since program size alone is equal to 70k bytes (Table 4). Therefore, MF = 1.1. Substituting all factors into Eq (1) gives

$$NP = \frac{(9.23)\ (1)\ (1.1)\ (1.1)\ +\ 0.192}{0.9} = 12.6 \qquad (8)$$

Therefore, 13 terminal processors are required.

Size of each processor's memory is calculated by substituting the values of Table 4 into Eq (3), with NP = 13. This gives

$$MS = 40 + 2 + 30 + \frac{(15 + 123)}{13} = 82.6\text{k bytes} \qquad (9)$$

Recommended terminal processor size is 96k bytes, allowing space for expansion purposes.

ICN Processing

Next ICN requirements are determined. In the worst case, all trunk, terminal, and host traffic will be transmitted through the ICN (Fig 4). Aggregate rate is 1880k bits/s, representing a rate of 118k 16-bit words/s. Required bandwidth is given by

$$BW = \frac{(AR)\ (OH)}{(ML)} \qquad (10)$$

where

AR = Aggregate ICN rate in words/s

OH = ICN overhead

ML = Maximum loading on link

Assuming 50% overhead (ie, OH = 1.5) and ML = 0.5, then

$$BW = \frac{(118K)\ (1.5)}{0.5} = 354\text{k words/s}$$

Factor ML is kept at 0.5 to prevent excessive waiting time for a processor that needs access to the ICN. The ICN can be developed by several methods (see "Multiple Processor Minicomputer Systems—Part 1: Design Concepts," *Computer Design*, Oct 1978, pp 87-95). Because of high bandwidth and point-to-point com-

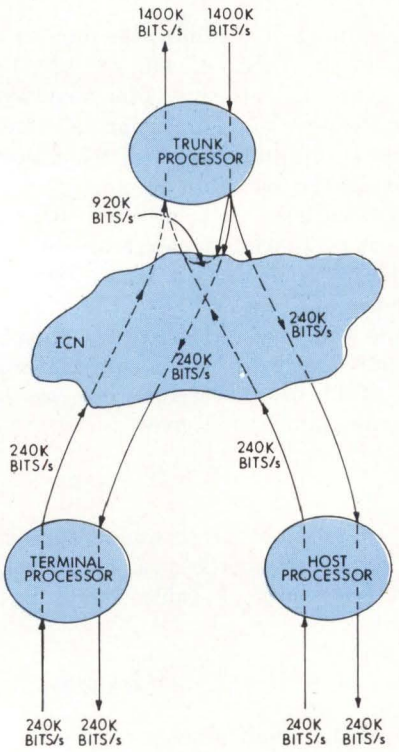

Fig 4 Worst case ICN load for large switch. Traffic flow model assumes that all trunk, terminal, and host lines are fully loaded. Incoming trunk packet data flow (1400k bits/s) is split three ways: 240k for local host processing, 240k for local terminal processing, and 920k bits/s for output on trunk lines. All data are assumed to be transmitted on the ICN. Total ICN data load is 920k + 240k + 240k + 240k + 240k = 1880k bits/s. To this value must be added overhead traffic necessary to ensure reliable traffic flow. If each packet is 1000 bits long, terminal processing generates 4 x 240 = 960 packets/s, host processing generates 4 x 240 = 960 packets/s, and trunk processing generates 4 x 1400 = 5600 packets/s; a total of 7520 packets/s. Each transfer creates 200-cycle/s processing load; therefore total load is 1.504 x 10^6 cycles, equivalent to processing power of 1.5 standard computers

munications requirements, a shared bus approach seems effective. Such buses can be built economically to handle 10^6 16-bit word/s rates, easily satisfying the above requirements.

Final Processing Design/Large Switch

For reliability, dual buses are used for data transfer in the completed system design (Fig 5). Twenty-five operational processors are required, ranging in size from 64k to 128k bytes. Note that communication lines cannot be evenly distributed between processors. Trunk processors can handle either two or three lines, but processors that support three lines will be more heavily loaded. These processors must be analyzed to determine if the 0.9 CPU loading constraint is violated. In this case, the 3-line trunk processor will be loaded at 0.92*; this is close enough to the stated goal of 0.9 CPU utilization. Similar investigations of host and terminal processors indicate that their CPU loadings are satisfactory. With this large number of processors, spares must be provided to ensure that the overall system availability goal of 0.995 is achieved. If each processor is assumed to have an availability of 0.99 (a reasonable number for a minicomputer), then the number of spares can be calculated.[3] If one spare is used, then N − 1 out of N processors must work, as follows:

$$a = a_1^N + Na_1^{N-1}(1 - a_1) \quad (12)$$

where

a = System availability

N = Total number of processors including spares

a_1 = Availability of one processor

Substituting $N = 26$ and $a_1 = 0.99$ into the equation gives $a = 0.978$. This value does not meet the stated availability goal of 0.99. If two spares are used, then:

$$a = a_1^N + Na_1^{N-1}(1 - a_1) + \frac{N(N-1)\,a_1^{N-2}(1 - a_1)^2}{2} \quad (13)$$

When $N = 27$, Eq (13) gives $a = 9.998$, which exceeds the availability requirement. Hence, two spares are used; each is configured with 128k bytes of memory so that it can take over any function. One spare is configured with discs to store programs for all system processors and to keep backup records of system status and routing tables. This spare processor is controlled from a console by a system operator, who can

*This loading is derived from the fact that the processor is handling 3/25 of the total trunk load (3 of 25 lines). A previous calculation showed NP = 8.46 at 90% loading for trunk processors. Therefore, full load would be 8.46 (0.9) = 7.614. Dividing across nine processors gives 0.846 loading/processor on a uniform basis. Uniform loading implies 25/9 = 2.78 lines/processor. Hence, 3-line processors would have a loading of 0.846 (3/2.78) = 0.92.

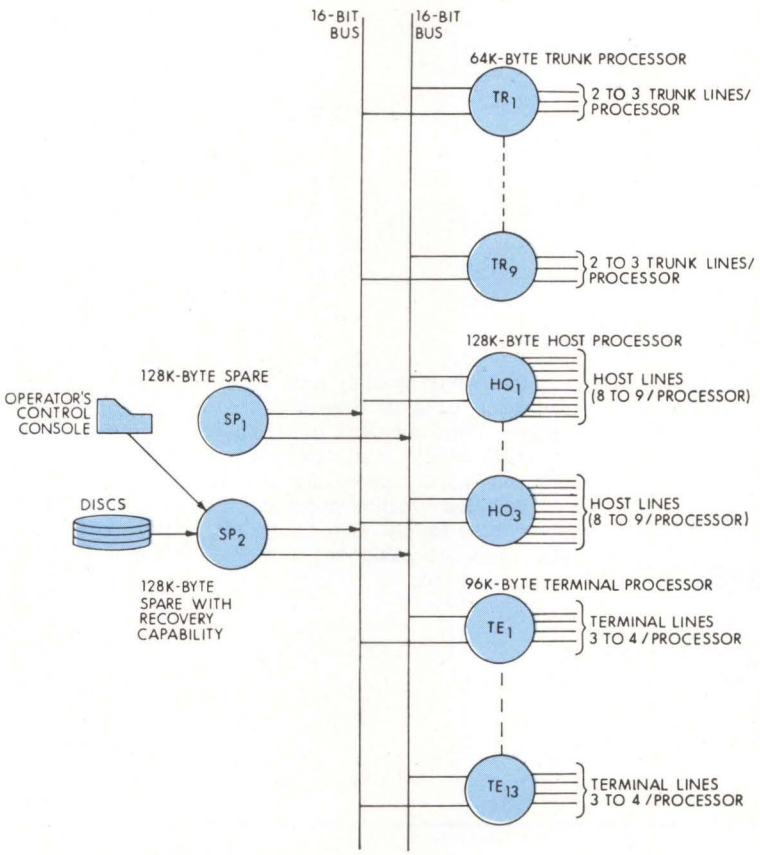

Fig 5 Large switch dedicated function architecture. Network uses 25 operational processors, plus two spares. Total memory requirement including spare is 2464k bytes. Dual buses are used, requiring 54 bus interfaces. No processor is more than 92% loaded under full input. Number of lines is divided as evenly as possible within functionally equivalent processors. Spare processor SP2 is equipped with control console and discs, and monitors status of all other processors. If failure is detected, SP2 will load spare processor SP1 with failed processor's program, reinitialize system to incorporate new processor, and isolate failed processor. Switching mechanism is required to attach failed processor's lines to spare

command a reconfiguration. A faulty module can be detected by other processors by means of error-check messages. Faulty responses can be transmitted to the spare control processor for printout on the system console.

Traffic Sharing Approach/Large Switch

An alternative distributed approach to the design of the large switch is to divide the processing load by traffic [Fig 3(b)]. Each processor performs all functions for a subset of the traffic. The total number of processors can be calculated from Eq (1), by adding all contributions from host, trunk, and terminal processing. In a traffic sharing approach, all processors will handle greater than 64k bytes because each processor will contain a copy of the total program; therefore, the mapping factor is 1.1. I/O processing can be assumed to be the same as in the dedicated function approach because all packets will be assumed to be moved between two processors. Solving Eq (1) for each function and summing across all functions yields

$$\begin{aligned} \text{NP (total)} &= \text{NP (trunk)} + \text{NP (host)} + \text{NP (terminal)} \\ &= 9.18 + 2.23 + 12.6 = 24.01 \end{aligned} \tag{14}$$

NP (host) and NP (terminal) are the same as they are for the dedicated function approach. NP (trunk) is larger because of the mapping factor. Note that 24 processors are required for the traffic sharing approach. Memory (M) requirements in kilobytes can be calculated from

$$M = P + CT + \frac{(B + T - CT + Btr + Ttr)}{NP} \tag{15}$$

where

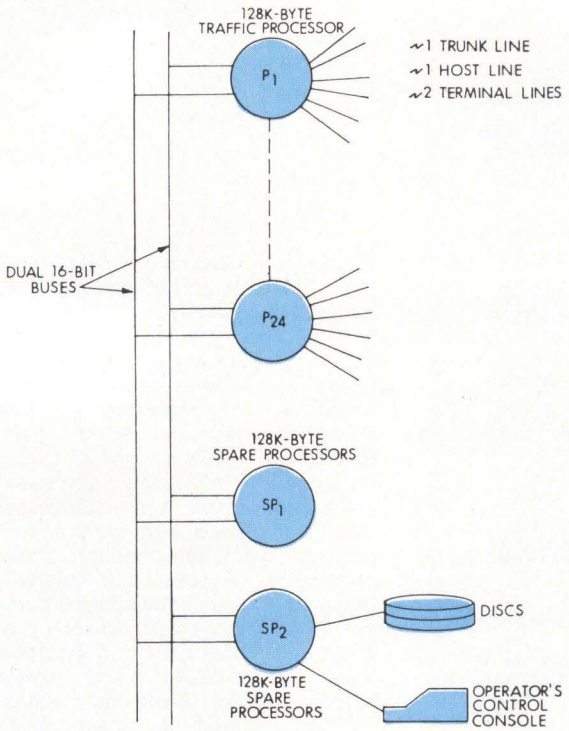

Fig 6 Traffic sharing architecture for large switch. Approach uses 24 operational processors, plus two spares. Total memory requirement including spares is 3328k bytes. Dual buses are used, requiring 52 bus interfaces. Spares are utilized similarly to those in dedicated function approach. Each processor supports three to five lines, for trunks, hosts, and terminals. Lines are assigned to evenly distribute load on each processor

P = Total program size
CT = Common table size
B = Total buffer size
T = Total table size
Btr = Trunk buffer size
Ttr = Trunk table size
NP = Number of processors

Trunk tables and buffers are included twice in Eq (15) to account for trunk packet hopping; ie, each trunk packet is processed in two processors. Substituting parameters from Table 4 into Eq (15) gives

$$M = 102 + 2 + \frac{(215) + 34.4 - 2 + 28 + 2.8)}{24} = 116\text{k bytes} \quad (16)$$

Thus, recommended processor memory size is 128k bytes.

For reliability, two spare processors are included, yielding a total of 26 processors for the traffic sharing approach. ICN requirements are similar to those for the dedicated function approach. Therefore, two 10^6-word/s shared buses are used to obtain the system configuration shown in Fig 6. Lines cannot be uniformly distributed between the processors; some processors will support four lines, a few will support five. Assignment of lines will have to distribute the load evenly to ensure that no processor is excessively loaded.

Small Switch Design

With regard to designing small switches,* both the dedicated function approach and the traffic sharing approach are modular in a cost-effective manner. By utilizing data from Table 4 and the same equations described for the large switch design, the number of processors required for the dedicated function approach to designing a small switch is four trunk at 64k bytes each, one host at 96k bytes, and two terminal at 96k bytes each. One spare processor at 96k bytes is adequate for system availability. The same ICN specified for the large switch can be used for the small switch.

*Interested readers may obtain detailed design data for the small switch by writing to: Editor, *Computer Design* magazine, 11 Goldsmith St, Littleton, MA 01460.

TABLE 5

Hardware Cost Comparisons of MPS Approaches

Item	Cost/Item*	Number Used In Dedicated Function Approach		Number Used In Traffic Sharing Approach	
		Large Switch	Small Switch	Large Switch	Small Switch
Processors	$5000	27	8	26	7
Memory Maps	1000	18	4	26	7
Memory (kilobytes)	100	2464	640	3328	896
Interconnects	2000	54	16	52	14
Total Cost**		$507,400	$140,000	$592,800	$159,600

*Estimated cost for dual mainframe in Univac 1100 class is $3,000,000
**Exclusive of peripherals

For the traffic sharing approach to small switch design, a total of six processors is required at 128k bytes each. One spare processor at 128k bytes is needed for system availability.

System Comparisons

Table 5 compares hardware costs of the MPS approaches discussed to a centralized mainframe approach using a backup machine. All approaches are comparable in performance and reliability. However, MPS approaches are less costly than the centralized approach, and are more expandable if increased requirements have to be integrated at a later date. MPS cost advantages are even greater for the low end switch. The modularity of MPS also proves attractive, compared to the centralized approach. The large switch processes 1880k bits/s of data, the small switch 632k bits/s (Table 3); the ratio between these two loads is 2.97. Hardware cost of the large dedicated function switch is 3.6 times that of the small switch; cost of hardware for the large traffic sharing switch is 3.7 times that of the small switch (Table 5). From this first-level comparison, both MPS approaches are concluded to be superior to the mainframe.

The next level of analysis is to determine which of the two MPS architectures should be chosen. If hardware cost is the main criterion, then the dedicated function MPS approach is more economical. However, other factors may influence the decision, including software cost, development time, development risk, previous experience, maintenance, and expandability. For this discussion, assuming that hardware cost is the dominant design decision factor, the dedicated function MPS approach is selected as the candidate system architecture.

Summary

A systematic approach to MPS design is essential to ensure a cost-effective solution. A design methodology is described that allows alternative MPS architectures to be compared with each other and with a centralized mainframe approach. In this methodology, a level of performance is specified. Alternate systems are designed, and then all systems are compared for cost. The system example, although simplified, provides a basis for understanding the elements of the methodology. However, extensive refinement of the process is still required to custom fit a particular application.

The system also illustrates the potential advantages of an MPS over a centralized approach in a demanding real-time application; two of the most important advantages are cost-effectiveness and modularity. Many MPS applications fulfill the basic characteristics of a packet switch—high reliability, expandability, high throughput, and fast response time—and should increase significantly in other data processing areas as the decreasing cost of computing creates a viable climate.

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APPLICATION NOTE

Applying Magnetic Circuit Breakers in Digital Circuits

Adequate dc current protection for the complete spectrum of electronic applications can be supplied by magnetic circuit breakers, provided the breakers are properly specified and applied

Donald S. Tall Airpax Electronics, Cambridge, Maryland

Most electronic equipment cannot distinguish between normal loads and overloads; they simply draw current to meet load demand. However, when properly specified and applied, magnetic circuit protectors provide low cost automatic protection for such equipment, including computers and related peripherals. That these magnetic protectors also double as integral on/off switches provides added benefits of power switching and circuit control in a single device.

The most versatile and reliable breaker responds primarily to current (electromagnetic) rather than to a secondary effect, such as heat. A magnetic breaker is, in effect, an electromagnetic coil and armature device that opens a set of contacts quickly to protect the circuit whenever current exceeds a predetermined value. This occurs because the current in the coil generates sufficient magnetic flux to attract the armature.

Circuit Protector Types

Magnetic circuit protectors offer a multiplicity of configurations, including series, shunt, and relay trip, with a wide choice of time delays and electrical ratings. Multipole protectors, auxiliary alarm switches, and dual coil versions are typical variations of the main protector concept.

The universally applied series trip configuration (Fig 1) has its sensing coil and contacts in series with the load being protected to provide conventional overcurrent protection. With protectors that double as on/off switches, handle positions conveniently indicate circuit status. Adding an auxiliary switch (Fig 2), operated by

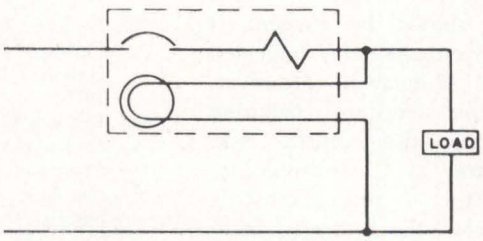

Fig 1 Series trip configuration. Circuit protector combines on/off and pilot lamp to provide overcurrent protection

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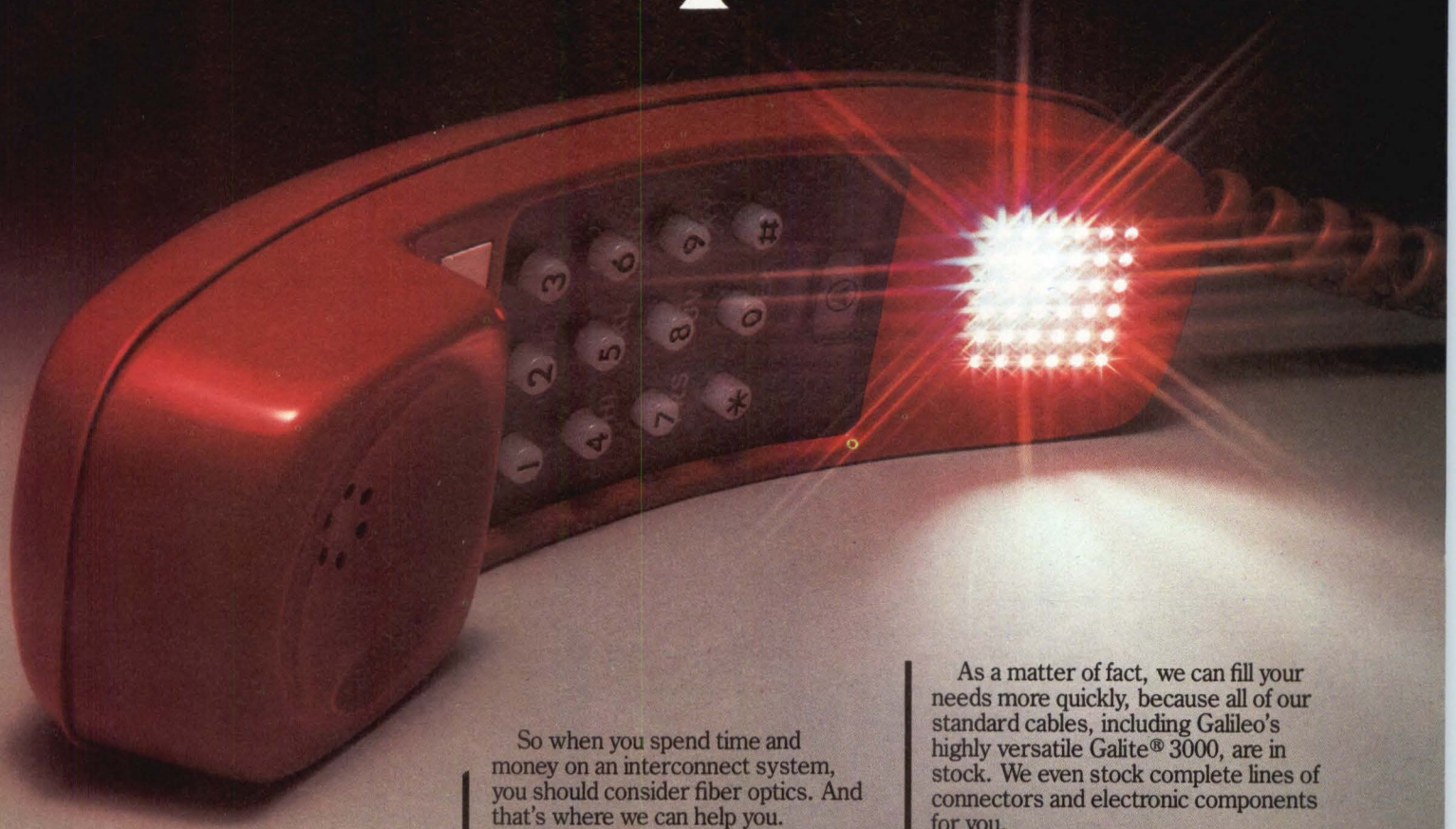

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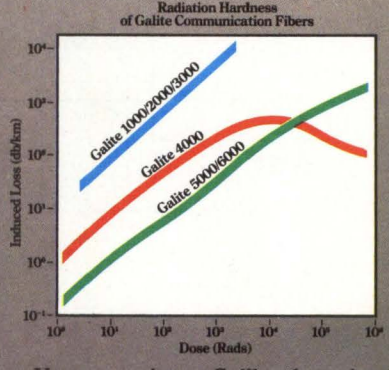

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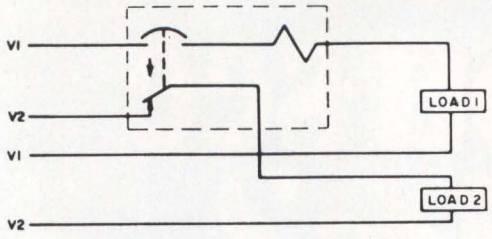

Fig 2 Remote location series trip type. Auxiliary contacts permit remote indication of protector operation

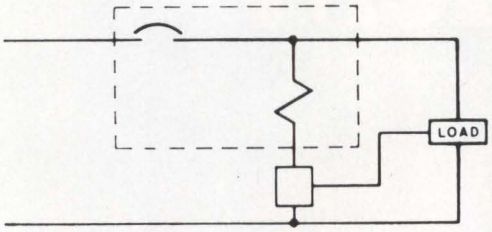

Fig 3 Shunt trip configuration. This circuit breaker acts as on-off switch and externally controls automatic shutdown device

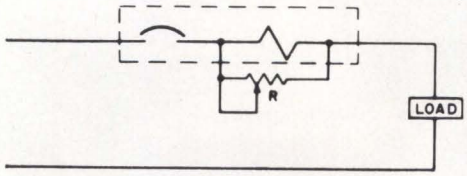

Fig 4 Adjustable shunt trip circuit breaker. This configuration can be closely trip adjusted by varying R; that resistor can be programmed to provide changes in trip point, as required, by sequencing changes in load

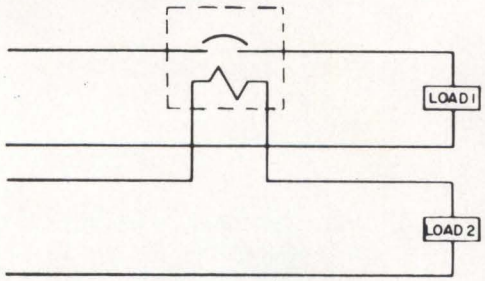

Fig 5 Relay trip type. With actuating coil and contacts internally isolated, protector senses overcurrent condition in load 2 and opens circuit to load 1. Both circuits could be opened, if desired, by using one series and one relay type in dual combination

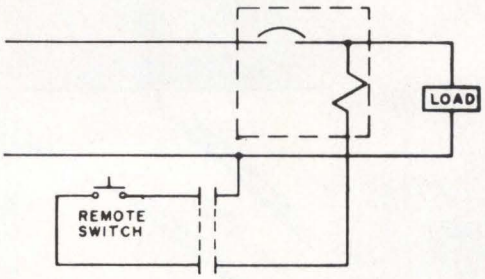

Fig 6 Remote shunt trip circuit breaker. This type acts as on-off switch for load with provision for remote turn-off capability. It is used where remote shutdown may be necessary in emergency situations

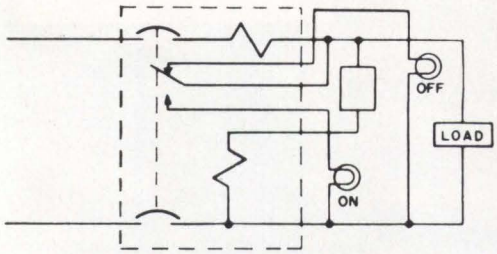

Fig 7 Multipole protector. Combination series and shunt type protector in multipole combination is used with additional circuitry to provide both overcurrent and overvoltage protection. Auxiliary switch contacts provide operation of external on-off lamps to indicate protector condition

an internal mechanism, provides trip indication at a remote location.

Shunt trip configurations (Fig 3) are applied primarily for control of multiple loads. Basically, a third connection is brought out from the internal coil contact junction to a third terminal, often referred to as a calibrating tap. This permits use of a shunt across the trip coil that, if made adjustable (Fig 4), can be used to accurately calibrate the trip level.

On relay trip types, coil contact leads are brought out to separate pairs of terminals (Fig 5). This configuration permits the overload sensing coil to be placed in a circuit that is electrically isolated from the trip contacts. The coil may be actuated by process control or monitoring sensors such as pressure, flow, temperature, and speed. Other typical applications include crowbar, interlock, and emergency/rapid shutdown circuitry (Figs 3 and 6). A trip can be accomplished by either voltage or current.

Two or more basic protectors may be combined in a multipole assembly with the actuating handles linked and the trip mechanisms internally coupled (Fig 7). A fault in any protected circuit opens all poles simultaneously. These protectors are applied in 2-wire or multiphase circuits, or in related but electrically isolated circuits. A mix of delays, ratings, and configurations is possible, providing an almost limitless number of combinations. The handle connecting rod may be removed in some devices to permit independent on/off switching while maintaining the common trip capability.

Combining two electrically independent coils in one common magnetic circuit provides contact opening when either an overcurrent or a trip voltage is applied to the respective coils (Fig 8). The current trip coil has standard specifications, while the auxiliary coil provides a control function to permit contact opening from a remote interlock or other transducer function.

Auxiliary switches, voltage trip versions, voltage protectors, and switch-only protectors are additional types available. One form of auxiliary switch enables remote indication of electrical overloads (Figs 5 and 9). It operates one lamp to indicate circuit "safe," and another lamp (not shown) to indicate circuit "unsafe."

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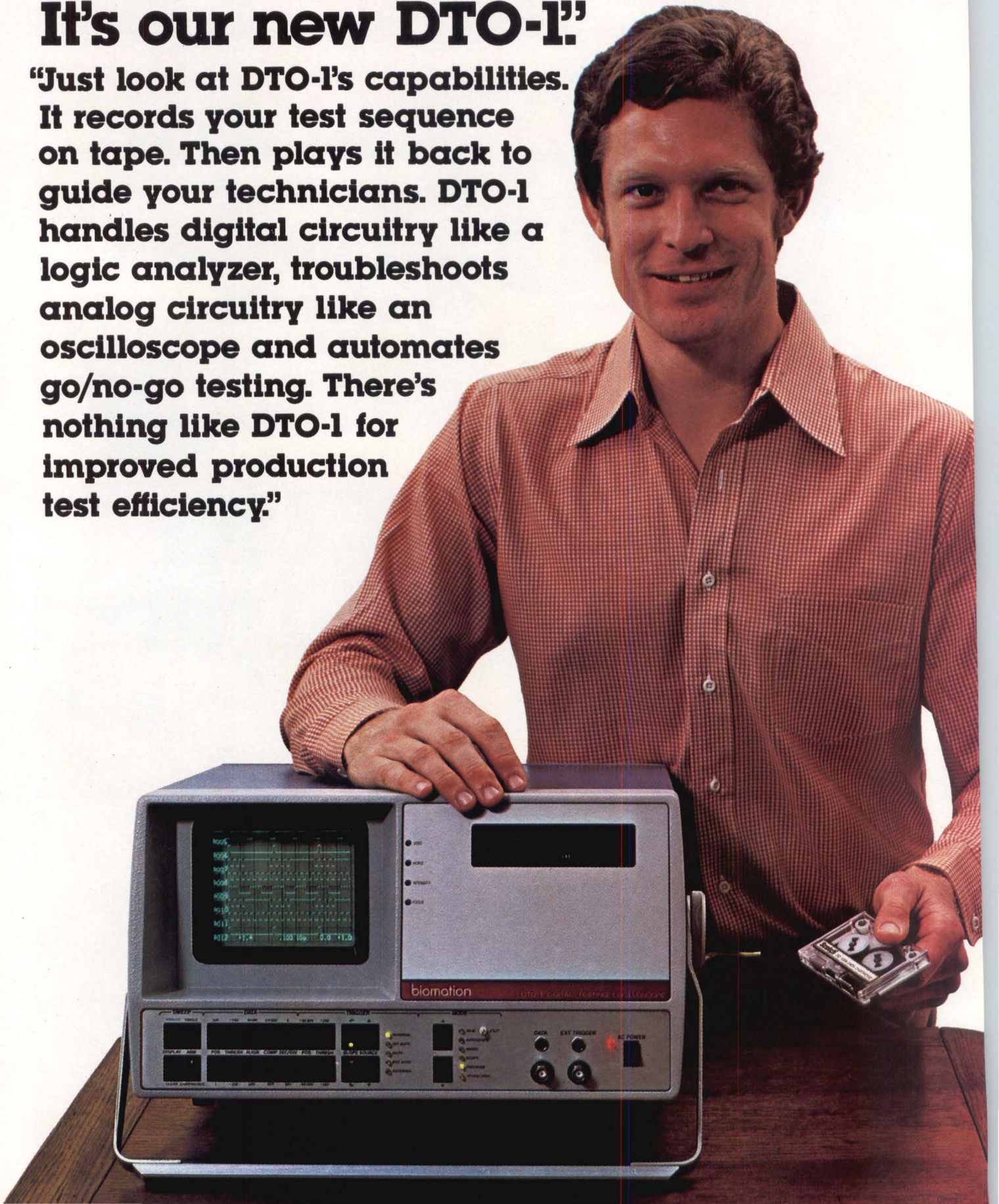

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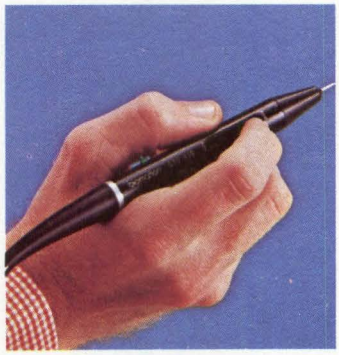
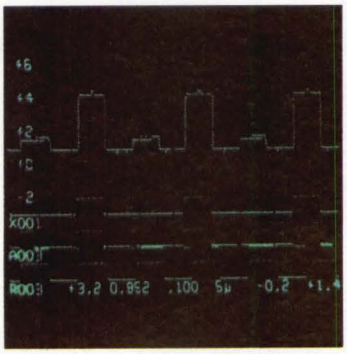
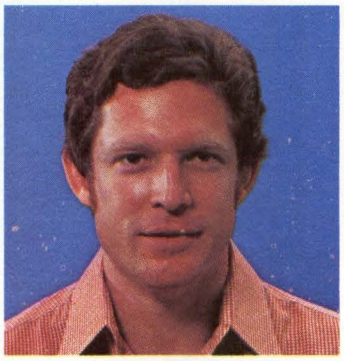


Speeds and simplifies trouble-shooting, too. When a fault is detected, the probe's red light alerts the technician to check DTO-1's built-in scope. There he has the diagnostic capability to pinpoint both digital and analog faults. Like a logic analyzer, DTO-1 displays time domain logic traces, comparing the test trace with the reference trace and highlighting any disagreement. Analog waveforms can be simultaneously displayed with logic traces, on the same time base.



That makes it easy for the troubleshooter to determine if the malfunction is digital or analog. Result: Quick, positive fault isolation.



Technicians love DTO-1. Finding, training and keeping test technicians is a growing, costly problem. DTO-1 is the answer. It practically trains technicians for you, using your recorded test programs to control the test sequence. It automatically aligns itself to the frequency of the system under test, is self-calibrating and includes built-in diagnostics. DTO-1 frees your technicians from the repetitious routine of product test, and lets them concentrate on finding and fixing malfunctions.

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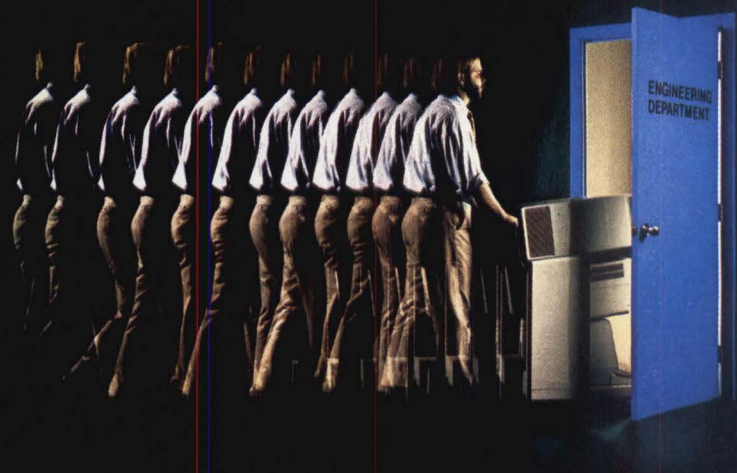
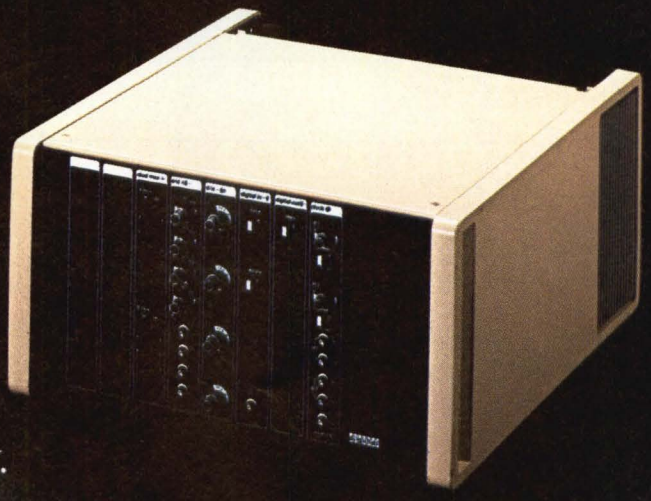


MINC



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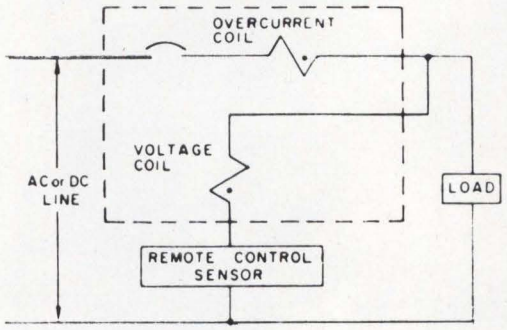

Fig 8 Dual coil protector. Contacts open when current exceeds 125% or more, or when voltage is applied to voltage coil by remote control sensor. Process control sensor can be in one or many locations. Voltage coil can also be used as emergency pushbutton for power removal from one or more remote locations.

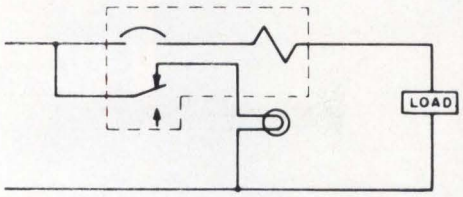

Fig 9 Remote overload indicators. For type-RS auxiliary alarm switch, lamp indicates only for electrical trip of main contacts. For -RE or -RO type auxiliary switch, lamp indicates circuit condition regardless of how main contacts are opened (manual or electrical trip)

Most protectors can be supplied for voltage trip applications, sometimes called "dump circuits" or "panic trip circuits." Basically, these protectors open main power contacts with low power inputs from one or more sources.

Undervoltage protectors prohibit contact closure in the absence of dc voltage. These devices will also trip open in the event that voltage drops below 40% of rated voltage. By combining an undervoltage function with an overcurrent function, it is possible to protect equipment from both malfunctions. A bridge arrangement is required for ac operation. Such protectors may also be used as on/off power switches. When no overcurrent protection is needed, the coil mechanism is deleted, providing a low cost single-pole or multipole power switch.

Time Delay Types

A time delayed operation for circuit protectors is necessary for many industrial applications to assure uninterrupted but safe operation. The delay should be long enough to allow nonharmful transients of current to pass without nuisance tripping, yet be fast enough to open the circuit to protect the system, when necessary. When specifying delay, all operating conditions must be evaluated because changes in application could shift protection emphasis.

Instantaneous—trips in milliseconds, usually under 100, with most at approximately 15. Such delays are used for sensitive circuits where low overloads of short duration could be harmful, such as solid-state or passive circuitry where inrush currents or transient spikes are present and cannot be tolerated. Applications vary. Where the lesser of two voltage drops makes the difference, such as in low voltage logic circuits, protectors with approximately zero delay have significantly lower terminal-to-terminal resistance than others. This results in reduced voltage drop across the circuit protector.

Fast—trips in seconds, usually 1 to 10. They are used for most dc and electronic applications where temporary overloads of over 200% cannot be tolerated for more than a few seconds.

Slow—trips in 10 to 100 s. These delays allow turn-on transients to pass without tripping for most large transformer coupled loads, where overloads of several seconds in duration can be tolerated without damage.

Very Slow—trips in 100 s or more. Such delays are mostly used in motor starting applications to protect wiring. A limited overload usually will not cause damage.

Summary

When choosing a magnetic circuit breaker, all parameters of the particular application must be known and evaluated. Factors such as electrical ratings, environment, shock, vibration, moisture resistance, endurance, insulation resistance, and dielectric strength must be considered.

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Underwriters' Laboratories Standards for Safety:

UL 489 Branch Circuit Breakers

UL 943 Ground Fault Circuit Interrupters

UL 1077 (Proposed) Component Appliance Protectors

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TECH NOTE

Information Preserving Codes Compress Binary Pictorial Data

Data compression equations and methods, derived through analysis of redundancy and variable-length coding based on frequency of message occurrence, can significantly reduce storage requirements for binary pictorial data without content distortion

Usko Moilanen University of Oulu, Oulu, Finland

High speed data acquisition systems accumulate large amounts of binary data easily and rapidly; however, when such data must be transmitted, stored, or processed, problems arise. For example, binary pictorial data collected for character recognition purposes consist of binary pictures 1024 bits wide and 224 bits high (see Figure), resulting in a 14k-word disc file size, given that a word is 16 bits. Applying data compression techniques to these data can substantially reduce the requisite channel or data storage capacity while sustaining the information content and purpose.

Information Theory and Data Compression

Data compression methods are usually divided into two categories: reversible and irreversible; the former is also known as information preserving transformations or exact coding.[1] Since the method described enables a binary picture to be reproduced without distortion, it is designated as reversible. Data compression theory and applications are not discussed in detail since they have been well-documented.[1,2,3,4,5,6] Only those basic concepts of information theory that are useful for data compression[7] are covered.

Assume a set of messages: $A = \{a_1, a_2, \ldots, a_n\}$. If the *a priori* probabilities of these messages are $p_1, p_2, \ldots, p_n$, respectively, the entropy (H) of this source is defined by

$$H(A) = -\sum_{i=1}^{n} p_i \log p_i \qquad (1)$$

Assume that base-two logarithms are used. If these messages are encoded using a variable length binary code,[8,9] $C = \{c_1, c_2, \ldots, c_n\}$, which maps every a_i, $i = 1, \ldots, n$ to c_i, $i = 1, \ldots, n$. Let $L = \{l_1, l_2, \ldots, l_n\}$ be a set of numbers in which l_i gives the length of the code word c_i. The average word length of the code is now given by

$$\bar{l} = \sum_{i=1}^{n} p_i l_i \qquad (2)$$

Then, coding efficiency (E) is defined by

$$E = \frac{H(A)}{\bar{l}} = \frac{-\sum_{i=1}^{n} p_i \log p_i}{\sum_{i=1}^{n} p_i l_i} \qquad (3)$$

According to Shannon's first theorem[10] (noiseless coding theorem),

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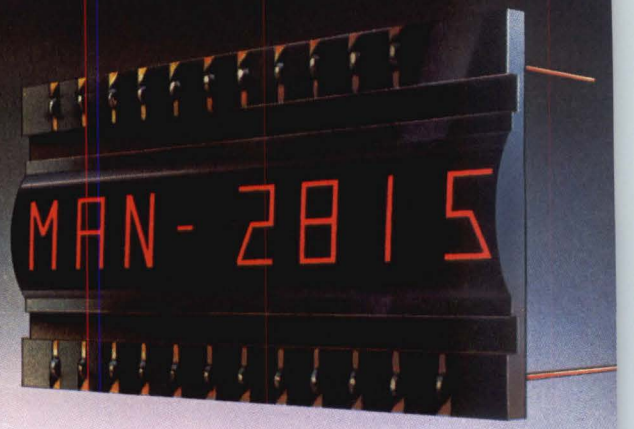

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Left: More characters—MAN2815 (top) and competitive unit character density in same panel space.
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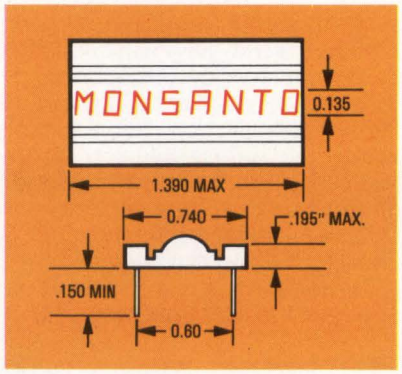

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$H(A) \leq \bar{l} \leq H(A) + 1$, implying that $E \leq 1$.

Employing Huffman's coding method[11] for any source, an optimal code can be constructed that has the following properties[7]: Its average word length is less than, or equal to, that of any other code for the same source; and it is instantaneously decodable, which implies that the code fulfils the "prefix condition," ie, no code word is a prefix of any other code word.

The useful concept of redundancy is defined by

$$R = 1 - \frac{H(A)}{H_{max}} \tag{4}$$

where H_{max} is the maximum entropy that can be conveyed by the symbols used. In this case, $H_{max} = \log n$.

If $\bar{l}_o$ is the average number of bits per source symbol before compression, and $\bar{l}_c$ is the average number of bits after data compression, the bit-compression ratio (ρ) can be defined by

$$\rho = \frac{\bar{l}_o}{\bar{l}_c} \tag{5}$$

Source Description

Let M_0 and M_1 be these sets of messages:

$$M_0 = \{m_{0,i} | m_{0,i} = 0^i, \quad i = 1, \ldots, 1024\} \tag{6}$$

$$M_1 = \{m_{1,i} | m_{1,i} = 1^i, \quad i = 1, \ldots, 1024\} \tag{7}$$

In these sets, 0^i denotes a string of i zeroes and 1^i denotes a string of i ones. A line 1024 bits long in the original picture files consists of messages that belong to either M_0 or M_1, in such a manner that no two successive messages belong to the same set (M_0 or M_1).

Experimental Results

The frequencies of the messages given in Eqs (6) and (7) have been computed from 10 picture files. Denote these frequencies as $f(m_{0,i})$, $i = 1, \ldots, 1024$ and $f(m_{1,i})$, $i = 1, \ldots, 1024$. Of these frequencies, $f(m_{0,1}) \ldots f(m_{0,31})$ and $f(m_{1,1}) \ldots f(m_{1,23})$ appeared more times than the other frequencies.

Let $M_0' = \{m_{0,1}, m_{0,2}, \ldots, m_{0,31}, m_{0,re}'\}$ be a set of messages. Then, the following estimates can be made for the *a priori* probabilities of the messages in M_0':

$$p(m_{0,i}) = \frac{f(m_{0,i})}{\sum_{j=1}^{1024} f(m_{0,j})}, \quad i = 1, \ldots, 31 \tag{8}$$

$$p(m_{0,re}') = \frac{\sum_{i=32}^{1024} f(m_{0,i})}{\sum_{j=1}^{1024} f(m_{0,j})} \tag{9}$$

A code C_0' is constructed for this source by Huffman's method: $C_0' = \{c_{0,1}, c_{0,2}, \ldots, c_{0,31}, c_{0,re}'\}$. In the same manner, the following estimates of the *a priori* probabilities are used for the other set of messages.

$$M_1' = \{m_{1,1}, m_{1,2}, \ldots, m_{1,23}, m_{1,re}'\}$$

Therefore,

$$p(m_{1,i}) = \frac{f(m_{1,i})}{\sum_{j=1}^{1024} f(m_{1,j})}, \quad i = 1, \ldots, 23 \tag{10}$$

$$p(m_{1,re}') = \frac{\sum_{i=24}^{1024} f(m_{1,i})}{\sum_{j=1}^{1024} f(m_{1,j})} \tag{11}$$

TABLE 1

Code C_1' Constructed for Source M_1' Using Huffman's Method

Symbol	Frequency	Variable Length Code Word	Bit Length
$m_{1,4}$	11416	10	2
$m_{1,3}$	10127	000	3
$m_{1,5}$	7237	011	3
$m_{1,2}$	4146	0011	4
$m_{1,6}$	3861	0101	4
$m_{1,11}$	2605	1110	4
$m_{1,7}$	2515	1111	4
$m_{1,8}$	2362	00100	5
$m_{1,10}$	2236	00101	5
$m_{1,9}$	2197	01000	5
$m_{1,12}$	1483	11000	5
$m_{1,13}$	1453	11001	5
$m_{1,14}$	1262	11011	5
$m_{1,15}$	934	010010	6
$m_{1,1}$	884	010011	6
$m_{1,16}$	632	110101	6
$m_{1,17}$	420	1101000	7
$m_{1,18}$	224	11010010	8
$m_{1,19}$	99	110100110	9
$m_{1,20}$	35	1101001110	10
$m_{1,21}$	21	11010011110	11
$m_{1,22}$	4	110100111110	12
$m_{1,23}$	2	1101001111110	13
$m_{1,re}'$	0	1101001111111	13

In Table 1 a variable-length code C_1' is also constructed for this source by Huffman's method: $C_1' = \{c_{1,1}, c_{1,2}, \ldots, c_{1,23}, c_{1,re}'\}$.

In order to code any singular message contained in $m_{0,re}'$ or $m_{1,re}'$, a string of 10 bits should be added to code words $c_{0,re}'$ or $c_{1,re}'$ to show which original message is concerned. In this manner, the following codes are obtained:

$$C_0 = \{c_{0,1}, c_{0,2}, \ldots, c_{0,1024}\} \tag{12}$$

$$C_1 = \{c_{1,1}, c_{1,2}, \ldots, c_{1,1024}\} \tag{13}$$

Exact performance data of codes C_0 and C_1 are given in Table 2. The values were computed using the files

TABLE 2

Performance Data of Codes C_0 and C_1

Source	Code	Entropy	$\bar{l}$	E
M_0	C_0	5.129	5.503	0.968
M_1	C_1	3.580	3.622	0.986

Binary pictures. Two copies of original picture files are shown as displayed on a CRT terminal. Each is sized with 1024 x 224 bits. Original alphanumeric characters were generated within 7-mm squares. Each displayed copy contains 32 x 7 characters and the size of each character matrix is 32 x 32 bits

obtained from calculating the frequencies of messages M_0 and M_1. In counting the listed entropies, the probability estimates for source symbols M_0 and M_1 have been counted using Eqs (8) and (10) for i = 1, . . . , 1024.

Method Evaluation

To compress picture files (such as those in the Figure), a bit is added at the beginning of each row to indicate whether the first message of that row belongs to set M_0 or M_1. The messages of each row are then coded using codes C_0 and C_1. This method results in a bit-compression ratio of 4.363 for the 10 picture files used when counting the frequencies of messages M_0 and M_1. This ratio implies that the total size of the original picture files is 4.363 times greater than that of the compressed picture files. Data compression has also been tested on 24 picture files, giving an average bit-compression ratio of 4.149. The inverse values of these two compression ratios are 0.229 and 0.241, respectively, revealing that 77.1% and 75.9% of the original file sizes have been removed by the described data compression method.

The behavior of the data compression method among different files has also been tested. Table 3 gives test results for the 10 picture files that were used while learning the statistics of the data. In this table, entropy symbols H_0 and H_1 have these meanings:

$$H_0 = -\sum_{i=1}^{1024} p(m_{0,i}) \log p(m_{0,i}) \qquad (14)$$

$$H_1 = -\sum_{i=1}^{1024} p(m_{1,i}) \log p(m_{1,i}) \qquad (15)$$

Estimates for the probabilities have been counted for the respective files. Bit numbers $\bar{l}_0$ and $\bar{l}_1$ give the average code word lengths when using codes C_0 and C_1, and ratios ρ and $1/\rho$ show the final performance of the coding method when applied to the respective picture files.

TABLE 3

Performance Variations of Data Compression Method Among 10 Learning Files

H_0	H_1	$\bar{l}_0$	$\bar{l}_1$	$1/\rho$	ρ
5.038	3.399	5.628	3.603	0.211	4.734
5.163	3.417	5.541	3.573	0.251	3.985
5.215	3.517	5.552	3.676	0.238	4.201
4.970	3.417	5.621	3.634	0.234	4.265
4.914	3.558	5.297	3.627	0.260	3.841
5.026	3.511	5.461	3.593	0.242	4.126
5.146	3.706	5.752	3.864	0.180	5.570
5.000	3.593	5.302	3.664	0.247	4.055
5.091	3.443	5.541	3.524	0.200	5.000
5.009	3.359	5.467	3.512	0.229	4.375

Data compression tests have been made for 24 other picture files. In the best case, 83.0% of redundancy was removed and, in the worst case, 69.7%. The described data compression method—easily implemented by computer programming—substantially reduces the data redundancy of binary pictorial information. Overall results indicate that an average saving of about 76.2% in storage capacity is achieved.

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CIRCLE 66 ON INQUIRY CARD

APPLICATION NOTE

Digital Input Units Isolate Microcomputers From Industrial Level Voltages

Interfacing microcomputers to comparatively high voltage input signals present in industrial process control applications can be accommodated via optical isolation. Digital input units containing opto-isolators protect the microcomputer from standard as well as overvoltage conditions

C. R. Teeple Burr-Brown Research Corporation, Tucson, Arizona

Although the current abundance of inexpensive microcomputers has made the computer control and monitoring of many industrial process functions economically feasible, most popular microcomputers do not interface readily with some of the control systems. For example, large industrial process monitoring relays and switches generate widely varying high voltage pulses that must be conditioned before interfacing to low voltage microcomputers; on/off states of large 24-Vdc or 110-Vac relays must somehow interface with the 5-V metal-oxide semiconductor or transistor-transistor logic level digital transitions of the microcomputer. In addition analog-to-digital and digital-to-analog conversion interfaces must be provided for system inputs and outputs.

As one solution to this problem, at least for Micromodule™ and SBC™-80 microcomputers, direct compatibility can be attained through use of digital input units (DIUs). Opto-isolators in the DIUs protect the microcomputers from damaging voltage transients, surges, and malfunctions that occur in harsh industrial environments. In addition, optical isolation tolerates widely varying inputs and prevents the occurrence of ground loops.

Opto-Isolation

Opto-isolators consist of a light source optically coupled to a light sensor. They transmit data while maintaining a high degree of electrical isolation between input and output. Isolators made up of incandescent or neon light sources coupled with cadmium or lead salt photoresistor sensors have been in service for many years. However, most present devices use a gallium arsenide infrared light-emitting diode (LED) as the light source and a silicon phototransistor as the sensor (Fig 1). These devices inherently possess reliability, low cost, relatively high switching speed.

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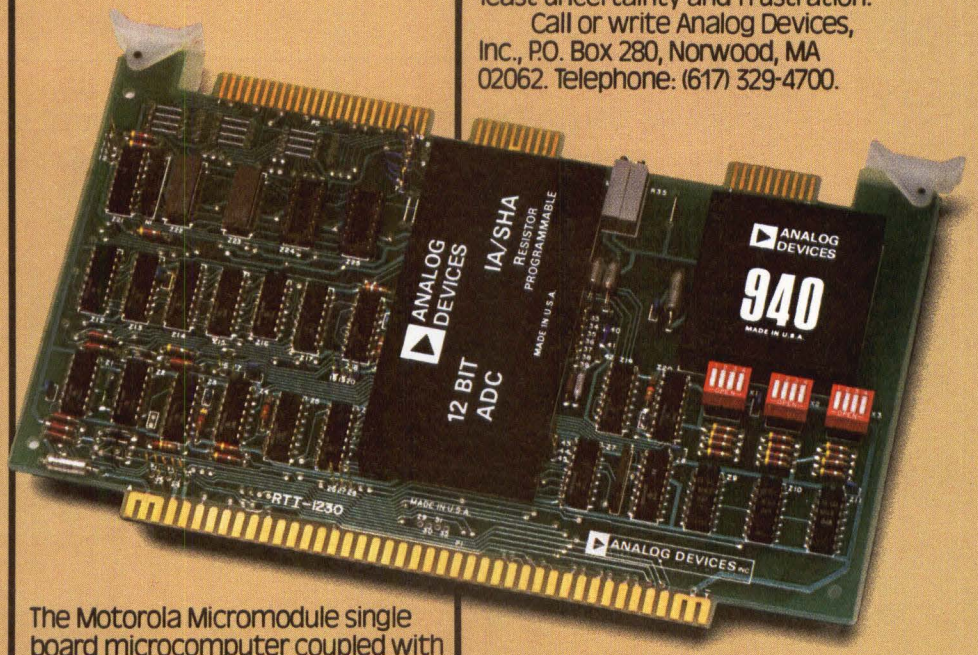

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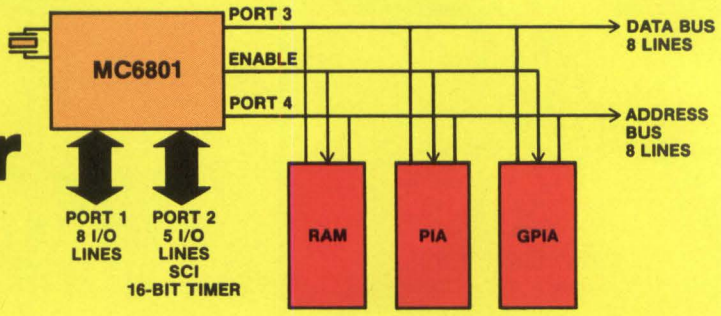
CIRCLE 67 ON INQUIRY CARD

Motorola announces microcomputer yet:

Three easily user-implemented modes on one powerful microcomputer chip.

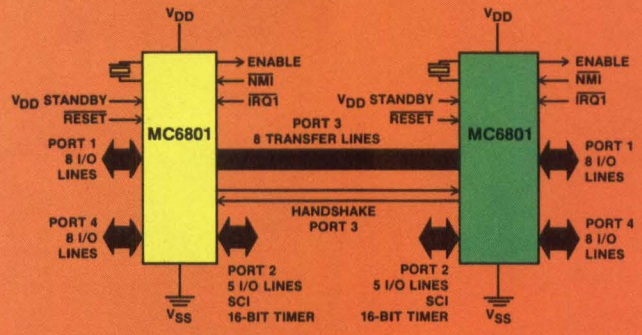
MC6801 Expanded Non-Multiplexed Mode

Minimal system configuration.



MC6801 Single-Chip Mode

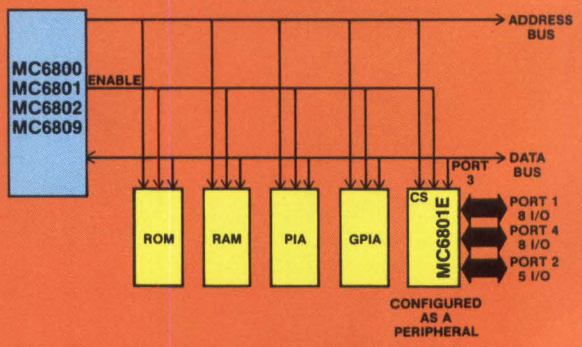
Two MC6801s tied together, both in single-chip mode, for dual processor configuration.



Parallel I/O Interface

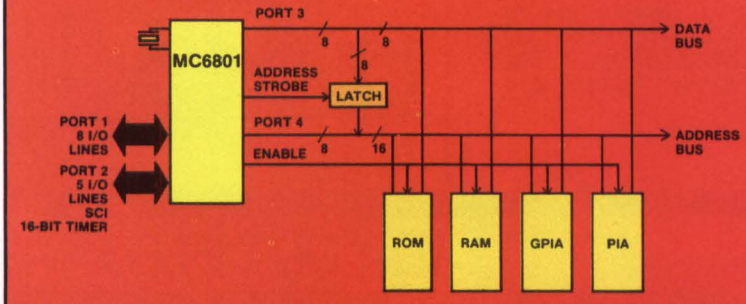
MC6801E Single-Chip Mode

Peripheral controller configuration as an alternative to custom chip or MSI design.



MC6801 Expanded Multiplexed Mode

Full 65-byte configuration for higher-end communication/EDP applications.



the most flexible the unique MC6801.

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The versatile MC6801 is an eight-bit microcomputer—with 16-bit instructions, an internal data bus, and on-board ROM, RAM, timer, clock, I/O and serial communications interface—and it's 100% bus-compatible, op- and source-code compatible, software-compatible and upward expandable with all M6800 micros, memories, peripherals, special purpose devices and development and support hardware and software.

And it's a powerful one-chipper. The CPU has 10 enhanced 16-bit instructions, one of which is an 8 x 8 hardware multiply with 16-bit result in 10 μsecs (1 MHz clock) and 64K external addressability.

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- Ten 16-bit instructions
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- Up to 64K addressability
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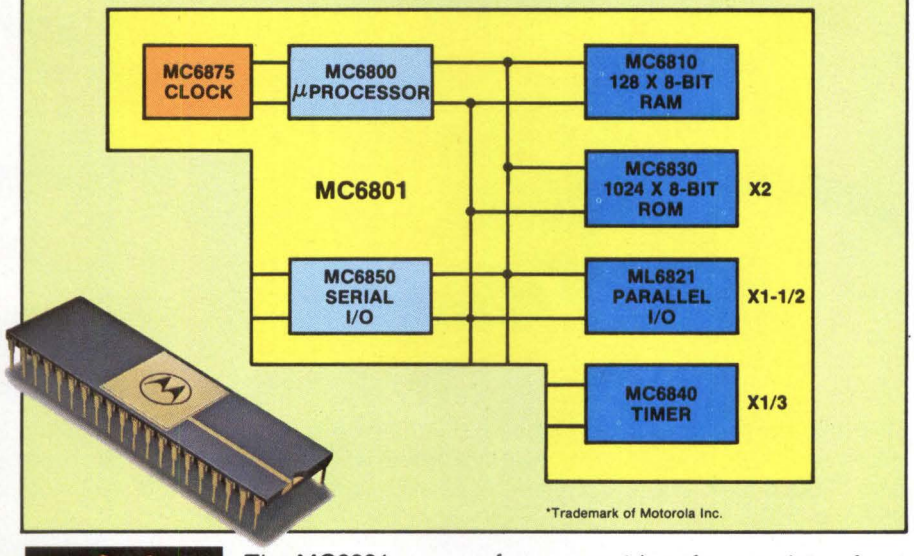

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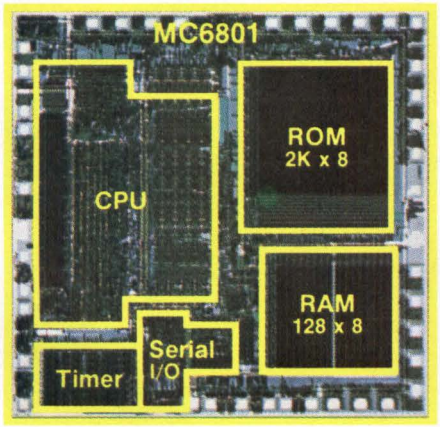


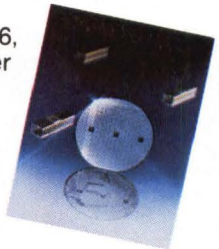
The MC6801 replaces many multi-chip and board-level systems with a single 5 V chip that's faster, more powerful and reliable, easier to test and lower in system cost. All of which gets you to market faster, more aggressively.

For serial communications in distributed processing, the I/O port can be used with the SCI in a slow-speed system or with parallel data I/O in higher-speed systems. It has full or half duplex capability, both with mark/space (NRZ) and bi-phase (FM) options; an on-board bit rate generator with four user-selectable baud rates; and three-wire transmission (clock, receiver and transmitter lines).

The MC6801 microcomputer is available now, in limited sample quantities. Production quantities will be available in December. Same for a no-ROM version of the '6801, the MC6803. An EPROM version—the MC68701—will also be out in the fourth quarter, while the MC6801E—which is the '6801 wired for external clock operation—will bow first quarter '79.

The versatile MC6801 is backed by not only one of the highest VLSI production capabilities in the world but also Motorola's vast commitment to continued expansion of the M6800 Family and full retention of software compatibility with all existing and planned parts. And thus users' systems of tomorrow.

Whether to gain the economy of a one-part buy for a variety of applications, or to win 100% compatible, expandable flexibility for your mid- to high-end applications of tomorrow, the MC6801 rates your very serious examination. For a data sheet and a complete overview brochure on this third-generation, first-of-its-kind-on-the-market microcomputer, write Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036, or circle the reader service number.



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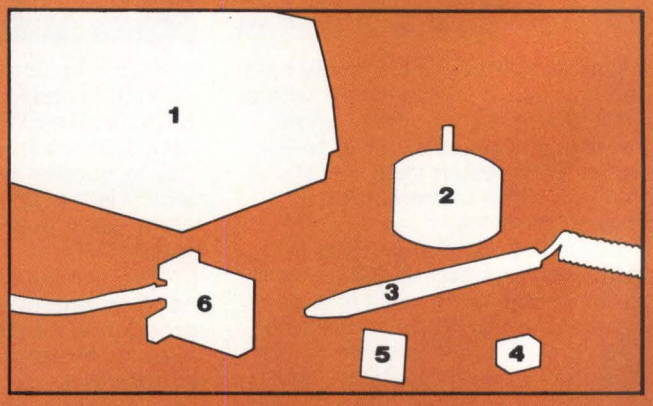

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Because they have no external optical characteristics, opto-isolators are considered as electrical devices; their major characteristics are efficient transfer of information from input to output, switching time, and electrical isolation from input to output. Transfer efficiency depends upon the combination of operating temperature and input (forward) current. Switching time is a function of the phototransistor base storage time and the output circuit time constant. Electrical isolation comprises insulation resistances above 10^{10} Ω, input-to-output capacitance of less than 0.5 pF, and typical breakdown voltages on the order of several kilovolts.

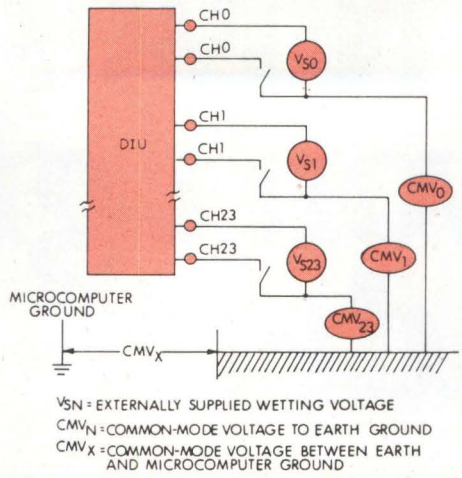

Fig 2 Common mode voltages. Different common mode voltages are possible from each input to earth ground. Isolated input channels ignore differences in common mode voltages, ie, differences in ground potentials and accidental overvoltages while breaking ground loops

Isolated Inputs

Optically isolating the source of the digital input from the microcomputer system rejects voltage transients at the DIU. For instance, a 500-V common mode surge on a TTL-type input of the microcomputer would immediately short across the input logic to the system 5-V supply and, most likely, destroy a majority of the system logic. With optical isolation, this surge would not reach the system bus, and might not even be noticed. As shown in Fig 2, different common mode voltages affect the operation of a digital input system; for example, CMV_0 through CMV_{23} are the common mode voltages from earth ground to each input pair of 24 data input channels (CH_0 to CH_{23}).

Each data input channel will operate properly (ie, each external switch contact closure will be detected) up to the maximum common mode voltage rating (600 Vdc). Different common mode voltages between channels must be less than 300 Vdc. Because the 24 data input channels of the DIU are typically arranged in three groups of eight (channels 0 to 7, 8 to 15, and 16 to 23), acceptable common mode voltage from channel to channel between groups is 600 Vdc. Thus, if the common mode voltage of some groups of channels varies widely, the inputs may be segregated to the three groups to accommodate the variations.

If the DIU supplies wetting current for external switch closures from its three onboard power supplies, it cannot withstand common mode voltages between channels within a group. (Wetting current is the current forced through the contact closures of a switch to detect whether they are open or closed.) However, the isolation of this DIU is 600 Vdc between groups of eight channels since the three onboard power supplies are separately isolated. Isolation from one DIU board to another is 600 Vdc.

Isolation prevents ground loop currents from flowing between remote grounds (at a contact closure for instance) and the local microcomputer ground. Voltage potentials between these two grounds can cause current to flow through the application sensing circuitry. This current could generate enough noise and interference to make the detection of open and closed contacts extremely difficult. Optical isolation interrupts the current flow path, resulting in clean, noise free input signals.

Differentially applied input voltage to each data channel circuit is shown in Fig 2 as V_{sn} where N = 0 to 23. The DIU input circuitry can handle a wide range of differential voltages, such as 17 to 84 Vdc and 34 to 168 Vac. Therefore, even differentially connecting input channels directly to line voltages (120 Vac) will not harm the microcomputer system or the input circuitry.

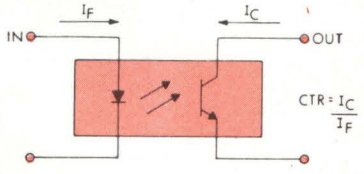

Fig 1 LED-phototransistor optoisolator. Key performance parameters include current transfer ratio (CTR), which is current gain in percent; operating speed, which reflects how rapidly output can be switched; and isolation voltage, which indicates dielectric strength between input and output

Digital Inputs

One type of DIU interfaces to "dry" contact closure inputs using an onboard power supply to supply wetting current, while a second DIU type interfaces to "wet" voltage inputs or contact closures using an external voltage source to supply wetting current. Fig 3 depicts the equivalent input circuitry of one data channel for dry contact closure sensing.

An ideal relay has zero impedance (R_{CLOSED}) between its contacts when closed and infinite impedance (R_{OPEN}) between its contacts when opened. In practice, a relay circuit has impedance when closed due to wire, contact, and termination resistances. This type of DIU is designed to detect a closure with R_{CLOSED} resistances as high as 6 kΩ. Similarly, when the contacts of an actual relay are open, the resistance detected at the input

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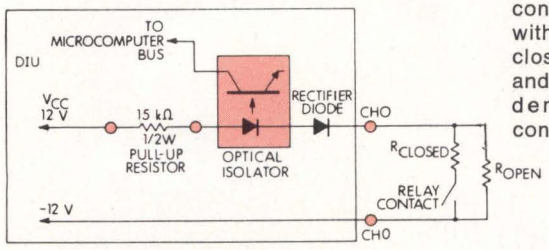

Fig 3 Dry contact closure interface. Input circuit comprises onboard wetting current supply for dry contact closure sense, input protection (pull-up) resistor, rectifier diode, and optical isolator for microcomputer interfacing. External "ideal" relay contact closure is shown with equivalent open and closed resistances (R_{OPEN} and R_{CLOSED} respectively) to demonstrate actual relay contact closure

circuitry is less than infinite. This may be due to wiring layout, printed circuit board traces, collected contaminants, or humidity. This DIU type will detect open relay contacts with R_{OPEN} resistances as low as 80 kΩ. The onboard ±12-Vdc voltage source provides wetting current for the external relay contacts being sensed. This isolated voltage is generated by the DIU from the microcomputer 12-Vdc supply. The rectifier diode protects the onboard circuitry if an accidental ac voltage is applied across the inputs; up to 168 Vac or 84 Vdc can be applied across the input channel without damage. This DIU can be modified by changing jumpers to operate on any selected data channels with either wet or dry contact closures.

The circuit shown in Fig 4 is basically the same as that described for Fig 3 except that this DIU does not have an onboard voltage source to supply wetting current for the relay contacts. Permissible limits for R_{CLOSED} and R_{OPEN} vary in direct proportion with external voltage source V_S. For instance, with V_S = 24 Vdc, R_{OPEN} = 80 kΩ minimum and R_{CLOSED} = 6 kΩ maximum; with V_S = 60 Vdc, R_{OPEN} = 235 kΩ minimum and R_{CLOSED} = 58 kΩ maximum. At any V_S between 24 and 84 Vdc, there is a proportionally wide range of acceptable resistances. This type of DIU also accepts direct voltage inputs. An input of 4 V or less will be detected as a logic 0, and an input of 17 V or more will be detected as a logic 1.

In microcomputer systems, these digital inputs are read as memory locations. Since each digital input is one memory bit, eight inputs constitute one byte of memory, and any read instruction may be used. When an input is read, a logic 0 represents an open contact or a low voltage, and a logic 1 represents a closed contact or a high voltage. Since each memory read instruction inputs the status of eight data channels, a double-byte read instruction, such as LDX (load index register), would be used to read the status of 16 channels. The remaining address lines are used to select the DIU itself. The address block occupied by each DIU is wire jumper selectable and can be located anywhere in memory. For example, a typical read instruction that inputs the status of eight channels is LDA $90FC, or load (LD) the accumulator (A) with the status of data channels 0 to 7 [90FC is the location of channels 0 to 7 in hexadecimal ($) code].

Then, a variety of simple operations can be done to determine further actions. For instance, if only one input channel is of importance for a particular operation, the accumulator may be ANDed with 00000010 to easily determine the status of the input channel in the second position (X_1) as

AND:	$X_7X_6X_5X_4X_3X_2X_1X_0$	Accumulator contents
	0 0 0 0 0 0 1 0	
	0 0 0 0 0 0 X_1 0	Result

The result in the accumulator may then be tested to act on the status of channel X_1, as

LDA	$90FC	Load status of channels 0 to 7 into accumulator
AND	$02	AND accumulator with 02_{16} (00000010_2)
JMP	ROP	If X_1 is a logical 1 (closed contact), jump program to ROP subroutine
LDA	$90FD	If X_1 is a logical 0 (open contact), continue program by loading status of data channels 8 to 15 into accumulator

ROP is a subroutine that takes the necessary action when X_1 is a closed contact. For instance, X_1 = 1 may mean that the flow of coolant has dropped below a preset limit. Consequently the ROP subroutine would stop the process being cooled and sound an alarm.

Each word read from the DIU represents the present status of each channel as the read operation occurs. An input delay time (due to the response time of the opto-isolator LED) is required to allow a change of state of any input to be detected. The input delay time needed to detect the change of an input from open to closed (logic 0 to 1) is typically 25 μs; the time required to detect the change of an input from closed to open (logic 1 to 0) is typically 100 μs. Also, the input delay time of the DIU acts as an input noise filter to eliminate

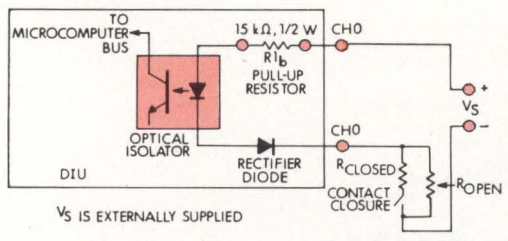

Fig 4 Wet contact closure interface. Input circuit handles either voltage inputs or "wet" contact closures. External source of wetting current is shown in series with relay circuit, rectifier diode, protection (pull-up) resistor, and optical isolator

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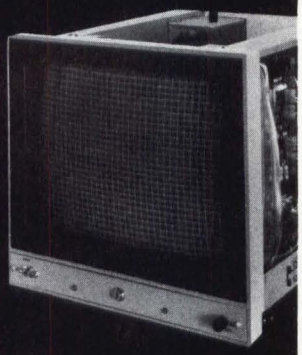

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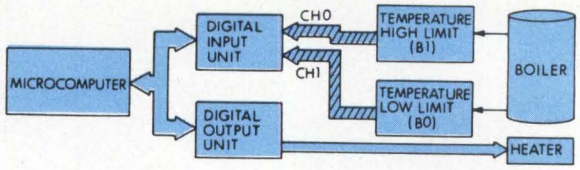

Fig 5 Temperature controller subsystem. DIU continuously feeds process status of temperature limit switches to microcomputer for control action. When boiler temperature drops below low limit, heater is activated; when boiler temperature rises above high limit, heater is de-activated. Both actions are triggered by microcomputer working through digital output unit (DOU)

high frequency noise from the input circuitry because noise pulses of less duration than the delay times will not pass through.

When the coil of a relay changes state, its contacts do not immediately make a change due to switching time, which is measured in hundreds of microseconds or milliseconds. The contacts also bounce from one state to the other during the transition. In most industrial applications, contact bounce can be disregarded. However, debouncing circuitry can be added to some DIUs to filter the input circuitry response to input changes. For instance, a debouncing time of 10 ms can be implemented. This means that an input change of state must hold beyond 10 ms before the DIU recognizes it is a legitimate change; thus, contract bounce is ignored. For the DIUs, debouncing typically is not needed. If the inputs are read during the bounce time of a contact change of state from open to closed (debouncing circuit not included), the data can read either open or closed. If the data reads open, the result is the same as if debouncing were in the circuit because the change has not been detected yet. If the data reads closed, the new reading is correct. The time between readings should be longer than the bounce time so that successive readings do not read a peak and then a valley. This limitation on time between readings is not a greater restraint than the delay that would be imposed by a debouncing circuit. If the actual bounce of the contacts is shorter than the debouncing time that would have been imposed, the nondebouncing method is actually faster.

Basic Temperature Controller Application

Fig 5 shows a simplified temperature controller subsystem using a microcomputer with isolated digital inputs and reed relay outputs. Contact closure inputs are obtained from two temperature limit switches. Switch B1 closes when the temperature rises above a high limit, while switch B0 closes when the temperature drops below a low limit. Application process monitoring status and resulting control action are

Input B_1B_0	Process Status	Control Action
0 0	Temp in range	No change
1 0	Temp too high	Turn off heater
0 1	Temp too low	Turn on heater
1 1	Controller malfunction	Indicate controller malfunction

Summary

By electrically isolating microcomputers from the high voltage pulses inherent to industrial applications, digital input units enable microcomputers to interface with process control and monitoring system components. Opto-isolators protect the 5-V microcomputers from the 24-Vdc or 110-Vac common mode voltages, ground potential differences, and accidental overvoltages while breaking ground loops. As a result, many available microcomputers can now be used in relatively inexpensive process control systems. □

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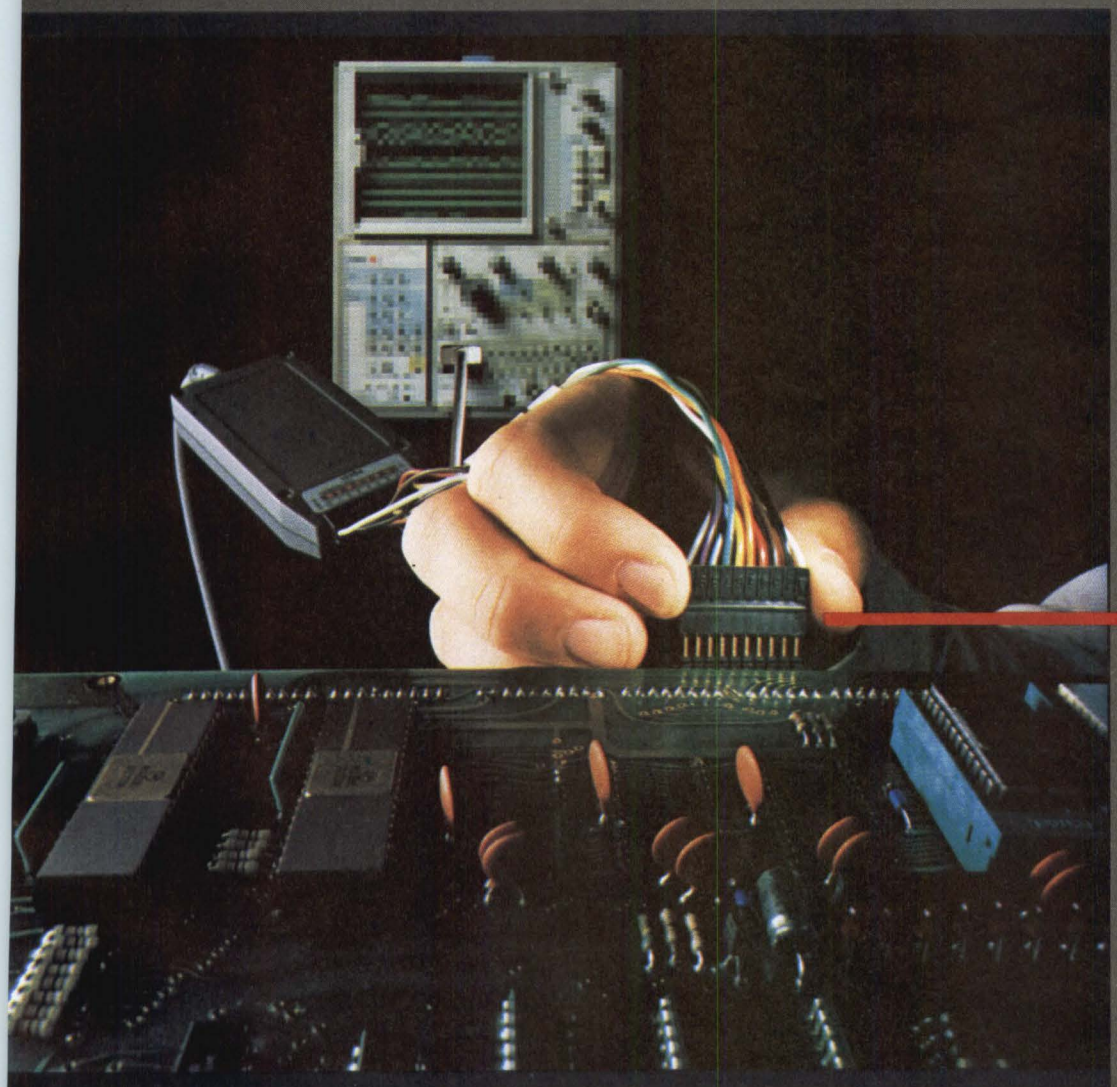

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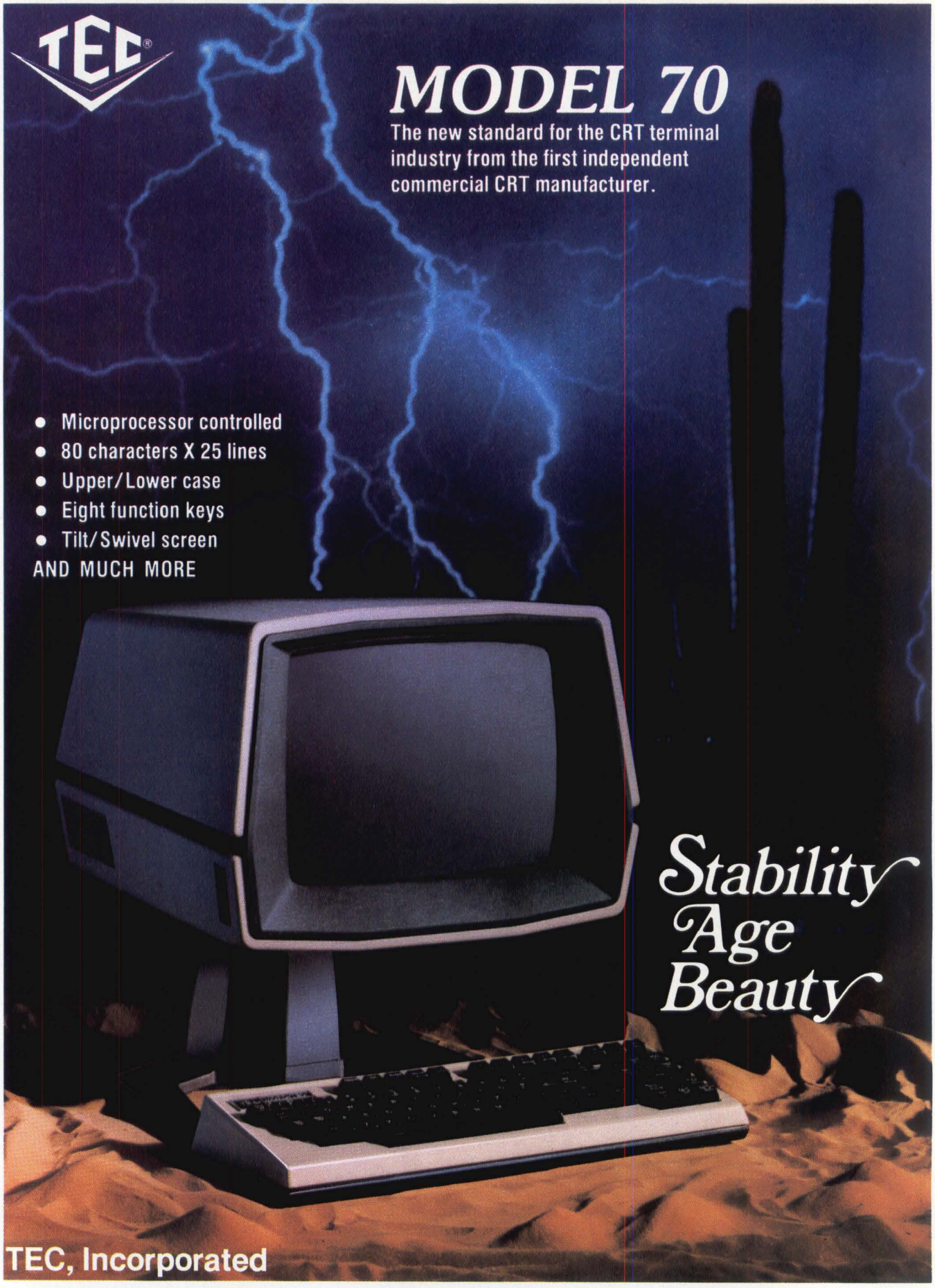

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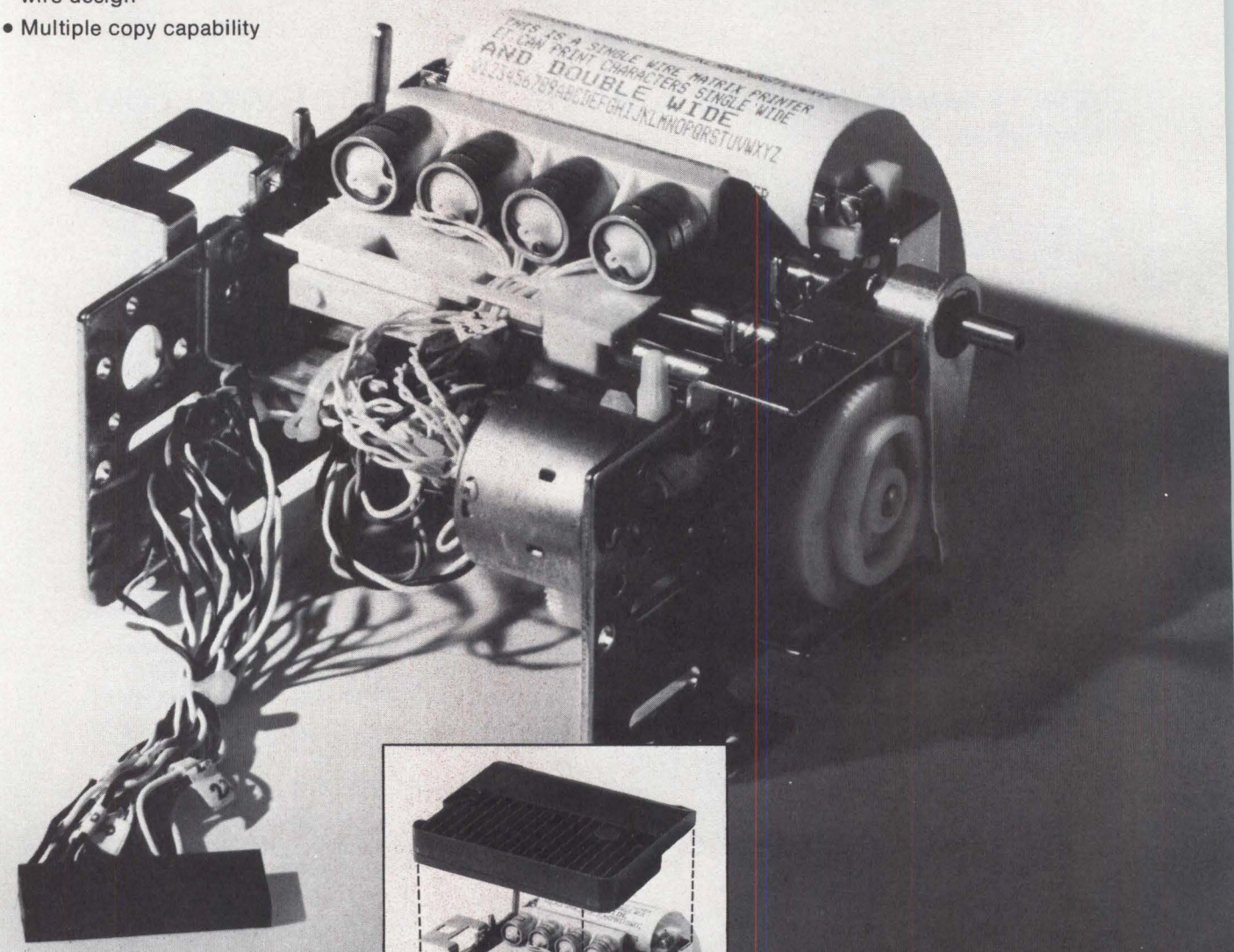

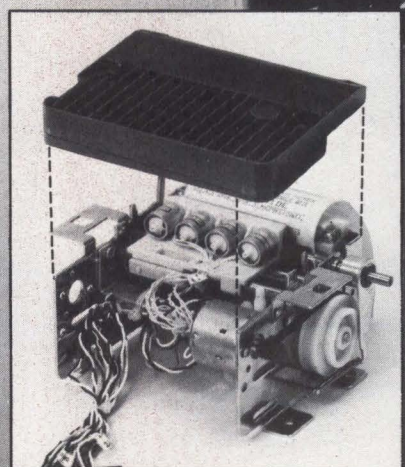

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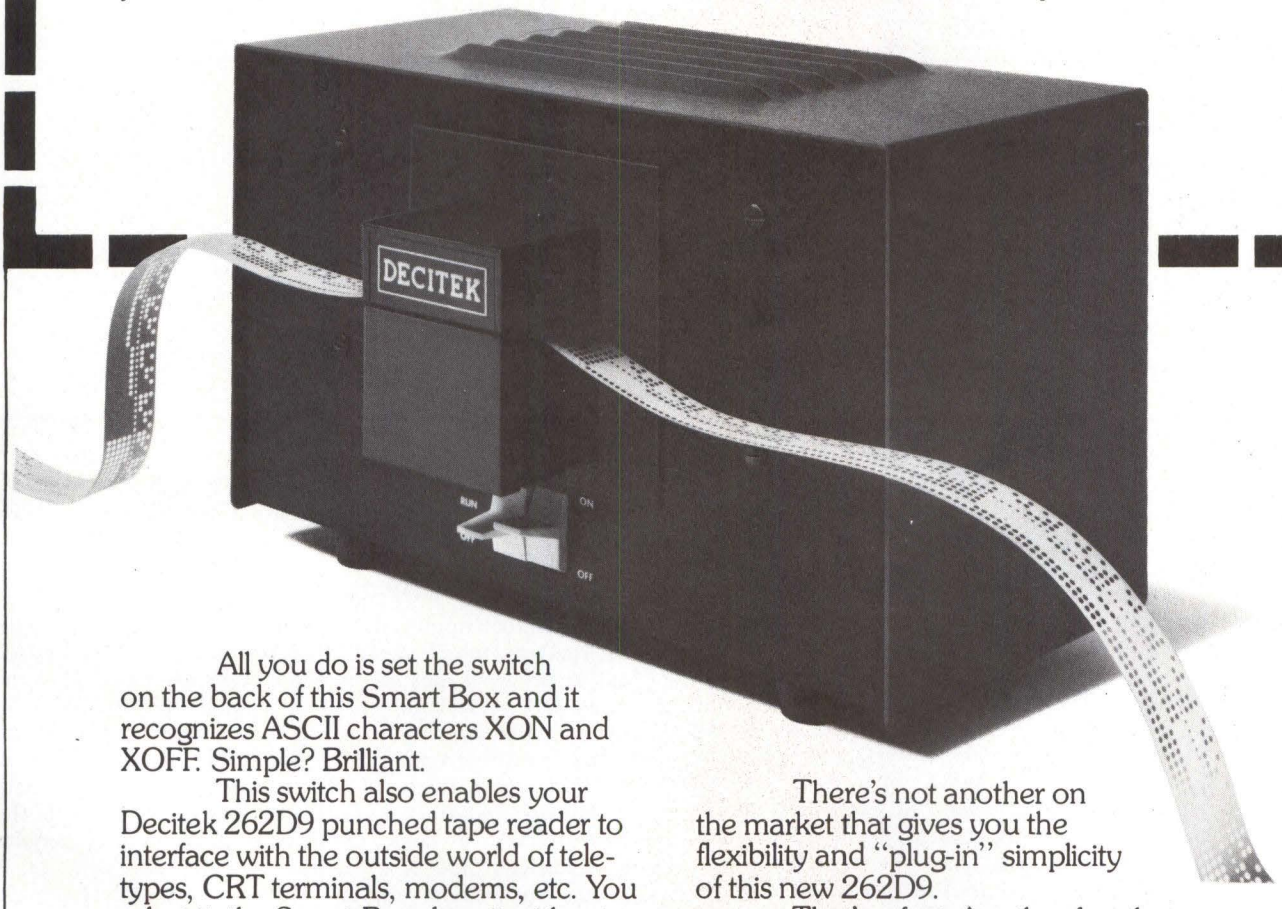

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INTERFACING FUNDAMENTALS: ASSEMBLY LANGUAGE OR BASIC, WHICH WAY TO GO?

David G. Larsen and Peter R. Rony
Virginia Polytechnic Institute and State University

Christopher Titus and Jonathan A. Titus
Tychon, Inc

As the application of microcomputers continues to grow, more and more users are wondering what the best language is for programming a microcomputer. Currently, the only two languages that have widespread support are assembly language and BASIC[R].

The choice of one language or the other involves a number of associated advantages and disadvantages that must be considered. The two languages should be compared on the basis of cost of programming, memory requirements, machine independence of programs, program relocatability, user's libraries, logical operations, use of nonstandard peripherals, and speed of execution. These factors are not in order of importance; in fact, there are probably items of interest that have been omitted. For a particular microcomputer application, the user may be interested in only one of the items, such as memory (storage) requirements. Other users may feel that all of the items are important and therefore must be considered.

Cost of Programming

Programming a microcomputer in *any* language includes the cost of preparing flowcharts, entering the program into the microcomputer (using the assembly language editor or BASIC interpreter), debugging the program, and producing the user's manuals, program listings with comments, and other documents that are needed to make the programs useful to others. Programs written in BASIC generally are much shorter than equivalent assembly language programs so that program entry costs should be much lower. Since one BASIC statement may be the equivalent of up to 50 or more assembly language instructions, debugging costs should also be less. Program listings and comments should also be shorter. Therefore in terms of programming costs, a program written in BASIC should be less costly than the same program written in assembly language.

Memory Requirements

Most microcomputer BASIC programs are in the form of interpreters, which means that the interpreter *and* application program must be in the computer's memory at the same time. Available BASIC interpreters require between 6k and 12k memory locations for storage. Some shorter BASIC interpreters may require only 2k memory locations, but they lack many of the features required for data acquisition, control, or data processing. Along with the interpreters, the BASIC application program may require an additional 500 or 1k memory locations for storage. A similar application program written in assembly language may require only 2k or 3k memory locations for storage. The important distinction between the two languages at this point is that only 2k to 3k memory locations are required for the assembly language program, as opposed to a BASIC program that requires 6.5k to 13k memory locations (the BASIC interpreter and the BASIC application program combined).

With a larger program, BASIC looks better, since the amount of memory required to store the interpreter becomes relatively smaller. On the other hand, for short programs, BASIC requires a great deal of memory; a short assembly language program that uses much less memory would be more practical. Memory costs money, consumes power, and may fail.

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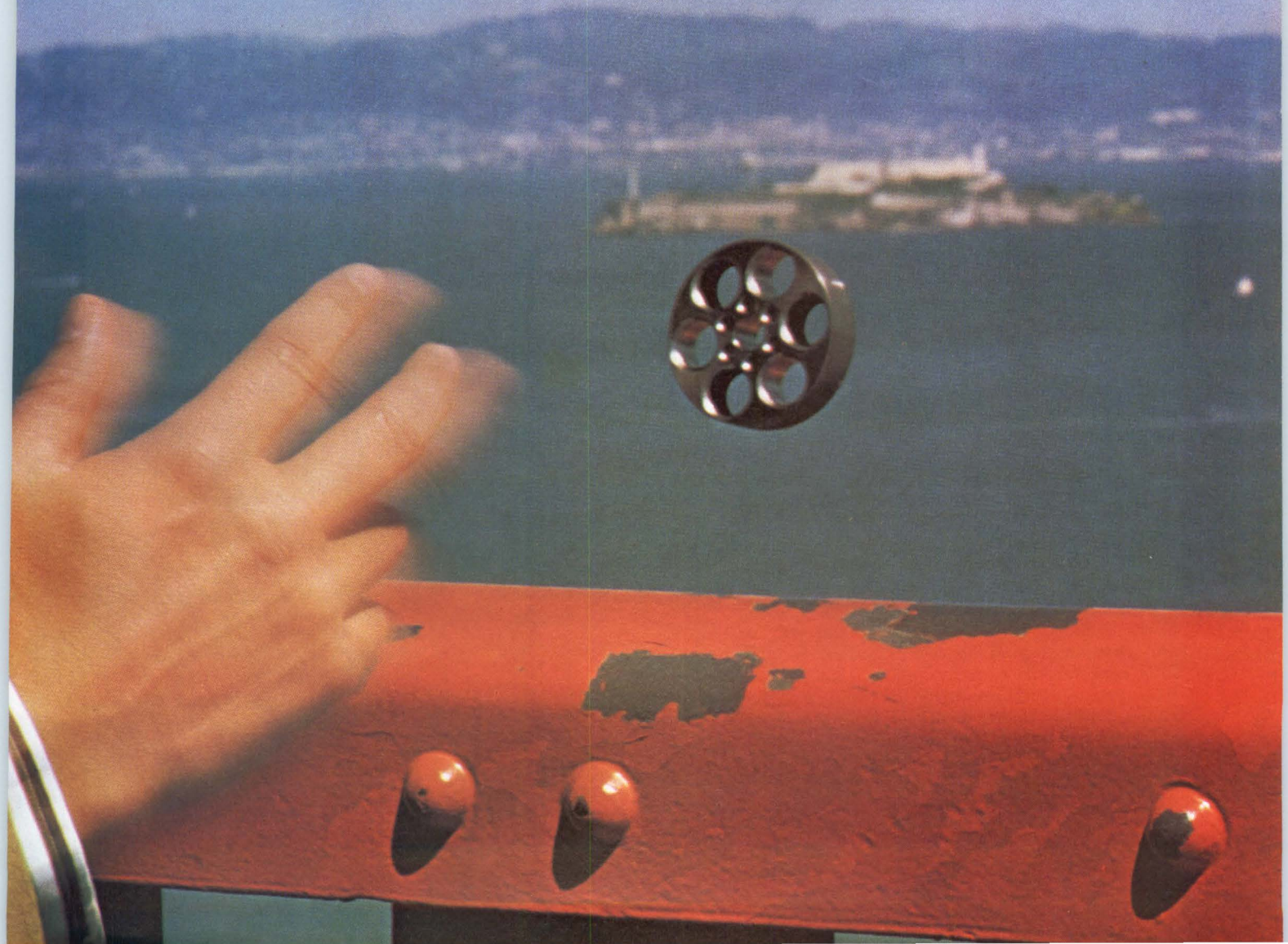


Machine Independence of Programs

Many project managers are becoming increasingly wary of assembly language programs that cost $10,000 or $20,000 and can be used with only one type of microcomputer (ie, an assembly language program written for the 8080 will not execute on a 6800, 8008, 6502, or 9900 based computer). Assembly language programs are very computer dependent. Programs written in BASIC, however, can be independent of the actual computer on which they are run. That is, a BASIC program written on an 8080 based microcomputer will probably execute properly on a 6800, 6502, or 9900 based microcomputer. Presently though, BASIC application programs are not totally machine independent, because the BASIC interpreters for the various microcomputers may or may not have identical functions. Thus, some BASIC interpreters have a "log" function while others may not; if a log function were not available, the user could add one in about 25 BASIC steps. For the most part, it is easier to modify a BASIC program for a different microcomputer system than it is to modify an assembly language program.

Program Relocatability

As assembly language programs grow in complexity, data storage areas, stack areas, and subroutines have to be moved about in memory. Reassembly of the entire program is often necessary. This is particularly true for an 8080 assembly language program, simply because the 8080 uses absolute addressing. For assembly language programs written for the 6800 or 6502, which use relative addressing, this reassembly process may not be required, although it is often recommended. For a BASIC application program, data storage areas and stack areas are allocated as the program is interpreted by the BASIC interpreter. Therefore, the programmer does not have to worry about where data values or subroutine return addresses are stored. The interpreter remembers where all data values are stored, allowing variables, constants, and arrays to be added, changed, or deleted.

User's Libraries

Many minicomputer programmers have resisted using a microcomputer simply because there are no comparable user's libraries for microcomputers. What most programmers fail to realize is that many of the programs in these libraries, particularly those submitted by the users, are very difficult to utilize. Many of them require a special peripheral device, special peripheral interface, certain types of memory at specific addresses, or extended mathematical capabilities. Unfortunately, this is also true of many of the programs in the various microcomputer user's libraries. Programs, submitted to the libraries just to gain entry, are not judged on their merits. Of course, if one program in the user's library saves you $10,000 or $20,000, the library is certainly worthwhile. However, do not depend on a program in a user's library until you have run it through its paces on *your* microcomputer system.

Logical Operations

Most microcomputers can perform AND, OR, exclusive-OR and compare logical operations, which may be particularly important if the microcomputer system must be used to control a number of devices. Many BASIC interpreters cannot perform these operations. If the microcomputer has to monitor 50 sensors and switches, and control 5 pumps, 15 valves, and 32 lights based on the states of these sensors and switches, it may be easier to write the program in assembly language. Of course, logic operations can be performed in BASIC by using a sequence of mathematical operations. However, if this is done in the BASIC application program, the logical operations may take tens or hundreds of milliseconds.

Using Nonstandard Peripheral Devices

If a nonstandard peripheral device is interfaced to the microcomputer system, then an assembly language subroutine (a device handler) can probably be written to control it. In all probability, a BASIC interpreter will not have a device handler for this device. Instead, the user must write the BASIC application program so that it can *call an assembly language subroutine* that operates the special device. Some BASIC interpreters have very sophisticated features when is comes to "patching-in" or adding an assembly language subroutine to the BASIC application program; others do not. Chances are that in order to do some interfacing, the user will have to write the assembly language subroutines for the peripheral device. If BASIC is used, then the BASIC interpreter must be able to access this device through the assembly language steps.

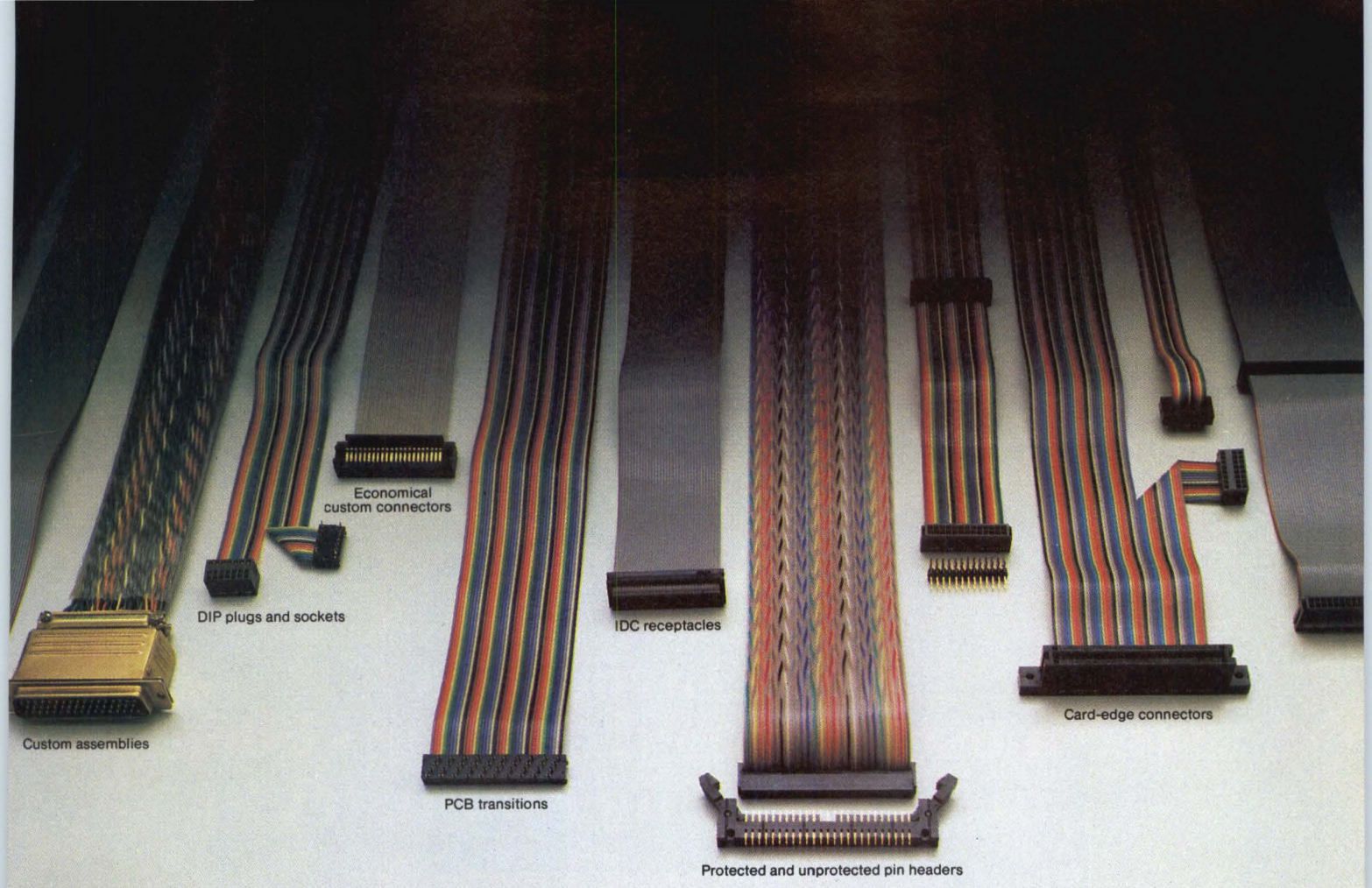
Speed of Execution

Actual speed of a program's execution may be an important consideration. In general, the speed at which a BASIC application program can be executed is determined by the particular BASIC interpreter and computer used. An interpreter that uses integer numbers will be faster than one that uses floating point numbers. A simple BASIC statement may require 1 or 2 ms in which to be executed while the equivalent assembly language operation may require only 30 to 40 μs. If the microcomputer must digitize an analog signal 10 times each second and do a slight amount of data processing, then either assembly language or BASIC will probably work. If a signal must be

EXAMPLE 1

Assembly Language Program to Read 8-Bit Values From Peripheral Device

```
          *010 000
TEST1,    LXISP     /Load the stack pointer with a
          STACK     /R/W memory address.
          0
          LXIH      /Load register pair H with
          350       /1000 decimal
          003
AGAIN,    CALL      /Call the read subroutine so that
          READ      /a character can be input
          0
          DCXH      /Decrement the count
          MOVBA     /Save the value in the B register
          MOVAH     /Get the MSBY of the count
          ORAL      /OR it with the LSBY of the count
          JNZ       /The count is nonzero, so
          AGAIN     /get another data value.
          0
          HLT       /Read 1000 values, so halt
READ,     IN        /Input the status word of the
          021       /peripheral device
          ANI       /Save only one of the flags
          004
          JZ        /The flag is 0, so wait for
          READ      /it to become a logic 1
          0
          IN        /The flag is a 1, input the
          020       /8-bit data value
          RET       /and then return
```



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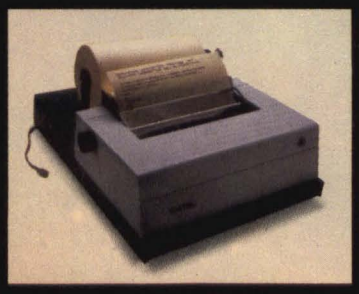

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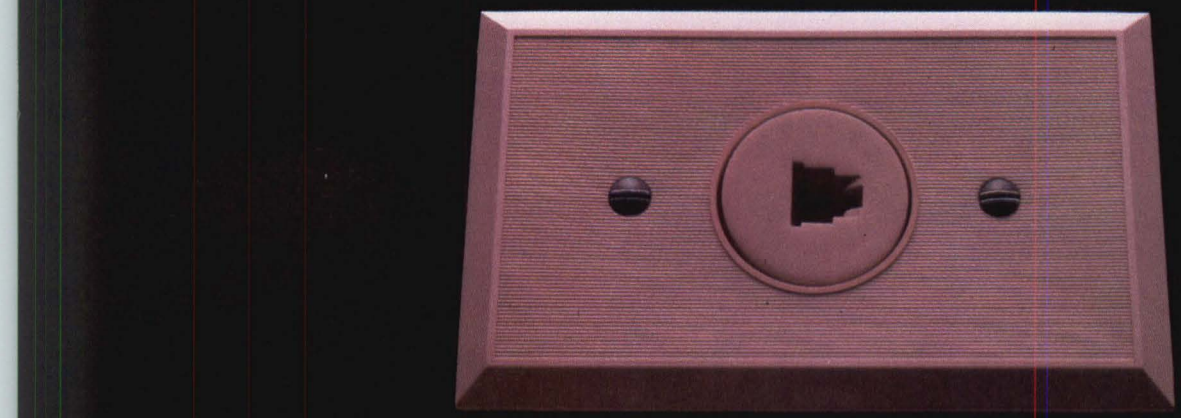

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digitized 1k times each second for long periods of time, then the BASIC interpreter probably would not be able to handle this data rate, while an assembly language program probably could.

Assembly Language/BASIC Benchmarks

As our two benchmarks, two admittedly simple programs are used. The first benchmark program simply reads an 8-bit data value from a peripheral device. The assembly language TEST1 program is listed in Example 1. In this program, register pair H is loaded with a decimal count of 1000. The READ subroutine is then called. When the peripheral device's flag is a logic 1, the 8080 inputs the 8-bit data value into the A register and then returns from the subroutine. When the 8080 does return, the count in register pair H is decremented and then checked to see if it is 0. If it is not 0, the 8080 jumps back to AGAIN so that another data value can be read from the peripheral device. Note that the program does not do anything with the data value read from the peripheral device. This benchmark was written simply to measure the time required to read a value from a peripheral. It is assumed that the peripheral device is a fairly fast one. The equivalent BASIC program is listed in Example 2.

Note that this example does not have any input/output instructions. This is because the BASIC interpreter was not written to directly access the peripheral device. The BASIC program accesses the peripheral device by calling an assembly language subroutine starting at memory location $15{,}000_{10}$. This subroutine is very similar to the READ subroutine in Example 1. Total elapsed time required by either benchmark is divided by 1000 to determine the time required to read a single 8-bit value. For the assembly language benchmark, the time required to read one data value was 46.5 μs; for the BASIC benchmark, 13 ms were required. Using a different BASIC interpreter might cut this time in half.

The second benchmark performs an 11-point "moving average" on an array that contains 256 8-bit data values. The assembly language program requires 165 memory locations for both the program and some temporary storage locations; it is not listed because of its length. The "equivalent" BASIC program is displayed in Example 3. The assembly language version of this benchmark required only 1.5 s to "smooth" the 256 data values in the array, while the BASIC program required 105 s. One notable difference between the two programs is the fact that the BASIC interpreter uses floating point math, so that the values in the array were smoothed as floating point numbers. The assembly language program used integer math subroutines. The initial digital data values were 8-bit values (0.4% accuracy), which do not necessitate the use of floating point numbers. However, this BASIC interpreter (along with most others) can operate only on floating point numbers.

EXAMPLE 2

BASIC Program to Read 8-Bit Values From Peripheral Device

```
10  FOR I=1 to 1000
20  LET A=CALL (15000)
30  NEXT
40  END
```

EXAMPLE 3

BASIC Program to Smooth 256-Entry Array

```
10  DIM A(256)
20  FOR I=1 TO 256
30  LET A(I)=CALL (14000)
31  NEXT
32  LET I=1
33  FOR J=1 TO 8
34  PRINT A(I),
35  LET I=I+1
36  NEXT
37  PRINT " "
38  IF I<257 THEN 33
45  PRINT "ARRAY FORMED"
50  DATA .074, .111, .182, .333, .666, 1,
    .666, .333, .182, .111, .074
55  X=1
60  S=0
61  FOR I=1 TO 11
70  READ C
80  LET S=S+(C*A(X))
90  LET X=X+1
100 NEXT
105 RESTORE
110 LET A(X-6)=S/3.732
120 LET X=X-10
130 IF X<247 THEN 60
135 PRINT "ALL VALUES ARE
    FILTERED"
140 LET I=1
145 FOR J=1 TO 8
150 PRINT %1%,A(I),
155 LET I=I+1
160 NEXT
165 PRINT " "
170 IF I<257 THEN 145
175 END
```

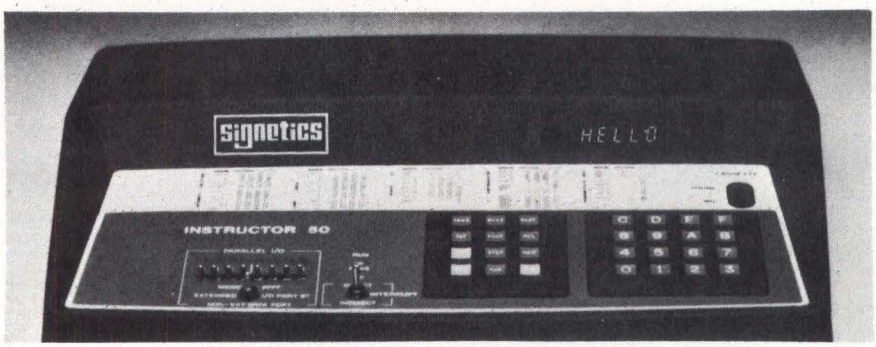
Conclusion

There are a number of points that must be examined when choosing between assembly language or BASIC, both of which have their advantages and disadvantages. Ideally, a user who has the time and money should try to solve particular problems using both assembly language and BASIC, and then choose the best solution. However, since few users have the time or money to do this, a logical compromise is to use benchmarks to point them in the right direction.

In general, if memory costs are of no consequence and relatively slow operation can be tolerated, then BASIC is probably the best choice. If the price of the product that is to use the microcomputer is to be very competitive, then assembly language might to best; it also allows faster execution of the program, as it is not slowed down by an interpreter. As more programmers realize the advantages and disadvantages of both languages, the demand for an efficient compiler language (BASIC, FORTRAN, CONVERS, etc) will increase. In a few years, this may be the way to program the majority of microcomputers.

This article is based, with permission, on a column appearing in *American Laboratory* magazine.

Low Cost Programming Training Aid Simplifies Microprocessor Applications



Instructor 50 microcomputer system is training aid for microprocessor users. Compact unit has user's guide, instructions, and programs prerecorded on audio cassette tape cartridges which can be entered via standard cassette tape player

Instructor 50 is a self-contained training system, designed by Signetics, PO Box 9052, 811 E Arques Ave, Sunnyvale, CA 94086 to provide users with indepth knowledge of how microprocessors function. Beginners are able to make an easy transition into the application of the Signetics 2650 and other microprocessors at a low cost ($350). To facilitate the learning process, step by step instructions and a prerecorded cassette tape are included with each instructor system.

A user's program can be input into the unit via the built-in hexadecimal/functional keyboard. A previously recorded program may be input via the audio cassette interface incorporated in the training system. The loaded program is then executed using debugging aids provided on an internal monitor.

Features of the system are a simple keyboard, an 8-digit display for I/O, and 512 bytes of RAM. An S-100 compatible expansion bus allows additional memory or prototyping cards to be used.

The internal User System Executive (USE) monitor controls the unit with debugging processes: single breakpoint, single step, register examine/alter, memory examine/alter/patch, and cassette load and store.

In operation, the unit enters the monitor when power is applied; following this the user may enter a program (any standard 2650 program), starting anywhere in memory or by issuing a RESET command. One parallel I/O port is available, providing eight switch inputs and eight individual LEDs as a latched output port. A flag/sense serial I/O is also available. Users are able to test the processor sense input, and may learn interrupt operation by issuing the interrupt provided on the function keyboard.

Circle 420 on Inquiry Card

4-Channel D-A Converter For Z80s or 8080s Operates With S-100 Bus

The S-100 bus compatible D-A converter to be used with Z80 or 8080/8085 microprocessors provides 12-bit resolution and uses plug-in hybrid DACs with ±½-LSB accuracy. Power requirements, which meet S-100 bus voltages, are 8 V at 338 mA, 18 V at 122 mA, and −18 V at 156 mA. Input coding may be binary or 2's complement. Conversion speed is 3 μs typ, with replaceable 74-V op amp output.

California Data Corp, 3475 Old Conejo Rd, Newbury Park, CA 91320 has incorporated selectable input and output configurations. Output is 10 or 20 V FS (strap selectable); output range may be ±5, ±10, 0 to 10, or 0 to −10 V. An inversion strap allows decreasing output with increasing input. Output current is 10 mA. Independent gain and offset adjustments are provided.

Circle 421 on Inquiry Card

Z80 Analog Subsystem Acts As Multiplexer, ADC, and Programmable Gain Amp

LLMAP is a single-card analog input subsystem that accepts 32 differential or 64 single-ended low level analog inputs, multiplexes, amplifies by one of seven computer selectable gains, and converts to digital. Compatible with the Zilog Z80 data bus and card cage, the board is offered by Signal Laboratories, Inc, 202 N State College Blvd, Orange, CA 92668 for $895. Featured are onboard space for user signal conditioning (filtering, voltage attenuation, current shunt); 12-bit resolution; ultralow drift; and throughput rates up to 8 kHz.

Circle 422 on Inquiry Card

Second Sourcing Is Agreed Upon for Z8000 16-Bit μProcessor Family

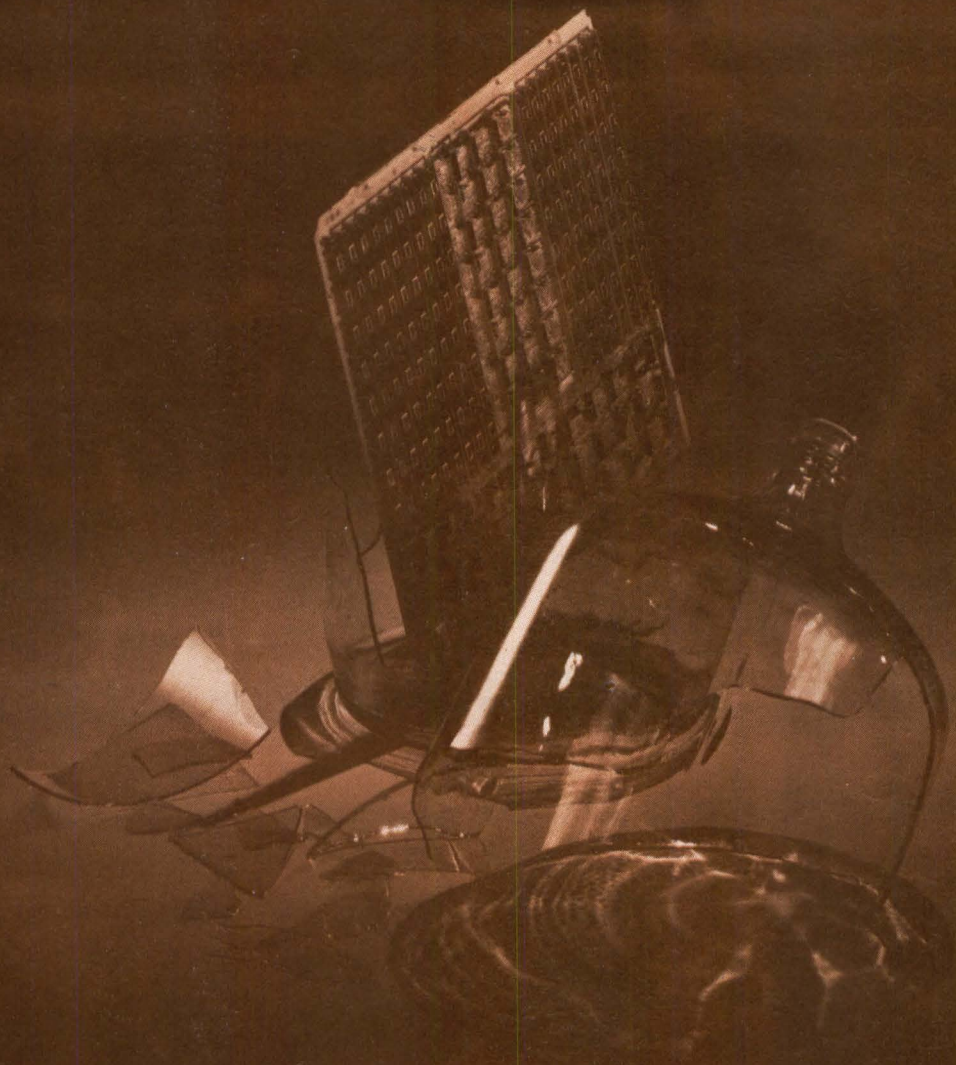
A technical exchange and cross-licensing agreement has been announced between Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086 and Zilog Inc, 10460 Bubb Rd, Cupertino, CA 95014. Under the terms of the agreement, AMD will alternate source Zilog's Z8000 16-bit microprocessor (to be available in the fourth quarter of 1978) and will cooperate on developing support peripheral circuits, thereby promoting the microprocessor and its bus structure. AMD will receive mask sets, in addition to test and other pertinent information.

Development System Integrates Elements Into Compact Station

The Advanced Microcomputer Development System (AMDS) is packaged to combine the microprocessor CPU, 64-key upper/lower case keyboard, and 80-character 12″ (30-cm) CRT display in one terminal, resulting in accessability and mobility. The user has a choice of 8080, 8085, 8086, 6800, 6802, or Z80 microprocessor; from 16k to 64k of dynamic or static RAM is available onboard.

The display is a 24-line, 7 x 9 dot matrix with upper/lower case

Break the Nova 3 bottleneck



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Let's face it. Even the Nova 3/12* has a limited number of card slots. In typical system applications, there just are not enough slots to accommodate needed memory, controllers, and usual options. It's the classic bottleneck and something has to give.

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The 7706 is physically, electrically and functionally compatible with the Nova 3/4 and 3/12.

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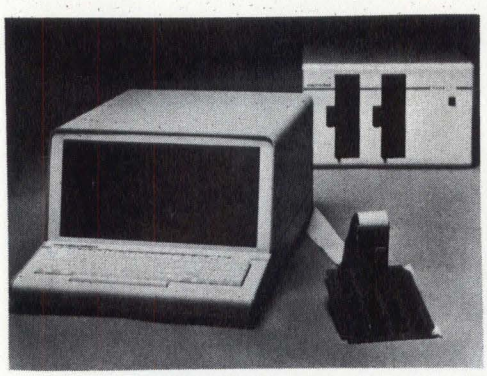


Futuredata Computer Corp has integrated components—CPU, CRT, and keyboard—of Microsystem/31 into one accessible station. As microprocessor development tool, unit provides software and hardware development capabilities

characters, offering blinking fields, reverse video, underlining, highlighting, and line graphics. The keyboard has cursor control keys, edit function keys, system control keys, selectric layout and N-key rollover.

Futuredata Computer Corp, 11205 S La Cienega Blvd, Los Angeles, CA 90045 has designed the Microsystem/31 as a microprocessor development tool with 48k bytes of memory and a 1M-byte double-density floppy disc unit. Hardware development makes use of the Microemulator™ in-circuit emulator and debug packages; software packages include monitors, debuggers, editors, assemblers, utilities, relocatable macro assemblers, linkage editors, and BASIC compilers. The terminal operates with any of the company's disc operating systems.

Circle 423 on Inquiry Card

Processor Board Allows Systems to Be Configured Through Options

Providing functional system support, the ZPU-2 is a 4-MHz, Z80A S-100 bus processor board offered by Xitan, Inc, 1101-H State Rd, Princeton, NJ 08540 with two integral options that may be added later. A user can configure a system immediately and expand the capabilities as needed.

Memory mapping and multitasking registers comprise the system support option. The board allows up to four tasks to run concurrently. More memory may be required by the multitasking function for larger tasks. Up to 1M bytes can be supported. The K series of memory modules in 32k-, 48k-, 64k-, and 128k-byte versions use 16-pin dynamic memory chips to achieve these densities on one S-100 bus size card.

Four DMA channels also supplied by the option allow I/O data transfer rates of 2M bytes/s. Complete interrupt control is provided for eight input lines under software control. This portion also furnishes three programmable timers providing clocked pulses at intervals ranging from 1 μs to 1 s.

A floating point option adds mathematical processing capabilities performed at increased speeds, since a separate processor handles these tasks leaving the main board free to perform other functions. This increases capabilities while reducing software overhead.

The board operates at 2 or 4 MHz (switch selectable). Wait state generation is provided separately on memory, DMA, and I/O operations.

Circle 424 on Inquiry Card

Power Modules Have Multiple Outputs for µProcessor Applications

Triple MT series and quadruple MQ series power supplies for microprocessor process controllers, shift registers, and RAM/ROM arrays plug in for PC board applications; chassis mounts and 7-terminal trip modules are available. All models operate from 115 Vac with 230 Vac optional.

AAK Corp, PO Box 7, Methuen, MA 01844 has supplied the 5-Vdc output with currents ranging from ±500 to ±2000 mA; −5 Vdc at −100 mA is available on quad output series. Output currents of ±12 or ±15 Vdc range from ±100 to ±300 mA. Altered voltages and currents may be requested.

Other specs include line/load regulation of 0.1% for 5 Vdc, and 0.05% for ±12, ±15 Vdc. Ripple and noise is 1 mV rms.

Circle 425 on Inquiry Card

SOFTWARE

Software Supports Development Capabilities of Low Power CMOS 1802

Microprocessor based systems requiring low power consumption for such uses as military and industrial applications can be developed with the 1802 CMOS microprocessor, utilizing the Tektronix 8002 microprocessor development system. The 1802X cross assembler software package offered by Xetron Corp, 11079 Reading Rd, Cincinnati, OH 45241 translates programs written using symbolic notation into executable machine code using the development system's hardware.

Directives and input format guidelines are the same for both the assembler and the Tektronix assembler program. Capabilities of flexible comment, spacing, and paging, and extensive error diagnostics aid program creation.

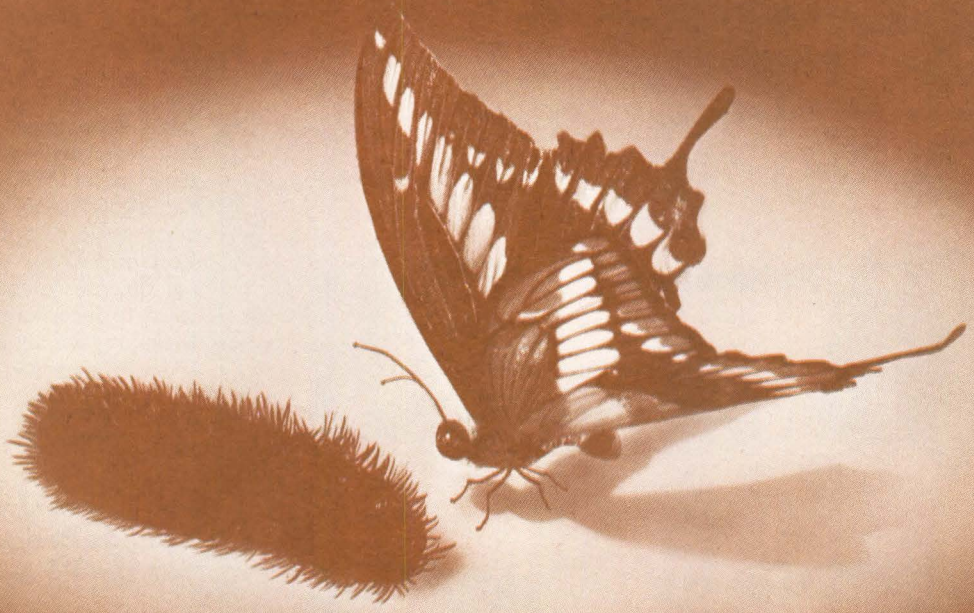
Circle 426 on Inquiry Card

Memory Manager Allows Implementation of Reentrant Code for 6800

INNOVA-STAK is a software development tool for programmers to use in situations that require reentrant code, eg, routines to be stored in ROM, recursive programs, and management of interrupt driven facilities. Incorporated into user code, it occupies less than 400 bytes of memory.

PUSH and POP are the two stack handling routines contained in the memory manager to provide a standard interface between user subrou-

Formula for memory metamorphosis



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Other versions of the MICRORAM 3400 Series are available in 16 to 22 bit configurations, 8 to 32K capacities, and access times as low as 180 nsec.

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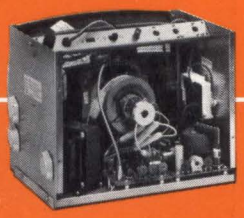

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tines. They employ a pushdown stack discipline to allocate and free memory as required, pass parameters, and perform error checking to assure the stack's integrity and detect program failures as early as possible.

Intended for M6800 microprocessors, the distribution package has a user's manual, sample validation program, and an MDOS diskette with routines in relocatable format, assembly language macros for stack initialization and for standard calling and receiving sequences. Innova Systems Inc, 115 E Main St, New York, NY 10003 also plans to introduce versions for other microprocessors. Cost of $35 for package and perpetual license includes permission for users to incorporate the manager into their programming products.

Circle 427 on Inquiry Card

High Level Language Speeds Programming for the R6500 Family

Designers can develop programs for the R6500 microprocessor family with increased productivity and reduced software development time and costs using PL/65. Resembling PL/1 and ALGOL, the high level language supports modular program design. It can be used for structured programs due to the general control structures for conditional and iterative looping.

The compiler, available to SYSTEM 65 users as a preprogrammed minifloppy diskette from the Electronic Devices Div of Rockwell International, 3310 Miraloma Ave, PO Box 3669, Anaheim, CA 92803, outputs source code to the resident assembler. Enhancing or debugging can be done at the assembler level before object code is generated. PL/65 statements may be mixed with assembly language instructions for timing or code optimization. For PDP-11 users, a PL/65 compiler and R6500 cross assembler are available using the RT-11 operating system.

Other features include assignment, integer arithmetic, conditional and collective execution, linear array manipulation, data area declaration, and array initialization. Block structures, subscripts, and parenthetical expressions are also supported. □

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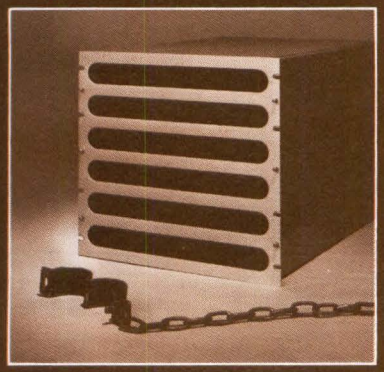

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IEEE 488: A PROPOSED MICROCOMPUTER I/O BUS STANDARD

Bert E. Forbes
Ziatech Corporation
Cupertino, California

The importance of one standard, plug compatible, input/output bus for microcomputers must be emphasized, as cost savings in design time for engineers, in development time for manufacturers, and in systems integration time for users would be dramatic. Of course, a single bus cannot be optimum for every application, but the benefits of standardization far outweigh the disadvantages. A standard bus would increase the usage of microcomputers through increased availability of peripherals and through enhanced competition. The IEEE Standard 488-1975 Bus,[1] commonly called the General Purpose Interface Bus (GPIB) or Hewlett-Packard Interface Bus (HP-IB),[2] is already widely accepted in the instrumentation field, and is therefore the logical choice.*

Two key factors governing the acceptance of a bus standard are how well the bus matches the needs of an input/output (I/O) bus, and how easily a hardware device or peripheral interfaces to the bus. The Listing enumerates the salient characteristics of the GPIB as a microcomputer I/O bus. Each characteristic will be examined from the viewpoint of a general I/O bus.

Data Rate—Most microcomputer systems utilize peripherals of differing operational rates, such as floppy discs at 31k or 62k bytes/s (single or double density), tape cassettes at 5k to 10k bytes/s, and cartridge tapes at 40k to 80k bytes/s. In general, the only devices that need high speed I/O are 0.5" (1.3-cm) magnetic tapes and hard discs, operational at 30k to 781k bytes/s, respectively. Certainly, the 250k-byte/s data rate that can be easily achieved by the IEEE 488 bus is sufficient for microcomputers and their peripherals, and is more than is needed for typical analog instruments. The 1M-byte/s maximum data rate is not easily achieved on the GPIB and requires special attention to considerations beyond the scope of this article. Although not required, data buffering in each device will improve the overall bus performance and allow utilization of more of the bus bandwidth.

Multiple Devices—Many microcomputer systems used as computers (not as components) service from three to seven peripherals. If a nonbus protocol such as the RS-232 were chosen,[3] each device would need a separate "channel" controller. With the GPIB, up to 8 devices can be handled easily by 1 controller; with some slowdown in interrupt handling, up to 15 devices can work together. The limit of 8 is imposed by the number of unique parallel poll responses available; the limit of 15 is set by the electrical drive characteristics of the bus. Logically, the IEEE 488 Standard is capable of accommodating more device addresses.

Bus Length—Physically, the majority of microcomputer systems fits easily on a desk top or in a standard 19" (48-cm) rack, eliminating the need for extra long cables. The GPIB is designed typically to have 2 m of length per device, which accommodates most systems. A line printer might require greater cable lengths, but this can be handled at the lower speeds involved by using extra dummy terminations. Several manufacturers produce GPIB to RS-232 adapters that may be used to extend bus length at some sacrifice in speed.

Byte Oriented—The 8-bit byte is almost universal in I/O applications; even 16- and 32-bit computers use byte transfers for most peripherals. The 8-bit byte matches the ASCII code for characters and is an integral submultiple of most computer word sizes. The GPIB has an 8-bit wide data path that may be used to transfer ASCII or binary data, as well as the necessary status and control bytes.

Block Multiplexed—Many peripherals are block oriented or are used in a block mode. Bytes are transferred in a fixed or variable length group; then there is a wait before another group is sent to that device, eg, one sector of a floppy disc, one line on a printer or tape punch, etc. The GPIB is, by nature, a block multiplexed bus due to the overhead involved in addressing various devices to talk

*Hewlett-Packard recently announced the HP300 and HP3000 series 33 that use the HP-IB as the I/O bus for these powerful computers.

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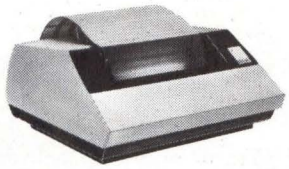

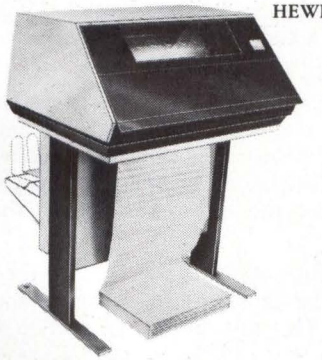

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model 6046 (single controller/2 drive).
model 6047 (single controller/3 drive).
model 6048 (single controller/4 drive).

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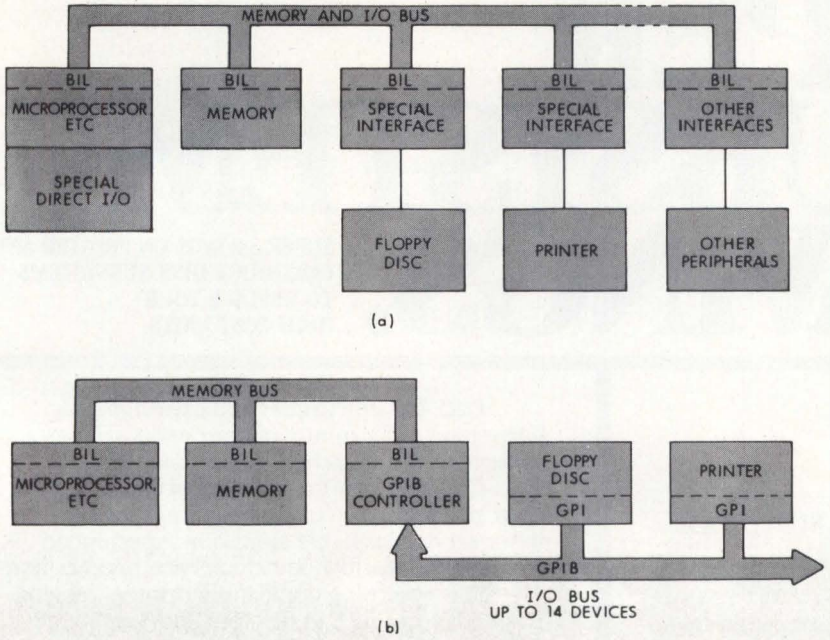

Microcomputer interfacing. With traditional I/O (a), all communications between modules occur on high speed memory bus. Each I/O module has some bus interface logic (BIL) and other specialized logic for particular I/O device, necessitating separate device design. In addition, each device would require a different interface card for each microcomputer backplane. When GPIB is used as I/O bus (b), each device contains general purpose interface (GPI) logic consisting mainly of one LSI IC (Motorola 68488 or Intel 8291) and uses standard IEEE 488 cable to connect to any microcomputer with GPIB controller. This allows shorter memory bus with fewer card slots, as well as easily expanded, uniformly interfaced I/O system

and listen. This overhead is less bothersome if it only occurs once for a large number of data bytes (once per block). This mode of operation matches the needs of microcomputers and most of their peripherals. Because of block multiplexing, the bus works best with buffered memory devices.

Interrupt Driven—Many types of interrupt systems exist, ranging from complex, fast, vectored/priority networks to simple polling schemes. The main tradeoff is usually cost versus speed of response. The GPIB has two interrupt protocols to help span the range of applications. The first is a single service request (SRQ) line that may be asserted by all interrupting devices. The controller then polls all devices to find out which wants service. The polling mechanism is well defined and can be easily automated. For higher performance, the parallel poll capability in the IEEE 488 allows up to eight devices to be polled at once—each device is assigned to one bit of the data bus. This mechanism provides fast recognition of an interrupting device. A drawback is the frequent need for the controller to explicitly conduct a parallel poll, since there is no equivalent of the SRQ line for this mode.

Direct Memory Access (DMA)—In many applications, no immediate processing of I/O data on a byte-by-byte basis is needed or wanted. In fact, programmed transfers slow down the data transfer rate unnecessarily in these cases, and higher speed can be obtained using DMA. With the GPIB, one DMA facility at the controller serves all devices. There is no need to incorporate complex logic in each device.

Asynchronous Transfers—An asynchronous bus is desirable so that each device can transfer at its own rate. However, there is still a strong motivation to buffer the data at each device when used in large systems in order to speed up the aggregate data rate on the bus by allowing each device to transfer at top speed. The GPIB is asynchronous and uses a special 3-wire handshake[2] that allows data transfers from one talker to many listeners.

I/O to I/O Transfers—In practice, I/O to I/O transfers are seldom done due to the need for processing data and changing formats or due to mismatched data rates. However, the GPIB can support this mode of operation where the microcomputer is neither the talker nor one of the listeners.

Uniform Device Protocol—For ease of use in a system, every device should look the same to the software and to the I/O driver routines. This goal is seldom met in a microcomputer system, and the GPIB is no improvement. However, an IEEE committee is working on documentation to help this situation: "IEEE Recommended Practice: Code and Format Conventions (for use with IEEE Standard 488-1975)." The problem is that many devices exist with widely varying approaches that are not strictly "IEEE 488 compatible."

High Level Interface Language—The designer should be able to perform I/O in terms of moving blocks of data without having to completely understand the entire bit level protocol of the bus. The GPIB is difficult to interpret in this respect. Therefore, specialized bus controllers have been designed to overcome this difficulty. For example, the Ziatech ZT 80 controller for the GPIB has adopted a high level interface language that provides complete access to the bus without having to specify each step of the control sequence needed to use the GPIB. High level instructions executed by the controller handle all addressing needs to talk and listen, byte counting and character recognition, and interrupt polling independent of the microprocessor central processing unit (CPU).

EXORterm 220

It's Motorola's "total" 2 MHz 6800 development system

EXORterm* 220 combines the necessary display terminal with the system development capability of the EXORciser*II, creating a single, more reliable and less expensive, easy-to-use, compact unit.

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EXORterm 220 software includes the resident relocatable macro assembler/linking loader and CRT editor. High level languages available include MPL, FORTRAN, and COBOL compilers, and a BASIC Interpreter.

EXORterm 220 is designed for software and hardware system development for all Motorola and second source M6800 Family microprocessors and single-chip microcomputers operating at speeds up to 2.0 MHz. It also adapts for use with the single-chip MC3870, single-chip MC141000, and the M10800 and 2900 bipolar 4-bit slice families.

EXORterm 220 rounds out the Motorola development-system line started by the EXORciser,* updated by the EXORciser II, and anchored recently by the 1 MHz EXORterm 200 — the economical, compact system for those who don't require the 2 MHz speed and dual-memory map compatibility of the EXORterm 220. Supplemented by appropriate software, Motorola disk operating system, and EXORprint*II printer, they also create the M6800 Software Development Station.

For technical information on Motorola's "total" 2 MHz development system, circle the reader service number or write to Motorola Microsystems, P.O. Box 20912, Phoenix, AZ 85036. For in-depth information on Motorola's complete system development support, contact your authorized Motorola distributor or Motorola sale office.

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MOTOROLA

Semiconductor Group

Major Characteristics of GPIB as Microcomputer I/O Bus

Data Rate
- 1M bytes/s, max
- 250k bytes/s, typ

Multiple Devices
- 15 devices, max (electrical limit)
- 8 devices, typ (interrupt flexibility)

Bus Length
- 20 m, max
- 2 m/device, typ

Byte Oriented
- 8-bit commands
- 8-bit data

Block Multiplexed
- Optimum strategy on GPIB due to setup overhead for commands

Interrupt Driven
- Serial poll (slower devices)
- Parallel poll (faster devices)

Direct Memory Access
- One DMA facility at controller serves all devices on bus

Asynchronous
- One talker
- Multiple listeners
- } 3-wire handshake

I/O to I/O Transfers
- Talker and listeners need not include microcomputer/controller

Uniform Device Protocol
- IEEE standardization in progress

Higher Level Language for Interfacing
- Maps directly onto bus capabilities
- Requires intelligence on controller

System Configuration: Traditional vs GPIB

The memory bus in a traditional microcomputer organization [see Figure, part (a)] is used for all communications between modules. It typically consists of an 86- to 122-pin printed circuit card edge connector for each board. Bus interface logic (BIL) necessary for communications requires 10 to 15 logic dual-inline packages for a slave interface that cannot initiate transfers (memories, I/O boards, etc), and even more logic for a master interface (DMA, processors, etc). Each peripheral device must have a separate interface card for each microcomputer memory bus.

The designer must also expend extra effort in configuring the system because each board must be explicitly accounted for in memory (or I/O) address space. Each device interface also has a unique access protocol that must be learned in addition to the device characteristics.

A long memory bus can present timing and noise problems as each new device is added. This is not a problem for small systems, but large systems must use carefully designed backplanes. Also, a physical bottleneck evolves with all the device cables attaching to their special interface card. Each cable is separate, adding extra cost and problems for their manufacture and test.

DMA is difficult in this bus configuration. Each interface must have its own DMA logic onboard and be a bus master, or each interface must be designed to work with a common but separate DMA board, which requires extra cabling and multiplexing. This style of system bus configuration is far from optimum for either the peripheral manufacturer or the system designer.

Part (b) of the Figure shows a system using the GPIB as the standard I/O bus. The high performance memory bus can be shorter and used in a more uniform manner, since only the memory and GPIB controller need to use this bus. The single GPIB controller can handle large systems of up to 14 devices before another controller must be added to the memory bus. DMA is easily accommodated —only the controller needs extra logic.

General purpose interface (GPI) logic is embedded in the control logic of each device, which is self-contained and can easily be connected to any system with a GPIB controller. This results in lower design costs for the manufacturer and easier, more uniform interfacing for the designer and user. Special cables are not needed, as the IEEE 488 Standard specifies the cable and connector characteristics. Many cable configurations are possible, ranging from daisy-chain to star connections. Total bus length must be less than 20 m which is adequate for most microcomputer systems.

Strong support for establishing a standard I/O bus is the ease of test and verification by both manufacturers and designers. The problems of incoming inspection, maintenance, and test fixtures, for example, are substantially reduced because only one interface is needed; also, CPU independent test programming is possible. This emphasizes the need to establish the next higher level of software standards for use with microcomputer peripherals on the GPIB, allowing even easier testing and use.

The GPIB controller can utilize an onboard microprocessor to enhance the system throughput and the level of interaction with the designer, as done in the ZT 80. The microprocessor can interpret the high level instructions and implement a simple multitasking monitor that keeps track of priority ordered GPIB programs.

Summary

Certainly, an I/O bus standard is needed in the microcomputer field.** The technology is available to allow easy GPIB implementations, and the GPIB has adequate flexibility and data rates to fit most microcomputer I/O requirements. In addition, the GPIB would furnish the following benefits:

(1) Microcomputer designers would have to implement only one I/O interface, saving both design time and cost.

(2) Peripheral manufacturers would need to develop only one type of device interface, thereby lowering cost.

(3) Users would have to learn only one protocol, saving time; they would also have easier testing and lower investment in tooling.

(4) Users would also have the capability to easily and quickly add instruments and peripherals to their systems.

References

1. Institute of Electrical and Electronics Engineers, "IEEE Standard 488-1975, Digital Interface for Programmable Instrumentation," New York, NY, 1975
2. Hewlett-Packard Co, *Hewlett-Packard Journal*, Palo Alto, Calif, Jan 1975
3. Electronic Industries Association, "EIA RS-232-C, Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange," Washington, DC, Aug 1969

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Portable Instrument Analyzes and Tests Z80 and Z80A Microprocessor Based Systems

MicroSystem Analyzer with emulation capability packaged in pod (at right) provides in-circuit emulation, signature analysis, and time domain analysis for products employing Zilog 4-MHz Z80A or 2.5-MHz Z80 microprocessors. Lightweight, portable test instrument from Millennium Systems operates under design/debug, production test, and field servicing conditions

Capabilities of in-circuit emulation, signature analysis, and time domain analysis are combined in the portable MicroSystem Analyzer (μSA) for automatic functional testing and fault detection in Z80 and Z80A based systems, up to the full 4-MHz clock speed possible with the microprocessor. System support is provided in the laboratory as a development system, in production as a full production tester, in repair depots as a diagnostic tool, and in the field as an analyzer. Cost of board replacement is reduced since the tool immediately identifies during field services those boards which are still good.

The analyzer serves as a complement to microcomputer development centers for the Z80. Test and diagnostic programs developed on these centers or other computers are transferred to P/ROMs in the analyzer. The tool can take online control of a manufacturer's system under test, monitor the system program, and display register contents and other information. Fault readouts are in a 20-character English display; fault locations can be identified through customer supplied diagnostic programs.

Under emulation, the analyzer is transparent to the system, without induced noise or delay. A plug fitting the microprocessor socket handles all Z80 functions provided by in-circuit emulation. These include setting hardware breakpoints, stepping through program instructions, and detecting faulty hardware and software logic by alternating CPU register, memory, and I/O values.

With signature analysis, node probing for good hexadecimal values locates component level faults. Repeatable stimuli that emerge as bit streams at the nodes are applied through the emulator. These bit streams are compressed by polynomial code generation technology to assure operator intelligible readout and a fault detection probability of 99.998%.

The final capability of time domain analysis covers pulse width, pulse interval, and frequency measurement as well as pulse and transition counting for cases in which the clock is inoperable or no system clock is included.

While Millennium Systems, Inc, 19020 Pruneridge Ave, Cupertino, CA 95014 has previously announced an analyzer system for the 8080 and 6800 (see *Computer Design*, Dec 1977, p 124), the Z80 analyzer can also be used for 8080 and 6800 based systems with the addition of extra cost, optional personality boards. Unit price is $2750 with alternate microprocessor emulators and signature analysis option priced at $1000.
Circle 429 on Inquiry Card

Additional System Further Enhances OEM Applications

Built around the PDP-11/03-L microcomputer, the PDP-11V03-L is the latest addition by Digital Equipment Corp, Maynard, MA 01754 to its L System line (see *Computer Design*, Aug 1978, p 148). Housed in a 31″ (78.7-cm) tall cabinet, the self-cooled unit can be used in standard work areas, adapting to a variety of environments. The universal power supply converts between 115 and 230 Vac at 46 to 63 Hz.

The processor has 32k bytes of MOS memory, space for up to 32k bytes of ROM or UV P/ROM, bootstrap loader, and system diagnostics. The RX02 dual density diskette system supplies a maximum storage of 1.2M bytes; a compatibility feature allows single-density diskettes to be used for data recovery or storage under program control. Choice of hardcopy or video terminals is available.

Standard software is the RT-11 operating system, editor, macro assembler, and utilities. High level languages are optional. The system also has an extended floating point instruction set. Prices start from $10,500.
Circle 430 on Inquiry Card

16-Bit Single-Board Computer Contains Nonvolatile Memory

The general purpose Mini-Mizer 100 series OEM computer is capable of performing industrial automation, small business system, and instrumentation functions, among others. The 16-bit high performance multiple general register architecture, similar to that of the Digital Equipment Corp PDP-11 is contained on a single 12 x 17″ (30 x 43-cm) PC board.

Each computer is partitioned into three types of semiconductor memory. RAM contains 32k bytes with a totally transparent refresh scheme. The memory protection scheme partitions the RAM into 4k-byte pages that are opened or closed by operating system service requests. P/ROM comprises the second section containing sockets for up to 28k bytes of UV P/ROM. Of this memory, 8k bytes are used by the resident operating system supplied with the unit. A full 20k bytes of P/ROM and 32k bytes of RAM are available to the user for application

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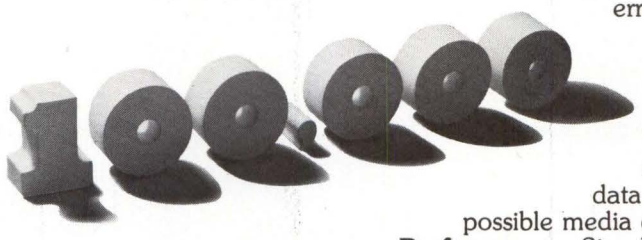
A year ago we introduced our minifloppy, we frankly didn't expect the revolution that was about to happen. Now we've delivered 100,000 units and our production experience allows us to pass along a nice 15% price reduction. Naturally, we are flattered by the acceptance the little drive has received (and by all the imitations). There are a lot of good reasons why our minifloppy has been accepted as number 1.

35 Tracks. A format with a future. The minifloppy provides fast, random access to the industry accepted 35 recording tracks. This format will help you grow *compatibly* and reliably into double density and double sided recording later, when you are ready. The compact minidiskette® media carries 110 KB of information. **Reliable Storage.** The Shugart minifloppy drive has the proven mechanical reliability and data integrity of standard flexible disk drives. It reads and writes with the same glass bonded ferrite/ceramic head used in Shugart's standard-sized SA800 flexible disk drives. Die cast construction offers high mechanical integrity. A DC drive motor with precision servo speed control using an integral tachometer eliminates AC power requirements. The unique stepping motor actuator uses a direct drive spiral cam with ball bearing V-groove positive indent. This assures perfect head registration every time.

Data Integrity. The Shugart minifloppy drive improves error rate by two orders of magnitude compared to cassettes. Soft errors are only one in 10^8, and seek errors one in 10^6. Write protect circuitry prevents loss of recorded information. It's standard with every Shugart SA400. The minidiskette media is recorded at 20% less density than our standard floppy. This generous safety margin is your assurance of data integrity and the lowest possible media costs.



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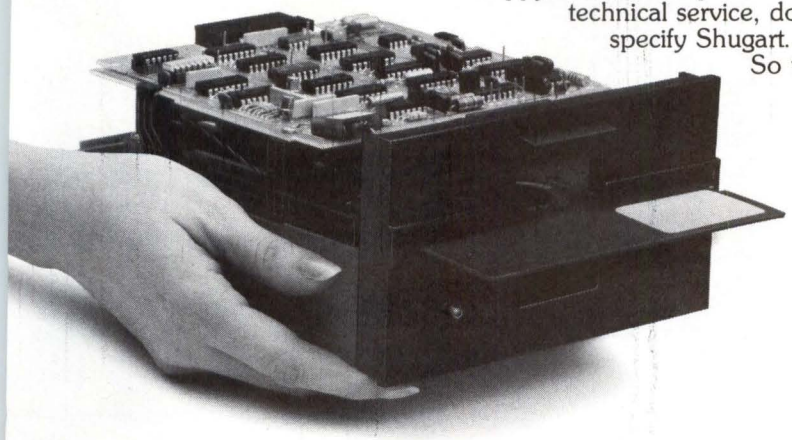
Inexpensive Storage. Applying floppy technology in a compact size reduces OEM and end user cost. And with our recent 15% price reduction minifloppy disk storage has never been more affordable. Small drive size (5.75″ wide, 3.25″ high and 9.0″ deep) reduces total system cost. Low unit weight of three pounds offers OEM system designers new application opportunities, too. Low power consumption. **The SA4400 ministreaker™ Controller.** The SA4400 ministreaker controller controls up to three minifloppy drives, providing up to 241.8 kilobytes of on-line data storage. **Support.** Shugart has made the floppy smaller and product support bigger. We give you more support—systems design, technical service, documentation and applications help. Two out of three OEM's specify Shugart. They get more experience, more technology, more support. So talk to number one in low cost disk storage. Talk to Shugart.



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CIRCLE 91 ON INQUIRY CARD

programs or program development software.

The third type of memory is a 2k-byte block of electrically alterable, nonvolatile ROM that effectively acts as a block of nonvolatile RAM. The CPU issues read and write requests to this memory to store and retrieve system data without regard to power outages. In addition, the CPU under operating system control automatically saves and retrieves the processor state in the nonvolatile memory on power down and auto restart cycles. Nonvolatile memory requirements of many system applications are met without the need for batteries.

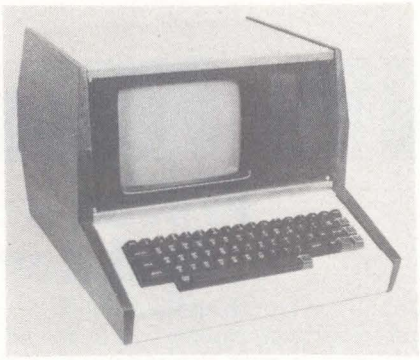
Other features of the card are a controller for dual, high speed digital cassette drives (1k bytes/s); a programmable serial line controller with speeds from 110 to 19.2k baud; programmable realtime clock with 16 selectable rates; up to 6 programmable event timers; software programmable memory protection and allocation register; and 32 general purpose I/O lines for user interface functions. In OEM quantities of 10 or more, the system costs $995. Stynetic Systems, Inc, Flowerfield Industrial Pk, St James, NY 11780 later plans to introduce a version with a dual floppy disc controller and serial communication channel, and possibly one with 64k bytes of RAM on a single board.

A P/ROM resident Executive Program supports the series with conventional command structures, online debug programs, relocating loader, device I/O utilities, interrupt handlers, realtime clocks, extended math functions, file and data management routines, etc. Capable of supporting program development and debugging are such development tools as assemblers, text editors, relocating linking loaders, object module linkers, and debug aids. Programming may be done in BTRAN[R], a high level language combination of BASIC and FORTRAN that maintains the execution speed and memory efficiency of assembly language.

Circle 431 on Inquiry Card

Video Computer Stands Alone, as Intelligent Terminal, or RJE Station

A Z80A microprocessor, minifloppy disc storage drive, 48k RAM, and



high speed video terminal comprise a 12 x 15 x 18″ (30 x 38 x 46-cm) computer for business or OEM applications. It serves as a standalone computer, or may be used with others as an intelligent terminal or remote job entry station.

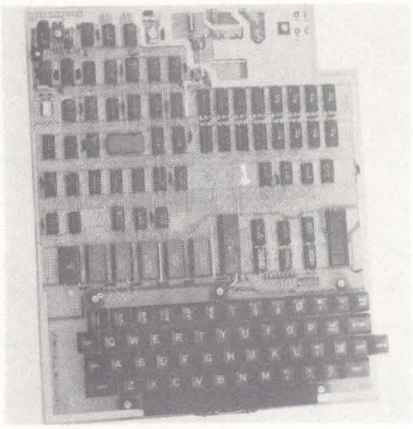
Video display is 25 lines x 80 characters including 96 upper and lower case characters and a 32-character line drawing and graphics set. Also featured are 48k of RAM, two serial I/O interfaces with programmable baud rates to 9600, parallel port for Centronics or Qume printers, lightpen port, and 67-key keyboard. As options, Zeda Computer Systems, 1662 W 820 N, Provo, UT 84601 offers two additional drives, two or four standard floppy drives, lightpen, numeric or function keypad, 10k of RAM, and software packages.

Circle 432 on Inquiry Card

Use of LSI Circuits Reduces Computer To Single Board

Superboard II design makes use of custom LSI circuits to fit the complete microcomputer system on one board. The range of features includes 8k of BASIC in ROM, up to 8k of static RAM, a 6502 microprocessor, full 53-key computer keyboard with upper/lower case and user programmability, Kansas City standard audio cassette interface, and full machine code monitor and I/O utilities in ROM. Direct access video display interface with an additional 1k of dedicated memory has upper case, lower case, graphics, and gaming characters for a screen resolution of up to 256 x 256 points. Display of normal TVs with overscan is about 24 rows of 24 characters; without overscan it is up to 30 x 30 characters.

Options that Ohio Scientific, Inc, 1333 Chillicothe Rd, Aurora, OH 44202 offers are an expander board with 24k of RAM, dual minifloppy interface port adapter for printer and



Computer system, Superboard II from Ohio Scientific, features single-board construction. It is comprised of microprocessor, memory, 53-key keyboard, and video display and audio cassette interfaces. Board may also be enclosed in case with onboard power supply

modem, and a 48-line expansion interface. An assembler/editor, extended machine code monitor, and software library also are available. A 5-Vdc, 3-A supply is required to power the board. Retail price is $279. Packaged as the Challenger 1P with power supply and case, the unit costs $349.

Circle 433 on Inquiry Card

Probe Subsystem Extends Troubleshooting to 8085 Microcomputer

Broadening the troubleshooting applications range of the μScope™ 820 microprocessor system console to cover 8085 and 8085A microprocessors as well as the 8080A, Probe 8085 connects the console to the system under test (SUT) via the microprocessor socket. The microprocessor, which is removed from the socket and plugged into the probe, continues to operate during the testing; thus, total system operations can be diagnosed. The SUT can run in realtime due to the sense and buffer circuits.

Various capacities are filled by the test instrument. Execution of automatic diagnostic programs on the

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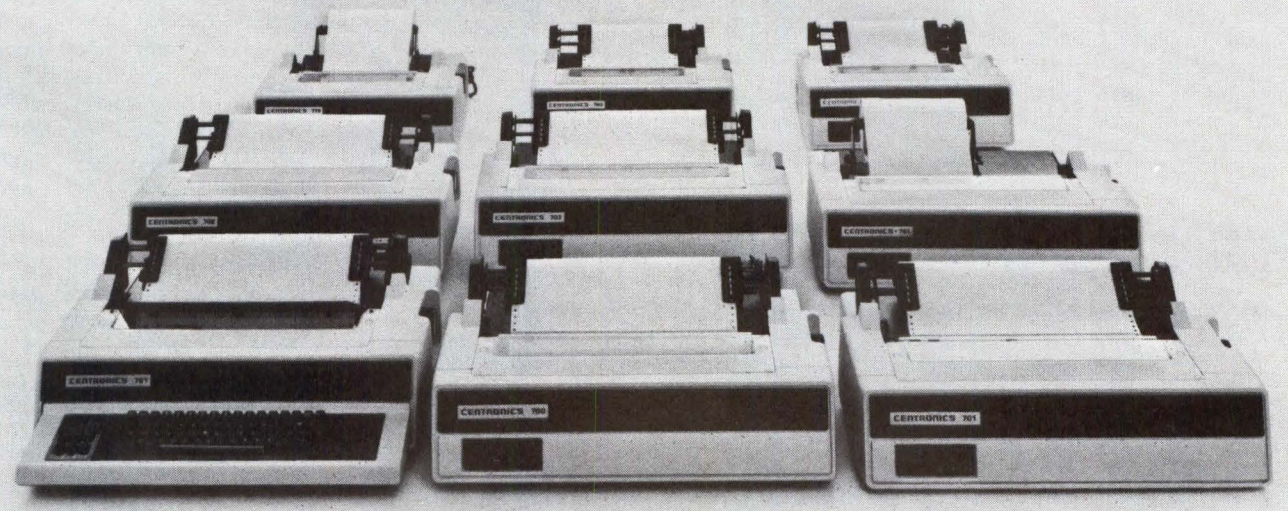

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Probe 8085 connects with Intel's μScope 820 system console to provide portable diagnostic instrument for troubleshooting microcomputer systems in both lab and field

8085 system simplifies fault isolation. Detailed troubleshooting mode is entered via the console's 32-bit wide breakpoint, 128-byte overlay RAM, and 256-level machine cycle trace memory. Once a fault is isolated to a peripheral or subsystem, the trace memory and breakpoint can locate the problem. Finally, the actual program flow can be examined.

Four user positioned accessory probes further extend the console to such applications as detecting a hardware interrupt signal, single stepping through the interrupt service routine, recording a data pattern, or reading back the digital state of any SUT.

Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 supplies the probe with a keyboard display overlay and personality ROM. Also included in the package are the probe buffer box and accessory test probes. As a kit, the console and probe cost $2795; separately the probe costs $825.

Circle 441 on Inquiry Card

Multiple Arithmetic Processor Speeds Complex Math Operations

Speeding and easing arithmetic operations in the areas of realtime process control, scientific computation, and multiuser systems, the 8008 arithmetic processor provides the company's microcomputer systems with arithmetic and trigonometric functions in a 32-bit floating point format. The processor can be expanded to use up to four Am9511 devices. Each is separately addressable for parallel processing or multiuser systems.

GNAT Computers Inc, 7895 Convoy Ct, Unit 6, San Diego, CA 92111 has equipped the general purpose arithmetic board with an 8253 programmable interval timer. Enhanced interrupt control for increased utility eases multitask functions. A high speed option, twice as fast as the standard board, is available.

Circle 442 on Inquiry Card

Boards Expand Memory of PET Microcomputers

Memory of the Commodore PET computer can be expanded in increments of 16k, 24k, or 32k bytes with the PME memory board from Computer Mart Systems, 13 E 30th St, New York, NY 10016. Delivered with all necessary hardware, the board installs inside the microcomputer. The onboard power supply derives power from the computer's transformer through a jumper cable. The 24k version allows programs to be written to the total capacity of the computer; the 32k model permits storage of protected machine language programs and displays.

Use of dynamic RAMS maintains extremely low power dissipation. Under worst case conditions, the 32k configuration requires less than 2.7 W. Timing is referenced at the computer's expansion memory connector; refresh is performed automatically and transparently, without slowing the CPU. A BASIC memory test is included; an optional machine language memory test shows defective memory locations on the computer's screen.

Circle 443 on Inquiry Card

Power Is Added to Z80/8080 Microcomputers With Floppy Disc System

Features of the V500 series floppy disc system that provide Z80/8080 microcomputers with more power include 512k bytes of online storage; instantaneous program loading and dumping; file management with random access; context editing of programs and text; dynamic debugging of programs; program assembly; and batch processing. The system includes two floppy disc drives enclosed in a case with power supply, fan, and power switch; an S-100 bus controller card that plugs into the computer and controls up to four drives; an I/O cable to connect the controller to the drives; and system software—CP/M (VOS) disc operating system and BASIC-E compiler—recorded on 8″ (20-cm) diskettes.

With the CP/M from Vista Computer Co, Dept P1, Torrance, CA 90503, up to 64 dynamically allocated, named files can be stored on each diskette. Files may be any length up to 250k bytes maximum. Files can be transferred back and forth between the user's disc and Tarbell cassette or other devices. Duplicate files may be copied onto backup diskettes.

Circle 444 on Inquiry Card

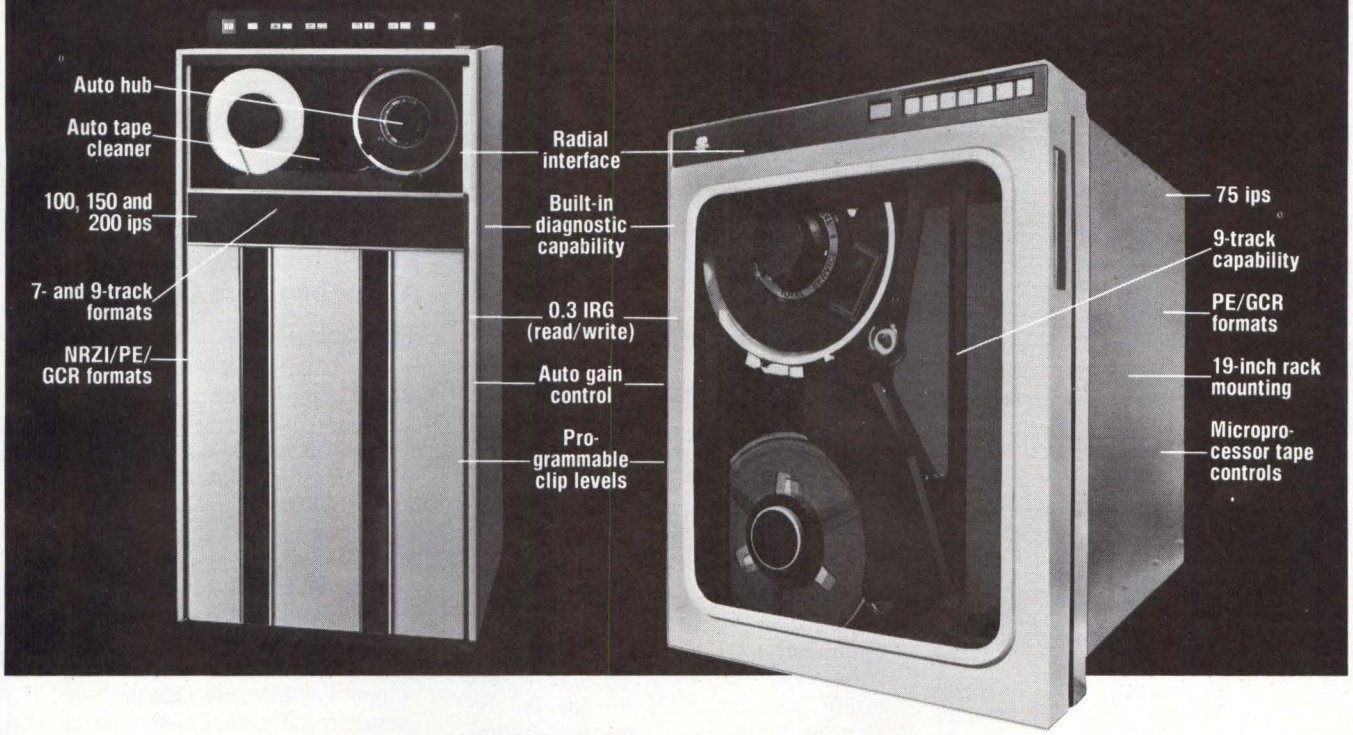
Family of 8″ Floppy Disc Systems for M6800 Based Computers

A family of floppy disc drives consisting of three systems for microcomputers based on the M6800 microprocessor has been introduced by Smoke Signal Broadcasting, 6304 Yucca St, Hollywood, CA 90028. Model LFD-1 is a single-drive, single-side, single-density system; model LFD-2 is a dual-drive, single-side, single-density system. Both use the Shugart SA-800 drive. Based on the Shugart SA-850 drive is model DFD-2, a dual-drive, double-sided, single-density system. Prices are $1395, $1895, and $2495, respectively.

Each includes a disc controller board capable of driving up to four disc drives, regulated power supply, chassis, cooling fan, diskette, and interfacing cables. The disc operating system (DOS-68) and disc file BASIC (DFB-78) are compatible with the company's existing software, requiring no software changes.

Circle 445 on Inquiry Card

Now...two OEM tape drives with GCR performance and CDC quality.



Once, the advantages of GCR recording were available only with large mainframes.

But now, minicomputer manufacturers have a choice of two transports from Control Data. Both provide GCR's exceptional data integrity and transfer rates consistent with today's high density disk systems.

Our new ATS-III and its companion formatter answer the need for cost-effective 75 ips GCR/PE applications. And our already well-established ATS-I is perfect for higher speed (up to 200 ips) requirements.

Space is at a premium in a minisystem, so we made the ATS-III and its formatter very compact. Both mount in a standard rack, and the formatter is little more than five inches high.

A μ-processor for reliability and maintainability

We know how important these are to the OEM market. So besides mechanical ease of maintenance, we incorporated a microprocessor in our design. It insures gentle tape handling and provides extensive microdiagnostics. That means trouble-free operation for you and your customers.

Put quality behind your nameplate. For more information on which is the better choice for you, call us at 612/853-5020. In Europe, contact one of our European representatives. Or return coupon to:

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Phone_____

CONTROL DATA CORPORATION

More than a computer company

CIRCLE 93 ON INQUIRY CARD

Dual Floppy Disc System For S-100 Bus Includes Controller and Software

Dual-Stor disc system with disc controller board, dual floppy disc drive, DOS, BASIC compiler, assembler, string oriented editor, and debug software has a storage capacity of 243k bytes/8″ (20-cm) diskette. Using programmed data transfer, it operates with static and dynamic memories at a rate of 250k bits/s.

The S-100 bus compatible system utilizes IBM compatible recording format. Vector Graphic Inc, 31364 Via Colinas, Westlake Village, CA 91361 has incorporated the reset-and-go function on power up. Packaged in a cabinet that matches the Vector 1 microcomputer, the system retails for $2300.

Circle 434 on Inquiry Card

Larger, Nonvolatile Memory Is Provided For 6800 Microprocessors

MM-6800/16 memory with internal power monitoring circuits to protect data from power failure or during turn on and off is a 16k x 8 core memory circuit for Motorola's EXORciser® and MEC 6800 evaluation module. No battery backup or special circuits are required for power supply sequencing.

Features include automatic power-on reset signal, a switch to write-protect 2k-increment portions of memory up to 16k max, and 4k-increment onboard module selection up to 64k words of memory. Micro Memory, Inc, 9438 Irondale Ave, Chatsworth, CA 91311 has combined two PC boards into a single plug-in package measuring 5.75 x 9.75 x 0.85″ (14.61 x 24.77 x 2.16 cm).

Circle 435 on Inquiry Card

Controller Connects Magnetic Tape Drives To LSI-11 Systems

DILOG 1 magnetic tape controller couples up to eight 7- or 9-track magnetic tape drives to LSI-11 based computer systems. The format is compatible with IBM and ANSI standards for NRZI recording on 0.5″ (1.3-cm) tape. Byte order is switch selectable for DEC or IBM compatibility. Selectable tape speeds are from 1.25 to 75 in (31.8 to 191 cm)/s. Software compatibility exists for DEC TM11 tape systems.

Manufactured by Distributed Logic Corp, 12800 "G" Garden Grove Blvd, Garden Grove, CA 92643, the single quad board which occupies two device locations in the LSI-11 backplane incorporates a microprocessor. This allows onboard automatic self-test diagnostics to permit malfunctions to be visually isolated to the computer, controller, or tape drives.

Circle 436 on Inquiry Card

Microcomputer With Operating System Has SS50 Compatibility

The JF68 6800 based microcomputer has 16 slots on the motherboard, which mounts in a walnut cabinet. The system's power supply has sufficient current handling to permit additional RAM or P/ROM configurations. JFBUG, a 2k operating system is resident in ROM. Commands in the monitor contain all necessary software to read and record programs on low cost cassette recorders.

Existing software for any MIKBUG-type system can be executed without modification of the computer from JF Products, 1441-5 Pomona Rd, Corona, CA 91720. Interfaces are provided for RS-232 or current loop, or for audio cassettes using the Kansas City Standard recording technique.

Circle 437 on Inquiry Card

Range of Computer Systems Provide Up to 780k Bytes of Storage

The PCS-4X integrated system based on an 8085 microprocessor features 32k/64k RAM, dual 5.25″ (13.34-cm) floppy discs, and serial and parallel I/O in a desktop cabinet. IMSAI Manufacturing Corp, 14860 Wicks Blvd, San Leandro, CA 94577 has designed three versions—PCS-40, -42, and -44—with disc storage capacities of 180k, 400k, and 780k bytes, respectively.

All that is needed to complete the system is a terminal, or keyboard, video interface board, and video monitor. Interface boards, RAM, and disc drives may be added for expansion. IMDOS, the company's multidisc operating system is supplied with the system; utilities include an 8085 assembler, video/context editor, dynamic software debugging program, and floppy disc system diagnostic program.

Circle 438 on Inquiry Card

Data Concentrator Multiplexes Synchronous/ Asynchronous Channels

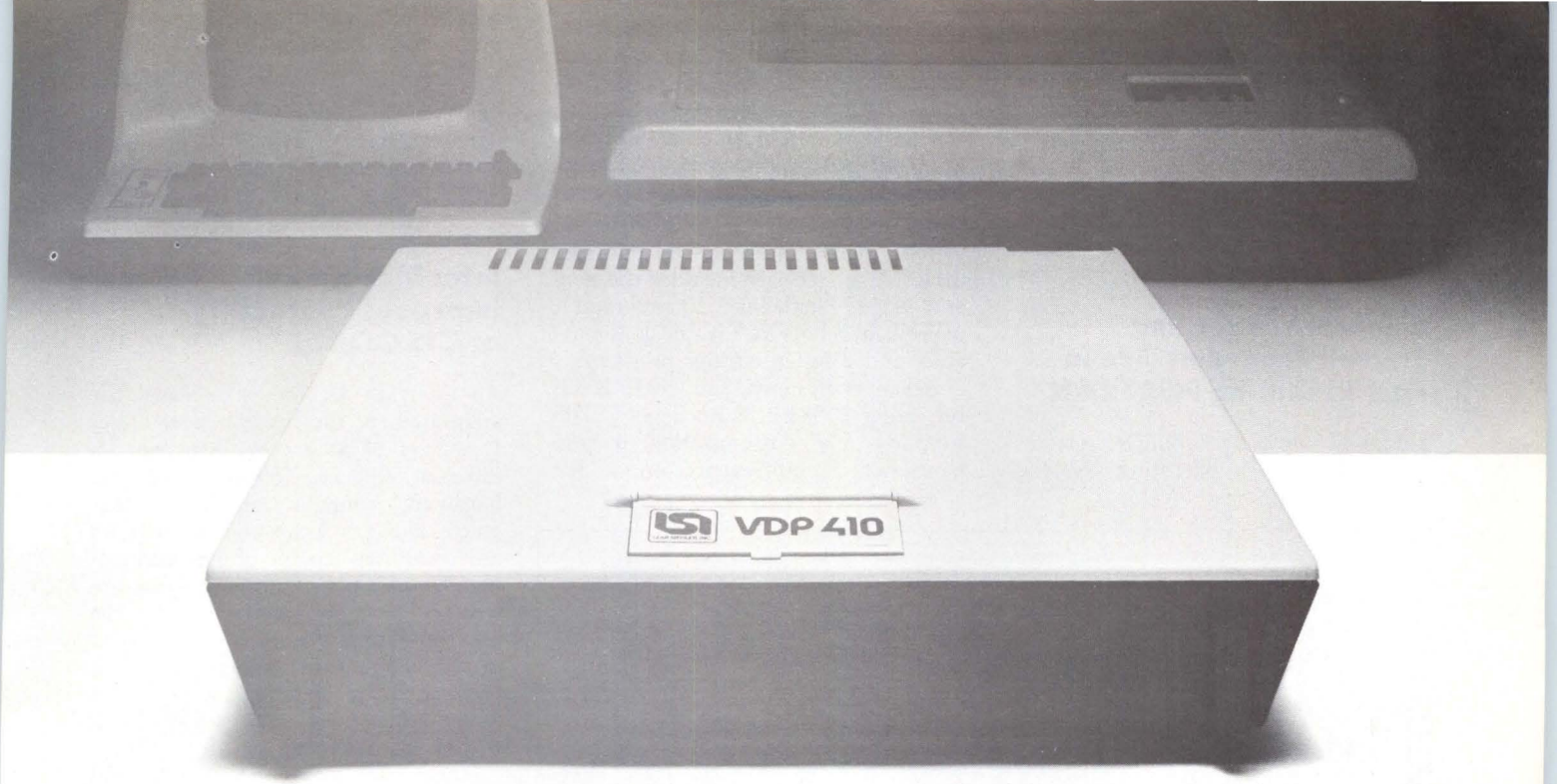
For applications requiring one or two synchronous channels to be multiplexed along with the asynchronous channels concentrated by the Micro-800, the synchronous channel option splits the high speed line data rate into subchannels operating at ¼, ½, or ¾ the composite data rate. One of these subchannels is used for concentrated asynchronous data. The single option 800/S from Micom Systems, Inc, 9551 Irondale Ave, Chatsworth, CA 91311 allows multiplexing of one synchronous channel with the concentrated asynchronous data; dual option 800/S2 allows multiplexing of two synchronous channels. High speed line data rates to 19.2k bits/s are supported.

Circle 439 on Inquiry Card

General Purpose 8085 Microcomputer Card Is Industrial Quality

Measuring 4.5 x 6″ (11.4 x 15.2 cm), the SSM-85/1 card for industrial use features 4-level programmable interrupt, 1280 bytes of RAM, 1k bytes of EPROM (expandable to 4k bytes), 22 parallel I/O lines, a serial I/O port, and programmable 14-bit binary counter/timer controlled by the 3-MHz crystal. A micro-monitor resident on the EPROM communicates through the serial I/O port. Software compatible with the 8080A, the card has 1.33-μs CPU instruction cycle time. System Service, 12120 Rochester Ave, West Los Angeles, CA 90025 has designed the unit so that it may also be powered by a single 5-V supply by using 2k EPROMS.

Circle 440 on Inquiry Card



This plain brown box keeps things under control.

It may not look like much, but our new VDP-410, a general purpose minicomputer, is one intelligent building block for system development.

It gives OEMs the flexibility to configure a wide variety of systems.

A CORNERSTONE THAT FITS IN A LOT OF PLACES.

The VDP-410 is a low-cost, 16-bit CPU with enough speed and ports to support a variety of peripherals. From communications controllers without external storage capabilities, to sophisticated time-sharing systems with a string of terminals, printers and disks—the VDP-410 feels right at home in any and all of them.

The 410's DMA channel provides easy expansion. You can get a cable and an expansion chassis with five slots for 15" cards and a hefty power supply.

HERE'S WHAT'S INSIDE THE BOX.

The basic system consists of a CPU with 600 nanosecond cycle time, and 16-bit, 32K word memory, and I/O capabilities for communication with three external devices. The CPU also includes an expansion port with serial/parallel I/O capabilities.

The VDP-410's instruction set, memory organization, and I/O architecture are compatible with hardware made by Data General and other manufacturers. Operating systems, file management systems, and programming utilities are available from leading software houses as standard packages, so it doesn't take any custom configuring to please the VDP-410.

THE VDP-410. SIMPLE, INTELLIGENT, AND POWERFUL.

The 410's instruction set is Nova* compatible, and provides memory access, arithmetic, logical, and I/O functions. And it's augmented with load/store-byte, inclusive/exclusive OR, exchange accumulators, multiply/divide, and block move. So OEMs get an incredibly powerful instruction set for tasking and data management.

If you're looking for a way to keep your system under control, call or write to us. We'll be happy to tell you all about our new VDP-410.

And how it can become as big a brainstorm for you as it was for us.

VDP 410
The intelligent building block.

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*Nova is a registered trademark of Data General Corporation.

CIRCLE 94 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS AND SYSTEMS

SOFTWARE

General Ledger and Payroll Programs Are in Fast Executing FORTRAN

Designed to run on 8080/Z80 systems with a CP/M™ operating system, software programs are coded in FORTRAN and use an indexed sequential access method that allows it to run fast, without being hampered by the overhead of an interpreter. Minimum configuration is 32k bytes of memory, a CRT, printer, and two disc drives. The software includes the general ledger (with over 20 programs), payroll, accounts receivable and payable, and a letter writing program.

Arkansas Systems, Inc, 8901 Kanis Rd, Suite 206, Little Rock, AR 72205 supports any customization or enhancement requirements on a fee basis. Fixes to legitimate software bugs will be supplied and a software update service is available.
Circle 446 on Inquiry Card

Interface Kit Improves Portability of CIS COBOL

An interface kit for OEMs eases the adaptation of the CIS COBOL compiler (a subset of ANSI COBOL) to run on different 8080 and Z80 microcomputer hardware configurations. The language runs as a resident system on any computer capable of byte addressing. Two simple program modules are written: one to interface with the user operating system and the other to drive the CRT. Actual linking is performed by patching a series of jump instructions in a vector block within the language.

The kit comprises the compiler and runtime system in object code form. MicroFocus Ltd, 18 Vernon Yard, Portobello Rd, London W11 2DX, England also supplies documentation consisting of a manual and system test library of 25 programs. Actual interfacing entails linking the runtime system with the user's operating system and CRT drive module. When interfaced, the compiler becomes resident on the system.
Circle 447 on Inquiry Card

Disc Operating System Supports 64k-Byte RAM And Online Disc Drives

SDOS disc operating system for 6800 systems with 24k of RAM and floppy (or other) disc drives suits applications software or development tasks. Up to 64k bytes of RAM and any number of compatible online disc drives are supported, as are files (random and sequential) on any storage device capable of up to 2.15G bytes. Features include device independent I/O, customizable command interpreter, and addition of device drives operating with or without interrupts.

Disc files are created automatically as needed. Electronic Product Associates, Inc, 1157 Vega St, San Diego, CA 92110 has devised the system so that all space management is done on a dynamic basis allowing files to grow or shrink. Assembly language interface to the system is the same as the Software Dynamic I/O package interface; available SD software can be run under the operating system.
Circle 448 on Inquiry Card

NOVA & ROLM users
...here's plug compatible cartridge storage

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LSI-11
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TAPE STORAGE SYSTEMS
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YOU SHOULDN'T HAVE TO SEE SIX DIFFERENT SUPPLIERS TO MAKE A NETWORK WORK.

Until now, putting together a distributed network for process control, experiment monitoring or test and inspection meant dealing with a lot of different companies. And you could still end up with a mish-mash of misfits.

Now, finally, there's an intelligent way to distribute intelligence. Because all the hardware and software you need is now available from a single company that specializes in systems for industrial and scientific applications: MODCOMP.

Classic 7810 — A new cost/performance leader for minis.

Designed specifically for use as a satellite in a distributed network, our new Classic 7810 minicomputer gives you MODCOMP's sophisticated hardware and software capabilities at microprocessor prices.

It has the largest directly-addressable memory of any 16-bit CPU — 128 K-bytes of solid state memory. This allows you to run larger memory-resident programs so you can do more work at the satellite level and free up the host for more complex tasks. As a result, the network will operate at maximum efficiency.

The 7810 is supported by a complete set of field-proven software including MAXNET III, our network operating system. And our MAX III Real-Time Operating System which enables the 7810 to be used as a stand-alone computer.

It's available as a computer-on-a-board for OEM's. As a fully packaged system. Or as an integral part of our new process I/O system, MODACS III.

MODACS III — Our new modular data acquisition and control subsystem.

MODACS III is designed to give you maximum flexibility in process control interface applications. Either as a local subsystem. Or, with the addition of the 7810, as a complete remote system in a network.

When used as a remote satellite, with our new HDLC/ADCCP/SDLC multi-drop communications link, MODACS III can be located right at the process you want to control.

This reduces your in-plant wiring requirements. The load on your host computer. And your risks as well. Because if the host goes down, the process that MODACS III is controlling doesn't have to.

For either the local or remote application it can contain up to 64 process I/O interface modules so you can hook up as many as 2,048 digital inputs or outputs; up to 1,024 wide range analog inputs; up to 256 analog outputs; a whole host of special functions; or any combination.

What does all this mean? It means that you can use MODACS III to control and monitor thermocouples, pressure transducers, strain gauges, meters, analyzers, amplifiers, potentiometers and hundreds of other analog or digital devices. In the harshest environmental conditions.

A complete family of real-time systems for the real world.

If you need more performance than the 7810 and MODACS III, we've got that, too.

The MODCOMP Classic 7860 and 7870 superminis have outperformed DEC's 11/70 and VAX. Interdata's 8/32. Prime's 400. And SEL's 32/75.

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CIRCLE 96 ON INQUIRY CARD

Disc Software for 8080 Microcomputers Operates Under CP/M System

Three advanced software packages, operating under the CP/M disc operating system have been introduced by Technical Systems Consultants, Inc, PO Box 2574, West LaFayette, IN 47906. These 8080 assembly language programs include a fully commented printed source listing.

The text editing system includes a line and content oriented editor. Commands may be used in a string, line, relative, local, or global sense. Features include block move and copy, tabs, overlays, append, and restrictive column searches. Any size file that fits a disc may be edited regardless of available RAM space.

The text processing system is an extensive output formatter that processes any number of named edit files. Over 50 commands allow such functions as pagination, multiple spacing, line centering, and justification. Macros may be defined along with conditional command execution, number registers, terminal prompts, and a loop command. A separate data file may be read for information such as names and addresses that are required by the text file.

Supporting standard pseudo-ops plus paging, titling, hex or octal listing, auto field formatting, sorting symbol table, and others, the mnemonic assembler is Intel compatible except for macros, conditional assembly, and logical expression operators. Hexadecimal or binary object codes, or print listing files may be produced directly on disc, with the listing routed to a line printer.

Circle 449 on Inquiry Card

Z80 Operating System Responds Quickly to Realtime Events

VIRTUAL MICRO II™ includes a multiuser/multitasking operating system supporting up to four users as well as concurrent tasks defined by the user's programs. Also featured are line printer spooling for efficient system utilization and performance, floppy disc file management support for both shared and user private files, and program development support of Z80 macro assembler and Business Disc BASIC languages.

Hardware requirements include bank switchable RAM, dual IBM compatible floppy disc drives, and a realtime clock. Presently, Systems & Software, Inc, 2801 Finley Rd, Downers Grove, IL 60515 has been using the system with the Cromemco System Three (CS-3); other versions can be made available for comparable Z80 based microcomputer systems.

Circle 450 on Inquiry Card

Signed Licenses Increase Supply of Software Programs

Two licensing agreements for its G/2 microcomputer software programs have been announced by the Consumer Computer Group of GRT Corp, 1286 Lawrence Station Rd, Sunnyvale, CA 94086. With the first agreement, Microsoft of Albuquerque, New Mexico will supply BASIC interpreter programs for SWTPC 6800 and Processor Technology SOL microcomputers. Prices are $34.95 and $49.95, respectively.

A second licensing agreement has been signed with Softape of Burbank, Calif for development of several programming applications, with graphic capabilities that will initially emphasize home entertainment packages. These packages will retail for $14.95.

Circle 451 on Inquiry Card

Alternate Configuration Prompts Release of CP/M Operating System

Release 1.4 of the Digital Research CP/M™ floppy disc operating system has been implemented by General Technics Inc, 1515 W Main St, Peoria, IL 61606 for Digital Group 8080 or Z80 microcomputers with a minimum of 18k of contiguous memory and a full size floppy disc drive. Because of the compatibility with other CP/M systems, owners of these microcomputers can exchange programs with those of other systems, and can utilize the software that runs under CP/M, including several BASICS, FORTRAN IV, COBOL, and business packages.

Up to four disc drives can be accommodated; the system can be easily relocated for larger memory size. Audio cassette storage is supported; Phi-deck support is planned.

The $100 package has the diskette, bootstrap ROM, manuals, and documentation. It includes the text editor, 8080 assembler, debugging tool, peripheral interchange program, relocator, and utilities. Among the special programs are a disc formatter and audio cassette read and write utilities. A variety of public-domain software from the CP/M User's Group, including a Z80 assembler and BASIC-E compiler/interpreter, is being distributed free of charge.

Circle 452 on Inquiry Card

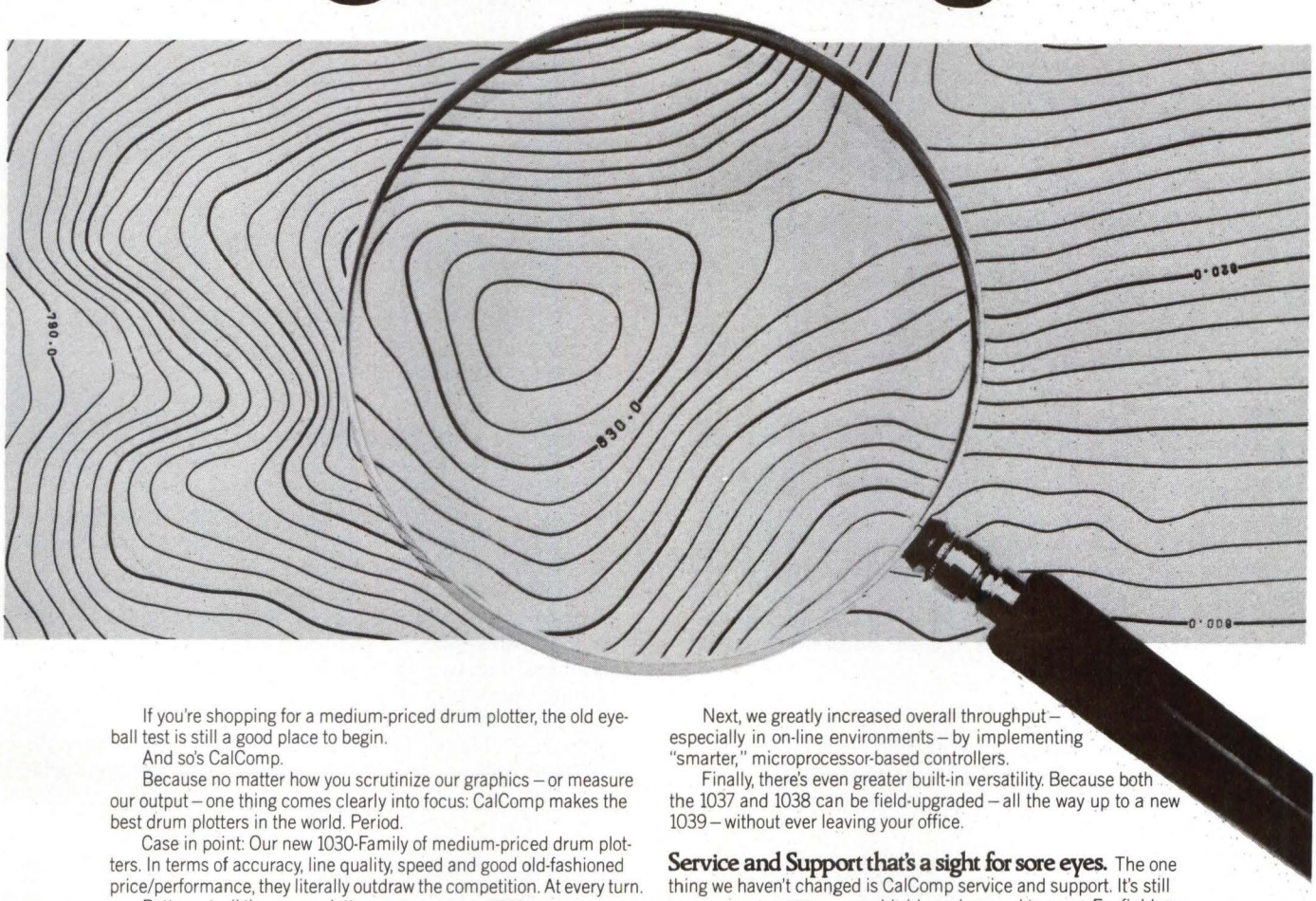
Task Based Processing Simplifies Programming of Realtime Systems

Enabling users of 8080 or Z80 based microcomputer systems to immediately begin to write multiprocessing programs, the Realtime Monitor (RTM) program in effect divides up the time and resources of a microcomputer and distributes it among separate and independent modules (tasks) so that each appears to operate by itself. Features include the ability for tasks to communicate via messages, synchronize each other with P and V operations, and schedule time dependent processes. It functions with or without a realtime clock.

The self-relocating program, announced by Oasis Systems, 2765 Reynard Way, San Diego, CA 92103, generates a kernal system that is less than 1300 bytes in size. It is ROM compatible for OEM applications. Operations are invoked with calls, which are, in addition, compatible with Microsoft™ FORTRAN IV. □

Circle 453 on Inquiry Card

No one else looks this good under glass.



If you're shopping for a medium-priced drum plotter, the old eyeball test is still a good place to begin.

And so's CalComp.

Because no matter how you scrutinize our graphics – or measure our output – one thing comes clearly into focus: CalComp makes the best drum plotters in the world. Period.

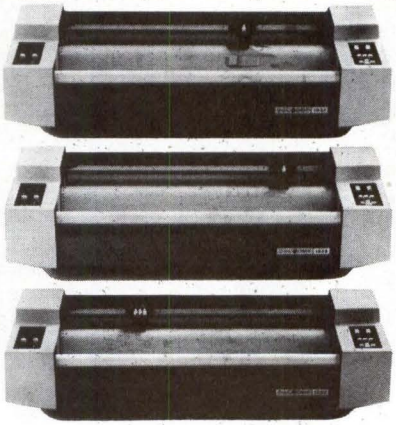
Case in point: Our new 1030-Family of medium-priced drum plotters. In terms of accuracy, line quality, speed and good old-fashioned price/performance, they literally outdraw the competition. At every turn.

Better yet, all three new plotters are perfectly suited to a wide range of graphics applications. And that means, with the help of a new 1037, 1038 or 1039 plotter, any data now in your computer can work even harder for you outputted in an easier-to-understand graphic form.

A clear case of superior engineering.

For starters, we made all three new models completely d.c. servo-motor driven. For increased accuracy in every mode. On-line. Remote/time-sharing. And off-line.

Then, we gave them all a newly-designed linear drive pen mechanism. For the kind of pen force control that produces consistently superior line quality. In every application.



Next, we greatly increased overall throughput – especially in on-line environments – by implementing "smarter," microprocessor-based controllers.

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1038	112.5 (≈4.5 in.)	1	.05 (≈.002 in.)
1039	112.5 (≈4.5 in.)	3	.05 (≈.002 in.)

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SINGLE-CHIP SPEECH SYNTHESIZERS

Scott Smith
Integrated Computer Systems, Inc
Santa Monica, California

Speech synthesis is a prime target for very-large-scale integration (VLSI) implementation in that the quantity of information manipulated in the synthesis matches the processing capabilities of the semiconductor technology. Consequently, several manufacturers are presently developing speech synthesizers utilizing VLSI, and two of them, Texas Instruments Inc, Dallas, Texas and Telesensory Systems Inc, Palo Alto, California, are manufacturing products incorporating speech synthesis logic on a single VLSI chip.

The TI System

Texas Instruments (TI) has introduced a speech synthesis system employing a monolithic integrated circuit designated as the TMS0280. This chip can be used in configurations utilizing as few as 1 or as many as 16 separate 128k-byte read-only memories (ROMs) to provide from 100 s up to almost 27 min of recorded speech. Intelligence is provided through incorporation of a microcomputer such as the TMS1000. A block diagram for a general speech synthesis system of this type is shown in Fig 1.

Presently, TI is producing a learning aid, Speak and Spell™, using one speech synthesizer chip, one microcomputer, and two 128k-byte ROMs, but has no plans for separate marketing of the synthesizer chip at this time (see *Computer Design*, Sept 1978, pp 200-202). The synthesizer chip is an interesting example of a VLSI design that utilizes the most inexpensive of semiconductor

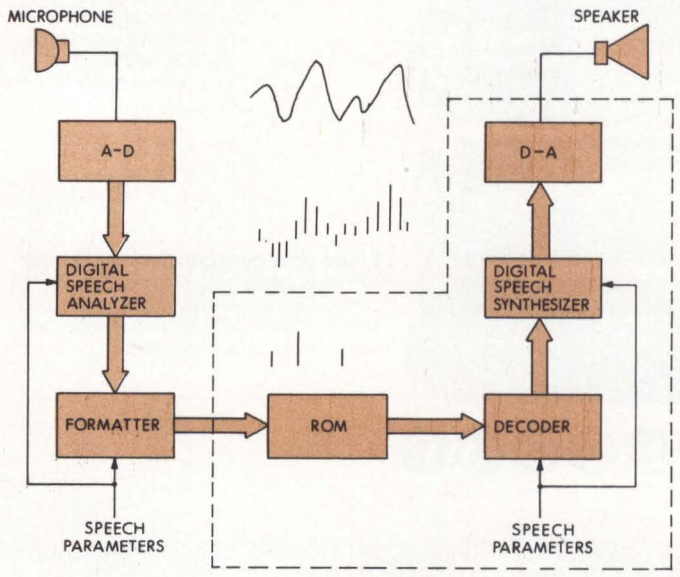
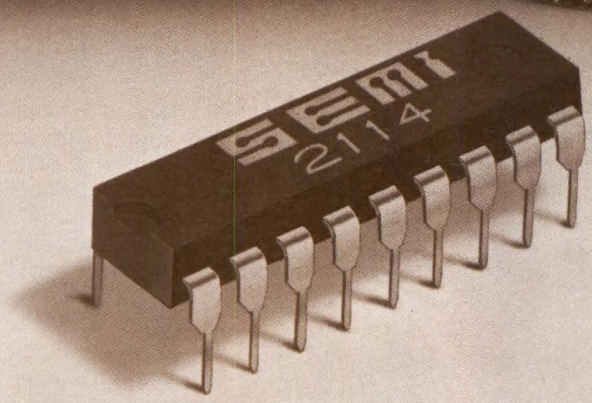


Fig 1 Block diagram of general speech simulator. Equivalent of Texas Instruments speech synthesis system in Speak and Spell™ is outlined by dotted line. Note that simple speech production system would involve connecting output of A-D to input of D-A. Objective in speech simulation is to extract characteristics of speech sample so as to minimize amount of storage required to describe sample, hence addition of analyzer and formatter before storing information on ROM, and decoder and synthesizer after ROM to regenerate information

The 2114 from the Royal Family...

it saves power, naturally



Most members of the Royal Family of Static RAMs know all about power and how to save it. That's an inherited trait, and the L2114 is no exception. It draws only 240 mw which is about what you have come to expect from the leading supplier of static RAMs. But, that's not all. We also have a "Power Down Part" that operates on 2.5 volts and draws less than 100 mw. That's real power saving from the company that has been delivering 18-pin 1K x 4 static RAMs for at least a year longer than anyone else. And not only that, but we have a new MIL version on the way.

In addition to low power, the SEMI 2114 features a common I/O structure with TTL compatible three-state outputs, and more than adequate speed for second generation microprocessor applications.

You can learn more about the SEMI L2114 — or any other members of the Royal Family of Static RAMs — by simply calling your local EMM SEMI rep or distributor, or contacting us directly at the address below.

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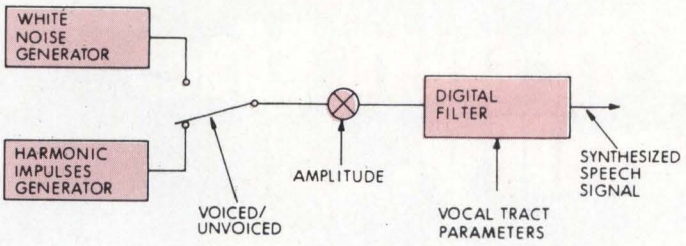


Fig 2 Digital speech generation. White noise is generated as random pulses while vowel sounds are implemented using periodic pulses. Pulses are selected and routed through digital filter, simulating human modulation. Output is digitized audio speech signal that can be D-A converted, amplified, and transmitted to speaker

Desired Parameter Resolution

Parameter	Number of Levels	Number of Bits
Amplitude	15	4
Pitch	32	5
K1	32	5
K2	32	5
K3	16	4
K4	16	4
K5	16	4
K6	16	4
K7	16	4
K8	8	3
K9	8	3
K10	8	3
	Total	40

fabrication techniques, p-channel metal oxide semiconductor (PMOS), to achieve a cost-effective consumer product.

Human speech is modeled electronically by the synthesizer as shown in Fig 2. Speech is a modulated audio wave, and the components of that modulation are extracted and stored on the ROM. Pitch, voiced/unvoiced source selections, amplitude, and digital filter coefficients are specified. If the pitch input is 0, the white noise generator is selected; otherwise the harmonic impulse generator is selected, with the pitch parameter determining frequency. The digital result is amplified by a simple multiplier whose gain is determined by an amplitude parameter.

Characteristics of the digital filter are determined by 10 coefficient words. The resolution of these words plus the pitch and amplitude is shown in the table. Note that a total of 48 bits is required for each speech "frame." Since each frame is defined to be 20 ms, a total of 2400 bits is needed from the ROM for each second of generated speech.

However, ROM economies are accomplished through taking advantage of certain speech properties. For example, since the vowel sounds change relatively slowly, it is often possible to repeat the coefficient words verbatim. Also, unvoiced sounds require fewer coefficient words. Finally, when the amplitude is 0, no other data are needed; this might occur during intersyllable pauses. Special codes are defined to cover all three of these cases, with the result that the average rate is decreased to 1500 bits/s. A last improvement is that an interpolation facility is available to update the coefficients between frames to achieve better fidelity.

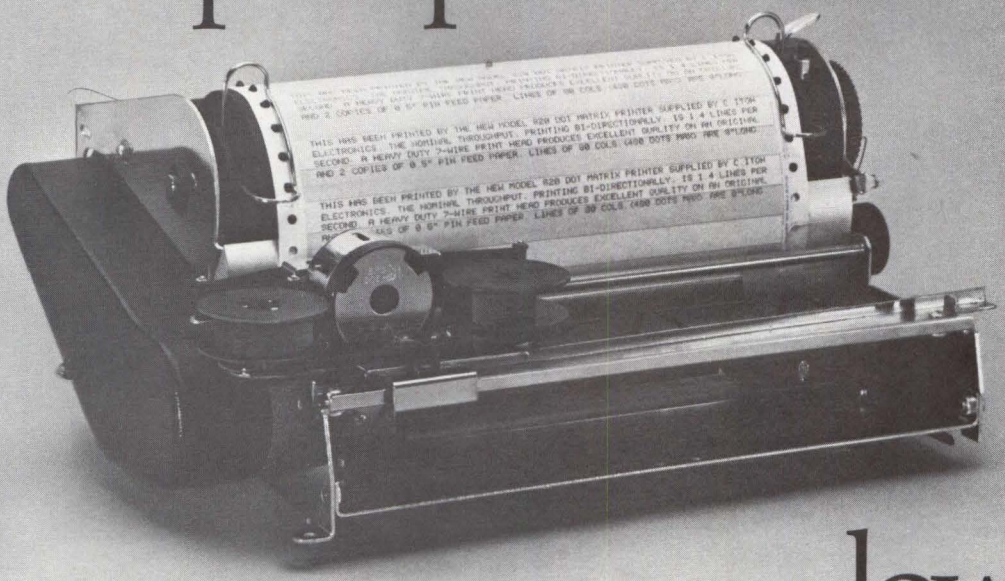
In order to minimize the number of interconnections, the interface to the ROMs was designed as a serial path. This means that although the 128k ROMs are internally organized as 16k bytes x 8, addresses and data must be shifted in and out serially on a 1-bit data "bus." The serial data handling structure is provided to minimize ROM storage and ease interfacing to the ROM chips. This is somewhat unusual, contrasting with the more common parallel data structures. However, it is of interest because the philosophy of maximizing component efficiency, through serializing as much of the digital logic as possible, results in a compact chip design. Furthermore, because the serial facility requires less than a 2400-baud rate of message input, no special high speed hardware is required.

Programming the TI Synthesizer

Programming the synthesizer chip is intimately tied to the interface with the 128k ROMs. These ROMs have 18 bits of addressing: 14 bits to select 1 of the 16,384 locations, and 4 as a 1-of-16 chip select. The data bus is only one bit wide; therefore, data words must be shifted in and out serially. Finally, there are two control lines. The first is a load/read line that, when 1, causes one bit to be serially shifted into the address register from the data bus; when 0, one bit of data is shifted out onto the data bus. The second is a positive 5-μs strobe pulse that clocks data on the data bus. It has a maximum frequency of 100 kHz.

The synthesizer chip is designed to interface to the serial ROM chips by taking advantage of special software features and must be programmed accordingly. It is designed to load the parameters automatically in the order listed in the table. The engineer can achieve further efficiencies by taking advantage of the following software features:

Model 820, 150 cps, 80-column, dot matrix impact print mechanism...



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CIRCLE 99 ON INQUIRY CARD

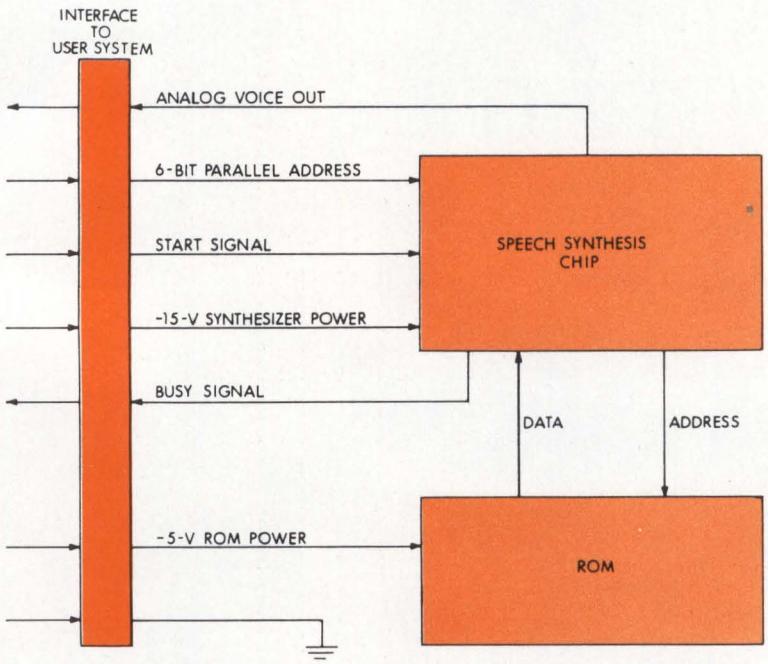

Fig 3 Simplified block diagram of Telesensory Systems synthesizer chip. Synthesizer is initiated by strobing 6-bit address of desired word with start signal. Device will indicate busy until it has completed speaking of word, at which time another one of 64 words can be selected

(1) To repeat the coefficients, set the most significant bit of the K1 parameter to 1. The synthesizer will not request any further data for that frame.

(2) When pitch = 0, unvoiced speech is being selected so that only K1 through K4 will be used by the synthesizer.

(3) When amplitude = 0, a pause is indicated and the synthesizer will not request any more data for that frame.

A user who is not employing TI ROM chips can start the system by simply issuing a "speak" (binary 101X on CTL8, CTL4, CTL2, and CTL1 lines) or "speak slowly" (011X) command. The synthesizer will then fetch speech data automatically until it receives an "F" code for amplitude, at which time it concludes that the speech transmission is complete. It will then wait for another "speak" or "speak slowly" command.

The TSI System

Originally intended for use in the Speech Plus® talking calculator for the blind, the Telesensory Systems (TSI) S14001A synthesizer chip is now available to original equipment manufacturers (OEMS) on a 3 x 3" (7.6 x 7.6 cm) printed circuit board. This board also contains one or two Intel 8316 16k-byte ROMS, which contain the vocabulary of the synthesizer. Each of the ROMS, organized as 2k x 8, can contain up to 64 spoken words. Presently, a standard 24-word calculator vocabulary is offered in English, German, Arabic, or French, as well as more extensive options in a 64-word English calculator vocabulary or a 64-word ASCII vocabulary.

Speech is stored on the ROM in a specially encoded compressed digitized form. Each word requires up to 800 bits, of which approximately 600 bits represent encoded waveform information, while the remaining 200 are control commands.

The synthesizer is directed to generate one of 64 words from a 6-bit command bus. It automatically extracts compressed speech information from the ROM, generates the expanded digitized speech, and converts it to an analog waveform. This waveform must be filtered externally before it is transmitted to a speaker (Fig 3). Featuring an extremely simple and straightforward interface requirement, this synthesizer would have application when an inexpensive portable speech source is required.

Summary

The VLSI approach should greatly enhance the growing speech synthesis technology. Single-chip speech synthesis systems from two manufacturers (one of these also providing synthesizer chips to OEMS) have been examined here. As increasing numbers of companies become involved in this technology, small, portable, inexpensive talking machines may ultimately become as ubiquitous as the calculator or transistor radio.

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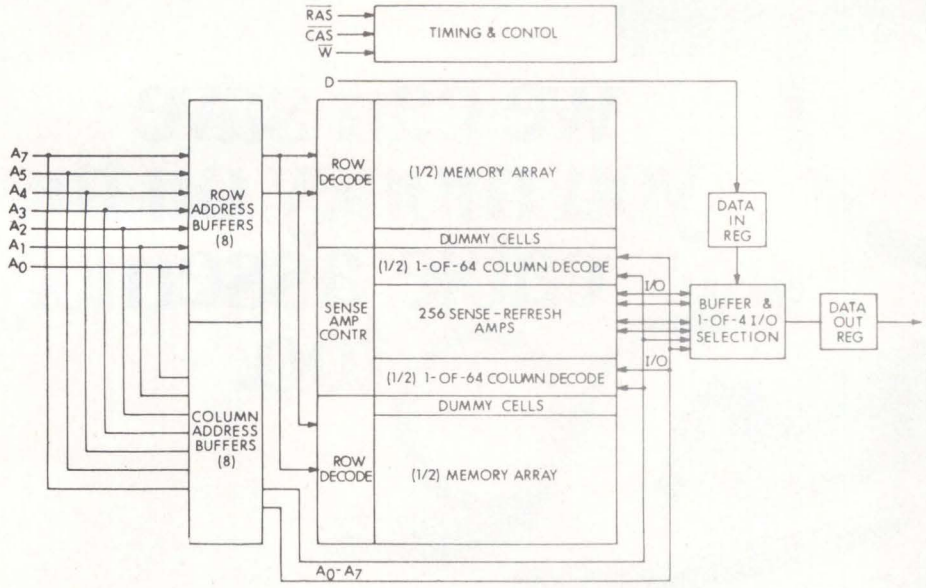
CIRCLE 100 ON INQUIRY CARD

5-V 64k Dynamic RAM Achieves High Performance from SMOS Technology



Functional block diagram of Texas Instruments TMS 4164 JL 64k dynamic RAM. During refresh period of 4 ms (twice that of 16k RAM) each of 256 rows must be strobed with RAS (row address strobe) to retain data. CAS (column address strobe) remains high during refresh sequence to conserve power. Operating power dissipation is only 125 mW (typ). Max access time from RAS is <150 ns; min cycle time (read or write) is <250 ns

Scaled MOS technology and use of electron-beam equipment in mask fabrication are said to be keys behind development of what is expected to be the first available single 5-V 64k dynamic random-access memory on the market. SMOS n-channel double level polysilicon gate technology results in very high performance, low cost, and improved reliability. Electron-beam equipment controls mask geometries to better than 0.25 μm.

The TMS 4164 JL, announced by Texas Instruments Inc, PO Box 5012, Dallas, TX, 75222, is organized as 65,536 x 1. Its single 5-V power supply, another feature resulting from SMOS technology, is TTL compatible and offers low power dissipation—typically 125 mW operating, 20 mW standby—and good immunity to system noise (supply current peaks have been reduced to 60 mA maximum, and a −1-V input voltage undershoot can be tolerated). In addition, the reduction in effective electric field across gate oxide offers higher system reliability, and the compact layout for 5-V operation results in performance improvements.

This device is upward pin compatible with the 16k TMS 4117 dynamic RAM. However, access times for the 64k RAM range from 100 to 150 ns maximum with minimum cycle times of 200 to 250 ns, opposed to 375 ns for the 16k RAM. Maximum power dissipation is 200 mW (or 3 μW/bit), a 60% reduction compared to the 462-mW power dissipation of the 16k device. Refresh period is extended to 4 ms maximum, a 100% improvement over the 2-ms period for 4k and 16k RAMs. Refresh overhead time is as low as 1.3% of the total refresh period. Because of refresh compatibility between the 64k and 16k devices, the only provision required when upgrading from a 16k to a 64k system is an 8-bit refresh counter/multiplexer.

Two clocks, RAS (row address select) and CAS (column address select), control the gating of the 8-bit addresses so that timing characteristics are essentially identical to the 16k RAM. Row address setup time is 0 ns; hold time is 15 ns. The system designer has a full 35-ns interval to change addresses and bring CAS low, without extending access time beyond 150 ns.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. Address lines and data in are latched onchip to simplify system design; data out is unlatched to allow greater system flexibility. Pin 1 is "no connect" to allow compatibility with other 64k RAMs using this pin for −5-V power supply.

The 64k device has a chip size of 33,000 sq mils and is offered in a 16-pin, 300-mil (0.762-cm) standard dual-inline package that complies with JEDEC standardized pin out requirements. It is guaranteed for operation from 0 to 70 °C. Sample quantities are available (at $125 each) and volume production is scheduled for the first quarter of 1979.

Circle 350 on Inquiry Card

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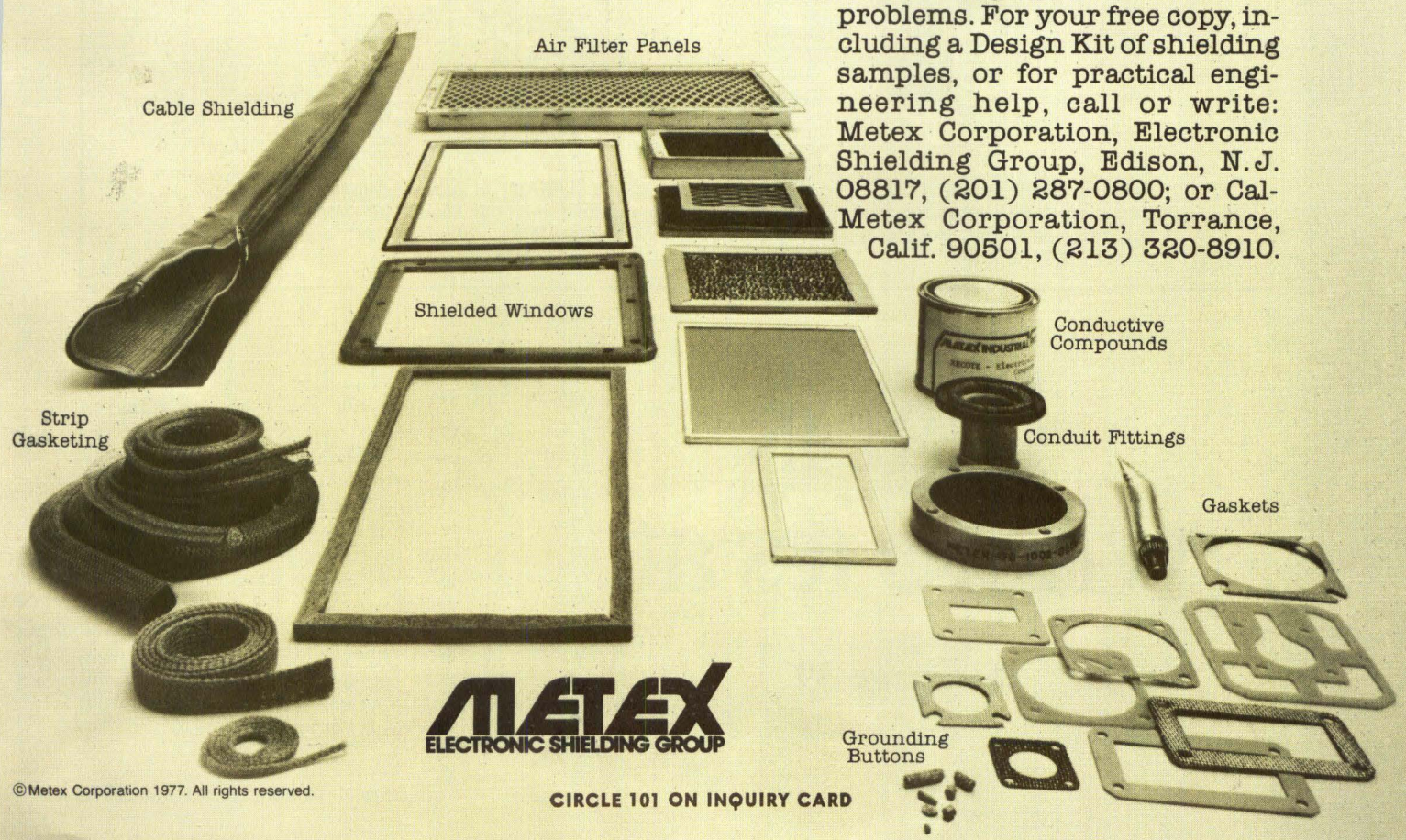

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CIRCLE 101 ON INQUIRY CARD

2-Chip Codec System Meets Both μ-Law and A-Law Requirements

A single-channel coder/decoder (codec) system, meeting both U.S. and CCITT specifications, and now in high volume production, is claimed by its manufacturer to be the first such system commercially available. The TP3000 is available from National Semiconductor Corp (2900 Semiconductor Dr, Santa Clara, CA 95051) as a 2-chip system consisting of separate digital and analog ICs.

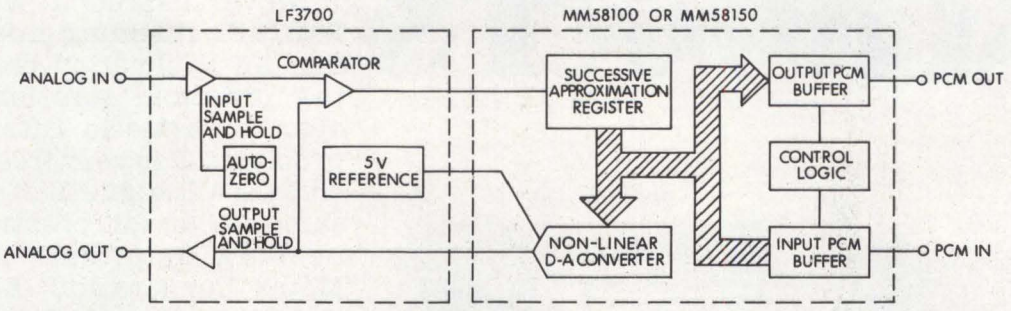
There are two versions of this pulse code modulation (PCM) system, both used for the digital coding and decoding of analog signals in the voice frequency band. The TP3001 uses the standard μ-255 code and the TP3002 uses the standard A-law code. These are variations of the same basic design, varying through slightly different CMOS components—MM58100 and MM58150, respectively.

The system samples a filtered (300 Hz $\leq$ F $\leq$ 3.4 kHz) analog signal at an 8-kHz rate, converts this sampled voltage to an 8-bit companded digital code (μ-law or A-law) and loads this code into a high speed serial output buffer. This output buffer will operate at any speed between 64k and 2100k baud and will automatically interrupt the encode cycle to decode the PCM word and update the codec output sample-and-hold. After decoding, the system will automatically return to the encoding cycle. This interrupt capability allows the asynchronous sending and receiving of PCM data. The system was specifically designed for low cost per line or per channel codec applications.

Digital parts of the device, including input and output PCM buffers, nonlinear DAC, control logic, and successive approximation register, utilize CMOS technology. For the analog parts the Bi-Fet™ ion implantation technique is used—specifically for sample-and-hold circuits, comparator, auto-zero circuitry, and 5-V reference. Life of the circuits is estimated to be on the order of 20 to 50 years.

The master clock for the system must be run at 128 kHz, dividing the 125-μs time-frame into 16 time slots. Rising edge of the output sync initiates the encoding cycle. Input sample-and-hold control goes high for 19 μs, causing the sample-and-hold to acquire a new input analog voltage, which is next presented to a unity gain buffer on the CMOS chip, and then forwarded to the positive comparator input on the linear chip. Successive approximation begins at this point, with the successive approximation register loading a zero code into the nonlinear DAC (diagram).

Output from the DAC goes to a second unity gain buffer and then to the negative input of the comparator on the linear chip. The comparator tests the sampled analog voltage, and if this is found to be positive, the control logic will pull the polarity control line high, which in turn will cause the voltage reference on the linear chip to deliver a positive reference voltage to the DAC. Conversely, if the analog input voltage is negative, a negative reference voltage will be applied to the DAC.



National Semiconductor 2-chip codec system. Analog IC (LF3700) includes comparator, auto-zero circuit, 5-V reference, and input/output sample-and-hold circuits. Digital IC (MM58100 or MM58150) includes successive approximation register, control logic, nonlinear DAC, and input/output PCM buffers

Flat is where it's at.

See page 39

Successive approximation turns on the second bit to the DAC and a decision is made to either leave that bit on or turn it off. The logic then operates in similar fashion on the third bit. In this way, analog input voltage can be converted in standard 8-bit μ-law or A-law code in eight clock cycles.

At the end of the encode cycle the 8-bit code is loaded into the output PCM buffer. The word is read out serially (MSB first) by the output clock and output sync.

THE EXPANDED CONVERSATIONAL MICRO BEE 1

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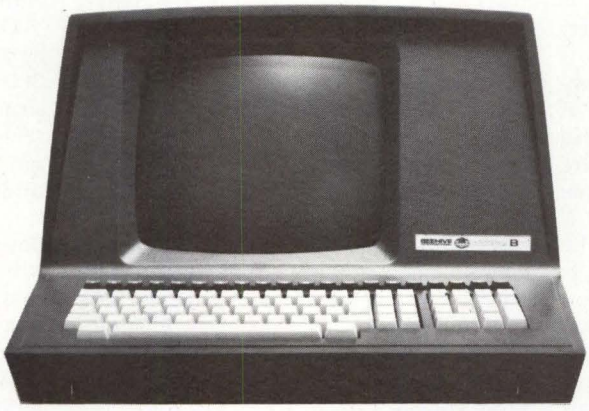

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features

Status Line
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Memory Lock
Read Status
Video Attributes
Line Drawing
128 ASCII Character Set
14 Key Numeric Pad
Time of Day Clock

Beehive International's Micro Bee 1 is an 8085A microprocessor controlled terminal offering numerous user oriented features, such as self-diagnostics, which ensures at a glance that the terminal is operating correctly. The status line is used extensively by the Micro Bee 1 system firmware to display modes of operation, error messages, communication protocol data as well as a status message showing optional switch configurations.

Among the Micro Bee 1 features is the ability to evoke the memory lock condition that allows the operator or host computer to lock a portion of the display memory while retaining the capability to enter or receive data in the unlocked portion of the display memory. Sixteen non-displayable character cells are available on each line for establishing character and field attributes. Other visual features include normal, reverse, blink, underline and half intensity video levels. The line drawing graphics capability allows for the creation of forms on the display using the vertical and horizontal line feature.

The expanded characteristics of the Micro Bee 1 include X-Y addressing, read cursor address, invisible memory address pointer, 128 ASCII characters set with descenders, 25 x 80 line format, and read terminal status.

OPTIONS

- *20 milliamp current loop*
- *Twelve function keys, cursor control keys, auxiliary on/off keys plus a serial buffered bidirectional peripheral interface*

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CIRCLE 102 ON INQUIRY CARD

CMOS Timer Offers Improved High Speed Operation

Pin-for-pin equivalent to the industry standard 555 RC timer, a high performance CMOS device features a typical power supply current rating of only 80 μA, less than 5% of that required by its bipolar counterpart. The ICM7555 general purpose timer is produced by Intersil Inc, 10710 N Tantau Ave, Cupertino, CA 95014. Expanded high speed operation to 500 kHz is guaranteed, for an approximate 5-fold performance improvement over the 555.

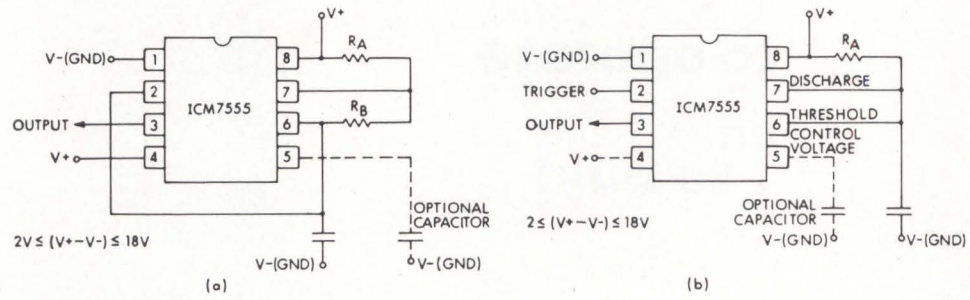
Other features include trigger, threshold, and reset currents that are typically 20 pA; a widened supply voltage range guaranteed from 2 to 18 V; and a typical temperature stability of 0.005%/°C at 25 °C. Timing range is from microseconds through hours, and the duty cycle is adjustable, with operation in both astable and monostable modes.

The ICM7556 is a dual ICM7555, with the two timers operating independently of one another, sharing only V+ (V_{CC}) and V− (gnd). In the time delay 1-shot mode of operation for each circuit, time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both controlled by two external resistors and one capacitor. In this mode (diagram), the external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle is precisely set by ratio of resistors. The capacitor charges and discharges between ⅓ and ⅔ (V+ − V−). Charge and discharge times, and therefore frequency, are independent of supply voltage.

In monostable operation, the external capacitor is held discharged by the transistor inside the timer. Upon application of a negative trigger pulse to pin 2, the flip-flop is set, releasing a short circuit across the external capacitor and driving the output high. Voltage across the capacitor then increases exponentially with time constant equal to R_AC. When voltage across capacitor equals ⅔ (V+ − V−), the comparator resets the flip-flip, which discharges the capacitor rapidly and drives the output to a low state.

Operating capability is up to 3750 h, with the timer driven by only two 300-mA-h NiCd batteries. CMOS construction eliminates the crowbar currents usually encountered in the output driver of bipolar devices, and traditional supply voltage and control voltage decoupling capacitors are not required to eliminate supply voltage transients. The high output source/sink driver can drive either TTL or CMOS gates.

Absolute maximum ratings include supply voltage (V+ − V−) of 18 V, input voltages between −0.3 and 0.3 V, and output current not to exceed 100 mA. Power dissipation is limited to 200 mW (300 mW for the dual device).



Astable (a) and monostable (b) operational modes for Intersil ICM-7555 timer. In astable mode, circuit can be connected to trigger itself and free run as multivibrator. In monostable mode, timer functions as one-shot

Circle 351 on Inquiry Card

Data Acquisition System Features Switchable Mode Selection

An integrated circuit data acquisition system provides the user with the option of connecting multiplexers to a differential amplifier in either 16 single-ended or 8 differential channels. The selection is performed by means of an internal analog switch governed by a digital input, a feature that gives the device the ability to perform in either mode without hardwired interconnections and permits a mixture of single-ended and differential sources to be interfaced to the system.

Produced by Analog Devices (Rte 1 Industrial Pk, PO Box 280, Norwood, MA 02062), the AD363 consists of two separate functional blocks, each hermetically sealed in an electrostatically shielded 32-pin metal dual-inline package. The analog input section contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold, a channel address register, and control logic. A complete 12-bit successive approximation ADC is contained in the analog-to-digital converter section. This converter includes an internal clock, precision 10-V reference, comparator, buffer amplifier, and a proprietary design 12-bit DAC. Active laser trimming of the reference and DAC results in maximum linearity errors of ±0.012% while performing a 12-bit conversion in 25 μs.

Analog input voltage ranges of ±2.5, ±5.0, ±10, 0 to 5, and 0 to 10 V are user selectable. Adding flexibility and value are the precision 10-V reference (active-trimmed to a tolerance of ±5 mV) and the internal buffer amplifier, both of which may be used for external applications. All digital signals are TTL/DTL compatible and output data are positive-true in parallel and serial form. Additional features include a 15-μs maximum acquisition time and a short cycle capability.

(Continued on p 200)

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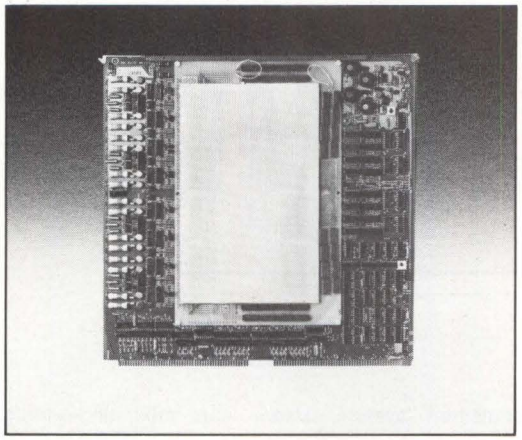

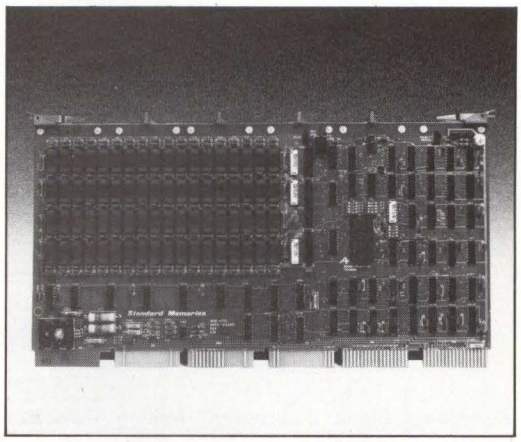

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It's the first...with more on the way! PINCOMM PS is a 64K pin-compatible add-in memory for DEC PDP-11 minicomputers. Using 16K MOS memory chips, PINCOMM PS is available in depopulated versions of 48K, 32K and 16K. Features include 100 nsec write access, 350 nsec read access and 450 nsec cycle time. Plus, a parity option that eliminates the need for the DEC parity card, increasing CPU space and memory throughput.

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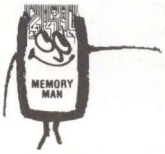

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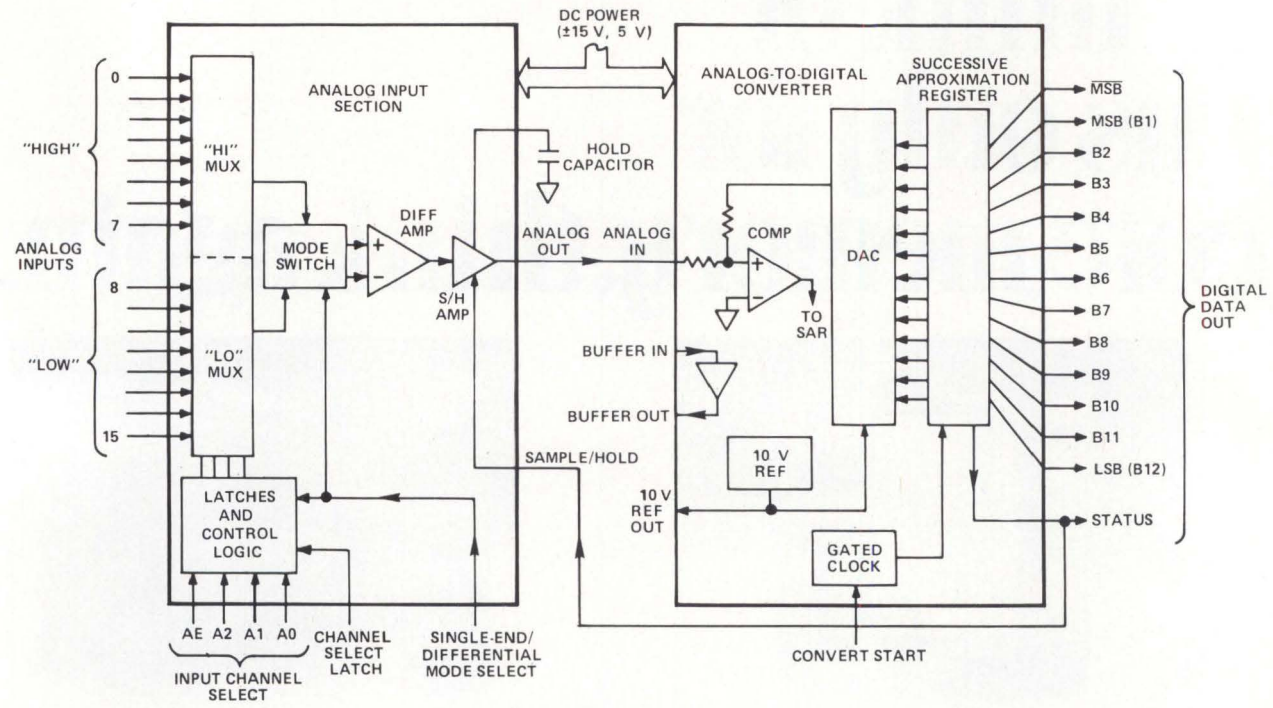


Functional block diagram of Analog Devices 12-bit data acquisition system. Users can mix single-ended and differential signals and select either without hardwiring

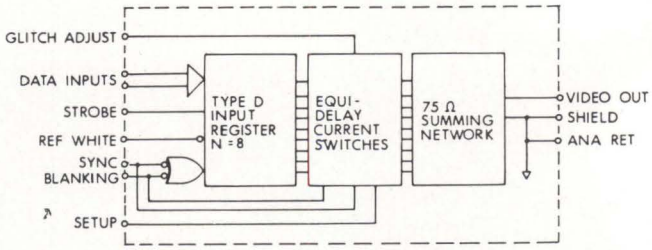
System throughput rate is as high as 30 kHz at full rated accuracy. The AD363K is specified for operation over a 0 to 70 °C temperature range, while the AD363S operates to specification from −55 to 125 °C. Processing to MIL-STD-883B is available for the S version. Both device grades are guaranteed to have no missing codes over their specified temperature ranges.

Circle 352 on Inquiry Card

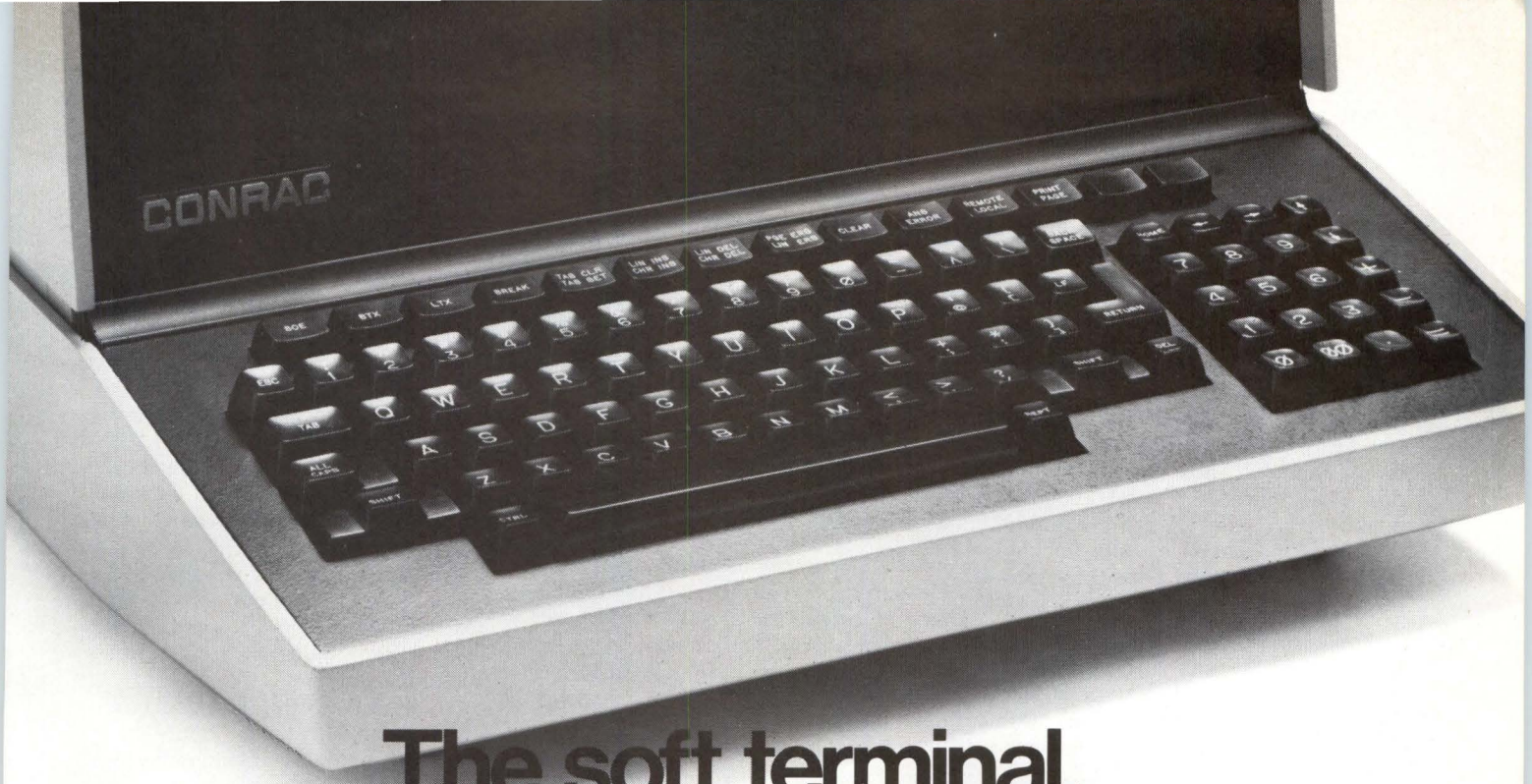
Video DACs Operate At High Speeds Without Support Circuitry

Designed specifically for video and graphic display applications, a family of 8-bit digital-to-analog converters provide 4-ns rise times, 100-MHz update rates, built-in data registers, and direct drive to 75-Ω loads. The MP8308 contains input data latches and generates a complete video signal with 256 gray levels, a blanking pedestal, and a synchronizing level. It produces output steps clean enough not to need deglitching. Because of the unusually small differential delay among the eight data channels, the glitches introduced by code switching are maintained at an extremely low level, virtually invisible on the best monitors.

The manufacturer, Analogic Corp, Audubon Rd, Wakefield, MA 10880, claims that the device is unique in combining all of the above features without the need for support circuitry. This is in contrast to older design video converters that provide only the basic 8-bit DAC to which users must add an input register, an output amplifier to drive 75-Ω loads, a deglitcher



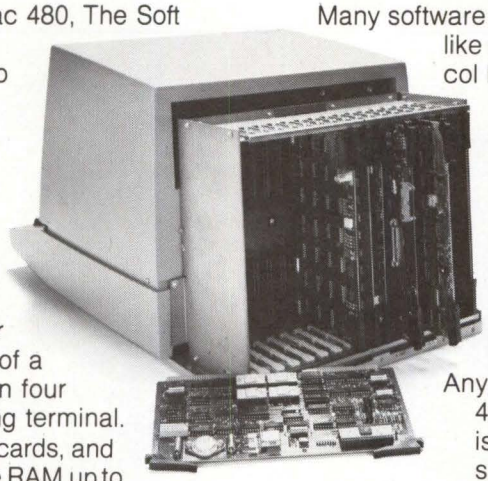
Functional block diagram shows three main parts of Analogic's high speed MP8308 video DAC: input register, equi-delay current switches, and summing network. Independent of extend support circuitry, device produces output that does not need deglitching



The soft terminal. Designed to be redesigned.

Chances are, the intelligent terminal you really need doesn't exist yet.

That's why we build the Conrac 480, The Soft Terminal. It's designed to be redesigned by your software to fit your system like a glove.



Flexible hardware to start you off.

Most CRT terminals are built around one large circuit board, which doesn't leave you much flexibility.

The Conrac 480, on the other hand, offers you the benefits of a *clean bus architecture.* Plug in four cards, and get a basic working terminal. Plug in up to twelve additional cards, and get some real power. Cards like RAM up to 48K bytes, PROM up to 16K bytes, and interfaces to floppy disk drives, printers and other peripherals.

Software to make it happen.

Do you need a special keyboard, character set, or set of terminal attributes? No problem. Just plug in a special PROM.

With the proper MPU software, the Conrac 480 can be configured as a polling terminal or as a powerful microcomputer. Or as anything in between. This software can reside in PROM, or can be downloaded into RAM from a host computer or from disk.

Many software modules are available off-the-shelf, like a basic editing package, and protocol handlers for IBM, Burroughs, and Univac. More are on the way. To make microprogramming easy, you can use the AMI 6800 Microcomputer Development Center software, which runs perfectly on our terminal. That's power!

Attractive outside as well as inside.

Any way you look at it, the Conrac 480 is attractive. The basic version is only 20" deep and fits where space is limited. Its understated modern styling blends into virtually any decor. And you can have your own color and texture.

Operators love the feel of our long-life capacitive keyboard with sculptured keys. And our sharp and stable CRT display. As a matter of fact, we're known worldwide as *the* manufacturer of professional video monitors.

Write to us or give us a call for more facts. We'll send you a comprehensive 12-page brochure on The Soft Terminal. And we promise not to use "hard sell."

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Conrac GmbH, Industriestrasse 18, D-6992 Weikersheim, W. Germany
Telephone (07934) 675, Telex 74250

CIRCLE 104 ON INQUIRY CARD

to get rid of output spikes to prevent unwanted black or white lines in the displayed picture, and, finally, a means for developing synchronization and blanking signals for driving the monitor.

The output signal, which is electrically compatible with EIA performance standards RS-170 and RS-343A, will drive monitors such as the Conrac QQA series directly. Operating from 5 and −5 V (or −5.2 V) supplies, the DAC is packaged in fully-shielded 50 x 75 x 9-mm metal cases, permitting 0.5″ (1.27-cm) board spacing.

These converters were engineered to interface directly between a TV timing ROM such as the MM5320 and high resolution monitors. The result is a circuit consisting of three major parts: an input data register, eight equal-delay switches, and a high speed summation network. Register flip-flops drive high speed switches that are capacitively trimmed for equal delay; the switches, in turn, steer current into a switching network whose intrinsic bandwidth exceeds 200 MHz. This network has a Thevenin impedance of 75 Ω; the current steered into it is sufficient to develop a 1-V pk-pk signal directly into a 75-Ω load. Because the network itself directly generates the required output voltage, no amplifier or buffer is needed. This results in an unusually clean transition at the output, totally free of ringing or overshoot, with an extremely short rise time.

The device is designed to drive high resolution, raster scan TV monitors in monochrome or color from digital input data. Pricing in OEM quantities is under $70 per unit.

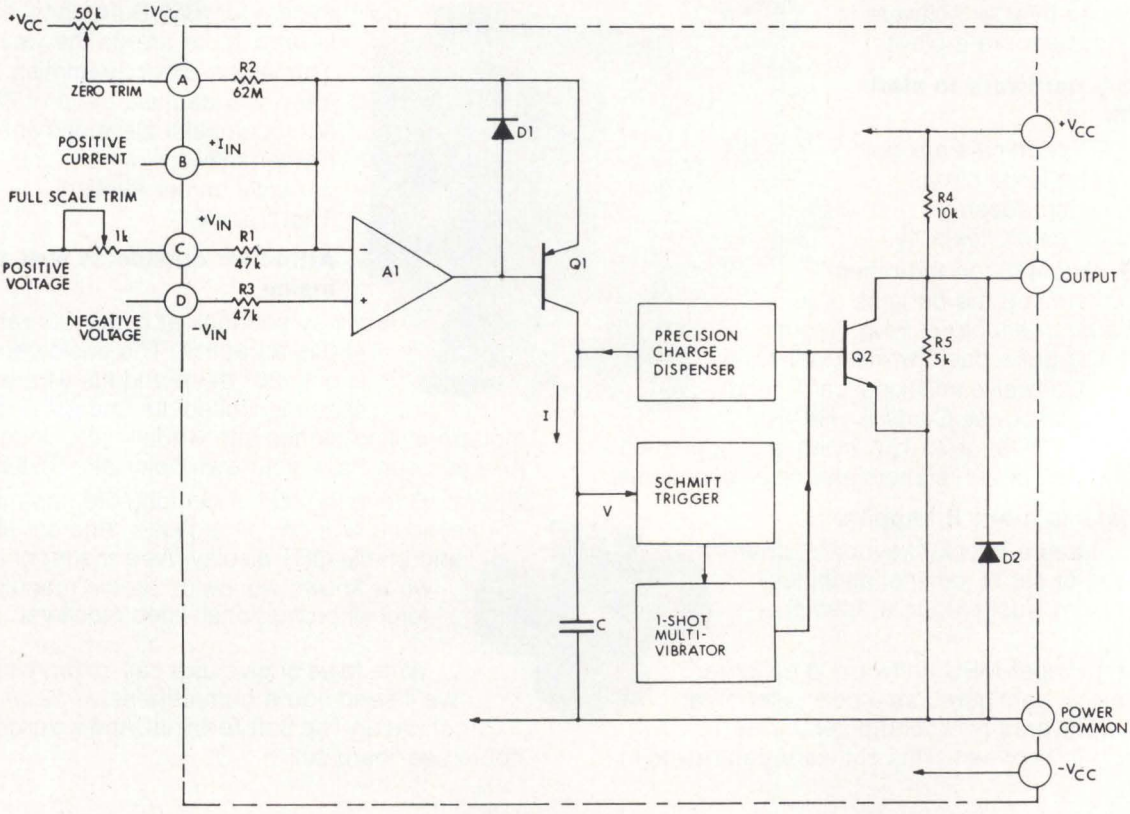
Circle 353 on Inquiry Card

10-kHz V-F Converters Give Linear Response Over Wide Temp Range

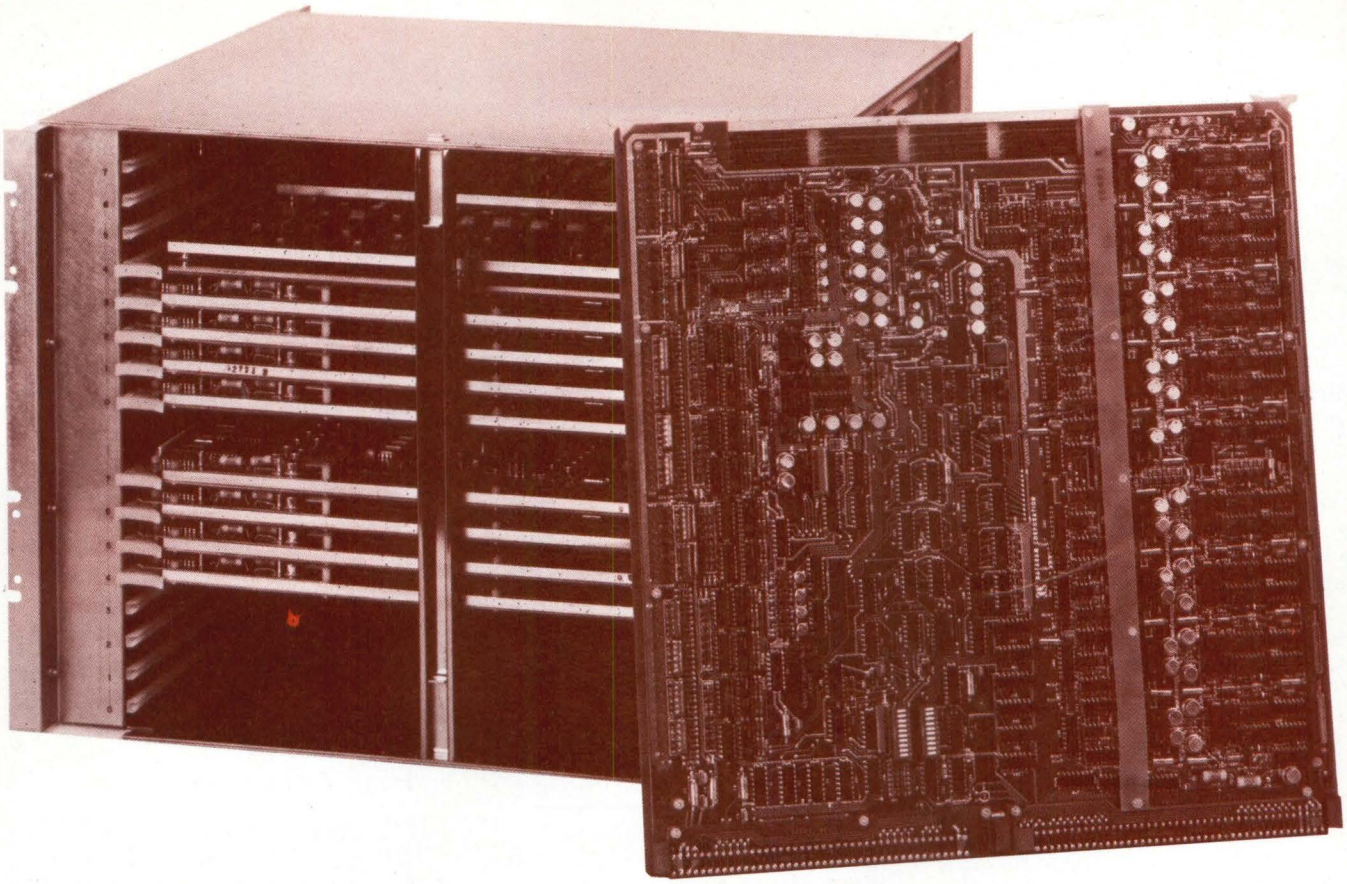
Low drift 10-kHz voltage-to-frequency converters, guaranteed over a −25 to 85 °C range, provide pulse trains whose repetition rates are a precision linear function of input voltage, having a nonlinearity of less than 0.005%, to 16 bits end point linearity. Differential linearity and dynamic range approach 20 bits. Linear characteristics are specified for input voltages from ±10 μV to ±13 V. Two versions of the V-F converter are produced by Teledyne Philbrick, Allied Dr at Rte 128, Dedham, MA 02026; these differ only in their temperature coefficients, which are ±50 ppm/°C for the 4727 and ±30 ppm/°C for the 4727-01.

Other capabilities include 80-dB CMRR and 30% overrange. The current input pin (summing point of an op amp) resolves currents as low as 250 pA, which makes possible operation with full scale input voltages from less than 250 mV to greater than 100 V, and allows offsetting to increase frequency response.

As shown in the block diagram, effective currents from inputs A, B, and C are summed at minus input of op amp A1. Op amp and transistor Q1 form precision current pump, producing current I from collector of Q1, which is linear function of A1 input currents. Current I charges capacitor C at rate which is precise linear function of 4727's input signal. When voltage on C reaches fixed pre-



Simplified block diagram of 4727 V-F converter. Device is free running (astable) voltage controlled multivibrator



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And now, Dataram's BULK CORE is available for Interdata users who want to go beyond the normal addressing boundaries of the host minicomputer. BULK CORE does it at much higher speeds and is all-electronic, and that means no moving parts. And a 15¾" BULK CORE system offers 2.0 megabytes of peripheral storage.

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cision threshold, Schmitt-trigger output changes state and triggers 1-shot (monostable) multivibrator, which produces constant width output pulse. Amplified by Q2, pulse functionally activates precision charge dispenser (PCD). Every time output pulse is produced, PCD discharges C to same "zero" level. Thus, C is repeatedly charged between two precise voltages at rate that is linear function of input signal to produce output waveforms.

This device can handle positive, negative, and differential input signals over a wide range of power supply voltages (±12 to ±18 V). Zero offset voltage, typically ±1 mV, is guaranteed to lie within ±3 mV, trimmable to zero.

Circle 354 on Inquiry Card

P/ROMs Switch Off 70 to 80% of Power When Unselected

Four newly announced field-programmable read-only memories, including power switched versions, are included in the 29000 series produced by Raytheon Semiconductor, 350 Ellis St, Mountain View, CA 94040. The 29624 (open collector) and the 29625 (3-state) are standard P/ROMS. Their power switched counterparts are the 29626 (open collector) and the 29627 (3-state). All four devices, available in standard 24-pin packages, have 4k-bit stores, organized as 512 x 4, and dissipate 850-mW maximum power.

A power-switched P/ROM designated as an "SPROM" is able to turn off most of its internal circuitry when unselected. In the unselected situation, power dissipation drops from the 850-mW level to 165 mW (for the 29626) and to 250 mW for the 29627. This capability causes only a 5-ns degradation in performance; two standard devices have a 50-ns access time over the commercial 0 to 75 °C range (70 ns over the military −55 to 125 °C range); the corresponding access times for the SPROMS are 55 ns (commercial) and 75 ns (military).

In contrast to previous power switching schemes employing external transistors and resistors, the SPROMS include all power switching circuitry on the same chip as memory. The power switch is activated by the same chip select input that is used to address a standard P/ROM. Therefore, in most cases, an SPROM can be substituted directly for a standard device without system redesign. Access times and full V_{CC} tolerance under power-switched conditions are guaranteed.

As with other members of the 29000 series, these devices (both standard and power switching models) are based on low power Schottky technology and employ nichrome fuses. They are shipped with all bits in the high (logical 1) state. A low state is produced by passing a short, high current pulse through the nichrome link, fusing the link open. Maximum ratings establish limits from −0.5 to 7 V for supply voltage relative to ground (continuous), dc voltage applied to outputs not to exceed 26 V during programming and otherwise falling between −0.5 V and V_{CC} max, and dc voltage between −0.5 and 5.5 V at the address inputs and between −0.5 and 33 V at the chip select input.

Circle 355 on Inquiry Card

Versatile 14-Bit Hybrid D-S Converter Comes in Small Package

Digital input representing angle is converted by a 14-bit hybrid to either resolver type sine/cosine or 3-line synchro output. The manufacturer (ILC Data Device Corp, Airport International Plaza, Bohemia, NY 11716) claims this to be the smallest digital-to-synchro or digital-to resolver converter available. It is a versatile function generator, able to generate a cartwheel rotating sweep for PPI displays, or convert from polar to rectangular coordinates. A variety of functions can be implemented because the reference input can accommodate any waveform with frequencies from dc to 1 kHz (including a sawtooth for CRT drive), and because the low scale factor variation (±0.2%) allows displays to be driven directly.

The HDSC-14 has applications in computer based systems in which digital angle information is processed, such as simulators, control systems, and moving target indicators in PPI displays. Its high reliability, low power consumption, and small size make it appropriate to uses involving remotely located or hard to access equipment. All units are processed to MIL-STD-883.

Other features include a short circuit proof ±2-mA rms output that is pin-programmable for synchro or resolver mode. A differential solid-state reference input with a high ac and dc common mode rejection eliminates the need for isolation transformers in most applications. The digital input, which is transient protected CMOS with internal pull-up resistors, is CMOS and TTL compatible. Output settles to final value in less than 20 μs for a 180-deg step.

Contained in a single 36-pin DDIP module, the device requires ±15-V power supplies, while the CMOS logic voltage can range from 4.5 to 13 V. Two standard operating temperature ranges are available: 0 to 70 °C and −55 to 125 °C. The hybrid module measures 4.8 x 2.0 x 0.53 cm and weighs 28 g.

Circle 356 on Inquiry Card

Fast Onchip DACs Operate at High Accuracy

Monolithic 8-bit digital-to-analog converters having 200-ns settling times for output current are compatible with 2650, 8080, and many other microprocessors. Available from Signetics, 811 E Arques Ave, Sunnyvale, CA 94086, the NE5118 features a ±0.2% accuracy, and the NE5119 a ±0.1% accuracy.

Data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. When the $\overline{LE}$ input (diagram) is in the low state, the latches appear transparent. Upon $\overline{LE}$ going high, the input data present at the moment of transition are latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

A stable voltage reference (5 V nominal) may be externally trimmed with a potentiometer for easy full scale adjustment while a low temperature coefficient is maintained. The output has high voltage compliance to increase versatility.

While operating temperature is 0 to 70 °C for the NE5118/9, the related SE5118/9 model can operate from −55 to 125 °C. Output dissipation of either is typically 255 mW.

Other features include 8-bit resolution and monotonicity and a full scale current drift of ±10 ppm/°C. Absolute maximum ratings are set at ±18-V supply voltage, 0- to 18-V logic input voltage, and 800-mW power dissipation for the NE and 1000 mW for the SE packages.

(Continued on p 206)

Buy the first page, get the second one free.

Our new smart terminal, the ADM-31, features a full two-page display as standard equipment. Not as an option. And its low cost and high reliability tell you it was made by those same people who make the world-famous Dumb Terminal.™ But the 31's similarity to the Dumb Terminal ends with its dependability and rugged, proven case.

THE ADM-31 PROVES DUMB IS ONLY SKIN DEEP.

The ADM-31 is completely self-contained, with full editing, formatting and protected fields capabilities. And equipped with keyboard, control logic, character generator, refresh memory, and interface. Not to mention a microprocessor which increases reliability and ease of use. You can even order it with a printer port option, and get printouts along with your readouts.

And the 31's behavior modification gives you a factory installed personality for an alternate ESC sequence lead-in — in addition to the standard ESC. And End Block character. A New Line character sequence. A field separator. And even a function sequence preamble.

THE ADM-31 IS ALL KEYED UP.

The ADM-31's 91-key solid-state keyboard is integrated with the main logic, and can generate all 128 ASCII characters. And it features an integral numeric key pad, with period, comma, tab, minus and numerals. All arranged in a familiar calculator format.

The ADM-31 comes complete with character insert/delete, line insert/delete, erase to end of line/field/screen, back tab, and six send sequences. All standard equipment.

And the Standard Edit feature lets the ADM-31 clear to protected spaces, clear to unprotected nulls, and set and reset copy-print.

As if that wasn't enough, the keyboard includes a caps lock key (to lock the keyboard into upper case only).

THE SMART CHOICE FOR A SMART TERMINAL.

After all this, you're probably thinking the ADM-31 is one of the smartest ideas to come along in quite a while. Modesty aside, we'd have to agree.

So if you're in the market for a new, smart display terminal, consider ours. Then give us a call, or contact your local distributor. We'll be glad to tell you all about our new ADM-31.

A terminal far too smart to be considered Dumb.

ADM 31
Two pages are better than one.

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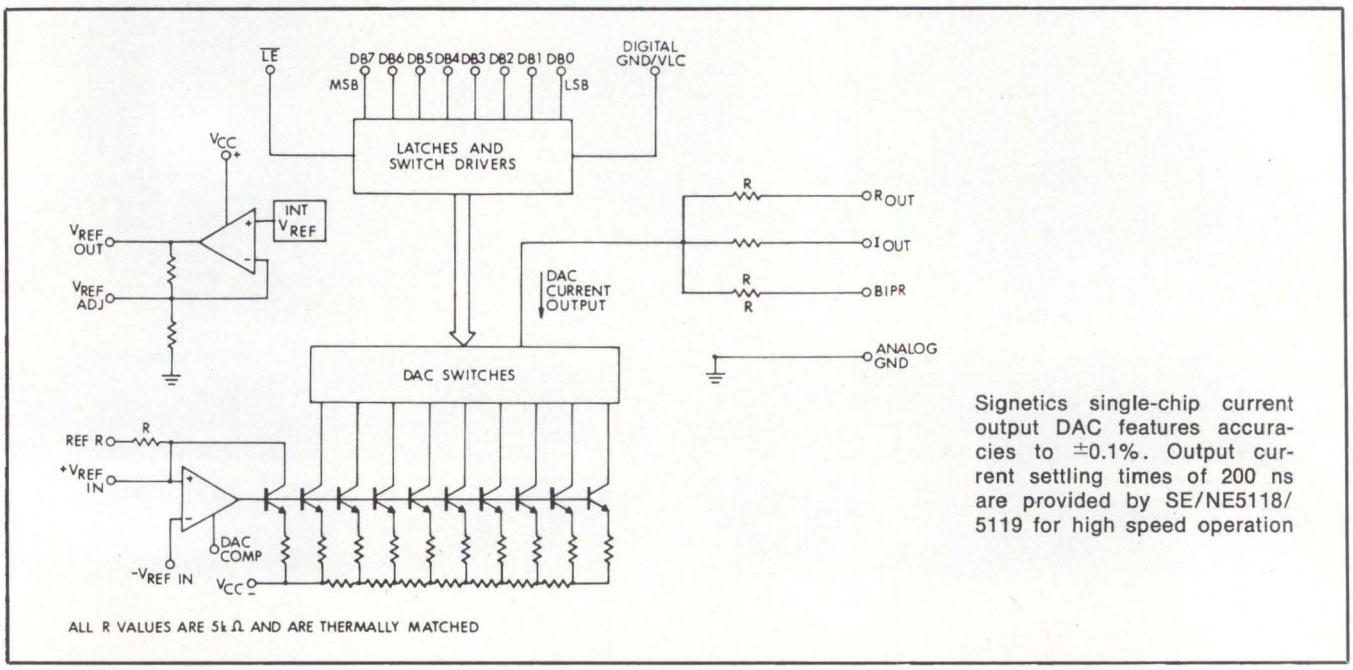
CIRCLE 106 ON INQUIRY CARD



Signetics single-chip current output DAC features accuracies to ±0.1%. Output current settling times of 200 ns are provided by SE/NE5118/5119 for high speed operation

Applications for the chip are precision 8-bit D-A converters, high speed 8-bit A-D converters, programmable power supplies, CRT display drivers, high speed modems, test equipment, and measuring devices. All versions of the converter are available in plastic and ceramic 22-pin DIPS. □

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Ampex minicomputers are available in your choice of 800 or 1200 nanosecond operation, and feature direct addressing of 64K words of core or MOS memory. There's even a version with 64K words of MOS memory right on the CPU board.

Of course they execute the Nova instruction set, and they're compatible with peripherals and controllers designed for use with Nova computers, but that's only the start.

You'll also find front access to all components, a single bus structure, and a programmer's console with octal pad input, octal readout and LED indicators. And options include automatic program load, firmware multiply/divide and power fail/auto-restart.

Three chassis configurations let you specify 5, 13 or 21 slot capacity. The 21 slot version accepts 17 boards plus a staggering 2 megabytes of Megastore—the Ampex solid-state alternative to fixed-head disk.

The technical story is in a free brochure, and the economic advantages will be obvious when we discuss quantity, dollars and cents. Write Ampex Memory Products Division, 200 North Nash Street, El Segundo, California 90245. Or call Charley Penrose at (213) 640-0150. Extra value makes *this* alternative the first choice.

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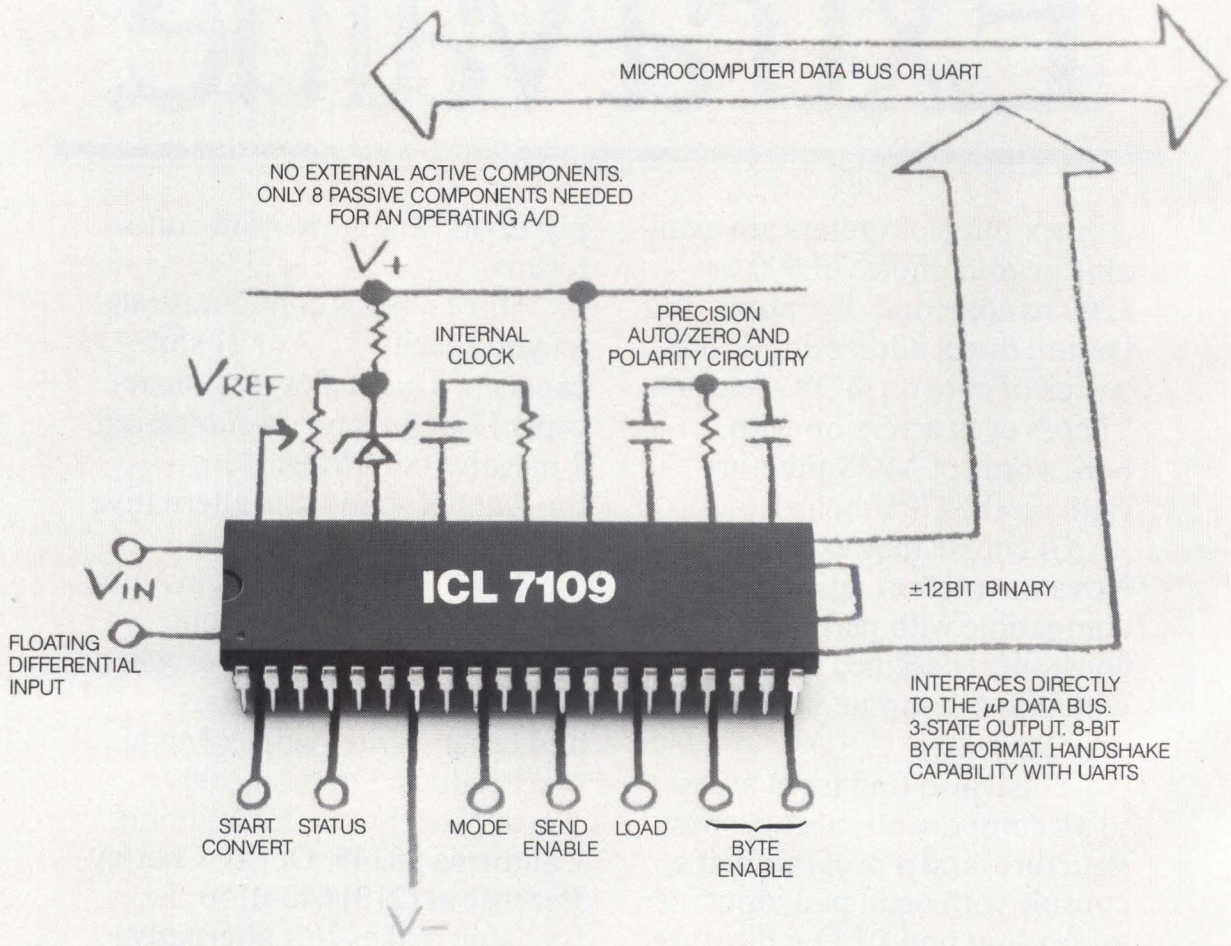
NOW, A 12-BIT A/D CONVERTER

THE 7109: $10*



*100 piece price in plastic

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Down goes the component count. The ICL7109 is the first ±12-bit binary, .01% accurate, single chip A/D converter with true handshaking capabilities for a wide variety of UART and μP data logging applications. On a single chip, the ICL7109 contains all active analog and digital circuitry necessary to accurately convert analog input into digital data. Byte oriented, three-state output allows the ICL7109 to interface directly with 8-bit and wider microprocessor data busses.

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The ICL7109's handshake ability allows it to interface directly with industry standard UART's for remote serial data transmission. Sequencing the output of the two 8-bit bytes is performed by the 7109 either synchronously with conversions, or on demand. Without the addition of any external components. Again, down goes the component count.

ANALOG FEATURES

- True differential signal and reference input
- Zero drift $<1\mu V/°C$
- Full scale <5ppm/°C (not including reference)
- Linearity $<0.01\%$
- Conversion rate of .1 to 7.5 conversions per second

DIGITAL FEATURES

- Direct interface with popular μP's (6100, 6800, 8048, 8080, etc.)
- Three-state byte organized outputs
- Run/hold input, status output
- UART handshake capability

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If you're sensing temperature, pressure, humidity, light intensity or any of a host of "real world" signals, the ICL7109 is your answer. One IC. Straight to the data bus.

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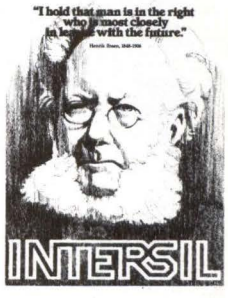

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_____Send me a free* sample of ICL7109CPL

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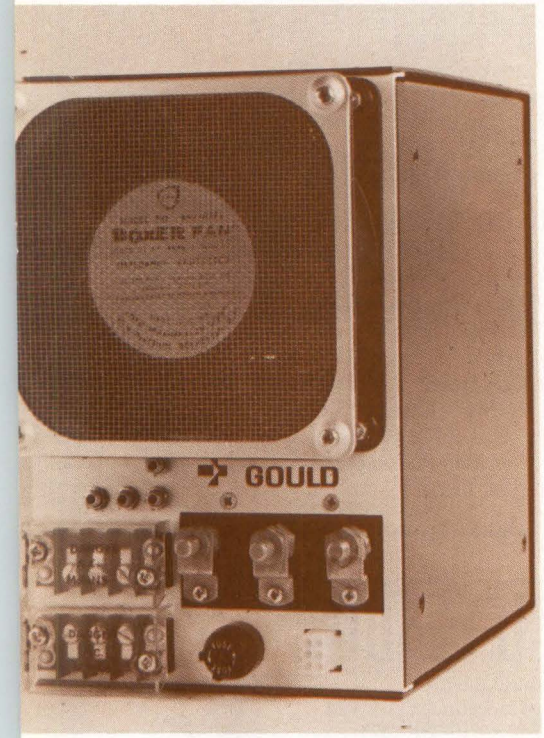
*For a free sample, attach this coupon to your company letterhead. Sample offer valid for the first 1000 industry requests received within 60 days of publication. One per person.

CD1178

PRODUCT FEATURE

Dual Output Switching Supply Gains High Power Density With Fan Cooling



Fan cooling in the dual output MGD 500 enables the unit to provide 1.2 W/in^3 (0.076/cm^3) and offers the facility for mounting in any plane. Designed specially to power systems using ECL circuits, Gould's switching power supply provides independently controlled 5.2- and 2.2-V outputs that track together, and produces total power output of 526 W in a package measuring 5 x 8 x 10.5" (12.7 x 20.3 x 26.7 cm), and weighing less than 20 lb (9 kg).

Description

Using the principle of direct offline conversion and half bridge inversion, the unit produces two independently controlled outputs. The voltage amplifier is a conventional detection circuit comparing the output voltage with a low temperature coefficient reference diode. An overvoltage protection circuit operates by causing a small signal thyristor to fire when the output voltage reaches a predetermined level, shutting down the drive circuitry and preventing drive power from reaching the main transistors. The current amplifier derives its signal from a current transformer in the primary circuit of the inverter and operates to override the voltage amplifier when the load current exceeds a preset level, thus placing the output in a constant current mode.

Specifications

Accepting inputs of either 115 or 230 Vac ±15%, at a frequency of 47 to 63 Hz, selectable from the front panel, the unit outputs 5.2 Vdc (±0.2 V), adjustable from 0 to 80 A, and 2.2 Vdc (±0.1 V), adjustable from 0 to 50 A, with a common positive terminal. Output returns to within 1% in less than 500 μs following a 50% load change. Under nominal input voltage at full load, the supply provides 28-ms hold-up in the event of primary power failure.

Regulation is within 0.2% on both outputs for a worst case combination of ±15% input and 0 to 100% load change. Ripple on both outputs is 10 mV rms max and 50 mV pk-pk (30 MHz bandwidth). Temperature coefficient is less than 0.01%/°C.

Standard features include overcurrent protection, adjustable from 70 to 110% constant current for both outputs, and overvoltage that is fixed at 7 V ±5% for the 5-V output only. The unit shuts down in the event that internal temperatures are excessive and resets after cooling.

Insulation voltage is 2.1k Vdc between input and ground and 500 Vdc between output and ground. Insulation resistance is not less than 50 mΩ at 500 Vdc.

There is no limit on parallel operation with other units. Units may be operated in series to a total voltage of 250 V max. Output voltage may be remotely programmed with a ±5% variation for system margin checking.

Price and Delivery

Single unit price for the MGD 500 is $698. OEM quantity discounts are available. Delivery is from stock. Gould Electronic Components Div, 4601 N Arden Dr, El Monte, CA 91731. Tel: 213/442-7755.

For additional information circle 199 on inquiry card.

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FAST is a whole new Schottky TTL logic family that delivers up to 75% more speed than Low Power Schottky, up to 20% more speed than Schottky, but at only 25% the power of Schottky. So now you can drive more circuits with less power. And put the power you save to work somewhere else.

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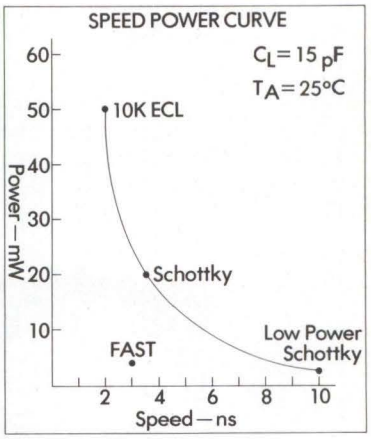


Give your TTL a boost.

If you're running with a Schottky/Low Power Schottky logic combination and you need more speed, you no longer have to go to ECL school to get there.

FAST cuts the speed difference between Schottky and 10K ECL to almost nothing. This gives you another generation of TTL logic. It drastically cuts design time. And it gives you more years out of your existing equipment and logic designs.

Strengthen your specs.

FAST gives you external gate delays of 4-4.5 ns over the full commercial and military temperature and voltage ranges while driving 50 pF load capacitance. Internal gate delays are 1.5 ns and power consumption is typically 4 mW per gate function. Input thresholds are 1.5 V and output drive is identical to 20 mA Schottky.

To find out how to cost-effectively rejuvenate your TTL systems, just contact your Fairchild sales office, distributor or representative today. Or use the direct line at the bottom of this ad to reach our Digital Division. Fairchild Camera and Instrument Corporation, P.O. Box 880A, Mountain View, CA 94042. Tel: (800) 227-8158, (800) 982-5805 (in California). TWX: 910-379-6435.

FAIRCHILD

Call us on it.

CIRCLE 110 ON INQUIRY CARD

ADVANCED TECHNICAL

Course 142 — Five days

Troubleshooting Microprocessor-Based Systems

LOS ANGELES
March 12-16

WASHINGTON, D.C.
March 19-23

DALLAS
March 26-30

BOSTON
April 23-27

PHILADELPHIA
April 30-May 4

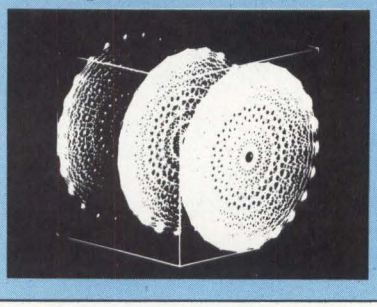
NEW YORK
May 14-18

Nearly all manufacturers, OEMs and end users are suffering from major production bottlenecks and customer service problems directly caused by the unavailability of trained personnel to test and troubleshoot microprocessor systems. This unique course is specifically designed for engineers and senior technicians involved in production testing, field service and design of microprocessor-based systems. The course provides these personnel with the practical knowledge they require, including an in-depth understanding of: a) microprocessor software and hardware; b) how to apply the most powerful microprocessor debugging techniques and c) how to use microprocessor troubleshooting equipment.

- **Hardware Design Fundamentals**
- **Programming Fundamentals**
- **Overview of Microprocessor System Troubleshooting**
- **Writing Diagnostic Software**
- **Troubleshooting & Test Equipment**
- **Using Logic Analyzers**
- **In-Circuit Emulators**
- **Signature Analysis Techniques**
- **Microcomputer Development Systems**
- **Pre-Planning Requirements**

Course 365 — Four days

Computer Graphics



ATLANTA
January 16-19

NEW YORK
February 13-16

LOS ANGELES
February 27-March 2

DALLAS
March 20-23

WASHINGTON, D.C.
March 27-30

DETROIT
April 17-20

BOSTON
April 24-27

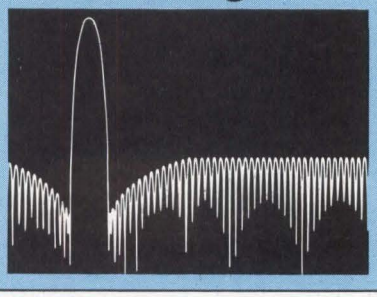
SAN FRANCISCO
May 8-11

Hardware elements of computer graphics systems are presented at the level required for detailed system specification, selection and acquisition. Software techniques for computer graphic systems are developed from the elementary level of line generation and continue through advanced approaches to animated three-dimensional color displays with hidden surface removal. Off-the-shelf, commercially available software packages are analyzed and evaluated. Emphasis is placed on hardware/software tradeoffs, cost effectiveness and the advantages and limitations of alternative approaches.

- **Display Hardware**
- **Color Display Techniques**
- **Two Dimensional Graphics**
- **Three Dimensional Graphics**
- **Transformations**
- **Software Structures**
- **The Hidden Line Problem**
- **The Hidden Surface Problem**
- **Software 'Build or Buy'**
- **Selection Methodology**

Course 412 — Five days

Digital Signal Processing



FT. LAUDERDALE
February 12-16

DALLAS
March 12-16

LOS ANGELES
March 19-23

PHILADELPHIA
April 2-6

WASHINGTON, D.C.
April 23-27

BOSTON
April 30-May 4

The objective of this course is to present the necessary fundamentals of digital signal processing in a clear and comprehensible manner, to develop an understanding of new processing techniques, to survey the state of the art of hardware and software available, and to apply this information to a range of concrete design examples. The course is of benefit both for those who wish to achieve a basic understanding of this exciting area, and for those whose interest is in advanced techniques and the implementation of practical systems.

- **An Overview of Applications**
- **Digital vs. Analog Signals**
- **Operations on Digital Signals**
- **Recursive Filters**
- **Nonrecursive Filters**
- **Design Techniques**
- **Computer Aided Design**
- **Statistical Approaches**
- **Spectral Estimation**
- **Application Case Study**

COURSE ENROLLMENT INFORMATION

Course Hours:

Orientation (First Day): 8:15–9:00 A.M.
Lecture Sequence: 9:00 A.M.–4:30 A.M.
Informal Discussion Session with Instructor: 4:30–6:30 P.M.

Course Fees:

Four-Day Courses: (365, 445, 440): **$695.00** (U.S.)
Five-Day Courses: (412, 142): **$795.00** (U.S.)

Microprocessors and Microcomputers Series

Individual Courses: 111 or 102s (One Day): **$195.00** (U.S.)
130 (Three Days): **$495.00** (U.S.)
Combinations: 111 and 102s (Two Days): **$390.00** (U.S.)
102s and 130 (Four Days): **$595.00** (U.S.)
Complete Series: 111/102s/130 (Five Days): **$695.00** (U.S.)

Course Fees Include: lectures, lecture-coordinated notes, extensive reference materials, luncheon & coffee breaks.
Team/Group Discount: 10% reduction for three or more participants from the same organization, if invoiced at the same time.

DIPLOMA/CONTINUING EDUCATION UNITS

Each attendee receives a Course Completion Certificate awarding one Continuing Education Unit (CEU) for each ten hours of class participation. The CEU is a nationally recognized unit awarded by universities and educational organizations for participation in continuing educational programs.

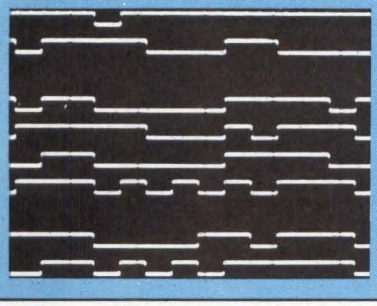
EDUCATION

INTEGRATED COMPUTER SYSTEMS, INC.

Course 445 — Four days

Data Communications

Digital Techniques and System Design



LOS ANGELES
December 12-15

DALLAS
January 23-26

CHICAGO
February 6-9

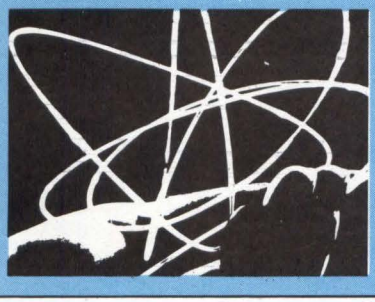
WASHINGTON, D.C.
March 13-16

This course is designed for engineers, scientists and system designers who are involved in the planning, design or implementation of all types of digital communications systems. The course covers the fundamental principles of signal conversion, encoding/modulation, data transmission and error control. It analyzes the individual elements of a data communication system and clearly describes how these elements may be synthesized to form a system which best meets application specific objectives.

- **Coding for Data Transmission**
- **Detection of Data in Noise**
- **Digital Modulation**
- **Security Considerations**
- **Errors and Error Control**
- **Analog to Digital Conversion**
- **Pulse Code Modulation (PCM)**
- **Signal and Video Encoding**
- **Packet Switching/ Packet Radio**
- **Implementing a Data Communications System**

Course 440 — Four days

Fiber Optic Communication Systems



WASHINGTON, D.C.
February 27-March 2

DALLAS
March 13-16

LOS ANGELES
April 3-6

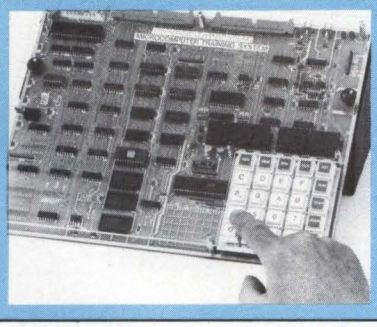
NEW YORK
May 1-4

This course is designed for engineers, scientists and managers involved in the planning, design and implementation of all types of communication systems. The course covers the fundamental principles of fiber optic based systems, and the state of the art in system components including light sources, optical fibers, single and multifiber cabling, fiber coupling, photodetectors, receiver and repeater technology, and fiber optic networks. Commercially available components will be surveyed to illustrate design techniques for the cost effective, practical application of this important new technology.

- **Advantages of Fiber Optics**
- **Optical Fiber Transmission**
- **Cabling Technology**
- **Light Sources**
- **Detection Technology**
- **Receiver/Transmitter Technology**
- **Modulation Techniques**
- **Digital Communications**
- **Data Bus Design**
- **System Design and Analysis**

FIVE-DAY COURSE SERIES

MICROPROCESSORS & MICROCOMPUTERS



LOS ANGELES
January 15-19

DENVER
January 22-26

DALLAS
January 29-February 2

FT. LAUDERDALE
February 5-9

WASHINGTON, D.C.
February 26-March 2

NEW YORK
March 12-16

PHILADELPHIA
April 2-6

Course 111: One day — Monday

MICROPROCESSOR PROJECT MANAGEMENT
From design through manufacture, QA and field service

Course 102s: One day — Tuesday

MICROPROCESSORS AND MICROCOMPUTERS:
A Comprehensive Technical Introduction and Survey

Course 130: Three days — Wed., Thurs., Fri.

HANDS-ON MICROCOMPUTER PROGRAMMING AND INTERFACING WORKSHOP
EACH student receives a complete 8080 microcomputer and interfacing system for his personal use throughout the course.

☐ PLEASE ENROLL ME IN **COURSE:**_____

CITY_____

DATE(s)_____

MAIL TO:
Integrated Computer Systems, Inc.
3304 Pico Blvd., P.O. Box 5339
Santa Monica, CA 90405
OR:
Integrated Computer Systems, Inc.
300 N. Washington St., Suite 103
Alexandria, VA 22314

OR CALL:
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LOS ANGELES
OR
(703) 548-1333
WASHINGTON, D.C.

A confirmation letter with complete details will be forwarded to you.

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Address_____

City_____

State_____ Zip_____ Telephone_____

☐ Please send FREE BROCHURES describing these courses.
☐ Please put me on your mail list to receive future course schedules.

CIRCLE 111 ON INQUIRY CARD

PRODUCTS

P/ROM Programmer Couples Large Memory With Powerful Software to Handle Large Devices

Large RAM coupled with powerful system software allows the System 19 to program 32k, 64k, and 128k devices. Self-tests and error detection are completely automatic. Hexadecimal keyboard and display, and simple single-key operations provide operator flexibility in sophisticated data editing. Plug-in Programming Paks, which give the correct currents and voltages for max programming yields and long term reliability, can be changed without disturbing RAM memory. This allows programs to be partitioned into different device configurations, ie, data can be loaded into RAM from a 32k MOS EPROM and then loaded out into four 8k bipolar P/ROMs. Equipped with a 4k x 8 (32k-bit) RAM (expandable to 16k x 8 or 128k bits) for data storage, the system interfaces readily with terminals, computers, and microprocessor development systems. An integral dual function serial port comes std with the unit, which will accommodate RS-232-C and 20-mA current loop, full or half duplex. Baud rates are

externally switch selectable from 50 to 19,200. **Data I/O Corp,** 1297 NW Mall, Issaquah, WA 98027.
Circle 200 on Inquiry Card

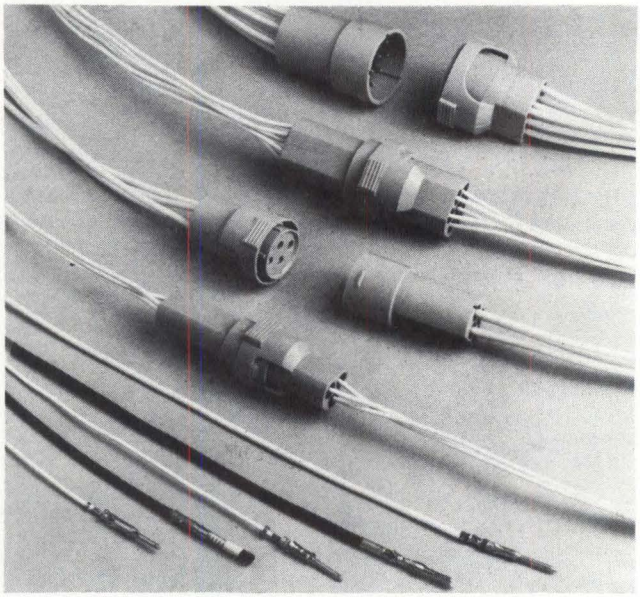
2-Wire, Full-Duplex 2400-Bit/s Modem Operates Over Dial Networks

Circle 201 on Inquiry Card

Permitting 2400-bit/s operation in a full-duplex mode on 2-wire dial or dedicated lines, the LSI 24/24 allows upgrade of networks operating with 1200-bit/s full-duplex 2-wire modems such as Bell 212, can be used with full-duplex prototcols such as SDLC, HDLC, BDLC in dial applications over satellite circuits without loss of throughput, provides dial-up full-duplex 2400-bit/s tail circuits when used with high speed modem having built-in multiplexer, and can achieve throughput the same as or better than 4800-bit/s half-duplex modems in dial applications with half-duplex protocols, depending on message block characteristics, transmission delay, and line turnaround. Supplementing std operation at 2400 bits/s is a 3200-bit/s fallforward capability for especially good lines, as well as 1600-bit/s fallback mode for poor quality connections. An optional built-in asynchronous adapter provides dial network operation for most asynchronous terminals as well as conventional synchronous operating mode at this speed. **Codex Corp,** 15 Riverdale Ave, Newton, MA 02195.

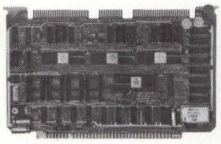
Standard Fiber Optic Connector Housings Permit Mix of Power, Signal, and Coaxial Cables

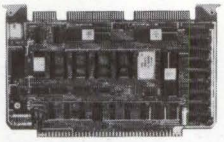
Multimate fiber optic ferrules permit assembly of power, signal, coaxial, and fiber optic cables in a single std connector housing, allowing various cable types to be intermixed to optimize connector system design. The ferrules are resilient to help maintain core centering, eliminate the effects of inherent initial tolerance differences in fiber size, and help cushion the fiber against damaging vibration and other mechanical problems. Decibel losses can be held to 2 dB. Efficiency of the ferrules permits assembly in low cost plastic connector housings. The connector's male and female ferrules are virtually identical; the female side is distinguished by a plastic alignment bushing. Body of the ferrule is molded of resilient thermoplastic, then fitted into a brass retention sleeve. Retention springs are stainless steel and compression springs are cadmium plated music wire. Designed to fit size 16 connector cavities, the ferrules accommodate 400- to 600-μm and 1125-μm dia single optical fibers, jacketed to a max of 90 mils dia. **AMP Inc, Industrial Div,** Harrisburg, PA 17105.
Circle 202 on Inquiry Card

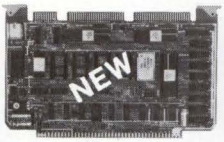


The one word for microcomputer systems: Micromodules.

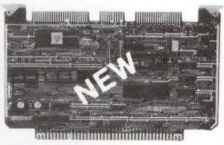
Monoboard Micro computers


M68MM01


M68MM01A



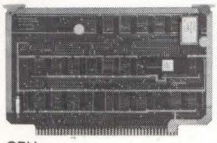
M68MM01A2

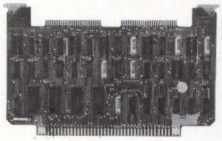


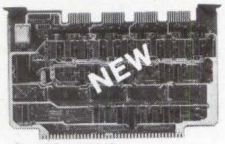
M68MM01B

M68MM01B1

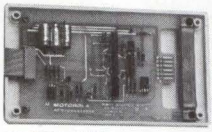
Modular Microcomputer Subassemblies

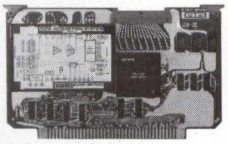

CPU
M68MM02

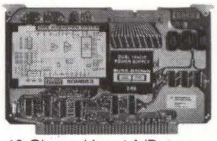

32 Input/Output
M68MM03

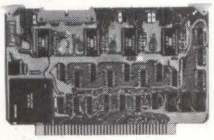


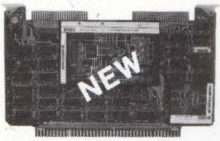
Quad Serial I/O
M68MM07 Coming 4th Qtr.


RS-232 to TTY
M68MM11


8-Channel Input A/D
M68MM05A

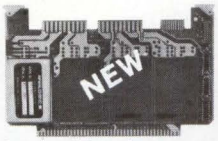

16-Channel Input A/D
M68MM05B


4-Channel Output D/A
M68MM05C

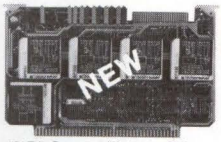


12-Bit 16/32 Channel D/A
M68MM15A/15A1

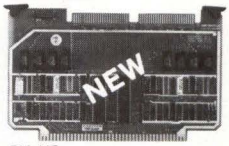
16-Bit Low-Level A/D
M68MM15B



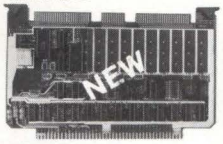
Low-Level Expander
M68MM15BEX



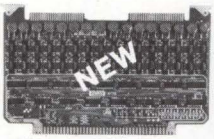
12-Bit Current/Voltage D/A
M68MM15C



PIA I/O
MEX6821-2



ACIA-SSDA Interface
MEX6850-2

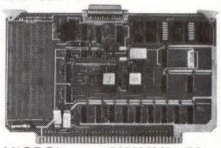


16/32 Isolated Relay
Output Channels
M68MM13A/13B

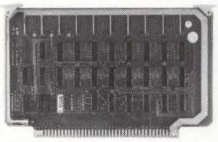
24 Channel Optically Isolated
Digital Input
M68MM13C/13D

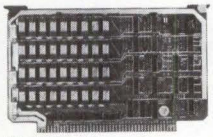
16 Solid State Relay
Input/Output
M68MM23 Coming 4th Qtr.

Program Debug

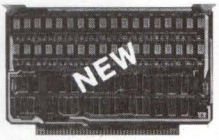

MICRObug for M68MM01/02
and M68MM01A/02A
M68MM08/08A

Memory Modules

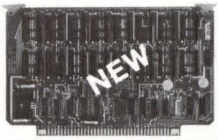

8K/16K EROM/ROM
M68MM04


2K Static RAM
M68MM06

8K/16K Static RAM
MEX6808/6816-22S



16K/64K Dynamic RAM
MEX6816/6864



16K/64K Hidden Refresh RAM
MEX6816/6864-1HR

Micromodules in development now

- **IEEE 488-1975 Functions**
  M68MM12/12A
- **Hardware Arithmetic Processing**
  M68MM14
- **MC6809 Monoboard Microcomputer**
  M68MM19
- **1.5 & 2.0 MHz Versions of Selected Micromodules**

The broad range of microcomputer system design options open with Motorola's Micromodules has been enlarged to an even greater capability by a host of recent additions to the line.

You get this wide variety of system configurations whether you select the Monoboard Microcomputer approach or choose to mix-and-match with the subassembly modules. Micromodules are fully supported with software, disk operating system, and an accessory line of power supplies, card cages, and chassis.

The five standard Micromodule 1 series Monoboard Microcomputers all are based on either the MC6800 or MC6802 microprocessor. They vary primarily in I/O and memory.

Modular microcomputer subassemblies include the CPU and a selection of I/O, Isolated I/O, A/D and D/A, Memory, and Debug modules. These are supplemented by additional capability in the form of fully-compatible EXORciser* memory and I/O boards. Family compatibility also permits the simple expansion of any Micromodule microcomputer system, whether it be monoboard or modular.

Contact your Motorola sales office or your authorized Motorola distributor for additional information on Micromodules, the one word for microcomputer systems. We will respond promptly to itemized letterhead requests for data sheets addressed to Motorola Microsystems, P.O. Box 20912, Phoenix, AZ 85036.

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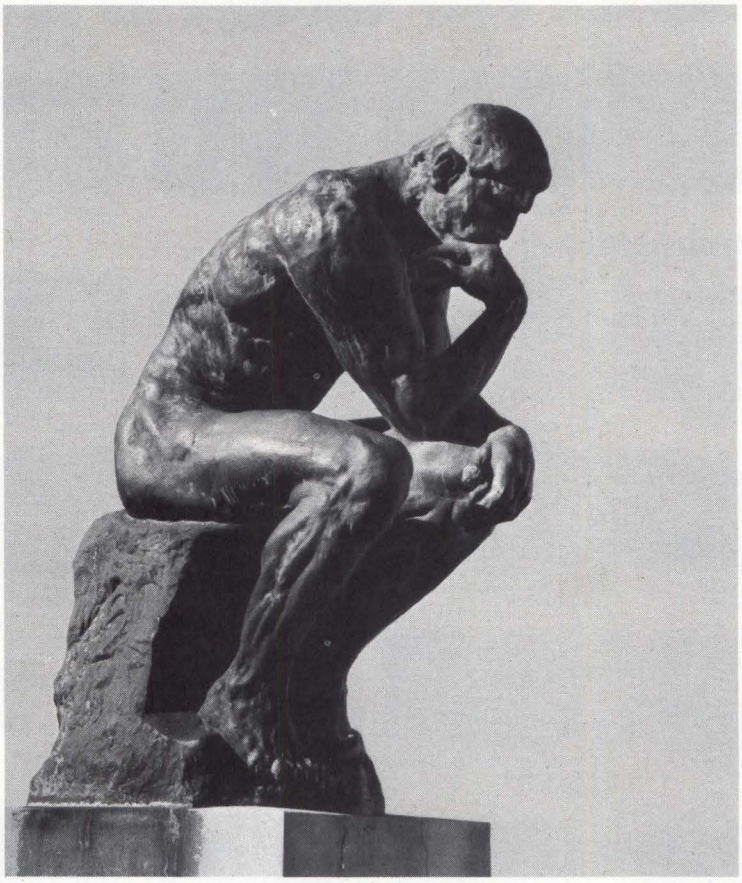
Thinking of adding mass memory to your S-100 bus?



Think twice!

You say you're ready for greater storage? Well now, with average access times of 28 milliseconds, large, on-line direct access cartridge disk files have become a reality in microcomputing. And, ALPHA MICRO offers you not one, but TWO ways to vastly increase your system capacity...and do it without overtaxing your budget.

First, there's the ALPHA MICRO AM-500™ Hard Disk Subsystem. It uses the popular CDC 9427H (Hawk) cartridge disk drive with a total of 10 megabyte capacity (5 fixed, 5 removable). The AM-500 comes complete with interface formatter/controller, cabling, and disk drive. You can expand your mass memory to meet your requirements, in 10 megabyte increments, up to 40 megabytes.

Thinking of even more mass memory? Check out the ALPHA MICRO AM-400™ Hard Disk Subsystem. It features the CALCOMP TRIDENT Series Hard Disk Drive in a choice of models with 25, 50, 80, 200, or 300 megabyte capacity. And, you can daisy-chain up to four units, on-line, in any mix. How's that for capacity?

So, if you're thinking of adding mass memory to your S-100 bus, be sure to check out the ALPHA MICRO AM-400 or AM -500 Hard Disk Subsystem at your nearest ALPHA MICRO Dealer. And while you're there, ask him to show you the rest of the ALPHA MICRO hardware and software lines.

AM 400™

AM 500™

alpha micro

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PRODUCTS

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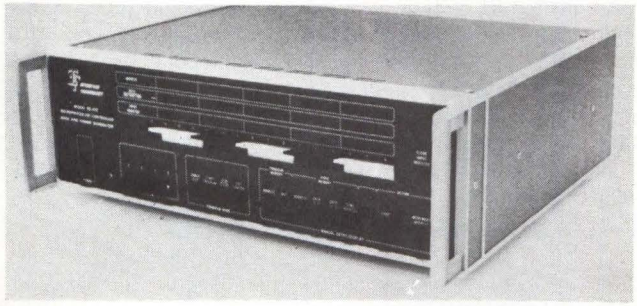

RST-432, for use as a subsystem component of large ATE systems, provides digital signal generation, comparison detection, and recording capabilities for checkout of digital circuits. The unit receives programming data for its internal microprocessor, data patterns for clock generation network, and data patterns for transmission to the DUT, directly from the master computer via an IEEE 488-1975 interface. Upon command it performs specific test and reports results and recorded data patterns to the master computer. Test results can be monitored visually on the front panel or read back via the interface. Microprocessor program memory can store up to 256 instructions programmed by the user. **Interface Technology,** 852 N Cummings Rd, Covina, CA 91724.
Circle 203 on Inquiry Card

MINIATURE THERMAL ALPHANUMERIC PRINTER

A self-contained, panel mounting unit that prints 20-col, APP-20 has the same panel mounting and outline dimensions as the DPP-7, and includes microprocessor based interface electronics and ac power supply in its housing. With outline dimensions of 4.44 x 2.70 x 8.75" (113 x 69 x 222 mm), the device prints the full ASCII char set of u/lc letters, numerals, and punctuation, across 2.25" (57.2-mm) wide thermal paper. A dot line thermal printhead forms 5 x 7 matrix chars which are 0.11" (2.8 mm) high. Printing rate is 1.5 lines/s and a 150' (45.7-m) roll holds about 9000 lines of data at 5 lines/in (2/cm). A dual voltage transformer offers switch selected input power of 115 or 230 Vac ±10% at approx 25 W max. **Datel Systems, Inc,** 1020 Turnpike St, Canton, MA 02021.
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Transmitting and receiving computer generated data at 4800-bits/s over std, unconditioned, and dedicated 3002 telephone lines at distances up to 50 mi (80 km), the 3002 also operates over twisted pairs, loaded wire cables, and carrier systems with frequency shift up to ±20 Hz. Cost-effectiveness is achieved by elimination of automatic equalizer required by conventional modems. Std operating modes are full-duplex, 2- or 4-wire; half-duplex, 2-wire; point to point; and multipoint. An asynchronous option allows operation with asynchronous terminals; a dual channel option allows two 2400-bit/s channels, synchronous or asynchronous, to utilize a single modem. **Avanti Communications Corp,** Box 205, Broadway Sta, Newport, RI 02840.
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PRODUCTS

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Testing analog PC boards with up to 128 nodes, the 2230I, based on the company's model 2230 component test system, adds special software to simplify board description and test conditions, lower test signal levels, and 4k words of RAM. Together these features allow a 100-component PC board to be tested in 5 to 10 s, with data printout on faulty components. Programming is done using an English language-like macroinstruction keyboard that allows entry of component part number, scanner connections, test type, and limits. Entered programs, stored on convenient magnetic strip cards are loaded into the system for each type of PC board tested. Testing is initiated by pushing a button. **GenRad, Inc,** 300 Baker Ave, Concord, MA 01742.
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PARALLEL I/O PROCESSING FOR MIL-SPEC COMPUTERS

The 1626 I/O processor extends I/O capabilities of any of the company's CPUs. By operating in parallel with its controlling (host) processor, the unit efficiently assumes the burden of processing slow devices. A 16-bit dedicated processor compatible with the 1602 instruction set, the IOP consists of chassis with 16 external connectors, model 5606 single-board CPU, model 5615 power supply, max of 2 model 2033 8k semiconductor memory modules, model 3565 control host interface module, and 10 slots for I/O modules. Each semiconductor module provides 8k x 17 bits of static RAM. Parity checking and generating circuits can interrupt or halt the unit in the event of a parity fault. **ROLM Corp,** 4900 Old Ironsides Dr, Santa Clara, CA 95050.
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Containing 2 rows of 16 char each, for use in point of sale terminals, microcomputer displays, and similar applications, the 3200 consists of the LCD 5 x 7 dot matrix display with multiplexed driving circuits mounted on a PC board. Dimensions are 162 x 67 x 15 mm with 8.6 x 6.0-mm high display char. A patented charge compensation circuit reduces interdisplay crosstalk, resulting in a higher degree of contrast. Proprietary module drive electronics temperature compensate for the multiplexed matrix LCD, allowing display operations from 0 to 50 °C. The module runs off a 12-Vdc supply voltage, and draws 14 mA dc. It is designed for mounting on a sloping panel. Typ contrast ratio is 20:1. **Hamlin, Inc,** Lake & Grove Sts, Lake Mills, WI 53551.
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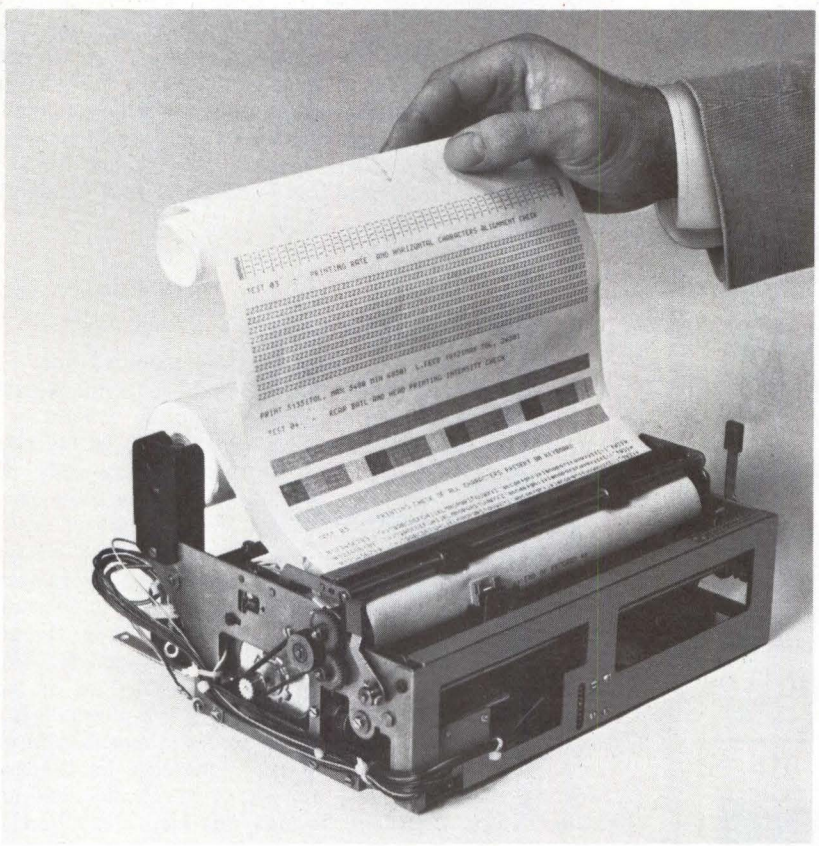

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Based on the world-famous LSI-11, the WH11 brings you amazing computer power and versatility at a great low price. And it's supplied with 4K memory and complete paper tape software including utilities plus BASIC and FOCAL — at no extra charge!

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WH11-16 16K MEMORY MODULE

Provides 16K dynamic MOS RAM on a 5 x 8½" board. Has on-board refresh, 570 nS cycle time and 250 nS access time. DEC designation MSV11-DC.

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WH11-32 32K MEMORY MODULE

Identical to 16K at left, but with 16 additional IC's for a total of 32K memory. DEC designation MSV11-DD.

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LA36 DEC WRITER II PRINTER TERMINAL

Provides hard-copy computer readout for the H11. Has 7 x 7 dot matrix print head; 10, 15 and 30 cps print speeds; variable width forms handling from 3" to 14⅞"; adjustable left and right hand tractors, half or full duplex operation.

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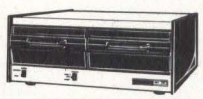
FULLY COMPATIBLE WITH LSI-11.



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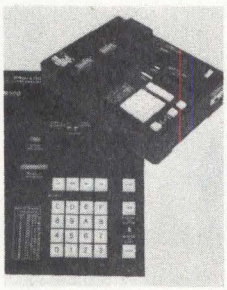
PRODUCTS

BUFFERED P/ROM PROGRAMMER

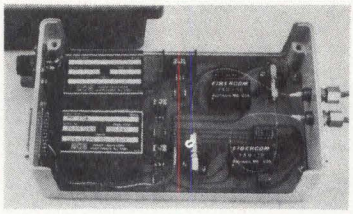


M900B has a 2k x 8 CMOS read/write buffer memory that allows ac power to the unit to be removed for up to 1 min with no loss of data in the memory. The user can thus remove one P/ROM personality module and replace it with another, easily transferring data between P/ROM types and sizes. Buffer memory can also be switched out for direct P/ROM to P/ROM copying. Advantages include ability to load data into the buffer and verify it before programming begins, and increased speed of communication because the unit supplies programming data in uninterrupted serial bit stream operation. Data location shift capability permits blocks of addresses stored in the buffer to be moved to any location within the P/ROM being programmed. **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940.

Circle 209 on Inquiry Card

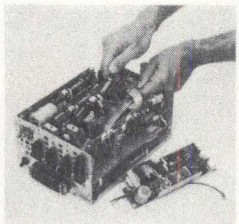
FIBER OPTIC DUPLEX LINK

Fibercom® full-duplex links using field prepared fiber optic cables for interconnection have either TTL or RS-232 interfaces and are capable of operation from dc to 500k or 5M bits/s, depending on model. Field preparation of the plastic clad fused silica fiber optic cables used with the links consists of mechanical procedures which can be learned by competent installers in an hour of instruction and practice. Options include optical sources for operation to 200 m or to 2000 m or more, power from 115 Vac, 50- to 400-Hz single-phase lines, or from user-supplied ±15 to ±24-V sources, compression entry fittings, and source detector fiber interfaces for Belden as well as Valtec PC-10-01 and PC-10-02 plastic clad fused silica cables. **Radiation Devices Co, Inc,** 10026 York Rd, Cockeysville, MD 21030.



Circle 210 on Inquiry Card

MULTIPLE OUTPUT SWITCHING POWER SUPPLY



SM MultiSwitcher employs multiple switching power supplies operating from a common dc bus, derived directly from the ac line. Switching frequencies of individual supplies are synchronized to prevent interaction. Type SM2 is housed in a 5.5 x 5 x 11" (13.97 x 12.7 x 27.9-cm) package, is fan cooled, and provides a max of 3 separate outputs, delivering a total of approx 400 W. SM3 is housed in an 8 x 5 x 11" package (20.3 x 12.7 x 27.9 cm), is fan cooled, provides a max of 4 outputs, and delivers approx 600 W. Each series consists of a 5-V, 45-A switcher as part of the mainframe package. Individual modules can be added to make up a multioutput supply meeting specific requirements. **Todd Products Corp,** 123 Milbar Blvd, Farmingdale, NY 11735.

Circle 211 on Inquiry Card

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Mark Stamp Steel, a division of Mohawk Data Sciences Corp., engineers and manufactures quality print drums, print wheels, type slugs and similar character elements for some of the largest printer and teleprinter manufacturers in the world.

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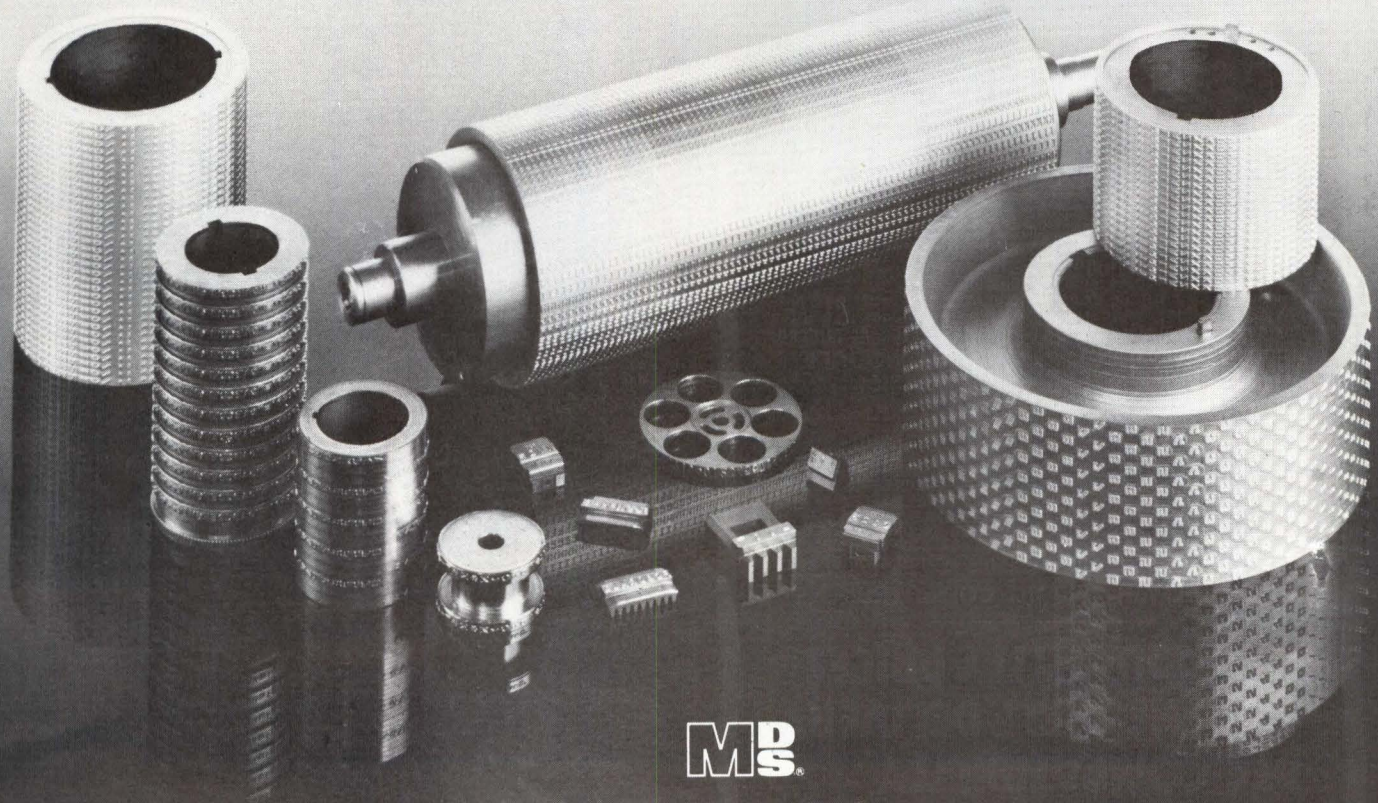
CIRCLE 116 ON INQUIRY CARD



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PRODUCTS

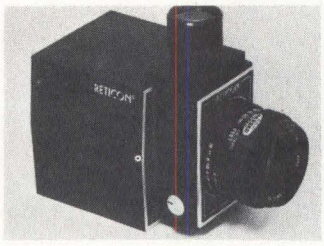
FIBER OPTIC DIRECTIONAL COUPLER

Design and optical characteristics of model TC4-A, -B, and -C allow bidirectional information transmission on a single, hair-thin, optical fiber. Available in a range of coupling ratios, devices are designed for use as both taps and feeds in fiber optic systems. Used as taps, the couplers divide the optical power in a single channel and distribute it among one or more secondary channels. As feeds, they can feed signals from one channel into another to merge channels to or from an optical source. TC4 models have 4 I/O ports. Light entering through any port is cross-coupled to both fibers on the opposite side. Insertion losses are well below 1 dB, and directivity is greater than 40 dB. **Canstar Communications,** 1240 Ellesmere Rd, Scarborough, Ontario M1P 2X4, Canada.

Circle 212 on Inquiry Card

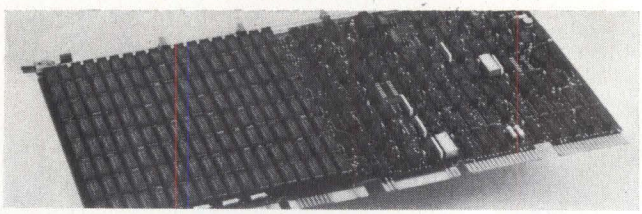
100 x 100-ELEMENT SOLID-STATE IMAGE SENSOR CAMERA

MC520 uses a solid-state photodiode array having excellent uniformity, smooth spectral response, low blooming characteristics, and 200:1 dynamic range. Functionally similar to a vidicon TV camera, but having greater geometric accuracy, higher scan rates, digital outputs, small size, low voltage and power requirements, and ruggedness and reliability, the camera uses a 100 x 100 photodiode array image sensor which requires no semitransparent electrode and therefore provides superior sensitivity and spectral uniformity. The unit features 10k pixels in a 100 x 100 matrix configuration and can be scanned at variable data rates up to 5 MHz (500 frames/s). Each pixel is spaced on 60-μs centers. **Reticon Corp,** 910 Benicia Ave, Sunnyvale, CA 94086.



Circle 213 on Inquiry Card

256k-BYTE ADD-IN MEMORY CARD



Supplying a full 256k bytes (128k x 18 bits) of add-in memory in a single card slot of Digital Equipment PDP-11/04 and /34 minicomputers, the MS11/34Q uses dynamic NMOS RAM with read access time of 300 ns and write cycle time of 450 ns max. Onboard parity generation and checking circuits, normally contained in the DEC M7850 parity controller, are incorporated to eliminate need for a controller and improve bus access by eliminating extra read and write transfer cycles required by the separate controller. Address and data latches insulate memory operation from spurious bus noises and improve system throughput by making the bus available in 100 ns on write operations. Depopulated versions of the board supply 96k and 64k words, with nonparity, 16-bit word versions available as an option. **National Semiconductor Corp, Computer Products Gp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

Panasonic electrosensitive alphanumeric printers.

When you're this small, you don't have to make a lot of noise about your low price.

Print in silence and print at low cost with our electrosensitive alphanumeric-plus printer Model EUY-10E.

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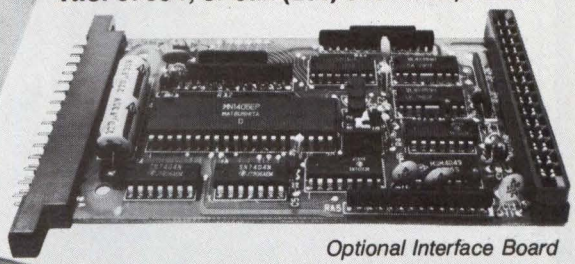
It isn't even the fact that the package is small (4.33″L x 3.5″W x 1.5″H). That makes it great in tight applications like POS cash registers, electronic calculators, data loggers, home computers and general peripherals—anywhere, in fact, where inexpensive hard copy is required.

The real achievement was to pack so much character-forming flexibility in that tiny space. We did it, with a 5 x 7-dot matrix that prints up to 128 different characters or symbols (including a full ASCII character set) on either 15, 21, 32 or 48 characters per line at just 530 msec per line with legibility that's sharp and clear.

There are four models to choose from, each with reliability designed-in by eliminating all moving parts except the print head and the paper.

To make it easier for you to get rid of noise, bulk and big pricetags, we've also made the EUY-10E easy to talk to. For quick microprocessor compatibility, we supply a 4-bit 1-chip microcomputer on a pre-programmed plug-in board that meets a variety of interfacing requirements, including that 128-strong variety of character formations.

For specifics on how beautiful small can be, write for information and prices to: Panasonic Electronic Components, One Panasonic Way, Secaucus, N.J. 07094; or call (201) 348-7282/7289.



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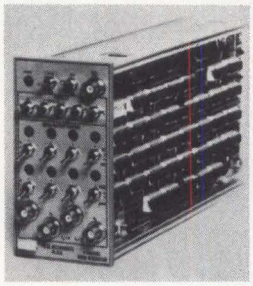
CIRCLE 121 ON INQUIRY CARD

PRODUCTS

ULTRA HIGH SPEED PROGRAMMABLE GENERATORS

Operating on the IEEE 488 bus, with each GPIB handshake averaging 1.25 μs, or directly in ASCII, generator models include a 14-MHz, model 820, function generator that offers sine, squarewave, ramp, triangle, and dc functions; trigger/gate; offset; 30-V pk-pk; IEEE 488 bus; and ASCII. The 845, a 14-MHz pulse/function generator, in addition to function features, provides true pulse and crystal referenced clock frequencies together with programmability of pulse delay, width, offset, amplitude, and mode. The 20-MHz model 860 retains ultra high speed while using an auxiliary microprocessor to provide store, recall, and learn modes for 20 sets of programmed parameters, which are retained even in a power-off condition. **Interstate Electronics Corp,** 707 E Vermont Ave, Anaheim, CA 92803.
Circle 214 on Inquiry Card

4-CHANNEL x 32-BIT WORD GENERATOR

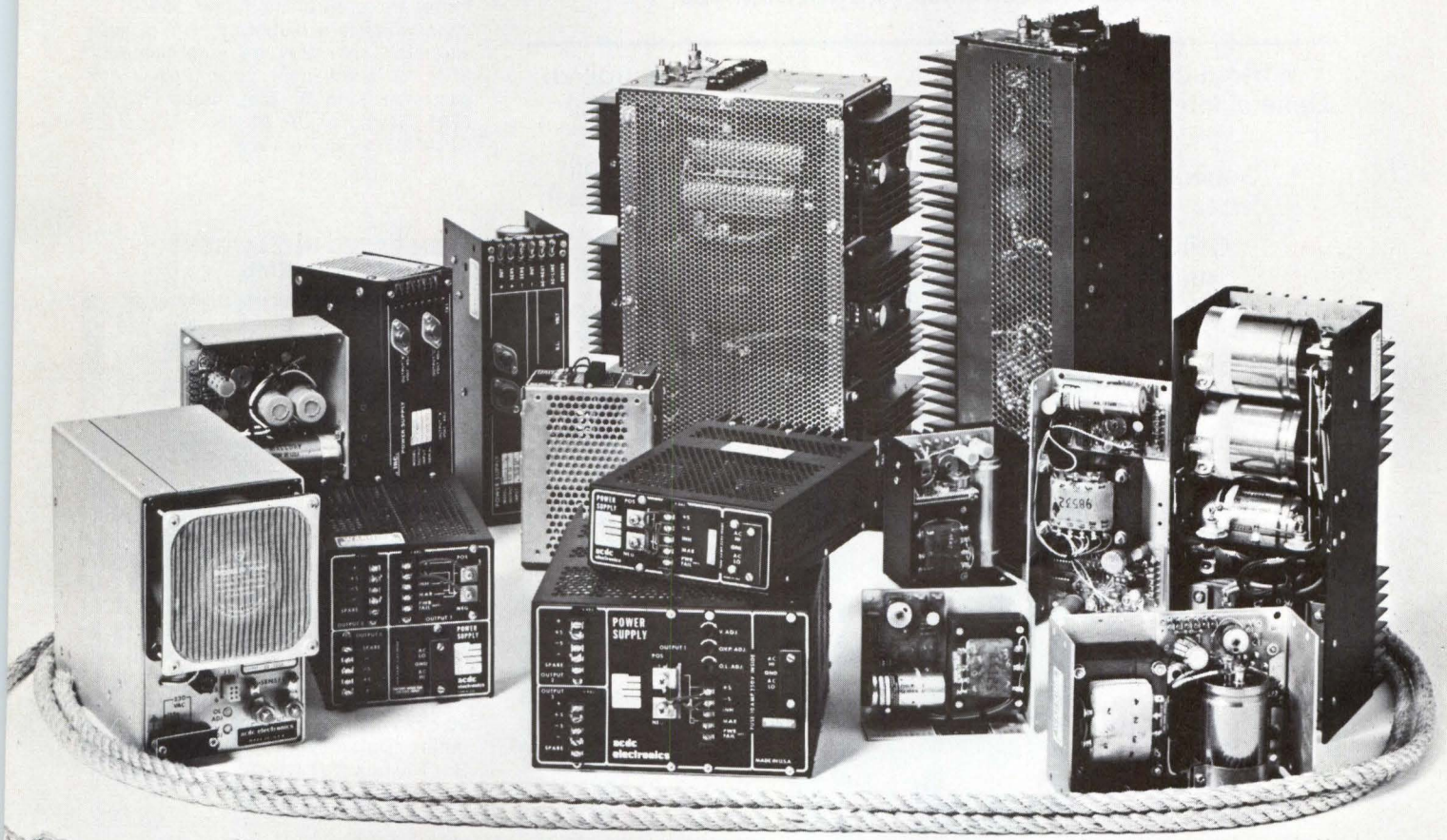


A 30-MHz unit that plugs into Tektronix TM-500 series power modules, the PI-210 is designed to operate with the company's -100A clock generator. This combination allows testing of high speed digital circuits and systems where the combination of digital word pattern and continuously adjustable pulse delay and width controls are required. The combined units can provide digital word pattern outputs with 3 independently adjustable pulse delay and RX width controls, all at bit rates up to 30 MHz. Number of word channels is expandable to a max of 16 in a given power module, in 4-channel increments. Other features include 2- to 32-bit variable word length, 128-bit max word length by cascading, serial or parallel data format, and 2-V min 50-Ω outputs to drive TTL and unterminated cables. **Pulse Instruments Co,** 1536 W 25th St, San Pedro, CA 90732.
Circle 215 on Inquiry Card

DC TO 5M-BYTE/s OPTICAL FIBER

Used in combination with appropriate optical fibers, modules can transmit digital data up to 1.5 km at rates from true dc or digital steady state to 5M bits/s NRZ, regardless of data format. Thus, arbitrarily long streams of 1s and 0s or bursts of data can be sent without dc drift problems common in fiber optic links. Electrical inputs and outputs are TTL compatible with amplitude-regenerated data supplied at the electrical output of the receiver. Additionally, special circuitry in the modules provides for min pulse distortion over a wide optical dynamic range. T-614 transmitter uses a high brightness LED, and T-615 receiver uses a low power PIN photodetector. An optical fiber pigtail 2-m long is provided for optical interface. **International Telephone and Telegraph Corp, Electro-Optical Products Div,** 7635 Plantation Rd, Roanoke, VA 24019.
Circle 216 on Inquiry Card

UL recognized power supplies Я us.



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CIRCLE 122 ON INQUIRY CARD

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Card equipment

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Multiple I/O board for two TTY and/or RS232 Controllers; other options include Real Time Clock and Modem Control

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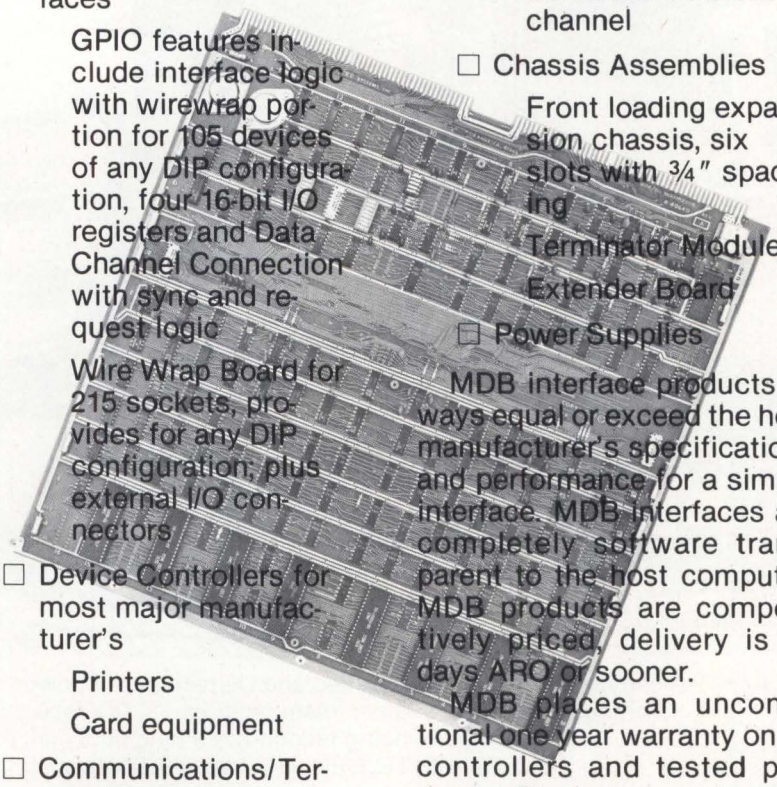
Front loading expansion chassis, six slots with ¾" spacing

Terminator Modules

Extender Board

☐ Power Supplies



MDB interface products always equal or exceed the host manufacturer's specifications and performance for a similar interface. MDB interfaces are completely software transparent to the host computer. MDB products are competitively priced, delivery is 14 days ARO or sooner.

MDB places an unconditional one year warranty on its controllers and tested products. Replacement boards are shipped by air within twenty-four hours of notification. Our service policy is exchange and return.

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*TMs Data General Corp & Digital Equipment Corp.

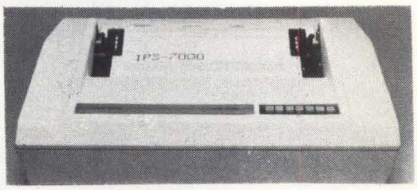
Circle 123 for DG; 124 for PDP; 125 for LSI; 126 for IBM; 127 for Interdata

PRODUCTS

COMMUNICATIONS TERMINAL BOARD

Single-board ESAT 200B standard interface terminal features EPROMs containing 2 fonts of up to 128 char each. One 2708 EPROM is supplied. Split speed serial data transmission and reception, RS-232-C, 20-mA loop, and TTL interface levels are included. Since fonts are programmed into 256 7 x 8 cells which are displayed contiguously, extended char may be programmed in 2 or more adjacent cells. Power consumption is 15 W. **Electrolabs,** PO Box 6721, Stanford, CA 94305.
Circle 217 on Inquiry Card

HIGH SPEED INTELLIGENT PRINTING SYSTEMS



A higher speed version of the IPS-7000™ comes with 3 firmware packages allowing 3 different printer configurations. Each version pairs 160-char/s serial interface matrix printer and 8-bit microcomputer with RAM and P/ROM. Systems available are: IPS-7201, 64 ASCII chars, 5 x 7 dot matrix, 500-char buffer; IPS-7208, 96-char set, 9 x 7 matrix, 500-char buffer; and IPS-7209 96-char set, 9 x 7 matrix, 3500-char buffer. **Dataroyal, Inc,** Main Dunstable Rd, Nashua, NH 03060.
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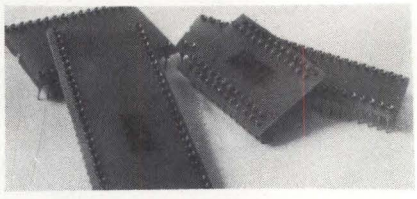
DUAL- AND QUAD-INLINE LSI SOCKETS



LSI socket series accepts LSI circuits with up to 64 pins on 0.900" (2.3-cm) spacing. 1-piece tapered entry socket terminal features a 4-leaf machined beryllium copper gold- over nickel-plated machined inner sleeve. Special design of lead socket sleeve permits sockets to double as carriers. Closed end contact construction eliminates solder or flux wicking. Sockets are designed to withstand high shock, vibration, and severe environments. **Augat, Inc,** 33 Perry Ave, Attleboro, MA 02703.
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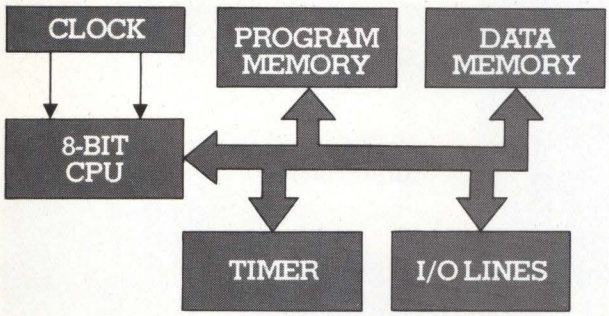
Introducing the first Intelligent keyboard.

It thinks like you do.



Designing a full-function keyboard for your system used to have a major problem. A full-function price.

MICRO SWITCH has changed all that with the intelligent keyboard. It's the first microcomputer-based keyboard. Ever.

Which means when you equip it with virtually every function you can think of, it still comes in for the price of a simple encoded keyboard. Because all the functions that used to require extra components are now available on a single microcomputer chip.

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MICRO SWITCH

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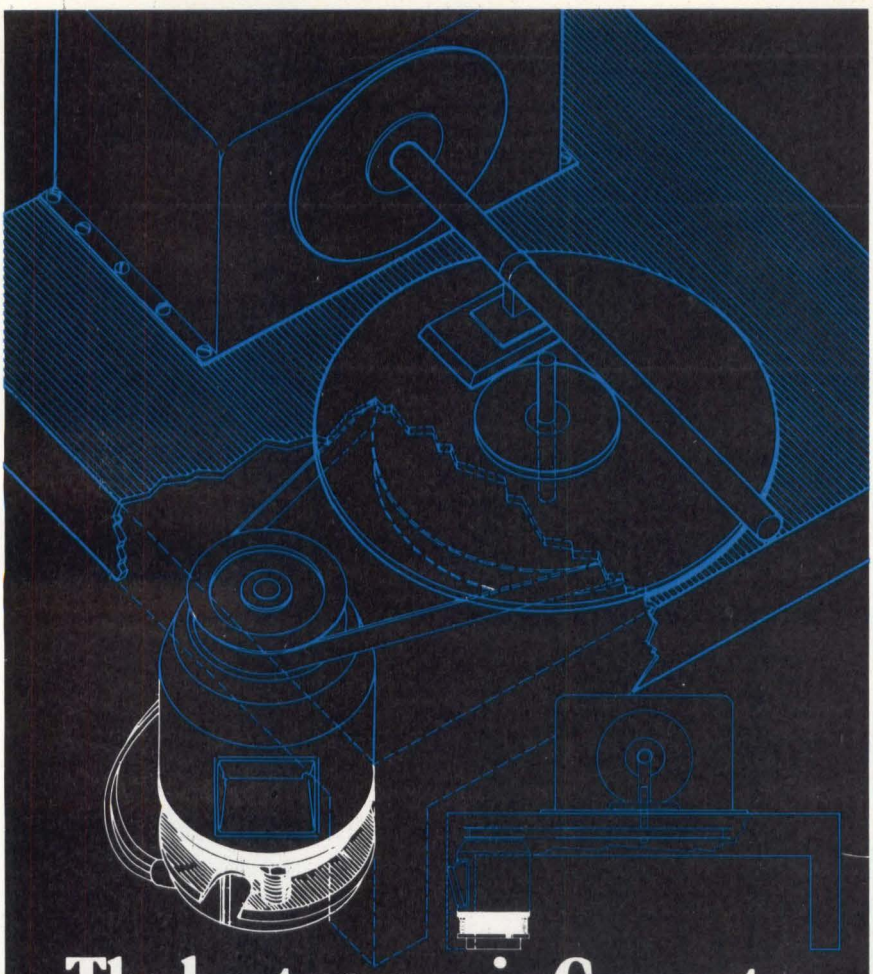
CIRCLE 128 FOR DATA.



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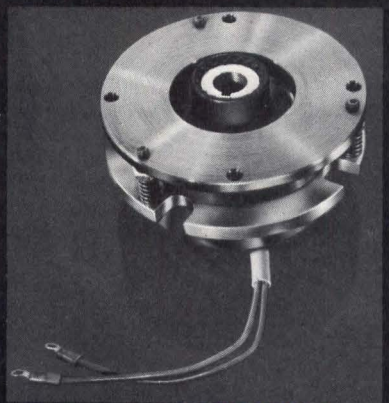
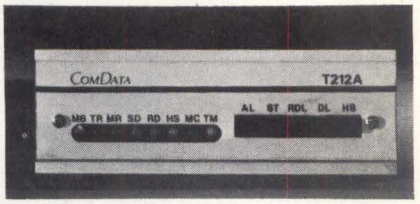


DANA INDUSTRIAL

Simplatrol Products, P.O. Box 870, Simplatrol DANA *Gore Road, RFD #1, Webster, Massachusetts 01570*

PRODUCTS

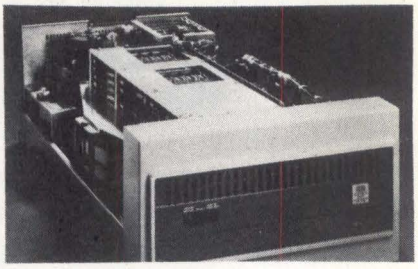
FULL-DUPLEX LOW/MEDIUM SPEED MODEM



Bell 113B and 212A compatible T212A provides full-duplex operation over public switched network in the low (0 to 300) and medium (1200) baud range. Available in standalone or rack-mountable models, std features include LSI circuitry, manual speed selection for originating modem, and automatic speed adjustment by answering modem. Four test switches plus diagnostic indicators allow for isolation of system malfunctions. **ComData Corp,** 8115 N Monticello, Skokie, IL 60076.

Circle 220 on Inquiry Card

80M-BYTE MODULE DISC DRIVE



Using fixed, sealed data modules, mini-module drive 9730-80 provides 80M bytes of data storage. Drives are data format and interface compatible with the 970 series of OEM storage module drives. A sealed data module containing the disc spindle, recording media, rotary actuator and data recording heads protects the recording environment from accuracy-affecting external contaminants. **Control Data Corp,** Box O, Minneapolis, MN 55440.

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Designed to support either Centronics or Dataproducts type printers, DEC® PDP-11® DLP 11 controller operates on any DEC PDP-11 computer without hardware modification. The unit comes with all necessary cabling and connectors to interface directly to the printer used. Self-test mode is provided to simplify installation and testing. Unit uses low power Schottky TTL logic, and requires 5 V at 1.1 A. **DataSystems Corp,** 8716 Production Ave, San Diego, CA 92101.

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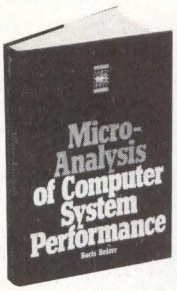
MICRO-ANALYSIS OF COMPUTER SYSTEM PERFORMANCE



By Boris Beizer

Here are proven techniques for analyzing system performance. Analytical methods—as contrasted with simulation—are featured, providing you with an easy-to-follow approach to the construction, validation and use of analytical models. Only expressions that can be programmed with relative ease are included. Mathematical prerequisites are minimal and formal derivations are used only when they serve to explain, illustrate or build intuition. This book will save you countless hours of experimentation and reinvention of analytical methods.

Gives you thoroughly tested procedures.

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VNR VAN NOSTRAND REINHOLD

PRODUCTS

SOLID-STATE COMPUTER KEYBOARD

Micro-proximity touch sensor technology and CMOS/LSI ICs are utilized in the flat keyboard, which is electronically and mechanically complete. Full ASCII coding is provided in a color-keyed layout for readability. Sensors are protected by a shield of polycarbonate for durability. Keyboard contains shift, shift lock, control functions, and normal tyepwriter format with 51 keys covering the 128-position ASCII code output. A plastic support stand is optional. **TASA, Inc,** 2346 Walsh Ave, Santa Clara, CA 95050.

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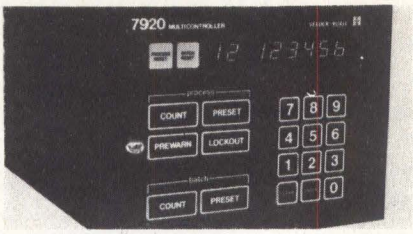
50-ROW BIDIRECTIONAL MULTICONTROLLER



Series 7920 microprocessor based predetermining counter has up to 50 preset numbers for automatic control of multiple-step machining and processing. Front panel keyboard enters preset numbers, and 6-decade LED display provides count and preset information. Second display shows preset row number. Input circuitry accepts pulses up to 10 kHz for unidirectional, and quadrature, add/subtract, or count/direction for bidirectional operation. Nonvolatile electronic memory retains all count, preset, and programming data. **Veeder-Root,** 70 Sargeant St, Hartford, CT 06102.

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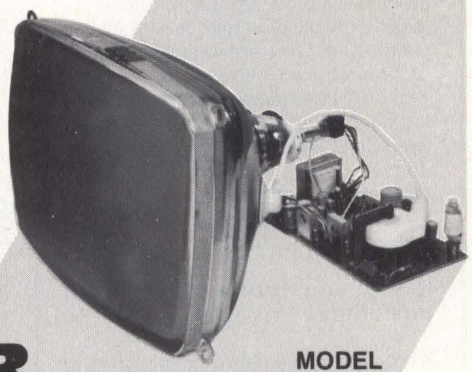
12" CRT DISPLAY MONITOR



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The low-cost CIQ-12 CRT Display Monitor provides data equipment manufacturers with sharp, highly reliable image presentation.

Separate horizontal drive, vertical drive, and video signal inputs mean elimination of composite sync and video signal processing and simple output circuitry.

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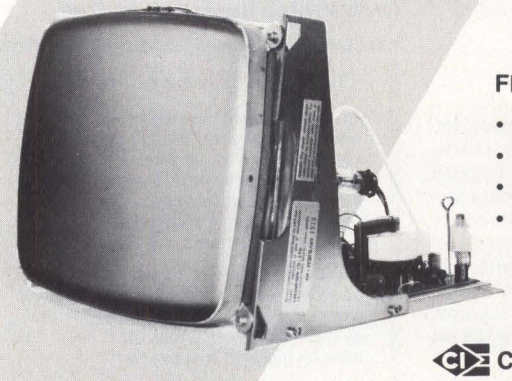
Delivered with P4 phosphor as standard. Available options are P31 and P39 phosphors, sturdy zinc chromate plated chassis and a power supply module which is compatible with practically any power supply standard in the world.



MODEL CIQ-12C (with optional chassis)

FEATURES

- Uniform High Resolution
- Integrated PC Board
- Dependable Construction
- Squareness of Picture

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Telephone: (213) 390-7778 Telex: (WU) 65-2451

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A hardware technique embodied in the emulator verifies against several types of fault classes, pinpoints defects in tests, and provides hardcopy documentation of the results. Faults emulated are a range of functions, such as monitoring activity at a node, emulating simple "stuck at" faults, and finding complex pseudorandom single-bit errors. Information is provided about the programming process to help the user evaluate the process. **Fluke Trendar Corp,** 630 Clyde Ave, Mountain View, CA 94043.

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DUAL CARTRIDGE DRIVE DATA SYSTEM

Desktop model 200 and rack-mountable model 200R using 3M DCD-1 data cartridge drives and 8080 microprocessor-based controller offer parallel output to external processor with bidirectional data lines and handshake capability. EIA std RS-232-C interface offers baud rates from 110 to 9600. Input data are double-buffered; average transfer rate is 2400 bytes/s, and typical data integrity is 1 in 10^{11} soft errors. **Hefte Industries,** 17465-A Shelburne Way, Los Gatos, CA 95030.

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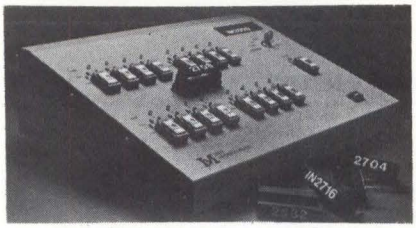
PRODUCTS

GANG P/ROM PROGRAMMER



Supporting 2704, 2708, 2768, 2716 (TI and Intel), and 2532 P/ROMs, IM2020 is intended for use in production environments and can program 16 P/ROMs simultaneously. No technical skill is required to operate the device. Various automatic operating modes are selected using a lockable switch. Operator prompting and programmer status are provided by a 10-digit alphanumeric display, 2 status LEDs per P/ROM socket, and an audible buzzer. A lighted pushbutton switch initiates all functions. **International Microsystems, Inc,** 11554 C Ave, Auburn, CA 95603.
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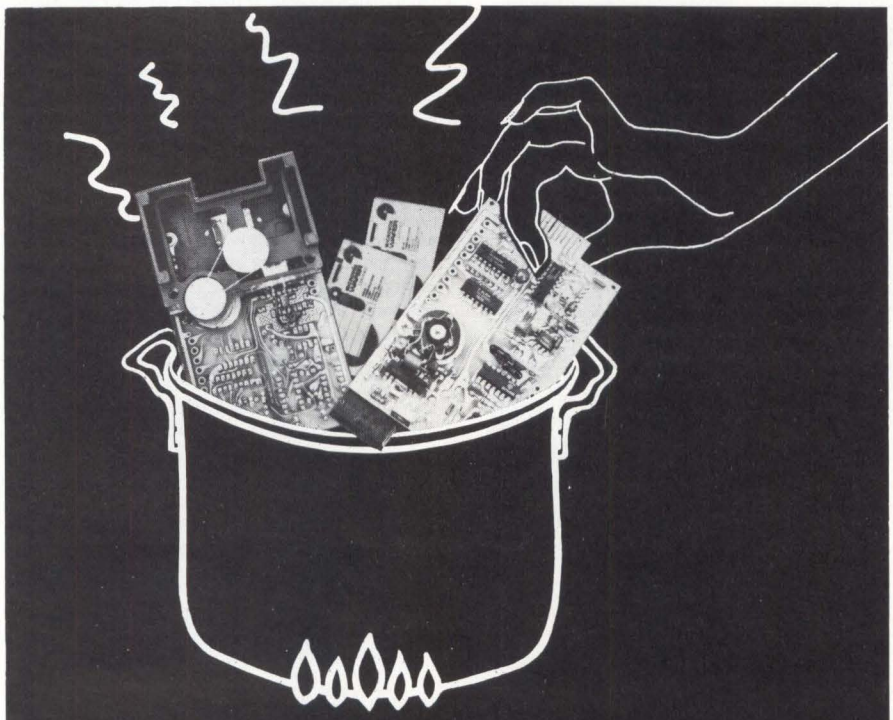

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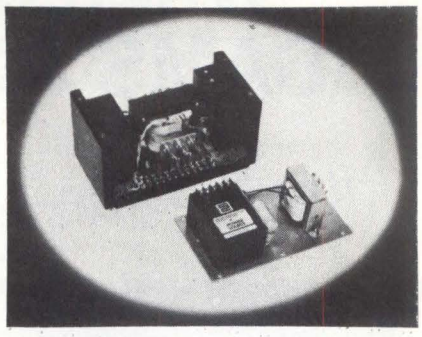
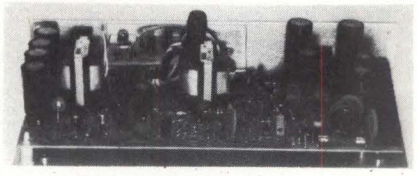
SINGLE- AND MULTIPLE-OUTPUT POWER SUPPLIES



Nine single-, dual-, and triple-output models added to the OE series, deliver up to 76 W at near-constant 60 to 70% efficiency. Single output model delivers 5 Vdc at 8 A. 2 dual-output units provide 5 Vdc at 3 or 6.5 A and 12 Vdc at 3.5 or 2 A. 6 triple output supplies offer 5, 12, and 12 Vdc at either 3, 1.5, and −1.5 A; 6.5, 1, and −1 A; or 8, 1, and −1 A; as well as 5, 15, and −15 Vdc at either 3, 1.5, and −1.5 A; 6.5, 1, and −1 A; or 8, 1, and −1 A, depending on model. User-connectable input ranges are 105 to 125 Vac or 210 to 250 Vac over 50- to 440-Hz range. **Semiconductor Circuits, Inc,** 306 River St, Haverhill, MA 01830.
Circle 228 on Inquiry Card

130-W SWITCHING POWER SUPPLY



Open-frame, quad output unit OL 130 operates at 60 to 70% power efficiency, weighs 2.5 lb (1.1 kg), and measures 10.5 x 5.0 x 2.5" (26.7 x 12.7 x 6.4 cm). Unit supplies 130 W of continuous power: 5 V at 15 A, −5 V at 2 A, 12 V at 4 A, and −12 V at 2 A. The 115-Vac unit operates at line voltages from 95 to 130 Vac, the 230-Vac unit from 196 to 260 Vac. Std features include input EMI filter, reverse voltage protection, series thermistor, and short circuit protection. **Boschert, Inc,** 384 Santa Trinita Ave, Sunnyvale, CA 94086.
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IBM COMPATIBLE DISKETTES

Compatible with IBM System/32, /34, Series 1, 5110, and OS-6 word processing systems, model 3740 formatted 8" (20.3-cm) diskettes are available in these versions: 1-sided/single-density (equivalent to IBM Diskette 1), 2-sided/single-density (IBM Diskette 2), and 2-sided/double-density (IBM Diskette 2D). The diskettes come in an easy-to-file container including a set of color coded identification labels. **Dysan Corp,** 2388 Walsh Ave, Santa Clara, CA 95050.
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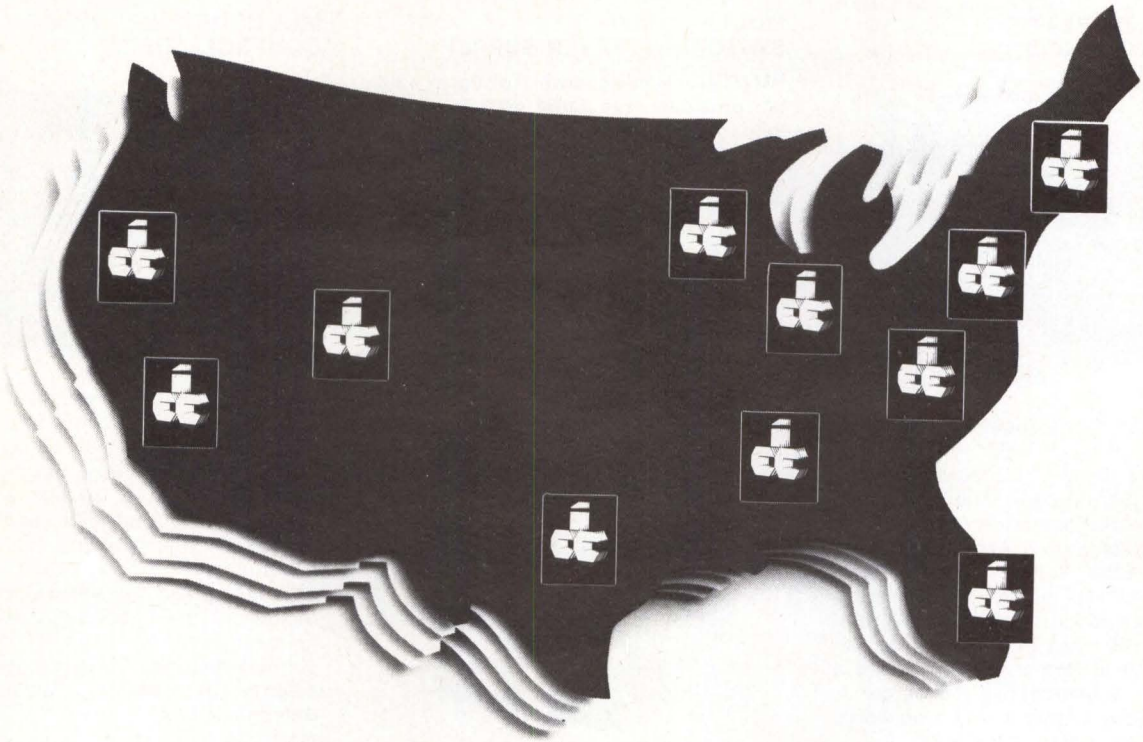
OEM America Meets



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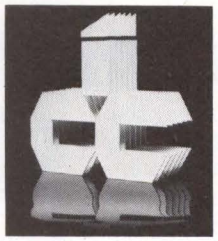
Feb. 8, 1979	Ft. Lauderdale, Fla.
Feb. 26, 1979	Atlanta, GA
Mar. 29, 1979	Dallas, Texas
April 17, 1979	Dayton, Ohio
April 19, 1979	Chicago, Ill.
May 8, 1979	Denver, Colo.

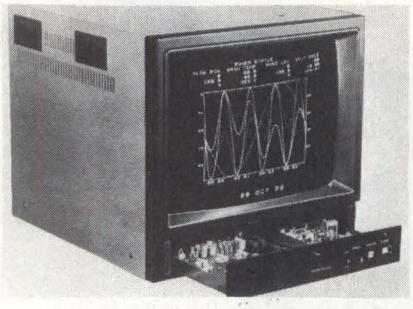


Invitational Computer Conferences

Invitations are available from participating companies or the ICC sponsor. For further information contact: B. J. Johnson & Associates, 2503 Eastbluff Drive, No. 203, Newport Beach, CA 92660. (714) 644-6037

CIRCLE 133 ON INQUIRY CARD

GRAPHIC DISPLAY COLOR MONITORS

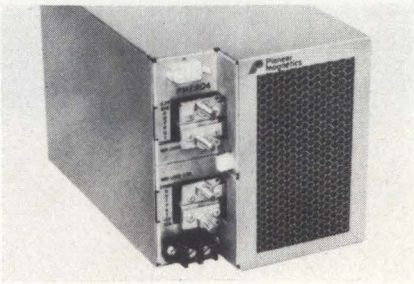


Model 8000 series feature displayable resolution of up to 1024 elements or 1024 raster lines. 13″ (33-cm) model 8024 and 19″ (48-cm) model 8025 have a 15-MHz video bandwidth and a 15- to 18-kHz horizontal frequency. Model 8026 has a 25-MHz video bandwidth and 28.3- to 34.6-kHz horizontal frequency, and displays video images of 1024 elements by 512 lines in a flicker-free 60-Hz repeat field format. All units have a sectorized noninteractive convergence system. **Aydin Controls,** 414 Commerce Dr, Fort Washington, PA 19034.

Circle 231 on Inquiry Card

MULTIPLE-OUTPUT SWITCHING POWER SUPPLY

PM2804 has power levels of up to 1350 W, providing regulated output at full load over input voltage ranges of 184 to 250 Vac. Extreme brownout protection allows it to operate for several minutes at inputs as low as 140 Vac. During complete failure, output voltage lasts for min of 30 ms for system shutdown. Output channels have max power ratings of 750, 600, and 300 W. Std output voltage channels are available from 2 to 48 V. Package with self-contained cooling measures 8 x 8.125 x 13.75″ (20.5 x 20.6 x 34.9 cm). **Pioneer Magnetics, Inc,** 1745 Berkeley St, Santa Monica, CA 90404.



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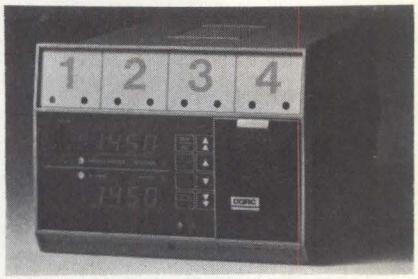
MULTIPLE LOOP INDUSTRIAL CONTROLLERS



Control:80 models, available in 2- and 4-loop configurations, feature input, output, and control action selection on a per-loop basis. Field interchangeable inputs include all common thermocouple types, millivolts, and process inputs. Plug-in outputs include relays and triacs rated at 2 A, 240 V, as well as voltage and current outputs. Capabilities of the microprocessor based units include 1 °F or °C accuracy, alarm monitoring package and integral setpoint programming package. **Doric Scientific,** 3883 Ruffin Rd, San Diego, CA 92123.

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INTERNATIONAL DATA SCIENCES, INC.

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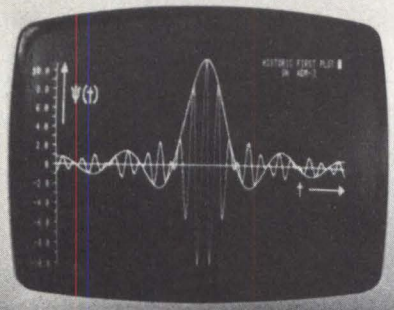

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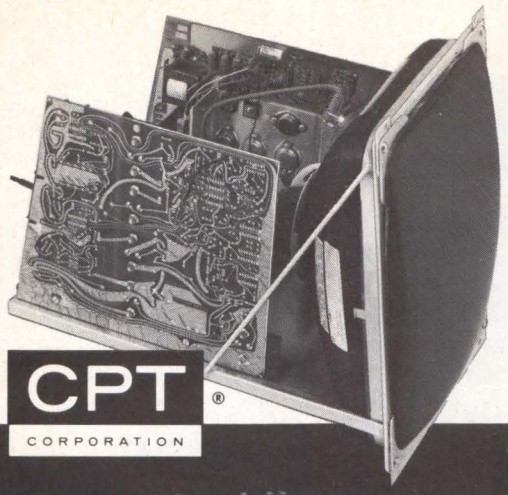
CIRCLE 163 ON INQUIRY CARD →



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This is an un-retouched photo of the new CPT HRD-15 Model S, black-on-white high resolution, high density raster display. As a result of faster scanning speeds and faster rise/fall rates, it gives you this unique clarity and high density. The "smear" at the edge of the dot is eliminated. The dot has more edge contrast, better definition. Developed to look as much as possible like the typewritten page, the CPT HRD-15 is human engineered for daily use without eyestrain.

For this photo, the non-interlaced system scans at 50,000 scan lines per second, refreshing the entire image at 60 times per second. Dot resolution is rated at .01 inch with clear definition, since rise/fall time is less than 3 nanoseconds. The phosphor is P-4, with others available on request.

Designed for text processing, the HRD-15 uses a 15" CRT to display up to 64 lines of text, 96 characters to the line and at a lower cost per character than ordinary display tubes. Other applications include graphics, typesetting, and data terminal users.

This monitor component is offered with an attractive OEM schedule, and is available within 30 days of receipt of order. Choose from two models:

	Model S	Model H
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Visible Lines	800	1024
Rise/Fall rate less than	3 nanoseconds	2 nanoseconds

With more than 12,000 word processing systems in use, CPT has proved itself an established and reliable leader in the field. CPT products are sold and serviced in over 100 U.S. cities and 30 countries around the world.

For more information or a demonstration on the new HRD-15, write: CPT Corporation, 1001 Second Street South, Hopkins, MN 55343. Or phone: (612)935-0381

PRODUCTS

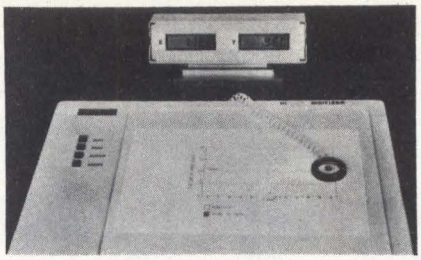
P/ROM-ROM MEMORY MODULE

Selectable access time delay permits model PM-116 DataRom to accept erasable and fusible-link P/ROMs and masked ROMs in all current 24-pin std and proposed formats from 1k x 8 to 8k x 8 bits. Module provides up to 128k-bytes P/ROM-ROM storage for Intel SBC/NSC BLC single board computers. It has individually switch-enabled sockets for 16 24-pin DIPs. Data are selected by a 16-bit address and are presented on the bus as 8- or 16-bit words. 20-bit address and −5-V regulator are optional. **Datacube SMK, Inc,** 670 Main St, Reading, MA 01867.
Circle 234 on Inquiry Card

STATISTICAL MULTIPLEXER

Increased throughput, error protection, downline loading, and built-in diagnostics are incorporated in the microprocessor controlled Supermux 480. One telephone line transmits data previously carried by up to 8 links. Units use statistical techniques to transmit only active data inputs, which may be dial-up or dedicated at mixed speeds up to 9600 bits/s asynchronous. Transmission errors also are eliminated. **Infotron Systems Corp,** Cherry Hill Industrial Ctr, Cherry Hill, NJ 08003.
Circle 235 on Inquiry Card

INTELLIGENT ACTIVE SURFACE DIGITIZER



HI PAD is an 11 x 11" (28 x 28 cm) digitizer offering such user controllable features as metric/inch capability, binary/BCD outputs, and RS-232-C/8-bit parallel interface, all selectable at interface connector. It is accurate to ±0.015" (0.38 mm) with resolution of 0.005" (0.13 mm). Data rate may be set to input up to 100 coordinate pairs/s. Edge-mounted buttons allow user to relocate origin and select point or stream modes of operation. **Houston Instrument,** One Houston Square, Austin, TX 78753.
Circle 236 on Inquiry Card

ASYNCHRONOUS-SYNCHRONOUS CONVERTER FOR MODEMS

Model ASI-192 interface allows asynchronous devices to transmit data through synchronous modems in polled or switched networks, or in dedicated line environments, at speeds of up to 19.2k bits/s. It supports modems operating at 2400 bits/s on unconditioned 3002 communications lines, 4800- and 9600-bit/s modems, and SRM-192 short-range modems operating at 19.2k bits/s. Device converts serial asynchronous words to parallel words, stores them, and sends the data serially. **Paradyne Corp,** 8550 Ulmerton Rd, Largo, FL 33541.
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25-W SWITCHING POWER SUPPLY

The totally encapsulated 2.5 x 4 x 1.25" (6.4 x 10 x 3.2-cm) SR1.5.5 is easily mounted directly on a PCB. Unit features 80% min efficiency, regulation of ±0.1% for 0 to 100% load and ±10% line, 50-mV pk-pk max (30-MHz bandwidth) ripple, with 115-Vac ±10%, 50- to 400-Hz input voltage, and 5-V at 5-A output. Cased in metal for RFI shielding and optimum thermal design, switcher is protected against output short circuits and features an overvoltage crowbar. **Calex Mfg Co, Inc,** 3355 Vincent Rd, Pleasant Hill, CA 94523.
Circle 238 on Inquiry Card

MICROPROCESSOR-BASED IEEE 488 BUS ADAPTOR

DBA-488 controls transmission of data, timing, and control signals between instruments and other data handling devices and IEEE 488 general-purpose interface bus. It stores interfacing information as firmware in plug-in ROM, which can be custom programmed for linking almost any device to the bus without hardwiring changes. Adapter is self-contained and requires standard line voltage. Externally accessible rocker switches change bus address. Dimensions are 8.1 x 6.1 x 1.7" (20.6 x 15.5 x 4.3 cm). **ILC Data Device Corp,** Airport International Plaza, Bohemia, NY 11716.
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Looking for Static Memory? Look to Econoram™.

Econoram static memory products are now available for the S-100, Heath H8, Intel/National 80/10 and 80/20, and Digital Group busses. We also offer a memory expansion kit for the Radio Shack TRS-80 and APPLE computers.

Most Econoram products are available in 3 forms: "unkit" (sockets and bypass capacitors pre-soldered in place for easy assembly), assembled and tested, or qualified under the Certified System Components program. CSC boards are assembled, burned in for 200 hours, serial numbered, and guaranteed to run at 4 MHz over the full commercial temperature range. Additionally, we back up all of our products with a 1 year (not 90 day) limited warranty.

Our design philosophy is simple: Maximum reliability, coupled with minimum cost and liberal inclusion of user-oriented features. If this sounds like what you're looking for in memory, contact us for more information.

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CompuKit™ from GODBOUT
BILL GODBOUT ELECTRONICS
BOX 2355, OAKLAND AIRPORT, CA 94614

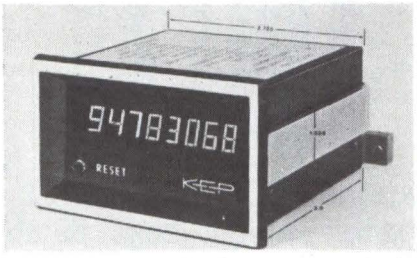
COMMUNICATIONS-TYPE UNIVERSAL COUNTER

With a multistage pin diode attenuated agc high frequency input channel, PM 6616 optimizes triggering on rf signals up to 1.3 GHz, and on If signals up to 80 MHz. Rated at 10-mV sensitivity, it offers overload protection and noise immunity. Period, period-average, multiple ratio, count, and frequency measurements can be performed. Max rf input voltage on input B is 12 V rms. Packaged in an optional carrying case, the unit weighs 9.2 lb (4.2 kg). **Philips Test & Measuring Instruments,** 85 McKee Dr, Mahwah, NJ 07430.
Circle 240 on Inquiry Card

TIMESHARE SMALL COMPUTER SYSTEM

Model 5000 provides 29M bytes of disc storage, 1 cartridge drive, and 8 user ports in its basic configuration. Disc storage may be expanded in 29M-byte increments to 58M, 87M, or 116M bytes. Addition of up to eight 49M-byte removable pack drives expands storage to 392M bytes. The mag tape cartridge module may be expanded to 2, 3, or 4 drives, and user port capacity can be expanded to 16, 24, or 32 ports. **BTI Computer Systems,** 870 W Maude Ave, Sunnyvale, CA 94986.
Circle 241 on Inquiry Card

8-DIGIT COUNTER/TIMER



Modular plug-in function cards of 8000 series are inserted to permit direct counting with switch closures and ac or dc pulses. Cards are DIP switch field programmable; they also convert the unit from a counter to a programmable timer/rate meter/digital tachometer. All versions have BCD and/or 0 output. Orange high efficiency LED displays are available with 8 digits, 0.330" (0.838 cm) high, or 6 digits, 0.430" (1.09 cm) high. Power supply is 110/220 V, 50/60 Hz. **Kessler-Ellis Products Co,** Atlantic Highlands, NJ 07716.
Circle 242 on Inquiry Card

QPSK MODEMS FOR SATELLITE COMMUNICATION

Series 1463 single channel per carrier modems are designed specifically for satellite communications networks where transponder is power-limited because of a large number of single channels. Consisting of 1463T encoder/modulator and 1463R demodulator/decoder units, they are of all solid-state IC design, and include error-correcting encoding and decoding. Standard interfaces available are V.35, WE302 and RS-232-C (or V.24). **American Modem Corp,** 160 Wilbur Place, Bohemia, NY 11716.
Circle 243 on Inquiry Card

VERTICALLY SUPPORTED PC SLIDE SWITCH

Subminiature spdt slide switches have V3 or V4 electrotin-plated vertical support brackets to help absorb actuation shock and relieve excessive terminal stress. Bracket heights are 0.350" (8.9 mm) and 0.525" (13.3 mm) above the PC board. Contact material is gold over brass, with contact rating of 0.4 VA max; 20 V or 1 A max. Mechanical life is 250k low energy actuations, with an initial actuator force of 150 to 350 g. **C & K Components, Inc,** 103 Morse St, Watertown, MA 02172.
Circle 244 on Inquiry Card

Give your PDP-11 a Calendar.

When you equip your computer with a TCU-100, you'll automatically have the date and time available when you power up.

It's an easy way to keep track of downtime, too. Furthermore, you can use the unit like an alarm clock. Set it to interrupt at preset times—or at intervals as short as 1/2048 second.

TCUs are shipped preset to your local time, but can be set to any time you want by a simple software routine. The built-in battery back-up is good for months with out computer power.

For the *LSI-11 user,* we offer the TCU-50 — the same reliable timekeeper without the interrupt capability. With either unit, time is cheap. The TCU-100 is just $495. And the TCU-50 is only $325.

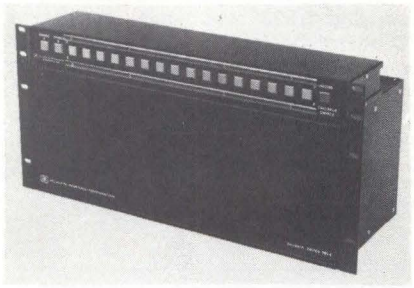
Time is only one way we can help you upgrade your PDP-11 or LSI-11 system. We'd also like to tell you about the others.

So contact Digital Pathways if you're into -11's. *We are too.*

DIGITAL PATHWAYS INC.
4151 Middlefield Road • Palo Alto, California 94306 • Telephone (415) 493-5544

PRODUCTS

FALLBACK SWITCH SYSTEM



FBS-1 switches up to 16 RS-232/V.24 interfaces between active and fallback or alternate positions using magnetic latching relays to prevent power-loss scattering. Remote control unit RP-2-1 provides control, and contains switches and indicator lights for individual circuit or master switching. Up to 16 FBM-1-1 fallback switch modules and a control/power supply module are housed in a DMA-4-52 mounting assembly. Std cable lengths of 10, 25, and 50′ (3, 7.5, and 15 m) are available. **Atlantic Research Corp,** 5390 Cherokee Ave, Alexandria, VA 22314.
Circle 245 on Inquiry Card

15-W WIDE INPUT DC-DC CONVERTER

Triple-output CS series dc-dc supply handles input range of 7 to 40 Vdc (12 Vdc nom) and provides outputs of ±12 or ±15 Vdc at ±165 mA, and 5 Vdc at 2 A. Efficiency of 70% at 12-V input is maintained virtually flat, falling to 69% at 40-Vdc input. Output accuracy at full load is ±0.7% dual, ±1.0% max. Tempco (dual) is ±0.01%/°C max and single is ±0.02%/°C max. Voltage stability is ±0.05%/24 h. Supply is housed in electrically isolated 3.2 x 7 x 0.83″ (8.1 x 17.8 x 2.1-cm) metal case with 7 I/O solder turret terminals. **Stevens-Arnold, Inc,** 7 Elkins St, South Boston, MA 02127.
Circle 246 on Inquiry Card

MONOCHROME DATA MONITORS

M15 series high resolution, raster scan unit features 73 lines/in (29/cm) vertical and 97 elements/in (38/cm) horizontal. Vertical mounting configuration has 800 x 800 elements, horizontal format has 1067 x 600 elements. Picture steady, nonflickering white display has 60-Hz refresh rate, P4 phosphor, and no interlace display. Also included are std TTL data and sync outputs; 0, 5, or 7.5° of screen tilt; and dc or ac power options. **Video Monitors, Inc,** 2533 A2 Bernice Rd, Lansing, IL 60438.
Circle 247 on Inquiry Card

8″ OEM DISC

8″ (20.3-cm) disc for the OEM market is designed for use with drives employing fixed media. It has packing densities of up to 7k bits/in (2756/cm) and 600 tracks/in (236/cm), or approximately 23M 8-bit bytes/in (9M/cm). Operating speed is up to 6k r/min. Disc inner dia is 2.5″ (63.5 mm); outer radius measures 3.9″ (100 mm). 75-mil thick aluminum substrate is coated with a magnetically oriented iron oxide dispersion. **BASF Systems, Computer Products,** Crosby Dr, Bedford, MA 01730.
Circle 248 on Inquiry Card

HOMOGENEOUS DATA BUS OPTICAL COUPLER

Model O-OCS-9-10110 interconnects various sources and receivers in fiber optic systems. By averaging total energy among all given ports it is said to minimize total dB loss and maximize overall energy transmission. It has total input to any output insertion loss of 13.8 dB, comprising an optical loss of 4.3 dB and an intrinsic light division loss of 9.5 dB. Two different types are available: one providing separate input and output ports with isolation between ports, the other with duplex ports—any port can serve as an input or output. **Olektron Corp,** 61 Sutton Rd, Webster, MA 01570.
Circle 249 on Inquiry Card

3SX-11

Another Breakthrough

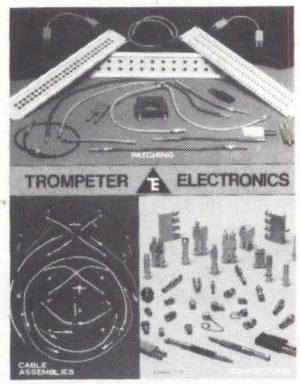
To meet the needs of LSI-11 users, 3SX-11 is a real-time executive which allows you to quickly and efficiently develop applications. No need to develop your own optimized software executive.

As computer application experts in the real-time industrial field, we develop complete application packages, or, customize any software enhancements you may require.

Scientific Systems Services, Inc.
Bob Chudoba
P.O. Box 610, Melbourne, Florida 32901
Phone: 305/725–1300

NEW ELEMENTS OF COST SAVINGS IN INDUSTRY, THROUGH ADVANCED COMPUTER TECHNOLOGY

NEW FREE CATALOG



TROMPETER ELECTRONICS has just published a new 40 page catalog T11, illustrating a complete line of coax, twinax, triax and quadrax connectors, patch panels, plugs, jacks, patch cords, cable assemblies, networks and accessories. The catalog includes an eight page technical discussion of noise in cable systems.

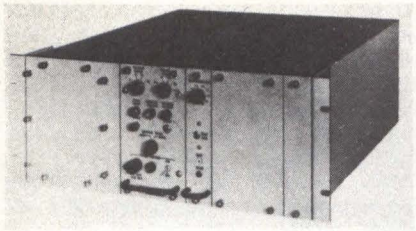
SEND FOR YOUR FREE COPY TODAY.

TROMPETER ELECTRONICS, INC.
8936 Comanche Avenue, Chatsworth, CA. 91311
(213) 882-1020/TWX: 910-494-1210

CIRCLE 137 ON INQUIRY CARD

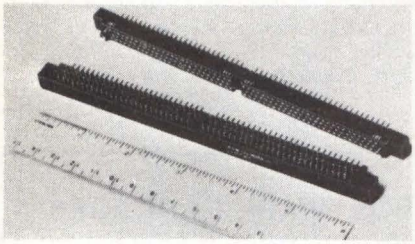
CIRCLE 150 ON INQUIRY CARD

HIGH SPEED CRYPTO ANCILLARY UNIT



Series 3000 CAUs are designed for use with either KG-13 or KG-30 crypto units, and provide red/black interface between terminals and modems plus all interface and synchronization capability for KG-type crypto devices. Operation is also compatible with distant terminal sites which use SN-394 crypto adapter when operating with the KG-13. Full-duplex synchronous data terminals are accommodated at speeds up to 64k bits/s and asynchronous up to 1200 bits/s. **Dataproducts New England, Inc,** Barnes Park N, Wallingford, CT 06492.
Circle 250 on Inquiry Card

LOW FORCE MIL-SPEC CONNECTORS



Hypertac multi-layer board connectors use pin and socket type contacts. Designed for field use necessitating multiple insertions and extractions, the 90-pin connector demates with a force of 8 lb (3.6 kg), the 120-pin unit with 12 lb (5.4 kg), and the 160-pin unit with 15 lb (6.75 kg). Tests reveal no deterioration in connector performance after 100k mating and demating cycles. Hypertac connectors are equivalent to the specs of Mil-C-55302. **Industrial Electronics Hardware Corp,** 5423 Smooth Meadow, Columbia, MD 21044.
Circle 251 on Inquiry Card

SIP AND DIP RC NETWORKS

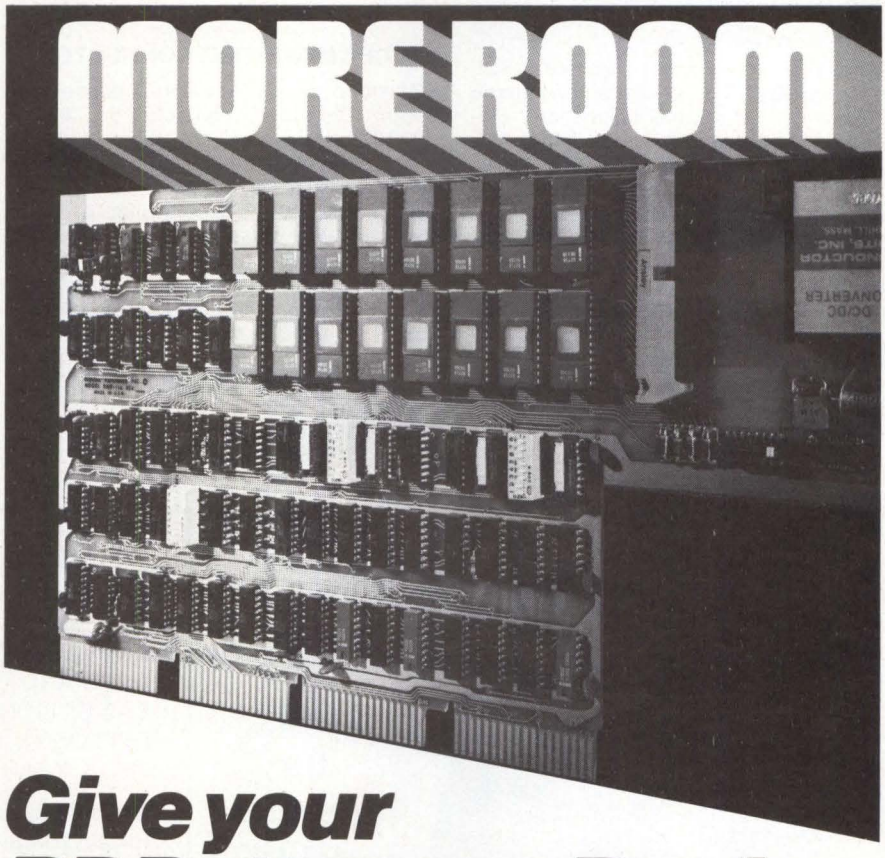
Networks are available in either single- or dual-inline packages for use with std ICs. Thick film resistors are protected with a glaze coating. Specs include compactness of 10-mil lines and 10-mil spaces, circuit isolation with substrate resistivity of 10^{14} Ω-cm at 25 °C, 490-V/mil dielectric rating, and high breakdown voltages according to MIL-STD-702, Method 301. Devices have flame retardant (UL VE-O) epoxy coating. **International Sensor Systems, Inc,** PO Box 345, Aurora, NE 68818.
Circle 252 on Inquiry Card

CARTRIDGE DISC CONTROLLER

Based on the X2 microprocessor, Quad™ is the width of 4 boards and is used with DEC PDP-11® minicomputers and LSI-11® microcomputers; it is RK-11 plug compatible and software transparent, and RK-05 media compatible to provide emulation of the DEC RK-11 system. The board is available as controller only, single-drive system, or multiple-drive system with various industry std cartridge disc drives of 5M-, 10M-, or 20M-byte capacity. **Xebec Systems Inc,** 2985 Kifer Rd, Santa Clara, CA 95051.
Circle 253 on Inquiry Card

ABSOLUTE WHOLE WORD ENCODER

Digisec® model RA/35C offers 17-bit resolution in a 3.5" (8.9-cm) self-contained package. Providing resolutions to 9.9 arc-s, it has a natural binary code with parallel or serial readout. Operating speed is 90 r/min, max slew speed 1000 r/min. Fully MIL-Spec rated unit is designed to operate in temp range from −40 to 70 °C. Base construction is stainless steel and weight is 4.5 lb (2 kg). **Itek Corp, Measurement Systems Div,** 27 Christina St, Newton, MA 02161.
Circle 254 on Inquiry Card



Give your PDP-11 some Bank-Switched ROM.

It will be the best investment you ever made. ROM means rapid access and permanent storage.

One board gives you 16k of ROM or EPROM (using Intel 2716's). You can add as many boards as you like, using manual or program control to enable the memory in banks as small as 4k.

You can program the EPROM's in place on your PDP-11 or use the handy remote programmer. Either way, you'll stretch your system capacity with no fuss — and at very low cost. Only $895. And the remote programmer is just $250. In case you don't need bank switching, we have a 24k ROM system with conventional addressing for $450.

By the way, you can get equivalent capability for the LSI-11.

So contact Digital Pathways if you're into -11's. *We are too.*

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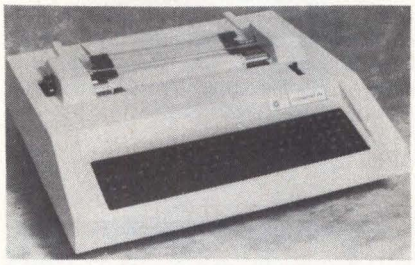
CIRCLE 138 ON INQUIRY CARD

PRODUCTS

100-CHAR/s KSR PRINTING TERMINAL



Datewriter III transmits 128 std ASCII char codes from 80-key alphanumeric keyboard with numeric/function keypad. 95 u/lc ASCII chars plus APL char set are printed in a 7 x 7 dot matrix at 13.6 char/in (5.3/cm) using impact technology. Up to 136 single width chars/line printed at 6 or 8 lines/in (2.4 or 3.1/cm) vertical, allows up to 68 lines of 136 chars on 11 x 8.5" (27.9 x 21.6 cm) paper. Transmission is at std rates from 110 to 9600 baud over RS-232 or current loop interfaces. **Datagroup, Inc,** 811 S 500 W St, Bountiful, UT 84010.
Circle 255 on Inquiry Card

HIGH TORQUE REVERSIBLE SYNCHRONOUS MOTOR

Series 81900 permanent magnet electrically reversible synchronous motor, measuring 2.75" (7 cm) dia and 1.687" (4.3 cm) depth provides 21 oz-in (0.15 N•m) synchronous torque for a high torque-to-frame size ratio. Power input is 17 W. Motor can be furnished for 120- or 24-V, 60-Hz operation. Output speed is 300 r/min. It is furnished with a 2.75" (7-cm) square mounting plate. Choice of permanently lubricated porous bronze or roller bearings is offered. **North American Philips Controls Corp,** Cheshire Industrial Pk, Cheshire, CT 06410.
Circle 256 on Inquiry Card

MICROMINIATURE CONNECTOR

Shielded metal Dura-Con-D connectors, with Dura-Con contacts on 0.050" (0.127-cm) centers, are suited for harsh environmental applications. Male contact consists of 7 wires, twisted into miniature helical spring pin; it is recessed in a glass-filled polyester insulator to prevent misalignment. Corrosion resistant cast aluminum alloy shell provides emi shielding of 40 dB min from dc to 1000 MHz. Contact sizes are 9, 15, 21, 25, 31, 37, and 51. **TRW Cinch Connectors,** 1501 Morse Ave, Elk Grove Village, IL 60007.
Circle 257 on Inquiry Card

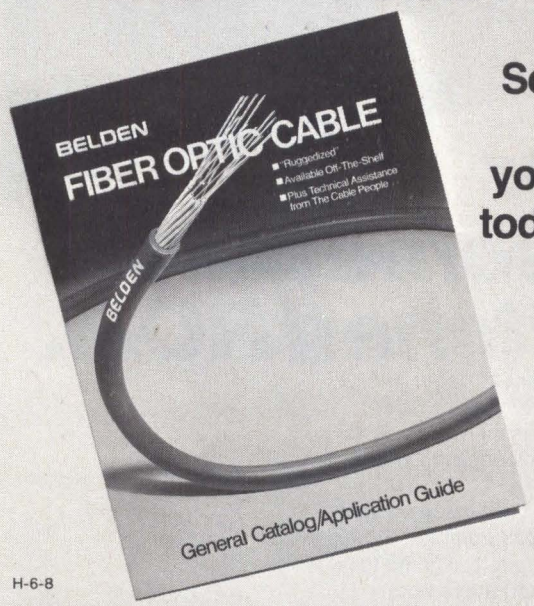
FORTRAN SOFTWARE PACKAGES

A simulation package and reliability analysis program—SIMTRAN and RAP—are FORTRAN products, supplied in source code form. The first has simulation oriented statements for developing models of systems of various complexity. Simulations are performed in FORTRAN. The latter features system modeling equations to develop reliability analysis models. Results are given in terms of MTBF, MTTR, and overall system availability. **Sysmetrics,** 6545 Balsam N, Osseo, MN 55369.
Circle 258 on Inquiry Card

LSI DATA SET

FCC registered modem is a single modular solid-state data set to transmit and receive full-duplex asynchronous serial data at rates up to 300 bits/s in either originate or answer mode over 2-wire DDD network. LED lamps monitor EIA RS-232-C digital interface leads and status of data modem in various test modes. Self-test word generator and comparator, and analog and digital loopback are incorporated in 103J family. It is compatible with Bell 103 and 113 data modems, and 801A and 801C automatic calling units. **Rixon, Inc,** 2120 Industrial Pkwy, Silver Spring, MD 20904.
Circle 259 on Inquiry Card

FIBER OPTIC CABLE CATALOG



Send for yours today!

H-6-8

Belden Corporation, Fiber Optics Group,
2000 S. Batavia Ave, Geneva, IL 60134 Phone: 312-232-8900.

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with new ideas for moving electrical energy

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COMPUTER SOFTWARE PACKAGES AND PACKAGED SERVICES MARKETS

ANNUAL EXPENDITURES FOR SOFTWARE PACKAGES AND PACKAGED SERVICES NOW EXCEED $1.2 BILLION A YEAR AND ARE GROWING AT AN EXPLOSIVE AVERAGE ANNUAL RATE OF ABOUT 25% A YEAR.

Frost & Sullivan has completed a 170-page report (plus 55 pages of Appendices) analyzing and forecasting the computer software packages and packaged computer services market. The primary input to the study are two highly detailed questionnaire surveys sent to users and suppliers. Two other reports published on the same subject by Frost & Sullivan in 1973 and 1975 serve as benchmarks, with comparisons of findings in the three reports indicating changes in thinking by those who use the product and those who market. In the report software packages and package services are grouped into eight categories with ten-year sales forecasts furnished for each type.

Price $700. Send your check or we will bill you. For free descriptive literature plus a detailed Table of Contents contact:

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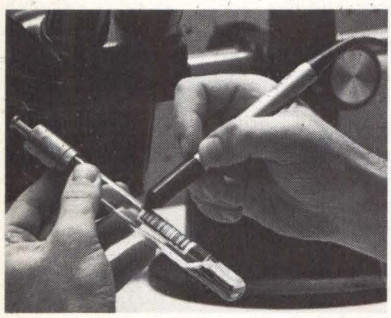
For Fast, Accurate Data Entry.



ABCD+1234

Bar code gives you virtually error free input, confirmed by an audible read signal.

Unskilled factory workers achieve data entry rates of several hundred characters per second with virtually no training.

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Inventory Control
Wholesale Distribution
Hospital Records Systems
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Intermec bar code printers and readers are microprocessor based for system flexibility and compatibility.

- Multiple Bar Codes
- User Selectable Protocol
- Readers with Dual I/O Connectors
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- RS232C • ASCII

Intermec manufactures a complete line of bar code printers and readers which have become standards of the industry.

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P.O. Box "N," Lynnwood, WA
98036, Phone (206) 743-7036,
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READERS PRINTERS WANDS

PRODUCTS

UNINTERRUPTIBLE POWER SYSTEMS

UPS regulates and conditions incoming power to protect such devices as computers, peripherals, and communication equipment. Continuous power is provided during power fluctuations, transients, short circuits, unstable environmental conditions, brownouts, and blackouts. The solid-state system consists of an input transformer, rectifier/charger, dc bus, inverter, filters, static switch, and battery. Std 60-Hz models are available with ratings of 1 to 15 kVA. **Power Dynamics Corp,** 422 Park Ave, San Fernando, CA 91340.
Circle 260 on Inquiry Card

INSULATION DISPLACEMENT CONNECTORS

Jaguar 156 assembles with ease and speed to ribbon cable and discrete wire, complete with strain relief. Connectors are interchangeable with existing crimp and stuff connectors. On 0.156" (0.396-cm) center spacings, the connectors mate with 0.045" (0.114-cm) round or square pins. Both locking and nonlocking styles are available with from 2 to 24 circuits. Brass tin plated contacts are std; gold plating is optional. **Methode Electronics, Inc, Interconnect Products Div,** 1700 Hicks Rd, Rolling Meadows, IL 60008.
Circle 261 on Inquiry Card

VIRTUAL MEMORY SYSTEM

Base configuration of the VM-10 offers 64k bytes of semiconductor memory, with 1000-ns CPU, top loading 10M-byte disc drive, 8-channel multiplexer, realtime clock, cartridge mag tape, 300-line/min impact printer with insulated cabinet, and 24-line CRT with extended keyboard. It uses the VMOS virtual memory operating system. Several options include 64k bytes of additional memory, I/O expansion, up to 300M bytes of disc storage, and 800- or 1600-bit/in (315 or 630/cm) mag tape units. **Minimax Computers,** 1434 E Katella, Anaheim, CA 92805.
Circle 262 on Inquiry Card

ANTI-GLARE CATHODE-RAY TUBES

Data-Vu™ tubes feature a reflection-reducing, nonglare surface directly on the face of the bulb. JEDEC std tests gave gloss meter readings comparable to those of bonded etched panels with no significant loss of resolution. This feature is available on all bulb sizes and shapes. **Clinton Electronics Corp,** 6701 Clinton Rd, Rockford, IL 61131.
Circle 263 on Inquiry Card

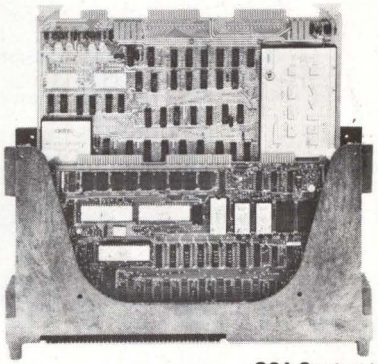
Intel compatible data acquisition system for only $495*

The low-cost ADAC Model 735 series of data acquisition systems is mounted on a single PC board that plugs into the same card cage as the Intel SBC-80/10, and SBC-80/20 single board computers and also the Intel MDS-800 microcomputer development system. The Model 735 bus interface includes a software choice of program control or program interrupt and a jumper choice of memory mapped I/O or isolated I/O.

The basic 735 OEM system which is contained on a single PC board (12" x 6.72" x 0.4") consists of 16 single-ended or 8 differential analog input channels, either voltage or current inputs (4-20 mA or 5-50 mA), 12 bit high speed A/D converter, sample and hold and bus interface. The throughput rate of the Model 735 is 35 KHz. Optionally available is the capability of expanding on the same card to a total of 64 single ended or 32 differential voltage/current inputs. up to two 12 bit D/A converters, software programmable gain amplifier with auto zero circuit, scope control and third wire sensing.

ADAC Corporation, 15 Cummings Park, Woburn, MA 01801.
(617) 935-6668

***Price in quantities of 1 to 4.**

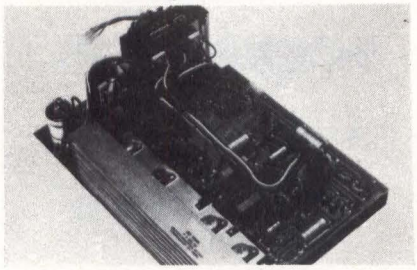


GSA Contract Group 66

adac corporation

PRODUCTS

DUAL FLOPPY DISC POWER SUPPLY



Multiple-output supply for OEM use provides 5 Vdc regulated at 18 A with OVP, 12 Vdc regulated at 4 A with OVP, 24 Vdc at 2 A, and −5 Vdc at 0.5 A. Peak rating is 21 A. Dimensions are 4 x 10 x 15" (10.2 x 25.4 x 38 cm). Unit incorporates "power OK" circuitry with TTL compatible output, 60-pulse/s line synchronized clock output, and individual outputs for each disc drive using standard AMP® connectors. Standard supplies with up to 25-A logic current are also available. **CEI Corp,** Grenier Industrial Pk, Londonderry, NH 03053.
Circle 264 on Inquiry Card

RS-232 INTERFACES FOR MATRIX PRINTER

Two RS-232 interfaces—one microprocessor controlled with a 128-, 960-, or 1968-char buffer and the other unbuffered—are available for the CP110 printer. The buffered version operates in receive only, half-duplex, and full-duplex modes. The 1968-char buffer transfers a 24 x 80 CRT screen without handshaking delays. Unbuffered unit for dumb CRT applications operates in simplex mode with reverse channel busy signal. Speeds are from 150 to 9600 bits/s for both. **Okidata Corp,** 111 Gaither Dr, Mount Laurel, NJ 08054.
Circle 265 on Inquiry Card

10-MHz VOLTAGE-FREQUENCY CONVERTER

Said to double the upper frequency limit previously available in VFCs, the 8710 opens up many high speed applications now served by ADCs. Six full decades of dynamic range provide high system resolution, single output simplifies interfacing, and high noise rejection make it well-suited to drive long lines. Max gain tempco is 100 ppm/°C. Analog input range is ±10 μV to ±10 V, min common mode voltage is ±10 V, and min full-scale frequency is 10 MHz. **Dynamic Measurements Corp,** 6 Lowell Ave, Winchester, MA 01890.
Circle 266 on Inquiry Card

IMPROVED CONVERSATIONAL BASIC COMPILER

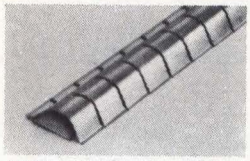
Compatible with Dartmouth BASIC, OS/3 Extended BASIC has been introduced for the company's 90/25, /30, and /40 systems. Enhancements include file support for sequential and direct access files, formatted printing, subprogram support, program segmentation, execution time limits, and execution of program stored on disc, as well as improved string support, matrix arithmetic, and I/O. Existing BASIC programs can be compiled and executed without change. **Sperry Univac, a div of Sperry Rand Corp,** PO Box 500, Blue Bell, PA 19422.
Circle 267 on Inquiry Card

T-1¾ GREEN/RED BICOLOR LED

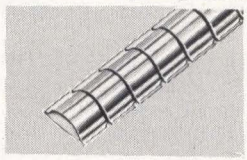
Lens of the go/no-go lamp is manufactured with a rugged uncolored diffused epoxy encapsulant which results in a lens fully flooded with light. High light output at low operating current is obtained from the III-IV compound technology combined with reflector design. Typ luminous intensities are 2 mcd for red and 4 mcd for green at a forward current (I_f) of 25 mA. Typ voltage drop for red and green is 2.4 V at 25 mA. **Opcoa Div of IDS Inc,** 330 Talmadge Rd, Edison, NJ 08817.
Circle 268 on Inquiry Card

When RFI problems get sticky, try sticky fingers®

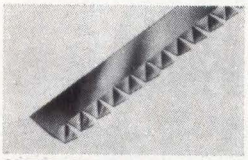
Attaches faster, shields better than anything else!



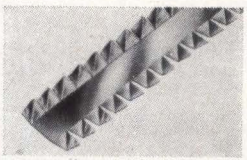
SERIES 97-500 The original Sticky Fingers with superior shielding effectiveness.



SERIES 97-520 A smaller size strip; highly effective in less space.



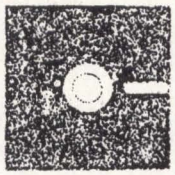
SERIES 97-555 New Single-Twist Series for use when space is at a premium. Measures a scant ⅜" wide.



SERIES 97-560 New ½" wide Double-Twist Series, ideal for panel divider bar cabinets.

Now you can specify the exact type beryllium copper gasket that solves just about every RFI/EMI problem. Perfect for quick, simple installation; ideal for retro-fitting. Self-adhesive eliminates need for special tools or fasteners. Write for free samples and catalog.

INSTRUMENT SPECIALTIES COMPANY, Dept. CD-57
Little Falls, N. J. 07424
Phone—201-256-3500 • TWX—710-988-5732



CP/M™ CONTROL PROGRAM FOR MICROCOMPUTERS

CP/M FOR SBC 80/10, 80/20

CP/M, the industry standard diskette operating system, is widely used for microcomputer software development and is the basis for many application software packages. CP/M facilities include dynamic file management, a fast assembler, general purpose text editor, and advanced debugger. Hardware requirements for the SBC Version of CP/M are SBC 80/10 or 80/20 (please specify when ordering) with minimum of 16 kilobytes of RAM starting at location 4000 (hex) and the Intel SBC 201 Disk Controller (other controllers can be supported through field modification of the software). Cost of the SBC Version of CP/M is $200, which includes IBM-compatible single density diskette, bootstrap PROM and documentation. Additional software available from **Digital Research** includes MAC Macro Assembler, SID Symbolic Instruction Debugger, and TEX Text Formatter.

DIGITAL RESEARCH

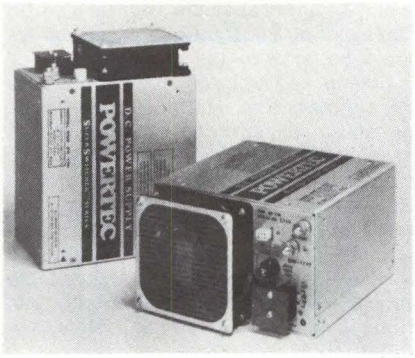
P.O. Box 579 • Pacific Grove, California 93950
(408) 649-3896

9-TRACK MAG TAPE DRIVE

200-in/s, 800/1600-bit/in, NRZI/phase encoded model MTU0610 supports Series 60, Levels 66, 66/DPS, 68, and 68/DPS computer systems. Dual density tape unit features data transfer rates of up to 320k bytes/s at 1600 bits/in (630/cm) and up to 160k bytes/s at 800 bits/in (315/cm), forward/reverse transport speed of 200 in/s (78.7 cm/s), full-reel rewind time of 45 s, and interrecord gap of 0.6" (1.5 cm). Automatic tape and head cleaners increase throughput. **Honeywell Inc, U.S. Information Systems Gp,** PO Box 6000, Phoenix, AZ 85005.

Circle 269 on Inquiry Card

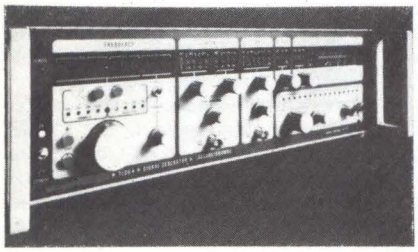
SINGLE-OUTPUT SWITCHING POWER SUPPLIES



Ten models added to the 9N "Super-Switcher™" series include outputs of 2, 5, 12, 15, and 24 V—each available at 250 and 400 W. Features are soft-start circuitry, logic inhibit function, and overload and overtemp protection. Motherboard design eliminates internal wire harnessing. The 5 x 8" (12.7 x 20.3-cm) unit with built-in fan cooling also has remote programming and up to 30-ms energy storage. Units undergo 24-h elevated temp burn-in with input and load cycle testing. **Powertec, Inc,** 20550 Nordhoff St, Chatsworth, CA 91311.

Circle 272 on Inquiry Card

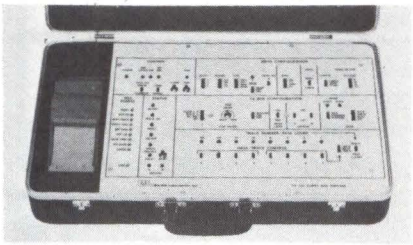
FULLY PROGRAMMABLE SIGNAL GENERATOR



Fully programmable via IEEE 488 bus, microprocessor-based model 7100 covers 300 kHz to 650 MHz with 1-Hz resolution. Optional doubler extends operation to 1.3 GHz. Single ASCII char string programs entire unit. Frequency switching speed is 100 ms. Modulation is am, fm, pm, VOR, FSK/PSK, and pulse. Spectral purity includes total noise spec of better than −136 dB/Hz at 20 kHz from carrier. Dynamic range, programmable in 0.1-dB steps, is 160 dB from 20 dBm to −140 dBm. **Comstron/Adret,** 200 East Sunrise Highway, Freeport, NY 11520.

Circle 270 on Inquiry Card

FLOPPY DISC EXERCISER

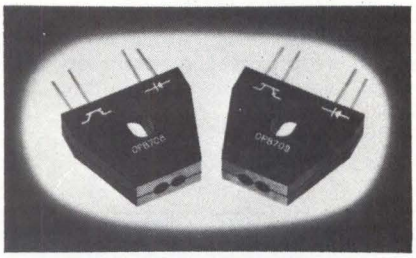


Typ problems encountered in floppy disc drives can be exercised and evaluated with model FX-500. Drive characteristics, controlled by switching, range from hard sectoring, 32-, 16-, 10-, or 8-sector pulses; separated or composite data and clock; single/dual heads; to 125k/250k/500k-byte/s transfer rates for std density. A variable step delay control and 6 stepping modes are provided. Also offered are 3 basic data patterns. **Wilson Laboratories, Inc,** 2536 E Fender Ave, Fullerton, CA 92631.

Circle 271 on Inquiry Card

PRODUCTS

REFLECTIVE OBJECT SENSORS



Designed for noncontact sensing applications, OPB 708 and 709 combine high efficiency solution-grown LED with silicon npn phototransistor (708), or max sensitivity photodarlington (709), in molded plastic package. With LED current of 40 mA and with OPB 708 positioned 0.150" (3.8 mm) from a reflective surface, typ output current is 50 μA for 90% diffuse surface and 1.0 mA for specular surface such as aluminum foil. Under similar conditions output current of OPB 709 is 7.5 mA and 100 mA. **Optron, Inc,** 1201 Tappan Cir, Carrollton, TX 75006.
Circle 273 on Inquiry Card

3-DIMENSIONAL DISPLAY SYSTEM

Over 13k short absolute vectors can be displayed at 30 frames/s from an internal buffer with the model 3303. For command and control applications, the unit can switch to nontransformed mode for static background data such as maps, and then overlay 3D dynamic images. The 16k-word, 16-bit buffer is expandable to 128k words. It is software compatible with the company's Series 3 3D displays and is supported by the VGAM/VGL FORTRAN callable software system. **Vector General, Inc,** 21300 Oxnard St, Woodland Hills, CA 91364.
Circle 274 on Inquiry Card

PATCH AND MONITOR MODULE

Full-duplex clock and data patching capability is provided by the model 3-2701 using miniature bantam jacks accessible from the front panel. Functions are break and insert signal, break and terminate line, and bridge line and monitor. Each monitor jack supplies a buffered output. Interface adapts to V.35, WECO 303, RS-232-C, MIL-188, or buffered TTL outputs using piggyback plug-in PC boards. **Telecommunications Techniques Corp,** 112 Frederick Ave, Rockville, MD 20850.
Circle 275 on Inquiry Card

20-kVA UNINTERRUPTIBLE POWER SYSTEM

System efficiency in excess of 83% and inverter efficiency of 90% are features of the UPS. Also included are frequency and phase synchronization, ¼-cycle solid-state transfer switch, output current limiting, short-circuit protection, and automatic float/equalize circuits. Specs are output voltage of 120 or 240 V; output frequency of 60 or 50 Hz; voltage regulation of ±1%, frequency regulation of ±0.5%; and overload to 150% for 30 min. **Nova Electric Mfg Co,** 263 Hillside Ave, Nutley, NJ 07110.
Circle 276 on Inquiry Card

1-PIECE SQUARE INDICATOR LIGHT FOR LEDS

A lens/mount for LEDs, Cubelite is square, offering 20% greater visibility and brightness. It uses std round T-1¾ LEDs. Edges and sides are of uniform thickness, with striated lines and fresnel rings. Using finger pressure, the unit is snapped into a 0.25" (0.64-cm) square hole or gang mounted in a 0.25" (0.64-cm) slot; the LED is then inserted into the back of the lens/mount. Butyrate plastic unit is available in 5 transparent colors. **Visual Communications Co,** PO Box 986, El Segundo, CA 90245.
Circle 277 on Inquiry Card

TERMINALS FROM TRANSNET

PURCHASE
12-24 MONTH FULL OWNERSHIP PLAN
36 MONTH LEASE PLAN

DESCRIPTION	PURCHASE PRICE	PER MONTH 12 MOS.	24 MOS.	36 MOS.
DECwriter II	$1,495	$145	$ 75	$ 52
DECwriter III, KSR	2,695	257	137	95
DECwriter III, RO	2,095	200	107	73
DECprinter I	1,795	172	92	63
VT100 CRT DECscope	1,595	153	81	56
TI 745 Portable	1,875	175	94	65
TI 765 Bubble Mem.	2,995	285	152	99
TI 810 RO Printer	1,895	181	97	66
TI 820 KSR Terminal	2,395	229	122	84
QUME, Ltr. Qual. KSR	3,195	306	163	112
QUME, Ltr. Qual. RO	2,795	268	143	98
ADM 3A CRT	875	84	45	30
HAZELTINE 1400 CRT	845	81	43	30
HAZELTINE 1500 CRT	1,195	115	67	42
HAZELTINE 1520 CRT	1,595	153	81	56
DataProducts 2230	7,900	725	395	275
DATAMATE Mini floppy	1,750	167	89	61

FULL OWNERSHIP AFTER 12 OR 24 MONTHS
10% PURCHASE OPTION AFTER 36 MONTHS

ACCESSORIES AND PERIPHERAL EQUIPMENT
ACOUSTIC COUPLERS • MODEMS • THERMAL PAPER
RIBBONS • INTERFACE MODULES • FLOPPY DISK UNITS

PROMPT DELIVERY • EFFICIENT SERVICE

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201-688-7800

CIRCLE 155 ON INQUIRY CARD

COMPONENTS ENGINEER

Our growth as a leading manufacturer of measuring and controlling instrumentation, computers and systems for the process industries, offers an outstanding career opportunity for an exceptional individual interested in supporting the advance design and development of our electronic instrumentation and computer systems.

We are looking for a talented professional with experience in the following areas:

- Evaluation of linear/digital IC including LSI and microprocessors
- Discrete components
- Reliability and failure analysis

Qualified individuals may forward resume and salary history in confidence to:

Technical and Professional Personnel
TAYLOR INSTRUMENT COMPANY
95 Ames Street
Rochester, NY 14601

SYBRON | Taylor

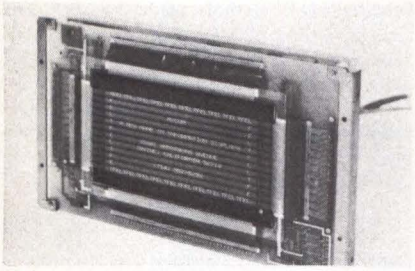
We Are An Equal Opportunity Employer M/F

CIRCLE 168 ON INQUIRY CARD

HIGH POWER DIGITAL-SYNCHRO CONVERTER

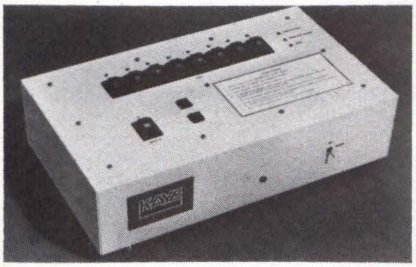
Miniature, modularized, series 192D500 units are TTL/CMOS compatible, and use industry std pinout and dimensional outline, with the exception of 2 added 10-32 Al studs for heat transfer. Converters accept 12-bit (0.088°) natural binary angle data at up to 4000°/s, and continuously convert to 3-wire synchro data with worst case accuracy of ±6 arc-min. All units are trimmed and adjustment-free. **Control Sciences, Inc,** 8399 Topanga Canyon Blvd, Canoga Park, CA 91304.
Circle 278 on Inquiry Card

THIN FILM DISPLAY ASSEMBLY



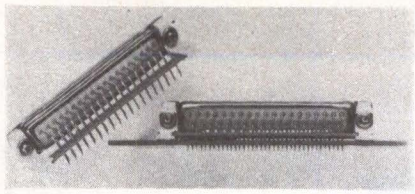
TFEL, an electroluminescent alphanumeric assembly panel measuring 2.4 x 18.8 x 7.9" (6.0 x 35.1 x 20 cm) is composed of a display panel and 3 PC boards. It is formatted for 480 char using a 7 x 9 dot matrix font. Char are refreshed at 100 Hz using a self-contained memory and char generator. Memory is asynchronously addressed by a 7-bit parallel ASCII code at 9600 baud or less. **Hycom, Inc,** 16842 Armstrong Ave, Irvine, CA 92714.
Circle 279 on Inquiry Card

P/ROM DUPLICATOR AND VERIFIER



P/ROM "Cloner," with 2 operator controls to select either "duplicate" or "verify" cycle, can produce up to 8 copies of a master P/ROM in less than 2 min. Duplicate cycle checks blank Intel 2716 or TI2516-type P/ROMs for proper erasure, duplicates from the master, and verifies. Verify cycle is used to check preprogrammed P/ROMs against a master. Failure of a P/ROM to pass test activates signal lamp above faulty unit. **Kaye Instruments, Inc,** 15 De Angelo Dr, Bedford, MA 01730.
Circle 280 on Inquiry Card

RIGHT ANGLE PC MOUNT CONNECTORS

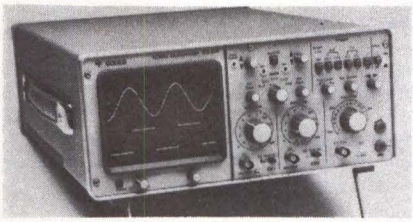


The 831 series expanded range of right angle PC mount subminiature type "D" connectors includes a fixed contact strap; nonmetallic, fully insulated plastic mounting bracket; and UL 94-VO rated thermoplastic insulator with a temp range of −55 to 105 °C. Modifications are available in all layouts of 9, 15, 25, 37, or 50 pins. Connectors mate with those of other manufacturers. **Souriau, Inc,** 7740 Lemona Ave, Van Nuys, CA 91405.
Circle 281 on Inquiry Card

FLAT CONDUCTOR CONNECTOR

"Clincher" terminates flat conductors of flat cable or flexible circuitry simultaneously. Connector accepts 1- to 2-oz (28- to 57-g), 0.062" (1.6-mm) wide copper cable, and is stackable on 0.100" (2.54 mm) centers in double row configurations. Available in 60/40 tin-lead plating over entire connector or gold stripe plating in the receptacle area, connector requires no cable stripping, and is compatible with 0.025" (6.4-mm) pins. **Berg Electronics Div, Du Pont Co,** Interstate 83, New Cumberland, PA 17070.
Circle 282 on Inquiry Card

15-MHz DUAL-TRACE/X-Y OSCILLOSCOPE



The OS255 uses an 8 x 10-cm rectangular CRT in a 5.25 x 12 x 16.5" (13 x 30 x 42-cm) case to present single-trace, dual-trace, or X-Y displays of signals within its frequency range. Specs include dc- to 15-MHz bandwidth (−3 dB), 2-mV/cm vertical sensitivity over full bandwidth, and timebase speeds to 500 ns/cm (a 5X Expand gives an effective max sweep speed of 100 ns/cm). Triggering modes include ac and dc coupling plus TV—all with + or − slope selection. **Gould Inc, Instruments Div,** 3631 Perkins Ave, Cleveland, OH 44114.
Circle 283 on Inquiry Card

TICKET PRINTER

Designed for printing document forms, the printer uses a 40-col impact mechanism which prints a 64-char ASCII alphanumeric set in a 5 x 7 dot matrix pattern. Multiple copy forms may be printed with a max throughput rate of 50 char/s. The microprocessor controlled serial interface accepts RS-232-C or 20-mA current loop data at any of 8 selectable baud rates from 110 to 9600. Input format handles 10- or 11-bit ASCII data with even, odd, or no parity. A 200-char buffer is included. **Micro Peripherals, Inc,** 2099 W 2200 S, Salt Lake City, UT 84119.
Circle 284 on Inquiry Card

QUAD ISOLATED DC-AC CONVERTER

The 724 converts a single 5- to 16-Vdc input into 4 pairs of isolated +/− outputs having about half the input voltage. Contained in a 1.1 x 1.1 x 0.3" (27.0 x 27.9 x 7.6-mm) 20-pin ceramic DIP, the converter can provide 128-mA total output current at rated voltage accuracy and up to 500 mA without damage. There is 1k-V continuous, 3k-V test isolation between the 4 output channels and between input and outputs. **Burr-Brown Research Corp,** International Airport Industrial Pk, Tucson, AZ 85734.
Circle 285 on Inquiry Card

The end is near.

See page 161

LITERATURE

Backpanel Packaging Systems

Covering both PC and metal plate packaging with photos, drawings, charts, and graphs, brochure discusses single- or multilayer backpanels with Press-T-Mate™ interconnects for PC boards or ECS card-edge connectors for metal plates. **ITT Cannon Electric,** Santa Ana, Calif.
Circle 300 on Inquiry Card

Mass Termination Systems

Brochure contains specs, photos, and line drawings of Jet-Flecs product line for 0.150, 0.100, and 0.156" (0.381-, 0.254-, and 0.396-cm) centers, and describes basic cost/labor saving techniques used with the devices. **Molex Inc,** Lisle, Ill.
Circle 301 on Inquiry Card

Magnetic Tape Controller

Data sheet describes TC-150, explains its features, and illustrates the unit as well as listing software and service information. **Western Peripherals Div, Wespercorp,** Anaheim, Calif.
Circle 302 on Inquiry Card

Microprocessor Displays

Summarizing line of microprocessor display interfaces, catalog includes details on company's video RAM, graphic, and alpha-chip product lines, plus accessories. **Matrox Electronic Systems,** Montreal, Quebec, Canada.
Circle 303 on Inquiry Card

Electronic Wire/Cable

Construction details as well as physical specs and electrical characteristics in both conventional and metric units are provided in updated catalog listing more than 1300 constructions. **Belden Corp, Electronic Div,** Richmond, Ind.
Circle 304 on Inquiry Card

Minicomputers

Effective Use and Application of Minicomputers, a 350-p book, provides a practical look at minis, peripherals, characteristics, installation, operation, uses, problem areas, and strengths/weaknesses, with evaluation factors for selecting hardware and programming languages. Price is $32.50 U.S. ($28.50 prepaid). **Q.E.D. Information Sciences, Inc,** PO Box 181, 141 Linden St, Wellesley, MA 02181.

Custom LSI Capability

Brochure describes the company's approach to custom LSI, listing technologies and design techniques used, and customer derived benefits. **Alphatron, Inc,** Cupertino, Calif.
Circle 305 on Inquiry Card

Clustered Terminal System

Brochure describes advantages and details features of System 4000, discussing how they allow expansion of capabilities from simple cluster emulation terminals to distributed processing. **Racal-Milgo Information Systems, Inc,** Miami, Fla.
Circle 306 on Inquiry Card

Heat Sinks

Dimensional information, temp curves, and application information for fabricated heat sinks are supplied in catalog which illustrates standard and special extrusions. **Aavid Engineering, Inc,** Laconia, NY.
Circle 307 on Inquiry Card

DC Power Supplies

Featuring 2- to 24-V, 40- to 220-A, single-, dual-, triple-, and quad-output units, catalog contains all information needed to specify high efficiency power ranging from 200 to 1500 W. **Switching Power, Inc,** Bohemia, NY.
Circle 308 on Inquiry Card

Oscilloscopes

Application features and specs for high performance, dual- and single-trace scopes are spotlighted in 16-p booklet detailing eight models available in 3 and 5" (8- and 13-cm) CRT display formats. **Leader Instruments Corp,** Plainview, NY.
Circle 309 on Inquiry Card

Fans/Blowers

Catalog contains specs, cutaway and dimensional drawings, datings, and performance curves for box and open fans and FHP blowers, and presents specs for line of unit bearing motors. **Howard Industries,** Milford, Ill.
Circle 310 on Inquiry Card

Solderless Connectors

Mechanical simplicity, convenience, and dependability of "Scotchflex" cable/connector system are enhanced by six improvements described in brochure. **3M Co, Electronic Products Div,** St Paul, Minn.
Circle 311 on Inquiry Card

Power Supplies

In addition to detailed descriptions and specs for switching regulated and ferroresonant power supplies, catalog offers data on standard, series regulated, and modular supplies, and power system accessories. **NJE, a div of Technology Development Corp,** Dayton, NJ.
Circle 312 on Inquiry Card

Trimmer Resistors

Detailed information on Cerbon™ and Cermet resistors in catalog comprises electrical, environmental, and mechanical specs, with emphasis on performance data for ceramic base trimmers. **Centralab Electronics Div, Globe-Union Inc,** Milwaukee, Wis.
Circle 313 on Inquiry Card

Distributed Processing Systems

"Building Your XL Distributed Processing Network" discusses advantages offered by distributed processing, and describes XL40 and XL20 systems and a remote online subsystem for creation of network nodes. **Pertec Computer Corp, CMC Div,** Los Angeles, Calif.
Circle 314 on Inquiry Card

Automated Manufacturing Technologies

Free bimonthly publication devoted to NC and CAM, *N/C Commline* focuses on subjects such as robots CNC, group technology, NC programming, CAD, and machine tool advancements. **Numeridex, Inc,** Wheeling, Ill.
Circle 315 on Inquiry Card

European Line Voltage Selector Switches

Literature provides details on two series of line voltage selector switches designed for test epuipment, instruments, and OEM products sold in international markets. **Switchcraft, Inc,** Chicago, Ill.
Circle 316 on Inquiry Card

Connectors

Guide provides complete specs and dimensional drawings for card-edge, Reli-Amod®, single readout wirewrap, fork contact plugs and receptacles, test point, right angle molded, NAFI headers and receptacles, and relay connectors. **Methode Electronics, Inc, Connector Div,** Chicago, Ill.
Circle 317 on Inquiry Card

CRT Displays/Video Monitors

Brochure describes line of color and B/W monitors, and 5, 9, and 12″ (13-, 23-, and 30-cm) CRT displays, and discusses company's capabilities to produce specialized OEM modifications. **Audiotronics, Video Display Div,** New Brighton, Minn.
Circle 318 on Inquiry Card

Passive Components

Electrical and mechanical data, and applications information are included in catalog C-564A for 18 product types including capacitors, resistors, voltage converters, pulse transformers, and interference filters. **Sprague Electric Co,** North Adams, Mass.
Circle 319 on Inquiry Card

COS/MOS Integrated Circuits

Designers' aid provides max ratings, recommended operating conditions, static electrical characteristics, classification, and selection charts, and functional diagrams for line of digital ICs. **RCA Solid State Div,** Somerville, NJ.
Circle 320 on Inquiry Card

Automatic Test Equipment

Pointing out hidden costs that affect the total cost of an ATE system, brochure describes features of the System 390 circuit board tester, and offers a no-obligation evaluation of cost savings that can be achieved by its use. **Instrumentation Engineering, Inc,** Franklin Lakes, NJ.
Circle 321 on Inquiry Card

Remote Multiplexer

Process control applications of high speed remote multiplexing system are detailed in 10-p booklet that includes system flow diagram describing capabilities and benefits of system. **The Anaconda Co, Wire and Cable Div,** Greenwich, Conn.
Circle 322 on Inquiry Card

Communications System Performance

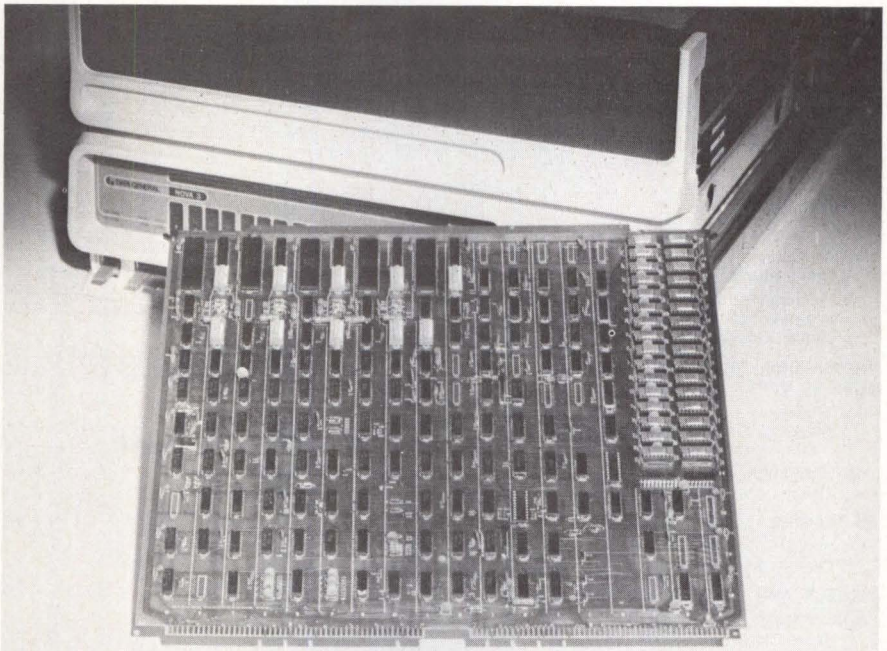
"Determination of Performance of Data Communications Systems That Use Bit-Oriented Communication Control Procedure," a draft document of proposed standard BSR X3.79, covers performance of data communications links and networks. Copies may be obtained by sending $3 to **CBEMA Standards,** 1828 L St, NW, Washington, DC 20036.

Cabinet Racks

Design features for line of equipment enclosures are highlighted in catalog which also presents dimensional diagrams and lists of optional modules and accessories. **Bud Industries, Inc,** Willoughby, Ohio.
Circle 323 on Inquiry Card

Digitizing System

Brochure presents general system description, typical applications, operational software, and system hardware for both basic and interactive configurations of Datagrid II. **Summagraphics Corp,** Fairfield, Conn.
Circle 324 on Inquiry Card



Our Quintroller can make your Nova 3/4* a systems star!

The Quintroller can slash system cost and bulk by making a 4-slot Data General NOVA 3/4 chassis do the work of a 12-slot chassis. That's because a 15″ x15″ Quintroller card contains a 64KB MOS memory plus four additional functions: four asynchronous communications channels, parallel line printer interface, real time clock, and TTY port. This card replaces four individual boards from Data General. Quintroller software compatibilities include:

- Communication channels—DG 4060 Multiplexer
- Printer—DG 4034/4193 Controller
- Clock & TTY—DG 4008 & 4010
- Memory—DG 8547.

The printer controller interfaces Data Products, Centronics, Printronics, Tally and equivalent printers. The Model 28XX Quintroller, configured to your requirements, with cable set and documentation, can be delivered in 30 days from

RIANDA
ELECTRONICS, LTD.
2535 Via Palma Ave. • Anaheim, CA 92801
Telephone: (714) 995-6552
Contact us for all your Data General controller needs.
*Registered Trade Mark of Data General Corp.

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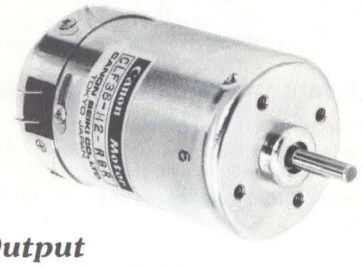

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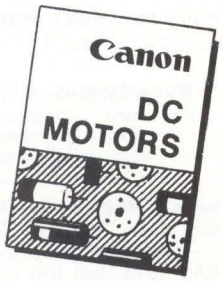

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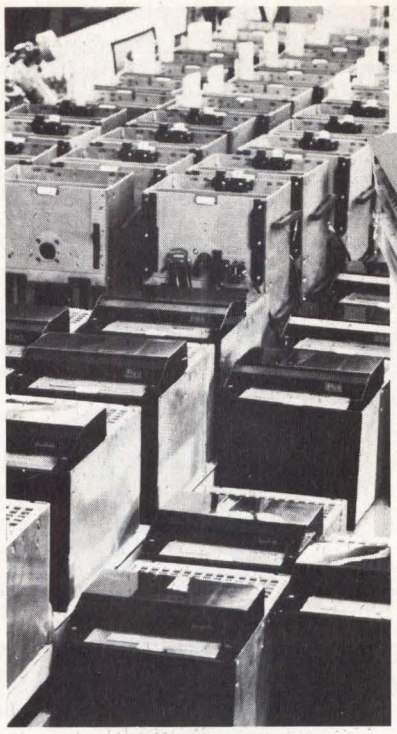

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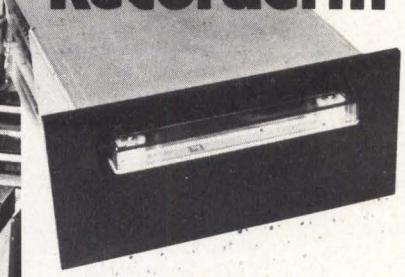

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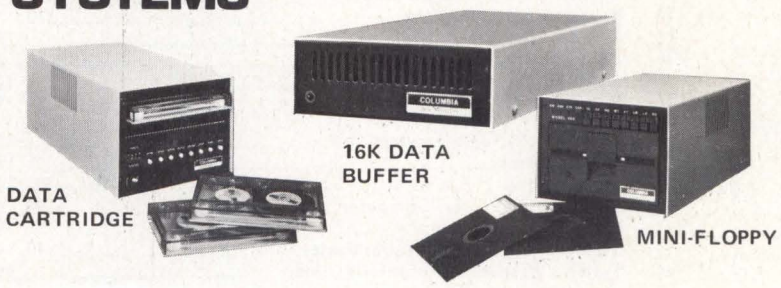

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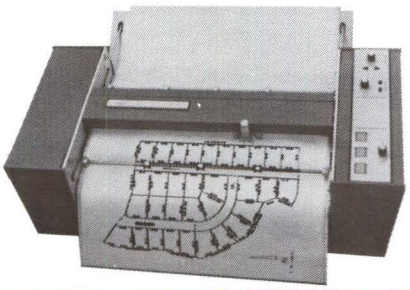

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