

# COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

DECEMBER 1978

REALTIME PROTOTYPE ANALYSIS AS A MICROPROCESSOR DESIGN AID

INTEGRATING PERIPHERALS INTO PROCESSING SYSTEMS

WIDEBAND COMMUNICATION SYSTEM IMPROVES RESPONSE TIMES

4155634321  
382946  
7710  
DE004  
CA 94115  
WA HILL  
ENGR  
INST OF VISUAL SCIENCE  
2232 WEBSTER  
SAN FRANCISCO

```
> GO 0  
LOC INST MNEM OPER SP RF RA RB RC RD RE  
0006 00 NOP 0000 56 00 00 00 00 00  
0006 BREAK
```

```
> DRT 10  
ADDR DATA MNEMONIC EXTERNAL BUS  
0005 00 00000000 M R  
0002 3C IMR A 00000000 M R F  
0003 C2 JNZ 00000000 M R F  
0004 02 00000000 M R  
0005 00 00000000 M R  
0002 3C IMR A 00000000 M R F  
0003 C2 JNZ 00000000 M R F  
0004 02 00000000 M R  
0005 00 00000000 M R  
0006 00 NOP 00000000 M R F
```

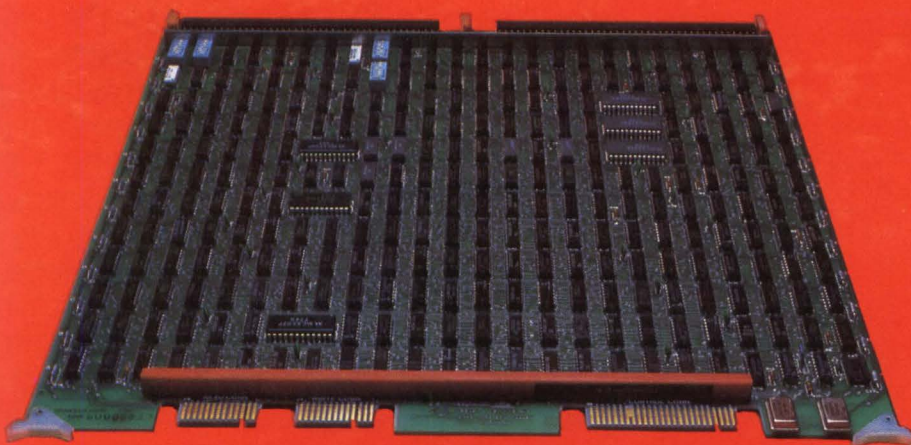
```
> CNT  
COUNT=01619 USEC
```

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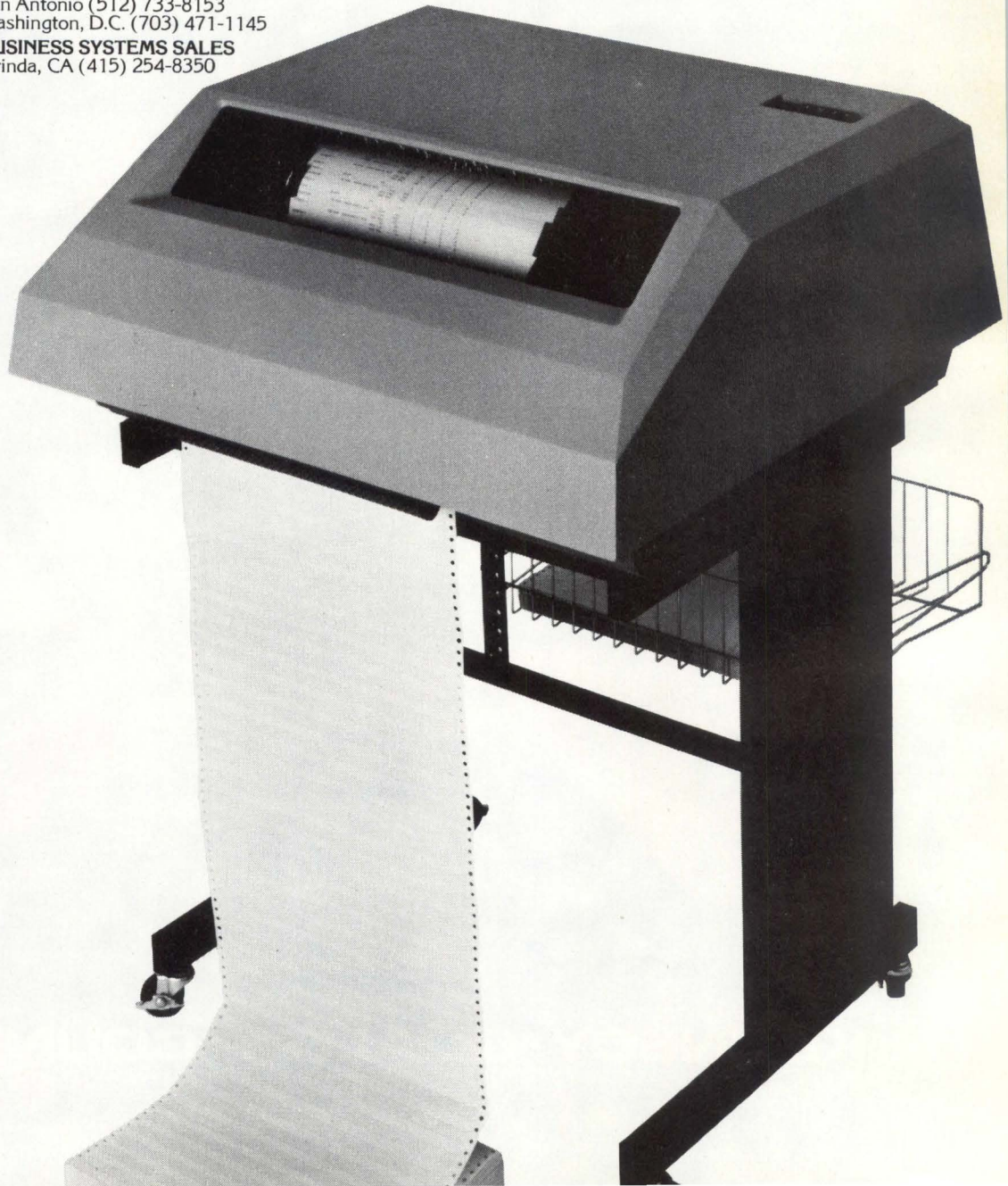
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**THIS ISSUE  
CONTAINS  
5-YEAR  
EDITORIAL  
INDEX—  
PAGES A1-A24**

# COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

DECEMBER 1978

VOLUME 17, NUMBER 12

## DEPARTMENTS

- 6 LETTERS TO THE EDITOR**
- 10 CALENDAR**
- 14 COMMUNICATION CHANNEL**  
This final article reviews the dramatic technological, applications, and regulatory developments that have occurred in data communications since the column began in January 1970
- 33 DIGITAL TECHNOLOGY REVIEW**  
Two midrange business computer systems employ SOS LSI technology to achieve high performance, while reducing size, cost, and power requirements
- 50 DIGITAL CONTROL AND AUTOMATION SYSTEMS**  
A microcomputer controlled laser welding system spot welds terminals on miniature relays four times as fast and more reliably than a resistance welding system
- 104 TECH BRIEF**
- 106 DESIGN BRIEF**
- 110 MICRO DATA STACK/ PROCESSORS AND ELEMENTS**  
External realtime clocks—programmable, free-running, and time-of-day—can precisely time intervals, freeing the microcomputer to simultaneously handle other functions
- 122 MICRO DATA STACK/ COMPUTERS AND SYSTEMS**  
A customized development system supports installation, testing, and checkout of a microprocessor based data acquisition system using a hardware oriented design approach
- 144 AROUND THE IC LOOP**  
Powerful computational tools result from combination of arithmetic processing chips with the control capabilities of the microprocessor. Available devices range from multiplier-accumulator chips to firmware programmable chips having all necessary arithmetic elements and control circuits
- 164 PRODUCT FEATURE**  
Standard one measurement and control system provides all necessary signal conditioning and logic to permit direct sensor hookup
- 185 LITERATURE**
- 186 GUIDE TO PRODUCT INFORMATION**
- 190 ADVERTISERS' INDEX**

Reader Service Cards  
pages 193-196

## FEATURES

**REALTIME PROTOTYPE ANALYSIS  
AS A MICROPROCESSOR DESIGN AID 65**  
by Robert Francis and Robin Teitzel

Design/development aid provides actual emulation of all system elements during in-process execution to ease the complex task of integrating hardware and software into a prototype microprocessor based system

**INTEGRATING PERIPHERALS INTO PROCESSING SYSTEMS 77**  
by Reinholdt J. Eufinger

Advantages and disadvantages of each of three design approaches to connecting peripherals to CPUs—hardware, software, and combined hardware/software—are investigated as to development, application, and cost

**WIDEBAND COMMUNICATION SYSTEM  
IMPROVES RESPONSE TIMES 85**  
by James F. Wanner

Data handling system for economical computer-peripheral interactive communications at distances up to 20 miles is marked by wide bandwidth, fast response time, reliable performance, and multiple interconnect ports

**BCD/BINARY CONVERSION WITH SINGLE IC CELL 94**  
by M. G. Phadnis and D. Joshi

A hardware design approach for fast conversion of whole or fractional numbers from binary to BCD or BCD to binary proves the feasibility of implementing these capabilities within single integrated circuit chip

**5-YEAR INDEX A1**

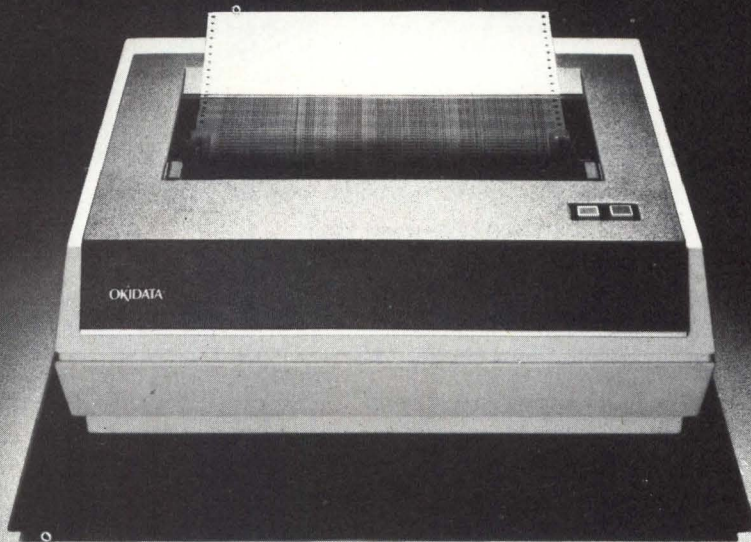
Advances in the electronics industry are documented in alphabetical index of feature material published in *Computer Design* over the past five years



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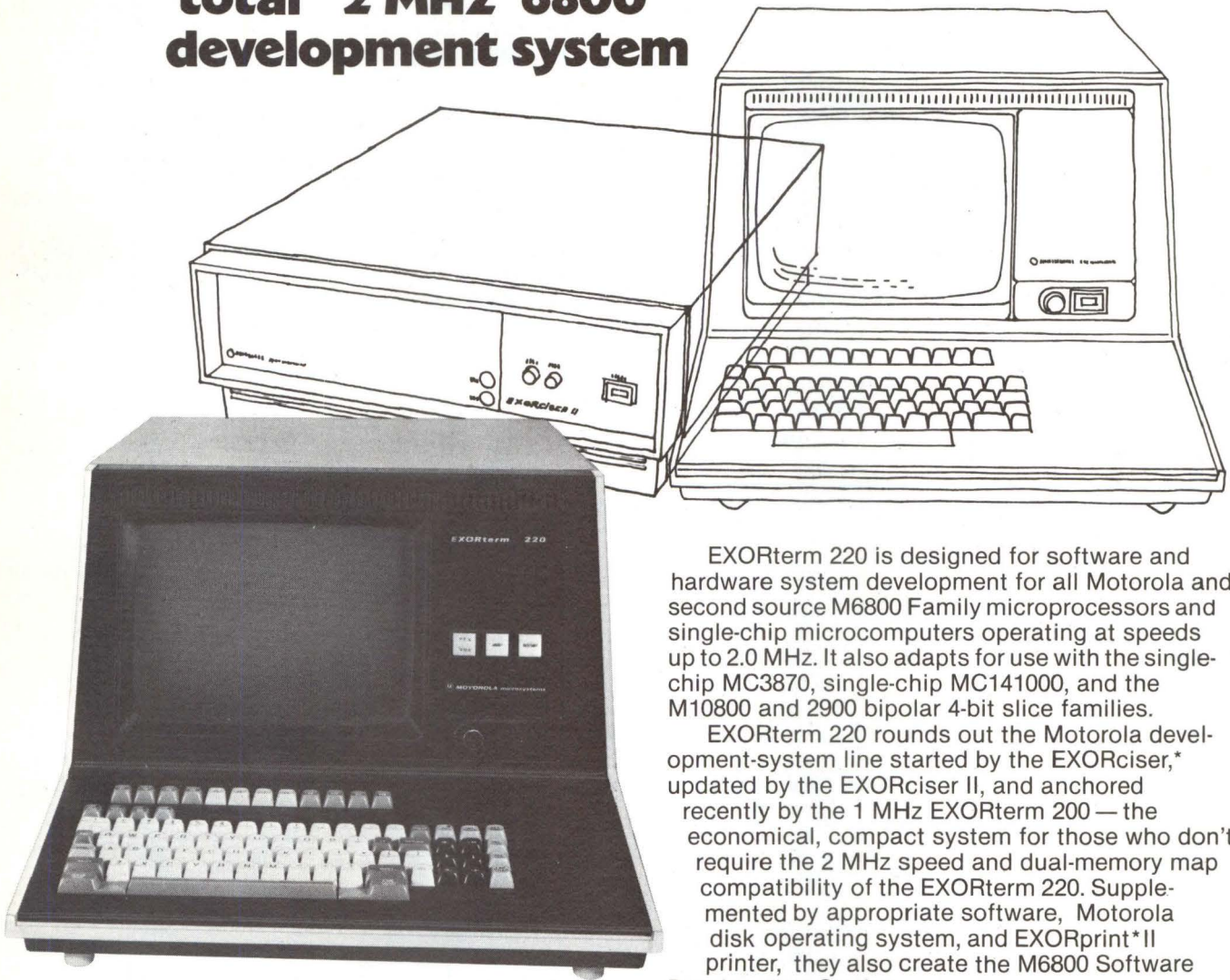
Editorial manuscripts should be addressed to Editor, Computer Design, 11 Goldsmith St., Littleton, MA 01460. For details on the preparation and submission of manuscripts, request a copy of the "Computer Design Author's Guide."

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Semiconductor Group

## LETTERS TO THE EDITOR

To the Editor:

The article entitled "Software-Based Single-Bit I/O Error Detection and Correction Scheme" (Sept 1978, pp 130, 134, 136, 137) presents a scheme for checking 4-bit characters by using three check bits. A direct table lookup is used to convert each 4-bit character to one of 16 reference 7-bit characters. A decode subroutine is then used to correct any single-bit error which may have occurred, to remove the check bits, and to restructure the character into the original 4-bit form.

Selection of the reference 7-bit characters and the subsequent checking and stripping of the check bits represent an elegant algorithm, and the detailed decode subroutine is a commendable academic exercise, but the 40-odd instructions which must be executed for every 4-bit character are entirely unnecessary for any practical implementation. A simple table lookup from 128 entries can be used to convert any 7-bit character to the original 4-bit character and even identify the error, if desired.

It is fairly simple to find a set of 16 reference patterns of 7 bits, each of which differs from the others by at least 3 bits. This ensures that the 7 patterns generated by a single error in each of the 16 reference patterns is distinct from those generated by a single error in any of the other 15. Thus, of the 128 7-bit patterns possible,  $7 \times 16 = 112$  are unique error transforms of the original 16. It is not difficult, therefore, to associate each of the 128 entries in a table with the original 4-bit pattern and even identify which bit was in error to generate that entry.

John M. Harriman  
General Electric Nuclear Energy  
Group  
San Jose, Calif

To the Editor:

The Design Note entitled "Software-Based Single-Bit I/O Error Detection and Correction Scheme" (Sept 1978, pp 130, 134, 136, 137) interested me

for a variety of reasons. However, I would like to point out one misleading "conclusion" shown on p 134, ie, "A triple error would be received as if it were correct; no error would be detected."

This is not, in general, true. Using the scheme and notations in that article, an example is given as follows. Assuming that  $I_3 I_5 I_6 I_7 = 0000$  ( $C_1 C_2 I_3 C_4 I_5 I_6 I_7 = 0000000$ ), and  $I_3, I_5,$  and  $I_7$  are incorrect ( $C_1 C_2 I_3 C_4 I_5 I_6 I_7 = 0010101$ ), error pattern 001 can easily be derived. This pattern, however, reflects information on error detection in some sense other than "as if it were correct."

Tzong-Yu Paul Lee  
Sycor, Inc  
Ann Arbor, Mich

To the Editor:

Your Aug 1978 publication contained an article by John E. Buckley on "Multi-Vendor Information Systems" (pp 11-12), which was misleading with respect to the Bell of Pennsylvania policy on joint inter-vendor diagnostic testing efforts. The article implies that Bell of Pennsylvania does not participate in cooperative diagnostic efforts at a customer's premise. This is simply not the fact; indeed, the contrary is true.

In our zeal to effectively support customer data communications needs, we, as well as all other Bell System Operating Companies, have established especially trained "data communication systems oriented" organizations to accommodate the in-depth diagnostic requirements inherent in multi-vendor environments. This course of action was instituted in the early 1970s when it became apparent that meaningful inter-vendor cooperative efforts required a level of technical expertise that was beyond the scope of our normal "service personnel." Only subsequent to the establishment of these specialized organizations did we place the cooperative diagnostic constraints on our normal service personnel mentioned in the Buckley article.

The existence and function of these specialized organizations termed Data Technical Support (DATEC) and Customer Software Support Specialists (CSSS) is well known throughout the Bell System, as well as to the data communications vendor community. Many articles acknowledging these organizations have appeared in trade journals, eg, *Computerworld* (July 1973), *Telephone Engineering and Management* (Mar 1975, Aug 1978), and *Data Management* (Sept 1973). In addition, listings detailing specific DATEC contacts in each Bell System Operating Company have been distributed to requesting vendors by AT&T headquarters.

To bring these specialized organizations into action, a customer need only express this requirement to the normal telephone company interface, ie, service or marketing representative, once each involved vendor has unilaterally verified the proper performance of his portion of the overall data communications system.

Thomas K. Weigand  
Bell of Pennsylvania  
Philadelphia, Pa

Letters to the Editor should be addressed:

Editor, Computer Design  
11 Goldsmith St  
Littleton, MA 01460

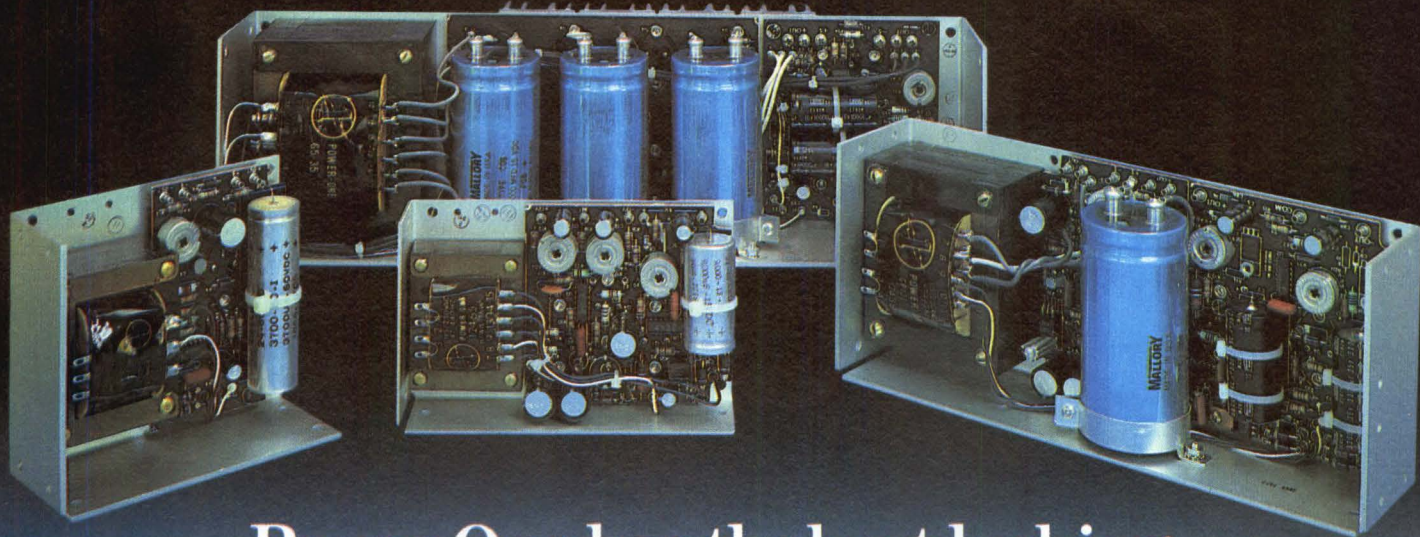
### CORRECTION

In the October Micro Data Stack/Computers and Systems item entitled "Emulator Permits Faster File Sorting and Accessing" contained on pp 190, 192, the access times of the General Robotics SDV11 SUPERDISK should be listed as under 100  $\mu$ s. It should also be noted that the logic and timing strategies discussed "are designed . . . so that the memory seems to be always ready to transfer data from the sector being addressed."



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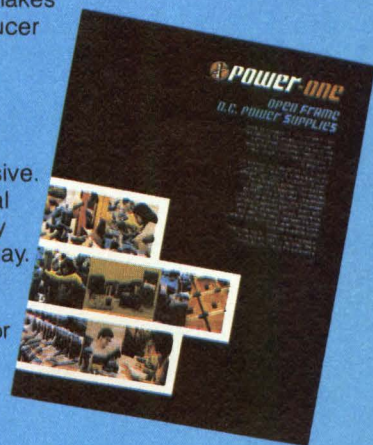
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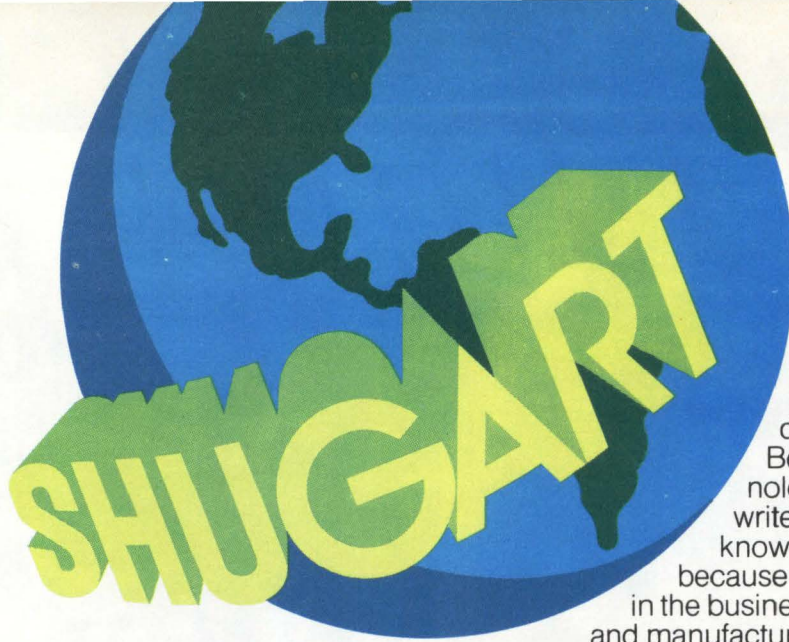
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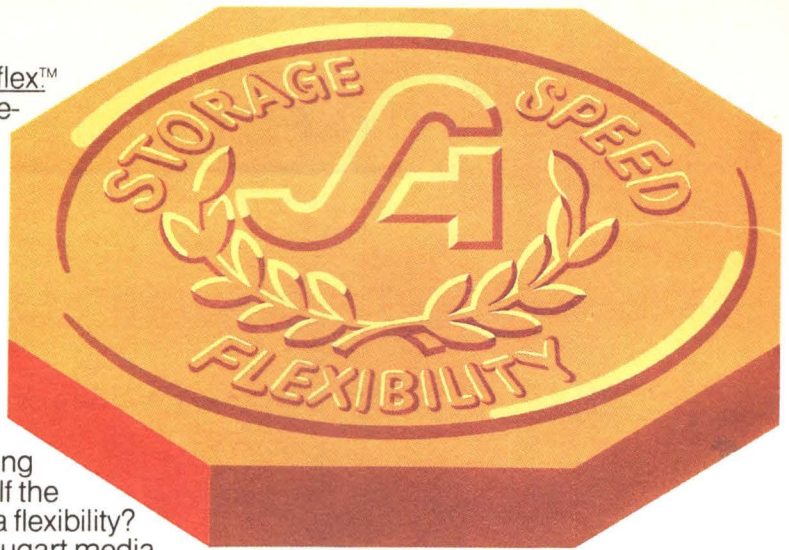
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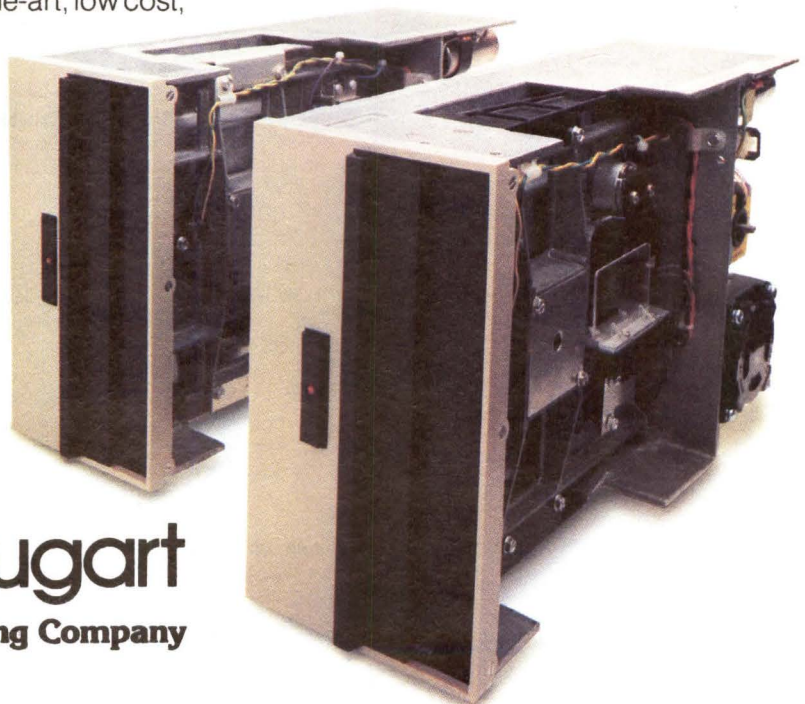
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# CALENDAR

## CONFERENCES

**JAN 8-9—Internat'l Sym on Mini and Microcomputers in Control**, Islandia Hyatt House, San Diego, Calif. INFORMATION: The Secretary, Computers in Control Symposium, PO Box 2481, Anaheim, CA 92804. Tel: (714) 774-6144

**JAN 16-18—Internat'l Sym on Mini and Microcomputers (MIMI)**, Disneyland Hotel, Anaheim, Calif. INFORMATION: MIMI 79 Anaheim, PO Box 2481, Anaheim, CA 92804. Tel: (714) 774-6144

**JAN 16, FEB 8, and FEB 26—Invitational Computer Conf**, Orange County, Calif; Ft Lauderdale, Fla; and Atlanta, Ga. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: (714) 644-6037

**JAN 22-26—Computers and Peripheral Trade Show**, London, England. INFORMATION: E. Belden, U.S. Dept of Commerce, Bureau Export Div, Washington, DC 20230

**JAN 30-FEB 1—Communication Networks**, Sheraton-Park Hotel, Washington, DC. INFORMATION: Ed Halsted, The Conference Co, 60 Austin St, Newton, MA 02160. Tel: (617) 964-4550

**FEB 6-8—Sym on Modeling and Performance Evaluation of Computer Systems**, Technische Universität Wien, Austria. INFORMATION: Dr A. Butrimenko, Internat'l Institute for Applied Systems Analysis, A-2361 Laxenburg, Austria

**FEB 14-16—European Conf on Parallel and Distributed Processing**, Toulouse, France. INFORMATION: C. Girault, Institut de Programmation, 4 Place Jussieu, 75230 Paris Cedex 05, France

**FEB 14-16—IEEE Internat'l Solid State Circuits Conf (ISSCC)**, Philadelphia, Pa. INFORMATION: Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: (305) 446-8193

**FEB 26-MAR 1—COMPCON Spring**, San Francisco, Calif. INFORMATION: COMPCON Spring 79, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

**FEB 26-MAR 2—INTELCOM**, Dallas Convention Ctr, Dallas, Tex. INFORMATION: M. Raftery, Mgr of Promotion, Horizon House Internat'l, 610 Washington St, Dedham, MA 02026. Tel: (617) 326-8220

**FEB 27-MAR 2—NEPCON WEST**, Anaheim Convention Ctr, Anaheim, Calif. INFOR-

MATION: Industrial and Scientific Conf Management, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

**FEB 28-MAR 2—Internat'l Computer Expo**, Tokyo Internat'l Trade Ctr, Tokyo, Japan. INFORMATION: Golden Gate Enterprises, Inc, 1307 S Mary Ave, Suite 210, Sunnyvale, CA 94087. Tel: (408) 735-1122

**MAR 4-8—Business Systems Exhibition**, U.S. Trade Ctr, Tehran, Iran. INFORMATION: Susan Blackman, Project Mgr, Commerce Action Group for the Near East (CAGNE), Rm 6015B, Washington, DC 20230. Tel: (202) 377-2952

**MAR 6-8—Optical Fiber Communication**, Shoreham Americana Hotel, Washington, DC. INFORMATION: Optical Society of America, 2000 L St, NW, Suite 620, Washington, DC 20036. Tel: (202) 293-1420

**MAR 19-21—IECI Conf and Exhibit on Industrial and Control Applications of Microprocessors**, Philadelphia, Pa. INFORMATION: S. J. Vahaviolos, Physical Acoustics Corp, PO Box 3135, Princeton, NJ 08540. Tel: (609) 799-8266

**MAR 25-28—Numerical Control Society Annual Meeting and Technical Conf**, Marriott Hotel, Los Angeles, Calif. INFORMATION: Joyce Scholl, Numerical Control Society Headquarters, 1800 Pickwick Ave, Glenview, IL 60025

**APR 2-6—Computers and Peripheral Equipment**, Melbourne, Australia. INFORMATION: Peter Ryan, Office of International Marketing, Industry and Trade Administration, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-2849

**APR 3-5—Specifications of Reliable Software Conf**, Hyatt Regency Hotel, Cambridge, Mass. INFORMATION: Software Engineering, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

**APR 9-12—INTERFACE**, Chicago, Ill. INFORMATION: Sheldon G. Adelson, President, Datacomm Interface, Inc, 160 Speen St, Framingham, MA 01701

**APR 23-25—Sym on Computer Architecture**, Marriott Hotel, Philadelphia, Pa. INFORMATION: Dr Barry Borgerson, Sperry Univac, PO Box 500, Blue Bell, PA 19422. Tel: (215) 542-2013

**APR 24-26—Electro**, New York Coliseum and Americana Hotel, New York, NY. INFORMATION: William C. Weber, Jr, General Mgr, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965

**APR 24-26—Reliability Physics Sym**, Airport Hilton, San Francisco, Calif. INFORMATION: Dr Frank B. Micheletti, Rockwell International, Electronics Research Ctr, D/545, 022-HA27, 3370 Miraloma Ave, Anaheim, CA 92803. Tel: (714) 632-4380

**MAY 21-23—European Hybrid Microelectronics Conf and Exhibition**, Internat'l Congress Centre, Ghent, Belgium. INFORMATION: Prof R. Govaerts, Katholieke Universiteit Leuven, Afdeling E.S.A.T., Kardinaal Mercierlaan 94, B-3030 Heverlee, Belgium

## SEMINARS

**FEB 22-23 and MAR 29-30—Microprocessors: Hardware, Software, and Application**, Worcester Polytechnic Institute, Worcester, Mass; and Boston, Mass. INFORMATION: Ginny Bazarian, Program Coordinator, Office of Continuing Professional Education, Worcester Polytechnic Institute, Worcester, MA 01609. Tel: (617) 753-1411, X517

**MAR 19-20—Microcomputers: Operating Principles, Hardware, and Software; and MAR 21-23—Microcomputer Hardware and System Design**, Holiday Inn, Palo Alto, Calif. INFORMATION: Prof Donald D. French, Institute for Advanced Professional Studies, One Gateway Ctr, Newton, MA 02158. Tel: (617) 964-1412

## SHORT COURSES

**JAN 15-19—ECM and ECCM for Digital Communications**, **JAN 23-26—Design and Applications of Computer Graphics Systems**, **FEB 5-7—Data Compression: Techniques and Applications**, **FEB 7-9 and MAR 7-9—Microprocessors**, and **FEB 14-16—Applications of Microcomputers in Control Systems**, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

**Announcements intended for publication in this department of Computer Design must be received at least two months prior to the date of the event. To ensure proper timely coverage of major events, material preferably should be received six months in advance.**

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**DEC RX01**  
10½"  
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5¼"  
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Bootstrap included



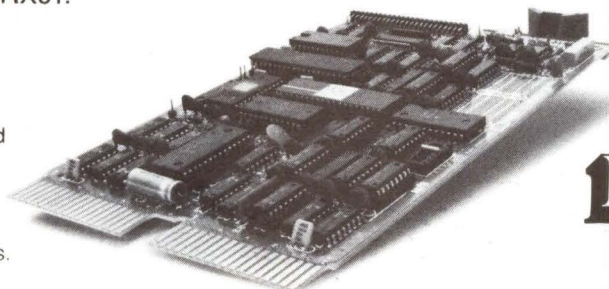
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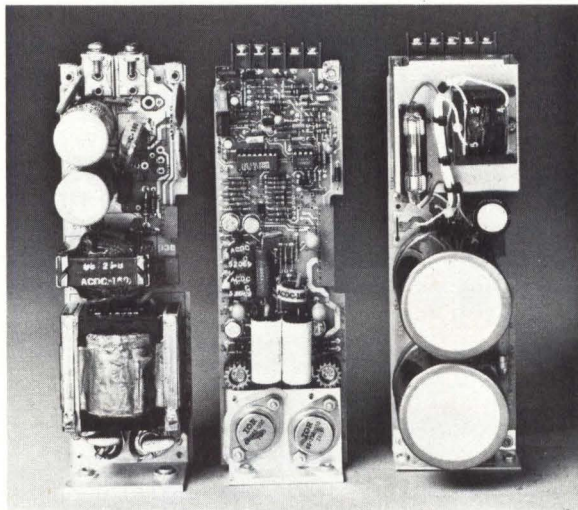
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# Our new Sub-M

## Beauty More than Skin Deep.

You might agree that our new RS/RT Series of single and triple output switchers are nicely packaged. The *real* beauty, however, of these high-performance supplies lies *under* their covers. Designed for high-reliability applications, they consist of three separate function sub-modules. An input board, converter board and an output board are joined by a mother strip to eliminate all interconnecting harnessing.

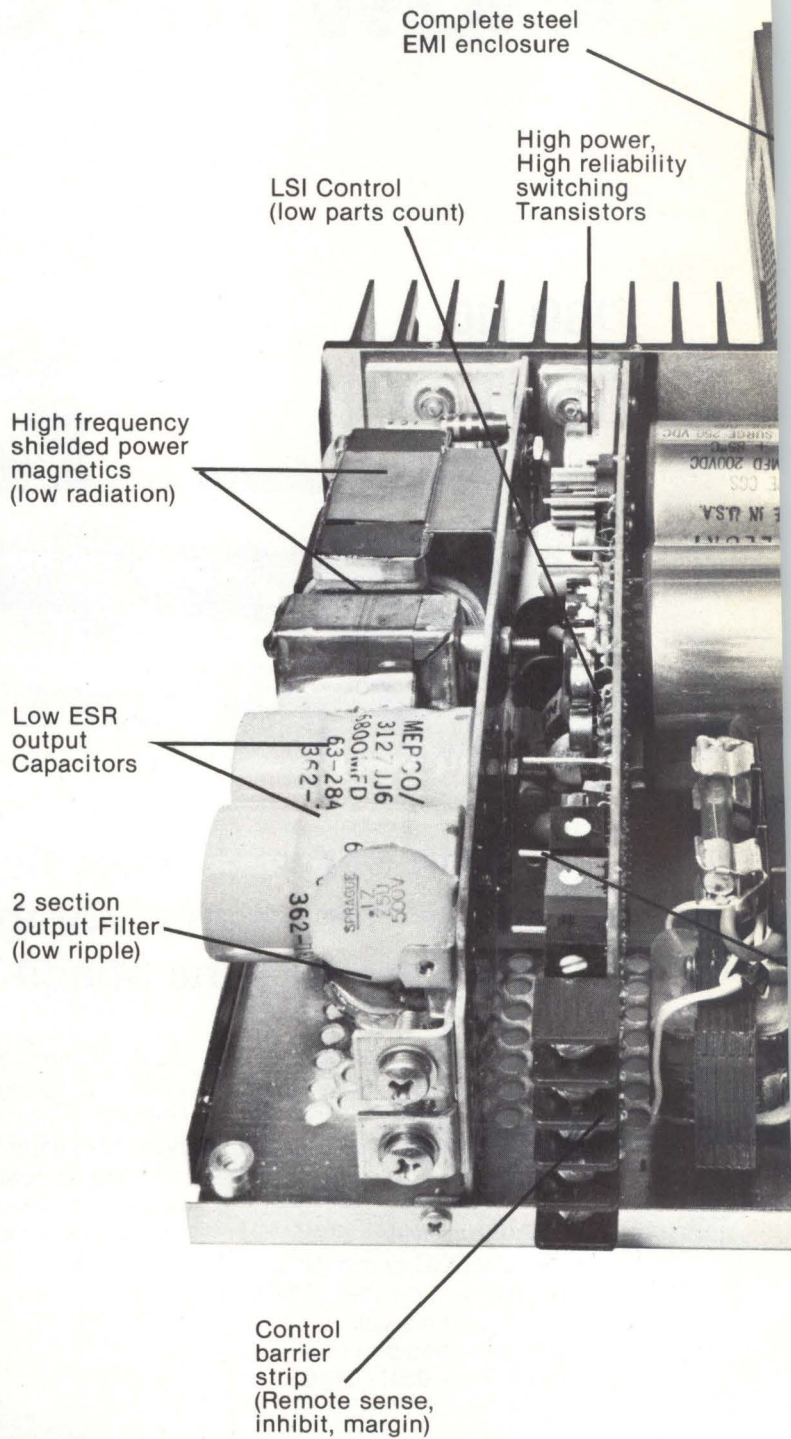
Utilizing the latest technology, the switchers feature soft-start; LSI circuit modulator chip; low ESR capacitors for reduced ripple and noise; and an impressive 40 MSEC *minimum* holdover storage capability. To make sure that they keep on performing way past their 5-year warranty, we subject every unit to a rigorous testing program: 100% component screening; numerous in-process electrical inspections; each module is functionally tested; the complete unit is burned-in for 48 hours at 50°C, and the supply is then computer tested to all its performance specifications.



Output Module

Converter Module

Input Module

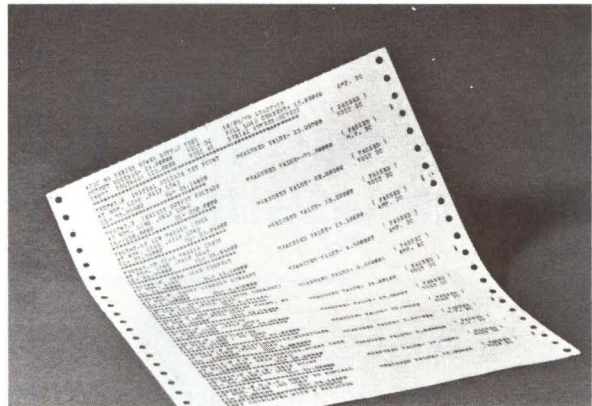


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A 12-page brochure gives complete details including how the series meets the stringent VDE requirements for EMI. Send for it now.

## Models

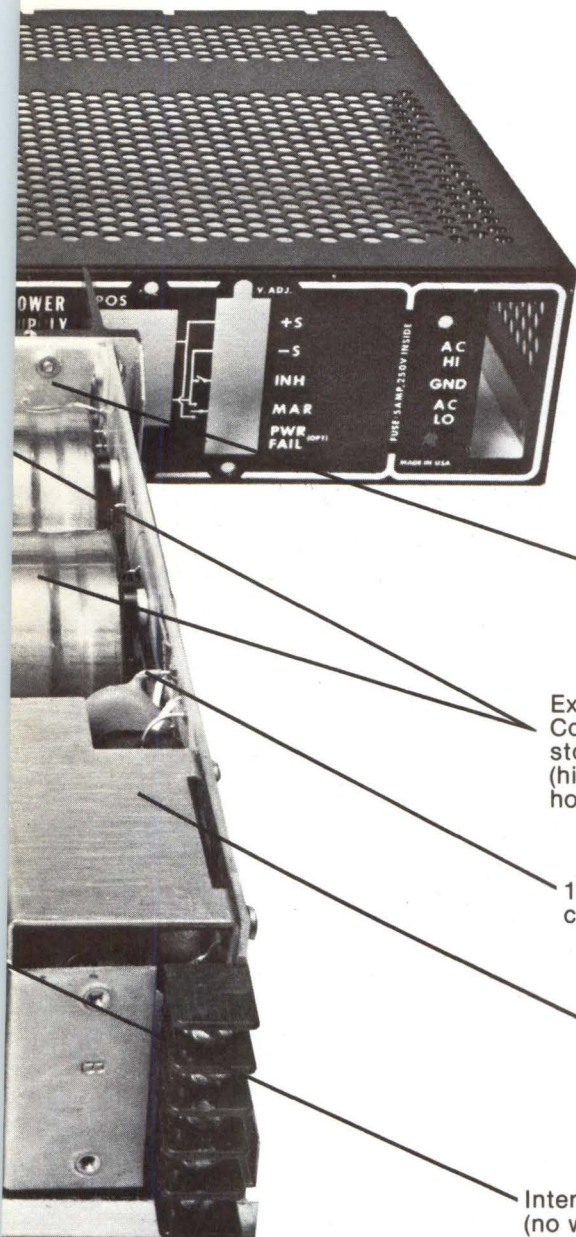
### RS Series - Single Output

CASE SIZE	OUTPUT CHARACTERISTICS	VOLTAGE (ADJUSTABLE ± 5%)				PRICE* (FOR 1-9) \$
		5V	12V	15V	24V	
		M5	MAX. CURRENT AMPS	10.0	4.5	
M10	MAX. CURRENT AMPS	20.0	9.0	7.2	5.0	259
M15	MAX. CURRENT AMPS	30.0	13.5	10.8	7.0	279
M30	MAX. CURRENT AMPS	60.0	27.0	21.0	13.0	395

### RT Series - Triple Output

CASE SIZE	OUTPUT CHARACTERISTICS	VOLTAGE (ADJUSTABLE ± 5%)		PRICE* (FOR 1-9) \$
		5V/12V/12V	5V/15V/15V	
		T10	MAX. CURRENT AMPS	
T15	MAX. CURRENT AMPS	30/5/2	30/4/2	415
T30	MAX. CURRENT AMPS	60/5/5	60/4/4	525

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## INFORMATION SYSTEMS REVIEW— AND EPILOGUE

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**John E. Buckley**

Telecommunications Management Corporation  
Cornwells Heights, Pennsylvania

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In this month's "Communication Channel" is the last in a series of monthly columns that it has been my pleasure to write for *Computer Design*. Since the January 1970 issue I have been able to explore and discuss many of the technologies, applications, and developments of data communications systems through this column.

After nine years of commenting on this dramatic period in the evolution of information systems, I have made the decision to "retire" as an author for "Communication Channel." Appropriately then, this last column reviews developments that we have experienced during this time. I am also taking this opportunity to express acknowledgment and appreciation for the courtesies and cooperation that have been provided me by the staff of *Computer Design* magazine over these years. Most importantly, I want to take this opportunity to bid farewell to my readership. I have had the pleasure of personally meeting many of you in the course of business activities. Such encounters have reinforced my basic conviction that this column has made a positive contribution to the advancement of this technology and its applications.

During these nine years, advancements and developments relative to information systems have been significant. With respect to data transmission rates, the maximum practical limit in 1970 was generally accepted as 2000 bits/s for the switched telephone network and, with caution, 4800 bits/s for a conditioned leased channel. Any references to 7200 bits/s or 9600 bits/s were considered to be in a pioneer category. Today, 9600 bits/s

is not only recognized as a reliable leased channel data rate but is considered practical for the switched telephone network under certain controlled circumstances.

Cost of modems (modulating-demodulating equipment) has been significantly reduced due to the application of new component technology. The typical asynchronous modem operating at 1200 bits/s in 1970 carried a purchase price of \$1500 to \$2000. Today, this same type of data set can be purchased for less than \$1000, with some models as low as \$500.

Remote data communication terminals at the beginning of this decade were primarily batch transmission terminals, operated under control of a central processor for RJE applications. A few such terminals were available with a new concept called a minicomputer as an integral part of the terminal. Such RJE or batch transmission terminals typically demanded a purchase price of over \$25,000 with the majority of the programming control still being resident in the central processor.

Interactive terminals were available as either teletypewriter printing devices or CRT display devices. In both cases, these historic interactive terminals lacked significant flexibility in application or operation. Limited switch settings or internal wiring changes were the typical means of providing some application adaptability. With such primitive terminals, it was obvious that all processing and control decisions had to be resident in a centralized processing complex. Major interactive terminal differences were whether the terminal was buffered (CRT only) and



Our new line of 80-column, dot-matrix line printers – the Anadex DP-8000 Series – combines high performance and operating convenience with a price that's causing OEM's to take a closer look.

#### Looking for Performance?

All models feature a precision engineered, continuous duty printer mechanism that can print the complete 96 ASCII character set, bi-directionally, at 84 LPM actual throughout. And three lines of internal FIFO buffer storage (optionally, 2K character FIFO buffer for CRT dump, etc.) allow faster external system operation.

A 9 x 7 character font provides virtually half-dot resolution for superior print quality.

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Precise positioning of single or multiple-part paper is ensured by sprocket-feed paper advance, user-programmable Top of Form Control, and up to 8 Vertical Tabs.

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#### Looking for Low Cost?

The best news is the price. A complete DP-8000, including case, is priced under \$600 in OEM quantities.

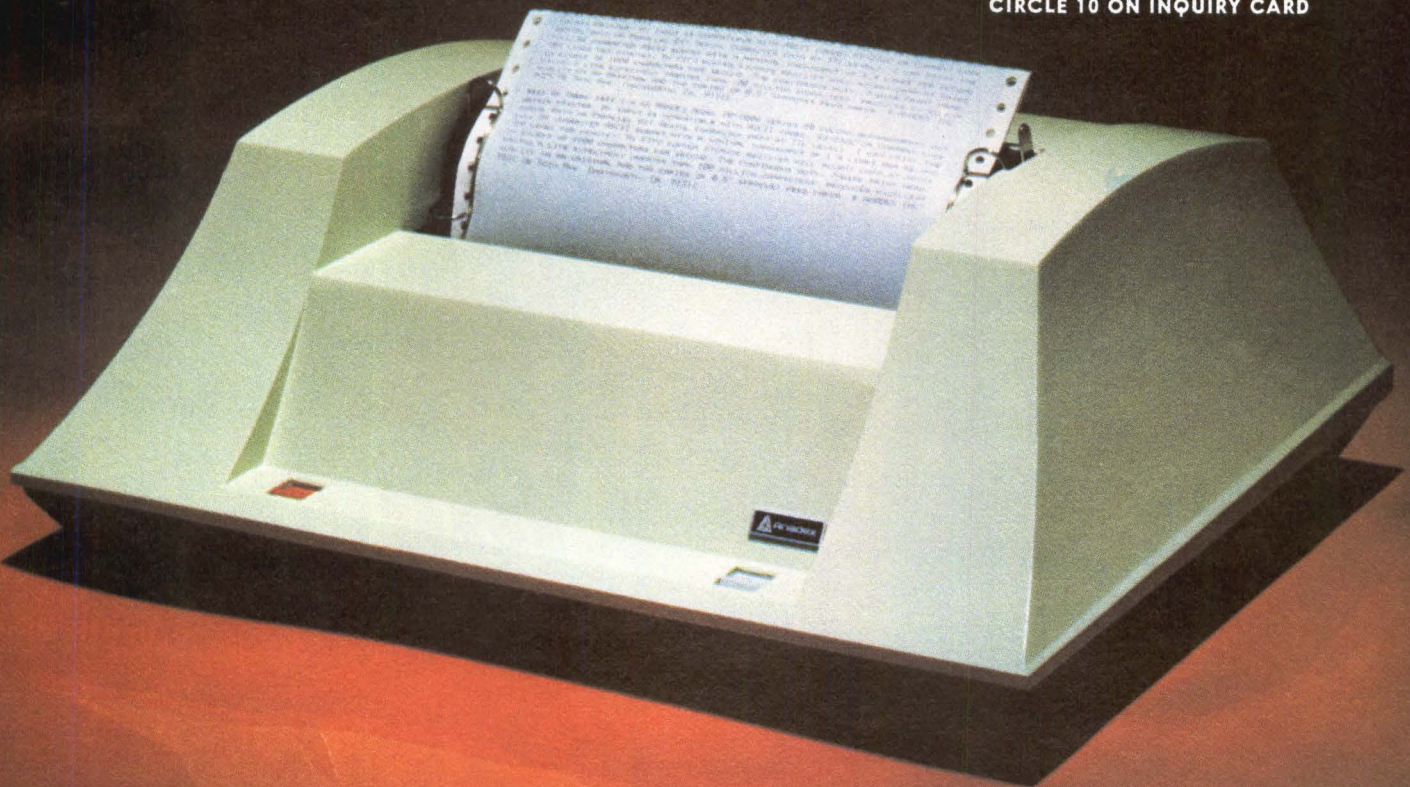
Once you've examined the specifications and seen the printer in operation, we think you'll agree, "Printer Price/Performance never looked better."

# Printer Price/Performance never looked better.

For complete details, contact DP-8000 Marketing Dept.; Anadex, Inc.; 9825 DeSoto Ave.; Chatsworth, CA 91311; Phone (213) 998-8010; TWX 910-494-2761.

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CIRCLE 10 ON INQUIRY CARD



# THINK

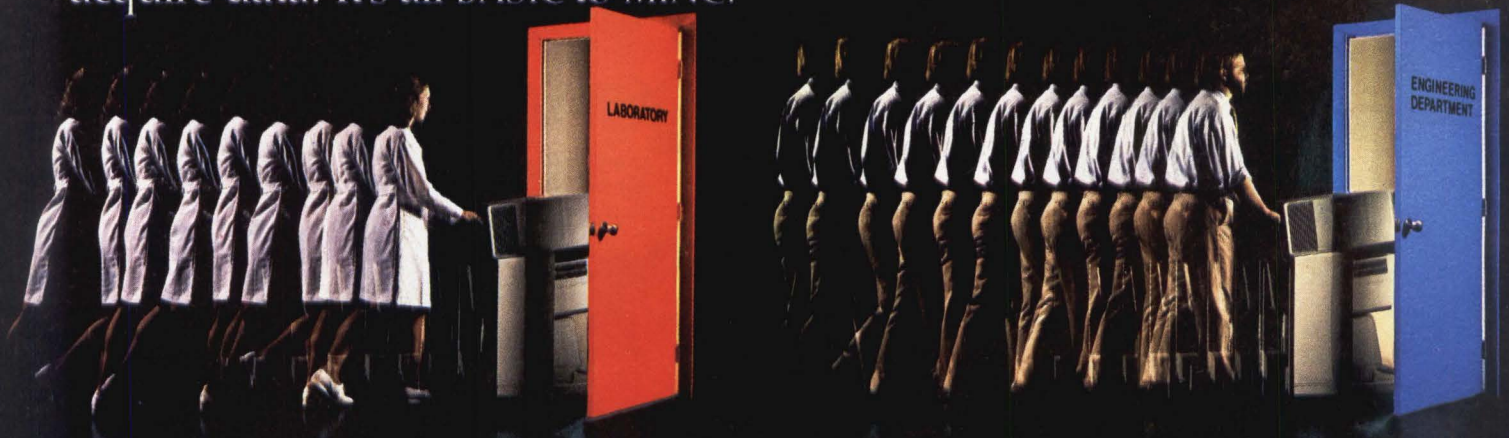
The easy-to-use, BASIC, scientific and engineering computer you buy on a calculator budget.



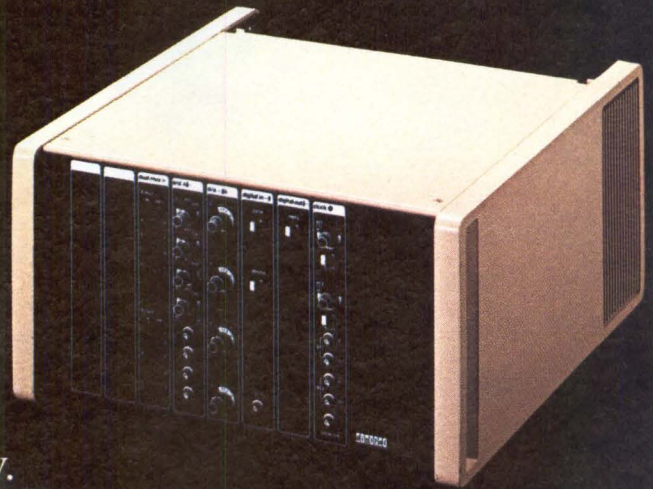
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CIRCLE 11 ON INQUIRY CARD

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therefore would permit some local screen editing, or whether the terminal had a direct keyboard entry so that the terminal's output device (printer or display) was merely a monitor of the data exchange with the central computer center.

Today's interactive terminals are, in many cases, complete programmable processing elements with the application of the microprocessor and semiconductor memory elements (RAM, P/ROM, EPROM, etc). In most interactive applications, data control and data manipulation is performed totally by the interactive terminal with the central processor being involved only with exception or conclusion data. This transfer to distributive processing has not only improved the processing efficiency of the central processor but also reduced the data transmission volume. Since actual data exchange now takes place on an exception and scheduled basis, the sensitivity of the application to transient communications channel permutations has been significantly reduced.

In the area of data memories, the traditional magnetic core arrays or early semiconductor memories have significantly evolved. This memory evolution, coupled with the advent of the microprocessor, has had the most profound influence in reshaping the concepts of information processing systems. Low cost data storage has moved from traditional serial data media such as magnetic tape to the low cost random memories of the floppy disk. Those who can clearly remember the application concepts of 1970 will recall that the punched card was still king. Today a punched card is viewed with reverent interest as one would normally consider other evidences of our antiquity.

Data network options have also emerged as one of the most significant developments of this period, eg, packet switching, digital transmission as well as the alternative analog channels from the specialized communications common carriers. The future growth and development of information systems will be heavily influenced during the remainder of this century by these new data network services. The trend in data networks is toward a total digital environment, providing the information system user a communications medium compatible with the signal characteristics of digital processing. The future of modulating-demodulating equipment required for the traditional analog transmission channels can be expected to diminish in future information systems. In this same context, we have witnessed the commercialization of satellite-derived channels. These facilities have not only contributed to the lower cost of communications but have improved inherent data transmission reliability by orders of magnitude. The 1980s promise a considerably wider use of these satellite-derived facilities on a domestic scale. Such facilities will typically be offered as digital transmission channels with respect to the end user's interface.

Two of the most significant developments of the 1970s have been the maturation of the communications regulatory attitude and the application of microprocessor technology. These occurrences were only in their embryonic state as of January 1970. Today, they exert the greatest influence on advancements being experienced as well as anticipated in the evolution of information system applications. In January 1970, the landmark decision of the FCC in the Carterfone case was slightly more than one year old. Most participants in the telecommunications industries could only speculate on the ultimate ramifications of that decree. The traditional communications common carriers were bemoaning the ultimate collapse of the public telecommunications system due to this permitted intrusion of destructive products and practices by unscrupulous and uninformed private sources. At the other extreme

of this emotional spectrum, technically liberal advocates were acclaiming the dawn of new application freedoms and the elimination of utility suppression.

Over the past nine years we have fortunately seen the emergence of responsible practices from these joint users of the public telecommunications system. The introduction of responsible competition in both the equipment and facility domains has resulted in better values in communications services and products being available to the information system user community. Today, there are still vestiges of the old animosities. These prejudices will fade from practice as the regulatory philosophy continues to change from directing to guiding the telecommunications industries. The 1970s can be characterized as a containment of the large communications utilities while emerging competitive entities gained viable positions. The next decade will tend to evidence a liberalization of the restrictions that are presently imposed on the larger utilities, such as the AT&T Consent Decree.

In the technological arena, the advent of the microprocessor and its peripheral technologies has achieved the economic objectives necessary to permit the realization of truly distributive information. The majority of the older information systems were actually manifestations of design compromises. Traditional costs of computational and data storage capabilities relegated these functions to larger processing environments. In a number of applications, these constraints were accepted as absolutes with no encouragement to re-analyze basic design premises. Microprocessor concepts have stimulated a total re-examination of these previously accepted absolutes. The results can be seen throughout today's information systems and will continue to provide lower cost and more adaptive telecommunications equipment and systems.

My contributions to "Communication Channel" have been made during this period of evolution and advancement. At its inception a majority of data processing personnel had little awareness or understanding of data communications. Today, virtually every computer system has a telecommunications aspect, and its associated personnel have at least a comfortable conversational understanding of the physics and applications of data communications. During these dynamic nine years the user community has matured as well as the technology. I trust that "Communication Channel" had at least a small part in contributing to this maturity.

I have always adhered to the philosophy that the basic laws of physics do not change. There are certain absolute relationships among the principles involved in data communications. For example, the signal propagation time on a satellite channel is longer than that on a terrestrial channel because of the speed of light. This relationship will remain valid until the speed of light is changed. Therefore a thorough understanding of the applicable physics of a data communications aspect will always provide the ability to properly evaluate that aspect. The only major difficulty is in maintaining a current glossary and/or syllabus of the terms and colloquialisms that manufacturers continually apply to the same basic concepts and techniques. We are now entering an era in which applications will dominate. The necessary innovative developments have occurred during the 1970s. A basic understanding of the physical principles involved will enable anyone to effectively evolve with this technology.

It is with a twinge of nostalgia that I conclude nine years of unidirectional conversation with my unseen readers. Many thanks and best wishes to my friends at *Computer Design* and most importantly, best wishes and success to each of you during this holiday season and during the infinite seasons to come.



# TWELVE REASONS WHY THE L135 IS THE MOST PRODUCTIVE LSI BOARD TEST SYSTEM YOU CAN OWN.

To compare productivity in LSI board testers, take their three common operations: diagnosing, testing, and programming. Now, to each operation apply the basic measures of productivity: cost, throughput, and quality of testing.

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*The L135 has the highest diagnostic throughput, the lowest operating cost. No other test system comes even close.*

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## 1. The L135 finds bad LSI devices on long buses.

*The Electronic Knife does it.* It takes just a few more probes after regular guided probing finds the failing bus. Without the Electronic Knife, you're faced with trial and error replacement of LSI chips. Or skilled technicians tying up the system for an hour or more per bad IC.

## 2. The L135 makes fewer diagnostic probes – by an order of magnitude.

*State-sensitive trace does it.* Most LSI boards are loaded with multi-input LSI chips linked through “wired-and” bidirectional buses. These often require hundreds of diagnostic probes per fault. State-sensitive trace cuts the number dramatically.

## 3. The L135 produces immediate probe commands.

*The on-line circuit model with a large random-access memory does it.* With circuit structure immediately accessible, the operator does not wait for commands between probes. Other test systems that use fault dictionaries often delay each command several seconds, adding minutes to each diagnosis.

## 4. The L135 mechanizes probing.

*The M150 Automatic Prober does it.* Seven to ten times faster than a human operator, the M150 speeds up board diagnosis even more because its operation is both error-free and fatigue-free.

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*The L135 delivers the highest quality of testing, thereby slashing costs for diagnosis later at systems test and service out in the field.*

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## **5. The L135 emulates LSI-board operating environments.**

*5-MHz clock-rate testing does it.* To ensure adequate board quality, you usually have to run LSI boards at clock rates as the last step in testing. Only the L135 provides test rates of up to 5-MHz, the speed of many microprocessors seen in today's products.

## **6. The L135 emulates and tests CPU sets.**

*Multiple drive/compare phase control does it.* During clock-rate testing, the test system must first replace the CPU set and then test it at speed. The associated microprocessors usually receive multi-phase inputs and generate multi-phase outputs. The L135 provides the necessary, easy-to-program, precise phase controls over driver inputs and comparator strobing.

## **7. The L135 tests and diagnoses analog circuits.**

*Integrated ac-dc-parametric capability does it.* The L135 offers many analog force-and-measure functions through matrix connections, all completely integrated into system hardware and software. If these capabilities aren't integrated into the test system, they must often be added to accommodate the increasing analog content of LSI boards. That prolongs test time and slows diagnosis considerably.

## **8. The L135 tests at dc and clock-rate on the same channel.**

*All-speed pin compatibility does it.* In clock-rate testing, high-speed tests are usually applied on the same pins tested earlier with dc. The L135 allows you to apply both types of tests at the same system channel, eliminating the need for awkward switching or extra channel capacity.

## **9. The L135 has enough clock-rate channel capacity for the big jobs.**

*444 I/O pins does it.* Big LSI boards have upwards of 250 edge-connector pins, all active. In addition, you need simultaneous access to dozens of internal test points and devices invisible to the edge connector. The L135 offers the highest clock-rate channel capacity, enough for all foreseeable LSI boards.

## **10. The L135 cuts total programming time.**

*The P400 Automatic Test Generation System does it.* The P400 automatically generates all the dc patterns and diagnostic data for the toughest part of most LSI boards: the jungle of random digital logic, as well as those portions containing modeled LSI devices. Total programming time is shorter. The best of the so-called "automated test generation" techniques offered by other systems still require manual pattern-writing. That takes longer and costs much more.

---

*The L135 cuts the time needed to get products into the production line and out to the market place.*

---

## **11. The L135 cuts system time for debugging.**

*Immediate-response debug software does it.* During test-plan debugging, the L135 responds to the test engineer's commands and displays results immediately. Total debugging time is cut to a fraction because the test engineer is not distracted by system delays; he can concentrate on his circuit and his test plan.

## **12. The L135 readily assembles the many parts of LSI test plans.**

*Structure-merge programming does it.* Test plans originate in many places: manual patterns and circuit models, learned data from known good boards, circuit and device simulators, automatic pattern generators, etc. The L135's structure-merge software and its straightforward protocol assembles them all into a coherent package, saving your engineers hours of tedious and costly work.

For more information on these and other L135 features, write Teradyne, Inc., 183 Essex Street, Boston, Massachusetts 02111.

The logo for Teradyne, featuring the word "TERADYNE" in a bold, blue, stylized font with a white outline. The letters are blocky and have a slight shadow effect.

## Single-Board Intelligent Controller Performs Communications Tasks

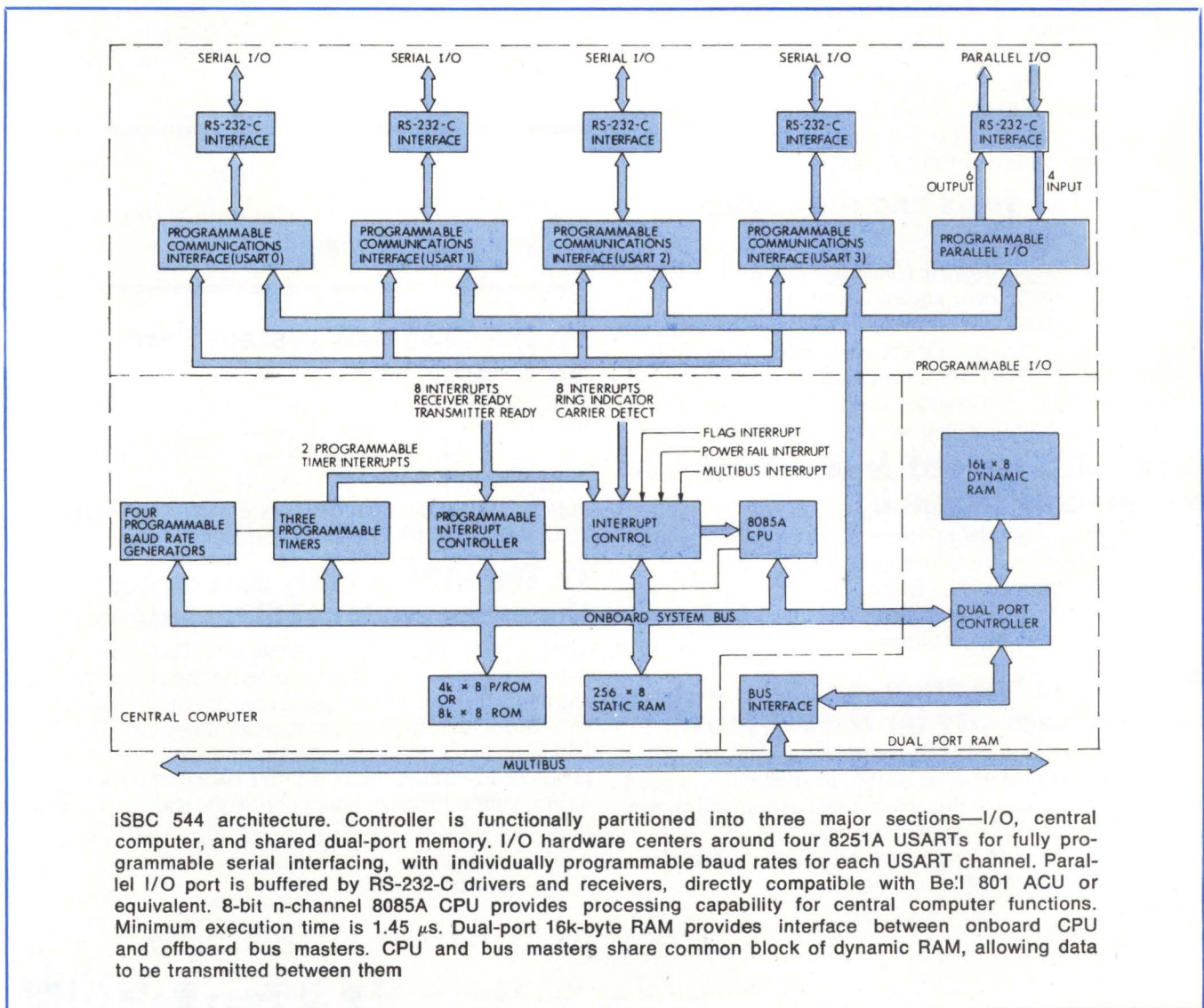
Intelligent communications controller isbc544™, combining microcomputer, memory, and multichannel capabilities, is a complete 8-bit computer system assembled on a 6.75 x 12" (17.1 x 30.5-cm) PC board. MULTIBUS™ compatible, it contains 4 programmable synchronous/asynchronous serial i/o channels, 8085A microprocessor, 16k-byte dual-port dynamic read/write memory, sockets for up to 8k-bytes of ROM, 10 programmable parallel i/o lines compatible with the Bell 801 automatic calling unit (ACU), 4 programmable baud rate generators, 3 independent programmable interval timers/counters, 12 levels programmable interrupt control, and extended

system bus addressing for access in partitioning a 1M-byte address space. Developed by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, the board can operate either as a standalone communications computer or as an intelligent slave to additional SBCs.

In the standalone configuration, the unit can be programmed as an intelligent controller for a group of "dumb" terminals and provide data link control and data buffering to each terminal. In addition, it can handle code conversions and interterminal protocols. Memory and i/o can be expanded and functions added using compatible expansion boards.

As an intelligent slave, onboard processing and dual-port memory capabilities allow the unit to offload communications-related tasks from the master processor and locally control them without accessing the system bus. Such operations include serial data accumulation, error checking, and protocol management.

With the isbc 544, equipment manufacturers can dedicate communications tasks, usually requiring subsystems containing several conventional logic boards, to a single-board intelligent controller. Applications range from communications functions such as concentrators and message switches to terminal and industrial controllers.



isbc 544 architecture. Controller is functionally partitioned into three major sections—I/O, central computer, and shared dual-port memory. I/O hardware centers around four 8251A USARTs for fully programmable serial interfacing, with individually programmable baud rates for each USART channel. Parallel I/O port is buffered by RS-232-C drivers and receivers, directly compatible with Bell 801 ACU or equivalent. 8-bit n-channel 8085A CPU provides processing capability for central computer functions. Minimum execution time is 1.45 μs. Dual-port 16k-byte RAM provides interface between onboard CPU and offboard bus masters. CPU and bus masters share common block of dynamic RAM, allowing data to be transmitted between them

Circle 400 on Inquiry Card

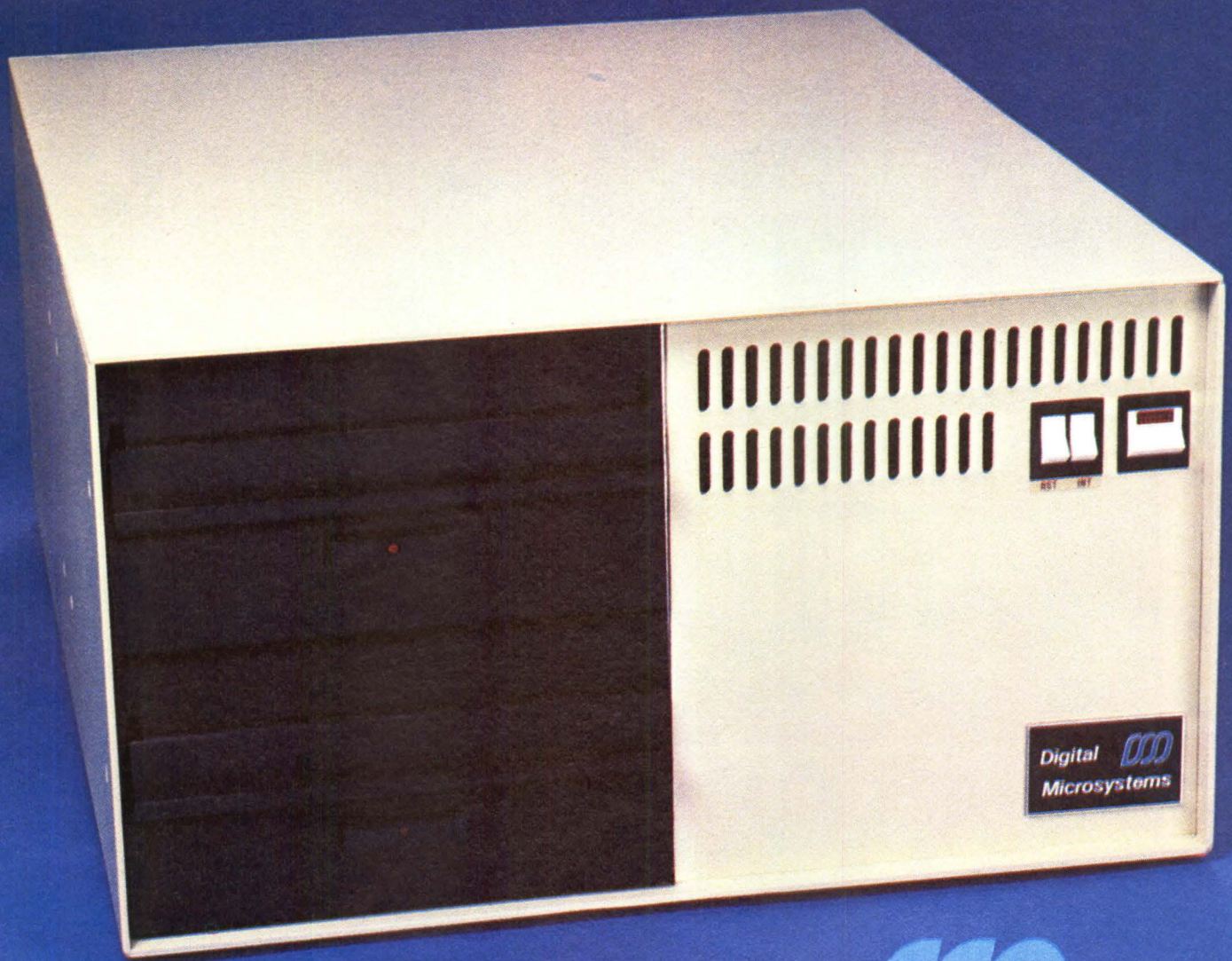


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# Never-Say-Die supply!

## Now you have reliability that won't melt away.

Motorola's new, ICEMAN switching power supplies offer simple, efficient, protected performance.

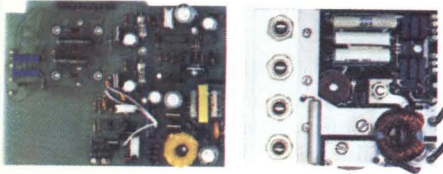
Just like our line of ICEMAN linear supplies, long-term reliability in a switcher begins with how it's made.

Fewer components mean fewer connections, less wiring, reduced failure points and modes.

That was our design goal . . . to make a switcher so simple, so reliable, it would unquestionably be the outstanding example of high-quality, state-of-the-art design.

By actual count, this Motorola PSN1801 switcher contains only 143 electrical parts—about 25% less than the nearest comparable. It employs only 22 wires . . . others have 200 or more. It uses just one connector. Some use as many as 20.

### Two boards and MTBF.



There's more protective circuitry, in less space, in a Motorola ICEMAN switcher than anyone else offers.

Just two circuit boards do it all.

The control board measures only 24" square and contains the latest



400 W, PSN1801, Single-Output ICEMAN Switching Power Supply

multiple-function ICs in place of dozens of discrete parts. The board furnishes remote turn-on/turn-off, overcurrent and short-circuit protection, soft-start to limit overshoot voltage, automatic reset of OVP, primary current limit and capacitor bleed-off circuits.

The 18" square main output board combines OVP, soft-start for inrush current limiting and all output supply components.

ICEMAN switchers are head-and-shoulders above others in shrugging off faults, transients and fatigue.

### ICEMAN keeps his cool.

All the way through. Longer. More efficiently.

Our conservative guardbanding and hefty heat sinking provide unequalled efficiency.

Four paralleled, 60 A, high-temperature Switchmode\* Schottkys, with a maximum of 120 A capability, are used to achieve the 5 V, 80 A output. In other words, they're run at just 67% of total capability. And the Schottkys and the low-sat, high-speed Switchmode power transistors run at no more than 65% and 60%, respectively, of maximum rated junction temperatures, minimizing thermal stress.

The heat sinking is up to 100% thicker than others ensuring even thermal gradients with all the heat quickly going where it's supposed to go . . . out. We've even special-wound the transformer to cut losses.

### Specifications

- PSN1801, 5 V/80 A
- PSD1802, 5 V/60 A, 12 V/8 A
- PST1803, 5 V/60 A, 12 V/4 A, 12 V/4 A

**Input.** 90-130 Vac/180-260 Vac (Selectable), 45-440 Hz Single Phase

**Output.** Floating, isolated from each other and from ground, 600 Vdc max

**Regulation.** Line:  $\pm 0.1\%$  Output, for 90-130 or 180-260 Vac. Load:  $\pm 0.1\%$  Output, no load to full load

**Ripple and Noise.** Less than 10 mV RMS, 50 mV p-p, as measured, with 50 MHz scope

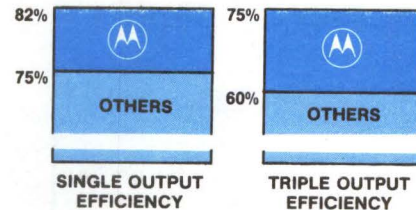
**Temp. Coefficient.** Less than 0.2%/°C

**Switching Frequency.** 25 kHz (Pulse width modulated)

**Transient Response.** 500  $\mu$ s to within 1% after a 25% load change at 5 A/ $\mu$ s, main output

The standard warranty period for all Motorola linear and switching power supplies is 1 year.

Whatever temperature you run an ICEMAN at, your pedal won't be to the metal.



Motorola switchers are designed to meet not only our own high standards but those who set the industry's: VDE 0875/7.71 Curve N and all FCC requirements for EMI plus UL standards for electronic data processing equipment.

You also get minimum 30 ms hold-up time so the regulated 5 V supply is retained after interruption under full load.

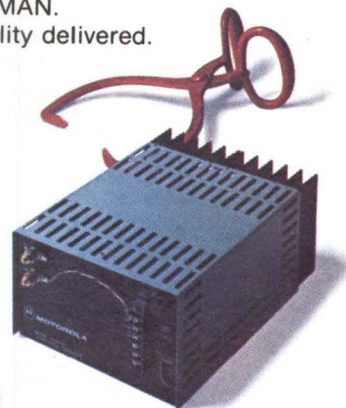
### Cost is cool, too.

Go to any other source for a design of this kind and you'll probably pay substantially more. But Motorola switchers are priced right on the button with units of lesser wattage and quality so you know an ICEMAN saves you cold, hard cash right from the start.

Prices for the three models range from \$495 to \$625, 1 to 9 quantity.

Contact Motorola Subsystem Products, P.O. Box 20912, Phoenix, AZ 85036, (602) 244-3103 or your authorized Subsystem distributor or representative for more information.

ICEMAN.  
Quality delivered.



\*Trademark of Motorola Inc.

**MOTOROLA INC.**

## Network Processor Handles Asynchronous Data Streams

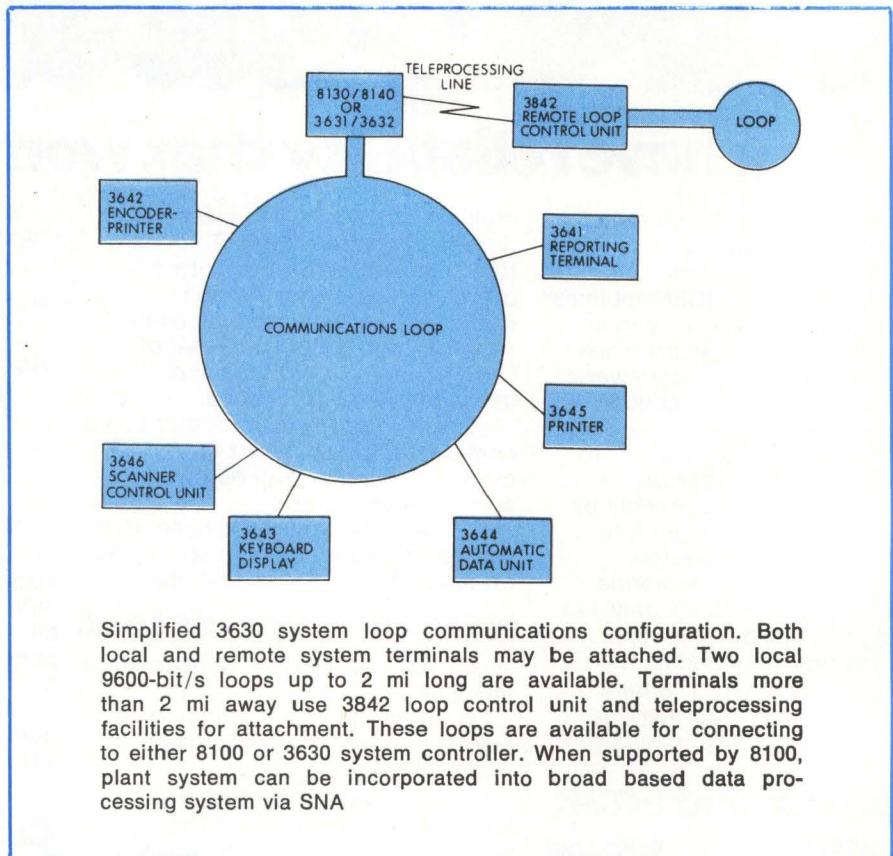


6010 intelligent network processor provides data management functions at nodes of communication network. Standard hardware includes processor/controller, nest to accommodate 30 port channels, and high speed interface

Dual microprocessor based 6010 Intelligent Network Processor™ (INP) combines information from up to 30 asynchronous devices using statistical concentration techniques, thereby reducing requirements for multiple lines and associated data communications equipment. It is the latest addition to the 6000 series INPs from Codex Corp, 20 Cabot Blvd, Mansfield, MA 02048. The 6010 may be used with a variety of terminal types in either dedicated or dial-up arrangement at standard data rates up to 1200 bits/s, with high speed line rates up to 9600 bits/s. CCITT x.25 level 2 compatible full-duplex link protocol provides error protection, and online diagnostic routines are executed as a background function. The unit has the capability for centralized network control and monitoring from either end of a 6010 link. Information collected related to system performance includes terminal char error rate, trunk error rate, free buffers (available data storage), and traffic density. RS-232-C, current loop, and MIL-STD-188C terminal port modules are available. The unit is applicable in point-to-point networks, as a feeder to a 6030/6040 network, or directly attached to a single port on a communications frontend processor. Circle 401 on Inquiry Card

## Interactive Communication System Improves Plant Productivity

Interactive terminal based 3630 plant communication system is a family of



Simplified 3630 system loop communications configuration. Both local and remote system terminals may be attached. Two local 9600-bit/s loops up to 2 mi long are available. Terminals more than 2 mi away use 3842 loop control unit and teleprocessing facilities for attachment. These loops are available for connecting to either 8100 or 3630 system controller. When supported by 8100, plant system can be incorporated into broad based data processing system via SNA

data input and output devices designed for operation in industrial environments. Supported by the 8100 Information System\* and by System/370 Processors, it collects such current data as material movement, status of work in progress, and employee activity, and distributes it to wherever it is needed. The plant system's 3640-series terminals, supported by the 8100, can also be programmed to intermix with general purpose terminals for distributed processing functions. The system, introduced on a limited basis during the past year by IBM Corp, 1133 Westchester Ave, White Plains, NY 10604, is now generally available.

System 3630 includes the following devices: 3631 and 3632 programmable controllers, to coordinate communications between system terminals and 8100 or System/370 processors; models 1 and 2, 3641 reporting terminal, work stations having 22-char alphanumeric display and 35-key numeric or 70-key alphanumeric keyboards respectively; models 1 and 2, 3642 mag stripe encoder-printers; 3643 interactive keyboard, gas-panel display terminals, (models 2, 3, and 4) with 240-, 480-, and 1024-char displays respectively; 3644 automatic

data unit, acquisition and distribution device combining analog and digital I/O capabilities; 3645 document printer; 3646 scanner control unit, a work station terminal that can accommodate up to 4 mag readers; and both handheld mag scanners and slot readers.

Circle 402 on Inquiry Card

## Key Management Devices Expand Data Encryption Capabilities

A key generator and key loader have been added to the Info-guard™ series of data security products by Motorola, Government Electronics Div, 8201 E McDowell Rd, Scottsdale, AZ 85252. DES4100KGM key generator randomly generates, stores, and provides operator control over keys used to encrypt computer information without human knowledge of the keys. Each protected line in an encrypted data communications network has an associated unit number and address under which encrypted keys are stored in the generator's nonvolatile memory.

\*Computer Design, Dec 1978, p 42, 47

# Flicker-free and ultrahigh resolution color TV displays...

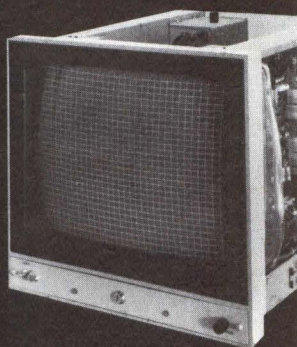
You can have your choice with the Model 374.

1024 x 512 pixel graphics displayed at a non-flicker, 60-Hz refresh rate. Ideal for the display of computer graphics.

OR

1024 x 1024 ultrahigh resolution pixel graphics displayed at a 30-Hz rate using 2:1 interlace. Video bandwidth in excess of 30 MHz assures that resolution is not electronically limited.

Write or call Dick Holmes for a Model 374 descriptive brochure.



## Electronic Image Systems

Division of Systems Research Laboratories, Inc.  
2800 Indian Ripple Road • Dayton, Ohio 45440  
Phone 513/426-6000 • TWX 810/450-8621

CIRCLE 16 ON INQUIRY CARD

## COMMUNICATION CHANNEL

An operator designates from a key pad which keys shall be generated for which units, but not the keys themselves. These are produced by the generator, stored in its own control memory, and are inaccessible to the outside.

DES4100KLM key loader is a portable, handheld intelligent micro-processor based unit capable of storing 32 different keys (256 optional). It is electro-optically interfaced to the key generator and network security module (NSM) via a phototransistor and LED. After keys are loaded into the unit, it is then used to load key data into the appropriate local or remote NSMs, where, through another optical interface, it will transfer new key information. Tampering with key loader or interfacing it to an unauthorized NSM will activate switches cutting off power and destroying all keys within the loader.

All Info-guard products use the NBS data encryption standard algorithm, which is public. Therefore security lies in the keys and key management, and not in the secrecy of the algorithm.

Circle 403 on Inquiry Card

## Software System Aids Volume Transaction Processing

TRAN-PRO (transaction processing) system is a software package designed to facilitate the development of online communications networks in applications where a large number of transactions must be handled. It supports over 200 online terminals, can process more than 10,000 transactions/h, and allows the application programmer with little or no communications experience to become a productive online programmer, according to NCR Corp, Davton, OH 45479.

Intended for operation with either 8000 Criterion or Century series computers, the software can function in a multiprogramming environment. It works with the TOTAL data base management system, allowing user's data to be organized into an integrated comprehensive data base and easing the implementation of online systems. Company spokesmen say that the system can significantly reduce the cost of online system development by performing editing, formatting, and transaction logging functions, as well as by providing user security.

Circle 404 on Inquiry Card

# ICEMAN'S Available

... from these authorized Motorola distributors and representatives. Contact them about any Motorola linear or switching power supply for MPU and other logic-related applications. Or call Motorola Subsystem Products, (602) 244-3103.

### Manufacturers' Representatives

Austin • P.J. Scanlon Co., Inc. ....	(512) 863-2319
Baltimore/	
Washington • Coulbourn DeGreif, Inc. ....	(301) 247-4646
Boston • New England Tech. Sales ..	(617) 272-0434
Cedar Rapids • Dy-Tronix, Inc. ....	(319) 377-8275
Chicago • Sumer Inc. ....	(312) 991-8500
Cleveland • McFadden Sales .....	(216) 381-8070
Columbus • McFadden Sales .....	(614) 459-1280
Dallas • P.J. Scanlon Co., Inc. ....	(214) 231-4661
Dayton • McFadden Sales .....	(614) 877-9934
Denver • Thorson Company .....	(303) 759-0809
Detroit • McFadden Sales .....	(313) 681-7540
Ft. Wayne • McFadden Sales .....	(219) 485-2526
Houston • P.J. Scanlon Co., Inc. ....	(713) 496-1170
Huntsville • Macro-Marketing Assoc. ....	(205) 883-9630
Indianapolis • McFadden Sales .....	(317) 896-5070
Kansas City • Dy-Tronix, Inc. ....	(816) 373-6600
Los Angeles • Ed Landa Company ..	(213) 879-0770
Milwaukee • Sumer Inc. ....	(414) 259-9060
Minneapolis • Comstrand, Inc. ....	(612) 788-9234
New York • HLM Associates .....	(516) 757-1606
New Jersey • HLM Associates .....	(201) 263-1535
Philadelphia • TAI Corp. ....	(215) 627-6615
Phoenix • Summit Sales .....	(602) 994-4587
Rochester • T-Squared .....	(716) 924-9101
Salt Lake • Anderson Associates ..	(801) 292-8991
San Francisco • QuadRep Inc. ....	(408) 733-7300
St. Louis • Dy-Tronix, Inc. ....	(314) 731-5799
St. Petersburg • Tech-Rep .....	(813) 577-2779
Syracuse • T-Squared .....	(315) 463-8592
Winston-Salem • Macro Marketing ..	(919) 768-8740

### Distributors

Baltimore • Pioneer/Washington ...	(301) 948-0710
Boston • Cramer Electronics, Inc. ..	(617) 969-7700
Chicago • Newark Electronics .....	(312) 638-4411
Cleveland • Pioneer/Standard Inc. ...	(216) 587-3600
Columbia • Dixie Electronics Inc. ...	(803) 779-5332
Dallas • Hall-Mark Electronics Corp. ...	(214) 234-7400
Dayton • Pioneer-Standard Inc. ....	(513) 236-9900
Denver • Elmar Electronics .....	(303) 287-9611
Detroit • Pioneer-Standard Inc. ....	(313) 525-1800
Houston • Sterling Electronics .....	(713) 627-9800
Huntsville • Hall-Mark Electronics ..	(205) 837-8700
Indianapolis • Pioneer-Standard Inc. ...	(317) 849-7300
Kansas City, MO • LCOMP KC .....	(816) 221-2400
Los Angeles • Liberty Electronics ..	(213) 986-6850
Minneapolis • Cramer/Minnesota ..	(612) 835-7811
New York • Harrison Radio, Corp. ...	(516) 293-7979
New York • Schweber Electronics ..	(516) 334-7474
Orlando • Hall-Mark Electronics .....	(305) 855-4020
Philadelphia • Philadelphia Elec., Inc. ....	(215) 568-7400
Phoenix • Liberty Electronics .....	(602) 249-2232
Pittsburgh • Pioneer-Standard Inc. ...	(412) 782-2300
Rochester • Cramer/Rochester .....	(716) 275-0300
St. Louis • LCOMP St. Louis, Inc. ....	(314) 291-6200
San Diego • Liberty Electronics .....	(714) 565-9171
San Francisco • Elmar Electronics ..	(415) 961-3611
Seattle • Almac/Stroum Electronics ..	(206) 763-2300
Syracuse • Cramer/Syracuse .....	(315) 437-6671



**MOTOROLA INC.**

## Equipment Approved for Direct Connection to Telephone Network

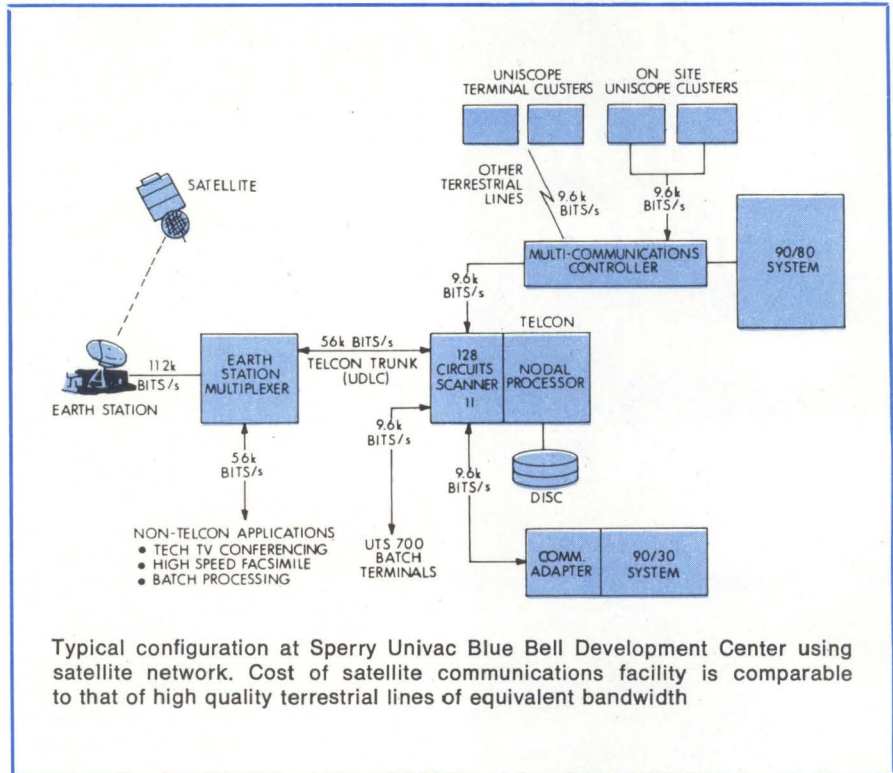
The Federal Communications Commission has granted a complete "fully protected" and "grandfathered" status ("Certification Update," *Computer Design*, July 1978, pp 12-14) to the D1200 family of PBX (public branch exchange) systems from Digital Telephone Systems, Inc, PO Box 1188, Novato, CA 94947. The decision means that nationwide interconnect without interface couplers of past and present D1200 installations is approved as being harmless to the public telephone network. The company, a division of Farinon, Inc, of San Mateo, Calif, had already received similar approval from the California Public Utilities Commission.

Another company granted this certification after meeting requirements in compliance with the newly enacted FCC Rules Regulations, under the terms of the Third Report and Order in Docket 19528, is T-Bar Inc, 141 Danbury Rd, Wilton, CT 06897, manufacturer of online switching and control equipment for data communications applications. Included in the certification are the company's 5700 series analog switches which allow users to switch to backup circuits or to substitute alternate pieces of data communications equipment as faults occur or as tasks change.

## Expansion Planned for Satellite Communications Data Network

A third earth station, located at Salt Lake City, Utah, will be added to its satellite communications network by Sperry Univac, PO Box 500, Blue Bell, PA 19422, in order to allow a more effective evaluation of network parameters. At the present time two earth stations, one at Blue Bell and the other at Roseville, Minn are being used for 2-way data communications via satellite. This is said to be the first such commercially licensed link using all-digital two-way transmission in C band (3.9 to 6.2 GHz with 5-m dia antennas).

Many areas of the company's development and manufacturing operations avail themselves of these data communications links. Large-scale 1100 series systems in Roseville and



Typical configuration at Sperry Univac Blue Bell Development Center using satellite network. Cost of satellite communications facility is comparable to that of high quality terrestrial lines of equivalent bandwidth

series 90 computers in Blue Bell, using the network, provide processing power for various development groups, who access the large computers via computer terminals, minicomputers, and the smaller 90/25 and 90/30 systems. Such projects as hardware design, development of software and applications programs, and exchange of manufacturing and financial information are implemented over the intersite link. Salt Lake City applications will include development of communications subsystems and computer termi-

nals. Sperry's TELCON networking system will be used for these communications activities.

The additional earth station will be installed and operated by American Satellite Corp (ASC), 20300 Century Blvd, Germantown, MD 20767. ASC, using Sperry Univac specifications, designed, installed, and operates the present link which joins the large computer complexes at both sites via its SDX (satellite data exchange) services, using WESTAR, Western Union's domestic satellite.

## Software System Developed for European Data Net Design

The development of a European version of its MIND (Modular Interactive Network Designer) system, called EMIND, has been announced by Network Analysis Corp (NAC), 130 Steamboat Rd, Great Neck, NY 11024. The new version includes a tariff module which reflects British and European private line costs and restraints, enabling users to obtain least-cost layouts for centralized data networks in Great Britain and on the European continent. The basic MIND

version computes cost for U.S. networks based on AT&T's MPL (multi-schedule private line) tariff. Access to both versions is offered on a time-shared basis under a license arrangement.

EMIND is being marketed in Europe and Great Britain by PACTEL, a London based computer and telecommunications consulting organization. Under the terms of a recently announced agreement, NAC and PACTEL have combined to offer clients worldwide capabilities in design, analysis, testing, and implementation of computer and telecommunications networks. □

Circle 405 on Inquiry Card

# Two new ways to add 256K bytes to your PDP-11<sup>®</sup>

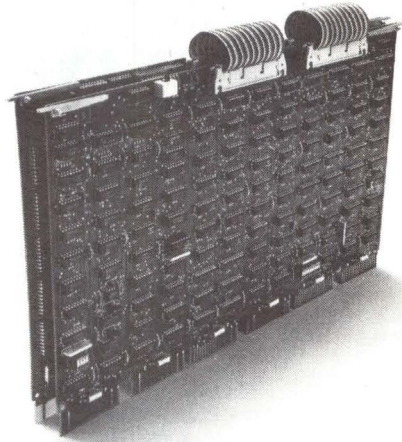


## Their way

When it's available, DEC<sup>®</sup>'s MS11-L<sup>®</sup> will allow you to add 256K bytes of MOS memory to your PDP-11 systems with a single plug-in module. It improves system density and performance while lowering system power consumption and costs.

Great idea, DEC.

®Registered trademark of Digital Equipment Corporation



## The right way

Plessey's PM-S11E does all that and more.

Our S11E consists of 256K bytes of high-speed, state-of-the-art MOS memory for the PDP-11, the first with ECC. Multiple bit errors are detected and single bit errors (dominant with MOS devices) are corrected, for maximum data integrity and a substantially higher MTBF.

The Plessey S11E is fully PDP-11 hardware and software compatible, may be used with parity and non-parity operating systems and presents only one bus load to the Unibus<sup>®</sup>.

And maybe best of all, we're shipping now for \$6,995 (unit quantity).

Providing mini users what they need when they need it at a price they can live with has made us the largest independent supplier of DEC-compatible peripherals. Our product line presently includes add-in/add-on core and semiconductor memories, cartridge disc systems, floppy disc systems, mag tape systems, complete computer-based systems, and a wide variety of backplanes, expansion chassis and other accessories.

We're the only real alternative to DEC, a complete single source. For all the details, please contact the nearest Plessey sales office today.



## Plessey Peripheral Systems

17466 Daimler, Irvine, California 92714, (714) 540-9945

### The only real alternative.

# The Bantam.

## The cocky new \$599\* CRT that just changed the pecking order.

User Need	Feature	P-E BANTAM	LSI ADM-3A	Hazel- tine 1400	Hazel- tine 1500	Adds Regent 100
Easy to read display	7 x 10 matrix for highly legible characters	Yes	No	No	Yes	No
	Black on white or white on black display	Yes	No	No	Yes	Yes
	Display set deep in hood to reduce glare	Yes	No	No	No	No
	Full 24 x 80 display	Yes	Yes	Yes	Yes	Yes
	Full upper and lower case	Yes	Option	No	Yes	Yes
	Non-glare screen	Option	Yes	No	Yes	Yes
High operator throughput, low operator fatigue	Tab stops/tab key	Yes	No	No	Yes	Yes
	Backspace key	Yes	No	No	Yes	Yes
	Repeat key	Yes	Yes	No	No	Yes
	Shiftlock key	Yes	No	No	No	No
	Separate print key	Yes	No	No	No	Yes
Convenient switching Local/on-line	Local—remote key	Yes	No	Option	Option	Yes
International Character sets	French/German/Swedish/Danish/British/Spanish	Option	Option	No	Option	Option
High speed numeric	Integrated numeric pad	Yes	Option	No	Yes	Yes
Convenient system interfacing	RS-232/CCITT-V24	Yes	Yes	Yes	Yes	Yes
	Current loop	Option	Yes	No	Yes	Yes
Simplified program debugging	Transparent mode and displayable control characters	Yes	No	No	No	No
Faster maintenance	Self-test	Yes	No	Yes	No	Yes
Minimum desk space	Small size	15Wx 19Dx 14H	15.5Wx 20.2Dx 13.5H	15.5Wx 20.5Dx 13.5H	15.5Wx 20.5Dx 13.5H	21Wx 23Dx 14.5H
Printer port	Printer port	Option	Yes	No	Yes	Option
Cost effectiveness	Qty. 100 OEM price	\$599†	\$740	Less than \$550 in quantity 1000	\$860	\$895

\*In quantities of 100.  
†Qty. 1, End User Price \$966.



Nobody ever offered you a tough, high quality, compact CRT like the BANTAM before. At \$599 or any price. Designed for hectic office environments. And, human engineered to make an operator's life easier.

**You get everything you need for cleaner input and faster throughput.** An upper and lower case character set displayed on a sharp 7 x 10 dot matrix. A full 24-line by 80-character screen. A complete, sure-touch keyboard with shadow numeric pad.

You get complete tabbing. Full cursor addressing. Repeat, backspace and shiftlock keys. A transparent mode with displayable control characters to simplify host program debugging. And, a self-test mode for easy maintainability.

**And, you get everything your operators need to make their jobs a joy.** A hooded display that cuts glare. A wide bandwidth monitor for sharp images everywhere on the screen. Below-the-line character descenders\* to make reading easier.

A switchable white-on-black or black-on-white display, whichever your operator prefers. An easy-to-find cursor that frames the entire character position in a transparent, inverted video block.

**Plus plenty of options you can't get with CRTs costing much more.** Like our low-cost Pussycat page printer. A full range of foreign language character sets. We even have a model you can switch from ASCII to full overstrike APL.

**But that's not all.** The BANTAM's compact good looks fit any decor. It's handsome enough for executive row and rugged enough for the stockroom. Silent? The BANTAM's fan-free design makes it quieter than an electric typewriter. And, the BANTAM only weighs 28 pounds.

**Only an industry leader like Perkin-Elmer could do it.** We designed a powerful, custom LSI controller chip that makes the BANTAM the one and only high quality CRT in its class.

But see for yourself. Use the comparison chart. Learn why we're so proud to add this \$599 CRT to the 250,000 peripherals that bear our good name.

And, remember our terminals come equipped with a No Hassle, 800 toll-free service phone number.

**One call does it all.** We give you service *where* you need it, when you need it. We're there. Not just "worldwide," but wherever you are.

For more information call or write Perkin-Elmer Terminals Division, Randolph Park West, Route 10 & Emery Avenue, Randolph, N.J. 07801 (201) 366-5550. Or contact any of our sales offices. Then watch the feathers fly.

## The Bantam's available at all these places

### PERKIN-ELMER SALES OFFICES

Santa Clara, CA (408) 249-5540.

Tustin, CA (714) 544-9093.

Atlanta, GA (404) 393-8440.

Arlington Heights, IL (312) 437-3547.

Waltham, MA (617) 890-1305.

Oceanport, NJ (201) 229-4471.

McLean, VA (703) 827-5900.

Singapore, Republic of  
Singapore 2200949

Sydney (North Ryde), Australia  
887-1000.

Toronto (Mississauga), Canada  
(416) 677-8990.

Slough, England 753-34511.

Paris, France 664-1858.

Munich, Germany 089-753081.

Schiphol-Oost,

The Netherlands 020-458-269.

### PERKIN-ELMER SERVICE CENTERS

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NJ; West Long Branch, NJ;

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OH; Dayton, OH; Englewood

Cliffs, NJ; Detroit, MI;

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MN; Kansas City, KS; Tulsa,

OK; Dallas, TX; Houston, TX;

Denver, CO; Phoenix, AZ;

Seattle, WA; San Francisco,

CA; Los Angeles, CA;

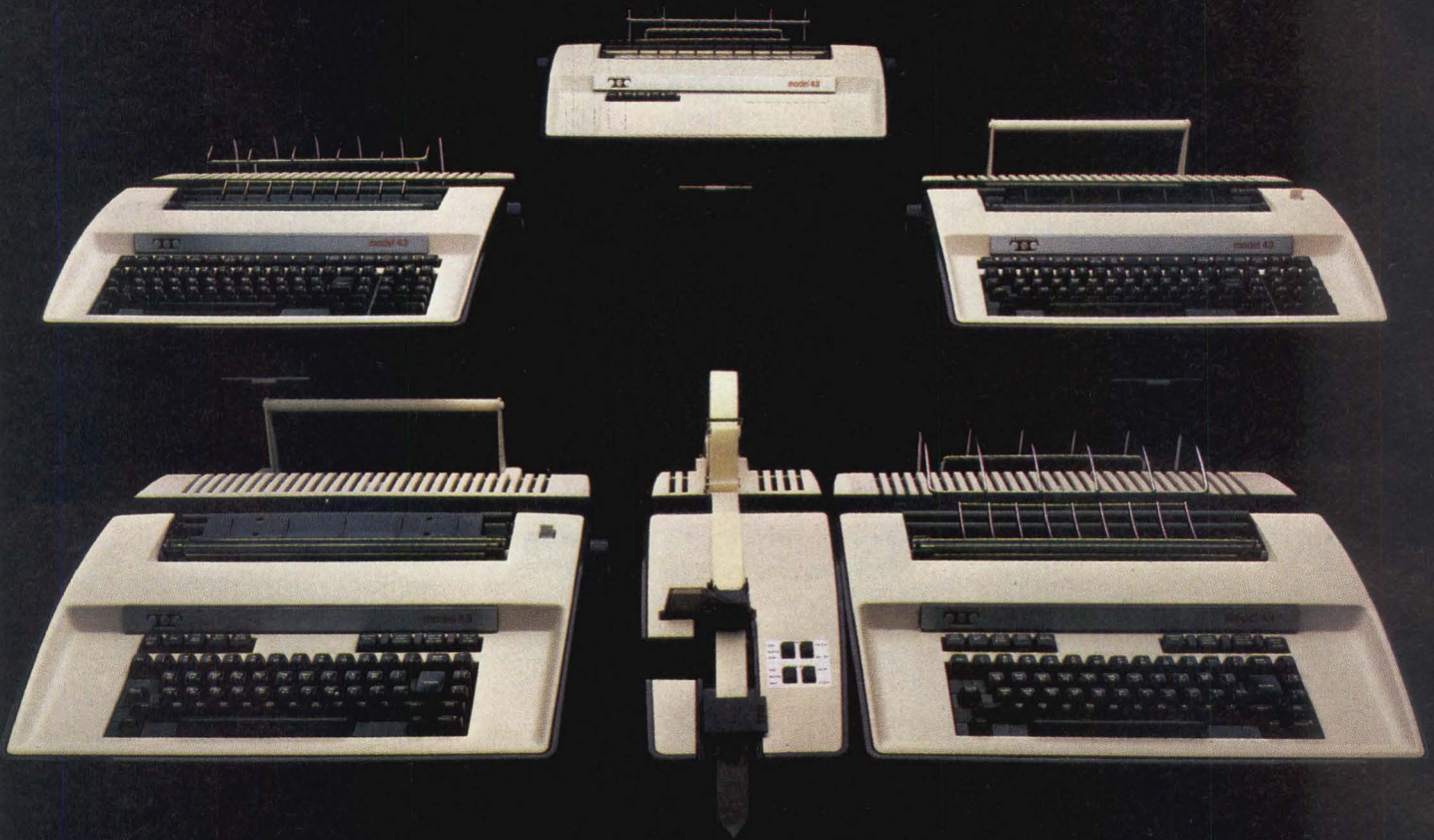
Orange County, CA; San

Diego, CA.

## PERKIN-ELMER

Data Systems





## OUR MODEL 43 TELEPRINTER FAMILY IS THE BEGINNING OF A NEW LEGEND.

When we introduced it just a year ago, the basic idea behind the Teletype\* model 43 proved so sound and flexible that today it's grown into a comprehensive terminal family with extensive capabilities for message communications.

Model 43's come in a variety of configurations with either 80 column friction-feed or 132 column pin-feed printers. Some units are designed for use on the switched network, others for point-to-point private-line systems. (There's also a new generation of 5-level buffered teleprinters for Telex applications.)

The basic model 43 series operates on-line at 10 or 30 cps in either the half- or full-duplex mode and prints multiple copies using the 96 character ASCII code set. A wide choice of interfaces, including EIA RS232C and DC 20-60ma, are available for easy system integration.

With the automatic send-receive configuration, messages can be prepared off-line via the paper tape punch, edited, combined with

a master tape, then sent at maximum terminal speed—automatically and unattended—when line rates are lowest.

Buffered 43's operate on-line at speeds ranging from 10 to 180 cps and provide up to 20,000 characters of storage for sending, receiving and editing. These terminals send and receive automatically via the buffer while messages are simultaneously being prepared for future transmission. They also include full forms control, the automatic answer capability and answer back.

Just like its predecessor, the legendary model 33, our model 43 family is designed for extreme reliability. The reason is simple: simplicity. Our model 43's use only five major pluggable components (six, counting the paper tape module on the ASR), along with extensive use of LSI circuitry.

So when you think of our model 43 family, think of it as the beginning of a new legend.



### THE TELETYPE MODEL 43 FAMILY.

Teletype Corporation, 5555 Touhy Avenue, Dept. 3185, Skokie, IL 60076. Tel. (312) 982-2000.

\*Teletype is a trademark and service mark of the Teletype Corporation.

CIRCLE 19 ON INQUIRY CARD

## Computer Systems Use SOS Technology To Offer Performance in Compact Unit

To fill in the midrange of its business computer family, Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304 has introduced two computer systems based on proprietary SOS LSI semiconductor technology. The SOS chips result in high performance computers of smaller size, lower cost, and lower power requirements than comparable computers using traditional technologies. The HP 300, a general purpose business computer that takes no more space than a free standing data terminal and can support 16 terminals in transaction processing, uses nine microprocessor chips—three for I/O, three for CPU, and three for random logic. In the HP 3000 series 33, an LSI version of the HP 3000 line uses a 3-chip SOS/CMOS CPU in place of nine boards in the series III. Offering five programming languages, data base management system, and remote diagnostic capability, it expands to 1M bytes of main memory and 960M bytes of disc storage and supports up to 32 terminals.

Capable of expanding to 1M bytes of error correcting memory within the basic terminal-sized enclosure, the HP 300 has few of the arbitrary restrictions normally associated with computers in its price class. Including either Business BASIC or RPG-II language, the system is based on the Amigo/300 virtual memory operating system, which, in conjunction with the intelligent integrated display system (IDS), greatly simplifies development and control of dedicated online business applications. The Amigo system permits the system to perform background jobs while higher priority tasks are occurring from application



Occupying no more space than data terminal, Hewlett-Packard's SOS LSI based HP 300 Business Computer System supports 16 terminals and operates as multiprogramming, multitasking system managing both background and foreground jobs

terminals. IDS schedules, monitors, and controls these concurrent activities and simplifies the process of program development and testing.

Packing up to 1M bytes of main memory and a 1M-byte flexible disc drive in a desk sized unit, the HP 3000 series 33 runs the MPE-III multiprogramming executive operating system of the larger Series II and III systems. Online transaction processing applications are served through MPE-III features that include virtual memory, multiprogramming, and multilevel security. The SPL/3000 systems programming language, and COBOL, RPG, FORTRAN, and BASIC applications programming languages are supported.

Data base management is provided by IMAGE/3000 with its QUERY subsystem; KSAM/3000, an optional access method, provides keyed sequen-

tial access to fields having 1 primary and up to 15 alternate keys per data record. Designed to provide both standalone source data entry capability and a frontend to online transaction processing systems, VIEW/3000 allows users to create custom business forms on a CRT terminal.

Incorporated into the system console is a diagnostic microcomputer that gives users the ability to check for correct operation using a data cartridge that plugs into the console. In addition, it is possible via modem to pass complete interactive control of all console capabilities to a remote location.

With a U.S. list price of \$36,500, a basic HP 300 includes one language, 256k bytes of error correcting main memory, 12M-byte fixed disc, 1M-byte flexible disc drive, and integrated display. Optional peripherals include HP 2640 and 2621 CRT terminals, 2631 180-char/s dot matrix serial printer, and two removable pack disc drives, including 20M-byte 7906, 50M-byte 7920, or 120M-byte 7925.

A basic configuration series 33 includes CPU, 256k-byte fault correcting main memory, 1M-byte flexible disc drive, 20M-byte fixed system disc, system/maintenance console, and desk enclosure. List price is \$70,000 and deliveries are scheduled to begin in January. Terminal options include the HP 2621 or 2640 series; both 50M-byte 7920 and 120M-byte 7925 moving head discs are supported.

Plans for the future include data communications facilities for HP distributed systems networking on the 300; for the Series 33, future capabilities will include advanced synchronous data communications such as networking, remote job entry, and multipoint terminal support.

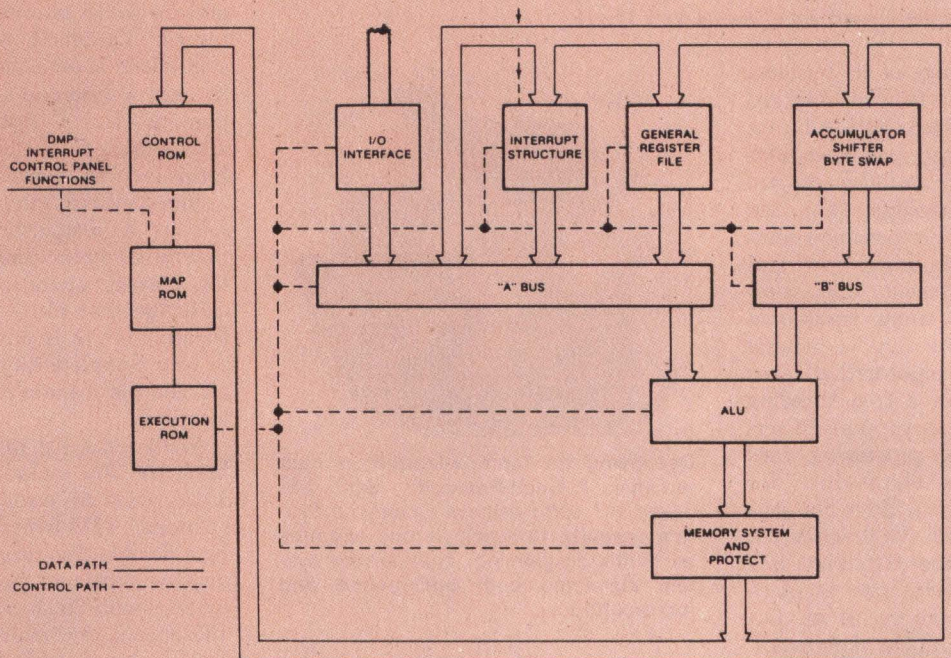
Circle 170 on Inquiry Card



Supporting five programming languages, data base management, and data entry software, the HP 3000 Series 33 uses SOS LSI technology to achieve compactness and freedom from site constraints, and to reduce power requirements and offer diagnostic self-test

## Computer On A Board Offers Low Cost Power For Realtime Applications

A 16-bit parallel processor, offered as a board level unit or fully integrated system, the CLASSIC 7810 adapts the power and flexibility of other family members to use in lower levels of measurement, control, scientific, and information processing applications. Areas pinpointed by Modular Com-



Basic organization of Modular Computer's CLASSIC 7810. All major system elements are connected to the modular data bus structure, 16-bit parallel path used for all data transfers within computer. Data transfers and processing are controlled by execution of microinstructions stored in ROM control memory

puter Systems, Inc, 1650 W McNab Rd, Fort Lauderdale, FL 33309 as now cost-justifiable include use as a standalone system CPU, as a node in a distributed network, or as distributed intelligence within measurement and control systems based on the MODACS III process input/output system.

Available with 64k, 96k, or 128k bytes of solid-state memory, the 7810 has a full MODCOMP II instruction set as well as 15 general purpose registers and system protect features. It is fully compatible with MODCOMP II and with the company's other computers. It uses MAX II and III operating systems as well as their MAXNET extensions.

Effective memory cycle time is 600 ns with error checking. All memory is directly addressable in any of seven addressing modes.

The system's 15 16-bit general registers enable handling of high speed computations as well as communication and control applications. In many problems all operands can be held in the registers and operated on by the

register to register instruction set. Execution time for a typical register to register instruction is 900 ns. A sixteenth addressable register is provided for direct operator communication with the program.

The processor's input/output system has 63 peripheral device addresses and synchronizes transfers with interrupts. A direct memory processor consisting of four automatic multiplexed transfer channels enables up to eight blocks of words to be transferred between memory and peripheral devices. Automatic data chaining capability is also provided.

Sixteen interrupt levels can be selectively enabled and disabled under program control. Request signal for all levels can be program generated to serve as a debugging aid and to reduce overhead in monitor operations. The priority queue can be program manipulated by deferring interrupt processing to the low priority end of the queue.

An optional control panel allows data entry and display, program fill, master clear, console keylock, and

console interrupt functions. A battery backup option serves to maintain MOS memory refresh on power loss.

Three versions of the processor are available: two are board-only, the other is a fully packaged system including 4-slot chassis and power system. A board level processor with 64k-bytes memory is priced at \$3250 (single quantity). A fully packaged system with remote fill capability has a tag of \$7500. Deliveries are scheduled for second quarter 1979.

Circle 171 on Inquiry Card

### Data System Additions Aimed at Needs of Distributed Processing

An entry level machine and expanded memory models on the top of the line have been announced by Data General Corp, Westboro, MA 01581 to offer Eclipse Data System users the economies of a single vendor approach to distributed data processing. The

**Which CRT family  
now includes a simple,  
character-mode terminal with  
bright, high-resolution display, two full  
pages of continuously scrolling memory,  
familiar typewriter-like keyboard with  
embedded numeric keypad, comprehensive  
character and line editing, eight  
preprogrammed function keys,  
self-test and optional built-in  
120 cps hard copy?**

# HP introduc

We took a long, hard look at how you use a simple CRT terminal. We applied 10 years of experience producing sophisticated, high-performance computer products, so the newest member of HP's terminal family is engineered from just one point of view: yours.

If you used a CRT all day, you'd demand the brightest, sharpest display made. So we didn't take any shortcuts on the 2621's display. It's the same display with enhanced 9X15 character cell you see on every HP CRT terminal, even our top-of-the-line models.

Interactive sessions go faster if you can look back at what you've already done. So we designed two full pages (48 80-character lines) of continuously scrolling memory into the 2621.

Recognize the 2621's keyboard? It's a lot like the familiar typewriter almost everyone's used to. Which makes the 2621 easier to learn, faster to use. And to accelerate keying in numbers, we put the numeric keypad right in the middle of the keyboard.

Then we increased the capability of the 2621's simple keyboard with eight special keys. In regular use, they control the cursor, rolling and scrolling. But they're also labelled on the screen with preprogrammed functions which, with a touch of the shift key, control self-testing, terminal configuration, display functions and editing.

Editing? On a simple CRT? Sure, because editing gets more work done faster. The 2621's comprehensive editing includes character and line insert and delete, clear line and clear display. What's more, the 2621 keeps your input separate from your CPU's so you can edit data before sending it to your CPU. And all without rewriting a line of your system's software.

And the 2621 is Bell 103A compatible and communicates with your CPU at 110 to 9600 baud through an RS232C interface. Which makes interfacing a snap.

That's the 2621A.

But we've gone a step further. How many times have you wanted just to hit a key and get hard copy of your CRT display without making a big project out of it? Now you can with the 2621P. Its built-in 120 cps thermal printer zips out a

page of hard copy in seconds. With a single keystroke.

And here's more good news: the 2621A costs only \$1450; the 2621P with built-in hard copy costs only \$2550.

Surprised by all these features in a simple, inexpensive, character-mode CRT? We don't think simple has to mean unsophisticated. To prove it, we're turning HP's advanced technology and 40 years of manufacturing experience into products you need.

Like the 2621: the simple CRT you'd expect from Hewlett-Packard.



**Try this on your favorite CRT:** With the 2621P, you just hit a key and walk away in seconds with hard copy of your CRT display. The built-in thermal printer prints upper and lower case at up to 120 cps.

The 2621's bright, high-resolution CRT displays the full 128-character ASCII character set, including upper and lower case, control codes, and character-by-character underline, in 24 80-character lines.

Eight screen-labeled preprogrammed function keys magnify the power of the 2621's keyboard. Preprogrammed functions include editing, terminal configuration, printer control and self-test.

To make numeric data entry faster and easier, we put the 2621's numeric keypad right in the middle of the keyboard, instead of at one side.

The 2621's familiar 68-key keyboard is almost as easy to use as a typewriter.

**CIRCLE 20 ON INQUIRY CARD**

HEWLETT  PACKARD

\*U.S. List Price

- I'd like to know more about HP's new 2621A and 2621P with built-in hard copy.
- I'd like to see HP's new 2621A and 2621P with built-in hard copy.
- I'd like to know more about HP's complete family of terminals.

Name \_\_\_\_\_

Title \_\_\_\_\_

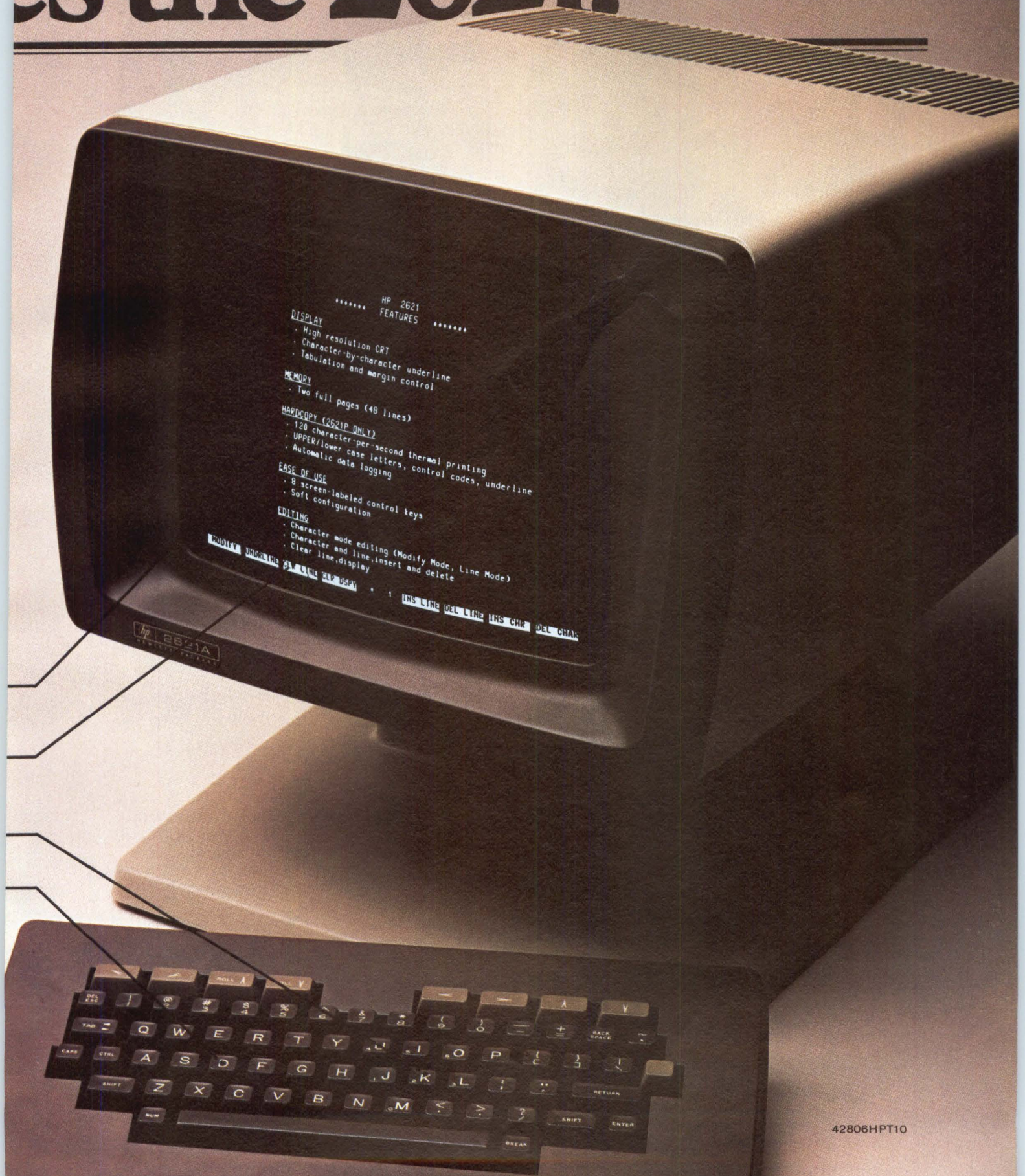
Company \_\_\_\_\_

Address \_\_\_\_\_

Phone \_\_\_\_\_

Mail to Hewlett-Packard, Attn: Ed Hayes,  
Marketing Manager, Data Terminals Division, Dept. 1239  
19400 Homestead Road, Cupertino CA 95014.

# es the 2621.



```
***** HP 2621
          FEATURES *****

DISPLAY
- High resolution CRT
- Character-by-character underline
- Tabulation and margin control

MEMORY
- Two full pages (48 lines)

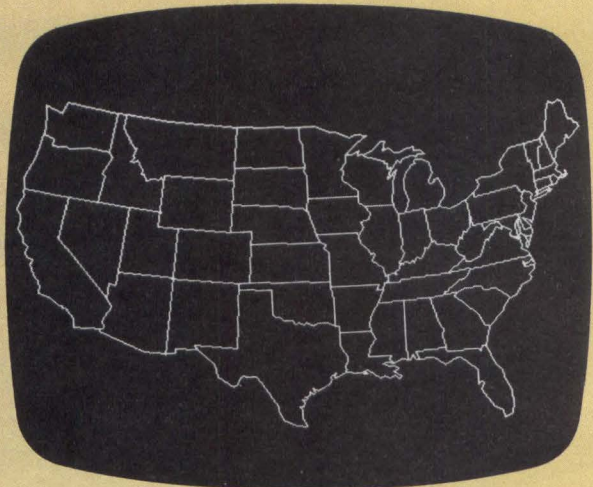
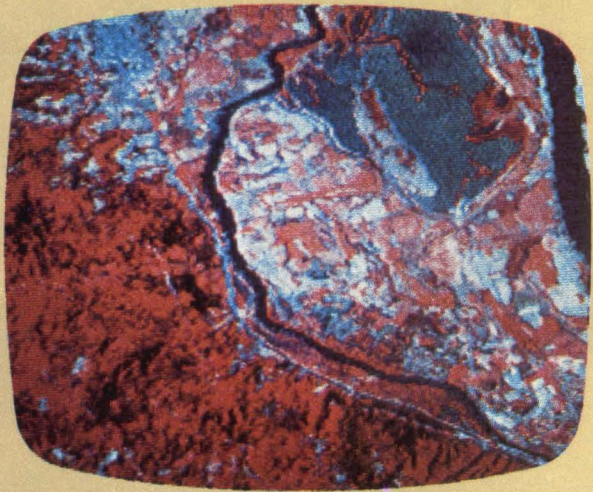
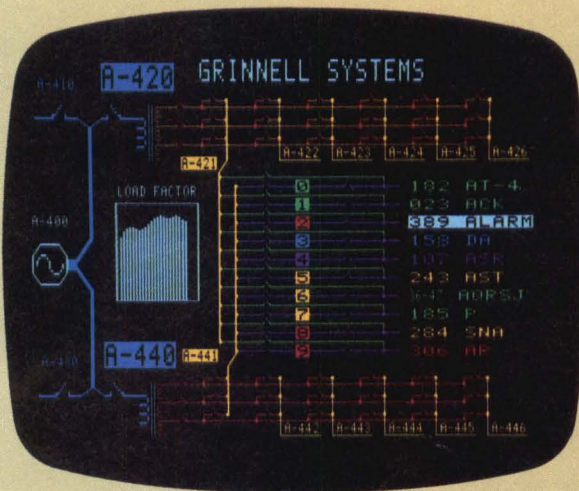
HARDCOPY (2621P ONLY)
- 120 character-per-second thermal printing
- UPPER/lower case letters, control codes, underline
- Automatic data logging

EASE OF USE
- 8 screen-labeled control keys
- Soft configuration

EDITING
- Character mode editing (Modify Mode, Line Mode)
- Character and line, insert and delete
- Clear line, display
```

hp 2621A  
2621P 2621S

# Grinnell has your display...



## from low cost imaging and graphics to full color image processing

Our modular, solid state systems can meet your computer display requirement, easily and economically.

And, they're intelligent. Every system has a complete alphanumeric and graphics package, and a powerful instruction set that simplifies programming—no need for complex macro-instructions and high order programming languages.

There's also a choice of standard resolutions: 256 x 256, 256 x 512, 512 x 512 (30 Hz or 60 Hz refresh) and 1024 x 1024. Plus plug compatible interfaces for most minis.

Options include overlays, function memories, pseudo-color tables, zoom and pan, independent cursors with trackball and joystick controls, split-screen, image toggling, and real time digitizers that grab and store images and sum consecutive frames.

Grinnell displays are already used for tomography, ERTS imaging, process control, image processing, animation and much more. All systems drive standard TV monitors.

So before you choose a display system, let our experts show you how to maximize performance and minimize cost. For details, and/or a quote, call or write.

# GRINNELL SYSTEMS

2986 Scott Boulevard, Santa Clara, California 95050 (408) 988-2100

CIRCLE 21 ON INQUIRY CARD



entry level Eclipse C/150 will allow organizations to cost-justify distributed processing in an increasing number of applications, and expanded memory on Eclipse M/600 machines will allow users to continue on up the line in online multifunction environments.

Designed for use either as a stand-alone computer or as part of a distributed data processing network, the C/150 is capable of using all major commercial computer languages and is compatible with larger systems in the line. The unit's CPU offers up to 256k bytes of MOS/ERCC or CORE main memory. Packed 256k bytes to a single board, MOS memory has a 700-ns maximum cycle time. Error checking and correction are standard. System throughput is maximized with an extended hardware stack and high speed interrupt handling.

Systems are controlled by the real-time disc operating system (RDOS), a compact operating system optimized for multiterminal applications where rapid terminal response is required and capable of supporting a limited amount of concurrent activity including program development, batch processing, or communications. Interactive data entry/access (IDEA) software provides a development and runtime system for multiterminal data entry and inquiry/response application.

Data storage is managed by INFOS, a database oriented file management system. IDEA, COBOL, and RPG II are fully integrated with INFOS to allow access and update of files in both interactive and batch applications. RJE80 and HASP II communication software packages facilitate data transmission between other C/150 systems, IBM systems, and the company's other systems.

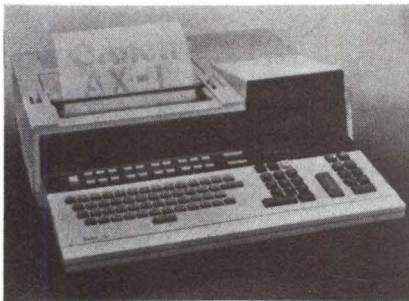
Extending the family upward, M/600 models incorporate two times the main memory of previous models (*Computer Design*, Mar 1978, pp 34, 38). This greater capacity serves to expand the performance range of the machines. Representative systems would include 1M bytes of memory, 4M bytes of fixed head disc, synchronous communications, and 32 terminals.

A typical small C/150 configuration would consist of processor with 128k-byte memory, 10M-byte cartridge disc, magnetic tape drive, and terminal printer. A large system might comprise 256k-byte memory, 190M-byte disc subsystem, magnetic tape drive, 16-line asynchronous line multiplexer, 2 CRT consoles and 12 displays, and 600-line/min printer. Approximate prices are \$54,000 and \$144,000, respectively. Deliveries are scheduled for January 1979.

Circle 172 on Inquiry Card

### Programmable Desktop Computers Incorporate Plotting Printer and Disc

Capable of performing fast, accurate information processing, AX-1 and BX-1 store data on minifloppy discs, provide a 16-digit alphanumeric display,



Canon's AX-1 incorporates a built-in minifloppy disc for use in conjunction with RAM, thermal plotting printer, and alphanumeric display. Up to 45 programs can be searched for, loaded, and executed using a single key on the keyboard

and print on 8.5" (21.6-cm) wide paper. The programmable desktop computers, developed by Canon, Inc, Tokyo and announced by Canon USA, Inc, Systems Div, 10 Nevada Dr, Lake Success, NY 11042, connect with additional optional peripheral devices through RS-232 (V.24) interface units and I/O controller.

Operating in the  $-10^{99}$  to  $10^{99}$  range on 13-digit mantissa and 2-digit exponent, the units perform +, -, x, ÷,  $a^x$ ,  $\sqrt{\quad}$ , log, and  $e^x$  operations and follow the algebraic operation system. Programming is done in Canon (AX) or Canon Extended BASIC (BX) language. The AX provides 20k-bytes ROM and 1k-byte RAM system memory area and a max of 16k-bytes of user accessible space. BX memory consists of 24k-byte ROM and 1k-byte RAM system area and a max of 16k-bytes of user memory.

The minifloppy drive, X-7309, has capacity for 71.7k bytes of data; 65.5k bytes are accessible to the user. The drive transfers at 125k bits/s. Print-

ing at 40 char/s, the integral thermal printer is capable of full or half pitch printing on 24-, 48-, or 80-digit wide lines. The 16-digit fluorescent tube panel displays numerals, upper and lower case letters, and symbols. Messages prompt the operator through the calculating sequence. On entry of erroneous data, the panel will display a specific error classification message to inform the operator of the error.

Among the BASIC functions provided by the BX-2 are record, load, call, link, flag, and half and full statements. Up to 10 levels of program subroutine nesting is possible, as well as up to 10 levels of FOR TO NEXT statements.

Circle 173 on Inquiry Card

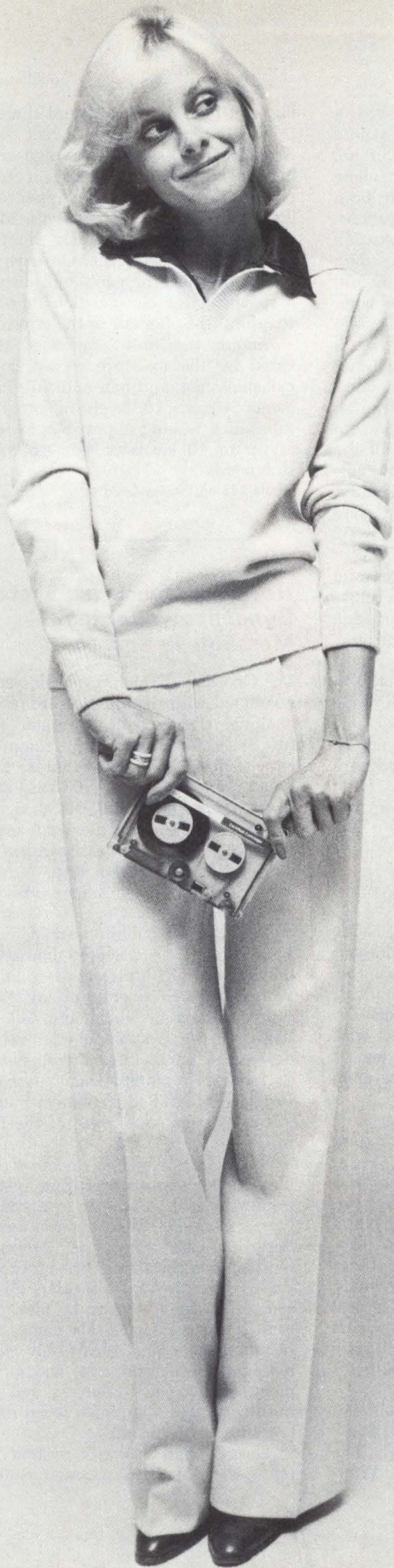
### Network Operating System Dynamically Routes Message By Best Path

The Guardian/Expand network system combined with the architecture of the NonStop Tandem/16 computer system serves to eliminate the computer as a source of network failures. Tandem Computers Inc, 19333 Vallico Pkwy, Cupertino, CA 95014 designed the system to allow users to access resources of any node regardless of its location, with the system automatically routing messages via the best path.

Designed for online terminal/transaction data base oriented operation, the Tandem/16 provides a multiple processor system tolerant of any single component failure. Although all resources in the system function as independent parallel resources, system components automatically assume workload of a failed component, while the user remains unaware of the failure.

Guardian, the system's general purpose multiprocessor operating system resides in each processor in a system but is aware of all other processors. Based on the concept of processes sending messages to other processes, the operating system considers all resources in the system to be files, and each to have a logical file name. Application programs deal only with file names, providing total geographic independence of resources, and requiring no reprogramming when hardware resources change.

The Expand network system extends the Guardian message system,



**USING  
OUR  
CARTRIDGE  
DRIVE FOR  
WINCHESTER  
DISK  
BACKUP  
IS BETTER  
THAN  
PLAYING  
DISK  
JOCKEY.**



If your mini-computer customer looks like a disk jockey, maybe it's time you gave some thought to our cartridge tape drive for Winchester disk backup.

Our increased capability  $\frac{1}{4}$ " cartridge tape drive does the work of an arm load of floppies.

The Funnel™ as we call our 6400 BPI High Density Cartridge Tape Drive, features four-track serial recording and boasts a transfer rate of 192 kilobits per second.

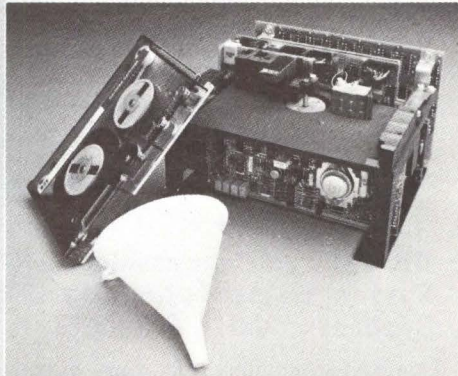
And with its ability to store up to 17.28 Megabytes on a single cartridge, it has about 17 times the capacity of the latest double density, double sided floppy.

When you add to all that the Funnel's high quality design and reliability, you can see why it's quickly becoming the preferred choice of mini-computer designers and users. In fact, we've delivered over 2,000 units for disk backup.

But our cartridge drive does more than just get your customer out of the D. J. doldrums. It can also offer significant savings even if your system presently uses just two floppies for fixed disk backup. Because with its increased capability, the Funnel lowers your storage cost to just a penny per kilobit.

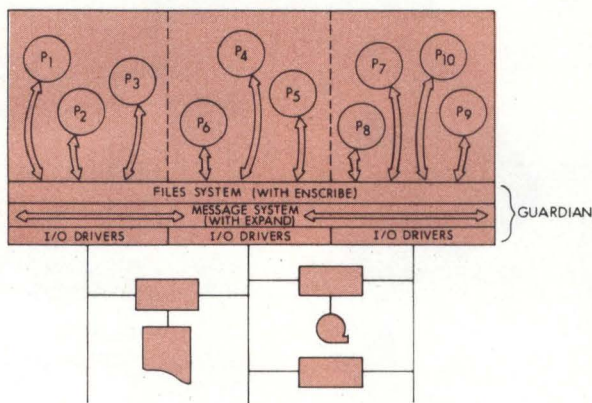
So stop asking your customers to play disk jockey and start calling DEI for OEM quotations. We think what we have to say will be music to your ears.

Call (213) 351-8991, or write The Funnel, Data Electronics, Inc., 370 North Halstead St., Pasadena, Ca. 91107. Telex 67-5327.



**DEI** WE STORE BYTES  
IN M'S NOT IN K'S

CIRCLE 22 ON INQUIRY CARD



Message system in Tandem's Guardian/Expand network operating system is software analog of hardware bus, handling automatic path retries in case of path errors. Communication between process (denoted by circles) and other resource is via file system, which passes message to message system. Message system in turn determines recipient's physical location and routes message there by best path

allowing up to 255 separate computers to be linked together. Major components of the network system are end to end protocol, network control process, network line handler, network routing table, and network utilities.

Based on exchange of packets over a communications path, the end to end protocol insures integrity of messages regardless of the number of intervening nodes and resources utilized in the transmission. Support is provided for communications paths on either a full-duplex telephone line or a virtual circuit through an X.25 network.

Maintaining the routing table, logging network changes, and servicing some requests from remote nodes, the network control process also handles requests for remote resources.

Line handlers establish and maintain the communications path between two physically connected nodes. They can also create a logical connection between non-neighboring nodes by forwarding messages.

Utility programs aid the user in monitoring network status and in tracing problems. A tracing facility creates a trace file that tracks events occurring with a specific line handler; these data are formatted for report generation. Statistics for a given line handler are reported by protocol level, including counts of frames sent and received by type, and number of requests initiated or processed. Utilities can be run from any terminal in the network, and their output directed to any terminal or other output device.

Circle 174 on Inquiry Card

### Distributed Processing System Elements Include Processor Using 64k RAM

Compact computers featuring distributed processing and easy to use control programming, the 8100 Information System family initially consists of two processor models plus associ-

ated display stations, printers, and storage devices. Versatility and cost/performance benefits are provided by use of high density storage components—64k- and 18k-bit memory chips. Made using an n-channel metal gate FET process that enhances gate reliability using silicon nitride and controls surface leakage with a conductive

field shield, the monolithic RAM array chips take advantage of dynamic 1-device cell arrays and the FET process to provide greatly improved density at low cost.

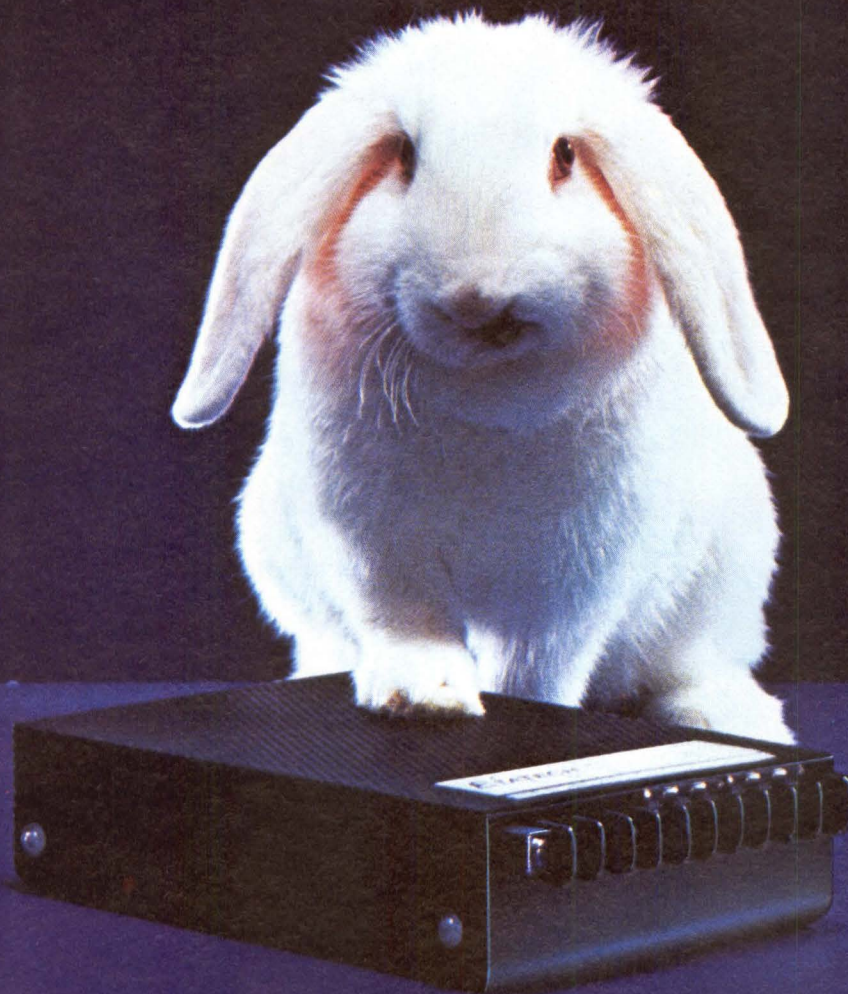
Combining with each other and with other systems and terminals, elements of the 8100 family, introduced by International Business Machines Corp, Data Processing Div, 1133 Westchester Ave, White Plains, NY 10604, include a choice of 8130 or 8140 processor, 8010 storage and communication unit, 8775 display terminal, and 8809 reel to reel magnetic tape unit. With an internal operating speed of 1.5  $\mu$ s, the 8130 has from 256k to 512k bytes of main memory; the 8140 operates at 800 ns. Both have 1M bytes of removable flexible disc storage and 64M bytes of main storage provided by built in high speed disc memory.

An 8101 storage and communication unit can increase data storage capacity to 320M bytes on high speed disc. Four of these units can be used with the 8140 (two with the 8130) to accommodate display, printer, and magnetic tape units. Data terminals and processing systems can be attached using available communications adapters.

A system might initially be used as a standalone computer, then later linked to a host System/370 in a cooperative network processing plan. Programs for the systems include a series of step by step programming instructions in English that will enable users to develop their own application programs, and control functions to accommodate multiple users. Additionally, common business and scientific languages can be used as well as software that allows operators at a central /370 site to program, test, and run remote 8100 processors.

High level functions are provided the systems by the distributed processing programming execution (DPPX) which permits multiple users to process transactions concurrently and enables operation as an independent or satellite distributed processing system, and distributed processing control executive (DPCX) which can handle up to 31 operations simultaneously. DPPX works with the data base and transaction management system, host command facility with 3270 data stream compatibility, development management system, and distributed presentation features. In addition, it can be programmed to respond to specific batch processing situations

# A low-cost DC/DC Converter is something worthy of protection



## ETATECH. THE PRICE AND QUALITY LEADER IN DC/DC CONVERTERS.

Etatech has a complete line of single and multiple output units, ranging in input voltage from 12 to 125VDC, output voltage from 5 to 48VDC and output power from 40 to 126 watts. Our exclusive "Univerter"™ design lowers parts counts so drastically (71 parts, Model B5D10) that our medium power density "B" and "D" series units are offered at the lowest prices available anywhere. As indicated in the table below,

Etatech is your answer for low price and reliable performance in modular and open frame DC/DC converters.

For complete specifications and prices on 71 other modular DC/DC converter models, plus information on Etatech's new open frame line, circle the reader service number and receive our new 28-page catalog. Or, for more immediate action, give us a call. Incidentally, Etatech's variety of AC input units are priced below the competition too.



ETATECH, INC.  
187-M W. Orangethorpe Ave.  
Placentia, CA 92670. (714) 996-0981

MODEL NO.	INPUT VOLTS (VDC)	OUTPUT VOLTS (VDC)	OUTPUT CURRENT (ADC)	PACKAGE SIZE	MIN. EFFICIENCY (%)	217B MTBF @ 80° C BASEPLATE	UNIT PRICE
OA5D10	28	5	10	4.87 x 7.50 x 2.12	69%	68K Hours	\$149.
B12E5	48	12	5	4.87 x 7.00 x 1.75	75%	68K Hours	\$195.
D5H20	125	5	20	5.00 x 9.00 x 2.25	71%	68K Hours	\$233.

A 5 Year Warranty is standard on all Etatech products.

# Computer Terminals

**We'll translate your next computer terminal design into the right ICs.**

We make it our business to know your business. We have to. Because we know your future depends on it.

It's no secret that things change fast in your business. Or that success or failure depends on how well you use semiconductor technology in your next computer terminal design.

That's where we come in.

Our people speak your language. They know how to save you time. And money. By helping you select the right ICs for your design. Every time.

Signetics wants to help keep you ahead in the terminal design game. Because if you're not ahead, you're not even a player.

That's why we give you more than just the right product. We also give you the Signetics Commitment. We don't publish specs on it. And it's not scribed on our ICs. But we do market this extra, personal commitment. And it's free.

Our professionals in IC technology and market support are backed by Signetics' six integrated divisions. That means we can combine our total resources in both MOS and bipolar technologies to give you the edge in computer terminal OEM design.

For example, our MOS Microprocessor Division's 2652 is the fastest multi-protocol communications controller in the world at

*Rudi Willers, Signetics sales engineer (left), talks terminals with Bo Fredricsson, Qantel's director of R & D.*



# Spoken Here.

2Mbits/second. It's right at home with most high-level protocols.

Every computer terminal OEM looks for unique logic functions. With the smallest amount of random logic practical. And Signetics wants to make it easy for the designer.

Working together, our Logic and Bipolar Memory Divisions have responded to the terminal OEM's demands for speed and flexibility.

We've gone beyond LSI to give the terminal OEM the 8A2000 I<sup>2</sup>L Gate Array. It's got 2000 gates. And you can customize the 8A2000 to your proprietary needs without losing LSI benefits.

In fact, all you stand to lose is the need to use 50 to 75 random logic packages by going with the 8A2000 in your design.

With our family of field programmable logic, including the FPLA, FPGA, and ROM patch, we make it easy for you to out-design the competition.

And more design freedom's on

the way. We'll soon be offering the world's first Field Programmable Logic Sequencer.

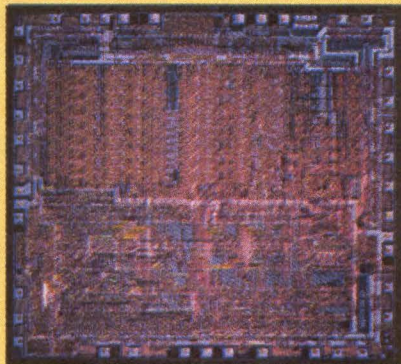
Responding to your needs, our Logic Division created the bipolar 8X300  $\mu$ P. Its blazing speed of 4 million operations/second and control-oriented architecture make it ideal for adding state-of-the-art peripherals to your terminal system.

While our field professionals help computer terminal OEMs translate difficult design choices into the right ICs, other Signetics professionals are applying the most advanced technologies into devices to meet the OEM's future demands.

Talk to a Signetics professional. We've bridged the communications gap between terminal OEM and IC manufacturer.

To learn how our leading-edge technologies are making innovation simpler for terminal OEM designers, write us today.

We've got a brochure that tells you how you can put our advanced ICs to work for you. On your own terms.



2652 multi-protocol communications controller

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a subsidiary of U.S. Philips Corporation

Signetics Corporation  
P.O. Box 9052  
811 East Arques Avenue  
Sunnyvale, California 94086  
Telephone 408/739-7700

To: Signetics Information Services, 811 East Arques Avenue  
P.O. Box 9052, Sunnyvale, CA 94086

Please send your brochure that describes the full range of ICs and capabilities available to the computer terminal OEM.

My need is urgent. Please have a Signetics professional phone me at (\_\_\_\_\_) \_\_\_\_\_

Name \_\_\_\_\_ Title \_\_\_\_\_

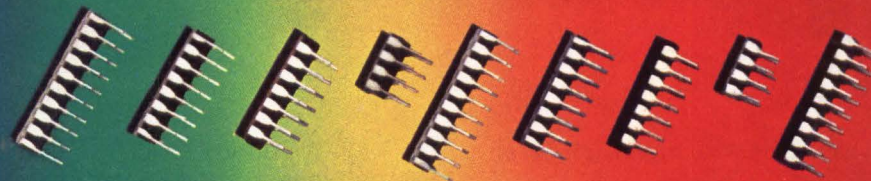
Company \_\_\_\_\_ Division \_\_\_\_\_

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CD-12

# PEP



## Beat the odds on early-life failures with PEP. And get the tightest AQL's in the industry. From the quality leader. Texas Instruments.

Lower your total system cost. Decrease field service. Decrease incoming test costs.

PEP, the Product Enhancement Program from Texas Instruments, provides off-the-shelf IC's with enhanced quality and higher reliability. With PEP you:

- Reduce or eliminate incoming IC inspection
- Improve yields through assembly

- Reduce field returns and service

PEP 3 and 4 provide 100% burn-in to accelerate the integrated circuit through early operational life, when IC failure rates are the highest, to the period where the failure rate typically reaches less than 0.0005% per 1000 hrs... a typical IC MTBF of 23 years for a system containing 1000 PEP ICs.

PEP processing is offered on

Linear, Bipolar Memory and Bipolar Microprocessor, as well as all TTL families including Low Power Schottky (74LS), Schottky (74S), and Standard TTL (74)...in either plastic or ceramic DIP.

The new PEP now offers in all popular TTL families:

- 100% high temperature functional, continuity, and parametric testing
- Industry's tightest AQL (0.1% AQL cumulative for parametric, functional, and continuity)
- 2% burn-in PDA on PEP 3 (Plastic) and PEP 4 (Ceramic)

For the complete story on updated PEP processing, and a copy of the new PEP brochure, contact your local TI field sales office or authorized TI distributor. Or, write Texas Instruments Incorporated, P.O. Box 225012, M/S 308, Dallas, Texas 75265.



TEST	CONDITION	GUARANTEED AQL %					
		BIPOLAR LOGIC		BIPOLAR MEMORY		LINEAR	
		PEP 1, PEP 3	PEP 4	PEP 1, PEP 3	PEP 4	PEP 1, PEP 3	PEP 4
Continuity	100°C	0.015	0.015	0.015	0.015	0.015	0.015
Functional	0°C to 70°C	0.10	0.10	0.25	0.25	0.10	0.10
DC Parametric	0°C to 70°C			0.65	0.65	0.25 (Note 1)	0.25 (Note 1)
AC Parametric	25°C (Note 2)	0.65	0.65	1.00	1.00	1.00	1.00
Fine Leak	1 x 10 <sup>-6</sup> Leak Rate	NA	0.65	NA	0.65	NA	0.65
Gross Leak	Step C-1	NA	0.40	NA	0.40	NA	0.40
Mechanical Defects (Note 3)	Critical	0.10	0.10	0.10	0.10	0.10	0.10
	Major	1.00	1.00	1.00	1.00	1.00	1.00

Notes:

(1) For linear devices, a 0.25% AQL at 25°C and a 0.65% AQL at 70°C apply.

(2) Sampled and guaranteed.

(3) Critical mechanical defects are those which affect device functionality. Major defects include problems not affecting functionality.

TEXAS INSTRUMENTS  
INCORPORATED



without operator intervention as an aid to balancing workloads.

For those requiring a host controlled network using systems network architecture, DPCX provides improved processing speed and access to 320M bytes of data. The program incorporates functions of the 3790 communication system including the ability to be tested and programmed from a central System/370.

Depending on configuration and control program, transmission method, and other factors, data speeds up to 56k bytes/s are possible between 8100 elements and other systems. The system is based on Systems Network Architecture for orderly network growth. Communications adapters allow bisynchronous and start-stop devices to be attached.

Elements of the system are available for purchase, lease, or rental. Individual elements are priced in the \$29,940 (8130 with 512k main memory, 1M-byte diskette, and 64M-byte disc) to \$46,980 (8140 with 512k-byte memory, 1M-byte diskette, and 64M-byte disc) range. First shipments are scheduled to begin in third quarter 1979.

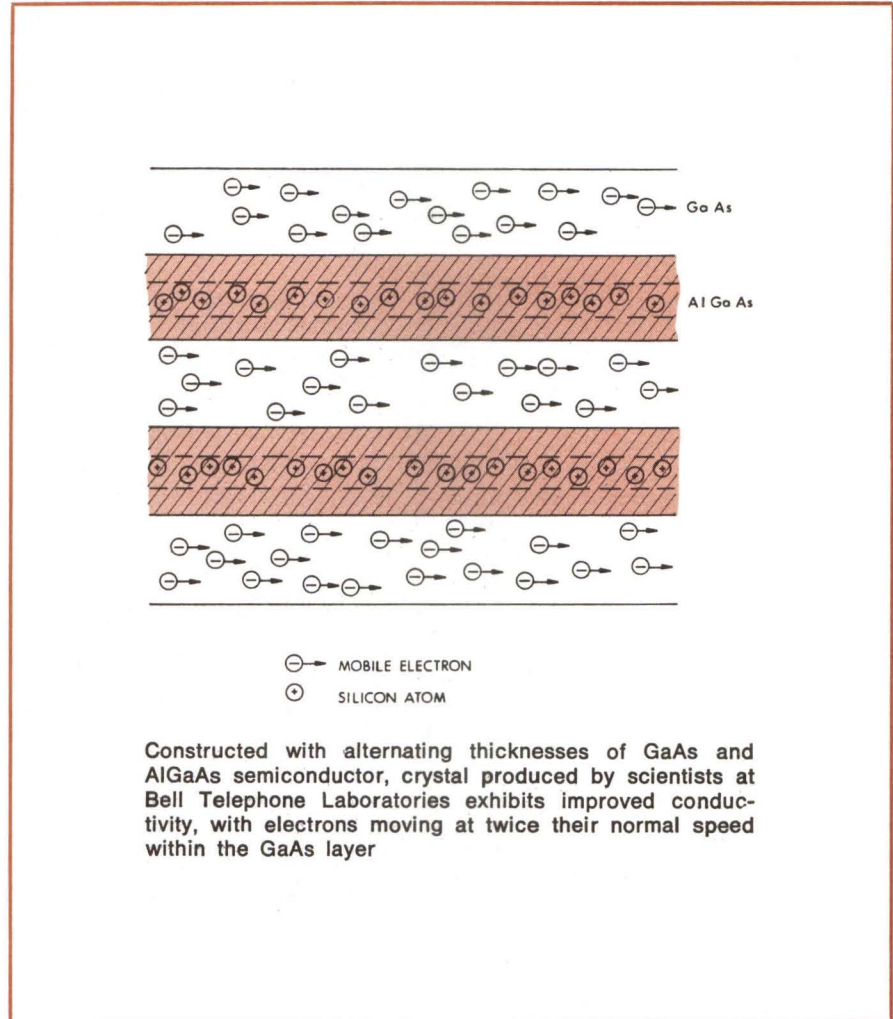
Circle 175 on Inquiry Card

### Technological Advance Speeds Electron Movement In Semiconductor Materials

Doubling the speed at which electrons can move through semiconductor crystals at room temperature could both improve circuit speed and reduce its power requirements. This fundamental advance in solid-state technology has been reported by scientists at Bell Telephone Laboratories, Mountain Ave, Murray Hill, NJ 07974.

Materials that conduct electricity better than insulators but not as well as metals, semiconductors have electrical properties that can be precisely controlled by addition of impurities. Such impurities limit their conductivity by slowing down their negatively charged electrons. By devising a technique to isolate electrons from these impurities, scientists have enabled the electrons to move freely and with little interference.

A semiconductor's ability to carry current can be boosted by adding small amounts of an impurity element



Constructed with alternating thicknesses of GaAs and AlGaAs semiconductor, crystal produced by scientists at Bell Telephone Laboratories exhibits improved conductivity, with electrons moving at twice their normal speed within the GaAs layer

that will donate free electrons. Each impurity atom gives up one electron that moves through the semiconductor as current. The impurity left behind is positively charged, having given off one negative charge, and therefore attracts free electrons, slowing them down.

To isolate these electrons from parent impurity atoms, a crystal growing process called molecular beam epitaxy was used to build crystals one layer of atoms at a time, layering two semiconductor materials to form a single crystal. Using this process, a crystal of alternating thicknesses of gallium arsenite (GaAs) and aluminum gallium arsenide (AlGaAs) was produced, with silicon impurities added only to AlGaAs layers. Since the two materials provide different environments for free electrons, when silicon is added to AlGaAs, electrons migrate spontaneously to the GaAs

layer, leaving positively charged silicon behind in the AlGaAs layer. To further assure isolation of electrons, silicon was added only to the middle region of AlGaAs layers, thus creating neutral borders between free electrons and silicon.

Once in different layers, silicon impurity atoms and electrons have little chance to interact, leaving the electrons free to move rapidly within the GaAs. Speeds were found to be twice as great as in standard GaAs semiconductors at room temperature, and 20 times as fast at lower temperatures. Moreover, the technique may be used with any combination of semiconductors having the same fundamental properties as GaAs and AlGaAs, and could provide a means for enhancing the performance of computer circuits and multiplying the capacity of communications systems.

Circle 176 on Inquiry Card

## **FORTRAN Based Computers Packaged To Fill Price/Performance Needs**

Packaged computer systems combining the 8/32 Megamini<sup>®</sup> computer with globally optimizing FORTRAN VII offer price/performance that answers the needs of FORTRAN users with applications in scientific research, simulation, and data acquisition. The Interdata Div of the Perkin-Elmer Corp, 2 Crescent Pl, Oceanport, NJ 08857 states that the systems will provide the fastest FORTRAN execution available and will enable users to develop application programs as fast or faster than other minicomputer systems.

The smaller FORTRAN system, priced at \$89,900, includes a model 8/32 with 512k bytes of main memory, high speed floating point hardware, 10M-byte disc, 800-bit/in (315/cm) magnetic tape, Carousel console, dynamic multitasking operating system, FORTRAN VII, and system diagnostics. With 768k bytes of memory, 67M-byte disc, and FORTRAN enhancement package with 2k writable control store, the larger system sells for \$134,000. FORTRAN VII offers the speed necessary for immediate response. Programs can be compiled at 1500 lines/min. Automatic job control allows programs to be compiled, linked, loaded, and executed with a single command input.

Circle 177 on Inquiry Card

## **Portable Computer System Can Be Configured by Laboratory Researchers**

Designed for use by a broad range of people, MINC contains hardware and software enhancements that accommodate laboratory interfacing and application development by researchers who are not computer experts. The compact, modular computer system, announced by Digital Equipment Corp's Laboratory Data Products Group, Maynard, MA 01754, mounts on a scope-cart-style portable cabinet for easy transportation between locations. The system's BASIC language operating system allows users to issue commands directly to mass storage devices without learning the operating system.

Standard for all configurations is a PDP-11/03 processor with 30k-word

memory capacity and extended and floating point instruction sets, three serial line channels, and IEEE-488 standard interface. Seven functional module types can be used in combinations to a maximum of eight to customize a laboratory system. Available are analog-to-digital converter, digital-to-analog converter, digital input, digital output, multiplexer, pre-amplifier, and programmable clock modules.

Input/output modules have from 4 to 64 channels depending on module type and use. MINC connection blocks may be detached from the system and remain connected to instrumentation. When the system is wheeled up to the instruments, connector blocks can be plugged directly into the system module permitting minimum connection time.

The system uses an rx02 double density dual diskette unit for program and data storage, and the vt105 video graphic terminal for display. The terminal has full alphanumeric capabilities plus a graphics facility of 512 horizontal by 190 vertical positions. Data can be presented graphically in point or histogram mode, and alphanumeric are presented in upper or lower case, double-height, double-width, or both.

MINC BASIC software, an extension of PDP-11 BASIC, permits the user to issue commands directly to mass storage devices to perform functions such as transferring files between discs. Other commands allow user control of data transfer through analog and digital interfaces. The system will also run RT-11 FORTRAN IV which is available with a library of subroutines to support module options, interface, and terminal.

Circle 178 on Inquiry Card

## **Storage/Refresh Graphics Display Offers 70% Increase in Capacity**

A 25" (63.5-cm) storage/refresh graphics display, the GMA 125 claims capacity for 70% more information than other available units. This capacity and the screen's large visual angle enable resolution of adjacent points that would be indistinguishable on a 19" (48-cm) display and increase the number of screen size alternatives.

In addition, the unit, manufactured by Tektronix, Inc, Information Display Group, PO Box 500, Beaverton,

OR 97077, incorporates an extension of the DVST with refresh technology used in other members of the series. The storage CRT achieves high density, high quality graphic images; addition of substantial refresh (write through) capability yields dynamic interactivity, simplifying, cutting time, and increasing comprehension of graphics.

Option 42 vector generator and option 43 vector/dot character generator transform digital signals from most computers into analog signals required by the basic display, providing a parallel interface that is compatible with all series members. By allowing higher throughput speeds than a serial interface, these options significantly reduce the time required to electronically integrate the display into a product. 12-bit addressing resolution for 12.6M viewable picture elements is available with option 42.

Compatibility with 220-V and 50-Hz international power sources are offered by the unit's energy-efficient switching type power supply. The display chassis is symmetrical in structure allowing the whole unit to be rotated to obtain a long vertical axis format.

Circle 179 on Inquiry Card

## **Updated COBOL Specs Available for Comment**

Being considered as a candidate for standardization by the American National Standards Institute Committee on Computers and Information Processing (ANSI/X3), the Journal of Development of the CODASYL COBOL Committee includes developments to Dec 1977. A few of the 21 changes that have been incorporated are (1) a facility to specify symbolic characters and positionally relate them to the native character set or user-defined alphabet; (2) global and external specification for data items; (3) a multibranch, multijoin structure, the EVALUATE statement, to cause multiple conditions to be evaluated; (4) an inline PERFORM statement capability.

Copies of the CODASYL COBOL 1978 Journal of Development may be obtained from Department of Supply and Services, Material Data Management Center, 4/B1 Place du Portage, Phase III, 11 Laurier St, Hull, Quebec, K1A 0S5, Canada. Orders must include \$10 remittance made payable to "The Receiver General for Canada."

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compatible series, there's another Ampex storage module family that begins at 100 megs and grows all the way to 300 megs. This 10-high drive series uses the same industry-compatible interface as the 40-80-160 family.

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easy disk storage growth. Call Larry Russell at 213/640-0150. Or write to him at Ampex Memory Products Division, 200 North Nash Street, El Segundo, California 90245. Ask him how to improve your drive.

## All the way to 160 megabytes.

# AMPEX

# DIGITAL CONTROL AND AUTOMATION SYSTEMS

## High Speed Laser System Welds Terminals of Miniature Relays Under Microcomputer Control

Terminals can now be spot welded on miniature relays at speeds up to 20 welds/s. A microcomputer controlled high speed laser welding system developed by Western Electric at its Engineering Research Center in Princeton, NJ is claimed to be four times as fast as the resistance welding system it replaces—and much more reliable.

In order to fit properly on telephone transmission equipment printed circuit boards, the relay first must be attached to adapter plates. Terminals jutting from a relay's base fit through holes in the adapter plates and are crimped to tabs on the plates to insure proper positioning and good thermal contact before welding.

The spot welding system, made up of a 200-W average power pulsed Nd:YAG laser and an x-y positioning system, is controlled by a Motorola 6800 microprocessor and programmable read-only memory. Four different programs can be switch-selected to accommodate different relay configurations. Linear encoders enable the microprocessor to monitor the position of x-y table [which has 0.0001" (2.54- $\mu$ m) accuracy] and anticipate targets within a 30-ms period. Welding occurs "on-the-fly" at speeds up to 5" (12.7 cm)/s.

At the welding station, batches of up to 30 relays are loaded onto a precision tray that positions each phosphor-bronze tab within  $\pm 0.002$ " (0.051 mm). The

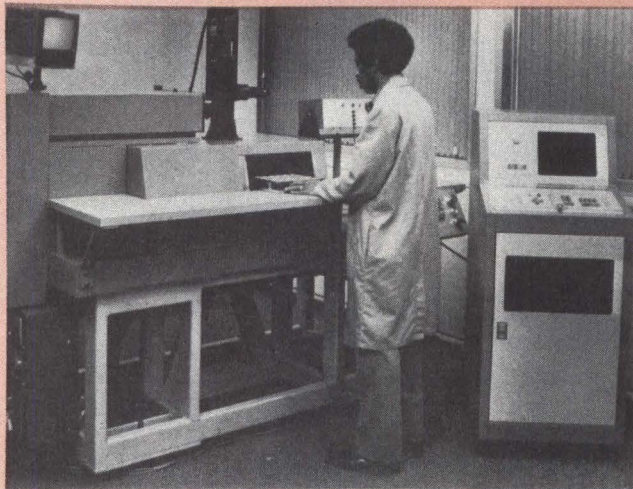
microprocessor indexes the x-y table and, in turn, the tray to preprogrammed positions within the laser beam's focal plane.

Laser pulses of 5-ms duration and 8 J of energy content are focused down to approximately 0.020" (0.508-mm) diameter to provide welds at  $8 \times 10^5$ -W/cm<sup>2</sup> intensity. To minimize wear on the positioning system, the targets are scanned past a stationary focused beam at constant speed. The microprocessor controller requires approximately 30 ms to compute the next target location and fire the laser. Because of this interval and because some of the relay adapter plates have spacing between consecutive tabs as small as 0.150" (0.381 cm), scanning speed can be no greater than 5" (12.7 cm)/s.

Once a loaded fixture is mounted on the x-y table and the program cycle is initiated by the operator, both the fixture and the enclosure door are locked in position by two solenoid driven mechanisms that insure target location and light-tightness. The loading door and all access panels are interlocked to the laser firing circuitry, while a TV monitor allows safe viewing of the welding operation.

Before the laser welding system was developed, inspection and mechanical testing for bond strength often ruptured otherwise acceptable spot welds. Such tests were necessary because welds created by the resistance welding system were completely hidden and could not be inspected visually. However, laser welding produces a highly visible, shiny nugget on the terminals that reduces inspection to a simple visual check. Studies show that an appreciable nugget almost always indicates a strong weld. Reliability is even further increased by making two welds on each tab.

Circle 160 on Inquiry Card



Microcomputer controlled laser welding system. Tray of 30 miniature relays is fed onto X-Y table. Laser welds each relay terminal to tab on adapter plate that assures proper positioning on PC board. System not only improves reliability by making two welds instead of previous one, but welds are now visible for easy inspection and are made at one-fourth the time of replaced resistance welding system

### DC&AS BRIEFS

#### Data Acquisition Systems Use Desktop Computers as Controllers

Research and development of process control systems as well as monitoring of transducer parameter measurements, testing of production devices, and analysis of phenomena are all feasible with a data acquisition system announced by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304. This diversity of application exists because the user has a choice of three

# FPS Expands the Scientific Universe of PDP-11 Applications

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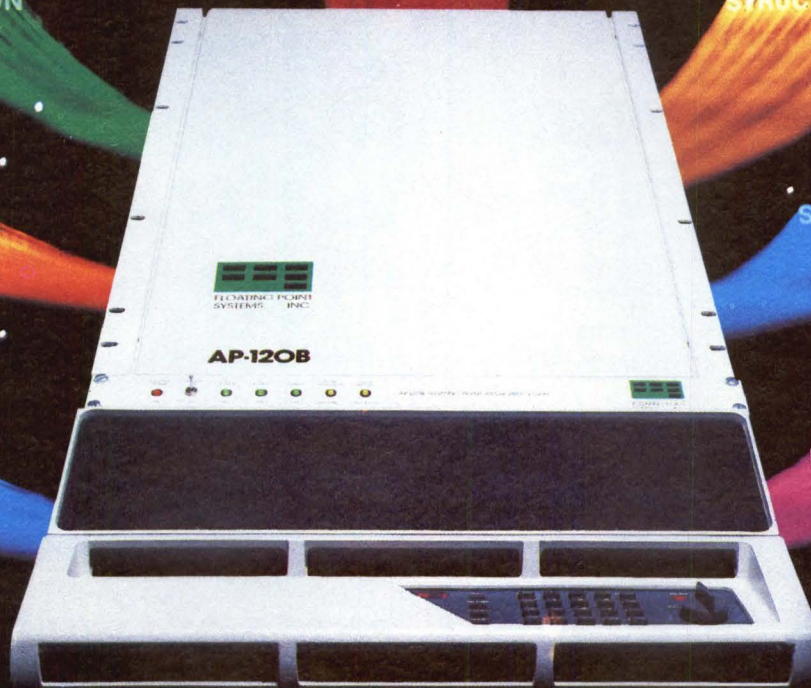
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SIGNAL PROCESSING

STATISTICAL ANALYSIS

LOAD-FLOW ANALYSIS

IMAGE PROCESSING



## FPS MAKES GREAT COMPUTERS BETTER

### The FPS AP-120B Array Processor

A great contribution to technology, the DEC PDP-11\*, but it can't give you the computational power required for many scientific applications. That's why FPS developed the AP-120B Array Processor.

The AP-120B Array Processor gives economical minicomputer systems the extraordinary computational power of large scientific computers. For example, an AP-120B has been used in a PDP-11/34 system to reconstruct and analyze complex digital images. Without the AP-120B, the task would take more than two hours. With the AP-120B, it takes less than thirty seconds — that's a 240X improvement!

A PDP-11/70 and AP-120B would offer

even greater data handling capabilities.

The FPS architecture is no secret. Internally synchronous operation and seven parallel data paths provide unequalled cost performance, reliability, and programmability. Programmable I/O units also enable exceptional features, such as direct control of disc storage and real time data flow.

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Hundreds of FPS Array Processors are in use today by people who want to retain the hands-on control and affordability of a minicomputer system, but require the exceptional throughput of a large mainframe for their application.

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My Computer System is  My Application is

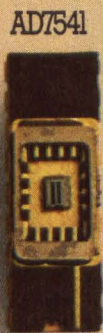
# FORGET HYBRIDS. 12 BIT

## 12 BITS, 12 BUCKS. OUR NEW AD7541 CMOS M-DAC GIVES YOU EVERYTHING A HYBRID CAN'T.

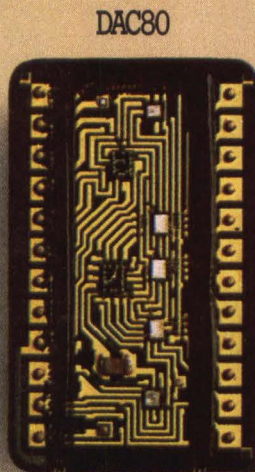
Our new AD7541 is the world's only true 12-bit-accurate monolithic multiplying DAC. Its low, low price, only \$12 in 1000s, is big news. But more important is the performance of the AD7541. It offers full 4-quadrant multiplication and guaranteed 12-bit linearity (0.012% over temperature).

The AD7541's inputs are TTL and CMOS logic compatible. For the AD7541's current output, settling time is 500 nanoseconds, typically, 1 microsecond maximum. High density CMOS and laser wafer trimming of its onchip thin film resistors are the keys to the AD7541's high performance, low power, low price and small size. In addition, single-chip construction inherently offers vastly improved reliability over multi-chip hybrid designs.

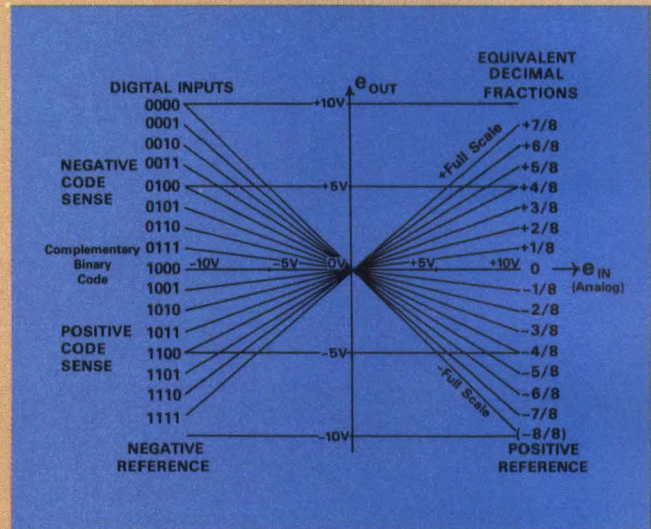
Below: unretouched photo of AD7541 and typical DAC80 with lids removed.



THIS.

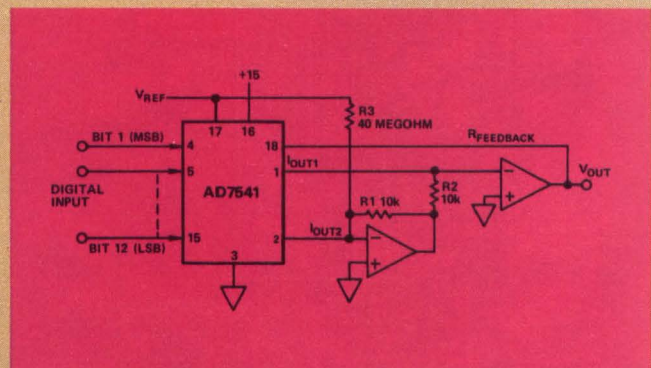


NOT THIS.

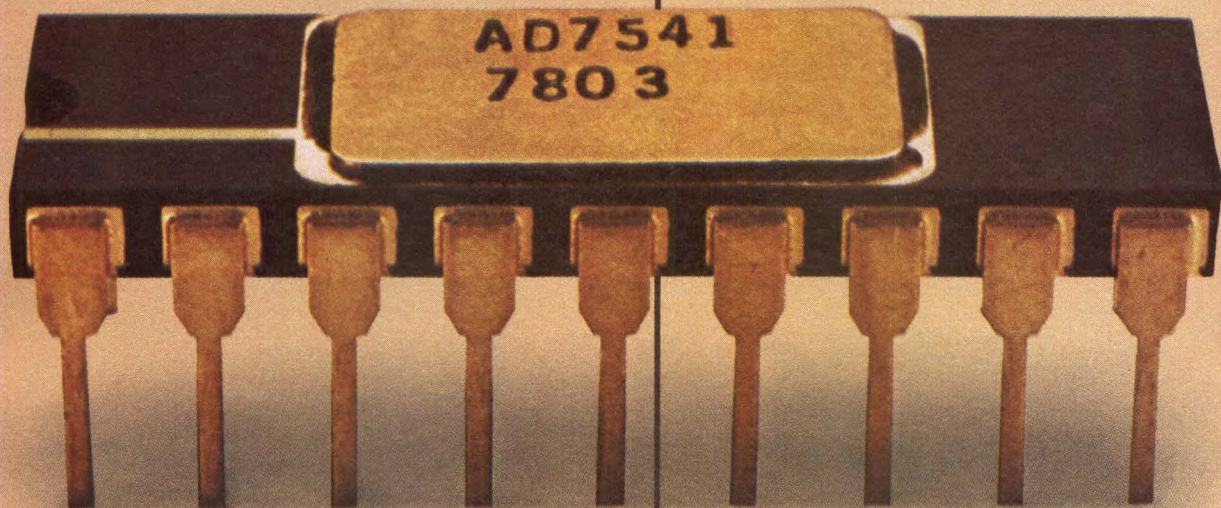


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The 4-quadrant multiplication feature of the AD7541 M-DAC permits it to function with both positive and negative variable references, either AC or DC, without any circuit changes. This opens up a wide range of applications for the AD7541 in digitally controlled gain or attenuator circuits, synchro-to-digital converters and ratio-metric low-power converters, as well as digitally controlled power supplies.



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# \$12



## WAY OUT IN FRONT.

# How to get a jump on the future in microcomputer design.

Don't wait for the future. It's here today with the 8086, Intel's advanced new 16-bit microcomputer. And now there's SDK-86, the System Design Kit that gives you valuable hands-on experience with 8086 hardware, introduces you to the "architecture of the future" and enables you to begin actual prototype development today.

Everything you need to get started is included, from resistors and crystal to CPU. For data memory, there are 2K bytes of 2142 static RAM, with sockets to double that. And there's room for 8K bytes of program memory, using either or both of the keyboard and TTY/CRT 4K ROM-resident software monitors included in the kit, or 2716/2316E EPROM/ROM. Plus there's a fully-buffered system bus and plenty of board space for your own prototype circuitry.

To make it easy to use SDK-86, we've provided three separate ways to control the system and enter programs and data.

There's a keyboard with LED display, a built-in serial communications interface, and we've provided a cable that connects the SDK-86 to any Intellec<sup>®</sup> microcomputer development system.

In addition to the 8251A USART interface, there are two 8255A programmable peripheral interfaces, providing up to 48 I/O lines, and an 8279 programmable keyboard/display interface. You can assemble SDK-86 in a day with a soldering iron and a few tools. Naturally, there are both Assembly and User's Manuals, plus an 8086 User's Manual. The kit is \$780 in single unit quantities.

You can order it, or any 8086 system components from your local Intel distributor. Or, for data sheets on our complete 8086 system, call your local Intel sales office or write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone 408/987-8080.

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Europe: Intel International, Rue du Moulin a Papier, 51-Boite 1, B-1160, Brussels, Belgium. Telex 24814.

Japan: Intel Japan, K.K., Flower Hill-Shinmachi East Bldg. 1-23-9, Shinmachi, Setagaya-ku, Tokyo 154. Telex 781-28426.

**CIRCLE 29 ON INQUIRY CARD**







Automatic data acquisition system. Version shown is 3052A system with 9845S desktop computer serving as controller

system controllers, each with specific computation and analysis capabilities.

The model 3052A data acquisition system consists of a 3455A high accuracy/high resolution digital multimeter (DMM), a 3437A high speed sampling digital voltmeter (DVM), and a 3495 scanner, in addition to the controller. Inclusion of the two voltmeters provides both high speed and high accuracy measurements. For example, on the 100-mV DMM range, dc measurement rates up to 19 channels/s are possible with 1- $\mu$ V resolution, while 4500 readings/s can be made on a single high speed channel with the DVM. By multiplexing the DVM input with the scanner, as many as 1000 channels/s can be measured with 100- $\mu$ V resolution and 3 $\frac{1}{2}$  digits.

Accurate, repeatable, low level measurements are claimed to be possible even in the presence of noise. A DMM and scanner combination provides >120-dB effective common-mode rejection to cancel out unwanted offsets or superimposed noise signals.

Measurements of up to 1 MHz can be made with the standard ac true rms converter. A programmable fast ac mode provides an ac measurement rate of up to 10 channels/s for inputs above 300 Hz. Repetitive waveforms up to 1 MHz or low frequency transients below 1 kHz can be digitized by the DVM.

Resistance measurements can be made with either an easy-to-connect 2-wire technique or more accurate 4-wire method. Multiplexed high resistance measurements up to 15 M $\Omega$  are possible with the full DMM accuracy.

The three system controllers are the HP 9825S, 9835A, and 9845S desktop computers. Both the 9835A and 9845S use BASIC language, while the 9825S uses HPL. (HPL is similar to but more flexible than BASIC and FORTRAN. It features multiple statement lines, multidimensional arrays, and dynamic dimensioning of arrays.) All three controllers use HP-IB (IEEE-488) I/O.

Standard memories for the 9825S, 9835A, and 9845S, respectively, are 23k, 50k, and 62k 8-bit bytes. Memory on the 9835A is expandable to 246k. The 9825S includes alphanumeric display and 16-character thermal strip printer; the 9835A has a CRT display with printing and character plotting and a 16-character thermal line printer; while the 9845S features a CRT display with

full graphics, an 80-character thermal printer, and a dual tape cartridge drive (with 217 bytes/transport).

Relay actuator cards in the scanner enable control, alarm, and multiple switching functions. Each card provides 10 dpst contact closures for connection to external devices.

The system is fully integrated, tested, verified, and specified with complete software and documentation supplied. Various subroutine software packages are arranged in order by the user to suit a particular application. An "auto-loader" routine configures subroutines automatically into a single program and stores the program on tape for use at any time.

Circle 161 on Inquiry Card

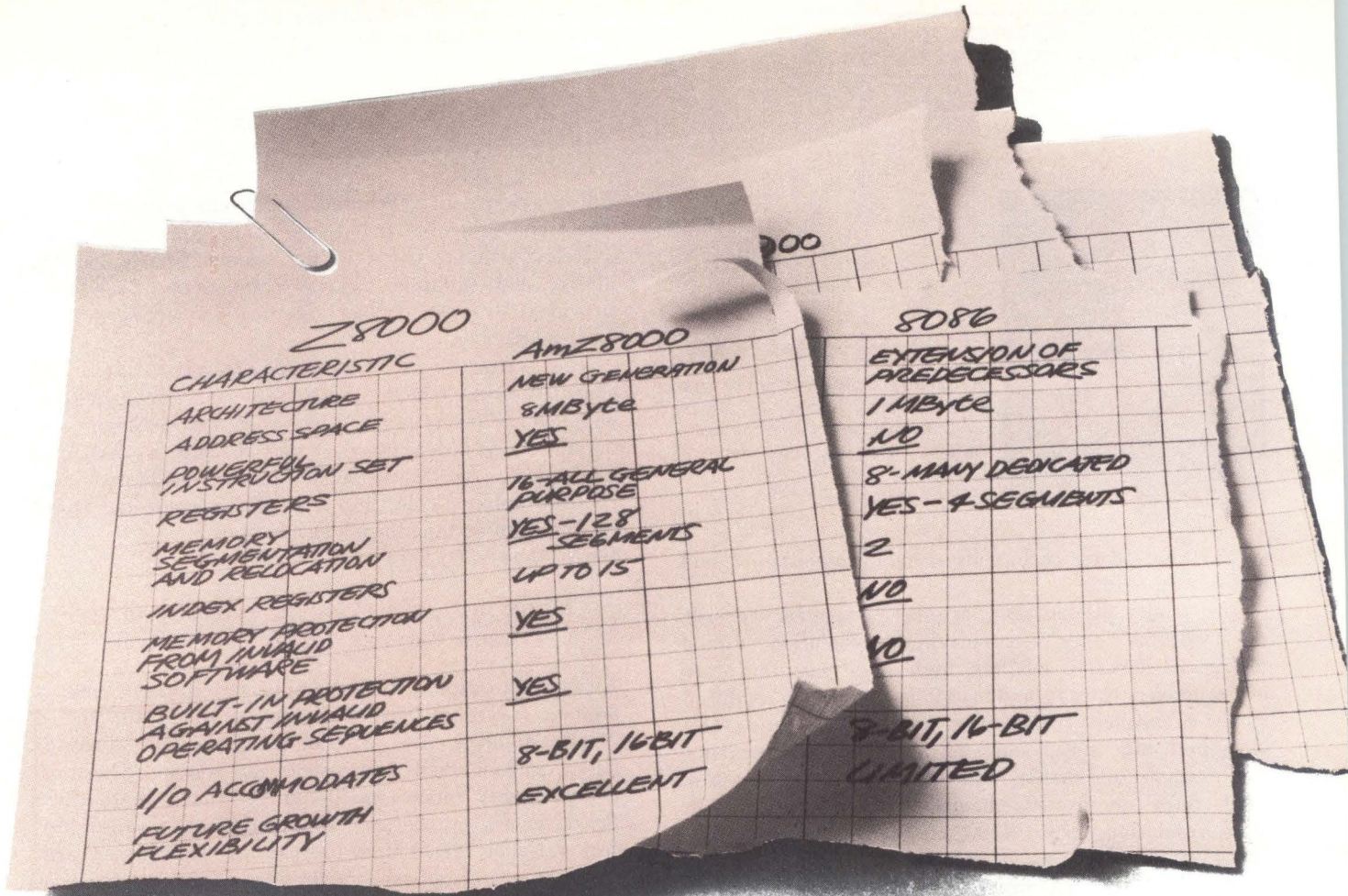
### Single Instrument Generates and Controls Process Variable Versus Time Profiles

A variable setpoint versus time programmer plus a 3-mode controller have been combined in the model 770011 digital control programmer. This microprocessor based rackmounted instrument and three other programmer-only models made up of from one to three programmers can be used to generate and control process variable versus time profiles for applications such as vacuum and atmosphere heat-treat furnaces, environmental chambers, batch ovens, and kilns. All models have been introduced by Honeywell Inc, Process Control Div, 1100 Virginia Dr, Ft Washington, PA 19034.

The programmer/controller overcomes the mechanical problems of typical cam-type and curve-follower programmers and eliminates the need for separate programming and control units in a process control system. It can store up to nine separate programs consisting of up to 200 functions such as ramp or soak



Programmer/controller. Microprocessor based device combines variable setpoint versus time programmer with 3-mode controller in single instrument. All inputs are in engineering units. Other members of instrument family contain one, two, or three programmers but no controller



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## DIGITAL CONTROL AND AUTOMATION SYSTEMS

segments and event switches. Controller output forms include a choice of current proportional, time proportional, heat/cool, and position proportional. In industrial heating and environmental test applications, a guaranteed soak function allows the soak to proceed only when the process variable enters a selectable band around the setpoint.

Front panel pushbuttons are used to enter, verify, and edit program parameters. Operator commands for starting, stopping, and resetting the program can be actuated either at the front panel or via remote contact closures. Status-indicating LEDs and displays for program and segment numbers, setpoint, time, process variable, and error codes simplify the programming procedure. All data are entered directly in engineering units. Temperatures and ramp rates are set in actual degrees rather than percentages, and the progress of each program during entry, running, or verification modes is displayed in engineering units.

Automatic cycling of the same program for a preset number of times gives maximum flexibility for environmental chambers. In addition, program parameters can be changed without having to re-enter the existing program. Programs are stored in nonvolatile memory, requiring no battery backup facilities to retain stored programs during power failure. In the event of power



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failure, the memory holds all program elements and the program resumes from the point of the failure.

Proportional, integral, and derivative actions can be provided. Output can be controlled automatically or manually. Temperature range can be field selected for Fahrenheit or Celsius by an internal slide switch.

A self-diagnostic program is permanently stored in the instrument. When this program is run it exercises all electronics, digital displays, LED indicators, and pushbuttons, indicating the device to be fully operational. Circle 162 on Inquiry Card

### Solid-State Camera and Processor Function in Noncontact Inspection Applications

Charge injection device (CID) technology is the basis of the TN-2500 solid-state camera announced by General Electric Co, Optoelectronic Systems Operation, Syracuse, NY 13221. Designed for industrial applications, the camera is nonmicrophonic, is operable in a high magnetic environment, and utilizes a sensor that is said to provide 30% greater resolution than previous CID cameras. CID technology eliminates problems of image burn and lag associated with some other imagers, and provides an antiblooming capability that enables optimum imaging despite extreme highlights in the scene. (For a discussion of CIDs, see *Computer Design*, Nov 1977, pp 146-152.)

The camera is made up of two units: a body (electronics package) and a 3 x 3 x 2.1" (7.6 x 7.6 x 5.3-cm) remote head unit that can be operated at a distance of up to 50' (15 m) from the camera body. It provides low noise video output signals in both analog and digital format and requires no operating adjustments.

An associated PN-2303 decision processor segments the camera's field of view into electronic windows, and extracts measurement features from the image in each window. It then compares the measured features with predetermined standards of acceptance or rejection and provides output instructions to the user's system control.

Circle 163 on Inquiry Card

### Microcomputer System Designed for Process Monitoring

The cps03 is a self-contained, 3-board microcomputer system for OEM use in data concentration/process monitoring applications. It is based on an M6800 microprocessor and incorporates 10 serial communications lines, three parallel input/output ports, 5k bytes of RAM, 4k bytes of EPROM, realtime clock, and power supply.

Introduced by Pichler Associates, 410 Great Rd, Littleton, MA 01460, the system provides an RS-232-C EIA voltage level or 20-mA current loop line signal in any mix with full asynchronous modem control on any RS-232-C line. Under program control, the system accepts any 5-, 6-, 7-, or 8-level asynchronous code with or without parity. It features analog I/O points as well as isolated digital I/O points, and runs online self-test concurrently with data concentration.

Circle 164 on Inquiry Card

# NEC's Spinwriter repair kit.



## One screwdriver. 30-minute MTTR.

NEC's Spinwriter character printers are a serviceman's dream.

That's because 90 per cent of all routine service problems can be fixed with nothing more than a #2 Phillips screwdriver. Result: your service rep can fix almost any printer problem in less than a half-hour.

Take the carriage assembly, for example. With most printers, it's a huge time-consumer to fix, and often requires shipment of the printer back to the factory. With Spinwriter printers, you remove three screws, lift the carriage out, insert a new one, and replace the screws. That simple. Ten minutes, no more.

Or printed circuit boards. Any one or all can be replaced by removing just two screws—so a Spinwriter board can be changed in just three minutes. Much faster than on other printers.

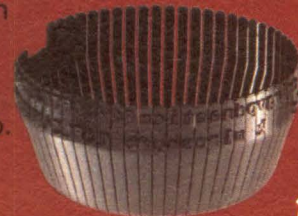
The operator control panel. A cinch. Remove four screws, and the entire assembly comes off—right down to the baseplate. The same is true with power

supply, fan, inverter block and keyboard assemblies. The only tool: a #2 Phillips.

Extraordinary serviceability? Sure. Now add to MTTR the Spinwriter MTBF—more than 2000 hours, the highest in the industry—and you get a printer that not only can be fixed faster, but one that needs very little service at all.

There's much more to Spinwriter printers: the superior print quality that comes from its unique thimble print element, the wide range of available fonts and forms-handling options, the eight most popular interfaces, and the whisper-quiet operation.

Find out more about Spinwriter character printers. And when you do, ask about our brand new Trimliner™ series of line printers too.



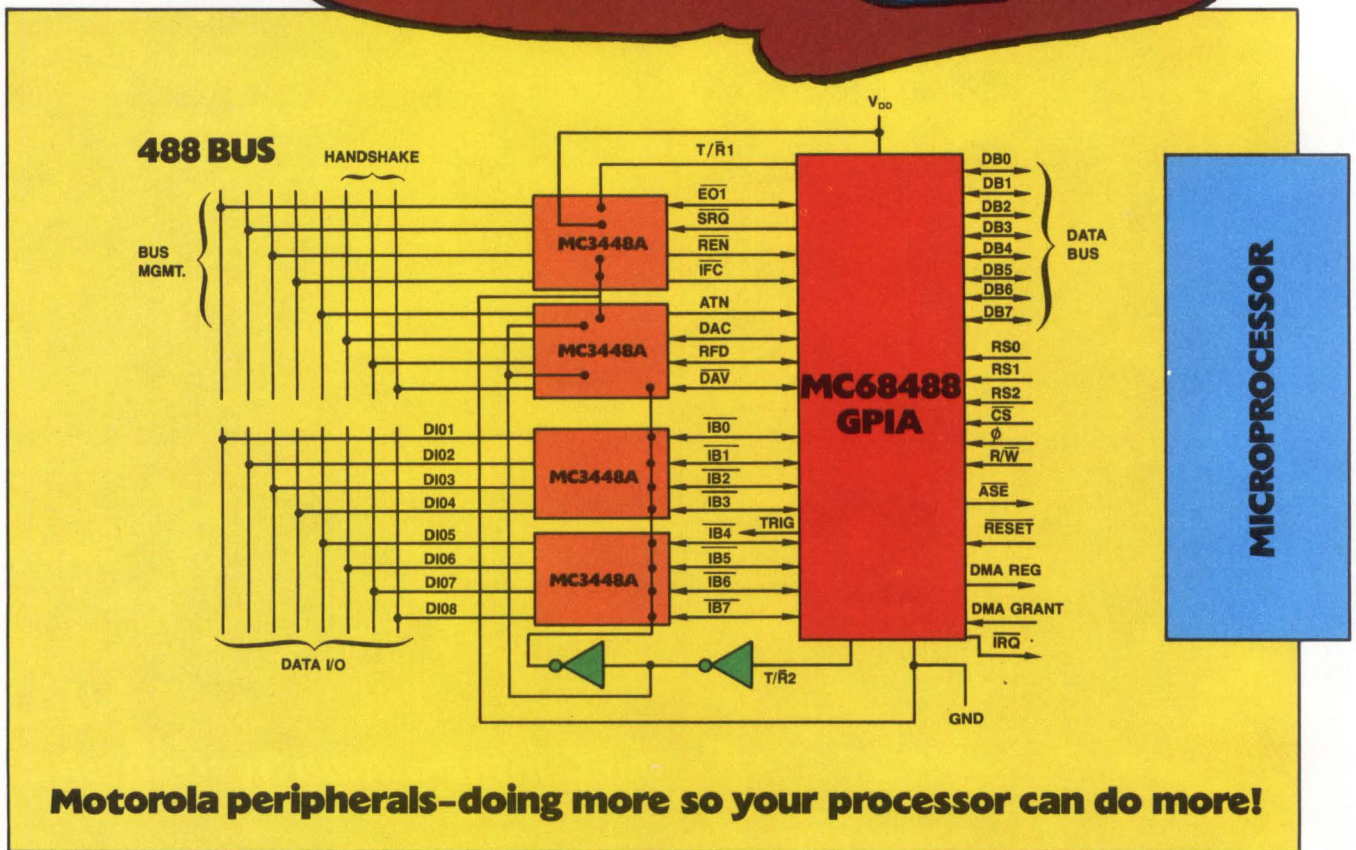
**NEC**

**NEC Information Systems, Inc.**

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Central Office: 3400 South Dixie Drive, Dayton, OH. 45439, (513) 294-6254  
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CIRCLE 32 ON INQUIRY CARD

# Implement your 488 bus with the MC68488,



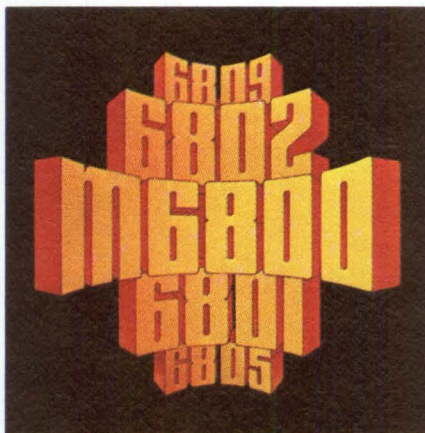
**Motorola peripherals—doing more so your processor can do more!**

# the easy, low-cost way Motorola's unique GPIA.

Motorola's MC68488 General-Purpose Interface Adapter, GPIA, makes microprocessors-microcomputers IEEE 488-bus compatible.

Development of the IEEE Standard 488 instrument bus enabled practical interconnection and remote programming or controlling of multiple programmable instruments. However, interface between the microprocessor or microcomputer and the 488 bus remained a costly and cumbersome task.

The GPIA provides that interface simply and inexpensively, and automatically handles handshake protocol needed on the instrument bus. As part of our fully compatible M6800 Family, it's designed to operate with all the M6800 microprocessors and single-chip microcomputers, but it serves other microprocessors, too. It's absolutely unique.



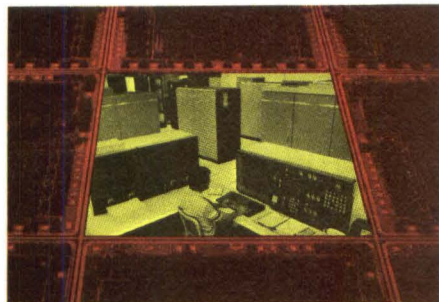
Probably most useful among the GPIA benefits are features like its serial polling capability, single or dual primary address recognition, and secondary address capability. There's so much more: complete source and acceptor handshakes, talk-only or listen-only capability,

synchronization trigger output, and selectable automatic features that minimize software. There's plenty of software to implement your own features, though, never fear.

Many designers will appreciate the GPIA's operation with a DMA controller, the programmable interrupts, and RFD holdoff for prevention of data overrun. As indicated, although the MC68488 is a member of the M6800 Family, with some additional logic it also can serve non-'6800 processors as the easiest, least expensive 488 bus interface. In 25-99 quantities, the plastic MC68488P is \$19.00, and the MC68488L ceramic device is \$21.50.

The GPIA is designed to team up with our MC3448A standard 488 bus drivers, to meet the complete electrical specifications of the IEEE 488 bus. Use it, and we believe you'll agree, it's *the* way to get your instruments on the bus.

## Your microprocessors can do more, because Motorola LSI puts systems on silicon.



Our various LSI and VLSI technologies range across CMOS, NMOS, LSTTL, and ECL, from single-bit to 16-bit capability, and provide a choice among multi-chip, two-chip, single-chip, and the bit-slice approach. There's a full complement of hardware and software support to make it all go.

The M6800 Family is the epitome of our concept for putting your systems on our silicon. With existing and soon-to-be available components, it offers an amazing variety of complexity and performance in applications from controls, to instrumentation, to data handling and communications.

- Multi-chip microprocessor-based systems from the MC6800 to the MC6809
- two-chip MC6802 systems
- single-chip microcomputers and microcontrollers like the MC6801 and the MC6805.

Everything, including development and support hardware and software is fully compatible.

Family memories, RAMs, ROMs, and EPROMs, a variety of peripheral control and I/O chips, and special purpose components like the GPIA generate an unmatched synergism. To ensure that your microprocessors can do more, we don't just build components, we put systems on silicon.

A new brochure covering Motorola's total systems-on-silicon capability is now available. For a copy, and copies of both the MC68488 data sheet and our 32-page IEEE 488 Bus Implementation brochure, circle the reader service number or send your written request to Motorola Semiconductor Group, P.O. Box 20912, Phoenix, AZ 85036.

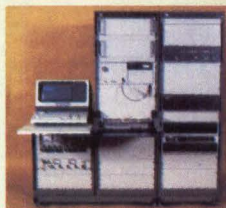


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**HP's simulator-based system**, at a cost roughly equivalent to comparison testers, increases testing efficiency. It gives

known fault-detection effectiveness. And it provides design feedback by analyzing circuits for failure modes and testability before they're even built.

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\* HP's implementation of IEEE Standard 488-1975.



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CIRCLE 34 ON INQUIRY CARD



### **Temperature Transmitter Provides Data in Digitized Format**

Temperature information from standard industrial thermocouples and platinum resistance thermometers is relayed to the computer in a control or monitor system in digitized format by the model 2600-D digital temperature transmitter introduced by RdF Corp, 23 Elm Ave, Hudson, NH 03051. Device design is based upon the industry standard 2-wire 4- to 20-mA process

control transmitter, except that data are signal conditioned, digitized, and transmitted in standard Teletype<sup>®</sup> terminal interface format. Specifications include accuracy of 0.1%, linearized output, compatibility with digital systems, UART data transfer, fm explosion proof housing, humidity-resistant construction, low installation cost, and 0.025% resolution of data. Another model, 2600-E, allows addressing of each individual data point, minimizing wiring to a large number of data points.

Circle 165 on Inquiry Card

### **Software Improves Programmable Controller Time Limiting Factor**

CREFL4, an addition to the library of utility programs for the DEC Industrial 14 programmable controller, allows the user to make ladder diagrams without a vt14 terminal. With CREFL4 (cross reference for Industrial 14), the time limiting factor in producing a ladder diagram is the output device, rather than the time it takes to compute the elements of the ladder diagram. Therefore, an entire ladder diagram can be printed in a matter of minutes instead of the hours required with a vt14. In addition, this software product from Process Control Systems, Inc, 18130 S Thornapple Lane, New Berlin, WI 53151 will make a ladder diagram for a spec-

ified output or all outputs after and including a specified output. When multiple circuits are requested, ladder diagrams are produced either in numerical order or in order of occurrence in the Industrial 14 memory.

A cross reference feature lists every output circuit in which the specified input or output is used, whether it is normally open or normally closed. An optional extended symbol feature lists both the input/output number and its symbolic designation if one is assigned.

A minimum organization requires an os/8 or os/78 system hardware or an os/8 partition under RTS-8 with 12k to 24k of memory, and related software. Any appropriate os/8 device may be used for I/O.

Circle 166 on Inquiry Card

### **Time Sequence Controller Is Replacement for Mechanical Timer**

As many as 256 events with 32 solid-state outputs are controlled by a device developed by Theta Instrument Corp, 24 Dwight Pl, Fairfield, NJ 07006. The model tsc-1000 time sequence controller stores events as independent groups of recallable programs. Program start addresses are selected through a 3-decade thumbwheel. Standard time ranges are 999 s or 999 min. Time readout is a 3-decade display of 0.43"

(1.09-cm) high LEDs. Other LEDs on the terminal strip indicate when a specific output is on. A battery backup supply automatically provides power to the RAMs for a 12-h period in case of loss of line power.

A separate sequence entry module with 3' (0.9-m) cable can be used to enter control points into the controller. The model SEM-256 handheld keyboard device displays numeral keys, store and increment, store, clear data, address increment, and reset.

Circle 167 on Inquiry Card

### **Strip Plating Thickness Monitored Without Interruption of Motion**

Thickness of gold, silver, tin, or other plating on flat or preformed strip can be measured automatically and accurately by a system called continuous strip monitor that does not interrupt motion of the strip. It functions without operator attention but triggers a signal if plating is greater or less than preset limits. Two models are available from UPA Technology, Inc, 60 Oak Dr, Syosset, NY 11791: CSM-1 for measuring on flat or unformed strip, and CSM-2 for "preformed" strip.

Thickness measurements are computed by a microprocessor-based instrument called Memoderm that provides an alphanumeric printout of all thickness readings and statistics. The instrument automatically standardizes itself and stores, in any one of its 15 memory positions, the precise calibration constants required for accurate, repeatable, drift free measurement of plating thickness. In addition, the printer provides a permanent record histogram of thickness distribution. □

Circle 168 on Inquiry Card

# MDS 2021/2022 CARTRIDGE TAPE DRIVE -a miniperipheral with big capabilities

We've shed light upon a 3M-compatible\* cartridge tape drive that is in use by more OEM's than any other cartridge drive. It's simple to see why.

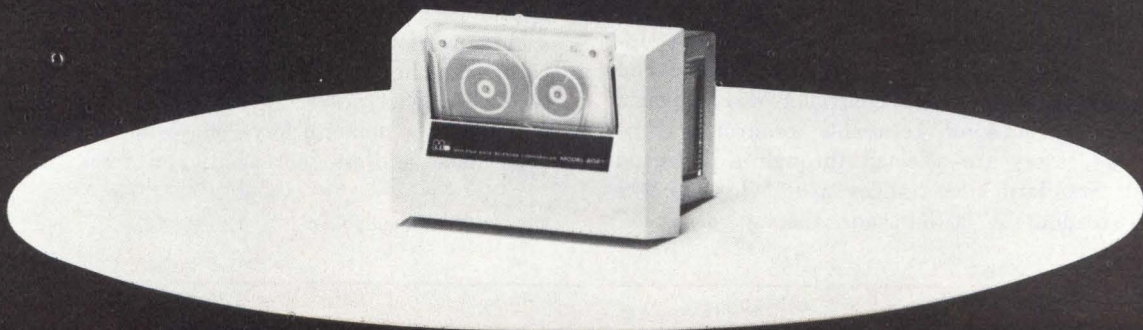
You'll find the flexibility you need for virtually any digital data handling requirement. Features like 30 ips read/write, 90 ips search and rewind, read-after-write checking, 800/1600 bpi recording density, and phase or biphas encoding on 1, 2, or 4 tracks. Storage capacity per cartridge is up to 23 million bits. But there's more to this drive's wide acceptance than meets the eye. Features like interchangeable printed circuit boards, long-life motor, and initial

low cost have made this unit particularly suitable for small system integration where cost/performance, reliability and serviceability are of utmost concern.

Applications like remote data collection, data communications, word processing, POS, and data entry are just a few ways that these drives are handling data in thousands of systems today.

To get all the facts on the MDS 2021/2022 Cartridge Tape Drive, mail the attached coupon, or call us collect today.

\*3M DC300A Data Cartridge



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CIRCLE 35 ON INQUIRY CARD

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# REALTIME PROTOTYPE ANALYSIS AS A MICROPROCESSOR DESIGN AID

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By providing the designer with the ability to build a fully compatible hardware/software system in progressive stages, this design tool helps to isolate problems while the prototype operates at full rated speed

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**Robert Francis and Robin Teitzel**      Tektronix, Incorporated, Beaverton, Oregon

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**W**ith the proliferation of available microprocessors, the designer faces a system development process that poses severe hardware/software integration problems. This process revolves around microprocessor architectural basics. Most functions are stored in memory rather than being implemented in logic components; therefore, a design change is effected rapidly and easily by simply substituting program instructions. In other words, software emerges as the dominant factor in overall microprocessor-based system design. More importantly, software/hardware design becomes a dynamic interactive process and integration emanates as the critical development phase. It is during integration that the potentially substantial savings in design effort, time, and cost can be gained.

Without support equipment assistance, however, the designer encounters unnecessarily complex and time consuming tasks. If microprocessors are selected on the basis of manufacturers' specifications with no way to perform benchmark tests, the designer may not optimally match the best microprocessor to system requirements. Designing a customized debugging tool is expensive, is restrictive in versatility, and does not guarantee that the microprocessor will run properly. Also, generating the entire program for a prototype system runs the risk of mismatch when hardware and software are exercised together, with no means of detecting where or why defects occur.

Alternatively, a comprehensive integration equipment, the 8002 Microprocessor Lab, allows the designer

to build a fully compatible hardware/software system in progressive stages. This development system permits detailed investigation of a microprocessor prototype and its functional programs, and fully tests all elements of the overall system design. Microprocessors that can be analyzed include: 8080A, 6800, Z80, 9900, and 8085A.

Hardware/software debugging techniques in general, and realtime analyses in particular, are explored by describing capabilities of the realtime prototype analyzer (RTPA), an integral proficiency of the microprocessor lab. Primarily useful in the intermediate and final stages of microprocessor-based system integration, the RTPA helps the designer to isolate prototype problems by providing realtime tracings, event comparisons, and expanded breakpoint capabilities. The prototype address bus, data bus, and selected system signals can be monitored simultaneously with the microprocessor executing at rated speed. The designer has complete access to, and control of, internal functions of a prototype system.

## **RTPA Functional Description**

An interconnected realtime trace printed circuit (PC) card, a multclip-lead test probe, and a data acquisition interface panel (Fig 1) comprise the analyzer. The PC card, a special high speed buffer memory, and the interface panel, a data handling module with

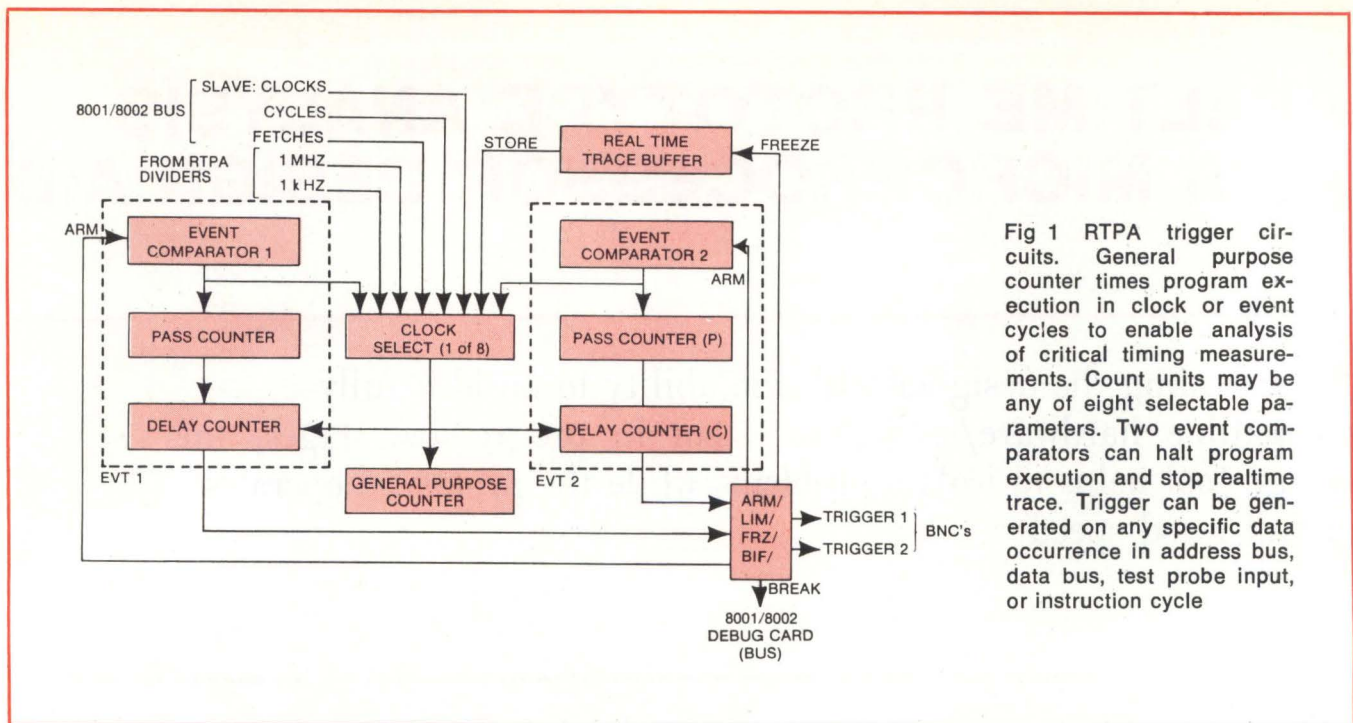


Fig 1 RTPA trigger circuits. General purpose counter times program execution in clock or event cycles to enable analysis of critical timing measurements. Count units may be any of eight selectable parameters. Two event comparators can halt program execution and stop realtime trace. Trigger can be generated on any specific data occurrence in address bus, data bus, test probe input, or instruction cycle

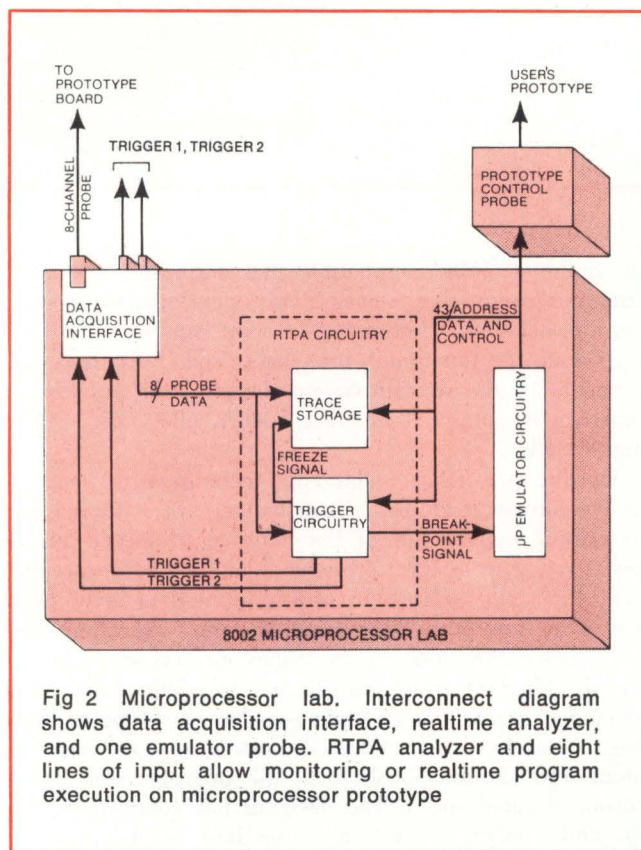


Fig 2 Microprocessor lab. Interconnect diagram shows data acquisition interface, realtime analyzer, and one emulator probe. RTPA analyzer and eight lines of input allow monitoring or realtime program execution on microprocessor prototype

switch selectable transistor-transistor logic (TTL) or variable input threshold levels ( $\pm 10$  V), are installed into the microprocessor lab (Fig 2). High input impedance ( $1 \text{ M}\Omega$  at  $5 \text{ pF}$ ) test probe leads connect directly to the prototype to obtain eight input data channels. Acquired data are picked up and buffered by the test probe, modified by the interface panel,

and driven to and stored in the realtime trace buffer. Logic control circuits for effecting the analyzer's command set (see "RTPA Command Set") are also mounted on the buffer memory card.

When the designer's program executes, 48-bit data words (Fig 3) are sequentially acquired from the prototype and loaded into the realtime trace buffer. Each data word contains 16-bit data from the address bus, 8- or 16-bit data from the data bus, 8-bit data from the test probe extension, 3-bit data identifying cycle type (read, write, input/output, memory, or instruction fetch), and 5-bit data used internally to identify the last start/stop of the emulator processor. Data are acquired synchronous to the microprocessor clock.

The analyzer loads sequential cycles of logic input until the emulator processor is stopped or the realtime trace buffer is frozen by a specified trigger. Using parameters such as A = address bus, D = data bus, T = test probe, and B = cycle type, two event comparators (EVT1 and EVT2) located in buffer memory generate a trigger on any combination of a 48-bit wide transaction.

Pass (P) and delay counters (C) delay triggering by n repetitions of an event occurrence, or by n repetitions of a specific count unit. Clock select defines the parameters in count units of either instruction fetches, bus cycles, emulator clocks, trace stores, microseconds, milliseconds, event 1 compares, or event 2 compares. Clock select also defines the count units of the general purpose counter, which times program execution during a start/stop of the emulator processor.

After event trigger and count values have been designated, the two event comparators initiate a break in program execution. These comparators trigger as independent breakpoints where either or both generate a break, or they may be combined in the ARM, FRZ, or LIM modes (see RTPA Command Set).

## RTPA Command Set

Command (Definition)	Function
BIF (Break if)	Set or clear break options established for event trigger
CNT (Count)	Set or display count units and values
DRT (Display realtime trace)	Display RTT buffer contents
EVT (Event)	Set or display event comparator trigger options
RTT (Realtime trace storage)	Select type of bus transactions to be stored
Parameter (Definition)	Function
ARM (Arm trigger)	If EVT1 occurs, then trigger or break on EVT2
FRZ (Freeze buffer)	Freeze RTT buffer with EVT1 trigger. Break emulation with EVT2 trigger
LIM (Limit trigger)	All conditions of EVT1 and EVT2 must be true at same time before trigger or break occurs

Through two connectors located on the acquisition interface panel, the event comparators also generate an external trigger pulse to a logic analyzer or oscilloscope, allowing the designer to troubleshoot circuitry during program execution while maintaining debugging control through the microprocessor lab.

## Execution Time Capture

In a typical procedure for the 8080A microprocessor, the analyzer is set to capture the execution time between two specified program addresses. A simple timing loop is programmed that repeatedly executes a no-operation (NOP) instruction (Fig 4).

The timing routine is constructed to measure the time interval in microseconds between initiation of the loop cycle and the first occurrence of a NOP instruction output. Various analyzer commands and mode parameters allow effective determination of how long it takes this piece of code to execute.

Event comparators EVT1 and EVT2 are invoked by the event (EVT) command. These comparators trigger to halt program execution and to stop the realtime trace. A trigger may be generated on any specified data occurrence in the address bus, data bus, test probe input, or instruction cycle type. In this application, the two event comparators trigger on two addresses: address location of the initial loop NOP instruction (EVT1 A = 02) and address location of the second NOP location (EVT2 A = 06).

Activated to ensure acquisition of data pertinent to the measurement, the break-if (BIF) command sets break parameters for the two event comparators. These parameters specify whether the two comparators are used as independent breakpoints, or together to enable a breakpoint on a specific event combination. For instance, the ARM mode parameter works as an "If, Then" break condition—if EVT1 occurs, then break on EVT2—thereby limiting the analyzer timing function to a particular section of program execution. The CNT command invokes the general purpose counter and specifies count units—in this application, U for microseconds. When EVT1 occurs, the general purpose counter counts in microseconds until halted by the occurrence of EVT2, thus accomplishing the realtime measurement of program execution.

After the timing routine has been programmed, the GO command is activated to start program execution; all analyzer commands are programmed through the microprocessor lab console. Then, the analyzer monitors prototype activity synchronous to the microprocessor cycle, loading sequential cycles of data into the high speed memory buffer. When EVT1 (address = 02) is triggered, the ARM break parameter is initiated, and the timing function begins. With the occurrence of EVT2 (address = 06), timing is stopped, and a breakpoint is activated as indicated on the console CRT (Fig 5).

When a break in program execution takes place, up to 128 bytes of the most recent program bus transactions are retained in the analyzer memory buffer. Display commands allow a portion or all of this buffer content to be displayed on the console CRT. By utilizing the DRT command, all analyzer buffered transactions—

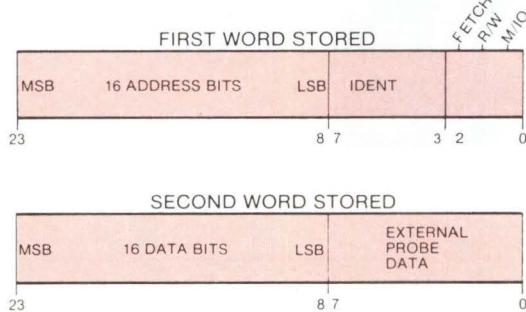


Fig 3 Prototype data word. Data storage format is 48-bit word with 43 bits of pertinent data. Depending on microprocessor prototype, either 8 or 16 bits of data are stored. Bus operation data indicate which cycles are responded to

```

ORG 0
NOP          ; START OF TIMING LOOP
XRA         ; CLEAR ACCUMULATOR
LOOP INR A  ; COUNT TO 256 BY COUNTING BY 1
JNZ LOOP    ; AND DETERMINE IF FINISHED COUNTING
NOP         ; END OF LOOP
END

```

Fig 4 Source code for 8080 timing loop. Register A (accumulator) is used as counter. Program is used to demonstrate timing functions shown in Fig 5

address location, data, probe input, and control bus data—are displayed (Fig 6). If the transaction is an instruction fetch, this instruction is also disassembled into the appropriate mnemonic.

The CNT command is again activated to display the current count value, allowing determination and display of an accurate time measurement of 01619  $\mu$ s (Fig 6).

## Flexible Triggering and Break Logic

An analyzer procedure for an 8080A microprocessor illustrates how flexible breakpoint triggering can be used to monitor a specific portion of prototype execution. In this procedure, analyzer commands are implemented to invoke a memory range routine that effectively moni-

```

> DEB
> EV 1 A=02 ← START COUNTER WHEN PROGRAM ENTERS LOOP
              (INSTRUCTION LOOP INR A)
> EV 2 A=06 ← STOP COUNTER WHEN PROGRAM LEAVES LOOP
              (INSTRUCTION NOP)
> BIF ARM ← BREAK PROGRAM EXECUTION
> CNT U ← COUNT IN MICROSECONDS
> █

```

Fig 5 Timing functions. Analyzer triggering and counter commands needed to time, in microseconds, the loop code of Fig 4 are listed. Execution time between occurrence of address 02 and address 06 is measured

```

> GO 0
LOC INST MNEM OPER SP RF RA RB RC RD RE RH RL
0006 00 NOP 0000 56 00 00 00 00 00 00 00
0006 BREAK

> DRT 10
ADDR DATA MNEMONIC EXTERNAL BUS
0005 00 00000000 M R
0002 3C INR A 00000000 M R F
0003 C2 JNZ 00000000 M R F
0004 02 00000000 M R
0005 00 00000000 M R
0002 3C INR A 00000000 M R F
0003 C2 JNZ 00000000 M R F
0004 02 00000000 M R
0005 00 00000000 M R
0006 00 NOP 00000000 M R F

```

ADDR	DATA	INSTR	DATA FROM PROBES	BUS CYCLE TYPE
> CNT	COUNT=01619 USEC			

```

> █

```

Fig 6 Timing loop execution. DRT 10 command causes last 10 traces in realtime trace buffer to be displayed. Event 2 trigger occurs when address 06 is accessed. COUNT indicates that 1619  $\mu$ s have been spent in loop

tors a particular section of program activity. This routine (Fig 7) stops program execution whenever the program attempts to read from, or write into, a specified range of memory.

With the EVT command, the two event comparators are set to define the boundary addresses of a specific memory range. Relational operators are available to qualify an event trigger as greater than or equal to (>), less than or equal to (<),\* or equal to (=) any specific bit equality. Thus, by setting EVT1 A > 107 and EVT2 A < 109, the analyzer will generate a trigger on any memory address between 107 and 109, inclusive.

Through the BIF command, conditions are set on which a break in program execution is initiated. By

```

ORG 100H ; LOCATE PROGRAM AT 100 HEX
NOP ; DO NOTHING INSTRUCTION
NOP ;
NOP ;
NOP ;
JMP SKIP ; BRANCH AROUND DATA
DATA BYTE 0FBH ; DATA LOCATED AT LOCATION 107
BYTE 0FBH ; DATA
BYTE 0FBH ; DATA LOCATED AT LOCATION 109
ORG 10A ; LOCATE NEXT PORTION OF PROGRAM AT 10A HEX
SKIP NOP ; DO NOTHING INSTRUCTION
NOP ;
LDA DATA ; LOAD A DATA ITEM INTO REGISTER A

```

Fig 7 Do-nothing program. Written in source code appropriate to 8080, program demonstrates capabilities used in Fig 8

activating this command's LIM break parameter, a breakpoint will occur only if the conditions of EVT1 and EVT2 are met simultaneously. In this manner, the program continues to execute as long as the specified range of memory is not accessed.

After the range routine has been programmed through the lab console with all desired parameters, program execution is activated with the GO command. The analyzer monitors program activity around the specified memory range and, as displayed on the CRT, a breakpoint will occur when an attempt is made to load data at address 107.

The analyzer automatically acquires and stores data in a pretrigger format. By using the DRT (display) command, up to 128 byte transactions (stored in buffer memory) that occurred prior to the initiated breakpoint may be viewed.

To view data in a center- or post-trigger format,\*\* the delay counter (C) must be programmed in the EVT command. Clock select sets the delay counter to any one of the eight available count units. By implementing the delay counter as EVT1 A > 107 C = 5, and the clock select as CNT trace stores (T), the trigger is delayed by five trace stores. This then enables a post-trigger position of five for the breakpoint in the analyzer trace buffer. If a center-trigger position is programmed into this application program, the final buffer contents are also displayed (Fig 8).

\*Note that > and < are implemented as  $\geq$  and  $\leq$ , respectively.

\*\*In post-trigger format, up to 128 byte transactions that occurred after the breakpoint may be viewed; in center-trigger format, up to 64 byte transactions that occurred prior to the breakpoint and up to 64 byte transactions that occurred after the breakpoint may be viewed.

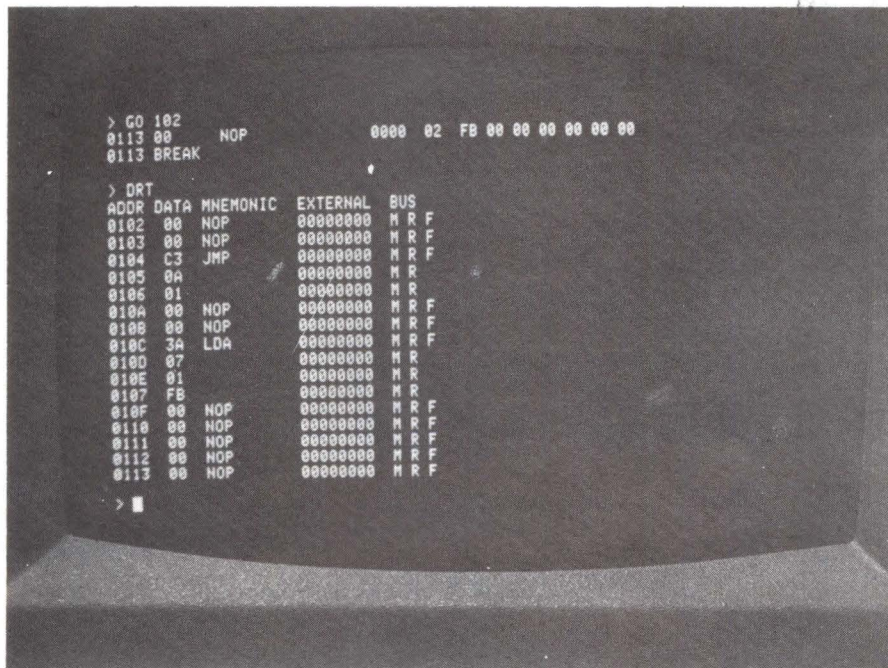


Fig 8 Display of realtime trace buffer. Program flow should always branch around data. RTPA commands (a) EVT1 A > 107 C = 5, (b) CNT T, (c) EVT2 A > 109, and (d) BIF LIM cause break in program execution if data are accessed. Breakpoint occurs five trace stores following initial trigger point at address 0107

## Memory Hardware Examination

To illustrate the procedure for examining memory hardware to isolate a stack overflow problem in memory consider an application program\* that contains Ackerman's Function (see Ralston), a highly recursive subroutine that requires large amounts of stack storage (Fig 9).

The program is written for the 6800 microprocessor, and the assembled listing (Fig 10) indicates both the instruction sequence and the memory configuration. Memory addresses 300 to 3FF\*\* are allocated to main program instruction, addresses 400 to 418 to subroutine instruction, and addresses 419 to 500 to stack storage. When this program is executed, an overflow problem occurs due to the highly recursive nature of the subroutine. Program flow is disrupted when data being loaded onto the stack overwrite memory where pertinent subroutine instructions reside. To isolate this problem, the analyzer monitors program activity within the memory range containing the subroutine data.

With the address bus (A) parameter, the two event comparators are set to define the limits of the desired memory range. The first is set to trigger if address bus data are less than or equal to 418 (EVT1 A < 418), and the second to trigger if address bus data are greater than or equal to 400 (EVT2 A > 400). This range ensures that the analyzer will generate a trigger when access is made to any address between 418 and 400, inclusive.

Since this application concerns a stack overflow problem, triggering conditions are further limited to

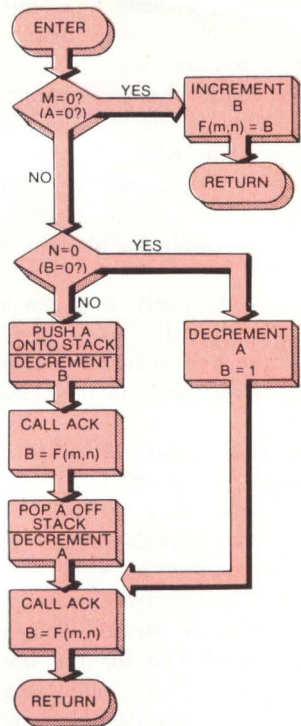


Fig 9 Ackerman's function ACK (M, N) for 6800 processor. If  $M = 0$ , then  $f(m,n) = N + 1$ . If  $N = 0$ , then  $F(m,n) = F(m-1, 1)$ ; otherwise,  $F(m,n) = F(m-1, F(m,n-1))$

\*The program used is from "Class Notes on Data Structures," Naising Deo, Washington State University, Fall 1974.

\*\*All memory addresses are in hexadecimal notation.

```

00001 0028 M EQU 40 ; SET M EQUAL TO 40 (DECIMAL)
00002 0028 N EQU 40 ; SET N EQUAL TO 40 (DECIMAL)
00003 0300 ORG 300H ; START PROGRAM AT LOCATION 300 HEX
00004 0300 BE0500 START LDS # STACK ; INITIALIZE STACK POINTER
00005 0303 8628 LDA A # M ; LOAD A & B REGISTERS
00006 0305 C628 LDA B # N
00007 0307 B00400 JSR ACKER ; CALL ACKERMANS FUNCTION
00008 030A 01 NOP
00009 030B 01 NOP
00010 030C 7E0300 JMP START
00011 0400 ORG 400H ; LOCATE ACKERMANS FUNCTION AT 400 HEX
00012 0400 8100 ACKER CMP A #0H ; IF A=0
00013 0402 2602 BNE ACK 1
00014 0404 5C INC B ; THEN SET B=B+1
00015 0405 39 RTS ; RETURN
00016 0406 C100 ACK1 CMP B #0H ; OTHERWISE; IF B=0
00017 0408 2606 BNE ACK 2
00018 040A 4A DEC A ; THEN SET A=A-1
00019 040B C601 LDA B #01H ; SET B=1
00020 040D 8DF1 BSR ACKER ; CALL ACKERMANS FUNCTION
00021 040F 39 RTS ; RETURN
00022 0410 36 ACK2 PSH A ; OTHERWISE; SAVE A ON STACK
00023 0411 5A DEC B ; SET B=B-1
00024 0412 8DEC BSR ACKER ; CALL ACKERMANS FUNCTION
00025 0414 32 PUL A ; RECALL OLD A FROM STACK
00026 0415 4A DEC A ; SET A=A-1
00027 0416 8DE8 BSR ACKER ; CALL ACKERMANS FUNCTION
00028 0418 39 RTS ; RETURN
00029 0500 ORG 500H
00030 0500 0001 STACK WORD 1 ; STACK AREA ENDS AT LOCATION 500 HEX
00031 END
  
```

Fig 10 6800 macro assembler listing of program for Ackerman's function. On entering function, M is in register A and N is in register B. On exit from routine, register B contains result ( $B = F(m,n)$ ). Since function is a recursive algorithm, variables are temporarily stored on stack



```

> DRT 20
ADDR DATA MNEMONIC EXTERNAL BUS
0407 00 00000000 M R
0408 26 BNE 00000000 M R F
0409 06 00000000 M R
040A 4A DEC A 00000000 M R F
040B C6 LDA B 00000000 M R F
040C 01 00000000 M R
040D 8D BSR 00000000 M R F
040E F1 00000000 M R
0418 0F 00000000 M W ← STACK OVERFLOW AT THIS POINT
0417 04 00000000 M W
0400 81 CMP A 00000000 M R F
0401 00 00000000 M R
0402 26 BNE 00000000 M R F
0403 02 00000000 M R
0406 C1 CMP B 00000000 M R F
0407 00 00000000 M R
0408 26 BNE 00000000 M R F
0409 06 00000000 M R
0410 36 PSH A 00000000 M R F
0416 11 00000000 M W
> █

```

Fig 11 Display of analyzer buffer contents. Initial trigger point, stack overflow, and trace of following instructions are indicated. Stack overflow occurs at location 0418. As defined by commands, 10 post-trigger traces have been stored in the trace buffer

the occurrence of memory write instructions only. This limitation is accomplished by the EVT command's instruction cycle type (B) parameter. By designating B = MW (break on memory writes only) as an additional qualifier for both event comparators, a trigger will be generated only when an attempt is made to write data within the specified memory addresses.

The analyzer automatically acquires and stores data in a pre-trigger position. In this application, however, program activity is viewed following the initial trigger point. To do this, a triggering delay must be implemented with the EVT command delay counter (C) parameter. In this case, triggering delay is set as 10 (C = 10). Then, with clock select, the value of the delay counter is set equal to trace stores (CNT T). This procedure ensures that the analyzer will continue to acquire data after the initial trigger occurrence, and will enable a post-trigger position of 10 trace stores (Fig 11).

After triggering specifications have been determined, the BIF command designates the conditions on which a break in program execution is initiated. For this application, BIF LIM is implemented. This mode parameter specifies that a breakpoint will occur only if the triggering conditions of EVT1 and EVT2 are met simultaneously.

By using triggering and break logic in this manner, a localized monitoring routine is devised that will isolate the stack overflow problem. The two event comparators define the monitoring range, with triggering dependent on memory write instructions only. Furthermore, with delay counter and clock select, triggering is delayed to enable a post-trigger acquisition of 10 trace stores. Then, to ensure capture of pertinent data, the LIM break parameter specifies that a break in program execution will occur only if all triggering conditions are met.

With the GO command, program execution and real-time trace are initiated. The analyzer monitors program activity synchronous to the processor cycle, and loads sequential cycles of data into the realtime trace buffer. When stack overflow occurs, data are pushed into the memory area containing subroutine instructions, and the event trigger is activated. Because of the designated trigger delay, program execution continues for 10 additional trace stores before a breakpoint is generated. Next, the DRT display command is used to specify that the last 20 transactions, including the 10 post-trigger traces, be displayed as shown in Fig 11.

The sequence of events shown in Fig 11 depicts the initial trigger point—a memory write instruction changes

```

> GO 0
LOC INST MNEM OPER SP RF RA RB RC RD RE RH RL
0038 C5 PUSH B 0240 56 0F 00 00 02 00 02 40
003B BREAK

> DRT 15
ADDR DATA MNEMONIC EXTERNAL BUS
0062 FF 00000000 M R ← INTERRUPT OCCURS
0249 00 11111111 M W ] PC STORED ON STACK
0248 62 11111111 M W
0038 F3 PUSH P 11111111 M R F ← INTERRUPT ROUTINE
0247 0F 11110101 M W
0246 56 11110101 M W
0039 E5 PUSH H 11110101 M R F
0245 02 11100101 M W
0244 40 11100101 M W
003A D5 PUSH D 1100101 M R F
0243 02 11010101 M W
0242 00 11010101 M W
003B C5 PUSH B 11000101 M R F
0241 00 11000101 M W
0240 00 11000101 M W ← STACK OVERFLOW

```

Fig 13 Instruction by instruction trace. After trace of portion of program shown in Fig 12, breakpoint information and last 15 transactions stored in realtime trace buffer are displayed at system console. Transactions show occurrence of interrupt and point of stack overflow at address 0240

```

ORG 024AH
STACK EQU $
DSPPTR BLOCK 2 ;OUT DISPLAY POINTER
CURPTR BLOCK 2 ;KB DISPLAY POINTER
ADDR BLOCK 2 ;KB ADDRESS FOR DSPLY
TEMP BLOCK 2 ;KB NUMBER TEMP
DIGCNT BLOCK 1 ;KB COUNTER
MODE BLOCK 1 ;KB MODE OF OPERATION
SPSAVE BLOCK 2
DSPDATA BLOCK 6
END

```

Fig 12 Source code error. Segment of source code indicates designer's error in setting stack location (ORG 024AH). Stack space should have been assigned to begin at address 10FFH.

data located at address 0418. Two solutions to this problem would be to either increase memory stack space or, perhaps more feasible, substitute a less recursive algorithm.

### Program Instruction Problem

A second application example demonstrates a procedure for tracking down an overflow problem in memory. The program for this application is interrupt driven; ie, an 8080A microprocessor has been programmed to respond to external signals.

Assume that while coding this program the designer made an error that effects the memory configuration. Main program instructions are allocated to memory addresses 0000 to 023F, and stack space is intended to begin at address 10FF (Fig 12). In the ORG statement that sets stack location, however, the designer has entered an incorrect operand (024AH) that moves

stack storage space directly below program data, address 024A. This error is shown in the segment of original source code.

When the program is tested with prototype hardware, difficulties arise due to the initial programming error. Program flow is disrupted at random since, whenever an interrupt occurs, data being loaded into the stack are, in effect, overflowing into main memory. To isolate this problem, program activity during an actual interrupt sequence must be monitored. With the analyzer command set, a routine is implemented that will allow capture of a snapshot view of software and hardware functional elements leading up to the overflow problem.

With the analyzer EVT command, the conditions on which a trigger is generated are specified. For this application, only one of the two event comparators is needed. It is set to trigger if address bus data are less than or equal to the upper address limit of stack storage. By designating EVT1 A < 240, a trigger will be generated if access is made to any address located beyond the intended stack space, thus limiting triggering conditions to the section of memory that contains main program instructions. The event trigger is further qualified as to the type of instruction being executed. Using the instruction cycle type (B) parameter, a trigger is generated only when the attempt is made to write data within the designated memory addresses. By implementing B = MW with the event command, triggering conditions are limited to the occurrence of memory write instructions only.

With triggering conditions defined in this manner, the BIF command is implemented to ensure capture of pertinent information. Since only the first event comparator is used, this command is set to generate a breakpoint on the occurrence of EVT1. Thus, a break in program execution will take place immediately if the event trigger is activated.

Through manipulation of analyzer commands, a routine is developed that will isolate the stack overflow problem. First, using only one event comparator, a trigger will be generated if data are written into any address located outside the intended stack space. Then, by designating an immediate breakpoint, the capture of program activity leading up to the overflow problem is ensured.

After analyzer commands and parameters have been programmed, the GO command is activated to start program execution. The analyzer traces prototype activity in real time, monitoring the specified address locations for any occurrence of a memory write instruction. When the prototype hardware generates an interrupt, the 8080A microprocessor responds to this signal, and data are pushed into stack storage. When the interrupt call is executed, a stack overflow problem occurs almost immediately.

For this application, the DRT command displays the last 15 transactions stored in the realtime trace buffer

(Fig 13). This display shows initial trigger occurrence, a memory write at address 0240, and the sequence of events that preceded the overflow. It is easy to locate the point at which an interrupt is called, and further analysis indicates that data have been loaded too close to the main program. Therefore, the stack space needs to be increased; that is, moved from 024AH to 10FF.

## Summary

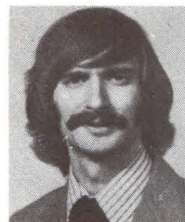
In many hardware/software integration applications, the RTPA has proved to be an efficient support aid to the designer of a microprocessor based system. The tool allows the designer to evaluate prototype activity through an accurate measurement of execution time, center in on a particular area of program execution without spending hours single-stepping through complex software code, view many aspects of software and hardware states while the microprocessor operates at full speed, and capture realtime signals external to the microprocessor to analyze the relationship of the microprocessor to outside events. Several application procedures emphasize the system's dynamic capabilities and how they can be used to enhance the hardware/software interaction process of microprocessor system design and development.

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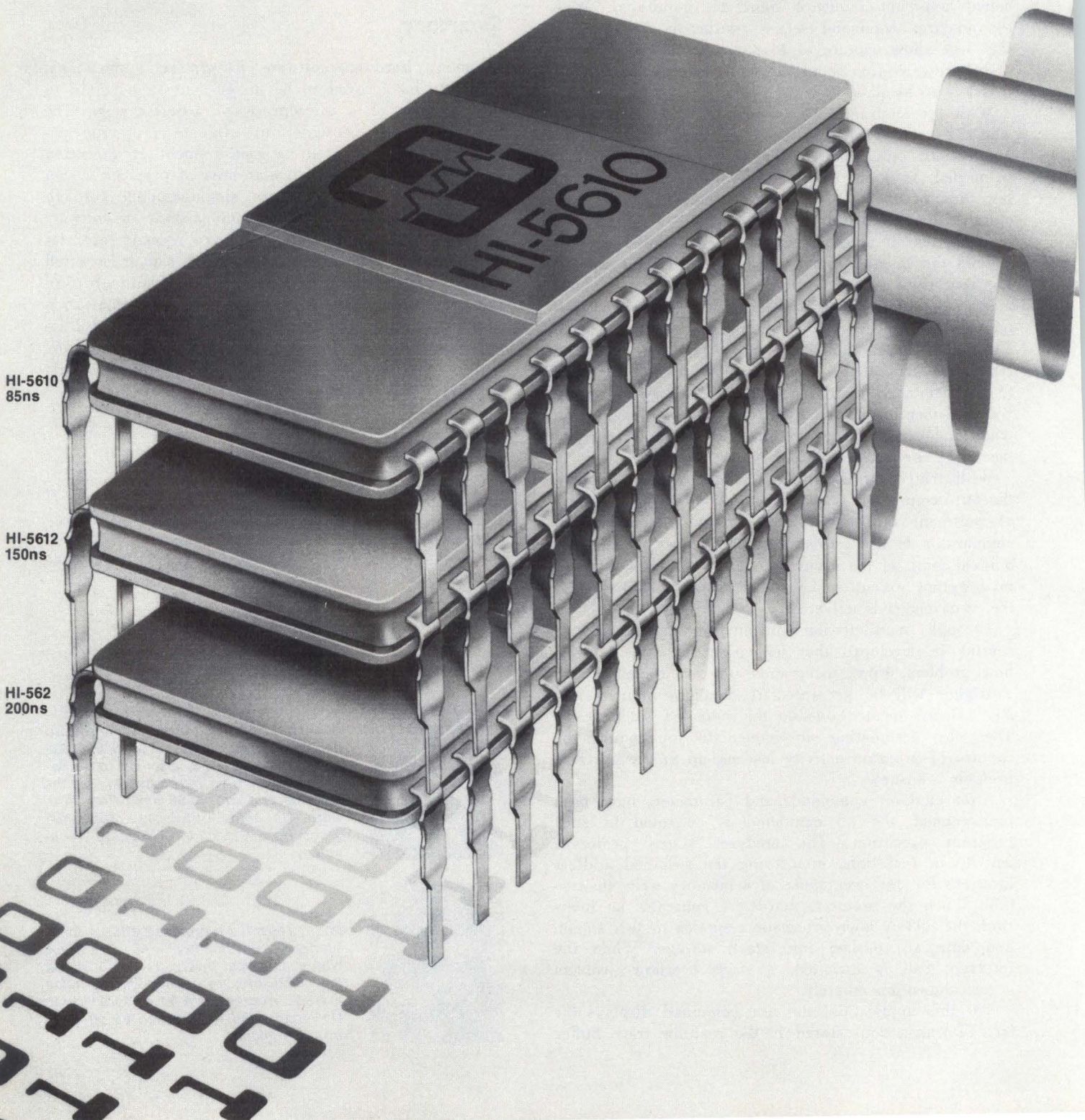


Robert S. Francis, currently hardware design project leader for 8001/8002 microprocessor labs, also has been involved with hardware design of the systems and with 8085 emulation hardware. He holds BSEE and MEEE degrees from Clarkson College of Technology.



Robin Teitzel is a project leader in logic analyzer development at Tektronix, where he was involved previously in the 8002 software evaluation. He holds a BSEE degree from Washington State University, and has worked as an electronic engineer.

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HI-5610  
85ns

HI-5612  
150ns

HI-562  
200ns

# STACK.

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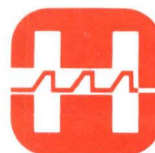
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Bits	12	12	10
Settling Time to $\pm 1/2$ LSB	200 ns typ	150 ns typ	85 ns typ
Differential Linearity (0-75°C)	$\pm 1/2$ LSB max	$\pm 1/2$ LSB max	$\pm 1/2$ LSB max
Low Gain Drift (0-75°C)	$\pm 5$ ppm/°C	$\pm 5$ ppm/°C	$\pm 5$ ppm/°C
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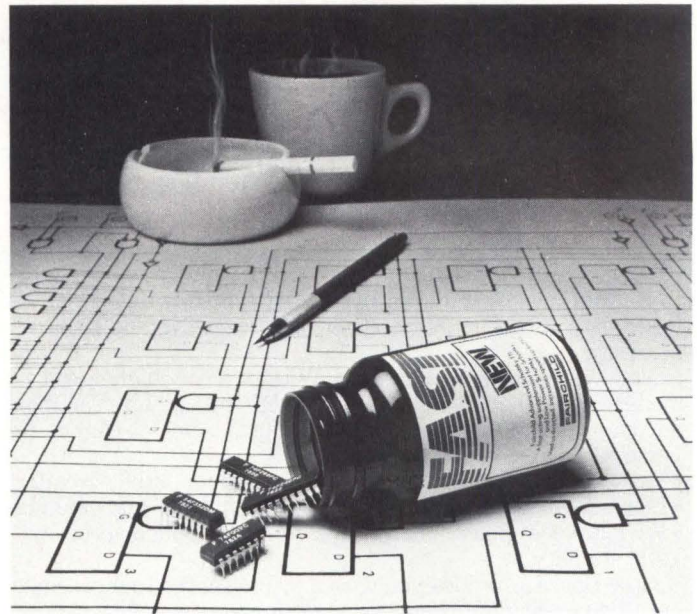
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74F02PC	2.6	3.5
74F04PC	2.5	2.7
74F08PC	3.6	4.1
74F10PC	2.7	2.9
74F11PC	3.7	4.2
74F20PC	2.8	2.9
74F32PC	3.5	3.9
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# INTEGRATING PERIPHERALS INTO PROCESSING SYSTEMS

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Diversified integration of peripherals into a processing system can be approached from the point of dedicated hardware to a particular controller function, dedicated software requiring only I/O lines, or a combination of both with a partially dedicated CPU and enough software to customize the I/O device functions

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**O**f three design approaches to the integration of peripherals into processing systems—dedicated hardware, dedicated software, and a combination of the two—the first is usually fastest in speed of execution. Reading or writing a disc file can be accomplished by setting direct memory access controller pointers to the data and issuing a start command. An interrupt circuit is another example, since this function is performed totally in central processing unit hardware. With the total hardware approach, very little software is required to perform relatively major tasks. To be economical, high volumes are needed for such dedicated custom chips, for which no second sourcing is likely. However, if high volumes are the case, the dedicated hardware approach would be least expensive.

In the total software control approach, general purpose input/output (I/O) chips perform universal interface functions by customized programs. For example, the chips are used in handshake operations to indicate incoming or outgoing data; however, the software uniquely defines their functions. Although the total software approach can be implemented quickly—in several days usually, compared to weeks or months for dedicated hardware—it is probably the slowest of the three approaches in speed of execution. Cost is normally small, especially if unused capabilities exist in the system, such as memory or I/O lines. Otherwise, incremental hardware must be purchased, such

as extra memory. Implementation of this approach is feasible in low volumes.

Between the total hardware and total software approaches lies a broad area in which standard central processing units (CPUs) are customized with software to perform peripheral integration functions. A second CPU would relieve the main CPU of the peripheral control burden, thus permitting more sophisticated programs to be executed by the main CPU. The expense of this approach depends on particular circumstances, and implementation may be in low volumes.

## Methods of Data Transfer

The need for transferring data and information exists regardless of the method of I/O control. Peripheral interfaces require data transfer between the main CPU and the peripheral device. The following methods of transferring data and control from the main CPU to the peripherals should be considered.

*Normal software operation*—Peripherals are polled in sequence by the CPU for service needs, and individual inputs are switched. The advantage is that the CPU program is totally in control of the sequence of events. This makes for simple programming. The service sequence is fixed by the program. The disadvantage is that a high speed device must wait its turn in the

polling sequence while other devices are serviced. Total time around the loop must be short enough to handle the high speed device requirements, which may not always be possible. This method may be used to control status lamps, selection switches sensed only at power on, and other devices with low service requirements.

*Programmed I/O handshake operations*—When the CPU outputs data, it also causes a control pin to be set, which indicates that data are available in an output register. The addressed peripheral senses this control signal, accepts the data, and signals this acceptance on a second control line. This method is faster than the normal software operation because the additional hardware takes over the task of determining whether or not the data transfer is complete. The I/O device and CPU are synchronized, and both run at a speed determined by the slower of the two. This method can be used for applicable response time and data transfer speeds to implement many medium speed devices, such as printers or alphanumeric displays, or for intersystem communications.

*Interrupt driven*—In general, the peripheral generates an interrupt signal to the CPU, causing the CPU to stop processing and to execute an interrupt service routine. Using this service routine, the CPU reads the data, processes them, and then returns to the interrupted task. Faster than the first two, this process allows the servicing to be ordered by the peripheral devices. However, more hardware usually is needed, and the programming may be complex. In general, it is used where response is required on an irregular basis, eg, with card readers, since the card must be read as it moves through the read station. In other words, immediate service is required because the card is read "on the fly."

*Direct memory access (DMA)*—In general, access to peripherals is handled easily through a DMA controller, significantly lightening the burden on the CPU. This approach is the fastest, since the CPU does not participate in the data transfer. The controller is in charge of data transfer, and since that is its only task, it can be built for speed. It should be able to run at the access time of the memory, which is five to ten times faster than if the CPU were to make the transfer. The main disadvantage of this approach is the increased cost of the DMA controller. It is an additional part in the system and may increase the complexity of the memory interface.

A novel application of DMA is an N-key rollover function for an encoded keyboard. Key stacking is performed via the DMA by assigning a block of memory to the keyboard input and pointing the controller to the beginning of the block. A 1000-key rollover is put into operation by assigning a variable length stack and using DMA to access the storage locations. After the CPU has processed the keys, it moves the DMA controller pointer back to the beginning of the key stack.

In the real world, combinations of all four methods of data transfer may be used together to implement an I/O device control. An example might be a floppy disc controller, where the normal software operation or programmed I/O handshake would be used to load

control registers. The DMA method would be used for data transfer, and the interrupt driven I/O would be used to signal completion of the operation and need for a new command. Realtime requirements of this device may entail the combined use of these methods, as well as its increased cost.

## Total Hardware Approach

Dedicated hardware control for peripheral integration is a collection of logic gates specifically designed to provide a particular data transfer function. The CRT controller (which controls the timing for scanning, displays, etc) and the floppy disc controller are dedicated hardware. In general, they must be parts that will experience high usage at high speed, and have a well-defined task. In some applications, it may not be possible to determine from the functional specifications whether a controller is dedicated hardware or a programmed CPU. Fig 1 is a block diagram of a floppy disc controller that represents the dedicated hardware approach.

Custom hardware is expensive and requires a lead time of six to nine months to produce. However, it provides the fastest form of peripheral integration and requires the least amount of software. The primary reason for designing new hardware controllers is the time factor of CPU loading. In many instances, the speed (throughput) of CPU technology does not permit the interface to be handled in software, even with a dedicated CPU. A dedicated hardware approach, for a given technology, is faster because the hardware takes advantage of the custom data path and parallelism of the hardware controller, but does not require the instruction fetch time. Only execution time is required.

Hardware is selected over software processing because of the software complexity required to simulate some logic functions. If program size exceeds the memory space available in a single controller or microprogrammed chip, a new hardware design is justified. If the hardware controller under consideration already exists, the capabilities of the CPU may be extended through use of dedicated hardware to control the peripherals at minimum cost.

As microprocessors become faster and more powerful, the gap between the total software and total hardware approaches is closing. More realtime physical phenomena are now falling within the range of programmed control. A dot matrix printer controller is an example of total software control by programming. Another example is the counting loop in an R6500 n-channel microprocessor.

An example of dedicated hardware, a 1-MHz up/down counter, has been placed on a PPS-4/1 chip and runs essentially in parallel with the microprocessor. A quadrature input mode allows this counter to be used for many industrial control applications without additional logic. Typical applications may use an optical encoder, such as numerically controlled machine tools. This chip with the counter may also be used in scales and other weighing devices, or in counting or speed/position controlling operations in industrial applications.



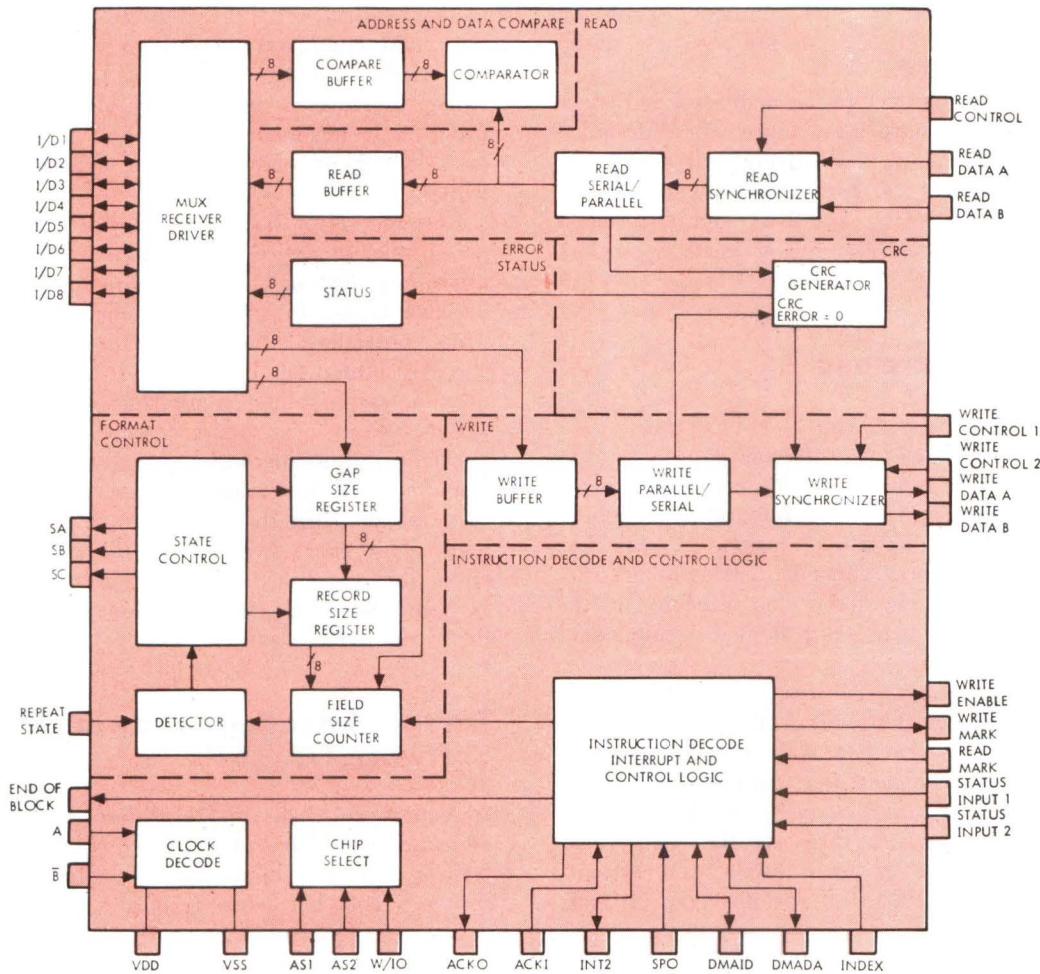


Fig 1 PPS floppy disc controller. Dedicated hardware approach is demonstrated by controller implemented with fixed logic. It controls formatting, error check address comparison, and data transfer between PPS-8 microprocessor memory and IBM 3740 formatted floppy disc. Operation is performed in parallel with normal CPU operation so that only 12.5% of system time is required during actual data transfer

## Total Software Approach

In a total software approach, a main CPU program is responsible for the peripheral control task, and only general purpose I/O lines are needed [Figs 2(a) and (b)]. Generally, the software approach is used for functions that are relatively slow and simple, like those involving human interaction with the microprocessor, such as operating a keyboard.

If only output switching is required, the CPU could perform the task in the same amount of time that it would take a dedicated controller. However, for most tasks, several instruction fetch and execution operations are required, each taking several cycles. The software approach also generates a high load on the CPU time, and software must be written for the main CPU.

The software approach is the lowest cost approach, especially if unused ROM and I/O pins exist. General purpose I/Os, such as parallel interface adapters (PIAs) and serial channels, have nonspecialized functions at low cost. These devices are produced in high volume, and nonspecialization allows for small die size.

Very short lead times are provided by the software approach. Depending on the control, it may be possible to write a software routine and debug it in a matter of hours, if off-the-shelf peripherals and existing memory can be used. It is possible to execute a function stored in RAM as soon as the program is written into the system. If the required RAM and I/O lines already exist in the system, the program could be stored offline, on floppy discs for example.

Design care is needed to include only enough power (and expense) in the main CPU to justify the system task—and no more. It is easy to spend more on the CPU expecting to justify the increased cost and software to handle an I/O function. A better approach may be to offload the CPU, or to use two less costly CPUs to handle I/O functions.

Peripheral controllers, primarily dedicated hardware just a few years ago, are now more often designed as a custom program in a relatively universal CPU. Printers and cassette tapes, for instance, can now be handled totally in software. Figs 2(a) and (b) depict a keyboard scanning technique using general purpose I/O software control.

## Combined Hardware and Software Approach

The combined hardware and software approach (Fig 3) generally uses a standard CPU with customized software to handle the peripheral integration function. A CPU dedicated to a particular task is not as fast as a customized hardware controller. Several instructions may be required to fetch and execute in the CPU, while in custom hardware a single execute could perform the same function.

To use a dedicated CPU requires only that the controlling program be written within the CPU and that the main program be provided with a communication program to the CPU. The increased parallelism of using multiple CPUs allows multiple tasks to be handled. However, a second CPU also increases the cost.

The application trend is to multiple CPU systems with each CPU dedicated to a specific control task.

Again, this is due to an increase in the speed and power of the CPU, in particular to the advent of the 1-chip microprocessor. With one chip, it becomes reasonable to put custom programming into read-only memory (firmware). Less programming is needed for the main CPU, but read-only memory (ROM) codes are needed for the particular 1-chip peripheral controller function in question. In some cases, a dedicated program is included with the one chip, as for turning the PPS-4/1 or 6500/1 into a dedicated printer controller.

Lower costs of fast and powerful microprocessors increase the range of applications. A new device is a microprogram controller, in which a CPU design may be customized to perform a dedicated I/O function. This controller, although similar to a multichip bit slice, is preferable because it is a 1-chip system and does not suffer intercircuit delays. At least a 10-to-1 speed "penalty" is incurred when going to more than one chip due to increased circuit capacitance. Propagation of carry, for example, takes place 10 times faster on a single chip than between chips. With bit slices, eight 1-bit slices are needed for one byte, two 4-bit slices for one byte, etc. The microprogram controller is being used in several custom controllers, such as floppy disc controllers.

## Factors Affecting Hardware/Software Tradeoffs

In determining whether to choose dedicated hardware, dedicated software, or some combination of the two, tradeoff factors should be evaluated. Availability of software and hardware resources, main CPU loading,

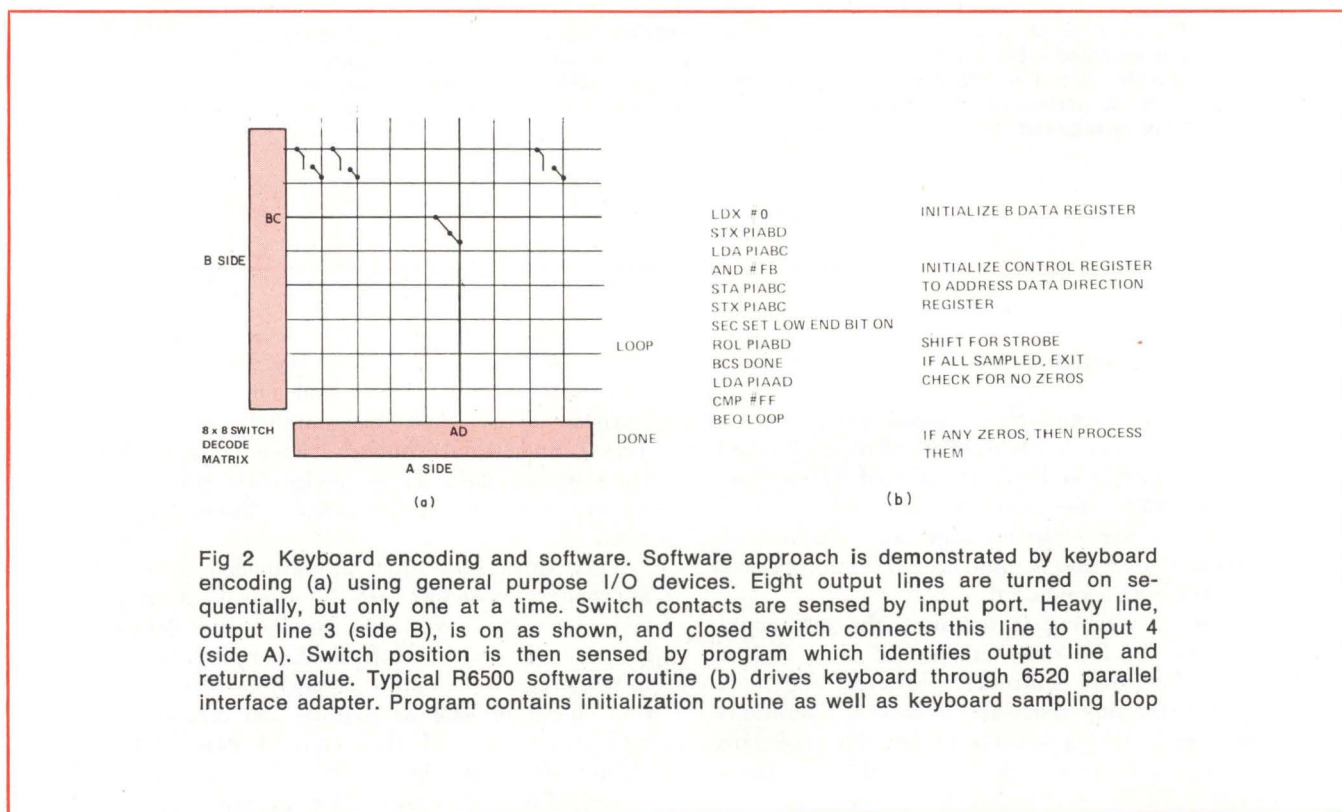


Fig 2 Keyboard encoding and software. Software approach is demonstrated by keyboard encoding (a) using general purpose I/O devices. Eight output lines are turned on sequentially, but only one at a time. Switch contacts are sensed by input port. Heavy line, output line 3 (side B), is on as shown, and closed switch connects this line to input 4 (side A). Switch position is then sensed by program which identifies output line and returned value. Typical R6500 software routine (b) drives keyboard through 6520 parallel interface adapter. Program contains initialization routine as well as keyboard sampling loop

time restrictions, and costs are prime factors impinging upon the selection.

### Resource Availability

**Software resources**—If staff programmers cannot program the desired I/O function, then consultants must be contracted to aid in the interfacing task. Otherwise, a complete peripheral must be bought to perform the particular function. For instance, a matrix printer with either a dedicated hardware controller or a custom

program microcomputer can handle the details of print control.

**Hardware resources**—A floppy disc controller, for example, may be available if that function is needed. Certain tasks then are offloaded from the main CPU onto dedicated peripheral controllers; other controllers include keyboard encoders, printers, and serial communication boards. They permit the main CPU to perform increasingly complex tasks. This is not a feasible approach, if no dedicated controller is available, ie,

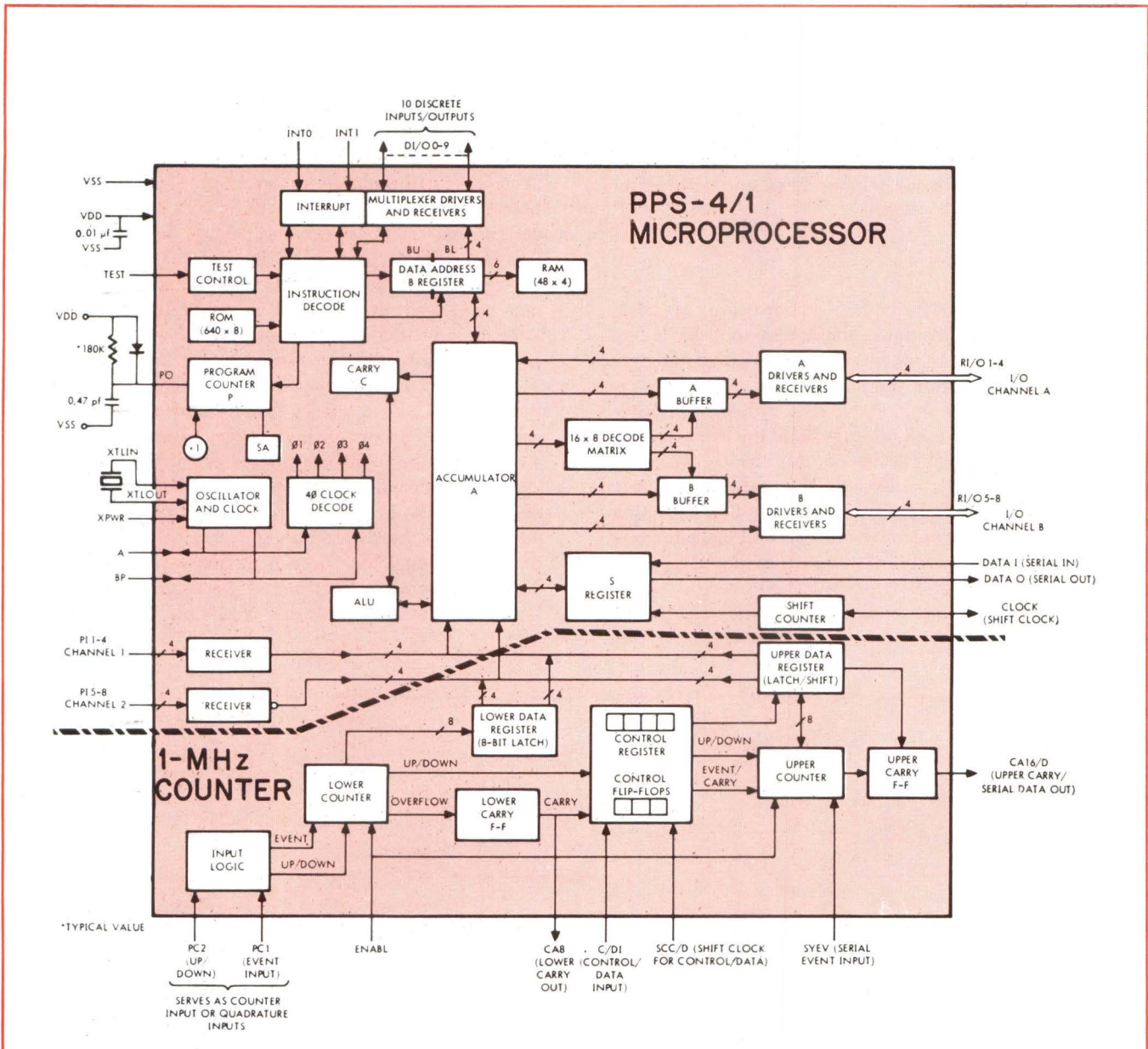


Fig 3 General purpose microprocessor with counter. Combined hardware/software approach is illustrated by microprocessor combined with dedicated hardware up/down counter. Instruction added to PPS-4/1 microprocessor instruction set allows processor to access counter, which has 8-bit 1-MHz up/down counter and lower speed counter. They may be used separately or connected together to provide full 16-bit up/down counter. High speed counter inputs may be used as both count input and direction control input, or may be used in quadrature mode where two input signals of same frequency have 90° phase shift between them. Latter type of input is found in relative position encoders such as shaft angle encoders

to control a spectrum analyzer. When software drivers are available, they obviously do not have to be reconstructed with teletypewriter drivers, for example.

### Main CPU Loading

A CPU bound system (ie, the CPU is fully loaded and cannot accept any more software) may be relieved by additional hardware to perform some of the peripheral functions. In a printing function, an auxiliary CPU could be dedicated to a particular peripheral controlling task. The cost of hardware versus a relatively free software controller is offset by the increased throughput of the CPU.

The opposite of being CPU bound is being I/O bound (ie, the CPU is idle most of the time, waiting for data). This situation can be overcome by having the CPU perform some of the peripheral functions by obtaining the data itself. If the program is waiting for keyboard input, it may be better to have the CPU perform the keyboard encoding function [Figs 2(a) and (b)] rather than use a dedicated keyboard.

### Time Restrictions

Time restrictions may dictate a hardware approach. In some realtime situations, there may not be enough time for input, test, and output, which could take several CPU cycles. For the floppy disc controller, current microprocessors that use a total software approach are not capable of maintaining both the data transfer rate and the data checking of IBM 3740 compatible floppy discs. In this situation, the use of dedicated hardware is justified. In the case of PPS-8 microprocessors, the floppy disc controller performs all tasks for reading and writing a sector of data from the floppy disc into memory. That is, it reads track and sector identification information, monitors the cyclic redundancy

check characters to verify the information, and when the desired address is encountered, transfers and checks the data. All these functions are performed on a variable track format, variations of which include full IBM 3740 compatibility. The disc control task runs independently of the main CPU.

### Costs

Primary factors affecting cost as the designer moves from a total software to a total hardware approach are (a) programming time and effort; (b) ROM mask charges or programmable ROM (P/ROM) programming charges, if software is not loaded into random-access memory (RAM); (c) hardware design; and (d) for the total hardware approach, expensive design and development costs of integrated circuit (IC) vendors or metal-oxide semiconductor/large-scale integration designers. When machine time and software space are available, the software approach should be least expensive. Furthermore, in estimating a programmer's time as opposed to a logic designer's time, even if the design time is approximately equal, hardware fabrication time must be added in order to customize the devices. When software is written and debugged, it can be placed in RAM and is ready to start working; after a logic design is completed, however, the masks and semiconductor processing must then be started.

In general, it is inexpensive to purchase ROM. Memory device costs are a direct function of area. Since ROM cells are an order of magnitude smaller in size than RAM cells, the cost per bit is accordingly less.

ROM incremental costs must also be considered. For instance, if the program overflows the memory boundary, adding extra hardware would suffice. However, the cost of an additional byte or two of ROM over the boundary, 4k at present, is expensive because area must be bought in increments; this situation is also true of

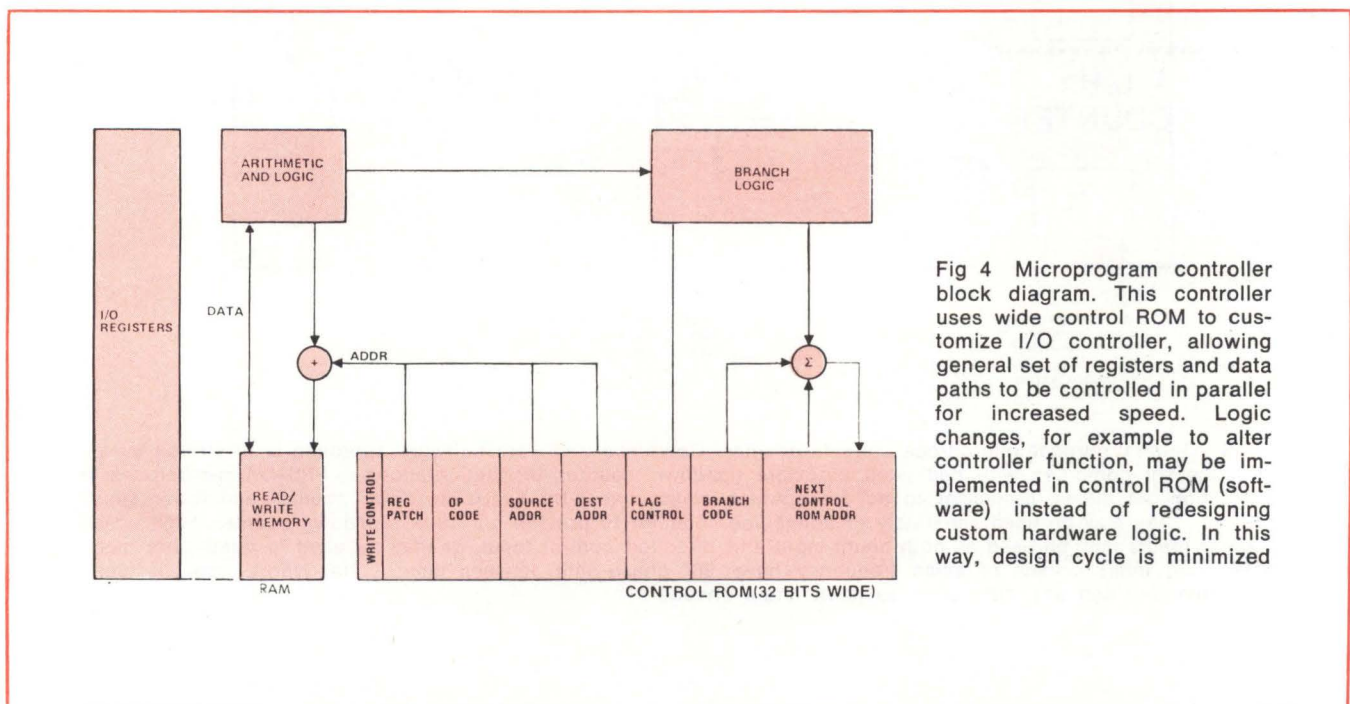


Fig 4 Microprogram controller block diagram. This controller uses wide control ROM to customize I/O controller, allowing general set of registers and data paths to be controlled in parallel for increased speed. Logic changes, for example to alter controller function, may be implemented in control ROM (software) instead of redesigning custom hardware logic. In this way, design cycle is minimized

RAM space. As ROMs get larger than 4k, the boundary problem will lessen. Incremental costs also apply to I/O lines. Both memory and I/O lines are available in fixed quantities. If the boundaries are exceeded, as with memory, an additional I/O line will be expensive, and may not even be available.

If the volume requirement of the user's application is large, then development costs are justified since the unused functions of the main or secondary CPU can be eliminated. This elimination will result in reduced chip area. Most applications not limited by the speed factor being state-of-the-art (ie, if the application can be handled by software at one-tenth of the CPU clock speed) can be accommodated by the general approach of a secondary CPU, as for example, the 1-chip microprocessor or microprogram controller. Another condition would be when the cost difference between a secondary CPU and a dedicated hardware controller is in favor of the secondary CPU.

## Microprogram Controllers

A microprogram controller (Fig 4) customizes the instruction set toward a particular task. One of the characteristics of microprogram controller architecture is a very wide word (32 to 40 bits) in the control ROM. Individual bit fields are used to control the specific registers within the machine. Thus, by encoding the control ROM, the controller may be customized to perform specific tasks and become minifloppy disc controllers, printer controllers, and communications interfaces. Another characteristic of the architecture is that each instruction requires only one word of microcode and executes in one clock cycle. By contrast, conventional fixed architectures may require several CPU clock cycles and many memory accesses to perform an equivalent instruction.

Since direct control of all gates and registers is available, it is possible to create combined operations or instructions in the microprogrammed architecture. Microprogrammable control allows a standard layout of registers and control gates to be customized for a desired logic function, eg, the microprogram controller contains special instructions to perform the cycle redundancy calculations used in discs and communications interfaces.

Two classes of microprogrammable control are a fixed control store coded in ROM, with a 32- to 40-bit or wider word, and a writable control store coded in RAM, which may also be a wide control word, 32 to 40 bits. The latter is used in an emulation function or a variable operation. The flexibility of loading a task to any of a number of different microprocessor controllers is available; however, the writable control store operations in microprogrammable controllers have not been successful to date.

The reason for staying in fixed control stores is that, for a given chip area, ROM of an order of magnitude greater than RAM is available. This means that if 1k bytes of control store are needed in ROM, it would be one-tenth the size needed in RAM. Therefore, it is preferable to stay with a fixed control store to be able to handle a more sophisticated control task because of larger ROM.

In microprogramming, addressing the next bit of information or control word requires care. One solution involves placing the address of the next control word within the current control word. Then, a portion of the control store is loaded into the program counter.

The speed of a microprogrammed controller will, in general, be faster than the fixed instruction set in the CPU because instructions are customized for the task. For example, sending information to X and Y registers simultaneously takes one instruction with the microprogrammed controller, while it takes several instructions in a fixed instruction set. The wide control word allows parallel operation; that is, all information is accessed in parallel with the op code instead of using several fetches for each instruction. The op code and information, eg, branch address, are fetched in parallel for the microprogrammed controller as opposed to sequentially as in the conventional approach.

## Summary

In general, a transition toward CPUs dedicated to tasks is emerging. The circuit density of ICs has been doubling every year for the past 14 years, and the speed of each function has been increasing accordingly. The integration of peripherals into systems is undergoing a rapid change. Architectural alterations, such as memory-mapped I/O, are increasing the throughput of software peripheral controllers. Previously, for an I/O register to shift or increment, several steps were necessary involving the accumulator where the shifting and incrementing occurred. Memory-mapped I/O allows shifting and incrementing to be performed directly on the peripheral ports.

Dedicated hardware is being included in general purpose devices. Notably, interval timers and counters are appearing in RAM, ROM, I/O, and timer combination chips, and as additions to 1-chip microcomputers. These 1-chip microcomputers are primarily cost-saving devices, since the architecture and instruction sets are based on proven multichip designs.

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# WIDEBAND COMMUNICATION SYSTEM IMPROVES RESPONSE TIME

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Interactive multiple-access data communications system provides full-duplex transactions over VHF coaxial bus to dispersed peripherals. Under minicomputer control, wide bandwidth, high data rates, and fast response time furnish immediate information throughout a nonswitched multipoint link, all at low cost and high reliability

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**James F. Wanner**      PROMIS Laboratory, Burlington, Vermont

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**A** data communications system has been designed to support the Problem-Oriented Medical Information System (PROMIS)—a computerized health information system that furnishes effective organization of medical data and coordination of health care delivery.<sup>1</sup> Large and comprehensive, the data base is structured to facilitate immediate access as required for decisions and to support performance audit with feedback for correction of deficiencies. The data base also contains patient-specific information that is widely accessible to all requestors in order to provide close coordination of health care activities. Rather than provide research style access to the data base, the system presents cathode-ray tube (CRT) text displays, each of which provides multiple choices for selection of next display and for various actions. Megadata SIR 1000 touch-screen terminals are used; the user can simply point to, and actually contact the desired selection. The touch-sensitive outer screen detects the finger touch and determines its position.

To support system terminals, as well as other peripherals such as printers, minicomputers with large disc storage capacity and high speed data communications capability are employed (Figs 1 and 2). Each minicomputer supports about 30 terminals and several minicomputers may be interconnected to provide coordinated service to several hundred terminals. Data communica-

tions lines may be extended up to 20 mi (32 km) by cable and further extended with microwave links.

## Communications System

Communications between computers and terminals or other peripherals are usually restricted in data rate or in length. A voice-grade telephone line can carry data almost anywhere, but is limited to a data rate of 9600 bits/s. A CRT display can be transferred in about 1 s over a telephone line, but PROMIS requires a total response time of 250 ms for data communications and selection processing combined, about 50 ms of which are available for data communications. Even a special data-grade telephone link at 50k bits/s would be too slow. Special peripheral interconnections provided with computers operate at much faster rates—often megabits/s—but cable length restrictions typically require the peripheral and computer to be located in the same room. The PROMIS communications system has been designed to provide 50-ms transfer times for typical 800-character CRT displays and serve dispersed locations within a community—usually within a 20-mi (32-km) radius. A very high frequency (VHF) 2-way coaxial bus is employed to provide many inexpensive interconnect ports.

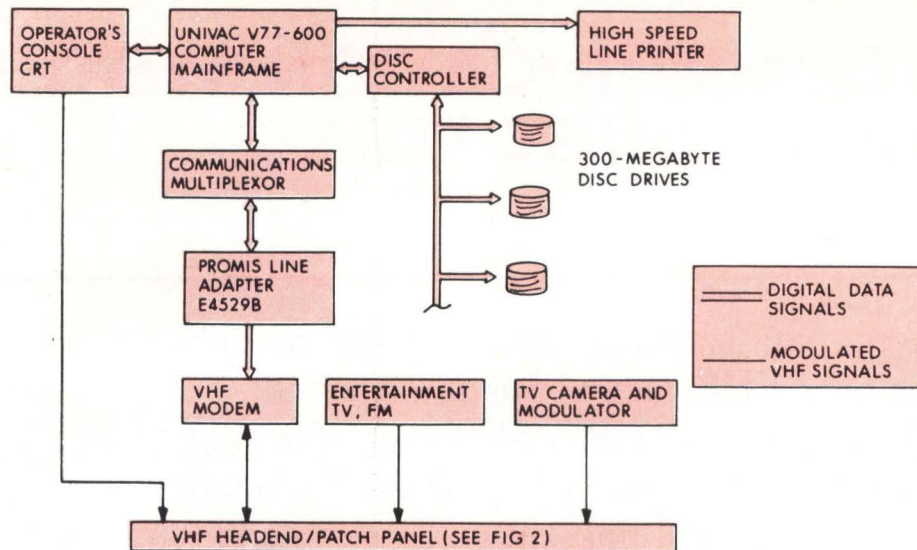


Fig 1 PROMIS computer hardware schematic. Univac V77-600 has 16-bit word with basic cycle time of about 750 ns. Peripherals are divided into system resources in computer room (mass storage discs, high speed line printer) and medical applications devices geographically distributed (CRT terminals, printers, floppy discs, etc)

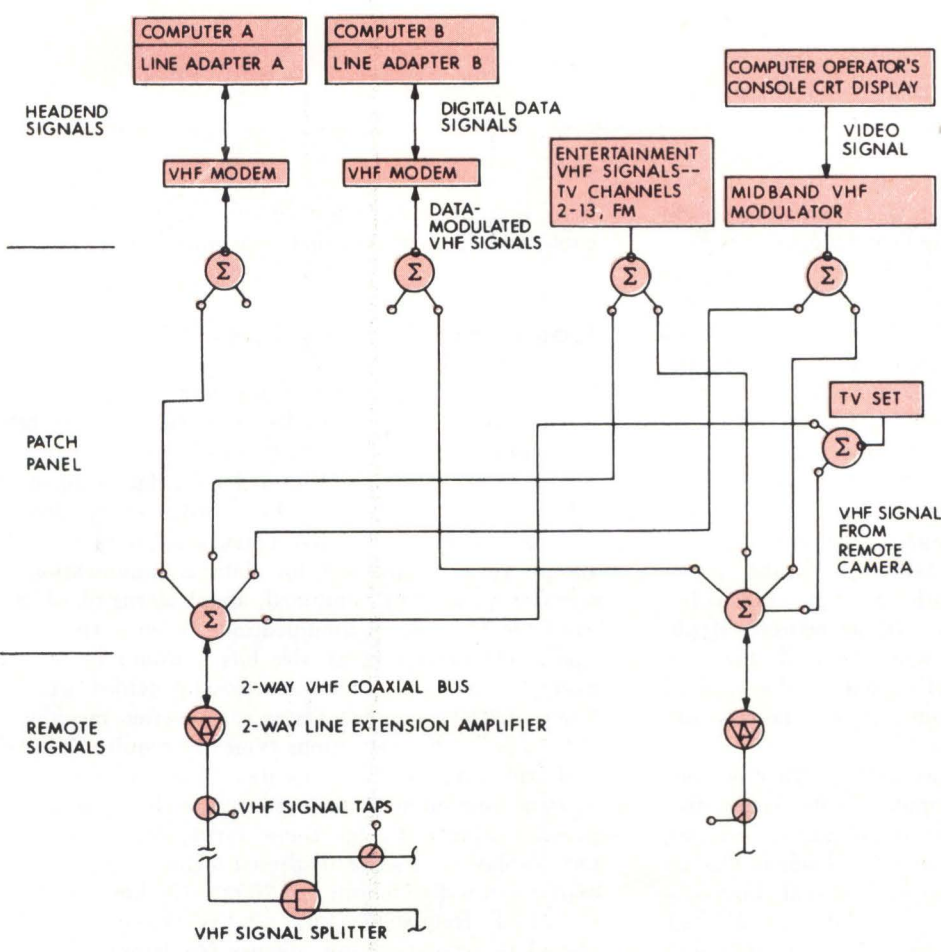
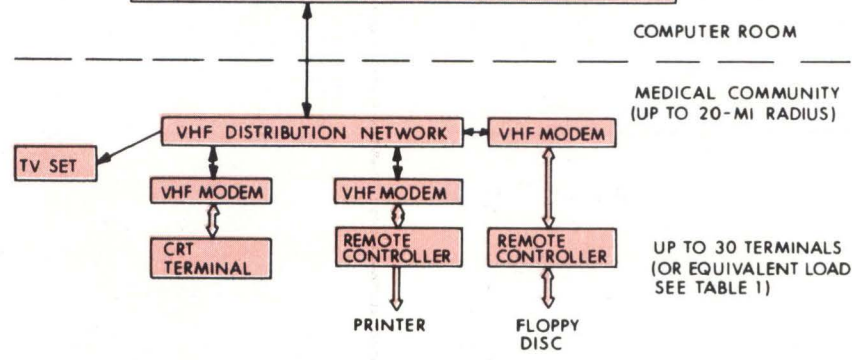


Fig 2 VHF signal bus headend patch panel. Key element is passive device (usually called a splitter) which divides or combines VHF signals with typical loss of only 10%. VHF signals of various frequencies are thus flexibly combined onto a single cable. In particular, switching all devices connected on a cable from one to another (eg, for backup during hardware repairs) is accomplished by moving single coaxial jumper from one tap to another



Modems are available to convert between serial digital data and modulated VHF carrier signals, as well as programmable controllers to manage peripheral devices that operate at remote interconnect ports. This arrangement not only allows easy relocation of devices, but also replaces much controller hardware normally required in the computer mainframe.

Although a VHF bus has been used previously for data communications, it has served primarily as an improved replacement for telephone lines.<sup>2,3,4,5</sup> Therefore, the computer and peripheral equipment from standard telephone communications systems have been implemented, but the higher data rates available on the VHF bus were not exploited. In PROMIS, high speed VHF bus communications provide responsive, reliable service, not just to devices located in the computer room, but to remote peripherals, situated where they are most needed.

## VHF Signal Bus

A VHF signal bus can be easily built from 75- $\Omega$  coax cable, line amplifiers, splitters/summers and other parts produced for the community antenna television (CATV) industry. Cost is low because of large demand (total parts cost in a complete VHF bus system recently installed was below \$20 per port), and reliability is high [mean time before failure (MTBF) of at least 100,000 h]. Two-way communications on a single coax cable are available, supported by line extenders that amplify higher frequencies in one direction and lower frequencies in the other. A typical VHF bus carries 50-MHz to 300-MHz signals outbound and 5- to 30-MHz signals inbound, and may be extended up to 20 mi (32 km) from the cable headend. PROMIS occupies a 3-MHz bandwidth in each direction for data communications; therefore, on the same cable, 16 television channels and many frequency modulation (FM) stations are carried along with the outbound data, and a closed circuit TV (CCTV) signal shares the inbound band with the data signals.

VHF signal splitter/combiner units constructed of passive components are efficient and inexpensive (less than

\$2 for a one-to-two splitter). When used with push-on coax connectors, these splitters allow flexibility in the construction of patch panels from which signals can be selected for a cable system (Fig 2). All components used for the PROMIS VHF bus are commercially available, reliable, and inexpensive; furthermore, since this equipment is widely used for TV signal distribution, installation and maintenance services are available from local companies in most cities.

## Access to the VHF Bus

Simple full-duplex modems that modulate and demodulate digital signals on VHF carriers have been developed. These use frequency modulation of the VHF carrier signals (51 MHz outbound, 28 MHz inbound) and operate at 307,200 bits/s. To minimize errors, an isochronous serial character format is used (Fig 3) wherein each character has a start and stop bit as asynchronous characters do, but the modem also supplies a data clock, as is usual for synchronous serial communications. This clock is produced using a flywheel oscillator that is resynchronized by each transition of the data signal (at least once each character, due to the start and stop bits). This isochronous format is more efficient than the usual synchronous self-clocking schemes, such as Manchester, in which the channel signal rate must be doubled to include the clock with the data in a single serial channel.<sup>6</sup> It is also much simpler than synchronous communications, since initial synchronization and fill characters are not required. The modem is connected to the VHF bus with a single coax drop cable and push-on connector (Fig 4), which can be moved between taps by any operator without disrupting other users on the bus.<sup>7</sup>

## Line Control Protocol

In a high speed VHF bus environment, line control protocol can be based on the following assumptions: (1) communications errors will be rare, (2) retries following errors may be initiated automatically, and

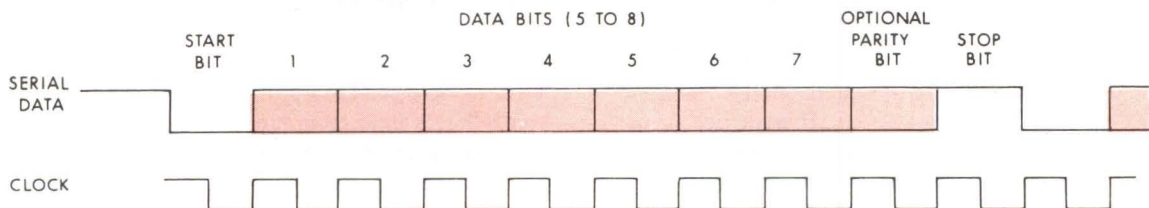


Fig 3 Isochronous serial character format. Identical to asynchronous except that it requires clock signal (as does synchronous). Start and stop bits in isochronous format reduce effective data transfer rate, but permit simple clock regeneration from data transitions alone since at least one transition occurs with each character. Data can then be modulated onto single channel with data capacity equal to clock rate, and clock can be recovered from demodulated data. Synchronous format, in which start and stop bits are missing, requires single channel capacity of twice clock rate for successful modulation/demodulation data communications.

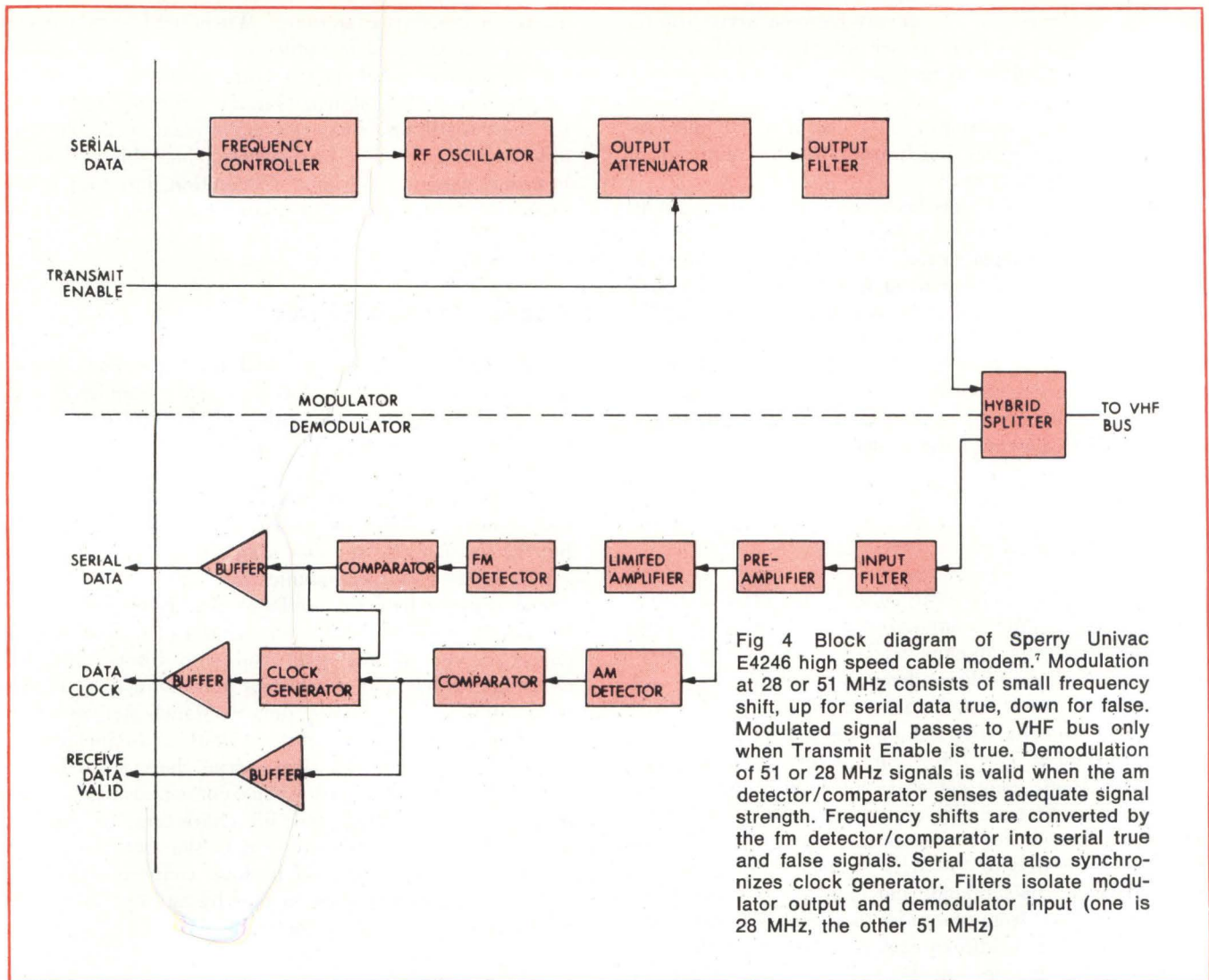


Fig 4 Block diagram of Sperry Univac E4246 high speed cable modem.<sup>7</sup> Modulation at 28 or 51 MHz consists of small frequency shift, up for serial data true, down for false. Modulated signal passes to VHF bus only when Transmit Enable is true. Demodulation of 51 or 28 MHz signals is valid when the am detector/comparator senses adequate signal strength. Frequency shifts are converted by the fm detector/comparator into serial true and false signals. Serial data also synchronizes clock generator. Filters isolate modulator output and demodulator input (one is 28 MHz, the other 51 MHz)

(3) operators can be free to move peripherals from one location to another and continue without any protocol access (sign-on) requirements. On a nearly error-free communications link, the protocol can be limited to line access control, with introductory handshaking minimized. Since the data rate is 307,200 bits/s, polling overhead is minimal—even when many unused poll addresses are included in the poll list.

PROMIS line control protocol is presented in the style of ANSI Standard X3.28<sup>8</sup> (Fig 5). It is a simple polling protocol with minimum overhead. A unique poll address is assigned to each peripheral operated on the line, and a sequential poll address list is used. If a device is not in service, a poll with its address yields no reply, and is passed over subsequent to a response timeout. Polls to peripherals on the line are answered with a single NAK (not Acknowledge) character unless the peripheral has an input message, in which case this message is transmitted in response to the poll. When an output is required, polling is suspended, the output message is broadcast from the line controller, and the target device must recognize its address and accept the message. A single ACK (Acknowledge) response indicates successful receipt of a message; a failure leads to retrieval of the message transmission.

To detect transmission errors, a parity bit accompanies each character (Fig 3) and any parity error detected nullifies the entire message. To guard further against misidentification of the source or destination of a message, the crucial poll address is duplicated wherever it is used.

## Digital Communications Hardware and Software

Two devices make up the mainframe communications controller, a data communication multiplexer (MUX) and a line adapter (Fig 1). The MUX supports up to four line adapters, each operating at 307,200 bits/s; the line adapter handles the line protocol, including polling, so that computer system software overhead is minimized.

Since many CRT terminals are used for the application, each terminal has its own special line control hardware to manage transfers of blocks of data characters on the data communications line. This management includes recognition of messages targeted to the terminal, and sending messages from the terminal in response to its poll (Fig 5). For other peripherals, a remote controller is used (Fig 6). This device interfaces a programmable

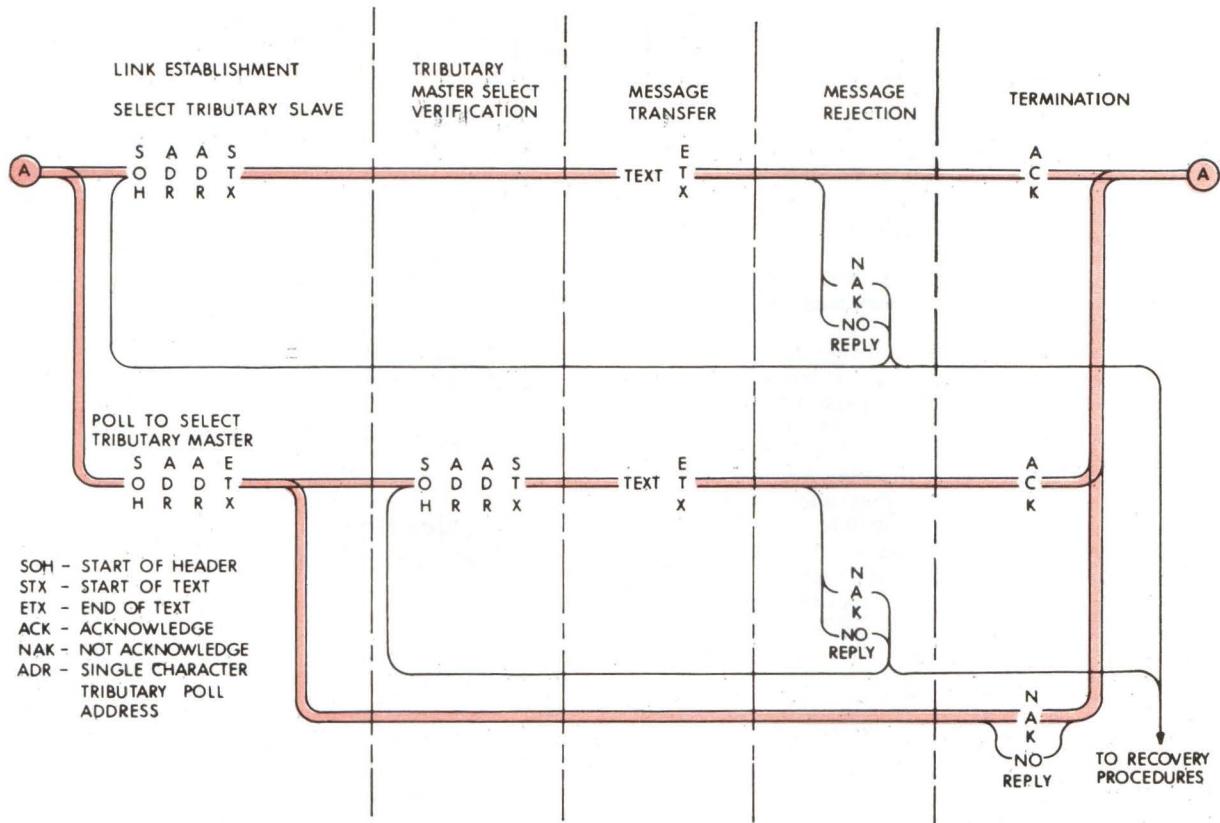


Fig 5 PROMIS communications control protocol. Many peripherals are attached to nonswitched, multipoint link. Computer mainframe serves as control station and may select any peripheral and immediately transfer a message to it. Alternatively, computer may poll peripherals in turn to allow peripheral to gain control and transfer message to computer. Successful (error-free) transfer acknowledgement terminates peripheral selection while transfer failure is always retried

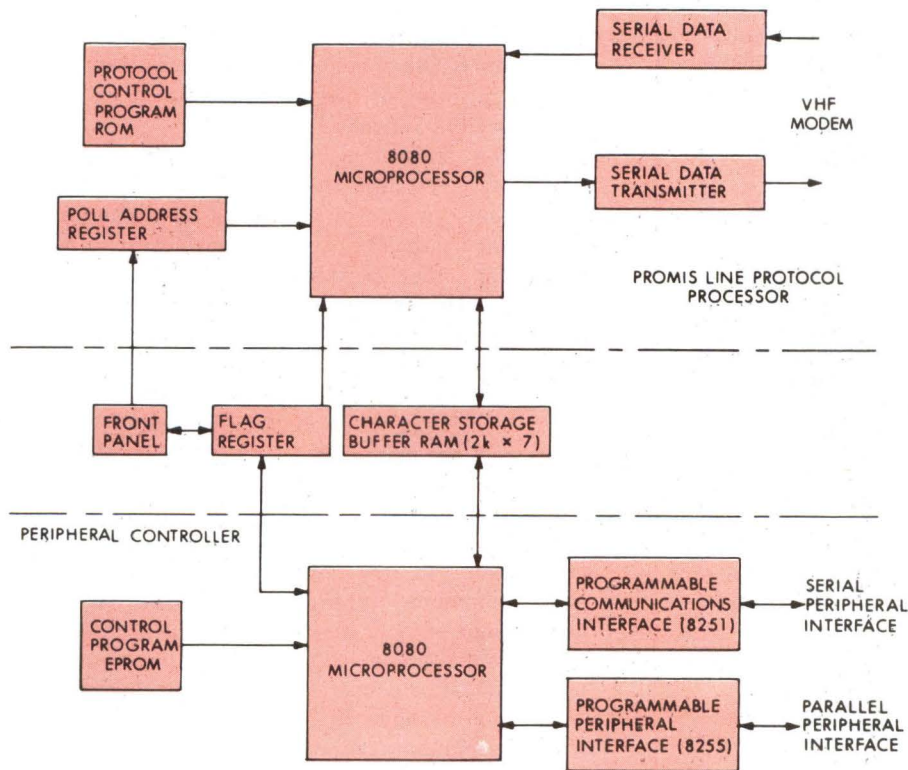


Fig 6 Remote controller functional block diagram. Each remote controller has control program in erasable programmable read-only memory (EPROM) to manage specific peripheral device, such as a printer or floppy disc

### Communications System Model

Communications request sequence for PROMIS can be broken into the following steps:

1. Device prepares message for transfer to computer. This represents start of communications for a request
2. Device waits for line if it is busy. From single server queuing theory, average wait is function of average busy duration (or average line service time)  $S$ , and fraction of available time that line is in use,  $\rho$ : Wait for Busy Line =  $S\rho(1-\rho)^{-1}$
3. Device waits for its poll address. Average wait is half the total poll cycle of  $N$  addresses with single address poll time of  $P$ : Wait for Poll =  $\frac{1}{2}NP$
4. Device transfers inbound message. Time depends on average number of input characters ( $I$ ), and line data rate ( $D$ ): Inbound Transfer Time =  $I/D$
5. Computer accepts input, restores polling. This overhead may vary with computer load, but can be approximated as fixed delay ( $X$ )
6. Computer prepares next output message. For evaluation of communications performance, this is assumed to require fixed time ( $B$ )
7. Computer waits for line if it is busy. This is identical to Step 2
8. Computer transfers outbound message. Transfer time depends on average number of output characters ( $O$ ) and line data rate ( $D$ ): Outbound Transfer Time =  $O/D$
9. Device receives message. This concludes communications associated with one request

Wait for a busy line depends on average busy duration ( $S$ ) which can be expressed as average of input and output transfer times (Steps 4 and 8) plus fixed input processing overhead,  $X$  (Step 5):  $S = \frac{1}{2} (I/D + X + O/D)$ .

Average communications service time per request ( $T_c$ ) is sum of above items (excluding Step 6, computer processing time):

$$T_c = S\rho(1 - \rho)^{-1} + \frac{1}{2}NP + I/D + X + S\rho(1 - \rho)^{-1} + O/D$$

or

$$T_c = 2S\rho(1 - \rho)^{-1} + \frac{1}{2}NP + 2S$$

Fractional line usage ( $\rho$ ) can be found from service request rate ( $Q$ ) and average service time per request ( $2S$ ). Interval between requests for a single user is communications time ( $T_c$ ) plus computer processing time ( $B$ ) plus user "processing" time (or output received to next service request delay) ( $M$ ). Thus, service request rate for  $U$  active users is:  $Q = U/(T_c + B + M)$ , and fractional usage becomes:  $\rho = 2SU/(T_c + B + M)$ .

By substitution for  $\rho$ :  $T_c = 4S^2U(T_c + B + M - 2S)^{-1} + \frac{1}{2}NP + 2S$ . (Eq 1) This quadratic equation has been solved for  $T_c$  as a function of  $U$ , to illustrate the performance expected from the PROMIS Communications System (Fig 7).

peripheral controller to the line, so that the peculiarities of each peripheral can be managed by the program in the controller. The peripheral software control module and the controller hardware usually operated for each device in the computer mainframe are thus largely replaced by the remote controller, and peripherals can be located wherever a cable bus tap is available.

Although most of the device-specific control resides in the terminals and remote controllers, and most of the line protocol is provided by the line adapter hardware, certain functions such as MUX and line adapter set-up, interrupt processing, application task interfacing, and error reporting remain in computer control communications software, with appropriate modules added for the PROMIS line adapter. Device-specific control routines to deal with error recovery, status reports, and performance monitoring are also used.

### Communications System Performance Theory

To predict system performance under design conditions, as well as overloads, a worst-case model has been developed (see "Communications System Model"). Primary parameters are line data rate, average load, and response time. Structure of the load is less important, since short messages appear from the model to entail about the same overhead as long messages when the average load is the same.

To evaluate performance as predicted by the model, the terminal used for data base enquiry has been defined as a unit load. From measurements of actual use, an average enquiry transaction includes an 8-char input request followed by an 800-char display output. Typical users take an average of 2.5 s to study a display and request the next display, and the computer request processing time is about 200 ms.<sup>1</sup> Therefore, the average communications capacity required per unit load is about 300 chars/s. Other common peripheral loads can be expressed in terms of this unit load based on the average data capacity required (see Table).

For the interactive PROMIS enquiry system, an unusually fast response time of 50 ms is allotted to communications in a typical request involving transfer of about 800 characters. This responsiveness is also appropriate for other peripherals, such as those listed in the Table. The line data rate is selected to support about 30 load units with the required response time, and is set, for convenience, at  $32 \times 960$  or  $30,720$  char/s. This is well below the capacity of a VHF channel, which is at least  $2 \times 10^6$  bits/s.<sup>7</sup> If communications system overhead is ignored, the maximum data capacity is about 100 unit loads.

From the model (see "Communications System Model"), performance of the communications system can be predicted for the parameters indicated above. Fig 7 shows communications time and utilization of capacity as functions of load. Response times assume that the number of addresses polled is twice the number actually in use, which should overestimate polling overhead.

Fig 7 also shows the characteristics of a polled line, with the communications overhead time growing slowly until maximum line capacity is approached, at which point the wait for a busy line becomes a major factor.

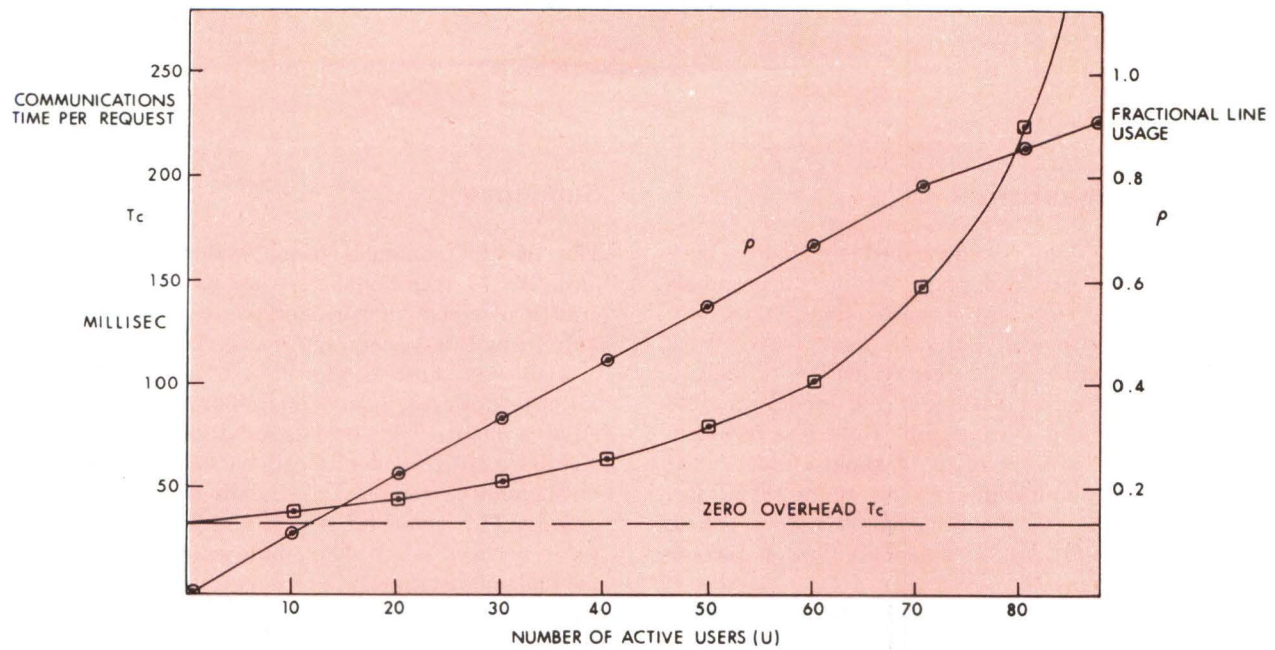


Fig 7 Predicted communications performance. Average communications time,  $T_c$ , for typical request, and fractional line usage,  $\rho$ , are shown as function of load, as predicted from Eq 1.\* Following parameters are assumed: line data rate,  $D = 30720$  char/s; input message length,  $l = 8$ ; output message length,  $O = 800$ ; input computer overhead,  $X = 5$  ms; computer request processing,  $B = 200$  ms; user request preparation interval,  $M = 2.5$  s; average single poll time,  $P = 180 \mu\text{s}$ ; and number of addresses polled,  $N = 2U$  (number in active use). Usage,  $\rho$ , increases nearly in step with number of active users,  $U$ ; however, communications time increases very slowly with  $U$  until usage exceeds 50% ( $\rho = 0.5$ ). For example, doubling number of users from 15 to 30 increases communications time only 30%, (41 to 53 ms) while doubling the users again (from 30 to 60) increases communications time 100% (53 to 105 ms). Thus, high speed polled line remains very responsive over considerable load variation, and degrades gracefully when overloaded

\*See "Communications System Model"

TABLE  
Communications Loads of Peripherals

Active Peripheral	Approximate Average Characters/Request	Estimated Request Interval	Load Units
Enquiry CRT terminal	808	2.7 s	1
Edit CRT terminal	4000	60 s	1/4
Character printer, (120 char/s)	2000*	20 s	1/3
Line printer, (200 lines/min)	2000*	7 s	1
Floppy disc	2000*	3 s	2

\*Block data transfer to a remote controller is assumed

Note that at a design load of 30 units, line utilization is only about 35%. On overload, the line should degrade gracefully, since on a polled line, service requests queue at the communications system/device interface and not in computer software; therefore, the effect of overload-

ing is to increase communications service time which, in turn, decreases the effective service request rate. This request rate should be further reduced by an inevitable but unpredictable increase in computer request processing under heavy load, a factor that has been ignored here.

## System Implementation

Three VHF bus systems as described previously have been in use for the past two years, serving 30 terminals and three printers. Observed response times have been consistent with the model, although heavy loads have not yet been encountered. Precise evaluation is difficult because of the statistical nature of the model and the variability of the load during use. However, measurements made during average loads of about 10 load units yield average communications service times of 37 ms. During these measurements, 60 addresses were polled, and under these conditions, the model predicts an average service time of 35.7 ms.

System reliability has been monitored in various ways. The main VHF bus systems are installed in a large hospital complex with trunks passing through the main ac switch room, boiler room, and x-ray department, ie, in many areas with electrical noise potential. In addition, one hospital ward uses entertainment signals from the VHF bus, and the constantly changing receivers interconnected by patients represent potential sources of noise interference. Finally, communications errors often occur when peripherals are powered up or down while they are connected to the line. The bit error rate measured under these conditions has been 4 in  $10^8$ . These errors are attributed to line noise interference, since the modems on the test bench run without error (less than 1 in  $10^{11}$ ). The observed error rate for a typical active terminal translates into one communications error every 35 h. Since retries are usually completed automatically in less than 200 ms, terminal users are rarely aware of line errors and the communications system can be considered nearly error-free.

On the basis of a single line amplifier failure, the VHF bus MTBF has been 140,000 h, which far exceeds that for typical computer equipment. The modem MTBF has been 13,000 h based on prototype units, although only 25% of the failures were due to component malfunctions while the others were due to modem misadjustments. The latter have decreased in frequency over the past year so the MTBF given may represent a lower limit, especially for the production modems. Thus the communications hardware is very reliable, equal to or better than the other equipment served by the communications system.

One special type of failure that attends a polled, multi-drop communication line deserves mention. If any device fails and transmits either at random or continuously, not only does the line fail, but retries of errors are impossible because the guilty location cannot be identified. The only cure is to unplug each device in turn, until the faulty transmission clears and the line begins to function again. Fortunately, this failure mode is rare. PROMIS Laboratory uses two fully redundant cable systems so that in the event that one fails, the other provides uninterrupted service.

## Summary

The PROMIS communications system illustrates an alternative to traditional restrictions on the remote operation of computer peripherals. Components required to implement this system are not as familiar or as widely available as those used with telephone data communications; however, commercial sources are available for all components. The VHF bus provides responsive, reliable, and inexpensive communications for peripherals located throughout a complex of buildings or across a community. This powerful system can greatly enhance computer services for medical, industrial, academic or commercial applications where geographically dispersed peripherals are required.

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## Acknowledgement

This article describes only a small segment of a large health care delivery system, built not by the author alone, but by a coordinated team of computer and medical personnel both within and outside PROMIS Laboratory. The project has been funded primarily by the National Center for Health Services Research, OASH, DHEW. Prototype modems were developed by David Willard and Paul Wagner, MITRE Corp, Bedford, Mass.



James F. Wanner is hardware coordinator at PROMIS Laboratory where his responsibilities include hardware specification, design, procurement, and maintenance. He has degrees in mechanical engineering (University of Colorado), physics (Earlham College), and astronomy (University of Pennsylvania and Harvard University). He became involved with digital electronics while automating astronomical measurements at the U. S. Naval Observatory.



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## BCD/Binary Conversion With Single IC Cell

Operating on 4-bit inputs, fast BCD/binary conversion circuits, based on repeated division by the radix of the desired number system, use only seven gates, allowing realization of a single universal IC cell to handle both whole and fractional conversions

M. G. Phadnis and D. G. Joshi

Bhabha Atomic Research Center, Bombay, India

**F**requently, man-machine interactions dictate the conversion of whole and fractional numbers from one radix of notation to another. In many control/panel displays, decimal (radix 10) data in binary-coded decimal format must be converted to and from binary (radix 2) for computer usage. A hardware design scheme for fast conversion is based on the standard algorithm of repeated division of the number to be converted by the radix of the desired number system. This scheme has been developed into a practical integrated circuit realization—a universal, single-cell structure that provides multiple function adaptability, reduced parts inventory, and simple array design.

### Conversion Principles

The conventional method for converting an integer from radix  $r_1$  to radix  $r_2$  is to divide repeatedly by the new radix expressed in the notation of the old radix, where each remainder is a digit of the transformed number. Thus the remainder of the first division is the least significant bit (LSB) of the number in radix  $r_2$ . Then, the quotient of the first division is again divided by  $r_2$ , and the process is repeated until the final remainder, which is the most significant bit (MSB) in radix  $r_2$ , is obtained.

### Binary-To-BCD Conversion

In converting from the binary to the

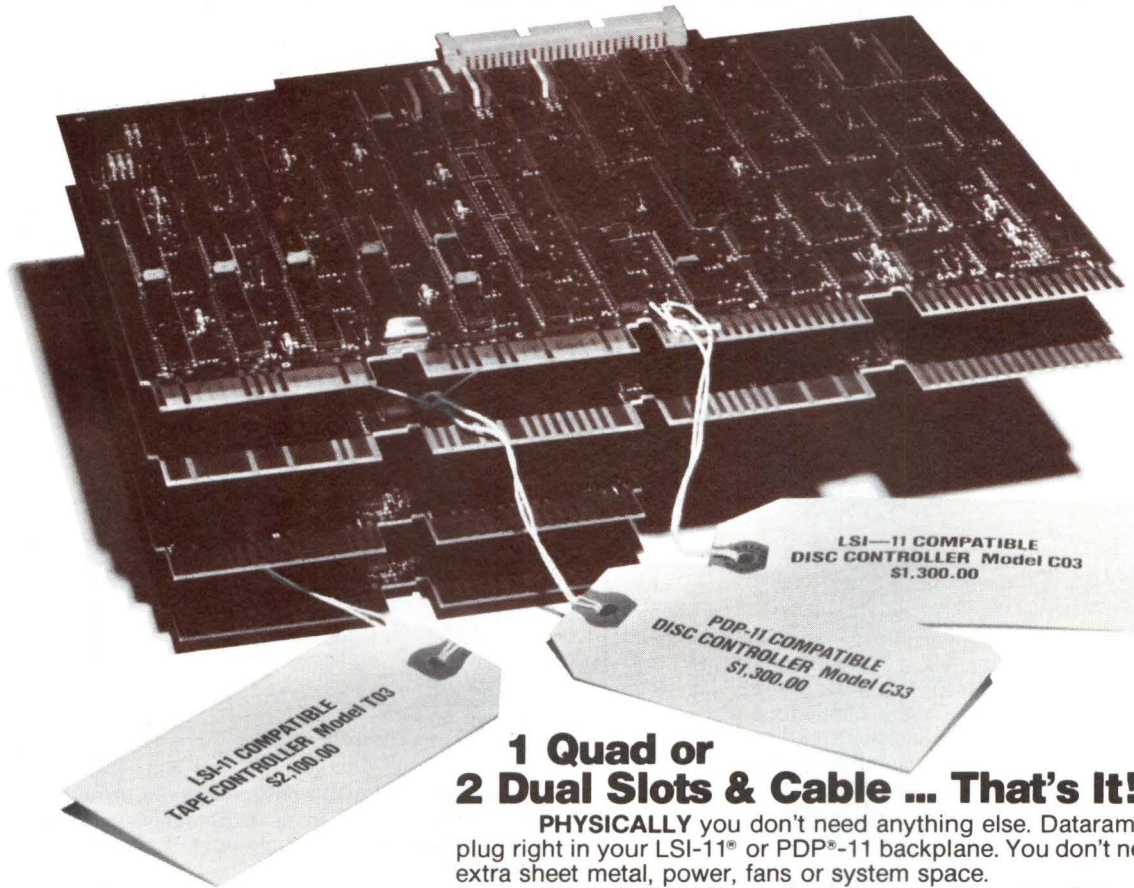
binary-coded decimal (BCD) number systems, repeated division by  $10_{10}$  ( $1010_2$ ) is necessary. However, note that  $1010_2 = 101_2 \times 10_2$ . Hence, division by  $1010_2$  can be implemented by first dividing by  $10_2$ , then by  $101_2$ . Division by  $10_2$  in binary arithmetic is achieved by simply shifting the dividend one bit to the right. This shift can be effected in a hardwired scheme by omitting the LSB of the binary number to be converted and moving the remaining bits forward, forming the quotient.

Division by  $101_2$  is implemented as shown in Fig 1. First, the four most significant bits of the binary number to be converted are connected as inputs to a conversion cell. This 4-bit input is tested for a



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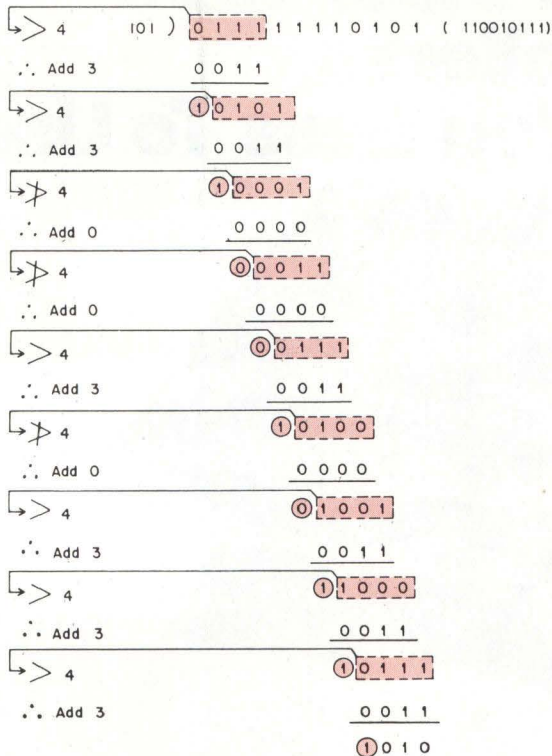


Fig 1 Binary-to-BCD conversion using division by radix technique. To convert  $X = 1111\ 1110\ 1011_2$  to  $4075_{10}$ , let  $X/10 = Q + R/10$ ;  $X/2 = Q_1 + R_1/2$ ; and  $Q_1/5 = Q_2 + R_2/5$  where  $Q_s$  are quotients and  $R_s$  are remainders of respective divisions. Then  $Q = Q_2$  and  $R = 2R_2 + R_1 =$  least significant BCD digit. In this example,  $R_1 = 1$  as given by one right shift,  $Q_1 = 0111\ 1111\ 0101_2$ , and  $R_2 = 010_2$  after dividing  $Q_1$  by  $5_{10}$  ( $101_2$ ). Therefore, least significant BCD digit  $R = 0101_2$  and  $Q_2 = 110010111_2$ . Remainders obtained in subsequent divisions of quotients obtained from previous division are  $0111_2$ ,  $0000_2$ , and  $0100_2$ , the latter being most significant BCD digit. Hence  $1111\ 1110\ 1011_2 = 0100, 0000, 0111, 0101_2$ , or 4075 in BCD

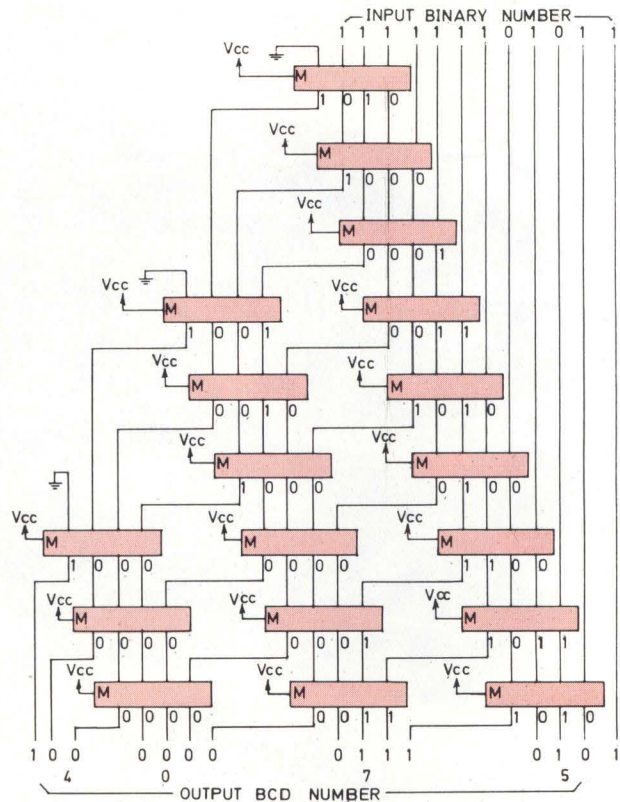


Fig 2 Integer binary-to-BCD conversion logic. Array converts 12-bit binary number to its BCD equivalent, using hardware cell shown in Fig 3. Mode control input of each cell is connected to  $V_{CC}$

greater-than- $4_{10}$  value within the cell. If this condition is true,  $5_{10}$  is subtracted from the input; otherwise, 0 is subtracted. Subtraction of  $5_{10}$  or 0 is done in 2's complement arithmetic by adding  $3_{10}$  ( $0011_2$ ) or  $0000$ , respectively, resulting in a 4-bit output from the cell. The MSB ( $1_2$ ) of this output ( $1010_2$ ) is the MSB of the second quotient, and the remaining three bits ( $010_2$ ) constitute the remainder of the first division. The next significant bit of the original binary number is then inducted and combined with the three remaining

bits to form a new partial 4-bit number ( $0101_2$ ), which serves as the input to the next cell. This division process is repeated until the LSB of the original binary number is inducted and processed. Each division step shifts the divisor operation to the right, which in effect shifts the main input number to the left. This can be conveniently effected in a hardware scheme as a "wired" shift (Fig 2).

In practice, the binary-to-BCD conversion can be implemented by using an adder chip with additional logic,

both to check for the greater-than- $4_{10}$  condition and to generate the required forcing function—to add  $3_{10}$  if the 4-bit input number is greater than  $4_{10}$ . This logic consists of gates 1, 2, and 3 in Fig 3. A true level is generated at the output of OR gate 3 if binary inputs  $A_4A_3A_2A_1$  constitute a number greater than  $4_{10}$ , as defined by the Boolean expression  $A_4 + A_3A_2 + A_3A_1 = 1$ . This output is used for forcing  $0011_2$  or  $0000_2$  as the situation may demand at the  $B_4B_3B_2B_1$  inputs of the 4-bit full adder.

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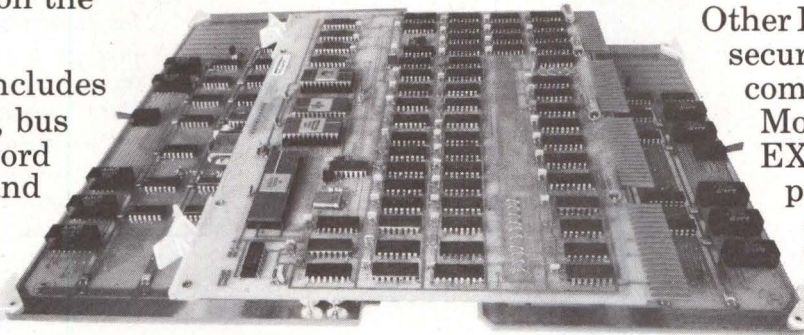
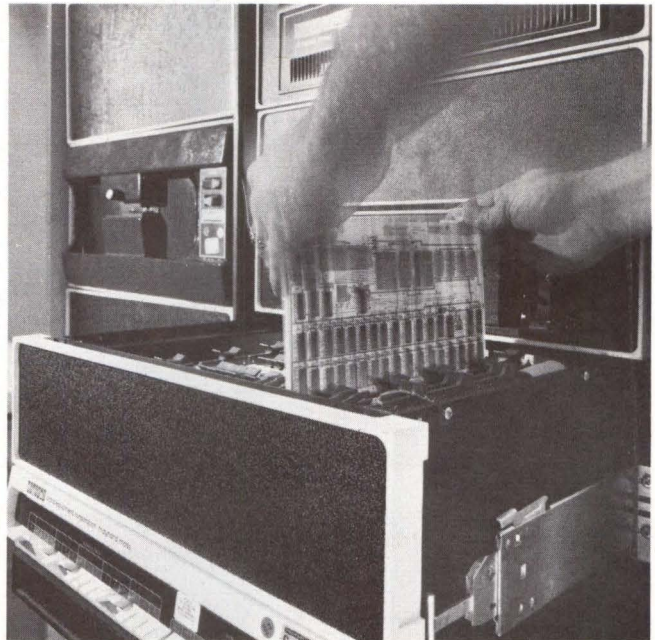
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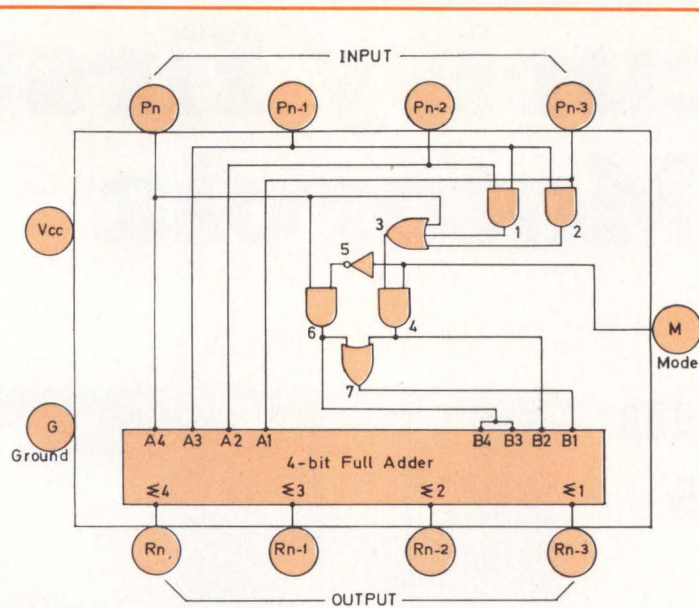


Fig 3 Universal conversion cell. Gates 1, 2, and 3 generate forcing function for conditionally adding  $3_{10}$  in binary-to-BCD conversion. For BCD-to-binary conversion, forcing function is derived from MSB of input. Remaining gates multiplex both forcing functions by means of mode control input

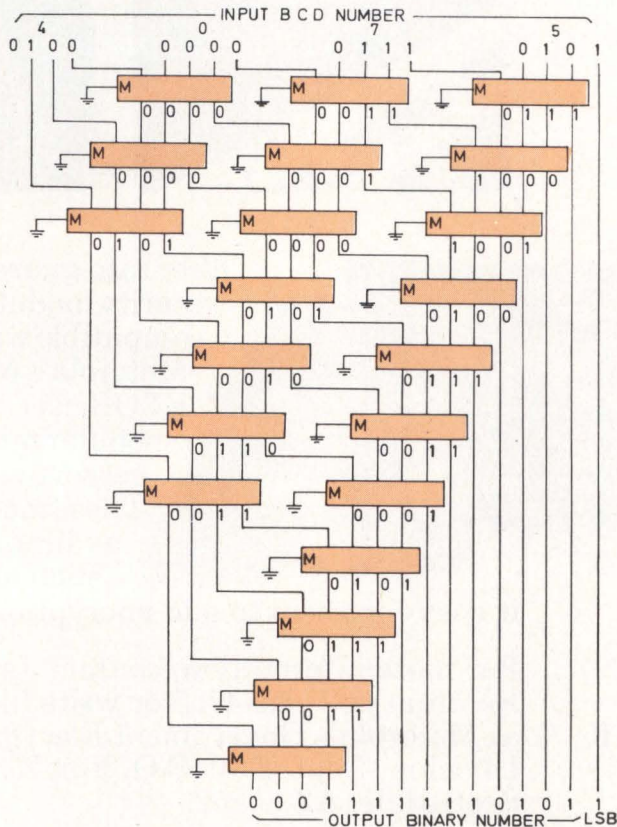


Fig 4 Integer BCD-to-binary conversion logic. Array converts 4-digit BCD number to its binary equivalent, using hardware cell of Fig 3. Mode control input of each cell is connected to ground

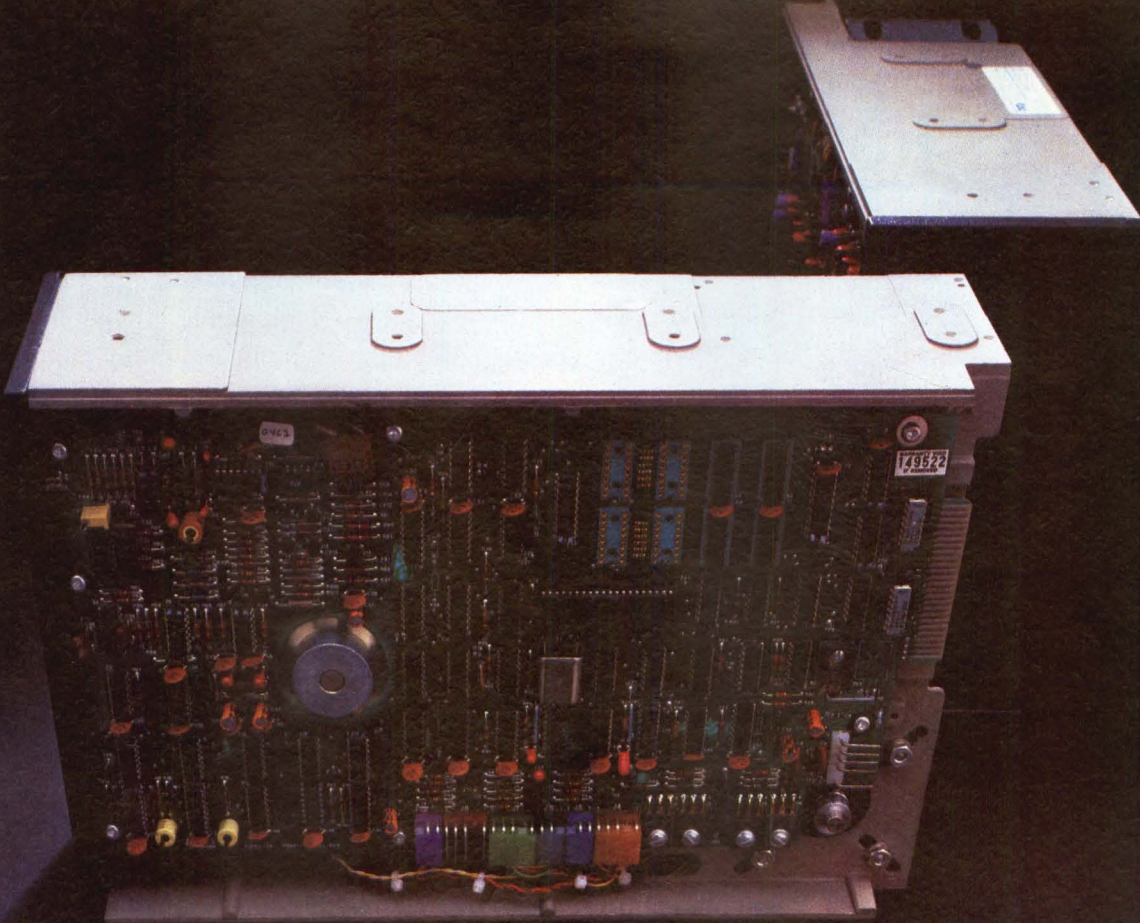
## BCD-to-Binary Conversion

BCD-to-binary conversion (Fig 4) is much simpler than its counterpart because the required repeated division by  $10_2$  can be easily implemented by shifting the given BCD number one place to the right. The rightmost-shifted bit is the remainder, hence, the corresponding transformed bit in each successive division. However, an error is introduced when the LSB of a higher decade (4-bit group) having a value of  $1_2$  crosses to the next lower decade. In this process, the value of the bit becomes 80% instead of the required 50%. The correction is simple and can be done by subtracting  $3_{10}$  from the wire-shifted decade, subject to the condition that the shifted MSB value is  $1_2$ . Correction is not necessary when the value of the decade bit crossing to the right is 0. Subtraction of  $3_{10}$  can be done by adding its 2's complement, which is  $13_{10}$  or  $1101_2$  in this case. Thus, BCD-to-binary conversion can be implemented by using an adder chip alone. Additional logic is not required as the wire-shifted MSB itself can be used as a forcing function.

## Universal Conversion Cell

Solutions to the two conversion types can be combined logically using four additional gates to provide a universal cell, capable of implementing both conversions through a mode control input. Gates 4, 5, 6, and 7 (Fig 3) multiplex the desired forcing functions at inputs  $B_4$ ,  $B_3$ ,  $B_2$ , and  $B_1$  of the full adder chip, depending on the mode control input condition. If the mode control input is high and  $A_4A_3A_2A_1$  is greater than  $4_{10}$ , the function forced at  $B_4B_3B_2B_1$  is  $0011_2$ , which is the same as add  $3_{10}$ . If the input number at  $A_4A_3A_2A_1$  is less than or equal to  $4_{10}$ , the number added is  $0000_2$ . Thus, the cell implements binary-to-BCD conversion with the mode control input at high.

Similarly, with the mode control input at low, the cell implements BCD-to-binary conversion by forcing the input condition  $1101_2$  at  $B_4B_3B_2B_1$  if  $A_4$  is  $1_2$ ; otherwise, input condition  $0000$  is forced. In this discus-



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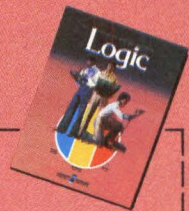


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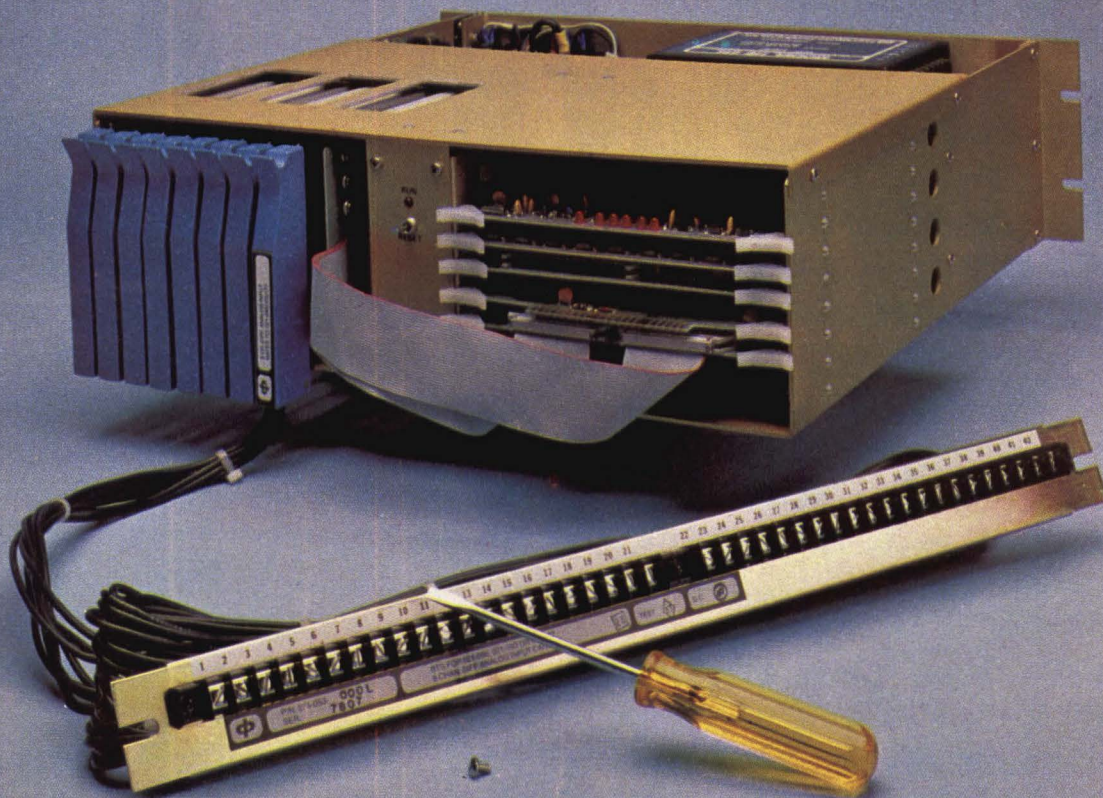
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sion, only integer conversions are implied. However, the cell can also perform conversions of fractional numbers. The logic in this case has a mirror image symmetry with respect to the integer conversions.\*

Fig 2 shows an array constructed for the conversion of a 12-bit binary number to its BCD equivalent. Conversely, the BCD number is converted back to its binary equivalent by the array shown in Fig 4. These arrays are essentially similar to those proposed by Raphael in construction and package count and have comparable conversion times.

### Summary

Solution of the binary-to-BCD conversion problem has been obtained by defining a cell based on a 4-bit full adder IC and three additional gates to generate the appropriate forcing function to implement division by the required radix. For solution of the BCD-to-binary conversion problem, the cell contains a 4-bit full adder, in which the forcing function is derived from the wire-shifted MSB itself. These two solutions are then combined logically with four more gates to provide a universal cell capable of implementing both conversions through a mode control input. The resulting design is readily amenable to integrated circuit realization as the additional 7-gate circuit can easily be accommodated on any commercially available 4-bit full-adder IC chip, such as the SN7483, requiring only 11 pins of a 14-lead package.

### Bibliography

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J. R. Linford, "Binary-to-BCD Conversion With Complex IC Functions," *Computer Design*, Sept 1970, pp 53-61

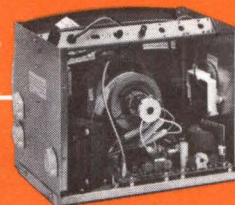
H. A. Raphael, "Fast BCD/Binary Conversions," *Electronic Design*, Oct 25, 1973, pp 84-89

\*Interested readers may obtain information on fractional number conversion by requesting it in writing from the Editor, *Computer Design Magazine*, 11 Goldsmith St, Littleton, MA 01460.

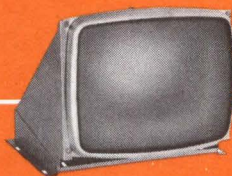
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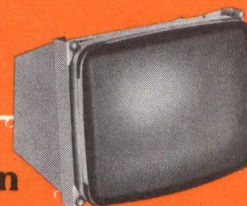
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## Digitized Video Processing In Realtime

A signal processing system tracks the constantly shifting location of a randomly moving object in realtime using ultra fast array processing

**John Meyn** CSP, Incorporated, Burlington, Massachusetts

Except for costly special purpose systems or special interfacing to powerful mainframes, digitizing and processing video data in realtime at standard television scan and frame rates has been extremely difficult to accomplish. A high performance digital signal processor (Figure) provides this capability with a high

speed programmable floating point Macro Arithmetic Processor (MAP-300\*), three independent memory buses, and several parallel processors. One processor—an Input/Output Scroll\* (IOS2)—is programmed and interfaced to accept sliced digitized video from a TV camera controller at roughly  $4 \times 10^6$  pixels/s (picture

elements). Other processors comprise a host interface module (HIM), programmed to communicate with the host minicomputer; a central system processing unit (CSPU), with a resident Executive program and a large library of powerful array processing routines; and an AP-300 arithmetic processor, which provides the ultrafast array processing capability, including 32-bit floating point multiplies at a 4-MHz rate. The host can be any minicomputer, which is programmable in FORTRAN, using subroutine calls to the SNAP-II\* (Simple Notation for Array Processing) library that are executed in MAP-300.

Frames arrive at 60/s, 256 scans/frame, and 256 pixels/scan, ie, 3.93M pixels/s. The IOS2 is programmed to recognize start-of-frame, then select a subset of 180 x 180 pixels, pack them into 16-bit words of four pixels each, and transfer them to MAP-300 memory on a selectable bus. The 180 x 180 size is chosen for convenience to fit available 4k memories (32-bit words). Larger memory sizes can be selected, should higher resolution video be required.

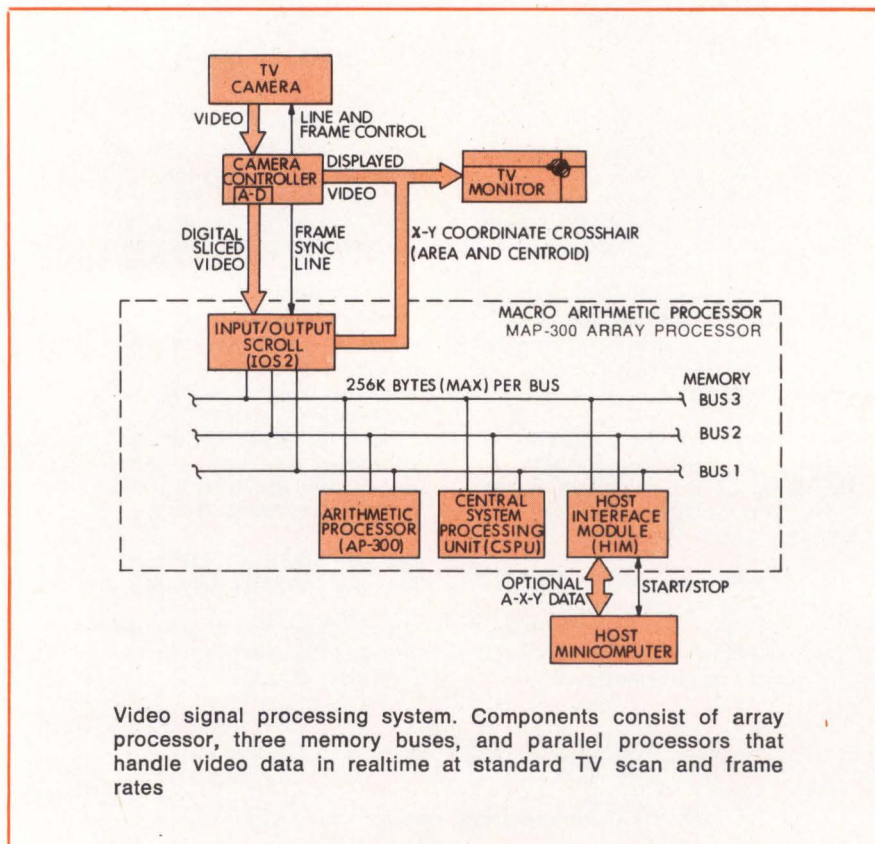
The AP-300 processes each array, computing area (A)—a measure of image size—and centroid ( $\bar{X}, \bar{Y}$ )—a measure of image location—according to:

$$A = \sum \sum P_{ij}, \quad \bar{X} = \frac{\sum \sum iP_{ij}}{A}, \quad \text{and} \\ \bar{Y} = \frac{\sum \sum jP_{ij}}{A}$$

where  $P_{ij}$  is the pixel at location (i, j), having value 1 where the binary image exists and 0 where it does not. The three functions are performed over the 32.4k (180 x 180) pixel images in 13.5 ms, an average of 133 ns per arithmetic operation. Results are stored in the MAP-300 Bus-1 memory, where the host can optionally access them without interfering with the realtime process. The centroid is also output through a parallel port in IOS2 to control the crosshairs on the TV monitor.

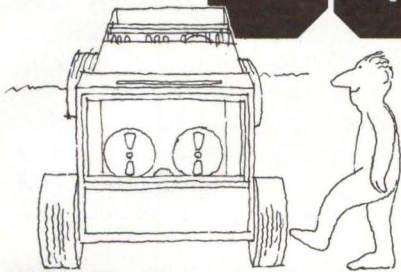
Controlling and bringing data in and out of a host/array processor combination weighs heavily on overall system efficiency and realtime capability. Peripheral device interfacing by the MAP-300 successfully unburdens the host from data acquisition or data output and display tasks by providing I/O scrolls for direct data access and integral software for onboard control. □

\*MAP, I/O Scroll, and SNAP-II are trademarks of CSP, Inc, Burlington, Mass.



Video signal processing system. Components consist of array processor, three memory buses, and parallel processors that handle video data in realtime at standard TV scan and frame rates

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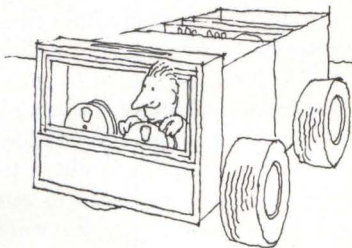


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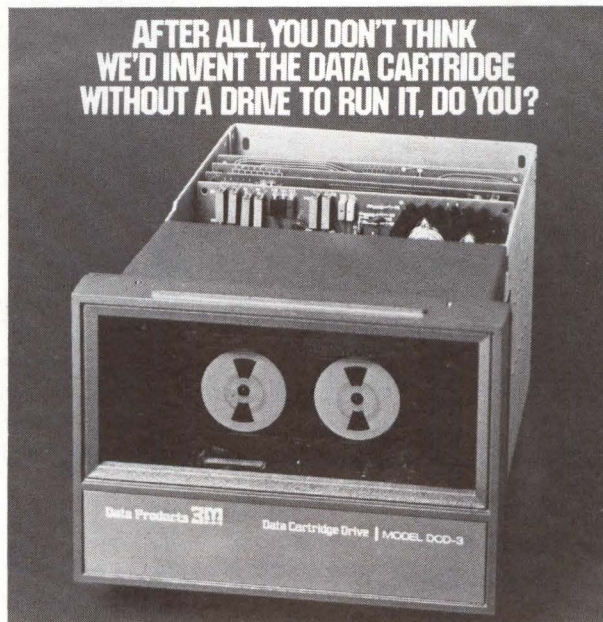
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# 3M

## Computer Connector Saves Space And Cuts Costs

Inexpensive but reliable connector achieves increased contact density within smaller area

**Paul K. Winklebleck**

GTE Sylvania Connector Products Operation, Titusville, Pennsylvania

Packaging requirements of a leading computer manufacturer have generated the need for a custom, high density, card-edge, gold-dot connector with 33% more contacts but less than 50% of the overall size compared with the existing connector. The existing connector measures 4 x 3 x 1.75" (10.2 x 7.6 x 4.45 cm) in size with 216 contacts for 8 printed circuit (PC) boards, while the new connector is 5.25 x 0.75 x 1.75" (13.34 x 1.9 x 4.45 cm) with 288 contacts for 3 PC boards. In addition, the new design is to withstand temperature extremes and corrosive atmospheres found in many computer applications, and contact resistance is to be low and stable for compatibility with solid-state electronics. All requirements must be met at the lowest possible cost and with the reliability of the previous connector.

To achieve the desired design, several problems must be solved. The connector insulator needs very thin

but strong walls because the packaging density requires card spacing on 0.25" (6.35-mm) centers. To overcome this stringent factor, a special glass-reinforced phenolic material possessing exceptional physical strength and dimensional stability was formulated. For dimensional integrity the mold is made to precise tolerances and molding processes are controlled closely.

Although the conventional contact PC board interface is a gold contact to a gold board finger, the computer manufacturer prefers solder plating instead of gold on the board. This requirement lowers board manufacturing costs, but it demands a dependable, gas-tight connection.

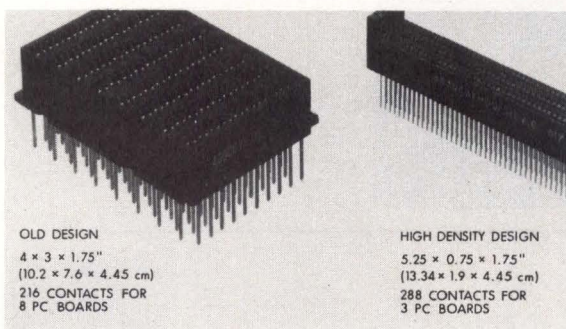
Final contacts chosen feature a single cantilever beam design with inherent preload to ensure high normal force, and are made from a high tensile phosphor bronze base material. Contact interface is through a spherical gold dot that is welded

to the contact after solder plating. This dot has a minimum 0.002" (0.05-mm) thickness, much greater than the 0.000050" (0.00127 mm) typically available with overall or selective gold plating. Normal contact force is approximately 350 g at nominal deflection, which is sufficient to ensure a gas-tight interface with the solder plated PC board, while maintaining a low and stable contact resistance.

Because the new connector has a contact grid of 0.100 x 0.150" (2.54 x 3.8 mm), special assembly tools were developed to enable a 0.020" (0.5-mm) true position of the contact tails. This tolerance ensures low installation cost and high manufacturing ease in assembling the connector to the computer backpanel, as well as for the subsequent automatic wirewrapping operation.

For acceptance testing, an automatic resistance measuring system is used, which sequentially measures resistance on up to 100 contacts, one per second. Any variation of more than twice the initial resistance of a contact pair after mechanical and environmental stressing is considered an indication of failure. Sample connectors were tested for durability through 200 insertion and withdrawal cycles, with resistance measured at intervals throughout the range. To prove connector capability to withstand long-term exposure to environmental extremes, samples were subjected to a temperature and humidity test based on EIA RS-364, TP 31, Method 2 criteria. Other samples were exposed to a humid, 1% by volume, sulfur dioxide atmosphere; and another group was exposed to concentrated nitric acid for 1 h, followed by exposure to fumes of 22% ammonium sulfide for 15 min. Temperature cycles ranged from 0 to 75 °C. In the final test sequence, samples were vibrated at 20 Hz at cycles of 10 s on and 10 s off in different planes with contact resistance measurements made every 100 cycles. For all tests, resistance changes were negligible or well within specified limits; all contacts remained reliable and gas-tight.

The connectors with gold-dot contacts meet or exceed all performance criteria. In a higher density, smaller size, and lower cost configuration, they have passed severe, accelerated life tests simulating the operating conditions the computer would likely encounter over its service life. □



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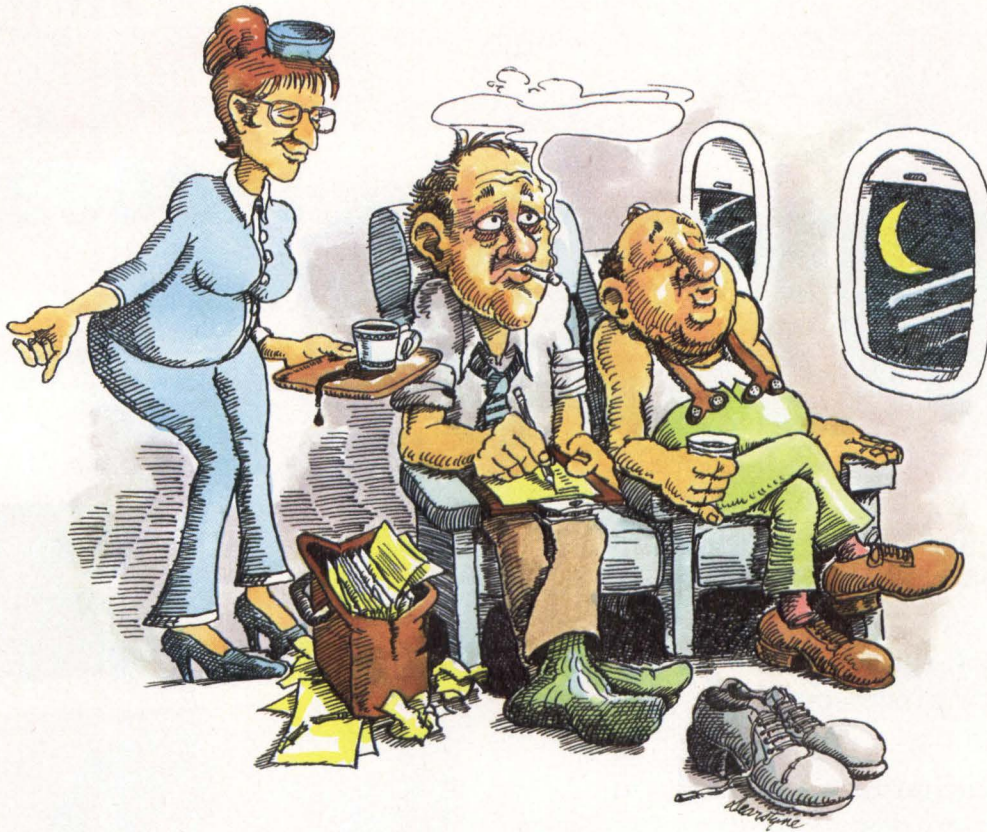
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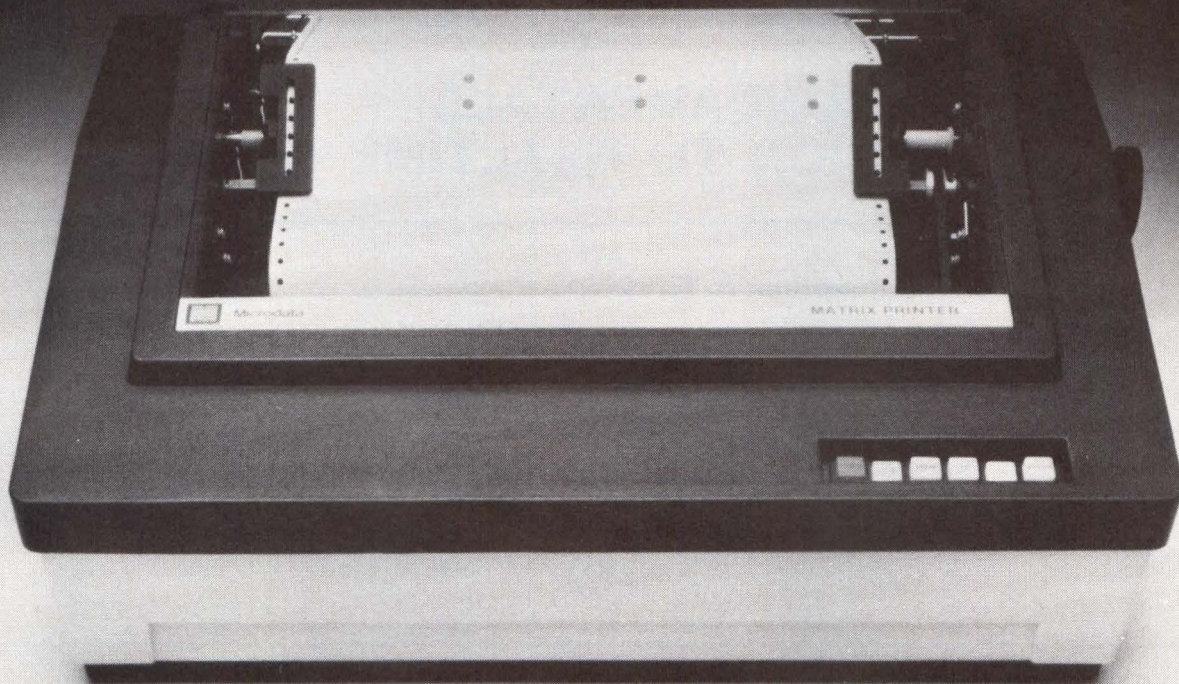
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## **INTERFACING FUNDAMENTALS: AN INTRODUCTION TO REALTIME CLOCKS**

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**Christopher A. Titus and Jonathan A. Titus**  
Tychon, Inc

**David G. Larsen and Peter R. Rony**  
Virginia Polytechnic Institute and State University

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In many microcomputer applications the computer must perform actions at accurately timed intervals. This allows the computer to make accurate measurements of an analog signal at specific intervals, for example, at 100 ms. This 100-ms period may be "timed" through the use of a time-delay loop in which software commands are used, or through the use of an external clock of some sort.

At this point, it may be realized that while a time-delay software routine may generate a delay of the required accuracy, the computer can do nothing else while it is performing the timing software steps. This is a serious limitation. Although probably less obvious, the time-delay software steps may be interrupted by some external device that requires immediate servicing by the computer. The overall effect is to "lengthen" the time required for the time-delay software steps. The actual time delay would be the sum of the time spent in the software steps and the time spent servicing the external interrupt.

In most instances in which accurate periods are required, an external circuit is used to time the necessary periods with as little interaction between the computer and external clock as possible. Such clocks are immune to external interrupts and to changes in the normal flow of a program. Once started, they continue to time a period until it is completed and the time is up. In this way, the clock runs in parallel with the computer; the computer then can perform other tasks and service interrupts while the clock is running. This type of external clock is often called a realtime clock, since its time is real, in that it cannot be altered or delayed by events that would normally affect a program.

There are several types of realtime clocks, indicated by the following listing.

*Programmable Realtime Clock*—The actual required period is preprogrammed within the clock through either hardware or software. Once the clock has been started, it continues timing until the period has ended. At the end of the period, the clock signals the computer that the timing task has been completed.

*Free-Running Realtime Clock*—Running continuously, the clock signals the computer at the end of each period. The periods generally are of equal length, for instance 10 ms.

*Time-of-Day Clock*—This type of clock will provide the computer with the actual time, eg, 16:20 hours; however, it is not frequently used in small computer systems.

The concept of realtime has been introduced subtly in previous columns. Operation of an 8085 based computer system, use of the 14-bit timer contained within the 8155 read/write memory, and a description of an interface chip in terms of its realtime operation have all been covered. An excellent example of a programmable realtime clock is the 14-bit counter used in the 8085 based computer. It obtained its time base from the crystal clock that controlled the microprocessor chip; an interrupt was used to signal the end of the timing period. Assuming that a frequency of 1 MHz was used to control the clock, a 14-bit counter could provide a total count of 16,384  $\mu$ s, or just over 16 ms. This might be somewhat limiting if periods of several seconds are required, but the scheme is fairly flexible. If longer periods are required, the 14-bit counter could be programmed to time



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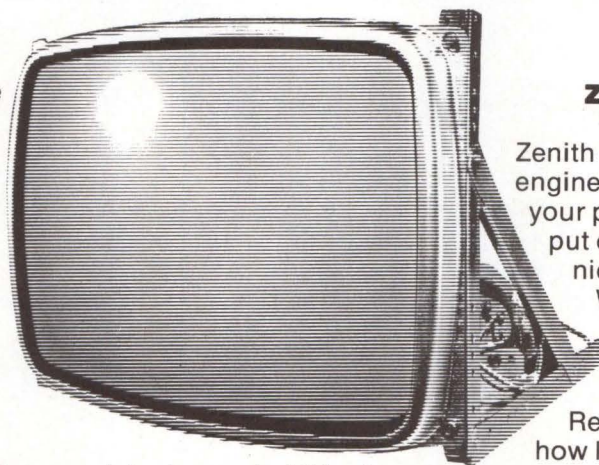
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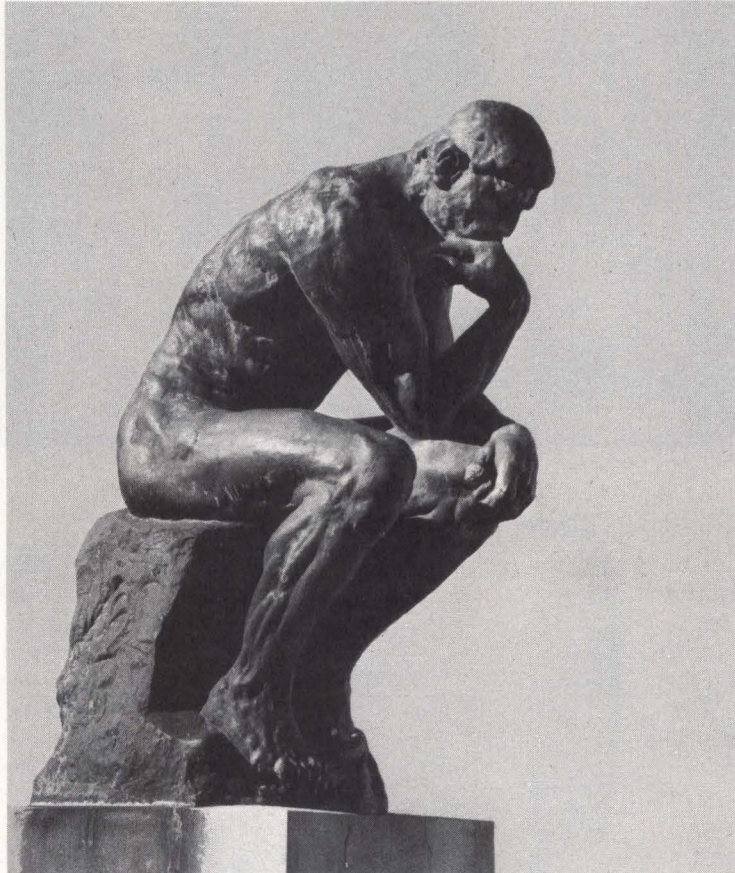
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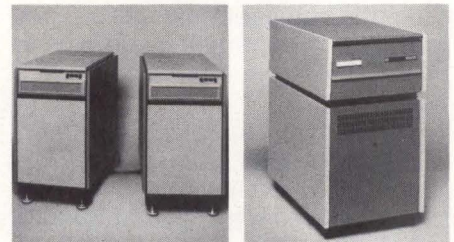
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some integer fraction of the period and the computer could be used to total the number of shorter periods that are required for the entire period to have elapsed. The computer would only have to increment and test a count each time the clock interrupted it. One drawback to this is that additional software is required, something that the use of realtime clocks was intended to avoid in the first place; however, the additional program steps are quite minimal.

In many cases, it would be valuable if the realtime clock could be preset for the clock's basic frequency, eg, 1 MHz, 10 kHz, etc, as well as for the actual count. If these various intervals were available, the timing of longer periods would be relatively easy and no additional software steps would be required. A simple series of divide-by-10 counters such as the SN7490 or SN74390 could be used to divide a high frequency clock signal into lower frequencies for use by the realtime clock's counters. Various frequencies could be selected readily through the use of jumper wires on the computer board. A more sophisticated realtime clock scheme could use an electronic switching circuit that would allow the computer itself to select the frequency required. Thus, a programmer could select the basic period and the actual count through software commands to the realtime clock.

Freerunning realtime clocks are preset to time a period of predetermined length, perhaps 10 ms. This period is timed over and over again, interrupting the computer each time that a period has been completed. In many computer systems, the line power frequency, 60 or 50 Hz, is used to provide a very stable, fixed-length period that may be used equally as well. The freerunning type of realtime clock is not as independent of the computer (eg, software control) as is the programmable realtime clock. Software steps to accumulate the number of periods are still required, and the total timing period may have an error of up to two of the basic frequency periods.

Since freerunning realtime clocks have a regular period, they are often used to signal the processor that it is time to start a software routine that will check various input/output devices to determine whether or not they require some computer service. Through the use of a software table, the computer can check to see what devices are enabled or disabled, and it can also determine the frequency at which they must be checked. It is useless to check a 10-char/s teletypewriter every 10 ms; instead, it would be checked every 80 or 90 ms, while a faster device is checked at the end of each 10-ms period. Such a scheme allows computer and programmer flexibility in the way that realtime operations are handled, particularly for situations in which the computer must perform many realtime operations simultaneously.

In almost all cases, the computer and realtime clock are connected by an interrupt signal. In this way, the clock can immediately signal the computer that the current period has been completed or "timed out." Since interrupts can be quite complex, as has been described previously in these columns, only one realtime clock should be used with a microcomputer. It will be up to the user to determine the priority, and thus the importance, of the realtime clock. Often it is assigned the highest priority.

Unfortunately, there are few, if any, realtime clock interfaces available for the Intel/National Semiconductor 8080 based microcomputer boards, or for the S-100 microcomputer systems. A future column will deal with the hardware interface for a programmable realtime clock, in addition to the software.



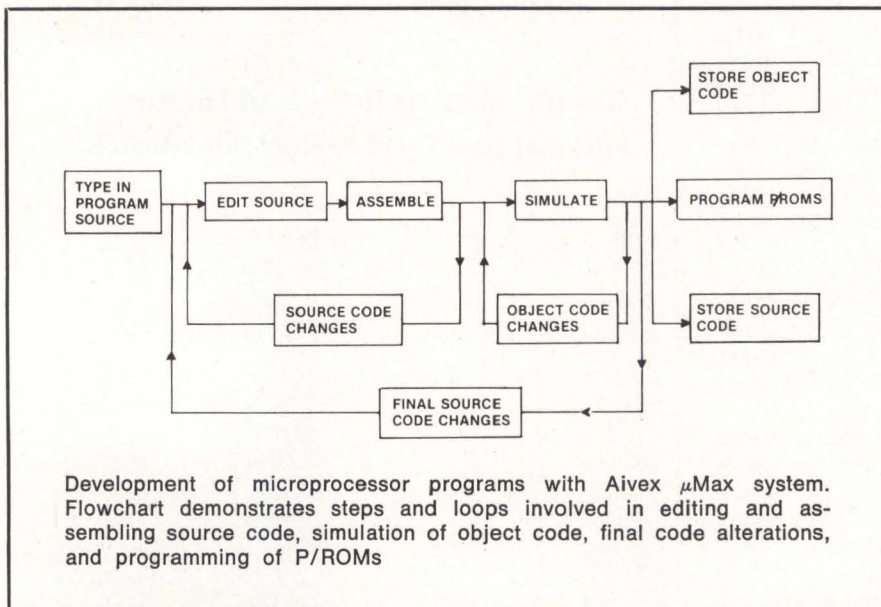
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## Development of Microprocessor Programs Is Accomplished Using Integrated System



The  $\mu$ Max system, consisting of an LSI-11 CPU, 20k solid-state memory, LA-36 DECwriter, M9200 P/ROM programmer, dual flexible disc system, and software, applies techniques of large-scale computer systems to the development of microprocessor programs. Most microprocessor types are supported by the software.

Aivex, Inc, 6 Preston Ct, Bedford, MA 01730 has supplied the AOS-II monitor, directory/delete, symbolic editor, file rename, file transfer, P/ROM programmer transfer, macro assembler, and simulator as software components. First step in the development cycle (see diagram) is typing in the source code using the editor. Changes may be made before the recursive assembly/correction cycles, as well as after each assembly. The cycle continues until all assembly errors are eliminated. The simulator then executes the object code produced by the assembler.

During execution the simulator can examine and alter the contents of the simulated ROMs through interactive debugging; this eliminates the necessity of reassembling the sources. In addition, various status and condition signals, inaccessible to the user in the microprocessor, are available for examination and alteration in the simulator. Once the program is operating properly, final assembly is made incorporating all object code changes made during simulation.

This final object code is used to program the P/ROMs, which are inserted in the programmer. Data are transferred from the system floppy disc to the programmer without the use of paper tapes. Source code is saved offline for documentation purposes and for later changes; the object code is saved for programming additional P/ROMs.

Circle 410 on Inquiry Card

## Cards Can Operate in Any Microcomputer Slot With Data Bus Structure

STD BUS is a data bus structure containing a logic power bus, data bus, address bus, control bus, and analog power bus with similar functions

grouped on the bus connectors. The concept was developed by Pro-Log Corp, 2411 Garden Rd, Monterey, CA 93940 in association with Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006 to allow any card in an 8-bit microprocessor system to operate in any slot. The bus handles all in-

ternal communications to facilitate orderly signal flow between cards. System function, memory type, and microprocessor type can be changed by exchanging cards.

Compatible with Pro-Log's standard 4.5 x 6.5" (11.4 x 16.5-cm) edge connected cards, the bus is 56 lines wide. A motherboard contains the bus structure and a ground plane to minimize noise, in addition to card edge connectors for up to 16 cards and mounting brackets. It has been incorporated in the 7000-series of 8-bit systems that consist of Z80 and 8085 based processor cards, 16k-byte EPROM and RAM cards, 64-line TTL input and output port cards, and a TRIAC output card.

A cross-licensing agreement between the two companies permits them to begin manufacturing the same types of cards. Additional processor, memory, digital and analog I/O, peripheral I/O, and industrial I/O cards for the bus are under development.

Circle 411 on Inquiry Card

## Memory and I/O Devices Upgrade Performance and Speed of 8085A Systems

Compatible with the 8085A-2 CPU which operates at a clock rate of 5 MHz and an instruction cycle of 0.8  $\mu$ s, three high performance memory and I/O peripherals are high speed versions of comparable components introduced with the 3-MHz 8085A. The MOS/LSI devices are the 8155-2/8156-2, each of which contains a 2k-bit static RAM with three programmable I/O ports (22 I/O lines) and a 14-bit programmable counter/timer; and the 8355-2, which is a 16k-bit ROM with two programmable I/O ports (16 I/O lines). The former device consists of RAM cells organized as 256 x 8; the I/O lines can be configured as two 8-bit ports and a 6-bit handshaking port. The latter contains a 2k x 8-bit ROM; each line may be individually programmed as input or output.

Combined with the CPU, the devices form a 3-chip microcomputer system that allows the CPU to function without wait states. Operating with a 5-V supply, the system includes 38 programmable parallel I/O lines, serial I/O ports, system clock, system con-

A military computer system isn't complete without a full line of peripherals... anymore than a commercial system is. That's why ROLM provides peripheral devices in every major category.

ROLM's family of Mil-Spec peripherals has a tougher role to fill than their commercial cousins. They have to be rugged... reliable... proven... documented... fully integrated and meets a long list of Mil-Specs.

ROLM Tape Transports not only meet crucial Mil-Specs, they've established long term data reliability plus unit MTBF in excess of 4000 hours.

Our compact Printer, which is as solid as a heavy-weight, weighs less than 65 pounds and provides a 64-character ASCII subset at speeds up to 400 lines per minute.

For random access storage the ROLM Flexible Disk Drive provides over three million bits of memory on interchangeable floppy disk media.

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These are just a few examples of ROLM's line of Mil-Spec peripherals. We offer commercial devices too. And they're all supported by compact interfaces, like our new 3364 single-board magnetic tape controller, and by system and diagnostic software to enable you to easily and effectively operate each peripheral. Peripheral selection. Full system support.

## That's Why We're #1 in Mil-Spec Computer Systems

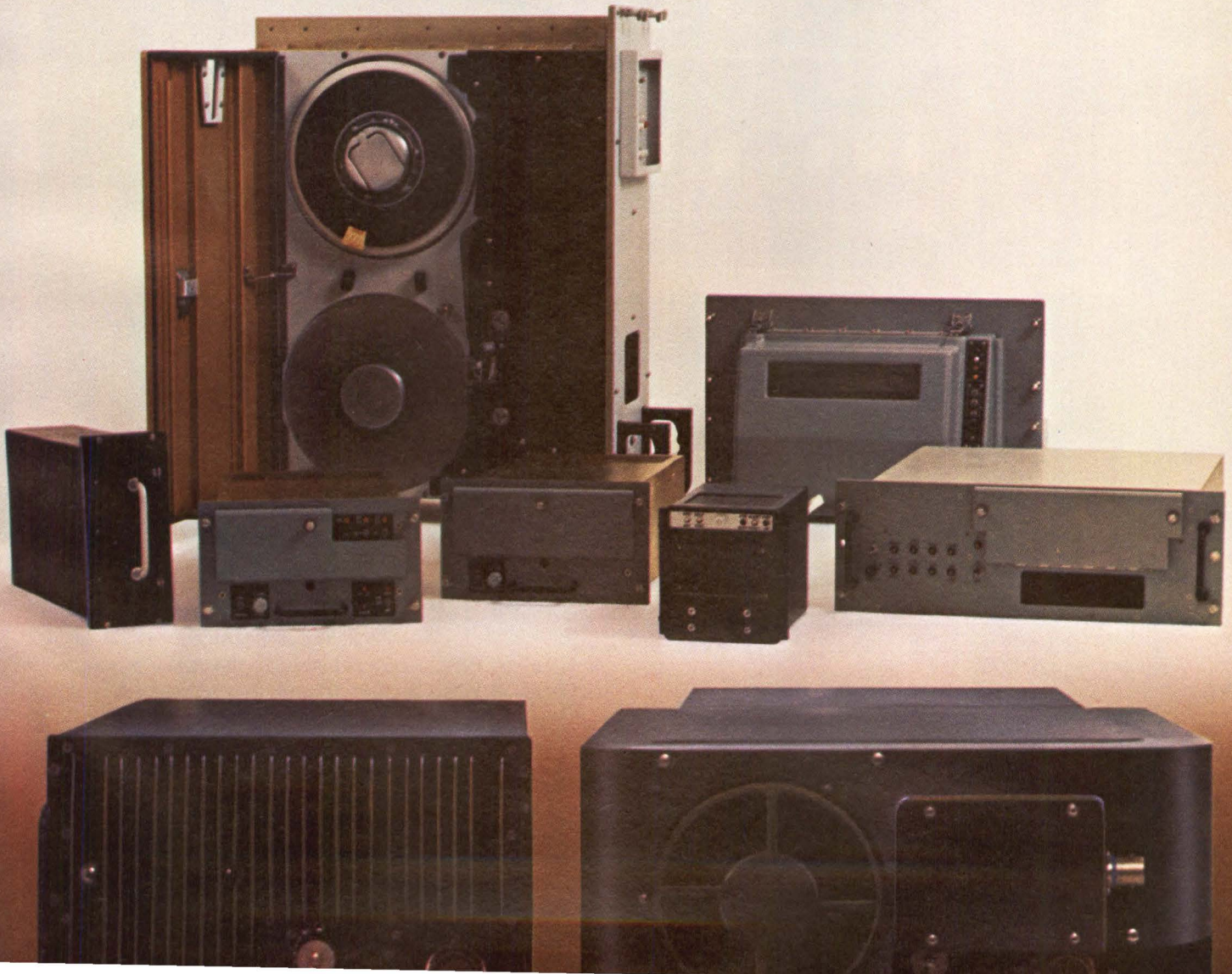
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# ROLM backs up its processors with Mil-Spec peripherals



# Microprogramming:



Advanced Micro Computers announces System 29, the world's first complete development system for microprogrammed machines. It's yours for under \$20,000.

There has never been a single tool available to assist in the complete development of microprogrammed machines. Until now.

System 29 is completely self-contained. It has everything from the microassembler that generates the code to the writable control store that simulates your PROMs. You build your prototype inside on universal cards. Or outside with interface and cables.

And you don't need to stop at hardware. System 29 comes with a resident microassembler, microcode editing and debugging capabilities,

# It's as easy as AMC.



and a time-proven disc-operating system.

We saved the best for last: System 29 saves you gobs of expensive time. Whether you're writing, debugging or documenting microprograms, your first job will go 50% faster. And you can bank on even greater time-saving after that.

So don't let microprogramming give you a hard time. Get System 29. It's as easy as AMC.

## Advanced Micro Computers



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troller, multilevel maskable vectored interrupt control, and a programmable interval timer and event counter. Areas to which the system may be applied are industrial process control and instrumentation systems, peripherals, diagnostic subsystems, test equipment, and commercial equipment.

The three devices are offered by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 in 40-pin plastic and ceramic DIPs. The 8755A-2, a 16k-bit EPROM that is pin and function compatible with the 8355-2, will be introduced later.

Circle 412 on Inquiry Card

### **Dc-Dc Converter's Triple Output Is Proportioned For Microprocessors**

The "sa" series module provides 30 W of isolated regulated dc-dc power for 8080 microprocessors and microcomputers. Standard input voltages are 12, 24, 28, 48, or 60 Vdc with output ratings of 5 V at 3 A, 12 V at 1 A, and -5 V at 0.5 A.

The 4 x 6 x 0.78" (10.16 x 15.24 x 1.98-cm) metal "V" package has turret terminals on one side, and a 24-in<sup>2</sup> (155-cm<sup>2</sup>) bottom mounting surface for external heat sink or chassis to maintain case temperature at less than 85 °C. Stevens-Arnold, Inc, 7 Elkins St, South Boston, MA 02127 performs 100% testing and a minimum of 100-h burn-in on the series.

The emi-rfi shielding consists of a 6-sided continual case shield, multiple transformer shielding, internal i/o filtering, and low noise circuit design. Specs include ±0.1% regulation, 60% power transfer efficiency at full load, 100-μs maximum load transient recovery time, and isolation of  $1 \times 10^9 \Omega$  min/500 Vdc min. Operating temperature range is -25 to 71 °C. Overvoltage protection is standard on the 5-V output.

Circle 413 on Inquiry Card

### **Simulator/Assembler Tools Facilitate μComputer System Design**

Plugging directly into the motherboard of EXORCISER/EXORterm development systems, the MEX6809SIM simu-

lator module and macro assembler serve as a development tool for the MC6809 microprocessor, which is to be announced shortly by Motorola Semiconductor Products, Inc, Microsystems Div, PO Box 20912, Phoenix, AZ 85036. The module holds P/ROMS containing an expanded version of EXBUG 1.2 and a program which simulates the CPU instructions. Also included is an MC6810 RAM to store simulated variables and an MC6820 PIA to handle user interrupts. A diskette contains the macro assembler and program to demonstrate the switch functions.

With the editor, processor source code is entered through the terminal console and stored on diskette. The assembler then assembles the program. This edit/assemble sequence continues until the assembly is error free. To perform debugging, the user loads the resulting object code into the development system's memory. Memory and i/o boards compatible with the EXORCISER may be used with the module to simulate other portions of the MC6809 microcomputer system.

Circle 414 on Inquiry Card

### **Rapid Information Exchange Is to Occur Through "Z Users Group"**

Formation of the "Z Users Group" by Jon D. Roland, its organizer, is intended to facilitate the interchange of information, services, and products among users of devices based on the Zilog Z8, Z80, Z8000, Mostek 3880, and other microprocessors in the family, and also to encourage further development of components and systems. Independent of Zilog, Inc, Mostek, or other producers or users of Z chips, the group will exchange data on the processors, software, and interfacing in systems through a newsletter, for which contributions are solicited. Dues for the group, located at 1015 Navarro, San Antonio, TX 78205, are \$5 per year.

### **Wirewrap Panel Handles Interface Designs for 6800 Microprocessors**

Dimensionally, i/o, and bus compatible with the 6800MMA Microdesigner

series panels, the wirewrap panel for the Motorola 6800 microprocessor interfaces memory, printer, or single-board computers used in the Micro-module family. Hybricon Corp, 410 Great Rd, Littleton, MA 01460 has placed 52 columns of 43 contact holes/column on a 0.100 x 0.100" (0.254 x 0.254-cm) grid pattern. Plated through holes allow mounting of any combination of ICs with from 8 to 40 pins. Maximum capacity is 95 16-pin DIPs.

The 2-6800MMA panel contains a combination of 10 uncommitted V<sub>cc</sub> and ground planes. The i/o structure has two 62-pin flat cable connectors and an 86-pin edge connector. Models are available in prepinned format with either nailhead or tin-gold socket pins.

Circle 415 on Inquiry Card

## **SOFTWARE**

### **Software Supports 9900 Family on Intel MDS Development System**

Pivot 9900, a cross support product, provides the Intel MDS-800 or Series II user with development support software for the 16-bit 9900 microprocessor family. The software is constructed to work with the user's ISIS-II operating system, in 48k of memory; editing, file management, and P/ROM programming remain functions of the operating system.

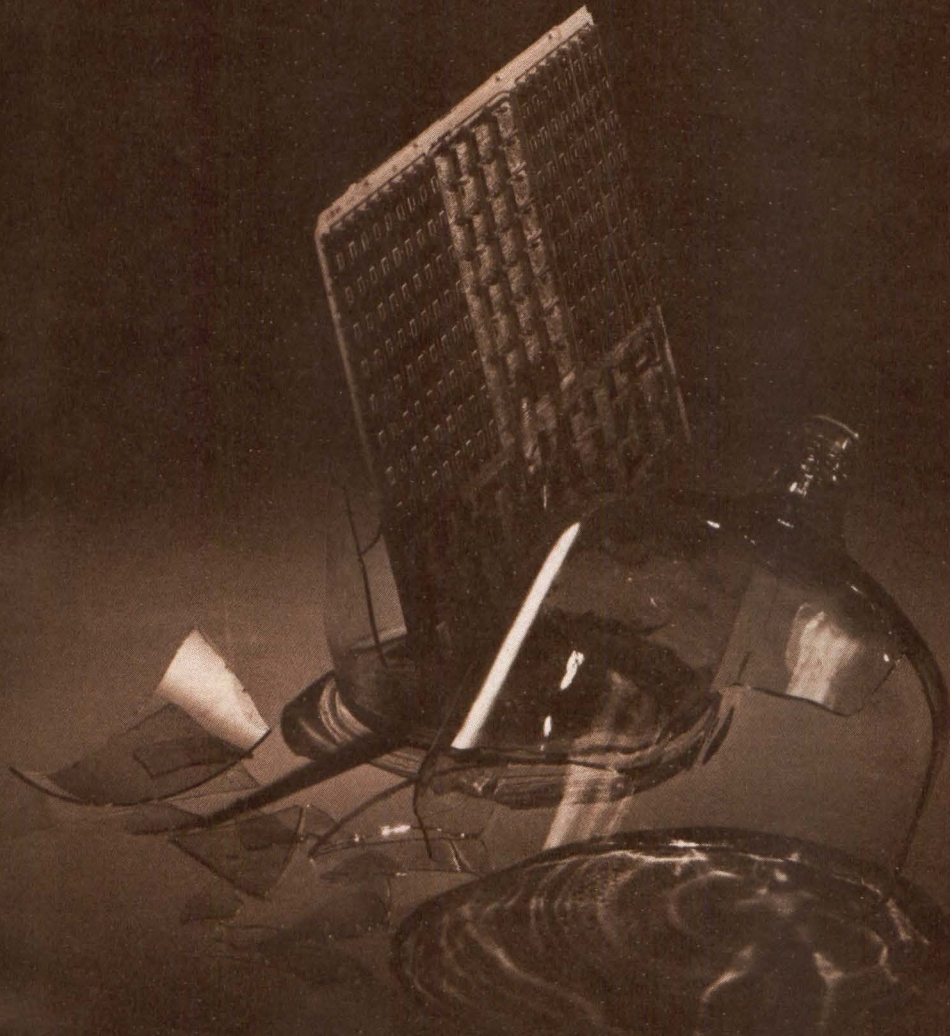
Various program modules comprise the package. Source files are created and modified using the ISIS-II text editor. The 9900 relocating, 2-pass cross assembler is then invoked to assemble these modules, producing object and list files.

A linking locator creates a module for the simulator, and if desired, an absolute object module for the P/ROM programming utility. Linker directives are contained in a command file. Performance measurement, debug, and error diagnostic features of the simulator allow verification of 9900 program designs. The simulator operates in batch mode or normal interactive mode.

After the 9900 code is debugged, the P/ROM programming utility converts an absolute module containing 16-bit words into two firmware data files containing 8-bit words. These meet the formatting requirements of Intel's P/ROM mapper software, which is used with the universal P/ROM programmer to create P/ROM firmware.



# Break the Nova 3 bottleneck



## with EMM 128K word memory

Let's face it. Even the Nova 3/12\* has a limited number of card slots. In typical system applications, there just are not enough slots to accommodate needed memory, controllers, and usual options. It's the classic bottleneck and something has to give.

Relax. That's a thing of the past. With EMM's 7706 add-in memory you can put all the memory the system can handle — 128K words — into a single slot. That frees up 3 slots when compared with memory available from the

computer manufacturer. If you don't need that much memory immediately, the 7706 is available in 32 and 64K versions as well. All are expandable to 128K. All offer significant cost advantages.

The 7706 is physically, electrically and functionally compatible with the Nova 3/4 and 3/12.

Call or write us today for complete details.



\*Nova 3 is a trademark of Data General Corporation.

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Either single- or double-density versions are available, together with documentation and one year of software upgrade packages. Processor Innovations, 118 Oakland St, Red Bank, NJ 07701 is planning to introduce Pivot 9940 in January as an add-on or standalone development package; 9900 family in-circuit emulation will be announced later.  
Circle 416 on Inquiry Card

### Debugging Is Achieved Through Simulation of 6800 Microprocessor

To replace hardware logic analyzers or CPU emulators, Technical Systems Consultants, Inc, Box 2574, West Lafayette, IN 47906 has announced an assembler language program debugging tool that simulates all functions

of the 6800 microprocessor. User defined breakpoints set in RAM or ROM invoke any of eight actions in any combination. These actions may be delayed or limited by a pass count. For profiling the executed program, histogram breakpoints can be set.

Trace mode allows viewing of the past 256 executed instructions, with registers and op code mnemonics displayed after each instruction is executed. Single or multiple instruction stepping and simulation speed control are permitted. An operator command halts program execution at any time.

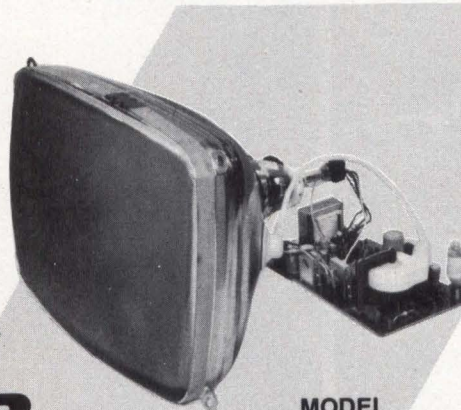
Write, execute, memory, or simulate protection of any section of memory, as well as execution traps allowing program exit on general conditions are featured. Also included are a line at a time assembler, disassembler, memory interrogation commands, hexadecimal calculator, machine states counter, stack protection, register modifier, and mode control.

In a related announcement, the company is making the FLEX™ 6800 disc operating system available for general OEM licensing. The utility command set residing on the system disc provides the user with control of all disc operations from the user's terminal. Support software to run under the system also is offered.

Circle 417 on Inquiry Card

## 12" CRT DISPLAY MONITOR

Compatible with TV12 or TV120  
Priced Below the Competition  
Built-in Quality, Performance, Dependability



MODEL CIQ-12 (Kit)

The low-cost CIQ-12 CRT Display Monitor provides data equipment manufacturers with sharp, highly reliable image presentation.

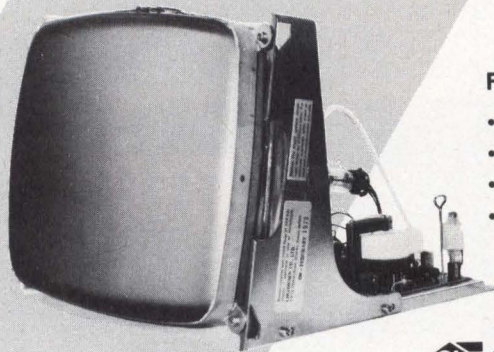
Separate horizontal drive, vertical drive, and video signal inputs mean elimination of composite sync and video signal processing and simple output circuitry.

The completely new design of the compact integrated PCB utilizes the latest semiconductor and other components, providing a dependable performance level never before possible.

Delivered with P4 phosphor as standard. Available options are P31 and P39 phosphors, sturdy zinc chromate plated chassis and a power supply module which is compatible with practically any power supply standard in the world.

#### FEATURES

- Uniform High Resolution
- Integrated PC Board
- Dependable Construction
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(with optional chassis)

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### Simulator for 6502 Assists In Design and Testing of 8080 Software

Executing the full 8080 instruction set, the 8080 simulator is configured for the KIM-1, supporting register single step, program counter single step, and run modes. An input and output port, breakpoint operation, and rejection of illegal op codes are also offered. Internal 8080 registers are maintained so that contents may be examined or modified.

Up to 224 bytes of 8080 programming space is available with an unexpanded KIM-1, since the simulator runs in less than 1k of memory. It is ROM relocatable and can be adapted to other 6502 based systems.

Dann McCreary, 4758 Mansfield St #2V, San Diego, CA 92116 designed the simulator for use as a training aid, and for testing, designing, and running 8080 application software (except for time sensitive applications). A KIM-1 format cassette tape, user manual, and commented assembly level source/object listing comprise the package, priced at \$18, plus \$1.50 postage and handling. □

Circle 418 on Inquiry Card

# Formula for memory metamorphosis



## High-speed Static NMOS memory from EMM

Are you condemning your system to dynamic memory speeds? It's time to move up to high-speed static NMOS memory technology.

The EMM MICRORAM 3420 is your formula. It contains 32K by 21 bits of memory on a single pluggable module. Yet it accesses in 200 nsec, and cycles in 300. And it incorporates a Late Data Control which allows a delay in the execution of a write cycle pending the arrival of data.

The 3420 saves power, too. Typically it draws less than 30 watts in standby, less than 40 watts in operate mode. System design is very simple, as the static RAMs require no charge pump or

refresh circuitry. And they don't generate soft-bit errors, so reliability is much higher than with dynamic RAM systems.

Other versions of the MICRORAM 3400 Series are available in 16 to 22 bit configurations, 8 to 32K capacities, and access times as low as 180 nsec.

Transform your system from sluggish dynamic to reliable high speed static NMOS memory. Call or write today for full technical details as well as price and delivery information.



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## MICROCOMPUTER DEVELOPMENT SYSTEM OFFERS ADAPTABLE TEST CONFIGURATIONS

**Alan W. Bentley**

Cubic Corporation, Defense Systems Division  
San Diego, California

**A** survey of microprocessors to determine the optimal choice for a data acquisition system application requiring arithmetic processing of 12-bit analog-to-digital converter output with a minimum of 24 bits of resolution to identify anomalies in the input signal led to the selection of the TMS 9900 microprocessor. This is primarily because of the arithmetic capabilities of its instruction set and the 16-bit data bus, which provides 32 bits of resolution when using double-precision data manipulation.

Existing compact microcomputer development systems, which would be suitable for both prototype and service installation and testing, were dedicated to 8-bit 8080 or 6800 architectures. Since these systems were not compatible with the desired central processing unit (CPU) and its wide data bus, the decision was made to simultaneously design an associated development system. This system was required initially to perform the functions of prototype hardware checkout and software development, and subsequently, to field-test the final configuration. Fulfilling these goals required a general purpose hardware design approach that stressed portability, low power consumption, and versatile front panel controlled testing.

In addition, the following overall system requirements had to be fulfilled: (a) response time less than CPU cycle time to perform desired functions in CPU real time, (b) data monitoring transparent to CPU system, (c) no restrictions on CPU hardware or software, (d) no appreciable loading on bus and control lines, and (e) no interface modifications to CPU hardware or software.

### Data Acquisition System

The microprocessor based data acquisition system is designed around the TMS 9900 CPU (Fig 1), which has a 16-bit data word divided into two 8-bit bytes. Internally, the CPU is byte oriented, but external addressing is word oriented. Addressing capability is  $2^{16}$  bytes, or

$2^{15}$  words; therefore, there is a 15-bit external address bus (A0 to A14), with a sixteenth least significant address bit (LSB), A15, contained internally for byte manipulation. For both the address and data buses, the most significant bit (MSB) location is labeled zero; thus, the 16-bit data bus is labeled D0 through D15 and the 15-bit address bus is labeled A0 through A14, both MSB to LSB.

The system algorithm processes 12-bit digitizations of analog voltages, forms a Gaussian distribution by determining background and variance values, and then performs exponential smoothing to update these values, thereby allowing the tracking of slow signal variations while searching for discontinuities in the changing input data. To perform the programming tasks for implementing the system algorithm and servicing the display interface with the CPU instruction set, 512 x 16 words of read-only memory (ROM) and 256 x 16 words of random-access memory (RAM) are required. Consequently, memory is partitioned into pages of 512 words, using the nine least significant address bits (A6 through A14). The six most significant address bits (A0 through A5) are available for page addressing, allowing up to  $2^6$  (or 64) pages to be uniquely addressed. Since all external addresses are even, due to word orientation, the span of addresses is twice the number of unique locations. For example, the first (or ROM) page of 512 locations is addressed  $0000_{16}$  through  $03FE_{16}$ , using only even addresses ( $0002_{16}$ ,  $0004_{16}$ , etc). Address bits A3 through A5 are demultiplexed to become address vectors Y0 through Y7, representing decoding for the 8 lower order pages of the available 64. Five of these address vectors (Y0 through Y4) are used for software control of system functions, and one address vector (Y5) is delivered to the development system as a programmable storage command (strcmd). The last two address vectors (Y6 and Y7) are unused, along with the upper address bits A0 through A2 and

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STOP PROGRAM:  
 RUN • illadd + CLOCK • ph2 + IAQ • iaq +  
 BKPT (NORMAL + PROG) "equal"

ADDRESS VECTORS	HEX ADDRESS SPAN	
Y0	ROM ENABLE	0000-03FE
Y1	RAM ENABLE	0400-05FE
Y2	A-D ENABLE	0800-0BFE
Y3	DISPLAY STORAGE	0C00-0FFE
Y4	INTERRUPT CLR	1000-13FE
Y5	PROGRAM STORE COMM	1400-17FE
Y6-Y7	NOT USED	1800-1FFE

\*ILLEGAL ADDRESS:  
 $A0 + A1 + A2 + Y6 + Y7 + Y1 \cdot A6$

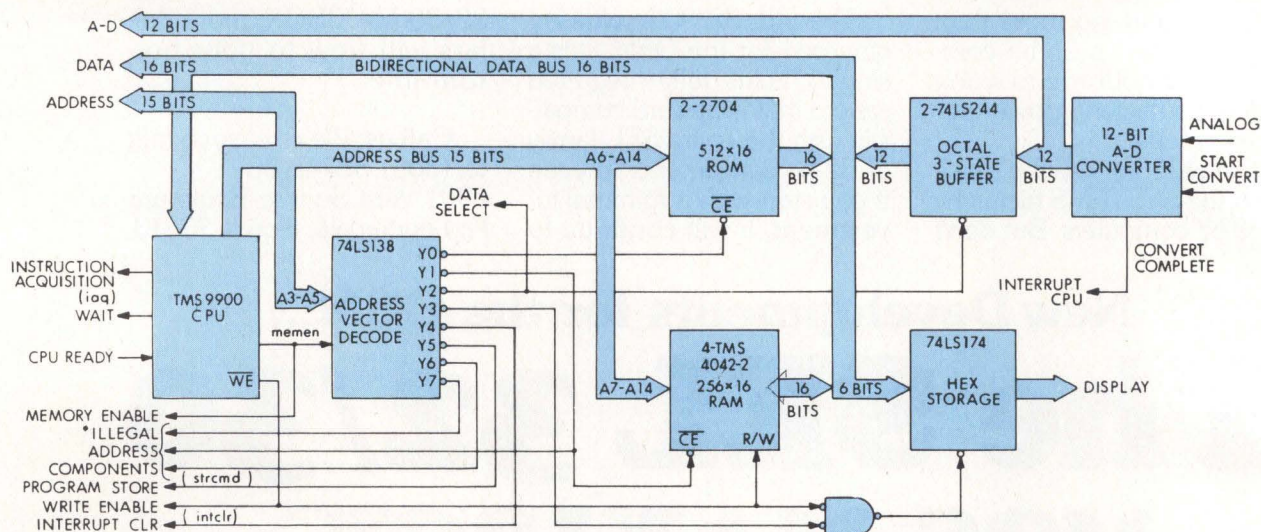


Fig 1 Microprocessor based data acquisition system. Block diagram shows origin of development system interface signals and functional control by address vectors. Listing defines address range and function of address vector decoder outputs Y0 to Y7. Stop program expression allows dynamic operation while monitoring address boundary. Also, program may be stopped at selected breakpoint, at each instruction acquisition cycle to verify ROM program, or at each clock cycle to monitor instruction execution and interregister data transfers

the upper portion of RAM address page  $0600_{16}$  through  $07FE_{16}$ .

These unassigned signals, however, are hardwired to form an illegal address expression (Fig 1) for detecting illegal or unused addresses during checkout. The 64 memory pages can be considered as 8 sets of 8 pages each, with only the lowest set valid for this application. To address the lowest set, three address bits ( $A0, A1$ , and  $A2$ ) must be false. The seven unused sets are addressed when one (or more) of these three bits is true; therefore, the condition " $A0$  OR  $A1$  OR  $A2$  is true" forms a portion of the illegal address expression, along with component " $Y6$  OR  $Y7$ ." The remaining component ( $Y1$  AND  $A6$ ) represents the unused upper half of the RAM address page. Since  $A6$  is the most significant address bit within the page, it is false for the lower or RAM half of the page, and true for the upper or unused half of the page.

### Microcomputer Development System

In the development system (Fig 2), one of three input sources—address bus, data bus, or analog-to-digital (A-D) converter output—is selected by the source switch for routing to a 16-bit comparator. The comparator continuously relates the selected source signal with the setting of four hexadecimal thumbwheels. When the selected input value equals the thumbwheel settings, an Equal signal is issued to either store data or to suspend CPU operations. Additionally, the selected input source and data bus are both available to a 16-register last in, first out

(LIFO) stack via the store control switch. Stack storage commands and data inputs are controlled by the source and store control switch positions and appropriate logic commands.

Storage flexibility is shown by the store command expression and tabular listing (Fig 2). For example, when the store control switch is in the COMP (comparator) position and the source switch is in the address position, if the thumbwheel settings and address bus are equal on a data write cycle, then the contents of the data bus are stored in the LIFO stack. Thus, this store operation uses the Memory Enable (memen), Equal, and Write Enable (we) commands as qualifiers, and allows all data written into an operator-selected address to be stored in the stack. The latest stack entry or the input bus signal selected by the source switch is routed by the display switch to the 4-character hexadecimal display.

Three address vectors—A-D Enable ( $Y2$ )  $0800_{16}$ , Display Storage ( $Y3$ )  $0C00_{16}$ , and Interrupt Clear ( $Y4$ )  $1000_{16}$ —are used in conjunction with a move (MOV) instruction for system digital control. Coded within the move instruction are a source address and a destination address, and upon execution, a 16-bit data word is moved accordingly. The A-D converter reading is stored in RAM by executing a move instruction with source address  $0800_{16}$  ( $Y2$ ) and the destination address within RAM address span  $Y1$ . Address vector  $Y2$  is used to switch the 3-state buffers to the active mode, placing the A-D converter output on the data bus; with the destination address bits  $A7$  through  $A14$  applied to the RAM address

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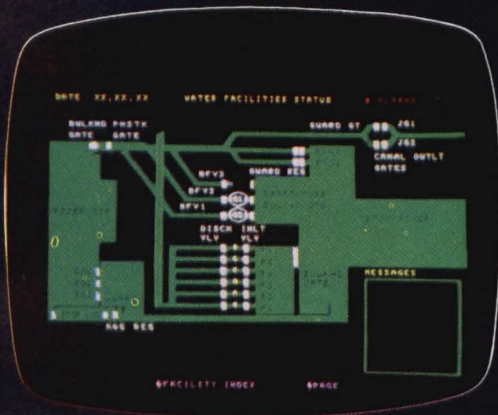
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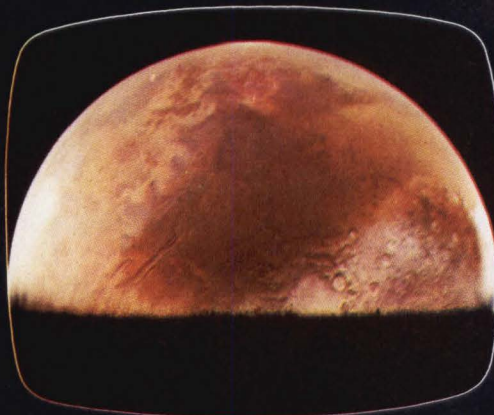
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CIRCLE 59 ON INQUIRY CARD



TABULAR REPRESENTATION OF STORE COMMAND EXPRESSION

STORE CONTROL SWITCH	SOURCE SWITCH	DATA STORED	QUALIFIERS	REMARKS
NORMAL	ADDRESS	ADDRESS	"memen"	TRAIL OF LAST 16 ADDRESSES
NORMAL	DATA	DATA	"memen"	TRAIL OF LAST 16 DATA WORDS
NORMAL	A-D	A-D OUTPUT	"memen" "dtasel"	TRAIL OF LAST 16 A-D CONVERSIONS
COMP	ADDRESS	DATA	"memen" "equal"	TRAIL OF LAST 16 UPDATES OF DATA IN MEMORY LOCATION
PROGRAM	XXX (ANY POSITION)	DATA	"write enable" "memen" "strcmd" "write enable"	SELECTED BY THUMBWHEELS TRAIL OF LAST 16 DATA WORDS WRITTEN TO STACK UNDER PROGRAM CONTROL

Note: When storing slowly changing data in the stack using COMP or PROGRAM, data can be monitored in real time by placing "DISPLAY" switch to MEMORY.

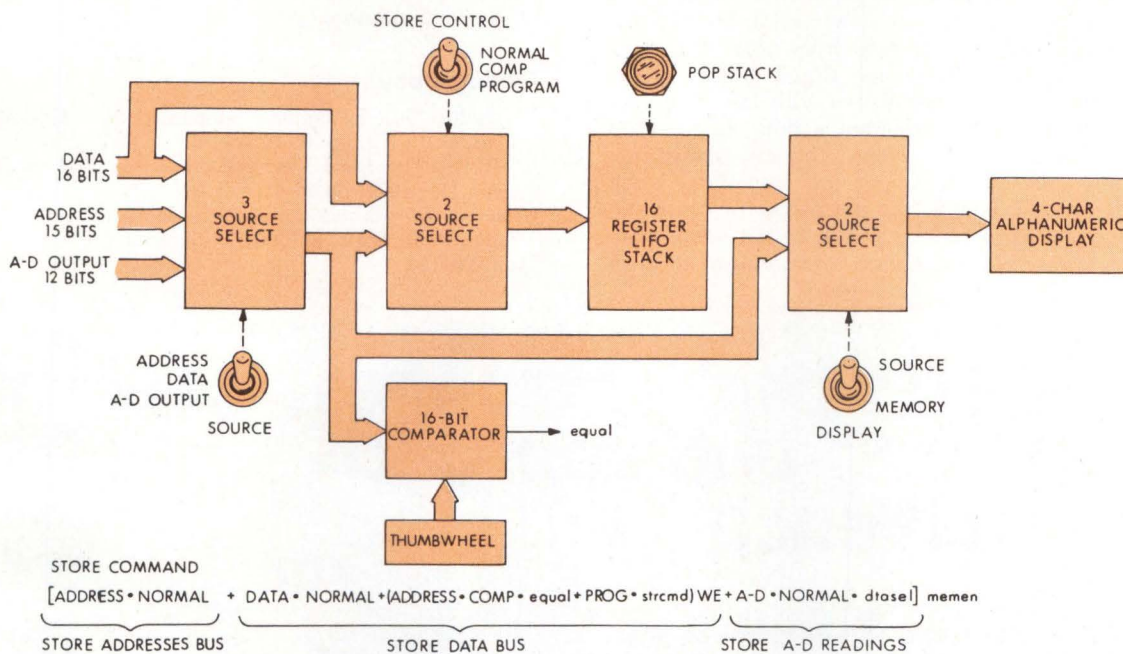


Fig 2 Development system data flow. Functional diagram shows routing of system buses to comparator, stack, and display. Store command expression and tabular listing demonstrate flexibility of data storage selection

inputs and the RAM address vector Y1 applied to RAM Chip Enable (CE), then the A-D converter reading is written into a RAM location. Address vector (Y2) is used as a "dtasel" (data select) command to signify that valid A-D data are on the CPU data bus. Vector Y3 is used to store the six LSBs of the data bus (D10 through D15) in a hexadecimal storage flop for system display. Again, the move instruction is used, the source address is the data location in RAM, and the destination address is  $0C00_{16}$ . Vector Y3 is ANDed with Write Enable (WE),

and this output strobes the data bits into the hexadecimal storage flops.

Vector Y4 is generated with  $1000_{16}$  as the destination address of a move instruction. Since this is a control function and data are not used, the source address can have any value. When executed, Y4 clears the interrupt flop.

The address vector output Y5 (address  $1400_{16}$ ) is routed to the development system as a store command. With the store control switch in the program position, a move instruction with a RAM source address and  $1400_{16}$

as the destination stores the addressed data in the LIFO stack. This provides a means of saving computational results, while also allowing the stored values to be monitored in real time if the display switch is in the memory position.

### System Test Control

Operation of the data acquisition system can be varied by a mode switch that externally controls the CPU ready line (Fig 1). During each memory cycle, the CPU tests its ready line; if it is false, CPU operations are suspended and a wait state is entered, illuminating a wait lamp. The current value of the input sources may be examined by using the source switch, and placing the display switch in the source position. While in the wait state, the CPU continues to sample the ready line. When this line returns true, the suspended memory cycle is completed and CPU processing is resumed.

The mode switch has four positions, which allow selection of test functions. In the run position, the address bus is monitored, and the program will stop on an illegal address. The clock position will stop the CPU during each memory cycle, allowing monitoring of inter-register transfers. The IAQ position uses the CPU's instruction acquisition (iaq) output signal, which becomes true each time the CPU fetches a new instruction, to suspend operations. This permits program flow tracing by monitoring each instruction as it is fetched from ROM. The BKPT (breakpoint) position monitors the Equal output of the 16-bit comparator and, in conjunction with the store control switch, determines the resultant action. As the stop program expression (Fig 1) shows, the CPU ready line is driven false and CPU operations are suspended when the store control switch is in the normal or program position. Moving the store control switch to the COMP position, however, uses the comparator Equal output to push

the contents of the data bus onto the LIFO stack. Contents of the LIFO stack may be examined by the use of the pop stack pushbutton with the display switch in the memory position. The continue pushbutton sets the CPU ready line true, allowing the CPU to resume operation from the point of suspension, or the program can be restarted by use of the reset pushbutton.

Data under program control, data written into any selected address, or a trail of the last 16 values of the bus selected by the source switch can be stored in the LIFO stack. The program can be allowed to run without interruption while monitoring the address bus for illegal addresses, or while storing and displaying data written into any address; when desired, processing can be suspended at any address. Also, the CPU can be stepped through each Memory Enable cycle to monitor instruction execution, or through each instruction acquisition cycle to monitor instruction flow.

The development system, including controls and display, is mounted on a 60-in<sup>2</sup> (387-cm<sup>2</sup>) printed circuit board, has a single voltage power requirement of 4 W at 5 V, and mates with the microprocessor based data acquisition system through a test connector. Hardware implementation of the development system is an efficient design approach, as it fulfills the requirements of software development, hardware checkout, and test support by test configuration flexibility.

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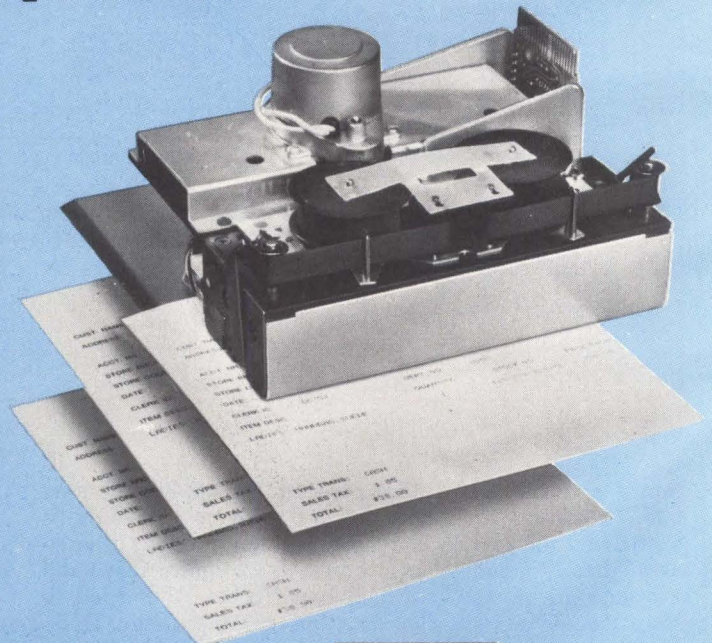
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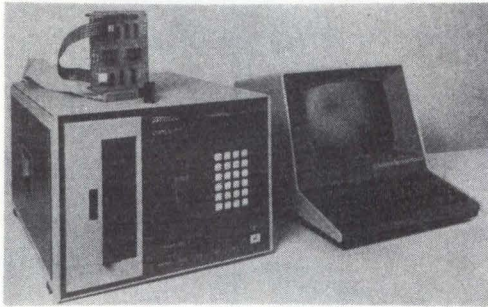
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## Single-Chip 4-Bit Microcomputer Family Matches Optimum Microcontroller to Specific Low End Needs



Covering microcontroller development activities from concept to production, COP400 Product Development System is based on 16-bit microcomputer. It includes editor, macro assembler, and emulator card attachment. Functional test module handles incoming inspection

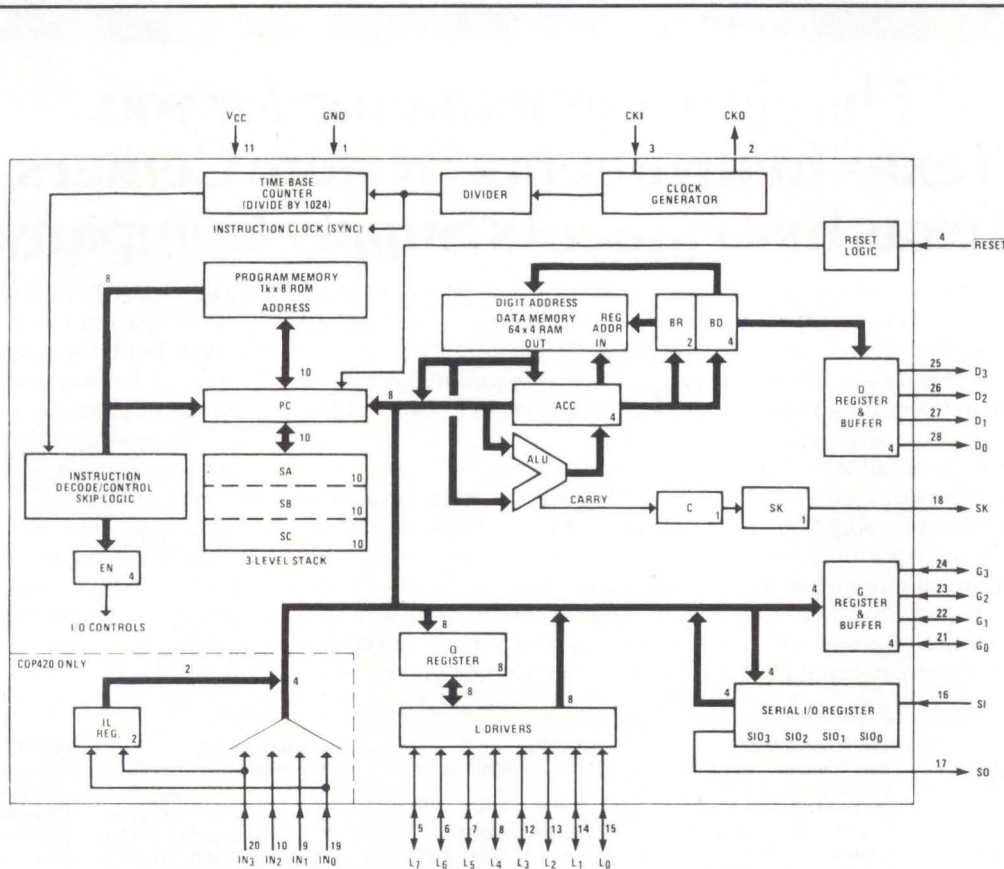
The COP400 series of microcontrollers, consisting initially of 12 devices, are computers on a single chip with the necessary system timing, internal logic, ROM, RAM, and I/O to implement dedicated low end control functions in

such high volume applications as clocks, timers, laboratory instruments, calculators, sequencers, and radio and appliance controllers. Range of members allows the user to specify a microcontroller to meet a particular ap-

plication, eliminating most needs for external interface logic. Memory, I/O, and speed of parts vary, as do the electrical characteristics. Various clock, I/O, and other options are mask programmed into the device when the ROM is coded with the user's dedicated program.

National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051 has designed the instruction sets, internal architecture, and I/O schemes to ease keyboard input/display output and provide efficient BCD data manipulation. Three fabrication processes used are an advanced high speed NMOS, a low power NMOS, and lower power CMOS.

All devices operate from a single supply and feature standardized test procedures to verify the internal logic and user program. Typical interfaced

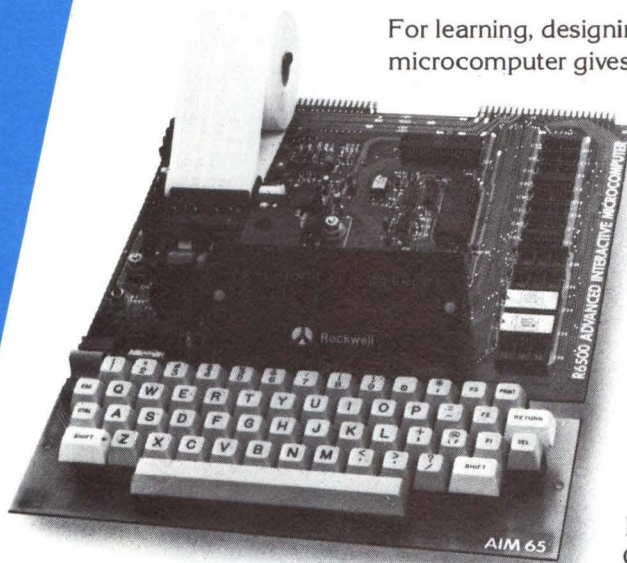


Designated COP400 series, National Semiconductor's family consists of 12 single-chip microcontrollers. Typical device is COP420/421. NMOS microcomputer contains system timing, internal logic, ROM, RAM, and I/O, providing customized control oriented processor at low end-product cost for medium to large volume users

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devices include keyboards and displays, external memories, printers, other COP devices, ADCS, DACS, power control devices, and general purpose microprocessors. Software/hardware compatibility exists among the family devices.

Program development for the series is facilitated by the cops Product Development System (PDS) that is also being introduced. Built around a 16-bit microcomputer, 32k bytes of R/W memory, and 12k bytes of P/ROM firmware, the disc based system has a circuit fixture for incoming inspection of the devices, as well as an editor and assembler for handling source code entry, conversion to object code, and maintenance of documentation. An in-circuit emulator card attachment allows object code to be executed under control of a COP monitor debug utility.

Central configurations of the family are the 28-pin DIP COP420/420L/420C devices, with 1k x 8 ROM, 64 x 4 RAM, vectored interrupt plus restart, 3-level subroutine stack, 23 I/O lines, 57-command instruction set, internal time-base counter, internal binary counter register with serial I/O capability, general purpose and Tri-State™ outputs, and LED direct drive. The NMOS 420 operates over a 4.5- to 6.3-V single supply range and has a 4- $\mu$ s instruction cycle execution time. Operating supply current is 20 mA at 5 V.

Differences with the low power (40 mW, max) NMOS 420L are a 4.5- to 9.5-V supply range, 16- $\mu$ s instruction cycle execution time, and divide by 32 crystal clock option. The CMOS version, 420C, has a 2.4- to 6.3-V operating supply range; a dual clock mode option permits operation either at low speed (244  $\mu$ s) with low power consumption or at high speed (16  $\mu$ s) to perform internal data computations at a faster rate. A timed pause mode is provided that can be entered under program control.

The 24-pin 421/421L devices are identical to the 420/420L except that they have 19 I/O lines and no interrupt capability. With the same electrical specs as the 420L/421L, the 24-pin 410L and 20-pin 411L instead have 512 x 8 ROM, 32 x 4 RAM, 43 instructions, two stack levels, no interrupt capability, and 19 and 16 I/O lines, respectively.

Expanded versions of the 420/420L, the 440/444L have the same instruc-

tion set and double the memory—2k x 8 ROM and 128 x 4 RAM. The 40-pin 440 has 36 I/O lines, while the 28-pin 444L has 24 lines. The MICROBUS™ compatibility option for the 420 and 440 allows it to operate as a peripheral microprocessor device. As such, it inputs and outputs data to and from any host microprocessor in the company's MICROBUS compatible family of 8- and 16-bit microprocessors.

The 40-pin 402 and 404L, alternate versions of the 420 and 444L respectively, contain no ROM. They

are applicable to prototyping a COP-400 system using the COP PDS. In quantity, they suit small volume applications using up to 1k x 8 and 2k x 8 bits of external ROM. The 402M is a MICROBUS compatible version of the 402, for use in prototyping systems in small applications that use the 420 as a host CPU peripheral component. Additional members to be introduced will feature expanded hardware and software capabilities, alternative electrical specs, and smaller devices for less demanding applications.

### Integrated Design of Computer Produces Portable System

Processor and peripherals have been integrated by Durango Systems, Inc, 10101 Bubb Rd, Cupertino, CA 95014 to form a portable computer system slightly larger than a typewriter. The basic F-85, containing only 40% of the parts of other systems, includes a processor with 8k of ROM and 48k of RAM, two random access diskette drives with almost 1M characters of storage, a 1920-character CRT display screen, keyboard with 10-key pad, and 165-character/s bidirectional matrix printer. It is priced at \$13,520. A second microprocessor and two intelligent controllers handle and optimize the performance of the printer, diskette drives, and display screen.

Weighing about 65 lb (29 kg), the system is supplied with the dx-85 single tasking operating system and dx-85M multitasking system that can

handle up to five programs operating simultaneously. D-BASIC compiler/interpreter, a commercially oriented BASIC language with extended capabilities, is available, as are small business applications software packages. The software supports ISAM, sequential, and random file capabilities.

Without affecting the unit's size, the system can be expanded to include 65k of memory, almost 2M bytes of RAM on diskette, and communications capabilities. A further increase can be made with the addition of up to four auxiliary keyboard/CRT units, and a dual diskette drive unit for a total of almost 4M bytes. A random access fixed disc drive with capacities of 10M and 20M bytes will be offered later.

The system operates from a standard 110-V outlet. This low power requirement allows an optional standby power unit to protect the user's file from power failure and to provide automatic restart upon power resumption.



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Portability of Durango Systems' F-85 desktop computer, achieved through 40% reduction in parts, is major factor for small business users. It also suits intelligent terminal applications of larger users

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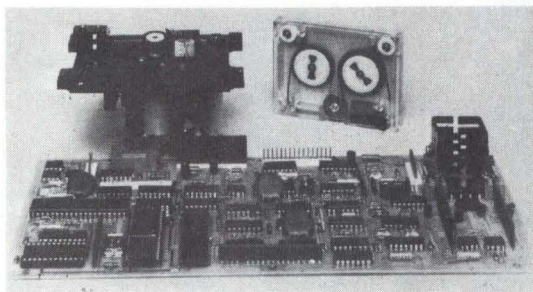
A data storage component employing magnetic tape cartridges provides OEMs with an inexpensive means of building mass storage capabilities into microcomputer systems. DEctape II provides up to 262,144 bytes of auxiliary data storage per cartridge. Recording data in block addressable form, the TU58 subsystem enables blocks to be replaced randomly, without disturbing data that has previously been recorded.

A microprocessor employed in the TU58 controller handles tape motion when seeking a location. The cartridge

drive can thus be operated with simpler software than is usually required, and as an added benefit reduces overhead of the host computer.

The unit from Digital Equipment Corp's Components Group, One Iron Way, Marlborough, MA 01752 connects to DLV11 or DLV11-J interfaces for use with the LSI-11 or PDP-11/03; it may also be used with other processors. Features include asynchronous, full-duplex serial output, and jumper selectable baud rates from 150 to 38.4k.

A maximum of two drives may be connected to a controller. A single drive with controller is \$446 per subsystem (100-unit quantity). Additional drives, also 100-unit quantity, are priced at \$116 each.



Circle 420 on Inquiry Card

DEctape II component level data storage system interfaces with Digital Equipment Corp's LSI-11 and PDP-11/03 microcomputers. TU58 subsystem cartridge drive records data in block addressable form, facilitating data replacement

## Analog I/O Board Couples With LSI-11s to Perform Signal Data Processing

SineTrac LSI series of analog interface boards slide directly inside the card cage of an LSI-11 or PDP-11/03 microcomputer, transforming it into a programmable data logger, industrial process controller, data acquisition system, or other form of signal data processor. Built into the board is the ability to modify software and add on hardware in order to manage changes.

Three circuit boards comprise the series. The primary board is an A-D/D-A master peripheral with a maximum of 32 single-ended or 16 differential A-D channels and 2 optional D-A channels. A Pacer clock with 16 programmable timebases, interrupt circuit, and 4-bit digital outputs are included. An optional  $\pm 15$ -V dc-dc power converter eliminates external power requirements. Featured are 12-bit binary resolution, 25k-sample/s throughput rate, and optional pro-

grammable gain or low level instrumentation amplifier. Pricing starts at \$625 for a board with only 16 single-ended A-D channels.

The slave A-D multiplexer expander, adding another 32 single-ended or 16 differential channels to the system, offers a maximum of 64 single-ended channels on two boards. The master board controls and powers the expander board. Both boards occupy two 8.5 x 10" (21.6 x 25.4-cm) quad positions in the microcomputer; other master/slave combinations may be added.

The third board, an 8.5 x 5" (21.6 x 12.7-cm) 4-channel D-A analog output peripheral, can be cascaded. Digital outputs are included for external device select lines, pen up/down controls, and write/erase commands. Options are dc-dc  $\pm 15$ -V power converters.

A-D throughput period is 20  $\mu$ s, and input ranges are 0 to 5, 0 to 10,  $\pm 5$ , or  $\pm 10$  V. Eight channels accept shunt resistors for current input ranges. Accuracy of the A-D section without the

amplifiers is  $\pm 0.025\%$  of FSR,  $\pm \frac{1}{2}$  LSB. Full-scale drift is  $\pm 20$  ppm of FSR/ $^{\circ}$ C. Inputs sustain  $\pm 35$ -V continuous overvoltage.

Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021 includes a diagnostic program on paper tape. Octal printouts of A-D data are obtained as soon as signal inputs are connected and the diagnostic is loaded. For troubleshooting, the program tests all data paths by looping on error conditions for study by oscilloscope or logic analyzer. The A-D output may be routed to the D-A section for comparison; sawtooth patterns may be generated by the D-As.

Circle 421 on Inquiry Card

## Expansion Board Interfaces S-100 Type Boards to PET $\mu$ Computer

Attaching directly to the Commodore PET microcomputer's memory expansion connector, the Betsi interface board provides interface logic and four S-100 slots. It operates from any S-100 power supply, without interfering with the computer's parallel or IEEE ports.

Announced by Forethought Products, PO Box 8066, Coburg, OR 97401, the single 10 x 5.5" (25.4 x 13.9-cm) board contains an onboard dynamic memory controller for the s.d. Sales "Expandoram" memory board. This permits the computer's memory to be expanded to 32k with a single S-100 card. Sockets and decoding circuitry for 8k of P/ROM (2716) allow for additional firmware. Prices are \$119 for the kit, \$165 assembled and tested.

Circle 422 on Inquiry Card

## Analog I/O Board Includes Digitally Controlled Amplifier

Plug-in compatible with Intel SBC-80, Intellec<sup>®</sup> MDS, and National BLC-80 microcomputers, the MP8418 microperipheral offers 12-bit resolution with 31-channel analog input and 2-channel analog output. The CPU treats these analog systems as memory.

Analog input portion of the board includes overvoltage protection to 24 Vdc; provision for up to eight 4-



# Gold medal FORTRAN



## Interdata FORTRAN VII

FORTRAN VII makes our fast-running 8/32 computer even faster. It comes in ahead of any other comparably-priced FORTRAN system. Faster by factors of five, ten, even 100, in execution time benchmark comparisons.

For example, when we ran a Table-handling Binary Search (40KB Array) with FORTRAN VII, it took only 26 seconds. On other systems, the best previous time recorded was about two minutes.

To achieve this speed without compromise, we brought together a group of mathematicians; their assignment was

to find and refine algorithms to establish new standards of accuracy for the industry. They did just that.

### **Optimizing makes it fast.**

FORTRAN VII speed is in the optimizing compiler: not local, not block, not peephole, not window, but global. Global optimization gives the FORTRAN VII compiler the high-level intelligence which compresses FORTRAN programs into absolute minimum run times.

### **How fast will your programs run?**

You can measure Interdata FORTRAN VII performance against your standards:

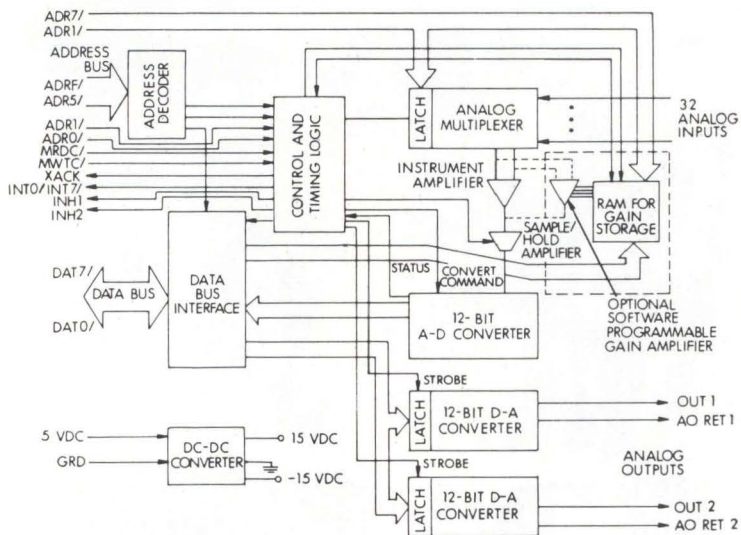
run your FORTRAN programs on our system and make your own unquestionable comparisons. There is no obligation, of course. For more about FORTRAN VII or to arrange to run your program, please call us:

Toll-free: (800) 631-2154

New Jersey (201) 229-6800, or TWX 710 722-3897.

Arcueil (Paris) 1 664-4110	Slough (England) 0753-34511
München 089 753081	Sydney 612-887-1000
Singapore 2200949	Toronto (416) 677-8990

**PERKIN-ELMER**  
Data Systems



High and low level inputs are features of the analog I/O system developed by Burr-Brown. Electrically and mechanically compatible with Intel's Multibus<sup>®</sup> and other similar microcomputer configurations, 15-channel differential board has input portion of analog multiplexer, resistor or software programmable amplifier, sample/hold amplifier, and 12-bit ADC. Output section—two 12-bit DACs—is optional

20-mA inputs; analog multiplexer; sample and hold amplifier; and 12-bit ADC. A software programmable amplifier or resistor programmed instrumentation amplifier can be selected. The programmable amplifier offers 11 binary weighted gains from 1 to 1024, suitable for low signal level applications. An onboard RAM allows the proper gain for each channel to be set automatically when the channel is addressed.

Designed by Burr-Brown Research Corp, International Airport Industrial Pk, PO Box 11400, Tucson, AZ 85734 for high and low level inputs, the

board is available with an optional analog output system, consisting of two 12-bit DACs with control logic and double buffered inputs to minimize glitches. A dc-dc converter also is included.

One expander board extends the system to 63 differential channels. Another input channel is used as ground reference for automatic calibration.

The board features memory mapping and easy programming. With resistor programmed gain, it costs \$450; with software programmed gain, \$550.

Circle 423 on Inquiry Card

### Microcomputer Offers Onboard Keyboard, Printer, and Display

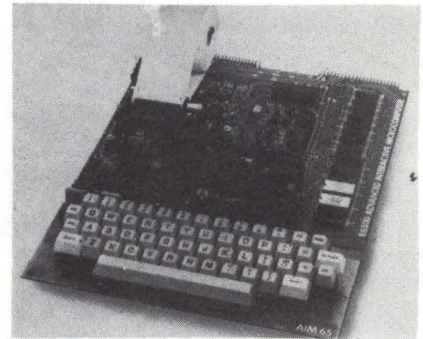
Intended as an educational aid and general purpose or development microcomputer, the R6500 Advanced Interactive Microcomputer (AIM 65) incorporates a 20-column printer, 20-character alphanumeric display, and 54-key terminal style keyboard. Both the 1k- and 4k-byte RAM versions are

designed around the R6502 CPU, which has 65k address capability with 13 addressing modes, true indexing, and decimal and binary functions.

The 8k ROM resident monitor program provided by Rockwell International's Electronic Devices Div, 3310 Miraloma Ave, PO Box 3669, Anaheim, CA 92803 contains a set of self-prompting debug and text editor commands. Programming is done at assembly language level with mnemonic

instruction entry and memory disassembly functions.

With spare sockets, memory can be expanded to 20k bytes via user P/ROM based programs or the company's 2-



pass assembler and BASIC interpreter ROM options. An edge connector allows external access to the system bus for memory and I/O expansion. A separate connector interfaces a TTY and two standard audio cassette recorders. It includes a Versatile Interface Adapter (VIA) that has three 8-bit bidirectional ports (two parallel, one serial) and two 16-bit programmable interval timer/event counters.

Circle 424 on Inquiry Card

### Three Components Are Standalone, 8-Bit Parallel Microcomputers

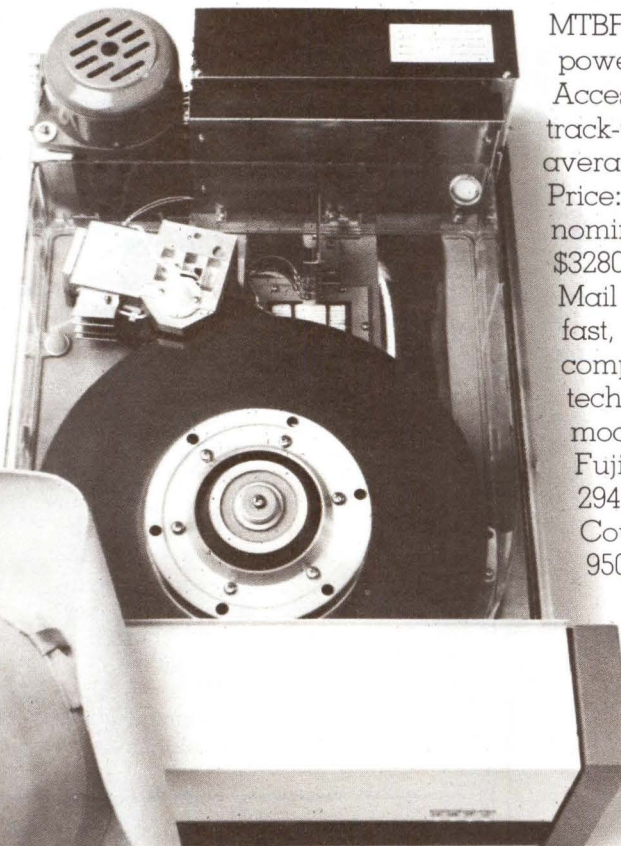
The  $\mu$ PD8035 and  $\mu$ PD8048, as well as the forthcoming  $\mu$ PD8748, are single component NMOS microcomputers fully compatible with the industry standard 8035/8048/8748. Operating from a single 5-V supply, they have a 2.5- $\mu$ s cycle time, single-level interrupt, 96 1- or 2-byte instructions, and 8-level stack.

The  $\mu$ PD8048 contains 1024 x 8 bits of program ROM, 64 x 8 bits of data RAM, 27 I/O lines, 8-bit interval timer/event counter, and oscillator and clock circuitry. The -8748 differs in the use of a 1k x 8-bit EPROM, while the -8035 is scheduled for applications using external program memory. NEC Microcomputers, Inc, 173 Worcester St, Wellesley, MA 02181 has manufactured the 40-pin plastic or ceramic DIPs so that their functional power can be expanded using standard 8080A/8085A peripherals and memory products.

Circle 425 on Inquiry Card

# THE WINCHESTER THAT'S WINNING THE WEST.

Fujitsu design. Western quality. From the world's largest alternative manufacturer of Winchester technology disk drives. Drives that are winning OEMs on reliability, performance, price: The M2251, M2252, and M2253 with 12.5, 25, or 50 megabytes of unformatted storage and flexible program or data loading from external sources such as diskette drives, cartridge drives, storage module drives, tape drives or communications lines.



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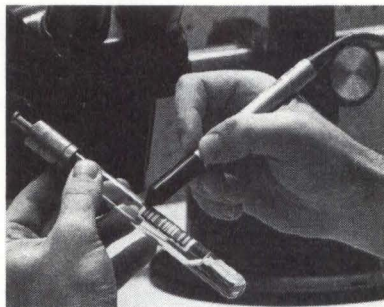
**Northeast** R. H. Sturdy Co., Inc.: **Massachusetts**—167 Worcester Street, Wellesley Hills 02181. Telephone: (617) 235-2330. Charles Sutherland. **Connecticut**—32 Horseshoe Road, Guilford 06427. Telephone: (203) 453-5424. Robert Rosenbaum. **New Jersey**—Hansen Associates, Inc., 215 Brookside Ave., Hohokus 07423. Telephone: (201) 652-7055. Art Hansen. **Pennsylvania**—Hopkins Associates, 26 Summit Grove Ave., Suite 208, Bryn Mawr 19010. Telephone: (215) 527-1127. John Hopkins. **East Central** Dietrich & Assoc. Inc.: **Ohio**—319 Marion Bldg., 1276 W. Third Street, Cleveland 44113. Telephone: (216) 781-1855. Jim Dietrich. **Michigan**—7200 E. Ten Mile Road, Centerline 49015. Telephone: (303) 754-6450. David Walton. **Pennsylvania**—90 Claireton Blvd., Pittsburgh. Telephone: (412) 892-2992. William Dietrich. **Southwest** The Thorson Company: **Texas**—6633 Hillcross, Suite 105, Houston 77081. Telephone: (713) 771-3504. Rex Zenger; 4445 Alpha Road, Dallas 75240. Telephone: (214) 233-5744. Joe Bonick; 300 E. Huntland Drive, Austin 78752. Telephone: (512) 451-7527. Jim Trulove. **West and Hawaii** Bergis Associates, Inc.: **Northern California**—14431 Miranda Court, Los Altos Hills 94022. Telephone: (415) 941-4133. Tony Bergis; Edwards Associates: **Southern California**—Bldg. K 2808, Oregon Court, Torrance 90503. Telephone: (213) 328-9770. Allen J. Edwards.

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## MICRO DATA STACK COMPUTERS AND SYSTEMS

### S-100 Bus Disc Subsystem Stores 10M Bytes of Data In a Single Device

A single-board controller, interconnect cable, and Control Data Corp "Hawk" disc drive that utilizes a 5M-byte fixed disc and 5M-byte removable cartridge for a total of 10M bytes of storage comprise the AM-500 subsystem. The

interrupt driven controller board requires a simple interface to the CPU operating system; it performs complete 512-byte transfers.

Although Alpha Micro, 17881 Sky Park N, Irvine, CA 92714 designed the rackmount device to work with the AMOS operating system, it may be purchased in a standalone cabinet to be used with other operating systems on the S-100 bus. AMOS permits multiple user, multiple tasking, time-sharing, and memory management; up to four drives can be daisy-chained to one controller. Unit price is \$7995. Circle 426 on Inquiry Card

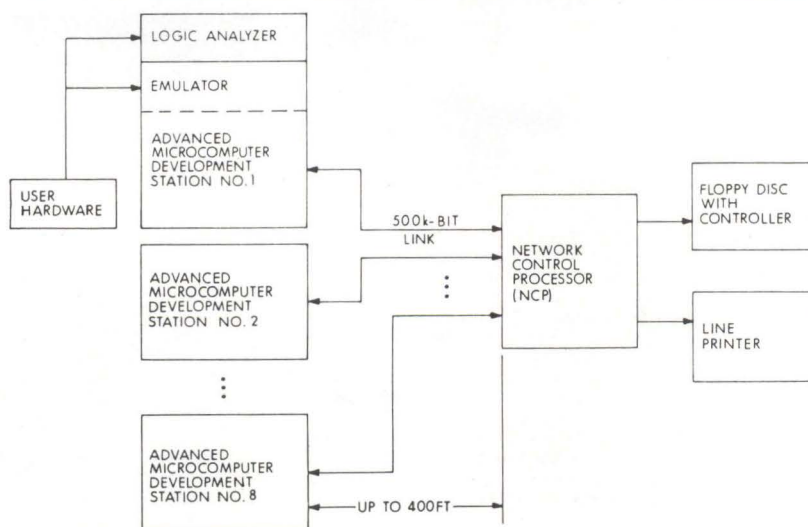
### Development System Network Shares Resources Among Eight Designers

The multistation network of Advanced Microcomputer Development Systems (AMDS) allows disc memory and printer resources to be shared simultaneously with up to eight users, reducing the typical development system cost/station by utilizing these resources fully. Comprising the network are the Network Control Processor (NCP); double-sided, double-density floppy disc unit; medium speed line printer; and up to eight satellite AMDS terminals, which combine CPU, keyboard, and CRT in one enclosure.

Sharing the disc and printer on a "round robin" basis using a disc sharing algorithm and communications protocol, the NCP controls access to

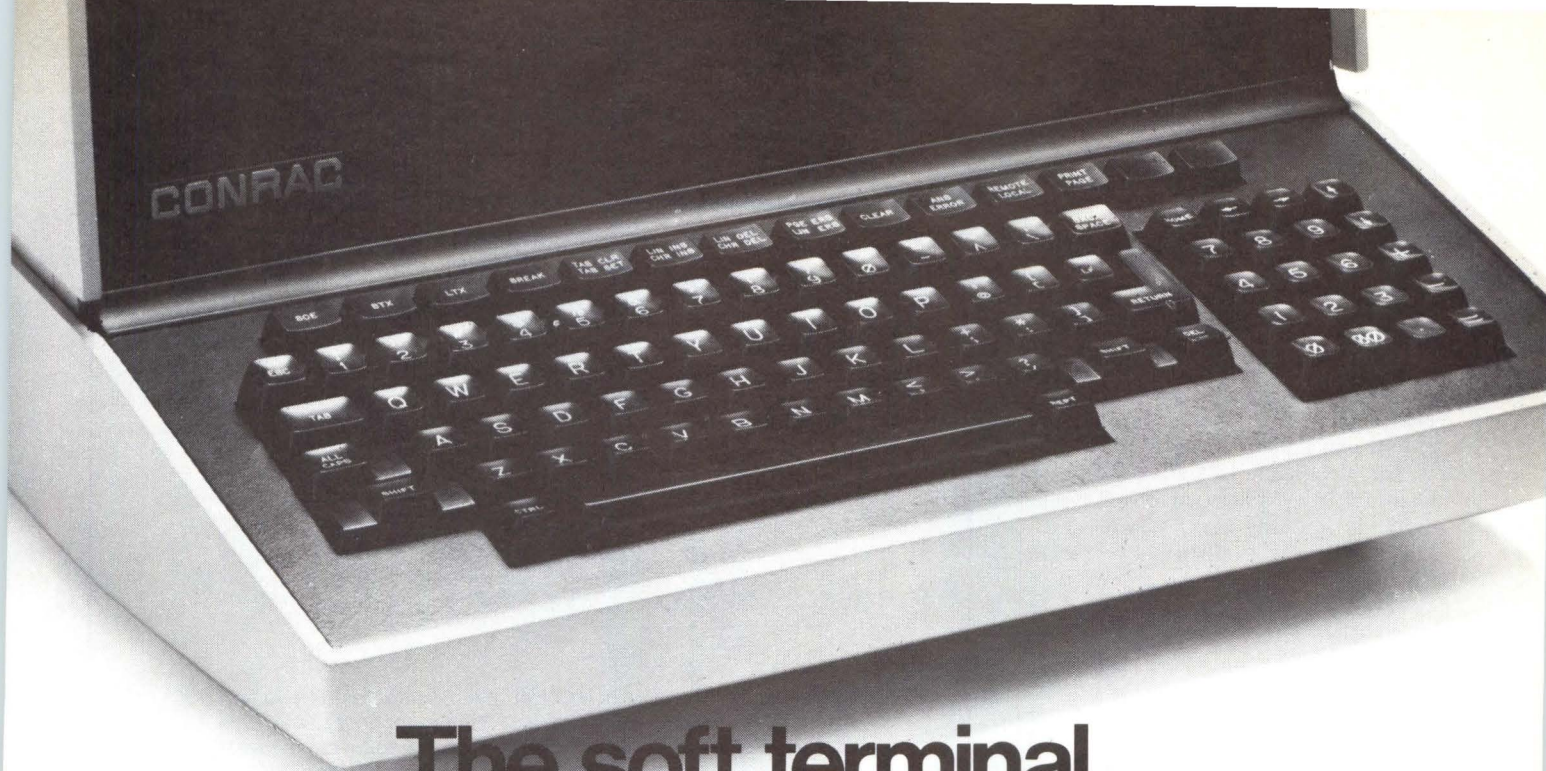
these devices, providing exclusive/shared access to files, freeing files when a satellite station is powered down, and queuing printing requests. In the worst-case condition with all users simultaneously making requests, max wait time for disc access is 9 s.

Futuredata Computer Corp, 11205 S La Cienega Blvd, Los Angeles, CA 90045 has developed the system as a distributed processing network with dedicated CPU and memory in each satellite terminal. Supporting hardware/software development for the 8080, 8085, 8086, 6800, 6802, and Z80, the terminals can be located up to 400 ft (122 m) from the NCP. A high speed serial data link transmits 50k bytes/s over a single twisted pair cable. AMDS terminals are converted for use as an NCP by interchanging two plug-in cards.



Futuredata Computer Corp's distributed processing approach to microcomputer development system network allows up to eight users to work independently. Each satellite station can support a different processor type. Network control processor governs access to disc unit and printer

Circle 427 on Inquiry Card



# The soft terminal. Designed to be redesigned.

Chances are, the intelligent terminal you really need doesn't exist yet.

That's why we build the Conrac 480, The Soft Terminal. It's designed to be redesigned by your software to fit your system like a glove.

### Flexible hardware to start you off.

Most CRT terminals are built around one large circuit board, which doesn't leave you much flexibility.

The Conrac 480, on the other hand, offers you the benefits of a *clean bus architecture*. Plug in four cards, and get a basic working terminal. Plug in up to twelve additional cards, and get some real power. Cards like RAM up to 48K bytes, PROM up to 16K bytes, and interfaces to floppy disk drives, printers and other peripherals.

### Software to make it happen.

Do you need a special keyboard, character set, or set of terminal attributes? No problem. Just plug in a special PROM.

With the proper MPU software, the Conrac 480 can be configured as a polling terminal or as a powerful microcomputer. Or as anything in between. This software can reside in

PROM, or can be downloaded into RAM from a host computer or from disk.

Many software modules are available off-the-shelf, like a basic editing package, and protocol handlers for IBM, Burroughs, and Univac. More are on the way.

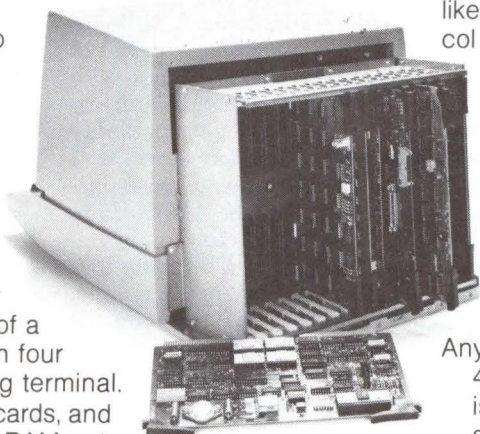
To make microprogramming easy, you can use the AMI 6800 Microcomputer Development Center software, which runs perfectly on our terminal. That's power!

### Attractive outside as well as inside.

Any way you look at it, the Conrac 480 is attractive. The basic version is only 20" deep and fits where space is limited. Its understated modern styling blends into virtually any decor. And you can have your own color and texture.

Operators love the feel of our long-life capacitive keyboard with sculptured keys. And our sharp and stable CRT display. As a matter of fact, we're known worldwide as *the* manufacturer of professional video monitors.

Write to us or give us a call for more facts. We'll send you a comprehensive 12-page brochure on The Soft Terminal. And we promise not to use "hard sell."



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Telephone (213) 966-3511, Telex 670437

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Telephone (07934) 675, Telex 74250

CIRCLE 67 ON INQUIRY CARD

## Controller/Formatter Interfaces Multibus to Hard Disc Drives

HDC1880 is a single-board bipolar microprocessor controlled formatter/controller that connects microcomputers using Intel's Multibus to front or top loading disc drives such as Diablo 44B, Wangco, or other similar units. It features DMA, 20-bit Multibus addressing, built-in soft error recovery, and 5-V only operation.

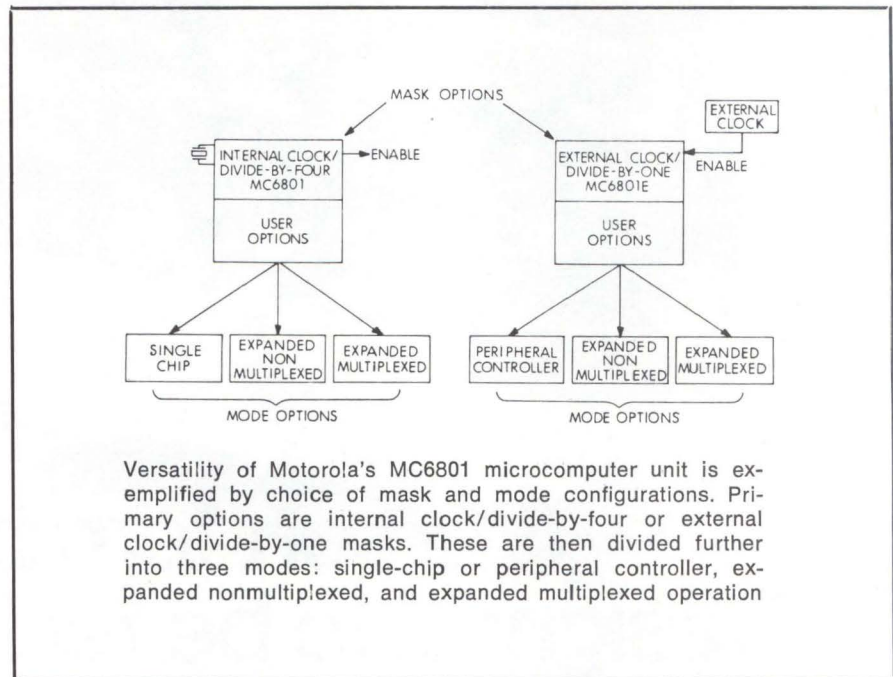
Four drives can be controlled by one device. Each drive has one fixed and one removable 5440 type cartridge pack to provide 40M bytes of online storage. Firmware that Interphase Corp, 200 E Spring Valley Rd, Richardson, TX 75081 supplies on-board can be custom coded to interface to other discs or CPUs, or to allow the CPU to independently perform time-consuming system level functions.

Circle 428 on Inquiry Card

## Enhanced Single-Chip Microcomputer Gives High Level Performance

Inherent in the design of the mc6801 microcomputer unit is flexibility, due to the presence of an onboard serial communications interface, ROM, and RAM, and to the chip's ability to operate with either an internal or external clock, each having a choice of three mode options. In single-chip mode, all four ports (three 8-bit and one 5-bit) are configured as parallel I/O; the comparable peripheral controller mode configures all ports as parallel I/O except for port 3 which becomes a peripheral data bus for interface to a master microprocessor unit. Expanded, nonmultiplexed mode allows direct interface to M6800 peripherals, but limits the address to 256 bytes. Expanded multiplexed mode provides the full 64k bytes of address when used with a standard multiplex latch.

Introducing prototype quantities of the single-chip unit, Motorola Semiconductor Products, Inc's Integrated Circuit Div, 3501 Ed Bluestein Blvd, Austin, TX 78721 is aiming it at low cost, high performance systems. The 31 TTL compatible, parallel I/O lines allow the configuration to be tailored to specific needs or criteria, serving as a cost-effective instrument and tool for design and instrumentation efforts.



Versatility of Motorola's MC6801 microcomputer unit is exemplified by choice of mask and mode configurations. Primary options are internal clock/divide-by-four or external clock/divide-by-one masks. These are then divided further into three modes: single-chip or peripheral controller, expanded nonmultiplexed, and expanded multiplexed operation

An enhanced mc6800 CPU with an increased instruction set is expandable to 64k words of address. Other features include a 16-bit timer, 2k bytes of mask programmable ROM, 128 bytes of RAM, an internal clock with a divide-by-four circuit, interrupt capability, and object code compatibility with the M6800 instruction set. It is compatible with hardware and software components of the M6800 family, and interfaces directly with TTL and MOS peripherals. The NMOS device requires only a 5-V power supply.

mc6801L1, the first offering, is programmed with a general purpose routine called LIL-BUG™ for use in prototyping systems for evaluation; it

is used in the mc6801EVM Microcomputer Evaluation Module. An mc6801E version will also be offered. This mask option uses an external clock for slaving in a multiprocessor system in which the host is any M6800 family processor; the microcomputer acts as an intelligent peripheral interface without sacrificing computing power.

The 40-pin ceramic DIP mc6801 costs \$35 each (minimum of 250). mc6801L1 is priced at \$49.95 (unit quantity). An EPROM version mc68701, to be available first quarter of 1979, is tentatively priced at \$95 in unit quantities.

Circle 429 on Inquiry Card

## Timeshare System Based On Single-Board Computer Reduces Maintenance Cost

The functions of the CPU, 65k bytes of RAM, DMA, realtime clock, programmable interrupt controller, floppy disc controller, and three RS-232 interfaces with programmable synchronous and asynchronous baud rates are placed on a single 9.5 x 13.5" (24.1 x 34.3-cm) PC board. Micro V Corp, 17777 SE Main St, Irvine, CA 92714 houses this board with two double-sided 8" (20-cm) floppy disc drives and a power supply in a tabletop 8 x 17.5 x

24" (20 x 44.5 x 61-cm) console, labeled the MicroStar™ model 45.

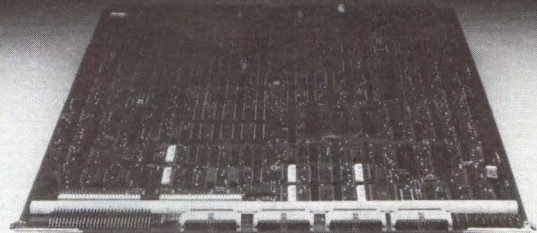
The RETMA rack mountable unit features an optional system configuration integrating a video display and detachable typewriter keyboard with 10-key pad. The timeshare, small business computer features the UPDATE™ database management system to ease custom programming. The user can define a dictionary of words that is used to facilitate report generation. Also supported are the STARDOS™ multiuser timesharing system and CP/M™ disc operating system.

Circle 430 on Inquiry Card

# MSC Makes The Best Controller You'll Ever See.



# Or Won't.



On the left, the cabinet model of our 1000 Series disk-based controller. On the right, our host resident version of the same series. But left or right, a lot of folks for a lot of reasons think of the 1000 Series as "the consummate controller."

It's simply got so much more going for it.

## **More Functional. More Versatile. More Reliable. More Maintainable.**

In short, the 1000 Series by MSC is a more sensible controller buy. Because that's the way we designed it.

*Powerful.* So that users can access up to 1200 megabytes of on-line storage at data transfer rates of up to 1.2 megabytes/sec.

*Flexible.* So that users aren't locked into one manufacturer's drive or one particular drive technology. The MSC 1000 Series accommodates both removable and Winchester fixed media — in Ampex, Memorex, CalComp, CDC, ISS, Microdata, Okidata, Kennedy and Fujitsu drives.

*Modular. Simple. Smart.* So that users can easily upgrade the 1000 Series in the field. And so that maintenance and downtime will be negligible anyway. Thanks to the single board construction, low parts count, on-board microdiagnostics, all quality components and low stress design that account for a phenomenal MTBF.

## **More Features Up Front. More Experience Behind It.**

The MSC 1000 Series boasts a history of proven performance in a wide range of minicomputer operating systems. As a single, host resident board in the Nova and Eclipse,

as well as with Interdata. And as a separate cabinet in the HP3000 and 21MX. IBM Series/1. PDP-11. Microdata 1600.

In the four years that MSC's 1000 Series has been at work in the field, the installed base has grown to over 2000 units. So that when we talk reliability, maintainability, power and performance, it's more than just talk.

And when we talk operational features like error correction, sophisticated channel techniques, automatic self-test, overlap seek capability and logical to physical drive correlation, we are talking about a *commitment to incorporating innovation in all of its scope and each of its details into every product we design and manufacture.*

The MSC 1000 Series disk-based controller is a measure of that commitment.

Call us for more information. **MSC. Microcomputer Systems Corporation.** 432 Lakeside Drive, Sunnyvale, California 94086. (408) 733-4200. TWX 910-339-9359.

**One  
More Miracle  
From Microcomputer  
Systems Corporation.**

The   
**MSC 1000  
Series.**

**SOFTWARE**

**Added Utilities Enhance User Oriented Multidisc Operating System**

Version 2.05 of IMDOS, the IMSAI multidisc operating system, contains over 20 utilities such as an 8080/8085 assembler, peripheral interchange program, dynamic debugging tool, disc and memory diagnostic program, and data management facilities. Enhancements added by IMSAI Manufacturing Corp, 14860 Wicks Blvd, San Leandro, CA 94577 include a video/context editor with video cursor editing, character pointer position, and contextual string/matching editing; support of 17 floppy disc formats, such as various sector sizes, single- and double-density, and standard and double track; and formats for 35-, 40-, and 77-track mini-floppies. The system supports hardware compatible with IBM formats for double density.

Customized drivers can be added, since the system includes the source for user modification of i/o drivers. The GENESYS utility contains a built-in linking loader that handles any changed length of the i/o driver. A cold-start command provided by the utility allows the user to specify any valid system command during system generation.

Sequential and random access modes are provided. A program file load command supports program overlays and chaining. Compatible with CP/M™, the user oriented system concurrently supports multiple disc interfaces online. Scientific BASIC-E is supplied with the operating system.  
Circle 431 on Inquiry Card

**Features of Disc Operating System Upgrade Performance**

MZOS, a disc operating system for the Z80 and Micropolis disc drives (up to four drives) featuring compatibility with North Star dos software, is designed to support the company's MZ computer system or a similar configuration. System performance is improved with such features as implied execution which permits a file to be executed by typing the name, listing

of the directory in two formats, and drive recalibration each time the directory is listed.

Other features incorporated by Vector Graphics Inc, 31364 Via Colinas, Westlake Village, CA 91361 include a set of error messages, file protection against deletion, and a special method of writing data on the disc. Specific identification is associated with each sector, eliminating the possibility of unknown seek errors. Added commands allow verification of sectors of files and renaming of files.  
Circle 432 on Inquiry Card

**Multuser BASIC Has COBOL File Handling for Microcomputers**

PANA/BASIC is a multiuser operating system, extended BASIC language processor, and comprehensive file management system for use on Intel 8080, 8085, and Zilog Z80 microprocessor systems. Most of the functional capabilities specified in Level 2 of the 1974 ANSI COBOL have been included by Panatec Inc, 1527 Orangewood Ave, Orange, CA 92668.

The timeshared, multiterminal operating system features quick response time in multiterminal environments. Queued i/o permits overlap of computation and i/o operations while a background processor is provided so that long running programs can be run in the background freeing terminals for independent data entry or inquiry.

File organizations include sequential, relative (direct), and indexed sequential; access modes include sequential, relative, indexed, and consecutive. Dynamic access allows one or more users to access the same file in more than one access mode. The system handles multiple user access, automatically protecting files during update.

Four data formats are decimal, extended precision decimal, binary integer, and string. Normal internal accuracy is nine decimal digits; in extended precision decimal format, it is up to 15 digits.

String handling capabilities suit the language to text editing, word processing, and data formatting. Both substring reference and string arrays are included. COBOL style format editing and string match facilitate report writing and screen formatting.

Further capabilities of the software are interactive data entry and control, external subroutine capability, inter-task communications, and various system utilities. The system is available on a nonexclusive permanent license basis. □

Circle 433 on Inquiry Card

**Micro computer size**

**Macro data capacity**

Raymond's Model 6409 Mini-Raycorder packs 128K bytes of storage and the performance of much larger systems into micro-sized hardware. Yet, it has all the reliability which you have come to expect from Raymond, The Small Tape Drive Experts.

For complete information, contact:

Raycorder Products Division  
**Raymond Engineering Inc.**  
217 Smith Street, Middletown, Connecticut 06457 (203) 632-1000  
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## Is the real cost of your next disk controller being buried?

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## EXTERNAL ARITHMETIC PROCESSORS

**Scott Smith**

Integrated Computer Systems, Inc  
Santa Monica, California

Since their introduction, microprocessors have found widespread acceptance as control "black boxes" to route data and command signals. On the other hand, the microprocessor's lack of fast computational power has been responsible for its failure to penetrate markets requiring such capabilities for use in complex numerical processing. These markets have therefore resorted largely to older arrangements such as minicomputers with custom arithmetic processors added, or expensive hardware logic processors implemented in medium-scale integrated (MSI) logic, bipolar bit-slice processors, or even analog systems. However, even these solutions are faced with constraints involving expense, bulkiness, and power consumption.

In response to this situation, semiconductor manufacturers are handling a wide range of arithmetic processor

needs by introducing very-large-scale integrated (VLSI) chips that interface easily with microprocessors. Thus, the control capabilities of the microprocessor are combined with an external chip having powerful arithmetic capabilities, resulting in computational tools that rival complex minicomputers at a fraction of the cost. Examination of the VLSI arithmetic processors being produced reveals a hierarchy of strategies that are being used by the semiconductor vendors in their efforts to provide arithmetic processing at low cost.

### Need for Arithmetic Processors

Arithmetic processing is required for all kinds of signal processing applications. These applications include, but are not limited to, graphics, filtering, data reduction,

**Typical Multiplier Chip Performance**

Manufacturer	Model No.	Word Size	Speed (ns)	Power (W)	Comments
TRW	MPY-8HJ	8	65	1.0	Multiplier
TRW	MPY-12HJ	12	80	2.0	Multiplier
TRW	MPY-16HJ	16	100	3.0	Multiplier
TRW	MPY-24HJ	24	200	3.5	Multiplier
Monolithic Memories	57558	8	100	0.9	Multiplier
AMD	25S05	2 x 4	40	0.9	Multiplier
TRW	TDC1003J	12	175	2.5	Multiplier-Accumulator
TRW	TDC1008J	8	70	1.2	Multiplier-Accumulator
TRW	TDC1009J	12	95	2.5	Multiplier-Accumulator
TRW	TDC1010J	16	115	3.5	Multiplier-Accumulator

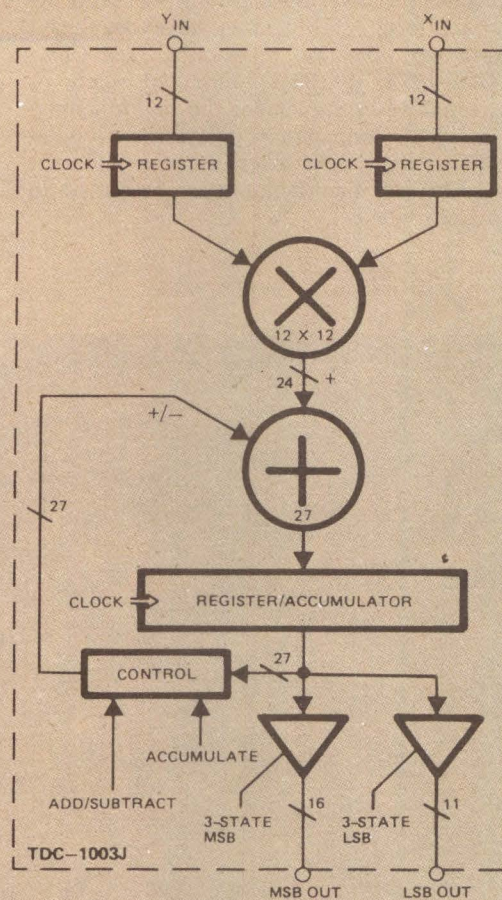
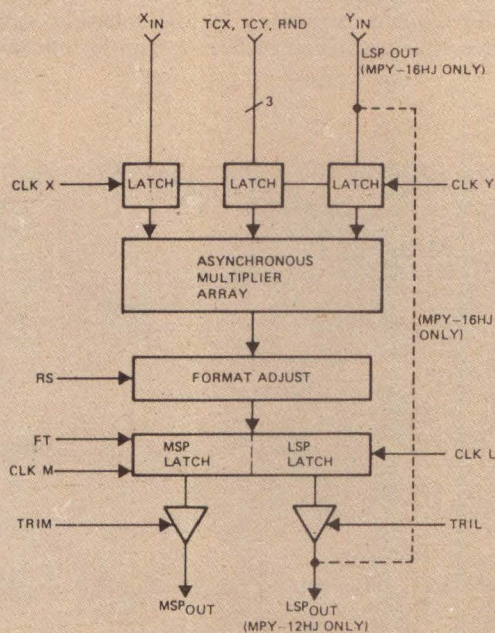


Fig 1 Logic for multiplier and multiplier-accumulator chips. Multiplier generates products as rapidly as possible, whereas multiplier-accumulator chip accumulates sums of products. Both chips input integers into multiplier stage and output product through 3-state buffers. Provision is made for multiplexing product on output bus if desired. In multiplier, FT can cause product to bypass output latch to achieve more speed. In multiplier-accumulator chip, running sum of products held in register/accumulator may be added or subtracted to last product from multiplier (Courtesy of TRW LSI Products)

radar, speech synthesis, and other forms of analog synthesis. When these applications are carried out in real time, the computational loads increase enormously. Maximizing the data throughput rate becomes the single most important requirement and has several effects on design.

Hardwired logic processors are implemented in fast semiconductor technologies, usually Schottky TTL or ECL. As many operations as are economically possible are performed in parallel and systems are virtually custom designed to eliminate (or at least minimize) any nonarithmetic movement of data.

Since minimum word size is usually 12 bits and floating point numbers are typically 32 bits, large numbers of logic elements must be interconnected in very complex configurations to handle the data volume. This complexity, combined with the speed requirements of the devices, causes a heat dissipation problem when the circuit is reduced to fit on a single semiconductor chip. Consequently, some arithmetic chips require special cooling or must be fabricated in packages that include heat sinks.

## Design Approaches

Since the design of the processing section must be optimized, available chips vary widely in their approach. These approaches range from the fast specific multiplier-accumulator chips for which the user must provide the control circuitry to the general and somewhat slower firmware processors such as the Advanced Micro Devices (AMD) 9511 (see *Computer Design*, Aug 1978, p 176). Another strategy is to draw on both of these approaches and mount all necessary arithmetic elements and control circuits along with a firmware memory on one chip. The user then optimizes the arithmetic performance of the chip for his application by specifying the firmware. This approach is used by American Microsystems Inc (AMI) in the S2811 signal processing peripheral chip.

*Beginning with Basics—User-Built Peripherals*—Most computation in signal processing is implemented as addition, subtraction, multiplication, or division. Although microprocessors can handle addition or subtraction, their per-

formance of multiplication and division is lacking. For example, the software to perform a 16-bit addition on the 8080 requires only on the order of tens of microseconds while 16-bit multiplication takes over 1.2 ms. Consequently, several manufacturers, notably TRW, have developed chips that perform multiplication in parallel (see *Computer Design*, Dec 1978, p 162). Composed solely of those logic gates required to implement the multiplication function itself, the chip's propagation delays are dropped to the 100- to 200-ns range. Multipliers come in different word sizes from different manufacturers as indicated in "Multiplier Chip Performance."

Frequently, numerical calculations of the form  $Az + By + Cz + \dots$  are performed. For this purpose the multiplier-accumulator chip is frequently used (see Fig 1). Multiplier chips can be used with floating point numbers as well as fixed point, as is illustrated in Fig 2. *Coming From the Calculator End—Arithmetic Processing Units*—Complex math functions such as trigonometric functions or exponentiation have been performed for some time in MOS calculator chips. These chips are so slow however, that at the present time, complex math is instead being performed in the microprocessor itself. To close this gap, vendors have begun introducing chips with

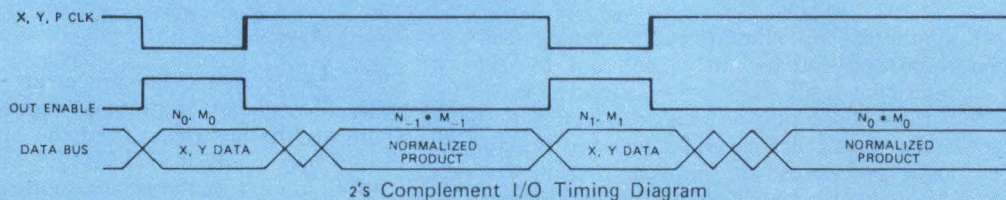
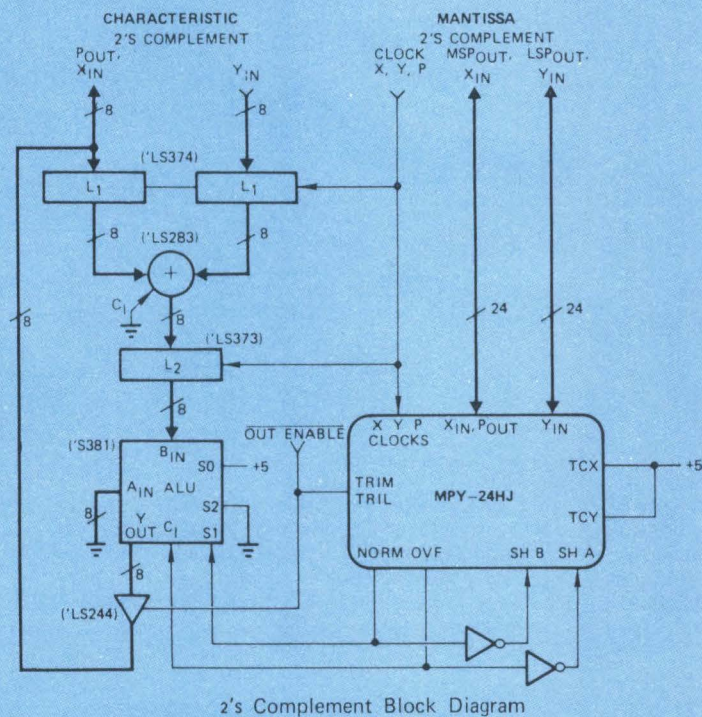


Fig 2 Floating point multiplication using one multiplier. In this circuit, clock X, Y, P causes circuit to operate in two phases. In first phase, source registers  $L_1$  are loaded with two characteristics while multiplier calculates mantissa products. On second clock, output of adder is loaded into  $L_2$ , and its contents (in conjunction with multiplier NORM and OVF outputs calculated in previous clock phase) are processed by ALU to normalize  $P_{OUT}$ . At same time, multiplier outputs results of previous multiplication on  $MSP_{OUT}$  and  $LSP_{OUT}$  lines. In this way, data lines are effectively multiplexed for both input and output, and floating point result is kept normalized at same time (Courtesy of TRW LSI Products)

the necessary speed, most notably AMD with the 9511 arithmetic processing unit. This chip features all "slide rule" functions—add, subtract, multiply, divide, trigonometric functions, inverse trigonometric functions, square roots, logarithms, exponential functions, and floating point/fixed point conversions—and performs them on 16- or 32-bit fixed point numbers or 32-bit floating point numbers.

Data are communicated between the microprocessor and the 9511 via either programmed I/O or direct memory access if a DMA controller is used. Packaged in a 24-pin DIP that requires 12 and 5 V, it can multiply two

16-bit fixed point numbers in 42  $\mu$ s; a high speed Am9511-4 version performs the same multiplication in 21  $\mu$ s. This represents arithmetic processing that is 200 to 400 times faster than implementing the function in software. The function requiring the longest time to execute is the floating point power function which takes up to 3 ms in the fast version.

Programming the unit is accomplished by transmitting command bytes to the arithmetic processing unit. Five bits in the command byte specify 32 different arithmetic calculations, two bits select the data format, and one bit commands the unit to interrupt when it has completed

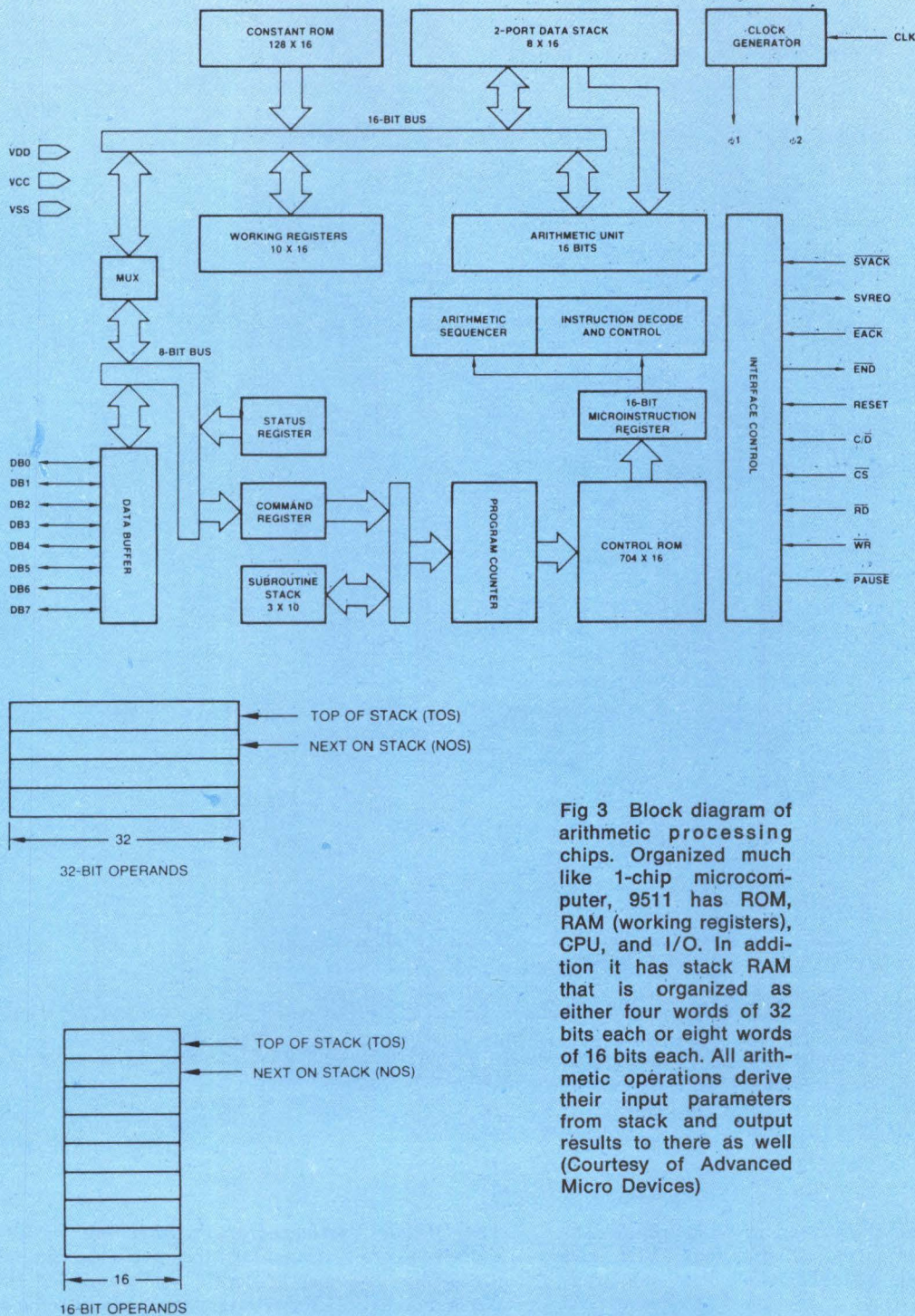


Fig 3 Block diagram of arithmetic processing chips. Organized much like 1-chip microcomputer, 9511 has ROM, RAM (working registers), CPU, and I/O. In addition it has stack RAM that is organized as either four words of 32 bits each or eight words of 16 bits each. All arithmetic operations derive their input parameters from stack and output results to there as well (Courtesy of Advanced Micro Devices)

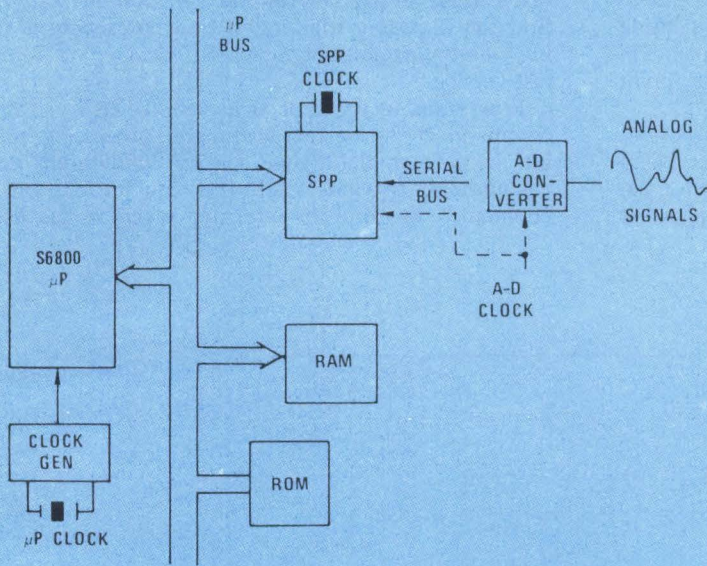


Fig 4 Signal processing peripheral within microcomputer systems. Designed to interface to, but operate independently of, microprocessor, S211 optimizes performance, with its own clock oscillator. Data may be transferred serially or in parallel; here SPP is shown reading serial input from A-D converter (Courtesy of American Microsystems Inc)

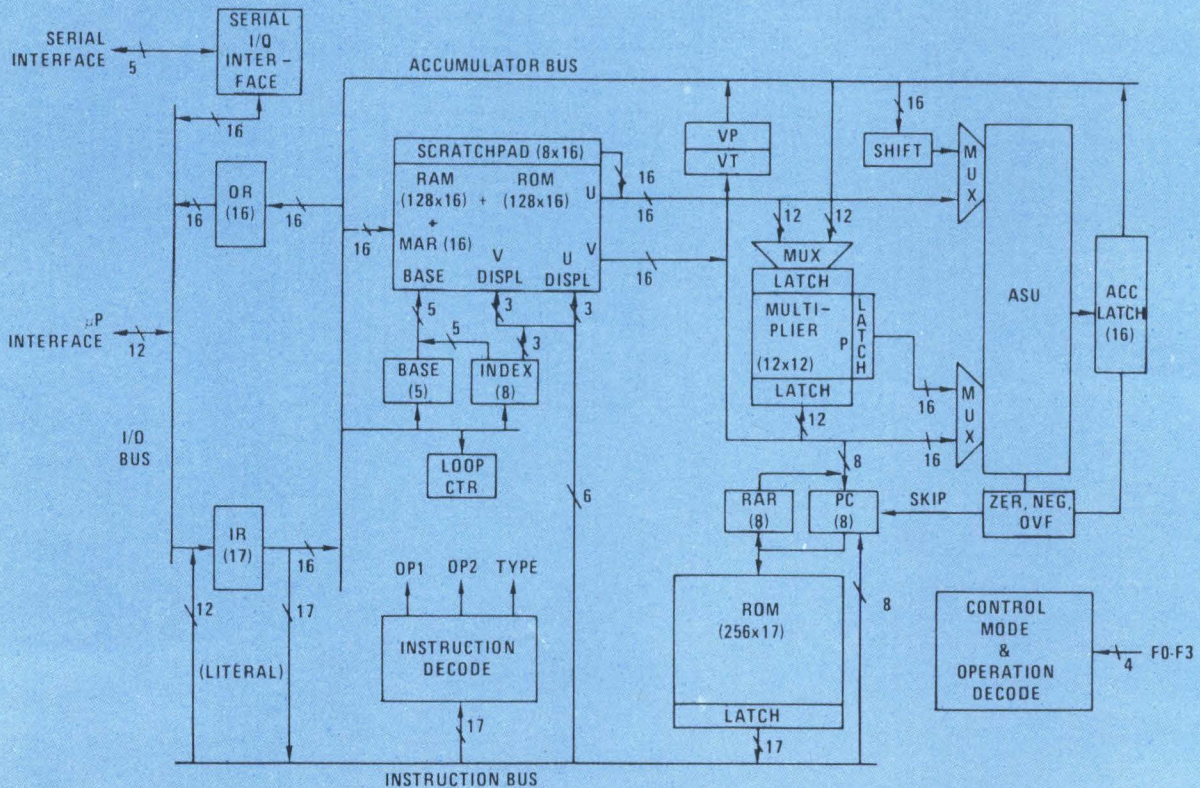


Fig 5 SSP block diagram. Chip contains two arithmetic units: 12-bit multiplier and 16-bit adder/subtractor unit (ASU). OP1 and OP2 signals leaving instruction decode block specify two independent operands to be specified per instruction. Scratchpad memory is composed of both ROM and RAM and may be accessed via indirect and base relative addressing (Courtesy American Microsystems, Inc)

the calculation. Data are transferred in 8-bit "chunks" to a register stack that is organized either as four 32-bit fixed or floating point registers or eight 16-bit fixed point registers (see Fig 3).

*The Middle Method—User-Programming of Arithmetic Processor*—After examining the available digital signal processing strategies in depth, AMI concluded that there was a minimal price/performance threshold to be achieved

in order to realize a fast inexpensive processing peripheral that could quickly perform algorithms such as fast Fourier transforms (FFTs). Previous approaches have relied on bipolar bit-sliced technologies or analog techniques. AMI has produced a chip, called the "S2811 Signal Processing Peripheral," that effectively competes with bipolar and analog approaches. Location of the SPP within a microcomputer system is shown in Fig 4. This chip has the following features:

- (1) High density (32,000 transistors) achieved utilizing V-groove MOS (VMOS).
- (2) Architecture oriented toward custom digital signal processing via an onboard 12-bit parallel multiplier and customer defined algorithms implemented in a 256 x 17-bit firmware ROM.
- (3) Directly compatible with the Motorola 6800, and with others if a few MSI packages are added. Packaged in a 28-pin DIP, it consumes 500 mW and will cost less than \$75. Development aids are available including an ICE, assembler, and a microcomputer development unit.

The block diagram (Fig 5) shows how the SPP is utilized in a microcomputer system. Operation of the unit is dependent, of course, on the application firmware inside the unit. This unit can make use of the 128 x 16-bit RAM and 128 x 16-bit ROM, high speed (300 ns) 12-bit parallel multiplier, four different addressing modes, special registers for indexing, and the multibus structure, which promotes concurrent operations. Indeed, two operands are specified in each microinstruction. A skilled firmware programmer can achieve impressive results with this unit; for example, it has been programmed to perform a 128-point complex FFT in 11 ms. This compares to 20 ms and more for a dedicated minicomputer and approximately 2 ms for a dedicated system that utilizes the fast multiplier chips. AMI feels this performance represents a cost/benefit breakthrough in digital signal processing and is planning further signal processing products that will include EPROM programming, greater multiplier accuracy, larger memory capacity, and faster instruction execution times.

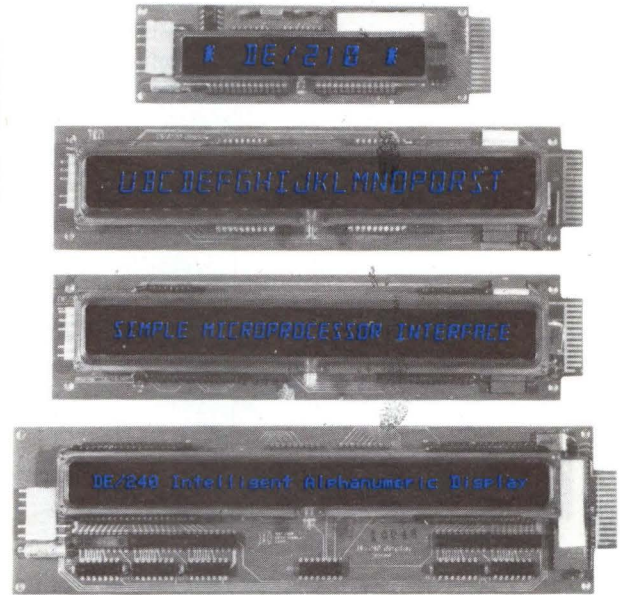
### Summary

Parallel multiplier or multiplier-accumulator chips (such as those produced by TRW) used in a custom circuit will provide the fastest performance, albeit at the cost of designing a circuit containing several MSI and LSI chips. For slower but more versatile mathematical capability at low cost, the 9511 arithmetic processing unit from AMD will perform slide rule functions hundreds of times faster than an equivalent software routine in the microprocessor itself. Finally, the AMI S2811 signal processing peripheral can be optimized through firmware to achieve very high performance at low production cost. These and future chips will revolutionize digital signal processing as much as microprocessors have impacted the low end digital computer market.

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### Bus-Compatible Multiplying DACs Have High Speed Data Latch

Monolithic 8-bit multiplying digital-to-analog converters are able to interface to virtually any microprocessor, whether bipolar or mos. Features

of the 20-pin dual inline Am6080 include an 8-bit input data latch; onchip write, chip select, MSB-select, and data enable logic; and a differ-

ential analog output. The 24-pin Am6081 also contains a status enable and output select as well as a second pair of differential outputs, enabling it to range select at the output, or function as a timeshared DAC or ADC.

Both devices have a minimum data-hold time of 10 ns guaranteed over the entire operating temperature range. Power requirements are  $\pm 5$  to  $\pm 15$  V, allowing use of digital system supply levels. The devices are available in 0.1 and 0.19% accuracy levels over the operating temperature range. Both commercial and military temperature range units are available.

These converters allow a choice of several different coding formats—six formats for the 6080 and eight for the 6081. The most significant bit can be inverted or noninverted under control of the code select input. Code control also provides a zero differential current output for 2's complement coding. A high voltage compliance, complementary current output pair is provided. The data latch is very high speed, making the device capable of interfacing with high speed microprocessors. To the microprocessor, the DAC appears as a memory element.

Monotonic multiplying performance is maintained over a more than 40

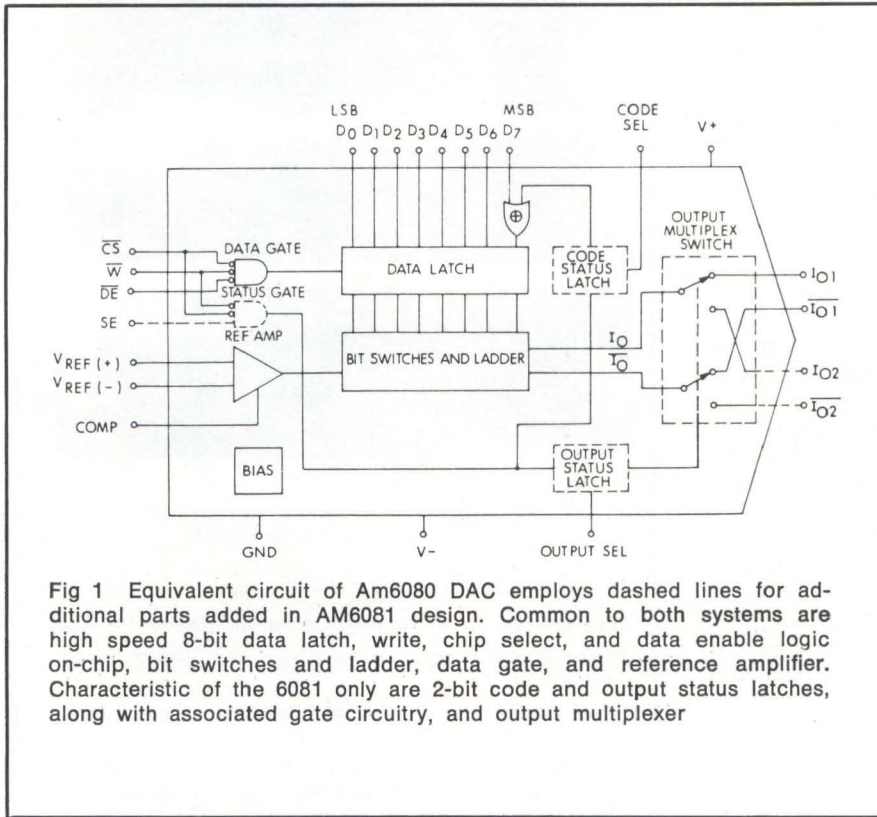


Fig 1 Equivalent circuit of Am6080 DAC employs dashed lines for additional parts added in AM6081 design. Common to both systems are high speed 8-bit data latch, write, chip select, and data enable logic on-chip, bit switches and ladder, data gate, and reference amplifier. Characteristic of the 6081 only are 2-bit code and output status latches, along with associated gate circuitry, and output multiplexer

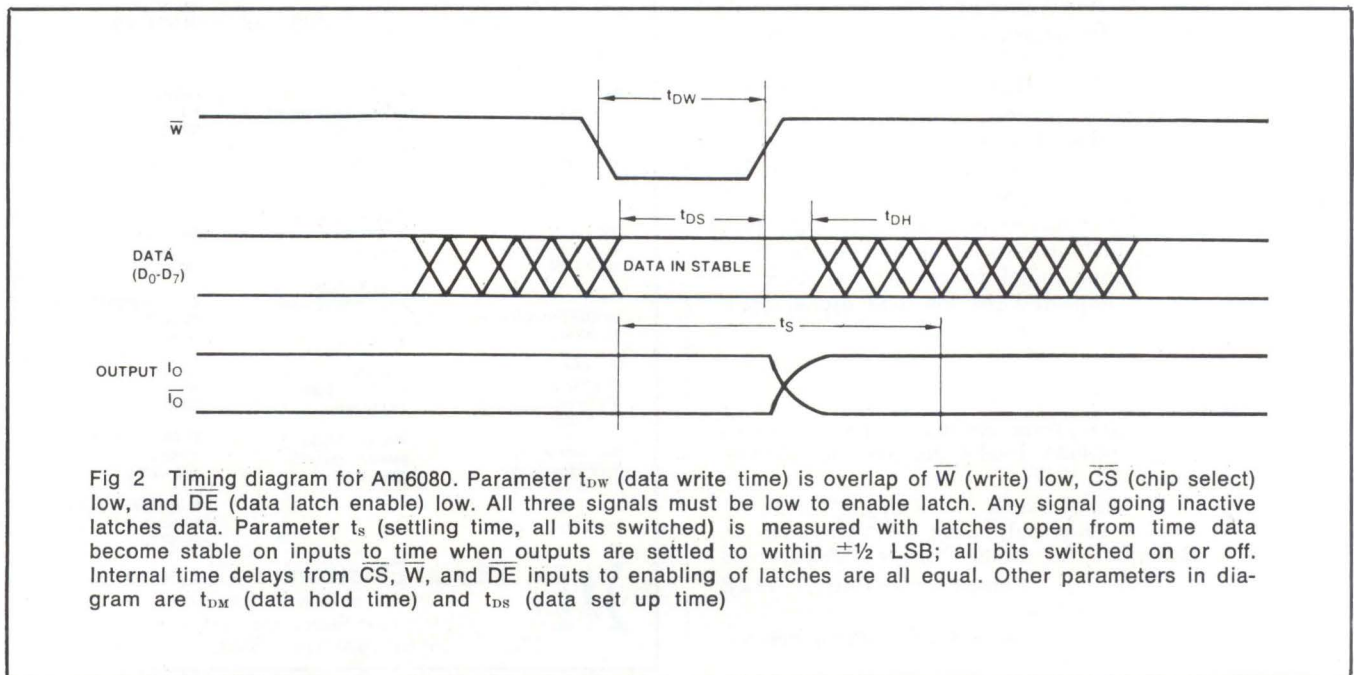
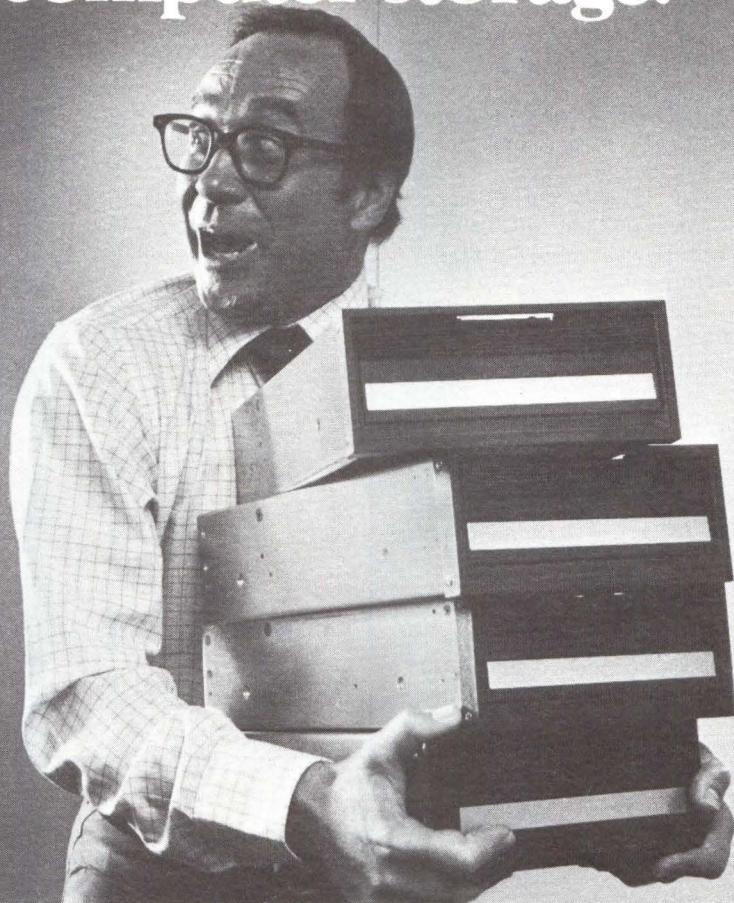


Fig 2 Timing diagram for Am6080. Parameter  $t_{DW}$  (data write time) is overlap of  $\overline{W}$  (write) low,  $\overline{CS}$  (chip select) low, and  $\overline{DE}$  (data latch enable) low. All three signals must be low to enable latch. Any signal going inactive latches data. Parameter  $t_s$  (settling time, all bits switched) is measured with latches open from time data become stable on inputs to time when outputs are settled to within  $\pm 1/2$  LSB; all bits switched on or off. Internal time delays from  $\overline{CS}$ ,  $\overline{W}$ , and  $\overline{DE}$  inputs to enabling of latches are all equal. Other parameters in diagram are  $t_{DM}$  (data hold time) and  $t_{DS}$  (data set up time)



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to 1 reference current range. Matching within  $\pm 1$  LSB between reference and full scale current eliminates the need for full scale trimming in most applications.

The manufacturer, Advanced Micro Devices, Inc (901 Thompson Pl, Sunnyvale, CA 94086) guarantees full 8-bit monotonicity. Device performance is stated to be essentially unchanged over the full power supply voltage and temperature range.

Among other device characteristics are 160-ns settling time for the 6080 (200 ns for the 6081), full scale current prematched to  $\pm 1$  LSB, high output impedance and voltage compliance, full scale current drift of  $\pm 5$  ppm/ $^{\circ}$ C, multiplying capability over a 2-MHz bandwidth, direct interfacing to TTL, CMOS, and NMOS, and a high speed data latch having an 80-ns minimum write time. Absolute maximum ratings are set at the same levels for the two devices. Temperature must remain between 0 and 70  $^{\circ}$ C during operation of commercial version and between -55 and 125  $^{\circ}$ C during operation of military version. Storage temperature is between -65 and 150  $^{\circ}$ C. Other maximum ratings include a  $\pm 18$ -V power supply and logic inputs from -5 to 18 V.

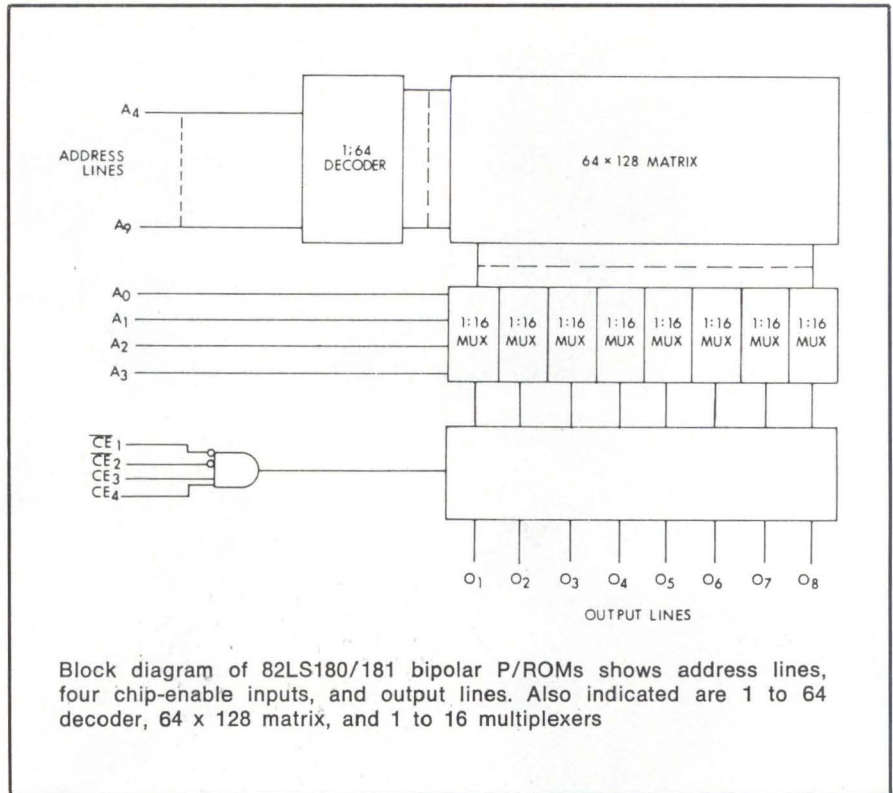
Applications include microprocessor compatible data acquisition systems and data distribution systems, 8-bit ADCs, servomotor and pen drivers, waveform generators, programmable attenuators, analog meter drivers, programmable power supplies, CRT display drivers, and high speed modems.

Circle 350 on Inquiry Card

### Fast P/ROM Features Low Power Operation

Having a typical power dissipation of 37  $\mu$ W/bit and an 80-mA supply current, the 8192-bit bipolar field programmable read-only memory provides an access time no greater than 175 ns. The manufacturer, Signetics, 811 E Arques Ave, Sunnyvale, CA 94086, claims that the highest speed available in a comparable MOS P/ROM is 450 ns.

The N82Ls180/81 uses 60% less power supply current than the earlier 8k-bit P/ROM, the N82S180/181 (which has a 70-ns access time). This reduction in power supply current



provides substantial power savings and higher field reliability through reduced junction temperature.

Devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by the fusing of a Ni-Cr link matrix. There are no separate fusing pins.

The 180 is an open collector model and the 181 has a 3-state output. Other characteristics common to both versions include full TTL compatibility, onchip decoding, and four chip-enable inputs for memory expansion. Absolute maximum ratings limit supply voltage ( $V_{CC}$ ) to 7 V, and I/O voltages to 5.5 V.

Military versions S82Ls180/181 are characterized by a maximum loading current of -150  $\mu$ A (in contrast to -100  $\mu$ A for the com-

mercial version) and by an operating temperature range from -55 to 125  $^{\circ}$ C (in contrast to 0 to 70  $^{\circ}$ C for the commercial version). Commercial parts are available in standard 24-pin plastic or ceramic packages, and the military components conform to mil specs in ceramic.

The combination of low power, fast access, and high reliability makes the chip appropriate for use in MOS microprocessor units, telecommunications, portable instrumentation, automotive engine controls, and military applications. Within these general applications, the component lends itself to both prototyping and volume production for sequential controllers, microprogram storage, hardwired algorithms, control store, random logic, and code conversion.

Circle 351 on Inquiry Card

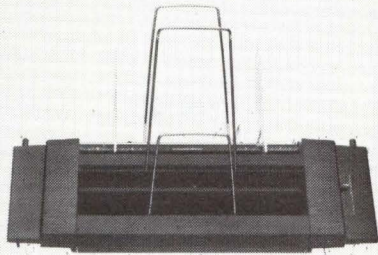
### CMOS A-D Converters Provide Flexible $\mu$ Processor Interface

Based on CMOS technology, a pair of monolithic analog-to-digital converter circuits interface easily to microprocessor systems. Available from National Semiconductor Corp (2900

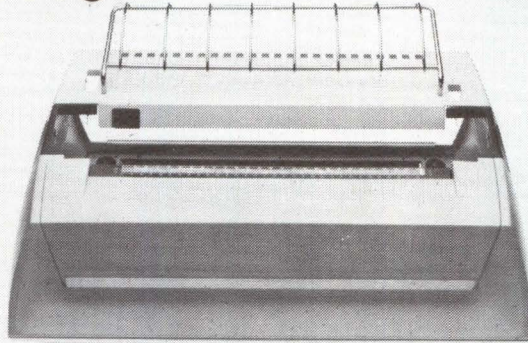
Semiconductor Dr, Santa Clara, CA 95051) in both a  $3\frac{1}{2}$ -digit version, ADC3511, and a  $3\frac{3}{4}$ -digit version, ADC3711, the devices provide addressed, binary coded decimal output for digital systems.

Two CMOS chips similar to these (the ADD3501 and ADD3701) have been offered by the same manufacturer for some time as digital volt-

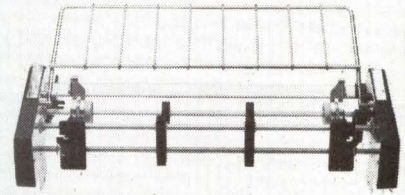
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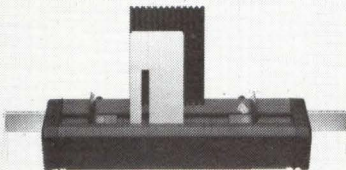
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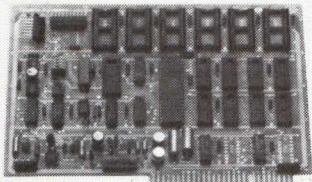
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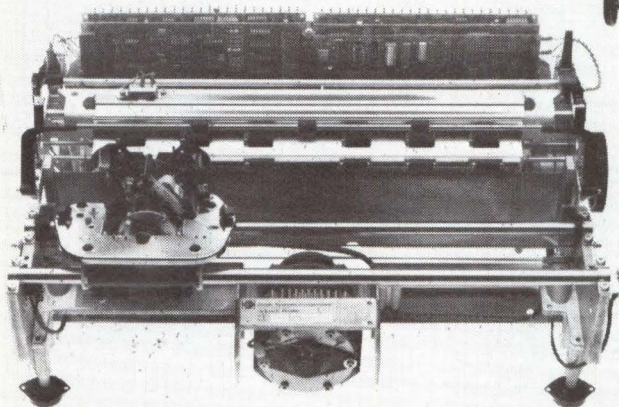
*Mechanical and Auto Front Feeders*



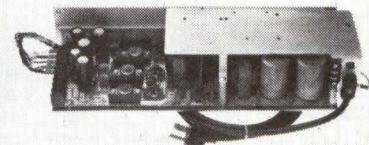
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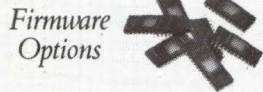
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*1650 Print Mechanism*



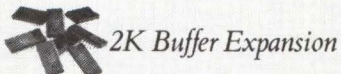
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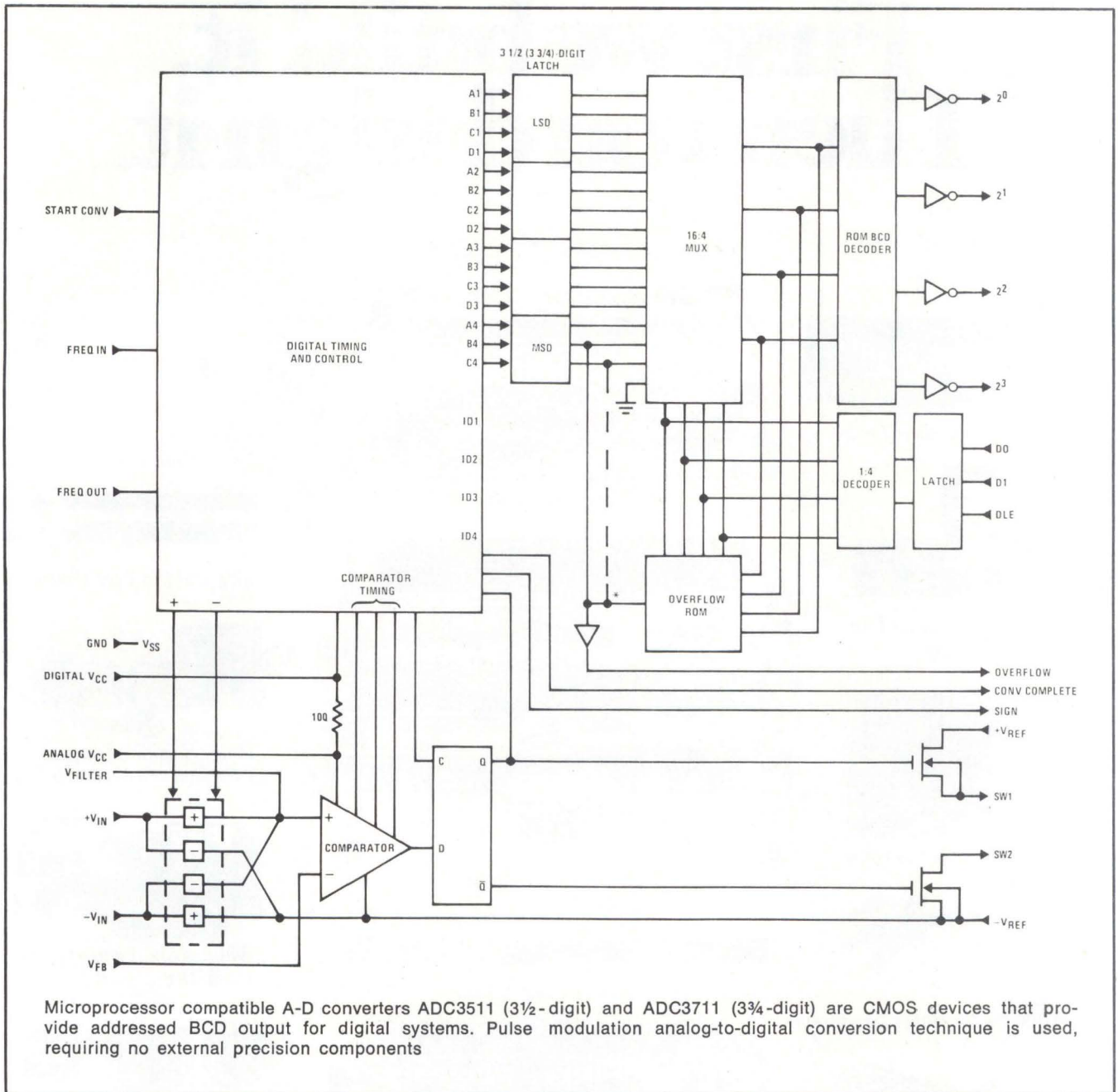
The new Diablo 1650 Series Printers and Terminals are what you make them. Because you have a lot more options with Diablo than you'll find with other manufacturers. So now you can design the exact communications, word processing, or data processing printing system you need, and easily change it as your needs change.

You can select interface options, paper handling options, as well as expanded processing options.

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And you'll see the advantages of having equipment designed by the leading authority in the field. You.

## Diablo Systems



eters. The low cost of these devices led system designers to consider their use as A-D converters in data acquisition systems. However, their internally generated digit scanning rates, meant for driving multiplexed 7-segment displays, made them difficult to interface to digital systems. This led to the design of the present devices with addressed BCD outputs making them suitable for use as ADCs and allowing easy interfacing.

An ADC (of either of these two types) makes the converted value of the input sign available one BCD

digit at a time. The value of the digit selected by the two latching digit select inputs is presented on demand at the device outputs. This "addressed" BCD method of data transfer not only simplifies system interface, but allows these converters to be housed in 24-pin DIPs.

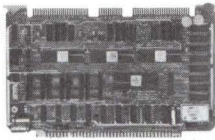
The converters use pulse modulation conversion, an integrating conversion technique, requiring no external precision components, that allows a reference voltage of the same polarity as the input voltage to be employed. Operating from a single

isolated 5-V supply, the microprocessor oriented devices are designed to convert input voltages from -2.00 to 2.00 V. The sign of the input voltage is automatically determined and indicated on the sign output pin. Unipolar input voltages do not require the use of isolated supplies.

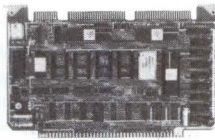
Conversion rates are set by an internal oscillator whose frequency may be determined by an external RC network, or can be driven from an external frequency source. Timing of conversions may be controlled and monitored via the start conver-

# The one word for microcomputer systems: Micromodules.

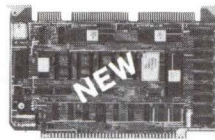
## Monoboard Micro computers



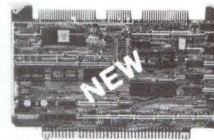
M68MM01



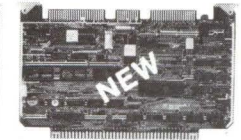
M68MM01A



M68MM01A2

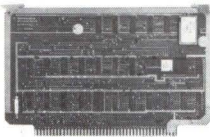


M68MM01B

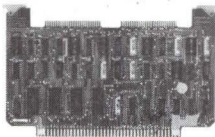


M68MM01B1

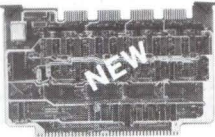
## Modular Microcomputer Subassemblies



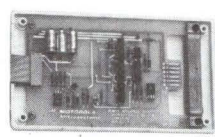
CPU  
M68MM02



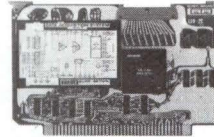
32 Input/Output  
M68MM03



Quad Serial I/O  
M68MM07 Coming 4th Qtr.



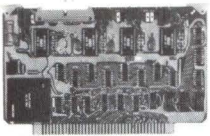
RS-232 to TTY  
M68MM11



8-Channel Input A/D  
M68MM05A



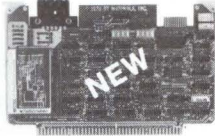
16-Channel Input A/D  
M68MM05B



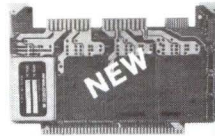
4-Channel Output D/A  
M68MM05C



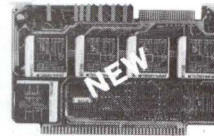
12-Bit 16/32 Channel D/A  
M68MM15A/15A1



16-Bit Low-Level A/D  
M68MM15B



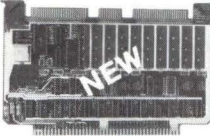
Low-Level Expander  
M68MM15BEX



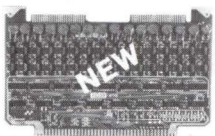
12-Bit Current/Voltage D/A  
M68MM15C



PIA I/O  
MEX6821-2



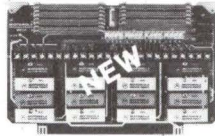
ACIA-SSDA Interface  
MEX6850-2



16/32 Isolated Relay  
Output Channels  
M68MM13A/13B



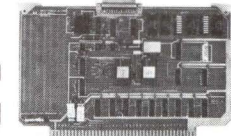
24 Channel Optically Isolated  
Digital Input  
M68MM13C/13D



16 Solid State Relay  
Input/Output  
M68MM23 Coming 4th Qtr.

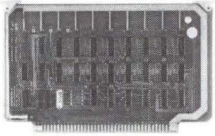


**Program  
Debug**

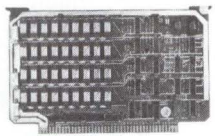


MICRObug for M68MM01/02  
and M68MM01A/02A  
M68MM08/08A

## Memory Modules



8K/16K EROM/ROM  
M68MM04



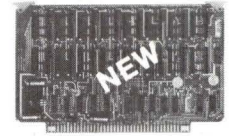
2K Static RAM  
M68MM06



8K/16K Static RAM  
MEX6808/6816-22S



16K/64K Dynamic RAM  
MEX6816/6864



16K/64K Hidden Refresh RAM  
MEX6816/6864-1HR

Micromodules in  
development now

IEEE 488-1975 Functions  
M68MM12/12A  
Hardware Arithmetic Processing  
M68MM14  
MC6809 Monoboard Microcomputer  
M68MM19  
1.5 & 2.0 MHz Versions of  
Selected Micromodules

The broad range of microcomputer system design options open with Motorola's Micromodules has been enlarged to an even greater capability by a host of recent additions to the line.

You get this wide variety of system configurations whether you select the Monoboard Microcomputer approach or choose to mix-and-match with the subassembly modules. Micromodules are fully supported with software, disk operating system, and an accessory line of power supplies, card cages, and chassis.

The five standard Micromodule 1 series Monoboard Microcomputers all are based on either the MC6800 or MC6802 microprocessor. They vary primarily in I/O and memory.

Modular microcomputer subassemblies include the CPU and a selection of I/O, Isolated I/O, A/D and D/A, Memory, and Debug modules. These are supplemented by additional capability in the form of fully-compatible EXORciser\* memory and I/O boards. Family compatibility also permits the simple expansion of any Micromodule microcomputer system, whether it be monoboard or modular.

Contact your Motorola sales office or your authorized Motorola distributor for additional information on Micromodules, the one word for microcomputer systems. We will respond promptly to itemized letterhead requests for data sheets addressed to Motorola Microsystems, P.O. Box 20912, Phoenix, AZ 85036.

\*Trademark of Motorola Inc.



**MOTOROLA**  
Semiconductor Group

sion input and conversion complete output included on both devices.

Additional features of both converters include a medium conversion speed of 200 ms, TTL compatibility, and indication of overflow by means of hexadecimal EEEE output reading as well as an overflow output pin. The ADC3511 converts 0 to  $\pm 1999$  counts and the ADC3711, 0 to  $\pm 3999$  counts.

These chips can be utilized as low cost ADCs or as remote ADCs in the elimination of analog multiplexing. They can also be used to convert analog transducers (temperature, pressure, displacement, etc) to digital transducers.

### Schottky Logic Family Is Fast At Low Power

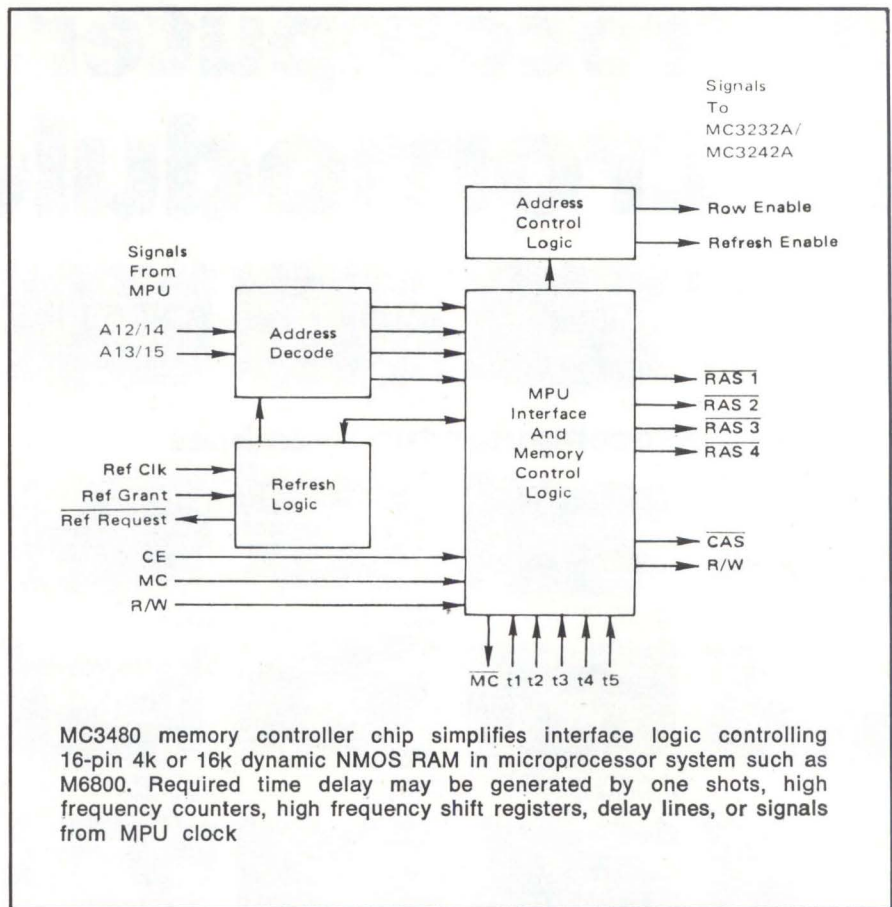
A digital logic family developed by Fairchild Camera and Instrument Corp, Integrated Circuits Group, 464 Ellis St, Mountain View, CA 94042 utilizes isoplanar Schottky logic to achieve 3-ns typical gate delays and 4-mW/gate typical power consumption. The manufacturer has named the product line "FAST" (Fairchild Advanced Schottky TTL), and states that power consumption for a device of this family is approximately 25% that of conventional Schottky devices.

These devices are functionally equivalent to current 5400/7400 device types and are designated as 54Fxxx or 74Fxxx parts. I/O characteristics are compatible with current 5400/7400 Schottky devices. Pricing will be competitive with standard Schottky circuits.

Circle 352 on Inquiry Card

### LSI System Offers Memory Control In Compact Design

A 2-chip system, including a dynamic memory controller (MC3480) and an address multiplexer/refresh counter (MC3242A), provides complete control for up to 64k bytes of memory, including row address, column address, read/write selection, and refresh. The Schottky TTL device is designed to simplify interface logic between a microprocessor and 16-pin 4k or 16k dynamic NMOS RAMS and, on command from the



processor, will generate the timing signals required for data transfer in and out of memory. In conjunction with an oscillator, it will also generate signals to insure that the dynamic memories are refreshed for the retention of data.

Features of the 3480 memory controller include high input impedance for minimum loading of the microprocessor bus and the use of a chip enable for expansion to larger word capacities. It provides a reduction of 30% in package count and system access/cycle times.

The 3242A multiplexes 14 system address bits to the seven address pins

of the memory device. Its 7-bit refresh counter is clocked externally to generate the 128 sequential addresses required for refresh. It is a second source to the Intel 3242, but the detect zero function at pin 15 is replaced by an additional chip enable feature.

A significant reduction occurs in the component count required for the control of random-access memory in MPU/MCU systems, through use of this 2-chip system. The manufacturer is Motorola Semiconductor Products, Inc, PO Box 20912, Phoenix, AZ 85036.

Circle 353 on Inquiry Card

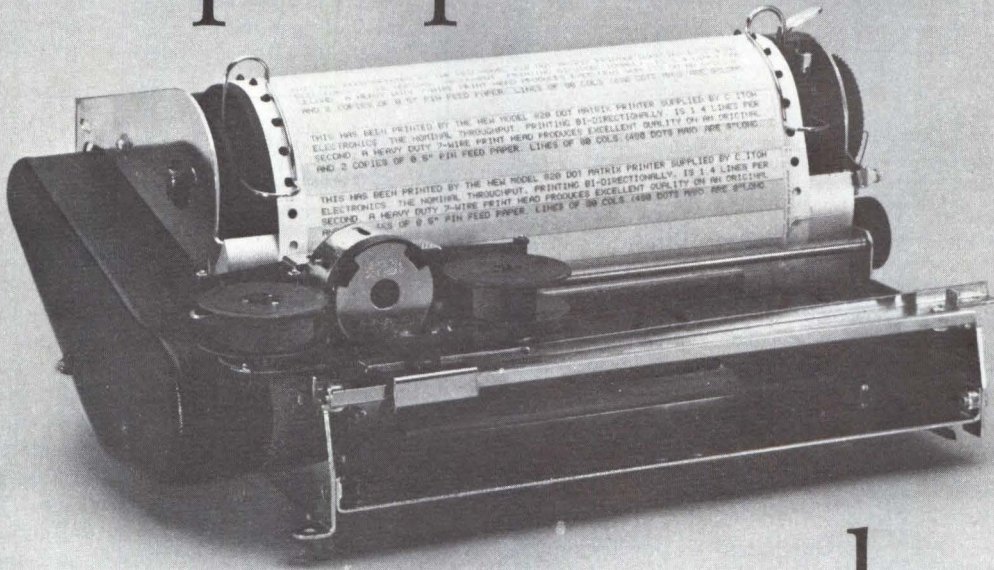
### Precision 12-Bit Binary Current D-A Converter Operates At High Speed

A digital-to-analog converter has a settling time that is typically 60 ns, guaranteed to a maximum of 100 ns, with  $\pm 0.01\%$  precision. The device features TTL/DTL compatible inputs,

externally trimmable gain and offset, and pin programmable current output ranges of 4 and  $\pm 2$  mA. Internal thin film resistors are provided for maximum accuracy and stability in utilization of external op amps.

Performance is guaranteed over the full military temperature range from  $-55$  to  $125$  °C, with monoton-

# Model 820, 150 cps, 80-column, dot matrix impact print mechanism...



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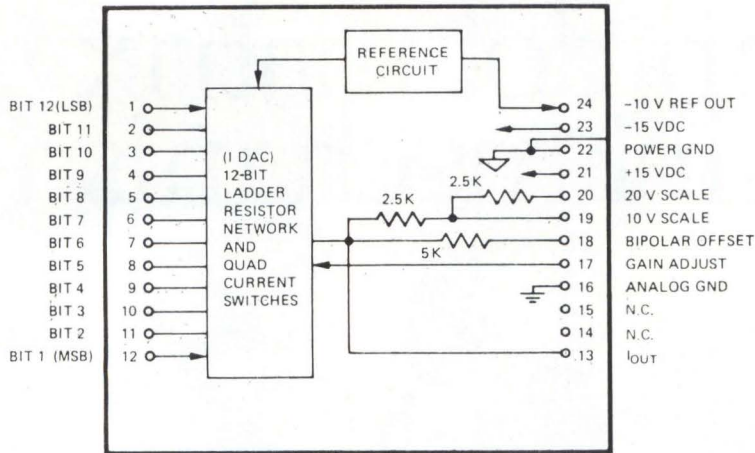
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low cost  
too!

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Features of 12-bit binary current DAC include TTL/DTL compatible inputs and externally programmable current output ranges of 4 and  $\pm 2$  mA. Internal thin film resistors are used with external op amps. Internal reference is capable of supplying 2 mA maximum in addition to current requirements of bipolar offset

carried out with the aid of an external channel pulse control unit.

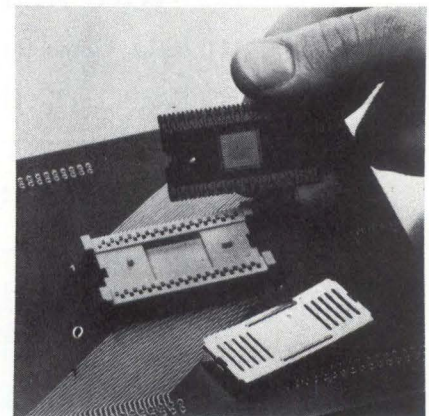
The codec can be used as a multiplex terminal unit in a transmission system. Applications in switching systems include usage as a digital subscriber circuit, a single-stage concentrator (32 through-connected channels), or as a single-stage switching network for private systems and PABXs (also with 32 through-connected channels).

Circle 355 on Inquiry Card

### Quad-Inline Package Houses 64-Lead LSI Chip

A package that uses a leadless 64-position ceramic chip carrier has been developed by the Electronic Products Div of 3M Co, PO Box 33600, St Paul, MN 55133 in conjunction with Intel Corp, to provide a reliable low cost mounting system for a 64-lead LSI chip. The quad-inline package (QUIP) uses approximately 40% less space on a PC board than an equivalent dual-inline package. No insertion force is required to connect the chip carrier and socket, and once connected it is securely supported between spring wiping contacts and a heat dissipating cover.

Installation or replacement is done without special tools, and since the chip carrier package is leadless there is no chance of having to scrap an



Quad-inline package (QUIP) includes leadless 64-position ceramic chip carrier (top), socket (middle), and heat dissipating cover (bottom). Mechanical polarization provides positive protection against improper insertion of chip carrier into socket or incorrect attachment of socket to circuit board. When assembled, chip carrier and socket are securely supported between spring wiping contacts and heat dissipating cover

icity (differential nonlinearity  $\leq \pm 1$  LSB) guaranteed from  $-36$  to  $125^\circ\text{C}$ . Stability over the entire operating temperature range is  $\pm 20$  ppm/ $^\circ\text{C}$  max, full scale, and  $\pm 1$  ppm/ $^\circ\text{C}$  max, zero offset.

The 12-bit DAC, produced by Tele-dyne Philbrick, Allied Dr at Route 128, Dedham, MA 02026, comes in two models, the 4065 and the 4065-83. Both are screened in a method similar to MIL-STD-883, Method 5008, including internal visual, stabilization bake, acceleration, and fine gross leak. The 4065-83 model differs from the 4065 only in being burned-in and temperature cycled.

Only  $\pm 15$ -V power supplies are required for the hermetically sealed, metal cased 24-pin dual-inline devices. Power supply rejection ratio is  $\pm 0.0024\%$  per percentage change in supply voltage, with or without external gain and zero offset circuits.

These devices are considered to be particularly appropriate for uses requiring ultra fast voltage DACs, precision displays, portable instrumentation, and fast A-D conversion. Applications in military environments and with high reliability industrial equipment are emphasized.

Circle 354 on Inquiry Card

### 2-Channel Codec Uses Pulse Code Modulation

A pair of LSI circuits, the sm61A (MOS) and S291 (bipolar), are combined in a 2-channel codec using pulse code modulation. The coding/decoding can be performed at any point in a telephone connection—along the transmission path, at the switching center, or in the telephone terminal.

With the 8-kHz sampling rate recommended by CCITT, a maximum of two 4-kHz voice channels can be

assigned to the codec. Alternatively, coding and decoding of one 8-kHz voice channel is possible, the sampling rate then being 16 kHz.

The A-companding sm61A/S291, produced by Siemens AG, Postfach 103, D-8000 Munich 1, Federal Republic of Germany for overseas applications but not marketed in the U.S., features TTL compatible digital interfaces, independent reading-in and -out of PCM words (in no fixed sequence), and a single-stage arrangement enabling codecs to be interconnected directly. PCM switching is



# ADVANCED TECHNICAL EDUCATION



INTEGRATED COMPUTER SYSTEMS, INC.

## 1979 WINTER SCHEDULE

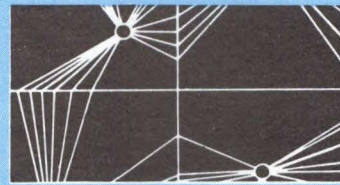
### FIVE-DAY COURSE SERIES MICROPROCESSORS & MICROCOMPUTERS



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January 15-19  
**DENVER**  
January 22-26  
**DALLAS**  
January 29-February 2  
**FT. LAUDERDALE**  
February 5-9  
**WASHINGTON, D.C.**  
February 26-March 2  
**NEW YORK**  
March 12-16  
**PHILADELPHIA**  
April 2-6

Course 350 — Four days

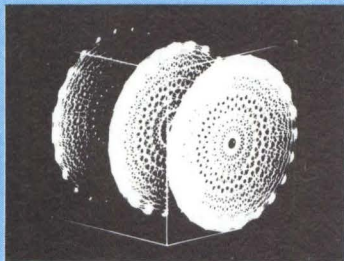
### Distributed Processing and Computer Networks



**ATLANTA**  
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**DALLAS**  
January 30-February 2  
**NEW YORK**  
February 13-16  
**WASHINGTON, D.C.**  
March 6-9  
**PHILADELPHIA**  
March 20-23  
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**BOSTON**  
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Course 365 — Four days

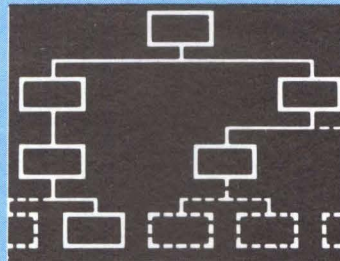
### Computer Graphics



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**LOS ANGELES**  
February 27-March 2  
**DALLAS**  
March 20-23  
**WASHINGTON, D.C.**  
March 27-30  
**DETROIT**  
April 17-20  
**BOSTON**  
April 24-27  
**SAN FRANCISCO**  
May 8-11

Course 320 — Four days

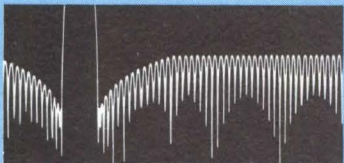
### Structured Programming



**WASHINGTON, D.C.**  
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**BOSTON**  
January 30-February 2  
**NEW YORK**  
February 20-23  
**DALLAS**  
March 6-9  
**LOS ANGELES**  
March 27-30  
**ATLANTA**  
April 17-20  
**DETROIT**  
May 1-4  
**WASHINGTON, D.C.**  
May 15-18

Course 412 — Five days

### Digital Signal Processing



**FT. LAUDERDALE**  
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March 12-16  
**LOS ANGELES**  
March 19-23  
**PHILADELPHIA**  
April 2-6  
**WASHINGTON, D.C.**  
April 23-27  
**BOSTON**  
April 30-May 4

Course 142 — Five days

### Troubleshooting Microprocessor- Based Systems



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March 19-23  
**DALLAS**  
March 26-30  
**BOSTON**  
April 23-27  
**PHILADELPHIA**  
April 30-May 4  
**NEW YORK**  
May 14-18

Course 440 — Four days

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expensive chip because a leg is damaged. Mechanical polarization of the chip carrier and socket provides positive protection against improper insertion of the carrier into the socket or the incorrect attachment of the socket to the circuit board.

QUIP measures 1.1" x 1.89" (2.8 x 4.8 cm) and has a square cavity measuring 0.400" (1.016 cm) on each side. Overall height is 0.350" (0.889 cm). Thermal resistivity of the package and socket assembly is 35 °C/W (nominal) in still air, and 50 °C/W (maximum). Longest lead resistance is 300 mΩ nominal and 500 mΩ maximum. Interlead capacitance (longest lead) is 3 pF nominal and 5 pF maximum. The socket has pins spaced on a standard 0.050" (0.127-cm) grid and 0.100" (0.254-cm) centers, and it provides top access for probe testing. The ZIF burn-in socket is rated at 200 °C.

Circle 356 on Inquiry Card

**Chip Set Is Used To Construct ADC Variations**

A building block approach, involving the use of separate analog and digital processor chips, is used to construct dual-slope-integrating analog-to-digital converters. The analog devices are the TL500C/TL501C, and the digital devices are the TL502C/TL503C—the "C" suffix indicating commercial temperature range. No military versions of the chips are being produced by the manufacturer, Texas Instruments Inc, PO Box 5012, Dallas, TX 75222. In the 2-chip ADC, either of the two analog parts can be used with either of the two digital parts, for four possible configurations, depending on the characteristics required. (Additional versions are also being made available as ADC building blocks, creating further possible 2-chip configurations.)

When used in complementary fashion, these devices form a system that features automatic zero-offset compensation, true differential inputs, high input impedance, and capability for 4½-digit accuracy. Applications include the conversion of analog data from high impedance sensors of pressure, temperature, light, moisture, and position. Analog-to-digital logic conversion provides display and control signals for weight scales, industrial controllers, ther-

момeters, light-level indicators, and many other applications.

The analog processor (whether the 500 or 501 model) contains the necessary analog switches and decoding circuits, reference voltage generator, buffer, integrator, and comparator. These devices may be controlled by the digital processor, by discrete logic, or by a software routine in a microprocessor.

Features provided with the TL500C analog option include a linearity error of 0.001%, 4½-digit readout accuracy with an external precision reference, and 14-bit resolution (when used with the TL502C). Cor-

responding values for the TL501C are a linearity error of 0.01%, a 3½-digit readout accuracy, and 10- to 13-bit resolution (with TL502).

The digital processor includes oscillator, counter, control logic, and digit enable circuits. Seven-segment display drivers with decimal point are provided by the TL502C.

The -503C logic controller has an internal oscillator that can be slaved directly from any TTL source or connected to a 470-pF capacitor to develop an internal clock frequency. Multiplexed 5-digit outputs and four BCD outputs are provided.

Circle 357 on Inquiry Card

**Monolithic 12-Bit D-A Converter Offers Temperature Stability**

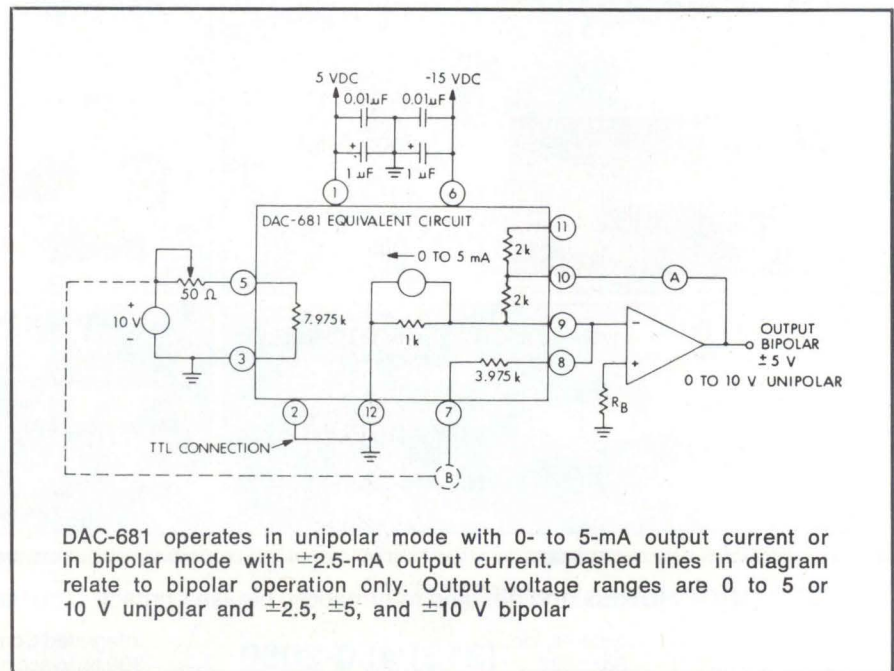
Utilizing a precision, laser-trimmed thin film R-2R ladder network driven by equal-value switched current sources, a monolithic digital-to-analog converter provides a 200-ns settling time, ¼-LSB typical linearity (½ LSB max), with output monotonicity guaranteed over the operating temperature range, and ±5-ppm/°C max gain tempco. Produced by Datel Systems Inc, 1020 Turnpike St, Canton, MA 02021, the bipolar 12-bit DAC operates from TTL or CMOS input logic and provides a 0- to 5-mA unipolar or ±2.5-mA bipolar output current.

The converter contains tracking

feedback and bipolar offsetting resistors to provide five output voltage ranges when used with an external operational amplifier: 0 to 5, 0 to 10, ±2.5, ±5, and ±10 V. These resistors closely track the R-2R ladder with temperature to achieve gain stability.

An external 10-V reference is required, and the device is capable of multiplication over a 2- to 10-V reference range. Pin compatibility with 562-type DACs is featured, and the manufacturer states that the new DACs offer better performance than those earlier devices.

The package is a 24-pin hermetically sealed ceramic DIP. Power requirement is 5 to 15 V and -15 Vdc. Two basic models are the DAC-681C operating over 0 to 70 °C, and DAC-681M operating over -55 to 125 °C.



DAC-681 operates in unipolar mode with 0- to 5-mA output current or in bipolar mode with ±2.5-mA output current. Dashed lines in diagram relate to bipolar operation only. Output voltage ranges are 0 to 5 or 10 V unipolar and ±2.5, ±5, and ±10 V bipolar

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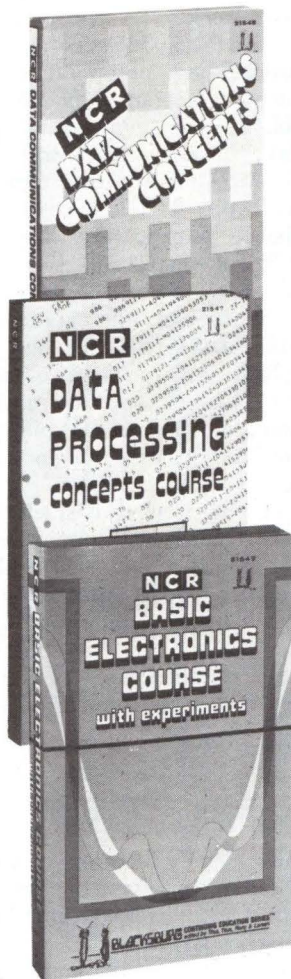
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## FET Op Amps Provide Ultra-Low Levels For Input Bias Current

Input offset voltage, offset voltage drift, input bias current, and supply current are extremely low for two families of operational amplifiers produced by Analog Devices (Route 1 Industrial Park, PO Box 280, Norwood, MA 02062). The devices are the AD542 BiFET op amps and the AD545 FET-input op amps.

In the case of the AD542, guaranteed maximum values are input bias current (warmed up) as low as 25 pA, and input offset voltage as low as 0.5 mV. Also, only 1.5 mA are drawn from supplies. The manufacturer claims that these three values fall below those of any other BiFET amplifier.

Another key specification is the very low 1/f noise of 2  $\mu$ V peak-to-peak, from 0.1 to 10 Hz, which permits use with low level signals from high source impedances. An 80-dB minimum common mode rejection ratio assures better than 13-bit linearity. Open loop gain is guaranteed at 110 dB, min. Slew rate is 3 V/ $\mu$ s, and bandwidth is 1 MHz.

## LSI Multipliers Process Large Numbers At High Rates

Monolithic multipliers provide high-speed n by n bit multiplication of 24-, 16-, 12-, and 8-bit numbers. Operation is facilitated by input registers featuring zero data-hold time (clock overlap). All of the multipliers, except the 8-bit device, employ output registers that can be made transparent for asynchronous output. They also provide a programmable selection of output-product formats and can intermix 2's complement numbers with numbers in absolute magnitude in the same operation.

The devices are the MPY/HJ series, produced by TRW LSI Products Div, PO Box 1125, Redondo Beach, CA 90278. They are n-by-n parallel array multipliers with double precision outputs. All the new chips are plug compatible with their first generation counterparts. Inserting one into a socket wired for an "/AJ" device automatically masks out the

Four versions are available. The AD542J, K, and L are specified over the 0 to 70 °C temperature range and the AD542S over the -55 to 125 °C range. All versions are available from stock.

For the AD545, guaranteed maxima after 5 min of operation at an ambient temperature of 25 °C are as follows: offset voltage as low as 0.25 mV; offset voltage drift as low as 3  $\mu$ V/°C; input bias current as low as 1 pA. The low cost electrometer device also features low power, at 1.5 mA, max, and low noise, at 3  $\mu$ V peak-to-peak, 0.1 to 10 Hz.

Here, too, four grades are available, AD545J, K, L, and M, all of which are specified over the 0 to 70 °C temperature range. Pricing starts at \$5.95 in 100-piece quantities for the J version, and all grades are available from stock.

Input circuitry is shielded from external noise and supply transients by the guarded case, which also reduces common mode input capacitance. All devices are temperature cycled and subjected to a high G shock test prior to final test to assure reliability and longterm stability.

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new "/HJ" features while still providing up to twice the speed and one-third less power consumption.

The largest in the series is the MPY-24HJ (24-bit multiplier), which has an onchip shift/normalize feature. It yields a 48-bit product in 200 ns. Its internal silicon chip measures 324 x 348 mils and attains VLSI density with over 30,000 components onchip. This multiplier is supplied in a standard 64-pin DIP.

Next in capability is the MPY-16HJ, which produces a 32-bit product in 100 ns. It consumes only 3 W, is pin compatible with the older 16-bit multipliers, and like the MPY-24HJ, can be expanded to operate on 32-, 48-, and 64-bit numbers and larger.

The MPY-12HJ multiplies a pair of 12-bit numbers and yields their product in just 80 ns. It consumes 2 W, and like the others, is ideal for digital signal processing applications such as fast Fourier transforms and digital filters.

MPY-8HJ produces a 16-bit product in 65 ns requiring only 1 W. A super-fast version of the 8-bit multipliers,

called the MPY-8HJ-1, produces a 16-bit product in 45 ns and is intended for use in digital television systems.

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## 1024-Bit RAM/EAROM Chip Saves Changing Data

In normal operation, the ER1711 operates as a fully decoded 256 x 4-bit RAM with a 1.5- $\mu$ s cycle time and a 900-ns access time; however, during powering down, a single negative pulse on the erase/write control line (E/W) saves the entire 1024-bit memory contents in associated onchip EAROM cells. This RAM/EAROM is intended for applications where data are constantly changing and must be saved in case of a power failure.

Produced by General Instrument Corp Microelectronics (600 W John St, Hicksville, NY 11802), the device provides storage of data for 72 h minimum after a 1-ms write pulse or for 30 days min after a 10-ms write pulse. Data can be recalled following power-up by application of a positive pulse to the erase/write control line, which results in data being written into RAM cells and bulk erase of the EAROM cells.

TTL compatible pins and the 4-bit wide word make this nonvolatile RAM directly compatible with 4-bit microprocessors. Typical microprocessor usages include process control applications to save state variables during power interruptions; machine or motor control to hold set points and feedback data; navigation equipment to hold varying time and position data; and cash registers for holding changing cash totals.

Additional features include 8-bit binary addressing, onchip address latching, and 3-state outputs. Power supply requirements are 5 and -12 V, and power dissipation is 540 mW. Maximum ratings for the p-channel, ion implanted MNOS device specify voltages relative to  $V_{SS}$  to lie between -26 and 28 V on the E/W pin, and between -30 and 0.3 V for all other inputs and outputs. Temperature range is from 0 to 70 °C for operation and -65 to 150 °C for storage. □

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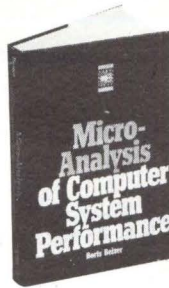
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By Boris Beizer

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### Gives you thoroughly tested procedures.

All the techniques have been proven in practice and can be directly used in the performance analysis of systems based in mini- or microcomputers, analysis of component elements of a large system, and the kinds of analyses done with limited resources such as a calculator or a pocket computer. The assembly language and system programmer will find tools for optimizing the design of individual routines or program modules; the system user and designer will find most of the analytical techniques likely to be required; and the system modeler will find practical methods that quickly get to the heart of a problem. The book includes numerous illustrations and examples that help answer the questions you face daily. 402 pp., illus., 6 x 9, \$22.50. **Circle #141 on Reader Inquiry Card.**



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## Standalone Control System in a Box

MACSYM II, a low cost realtime measurement and control system introduced by Analog Devices, Inc's Instruments and Systems Group, is said to provide a level of signal processing and control that is not available from data loggers and programmable calculators but is too costly to obtain from minicomputer alternatives. Typical applications are those requiring acquisition, storage, computation, reduction, and output of high and low level analog signals from thermocouples, strain gauges, or other universally used sensors. For example, the system could be used in laboratories, research and development facilities, and pilot plants for process control.

### Operating and Design Features

Specific measurement and control requirements are met by choice of I/O cards containing signal conditioning that directly interfaces to sensors. For example, the I/O card for a thermocouple contains isolation, linearization, and cold junction compensation.

I/O cards are available for low and high level analog signals, analog output in voltage or current configurations, direct sensor interfaces, digital I/O, isolation, and other special functions. All cards fit in all slots. Up to 16 dedicated cards can be mixed in a single chassis to provide as many as 256 channels of analog input in each backplane bay; additional chassis can be attached to provide even more channels.

The I/O cards interface to an analog-digital input/output (ADIO) controller on the analog bus that contains all components necessary for data acquisition as well as all logic necessary to interface with the computer bus. This controller isolates the microvolt signals common to the analog bus from the noisy, high level digital signals on the computer bus.



## Interfaces Directly to Sensors

Because all needed data acquisition components and logic are on the ADIO there is no need to repeat them on the I/O cards. This enables both fast turnaround time and lower cost in designing control systems.

Some examples of available cards and specifications are

*Thermocouple—nonisolated:* 4 channels; gains of 256, 512, or 1024; 120-dB CMRR at  $\pm 10$  V; 0.01%, 12-bit linearity;  $\pm 90$ -Vdc protection.

*Thermocouple—isolated:* 4 channels; 120-dB CMRR at  $\pm 600$  V; gains of 256, 512, or 1024; 0.05%, 10-bit linearity.

*Analog out:* 4 channels;  $\pm 10$ -mA output at  $\pm 10$  V; 0.05%, 10-bit linearity; 40-Vdc protection.

*CMOS MUX:* 32 single-ended or 16 differential inputs; gains of 1, 16, or 256;  $\pm 0.001\%$ , 16-bit linearity;  $\pm 0.025\%$ , 11-bit accuracy.

*Pacer clock:* 10-MHz crystal time base; 20- $\mu$ s to 12-h interval; external trigger user input; 100-kHz clock, pacer signal user output.

*Strain gauge:* 4 channels; 0.005%, 14-bit linearity; 5- to 10-V or 0.1- to 10-mA excitation;  $\pm 115$ -Vac protection.

*Digital output:* 16 discrete, isolated outputs; 1.5-V at 100-mA output; 30-V to gnd protection; 250-V common mode protection.

System control is provided by a bit-slice microprocessor designed by the company specifically for this ap-

plication. Four 4-bit chips effectively provide a 16-bit processor.

Programming can be accomplished with an easy to use extension of high level BASIC as well as in assembly language. MACBASIC, developed as an extension of Dartmouth BASIC, allows each user to write simple instructions for a specific application. In multi-task mode, MACBASIC can be used to provide simultaneous execution of multiple, independent tasks.

MACBASIC software features include real-world I/O statements, multitasking, realtime reference, and data reduction, storage, and presentation. Real-world signals can be treated as any other variable in any program.

Because the language is interactive, a program can be examined and modified while it is running. Development errors are immediately reported at the end of each line. Lines may be added or deleted at any time.

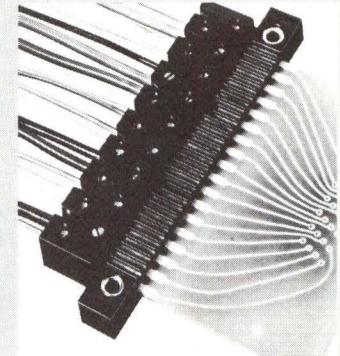
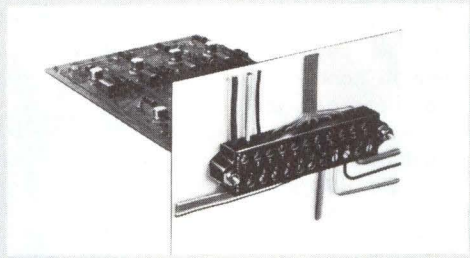
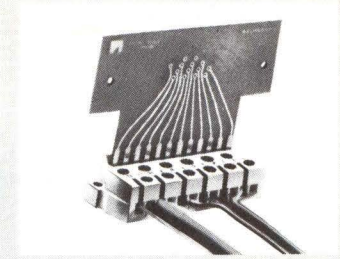
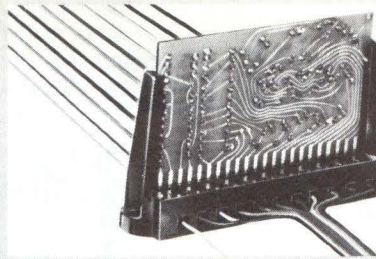
Multitasking allows simultaneous and independent running of tasks. Any task can be started or stopped at any time without affecting others. The realtime reference allows easy recording of real-world events in real time.

Standard system output is RS-232 compatible. Presentation of data can be alphanumeric via CRT, teleprinter, or external printer; or graphic, including easy generation of axis, tic marks, and labels. Up to four recorders can be operated simultaneously and independently; field size can be changed readily.

### Price and Delivery

Basic MACSYM II machines—including 16-bit processor, analog-digital I/O subsystem, realtime MACBASIC, and 64k bytes of memory in standard chassis, plus full documentation and system support—are priced at \$5600 each in 50-piece quantities. In these same quantities, complete systems, ready for operation without required extras—including basic machine plus cartridge tape drive, full ASCII keyboard, and operator control panel and CRT—cost \$7200 each. Single unit price for a complete system is \$8990. I/O cards are about \$500 each. Deliveries are scheduled to begin after February 1979. Analog Devices, Inc, PO Box 280, Norwood, MA 02062. Tel: 617/329-4700.

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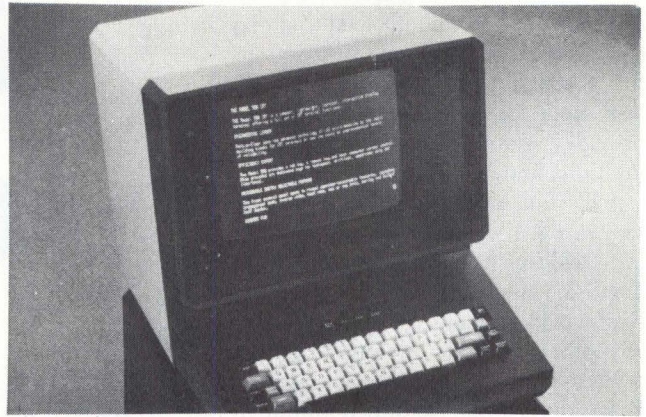
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# PRODUCTS

## Human-Engineering Features of Full Function OEM CRT Terminal Speed Data Entry

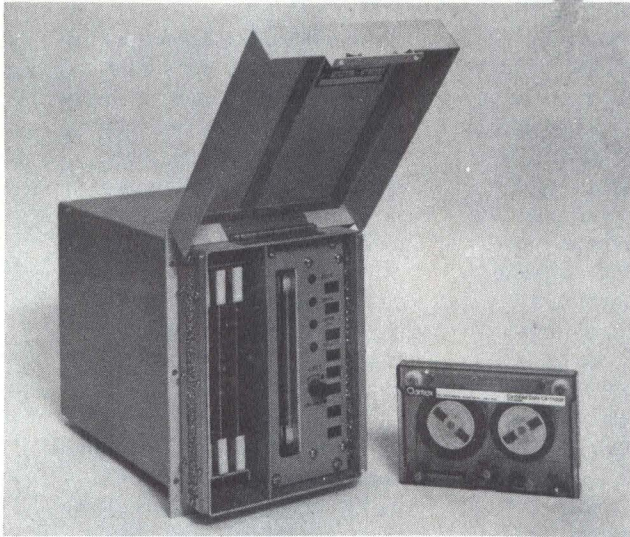
Standard features on the low cost Bantam CRT terminal such as full u/lc character set with well defined descenders, high density 7 x 10 matrix for highly legible characters, operator's choice of white on black or black on white 24-line x 80-char display, full typewriter-like keyboard with shadow numeric pad, display set deep in hood to reduce glare, and built-in self-test are said to speed data entry as well as reduce operator fatigue. Complete tabbing, full cursor addressing, and repeat, backspace, shiftlock, and separate print keys as well as ASR 33 compatible RS-232/CCITT-V.24 interfacing, key for local/online switching, and transparent mode with displayable control characters to simplify host program debugging are also standard. Available options include nonglare screen, full overstrike APL, current loop

interface, printer port, and choice of foreign language character sets. An LSI CRT controller chip contains both character decoding logic and CRT control logic. The desktop terminal weighs only 28 lb (13 kg) and measures 15 x 19 x 14" (38 x 48 x 36 cm). **Perkin-Elmer Corp, Terminals Div, Rt 10 & Emery Ave, Randolph, NJ 07801.**



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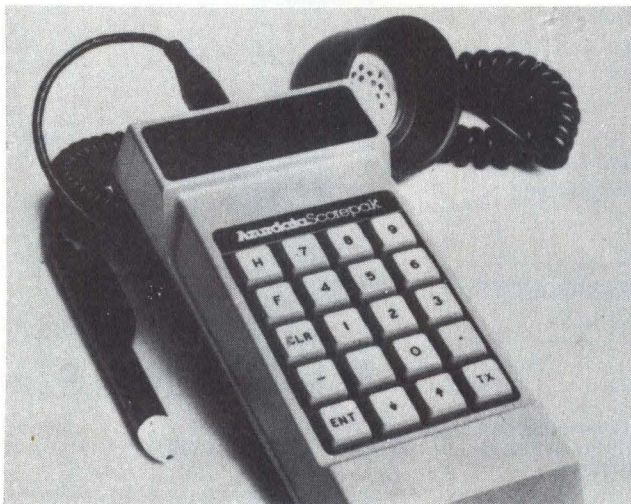
## Ruggedized 4.3M-Byte Cartridge Tape Storage Unit Functions in Hostile Environments



Developed for avionics checkout on desert airfields, the model 5100 ruggedized tape storage unit is built to MIL-T-21200 specifications and provides 2.8M- or 4.3M-byte storage capacity for severe environment applications such as exposure to extremes of temperature, salt spray, humidity, and vibration. Interfaces are available for Digital Equipment, Nova, and ROLM computers as well as all RS-232 devices. Units will operate over a range of -10 to 50 °C (to 71 °C intermittently), are drip proof, and have RFI gaskets. They contain all necessary formatting and interfacing electronics as well as R/W and tape control circuits. Data are recorded on either 3M DC-300A tape cartridges or 450-ft (137-m) "supercartridges." 30-in (76-cm)/s record/read operating speed yields a 48k-bit/s data transfer rate at the normal 1600-bit/in (630/cm) recording density. Fast search at 90 in (229 cm)/s accesses any stored data in approx 20 s. Weight is about 14 lb (6.4 kg); overall dimensions are 11 x 8.25 x 5.75" (28 x 21 x 14.6 cm). **North Atlantic Industries, Inc, Qantex Div, 60 Plant Ave, Hauppauge, NY 11787.**

Circle 201 on Inquiry Card

## Bar Code Reader Handheld Data Entry Terminal Contains 16k-Character Memory



Microcomputer control of the Scorepak portable data entry terminal allows a choice of 28k useful operating configurations through entering appropriate option codes. Units are available to read all common bar codes including Codabar, UPC (A, E<sub>o</sub>, and E<sub>i</sub>), and Plessey, with optional capabilities to read more than one bar code or automatically distinguish and read Plessey and UPC labels. Keyboard entries and wand bar code readings can be mixed in any combination as input to the 16k NMOS memory. Length of product code and option code; choice of MOD-10, -11, or no check digitizing; and choice of parity, transmission speed, and transmission code are user selectable. The units transmit in std 8-bit ASCII and either MSI bit synchronous, MSI character synchronous, or Telxon compatible codes. Operators can conduct line-by-line or rapid scans through memory or locate a specific entry or group of entries by searching for a full or partial product code or a complete line of data. Human engineering concepts in package design enable long periods of use without fatigue and operator-related errors. **Azurdata, Inc, PO Box 926, Richland, WA 99352.**

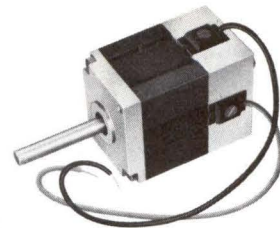
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# PICK A PITTMAN® D-C MOTOR FOR YOUR PRODUCT



**LO-COG® Servo Motors**  
3 series: 1.2, 1.6 and 2.0" OD  
Stall torques: about 1 to 128 oz.-in.



**NEW Rare Earth Field  
D-C Motors**  
1 x 1¼" cross-section  
Stall torques: 12 to 24 oz.-in.



**PITMO® Gearmotors**  
2 series: 1.38 and  
2.00" OD gearboxes  
Torque limits with  
standard gearing:  
100 & 175 oz.-in.

**PITMO® Motor-Tachs**  
2 series: 1.2 and 1.6" O.D.  
Standard tachometer gradient:  
2 volts/1,000 rpm



## THE PITTMAN CORPORATION

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9A

CIRCLE 77 ON INQUIRY CARD

### PRODUCTS

#### INTELLIGENT TERMINAL



CT-82 works with most modems or computer systems that have RS-232-C serial interfaces operating at 50 through 38,400 baud. It features 128 control functions operable from either terminal keyboard or computer program. Design incorporates Motorola 6802 microprocessor and 6845 CRT controller integrated into modular system. Internal editing functions allow inserting and deleting lines and char; erasing quadrants or lines; and doing rolls, scrolls, slides. Completed material can be block transmitted to computer or output to remote printer through built-in parallel printer I/O port. **Southwest Technical Products Corp.**, 219 W Rhapsody, San Antonio, TX 78216.  
Circle 203 on Inquiry Card

#### INTERACTIVE GRAPHICS OPERATING SYSTEM

CGOS, a multiuser operating system, is designed specifically for interactive graphics CAD/CAM applications. It supports the Designer™ IV series turnkey systems, which incorporate the CGP-100™ minicomputer. Features include support for up to 10 simultaneous tasks; file management system with multivolume disc capacity up to 600M words; dynamic allocation of task priorities; file protection and user accounting; and CPU to CPU communications and network support. **Computer-  
vision Corp.**, 201 Burlington Rd, Bedford, MA 01730.  
Circle 204 on Inquiry Card

#### SEALED DIP SWITCHES

Wave solder and flux cleaning can be performed on PC boards using DIP switches which have bottoms and terminals sealed with a thermoplastic resin. Immersion cleaning is possible when a top tape seal is added to the switch. Sealed feature is available on the full line of spst DIP switches in 2- through 10-stations with raised or recessed rockers. Thermoplastic potting operation is a part of the assembly process, not an added operation. **Grayhill, Inc.**, 561 Hillgrove Ave, La Grange, IL 60525.  
Circle 205 on Inquiry Card

#### ZERO INSERTION FORCE IC CONNECTOR

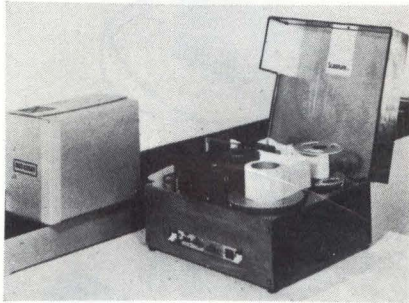
Allowing installation and removal of card file ICs without placing stress on lead pins or substrates, actuating bars on each side of connector open and close contacts to hold IC firmly in position. Edge-wipe contact design provides high contact pressure, and tapered entry ramps condition and guide IC leads into semi-closed contact entry area. Normally closed contacts prevent accidental opening of contacts during IC operation. **Scanbe Div, Zero Corp.**, 3445 Fletcher Ave, El Monte, CA 91731.  
Circle 206 on Inquiry Card

#### 3840-CHARACTER VISUAL DISPLAY UNIT

Intelligent CRT terminal model 4800 has 48 x 80 format for a 3840-char display on a 35-cm vertically mounted CRT. It features microprocessor based logic, fully regulated switching power controller, and a monitor quality orange phosphor CRT with antiglare faceplate. Separate ASCII keyboard connects to unit via a 2-m cable. Selection of transmission speed, duplex or half-duplex mode, parity, and stop bit options are performed immediately when unit is switched on. **ATL Datatronics Pty Ltd.**, Nancarrow Ave, Meadowbank, New South Wales, Australia 2114.  
Circle 207 on Inquiry Card

## PRODUCTS

### ONLINE LABEL PRINTER/APPLICATOR



Developed for online use with computer based material handling systems, U-1239 automatically prints and applies variable information labels to cartons as they pass through on a conveyor line to accuracy within  $\pm 0.25''$  (0.64 cm). Unit can print and apply fixed, random, sequential, or batch information labels, and be controlled by computer, scale, tape reader, or integral keyboard. Bar codes, OCR, human readable chars, or combinations can be printed at rates dependent on size and printing requirements. **Markem Corp**, 150 Congress St, Keene, NH 03431.  
Circle 208 on Inquiry Card

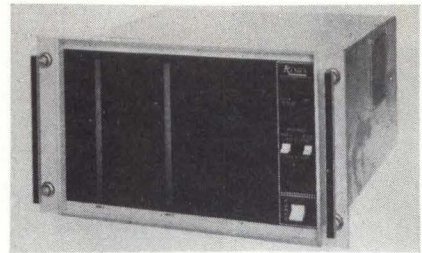
### INTELLIGENT CARD READERS

Punched hole or optical mark readers, in speeds from 150 to 600 cards/min, are available in rackmounted and table units. Occupying a single card slot, the controller contains a 6800 microprocessor, 2k x 8 RAM, up to 4k x 8 P-ROM, and interfaces to the card reader electronics. External interfaces include 20/60-mA current loop, EIA std RS-232-C, and IEEE-488 std instrument bus. Functions performed include card reader control, reading of data, code conversions, and counting. **MicroPro Inc**, Technology Ctr, Rt 309, Montgomeryville, PA 18936.  
Circle 209 on Inquiry Card

### 1000 LINES/MIN CHAIN PRINTER

ChainTrain 1210 offers full-line buffering, paper skip speed of 40 in/s (102 cm/s), paper puller, and vacuum system. Unit is a microprocessor controlled, horizontal moving font line printer whose carrier uses 8-char links riding on a monorail track. Interchangeable links enable replacement of char sets. 64-char set is standard with 48-, 96-, 128-char sets as options. Printer accepts forms from 3.5 to 19.5" (8.9 to 49.5-cm) wide, and has motorized upper and lower tractors. **Data Printer Corp**, 99 Middlesex St, Malden, MA 02148.  
Circle 210 on Inquiry Card

### PDP-11 COMPATIBLE DISKETTE SYSTEMS



Connecting directly to the PDP-11 Uni-bus and LSI-11 Q-bus, models 11/11 and 11/12 incorporate two flexible disc drives with built-in formatters, interface, and diagnostics. All elements are transparent to the DEC RT-11 operating system. ROM bootstrap is std. Individual write protect switches on each drive, busy and error status indicators, and an automatic reinitialization function are other features. **Remex Div of Ex-Cell-O Corp**, 1733 Alton St, Irvine, CA 92713.  
Circle 211 on Inquiry Card

### ECLIPSE/NOVA SOFTWARE SYSTEMS

Screen Handler and Data Dictionary are software systems for Eclipse and Nova users. Screen Handler operates as an online interface to FORTRAN and assembly language programs, as a stand-alone data collection system, and as a development tool for interactive systems. It is useful in limited memory environments. Data Dictionary is a set of standalone utilities which create, update, and report on contents of a data dictionary, plus a runtime retrieval system to interface FORTRAN programs. **Advanced Computer Techniques**, 437 Madison Ave, New York, NY 10022.  
Circle 212 on Inquiry Card

### DIRECT CONNECT ORGINATE/ AUTOANSWER MODEM



Unlike direct connect modems that use a telephone with an exclusion key arrangement to access the line after dialing, the 9113BOD has dialing capability built into its top. An audio line monitor with volume control enables the operator to hear call progress tones, and automatically shuts off upon detection of a valid carrier from the remote end. Std data rate is up to 450 baud (600 baud optional); RS-232 as well as 20-mA active current loop interface is provided. **Omnitec Data**, 2405 S 20th St, Phoenix, AZ 85034.  
Circle 213 on Inquiry Card

## Fastest EPROM Erasing!

WITH RELIABLE **SPECTROLINE**® SYSTEMS



Whether you're erasing one EPROM chip or a thousand, you'll want the latest and most advanced UV erasing system available. We have seven high performance systems to match your specific needs and your pocketbook. Prices start at \$59.50. You can erase safely and completely in as little as 7 minutes! And each system is backed by Spectronics Corporation...leader in ultraviolet technology since 1955. Write or call for more information and the name of your nearest authorized stocking dealer.

System	Automatic Timer Control	Chip Capacity	Price
PE-14	No	6	\$ 59.50
PE-14T	Yes	6	84.50
PE-24T	Yes	9	104.50
PR-125T	Yes	16	239.00
PR-320T	Yes	36	395.00
PC-1000	Yes	72	795.00
PC-2000	Yes	144	1,150.00

220 VOLT UNITS AVAILABLE

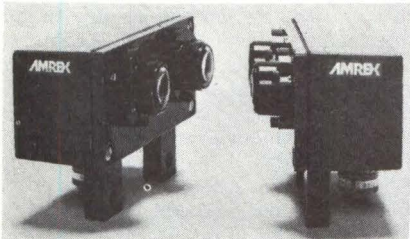


**SPECTRONICS CORPORATION**  
956 BRUSH HOLLOW ROAD, P.O. BOX 483  
WESTBURY, NEW YORK 11590  
516-333-4840

## IN-CIRCUIT TEST SYSTEM

MB9280 individually tests all components on a PCB and the PCB itself. A bed-of-nails fixture interfaces unit under test to a measurement module controlled by a Z80 based microcontroller. A floppy disc loads test programs into the controller memory. Copy of the PCB artwork serves as cutting and drilling template for customizing test fixture. Writing in-circuit test program consists of little more than a list of component positions, values, and tolerances. **Membrain Ltd**, 23 Cobham Rd, Wimborne, Dorset BH217PE, England.  
Circle 214 on Inquiry Card

## INDUSTRIAL OPTICAL DATA LINK



Solid-state model XD300 transmits digital data between two remote locations at a 300-baud data rate. The compact, 2.25 x 5 x 2.25" (5.7- x 12.7- x 5.7-cm), unit uses IR focused sources and detectors for line of sight communications. Digitized data from one or more remote sensors are sent to the link, which transmits data to another unit up to 200 ft (60.9 m) away. Op temps are -20 to 140 °F (-28.9 to 60 °C). Ambient light immunity of 10,000 ft-cd provides reliable communications even in sunlight. **Amrex Corp**, 9215 151st Ave, NE, Redmond, WA 98052.  
Circle 215 on Inquiry Card

## 10M-BYTE HARD DISC SUBSYSTEM

iCOM<sup>®</sup> 4511 consists of D3000 disc drive with fixed and removable disc units, and iCOM intelligent controller that uses a bipolar microprocessor. Up to 3 additional drives can be added to the controller for a max of 40M bytes of storage. An S-100 bus version is also available. The unit operates at 2400 rpm and has a data transfer rate of 5.0 MHz. Recording density is 2200 bits/in (866/cm), and positioning times are 10 ms track-to-track, 40 ms avg, and 70 ms max. **Pertec Computer Corp**, 20630 Nordoff St, Chatsworth, CA 91311.



Circle 216 on Inquiry Card

# LSI-11 interface . . . from MDB

GP Logic Modules ■ Peripheral Controllers  
Communications Interfaces ■ Systems Modules  
Chassis Assemblies ■ Microprocessor Modules  
Memory ■ Power Supplies

When it comes to LSI-11 interface, MDB has it:

- General Purpose Interfaces

Parallel for programmed I/O and DMA  
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Printers  
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Asynchronous  
Asynchronous with modem/data set control  
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For 2704, 2708 and 1702 UV PROMS

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Backplane/Card Guide (8 quad slots)  
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- I/O Cable Assemblies

MDB interface products always equal or exceed the host manufacturer's specifications and performance for a similar interface. MDB interfaces are completely software transparent to the host computer. MDB products are competitively priced, delivery is 14 days ARO or sooner.

MDB places an unconditional one year warranty on its controllers and tested products. Replacement boards are shipped by air within twenty-four hours of notification. Our service policy is exchange and return.

MDB also supplies interface modules for PDP\*-11, Data General, Interdata and IBM Series/1 computers. Product literature kits are complete with pricing.

**MDB** SYSTEMS INC. 1995 N. Batavia Street  
Orange, California 92665  
714-998-6900  
TWX: 910-593-1339

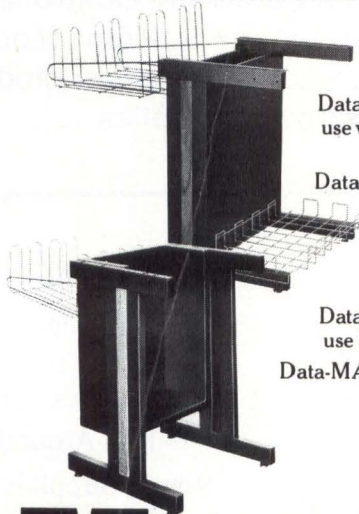
\* TM Digital Equipment Corp.

Circle 79 for PDP; 80 for LSI; 81 for IBM; 82 for DG; 83 for INTERDATA

# Data-MATE™

## PRINTER STANDS FOR USE WITH CENTRONICS PRINTERS

IN STOCK FOR IMMEDIATE DELIVERY



Data-MATE Model #10700 for use with Centronics Models 700, 701, 702, 703, 761, 763.

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Shipped assembled



### Other Data-MATE Models Available

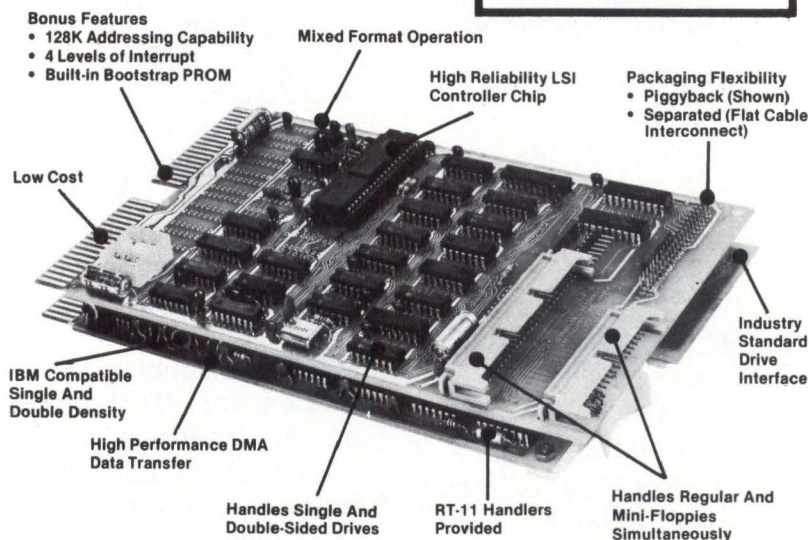
The Maine Manufacturing Company  
46 Bridge Street  
Nashua, New Hampshire 03060  
Telephone: (603) 882-5142

Distributors Inquiries Invited

CIRCLE 121 ON INQUIRY CARD

## performance

### FDI-L11 / oem FLOPPY DISK SUBSYSTEM



### FOR THE LSI-11

#### COMPUTER TECHNOLOGY

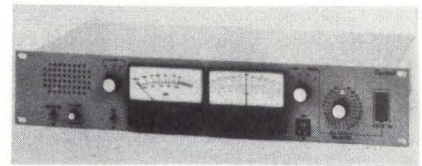
For Systems Designers 3014 Lakeshore Ave.  
Oakland, CA. 94610  
(415) 465-9000

Ask about our other LSI-11 products too...

CIRCLE 84 ON INQUIRY CARD

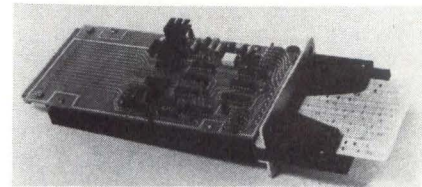
## PRODUCTS

### COMMUNICATIONS SIGNALS MONITOR PANEL



Analog/digital monitor panel for signal analysis is accessed to the EIA digital interface via std Dyna-Patch MK II patch cords at the tech control center. A selector switch and voltmeter permit precise measurement of either a positive or negative voltage on any of the interface's individual leads. Levels of VF analog signals patched to panel are measured on a selectable range dB meter. A speaker with volume control permits qualitative analysis. **Dynatech Data Systems**, 7644 Dynatech Ct, Springfield, VA 22153.  
Circle 217 on Inquiry Card

### OPTICAL CARD READER

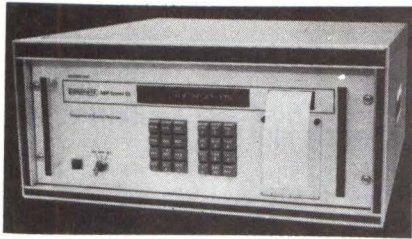


Model H-68 avoids readout errors that could otherwise be caused by motion variables in inserting and withdrawing cards. Incorporating a single PC board, the unit reads cards containing up to 68 col. Cards are inserted all the way into the reading slot and then withdrawn. As the card is removed, the punched holes are scanned optically and card data are read out column serial, row parallel. Reader is suited to OEM and systems applications. **Taurus Corp**, Lambertville, NJ 08530.  
Circle 218 on Inquiry Card

### STANDARD LINK I/O CONTROLLER

External interface of the I/O controller to the company's std I/O bus is serial synchronous and conforms to the transmission formats common to HDLC, ADCCP, and SDLC industry stds allowing interfacing between multiple vendors equipment. Basic protocol functions are performed in the controller itself. Direct memory transfer is included. An RS-232-C EIA electrical interface, wide-band WE301/303 electrical interface, and CCITT V35/WE306 high speed balanced voltage interface are available. **Modular Computer Systems Inc**, 1650 W McNab Rd, Ft Lauderdale, FL 33309.  
Circle 219 on Inquiry Card

## SEQUENCE-OF-EVENTS RECORDERS



Monitoring the status of many 2-state inputs, the System 22 recorder includes comprehensive, continual, diagnostic self-testing; plug-in emi/rfi filters for noisy channels; redundant input optoisolators; EAROMs; and RS-232 interface. Cable plug-in of an additional input chassis expands it from 32 to 1024 channels in steps of eight. It operates directly from a 125-Vdc station battery.

**Dranetz Engineering Laboratories Inc.**, 2385 S Clinton Ave, South Plainfield, NJ 07080.

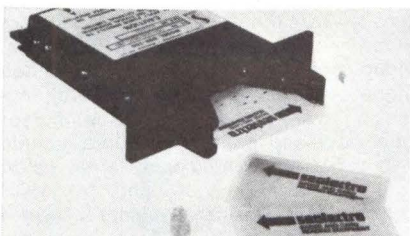
## LOW PROFILE KEYSWITCHES

FES-9 series offers choice of snap and nonsnap action keyswitches, as well as incandescent lamp or LED indication, suited to computer and automatic control systems. Additional variations are reed capsule or solid-state types, momentary or alternate action, and direct panel or adapter mounting. Operating forces are 50 ±15 g at max stroke nonsnap, 70 ±30 g at snap point, 150 max for lock type, and 90 ±30 g max stroke for nonsnap with LED.

**Fujitsu America, Inc, Component Sales Div.**, 910 Sherwood Dr, Lake Bluff, IL 60044.

## SOLID-STATE OPTICAL BADGE READER

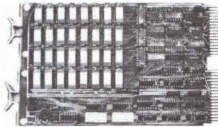
Using GaAs LED light source and photo-transistor sensors, DSR-100 reads std 12-row, 22-col badges or 12-row, 20-col credit cards. Built-in optically generated strobe pulse provides up to 22 pulses for data verification, regardless of badge punching. Sensor outputs are open collector and can be directly interfaced with low impedance TTL or high impedance CMOS logic without intermediate circuitry. All external connections are via 2 20-way ribbon cable connectors. **Programming Devices Div of Sealectro Corp.**, Mamaroneck, NY 10543.



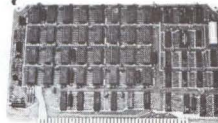
Circle 222 on Inquiry Card

# 64KB MICROPROCESSOR MEMORIES

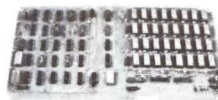
- S-100-\$695.00
- LSI 11 - \$890.00
- 6800 - \$995.00



**CI-1103 32K x 16**



**CI-6800 64K x 8**



**CI-8080 64K x 8**

**CI-S100** — 64K x 8 on a single board. Plugs directly into the IMSAI, MITS, TDL, SOL and most other S-100 Bus computers. No wait states even with Z80 at 4Mhz. Addressable in 4K increments. Power 6 watts. Price \$695.00

**CI-1103** — 8K words to 32K words in a single option slot. Plugs directly into LSI 11, LSI 11/2, H11 & PDP 1103. Addressable in 2K increments up to 128K. 8K x 16 \$390.00. 32K x 16 \$890.00 qty. one.

**CI-6800** — 16KB to 64KB on a single board. Plugs directly into Motorola's EXORcisor and compatible with the evaluation modules. Addressable in 4K increments up to 64K. 16KB \$390.00. 64KB \$995.00.

**CI-8080** — 16KB to 64KB on single board. Plugs directly into Intel's MDS 800 and SCB 80/10. Addressable in 4K increments up to 64K. 16KB \$390.00. 64KB \$890.00.

Tested and burned-in. Full year warranty.



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Computer Products Division

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**CIRCLE 88 ON INQUIRY CARD**

# ROYTRON™ plug-compatible reader/punch

Desktop combination reader/punch with serial asynchronous RS-232C compatible interface. Designed to operate with a terminal device on the same serial data lines or alone on a dedicated serial line. Reader will generate data at all standard baud rates up to 2400 baud.

Punch accepts data at all standard baud rates up to 600 baud continuous or 4800 baud batch, utilizing a 32 character buffer.

Two modes of operation are provided: *Auto Mode* — Simulates Model ASR 33 Teletype using ASCII defined data codes (DC 1, 2, 3 and 4) to activate/deactivate the reader or punch; *Manual Mode* — Code transparent mode. Panel switches control activation/deactivation of reader or punch and associated terminal device.

Tape duplication feature is provided by setting unit to LOCAL mode.



**MODEL 1560-AS**

High-speed, compact, with self-contained electronics and power supply. Complete in attractive noise dampening housing.



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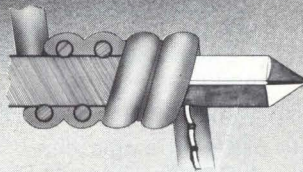
**CIRCLE 86 ON INQUIRY CARD**

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SLIT-N-WRAP**  
tool with Tefzel  
wire makes  
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other wrap tools.

Now you can wrap  
thick insulated wire  
**4 TIMES FASTER**  
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P184, with  
100' of 28  
gage Tefzel  
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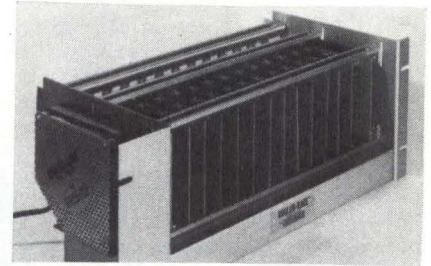
**CIRCLE 87 ON INQUIRY CARD**

## PRODUCTS

### FREQUENCY SHIFT KEYING SYSTEM FILTERS

Passive filters JW33-2267A-68B are voice-channel devices used to eliminate the 8-kHz sample rate for PCM systems while assuring adequate voice frequency transmission. -2218A-19A are designed for FSK modem circuits to differentiate between mark and space transmissions, and -2133A-34A are bandpass and band-rejection filters for use in telecommunications test equipment where a 1020-Hz test tone is used as the holding tone. Advantages include low noise, inherent immunity to external rf interference, and an extended op temp range. **Sprague Electric Co.**, 555 Marshall St, North Adams, MA 01247. Circle 223 on Inquiry Card

### PCB RACK WITH BLOWER



Kooler-Kage™ for std 19" (48-cm) cabinetry has a built-in centrifugal blower that moves 25 ft<sup>3</sup>/min (0.75 cm<sup>3</sup>/min) into a baffled plenum chamber to reduce the velocity and distribute the air volume over the entire area. As the cool air flows from bottom to top displacing the air heated by the components, each card is cooled on both sides, and all cards are cooled equally. Card guides have a 75% open design to facilitate air flow. **UNITRACK<sup>®</sup> Div, Calabro Plastics, Inc.**, 8738 W Chester Pike, Upper Darby, PA 19082.

Circle 224 on Inquiry Card

### IMAGE ARRAY PROCESSOR

IP 5000 meets requirements for high resolution color, multi-image monochrome, or pseudocolor displays. The processor consists of computer interface, memory management and data control, memory control units with intensity transformation, master timing, video cards with 8-bit DACs, digital video processor arithmetic unit, video signal digitizer and control, alphanumeric overlay generator, and cursor generator and control. Features include 640 x 512 element display area, up to four 256 level images, and 16k MOS refresh RAM. **DeAnza Systems Inc.**, 3444 De La Cruz Blvd, Santa Clara, CA 95050. Circle 225 on Inquiry Card



ELIMINATE NOISE  
PROBLEMS WITH DELTEC'S

# COMPUTER POWER CONDITIONER

## 5 KVA FOR LESS THAN \$1,500

Only One Computer Power Conditioner Eliminates All Noise Problems. Noise on a computer power line causes data and memory loss as well as mysterious crashes and errors. This noise can pass through voltage regulators and dedicated power lines.

Deltec DLC Series computer power conditioners eliminate noise and regulation problems. Unique shielding provides 120 dB (1,000,000:1) reduction for: Transients—Voltage Spikes—Ground Loops—Line Noise caused by RFI or EMI (radiated noise).

The DLC regulates voltage within 3% over a 30% input voltage range.

RANGES: 1200VA - 30KVA 1ø; 9KVA - 90KVA 3ø

### AC POWER HANDBOOK

... gives you hard answers on how to solve AC Power problems. Now available at our cost of \$3.00. Write or call for a copy.

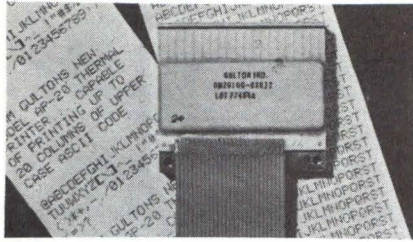
**DELTEC**

CORPORATION

80 Buenos Ave. • San Diego, CA 92110  
Phone (714) 275-1331

**CIRCLE 85 ON INQUIRY CARD**

## GANGABLE 20-COLUMN THERMAL PRINTHEAD



The 2" (50-cm) DM20100 permits non-impact printing. Applications include medium speed alphanumeric strip and page printing, and ganging in wider column applications such as 40- and 80-col printers. Side-by-side stacking extends the col width without forming a large printing gap. Char line speeds through 7 lines/s are possible printing a full 5 x 7 matrix char on std 90 °C heat sensitive paper. **Gulton Industries Inc, Hybrid Microcircuit Dept**, 212 Durham Ave, Metuchen, NJ 08840. Circle 226 on Inquiry Card

## SNAP-IN LED INDICATORS

558 series mounts in a 0.156" (0.396-cm) hole and 559 series in 0.250" (0.635-cm) hole, in panels from 0.031 to 0.062" (8 to 1.6 mm) thick, with no need for mounting hardware. Both series include red, green, or yellow LEDs with or without integral current-limiting resistors. 5 V at 15 mA is typ power requirement for units with resistors; 559 series includes red LED with integral resistor for 12-V applications. Both series are available with 6" (15.2-cm) color-coded wire leads or with straight terminals suitable for wire-wrapping. **Dialight, a North American Philips Co**, 203 Harrison Pl, Brooklyn, NY 11237.

Circle 227 on Inquiry Card

## SERIES/1 SUBSYSTEMS

Including software drivers that provide software compatibility with IBM series/1 operating systems, 7- or 9-track 1050 magnetic tape systems have recording densities of 200 to 1600 bits/in (78 to 630/cm) and speeds of 12.5 to 125 in/s (31.7 to 317.5/cm). With 40M to 300M bytes of storage on removable media, 6050 disc storage system can accommodate from 1 to 4 drives in a single or dual processor environment. Model 9550 300-, 600-, 900-, and 1500-line/min (64 char) printer systems operate without software modifications. **Datum Inc**, 1363 S State College Blvd, Anaheim, CA 92806.

Circle 228 on Inquiry Card

## VIDEO INTRUSION DETECTOR

Performing surveillance activities of up to 25 acres (10 ha), MDU-2-CPR motion detector features detection probabilities in excess of 99.9%. Normal amb motion is processed to eliminate false alarms. Detection is based on light measurements made at over 16k locations in the monitored scene. These are compared with live incoming video; locations where differences occur are then processed. The equipment outputs alarm signals to devices and displays the alarmed scene. **Video Tek, Inc**, 8 Morris Ave, Mountain Lakes, NJ 07046.



Circle 229 on Inquiry Card

## TRANSPORTABLE META ASSEMBLER



For use with Intel MDS systems, mini-computers, and large computer systems, TMA language and syntax are compatible with AMD AMDASM. Allowing users to define assembly language, and then assemble product format object code, it can be used alone or in conjunction with STEP-2, a standalone realtime interactive development instrument. When used on an MDS system, 64k memory and ISIS II are required; a computer system requires a 16-bit word, FORTRAN, 18k words of memory, and a disc file. **Step Engineering, Inc**, PO Box 61166, Sunnyvale, CA 94088.

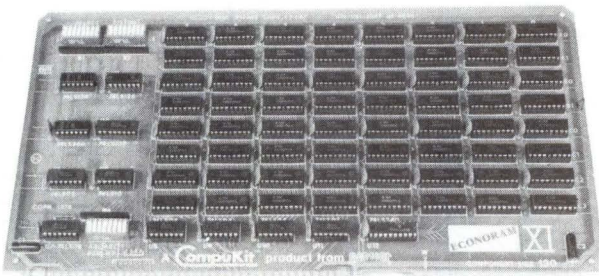
Circle 230 on Inquiry Card

## ELECTRO OPTIC CONNECTORS

Threaded SMA and quick disconnect bayonet TPS accommodate single fibers as small as 125 μm and bundles as large as 1143 μm in diameter. SMA requires precision torquing in assembly, and is subject to loosening under vibration. Fiber cables using Tefzel or Kevlar strength members must be either tool crimped or epoxied to the connector. TPS overcomes these weaknesses using a 3-lug bayonet for stability. In addition, it is positive locking, requires no torquing, and cannot come loose under vibration. **Trompeter Electronics, Inc**, 8936 Comanche Ave, Chatsworth, CA 91311.

Circle 231 on Inquiry Card

# Econoram XI™ is a 32K X 8, SBC compatible static memory board.



These boards are burned in for 200 hours, serial numbered, guaranteed to operate at 3.2 MHz over the full commercial temperature range, and qualified under our Certified System Component program (in the event of failure, boards are immediately replaced — not repaired — for fastest possible turnaround).

They are designed specifically for the Intel/National 80/10 and 80/20 machines, and feature a multi-block configuration that allows independent addressing of blocks of memory anywhere on the memory map. Where cost is a prime consideration, Econoram XI is also available in "unkit" form (similar to standard kit products, but with sockets and bypass capacitors pre-soldered in place) at substantial savings.

We have the memory you want, and we have it now: contact us for OEM/production quantity pricing schedules and additional technical information.

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## PRODUCTS

### FREQUENCY SYNTHESIZER INTERFACE



Model 1488A-12 is designed for incorporating the company's 5100 series synthesizers into the IEEE 488/1975 GPIB. Connected into synthesizer and host system via std cables, the interface meets all constraints specified for the GPIB, and provides everything needed for full control of programmable parameters. It accommodates up to 1M 8-bit data transfers/s and provides full buffering of data. Data entry is byte serial. **Rockland Systems Corp**, 230 W Nyack Rd, West Nyack, NY 10994.  
Circle 232 on Inquiry Card

### 100- AND 325-MHz CLOCK GENERATORS

Offering variable frequency clock signals over a wide bandwidth, instruments provide basic clock source for pattern generator and bit error rate test modules at up to 325M-bit/s data rates. MS-101 operates from 1 kHz to 100 MHz, and uses a voltage controlled oscillator to provide a variable frequency clock output signal. Up to 3 separate crystal oscillators may be installed as an option. MS-301 operates from 1 to 325 MHz, but only 1 crystal oscillator is optional. **Tau-Tron, Inc**, 11 Esquire Rd, North Billerica, MA 01862.  
Circle 233 on inquiry card

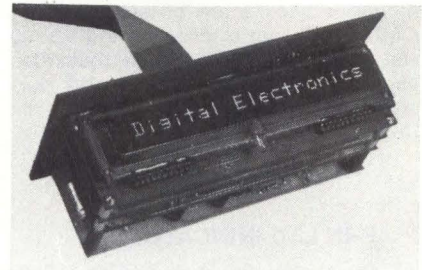
### 6400-BIT/IN DIGITAL CARTRIDGE DRIVE

Model 3164 contains 3100 drive mechanism with mechanical latch, 6400-bit/in (2519/cm) 4-track head with selective erase features, and single board electronics assembly. It records and reproduces data using a cartridge which mechanically conforms to ANSI Std X3B5/75-43. Drive mechanism complies with ANSI/ECMA/ISO stds and is built to operate in environmental and vibration/shock extremes. Center of gravity mounting of motor and attached optical tachometer enable drive to maintain proper capstan pressure in any position. **Tandberg Data Inc**, 4060 Morena Blvd, San Diego, CA 92117.  
Circle 234 on Inquiry Card

### PDP-11/34 MOS MEMORY

Single-board MS11 memory can be added to current PDP-11/34 processors and will be standard with some PDP-11/34A configurations. It is available in 128k- and 256k-byte versions. Both show performance improvements of 20% in noncache and 10% in cache over previously used memory. Nominal cycle time is 15 ns, and power consumption is 50 to 75% that of equivalent memory configurations. **Digital Equipment Corp**, Maynard, MA 01754.  
Circle 235 on Inquiry Card

### INTELLIGENT RANDOM-ACCESS DISPLAY MODULE



A 20-char/col, dot matrix, vacuum fluorescent microdisplay, the DE/320 features the full ASCII 96-char set, on-board microprocessor with character generator, display buffer, refresh, and control logic; and 5-V dc to dc converter. Natural blue-green chars are bright and clear and can be filtered to different colors. Chars are formed on low power displays and can be viewed from up to 10' (3 m). All char positions are uniquely addressable. Both parallel and serial (1200-baud) interfaces are available. **Digital Electronics Corp**, 415 Peterson St, Oakland, CA 94601.  
Circle 236 on Inquiry Card

### FULL-DUPLEX ORIGINATE/ANSWER MODEM



Model 1255, an efficient 1200-bit/s modem, eliminates line turns characteristic of half-duplex operation to increase throughput 4-fold, reduce connect time, and maintain viable data integrity. The unit is designed specifically to work in a direct connect mode, and is registered with the FCC to work with permissive jack or "data" jacks. It is compatible with itself, VA34XX modems, and the 1234 acoustic coupler. **Anderson Jacobson, Inc**, 521 Charcot Ave, San Jose, CA 95131.  
Circle 237 on Inquiry Card



### SMALL BUSINESS COMPUTER CRT TERMINAL



Compatible with S-100 bus microcomputers, terminal accepts separate TTL video and sync, and interfaces with existing alphanumeric video display boards. It also offers a monitor projecting char-by-char reversed video, reduced intensity, and block and line graphics. When used with Flashwriter video board, it provides a 16 x 64 display on a 12" (30.5-cm) screen, 900-line resolution at center, and 750-line resolution at the borders. Keyboard has typewriter format and numeric keypad. **Vector Graphic Inc**, 31364 Via Colinas, Westlake Village, CA 91361. Circle 238 on Inquiry Card

### FIBER OPTIC PCB SOURCE AND DETECTOR ASSEMBLIES

Featuring a plastic DIP and an integral fiber optic cable that exits the 0.35 x 0.42 x 0.60" (0.889 x 1.067 x 1.524 cm) package parallel to the PC board, detector assemblies have a low voltage, high speed silicon PIN photodiode that operates in reverse bias mode. Source assemblies use a high power GaAlAs emitter having a peak emission wavelength of 790 nm for optimum transmission in plastic fiber, and a radiant rise-time of 20 ns. Radiant power output from the end of the integral fiber optic cable is as much as 200  $\mu$ W depending on length of fiber. **Texas Instruments Inc**, PO Box 5012, Dallas, TX 75222. Circle 239 on Inquiry Card

### 400-LINE SPECTRUM ANALYZER

Model SD345 FFT signal analyzer operates both as standalone instrument and as element in signal processing systems. It combines narrowband spectrum analysis of signals up to 100 kHz with ability to perform  $\frac{1}{3}$  octave and octave analysis of acoustic data by addition of a single optional plug-in board. Video display with clear across non-parallax X and Y grids, alphanumeric annotation, and data scaling presents time-domain and frequency domain data simultaneously. Dynamic range is 70 dB. Touch control front panel is operator/instrument interface. **Spectral Dynamics**, PO Box 671, San Diego, CA 92112. Circle 240 on Inquiry Card

### HEAT DISSIPATION SYSTEM

PE series conduction bar heat dissipation system for 0.300" (7.6-mm) DIP systems places no restrictions on distance between rows of DIPs or between DIPs in a row. Adaptable to any size boards, system consists of conduction bars and side rails, both made of certified high thermal conductivity copper and solder plated. Conduction bars for a single DIP with up to 16 pins have solder pins at 0.70" (1.77 cm) OC in lengths up to 14" (35.6 cm). **International Electronic Research Corp**, 135 W Magnolia Blvd, Burbank, CA 91502. Circle 241 on Inquiry Card

### PRINTER/PLOTTER INTERFACE

A 2-board, microcontroller based Nova/Eclipse compatible interface that links the company's 5000 refresh vector graphic system to electrostatic printer/plotters, the MG556 converts a non-ordered vector list directly to raster input. Hardcopy generation is performed in hardware, eliminating the time delay inherent in software processing. Vector-to-raster conversion proceeds at the plotter's max output rate with hardcopy obtained in approximately 10 to 15 s. **Megatek Corp**, 1055 Shafter St, San Diego, CA 92106. Circle 242 on Inquiry Card

## PDP-11 & LSI-11 users ...here's plug compatible cartridge storage



### CARTRIDGE TAPE DRIVE

#### THE MODEL 650 PROVIDES:

- 30 IPS Read/Write, 90 IPS Rewind/Search
- 48,000 Bits/Sec Transfer Rate
- 2.5+ Megabytes per cartridge
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- Model 2200—1 or 2 Tape Drives in 5" package
- Model 2400—Up to 8 Tape Drives in 9" package
- Model 2710—Portable Recording System with up to 2 Drives
- Model 86008 Formatter—Used in all Tape Storage Systems. Complete ANSI compatibility with powerful data handling features.

### INTERFACES

All tape systems are available with the following controllers: PDP-11/LSI-11/NOVA, ROLM/INTERDATA/ALTAIR/8080/RS232/NTDS.

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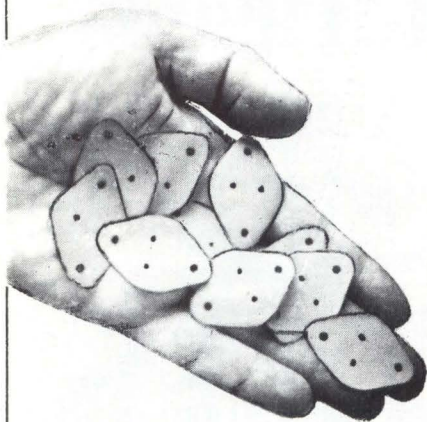
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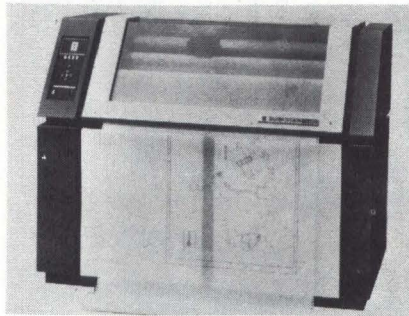
## **PRODUCTS**

### **1.75" HIGH CHARACTER LED DISPLAY PANEL**

Taskdata provides 1.75" (4.45-cm) high alphanumeric chars using red LEDs in 5 x 7 dot matrix font. Display panel is 14" (35.6 cm) long and displays up to 8 chars with serial or parallel input ASCII data. Multiple panels can be joined horizontally or stacked vertically. 32-char memory allows sequential rotation through 4 8-char groups, or focus on single 8-char message. One PC card holds all support electronics. Unit is plug-compatible with most computers through RS-232-C interface or differential inputs for daisy-chaining. **Logic Electric**, PO Box 5154, Kingwood, TX 77339.

Circle 243 on Inquiry Card

### **DIGITAL PLOTTING SYSTEM**



A 36" (91.4-cm) wide, 4-pen unit, model 3653SX uses built-in microcomputers to achieve an exceptionally smooth line. Resolution is 0.001" (0.025 mm); resolutions of 0.002, 0.004, 0.005, 0.008, and 0.010" (0.051, 0.102, 0.127, 0.203, and 0.254 mm) can be switch selected. Compatible with the company's graphic machine language, the plotter incorporates interface considerations including online, offline, or remote with error correction, and is supplied with plotting software. **Zeta Research Div, Nicolet Instrument Corp**, 2300 Stanwell Dr, Concord, CA 94520.

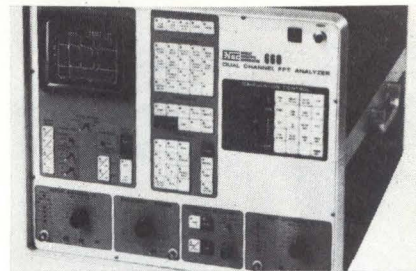
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### **MODULAR DESKS**

Modules can be arranged in a variety of combinations at the same or varying heights, in straight lines or return, for a variety of EDP applications. Variations may be provided initially or later as requirements change. The modular desk is available in std [28" (71-cm)] or keyboard [26.25" (66.68-cm)] heights; return wedges are 45 and 90°. Work surfaces are 48, 60, and 72" (122, 152, and 183 cm) wide, 30" (76 cm) deep. **Scientific-Atlanta, Inc, Optima Div**, 3845 Pleasantdale Rd, Atlanta, GA 30340.

Circle 245 on Inquiry Card

### **MULTIRANGE EXPANSION FOR FFT ANALYZER**



Portable 2-channel model 660A digital expander option -2D preserves basic 800-line (1 channel) or 400-line (2 channel) high resolution of the analyzer within the expanded window. Window can be set as high as 100 kHz. Out-of-window large signal protection is provided by a choice of 13 low pass filters from 10 Hz to 100 kHz. Resolution ranges from <0.64 mHz to 6400 Hz. **Nicolet Scientific Corp**, 245 Livingston St, Northvale, NJ 07647.

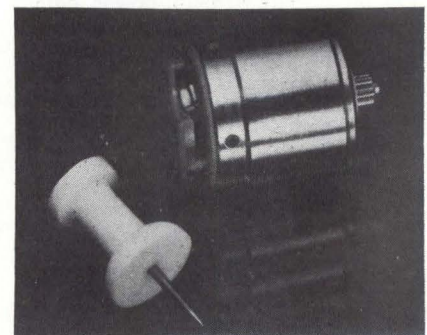
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### **ELECTROMAGNETIC BRAKES**

"Failsafe" line, for controlled stopping and/or holding rotating loads, is claimed to be smaller and lighter than competitive designs. Standard brake is spring-applied and electromagnetically released. Available static torques range from 6 to 75 lb/in (1.07 to 1.32 kg/cm). **Automotive Components Marketing Div, Facet Enterprises, Inc**, Oakwood Ave, Elmira, NY 14903.

Circle 247 on Inquiry Card

### **DC MICROMOTOR WITH INTEGRATED TACHOMETER**



Model 16 GIC, for use in miniature drive systems requiring speed control, has ironless rotor with tachometer coil wound directly on motor coil. Unit is 16 mm in dia, with body length of 17.7 mm. Coil arrangement reduces voltage induced by motor current by half. 5-segment motor commutators are silver alloy; those for tachometer are gold alloy, as are both sets of brushes. Max rotor temp is 100 °C; motor voltage is 6 Vdc. Unit is available with or without output pinion. **Portescap U.S.**, 730 Fifth Ave, New York, NY 10019.

Circle 248 on Inquiry Card

### MINIATURE 6-POLE C FORM LATCHING RELAYS

PC board mountable 205 relays, 1.437" (3.649 cm) high and 0.50" (1.27 cm) wide, offer edge to dome<sup>™</sup> contacts for reliability in situations where they are infrequently used. Orthogonal wiping action provides a constantly clean surface critical for low level signal applications. Life expectancy is 30M operations. Bistable magnetic action helps sustain contact closure in either position of the double throw, and protects against shock and vibration. **T-Bar Inc.**, 141 Danbury Rd, Wilton, CT 06897. Circle 249 on Inquiry Card

### MINI-FLOPPY RS-232 STORAGE SYSTEM

Up to 179.2k char are stored in the model 400, which is designed to interconnect between asynchronous RS-232 or TTY compatible terminals and a modem/CPU for store and forward applications. Dual UARTs provide for online selectable baud rate conversion from 110 to 19.2k. Software, including directory controlled file management system and context editor, resides in ROM. Additional features are auto answer, transparency mode, automatic line feed, and line mode. **Columbia Data Products, Inc.**, 6655 Amberton Dr, Baltimore, MD 21227. Circle 250 on Inquiry Card

### ECONOMICAL DATA ACQUISITION MODULES

Model DT6812 samples up to 30k channels/s with A-D conversion of each channel requiring 25  $\mu$ s. 3-state data outputs for computer bus connection are available in either CMOS or TTL. A-D converter can be externally jumpered for faster conversion with less resolution. Model DT2009 samples 100k channels/s, with A-D conversion in 6.5  $\mu$ s. Throughput rates of 75k and 35k channels/s are optionally available. Outputs are std TTL levels. Models are respectively pin and function compatible with Analogic MP6812 and MP6912. **Data Translation, Inc.**, 4 Strathmore Rd, Natick, MA 01760. Circle 251 on Inquiry Card

### 2-mW DIGITAL OPTICAL TRANSMITTER

Injection laser diode light source of OTL-1101-D provides peak optical power output of 2 mW from -40 to 50 °C. Bandwidth is 1 nm, wavelength 830 nm, and rise time less than 3 ns. Input impedance is 50/75  $\Omega$ ; input signals may be any serial format. Stably operating laser has projected life of 10<sup>5</sup> h. PIN photodiode samples laser output for demodulation and control. Companion rackmountable receiver is available. **Electro-Optic Devices Corp.**, 223 Crescent St, Waltham, MA 02154. Circle 252 on Inquiry Card

### NOVA/ECLIPSE BAUD RATE GENERATOR

A dual rate generator with one rate committed to a specific backplane pin for internal use on the I/O board, and the second totally independent generator providing different rates for use in other parts of the system, the board mounts directly to the backplane of an Eclipse/Nova CPU. Power and signals are derived from the backplane. Switchable baud rates range from 50 to 19.2k. A crystal control oscillator assures accurate timing. **California Data Corp.**, 3475 Old Conejo Rd, Newbury Park, CA 91320. Circle 253 on Inquiry Card

### PRINTER/PLOTTER

Replacing line printers and pen plotters, the 1641 HCS prints 1000 132-col lines/min. Plotting at 1" (2.54 cm)/s it produces 6 pages/min. The system prints and plots simultaneously under machine control without changing hardware. Consisting of 1600A printer/plotter and integral digital video source controller, the unit produces max hardcopy image size of 10 x 8.5" (25.4 x 21.6 cm) with resolution of 160 dots/in (63/cm) linear. Max plot width is 10.24" (26.01 cm) across 11" (27.9 cm) wide paper. **Ver-satec**, 2805 Bowers Ave, Santa Clara, CA 95051. Circle 254 on Inquiry Card

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Now, we've taken all we've learned from ChainTrain technology and applied it to our new Band Line Series of band-type printers.

The Model 3300 is just one example: it features a print data buffer/single line memory; Bit parallel, Character-serial, TTL compatible electronics. And it spews out hard copy at 300 LPM's, 132 positional line length, 64 character set, with ASCII print coding.

Our new "Band" is available for a free 30-day audition. Write or call for Model 3300 particulars!

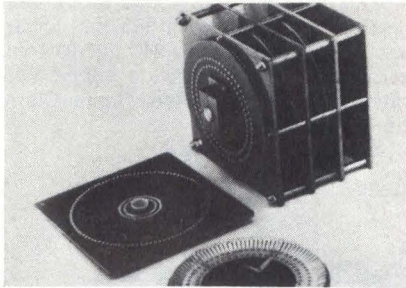


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## PRODUCTS

### PARALLELING SWITCH



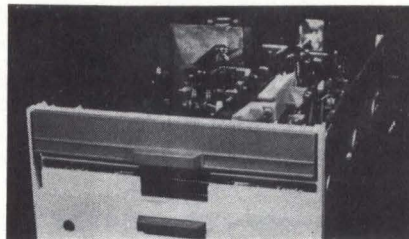
In paralleling form, all switch positions are shorted together as it is rotated, with the exception of 1 which is isolated from the rest on the same deck. Design is useful in multiple circuit cable testing or solid-state testing where all except the circuit being tested are connected, to eliminate transients causing erroneous test data. A progressive shorting form connects a new contact to all preceding contacts each time the switch is rotated from 1 position. **Cole Instrument Corp.**, 2650 S Croddy Way, Santa Ana, CA 92704. Circle 255 on Inquiry Card

### COLOR GRAPHIC DISPLAY TERMINAL

Semigraf 240, using raster scan technology, displays graphics and alpha- numerics in 8 different colors on a conventional RGB TV monitor. Microprocessor controlled, the terminal has several display formats, selectable either from keyboard or external computer. Display consists of 32 or 48 lines with 80 or 64 char/line. Characters may be displayed either normal size or double width. Both page and roll mode are provided. Four pictures may be stored in the memory of the control unit. **SRA Communications AB**, Fack, S-163 00 Spånga, Sweden. Circle 256 on Inquiry Card

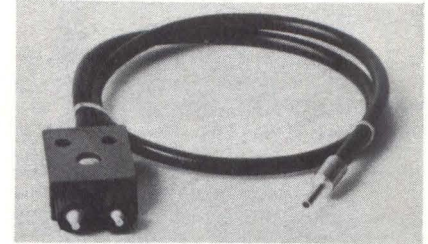
### DUAL-SIDED, DOUBLE-DENSITY FLOPPY DISC DRIVE

DataTrak 8 achieves low media wear using a fast approach and slow soft landing followed by slow takeoff with



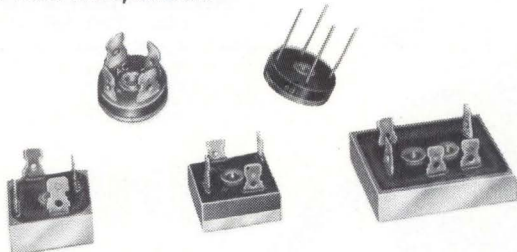
rapid acceleration through electronic and mechanical dampening of the solenoid, putting more constant pressure on the media. Storing 1.6M bytes unformatted, the unit has track-to-track access time of 3 ms, avg access time of 91 ms, and settling time of 15 ms. **Qume Corp.**, 2323 Industrial Pkwy W, Hayward, CA 94545. Circle 257 on Inquiry Card

### FIBER OPTICS SENSOR



The 0.125" (3.175-mm) dia model 6276A connects with model 1571A threaded sensor heads that mate directly with glass fiber cable to transmit light from the source head to a compact brass sensor tip and back to the detector head after bouncing off the detected object. Diodes emit either std IR or visible red light. Sensor detects small objects at close range, and/or discriminates them from nearby backgrounds. **Opcon Inc.**, 720 80th St SW, Everett, WA 98203. Circle 258 on Inquiry Card

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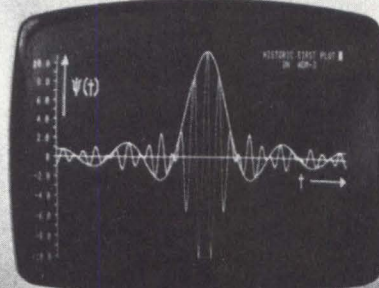
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### STEPPING MOTOR TRANSLATOR

Model 4006 is a 40-V, 6-A/phase unipolar chopper translator designed to drive 650- to 800-oz-in (4.55 to 5.6-N\*m) stepping motors. Operating at a switching frequency of 5 kHz, the unit can, when externally ramped, operate 800-oz-in (5.6 N\*m) motors in excess of 4000 steps/s. It has 12-V regulated and 40-V unregulated voltage for external use. Std features are integral power supply; 50 to 500 adjustable internal clock; 115/230-V, 50/60-Hz operation; and external TTL clock input. **Aerotech, Inc.**, 101 Zeta Dr, Pittsburgh, PA 15238.

Circle 259 on Inquiry Card

### PROGRAMMABLE REMOTE TIME DISPLAY

Model 375 allows switch selection of five time codes. Decoding logic resides in a replaceable P/ROM allowing additional codes to be provided when needed. High input impedance permits use of multiple units with a single time code source. Variable intensity LED numerals display hours, minutes, and seconds, or day-of-year/ID information can be added to increment at 365, 366, or 999. Unit mounts on ceiling, rack, or wall. **Moxon, Inc.**, 2222 Michelson Dr, Irvine, CA 92715.

Circle 260 on Inquiry Card

### UNIVERSAL SCOPE PROBE

Consisting of screw-together elements, 100-MHz system for oscilloscopes and frequency counters permits optional modules to be added on. Model WG-478 includes a coax cable with direct probe and BNC connector, low cap X10 adapter with integral probe tip, compensator with male and female BNC connectors, spring loaded hook-on probe element, ground clip assembly, and isolation boots which slip over the probe tip. **VIZ Test Instruments Group of VIZ Manufacturing Co.**, 335 E Price St, Philadelphia, PA 19144.

Circle 261 on Inquiry Card

### PC BOARD RELAYS

LZN line consisting of 24 models of low profile relays for low voltage/low current dry circuit PCB applications in communication systems minimize contact resistance. Offered in dpdt, 4pdt, or 6pdt, plus latching types, they operate on dc signals of 6, 12, 24, or 48 V, and switch dry circuits to power circuits up to 3 A at 24 Vdc. For use on PCBs mounted on 0.5" (1.27-cm) centers, models measure 0.453" (1.15 cm) in height by 1.201" (3.05 cm) in length. **Omron Electronics, Inc.**, 233 S Wacker Dr, Sears Tower Suite 5300, Chicago, IL 60606.

Circle 262 on Inquiry Card

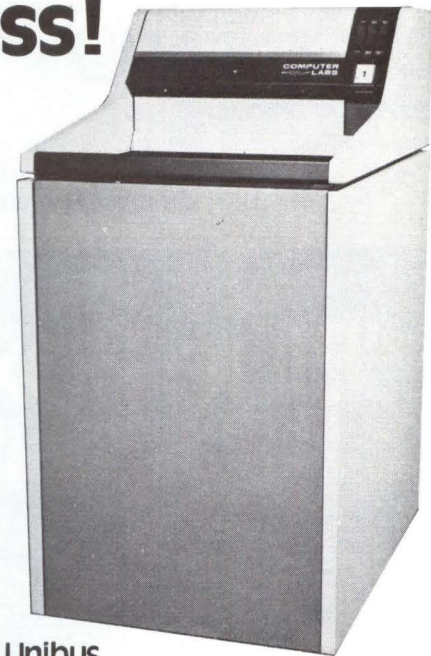
### Z80 BASED CRT TERMINAL



Special P/ROMs allow I-100 to emulate control code sets of a variety of other terminals. Features include computer control of keyboard scanning, screen formatting and editing, paging, and line drawing with a 32-char set. 1920-char screen (80 x 24) offers 25th line for status displays. There are also full 96-char ASCII set, selectable baud rates to 19.2k bits/s, block mode transmission with protected/unprotected fields, up to 8 programmable function keys, and 15-key numeric cluster. **Infoton, Inc.**, Second Ave, Burlington, MA 01803. Circle 263 on Inquiry Card

## 176 MBytes of PDP-11 disk storage for \$1000's less!

You can have up to 176 MBytes of formatted storage in an all-new moving-head disk memory system from Computer Labs. The M7000 uses a single floor-standing drive which plugs into your DEC PDP-11 Mini-Computer without any hardware or software alterations. It looks just like a DEC RJP-05 or RJP-06 to the Unibus.



This system is completely compatible with DEC disk-pack media and software such as RT-11, RSX-11, RSTS, MUMPS, etc....but it costs thousands of dollars less. In fact, add-on drives for this system cost about 50% of the DEC equivalents.

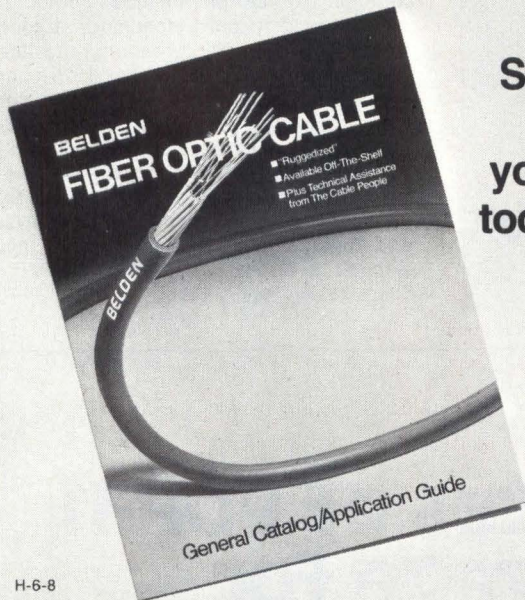
Computer Labs also offers PDP-11 users a selection of disk memory systems equivalent to the RK-05 with storage capacities through 20 MBytes, and tape memory systems compatible to TM-11. Call or write now for all the details.

## COMPUTER LABS

COMPUTER LABS, INCORPORATED

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### IDS MODEL 60 MODEM AND TERMINAL INTERFACE POCKET ANALYZER



Our Model 60 is called "The Blue Box" by thousands of users. This compact unit packs the most testing capability per dollar. Pinpoints the source of trouble between the Modem and Terminal. Provides access to all 25 lines of the EIA RS 232 interface. Has 12 monitoring LED's plus two

voltage-sensing LED's. 24 miniature switches allow isolated testing and observation of all signals. Mini-jumpers included for cross-patching and signal monitoring. Sturdy 10 oz. unit has hard plastic case, is battery powered, regular or rechargeable. Immediate delivery.

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Export: EMEC, Box 1285, Hallandale, Florida 33009

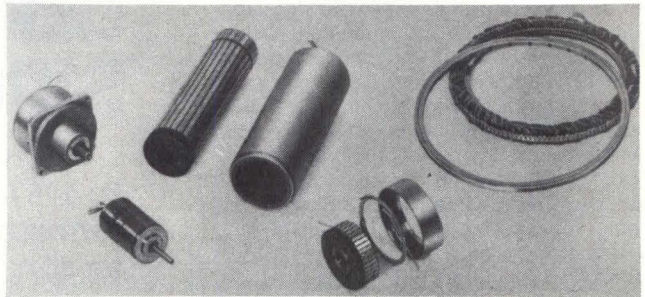
CIRCLE 97 ON INQUIRY CARD

## PRODUCTS

### TOUCH SCREEN DIGITIZER

Eliminating fixed function keyboards and lightpens, digitizer allows operators to access displayed data by touching a finger to the screen to identify the point of interest, permitting direct input to computer-controlled systems. Touch screen operation is accomplished using echo surface wave ratio process which operates on same principles as radar. Process uses 2 rows of piezoelectric transducers: 1 row on vertical edge of the screen and 1 on horizontal edge. By pulsing these transducers with signal, a wavefront is propagated across the surface of the special faceplate. Pressing a finger on the faceplate causes a reflected wave which is propagated back to the transducers and detected at that point. The unit is available for 15" (38-cm) screens with a 25° radius. **Megadata Corp.**, 35 Orville Dr, Bohemia, NY 11716. Circle 264 on Inquiry Card

### RARE EARTH DC TORQUE MOTORS



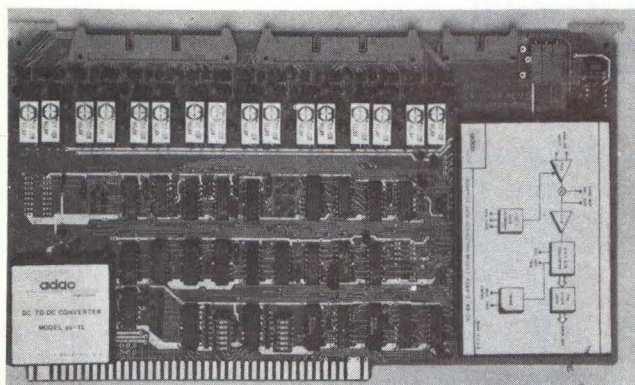
With 3 to 6 times the energy product of conventional permanent magnet dc motors, units can be packaged in much less space, offering design advantages of weight reduction and miniaturization. In addition, the motors are not permanently demagnetized by excessive current spikes or by driving them to the thermal limit of their high temperature insulation. Installation at the system level is simplified by the conventional unhusd permanent magnet motor. The devices are available in pancake, brushless, and brushless inside/out configurations. Typical applications are gimbal drives, servosystems, control surface actuation, computer peripheral equipment drives, and fin actuation. **Clifton Precision, Litton Systems, Inc.**, Marple at Broadway, Clifton Heights, PA 19018.

Circle 265 on Inquiry Card

### PROGRAMMABLE 16-LINE MULTIPLEXER

Connecting PDP-11 computers to 16 asynchronous serial communications lines, DMAX/16™ makes use of the computer's DMA capabilities to reduce CPU overhead to a minimum. Comprised of two hex modules that install into std SPC slots and connect to the rackmounted current loop or EIA RS-232-panel by separate flat ribbon cables, the unit provides complete program control of the lines, each of which operates with several individually programmable parameters. Char length is 5, 6, 7, or 8 bits; number of stop bits is 1 or 2 for 6-, 7-, or 8-bit char and 1 or 1.5 for 5-bit char. Parity generation and detection are odd, even, or none. The operating mode is half or full duplex. 15 software programmable baud rates from 0 to 9600 baud, 19,200 baud, and an external baud rate are served. **Able Computer Technology, Inc.**, 1751 Langley Ave, Irvine, CA 92714. Circle 266 on Inquiry Card

## LOW LEVEL DATA ACQUISITION SYSTEMS



Fitting directly into the Multibus of single board computers from Intel and National, 710 series units withstand common mode voltage of 250 V in presence of low level inputs. 12-bit ADC with software programmable gain amp includes automatic zero and 6 gain settings, set on a channel to channel basis to 10, 20, 50, 100, 200, and 500 mV full scale. Optional cold junction compensation circuit can be software programmed on channel to channel basis to allow direct operation with all std thermocouples. Multireed low thermal emf flying capacitor low level multiplexer processes either 8 or 16 differential low level analog inputs at 200 samples/s. Expansion beyond 16 channels is accomplished with 710-RX which contains 8 or 16 additional analog input channels/card. **Adac Corp**, 15 Cummings Pk, Woburn, MA 01801. Circle 267 on Inquiry Card

## 100-MHz FREQUENCY SOURCE

Crystal controlled 100-MHz pulse output of the Zepher C-1000 circuit card is instantly synchronized to random input triggers that can occur at rates to 20 MHz or more. Coherence is established with  $\pm 100$ -ps precision and the entire synchronization process is completed within 55 ns after arrival of external trigger. In addition to the main 100-MHz clock output, two trigger outputs are available for auxiliary synchronizing, triggering, or reference purposes. Card measures 7 x 8" (17.8 x 20.3 cm) and offers frequency stability (aging) of  $\pm 2 \times 10^{-7}$ /wk; for temperatures stability is better than  $1 \times 10^{-6}$  through a 0 to 50 °C range. Input and output levels are ECL compatible. Unit is put into use by applying dc power and coupling a trigger input and an output cable to the miniature coax connectors on the board. **Berkeley Nucleonics Corp**, 1198 Tenth St, Berkeley, CA 94710. Circle 268 on Inquiry Card

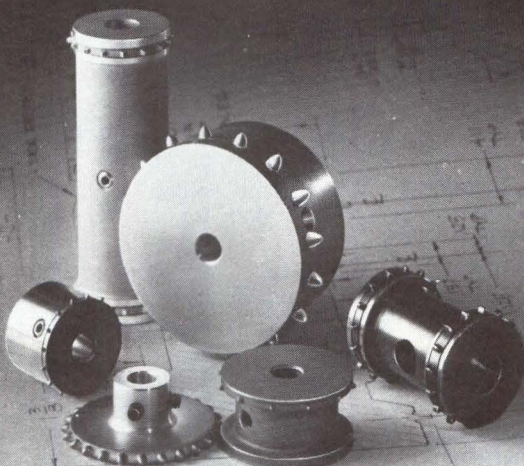
## FIBER OPTIC TRANSMITTER/RECEIVER ASSEMBLIES



Printed wiring board mountable digital fiber optic transmitter model 5000 is suitable for BiPhase-L (Manchester) encoded data transmission at rates of  $>30$ M bits/s over distances up to 1 km. Companion model 6000 provides encoded data reception. Inputs are either TTL or ECL compatible depending on whether transmitter is

operated from 5- or -5-V power supply, respectively. A GaAlAs LED serves as source. The receiver uses a silicon PIN photodiode as an optical detector. The design optimizes sensitivity for 50% duty cycle data formats and has minimal propagation delay for use in realtime systems. **Maxlight Optical Waveguides, Inc**, PO Box 11288, Phoenix, AZ 85061. Circle 269 on Inquiry Card

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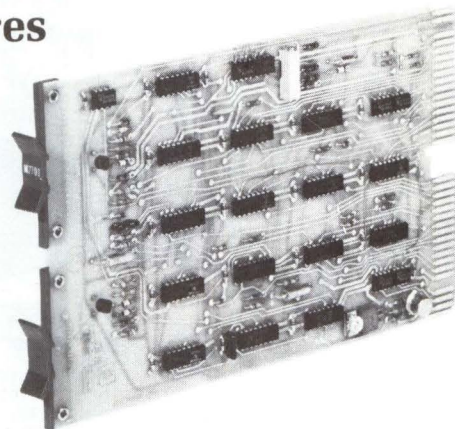
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CIRCLE 101 ON INQUIRY CARD

## PRODUCTS

### COMMUNICATIONS PORT SHARING UNIT

Model 2316, a rack or deskmounted assembly, provides a means to access up to 8 modems from 1 computer port. Designed for asynchronous/synchronous operation and supplied in modular form, the motherboard accepts a power supply unit with provision for standby, port interface unit, and up to 8 modem interface units. The system is intended for half-duplex operation; a selector switch provides speeds of 600/1200 baud asynchronous or 1200/2400/4800/9600 baud synchronous. A crystal controlled clock provides the timing. Diagnostic indicators define the operation and control between port and modems with external clock options. Each unit is self powered by 220/240 Vac, 50/60 Hz. Interface meets CCITT V.24 and RS-232-C. **Lion Systems Developments Ltd**, Halifax House, Halifax Rd, High Wycombe, Bucks HP12 3SE, England.

Circle 270 on Inquiry Card

### RUGGEDIZED PDP-11/34 COMPUTER SYSTEM

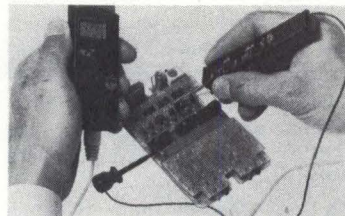
PM-1150/5RP, tested and qualified to withstand shock and vibration typical of onboard ship or mobile carrier environments, is packaged in a 10.5 x 19" (26.7 x 48-cm) chassis equipped with heavy duty rackmount slides, dowel pin receptacles, front retaining screws, reinforced cover, and removable air filter. System consists of chassis, heavy duty power supply, PDP-11/34A processor cards and backplane, bootstrap ROM loader with ASCII console emulator,

parity controller, and 32k bytes of core or semiconductor memory. Std performance features include memory management, hardware multiply/divide, memory parity, multilevel priority interrupts, and power-fail/auto-restart. System is expandable to 256k bytes of memory. **Plessey Peripheral Systems**, 17466 Daimler, Irvine, CA 92714.

Circle 271 on Inquiry Card

### MINIATURE DIGITAL MULTIMETER

Weighing <3 oz (80 g) including probe and batteries, and measuring 100 x 40 x 14 mm for base unit, and 100 x 20 x 12 mm for std probe, DMM 2000 provides 4 measuring ranges for every mode: dc to 1 kV and ac to 700 V, ac and



dc current to 2 A, and resistance to 20 MΩ, with typ accuracy of 0.5% on dc range. Unit provides true rms measurement of ac range and is completely shielded against rf and other types of interference. Permanent identification of measuring mode on LCD display and remote control of measuring mode and range on the probe simplify operation and assure error-free readout of results. Up to 100-h battery life is provided by 4 1.5-V watch batteries.

**Heuer Time & Electronics**, 960 S Springfield Ave, Springfield, NJ 07081.

Circle 272 on Inquiry Card



## NETWORK DIAGNOSTIC CONTROLLER



System 185 offers microprocessor based monitoring, diagnostics, and comprehensive management of data communications networks from the central site. It provides realtime information and status checks for a variety of malfunctions or abnormal conditions in data lines, modems, or terminal equipment, continuously monitoring all network lines with capability of polling up to 16 lines simultaneously. The system allows line and modem control and test of IBM 3600 finance communication loop systems using 1200- or 2400-bit/s loop modems, automatically notifying the central site operator of network problems and fault isolation at unattended remote sites. The unit can operate in conjunction with up to 16 central site lines equipped with 254 devices/line. **Racal-Milgo Information Systems, Inc**, 8600 NW 41st St, Miami, FL 33166. Circle 273 on Inquiry Card

## CHARACTER MODE, INTERACTIVE CRT TERMINALS



Teleprinter compatible 2620 series offer high resolution display, silent operation through high frequency scan rate, easy to use typewriter-like keyboard, editing capability, and 48 lines of data storage. HP 2621 models offer a 15.2- x 21.6-cm screen that displays u/lc and control characters. The 9 x 15 dot matrix character cells allow even

complex characters to be accurately represented. Using the built-in 120-char/s thermal printer of the HP 2621P, the operator can copy the entire display memory, the screen display, or only selected data lines. The terminal has a data logging mode that provides a printed record of all interactive transactions. **Hewlett-Packard Co**, 1507 Page Mill Rd, Palo Alto, CA 94304.

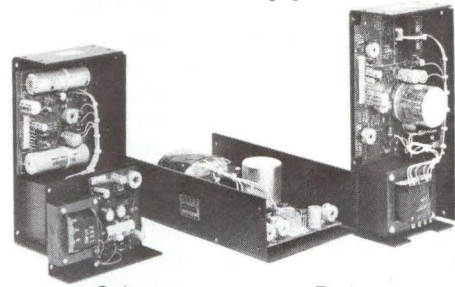
Circle 274 on Inquiry Card

## SERIAL IMPACT PRINTER

Model 5500Q Spinwriter™ plug compatible with Qume character printers uses a character print "Thimble" which contains up to 128 char. At operating speed of 55 char/s, noise level is 67 dB with cover removed and 60 dB with die cast aluminum cover installed. All components are accessible for service. Avg MTBF is >2000 h with corresponding MTTR of 0.5 h. Std printer configurations are 10 or 12 char/s (3.9 or 4.7/cm) each with proportional spacing. The unit prints either 136 col at 10 char/in or 163 col at 12/in. Subscripts and superscripts are possible as are fine line plotting and graphing. Positioning of 0.0083" (0.0211 cm) horizontal and 0.021" (0.0529 cm) vertical provides 5760 plot points/in<sup>2</sup> (892/cm<sup>2</sup>). **NEC Information Systems, Inc**, 5 Militia Dr, Lexington, MA 02173.

Circle 275 on Inquiry Card

# Floppy Disk Power Supplies



- Calcomp
- Century Data
- Persci
- Pertec
- Shugart
- Wangco

1st Output		2nd Output		3rd Output		Model	Price 1-9
Voltage	Current	Voltage	Current	Voltage	Current		
+5V	0.5A Avg 0.7A Pk	+12V	0.9A Avg 1.8A Pk			2BXFD	\$ 46.95
+5V	2.2A	-5V	0.2A	+24V	1.2A Avg 3.0A Pk	2DFD*	79.50
5V	3.0A	5V	0.6A	24V	4.0A	2PFD	99.50
+5V	6.0A	-12V	1.0A	24V	4.0A	2QXFD	134.95

Shading indicates output includes OVP.  
\*Also includes +8V @ 2A output for motor

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CIRCLE 103 ON INQUIRY CARD

## PRODUCTS

### TELEPRINTER BUFFERED MEMORY BOARD

Telebuffer 43 is a built-in memory board that combines data storage capacity of 16k char with editing and communications flexibility to support offline entry and preparation of data for efficient line and system utilization by users of Teletype model 43. Sensitive to std send and receive codes as received from downline for automatic send-receive operations, the card is completely plug compatible with the model 43. The unit features 1200-bit/s communications capability, forms handling enhancements including top of forms control and skip over perforation, control character visibility, automatic answer-back capability, and an optional offline prompt generator. **Hands On Terminals Inc**, 1215 SE Ivon, Portland, OR 97202.

Circle 276 on Inquiry Card

### SELF-SUPPORTING CONNECTORS

A std 1010 Zebra supported by nonconductive silicone sponge rubber on one or both sides, the self-supporting connector is used where a minimum force is required. With the silicone sponge a large width is provided but the force needed for deflection is drastically reduced. The device has

an 0.020" (0.051-cm) wide connecting element with a choice of 0.085, 0.115, and 0.150" (0.216-, 0.292- and 0.381-cm) sponge widths. It forms a reliable connection for larger LCDs to PC boards, where the bowing of the board has to be eliminated and where the display can be mounted flush to the board with a minimum force applied. Contact spacing center to center is 0.040" (0.102 cm), nominal resistance is 1050 to 6000  $\Omega$ , and humidity is to 100%. **Technical Wire Products, Inc**, 129 Dermody St, Cranford, NJ 07016.

Circle 277 on Inquiry Card

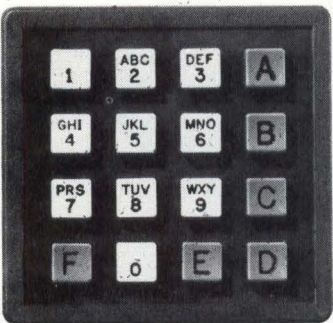
### PDP-11 UNIBUS MONITOR

Designed to aid in hardware and software debugging on PDP-11 based systems, monitor displays all 56 Unibus signals with LED indicators. Follow or hold modes are switch selectable on address and data lines. Hold is controlled by 9-position function select rotary switch. 18 3-position address switches allow the monitor to display only the activity that occurs on a single address or group of addresses.

Unibus operation may be suspended by such events as a memory reference, write to device register, interrupt, parity error, or externally supplied signal. Function select outputs and inputs are provided for interconnection with logic analyzers, digital counters, and oscilloscopes. The unit is packaged in a 5.25" (13.33-cm) high rack mountable box that includes power supply. **Three Rivers Computer Corp**, 160 N Craig St, Pittsburgh, PA 15213.

Circle 278 on Inquiry Card

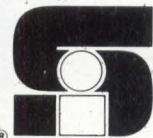
# Low Profile LED Keyboards



High performance LEDs mounted inside keybutton give visual indication of function status. 10, 12, or 16 station keyboards easily mounted from front of panel. Square or round keys, key-top or overlay decal marking. Universal circuit and pin-outs interface with most logic. Unlighted keyboards offer same design advantages but without LED lighting. Low cost, dependable, attractive. Wide selection of colors offer custom design at off-the-shelf prices.

Single station keyswitch modules, LED or unlighted, round or square, provide inexpensive method of assembling custom layouts or short-run prototype keyboards. Mount on PC or pre-punched boards with holes on .100" centers. Optional BCD or hexadecimal encoder "Addef-Boards" can be added to the Low Profile Keyboards. Compact packaging minimizes required space behind the panel.

Get the complete story now. Write for colorful descriptive catalog covering complete keyboard line.

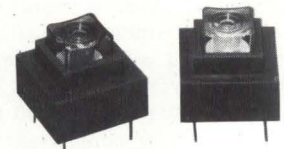
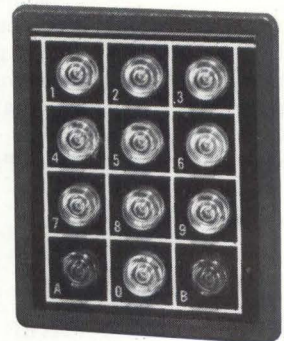


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Other STACO Company products: Custom Transformers, STACO, INCORPORATED, Richmond, Indiana; Variable Transformers, STACO, INCORPORATED, Dayton, Ohio.



## Power Supplies

Features, options, illustrations, and dimensional drawings are provided in design data catalog for open frame, modular, and power card models, in addition to custom supplies. **Power Pac Inc**, South Norwalk, Conn. Circle 300 on Inquiry Card

## Bidirectional System Printer

Brochure summarizes features of 180-char/s, logic seeking Dasher™ LP2 printers with throughputs of 80 to 300 lines/min. **Data General Corp**, Westboro, Mass. Circle 301 on Inquiry Card

## Precision Ball Bearings

Illustrated catalog contains tables of dimensions as well as characteristics of bearings, nomenclature, key terms, and information on bearing types and closures. **Barden Corp**, Danbury, Conn. Circle 302 on Inquiry Card

## Capacitive Keyboard

Brochure shows cutaways, basic specs, and options of 250M-key operation units designed to customer requirements. **Digitran Co**, a div of **Becton, Dickinson and Co**, Pasadena, Calif. Circle 303 on Inquiry Card

## Bidirectional Printer

Available in serial and parallel interface models, microprocessor based, 180-char/s Ballistic™ printer is featured in brochure. **Lear Siegler, Inc, Data Products Div**, Anaheim, Calif. Circle 304 on Inquiry Card

## CMOS Microprocessor Products

Covering the HM-6100 CPU, support circuits, bus drivers, communication circuits, and I/O controllers, 36-p reference guide provides specs, pinouts, and features. Write on letterhead to **Harris Semiconductor**, a div of **Harris Corp**, Dept 53-035, PO Box 883, Melbourne, FL 32901.

## Systems Houses and Minicomputer OEMs

Hardcover directory lists over 3000 systems houses, turnkey systems suppliers, dealers, and other "re-sellers" of minicomputers, and features a demographic profile of the OEM minicomputer market. Price is \$347, available from **Sentry Publishing Div, Sentry Computer Services, Inc**, 5 Kane Industrial Dr, Hudson, MA 01749.

## Rocker, Toggle, and Lever Operated Switches

Catalog on expanded switch series includes cross-reference guide; mechanical, electrical, and materials specs; dimensions; and mounting and wiring diagrams. **Dialight**, a **North American Philips Co**, Brooklyn, NY. Circle 305 on Inquiry Card

## Solid-State Relays

Catalog covers entire line of relays with pictures and mechanical drawings of each series, plus performance curves, and tables of electrical and general operating ratings. **Hamlin, Inc**, Lake Mills, Wis. Circle 306 on Inquiry Card

## MIL Approved Connectors

"D" subminiature, PC, circular, micro-miniature, rack and panel, rectangular, underwater, hermetic, aerospace, and modular type connectors are featured in short-form catalog. **Souriau, Inc**, Van Nuys, Calif. Circle 307 on Inquiry Card

## Optoelectronics

Specs, outline dimension drawings, and photos for reflective and optical switches, isolators, IR LEDs, and fiber optic components and data systems are supplied in catalog. **Spectronics Inc**, Richardson, Tex. Circle 308 on Inquiry Card

## Converters and Amplifiers

Specs on 1414-83 precision and 1430-83 fast settling FET op amps, 4902-83 hybrid deglitcher, and 4858 video sample/hold amplifier, among others, are shown in catalog. **Teledyne Philbrick**, Dedham, Mass. Circle 309 on Inquiry Card

## Smart Editing Terminals

Guide covers what to look for in a smart CRT, summarizes major terminals on the market, and compares features among five manufacturers. **EECO**, Santa Ana, Calif. Circle 310 on Inquiry Card

## Plasma Display Units

Separate data sheets list specs, diagrams, power requirements, and dimensions of ac driven units, available with 32- to 480-char display, alphanumeric or Katakana capability, and inherent memory function. **Fujitsu America Inc**, Chicago, Ill. Circle 311 on Inquiry Card

## Data Conversion Modules

Catalog details specs and technical information of modules and accessory circuits, and devotes one section to principles of data acquisition and conversion. **Datel Systems, Inc**, Canton, Mass. Circle 312 on Inquiry Card

## Submodular Power Supply

Block diagrams, performance specs, outline drawings, and emi and holdover storage data for 22 models of 50- to 300-W single- and triple-output switchers are furnished in brochure. **ACDC Electronics**, Oceanside, Calif. Circle 313 on Inquiry Card

## DC Switching Power Supplies

The 69 models, including SSD series rated at 1.8 to 56 V and STM series rated from 3 to 56 V, are profiled in 8-p brochure. **Sorensen Co**, Manchester, NH. Circle 314 on Inquiry Card

## Bipolar LSIs

Sections on P/ROMs, ROMs, character generators, RAMs, programmable logic, LSI logic, arithmetic elements, and interface are cataloged in data book. **Monolithic Memories, Inc**, Sunnyvale, Calif. Circle 315 on Inquiry Card

## Synchronous Modems

Data sheets describe models LDS 309 and LDS 404-B which transmit data at speeds up to 19.2k and 4800 bits/s, respectively. **Gandalf Data Inc**, Wheeling, Ill. Circle 316 on Inquiry Card

## Industrial Power Supplies

Six-page technical selector guide lists dc power supplies for computers and peripherals, telecommunications equipment, and instruments, along with specs, sizes, and weights for over 200 models. **Standard Power, Inc**, Santa Ana, Calif. Circle 317 on Inquiry Card

## Factory Computer Applications

Brochure containing eight data sheets outlines how modular system SAFES can be used for inventory control; for factory costing, documentation, and loading; and as a production planning system. **ICL, Inc**, East Brunswick, NJ. Circle 318 on Inquiry Card

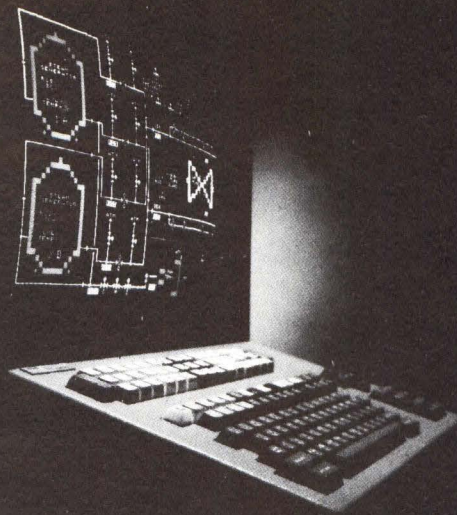
# GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—not the reader service number. Please do **not** circle the page number on the reader service card.

	PAGE		PAGE
<b>MATERIALS</b>		<b>MOTORS; ROTATIVE COMPONENTS</b>	
<b>INSULATING MATERIALS AND FORMS</b>		DC Motors	
Heat Sink Insulators		Clifton Precision/Litton Systems .....	180
Bergquist .....	176	Pittman/Penn Engineering and Manufacturing .....	167
<b>MAGNETIC MATERIALS AND FORMS</b>		Portescap .....	176
Magnetic Materials		Stepper Motor Translator	
Permag .....	191	Aerotech .....	179
<b>OTHER MATERIALS</b>		Electromagnetic Brakes	
Quartz Crystals		Automotive Components Marketing/ Facet Enterprises .....	176
Bulova Watch/Electronics .....	174	<b>PHOTODEVICES; PHOTODEVICE ASSEMBLIES</b>	
<b>HARDWARE</b>		Fiber Optics Sensor	
<b>COMPONENT PACKAGES</b>		Opcon .....	178
Quad-Inline Package		Digital Optical Transmitter	
3M/Electronic Products and Intel .....	158	Electro-Optic Devices .....	177
<b>CONNECTORS AND INTERCONNECTION SYSTEMS</b>		Fiber Optic Source/Detector Assemblies	
PC Connectors		Texas Instruments .....	175
Amerace/Control Products .....	165	<b>POWER SOURCES, PROTECTORS, AND REGULATORS</b>	
Fiber Optic Connectors		Power Supplies	
Trompeter Electronics .....	173	acdc electronics .....	12, 13
Connectors		Alpha Power .....	183
Scanbe/Zero .....	167	Eatech .....	43
Technical Wire Products .....	184	Motorola Subsystem Products .....	24, 25, 27
<b>HEAT SINKS</b>		Pioneer Magnetics .....	108
Heat Sinks		Power-One .....	7
International Electronic Research .....	175	Power Conditioner	
<b>INDICATORS; READOUTS; DIGITAL DISPLAYS; LAMPS</b>		Deltac .....	172
Displays		DC-DC Converter	
Digital Electronics/Chemetrics .....	149	Stevens-Arnold .....	118
Display Panel		<b>RELAYS</b>	
Logic Electric .....	176	PC Board Relays	
LED Indicators		Omron Electronics .....	179
Dialight/North American Philips .....	173	Miniature Relays	
<b>MOUNTING HARDWARE</b>		T-Bar .....	177
Card Rack		<b>SEMICONDUCTOR COMPONENTS</b>	
UNITRACK/Calabro Plastics .....	172	Rectifier Bridges	
<b>PANELS AND BACKPLANES</b>		Electronic Devices .....	178
Wirewrap Panel		<b>SENSORS; TRANSDUCERS</b>	
Hybricon .....	118	Audio Indicators	
<b>PARTS</b>		Citizen America .....	191
Sprockets		<b>SWITCHES</b>	
La Vezzi Machine Works .....	181	DIP Switches	
<b>WIRE AND CABLE</b>		Grayhill .....	167, 192
Fiber Optic Cable		Rotary Paralleling Switch	
Belden/Fiber Optics .....	180	Cole Instrument .....	178
<b>COMPONENTS AND ASSEMBLIES</b>		Instrument Switch	
<b>CAPACITIVE COMPONENTS</b>		A.D. Data Systems .....	188
Capacitors		<b>CIRCUITS</b>	
Union Carbide/Electronic-Components .....	183	<b>ARITHMETIC CIRCUITS</b>	
<b>FILTERS</b>		LSI Multipliers	
Filters		TRW LSI Products .....	162
Sprague Electric .....	172	<b>DIGITAL AND INTERFACE INTEGRATED CIRCUITS</b>	
		(See also Semiconductor Memories under Memory/Storage Equipment)	
		Logic Circuits	
		Texas Instruments/Components .....	46
		Schottky TTL ICs	
		Fairchild Semiconductor .....	76, 156
		Interface IC	
		Motorola Semiconductor Products .....	60, 61
		RAM/EAROM	
		General Instrument/Microelectronics .....	162
		P/ROM	
		Signetics .....	152
		Memory Controller Chips	
		Motorola Semiconductor Products .....	156
		Codec Chip	
		Siemens .....	158
		Communications Controller Chip	
		Signetics .....	44, 45
		Microprocessor Family	
		Advanced Micro Devices .....	56, 57
		Intel .....	114
		Texas Instruments Supply .....	129
		Single-Chip Microcomputers	
		Motorola Semiconductor Products/ Integrated Circuits .....	140
		NEC Microcomputers .....	136
		Rockwell International/ Microelectronic Devices .....	131
		Single-Chip Microcontrollers	
		National Semiconductor .....	130
		D-A Converter ICs	
		Advanced Micro Devices .....	150
		Analog Devices .....	52, 53
		Datel Systems .....	160
		Teledyne Philbrick .....	156
		A-D Converter ICs	
		National Semiconductor .....	152
		A-D Converter Chip System	
		Texas Instruments .....	160
		<b>LINEAR INTEGRATED CIRCUITS</b>	
		FET Op Amps	
		Analog Devices .....	162
		<b>MEMORY/STORAGE EQUIPMENT</b>	
		<b>BUFFER MEMORIES</b>	
		Teleprinter Buffered Memory	
		Hands On Terminals .....	184
		Communications Storage System	
		Columbia Data Products .....	177
		<b>FLEXIBLE DISC UNITS</b>	
		Flexible Disc Systems	
		Computer Technology .....	170
		Data Systems Design .....	11
		ICOM/Pertec Computer .....	151
		Flexible Disc Drives	
		Ex-Cell-O/Remex .....	99, 168
		Qume .....	178
		Shugart Associates .....	8, 9
		<b>MAGNETIC DISC AND DRUM UNITS</b>	
		(See also Flexible Disc Units)	
		Disc Systems	
		Alpha Micro .....	112, 113, 138
		Amplex Memory Products .....	49
		Computer Labs .....	179
		Microcomputer Systems .....	141
		Pertec Computer .....	169
		Kennedy .....	1

	PAGE
Disc Drives	
Fujitsu America .....	137
Disc Controller	
Advanced Electronics Design .....	143
Disc Drive Controller/Formatter	
Interphase .....	140
<b>MAGNETIC TAPE UNITS</b>	
Tape Systems	
Datum .....	173
Cartridge Tape System	
Digital Equipment/Components .....	134
Cartridge Tape Drives	
Data Electronics .....	40, 41
Mohawk Data Sciences .....	64
Qantex/North Atlantic Industries .....	175, 166
Tandberg Data .....	174
3M/Data Products .....	105
Cassette Recorder	
Raymond Engineering .....	142
<b>ROM/RAM PROGRAMMERS AND SIMULATORS</b>	
P/ROM Programmer	
Pro-Log .....	Cover IV
EPROM Eraser	
Spectronics .....	168
<b>SEMICONDUCTOR MEMORIES</b>	
Semiconductor Memory Systems	
Chrislin Industries .....	171
Digital Equipment .....	174
Digital Microsystems .....	23
EMM CSD/Electronic Memories and Magnetics .....	119, 121
Bill Godbout Electronics .....	173
Plessey Peripheral Systems .....	29
RAM/EAROM	
General Instrument/Microelectronics .....	162
P/ROM	
Signetics .....	152
Memory Controller Chips	
Motorola Semiconductor Products .....	156
<b>INPUT/OUTPUT AND RELATED EQUIPMENT</b>	
<b>BADGE READERS</b>	
Optical Badge Reader	
Programming Devices/Sealectro .....	171
<b>BAR CODE EQUIPMENT</b>	
Bar Code Equipment	
Interface Mechanisms .....	138
Bar Code Reader Terminal	
Azurdata .....	166
<b>COMPUTER PERIPHERALS</b>	
Militarized Computer Peripherals	
Rolm .....	115
<b>DATA TERMINALS</b>	
(See also Graphic Equipment)	
CRT Display Terminals	
Applied Digital Data Systems .....	133
ATL Datatronics Pty .....	167
Conrac .....	139
Hewlett-Packard .....	35, 36, 37, 183
Infoton .....	84, 179
Perkin-Elmer/Terminals .....	30, 31, 166
Southwest Technical Products .....	167
Vector Graphic .....	175
Teleprinters	
Diablo/Xerox .....	153
Teletype .....	32
Teleprinter Buffered Memory	
Hands On Terminals .....	184
<b>DISPLAY EQUIPMENT</b>	
(See also Data Terminals and Graphic Equipment)	
CRT Displays	
Audiotronics/Video Display .....	103
Digital Electronics .....	174
C. Itoh Electronics .....	120
Zenith Radio .....	111
Display Subsystem	
Intelligent Systems .....	190
<b>GRAPHIC EQUIPMENT</b>	
Color Graphic Display System	
Grinnell Systems .....	38
Color Graphic Display Terminals	
Ramtek .....	126
SRA Communications .....	178
Color Graphic Display Generator	
Aydin Controls .....	187

	PAGE
Graphic Display Terminals	
Vector General .....	125
Graphic Displays	
Systems Research Laboratories/ Electronic Image Systems .....	27
Image Display System	
DeAnza Systems .....	172
Touch Screen Digitizer	
Megadata .....	180
<b>INTERFACE EQUIPMENT; CONTROLLERS</b>	
Data Bus Structure	
Pro-Log and Mostek .....	114
Interface Boards	
Forethought Products .....	134
MDB Systems .....	169
Printer/Plotter Interface	
Megatek .....	175
I/O Controller	
Modular Computer Systems .....	170
Analog I/O Boards	
Burr-Brown Research .....	134
Datel Systems .....	134
Tape and Disc Controllers	
Dataram .....	95
Western Peripherals/ WESPERCORP .....	Cover II
Disc Controller	
Advanced Electronics Design .....	143
Disc Drive Controller/Formatter	
Interphase .....	140
Memory Controller Chips	
Motorola Semiconductor Products .....	156
<b>KEYBOARD EQUIPMENT</b>	
Lighted Keyboards	
Stacoswitch .....	184
Keyswitches	
Fujitsu America/Component Sales .....	171
<b>PLOTTING EQUIPMENT</b>	
Digital Plotters	
Houston Instrument/Bausch and Lomb .....	Cover III
Zeta Research/Nicolet Instrument .....	176
<b>PRINTER/PLOTTERS</b>	
Printer/Plotter	
Versatec .....	177
Printer/Plotter Interface	
Megatek .....	175
<b>PRINTING EQUIPMENT</b>	
Printers	
Dataprinter .....	177, 168
C. Itoh Electronics .....	157
Microdata .....	109
NEC Information Systems .....	59, 183
Tally .....	2
Line Printers	
Anadex .....	15
Okidata .....	4
Forms Printer	
Practical Automation .....	128
Label Printer/Applicator	
Markem .....	168
Thermal Printhead	
Gulton Industries/Hybrid Microcircuit .....	173
<b>PUNCH CARD EQUIPMENT</b>	
Card Readers	
MicroPro .....	168
Optical Card Reader	
Taurus .....	170
<b>PUNCHED TAPE EQUIPMENT</b>	
Tape Reader/Punch	
Sweda International/OEM Products .....	171
<b>COMPUTERS AND COMPUTER SYSTEMS</b>	
<b>BUSINESS COMPUTERS</b>	
Business Computer	
Micro V .....	140
<b>COMPUTER AUXILIARY UNITS</b>	
Array Processor	
Floating Point Systems .....	51
<b>MICROCOMPUTERS AND MICROPROCESSORS</b>	
Microprocessor Family	
Advanced Micro Devices .....	56, 57
Intel .....	114
Texas Instruments Supply .....	129
(Continued on page 188)	



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**CIRCLE 107 ON INQUIRY CARD**

Single-Chip Microcontrollers National Semiconductor .....	130
Single-Chip Microcomputers Motorola Semiconductor Products/ Integrated Circuit .....	140
NEC Microcomputers .....	136
Rockwell International/ Microelectronic Devices .....	131
Microcomputer Modules Motorola Semiconductor Products .....	155
Plessey Microsystems .....	93
Rockwell International/ Electronic Devices .....	136
Real-Time Microcomputer Computer Products .....	102
Portable Microcomputer Digital Equipment/ Laboratory Data Products .....	16, 17
Durango Systems .....	132
Micro Development Systems Advanced Micro Computers .....	116, 117
Intelligent Systems .....	58
Microcomputer Development Systems Futuredata .....	18, 138
Process Computer Systems .....	107
Microcomputer Design Kit Intel .....	54
Microprocessor Development Systems Aivex .....	114
Motorola Semiconductor Products .....	5
Microcomputer Software Panatec .....	144
Processor Innovations .....	118
Microprocessor Software Dann McCreary .....	120
Motorola Semiconductor Products/ Micro Systems .....	118
Technical Systems Consultants .....	120
<b>MINICOMPUTERS; SMALL- AND MEDIUM-SCALE COMPUTERS</b>	
Minicomputers Perkin-Elmer/Interdata .....	135
Systems Engineering Laboratories .....	123
Ruggedized Computer System Plessey Peripheral Systems .....	182
<b>REALTIME COMPUTERS</b>	
Realtime Microcomputer Computer Products .....	102
<b>SIGNAL PROCESSORS</b>	
FFT Analyzer Option Nicolet Scientific .....	176
<b>DATA COMMUNICATIONS EQUIPMENT</b>	
<b>COMMUNICATIONS CHIPS</b>	
Codec Chip Siemens .....	158
<b>COMMUNICATIONS INTERFACES</b>	
Communications Port Sharing Unit Lion Systems Developments .....	182
<b>COMMUNICATIONS MONITORS</b>	
Communications Monitor Dynatech Data Systems .....	170
<b>COMMUNICATIONS MULTIPLEXERS</b>	
Programmable Multiplexer Able Computer Technology .....	180
<b>COMMUNICATIONS SYSTEMS</b>	
Network Diagnostic Controller Racal-Milgo Information Systems .....	183
<b>DATA COMMUNICATIONS TEST EQUIPMENT</b>	
Communications Equipment Tester International Data Sciences .....	180
<b>DATA TRANSMISSION EQUIPMENT</b>	
Fiber Optic Transmitter and Receiver Maxlight Optical Waveguides .....	181
Industrial Optical Data Link Amrex .....	169
<b>MODEMS; DATA SETS</b>	
Data Modems Anderson Jacobson .....	174
Omnitac Data .....	168
<b>DATA ACQUISITION AND CONTROL EQUIPMENT</b>	
<b>A-D AND D-A CONVERTERS</b>	
D-A Converter ICs Advanced Micro Devices .....	150

	PAGE
<b>Analog Devices</b> .....	52, 53
Datel Systems .....	160
<b>Harris Semiconductor</b> .....	74, 75
Teledyne Philbrick .....	156
A-D Converter ICs	
National Semiconductor .....	152
A-D Converter Chip System	
Texas Instruments .....	160
<b>ANGLE AND POSITION ENCODERS</b>	
Optical Encoder	
<b>EEL Electronics</b> .....	182
<b>DATA ACQUISITION SYSTEMS</b>	
Data Acquisition Systems	
Adac .....	181
Data Acquisition Modules	
Data Translation .....	177
<b>DATA TRANSFER AND INTERFACE EQUIPMENT</b>	
Analog I/O Boards	
Burr-Brown Research .....	134
Datel Systems .....	134
Frequency Synthesizer Interface	
Rockland Systems .....	174
<b>MONITORING AND CONTROL EQUIPMENT</b>	
Realtime Measurement/Control System	
Analog Devices/Instruments and Systems .....	164
<b>TEST AND MEASUREMENT EQUIPMENT; INSTRUMENTATION</b>	
<b>COUNTERS; TIMERS</b>	
Programmable Remote Time Display	
Moxon .....	179
<b>DATA GENERATORS</b>	
Baud Rate Generator	
California Data .....	177
Clock Generators	
Tau-Tron .....	174
<b>DIGITAL EQUIPMENT TESTERS</b>	
Logic Test Equipment	
<b>Hewlett-Packard</b> .....	100, 101
Logic Board Tester	
<b>Hewlett-Packard</b> .....	62
LSI Board Tester	
<b>Teradyne</b> .....	20, 21
Unibus Monitor	
Three Rivers Computer .....	184
<b>FUNCTION GENERATORS AND SYNTHESIZERS</b>	
Frequency Source	
Berkeley Nucleonics .....	181
Frequency Synthesizer Interface	
Rockland Systems .....	174
<b>INSTRUMENTATION RECORDERS</b>	
Sequence-of-Events Recorders	
Dranetz Engineering Laboratories .....	171
<b>METERS</b>	
Miniature Digital Multimeter	
Heuer Time and Electronics .....	182
<b>OTHER TEST AND MEASUREMENT EQUIPMENT</b>	
PC Board In-Circuit Test System	
Membrain .....	169
Spectrum Analyzer	
Spectral Dynamics .....	175
FFT Analyzer Option	
Nicolet Scientific .....	176
Test Probe	
VIZ Test Instruments/VIZ Mfg .....	179
<b>OTHER PRODUCTS; SERVICES</b>	
<b>EDP ACCESSORIES AND SUPPLIES</b>	
Rolls and Tapes	
<b>Eastern Specialties</b> .....	182
Data Security Modules	
<b>Motorola Government Electronics</b> .....	97
Video Intrusion Detector	
Video Tek .....	173
Modular Desks	
Scientific-Atlanta/Optima .....	176
<b>EDUCATION</b>	
Seminars	
<b>Integrated Computer Systems</b> .....	159

	PAGE
<b>EMPLOYMENT OPPORTUNITIES</b>	
Employment Opportunity	
<b>Litton Systems/Amecon</b> .....	189
<b>EQUIPMENT BUYING, SELLING, AND LEASING</b>	
Distributor	
<b>Radgo</b> .....	181
<b>MARKET REPORTS</b>	
Market Reports	
<b>Frost and Sullivan</b> .....	190
<b>OTHER NONDIGITAL PRODUCTS</b>	
Z Users Group	
Jon D. Roland .....	118
<b>PRODUCTION AND ASSEMBLY EQUIPMENT</b>	
Wire-Wrapping Tools	
<b>Vector Electronics</b> .....	172
<b>PUBLICATIONS</b>	
Books	
<b>Blacksburg Continuing Education Series</b> .....	161

	PAGE
<b>Van Nostrand Reinhold</b> .....	163
<b>SOFTWARE</b>	
Software	
<b>S &amp; H Computer Leasing</b> .....	188
Software Systems	
Advanced Computer Techniques .....	168
Microcomputer Software	
Panatec .....	142
Processor Innovations .....	118
Microprocessor Software	
Dann McCreary .....	120
Motorola Semiconductor Products/ Micro Systems .....	118
Technical Systems Consultants .....	120
Assembler	
Step Engineering .....	173
Disc Operating Systems	
IMSAI Manufacturing .....	142
Vector Graphic .....	142
Interactive Graphics Operating System	
Computervision .....	167

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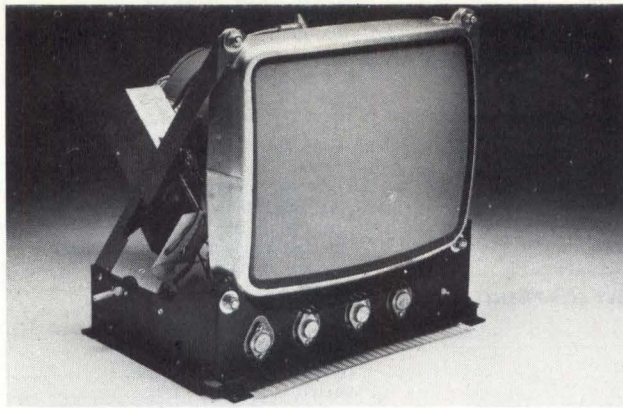
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**CIRCLE 109 ON INQUIRY CARD**

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## ADVERTISERS' INDEX

acdc electronics .....	12, 13
A. D. Data Systems, Inc., a subsidiary of Techtran Industries, Inc. ....	188
Advanced Electronics Design .....	143
Advanced Micro Computers .....	116, 117
Advanced Micro Devices .....	56, 57
Alpha Micro .....	112, 113
Alpha Power, Inc. ....	183
Amecon Div., Litton Systems, Inc. ....	189
Ampex Memory Products, Inc. ....	49
Anadex Corp. ....	15
Analog Devices, Inc. ....	52, 53
Applied Digital Data Systems, Inc. ....	133
Audiotronics, Video Display Div. ....	103
Aydin Controls .....	187
BEI Electronics, Inc. ....	182
Belden Corp. ....	180
Bergquist Co. ....	176
Bill Godbout Electronics .....	173
Blacksburg Continuing Education Series .....	161
Bulova Watch Co., Inc. ....	174
Chrislin Industries .....	171
Citizen America Corp. ....	191
Computer Design Publishing Corp. ....	192
Computer Labs, Inc. ....	179
Computer Products, Inc. ....	102
Computer Technology .....	170
Conrac Corp. ....	139
Control Products Div., Amerace Corp. ....	165
Data Electronics, Inc. ....	40, 41
Data Printer Corp. ....	177
Dataram Corp. ....	95
Data Systems Design, Inc. ....	11
Deltec Corp. ....	172
Digital Electronics Corp. ....	149
Digital Equipment Corp. ....	16, 17
Digital Microsystems .....	23
Digital Research & Engineering .....	178
Eastern Specialties Co., Inc. ....	182
Electronic Devices, Inc. ....	178
Electronic Memories & Magnetics Corp., EMM/CSD/OEM Systems Div. ....	119, 121
Etatech, Inc. ....	43
Ex-Cell-O Corp., Remex Div. ....	99
Fairchild Semiconductor Corp., Operations Div. ....	76
Floating Point Systems, Inc. ....	51
Frost & Sullivan, Inc. ....	190
Fujitsu America, Inc. ....	137
Futuredata Computer Corp. ....	18
Grayhill, Inc. ....	192
Grinnell Systems, Inc. ....	38
Harris Semiconductor Corp. ....	74, 75
Hewlett-Packard Co. ....	35-37, 62, 100, 101
Houston Instrument, Div. of Bausch & Lomb .....	Cover III
Infoton Corp. ....	84
Integrated Computer Systems, Inc. ....	159
Intel Corp. ....	54
Intelligent Systems Corp. ....	58, 190
Interface Mechanisms, Inc. ....	138
International Data Sciences .....	180
C. Itoh Electronics, Inc. ....	120, 157
Kennedy Co. ....	1



La Vezzi Machine Works, Inc. ....	181
3M Company .....	105
Maine Manufacturing Co. ....	170
MDB Systems, Inc. ....	169
Microcomputer Systems Corp. ....	141
Microdata Corp. ....	109
Mohawk Data Sciences Corp. ....	64
Motorola, Inc., Government Electronics Div. ....	97
Semiconductor Products, Div. ....	5, 24, 25, 27, 60, 61, 155
NEC Information Systems, Inc. ....	59
Okidata Corp. ....	4
Perkin-Elmer Corp., Terminals Div. ....	30, 31
Interdata Div., ....	135
Permag Corp. ....	191
Pertec Computer Corp., iCOM Div. ....	151
Pittman Corp. ....	167
Pioneer Magnetics ....	108
Plessey Trading Corp., Microsystems Div. ....	93
Peripherals Div. ....	29
Power One, Inc. ....	7
Practical Automation, Inc. ....	128
Process Computer Systems, Inc. ....	107
Pro-Log Corp. ....	Cover IV
Qantex, Div. of North Atlantic Industries ....	175
Radgo, Div. of Adgo, Inc. ....	181
Ramtek Corp. ....	126
Raymond Engineering Corp. ....	142
Rockwell International, Microelectronics Div. ....	131
Rolm Corp. ....	115
S & H Computer Leasing, Inc. ....	188
Shugart Assoc. ....	8, 9
Signetix Corp. ....	44, 45
Spectronics Corp. ....	168
Stacoswitch, Inc. ....	184
Sweda International, OEM Products Div. of Litton Industries ....	171
Systems Engineering Laboratories, Inc. ....	123
Systems Research Laboratories, Inc., Electronic Image Systems Div. ....	27
Tally Corp. ....	2
Teletype Corp. ....	32
Teradyne, Inc. ....	20, 21
TEXAS INSTRUMENTS INCORPORATED, Components Div. ....	46
Texas Instruments Supply Co. ....	129
Union Carbide Corp. ....	183
Van Nostrand Reinhold Co., a div. of Litton Industries ....	163
Vector Electronics Co. ....	172
Vector General, Inc. ....	125
Western Peripherals Div., WESPERCORP .....	Cover II
Xerox Corp., Diablo Div. ....	153
Zenith Radio Corp., CRT Display Engineering Div. ....	111

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### SUBJECT INDEX

#### COMPONENTS

##### Buses

Implications of Busing for Cellular Arrays, F. Heutink ..... Nov 74, p 95

##### Cables

Choosing the Correct Flat Cable for High Speed Logic Circuits, S. Sullwold ..... Dec 75, p 97

POS Cable: A Design Study, R. D. Sheth ..... Nov 75, p 106

##### Circuit Protectors

Applying Magnetic Circuit Breakers in Digital Circuits, D. S. Tall ..... Nov 78, p 132

Digital Input Units Isolate Microcomputers From Industrial Level Voltages, C. R. Teeple ..... Nov 78, p 142

Overload-Protector/Fault-Indicator Circuit, NASA ..... May 77, p 130

Protecting Minicomputers From Power Line Perturbations, R. M. Teets June 76, p 99

##### Connectors

Computer Connector Saves Space and Cuts Cost, P. K. Winklebleck .. Dec 78, p 106

Flexible-Cable/Connector Simplifies PCB Wiring, J. Knudson ..... Aug 75, p 90

Other Performance Factors in PC Board Connectors, C. Ladstatter .. Nov 74, p 112

##### Data Converters

Binary/BCD-to-ASCII Data Converter, NASA ..... Nov 77, p 110

A Cellular Array for Integer and Fractional BCD-Binary Conversion, J. G. Bredeson ..... May 74, p 104

Conversion of Resolver or Synchro Trigonometric Outputs to Digital Data, E. L. Griffin ..... Oct 74, p 105

Digital-to-Analog Converters: Some Problems in Producing High-Fidelity Systems, R. P. Talambiras .....	Jan 76, p 63
Highly Stable Analog-to-Digital Converter, NASA .....	Jan 77, p 106
Hybrid D-A Implementation of Digital Filters, NASA .....	Apr 78, p 162
Interfacing the Teletypewriter—Part 1: A-D and D-A Converters, M. Klafish .....	June 74, p 94
Interpretation of Data Converter Accuracy Specifications, E. L. Zuch ..	Sept 78, p 113
Low Cost A-to-D Conversion During Microcomputer Idle Time, H. A. Raphael .....	Mar 77, p 112
Microprocessor-Based Interface Converts Video Signals for Object Tracking, K. Lubinski, et al .....	Dec 77, p 81
Noise Effects on Analog-to-Digital Conversion Accuracy—Part 1, B. M. Gordon .....	Mar 74, p 65
Part 2, B.M. Gordon .....	Apr 74, p 137
A 1½ Level On-Chip-Decoding Bubble Memory Chip Design, NASA ..	Feb 77, p 116
Programmable Handheld Calculator Computes Digital-to-Analog Converter Errors, P. Prazak .....	June 78, p 122
Specifying Settling Time for Current-Switched D-A Converters .....	Mar 74, p 112

#### Enclosures

Steel Wire Frames Reduce Computer Equipment Costs .....	Feb 78, p 130
Structural Foam for Computer Equipment Enclosures, W. Victor and P. LeBlanc .....	Oct 78, p 120

#### Power Converters

Majority-Voted Logic Fail-Sense Circuit, NASA .....	Mar 78, p 130
Microprocessor/Microcomputer Application Contest, Second Prize—A Microprocessor-Controlled Three-Phase Power Inverter, P. van der Gracht and K. Mauch .....	May 77, p 120

#### Power Sources and Regulators

Protecting Minicomputers From Power Line Perturbations, R. M. Teets ..	June 76, p 99
Specifying and Selecting Uninterruptible Power Supply Systems, J. A. Camuso .....	July 74, p 63
Static UPS: Systems—Configurations and Inverter Specifications, J. N. Holscher .....	July 74, p 65
Application Case Histories, C. G. Helmick .....	July 74, p 71
Switching Power Supplies: Design Considerations, E. R. Hnatek .....	Feb 77, p 89
Switching Power Supplies: Specification Criteria, J. H. Burens .....	May 77, p 91
Switching Regulator-Noise Suppression Techniques, E. R. Hnatek .....	Jan 75, p 94
Universal Switching Regulator Diversifies Power Subsystem Applications, R. J. Apfel and D. B. Jones ..	Mar 78, p 103
Versatile, Analog-to-Digital Power-Regulator Controller, NASA .....	Feb 75, p 104

#### Relays

Interfacing the Teletypewriter—Part 2: Programming Remote Relays, Solenoids, and Other Power Devices, M. Klafish .....	July 74, p 100
--	----------------

#### Step Motors

An Automated Testing Procedure for Step Motor Simulation and Validation, R. E. Knoerzer .....	June 75, p 84
Digital Display of Stepper Motor Rotation, H. Lo .....	Apr 78, p 147
Selecting and Applying Stepping Motors in Computer Peripheral Equipment, S. Davis .....	May 75, p 141
Small Stepping Motors Meet Varied Application Requirements, W. Riggs .....	Feb 78, p 120

#### Switches

Field-Effect Transistors as Analog Switches, S. Givens .....	June 74, p 106
Solid-State Analog Switch Matrix Replaces Relay and Crossbar Selectors, R. W. Embley .....	Nov 75, p 112

#### Synchros and Resolvers

Digital Measurement of Shaft Position: Synchros and Resolvers or Encoders, S. Davis .....	Feb 76, p 50
---	--------------

### COMPUTERS

#### Aerospace

Architecture of Aerospace Computer Simplifies Programming, H. C. Kancler .....	May 76, p 159
Design Considerations for Aerospace Digital Computers, J. Jurison, et al	Aug 74, p 113
Organization of a Microprogrammed Aerospace Computer, G. C. Vandling .....	Feb 75, p 65

#### Array Processors

Array Processor Provides High Throughput Rates, W. R. Wittmayer .....	Mar 78, p 93
---	--------------

#### Auxiliary Units

An Asynchronous Arbiter Resolves Resource Allocation Conflicts on a Random Priority Basis, K. S. Højberg .....	Aug 77, p 120
--	---------------

#### Communications Processors

Programmable Multiline Communications Processor Provides Front-End Flexibility, K. T. Coit .....	May 77, p 99
--	--------------

#### Design Systems

A Formal Design Language for Digital Systems, R. Crall .....	Nov 74, p 103
Logic Design and Its Recent Development—Part 6: Computer-Aided Logic Design, S. Y. H. Su .....	Feb 74, p 77

#### Microcomputers

See MICROCOMPUTERS

#### Microprocessors

See MICROPROCESSORS

## Microprogramming

- Evolution of Microprogrammed Input/Output Processing in One Processor Family, R. Vahlstrom and M. Malone ..... Jan 76, p 98
- Microprogramming: A General Design Tool, R. Jaeger ..... Aug 74, p 150
- Microprogramming in an Integrated Hardware/Software System, J. V. Sell ..... Jan 75, p 77
- Organization of a Microprogrammed Aerospace Computer, G. C. Vandling ..... Feb 75, p 65

## Mini- and Small Computers

See **MINICOMPUTERS**

### Multiple Processors

- Design Motivations for Multiple Processor Microcomputer Systems, G. Adams and T. Rolander ..... Mar 78, p 81
- Designing Interrupt Structures for Multiprocessor Systems, R. Jaswa .. Sept 78, p 101
- Hardware Allocation of Data System Resources, G. L. Anderson and K. Bartlett ..... July 74, p 89
- Multiple Processor Minicomputer Systems—Part 1: Design Concepts, B. H. Liebowitz ..... Oct 78, p 87
- Part 2: Implementation, B. H. Liebowitz ..... Nov 78, p 121
- One-Step Programmable Arbiters for Multiprocessors, K. S. Højberg ..... Apr 78, p 154
- Time Slicing Offers an Alternative to Multiprocessor Systems, J. Pathak .. July 77, p 95

### Simulation and Analysis

- Computer Queuing Analysis on a Handheld Calculator, R. Zussman .. Nov 77, p 85
- Computer Simulation on a Pocket Calculator, R. Zussman ..... May 77, p 105
- Computer Simulation Program for a Second Generation Handheld Calculator, R. Zussman ..... Mar 78, p 116
- Learning Networks Improve Computer-Aided Prediction and Control, R. L. Barron ..... Aug 75, p 65
- Matrix Computations Forecast Computer Reliability, R. Sharan ..... Aug 76, p 95
- Procedure Evaluates Computers for Scientific Applications, L. Wolin .... Nov 76, p 93

### General

- Analyzing Computer Technology Costs—Part 1: Development and Manufacturing, M. Phister ..... Sept 78, p 91
- Part 2: Maintenance, M. Phister .... Oct 78, p 109
- Associative Processors: A Panacea or a Specific? L. C. Higbie ..... July 76, p 75
- Building Today's Technologies Into a Large-Scale Time-Sharing System, G. F. Atterbury and G. F. Adams Sept 75, p 79
- Diagnostic Structures and Formats for Complex Computer Systems, W. S. Holderby ..... May 75, p 148
- Digital Simulator Replaces Analog Portion of Hybrid Computer, B. R. Gilbert and M. J. Morse ..... Apr 76, p 91
- A Distributed Computer System for Laboratory Automation, G. A. Korn ..... June 77, p 177

- Hardware Allocation of Data System Resources, G. L. Anderson and K. Bartlett ..... July 74, p 89
- An Introduction to Vector Processing, P. M. Johnson ..... Feb 78, p 89
- Multivariable Function Generation for Hybrid Computers, A. I. Rubin Feb 76, p 99
- Top-Down Approach to LSI System Design, H. D. Caplener and J. A. Janku ..... Aug 74, p 143
- Top-Down Design Streamlines Digital System Projects, M. L. Fichtenbaum Sept 76, p 77
- Trends in Computer Hardware Technology, D. A. Hodges ..... Feb 76, p 77
- Verbal Communication System Enhances Computer/Student Interaction, M. J. Freeman and G. P. Mulkowsky ..... Jan 76, p 81
- Virtual Memory Design Reduces Program Complexity, J. E. Requa ..... Jan 78, p 97

## CONTROL AND AUTOMATION

### Data Acquisition

- Computer Systems Simulate Braking Conditions for 300-Car Trains ..... Oct 78, p 52
- Computers Overcome Tedium of Manual Monitoring in Data Acquisition and Control ..... July 78, p 54
- Designing a Microprocessor-Based Terminal for Factory Data Collection, W. S. Holderby ..... Mar 77, p 81
- Low Cost Data Acquisition System Using Standard DIPs, J. F. Munn .. May 78, p 200
- Low Cost Pressure-Data Encoder, NASA ..... Feb 78, p 134
- Maneuvers of Dogfighting Pilots Displayed to Instructors Under Computer Control ..... May 74, p 56
- Microprocessor-Controller Torque Certification System Has Capacity for 4096 Tool Stations ..... June 74, p 60
- Microprogramming for Real-Time Data Acquisition, NASA ..... Nov 77, p 112
- Multiple-Computer Hierarchy Tests 1975 Carburetors ..... Oct 74, p 56
- Programmable Calculators Control Data Acquisition Systems, J. Estes Oct 75, p 73

### Environmental

- Air Pollution Monitored By Microprocessor Based Instruments ..... Oct 78, p 56
- Aircraft Landing/Take-Off Noise Levels Identified and Monitored by Computer Systems ..... Sept 77, p 76
- Multiple-Microcomputer Building Control System Reduces Both Electrical and Employee Costs ..... May 78, p 50
- Reliability of Energy Control Center Is Proven By Time ..... Apr 76, p 54
- Weather Study System Incorporates High Capacity Semiconductor Memories ..... Oct 77, p 77

### Inventory

- Automated Updating Gives Security Traded Firm Constant View of Inventory ..... Aug 77, p 52

Computer-Directed Warehouse System Relieves Personnel by Locating Parts and Maintaining Paperwork ..... Oct 77, p 54

### Laboratory

Chromatography System Provides Continuous Analysis of Gas Supply ..... June 77, p 67

Microprocessor-Controlled Instrument Monitors Exhaust Gas Temperatures ..... July 76, p 66

### Manufacturing/Production

Data Acquisition System Automatically Monitors Steel Rolling Mill .. June 77, p 62

DDC Automates Chemical Reactor at Pharmaceutical Manufacturing Plant ..... Sept 75, p 46

Dual-Computer System Provides Continuous Control of Cement Plant .. July 76, p 54

Microcomputer-Controlled Laser Burns Labels on Containers ..... Oct 77, p 66

Microprocessor Solves Batch Mixing Problems for Supplier of Bread Ingredients ..... Dec 76, p 48

Production Processes Monitored By Microprocessor Controlled Non-contact Inspection Systems ..... Sept 78, p 55

Real-Time Computer Control of Butadiene Purification Increases Production, Improves Quality ..... Nov 74, p 56

Record-Size Control System Provides Process Security in High Energy Munitions Manufacturing Plant ..... Apr 75, p 56

System Measures and Sorts Green Lumber at 38 Boards/Min with 99.5% Accuracy ..... July 74, p 52

### Medical

Program and Extensive Data Base Alert Physicians to Possible Adverse Drug Reactions ..... June 77, p 72

Real-Time Medical Information System Automatically Updates All Data on Hospital Patients ..... Mar 75, p 48

### Test

Automated Laboratory Testing System Reports Results Verbally ..... Apr 77, p 44

Automated Test Equipment Functions Without Conventional Test Generation/Analysis Devices ..... Jan 75, p 56

Automated Test Systems Assure Adherence to Government Standards in Automotive Manufacturing ..... Feb 74, p 42

Computers Overcome Tedium of Manual Monitoring in Data Acquisition and Control ..... July 78, p 54

Quality Control System Tests Automotive-Exhaust Catalytic Converters ..... Feb 75, p 52

Versatile System Tests Electronic Components Automatically ..... Sept 74, p 54

### Transportation

Computer Complex Automates and Protects Rapid Transit System ..... Oct 76, p 54

Computer Systems Simulate Braking Conditions for 300-Car Trains ..... Oct 78, p 52

Microprocessor-Controlled System Diagnoses Tugboat Engine Malfunctions ..... June 76, p 58

Program Flexibility of Microprocessor-Controlled Elevators Enables Easy System Modifications ..... Sept 77, p 54

Real-Time Computer Adjustment of Traffic Light Sequencing Eases Vehicle Congestion ..... June 75, p 40

### Utilities

Automatic, Interactive Graphic Systems Maintain Pipeline Network Maps ..... Apr 77, p 58

Computerized Ripple Control Eliminates Excessive Drain On Electric Utility Supply ..... Mar 77, p 55

Efficiency of Electric Power Generation and Distribution Improved by Energy Management System ..... July 77, p 48

Redundant Computer Subsystems Monitor and Control Gas Distribution ..... Feb 77, p 46

Single-Board Microcomputers Monitor and Control Hydroelectric Plant With Remote Supervision .... Mar 78, p 64

Turbine-Generator Power Systems Operate Under Direct Digital Control ..... July 75, p 50

### General

Benefits of Localized Control with Microcomputers, A. D. Harmala .... May 75, p 59

Brooklyn Firefighting Units Respond to Computer-Aided Dispatching System ..... Nov 77, p 48

Cargo Vessel Load Stresses Simulated by Multipoint Computer Systems ..... Dec 77, p 48

CMOS Logic Modules for Industrial Control, M. Cohen ..... Mar 74, p 50

The Computer in Machine Tool Control Today, and Its Future ..... Aug 78, p 50

Computerized Graphic Display System Aids in Automatic Design of Tractor Parts ..... July 76, p 64

Computer Network Automates And Controls Mailgram Service ..... Aug 74, p 72

Computer Process Control Around the World, S. F. Shapiro ..... Nov 75, p 58

Computers Oversee All Activities of Tower Restaurant ..... May 77, p 50

Control and Instrumentation Conference Emphasizes Industrial Applications of Microprocessors ..... June 78, p 64

Custody Transfer of Crude Oil Automated by Minicomputer ..... June 76, p 66

Decision-Making With Flags in Process Control, L. F. Donaghey, et al Dec 76, p 50

Digital Control at WESCON ..... Nov 78, p 52

Digital Measurement of Shaft Position: Synchros and Resolvers or Encoders, S. Davis ..... Feb 76, p 50

Digital Technology Enables Robots To "See," S. F. Shapiro ..... Jan 78, p 43

Direct Numerical Control: Will It Be in Your Future? ..... Aug 75, p 42

A General-Purpose Interface for Industrial Process Control, F. J. Trudo .....	Dec 74, p 78
Hardware/Software for Process Control I/O, A. D. Marathe and A. K. Chandra .....	Mar 78, p 122
High Speed Laser System Welds Terminals of Miniature Relays Under Microcomputer Control .....	Dec 78, p 50
Instrument Industry Recognizes Digital Electronics—Almost, S. F. Shapiro .....	Jan 77, p 50
International Industrial Computer Systems Workshop Summary .....	Jan 76, p 50
Learning Networks Improve Computer-Aided Prediction and Control, R. L. Barron .....	Aug 75, p 65
Microcomputer Controls Eye's Focus and Measures Refractive Error .....	Apr 78, p 64
Microcomputers Replace Gas Station Attendants .....	Aug 76, p 57
Microprocessors and LSI Devices Are Prime Contributors to Design of Automatic Bowling Scorer .....	Sept 76, p 50
Microprogramming Simplifies Control System Design, R. Kenny .....	Feb 75, p 96
The Mini: Efficient Alternative to Large Computer Control, S. Gaal .....	Jan 74, p 46
Minicomputer Control Eases Mapping Tedium .....	Feb 78, p 56
1974 International Machine Tool Show, In Retrospect .....	Dec 74, p 46
Professional Group Conference Stresses Microprocessor Applications for Process Control, S. F. Shapiro .....	May 76, p 84
The Role of Microcomputers in Robotics, K. Goksel and E. A. Parrish, Jr. ....	Oct 75, p 56
Self-Checking Tandem Minicomputers Maintain Security System in High-Rise Office Building .....	Mar 76, p 42
Social/Economic/Governmental Considerations of Automation, S. F. Shapiro .....	Dec 75, p 50
Television Network Automated by Minicomputer-Controlled Channels .....	Nov 76, p 50
Training Lab Doubles as Control System Breadboarding Unit .....	Apr 74, p 50

## DATA COMMUNICATIONS

### Data Transmission

Code Conversion Techniques for Digital Transmission, S. Ghosh .....	Aug 78, p 103
Data Compaction in Computer Systems, Y. Dishon .....	Apr 77, p 85
Hardware Considerations for High Level Data Link Control Communications, S. B. Cooper .....	Mar 75, p 81
Improved CRC Technique Detects Leading and Trailing 0's in Transmitted Data Blocks, H. C. McKee ..	Oct 75, p 102
Integrating Medium Speed Modems Into Communications Networks, K. Krechmer .....	Feb 78, p 101

Serial Communication Protocol Simplifies Data Transmission and Verification, J. G. Fletcher .....	July 78, p 77
Two-Step Procedure Improves CRC Mechanism, P. J. Fortune .....	Nov 77, p 120

### Interfaces

Computer Interface-Timing Control Logic, T. O. Anderson .....	Feb 74, p 96
Data Transfer with ASCII Eliminates Computer Interface Problem, W. Nadler .....	June 75, p 74
Design Constraints for a UART-Based Minicomputer Communications Interface, A. Hirsch .....	June 77, p 167

### Multiplexers

An Asynchronous Time-Division Multiplexing System, C. T. Pardoe and R. L. Appel .....	July 75, p 110
Dynamic Multiplexing Applications, J. E. Buckley .....	Nov 76, p 14
Multiplexer System Reduces Cost of Terminal Interfacing, A. Lesea and N. Urkumyan .....	Aug 77, p 109
A Time Division Multiple Access System for Digital Communication, D. G. Willard .....	June 74, p 79

### Networks

Computerized Voice Network Control, J. E. Buckley .....	Aug 77, p 12
Data Network Response, J. E. Buckley .....	Jan 77, p 14
Functional Approach to Information Network Design, H. B. Becker .....	May 74, p 83
Intelligent Networks, J. E. Buckley .....	Dec 74, p 10
Microcomputers Decentralize Processing in Data Communications Network, D. J. Mueller .....	Oct 77, p 81
Network Design Criteria, J. E. Buckley .....	May 75, p 14
Network Node Criteria, J. E. Buckley .....	Dec 75, p 10
A New Approach to Network Storage Management, J. E. Thornton, et al .....	Nov 75, p 81
Satellite Business Systems, J. E. Buckley .....	June 76, p 10
Shared User Networks, J. E. Buckley .....	June 77, p 11

### Regulations

Certification 1977, J. E. Buckley .....	Dec 77, p 11
Certification Update, J. E. Buckley ..	July 78, p 12
Communication Act of 1978, J. E. Buckley .....	Nov 78, p 14
Implication of the Communications Reform Act, J. E. Buckley .....	Sept 76, p 14
Interconnection Certification, J. E. Buckley .....	Jan 76, p 14
1956 Consent Decree—History and Implications, J. E. Buckley .....	Sept 78, p 14
Private Line Tariff Revisions, J. E. Buckley .....	July 76, p 10

### Services

AT&T's Digital Transmission Service, J. E. Buckley .....	June 74, p 10
Competitive Dialed Services, J. E. Buckley .....	Mar 76, p 11
Data Communications Consultants, J. E. Buckley .....	Oct 77, p 10

In-WATS System Access, J. E. Buckley .....	Aug 76, p 16
Leased Communications Services, J. E. Buckley .....	Aug 75, p 12
Possible 1977 WATS, J. E. Buckley ..	Mar 77, p 12
Ramifications of the Revised WATS Tariff, J. E. Buckley .....	July 77, p 11
Switched Communications Services, J. E. Buckley .....	June 75, p 10
Switched Network Service Alternatives, J. E. Buckley .....	Apr 78, p 14
Trans-Canada Datapac, J. E. Buckley	Apr 75, p 10
Unbundled Communications Services, J. E. Buckley .....	July 75, p 11
WATS Past and Present, J. E. Buckley	Feb 77, p 14

### Software

Communications Software: Application Overview, J. E. Buckley .....	Sept 74, p 16
Communications Software: Functional Considerations, J. E. Buckley .....	Oct 74, p 12

### Systems

Communication System Security, J. E. Buckley .....	Mar 75, p 10
Computerized PBX Systems, J. E. Buckley .....	May 76, p 14
Multi-Vendor Information Systems, J. E. Buckley .....	Aug 78, p 11
Packet Switching, J. E. Buckley .....	Apr 74, p 10
"Pacuit" Switching Combines Two Techniques in One Network, J. de Smet and R. W. Sanders .....	June 76, p 83
Programmable Multiline Communications Processor Provides Front-End Flexibility, K. T. Coit .....	May 77, p 99
Remote Memory Systems and Applications, J. E. Buckley .....	Oct 78, p 11
Wideband Communication System Improves Response Times, J. F. Wanner .....	Dec 78, p 85

### Test

Implementation of a Parallel Cyclic Redundancy Check Generator, K. M. Helness .....	Mar 74, p 91
Telecommunications Diagnostics, J. E. Buckley .....	Feb 74, p 10
Telecommunications Systems Measurements, J. E. Buckley .....	Mar 74, p 12

### General

Asynchronous Timing Error Characteristics, J. E. Buckley .....	Feb 78, p 12
Automatic Dialing for Computer Communications, T. J. McShane ..	Apr 74, p 146
Communications Code Compatibility, J. E. Buckley .....	May 74, p 11
Communications Conference Shows Impact of Digital Technology .....	Aug 78, p 14
Communications Traffic Analysis, J. E. Buckley .....	June 78, p 14
Computer-Aided Network Design, J. E. Buckley .....	Apr 77, p 18
Computer Communications Inquiry, J. E. Buckley .....	Oct 76, p 10

Continuous-Phase Frequency-Shift-Keyed Generator, NASA .....	Feb 77, p 118
Design Technique for a Near-Field Communication System, A. A. Smith, Jr .....	Sept 74, p 85
Dial'd Digital Data Channels, J. E. Buckley .....	Apr 76, p 10
Domestic Communications Satellite System, J. E. Buckley .....	Oct 75, p 15
Generation of Key in Cryptographic System for Secure Communications, NASA .....	July 76, p 114
High Speed Data Word Monitor, NASA .....	Sept 76, p 110
IBM Protocols—Part 1: BSC, J. E. Buckley .....	Jan 75, p 12
Part 2: SDLC, J. E. Buckley .....	Feb 75, p 14
Information Systems Review—And Epilogue, J. E. Buckley .....	Dec 78, p 14
Local Modems, J. E. Buckley .....	Jan 78, p 14
Local System Access, J. E. Buckley ..	Dec 76, p 20
Management Automation Applications, J. E. Buckley .....	May 78, p 11
Manchester Transition Tracking Loop, NASA .....	Oct 77, p 124
Microcomputer Converter, J. E. Buckley .....	Feb 76, p 12
Non-Communications Programming Acronyms, J. E. Buckley .....	Nov 74, p 14
Office Automation, J. E. Buckley .....	Nov 77, p 14
Remote Batch vs Interactive Processing, J. E. Buckley .....	Sept 75, p 10
Remote Data Terminal Selection, J. E. Buckley .....	Aug 74, p 10
Synchronous Timing Error Characteristics, J. E. Buckley .....	Mar 78, p 14
System Environmental Factors, J. E. Buckley .....	Sept 77, p 18
System Installation Criteria, J. E. Buckley .....	Nov 75, p 14
Telephone Controllers, J. E. Buckley	Jan 74, p 11
Terminal Storage Systems, J. E. Buckley .....	May 77, p 11
Terminals: Human Factor Considerations, J. E. Buckley .....	July 74, p 8

## DIGITAL CIRCUITS

### Arithmetic

External Arithmetic Processors, S. Smith .....	Dec 78, p 144
A Multivibrator Using RC-Coupled Cascade Stages as a Ring Counter, S. Chang and P.-L. Lam .....	May 74, p 120
Operation of Programmable Frequency Dividers, A. C. Erdman ..	May 74, p 110
State-of-the-Art in High Speed Arithmetic Integrated Circuits, S. Waser	July 78, p 67

### Custom Circuits

Custom Integrated Circuits: A Viable Alternative for Low to Intermediate Volume Applications, E. R. Garen	July 78, p 156
Semicustom Integrated Circuits—The Do-It-Yourself LSI Chips, E. R. Garen .....	Sept 77, p 148



## Memory

- Designing Minicomputer Memory Systems with 4-Kilobit n-MOS Memories, D. Brunner ..... July 75, p 61
- Magnetic Bubble Memory Devices and Applications, E. R. Garen .... Feb 78, p 164
- Multiple-Word Buffering for Disc Controllers with Bipolar FIFO Memory, K. Rallapalli ..... Dec 77, p 73
- Using p/ROMs as Logic Elements, D. C. Wyland ..... Sept 74, p 98

## Technologies

- Advances in CMOS Device Technology, A. Nguyen-Huu ..... Jan 75, p 87
- The Changing World of Advanced LSI ..... Nov 76, p 134
- Charge-Transfer Devices—Part 1: The Technologies, E. R. Garen ..... Nov 77, p 146
- Part 2: CCD Memories, E. R. Garen ..... Dec 77, p 130
- Part 3: Diverse Uses of CTDs for Analog, Digital, and Optical Applications, E. R. Garen ..... Jan 78, p 154
- CMOS on Sapphire, S. Smith and E. R. Garen ..... Sept 78, p 194
- Integrated Injection Logic—A Technology Status Report, E. R. Garen ..... June 78, p 162
- Technology Status Report on Recent NMOS Processes, S. Smith and E. R. Garen ..... Aug 78, p 160

## General

- Digital Second-Order Phase-Locked Loop, NASA ..... Nov 75, p 118
- DMA Controller Capitalizes on Clock Cycles to Bypass CPU, J. Nissim .. Jan 78, p 117
- Have the LSI Parts You Buy Been Thoroughly Tested? E. R. Garen .. Oct 77, p 152
- A Hybrid General-Purpose Bit Synchronizer, NASA ..... Apr 76, p 126
- Impact of LSI on Terminal Architecture, P. G. Cook and T. B. Cheek Nov 76, p 103
- The Impact of VLSI Upon Computer Architecture, S. Smith and E. R. Garen ..... Oct 78, p 200
- A Low Cost, Crystal-Controlled Oscillator Design, R. A. Mancini ..... Jan 74, p 94
- Master Calendar-Clock Serves Multiple Minicomputers, R. Piankian .... Oct 78, p 156
- Monolithic Data Conversion Devices—Part 1: Digital-to-Analog Converters, E. R. Garen, et al ..... Mar 78, p 152
- Part 2: Analog-to-Digital Converters, E. R. Garen ..... Apr 78, p 188
- Part 3: Auxiliary Integrated Circuits, E. R. Garen ..... May 78, p 236
- Monolithic Processors, H. Schmid .... Oct 74, p 87
- Synchronizer for Random Binary Data, NASA ..... July 76, p 118
- Using a Calculator Chip to Extend a Microprocessor's Capabilities, P. H. Stakem ..... Sept 75, p 98
- VMOS Peripheral Drivers Solve High Power Load Interface Problems, L. Shaeffer ..... Dec 77, p 90

- Voltage-Offset Reduction in Data Transmitters, NASA ..... July 78, p 112

## DIGITAL MATHEMATICS

### Arithmetic

- Algorithm for Computing Logarithms and Antilogarithms, M. Clugudean July 74, p 106
- An Algorithm for Nonrestoring Division, S. Sanyal ..... May 77, p 124
- Arithmetic Logic Unit Design for an LSI Minicomputer, R. Blacksher .... Apr 75, p 96
- Carrying Out Division by Addition Reduces Hardware Complexity, N. T. Simopoulos ..... June 75, p 80
- Hardware Multiplication Techniques for Microprocessor Systems, B. Parasuraman ..... Apr 77, p 75
- Numerical Interpolation for Microprocessor-Based Systems, T. A. Seim ..... Feb 78, p 111
- Shortcut to Logarithms Combines Table Lookup and Computation, S. Shi ..... May 76, p 184

### Digital Logic and Switching Theory

- Complementary MOS Four-Phase Logic Circuits, NASA ..... Sept 74, p 110
- Congruent Partitioning and Network Synthesis, J. R. Logan ..... Dec 74, p 53
- Eliminating Glitches from One-Shots in Logic Systems, J. Carroll ..... Sept 75, p 104
- Exclusive-OR Frequency Multiplier, NASA ..... June 78, p 130
- Index-Register Logic Saves One Instruction Per Loop, D. Mandelbaum Oct 75, p 98
- Logic Design and Its Recent Development—Part 5: Fault Diagnosis in Digital Networks, S. Y. H. Su ..... Jan 74, p 87
- Part 6: Computer-Aided Logic Design, S. Y. H. Su ..... Feb 74, p 77
- Mixed Logic Leads to Maximum Clarity with Minimum Hardware, F. Prosser and D. Winkel ..... May 77, p 111
- Software Analyses for Combinatorial Logic, J. L. Pokoski ..... June 78, p 113

### Information Theory

- An Asynchronous Arbiter Resolves Resource Allocation Conflicts on a Random Priority Basis, K. S. Højberg ..... Aug 77, p 120
- Automatic Error Correction in Memory Systems, B. Rickard ..... May 76, p 179
- Calculating an Error-Checking Character in Software, S. Vasa ..... May 76, p 190
- A Cellular Array for Integer and Fractional BCD-Binary Conversion, J. G. Bredeson ..... May 74, p 104
- Code Conversion Techniques for Digital Transmission, S. Ghosh ..... Aug 78, p 103
- Computer Queuing Analysis on a Handheld Calculator, R. Zussman Nov 77, p 85
- Concatenated Algebraic Decoder, NASA ..... June 78, p 132
- Cyclic Sequence Generator Increases Security of Alarm System, R. Krishnaiyer and J. C. Donovan ..... July 75, p 73

Data Compaction in Computer Systems, Y. Dishon .....	Apr 77, p 85
An Efficient Software Method for Implementing Polynomial Error Detection Codes, J. S. Whiting .....	Mar 75, p 73
Enciphering Data for Secure Transmission, C. H. Meyer .....	Apr 74, p 129
Generation of Key in Cryptographic System for Secure Communications, NASA .....	July 76, p 114
Group Coded Recording Reliably Doubles Diskette Capacity, P. S. Sidhu .....	Dec 76, p 84
Hardware Binary-to-BCD Conversion and BCD Addition, R. A. Bernay ..	Mar 74, p 98
Implementation of a Parallel Cyclic Redundancy Check Generator, K. M. Helness .....	Mar 74, p 91
Improved CRC Technique Detects Erroneous Leading and Trailing 0's in Transmitted Data Blocks, H. C. McKee .....	Oct 75, p 102
Information Preserving Codes Compress Binary Pictorial Data, U. Moilanen .....	Nov 78, p 134
Matrix Computations Forecast Computer Mainframe Reliability, R. Sharan .....	Aug 76, p 95
New Error-Correcting Technique for Solid-State Memories Saves Hardware, G. R. Basham .....	Oct 76, p 110
Parallel CRC Lets Many Lines Use One Circuit, A. K. Pandeya and T. J. Cassa .....	Sept 75, p 87
Predicting Queue Performance on a Programmable Handheld Calculator, R. Zussman .....	Aug 78, p 93
The Serialized Approach to Reading Phase-Encoded Data, A. Wrobel and M. Gray .....	Feb 75, p 77
Simple Encoding Schemes Double Capacity of a Flexible Disc, D. J. Kalstrom .....	Sept 76, p 98
Simple Hardware Approach to Error Detection and Correction, R. C. Montgomery .....	Nov 78, p 109
Single Error Correcting Code Maximizes Memory System Efficiency, S. Sanyal and K. N. Venkataraman	May 78, p 175
Software-Based Single-Bit I/O Error Detection and Correction Scheme, G. M. White .....	Sept 78, p 130
Tradeoffs Among Binary Codes in Magnetic Tape Cassettes, J. J. Pastoriza .....	Jan 76, p 102
Two-Step Procedure Improves CRC Mechanism, P. J. Fortune .....	Nov 77, p 120
Understanding Cyclic Redundancy Codes, R. Swanson .....	Nov 75, p 93
<b>Number Representation and Conversion</b>	
BCD/Binary Conversion with Single IC Cell, M. G. Phadnis and D. Joshi	Dec 78, p 94
A BCD Conversion Technique for Teletypewriter Applications, C. Ellsworth and W. Malloch .....	Dec 74, p 69

A Cellular Array for Integer and Fractional BCD-Binary Conversion, J. G. Bredeson .....	May 74, p 104
General Algorithms for Direct Radix Conversion, W. C. Lanning .....	June 75, p 61
Hardware Binary-to-BCD Conversion and BCD Addition, R. A. Bernay ..	Mar 74, p 98
Self-Checking Number Systems, J. R. Herr .....	June 74, p 85
<b>General</b>	
Another Use for NAND Gates, J. Miles .....	Dec 74, p 84
Applications of Vector Processing, L. C. Higbie .....	Apr 78, p 139
CMOS Enhances Video Display Terminal Design, K. Karstad .....	Sept 74, p 91
Counting Digital Filter, NASA .....	Feb 78, p 132
Design of a Programmable One-Shot Multivibrator, L. Ruggeri .....	Mar 74, p 110
Digitized Video Processing in Real-time, J. Meyn .....	Dec 78, p 104
Exclusive-OR Frequency Multiplier, NASA .....	June 78, p 130
Interfacing Calculator Chips as Microcomputer Preprocessors, W. W. Moyer .....	May 78, p 187
Interval Timer Serves As a Baud Rate Generator, J. Beaston .....	Aug 78, p 112
Single-Chip Speech Synthesizers, S. Smith .....	Nov 78, p 188

## INPUT/OUTPUT

### Bar Code Recognition

Printers and Readers Handshake for Effective Bar Code System, G. Whittaker and W. Sexton .....	Sept 74, p 69
--	---------------

### Character Recognition

Algorithm for a Low Cost Hand Print Reader, A. W. Holt .....	Feb 74, p 85
Electro-Optical Scan Converter Shares Benefits of Conventional Units, N. M. Potey .....	Dec 75, p 75
OCR System Design Benefits from Technological Advances, R. K. Dove .....	Oct 75, p 91

### Controllers

Simplified Floppy-Disc Controller for Microcomputers, T. H. Kehl and L. Dunkel .....	June 76, p 91
--	---------------

### Displays

Addressing the Elements of a Visual Display, J. E. Bryden .....	Nov 74, p 85
CMOS Enhances Video Display Terminal Design, K. Karstad .....	Sept 74, p 91
CRT Considerations in Data Terminal Design, A. D. Bedford .....	Feb 75, p 84
Economics of Designing with Raster Scan Displays, R. L. Chisenhall .....	July 78, p 98

### Graphics

Digital Image Processor Links TV Signal Sources to Computer, R. Dahlberg .....	Oct 77, p 115
--	---------------

- Flat Panel Displays Offer Graphics Alternatives, J. W. Aichroth ..... Oct 77, p 101
- High Speed Character Generator for Graphics Terminals, J. A. Glaab .... Mar 74, p 106
- An Interactive Software Program for a Standalone Graphic System, R. I. Ross ..... Sept 77, p 114

#### Interface

- Computer/Computer Interface, NASA ..... Mar 77, p 118
- Data Transfer with ASCII Eliminates Computer Interface Problem, W. Nadler ..... June 75, p 74
- Design Constraints for a UART-Based Minicomputer Communications Interface, A. Hirsch ..... June 77, p 167
- DMA Controller Capitalizes on Clock Cycles to Bypass CPU, J. Nissim .. Jan 78, p 117
- Integrating Peripherals into Processing Systems, R. J. Eufiger ..... Dec 78, p 77
- Interfacing Peripherals in Mixed Systems, R. Moffa ..... Apr 75, p 77
- Interfacing the Teletypewriter—Part 1: A-D and D-A Converters, M. Klafish ..... June 74, p 94
- Part 2: Programming Remote Relays, Solenoids, and Other Power Devices, M. Klafish ..... July 74, p 100
- Peripheral Interfacing With Microprocessors, A. J. Weissberger ..... Feb 77, p 108
- Technical Factors in Selecting Components for Mixed Systems, D. Hamblen ..... Mar 76, p 100

#### Terminals

- A BCD Conversion Technique for Teletypewriter Applications, C. Ellsworth and M. Malloch ..... Dec 74, p 69
- Choosing Proper Computer Output Systems, I. Wieselman ..... Dec 74, p 63
- Impact of LSI on Terminal Architecture, P. G. Cook and T. B. Cheek .. Nov 76, p 103
- Interfacing the Teletypewriter—Part 1: A-D and D-A Converters, M. Klafish ..... June 74, p 94
- Part 2: Programming Remote Relays, Solenoids, and Other Power Devices, M. Klafish ..... July 74, p 100
- Parallel CRC Lets Many Lines Use One Circuit, A. K. Pandeya and T. J. Cassa ..... Sept 75, p 87

#### Voice Response

- Design Guidelines for a Computer Voice Response System, P. Thorndarson ..... Nov 77, p 73
- Oral Annunciator With Programmable Vocabulary, NASA ..... Mar 78, p 128

#### General

- Digital Controller for Microfiche Display Selection, G. E. King ..... Oct 77, p 110
- Enormous Bucket-Brigade Optical Scanner Achieves High Efficiency, B. J. Deliduka ..... Feb 76, p 89
- Evolution of Microprogrammed Input/Output Processing in One Processor Family, R. Vahlstrom and M. Malone ..... Jan 76, p 98

- Floppy-Disc-Based Emulator Replaces Paper Tape Reader, K. W. Fisher .. May 78, p 192
- Hardware Versus Software for Microprocessor I/O, J. L. Nichols ..... Aug 76, p 102
- Ink-Jet Printer Mechanism Uses Non-Static Vacuum Technique, J. Heinzl and G. Rosenstock ..... July 78, p 104
- Minicomputer Peripheral Aids Program Debugging, S. R. Alpert .... Sept 76, p 104

## INSTRUMENTATION

### Data and Signal Generators

- A Computer Read/Write Clock, W. Nadler and G. G. McDonald ..... Sept 74, p 102
- Digital Synthesizers Produce Wide Frequency Range from Single Source, J. D. Fogarty ..... July 75, p 100
- A Digitally Controlled Pulse Generator for FM Modulation, V. L. Appleby ..... July 74, p 83
- Generating a 10-Hz Clock From a 50-/60-Hz Line, A. R. Rosenbaum Oct 74, p 118
- High Speed Character Generator for Graphics Terminals, J. A. Glaab ..... Mar 74, p 106
- Inexpensive Programmable Computer Clock, NASA ..... June 74, p 114
- Interval Timer Serves As a Baud Rate Generator, J. Beaston ..... Aug 78, p 112
- Programmable Sequence Generator Comprises Three Integrated Circuits, S. Waser ..... Apr 76, p 124
- A Universal Bipolar/MOS Clock Driver, J. Roberts and C. Chan .... Apr 74, p 152

### Digital Filters

- Hybrid Digital-Analog Implementation of Digital Filters, NASA ..... Apr 78, p 162
- RAM Digital Filter, NASA ..... May 77, p 134

### General

- Applications of Vector Processing, L. C. Higbie ..... Apr 78, p 139
- A Distributed Computer System for Laboratory Automation, G. A. Korn ..... June 77, p 177
- Measuring Settling Time, H. W. Crowley ..... Oct 74, p 120
- Multichannel High Speed Correlator, NASA ..... Feb 77, p 114
- Pattern Recognition: Basic Concepts and Implementation, D. Feucht .... Dec 77, p 57
- Programmable Amplifier for Binary/BCD-Mode Operation, R. Mauro .. Feb 75, p 102
- Providing Software Flexibility for Optical Processor Noise Analysis, R. G. Lyons ..... July 78, p 89
- Signal Processing and Display for Electrochemical Data, NASA ..... Apr 78, p 166
- Tools for Logic Analysis, J. Wagner .. Feb 76, p 108

## MEMORY/STORAGE

### Bubble

- Designing a Magnetic Bubble Data Recorder, Part I—The Component

Level, E. J. Hoffman, et al .....	Mar 76, p 77
Part 2—The System Level, E. J. Hoffman, et al .....	Apr 76, p 99
Magnetic Bubble Systems Approach Practical Use, J. E. Juliussen .....	Oct 76, p 81
A 11/2 Level On-Chip-Decoding Bubble Memory Chip Design, NASA ..	Feb 77, p 116
Open Coil Structure for Bubble-Memory-Device Packaging, NASA .....	Sept 76, p 112
Stripe-Line Coil for Magnetic-Field Generation in Bubble Memory Devices, NASA .....	July 76, p 116
Variable-Gap Bias Structure for Magnetic Bubble-Memory Package, NASA .....	Jan 77, p 104

#### Core

New Magnetic Materials Help Core Memories Stay Alive, R. D. Thurás .....	July 76, p 100
--	----------------

#### Flexible Disc

Design Considerations for Dual-Density Diskette Controllers, J. Worden .....	June 78, p 103
Floppy Disc-Based Emulator Replaces Paper Tape Reader, K. W. Fisher .....	May 78, p 192
Group Coded Recording Reliably Doubles Diskette Capacity, P. S. Sidhu .....	Dec 76, p 84
Hard Sectoring Without Holes Increases Capacity of Floppy Discs, R. M. Steincross .....	Feb 75, p 100
A Method of High Density Recording on Flexible Magnetic Discs, R. C. Franchini and D. L. Wartner .....	Oct 76, p 106
Simple Encoding Schemes Double Capacity of a Flexible Disc, D. J. Kalstrom .....	Sept 76, p 98
Simplified Floppy-Disc Controller for Microcomputers, T. H. Kehl and L. Dunkel .....	June 76, p 91
Synchronous Adapter Reduces Complexity of Floppy Disc Controller, M. E. Eidson and L. A. Parker .....	Apr 77, p 102

#### Hard Disc

Design/Application Consideration of Sealed vs Nonsealed Fixed-Head Units, M. Mougel .....	Sept 78, p 122
Jitter-Free Displays of Disc File Data, R. Beville .....	Dec 74, p 80
Multiple-Word Buffering for Disc Controllers with Bipolar FIFO Memory, K. Rallapalli .....	Dec 77, p 73
Servo Control Technique Enhances Performance of Disc Storage Units, T. W. Wright .....	Mar 77, p 99

#### Semiconductor

Adapter Simplifies Development of Microprocessor Systems, R. L. Morrison and C. A. Wiatrowski .....	May 76, p 175
Amorphous Semiconductors for Electrically Alterable Memory Applications, R. R. Shanks .....	May 74, p 95
An Associative-Capacitive ROM for Reprogrammable Logic Applications, M. Quinones .....	Jan 74, p 98

Automatic Error Correction in Memory Systems, B. Rickard .....	May 76, p 179
Battery Backup for Minicomputer Semiconductor Memories, J. Washburn .....	Apr 77, p 108
The Case for Using Partially Good Memory Devices, R. H. F. Lloyd .....	Apr 77, p 93
CCDs in Memory Systems Move into Sight, H. R. Crouch, et al .....	Sept 76, p 75
Current Semiconductor Memories, E. R. Hnatek .....	Apr 78, p 115
Designing Minicomputer Memory Systems with 4-Kilobit n-MOS Memories, D. Brunner .....	July 75, p 61
4-Kilobit Memories Present a Challenge to Testing, E. R. Hnatek .....	May 75, p 117
Large Bipolar ROMs and p/ROMs Revolutionize Logic and System Design, J. McDowell .....	June 74, p 100
LSI Bipolar FIFO Memory Increases Peripheral Controller Speed, P. Chu .....	Oct 78, p 136
Measurement Techniques for Testing High Speed Memories, K. Jackson and B. E. Sear .....	May 75, p 127
A Minicomputer Designer Chooses Semiconductor Over Core Memory, R. J. Frankenberg .....	Mar 75, p 59
New Error-Correcting Technique for Solid-State Memories Saves Hardware, G. R. Basham .....	Oct 76, p 110
Pattern Sensitivity on 4k RAM Devices, A. C. L. Chiang and R. Standridge .....	Feb 75, p 88
Pattern Sensitivity Techniques for Testing CCD Memories, I. D. Vancov .....	Nov 77, p 106
p/ROM Card Simplifies Computer Diagnosis, S. Waser .....	Jan 77, p 98
Selection and Application of Semiconductor Memories, S. Davis .....	Jan 74, p 65
Single Error Correcting Code Maximizes Memory System Efficiency, S. Sanyal and K. N. Venkataraman .....	May 78, p 175
Solving Mass-Produced ROM Programming Problems with Base Registers, J. A. Carroll .....	Aug 77, p 99
Timing Peculiarities of Multiplexed RAMs, J. R. Brown .....	July 77, p 85
An Update on MOS ROMs, D. Huffman .....	Sept 77, p 95

#### Tape Cassette/Cartridge

An Approach to Digital Recording by Low Cost Audio Cassette, F. W. Etcheverry .....	Oct 74, p 112
Data Rate Servo for Phase-Encoded Recording Systems, W. J. Kelly ..	Sept 74, p 77
Magnetic Tape Formatter Design Reduces Hardware/Software Requirements, A. S. McPhillips .....	Nov 77, p 99
New Method for Magnetic Encoding Combines Advantages of Older Techniques, A. M. Patel .....	Aug 76, p 85
The Serialized Approach to Reading Phase-Encoded Data, A. Wrobel and M. Gray .....	Feb 75, p 77

Smooth Tape Handling Increases Cassette Drive Reliability, S. Davis ..... Sept 75, p 94  
 Tradeoffs Among Binary Codes in Magnetic Tape Cassettes, J. J. Pastoriza ..... Jan 76, p 102  
 Update on Magnetic Tape Memories, S. Davis ..... Aug 74, p 127

**General**

Add-On Memory Sharing Scheme for Minicomputers, J. Protopapas ..... Apr 75, p 100  
 Advances in Memory Technology, H. F. Koehler ..... June 74, p 71  
 Clearing Up the Confusion: Virtual vs Mapped Memory, D. J. Tanner ..... Oct 76, p 101  
 Design Considerations for Ruggedized Memories, M. J. Maloney and S. Murahashi ..... May 74, p 114  
 Designer's Guide for Selecting Magnetic Mini-Media, A. B. Manildi .. Sept 77, p 120a  
 Design Techniques for Microprocessor Memory Systems, A. T. Thomas .... Aug 75, p 73  
 Expanding a Memory Without Plug-Compatibility, C. E. Cohn ..... Nov 75, p 102  
 Increasing Memory System Speed with a High Speed Buffer ..... May 74, p 118

**MICROCOMPUTERS**

**Applications**

Microprocessor/Microcomputer Application Contest, First Prize—Microprocessor Restroom Robot, C. A. Wiatrowski ..... Apr 77, p 98  
 Microprocessor/Microcomputer Application Contest, Second Prize—A Microprocessor-Controlled Three-Phase Power Inverter, P. van der Gracht and K. Mauch ..... May 77, p 120  
 Microprocessor/Microcomputer Application Contest, Third Prize—A Microcomputer-Controlled Seeder, V. Wrobel ..... June 77, p 184  
 Microprocessor/Microcomputer Application Contest, Fourth Prize—A Microprocessor Controller For an Epitaxial Reactor, D. Herberg, et al ..... July 77, p 108  
 Microprocessor/Microcomputer Application Contest, Fifth Prize—Electronic Diet Controller, K. M. Moran ..... Aug 77, p 116

**Architecture**

Current Microcomputer Architecture, R. M. Holt and M. R. Lemas ..... Feb 74, p 65

**Programming**

Altair Timesharing BASIC, S. Blumenthal and S. Webb ..... July 78, p 128  
 Developing Software for Microcomputer Applications, J. L. Pokoski and O. Holt ..... Mar 75, p 88  
 Handling Multilevel Subroutines and Interrupts in Microcomputers, J. F. Vittera ..... Jan 78, p 109  
 An Integral Real-Time Executive for Microcomputers, K. Burgett and E. F. O'Neil ..... July 77, p 77  
 Macro Processor Simplifies Microcomputer Programming, N. Sohrabji .. Aug 76, p 108

A Task-Scheduling Executive Program for Microcomputer Systems, D. A. Townzen ..... June 77, p 194

**General**

An Add-In Recognition Memory for S-100 Bus Microcomputers, Part I: An Introduction, S. Lamb ..... Aug 78, p 140  
 Part 2: Structure and Specification, S. Lamb ..... Sept 78, p 162  
 Part 3: Applications, S. Lamb ..... Oct 78, p 182  
 Design Motivations for Multiple Processor Microcomputer Systems, G. Adams and T. Rolander ..... Mar 78, p 81  
 Digital Input Units Isolate Microcomputers From Industrial Level Voltages, C. R. Teep'le ..... Nov 78, p 142  
 Economic Alternatives in Microcomputer Design, J. L. Nichols ..... Apr 76, p 110  
 A Fresh View of Mini- and Microcomputers, S. Davis ..... May 74, p 67  
 Generating Input/Output Device Select Pulses for Microcomputer Interfacing, D. G. Larsen, et al ..... May 76, p 196  
 Hybrid/LSI Package Yields a Single-Component Microcomputer, F. I. Redding and F. G. Snyder ..... Apr 76, p 114  
 IEEE 488: A Proposed Microcomputer I/O Bus Standard, B. E. Forbes .... Nov 78, p 140  
 Interfacing Calculator Chips as Microcomputer Preprocessors, W. W. Moyer ..... May 78, p 187  
 Microcomputer Development System Offers Adaptable Test Configurations, A. W. Bentley ..... Dec 78, p 122  
 Microcomputers Decentralize Processing in Data Communications Network, D. J. Mueller ..... Oct 77, p 81  
 Putting a Microcomputer on a Single Chip, H. A. Raphael ..... Dec 76, p 59  
 Restored Processor Function Saves Logic and Improves Performance in Microcomputer System, D. R. Ahlgren ..... Aug 75, p 88  
 Testing Microcomputer Boards Automatically, E. B. Foley, Jr and A. H. Firman ..... Dec 76, p 92  
 What is a Microcomputer Input/Output Device? J. A. Titus, et al ..... Mar 76, p 112

**MICROPROCESSORS**

**Architecture**

Analysis of a Multi-Microprocessor System Architecture, A. J. Weissberger ..... June 77, p 151  
 Comparisons and Trends in Microprocessor Architecture, E. E. Klingman ..... Sept 77, p 83  
 Distributed Function Microprocessor Architecture, A. Weissberger ..... Nov 74, p 77

**Interface Techniques**

Computer Interfacing: Anatomy of a Microcomputer, D. G. Larsen, et al ..... Feb 76, p 128  
 Interfacing Fundamentals:  
 An Application of the 8085 Processor—Part 1, P. R. Rony, et al ..... Sept 78, p 140  
 Part 2, J. A. Titus, et al ..... Oct 78, p 164

The 8085 Family of Memory Devices, C. Titus, et al .....	Aug 78, p 122
The 8085 Processor, D. G. Larsen, et al .....	July 78, p 114
An Introduction to Realtime Clocks, C. Titus, et al .....	Dec 78, p 110
<b>Microcomputer Interfacing:</b>	
Accumulator I/O Versus Memory I/O, J. A. Titus, et al .....	June 76, p 114
Analog Multiplexers, J. A. Titus, et al .....	Jan 78, p 132
Characteristics of the 8253 Programmable Interval Timer, M. L. DeJong, J. A. Titus, et al .....	Feb 78, p 136
Command Decoders, J. A. Titus, et al .....	June 78, p 135
Data Acquisition, J. A. Titus, et al .....	Sept 77, p 124
How Does a Microcomputer Make a Decision? D. G. Larsen, et al ..	Aug 76, p 118
Integer Addition and Subtraction, C. Titus, et al .....	Apr 78, p 168
Integer Multiplication and Division, P. R. Rony, et al .....	May 78, p 214
Interfacing a 10-Bit DAC, J. A. Titus, et al .....	June 77, p 203
Interfacing Analog-to-Digital Converters, D. G. Larsen, et al .....	Aug 77, p 124
Interfacing a Digital Multimeter, J. A. Titus, et al .....	Sept 76, p 114
Internal Registers Within the 8080 Chip, P. R. Rony, et al .....	Jan 77, p 122
Microcomputer Interrupts, D. G. Larsen, et al .....	Nov 76, p 142
Sample-and-Hold Devices, D. G. Larsen, et al .....	Dec 77, p 106
Using Digital-to-Analog Converters, C. Titus, et al .....	July 77, p 116
The Vectored Interrupt, J. A. Titus, et al .....	Dec 76, p 112
Peripheral Interfacing with Microprocessors, A. J. Weissberger .....	Feb 77, p 108
<b>Microprogramming</b>	
Designing Optimized Microprogrammed Control Sections for Microprocessors, G. W. Schultz .....	Apr 74, p 119
Hardware Approaches to Microprogramming with Bipolar Microprocessors, J. C. Conway .....	Aug 78, p 83
<b>Software</b>	
Implementing Branch Instructions with Polynomial Counters, O. Kaestner .....	Jan 75, p 69
Indexed Jump Feature for Intel 8008 Microprocessor, D. L. Abbott .....	June 74, p 112
<b>Interfacing Fundamentals:</b>	
Assembly Language or BASIC, Which Way to Go? D. G. Larsen, et al .....	Nov 78, p 158
A Demonstration Program for the 8253 Timer, D. G. Larsen, et al .....	Mar 78, p 134
A Look at Trends in Microprocessor/Microcomputer Software Systems, R. Martinez .....	June 75, p 51
<b>Microcomputer Interfacing:</b>	
The 8080 Logical Instruction, D. G. Larsen, et al .....	May 77, p 136
The 8080 Microcomputer Output Instruction, P. R. Rony, et al .....	Apr 76, p 128

The MOV and MVI 8080 Instructions, D. G. Larsen, et al .....	Feb 77, p 120
Preparing Your Programs, J. A. Titus, et al .....	Nov 77, p 132
Register Pair Instructions, J. A. Titus, et al .....	Mar 77, p 122
A Software UART, P. E. Field, et al .....	Oct 76, p 118
Subroutines and Stacks, P. R. Rony, et al .....	Oct 77, p 132
The Substitution of Software for Hardware, P. R. Rony, et al .....	July 76, p 120
What Is a Logical Instruction? P. R. Rony, et al .....	Apr 77, p 116
Multi-Level Nesting of Subroutines in a One-Level Microprocessor, P. de Marchin .....	Feb 76, p 118
Programming Hints Ease Use of Familiar Microprocessor, B. Gladstone and P. D. Page .....	Aug 76, p 77
Software Control of Microprocessor Based Realtime Clock, K. Karstad .....	Oct 78, p 99
Software Support for Microprocessors Poses New Design Choices, E. S. Nauful .....	Oct 76, p 93
System Languages for Microprocessors: Considerations and Trends ..	July 76, p 87
Using a Microprocessor. A Real-Life Application—Part 2: Software, L. E. Cannon and P. S. Kreager .....	Oct 75, p 81
<b>System Design</b>	
Adapter Simplifies Development of Microprocessor Systems, R. L. Morrison and C. A. Wiatrowski .....	May 76, p 175
Challenges in Microprocessor System Design, T. Jones and P. Thomas .....	Nov 76, p 109
Design Techniques for Microprocessor Memory Systems, A. T. Thomas .....	Aug 75, p 73
Formal Methods Expedite Microprocessor-Based System Design, B. J. Carey .....	Feb 77, p 97
Realtime Prototype Analysis as a Microprocessor Design Aid, R. Francis and R. Teitzel .....	Dec 78, p 65
<b>Test</b>	
A Flexible Approach to Microprocessor Testing, B. Schusheim .....	Mar 76, p 67
Microprocessor System Validation and Failure Isolation with Portable Tester, J. W. Neese .....	Sept 77, p 105
Microprocessor Test Technique Reveals Pattern Sensitivity, D. Hackmeister and A. C. L. Chiang .....	Dec 75, p 81
Testing Schemes for Microprocessor Chips, A. C. L. Chiang .....	Apr 75, p 87
<b>General</b>	
Block Transfer with DMA Augments Microprocessor Efficiency, J. Cosley and S. Vasa .....	Jan 77, p 81
Hardware Multiplication Techniques for Microprocessor Systems, B. Parasuraman .....	Apr 77, p 75
Hardware/Software for Process Control I/O, A. D. Marathe and A. K. Chandra .....	Mar 78, p 122

Hardware Versus Software for Microprocessor I/O, J. L. Nichols .....	Aug 76, p 102
Microprocessors Aid Experimentation in Scientific Laboratory, T. A. Seim .....	Sept 76, p 83
Microprocessors: Where Do They Fit? P. R. Rony, et al .....	Jan 76, p 108
Monolithic Processors, H. Schmid .....	Oct 74, p 87
Numerical Interpolation for Microprocessor-Based Systems, T. A. Seim .....	Feb 78, p 111
Operator's Console Considerations in Microprocessor System Design, J. Little and A. T. Thomas .....	Nov 75, p 87
Performance and Control of Multiple Microprocessor Systems, G. R. Reyling, Jr .....	Mar 74, p 81
Using a Calculator Chip to Extend a Microprocessor's Capabilities, P. H. Stakem .....	Sept 75, p 98
Using a Microprocessor: A Real-Life Application—Part I: Hardware, J. D. Logan and P. S. Kreager .....	Sept 75, p 69
Using a Microprocessor at Speeds Beyond Its Apparent Intrinsic Limit, M. Schwartz and K. Winter .....	June 76, p 106

## MINICOMPUTERS

### Architecture

Approach to Unified Bus Architecture Sidesteps Inherent Drawbacks, J. W. Conway .....	Jan 77, p 71
Microprogrammed CPU Architecture Offers User-Alterable Minicomputer Performance, P. Gordon and S. Stallard .....	June 78, p 91

### Design

Advanced Minicomputer Designed by Team Evaluation of Hardware/Software Tradeoffs, P. F. Conklin and D. P. Rodgers .....	Apr 78, p 129
Design Decisions Achieve Price/Performance Balance in Mid-Range Minicomputers, J. C. Mudge .....	Aug 77, p 87
Increasing Minicomputer Speed With Emitter-Coupled Logic, J. DeLaune .....	Feb 74, p 90
System-Level Integration Shrinks Size and Cost of Medium-Scale Computer, G. Hoff .....	Apr 76, p 81

### Programming

An Improved Minicomputer Program Interrupt Structure, A. Allison .....	Jan 74, p 81
Microcode Increases Minicomputer Processing Capability, S. Buchwald .....	Oct 77, p 91

### General

A Fresh View of Mini- and Microcomputers, S. Davis .....	May 74, p 67
Low Power Computers: A Make or Buy Decision, J. Washburn .....	Nov 76, p 120
Market Factors Portend Design Changes in Small Computers, D. R. Wulfinghoff .....	Aug 75, p 81
Protecting Minicomputers From Power Line Perturbations, R. M. Teets .....	June 76, p 99

## PROGRAMMABLE CALCULATORS

Computer Queuing Analysis on a Handheld Calculator, R. Zussman ..	Nov 77, p 85
Computer Simulation on a Pocket Calculator, R. Zussman .....	May 77, p 105
Computer Simulation Program for a Second Generation Handheld Calculator, R. Zussman .....	Mar 78, p 116
Predicting Queue Performance on a Programmable Handheld Calculator, R. Zussman .....	Aug 78, p 93
Programmable Calculators Control Data Acquisition Systems, J. Estes .....	Oct 75, p 73
Programmable Calculators Control Electronic System Testing, P. Chuhnov .....	Jan 76, p 73
Programmable Handheld Calculator Computes Digital-to-Analog Converter Errors, P. Prazak .....	June 78, p 122

## SOFTWARE

### Hardware Dedicated

A CAD Program for High Speed Logic Element Interconnections, T. Balph, et al .....	May 75, p 135
An Efficient Software Method for Implementing Polynomial Error Detection Codes, J. S. Whiting .....	Mar 75, p 73
An Interactive Software Program for a Standalone Graphic System, R. I. Ross .....	Sept 77, p 114
An Introduction to Vector Processing, P. M. Johnson .....	Feb 78, p 89
Minicomputer Peripheral Aids Program Debugging, S. R. Alpert .....	Sept 76, p 104
Moving Inversions Test Patterns is Thorough, Yet Speedy, J. H. de Jonge and A. J. Smulders .....	May 76, p 169
Virtual Memory Design Reduces Program Complexity, J. E. Requa .....	Jan 78, p 97

### Microprocessor/Microcomputer

Breakpoint Design for Debugging Microprocessor Software, T. P. Hughes and H. Sawin III .....	Nov 78, p 99
Calculating an Error-Checking Character in Software, S. Vasa .....	May 76, p 190
Developing Software for Microcomputer Applications, J. D. Pokoski and O. Holt .....	Mar 75, p 88
Handling Multilevel Subroutines and Interrupts in Microcomputers, J. F. Vittera .....	Jan 78, p 109
A Look at Trends in Microprocessor/Microcomputer Software Systems, R. Martinez .....	June 75, p 51
Macro Processor Simplifies Microcomputer Programming, N. Sohrabji .....	Aug 76, p 108
Programming Hints Ease Use of Familiar Microprocessor, B. Gladstone and P. D. Page .....	Aug 76, p 77
Software Analyses for Combinatorial Logic, J. L. Pokoski .....	June 78, p 113

Software Control of Microprocessor Based Realtime Clock, K. Karstad	Oct 78, p 99
Software Support for Microprocessors Poses New Design Choices, E. S. Naful	Oct 76, p 93
System Languages for Microprocessors: Considerations and Trends	July 76, p 87
A Task-Scheduling Executive Program for Microcomputer Systems, D. A. Townzen	June 77, p 194
Using a Microprocessor: A Real-Life Application—Part 2: Software, L. E. Cannon and P. S. Kreager	Oct 75, p 81

### Systems

Computer Simulation Program for a Second Generation Handheld Calculator, R. Zussman	Mar 78, p 116
Designing Interrupt Structures for Multiprocessor Systems, R. Jaswa	Sept 78, p 101
A Formal Design Language for Digital Systems, R. Crall	Nov 74, p 103

### TESTING

#### Automatic

Adversary Analysis: Computerized Testing of Computers, W. S. Holderby	Sept 75, p 100
An Automated Testing Procedure for Step Motor Simulation and Validation, R. E. Knoerzer	June 75, p 84
Automatic vs Manual Test Equipment, B. Sigsby	Feb 75, p 92
Data Reduction and Display in Automated Test Systems, T. Cave and D. Smith	May 78, p 161

#### Board/Component

Considerations in Semiconductor Tester Selection, D. Alvarez	Dec 76, p 69
Electrical Scanning Reduces Back-Panel Testing Time, M. Karr	Mar 77, p 104
A Flexible Approach to Microprocessor Testing, B. Schusheim	Mar 76, p 67
4-Kilobit Memories Present a Challenge to Testing, E. R. Hnatek	May 75, p 117
How Computers Can Test Their Own Memories, R. C. Goldblatt	July 76, p 69
Measurement Techniques for Testing High Speed Memories, K. Jackson and B. E. Sear	May 75, p 127
Microprocessor Test Technique Reveals Pattern Sensitivity, D. Hackmeister and A. C. L. Chiang	Dec 75, p 81
Pattern Sensitivity Techniques for Testing CCD Memories, I. D. Vancov	Nov 77, p 106
Testing Microcomputer Boards Automatically, E. B. Foley, Jr and A. H. Firman	Dec 76, p 92
Testing Schemes for Microprocessor Chips, A. C. L. Chiang	Apr 75, p 87

### System

Microprocessor System Validation and Failure Isolation with Portable Tester, J. W. Neese	Sept 77, p 105
Programmable Calculators Control Electronic Systems Testing, P. Chuhnov	Jan 76, p 73

### Tools

A Control Storage Simulator for Debugging Microprograms, P. Breeden	Apr 74, p 150
The Logic Analyzer: A Computer Troubleshooting Tool, N. A. Robin	Mar 76, p 89
Logic Analyzers in System Debugging Make Time Run Backward, J. C. Hill and C. Fiedler	Dec 75, p 67
Pattern Analyzer Synchronizes Scope in Presence of Jittery Signal, R. Reiser	July 75, p 106
Programmable Interface Drivers Simplify Logic Testing, D. T. Kan	July 76, p 106
p/ROM Card Simplifies Computer Diagnosis, S. Waser	Jan 77, p 98
Simplifying Processor Maintenance with a Carefully Designed Maintenance Panel, G. Gillow	July 75, p 95
Understanding Logic Analyzers, R. L. Down	June 77, p 188

### General

Common Misconceptions in Digital Test Generation, J. J. Thomas	Jan 77, p 89
Implementation of a Parallel Cyclic Redundancy Check Generator, K. M. Helness	Mar 74, p 91
Moving Inversions Test Pattern is Thorough, Yet Speedy, J. H. de Jonge and A. J. Smulders	May 76, p 169
What the Computer User Should Know About Computer-Controlled Testing, P. C. Jackson	Oct 74, p 97

### MISCELLANEOUS

#### Documentation

Competent Purchase Specifications Help Assure Successful Product, D. M. Hamblen	May 77, p 128
Documentation Standards Clarify Design, J. F. Wakerly	Feb 77, p 75
Signal Names Help System Understanding, W. Myers	July 75, p 81

#### Economics of Digital Electronics

Analyzing Computer Technology Costs—Part 1: Development and Manufacturing, M. Phister, Jr	Sept 78, p 91
Part 2: Maintenance, M. Phister, Jr	Oct 78, p 109

#### Security

Cyclic Sequence Generator Increases Security of Alarm Systems, R. Krishnaiyer and J. C. Donovan	July 75, p 73
---	---------------



# AUTHOR INDEX

- Abbott, D. L.**, Indexed Jump Feature for Intel 8008 Microprocessor .. June 74, p 112
- Adams, G. and Rolander, T.**, Design Motivations for Multiple Processor Microcomputer Systems ..... Mar 78, p 81
- Adams, G. F. and Atterbury, G. F.**, Building Today's Technologies Into a Large-Scale Time-Sharing System ..... Sept 75, p 79
- Adan, M. E.**, et al, Monolithic Data Conversion Devices, Part I: Digital-to-Analog Converters ..... Mar 78, p 152
- Ahlgren, D. R.**, Restored Processor Function Saves Logic and Improves Performance in Microcomputer System ..... Aug 75, p 88
- Aichroth, J. W.**, Flat Panel Displays Offer Graphics Alternatives .... Oct 77, p 101
- Allison, A.**, An Improved Minicomputer Program Interrupt Structure ..... Jan 74, p 81
- Alpert, S. R.**, Minicomputer Peripheral Aids Program Debugging .. Sept 76, p 104
- Alvarez, D.**, Considerations in Semiconductor Tester Selection ..... Dec 76, p 69
- Anderson, G. L. and Bartlett, K.**, Hardware Allocation of Data System Resources ..... July 74, p 89
- Anderson, T. O.**, Computer Interface-Timing Control Logic ..... Feb 74, p 96
- Apfel, R. J. and Jones, D. B.**, Universal Switching Regulator Diversifies Power Subsystem Applications ..... Mar 78, p 103
- Appel, R. L. and Pardoe, C. T.**, An Asynchronous Time-Division Multiplexing System ..... July 75, p 110
- Appleby, V. L.**, A Digitally Controlled Pulse Generator for FM Demodulation ..... July 74, p 83
- Atterbury, G. F. and Adams, G. F.**, Building Today's Technologies Into a Large-Scale Time-Sharing System ..... Sept 75, p 79
- 
- Balph, T.**, et al, A CAD Program for High Speed Logic Element Interconnections ..... May 75, p 135
- Barron, R. L.**, Learning Networks Improve Computer-Aided Prediction and Control ..... Aug 75, p 65
- Bartlett, K. and Anderson, G. L.**, Hardware Allocation of Data System Resources ..... July 74, p 89
- Basham, G. R.**, New Error-Correcting Technique for Solid-State Memories Saves Hardware ..... Oct 76, p 110
- Beaston, J.**, Interval Timer Serves As a Baud Rate Generator ..... Aug 78, p 112
- Becker, H. B.**, Functional Approach to Information Network Design .. May 74, p 83
- Bedford, A. D.**, CRT Considerations in Data Terminal Design ..... Feb 75, p 84
- Bentley, A. W.**, Microcomputer Development System Offers Adaptable Test Configurations ..... Dec 78, p 122
- Bernay, R. A.**, Hardware Binary-to-BCD Conversion and BCD Addition ..... Mar 74, p 98
- Beville, R.**, Jitter-Free Displays of Disc File Data ..... Dec 74, p 80
- Blacksher, R.**, Arithmetic Logic Unit Design for an LSI Minicomputer ..... Apr 75, p 96
- Blood, W.**, et al, A CAD Program for High Speed Logic Element Interconnections ..... May 75, p 135
- Blumenthal, S. and Webb, S.**, Altair Timesharing BASIC ..... July 78, p 128
- Bobba, G. M.**, et al, Decision-Making With Flags in Process Control .. Dec 76, p 77
- Bredeson, J. G.**, A Cellular Array for Integer and Fractional BCD-Binary Conversion ..... May 74, p 104
- Breeden, P.**, A Control Storage Simulator for Debugging Microprograms ..... Apr 74, p 150
- Brown, J. R., Jr.**, Timing Peculiarities of Multiplexed RAMs ..... July 77, p 85
- Brunner, D.**, Designing Minicomputer Memory Systems with 4-Kilobit n-MOS Memories ..... July 75, p 61
- Bryden, J. E.**, Addressing the Elements of a Visual Display ..... Nov 74, p 85
- Buchwald, S.**, Microcode Increases Minicomputer Processing Capability ..... Oct 77, p 91
- Buckley, J. E.**, Asynchronous Timing Error Characteristics ..... Feb 78, p 12
- AT&T's Digital Transmission Service June 74, p 10
- Certification 1977 ..... Dec 77, p 11
- Certification Update ..... July 78, p 12
- Communication System Security .. Mar 75, p 10
- Communications Act of 1978 ..... Nov 78, p 14
- Communications Code Compatibility ..... May 74, p 11
- Communications Software: Application Overview ..... Sept 74, p 16
- Communications Software: Functional Considerations ..... Oct 74, p 12
- Communications Traffic Analysis .. June 78, p 14
- Competitive Dialed Services ..... Mar 76, p 11
- Computer-Aided Network Design .. Apr 77, p 18
- Computer Communications Inquiry Oct 76, p 10
- Computerized PBX Systems ..... May 76, p 14
- Computerized Voice Network Control ..... Aug 77, p 12
- Data Communications Consultants Oct 77, p 10
- Data Network Response ..... Jan 77, p 14
- Dialed Digital Data Channels ..... Apr 76, p 10
- Domestic Communications Satellite System ..... Oct 75, p 15

Dynamic Multiplexing Applications	Nov 76, p 14	<b>Caplener, H. D. and Janku, J. A.,</b> Top-Down Approach to LSI System Design	Aug 74, p 143
IBM Protocols—Part 1: BSC	Jan 75, p 12	<b>Carey, B. J.,</b> Formal Methods Expedite Microprocessor-Based System Design	Feb 77, p 97
Part 2: SDLC	Feb 75, p 14	<b>Carroll, J.,</b> Eliminating Glitches From One-Shots in Logic Systems	Sept 75, p 104
Implications of the Communications Reform Act	Sept 76, p 14	<b>Carroll, J. A.,</b> Solving Mass-Produced ROM Programming Problems With Base Registers	Aug 77, p 99
In-WATS System Access	Aug 76, p 16	<b>Cassa, T. J. and Pandeya, A. K.,</b> Parallel CRC Lets Many Lines Use One Circuit	Sept 75, p 87
Information Systems Review—and Epilogue	Dec 78, p 14	<b>Cave, T. and Smith, D.,</b> Data Reduction and Display in Automated Test Systems	May 78, p 161
Intelligent Networks	Dec 74, p 10	<b>Chan, C. and Roberts, J.,</b> A Universal Bipolar/MOS Clock Driver	Apr 74, p 152
Interconnection Certification	Jan 76, p 14	<b>Chandra, A. K. and Marathe, A. D.,</b> Hardware/Software for Process Control I/O	Mar 78, p 122
Leased Communications Services	Aug 75, p 12	<b>Chang, S. and Lam, P.-L.,</b> A Multivibrator Using RC-Coupled Cascade Stages as a Ring Counter	May 74, p 120
Local Modems	Jan 78, p 14	<b>Cheek, T. B. and Cook, P. G.,</b> Impact of LSI on Terminal Architecture	Nov 76, p 103
Local System Access	Dec 76, p 20	<b>Chiang, A. C. L.,</b> Test Schemes for Microprocessor Chips	Apr 75, p 87
Management Automation Applications	May 78, p 11	<b>Chiang, A. C. L. and Hackmeister, D.,</b> Microprocessor Test Technique Reveals Instruction Pattern Sensitivity	Dec 75, p 81
Microcomputer Converter	Feb 76, p 12	<b>Chiang, A. C. L. and Standridge, R.,</b> Pattern Sensitivity on 4k RAM Devices	Feb 75, p 88
Multi-Vendor Information Systems	Aug 78, p 11	<b>Chisenhall, R. L.,</b> Economics of Designing with Raster Scan Displays	July 78, p 98
Network Design Criteria	May 75, p 14	<b>Christensen, G. S., et al,</b> A New Approach to Network Storage Management	Nov 75, p 81
Network Node Criteria	Dec 75, p 10	<b>Chu, P.,</b> LSI Bipolar FIFO Memory Increases Peripheral Controller Speed	Oct 78, p 136
1956 Consent Decree—History and Implications	Sept 78, p 14	<b>Chuhnov, P.,</b> Programmable Calculators Control Electronic System Testing	Jan 76, p 73
Non-Communications Programming Acronyms	Nov 74, p 14	<b>Ciugudean, M.,</b> Algorithm for Computing Logarithms and Antilogarithms	July 74, p 106
Office Automation	Nov 77, p 14	<b>Cohen, M.,</b> CMOS Logic Modules for Industrial Control	Mar 74, p 50
Packet Switching	Apr 74, p 10	<b>Cohn, C. E.,</b> Expanding a Memory Without Plug Compatibility	Nov 75, p 102
Possible 1977 WATS	Mar 77, p 12	<b>Coit, K. T.,</b> Programmable Multiline Communications Processor Provides Front-End Flexibility	May 77, p 99
Private Line Tariff Revisions	July 76, p 10	<b>Conklin, P. F. and Rodgers, D. P.,</b> Advanced Minicomputer Designed By Team Evaluation of Hardware/Software Tradeoffs	Apr 78, p 129
Ramifications of the Revised WATS Tariff	July 77, p 11	<b>Conway, J. C.,</b> Hardware Approaches to Microprogramming With Bipolar Microprocessors	Aug 78, p 83
Remote Batch vs Interactive Processing	Sept 75, p 10		
Remote Data Terminal Selection	Aug 74, p 10		
Remote Memory Systems and Applications	Oct 78, p 11		
Satellite Business Systems	June 76, p 10		
Shared User Networks	June 77, p 11		
Switched Communications Services	June 75, p 10		
Switched Network Service Alternatives	Apr 78, p 14		
Synchronous Timing Error Characteristics	Mar 78, p 14		
System Environmental Factors	Sept 77, p 18		
System Installation Criteria	Nov 75, p 14		
Telecommunications Diagnostics	Feb 74, p 10		
Telecommunications System Measurements	Mar 74, p 12		
Telephone Controllers	Jan 74, p 11		
Terminal Storage Systems	May 77, p 11		
Terminals: Human Factor Considerations	July 74, p 8		
Trans-Canada Datapac	Apr 75, p 10		
Unbundled Communications Services	July 75, p 11		
WATS Past and Present	Feb 77, p 14		
<b>Burens, J. H.,</b> Switching Power Supplies: Specification Criteria	Mar 77, p 91		
<b>Burgett, K. and O'Neil, E. F.,</b> An Integral Real-Time Executive For Microcomputers	July 77, p 77		
<b>Cairns, J., Jr, et al,</b> Microprocessor-Based Interface Converts Video Signals for Object Tracking	Dec 77, p 81		
<b>Camuso, J. A.,</b> Specifying and Selecting Uninterruptible Power Supply Systems	July 74, p 63		
<b>Cannon, L. E. and Kreager, P. S.,</b> Using a Microprocessor: A Real-Life Application—Part 2: Software	Oct 75, p 81		

- Conway, J. W.**, Approach to Unified Bus Architecture Sidesteps Inherent Drawbacks ..... Jan 77, p 71
- Cook, P. G. and Cheek, T. B.**, Impact of LSI on Terminal Architecture ..... Nov 76, p 103
- Cooper, S. B.**, Hardware Considerations for High Level Data Link Control Communications ..... Mar 75, p 81
- Cornett, J. B., Jr, et al**, CCDs in Memory Systems Move Into Sight ..... Sept 76, p 75
- Cosley, J. and Vasa, S.**, Block Transfer With DMA Augments Microprocessor Efficiency ..... Jan 77, p 81
- Crall, R. F.**, A Formal Design Language for Digital Systems ..... Nov 75, p 103
- Crouch, H. R.**, et al, CCDs in Memory Systems Move Into Sight .... Sept 76, p 75
- Crowley, H. W.**, Measuring Settling Time ..... Oct 74, p 120
- 
- Dahlberg, R.**, Digital Image Processor Links TV Signal Sources to Computer ..... Oct 77, p 115
- Davis, S.**, Digital Measurement of Shaft Position: Synchros and Resolvers or Encoders ..... Feb 76, p 50
- A Fresh View of Mini- and Microcomputers ..... May 74, p 67
- Selecting and Applying Stepping Motors in Computer Peripheral Equipment ..... May 75, p 141
- Selection and Application of Semiconductor Memories ..... Jan 74, p 65
- Smooth Tape Handling Increases Cassette Drive Reliability ..... Sept 75, p 94
- Update on Magnetic Tape Memories ..... Aug 74, p 127
- DeJong, M. L.**, et al, Microcomputer Interfacing: Characteristics of the 8253 Programmable Interval Timer ..... Feb 78, p 136
- A Demonstration Program for the 8253 Timer ..... Mar 78, p 134
- de Jonge, J. H. and Smulders, A. J.**, Moving Inversions Test Patterns Thorough, Yet Speedy ..... May 76, p 169
- DeLaune, J.**, Increasing Minicomputer Speed with Emitter-Coupled Logic ..... Feb 74, p 90
- Deliduka, B. J.**, Enormous Bucket-Brigade Optical Scanner Achieves High Efficiency ..... Feb 76, p 89
- de Marchin, P.**, Multi-Level Nesting of Subroutines in a One-Level Microprocessor ..... Feb 76, p 118
- de Smet, J. and Sanders, R. W.**, "Pacuit" Switching Combines Two Techniques in One Network ..... June 76, p 83
- Dickson, K. L.**, et al, Microprocessor-Based Interface Converts Video Signals for Object Tracking ..... Dec 77, p 81
- Dishon, Y.**, Data Compaction in Computer Systems ..... Apr 77, p 85
- Donaghey, L. F.**, et al, Decision-Making With Flags in Process Control ..... Dec 76, p 77
- Donovan, J. C. and Krishnaiyer, R.**, Cyclic Sequence Generator Increases Security of Alarm Systems ..... July 75, p 73
- Dove, R. K.**, OCR System Design Benefits from Technological Advances ..... Oct 75, p 91
- Down, R. L.**, Understanding Logic Analyzers ..... June 77, p 188
- Dunkel, L. and Kehl, T. H.**, Simplified Floppy-Disc Controller for Microcomputers ..... June 76, p 91
- 
- Eidson, M. E., and Parker, L. A.**, Synchronous Adapter Reduces Complexity of Floppy Disc Controller ..... Apr 77, p 102
- Ellsworth, C. A. and Malloch, W. G.**, A BCD Conversion Technique for Teletypewriter Applications .. Dec 74, p 69
- Embley, R. W.**, Solid-State Analog Switch Matrix Replaces Relay and Crossbar Selectors ..... Nov 75, p 112
- Erdman, A. C.**, Operation of Programmable Frequency Dividers .. Apr 74, p 110
- Estes, J.**, Programmable Calculators Control Data Acquisition Systems ..... Oct 75, p 73
- Etcheverry, F. W.**, An Approach to Digital Recording by Low Cost Audio Cassette ..... Oct 74, p 112
- Eufinger, R. J.**, Integrating Peripherals into Processing Systems .... Dec 78, p 77
- Eward, R. S.**, et al, CCDs in Memory Systems Move Into Sight ..... Sept 76, p 75
- 
- Feucht, D.**, Pattern Recognition: Basic Concepts and Implementations .. Dec 77, p 57
- Fichtenbaum, M. L.**, Top-Down Design Streamlines Digital System Projects ..... Sept 76, p 91
- Field, P. E.**, et al, Microcomputer Interfacing: A Software UART .... Oct 76, p 118
- Fiedler, C. and Hill, J. C.**, Logic Analyzers in System Debugging Make Time Run Backward ..... Dec 75, p 67
- Firman, A. H. and Foley, E. B., Jr**, Testing Microcomputer Boards Automatically ..... Dec 76, p 92
- Fisher, K. W.**, Floppy Disc-Based Emulator Replaces Paper Tape Reader ..... May 78, p 192
- Fletcher, J. G.**, Serial Communication Protocol Simplifies Data Transmission and Verification ..... July 78, p 77
- Fogarty, J. D.**, Digital Synthesizers Produce Wide Frequency Range from Single Source ..... July 75, p 100
- Foley, E. B., Jr and Firman, A. H.**, Testing Microcomputer Boards Automatically ..... Dec 76, p 92
- Forbes, B. E.**, IEEE 488: A Proposed Microcomputer I/O Bus Standard ..... Nov 78, p 170
- Forsyth, D. M.**, et al, Monolithic Data Conversion Devices—Part I: Digital-to-Analog Converters .... Mar 78, p 152
- Fortune, P. J.**, Two-Step Procedure Improves CRC Mechanism ..... Nov 77, p 116

<b>Franchini, R. C. and Wartner, D. L.</b> , A Method of High Density Recording on Flexible Magnetic Discs .....	Oct 76, p 106	<b>Goldblatt, R. C.</b> , How Computers Can Test Their Own Memories ..	July 76, p 69
<b>Francis, R. and Teitzel, R.</b> , Realtime Prototype Analysis As a Microprocessor Design Aid .....	Dec 78, p 65	<b>Gordon, B. M.</b> , Noise-Effects on Analog to Digital Conversion Accuracy—Part 1 .....	Mar 74, p 65
<b>Frankenberg, R. J.</b> , A Minicomputer Designer Chooses Semiconductor Over Core Memory .....	Mar 75, p 59	Part 2 .....	Apr 74, p 137
<b>Freeman, M. J. and Mulkowsky, G. P.</b> , Verbal Communication System Enhances Computer/Student Interaction .....	Jan 76, p 81	<b>Gordon, P. and Stallard, S.</b> , Microprogrammed CPU Architecture Offers User-Alterable Minicomputer Performance .....	June 78, p 91
<b>Gaal, S.</b> , The Mini: Efficient Alternative to Large Computer Control .....	Jan 74, p 46	<b>Gray, M. and Wrobel, A.</b> , The Serialized Approach to Reading Phase-Encoded Data .....	Feb 75, p 77
<b>Garen, E. R.</b> , Charge-Transfer Devices—Part 1: The Technologies .....	Nov 77, p 146	<b>Griffen, E. L.</b> , Conversion of Resolver or Synchro Trigonometric Outputs to Digital Data .....	Oct 74, p 105
Part 2: CCD Memories .....	Dec 77, p 130	<b>Hackmeister, D. and Chiang, A. C. L.</b> , Microprocessor Test Technique Reveals Instruction Pattern Sensitivity .....	Dec 75, p 81
Part 3: Diverse Uses of CTDs For Analog, Digital, and Optical Applications .....	Jan 78, p 154	<b>Hamblen, D. M.</b> , Competent Purchase Specifications Help Assure Successful Product .....	May 77, p 128
Custom Integrated Circuits: A Viable Alternative for Low to Intermediate Volume Applications .....	July 78, p 156	Technical Factors in Selecting Components for Mixed Systems .....	Mar 76, p 100
Have the LSI Parts You Buy Been Thoroughly Tested? .....	Oct 77, p 152	<b>Harmala, A. D.</b> , Benefits of Localized Control with Microcomputers .....	May 75, p 59
Integrated Injection Logic—A Technology Status Report .....	June 78, p 162	<b>Heinzl, J. and Rosenstock, G.</b> , Ink-Jet Printer Mechanism Uses Non-Static Vacuum Technique .....	July 78, p 104
Magnetic Bubble Memory Devices and Applications .....	Feb 78, p 164	<b>Helmick, C. G.</b> , Static UPS Systems: Application Case Histories .....	July 74, p 71
Monolithic Data Conversion Devices—Part 2: Analog-to-Digital Converters .....	Apr 78, p 188	<b>Helness, K. R.</b> , Implementation of a Parallel Cyclic Redundancy Check Generator .....	Mar 74, p 91
Part 3: Auxiliary Integrated Circuits .....	May 78, p 236	<b>Herberg, D.</b> , et al, Microprocessor/Microcomputer Applications Contest, Fourth Prize—A Microprocessor Controller for an Epitaxial Reactor .....	July 77, p 108
Semicustom Integrated Circuits—The Do-It-Yourself LSI Chips .....	Sept 77, p 148	<b>Herr, J. R.</b> , Self-Checking Number Systems .....	June 74, p 85
<b>Garen, E. R. and Smith, S.</b> , CMOS on Sapphire .....	Sept 78, p 194	<b>Heutink, F.</b> , Implications of Busing for Cellular Arrays .....	Nov 74, p 95
The Impact of VLSI Upon Computer Architecture .....	Oct 78, p 200	<b>Higbie, L. C.</b> , Applications of Vector Processing .....	Apr 78, p 139
Technology Status Report On Recent NMOS Processes .....	Aug 78, p 160	Associative Processors: A Panacea or a Specific? .....	July 76, p 75
<b>Garen, E. R.</b> , et al, Monolithic Data Conversion Devices—Part 1: Digital-to-Analog Converters .....	Mar 78, p 152	<b>Hill, J. C. and Fiedler, C.</b> , Logic Analyzers in System Debugging Make Time Run Backward .....	Dec 75, p 67
<b>Ghosh, S.</b> , Code Conversion Techniques For Digital Transmission ..	Aug 78, p 103	<b>Hirsch, A.</b> , Design Considerations For a UART-Based Minicomputer Communication Interface .....	June 77, p 167
<b>Gilbert, B. R. and Morse, M. J.</b> , Digital Simulator Replaces Analog Portion of Hybrid Computer .....	Apr 76, p 91	<b>Hnatek, E. R.</b> , Current Semiconductor Memories .....	Apr 78, p 115
<b>Gillow, G.</b> , Simplifying Processor Maintenance with a Carefully Designed Maintenance Panel .....	July 75, p 95	4-Kilobit Memories Present a Challenge to Testing .....	May 75, p 117
<b>Givens, S.</b> , Field-Effect Transistors as Analog Switches .....	June 74, p 106	Switching Regulator-Noise Suppression Techniques .....	Jan 75, p 94
<b>Glaab, J. A.</b> , High Speed Character Generator for Graphics Terminals .....	Mar 74, p 106	Switching Power Supplies: Design Considerations .....	Feb 77, p 89
<b>Gladstone, B. and Page, P. D.</b> , Programming Hints Ease Use of Familiar Microprocessor .....	Aug 76, p 77	<b>Hodges, D. A.</b> , Trends in Computer Hardware Technology .....	Feb 76, p 77
<b>Goksel, K. and Parrish, E. A., Jr.</b> , The Role of Microcomputers in Robotics .....	Oct 75, p 56	<b>Hoff, G.</b> , System-Level Integration Shrinks Size and Cost of Medium-Scale Computer .....	Apr 76, p 81

- Hoffman, E. J., et al**, Designing a Magnetic Bubble Data Recorder—Part 1: The Component Level ..... Mar 76, p 77  
 Part 2: The System Level ..... Apr 76, p 99
- Højberg, K. S.**, An Asynchronous Arbiter Resolves Resource Allocation Conflicts On a Random Priority Basis ..... Aug 77, p 120  
 One-Step Programmable Arbiters for Multiprocessors ..... Apr 78, p 154
- Holderby, W. S.**, Adversary Analysis: Computerized Testing of Computers ..... Sept 75, p 100  
 Designing a Microprocessor-Based Terminal for Factory Data Collection ..... Mar 77, p 81  
 Diagnostic Structures and Formats for Complex Computer Systems ..... May 75, p 148
- Holscher, J. N.**, Static UPS Systems: Configurations and Inverter Specifications ..... July 74, p 65
- Holt, A. W.**, Algorithm for a Low Cost Hand Print Reader ..... Feb 74, p 85
- Holt, O. and Pokoski, J. L.**, Developing Software for Microcomputer Applications ..... Mar 75, p 88
- Holt, R. M., and Lemas, M. R.**, Current Microcomputer Architecture ..... Feb 74, p 65
- Huffman, D.**, An Update on MOS ROMs ..... Sept 77, p 95
- Hughes, T. P., and Sawin, D. H., III**, Breakpoint Design for Debugging Microprocessor Software .. Nov 78, p 99
- 
- Iser, D. A., et al**, Design Considerations for Aerospace Digital Computers ..... Aug 74, p 113
- 
- Jackson, K. and Sear, B. E.**, Measurement Techniques for Testing High Speed Memories ..... May 75, p 127
- Jackson, P. C.**, What the User Should Know About Computer-Controlled Testing ..... Oct 74, p 97
- Jaeger, R.**, Microprogramming: A General Design Tool ..... Aug 74, p 150
- Janku, J. A. and Caplener, H. D.**, Top-Down Approach to LSI System Design ..... Aug 74, p 143
- Jaswa, R.**, Designing Interrupt Structures for Multiprocessor Systems ..... Sept 78, p 101
- Johnson, P. M.**, An Introduction to Vector Processing ..... Feb 78, p 89
- Jones, D. B. and Apfel, R. J.**, Universal Switching Regulator Diversifies Power Subsystem Applications ..... Mar 78, p 103
- Jones, P. D., et al**, A New Approach to Network Storage Management ..... Nov 75, p 81
- Jones, T. and Thomas, P.**, Challenges in Microprocessor System Design ..... Nov 76, p 109
- Joshi, D. and Phadnis, M. G.**, BCD/Binary Conversion with Single IC Cell ..... Dec 78, p 94
- Juliussen, J. E.**, Magnetic Bubble Systems Approach Practical Use .... Oct 76, p 81
- Jurison, J., et al**, Design Considerations for Aerospace Digital Computers ..... Aug 74, p 113
- 
- Kaestner, O.**, Implementing Branch Instructions with Polynomial Counters ..... Jan 75, p 69
- Kalstrom, D. J.**, Simple Encoding Schemes Double Capacity of a Flexible Disc ..... Sept 76, p 98
- Kan, D. T.**, Programmable Interface Drivers Simplify Logic Testing .. July 76, p 106
- Kancler, C. H.**, Architecture of Aerospace Computer Simplifies Programming ..... May 76, p 159
- Karr, M.**, Electrical Scanning Reduces Back-Panel Testing Time ..... Mar 77, p 104
- Karstad, K.**, CMOS Enhances Video Display Terminal Design ..... Sept 74, p 91  
 Software Control of Microprocessor Based Realtime Clock .... Oct 78, p 99
- Kehl, T. H. and Dunkel, L.**, Simplified Floppy-Disc Controller For Microcomputers ..... June 76, p 91
- Kelly, W. J.**, Data Rate Servo for Phase-Encoded Recording Systems ..... Sept 74, p 77
- Kenny, R.**, Microprogramming Simplifies Control System Design .. Feb 75, p 96
- King, G. E. and Nelson, A. V.**, Digital Controller for Microfiche Display Selection ..... Oct 77, p 110
- Klappfish, M.**, Interfacing the Teletypewriter—Part 1: A-D and D-A Converters ..... June 74, p 94  
 Part 2: Programming Remote Relays, Solenoids, and Other Power Devices ..... July 74, p 100
- Klingman, E. E.**, Comparisons and Trends In Microprocessor Architecture ..... Sept 77, p 83
- Knoerzer, R. E.**, An Automated Testing Procedure for Step Motor Simulation and Validation ..... June 75, p 84
- Knudson, J.**, Flexible-Cable/Connector Simplifies PCB Wiring ..... Aug 75, p 90
- Koehler, F. H.**, Advances in Memory Technology ..... June 74, p 71
- Korn, G. A.**, A Distributed Computer System for Laboratory Automation ..... June 77, p 177
- Kreager, P. S. and Cannon, L. E.**, Using a Microprocessor: A Real-Life Application—Part 2: Software ..... Oct 75, p 81
- Kreager, P. S. and Logan, J. D.**, Using a Microprocessor: A Real-Life Application—Part 1: Hardware ..... Sept 75, p 69
- Krechmer, K.**, Integrating Medium Speed Modems Into Communications Networks ..... Feb 78, p 101
- Krishnaiyer, R. and Donovan, J. C.**, Cyclic Sequence Generator Increases Security of Alarm Systems ..... July 75, p 73

<b>Ladstatter, C. F.</b> , Other Performance Factors in PC Board Connectors	Nov 74, p 106
<b>Lam, P.-L. and Chang, S.</b> , A Multi-vibrator Using RC-Coupled Cascade Stages as a Ring Counter	May 74, p 120
<b>Lamb, S.</b> , An Add-In Recognition Memory for S-100 Bus Minicomputers—Part 1: An Introduction	Aug 78, p 140
Part 2: Structure and Specifications	Sept 78, p 162
Part 3: Applications	Oct 78, p 182
<b>Lanning, W. C.</b> , General Algorithms for Direct Radix Conversion	June 75, p 61
<b>Larsen, D. G.</b> , et al, Computer Interfacing: Anatomy of a Microcomputer	Feb 76, p 128
Generating Input/Output Device Select Pulses for Microcomputer Interfacing	May 76, p 196
Interfacing Fundamentals: Assembly Language or BASIC, Which Way to Go?	Nov 78, p 158
The 8085 Processor	July 78, p 114
Microcomputer Interfacing: A Demonstration Program for the 8253 Timer	Mar 78, p 134
The 8080 Logical Instructions	May 77, p 136
How Does a Microcomputer Make a Decision?	Aug 76, p 118
Interfacing Analog-to-Digital Converters	Aug 77, p 124
Microcomputer Interrupts	Nov 76, p 142
The MOV and MVI 8080 Instructions	Feb 77, p 120
Sample-and-Hold Devices	Dec 77, p 106
See Also Rony, P. R., Titus, C., and Titus, J. A.	
<b>LeBlanc, P. and Victor, W.</b> , Structural Foam for Computer Equipment Enclosures	Oct 78, p 120
<b>Lemas, M. R. and Holt, R. M.</b> , Current Microcomputer Architecture	Feb 74, p 65
<b>Lesea, A. and Urkumyan, N.</b> , Multiplexer System Reduces Cost of Terminal Interfacing	Aug 77, p 109
<b>Liebowitz, B. H.</b> , Multiple Processor Minicomputer Systems—Part 1: Design Concepts	Oct 78, p 87
Part 2: Implementation	Nov 78, p 121
<b>Little, J. and Thomas, A. T.</b> , Operator's Console Considerations in Microprocessor System Design	Nov 75, p 87
<b>Lloyd, R. H. F.</b> , The Case For Using Partially-Good Memory Devices	Apr 77, p 93
<b>Lo, H.-Y.</b> , Digital Display of Stepper Motor Rotation	Apr 78, p 147
<b>Lobban, P. E.</b> , et al, Microprocessor/Microcomputer Applications Contest, Fourth Prize—A Microprocessor Controller for an Epitaxial Reader	July 77, p 108
<b>Logan, J. D. and Kreager, P. S.</b> , Using a Microprocessor: A Real-Life Application—Part 1: Hardware	Sept 75, p 69
<b>Logan, R. L.</b> , Congruent Partitioning and Network Synthesis	Dec 74, p 53
<b>Lubinski, K.</b> , et al, Microprocessor-Based Interface Converts Video Signals for Object Tracking	Dec 77, p 81
<b>Lyons, R. G.</b> , Providing Software Flexibility for Optical Processor Noise Analysis	July 78, p 89
<b>Malloch, W. G. and Ellsworth, C. A.</b> , A BCD Conversion Technique for Teletypewriter Applications	Dec 74, p 69
<b>Malone, M. and Vahlstrom, R.</b> , Evolution of Microprogrammed Input/Output Processing in One Processor Family	Jan 76, p 98
<b>Maloney, M. J. and Murahashi, S.</b> , Design Considerations for Ruggedized Memories	May 74, p 114
<b>Mancini, R. A.</b> , A Low Cost, Crystal-Controlled Oscillator Design	Jan 74, p 94
<b>Mandelbaum, D.</b> , Index-Register Logic Saves One Instruction per Loop	Oct 75, p 98
<b>Manildi, B. A.</b> , Designer's Guide for Selecting Magnetic Mini-Media	Sept 77, p 120a
<b>Marathe, A. D. and Chandra, A. K.</b> , Hardware/Software for Process Control I/O	Mar 78, p 122
<b>Martinez, R.</b> , A Look at Trends in Microprocessor/Microcomputer Software Systems	June 75, p 51
<b>Mauch, K. and van der Gracht, P.</b> , Microprocessor/Microcomputer Applications Contest, Second Prize—A Microprocessor-Controlled Three-Phase Power Inverter	May 77, p 120
<b>Mauro, R.</b> , Programmable Amplifier for Binary/BCD-Mode Operation	Feb 75, p 102
<b>McDonald, G. G. and Nadler, W.</b> , A Computer Read/Write Clock	Sept 74, p 102
<b>McDowell, J.</b> , Large Bipolar ROMs and p/ROMs Revolutionize Logic and System Design	June 74, p 100
<b>McGovern, T. L.</b> , et al, Designing a Magnetic Bubble Data Recorder—Part 1: The Component Level	Mar 76, p 77
Part 2: The System Level	Apr 76, p 99
<b>McKee, H. C.</b> , Improved CRC Technique Detects Erroneous Leading and Trailing 0's in Transmitted Data Blocks	Oct 75, p 102
<b>McPhillips, A. S.</b> , Magnetic Tape Formatter Design Reduces Hardware/Software Requirements	Nov 77, p 99
<b>McShane, T. J.</b> , Automatic Dialing for Computer Communications	Apr 74, p 146
<b>Meyer, C. H.</b> , Enciphering Data for Secure Transmission	Apr 74, p 129
<b>Meyers, W.</b> , Signal Names Help System Understanding	July 75, p 81
<b>Meyn, John</b> , Digitized Video Processing in Realtime	Dec 78, p 104
<b>Miles, J.</b> , Another Use for NAND Gates	Dec 74, p 84
<b>Moffa, R.</b> , Interfacing Peripherals in Mixed Systems	Apr 75, p 77

- Moilanen, U.**, Information Preserving Codes Compress Binary Pictorial Data ..... Nov 78, p 134
- Montgomery, R. C.**, Simple Hardware Approach to Error Detection and Correction ..... Nov 78, p 109
- Moore, R. C.**, et al, Designing a Magnetic Bubble Data Recorder—Part 1: The Component Level .. Mar 76, p 77  
Part 2: The System Level ..... Apr 76, p 99
- Moran, K. M.**, Microprocessor/Microcomputer Applications Contest, Fifth Prize—Electronic Diet Controller ..... Aug 77, p 116
- Morrison, R. L. and Wiatrowski, C. A.**, Adapter Simplifies Development of Microprocessor Systems ..... May 76, p 175
- Morse, M. J. and Gilbert, B. R.**, Digital Simulator Replaces Analog Portion of Hybrid Computer .... Apr 76, p 91
- Mougel, M.**, Design/Application Considerations of Sealed vs Non-sealed Fixed-Head Disc Units .. Sept 78, p 122
- Moyer, W. W.**, Interfacing Calculator Chips As Microcomputer Preprocessors ..... May 78, p 187
- Mudge, J. C.**, Design Decisions Achieve Price/Performance Balance in Mid-Range Minicomputers ..... Aug 77, p 87
- Mueller, D. J.**, Microcomputers Decentralize Processing in Data Communications Network ..... Oct 77, p 81
- Mulkowsky, G. P. and Freeman, M. J.**, Verbal Communication System Enhances Computer/Student Interaction ..... Jan 76, p 81
- Munn, J. F.**, Low Cost Data Acquisition System Using Standard DIPs ..... May 78, p 200
- Murahashi, S. and Maloney, M. J.**, Design Considerations for Ruggedized Memories ..... May 74, p 114
- Nadler, W.**, Data Transfer With ASCII Eliminates Computer Interface Problems ..... June 75, p 74
- Nadler, W. and McDonald, G. G.**, A Computer Read/Write Clock .. Sept 74, p 102
- Naufel, E. S.**, Software Support for Microprocessors Poses New Design Choices ..... Oct 76, p 93
- Neese, J. W.**, Microprocessor System Validation and Failure Isolation With Portable Tester ..... Sept 77, p 105
- Nelson, A. V. and King, G. E.**, Digital Controller for Microfiche Display Selection ..... Oct 77, p 110
- Nguyen-Huu, A.**, Advances in CMOS Device Technology ..... Jan 75, p 87
- Nichols, J. L.**, Economic Alternatives In Microcomputer Design ..... Apr 76, p 110  
Hardware Versus Software for Microprocessor I/O ..... Aug 76, p 102
- Nissim, J.**, DMA Controller Capitalizes on Clock Cycles to Bypass CPU ..... Jan 78, p 117
- O'Neil, E. F. and Burgett, K.**, An Integral Real-Time Executive for Microcomputers ..... July 77, p 77
- Page, P. D. and Gladstone, B.**, Programming Hints Ease Use of Familiar Microprocessor ..... Aug 76, p 77
- Pandeya, A. K. and Cassa, T. J.**, Parallel CRC Lets Many Lines Use One Circuit ..... Sept 75, p 87
- Parasuraman, B.**, Hardware Multiplication Techniques for Microprocessor Systems ..... Apr 77, p 75
- Pardoe, C. T. and Appel, R. L.**, An Asynchronous Time-Division Multiplexing System ..... July 75, p 110
- Parker, L. A. and Eidson, M. E.**, Synchronous Adapter Reduces Complexity of Floppy Disc Controller ..... Apr 77, p 102
- Parrish, E. A., Jr and Goksel, K.**, The Role of Microcomputers in Robotics ..... Oct 75, p 56
- Pastoriza, J. J.**, Tradeoffs Among Binary Codes in Magnetic Tape Cassettes ..... Jan 76, p 102
- Patel, A. M.**, New Method for Magnetic Encoding Combines Advantages of Older Techniques .. Aug 76, p 85
- Pathak, J.**, Time-Slicing Offers an Alternative to Multiprocessor Systems ..... July 77, p 95
- Phadnis, M. G. and Joshi, D.**, BCD/Binary Conversion with Single IC Cell ..... Dec 78, p 94
- Phister, M., Jr**, Analyzing Computer Technology Costs—Part 1: Developing and Manufacturing .... Sept 78, p 91  
Part 2: Maintenance ..... Oct 78, p 109
- Piankian, R. A.**, Master Calendar-Clock Serves Multiple Minicomputers ..... Oct 78, p 156
- Pokoski, J. L.**, Software Analyses for Combinatorial Logic ..... June 78, p 113
- Pokoski, J. L. and Holt, O.**, Developing Software for Microcomputer Applications ..... Mar 75, p 88
- Poley, N. M.**, Electro-Optical Scan Converter Shares Benefits of Conventional Units ..... Dec 75, p 75
- Prazak, P.**, Programmable Handheld Calculator Computes Digital-to-Analog Converter Errors ..... June 78, p 122
- Prioste, J.**, et al, A CAD Program for High Speed Logic Element Interconnections ..... May 75, p 135
- Prosser, F. and Winkel, D.**, Mixed Logic Leads to Maximum Clarity with Minimum Hardware ..... May 77, p 111
- Protopapas, J.**, Add-On Memory Sharing Scheme for Minicomputers ..... Apr 75, p 100
- Quinones, M.**, An Associative-Capacitive ROM for Reprogrammable Logic Applications ..... Jan 74, p 98

- Rallapalli, K.**, Multiple-Word Buffering for Disc Controllers With Bipolar FIFO Memory ..... Dec 77, p 73
- Raphael, H. A.**, Low Cost A-to-D Conversion During Microcomputer Idle Time ..... Mar 77, p 112
- Putting a Microcomputer On a Single Chip ..... Dec 76, p 59
- Ratnakumar, N.**, et al, Microprocessor/Microcomputer Applications Contest, Fourth Prize—A Microprocessor Controller for an Epitaxial Reactor ..... July 77, p 108
- Redding, F. I. and Snyder, F. G.**, Hybrid/LSI Package Yields a Single-Component Microcomputer ..... Apr 76, p 114
- Reiser, R.**, Pattern Analyzer Synchronizes Scope in Presence of Jittery Signal ..... July 75, p 106
- Requa, J. E.**, Virtual Memory Design Reduces Program Complexity .. Jan 78, p 97
- Reyling, G., Jr.**, Performance and Control of Multiple Microprocessor Systems ..... Mar 74, p 81
- Rickard, B.**, Automatic Error Correction in Memory Systems ..... May 76, p 179
- Riggs, W.**, Small Stepping Motors Meet Varied Application Requirements ..... Feb 78, p 120
- Roberts, J. and Chan, C.**, A Universal Bipolar/MOS Clock Driver .. Apr 74, p 152
- Robin, N. A.**, The Logic Analyzer: A Computer Troubleshooting Tool ..... Mar 76, p 89
- Rodgers, D. P. and Conklin, P. F.**, Advanced Minicomputer Designed By Team Evaluation of Hardware/Software Tradeoffs ..... Apr 78, p 129
- Rolander, T. and Adams, G.**, Design Motivations for Multiple Processor Microcomputer Systems .. Mar 78, p 81
- Rony, P. R.**, et al, Interfacing Fundamentals: An Application of the 8085 Processor—Part I ..... Sept 78, p 140
- Microcomputer Interfacing: The 8080 Microcomputer Output Instruction ..... Apr 76, p 128
- Integer Multiplication and Division ..... May 78, p 214
- Internal Registers Within the 8080 Chip ..... Jan 77, p 122
- A Software UART ..... Oct 76, p 118
- Subroutines and Stacks ..... Oct 77, p 132
- The Substitution of Software for Hardware ..... July 76, p 120
- What Is a Logical Instruction? .. Apr 77, p 116
- Microprocessors: Where Do They Fit? ..... Jan 76, p 108
- See also Larsen, D. G., Titus, C., and Titus, J. A.
- Rosenbaum, A. R.**, Generating a 10-Hz Clock From a 50-/60-Hz Line ..... Oct 74, p 118
- Rosenstock, G. and Heinzl, J.**, Ink-Jet Printer Mechanism Uses Non-Static Vacuum Technique ..... July 78, p 104
- Ross, R. I.**, An Interactive Software Program for a Standalone Graphic System ..... Sept 77, p 114
- Rubin, A. I.**, Multivariable Function Generation for Hybrid Computers ..... Feb 76, p 99
- Rubin, X. K.**, et al, Decision-Making with Flags in Process Control .... Dec 76, p 77
- Ruggeri, L.**, Design of a Programmable One-Shot Multivibrator .. Mar 74, p 110
- Russell, B. J.**, et al, Design Considerations for Aerospace Digital Computers ..... Aug 74, p 113
- 
- Sanders, R. W. and de Smet, J.**, "Pacuit" Switching Combines Two Techniques in One Network ..... June 76, p 83
- Sanyal, S.**, An Algorithm for Nonrestricting Division ..... May 77, p 124
- Sanyal, S. and Venkataraman, K. N.**, Single Error Correcting Code Maximizes Memory System Efficiency ..... May 78, p 174
- Sawin, D. H., III and Hughes, T. P.**, Breakpoint Design for Debugging Microprocessor Software ..... Nov 78, p 99
- Schmid, H.**, Monolithic Processors .. Oct 74, p 87
- Schultz, G. W.**, Designing Optimized Microprogrammed Control Sections for Microprocessors ..... Apr 74, p 119
- Schusheim, B.**, A Flexible Approach to Microprocessor Testing ..... Mar 76, p 67
- Schwartz, M. and Winter, K.**, Using a Microprocessor at Speeds Beyond Its Apparent Intrinsic Limit ..... June 76, p 106
- Sear, B. E. and Jackson, K.**, Measurement Techniques for Testing High Speed Memories ..... May 75, p 127
- Seim, T. A.**, Microprocessors Aid Experimentation in Scientific Laboratory ..... Sept 76, p 83
- Numerical Interpolation for Microprocessor-Based Systems ..... Feb 78, p 111
- Sell, J. V.**, Microprogramming in an Integrated Hardware/Software System ..... Jan 75, p 77
- Sexton, W. and Whittaker, G.**, Printers and Readers Handshake for Effective Bar Code Systems ..... Sept 74, p 69
- Shaeffer, L.**, VMOS Peripheral Drivers Solve High Power Load Interface Problems ..... Dec 77, p 90
- Shanks, R. R.**, Amorphous Semiconductors for Electrically Alterable Memory Applications ..... May 74, p 95
- Shapiro, S. F.**, Computer Process Control Around the World ..... Nov 75, p 58
- Digital Technology Enables Robots to "See" ..... Jan 77, p 43
- Instrument Industry Recognizes Digital Electronics—Almost ..... Jan 77, p 50
- Professional Group Conference Stresses Microprocessor Applications for Process Control ..... May 76, p 84
- Social/Economic/Governmental Considerations of Automation .. Dec 75, p 50
- Sharan, R.**, Matrix Computations Forecast Computer Mainframe Reliability ..... Aug 76, p 95

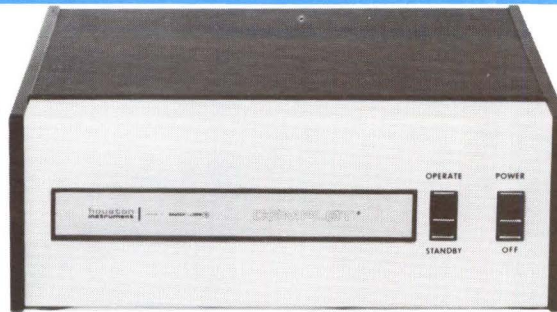


- Sheth, R. D.**, POS Cable: A Design Study ..... Nov 75, p 106
- Shi, S.-Y.**, Shortcut to Logarithms Combines Table Lookup and Computation ..... May 76, p 184
- Sidhu, P. S.**, Group-Coded Recording Reliably Doubles Diskette Capacity ..... Dec 76, p 84
- Sigsby, B.**, Automatic vs Manual Test Equipment ..... Feb 75, p 92
- Simopoulos, N. T.**, Carrying Out Division By Addition Reduces Hardware Complexity ..... June 75, p 80
- Smith, A. A., Jr.**, Design Technique for a Near-Field Communication System ..... Sept 74, p 85
- Smith, D. and Cave, T.**, Data Reduction and Display in Automated Test Systems ..... May 78, p 161
- Smith, S.**, External Arithmetic Processors ..... Dec 78, p 144  
Single-Chip Speech Synthesizers .. Nov 78, p 188
- Smith, S. and Garen, E. R.**, CMOS on Sapphire ..... Sept 78, p 194  
The Impact of VLSI Upon Computer Architecture ..... Oct 78, p 200  
Technology Status Report on Recent NMOS Processes ..... Aug 78, p 160
- Smulders, A. J. and de Jonge, J. H.**, Moving Inversions Test Pattern Is Thorough, Yet Speedy ..... May 76, p 169
- Snyder, F. G. and Redding, F. I.**, Hybrid/LSI Package Yields a Single-Component Microcomputer ..... Apr 76, p 114
- Sohrabji, N.**, Macro Processor Simplifies Microcomputer Programming ..... Aug 76, p 108
- Stakem, P. H.**, Using a Calculator Chip to Extend a Microprocessor's Capabilities ..... Sept 75, p 98
- Stallard, S. and Gordon, P.**, Microprogrammed CPU Architecture Offers User-Alterable Minicomputer Performance ..... June 78, p 91
- Standridge, R. and Chiang, A. C. L.**, Pattern Sensitivity on 4k RAM Devices ..... Feb 75, p 88
- Steincross, R. M.**, Hard Sectoring Without Holes Increases Capacity of Floppy Discs ..... Feb 75, p 100
- Su, S. Y. H.**, Logic Design and Its Recent Development Part 5: Fault Diagnosis in Digital Mathematics ..... Jan 74, p 87  
Part 6: Computer-Aided Logic Design ..... Feb 74, p 77
- Sullwold, S.**, Choosing the Correct Flat Cable for High Speed Logic Circuits ..... Dec 75, p 97
- Swanson, R.**, Understanding Cyclic Redundancy Codes ..... Nov 75, p 93
- Talambiras, R. P.**, Digital-to-Analog Converters: Some Problems in Producing High-Fidelity Signals ..... Jan 76, p 63
- Tall, D. S.**, Applying Magnetic Circuit Breakers in Digital Circuits ..... Nov 78, p 132
- Tanner, D. J.**, Clearing Up the Confusion: Virtual vs Mapped Memory ..... Oct 76, p 101
- Teeple, C. R.**, Digital Input Units Isolate Microcomputers From Industrial Level Voltages ..... Nov 78, p 142
- Teets, R. M.**, Protecting Minicomputers From Power Line Perturbations ..... June 76, p 99
- Teitzel, R. and Francis, R.**, Realtime Prototype Analysis As a Microprocessor Design Aid ..... Dec 78, p 65
- Thomas, A. T.**, Design Techniques for Microprocessor Memory Systems ..... Aug 75, p 73
- Thomas, A. T. and Little, J.**, Operator's Console Considerations in Microprocessor System Design .. Nov 75, p 87
- Thomas, J. J.**, Common Digital Misconceptions in Digital Test Generation ..... Jan 77, p 89
- Thomas, P. and Jones, T.**, Challenges in Microprocessor System Design ..... Nov 76, p 109
- Thordarson, P.**, Design Guidelines for a Computer Voice Response System ..... Nov 77, p 73
- Thornton, J. E., et al.**, A New Approach to Network Storage Management ..... Nov 75, p 81
- Thuras, R. D.**, New Magnetic Materials Help Core Memories Stay Alive ..... July 76, p 100
- Titus, C., et al.**, Interfacing Fundamentals: The 8085 Family of Memory Devices ..... Aug 78, p 122  
An Introduction to Realtime Clocks ..... Dec 78, p 110  
Microcomputer Interfacing: Integer Addition and Subtraction ..... Apr 78, p 168  
Using Digital-to-Analog Converters ..... July 77, p 116  
See also Larsen, D. G., Rony, P. R., and Titus, J. A., beginning June 1977
- Titus, J. A., et al.**, Interfacing Fundamentals: An Application of the 8085 Processor—Part 2 .... Oct 78, p 164  
Microcomputer Interfacing: Accumulator I/O vs Memory I/O .. June 76, p 114  
Analog Multiplexers ..... Jan 78, p 132  
Characteristics of the 8253 Programmable Interval Timer .... Feb 78, p 136  
Command Decoders ..... June 78, p 135  
Data Acquisition ..... Sept 77, p 124  
Interfacing a Digital Multimeter ..... Sept 76, p 114  
Interfacing a 10-Bit DAC ..... June 77, p 203  
Preparing Your Programs ..... Nov 77, p 132  
Register Pair Instructions ..... Mar 77, p 122  
The Vectored Interrupt ..... Dec 76, p 112  
What Is a Microcomputer Input/Output Device? ..... Mar 76, p 112  
See also Larsen, D. G., Rony, P.R., and Titus, C.
- Townzen, D. A.**, A Task-Scheduling Executive Program for Microcomputer Systems ..... June 77, p 194
- Trudo, F. J.**, A General-Purpose Interface for Industrial Process Control ..... Dec 74, p 78

<b>Urkumyan, N. and Lesea, A.</b> , Multiplexer System Reduces Cost of Terminal Interfacing .....	Aug 77, p 109	<b>White, G. M.</b> , Software-Based Single-Bit I/O Error Detection and Correction Scheme .....	Sept 78, p 130
<b>Vahlström, R. and Malone, M.</b> , Evolution of Microprogrammed Input/Output Processing in One Processor Family .....	Jan 76, p 98	<b>Whiting, J. S.</b> , An Efficient Software Method for Implementing Polynomial Error Detection Codes ..	Mar 75, p 73
<b>van der Gracht, P. and Mauch, K.</b> , Microprocessor/Microcomputer Applications Contest, Second Prize—A Microprocessor Controlled Three-Phase Power Inverter .....	May 77, p 120	<b>Whittaker, G. and Sexton, W.</b> , Printers and Readers Handshake for Effective Bar Code Systems .....	Sept 74, p 69
<b>Vancov, I. D.</b> , Pattern Sensitivity Techniques for Testing CCD Memories .....	Nov 77, p 106	<b>Wiatrowski, C. A.</b> , Microprocessor/Microcomputer Applications Contest, First Prize—Microprocessor-Restroom Robot .....	Apr 77, p 99
<b>Vandling, G. C.</b> , Organization of a Microprogrammed Aerospace Computer .....	Feb 75, p 65	<b>Wiatrowski, C. A. and Morrison, R. L.</b> , Adapter Simplifies Development of Microprocessor Systems .....	May 76, p 175
<b>Vasa, S.</b> , Calculating an Error Checking Character in Software .....	May 76, p 190	<b>Wieselman, I. L.</b> , Choosing Proper Computer Output Systems .....	Dec 74, p 63
<b>Vasa, S. and Cosley, J.</b> , Block Transfer With DMA Augments Microprocessor Efficiency .....	Jan 77, p 81	<b>Willard, D. G.</b> , A Time Division Multiple Access System for Digital Communications .....	June 74, p 79
<b>Venkataraman, K. N. and Sanyal, S.</b> , Single Error Correcting Code Maximizes Memory System Efficiency .....	May 78, p 175	<b>Winkel, D. and Prosser, F.</b> , Mixed Logic Leads to Maximum Clarity with Minimum Hardware .....	May 77, p 111
<b>Victor, W. and LeBlanc, P.</b> , Structural Foam for Computer Equipment Enclosures .....	Oct 78, p 120	<b>Winklebleck, P. K.</b> , Computer Connector Saves Space and Cuts Cost .....	Dec 78, p 106
<b>Vittera, J. F.</b> , Handling Multilevel Subroutines and Interrupts in Microcomputers .....	Jan 78, p 109	<b>Winter, K. and Schwartz, M.</b> , Using a Microprocessor at Speeds Beyond Its Intrinsic Limit .....	June 76, p 106
<b>Wagner, J. W.</b> , Tools for Logic Analysis .....	Feb 76, p 108	<b>Wittmayer, W. R.</b> , Array Processor Provides High Throughput Rates .....	Mar 78, p 93
<b>Wakerly, J. F.</b> , Documentation Standards Clarify Design .....	Feb 77, p 75	<b>Wolin, L.</b> , Procedure Evaluates Computers For Scientific Applications .....	Nov 76, p 93
<b>Wanner, J. F.</b> , Wideband Communication System Improves Response Times .....	Dec 78, p 85	<b>Worden, J.</b> , Design Considerations for Dual-Density Diskette Controllers .....	June 78, p 103
<b>Wartner, D. I. and Franchini, R. C.</b> , A Method of High Density Recording on Flexible Magnetic Discs ..	Oct 76, p 106	<b>Wright, T. W.</b> , Servo Control Technique Enhances Performance of Disc Storage Units .....	Mar 77, p 99
<b>Waser, S.</b> , Programmable Sequence Generator Comprises Three Integrated Circuits .....	Apr 76, p 124	<b>Wrobel, A. and Gray, M.</b> , The Serialized Approach to Reading Phase-Encoded Data .....	Feb 75, p 77
p/ROM Card Simplifies Computer Diagnosis .....	Jan 77, p 98	<b>Wrobel, V.</b> , Microprocessor/Microcomputer Applications Contest, Third Prize—A Microcomputer-Controlled Seeder .....	June 77, p 184
State-of-the-Art in High Speed Arithmetic Integrated Circuits ..	July 78, p 67	<b>Wulfinghoff, D. R.</b> , Market Factors Portend Design Changes in Small Computers .....	Aug 75, p 81
<b>Washburn, J.</b> , Battery Backup for Minicomputer Semiconductor Memories .....	Apr 77, p 108	<b>Wyland, D. C.</b> , Using p/ROMs as Logic Elements .....	Sept 74, p 98
Low Power Computers: A Make or Buy Decision .....	Nov 76, p 120	<b>Zuch, E. L.</b> , Interpretation of Data Converter Accuracy Specifications .....	Sept 78, p 113
<b>Webb, S. and Blumenthal, S.</b> , Altair Timesharing BASIC .....	July 78, p 128	<b>Zussman, R.</b> , Computer Queuing Analysis On a Handheld Calculator .....	Nov 77, p 85
<b>Weissberger, A. J.</b> , Analysis of Multiple-Microprocessor System Architectures .....	June 77, p 151	Computer Simulation on a Pocket Calculator .....	May 77, p 105
Distributed Function Microprocessor Architecture .....	Nov 74, p 77	Computer Simulation Program for a Second Generation Handheld Calculator .....	Mar 78, p 116
Peripheral Interfacing With Microprocessors .....	Feb 77, p 108	Predicting Queue Performance on a Programmable Handheld Calculator .....	Aug 78, p 93

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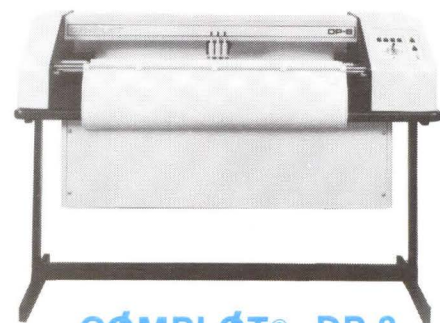
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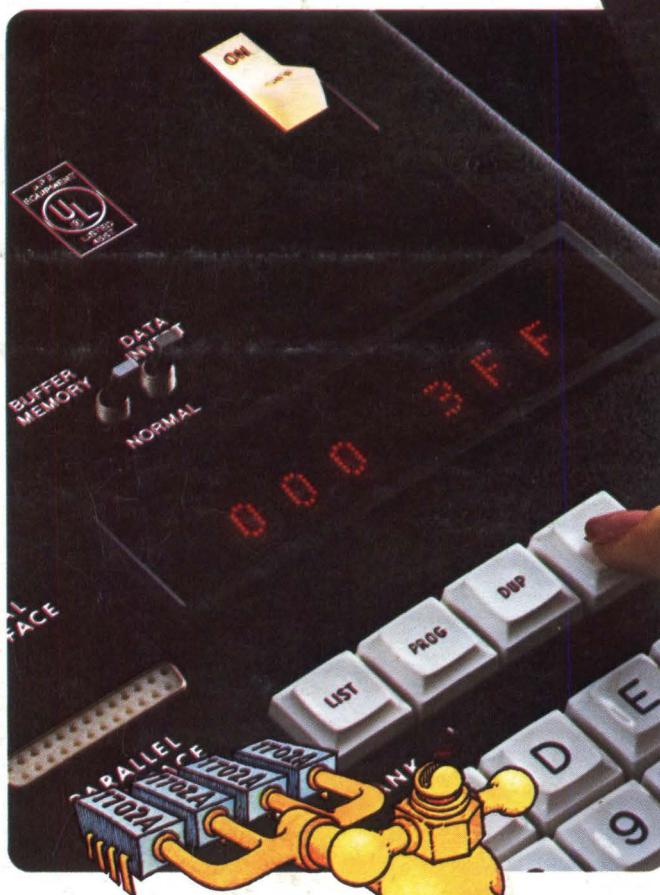
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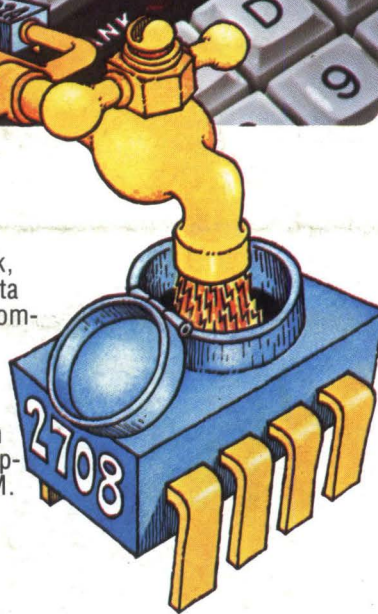
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