# COMPUTER DESIGN

**THE** MAGAZINE OF DIGITAL ELECTRONICS

SEPTEMBER 1979



**SEMICONDUCTOR ADVANCES BOOST DIGITAL IMAGE PROCESSING SYSTEM PERFORMANCE**

**UNIFIED APPROACH TO DESIGNING HARDWARE BASED ON IEEE STD 488**

**AUTOMATIC NETWORK SYNTHESIZER IDENTIFIES STANDARD LSI CELLS**


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CIRCLE 2 ON INQUIRY CARD

# COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

SEPTEMBER 1979

VOLUME 18, NUMBER 9


## DEPARTMENTS



## FEATURES




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(USPS 127-340)

## STAFF




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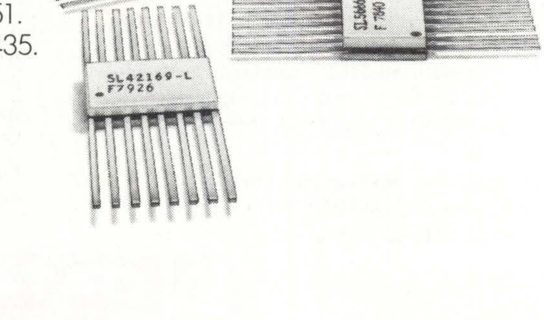
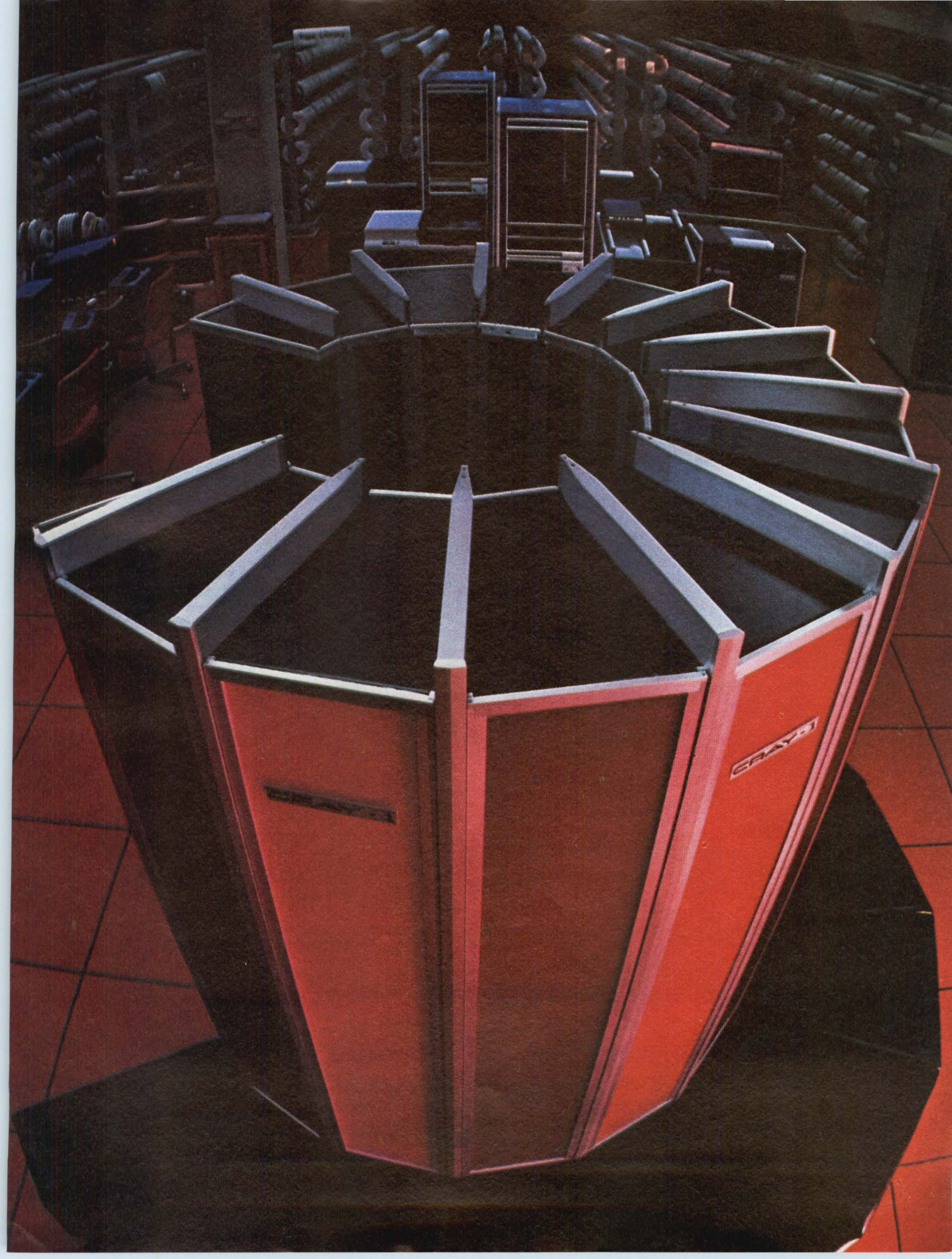



**CIRCLE 6 ON INQUIRY CARD**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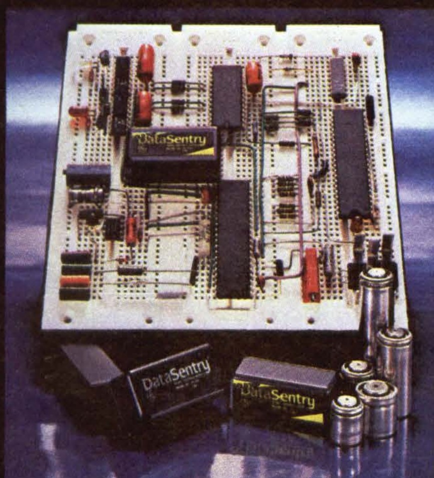


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CIRCLE 7 ON INQUIRY CARD

# WHEN IT COMES TO PUTTING IT ALL ON DISPLAY, THE ORION-60/S4 STANDS ALONE.

Magnavox combines the superior display and control features of the plasma-panel-based Orion-60 terminals with the powerful S4 Micro-Computer System.

The result is a stand alone graphics system that allows you the freedom to develop a wide variety of graphics application and development programs—while maintaining complete control over program storage, program-generated data, library routines and other facilities.

The Orion-60 display terminal offers full graphics with floppy-disc storage, as well as optional rear-projection functions. It lets you create your own displays and enter data by simply touching the screen with your finger. So you can program your own character sets and generate vectors of any length to absolute coordinates. And because the Orion-60 is plasma-based, you'll get bright, high-contrast images free of jitter or distortion.

The S4 Micro-Computer has system software with development capabilities that are as good or better than those found in many larger computer systems.

Features include CP/M* 8080 system utilities, Fortran with 32K RAM, and a full range of graphic utility routines including window, zoom, sub-image movement and rotation.

The Orion-60/S4.

For a demonstration, call or write Tyler Hunt at Magnavox Display Systems, 2131 South Coliseum Boulevard, Fort Wayne, Indiana 46803, (219) 482-4411.

**Magnavox**
**DISPLAY SYSTEMS**

**CP/M is a trademark of Digital Research.*

**CIRCLE 8 ON INQUIRY CARD**

# CALENDAR

## CONFERENCES

**OCT 10; NOV 1; AND NOV 15—Invitational Computer Conference,** Newton, Mass; Cherry Hill, NJ; and Southfield, Mich. INFORMATION: B. J. Johnson & Assoc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

**OCT 17-18—Connector Sym,** Hyatt House, Cherry Hill, NJ. INFORMATION: Electronic Connector Study Group, Inc, PO Box 1428, Camden, NJ 08101

**OCT 17-18—Western Computer Conf,** Calgary Convention Ctr, Alberta, Canada. INFORMATION: Janet Glover, Whitsed Publishing Ltd, 2 Bloor St W, Suite 2504, Toronto, Ontario M2W 3E2, Canada. Tel: 416/967-6200

**OCT 17-19—Design Automation Workshop,** Michigan State U, East Lansing, Mich. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

**OCT 22-23—Conf on Local Computer Networking,** Marquette Inn, Minneapolis, Minn. INFORMATION: Kenneth J. Thurber, Sperry Univac, PO Box 3525, St Paul, MN 55165. Tel: 612/456-3806

**OCT 23-25—Semiconductor Test Conf,** Hyatt House, Cherry Hill, NJ. INFORMATION: Tess Mitchell, PO Box 38, Collegeville, PA 19426. Tel: 215/489-9387

**OCT 25-26—Newport Conf on Fiber-Optic Markets,** Sheraton-Islander Hotel, Newport, RI. INFORMATION: Kessler Marketing Intelligence, 22 Farewell St, Newport, RI 02840. Tel: 401/849-6771

**OCT 30-NOV 1—CAD/CAM VII at Automated, Integrated, Factory of Tomorrow Conf,** Cobo Hall, Detroit, Mich. INFORMATION: Jeff Spire, SME Technical Div, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1500, X405

**OCT 30-NOV 1—Interface West,** Anaheim Convention Ctr, Anaheim, Calif. INFORMATION: Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502

**NOV 5-7—Asilomar Conf on Circuits, Systems and Computers,** Asilomar Hotel and Conf Grounds, Pacific Grove, Calif. INFORMATION: Donald E. Kirk, Naval Postgraduate School, Monterey, CA 93940. Tel: 408/646-2081

**NOV 5-8—Computer Software and Applications Conf (COMPSAC),** The Palmer House, Chicago, Ill. INFORMATION: Dr William Smith, Bell Laboratories, Naperville, IL 60540. Tel: 312/690-2389

**NOV 6-8—Federal Computer Conf,** Sheraton-Park Hotel, Washington, DC. INFORMATION: Federal Computer Conf, PO Box 368, Wayland, MA. Tel: 617/358-5181

**NOV 6-8—MIDCON,** O'Hare Convention Ctr and Hyatt Regency O'Hare, Chicago, Ill. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

**NOV 14-16—Micro and Mini Computer Conf,** Astro Village, Houston, Tex. INFORMATION: Dr Sam Lee, School of Electrical Engineering and Computer Science, U of Oklahoma, 202 W Boyd, Norman, OK 73019. Tel: 405/325-4721

**NOV 18-21—Micro 12,** Hershey, Pa. INFORMATION: Harry Hayman, Micro 12, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

**NOV 26-29—Data Communications Sym and Tutorial,** Asilomar Conf Grounds, Pacific Grove, Calif. INFORMATION: Kenneth J. Thurber, Sperry Univac, U2U19, PO Box 3525, St Paul, MN 55165. Tel: 612/456-3806

**NOV 26-29—Internat'l Telecommunications Energy Conf (INTELEC),** Sheraton Park Hotel, Washington, DC. INFORMATION: R. H. Jones, ITT North Electric, PO Box 688, Galion, OH 44833. Tel: 419/468-8525

**NOV 27-29—Nat'l Telecommunications Conf,** Shoreham-Americana Hotel, Washington, DC. INFORMATION: John N. Birch, Dept of Defense, 3311 Marlbough Way, College Pk, MD 20740. Tel: 301/935-0684

**DEC 3-5—Internat'l Electron Devices Meeting (IEDM),** Washington Hilton Hotel, Washington, DC. INFORMATION: Sarah M. Cooper, Courtesy Assoc, Inc, 1629 K St, NW, Suite 700, Washington, DC 20006

**DEC 10-11—Internat'l Sym on Mini & Microcomputers in Control,** Galt Ocean Mile Hotel, Ft Lauderdale, Fla. INFORMATION: The Secretary, Computers in Control Sym, PO Box 2481, Anaheim, CA 92804. Tel: 714/774-6144

**DEC 10-15—MESUCORA (Measurement, Control, Regulation, Automation) Exhibition, Physics Exhibition, and Internat'l Exhibition of Electrical Equipment,** Parc des Expositions, Porte de Versailles, Paris, France. INFORMATION: Sepic/Mesucora, 40 Rue du Colisée, 75381 Paris Cedex 08, France

**JAN 23-25—Internat'l Microcomputers, Minicomputers, Microprocessors (IMMM)—Japan '80,** Harumi Exhibition Ctr, Tokyo, Japan. INFORMATION: Industrial & Scientific Conf Management, Inc, 222 W Adams St, Chicago, IL 60606. Tel: 312/263-4866

## SEMINARS

**NOV 5-6—Understanding Data Communications Network Components, and NOV 19-20—Data Communications Standards,** McGraw-Hill Headquarters, New York, NY; and Hyatt on Union Square, San Francisco, Calif. INFORMATION: McGraw-Hill Conf Ctr, 1221 Ave of the Americas, Rm 3677, New York, NY 10020. Tel: 212/997-2930

**NOV 7-9—Internat'l Telecommunications Forum,** Innisbrook, Tarpon Springs, Fla. INFORMATION: Kate Dalton, Arthur D. Little, Inc, Acorn Pk, Cambridge, MA 02140. Tel: 617/864-5770, X3407

## SHORT COURSES

**OCT 8-12—Data Communication Systems and Networks, OCT 29—Modern Software Development Techniques, and OCT 29-31—Magnetic Bubble Memory Technology,** George Washington U, Washington, DC. INFORMATION: Continuing Engineering Education, George Washington U, Washington, DC 20052 .Tel: 202/676-6106

**OCT 15, OCT 22, AND DEC 3—Micro—Hands-On Microprocessor Workshop,** Washington, DC, and Lafayette, Ind. INFORMATION: Wintek Corp, 902 N 9th St, Lafayette, IN 47904. Tel: 317/742-6802

**OCT 17-19—An Introduction to Pascal Programming, and NOV 14-16—Advanced Programming Techniques Using Pascal,** Sheraton Inn, Allentown, Pa. INFORMATION: Software Consulting Services, 901 Whittier Dr, Allentown, PA 18103. Tel: 215/797-9690

**Announcements intended for publication in this department of *Computer Design* must be received at least *three* months prior to the date of the event. To ensure proper timely coverage of major events, material preferably should be received six months in advance.**

# LETTERS TO THE EDITOR

To the Editor:

In reference to Martin Newman's application note, "Number Sorting Algorithm Saves Processing Time," *Computer Design*, Apr 1979, p 104, a careful analysis of the algorithm exposes an error in Pass 2. Generating a result table from the Pass 2 example (shown as Table 3 on p 110 in the article) yields the table "Error Conditions in Table 3." The error occurs when performing the transformation of the contents of the Auxiliary Table.

The actual transformation is performed as follows:

(a) Load the number of entries in the number table into register A.

(b) Save the contents of the location to be transformed.

(c) Store the contents of register A in location to be transformed.

(d) Subtract the data saved in step (b) from register A.

(e) Repeat steps (b), (c), and (d) for each consecutive location of the Auxiliary Table.

This completes the Pass 2 processing. Pass 3 of the algorithm is completed as described in the article.

The table "Results from Revised Algorithm" shows Table 3 of the example problem completed with the revised algorithm.

Harry H. Dill
Baltimore, Md

**Error Conditions in Table 3**

| Number Table | | | Auxiliary Table | | Results |
|---|---|---|---|---|---|
| Linc Address Table | Location Contents | LOC | Contents After Pass 2 | LOC | Contents |
| A | 6 | 0 | ~~0~~ −1? | 0 | J |
| B | 8 | 1 | 1 | 1 | H |
| C | 4 | 2 | ~~1~~ 0 | 2 | * D,G |
| D | 4 | 3 | ~~2~~, 1 | 3 | C |
| E | 12 | 4 | ~~3~~,~~2~~,1 | 4 | I |
| F | 9 | 5 | 0 | 5 | A |
| G | 3 | 6 | ~~5~~,4 | 6 | * |
| H | 2 | 7 | ~~7~~,6 | 7 | K |
| I | 6 | 8 | ~~8~~,7 | 8 | B |
| J | 0 | 9 | ~~9~~,8 | 9 | F |
| K | 10 | 10 | 10 | 10 | E |
| | 11 | 10 | 10 | 11 | |
| | 12 | 9 | ~~10~~,9 | 12 | |

* — Error Condition

*The Author Replies:*

Mr Dill is mistaken in his analysis of the example given in my article "Number Sorting Algorithm Saves Processing Time" (*Computer Design*, Apr 1979).

Referring to p 110, Table 3, and to the description of Pass 2, the values in the third column are obtained as follows:

1) Number of entries in Number Table (11) is loaded into accumulator.

2) Entry in location 12 (1) is subtracted from 11; leaves 10; 10 is inserted into location 12.

3) Entry in location 11 (0) is subtracted from 10; leaves 10; 10 is inserted into location 10.

4) Entry in location 10 (0) is subtracted from 10; leaves 10; 10 is inserted into location 10.

5) Entry in location 9 (1) is subtracted from 10; leaves 9; 9 is inserted into location 9.

This procedure continues until the whole auxiliary table has been

**Results From Revised Algorithm**

| Number Table | | | Auxiliary Table | | Results |
|---|---|---|---|---|---|
| Linc Address Table | Location Contents | LOC | Contents After Pass 2 | LOC | Contents |
| A | 6 | 0 | ~~1~~,0 | | |
| B | 8 | 1 | 1 | 1 | J |
| C | 4 | 2 | ~~2~~,1 | 2 | H |
| D | 4 | 3 | ~~3~~,2 | 3 | G |
| E | 12 | 4 | ~~5~~,~~4~~,3 | 4 | D |
| F | 9 | 5 | 5 | 5 | C |
| G | 3 | 6 | ~~7~~,~~6~~,5 | 6 | I |
| H | 2 | 7 | ~~8~~,7 | 7 | A |
| I | 6 | 8 | ~~9~~,8 | 8 | K |
| J | 0 | 9 | ~~10~~,9 | 9 | B |
| K | 7 | 10 | 10 | 10 | F |
| | | 11 | 10 | 11 | E |
| | | 12 | 11 | | |

scanned. The values shown by Mr Dill are incorrect and do not result from application of Pass 2, as described in the article.

In addition, there is a correction to be made to Table 3. The entry in "Location Contents After Pass 2" sixth from the top should be 5 instead of 0.

The following corrections should be made to the description of Pass 3:

1) On p 110, text column 3, line 17 from top should read "contents are incremented by one."

2) Table 4's Auxiliary Table, p 110, should be $7(+1 = 8)$ instead of $7(-1 = 6)$ and $6(+1 = 7)$ instead of $6(-1 = 5)$.

3) In the third column of the program on p 112 under SCAN 3, the instruction "INR M ; Increment memory by 1" should be inserted between the instructions MOV E,M and MOV L,A.

Martin Newman
Tadiran Electronics Industries
Petach Tikvah, Israel

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To the Editor:

I would like to correct some of the specifications for the AP-120B cited in the article "Comparison of Selected Array Processor Architectures" (Stephen P. Hufnagel, *Computer Design,* Mar 79, pp 151-158).

(1) RAM table memory increments are 1k words.

(2) Main data memory increments are 8/16/32/64k words up to 512k words.

(3) Program source memory increments are 1k words up to 4k words.

(4) Maximum programmed I/O rate is 3.0M words/s.

(5) Floating point mantissa guaranteed precision is 27 bits.

(6) "AP-120B Array Processor Handbook" is FPS 800-7259-003.

Roy D. Gwin
Floating Point Systems, Inc
Portland, Ore

**Letters to the Editor should be addressed:**

**Editor, Computer Design**
**11 Goldsmith St**
**Littleton, MA 01460**

# DISTRIBUTED SYSTEM HARDWARE DESIGN OFFERS INTERCHANGEABLE COMMUNICATIONS

**E. J. Steubesand**

International Business Machines Corporation
Kingston, New York

A distributed processing system that could also be used in a centralized or standalone processor environment must allow for attachment to many types of communications facilities. Common carrier and Postal Telephone and Telegraph administrations furnish a wide range of these for data processing networks. Switched facilities are offered for occasional data link connections, and nonswitched point to point and multipoint facilities are provided for networks that require dedicated data links. These links are used for long and short haul network connections and use both analog and digital transmission techniques. In addition, onsite communication capabilities are provided by a number of private companies. Many data link protocols and interface standards are used.

### Network Environment

A network uses data links to interconnect processors and terminals. In the centralized network concept, each terminal uses these links to interact with a remote host processor and its data base (Fig 1). In this environment, data processing equipment must be designed to attach to the long and short haul common carrier and Postal Telephone and Telegraph (PTT) data links so that centralized networks can be formed.

In a distributed system, a processor is added between the central host and the terminal sites (Fig 2). Some programs and data that were resident at the central site are now located at the terminal site. With the latter approach, less communication with the host is required, but the processor at the terminal site must accommodate onsite communication capabilities while still supporting attachment to central host systems. The IBM 8100 Information System* provides two onsite communication capabilities, a synchronous data link control (SDLC) loop, and direct connection without data sets. The loop allows attachment of many terminals dis-

*_Computer Design_, Dec 1978, pp 42-47

# ADVANTAGE: CENTRONICS

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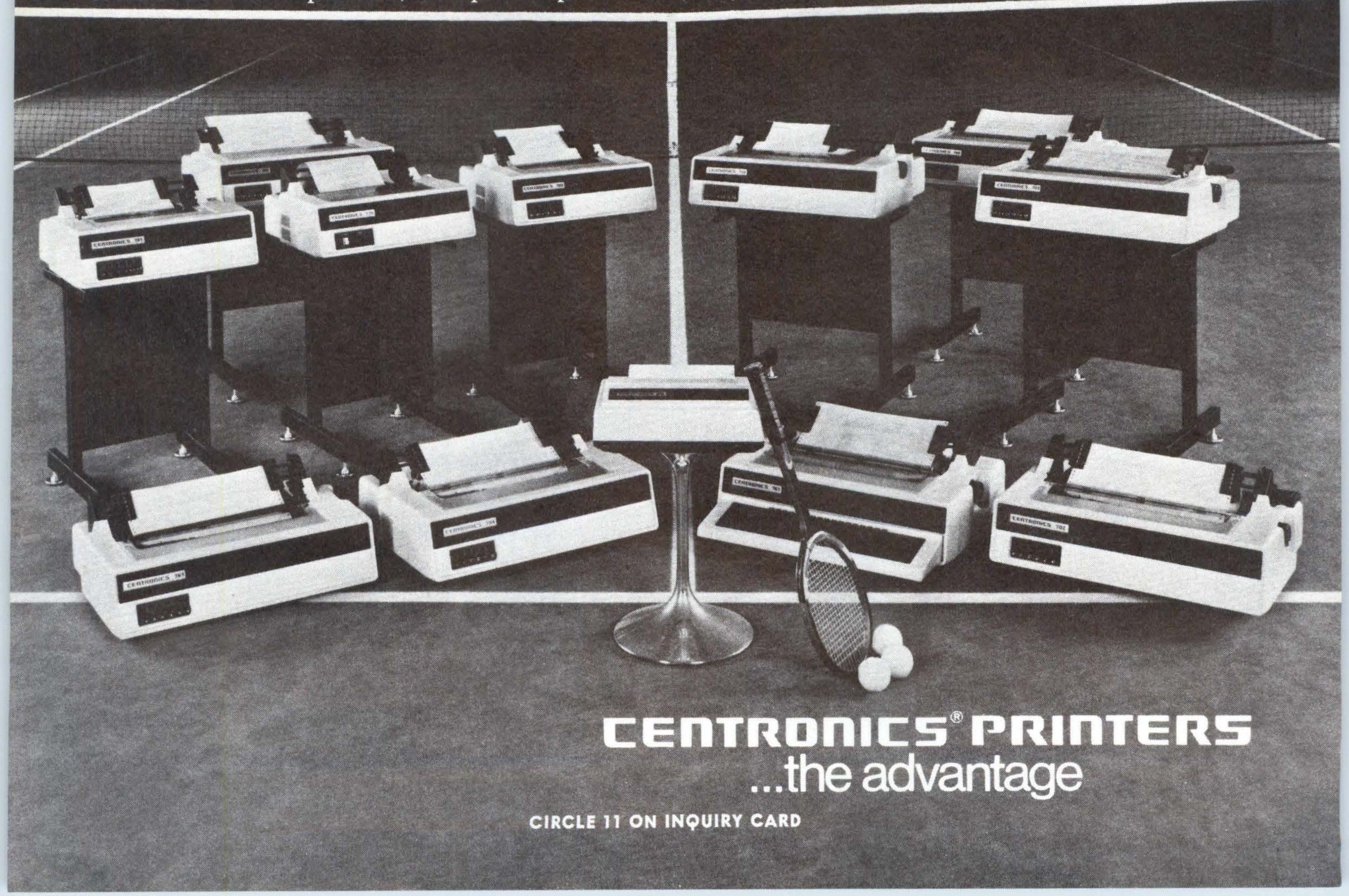
For more information on products or employment opportunities, call or write today: Centronics Data Computer Corporation, Hudson, New Hampshire 03051, (603) 883-0111.



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The HP 1000 system also comes with a number of applications tools to minimize your programming costs. HP's new DATACAP/1000 software, for example, lets you design a real-time factory data collection system according to your shop floor needs. And to help you manage vast quantities of technical data, we developed our powerful IMAGE/1000 data base management system. Just a few simple keystrokes give you up-to-the-minute information on inventory levels or instrument check-out status. If you'd like a really clear picture of your information, HP's GRAPHICS/1000 will plot your data in a way you can understand: as a bar graph, pie chart, logarithmic graph, and more.

# nd from a computer,
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Here are just a few of HP's range of products for manufacturers and engineers:

1. HP 9845 Desktop Computer.
2. HP 9825 Desktop Computer.
3. HP 1000 Model 45 Real-time System with HP 7906 Disc Drive and HP 2648A Graphics Terminal.

4-6. HP 1000 F-, E-, and M-Series Computers.

7. HP 2108 Board Computer.
8. HP 7925 Mass Storage Unit.
9. HP 2240 Measurement & Control Processor.
10. HP ATS Automatic Test System.
11. HP 12050 Fiber Optics.
12. HP-IB Link IEEE-488 Standard Interface.
13. HP 2621 CRT Terminal.
14. HP 3075 Data Capture Terminal.
15. HP 3077 Time Reporting Terminal.
16. HP 3455 Voltmeter.
17. HP 3495 Scanner.
18. HP 5328A Universal Counter.
19. HP 5342 Microwave Frequency Counter.
20. HP 436A Power Meter.
21. HP 4262 LCR Meter.
22. HP 8566A Spectrum Analyzer.
23. HP 8754A Network Analyser.
24. HP 3325A Synthesizer/Function Generator.

25-6. HP 8660A & HP 8672A Synthesizer/Signal Generators.

27-8. HP 9876A & HP 2608 Printers.

29. HP 2631G Graphics Printer.
30. HP 7245A Thermal Plotter/Printer.
31. HP 7221A Plotter.
32. HP 7225A Graphics Plotter.
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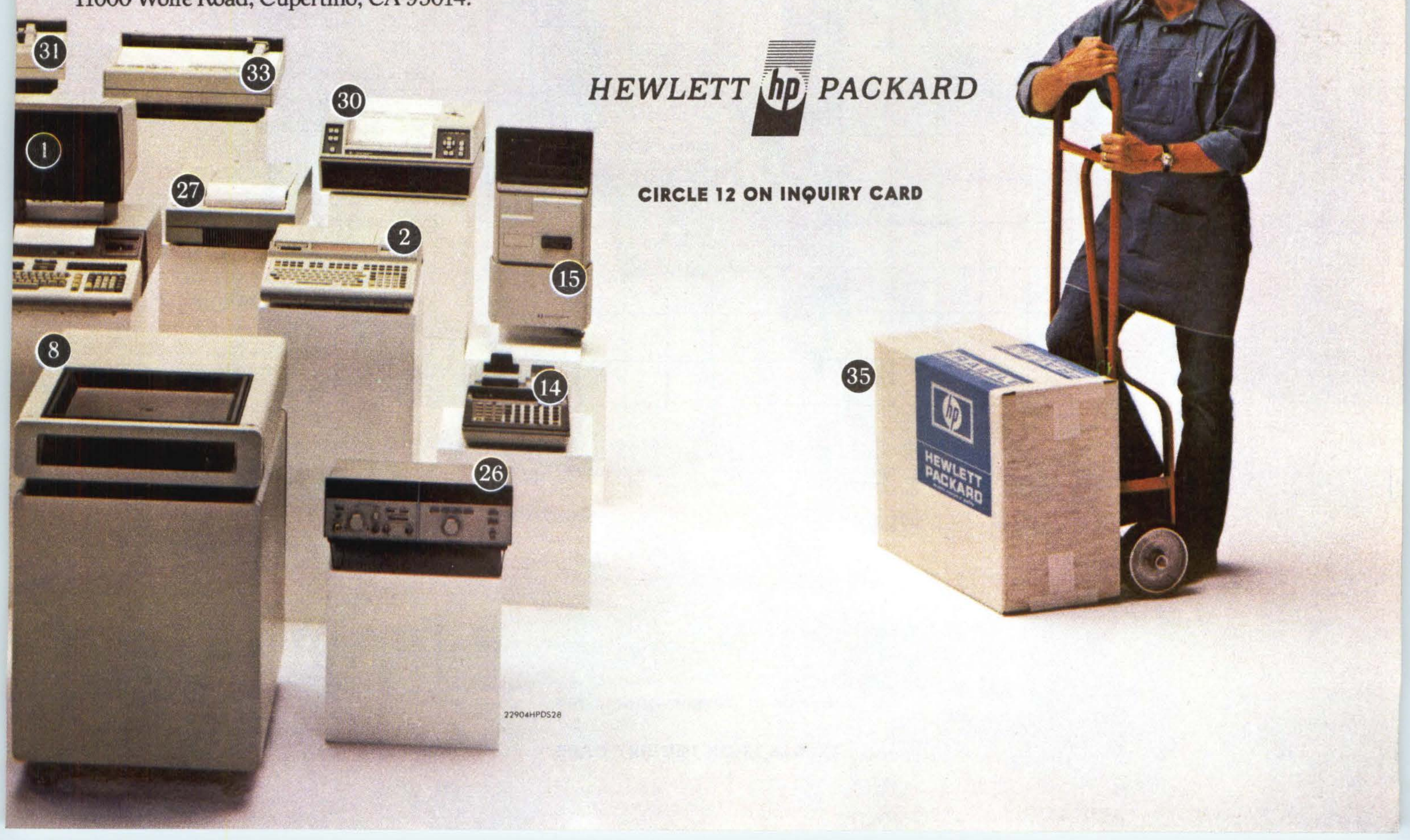



HEWLETT hp PACKARD

**CIRCLE 12 ON INQUIRY CARD**

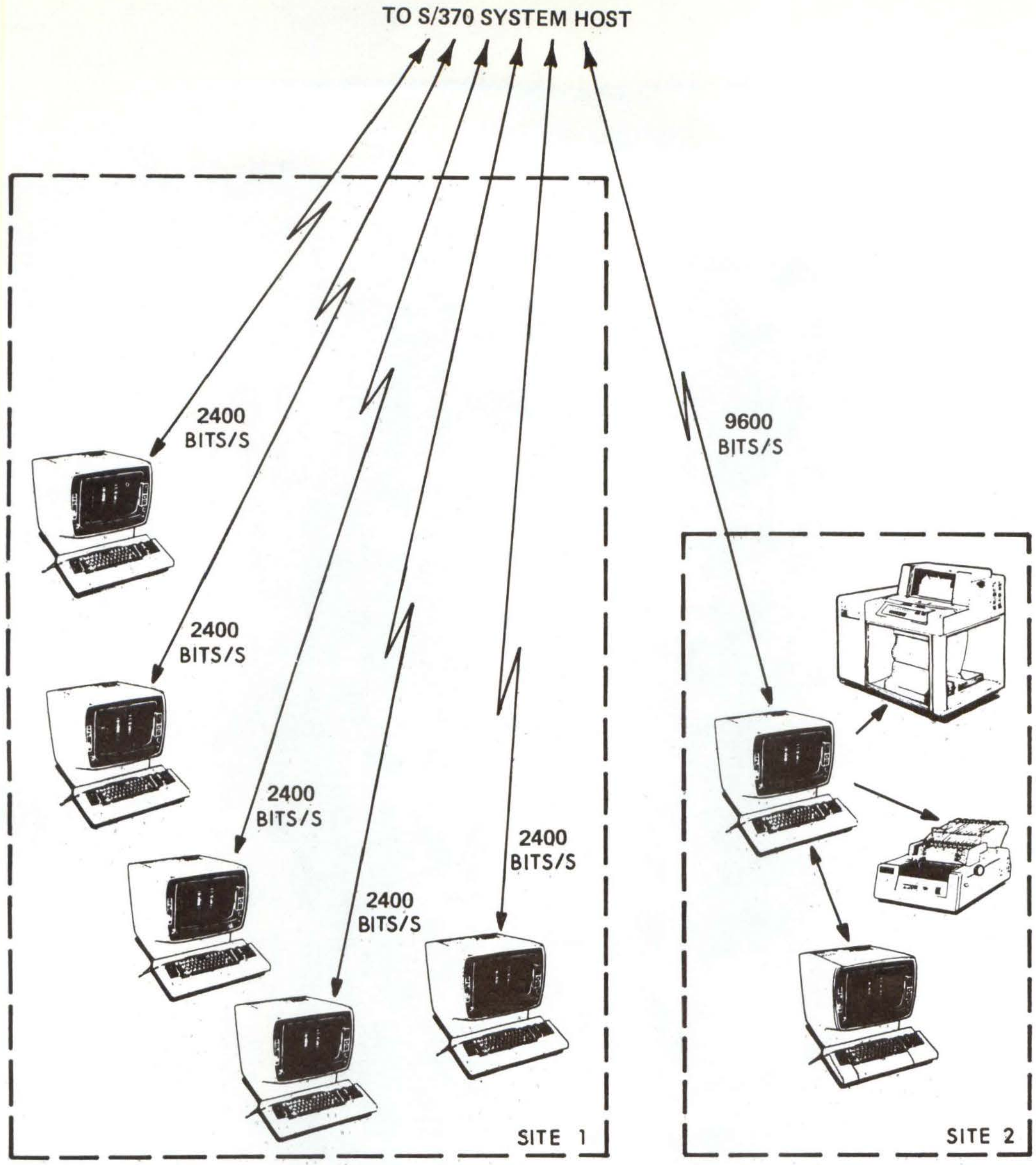



Fig 1 Centralized system concept. Single terminals (Site 1) and terminal clusters (Site 2) are each connected to central host site using 2400- and 9600-bit/s analog or digital data links. For simplicity, multidrops and concentrators are not included

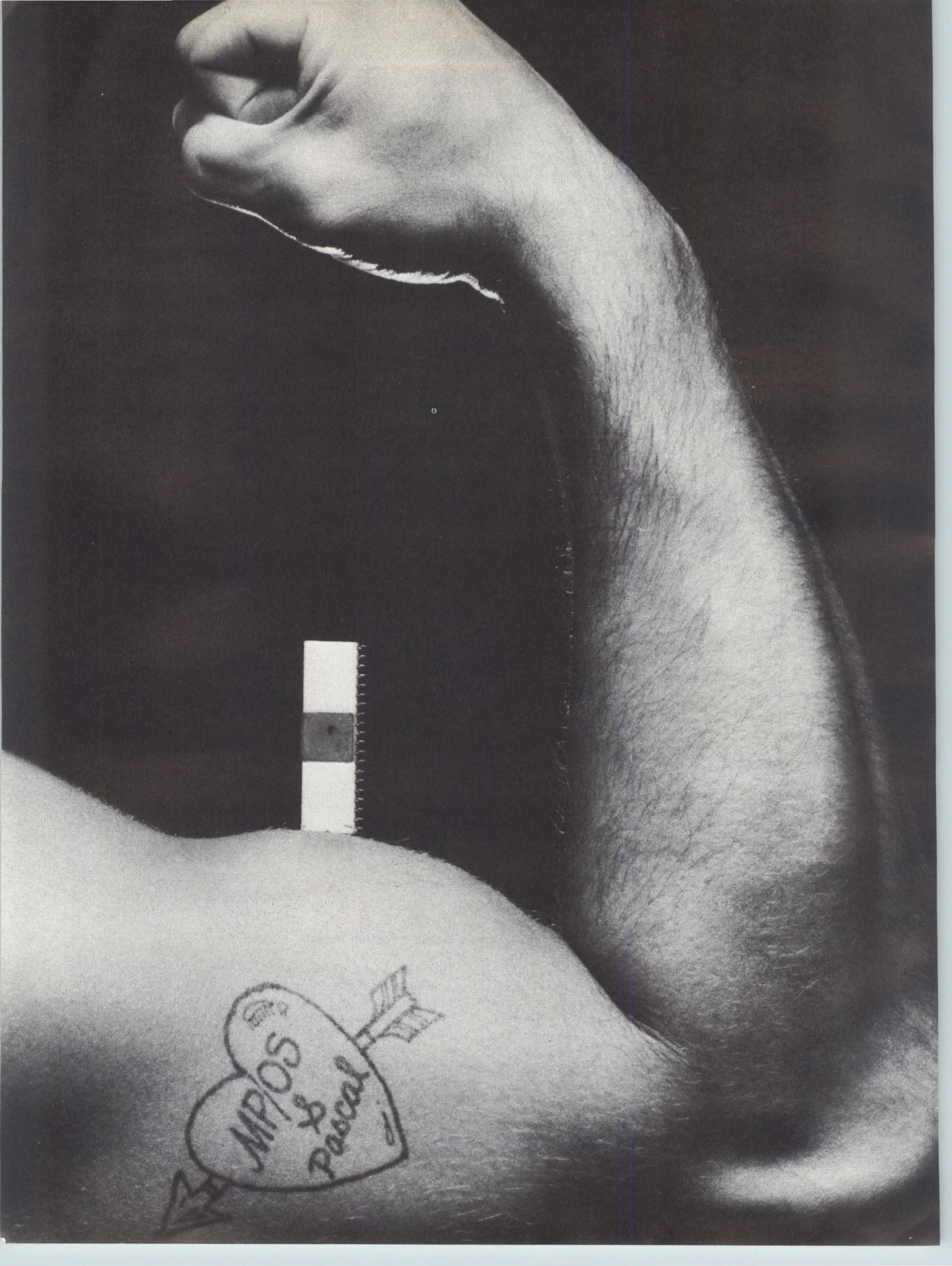
tributed within one or more buildings and operates at 9600 or 38,400 bits/s.

Multiple loops are provided and each can be installed with up to two miles (3.2 km) of cable. Every loop has a second lobe capability that can redrive each received loop signal onto another two miles of cable for extended onsite coverage. To provide offsite capability, a remote loop control unit is supplied that allows a loop attachment to the 8100 system via common carrier or PTT facilities and operates at 1200 or 2400 bits/s. Direct connection allows onsite point to point connections to terminals at up to 40′ (12.2 m) using the EIA RS-232-C interface standard and up to 1000′ (305 m) using the International Telegraph & Telephone Consultative Committee (CCITT) V.35 interface standard.

## Communication Design

Instead of using the more costly method of providing a separate design for each type of data link to accommodate the various communication facilities, the 8100 system design partitions the communication functions into three data link elements: interface hardware, control hardware, and control software (Fig 3). Families of elements are offered within each partition. This separation is important, because without it the data link interfaces would cause a proliferation of different hardware and software designs.

A significant aspect of the design effort defined an interface from which the family of data link interface hardware could be designed. A signal converter inter-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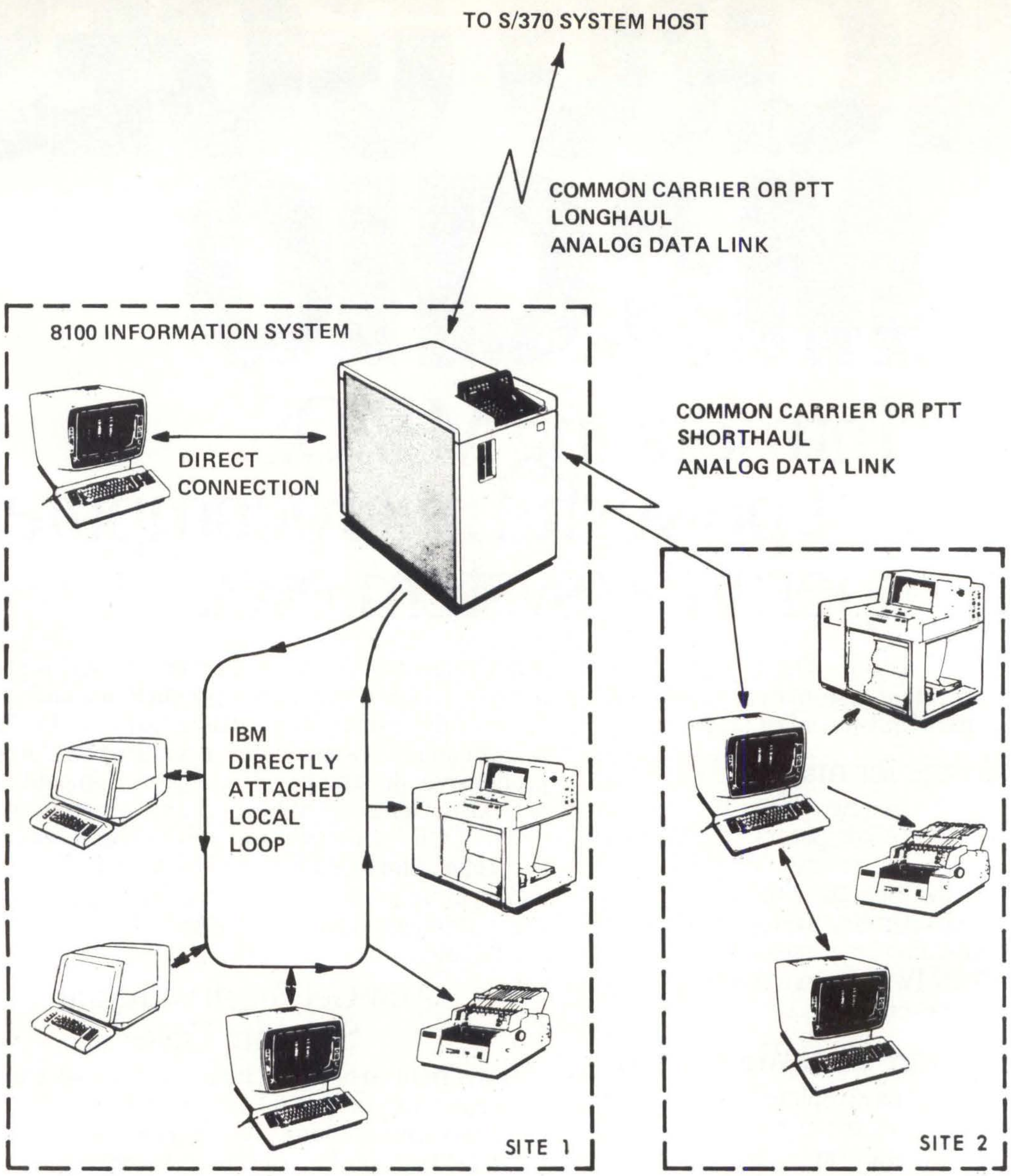


Fig 2 Distributed system concept. Processor is used between central system host and terminal sites. At terminal sites, directly attached SDLC loops and direct connections without data sets provide additional onsite communication flexibility

face is selected to incorporate the RS-232-C standard, plus additional control lines for maintenance. Only voltage level conversion is necessary for use with RS-232-C, CCITT V.24/V.28, and CCITT X.21 bis/V.28 interfaces. The CCITT V.35 interface hardware is the same except for the substitution of four balanced circuits for transmit, receive, and two clock lines. In addition to level conversion circuits, logic circuits were added to support the 8100 SDLC loop and the AT&T Dataphone[R] digital service (DDS) interface hardware.

### Data Link Interface Family

Another task of the design effort was to develop a data link interface hardware family having the signal converter interface on one side and the data link standard on the other (Fig 3). The data link hardware family is designed with a common logic card size and common card pin assignment to assure physical compatibility. The family of data link interfaces includes

(1) EIA RS-232-C, CCITT V.24/V.28, CCITT X.21 bis/V.28 interface. (These are different names for the same interface, depending on where used.) This interfaces external data circuit-terminating equipment (DCE) and is also used for direct connection to other data terminal equipment

(2) A 1200- or 600-bit/s integrated switched modem

(3) A 1200- or 600-bit/s integrated nonswitched modem

(4) An interface to the AT&T DDS channel service unit

(5) A CCITT V.35 interface to external DCE or for direct connection to other data terminal equipment


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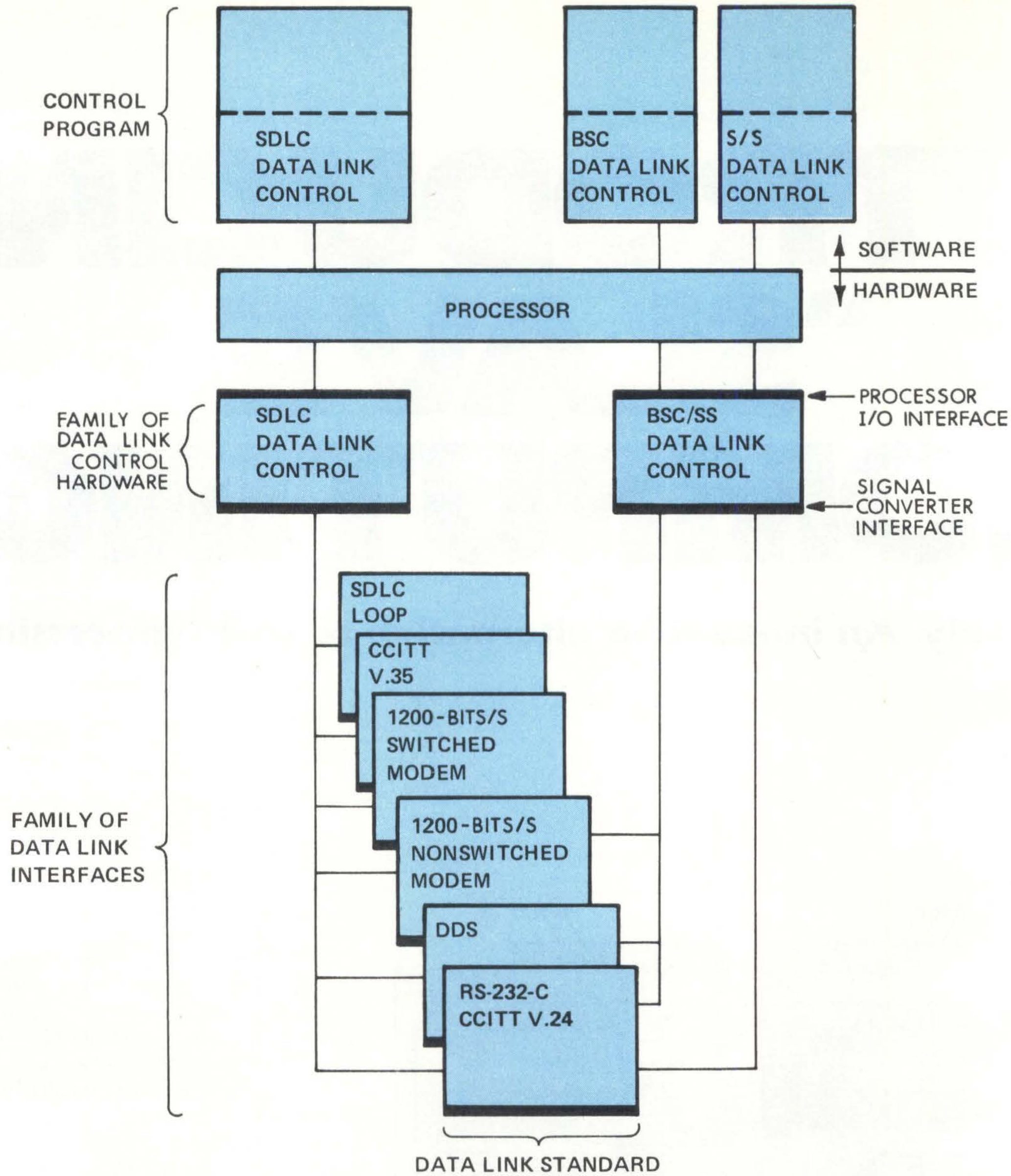


Fig 3 Communication design. System design is partitioned into three families: data link control software, data link control hardware, and data link interface hardware. One design from each family is required for each communication attachment.

(6) An interface to a directly attached (local) 8100 SDLC loop with second lobe capability.

This design facilitates the change from one data link interface to another. By exchanging one of the data link interface cards, the 8100 system can be connected to a different communication facility with the same data link protocol. For example, the distributed system configuration shown in Fig 2 has a remote 8100 system connected to a central system/370 host via common carrier or PTT long haul data link with modems. To migrate to AT&T's DDS, the RS-232-C interface hardware to the modem is removed, and the DDS interface hardware is inserted and connected to the AT&T channel service unit.

### Data Link Control

Both hardware and software are used in the design and implementation of data link control. Tradeoffs between hardware and software are determined by cost, performance, storage size, and protocol. Given these tradeoffs, the hardware is defined with two physical and electrical interfaces: the signal converter interface already mentioned on one side, and the input/output (I/O) bus of the 8100 processors on the other. Here again, all data link control hardware is designed to be physically compatible.

There are two different hardware implementations. The first supports binary synchronous communications (BSC) and start/stop (S/S) protocols. The second is for the SDLC protocol which is used with the IBM systems network architecture (SNA). Both implementations provide buffering, serialization, and deserialization, clocking to the modem when required, NRZI transformation, parity checking, bit timing, and an interval timer. This hardware maintains the signal converter interface and controls the number of bits/character. It also tests for and transmits the "break" condition.

SDLC hardware also provides channel I/O operation. This performance enhancement suspends processor instruction execution and uses the processor and its data paths to transfer information to and from storage. Without channel capability, data would have to be passed between storage and data link control hardware by execution of I/O instructions as is done in BSC and S/S hardware.

Tradeoffs moved SDLC software functions into hardware to increase performance and reduce processor utilization. This hardware logic provides recognition of the SDLC station address, generation and validation of the CCITT V.41 cyclic redundancy check polynomial, zero bit insertion and deletion, and recognition of the flag, abort, and idle bit sequences. When the total communication system is considered, the gain in performance and processor utilization justifies the added hardware cost.

Assume that the long haul data link in Fig 2 remains unchanged and the data link protocol is being changed from BSC to SDLC. In this case, one element of data link control hardware is exchanged, and the data link control software for SDLC replaces the BSC software. If another communication data link already uses the SDLC protocol, existing software can be shared with the new SDLC hardware. In this example, other parts of the control program are affected.


## Summary

Communications hardware design of the IBM 8100 information system provides the ability to select one of three data link protocols: SDLC, BSC, or S/S. The equipment can be attached to a variety of worldwide analog and digital networks by using one of two data link control elements and one of six data link interface elements (Fig 3). For the hardware designer, the number of different communications attachment designs has been reduced, and flexibility for network attachment has been achieved.


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(Turn to page 224 and find out.)


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ICC '79 will be remembered as having set several precedents: first for breaking all attendance records with a registration of over 2000, then for running an unprecedented fourth meeting day, which made necessary a new high for the conference record of four volumes.

An extensive technical program comprised 58 sessions and panel discussions, and some 320 technical paper presentations. The following summaries of a few of these papers are but indications of the growing interaction of computer and communications technologies.

### Digital Capabilities of Local Loops

All over the world digital technology is penetrating the telephone loop plant at an ever increasing rate. In due course, telephone administration plans call for evolution to an all-digital network, where digits providing voice and data services will be transmitted into the subscriber's premises. This raises the question, to what extent can the existing loop plant carry above voiceband digital signals?

Even, *et al*,[1] describe an investigation into this capability in terms of the longest loop over which a repeaterless system of acceptable cost can transmit these signals at a given (200k-bit/s) rate. The performance of a 4-wire digital line is used as a benchmark to compare that of three alternative 2-wire full duplex systems: hybrid balance, time compression multiplex, and frequency division multiplex.

Loop plant transmission capacity is governed by the following constraints: attenuation, inductive loading, gauge discontinuities, bridged taps, noise, and crosstalk. Inductive loading places severe limitations on the type of transmission under discussion, and this is therefore confined to consideration of nonloaded loops. Data available to characterize loop noise, especially impulse noise, are presently very limited. Other constraints can be compensated for by existing strategies of varying degrees of complexity.

Present day digital transmission is supported by three basic types of systems. (1) Loop pair gain, conceived for a purpose other than the systems under consideration here, uses T1 lines between central office (CO) and remote terminals for 4-wire, 1.544M-bit/s transmission. (2) Dataphone[R] service is used over the switched message network within the voice bandwidth of carrier trunk channels. Signal format is optimized for characteristics of these channels. (3) Private line digital data service (DDS) provides for up to 56k-bit maximum transmission over one of the 24 DSO channels of T1 interoffice facilities. Transmission range is limited to 24k ft (7.28 km) of 22-gauge cable. To supplement these offerings, local area data service (LADS), with selectable bit rates to 19.2 bits/s, is provided.

A 4-wire bipolar digital loop was implemented and its performance was used as a basis for comparison with the 2-wire options mentioned. All systems were assumed to have matched cable terminations, and were designed to provide full duplex transmission in the same 50-pair cable unit with 100% occupancy and a bit error rate not exceeding $10^{-7}$. All calculations were done on the basis of 22-gauge cable with no bridged tap. Performance limits of the 4-wire system are shown in Fig 1, with distance limits on the T1, DDS, and LADS systems included for comparison.

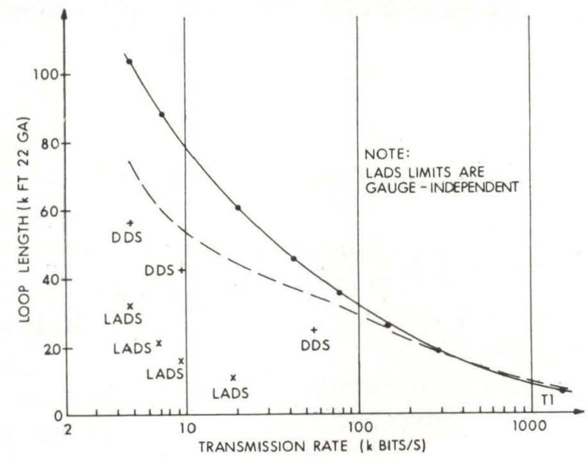


Fig 1 Length limits on 4-wire bipolar transmission.[1] Solid line is limit set by near-end crosstalk, dashed line limit imposed by equalizer gain. Limits on DDS, LADS, and T1 systems are shown for comparison

Results of the investigation showed that for a 200k-bit/s rate over 22-gauge cable, 4-wire baseband transmission is possible up to 24k ft (7.28 km); this system requires twice the cable length of the others under study. Up to 20k-ft (6.1-km) transmission is possible with the hybrid balance technique. The same result applies to a multigauge loop (ie, having gauge discontinuities) provided the system includes an echo canceller. Time compression and frequency division multiplex systems can each transmit 200k bits/s over 14k ft

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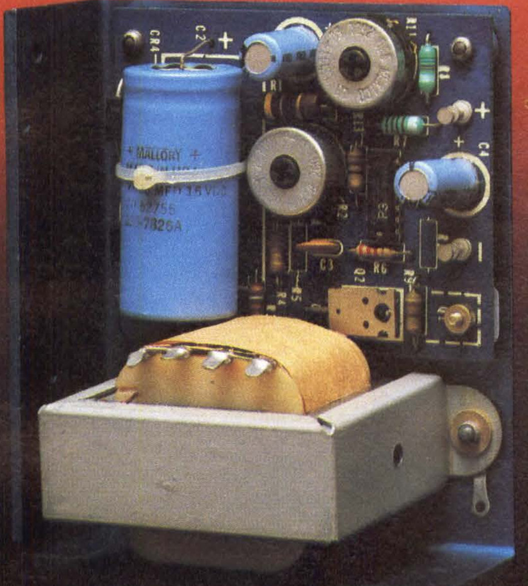

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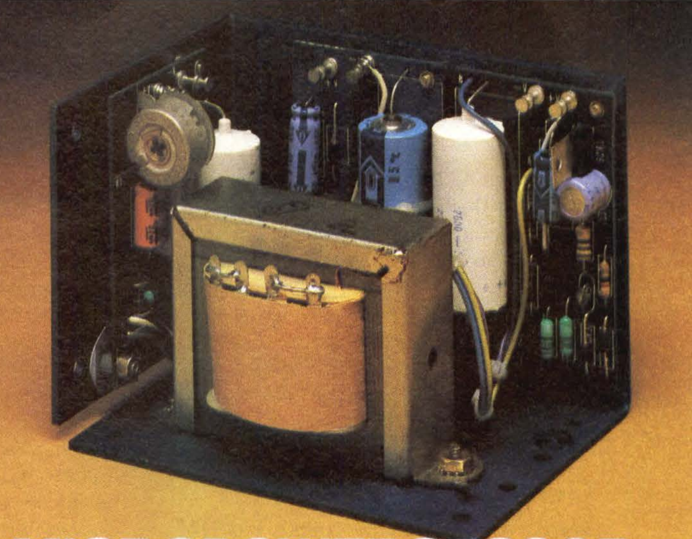

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CIRCLE 20 ON INQUIRY CARD

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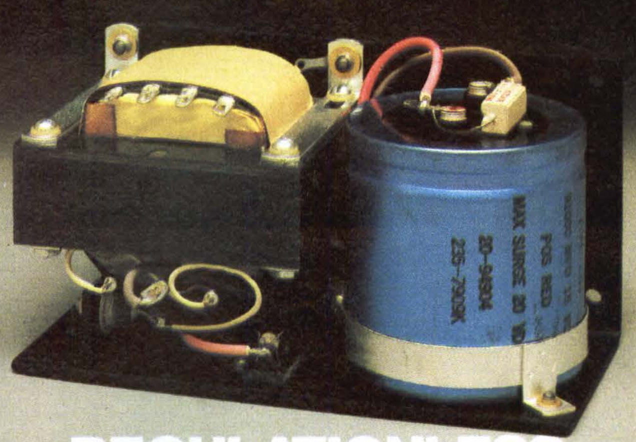
Wattage: 750 Watts
Temperature Coefficient: .02% C°
Overcurrent Protection: Automatic current limiting

# SWITCHERS


CIRCLE 21 ON INQUIRY CARD



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(4.24 km). The time compression system is the simpler of the two.

Additional characterization of impulse noise, which may be a limiting factor in system performance, is necessary. Maximum benefit from this new technology will also require careful spectrum management to avoid mutual interference among many different kinds of systems.

### Loop Plant Services Expansion

Harris Corp is prime contractor for design, development, and implementation of an enhanced urban communications system (EUCS), being marketed under the name TELDAT.[2] Basic function of the system is to expand the use of the twisted pair telephone distribution network. Additional services, such as alarm monitoring, remote utility meter reading, electrical energy management, opinion polling, interactive view data/video text type service, and digital data services are integrated in a manner transparent to the basic telephone service. Add-on services and the telephone can be in use simultaneously.

EUCS connects equipment at the home or business subscriber site to central office (CO) equipment through two technically different communications subsystem approaches, depending on the nature of the local loop. First approach is data above voice, using filters and modems to provide band separation and transmission of data over one twisted pair linking subscriber to CO. This technique cannot be used on loaded pairs or on loops using local carriers. The second approach uses the serving area concept (SAC) where feeder cables are

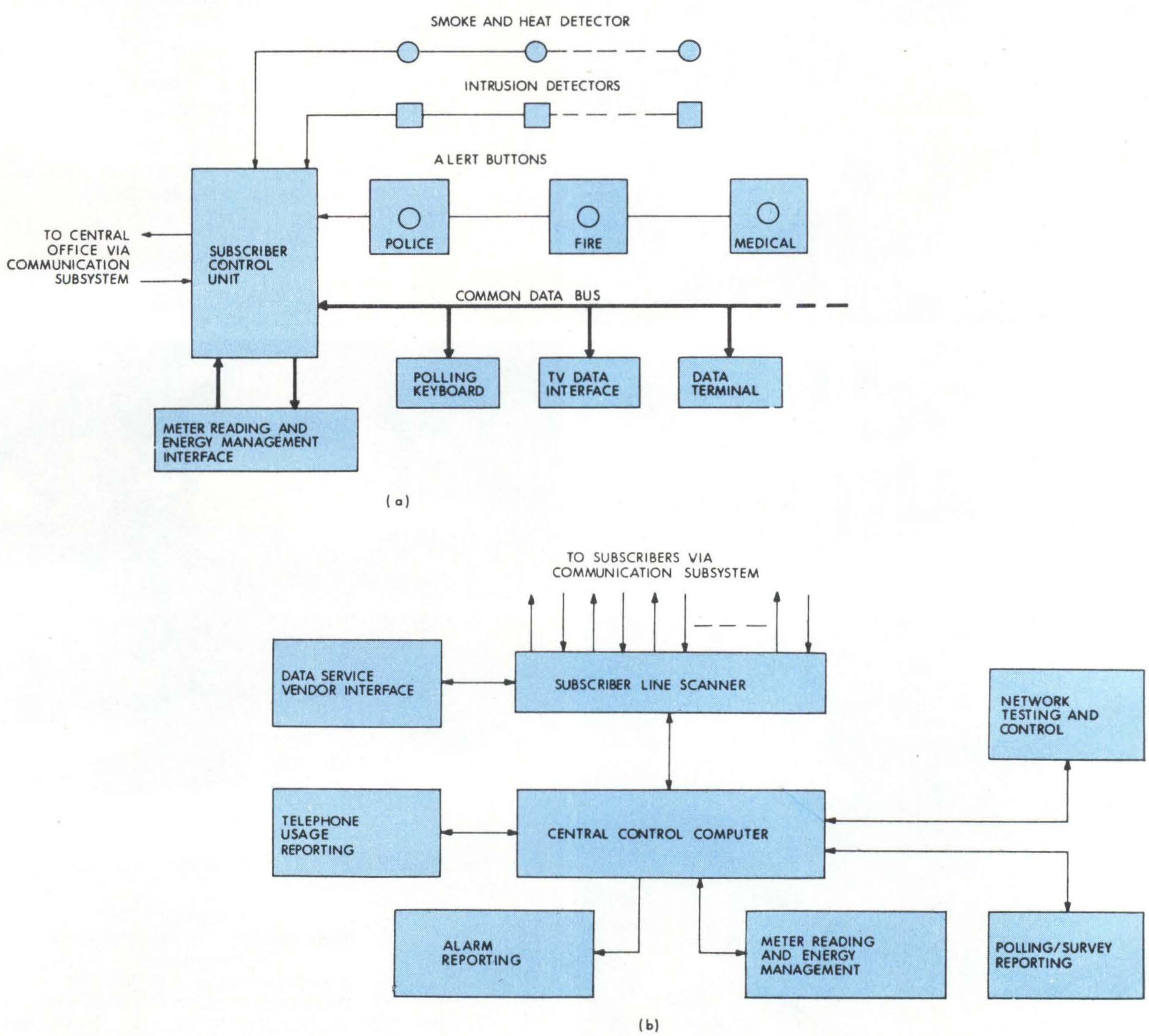


Fig 2 EUCS subscriber (a) and CO (b) communication subsystems.[2] Data bus at subscriber site, accessed by standard minijacks, allows for portable nature of some data services devices. Automatic network testing at the CO ensures proper functioning of all equipment

# PROMs

## ECL PROMs

| Organization | Part Number | Access Time (ns max) | Output | No. of Pins |
|---|---|---|---|---|
| 32 x 8 | MCM10139▲ | 25 | ECL output | 16 |
| 256 x 4 | MCM10149▲ | 30 | ECL output | 16 |

## TTL PROMs

| Organization | Part Number | Access Time (ns max) | Output | No. of Pins |
|---|---|---|---|---|
| 64 x 8 | MCM5003/5303▲ | 125 | Open collector | 24 |
| 64 x 8 | MCM5004/5304▲ | 125 | 2K pull-up | 24 |
| 512 x 4 | MCM7620▲ | 70 | Open collector | 16 |
| 512 x 4 | MCM7621▲ | 70 | 3-state | 16 |
| 512 x 8 | MCM7640▲ | 70 | Open collector | 24 |
| 512 x 8 | MCM7641▲ | 70 | 3-state | 24 |
| 1024 x 4 | MCM7642▲ | 70 | Open collector | 18 |
| 1024 x 4 | MCM7643▲ | 70 | 3-state | 18 |
| 1024 x 8 | MCM7680▲ | 70 | Open collector | 24 |
| 1024 x 8 | MCM7681▲ | 70 | 3-state | 24 |
| 2048 x 4 | MCM7684*▲ | 70 | Open collector | 18 |
| 2048 x 4 | MCM7685*▲ | 70 | 3-state | 18 |
| 2048 x 4 | MCM7686*▲ | 70 | Open collector with latches | 20 |
| 2048 x 4 | MCM7687*▲ | 70 | 3-state with latches | 20 |
| 2048 x 4 | MCM7688* | ---- | Open collector with registers | 20 |
| 2048 x 4 | MCM7689* | ---- | 3-state with registers | 20 |
| 1K x 8 | MCM76LS81* | 175 | 3-state | 24 |
| 1K x 8 | MCM82708*▲ | 70 | 3-state | 24 |

# EPROMs

## MOS EPROMs

| Organization | Part Number | Access Time (ns max) | No. of Power Supplies | No. of Pins |
|---|---|---|---|---|
| 1024 x 8 | MCM2708C▲ | 450 | 3 | 24 |
| 1024 x 8 | MCM27A08C▲ | 300 | 3 | 24 |
| 1024 x 8 | MCM68708C▲ | 450 | 3 | 24 |
| 1024 x 8 | MCM68A708C | 300 | 3 | 24 |
| 2048 x 8 | TMS2716C▲ | 450 | 3 | 24 |
| 2048 x 8 | TMS27A16C▲ | 300 | 3 | 24 |
| 2048 x 8 | MCM2716C*▲ | 450 | 1 | 24 |
| 2048 x 8 | MCM27A16C*▲ | 350 | 1 | 24 |
| 4096 x 8 | MCM2532C*▲ | 450 | 1 | 24 |
| 8192 x 8 | MCM68764C* | 450 | 1 | 24 |

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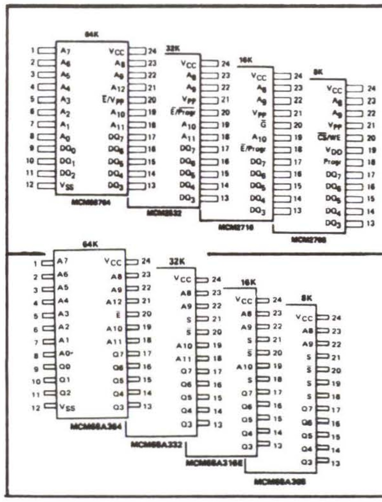

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# RAMs ROMs PROMs EPROMs

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# RAMs

## MOS DYNAMIC RAMs

| Organization | Part Number | Access Time (ns max) | No. of Power Supplies[1] | No. of Pins |
|---|---|---|---|---|
| 4096 x 1 | MCM4027AC-2▲ | 150 | 3 | 16 |
| 4096 x 1 | MCM4027AC-3▲ | 200 | 3 | 16 |
| 4096 x 1 | MCM4027AC-4▲ | 250 | 3 | 16 |
| 4096 x 1 | MCM6604AC | 350 | 3 | 16 |
| 4096 x 1 | MCM6604AC-2 | 250 | 3 | 16 |
| 4096 x 1 | MCM6604AC-4 | 300 | 3 | 16 |
| 16,384 x 1 | MCM4116BC-15▲ | 150 | 3 | 16 |
| 16,384 x 1 | MCM4116BC-20▲ | 200 | 3 | 16 |
| 16,384 x 1 | MCM4116BC-25▲ | 250 | 3 | 16 |
| 16,384 x 1 | MCM4116BC-30▲ | 300 | 3 | 16 |
| 16,384 x 1 | MCM4516L-15*▲ | 150 | 1 | 16 |
| 65,536 x 1 | MCM6664L-20*▲ | 200 | 1 | 16 |

## TTL BIPOLAR RAMs

| Organization | Part Number | Access Time (ns max) | Output | No. of Pins |
|---|---|---|---|---|
| 256 x 4 | MCM93412*▲ | 45 | Open collector | 22 |
| 256 x 4 | MCM93422*▲ | 45 | 3-state | 22 |
| 1024 x 1 | MCM93415▲ | 45 | Open collector | 16 |
| 1024 x 1 | MCM93425▲ | 45 | 3-state | 16 |

*To be introduced.
▲Second source.
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## MOS STATIC RAMs

| Organization | Part Number | Access Time (ns max) | No. of Power Supplies | No. of Pins |
|---|---|---|---|---|
| 128 x 8 | MCM6810 | 450 | 1 | 24 |
| 128 x 8 | MCM68A10 | 360 | 1 | 24 |
| 128 x 8 | MCM68B10 | 250 | 1 | 24 |
| 1024 x 1 | MCM2115AL-70*▲ | 70 | 1 | 16 |
| 1024 x 1 | MCM2115AL-45*▲ | 45 | 1 | 16 |
| 1024 x 1 | MCM2125AL-70*▲ | 70 | 1 | 16 |
| 1024 x 1 | MCM2125AL-45*▲ | 45 | 1 | 16 |
| 1024 x 4 | MCM2114P-20▲ | 200 | 1 | 18 |
| 1024 x 4 | MCM2114P-25▲ | 250 | 1 | 18 |
| 1024 x 4 | MCM2114P-30▲ | 300 | 1 | 18 |
| 1024 x 4 | MCM2114P-45▲ | 450 | 1 | 18 |
| 1024 x 4 | MCM21L14P-20▲ | 200 | 1 | 18 |
| 1024 x 4 | MCM21L14P-25▲ | 250 | 1 | 18 |
| 1024 x 4 | MCM21L14P-30▲ | 300 | 1 | 18 |
| 1024 x 4 | MCM21L14P-45▲ | 450 | 1 | 18 |
| 4096 x 1 | MCM6641P-20▲ | 200 | 1 | 18 |
| 4096 x 1 | MCM6641P-25▲ | 250 | 1 | 18 |
| 4096 x 1 | MCM6641P-30▲ | 300 | 1 | 18 |
| 4096 x 1 | MCM6641P-45▲ | 450 | 1 | 18 |
| 4096 x 1 | MCM66L41P-20▲ | 200 | 1 | 18 |
| 4096 x 1 | MCM66L41P-25▲ | 250 | 1 | 18 |
| 4096 x 1 | MCM66L41P-30▲ | 300 | 1 | 18 |
| 4096 x 1 | MCM66L41P-45▲ | 450 | 1 | 18 |
| 4096 x 1 | MCM2147C-55*▲ | 55 | 1 | 18 |
| 4096 x 1 | MCM2147C-70*▲ | 70 | 1 | 18 |
| 4096 x 1 | MCM2147C-85*▲ | 85 | 1 | 18 |

## CMOS STATIC RAMs

| Organization | Part Number | Access Time (ns max) | No. of Power Supplies | No. of Pins |
|---|---|---|---|---|
| 256 x 4 | MCM5101-1▲ | 450 | 1 | 22 |
| 256 x 4 | MCM5101-3▲ | 650 | 1 | 22 |
| 256 x 4 | MCM5111-8▲ | 800 | 1 | 22 |
| 4096 x 1 | MCM6504-45*▲ | 450 | 1 | 18 |
| 1024 x 1 | MCM6508-46*▲ | 460 | 1 | 16 |
| 1024 x 1 | MCM6508-30*▲ | 300 | 1 | 16 |
| 1024 x 1 | MCM6518-46*▲ | 460 | 1 | 18 |
| 1024 x 1 | MCM6518-30*▲ | 300 | 1 | 18 |

## ECL BIPOLAR RAMs

| Organization | Part Number | Access Time (ns max) | Output | No. of Pins |
|---|---|---|---|---|
| 8 x 2 | MCM10143 | 15 | ECL output | 24 |
| 256 x 1 | MCM10144▲ | 26 | ECL output | 16 |
| 16 x 4 | MCM10145▲ | 15 | ECL output | 16 |
| 1024 x 1 | MCM10146▲ | 29 | ECL output | 16 |
| 128 x 1 | MCM10147▲ | 15 | ECL output | 16 |
| 256 x 1 | MCM10152▲ | 15 | ECL output | 16 |
| 256 x 4 | MCM10422*▲ | 10 | ECL output | 24 |

# ROMs

## MOS STATIC ROMs

### Character Generators[2]

| Organization | Part Number | Access Time (ns max) | No. of Power Supplies | No. of Pins |
|---|---|---|---|---|
| 128 x (7 x 5) | MCM6670P | 350 | 1 | 18 |
| 128 x (7 x 5) | MCM6674P | 350 | 1 | 18 |
| 128 x (9 x 7) | MCM66700P▲ | 350 | 1 | 24 |
| 128 x (9 x 7) | MCM66710P▲ | 350 | 1 | 24 |
| 128 x (9 x 7) | MCM66714P▲ | 350 | 1 | 24 |
| 128 x (9 x 7) | MCM66720P▲ | 350 | 1 | 24 |
| 128 x (9 x 7) | MCM66730P▲ | 350 | 1 | 24 |
| 128 x (9 x 7) | MCM66734P | 350 | 1 | 24 |
| 128 x (9 x 7) | MCM66740P▲ | 350 | 1 | 24 |
| 128 x (9 x 7) | MCM66750P▲ | 350 | 1 | 24 |
| 128 x (9 x 7) | MCM66760P▲ | 350 | 1 | 24 |
| 128 x (9 x 7) | MCM66770P | 350 | 1 | 24 |
| 128 x (9 x 7) | MCM66780P | 350 | 1 | 24 |
| 128 x (9 x 7) | MCM66790P | 350 | 1 | 24 |

### Binary ROMs

| Organization | Part Number | Access Time (ns max) | No. of Power Supplies | No. of Pins |
|---|---|---|---|---|
| 1024 x 8 | MCM68A30P8 | 350 | 1 | 24 |
| 1024 x 8 | MCM68A308P7 | 350 | 1 | 24 |
| 2048 x 8 | MCM68A316P91 | 350 | 1 | 24 |
| 1024 x 8 | MCM68B30AP▲ | 250 | 1 | 24 |
| 1024 x 8 | MCM68A30AP▲ | 350 | 1 | 24 |
| 1024 x 8 | MCM68B308P▲ | 250 | 1 | 24 |
| 1024 x 8 | MCM68A308P▲ | 350 | 1 | 24 |
| 2048 x 8 | MCM68A316EP▲ | 350 | 1 | 24 |
| 2048 x 8 | MCM68A316AP▲ | 350 | 1 | 24 |
| 4096 x 8 | MCM68A332P▲ | 350 | 1 | 24 |
| 4096 x 8 | MCM68A332P2 | 350 | 1 | 24 |
| 8192 x 8 | MCM68A364P*▲ | 350 | 1 | 24 |
| 8192 x 8 | MCM68A364P3* | 350 | 1 | 24 |
| 8192 x 8 | MCM68B364P*▲ | 250 | 1 | 24 |

## CMOS ROM

| Organization | Part Number | Access Time (ns max) | No. of Power Supplies | No. of Pins |
|---|---|---|---|---|
| 256 x 4 | MCM14524 | 1200 | 1 | 16 |

run to a distribution box serving several hundred local subscribers. EUCS signals are sent over the commonly provided spare distribution pair from subscriber to distribution point, where they are multiplexed and transmitted via a T1 carrier line to the CO.

EUCS subscriber and CO subsystems are shown in Fig 2. Dedicated wiring connects fixed location sensors and monitors at the subscriber premises to the subscriber control unit (SCU). A common data bus makes data services available at several locations and allows for flexibility in adding or changing services. Microprocessor based SCU formats and coordinates communication with the CO and provides self-test and subsystem test capabilities.

At the CO, the control computer exercises master control over the system and recognizes, verifies, and reports the various inputs from the subscriber site.

Extensive implementation of control functions in both software and modular hardware allow for system growth in terms of both services and number of subscribers served.

### Network Synchronization

Considerations such as the impact on customer service due to the synchronization plan, choice of synchronization strategy, and the current state of the art in the field of timing resources govern the development of a suitable plan for synchronizing a switched digital communication network. Abate *et al*[3] trace the performance objective of each of the components of the network back to the service objective, from the point of view of the customer.

When design or malfunctions result in imperfect synchronization, information bits are repeated or lost; such events are called "slips." Because of the format of the DS-1 1.544M-bit/s digital signal, voice band signals fall into an area of controlled slips and are either inaudible or are perceived by the human ear as clicks—or, at worst, as variations in apparent pitch. In data transmission, however, the effects of slips, controlled or not, could range from a single error to several seconds of lost transmission. Therefore the slip rate objective of the network is based on the impact of slips on data customers, and has resulted in an end to end objective of one slip in five hours.

The simplest way to achieve this is to use stable clocks at each network node, but the slip rate objective here would require the use of costly atomic clocks. The economic burden of this method is prohibitive. Another method would be to use a separate network, such as those being used for navigation and other services. These, however, not being specifically charged with the communications responsibility, could not be regarded as dependable. Pulse stuffing, a method in use for high bit rate systems for a long time, requires neither a timing distribution net nor accurate clocks. For a switched digital network, however, the cost of processing each low speed signal as it passes through each node would again be prohibitive. A master-slave clock distribution system using the communication links themselves for timing reference distribution is chosen as the one best suited for the North American switched digital network.

The plan is for each network node, in most cases a switching office, to use an existing digital trunk to derive timing reference from another node called the master, and its clock will be "slaved" to the master. The master and selected trunk used for such timing is called the primary synchronization reference (Fig 3). A node serving as master is in turn slaved to another reference, so that the entire system has a tree-like hierarchic structure, at the apex of which is the Bell System Reference Frequency (BSRF). BSRF is distributed to the timing regions as shown in Fig 4.

BSRF is derived from a primary standard consisting of three cesium oscillators located in Hillsboro, Mo. Each provides an accuracy of one part in $10^{11}$. BSRF transmits reference frequencies of 2.048 and 20.48 MHz nationwide over certain analog cable and radio facilities.

For those toll offices not directly connected to BSRF, another toll switch with a very stable clock, such as a No 4 ESS, will be used as master, and may be regarded as a digital extension of BSRF. These extensions will be referred to as the reference distribution system (RDS), and will be available to provide timing to any interconnected node. Short outages within RDS will have little or no effect, since No 4 ESS local oscillators allow 16 days of reference outage while still meeting the slip rate objective.

Operation of such an extensive timing network is one in which there is little experience. Rapid detection of trouble and restoral of proper operation are essential. The objective of a low slip rate under normal operating conditions will be helpful by providing a high contrast background against which troubles can be perceived.

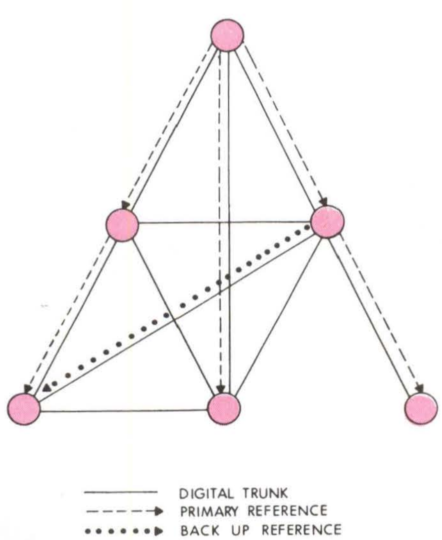


Fig 3 Master-slave synchronization.[3] Alternate transmission paths and alternate masters are provided to guard against failures within the distribution plan

### Local Computer Networks

Interest and activity in the field of local computer networks (LCNs) has been rapidly developing in the past few years. Nonetheless, to this point in time, no precise definition of an LCN has emerged. In this survey of the field, Freeman and Thurber[4] define LCNs as a class of systems that meet the following basic criteria: (a) generally owned by a single organization, (b) generally local, covering distances on the order of a few miles, and (c) that generally contain some form of switching element technology.

Two different stimuli lie behind the interest in LCNs. One comes from those who wish to improve their current systems, and the other from groups who want to incorporate new system concepts. Categorization of LCNs is not easy because the difference between them and distributed processors or geographically distributed networks may be one of degree rather than kind.

In attempting to describe LCNs, a taxonomy tree (Fig 5) of LCN architectures and currently identified systems from each category was developed. These systems are examined from the point of view of design and

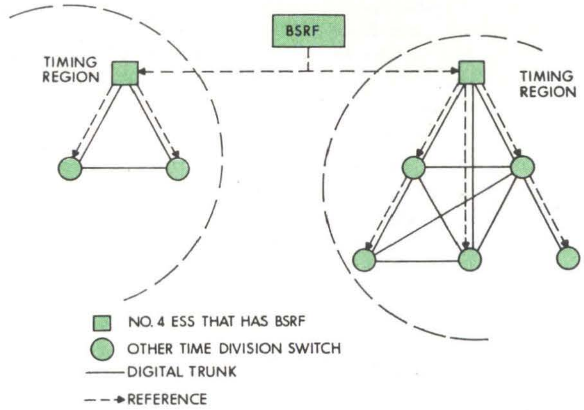


Fig 4 Timing regions.[3] Within each region a digital toll office will serve as regional master, and uses only BSRF as its reference

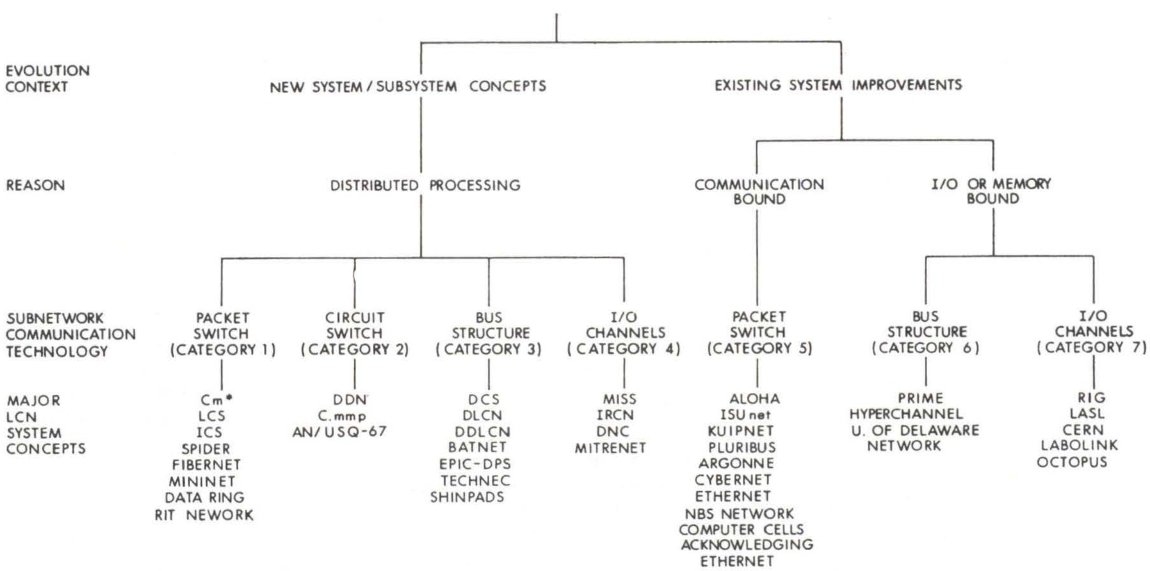


Fig 5 LCN taxonomy and systems.[4] While LCNs have a communications subnetwork, some use subnetwork designs which encompass not only packet and circuit switching, but also I/O channel and bus structures. These structures are legitimate technologies for the communications subnetwork because they are very cost competitive in short distance applications

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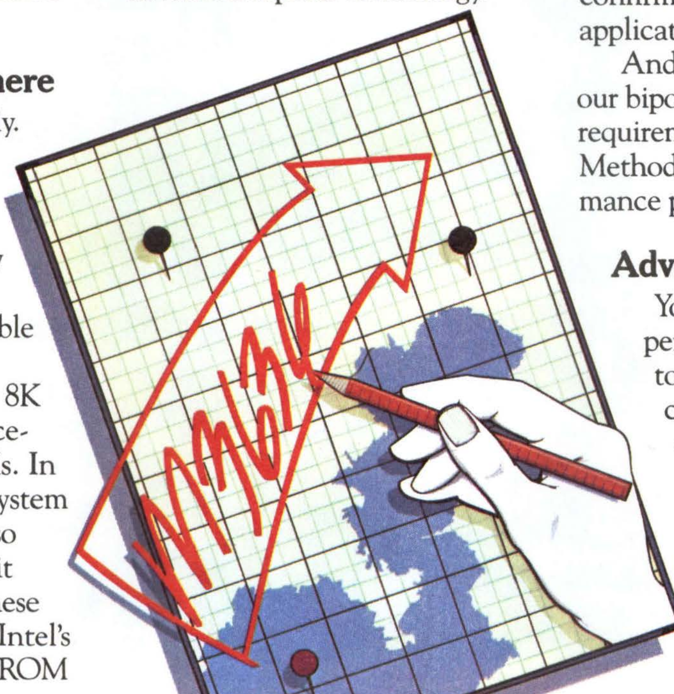

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|---|---|---|---|
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**CIRCLE 45 ON INQUIRY CARD**

operational issues, grouped and summarized by network components (both hardware and software), configurations of these components, network operation, performance, and user-oriented concerns. An extensive reference to current LCN systems is included.

### References


All references are included in the ICC '79 Conference Record.

1. R. K. Even, R. A. McDonald, H. Seidel, "Digital Transmission Capacity of the Loop Plant," Vol 1, pp 2.1.1-2.1.7
2. E. J. Claire, "A Multiple Service Broadband System for the Existing Telephone Local Loop," Vol 1, pp 2.2.1-2.2.4
3. J. E. Abate, C. A. Cooper, J. W. Pan, and I. J. Shapiro, "Synchronization Considerations for the Switched Digital Network," Vol 1, pp 11.5.1-11.5.4
4. H. A. Freeman and K. J. Thurber, "Issues in Local Computer Networks,", Vol 2, pp 20.3.1-20.3.5

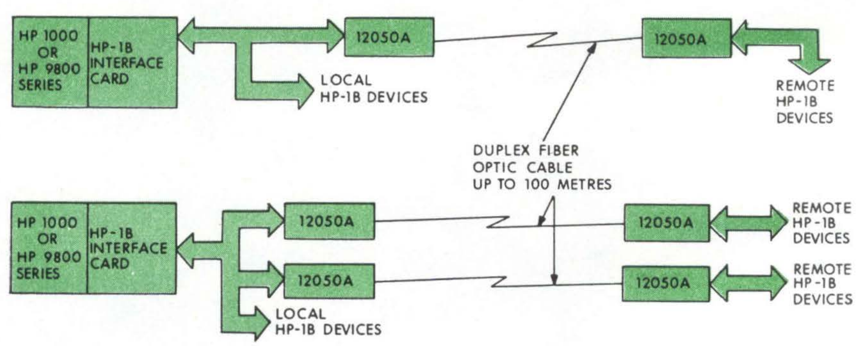

Copies of the ICC '79 Conference Record are available from IEEE Single Copy Sales, 445 Hoes Lane, Piscataway, NJ 08854. Order by IEEE catalog number 79CH1435-7 CSCB at $50 each set of four volumes.

## Fiber Optic Link Extends Standard Instrumentation Interface Bus

Overcoming previous HP-IB* distance requirements, the 12050A fiber optic HP-IB link permits separation of up to 100 m between HP-IB compatible devices and associated computer-controller. The remote instrumentation interface uses a dual-channel fiber optic cable for bidirectional 20k-byte/s data transfer between distant sites. One unit, functioning as transmitter/receiver, is required at each end of the link. According to Hewlett-Packard Data Systems Div, 11000 Wolfe Rd, Cupertino, CA 95014, the inherent noise immunity and electrical properties of the fiber optic transmission medium make the link especially suited to severe environment industrial applications.

Bit-parallel signals are accepted from any IEEE-488 compatible controller through the standard 24-conductor connector and are converted to bit-serial light pulses These are transmitted via the cable to a remote 12050A that reconverts them to the standard bit-parallel form and makes them available through a standard port to compatible instruments or instrument clusters. Using standard HP-IB programming techniques, the devices communicate remotely as they would in local operation; no additional software development is needed. There is no system degradation when extending the bus length with the link. 12050A units support all HP-IB functions except parallel poll and pass control.

Interrupts can be detected in realtime, typically within 100 μs. An onboard silicon-on-sapphire (SOS) microprocessor performs self test automatically at power-on, or upon request from a user program. The microprocessor also detects transmitted errors during communication using a checksum algorithm, and if necessary retransmits without computer intervention until transfer is successfully completed.




Typical fiber optic HP-IB link configurations. Multiple point to point configurations can be used to locate instrumentation at more than one remote site depending on computer used. Each 12050A counts as one device for each computer HP-IB interface card

Preassembled and tested connectorized cables (39200 series) come in simplex or duplex versions, with two simplex or one duplex cable required per system. Cables are of fused silica, slightly graded index, 140-μm dia glass-clad fiber, surrounded by silicone coating, buffer jacket, and tensile strength members, with a polyurethane outer jacket. Cable is available in any of five lengths from 10 to 100 m.

Price of each 12050A unit (U.S.) is $1950. Dual-channel cable in connectorized lengths of 100 m is priced at $8.50/m. □

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*HP-IB, Hewlett-Packard interface bus, is the company's implementation of IEEE Standard 488-1978 instrumentation interface




See page 112


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# TECHNOLOGY AND ECONOMICS
# SYSTEM PERFORMANCE AND WORKLOADS

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In establishing processor, bus, memory, channel, controller, and peripheral equipment characteristics, and in planning and developing system software, the designer must be aware of those system and workload features that have the greatest influence on throughput and turnaround time. A simple model can provide helpful insight.

### Determining Throughput and Turnaround Time

Assume a system with a processor and I input/output channels. Suppose that each channel has a data rate D′/I bytes/s, for a total I/O rate of D′, and that the processor itself has an average computing rate of C′ operations/s.

Specify the characteristics of this system's workload as requiring the processing of a total of D bytes (the total number of input and output characters), each of which on the average requires s computer operations for processing.[1,2] Finally, specify that program and database bytes must be handled by the system as well as I/O bytes, and that the operating system may cause multiple I/O transfers. For these reasons, total bytes transferred is kD, with $k > 1$.

In the worst case—a simple system with only one job processed at a time—we see that time to complete one job equals compute time plus I/O time

$$T = \frac{sD}{C'} + \frac{kD}{D'} = D\left[\frac{s}{C'} + \frac{k}{D'}\right]$$

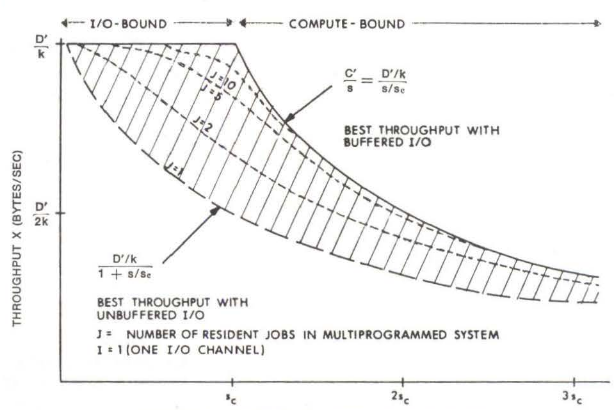


Fig 1 System throughput as function of workload. As measured by s, workload is number of computer operations required for each I/O byte processed. If s is less than critical value $s_c$, system is I/O-bound; if s is greater than $s_c$, system is compute-bound. With only one program in system, throughput vs s follows lower, dashed curve; with multiprogramming and large number of resident programs, it tends to follow upper solid line. Intermediate lines show throughput variation for 2, 5, and 10 resident jobs

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The job execution rate can be expressed as

$$\text{Throughput} = X = \frac{D}{T} = \frac{D'/k}{1 + s\,\frac{D'}{kC'}}$$

If we define

$$s_c = \frac{kC'}{D'}$$

then

$$X = \frac{D'/k}{1 + \frac{s}{s_c}}$$

This equation is plotted as the dashed line in Fig 1.

Next, suppose that an unlimited number of jobs can reside in the system, so that I/O channels are always working to full capacity. To determine the throughput under these circumstances, consider these two cases:

(1) I/O time is greater than compute time; ie, $kD/D' > sD/C'$, or $s < s_c$. Then the system is I/O-limited and throughput is

$$X = \frac{D}{\text{I/O time}} = \frac{D}{kD/D'} = \frac{D'}{k} \text{ bytes/s}$$

(2) Compute time is greater than I/O time; ie, $s > s_c$. Then the system is compute-bound and throughput is

$$X = \frac{D}{\text{Compute time}} = \frac{D}{sD/C'} = \frac{C'}{s} = \frac{D'/k}{s/s_c} \text{ bytes/s}$$

Compute-bound and I/O-bound equations are plotted as solid lines in Fig 1.

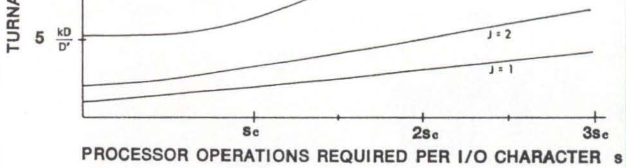



Fig 2 Turnaround time. Duration of interval which starts when job is read into system and ends when last results have been output, turnaround time increases with s and with multiprogramming level J. Adding jobs to make system more productive results in delayed output

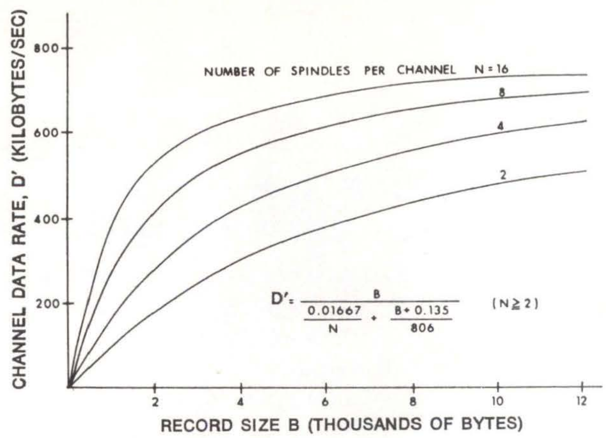
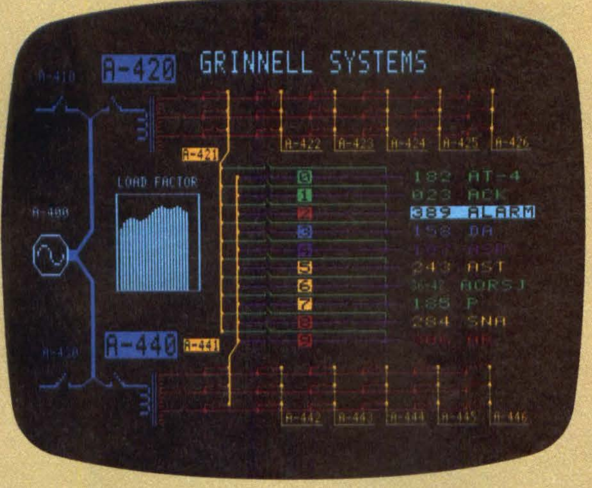


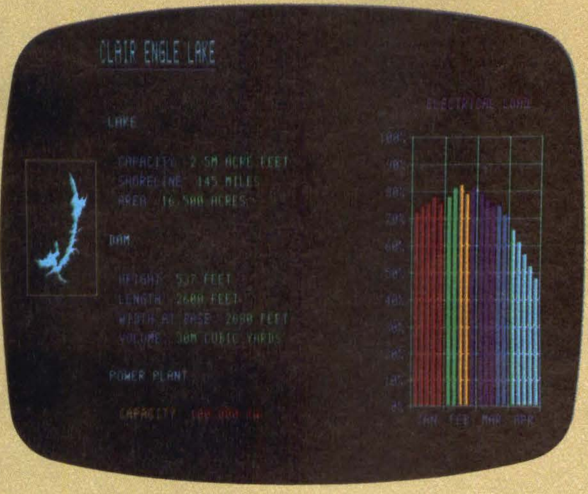

Fig 3 Effects of multiple channels on data rate. Data rate from N IBM 3330s connected to block multiplexer channel is function of N and of block size B. For given N, data rate increases with increasing block size because proportionally less time is spent reading fixed number of format bytes which precede each record. For given B, data rate increases with increasing N because less time is lost waiting for next record to rotate into position under read heads. Even with large values of B and N, data rate is significantly less than maximum instantaneous rate of 806k bytes/s. Note that, for given block size: (1) doubling number of spindles per channel results in less than double data rate; (2) doubling number of channels for *fixed* total number of spindles results in less than double data rate. With four spindles at B = 3k bytes, for example, data rate on single channel is 370k bytes/s, while rate on two channels of two spindles each is 2 x 245 = 490k bytes/s

In a typical system today there will be some degree of multiprogramming, and actual throughput will be somewhere in the shaded area of Fig 1, depending on the statistical characteristics of the workload. In a recent paper, Denning and Buzen[3] have shown how to calculate throughput for various levels of multiprogramming. Assume that the system contains a fixed number of jobs J; jobs may be queued at the processor and at each I/O device, and are handled on a first in, first out basis; a job alternates between channels and processor, with each channel handling kD/I characters in an average time $(kD/I) \div (D'/I) = kD/D'$, and the processor manipulating those characters in an average time $sD/C'I$; and the service time at the processor and each channel is given by an exponentially distributed random variable. From this we can compute throughput as a function of the number of jobs J and the number of I/O channels I. The result for $I = 1$ and $J = 2, 5$, and $10$ is shown as dotted lines in Fig 1.

Denning and Buzen also show that it is easy to compute job turnaround time from throughput. First they note that, since each job requires the processing of D bytes, throughput of X bytes/s is equivalent to X/D

# Vector graphics. OEM prices.




Now, with Grinnell's GMR-37 graphic display systems, you can have the resolution and input advantages of dot matrix television for about the same price as more limited character-based systems.

And, every GMR-37 display is a complete operating system: display generator, MOS refresh memory, vector and rectilinear graphics, alphanumerics in 4 sizes, bi-directional RS-232 computer interface and RS-170 video interface. Systems, including power supplies, are housed in a 7″, rack-mountable chassis and drive standard closed circuit monitors.

Four basic GMR-37 models can be tailored to fit into almost any computer-based system. Here are just a few examples. (Prices are F.O.B. San Jose, and quantity discounts are available. TV monitors are extra.):

## GMR 37-20: $3700
256 x 512 resolution, one channel RGB color plus blink. (Two channels: $4500)

## GMR 37-30: $4500
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## GMR 37-60: $4700
1024 x 1024 resolution, one channel B/W.

In addition, you can also have several economical options: independent cursors, joysticks, keyboards, special character sets and 16 bit, plug-compatible parallel minicomputer interfaces.

Further, if you ever want to move up, Grinnell has a complete line of larger systems—all software compatible with the GMR-37—to do things like animation, image processing and real-time frame grabbing.

So, if quality graphic displays are important to your product, look at the GMR-37 line. For a quotation on the system that meets your specific requirements, call or write.

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IMAGINE

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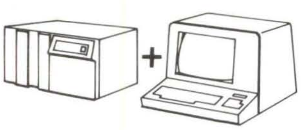
Zilog's powerful Z8000, the generation-ahead 16-bit microprocessor that delivers big computer performance at microprocessor prices, is on the shelf today at Zilog distributors around the country. Order it as the 40-pin Z8002 with 64KB direct addressing, $107.10.* Or, choose the 48-pin Z8001 with 8 MB segmented addressing, $139.30.* Supporting it is the versatile PDS 8000 family of development systems.

## The base package, the Model 10.

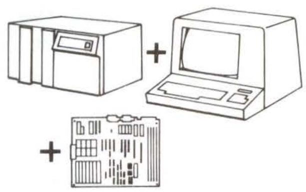
Your most economical entry to Z8000 product development. Everything you need to start your Z8000



software development: a 64K byte microcomputer, CRT, dual floppys, interfaces, 9-slot card cage, power supplies, a Z8000 software development package, operating system, editor, linker and utilities. $10,500.*

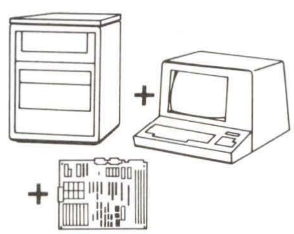
## Try it out with the Model 15.

Everything in the PDS 8000 Model 10, plus Zilog's Z8000 Development Module, a Z8000 based computer board with 2K words



of EPROM (expandable to 8K words), 16 K words of dynamic RAM (expandable to 32K words), dual serial interface, 32 programmable I/O lines, four 8-bit programmable counter-timers and a generous wire wrap area. $11,995.*

## For more complex ideas, Models 25 and 30.



These two PDS 8000 models parallel the capabilities of the Model 10 and 15 but give you the added power of 10 megabytes of rack-mounted hard disc drive. $20,000* and $21,500.*

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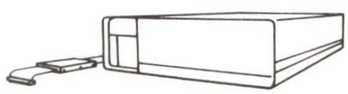

support capability for the Z8000 as well as the Z8.

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We'll send you a complete packet of technical data on the PDS 8000 family and Z8000 Development Module together with the name and location of your nearest Zilog distributor. Address: Zilog, 10460 Bubb Road, Cupertino, CA 95014. Or call (800) 538-9367 toll free. (In California call (408) 446-4666.)

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jobs/s. Next they point out that, with the system in equilibrium handling X/D jobs/s, the CPU and each channel must obviously be handling X/D jobs/s—no one component can get ahead of the rest. Therefore each job spends an average time D/X s being processed at the CPU and at each channel. Now, suppose $n_i$ is the average number of jobs in the queue at the ith facility—i = 1 for the processor, and i = 2, 3, . . . , (I + 1) for the channels. Then turnaround time is

$$R = \sum_{i=1}^{I+1} n_i \frac{D}{X}$$

But we know that there are always J jobs in the system, so the sum of the queue lengths is J, and

$$R = \frac{JD}{X}$$

Turnaround time is plotted in Fig 2 for the same conditions as shown in Fig 1.

## Effects of Multiple Channels

To illustrate the effect of multiple channels, assume a large system having sixteen 3330 discs, and examine how its throughput varies with the number of channels the discs share. Adding channels increases the total data rate from the system; however, adding channels with a fixed number of discs reduces the number of discs per channel. How does channel data rate vary with the number of discs per channel? Kolence points out that channel data rate is a function of the block size and of detailed characteristics of the discs.[4] If N 3330 discs are connected to the channel, data rate for a block size of B kilobytes is given in Fig 3, which shows how D′ varies with B for several values of N. The denominator in that formula is the time required to transfer B kilobytes, assuming use of a block multiplexer channel with rotational position sensing. Transfer time includes a fraction of the 16.7-ms disc rotation time, plus the time necessary to read the B kilobytes and their fixed 135-byte preamble, at 806k bytes/s.

Using the results of Fig 3, we can employ Denning-Buzen calculations to determine the effect of number of channels on throughput. The result is shown in Fig 4, for two different values of s—40 and 80 operations per I/O character.

System performance has of course improved substantially since the 1950s. Fig 5 shows on a log-log scale (so the hyperbola of Fig 1 becomes a straight line) how performance has improved as the generations have passed. Unfortunately, too little is known about workloads. Although I speculated in "Market Elasticity" (see *Computer Design,* Aug 1979, pp 46-54) that average computer operations per I/O character have increased

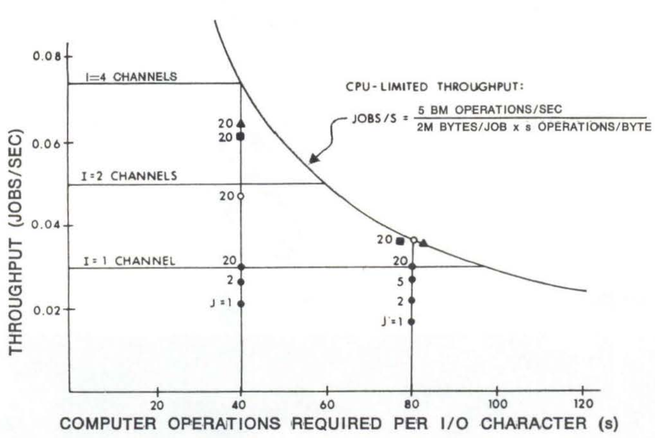


Fig 4 Effect of multiple channels on throughput. System throughput for Amdahl 470/V5 CPU connected to 16 IBM 3330 disc files is function of number of I/O channels used. Graph assumes B = 3k bytes, D = 2M bytes, k = 10, and C′ = 5.81M operations/s. With all 16 discs on one channel, throughput is I/O-limited at 0.03 jobs/s for s = 40 or 80 operations/byte, and increases as multiprogram level increases, as shown by solid dots. With eight discs on each of two channels, maximum possible throughput is raised to 0.05 jobs/s. System is compute-bound at s = 80, and handles about 0.036 jobs/s with 20 resident jobs; it remains compute-bound as I increases. At s = 40, system is I/O-bound; 20 resident jobs bring throughput to about 0.047 jobs/s (open dot). With i = 4 or 8 channels, system is compute-bound again, and 20-job multiprogramming level raises throughput to 0.061 or 0.064 jobs/s as shown by square and triangle

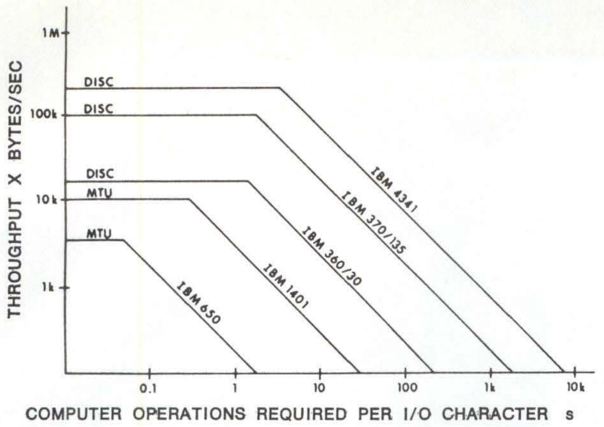


Fig 5 Throughput trends. Changes in throughput versus s over five successive generations of IBM processors is plotted on a log-log scale so that the compute-bound line becomes a straight line. I/O-bound limit for each system is based on operations of indicated peripheral device on single channel with specific block length (see Ref 2, p 111), and can be increased by increasing number of I/O channels. Note that value of s for single-channel system has been increasing, reflecting the fact that processor speeds have increased faster than I/O speeds

with time, there are few measurements of this important workload parameter. This makes it extremely difficult to visualize where systems have operated and are operating in the plane of Fig 5.

## Summary

This simple model thus suggests that the system designer focus attention on expected workload parameters s, D, and k, and on system parameters C′ and D′. The relationship between system I/O rate D′ and peripheral (eg, disc) design parameters is of great importance, for the instantaneous data rate handled by the electronics is never seen by the system.

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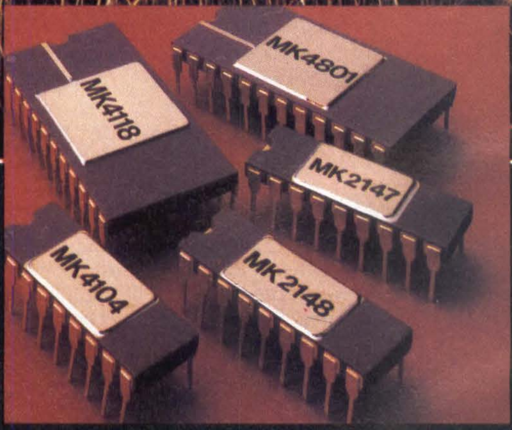
2. M. Phister, *Data Processing Technology and Economics*, Santa Monica Publishing Co, 1976, pp 88-96, 104-111
3. P. I. Denning and J. P. Buzen, "The Operational Analysis of Queueing Network Models," *ACM Computing Surveys*, Sept 1978, pp 225-261
4. K. W. Kolence, *An Introduction to Software Physics*, Institute for Software Engineering, Palo Alto, 1976


The Author solicits comments on the material presented here, data supporting or contradicting his approach, and suggestions for topics to be explored in future articles.—Ed.

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| *MK2147 | 4K X 1 | <100ns |
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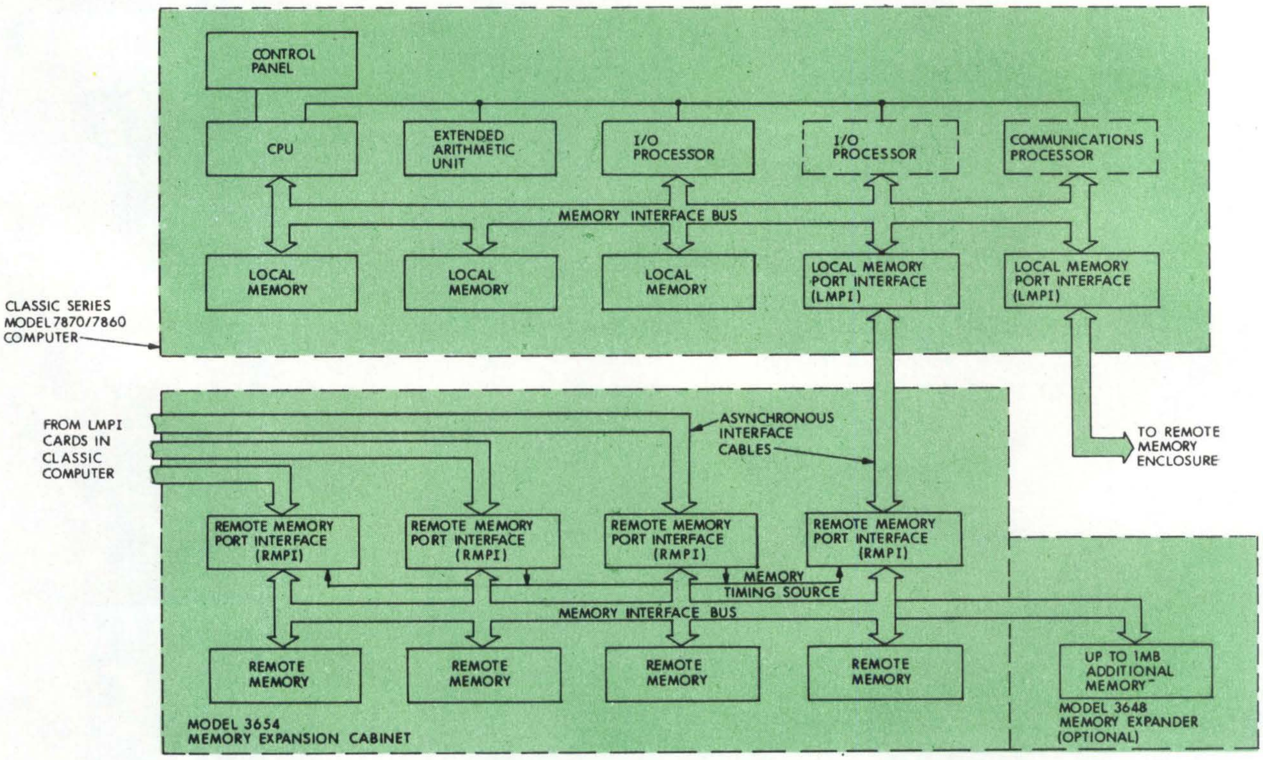
CIRCLE 29 ON INQUIRY CARD

*Available first quarter 1980

## Multiport Memory System Permits Multiple Computers To Share Common Memory




**Modcomp's shared multiport memory system hardware provides the ability to extend and connect two or more CLASSIC 7860/7870 memory buses. When the second bus is housed in a memory expansion cabinet, the result is memory expansion. When two or more computers connect their buses to the cabinet, all gain shared access to data stored there**

Allowing up to four CPUs to access and share data stored in a 4M-byte memory, the Shared Multiport Memory (SMM) System enhances online processing by reducing the time wasted in loading frequently activated tasks from peripheral storage devices. By permitting multiple computers to divide the work load and store common data in shared memory, the hardware, developed by Modular Computer Systems Inc, 1650 W McNab Rd, Ft Lauderdale, FL 33309, significantly increases total realtime processing capability.

The hardware device consists of model 3654 memory expansion cabinet and 3655 memory port interface, combined with CLASSIC 7860/7870 series computers. The cabinet includes an 8-slot card file, interface connector panel, and switching power supplies which power logic and memory. Consisting of two memory port interface PCs and supporting interface cables, the interface contains everything necessary to connect two standard memory buses.

The local memory port interface (LMPI) card resides in the same card file with the computer that is seeking to share external memory. The second card is the remote memory port interface (RMPI) which resides in the card file containing remote or shared memory. Shared memory can be that in another 7860/7870 computer or in a 3654 expansion cabinet. Two LMPI cards can be configured in each computer.

The shared memory hardware provides ability to extend and connect two or more memory buses, resulting in memory expansion when the second bus is housed in an expansion cabinet. When two or more computers connect their buses to an expansion cabinet, all computers can access that memory and share data stored there. Sharing between two computers is accommodated when a

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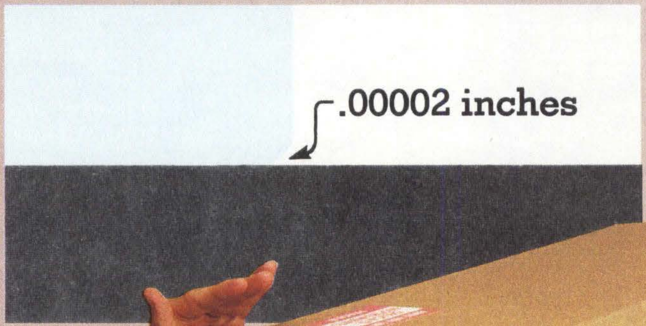


The ultra-clean room facilities alone mind-boggle the uninitiated. Marksman units are assembled and sealed in a room so clean that excessive hand movement is prohibited because it creates five times the contamination of normal movement.

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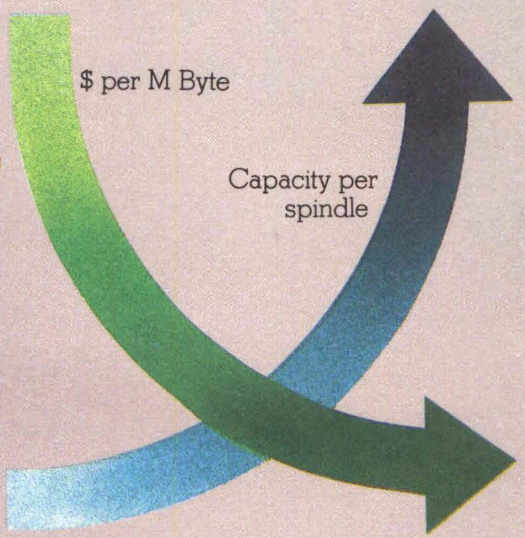


We're currently shipping both 10 MB and 20 MB versions, with a 40 MB model right on their heels and even more to come.

Pricing for the 40 MB Marksman is under $1800 in OEM quantities—actually less than projections on rumored smaller competitive units which will someday have only one-fourth the capacity.

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To save you interfacing time and money, one Marksman model comes with a built-in microprocessor-based controller/formatter. It contains many of the interface and overhead functions normally relegated to the custom controller and CPU. That leaves you very little to do to put the whole system on-line.

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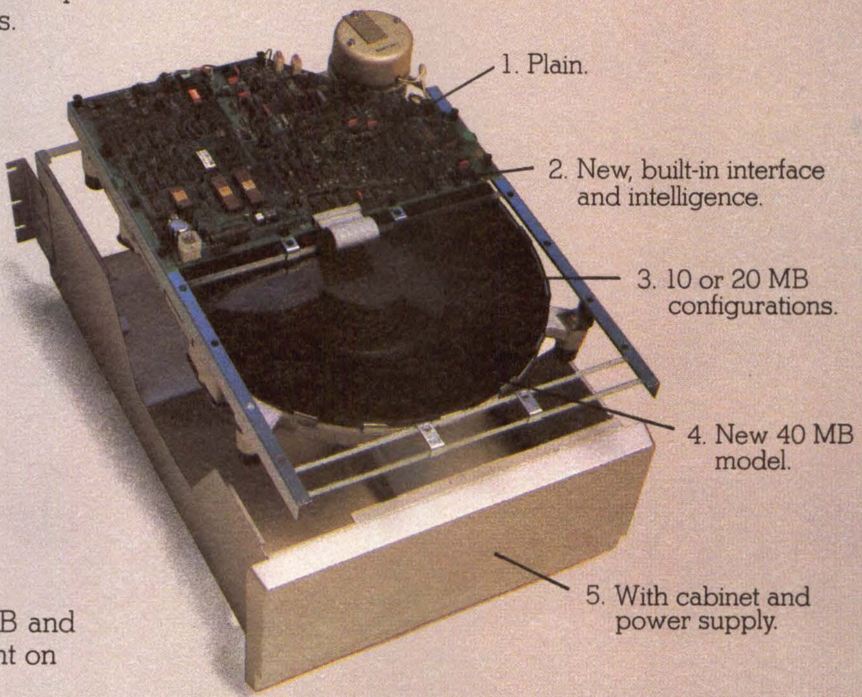


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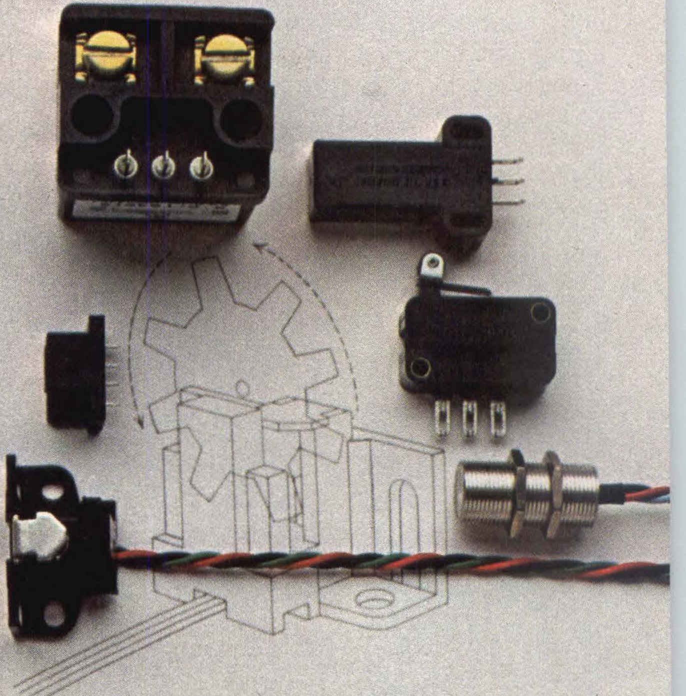
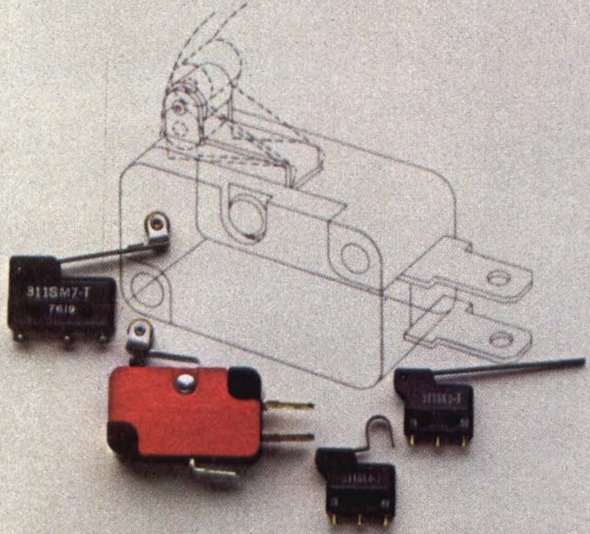
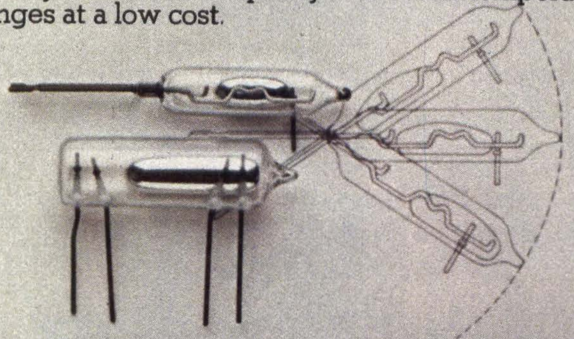




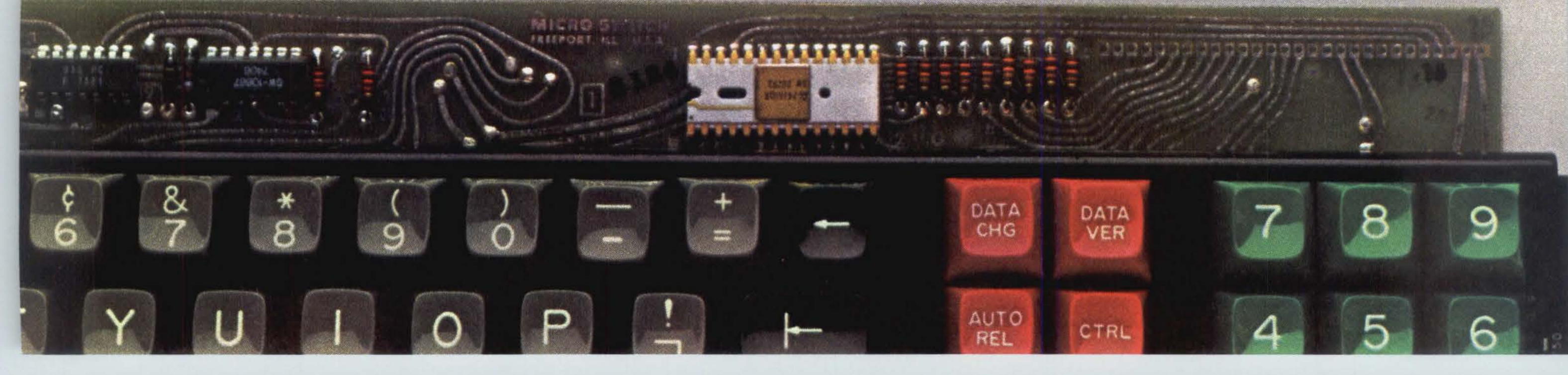

Snap-action V3, SM and SX switches offer wide variety of actuators, electrical capacity and termination.

Mercury switches offer hermetic sealing, a variety of electrical capacity and broad temperature ranges at a low cost.



AML manual devices for low installed cost, electrical flexibility and attractive panel appearance. Series 8 miniature manual switches provide small size and wide variety of operators. DM offers inexpensive snap-in panel mount design.

Solid state keyboards provide high reliability no mechanical keyboard can offer. Panel sealed versions also available.



computer extends and connects its memory bus to another computer using the memory port interface.

To achieve memory bus extension the LMPI card assumes the role of a memory module, responding to and initiating activity on the standard memory interface bus. When the computer accesses memory outside the cabinet, the card automatically buffers and passes necessary information and control to the RMPI card. The RMPI interfaces with the second memory bus and activates memory as commanded by the LMPI card.

Communication between LMPI and RMPI cards is asynchronous to allow flexibility in cable length. To allow private areas in remote memory, the RMPI card can prevent access to portions of remote memory.

Configuration flexibility provides solutions to various industrial, real-time, and scientific problems. In a 4M-byte dedicated memory configuration, system performance can be enhanced by adding 3M bytes of dedicated remote memory within two expansion cabinets, one containing the memory expander. A shared configuration may have a private address space with all other memory available to both computers. In a multiprocessor environment, up to four computers may access a single expansion cabinet containing 2M bytes of memory. Total system memory may consist of a variety of module sizes, but must be the same technology (eg, core or RAM).

Memory cycle times may vary depending on configuration and application. Effective cycle time with 4-way interleaving is approximately twice as fast as with 2-way interleaving. Some typical cycle times are 125 and 250 ns for 4- and 2-way interleaving with 128k bytes of MOS, and 225 and 450 ns for 128k bytes of core. Through a memory port interface, a write word operation requires 600 ns/transfer; a read word, 700 ns/transfer; and a DMP output takes place at a 1-MHz rate.

**Circle 175 on Inquiry Card**

## Expanded Business System Offers Additional Flexibility

In addition to cost-performance values the fully programmable System 200 small business computer provides the flexibility to meet future data processing requirements. By expanding the system from a bundled 9-module basic accounting system, Basic Four Corp, PO Box C-11921, Santa Ana, CA 92711, has given users the option of upgrading to a System 410, opening an entire range of capability.

Standard configuration of the system consists of CPU with 10M-byte fixed disc storage, 32M-byte system memory, 8k-byte user memory, one video display terminal, 120-char/s bidirectional printer, and 2.3M-byte magnetic tape cartridge drive. Base price is $24,990. Disc storage expands to a maximum of 20M bytes in increments of 5M bytes; main memory expands to 48k and 64k bytes. An additional VDT may be used with the system, and 150-line/min or 160-char/s printers are available as options.

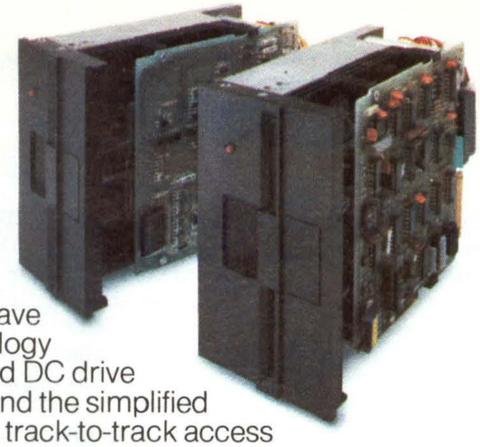
**Circle 176 on Inquiry Card**

## Solid State Data Recorder Achieves Accuracy With Light Gate Array

HR-2000 Datagraph[R], a solid state direct writing, analog signal recorder, achieves high fidelity and accuracy through use of a programmable light gate array that eliminates problems of linearity, overshoot, beam deflection, inertia, and torque. Developed by Bell & Howell, CEC Div, 360 Sierra Madre Villa, Pasadena, CA 91109, the unit records up to 28 channels of data. It is capable of recording incoming signals up to 5 kHz and can record high frequency transient signals that have previously gone unseen.

The system is based on a concept developed at Sandia Laboratories that involves a special ceramic material which is transparent to light. This material, a ferroceramic compound based on lanthanum modified lead zirconate titanate (PLZT), acts as a light shutter. When no field is applied, light passes through a wafer unchanged; when a field is applied, the material's crystal orientation changes, thus altering the index of refraction and causing a virtual rotation of an incoming wavefront of light.

The light gate array within the system consists of a sandwich of opposing polarizing filters applied to either side of a precision pattern of electronic gates. 80 such gates per



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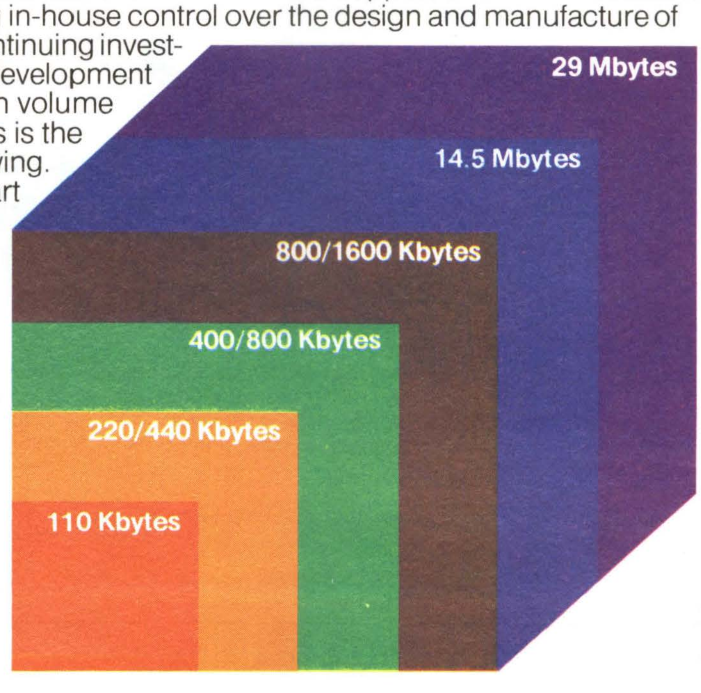


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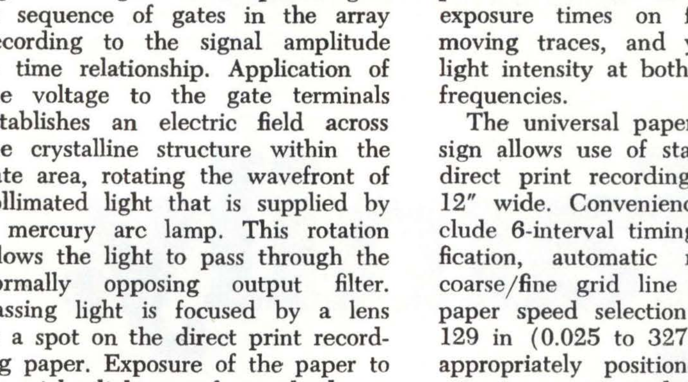
CIRCLE 33 ON INQUIRY CARD

inch each 0.0125" (0.3175 mm) wide are formed by depositing electrodes on modular wafers of PLZT material using photomask thin film deposition methods. A 12" (30.5-cm) wide array contains 960 light gates, while an 8" (20.3 cm) wide array has 640, providing high resolution.

Incoming analog signals are directed to voltage to time converters, which impress the data on a ramp voltage. This voltage effectively assigns the signal to a specific gate or sequence of gates in the array according to the signal amplitude to time relationship. Application of the voltage to the gate terminals establishes an electric field across the crystalline structure within the gate area, rotating the wavefront of collimated light that is supplied by a mercury arc lamp. This rotation allows the light to pass through the normally opposing output filter. Passing light is focused by a lens as a spot on the direct print recording paper. Exposure of the paper to ultraviolet light transforms the latent spot images into visible data.

Individual gates in the array act as solid state digital light shutters. Turn-on and turn-off times are on the order of 1 or 2 $\mu$s. Each gate remains open for 20 $\mu$s, the length of time it takes to scan the full array. Since focal length and beam deflection angles are nonexistant, and the final collimating lens distance from array to paper is constant across the entire width, linearity is directly proportional to precision of the photomask used to produce the gates. In addition, the technique produces the same instantaneous spot exposure times on fast and slow moving traces, and yields constant light intensity at both high and low frequencies.

The universal paper transport design allows use of standard sizes of direct print recording paper up to 12" wide. Convenience features include 6-interval timing, trace identification, automatic record length, coarse/fine grid line selection, and paper speed selection from 0.01 to 129 in (0.025 to 327.66 cm)/s. An appropriately positioned mirror assures proper recording position by permitting the actual recording point to be viewed during set up and data runs. Circle 177 on Inquiry Card




Light gate array within Bell & Howell's HR-2000 Datagraph can be scanned in 20 $\mu$s, providing capability of recording signals up to 5 kHz. For the dynamic sine wave trace shown, data commands address adjacent gates which open and close in relation to the polarity and amplitude of data waveform

## Computer Systems Supply Power/Performance With Pipeline Architecture

Series 800 computers, S850 and S870 perform 1.8 times faster than previous S500 systems and can support up to 128 interactive users. Demonstrated by Harris Corp, Computer Systems Div, 2101 W Cypress Creek Rd, Ft Lauderdale, FL 33309, the systems incorporate a 48-bit pipeline architecture, cache memory, and an advanced diagnostic unit.

Utilization of the systems is accomplished through multiple batch operations, various interactive terminals, remote job entry, or direct connection to instrumentation or control apparatus. Interfaces can be engaged simultaneously with precedence and priority established by the user. System power can be concentrated on a single task or dynamically distributed to concurrent solution of smaller tasks.

Full word (48-bit) floating point operations use an 8-bit exponent and 39-bit mantissa. Double-precision operations provide greater accuracy where required.

Upward compatible extensions of S100, S200, and S500 systems, the S850 supports up to 96 users, the S870 up to 128. Running under the VULCAN virtual memory operating system, each can perform concurrent timesharing, multistream batch, remote job entry, and realtime processing.

Each system can directly address up to 3072k bytes of MOS memory. A 6k-byte cache memory provides separate rapid access storage for instructions and data. Hit rate has been demonstrated to be above 90% providing an effective operating access time of one-tenth that of main memory.

An integral scientific arithmetic unit in the S800 is a hardware floating point processor that enhances program performance in scientific and engineering applications. Another standard feature of this machine is the maintenance aid processor which acts as a diagnostic tool, providing selective, online monitoring and control of computer logic.

A standard S850 consists of series S800 CPU, 960k-byte main memory,

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**CIRCLE 34 ON INQUIRY CARD**

12,288k-byte virtual memory, system console CRT with keyboard and controller, MAP console CRT with keyboard, 80M-byte storage module drive with controller, and DMA communications processor with two dual asynchronous ports or one single synchronous port. An S870 offers 2112k bytes of MOS memory, 12,288k bytes of virtual memory, CPU, system console, MAP console, 300M-byte storage module drive, 9-track, 45-in/s magnetic tape unit, 600-line/min printer with controller, DMA communications processor, and memory expansion unit.

Both systems are supported by the VULCAN operating system, interactive text editor, support libraries, and language processors. Included in these languages are the company's macroassembler, COBOL, SNOBOL, and FORGO. VULCAN also supports the company's multipass FORTRAN 77, a multiuser APL language based on APL shared variables, total database management system, and interactive BASIC language.

Circle 178 on Inquiry Card

## 16- and 32-Bit Computers Adapt Readily to Changing Requirements

NORD-100 and -500 computer systems meet requirements covering the range from small dedicated units to large multimachine systems. Developed by Norsk Data, AS, Lindebergveien Nord 20, PO Box 4, Lindeberg Gard, Oslo 10, Norway (available in the U.S. through Norsk Data NA, Inc, 65 William St, Wellesley, MA 02181), the machines communicate directly by means of interactive terminals. Both hardware and software are capable of reacting to time-critical events. The operating system provides capability of handling realtime applications for externally controlled processes, timesharing for program development, transaction processing for administrative applications, and online database operation for periodic or low priority tasks.

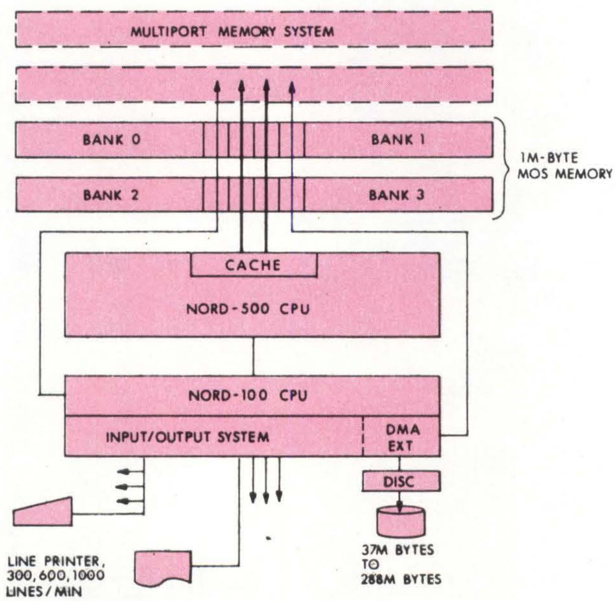
An advanced single-card minicomputer, the NORD-100 uses bit-slice components to reduce the CPU from 16 cards to a single 28 x 37-cm multilayer card. This 16-bit parallel microprogrammed processor executes bit, byte, single-, double-, and triple-word, and register file instructions. The CPU has an 180-ns internal cycle time. All instruction execution is in firmware using a 2k x 64-bit ROM. Instruction prefetch increases performance. A 256-word x 64-bit writable control store allows dynamic microprogramming. Both fixed and floating point arithmetic are standard.

A plug-in operator console is operated by a microprocessor that is independent of the program being run in the CPU. The console includes a digital clock that runs on a battery in the event of power failure. If power fails, the system is automatically restarted and the computer clock is set by the digital clock; an automatic fault-finding routine is simultaneously initiated from the CPU.

Modularly designed, the -100 system adapts to changes in routine. It is capable of addressing up to 32M bytes of main memory and an additional 2304M bytes of disc storage. 64k- or 128k-byte memory modules are available. An optional 2k-byte cache memory increases speed. Cache is organized as a 1k x 31-bit lookup table, and is homogeneous—it does not discriminate between data words, instructions, or indirect addresses.

A 32-bit multiprogrammed computer, the NORD-500 is capable of executing programs requiring up to 4300 bytes of logical address space and another 4300M bytes of data. The system is designed specifically for large calculation tasks such as simulation, numerical analysis, and scientific.

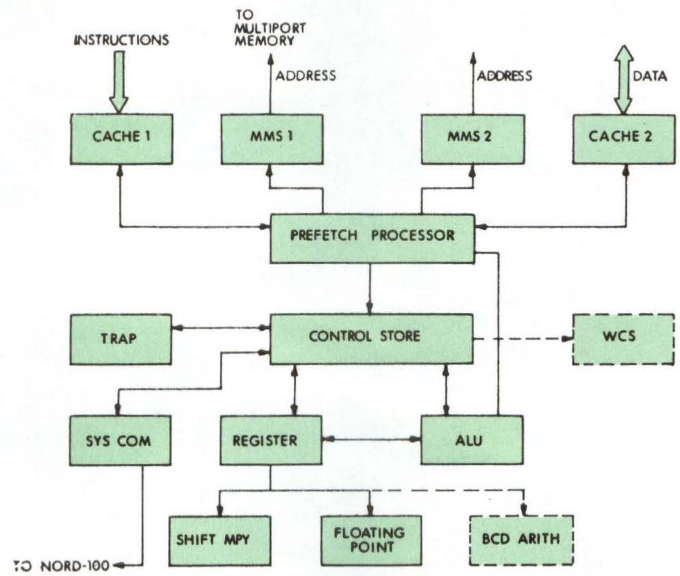
With the 32-bit architecture necessary to accommodate very large programs, the unit incorporates high capacity cache memory, prefetching




NORD-500 from Norsk Data uses 32-bit architecture with high capacity cache memory, efficient instruction repertoire, prefetching of data and instructions, and high speed floating point hardware. Dual computer system consists of -500 CPU, executing large user programs, integrated with -100 minicomputer, which runs the multimode, multiuser operating system and performs all I/O handling, job scheduling, and resource allocation. Up to 64 users can access the system and share up to 32M bytes of MOS memory and 2300M bytes of disc storage of data and instructions, and high speed floating point hardware. The dual computer system consists of a -500 CPU, which executes large user programs, integrated with a -100 minicomputer that runs the multimode, multiuser SINTRAN III/VS operating system, and performs all I/O handling, job scheduling, and resource allocation. A multiport memory system allows shared access between the -500, -100, and I/O devices. Additional -500 processors with hardware augmented with 32/64-bit floating point multiply/divide can be connected to act as a multiprocessor system supervised by a -100.

Included in the -500 CPU are a set of programmer accessible special and general purpose registers as well as a scratchpad file accessible only by the microprogram. Microcode for execution of machine level instructions resides in control store. Standard instruction set as well as routines for context switching and communication with the supervisory processor are implemented in approximately 72k bytes of ROM.

A prefetch processor handles predecoding and assembling of machine level instructions in the pipeline and initiates data fetch cycles for memory reference instructions. By keeping the pipeline full, this processor assures minimum idle time.




Implemented in bit-slice modules, the NORD-500 CPU provides a full 32-bit addressing scheme. Main memory can range from 128k to 32M bytes formed from 16k MOS RAM chips with error checking and correction. Separate data and instruction caches resolve address conflicts and result in high hit rate. Prefetching processor decodes codes and specifiers, and performs address calculations while the previous instruction is executed in the ALU

Separate but identical memory management systems (MMS) are provided for instructions and for data. MMS maps the 32-bit logical byte address into a 25-bit physical byte address used to address main memory. A multilevel table lookup procedure is used to convert from logical to physical address. The system acts to protect sections of memory designated as read only or system data.

Cache is also made up of two separate but identical memories for instructions and for data. Cache words can be 32, 64, or 128 bits wide; depth is 4k words. Cache is addressed by logical address from the CPU and is byte addressable. It has a 110-ns access time.

All system memory is shared between the system's processors and I/O devices. The multiport memory can be established with 2, 4, or 8 1- or 2-bank racks and with 4- to 16-way interleaving, depending on the number of banks used. Four independent paths to memory are provided: the -500 uses two, the -100 uses one, and the other is used for DMA from high speed peripherals.

Running on the -100 system supervisor the SINTRAN III/VS operating system incorporates a sophisticated NORD-500 MONITOR. All management functions are handled by the operating system, leaving the -500 CPU free. Features of the operating system include a time-slicing mechanism, output spooling, and integrated file system. Resource sharing capabilities permit concurrent activities in interactive, realtime, and local and remote batch modes.

Programming languages include an ANSI 77 based FORTRAN, ANSI-74 COBOL, BASIC, RPG II, and macroassembler. Pascal, Simula, and CORAL 66 are available. Library functions include QED text editor, SIBAS data base system, relocating loader, ISAM, screen handler, data entry system, transaction processing system, packet switching system, file utility, sort package, and scientific subroutines.

Circle 179 on Inquiry Card

## Single Component Resins Offer Epoxide Performance With Processibility

ARNOX™ resins, a family of high performance epoxides, are versatile rapid cure materials that respond to demands of mass production. Developed through intensive research conducted by General Electric's Corporate Research and Development Center in Schenectady, NY and Plastics Division R & D Facility at One Plastics Ave, Pittsfield, MA 01201, the resin cuts cure time and solves problems relating to storage, handling, and batch consistency. The resin can be compression and transfer molded without refrigeration or special handling of resin supplies. It can be injection molded, and can be used in low pressure liquid processes.

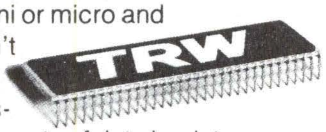
Featuring single-component epoxide technology, the system requires no component mixing to initiate the curing process. Cure is thermally

TRW keeps you ahead in digital signal processing

# A monolithic 16-bit, 115 nsec multiplier/accumulator

Use our new TDC 1010J multiplier/accumulator (MAC) to build a high-speed digital signal processor. With it you can analyze radar signals or X-ray data; communicate with satellites or computers; synthesize complex waveforms—even music.

A small FFT processor based on TRW's new MAC operates as a spectrum analyzer too—add one to your mini or micro and you don't have to lug massive amounts of data back to a number-crunching mainframe for reduction; you can reduce it right there on site and in real time!




It can analyze voices, earthquakes, geological soundings and submarine signatures. It can recognize a sticky valve in an automobile engine or in a human heart.

There was a time when the phrase "FFT processor" conjured up the image of an entire bay of sophisticated electronic hardware, but that's all changed now.

Starting with just a single TDC 1010J, you can design your own FFT processor on a small pc card. It will operate on just a few Watts and the CPU's microcode need never even touch the data.

Simply strobe any pair of 16-bit numbers into the MAC's on-chip input registers and zip—the chip delivers the correct 32-bit product for you in a mere 115 nsec.

An on-chip, 35-bit wide accumulator lets you choose to sum a series of products with no time penalty; that's both a double-precision multiply and a 35-bit add in the same 115 nsec!

Flexibility is a key feature of the TDC 1010J—it works on numbers as either two's complement or unsigned magnitude; the 35-bit accumulator can be directly pre-loaded, and you can round off the accumulated products to single precision.

Our new MAC is fully compatible with industry standards TTL. (It should be—after all, TRW invented TTL and patented it back in the early '60's, remember?) Of course, 3-state output buffers are provided.

TRW's TDC 1010J multiplier/accumulator is packaged in a 64 pin DIP. It consumes just 3½ Watts, uses a single +5V supply and is radiation hard. It is priced at only $205 in quantities of 100.

These products are now in stock at Hamilton/Avnet.

**For immediate information call 213/535-1831 or send in coupon. If you can wait several weeks, use reader service card.**

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**TRW LSI PRODUCTS**

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triggered at a specific temperature in the 250 to 350 °F (121 to 176 °C) range. At lower temperatures the resin is stable, requiring no refrigeration or special handling. Cure rates, however, are exceptionally fast, providing processibility.

Three series of resins are available. 1000 series is a black granular resin designed for high performance compression and transfer molding. A pelletized, colorable, injection moldable material, 2000 series combines high heat and impact performance with high volume injection molding technology. This material is suggested for metal replacement applications in heated appliance parts, motor frames, and other applications where thermal and environmental stability combined with electrical performance are required. 3000 series resin is a liquid material for pultrusion and filament winding.

Circle 180 on Inquiry Card

## Instruction Set Allows Vector Processing On Minicomputer

Vector instruction set allows vector processing operations, formerly the province of supercomputers, to be performed on midscale HP 1000 F-series minicomputers. Introduced by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, the instruction set accomplishes vector operation by relatively simple FORTRAN commands at speeds 4 to 10 times faster than before possible.

Offered as optional equipment on HP-1000 F series computers or as a retrofit to earlier systems in the series, the instruction set gains its speed from an architecture that allows pipelining of data to the system's floating point processor and from elimination of the loop overhead formerly associated with vector operations. The result is inversion of a 100 x 100 matrix, for example, in 12.25 s. Capability for handling matrices of up to 600 x 600 is provided by the extended memory area of the RTE-IVB operating system which allows direct addressing of data arrays of almost 2M bytes from a user program.

The vector instruction set includes 38 new vector instructions that are used to replace the FORTRAN DO loops previously needed to define necessary interactive operations. Vector addition, for example, replaces a 25-character instruction with VADD, and executes 10 times faster than the DO loop replaced. Instructions are provided for vector-vector and vector-scalar arithmetic, as well as products, pivot, swap, and maximum/minimum operations.

Circle 181 on Inquiry Card

## CPUs Extend Mainframe Family Into High Performance Range

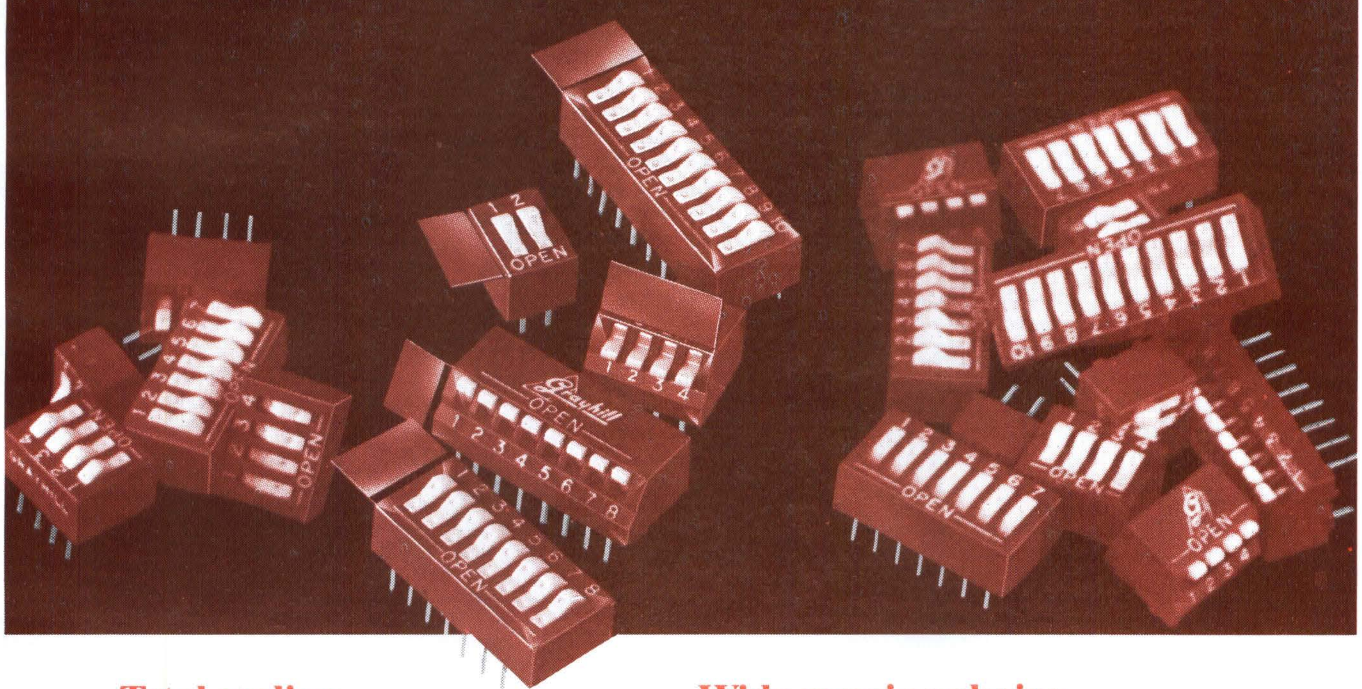
Geared to meet needs of sophisticated large scale users, AS/7 model 7033 and AS/8 model 7034 offer the reliability of their predecessor, the AS/6, as well as greater computer power at lower cost than is currently available. Developed jointly by Itel Corp, Data Products Group, One Embarcadero Ctr, San Francisco, CA 94111, and Hitachi Ltd of Japan, the units incorporate modular architecture and make use of LSI logic components. Like the IBM 4300 and expected "H" series, the units run in 370/303X compatibility mode.

Internal performance of the AS/7 model 7033 dual processor complex is claimed to equal or better that of the IBM 3033 when operating under identical programs and similar system configurations. Modular architecture and dual processor concept of the system provide increased system availability and result in improved performance. Appearing to the user as one CPU, the dual processor complex offers a simplified operating environment, improved scheduling, and enhanced utilization of system resources when compared to multiple unit processor environments.

AS/8 model 7034 offers internal performance claimed to be 1.6 times that of the AS/7. Featured are LSI semiconductor technology, modular architecture, and air cooling. Operating speed is provided by the use of 550-gate LSI and bipolar RAMs. Expandable memory capacity, firmware microcode flexibility, and upgrade models are planned to support large user complexes beyond single unit configurations.

Circle 182 on Inquiry Card

# Grayhill totally sealed DIP switches better than ever better than others




## Total sealing

Each Grayhill SPST Rocker DIP Switch is now potted as part of the assembly process, to provide a more professional and economical bottom seal, with maximum seal integrity. Flux entry during wave soldering is totally prevented; contamination is eliminated; reliability is enhanced; and prices are unchanged . . . there is no cost premium for this important new feature. Grayhill also offers 3 topside sealing options, for raised or recessed rockers—a tape seal, applied at Grayhill; cards of tape seals, for your application; or re-usable protective covers. Whichever you choose, you get complete freedom during PC Board cleaning.

## Exceptional reliability

All Grayhill DIP Switches incorporate our exclusive spring-loaded, sliding ball contact system. This highly reliable contact system provides positive wiping action, immunity to normal shock and vibration, and exceptional 50,000 cycle life.

## Wide ranging choice

Grayhill Sealed Base Rocker DIP Switches are available SPST, from 2 to 10 rockers, with raised or recessed rockers. Grayhill also provides the Piano DIP™ SPST side-actuated DIP Switch, sealed; the Toggle-DIP (SPDT or DPDT) for front panels, plus SPDT or DPDT back panel programming DIP Switches.

## Off-the-shelf distributor availability

Procurement made simple—call Grayhill or your local distributor, for off-the-shelf delivery of most types. Only Grayhill offers you this purchasing convenience!

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## 1.2G-Byte Disc Subsystem Uses Intelligent Switching, Winchester Technology

Model 3652, a dual-spindle, double-capacity version of the 3650 drive, provides 1.2G bytes of stored data per module, yet occupies the same area as the 3650. Announced by Memorex Corp, Large Storage Systems Group, San Tomas at Central Expy, Santa Clara, CA 95052, the unit incorporates advanced Winchester technology and high performance features that significantly improve system throughput.

Among the features that achieve improved throughput is the intelligent dual interface. This feature provides dynamic dual-port access to each disc drive spindle, 2-string switching, and automatic backup of the disc string via one of two controllers. The interface provides the intelligence necessary to direct data flow to the appropriate channel. As a result, disc strings are always available, even if one of the two controllers is busy. In a 2-CPU environment this gives both computers simultaneous access to both strings.

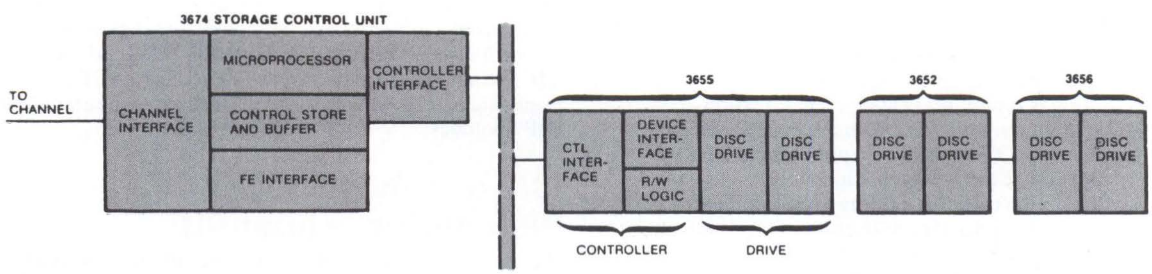
The 3652 offers optional fixed head storage capacity of 2.28M bytes/spindle. It has an average access time of 22 ms with standard moving heads and a data transfer rate of 1.198M bytes/s. To accommodate its 6350-bit/in (2500/cm) recording density and to meet head to track alignment requirements the unit incorporates head/disc assembly technology. HDA achieves highly reliable performance and maximum data integrity by combining critical equipment components such as read/write heads with the discs in an environmentally sealed unit.

Another design feature is its built-in microdiagnostic fault isolation aids. These assure maximum system reliability by allowing problems to be diagnosed down to the smallest field replaceable unit rather than to the component. Modular packaging of components further eases maintenance by isolating each function to one specific PC board.

Other user oriented features encompass full track read, which allows data on one track to be read from one command; error correction, which detects single-error bursts up to 10 bits in length and corrects single-error bursts of up to four bits; and command retry, which enables the storage control unit and channel to recover from subsystem errors. Rotational position sensing allows for channel disconnect during most of the rotational latency period giving greater channel availability. Enabling the read only switch prevents writing or erasure of previously recorded data. A write format release enhances subsystem performance by permitting a single spindle to continue an erase from the end of a formatted write while freeing the rest of the subsystem for other functions.

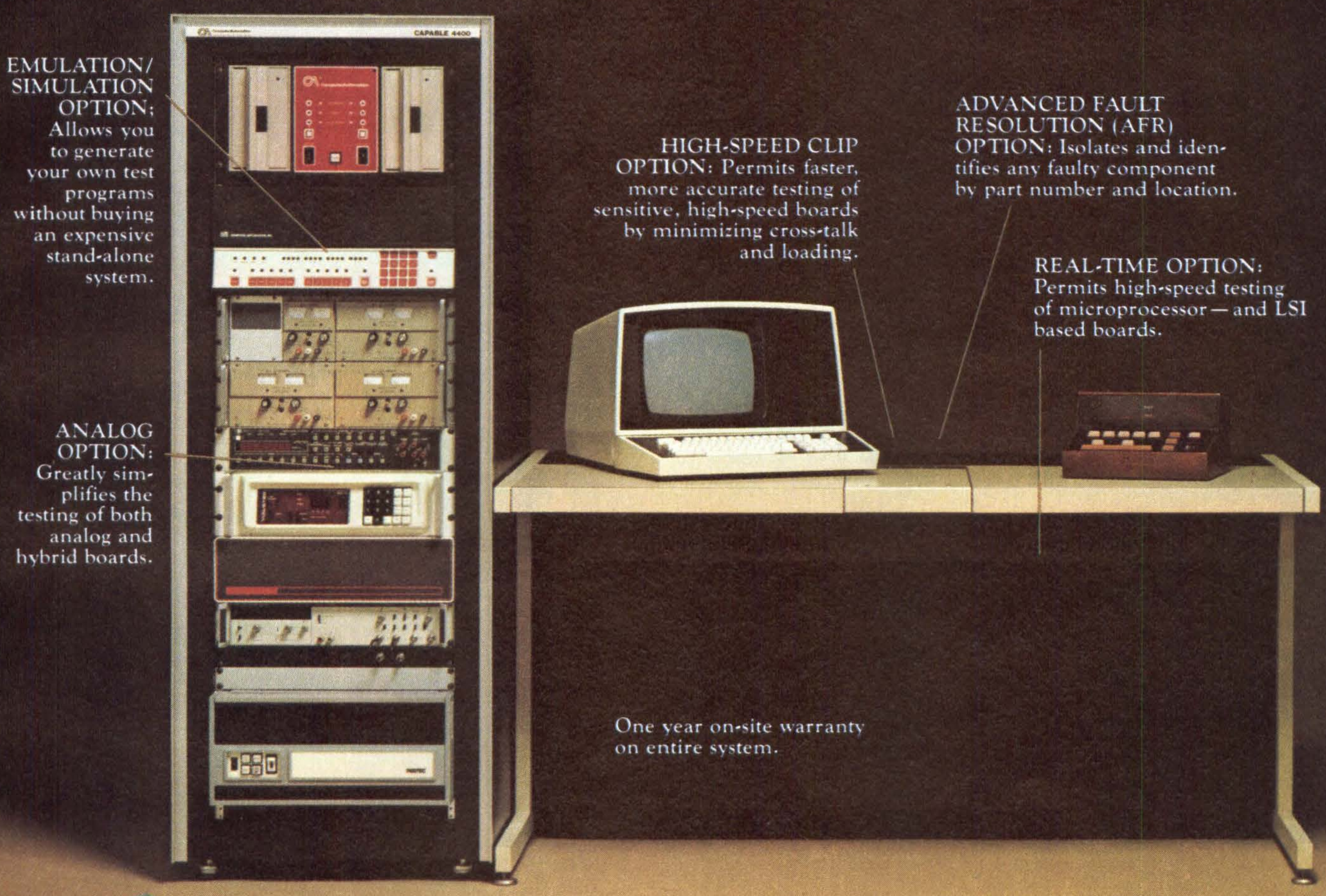
From the systems standpoint, the subsystem is compatible with the 3650 and is supported by the 3674 storage control unit. In large configurations it may be expanded via the 3675 storage modules and controllers and from one to twelve 3652 storage modules. The subsystem is totally compatible with IBM System/370 models 158 and 168, IBM Systems 3031, 3032, 3033, 4341, Amdahl 470 V series, and other compatible processors.

Circle 183 on Inquiry Card




Providing users with 1.2G-byte capacity, Memorex's 3652 disc storage subsystem can be intermixed with existing 100M-, 200M-, 317.5M-byte drives, permitting efficient reconfiguration for balancing backup and load

# INTRODUCING THE AUTOMATIC CARD TESTER YOU CAN'T OUTGROW.




You're looking at a CAPABLE™ Tester from ComputerAutomation. But what's more important, you're looking at an automatic card tester that's truly modular in design.

And that makes it totally different from any other brand of tester on the market today.

Designed-in modularity means no matter how complex your boards become, they can't outgrow a CAPABLE Tester.

Designed-in modularity means the end of expensive overbuying, too. Because with a CAPABLE, you simply buy what you need—when you need it.

**An Ample Example.**

Take our CAPABLE Tester Model 4100. It's perfect for fast production-line testing and fault isolation. While keeping overall costs down.

What's more, you get all the basics. A powerful ComputerAutomation LSI-2 computer. 32K words of memory. A rugged floppy disk drive. A full-function CRT. Plus a comprehensive software package that includes computer Guided Fault Isolation (GFI), Fault Detection Verification (FDV) and Automatic Fault Isolation (AFI).

Where you grow from there, though, is entirely up to you.

You can keep things small, relatively specialized. Or, you can build your CAPABLE up into a model like the 4400 (as shown) to test complex boards containing LSI, VLSI and microprocessor components.

**No more growing pains. Ever.**

The CAPABLE's designed-in modularity makes it remarkably easy to add-on whatever you need. More programmable pin modules. Real-time testing. Advanced Fault Resolution (AFR). Or an analog test option.

You can even expand your CAPABLE into a full-blown Logic Simulation System and develop your own test programs.

Best of all, no matter how far you grow, Computer-Automation provides you with all the operating software you need—absolutely free—including enhancements, updates and new features.

So, before you buy an automatic card tester that will literally stunt your growth, look into the CAPABLE Family from ComputerAutomation.

We have a way of growing on you.

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**CIRCLE 38 ON INQUIRY CARD**

# The HP 2621: sim

Simple doesn't have to mean unsophisticated. The proof is in our new CRT terminal, the HP 2621.

Before building it, we took a long, hard look at the way you use a simple terminal. Then we took the knowledge gained in more than 10 years designing computer products and applied it to engineering an interactive character-mode CRT terminal from the .user's point of view.

The outcome was actually two models. The HP 2621A, which sells for $1450. And the HP 2621P, which has a built-in printer, costs $2550. You obviously want the sharpest display made. So we used the 9x15 character cell you see on every HP CRT terminal, including the top-of-the-line. And, to help you look back at the data you've entered, we provided two full pages of continuously scrolling memory.

We designed the keyboard like the familiar typewriter, so you don't have to waste time relearning it. We built in eight function keys, too. These control the cursor, rolling and scrolling. And, to make life easier, they're labeled on the screen for self-test, configuration, display and editing.

Editing? On a simple terminal? Certainly. We included character and line insert and delete, clear line and clear display. And, since the 2621 keeps your input separate from your CPU's, you can edit data before sending it to the computer. All without writing a line of system software.

Since flexibility is important in interfacing, we included a user-definable return key that will send your computer whatever code it expects. We also made our terminals compatible with RS232C and Bell 103A, and able to communicate with your CPU at 110 to 9600 baud.

If you need hard copy at your fingertips, take a look at the HP 2621P. With a keystroke, its built-in 120 cps thermal printer will deliver a printout from the screen in seconds.

So why don't you check out the HP 2621 by calling the nearest HP sales office listed in the White Pages. Or send us the coupon. Then see for yourself how sophisticated a simple CRT terminal can be.

**Try this on your favorite CRT!** With the 2621P, you just hit a key and in seconds you have hard copy of your CRT display. The built-in thermal printer prints upper and lower case at up to 120 cps.

The 2621's bright, high-resolution CRT, with enhanced 9x15 character cell, displays the full 128-character ASCII character set, including upper and lower case, control codes, and character-by-character underline, in 24 80-character lines.

Eight screen-labeled preprogrammed function keys magnify the power of the 2621's keyboard. Preprogrammed functions include editing, terminal configuration, printer control and self-test.

To make numeric data entry faster and easier, we put the 2621's numeric keypad right in the middle of the keyboard. And the 2621's familiar 68-key keyboard is almost as easy to use as a typewriter.

☐ I'd like to know more about HP's new 2621A and 2621P with built-in hard copy.
☐ I'd like to see HP's new 2621A and 2621P with built-in hard copy.
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CIRCLE 39 ON INQUIRY CARD

# ple sophistication.

## Keyboard/Printer System Offers Large Buffers, 200-Char/s Transmission

Editing capabilities, buffer capacities, and transmission speeds provided by the model 4520 adapt it to use in data communications applications. Teletype Corp, 5555 Touhy Ave, Skokie, IL 60076, added the keyboard/printer system to its 4500 family to provide a means of attaining cost-effective data communications.

Designed for asynchronous multipoint networks where a common communications line is shared with a host computer, the 4520 operates under 2740 model 2 protocol. A network consisting of several terminal stations enables the computer operator to poll each station for messages, and send data to individual stations, groups of stations, or all stations. All online transmissions use the extended binary coded decimal code.

Buffer capacity of from 120 to 7600 characters enables operators to edit information in the receive or send/edit buffer. Approximately 15,200 characters of solid state internal buffer storage is provided for editing, sending, and receiving. Up to 7600 characters may be allocated to the send-edit buffer with the rest assigned to the receive buffer.

Capabilities of the system allow a computer's data base to be accessed and data to be sent to the terminal's receive buffer. The system detects errors due to faulty transmission under the 2740-2 start-stop protocol by performing a vertical redundancy check on each character and a longitudinal redundancy check on each test block. Blocks sent with an error are retransmitted automatically.

System console provides control keys, status indicator lamps, and a 3-digit display to indicate print position or error codes. The keyboard has several editing controls and a numeric pad; a lock provides security. The impact matrix printer operates at a rate of 47.5 char/s when data are waiting in the receive buffer. Forming legible characters from a 4 x 7 dot matrix, the standard printer uses a 15" (38-cm) friction feed platen and accommodates a removable tractor feed mechanism, handling forms from 3 to 15" (8 to 38 cm) wide.

Circle 184 on Inquiry Card

## Offline Laser Printer Produces Quality Output At 21,000 Lines/Min

A high speed, nonimpact printing system, the model 0777 is an offline unit that uses laser electrophotographic techniques to produce up to 21,000 lines/min. Among the benefits of the system, introduced by Sperry Univac, PO Box 500, Blue Bell, PA 19424, are page by page rather than conventional line by line printing, reduced inventory cost of preprinted forms, and improvements in printing scheduling.

System components consist basically of system controller, display console, disc drive, magnetic tape system, and printing station. This configuration expands through addition of a 10M-byte disc drive, second magnetic tape drive, and hardcopy printer console.

Control of the unit is attained from the operator's console. After loading a print tape, the operator initiates a job by simply keying in control information via the console keyboard. Standard single-part sprocketed paper is continuously fed into the printer for page by page reproduction.

Operators can interrupt jobs to stop or restart printing, display statistics, create or modify files of print information, or recover in the case of system error. Multiple copies can be repeat printed up to 255 times with no operator intervention.

The unit outputs at a constant speed of 29.167 in/s (0.741 m/s), and can print 6 lines/in (2.36/cm) at 10,500 lines/min, and 12 lines/in (4.7/cm) at 21,000 lines/min. Print line length can be up to 13.6" (34.5 cm). At 10 char/in, the unit will print up to 136 columns; at 12 char/in, it prints up to 163 columns; and at 15 char/in, 204 columns.

Fifteen different character sets reside on a flexible diskette. The system can intermix 10-, 12-, and 15-pitch fonts on the same print line. Other features of the unit allow graphic characters to be added or substituted to an already defined character set through graphic character modification.

A copy modification feature permits data on selected lines of selected pages of copies to be suppressed or changed. Specialized forms can be printed simultaneously with text printing via the forms overlay feature. By using disc storage the unit can print multipage reports in collated sets.

Price for a basic system including print station, tape and disc drives, controller, CRT console, and control software is $364,000. First deliveries are scheduled for the second quarter of 1980.

Circle 185 on Inquiry Card

## RO/KSR Units Expand Electronic Data Terminal Family

The 150-char/s model 820 receive-only, and 75-char/s model 825 keyboard send-receive and receive-only data terminals are the latest additions to the OMNI 800 line from Texas Instruments Inc, Digital Systems Group, 9777 W Gulfbank Dr, Houston, TX 77001. All three units provide optimized bidirectional printing with a 9 x 7 dot matrix character font, full ASCII character set, and operator programmable answerback memory.

Transmitting data at rates from 110 to 9600 baud, the 820 RO printer uses a FIFO buffer capable of storing 1280 characters for data overflow protection. This buffer adapts the unit to use as a demand printer interfaced with a CRT terminal.

Additional features include a printhead with a 150M impression printing life and a 132-col wide adjustable carriage for handling ticket forms, invoice, and purchase orders.

The front panel operator control keyboard provides reference to offline printing and control functions, terminal operating selection, and operator programmable answerback memory. A 3-digit LED terminal status control panel indicates the printer's next position, terminal status and configuration parameters, and gives the appropriate error code when an error condition exists.

Preprogrammable self-testing diagnostics verify power up and maintenance features. Accessible to the operator are the auto perforation skipper, automatic last character visibility, and programmable answerback memory capable of storing 21 characters for terminal identification.

The 75-char/s 825 RO printer communicates at rates from 110 to 600

# The Squeezable One

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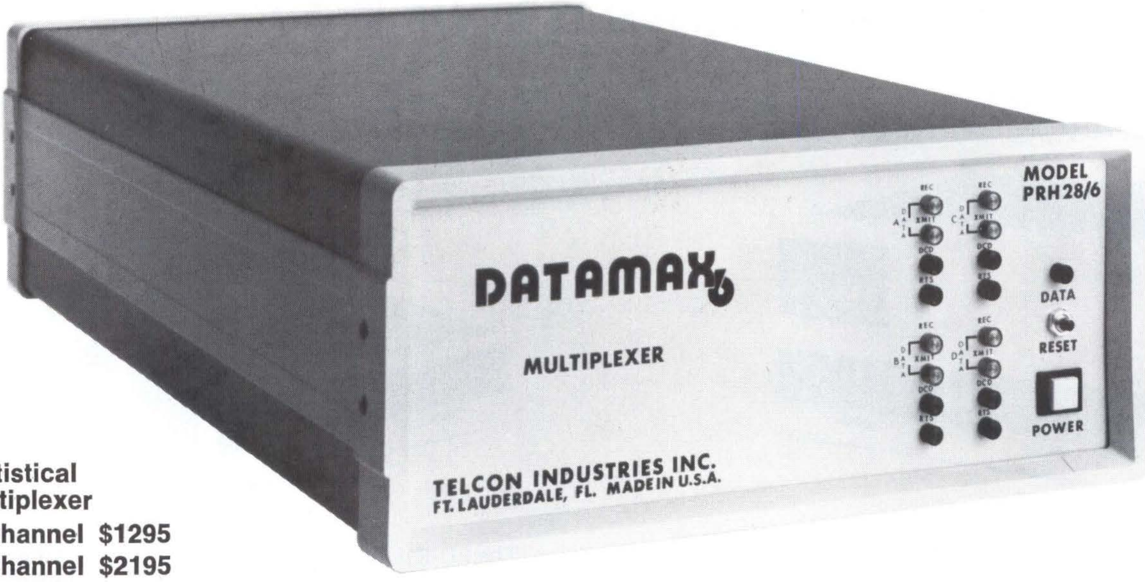


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*Leaders in Data Communications Since 1968* baud, and incorporates a 256-char FIFO buffer for data overflow protection. It has a 132-col adjustable carriage and produces an original and up to three copies. The KSR version of the model 825 provides all features of the RO version plus a full ASCII keyboard.

Circle 186 on Inquiry Card

## Integrated Transaction Processing System Serves Complex Applications

A COBOL based transaction processor, Reliance supports up to 128 transaction processing users on the Series 3200 minicomputer. The integrated software package, developed by Perkin-Elmer Corp, Computer Systems Div, 2 Crescent Pl, Oceanport, NJ 07757, consists of COBOL, data management, and transaction processing facilities. The package offers efficient program development, rapid terminal response, data integrity, and growth.

The package's ANSI-74 COBOL compiler eases program development. Automatic record locking, online transaction rollback, and system-wide recovery features offer data integrity and free the programmer to concentrate on application solution. Facilities are provided for batch simulation of anticipated transactions significantly reducing test time. Resource utilization and response time is maximum because each transaction requires only those resources unique to it, while terminal and data management components are shared by all users.

If additional terminals are required, users can expand the system to 128 workstations; a virtually unlimited number of disc drives can be added. Hardware, application, and environment disruptions are handled automatically. Database updates from incomplete or incorrect transactions are rolled back transparent to the operator.

An RPG II compiler designed for use with the system provides a batch oriented report generating facility. RPG II is also compatible with IBM System/3 RPG II.

Circle 187 on Inquiry Card

## Modular Computer Systems Packaged to Fill Range Of User Requirements

Reality family systems—2000, 4000, and 6000—meet user needs that range from entry level to database management, and are designed for optimum price/performance. Included in the systems, manufactured by Microdata Corp, 17481 Red Hill Ave, Irvine, CA 92714, are magnetic tape subsystems, 165-char/s matrix printers, and 150-, 300-, and 600-line/min printers, and up to 32 operator terminals.

In its basic configuration, the series 2000 includes CPU with 16k bytes of memory, Prism® CRT display terminal, 10M-bytes disc storage, 165-char/s matrix printer, and 25-in (64-cm)/s magnetic tape unit. The series can expand to eight terminals, 64k-bytes main memory, 20M-bytes disc storage, and 45-in(114-cm)/s tape drive. The matrix printer can be exchanged for a 150-, 300-, or 600-line/min printer.

Series 4000 expands from the basic model 4520 with 16k core memory to the model 4530 with a maximum of 64k memory and up to 32 Prism terminals. Standard with these configurations is a Reflex® Winchester type fixed disc subsystem with capacity for 20M, 30M, or 40M bytes.

Three models, the 6550, 6580, and 6790, comprise the 6000 series. The basic configuration 6550 includes 32k memory, 50M-bytes Reflex disc storage, two Prism terminals, and a 150-line/min printer. Both 6580 and 6790 feature MOS memory that is expandable to 128k. The 6790 also offers a Reflex disc system with storage capacity from 257.4M to 514.8M bytes.

An interactive screen processor, SCREENPRO™ guides the user through a menu driven sequence of steps to set up terminal displays and to provide for the simplified creation of programs for data input and file maintenance procedures. The package is comprised of a builder that prompts the user through construction of display screen formats, and a handler that makes previously constructed screen displays available to the Data/Basic™ software programs. □

Circle 188 on Inquiry Card

# Vision Expands Robotic Skills For Industrial Applications

**Sydney F. Shapiro**
Managing Editor

Robotics has been an important factor in the advance of industrial automation for many years, especially in the diverse manufacturing processes. More recently, the technologies of both robots and automation have progressed dramatically because of the application of microprocessors. Yet even those advances seem to be hindered by lack of one robotic sense: vision.

Considerable research has been conducted in an effort to develop feasible vision systems for robots, in particular, solid state TV cameras, photodiode arrays, and CCDs. Although not yet fully successful, that research is continuing both in the United States and in several foreign countries—notably Japan—and it appears that industrially practicable systems may soon be available.

Within the United States, several federal groups—particularly the National Science Foundation and the National Bureau of Standards—and private organizations—the Society of Manufacturing Engineers and the Robot Institute of America—have been instrumental either in financing research for all phases of robotics or in pressing for greater use of robots. In addition, private firms such as General Motors and other automotive manufacturers finance research and development programs in their laboratories as well as in colleges, universities, and independent research centers. In Japan, one of the foremost foreign nations in the advancement of robotics, the Japan Industrial Robot Association is a key organization for stressing development.

### University of Rhode Island Research Progress

Under one of many grants supported by the National Science Foundation for research in robotics, a team at the University of Rhode Island has been developing "general methods for robots with vision to acquire, orient, and transport workpieces . . . to assist in increasing the range of industrial applications" for such robots.[1] This research team, headed by Drs John Birk and Robert Kelley, has developed an experimental robot system—based on a 6-axis arm—that uses vision to locate and pick up arbitrarily oriented workpieces in a bin, again uses vision to determine orientation of the workpiece in the robot's hand, and then manipulates the piece so as to transport it to a goal site and insert it without collision. Several alternative paths exist for removing unoriented workpieces from containers and feeding them into machines (Fig 1).

Evolution of the current experimental system at the University of Rhode Island, which essentially enables use of the path shown in heavy lines in the figure, was carried out in three stages. The first stage included workpiece orientation classification in the bin to aid acquisition. Attempts to use binary image analysis failed. Orientation classification by hand, used for the second stage, was more successful and simplified use of image analysis to determine workpiece orientation. During both of these phases it was assumed that workpieces would be classified by arbitrary orientations.

Components of the third stage comprise robot arm, two General Electric TN-2200 solid state TV cameras, sources of illumination, supply of workpieces, and goal site. The relatively simple arm has six degrees of freedom and can completely position and orient a workpiece.

One camera is mounted on the robot arm facing downward and parallel to the Z axis; it is used both to view the bin containing workpieces and to confirm proper placement of each workpiece at the goal site. The second camera is mounted to the workstation and faces parallel to the minus X axis. Aligning the cameras to robot axes of motion simplifies transformation from camera to robot coordinates. Camera resolution is 128 x 128.

Separate lighting systems accommodate the two cameras. Two lights are mounted beside the arm camera to illuminate the bin; two others, for the workstation camera, illuminate workpieces in the robot hand.

In operation, data from the arm camera are analyzed to locate regions where workpieces can be grasped by a vacuum gripper on the arm. This gripper, hanging from a spring, can adapt to surfaces angled at up to 45°. A piston connected to the gripper permits the workpiece to be held firmly once acquired. The workstation camera computes orientation and position of the workpiece relative to the hand. At this point, lights for the arm camera are turned off under computer control to eliminate interference with analysis of the workpieces via data acquired by the workstation camera. If those data are inadequate for making a decision about orientation, the arm rotates the workpiece to provide another view.

Two goal sites, each hemispherically approachable by the robot hand, are provided so that all workpieces can be transported and placed on one of them regardless of orientation in the hand. One goal site functions as a regrasping station; the other is an insertion tool that the arm can pick up. When the workpiece is placed correctly in the insertion tool, the workpiece can be delivered to a goal site without collision. One site receives workpieces rotated 180° about a horizontal axis relative to the other so that the two sites closely satisfy the requirement of being able to receive all pieces in the hand.

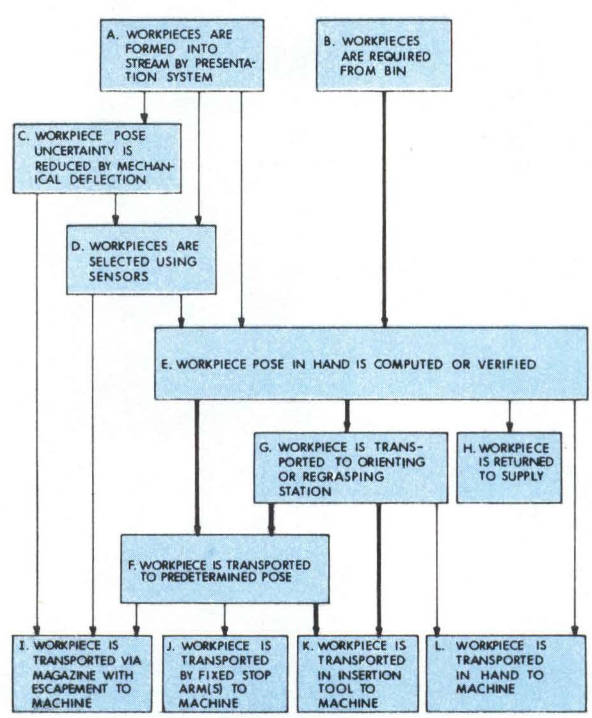



Fig 1 Alternative approaches to feeding machines with workpieces.[1] Paths shown as broad lines indicate current research at University of Rhode Island to develop robots with vision that will pick up, adjust position, and move workpiece to machine. Solid state TV camera locates workpieces in bin and determines orientation for pick up by robot hand. Second camera then checks orientation in hand for proper placement at machine without collision

Although some robots have fewer axes of motion, the University of Rhode Island Mark IV arm has six: three linear and three rotary. The researchers believe that this will better enable future workers or central computers in batch manufacturing applications to reprogram the system for feeding a variety of workpieces to different machines.

Repeatability of the arm is ±0.0001″ (0.00254 mm) for each linear axis and ±0.007° for each rotary (wrist) axis. Total travel for X, Y, and Z linear axes is 36, 24, and 24″ (91, 61, and 61 cm), respectively; for $\theta_4$, $\theta_5$, and $\theta_6$ rotary axes, it is 286°, 233°, and 310°, respectively. Maximum linear velocity is 12 in (30.5 cm)/s and angular velocity is 0.771 rad/s.

A servo system interfaces to a Computer Automation 16-bit robot minicomputer for control of the six axes (plus two more provided for possible future use). The digital interface accepts parallel computer input commands including a *home* signal that causes all axes to move in a negative direction until a home switch is sensed, at which time the encoder counter is set to zero, an *axis select* signal to choose one of the six axes, a *read/write* signal that determines if position should be read or written to the controller, and *position command* signals that indicate absolute position in binary. Format is two 8-bit bytes, with the first byte transferred being most significant.

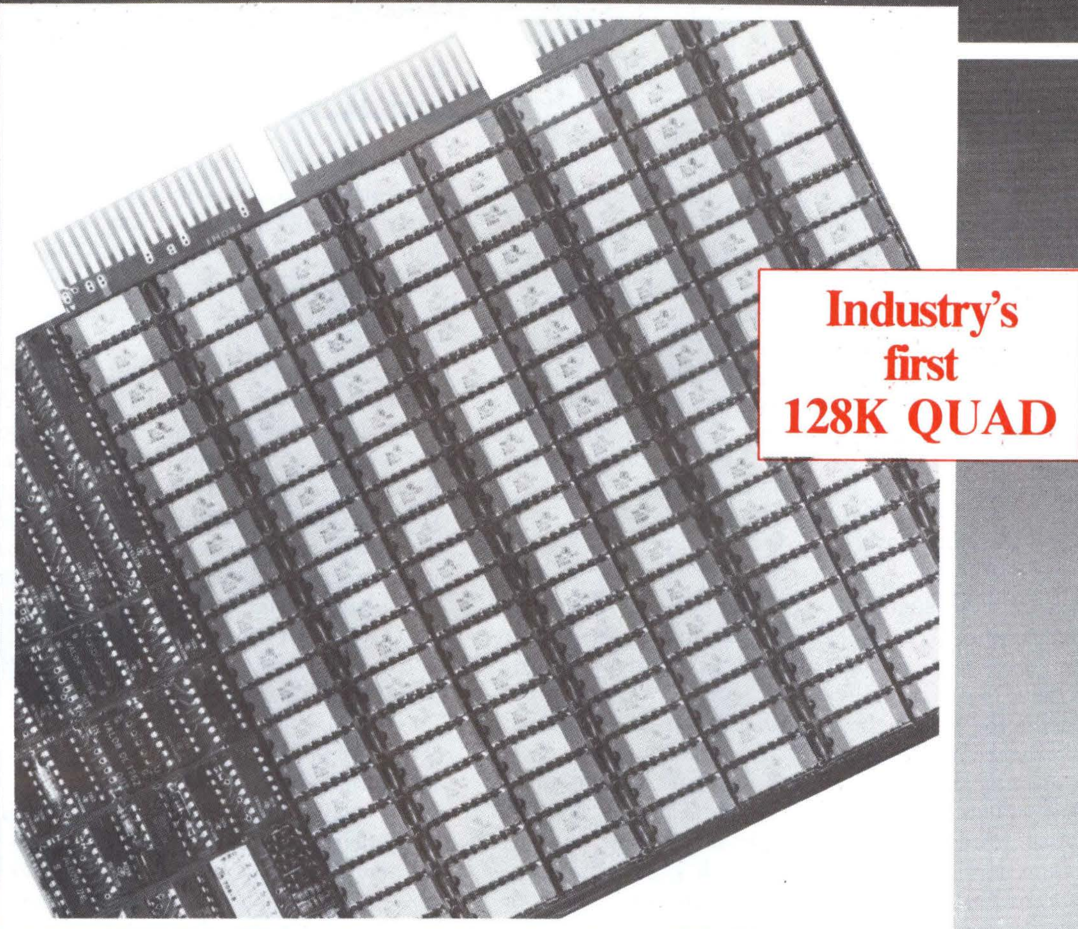
Other signals are *shift line* to determine which byte is being written or read, *start* to initiate reading or writing of position information, *ready* to indicate when all axes are in position, *reset* to reset all controller logic, *limit switch interrupt* to indicate that an axis reached a limit, and *limit switch word* to decode which axis reached the limit.

A nonlinear stabilizing circuit allows high accelerations to be achieved on an axis without overshoot. Speed is reduced smoothly as the destination is reached.

Analog lock circuitry allows fine positioning and high repeatability. Also, the controller can position each axis at an absolute home position. Adjustable optical limit switches and positive mechanical stops restrict motion of the work table. Ready and limit indicators are provided for each axis and the current position of each axis is shown on a LED display on the front panel of the Anorad controller. This controller multiplies by four a 2-channel, 250-pulse/r sinusoidal wave output from encoder units to provide an angular resolution of 0.36°/pulse.

A program written to measure wrist repeatability causes an axis to servo to a destination, pause, return to the original position, and then stop. Deviations of all moves are measured and data are collected for moves of ±10°, ±45°, and ±90°.

Dr Birk believes that this experimental unit is the first integrated system for feeding parts with completely arbitrary orientations in a container. At the time the last report[1] was published, average time to feed a workpiece was 45 s and each piece could be placed with an accuracy of 0.25″ (6.38 mm) and 5°. The speed is considered to be slow for most machine load-

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**CIRCLE 44 ON INQUIRY CARD**

ing applications, but the accuracy is reasonable. However, for NC machining centers that have relatively long cycle times, or for use in loading systems that must handle heavy loads (eg, 100 lb, 45 kg), these specifications may be adequate.

Improvements expected before completion of the project include a direct memory access interface for the cameras that will significantly improve quality of images. In addition, the time required to input an image should be reduced from approximately 1 s to about 0.5 s. Velocity control of arm axes will also permit the arm to be moved faster when it is acquiring pieces from the bin and when placing those pieces at the goal sites.

### Online and Developmental Industrial Applications

Research and development in machine vision has been stressed continually by several manufacturers, particularly for use in automotive production plants. Robots have been in use at such plants for some time, but usually for welding operations, lifting heavy loads, or performance in potentially hazardous locations. Success in meeting these requirements has led to the realization that robots would be even more useful if they could "see" and could make decisions among alternative actions based on variations in job situations.[2,3,4]

There are estimated to be 5000 industrial robots currently in use. Of these, approximately 150 are performing a variety of jobs at General Motors plants; but, more importantly, another dozen or so are being used for development of new uses in the corporation's Tech Center and laboratories.[2]

Of the robots in production areas, most operate in a fixed sequence; that is, the parts on which they function must be stationary and must be positioned exactly. There can be no variations in orientation or attitude. Although such robots function well within their limitations, they sometimes lack in efficiency.

Efforts toward providing machine vision at GM have resulted in a fully integrated production prototype machine vision/industrial robot system that adaptively reacts to visually sensed changes in workpiece type and placement.[3] Since 1968, a major goal in GM research has been to develop robots that could handle real-life production conditions, for example, finding parts on conveyor belts, determining orientation, picking up the desired part, and assembling it on the item being built.

Most second generation laboratory robots are controlled by minicomputers and can be used for more complex operations. Some have sensory input and the capability to adapt automatically to changing situations.

Early experiments were based on a Unimate 2000 robot with a Data General Nova 1220 minicomputer substituted for the standard control hardware.[2] Part location data were transmitted to the robot from a General Electric 128 x 128-element solid state camera that was connected to a Digital Equipment PDP-11/40 minicomputer. The latter computer ran a simple program to find the center of white objects on a black conveyor belt.

Although this robot could pick up plastic cups as they passed by, it could not reliably sense real parts under production conditions. However, the robot control was found to be capable of operating with a better vision system, one that used displacement of a projected line of light to detect parts regardless of color or reflectivity.

A prototype system being developed for production testing and evaluation is based on a Cincinnati-Milacron 6 CH robot because that robot was considered to have the only commercially available computer based control that could readily accept visual guidance. This robot is modified with an RS-232 serial communications link and associated software handlers. Robot actions are directed by a perception system that recognizes the identity and position of each part, assembles instructions for new part handling sequences, senses and keeps track of conveyor belt motion, and transmits appropriate instructions as the part moves within reach. At the end of each task the robot asks for new instructions. These are provided by the computer and perception system.

To train the vision system to accept new parts, appropriate parameters of the parts are selected and minimum/maximum values are entered for each. Normally the robot is taught by steering it manually through the required motions and recording end point positions for future play back. Robot and perception system software eliminate the need for the operator to be concerned with details of camera to conveyor to robot spatial transformations and calibrations.

With the patented Consight-1 lighting apparatus, a narrow, intense line of light is projected across the surface of the conveyor belt (Fig 2).[3] As the object

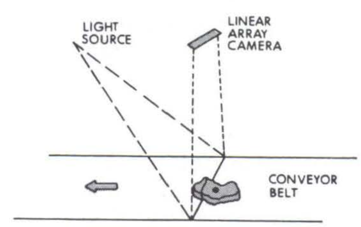
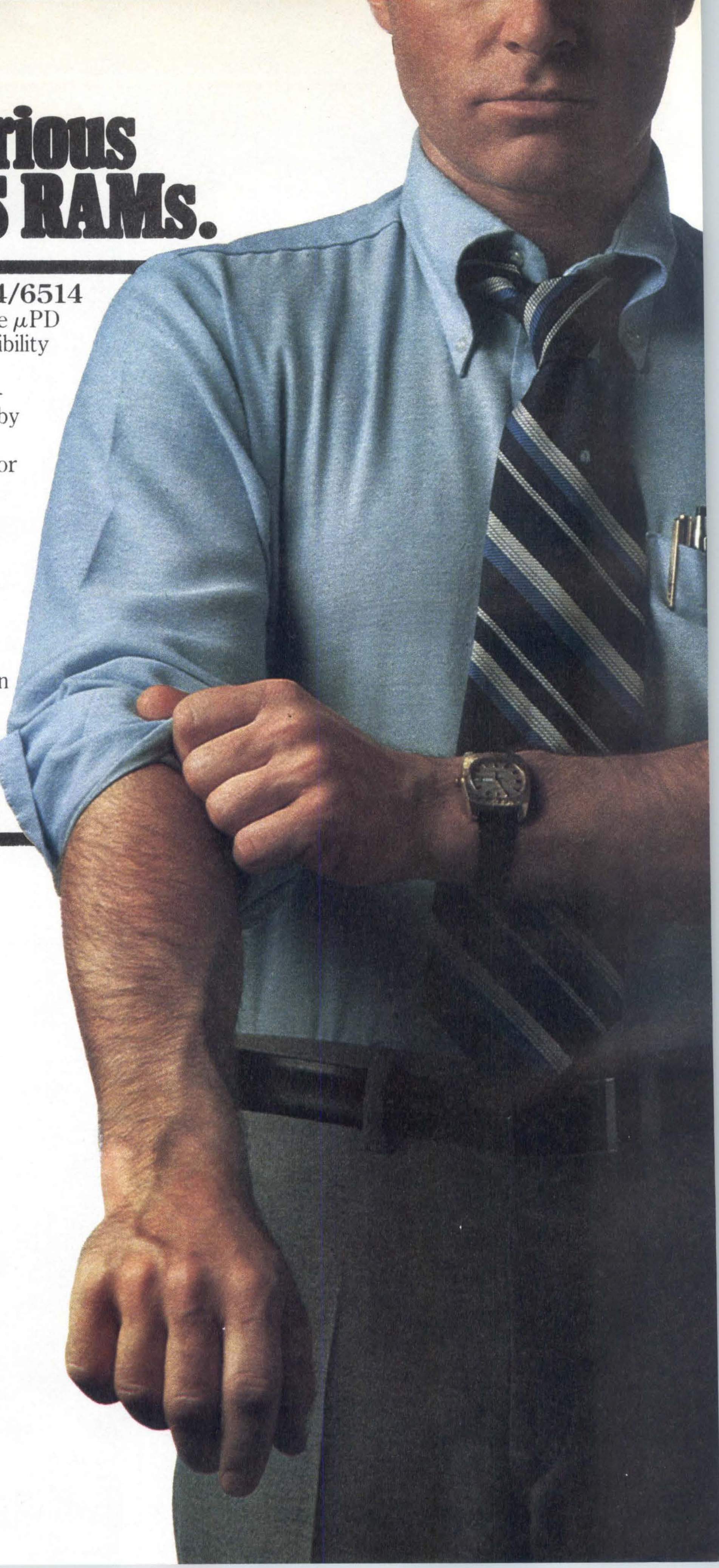
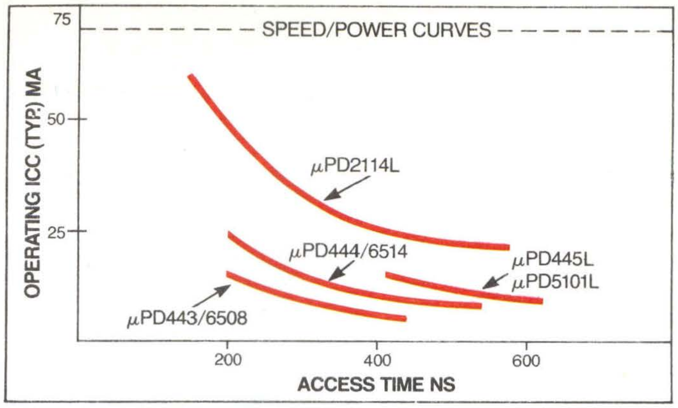



Fig 2 Principle of Consight-1 lighting apparatus.[3] Reflection of narrow line of intense light to camera is interrupted, indicating presence of part on moving belt. Multiple light sources, aimed from different locations, eliminate shadowing errors



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|---|---|---|---|---|---|
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| μPD444/6514C-1 | 300 ns | 60 mW | 18 | .065 μW | .022 μW |
| μPD444/6514C-2 | 250 ns | 75 mW | 18 | .065 μW | .022 μW |
| μPD444/6514C-3 | 200 ns | 95 mW | 18 | .065 μW | .022 μW |
| μPD445LC | 650 ns | 45 mW | 20 | 100 μW | 1 μW |
| μPD445LC-1 | 450 ns | 75 mW | 20 | 100 μW | 1 μW |
| μPD5101LC | 650 ns | 45 mW | 22 | 1 μW | .016 μW |
| μPD5101LC-1 | 450 ns | 75 mW | 22 | 1 μW | .016 μW |
| μPD443/6508C/D | 450 ns | 25 mW | 16 | 5 μW | .3 μW |
| μPD443/6508C/D-1 | 300 ns | 45 mW | 16 | 5 μW | .3 μW |

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enters the line it prevents light from reaching the belt surface. To a linear array camera positioned above the belt the line then appears deflected from its target. Brightness indicates an unobstructed belt surface; darkness indicates presence of a part. To eliminate shadowing effects, two or more light sources are aimed at the same strip across the belt.

Three computers are used. A vision system computer reads and analyzes the linear array camera data and reduces those data to spatial coordinates of the part center of area relative to the line of light, part orientation, and part identification. Transformations between Cartesian coordinates and the 6-axis jointed-spherical coordinate system of the robot are calculated by a second computer, and a third supervises interaction of all system components.

A Consight production prototype uses an enhanced Cincinnati-Milacron T3 robot with its 1270-mm/s operating speed increased to 2500 mm/s, and an adaptive branch function provided for external modification of the robot program.[5] In place of the single control computer, a Digital Equipment PDP-11/34 minicomputer controls vision, a Digital Equipment LSI-11/03 microcomputer monitors the activities, and a controller within the T3 controls the robot.

Much more sophistication is afforded the monitor subsystem in the production system than for the experimental unit. The microcomputer implements part programming and queues multiple parts. Cycle time for a simple pick up, transfer, and put down operation is reduced to 5 s with a belt speed of 20 cm/s.

In still another application, a robot with vision is used at an assembly station to attach covers to automobile air conditioning compressors.[6] The station is made up of a Unimate 2000B manipulator with a special gripper, an X-Y table, a 100 x 100-element General Electric Z7891 solid state camera, a Digital Equipment PDP-11/40 supervisory minicomputer, and a Digital Equipment LSI-11 slave microcomputer for robot control (Fig 3).

A binary image of the compressor housing is processed by the minicomputer to determine midpoint and orientation of the centerline between bolt holes. After the X-Y table positions the centerline midpoint at the center of the camera's field of view, the robot picks up a cover from its fixture, rotates it to the proper attitude, and pushes it down over the compressor housing. Through several succeeding steps, the robot picks up an impact wrench, inserts eight bolts, and tightens each bolt. At each step, the camera views the operation, eg, to be certain all bolts are in place and properly tightened. The entire assembly operation requires about 160 s.

Still another research project in robotic vision is underway at the National Bureau of Standards' Center for Mechanical Engineering and Process Technology. Roboticists there have developed a prototype industrial robot that can see for about 1 m. This robot has a small, solid state TV camera mounted on its wrist with

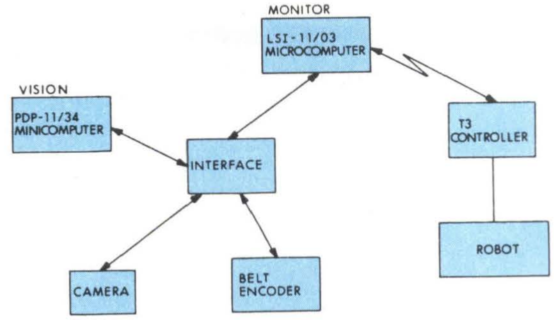


Fig 3 Production prototype hardware of Consight system.[5] System interface accepts data from camera, automatically thresholds them, and sends only transition points between black and white segments to vision minicomputer. Interface also passes position data from vision minicomputer to monitor microcomputer

its field of view between two finger grippers. A strobe light, mounted just below the wrist, flashes a narrow plane of light toward the fingers so that the robot sees an object in its field of view as a narrow line of light across the object.

A microcomputer, which also controls flashes of light from the strobe, determines the distance of the object from the grippers, as well as the object's orientation. The computer judges position and orientation from apparent shape and position of the bar of light on the object. If the robot is not positioned correctly to pick up the object, the computer moves the robot to another position and again views the object to determine if its orientation is proper for pick up.

Considered innovative in this system is the use of a strobe to provide optimum light to the camera. The robot microcomputer controls timing and intensity of strobe flashes through a feedback system that compares images frame by frame. Background light can be filtered out electronically to obtain clear images under a variety of lighting conditions. Further research is underway on refining the capability of the robot to locate a desired part from among different kinds of objects and to simplify reprogramming to handle a variety of jobs.

### Status of the Robot Industry in Japan

Almost simultaneously, Japan imported its first industrial robot from the U.S. in 1967 and developed its own first prototype in 1967-68.[7] Possibly to even a greater degree than in the U.S., Japan's automobile industry is the biggest single user of its industrial robots, about 30 percent of the total.

A longterm demand forecast made from a 1977 survey by the Japan Industrial Robot Association indicated that 1980 and 1985 production of industrial robots will be, respectively, 5 and 15 times that of the 1977 figure. This survey stated that about 70 university and governmental research laboratories were then engaged in research on robots. There were about 300 researchers operating on a budget of approximately 2M dollars (400M yen at that time), not including personnel expenses. Both university and public research organization facilities now concentrate on artificial intelligence, pattern recognition, computer applications for control and instrumentation, and automatic control techniques. Visual sensors have been consistently stressed —but not to the detriment of other sensory recognition techniques.

Three categories of measurement and recognition techniques are being studied, typified by tactile sensors, electric measurement sensors, and image sensors (vidicon cameras, image dissectors, photodiode arrays, and charge coupled devices). However, more recently speech recognition has been added to the areas of study. In 1974, patents issued in Japan for tactile, internal measurement, and visual sensors numbered 2, 7, and 4, respectively. In 1975 and 1976, the numbers were 5, 11, and 4 and 4, 8, and 4. However, in 1977, the totals were 10, 8, and 11, indicating greater advances in development of visual sensors.

Among the Japanese manufacturers of industrial robots having vision sensors for recognition functions are Hitachi, which uses vidicon cameras for shape recognition and positioning of transistors in die bonding as well as for remote inspection within nuclear power plants. In addition, such cameras are designed into robots by Mitsubishi Electric for shape recognition and positioning of assembling and transistor die bonding, by Yasukawa for arc welding, and by Kawasaki Heavy Industries for assembly. Toshiba Electric uses semiconductor image sensors for similar tasks in transistor die bonding.

## Summary

Because research in robotics underway in the United States and in many foreign countries, such as Japan, is so extensive, only a relatively small area of progress has been discussed here. Projects funded by the National Science Foundation and private organizations are continuing and unquestionably will expand as breakthroughs occur and as industrial robots become more practical.

What effect the changing economic situation will have on the advance of robotics—or vice versa—is indeterminate. However, it is estimated that large robots with enhanced control capabilities and sensors—such as vision—will be available during the 1980s for $80,000 and that smaller machines will cost $40,000 or even less.[2] Unquestionably, such robots will be able to perform certain tasks faster, more reliably, and cheaper than human operators. Economists and manufacturers will unfortunately have to consider many factors in determining how to balance technological advancements with the need for more jobs.

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## DC&AS BRIEFS

### Data Collection Terminals Function in Harsh Environments

Plant information on inventory, work in progress, machine downtime/usage, and personnel attendance can be collected for management reports with the model 2802 data transactors introduced by General Automation, Inc, 1055 S East St, Anaheim, CA 92803. Each contains complete alphabetic keypad, 10-digit numeric keypad, and 24 programmable function keys. All keys are oil, dust, and moisture resistant and the terminals are housed in rugged steel cabinets for operation in harsh industrial environments. Other operator function components include a 32-char alphanumeric display with integral time clock and a reader for 10- to 22-char alphanumeric badges and 80-col punch cards.
Circle 160 on Inquiry Card



### Programmable Controller Is Readily Programmed

Programmable from existing ladder diagrams, without modification and with only minimal instructions, the D120 programmable controller from Cutler-Hammer, PO Box 463, Milwaukee, WI 53201, performs without cooling fans or air conditioning at temperatures up to 130 °F (55 °C) and relative humidity up to 95%. Features include CMOS circuitry, integral power supply, and I/O boards in a single chassis. Typical specifications include 256-, 512-, or 1k-word RAM or P/ROM and capacity of up to 400 I/O channels.
Circle 161 on Inquiry Card

### Microcomputer Fits Into Control System Network

A family of realtime, industrial microcomputers called RacPac[R] by manufacturer Process Computer Systems, Inc, 750 N Maple Rd, Saline, MI 48176, meet requirements for both host/development and target/remote systems. The first unit announced, the 3935A, contains integral 5" (13-cm) CRT, panel mounted keyboard with external connector, 12-slot card cage, three furnished system boards, and 10-A power supply. Software is also provided.

Of the system boards, the CPU board provides Z80 performance enhanced by extended arithmetic capabilities of an APU processor. It has switch selectable rates from 50 to 9600 baud, switch selectable base starting address, nonmaskable interrupt for a power fail detecting device, five vectored priority interrupts, four interrupt modes, and system DMA capabilities.

The second board provides CRT and keyboard support. It uses 1k-byte RAM as a display buffer for the CRT, with the RAM base memory address set on any 1k boundary between 0 and 63k.

The third board features software selectable 10-ms to 1-min interrupts, realtime clock with software initialization, 30-day battery with status monitor, two sockets for 1k-, 2k-, or 4k-byte EPROMs, jumper selectable EPROM select, switch selectable base starting address, and switch selectable memory enable/disable.

Software for the system, called Spurcom, offers a base operating system, communications support, and software debug facilities. Standardization between host and target processors permits users to test software on a development system and download to a target machine without software changes.
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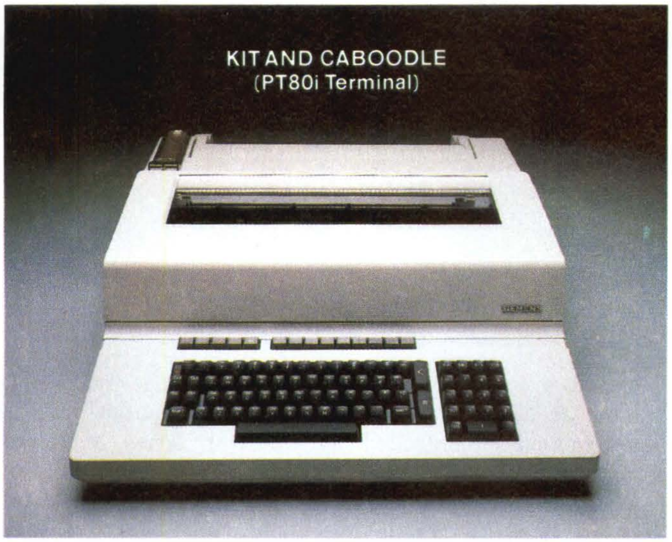



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Either ladder or logic diagrams can be used in programming the MPC-8/02 programmable controller through a portable MPC-8 program loader/monitor. Available from Dynage, Inc, 1331 Blue Hills Ave, Bloomfield, CT 06002, the unit handles up to 2048 digital and 256 analog I/Os, has up to 20k program and 12k scratchpad memory, and enables programs to be changed by a host computer. It is applicable for both small and large control systems. Because each input is sampled twice for agreement before being recognized, input errors are reduced. Fully debugged programs can be transferred to EPROM for long term use.

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### Programmable Controllers Designed For Small Systems

Small processes with as few as 4 inputs and 4 outputs or as many as 30 inputs and 32 outputs can be economically controlled by the ICM series of microprocessor based programmable controllers. All are programmed from ladder or logic diagrams with not more than 16 instructions. Ultraviolet light erasable P/ROMs of 512, 1k, or 2k capacities store program instructions. Construction is modular, with plug-in power supply and CPU boards held in place with four screws each and I/O modules secured by single screws. P/ROMs plug into sockets on CPU boards. These systems, from Divelbiss Corp, Fredericktown, OH 43019, interface with 90- to 140-Vac or 10- to 32-Vdc input signals and can control output loads of from 12 to 140 Vac or 0 to 60 Vdc, both at 3 A max.

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# SEMICONDUCTOR ADVANCES BOOST DIGITAL IMAGE PROCESSING SYSTEM PERFORMANCE

Current dual-ported refresh RAM and pipeline processor techniques applied to standalone interactive systems have enhanced digital image processing and analysis of black and white or full-color 2-dimensional data for high resolution and large dynamic range data extraction

**Harry C. Andrews** Comtal Corporation, Pasadena, California

Digital image processing generally involves mathematical transforms for image analysis, coding to permit image compression, enhancement for improved image display, restoration for elimination of image degradation, and investigation of image recognition and classification. Processing techniques have progressed to where large dynamic range imagery—10 bits or 1024:1 signal to noise ratios—are prevalent—and high resolution imagery—$10^8$ pixels (or picture elements) in a single image—are possible in system architectural designs. Currently, the state of the art of digital refresh black and white imagery is between 512 by 512 by 8 bits (X3 for color) and 1024 by 1024 by 8 bits (X3 for color) presented at 30 frames per second.

Constraints caused by flicker and horizontal bandwidths will probably not yield significant design breakthroughs in these characteristics within the near future. However, digital image processing evolves steadily in sophistication because of recent design advances in multiplexed data channels, pipeline processors, refresh random access memories (RAMs), and color shadow mask and monochrome monitors. These advances in technology are due to the increasing demands of interactive realtime digital image data exploitation.

Early digital image display systems were usually peripheral devices, consisting of either digital discs or charge-coupled device (CCD) shift registers as simple refresh memories, with little additional capability. Such device oriented systems offered only single-pixel monochrome or pseudocolor enhancement. However, these systems had the capability to display in real time, without photographic processing, the results of algorithm development procedures implemented on the imagery in a host machine. Experience with these peripheral display systems, attached to various host computer facilities, soon demonstrated the inefficiency of such configurations. Specifically, a host machine, cycling around to the interactive station port, at the same servicing rate as for the other ports, was considerably less than interactive. The solution was for the interactive port to "capture" the host, obviously unacceptable to other host ports. However, even if the display station did have complete control of the host, the standard input/output (I/O) channel rates of 1M bytes/s were much slower than acceptable for efficient interactive image processing. Consequently, the concept of offloading certain functions to the frontend display developed to minimize image I/O processing rates. This offloading from host to display caused considerable architectural problems, as the frontend terminal, to be truly interactive, had to process data at the rate of 10M pixels/s or more. These constraints led to the design philosophy of the standalone or interactive digital image processing system.

## System Design Principles

Standalone system design has only one interfacing or realtime criterion. Essentially, all processing on a single frame of data must be performed in less than 1/30 s, so that a human operator is visually and manually involved in the process of image manipulation; otherwise, processing operations are not considered as real time within this context. This design constraint precludes I/O to foreign hosts, array processors, or other off the shelf processors with interfaces less than 10M pixels/s. A pixel is typically 1 bit deep (ie, on or off) for raster graphics, 8 bits (ie, 256 levels of gray) for monochrome imagery, 16 bits for radar imagery, 24 bits for true color imagery, and 32 bits for 4-band multispectral imagery. The 10M-pixel/s rate comes from the horizontal bandwidth of a 512 x 512 display refreshed 30 times/s. For a 1024 x 1024 display, the processing rate rises to 40M pixels/s. At these rates, design architectures and image array processes have to be intimately built into the refresh memory structure of the interactive system.

Recent architectures have capitalized on the decreasing cost and increasing availability of dual-ported RAMs, which afford multiple access to a common expandable data base; for example, 4096 x 4096 x 8-bit pixel memory images are possible with dynamic partitioning to provide a multiplicity of applications. With a window size of up to 1024 x 1024 pixels, realtime roaming through the data base is possible with zooming, and 3 x 3 arbitrary convolution filters followed by both linear and nonlinear function memory combinations can process a 512 x 512 x 8 monochrome image in 1/30 s, equivalent to one television (TV) time frame. Convolution is the process of linear spatial filtering to cause a single pixel in the image to be modified as a function of its surrounding pixel values.

Typically, convolution is implemented by sliding a kernel matrix (ie, a set of weighting coefficients) over each pixel in the image and replacing the center pixel by the linear sum of the coefficients of the kernel

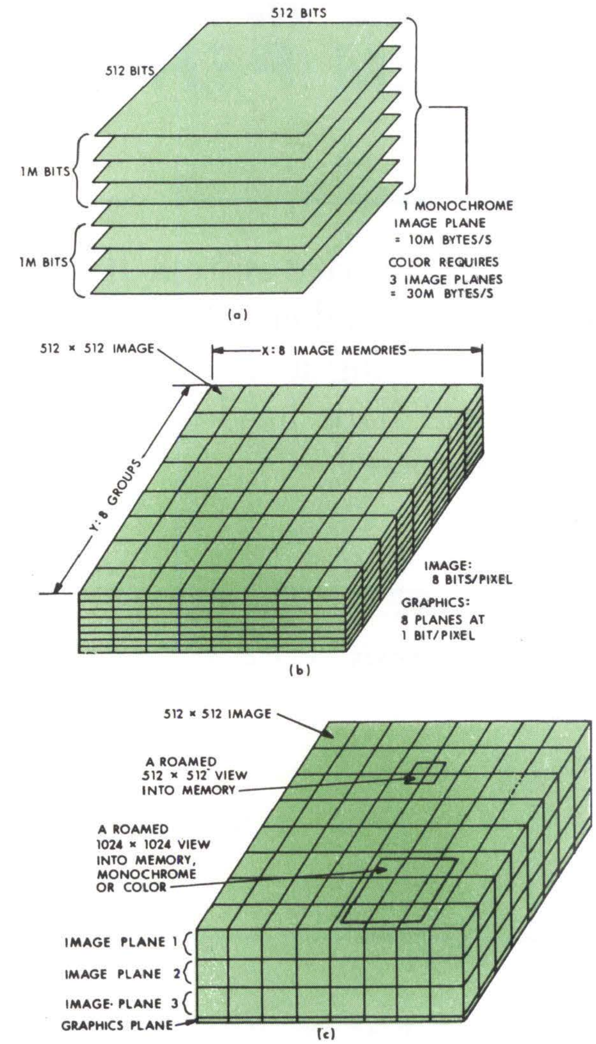



Fig 1 RAM architecture. This organization is structured in contiguous blocks for dynamically allocating memory to monochrome, true color, or multispectral applications. Architecture allows for stacking of images or abutting of images under keyboard control. Single 512 x 512 x 8-bit image memory (a) and virtual address space (b) are shown, along with arbitrary, but common, configuration (c)

multiplied by the surrounding pixels. For a 512 x 512 image to be filtered with a 3 x 3 kernel in 1/30 s requires 70M operations/s. With graphic overlay memories, such image processing techniques as annotating, labeling, outlining, and monochrome or color correcting are possible. Due to the dynamic allocation of database memory, digital loop movies (the sequential readout of different sections of refresh memory) in real time are feasible, as are left-right, right-left, up-down, or down-up scrolling of new imagery into the refresh memory and viewing window. Pipeline processing, freeze frame iterative image array feedback, and firmware burned control and instruction commands are among the image processing techniques presently utilized in interactive system design.

## Refresh RAM

A refresh RAM is usually designed as 512 x 512 x 1-bit planes [Fig 1(a)], cycling at 800 ns/bit or spatial position. Four such planes are packaged to provide 1M bits of 16k RAM, or one half of an 8-bit image. A full 512 x 512 x 8-bit monochrome image requires eight planes. In turn, 64 of these planes (at 8 bits deep) represent a 4096 x 4096 image in refresh memory at one time [Fig 1(b)]. The architecture is structured so that each bit plane can be interpreted as a raster graphics plane. In addition, readout addressing can be organized so that image planes can be "stacked" to represent true color (three image planes), monochrome with four graphics (one and one-half image planes), or true color with four graphics (three and one-half image planes), as depicted in Fig 1(c).

Because all bit planes are in synchronization, it is possible to offset the X, Y starting location, thereby providing arbitrary roaming capability. For a 4096 x 4096-image base, a total of 64 separate 512-image planes are roamable, with as small a step as 1 pixel. In general, an image memory structure can be dynamically allocated, so that an L•512 x N•512 x M•4 deep data base can be dynamically redefined, where L is the number of vertical images, N is the number of horizontal images, and M is the number of 4-bit deep image or graphics planes.

Refresh RAM is handled by three separate I/O control functions (Fig 2). First, image refresh I/O control provides random addressing for loading. This process takes advantage of dual-ported memory to allow slow loading into random locations at random rates, thereby allowing refresh memory to be asynchronously loadable from any external device running slower than 80M bits/s. Both single-line and single-pixel loading and reading formats are possible. Automatic addressing increments are also provided for burst load modes, when needed, as in direct memory access transfers and with online image sensors.

Eight directions of pixel loading may be accomplished, thereby allowing horizontal, vertical, 45°, or 135° readout of and/or writing into refresh memory at synchronous rates. Thus, the memory can easily be used for corner-turning algorithms, prevalent in many image processing applications, where 90° image rotations and transpositions are necessary.

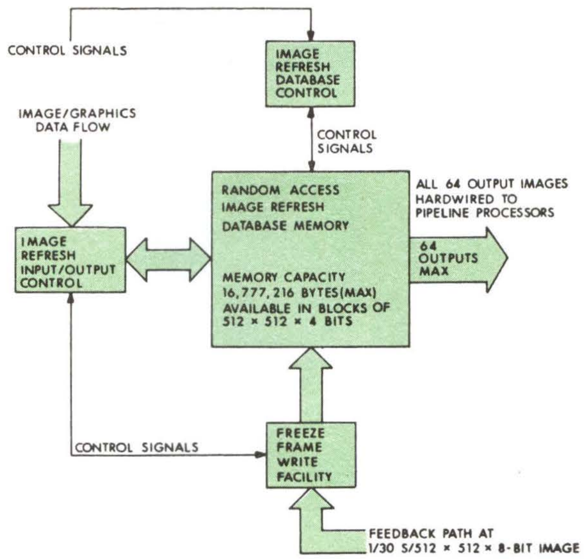
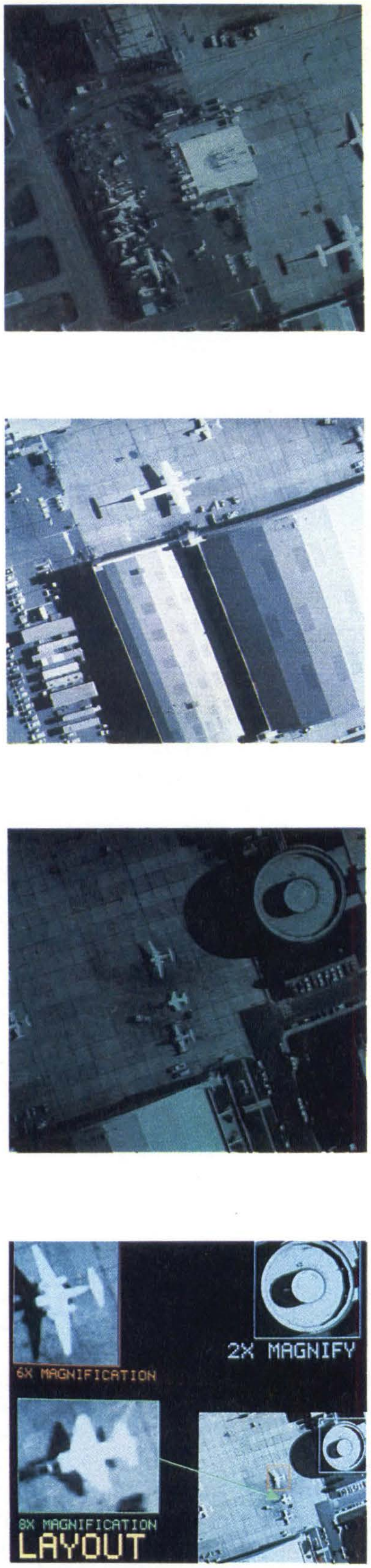



Fig 2 Controlling dual-ported refresh RAM. Control is accomplished with three different functions. First is random I/O to RAM. Second is offset readout (for roam) and X2 or X4 slowdown (for zoom). Third is freeze frame writing back into memory for video input and feedback array processor storage

Second, image refresh database control defines the offset memory values for arbitrary roam positioning. This control is a raster addressing circuit that designates the starting pixel (usually, upper lefthand corner) of each image plane at that roam location. Because this address can change rapidly, roaming is done quickly with respect to operator response. Roam addressing is changed during vertical blanking of the display, thus permitting a smooth or continuous roam without interference to the displayed scene. Image refresh database control also provides for two times (X2) and four times (X4) magnification (zoom) at any location in memory by two or four times replication. A visual illustration of this technique is shown




(a)

(b)

(c)

(d)

Fig 3 Zooming and roaming capabilities. This sequence of displays [(a) through (d)] illustrates use of zooming and roaming simultaneously. Note ability to move to and extract selective sections of image for examination and greater magnifications

in Fig 3, in which an aerial overview is presented with a X2 zoom and roam to the lower righthand quadrant and another roam (still at X2 magnification) farther to the right of the scene. Magnification is implemented in real time by slowing memory output by a factor of two (or four, respectively), and reading every pixel twice (or four times). Thus, although memory output is decreased by a given factor, the double (or quadruple) reading rate brings the output data up to the original digital TV refresh rate, thereby accomplishing two times or four times zoom instantly. Because this control also defines roam offset, both roam and zoom are easily coupled.

Since roam offset addressing can be changed often, it is possible to regularly pass through memory in a controlled manner. Therefore, loop movies are available. Size and extent of the movie are determined by the amount of memory sequenced; a 64 sequence for $512^2$ frames, a 256 sequence of $256^2$ frames in the X2 zoom mode, and a 1024 sequence of $128^2$ frames in the X4 zoom mode provide approximately a 2-s, 8-s, or 32-s sequence of nonrepeated imagery, respectively, at 30 new frames/s. Naturally, program control allows for slower sequencing for slow motion effects.

The third control designed into refresh memory provides the freeze frame write facility, which allows data entry into memory at 80M bits/s for a burst of 1/30 s. This facility allows memory to be used as a video frame grabber (ie, capturing a single frame of video), but more importantly, it allows a feedback path into refresh memory from processed results implemented in the pipeline processor or in the convolution and image combination circuits. This feedback path permits interactive full-frame array processing on the imagery. In addition, the progression of the algorithm is visually available.

## Pipeline Processing

Pipeline processing functions are hardwired data entry tables, connected to each possible image and graphics plane in refresh memory (Fig 4). For a 64-image system (ie, 4096 x 4096 pixels), a total of 64 tables, each of which is an 8-bit by 8-bit (256-level by 256-level) function memory, can be loaded with arbitrary values under interactive operator control. These tables are loaded during horizontal and vertical retrace periods, thereby guaranteeing no visual breakup of the displayed imagery. Typical uses of these tables include gamma correction to compensate for sensor nonlinearities, contrast enhancement for sharper image definition (Fig 5), and log curves for transmission/density conversion.

Internal to the selector switch are logic circuits that allow graphics bit planes to control which image number is passed. This logic enables the definition of a region, or regions, of an image using the graphics as a mask, accurate to the single-pixel position. This mask or graphics plane then becomes the control signal, determining which image/function memory combination is allowed to be displayed. By wiring one image plane to two different function memories and

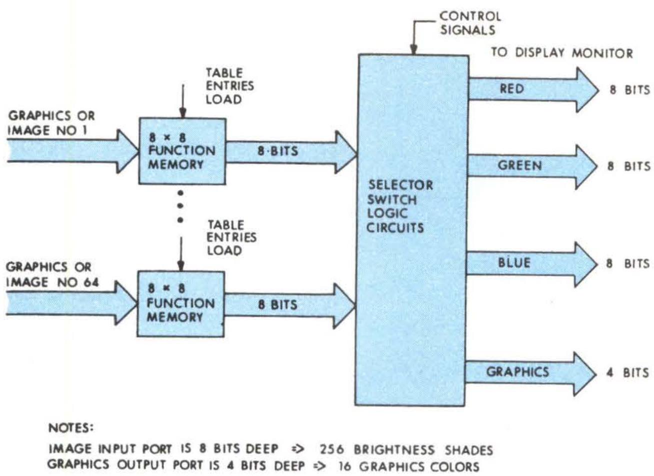
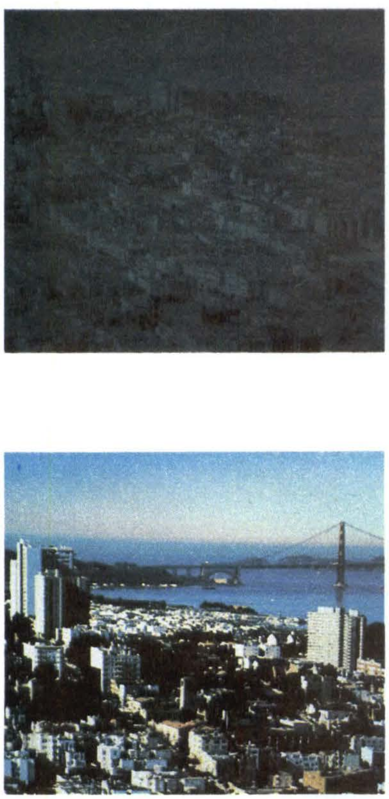



Fig 4 Pipeline processing functions. Multi-image pipeline processing consists of hard-wired tables available for loading during horizontal and vertical blanking intervals. Tables are addressed and read out at 10M times/s. Displayed image is any combination of 64 input images



(a)

(b)

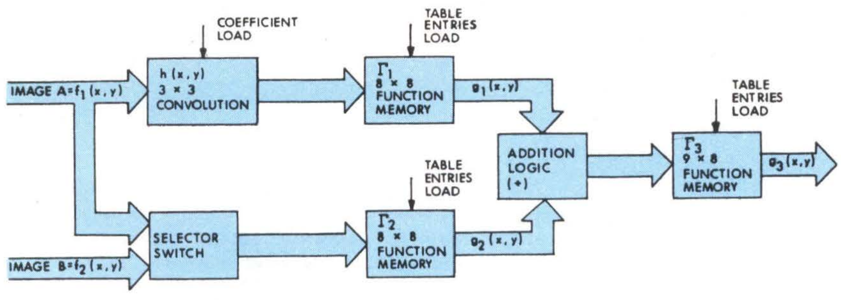
Fig 5 Contrast image enhancement. Function memories in pipeline processors are used to increase contrast in both monochrome or color imagery. Displays are taken directly from monitor; (a) shows original, and (b) is zoomed and contrast stretched in upper left quadrant

loading them differently, local brightness variations are achieved in the displayed image with spatial accuracies to the single-pixel position.

Pipeline processing can define a color image out of any three monochrome image planes. Selector switch control logic selects any 3 of 64 possible images to be defined as any combination of red, green, and blue channels for a final color display. Thus, monochrome to color dynamic memory allocation is done simply at the parallel pipeline selector switch. Because all image planes pass through function memories, a 24-bit color correction control is implemented by the respective three 8 x 8 function memory tables.

## Convolution and Image Combination

Because all image processing must be implemented at digital TV rates, realtime arithmetic operations must be computationally efficient. That is, vertical frequency is 60 Hz, and 16,770 Hz for horizontal frequency when the raster is driven at 559 lines/frame to make 512 lines viewable—not 480 viewable lines as in 525-line systems. For spatial filtering, small convolution kernels are fairly efficient, and with iterative feedback, the effective domain of the kernel enlarges. Based upon this design approach, convolution and image combination circuits have been organized for maximum throughput speeds (Fig 6). Table lookup techniques are used wherever possible, and arbitrary entries in the tables are operator loadable. The listing of "Typical Entries in Kernel and Function Memory Lookup Tables" is necessary for implementing various arithmetic expressions. Note from Fig 6 that powerful functions




NOTES:

3 × 3 CONVOLUTION ± 8-BIT COEFFICIENTS × 9 MULTIPLIES AND ADDS/PIXEL ⇨ 70M OPERATIONS/S

$g_1(x,y) = \Gamma_1\{f_1(x,y) \bullet h(x,y)\}$

$g_2(x,y) = \Gamma_2\{f_1(x,y) \text{ or } f_2(x,y)\}$

$g_3(x,y) = \Gamma_3\{g_1(x,y) + g_2(x,y)\}$

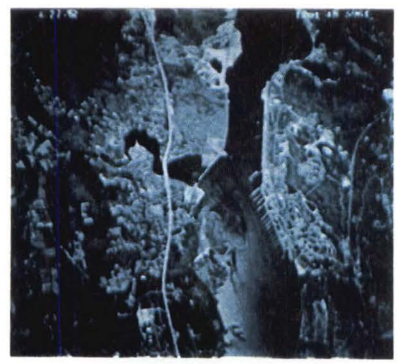
$\bullet$ = CONVOLUTION

Fig 6 Convolution/image combination circuits for maximum throughput. Processing is accomplished at 10M-pixel/s rates. Convolution output is fed to 8-bit x 8-bit (256-level x 256-level) function memory (Γ). Two other function memories are available for further image combinations. By appropriate table loading, very large number of image arithmetic operations are possible (see "Typical Entries in Kernel and Function Memory Lookup Tables"). Base arithmetic expression for this operation is listed

are implemented by this hardware configuration. Nonlinear entries in the function memory tables allow spatially adaptive filtering, examples of which are low pass filtering in the dark regions and high pass filtering in the bright regions. Unsharp masking and other edge enhancements are also available with this architecture. Because all three tables and nine convolution coefficients are changeable 30 times a second, highly interactive filtering and image combinations are possible. For a 512 x 512-pixel image, a total of approximately 70M operations/s are implemented in the convolution processors; a typical operation is a multiply and addition of an 8-bit pixel with a 9-bit designer defined coefficient to result in a spatially filtered image.

A difficult technical aspect to illustrate, but undoubtedly the most relevant to interactive image processing, is the highly responsive nature of realtime convolution kernel modification. Interactive exploitation technology has adapted the power of realtime updatable function memories. These are loadable and changeable at up to 30 times a second, a rate that greatly exceeds the bandwidth of human photointerpretation capabilities. Therefore, by implementing a particular update rate, effective and customized interactive scenarios can be developed. A similar capability is available for spatial filter kernel updates; these updates are software reloadable during the vertical flyback period of display. Thus, no interference is experienced with the display process. Because convolution is implemented on a full frame, it is possible to develop spatially interactive scenarios, which cycle through an unprecedented number of filtering operations, all in real time, with instantaneous visual feedback

(a)



(b)

Fig 7 Spatial filtering. Spatial convolution illustrates two extremes of edge sharpening. Simple 3 x 3 kernel window is passed over every pixel in display, modifying its value according to surrounding pixel coefficient weighting. Views are original (a) and after edge enhancement (b)

**Typical Entries in Kernel and Function Memory Lookup Tables**

| Process | Coefficient Matrix | Function Memory ($\Gamma_1$) | Function Memory ($\Gamma_2$) | Function Memory ($\Gamma_3$) |
|---|---|---|---|---|
| Convolve $f_1(x,y)$ Arbitrary | $\begin{bmatrix} a & b & c \\ d & e & f \\ g & h & i \end{bmatrix}$ | Linear | Linear | Linear |
| Convolve $f_1(x,y)$ Parametric | $\begin{bmatrix} a & b & a \\ b & 1 & b \\ a & b & a \end{bmatrix}$ | Linear | Linear | Linear |
| | $a = b = 1$ (Low Pass) | Linear | Linear | Linear |
| | $a = \frac{1}{4} b = \frac{1}{2}$ (Gaussian Low Pass) | Linear | Linear | Linear |
| | $a = b = 0$ (No Filtering) | Linear | Linear | Linear |
| | $a = 0, b = -1$ (Laplace Transform) | Linear | Linear | Linear |
| | $a = \frac{1}{4}, b = -\frac{1}{2}$ (Laplace Transform) | Linear | Linear | Linear |
| | $a = b = -\frac{1}{8}$ (Laplace Transform) | Linear | Linear | Linear |
| $f_1(x,y) + f_2(x,y)$ | $\begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix}$ | Linear | Linear | Linear |
| $f_1(x,y) - f_2(x,y)$ | $\begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix}$ | Linear | Linear Negative | Linear |
| $f_1(x,y) \times f_2(x,y)$ | $\begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix}$ | Logarithm | Logarithm | Antilogarithm |
| $f_1(x,y) \,/\, f_2(x,y)$ | $\begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix}$ | Logarithm | Logarithm Negative | Antilogarithm |

for each filter result. Such spatially interactive scenarios are difficult to illustrate with still photographs. However, Fig 7 presents the results of two extremes of spatial filtering. The first represents no spatial enhancement while the second represents sharp edge emphasis. Varying degrees of "sharpening" are available via kernel coefficient modification at a definable update rate.

## Feedback and Iterative Processing

In Fig 8, a complete multiterminal interactive system design is controlled by a small system computer (the size of a Digital Equipment Corp LSI-11™ minicomputer), through which firmware commands are initiated to allow interaction via keyboard, trackball, or data tablet entry. However, no realtime image data pass through the system computer, as its bandwidth of less than 1M bytes/s will not support digital TV rates, which require 10M bytes/s.

Probably the most significant design aspect of the total system configuration, in a mathematical sense, is the feedback path that allows the actual displayed imagery to be read back into memory. This feedback permits iterative processing and updating with pipeline processor tables, convolution kernels, and image combination circuits. True image parallel array processing involves a cycle time of 1/30 of a second, and the array is 512 x 512 pixels x 8 bits deep. This configuration permits recursive and iterative filtering on an image to image basis. The system can ping-pong (ie, alternate buffer frames) through refresh memory, using recursive filters (512 x 512 in pixel size), N deep, with an N + 1 image memory. Thus, for a 4-image system (1024 x 1024), a 3-lag memory filter would be possible.

Recursive filtering allows time sequential processing of large amounts of imagery, thereby saving hardware expense. Typical recursive filters trade off hardware complexity for longer processing times. In addition, the theory of recursive filtering has been well established to be a viable alternative to large number crunching noniterative solutions, as well as lending themselves to adaptive and data dependent processing.

While recursive algorithms can illustrate rather complex processing power, a simple application using feedback would be to zoom at a magnification factor of 16 times. This feedback could be accomplished in 2/30 s with X4 magnification each time, or in 3/30 s with X4 magnification once and X2 twice, or in 4/30 s with X2 magnification, four times. Another common use of the feedback path is the development of an effectively larger convolution kernel than a simple 3 x 3 kernel.

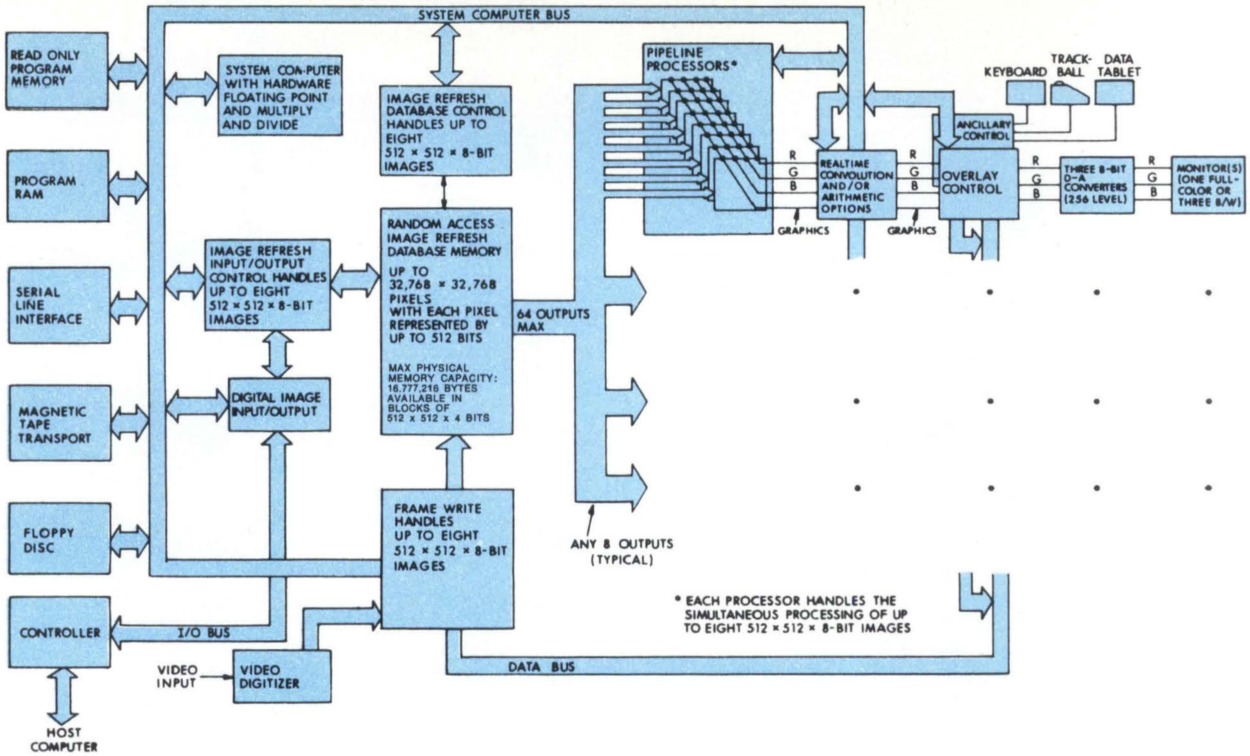



Fig 8 Block diagram of 10M-pixel/s interactive system. All processing paths operate at up to 240M bits/s for realtime display of various processes

Thus, in five iterations, reconvolving results in a kernel size of 11 x 11, since each iteration causes the data to be effected by two more pixels on a side. While this "cascaded convolution" does not provide the same total number of degrees of freedom as a single-pass full kernel implementation (45 versus 121—9° of freedom in five passes versus 121° of freedom from an 11 x 11 matrix in one pass), it is interesting to speculate on the limitations (if any) of this iterative approach.

Naturally, there is a system tradeoff as to convolving kernel size and the decision to go to a conventional array processor for more complex operations. However, a 3 x 3 convolver, or its generic form, is still a powerful tool; noise suppression, unsharp masking, and nonlinear edge weighting are only a few of the forceful capabilities available. More importantly, because the filters can be parameterized for interactive updating (at a rate of an entire new filter), the effects of numerous filters can be rapidly evaluated.

## Overlay Control

Overlay control presents pictorial results of interactive requests. This control has three important capabilities: cursor/target definition, pseudocolor implementation, and final display priority commands (Fig 9). Because of a 16 x 16 programmable cursor or target, firmware commands can select target coefficients. Each of the 256 (16 x 16) pixels defining the target has the ability of producing eight colors, if desired. Therefore, crosses, circles, and other shapes and colors defineable in a 16 x 16 array can be developed. In addition, target position is evolved on an interactive basis for operator coordination, and can be updated at a rate of 30 times/s.

From Fig 9, a final set of 8 x 8-bit function memories are available for table lookup, prior to passing image data to the display. These function memories can be used for final monitor gamma correction or they can be used to generate 24 bits of pseudocolor (the mapping of gray shades to color for visual effects). In this mode of operation, pipeline processing causes one image to be placed on all three red, green, and blue digital channels. Then, the red, green, and blue function memories can be loaded with 256 different values, each to define any of $2^{24}$ possible color outputs. This capability allows for subtle detail, made viewable by proper loading of these tables, again with updated coefficients.

Overlay control develops the proper priority selection for ultimate display on a per pixel basis. Thus, imagery, graphics, targets, and annotation must be sorted out for presentation on the monitor. This priority selection must take place within a single pixel display time, and must be switchable interactively, 30

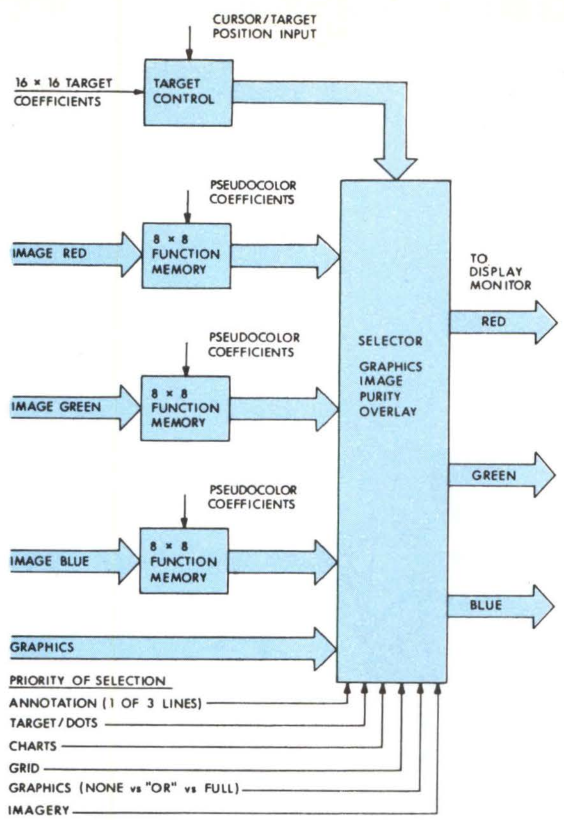



Fig 9 Overlay control. This control is used for final output to display monitor. Priority switching adds graphics, target, or pseudo-color to emphasize and locate detail on image

times/s within the retrace and flyback times of the digital TV synchronization system to avoid flicker or other noticeable image distortion; Fig 9 lists the priority of selection in decreasing order.

## Firmware Control

Probably the second most significant breakthrough in digital image processing system design (after high speed RAMs) lies in the turnkey operation provided by firmware (read only memory) operating systems. Typically, controls of the architecture and data paths for the flow of such imagery are under control of the system minicomputer, in which speed of transfer and control is the underlying design objective. Responsive interactivity is the bottom line, and firmware implementation at the frontend exploitation station seems to be the current solution.

The minicomputer (Fig 8) with its hardware arithmetic functions is an integral aspect of the overall system with all display processing hardware instructions stacked and processed via direct memory access, thereby eliminating the normally encountered time-consuming operation of instruction I/O. The typical operating system program accommodates more than 150 high level language graphics and image manipulation instructions burned into firmware. Instruction programming, linking (macros), and execution in software are all keyboard implementable. Firmware memory management by the minicomputer facilitates the handling of diverse applications, such as high resolution color imagery, multiple station monochrome reconnaissance imagery, and multilevel raster color graphics.

## Conclusions

Present capabilities in digital image processing system architectures and hardware techniques as described here should not be equated with raster graphics terminals or simple slave refresh peripheral stations being driven by host machines. Rather, these system architectures represent unique designs for specific high resolution data sets describing 2-dimensional data arrays for operator interpretation.

Future designs will include digital rotation and spatial warping interactively, as well as 16-bit deep image arrays with interactive 16 x 8-bit tables (function memories) for realtime interpretation of radar and large dynamic range tomography images. In the area of true digital color processing, small area color correction and prepress color compensation for printing are expected soon. Such color processing will be accomplished by using 24-bit by 24-bit color computer tables to compensate for any final output color hardcopy device (ie, ink, film, or paper). Digital image processing is beginning to emerge as a powerful tool for interactive human manipulation of all forms of 2-variable data displays.

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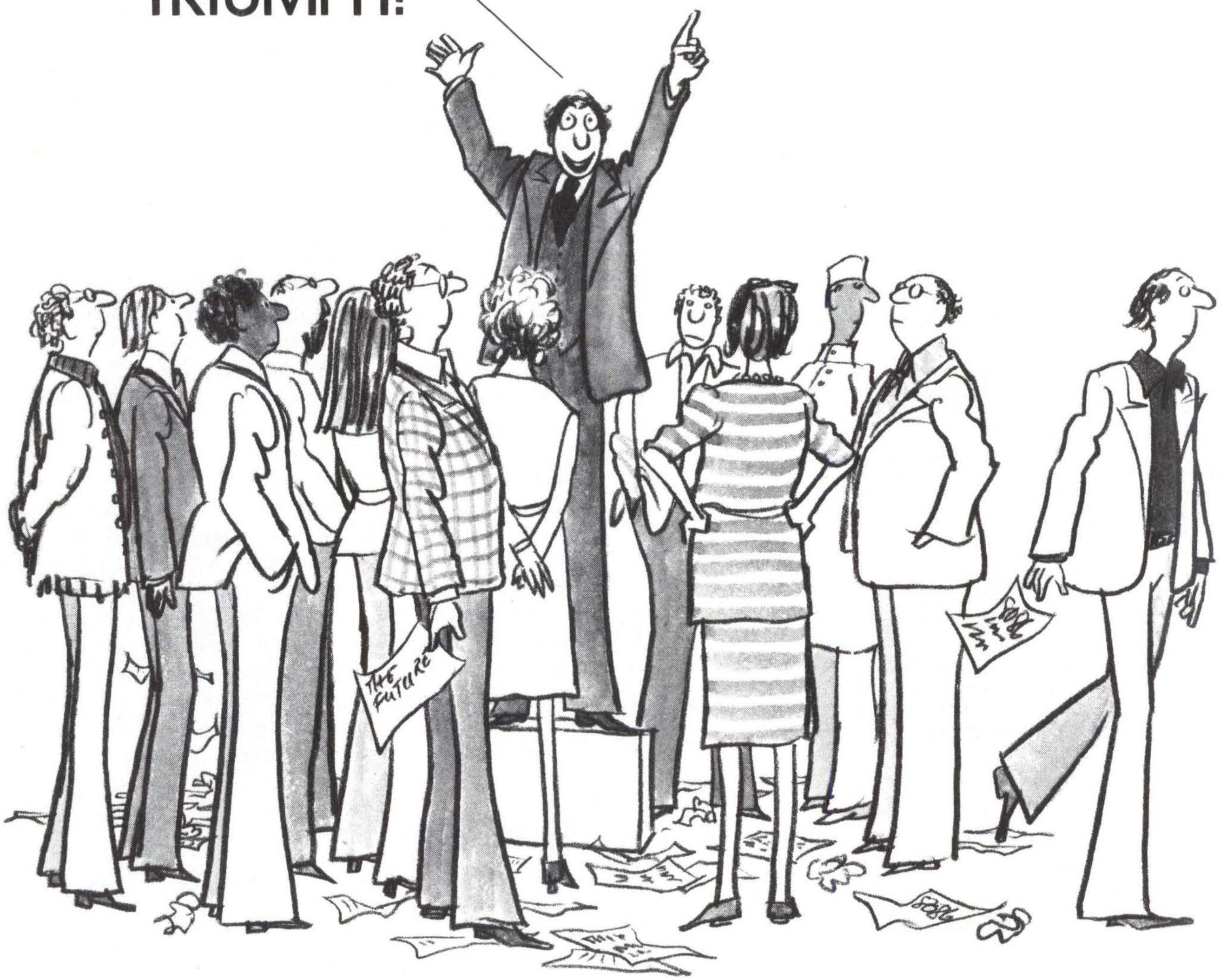


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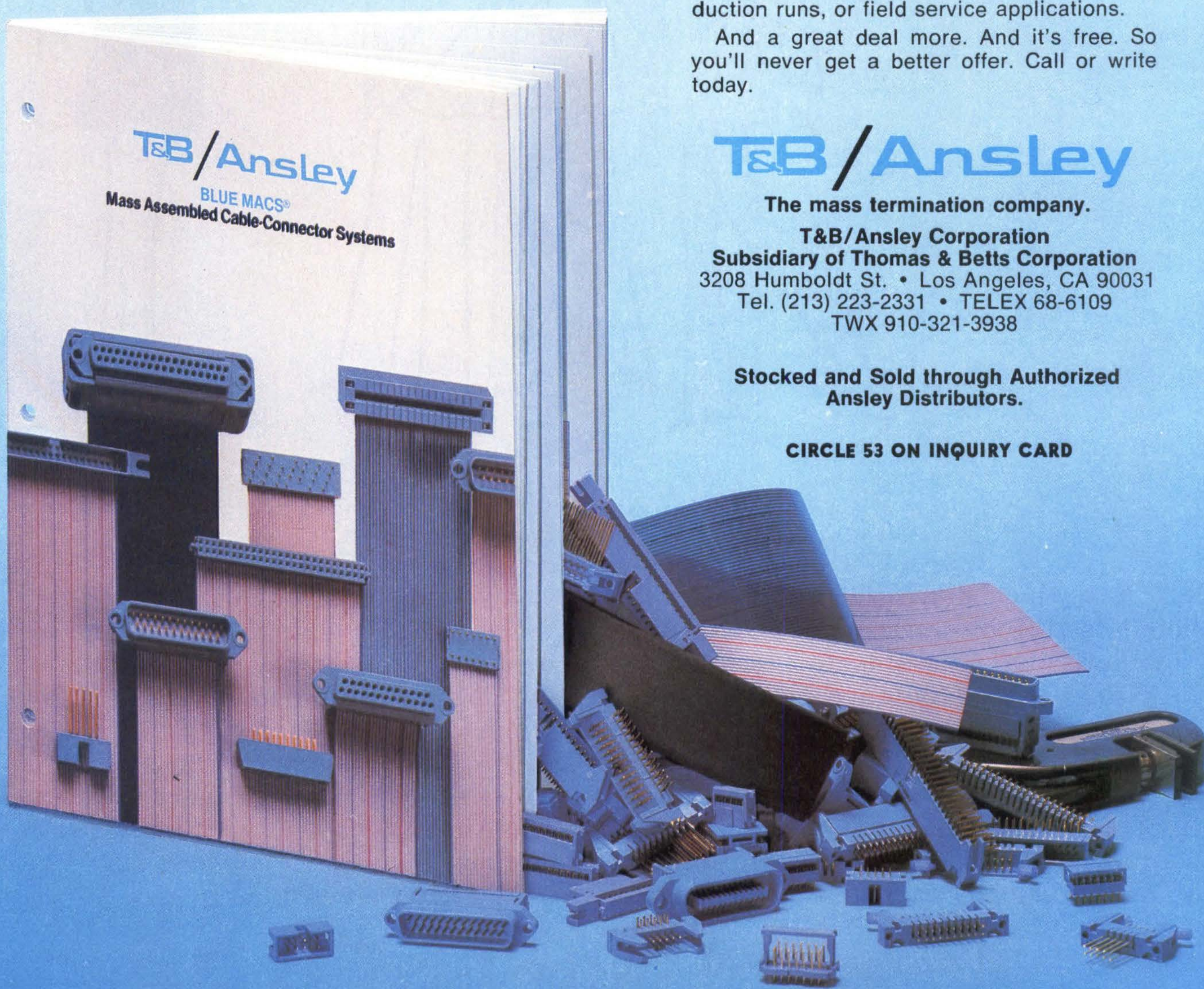


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# UNIFIED APPROACH TO DESIGNING HARDWARE BASED ON IEEE STD 488

Conventional techniques for hardware realization of the state diagrams of IEEE Std 488 are restricted by the number of required inputs. A modification of the level mode technique implements controller hardware for a standard state diagram requiring up to 12 input variables

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Restraints on designs based on IEEE Std 488 result from the complexity of the logic protocol and the unavailability of low cost LSI chips that incorporate the required digital bus interface functions. This first of two related articles—written while IEEE Std 488-1975* was in effect—demonstrates the TTL design approach needed to implement the specified controller functions. Next month, a design approach that takes advantage of recently available LSI chips dedicated to the standard functions and protocol offers a cost-effective, highly flexible solution to meeting the listener/talker/controller requirements of the standard.—**Ed.**

**A** unified design approach for computer interfacing in instrumentation and control systems is provided by IEEE Std 488,[1] which adopts the well-known state diagram to describe device and interface functional specifications. A device connected to an interface system based on the standard performs at least one of three functions: listener, talker, or controller.** According to this classification, a set of interface specifications is defined, as well as state diagrams, for each of the three functions.[2,3,4]

State diagrams are advantageous in that they offer a complete and unambiguous method to specify the particular interface required. These diagrams are usually synthesized by assuming a level mode operation.[1,5] Since the minimization procedures used in the hardware design of such circuits are based on four or less inputs and 16 or less states, a modification of this approach is dictated when more than four inputs are required. The modified method derives a set of transition tables for a state diagram with up to 12 inputs. Then, conventional minimization procedures are applied to these transition tables to implement the necessary hardware design. This method has been field-proven by implementing the resulting hardware configurations for many IEEE Std 488 interface functions. Because the controller is the most complicated specified function, its design is described in detail to demonstrate the evolved synthesis process.

*IEEE Std 488-1975 has been superseded by IEEE Std 488-1978, *IEEE Standard Digital Interface for Programmable Instrumentation*, The Institute of Electrical and Electronics Engineers, Inc, 345 E 47th St, New York, NY 10017, Nov 30, 1978.

**The term "controller" refers strictly to the management (control) of the interface system and does not imply the broad capabilities typically associated with the word in a data processing context.[1]

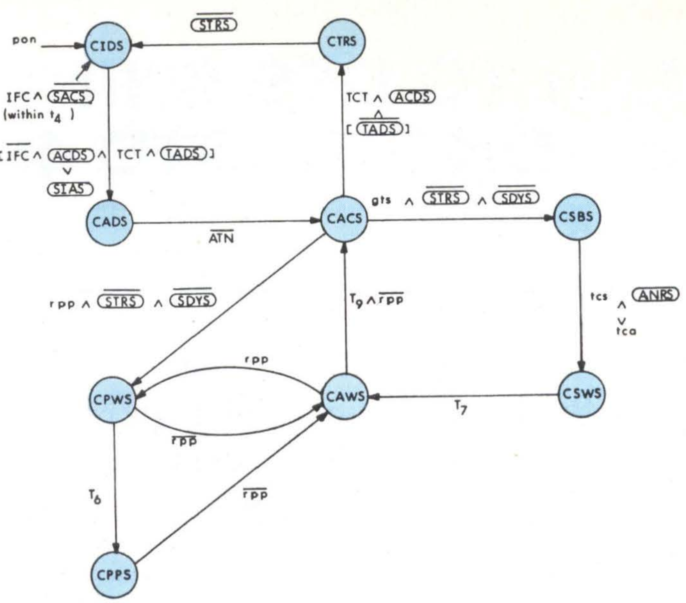


Fig 1 State diagram of controller interface function. Diagram illustrates permissible transitions between states and required conditions to effect transitions. Each state is defined by circled 4-letter mnemonic, beginning with C (controller) and ending with S (state). Arrows connect various states and indicate path direction. Controller function allows device to send addresses, universal commands, and addressed commands to other devices on same interface bus (Reproduced from *IEEE Standard Digital Interface for Programmable Instrumentation,* IEEE Std 488-1978 by permission of the Institute of Electrical and Electronics Engineers, Inc)

## Synthesis Approach

The conventional technique used to design minimal level mode circuits[5] normally deals with up to four input variables. Problems arise in realizing standard state diagrams with this technique when a larger number of inputs are included. For example, one standard state diagram for the controller interface function contains 12 different inputs.[1] Obviously, it would be inconvenient to form a single transition table with $2^{12}$ columns that covers the entire state diagram. To overcome this difficulty, the technique is modified to provide an individual table structured for each state.

An inherent feature of standard state diagrams is that, although the total number of inputs for a state diagram is large, each specific state is concerned with only a few of these inputs. Occurring on a branch between states, these inputs cause a transition from one state to another. Therefore, a reasonable number of input combinations will be required if a separate transition table is developed for each state that consists of only one row of next-state values. The standard state diagram of the basic controller function (Fig 1) is used to illustrate the different hardware design steps. "Controller Mnemonics" lists and defines the associated controller function mnemonics. Formation of the transition tables and derivation of interface circuits are explained, and necessary synthesis process definitions are given.

### Process Definition I

A set of four state variables ($y_1$, $y_2$, $y_3$, and $y_4$) are required to define a controller state diagram with nine states, as depicted by the circled CXXS mnemonics in Fig 1. This state diagram is repeated in Fig 2 with

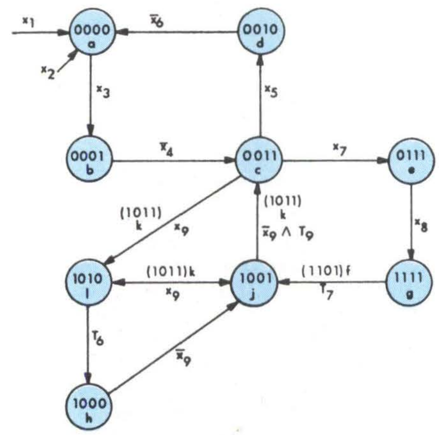


Fig 2 State diagram of basic controller function with input and state variable assignments. Diagram contains 12 input variables ($x_1$ though $x_9$ and $T_6$, $T_7$, and $T_9$). Transition from one circled state to another occurs whenever certain expression (defined by $x_n$) is true, or after certain time limit ($T_n$) is exceeded. State binary assignments are purposely selected to overcome racing problems with minimum cycling. Unstable states (f and k) entered during cycling are shown on branches between states

**Controller Mnemonics**

| Local Message Received From Device Functions | |
|---|---|
| gts | Go To Standby |
| pon | Power On |
| rpp | Request Parallel Poll |
| tca | Take Control Asynchronously |
| tcs | Take Control Synchronously |

| Remote Message Received Via Interface Bus | |
|---|---|
| ATN | Attention |
| IFC | Interface Clear |
| TCT | Take Control |

| Linkage From Another State Diagram | |
|---|---|
| ACDS | Accept Data State [Acceptor Handshake (AH) Function] |
| ANRS | Acceptor Note Ready State [Acceptor Handshake (AH) Function] |
| SDYS | Source Delay State [Source Handshake (SH) Function] |
| STRS | Source Transfer State [Source Handshake (SH) Function] |
| TADS | Talker Addressed State [Talker (T) Function] |

| Interface State | |
|---|---|
| CACS | Controller Active State |
| CADS | Controller Addressed State |
| CAWS | Controller Active Wait State |
| CIDS | Controller Idle State |
| CPPS | Controller Parallel Poll State |
| CPWS | Controller Parallel Poll Wait State |
| CSBS | Controller Standby State |
| CSWS | Controller Synchronous Wait State |
| CTRS | Controller Transfer State |
| SACS | System Control Active State |
| SIAS | System Control Interface Clear Active State |
| $t_4$ | Response to Interface Clear (IFC) or Remote Enable (REN) false, $<100\ \mu s$ |
| $T_6$ | Parallel Poll Execution Time, $\geq 2\ \mu s$ |
| $T_7$ | Controller Delay to Allow Current Talker to see Attention Message, $\geq 500\ \mu s$ |
| $T_9$ | Delay for End or Identify (EOI) Signal Line to Indicate Valid State, $\geq 1.5\ \mu s$ or 600 ns for 3-state drivers |

input expressions replaced by x and state mnemonics replaced by their assigned binary state variables. State assignments have been chosen to overcome racing problems with minimum cycling.

Racing problems arise when more than one state variable changes during a transfer from one state to another, eg, in a transfer from 0000 to 0011. Binary values have been assigned to states a through h so that only one state variable changes while transferring from one state to another. Wherever it was impossible to allow only one state variable to change, such as for states that have several branches (eg, states c and j), racing problems have been overcome by allowing an intermediate transfer through one or more unstable states. For instance, in Fig 2 an intermediate path is made through k (1011) while cycling from j (1001) to l (1010) to accomplish only one state variable change during each transfer. Cycling requires additional hardware and cost; thus, the need for minimization.

Whenever the circuit must cycle through an unstable state in transferring from one stable state to another, the unstable state is shown on the transition branch in the state diagram.

## Process Definition 2

A set of 11 states (a, b, c, d, e, f, g, h, j, k, and l) include nine stable states plus two unstable states (f and k). Each state i is active whenever a certain combination of state variables, $S_i$ ($y_1$, $y_2$, $y_3$, and $y_4$) is true. For example, in Fig 2, state a—corresponding to stable state 0000 (CIDS)—is active when $S_a = \overline{y_1} \cdot \overline{y_2} \cdot \overline{y_3} \cdot \overline{y_4}$ is true; similarly, state k—corresponding to unstable state 1011—is active when $S_k = y_1 \cdot \overline{y_2} \cdot y_3 \cdot y_4$ is true.

## Process Definition 3

For each state i of the 11 defined states, there is an input variable, $X_i$, which contains all the inputs that cause state transitions. The relationships between the 11 states and the 12 inputs ($x_1$ through $x_9$ and $T_6$, $T_7$, and $T_9$) of the controller state diagram under discussion are as follows:

$X_a = (x_3)$

$X_b = (x_1, x_2, x_4)$

$X_c = (x_1, x_2, x_5, x_7, x_9)$

$X_d = (x_1, x_2, x_6)$

$X_e = (x_1, x_2, x_8)$

$X_f = (x_1, x_2, T_7)$

$X_g = (x_1, x_2, T_7)$

$X_h = (x_1, x_2, x_9)$

$X_j = (x_1, x_2, x_9, T_9)$

$X_k = (x_1, x_2, x_9, T_9)$

$X_l = (x_1, x_2, T_6)$

The transition table for each state i includes combinations of inputs in $X_i$ only. For example, the transition table for state c—0011 (CACS)—is shown in Fig 2, where $X_c$ equals $x_1$, $x_2$, $x_5$, $x_7$, and $x_9$. Two inputs ($x_1$ and $x_2$) are common to all states except state a (0000). Whenever either of these two inputs is true, all state variables return to zero.[1] Therefore, for any

| $x_5\ x_7\ x_9$ | 000 | 001 | 011 | 010 | 100 | 101 | 111 | 110 |
|---|---|---|---|---|---|---|---|---|
| NEXT STATE $Y_{1c}\ Y_{2c}\ Y_{3c}\ Y_{4c}$ | 0011 | 1011 | 0111 | 0111 | 0010 | 0010 | 0010 | 0010 |

(a)

| $x_5$ \ $x_7\ x_9$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 |

$Y_{1c} = \bar{x}_5 \wedge \bar{x}_7 \wedge x_9$

$\wedge$ = AND

| $x_5$ \ $x_7\ x_9$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |

$Y_{2c} = \bar{x}_5 \wedge x_7$

$\vee$ = OR

| $x_5$ \ $x_7\ x_9$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

$Y_{3c} = 1$

| $x_5$ \ $x_7\ x_9$ | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |

$Y_{4c} = \bar{x}_5$

(b)

Fig 3 Transition table and Karnaugh maps for state c (0011). While total number of input variables to controller is 12, transition table (a) for state c contains only three ($x_5$, $x_7$, and $x_9$). Transition listing requires one row of next state values. There are four derived Karnaugh maps (b), one for each state variable ($Y_{1c}$, $Y_{2c}$, $Y_{3c}$, and $Y_{4c}$). Thus, minimization procedure is partitioned allowing large number of input variables to be handled effectively

state variable ($Y_n$) to be a 1, both $x_1$ and $x_2$ must be 0. Consequently, since $\overline{x_1} \bullet \overline{x_2}$ is common to all expressions for all $Y_n$ values, these two inputs are excluded from the synthesis procedure.

A Karnaugh map for each state variable can be derived from these transition tables. For example, four Karnaugh maps, one each for $Y_1$, $Y_2$, $Y_3$, and $Y_4$, have been formed from the transition table for state c [Fig 3(a)] and are shown in Fig 3(b). From each Karnaugh map, a minimum expression is derived for each $Y_n$ value; thus, for each state i of the controller state diagram, there is a set of such expressions where each equation is a sum of products expression of the input variables: $Y_{1i} = f_1\ (X_i)$; $Y_{2i} = f_2\ (X_i)$; $Y_{3i} = f_3\ (X_i)$; and $Y_{4i} = f_4\ (X_i)$.

The set of Ys for all states of the controller function is grouped in a present state/next state relationship diagram (Fig 4). The next state entry for row i and column j is $Y_{ji} = f_j\ (X_i)$. An entry of 1 means that the next value of the state variable is 1 if state i is active, independent of any input condition. Similarly, a 0 entry means that the next value of the state variable is always 0.

The complete expression for the next value for each Y is the logical summation* of all the active subexpressions for those Y values listed in one entire column of the present state/next state relationship diagram logically multiplied* by each associated

*In the expressions for $Y_n$, + indicates a logic OR function, and • signifies a logic AND function.

| STATE | PRESENT STATE | | | | NEXT STATE | | | |
|---|---|---|---|---|---|---|---|---|
| $(x_i)$ | $y_1$ | $y_2$ | $y_3$ | $y_4$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_4$ |
| a | 0 | 0 | 0 | 0 | 0 | 0 | 0 | $x_3$ |
| b | 0 | 0 | 0 | 1 | 0 | 0 | $\bar{x}_4$ | 1 |
| c | 0 | 0 | 1 | 1 | $\bar{x}_5 \cdot \bar{x}_7 \cdot x_9$ | $\bar{x}_5 \cdot x_7$ | 1 | $\bar{x}_5$ |
| d | 0 | 0 | 1 | 0 | 0 | 0 | $x_6$ | 0 |
| e | 0 | 1 | 1 | 1 | $x_8$ | 1 | 1 | 1 |
| f | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| g | 1 | 1 | 1 | 1 | 1 | 1 | $\bar{T}_7$ | 1 |
| h | 1 | 0 | 0 | 0 | 1 | 0 | 0 | $\bar{x}_9$ |
| j | 1 | 0 | 0 | 1 | 1 | 0 | $\bar{x}_9 + T_9$ | 1 |
| k | 1 | 0 | 1 | 1 | $x_9$ | 0 | 1 | $\bar{x}_9$ |
| l | 1 | 0 | 1 | 0 | 1 | 0 | $\bar{T}_6$ | 0 |

Fig 4 Present state/next state relationship diagram for controller interface function. Next state values of state variables ($y_1$, $Y_2$, $Y_3$, and $Y_4$) depend on input variable (x and T) values. Listing shows next values whenever column state is active (1)

present state row value. General forms of these expressions are

$$Y_1 = f_{1a}(X_a) \bullet S_a + f_{1b}(X_b) \bullet S_b + \ldots$$
$$Y_2 = f_{2a}(X_a) \bullet S_a + f_{2b}(X_b) \bullet S_b + \ldots$$
$$Y_3 = f_{3a}(X_a) \bullet S_a + f_{3b}(X_b) \bullet S_b + \ldots$$
$$Y_4 = f_{4a}(X_a) \bullet S_a + f_{4b}(X_b) \bullet S_b + \ldots$$

For the controller function, the above expressions have the specific form

$$\begin{aligned} Y_1 = {} & \overline{x_5} \bullet \overline{x_7} \bullet x_9 \bullet \overline{y_1} \bullet \overline{y_2} \bullet y_3 \bullet y_4 + x_8 \bullet \overline{y_1} \bullet y_2 \bullet y_3 \bullet y_4 \\ & + y_1 \bullet y_2 \bullet \overline{y_3} \bullet y_4 + y_1 \bullet y_2 \bullet y_3 \bullet y_4 \\ & + y_1 \bullet \overline{y_2} \bullet \overline{y_3} \bullet \overline{y_4} + y_1 \bullet \overline{y_2} \bullet \overline{y_3} \bullet \overline{y_4} \\ & + x_9 \bullet y_1 \bullet \overline{y_2} \bullet y_3 \bullet y_4 + y_1 \bullet \overline{y_2} \bullet y_3 \bullet \overline{y_4} \end{aligned}$$

$$\begin{aligned} Y_2 = {} & \overline{x_5} \bullet x_7 \bullet \overline{y_1} \bullet \overline{y_2} \bullet y_3 \bullet y_4 + \overline{y_1} \bullet y_2 \bullet y_3 \bullet y_4 \\ & + y_1 \bullet y_2 \bullet y_3 \bullet y_4 \end{aligned}$$

$$\begin{aligned} Y_3 = {} & \overline{x_4} \bullet \overline{y_1} \bullet \overline{y_2} \bullet \overline{y_3} \bullet y_4 + \overline{y_1} \bullet \overline{y_2} \bullet y_3 \bullet y_4 \\ & + x_6 \bullet \overline{y_1} \bullet \overline{y_2} \bullet y_3 \bullet \overline{y_4} + \overline{y_1} \bullet y_2 \bullet y_3 \bullet y_4 \\ & + \overline{T_7} \bullet y_1 \bullet y_2 \bullet y_3 \bullet y_4 + x_9 \bullet y_1 \bullet \overline{y_2} \bullet \overline{y_3} \bullet y_4 \\ & + T_9 \bullet y_1 \bullet \overline{y_2} \bullet \overline{y_3} \bullet y_4 + y_1 \bullet \overline{y_2} \bullet y_3 \bullet y_4 \\ & + \overline{T_6} \bullet y_1 \bullet \overline{y_2} \bullet y_3 \bullet y_4 \end{aligned}$$

$$\begin{aligned} Y_4 = {} & x_3 \bullet \overline{y_1} \bullet \overline{y_2} \bullet \overline{y_3} \bullet \overline{y_4} + \overline{y_1} \bullet \overline{y_2} \bullet \overline{y_3} \bullet y_4 \\ & + \overline{x_5} \bullet \overline{y_1} \bullet \overline{y_2} \bullet y_3 \bullet y_4 + \overline{y_1} \bullet y_2 \bullet y_3 \bullet y_4 \\ & + y_1 \bullet y_2 \bullet \overline{y_3} \bullet y_4 + y_1 \bullet y_2 \bullet y_3 \bullet y_4 \\ & + \overline{x_9} \bullet y_1 \bullet \overline{y_2} \bullet \overline{y_3} \bullet \overline{y_4} + y_1 \bullet \overline{y_2} \bullet \overline{y_3} \bullet y_4 \\ & + \overline{x_9} \bullet y_1 \bullet \overline{y_2} \bullet y_3 \bullet y_4 \end{aligned}$$

The Karnaugh map for $Y_2$ as derived from Fig 4 is shown in Fig 5. For combinations of state variables not found in the present state/next state relationship diagram, "don't cares" designated by an X are entered in the Karnaugh map. Don't care states are those that the controller function will never enter. The complete minimal expression for $Y_2$, including $x_1$ and $x_2$, is thus

$$Y_2 = \overline{x_1} \bullet \overline{x_2} \bullet (\overline{y_1} \bullet y_3 \bullet y_4 \bullet \overline{x_5} \bullet x_7 + y_2 \bullet y_3)$$

Expressions for the other three state variables, obtained in a similar manner, are as follows:

$$\begin{aligned} Y_1 = {} & \overline{x_1} \bullet \overline{x_2} \bullet (y_1 \bullet y_2 + x_8 \bullet y_2 + \overline{x_5} \bullet \overline{x_7} \bullet x_9 \bullet \overline{y_2} \bullet y_3 \bullet y_4 \\ & + x_9 \bullet y_1 + y_1 \bullet \overline{y_3} + y_1 \bullet \overline{y_4}) \end{aligned}$$

$$\begin{aligned} Y_3 = {} & \overline{x_1} \bullet \overline{x_2} \bullet (x_9 \bullet \overline{y_3} \bullet y_4 + T_9 \bullet \overline{y_3} \bullet y_4 + \overline{x_4} \bullet \overline{y_1} \bullet y_4 \\ & + \overline{T_6} \bullet y_1 \bullet y_3 \bullet \overline{y_4} + \overline{T_7} \bullet y_3 \bullet y_4 + x_6 \bullet \overline{y_1} \bullet y_3 \\ & + \overline{y_1} \bullet y_3 \bullet y_4 + \overline{y_2} \bullet y_3 \bullet y_4) \end{aligned}$$

$$\begin{aligned} Y_4 = {} & \overline{x_1} \bullet \overline{x_2} \bullet (y_2 + \overline{y_3} \bullet y_4 + x_3 \bullet \overline{y_1} \bullet \overline{y_3} + \overline{x_9} \bullet y_1 \bullet \overline{y_3} \\ & + \overline{x_5} \bullet \overline{y_1} \bullet y_4 + \overline{x_9} \bullet y_1 \bullet \overline{y_3}) \end{aligned}$$

A minimal circuit implementation of the controller hardware, designed according to the above method is shown in Fig 6. This circuit includes NAND gates and inverters in a total hardware design for extremely fast response time. To meet the time limits of IEEE Std 488, three time delays have been incorporated.

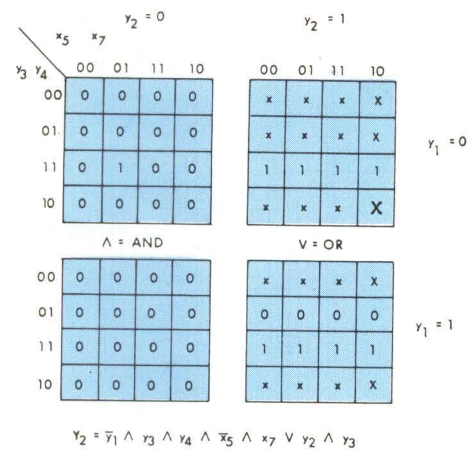


Fig 5 Karnaugh map for next state $Y_2$. Map is formed from $Y_2$ column of present state/next state relationships. Note that $Y_2$ depends on only 2 of 12 input variables ($\overline{x_5}$ and $x_7$)

## Summary

A design procedure is described to obtain a minimal controller hardware interface implementation derived from the standard state diagrams of IEEE Std 488. Primarily dealing with state diagrams having excessive inputs, the design procedure involves these steps:

(1) A binary state variable is assigned for each state. New unstable states may be introduced to overcome racing problems.

(2) A transition table is drawn for each state. This table includes only those input variables that affect the state.

(3) From each transition table, a set of Karnaugh maps is derived. In each set, one map is needed for each state variable ($Y_n$).

(4) Minimum expressions are formulated from the Karnaugh maps for the next values of the state variables ($Y_n$). Then, a present state/next state relationship diagram is developed.

(5) Final expressions for $Y_n$ are calculated from one column of the present state/next state diagram.

The procedure has been proven by implementing all standard interface functions in the Electrical and Electronic Engineering Laboratory of the National Research Centre, Cairo, Egypt.

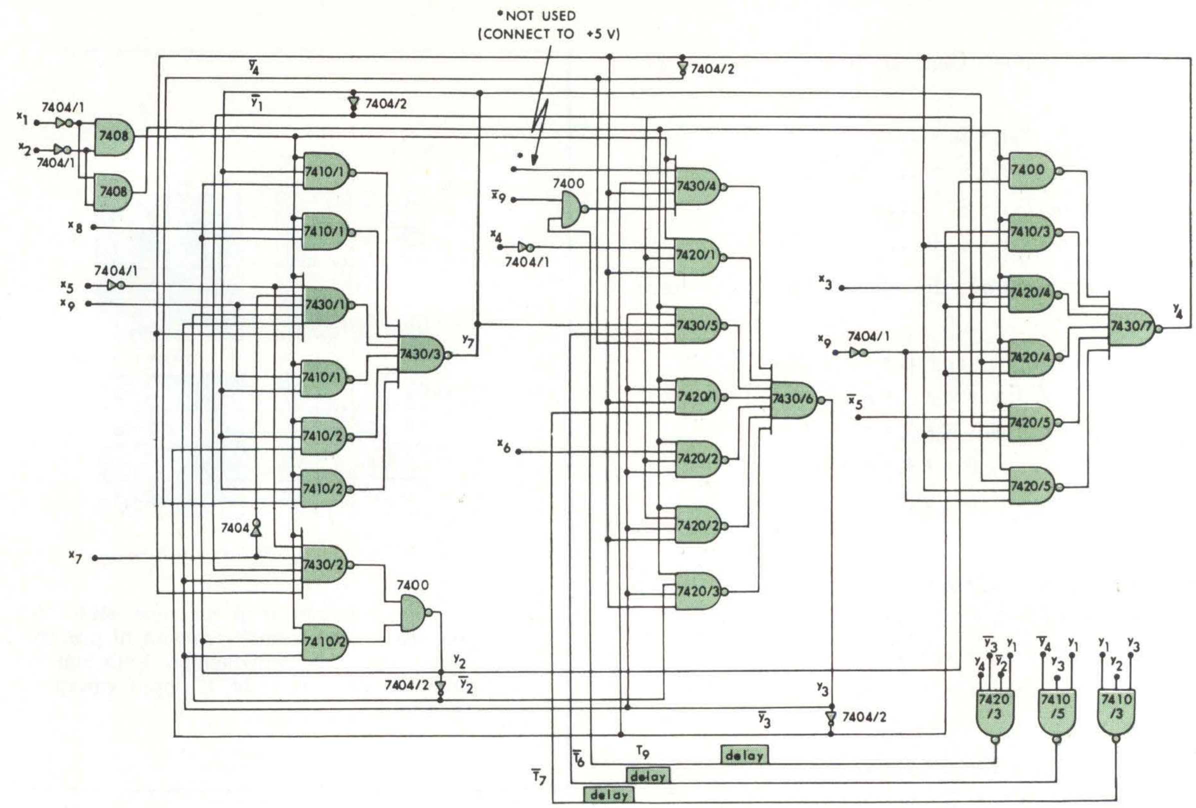


Fig 6 Basic controller interface circuit. Simple NAND gates implement controller function. Circuit contains four feedback variables ($y_1$, $y_2$, $y_3$, and $y_4$) and 12 inputs ($x_1$ through $x_9$ and $T_6$, $T_7$, and $T_9$). Three time delays are inserted for time limits $T_6$, $T_7$, and $T_9$


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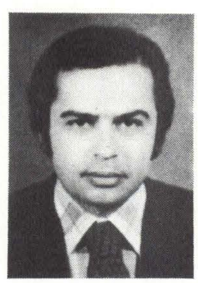


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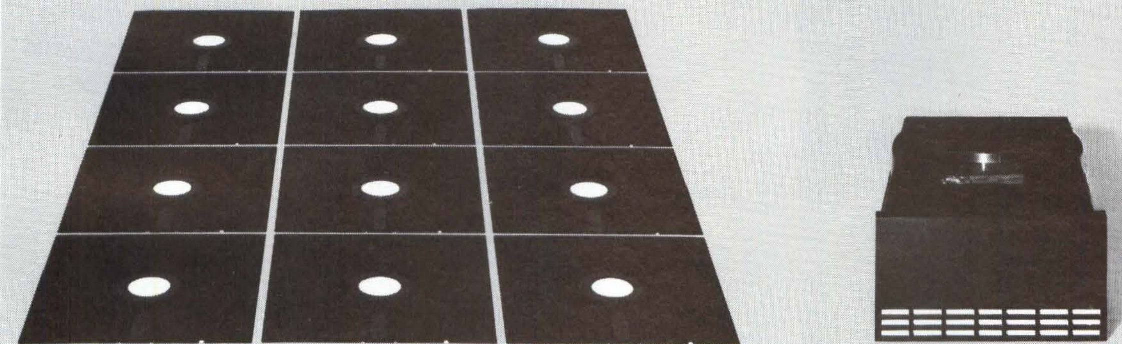

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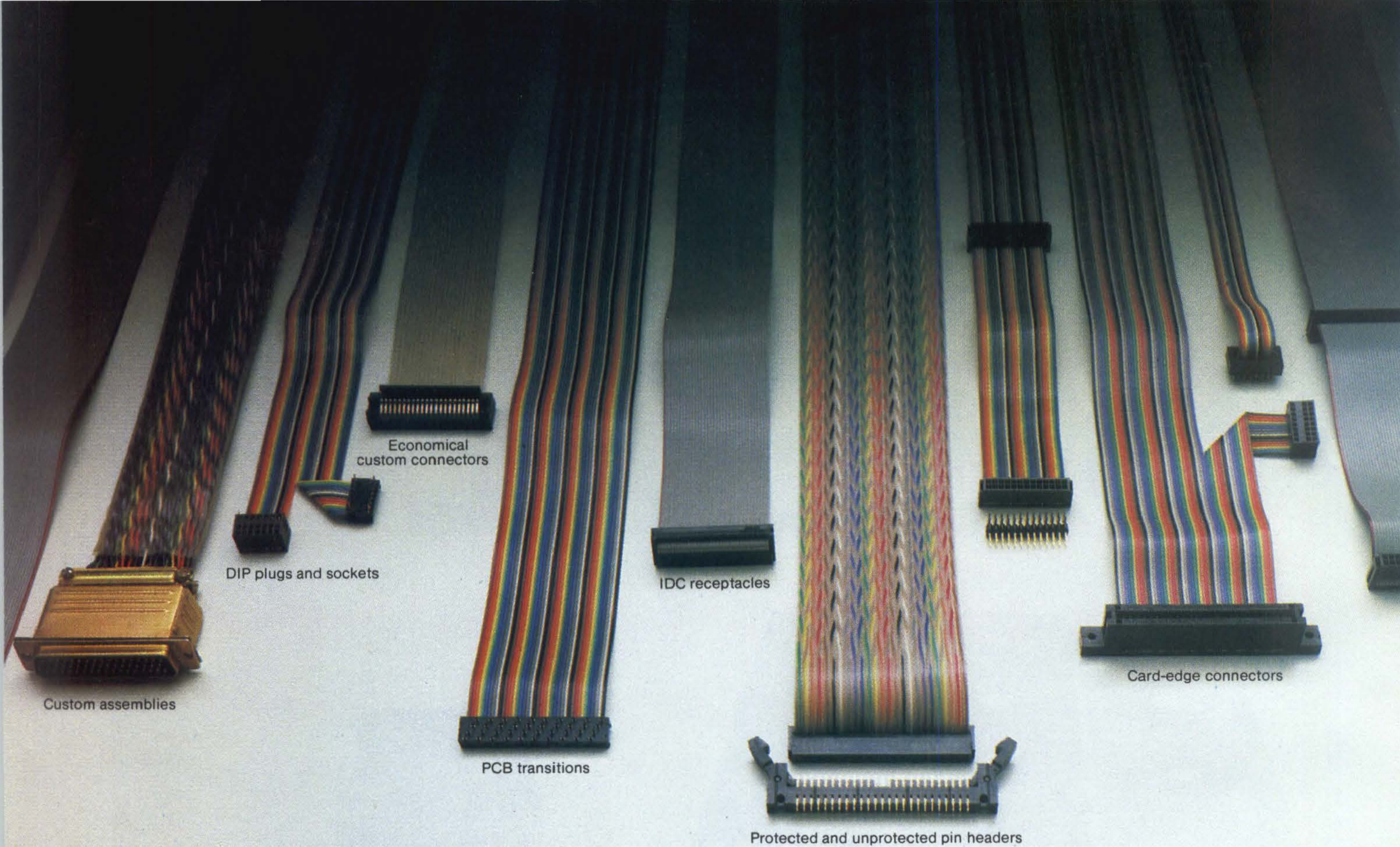


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# AUTOMATIC NETWORK SYNTHESIZER IDENTIFIES STANDARD LSI CELLS

LSI system design via pattern recognition in primitive Boolean functions is well within the range of the designer who is equipped with a synthesizer

**J. R. Logan** Hughes Aircraft Company, Fullerton, California

At the present time, design of a large scale integration chip of more than 2000 gates is a costly and tedious procedure. Any technique that can shorten the process while reducing project risks is highly cost effective and desirable. These requirements are met by implementation of an automatic network synthesizer, which is a set of software that accepts such design data as FORTRAN statements, decision tables, and logic equations, in several formats of Boolean functions.* While the synthesizer used in this objective appears to reduce truth table functions as do several well known schemes like Veitch maps, Quine reductions, and the like, it operates on the periodic structure of a Boolean function, rather than by any of the above methods. The highest periodicities of a Boolean function are its final logic, and are consequently called out deterministically.

## Methodology of the Synthesizer

Consider the truth table in Fig 1. It can be seen that function F1 is simply variable c, and function F2 is variable b; they exhibit the perfect periodicity of the

*J. R. Logan, "Congruent Partitioning and Network Synthesis," *Computer Design*, Dec 1974, pp 53-60

| INPUT VARIABLES | | | | OUTPUT FUNCTIONS | | |
|---|---|---|---|---|---|---|
| d | c | b | a | F1 | F2 | F3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Fig 1 Comparing periodic structure of truth table variables with several Boolean functions. High periodicities of output functions F1 and F2 show that they are simply input variables c and b respectively

basic variable. Note that function F3 is periodic too, although not to the extent of functions F1 and F2. Function F3 can be processed directly into the expression F3 = cb by reason of this periodicity. Note by the truth table that F3 is made by ANDing the two highly periodic variables c and b. Briefly, this is the method for the described synthesizer. The algorithm is fast enough to stand up to FORTRAN, in which it is currently coded. While this synthesizer can handle systems to a theoretical limit of 8000 variables, in actual experience it has not exceeded 300, about the limit of existing digital systems. Availability of the synthesizer means that complex logic circuit designs can be interactively worked and reworked at processor speeds, and thereby overcomes the prohibitive lengths of time incurred by unaided logic designers.

Moreover, the concept of a microfunction—compressed or standard cells—has emerged. These cells are logic subgroups that have been designed with expertise in the physics of large scale integration (LSI) techniques in order to derive simpler chips. For example, in bulk complementary metal-oxide semiconductor (CMOS) technology, the Exclusive-OR (XOR) gate can be mechanically produced so that it has a propagation delay of one gate level, even though it takes two gate levels to express the functional logic. Thus an XOR gate is a cell in a standard cell library.

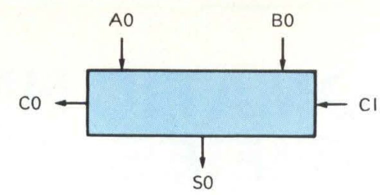
Many types of macros can be included in the typical cell library. Variations of a single category of cell, such as the simple NAND gate, can be laid out in various physical geometries, although identical in function from one example to the next. Geometries are controlled by such typical environmental factors as space restrictions, signal orientations, and loading effects. Function complexity varies from single gates to whole subfunctions, such as divide-by-N counters. Cells may also be nested; a complete arithmetic logic unit (ALU) may itself be a cell, made up of other cells. The process of system implementation can be a simple specification from the cell library. The design problem being addressed is one of identifying standard cell potentials for a complete logic set or library.

## Boolean Functions as Primary Tools

The network synthesizer works mainly with Boolean functions and their inherent patterns. Consider a simple adder, with inputs AO and BO, and a carry-in (CI), which generates a sum (SO) and a carry-out (CO) bit. The symbology and truth table for such a device are suggested in Fig 2. The horizontal line in the truth table divides the binary columns into two 4-bit row groups which can be designated in hexadecimal notation for space compaction. Columns CO and SO are called Boolean functions for this discussion, and can be restated without the counter or input side of the truth table, which is then implicit.

A hexadecimal method of representing the binary truth table of Fig 2 for CO and SO is

| CO | SO |
|---|---|
| 1 | 6 |
| 7 | 9 |




SYMBOLOGY OF ADDER

| INPUT | | | OUTPUT | |
|---|---|---|---|---|
| CI | BO | AO | CO | SO |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 |

TRUTH TABLE FOR ADDER

Fig 2 Definition of simple adder. Binary designation of how bits combine in manner that defines sum (SO) and carry-out (CO) outputs of binary adding device. Definitions show how truth table relates directly to buildable logic design

The format for this discussion is a left-to-right orientation for space economy, so the adder notation becomes

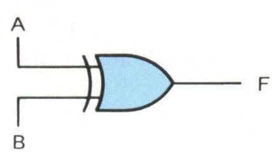
SO : 6 9

CO : 1 7

The adder circuit contains three input variable functions: AO, BO, and CI. Each time a variable is added, the associated function doubles in size, so that space compaction is mandatory. On the other hand, the more efficient notation of mathematical convention would tend to hide the all important binary patterns, details of which are the foundation of this discussion.

If the network synthesizer is given functions 69 and 17 for processing, logic equations would be produced to obtain the schematic of Fig 3. Designers skilled in pattern recognition schemes in Boolean functions try to decompose complex functions into simpler ones along the lines of a connective other than AND or OR gates. Because the XOR gate can be physically reduced into components which are of 1-gate time in signal propagation delay, designers might try to decompose 69 into XOR segments for a 2-variable function: A and B.

An XOR ($\oplus$) expression would be A′B + AB′. With bit patterns 01 and 10, the following truth table is obtained:




$$\equiv \begin{array}{cc} B & A \\ 0 & 0 \\ 0 & 1 \\ 1 & 0 \\ 1 & 1 \end{array} \oplus \; = \begin{array}{c} F \\ 0 \\ 1 \\ 1 \\ 0 \end{array} = 6_{16}$$

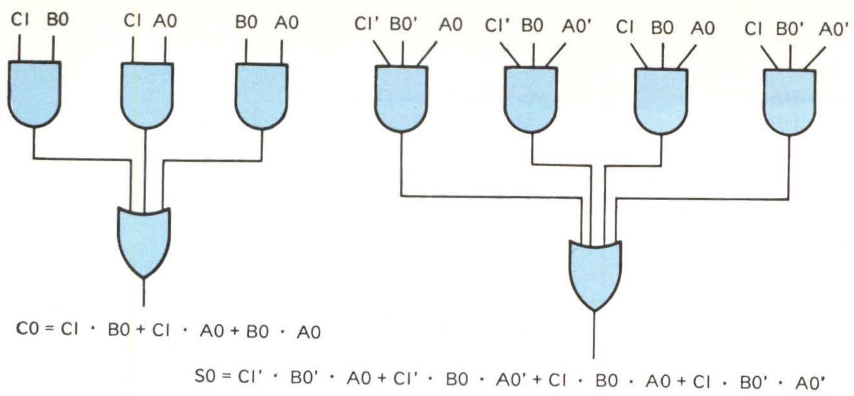



Fig 3 Logic schematic and Boolean functions of simple adder. Adder is implemented with 2-level gating logic, first or input level being made of AND gates and lower level of OR gates

Using the XOR relationship, the 3-variable function 69 of Fig 2 decomposes into 66 and OF as follows:

$$6\left\{\begin{matrix}0\\1\\1\\0\end{matrix}\right. = 6\left\{\begin{matrix}0\\1\\1\\0\end{matrix} \quad \oplus \quad \begin{matrix}0\\0\\0\\0\end{matrix}\right\}0$$

$$9\left\{\begin{matrix}1\\0\\0\\1\end{matrix}\right. = 6\left\{\begin{matrix}0\\1\\1\\0\end{matrix} \quad \oplus \quad \begin{matrix}1\\1\\1\\1\end{matrix}\right\}F$$

Note that function 66, when XORed into OF, yields 69. The network synthesizer responds accurately to pattern regularity, and for OF it would produce one signal or one wire. Observe that 66 can be further decomposed:

$$6\left\{\begin{matrix}0\\1\\1\\0\end{matrix}\right. = 3\left\{\begin{matrix}0\\0\\1\\1\end{matrix} \quad \oplus \quad \begin{matrix}0\\1\\0\\1\end{matrix}\right\}5$$

$$6\left\{\begin{matrix}0\\1\\1\\0\end{matrix}\right. = 3\left\{\begin{matrix}0\\0\\1\\1\end{matrix} \quad \oplus \quad \begin{matrix}0\\1\\0\\1\end{matrix}\right\}5$$

Thus, 66 yields 33 and 55, which are each only one signal; this means that simple XOR hardware can be used directly. In terms of the somewhat complex sum function SO (Fig 2), the resulting adder schematic is shown in Fig 4.

Each occurrence of function 69, regardless of contributory variables, can be satisfied with the application of a "standard cell" of cascaded XOR gates, which may be classified with a schematic symbol for these gates (Fig 5).

## Decomposition of a Function

According to the principles of congruent partitioning in network synthesis, the greater the periodicity exhibited by a Boolean function, the simpler will be

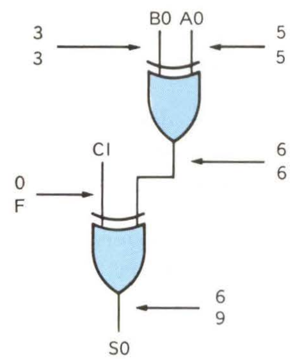



Fig 4 Sum function of simple adder. Single signal wires, noted with their hexadecimal truth table equivalents, are connected with two cascaded XORs to produce adder sum function

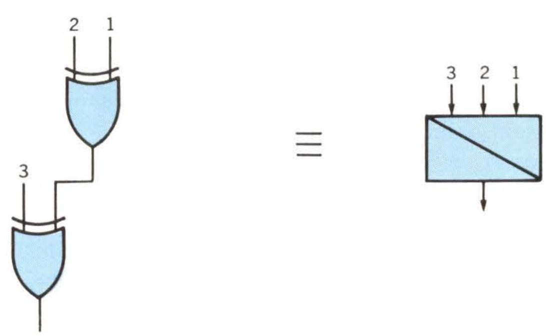



Fig 5 Cascaded XOR gate symbol. Because gate grouping is standard and frequently applied, it is replaced by single symbol which by its configuration represents function

its logic. A 4-variable function (D, C, B, and A) with the hexadecimal notation of 5555 is only a single wire or single variable A.

Consider the function 0F2D, which appears to have little periodicity. The derived logic is F = D′C + CB′ + CA + DC′BA′. Decomposing this function on an XOR basis yields two functions: 0F0F and 0022. Each function is clearly more periodic than the original. The logic for this combination is F = C ⊕ DBA′.

## Function Decomposition Example

A network synthesizer is not needed for identification of cascading XORs in an adder. The technique has been presented for familiarization with Boolean functions as patterned structures, and how they can be handled. Consider a corresponding standard cell candidate on the carry side of the adder. Observe another adder, also having a carry-in line, but with nine inputs (Fig 6). Here the 9-variable input function is very much larger than the 3-variable function of Fig 2 because the Boolean functional relationship has doubled in size six times. Complete listing of the 9-variable truth table would not only be awkward; it would also be difficult to read. It is enough to list the Boolean functions alone, for it is within these functions that the patterns of interest reside.

For functions of practical size, a designer seldom creates the Boolean function manually; instead, a FORTRAN expression is evolved. In this case, input to the synthesizer is simply F = N1 + N2 + N3. This input is accompanied by control parameters that inform the network synthesizer that N1 has only one variable (CI), while N2 (A0 to A3) and N3 (B0 to B3) have four variables each. The synthesizer is also advised that F has five output functions (CO and S0 to S3), which are one carry and four sum Boolean functions.

The synthesizer can be interrupted at any time during processing. If interrupted at the point of generating the Boolean functions, pattern characteristics of these added functions will appear as displayed in Fig 7. The 2-level (AND/OR) logic expressions of functions S2, S3, and CO are so complex that little would be gained by showing the gating schematic here. The simplifying effects of function decomposition have, as shown below, a substantial impact on this complexity.

Large scale function decomposition at present is more art than science. There is no closed expression or algorithm that will implement decomposition to the extent that the synthesizer, for example, implements Boolean functions with buildable logic equations. Even experienced designers resort to trial and error methods for evaluating their decomposition work. Were it not for the synthesizer, the cost of such trial and error methods would make function decomposition highly impractical. Since it is easy and inexpensive to submit decomposed functions to the synthesizer for analysis, a designer can afford an extensive search for simplifying patterns. Data from Fig 7 show how this search is implemented.

Functions S1 through S3 in Fig 7 will be decomposed into XOR segments. If handled correctly, decomposition

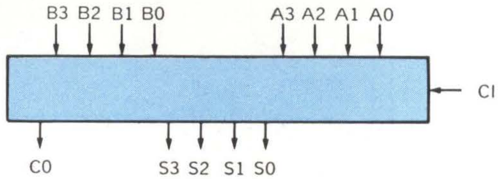



Fig 6 Symbology of 4 X 4-bit adder. 4-bit binary number (Bn) combines with another number (An) and carry-in (CI) to produce sum (Sn) and combined carry-out (CO)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| S0 | 5555 | AAAA | 5555 | AAAA | 5555 | AAAA | 5555 | AAAA |
| | 5555 | AAAA | 5555 | AAAA | 5555 | AAAA | 5555 | AAAA |
| | AAAA | 5555 | AAAA | 5555 | AAAA | 5555 | AAAA | 5555 |
| | AAAA | 5555 | AAAA | 5555 | AAAA | 5555 | AAAA | 5555 |
| S1 | 3333 | 6666 | CCCC | 9999 | 3333 | 6666 | CCCC | 9999 |
| | 3333 | 6666 | CCCC | 9999 | 3333 | 6666 | CCCC | 9999 |
| | 6666 | CCCC | 9999 | 3333 | 6666 | CCCC | 9999 | 3333 |
| | 6666 | CCCC | 9999 | 3333 | 6666 | CCCC | 9999 | 3333 |
| S2 | 0F0F | 1E1E | 3C3C | 7878 | F0F0 | E1E1 | C3C3 | 8787 |
| | 0F0F | 1E1E | 3C3C | 7878 | F0F0 | E1E1 | C3C3 | 8787 |
| | 1E1E | 3C3C | 7878 | F0F0 | E1E1 | C3C3 | 8787 | 0F0F |
| | 1E1E | 3C3C | 7878 | F0F0 | E1E1 | C3C3 | 8787 | 0F0F |
| S3 | 00FF | 01FE | 03FC | 07F8 | 0FF0 | 1FE0 | 3FC0 | 7F80 |
| | FF00 | FE01 | FC03 | F807 | F00F | E01F | C03F | 807F |
| | 01FE | 03FC | 07F8 | 0FF0 | 1FEF | 3FCF | 7F8F | FF00 |
| | FE01 | FC03 | F807 | F00F | E01F | C03F | 807F | 00FF |
| C0 | 0000 | 0001 | 0003 | 0007 | 000F | 001F | 003F | 007F |
| | 00FF | 01FF | 03FF | 07FF | 0FFF | 1FFF | 3FFF | 7FFF |
| | 0001 | 0003 | 0007 | 000F | 001F | 003F | 007F | 00FF |
| | 01FF | 03FF | 07FF | 0FFF | 1FFF | 3FFF | 7FFF | FFFF |

Fig 7 Boolean functions of 4 X 4-bit adder. Hexadecimal patterns are directly analogous to Boolean function patterns of Fig 2, with single exception that task is much larger

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 3333 | 3333 | CCCC | CCCC | 3333 | 3333 | CCCC | CCCC |
| 3333 | 3333 | CCCC | CCCC | 3333 | 3333 | CCCC | CCCC |
| 3333 | 3333 | CCCC | CCCC | 3333 | 3333 | CCCC | CCCC |
| 3333 | 3333 | CCCC | CCCC | 3333 | 3333 | CCCC | CCCC |
| | | | | | | | |
| 0000 | 5555 | 0000 | 5555 | 0000 | 5555 | 0000 | 5555 |
| 0000 | 5555 | 0000 | 5555 | 0000 | 5555 | 0000 | 5555 |
| 5555 | FFFF | 5555 | FFFF | 5555 | FFFF | 5555 | FFFF |
| 5555 | FFFF | 5555 | FFFF | 5555 | FFFF | 5555 | FFFF |

Fig 8 Decomposed function S1. Successful decomposition of function S1 from Fig 7 is marked by highly periodic binary patterns of two component functions

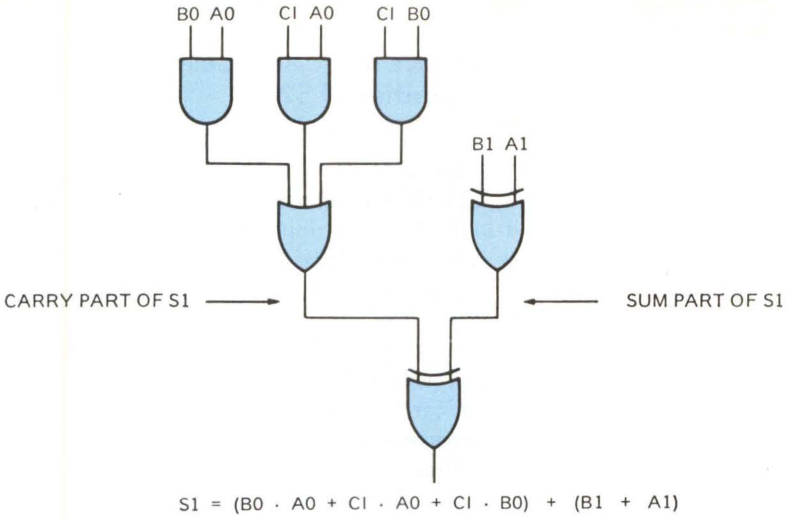



Fig 9 Schematic of adder function S1. Decomposing original function S1 into two simpler parts reveals that one part is sum subfunction and other is carry subfunction

cleanly separates the sum from the carry functions for each stage (0, 1, 2, 3) of addition. Now patterns of the carry function can be scrutinized for standard cell candidates via the synthesizer. The Boolean functions in the figure have been listed in groups of four characters to make readily apparent any binary-based patterns that may exist. Observe that function S1 is made up of sets of four identical hexadecimal characters: 3, 6, C, and 9. For simplicity, S1 can be abridged by using only one character for each set of four, resulting in

36C9 36C9
36C9 36C9
6C93 6C93
6C93 6C93

It has been shown that 3 ⊕ 5 = 6; so 6 can be decomposed into 3 and 5. Similarly, 5 ⊕ C = 9, and F, which is all ones, will complement whatever is XORed with it, eg, F ⊕ C = 3. The above array can then be decomposed into

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 36C9 | 36C9 | | 33CC | 33CC | | 0505 | 0505 |
| 36C9 | 36C9 | = | 33CC | 33CC | ⊕ | 0505 | 0505 |
| 6C93 | 6C93 | | 33CC | 33CC | | 5F5F | 5F5F |
| 6C93 | 6C93 | | 33CC | 33CC | | 5F5F | 5F5F |

Expanding the two simpler arrays in the same way that S1 is abridged, ie, by repeating each character four times, a new version of S1 is shown in Fig 8. The two functions of Fig 8, when combined with an XOR, produce function S1 of Fig 7. The synthesizer accepts these functions and produces logic equations that equate to the schematic of Fig 9.

Note that the standard cell previously defined as cascaded XORs applies in the case of Fig 9. Exploiting this relationship reveals that functions S0 and S1 result in a somewhat simpler combined schematic (Fig 10).

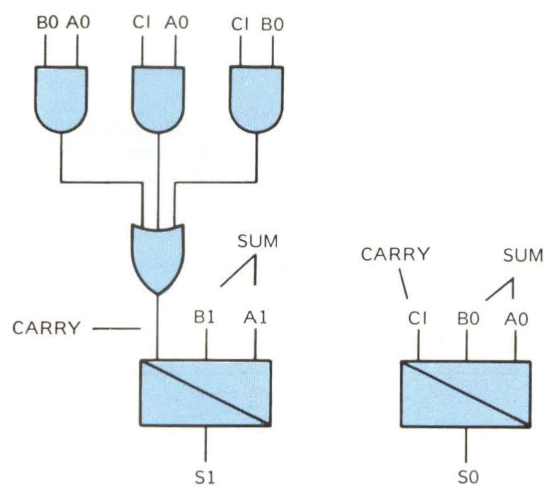



Fig 10 Symbolized schematics of functions S0 and S1. With symbol for cascaded XORs, it can be seen that sum function input is invariant, while carry-in function increases in complexity with additional stage

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| F1 | OFOF | OFOF | OFOF | OFOF | FOFO | FOFO | FOFO | FOFO |
| | OFOF | OFOF | OFOF | OFOF | FOFO | FOFO | FOFO | FOFO |
| | OFOF | OFOF | OFOF | OFOF | FOFO | FOFO | FOFO | FOFO |
| | OFOF | OFOF | OFOF | OFOF | FOFO | FOFO | FOFO | FOFO |
| F2 | 0000 | 1111 | 3333 | 7777 | 0000 | 1111 | 3333 | 7777 |
| | 0000 | 1111 | 3333 | 7777 | 0000 | 1111 | 3333 | 7777 |
| | 1111 | 3333 | 7777 | FFFF | 1111 | 3333 | 7777 | FFFF |
| | 1111 | 3333 | 7777 | FFFF | 1111 | 3333 | 7777 | FFFF |

Fig 11 Decomposed function S2. When compared with function S2 in Fig 7, it can be seen that not only do periodic structures appear, but also a highly structured pattern that should be investigated in function F2

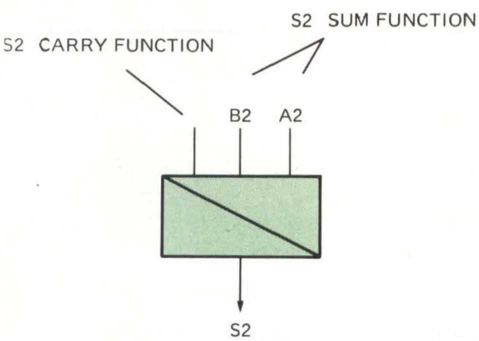



Fig 12 Part of developing S2 schematic. Signals B2 and A2 are XORed together and their result is in turn XORed with S2 carry function

## Appearance of a Carry Cell Candidate—Decomposition of S2

In a manner similar to that described above, function S2 is decomposed into the two functions F1 and F2 (Fig 11). The regularity of the patterns denotes simplified logic. First or upper function F1 appears to be the sum component. This is clear from the XOR appearance of the pattern, ie, the OFOF FOFO arrangement. The synthesizer quickly verifies this conclusion with logic equations that produce the schematic of Fig 12. The standard cell for the cascading XOR is used directly, and S2 carry logic is unresolved. Examination of the carry component of the decomposed function in Fig 11 shows that two predominant patterns prevail: 0137 and 137F. A possible standard cell candidate emerges because these same patterns appear in the adder carry function (CO) of Fig 7, although the distribution differs. In designing with pattern recognition, cross comparisons are indispensable.

Pattern 0137 is fed into the synthesizer, resulting in a suggestion that the candidate standard cell can be made up of four NAND gates. If 0137 is complemented into EC80 and fed into the synthesizer, it is seen that the same interconnection of four NAND gates is indicated, wherein all inputs and the output are inverted. Fig 13 symbolically depicts the candidate standard cell. The synthesizer can seek application of a subfunction like the standard cell candidate to a global function, in this case the complete adder. The system architect can evaluate the desirability of exploiting the findings of the synthesizer. In this case the synthesizer suggests that a likely set of signals to apply to the standard cell logic for function S2 is B1, B0, A1, and A0 in place of 4, 3, 2, and 1 respectively. If the designer concurs, the result provided by the synthesizer appears in Fig 14.

Here the S2 logic is resolved by three standard cells and two gates. In general, standard cells have very

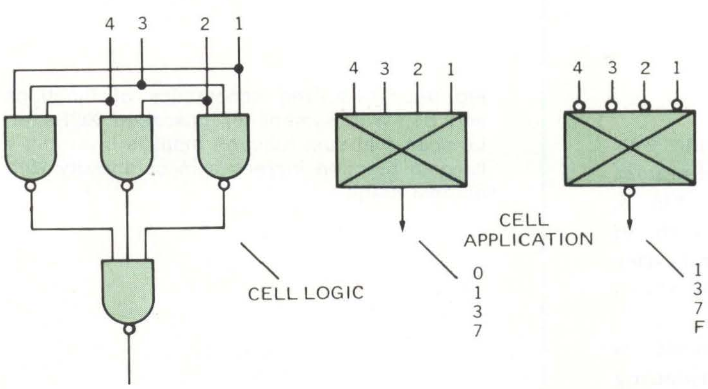



Fig 13 Candidate standard cell. Crossed rectangle is symbol for candidate standard cell. Invertors are peripheral to basic logic of pattern 0137

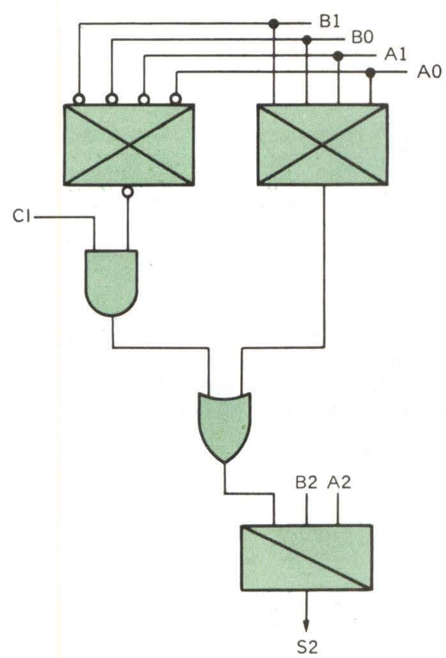



Fig 14 Completed schematic of function S2. External carry-in CI only appears in carry function where it is combined with carries from first stages of adder

compact and simple LSI designs. Each of the three standard cells in Fig 14 would take little more area than a full gate, so that parts count and overall area are reduced.

## Decomposition of S3 Function

Relatively complex function S3 of Fig 7 is analyzed by the same technique as that used for S2. When decomposed, the XOR components of S3 are as shown in Fig 15. Note that patterns of the decomposed S3 functions are much simpler than those of the original S3 of Fig 7. The complementing nature of the upper function indicates that it is a sum function, leaving the lower function as the carry component of S3. Patterns 0137 and 137F consistently reappear, albeit with differing distributions. Following the procedure outlined for function S2, the somewhat more complex function S3 is produced by the synthesizer as shown in Fig 16.

## Carry-Out Function Derivation

Carry-out (CO) function of Fig 7 has a clear distribution of standard cell patterns 0137 and 137F. Nothing can be gained by attempting a decomposition since there is a marked pattern regularity already in existence for this function. The implication is that there is no sum function component to make CO a complex pattern; a review of the original premise shows that there is indeed no B4, A4 combination present. According to described procedures, the synthesizer produces logic equations that lead to the schematic of Fig 17. The synthesizer handles factor assignments in the same manner as previously discussed.

Fig 18 shows the 4 x 4-bit adder in schematic composite form with the derived standard cells. The cells which are used should reside in a standard cell library; the designer who must make up the entire function needs only use these cells as though they were standard single gate cells, resident in the same library.

## Summary

Identification and application of standard cells which are unique to the adder function simplify design and layout for a 4 x 4-bit adder. The sum function cell is well known to the designer, but the fact that a carry function cell also exists, and is somewhat more frequently used than the sum function cell, is revealed by a network synthesizer. While the knowledgeable designer could, perhaps, identify the carry component cell without assistance of the synthesizer, it has been shown that it is a powerful aid in the pattern recognition task for the LSI designer. The adder used in this discourse is a simple device, but finding a common

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 00FF | 00FF | 00FF | 00FF | 00FF | 00FF | 00FF | 00FF |
| FF00 | FF00 | FF00 | FF00 | FF00 | FF00 | FF00 | FF00 |
| 00FF | 00FF | 00FF | 00FF | 00FF | 00FF | 00FF | 00FF |
| FF00 | FF00 | FF00 | FF00 | FF00 | FF00 | FF00 | FF00 |
| 0000 | 0101 | 0303 | 0707 | 0F0F | 1F1F | 3F3F | 7F7F |
| 0000 | 0101 | 0303 | 0707 | 0F0F | 1F1F | 3F3F | 7F7F |
| 0101 | 0303 | 0707 | 0F0F | 1F1F | 3F3F | 7F7F | FFFF |
| 0101 | 0303 | 0707 | 0F0F | 1F1F | 3F3F | 7F7F | FFFF |

Fig 15 Decomposed function S3. Complementing patterns of upper function clearly denote XOR properties while lower, or carry function, is regular

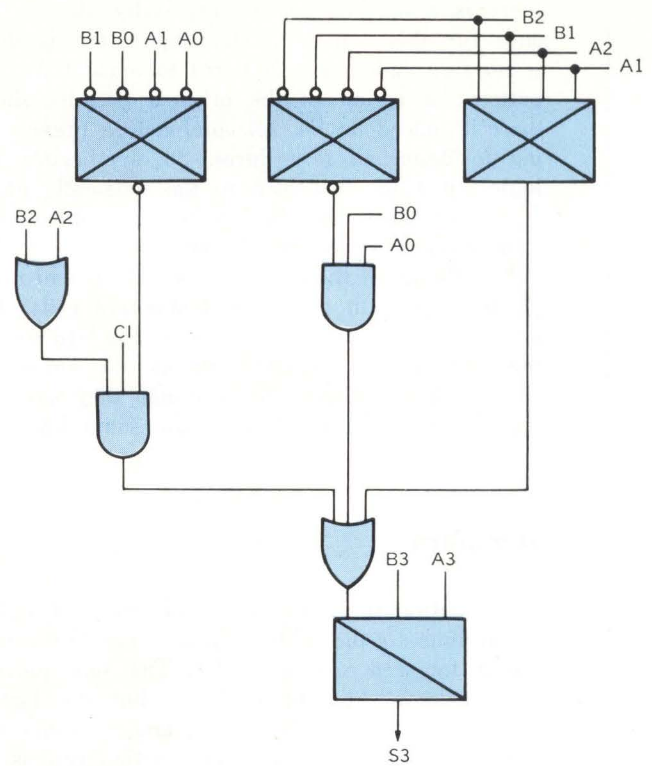



Fig 16 Completed schematic of function S3. Sum function (B3, A3) has been isolated completely from carry function by reason of decomposition action of Fig 15

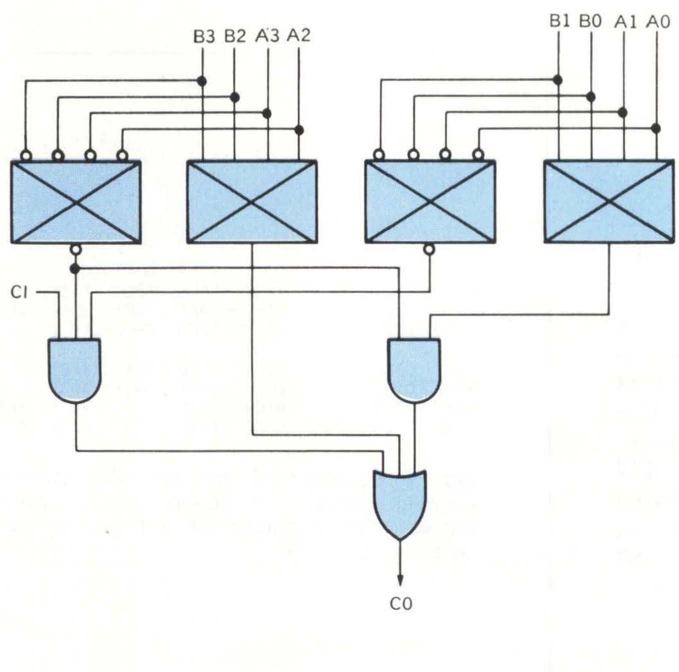



Fig 17 Completed schematic of carry-out. Four standard cells and three gates make end carry-out (CO) function relatively simple. Note complete absence of summing influence

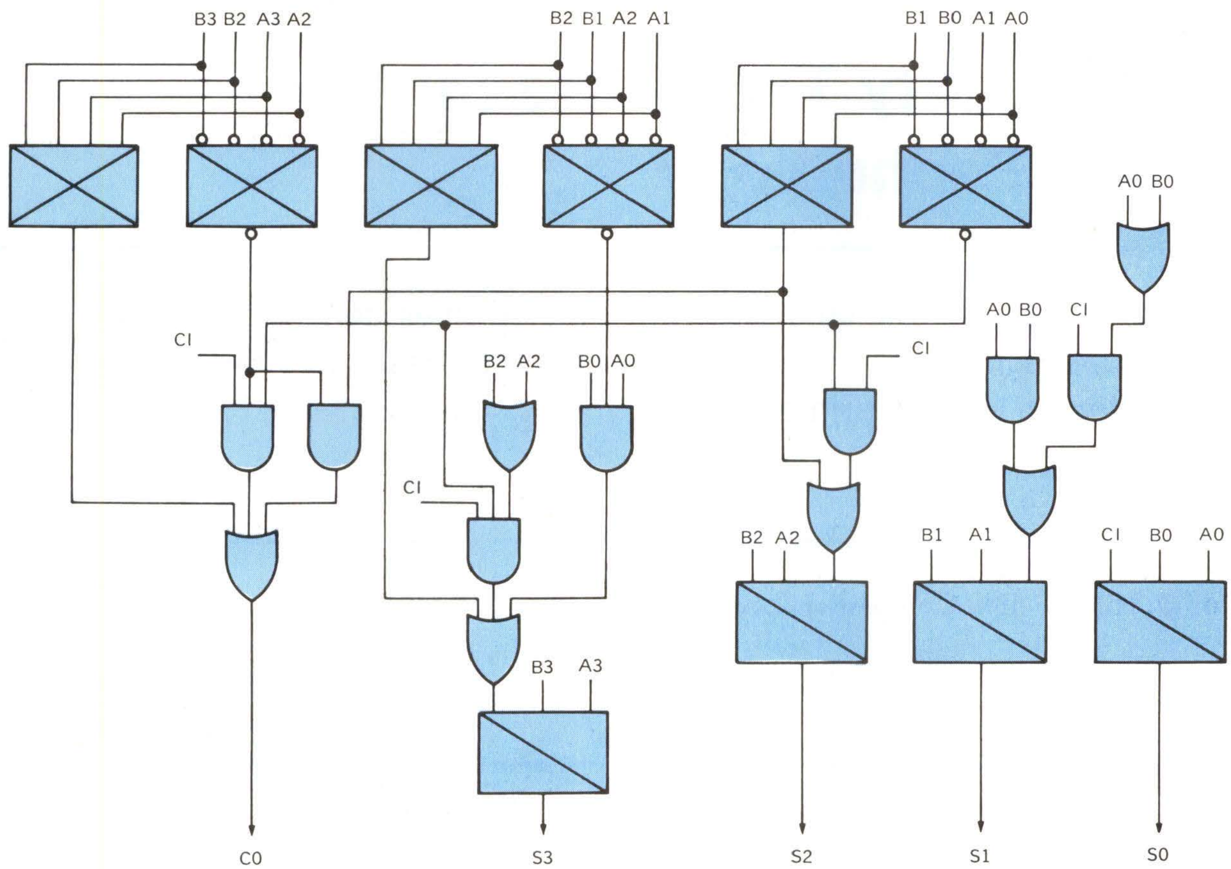



Fig 18 Four by four-bit adder composite schematic. Economizing impact of standard cells can be seen in this circuitry, where there are more carry cells than there are sum cells

hardware component in a more complex system would mandate use of the synthesizer. Last but not least, the analysis technique described should shorten and simplify LSI design for cost effectiveness.

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TECH NOTE

# Print Quality Tradeoffs in Ink Jet Technology

High quality dot matrix character printing involves concerted efforts by graphic, mechanical, and logic designers to resolve interacting tradeoffs for an ink jet printer

**James D. Hill** IBM Corporation, Lexington, Kentucky

Ink jet printing produces high quality characters by squirting extremely small drops of ink onto untreated paper (Fig 1). The minute drops pass through an electrostatic charging field that deflects them vertically to specific intersections of a dot column. The printhead—mounted on a carrier—moves horizontally at a constant velocity to sweep out a typical grid matrix of 240 dots/in (94/cm) on the paper. Dots are formed at the grid intersections, as specified by a read only memory, to produce a typewriter quality character. Print quality design ramifications for the IBM 6640 Document Printer included design tradeoffs and decisions that governed the chosen character configuration.

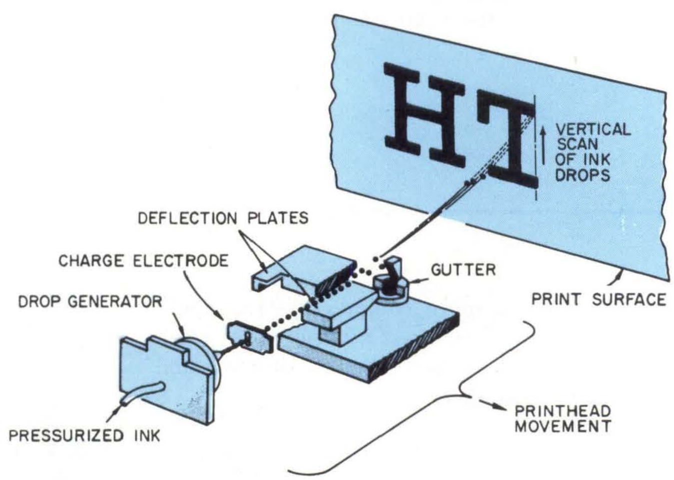


Fig 1 Components of ink jet printer. Ink is forced through nozzle in drop generator, forming jet. Ultrasonic pressure waves induced by generator break up jet into uniform drops. Drops form in region of charge electrode, which induces predetermined charge on each drop. Charged drops then pass through electrostatic field formed by deflection plates. Drops that possess little or no charge are intercepted by gutter and recirculated. Vertical impact point of drops that continue on to impact paper is determined by magnitude of initially induced charge

### Print Quality

The print design project began with the supposition that the best possible shapes,[1] or type fonts, would approximate the high quality characters produced by a Selectric® Composer.

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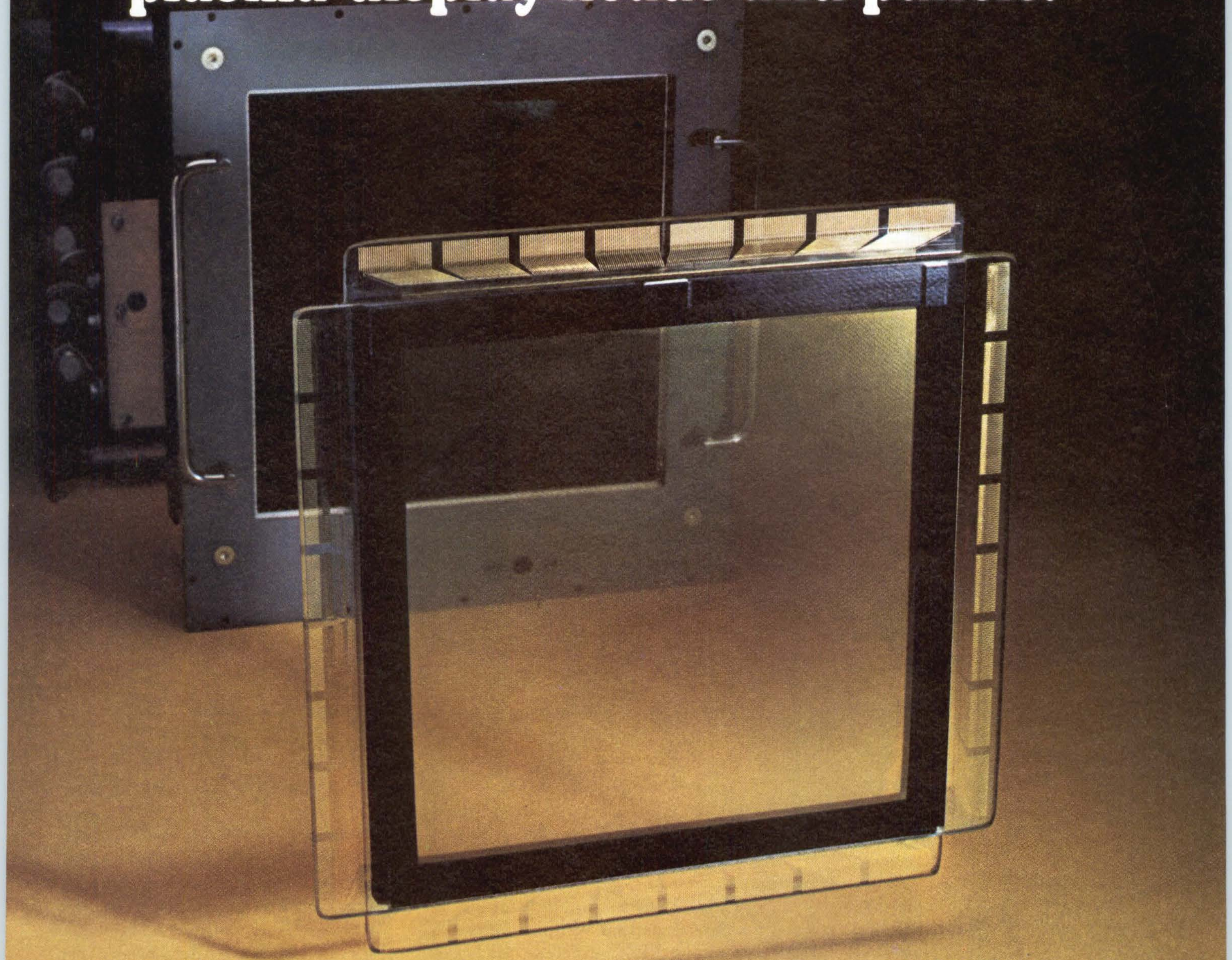

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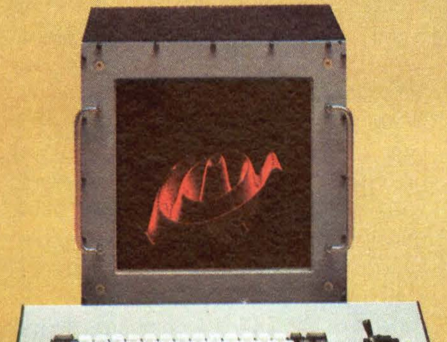

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However to attain this goal, several design tradeoffs had to be made. For example, resolution (number of dots/in) involved a compromise between print speed and print quality.

To establish an acceptable definition of print quality for the ink jet printer, the following design parameters were evaluated: character proportion, alignment, character fill, edge definition, and spatter (dirt). Aesthetic character proportion involves a compromise among artistic design of the character, need to make up the character as a series of dots in a matrix, and relationship to associated characters. Alignment is based on controlling the deflection of drops with respect to carrier position (horizontal alignment) while achieving accurate drop placement (vertical alignment). Character fill requires that the appropriate dot size be accurately placed on the paper without voids in the black areas. Edge definition—a measure of the intrusion of the white of the paper onto the black of the character—is a function of matrix grid resolution and dot size. Spatter concerns any extraneous ink particles produced on the paper surrounding the formed character. All these parameters are optimized by careful selection of operating point characteristics.

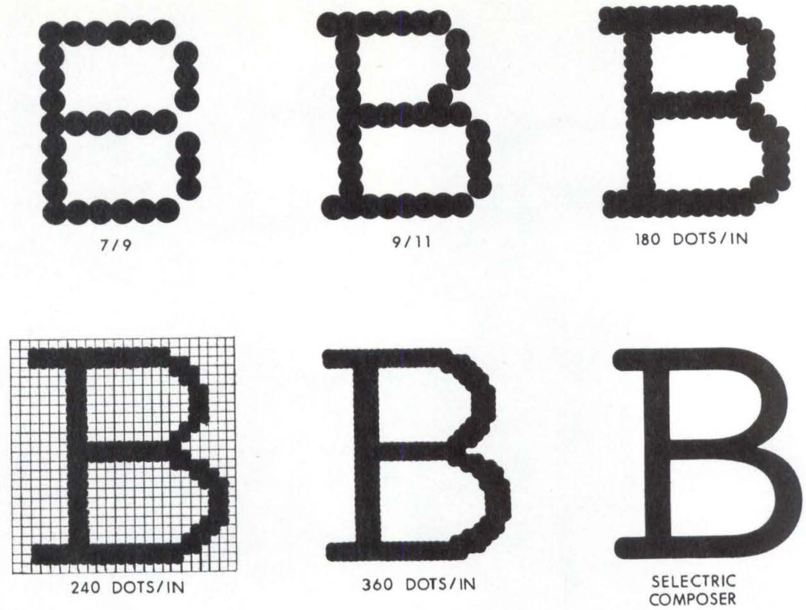


Fig 2 Dot matrix print examples. These examples show comparisons of letter B design in several matrix resolutions; Selectric Composer® B is shown for reference. Progression of resolutions demonstrates matrix printing limitations with respect to basic character form, line smoothness, and line-weight variation

### Resolution

Resolution significantly impacts the aesthetic aspects of print quality. Currently, a wide variety of matrix printers is available, ranging from low resolution wire matrices (7 x 9 dots and 9 x 11 dots) to extremely high resolution photocomposers[2] (Fig 2). A resolution choice lies between these two extremes. At a sufficiently high resolution, the discrete step-like changes associated with dot matrix printing become indiscernible to the eye and, therefore, cease to influence print quality.

The resolution chosen for the ink jet printer resulted from studies in character design, ink jet technology capabilities, application burst print rate requirements, and printer costs. Resolution interacts with ink jet technology mainly in dot size and print rate. State-of-the-art requirements dictated that dot size be 0.003 to 0.007" (0.076 to 0.178 mm) in diameter to be compatible with a 200- to 300-dot/in (80- to 120-dot/cm) resolution (Fig 2).

Character design investigations identified the requirements for line weights, effect of digitization on diagonals and curves, and impact of designing for different character widths. Line weight is the thickness of the various elements of a character; a 2-dot line weight implies a thickness in vertical elements of 0.010" (0.254 mm). Sample documents printed using a 2-dot line weight produce printed line weights slightly less than corresponding line weights in typewriter characters. With a 2-dot line weight, it is difficult to design diagonal and curved lines that print adequately. However, with a 3-dot line weight, the print quality is aesthetically acceptable. Character widths normally associated with word processor applications are 10 and 12 char/in (4 and 5/cm) (pitch), or proportional spacing.

Previous work on multiple-pitch printers determined that the least common denominator was 1/60 in; therefore, resolution should be 60n (where n is an integer). The Table lists the number of dots needed per character for a 12-pitch character at three resolutions to satisfy the 60n criterion.

To achieve a target print rate close to 100 char/s requires an ink jet printhead that can form 100,000 to 120,000 drops/s. This rate range implies that an average of 500 to 600 dots/char is available for printing. A 12-pitch typewriter character requires 800 dots at 240-dot/in (94-dot/cm) resolution. Considering the low black and white dot ratio in the specified typestyles and an ink supply rate of 117,000 drops/s, an acceptable 12-pitch burst print rate of 92 char/s was finally selected.

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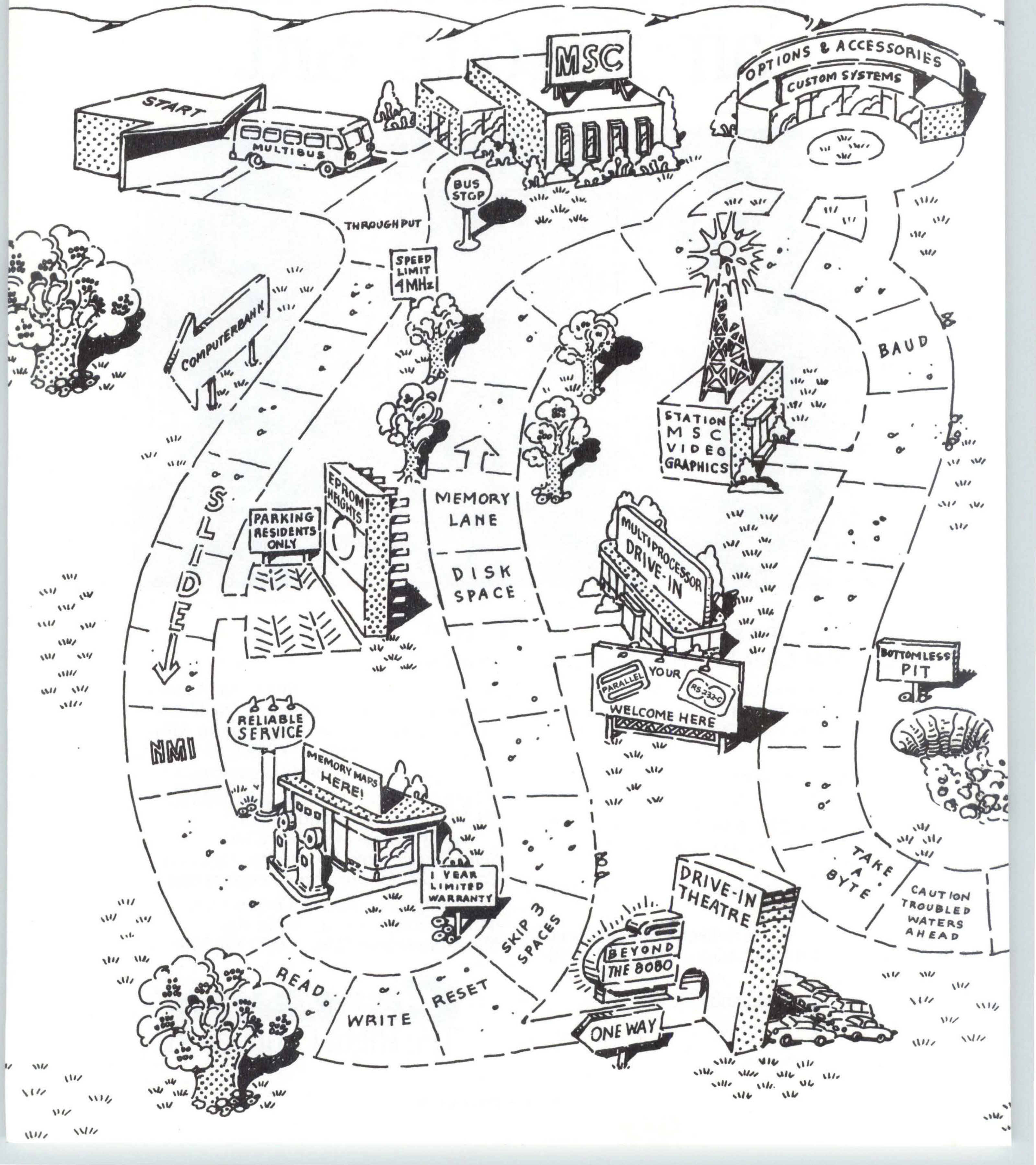

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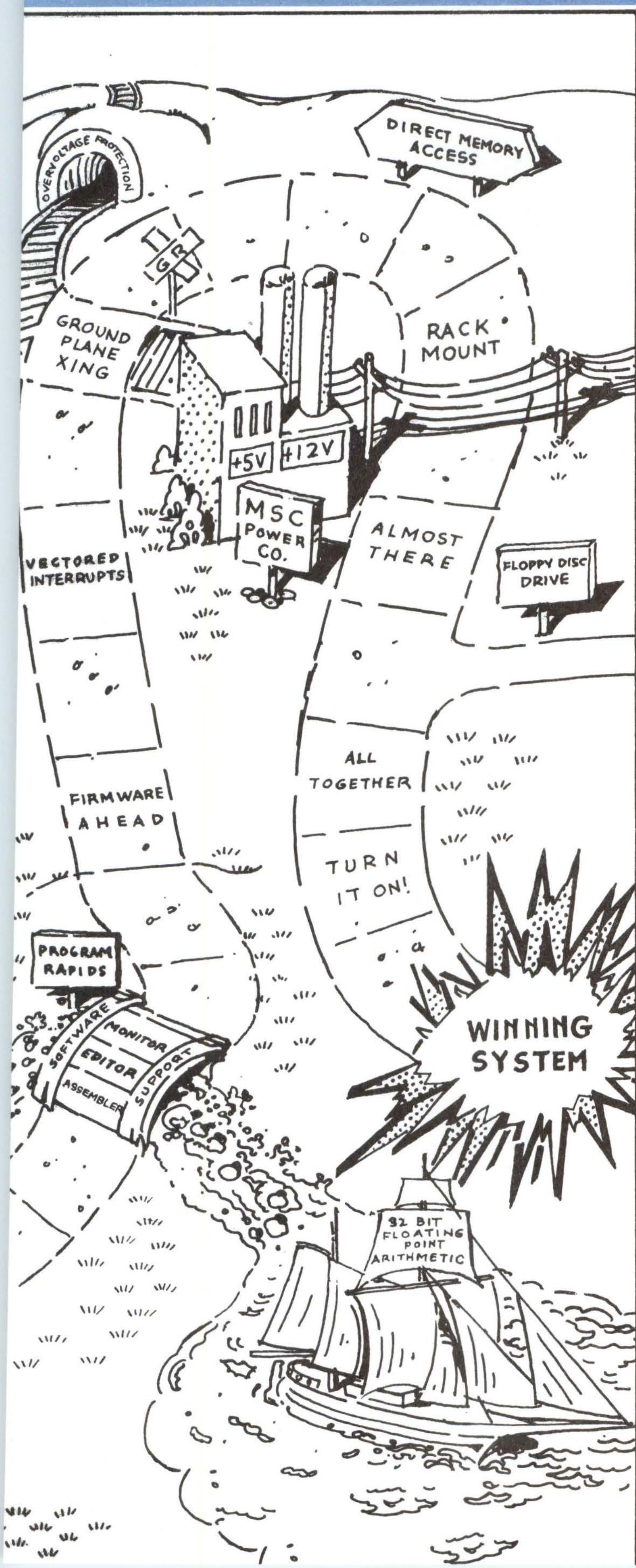


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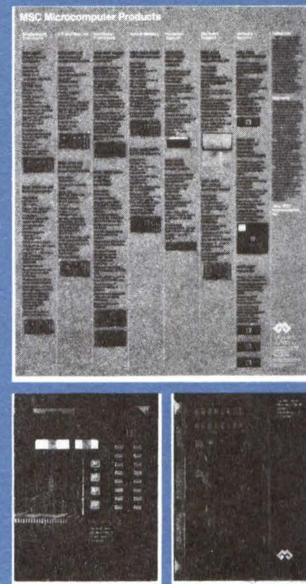


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Additionally, graphic design studies determined that a resolution of 240 dots/in provided adequate print quality for word processing applications.

### Drop Placement

A dot matrix technique has been designed to form the desired characters with a center to center spacing (both horizontal and vertical) of 1/R, where R = resolution (see Fig 2). Each square—or segment—formed by the dot matrix represents a potential black area on the printed page.

The drop placement mechanism has to place the dots accurately at each theoretical grid location on the paper. Failure to place dots accurately results in degradation of print quality and in deviation from the desired character shape. Examples of problems solved are uniform and nonuniform dimensional changes of the grid (distorted characters), rotational distortion of the grid (tilted characters), different dot sizes or shapes than anticipated (larger or smaller character heights or widths), and misplaced dots relative to neighboring dots (character voids or bumps).

Printer costs and print quality are strongly affected by the allowable tolerances on printer parameters that influence drop placement accuracy; fortunately, absolute placement is not necessary. For example, a dot can be 0.0013" (0.0330 mm) off the mark without degrading edge definition. Because ink spread and fill vary greatly with differences in paper, the drop-placement tolerance of ±0.0013" was selected. Drop placement accuracy depends on the drop placement scheme, the type of printhead transport drive, and the electronics for ink jet support.[3]

Initial design work yielded a print scheme that essentially used every drop of ink. This every-drop print scheme had acceptable print quality, but it required critical adjustment of the operating point parameters and was abandoned in favor of an every-other-drop print scheme that forces the first two drops of each black segment of a vertical column to coalesce in flight forming a merged pair. The mark on the paper made by the merged pair is circular and 0.008" (0.203 mm) in diameter. A mark made by two drops impacting independently would form an oblong dot. The center of impact of the merged pair is moved up in the segment to prevent the formation of a void between its mark and the remainder of the segment.

**Number of Dots in 12-Pitch Characters**

| Resolution (Dots/Inch) | Horizontal (Dots) | Vertical (Dots) | Dots/Char |
|---|---|---|---|
| 180 | 15 | 30 | 450 |
| 240 | 20 | 40 | 800 |
| 360 | 30 | 60 | 1800 |

Another characteristic of the drop placement scheme is that the time allocated for printing a segment of a vertical scan (black or white) is not a linear function of the length of the segment. The position of a given dot in a scan with respect to a neighboring dot in an adjacent scan is thus dependent upon the pattern being printed and the speed of the printhead, while the scans are being printed. Because of the parameter combinations involved, a computer program was derived to simulate the scanning of characters to be printed and to flag those that could have print quality problems in the range of anticipated printhead velocities. Then, the affected character design was altered, if necessary.

The low cost, typewriter like printhead drive selected for the ink jet printer provides accurate placement of vertical scans, while traveling in the horizontal direction, via a 60-line/in (23.6-line/cm) optical grating. A grating sensor provides two outputs 90° out of phase. This 2-phase function enables the printer electronics to detect the absolute position of the printhead at all times. The grating electronics only define the time at which a vertical scan should be started. This establishes the bottom edge of the printed character and assures proper horizontal spacing of the bottom of the scan. If the velocity of the printhead changes excessively during the time required to print a scan, the vertical slope of each scan will be different, resulting in a fanning-out effect at the top of the character being printed. By shaping the acceleration profile of the printhead via the carrier drive design, the fanning effect is minimized.

Printer electronics (Fig 3), comprised of four major functions, are the controlling factor for accurate placement of the individual dots on paper.[3,4] The character generator encodes the information needed to print each character, and then retrieves and decodes information to reproduce the character on paper. The character generator also permits selection of available fonts from font memory. Drop-placement logic uses the decoded scan information from the character generator to define the vertical position of the drops on paper. The decoded scan information is converted into accurate voltage levels that charge the individual drops of ink at the precise instant they break off from the ink stream. Stream maintenance logic turns the stream off and on, turns on the deflection voltage after the stream is up and operating, indicates when the ink supply needs replenishing, establishes when to charge drops, and controls deflection height through pump pressure changes. A mechanical controller tracks the position of the carrier and provides information of where to place the scans horizontally.

Character height is influenced by the tolerance on the high voltage power supply (3300 V regulated to ±5%) that creates the deflection field, the gain of the final amplifier that drives the charge electrode,

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**Innovative Cartridge:** Both D120 and D140 models use a flat, thin (11″ square by .9″) self-ventilated cartridge weighing only 2.8 pounds.

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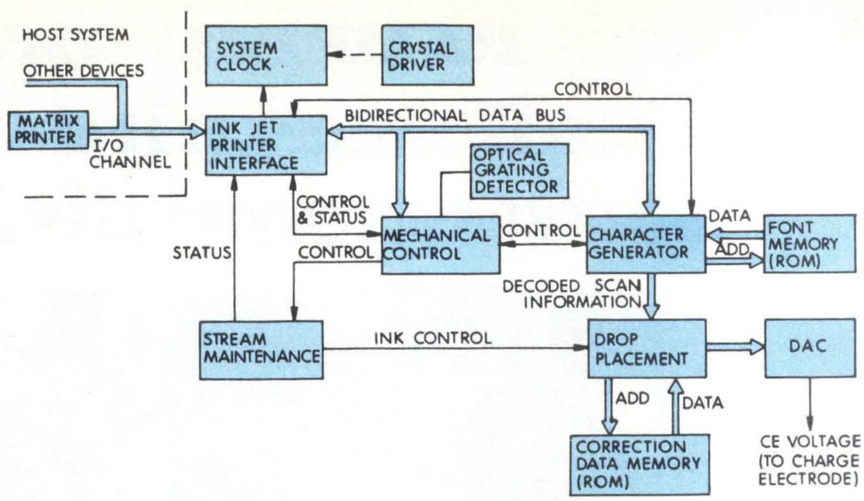


Fig 3 Printer electronics block diagram. Four major functional units—character generator, drop placement logic, stream maintenance, and mechanical control—influence drop placement accuracy by controlling drop generator and deflection system

and the accuracy of the deflection servo.[5] The latter maintains deflection height to ±2%, for example, deflection height of an upper case T is 0.102" (2.591 mm). The charge electrode amplifier is designed to tight tolerances to eliminate nonuniform distortion of characters because of amplifier nonlinearities.

The value of the charge-electrode voltage was determined through a table lookup (in excess of 3000 entries) and then converted from a binary number to a voltage. A resolution of 0.25 V achieves the dot placement tolerance of ±0.0013" (0.0330 mm). Therefore, a 10-bit digital to analog converter is needed to cover the range of charge-electrode voltages (0 to 210 V). The charge-electrode amplifier was designed to have a $2 \times 10^8$-V/s slew rate, a settling time of 4.3 µs (to 0.01% of final value), with a linearity of ±0.1% of final value.

### Summary

Judging the quality of the print produced by ink jet technology is highly subjective. However, certain important parameters beyond the aesthetics of graphic design can be identified and measured as criteria for acceptable print quality. Graphic design work on the ink jet printer demonstrated that it was possible to design quality type within the constraints of a medium resolution matrix of 240 dots/in (94/cm). Additionally, output demonstrated that the ink jet technology could yield high print quality documents at burst print rates of greater than 90 char/s.


### Acknowledgements

The author acknowledges the work of R. W. Roberson in establishing the font design parameters and his significant contribution in evaluating character resolution problems.

Acknowledgement is also due to L. G. Runyon for his invaluable help in determining print quality, to C. H. Wiebke for the extensive testing for print quality, and to K. Conklin for editorial assistance.


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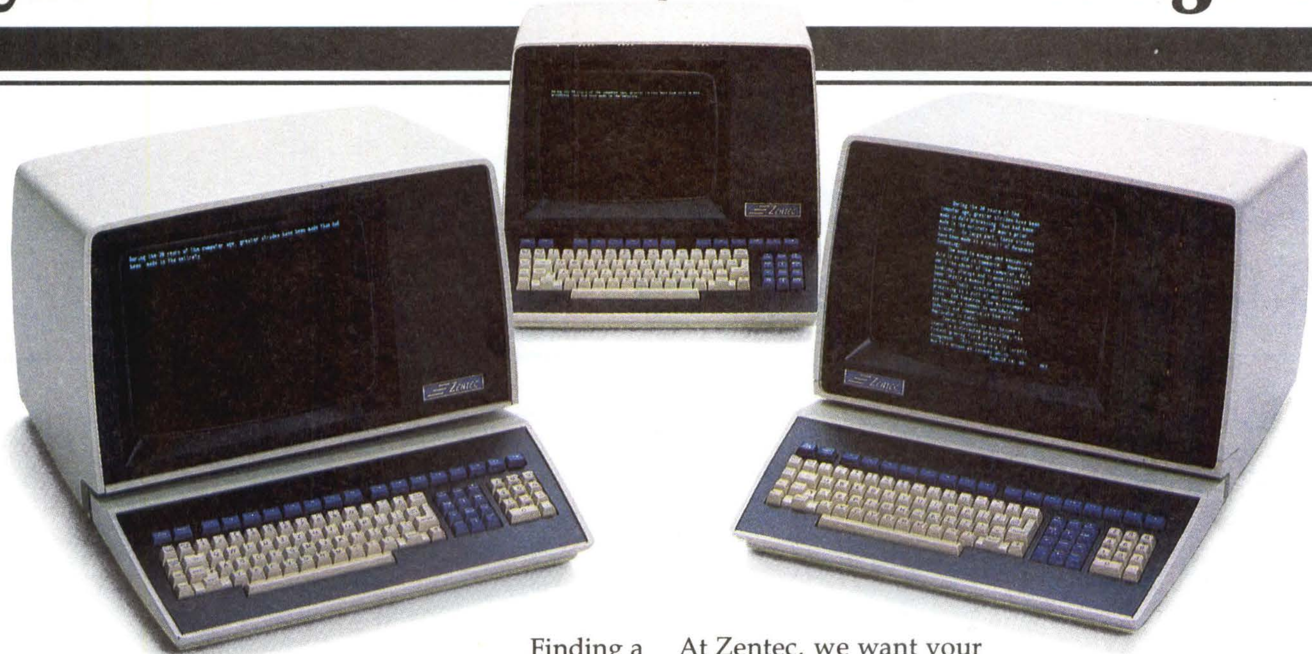

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DESIGN NOTE

# Computer Equipment Shielding Techniques

As computer sensitivity and sophistication increase, emi/rfi shielding becomes a more dominant factor in overall project design. Basic shielding design guidelines summarize the concepts of interference containment and exclusion

**John Severinsen** Metex Corporation, Edison, New Jersey

Associating electromagnetic interference exclusively with communications equipment—radio receivers, telephones, radar—evolved years ago when the term radio frequency interference was prevalent. Early applications of shielding were concerned mainly with attempts to exclude unwanted noise from radio frequency circuits. Today, however, electromagnetic interference shielding of digital and analog logic circuits in computers, microprocessors, and peripheral equipment is mandatory design practice.*

In addition to electromagnetic interference (emi) elimination, circuit protection must also be included against personnel interaction. Acrylic, wool, silk, and nylon materials within a computer room can create increased susceptibility to static charges. A spark from a human to a computer can produce a charge as high as 30 kV. If the cabinet and/or equipment are inadequately grounded, the charge can be transmitted to internal components, causing circuit overloading or malfunction.

In most computer installations, it is improbable that a single type of electronic shielding will solve all emi problems. Thus, several commonly encountered emi difficulties are presented along with recom-

*_EMI-RFI Shielding Handbook,_ Metex Electronic Shielding Group, Bulletin EMI 300, Edison, NJ, 1976

mended design guidelines for overcoming electromagnetic and static discharge interferences.

### Environmental Problems

Environmental shielding problems must be solved in two major areas: protecting equipment from exterior interference, and solving susceptibility problems from interior radiation. The emi source from which a computer, word processor, or peripheral equipment must be shielded may be a sparking commutator that is more than several feet distant, or a switching regulator power supply that is only inches away.

Broadband digital and analog circuits are sensitive to noise over a much wider spectrum than are tuned receiver circuits. Digital and analog circuits are often located in close proximity to other high speed, fast pulse devices, such as printers, teletypewriters, and keyboard terminals. In many industrial environments, broadband noise fields exist that are 40 to 60 dB stronger than those inside a communications center. Obviously, the 100:1 sensitivity advantage of digital circuits can be eliminated by a 1000:1 increase in environmental noise level. In an industrial environment, it is often difficult, time consuming, and costly to debug a contaminated system that operated correctly in production. Even after expensive debugging, a computer system may encounter a new source of emi and then malfunction again.

### Design Constraints

Shielding problem areas most often encountered by computer designers are presented below as a checklist, emphasizing features of the equipment that may require quantitative mathematical analysis (or, at least, qualitative estimates) of either generated interference levels or susceptibility, or both. Each of the three categories is divided into potential sources for generating internal interference and those circuits susceptible to external interference.

*Digital Computers, Peripherals, and Instruments*—Interference sources are switching power supplies; clock pulse and address strobe generators; drivers for impact printers, card punches, solenoid controls, and tape drive controls; brushes on drive motors for printers, discs, card readers, card punches, and drums; high voltage power supplies for cathode-ray tube (CRT) terminals; relays and contactors; and teletypewriters. Typical radiation spectrum is 50 kHz to 1 GHz.

Susceptible circuits are tape and disc reading heads and amplifiers; fast logic circuits; analog to digital input circuits; sense amplifiers; modem inputs; electro-optical isolators; regulator circuits in power supplies; and cables between enclosures.

*Analog Instruments and Process Control Systems*—Interference sources are relays and contactors; solenoid drives; switching power supplies; brushes on motors; switches; and program drums. Typical interference spectrum is 10 kHz to 50 MHz.

Susceptible circuits are power supply regulator circuits; signal conditioning and amplifying circuits; cables to transducers; and read heads on analog tape drives.

*Digital Process Control Systems*—Interference sources are essentially the same as for digital computers, peripherals, and instruments.

Susceptible circuits are fast logic circuits; multiplexer, signal conditioning, sampling, and preamplifier circuits on analog data acquisition front ends; electro-optical isolators; regulator circuits in power supplies; and input and intercabinet cables.

### Design Approaches

In general, shielding design practices for computers and process control equipment should guard against emi/radio frequency interference (rfi) by observing the following guidelines. Provide adequate power line filtering, continuous ground plane and busing integrity, and signal isolating cable layout. Position internal components to prevent signal interaction between disturbing elements and vulnerable circuits, eg, power supplies, relay contacts, and pulse generators. Provide as much shielding as usually found in moderately sensitive broadband radio frequency receiving equipment, eg, in an am/fm communications receiver with a 1-$\mu$V sensitivity from 0.5 to 100 MHz.

#### Filtering and Signal Isolation

For excellent signal isolation in cabling, yet allowing instantaneous access to cable leads when necessary, either before or after the cable is installed, a zip-on cable shielding should be used that has a 4-layer tin-plated copper-clad steel knitted wire mesh with an outer protective sheath of heavy duty vinyl.

Three paramount signal isolation rules should be observed. First, whenever possible, run balanced, parallel, differential, closely spaced —preferably twisted—signal lines into each 100 mV or less input. Designing for acceptance of differential inputs should be an early project decision. Second, always run low level signal input cables as near



See page 112


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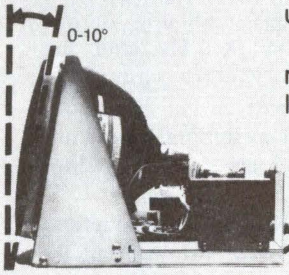


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to ground planes and equipment frames as possible. Never run noisy cables (ie, cabling carrying interference generating currents, such as dc into an inverter) near or parallel to ground planes, frames, or signal cables. Third, always shield signal lines separately, and ground both ends of the cable shield. An exception is when this grounding will cause ground loop currents to flow in the shield.

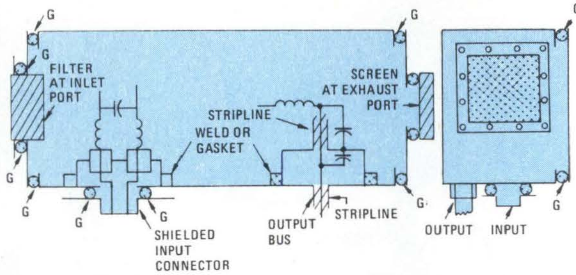


Fig 1 Containment shielding of switching regulator power supply. Main enclosure is gasketed for interference containment at all seams. Air inlet port has emi-tight and dust collecting air filter gasketed to main frame. Exhaust port has emi-tight screen gasketed to main frame. Shielded input connector subassembly, with appropriate gasketing, isolates input filter from power supply circuits. Feedthrough capacitors ensure effective line filtering. Shielded output bus subassembly, with appropriate gasketing, isolates output bus filter from power supply circuits. Stripline techniques supplement discrete component filtering

### Internal Component Arrangement

Specific recommendations for internal arrangement of components for minimum interactive emi depend upon the particular design. However, general guidelines are listed. In the near field case, which applies to equipment less than 10′ (3 m) in maximum internal dimension, component spacing is critical. In general, both the transverse and radial electromagnetic fields vary inversely with the cube of the distance between the interfering source and the sensitive circuit in the near field. Consequently, moving a noisy switching regulator module from an original position of 5″ (13 cm) from a PC card cage to a position that is 15″ (38 cm) away will reduce the interference effect by 27:1, or almost 30 dB.

Recommended methods to reduce interference coupling are to shield the interfering source generator, not the receiver (ie, the sensitive circuit and/or its associated cabling.) These methods involve enclosing power supplies, clock pulse power amplifiers, or printer drive triggered power circuits with a shield.

Careful evaluation is required in designing ground buses and ground planes. A long, thin ground bus is actually a fine, broadband, transmitting antenna for high level pulsed ground return currents. Make this bus type a low impedance path, as wide as possible in the direction perpendicular to the current flow, and very tightly coupled or electrically bonded to the structural frame and its separate electrical ground. Also, to avoid ground loops make sure that ground paths are not shared by both low level and high level circuits. The impedance of a bus is approximately inversely proportional to its perimeter transverse to current flow. Thus, doubling the width is more effective than doubling the thickness—except at dc.

### Containment Shielding of High Energy Broadband Power Supplies

A large percentage of power supplies in electronic equipment employ switching regulators, square wave inverters, blocking oscillator/flyback circuits, and other related duty cycle circuits that generate broad interference spectra at relatively high energy levels, typically, 80 to 100 dB above 1 $\mu$V/m in a 1-kHz bandwidth, from 10 kHz to 100 MHz.

The nominal input to a typical offline switching regulator power supply is 115 V, 60 Hz, and the output is 5 Vdc. However, input and output wiring will carry (and radiate) broadband switching noise, unless design steps are taken to eliminate this noise. In addition, switching circuits and associated inductors, transformers, rectifiers, and filters will all radiate broadband interference, unless shielded. Fig 1 illustrates several techniques recommended for shielding or otherwise inhibiting interference radiation from a switching regulator power supply.

### Exclusion Shielding of Digital Instruments

Many digital instruments, as well as small digital computers, digital process controls, and digital signal processors, contain logic circuits and sometimes low level analog interfaces that must be protected against both externally and internally generated interference. In Fig 2, internal sources of significant interference include the switching regulator power supply, the clock pulse/strobe pulse generator, and the impact printer mounted behind the front panel. External sources of interference are primarily other peripheral devices that are not adequately shielded themselves. The interference spectrum is 10 kHz to 50 MHz, which implies that slot lengths to 2.4″ (60 mm) are tolerable.

It would be possible to use containment shielding on the three internal sources of interference, and to use the enclosure to shield against

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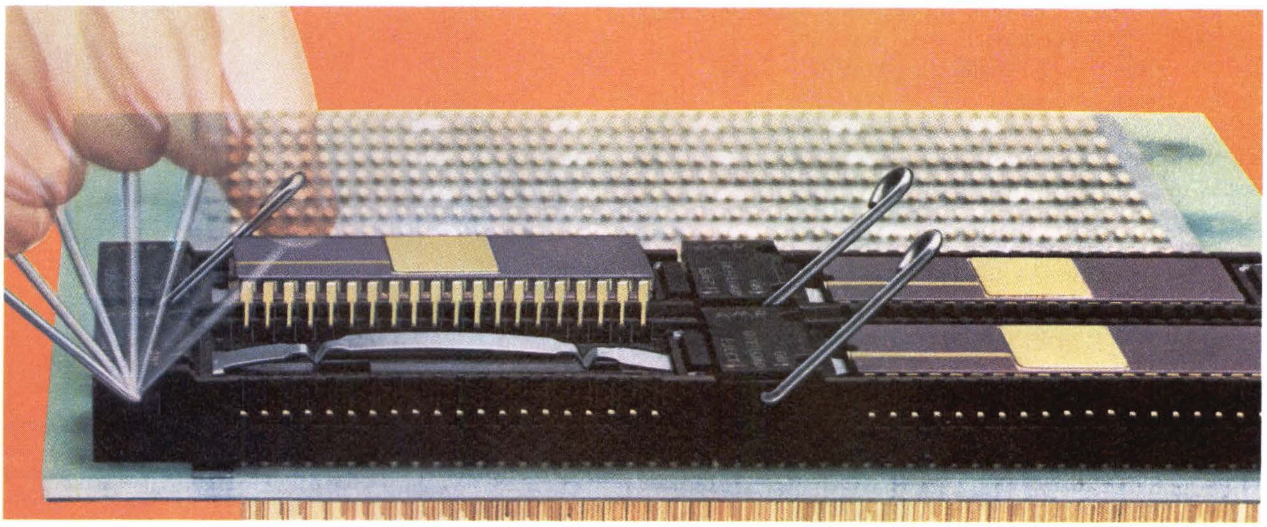

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the external interference; however, this approach would be much more expensive than the solution suggested: a single exclusion shield structure around the digital logic circuit. Fig 2 illustrates several recommended techniques for the construction of an exclusion shield for a compact group of circuit elements.

### Enclosure Considerations

Diverse emi shielding and static discharge protection requirements affect the design of a computer enclosure. Fig 3 highlights both the constraints and the available solutions. Each potential discontinuity in the shielding relates to the methods by which the designer can restore shield integrity.

Restoration of the emi shielding effects lost by panel holes, structural cutouts, and other necessary openings in the enclosure surface is required. This restoration may entail a variety of materials and devices, such as gasketing in the form of strip materials, available in all metal or with elastomer core, made of formed knitted wire mesh; elastomer pressure sealing strip in parallel with a knitted metal mesh strip for pressure seal gasketing; emi shielded windows containing finely knitted wire with asymmetrical openings laminated between two layers of acrylic or glass, for covering meters and displays; air filtering panels of several layers of woven wire mesh with integral emi frame gasketing and retaining grille; and ventilation panels consisting of aluminum honeycomb structures mounted in emi gasketed frames.

Provisions must be included against static discharge, regardless of the extent of emi shielding. Available, for example, are highly conductive and resilient knitted wire mesh pads that are placed between unpainted mating surfaces at strategic points to ensure excellent contact between parallel structures, such as ground planes and ground buses.

It is essential to take precautions to design into every aspect of electronic shielding those constructions that are necessary to meet, depending on the application, all key shielding specifications and standards. □

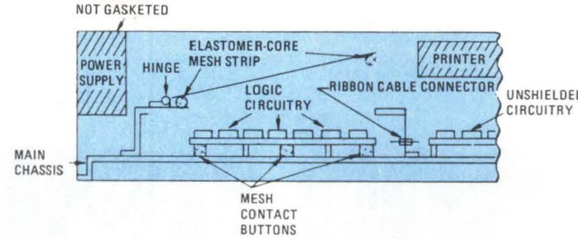



Fig 2 Exclusion shielding of digital logic PC board. Elastomer core gasketing located under hinged cover ensures uniform and continuous emi seal, with high compliance, despite relatively high flexibility of light metal cover. Mesh contact buttons ensure tight electrical contact between metal of main chassis and ground bus area on bottom of PC card. Metal well structure creates isolated environment for entire logic module. Well structure is gasketed at all seams to avoid need for close tolerances in manufacture. Only entry allowed to well structure is ribbon connector for digital signal and power supply leads. Connector is less than 2" (5 cm) in width—a tolerable slot length. Pickup external to well is handled by bypassing inside well or by impedance control of external circuits

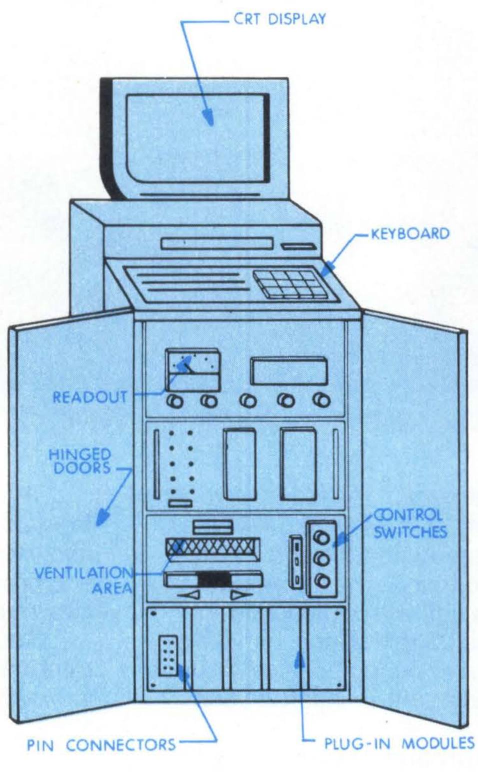
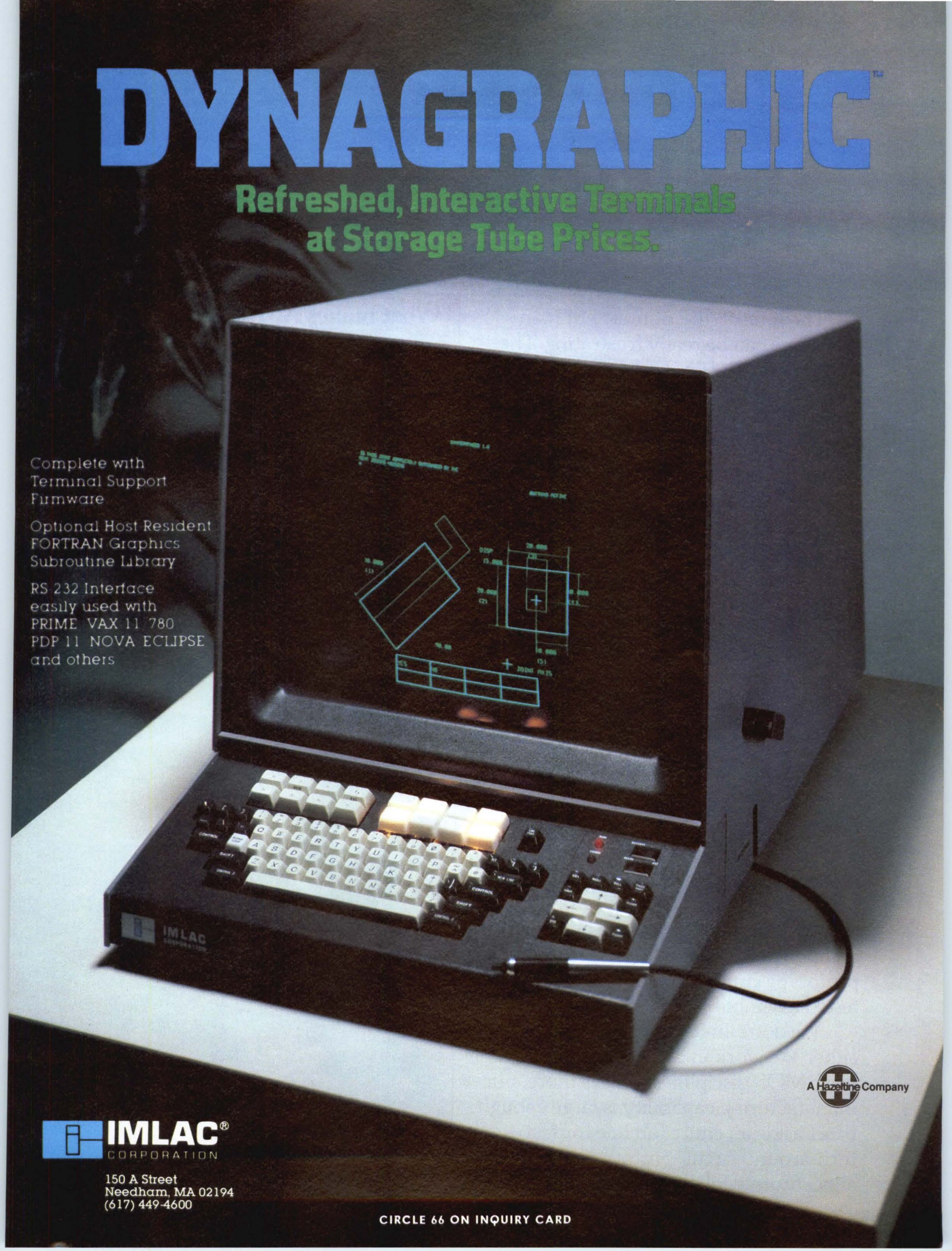



Fig 3 Typical shielding and static discharge problem areas in computer and process control enclosures. Digital logic, particularly clock pulse generators and data strobe circuits including core memory address generators, justify containment shielding of complete system enclosure, plus signal and power cables between computer and peripherals. Computer logic also demands exclusion shielding, as well as electrostatic discharge protection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In a word: experience. We have the longest history in custom, with a record of more than 1200 circuits designed and produced since 1966. And we've been involved in customer designed projects for six years, longer than anyone else, completing more than 300 circuits.

We're geared to work with your in-house MOS designers or an independent design firm. Or we can handle your

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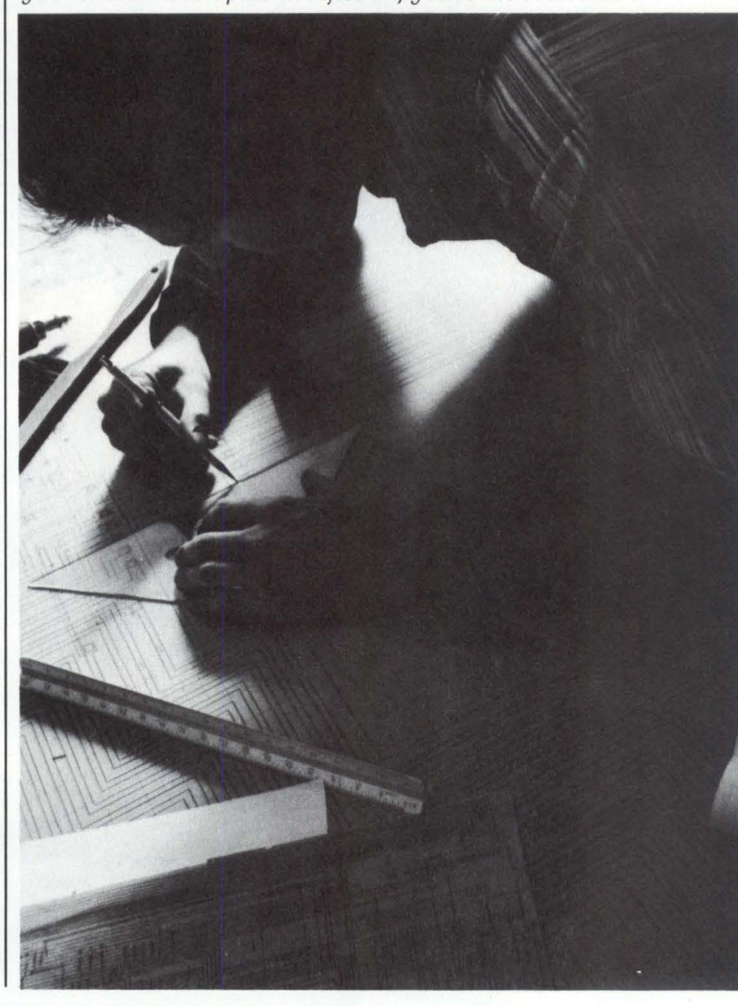

# circuit isn't the problem.
# a manufacturer

## Comparison of MOS Processes

| | P Chan Hi $V_T$ Metal | P Chan $1^2$ Metal | P Chan SiGate | N Chan SiGate | Comple-mentary MOS | N Chan $1^2$ | N Chan $1^2$ + dep Lds. | VMOS |
|---|---|---|---|---|---|---|---|---|
| Speed (per unit area) | 6 | 4 | 5 | 3 | 2 | 3 | 1 | 0 |
| Power Consumption (low speed) | 6 | 2 | 4 | 5 | 1 | 5 | 3 | 3 |
| Area (per logic function) | 4 | 3 | 3 | 2 | 5 | 2 | 1 | 0 |
| Noise Immunity | 4 | 2 | 5 | 5 | 1 | 4 | 3 | 3 |
| Logic Flexibility | 3 | 1 | 3 | 3 | 1 | 2 | 1 | 1 |
| On-Chip Clock Generation | 4 | 2 | 5 | 4 | 1 | 3 | 2 | 2 |
| Bipolar Compatibility | 5 | 2 | 3 | 1 | 1 | 1 | 1 | 0 |
| Power Supply Latitude | 4 | 2 | 4 | 4 | 1 | 3 | 2 | 3 |
| Process Simplicity | 1 | 2 | 2 | 2 | 6 | 3 | 4 | 6 |

Rankings are relative among the processes, with the lowest number being most desirable.

*AMI offers 25 variations of four basic MOS processes. So you can pick the one that fits your product and budget.*

job from scratch, giving it the full custom treatment that has made us the leader in this field.

We're also in a unique position to advise you on the best way to tackle your application. As we also produce standard 4, 8 and 16-bit microprocessors (the S2000, S6800 and S9900), we may be able to show you a cost-effective way to mix standard MPUs and custom peripherals. Or customize a standard MPU specially for you.

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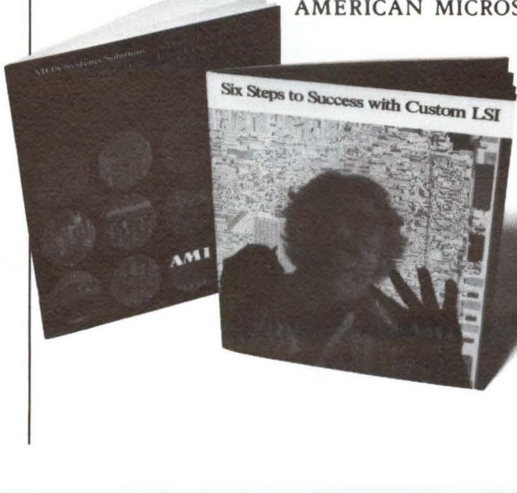


# INTERFACING FUNDAMENTALS: THE 6800 INSTRUCTION SET

**Andrew C. Staugaard**
Jamestown Community College

**Peter R. Rony and David G. Larsen**
Virginia Polytechnic Institute and State University

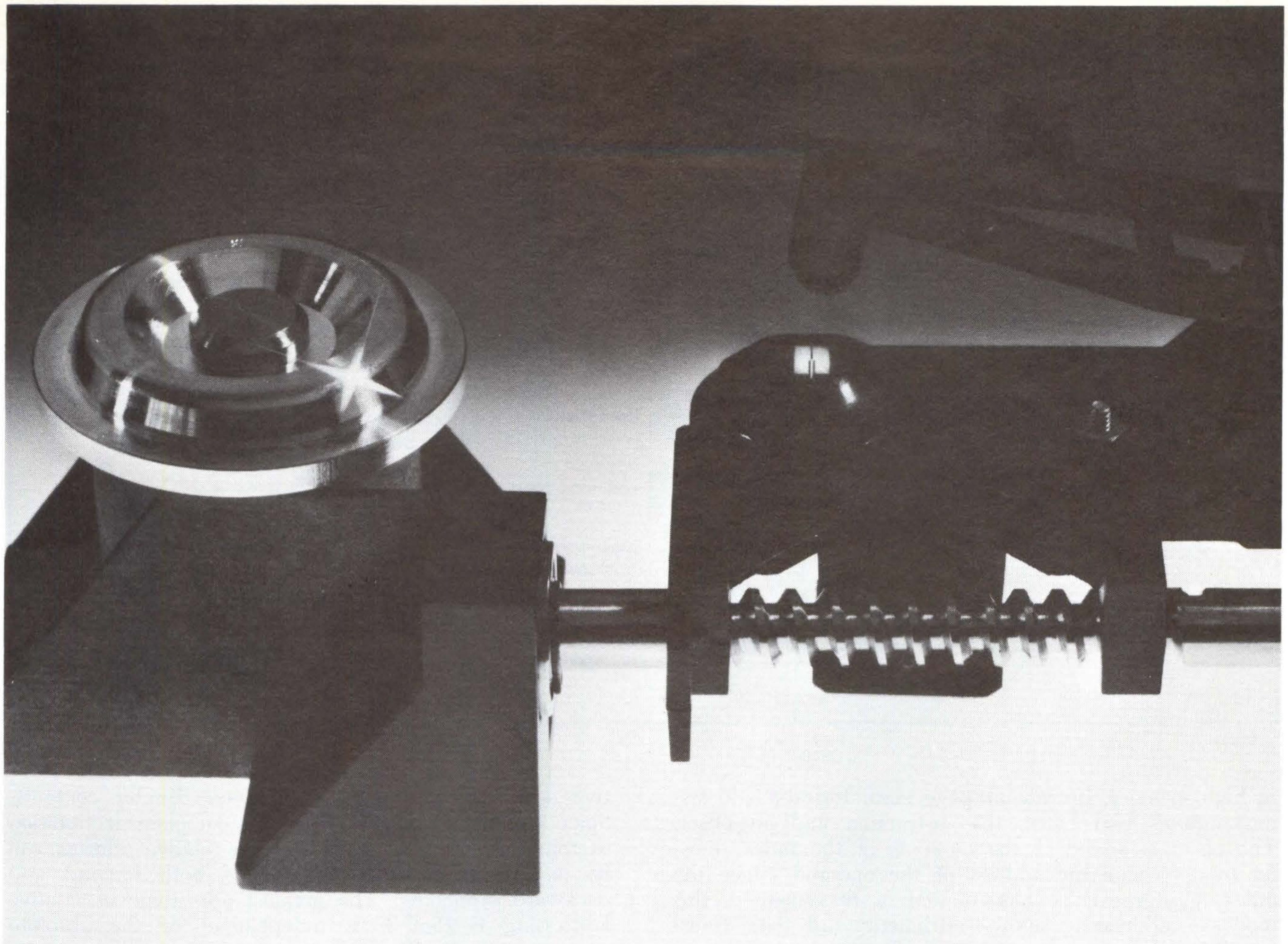
**Jonathan A. Titus and Christopher A. Titus**
Tychon, Inc

Evolved from Motorola's standard 6800 microprocessor architecture, the entire 8-bit family of central processing units provides hardware and software compatibility, as well as flexible and economic solutions to application problems. This covers a range from the sophisticated 6809 to the 6801, a complete single-chip microcomputer with onboard clock, read/write memory, read only memory, timer, and universal asynchronous receiver/transmitter. The instruction set of the 6800 central processing unit serves as the basis of all the rest. Future columns will build on this to detail the software and hardware features of the 6801/6803, 6802/6808, and 6809.

The 6800's internal organization is shown in Fig 1. All of the arithmetic and logic operations are performed using either of the 8-bit accumulators, A or B. Data may be loaded, transferred, added, subtracted, ANDed, ORed, XORed, and compared using either accumulator. Other instructions arithmetically combine the contents of the accumulators and transfer data between them. The 16-bit registers include the index register (IR), program counter (PC), and stack pointer (SP). As in other microprocessors, the program counter is simply a 16-bit counter that provides instruction sequencing. The index register gives the 6800 the power of indexed addressing, something that is not provided in the 8080/8085 family. This register may be incremented and decremented, as well as loaded from and copied into memory. The stack pointer register is similar to those used in other microprocessors; however, it always points to the next available location in a memory stack. The stack, located in read/write memory, saves the contents of other registers during the execution of subroutines and input/output interrupt operations. Unlike the 8080/8085 family, the 6800 provides automatic stacking of the contents of its internal registers when it starts the execution of subroutines and interrupt service routines.

Ability to make decisions is occasionally cited as the main reason that the concept of "intelligence" is associated with a computer. Results of various microprocessor operations cause conditions, which are represented by six flags inside the 6800: carry (C), overflow (V), zero (Z), negative (N), interrupt (I), and half-carry (H). When used in conjunction with the conditional branch instructions, these flags provide the microprocessor with decision making capability. Changes in the flags are generated as a result of arithmetic, logic, and data handling operations. The condition code register (CCR) keeps track of these flags. With the 6800 instruction set, the C, I, and V flags can be set or cleared and data can be transferred between the condition code register and accumulator A.

Six addressing modes utilized by the 6800 are inherent (implied), immediate, direct, extended, indexed, and relative. Fig 2 shows the instruction format for each mode. Inherent instructions are simply 1-byte instructions, such as halt, increment, and decrement, for which the meaning is obvious. Immediate instructions are those in which the operand immediately follows the instruction operating (op) code in memory. Direct addressing instructions require two bytes and are used when an operand is located in the lowest 256 bytes of memory (page zero). Extended addressing requires three bytes; it is utilized when an operand is located



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**CIRCLE 68 ON INQUIRY CARD**

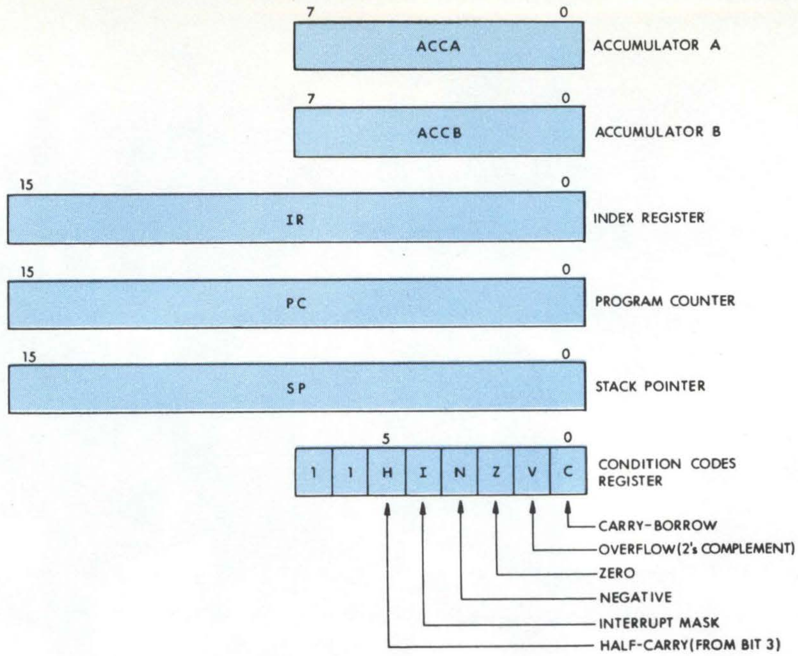



Fig 1 Internal architecture of 6800 microprocessor. Programming model consists of two accumulators that perform all arithmetic and logic operations, as well as three 16-bit registers and six flags (Courtesy of Motorola Semiconductor Products, Inc)

in high memory, outside of page zero. Indexed addressing requires two bytes, the instruction and an offset. The offset is added to the contents of the index register to determine the address of the operand. Since the index register can be incremented or decremented, this mode of addressing allows arithmetic and data transfer operations to be performed efficiently on data located in consecutive memory locations.

Relative addressing is utilized with the 6800 branch instructions. If a branch is initiated it will cause a new address to be loaded into the program counter, which in turn will cause the program to continue execution at the new address, the branch destination. Note in Fig 2 that a branch instruction requires two bytes: the instruction and a relative address. To determine the branch destination, the microprocessor adds the relative address to the current program counter contents. Since the microprocessor uses 2's complement notation to represent negative numbers, the relative address can be positive or negative to provide both forward and backward branching. The greatest advantage of relative addressing is that it is independent of the absolute memory address. Branching can be accomplished relative to the program counter contents; therefore, the proper branch destination is always achieved regardless of the program's location in memory.

The 6800 instruction set is comprised of 72 fundamental instructions. Along with the various addressing modes, the set totals 197 instructions. Other 8-bit microprocessors have more; however, it is not merely the number of unique instructions that makes one processor better than another. The power and flexibility of each

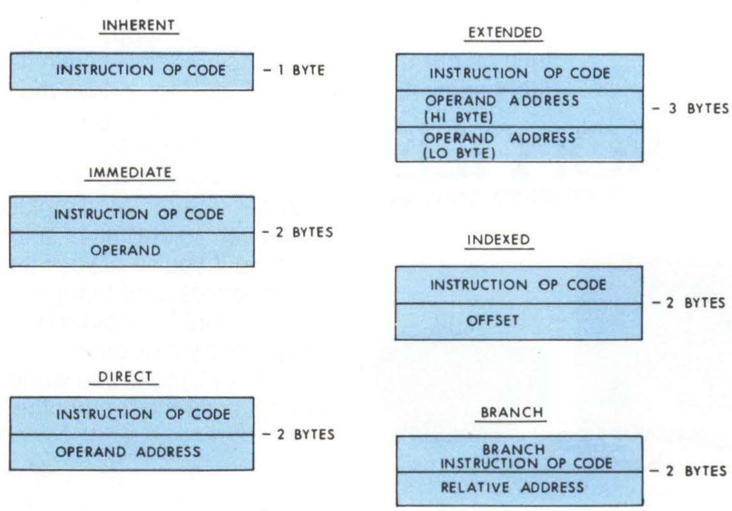
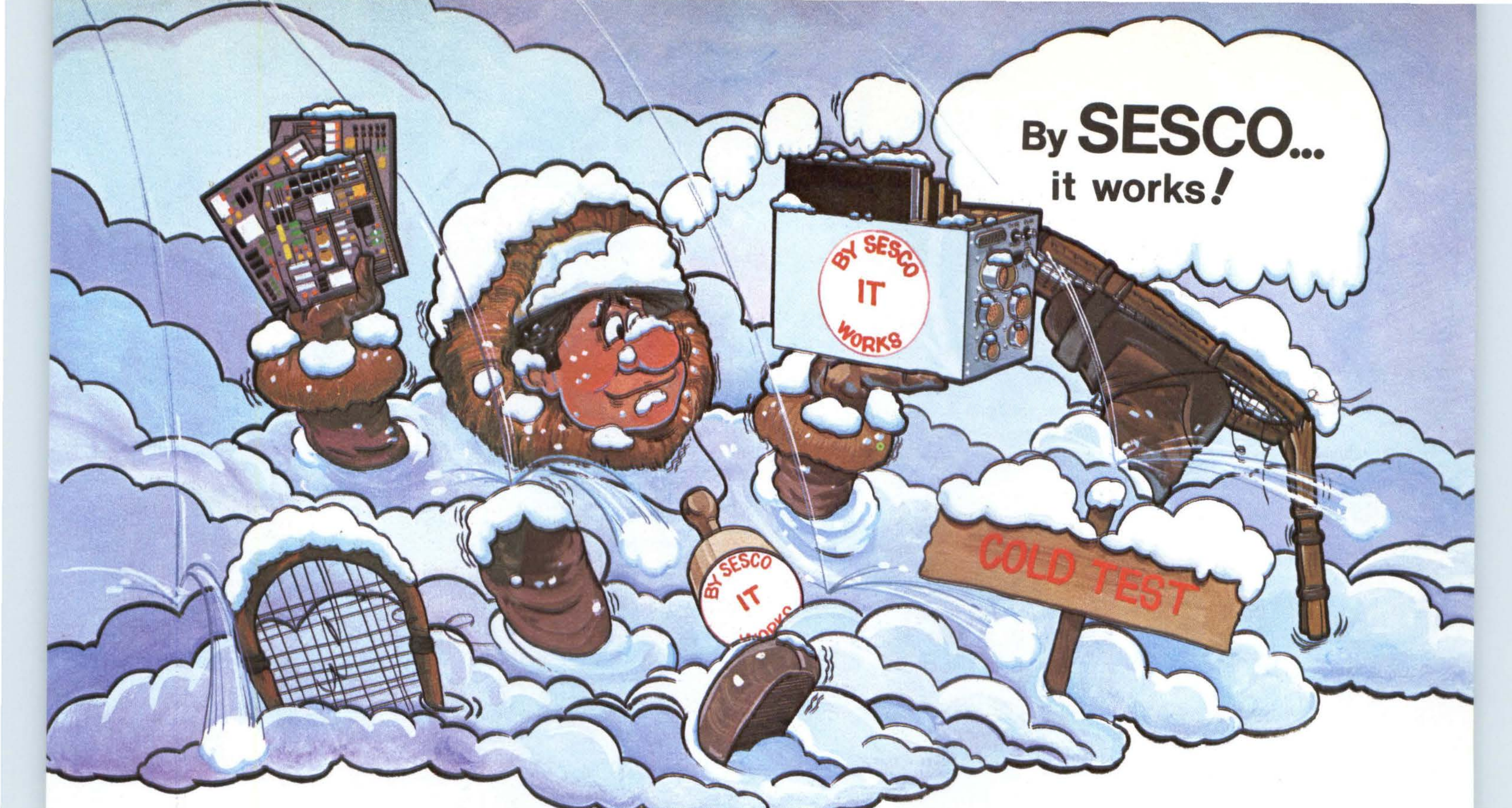



Fig 2 Addressing modes of 6800. Formats of six modes range from 1- to 3-byte instructions. Effective use establishes microprocessor's adaptability and instructional power

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Take our ruggedized SECS 80/10A Microcomputer, a functional counterpart of Intel's standard iSBC* single board computer, surround it with our equally ruggedized support modules, and you have the building blocks you need to design a system which will operate under the most severe environments.

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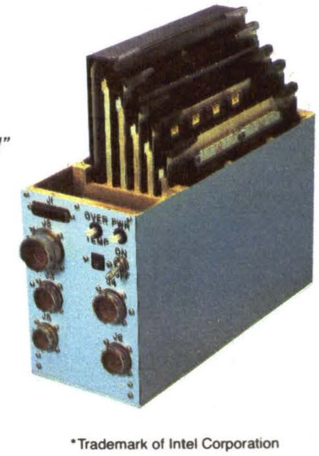

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**CIRCLE 69 ON INQUIRY CARD**

**Mnemonics For 6800 Instruction Set***

| | |
|---|---|
| ABA | Add Accumulators |
| ADC | Add with Carry |
| ADD | Add |
| AND | Logical AND |
| ASL | Arithmetic Shift Left |
| ASR | Arithmetic Shift Right |
| BCC | Branch if Carry Clear |
| BCS | Branch if Carry Set |
| BEQ | Branch if Equal to Zero |
| BGE | Branch if Greater or Equal Zero |
| BGT | Branch if Greater than Zero |
| BHI | Branch if Higher |
| BIT | Bit Test |
| BLE | Branch if Less or Equal |
| BLS | Branch if Lower or Same |
| BLT | Branch if Less than Zero |
| BMI | Branch if Minus |
| BNE | Branch if Not Equal to Zero |
| BPL | Branch if Plus |
| BRA | Branch Always |
| BSR | Branch to Subroutine |
| BVC | Branch if Overflow Clear |
| BVS | Branch if Overflow Set |
| CBA | Compare Accumulators |
| CLC | Clear Carry |
| CLI | Clear Interrupt Mask |
| CLR | Clear |
| CLV | Clear Overflow |
| CMP | Compare |
| COM | Complement |
| CPX | Compare Index Register |
| DAA | Decimal Adjust |
| DEC | Decrement |
| DES | Decrement Stack Pointer |
| DEX | Decrement Index Register |
| EOR | Exclusive OR |
| INC | Increment |
| INS | Increment Stack Pointer |
| INX | Increment Index Register |
| JMP | Jump |
| JSR | Jump to Subroutine |
| LDA | Load Accumulator |
| LDS | Load Stack Pointer |
| LDX | Load Index Register |
| LSR | Logical Shift Right |
| NEG | Negate |
| NOP | No Operation |
| ORA | Inclusive OR Accumulator |
| PSH | Push Data |
| PUL | Pull Data |
| ROL | Rotate Left |
| ROR | Rotate Right |
| RTI | Return from Interrupt |
| RTS | Return from Subroutine |
| SBA | Subtract Accumulators |
| SBC | Subtract with Carry |
| SEC | Set Carry |
| SEI | Set Interrupt Mask |
| SEV | Set Overflow |
| STA | Store Accumulator |
| STS | Store Stack Register |
| STX | Store Index |
| SUB | Subtract |
| SWI | Software Interrupt |
| TAB | Transfer Accumulators |
| TAP | Transfer Accumulators to Condition Code Reg |
| TBA | Transfer Accumulators |
| TPA | Transfer Condition Code Reg to Accumulator |
| TST | Test |
| TSX | Transfer Index Register to Stack Pointer |
| WAI | Wait for Interrupt |

*Courtesy of American Microsystems, Inc

fundamental instruction determines the capabilities of the processor. The 6800, like other microprocessors, achieves its instructional power and flexibility through the efficient use of its powerful addressing modes.

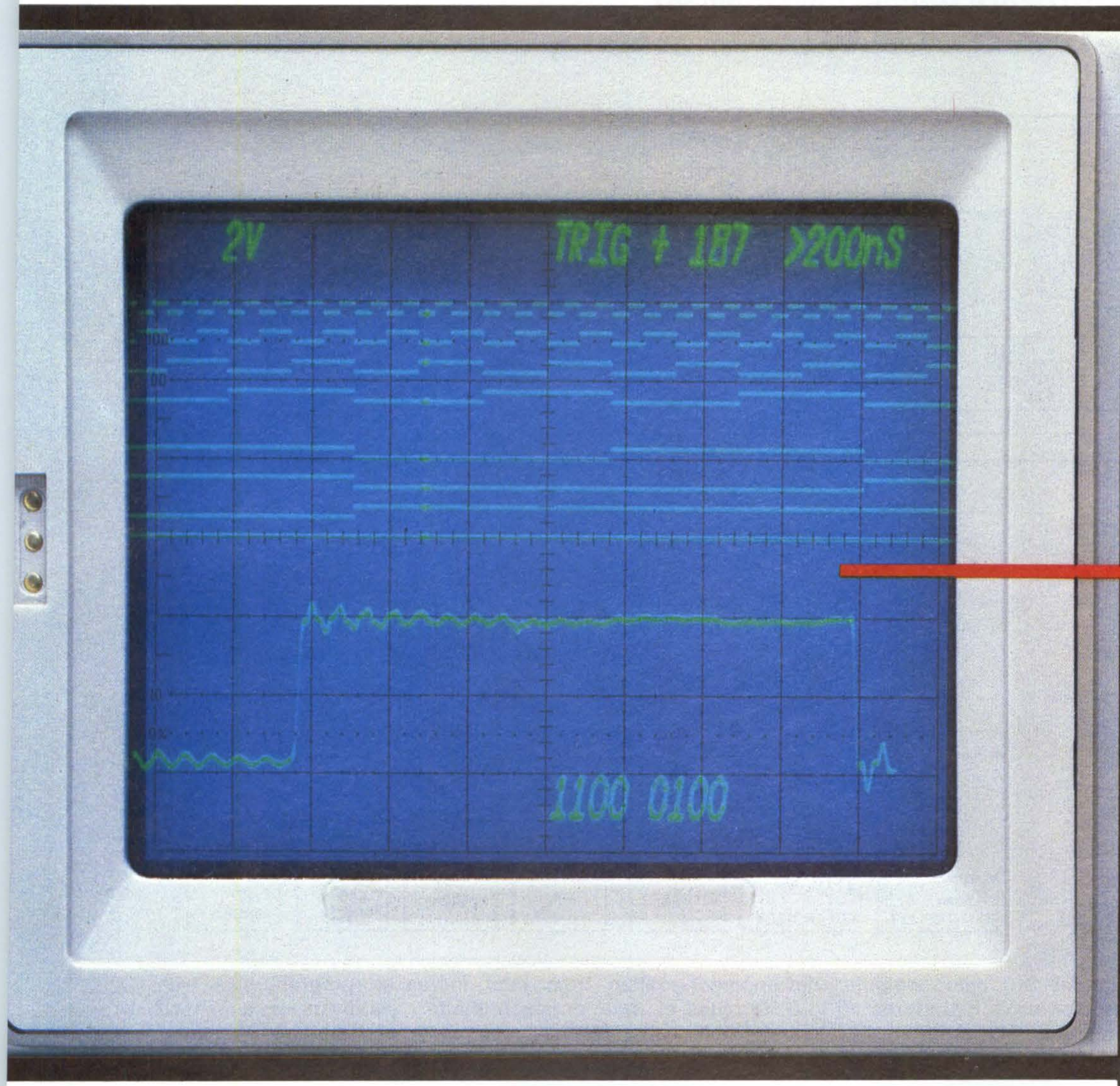
As stated earlier, most of the fundamental instructions (see listing of "Mnemonics For 6800 Instruction Set") can be used with several different addressing modes, bringing the total number of instructions to 197. These instructions can be separated into seven general categories: arithmetic, logic, data handling, data test, condition code, index register and stack pointer, and jump and branch. Many of the arithmetic, logic, data handling, and data test instructions can be used with either immediate, direct, extended, or indexed addressing. A few of the instruction capabilities are worth noting. The microprocessor has subroutine capabilities provided through the use of the jump to subroutine (JSR) and return from subroutine (RTS) instructions. Also, interrupts can be simulated, for hardware and software testing, through the use of the software interrupt (SWI). The decimal adjust accumulator (DAA) instruction allows you to perform arithmetic operations on binary coded decimal numbers directly, without any special conversion routines.* Hardware/interfacing aspects of the 6800 microprocessor will be discussed next month to develop a basic microcomputer system.

*For a more complete explanation of the 6800 instruction set and software techniques, consult *6800 Programming and Interfacing, with Experiments* by A. C. Staugaard (Howard W. Sams and Co, Indianapolis, Ind).

This article is based, with permission, on a column appearing in *American Laboratory* magazine.

# TEKTRONIX thinks your logic analyzer should be as versatile as you are

## So ours let you see analog and digital displays *at the same time.*




Verify logic and analog relationships at a glance

**D**igital troubleshooting usually involves two steps: First, logic analysis to find where the problem is located. Then analog measurement to pinpoint the source.

**T**ektronix 7000-Series Plug-Ins give you both steps. Presented together on the same display: a complete picture of the analog/digital relationship.

**M**any Tektronix 7000-Series Mainframes allow the 7D01 Logic Analyzer plus vertical amplifier and time base plug-ins to all be housed in a single mainframe. The same configuration gives you full analog *and* digital capability.

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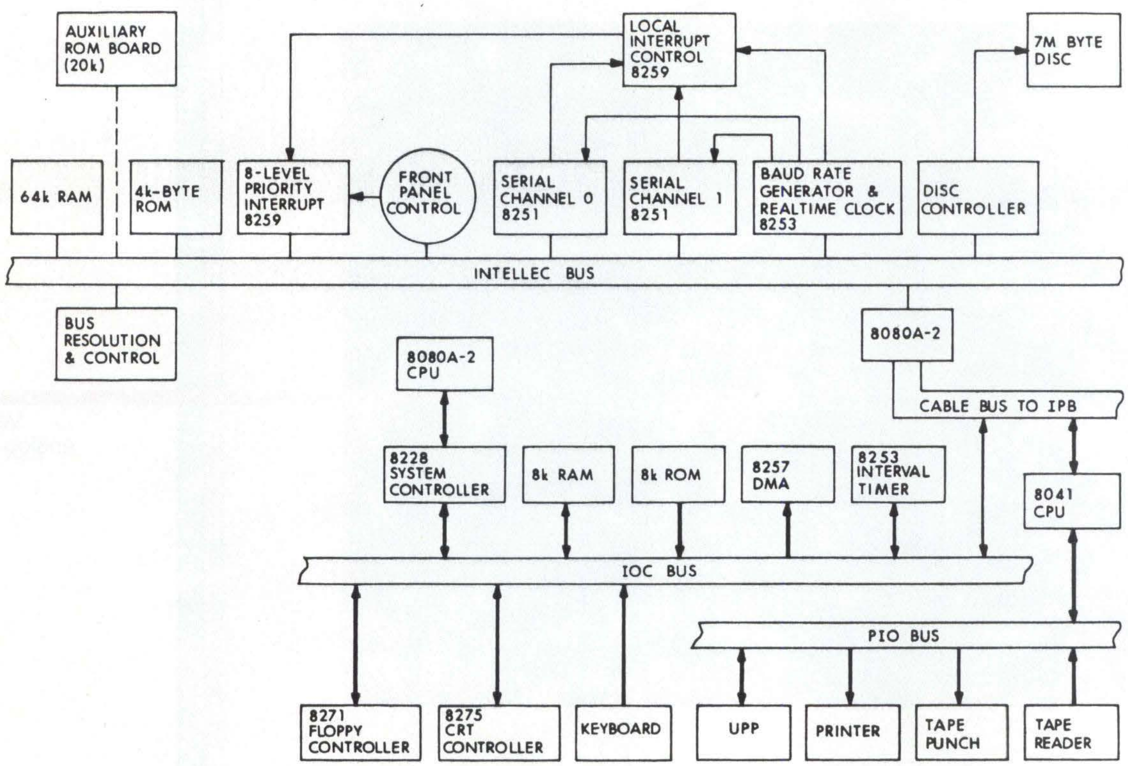
## Cartridge Disc and Software Double Development Performance and Increase Program Size




Intellec Series II model 240 microcomputer development system from Intel increases program size with addition of cartridge disc drive that stores up to 3.5M bytes of data on each platter. Hardware is enhanced by efficient software, enabling program development that uses 1M-byte capability of 16-bit 8086 microprocessor. Interface circuitry accepts standard peripherals through PIO bus

In response to the increase in use of 16-bit microprocessors which stretches the capabilities of current development systems, the Intellec® Series-II Model 240 gains speed, greater performance, and more program capacity through the combination of a cartridge disc drive and effective software. Faster than floppy disc subsystems, the cartridge drive contains a 5540 type fixed disc and a removable disc pack (to keep individual programs separate) for 3.5M bytes of data storage on each platter. The 250k-byte flexible disc drive offers convenient loading of programs into the development system; it is controlled by an Intel 8271 controller. Data are transferred between the disc and system by an 8257 DMA controller. Data transfer rate is 25M bits/s, contrasted to 160k bits/s for the Intellec flexible disc drive.

Overall performance of the development system is improved by the increase in the speed of the data interchange between the system's CPU and mass storage. Control circuitry, based on the series 3000 bipolar microcomputer chip set, resides on two PC boards that plug into the development system's MULTIBUS™ card cage. It can support two disc drives. The channel board receives, decodes, and responds to channel commands from the CPU in the development system. The interface board validates data during read operations by performing CRC polynomial error detection; during write operations, it generates CRC polynomials and appends them to the disc file.

The main CPU is the 8-bit 8080A-2, located on a board that sits in the first of six slots within the CRT chassis card cage. ROM firmware (4k bytes) stores system diagnostics and

# RAM Tamer

## Intel's new 8202 RAM controller makes dynamic memory behave like static.

Good news for microprocessor system designers. Now you can take advantage of the density and economies of dynamic memory with all the convenience and design simplicity of static RAMs. You'll reduce component count fourfold, cut power dissipation per bit tenfold or better and save money, too.

Just design in Intel's new single chip 8202 dynamic RAM controller. It unburdens the CPU of all refresh and address clocking and provides all bus multiplexing required to interface with 4K and 16K RAMs and Intel's 5V only 16K 2118, too.

**Another labor-saving device.**

Intel's family of 28 microprocessor peripheral devices all help designers avoid the time, cost and complexity of custom interface and control logic.

That's just what the 8202 does. It's a total solution; it handles all the arbitration, refresh and clocking required by dynamic memory and does it regardless of reset or DMA transfers and without asking the CPU to relinquish the bus. And it does all this with one 40-pin bipolar component.

Designers have always been attracted to dynamic memory for the highest density and power sensitive applications.

Now our 8086 16-bit microprocessor, able to address a full megabyte of memory, has created a new class of microcomputer applications where the traditional advantages of dynamic RAM look even more attractive.

**Performs all system control.**

The 8202 provides all system support needed to control and refresh up to 16K bytes of 4K

dynamic RAM or 64K bytes of 16K dynamic RAM in your 8085A systems. For 8086 systems, the 8202 output drives up to 128K bytes—as many as sixty-four 16K RAMs.

Failsafe refresh is assured. Internal refresh is done at the correct refresh rate for the specific memory device involved. Regardless of processor state, refresh takes place on schedule. External refresh—a CPU command to perform a refresh—permits synchronized or "hidden" refresh, too.

**Design flexibility.**

The 8202 interfaces directly to the 8080A bus, to the demultiplexed 8085A bus and to the demultiplexed 8086 bus. Eight 8202's can be grouped in an 8086 maximum mode system to provide control and addressing for a full megabyte of dynamic RAM.

To order any of the 28 Intel® peripheral interface and control components, contact your distributor. Or for more information on them and the 8202 dynamic RAM controller, write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051.

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**Circle No. 70 for information**

a monitor program. The 32k bytes of RAM resident on the CPU board is complemented by a board that contains 32k bytes of RAM for a total of 64k bytes of main memory. An 8-bit bidirectional data bus links the 2.6-MHz CPU to its slave processor. Support of the MULTIBUS architecture enables several bus masters (CPU and DMA devices) to share the bus and memory. Each bus master's associated priority level governs its bus accessibility and prevents contention situations.

The second 8080A-2 CPU, located on a separate board attached to the system's rear panel, controls I/O functions. This controller has 8k bytes of ROM I/O control firmware and 8k bytes of RAM for CRT screen refresh. Coupling of the development systems to standard peripherals enables the programmer, when satisfied with the program, to reproduce it in source code form (assembly or high level) as a printout, punched into paper tape, or stored in P/ROM in its machine language form.

The 12" (30-cm) CRT screen is formatted as 25 rows of 80 characters; the ASCII keyboard is detachable. Character information is stored in the I/O controller's RAM space and fed to the CRT's character generation circuitry during each complete scan of the screen by the electron beam.

Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, designed the system to support a number of microprocessors—among them, the 8049, 8080, 8085, and 8086—requiring large capacity program development. For the first time, Intel will be performing system setup and checkout at the user's site. The unit supports the latest release of 8086 family software and is especially useful for developing programs that use the 16-bit 8086's 1M-byte addressability. Also, all 8-bit support software for the MCS-80, -85, and -48 families work on the system. Existing Intellec software and user developed utilities run without change on the system's release of the ISIS.II operating system.

Several capabilities are handled by optional software. Used with the CRT, it allows the programmer to type lines of application code, view it, correct typographical errors, and move the code into the mass storage. Mass storage files can be scanned to find lines for deletion or movement. In addition, software converts assembly and high level language. Compilers are available for PL/M-80 and -86, FORTRAN, BASIC, and CIS-COBOL.

Circle 410 on Inquiry Card

## Hard Disc System For Microcomputers Stores 13.7M or 27.4M Bytes

Packaging more storage for microcomputers, the HDS-4000 consists of a Shugart fixed media disc drive, the company's intelligent controller with error correction, cabinet, cables, and power supply. The interface is via an 8-bit parallel port. Either the CP/M or OASIS operating system is available without modifications to existing programs.

The -4004 with 13.7M bytes of formatted capacity features two surfaces, four movable heads, and 808 tracks. In comparison, the -4008 handles 27.4M bytes, with four surfaces, eight movable heads, and 1616 tracks. Identical performance specs for the two versions are 202 cylinders, 17 sectors/track, 1024 bytes/sector, and 892k-byte/s drive transfer rate. Seek times are 20 ms track to track, 87 ms average, 220 ms max, and 10.1 ms average latency.

The disc controller includes error correction hardware that detects most errors and corrects up to a 6-bit error burst. With 32k bytes of buffer storage, the device can be microprogrammed to perform much of the file access overhead and reduce the host computer's computational load. The interface accommodates different host computers.

Digital Microsystems, 4448 Piedmont Ave, Oakland, CA 94611, has added a head per track storage option of eight fixed heads to the bottom surface, yielding 136k bytes of disc storage. The reduction of seek time on frequently accessed files or directories can improve throughput.

Circle 411 on Inquiry Card

## Microcomputer Switching Supply Performs Reliably In Severe Environments

Designed for airborne microprocessor systems, the 4-output power supply offers 5 Vdc at 15 A, 12 Vdc at 2 A, and −5 and −12 Vdc at 1 A for commercial and industrial OEM applications in hostile environments. CEA Div of Berkleonics, Inc, 1 Aerovista Pk, San Luis Obispo, CA 93401, has constructed the supply using an anodized aluminum heatsink plate, a circuit board with I/O connector, and a protective shielding cover. It plugs into the host computer chassis and is secured by tightening wedge-locks.

Optional 15-Vdc outputs can replace one or both of the 12-Vdc outputs. Each overcurrent and short circuit protected output features a Transzorb type device that provides overvoltage and reverse voltage protection to the supply and host system. Preset output voltages maintain a total regulation band within 3%, including the effects of variations in line voltage, load current (10% to full load), temperature (0 to 70 °C), and ripple/noise.

An ac input version is strappable at the I/O connector to accommodate 115- or 230-Vac, ±10%, single-phase, 47- to 440-Hz prime power. The dc input unit accepts 28 Vdc over an 18- to 31.5-V range. Application of a remote power switch signal or strapping of the internal thermal cutout signal effects supply shutdown.

Circle 412 on Inquiry Card

## Computer Maximizes Capabilities Using Floppy Disc Storage

As a large memory capacity, minifloppy based microcomputer, C4P MF is introduced as a powerful top of the line system at a price that is competitive with existing mid-range computer products. The standard model, claimed by Ohio Scientific, 1333 Chillicothe Rd, Aurora, OH 44202, to run at least twice as fast as competitive models, consists of a 2048-char display (32 x 64) with


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So if you want real support from an OEM drive supplier, look to the very first supplier of OEM drives; the supplier with the very latest in drives.

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For more information on our OEM drives, or to arrange for demonstration models, just contact your nearest Memorex sales office or distributor.

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**CIRCLE 71 ON INQUIRY CARD**

16 colors and an effective graphics resolution of 256 x 512 points, 24k static RAM, and a single floppy disc. The last two items are expandable to 48k and two floppy discs, respectively.

Faster operation—nearly doubled —is obtained with a limited production GT option. It uses the 6502C microprocessor together with ultrafast static memories to gain performances of 600 ns or less for memory to accumulator add time, 900 ns or less for jump extended, and 1.2M instructions/s for execution of typical applications programs.

For professional users, the 14-lb (6-kg) computer features full 64-char display width, line printer interface, modem interface, full keyboard with lower case, and advanced disc based software such as an information management system, word processor, and library of program development tools. Instant program loading, color graphics, high speed animation, sound output, a DAC for music and voice output, joystick interfaces, and a library of games, educational programs, and finance aids may be utilized by the personal user. Finally, for the home market, such features as a realtime clock, home control operating system with foreground/background operation, an ac remote control interface, and a home security and fire alarm interface are included.

Circle 413 on Inquiry Card

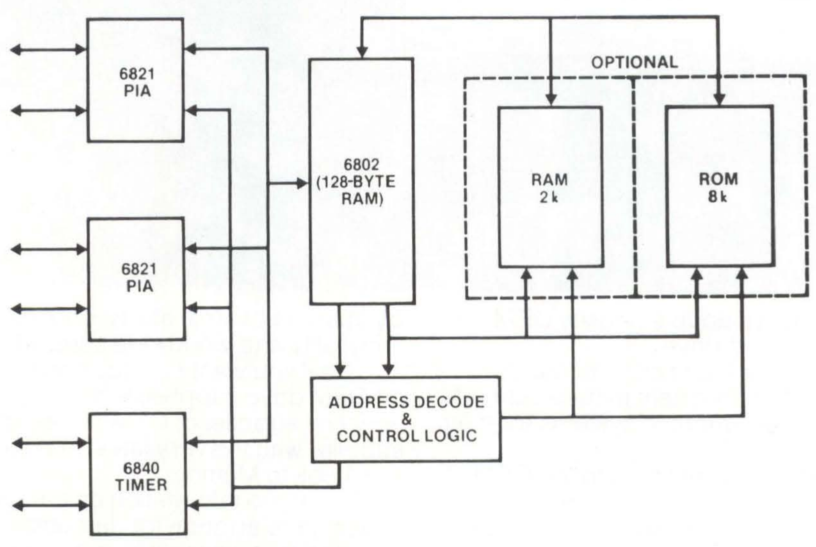
## Single-Board Computer Adapts Configurations to Process Control Uses

Module 1050 single-board microcomputer offers adaptable computing power for intelligent process control/monitoring applications on a 4.5 x 6.5" (11.4 x 16.5-cm) PC board. Required is 5 V ±5% at 500 mA. The design by Adaptive Science Corp, 4700 San Pablo Ave, Emeryville, CA 94608, uses the Motorola 6802 microprocessor which includes 128 bytes of RAM, operating at 1 MHz using an onboard crystal controlled clock. Component changes can increase this to 2 MHz. External interrupts are accommodated by eight control lines. An additional 2k bytes of RAM and 8k bytes of EPROM or P/ROM can be loaded into sockets on the board. Other P/ROM or EPROM types are available to bring the total module capacity to 16k bytes.

The unit receives 200 h of burn-in plus retest. Ceramic packaged LSI components are used. A 56-pin edge connector provides external communications for a typical configuration of three programmable 16-bit counter/timers and 32 bits of bidirectional parallel I/O.

In different configurations, either the three counters (all on a single IC) or 16 of the 32 bits of parallel I/O are omitted and replaced by a serial port (6850 ACIA). Serial information to and from the ACIA is TTL compatible and can be converted by means of off-module circuitry to meet RS-232-C, -422, or -423 specs. The baud rate, generated on the board, is selectable from 50 to 19.2k.

Circle 414 on Inquiry Card




Single board contains 6802 microprocessor with memory, logic, and sockets for additional memory to comprise Adaptive Science Corp's Model 1050. Alternative configurations replace three counters or 16 bits of parallel I/O with serial port option

## Bubble Memory System Adds Mass Storage to SBC-80 Microcomputers

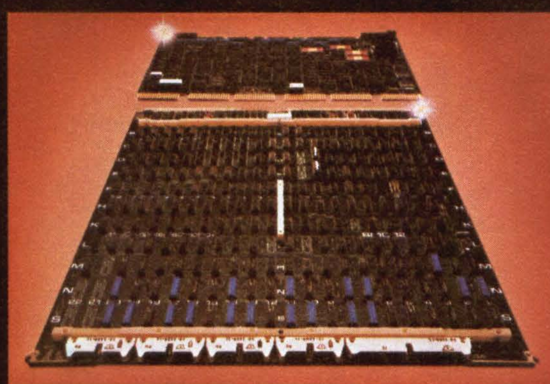
Environments requiring silent, long lasting memory with nonmoving mechanical parts can use the MBB-80 Bubbl-Board™, a single multilayer PC module that consumes one slot in the card cage for the Intel SBC-80 single-board microcomputer. Eight Texas Instruments type TIB0203 92k-bit bubble memory devices provide 92k bytes of nonvolatile storage (see *Computer Design*, July 1979, p 164). Included is all the required control logic and page buffering for interface to the Intel MULTIBUS™. As many modules as desired may be incorporated into a microcomputer system, and each can be removed and plugged into another computer. The Texas Instruments TMS-9916 device serves as the controller (see block diagram).

During a single-page write operation, the microcomputer first fills the controller's 18-byte FIFO memory

# MiniComputer Technology

The solid name in disk controllers
introduces two smart new single boards.
For DEC and Data General.

Above,
the SMC11 (DEC)



Below,
the SMC 12 (DG)

They're ready for delivery now. Intelligent storage module disk controllers with multi-drive capability, multiple sector transfer, and hardware error correction. They come complete with cables and manuals. For $3580, quantity one.

These controllers are substantial achievements. But then we've been making single board disk controllers for DEC, Data General, and Interdata systems for over four years. And more than three thousand trouble-free units are out there working now.

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Interdata people,
ask about the SMC903.

CIRCLE 72 ON INQUIRY CARD

by writing 18 bytes into a register in the controller. It next writes in the number of the 18-byte page that is to be written in the bubble memory device, and then sets the write-page bit in the controller's command register. The controller writes the data into the selected page and generates an interrupt when the operation is complete.

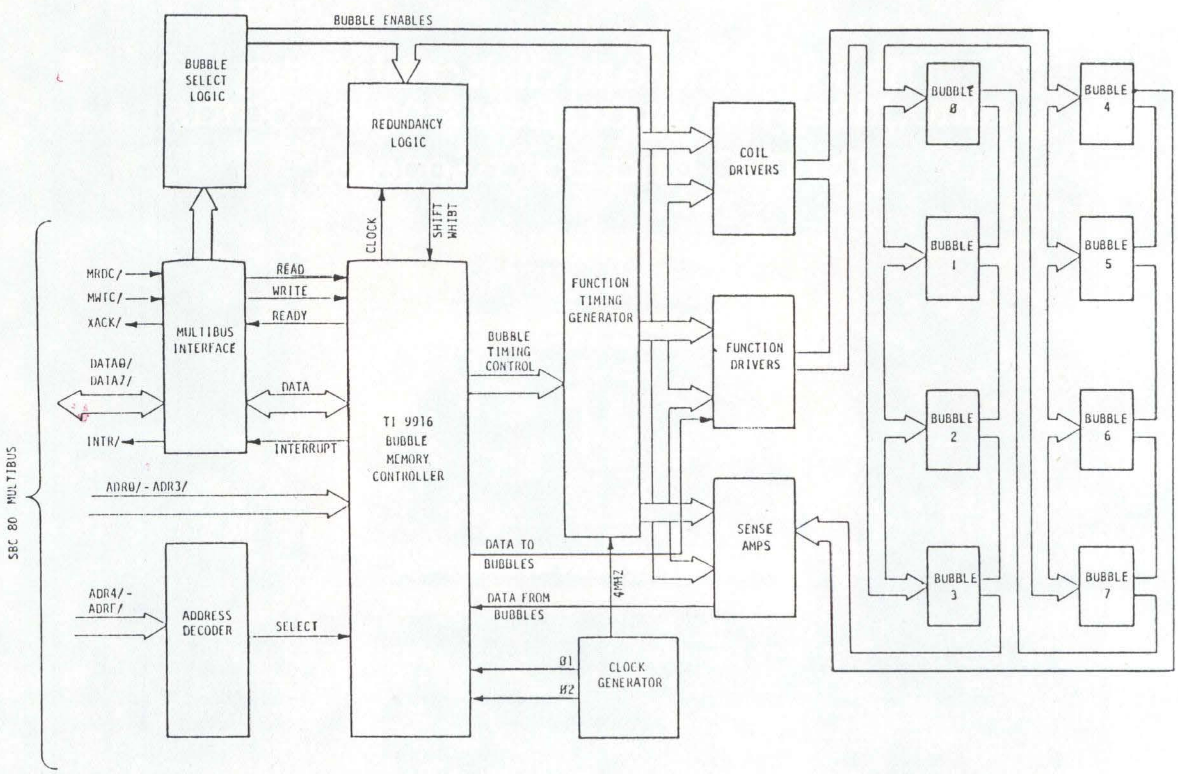
The single-page read is the inverse of the write operation. The microcomputer writes the page number into the controller's page number register and then sets the read-page bit in the command register. Once the page is read from the bubble memory, an interrupt is generated and the computer unloads the buffer by reading a controller register 18 times.

A multipage transfer mode also reads and writes larger blocks of data. The computer provides a starting page number and a page count to the controller. If it is a write operation, it loads the first byte into the FIFO and sets the multipage and read or write bits in the command register. An interrupt is generated each time the controller needs to transfer a data byte. When all pages are transferred, the controller busy bit in the status register is negated and the operation ends.

Power requirements are 5 V at 1.5 A, 12 V at 200 mA, and −12 V at 700 mA. Power consumption is less than 20 W. The power supply must have power-fail detect circuitry to insure that data are not lost during power-down. Onboard circuitry prevents data loss caused by transients during power-up and power-down.

The bubble devices are shifted at a 100-kHz rate. Since there are 641 page positions in a device, worst case seek time is 6.4 ms; average seek time is one-half of this maximum figure. Access time is 7.27 ms max to the first byte.

In single-page mode, the loops (157 minor loops, similar to shift registers, comprising each bubble device) are returned to page zero when the transfer is complete. To transfer a page of data between the bubble




Bubble memory controller in SBC-80 BUBBL-MACHINE is connected to MULTIBUS through interface that responds when any of 16 consecutive memory locations are addressed. Within address decoder, 12 MSBs are selected, so user may place controller anywhere in microcomputer's address space. Bubble-Tec's computer designates which of eight bubble devices will be accessed during subsequent controller operations

device and controller takes 1282 shifts or 12.82 ms at the 100-kHz rate (this, however, includes the seek time). The effective transfer rate of several pages of data is determined by dividing the 144 valid bits/page by the 1282 required shifts, and multiplying by the 100-kHz shift rate. This results in a transfer rate of about 11k bits/s.

Multipage mode improves this rate considerably. Generation or detection is essentially continuous after accessing the first page of data, so that the transfer rate of greater than 45k bits/s is determined by dividing the number of valid data bits/page (144) by the total number of bit positions in a page (157) and multiplying by the 50-kHz data shift rate.

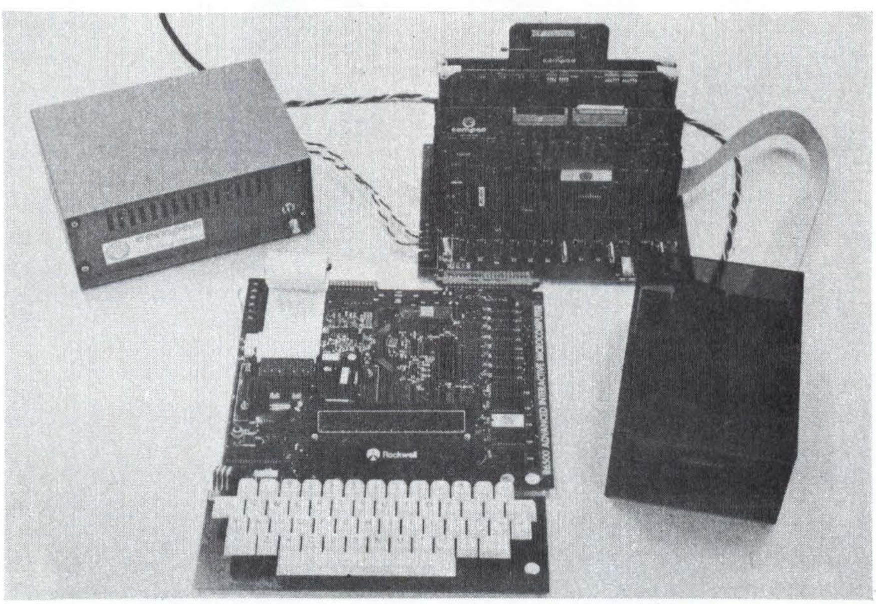
Bubble-Tec Div of PC/M, Inc, 3120 Crow Canyon Rd, San Ramon, CA 94583, includes software and documentation in the single-quantity price of $1695. This comprises installation procedures, maintenance and diagnostic routines, and example simplified device drivers, with suggested soft-error protection scheme, for user systems. **Circle 415 on Inquiry Card**

## Operating System Software Resides in EPROM Chips On Floppy Disc Controller

DAIM is a complete minifloppy disc system for the Rockwell International AIM 65. Components are a floppy disc controller, power supply, and one (or two) floppy disc drives. Compas Microsystems, a div of Computer Applications Corp, 224 SE 16th St, Ames, IA 50010, intends the controller board to be used with the Rockwell expansion motherboard which features the SYSTEM 65 bus standard.

With all of the features of the SYSTEM 65 operating system, the disc operating system software resides in EPROM chips mounted on the controller board. Discs written on either the DAIM system or SYSTEM 65 are interchangeable. Disc capabilities include load and save source and object files, initialize a disc, zero a disc directory, list a file, list a disc directory, rename files, delete and recover files, and compress a disc to recover unused space. All commands are identical to those that are used on the SYSTEM 65.

The power supply is adequate for two disc drives and the controller board. The disc mounts in a plastic enclosure to protect the drive while allowing the user to watch internal operation. The system's base price is $850; an additional drive is $350.
**Circle 416 on Inquiry Card**



DAIM floppy disc system from Compas Microsystems attaches to Rockwell's AIM 65 computer, forming the basis of low cost 6500 microcomputer development system

## MULTIBUS/Z80A Based Microcomputer Packs Added I/O Power

Three serial ports and one parallel port allow the MSC8007 single-board computer to link to such peripherals as a CRT terminal, line printer, communication link, and 24 programmable parallel lines. The number of boards in a system can be reduced from three or more to a single card. Fully compatible with the Intel MULTIBUS™, the computer uses the Zilog Z80A as the CPU. Monolithic Systems Corp, 14 Inverness Dr E, Englewood, CO 80112, further enhances the unit with the addition of the AM9511A 32-bit floating point arithmetic processing unit. Thus, arithmetic and transcendental functions as well as control and conversion commands are performed at higher speeds than comparable software techniques and do not take up memory space to store the routines. This processor operates concurrently with the CPU and can interrupt the CPU when terminating an operation.

Maximum RAM is 32k bytes. EPROM is compatible with standard 1k-, 2k-, and 4k-byte devices for a maximum of 16k bytes. The dual-ported feature allows simultaneous access by both the CPU and an external device. Also included are automatic onboard refresh control and memory mapping with either standard or user defined address maps. Commercially available 8080 and Z80 software packages such as CPM™ can therefore be used. A dual map is optional.

Operation of the board is in multimaster mode with either parallel or serial priority resolution. Up to 16 bus masters can share the MULTIBUS. Programming one of three bus modes lets the user exchange the bus master every cycle, every instruction, or when required at the end of a software routine. Current and asynchronous operations can be carried out on both an internal bus and the MULTIBUS when the CPU uses local memory and I/O devices.

Eight levels of priority interrupt vectoring, plus a nonmaskable interrupt to deal with system power failures or to evaluate hardware and software problems, is also provided. Each serial port on the computer includes a bidirectional USART, drivers, and an I/O connector.

Other features are a standard 16-MHz master clock and independent system timing functions such as power up, initialization, and a watchdog timer for evaluation and detection of such program and system problems


# Almost perfect.

Our new ADM-42 doesn't have quite everything. But it comes so close, you might never notice.

Because it's a complete, semi-intelligent terminal for just about any application you can name. And it does just what you want it to do, just when you want it done.

The ADM-42 is completely self-contained, and provides you with flexibility of format, security, editing, interface, and transmission. It also features a full two-page display as standard equipment. Not as an option. And it comes with a truly staggering array of options.

### THE MORE YOU USE IT, THE SMARTER IT SEEMS.

We gave the ADM-42 a bright, easy-to-read 2000 character display. A full 128 ASCII character set. 16 function keys for 32 separate commands. And five separate cursor control keys.

The 42's behavior modification gives you a factory installed personality for an alternative ESC sequence lead-in—in addition to the standard ESC. And End Block character. A New Line character sequence. A field separator. And even a function sequence preamble.

Its status displays on the screen give you a conveniently wide range of information at a glance. While its special symbols indicate the entry of control characters in memory. Also, all control characters can be stored using the escape sequence or program mode. And the Field Protect Mode allows rapid data entry into forms or instruction pages.

### THE ADM-42 WILL HAND YOU ANOTHER LINE.

The terminal's displayed data is formatted in 24 lines per page, 80 characters per line. And, to top it off, it comes with a 25th line established and reserved exclusively for status indicators and messages of up to 79 characters.

As if all this weren't enough, the ADM-42 has an impressive list of options. Like synchronous transmission with various line protocols. An extended memory capable of adding data space up to a maximum of 8 pages. And programmable function keys, to name but a few.

### THE ADM-42 IS ONE TOUGH ACT TO FOLLOW.

The ADM-42 has just about everything. Including a microprocessor that increases reliability and ease of operation. Any way you look at it, in fact, it's one pretty smart buy.

So if you're thinking of upgrading to a more intelligent terminal, at a more than reasonable price, call us today. Or better yet, contact your local distributor.

We'll show you how easy it is to move up to the ADM-42.

The terminal that's so smart, you'll swear it's got a mind of its own.

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**CIRCLE 74 ON INQUIRY CARD**

For the past several months, Advanced Micro Devices has been publishing an advanced course in microprogrammable microprocessing. This discussion ends the series.

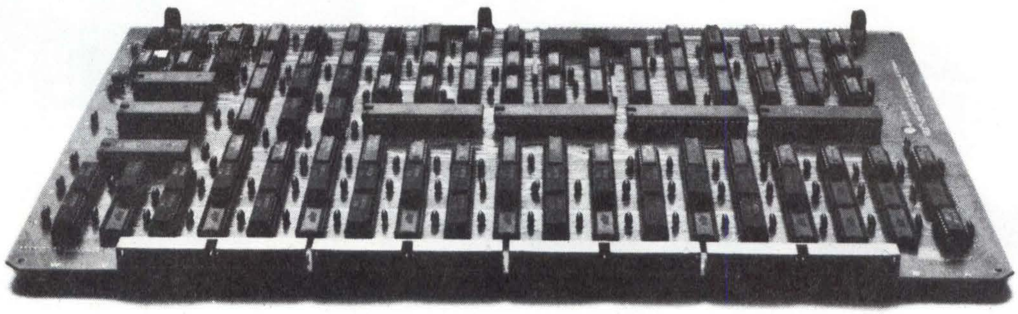
Our goal was to show you how to build a fast, microprogrammed machine. It had to have the processing power of an expensive computer without the cost. It had to have a design you could customize to your own needs. And it couldn't require a room full of parts. Here's how it came out:

## CHAPTER 8: THE BASIC 16-BIT MICROPROGRAMMED MACHINE.

It's your basic miracle.

This machine has a register-to-register cycle time of 320ns. It has an absolutely straight-forward architecture. It's easy to modify and easy to understand. And it comes with the complete microcode for 90, count 'em, 90 instructions.

Look a little closer and you'll see that we've done 90% of the design work for you.



The HEX-29. A commercially available computer based on the design in Chapter 8.

# BUILDING A MICROCOMPUTER, CONCLUDED.

After you figure the time and money you'll save, you still have to get used to the idea of skipping all that dirty work.

## THE DELUXE MACHINE.

Some people can't leave well enough alone, and you may be one of them. For you, Chapter 9.

It describes a 16-bit microcomputer with unheard of power and performance. This machine has an advanced architecture with overlapped instruction fetch, a unique high-speed synchronous bus, and a register-to-register execution time of 200ns.

Basic or deluxe, send for the information. With the running start it will give you, you'll be well on your way to building your very own microprogrammed machine. And that, after all, is what this series has been all about.

## BUILDING YOUR LIBRARY, CONCLUDED.

With Chapters Eight and Nine on the Basic and Deluxe microcomputers, you can have yourself a ton of theory and applications information. If you're not already on our mailing list, send in the coupon and we'll send you the whole book.

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as referencing to nonexistent memory or I/O devices. Power requirements are ±5 and ±12 V. It is priced at $1860. The company's 8301 monitor and 8303 operating system, editor, and assembler comprise the software support.
Circle 417 on Inquiry Card

### Effective Interfacing Is Design Rationale Behind Microcomputer

Code 64 features a 17 x 16.5" (43 x 42-cm) single-board format that may be user populated to achieve economical solutions to industrial control tasks. With 12 serial data channels, 12 parallel data channels, and 16 cascadable channels of event counter or realtime clock, the computer achieves realtime interrupt driven I/O. Computer Design Consultants, 1804 Dexter St, Broomfield, CO 80020, has coupled this capability with integral vectored interrupt and DMA structure, and supplied software support as well.

Based on the 4-MHz Z80 CPU, the computer has four separate channels of DMA, 16k of ROM, 64k of RAM with parity protection and dual independent floppy disc data channels. The dual floppy discs transfer data in IBM 3740 format.

In view of interfacing considerations, serial and parallel channels may be tailored with level translating, buffering, or special function personality cards (20-mA loop or RS-232-C), ranging from relay or lamp drivers to ADCs or P/ROM programmers. A library of public domain software is already written for the Z80 microprocessor. Floppy disc file manipulation is possible with the Digital Research Corp CP/M disc operating system. In addition, applications packages, software development and debugging tools, and high level languages can be obtained from Digital Research Corp, Microsoft, and other software development firms.

Five levels of the computer provide increasingly more powerful versions. At the basic level, without floppy disc drives, it can run extensive dedicated programming from ROM storage. Equipped with personality cards, it can monitor, control, and log processes (including remote locations or hazardous environments). High end use is as a software development system. Serial data channels adapt it to use as computer networks for distributed processing, as well as message preprocessors or peripheral controllers for a larger computer.
Circle 418 on Inquiry Card

### Software Command Modules Ease Operation Of Home Computer System

The TI-99/4 computer is comprised of a 16-bit 9900 microprocessor, 16k of RAM, a 9918 video display processor, and a 9919 sound generator. The console unit uses 16 colors for graphic display on a 13" (33-cm) video monitor. Texas Instruments, Inc, Consumer Relations, PO Box 53, Lubbock, TX 79408, has equipped the computer with an extended BASIC programming language; in addition, Solid State Software™ command modules serve as ready-made computer programs. Suggested retail prices are $1150 for the system and from $19.95 to $69.95 for the modules.

TI BASIC is a full floating point, 13-digit expanded BASIC, compatible with ASCII and the ANSI specification. It includes 24 BASIC statements, 14 commands, color graphics, and sound and music over four full octaves. A self-teaching beginner's BASIC guide is included.

The compact, rugged command modules each contain up to five ROM chips of stored data. The user instantly accesses specific functions by snapping in the module and pressing a few keys. Among the categories are personal finance, home management, education, and entertainment.

The Solid State Speech™ synthesizer is available for $150 as an accessory. This plug-in module has a 200-word vocabulary. Using BASIC, the user can write speech into programs. Future command modules will call up spoken words automatically.

Other accessories are remote controls, two of which may be connected to the computer at the same time. Each has a multiposition (360°) rotary lever with side mounted "fire" button. Peripherals to be introduced later are a printer, disc memory, and RS-232 interface device.
Circle 419 on Inquiry Card

### Combination Analog I/O Card Features Monolithic Data Converters

The RTI-1225 STD-BUS compatible analog subsystem combines input and output functions on a single 4.5 x 6.5" (11.4 x 16.5-cm) board. Microcomputers from Mostek and Pro-Log use the STD-BUS. Priced at $399 in quantities of one to nine, the card has an output that is compatible with the bus, and operates from the microcomputer's 5-V supply. (Power requirements are 5 V at 750 mA.)

Analog Devices, Inc, PO Box 280, Rt 1 Industrial Pk, Norwood, MA 02062, has included monolithic data converters throughout. This, together with a 1 x 2 x 0.4" (3 x 5 x 1-cm) dc-dc converter, has enabled the inclusion of 16 single-ended analog input channels and two analog output channels.

The input channels offer ±35-V input overvoltage protection and can be configured in differential mode. Input ranges are 0 to 10, ±5, and ±10 V; common mode rejection ratio is 60 dB min at 60 Hz. The input section of the 10-bit monolithic IIL ADC requires 40 μs to settle from a 20-V swing plus the A-D conversion. Other specs are guaranteed monotonicity from 0 to 50 °C, overall system error specified at ±0.15% of full-scale range, and gain and offset errors adjustable to zero.

Analog outputs are derived from two 8-bit DACs and output amplifiers, which settle to ±½ LSB in 30 μs for a 20-V step. With nonlinearity guaranteed to be ±½ LSB max, outputs range from 0 to 10, ±5, and ±10 V; output current is 5 mA at ±10 V.
Circle 420 on Inquiry Card

### Disc Storage and CRT Attachments Upgrade Desktop Microsystem

Enhancements to the PCC 2000 expand its capabilities beyond those of the original configuration, providing functionality of larger systems to companies which have outgrown the original system, as well as to those with large data bases requiring computer to computer communications. Users can expand peripheral disc capacity by up to 40M bytes of rigid

# Vision One/20

image processing by

**COMTAL®**

*The Versatile "YES" Machine*


Professional talk about the most sophisticated digital image exploitation equipment always mentions the leader, COMTAL. ☐ **YES**, and that includes the Vision One/20 with its unique features backed by the experience gained in developing superior image processing systems. ☐ **YES**, Vision One/20 has an exclusive 12K firmware operating system and up to 48 megabytes of dynamically allocatable refresh image memory and graphics. ☐ **YES**, field upgradeability through options such as expandable memory, video input and output, as well as TV rates for videotaping. COMTAL's "**YES**" system requires a minimum of training for effective utilization. Other options such as magnetic tape and disc storage are available. Specialized image processing hardware is available for image arithmetic combination, convolution, Landsat classification, plus small area color correction, and all function in real-time, in 1/30 second. ☐ **YES**, all this—in a system that can accommodate future growth as application requirements expand. Multiple user capability, up to 4 work stations, offers resource sharing. ☐ **YES**, with COMTAL's leadership pacing the state-of-the-art, it adds up to flexibility now—and flexibility later. ☐ **YES**, Vision One/20 image processing systems have dual-ported random access memories starting at 512x512 pixels at multiples of 4 bits of brightness depth, with growth up to 4096x4096-24 bit pixels. ☐ **YES**, random access refresh memories are constantly growing in size and shrinking in cost. Digital image rotation is a reality now. ☐ **YES**, a 24 bit x 24 bit color computer is available for image composition, as is independent arbitrarily shaped small area processing capability in monochrome and color. There's high resolution digital stereo and instantaneous—1/30th second—convolution for filtering. Or, bigger filters exist by recursively iterating and updating kernels 30 times/sec. ☐ **YES**, Vision One/20 provides stand-alone full feature image processing as well as the ability to interface to numerous host computers. ☐ **YES**, dynamic refresh memory partitioning allows for different applications. ☐ **YES**, real-time roaming, with window sizes 512x512 pixels or larger, through the data base, as well as 2X and 4X zooming and 3x3 convolution at 70 MIPS—all implementable in real-time. Ask about the future of image processing from the company with renowned research experts, hardware experts, firmware experts and software experts. COMTAL's field service offices on the East and West coasts are there to help users. ☐ **YES**, successful sales representation worldwide as COMTAL triples its present production capacity in new facilities.


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**CIRCLE 75 ON INQUIRY CARD**

disc mass storage and attach up to four more CRT terminals. Pertec Computer Corp, Computer Systems Div, 20630 Nordoff St, Chatsworth, CA 91311, offers the upgrades as additions to existing customer sites or as part of new small business systems.

Four 10M-byte fixed disc drives and a hard disc controller add to the 1.2M bytes of floppy disc that are built into the system. The hard drives can access data in large files and operate system software and applications programs faster, freeing the floppy discs for backup of system software, data exchange, and storage of smaller data files. A data transfer utility is used with the floppy discs to back up and restore data files on the hard disc. Factory installation of the disc platters minimize contamination of the disc surface, which is considered to be a main cause of disc failure. Containing a microprocessor, the controller plugs into the system's P-100 bus. It transfers data via DMA at an increased speed of 750k bytes/s.

Addition of CRT terminals allows five terminals to run BASIC programs concurrently, supported by the Multi-Terminal Executive (MTX) operating system that operates within the 64k bytes of standard main memory. CRT screen formatting commands, report generation commands, and special disc storage capabilities with keyed disc files facilitate business programming.

Circle 421 on Inquiry Card

## Converter Acts As Translator Between I/O and Computer Buses

Two I/O bus converters, constructed on 6.75 x 12" (17 x 30-cm) cards that require only one card slot in an SBC chassis, connect the line of RTP analog and digital I/O controllers to the Intel SBC 80 and 86 single-board MULTIBUS computer systems. These translators between the Intel MULTIBUS and RTP I/O bus use IN and OUT instructions, and are transparent to data transfers to or from the attached subsystem so that the subsystem appears to be directly connected to the MULTIBUS. In addition, the SBC 80 converter performs the necessary byte/word conversion between the 8-bit computer and the 16-bit subsystems.

Operating modes are programmed I/O and interrupt driven (with no DMA capability). Four sequential addresses are required for the I/O bus converter and each attached RTP controller. Address mode for the RTP/7410/68 (the SBC 86) is device I/O; for the 7410/67 (SBC 80) the modes are device I/O (standard) and memory mapped (user selectable). In the device I/O mode for the /68 and memory mapped mode for the /67, the upper eight address bits are jumper selected on the bus converter card and the next six address bits are switch selected on each device. In all modes, the lowest two bits select the specific functional register within the device.

Up to eight subsystems from Computer Products, Inc, 1400 NW 70th St, Fort Lauderdale, FL 33307, can be attached to either converter. All controllers can generate interrupt requests over a common line to the bus converter which interfaces into the MULTIBUS structure. Priority is determined by the proximity of a controller to the bus converter on the RTP I/O bus; the highest priority device responds to a CPU query with its address as an identifier.

Circle 422 on Inquiry Card

## Low Cost Unit Supplies Regulated Output to Power SBC Boards

Equivalent to the Intel SBC635, the IPS 635 power supply provides regulated dc output at ±12 and ±5 V. Full ratings from 0 to 55 °C produces power levels for Intel single-board computers loaded with I/O line terminators and drivers, and four 8708 EPROMS, with extra capability for combinations of up to three Intel SBC-80 memory I/O or combination expansion boards. Elpac Power systems, div of Elpac Electronics Inc, 3131 S Standard Ave, Santa Ana, CA 92705, has designed the pin for pin interchangeable supply with current limiting, overvoltage protection, and logic signals that sense a system ac power failure. The unit generates a TTL signal for power-down control.

Circle 423 on Inquiry Card

# DIGI-DATA SERIES 40

## the more OEMs demand of tape systems, the more we deliver.

OEMs are demanding. They want different models for different applications, the highest possible reliability, and value that reflects in their final product. Our Series 40 continues the 17 year Digi-Data tradition of satisfying these OEM requirements.

### More Selection

Within our Series 40 family, they can choose from 192 combinations of NRZI, PE and NRZI/PE models with reel sizes from 7 to 10.5 inches and speeds from 12.5 to 75 ips — all featuring a new control block with more functions, such as a density select switch and an optional unit select switch.

### More Reliability in a Simpler Package

Microprocessor controlled imbedded formatter improves reliability by reducing chip count as much as 50%. All versions occupy a single board, simplifying cabling and reducing spares requirements, while eliminating the need for separate outrigger housings. Improved transport modularity facilitates field upgrading, particularly data density and tape speed.

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SOFTWARE

## Microcomputer Emulator Configures Itself To Specific Terminals

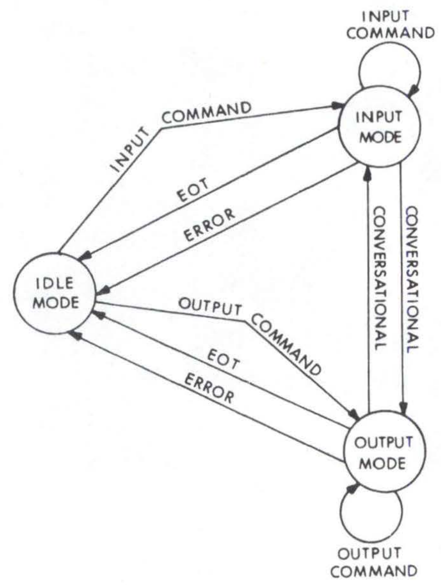
Intel and Zilog microcomputers running under CP/M may now use the universal binary synchronous emulator, known as the Remote Batch Terminal Emulator (RBTE), to emulate binary synchronous terminals such as the IBM 2780, 2770, 3741, and 3780. The minimum hardware/software system configuration must include a floppy disc system with file management software, synchronous RS-232 interface, and realtime clock.

These terminals are supported by dynamic configuration of the RBTE. Each supported terminal has a file containing 13 configuration parameters which are set to define a specific terminal. The four terminals can be varied to define new terminals without reprogramming.

The emulator consists of two main modules that are a bisync driver which performs all protocol handshaking and a terminal emulator which formats the transmission blocks. A diagnostic port feature of the emulator displays the bisync framing characters on a local CRT, allowing the user to diagnose communication problems without expensive line analyzers.

In operation, this FORTRAN program reads disc records from a CP/M file, reformats them into a bisync block, and transmits them to a remote terminal. Alternatively, a bisync block can be received from the remote terminal, unpacked into disc records, and written to the specified CP/M file. This standalone program sends or receives data files to and from a CP/M disc and communication port.

The bisync communication driver software package allows an application program to communicate directly to the bisync communication ports with simple open, close, read, write, connect, and disconnect commands. The I/O commands make the protocol mostly transparent to the user. The product has the same features as the RBTE, but it requires that the user pack or unpack the bisync block.




Bisync communication driver state transition diagram. From Winterhalter & Associates, software package emulates bisynchronous protocol, using I/O commands to send and receive data to and from remote terminals. Three modes—idle, input, and output—are interrelated

The driver may be in one of three states (see Figure). In idle mode there is no input or output activity present and no input or output commands queued. When either command is queued, a transition is made to that state. In input mode, data are being received from the remote terminal. Output mode becomes active if a conversational reply is sent to the last data message; data are sent to the remote terminal during output mode. Again, input mode becomes active if a conversational reply follows the last buffer in a data message. Both of these modes return to idle when an end of transmission (EOT) message is received or an error is detected.

Winterhalter & Associates, Inc, 3825 N Zeeb Rd, Dexter, MI 48130, plans to offer emulations for the IBM 3270, SDLC, DDCMP, HASP workstation, and X.25 protocols. A serial protocol processor will be released in the fourth quarter. This S-100 bus, microprocessor communications controller with four RS-232 serial ports is capable of communicating asynchronously, byte synchronously, and bit synchronously to the RS-232 ports. Its components are an 8k/32k P/ROM, baud rate generators, realtime clock, 4k/16k of dynamic RAM, and Zilog Z80 computer. It interfaces to the S-100 bus via bidirectional 124-character FIFO buffers.

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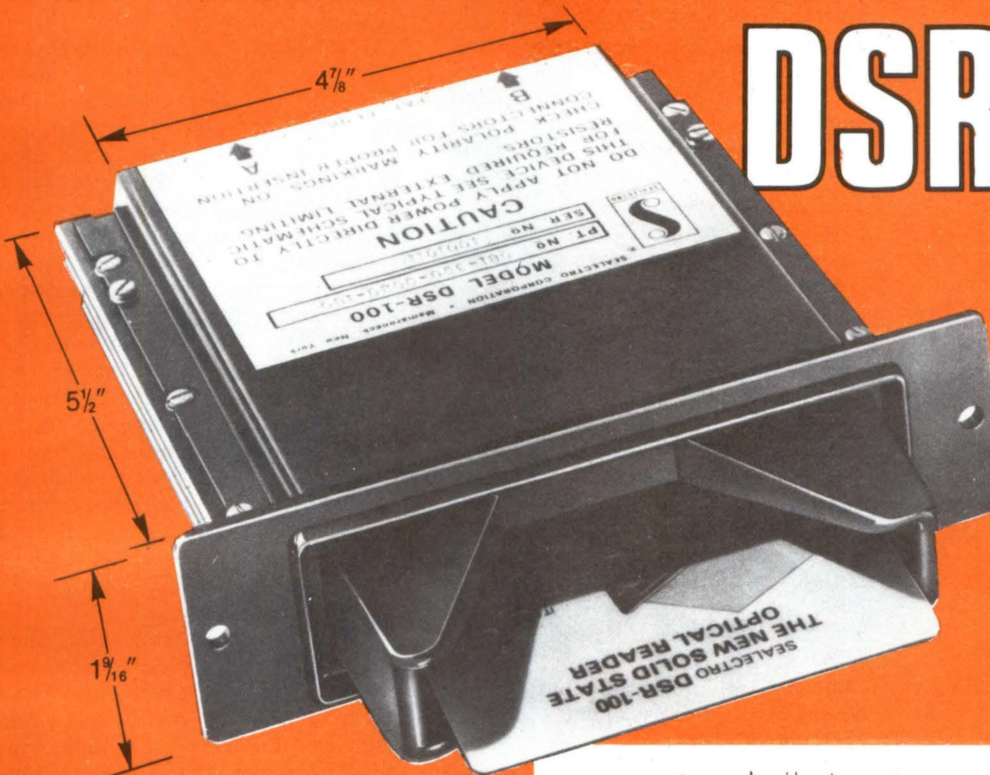


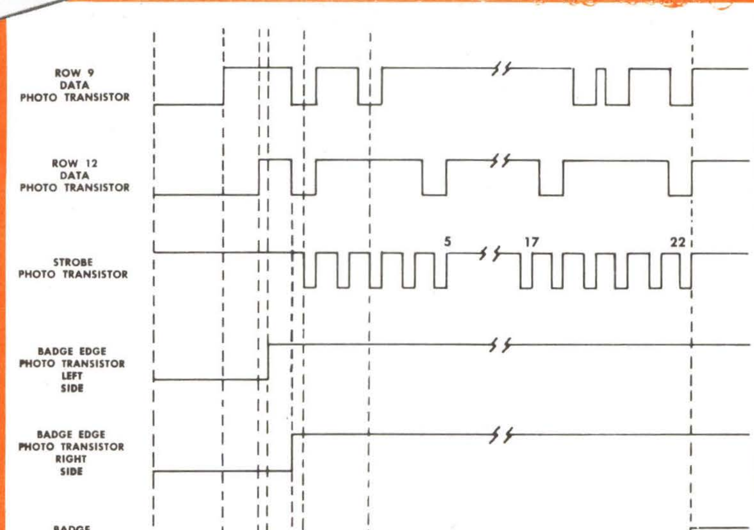


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## 3-Step Procedure Results In Structured Pascal Programs in Less Time

Z80 Pascal for microcomputer and development systems offers structured programming of business, educational, and scientific data. A set of disc based programs compatible with the RIO operating system, these programs are implemented in three steps: using a compiler, post-processor, and interpreter. The compiler accepts a program and produces an intermediate code file and a listing file indicating any compilation errors. The post-processor translates the intermediate (P-) code into a compressed object module for input to the interpreter, which in turn interprets and dynamically allocates space (for optimum usage) for the Pascal heap and stack through the RIO memory manager.

Although the language, as designed by Zilog, Inc, 10340 Bubb Rd, Cupertino, CA 95014, closely adheres to the specifications in Jansen and Wirth's *PASCAL User's Manual and Report,* it adds several extensions. A new standard procedure TRAP permits calling of external user defined assembly language routines, while a standard procedure EXIT allows termination of the program from anywhere within it. In addition, a constant subrange designator may be used instead of enumerating all values in a set constructor, and the tag field may be omitted in a case variant record.

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## Resident High Level Language Operates On 16-Bit Microprocessor

A version of BASIC, in use in Z80 and 8080 systems, has been released by Microsoft, 10800 NE 8th, Suite 819, Bellevue, WA 98004, for the 8086 16-bit microprocessor. It supports the language's standard features of double precision arithmetic, trace facilities, full PRINT USING, nested if/then/else, error trapping, renumbering, and edit mode. Dynamic string space allocation, variable names up to 40 char in length, and WHILE/WEND, CHAIN, and COMMON statements to link programs and share variables have been added.

Besides meeting all qualifications of the ANSI subset standard for the language, BASIC-86 is language compatible with the company's standard 8080 BASIC, release 5.0. Programs can be upgraded from use on the 8080 to the 8086 without modification. Both the extended and standalone disc versions operate on the Intel SBC 86/12.

Circle 426 on Inquiry Card

## 6800 Cross-Software Products Permit More Efficient Programming

Special versions of the Motorola 6800 cross-software have been released by Wintek Corp, 902 N Ninth St, Lafayette, IN 47904, for use on Digital Equipment Corp's PDP-11/03 systems (see *Computer Design,* Oct 78, p 179). The five products are offered on floppy discs for use with the RT-11 operating system. The PDP-11 V03 or the machine independent versions are available in ANSI X3.9 1966 FORTRAN.

The diskettes contain both the FORTRAN source and the compiled, ready to run object code files. Both the PL/W high level language compiler (PL/W is styled after IBM's PL/1) and the 6800/6801 cross assembler produce relocatable object code to facilitate rapid software development and to allow production of software libraries. Handling logical expressions efficiently, the compiler checks for constant subexpressions, special constants in various arithmetic contexts, and expressions containing redundant subexpressions. It automatically distinguishes between variables and program code/constants. A common package of storage management routines handles all internal compiler tables. Output consists of a program listing and a relocatable text file.

The 2-pass cross assembler, allowing free format input, detects 30 syntax errors and recognizes hexadecimal, decimal, octal, binary, and ASCII constants. It runs in both standalone and relocating modes. Three files that are produced are an assembly listing, an image of the executable binary in the same format as Motorola's software and firmware, and the hardware definition file.

The simulator allows free format input of commands, definition and expansion of command macros, partial simulation of ACIA and PIA devices, and partitioning of simulated memory into separate segments of ROM, RAM, and nonexistent memory. A special feature allows for the conditional interruption of simulation if several program faults are detected.

The final two products are a PL/W floating point/scientific function package and a 6800 relocatable linking loader. The latter produces a load map showing where each object module is located in memory along with addresses of global symbols. Absolute object code produced is a coded file in Motorola's MIKBUG format; it can be loaded into the 6800 hardware or the company's simulator. Hardware requirements for the instructions include 28k words of memory, EIS/FIS instructions (required for PL/W only), and a dual floppy disc drive.

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See page 112

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# IIL GATE ARRAYS MAKE CUSTOM ICS ECONOMICALLY FEASIBLE

**William D. O'Neil**

Exar Integrated Systems Incorporated
Sunnyvale, California

Semicustom monolithic LSI design uses a partially fabricated silicon wafer which is then "customized" by application of one or more special mask patterns. This technique greatly reduces design and tooling cost and time required for the prototype fabrication cycle in conventional full custom IC development. It thus makes custom ICs economically feasible for development and for low volume production.

To be economically feasible, a complex digital LSI chip must have a high functional density (ie, high gate count per unit chip area). Traditionally this requirement has not been compatible with the random interconnection concept integral to the semicustom or master-slice design approach.

However, an additional approach now solves this problem by achieving packing densities nearing those of full custom digital LSI layout while maintaining the low cost and quick turnaround advantages of semicustom IC design. This is made possible by the use of unique layout and interconnection properties of integrated injection logic (IIL) gates and by the extension of mask programming to additional mask layers beyond the metal interconnection.

### Features of IIL Technology

One of the most significant advances in monolithic LSI technology, IIL features high packing density, bipolar compatible processing, low power and low voltage operation, and low speed-power product. Fig 1 compares the speed and power capabilities of various logic families, including IIL. Since IIL is a direct extension of conventional bipolar IC technology, it lends itself readily to combining high density digital functions and conventional Schottky bipolar circuitry on the same chip. The availability of bipolar input/output interface and high density logic on the same chip facilitates the retrofit of custom IIL design into many existing logic systems.

With conventional photomasking and diffusion tolerances, gate densities greater than 200 gates/mm$^2$ can be achieved in full custom layout. Using the semicustom approach outlined in the following section, a packing density greater than 120 gates/mm$^2$ can be maintained—even with random metallization or interconnection requirements. This is at least four times better than conventional bipolar master-slice technology and approximately twice as good as the MOS master-slice approach in terms of gate density and chip area utilization.

### Designing with IIL Gate Arrays

A number of IIL gate arrays have been developed using bipolar compatible integrated injection logic technology. Two recent additions to the IIL product family offered by Exar are the XR-300 and XR-500—two gate array

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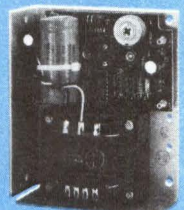
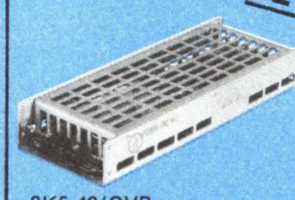
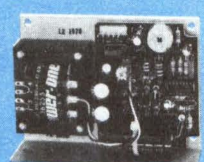
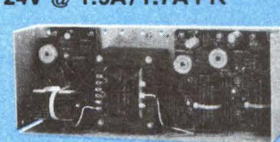
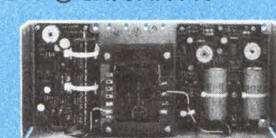
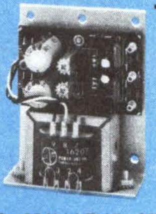
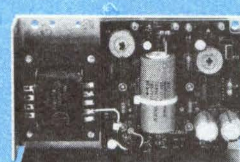
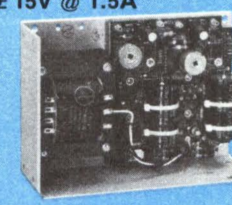
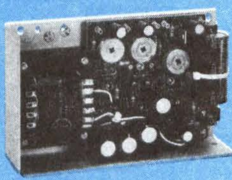
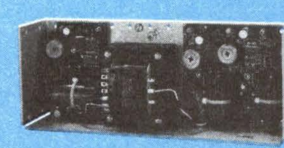
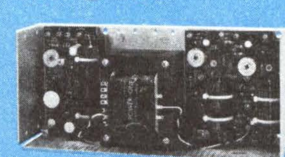
| **SINGLE OUTPUT & LOGIC POWER SUPPLIES**<br>• 56 "off the shelf" models<br>• 2V to 250V, 0.1A to 40A<br>• ±.05% regulation<br>• 115/230 VAC input | **5V @ 3A, w/OVP**<br><br>HB5-3/OVP<br>$24.95 single qty. | **5V @ 12A, w/OVP**<br><br>HD5-12/OVP<br>$79.95 single qty. | **5V @ 40A, w/OVP NEW**<br><br>SK5-40/OVP<br>Switching Model<br>$250.00 single qty. |
| **FLOPPY-DISK SERIES**<br>• 8 "off the shelf" models<br>• Powers most popular drives<br>• Single/dual drive applications<br>• 2-year warranty | **5V @ 0.7A, w/OVP NEW**<br>**12V @ 1.1A/1.7A PK**<br><br>CP340<br>For one 5.25" Media Drive<br>$44.95 single qty. | **5V @ 1A, w/OVP**<br>**−5V @ 0.5A, w/OVP**<br>**24V @ 1.5A/1.7A PK**<br><br>CP205<br>For one 8.0" Media Drive<br>$69.95 single qty. | **5V @ 2.5A, w/OVP**<br>**−5V @ 0.5A, w/OVP**<br>**24V @ 3A/3.4A PK**<br><br>CP206<br>For two 8.0" Media Drives<br>$91.95 single qty. |
| **DUAL OUTPUT MODELS**<br>• 15 "off the shelf" models<br>• ±5V to ±24V, 0.25A to 6A<br>• I.C. regulated<br>• Full rated to +50°C | **12V/15V @ 0.25A NEW**<br><br>HAD12-.25/HAD15-.25<br>$32.95 single qty. | **5V @ 2A, w/OVP**<br>**9−15V @ 0.5A**<br><br>HAA512<br>$44.95 single qty. | **±12V @ 1.7A or**<br>**±15V @ 1.5A**<br><br>HBB15-1.5<br>$49.95 single qty. |
| **TRIPLE OUTPUT MODELS**<br>• 10 "off the shelf" models<br>• 5V plus ± 9V to ± 15V outputs<br>• Models from 16W to 150W<br>• Industry standard size | **5V @ 2A, w/OVP**<br>**± 9V to ± 15V @ 0.4A**<br><br>HTAA-16W<br>$49.95 single qty. | **5V @ 3A, w/OVP**<br>**±12V @ 1A or**<br>**±15V @ 0.8A**<br><br>HBAA-40W<br>$69.95 single qty. | **5V @ 6A, w/OVP**<br>**±12V @ 1.7A or**<br>**±15V @ 1.5A**<br><br>HCBB-75W<br>$91.95 single qty. |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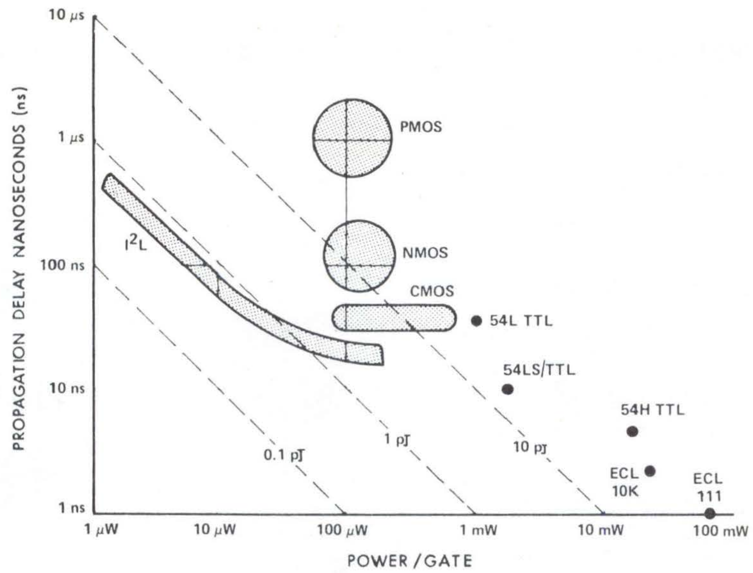



Fig 1 Comparison of speed and power capabilities of various logic families. IIL provides speed-power product of approximately 1.0 pJ

chips specifically intended for semicustom IC designs in complex digital systems. Some projected uses for the devices are in servocontroller circuits, antenna controllers, and pickup and proximity detectors. These chips contain many multiple-output IIL gates and Schottky bipolar input/output buffers. The Table summarizes the components available on each chip.

Fig 2 shows the layout architecture of the chips. At the periphery are the Schottky bipolar I/O interface circuits. The center section of each chip is a matrix of undedicated IIL gates arranged in the form of 8-gate cells. Each of these cells contains eight multiple-output IIL inverters which share a common set of four injectors.

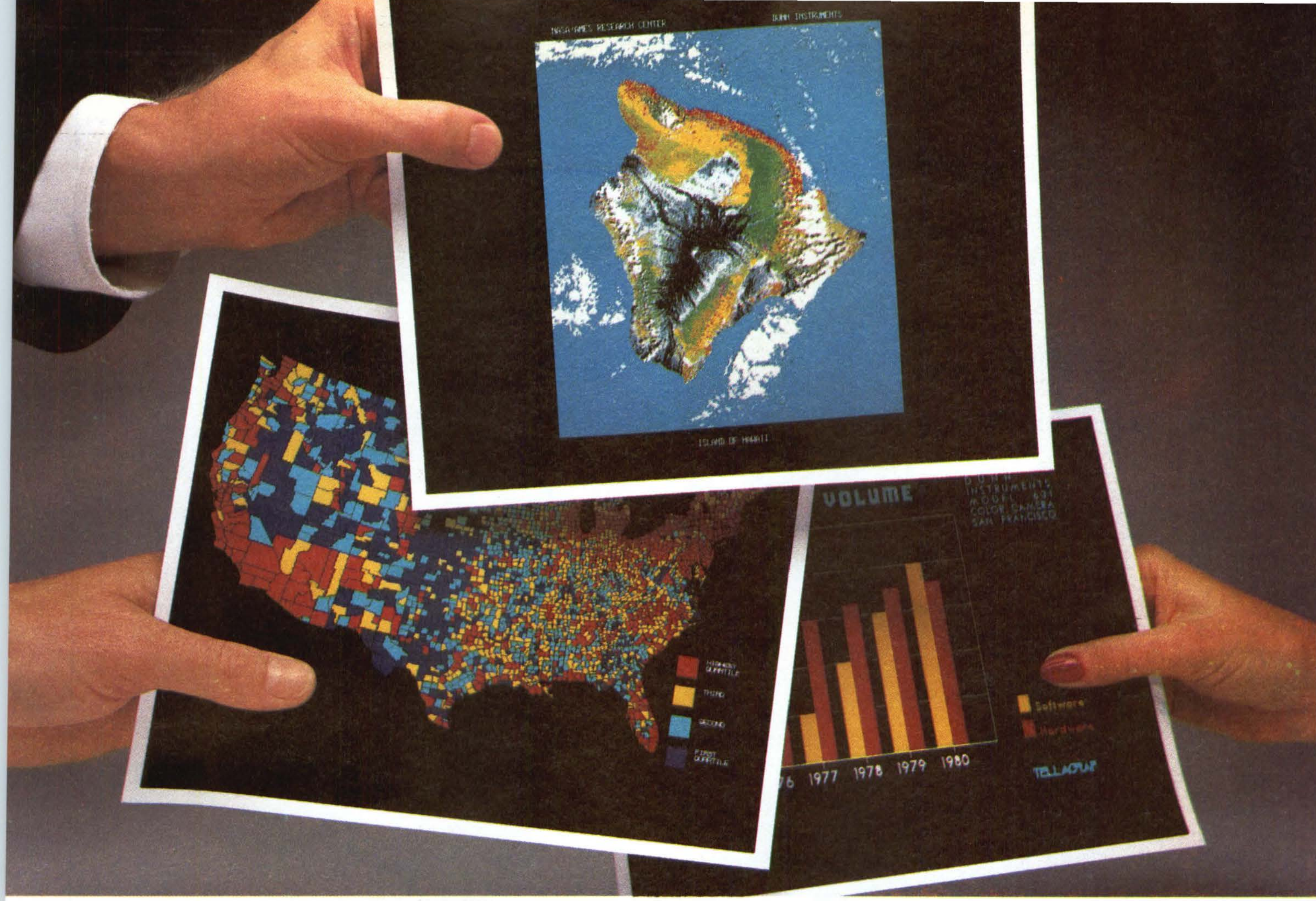
A basic 8-gate cell in the matrix consists of p-type injectors and gate "fingers" which serve as the base regions of the IIL gates (Fig 3). Dots on each gate area indicate the possible locations or sites for gate inputs or outputs. The use of a site as an input or output is determined by two custom masks: an n-type collector diffusion mask which defines output locations, and a custom contact mask which opens the appropriate input and output contact.

Finally, a third custom mask is applied to form the metal interconnections between the gates and the gate cells. The custom n-type diffusion step, which determines gate output locations, is also used to form low resistivity underpasses between the gate cells. Areas between gate cells can each accommodate two or three parallel underpasses in the horizontal and vertical directions, respectively. Since the n-type diffusion which forms these underpasses is a part of the customizing step, the location and length of each underpass can be chosen to fit a given interconnection requirement. This method provides the designer with virtually all the advantages and capabilities of multilayer interconnection paths on the chip surface and allows approximately 80% of the gates on the chip to be utilized in a typical random logic layout.

Turnaround time for development of these semicustom circuits is typically 33% of full custom development time. In view of this, and considering the density capability of approximately 60% of that offered by

**Components on XR-300 and XR-500 Semicustom Chips**

| Component Type | Chip Type XR-300 | XR-500 |
|---|---|---|
| Multiple-output IIL gates | 288 | 520 |
| Input/output buffers | 28 | 40 |
| Schottky—npn transistors | 56 | 80 |
| Resistors | 168 | 240 |
| Bonding pads | 34 | 42 |
| Chip size (mils) | 104 x 104 | 122 x 185 |

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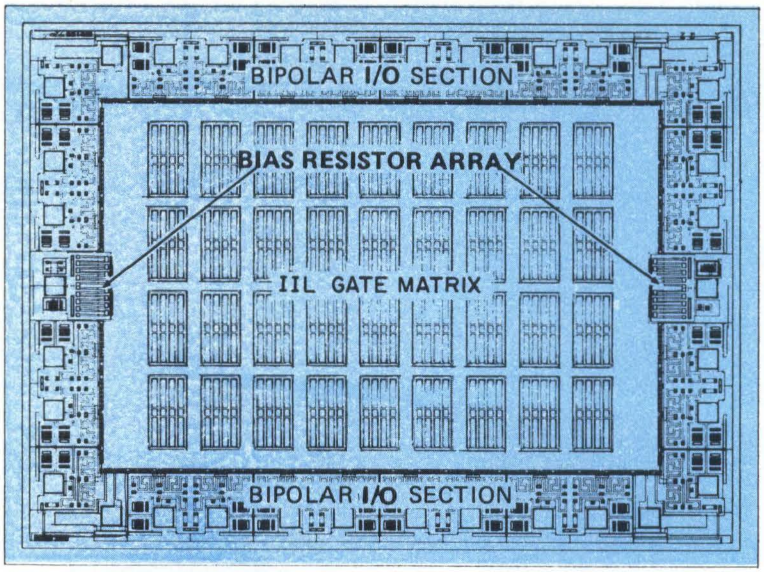



Fig 2 Basic architecture of IIL gate arrays XR-300 and XR-500. Central part of chip is matrix of undedicated 8-gate cells. Bipolar I/O circuits occupy periphery

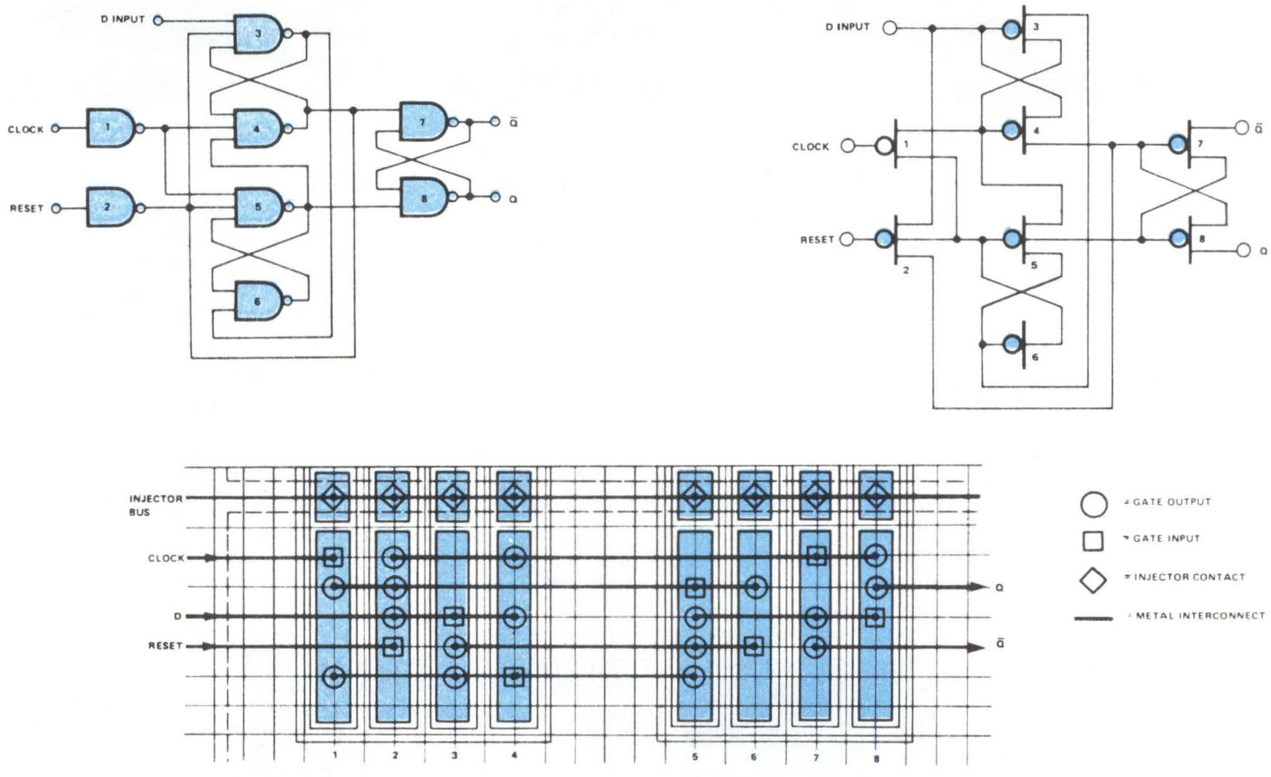
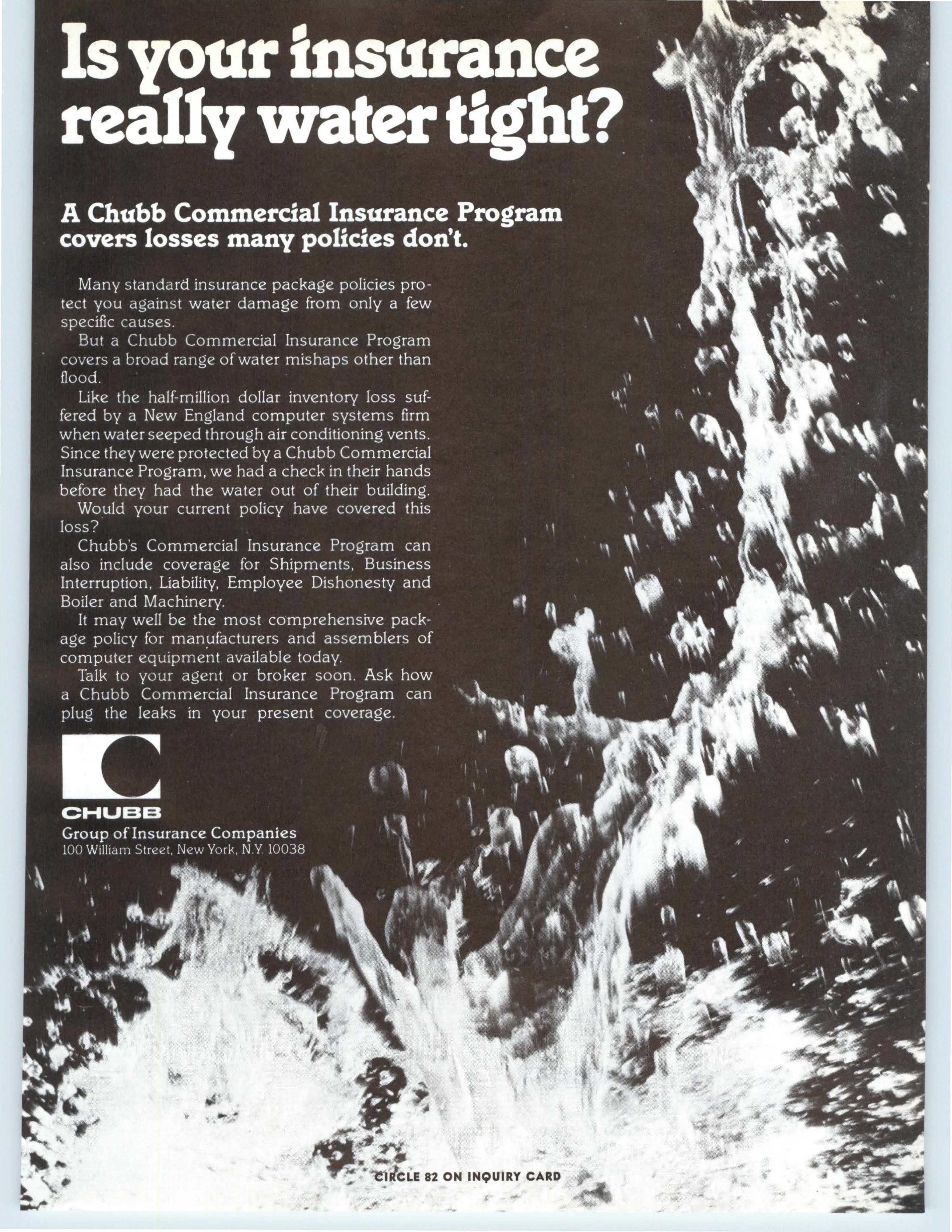



Fig 3 Typical design and layout example using one of 8-gate cells on IIL gate array. NAND logic diagram for D-type flipflop (a) is first connected to IIL gate equivalent (b), and then laid out on 8-gate cell, as shown in (c). In this layout, circles and squares indicate gate outputs and inputs, respectively, and solid lines connecting them correspond to metal interconnections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the full custom approach, the remaining key criterion to be examined in determining the utility of the semicustom approach is cost.

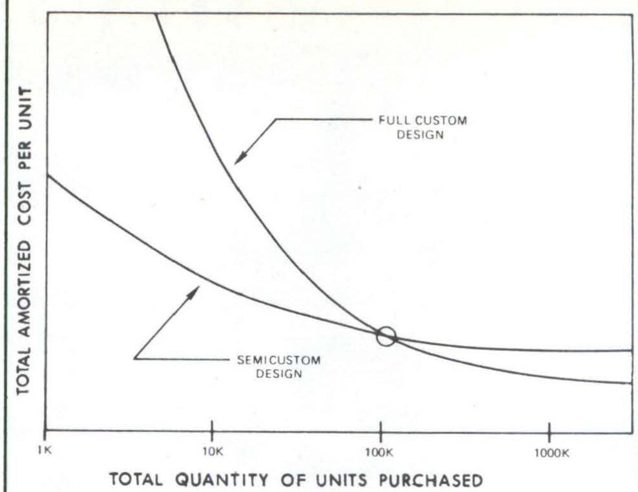



Fig 4 Comparison of relative cost advantages of semicustom and full custom LSI products. Amortized cost per unit includes development cost

### Economics of Semicustom Design

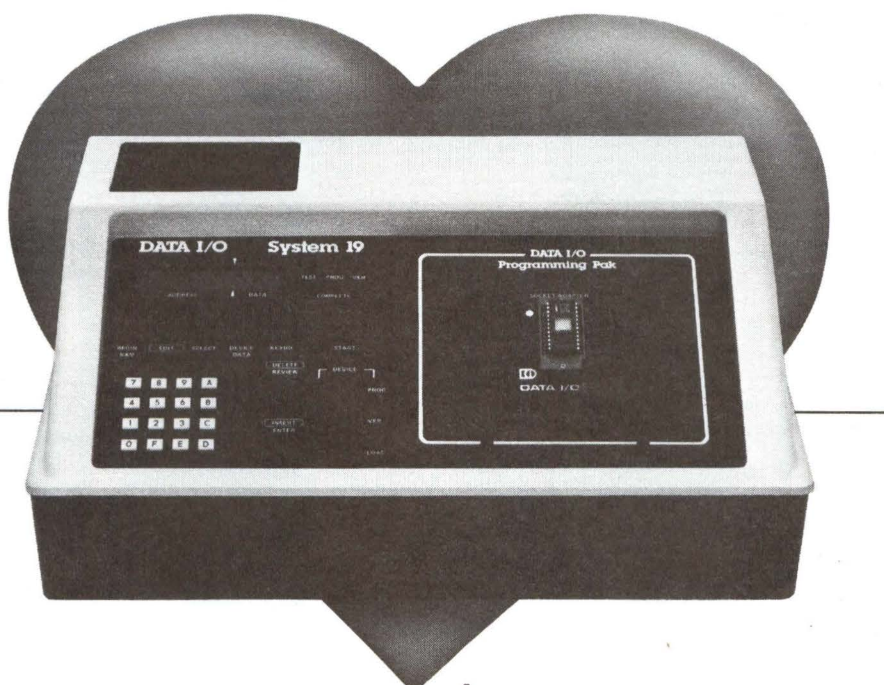
For a given production requirement, is it cheaper to develop a full custom or a semicustom LSI integrated circuit? Since performance and functional requirements of custom ICs vary widely, this question has no clear cut answer. Based on overall production requirements, however, it is possible to establish some economic guidelines for deciding which custom IC technology to use—and when to use it.

A major advantage of semicustom LSI design is development cost—typically 10 to 30% of that required for a complete conventional full custom IC design. However, since random interconnections resulting from the semicustom design technique tend to waste some of the IC chip area, the unit price of a semicustom LSI chip in volume production is slightly higher (approximately 10 to 30%) than that of a full custom design.

To decide on the most economical approach, therefore, estimated amortized unit cost per device at a number of different production quantities should be compared. Fig 4 provides such a comparison for a typical custom LSI chip as a function of total production requirement. Total amortized cost per unit is defined as the total cost of development plus production, divided by the total number of units purchased. At low production quantities, the extremely high development costs (typically $50,000 to $100,000) of full custom designs make them far more expensive than semicustom designs in terms of amortized unit cost. On the other hand, at high production volumes, full custom ICs are more economical because of their lower chip cost.

The typical crossover point between the economics of full and semicustom technology falls in the range of 50,000 to 100,000 pieces, as implied by Fig 4. This illustration, however, is only one case study; the actual crossover point for a given program will depend on circuit complexity, performance and test requirements, and the type of IC package used. □

# DEAR DEVELOPMENT SYSTEM:

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## Bit Lines Share Sense Amplifiers In 64k Dynamic RAM

Organized as 64k x 1, an N-channel MOS dynamic random access memory achieves high cell density through use of triple-polysilicon gate technology. Within each cell, two polysilicon plates separated by a thin dielectric layer form the memory capacitor. The transfer switch is a single, self-aligned poly element.

Another key attribute of the memory is the assignment of two pairs of bit lines to every sense amplifier, the sense amplifier then multiplexing between these pairs. This results in a halving of the number of memory cells on each bit line and therefore an increase in the signal voltage input to the sense amplifier.

The NMC4164, produced by National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051, is a 256-row by 256-column device, utilizing a 256-cycle refresh every 4 ms (Fig 1). It features a multiplexed address input with separate row and column strobes. Maximum access times are 120 ns for the -1 suffix model and 150 ns for the -2 suffix model. Other characteristics include a single 5-V supply, low power operation (250 mW), TTL compatibility on all inputs and outputs, and page mode operation.

Chip size is 0.24 cm$^2$, with memory cell size 195 $\mu$m$^2$. The RAM is to be provided in a 16-pin dual in-line package and is due for formal announcement during the fourth quarter of 1979.

This memory cell is said to provide two significant improvements over structures used in previous RAM generations. First, the storage medium is a high quality capacitor, with only 20% of the total area of the

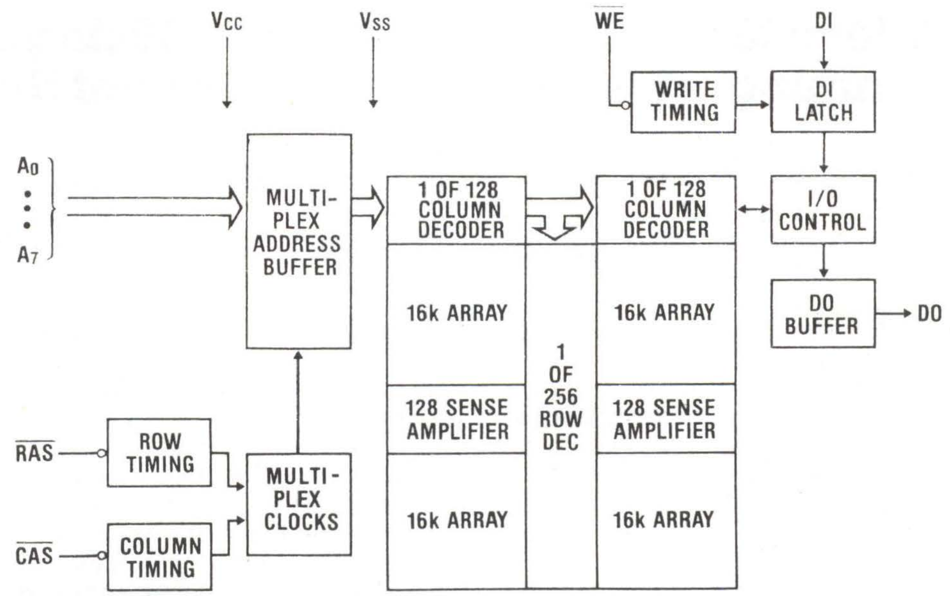


Fig 1 64k RAM, NMC4164, from National Semiconductor. Multiplexed address input utilizes separate row and column strobes. Device must be refreshed every 4 ms

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North Star has quadrupled the disk capacity of the Horizon computer but prices have increased a modest 15 percent. On a dollar per byte basis, that's a bargain that is hard to beat!

The proven North Star disk controller was originally designed to accommodate the two-sided drives. North Star DOS and BASIC are upgraded to handle the new capacity, yet still run existing programs with little or no change. Of course, single sided diskettes are compatible with the new disk system.

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| Horizon-1-32K-D | $1485 |
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**CIRCLE 85 ON INQUIRY CARD**

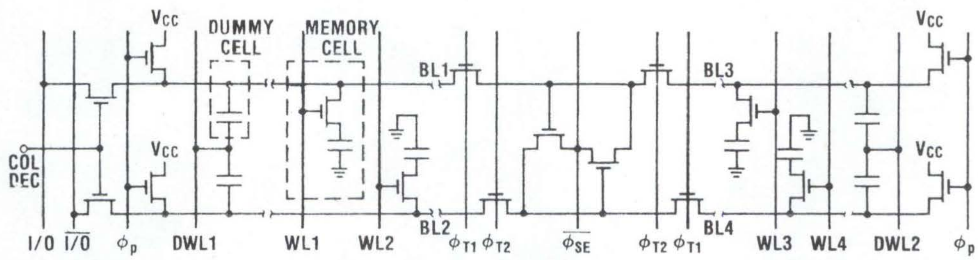


Fig 2 Memory cell and sense amplifier for 64k RAM. Sense amplifier is shown as pair of transistors on either side of sense amplifier enable line, $\overline{\phi}_{SE}$. Two pairs of bit lines share each sense amplifier, multiplexed at $\phi_{T1}$, $\phi_{T2}$

storage node subject to substrate leakage. This results in considerably improved refresh characteristics over an equivalent sized inversion capacitor and also provides a high degree of immunity to soft errors resulting from ionizing particles. Secondly, the space separating the capacitors can accommodate the transfer switch, and this results in a more efficient utilization of cell area.

Fig 2 indicates the sense amplifier design, which is symmetrical about the center point where the sense amplifier enable line, $\overline{\phi}_{SE}$ makes contact. Thus bit lines $BL_1$, and $BL_4$ are balanced, as are $BL_2$ and $BL_3$. The transfer devices clocked by $\phi_{T1}$ and $\overline{\phi}_{T2}$ are decoded to select one of these bit line pairs. The dummy cell omits the conventional transfer and reset devices, easing the layout and improving the matching of dummy and memory capacitors.

Recommended dc electrical characteristics include supply voltage, $V_{CC}$, between 4.5 and 5.5 V; input high voltage, $V_{IH}$, between 2.4 and 7.0 V; and input low voltage, $V_{IL}$, between −1.0 and 0.8 V. Absolute maximum ratings require that voltage on any pin (relative to $V_{SS}$) lie between −1.0 and 7.0 V. Maximum allowable power dissipation is 1 W. Temperature must remain between 0 and 70 °C during operation, and between −65 and 150 °C in storage.




CIRCLE 86 ON INQUIRY CARD

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**CIRCLE 87 ON INQUIRY CARD**

## 12-Bit DAC Provides 2-Quadrant Multiplication

Two chips are utilized in the design of a digital to analog converter offering 12-bit accuracy and a 2-quadrant multiplying capability. One of these is a stable, weighted current switch chip and the other is a thin film laser trimmed resistor chip. Analog output current is proportional to the product of the input reference voltage and the digital input word.

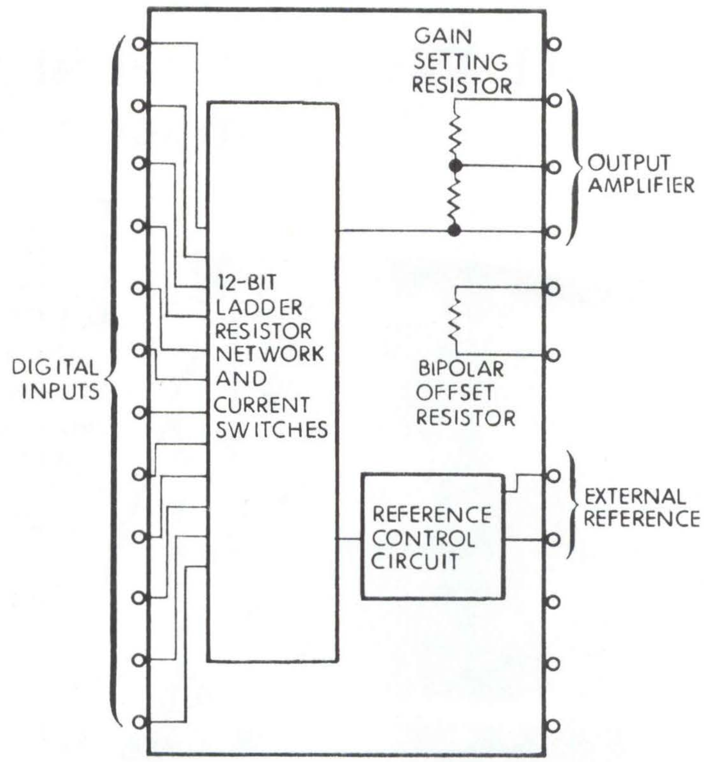
The digital input code is positive true logic and is compatible with TTL or CMOS logic without buffering. Offset binary code is created by offsetting the output amplifier with the DAC reference. Two's complement code is obtained from offset binary by externally inverting the most significant bit.

Manufactured by Burr-Brown Research Corp, PO Box 11400, Tucson, AZ 85734, the DAC862 offers ¼ LSB nonlinearity, ±5-ppm/°C max gain drift and ±4-ppm/°C bipolar offset drift, and is pin compatible with 562 type converters. Monotonicity is guaranteed over the entire specified temperature range, which is 0 to 70 °C (suffix KG version) or −25 to 85 °C (suffix BG). Other characteristics include 3.5-µs (max) settling time to ½ LSB, 400-ns (typ) major carry glitch duration to 90% complete, and a 20-µV (typ) noise level, pk-pk, from 0.1 to 10 Hz, all 1s.

Use as a 2-quadrant multiplying D-A converter is obtained by applying the analog signal to be processed through a 100-Ω potentiometer to the reference voltage input, pin 5. The analog signal must be between 0 and 10 V. While the error can be quite large for voltages near 0, dc error of the output signal is less than 0.05% for a reference voltage range of 1 to 10 V.

The DAC is provided in a 24-pin hermetic ceramic dual inline package and is priced from $24 in 100s. Screening is available to the requirements of MIL-STD-883.

Circle 350 on Inquiry Card

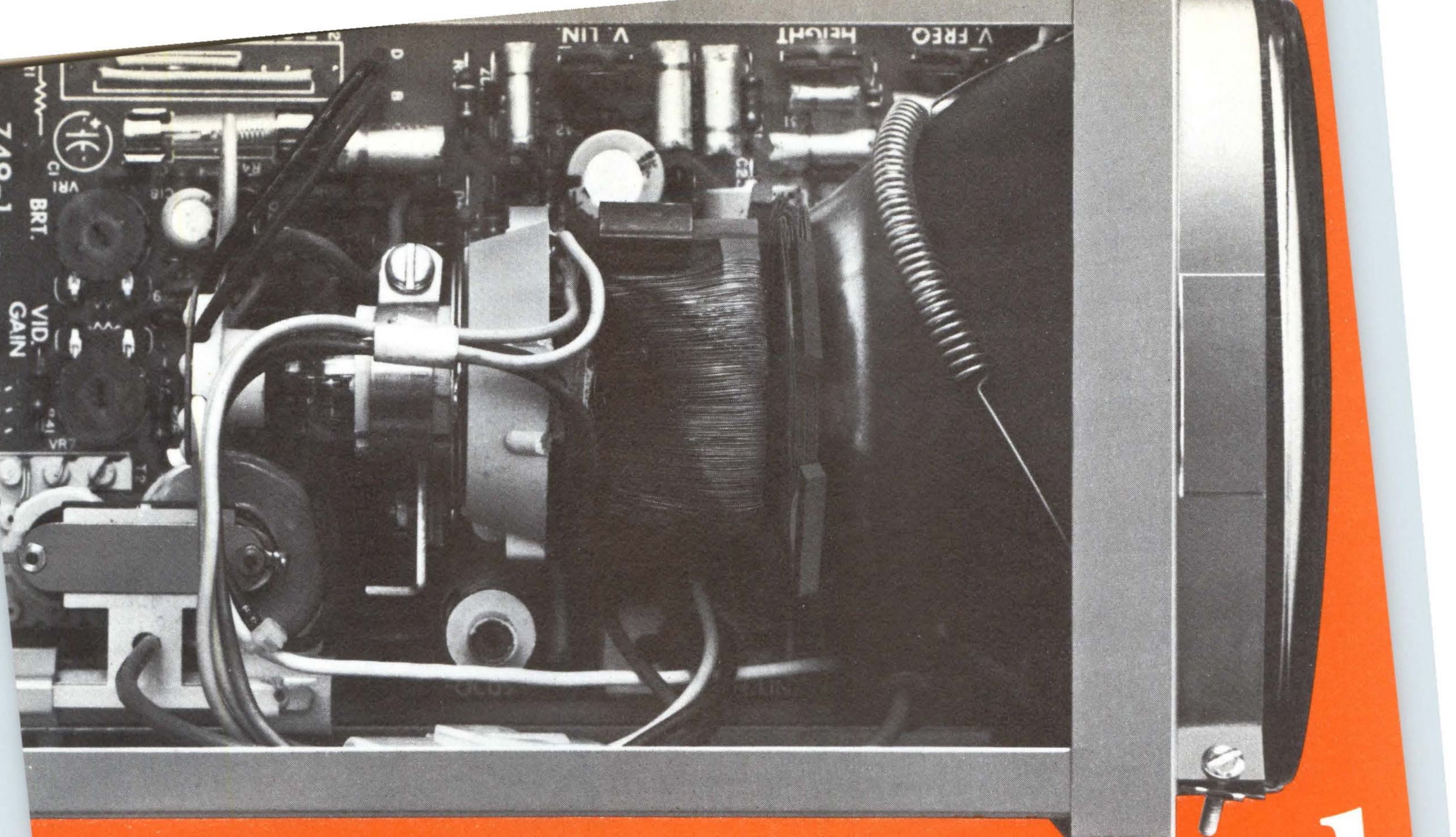



D-A converter, DAC862, from Burr-Brown. 2-chip IC provides 12-bit accurate analog output current proportional to product of input reference voltage and digital input word

## Precision Switching Cells Increase Speed, Accuracy of 12-Bit DAC

Settling to ½ LSB in 200 ns (typ) and 400 ns (max), a 12-bit monolithic digital to analog converter is available at $13 in thousands from Analog Devices, Rte 1 Industrial Pk, Norwood, MA 02062. A fully differential, nonsaturating precision current-switching cell structure provides a 30-ns full scale switching time.

Other features include operation from a single 15-V supply, low power dissipation of 180 mW (typ), and CMOS or TTL compatible inputs. On-chip thin film SiCr application resistors can be used as input resistors in building a successive approximation ADC or with an external operational amplifier to provide a precision voltage output. The resistors are





matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser trimmed for minimum full scale and bipolar offset errors.

Six grades are available. AD566 JN and JD grades guarantee worst case accuracy and differential nonlinearity to be ±¾ LSB over the 0 to 70 °C temperature range; KN and KD grades guarantee ±½ LSB accuracy and differential nonlinearity over the same range. Accuracy and differential nonlinearity are guaranteed to be ±¾ LSB and ±½ LSB for SD and TD grades, respectively, over the −55 to 125 °C range. Grades with D suffixes feature hermetic, ceramic side-brazed 24-pin DIPs, and grades with N suffixes are housed in 24-pin plastic DIPs.

This DAC is intended for applications in high speed display drivers, fast ADCs, and applications where high speed and precision are to be maintained over temperature extremes, humidity, and mechanical stress. It is pin compatible with industry standard AD562 DACs and features guaranteed monotonicity over the full operating temperature range of every version. In addition, 100% screening to MIL-STD-883B, method 5004, is available.

A wide compliance range of −2 to 10 V allows current to voltage conversion with a single output resistor and allows applications such as directly driving a long cable at high speed. The converter provides a current output of 0 to −2 mA. It may be used in a 2-quadrant multiplying mode, accepting bipolar digital inputs and reference inputs from 1 to 10 V at up to 40 kHz.

Absolute maximum ratings require that voltage from $V_{EE}$ to digital common lie between 0 and −18 V and that analog common to digital common lie between ±1 V. Voltage on the DAC output must remain between −3 and 12 V, and on digital inputs between −1 and 7 V. Maximum allowable power dissipation is 1 W.

Circle 351 on Inquiry Card

## Monolithic Pulse Width Modulator Replaces More Than 300 ICs

A pulse width modulator chip containing the equivalent of more than 300 discrete devices is designed for fixed frequency switching regulators and other power control applications. The SG1526, produced by Silicon General Inc, 11651 Monarch St, Garden Grove, CA 92641, is 2½ times larger than the earlier monolithic PWM, SG1524, from the same manufacturer. A significantly larger portion of the circuitry needed for switching power supplies has been packed into the newly announced device.

In addition to a temperature compensated voltage reference, sawtooth oscillator, error amplifier, and pulse width modulator, the linear LSI chip offers built-in pulse metering and steering logic, two low impedance output drivers, and a variety of protective features. Soft start circuitry and undervoltage lockout, digital current limiting, double pulse inhibit, and adjustable deadtime are included, as well as a provision for symmetry correction.

For ease of interface, all digital control ports are bidirectional and are TTL and B-series CMOS compatible. Active low logic design allows wired-OR connections for maximum flexibility. This device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled. The output drivers are capable of either sourcing or sinking currents to 100 mA, providing turn on and turn off commands to external power transistors, and are fully capable of driving VMOS power FETS at frequencies to 300 kHz. Current limiting on the source driver limits current spiking to 200 mA and also protects the driver against shorts to ground. Built-in pulse metering and steering logic permits pulse by pulse current limiting and eliminates chattering at the threshold of the PWM comparator.

The 5-V reference voltage is trimmed to ±1% during wafer test to eliminate production tolerances and the need for adjustment potentiometers. Specified operating conditions for the device are 8 to 40 V, over a frequency range of 50 to 300 kHz.

A synchronization input to the oscillator allows multiple units to be slaved together, or for a single unit to be synchronized to an external system clock, providing freedom from noise transients due to beat frequencies. Synchronization of up to six devices is guaranteed.

The PWM is provided in an 18-pin CERDIP. It is available in three models, with the 1526 characterized for operation from −55 to 125 °C, the 2526 operating from −25 to 85 °C, and the 3526 from 0 to 70 °C.

Circle 352 on Inquiry Card

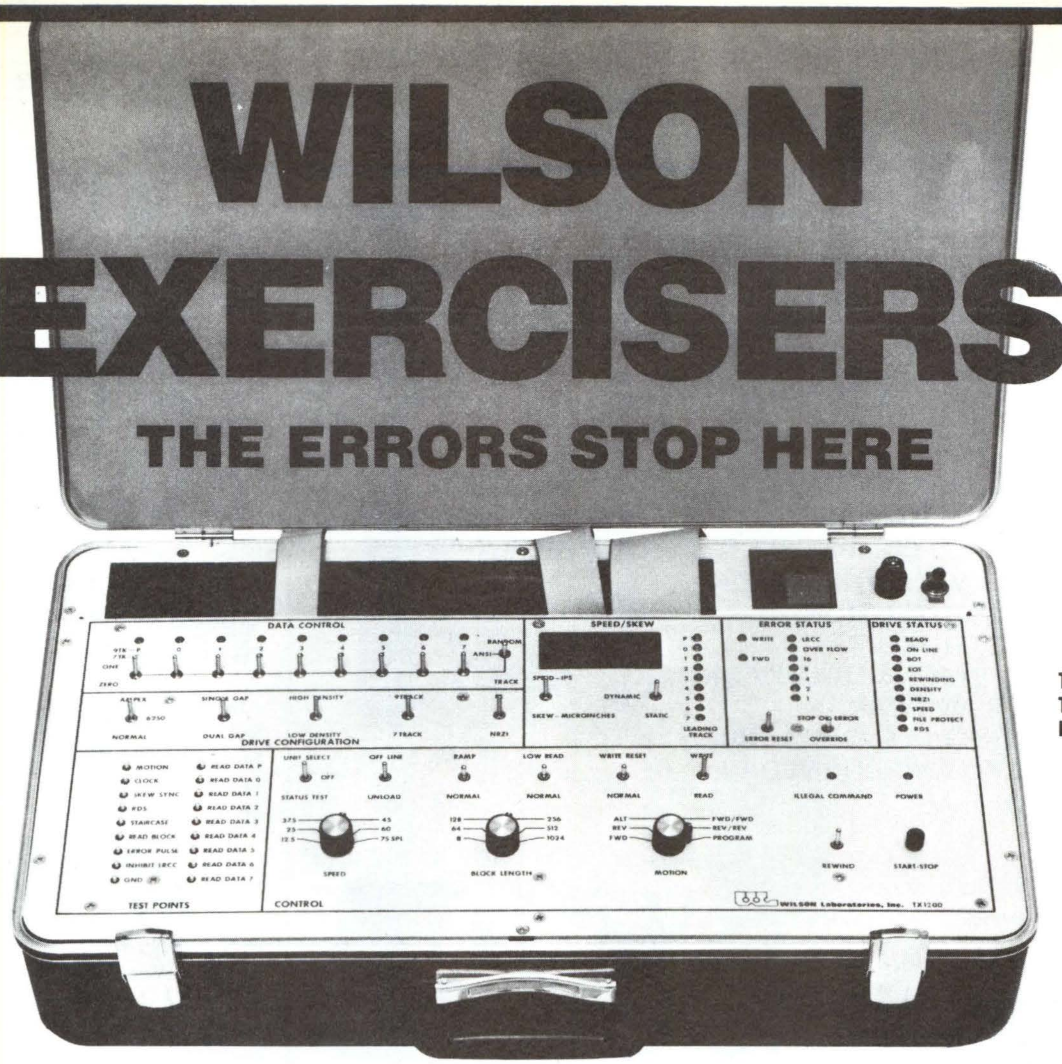
## Monolithic Interface Bus Adapter Fulfills IEEE 488 Requirements

Fabricated with n-channel silicon gate technology and completely TTL compatible on all inputs and outputs including power supply (5 V), a single-chip general purpose interface bus adapter (GPIBA) meets IEEE Std 488-1978. The TMS9914 from Texas Instruments Inc, PO Box 1443, Houston, TX 77001, has talker, listener, and controller capabilities. It provides complete microprocessor interface when used with GPIB octal transceivers SN75160/61 from the same manufacturer (see *Computer Design,* Jun 1979, p 200). In this capacity, it performs the interface function between the microprocessor and the bus and maintains IEEE 488-1978 protocol, relieving the microprocessor of that task.

Although this interface is designed for use in instrumentation applications, it is not restricted to such applications. It is also useful in microprocessor based systems where data must be transferred between processors. The device needs a single-phase clock (nominally 5 MHz) which can be independent of the microprocessor system clock, facilitating interfacing with the microprocessors.

Communication between the GPIBA and the microprocessor is carried out via 13 memory mapped registers—6 read and 7 write. Read types are interrupt status, address status, bus status, address switch, command pass through, and data in registers. Write types are interrupt mask, auxiliary command, address, serial poll, parallel poll, and data out registers. The device interfaces to the CPU with an 8-bit bidirectional data bus, three register select lines, two DMA control lines, reset and interrupt request lines, a DBIN, and a $\overline{\text{WE}}$ line.

Because of the interrupt capabilities of the device, the bus does not have to be continually polled, and fast responses can be made to changes in the interface configuration. The GPIBA can operate at rates up to 250k

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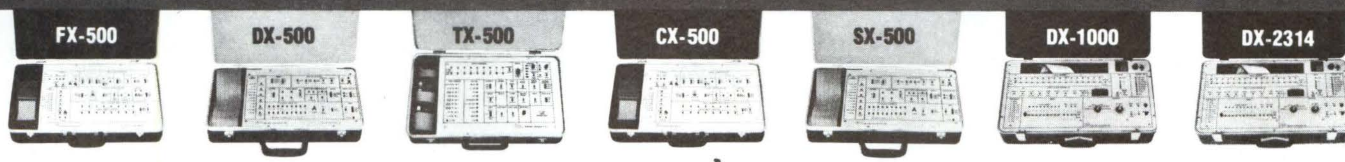


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bytes/s, a speed said by the manufacturer to be two to five times faster than competitive interface bus adapters presently on the market.

Recommended operating conditions include a supply voltage of 5 V, continuous power dissipation of 1 W, and an operating temperature range of 0 to 70 °C. Packaged in a 40-pin DIP, the device is priced at $25.60 in 100-piece quantities.

Circle 353 on Inquiry Card

## 8-Bit Registers Operate at High Speed

An 8-bit register using advanced low power Schottky technology contains eight positive edge triggered D-type flipflops. Clock to output delay is 18 ns (typ).

There are two versions of the device. The Am54LS/74LS273 has a buffered common clear. In operation, when the clear input is low, all outputs are forced low regardless of inputs. When the clear is high, data can be entered in the register. Data that meet the setup and hold time requirements of the D-type flipflop inputs are transferred on the low to high transition of the clock input.

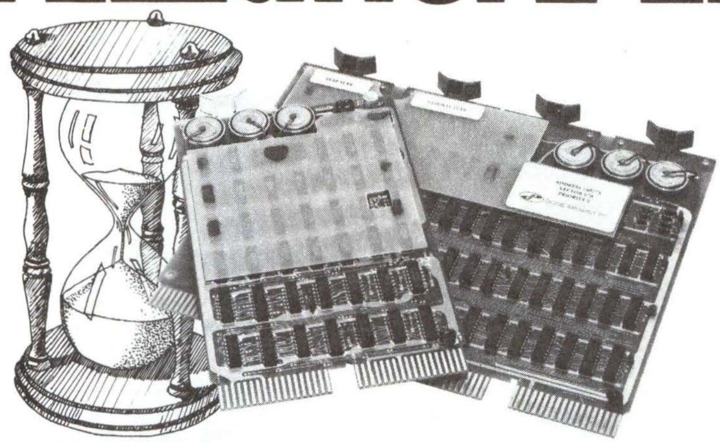
The Am54LS/74LS377 offers a buffered common clock enable. With the clock enable input low, new data are entered into the flipflop register on a low-to-high clock transition. When high, the register retains present data independent of clock inputs.

Both of these devices are also available in higher performance versions, Am25LS273 (with 15-ns typ clock to output delay) and Am25LS377 (with 14-ns typ clock to output delay). These also offer the following improvements over the standard devices: 50 mV lower $V_{OL}$ at $I_{OL} = 8$ mA, twice the fanout over the military temperature range, and 440-$\mu$A source current at high output. B-suffix models of the higher performance devices provide an additional output buffer to eliminate output commutation.

Produced by Advanced Micro Devices Inc, 901 Thompson Pl. Sunnyvale, CA 94086, all models are 100% screened to MIL-STD-883 requirements. They are provided in 20-pin packages with 0.3" (7.6-mm) row spacing. □

Circle 354 on Inquiry Card

# TIME after TIME



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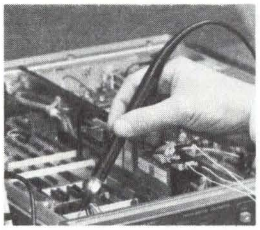

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Course 142 - Five days

This unique course is specifically designed for engineers and senior technicians involved in production testing, field service, and design of microprocessor-based systems. The course provides these personnel with the practical knowledge they require, including an in-depth understanding of: a) microprocessor software and hardware; b) how to apply the most powerful microprocessor debugging techniques; and c) how to use microprocessor troubleshooting equipment.

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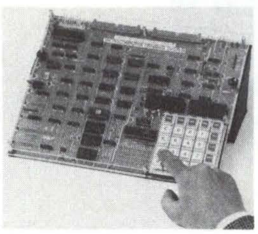

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Course 160 - Four days

This course is intended for engineers, programmers, systems analysts and their managers. It has been found extremely useful by attendees both with or without prior experience in either computers or electronics. In fact, managers who have attended report the course provides a level of familiarity, awareness, and confidence which enables them to better manage their staff in applying microprocessors.

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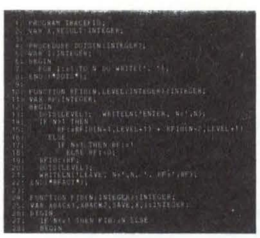

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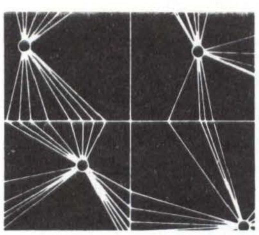
The PASCAL programming language is attracting widespread attention as a structured language tool for improving programmer productivity and reducing program maintenance costs. It is now being used both for implementing complex system programs and for applications ranging from commercial databases and word processing to scientific computations and instrument control. The course is designed for engineers, scientists, programmers, system analysts and their managers. THE COURSE INCLUDES HANDS-ON PROGRAMMING OF MICROCOMPUTERS IN PASCAL.

## Distributed Processing and Computer Networks



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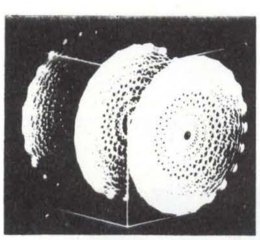
**SAN DIEGO** Jan. 22-25

Course 350 - Four days

This course provides a comprehensive introduction to distributed processing and computer network design techniques. It covers the individual elements of a distributed processing system and how these elements are synthesized to form a system which best meets application specific objectives. Throughout the course, application examples provide concrete examples of concepts presented, with emphasis on the factors affecting key planning, design and implementation decisions.

## Computer Graphics State of the Art Techniques and Applications



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**NEW YORK** Oct. 16-19
**LOS ANGELES** Oct. 30-Nov.2
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Course 365 - Four days

Hardware elements of computer graphics systems are presented at the level required for detailed system specification, selection and acquisition. Software techniques for computer graphic systems are developed from the elementary level of line generation and continue through advanced approaches to animated three-dimensional color displays with hidden surface removal. Off-the-shelf, commercially available software packages are analyzed and evaluated. Emphasis is placed on hardware/software tradeoffs, cost effectiveness and the advantages and limitations of alternative approaches.

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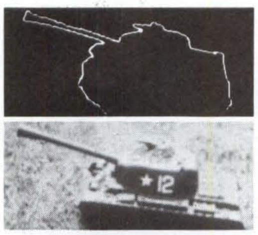
# Digital Image Processing



**WASHINGTON, D.C.** Oct. 9-12
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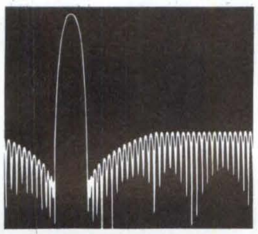
Course 410 - Four days

This course is designed for programmers, analysts, engineers and scientists who need to acquire a fundamental knowledge of digital image processing techniques. The course provides the comprehensive mathematical and conceptual background necessary to design and implement systems for: image acquisition and display, analysis and measurement, enhancement and restoration, and coding and representation. Application areas will include military and aerospace systems, biomedical, remote sensing, earth resources, cartography, non-destructive testing and quality control.

# Digital Signal Processing

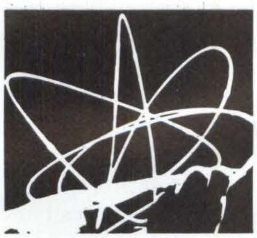


**LOS ANGELES** Oct. 15-19
**CHICAGO** Oct. 22 -26
**SAN DIEGO** Nov. 5-9
**HOUSTON** Jan. 21-25

Course 412 - Five days

The objective of this course is to present the necessary fundamentals of digital signal processing in a clear and comprehensive manner,to develop an understanding of new processing techniques, to survey the state of the art of hardware and software available, and to apply this information to a range of concrete design examples. The course is of benefit both for those who wish to achieve a basic understanding of this exciting area, and for those whose interest is in advanced techniques and the implementation of practical systems.

# Fiber Optic Communication Systems

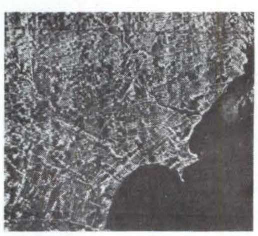


**LOS ANGELES** Nov. 13-16
**SAN FRANCISCO** March 18-21

Course 440 - Four days

This course is designed for engineers, scientists and managers who are, or will be, involved in the planning, design and practical implementation of all types of communication systems. Commercially available components will be surveyed and concrete case studies of existing systems will be used to illustrate key managerial and technical considerations, emphasizing design techniques for the cost effective, practical application of this important technology.

# Synthetic Aperture Radar Systems



**WASHINGTON, D.C.** Oct. 23-26
**LOS ANGELES** Nov. 13-16

Course 475 - Four days

The course provides an overview of SAR system design considerations; basic principles of operation; requirements on the antenna, transmitter-receiver, signal processor, display and motion compensation subsystems; and an exposition of image quality considerations. A quality evaluation model is developed which leads directly to the determination of detection probability for targets and terrain features. A concrete example SAR system will be designed and evaluated using a practical set of operational requirements.

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**Integrated Computer Systems, Inc.**
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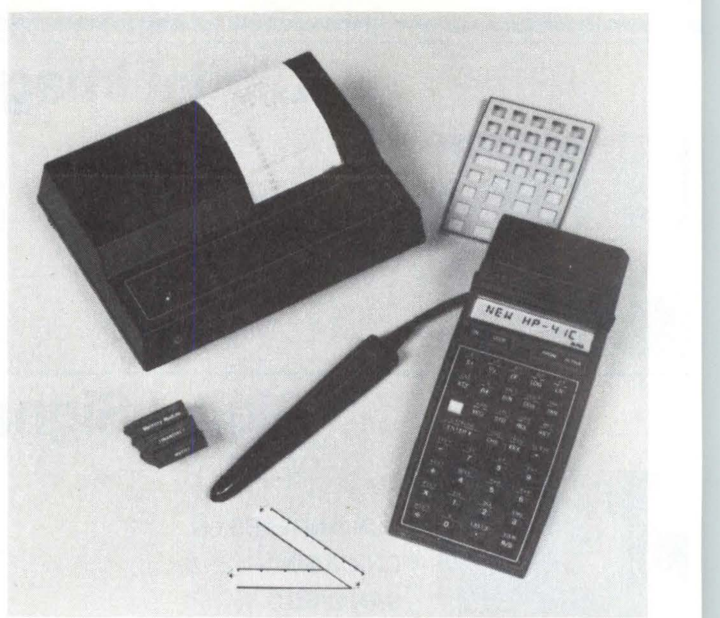
**Alexandria, VA 22314**

**(703) 548-1333**
WASHINGTON, D.C.

# PRODUCTS

## Personal Calculating System Has Power Of Small Computer




Even by itself, the alphanumeric HP-41C handheld calculator is claimed to be an advanced and versatile device that functions with both supplied and user written programs. However, when companion peripherals are connected through built-in ports, the device becomes a personal calculating system "as powerful as some small computers." Designed and manufactured by Hewlett-Packard Co at its Corvallis Div, this calculator is 100% faster than the company's earlier handheld models, contains up to four times the memory capacity (with available options), and has 40% more standard functions.

The basic calculator is programmed with more than 130 scientific and mathematical functions commonly used by engineers and scientists. User programs for solving problems in dedicated applications are provided in application pacs and solution books.

Of the functions, 58 are identified by the keyboard. A catalog of other available functions including those defined by the user is available from the calculator on user demand.

Programs are labeled in English and word messages alert the user to errors in calculations and programs. The continuous memory liquid crystal display also allows programs to contain messages that prompt the user.

Base program memory can be raised from 400 lines or 63 data storage registers to as many as 2000 lines or 319 registers through use of 4 plug-in memory modules. In addition, 16 plug-in application modules offer 4000 program steps each of preprogrammed solutions to problems in specific areas.

Programs also can be entered from recorded magnetic cards (or programs can be recorded on blank cards) via a plug-in card reader. Another option provides hardcopy records from a portable thermal printer. An optical wand to read and enter programs or data from printed bar codes will be available at a later date.

Nearly any function built or programmed into the calculator can be assigned to keyboard locations and the keys labeled, then relabeled when the functions are reassigned. To program the calculator for special calculations, the user assigns a program name and then presses keys in the order that would be required to solve a problem. When the program name is again keyed in, the full series of keystrokes is executed automatically.

Each of the calculator's programs can be called up by name, run, edited, or erased without affecting other programs. Program memory between data registers and program lines can be allocated by the user for programming flexibility.

CMOS technology protects user programs and data in the calculator when power is turned off. Frequently used programs and conversion constants are retained in "continuous memory," virtually indefinite storage.

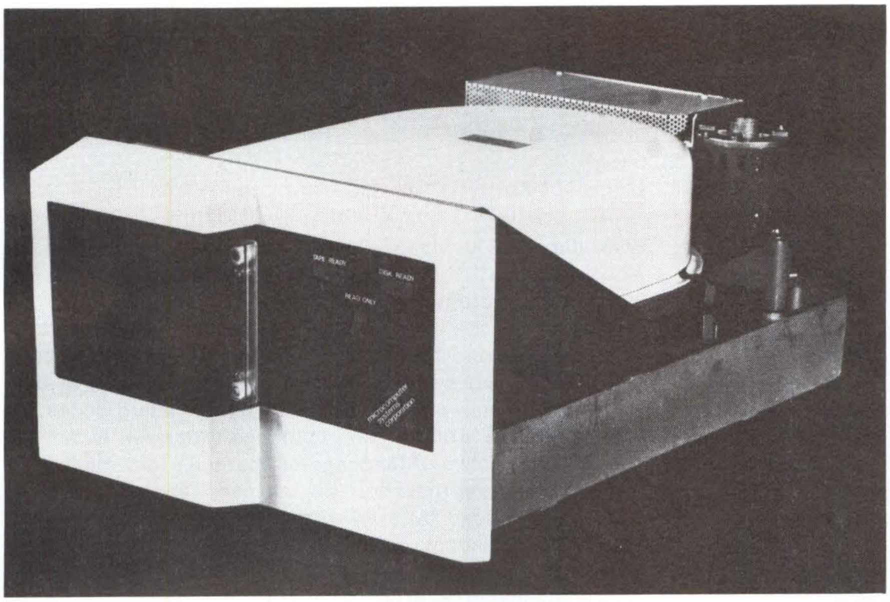
Data, constants, and results can be automatically compared by a program; outcome of the comparison can then alter execution. All 56 flags can be tested during programming, again with automatic altering of program execution based on test results.

### Price and Delivery

The basic HP-41C handheld calculator is priced at $295; each memory module, with 64 data storage registers, up to 400 lines of program registers, or any combination of user selected data storage and program memory, costs $45; the card reader costs $195; the printer is $350; and the applications modules are $45 each. All are immediately available. The wand will be available in early 1980. Hewlett-Packard Co, 1000 Northeast Circle Blvd, Corvallis, OR 97330. Tel: 503/757-2000.

Circle 199 on Inquiry Card

## Backup Tape Cartridge Protects Data on Companion Fixed Discs



Failsafe storage of user's data is provided in the MSC-5900 system by combining a backup tape cartridge with a Winchester type disc drive. If the disc drive fails, the tape can be removed and played back on another unit. Easy access is provided through the front panel.

In addition to the two storage devices, Microcomputer System Corp has included a microprocessor based controller in the same compact package. Only an initial data request command from the host CPU is required. All other control of the storage device is maintained by the microprocessor. It controls drive functions, data formatting and buffering, dump and restore operations for the tape cartridge, and communications with the host.

Each model of the data storage system contains a single spindle with 4 disc platters, and 2, 6, 10 or 14 data heads in a sealed module for storage capacities of 12.5M, 37.6M, 62.7M, and 87.8M bytes, respectively. Average head access time is 40 ms (10 to 70 ms) and average latency time is 10.12 ms (at a nominal 2964 r/min). Data transfer is at 885k bytes/s.

Speed of the standard 3M type cartridge, which contains 450 ft (137 m) of 0.25" (6.35-mm) tape for 17.1M bytes of removable storage, is 30 in (76 cm)/s forward and reverse when reading or writing data and 90 in (228 cm)/s for search mode. Data transfer rate is 1.1M bytes/min.

Microprocessor controlled resident diagnostics allow thorough exercising of the controller and both drives. In addition, they test search, read, and write operations for each data head. LEDs identify faults and aid in troubleshooting.

Single burst errors up to 11 bits long are corrected by the controller. Full-sector data buffering reduces data bandwidth requirements for the host CPU, and high level disc commands minimize I/O driver overhead.

Data storage systems are field expandable. Interface adapter boards are available for DEC PDP-11, Data General Eclipse and Nova, Hewlett-Packard 21xx, and IBM Series/1 computers.

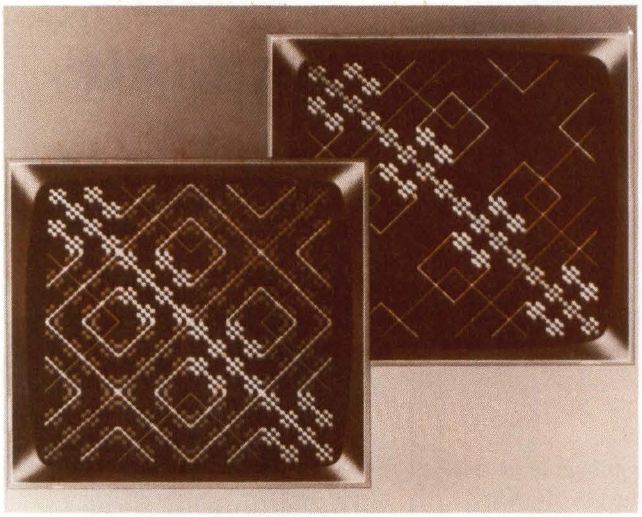
### Price and Delivery

The 87.8M-byte version of the MSC-5900 data storage system is priced at $8250 in OEM quantities. Deliveries are 90 days ARO. Microcomputer Systems Corp, 432 Lakeside Dr, Sunnyvale, CA 94086. Tel: 408/733-4200.

Circle 200 on Inquiry Card

# PRODUCTS

## Raster Display System Produces 1M-Pixel Resolution From Over 4k Color Values



Resolution of 1,048,576 pixels (1024 pixels/line by 1024 lines) is achieved on the model GCT-3500 microprocessor based full-color graphics system. The result is higher clarity and more concise color delineation than previously attainable with computer generated raster scan displays. As many as four 19 or 25" (48- or 63-cm) specially built, high resolution CRT monitors can be operated from a single system. With the exception of boards designed particularly for this application, most of the series of plug-in boards in the 10-board capacity rack mountable chassis with central bus structure have been proven during use in earlier configurations. They include the microprocessor board, refresh memory, and computer interfaces. Of the specially designed boards, a module handles up to 8 memory planes and displays 256 different colors from an available 4096 values. Optional monitor control systems accommodate up to 12 memory planes and display 4096 colors from a selection of over 16M shades.

A proprietary user programmable graphics microprocessor, with 55-mnemonic instruction set, provides a 150-ns internal cycle time and manipulates graphics data at a 600-ns maximum instruction time. Of 4k 16-bit words of memory, all provided in RAM, 2k are assigned to the software package and the remaining 2k are for user programs. The system offers direct memory access data transfer from a host computer, selective erase, and flicker-free operation. Standard interfaces are available for most minicomputers. RS-232 compatible interactive peripherals include a keyboard with 16 function switches, joystick, trackball, and data tablet. An optional scroll/zoom plug-in board enables pixel by pixel scrolling or up to 8X picture enlargement. GRAFPAC II, a FORTRAN callable subroutine package, allows transfer of instruction sets in complete program blocks, thereby simplifying control and display generation programming. The package includes maintenance diagnostics software. **Genisco Computers,** 17805 Sky Park Circle Dr, Irvine, CA 92714.

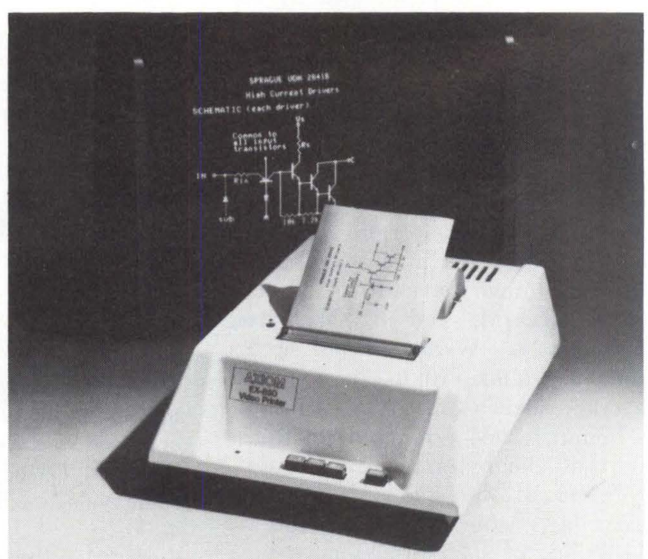
Circle 201 on Inquiry Card

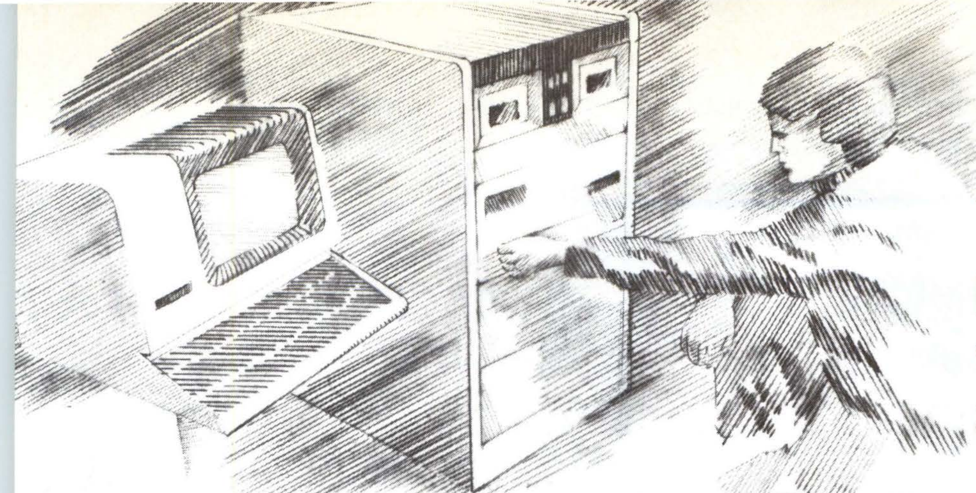
## Compact Printer Provides High Quality Reproduction Of Any Video Display Without Interface

With the EX-850 video printer, any monotone graphic or alphanumeric CRT display can be reproduced without hardware or software interface to the CRT. According to the manufacturer, the printer uses a unique video controller that connects directly to the video signal of any raster scan CRT display and samples information on the screen at high speed. Since conventional interfaces and standard codes are eliminated, the printer can reproduce whatever is on the screen, irrespective of language or character font. High quality permanent reproduction on inexpensive electrosensitive paper is produced by a 24-wire matrix, self-adjusting printhead with overlapping printer wires. A raster scan input from any black and white or color CRT terminal, TV, video monitor, or computer is acceptable to the printer.

Either an external command or a front panel button can initiate print operation. Other front panel controls permit selection of normal or high resolution and positive or negative image. Externally accessible controls in the rear of the unit include a gain trimmer for adjustment of incoming video signals to within the acceptable 0.5- to 10-V pk-pk range; a slice level trimmer to control line thickness for the desired contrast; a horizontal hold control; a raster select trimmer that adjusts the number of lines that will be accepted from the CRT for print out; and controls for selecting polarity of external sync signals, for adjusting input impedance, and for tuning out sensitivity to color burst signals (when copying from color displays). Power supply, video print controller, low paper detector, bell, and paper roll holder are included in the 16" D x 10" W x 4" H (41 x 25 x 10-cm) std unit with the printhead and all other electronics. Weight is 12 lb (5.4 kg). MTBF is claimed to be 11.6M lines. **Axiom Corp,** 5932 San Fernando Rd, Glendale, CA 91202.

Circle 202 on Inquiry Card





# TI Silent 700® or ANSI Compatible

## Emulates paper tape with DEC software at up to 9600 baud


# The Raycorder Cassette Terminal Model 6801

The Model 6801 Raycorder Cassette Terminal is a dual-cassette operating system capable of reading, writing, and copying data at switch selectable rates from 110 to 9,600 baud through a full duplex, asynchronous RS232C interface.

Operating under the control of a microprocessor with up to 4K of firmware, the Model 6801 has designed-in versatility never before available in a system of this type.

Connected to a serial port of a DEC PDP8 or PDP11 and given the proper address, it will emulate the typical paper tape reader/punch and perform the functions of program load, data logging, assembly, edit or duplication. Select one of two Texas Instruments Silent 700® modes, and tapes can be written, read, or copied that are completely compatible with the 733ASR but at much higher data rates.

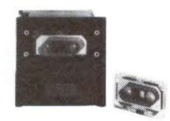
With its extension connector, the Model 6801 can be connected to any RS232C port without disturbing the device formerly connected there. With this feature, for example, tape storage can be added where only hard copy print out or CRT display had previously existed.

Utilizing two of Raymond's time-proven 6406 Raycorder cassette drives, the Model 6801 provides the ultimate in a reliable, flexible data storage and handling device for a multitude of applications. Detailed specifications will be provided on request.

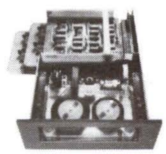
## For the OEM

Raymond's small tape drives, long the standard of the industry, are now available with all new electronics that make interfacing a cinch.

**Model 6406** for Philips Cassettes, redesigned with many new features at a lower cost.



**Model 6409** for Mini-Data Cassettes, now has a parallel interface and other changes you'll appreciate.



**Model 6413** for ¼-inch Data Cartridges, the newest member of the team is catching on fast.

Raycorder Products Division
**Raymond Engineering Inc.**
217 Smith Street
Middletown, Connecticut 06457
(203) 632-1000

*a subsidiary of Raymond Industries*

CIRCLE 93 ON INQUIRY CARD

## PRODUCTS

### DOT MATRIX IMPACT PRINTHEADS

With 100% duty cycles, 2 replacement heads feature 75M- and 100M-char lives for use with model 7040-T ticket printers and model 7040 journal printers, respectively. They consist of 7 ballistic clapper type solenoids which activate 7 printwires. Printwires strike the ribbon to form the char while the head is serially driven at a constant speed across the print area. Char width and density can be varied using software. Both can print continuously without overheating. **LRC, Inc,** Technical Research Pk, Riverton, WY 82501.

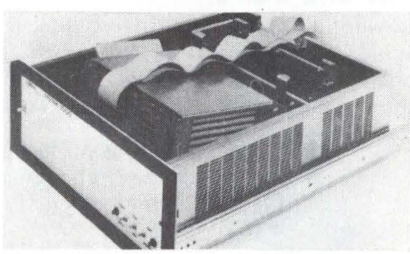
Circle 203 on Inquiry Card

### HIGH SPEED MULTIPLEXER

A line sharing device that can subdivide 38.4k-bit/s communications lines into multiple 9600-bit/s lines, the LSD 384 smart inverse multiplexer can be connected to IBM 370X frontend control units or to local control units in PIXNET data communications networking systems. The multiplexer includes microcomputer, channel interfaces, modem interfaces, and an integral LSI-96 9600-bit/s modem. **Paradyne Corp,** 8550 Ulmerton Rd, Largo, FL 33541.

Circle 204 on Inquiry Card

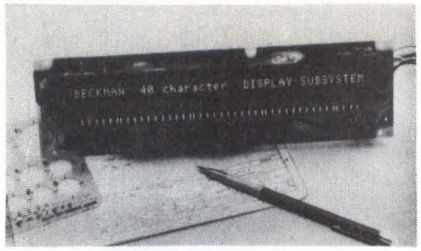
### HARD DISC COMPATIBLE ENCLOSURE AND INTERFACE



Compatible with the DEC RLV11 hard disc controller, the series 1000/RLV11 system contains a backplane/cardcage that is Q-bus, LSI-11, -11/2, and -11/23 compatible. The 11 x 4" (28 x 10-cm) backplane has connector rows 1 through 3 and 6 through 11 prewired to accept a total of 9 DEC Q-Bus compatible quad size or 18 half-quad cards. The rackmountable system enclosure [17 x 21.5 x 6.9375" (43 x 54.6 x 17.6213 cm)] also contains a switching power supply with 5 V at 25 A, 12 V at 3 A, and ±15 V at 1.5 A. **ADAC Corp,** 70 Office Tower Pk, Woburn, MA 01801.

Circle 205 on Inquiry Card

### PLANAR GAS DISCHARGE DOT MATRIX DISPLAY




The 40-char subsystem, driven by a single 5-V supply, has a std 8-bit parallel bidirectional bus interface and includes display, hardware, and software. Each char provides 100 ft-L (343 candela/m$^2$) of orange illumination. Char are dimmable and viewing angle is 130° min. Controlled by an Intel 8041A microcomputer, the subsystem accepts ASCII input. Char can be entered from left or right or randomly. **Beckman Instruments, Inc, Display Systems Div,** 350 N Hayden Rd, Scottsdale, AZ 85257.

Circle 206 on Inquiry Card

### GOLD INLAY OR COPPER ALLOY INSERT DIP SOCKETS

Construction of the 2xx-AG49D DIP uses nickel-silver alloy contacts with gold inlay on the contact area only, and tin overlay on the solder tail. The 2xx-AG29D model features low cost copper alloy contacts plated with tin lead and meets MIL-S-83734. Both additions to the 200 series low profile sockets are end to end and side to side stackable. Sockets are available with from 8 to 40 pins. **Augat Inc,** 33 Perry Ave, Attleboro, MA 02703.

Circle 207 on Inquiry Card

### ENCODED ASR-33 KEYBOARD REPLACEMENT

A 53-key encoded keyboard is a direct replacement for a 753 type keyboard. Switch layout of the M-53 keyboard is the same as standard ASR-33 format with hardwired keys for line feed, escape, and repeat. Encoded with MOS circuitry, 7-bit ASCII output, and std 2-key rollover, the keyboard interfaces via Cinch type 50-15-A-20 connectors; solder pads near the connector finger provide for alternate cabling arrangements. Options include u/lc, or uc alpha only. **Maxi-Switch Co,** 9697 E River Rd, Minneapolis, MN 55433.

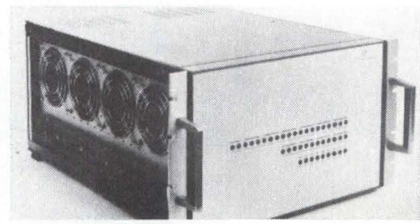
Circle 208 on Inquiry Card

### LOW PROFILE 2-SPEED S-D CONVERTER

True tracking type converters functioning from 50 to 1200 Hz without the need for external transformer modules, the 168F500 units feature industry std pinouts. Speed ratios are 1:36, 2:36, 1:4, 1:8, 1:16, 1:32, and 1:64, with resolution to 16 bits. Tracking rates are 720°/s; accuracy for the 1:36 speed ratio is ±0.41 min of arc (worst case). Std models accept 11.8- or 90-V rms inputs from synchros or resolvers with reference voltages of either 26 or 115 V rms, 50 to 1200 Hz. **Control Sciences, Inc,** 8399 Topanga Canyon Blvd, #303, Canoga Park, CA 91304.

Circle 209 on Inquiry Card

### DISC EMULATOR

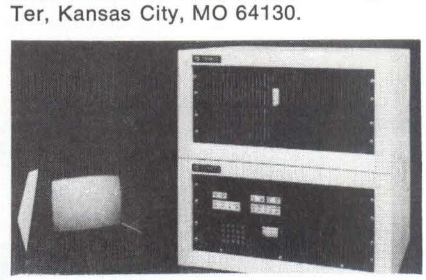


DE08 is a 256k-word solid state bulk memory system that emulates the DEC RF08 fixed head disc system. It is suitable for use in any situation that requires high speed memory swapping. Built around the company's std 16k-word memory boards, the emulator is packaged in a self-contained 10.5" (26.7-cm) high, 19" (48-cm) rack-mountable chassis. Power requirements are 115 Vac at 3.5 A max. Data access and transfer rates are 5.9 µs. **Computer Extension Systems, Inc,** 17511 El Camino Real, Houston, TX 77058.

Circle 210 on Inquiry Card

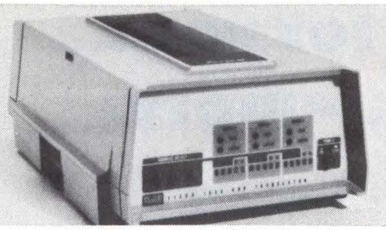
### CIRCUIT PATH TEST SYSTEM

Linking asynchronously with a host computer, model 1042 microprocessor controlled interconnect test system lists data in unit under test (UUT) language; test programs are in both UUT and analyzer language. Comprised of CRT operator console; control console with keypad, diskette drive, and alphanumeric printer; and switching console, the solid state system has a capacity of 128 terminations and is expandable to 16k terminations. **DIT-MCO International,** 5612 Brighton Ter, Kansas City, MO 64130.



Circle 211 on Inquiry Card

### IEEE 488-1978 BUS TO INSTRUMENT INTERFACE



A personality card located in the model 1120A IEEE translator permits the device to become the communications link between a variety of the company's instruments and the IEEE 488-1978 bus. The translator handles up to 3 interfaces; as many translators as necessary may be added to a system. The microprocessor based personality cards are each individually addressable, and are user transparent. **John Fluke Mfg Co, Inc,** PO Box 43210, Mountlake Terrace, WA 98043.
Circle 212 on Inquiry Card



### MULTIPLE I/O BUS CAPABILITY FOR MINICOMPUTER

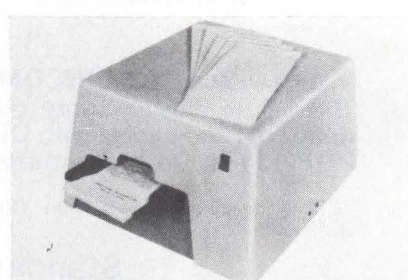
Multiple, medium speed I/O channel support for VAX-11/780 comouters allows connection of up to 4 Unibus adapters to the minicomputer. The multiple Unibus feature increases system throughput by permitting concentration of higher speed and lower speed peripherals on separate channels. Higher performance, short latency devices use 1 Unibus, while slower, char interrupt devices occupy another. This feature is supported by VAX/VMS operating software and diagnostic systems. **Digital Equipment Corp,** 146 Main St, Maynard, MA 01754.
Circle 213 on Inquiry Card

### MILITARY/COMMERCIAL 200-W POWER SUPPLIES

Military (MIL-E-5400) and commercial versions of single-output supplies consist of 5 models each, ranging from 5- to 48-Vdc output. Efficiency is 76 to 87% depending on output voltage. Commercial units are designed for a single-phase input with 115 Vac, 47 to 440 Hz; military versions are for 3-phase input, 115 Vac, 400 Hz. Operating temp ranges are 0 to 71 °C and −55 to 100 °C, respectively. Overload and short circuit protection are standard. **Century Electronics,** 5965 Washington Blvd, Culver City, CA 90230.
Circle 214 on Inquiry Card

### ALPHANUMERIC TICKET PRINTER/PLOTTER

Standalone dot matrix printer produces alphanumeric and graphic data on manually inserted 3.25" (8.26-cm) wide tab card sets. Microprocessor controlled model PK 970 requires only logic inputs (TTL level, parallel or serial ASCII, or RS-232), control signals, and line power. A stepper motor advances the ticket at 6 lines/in (2.4/cm) for alphanumeric data or in 0.110" (0.279-cm) increments for graphics. Line length may be 30, 37, or 49 char; char density may be 10, 12.4, or 16.5 char/in (4, 4.88, or 10.5/cm). **Practical Automation, Inc,** Trap Falls Rd, Shelton, CT 06484.



Circle 215 on Inquiry Card

# Another rule broken.

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Most PC connector series top out at about 50 contact pairs.

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They're whoppers.

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CONNECTORS

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TWX 910-494-2094

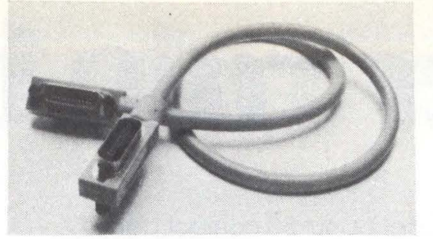
*Wire-Wrap—a registered trademark of Gardner-Denver Company.

Shown: JNK Series, with 70 pairs of .026" round tail contacts on .100" centers.

CIRCLE 96 ON INQUIRY CARD

## PRODUCTS

### IEEE 488-1978 INTERFACE BUS CABLE ASSEMBLY



Up to 15 instruments, peripherals, calculators, and computers interconnect in parallel to the IEEE 488 bus with the IEEE-488 assembly. Data are transmitted in a bit parallel, byte serial format. Data transfer is through the use of an interlocked handshake technique. A double-shielded cable increases protection from electrostatic and electromagnetic interference and a nickel plated housing offers resistance to corrosion. **National Electric Cable, Div of National Electric Control Co,** 16566 SW 72nd Ave, Portland, OR 97223.

Circle 216 on Inquiry Card

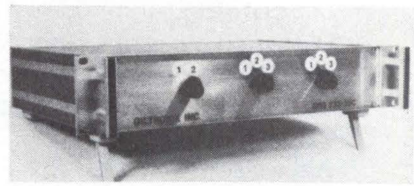


### DATA ENCRYPTION ALGORITHM SOFTWARE FOR ECLIPSE

Encode and decode operations which may be executed online or in the batch mode are included in a software package that contains all programs, subroutines, CLI macros, and help commands to allow immediate application to an Eclipse running RDOS or AOS. Routines may be used for encryption of disc files and mag tape dump files or interfaced to high level programs. A typ file encryption has a conversion time of 14 ms/64-bit block. **Gamma Technology, Inc,** 2452 Embarcadero Way, Palo Alto, CA 94303.

Circle 217 on Inquiry Card

### RS-232 SWITCHING AND MONITORING CONTROLLERS

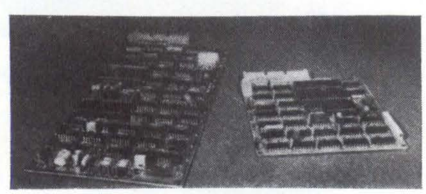


For technical control facilities and laboratories, GRS-232-SC, -2SC, and -3SC allow the user to switch and monitor any RS-232 interconnect system. Units mount in std 19" (48-cm) racks or can be used as desktop units. Basic -SC unit has 1 front panel rotary switch and 4 female 25-pin EIA connectors mounted on the rear panel for connection of cables as well as monitoring instruments. Monitoring and configuration options are available to switch 8 or 16 EIA pins. **Giltronix Inc,** 3156 Avalon, Palo Alto, CA 94036.

Circle 218 on Inquiry Card

### INTELLIGENT 5.25" FLOPPY DISC DRIVE CONTROLLERS

Preprogrammed intelligent controllers for 5.25" (13.33-cm) flexible disc drives provide 8-bit bidirectional or unidirectional buses for data, status, and control word transfers. Available in single-density, single-sided (FDC 100-5) and double-density single- or dual-head (FDC 200-5) models, the controllers use TTL and MOS LSI technology to perform all functions necessary for transfer of data between 1 to 4 drives and a host system and are compatible with any std 5.25" drive. **Siemens Corp,** 186 Wood Ave S, Iselin, NJ 08830.



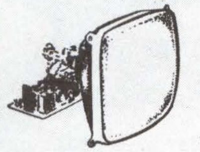
Circle 219 on Inquiry Card

# THE IMPORTANCE OF BEING FIRST

In today's fast-breaking terminal marketplace, getting there first with your product can decide its profit future. That's why it's important to design your terminal around a field-proven CRT module from an experienced manufacturer such as Motorola. Since we make more than 65 standard CRT module variations, in screen sizes from 5-inch to 23-inch, the chances are good that we already make one that fits your application.

## VARIETY IN 12-INCH

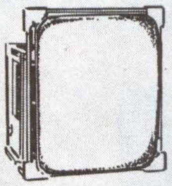
The popular 12-inch CRT is available in any of several ways: chassis or kit, economy or high performance, separate sync, composite or direct drive inputs, choice



of standard EIA phosphors, choice of scan frequencies, with or without anti-reflective faceplate.

## 15-INCH PERFORMANCE

The MD4000 series displays over 3,000 upper and lower case characters, including the 132-character-across wide-page printer format. Every line is sharp, even in the corners. StepScan™, 22 MHz bandwidth and dynamic focus are standard.



The M4408 displays a full page of upper and lower case text (6,000+ characters). Raster scan technique with TTL logic interface gives you low unit price and then saves again in your logic design costs.

## DEMONSTRATED MTBF

We go beyond calculating MTBF. Samples of each Motorola model are extensively tested, for thousands of hours under extreme conditions, to give you a demonstrated MTBF figure you can believe in. On our production lines, samples of every model are continuously monitored to duplicate customer life tests. Our customers report displays that are still going strong after logging over 40,000 hours.

## CALL TODAY

Call today to find out how Motorola can help you be first. ■ Santa Clara, CA (408) 988-3422 ■ Tustin, CA (714) 838-5621 ■ West Chicago, IL (312) 231-4400 ■ Richardson, TX (214) 231-9901 ■ Windham, NH (603) 898-5921 ■ Shrewsbury, NJ (201) 544-9541 ■ Baltimore, MD (301) 821-0062 ■ Overseas and Canada call West Chicago, IL (312) 231-4400 ■ TWX: 910-230-3117

**MOTOROLA INC.**

*Display Systems*

1155 Harvester Rd.
West Chicago, IL 60185

**CIRCLE 98 ON INQUIRY CARD**

MD3000—high performance 12-inch display module

## DIGITAL CASSETTE RECORDER

The 343CV digital cassette recorder accepts RS-232-C data, formats and writes data on cassettes, plays back, and transmits data in an RS-232 mode. Teletype data from a 20-mA current loop may also be recorded and read out. Baud rates of 110, 150, and 300 are available in both read and write modes and the unit will read continuously at 1200 baud. Each cassette stores

more than 72k words in a TTL or CMOS compatible format. **Memodyne Corp,** 220 Reservoir St, Needham Heights, MA 02194.
Circle 220 on Inquiry Card


## CASSETTE DATA RECORDING UNIT

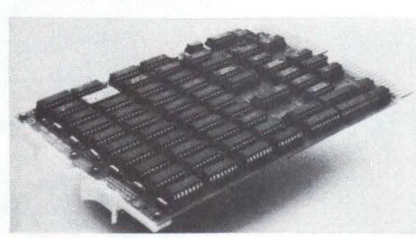
Dual-drive model 822 Datacassette employs microprocessor technology to supply intelligent storage and retrieval of 290k char. The 822 has switch selectable data rates to 2400 baud, RS-232 interfaces, full remote control of both drives, and optional ANSI/ECMA or TI recording format compatibility. The unit features automatic spillover from 1 drive to the other in both read and write modes; copy mode provides for automatic data flow from 1 drive to the other for tape duplication, merging, and text editing. **Techtran Industries, Inc,** 200 Commerce Dr, Rochester, NY 14623.
Circle 221 on Inquiry Card

## DC-DC CONVERTERS

Designed for 24-, 28-, and 48-V inputs, 36 models of encapsulated dc-dc converters feature lightweight, compact construction for PC card application. Available in 5- and 6-W, and 10- and 12-W models that output 5, 9, 12, 15, ±12, and ±15 Vdc, these converters are 65% efficient (typ) with a full-rated load. All models employ Pi type input filters, and have continuous 6-sided emi/rfi shielding and short circuit protection. **Computer Products, Inc, Power Products Div,** 1400 NW 70th St, Ft Lauderdale, FL 33309.
Circle 222 on Inquiry Card

## 32k-WORD MEMORY

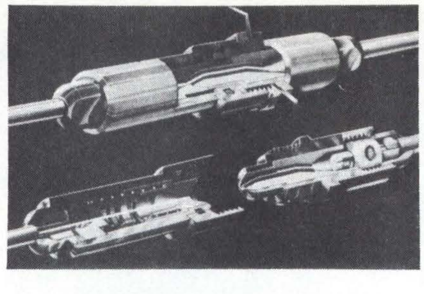
Storage capacity of the LSI-11/2 memory is enhanced with a systems bootstrap and diagnostics P/ROM. The P/ROM has memory sizing and diagnostics, and RX01 floppy disc bootstrap, an absolute binary loader, and a synchronous modem downline loader. Other standard features include 18-bit memory addressing, independent automatic refresh, switch selectable memory size (16k to 32k), and IC sockets. **Standard Engineering Corp,** 44800 Industrial Dr, Fremont, CA 94538.



Circle 223 on Inquiry Card

### FIBER OPTIC CONNECTOR

Optalign, designed for single fiber cable, holds light losses to less than 1 dB. The alignment element, based on a 4-rod glass array that is clean, inert, stable, and compatible with most commercially available fibers, permits fast, precise connections without the use of epoxies or matching liquids. The connection is immune to shock and vibration. **TRW Cinch Connectors,** 1501 Morse Ave, Elk Grove Village, IL 60007.



Circle 224 on Inquiry Card



### ENCODING SYSTEM FOR COMPUTER GRAPHIC DISPLAYS

RGB to NTSC color encoding system enables computer graphics or alphanumeric information to be displayed on std commercial color television monitors. Designed to encode high resolution RGB color graphic computer displays regardless of scan rates, the CCE-850 encoder may be used with any computer graphics system when NTSC video is required for video taping and/or distribution. The self-contained encoder system features a color reference test pattern and measures 1.75 x 17 x 8" (4.45 x 43 x 20 cm). **Lenco, Inc, Electronics Div,** 300 N Maryland St, Jackson, MO 63755.

Circle 225 on Inquiry Card

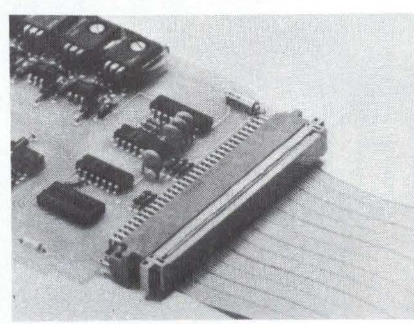
### 2-MIPS, 64-BIT COMPUTING ELEMENT

Designed for data manipulation, list/string processing, database management, and image processing applications, the F6401 computational processor provides a sustained processing speed of 2M instructions/s. Separate instruction, address, and data subprocessors operate in parallel at 250-ns cycle time to maximize throughput. 16 16-bit control registers, 16 28-bit address registers, 16 64-bit accumulators, and a 250k-byte RAM comprise the element. **Functional Automation, Inc,** 3 Graham Dr, Nashua, NH 03060.

Circle 226 on Inquiry Card

### EUROPEAN STANDARD INTERFACE CONNECTORS

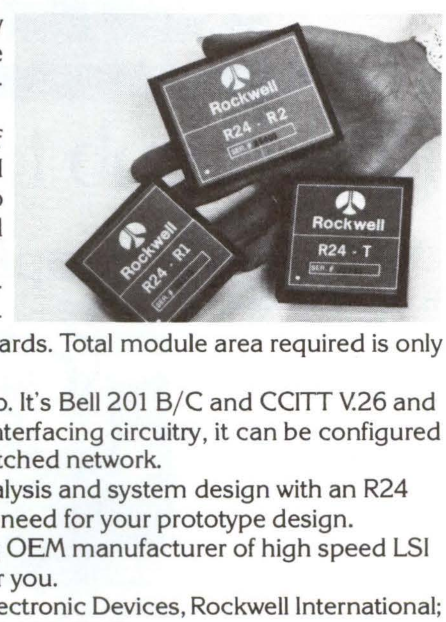
Two versions of 64-position European std interface connectors interface with DIN headers. One interfaces on grids of 2.54 x 2.54 mm, the other on grids of 2.54 x 5.08 mm. Both are available with or without snap-on strain relief that protects the connector during repeated insertion and extraction cycles. The connectors feature a 1-piece design that speeds installation—no wire stripping or soldering is required; a single crimping cycle terminates all 64 contacts. **T&B/Ansley Corp,** 3208 Humboldt St, Los Angeles, CA 90031.



Circle 227 on Inquiry Card

# Micro power

## The first modular 2400 bps modem. That's Rockwell Micropower.




Now you can easily and economically integrate a 2400 bps modem within the functional system of terminals or communications equipment.

The reason—the versatile design of Rockwell's R24, a synchronous MOS-LSI modem. The R24 divides its functions into three modules: one for the transmitter and two for the receiver.

Each module is encased in a plastic package that can be plugged into standard connectors or wave soldered onto system PC boards. Total module area required is only about 25 sq. inches.

R24 gives designers functional flexibility, too. It's Bell 201 B/C and CCITT V.26 and V.26 bis compatible. And with a minimum of interfacing circuitry, it can be configured for operation on leased lines or the general switched network.

Rockwell gets you started in performance analysis and system design with an R24 modem on an evaluation board. Everything you need for your prototype design.

A new generation of modems from the leading OEM manufacturer of high speed LSI modems. That's Rockwell Micropower working for you.

For more information, contact D-727-A8 Microelectronic Devices, Rockwell International; P.O. Box 3669, Anaheim, CA 92803, or phone (714) 632-3729.

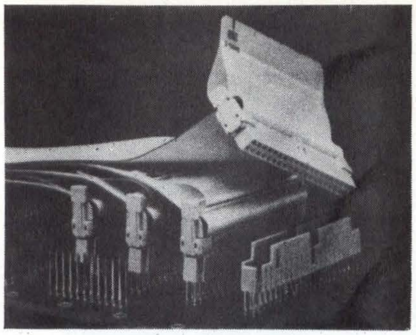
See us at TELECOM '79, Geneva, Switzerland, EIA/U.S. PAVILION, Stands #109, 110, 117, and 118.

**Rockwell International**

...where science gets down to business

CIRCLE 101 ON INQUIRY CARD

## 40-POSITION BACKPLANE SOCKET SYSTEM

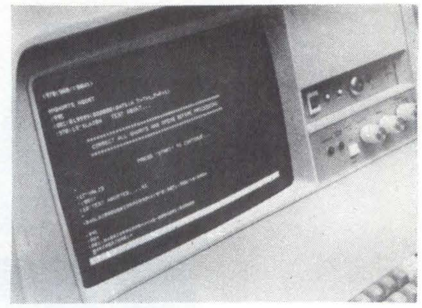


Designed to meet the requirements of the U.S. telecommunications industry, socket/header system is compatible with backplanes having 0.025" (0.635-mm) square posts on a 0.125 x 0.125" (3.175 x 3.175-mm) grid. The socket connector features double-wiping beam contacts spaced on the grid and utilizes insulation displacement contact to terminate round conductor flat cable with conductors on 0.0625" (1.5875-mm) centers. The mating header press fits over 2 rows of 22 0.025" square backplane pins on a 0.125 x 0.125" grid. **3M Co, Electronic Products Div,** PO Box 33600, St Paul, MN 55133.
Circle 228 on Inquiry Card



## PROGRAMMING STATION

Users of in-circuit test systems can edit and generate programs offline, thus freeing the model 400 and /A systems for full-time circuit board testing. The model 100 station is a microprocessor based edit terminal with a 48k-byte RAM, a 25-line x 80-col CRT display, an alphanumeric keyboard with edit pads and control keys, and 2 single-sided, single-density disc drives. All necessary software is supplied. **Plantronics/Zehntel, Inc,** 2625 Shadelands Dr, Walnut Creek, CA 94598.



Circle 229 on Inquiry Card

## CONTROL SYSTEM ARITHMETIC PROCESSING UNIT OPTION

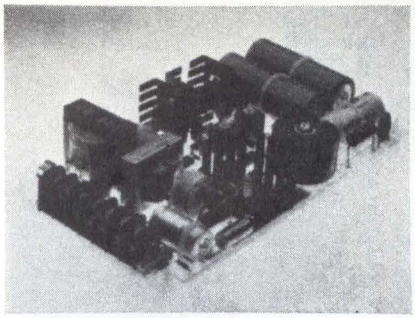
CP719 arithmetic processing unit fits into the CPU chassis of an EPTAK system, supplying 43 arithmetic, control, and conversion functions. APU offers fixed point single and double precision as well as floating point arithmetic. Execution times are 2 μs for basic functions to 6 ms for derived functions with 73 μs typ for a floating point multiply. A software driver provides the interface between user's control program and the APU **Eagle Signal Industrial Systems,** 736 Federal St, Davenport, IA 52803.
Circle 230 on Inquiry Card

## PROCESS I/O TERMINAL

SE100 measures, digitizes, isolates, and transmits industrial process data to computers, microcomputers, data terminals, and modems, and closes control loops with isolated DACs and switch closures. The modular data bus receives transducer scanners, converters, and interfaces. Direct byte serial porting, isolated RS-232-C serial transmission, and 20-mA current loop are available. Remote self-calibration and automatic cable break protection are included. **The San Diego Instrument Laboratory,** 7969 Engineer Rd, San Diego, CA 92111.

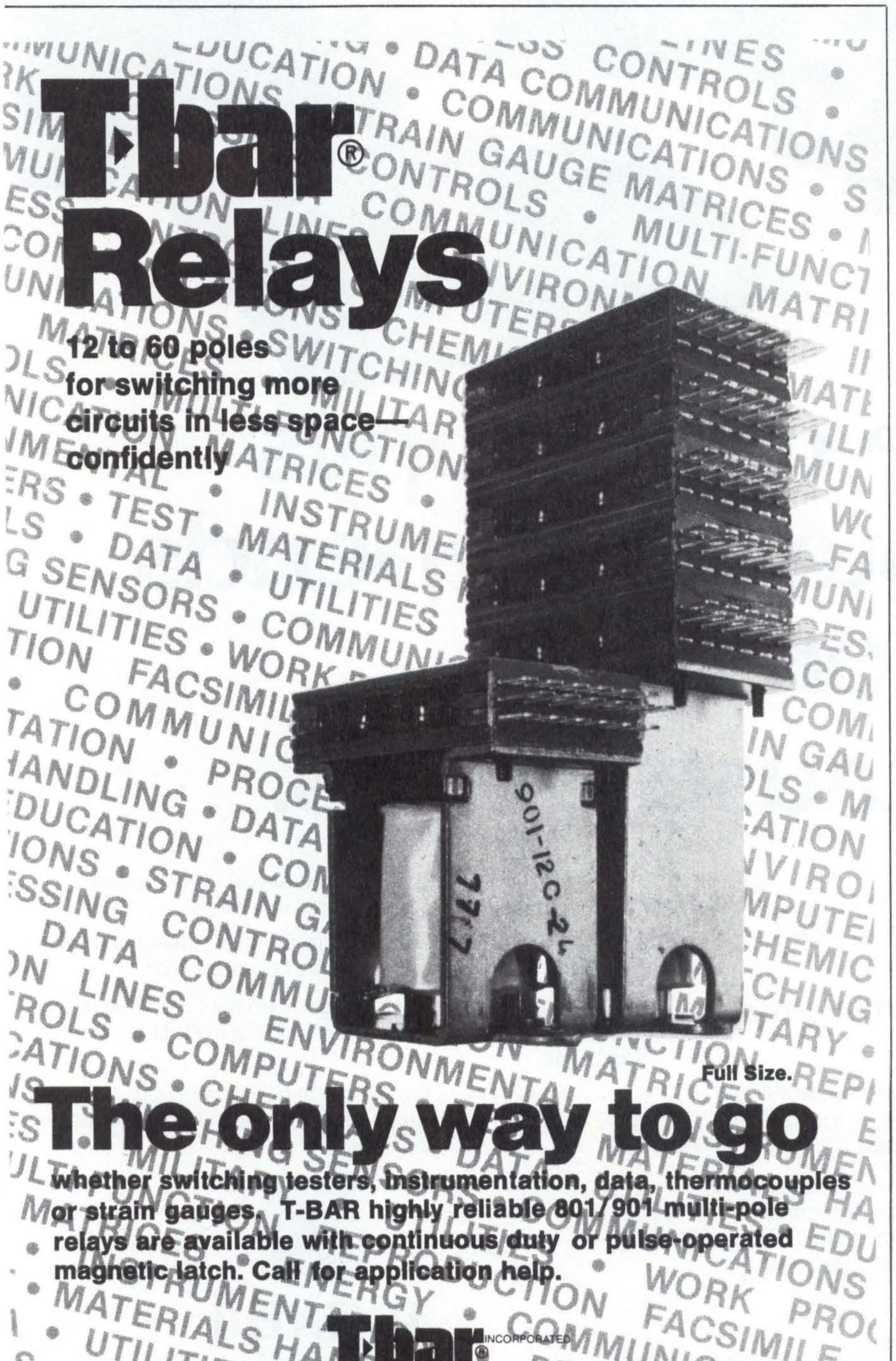
Circle 231 on Inquiry Card

## 50-W SWITCHED MODE POWER SUPPLY



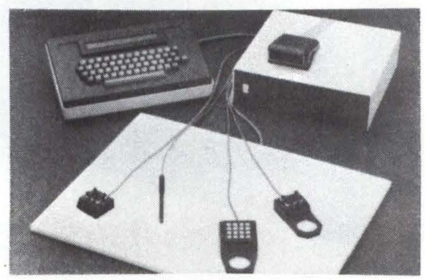
Using a half-bridge design, the SR1.5.10 achieves a min efficiency of 70%. It supplies 50 W (5 V at 10 A) of dc power; regulation is performed with ICs. Soft-start circuitry and electronic self-recovering overvoltage protection set to limit at 6.8 to 7 V are std. Output is current limited at approx 120% of full load current; emi/rfi is minimized with built-in line filters. Specs include load and line regulation of 0.1% and tempco of ±0.02%/°C. **Calex Mfg Co, Inc,** 3355 Vincent Rd, Pleasant Hill, CA 94523.

Circle 232 on Inquiry Card




## INTELLIGENT DIGITIZING SYSTEM

Microprocessor controlled Micro Datatizer™ processes and converts graphic data into a display or printout of X-Y length, volume, and other calculated physical or chart values. System consists of digitizing tablet, crosshair or pen cursor, and controller housing the microprocessor subsystem. The keyboard/display unit has a full set of TTY char and displays up to 16 alphanumeric char. Tablets are available from 6 x 6 to 42 x 60" (15 x 15 to 107 x 152 cm) with resolutions of 0.001 or 0.01" (0.025 or 0.25 mm). **GTCO Corp,** 1055 First St, Rockville, MD 20850.



Circle 233 on Inquiry Card

## VOICE RECOGNITION AND RESPONSE UNIT

The standalone MIKE recognizes 16 words or short phrases and can respond with an aggregate of 8 s of audio messages. The recognition memory expansion option allows 10 additional 16-word recognition vocabulary sets to be stored internally, and the response memory expansion option doubles audio response capability. A set of system commands effects control from an external computer. The I/O interface contains both an RS-232-C serial port and an 8-bit parallel port. **Centigram Corp,** 155A Moffett Pk Dr, Suite 108, Sunnyvale, CA 94086.

Circle 234 on Inquiry Card

## PRINTER/PLOTTERS FOR MOBILE APPLICATIONS

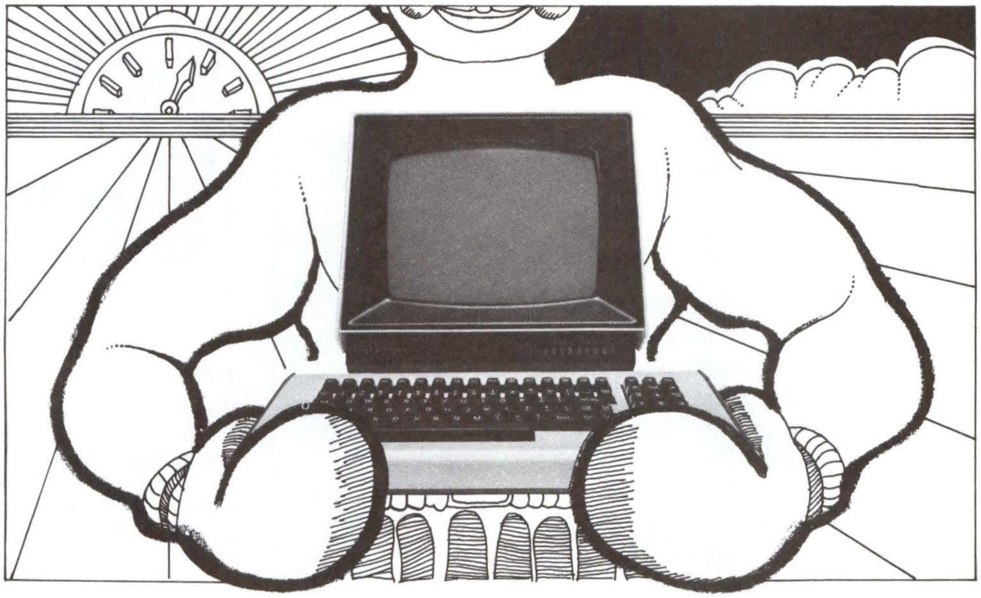
Electrostatic printer/plotters can run at a 30° tilt, altitudes up to 12,000 ft (3600 m), and ambient temperatures of 0 to 50 °C, and then can withstand a shock of 2 Gs. Heat dissipation is less than 1000 Btu/h (1055M joules). Nonoperating environmental specs provide for 45° tilt, temperature range of −40 to 70 °C, and shock of 15 Gs. Model 3210A plots with 200-dot/in (79/cm) resolution; the 3110A's resolution is 100 dots/in (39/cm). Both print 1k 132-col lines/min on 11" (28-cm) wide roll paper. Printing an 11 x 8.5" (28 x 22-cm) page in 3.9 s, they deliver up to 15 cut pages/min. **Versatec, a Xerox Co,** 2805 Bowers Ave, Santa Clara, CA 95051.

Circle 235 on Inquiry Card



CIRCLE 100 ON INQUIRY CARD

# ANNOUNCING A DEC®-DEFYING FEAT:



# DATAMEDIA BEATS THE HEAVY WAIT.

If you've been waiting, waiting, waiting for DEC's VT 100, you know what a heavy burden that places on your operations. Now there's hope, because Datamedia just beat DEC to the punch with its new DT 80/1 terminal.

The DT 80/1 not only matches the VT 100 feature for feature, but also takes a big step ahead, by adding full printer control.

Here's another jab: The DT 80/1 gives you the freedom to key in a split screen, double-size characters, and even limited graphics. In white-on-black or black-on-white.

The CRT screen has other special moves, too, like underline, blink, protect and dual intensity.

The DT 80/1 carries all these features in a very compact frame. It measures just 14" x 14" x 14," so it fits anywhere the VT 100 would fit. And the space flexibility of a detached keyboard is standard.

Like all Datamedia terminals, the DT 80/1 is engineered to run cooler and last longer, without the need for a noisy fan. In fact, we're so confident of its reliability, we've even given the DT 80/1 a full one-year warranty. Just what you'd expect from the company whose products have been Datapro-rated #1 for performance for the past two consecutive years.

Lighten up the burden of waiting. Get the DT 80/1 now. The coupon below will help you get started.

Please send me more information on your new DEC-compatible DT 80/1.

Name____________________

Company____________ Phone________

Address____________________

City________ State______ Zip______

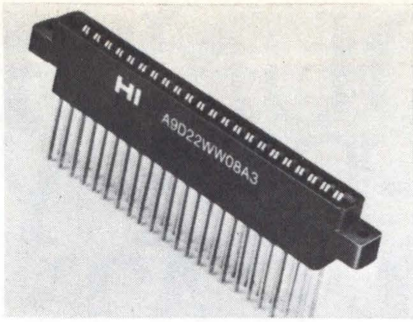
**Datamedia Corporation**

7300 N. Crescent Blvd., Pennsauken, N.J. 08110
Tel: (609) 665-2382 TWX: 710-892-1693

**CIRCLE 105 ON INQUIRY CARD**

### CARD EDGE CONNECTORS

Double readout connectors located on a 0.156 x 0.188" (0.396 x 0.478-cm) grid are available in 10, 15, 18, 22, 28, 30, and 40 positions for use in telecommunications applications. The device contains rugged bifurcated contacts with 0.031 x 0.062" (0.079 x 0.157-cm) wirewrap tail. Options are 10-, 15-, 30-, and 50-$\mu$in (0.25-, 0.38-, 0.76-, and 1.27-$\mu$m) full gold plating and selectively plated copper nickel alloy contacts. Insulators are molded




in UL94V-0 thermoplastic materials. **Holmberg Inc,** 17071 Murphy Ave, Irvine, CA 92714.
Circle 236 on Inquiry Card

### MICROPROCESSOR CONTROLLED PORTABLE DATA LOGGER

The PDL data logger, a portable cassette recording system, permits acquisition of as many as 8 (optionally 16) analog channels of information. Requiring 120 Vac, 60 Hz, the unit is factory programmable to provide special sampling rates, preliminary data reduction, and statistical analyses as the data are captured. A crystal controlled clock with battery backup permits time chronology in the event of power failure. **Schultz Instruments, Inc,** PO Box 13382, Gainesville, FL 32604.

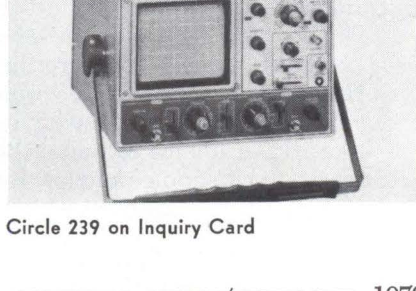
Circle 237 on Inquiry Card

### 1-MHz V-F CONVERTER

Modular voltage to frequency converters are factory trimmed to 0 and full-scale accuracy of better than 0.02%. The 4719 and 4719-01 both guarantee 0.02% nonlinearity, 50% overvoltage, and 100-dB dynamic range. The 4719 has ±50%-ppm/°C tempco, and the 4719-01 a ±25%-ppm/°C tempco. Outputs of both are TTL, CMOS, and HNIL compatible. Operating range is —25 to 85 °C, storage range is —55 to 125 °C. **Teledyne Philbrick,** Allied Dr at Rte 128, Dedham, MA 02026.
Circle 238 on Inquiry Card

### 20-MHz DUAL-TRACE OSCILLOSCOPE

An X10 magnifier on model 1520 20-MHz dual-trace oscilloscope isolates and expands any portion of the displayed waveform while maintaining relative time base calibration. Vertical sensitivity is 5 mV/div; 19 calibrated sweep time ranges covering 0.5 $\mu$s/cm to 0.5 s/cm are user selectable. Choices for trigger source capabilities include channel A, channel B, external, internal, or line—all with either positive or negative slope. **Dynascan Corp, B&K-Precision Group,** 6460 W Cortland St, Chicago, IL 60635.



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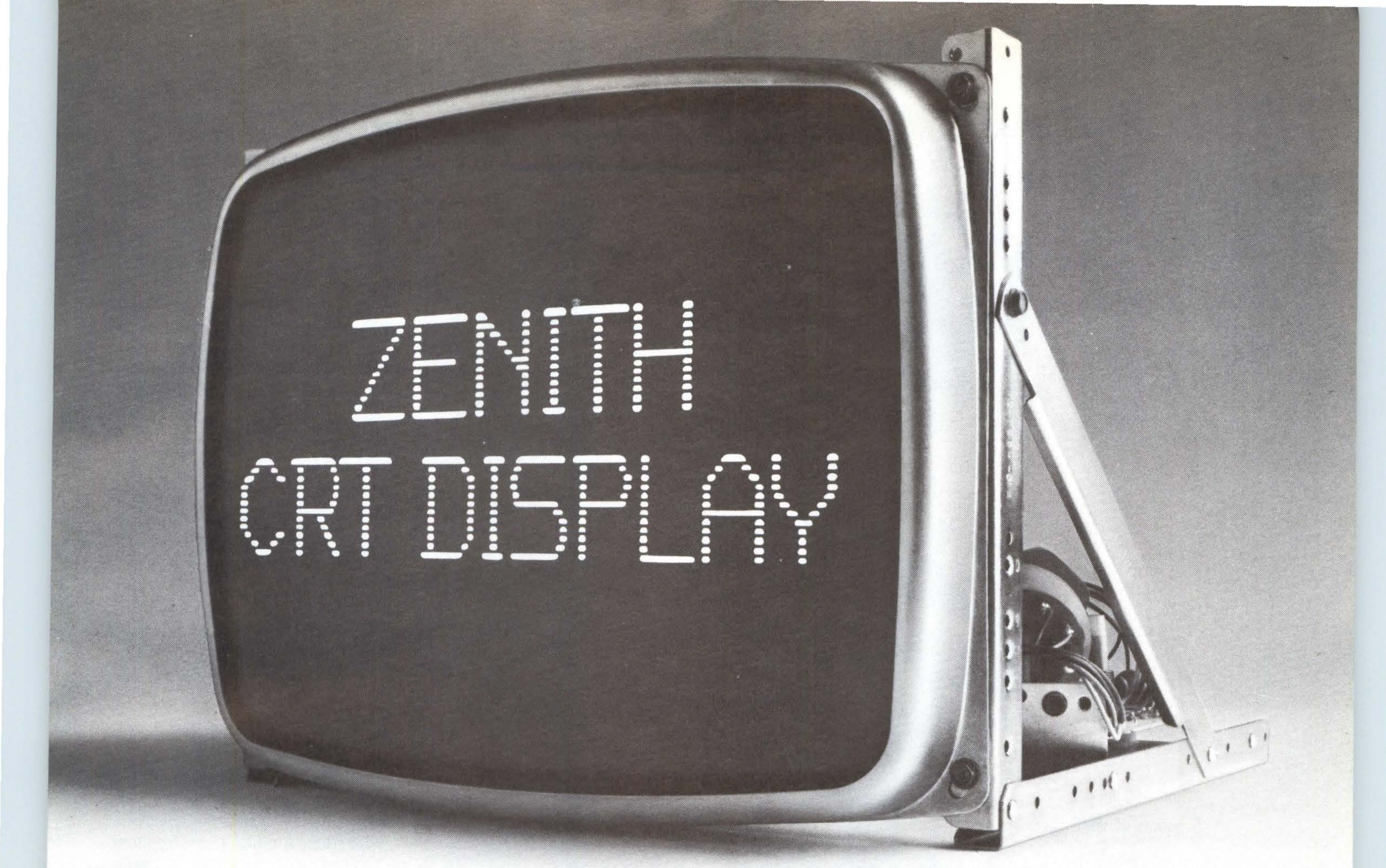



# The read-out is quality.

Quality is what has made Zenith famous for over sixty years and number one in the television industry. It's that quality, that commitment to excellence – that insures the reliability of every product we make.

Our manufacturing facilities, laboratories, equipment, procedures, experience and know-how give you the quality and reliability that you look for in a CRT Display. A CRT Display that will hold up under really tough operating conditions.

And to all this, our people add the personal service and special attention you want from your CRT Display source.

**Exhaustive testing**

Our testing insures that every component operates to exacting Zenith standards. Exhaustive computer analysis, electron microscope and thermograph scan tests are only a sample of what we do.

Our environmental lab tests Zenith CRT Displays for thousands of hours under extreme humidity, vibration, altitude and temperature conditions.

Zenith CRT Displays are designed not only to meet our exhaustive testing requirements, but your demanding specifications as well.

**Application engineering**

Every CRT Display we design has our customers in mind. Before our engineers even begin new circuit layouts, we'll meet with you and find out what your exact needs and specifications are.

**Advanced componentry**

Components in the CRT Display are designed with reserve capacity for low maintenance and continued reliability.

The Zenith CRT Display is equipped with a Zenith designed and built deflection transformer. It not only gives a consistent scan, but it is also embedded in epoxy for long-term reliability and the elimination of high frequency squeal.

**Important Zenith Features**

The Zenith CRT Display is precision engineered. No linearity controls are required and the CRT Display's vertical and horizontal synchronization is automatic.

The Zenith CRT Display frame can be adjusted to virtually any angle you want. This will satisfy many customer requirements without having a frame custom designed.

But we do welcome the opportunity to meet all your special requirements.

**Zenith tradition**

At Zenith we'll make sure you get the same service, quality and reliability in your CRT Display that we've been giving our customers for over sixty years.

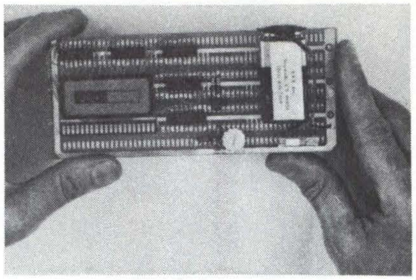
For further information and specifications, write CRT Display Engineering Division, Zenith Radio Corporation, 1000 Milwaukee Avenue, Glenview, Illinois 60025, or call 312-773-0074.

ZENITH®

**The quality goes in before the name goes on.®**

**CIRCLE 107 ON INQUIRY CARD**

## 10-SEGMENT LIQUID CRYSTAL DISPLAY

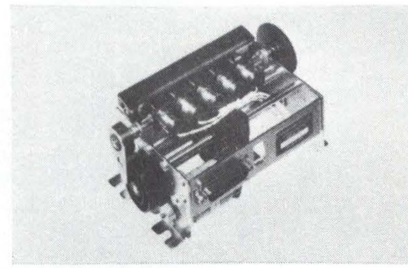


Each of the 10 segments in the 2210 AN analog-digital LCD has an integral digit outlined within it. The 2" (5-cm) wide display provides numbered cursor or continuous bar display. Segments may be cascaded for larger bar graphs. The LCD is available with black on pewter or white on clear for color filter backlighting or reflective use. An IC driver is available for ease of integration and application. **UCF Inc,** 20 N Main, Norwalk, CT 06854.
Circle 240 on Inquiry Card



## 40-COL LINE PRINTER MECHANISM

Model DMI-40 line printer mechanism will print any size font or graphics using any electronic drive circuitry. Mechanism uses five 12-Vdc solenoids, which when moved across the paper print 1 row of dots. A line of characters requires 7 passes plus 2 for the line space. These 9 passes require 0.5 s. Solenoid life is 20M char at 14 dots/char, while printer life is 10M print lines. **Data Machines International, Inc,** Tower Bldg-Terrace Hill, Ithaca, NY 14850.



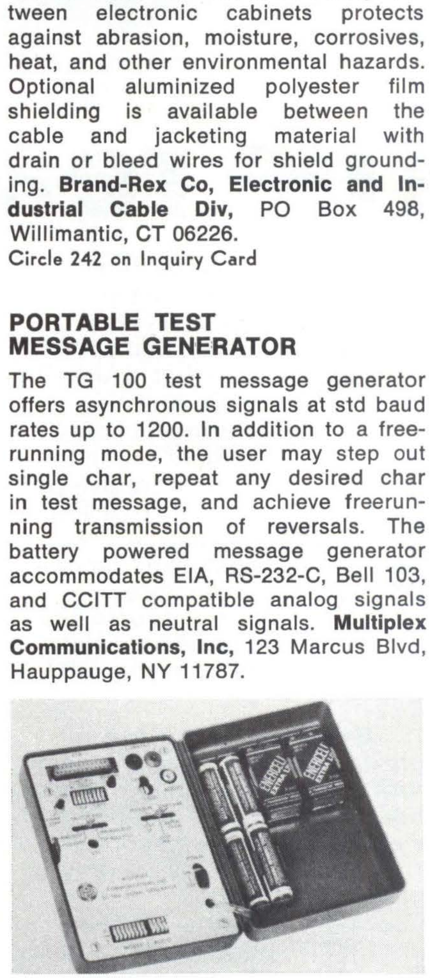
Circle 241 on Inquiry Card

## JACKETED FLAT CABLES FOR INTERCABINET WIRING

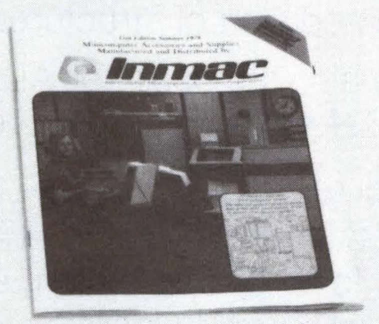
Line of PVC jacketed tape cable and ribbon cable for external wiring between electronic cabinets protects against abrasion, moisture, corrosives, heat, and other environmental hazards. Optional aluminized polyester film shielding is available between the cable and jacketing material with drain or bleed wires for shield grounding. **Brand-Rex Co, Electronic and Industrial Cable Div,** PO Box 498, Willimantic, CT 06226.
Circle 242 on Inquiry Card

## PORTABLE TEST MESSAGE GENERATOR

The TG 100 test message generator offers asynchronous signals at std baud rates up to 1200. In addition to a free-running mode, the user may step out single char, repeat any desired char in test message, and achieve freerunning transmission of reversals. The battery powered message generator accommodates EIA, RS-232-C, Bell 103, and CCITT compatible analog signals as well as neutral signals. **Multiplex Communications, Inc,** 123 Marcus Blvd, Hauppauge, NY 11787.



Circle 243 on Inquiry Card


# One way to order everything (all day on the phone)

# Our way to order everything (10 minutes on the phone)

Before he bought from Inmac, one customer required a pile of catalogs second only to Mt. Everest.

When the time came, he'd know just where to look for supplies.

A disk pack?
He'd go right to that 35-pound catalog under the philodendron.

A CRT stand?
Right to the furniture catalog. (Too bad he didn't read the fine print that said "2-month wait".)

EIA cables?
In the catalog that looked like last year's winning entry in the stump-the-engineer contest.

One day he needed a disk pack. And a CRT stand, 5 EIA cables, one box of thermal paper, 6 print-wheels and a harmonica ribbon.

If he didn't get them quick, he couldn't finish the Big Project. And top management was really breathing down his neck.

By the time he got all the catalogs together, figured out what would work with what, and made all the calls . . . 9 a.m. became 9 p.m.

And part of his order got stuck between Texas and Terre Haute.

Never again.

So he subscribed to the Inmac catalog. After all, 70 pages wasn't much for every supply he needed. Plus he could store it in a drawer.

He got rid of almost all those other catalogs. But his office looked empty. So he went out and bought a poster of Nepal.

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**CIRCLE 109 ON INQUIRY CARD**

# PROGRAMMING MICROCOMPUTERS / Oct. 22-26, 1979

E) PASCAL-V
- general concepts of data types
- user-defined data types
- scalar data types
- arrays
- exercise: use of data types

F) PASCAL-VI
- records
- sets
- pointers
- dynamic storage
- lab

G) PASCAL-VII
- sequential and text files
- formatting
- list processing
- interfacing to peripherals
- recursion
- advanced features–extensions
- survey of PASCAL implementations
- exercise: building a simple translator

3. High-level languages

Having learned one language, you will now be presented with a generic approach to programming languages. This approach will enable you to grasp the essential features of new languages in a matter of days.
- general approach to learning languages including PL/M and PL/Z
- introduction to ADA
- exercise: ADA program

4. Compilers and optimization

A brief introduction to compiler design and organization to illustrate trade-offs in language design and use. This session's objective is to enable you to utilize high-level languages in the most effective way.
- design and organization of compilers
- what good compilers will and won't do for you
- programming techniques to improve performance
- space/time trade-offs
- examples from LSI-11,Intel 8085, P-Code Machines

5. Evaluation of languages
- language comparison
- when and when not to use high-level languages

6. Summary
- new developments in languages and their use in small computers

## Course materials:

Specially prepared course notes, programming aids, and the following text are provided for class use and future reference:

*Programming In PASCAL* by P. Grogono.

## Tuition, schedule and continuing education credits

Tuition is $600. This includes course notes and text, as well as Tuesday evening reception. The seminar is scheduled for 8:30 a.m. Monday, October 22, 1979, through 4:30 p.m. Friday, October 26, 1979.

3 continuing education units will be offered by Polytechnic Institute of New York to participants completing the course.

## Further information

For additional information on course objectives and intended audience, you can call the course coordinator, Mr. Poonen, at 617/493-3537. For administrative information, call the Institute for Advanced Professional Studies at 617/964-1412. Participants are urged to register early as enrollment is limited.

## In-house programs:

This workshop plus a variety of other customized technical and management courses are available for on-site presentation. Contact Donald French at (617) 964-1412 for details.

## Course Registration Form

Please register me for the following course, PASCAL PROGRAMMING FOR MINI AND MICROCOMPUTERS co-sponsored by Polytechnic Institute of New York and Institute for Adanced Professional Studies:

- ☐ Oct. 22-26, Ramada Inn, Woburn, MA
- ☐ Dec. 3-7, Holiday Inn, Palo, Alto, CA
- ☐ Apr. 25-26, May 1-3, 1980, White Plains, NY
- ☐ Sorry, I cannot attend — but please add my name to your mailing list.

Tuition is $600. Make checks payable to Institute for Advanced Professional Studies.
*Please make room reservations early, directly with the hotel.*

Name ____________________ Job title ____________________

Employer ____________________ Business phone ____________________

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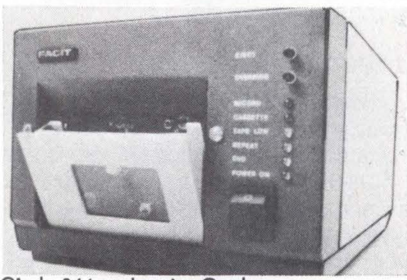
*Return this segment to:* Institute for Advanced Professional Studies
One Gateway Center, Newton, MA 02158 Tel. (617) 964-1412

CIRCLE 110 ON INQUIRY CARD

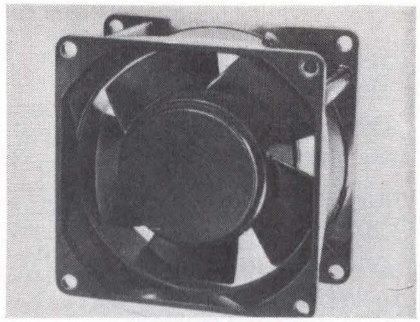
### DATA LOGGING CASSETTE TAPE UNIT

The 4208 tape cassette unit, compatible with the 4070 tape punch, takes care of all tape handling and data formatting internally, and allows fully asynchronous communication over its interface. Battery backup for buffer memories and extensive check routines provide high grade data integrity. Features include ECMA 34/Silent 700[R] compatibility, 500-char/s average transfer speed, 230k-char/track storage capacity, write and read functions in the same unit, and tape low and tape end indications. **Facit Data Products,** S-105 45 Stockholm, Sweden.



Circle 244 on Inquiry Card

### LOW PROFILE MIL SPEC COOLING FAN



The MIL-80 fan is a MIL-B-23071 version of the Sprite[R] fan. It delivers up to 56 $ft^3$/min (0.03 $m^3$/s) of cooling air on 115 or 220 Vac, 400 Hz, using the same motor as in the Spartan fan. The Mil Spec fan has an all metal blade, ensuring operation at amb temps up to 125 °C. A tubeaxial design combines motor and impeller in a single housing, giving the fan an outside diameter of roughly 80 mm. **Rotron Inc,** Woodstock, NY 12498.

Circle 245 on Inquiry Card



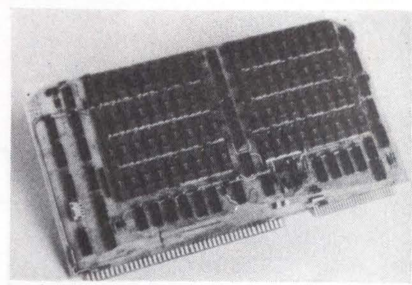
### ROM-P/ROM DEVELOPMENT SYSTEM

Logic to be burned into ROMs and P/ROMs can be debugged using the DS100 diagnostic tool, which emulates the performance of these memories in bit-slice microprocessors. It can also diagnose products containing these memories after they have failed. The large scale development system consists of the DS100-1 remote unit and the -2 with high speed RAMs. Max expansion is to 64k address locations times a max word length of 480 bits. **Hilevel Technology, Inc,** Park Irvine Business Ctr, Bldg 10, 14661A Myford Rd, Tustin, CA 92680.

Circle 246 on Inquiry Card

### MULTIBUS COMPATIBLE STATIC RAM BOARDS

Available in CMOS or NMOS, MR 80 static RAM boards are Multibus compatible. Configured as 8 banks of 4096 x 1 static RAM chips, the boards can service 8- or 16-bit CPUs. The CMOS version with 8k, 16k, or 32k bytes provides up to 96-h battery backup. The NMOS version is available in 16k- or 32k-byte sizes with optional parity checking/generation. Features of both boards include 1M-byte address decoding, and access times from 300 to 550 ns. **Comark Corp,** 257 Crescent St, Waltham, MA 02154.



Circle 247 on Inquiry Card

### CARTRIDGE MODULE DISC DRIVE

The 1667 CMD drive is composed of an 8M- or 16M-byte removable front-loading platter with 2 fixed platters of 8M, 16M, 48M, or 80M bytes for total capacities of 16M, 32M, 64M, or 96M bytes. Avg random access time is 30 ms at a rotational speed of 3600 r/min and an avg latency time of 8.3 ms. Data transfer rate is 1.2M bytes/s. Microprocessor control logic features fault monitoring and detection capabilities. **Harris Corp, Data Communications Div,** 16001 Dallas Pkwy, Dallas, TX 75240.

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# PROTECT YOUR SOFTWARE with EMI SHIELDED HARDWARE

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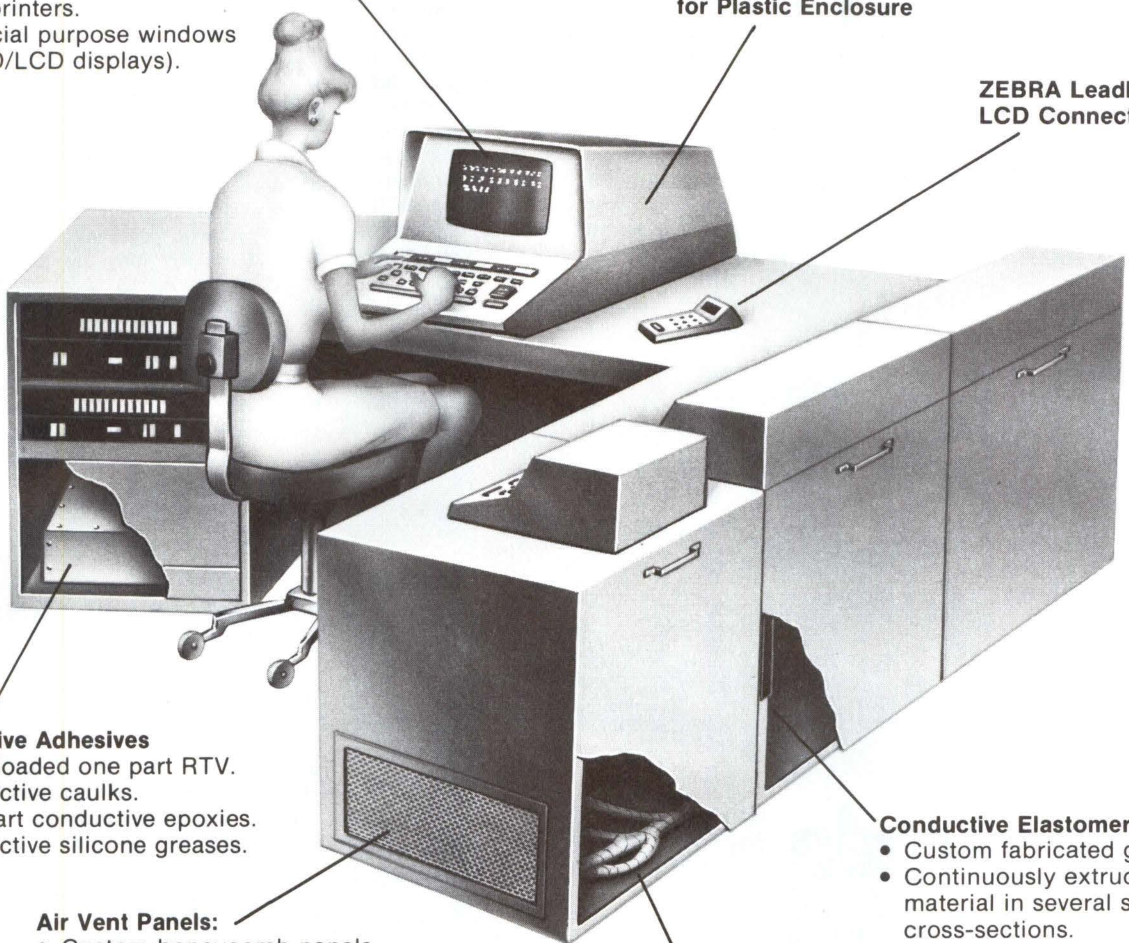

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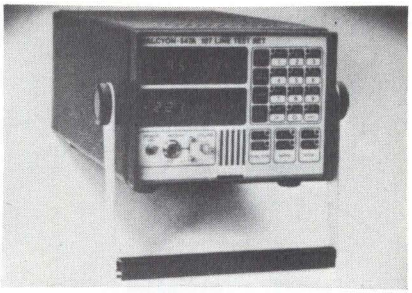
**CIRCLE 112 ON INQUIRY CARD**

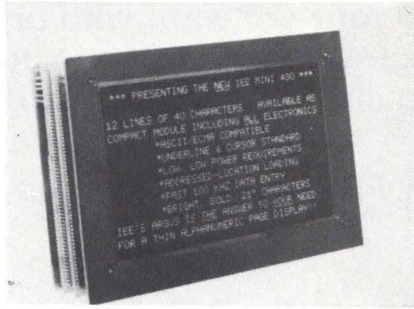
### AUTOMATIC LINE TEST SET

Operator errors are virtually eliminated using the 547A 107 which automatically follows the test sequence of the dial-up 107 test line. The microprocessor based instrument tracks the sequence and makes all appropriate tests. As each test is made, measurement results are identified and displayed in real time on dual alphanumeric displays. The device also stores all test results for display upon command at the end of the test. It operates in a "store-all/forward-all" mode, and has last-number recall. **Halcyon, Inc,** 2121 Zanker Rd, San Jose, CA 95131.



Circle 249 on Inquiry Card

### PAGE SIZE ALPHANUMERIC PANEL DISPLAYS



Pair of jitter free dc plasma displays offers 480 and 320 char, each with 40 char/line. Both have 0.21" (5.3-mm) char in a 5 x 7 dot matrix and present a neon-orange (or red) display. Std features are an editing cursor, 100-kHz data loading rates, and 120° viewing angles. It requires <30 W, offers 30k-hour life, is 2.75" (6.99 cm) deep, and operates with a std TTL/ASCII interface. **Industrial Electronic Engineers,** Inc, 7740 Lemona Ave, Van Nuys, CA 91405.

Circle 250 on Inquiry Card

### HIGH SPEED ELECTROSTATIC RECORDER

Capable of reproducing up to 32 channels of measurement data while simultaneously printing grids and alphanumeric annotation, the ESR-200 has a resolution of 200 dots/in (79/cm) across the 11" (28-cm) wide paper and 250 dots/in (98/cm) in the direction of paper motion. Recorder runs synchronously from 0.25 to 10 in (0.64 to 25 cm)/s and displays measurement or signal data at rates up to 2500 samples/s/channel. **Gould Inc, Instrument Div,** 3631 Perkins Ave, Cleveland, OH 44114.

Circle 251 on Inquiry Card

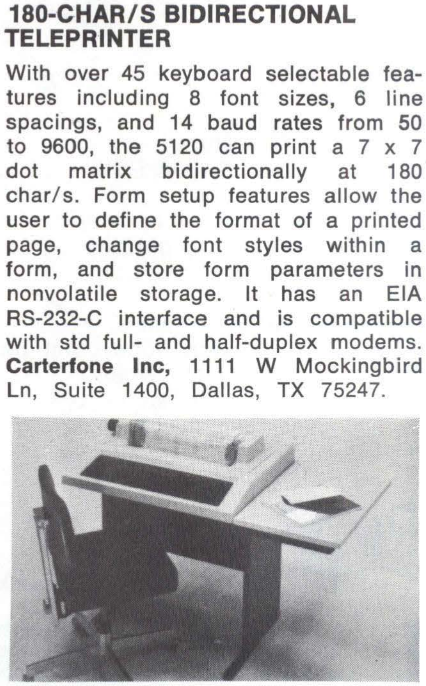
### DUAL-OUTPUT, 300-W SWITCHING POWER SUPPLIES

Features of SD300 series dual output switching power supplies include 117/234-Vac input and common mode emi suppression. One output is always 5 V at 60 A with overvoltage protection; second output may be the same or 12 V at 16 A, 15 V at 12 A, 18 V at 10 A, 24 V at 7 A, or 28 V at 6 A with optional overvoltage protection. All models have 0.1% line and load regulation. Ripple and noise is 50 mV pk-pk for outputs less than 15 V and 100 mV pk-pk for outputs 15 V or greater. **Deltron, Inc,** Wissahickon Ave, North Wales, PA 19454.

Circle 252 on Inquiry Card

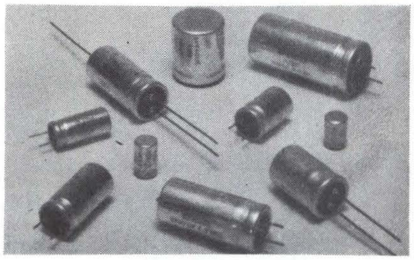
### 180-CHAR/S BIDIRECTIONAL TELEPRINTER

With over 45 keyboard selectable features including 8 font sizes, 6 line spacings, and 14 baud rates from 50 to 9600, the 5120 can print a 7 x 7 dot matrix bidirectionally at 180 char/s. Form setup features allow the user to define the format of a printed page, change font styles within a form, and store form parameters in nonvolatile storage. It has an EIA RS-232-C interface and is compatible with std full- and half-duplex modems. **Carterfone Inc,** 1111 W Mockingbird Ln, Suite 1400, Dallas, TX 75247.



Circle 253 on Inquiry Card

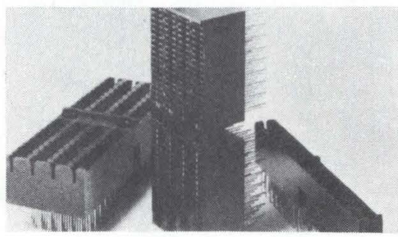
## VERY LOW INDUCTANCE ELECTROLYTIC CAPACITORS



Tubular Extralytic[R] capacitors feature low equivalent series resistance, inductance, and impedance. Type 672D have dia to 0.625" (1.59 cm); type 673D have 0.75, 0.875, and 1.0" (1.91-, 2.22-, and 2.54-cm) dia. Inductance of the aluminum capacitors is between 5 and 10 nH for type 672D and between 15 and 25 nH for the 673Ds. Capacitors with dia >0.484" (1.23 cm) are available with an optional third lead attached to the top of the can to anchor capacitors to board. **Sprague Electric Co,** 555 Marshall St, North Adams, MA 01247.
Circle 254 on Inquiry Card

## 72- AND 288-PIN CONNECTOR BLOCKS

Selective gold plating and a long wiping action through a 0.450" (11.43-mm) deep card slot achieve high reliability for 72- and 288-pin connector blocks. Contact resistance is 0.025 Ω max and the max current rating is 3 A. Constructed with copper alloy contacts and a black phenolic insulator, these connectors have an operating temperature range of −55 to 120 °C. Options include either slotted or closed ends, highlighted contact identification, or no contact identification. **Viking Connectors, Inc,** 21001 Nordhoff St, Chatsworth, CA 91311.



Circle 255 on Inquiry Card

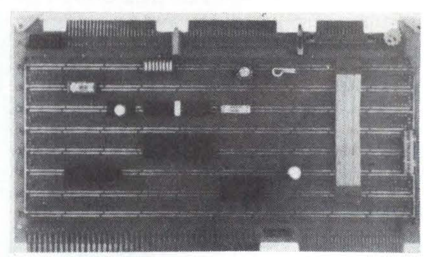
## INTELLIGENT VIDEO TERMINAL CONTROLLERS

Single-board BLC-8228 with a 5 x 7 matrix and 8229 with a 7 x 9 matrix provide an 80-char x 24-line display and a full 128 ASCII char set. Both have full software cursor control and programmable char display for blinking, inverse video, or alternate char. Std control functions include editing, formatting, and scrolling. Components are an 8080A CPU with 2k bytes of std control firmware, screen refresh memory, char attribute memory, and 1k bytes of scratchpad RAM. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

## SUBMINIATURE T-1½ WEDGE BASE LAMPS

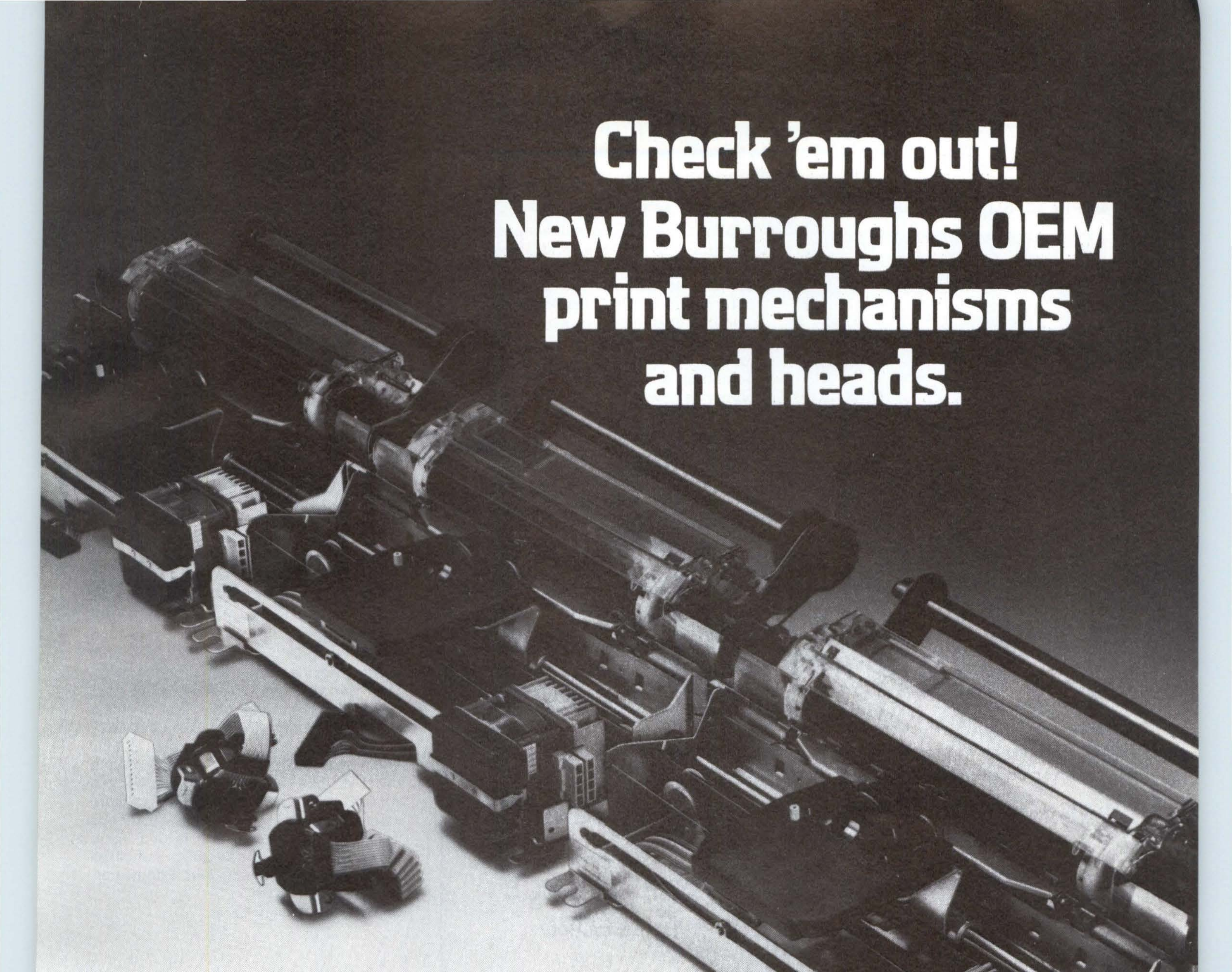
Augmenting T-3¼ and T-1¾ wedge base sizes, the T-1½ subminiature model is offered in voltage ratings of 6, 6.75, 12, 13.5, and 24 V with outputs ranging from 0.07 to 0.60 mean spherical candle power and life spans ranging up to 5 kh. The T-1½ lamps draw from 0.030 to 0.178 A in normal operation. The wedge base lamps easily mount on PCBs. Filament location is kept constant so replacement lamp filaments are automatically positioned the same as the original. **Chicago Miniature Lamp Works,** 4433 N Ravenswood Ave, Chicago, IL 60640.
Circle 256 on Inquiry Card

## SBC SERIES COMPATIBLE PROTOTYPING CARD



Intel Multibus™ compatible card has 4 independent staggered bus lines that can be user defined for either voltage or signal. All holes are plated-through and are sized to accept wirewrap posts. All connector fingers of the MPC-104 are gold plated and have adjacent, redundant, and usable hole patterns for bus expansion and flat ribbon cable headers. Mounting holes accept round, rectangular, or square potentiometers. **ADCO Electronics,** 2182 DuPont, Suite 222, Irvine, CA 92715.
Circle 257 on Inquiry Card

# Check 'em out! New Burroughs OEM print mechanisms and heads.



## You'll find every feature you've been looking for: speed, performance, price and reliability.

That's right. For the first time ever, Burroughs offers to OEM's our line of dependable, low-cost, dot matrix print heads and printer mechanisms. The print head options include 90, 120 or 180 cps operation with 7 or 9 pin configuration. Print mechanisms available with 132 print positions and print speeds to 90 cps.

You can add Burroughs dependability to your product for as little as $80 (PH 119-90 print head) or $270 (PM 100 Series print mechanism) in 100 quantity. They're worth looking into. Call or write for low evaluation unit prices and detailed specifications.

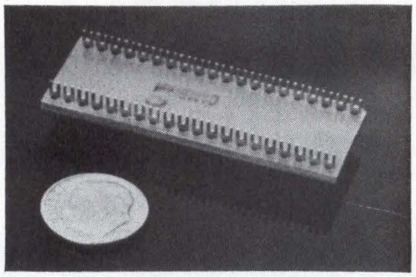
**Burroughs OEM Marketing Corporation,** P.O. Box 1226, Plainfield, NJ 07061, (201) 757-5000. In Europe, High Street, Rickmansworth Hertfordshire, England. Telephone 70545.

**Burroughs**

**Circle 116 For General Information** | **Circle 117 For Detailed Specifications**

# PRODUCTS

### 40-PIN IC SOCKET ADAPTER

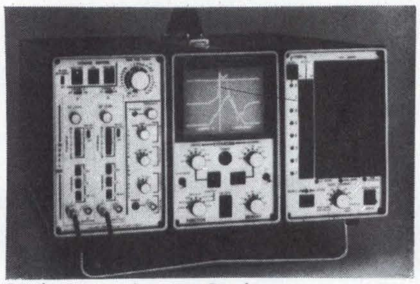


Flat pin socket adapter line is extended with the introduction of the 40-pin P/N 702-3700. Adapter plugs into a std 40-pin dual-inline socket with contacts on 0.1" (2.5-mm) pitch in each row. Rows must be 0.6" (15.2 mm) apart. Pins are of phosphor bronze, and units are offered with either gold plated pins or electro-tin plate. The adapter's fiberglass fabric reinforced material provides low profile, with high strength and rigidity. **Cambridge Thermionic Corp,** 445 Concord Ave, Cambridge, MA 02238.

Circle 258 on Inquiry Card

### DIGITAL OSCILLOSCOPES

Explorer digital oscilloscopes offer resolution to 0.025% and linearity to ±0.05% of full scale. Rise times are as fast as 50 ns. The 2-channel input operation is simultaneous. Mid-signal trigger mode is available. Waveform displays include digital scale expansion up to 64X, automatic trace centering, and cursor-selected accurate numerical voltage and time values. Display may be in YT or XY format; live and stored waveforms may be superimposed for comparison. **Nicolet Instrument Corp,** 5225 Verona Rd, Madison, WI 53711.



Circle 259 on Inquiry Card

### 20-BIT RESOLUTION S-D CONVERTER

With internal input/reference transformer isolation, SD562 is contained in a 3.12 x 3.62 x 0.82" (7.92 x 9.19 x 2.08-cm) package. Std accuracy is 19.8 arc-s, maintained with ±10% variation in input/reference voltage, 10% harmonic distortion, and ±5% variation in any dc voltages. Power requirements are ±15 Vdc at 100 mA and 5 Vdc at 600 mA. Output format for the converter is 20-bit parallel binary, DTL/TTL compatible. **Natel Engineering Co, Inc,** 8954 Mason Ave, Canoga Park, CA 91306.

Circle 260 on Inquiry Card

### SUBMINIATURE LED INDICATORS

Super-Brite subminiature LED indicator light assembly incorporates ultra-high intensity light output LEDs. The 3990 series provides snap-in mounting without hardware in a 0.219" (5.56-mm) dia panel mounting hole. Panel thickness may range from 0.031 to 0.063" (0.787 to 1.600 mm). Low profile lenses permit maximum light output over a 180° viewing angle. These solid state indicators have typ forward voltages of 2 V at 20 mA; luminous intensity at this current is typ 4 to 5 mcd for the bare LED. **Industrial Devices, Inc,** 7 Hudson Ave, Edgewater, NJ 07020.

Circle 261 on Inquiry Card

### LIMITED DISTANCE MODEM

Designed for limited distance operation of less than 20 mi (32 m) at speeds up to 19.2k bits/s over private lines or unloaded local telephone circuits, the Mc4800A features half-duplex/full-duplex, point to point or multipoint, and asynchronous/synchronous operation. Available in rackmounted or desktop configurations or as a single PC card, modem includes front panel digital and analog loopback switches and 6 LED status indicators. Modem conforms to Bell 43401 specs. **Data-Control Systems,** PO Box 860, Commerce Dr, Danbury, CT 06810.

Circle 262 on Inquiry Card

**PRODUCTS**

### HIGH FREQUENCY RANGE WIREWRAPPABLE BOARDS

Dual, quad, and hex boards, the 2-DE2-VHF, 2-DE4-VHF, and 2-DE6-VHF, cover the frequency range from dc to approximately 500 MHz. These DEC compatible boards feature dual ground planes, 1" (2.54-cm) stacking, full digital and analog capability, plated through holes, and unrestricted placement of 0.3, 0.4, 0.6, and 0.9" (7.6-, 10.2-, 15.2-, and 22.9-mm) DIP sizes. Documentation kits, consisting of master formats on vellum, are available for each board. **Hybricon Corp,** 410 Great Rd, Littleton, MA 01460.
Circle 263 on Inquiry Card

### MULTIPLE-PERIPHERAL I/O BOARD

Based on the original Bitstreamer design, Bitstreamer II board combines 2 parallel I/O ports with 3 serial I/O ports using programmable USARTs. The board can generate interrupt requests through a jumper option. By using the initialization and I/O software on option C extended System Monitor P/ROM, the board can be operated as an RS-232 port. Additional software can make concurrent use of the other serial and parallel ports. **Vector Graphic Inc,** 31364 Via Colinas, Westlake Village, CA 91361.
Circle 264 on Inquiry Card

### VIDEO DISPLAY BOARD

The VDB-1 Smoke Writer board controls an 80 x 24 display with 32 graphic char. Display board has u/lc characters with lc descenders; 128-char graphics are optional. Its programmable 128-character set is in a 2k EPROM. 246-char 4k EPROM is optional. Other features include reduced intensity or reversed video, programmable display rates from 10 to 5k char/s, protected fields, and addressable cursor. **Smoke Signal Broadcasting,** 31336 Via Colinas, Westlake Village, CA 91361.
Circle 265 on Inquiry Card



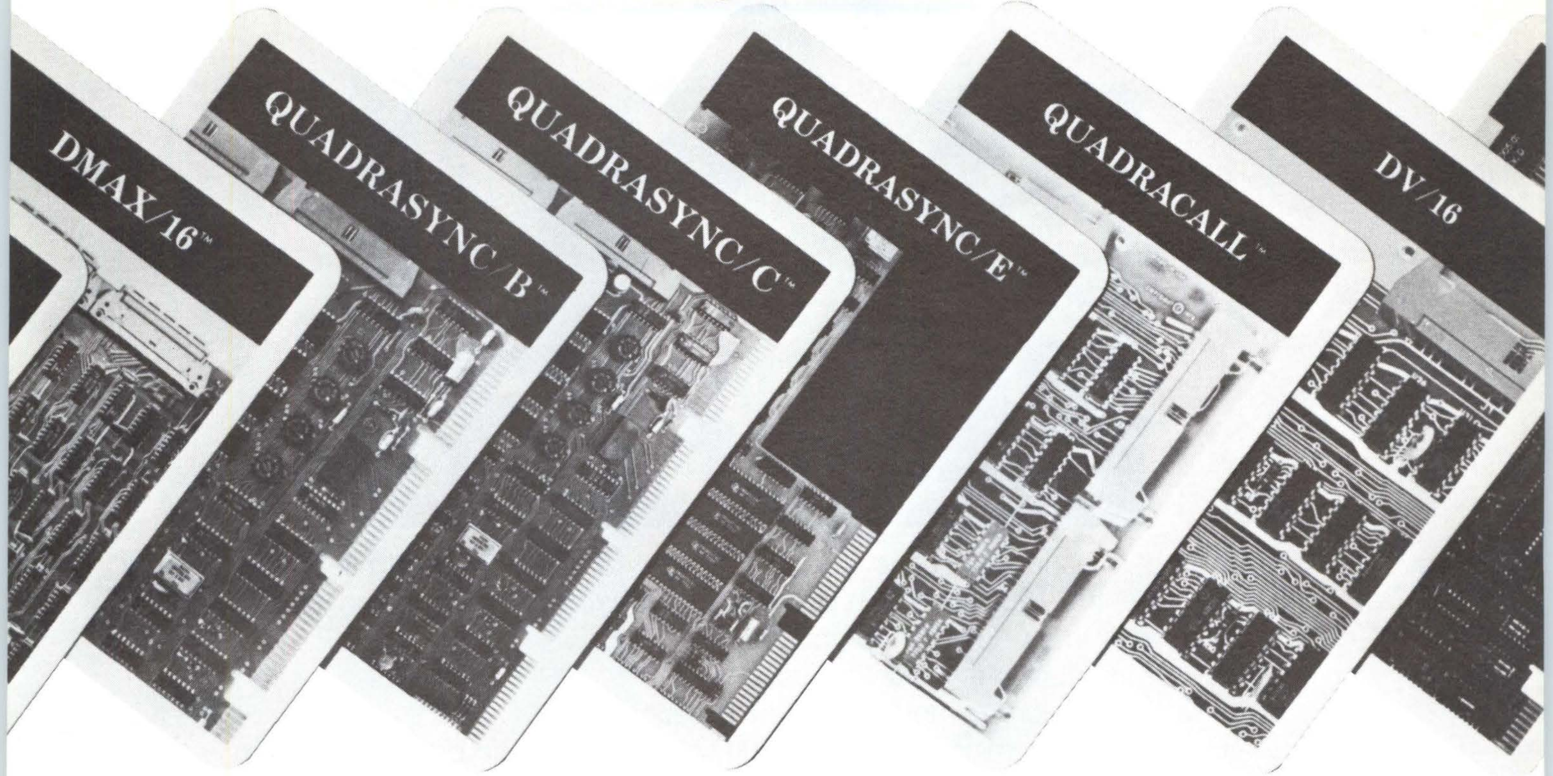
### INTELLIGENT TERMINAL

A source entry unit, the model 1100 intelligent terminal incorporates a 16-bit microprocessor, 1920-char video display, 64k bytes of RAM, and typewriter-style keyboard. Computing results can be stored on model 1105 dual diskette drive that contains 256k bytes/drive. Connected to companv's host computers, the intelligent terminal allows fully interactive computing. Terminal captures, edits, and validates data. **Tymshare, Inc,** 20705 Valley Green Dr, Cupertino, CA 95014.
Circle 266 on Inquiry Card

### PRINTED CIRCUIT VERSION SOLDERLESS BREADBOARD

Pre-etched, pre-drilled, PC version of EXP-300 Experimentor solderless breadboard, the Experimentor Matchboard™, emulates the contact and hole configuration of the solderless breadboard and echoes hole-indexing letters and numbers. The direct size and pattern correlation between the solderless breadboard and its PC counterpart facilitates transition from breadboard to printed circuit, eliminating the need for PC patterns, photography, chemistry, or tooling. **Continental Specialties Corp,** 70 Fulton Ter, New Haven, CT 06509.
Circle 267 on Inquiry Card

# Hotline to your PDP-11

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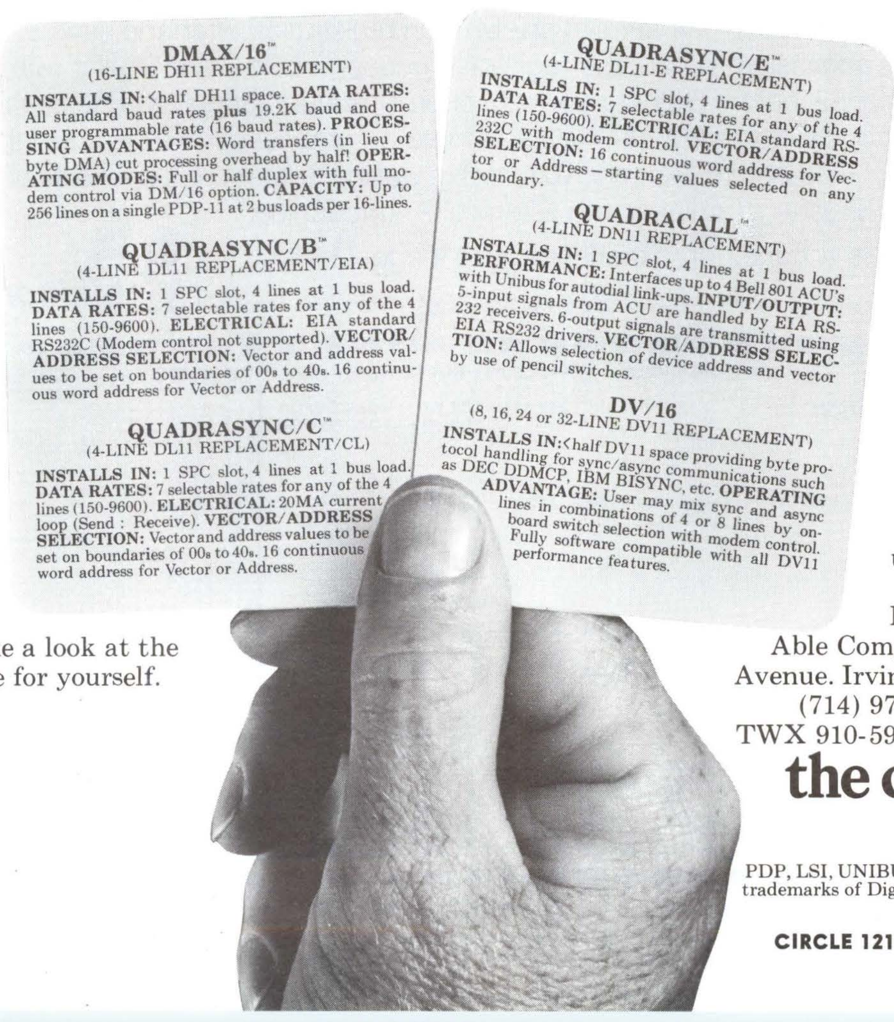


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CIRCLE 121 ON INQUIRY CARD

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| | E | Sales/Marketing |
| | F | Purchasing/Procurement |
| | G | Educator/Student |
| AREA OF MAIN PRODUCT INTEREST | H | Active components |
| | I | Passive components |
| | J | Hardware |
| | K | Tools & production equipment |
| | L | Computers |
| | M | Computer peripherals |
| | N | Control systems & components |
| | O | Electro-optical components |
| | P | Enclosures |
| | Q | Instruments, indicating |
| | R | Instruments, control |
| | S | Mechanical components |
| | T | Microwave components & systems |
| | U | Power sources |
| | V | Wire, cable & connectors |

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SYNERTEK PERFORMS

# 16K ROMs. 3 weeks. 32K ROMs. 4 weeks.

When it comes to service, product availability and fast prototype turnaround, we can't be beat. And that means 16K ROM prototypes in three weeks, 32K ROM prototypes in four weeks. Volume production in five to six weeks. Even quicker if it's absolutely needed.

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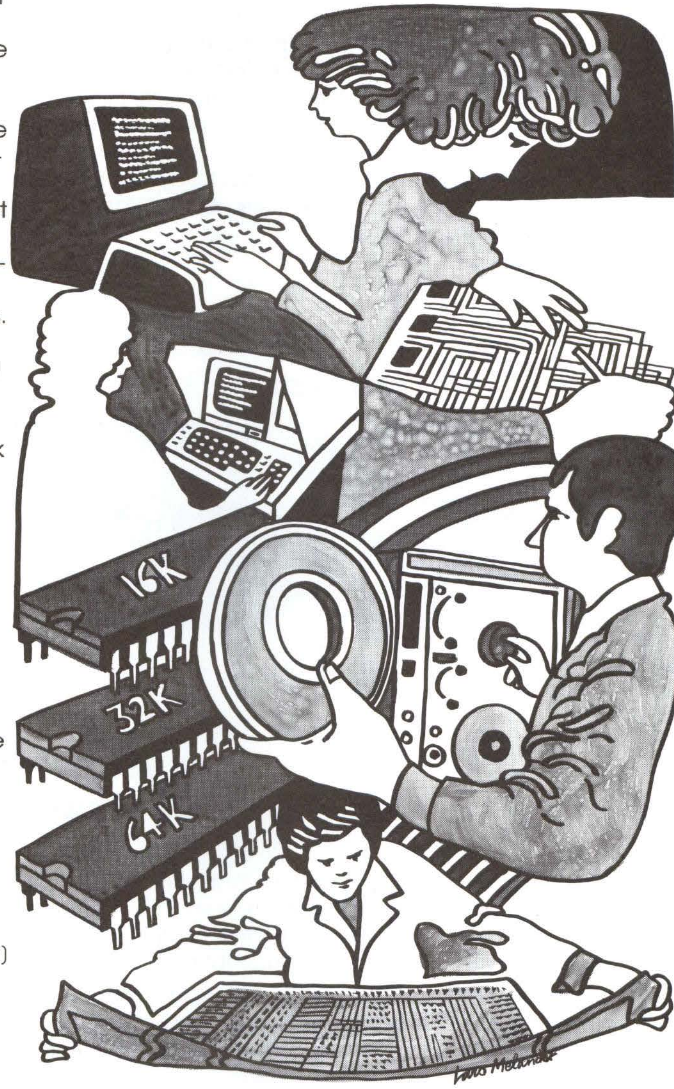
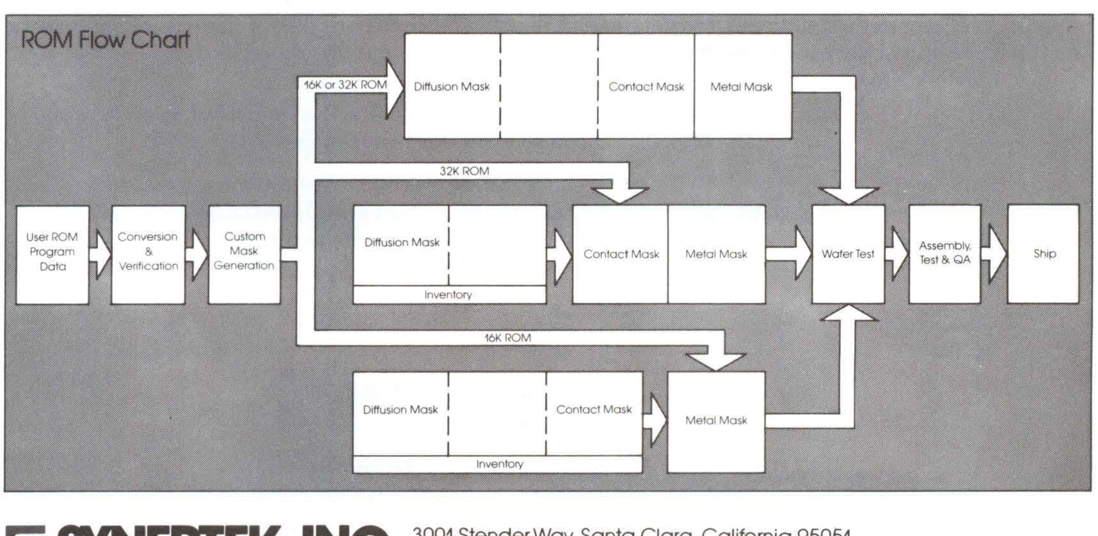
When you buy ROMs from Synertek, you're buying total service. For samples, data sheets and our comprehensive folder "Synertek ROMs ASAP," contact your local Synertek distributor, sales representative or Memory Product Marketing, Synertek, Inc., 3001 Stender Way, Santa Clara, California 95051. (408) 988-5611. TWX: 910-338-0135.

Synertek sales offices: **Eastern Region,** Boston (617) 329-5522; **Mid America Region,** Chicago (312) 986-8989; **Western and Northwest Regions,** Santa Clara (408) 255-3941; **Southwest Region,** Los Angeles (714) 752-5535; **Europe,** London, Direct Dial: 44-344-24555.




**SYNERTEK, INC.** 3001 Stender Way, Santa Clara, California 95051 (408) 988-5600. TWX: 910-338-0135.

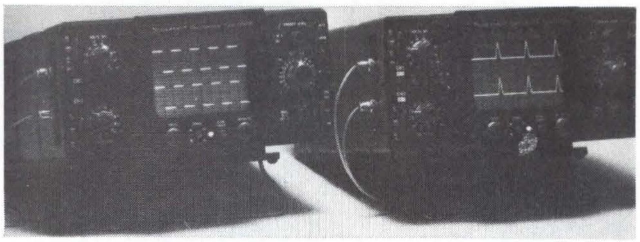
CIRCLE 122 ON INQUIRY CARD

### GRAPHICS OPTION FOR THERMAL PRINTER

Interspersed graphics and text for engineering, scientific, medical, and industrial use are obtained from an option to the T-80 5 x 7 dot matrix printer. When graphing, it employs a raster scan technique sequentially energizing any of the 7 vertical dots. Both vertical and horizontal spacing is 70 dots/in (28/cm) giving 4900 points/in$^2$ (760/cm$^2$). Distance between points is 0.014" (0.036 cm). Headings, legends, values, or any other text may be printed simultaneously with graphing. A std 96-char ASCII set is contained in ROM. Char spacing is 10/in (4/cm) with 6 horizontal lines/in (2/cm). On-the-fly printing occurs without stopping or lifting the head between char. **Dataproducts Corp,** 6219 DeSoto Ave, Woodland Hills, CA 91364.

Circle 268 on Inquiry Card

### LOW COST 15-MHZ DUAL-TRACE OSCILLOSCOPES



Telequipment D1015 and D1016 offer automatic, normal, and TV triggering; volts/div ranges from 5 mV to 20 V; and time base sweep speeds from 0.2 $\mu$s to 200 ms/div (5X magnifier increases max sweep speed to 40 ns/div). In addition, D1016 is equipped with 5X magnifiers for each vertical channel that extend sensitivity 1 mV/div (bandwidth is reduced to 4 MHz at this setting). Separate pushbuttons invert channel 2 and add channels 1 and 2, permitting balanced differential input measurements. Also included are direct X-Y displays using channel 1 and 2, and variable uncalibrated sweep control permitting continuously variable sweep rates between the detent positions of the time/div switch, extending the slowest sweep speed to 500 ms/div. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.

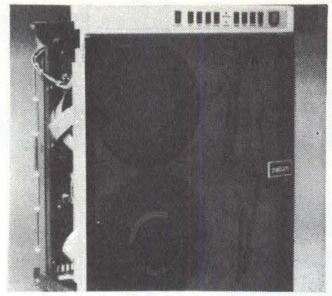
Circle 269 on Inquiry Card

### MICROPROCESSOR BASED STATISTICAL MULTIPLEXER

To cost-effectively connect remote terminals to DEC Unibus based computers, a single 205/11 board takes up 1 Unibus slot and can support up to 128 terminals, thus replacing up to 16 DZ-11 boards and a host-end multiplexer. The multiplexer takes multiple streams of data char from the host computer and concentrates them onto a single, bit-serial trunk link. Internal structure consists of a DZ-11 emulator coupled to the company's System-115 emulator. The unit appears as multiple DZ-11 boards to the Unibus and as a std network processor to the company's network. Few host software changes are required. Statistical multiplexing, full ARQ error control with extended CRC checking, and variable framing are featured. **Digital Communications Associates, Inc,** 135 Technology Pk, Norcross, GA 30092.

Circle 270 on Inquiry Card

### MINICOMPUTER TAPE TRANSPORT



Microprocessor control, self-diagnostics such as fault isolation and skew verify alignment, reduced electronic parts count, and hybrid chip read amplifiers are designed into the D-451 transport, which has a 45-in (114-cm)/s tension arm. The single PC board architecture allows system configurations that include 7- or 9-track NRZI and phase encoded tape formats. Tape density is 1600 bits/in (630/cm) for PE, and 800, 556, and 200 bits/in (315, 219, and 79/cm) for NRZI. An embedded dual-density formatter controls up to 4 tape transports. Other features are IBM tape path geometry, ceramic blade tape cleaners, photoelectric write ring detection, low inertia capstan drive, and digital write deskew control. **Datum Inc,** 1363 S State College Blvd, Anaheim, CA 92806.

Circle 271 on Inquiry Card

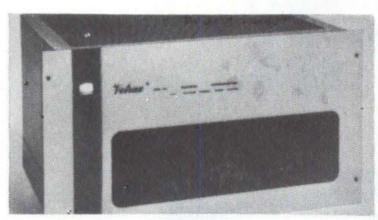
### S-D CONVERTERS WITH 3-STATE OUTPUTS

Output latches ease interfacing of S-D converters to data buses. The 12-bit resolution, ±3.2 arc-min ±1 LSB (0.04%) accurate SDC 1725 and the 10-bit resolution, ±22 arc-min (0.01%) accurate SDC 1726 also feature precision Scott Tee and reference microtransformers enabling the 3.125 x 2.625 x 0.35" (79 x 67 x 9-mm) package size. Synchro data can be transferred onto the microprocessor bus by utilizing enable/inhibit commands without interfering with the converter's internal control loop. The converters accept inputs of either 3-wire synchro plus reference or 4-wire resolvers plus reference. Tracking rates are specified at 5, 36, and 50 r/s, minimum, for 60-Hz, 400-Hz, and 2.6-kHz reference options, respectively. **Analog Devices, Inc,** PO Box 280, Norwood, MA 02062.

Circle 272 on Inquiry Card

### DIGITIZED AUDIO RESPONSE SYSTEM

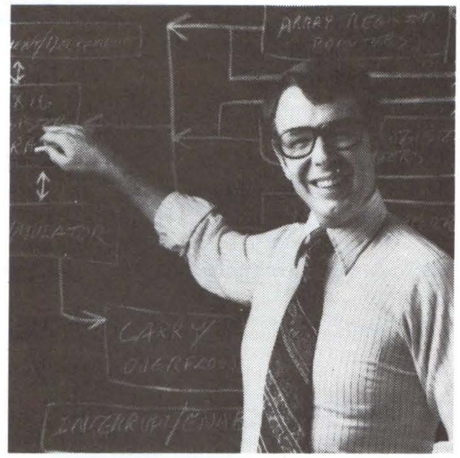
Multiline audio output and Touch-Tone™ input handling capability for microcomputers, minicomputers, and large business mainframes are produced by the solid state, multiplexed LVM-80 system. The vocabulary capacity is 512 s of speech or approx 1024 individually addressable messages. Memory capacity is 16k (EPROM) and can be erased and reused. The communications processor services up to 64 simultaneous telephone lines, and through a process of digitizing actual human speech, speaks words and phrases. Word and message lengths are variable; a custom vocabulary consists of words, phrases, and voice of the user's choosing. Communications data sets supported by the system include the Bell 407-A, -B, several 403 type units, and AT&T's MFR. **Votrax, a div of Federal Screw Works,** 500 Stephenson Hwy, Troy, MI 48084.



Circle 273 on Inquiry Card

# "To get ahead, I came back to the place where I started."



Some engineers and scientists leave Hughes only to return — a little older and a lot wiser.

The reasons they come back are always the same.

They want a bigger challenge and more exciting programs to choose from.

They want greater opportunities for career advancement, along with job security.

And, like everyone, they want a friendly, creative environment and lots of benefits. Most likely, the same things you want out of your job.

Are you getting them?

At Hughes, we're confident we can offer you all these things and more.

How do we know? We asked our staff in a survey. And in a time when fewer and fewer people are getting satisfaction from their jobs, Hughes people told us they're actually getting more. And that's saying a lot.

If you can't say the same thing about your present situation, give us a call. Whether you've worked here before, or not.

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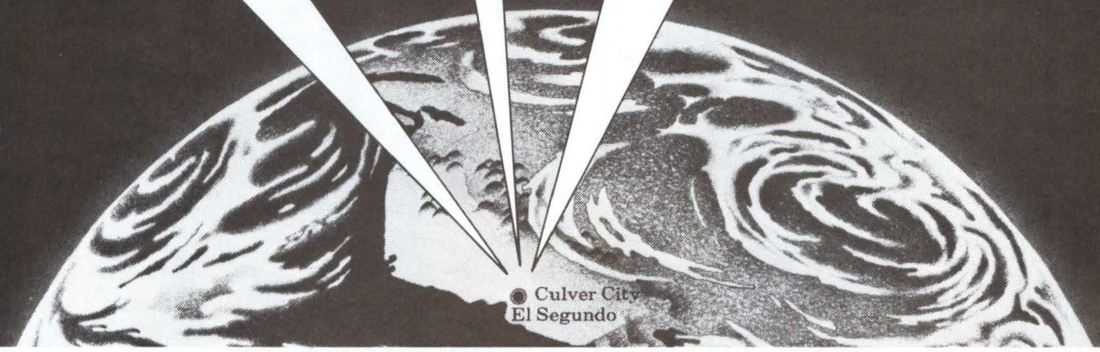
Call us at **(213) 391-0543** or send your resumé to: Professional Employment, Hughes Electro-Optical & Data Systems Group, Research and Development, 11940 W. Jefferson Blvd., Dept. CD, Culver City, CA 90230.

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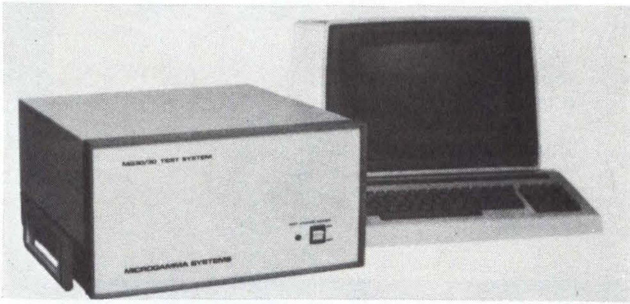
All positions require an appropriate engineering or technical degree from an accredited university. U.S. Citizenship Required. Equal Opportunity M/F/HC Employer.

### 15-V CONTROL SYSTEM I/O MODULES

Series of 6 I/O modules—with inputs and outputs of 140 Vac, 280 Vac, and 60 Vdc—interface between a 15-V microprocessor control (or other logic) system and external ac and dc voltage levels in industrial and commercial peripheral equipment. Dc output modules accept 15 V from the microprocessor and at the output drive dc loads to 3 A at 60 V. Dc input modules accept voltages up to 32 V and convert them back to the 15-V level for the microprocessor. When activated by an ac input signal, the ac input modules for 120- and 240-Vac operation provide a 15-Vdc output that alerts the processor that an external event has occurred. The output module, in response to a 15-Vdc signal from the processor, turns on an external 120- or 240-Vac device. **Motorola Semiconductor Products Inc,** PO Box 20923, Phoenix, AZ 85038.

Circle 274 on Inquiry Card

### SEMICONDUCTOR MEMORY TEST SYSTEM



Production testing of semiconductor memory devices, boards, or systems and testing of LSI devices is handled by the MG 30/30, which contains a single-board computer for test program control; this computer can also be interfaced to device handlers or other peripheral equipment. A software package permits board error mapping and software calibration of all programmable clocks. Operator interactions are provided via a CRT using a version of MTS BASIC, the company's high level, interpretive language. The test station portion of the system is a pattern processor that generates address and data patterns at 10 MHz. A 16-bit address generator expands to 24 bits and features dynamic field length definition. **Microgamma Systems Inc,** 950 Benicia, Sunnyvale, CA 94088.

Circle 275 on Inquiry Card

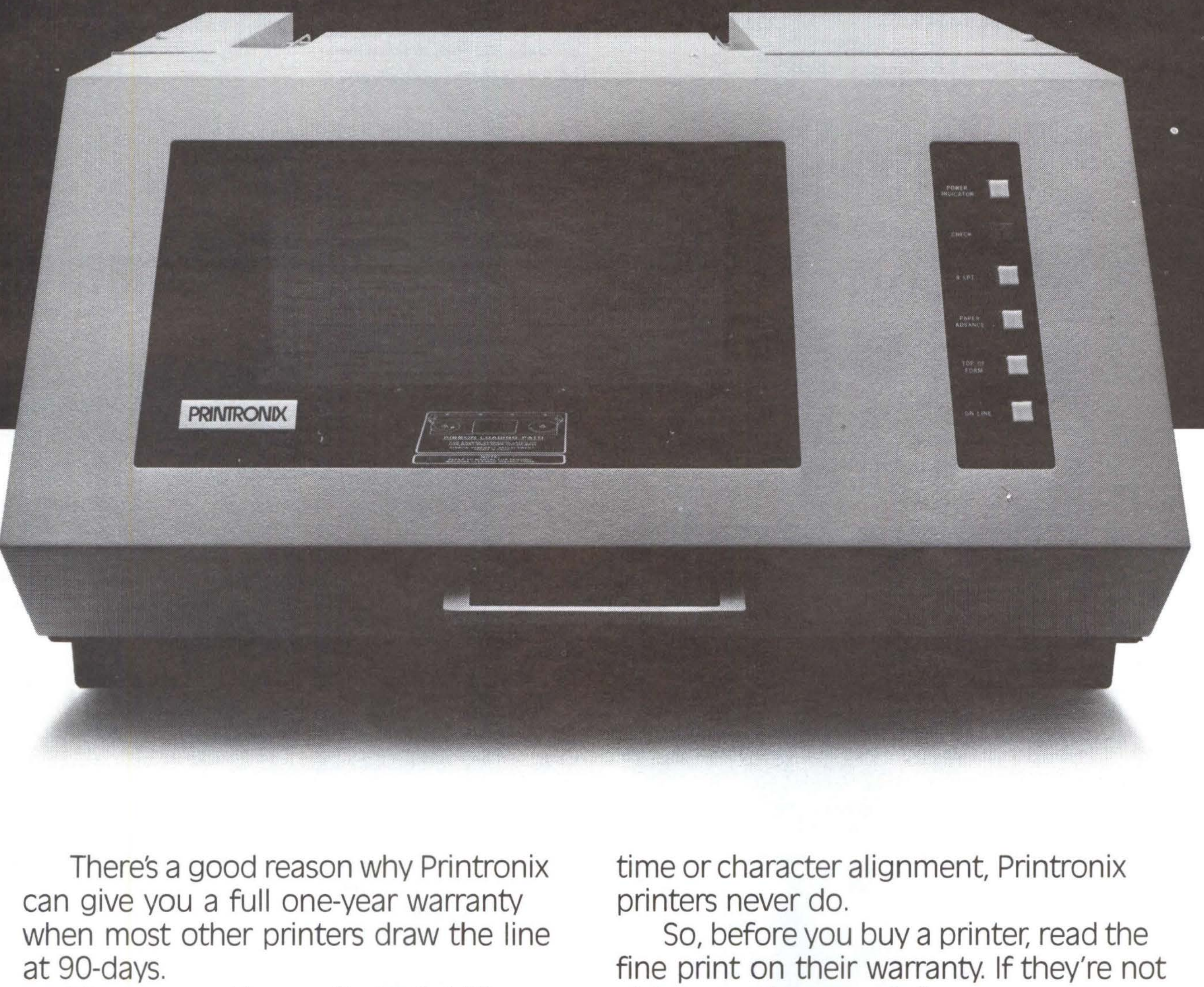
### LOW COST 2-AXIS TOUCH PANEL

Trazor™ brand touch panel gives 1-finger control of 2 parameters. The touched surface consists of a thick film of resistive material on an insulating backing. Four unshielded wires connect the surface to the electronic circuitry,


located at a distance, which senses the location of the users finger from minute electric currents capacitively coupled through the user's body. X and Y position outputs plus a binary "presence" signal are provided, as are either infinite resolution analog or digital position outputs. Linearity, limited to about ±5% by nonuniformities in silk screening, is satisfactory for most applications. Power required is 105 to 125 Vac, 50 to 400 Hz. **Peptek, Inc,** 9839 Singleton Dr, Bethesda, MD 20034.

Circle 276 on Inquiry Card

# BEFORE OTHERS CAN PRINT A WARRANTY LIKE OURS, THEY'VE GOT TO MAKE PRINTERS LIKE OURS.




There's a good reason why Printronix can give you a full one-year warranty when most other printers draw the line at 90-days.

The reason: *Unequalled reliability.*

Our reliability comes not only from what we put into our printers, but also because of what we leave out. For instance, Printronix printers have 50 percent fewer components than mechanical font printers. So there's less to go wrong!

And this same simple design has given our printers a head life 4 to 8 times longer than serial printers. And while drum, chain and belt printers require periodic adjustments of hammer flight time or character alignment, Printronix printers never do.

So, before you buy a printer, read the fine print on their warranty. If they're not giving you the same full one-year warranty that Printronix offers, then it's a sure bet they're not giving you the same solid reliability that Printronix gives.

For complete information on our 150, 300 and 600 line-per-minute printers call: (714) 549-7700. Or write: Printronix Inc., 17421 Derian Ave., P.O. Box 19559, Irvine, CA 92713.

**PRINTRONIX**

**It's simple, to be reliable.**

CIRCLE 127 ON INQUIRY CARD

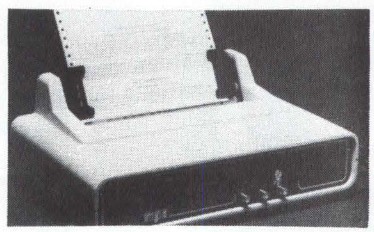
## FIBER OPTIC MODEM

FOM provides full-duplex operation at data rates up to 56k (synchronous) or 9.6k (asynchronous) bits/s over 2 fiber optic cables. Handling local distribution applications, it is suited for DTE/DCE interfaces since it appears fully transparent to all clock and data signals. Also featured is a full EIA interface with interactive handshaking. Control signals are multiplexed along with the data to provide positive DCE control. If full interactive controls are not required, the RTS-CTS signals may be connected at the remote location to give continuous, positive indication that the transmit and receive circuits are operational. Front panel LED indicators display traffic and control signal status. **Versitron, Inc**, 6310 Chillum Pl, NW, Washington, DC 20011.

Circle 277 on Inquiry Card

## DOT MATRIX IMPACT PRINTER

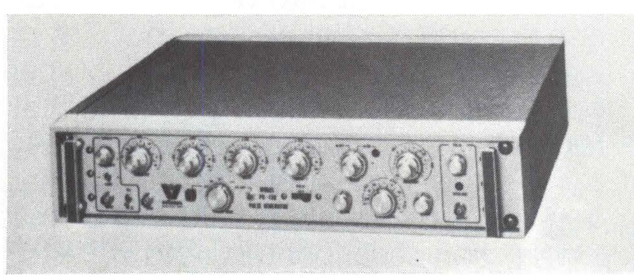
Featuring 100-char/s bidirectional printing and print line formats of 80, 96, or 132 col, model 88T prints a full upper and lower case 96-char ASCII set in a 7 x 7 matrix on the original plus 2 copies. Double width char are software selectable and can be intermixed on any line for message highlighting. The 10-, 12-, or 16.5-char/in (4, 5, or 6/cm) print density selection allows the user to print on std multiple copy forms. Also included are a stepper motor driven tractor paper feed system and 8 selectable form lengths. The microprocessor controlled interface accepts either serial RS-232/CL or parallel data. A 2-line buffer is std, with 1k and 2k data buffers as options for CRT screen dumps. **Micro Peripherals, Inc,** 2099 W 2200 S, Salt Lake City, UT 84119.



Circle 278 on Inquiry Card

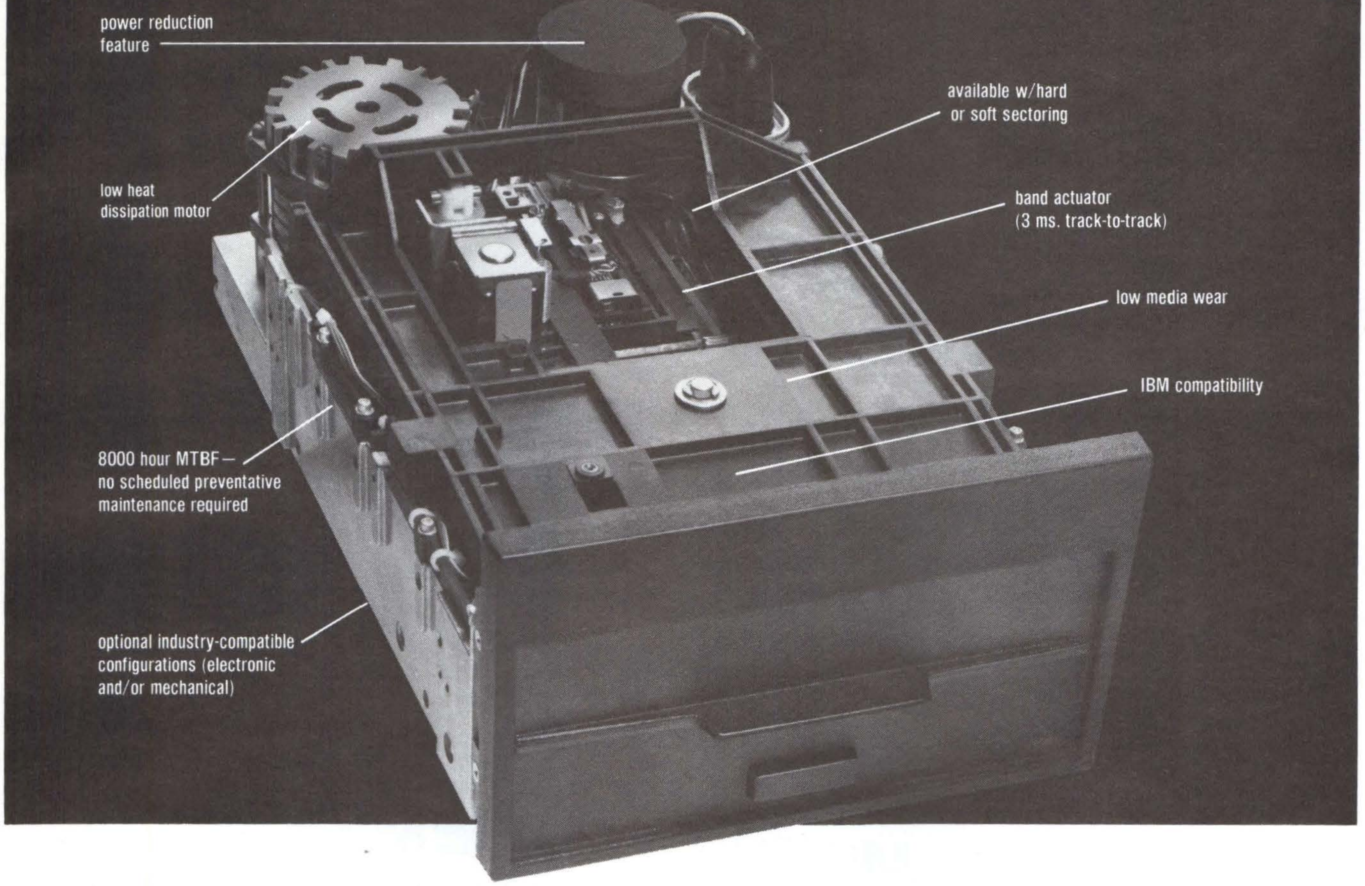
## HIGH POWER PULSE GENERATORS

PG-13D offers high amplitude voltage or current operation as either a current source to ±2 A or a voltage source to ±100 V. In addition to internal, external, a single-shot, and gated PRF operation, the unit provides a pulse of fixed delay (with reference to an input trigger) or 2 pulses with variable delay adjustment between them. Features are variable rise and fall times down to 10 ns, high level output, and adjustable baseline offset. Internal circuitry protects against damage by overload or excessive duty factor. When operated in the voltage mode, the device generates up to 100 V across a 50-Ω load. It operates at duty factors up to 15% on the 100-V/2-A range. **Velonex, a div of Varian,** 560 Robert Ave, Santa Clara, CA 95050.



Circle 279 on Inquiry Card

# CDC knows what OEM's want most in a two-headed floppy. Confidence.




Experience plus feedback. The success formula that earned us our reputation in rigid disk technology can work for you in flexible disk technology. Our 9406 incorporates all that we've learned from building more than 100,000 single-sided floppies. All that we've learned from talking to our OEM customers about a wide variety of two-headed floppy applications.

Our 9406 has two read/write heads for two-sided media. But depending upon your application, the 9406 can be operated in either one- or two-sided mode as well as single- or double-density formats.

You have requested IBM media interchangeability and we have it. Optional mechanical and electronic configurations that are industry-compatible are available. Or you can match the dimensions, mechanical mounting and interface protocol used by our single-sided drives.

Besides confidence in the product, our 9406 customers can enjoy confidence in the company that makes it. Control Data is one of the world's largest suppliers of OEM equipment. And we've built a service and support organization that you can depend on. For financing, maintenance or spare parts. For assistance in building quality and confidence into your product line.

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Please tell me more about your 9406 flexible disk drive.

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Firm__________ Phone__________

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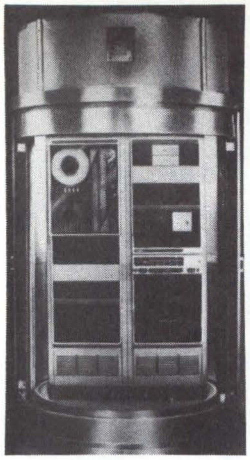
CIRCLE 130 ON INQUIRY CARD

## MINICOMPUTER/SYSTEM CYLINDRICAL ENCLOSURE



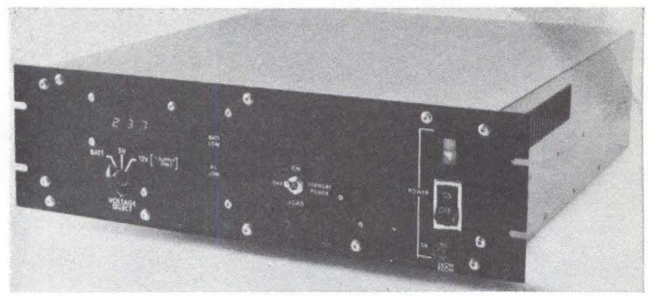
Enclosure 48 is a prefabricated capsule that houses minicomputers, peripherals, and other distributed processing and process control equipment. It provides a controlled and secure environment for uninterrupted operation, expanding the range of applications to commercial, industrial, and hostile areas. The unit is constructed of a transparent impact resistant outer shield and a strong composite paneling inner shield. Included are fire retardant layers, automated fire door, internal and external fire detectors, and fire suppression system. Other features are fully redundant HVAC, air distributing racks, rotating platform, self-sealing cable access points, warning sensors, and audible and visual alarms. **Transaction Security, Inc,** 299 Park Ave, New York, NY 10017. Circle 280 on Inquiry Card

## MINICOMPUTER 6250-BIT/IN MAGNETIC TAPE SYSTEM

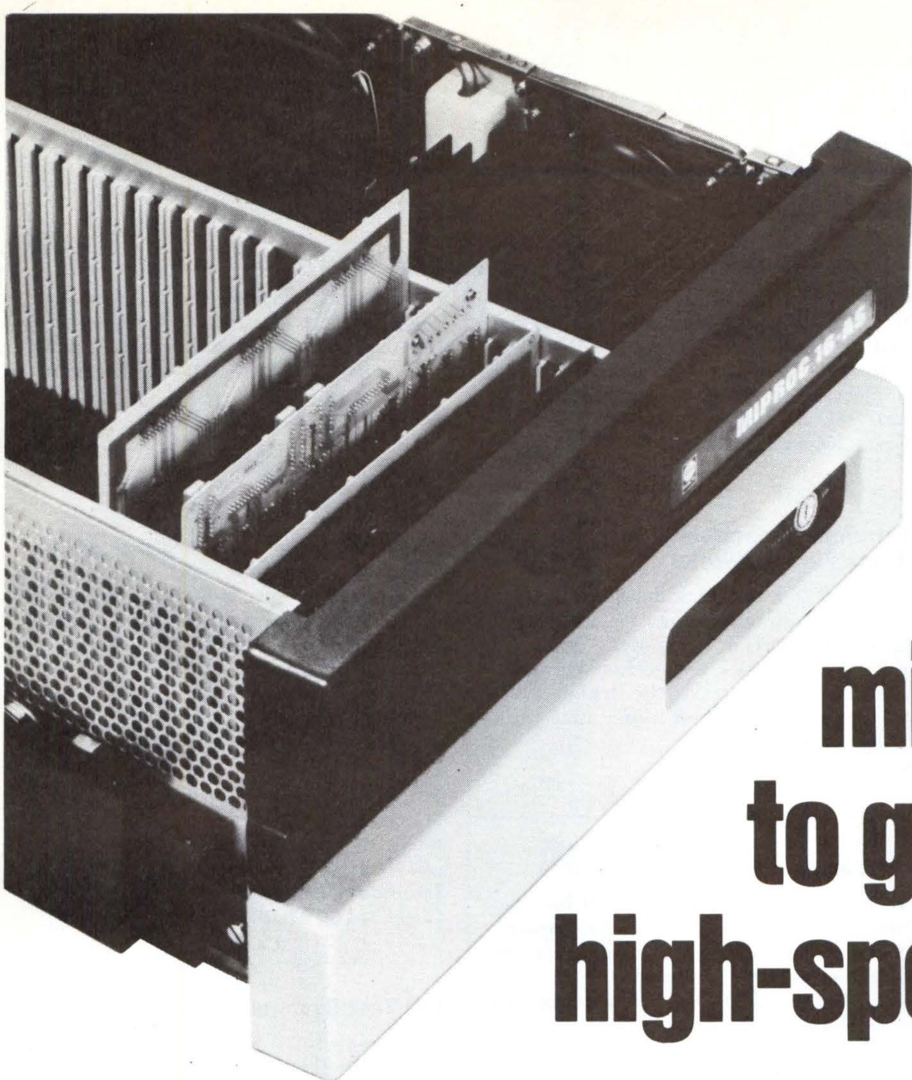
The dual-density 9-track 75-in (190-cm)/s system, having both 1600- and 6250-bit/in (630 and 2461/cm) recording capability, offers 150M bytes of storage on a 2400-ft (732-m) reel. It operates with DEC's Unibus computers. Model 804 consists of an STC microsequencer controlled tape drive and formatter, as well as the company's 4k-byte hex size controller adapter board employing bit-slice technology. The board fits into a small peripheral controller (SPC) slot in the host computer chassis and runs under all DEC operating systems that use the TM11 handler. Data transfer rate is 470k bytes/s. Simultaneous on-the-fly 2-track error correction capability enhances data integrity. **Aviv Corp,** 6 Cummings Pk, Woburn, MA 01801.
Circle 281 on Inquiry Card

## UNINTERRUPTIBLE POWER SOURCE FOR NORMAL/STANDBY OPERATION

MSC 3901 provides automatic switching to a self-contained battery backup supply upon loss of normal dc power without interruption to the main system. The dual-voltage system furnishes 5 Vdc at 1 to 20 A, and 12 Vdc at 0.5 to 8 A in normal operation; the single-voltage system provides a 5-Vdc output. Output voltages are ±5%. In standby mode, the discharge rate capability is 10 A at 5 Vdc and 5 A at 12 Vdc for 1 h. The single-voltage system can also parallel an additional 5-Vdc standby source for increased standby rating. Located on the front panel are a 3½ digit DPM, a standby power switch, and 2 LEDs. The unit is air cooled for elevated temp environments. **Monolithic Systems Corp,** 14 Inverness Dr E, Englewood, CO 80112.



Circle 282 on Inquiry Card



MIL VERSIONS NOW AVAILABLE

# Miproc 16-AS, micropower to give you high-speed faster.

Internationally acclaimed Miproc-16 with a compute-rate of up to 4 million instructions per second is the fastest 16-bit microcomputer card family available.

Now supplied with an OEM chassis package, Miproc-16 is even more quickly brought into action.

This cost-effective application system, named Miproc-16 AS, has room for one, two or even three Miproc-16 CPU's. Smartly styled and equipped with add-in 13-slot card bay modules, fans and power supply, this new OEM chassis package eases the way into high speed microcomputing.

## Instruction Power

Up to 170 instructions including multiply/divide and bit manipulation give Miproc-16 formidable processing capability.

## 16-bit Power

16-bit program words make programming easy. 16-bit data words maintain high precision in arithmetic operations.

## Addressing Power

16-bit dual memory architecture gives 65k words of directly addressable program memory *and* 65k words of data memory with 8 powerful address modes.

## Interrupt Power

Multilevel, priority vectored interrupt system handles context changes in less than 2 microseconds.

## I/O Power

256 directly addressable I/O channels with data I/O rates of up to 1.7 megabytes/sec. under program control, and up to 20 megabytes/sec. for DMA.

## High Speed Processing Power

The unique dual memory architecture combines with high speed Schottky TTL technology to execute most instructions in a single machine cycle.

## Software Power

Easy to use cross-assemblers for mainframe or minicomputer make programming faster, *and* PL-MIPROC, a super-efficient high level assembly language.

## Hardware Power

Comprehensive range of processor, memory and interface cards backed up by sophisticated hardware development aids.

## Ruggedized Power

Miproc can be configured to meet any known military specification.

**PLESSEY MICROSYSTEMS**

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Canada M3J 2M2

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Plessey Microsystems
19546 Clubhouse Road
Gaithersburg, Md.
20760, USA

Tel: (301) 948-2791

Plessey Microsystems
1641 Kaiser Avenue
Irvine, California
92714, USA

Tel: (714) 540-9931

**CIRCLE 132 ON INQUIRY CARD**

654 PP044

# LITERATURE

### Realtime Automatic PCB Test Systems

Simulation and programming station; analog, digital, and analog/digital test systems; plus optional features are presented in brochure. **Instrumentation Engineering, Inc**, Franklin Lakes, NJ.
Circle 300 on Inquiry Card

### Industrial Test Instruments

Catalog features descriptions, specs, application information, and photos of instruments including oscilloscopes, pulse generators, and variable output isolation transformers. **B&K-Precision, Dynascan Corp**, Chicago, Ill.
Circle 301 on Inquiry Card

### Stepper Motor Drive Chip

Outline, dimension, block, and timing diagrams; pin designation; performance curves; and specs in data sheet describe chip that drives 2-phase stepper motor. **Airpax/North American Philips Controls Corp**, Cheshire, Conn.
Circle 302 on Inquiry Card

### Matrix Boards

Single, dual, and multilayer matrix boards offer choice of 0.230, 0.157, or 0.100" (6.35, 4.0, or 2.54-mm) centers and shorting pins, component holders, or wireable programming pins. **Sealectro Corp**, Mamaroneck, NY.
Circle 303 on Inquiry Card

### Power Demand Controller

Brochure discusses system features, operational displays, data entry procedures, and options of microprocessor based units designed to reduce energy costs. **Dynapar Corp**, Gurnee, Ill.
Circle 304 on Inquiry Card

### Synchro Converters

Brief descriptions of S-D and D-S converters and related products in illustrated selection guide provide unit accuracies and modular dimensions. **Control Sciences, Inc**, Canoga Park, Calif.
Circle 305 on Inquiry Card

### Network Control System

Automatic monitoring, automatic preventive maintenance, and manual control operating modes of fully automated communications network monitoring and diagnostics system are explained in brochure. **Intertel**, Burlington, Mass.
Circle 306 on Inquiry Card

### Ceramic Capacitors and Thick Film Networks

Electrical and test specs, dimensional drawings, and performance data for disc, monolithic, and special application capacitors, as well as for thick film resistor networks, are furnished in catalog. **Centralab Electronics Div, Globe-Union Inc**, Milwaukee, Wis.
Circle 307 on Inquiry Card

### Test and Measuring Instruments

Technical specs, illustrations, and information for equipment including oscilloscopes, counters, counter/timers, recorders, and signal generators, are contained in catalog. **Philips Test and Measuring Instruments Inc**, Mahwah, NJ.
Circle 308 on Inquiry Card

### Digital Panel Meters

Specs, block and circuit diagrams, photos, typ connections, and options for digital process indicators/controllers, panel meters, counters, and timers are presented in catalog. **International Microtronics Corp**, Tucson, Ariz.
Circle 309 on Inquiry Card

### Cartridge Recorder/Reproducer

Environmental operating parameters of recorder are described in bulletin along with system performance, electrical specs, operating ranges, and capacity. **Genisco Technology Corp, Systems Div**, Compton, Calif.
Circle 310 on Inquiry Card

### Breadboard System

Comprised of solder and plug strips, dual sockets, 40-position header, insulated wire, PCB, and assembly tools, system described in brochure uses solderless connections for faster prototyping. **Electronic Products Div, 3M**, St Paul, Minn.
Circle 311 on Inquiry Card

### Statistics Enhancement

Statistics software described in data sheet enhances assembly inspection systems control of loaded PCB assembly by compiling failure data for each test run. **Teradyne, Inc**, Boston, Mass.
Circle 312 on Inquiry Card

### Multiplexers and Modems

Catalog covers statistical and time division multiplexers, modems, port selector, and modem/multiplexer tester plus company services. **Infotron Systems Corp**, Cherry Hill, NJ.
Circle 313 on Inquiry Card

### Switching Power Supplies

With up to 75% efficiency, series LG and LJ switching power supplies that are featured in brochure can halve electricity costs compared to equivalent linear units. **Lambda Electronics**, Melville, NY.
Circle 314 on Inquiry Card

### LSI Test Systems

Accompanied by individual spec sheets, brochure outlines features and applications of Sentry V, VII, and VIII LSI test systems. **Test Systems Group, Fairchild Camera and Instrument Corp**, San Jose, Calif.
Circle 315 on Inquiry Card

### Metal Replacement Resin

Illustrations of actual applications, plus page of specs, show properties of Lexan resin that replaces die-cast metal. **General Electric Co, Plastics Div**, Pittsfield, Mass.
Circle 316 on Inquiry Card

### Diskette Cartridge Systems

Describing cabinets, storage modules, CRT terminal workstations, and data safe, brochure outlines elements of media storage/work equipment. **Monarch Computer Products**, New Windsor, NY.
Circle 317 on Inquiry Card

### Permanent Magnet dc Motors

Bulletin highlights features of M5000 permanent magnet dc motor that is available from ⅛ to 1 hp, with voltage range from 12 to 115 Vdc. **RAE Corp**, McHenry, Ill.
Circle 318 on Inquiry Card

### Brushless dc Motors

Specs, dimensional drawings, wiring diagrams, and performance curves for motors and tachometers/position encoders comprise brochure. **Power Engineering Div, Siemens Corp,** Iselin, NJ.
Circle 319 on Inquiry Card

### Patching, Switching, and Tech Control Equipment

Brochure describes Data Patch patching and switching equipment, tech control systems, and network control system. **Atlantic Research Corp,** Alexandria, Va.
Circle 320 on Inquiry Card

### Graphic Display Computer

Literature describes hardware and software modules and provides typical specs and system configurations of the 5216 display computer. **Aydin Controls,** Fort Washington, Pa.
Circle 321 on Inquiry Card



### Band Line Printer

Data sheet outlines specs and features of microprocessor controlled 190- to 1100-line/min series 3001 band line printer. **Data Printer Corp,** Malden, Mass.
Circle 322 on Inquiry Card

### Communications Processor

Emulating an IBM 270X communications controller, processor profiled in brochure with features, characteristics, and network and architecture diagrams also functions as frontend processor. **Computer Communications, Inc,** Torrance, Calif.
Circle 323 on Inquiry Card

### Logic Analyzer

Sam, the digital detective, unravels a sabotage case using capabilities of a 532 logic state analyzer. **Paratronics, Inc,** San Jose, Calif.
Circle 324 on Inquiry Card

### Dc Micromotors, Tachometers, And Reduction Gear Boxes

Data provided in catalog include specs, schematic drawings, performance curves, construction details, and operating principles. **Portescap U.S.,** West Caldwell, NJ.
Circle 325 on Inquiry Card

### Sub- and Microminiature Lamps

Dimensional drawings, specs, and ordering information for T-1, -1¾, -¾, -½, -⅜, and TL size lamps and line filaments are included in catalog. **Oak Technology Inc,** Crystal Lake, Ill.
Circle 326 on Inquiry Card

### Microcomputers and Peripherals

Product guide contains specs and information on SYM microcomputer and peripherals, KTM keyboard terminal module, and SUPERJOLT single-board computer and accessories. **Synertek Systems Corp,** Sunnyvale, Calif.
Circle 327 on Inquiry Card


When it comes to flexibility, the Infoton 400 Data Display terminal can hand you all you need.

Designed around the Z-80 microprocessor, it offers complete control of all Blocking and Editing functions through software settable modes. One thing that's especially easy to handle about the I-400 is that it's the most versatile terminal you can get your hands on for the price.

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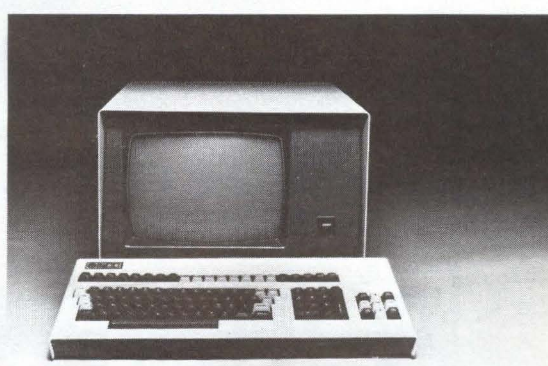


**INFOTON 400**

**CIRCLE 136 ON INQUIRY CARD**

### Thermal Printheads

Bulletin features performance characteristics, applications information, outline drawings, and performance charts for dot matrix alphanumeric thermal printheads—one with a larger plot dot for continuous traces. **Gulton Industries, Inc,** Metuchen, NJ.
Circle 328 on Inquiry Card

### Indicator Lights

Foldout chart indicates types of mountings, terminations, and options, as well as U.L. and C.S.A. status of Littlelite series lights. **Littlefuse, Inc,** Des Plaines, Ill.
Circle 329 on Inquiry Card

### Diskette Cross-Reference

Guide lists company's part numbers with those of 12 major diskette manufacturers for ease of cross-reference. **Wabash Tape Corp,** Des Plaines, Ill.
Circle 330 on Inquiry Card

### Mass Termination Connectors

Soca-Plex insulation displacement connectors are profiled in brochure with photos, specs, dimensional drawings, and tooling information. **Socapex,** Canoga Park, Calif.
Circle 331 on Inquiry Card

### Time Delay Relays

Dimensions, photos, wiring and terminal diagrams, and environmental, physical, and electrical characteristics for time delay relays are presented in catalog. **Midtex Inc,** N Mankato, Minn.
Circle 332 on Inquiry Card

### Counters and Timers

Technical data, options, and outline and dimensional drawings in catalog specify electromechanical counters and elapsed time meters. **Kessler-Ellis Products Co,** Atlantic Highlands, NJ.
Circle 333 on Inquiry Card

### Power Supplies

Handbook details electrical and mechanical parameters and lists case, pin, and socket configurations for line of power conversion products. **Datel Systems, Inc,** Canton, Mass.
Circle 334 on Inquiry Card

### Data Analyzer

Brochure details capabilities of D-901 line monitor and data analyzer and provides information on its programming language, operation, and self-diagnostics. **Spectron Corp,** Moorestown, NJ.
Circle 335 on Inquiry Card

### Single-Board Computer

Brochure covers features of Z80A processor, onboard APU, memories, and serial and parallel I/O ports plus available software, dual memory map option, and specs of MULTIBUS single-board computer. **Monolithic Systems Corp,** Englewood, Colo.
Circle 336 on Inquiry Card

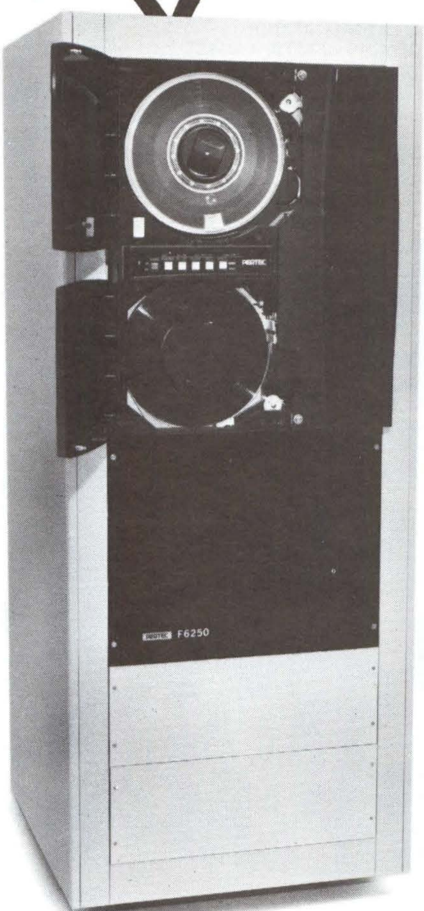
### Keyboards, Keyboard Switches, And Keycaps

Included in catalog and application guide are block diagrams, timing charts, dimensional drawings, legend format, output code, and connector pin assignment for hard contact or capacitive keyboards. **Cherry Electrical Products Corp,** Waukegan, Ill.
Circle 337 on Inquiry Card

### Electronic Test Instruments, Computers, and Peripherals

Featuring line of assembled and tested computers and peripherals, catalog also describes test instruments including oscilloscopes, strip and X-Y recorders, and signal and function generators. **Heath/Schlumberger,** Benton Harbor, Mich.
Circle 338 on Inquiry Card

# "Golly, I found a pain in my parity."

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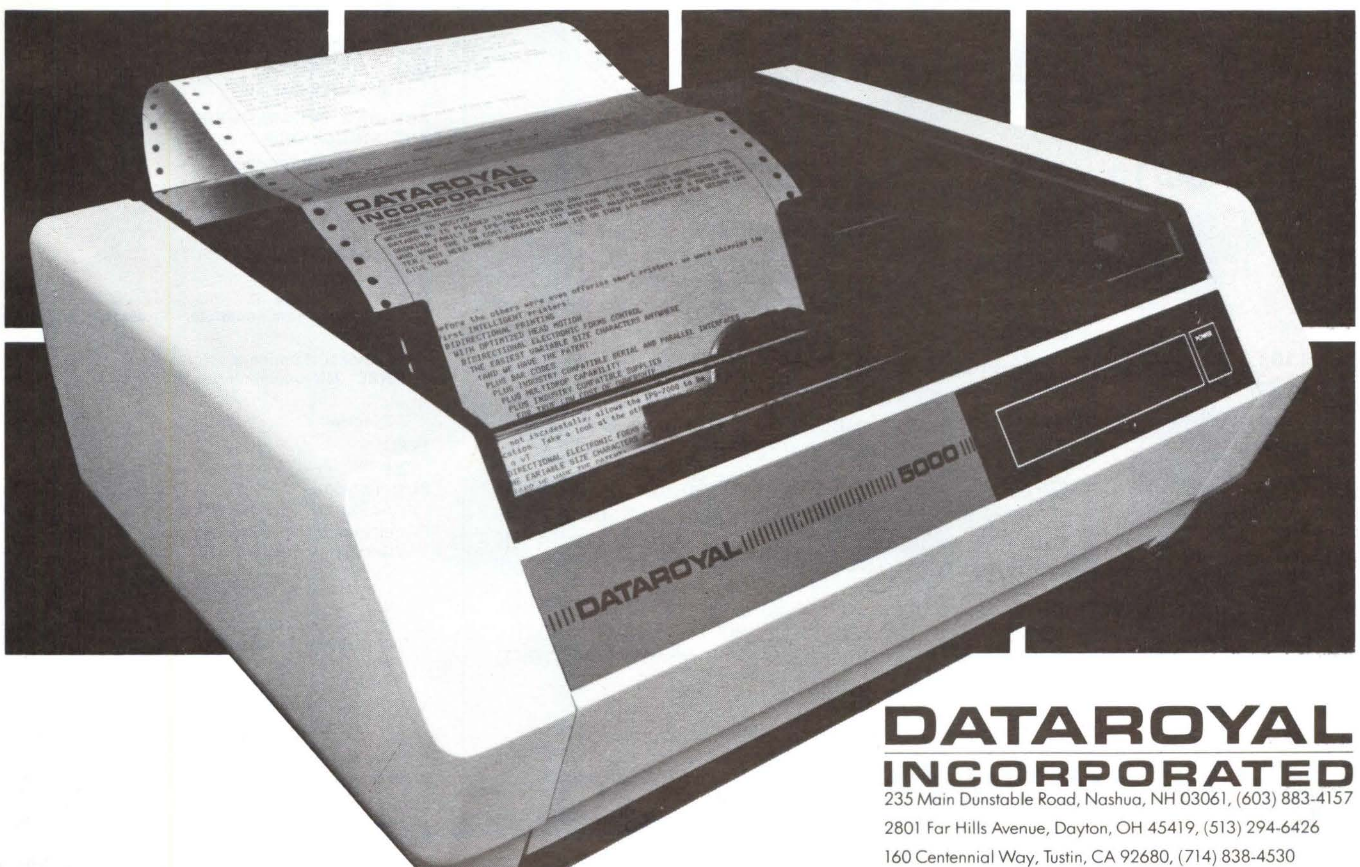


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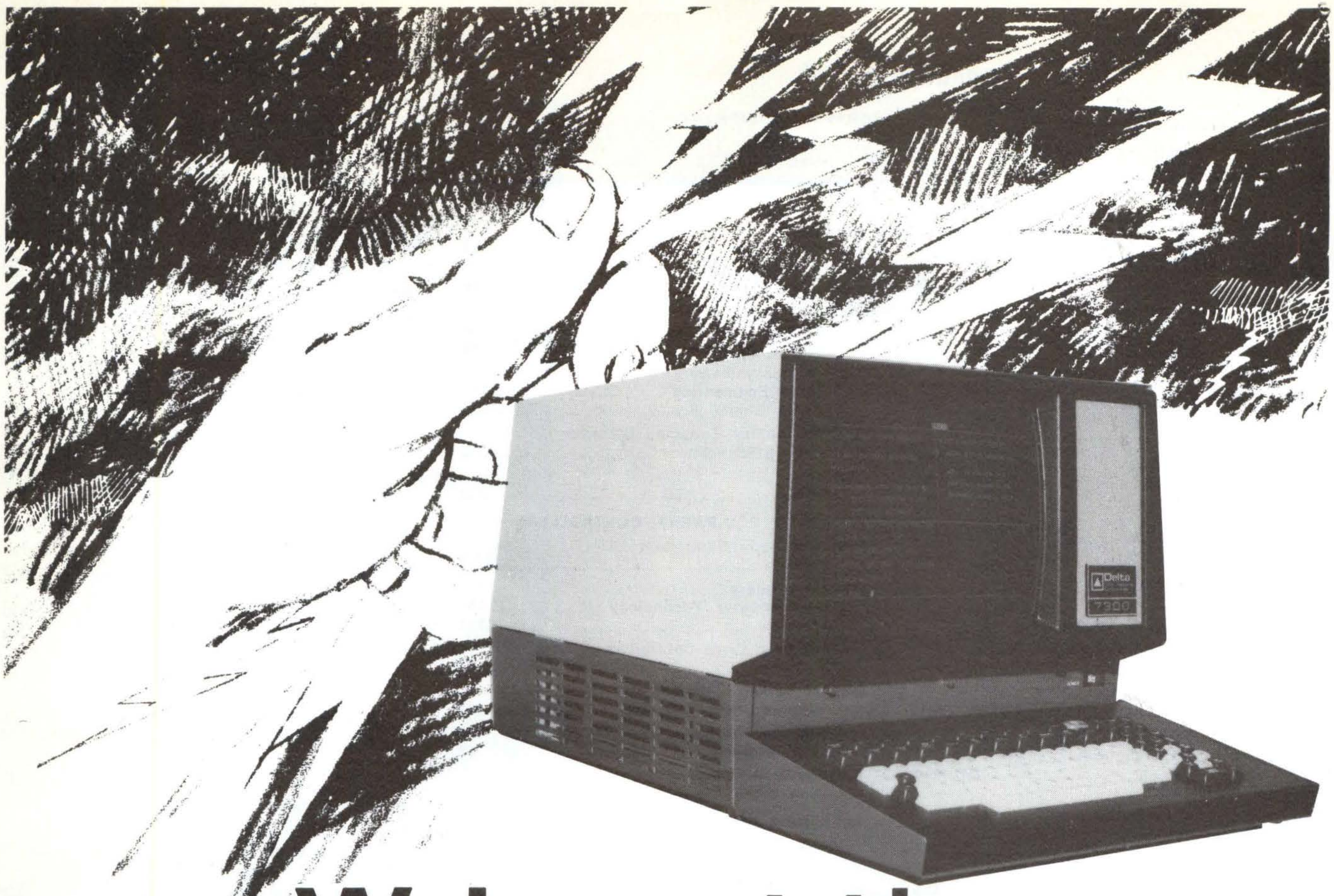
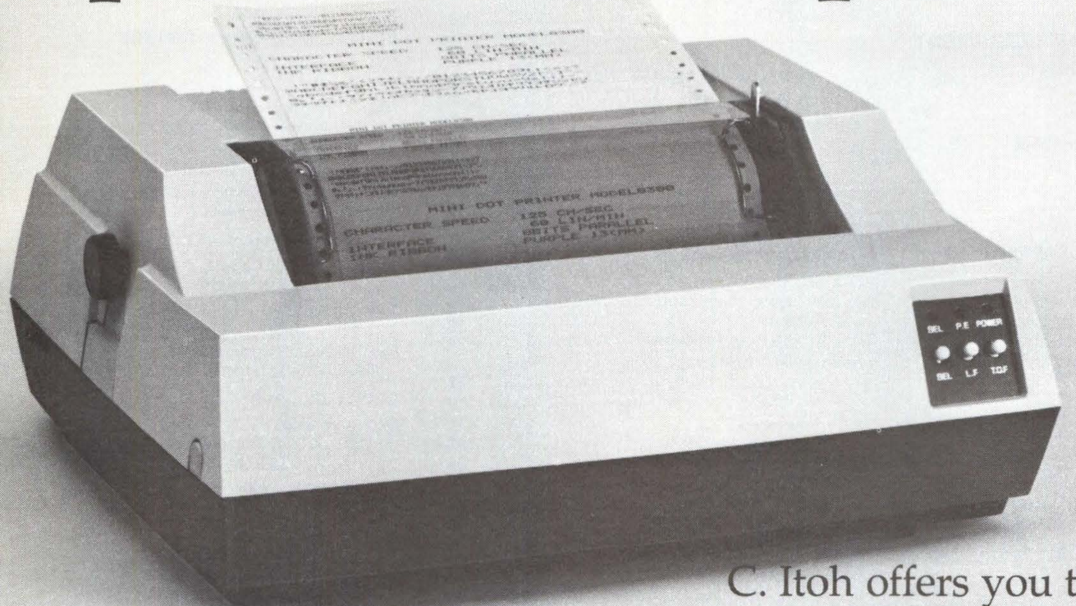
## GUIDE TO PRODUCT INFORMATION



# C. Itoh's Model 8300 printer looks superb.



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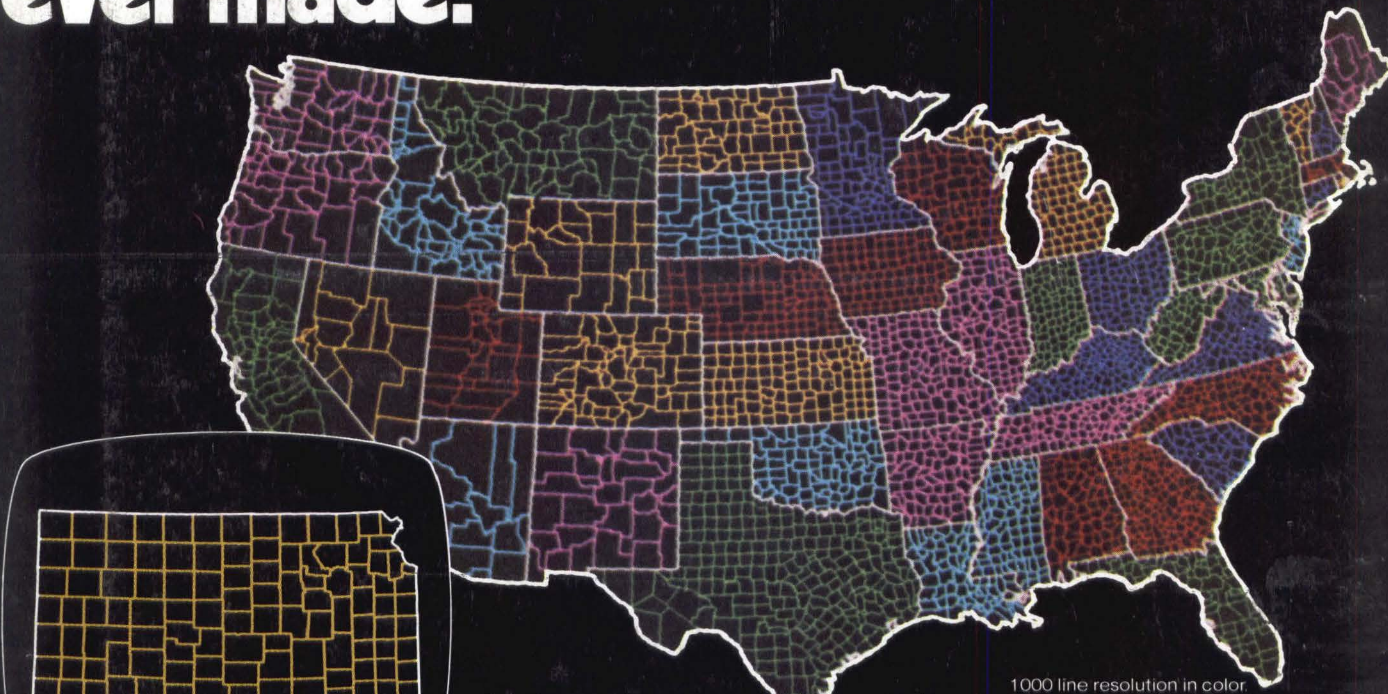

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