A PENNWELL PUBLICATION

COMPUTER DESIGN

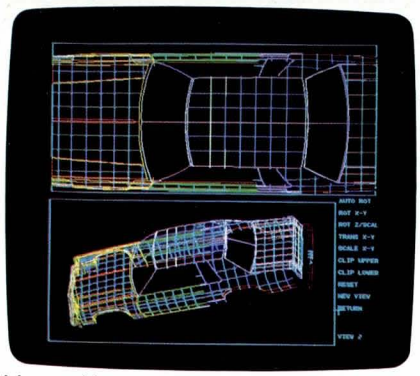
THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

MARCH 1981

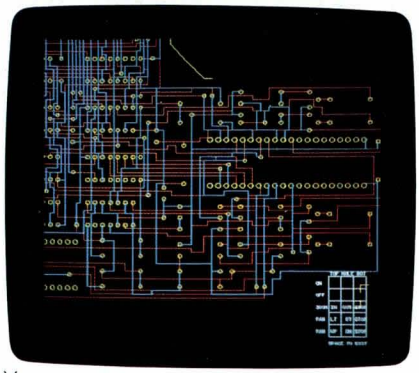
FUTURE DIRECTIONS IN COMPUTING

INTERCONNECTION SYSTEM APPROACHES FOR MINIMIZING DATA TRANSMISSION PROBLEMS

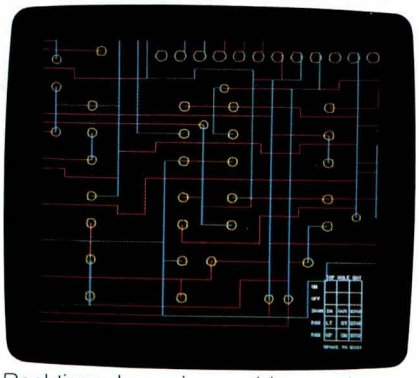
LOGIC ANALYZERS SIMPLIFY SYSTEM INTEGRATION TASKS



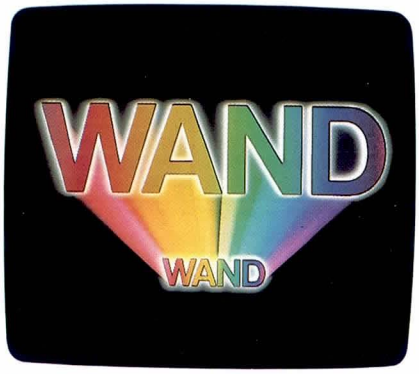
Megatek's new Whizzard 6250 raster system makes advanced computer graphics more economical than ever.



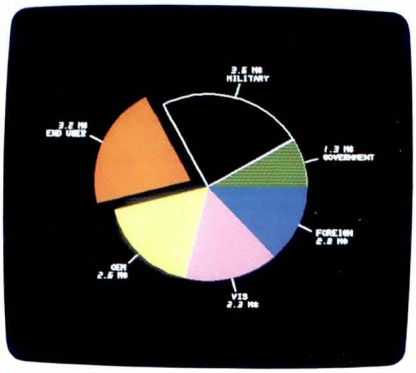
You can define your image in a 4096 x 4096 virtual space, with up to eight colors.



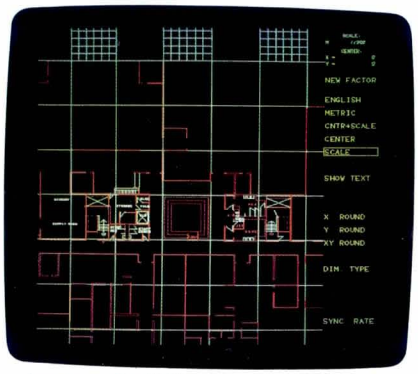
Real-time dynamics enable you to pan throughout this space, then zoom in with true scaling for added detail.



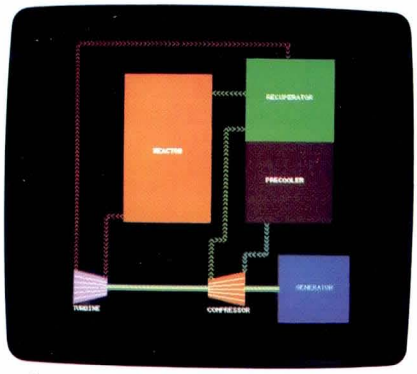
And our new system introduces you to low-cost, FORTRAN-based WAND software.



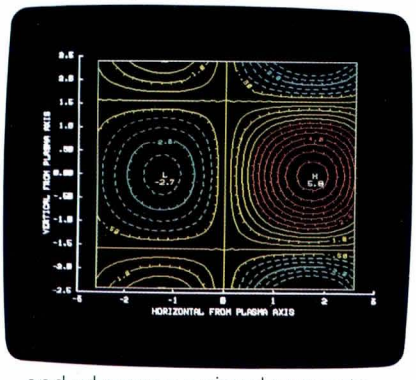
The Whizzard 6250 harnesses the power of Megatek technology for your business applications...



...for new flexibility in architecture and drafting...



...for an added dimension in process control...



...and wherever a visual presentation makes data easier to understand.

So imagine yourself at the Whizzard 6250 keyboard. Computer creativity has never been so affordable.

Imagine...all this technology for far less than you imagined.

At Megatek, we strive to set the standards for technology in computer graphics. Now we've set a new standard for value, too. Introducing our new Whizzard 6250 system.

It gives you graphics power you would expect from Megatek. For far less than ever before. You get the drama of full raster color. High resolution. Sophisticated dynamics implemented in hardware. Local vector memory. Double buffered bit planes. And the performance of advanced digital vector generation. Plus an RS-232 interface, standard.

The 6250 has its own version of easy to use WAND software. It's upward compatible to WAND 7200, software for our family of advanced systems and terminals.

MEGATEK

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The new Whizzard 6250 is the perfect starter system for end-users. OEM configurations are available too. Imagine all the possibilities. Better yet, write for all the facts. Megatek Corporation, 3931 Sorrento Valley Blvd., San Diego, CA 92121. 714/455-5590. TWX 910-337-1270. Megatek International/Europe 11 Woudstraat, 4031 JA Ingen, The Netherlands. Telephone: 31 3443-2800. TWX 70619.

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CIRCLE 2 ON INQUIRY CARD

Model 6450 shown in service position.

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CIRCLE 3 ON INQUIRY CARD

COMPUTER DESIGN®

THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

MARCH 1981

VOLUME 20, NUMBER 3

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Cover by Darcy Gerbarg
Created at the Computer Graphics Research Laboratory of the New York Institute of Technology

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Pseudorandom number generator blends modest software requirements with efficient organization of memory to achieve fast operation on almost any microprocessor used in modern data communications equipment

BPA

ABP

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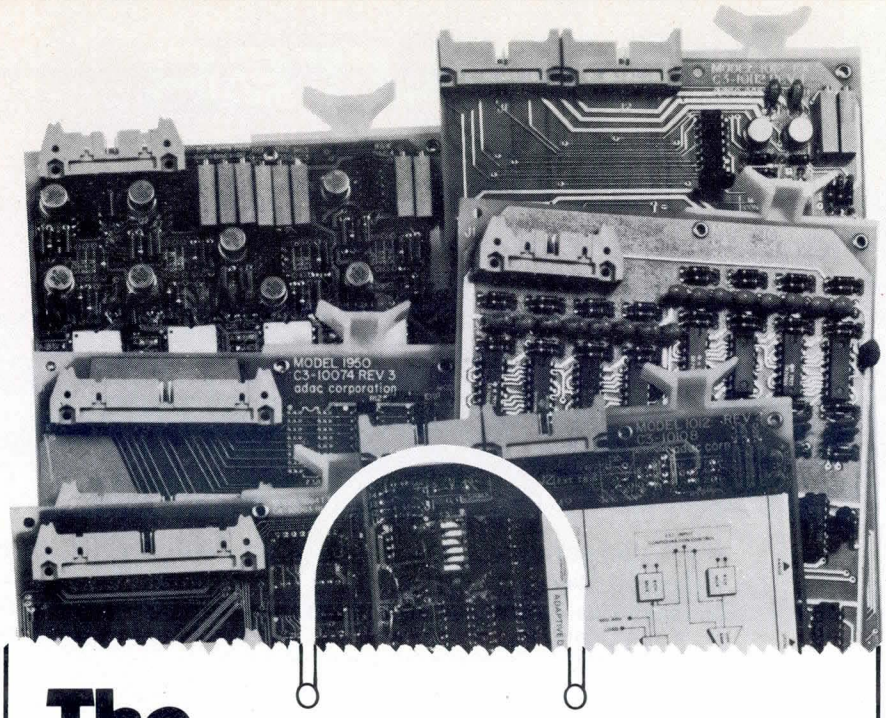

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1030	16-64 channels, high level inputs, 12 bit, 2 DACs
1112RL	8-16 differential low level and thermocouple inputs, 12 bit
1112RX	8-16 differential low level and thermocouple inputs, mux expander
1113	8-16 differential low level and thermocouple inputs, 12 bit, LSI-11/23 interrupt compatible
1113EX	8-16 differential low level and thermocouple inputs, mux expander, LSI-11/23 interrupt compatible
1412DA	1-4 D/A channels, voltage or current loop outputs

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SERIAL I/O CARDS

1750	Asynchronous line interface with two I/O ports

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1604/POC	2-4 pulse output channels
1616CCI	16 discrete inputs, contact closure detect
1616/MIC	16 discrete inputs with priority encoder
1616/OIO	16 parallel outputs, optically isolated
1616/OII	16 parallel inputs, optically isolated, can cause interrupt
1620TTL	16 latched inputs and outputs for DMA operation
1616HCO	16 discrete outputs, high current drive
1632HCO	32 discrete outputs, high current drive
1632TTL	32 TTL I/O lines
1664TTL	64 TTL I/O lines

BUS INTERFACE

1620DMA	Direct memory access controller
1900	Unibus to LSI-II translator
1950	Bus repeater
1900CT	Cable terminator card

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MEMORY...FROM THE LEADER

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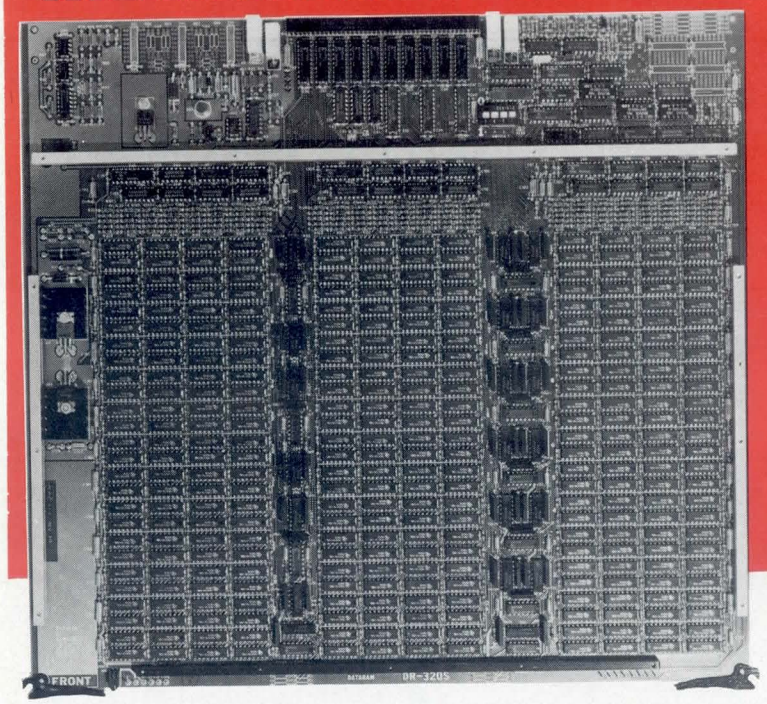
JUST ANNOUNCED
PDP 11/44 MEMORY



Perkin-Elmer 320 Series compatible 512KB ADD-IN

There's lots of good reasons to buy your ADD-ON/ADD-IN memory from the leader.

For starters, there's the wide range of core and semi mini-memories we offer. The industry's widest. In fact, Dataram is the only company in the world supplying minicomputer-compatible core and semiconductor main memory and disk emulation systems. The *only* company.

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India: Infosystems Private Limited, 79281 • **Israel:** Minix Computers & Systems Ltd., 03-298783 • **Japan:** Matsushita Electric Trading Co., Ltd., 06 (282) 5111

CIRCLE 5 ON INQUIRY CARD

BIOMATION K100-D

Got a glitch? Get a GLITCH FIXER FROM GOULD

Compare this general purpose logic analyzer with the currently accepted industry standard.

The K100-D wins over Hewlett-Packard's 1615A hands down!

Logic designers have made Gould's powerful Biomation K100-D our fastest selling logic analyzer

ever. You'll see why once you compare it to its nearest competitor, the 1615A from Hewlett-Packard.

Compare clocking speed.

With a 100 MHz clock rate, the K100-D gives you resolution to 10 ns—*five times better than the 1615A's*. Use the K100-D's latch mode to catch gliches as narrow as 4 ns. It gives you the most precise logic analysis for today's high speed minicomputer, mainframe and microprocessor systems. Best of all, you're already prepared for faster designs as they arrive.

Compare capacity.

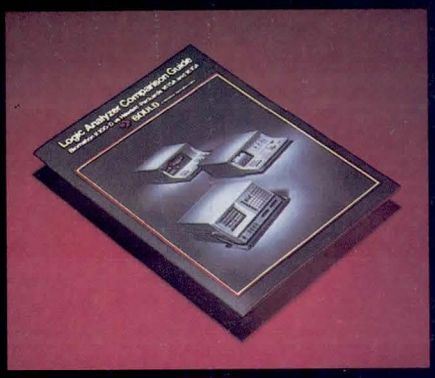
The K100-D's 1024 word memory is *four times as deep as the 1615A's*. This dramatically extends the length of data you can trap from your system at any one time. And that means faster, more accurate debugging. In addition, the K100-D's standard 16 channel format can be expanded to 32 channels for work on the new generation of 16-bit microprocessors.

Compare your productivity.

Finally, the K100-D makes designers more productive with convenience features superior to those of the 1615A. The K100-D has a larger keyboard, plus an interactive video display. Comprehensive status menu. Data domain readout in hexadecimal, octal, binary or ASCII. And the list goes on and on.

The final analysis.

To help you evaluate these two fine instruments before you buy, we've prepared a point-by-point *competitive comparison* of the two. If you're designing and debugging high-performance digital systems, you'll want to read this document carefully. To get your free copy, just use the reader service number or write Gould Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For faster response, call 408-988-6800.



Hewlett-Packard 1615A
A very good logic analyzer

Speed: to 20 MHz
Resolution: 50 ns
Memory: 256 words
Channels: 8 timing & 16 data, or 24 data

Biomation K100-D
The industry's finest logic analyzer

Speed: to 100 MHz
Resolution: 10 ns
Memory: 1024 words
Channels: 16 timing or 16 data, or 32 data

GOULD
An Electrical/Electronics Company

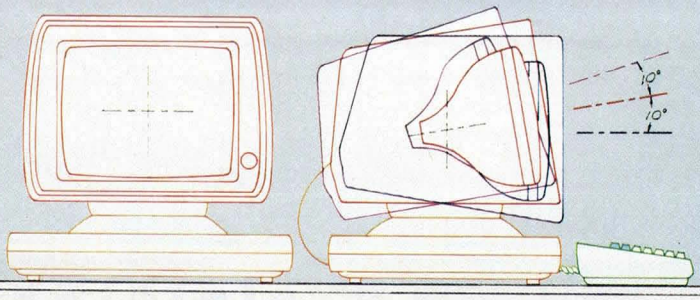
CIRCLE 6 ON INQUIRY CARD

THE ZENTEC SERIES 8000 INTELLIGENT TERMINALS

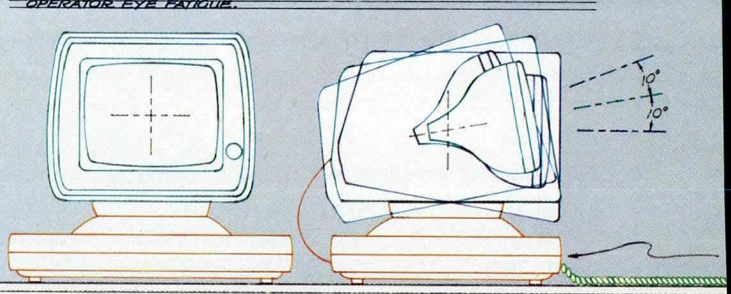
The first Intelligent Terminal designed specifically for OEMs to configure and for people to use.

THE ZENTEC 8002-15 A COMPLETE INTELLIGENT TERMINAL COMPRISED OF THREE SEPARATE MODULES, THE 8201 LOGIC BOX, THE 8302 (15") VIDEO MODULE AND THE 8401 KEYBOARD.

WITH THE 8002, THE 15" CRT IS BALL-JOINT CONNECTED TO THE TOP OF THE LOGIC BOX AND PROVIDES A CONVENIENT 20° ANGLE OF TILT AND A 60° ANGLE OF SWIVEL.



THE ZENTEC 8001 IS SIMILAR TO THE 8002 WITH THE SUBSTITUTION OF A 12" VIDEO MODULE, THE NON-GLARE, HIGH RESOLUTION CRT SURFACE WITH A WHITE, GREEN OR AMBER PHOSPHOR IS OFFERED TO REDUCE OPERATOR EYE FATIGUE.



With the Series 8000, Zentec successfully re-defines the words Human Engineering. Never before has there been a more powerful, more flexible, more operator-oriented video display terminal designed expressly for OEMs and system integrators.

The first thing you see on the CRT is the almost completely glare-free surface for reduced operator eye fatigue. The single knob right up front is used to turn the system on or off and to control the level of brightness. While a P31 green phosphor is standard, white or amber phosphors may be optionally provided. Character resolution and contrast go easy on the eyes, too, and wait until you see the character size on our 15" screen!

Configurability AND Flexibility

With Zentec's unique multiple-module concept, the 8000 may be easily configured with either a 12- or 15-inch CRT with full swivel and tilt, up to three snap-in printed circuit boards in the logic box for fast MTTR, and a wide variety of detachable keyboard styles. A single PCB is standard with the 8000, and the OEM may add one or two of his own PCBs. The standard logic contains Zentec's unique mini-computer-like bus architecture under the control of a powerful microprocessor. Hardware for synchronous or asynchronous communications and printer I/O is standard. The Zentec 8000 may be configured with 16, 32, or 64KB of RAM and 4, 8, 12, or 16KB of ROM or PROM. That's flexibility!

The microprocessor-controlled detached keyboard of the 8000 is canted 11° for operator comfort and the keys may be stepped, or optionally, sculpted.

Through Zentec, all OEMs can now offer a unique private label product so finely tuned to their customers' needs that it achieves the highest level of man-machine interface. For the direct story on the Zentec 8000, call us at (408) 727-7662, or write for our brochure.

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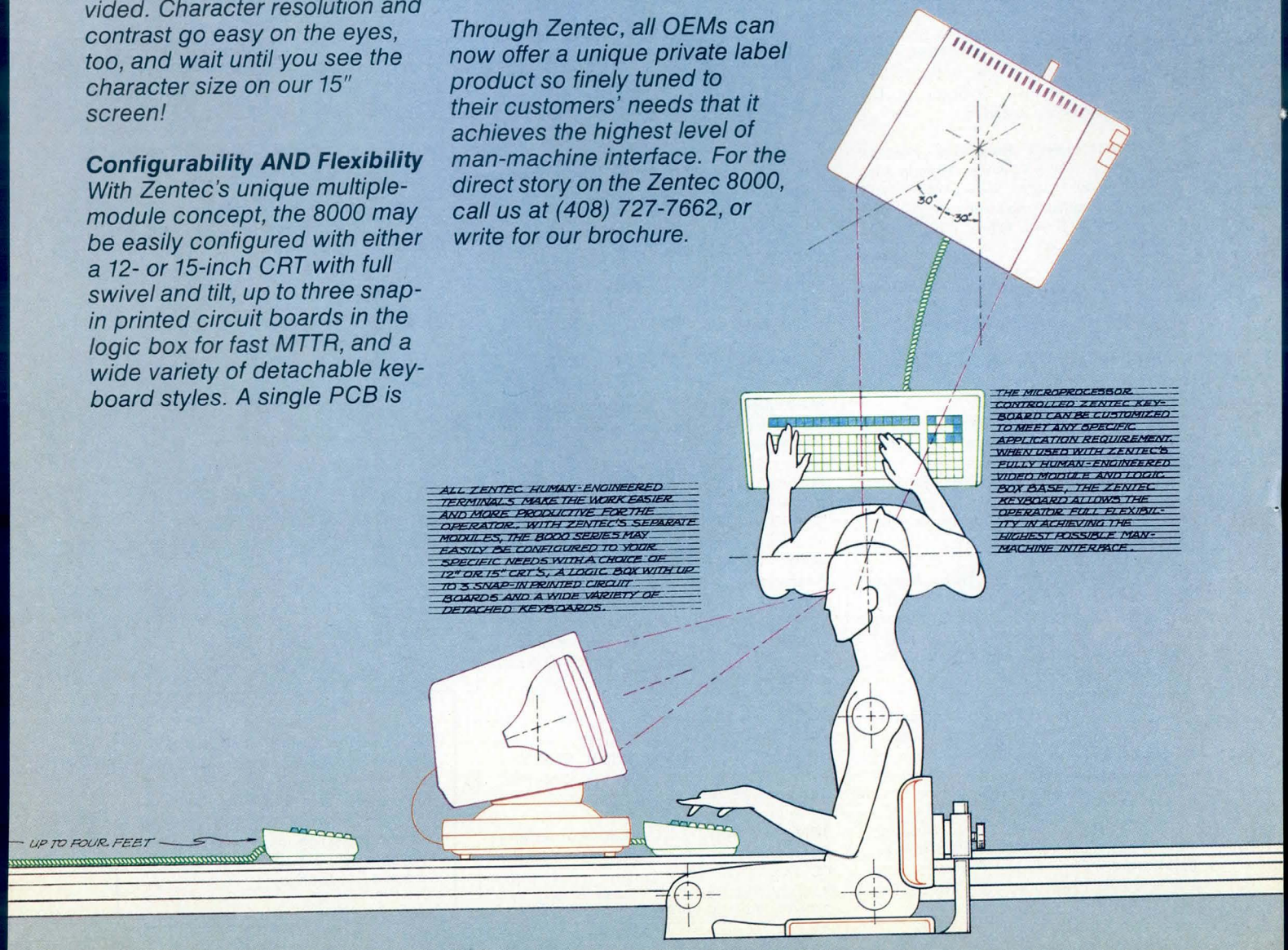

CIRCLE 7 ON INQUIRY CARD

CALENDAR

CONFERENCES

APR 2—Invitational Computer Conf, Sheraton Denver Tech Ctr, Denver, Colo. INFORMATION: B. J. Johnson & Assocs, Inc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

APR 3-5—West Coast Computer Faire, Civic Auditorium, San Francisco, Calif. INFORMATION: Computer Faire, 333 Swett Rd, Woodside, CA 94062. Tel: 415/851-7075

APR 6-9—Industry Oriented Spring Conf and Exhibit, Cervantes Conv Ctr, St Louis, Mo. INFORMATION: Instrument Society of America, 67 Alexander Dr, PO Box 12277, Research Triangle Park, NC 27709. Tel: 919/549-8411

APR 7-9—Electro, Coliseum and Sheraton Ctr, New York, NY. INFORMATION: Dale Litherland, Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

APR 7-9—Internat'l Reliability Physics Sym, Sheraton-Twin Towers, Orlando, Fla. INFORMATION: John Edwards, Gen'l Chm, American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051. Tel: 408/246-0330

APR 9-12—Southwest Computer Show and Office Equipment Expo, Market Hotel, Dallas Market Center, Dallas, Tex. INFORMATION: Bill Mayhan, Nat'l Computer Shows, 824 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

APR 27-29—IOOC '81 (Internat'l Conf on Integrated Optics and Optical Fiber Communication), Hyatt Regency, San Francisco, Calif. INFORMATION: Barbara Hicks, Optical Society of America, 1816 Jefferson Place, NW, Washington, DC 20036. Tel: 202/223-8130

APR 27-29—INFO/MFG (Information Management Expo and Conf for Manufacturing), McCormick Place, Chicago, Ill. INFORMATION: Banner & Greif, Ltd, 110 E 42nd St, New York, NY 10017. Tel: 212/687-7730

APR 27-30—National Design Engineering Show & ASME Conf, McCormick Place, Chicago, Ill. INFORMATION: Banner & Greif, Ltd, 110 E 42nd St, New York, NY 10017. Tel: 212/687-7730

APR 27-30—Powercon 8, Loew's Anatole Hotel, Dallas, Tex. INFORMATION: Powercon 8 Program Chm, Power Concepts, Inc, PO Box 5226, Ventura, CA 93003. Tel: 805/985-6978

APR 28-MAY 1—Society for Information Display Internat'l Sym, Grand Hyatt Hotel, New York, NY. INFORMATION: Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: 305/446-8193/4 (1 to 5 pm)

APR 30-MAY 1—An Assessment and Forecast of Computer Graphics Conf, Saddle Brook Marriott, Saddle Brook, NJ. INFORMATION: Bob Sanzo, Frost & Sullivan, Inc, 106 Fulton St, New York, NY 10038. Tel: 212/233-1080

MAY 4-7—NCC (National Computer Conf), McCormick Place, Chicago, Ill. INFORMATION: Gerard Chiffriller, 1815 N Lynn St, Suite 800, Arlington, VA 22209. Tel: 703/558-3600

MAY 5-8—PICA '81 (Power Industry Computer Applications), Marriott Motor Inn, Philadelphia, Pa. INFORMATION: T. A. Suman, Philadelphia Electric Co, 2301 Market St, N3-1, Philadelphia, PA 19101. Tel: 215/841-6397

MAY 11-13—Electronic Components Conf, Colony Square Hotel, Atlanta, Ga. INFORMATION: T. G. Graw, Bell Laboratories, Whippany Rd, Rm 3B-312, Whippany, NJ 07981. Tel: 201/386-3000

MAY 12-14—Internat'l Sym on Computer Architecture, Minneapolis, Minn. INFORMATION: Harry Hayman, Computer Architecture, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

MAY 20-22—MIMICOME (Internat'l Sym on Mini- and Microcomputers in Control and Measurement), Hilton Hotel, San Francisco, Calif. INFORMATION: P. L. Hsu, McDonnell Douglas Astronautics Co, 5301 Bolsa Ave, Huntington Beach, CA 92647. Tel: 714/896-3311

JUNE 10-12—CONPAR '81 (Conf on Analyzing Problem-Classes and Programming for Parallel Computing), Nurnberg, West Germany. INFORMATION: Wolfgang Handler, Immd, Universitat Erlangen-Nurnberg, Martensstrasse 3, D-8520 Erlangen, West Germany

JUNE 14-18—Second Annual NCGA Conf, Baltimore Convention Center, Baltimore, Md. INFORMATION: Society of Manufacturing Engineers, PO Box 930, Dearborn, MI 48121. Tel: 313/271-1500

JUNE 29-July 1—Design Automation Conf, Opryland Hotel, Nashville, Tenn. INFORMATION: Harry Hayman, Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

SEMINARS

APR 7-9—Survival and Growth of the Engineering Industries through Integration of CAD/CAM Technology, Carlton Hotel, Cannes, France. INFORMATION: Rhonda Gerganess, Computer Aided Manufacturing International, Inc, 611 Ryan Plaza Dr, Suite 1107, Arlington, TX 76011. Tel: 817/265-5328

MAY 16—Introduction to Pascal, Squibb World Hdqtrs, Princeton, NJ. INFORMATION: Bill Hafstad, EDUCOM, PO Box 364, Princeton, NJ 08540. Tel: 201/457-4055

SHORT COURSES

APR 1-3—Data Communications Systems, Sheraton Tara Hotel, Framingham, Mass. INFORMATION: Amer Inst for Professional Education, Carnegie Bldg, Hillcrest Rd, Madison, NJ 07940. Tel: 201/377-7400

MAY 4—General Purpose Interface Bus Workshop, Intel Training Ctr, San Francisco, Calif. INFORMATION: Ben Catanzaro, MCSD Customer Training SV3-1, 1350 Bordeaux Dr, Sunnyvale, CA 94086. Tel: 408/734-8102

JUNE 15-19—Info System Technology: Database and Performance, U of Mich, Ann Arbor, Mich. INFORMATION: Engineering Summer Confs, 200 Chrysler Ctr, N Campus, U of Mich, Ann Arbor, MI 48109. Tel: 313/764-8490

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CIRCLE 8 ON INQUIRY CARD

Local Area Networks Overview—Part 2: Standards Activities

J. Michael Kryskow
C. Kenneth Miller

Concord Data Systems, Inc
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Because of the diverse applications and definitions of local area networks, many different approaches have been taken to solve the local network problems that were described last month.* Three major groups in the U.S. are currently attempting to develop a local area network standard, or industry *de facto* standard. Each group is aiming at potentially different functional requirements and application objectives.

Purdue Workshop/Proway (TC5A of IEC/SC65A/WG 6) is a standards body defining local area networking for industrial applications. DEC/Intel/Xerox (DIX) is a 3-company combine engaged in solving local area network problems with particular emphasis on office automation. The IEEE Computer Society Local Area Network Standards Committee is a body trying to develop access and protocols in a layered approach similar to the ISO Open System Interconnection (OSI) layered protocol. The IEEE architecture is defined in a layered approach where media, distance, and topology can be independent. The Committee's objective is not to preclude any application. Certain parameters common to all three approaches are shown in the Panel. For ease of comparison, the work of all three standards bodies will be compared to the more familiar standards work of the ISO/OSI architecture (Fig 1).

Proway

Proway standards work has been in progress for several years. The Proway standard is oriented to the process control and industrial environment and requires realtime control and a guaranteed access time to the network. These applications result in several unique functional requirements.

Reliability—The system is to be defined in a manner that failure of a single device will not bring down the common resource medium. This requirement includes a timeout mechanism (JABBER CONTROL) that automatically disconnects a station after it has been transmitting for a period greater than the timeout. Also, redundant modems and taps and/or media are required. In addition, no active components can be used in the medium.

Realtime Control (Priority)—The access method must provide a priority mechanism that allows high priority users (demanders) to communicate in an expeditious manner on the medium. The current specification requires that a single demander gain access in less than 2 ms.

Flow Control at Link Level—Each station will have prior knowledge of allowable stations with which it can communicate on the system.

Broadcast, Message Transfer, and Transactions—There are three defined mechanisms for passing information between users. One (Datagram, broadcast) requires no acknowledgment in the communication protocol. Another (message transfer) requires an acknowledgment from the link transport or applications in a manner that is not time-critical. The third (transaction) is an uninterruptible (by any other device) transfer of a command/response pair across the medium.

The basic system architecture of Proway has not yet been finalized, but it can be roughly outlined and compared to ISO/OSI. Detailed information on frame, interface, and physical breakdown are shown in Figs 2(a) and 2(b). Concentration in effort has been on defining the media, modem coupler, coupler interface, link control layer path unit, and the requirements for access, acknowledgment, and reliability. Currently, Proway specifies a 1M- to 2M-bit/s data rate over 75-Ω RG-6 baseband coaxial cable.

In general, the system has been adhering to the form of standard RS-232/422/423 DTE/DCE interfaces and modified frame structure, using HDLC, available protocol integrated circuit (IC) chips, and ISO/OSI layered structures. It differs somewhat from the DIX

Parameters Common to Proway, DIX, and IEEE Local Network Approaches

- Primary emphasis is bus topology
- More rigorous error protection mechanism than just 16-bit CRC
- Peer to peer link protocol requirements
- Source/destination addressing
- Layered approach to system architecture
- Coaxial cable media
- Requirement for access technique

*J. Michael Kryskow and C. Kenneth Miller, "Local Area Networks Overview—Part 1: Definitions and Attributes," *Computer Design*, Feb 1981, pp 22-35

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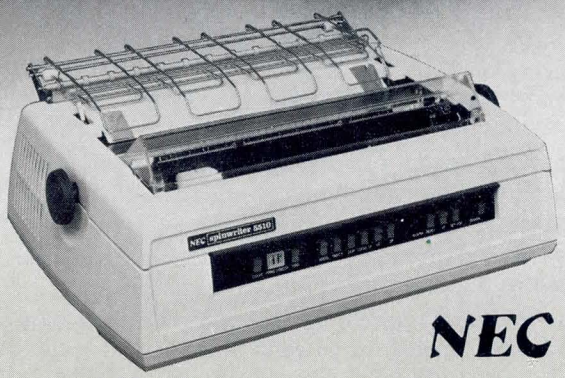

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CIRCLE 9 ON INQUIRY CARD

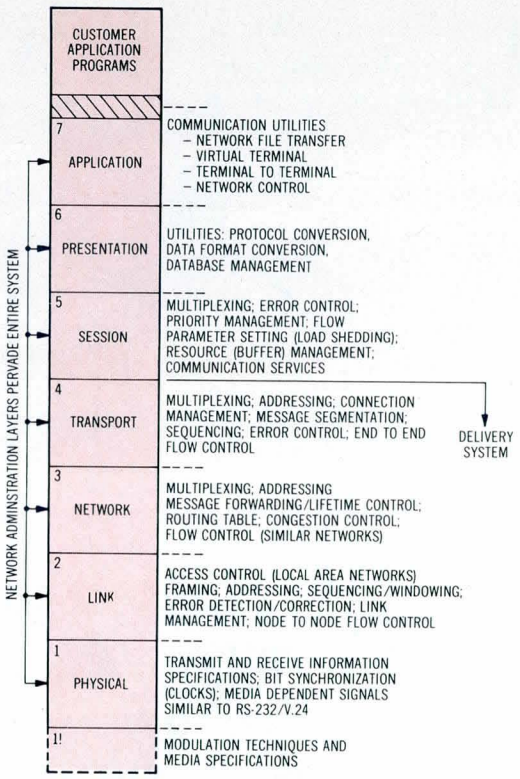


Fig 1 ISO/OSI structure for communications systems

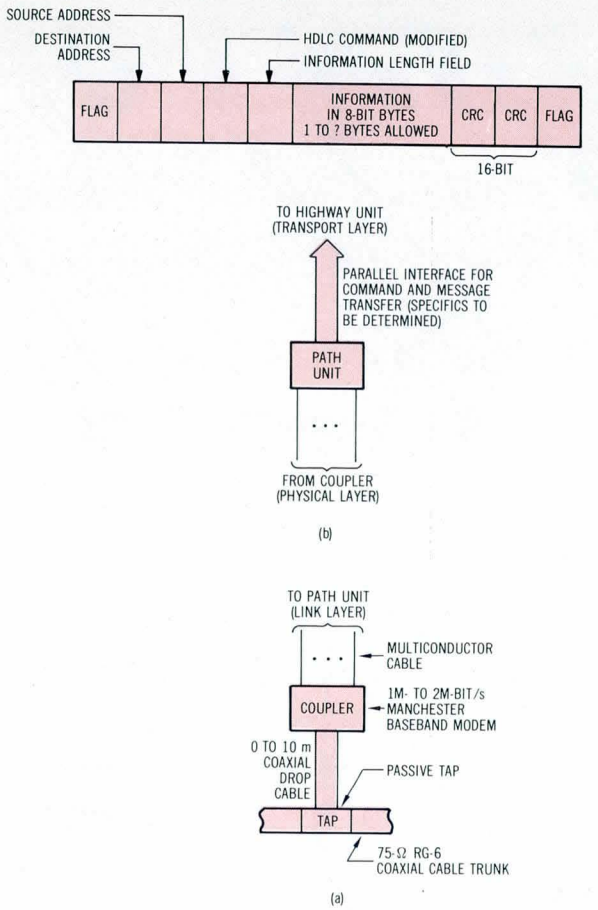


Fig 2 Proway physical layer (a). There are no active components in trunk line; provisions are made for redundancy in coupler, drop line, tap, and trunk. Multiconductor interface is similar logically to RS-232-C and electrically to RS-422 and -423

Proway link layer (b). Highway unit including network and transport layers have not been adequately defined at this time. Access mechanism leans toward tokens but is not yet defined. HDLC frame is used (flags and bit stuffing). Command field is not yet defined but is similar to ADCCP. Information length field is added for data integrity. Source and destination addresses are both extendable as in HDLC; upper limit not defined

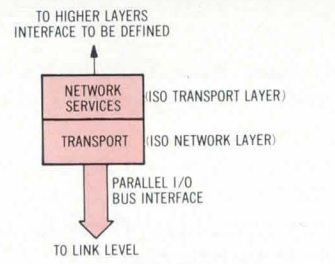
and IEEE approaches in its requirement relative to priority (urgency) and "transactions." Also, flow control is mandatory at link level. This tends to make carrier sense multiple access/collision detection (CSMA/CD) contention access techniques and Datagram messages at link level unpalatable to Proway. The tendency of Proway is to expand HDLC into a peer link protocol, using HDLC/ADCCP and "standard" ICs to develop a more rigorous access technique than CSMA/CD. In fact, Proway has recently stated a preference for the use of tokens as the access method. It is expected that Proway activities will come to completion in one to two years.

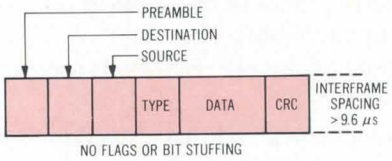
DEC/Intel/Xerox Combine (DIX)

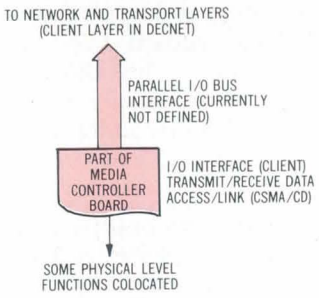
The DIX work began a little over a year ago and appears to be based on past work done on Ethernet and Decnet. The approach, however, is tightly coupled to a local (less than 2.5-km) cable environment for office automation. DIX current architecture at link level is characterized by no sense of priority, non-critical access times, and no realtime control requirement.

There are other principal characteristics of the DIX approach:

1. The network data rate is 10M bits/s, using Manchester baseband modulation over 50-Ω coaxial cable;
2. High impedance active taps (transceivers) are used to tie in to the medium;
3. There is no requirement for acknowledgment at the link level, therefore no control field;
4. Access method is CSMA/CD, derived from Ethernet;







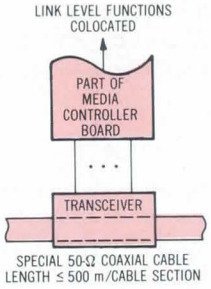
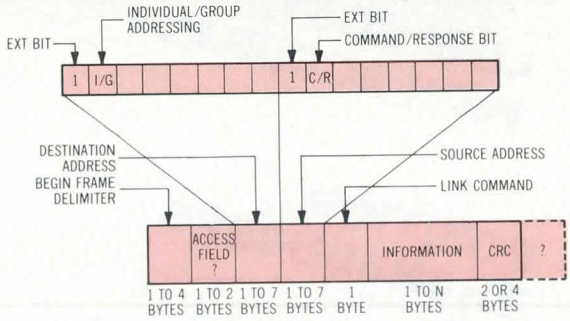
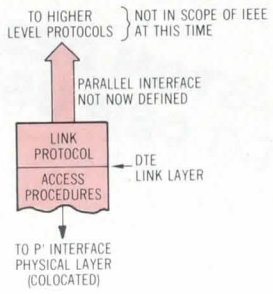


Fig 3 DIX physical layer (a). Drop line consists of five 78-Ω shielded twisted pair and carries transmit and receive modulation (Manchester encoded, 10M bits/s), carrier detect, collision detect, and power for transceiver. Special puncture tap in transceiver penetrates cable and contacts center conductor. Active components in transceiver act as zero-length stub, with transformer coupling to drop cable and direct coupling to trunk cable. Circuitry to detect carrier and collision, and hard limit Manchester modulation must be isolated from earth ground

DIX link layer (b). 32-bit preamble identifies start of frame. 64-bit source and destination addresses are globally unique—first bit in address field determines unique or multicast address. 16-bit type field defines different network routing structures. Data field (8N bytes, N = 46 to 1200) must be padded to 46 bytes min. 32-bit CRC is used for increased data integrity. End of frame is detected by carrier drop on last bit of CRC. Frame size is 72 bytes (576 bits)*min. There is no link field, Datagram service only at link level, and also no link layer priority mechanism. Access is CSMA/CD

DIX higher layers (c). Network and transport layers deal with flow control, acknowledgment, failure recovery (checkpointing), and prioritization algorithms. These layers are not currently finalized. Emphasis in network services layer is based on Decnet. Transport layer allows for different network types





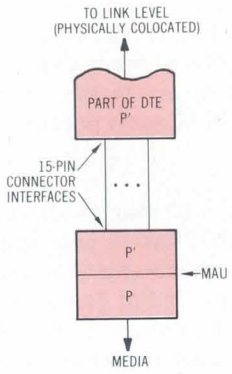


Fig 4 IEEE physical layer (a). Drop cable of five 75- to 150-Ω shielded twisted pairs up to 50-m long handles ECL, electrical drivers/receivers, data/clock; Manchester encoded—control by encoding violations. Data rates are 1M, 5M, 10M and 20M bits/s. Media access unit (MAU) is active and powered by DTE. P' section handles encoding/decoding of P' signals, frame delimiters for some media, eg, pre- and postambles and deals with disconnect, JABBER, and test functions. P section handles media/modem functions. Three MAU types are being considered to handle access by token only, CSMA/CD, or either. Media interface can be different for different media: baseband coax through passive or active taps, CCTV-type broadband, or optical fiber are being considered. Baseband modulation is likely differential Manchester encoding; broadband as yet undefined

IEEE link layer (b). More than one access procedure (CSMA/CD, token) being considered. Beginning of frame undefined; leaning to preamble or physical layer delimiter. Access field will be implemented for token access, not yet defined. Destination and source address extensions are similar to HDLC and support individual and multicast (group) addressing. Link control is similar to asynchronous balanced mode of ADCCP plus Datagram service. End of frame to be determined, leaning to postamble. Also, minimum frame or method to extend frame in CSMA/CD access is to be determined, as is "N" in information frame. There are two classes of service, Datagram and acknowledged

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5. All stations have fixed-length (48-bit) globally unique station address, assigned and administered by DIX;

6. There are no flow control procedures or connections at the link level;

7. Transport and a network service layer are included within the architecture;

8. No flags or bit stuffing is performed; frame delimitation is done at the physical level by using pre- and postambles; and,

9. Minimum frame size is 512 bits independent of information field.

The basic layers and their functions are listed and compared to ISO/OSI in Figs 3(a), (b), and (c). It is important to note that the DIX approach was not one of dependence on standard ICs or other standard protocols (like Proway). This allows greater architectural flexibility; it potentially allows for broadcast, multicast, and individual addressing on an IC that includes frame, address, and error recognition circuitry.

To sum up, the DIX approach to local area networking primarily addresses office automation in a layered approach, has no priority, with the bottom two layers operating in an unconnected (Datagram) mode, and the higher two layers dealing with acknowledgment and flow control. The DIX work at link layers and lower is complete, with specifications released to the public in Nov 1980.

IEEE Computer Society Local Network Committee, Project 802

IEEE standards work, in progress for about a year, has perhaps the widest set of functional requirements and the most ambitious and rigorous schedule of the three bodies. The intent of the IEEE standard is to handle more diverse applications than those addressed by DIX, eg, digitized voice and prioritized environments, but not to specifically preclude the Proway applications to any great extent. Thus, the IEEE is attempting to accommodate characteristics included in both Proway and DIX, which objectives have led to the following desirable goals of this standards effort:

1. Attempt not to limit (distance, topology, and number of stations) physical layer with restrictions from higher level functions (namely, access);

2. Allow higher levels not to preclude large topology applications such as pipelines, large city and industrial complexes, and satellite communications;

3. Allow a sense of priority in the access mechanisms—however, not necessarily oriented toward realtime control;

4. Support of broadcast, multicast, and individual addressing;

(continued on page 19)

CIRCLE 11 ON INQUIRY CARD

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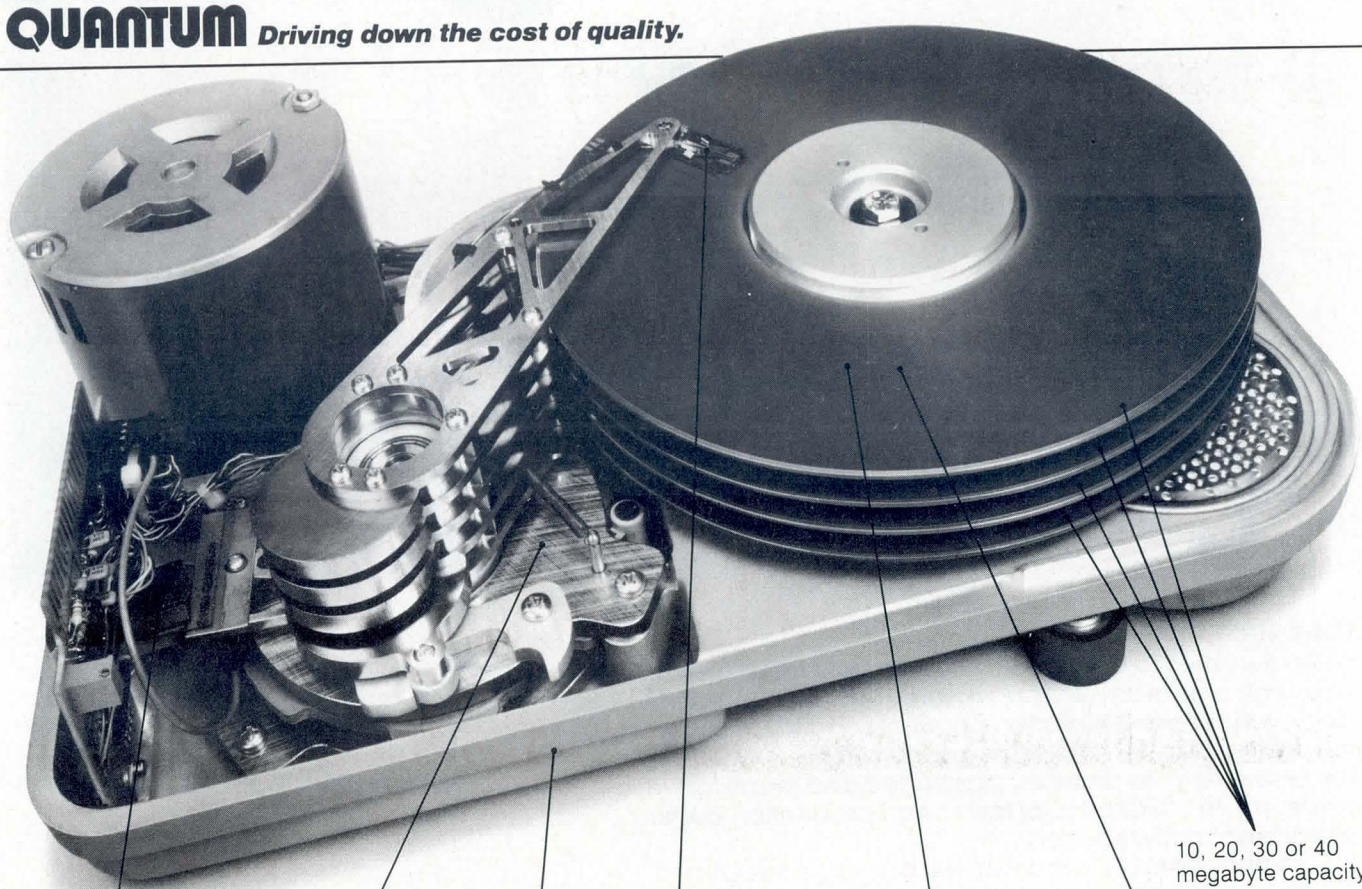

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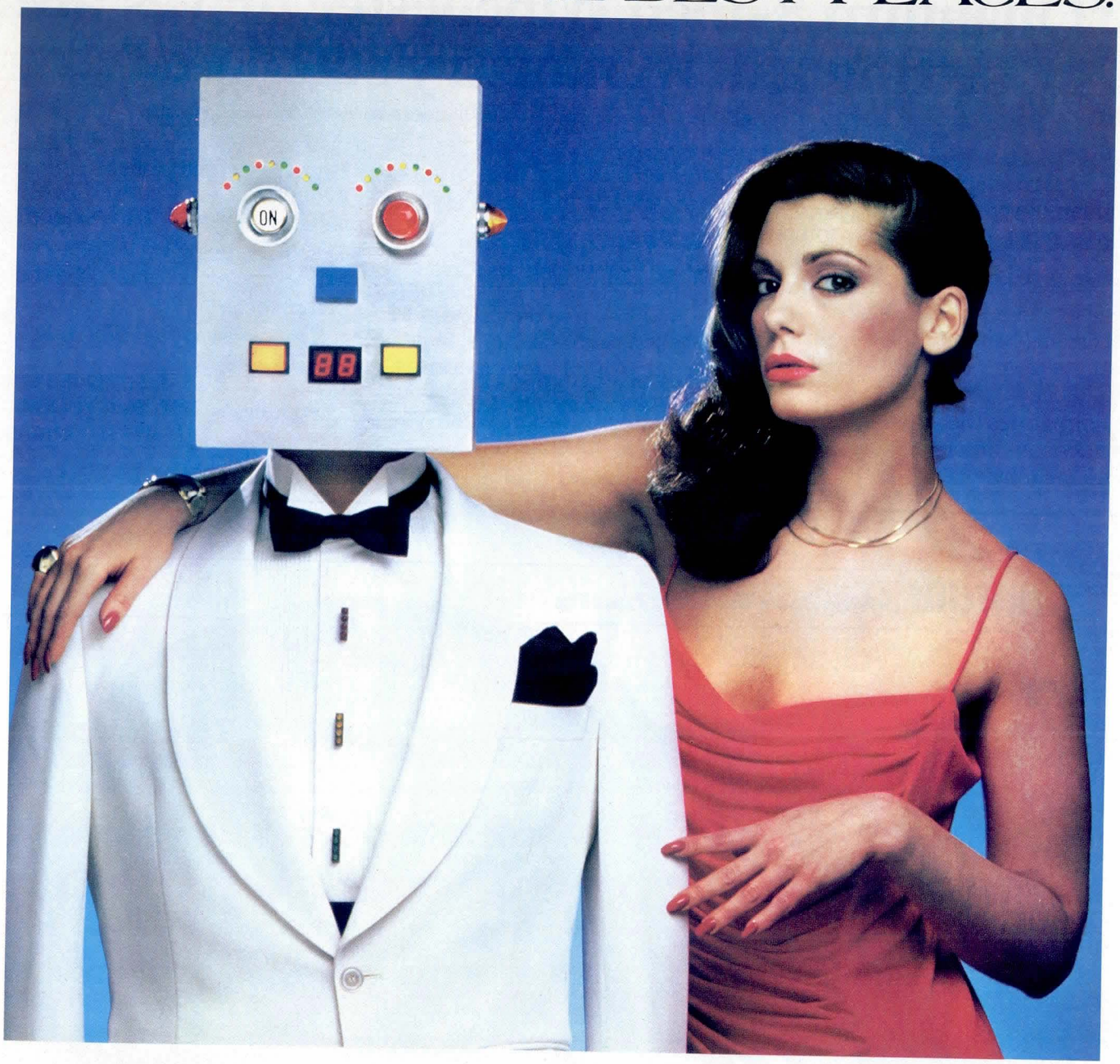

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5. Allow for both Datagram (unrestricted and no state information) and peer (with state information and some flow control) acknowledged communications at the link level;

6. No inclusion of the network or higher layers in their standards work, but a willingness to contribute to standardizing those layers, closely following the ISO/OSI structure and other standards activities; and,

7. Require some form of information exchange at the link level for exchanging identification and for administrative functions.

Figs 4(a) and (b) provide a more detailed description of the IEEE protocol structure, again referenced to ISO/OSI.

The most significant and controversial event in the past few months in the IEEE standards work has been the recent agreement (Dec 1980) to support two access methods, CSMA/CD similar to the DIX approach, and token. Before the Nov 1980 meeting it was generally assumed that the adopted access method would be a form of CSMA/CD, since it is the most understood and implemented technique in the U.S. and is being heavily promoted by DIX. At that meeting, however, many CSMA/CD deficiencies and token access advantages were delineated, causing Committee members to question the wisdom of recommending CSMA/CD. This was a rather extraordinary event, given the weight of the DIX companies, and the existence of their system specification.

Limitations of space preclude an adequate discussion here of the pros and cons of CSMA/CD vs token access. However, a brief synopsis of the advantages and disadvantages of each access method may serve to provide a perspective on the turnaround in IEEE thinking. Some of the advantages of the CSMA/CD access approach are: it is simple to implement the access algorithms; it performs well under light loads; there is a transparent connection to the medium; and it is transparent to a large number of users under light load conditions. Some of the disadvantages of CSMA/CD are that the non-deterministic mode of access means that maximum network access time cannot be guaranteed; requirement for collision detection limits the size of the network in baseband coaxial systems, and makes it very difficult to implement in broadband coaxial systems; there is a distance/network speed dependency, ie, frame size is tied to the medium for a given network data rate; under high network loading the network goes unstable—an increase in users demanding access to the network can actually result in a reduction of total system throughput; and, it is difficult to diagnose and troubleshoot because there is an error vs load dependency, ie, the access mechanism can cause errors.

By comparison, the token access method has the following advantages: access time may be guaranteed

(continued on page 20)

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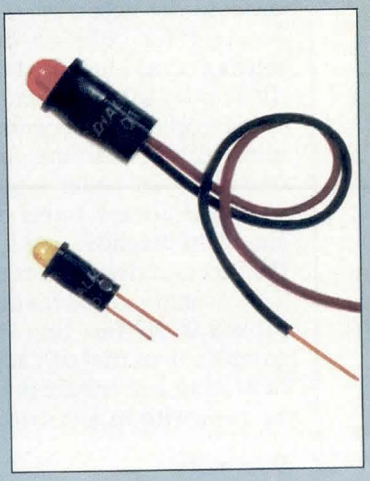

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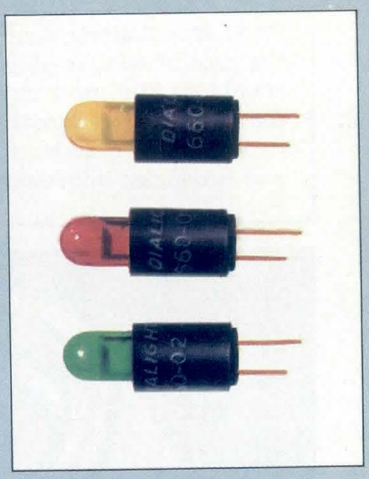

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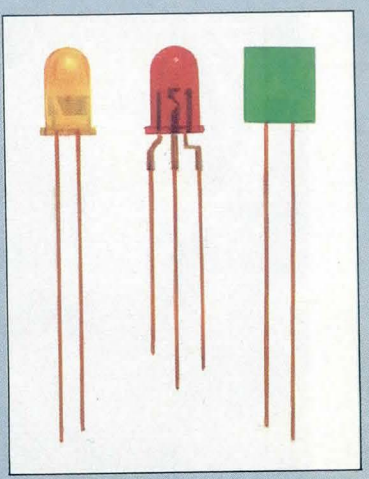

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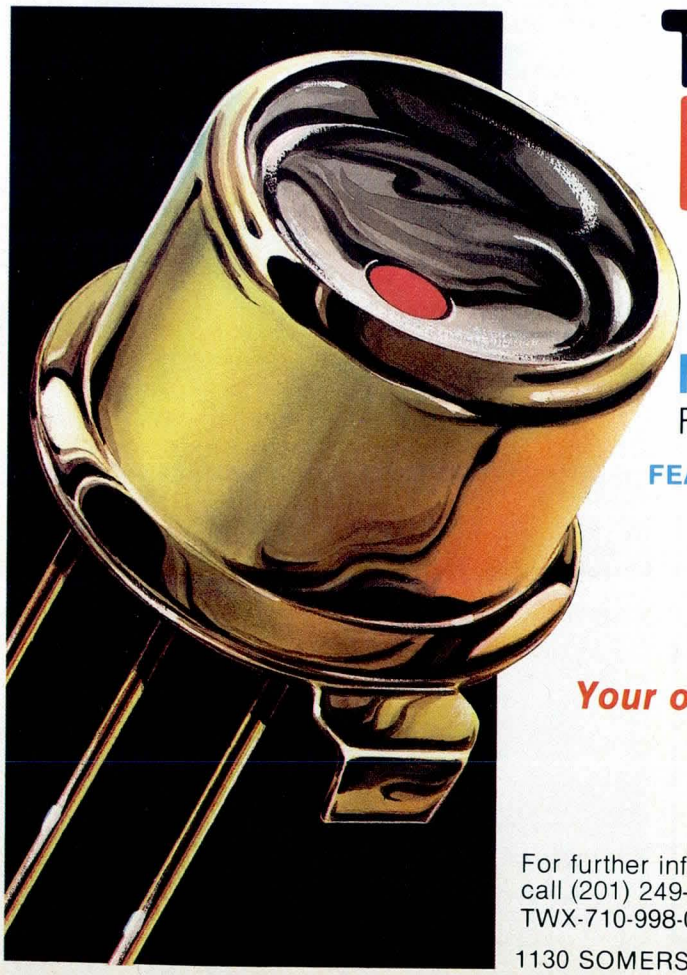
because the access method is deterministic; there is no need for collision detection (listen while transmitting) thus allowing long distances and eliminating difficulties with different media; there is no distance/speed/topology dependence; guaranteed response allows for realtime prioritized applications; it operates well under large load and distance and the system is always stable regardless of load; and, it is simple to diagnose and troubleshoot the system since the access is deterministic and does not create errors. The primary disadvantage of the token access approach is the fact that the access algorithm is more complex than that of CSMA/CD. For example, bus initialization and failure mechanisms of stations need to be dealt with in a distributed fashion.

Summary

Two standards bodies and a 3-company combine (DIX) are all attempting to generate standards, or in the case of DIX, establish an industry-wide *de facto* standard. The most encompassing effort is that of the IEEE. This approach supports different media, two alternative access methods, specific, multicast, and broadcast addressing, and Datagram as well as full acknowledging link protocols. In short, the resultant IEEE standard when completed (currently scheduled for June 1981) should provide the tools to allow simpler and more cost effective networks offering a larger range of services to the user.

Passage of the IEEE and Proway standards will start an unprecedented growth in local area networks. Companies with vested interests like the DIX group will resist meeting the standard, but as in the case of the CCITT X.25 packet-switched public data network recommendation, these companies will eventually conform to the standard. The authors predict that non-standard approaches such as currently offered by DIX, will at first gradually and later more rapidly lose influence.

The presence of standards will help to stimulate explosive growth in the field, so that currently separated information and control centers within homes, offices, cities, hospital complexes, and industrial environments will be tied together with high rate data communications. This proliferation of information and communications capabilities could well indeed validate the futuristic predictions made in James Martin's *Wired Society*.



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CIRCLE 15 ON INQUIRY CARD

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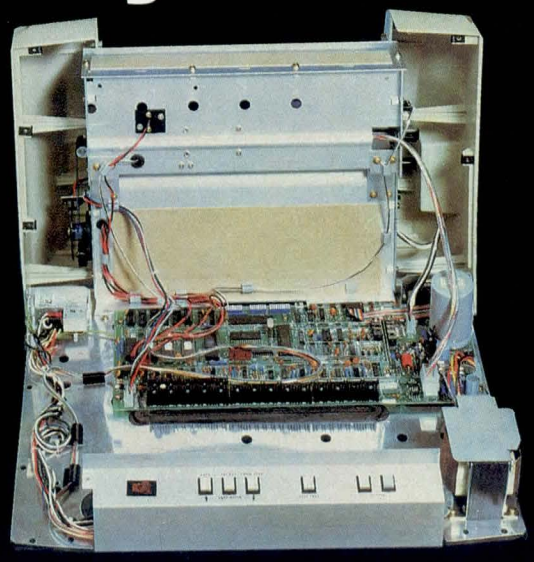

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The three ASCII compatible interfaces (parallel, RS-232-C and current loop) are standard, so connecting your computer is usually a matter of plug-it-in and print. Also standard are: a sophisticated communications interface for printer control and full point-to-point communications, DEC PROTOCOL, and a 700 character FIFO buffer. An additional 2K buffer is optional.

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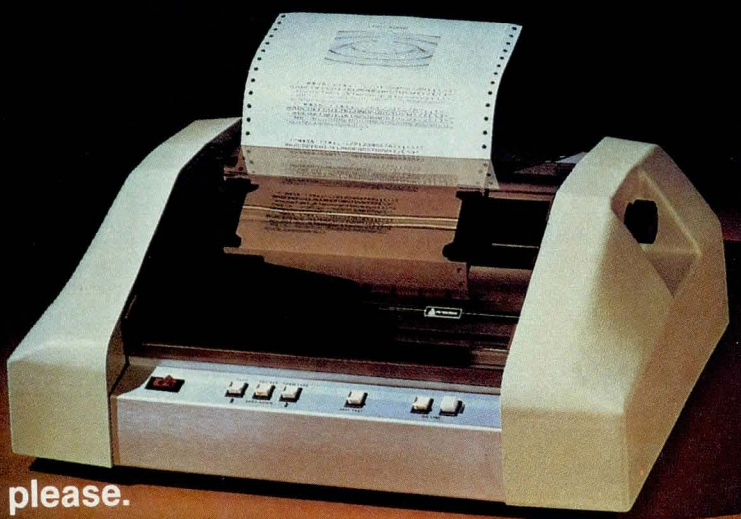

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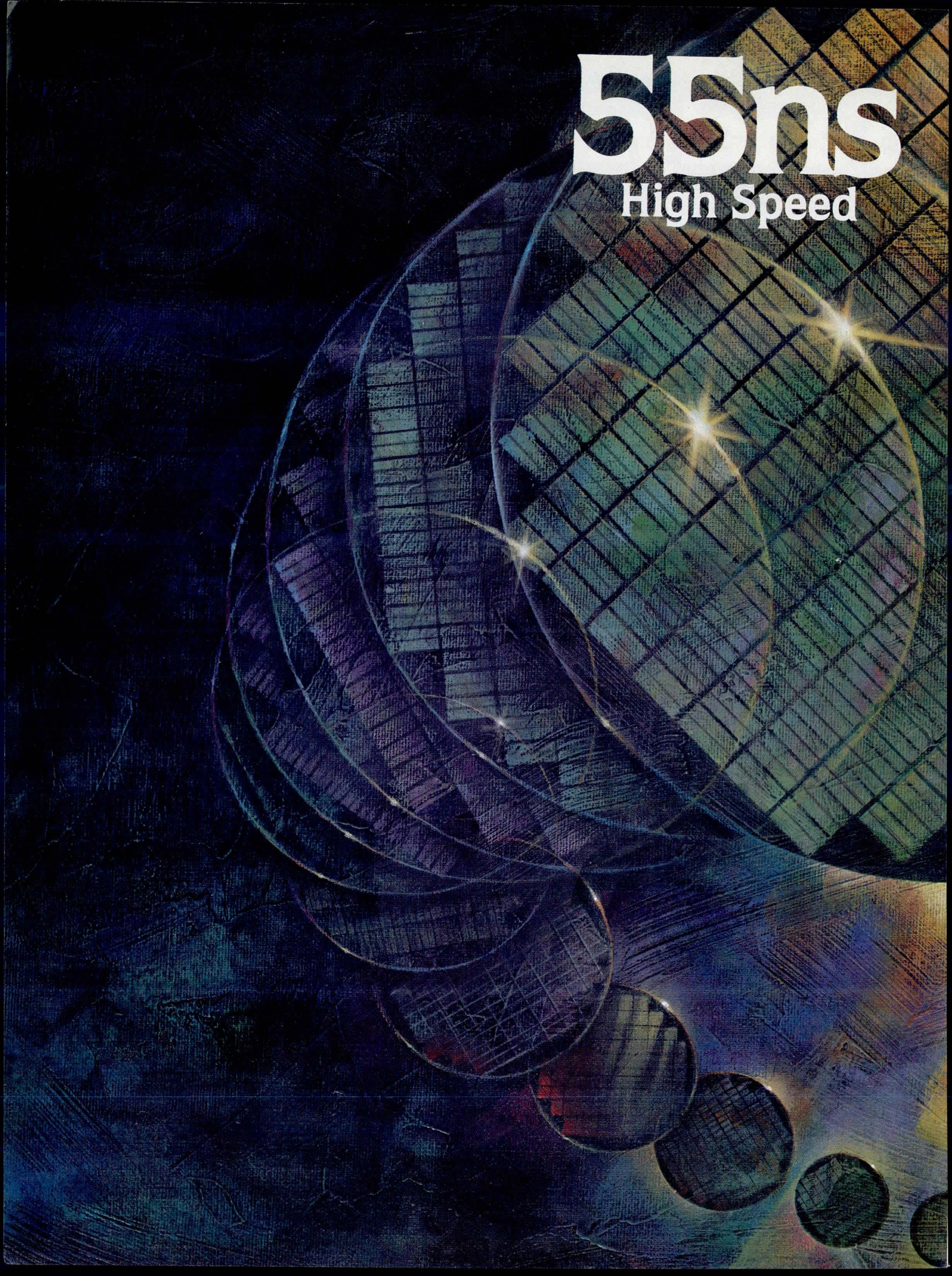
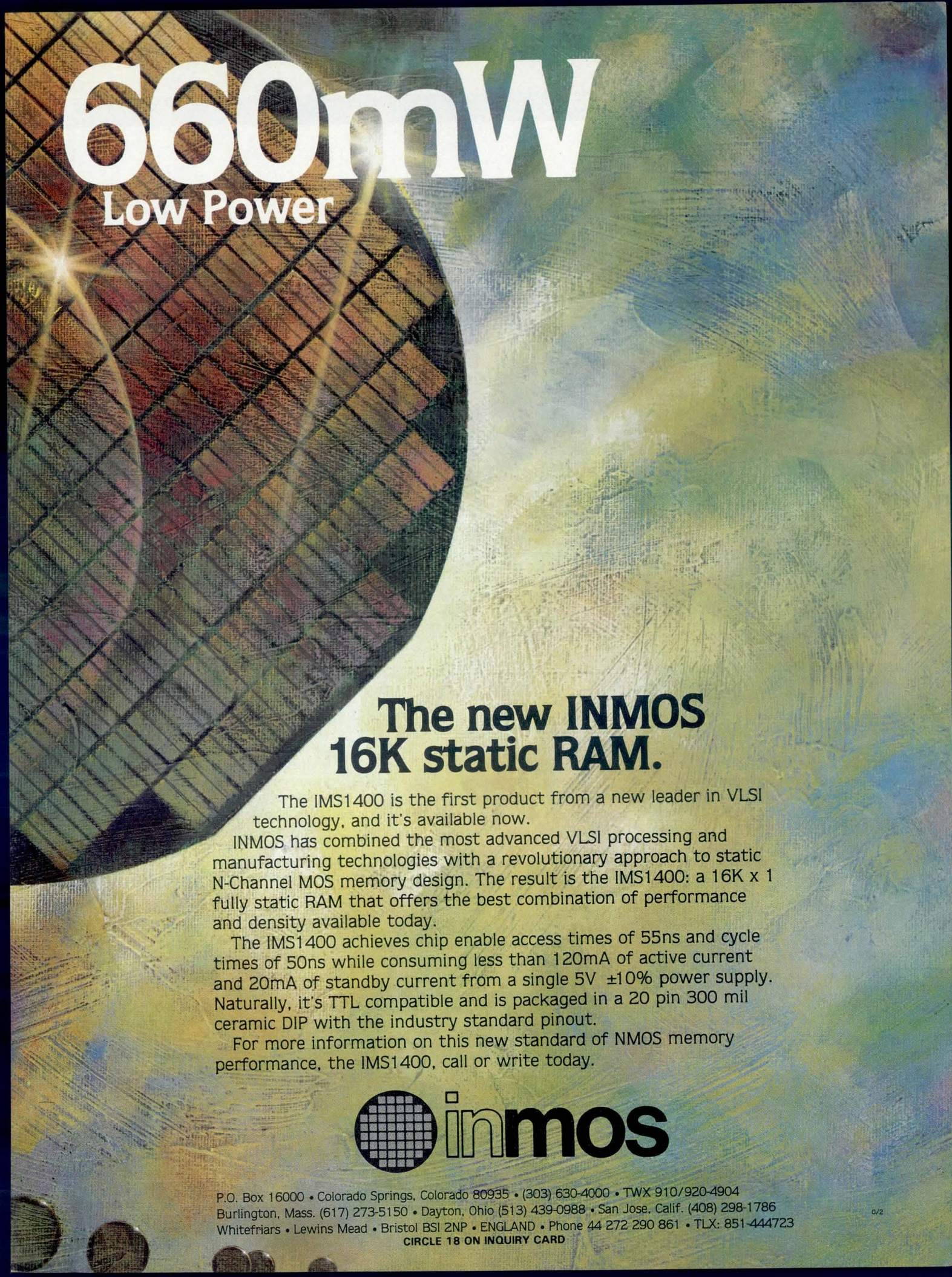

55ns
High Speed



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CIRCLE 18 ON INQUIRY CARD

Software Package Couples SNA with Public Packet-Switched Networks

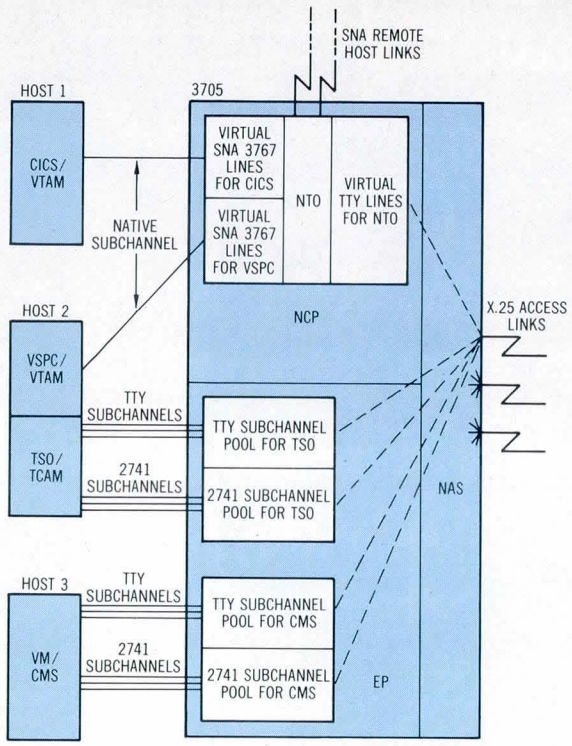
A network control program/emulator program (NCP/EP) path switch has been introduced for its X.25 Network Access Software (NAS) by Comm-Pro Associates, 638 14th St, Suite 700, Manhattan Beach, CA 90266. The original version of NAS enabled interactive asynchronous terminals (ITI) connected via a packet-switched network to selectively access multiple-host applications only through IBM's 3705 emulator program.

The new package allows use of the cost effectiveness of X.25 facilities and also of the benefits of the functionally superior IBM SNA program products. It allows ITI terminals to selectively access host applications through the NCP or EP portions of the partitioned emulator program (PEP) system. The package supports up to four channel-attached hosts and the applications can be running in the same or in different hosts. (See the Figure.) The NCP network terminal option (NTO) reroutes ITI connections into a multidomain SNA network for access to an additional number of remote hosts. From the host application viewpoint there is no difference between directly connected terminals and those communicating via an X.25 network. An optional X.25 callout facility uses standard DIAL channel control words (CCWs) with X.25 network addresses, replacing telephone dialing digits.

The NAS package supports Bell Canada's Datapac 3303 end to end protocol for real 3270 devices, which requires that network nodes act as remote hosts for the 3270s. The nodes handle device polling and selection, and NAS takes care of host poll and select channel programs. Only data packets pass between the nodes and the 3705. NAS provides true system select capability for network 3270s.

NAS operates as an extension of the company's network facilities package (NFP) on which it relies for management of its application interfaces. It will operate in an NCP5 or NCP7 PEP environment with type 1 or 4 channel adapters. X.25 access lines can be configured on type 2 or 3 communications scanners using either HDLC or Bisync framing. The basic NAS package requires 26k bytes min of 3705 storage in addition to the EP or PEP. The package is available for a free trial.

Circle 321 on Inquiry Card



NAS SNA/X.25 bridge. Low speed ITI traffic is multiplexed across X.25 access links. Network recognizes terminal type and speed and passes this information to NAS for proper session establishment. Application switching occurs at call connect time based on system select characters entered by terminal operator. Network terminal option (NTO) TTY/SNA conversion provides access to SNA networks

Data Communication System Designed for Distributed Data Networks

An addition to the family of modular communication processors from Microform Data Systems, Inc, 830 Maude Ave, Mountain View, CA 94043, ICOT 254 is a 2-way data communications system designed for application in existing or planned distributed data networks. It can be configured for line concentration, multiplexing, protocol/code conversion, and intranetwork message routing. The processor can operate as a satellite to the host in batch or interactive mode, as part of a network of interconnected processors, or as a standalone system.

Up to eight full-duplex asynchronous lines with up to 9600-baud aggregate speed, or up to four full-duplex 9600-baud synchronous lines can be accommodated. The processor, operating over common carrier or customer-owned lines, can also handle combinations of asynchronous and synchronous lines.

Used as a line concentrator, the processor allows any line to handle batch and interactive terminals; both synchronous and asynchronous lines can be multidropped. For the latter circuits, the processor handles polling of downline terminals based on poll addresses that are typically downline loaded from the host. In multiplexing operations the unit can eliminate the need for a multiplexer located at the host site, effectively halving the number of multiplexers required in conventional approaches.

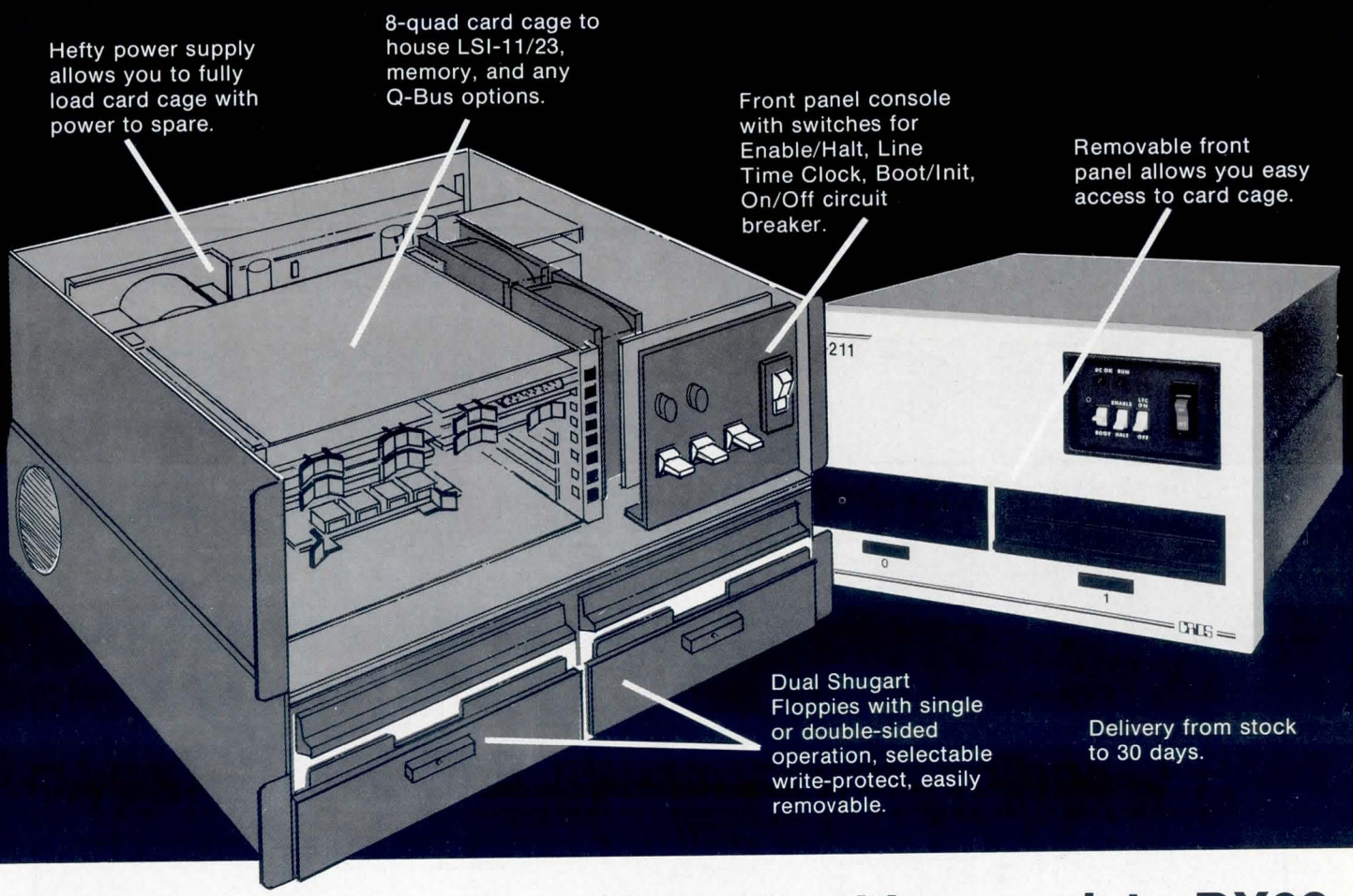
The processor supports standard protocols such as Teletype 33/35/37, Bisync, PARS, P1024, SNA/SDLC, Uniscope, and X.25/HDLC. Custom protocols can be accommodated on request. The processor can route messages to different hosts, to other terminals attached to it, or to another network processor.

The system uses a multiple-microcomputer architecture. There is a separate computer, line interface, and memory space for each synchronous circuit, while a single computer is shared by two asynchronous circuits. A system RAM is accessed by each microcomputer through the ICOBUS™, which handles interconnection, scheduling, and data transfer between microcomputers.

Circle 322 on Inquiry Card

Charles River Data Systems MF-211 System

an open and closed case for the **LSI-11/23** and **RX02** Floppy Disc System



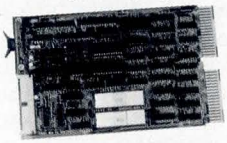
CRDS delivers your LSI-11/23 with complete RX02 software/media compatibility while costing less!

Economical in cost and space

Your MF-211 system combines DEC's LSI-11/23 with dual Shugart SA800 Floppies and an 8-quad slot backplane, all within an attractive 10½" rack mountable enclosure. Our dual height floppy Controller/Interface allows you complete software/media interchangeability with DEC's RX02 Floppy system. All DEC interface cards and software products are available for your use from CRDS. Join over 1,000 users with a new MF-211, the perfect answer to your Micro/Floppy requirement—in half the space . . . and up to 30% savings.

Immediate Problem Detection

A 90-day warranty comes with your MF-211. In addition, a detailed system diagnostic diskette is provided with each system to assure you of proper system operation and to allow for immediate detection and isolation of system failure. In the event of malfunction, the defective sub-module is normally found within minutes. After verification with the CRDS Maintenance Department, a replacement for your defective module will be promptly forwarded.



Unique Controller Card

- □ **RX02 software/media interchangeability**
- □ **IBM 3740 Formatter**
- □ **Built-in self diagnostic**
- □ **Bootstrap loader**
- □ **Single and double density operation**
- □ **DMA Data transfer**

Double-Sided Option

If double-sided floppy capability is desired, simply ask for the MF-411. This system uses the Shugart SA850 double-sided drives and provides two megabytes of total storage. A diskette with a modified RT-11 double-sided floppy handler is provided with each system, assuring you of software compatibility for both single and double-sided media operation.

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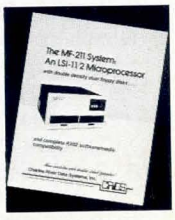

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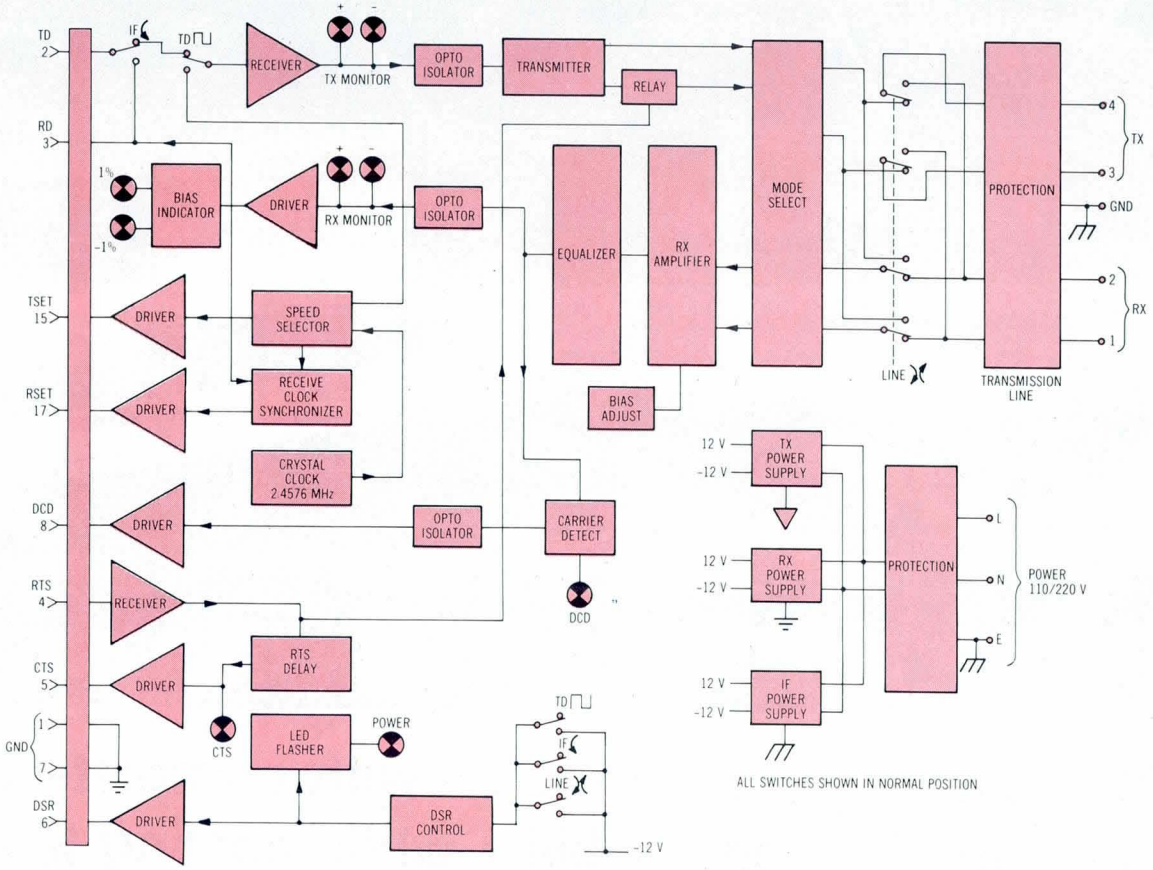
CIRCLE 20 ON INQUIRY CARD

Data Transceivers Withstand Adverse Environmental Conditions



DT19.2L data transceiver block diagram. Built-in MODEMGUARD® provides fail-safe protection to all inputs and outputs including line, ac power, and interface. In DT19.2S version (not shown) phone line inputs can withstand 250-V ac power if lines are accidentally transposed. Both models are compatible and can be mixed on multipoint lines

Short haul baseband modems DT19.2 are intended for serial binary communications between computers and remote terminals in demanding conditions such as are encountered with substandard telephone lines, high incidence of lightning, corrosive atmospheres, and rough handling. Model DT19.2S, for applications requiring less protection, can withstand 250 Vrms overvoltage indefinitely and has a range of 12 mi (19 km) at 9600 bits/s. Model DT19.2L is said to be completely immune to external overvoltages and lightning surges up to 20k A and has a range of 20 mi (32 km) at 9600 bits/s.

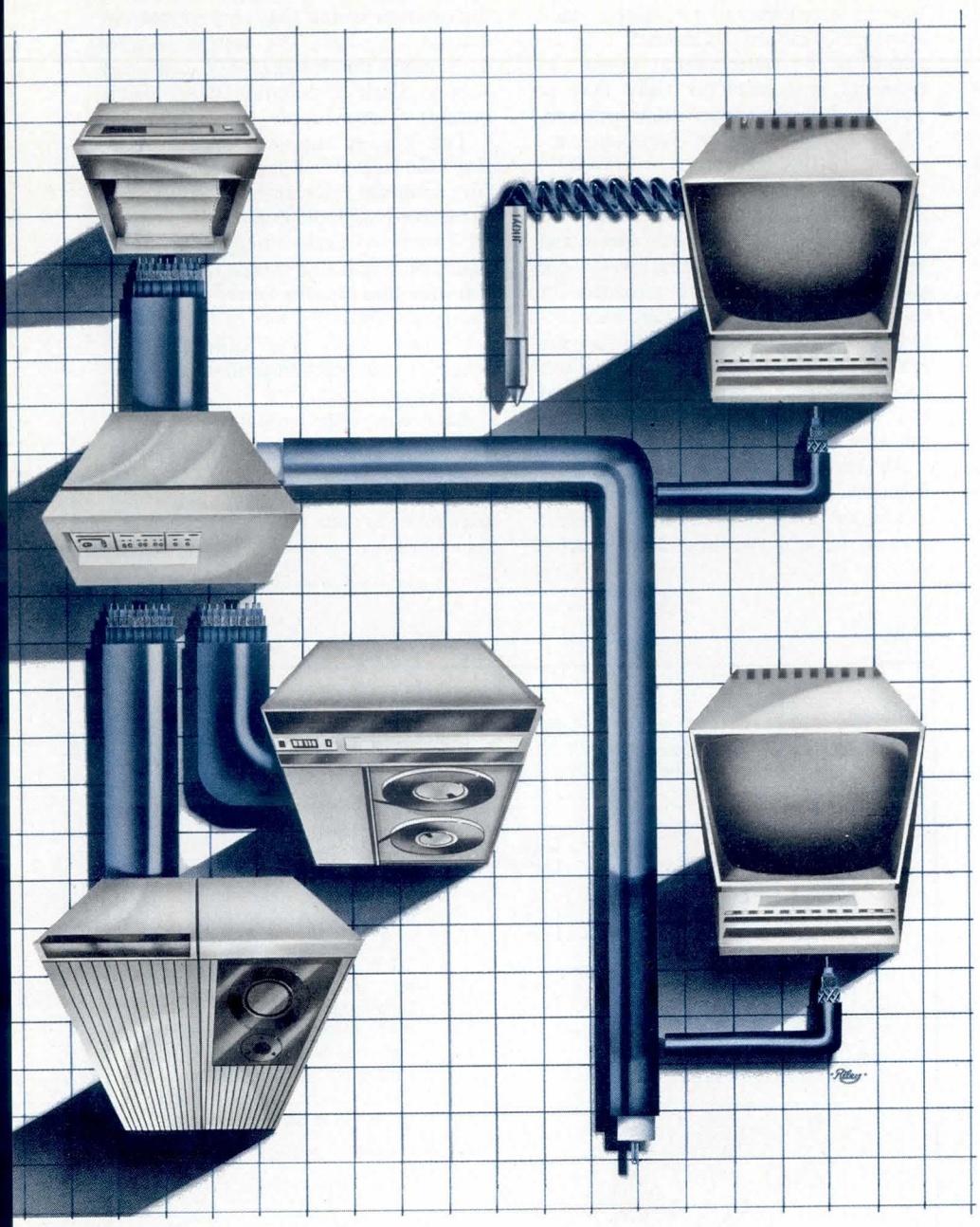
The data transceivers, from Kapusi Laboratories, 2121 S El Camino Real, San Mateo, CA 94403, operate both synchronously and asynchronously over dc-coupled voice grade twisted pairs or metallic private lines and are suitable for 2- or 4-wire point to point or multipoint applications at selectable rates to 19,200 bits/s. The devices meet AT&T Publication 43401 requirements and interface with CCITT V.24, V.28, and EIA RS-232-C circuits. A fast sync circuit allows 5-ms turnaround delay in switched carrier mode.

Modulation is baseband, bipolar, NRZ, and data format is unrestricted, code independent, and code transparent. Bit rates in synchronous mode are 2400, 4800, 9600, and 19,200 bits/s; in asynchronous operation, speed is transparent from 0 to 19,200 bits/s. Maximum distance reached is 10 mi (16 km) at 19,200 bits/s and 40 mi (64 km) at 2400 bits/s over unloaded 19 AWG lines. Error rates are similar to those of conventional long range modems.

Standalone unit dimensions are 1.6 x 8.2 x 15.94″ (41 x 208 x 405 mm), and weight is 8 lb (3.6 kg). Using available rack adapter trays, 88 units can be fitted into a 6-ft (183-cm) rack.

Circle 323 on Inquiry Card

TODAY'S EDP SYSTEMS ARE RUNNING ON TIMES.



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CIRCLE 21 ON INQUIRY CARD

Multiplexer System Improves Communications Performance Of PDP-11 and VAX-11 Computers

The CSII/H multiplexer system can connect up to 64 asynchronous communications line devices to a single-controller board housed in the backplane of any PDP-11 or VAX-11 computer. The system, from Emulex Corp, 2001 E Deere Ave, Santa Ana, CA 92705, is comprised of a single, hex-sized circuit board for the communications controller, connected by a 34-conductor ribbon cable to up to four distribution panels, and either one or two 8-channel line adapters.

The line adapters contain the data and modem interface circuitry, as well as UART-type circuits that provide serial to parallel and parallel to serial conversion for parallel data transfer between adapters and controller. The UARTs also contain a baud rate generator.

Line adapters may be initially configured for either RS-232 or current loop interface standards. Channels may be added in 8- rather than 16-line increments, and interface types may be changed, mixed or matched as required. All the line interface variations are located outside the CPU.

The system offers all such DEC DH11 features as DMA output transmission, FIFO input, and line interface, speed, and format selection. Individual byte count and address registers are provided for each line for DMA or characters transmitted from CPU memory. Firmware P/ROMs directly emulate DH11 functions for transparent execution of standard DEC diagnostics and operating system software.

All basic communications controller functions are on one board that plugs into a single UNIBUS™ SPC slot as one unit load on the bus. The single 34-conductor ribbon cable daisy chains up to four distribution panels that contain the line adapter circuitry. The system requires 4 A from the internal 5-V computer supply. Each distribution panel incorporates its own supply.

The system supports asynchronous line interfaces of all types and provides for program selection of such line parameters as individual line speeds of all commonly used rates up to 19.2k baud, plus split line speeds for different transmit and receive rates; 5- to 8-bit character size; stop bits of 1-, 1.5-, or 2-bit size, half- and full-duplex or echoplex transmission modes; and odd, even, or no parity.

Each controller emulates up to four 16-line DH11s in increments of eight lines to a maximum of 64. Operating mode and firmware enhancements are switch-selectable for each 8-line group.

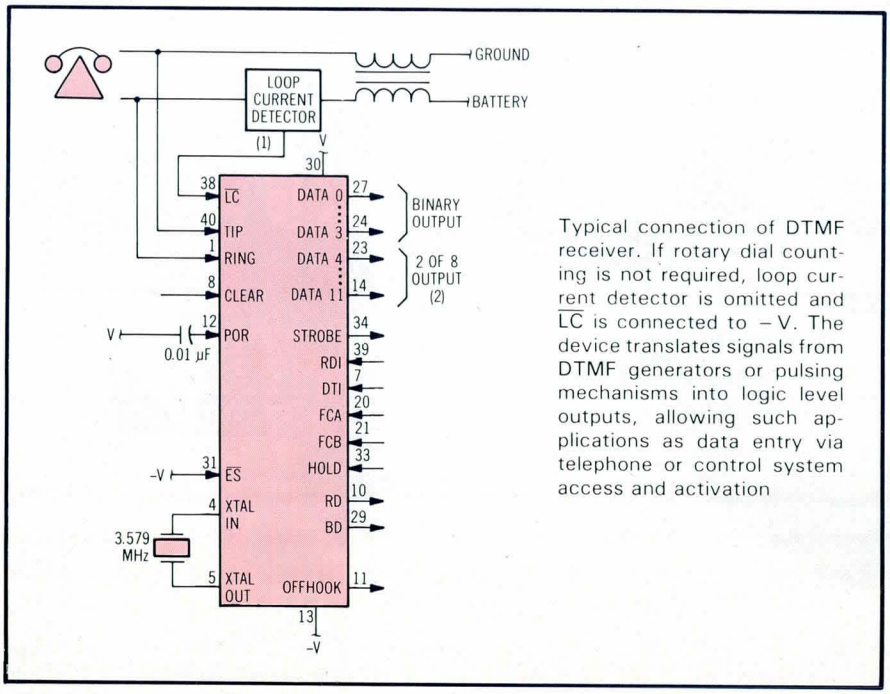
Circle 324 on Inquiry Card

DTMF Receiver Interfaces Touch-Tone® Phones to Data Processing Equipment

Hybrid M-927 dual-tone multifrequency (DTMF) receiver and/or rotary dial pulse counter accepts all 16 DTMF or touchtone digits plus rotary dial pulses from telephone, radio, or other sources. Logic output can drive a transistor, low power Schottky TTL, MOS, or CMOS device. It can operate a digital display when coupled with a CMOS driver.

The receiver is available from Teltone Corp, 10801-120th Ave NE, Kirkland, WA 98033. Typical data entry applications include remote computer and peripheral system interface, consumer credit and shopping systems, and telephone banking, credit, and bill-paying systems.

Housed in a 40-pin DIP, the receiver contains a proprietary LSI device, dial tone and bandsplit filters, and clock circuits. It requires no external components except a 3.579-MHz TV color burst crystal and a single 12-Vdc power source to become a complete decoder circuit. Pin-selectable logic outputs include binary, 2 of 8 (2 of 7), 1 of 12, or blank. The device accepts differential or single-ended inputs with no additional components, and has three different chip enable/disable inputs. Stable free-running clock outputs of 447 kHz, 881 Hz, and 20 Hz are provided. The receiver is designed to CEPT, CCITT, and USITA recommended specifications, and is typically connected in parallel with tip and ring of the voice pair of a telephone line. (See the Figure.)



Typical connection of DTMF receiver. If rotary dial counting is not required, loop current detector is omitted and $\overline{LC}$ is connected to −V. The device translates signals from DTMF generators or pulsing mechanisms into logic level outputs, allowing such applications as data entry via telephone or control system access and activation

Circle 325 on Inquiry Card

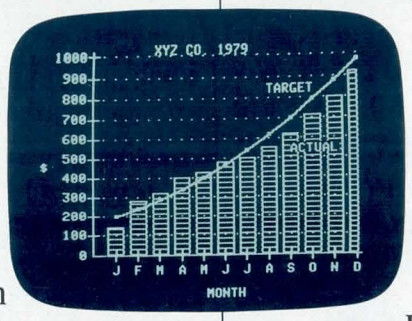
Three good reasons why professionals pick Apples.

1 In research

Apple personal computer systems help you collect, store and analyze data as fast as you can load a disk and execute a program. Because more than 100 companies offer software for Apple, you have the largest program library for manipulating your data in the personal computing world. Need special programs? Use any of Apple's development languages — BASIC, FORTRAN, Pascal.

2 In engineering

Apple personal computer systems let you define models, make trade-offs and refine prototypes. Want to study cause and effect of several variables? Apple computes new results instantly and displays them in colorful, easy-to-read graphs, charts or plots on a video monitor.



3 In production management

Apple personal computer systems make it easy to gather data, analyze productivity, measure yields and facilitate all phases of production control. Want to speed up repetitive tasks?

Rely on Apple's word processing capabilities to write, edit and print your reports.

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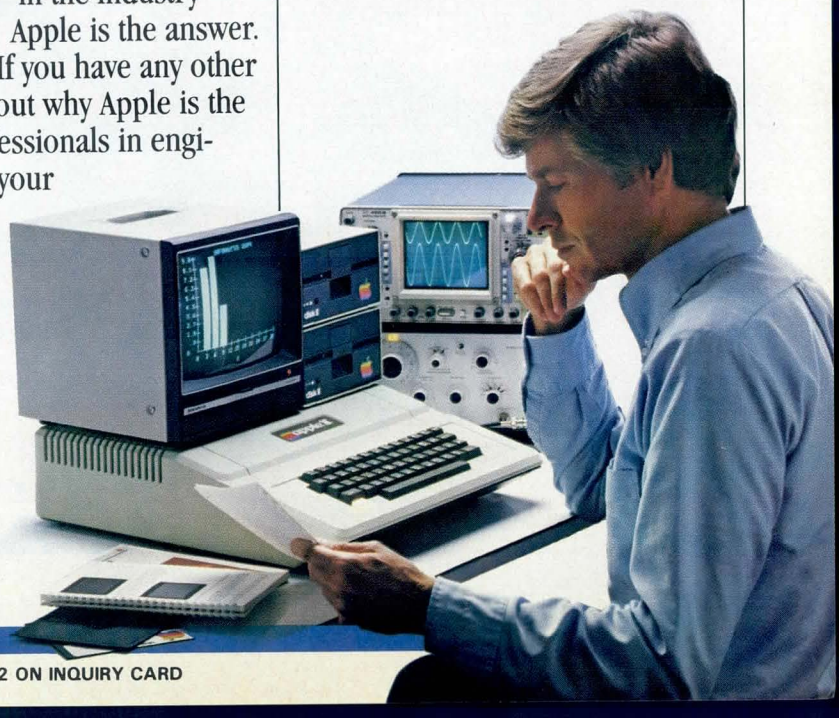
If you have any other questions about why Apple is the pick for professionals in engineering, see your nearest Apple computer dealer or call **800-538-9696**. In California, **800-662-9238**. Or write: Apple Computer, 10260 Bandley Drive, Cupertino, CA 95014.

	Apple II	Apple III
Maximum Memory Size	64K bytes	128K bytes
Screen Display	40 column (80 column with peripheral card) 24 Lines Upper Case	80 column 24 Lines Upper Case/Lower Case
Screen Resolution (B&W)	280 x 192	560 x 192
Screen Resolution (Color)	140 x 192 (6 colors)	280 x 192 (16 colors)
Keyboard	Fixed	Programmable
Numeric Key Pad	Accessory	Built-in
Input/Output	8 expansion slots	4 expansion slots plus built-in: disk interface RS-232 interface Silentype™ printer interface clock/calendar
Disk Drives	Add-on one to six drives	One drive built-in, plus interface to support three more drives
Languages	BASIC Fortran 77 Pascal Assembly Pilot	Enhanced BASIC Fortran 77 Pascal Assembly
Typical Configuration Pricing	CPU, 48K RAM, single disk drive, B&W Monitor (9"), Silentype™ printer, and BASIC. **$2875.00***	CPU, 96K RAM, integrated disk drive, B&W Monitor (12"), Silentype™ printer, SOS, Enhanced BASIC. **$4865.00***

* Suggested retail price.

apple computer inc.



CIRCLE 22 ON INQUIRY CARD

INTRODUCING THE $324* WE DO-IT-FOR-YOU WINCHESTER CONTROLLER.

Until now if you needed an inexpensive Winchester controller board, you were in big trouble.

They didn't exist.

Then we designed 5 chips that take the place of about 75 on an ST500/SA1000 interface. Which means it's now possible to fit a complete controller on one 6" x 9" board with about 40 chips instead of 150.

BIG ON RELIABILITY. Our WD1000 board gives you everything you need in a Winchester controller. Features like: a choice of 128, 256 or 512 byte buffers; a 5 MBITS/SEC transfer rate; control for up to 4 drives; control for up to 8 R/W heads and much more. All for about one-third the price of previously available controllers. The WD1000 is just $324 in quantities of 250.

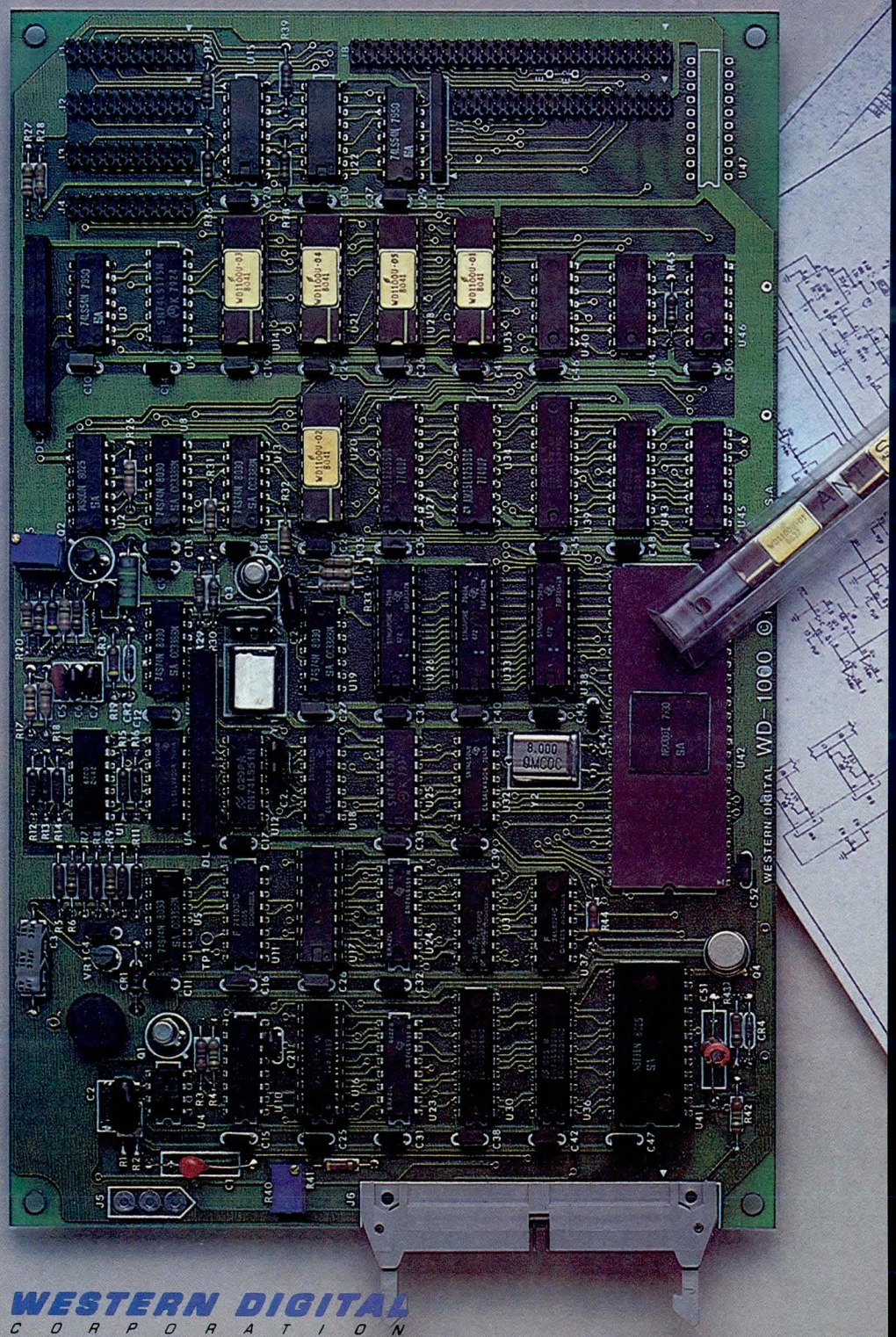
So suddenly you have greater design flexibility and the opportunity to create a system that's more reliable, less expensive and programs just like a floppy.

BIG JUMP ON THE MARKET. The WD1000 can save you up to 50% on your complete Winchester system and months of development time. Now's your chance to get a better product on the market, fast enough to make it very profitable.

For more information, including specifications on the WD1000 board, call (714) 557-3550 or mail in our coupon today.

With our boards, it won't be long before you're in the chips.

*Quantity 250.



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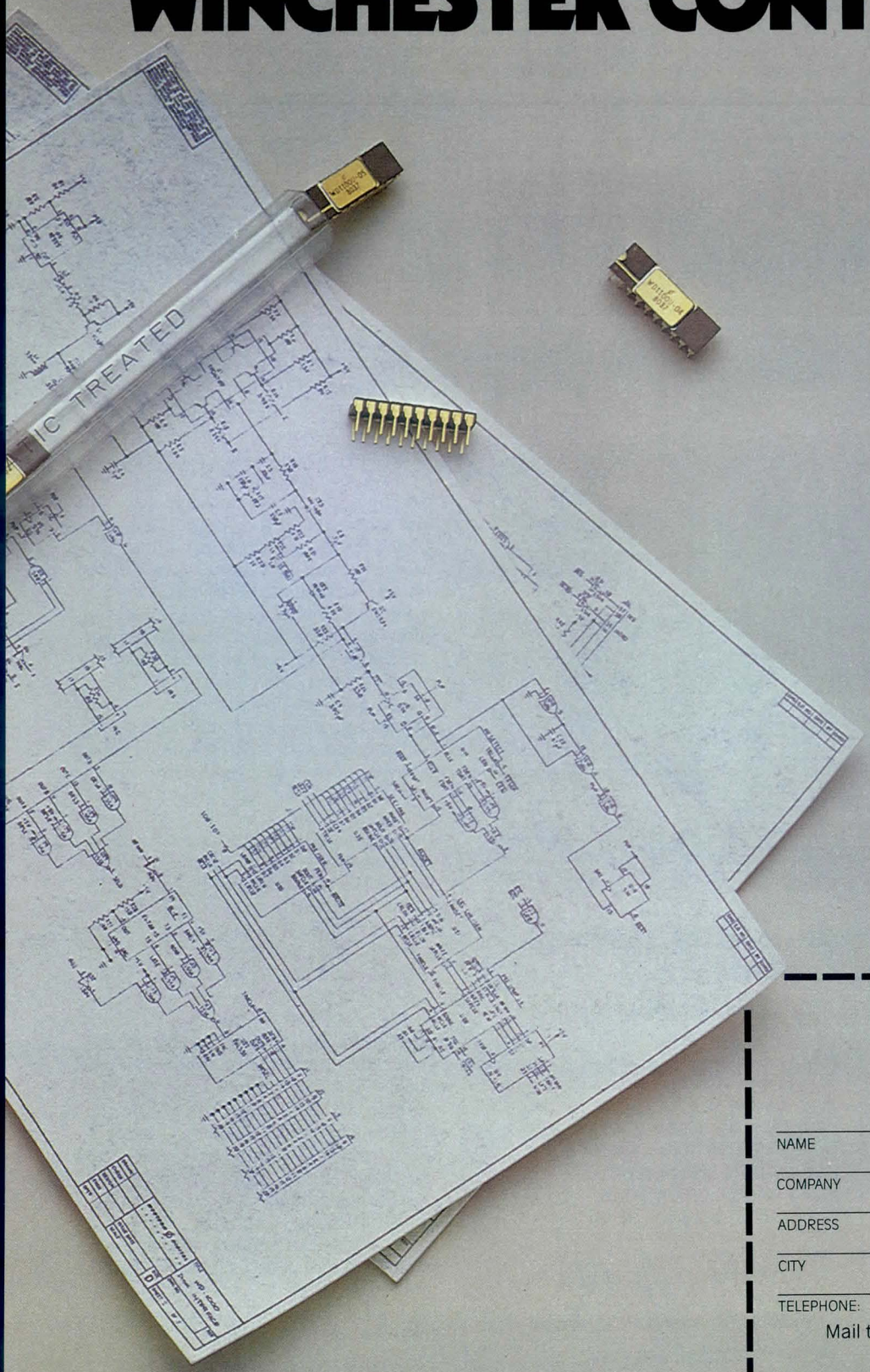
REGIONAL SALES OFFICES: Newport Beach, CA (714) 851-1221; Santa Clara, CA (408) 727-1777; Des Plaines, IL (312) 635-6090; Marblehead, MA (617) 631-6466; and Morden Surrey, U.K. 01-542-1036.

INTRODUCING THE $48* OEM DO-IT-YOURSELF WINCHESTER CONTROLLER.



Until now Winchester controllers had to be big, complex and very expensive.

SMALL WONDER. We've taken 75 discrete components from the usual Winchester controller and replaced them with 5 MSI chips (address mark detecter, CRC generator/checker, MFM generator, serial/parallel converter, parallel/serial converter) that can fit on a single board. And cost $48 per set.

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SMALL PACKAGE. An ST500/SA1000 interface for your system that's small, inexpensive, a lot less complicated and very reliable.

When you order the WD1100 5-chip set, we include complete instructions on how to design your controller board to make it work the way you want it too.

So not only will you save cold hard cash and months of development time, you'll be able to design a more compact, more reliable product. And get it into production while it's still new and exciting.

For more information, including specifications on the WD1100 chip set, call (714) 557-3550 or mail in our coupon today.

And it won't be long before you're in the chips.

Yes, I'm interested in saving money on my next Winchester controller.

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Newport Beach, CA 92663
Telephone: (714) 557-3550

CIRCLE 23 ON INQUIRY CARD

Data Communication Products Offered for Terminal and System to System Networks

Three data communication products for its HP 3000 series of computer systems have been announced by Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304. They are Interactive Mainframe Link/3000 (IML/3000), Multileaving Remote Job Entry/3000 (MRJE/3000), and Multipoint Terminal System/3000 (MTS/3000).

IML allows series 30, 33, and 44 systems of the computer family to communicate interactively with large mainframe systems by emulation of an IBM 3270 terminal, while MRJE emulates a remote HASP or JES2/3 multileaving batch workstation. The third product, MTS, allows multipoint terminal connections between an HP 3000 system and a mixture of HP terminals via a single communication line. All three products make use of the HP Intelligent Network Processor (INP) that offloads by as much as 50% the data communications overhead on the computer (*Computer Design*, Oct 1979, p 26).

IML network software product allows user application programs written in COBOL, COBOL II, BASIC, FORTRAN, or SPL to have online access to the IBM mainframe via a set of procedures available on the 3000 system. Data exchange with mainframe applications programs is provided by emulation of nearly all of the functions of Bisync versions of IBM 3271, 3274, and 3276 remote cluster control units, 3277/3278 display terminals, and 328X printers.

Inquiry and Development Facility (IDF), an available feature of IML, enables remote or local HP terminals to operate in "pass through" mode and communicate directly with the host. IDF also allows the host to use printers connected to the 3000 system without any user programming required. IML utilizes INP hardware and controller software as the network interface to the modem and communications link to the IBM system.

MRJE product performs the functions of a remote IBM HASP or JES2/3 multileaving batch workstation, so that HP 3000 users can send and receive jobs and data to and from IBM mainframe systems. MRJE also uses the INP to execute all of the multileaving Bisync line protocol on the controller, offloading these functions from the 3000 system. MRJE is supported at speeds of up to 9600 bits/s on switched or leased lines connected to IBM systems that execute ASP, HASP, JES2, or JES3 remote job entry software systems.

MTS/3000 software package adds to the capabilities of the 3000 systems by enabling, via the INP, multipoint communication between all models of the system and HP264X, 262X display stations and/or 307X data capture terminals over a single communication line at rates up to 9600 bits/s. INP, acting as a hardware/software "frontend processor" to the 3000, handles all multipoint Bisync protocol handling and handshaking, data buffering, CRC error checking, retransmission of spoiled data, and terminal polling. MTS supports remote multidrop terminal connections or inplant local connections up to 5 mi (8 km) from the computer.

Circle 326 on Inquiry Card

There are other vacuum column drives, but only Cipher's 900 Series gives you these exclusive features:

- ☐ quiet operation
- ☐ internal diagnostics
- ☐ low power usage
- ☐ no changing of 50/60Hz belts or pulleys

The 900 Series uses built-in Z-80 intelligence and far simpler mechanical design to provide total closed loop control for gentle tape handling. That means it uses 60 per cent less power and is so quiet you can even use it in office environments.

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Cipher is your source for all your tape drive needs. Call us at (714) 578-9100. Or write for our free product brochure— 10225 Willow Creek Road, San Diego, California 92131.

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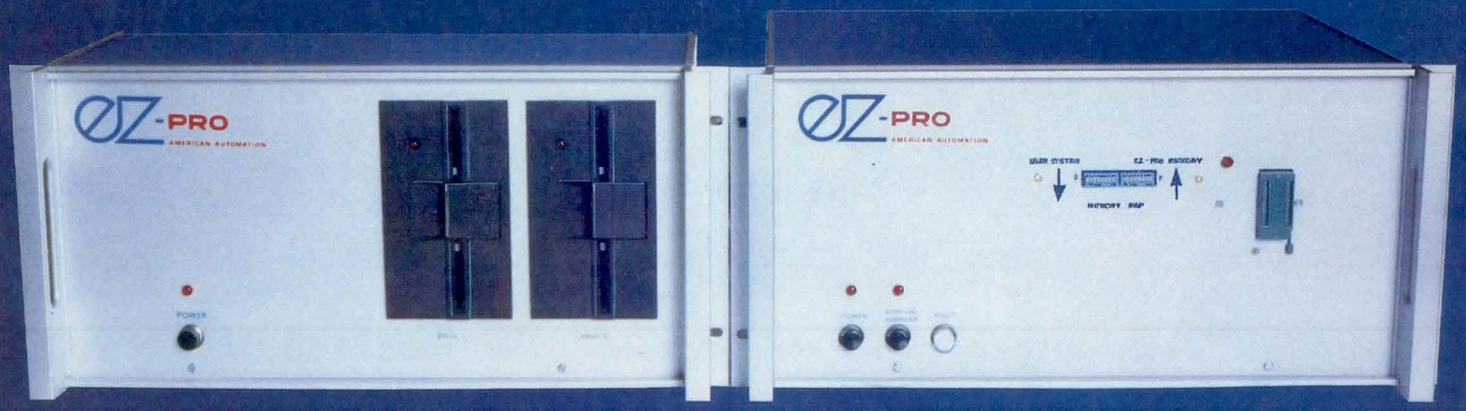
The EZ-PRO Development System



AA-591
Dual Disk

AA-570
Basic Development
Unit

AA-580 Interface Module equipped with eight AA-582 Memory Modules — used with bit slice systems.

THE EZ-PRO SYSTEM FEATURES:

Fixed Word Length Processors

- EZ-PRO supports a bunch and the bunch is getting bigger fast. Right now it's the Z80, 6800, 6802/8, 6805/146805, 6809, 6502/12, 6503-15 family, 3870/2/4/6, 8080, 8021, 8085, 8048 family. All are supported with real time in-circuit emulators.
- Emulators — Master/Slave type — Every resource in each slave is available to the user system including all interrupts and stack pointers.
- Trace and Logic Analyzer capabilities of course.
- EPROM Programmer, 2716 and 2732. Adaptor for 8748.
- Complete Software Support — Each emulator is provided with a Relocating Macroassembler, Linking Editor, Debugger and a DEMO program to show how the software is used. Higher level languages available include PASCAL and STRUBAL.

Bit Slice Processors

- EZ-PRO supports them all — You name it — 2, 4 or 8 bits wide — ECL or TTL.
- Microprogram word widths from 16 to 128 bits — Depths to 8K words.
- Bipolar PROM Programmers — ECL or TTL — 4 and 8 bit wide PROMs — intermixed if you like — Fast enough for production — Gang program 8 PROMS at a time with a single programmer.
- Complete Software Support — You'll have to experience it to believe the power and ease of use of AABASM, our Meta Assembler — And the rest of the software has the same standard of excellence.

The Basic EZ-PRO System

- 32 KB of static memory, expandable to 80 KB.
- Two RS-232 ports with selectable baud rates — one for a high speed printer and the other for a video terminal — Current loop port also provided.
- Choice of floppy disk capacities.
- Software provided for use on all systems includes a Resident Monitor, Disk Operating System, Disk Formatter and an Editor.

Prices

A complete EZ-PRO system equipped with one in-circuit emulator, dual disk unit, printer and video terminal sells for about $8,500. Bit Slice systems start at about $11,000.

What to do now that you're semi-sold . . .

Write or call us if you need more information. Then order a system at no risk. Advise us within 28 days of shipment from our plant that you don't want the system and return it to us in an undamaged condition within 35 days and we'll promptly return your money.

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TION FOR THE 8048.
TION FOR THE 6801.

Nobody builds a better emulator. Not Intel. Not Motorola. In fact, the μSE MicroSystem Emulator lets you run the Intel 8048 family at full 11MHz speed (something the Intel emulator doesn't). For the Motorola 6801/03, we give you an emulator that doesn't intrude on user space. It's transparent to the system under development. And here's the gotcha: One μSE supports both microcomputers.

One μSE. 15 μP's. With the MicroSystem Emulator, your mini-based computer becomes a universal 8-bit μP development system. For 15 microprocessors. Just change Millennium's inexpensive μP emulation modules and cross assemblers. And here's more good news, if your development system is no longer dedicated to a single μP, neither are you.

Real time. The MicroSystem Emulator emulates at the highest clock rate of the microprocessor. No artificial wait states. It's transparent to the system. That means more accurate debugging.

More productivity for your system. Use μSE's to add development stations to your mini. Develop hardware and software simultaneously. Then integrate. With the same system. Or, add μSE's to your dedicated microprocessor development system and turn it into an undedicated multi-user development network.

Now, price. Stand-alone or as part of your hardware/software development system, the MicroSystem Emulator is probably the best in-circuit emulator at any price. Yet, the base price is just $5,250. And individual emulation modules and cross-assemblers are available for 15 μP's and μC's. Starting at $1,375 for the module and $550 for the cross-assembler.

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BRIEFS

Recorder Provides Mass Storage for Data Link Analysis—Microprocessor based model 7000 Datatape enables nonvolatile mass storage for digital data associated with EIA RS-232-C and CCITT V.24 interfaces. Data can be recorded and rerun at any one of 16 data rates to facilitate analysis of data link problems. The device, from International Data Sciences, Inc, 7 Wellington Rd, Lincoln, RI 02865, records transmit data (TD), receive data (RD), and seven critical control signals. Operation is independent of code, line protocol, code level, and parity for both synchronous and asynchronous data links. Recorded data can consist of various combinations of TD, RD, and control signals to assist in fault isolation.

Circle 327 on Inquiry Card

Software Package Supports X.25 Standard—Designed in accordance with the CCITT X.25 packet-switching standard, MODCOMP/X.25 Network DTE/DCE product implements the three distinct and independent levels of the X.25 interface and is available from Modular Computer Systems, Inc, 1650 W McNab Rd, PO Box 6099, Ft Lauderdale, FL 33310. The package includes complete documentation and 6-mo warranty.

Circle 328 on Inquiry Card

Modem Transmits Synchronously Over ac Lines—Using carrier current techniques to transmit digital information over ac power lines, RAM-22 "wireless" synchronous short-haul modem operates at selectable speeds of 2400, 4800, and 9600 bits/s. A product of Data-Control Systems, Commerce Dr, Danbury, CT 06810, the unit accommodates up to 12 independent full-duplex channels using a building's ac wiring as the transmission medium. Each channel is separated in the frequency domain and can be used in point to point or multidrop mode. Standalone or rackmount versions are available.

Circle 329 on Inquiry Card

Analyzer Handles Byte-Oriented Protocols—Users of the Ei Model 120 data communications analyzer for byte-oriented protocols may view synchronous, asynchronous, or isochronous communications in ASCII, EBCDIC, hex pairs, EBCD, Baudot, IPARS, or other optional sets. The analyzer, from Epicom, Inc, 592 N Douglas Ave, Altamonte Springs, FL 32701, has a 5″ (13-cm) CRT display and can drive external displays. Refresh memory can call up as many as eight pages of data for detailed analysis. The analyzer can be programmed to stop for parity/framing errors, user selected detect character, or designated external events. Twelve standard rates from 50 to 9600 bits/s are available, as well as four selectable nonstandard rates.

Circle 330 on Inquiry Card □

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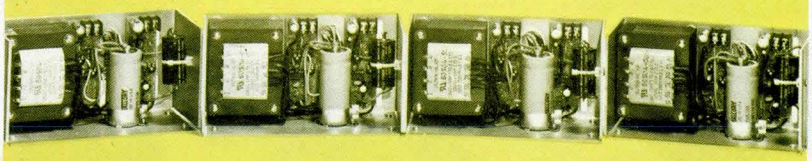

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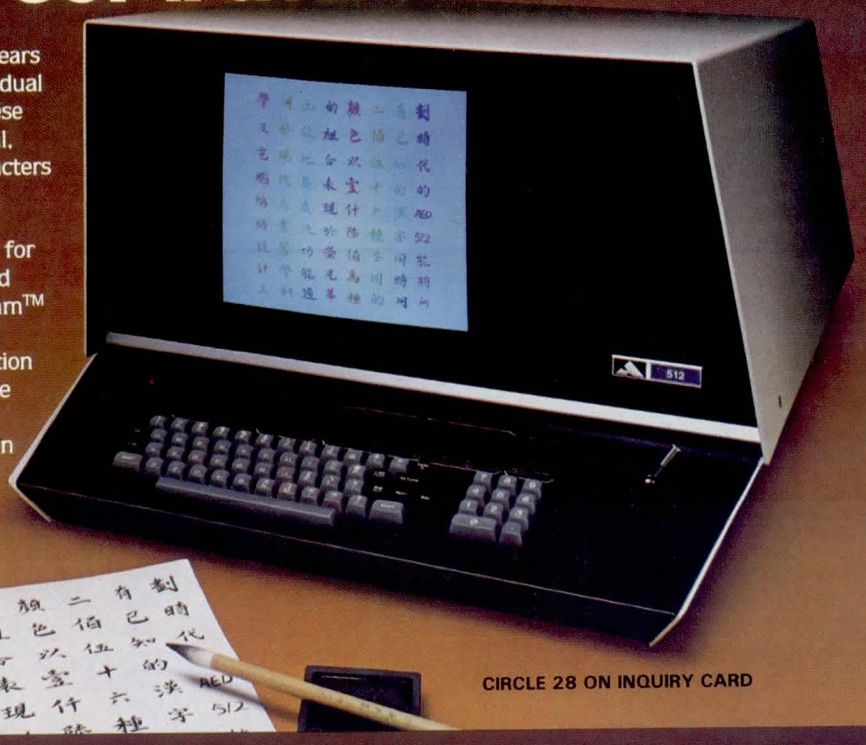

CIRCLE 28 ON INQUIRY CARD

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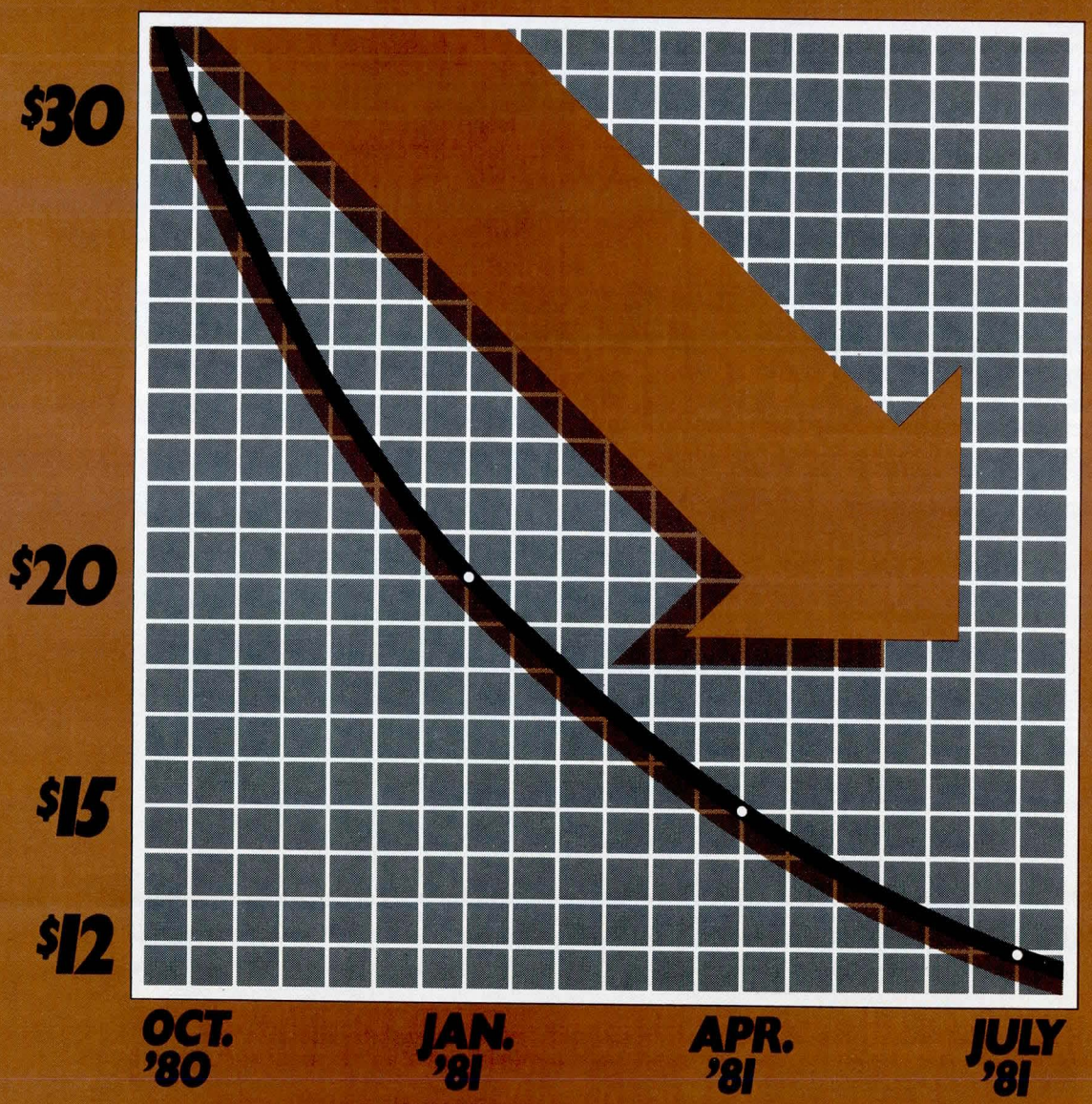
CIRCLE 174 ON INQUIRY CARD

4K CMOS GUARANTEED



Prices shown are for 100-piece quantities. Lower prices are applicable for volume requirements.

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It's an Intersil exclusive: the one and only 4K CMOS EPROM—the IM6653/54 (available in 1024 x 4 or 512 x 8).

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Guaranteed deliveries.

With capacities up and prices down, we're very well equipped to handle volume EPROM orders. And to back that up: Intersil hereby guarantees the on-time delivery of every factory-scheduled CMOS EPROM order placed in 1981.

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The IM6653/54 needs only 140μA in standby—guaranteed maximum. That's 20 to 100 times less current per bit than the popular NMOS EPROMs. Which means 20 to 100 times longer battery life in low-power applications. Which means lower system cost and less replacement inconvenience.

Get speed in the bargain.

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The advantages of CMOS.

Whether you're prototyping a system or in production, CMOS means energy savings, increased reliability and lower system cost. For harsh environments, it means a wider operating range—all the way up to full Mil on "M" versions. And a choice in single-supply operating voltage, anywhere from 5V to 10V.

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You can use our 6920 CMOS EPROM programmer. Or any of the other standard EPROM programmers. Either way, it's utterly simple.

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CD 3/81

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CIRCLE 29 ON INQUIRY CARD

8″ Winchester Drives Achieve 136M-Byte Capacity Using Digital Head Position Actuator

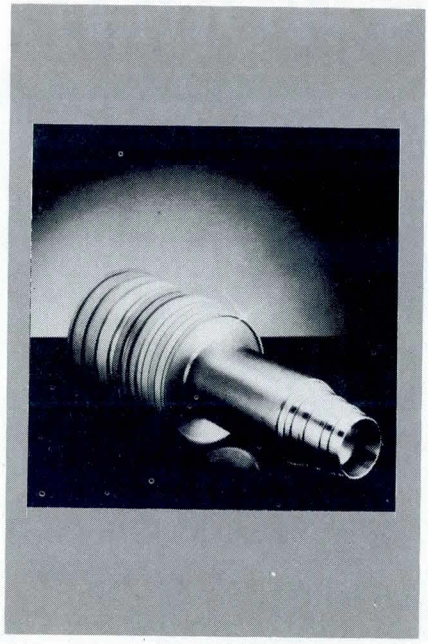
Three 8″ Winchester disc drive models use a unique digital head positioning device to provide capacity for up to 136M bytes on standard 210-mm media. The intelligent drives, developed by Ontrax Corp, 611 Vaqueros Ave, Sunnyvale, CA 94086, are small enough that two will fit side by side in a standard 19″ (48-cm) rack.

Each unit is composed of the disc drive itself and an integral power supply system. Native interface in basic drives is based on the proposed ANSI X3T9.3/143 Rev 5 standard. The associated formatter/controller is interconnected by a 50-wire ribbon cable for flexibility in configuration. All models use the same drive elements and circuit cards; they differ in number of plotters, heads, and positioners used to supply various capacities.

Units provide track density of 960 tracks/in (377.9/cm) using 600 cylinders. The drive spindle rotates at 4878 r/min to achieve a data rate of 9.2M bits/s and to attain an average rotational latency of 7.0 ms. Data are recorded at 7158 bits/in (2818/cm) in MFM.

Key to the large capacity and high throughput of the drives is the read/write head positioner, invented by Vice President Dieter Schulze, for which patents are now pending. Its actuator comprises a series of nine concentric elements that have a formed cup shape on one end and are graduated in size to accommodate the binary weighted seek distance for which each individual stage is responsible. Each element is made using powdered metal technology and has an embedded electromagnetic coil. Elements are nested in such a way that their cup elements make use of trapped air to provide cushioned damping upon completion of a seek.

Each element can travel a specific linear distance in either direction, and each can travel twice the distance of the previous element—thus the 9 allow the actuator to achieve 512 discrete physical locations equally spaced across the disc surface. Actuator elements are sprung so that in their natural state—that is, without the power on—the read/write heads are located at the outer edge of the 210-mm disc surface. When a track is selected for read/write operations, the intelligent unit selects the appropriate combination of actuator elements which will result in the proper distance of travel for the head. Current is applied to the coils embedded in the elements selected, and they are drawn together to cause the head travel.



Key to capacity of Ontrax's 8″ Winchester disc drive is read/write head actuator. Simpler in design and less expensive to manufacture, it is digital rather than analog, and far more accurate than conventional head positioners

When the head is located at the proper track, the current level used to "pick" the track is dropped to a "hold" level until the head must move again to another track. When no current is applied, the entire actuator moves back to its natural sprung state.

Since tolerances will vary, both from manufacturing techniques and from expansion errors caused by temperature or other operating conditions, an additive movement is provided by a squeeze coil. This device can move linearly over a limited range of a few mils to overcome these errors and cause the head to travel a few microinches for correction. The squeeze coil is simply a spring opposed by a coil to which a current can be applied so that each track location is spread equidistant from its neighbors.

Damping is provided between elements by controlling the size of the openings between elements. The air trapped between them acts as a natural "brake" to cushion the last part of the mechanical travel in either direction. This means the entire actuator is self-limiting and that no crash stops are required, as they are with conventional actuators.

Each formatter incorporates a 68000 microprocessor, a memory card containing data buffering and processor instructions, a storage port interface, and a communications port interface. Additional slots in the formatter backplane are available for connecting the drive system to a wide variety of user-specified interfaces, including SMD, RS-232, byte parallel, tape backup systems, and customer-developed interfaces.

The drives use a variation of an embedded servo technique to monitor the head position and verify its location. No servo surface is used, as is the case with conventional drives. Servo information is interspersed with data on each data track and is used simply to verify position, not control or maintain it.

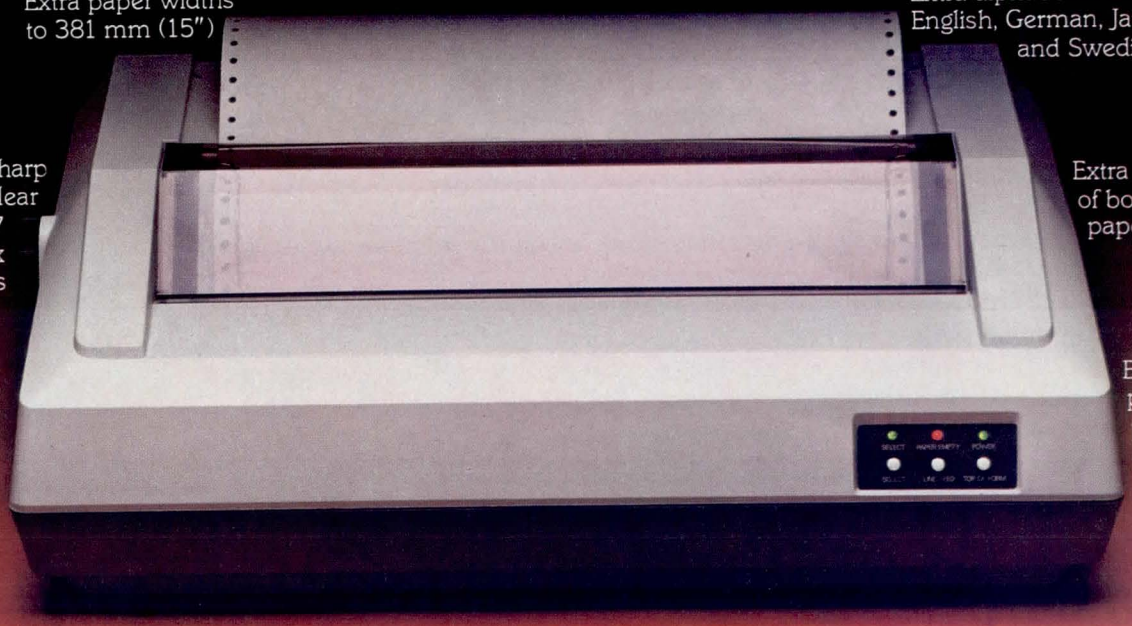
Since this is a linear positioning system, no radial to linear conversions are necessary. The positioner can rewrite its own servo data, if it is damaged or overwritten accidentally. Software in the formatter will recalibrate the drive and recertify all disc surfaces.

The drives also permit individual addressing of each positioner in dual positioner models. This means that a 136M-byte drive is addressable as two 68M-byte units. Providing a significant improvement in system throughput for tasks such as sort, merge, and copy.

Model 136 uses 2 positioners, 5 platters, and 16 read/write heads to achieve 136M-byte capacity in 9600 data tracks. The 68 uses 2 positioners, 3 platters, and 8 heads to provide 68M-bytes in 4800 tracks, and the 34 uses a single positioner, 2 platters, and 4 heads for 34M-byte capacity or 2400 tracks. In OEM quantities of 250 to 500 the 136 will sell for $4000 with ANSI interface and $5500 with formatter. Evaluation units will be shipped in April; full production is planned for June.

Circle 350 on Inquiry Card

EXTRA. EXTRA.



Now you get more extras when you pick the new dot matrix printers by C. Itoh. Choose the Comet 80-column printer and get the extra benefits of four character sizes and paper-saving print compression. Choose the Comet II 136-column printer and receive the added extra of a full-width computer size printer that accommodates paper widths to 381 mm (15").

Both the Comet and Comet II also offer the rare combination of low cost and high performance. Both models operate at an efficient 125 cps bidirectional print speed and in a 9 x 7 dot matrix.

C. Itoh's Comet series has the extra advantage of a unique multilingual capability with a selection of four different alphabets: English, German, Japanese and Swedish. Other special characteristics include a programmable VFU (Vertical Format Unit) plus self-test diagnostics. For your operator's convenience, there's easy bottom or back paper loading, and both Comets use a standard low-cost nylon ribbon. Plus our printers already meet 1981 Class A FCC, UL, and fire safety requirements.

If all that wasn't enough, Comet and Comet II are plug-compatible with all major printers in the industry, meeting standard parallel or serial interface specifications. Our printers are backed by C. Itoh's warranty and a nationwide field service organization.

And as a final, all important extra, when you choose either printer from C. Itoh you get immediate off-the-shelf delivery.

So if you want the highest quality at the best price, look into the extras the C. Itoh Comet and Comet II printers offer. You'll get a lot more than you bargained for. For more information, contact C. Itoh Electronics, Inc., 5301 Beethoven Street, Los Angeles, CA 90066; Tel. (213) 390-7778. Chicago Office: 240 E. Lake Street, Suite 301-A, Addison, IL 60101; Tel. (312) 941-1310. New York Office: 666 Third Ave., NY, NY 10017; Tel. (212) 682-0420. Dallas Office: 17060 Dallas Pkwy., No. 108, TX 75248; Tel. (214) 931-0177 C. Itoh represented in Canada by Canadian General Electric.

C. ITOH ELECTRONICS, INC.

One World of Quality

CIRCLE 30 ON INQUIRY CARD

CUSTOM MEMORY SYSTEMS

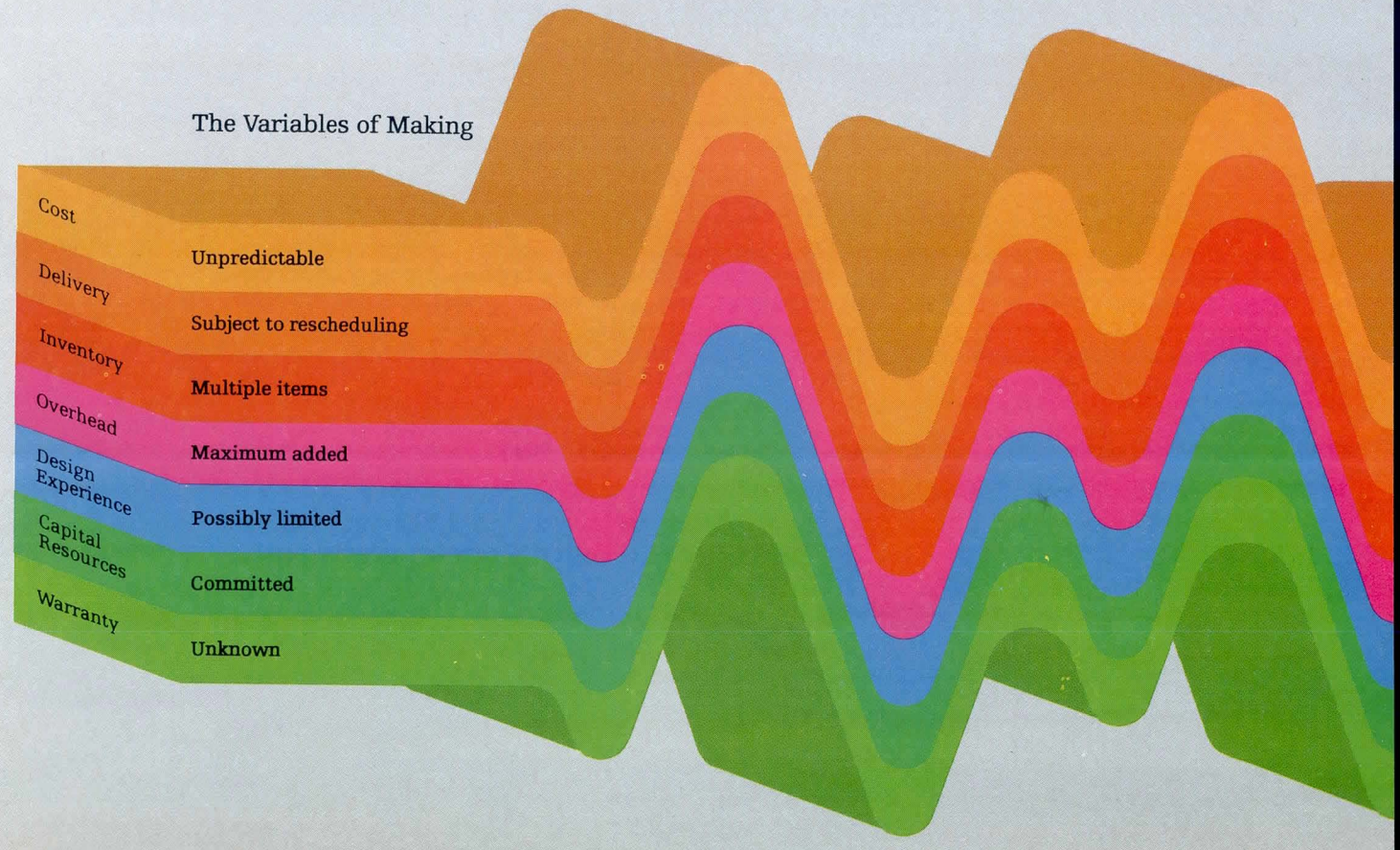
Make vs. buy. For a custom memory system, deciding between those alternatives is more accurately a question of could vs. can.

Granted, you have the engineering expertise. You could design and manufacture your own custom memory system. But if you did, there are some not-so-obvious variables that could get in the way. Variable lead times, for instance, from initial design to prototyping, as well as for test equipment and component delivery. And variable costs due to inflation, component market demand, additional personnel/physical plant overhead and others, equally interrelated. Offset those variables and you still incur the responsibility of a board-level warranty.

On the other hand, you can eliminate those variables with one purchase order to one vendor: Mostek. We already have experienced design and engineering talent, state-of-the-art testers, plus complete burn-in facilities. Consequently, we can quickly provide you with a fully tested, fully debugged and fully warranted custom memory system. One, we might add, that's every bit as specialized as the one you could make.

Consider our resources as proof of our capability: A memory systems engineering staff of 30 people, 14 of which are designers with a combined total of 90+ years of experience. Their output? Since 1977, more than 10,000 custom boards and systems shipped to customers all over the world. Yet even with that volume, we approach each project with a singular attention to detail.

From initial design through final testing, every Mostek memory system is "Mostek engineered." A product engineer, assigned to the product at its inception, remains with the system throughout its



Variables are why the smartest engineering decision you can make could be to buy.

MOSTEK®

development and product life cycle. To maintain product integrity, he continuously monitors the system at both the design and testing levels.

As for the components, they're exclusively Mostek memories; the same 100%-tested memories that have made us the recognized worldwide leader in dynamic RAM performance and volume production.

Now consider that your Mostek engineer is intimately familiar with Mostek memories. Consequently, he can help you take full advantage of the latest speed, power and density upgrades available. Including our new 5-volt only 16K and 64K dynamic RAMs. And our full offering of static memories.

But the advantages don't end there. Once designed, every system undergoes extensive testing and burn-in to insure that it meets or exceeds your operating requirements. The result is a highly reliable, fully warranted, high performance memory system from a proven single source.

Now, doesn't buying make a lot more sense than making? For more information, contact your nearest Mostek Sales Office.

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Central:
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Minnetonka, MN (612) 935-4020
Kettering, OH (513) 299-3405
Livonia, MI (313) 478-1470
Dallas, TX (214) 386-9141
Austin, TX (512) 458-5226
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The Certainties of Buying

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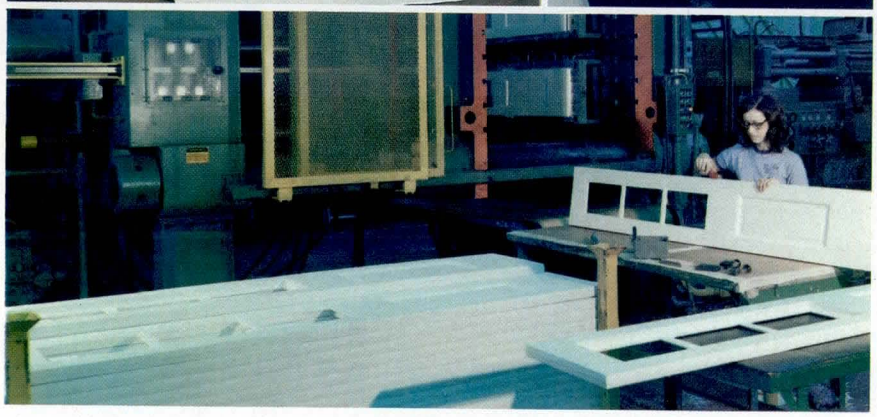
CIRCLE 31 ON INQUIRY CARD



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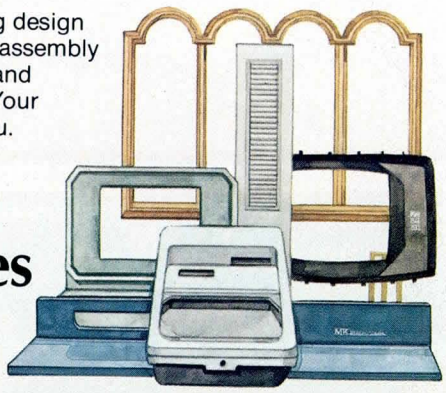

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CIRCLE 32 ON INQUIRY CARD

TECH REVIEW

Multiuser, Multitasking Supported by 16-Bit Small Business Systems

Providing up to 0.5M bytes of main memory, MICROSTAR™ II, a 16-bit business computer system supports database management and report generation, and can execute programs written in Business BASIC. Demonstrated by Micro V Corp, 17791 Sky Park Circle, Irvine, CA 92714, the unit runs multi-user, multitasking software.

Capable of handling four workstations in its basic configuration, the compact system offers up to 50M bytes of floppy or hard disc storage with tape backup available.

With capacity for storing 10M to 34M bytes on hard disc and 1.2M bytes on double-sided floppy disc, and providing 13M bytes of cartridge tape backup, the Series 3000 also offers 0.5M bytes of main memory and DMA channels for I/O. Five I/O ports are standard; up to 10 user stations can be supported.

The systems support both the STARDOS operating system and UPDATE™, a database management and report generating system. An optional conversion package allows execution of programs written in Business BASIC. Applications packages available for use on the systems include general accounting, word processing, distribution accounting, medical billing, service station accounting, and general contractor job costing.

Series 3000 will be available in the 2nd quarter of this year, with prices starting at $18,000. The MICROSTAR II is priced under $20,000.

Circle 351 on Inquiry Card

Conference to Focus on Productivity within Computer Industry

Compcon Fall '81 will provide a state of the art focus on productivity throughout the computer industry. Scheduled for Sept 14-17 at the Capital Hilton Hotel, Washington, DC, the conference is seeking papers covering the spectrum of productivity issues.

Prospective authors should send four copies of their papers to program chairman, Dr Raymond T. Yeh or Dr Victor R. Basili, University of Maryland, Dept of Computer Science, College Park, MD 20742. Deadline for submissions is April 1.

WHO COULD POSSIBLY MAKE A BETTER HIGH CAPACITY 5¼" FLOPPY THAN THE PEOPLE WHO INVENTED IT?

Who, indeed?

When we invented the high track density 5¼" floppy, we gave you all the capacity of larger 8" floppies in the process—96 or 100 tpi that yield up to 1.1 megabytes per drive. And we started a movement. Now, everyone is making the high capacity 5¼" drive.

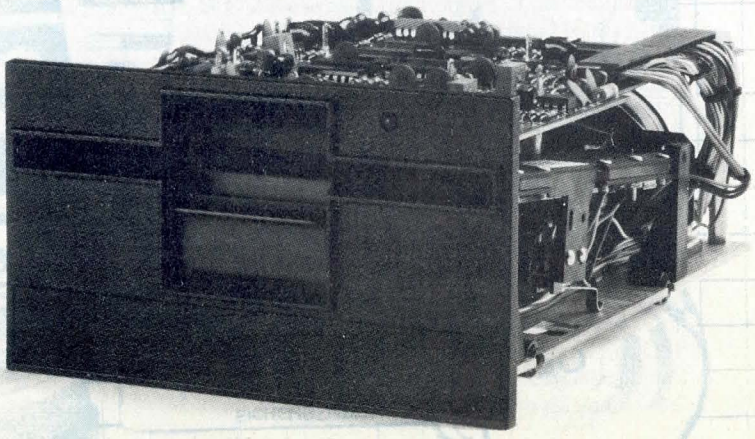
But they're just not the same as the original. Maybe that's because nobody knows as much about 5¼" floppies as we do. Or offers as much.

As a result, over 75% of the system manufacturers choose Micropolis. And over 95% of the double track density disk drives installed today are from Micropolis.

Our wide range of drives comes with a precision centering mechanism to insure accurate centering of a disk—every time (four times better than the competition). In addition, we include ceramic/ferrite double density recording heads, 10 msec track-to-track access time, stainless steel precision-ground positioning reference, and the highest quality electrical and mechanical components available. So you get high track storage capacity, fast access, lowest cost per K byte, significantly greater reliability and best of all, 3 years delivery experience of 85,000 high capacity drives.

	Maximum Capacity	# Delivered Through '79	Positioning Mechanism	Track Density	Av. Access Time (msec)
Shugart SA450	437.5K	<5,000	spiral cam	48	440
MPI B91	960K	Evaluation only	steel band and capstan	96/100	240
TEAC 50C	960K	<10,000 Mainly in Japan	steel lead screw	100	865
Micropolis 1016/1015	1,100K	60,000	steel lead screw	96/100	365

Our drive was designed from the ground up for its double density capacity, not merely redesigned from a single density unit. That's one reason we've shipped more high capacity 5¼" floppies by far than anyone else. Another is that no matter how many imitators there are, there's no substitute for the original.



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CIRCLE 33 ON INQUIRY CARD

THE EMM TOUGH

Mini's, Micro's, and

SECS 2

A militarized 16-bit minicomputer that's DEC PDP-11* software and I/O compatible.

SECS 2 is as rugged as a rhino.

It not only meets MIL-E-5400, 16400 and 4158, but has been FAA certified for avionic use as well. This powerful new minicomputer is fully compatible with DEC PDP-11 software. In fact, programs developed on commercial PDP-11's can be directly transferred to SECS 2.

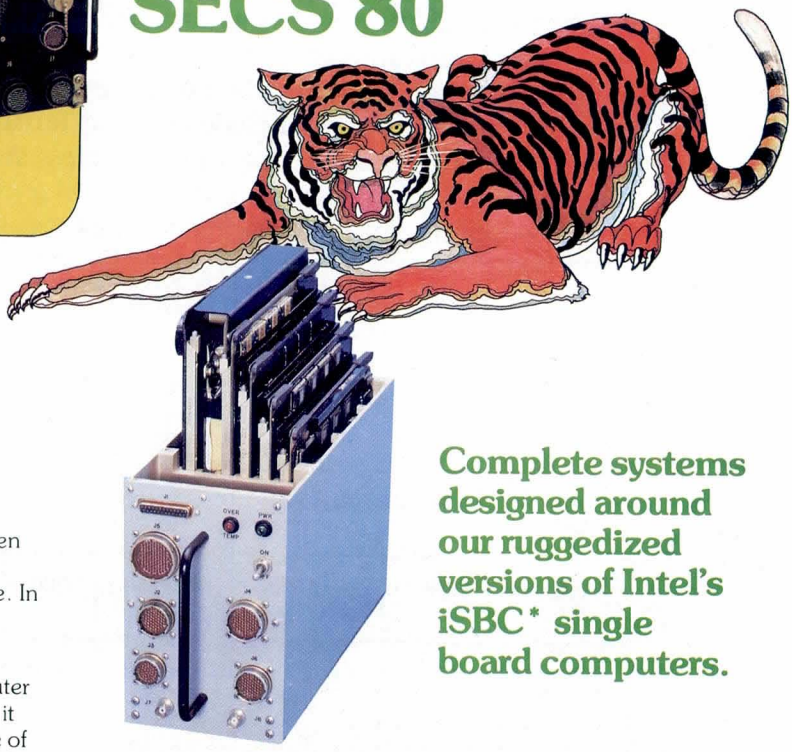
So there's no need for you to re-design a commercial computer to withstand severe environments when we've already done it for you. SECS 2 offers true system flexibility: a complete line of standard 6" by 9" support modules provide core, RAM, ROM, and EPROM memory, 1553B bus interface, power supplies, and more. Also, these individual modules are available for use in your own embedded systems.

Designed for airborne, shipboard, ground mobile and space applications, SECS 2 is the perfect minicomputer for tough military and commercial avionics requirements. Hundreds are currently in use as part of aviation fuel management systems, saving valuable fuel for commercial airlines throughout the world.

Packaged in a full-ATR chassis, 25 module slots are available; thus, a total system including CPU, power supply, memory and I/O can be accommodated in a single chassis while still allowing ample space for custom I/O, interfaces, etc. Another design advantage for you!

*Trademark of Digital Equipment Corporation

SECS 80



Complete systems designed around our ruggedized versions of Intel's iSBC* single board computers.

Like the mightly jungle cat, SECS 80 is tough, fast, and flexible.

By taking our ruggedized versions of Intel's 8-bit and 16-bit single board computers (which utilize 8080, 8085 and 8086 microprocessors) and surrounding them with our equally ruggedized support modules, you have all the building blocks you need to configure a microcomputer system that will operate in the most severe environments. And you can choose either a system that meets full MIL specs, or a lower cost industrial version that is perfect for applications involving oil exploration, construction, mining, transportation, etc.

A multitude of ATR packaged modules are available, including SBC's, RAM, ROM and EPROM memory, digital tape recorder and controller, 1553 serial I/O, digital input/output, analog to digital converter, high speed arithmetic unit, and power supplies.

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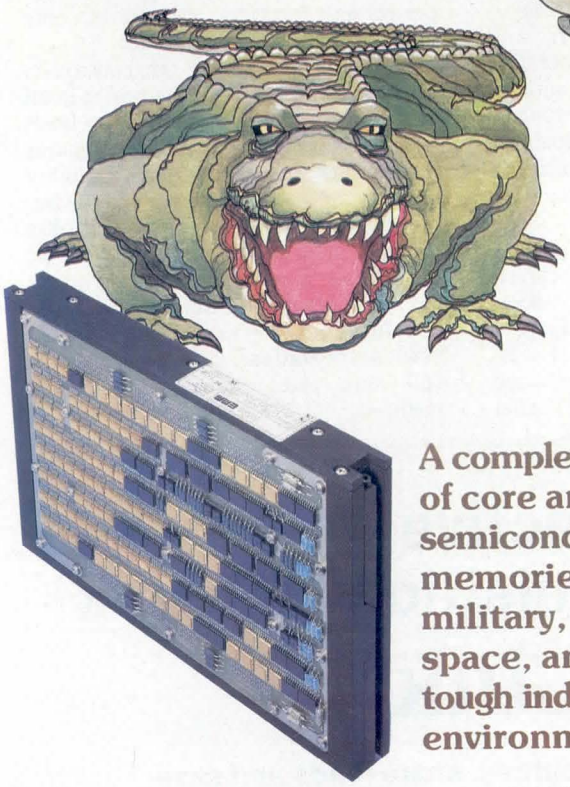
ONES ARE HERE

Memories. Too!

SEMS



A complete line of core and semiconductor memories for military, space, and tough industrial environments.

Our full line of memory systems, which meet MIL-E-5400, 16400, 4158 - and more, have the survival qualities of the alligator.

They've been fired into the sea, withstanding over 3,000 G's shock, and have survived. They've been blasted 80 miles into space and have continued to work.

Since 1961, SEMS memories have been part of major programs - Sea Sparrow, F-16, F-18, Pershing, AWACS, SR-71, Mirage and Harrier, just to name a few. On commercial jets, too - L1011, DC10, 727.

We have core and semiconductor memories. With wide variations in weight, capacity, cycle and access time. In full and ½-ATR packages.

SETS-1

A 23-megabit digital tape system for airborne and other severe environments.

Not only is SETS-1 at home in the air like the soaring eagle, it's also built for severe ground environments.

Meeting MIL-E-16400, 5400 and 4158, this compact recorder has a removable, hermetically sealed tape module which stores 23 megabits of data at 1600 bpi on 300 feet of ¼ inch magnetic tape. It also has bidirectional read/write capability on 4 tracks with a 192 K bps transfer rate.

At last, a recorder that's perfect for bulk data storage and data gathering from vehicles and remote sites. Or, as a data entry device for mission loaders and fire control systems.

Other EMM Products

We also have a complete line of commercial memories, both core and semiconductor, magnetic core storage stacks, mass memories, automatic test systems, and severe environment power supplies.

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COMPUTER PRODUCTS FOR SEVERE ENVIRONMENTS

CIRCLE 34 ON INQUIRY CARD

Magnetic Tape Interfaces, Disc Controllers Support DEC/DG Systems

Implemented on single boards to conserve space, reduce component count, and operate with reduced power requirements, 0.5″ (1.27-cm) magnetic tape interfaces and microprogrammed disc controllers emulate Data General and DEC tape units and DEC disc subsystems, respectively. Introduced by Datum Inc, 1363 S State College Blvd, Anaheim, CA 92806, they emulate standard subsystems and execute operating system and diagnostic software without modification.

High performance magnetic tape interface model 3512 operates with any formatted industry standard tape transport, supporting Data General Nova and Eclipse computers emulating TM11/TU10 tape systems. Any four 9-track drive operating at densities of 800/1600 bits/in (314/629/cm), speeds to 125 in (317 cm)/s, and at cable distances of 25 ft (7.6 m) may be incorporated. Data may be packed in DEC or IBM format. Users may edit previously recorded records.

Designed for large disc storage requirements of PDP-11 computers, the basic 6520 family consists of three different models, each designed to exactly emulate all existing models of large disc storage subsystems made by DEC. The 6520/A controller emulates DEC RP11/RP02/RP03 subsystems; the 6520/B emulates RH11/RM02/RP04/RP05/RP06 subsystems; and the 6510/C emulates RK611/RK06/RK07 subsystems. All models offer identical performance characteristics to the DEC controllers and therefore will execute all DEC operating systems and diagnostic software without any modification. Each controller incorporates an automatic self-test capability plus extensive subsystem diagnostics in onboard firmware; special operating functions can often be added to further enhance system performance.

Advanced microprocessor architecture of the controller family incorporates high speed bipolar technology to meet the performance demands of present and anticipated storage module and Winchester disc control/data transfer rates as well as to provide complete application flexibility.

The units use standard SMD interfacing. Any four industry-compatible drives may be integrated into a single subsystem, all operating at serial data rates up to 10 MHz. Fully buffered disc I/O circuitry permits operation at radial cable distances of 50′ (15.2 m) and daisy chain cable distances of 100′ (30.5 m). The controllers offer standard Unibus interfacing via a single board to any standard SPC slot, use approved bus drivers and receivers, and present only one unit load to all signal lines.

A 2048-byte RAM in the controllers provides a full 3-sector data buffer in all applications. This eliminates "data late" worries, permits multiple contiguous sector reads, allows complete flexibility in selection of data packing or interlacing strategy, and permits the controller to be operated at a low bus priority level. Dedicated hardware in the units enhances microprogrammed error control functions, permitting all standard ECC/CRC operations to be performed at full data rates under all interlace methods. *(continued on page 54)*

A Cost-Effective High-Speed Data Acquisition Network

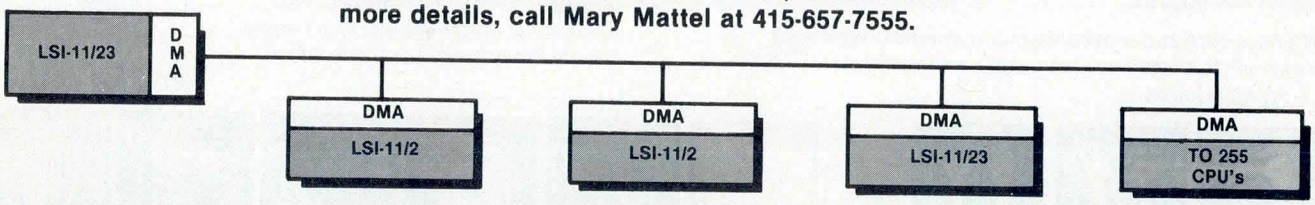
Micro-Link

LSI-11/2* and LSI-11/23* users can share resources, share loads and save money. Standard Engineering's new Micro-Link offers high-speed networking in a complete software/hardware package for only $4,950.

Micro-Link software is simple to use. The RT-11* handler supports HDLC protocol. Micro-Link reconfigures whenever a failure occurs. Files up to 65K words can be transferred.

An intelligent DMA controller gives fast Q-bus interface. One MHz speed is noise immune. Two dual-height boards make up a station. A coaxial cable interconnect minimizes installation costs.

The Micro-Link is offered with one master and one slave. Additional stations are $1,950 each. For more details, call Mary Mattel at 415-657-7555.



*LSI-11/2, LSI-11/23 and RT-11 are trademarks of Digital Equipment Corporation.

STANDARD ENGINEERING CORPORATION
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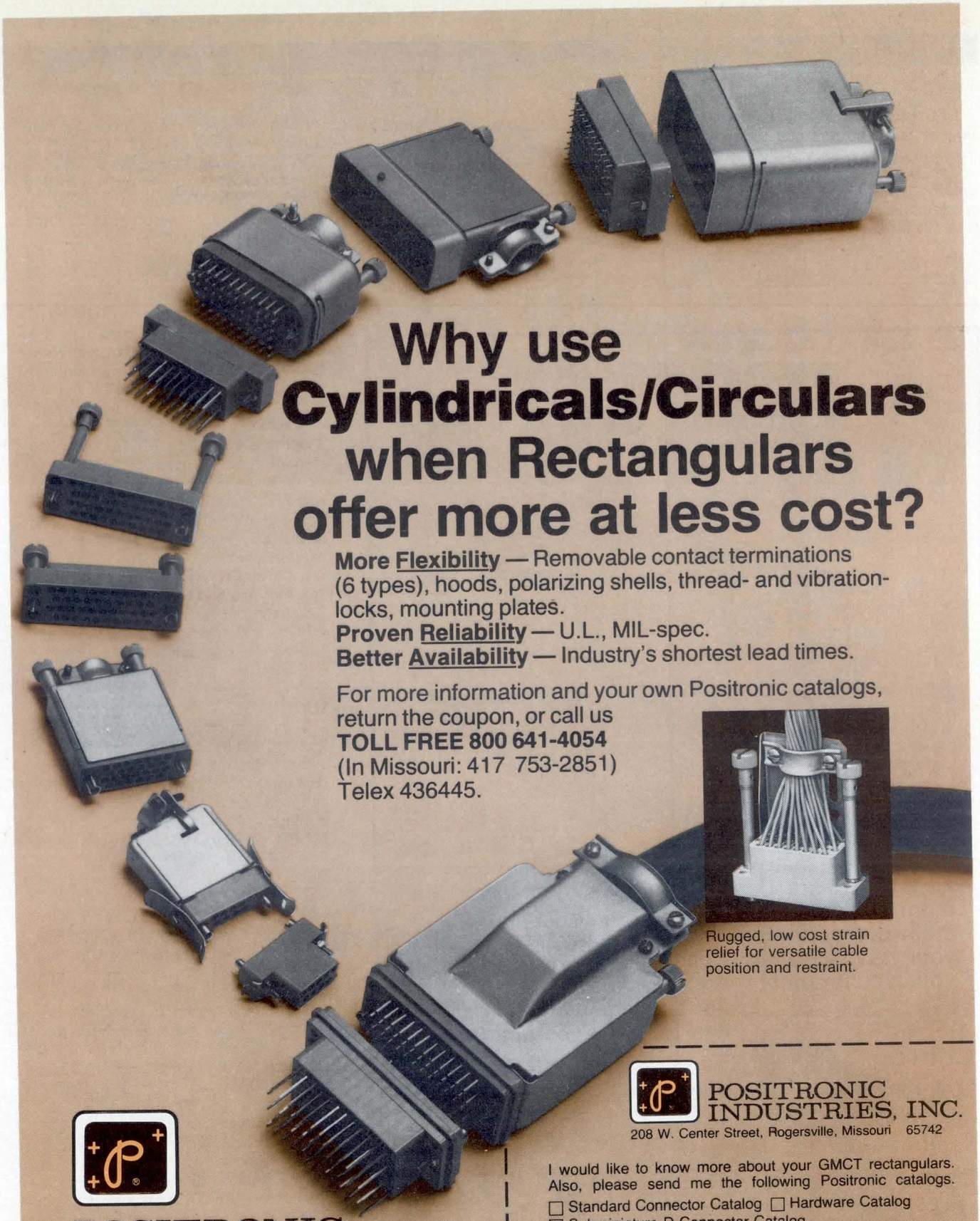

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CIRCLE 36 ON INQUIRY CARD

Convenience features include bus priority level jumpers and slide switch selection of bus address range, interrupt vector, and configuration or operational options. Onboard LEDs provide error condition and operating mode displays.
Circle 352 on Inquiry Card

Computer Graphics Subsystem Serves as Low Cost Alternative

A low cost computer graphics subsystem featuring a microprocessor video display terminal, graphic options board, and printer has been introduced by MQI Computer Products, 18381 Bandilier Circle, Fountain Valley, CA 92708. Offered as an alternative to systems costing nearly twice its $4500 approximate price, it is designed to work with existing systems, or on an individual basis.

Heart of the system is the model G100 microprocessor controlled graphics option board. The G100 is a Tektronix compatible graphics option for TeleVideo® TVI-192, -920, and -950, and converts video display terminals to Tektronix compatibility. The model G150 terminal is equipped with the G100 board.

Features of the board include Tektronix 4010/4012 graphics format, Tektronix 4012 Alpha Mode, 512 x 250 resolution scaled from 1024 x 780, optional alpha and graphics display keys, optional graphics clear key, and optional graphic cursor with keypad. The board also supports a FORTRAN subroutine package for DEC PDP-11 and LSI-11 installations available on RT-11, TSX, RSX-11M, and IAS operating systems. Installation of the board does not interrupt normal functions of the terminal, and may be accomplished by a qualified engineer, or arranged through MQI dealers. Suggested price for the G100 is $1395.

The G150 microprocessor video display terminal offers industry compatibility, using a Lear Siegler compatible code structure. Other features include upper and lower case characters, 12 x 10-char resolution, 24 x 80-char display, and a 12″ (30-cm) (diagonal measure) nonglare screen. Keyboard has 83 keys, including alpha lock, and a 14-key numeric pad with decimal. Cursor control provides left, right, up, down, home carriage return, line feed, tab, back tab, and new line. The G150 display terminal with G100 graphics option board carries a suggested price of $2495.

Hardcopy printout is provided with the model G160 computer printer that features a speed of 32 dot rows/s at 560 dots/row. Position accuracy is ±0.25 dot at 100 dots/in (39/cm) vertically. Line length is 560 dots in a 7.2″ (18.3-cm) line centered on an 8.5″ (21.6-cm) page. The printer may be used with or without a CRT as graphics input may be obtained directly from the CPU. Copies are provided on special 8.5″ (21.6-cm) width industry standard aluminized paper, available in 300′ (91-m) rolls. Images are formed directly on the paper, requiring no ribbons, toner, or type elements. Suggested price of the MQI G160 computer graphics printer is $1995.
Circle 353 on Inquiry Card

CIRCLE 37 ON INQUIRY CARD

Designing Digital LED or Laser 0.1–50Mb/s Fiber Optics?

This new Receiver puts you a MILE and a YEAR ahead!

Yes, even with an error rate better than 10^{-9}, this new OIS Series ORX5000 wide-band TTL receiver gives you far more link length than any conventional design in its price class. Think *kilometers*, not hundreds of meters...even with LED sources.

The same engineering staff that developed our state-of-the-art 275Mb/s ECL transmitters and 150Mb/s ECL receivers has created this lower-cost, medium-speed TTL design, and equipped it with *every one* of the special OIS circuit features that anticipate—*and respond to*—the system constraints of modern link design. Considered together, they could easily save you a *man-year or more* of engineering. Check them:

- Operates from the simplest low-cost unregulated power supply — all regulation required is *on board*, for all voltage levels. Transient protection? Also *on board*.
- Prevents reverse-voltage burnout — protection is *built in*.
- Blocks conducted interference — efficient, high-frequency EMI filtering, *plus* photodiode bias-decoupling filters, all included, all thoroughly field proven.
- Provides an *ancillary analog output* (as well as balanced, complementary digital line-driver outputs). This is invaluable for sophisticated clock-recovery systems.
- Prevents detector drift with temperature (in APD models), providing automatic, built-in bias-current compensation.
- Provides enough line-driver power for *reasonable* lengths of output-pulse distribution, on *low-impedance* coax lines.
- Provides EMI-tight electromagnetic and electrostatic shielding, for high S/N integrity in high-intensity noise environments.

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CIRCLE 38 ON INQUIRY CARD

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The Perfe

Possible? Why not? At Signetics, we're heading in the right direction.

For example, we helped you enhance your system performance with high-speed 4K and 8K PROM's. Their access times are a low 45ns and 55ns, respectively—with even faster speeds to come.

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We made one-stop shopping a reality with a broad selection of industry standards and special function memory products. From low-density memory and logic parts to high-density PROM's that meet the most demanding commercial, industrial, and military applications.

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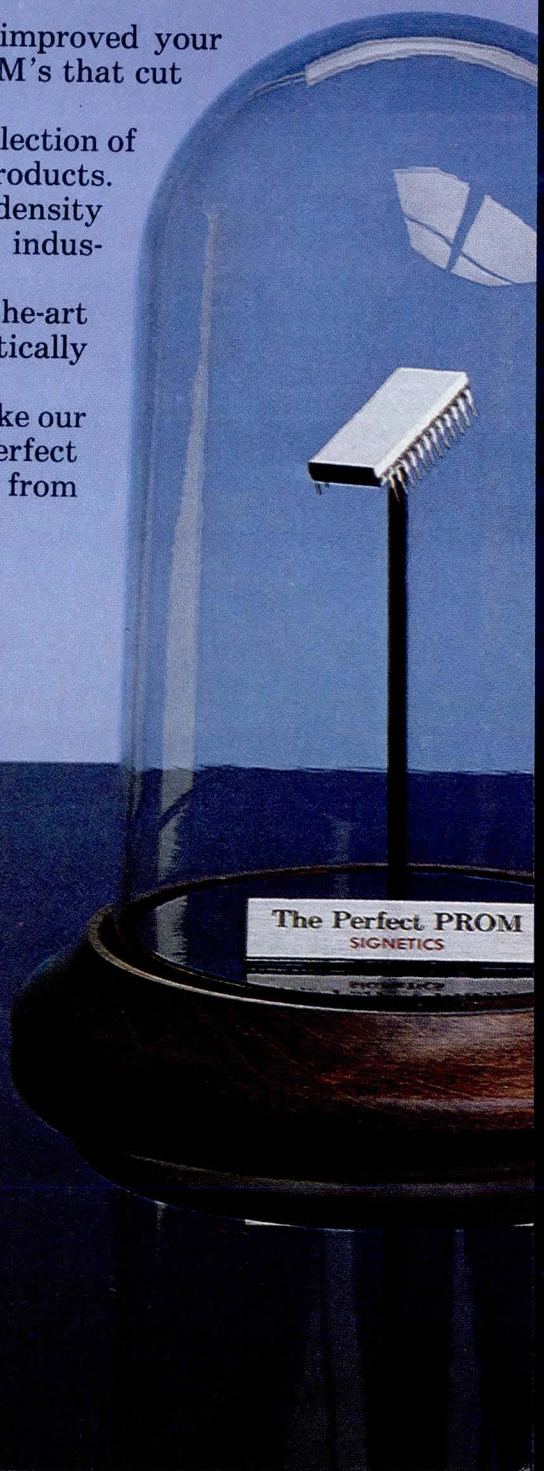
Other high-speed and high-density breakthroughs—like our 32K PROM—are just around the corner. Perhaps the Perfect PROM isn't far behind. When it does come, it will come from Signetics, your high performance PROM leader.



ct PROM.

BIPOLAR MEMORY SELECTION GUIDE

DENSITY	DEVICE TYPE	ORGANIZATION	OUTPUT CIRCUIT	ACCESS TIME (ns)	I_{CC}MAX. (mA)
256-Bit	82S23	32X8	OC	50	77
256-Bit	82S123	32X8	TS	50	77
256-Bit	10139	32X8	OC	20	145
1K	82S126	256X4	OC	50	120
1K	82S129	256X4	TS	50	120
1K	10149	256X4	OC	20	150
2K	82S130	512X4	OC	50	140
2K	82S131	512X4	TS	50	140
4K	82S115	512X8	TS	60	175
4K	82S141	512X8	TS	60	175
4K	82HS147	512X8	TS	45	155
4K	82S137	1024X4	TS	60	140
4K	82HS137	1024X4	TS	45	140
8K	82S180	1024X8	OC	70	175
8K	82S181	1024X8	TS	70	175
8K	82LS181	1024X8	TS	150	80
8K	82PS181	1024X8	TS	70	185
8K	82HS181	1024X8	TS	55	175
8K	82S2708	1024X8	TS	70	175
8K	82S183	1024X8	TS	60	175
8K	82S185	2048X4	TS	100	120
8K	82HS185	2048X4	TS	60	155
16K	82S191	2048X8	TS	80	175
16K	82HS191	2048X8	TS	60	175
16K	82S195	4096X4	TS	70	155
32K	82S321	4096X8	TS	90	175

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- ☐ 8K Power Strobe
- ☐ 8K High-Speed
- ☐ 16K High-Speed

☐ I have an urgent requirement. Please have a bipolar memory specialist phone me at once.
( ) _____.

Name _____ Title _____

Company _____ Division _____

Address _____ MS _____

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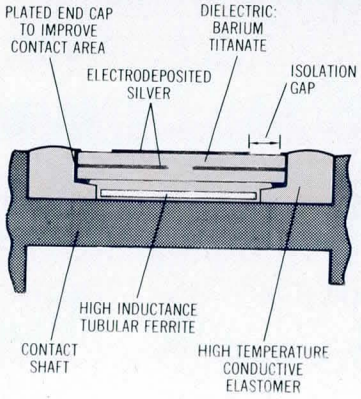
MIL-C-38999 Type Filtered Connector Replaces Discrete Blackbox Apparatus

A filter version of MIL-C-3899G high-density circular environmental connectors, the 418f series has 12 times the rf current grounding capability of standard circular filtered connectors. Developed by Bunker Ramo Corp's Amphenol North America Div, 2122 York Rd, Oak Brook, IL 60521, the filtered receptacles can be used to directly replace widely used "blackbox filtering," whereby sensitive electronic equipment requiring protection from conducted emi/emp is hardwired to individual discrete filters located in bulky blackbox housing. Instead, lumped element barium titanate filters within the connector's contacts remove spurious signals from the cable bundle. Elimination of the blackbox apparatus results in space savings of up to 70%, improves overall filtering performance, and removes the threat of equipment malfunction or failure associated with hardwiring.

Two design elements provide the superior grounding capability and ability to meet MIL-spec performance requirements. A unique mass grounding system allows each filter pin contact to conduct 5 Adc and simultaneously pass 3 A of rf current to ground. Standard offerings are able to bypass only 0.25 A rf to ground. The grounding system consists of a conductive metal-filled thermosetting polymer that is allowed to "cold-flow" into a 0.125" (0.317-cm) void between the connector's front and rear dielectric inserts. The void is created by a cast grounding ring placed around the contact matrix, near the filter capacitor's ground electrodes. Bypassed current is conducted through the polymer and grounding ring to ground via an rfi spring finger mounted in the connector shell that contacts the grounding ring when the connector is fully assembled. The polymer also serves as a heat sink, dissipating up to 60 °C heat generated by the bypassed current and enhancing connector reliability.

Enabling the unit to withstand shock and vibration during operation, and therefore meet stringent MIL-C-38999G requirements, a patented contact to filter stress isolation mechanism ensures protection of the relatively fragile barium titanate filter element. The mechanism consists of conductive washers made of a silver impregnated, high grade elastomer attached to each end of each capacitor contact electrode. The conductive washers dampen all connector stresses and virtually eliminate the chance of filter element cracking, from vibration, thermal and physical shock, and inadvertent bending and rotation of contacts during mating.



Amphenol's 418F, filtered version of MIL-C-38999G circular environmental connector, eliminates need to provide external filtering for sensitive electronic equipment. Cutaway drawing shows barium titanate ceramic tube capacitor, tubular ferrite, and conductive elastomer washer making up filter

Receptacles are available in Series I and II versions for either square flange or jam nut mounting. They feature bayonet coupling, self-sealing rear grommets, and choice of solder cup, pin tail, wire wrapped, or crimp piggyback socket rear release contacts. Four standard filter contact types are available with cutoff frequencies of 9 or 2.5 MHz and 400 or 60 kHz. Rf current dissipation is rated at 3 A for all filter types; all contacts exhibit a continuous current rating of 5 Adc.

The series includes eight high density insert configurations from 13 to 128 contacts, in shell sizes 11 through 25 and 10 through 24. They meet or exceed all performance requirements of MIL-C-38999G, except for temperature shock where the upper temperature has been reduced from 175 to 125 °C, and voltage at altitude where the upper limit has been reduced from 110,000 to 75,000 ft (33,528 to 22,860 m).

Circle 354 on Inquiry Card

Desktop Computer Systems Use Disc Resident Operating System

Small business computers based on the MC6809 microprocessor, BX-3 and CX-1 are compact desktop units designed to automate business operations. The system's disc resident operating system fully utilizes hardware features. Canon U.S.A., Inc, Systems Div, One Canon Plaza, New York, NY 11042, also provides a comprehensive file management system that supplements index sequential, sequential, and random file access.

About the size of a standard electric typewriter, the BX-3 provides the user with 32k bytes of RAM expandable to 96k bytes. 28k-bytes of RAM and 4k bytes of ROM are used by the system. Dual-mini-floppy discs provide 320k bytes of capacity on each drive.

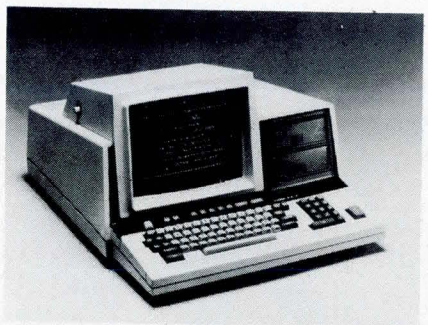
The system uses a full typewriter keyboard and 10-key numeric pad to access internal memory. Its single line 28-char display uses a full ASCII set; hard copy is provided by an integral serial impact printer that is also capable of 4-directional plotting. This unit outputs 80-col lines at 80 char/s, and 160-col lines half pitch at 160 char/s.

Designed for faster operations, the CX-1 replaces the single line display with a 12" (30-cm) monochrome CRT with capacity for 1920 characters. Internal capacity is the same as that of the BX-3; however, expansion is possible using high speed printers and 8" floppy disc drives.

Both units are programmable in BASIC and assembly language. BASIC offers a variety of instruction sets for matrix computation, index sequential access, and graph plotting by dot control.

A BX-3 has a price of under $5600; the CX-1 will sell for $4000.

Circle 355 on Inquiry Card



Canon's CX-1 small business computer offers 12" CRT screen with dual floppy disc system in desktop unit about size of standard typewriter

LSI Digital IC Tester Expands Capability to 48 Pins

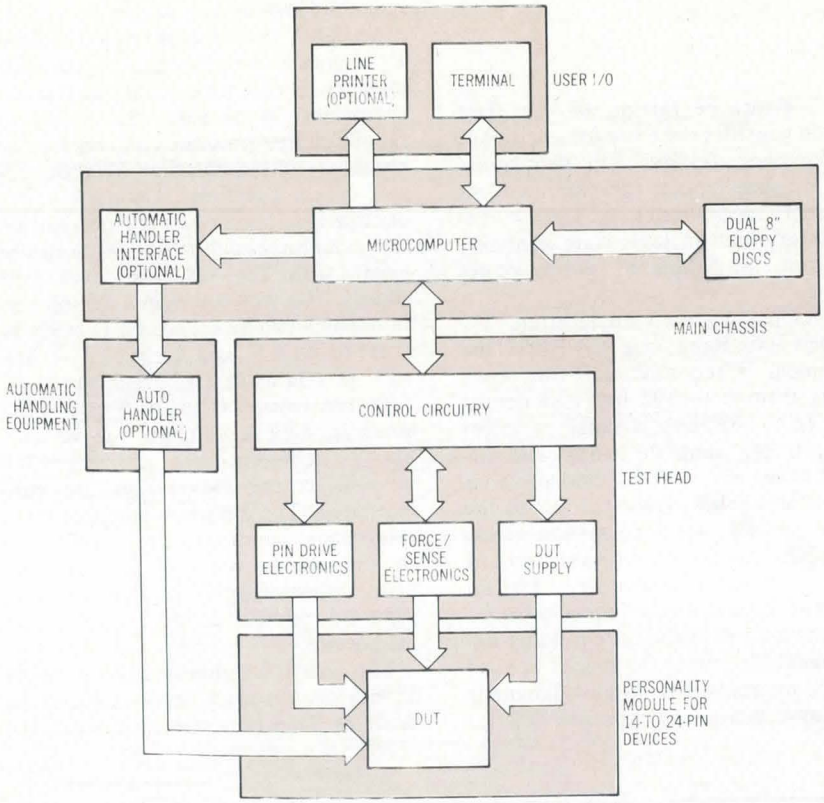
Inspector™ 100/4 is a microcomputer based tester designed for incoming inspection, production testing, and laboratory use. Providing 48-pin test capability, the unit, developed by Pragmatic Designs, Inc, 950 Benicia Ave, Sunnyvale, CA 94086, performs both functional and dc parametric tests on CMOS, PMOS, NMOS, and LS/TTL under control of the TRASIC-Y test language.

The system has three device power supplies, programmable to 25 V. All device pins are actively driven from the test head, eliminating the need for expensive device personality boards. All pin drivers have full force/measure capability. The system's precision measurement unit has full force current/measure voltage, force voltage/measure current, and differential measurement capability with resolution of 5 mV and 5 nA. The test head also has a programmable hardware clock generator up to 1 MHz.

Each test head is a complete set of test electronics and has its own set of parametric capabilities optimized for the particular device type being tested. Interchangeable test heads allow the system to be configured to optimize cost/performance for each class of devices and thereby reduce the cost to the end user. All test heads are capable of performing parametric tests on all critical parametrics for the various device families. Tests are performed on the device input parameters V_{IL} to I_{IL}, V_{IH} to I_{IH}, the output parameters V_{OL} to I_{OL}, V_{OH} to I_{OH}, 3-state parameters V_{OZL} to I_{OZL}, V_{OZH} to I_{OZH}, and supply currents.

Limits for all input and output pins are completely programmable. In the extreme, each device input or output pin can have its own set of parametric limits. This makes the tester useful for testing older, nonstandard parts, while also providing an effective tool for custom devices. The test language automatically keeps track of which pins have failed each test.

Functional tests are performed while applying user defined input patterns to the DUT inputs and testing the outputs for the correct state. Functional tests can be performed with the DUT output pins loaded or unloaded. Because the tester patterns are completely program controlled, most device test plans can be derived directly from data sheets and require relatively few statements. Programmability also means that complex sequential parts can be tested reliably, a very difficult task with the commonly used "random pattern generator" type of tester.



Microcomputer based Inspector 100 performs both parametric and functional tests on devices having up to 48 pins. Pragmatic Design's digital IC test system has three device power supplies and drives all device pins from test head

Personality modules configure the test heads to accept standard DIPs. Each personality module contains a TEXTOOL™ zero insertion force socket to allow fast, efficient handling of devices in a production environment.

Personality modules are available in 8-, 14-, 16-, 18-, 20-, 22-, and 24-pin sizes. All pins are actively driven allowing one personality module to be used to test all devices with the same number of pins. This provides great savings compared with testers that require one personality module for each device.

The system is controlled by the TRASIC-4 test language. Based on BASIC the language makes it easy for the system user to develop and modify test programs. Test programs for common devices are available and furnished in source form for easy understanding and modification. The language has an integral pattern compiler for generating fast functional test patterns.

Standard test system includes dual 8" floppy disc drives, CRT terminal, Z80 microcomputer system controller with 32k bytes of memory, and CPM disc operating system. Users need only the TM4 test head to upgrade existing Inspector systems to 100 full 480-pin capability.

A complete system with software is priced under $28,000. Options include line printer, auto handler interfaces, and test programs for standard devices. Initial deliveries are scheduled for first quarter 1981.

Circle 356 on Inquiry Card

Bit-Slice/Bipolar Development Tool Cuts Microprogramming Costs

Step-3 Firmware Integration and Test Station provides the tools for microcode development, testing, and debugging. The bit-slice/bipolar development instrument incorporates a fast P/ROM simulator, built-in logic state analyzer, terminal, and special debug-panel controls.

Developed by Step Engineering, 757 Pastoria Ave, Sunnyvale, CA 94088, the instrument is reconfigurable for word widths from 8 to 192 bits and depths from 1k to 48k, over a range of access times. It can simulate nearly 300 different ROMs and P/ROMs, and provides simulation cables engineered out to the P/ROM sockets, specified system access time including cables, and user tests of worst case system access time. The instrument is completely independent of and transparent to the system under development, requiring no special control lines or interconnects. English language commands along with extensive description messages and self-test capabilities make the system easy to use.

Writable control store (WCS) simulates all or part of the microcode/application memory in real time during system development. It provides the ability to rapidly change program contents for fast checkout and generation of processor and system functions. Up to five WCS organized as one or two independent arrays, can be resident. Nine WCSs can be used, with the optional expansion chassis. The WCS comes in a 32k-bit version which can be organized 1k x 32, 2k x 16, or 4k x 8, and a 128k-bit version with 4k x 32 or 3k x 16 organization.

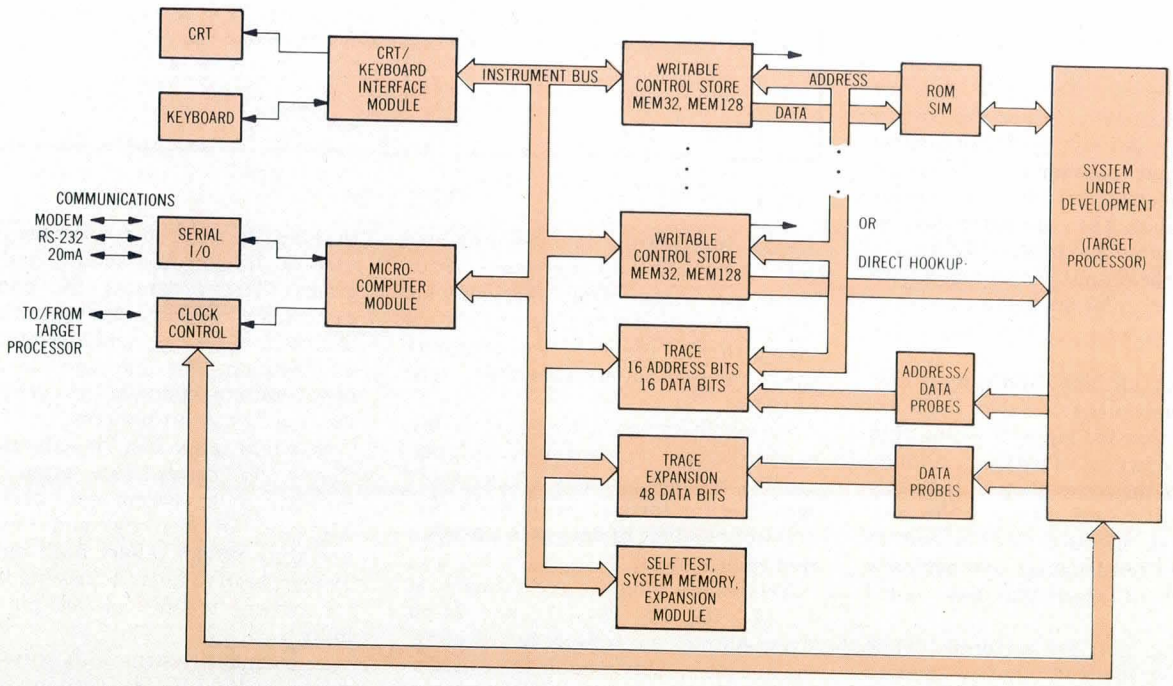
System organizations of 8 to 96 bits/word in 4-bit increments can be efficiently achieved; 192 bits/word are possible if the two arrays are concatenated. The ability to simulate more than one memory array is useful in multiprocessor systems, systems with ROM address mapping, and systems with separate microcode and application memories.

The system is connected to the target processor through ROM simulation modules. They plug directly into existing P/ROM sockets on both breadboard and production systems. These personality modules emulate existing ROMs and P/ROMs mechanically, electrically, and functionally and can be field upgraded as types change. Alternatively, the WCS can be connected directly to the target processor through a ribbon cable array connector. Each WCS has a bit mapping area and choice of interface type (buffered, nonbuffered, and register) to simplify the interconnect.

On each writable control store, a realtime breakpoint (BNC output) is provided which can be used to halt the user's processor or trigger a logic analyzer or oscilloscope. The state of each breakpoint along with the current processor address is displayed on the CRT. Multiple breakpoints simplify conditional jump analysis by displaying the alternative program paths being executed.

The instrument is controlled through the keyboard and front panel switches. Special purpose function keys simplify editing downloading and controlling the target processor. An easy-to-read, fully

(continued on page 62)



Step Engineering's firmware integration and test station has reconfigurable variable word width writable control store, P/ROM simulator, built-in logic state analyzer, terminal, and debug panel controls. Architecture independent, instrument speeds debugging of bit slice, sequencer/controller, and pipelined architectures as well as MOS processors

FROM STATISTICAL MULTIPLEXORS TO COMPLETE DATACOMM NETWORKS, EVERY DCA COMPONENT IS

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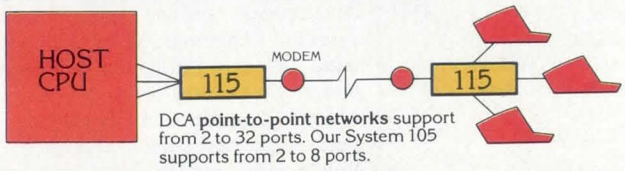
DCA protects your initial investment in statistical multiplexors with the lowest-cost network growth in the industry. So you can start with a small datacomm network today, and expand or modify it to meet your needs tomorrow.

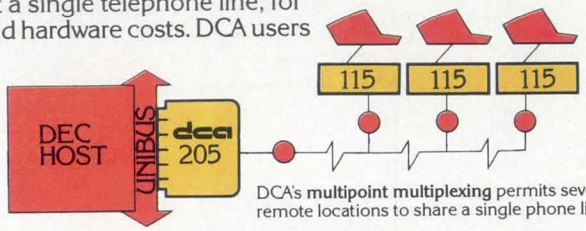
Our System 115 statistical multiplexor can be used in point-to-point networks to support from 2 to 32 asynchronous terminals at a remote site. DCA's statistical multiplexing assures excellent response time, character transparency and error-free transmission.



DCA **point-to-point networks** support from 2 to 32 ports. Our System 105 supports from 2 to 8 ports.

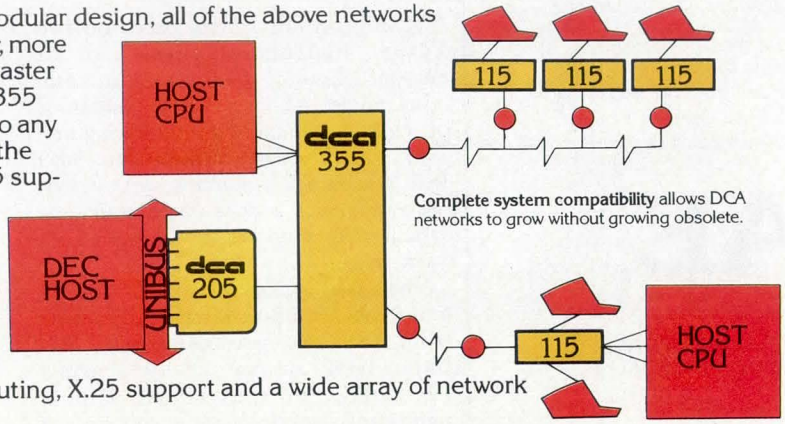
DCA's multipoint multiplexing configuration serves a number of remote terminal locations with just a single telephone line, for substantial savings in phone-line and hardware costs. DCA users have benefited from multipoint multiplexing since January 1979.

DCA's System 205 is a statistical multiplexor designed for DEC UNIBUS*-based computers. The 205 requires only one UNIBUS slot to emulate up to 16 DEC DZ11 modules and a 128-port stat mux. This greatly lowers hardware costs and improves response time as well.



DCA's **multipoint multiplexing** permits several remote locations to share a single phone line.

Because of DCA's unique modular design, all of the above networks could easily expand into larger, more powerful networks. As the master network processor, System 355 gives terminal users access to any host computer anywhere in the network. In addition, the 355 supports up to 126 ports, 62 of which can be high-speed synchronous trunk links. Several 355's can be combined to greatly expand this support. Features include port contention, switching, unlimited routing, X.25 support and a wide array of network management tools.



Complete system compatibility allows DCA networks to grow without growing obsolete.

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CIRCLE 39 ON INQUIRY CARD

New EPROM Tester and Duplicator

The new UPP-2700 is now saving thousands of dollars for its owners by testing EPROMS both before and after programming. Many customers like Bell Labs, IBM, Litton and others have found the value of screening marginal EPROMS *before* they reach their end product.

The UPP-2700 from OAE is the only EPROM duplicator which tests for shorts, opens, excessive leakage, and static damage on both data and address buses. This combined with sink and source current tests makes the UPP-2700 the most advanced production duplicator available today.

Simply touch the AUTO PROG key and the UPP-2700 will TEST-PROGRAM-VERIFY and TEST sixteen 2708's in less than 130 seconds! All EPROMS from 2704's to the new MCM68764 may be both tested and programmed using plug-in firmware modules. Add the UPP-2700S Satellite Tester/Duplicator and program up to 32 devices simultaneously!

For a complete information packet on the UPP-2700 simply fill out and return the form below or call the OAE HOTLINE at (213) 240-0080. Find out why 3 out of 4 manufacturers who try it, buy it!

OAE

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Dept. 321, 676 West Wilson Avenue
Glendale, CA 91203 (Telex: 194773)

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Div/Dept _____ Mail code _____

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State _____ Zip _____

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62 **CIRCLE 40 ON INQUIRY CARD**

formatted CRT displays the memory contents, system states, and all information required to operate the instrument. Descriptive error messages reveal improper instrument setup, invalid commands or addressing, and serial link failures. Recovery from an error condition is automatic upon entering the corrected information.

Internal self-test programs test CPU and memory. A self-test option measures WCS and ROM simulation access times at the target processor interface. Testing both ports of the dual-port WCS memory dynamically, the routines offer both short-form and more exhaustive long-form galloping pattern tests.

The system acts like a terminal, connecting to computers, minicomputers, development systems, and timesharing systems. Through keyboard control, baud rate and parity are configured to match an existing computer system (or P/ROM programmer). Once the computer link has been established, files, source code, object code, etc. can be displayed on the unit's CRT, or object code can be downloaded into memory. Transfer of object code to or from the external device is automatically initiated and synchronized on operator command.

Circle 357 on Inquiry Card

Small Business System Uses 16-Bit Micros For Task/Storage Processing

A multiprocessor system based on two Texas Instruments 9900 16-bit microprocessors, small business computer model T.I. 32 acts as a standalone or remote terminal in a timesharing network. Developed by Technico, Inc, 9051 Red Branch Rd. Columbia, MD 91405, the system has a ROM based operating system that supports from two to six workstations.

The system gains speed and ease in multi-user, multitasking applications from the 9900 microprocessor. Reentrant multi-user code lets users expand the number of workstations without significantly increasing the amount of main memory. In addition, FORTRAN, BASIC, and assembly language can be run on the same system, while other systems run only BASIC.

Offered as a standalone system or a remote processing terminal within a timesharing network, the system has 64k of user memory, expandable to 192k. Additional storage is attained through use of optional dual double-sided floppy drives, 8 or 14" Winchester discs, and 3M cartridge tape units with capacity for 1M to 116M bytes.

Business applications packages include a multijournal, multidivision, multiprofit center general ledger package, payroll/personnel package, receivables, payables, and inventory. Mailing list and database management are also offered.

Circle 358 on Inquiry Card

Minicomputer Based System Reduces Overall System Development Costs

OPTIMA 910, serves as a COBOL development tool, database manager, and online transaction processor. Utilizing proprietary CENTRAL SOFTWARE and configured around an interactive DEC PDP-11/34 minicomputer, the system from Planning Research Corp, Commercial Products Group, 3 Perimeter Rd, Manchester, NH 03103, provides a functionality and capability that has previously been associated with large mainframe installations.

Simple to understand and operate the COBOL based software can reduce overall development costs by approximately 60%. Once developed, CENTRAL SOFTWARE allows programs to be recompiled for use on IBM mainframes with only minor copy statement modification. The system can reduce system development time by as much as 80% when compared with conventional Cobol system development efforts.

Once information is entered, it need never be re-entered, the system organizes and stores information in a central set of files that can be immediately accessed by all programs. In addition to efficient data file management, the system's database manager provides complete record I/O management. It handles addition, deletion, and record modification automatically and immediately frees space following deletion. The database manager also permits selective index creation or deletion with complete backup and recovery, online with no batch utilities to run.

Standard configuration includes a PDP-11/34 minicomputer, 256k bytes of main memory, two RK07 disc drives with a combined storage of 56M bytes, VT100 video display terminal, and RSX-11M operating system. Prices begin at $57,700.

Circle 359 on Inquiry Card

- Motorola MC68000 16-bit processor
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CIRCLE 41 ON INQUIRY CARD

SOFTWARE

Pascal Package Added For Data General Operating Systems

Pascal packages for MP/OS and AOS/VS operating systems have been added to those available for disc based AOS, RDOS, and DOS operating systems by Rational Data Systems, 245 W 55 St, New York, NY 10019. MP/OS runs on microNOVA and NOVA 4 computers, while AOS/VS runs on the 32-bit MV-8000.

Each implementation's compiler generates P-code which can be executed on any other implementation. Programs developed on an MV-8000 under AOS/VS will execute on Eclipses, NOVAs, or microNOVAs; programs developed on a microNOVA execute on the 32-bit MV-8000.

Users may generate a P-code interpreter to match any hardware/software configuration. For example, floating point operations are performed in software on the microNOVA, but the same P-code makes use of hardware floating point processors on larger machines.

Evaluation releases of each implementation will be provided with Programmer's Manual for $50 to allow potential customers to evaluate the products on their own systems, using their own benchmarks. Standard license fees are MP/OS, $2500 and AOS/VS, $3500.

Circle 360 on Inquiry Card

BASIC Package Includes Extensions to ANSI Specification

High level MP/BASIC for microNOVA™ and NOVA® 4 computers includes powerful extensions to the ANSI specification that make the language suitable for applications in technical, scientific and educational fields. Announced by Data General Corp, Rte 9, Westboro, MA 01581, the package can increase productivity because it is easily learned and operates in an interactive way to provide quick turnaround.

It also helps the user maximize the return on his computer investment providing the ability to use the computer in areas where other languages are too complicated and time consuming. Enhancements to the ANSI standard include string variables of any length, string concatenation, substrings, and letter-digit array names. Nine additional math functions, eight string functions, fixed and variable length file manipulation, and integer data types are also provided. Provision for an assembly language interface enables BASIC programs to interface to the full range of system capabilities.

Circle 361 on Inquiry Card

Program Transfers Files Between Double-Sided Floppy Discs

File transfer between IBM and DEC computers can be accomplished rapidly with a software option for DSD 480 double-sided floppy systems from Data Systems Design, Inc, 2241 Lundy Ave, San Jose, CA 95131. Dubbed "EXCHNG," the option runs under RT-11 or RSX-11M operating systems, on either PDP-11 or LSI-11 computers.

EBCDIC is automatically converted to ASCII and ASCII to EBCDIC. Any IBM or DEC floppy disc format can be read, written, or copied from one to another. Combination of the floppy disc system and the software will prove useful in facilities that use both DEC and IBM computers. File transfer capability will improve efficiency and usefulness because data or programs resident on one computer can be easily moved to the other. A small DEC system with the combination will be useful even in an all-IBM installation, where translation of data from one IBM format to another is required.

The 480 disc system carries a single-unit price of $4495. The software option has a list price of $500. Quantity discounts are available.

Circle 362 on Inquiry Card

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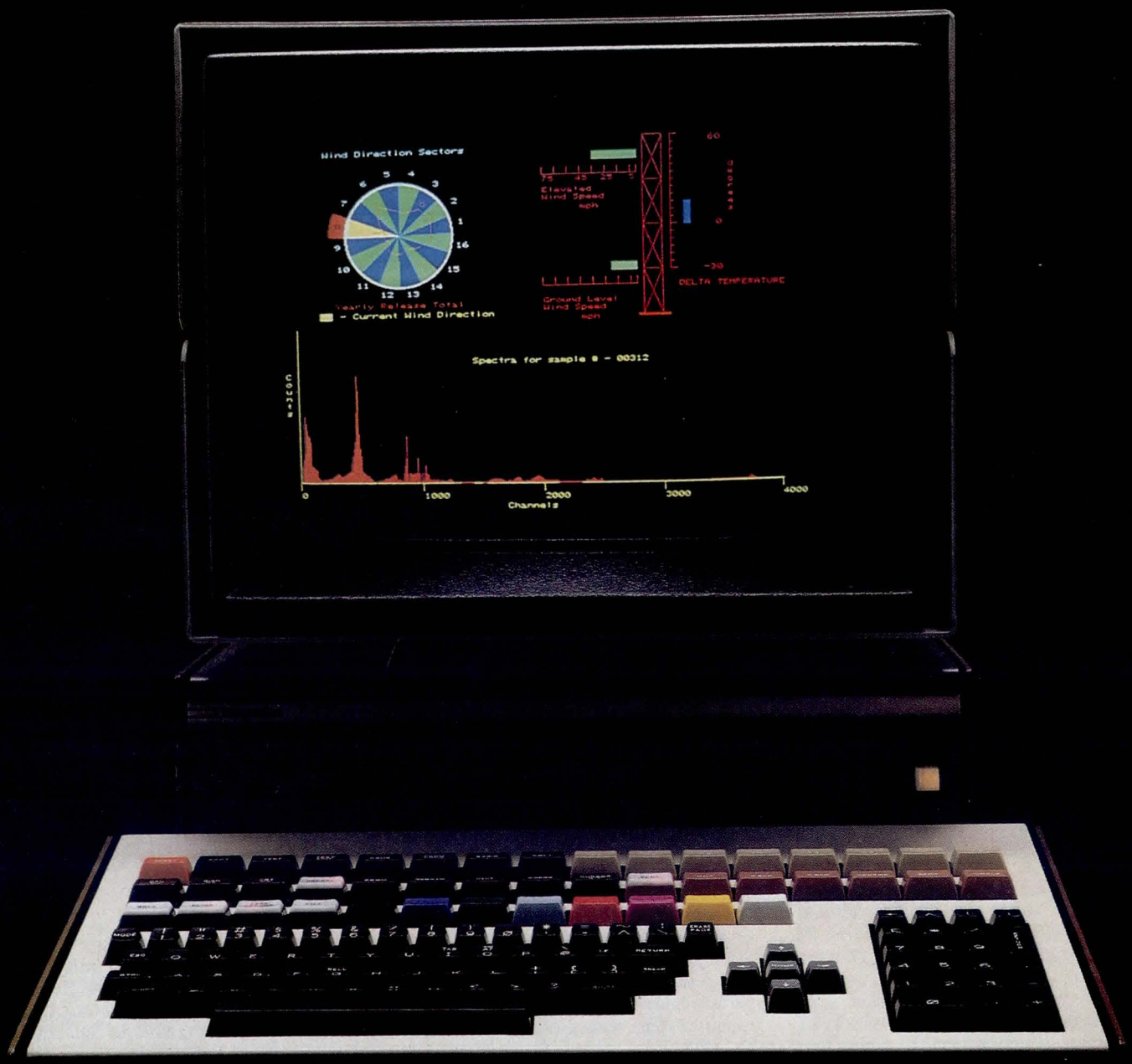

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CIRCLE 43 ON INQUIRY CARD

SOFTWARE

Software Library Extended to Use High Quality Graphics

PLOT 50 software has been extended with seven programs that use the high quality graphics created by 4050 series desktop computers. Included in the library from Tektronix Inc, PO Box 500, Beaverton, OR 97077, are graphing, drawing, document preparation, statistics, planning, management, and digitizing programs. Programs are sold separately at costs ranging from $800 to $4000.

Statistics: Analysis of Variance and Statistics: Multiple Linear Regression are disc based programs that utilize a standard file format to allow different programs in the series to share data. Standard statistical conventions have been incorporated. The software also includes state of the art graphing routines to generate box and whisker plots, scatter plots, and other exploratory plots. In addition, Statistics: Analysis of Variance features 1-, 2-, and 3-way classification of data. Multiple Linear Regression includes routines for multiple, weighted, stepwise multiple, and polynomial regressions.

Primarily developed for scientific and engineering applications, PLOT 50: Project Management consists of predictive modeling tools that analyze combinations of changes, delays, and conditions to minimize conflicts and costs within a project. The interactive modeling package is based on PERT (Product Evaluation and Review Technique) and CPM (Critical Path Method) models, 30 graphic output diagrams, and 19 types of printed reports.

PLOT 50: Picture Composition software is menu-driven. The complexity of drawings created is virtually unlimited, as the user builds drawings from "graphic primitives" including lines, arcs, boxes, and circles. The software also coordinates the Tektronix 4956 Graphics Tablet for digitizing existing artwork.

A package that creates bar charts, line graphs, pie charts, and text on overhead transparencies, PLOT 50: Presentation Aids utilizes a template format. It produces quality text with a software font, widths, and thicknesses, so that charts and graphs may be combined with text on a single overhead slide, as well as produces multiple styles of horizontal bars for graphs, multiple graphs per page to simplify comparison, and multiple styles of vertical bars.

Simplifying the creation of a graphic data base, PLOT 50: Interactive Digitizing is a precise "ruler" that inputs, calculates, and stores data quickly and easily. Graphic data may include drawings, maps, photographs, strip charts, line drawings, or other images which need to be manipulated and studied.

The software utilizes the 4956 graphic tablet for input, and the 4907 file manager, a flexible disc mass storage device. Stored data can be further processed by other software packages via standard file interchanges.

Software Supports Computer Measurement Monitoring Systems

Performance Database Release 2 summarizes, stores, and visually reports data collected by DYNAPROBE computer measurement monitoring systems. It includes support for the complete line of monitors and adds reports and control software enhancements to the previous release. Additional software capabilities include frequency distribution and data time-stamp reports, extended database control language, and enhanced utilities.

The data base, available from NCR Comten, Inc, 1950 W County Rd, B-2, St Paul, MN 55113, provides a complete data reduction and reporting system for performance measurement data. It can support extensive measurement activities by generating reports from data provided by hardware monitors, hardware or software measurement systems, and analytical models. Measurement data processed by the data base can be collected over extensive periods of time with reports generated for hourly, shift, daily, weekly, monthly, quarterly, or yearly time periods. Performance variables can be compared for similar time periods or can be used to track performance variables under different operational environments.

The data base operates on IBM /360, /370, 303X, 4300, or compatible processors running under OS, VS, or MVS, with a minimum of 320k bytes of storage for problem programs.

Circle 363 on Inquiry Card

Security System Protects Desktop Computers From Unauthorized Access

Program security system significantly improves the security of software for Hewlett-Packard 9845B/C and 9835A desktop computers by preventing unauthorized access to software proprietary algorithms and duplication of program media. Developed by Structured Software Systems, Inc, PO Box 1072 Irick Rd, Mt Holly, NJ 08060, OEMSEC enciphers a stored program so that symbol names for variables, labels, defined functions, and subroutines are deleted from the program listing. The listing is meaningless, and it is impossible to TRACE or to interrogate program variables. NODUP prevents duplication of programs stored on tape cartridges so that they cannot be copied or run unless the original tape is also present.

Both packages are supplied on tape cartridges and are available in versions to run on 9845 B/C or 9835A computers. Prices are $2000 for OEMSEC; $2500 NODUP. Together, price is $4000.

Circle 364 on Inquiry Card

Computer Command Language Eases Use and Increases Functionality

Command Procedure Language (CPL) offers greater power, ease of use, and functionality to users of 50 Series Systems from Prime Computer, Inc, Prime Pk, Natick, MA 01760. CPL allows sequences of PRIMOS commands and CPL directives to be stored in a command procedure file which can be executed simply by specifying the file name. Directives provide for passing of arguments into command procedure files for statement execution order control within the files and for error handling. Thus users can combine a number of complex steps into a single command.

The language offers a built-in debug facility that automatically checks syntax. Basic statements are PRIMOS commands; therefore, a user can begin performing simple functions with just a few commands or move quickly to more complex tasks with added experience. □

Circle 365 on Inquiry Card

The smallest 1/2 megabyte microcomputer has the biggest feature of all.

50 megabucks worth of software.

Sure, it's handy to get our HP 1000 L-Series microcomputer on just two boards—with a single board holding the full 1/2 megabyte of memory! But, before you consider buying any microcomputer, you should look beyond the hardware to the software.

After all, that's where most of the time and money is often spent in developing a microcomputer-based system. But you can eliminate almost all that effort by using an L-Series. With $50 million worth of software development behind it, you only have to worry about developing your applications programs.

The L-Series offers you the ideal combination of HP's big system software and economical microcomputer hardware. So you can build cost-effective solutions for data acquisition and control, communications, factory automation and a whole range of other products.

Designer software.

With the minicomputer software that HP has been perfecting for more than a decade, plus our Model 10 Development System, you'll find it's easy to create the system you need.

You can start with either RTE-L or RTE-XL, our powerful multi-programming, multi-user operating systems. Their modular construction lets you build the real-time computing environment your applications programs demand—programs you can develop in Assembler, FORTRAN 4X, BASIC and PASCAL. And our HP DSN networking software makes it simple to put low-cost computing wherever you need it.

Data base management on a board computer? With our IMAGE DBMS, you've got a powerful tool for simple and efficient data management. And you can easily picture the possibilities offered by our GRAPHICS/1000 software. Like our other software packages, these are all upwardly compatible throughout the entire HP 1000 line, giving you an easy growth path to even higher performance.

Efficiency across the board.

How to handle all this software power? Simple. We used an advanced distributed intelligence architecture that puts a separate LSI I/O processor on each interface board. This means each processor has its own direct channel to the entire 1/2 megabyte memory. (We used state-of-the-art 64K RAMS to put the 512K bytes of memory on just one board.) And with the CPU free to concentrate on computation, you get significantly increased throughput and exceptional microcomputer performance.

A range of solutions.

The L-Series comes in a variety of configurations to meet your needs best—from boards and boxes to entire systems. Prices start at only $1968 for a starter set that includes CPU, 64KB memory and one I/O board.

Like our other OEM products, the L-Series is backed by our full range of customer services—including worldwide software and hardware support.

If you'd like a hands-on demonstration, just contact your local HP sales office listed in the White Pages. Or write for more information, and our new OEM catalog, to Hewlett-Packard, Attn: Joe Schoendorf, Dept. 1296, 11000 Wolfe Road, Cupertino, CA 95014.

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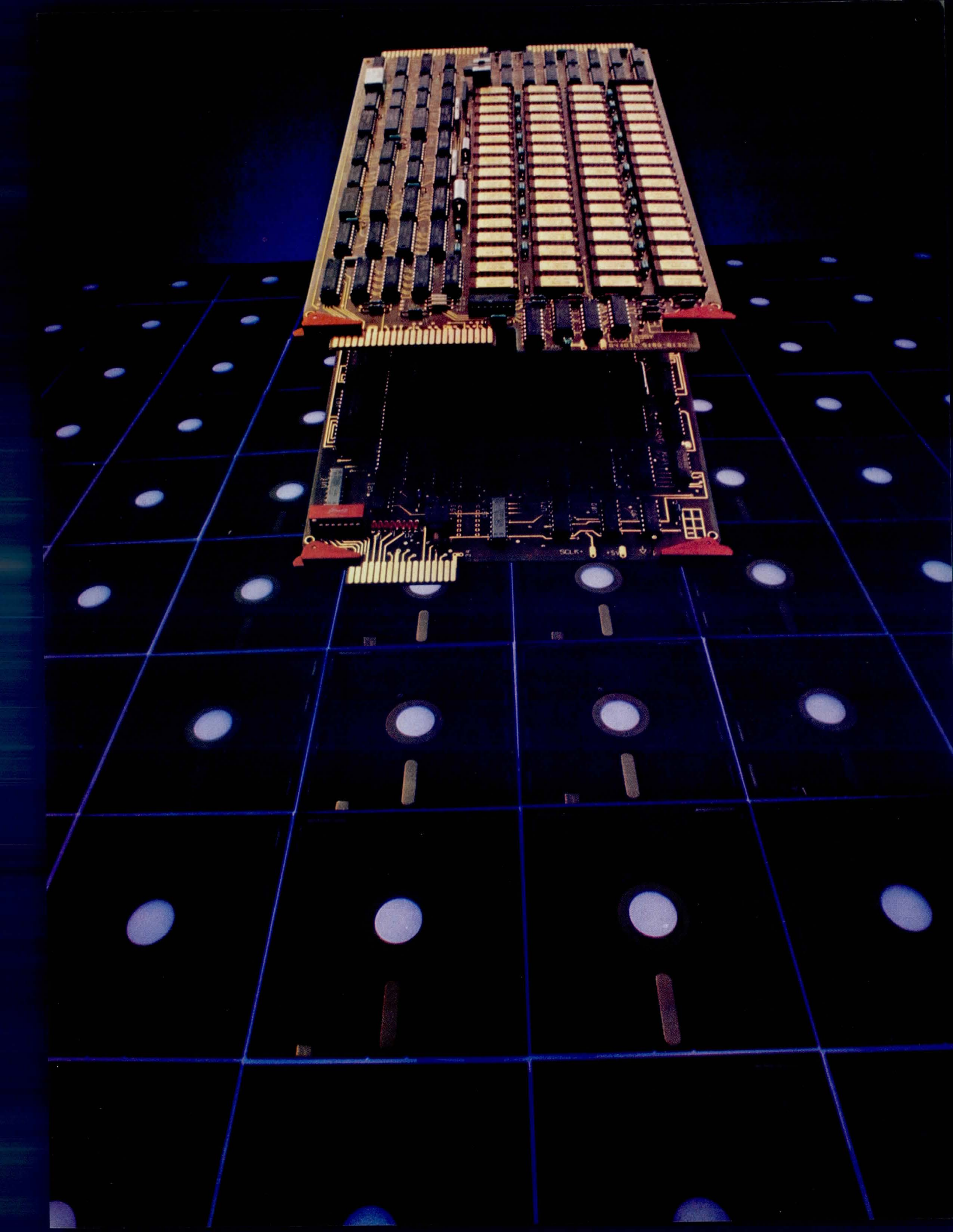
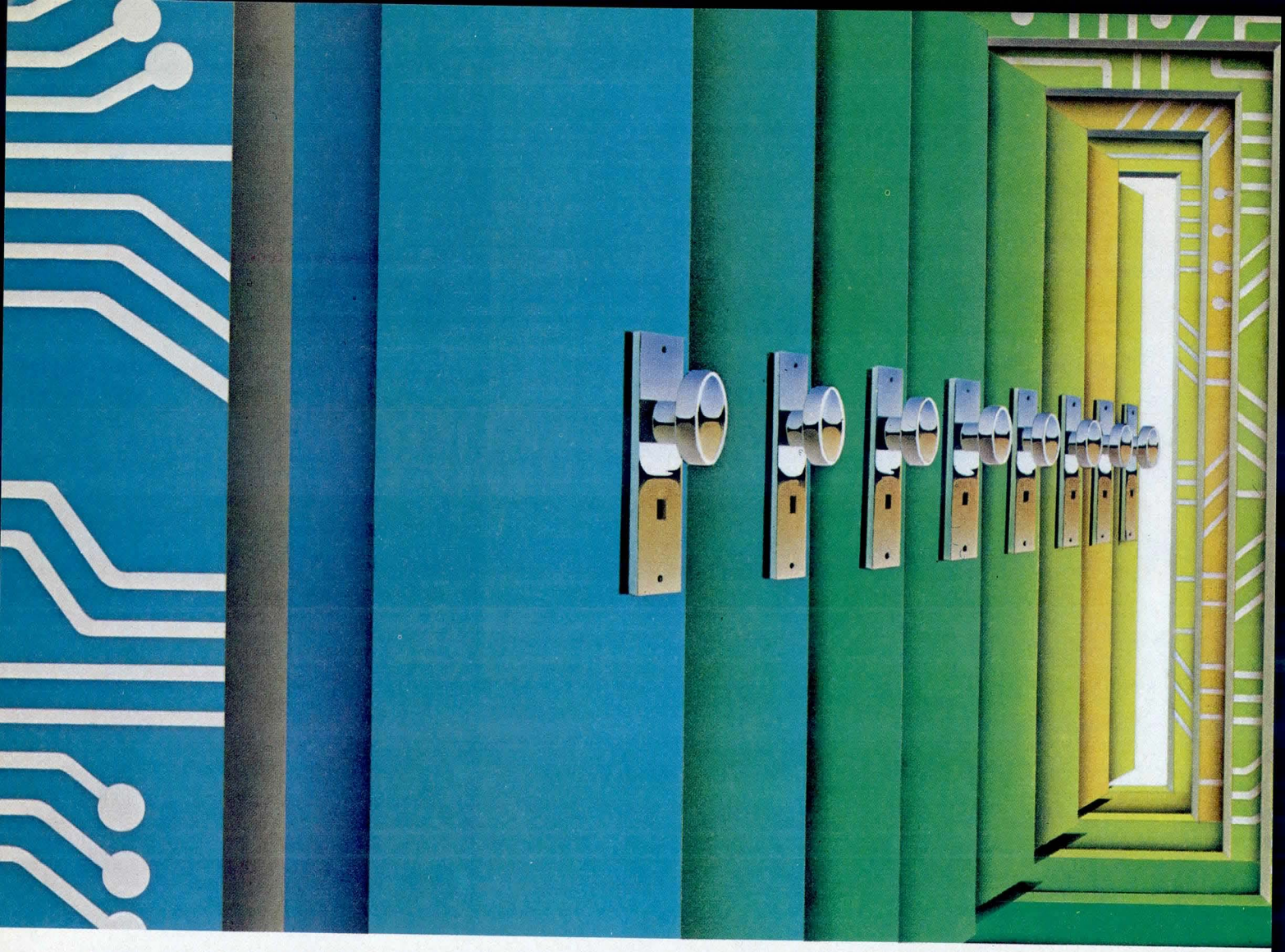




Intel's new E²PROM. We window, to open endless

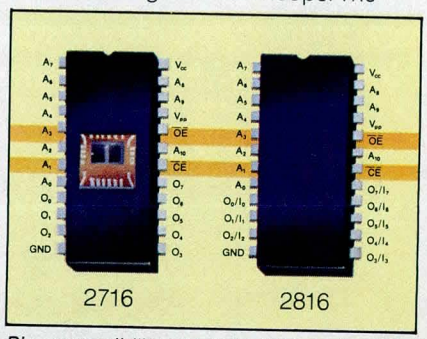
Intel introduces the 2816: the in-circuit Electrically Erasable 16K E²PROM that's both byte- and chip-erasable. Available in quantity today.

For years, system flexibility has been limited by both ROMs and EPROMs. But no more. Now, Intel's 2816 E²PROM combines in-circuit alterability and non-volatility, providing functionality that will advance today's high-performance microprocessor designs. This makes the 2816 a natural to replace conventional ROMs and EPROMs as the standard storage medium for programs. And opens the doors to a whole new generation of non-volatile memory applications.

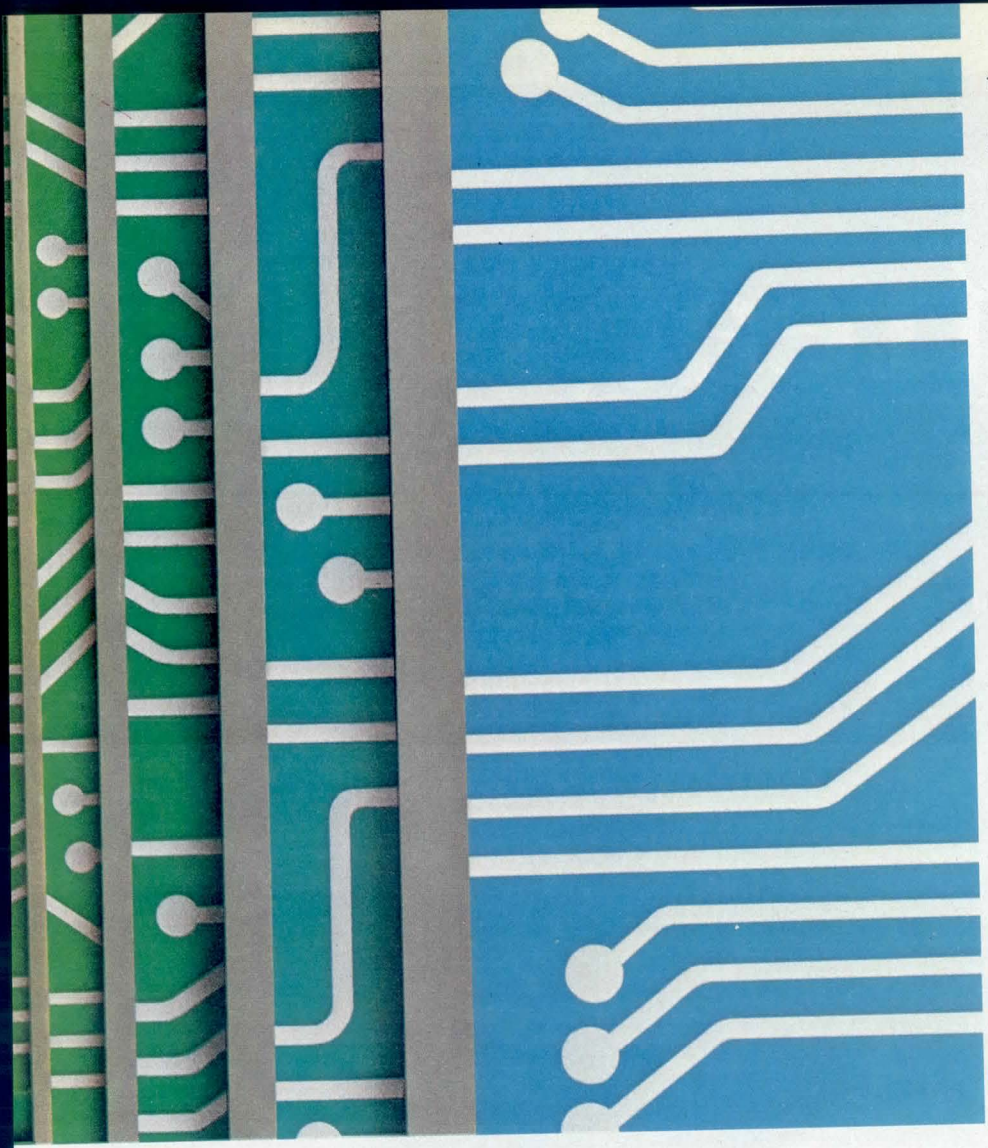
For systems smart enough to learn from experience

The 2816 E²PROM will revolutionize microprocessor system design. Now systems can be dynamically reconfigured—without human intervention. Consider the possibilities.

In industrial process control, equipment can be self-calibrating; machine tools, self-adjusting. In military and commercial aircraft, flight coordinates or radio frequencies can be changed remotely. In retail stores, point-of-sale terminals can have pricing tables updated instantly. In harsh industrial and manufacturing environments, programmable robots can make use of self-diagnosing/self-correcting feedback loops. The



Pin compatibility of Intel's 2716 and 2816



closed the design doors.

potential for convenient, low-cost system reconfiguration is enormous, for both OEM and end-user alike.

An exponential increase in design options

What are the E² advantages to designers? First, reprogramming flexibility. The 2816 can be reprogrammed electrically in the field, without interrupting in-service equipment operation. Or it can be reprogrammed remotely, via telecom or datacom links. Thus saving the labor and system downtime costs usually incurred with changing code in the field.

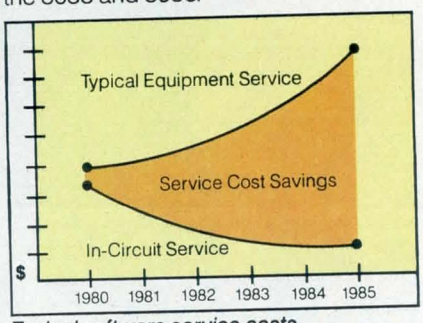
Second, the 2816 is both byte- and chip-erasable. Each byte can be rewritten up to 10,000 times, leading to simpler, more flexible systems. And reprogramming is fast: a single-byte program edit takes only 20 ms.

Third, the 2816 has the same reliability and data integrity as all non-volatile Intel memories. This reliability is a result of the 2816's floating-gate tunnel oxide (Flotox) cell structure and ten years of Intel experience in EPROM manufacturing. And unlike some other non-volatile ROMs, the 2816 does not require data rewrite to insure integrity. It will retain its data for at least 20 years—regardless of read frequency—without refreshing. And this kind of reliability—coupled with improved performance—will make the 2816 the industry standard for all program memories.

A match for today's micros

The 2816 is pin-compatible with the Intel® 2716. So it gives you all the microprocessor-oriented features that have made the 2716 the industry standard among EPROMs.

The 2816 also has the industry's fastest standard access time: 250 ns. And its two-line control eliminates bus contention between address and data lines. Plus it's low power. Thus changing existing concepts of memory storage and enabling designers to take full advantage of powerful new microprocessor capabilities, like those of the 8088 and 8086.



Typical software service costs

Remote reconfigurability in the here and now

Although the 2816 offers revolutionary capabilities, it's also the practical choice for microprocessor designs in the here and now. It's manufactured by Intel's proven HMOS*-E process. So you know it will follow the classical learning curve of a mainstream semiconductor technology.

To help you get started designing-in 2816s today, Intel provides full applications support and documentation. For instrumentation and control applications, we've already incorporated the E²PROM on an iSBC 88/40™ single-board computer.

We've closed the window; now you can open totally new design doors, and watch the world beat a path to your products. The 2816 E²PROM is available from stock through your local Intel distributor or Intel sales office. Or for further information, contact Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

*HMOS is a patented Intel process.

Europe: Intel International, Brussels, Belgium.
Japan: Intel Japan, Tokyo. United States and Canadian distributors: Alliance, Almac/Stroum, Arrow Electronics, Avnet Electronics, Component Specialties, Hamilton/Avnet, Hamilton/Electro Sales, Harvey, Industrial Components, Pioneer, L.A. Varah, Wyle Distribution Group, Zentronics.

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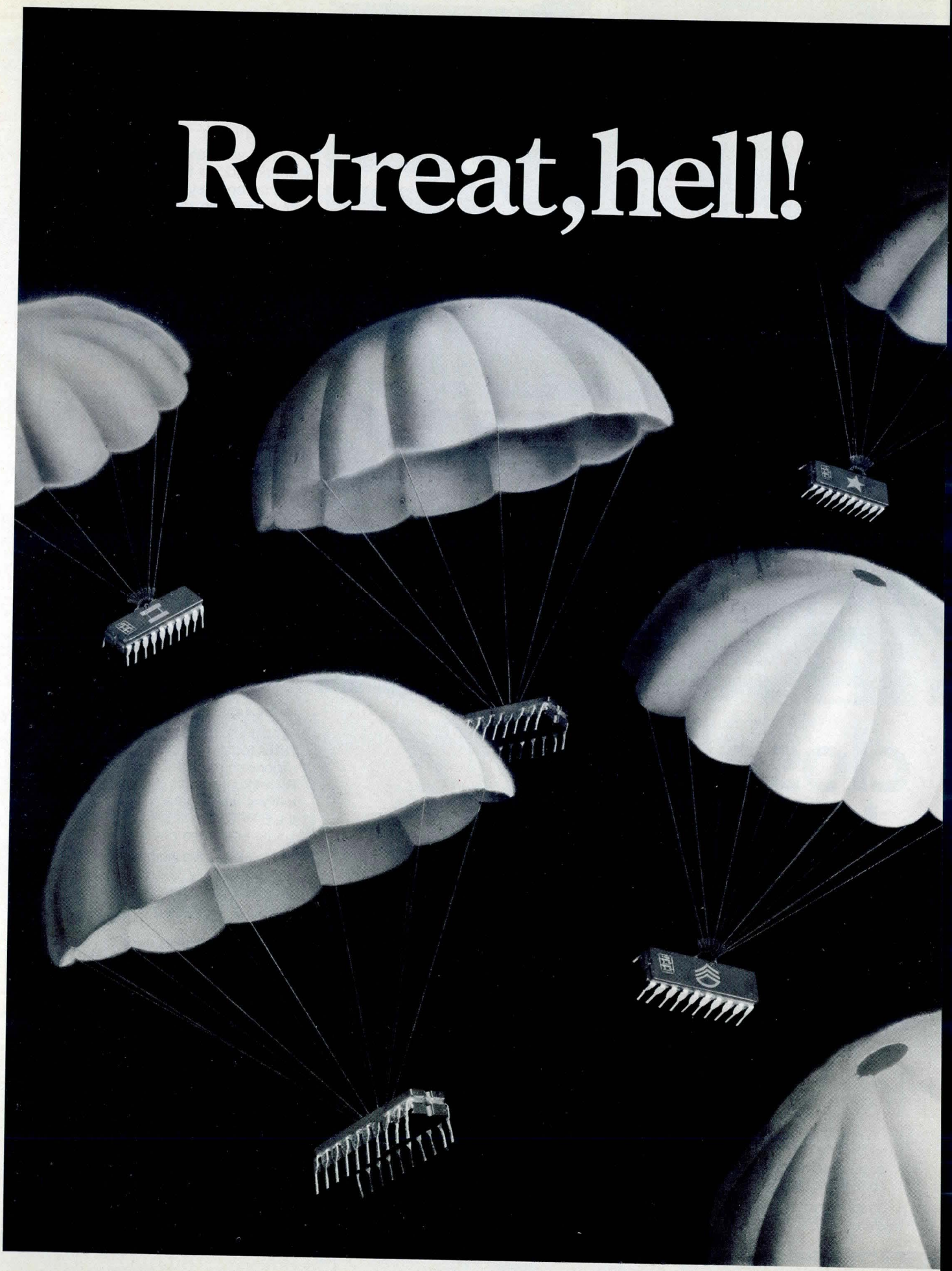
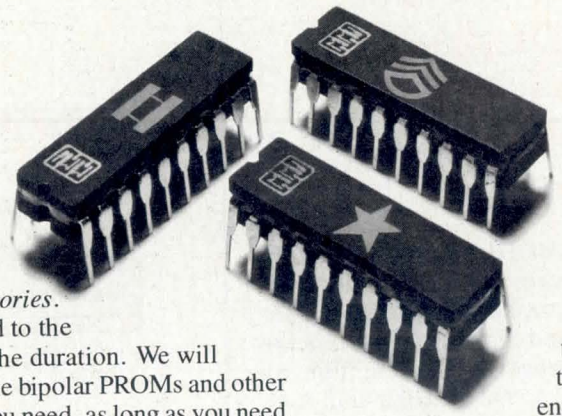

Retreat, hell!

While others pull out, Monolithic Memories supports and advances Hi-Rel.



Every time you turn around another Hi-Rel supplier is turning tail and running for cover. *Not Monolithic Memories.*

MMI is committed to the military market for the duration. We will continue to supply the bipolar PROMs and other integrated circuits you need, as long as you need them, made to military standards or your own specifications.

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For your complimentary copy of the Hi-Rel brochure and more information on our complete military line, contact your local Monolithic Memories stocking distributor or sales representative. Monolithic Memories, Inc., 1165 East Arques Avenue, Sunnyvale, California 94086.

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Monolithic Memories MMI

Digital Controls Govern Cameras and Displays in Automated Film Making

The production of film for television and motion picture applications has become an increasingly complex operation, involving sophisticated digital controls. An example of this kind of control is seen in the production of visual sequences on 35-mm film by Robert Abel and Associates, 953 N Highland Ave, Los Angeles, CA 90038.

Two different modes of operation are carried out at this studio. One involves digital control of camera motions during filming, the other the motion of images on a display screen for previewing subsequent filming sequences or for direct filming of the display with a fixed camera. (See Fig 1.)

Programmed Camera Motions

Camera motions are programmed on a minicomputer with 256k bytes of main memory and 532-ns effective cycle time, the PDP-11/60 from Digital Equipment Corp (DEC), 146 Main St, Maynard, MA 01754, utilizing a user developed applications software package called CAMCON (camera control), under supervision of the resident operating system RSTS/E (resource sharing, timesharing/extended). CAMCON allows the programmer to interpret required camera angles and distances as a series of sequential camera motion commands, keyed to specified film frames. The files that are generated by programmers at the timeshared VT-100 terminals of the minicomputer are stored on a model 440 floppy disc drive from Data Systems Design, 3130 Coronado Dr, Santa Clara, CA 95051. Located in a camera controller cabinet, this drive utilizes two dual-density, single-sided floppies of 0.5M capacity each.

Sharing the same cabinet as the disc drive is a single-board DEC LSI-11/2 microcomputer, which is half the width (double-wide rather than quad-wide) of the original LSI-11 from the same manufacturer, and, as employed here, includes 64k bytes of RAM. Using an RT-11 operating system, this computer reads the CAMCON disc file and also is accessible to operator intervention via a DEC VT-52 terminal. It then transmits commands to two control units, one of which governs the actions of stepper motors that move the camera, while the other governs actions within the camera relating to shutter operation and film advance.

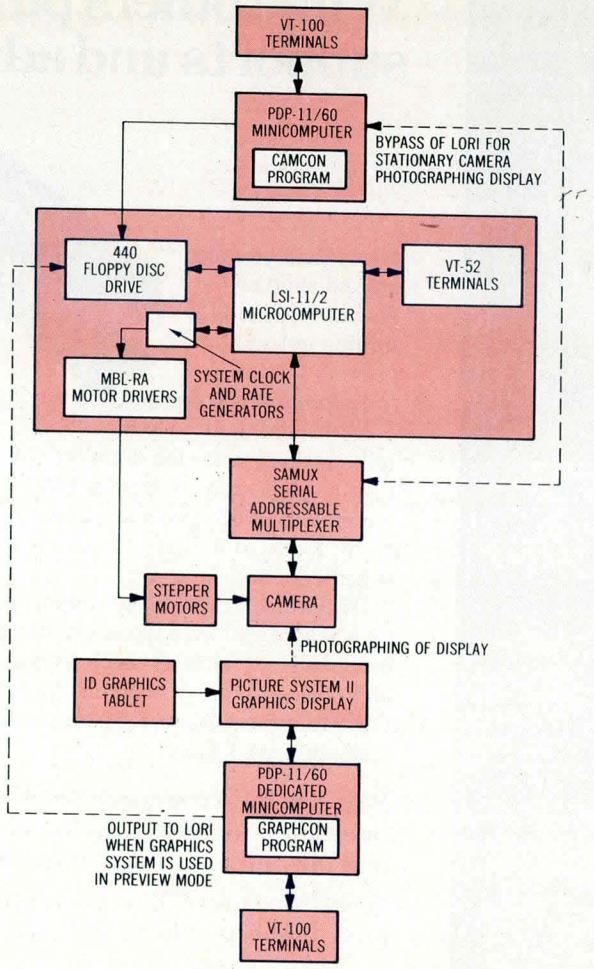

Fig 1 Film production systems. Camera photographs either real-world objects (with camera motions directed by CAMCON software) or display screen. When photographing objects, CAMCON program is entered into minicomputer and is stored on floppy disc drive to be read and utilized by microcomputer. When photographing screen, graphics system operates in conjunction with dedicated minicomputer to provide 3-dimensional moving image with variable orientation and magnification. In either case, serial addressable multiplexer interfaces with interior camera functions

The stepper motors receive their commands from stepper motor drivers. These bilevel drivers are implemented as 16 boards in the camera controller cabinet, one for each of 16 motors. The boards are the DBL1028RA from Anaheim Automation, 910 E Orangefair Lane, Anaheim, CA 92801, a custom version that provides a half-stepping option, thereby avoiding motor resonances.

A rate generator system, built according to an in-house design, receives commands from the microcomputer, and then issues rate and direction pulses to the motor driver. Receiving these pulses via

(continued on page 78)

OPTO 22 I/O MODULES

Of Course Opto 22 Has Buffered I/O Modules!

And High Voltage DC Modules
And True Normally Closed Modules
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Isn't this what you expect from Opto 22?

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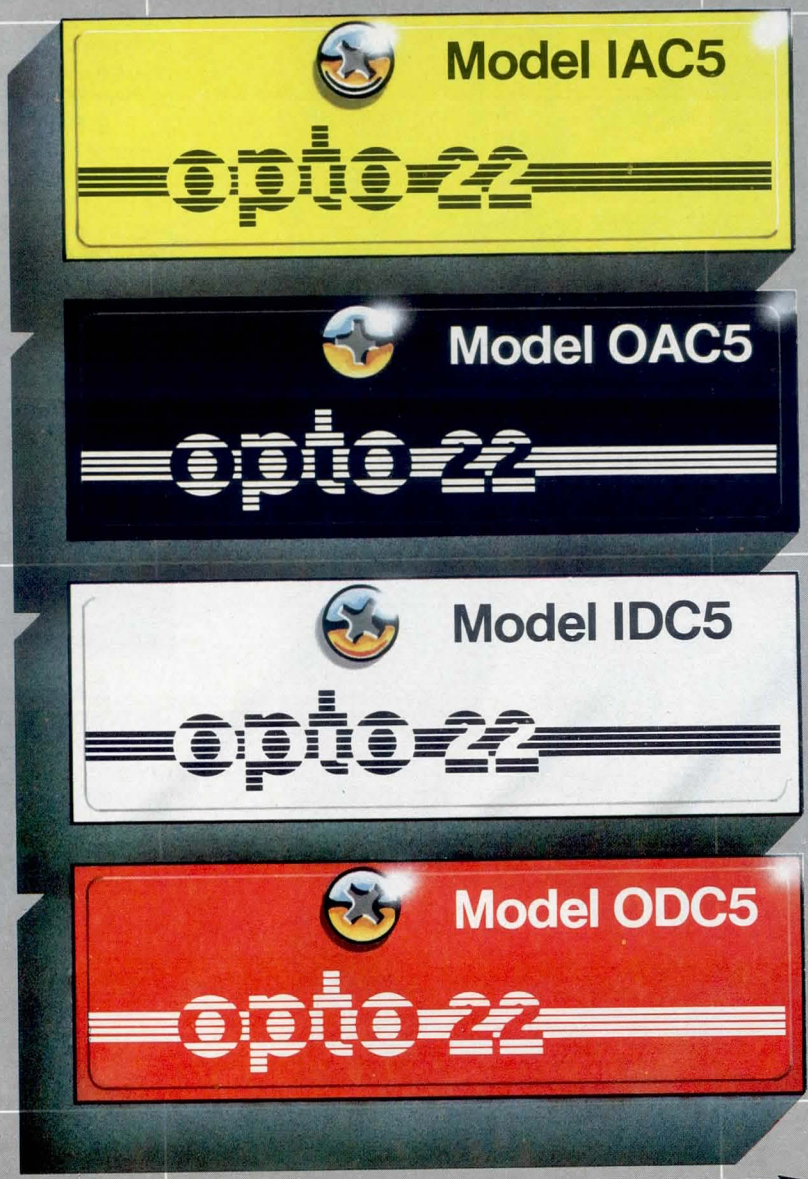

.6 Inches

Depth:
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1.7 Inches

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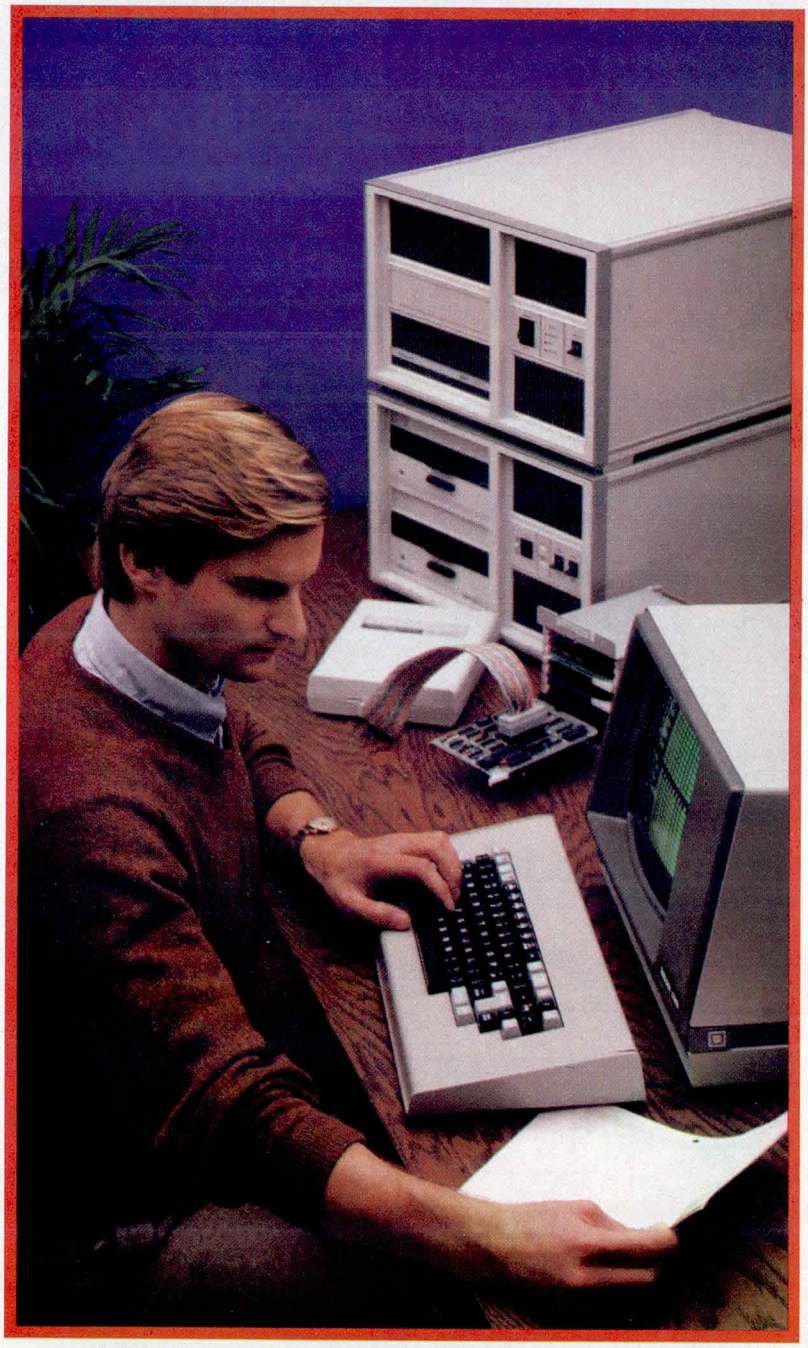
16 bits of information



1. Self-contained and upward compatible. The 8550 Microcomputer Development Lab is the single-user member of the new 8500 Modular MDL Series, which also includes the 8560 multi-user system and the 8540 Advanced Integration Unit for the host computer environment. The 8550 is a complete microcomputer design tool, covering both software development and integration into the prototype. The 8550 can also be used as a station on Tek's forthcoming 8560 multi-user system.

2. Real-Time Emulation. Takes the concept of emulation to a new performance level. Advanced circuitry eliminates the need for wait states during program execution and debugging. The emulator processor now functions in real-time, with its operation totally transparent to the user.

3. Multi-Vendor Chip Support. The 8550 MDL supports 26 chips in all. The broadest support available anywhere, covering a wide range of vendors. With microcomputers as well as microprocessors. The ultimate in design flexibility.

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on the new 8550 MDL.

4. 16-bit Support. You'll be able to choose from an entire new generation of 16-bit processors. Tektronix has the high performance tools to make it possible. Assembler support is available now for the 16-bit chips listed below. The TMS 9900 and SBP 9900 are fully supported with emulation today. Real-Time Emulation and Pascal support will be available in stages for the 68000, Z8000 and 8086 beginning the third quarter of 1981.

68000
Z8000
8086
TMS 9900
SBP 9900

5. 16-bit Trigger Trace Analysis. Gives you highly sophisticated triggering ability for selective snapshots of full-speed code execution on the prototype bus. Up to four data acquisition triggers can be combined in a wide variety of ways. Bus cycle resolution to 8 MHz.

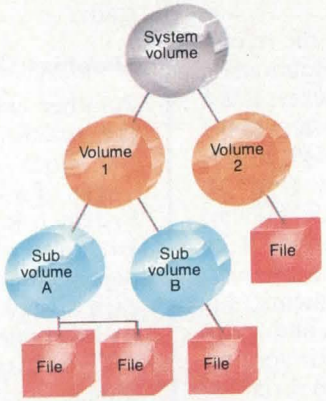
6. 8-bit Support. Besides the most up-to-date microprocessor coverage, you can also take advantage of extensive 8-bit microcomputer support. All 8-bit chip support includes real-time emulation.

6800	**8048**	**3870**
6802	**8039**	**3872**
6808	**8039-6**	**3874**
Z80A	**8035**	**3876**
8080A	**8021**	**F8**
8085A	**8022**	**1802**
8049	**8041A**	**6500/1**

7. 8-bit Real-Time Analysis. An optional Real-Time Prototype Analyzer lets you extract both bus and hardware logic at full operating speeds. You capture 48-bit words for storage in a 128-word memory. Two triggers for precise data acquisition.

8. Split-Bus Architecture. The 8550 uses one processor and bus for system operation, and another for real-time emulation. This architecture assures that the emulator processor is denied access to system memory, preventing the possibility of a system crash during prototype program execution.

9. Tree-Like File Structure. Combines ease of use, rapid access and in-depth organization. Allows files to be arranged in a predetermined hierarchy that best supports your current situation. A flexible tool that supports filing situations from very simple to extremely complex.



10. Advanced CRT-Oriented Editor. Gives you the quickest path possible to perform many editing operations. Lets you use screen-oriented editing as well as line-oriented editing. Up and down scrolling capabilities give you a total window on all of your code.

11. Macro Assembly. The most powerful assembler software available today in a development system. Lets you employ user-defined constructs and library resources. A conditional assembly feature allows sophisticated user manipulation of code at assembly time.

12. Pascal Compiler. Available in true compiler form, producing executable object code. Pascal's structured format allows a modular approach to programming. With extensions designed specifically for microcomputer development, Tektronix Pascal is ideal for the "top-down" method of product development.

13. MDL/μ Compiler. Tektronix' advanced form of Basic, with many extensions for microcomputer development. Often the quickest route from concept to fully developed code.

14. Transportable Emulators and Software. If you need to expand to a multi-user design environment, your 8550 can be incorporated as a workstation in an 8560 multi-user system. Source code and emulator modules can be readily transferred to the Tektronix 8560 system. If you move to a host environment, your 8550 emulator modules are totally compatible with the new Tektronix 8540 Advanced Integration Unit.

15. Worldwide Service. For service support, 36 centers around the globe. You get fast on-site service no matter where you are — without waiting weeks for parts or repairs.

16. Full Tektronix Support. Training, documentation, applications engineering. Nobody does it like Tektronix. An entire series of classes on microcomputer design, from high-level language to hardware/software integration. Applications engineers are available worldwide to assist you.

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optically isolated inputs, the driver responds by signaling the stepper motor to rotate through a 0.9°/pulse half-step, 400 pulses being required to take the motor through a complete revolution. By providing a sustaining voltage of 5 V and a high voltage of 40 V,* this driver's bilevel operation eliminates the need for large dropping resistors. When the motor steps and the operating phase current level is reached, the high voltage level is turned off and the current level is sustained by the low voltage supply. The lower voltage energizes the motor at standstill (0 steps/s). When the motor is stepping, the high voltage drives the current into the windings, supplying more of the required current as the stepping rate increases.

The second control device operated by the microcomputer is an input/output (I/O) device mounted on the camera box. A serial interface multiplexer, it is a specially adapted SAMUX 1 from Opto-22, 15461 Springdale St, Huntington Beach, CA 92649, that is ordinarily available as a single board (Fig 2). However, size limitations [packaging in a 19″ (48-cm) wide box] required that, for this application, it be provided in a 2-board configuration. One of these boards contains the microcomputer elements, including a Motorola 6802, 128 bytes of RAM, and a 2716 EPROM that is programmed by the user for specific functions required. The second contains 16 serial industrial I/O drivers that interface directly with the camera.

A 5-bit command word from the LSI-11/2 directs the SAMUX to send commands to the camera, directing its internal mechanical operations such as shutter cap open/close, film advance/rewind, running the main shutter motor forward/reverse, and putting the camera box on- or offline. Sensors detect any irregularities in the camera's state, such as film buckling, and return this information to the microcomputer for program interruption and the issuing of an alarm.

The entire system contained within the camera controller cabinet, including microcomputer, disc drive, stepper translators, power supply, and software operating system, is designated as LORI (latent-image optical recording instrumentation). Its capability to interpret disc file commands or to operate in direct response to keyboard commands provides a speed and efficiency in filming operations estimated to reduce filming time and costs by an order of magnitude from previous manually controlled operations.

Graphics Display

Another entire mode of operation is carried out in the studio, in which there are no camera motions. In this mode, the motion is simulated on the display screen of a strokewriter CRT graphics system, Picture System II from Evans and Sutherland, 580 Arapeen Dr, Salt Lake City, UT 84100. Two completely independent graphics systems are utilized in the studio, each hosted by a separate dedicated PDP-11/60, using an RT-11 operating system.

These display systems can be used to preview later filming sequences, or the screen can be photographed directly. When photographing the screen, the camera still receives commands from a SAMUX with regard to mechanical events within the camera box, but since there are no camera motions, the camera controller is not used and the SAMUX receives its commands

*Current level is a function of motor rating.

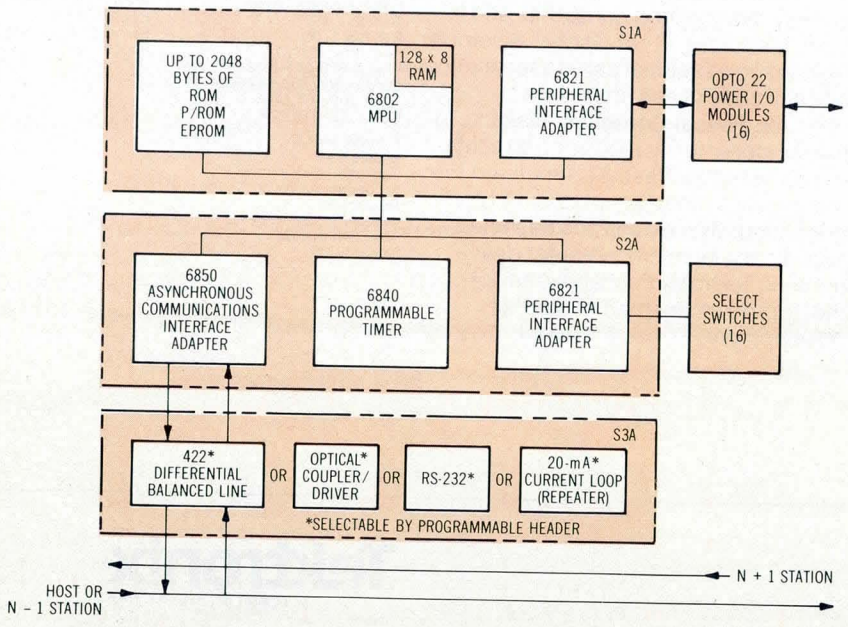
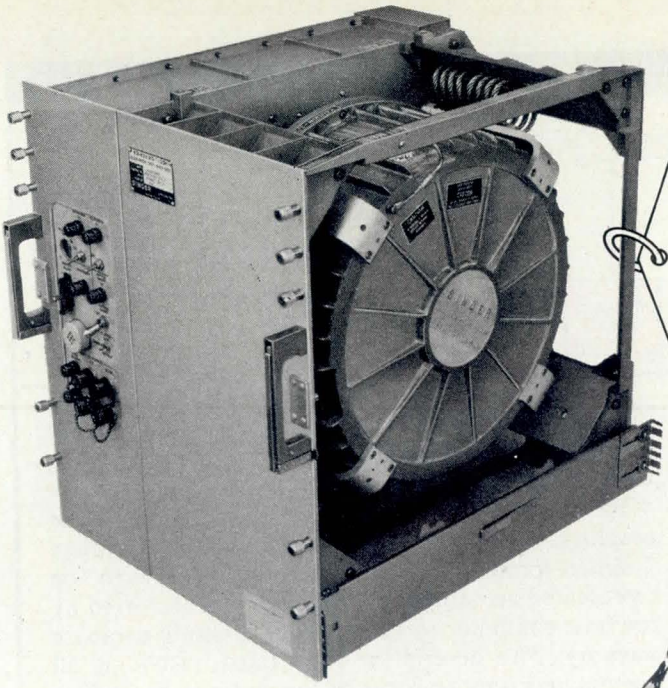


Fig 2 Block diagram of SAMUX 1. Logic modules consist of S1A (microprocessor and memory), S2A (timer and UART), and S3A (communications), while 16 I/O modules include ac-input, ac-output, dc-input, and dc-output types. For this custom application, logic modules are on one board, I/O modules on another



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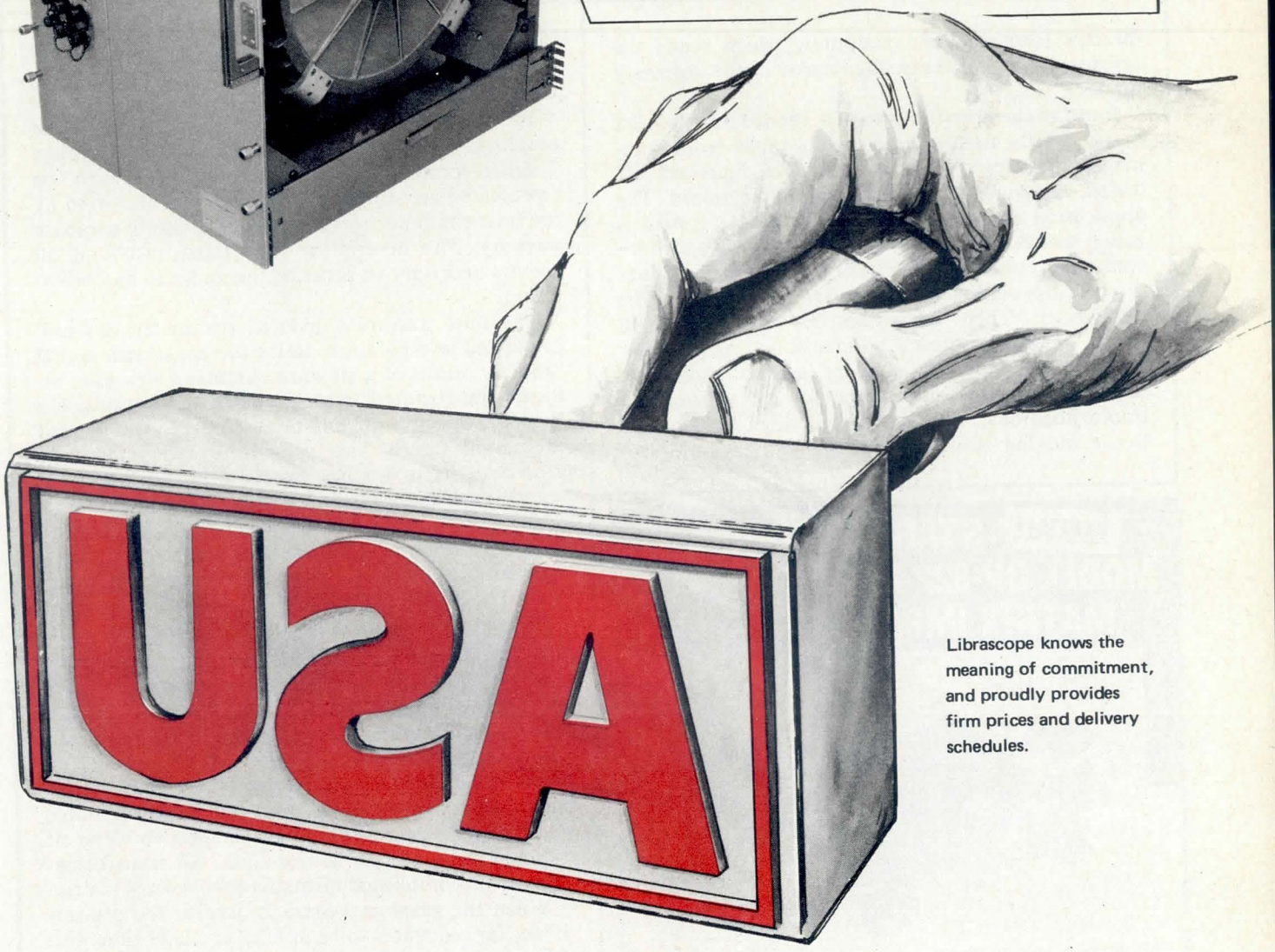

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The RD–433 Militarized Mass Memory

has been granted official **Approved for Service Use** (ASU) by the U.S. Navy. ASU means that the equipment is fully qualified, and assures the availability of logistics, software, and training support within the Navy. Extraordinarily reliable, the RD-433 is operational in the TACINTEL system aboard Naval ships at sea. TACINTEL is one of the largest communication systems in the Fleet Satellite Communications program. Other equally reliable Librascope Militarized Mass Memory Subsystems are used in the Navy's TRIDENT Integrated Radio Room and BQR-24 Sonar Systems, and on the U.S.C.G's WMEC-270 Cutter for command and control.

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CIRCLE 49 ON INQUIRY CARD

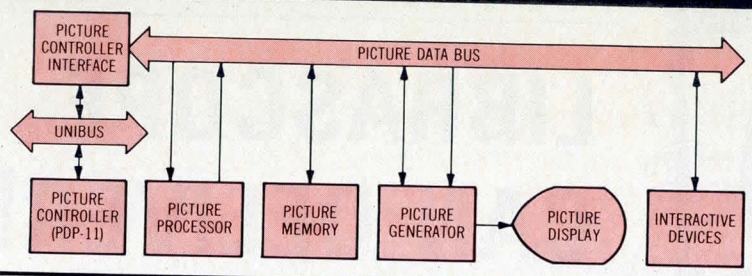


Fig 3 Picture System II. Application program and data base reside in picture controller. Picture parameters are read by picture controller from interactive devices, interpreted by user's program, and used to modify display file

directly from the minicomputer, which reads the previously generated disc file to provide the necessary inputs.

Input to the graphics system is carried out via a 3 x 4′ (90 x 120-cm) ID series graphics tablet from Summagraphics Corp, 35 Brentwood Ave, Fairfield, CT 06430, and via a DEC VT-100 terminal keyboard. The application software utilized on the host system is called GRAPHCON, a superset of CAMCON, which includes a graphics package. The programmer outlines three orthogonal views of the figure or figures to be represented. Then, the parameters are keyed in to define initial position, 3-dimensional orientation, and magnification of the figure, and corresponding sets of parameters are entered for a few later key frame positions. The system will then present the figure moving through these sequential configurations, with interpolated positions, orientations, and magnifications providing a continuously moving visual image.

Based on the orthogonal views entered onto the graphics tablet, the coordinates for a complete 3-dimensional description of the object to be represented are stored in disc files and transferred by the host computer to the graphics system's database memory. This description stays fixed, providing all vectors necessary to generate the image in any orientation.

The host transmits updated parameter sets and calculated interpolations to the picture system in real time, by means of a 16-word command string, to indicate the required sequence of configurations. On the basis of this input and on the fixed coordinates of the initial figure, also provided by the host, the graphics system applies matrix transformations to specify each successive video display. Two sections of RAM in the graphics system operate in alternating modes. While one is storing the current display configuration, the other is receiving the next configuration. The result is a moving image of the object or object set to be represented.

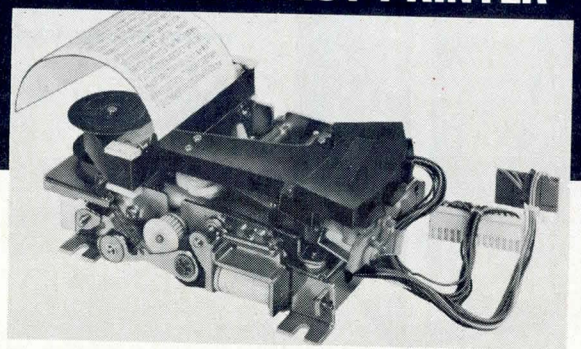
A display using N-dimensional data requires N words of data (in this application, three) to store coordinate values. Display screen size is 21″ (53 cm) square. Features include translation in any direction, rotation about any axis, scale with respect to any linear dimension, image clipping, zooming, and a capability for multiple viewports. The system is able to display hardware-computed perspective views of 3-dimensional objects in real time. All transformations are accomplished through use of a 4 x 4 matrix.

When the graphics system is used in the preview mode, for sequences to be utilized at a later time with a moving camera, data generated by GRAPHCON can be transferred to a disc file. From there they are utilized by LORI in filming with a movable camera, as previously described.

Summary

Digital controls enable this system user to generate either camera motions or moving images in the preparation of film sequences. Instruction sets generated by programmers working interactively with a host computer are subsequently fed to the camera or graphics system in a realtime filming sequence to generate a wide range of visual effects with considerable facility.

NEW! STAR MICRONICS MODEL DP-822 MINIATURE DOT MATRIX IMPACT PRINTER



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Compare Morrow Designs' DISCUS™ M26™ hard disk systems to any system available for S-100 or Cromemco machines. First, compare features. Then, compare cost per megabyte. The M26 works out to under $200 a megabyte. And the M10 is about half the cost of competing systems.

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The M26 and M10 are sealed-media hard disk drives. Both S-100 controllers incorporate intelligence to supervise all data transfers through four I/O ports (command, 2 status and data). Transfers between drives and controllers are transparent to the CPU. The controller can also generate interrupts at the completion of each command ...materially increasing system throughput. Sectors are individually write-protectable for multi-use environments. North Star or Cromemco? Call Micro Mike's, Amarillo, TX, (806) 372-3633 for the software package that allows the M26 and M10 to run on North Star DOS. MICAH of Sausalito, CA, (415) 332-4443, offers a CP/M expanded to full Cromemco CDOS compatibility.

Morrow Designs' 26 megabyte hard disk system: $4,995.

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Mult-I/O is an I/O controller that allows multi-terminal and multi-purpose use of S-100 and Cromemco computers. Three serial and two parallel output ports. Real time clock. Fully programmable interrupt controller. Designed with daisy-wheel printers in mind. Price: $299 (kit), $349 assembled and tested.

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Look to Morrow for answers.

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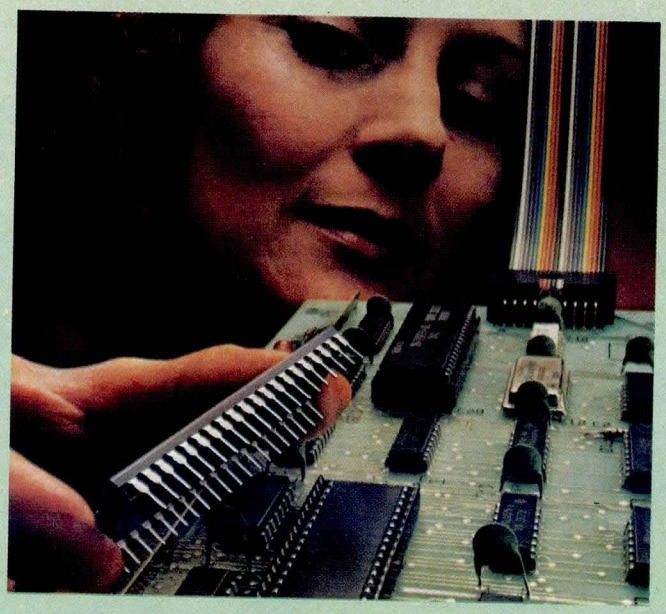
CIRCLE 51 ON INQUIRY CARD

We can't overstress the benefits of our socket's precision contact.



That's because AMP DIPLOMATE sockets' anti-overstress design prevents the major cause of socket failure. And at a cost-effective price.

DIPLOMATE sockets are available with the widest choice of features in the industry today. You can choose between .175" and .160" in profiles and solid or ladder housing construction. Our designs feature large contact target area for machine insertion, closed bottom to prevent solder contamination, and leg retaining detents to help increase productivity to meet your design needs. There are even MIL-S-83734 approved types.

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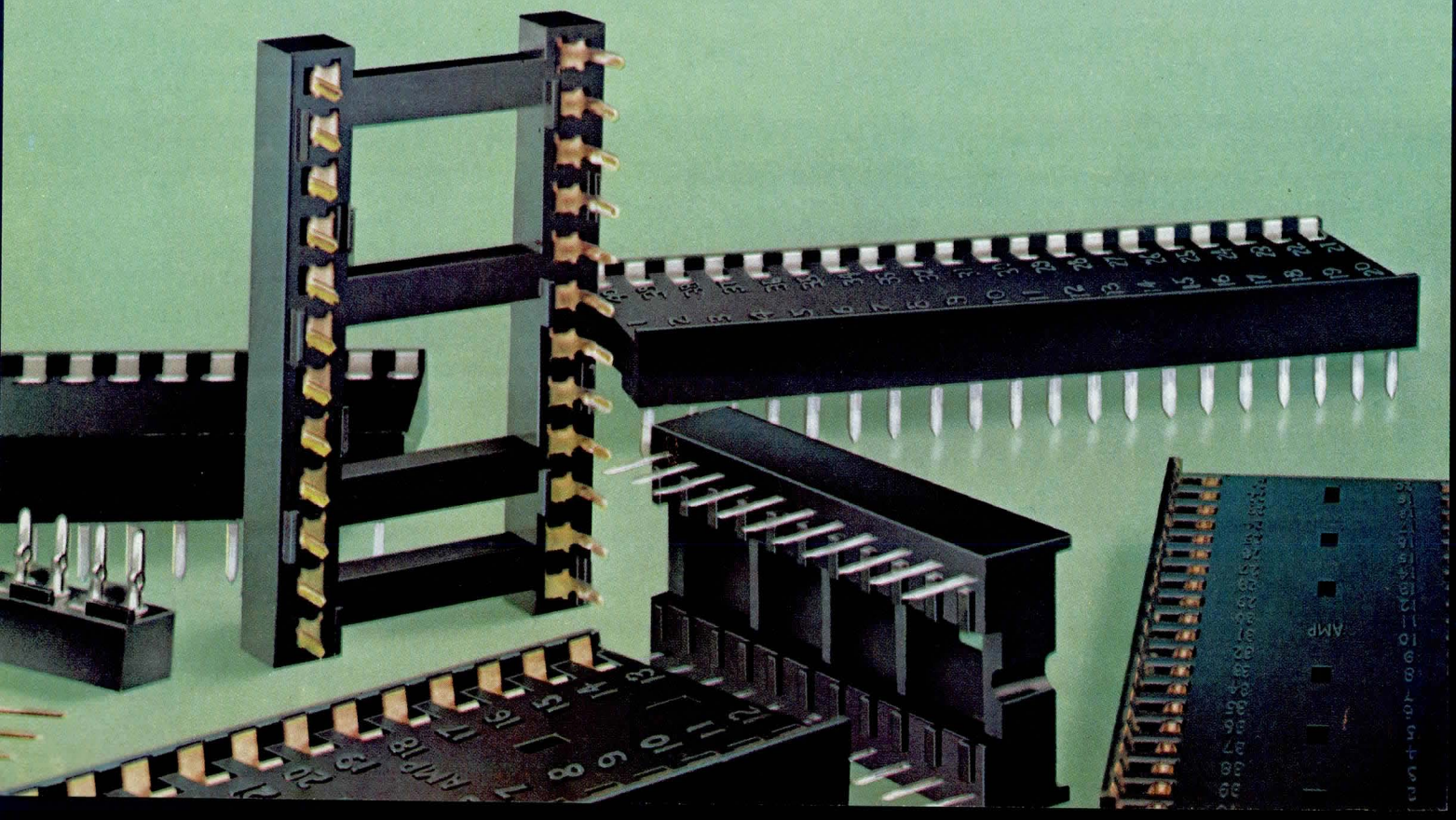


AMP Facts
for DIPLOMATE Sockets .175" Profile

Performance Characteristics

Physical

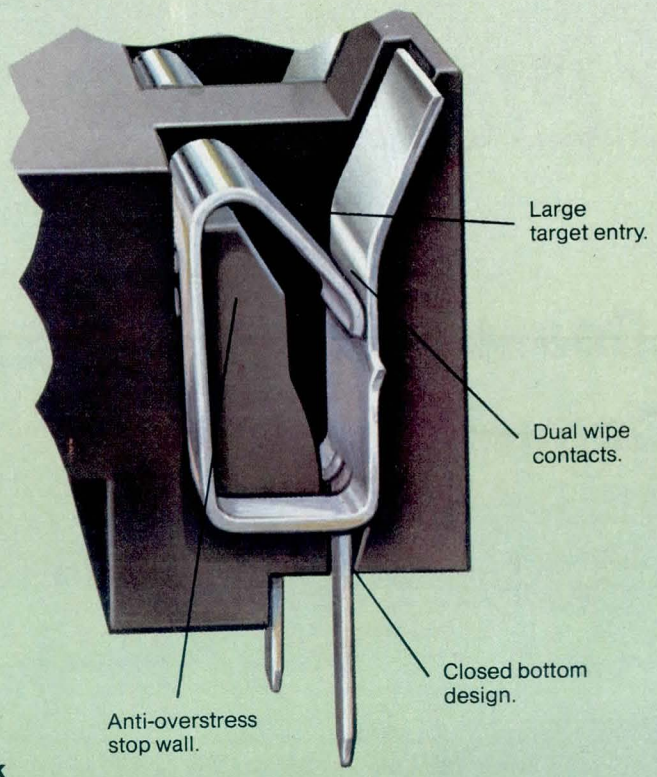
Engaging force: 340 grams max. (0.13) [0.33] pin)
Separating force: 14 grams min. (.008 [0.20] pin)

Electrical

Rating: 250 VAC
Contact resistance: 20 milliohms max. initial, 30 milliohms max. after test
Dielectric withstanding voltage: 1000 VRMS min.
Insulation resistance: 5000 megohms min.
Capacitance: 1 picofarad max.

Environmental

Operating temperature: −55°C to +105°C (tin plate)
Vibration: 10-2000-10 Hz in 20 minutes at .06 [1.52] or 15G's for 3 sweeps in each of 3 axes.
Shock: 100 G's, sawtooth waveform, total 6 shocks.



For a free sample, call the AMP DIPLOMATE Socket Information Desk at (717) 780-8400.

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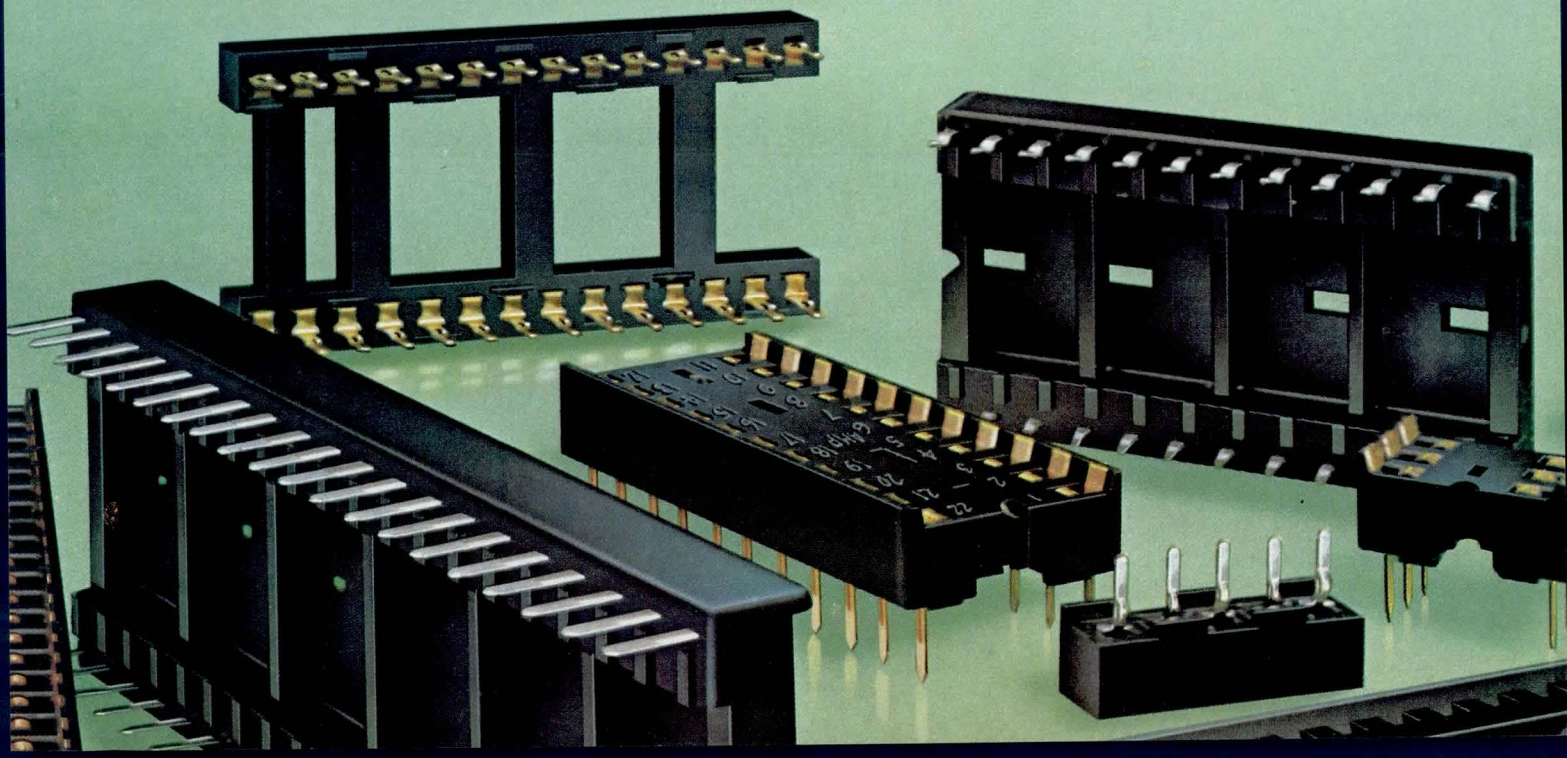
CIRCLE 10 ON INQUIRY CARD

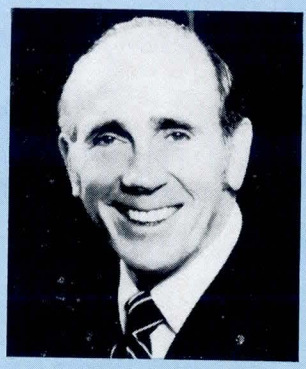


Electro/81

East Coast Electronics Exhibition And Convention

New York Coliseum and Sheraton Centre Hotel
April 7 to 9, 1981

Hsu Chang
Program Chairman



Harry J. Gray
Keynote Speaker

All phases of Electro/81—professional program, workshops, keynote address, purchasing conference, and exhibition—are concerned with the "Pathway to Productivity," theme of the largest Electro since the convention was formed as a merger of the old New York City IEEE Intercon and Boston Nerem meetings. Alternating annually between the two cities, Electro will be in New York City this year. The professional program will be presented at the Sheraton Centre Hotel (formerly the Americana), while the New York Coliseum will house the exhibition, which is to include a special display of small computers for engineering and business applications.

Although Electro itself will run from Tuesday, April 7 through Thursday, April 9, a 2-day special-fee workshop on Technology Forecasting will begin on Sunday, April 5, and two special tutorial workshops sponsored by IEEE's METSAC (metropolitan New York City electronics) sections will be conducted on Monday. In addition, both the purchasing conference and keynote luncheon will be held on Monday.

Professional Program

Nearly 40 scheduled sessions, with approximately 160 individual presentations, will be included in the professional program. Except for a few special sessions, blocks of four or five sessions will be provided three times each day: at 9 am, 12:30 pm, and 3:30 pm. (See final program to be distributed at Electro/81 for exact times and room assignments.) In addition, a presentation by Japanese and U.S. government and electronics industry representatives on "The New Relationship between American and Japanese Electronics Industries," covering objectives, operations, products, and problems, will be conducted on Wednesday evening.

Not surprisingly, program emphasis will be on three areas of technology that have proven interest among electronics professionals: data communications, microprocessors/microcomputers, and integrated circuits. Nine sessions (37 papers) will be devoted to communications, seven sessions (34 papers) to microprocessors, and six sessions (24 papers) to ICs. Of the other program areas of interest to *Computer Design* readers, three sessions (11 papers) will cover display technology, two sessions (9 papers) peripherals, and one session (4 papers) data acquisition.

(continued on page 88)

A FAMILY OF SOFTWARE-COMPATIBLE SMD CONTROLLERS FOR PDP-11 AND LSI-11

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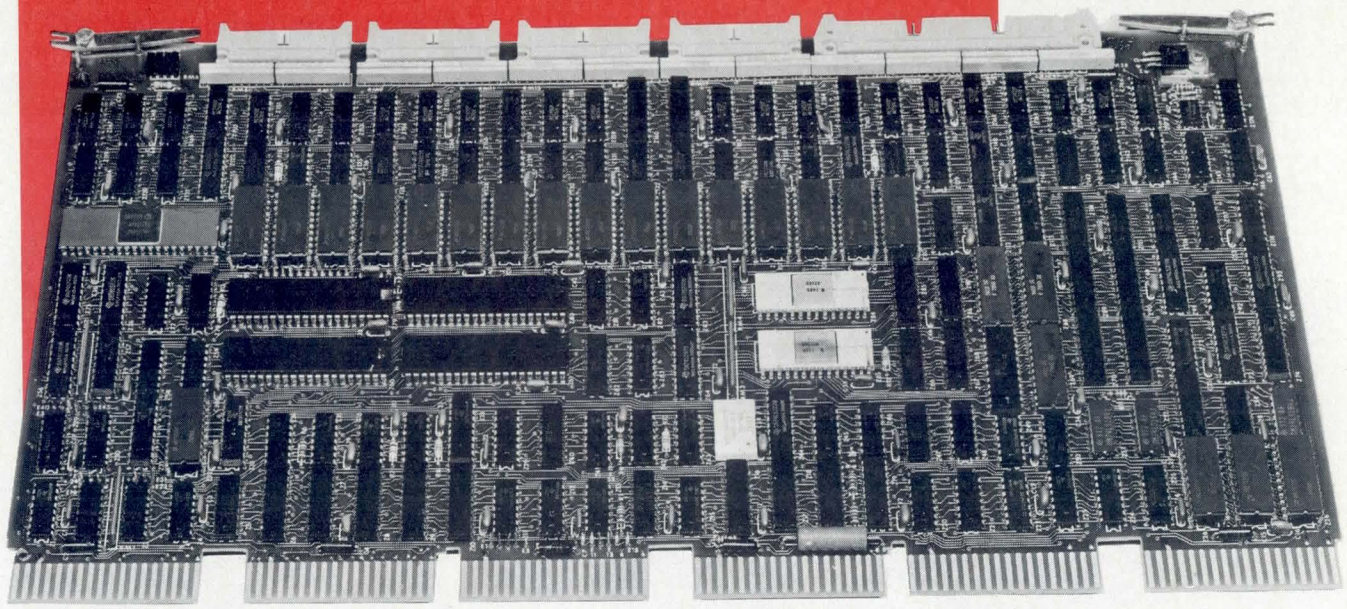

Now you can get all you want from a single family of DEC®-compatible SMD controllers for your PDP®-11 and LSI-11®minicomputers. All the features, all the performance, all the compatibility. And all available now, from Dataram.

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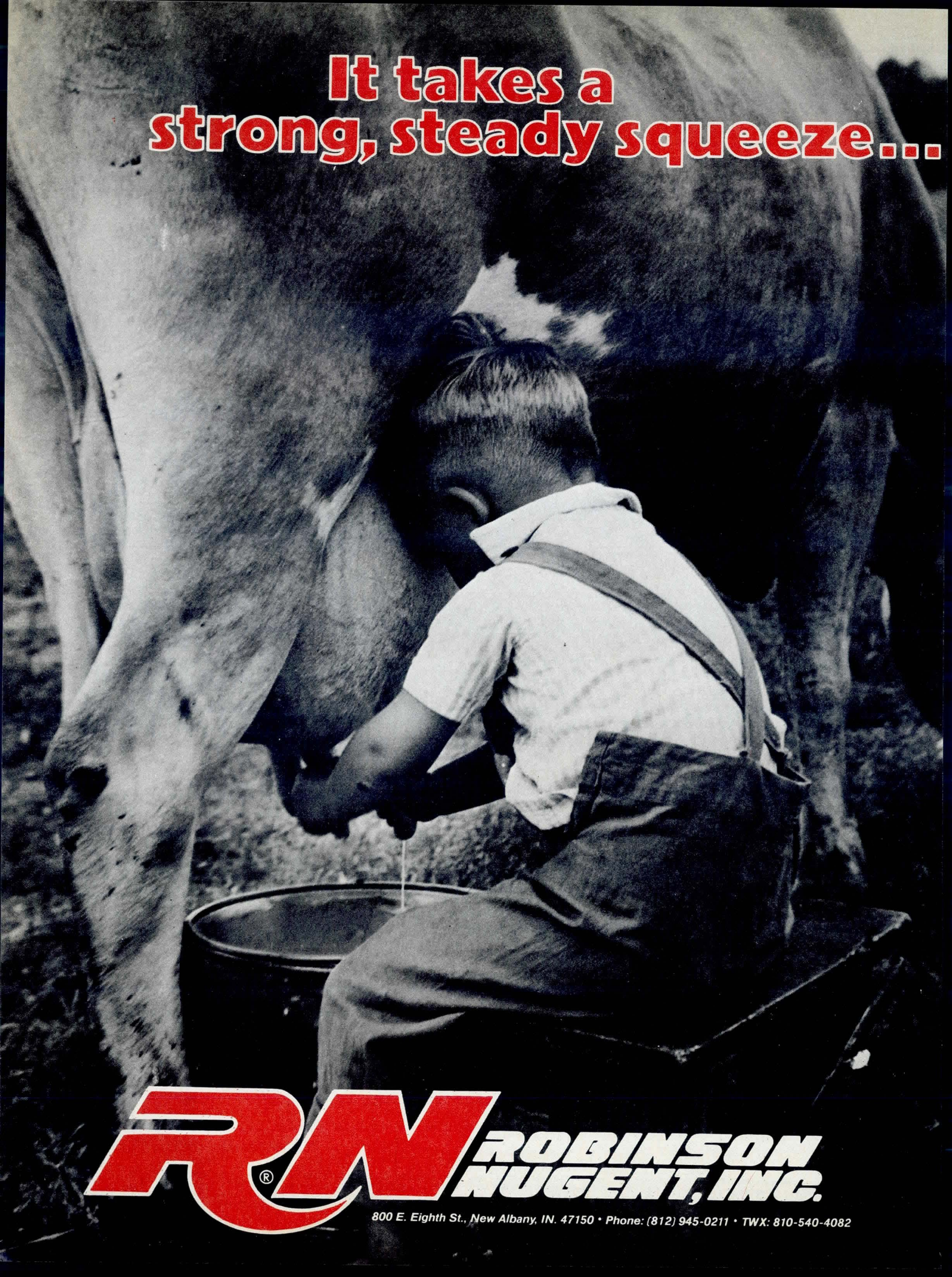
CIRCLE 53 ON INQUIRY CARD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strong, steady squeeze...
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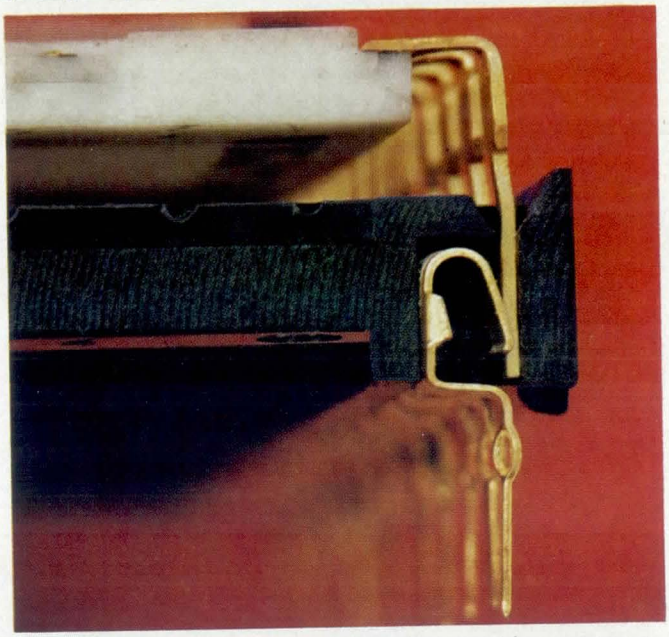
...to achieve GAS TIGHT RELIABILITY in a low profile socket



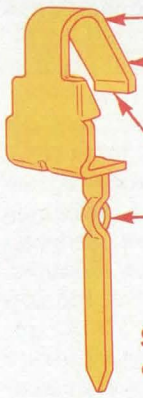
RN single leaf high compression contact provides maximum pressure against your IC lead.

You know the secret of gas tight reliability in a low profile DIP socket. It is the "squeeze" or force the contact exerts on your IC lead. RN single leaf high compression contacts exert a "normal force"* that is 4 to 5 times greater than conventional dual leaf contacts. Result? RN low profile ICL series sockets are MIL-SPEC qualified (MIL-S-83734) to meet the toughest gas tight performance standards in the world. You can't buy a more gas tight low profile socket—anywhere! And, our prices compare very favorably with any comparable socket.

*NORMAL FORCE means force at right angles to the IC lead.

MIL-S-83734 Environmental Test Data for ICL Series DIP Sockets

Test	Procedure	Results
Initial Contact Resistance	MIL-S-83734 Paragraph 4.7.15	R_C=7.0mΩ average
Corrosive Atmosphere	MIL-S-83734 Paragraph 4.7.16 10-25 ppm $(NH_4)_2S$, 4 hours	R_C=8.5mΩ average
Moisture Resistance	MIL-S-83734 Paragraph 4.7.14	$R_i \geq 10^{12}\Omega$
Thermal Shock	MIL-S-83734 Paragraph 4.7.13	No Damage
Mechanical Shock	MIL-S-83734 Paragraph 4.7.11	No Discontinuity
Vibration	MIL-S-83734 Paragraph 4.7.1	No Failures R_C=7.0mΩ average (final)
Socket Durability	MIL-S-83734 Paragraph 4.7.12 After 50 Cycles	R_C=7.8mΩ average



- Contact available in phosphor bronze, beryllium copper, with tin or selective gold plating.
- High compression contact design provides longer spring length for maximum pressure against IC lead.
- "Side-wipe" design meets flat, smooth side of IC lead for perfect contact.
- Self-lock lead holds socket firmly during wave soldering and prevents solder wicking.

Superior contact design

WRITE FOR COMPLETE DETAILS and latest RN catalog with full specs, dimensions and material data.

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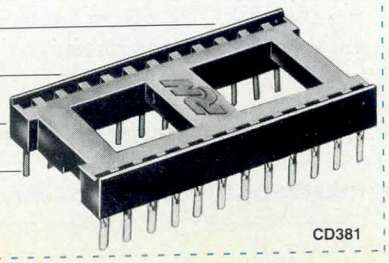
☐ Please send MIL-S-83734 Test Results



CD381

CIRCLE 54 ON INQUIRY CARD

Electro/81

Data Communications

Theoretical aspects of communications networks, covering both hardware and software, will be discussed in session 10, "Computer Communications: Theory and Experience." Session organizers and speakers, all from Italy, will propose a theoretical framework for designing and implementing computer networks. They will discuss protocols, interfaces, general theory, mathematical models used with general theory, performance valuation, and architecture. Backup for this discussion will be session 28, "Computer Communications—The View from ICC '80," in which issues raised at the October 1980 International Conference of Computer Communications will be described by a panel of speakers. An open discussion will follow.

Three sessions will be devoted specifically to networks: 6c, "Contention Based Local Area Networks Implementation: Ethernet and NET/ONE"; 17, "Local Networks"; and 21, "Data Network Interconnection." Each will cover specific areas of networking, including architectural considerations; management; system applications; practical implementation; the evolving IEEE 802 standard; specific networks and their relevance to X.25, HDLC, and other protocols; and interconnection of various data networks.

Other data communications discussion will occur in session 3, "Stored Program Switching Systems—Perspective on Performance and Achievements," and session 7, "Trends in Communications Software." Speakers in the first session will review stored program control applications in telecommunication switching systems, with emphasis on initial problems, progress toward solutions, field experience, and new features, services, and economic advantages. In the second session, speakers will present overviews of system requirements specifications, software switching, software architecture, and distributed software in communication networks, with emphasis on historical perspective of the evolution of call processing and network communications.

Sessions 8a and 8b, respectively, will cover "Optical Fiber Communication Media and Components" and "Upcoming Fiber Optics Systems and Applications." The first group of speakers will discuss the optical elements involved in fiber optic communications systems and how the design of such systems differs from that of conventional systems. In the companion session, the theme will be future applications of fiber optics, including optical data links.

Microprocessors/Microcomputers

Because of a wide range of interest as well as the diverse areas worthy of discussion, the sessions in this category—although closely related—will cover many separate aspects. Session 1, "Innovations in Microcomputer Architecture," will examine the impact of single-chip computers, particularly the cost effectiveness of having memory and input/output lines on-chip; while session 11, "Programming Aspects of Single-Chip Microcomputers," will consist of a treatise on the increasingly important program and programmer efficiencies, with emphasis on program features that permit greater function sophistication.

Systems, from single- to multiple-board, will be discussed in session 5, "OEM Microcomputer Modules: Potential Configuration and Case Studies of Industrial Applications." Session 6a, "Advances in Microprocessor Memory Management Unit," will examine the operation and application of semiconductor memory management units, a recent innovation for microprocessor systems.

Other discussions in this general category will include session 9, "Techniques and Applications for Multiple-Processor System Design," which will investigate several techniques and applications for the use of multiple microprocessors or microcomputers to solve a common system design problem, with emphasis on bus structures and parallel processors. Session 23, "Low Cost Microprocessor Development Systems—How Low Can You Go?" will deal with the hardware and software capabilities of several low cost systems available for developing software; included in the discussion will be high level languages, emulation support, assembly language support, host level debug, and distributed network development stations, with particular attention to solving OEM board level system design problems. Availability of full-performance complementary metal oxide semiconductor microprocessors, increasingly desirable because of their low power requirements, is the subject of session 27, "The CMOS Microprocessor Era Is Here."

Integrated Circuits

ICs, as a general category separate from that of microprocessors, will be discussed in various sessions. Of particular interest will be session 2, "Highlights from ISSCC '81." Probably the most prestigious of IC related conferences, the IEEE International Solid State Circuits Conference is a forum not only for current advances but also for future state of the art. In this Electro session, highlights, developments, and trends for three divisions of IC technology—analog, digital, and other—as viewed by session participants at the February 1981 ISSCC will be summarized by organizers from that conference.

Very large scale integration (VLSI), an important phase of the technology even before all the problems of

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CIRCLE 55 ON INQUIRY CARD

LSI have been solved, is the subject of four sessions. Key to all of them, however, is session 20, "VLSI Technology: What Is It? What Is It Good For?" Impact of VLSI technological advances, lithographic techniques (optical, e-beam, x-ray) and their inherent chip complexity problems, and consequent design innovations will be reviewed in detail. Knowledge of these developments will certainly help attendees to understand other facets of the VLSI sessions.

Of currently available VLSI devices, the 64k random access memory is produced in the highest volume. Speakers in session 6b, "The 64k RAM," will discuss features, market, likely users, price, availability, suppliers, and test problems. Session 16, "New Developments in VLSI Gate Arrays," will explore the technology, design, cost, and applications of VLSI gate arrays using CMOS and IIL (integrated injection logic); and session 12, "Recent Developments in VLSI-CAD," will consider the ramifications of very large scale integration on the problems of computer aided design.

A product of IC technology, the speech synthesizer chip is discussed in session 24, "Components for Speech Processing: Present and Future." The coverage will include a tutorial introduction to the technology, present capabilities, voice output, speech processing, and speech recognition.

Other Sessions of Interest

Display technology is the subject of three sessions: 14 and 18, "Display Technology Review—Parts I and II," and 22, "Computer Graphics: What Is It? What Can It Do for You?" Within the discussion of the first two sessions will be ac and dc electroluminescent, various liquid crystal, CRT, ac and dc plasma, and flat panel displays. The third session will be an introduction to both scope and benefits of computer graphics.

Session 15, "Peripheral Techniques Advance as Fast as Microprocessors," will aid engineers in keeping up with the latest peripherals and I/O techniques for use with available microprocessors, while session 19, "Intelligent Peripheral Controllers in Systems Context," will explore the architecture, I/O capability, and software features of IPCs in a variety of system applications. "Data Acquisition in Special Applications," session 26, will focus on applications of data converters in areas requiring specialized approaches; the intent will be to provide users of data acquisition components with ideas that are helpful in unique data conversion applications.

Exhibition

An early prediction is that 40,000 electronics professionals will attend some or all portions of Electro/81. To accommodate them this year, for an Electro first, the exhibition will occupy three floors of the New York Coliseum (reminiscent of the not too distant past when all four floors and various side rooms were crowded with IEEE exhibitors). Nearly 500 companies will exhibit their products and services in approximately 1000 booths.

Exhibitors will be separated into four groups: instruments/instrumentation and control systems; production, packaging, and test equipment; components, microelectronics, and fiber optics; and mini/microcomputers and EDP peripherals. Color coded carpeting and aisle signs will guide attendees to each group.

Exhibit hours will be 9:30 am to 6 pm on Tuesday; 9:30 am to 7 pm on Wednesday; and 9:30 am to 5 pm on Thursday. Free shuttle buses will run between the Coliseum and the Sheraton Centre Hotel, beginning operation 30 min before the exhibition opening hour and ending 30 min after the closing.

Special Events

Basic principles of technology forecasting and forecasting methodologies will constitute a major portion of the technology forecasting workshop, to be held on the Sunday and Monday before Electro/81 officially begins. Other areas to be examined in this workshop will include applications, resources, and disadvantages of various forecasting systems. The fee for this 2-day event is $250. Workshop instructors will be John H. Vanston, Jr and Ralph C. Lenz, both of Technology Futures/Industrial Management, Austin, Texas.

Two METSAC section tutorial workshops will be held on Monday. One will cover fiber optics technology, including principles, theories, light sources and detectors, and systems applicatons. The other will deal with capabilities and advantages of Ada, the computer language that will be standard for all Department of Defense programs. Registration fees for each workshop are $150 for IEEE or ERA members and $175 for nonmembers; fees cover course materials, keynote luncheon, and registration for Electro.

The keynote luncheon will be held at noon on Monday in the Sheraton Centre Hotel. Keynote speaker will be Harry J. Gray, chairman of the board and chief executive officer of United Technologies Corp.

The theme of this year's All-Industry Reception will be "The Sidewalks of New York," celebrating the gaslight era of the Gay 90s. A $15 admission charge for the 6:30 to 8:30 pm Tuesday reception covers hors d'oeuvres, wine, beer, soft drinks, and two stronger beverages.

Registration

At the door registration for Electro/81 will be $10 for IEEE and ERA members, and $20 for nonmembers. Half-price registration for nonmembers is available from the Electro office, 999 N Sepulveda Blvd, El Segundo, CA 90245, as well as through a preview mailing to industry professionals. Free registration cards will be distributed by engineers at many northeastern U.S. companies and may also be obtained from exhibitors. □

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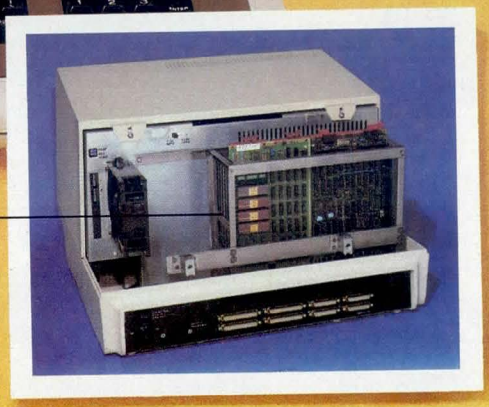

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CIRCLE 56 ON INQUIRY CARD

Products that talk.
The man-machine interface will never be the same.

Let's talk about speech capability. Voice synthesis products. From Texas Instruments.

The bright promise of products that think came closer to fulfillment in the 70s. The trend for the 80s is clear: Products that "talk."

Whether it's appliances, automotive consoles, transaction terminals, office systems, telecommunications, robotics or electronic toys and games, no other area of technology will have more impact during this decade.

Speech synthesis technology — pioneered by TI — portends a whole new generation of voice-prompting products. Products that will change the way you live and learn and work.

So, if you're designing new products with speech applications, talk to TI — the *only* total capability supplier with the experience and production-proven know-how to assure you of reliable speech products and services.

Let's talk technology

TI offers several methods of vocabulary analysis, dependent on your volume, versatility of application and voice quality desired. TI's Linear Predictive Coding (LPC) technique provides the highest quality speech reproduction because it's the only technique devised that models itself after the human vocal tract.

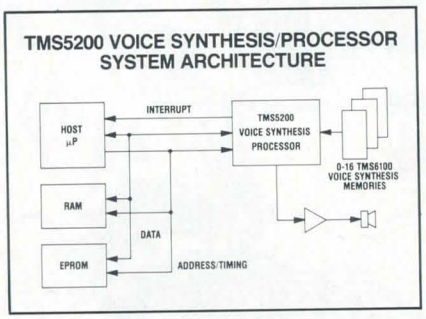
Define your vocabulary, consider your volume requirements, cost and development time, then talk to TI about your application.

Let's talk products

Choose from the industry's broadest, most cost-effective line of speech products. A growing line of integrated circuits, evaluation kits, OEM boards and a capability for the design and development of complete custom modules incorporating microprocessors, display and interface functions. A good example of our commitment to this technology: ROMs made especially for speech applications.

TI's LSI Voice Synthesis processors (VSP) and Voice Synthesis memories (VSM) are in volume production, now.

The TMS5200 single chip VSP produces high quality speech at a very low data rate (1200 bps), easily interfacing with 8 and 16-bit microprocessors. The on-chip FIFO buffer allows speech data to be stored in either the host microprocessor system, or off-line on bubble memory or floppy disk. Also, speech data may be stored in a custom ROM, such as the 128K-bit TMS6100. You can use TI VSPs with TMS6100 Series VSMs for storage of up to 3,000 words of speech.



The TMS5100 single chip VSP produces high-quality speech at data rates of 1200 bps and interfaces with 4-bit microprocessors. TMS5100 VSP directly addresses up to 16 TMS6100 VS memories for up to 30 minutes of speech.

For evaluation of TI's voice synthesis capabilities for 4, 8 and 16-bit microprocessors, complete speech evaluation kits are available for TMS5100 and TMS5200.

So, what are we talking about? We're talking about quality, flexibility, cost/performance effectiveness and right now delivery — only from the voice synthesis leader — only from Texas Instruments.

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For high-volume applications, user-developed vocabularies can be implemented on mask-programmed ROMs.

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Let's talk support

Like the development of production vocabularies at any of TI's Regional Technology Centers. Custom vocabularies can be synthesized at the RTCs at low cost with quick turnaround (so quick in some cases that you can walk out the door with your program) and delivered on EPROMs for use with either TI's TM990/306 speech board or TMS5000 Series VS processors.

And like tapping the resources of TI's word library where natural sounding speech is pre-recorded and readily available for specialized vocabularies.

And like an intensive one-day RTC seminar covering TI's Solid State Speech technology and its applications, including acoustics, phonetics, waveform analysis and LPC. Systems architectures as well as hardware and software design techniques and a demonstration of several speech products round out the day.

And like the Design Service assistance rendered by the RTCs for the application of cost-effective, state-of-the-art technologies to your specific product and program needs.

Let's talk now

About a total systems solution capability for voice synthesis technology. About low-cost, high-quality, quick turnaround Solid State Speech applications for your products.

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TRW CINCH CONNECTORS

CIRCLE 57 ON INQUIRY CARD

FUTURE DIRECTIONS IN COMPUTING

Extrapolating trends in critical areas of computer technology identifies paths in which computing will evolve

James R. Bell*

Digital Equipment Corporation
146 Main St, Maynard, MA 01754

Important developments are taking place in each of the areas of function, performance, ease of use, acquisition costs, operating costs, reliability, serviceability, and compatibility. By extrapolating trends in these areas, one can predict certain directions the evolution of computing will take in the next decade, and prepare to seize opportunities that the future will offer.

Function and Performance

Improvements in computer function and performance are fueled mainly by the rapid development of semiconductor technology. Processors illustrate this progress. The level of function in a computer system can be inferred from the amount of memory the system contains. (See Fig 1.) Main memory, today composed of semiconductors, follows the semiconductor technology trend

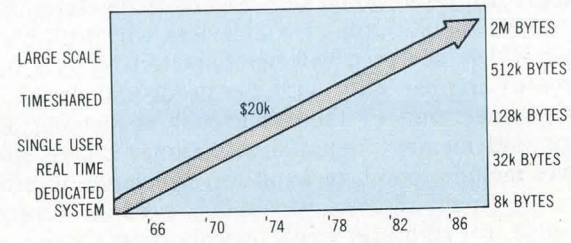

Fig 1 Greater function through semiconductor technology. Although it purchased few kilobytes of memory in 1965, $20k will buy several megabytes by 1985 (Adapted from Gordon Bell, 1975)

*Mr Bell is presently with Hewlett-Packard Co, 11000 Wolfe Rd, Cupertino, CA 95014

that yearly doubles the number of bits available on a single chip. The amount of main memory purchased per dollar increases each year. This increase in memory corresponds to an increase in function from small, dedicated systems to sophisticated, multi-user timesharing systems.

Decreasing semiconductor prices impact subsystems other than processors. Low cost memory permits construction of video terminals in which one bit of local memory corresponds to each dot position on the screen. Allowing a natural integration of graphics with text, these bit mapped terminals are further extendable to provide gray scale and color through additional memory bits. Adding features and intelligence to terminals makes good economic sense because it improves their cost/benefit ratio. Today's video terminals, using television technology, do not cost much more than television sets. Although terminal costs may continue to fall, there is more incentive to add new features than to focus only on further cost reduction. New features improve overall system productivity, and video displays will benefit as much from this as from the growing image based technologies, such as video disc, video tape, teletext, and Viewdata.

Although video terminals will be more common in the future, hardcopy terminals will continue to be used for copying images from video screens and as alternatives to video displays. Low cost, hardcopy terminals will improve output quality dramatically. Dot matrix technology, which now dominates the field, is capable of producing higher quality fonts by varying the number, size, and location of the dots.

Dot matrix technology will continue to remain cost effective, but it is likely that other printing technologies will dominate by the end of this decade. Among the nonimpact alternatives (eg, ink jet), those using techniques related to office copiers are the most promising. Building these devices involves many specific choices for image generation—liquid crystal displays, cathode ray tubes, or lasers, for example—as well as the choice for transferring the image onto paper. Ultimately, many combinations of choices will appear in computer output devices, both because of the large underlying investment in copier technology and because the functions of these devices are compatible with computer peripherals for facsimile, optical character recognition, and graphics.

Apart from traditional soft- and hardcopy terminals, alternative input/output (I/O) devices will proliferate. Those widely accepted will be characterized by a high degree of compatibility with the needs and desires of users, rather than by their efficiency in meeting processor and memory requirements alone. Likely alternatives include speech recognition, which will improve from the small, discrete vocabulary systems currently available to embrace larger vocabularies, voice independence, and connected speech. Voice identification, a related technology, also will be used—in computer room security, for example. Speech synthesis is considerably easier than speech recognition, and is already being used in many applications. Image sensors, particularly television cameras using charge-coupled devices (CCDs), will be common in applications like quality control during manufacturing operations. Touch sensitive screens will achieve another form of nonlinguistic communication with computers. On the other hand, the great demand for processor resources could inhibit acceptance of some I/O alternatives: for example, the best current speech input system, the HARPY system built at Carnegie-Mellon University, requires about five dollars of computer resources, including 28M instruction executions, to process one second of speech using a 1k-word vocabulary.

Functional changes will be paralleled by enormous changes in performance. Historically, computer performance on calculation intensive problems has improved by about an order of magnitude every decade. In 1960 a program involving one floating point multiplication per iteration, such as a program to compute the mean and standard deviation of a population, could process statistics for the population of Canada within ten minutes. By 1970 ten minutes would suffice to process statistics for the population of North America, and in 1980 this program could process statistics for the world population in the same ten minute time frame. Progressing at a rate that would be breathtaking in other fields, change in computer performance is constantly forcing design of new system structures and opening new application areas.

Emerging system structures will emphasize distributed processing. As costs drop and performance increases, it becomes economical to eliminate bottlenecks by dispersing computational power among many subsystems. Therefore, since machines often devote half of their central processing unit cycles to editing, smart terminals containing editors can reduce the load on their host machine. Similarly, intelligent disc subsystems not only perform traditional storage functions more effectively, but also can fetch records, sort files, and provide full database management capabilities.

Economic factors that encourage intelligent subsystems also suggest replication of processors. Processor replication will take several forms, ranging from tightly coupled multiprocessors that share memory to loosely coupled processors that communicate over telephone lines. During the next decade, the most important trend in this area will be toward the widespread use of high speed local networks as the underlying physical structure for many situations in which timesharing is used today. Multiple processors bring pitfalls, such as stale data and directory updating problems. Further, they make existing problems, like operating system security and communications, more difficult.

Changes in computer technology stimulate the opening of new markets. At this moment, we are witnessing revolutionary effects of computer technology in the office environment. Word processing equipment has proliferated, and acceptance of electronic mail also is spreading rapidly. Costs of electronic mail are now competitive with those of traditional alternatives on a per message basis and, in some respects, electronic mail is now the superior medium. Whereas telephones remove the distance barrier, electronic mail removes the barriers of both distance and time; participants need not be available simultaneously for a dialogue to occur. Although universality is one of the greatest assets of the

telephone, a property electronic mail terminals will not approach for several decades, computer terminals already are becoming available on a per desk basis within some commercial enterprises. With suitable communicating data bases, more sophisticated auxiliary functions are possible, such as calendar management and meeting scheduling.

Following the typewriter and the telephone, the file cabinet is likely to be the next piece of office equipment affected by computers. Paper based file management is expensive and inefficient. For instance, one international corporation makes an average of 19 copies of every letter it receives, and files 8 of those copies to increase the possibility that at least one copy will be found when needed. Inevitably, electronic document management will join word processing and electronic mail as an efficient solution to the problems of paper based file management.

In the office marketplace, the current trend is toward integration of document processing functions with more traditional computer terminal functions in a single physical unit. Combinations of numeric data, nonnumeric data, and text could merge with other types of information such as facsimile and digitized speech. As global economic factors dictate substitution of electronic communication for physical transportation wherever possible, these trends may result in sophisticated forms of computer mediated teleconferencing that incorporate online management science tools.

Ultimate limits of computer function and performance are yet to be realized. Present computing structures are primitive with respect to their environment. Progress in computer function and performance over the past several decades has been remarkable, but it is likely that developments during the next several decades will be astonishing.

Ease of Use

Two major barriers to more widespread use of computers are programming and the computing environment. Computers must be programmed, and most people cannot program computers. In the more advanced nations, perhaps 1% of the population can program, but the proportion is much lower on a worldwide basis. Even for such simple computational devices as consumer calculators, sales of programmable models have been about two orders of magnitude lower than those of nonprogrammable models. Although the situation is changing rapidly, and programming has become a popular subject from elementary school through college, it seems certain that programmers will remain a minority through the end of this century. (See Fig 2.) At present, lack of trained programmers is the greatest obstacle to advanced computer applications.

Various routes over and around the programming hurdle are possible. Less procedural languages help by focusing on the functional requirements of a problem rather than on its solution methodology. Less procedural approaches include very high level languages and nonprogramming approaches, like query by example or query by form. Another route is the use of automated methods, such as customizable application generators, or application workbenches in which predefined modules are plugged together. Natural languages constitute a third route; current state of the art compels a choice between restricted language in a broad domain and relatively unrestricted language in a narrow domain. Restrictions will recede steadily, however, enabling natural languages to play an important future role. In certain problem areas, even natural language will never be as desirable as other approaches. For example, in a factory situation involving computer controlled robots, training by example would be preferable to any approach based on language.

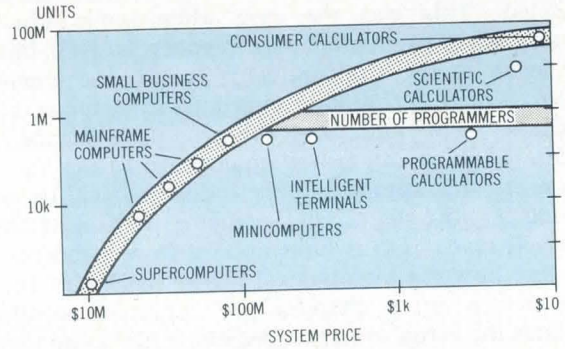

Fig 2 Programming hurdle. Number of programmers is still relatively small, making programming the most expensive cost factor in computing (Source: Mark Shepherd, Jr, 1977)

The other barrier to more widespread use of computers—the computer environment—requires operators to interact with computer systems in computer oriented terms. They must use an unnatural symbolism, beginning with an alphabet that features strange control characters. They must confront unnecessary distinctions, such as differing treatment of arrays and files; unpleasant tradeoffs, such as the choice between a friendlier, interpreter based environment and a harsher but more efficient compiler based environment; and unwanted bookkeeping, as in the generation and tracking of backup copies of current work. In short, users face a computer system with room for improvement at all levels, and need attention to the human engineering of the operator interface in particular. Because computer manufacturers are paying a great deal of attention to these problems, the next decade should see considerable progress toward their resolution.

Acquisition Cost

Acquisition cost has dropped steadily over the years and will continue to drop. Different portions of the acquisition cost are changing at different rates, however. Viewed as a whole, system costs will continue to decline by a factor of three every five years. This introduces the fear that the rate of technological progress will drive the technology intensive portion of computer costs to zero, leaving low technology, price stable components (eg, packaging) as the main determinant of system cost. This is unlikely during the coming decade.

On closer inspection, older technologies retain significant life. New technologies must shoot at a moving target; thus, the crossover point for a cost trend invariably lies further away in time than originally predicted. This was the case when semiconductor memory began to supplant core memory, and will be the case again in the semiconductor versus disc memory market. Older technology continues to change at a significant rate, and once the crossover occurs, by definition the overall rate of change accelerates.

Concern that computer price reductions will be self-limiting because the rapidly changing portion of costs soon will reach zero is built upon a false assumption. Consider how the hypothetical market basket of food, upon which price changes are reported monthly, misstates the actual situation because it allows no variation in product mix based on substitution effects that occur when the ratio of product prices changes. Fortunately, computer designers are bound by no such prescribed product mix. When the price of semiconductor gates declines, designers use them more liberally, especially as substitutes for more expensive components. This tends to prevent the overall semiconductor price component from dropping rapidly. Some of the most sluggish cost factors, like labor, are receiving particular attention as targets for substitution; this is the impetus for such trends as direct data entry, point of sale scanners, and optical character recognition.

Memory

Slashed by a factor of ten in the last five years, memory is the most rapidly changing component of computer costs, and one that will decline by at least as much again in the next five years. Here, the driving force is Moore's Law, a rule of thumb predicting that the number of bits on a memory chip will double every year. Changes in chip density translate with only modest dilution into changes in cost at the memory subsystem level. Computer architects have learned to build memory hierarchies that exploit price trends in subsystems that approximate their cheapest components in cost and their fastest components in performance.

In the next decade, semiconductor memory will be supplemented by newer technologies, especially magnetic bubbles. Serial semiconductor technologies, including CCDs, have the potential to be cheaper than conventional semiconductor memories by about a factor of three, but a variety of technological and market factors may deny them viability. Justified by their non-volatility and physical form factor, magnetic bubbles are already available for some applications. Widespread, future use will require a low and rapidly declining cost per bit as well.

Disc costs will decrease by a factor of three over each 5-year period. Semiconductor technology is gradually overtaking disc technology. However, the absolute difference between disc and semiconductor technologies will preserve a tenfold cost advantage for discs through the 1980s (Fig 3). Economy of scale is an important aspect of the disc cost advantage; rather than wait five years to achieve a factor of three reduction in cost per megabyte, one can obtain the same effect immediately by moving from a single- to a double-platter disc, or gain yet another factor of three by moving to a larger, multiple-platter disc. Thus, when semiconductor memory finally supplants discs, it will do so gradually by eroding the disc market from beneath. Continued disc improvements derive from parallel progress on recording heads (eg, thin film heads), recording media (eg, plated media), modulation techniques, and error correcting codes. Error correction, in particular, illustrates use of inexpensive computational power to realize the economy of a higher physical error rate while simultaneously achieving the performance of a lower visible error rate.

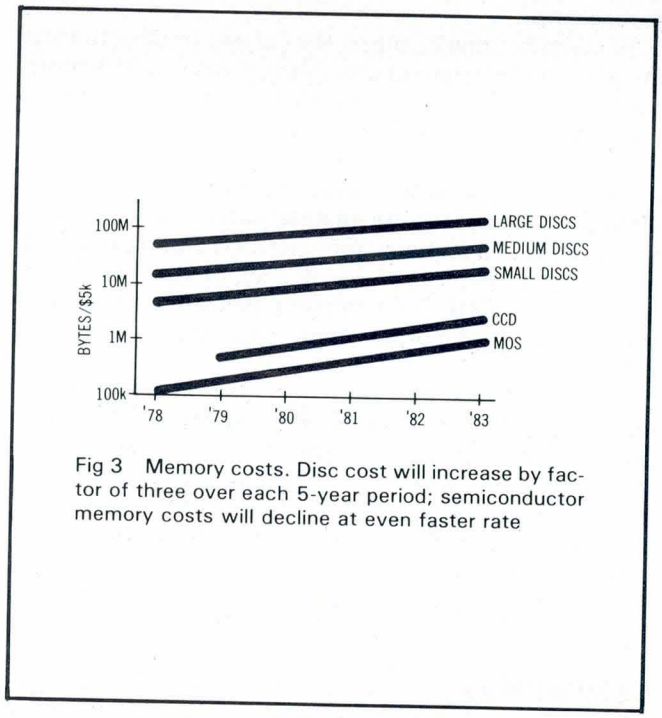

Fig 3 Memory costs. Disc cost will increase by factor of three over each 5-year period; semiconductor memory costs will decline at even faster rate

Processors

Processors, having a high proportion of semiconductor devices, decline faster in cost than do computer systems as a whole. Consequently, use of multiple processors is attractive in a variety of situations (Fig 4). Two microprocessors can handle foreground and background workloads separately on a single microcomputer

board. System or application programs can be partitioned among dedicated structures composed of multiple processors. More generally, large systems can be built from many smaller systems, as in the case of the CM* system, which contains 50 PDP-11s, built by Carnegie-Mellon University.

In the memory and processor areas, cost reductions are primarily accounted for by the use of semiconductor large scale integration (LSI). However, several problems must be considered in order to realize the potential benefits of LSI. LSI design costs are very high, especially when the cost of building computer aided design tools is included. For example, the cost of designing certain high volume microprocessors exceeded the total manufacturing cost for all of the units ultimately produced. Hardware economics is becoming more similar to software economics in this regard. Another problem with LSI is the overhead cost of interconnecting the chips. For instance, wire delay in the KL-10 processor accounts for about 40% of the instruction cycle time. The third problem with LSI is that full economic reward can be achieved only through high volume production of every part, a volume normally possible only for parts with regularity.

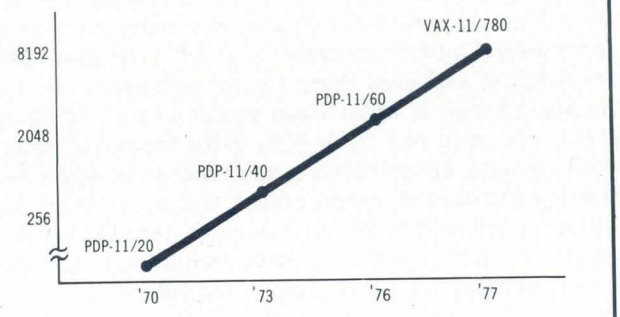

Fig 4 LSI components reduce cost. Although processor control storage has increased in size, its high proportion of LSI components makes processors decline in cost even faster than entire systems, motivating multiprocessor designs

Regularity has become a guiding principle that pervades every level of computer system design. At the hardware level, read only memories, random access memories, and programmable logic arrays are used wherever possible. Microprocessors are used in lieu of hardwired logic. In software, table driven and rule driven approaches are preferred. Even in architecture, regularity and symmetry are sought at both the instruction set/processor level and at the processor/memory system level. Examples at these levels include operation code regularity in the VAX-11 and a trend away from master-slave designs toward symmetrical multiprocessor designs.

A most dramatic example of increased reliance on regularity is the role of the microprogram control store in modern processor design. Whereas 100-byte control memories were typical a decade ago, modern designs use tens of thousands of bytes. Current micromachines and control stores are larger and more complex than many of the complete computers sold in 1970. It comes as no shock that the software issues of that era, including higher level implementation languages, program testing, and realtime operating system design, have resurfaced as issues in hardware engineering.

Power and Packaging

One final aspect of computer hardware cost is the surprisingly high price of power supplies and packaging; for example, these less glamorous technologies account for about 30% of the cost of a PDP-11/70. Although it is true that they are changing more slowly than other technologies, they offer as much potential for cost reduction. Higher volumes of products like terminals make affordable the initial tooling costs characteristic of inexpensive packaging methods, such as molded plastic. In power supplies, the typical cost of about $1 per watt is gradually but steadily declining. Drastic cost reduction can be achieved by using fewer watts; for example, an LSI version of the PDP-8 can run on flashlight batteries. One approach to power and packaging cost reduction integrates small computer systems within a single physical package to facilitate global design optimization and to reduce the packaging costs. The PDT series illustrates this trend by integrating processors and mass storage into terminals.

Operating Costs

Although acquisition cost receives a disproportionate share of attention during computer procurement, it is widely recognized that operating costs far outweigh the cost of acquisition. Users would like to come to grips with these other portions of the total life cycle cost of a computer system, but they find it difficult to do so because operating costs are spread out among programming, field service, other labor costs, power consumption, and expendable supplies.

Programming

Programming is the most expensive factor in computing, and this can be seen by comparing the monthly rental charge for computer equipment with the monthly salary and overhead costs of the programming staff, or by contrasting the cost of purchasing a byte of memory (between a penny and a nickel) to the cost of writing a byte of software to fill it (about a dollar). This analysis is misleadingly simplistic because the economics of replicating hardware and developing software are very dissimilar. However, given the trends of declining hardware costs and stable software costs, the situation a decade from now could be astounding—the cost of filling a byte of memory with software could be more than a thousand times the cost of buying it.

Programming cost provides overwhelming motivation to produce systems that require less programming. Furthermore, in many applications, the cost of software maintenance far exceeds the cost of software development. To some extent, software maintenance costs reflect a problem in terminology; "maintenance" implies repair of a mechanism to restore its original state, and "software maintenance" is usually a misnomer for what would more properly be called "software evolution," a special form of software development. One area of current research explores harnessing database technology to track and control software as it evolves. A frequently overlooked aspect of programming cost is the large amount of formal and informal training required to use computers effectively. Future systems will be not only easier to use, but also self-teaching in tutorial and reference modes.

Field Service and Other Labor

Because repair is labor intensive, the ratio of field service costs to equipment cost increased steadily in the last decade. The ratio of 100 months' field service cost to the purchase price of a computer gives a simple indication of the current state of affairs. Today, this ratio is likely to be about 50% for a typical medium size computer; and more than 100% for a microcomputer. In other words, repair costs may exceed the initial purchase price, a situation being attacked by increased reliability of computer systems and by alternative field service methods that are less labor intensive.

Other labor costs include the cost of data entry clerks and computer operators. Attempts to cut data entry costs focus on capturing data at the earliest opportunity in a form the computer can use, and on automating data capture wherever possible. Examples of these trends include supermarket point of sale scanners and optical character readers. Computer utilities charge up to $25 to mount and dismount a private disc pack. Repeated mountings and dismountings at these rates are less cost effective than a capital intensive solution, such as online archival storage.

User wait time is a labor expense that is easily overlooked (Fig 5). Instead of instantaneous response to most requests, the operator of a terminal in a multi-user system experiences a short delay, typically a few seconds and costing a penny or less. When multiplied by the number of transactions per hour, the number of hours in the life of the equipment, and the number of terminals on the system, however, the total cost is quite high. Specifically, when the average response time exceeds four seconds, the labor expense for operator wait time exceeds the hardware cost of a typical, large timesharing system. Since operator wait costs are directly proportional to response time, addition of hardware that improves response time is often an excellent investment. As with quantity, equipment quality exhibits a similar phenomenon. For example, purchase of a video terminal with slightly lower flicker and slightly higher productivity usually reflects a wise decision in terms of total life cycle costs.

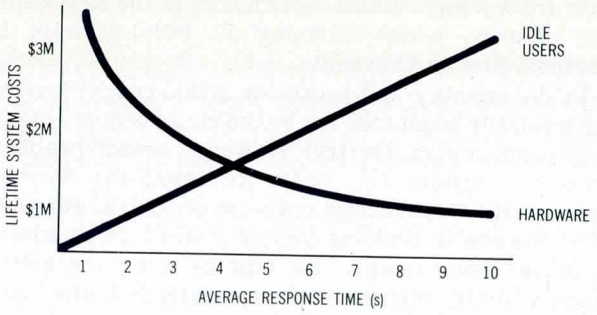

Fig 5 Labor expenses. Field service costs are increasingly significant, and user waiting time is easily overlooked major labor expense. When average response time exceeds 4 s, expense for waiting time can exceed typical system hardware cost

Electricity and Expendables

Though reduced by the rising level of semiconductor integration, the electricity costs to run a computer system should not be ignored. Lifetime electricity costs range from several hundred dollars for an LSI-11 to about $10k for a KL-10, and even these figures understate the true situation because, apart from power to run the equipment, one must pay 20 or 30% extra for power supply inefficiencies, about 10% extra for fans to dissipate heat into the surrounding environment, and a sizable air conditioning bill to cool this environment. (See Fig 6.) Here again, low power semiconductor technologies will play an increasingly important role in the future.

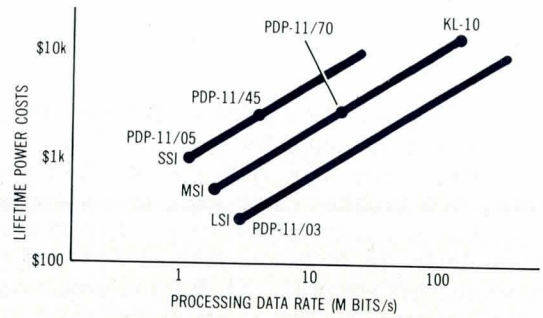

Fig 6 Power costs. Electricity costs can exceed thousands of dollars over system life. Power supply inefficiencies and electricity to control computer room environment can add 30 to 40% extra to operating costs

One final category of operating costs involves expendable supplies such as paper and storage media. For example, a typical nonimpact printer uses more than a million sheets of paper a month; the cost of this megasheet of paper dominates the cost of the printer itself. Removable disc pack subsystems further illustrate media costs. One current drive sells for $3800, and over its lifetime, the typical user purchases 20 disc packs for it at $150 each. That is, roughly as much will be spent on the disc packs as on the drive unit.

Since removable media induce extra hardware and extra labor costs, there will be a trend toward nonremovable media. However, removable storage will continue to play an important role owing to considerations of portability, security, long term backup requirements, and data interchange. In this last regard, a jumbo jet filled with magnetic tapes might be viewed as a high bandwidth, low cost, computer communications medium. Solid state removable storage media will come to dominate the smallest module sizes for two reasons. Magnetic media offer economies of scale that become drawbacks in this application—for half the price, one can buy half as much solid state storage but not half as much magnetic storage. More important, magnetic media tend to have a natural minimum size, whereas solid state storage lacks this limitation.

Reliability

At the current state of the art, small computers and systems of large computers that serve as backup for one another have reliability well in excess of 99%; however, individual, large multi-user systems typically "crash" every few days. Thus, there is still a difference in reliability of several orders of magnitude between computer utilities and, say, electric power utilities. User desires and designer skills will combine to narrow this gap in the next few years.

Full reliability demands a layered system approach. Any layer must be designed to be as reliable as possible, devoting particular attention to reliable operation even in the presence of errors in lower layers. There are important reliability and availability issues at every level from the innermost hardware circuitry to the outermost layer of application software.

Some rules of thumb can be applied in designing for reliability. First, select basic components that are as reliable as possible. For example, other things being equal, use semiconductor memory rather than rotating memory. Second, fewer components lead to fewer component failures. Thus, for instance, serial design techniques have the advantage of needing fewer circuits and fewer connectors. Standard methods for computing reliability depend heavily on component counts, but this factor alone can be misleading. Last, careful use of redundancy can significantly increase reliability. Many reliability techniques are based on some form of redundancy. The first reliability improvement to memories was addition of an extra parity bit for single-bit error detection. By adding more redundant bits, single-bit error correction and multiple-bit error detection became widely available. By doubling or tripling the number of memory bits, even higher levels of reliability based on standby memories and two out of three voting logic are possible for critical applications.

Currently, the weakest link in system reliability by far is software. Although some lessons in software reliability can be learned from the hardware reliability experience, progress is likely to be slow because the complexity of software is much greater than that of hardware, and many of its underlying failure mechanisms are different. For the long term, formal proofs of correctness for software (and hardware) hold promise; the first practical results in this area have just begun to emerge from research laboratories.

To build the high availability systems that will be commonplace a decade from now, reliable hardware and reliable software both will be needed. Hardware must be especially reliable, and in particular, it must be structured to avoid single points of failure. However, the main burden of providing high availability is likely to fall on the operating system software, which must be capable of dynamic recovery from a wide variety of failure modes through reconfiguration of hardware units. One of the tradeoffs to be faced by designers is the degree of coupling in future multiprocessor systems. Performance considerations encourage a tight coupling, whereas reliability considerations suggest a looser coupling to inhibit fault propagation.

Serviceability

Regardless of the attention paid to reliability, it is inevitable that failures will sometimes occur. In fact, higher reliability does not always go hand in hand with minimal service needs. For example, triple modular redundancy can be used to make availability rates very high, but the total number of failures requiring service will roughly triple. This scenario opens possibilities for new servicing techniques. If a user were able to continue operation at a reduced performance level after a failure had occurred, servicing could move to a more efficient, scheduled basis rather than the current, crisis driven basis. To avoid operational interruptions during the actual servicing, online diagnosis and repair are essential. Such techniques are now being used; for example, one of the KL-10 memory subsystems uses error correcting codes that allow a memory board swap while the memory is operating.

Remote diagnostics, the major recent improvement in servicing techniques, now is being used in North America and in Europe to diagnose many computer failures over telephone lines from a central site that houses more expertise and is more accessible than traditional alternatives. In the United States, more than 90% of PDP-11/70 customers have elected this approach. Since remote diagnostic equipment is furnished at no charge and may result in lower field service costs, it has been accepted enthusiastically. Moreover, the emphasis on diagnostic rather than repair functions is in keeping with current trends toward more complex structures. For instance, determining that the chip in an LSI

microprocessor is defective can be very difficult and time-consuming, despite the fact that actual repair, involving a component swap, is comparatively simple. As diagnostics become more highly automated and the repair aspect more straightforward, the prospect for greater user involvement in routine servicing gains promise. Both user installation of new systems and user repair of simple failures are inevitable, especially for smaller systems.

As in the case of reliability, the main challenge for serviceability in the coming decade lies not in hardware, but in software. Mechanical aspects of software service that have been automated include parameter generation for operating system installation and insertion of patches to remove software bugs. However, software servicing techniques remain quite primitive and labor intensive. Until more progress is made on this front, high serviceability costs provide an extra incentive to build a quality product that minimizes the need for service.

Compatibility

An economic necessity both for computer manufacturers and for their customers, compatibility is a vital element in other fields of technology. For example, the most important single reason that fluorescent lighting has been slow to replace incandescent lighting, even in this era of energy crisis, is that the physical form factors are not compatible. In computing, the magnitude of existing hardware and software investments often makes compatibility an overriding consideration.

Computer compatibility can be discussed at many different levels. One of the neglected levels of software compatibility is that of the operating system. In the past, this did not stand as a widely accepted goal; for example, the PDP-11 has supported a variety of operating systems that focused on different classes of applications. By late in their life cycles, these tended to converge in function while still requiring individual support. Thus, in the case of the newer VAX-11 computer series, one goal is to provide a single operating system that will serve the full range of machine sizes and applications.

Superficially controlled by existing standards, programming languages, particularly the less complex languages like BASIC, exhibit a wide spectrum of incompatible dialects and extensions. It is noteworthy when a manufacturer's various BASIC systems can share a common reference manual, as for the DECsystem-10, DECsystem-20, PDP-11, and VAX-11. In the same context, one can address data compatibility at the level of media, records, files, and even database management. In general, issues become more difficult—and compatibility less common—as one moves upward in this hierarchy.

Hardware designers have been quick to accept compatibility at some levels but slow to recognize its importance at others. There is a heavy emphasis on compatibility at the instruction set level, but compatibility below this level is almost unheard of. Although use of buses gave rise to interconnection standards and development of the plug compatible industry, there have been few standards for compatible buses, even among products from a single manufacturer. Economic burdens of incompatibility are great; because of the combinative nature of processors, operating systems, and buses, the cost of writing diagnostic software for each new peripheral device offered by DEC exceeds one million dollars.

Intersystem compatibility issues will receive more attention in the future than they have in the past. Already, most large users incorporate equipment from several vendors, and intersystem issues will become increasingly prominent as sophisticated interconnection services (such as AT&T's Advanced Communications Service) become widely available. Even users of a single manufacturer's equipment encounter issues of heterogeneous interconnected systems, since many vendors support multiple-product families. All users seek viable migration paths that can incorporate new technology as it becomes available. Questions that must be faced involve every aspect of compatibility and the full spectrum of interconnection from local buses to geographically distributed processing. Answers to these questions will determine the degree to which each user reaps the benefits achieved by underlying technological trends during the coming decade.

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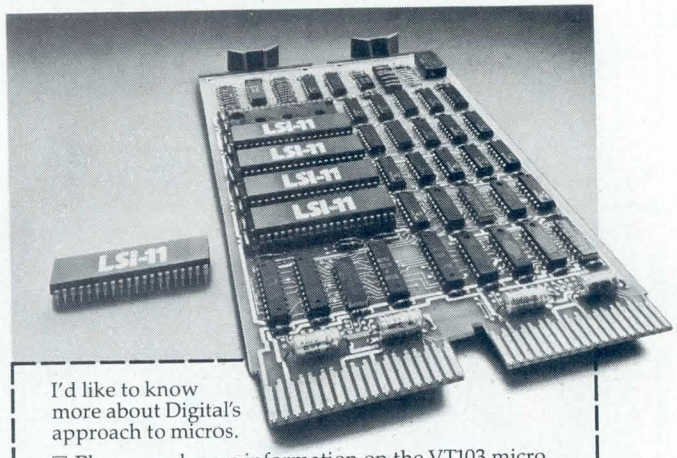

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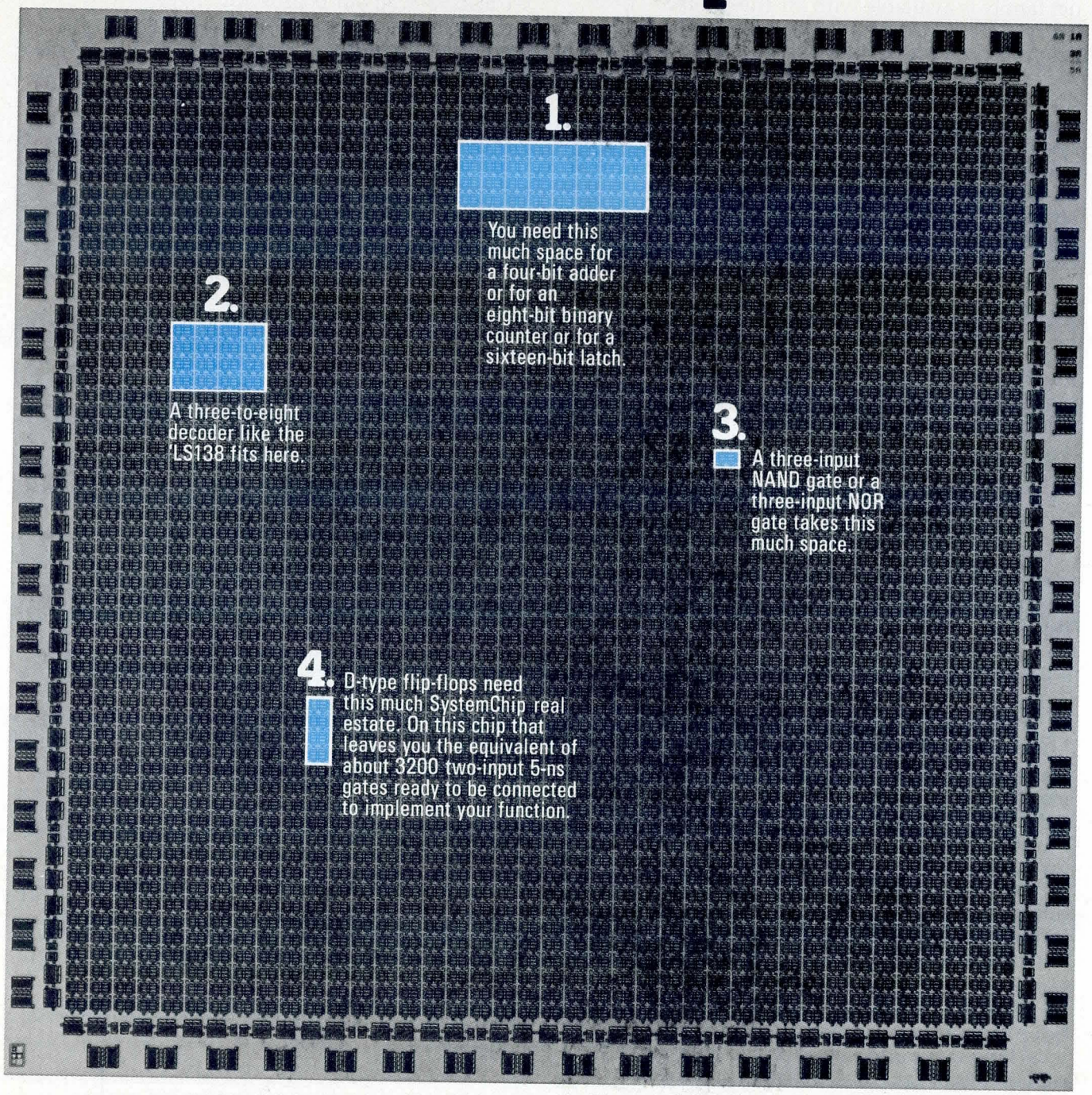

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FEATURE

INTERCONNECTION SYSTEM APPROACHES FOR MINIMIZING DATA TRANSMISSION PROBLEMS

Rf circuit design techniques reduce signal degradation and crosstalk to permit increased bandwidth in high performance digital systems

Robert K. Southard

AMP, Incorporated
Harrisburg, PA 17105

Advances in digital logic and complex components, in conjunction with the extraordinary speeds of charge-coupled devices, emitter-coupled logic, and gallium arsenide technologies, provide the high performance demanded by today's computing environment. As the speed of logic families increases, signal rise and fall times and propagation delays decrease. The problem of getting data from one place to another in a high performance system becomes more difficult with this delay and rise time decrease, often as a direct result of the bandwidth of the interconnection system required to carry data pulses.

The graph in Fig 1 plots the trend of common logic families, extending to the latest in high speed technology. Lines marked N = 1 and N = 10 plot the equation of the bandwidth required to pass the pulse signal.

$$BW = 0.35N/t_r$$

In the equation, t_r equals the device rise time and N is the highest harmonic of the propagation frequency to be passed.[1] At N = 1, the system distorts the pulse rise and fall times, and barely passes the leading and trailing edges of the desired pulse. In the normal high performance situation, at N = 10, the system passes signals

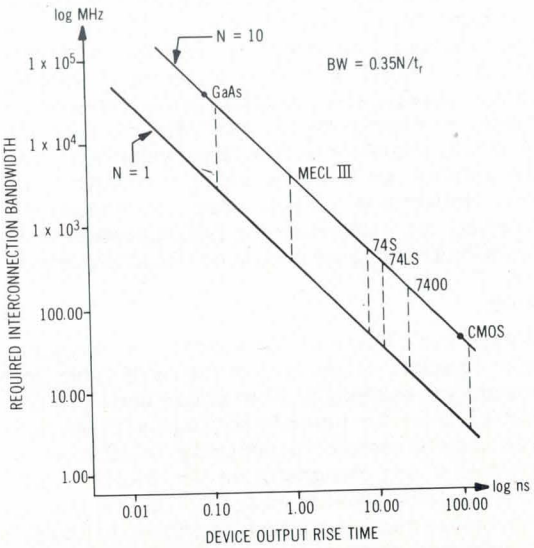


Fig 1 Fast logic demands high bandwidth. Graph plots approximate system interconnection bandwidth for maximum performance as function of device rise time for popular and more recent logic families. At N = 1 harmonic, system barely passes pulse rise time. At N = 10 harmonic, system passes rise time almost undisturbed

Transmission Line Factors

Characteristic Impedance

Characteristic impedance (Z_0) is a function of the geometry and the materials of a system. In a transmission line, two wires are surrounded by a dielectric material. Between the two wires is a capacitance, which is a function of the spacing between the wires, the dielectric constant of the material between them, and the effective plate area of the wires. In simple instances, plate area is equal to the diameter times the length of the wire, and capacitance is expressed as microfarads per unit length. The two wires have a mutual inductance that is essentially a function of the distance between the wires, their diameter, and the wire length (the magnetic permeability of the surrounding material is usually unity). This inductance could be expressed as microhenries per unit length. If a 1-unit section of wire had a capacitance of x microfarads, and an inductance of y microhenries, the impedance (Z_0) would be $Z_0 = (y/x)^{1/2} = A\ \Omega$. For a 2-unit section, the capacitance would be 2x and the inductance 2y; impedance would remain the same. Therefore, the impedance of a matched line is independent of its length. It could be said that each unit area of line cross section has its own characteristic impedance.

Reflection Coefficient

The reflection coefficient is a measure of how well the transmission line has achieved impedance control. A well-designed system, in which the circuits at both ends of a line are matched to the impedance of the line itself, provides for maximum energy transfer between the circuits. Furthermore (and more important for digital applications), a well-matched system prevents the generation of noise on the line, indicated by reflections at points where impedance changes. The amount of voltage reflected determines the voltage reflection coefficient, ϱ; when 10% of the voltage is reflected, $\varrho = 0.1$. In terms of voltage standing wave ratio (VSWR), this impedance mismatch is expressed as the ratio of the two characteristic impedances. The larger value is divided by the smaller, so that the result is always 1 or greater. Reflections, which occur at impedance mismatches, are delayed by the propagation time of the cable, and may cause undesired circuit triggering.

Crosstalk

Crosstalk is the amount of signal pickup on one quiet line from adjacent, driven lines in the same cable (for multiconductor cables), or from driven lines in adjacent cables; these are normally termed line to line and cable to cable crosstalk, respectively. In addition to representing a loss of signal from the driven circuit, crosstalk contaminates the adjacent, quiescent lines, and may cause false triggering, overloaded circuits, and interference. Crosstalk can be measured in both forward and backward, or reverse, directions. Backward crosstalk is measured at the input end of a quiet line with respect to a driving device. Here, coupling of the driven signal produces an output on the quiet line, which has the same polarity as the applied voltage, but is reduced in magnitude by a factor related to k_B, the back crosstalk coefficient.

Forward crosstalk, on the other hand, is related to the velocity of different modes of the propagating wave. In a homogeneous dielectric medium, the mode velocities are equal; consequently, forward crosstalk is zero. However, in an open transmission line system with composite dielectrics of both air and substrate, the forward crosstalk becomes a function of the transmission line length, the voltage rise time of the applied signal, and, indirectly, the circuit coupling. Although peak forward crosstalk can be fairly high, its duration is very short, (often less than t_r), so that little energy is actually transferred, and many circuits are unaffected.

Attenuation

Attenuation of digital pulses results in degradation or distortion of the pulse in terms of a loss in peak voltage, a slower pulse rise, or both. There are two possible sources for these problems: conduction loss in the dielectric and resistive loss in the conductor. Both are functions of frequency; dielectric attenuation varies directly, whereas conductor loss (skin effect) varies as the square root of frequency. The sum of these two loss parameters represents the total loss of a line section and is usually measured in dB per unit length. At frequencies of 1 GHz, the dielectric loss represents about one-third of the total attenuation. At 500 MHz, dielectric losses are down to one-fourth of the total. Thus, resistive losses tend to dominate below 1 GHz. With respect to conductor size, attenuation and its dc relatives, resistance and current carrying capacity, are essentially functions of wire size. As signal frequencies get higher, however, a greater portion of signal current is carried on the surface of the conductor (skin effect). A flat conductor, with its greater surface to volume ratio, thus provides lower high frequency attenuation than does a round wire of equal size.

Propagation Delay

Propagation delay is the time required for a pulse to travel through a transmission line system. It is the reciprocal of signal propagation velocity, and is, essentially, a function of the dielectric constant of the insulating material. Low-delay signal transmission is essential for high speed computer systems. In open transmission systems, where the insulation is not homogeneous, effective dielectric constant is an average value of the different materials. In most flat cables, some of the electromagnetic field escapes the insulation, and propagates in the air around the cable. This tends to decrease the dielectric constant, which increases the propagation velocity, but also increases the ground plane susceptibility, which may have the opposite effect. At high frequencies, when the dielectric constant of the insulation varies with the frequency, the different frequency components see different dielectric constants, and different propagation velocities cause pulse distortion.

easily, with almost no pulse edge distortion. For example, to use 74LS parts to maximum advantage, the system bandwidth must be extended from the very high frequency (vhf) range to the ultrahigh frequency (uhf) range mostly encountered by radio frequency (rf) circuit designers (and often unfamiliar to digital or data system hardware designers). As system speeds increase, system designers must familiarize themselves with parallel data transmission systems whose bandwidths easily extend into the microwave region.

Phase delay (time skewing) and ringing have a critical impact on system operation. In addition, parallel data transmission paths can produce crosstalk, significant noise in a "quiet" line induced from the active lines. Data integrity is maintained in typical systems by restricting ringing and crosstalk to about 10% of normal signal levels (−20 dB). High performance systems generally operate with relatively short runs in which data repeating amplifiers are not used along the basic transmission path and high noise margins are desirable. Amplitude losses in many systems, therefore, must be held to 20% to 25% (2 to 2.5 dB) along the transmission path.

When overall ringing, crosstalk, and signal levels cause signal degradation of more than about 30% at the chip receiving the data, noise margins become unacceptably high, and produce excessive error rates. High amplitude, wide bandwidth, and electrical noise environments must also be taken into account, but fortunately most system designs that eliminate crosstalk problems can eliminate outside electrical noise problems as well.

Failure to plan for the analog requirements of rf transmission at high frequencies when designing the interconnection system can create a system level malfunction that is almost impossible to cure through a retrofit. Often transmission problems do not show up until late in the design cycle, during board integration and test. Retrofit at that point would require significant changes in chip fanout and board layout densities; the selection and use of proper connectors adapted to wide bandwidths; and the use of special, low loss cable.

Data Transmission Problems

Circuit and systems designers unfamiliar with very high speed data transmission did not need to consider the effects of basic interconnection paths in previous designs; data transmission line problems do not exist over a signal transmission distance that is a very small fraction of the signal wavelength. However, system performance can be impaired as the wavelength of the highest frequency being transferred approaches the transmission path length. After the data transmission path exceeds a significant fraction of a wavelength, a transmission line approach must be introduced, with its attendant factors including characteristic impedance, attenuation, and reflection coefficient.

Fig 2 represents some critical signal path distances, and plots critical wavelength as a function of system cutoff frequency; the range of critical distances depicted extends from 8 ft (2 m) for 7400 logic, to 0.65 in (17 mm) for MECL III. The curve plots $\lambda_{1/8} = V/8f$, where V is the propagation velocity, and f is the rise time frequency being propagated. (Compare Fig 1.) The range of electrically equivalent distances for data transmission at each frequency extends from 23 ft (7 m) to 0.3 in (8 mm), as f varies from 3.5 MHz to 3.5 GHz.

Point A in Fig 2 represents a critical distance of 8 ft (2 m) at the 10-MHz frequency that represents the approximate lower end of useful bandwidth for a high performance 7400 transistor-transistor logic (TTL) system. Point B similarly represents the critical one-eighth wavelength distance of 2.3 ft (0.70 m) at 35 MHz, the approximate lower end of useful bandwidth in a high performance 74LS logic application. High performance 74S logic has a similar critical distance of 2.8 in (71 mm) for a transmission interconnection bandwidth of 350 MHz, shown at point C. Point D represents the high performance end of operation of MECL III logic, having a critical distance of 0.65 in (17 mm) at a frequency of 1.5 GHz. At these speeds, even the distance a signal travels through a connector is important.

Stray capacitance between signal conductors increases signal interference from one data line to another (crosstalk). As an example, 1.0 pF of stray capacitance between two conductors has a reactance of 450 Ω at 350 MHz and 45 Ω at 3.5 GHz. To illustrate, a 1.25-in (31.8-mm) length of typical ribbon cable, which has an approximate capacitance of 1 to 2 pF, can cause significant signal coupling from one parallel data line to another, and generate noise on the second line. Depending on the circuit impedance in the system, such signals can significantly reduce noise margins, thereby increasing error rate.

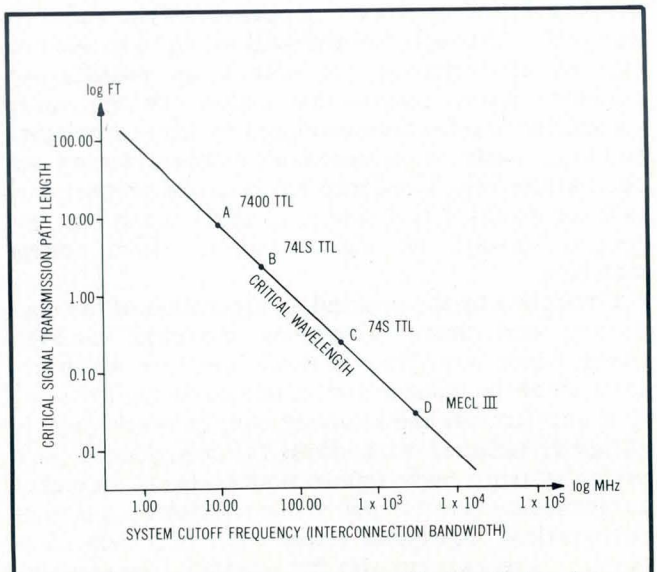


Fig 2 High bandwidth reduces critical path length. Graph plots critical signal path length as function of interconnection bandwidth, assuming critical path of one-eighth wavelength. Assumed system wave propagation velocity is 6.55×10^8 ft/s, which is typical propagation velocity in transmission system

Design Recommendations

Attention must be paid to every detail in the rf transmission path, but only a few basic concepts are essential for adequate system design. Choosing characteristic impedance, the most important design decision, involves a small set of tradeoffs among the logic family used, printed circuit (PC) boards that are practical to fabricate, and the impedance of available cable/connector combinations. Determining the design approach for the required system transmission bandwidth involves a tradeoff between the performance dictated by the PC technology and an acceptable error rate and cost.

Transmission Bandwidth

For high system performance, transmission bandwidth must pass the tenth harmonic of the system pulse rise time at the 3-dB point. (See the equation in Fig 1.) System design then can be continued, by assuming a critical transmission distance of one-eighth to one-tenth of a wavelength at this frequency and a signal propagation velocity of approximately 7.7 in (196 mm)/ns. For example, a system with a pulse rise time of 10 ns has a required signal bandwidth of 350 MHz for N = 10. The critical one-eighth wavelength distance at this frequency is 2.6 in (66 mm). (See Fig 2.) Any signal path in the system longer than this distance must be considered as a transmission line in the design. Each portion in turn, including PC board, and traces, connectors, and cables, must then be matched to a characteristic impedance.

Characteristic Impedance

After calculating the critical transmission distance, the designer should specify the impedance of the transmission cable. Although the ideal goal would be to select as high a characteristic impedance as possible—to minimize driver power—this makes the line more susceptible to reflections produced by load capacitance and to crosstalk. Also, since both PC board density and PC characteristic impedance are inversely proportional to trace width, it is desirable to select the system impedance toward its higher end for total system matching.

Controlled by the physical configuration of the conductors and their surrounding dielectric material, characteristic impedance is that impedance which absorbs all of the signal energy at one point in a transmission line—usually the receiving end, in which case no energy is reflected back down the line. Hence, in a perfect system a pulse appears undistorted at the end of a transmission line terminated in a resistance equal to its characteristic impedance (except that it is delayed in time). In a real system with fast rise times, the receiving integrated circuit (IC) input capacitance prevents this ideal resistive match.

When the line is not matched, energy is reflected from the end of the line and appears to reflect up and down the line, with a delay between each reflection that is proportional to the length of the line; reflections appear as ringing (or even distinct steps) at the receiving end. In short, the distorted signal appears as a coherent noise on the signal line; when sufficiently high in amplitude, this noise can cause data errors.

The reflection coefficient ratio determines how well a transmission line is matched to its characteristic impedance. Practical high performance systems must use a specific characteristic impedance throughout the transmission path. As the signal passes from the sending IC through the PC board; connector, backplane, or cables; a second connector; the receiving PC board; and, finally, the receiving IC, it goes through a number of physical elements [Fig 3(a)]. Any significant section of the path must maintain the selected transmission characteristic impedance. An abrupt change in impedance is called a discontinuity. Energy is reflected from the point of each discontinuity, and creates an effect similar to that of an unmatched line.

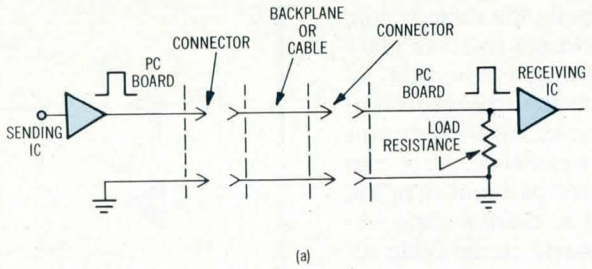
Testing

Testing is best accomplished using the time domain reflectometry (TDR) technique. TDR applies a step pulse (generated from a known source impedance and usually less than 150 ps) to the transmission system. A wide bandwidth oscilloscope measures the resulting signal waveform. Since the pulse step is very rapid, it is possible to locate the position of the system impedance discontinuities and measure their reflection coefficients by observing the resulting signal. The step signal propagates down the line at a controlled velocity, and the reflections from any impedance discontinuity appear as reflected voltage at a time measurable from the start of the pulse. TDR can also observe inductive and capacitive loading effects, and is used universally to determine the quality of transmission possible in a given system.[2] This includes determining the degree of mismatch in PC board traces, connectors, and cables. Using TDR, the designer can verify how well the design has achieved a matched condition.

TDR, however, has limitations. One is that the system bandwidth of TDR limits the shortest length of an observable discontinuity. Another limitation is that TDR equipment may have a rise time much faster than that of the system under investigation, and consequently give too much detail concerning discontinuities that will have little effect on the actual system. This latter problem can be reduced by adding controlled filters to slow the TDR rise time and limit the range of output frequencies from the TDR step generator. TDR can also be used to study the system crosstalk effects. In this case, the step is placed on the active line, and its effects are measured on the quiet line.

Basic System Elements

Once the characteristic impedance is selected, in practice somewhere between 50 and 150 Ω, the cables, connectors, and PC board can be chosen. Only a few approaches to PC boards are practical, and cable and connector choices are often interdependent (especially in



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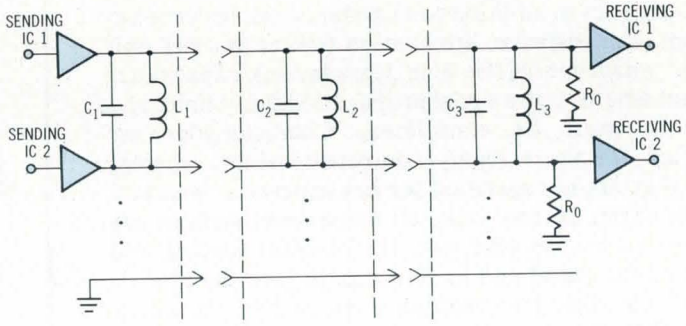

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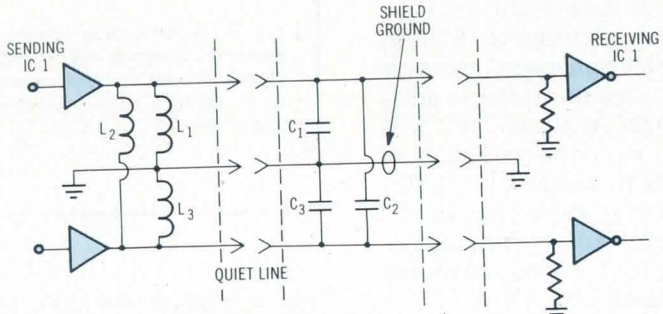


(c)

Fig 3 Signal path properties constrain data transmission. Typical data transmission path (a) carries signal through PC board traces, connectors, and backplane or cable. Each section of path must present same characteristic impedance; impedance discontinuity reflects signal energy back toward data source. In (b), capacitive coupling between parallel lines becomes more critical at high frequencies, causing crosstalk. Shield ground in (c) reduces crosstalk because inductance L_2 is much larger than L_1 or L_3 and capacitance C_2 is much smaller than C_1 or C_3; therefore, signal energy that would be coupled from path to path is instead coupled to ground

parallel data systems). Following these design decisions, PC board, connector, and cable transmission pairs may be configured for the longest expected run in the system. Critical to this process is the testing of a model transmission system.

Several other important circuit transmission line characteristics to consider are PC board microstrip (and other) rf techniques; specialized data about rf characteristics of standard connectors or special connectors designed for high speed use; and specialized rf characteristic data about standard cables such as ribbon or flat conductor types, or special cables designed for high speed data use. Also, crosstalk at high frequencies can be reduced by spacing the parallel data conductors farther apart, reducing the coupling in either PC board traces or cables [Fig 3(b)]. Shielding bypasses the mutual signal line capacitance to signal ground and is most effective in reducing crosstalk. [See Fig 3(c).] The shield ground, located between the two signal lines, presents a much lower impedance for signal currents to the signal return path than does the nearby quiet line; thus, capacitive reactance of C_2 is much higher than that of C_1 or C_3. Similarly, mutual inductive reactances L_1 and L_3, created by the effects of currents in either signal line and in the ground line, will be much smaller than the inductive reactance between the signal lines, L_2. An ideal transmission line configuration would be a totally shielded or coaxial cable, because the surrounding shield would reduce intercoupling dramatically.

Cables

Cables carry data between widely spaced sections of a subsystem; therefore, they are likely to be the most

critical portion of the transmission path. In high performance systems, it is imperative that the cables have a controlled impedance. Choices among the various controlled impedance cables include twisted pair, standard and special ribbon, flexible flat transmission, and coaxial. The choice of cable, as well as the arrangement of signals and grounds in the cable, will determine transmission path characteristic impedance. Low cost approaches, such as standard twisted pair and standard unshielded ribbon, do not permit a characteristic impedance below about 80 Ω; higher cost, special cable approaches allow well-controlled characteristic impedance ranging from 50 to 150 Ω.

Depending on the application, several cable characteristics in addition to impedance can become important. For instance, attenuation (signal loss per unit length, which causes rise time degradation), capacitance per unit length, pulse signal propagation delay time, and crosstalk must be considered. Characteristics are specified for more highly controlled cables, whereas often they are not specified for less expensive, standard ribbon cable. In any case, all cable specifications are determined by the wire size, the physical spacing and shape of the signal and its return path, and the properties of the dielectric medium surrounding the cable. Cable characteristics are predictable to the extent that these factors are controlled; if they are not controlled closely, the system experiences data signal degradation, signal distortion, or data loss.

In bit parallel systems, several data signals must be sent from one place to another concurrently. Parallel transmission complicates the cable application, because several data lines can generate crosstalk signals in adjacent signal lines. Another danger in parallel paths is pulse skewing, which is caused either by variations in path length from one signal line to another, or by differences in pulse delay time during cable runs of the same length. Furthermore, parallel data systems require cable that is reasonably flexible, so that it may be routed conveniently throughout the system.

Standard ribbon cable construction permits a good deal of control over transmission path spacing dimensions and signal path length in parallel data systems. To maintain well-controlled characteristic impedance and low levels of crosstalk, standard cables are driven with alternating signal and return lines for single-ended and differential drivers, as illustrated in Fig 4. Such an arrangement produces characteristic impedance of about 85 Ω. Fig 5(a) illustrates the expected variation of characteristic impedance for standard polyvinyl chloride (PVC) ribbon cable, and also for polyethelene cable clad with PVC. The wire diameter, d, varies from 0.02 in (0.5 mm) for #24 gauge to 0.01 in (0.3 mm) for #30 gauge wires.

Crosstalk is one of the major limitations of ribbon cables. Even when carrying relatively slow rise time pulses, such as 10 ns for 20-ft (6-m) distances, the crosstalk can be higher than 30% for standard cables. Fig 5(b) indicates typical forward crosstalk (at the far end) of a ribbon cable driven and loaded by its characteristic impedance.

Typical cable also has limited bandwidth capability, as illustrated by the pulse degradation with the distance

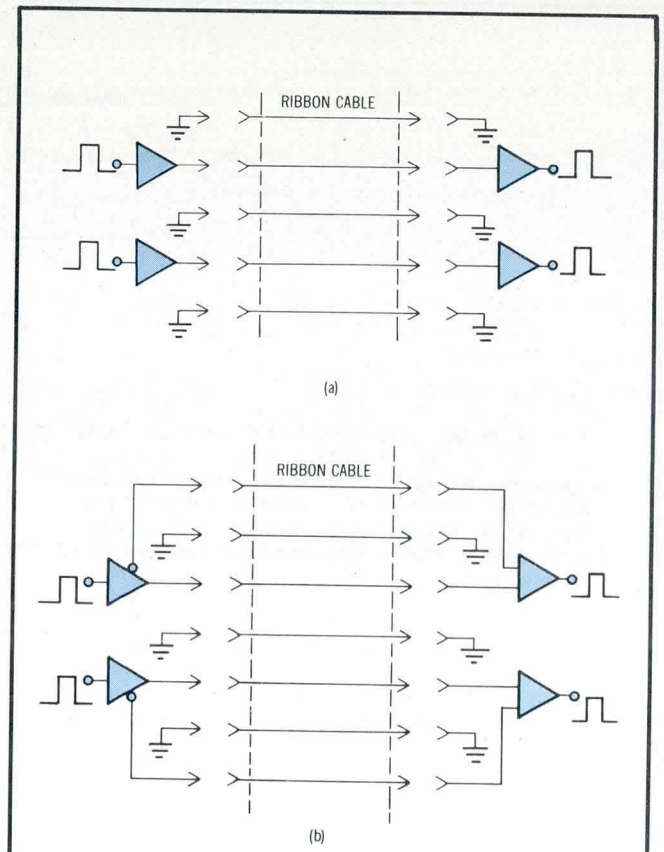
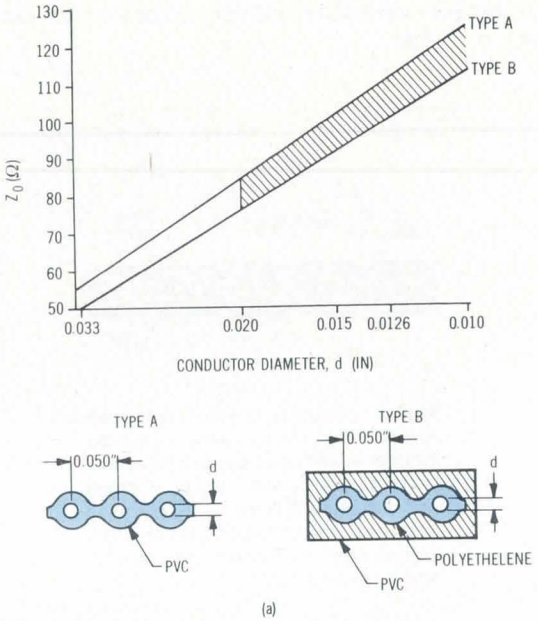


Fig 4 Ribbon cable controls path spacing and length. Alternating signal and ground return lines give ribbon cable closely constrained characteristic impedance and low crosstalk for single-ended drive (a) and differential drive (b) applications

transmitted, shown in Fig 5(c). Note that the rise time of a 1-ns driving pulse is severely degraded at 10 ft (3 m). Yet, even in this case, standard ribbon cable can be useful for short distances. Flat ribbon cables with dual dielectrics can significantly reduce the flat cable crosstalk.[3]

Unless both the wire and the twisting are subjected to close tolerance, twisted cable has the disadvantage of a lower control on its characteristic impedance and actual signal path length variations that introduce the possibility of pulse skewing. Characteristic impedance for twisted pair cable is about 100 to 120 Ω. These cables offer excellent shielding characteristics from low frequency external fields, but are little better than cabled wire pairs in their susceptibility to crosstalk. Although they are acceptable for single-signal applications, they are not recommended for parallel data transmission.

Special ribbon and flat, flexible cables meet requirements for transmission characteristics in high performance systems, which can be divided into two basic classes: those with flat wide conductors (sometimes including a parallel signal ground), and those with a surrounding shield for the signal conductor (coaxial cable). Cables with flat conductors are referred to as flexible



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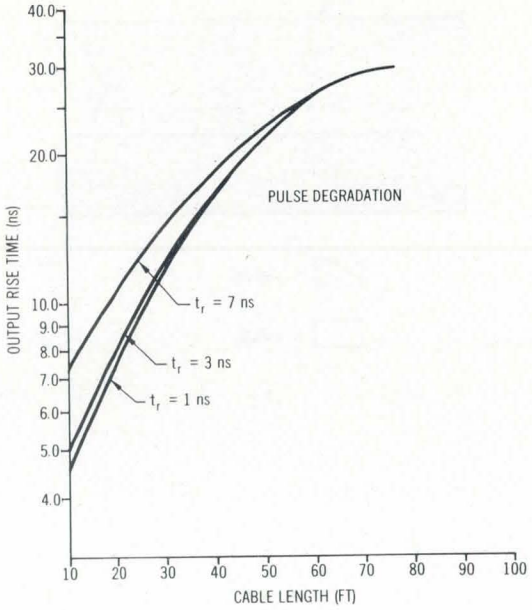

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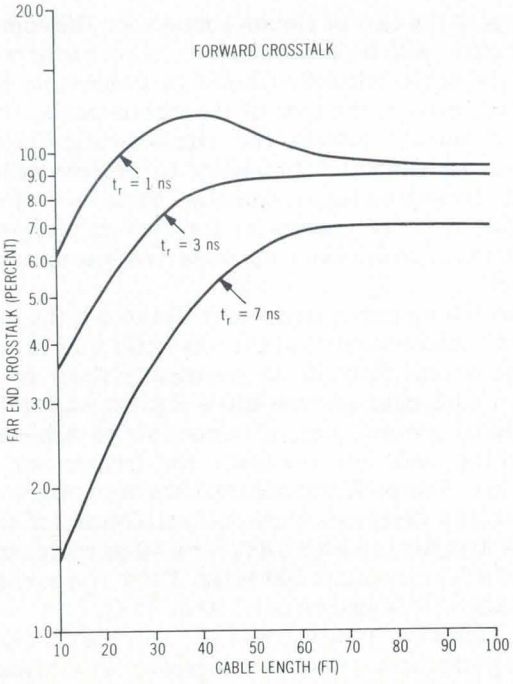
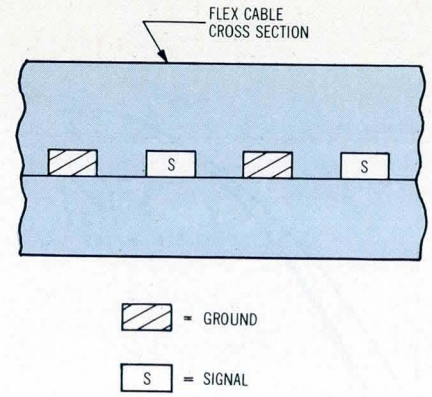


(b)

Fig 5 Ribbon cable properties. Graph in (a) plots characteristic impedance of unshielded ribbon cable as function of conductor size. PVC covering on clad ribbon cable increases dielectric constant and lowers characteristic impedance. Graph (b) plots ribbon cable crosstalk as function of cable length for 1-, 3-, and 7-ns rise times. In contrast, 20 ft of standard cable can have 30% crosstalk for rise times as slow as 10 ns. Graph (c) shows limited bandwidth of ribbon cable by plotting output rise time as function of cable length for 1-, 3-, and 7-ns input rise times. Here, in only 10 ft, 1-ns pulse suffers substantial degradation

transmission cables. They consist of etched copper on polyester film, and can have a parallel set of ground returns or a ground plane placed opposite them. Characteristic impedances of the etched copper cables range from 30 to 150 Ω. (See Fig 6.) Flat construction permits excellent control over the cable characteristics, and the square shape yields a lower attenuation factor. At high frequencies, the signal current tends to flow near the outside surface of the conductor (skin effect), and the square shape represents a surface area significantly larger than that of a round wire.

Coaxial cable performs even better than special ribbon and flat, flexible cable. Normally, the space required by individual connectors, in addition to the cost to assemble them, eliminates coaxial cable from consideration for parallel data systems, but ribbon coaxial cable with companion connectors creates a viable solution to these drawbacks. Manufactured with characteristic impedances of from 50 to 95Ω, cables are available with from 6 to 26 signal paths. A parallel



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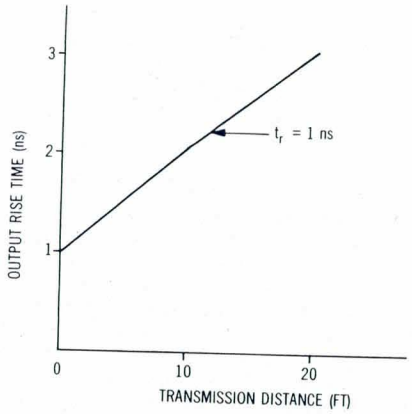

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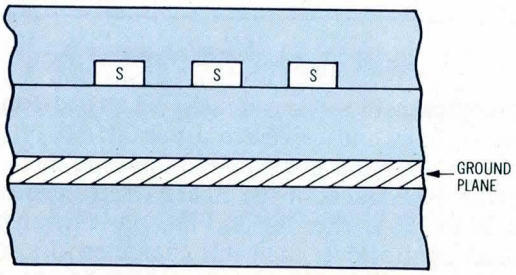


(c)

Fig 6 Flexible cable lowers degradation and crosstalk. Skin effect of square shape (a) reduces attenuation, and controlled rf properties increase bandwidth, causing less distortion of leading edges when high speed pulse travels relatively long distance (b). In (c), addition of ground plane reduces crosstalk to less than 4% for 10-ft cable carrying pulse with only 1-ns rise time

coaxial cable with full shield coverage appears in cross section in Fig 7. When examining the characteristics of a 10-ft (3-m) section of 50- and 91-Ω cable, very low forward crosstalk (less than 0.1% and 0.8%, respectively), and only a small amount (400 ps) of rise time degradation, are evidenced at input pulse times of 1 ns. Separate coaxial cables on individual connectors would perform as well or better.

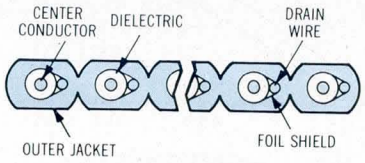


Fig 7 Coaxial cable achieves lowest degradation and crosstalk. However, cost and space considerations may preclude its use. Ribbon coaxial cable shown here performs nearly as well at lower cost and has companion connector to reduce space requirements

Connectors

Except in the case of ribbon connectors, the companion connector will be determined in accordance with the type of cable selected. Choice of connectors may be limited, even in the case of the ribbon cable, since the design must maintain the characteristic impedance across the connector boundary to prevent reflections from discontinuities. Generally, cable manufacturers provide matched connectors for their cables, and they sometimes furnish low cost, mass terminating capability as well.

Shortening transmission path distance is the best way to limit discontinuities at the connector interface. If the signal is sent through an electrically short connector with a controlled spacing and dielectric, and with nearby signal ground pins, it is possible to achieve good matching and low crosstalk for frequencies up to 10 GHz. This performance level has been obtained with a specially designed, chevron type connector that exhibits matching to within 4% for a 70-ps pulse, with less than 10% crosstalk at 100 MHz. These connectors have characteristic impedances of 50 or 75 Ω.

If connector impedance is not specifically matched, good performance may be achieved at wide bandwidths with the use of compensating pads on the PC board that receives the signal. At sufficiently low frequencies, the pins on the connector generally appear to be inductive, hence a capacitance pad on the PC board can add reactance to compensate for, or tune out, pin inductance using TDR method. Since a connector often represents a discontinuity in a transmission line, it is frequently measured using this technique to tune circuit

performance. A connector can compensate for the transition from coaxial cable to a PC board; signal returns are placed adjacent to the signal connector pin and soldered to the ground plane via plated-through holes. Fig 8(a) shows the measured reflection coefficient (degree of match) of a connector system before compensation. The large peak indicates the inductance of the pin section. Notice that two input signal rise times were used in the measurement, 650 ps and 350 ps. Since the 350-ps trace contains more high frequency components, it shows a greater mismatch in the region of the connector and higher resolution. Fig 8(b) shows the results of the compensated system; the reflection coefficient approaches 0 (a perfect match) more closely, even for the 350-ps exciting pulse. At this point, the connector has achieved the capability of a matched bandwidth of at least 500 MHz.

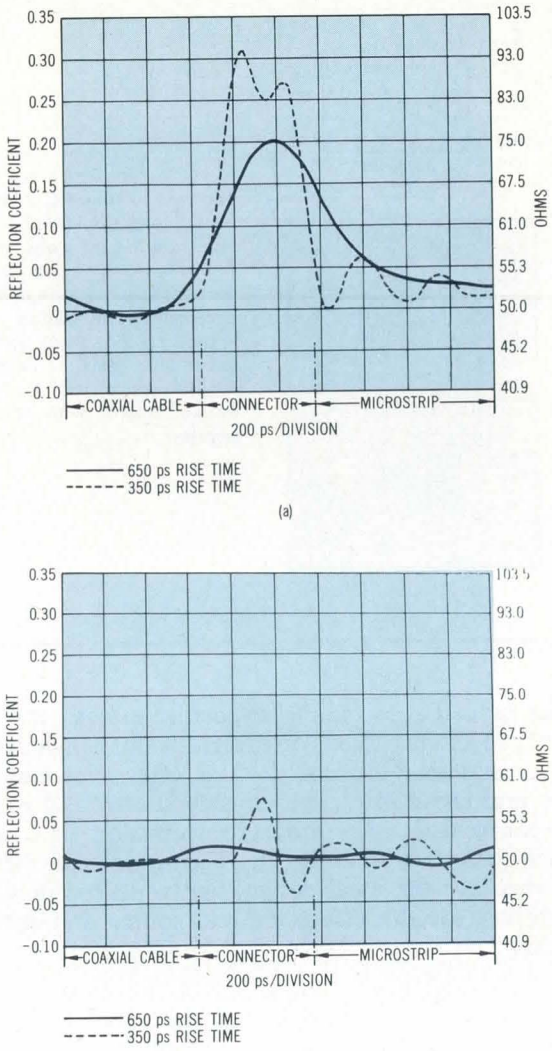


Fig 8 Connector compensates for impedance mismatch. Connector is used to compensate for mismatch at transition from coaxial cable to PC board. In (a), TDR plot before compensation, peaks resulting from connector pin inductance are shown. In (b), TDR plot of matched configuration shows effect of capacitance added to overcome pin inductance, achieving almost perfect match

PC Board

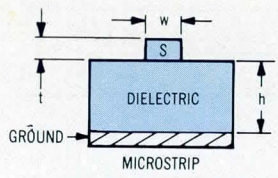
Microstrip transmission line technique is implemented on a 2-sided PC board by placing a ground plane on one side of the board, and a trace over it. By varying the trace width, and considering trace thickness, board thickness, and the dielectric constant of the board, the designer can create a practical transmission line. The approximate width of trace required to achieve a given characteristic impedance is illustrated in Fig 9, which shows trace requirements for the two standard board thicknesses of 0.06 in (2 mm) and 0.03 in (0.8 mm) on G-10 epoxy and 1-oz copper.[4] For 2-oz copper, the traces required are slightly narrower. Because the copper is not immersed in a constant dielectric, simple predicting equations for microstrip are relatively inaccurate. Often, the dielectric constant is not known beforehand; designers must experiment by building up simple transmission sections using known boards and traces, then fine tuning them by the TDR method for use in a critical application.

One interesting note is the rather large size of traces required for the thicker boards. For example, for a characteristic impedance of 50 Ω and a 0.06 in (2-mm) thick board, a 0.1-in (3-mm) trace is required. An 8-bit bus of such traces, separated for crosstalk, would occupy considerable board area. For this reason, and because of the physical constraints of other interconnection elements, designers tend to choose the highest target system characteristic impedance consistent with practical board fabrication techniques, crosstalk, and other interconnection limitations.

It is possible, by using at least a 3-layer board, to achieve a more predictable transmission line with the stripline approach (Fig 10). Striplining requires a ground plane on both sides of a conducting trace, thus immersing the trace in a constant dielectric, and making prediction easier. In the PC board, the trace lengths will determine the delay of the signal pulse; this effect can also become critical in high performance systems. For example, if the delay is about 150 ps/in, differences in the trace lengths of 1 in (25 mm) will produce skewing of 150 ps.

Thus, the designer must select a characteristic impedance for the board traces, make the traces as short as possible with sufficient separation to avoid crosstalk, and keep their lengths approximately the same for parallel signals. Stripline techniques, and even separate power distribution layers, will minimize power supply noise problems.

Although this discussion assumes that all lines in the parallel data system are driven by steps from a driver of the characteristic impedance and a receiver loaded by its characteristic impedance, real drivers, in practice, have ringing and do not necessarily present the desired output impedance. Resistors used for matching can have either



Z_0 (Ω)	LINE WIDTH, w (THOUSANDTHS OF IN)	
	0.06" BOARD	0.03" BOARD
50	103	47
55	89	41
60	77	35
65	66	30
70	57	26
75	49	22
80	42	19
85	36	16
90	31	14
95	27	11
100	23	10

Fig 9 Microstrip transmission line approach. Trace thickness (t), width (w), board thickness (h), and dielectric constant determine microstrip properties; approximate characteristic impedance is listed as function of trace width for two common thicknesses of G-10 epoxy board with 1-oz copper

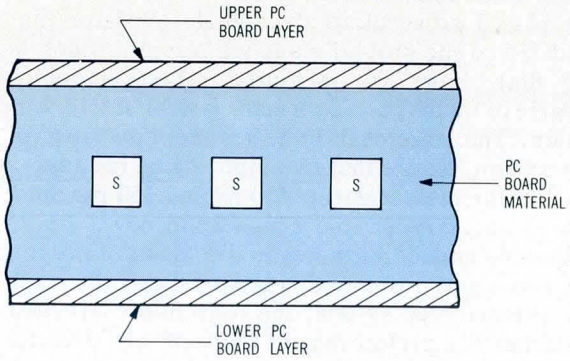


Fig 10 Stripline approach. Positioning ground plane on both sides of signal trace gives more predictable transmission line performance and better shielding, but at significantly higher cost because it requires multilayer board

series inductive or parallel capacitive effects. ICs have input capacitance that is often significant in high performance systems.[5] Normally, these effects increase rise time and crosstalk design considerations, and require the fabrication of a model transmission path upon which to base a final design. The system can then be matched for the ideal design, and observed in actual operation for the effects of real source and receiver loading.

Summary

Design plans for high performance, parallel data systems can compensate for the problems induced by increased transmission bandwidth. The process is lengthy and complex, and should be started early in the project. After characteristic impedance, attenuation, and crosstalk parameters have been traded off, and cables, connectors, and PC board layouts selected, a model transmission system should be established. The TDR technique will help the designer to obtain good, matched performance, and attain his final system design goal.

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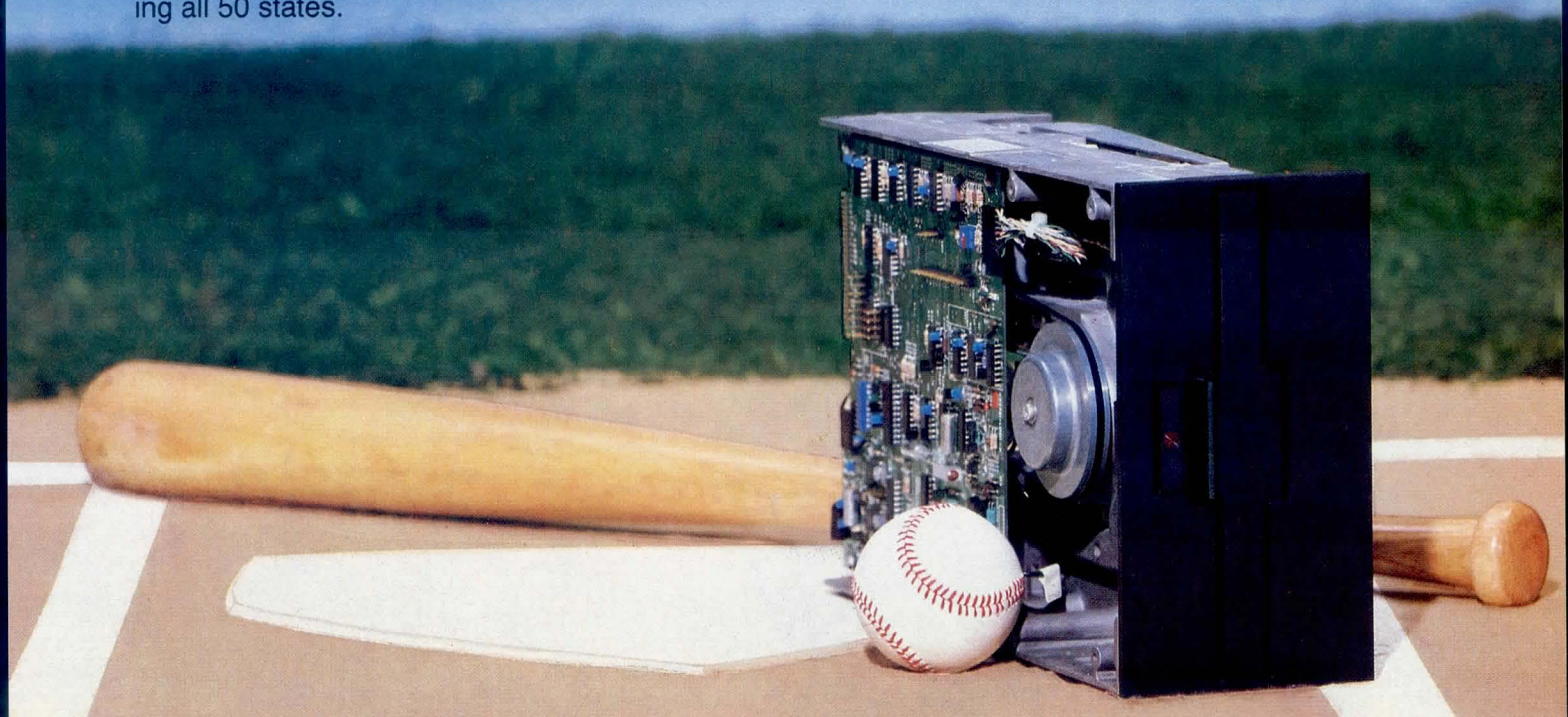

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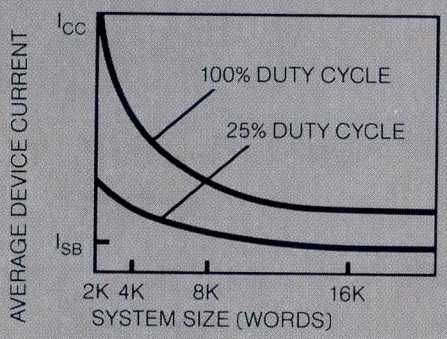

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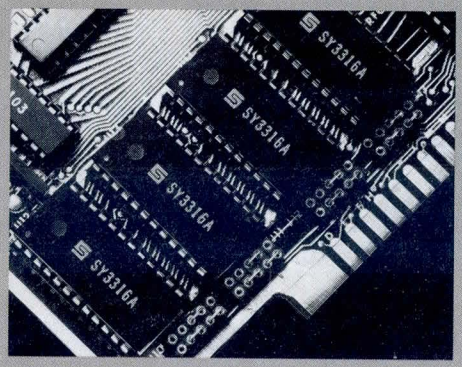

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SY3316A 20mA standby

FEATURE

LOGIC ANALYZERS SIMPLIFY SYSTEM INTEGRATION TASKS

Inexpensive resource isolates and solves typical system integration problems by recording logic states and realtime data simultaneously. When erroneous data identify an error, associated logic state information helps to pinpoint its cause

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One of the most frustrating tasks for the digital designer can be the integrating of hardware and software. At this critical stage in the design phase, problems often require many man-hours to locate and correct simply because of difficulty in identifying their source. Integration can be especially difficult when, as many applications require, the prototype system must operate in real time.

In the early phases of a microprocessor based design project, system performance objectives are defined in accordance with the constraints that govern both the hardware and software sectors of the project. Working within these constraints, the hardware and software design teams attempt to create respective designs that approximate the performance definition as closely as possible. At some point, these parallel design efforts must intersect, and then the software must begin to be exercised on the prototype hardware to verify that the system is performing as intended. Commonly known as hardware/software integration, this process often consumes half the total design time.

During the integration process, it is almost inevitable that design flaws will surface to prevent the system from meeting performance expectations. These flaws occur because the original hardware and software design constraints are of necessity generalized; the many smaller elements that might influence the final performance outcome at integration time cannot be foreseen. The flaws may be hardware related, software related, or a combination of both, and debugging, the process of isolating and correcting the flaws, must take place throughout the integration process.

In-circuit emulation, a common debugging method, employs an emulator processor to execute the developed software. However, in order to extract debugging information during execution of the prototype program, it is necessary to insert wait states that take the execution out of real time. Unfortunately, realtime operation is often essential to locate many software and hardware anomalies.

Hardware/Software Integration Technique

Some microprocessor development aids have special provisions for realtime debugging, but only at considerable expense. A less costly alternative is the logic analyzer, which allows the sampling of realtime information off the prototype's address, data, and control buses. Ideally, the logic analyzer allows two types of data acquisition. The first, synchronous acquisition of logic states, allows an examination of software flow in

the manner that it is actually executed. Synchronous data are transmitted and received over the microprocessor system bus on edges of regularly recurring control signals supplied by a clock that is part of the system under test. This clock signal is used by the logic analyzer to sample data into memory. When recalled for display, the stored information gives an accurate picture of synchronous data flow as it originally occurred on the system bus.

Asynchronous acquisition, the second type of data acquisition, allows an examination of individual logic levels at time points other than the system clock edge. It is accomplished by sampling with a clock that is part of the logic analyzer and therefore independent of the system under test. Using this technique, it is possible to observe signal anomalies that would have remained undetected unless they had occurred on the system clock edge. In addition, it is possible to observe the timing relationships between logic level transitions on the control lines of the processor under test.

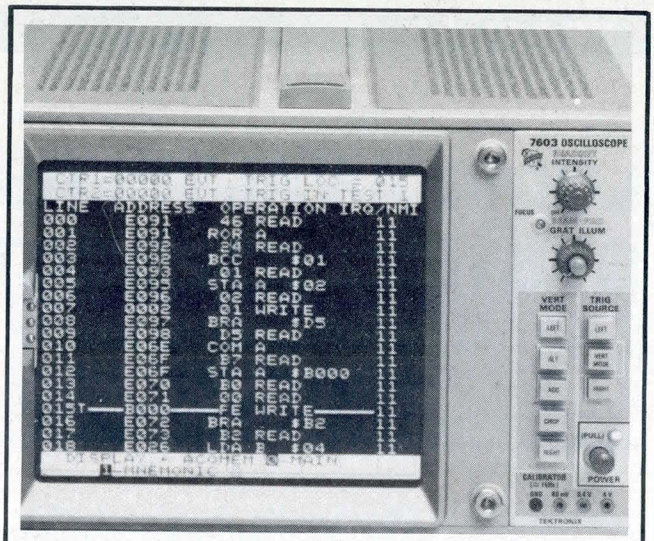
For this example, a Tektronix 7D02 logic analyzer is used. In the synchronous mode, the analyzer acquires and stores up to 44 channels of state information. Through the use of a series of personality modules this information can be disassembled into an alphanumeric display that shows each bus transaction in mnemonics native to the processor under test [Fig 1(a)].

To acquire specific state information, the analyzer's resources, which include four independent word recognizers and two programmable general purpose counters, are configured through a unique programming language. (Each word recognizer identifies a user specified 48-bit bus state; each counter can count either time or discrete events; and, via the logic analyzer programming language, the counters can be dynamically reset and/or stopped.)

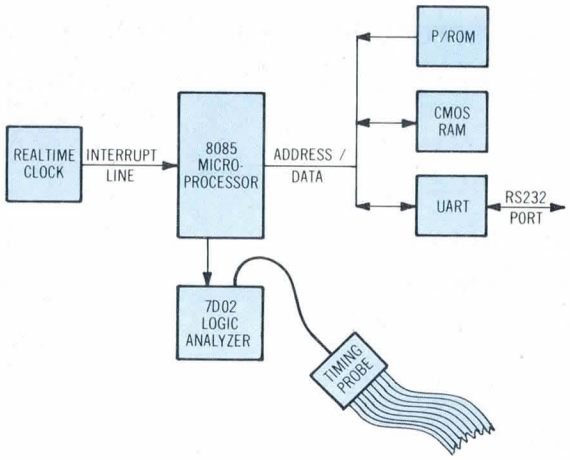
Using the programming language, the user can initiate the two basic operations involved in data acquisition: triggering, which halts the flow of test data through the logic analyzer's memory to accomplish the retention of pertinent information; and data qualification, which investigates the parameters of each bus event and then makes a decision whether or not to commit this information to the logic analyzer's memory.

In the asynchronous mode, the logic analyzer has a timing option that allows the acquisition of eight channels of timing data. Data storage can be triggered by the resources of the synchronous section or by the timing option's own independent word recognizer. Glitch triggering is included for the detection of transient signal anomalies. Alternately, the timing option's eight channels can be used by the synchronous section in addition to that section's normal complement of channels.

A simple, general purpose microcomputer system, made up of an 8085 microprocessor, a programmable read only memory (P/ROM) that contains the developed software, a complementary metal oxide semiconductor random access memory (CMOS RAM) for data manipulation during program execution, and a serial, asynchronous input/output (I/O) port, illustrates some typical debugging problems and their solutions. The system is interrupt driven and employs a realtime clock [Fig 1(b)].



(a)



(b)

Fig 1 Typical setup for system integration. Logic analyzer (a) implements unique programming language used to configure resources. System under test (b) incorporates 8085 microprocessor, P/ROM, CMOS RAM, and asynchronous serial I/O port. Microprocessor is removed from test system and inserted in logic analyzer personality module. Then, personality module attaches to microprocessor socket in test system. Timing probe connection depends on test being performed

Since integration and debugging are usually accomplished in ascending stages of complexity, in this application's first stage, I/O and interrupts are disabled and focus is on confirming the operation of the processor and the ability of individual memory locations to respond to the processor.

System Hardware Verification

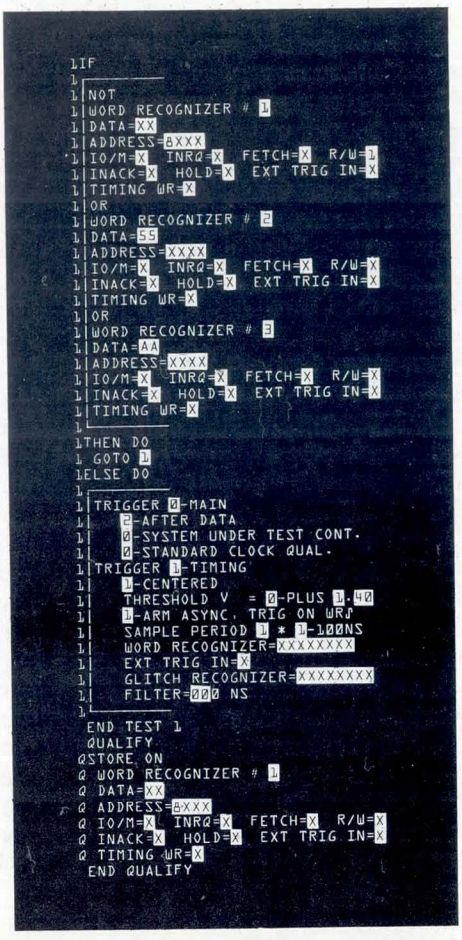
When developing system hardware, one of the first tasks is to verify the correct operation of a central processing unit (CPU) kernel, which can then be used as a

foundation in subsequent hardware and software testing. This kernel usually consists of the microprocessor unit, RAM, ROM, and their connecting circuitry. To verify the RAM portions of the CPU kernel, a software test package is used that contains a specific read/write routine. This routine exercises the RAM by writing a 55 (all addresses and data are in hexadecimal) to the first location in RAM and then immediately reading that same location. Next, the routine writes an AA to the same location and then reads it back. The routine increments the address location; and this double read/write cycle repeats until all RAM locations have been checked. In this particular system, the RAM address space is from 8000 to 8FFF.

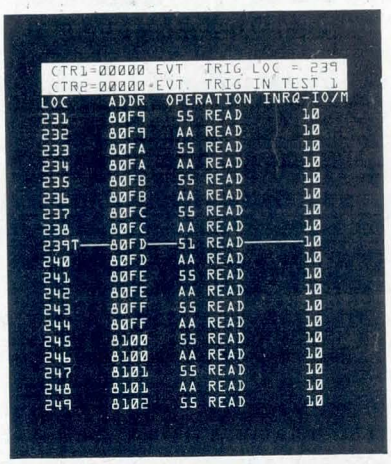
The software test package is designed to exercise the RAM in a worst case mode, with the CPU kernel running at full speed and continually calling upon the RAM for service. This mode is the one most likely to reveal any unforeseen hardware anomalies, such as timing problems or noise glitches. However, it does require realtime execution, as no software checking or wait states are added to the routine's normal running time. Here the logic analyzer becomes a convenient tool because it allows the test software to exercise the hardware at full speed while permitting the user to capture any abnormal activity occurring during the process.

Fig 2(a) shows the program used to monitor the RAM test routine during realtime execution. In this case, the most convenient solution is to describe the absence of an error condition (a cycle in which there is either no RAM read or the value read is 55 or AA) and to trigger the synchronous and timing sections when an error condition exists. Brackets in the program indicate that the analyzer will look for these conditions simultaneously on each bus cycle; the qualify block provides that only data reads in the RAM address range are committed for storage and display.

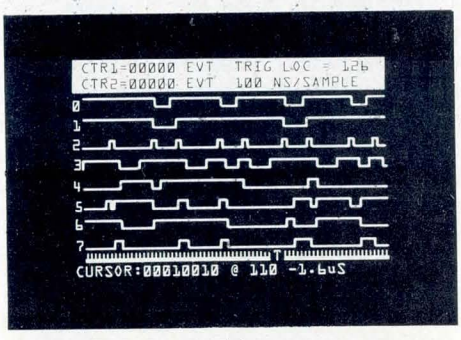
To begin the RAM test, the analyzer is connected to the prototype's address, data, and control buses. The software test package is then executed repeatedly on the



(a)



(b)



(c)

Fig 2 RAM exerciser. Reading and writing RAM at high speeds tests worst case operation in real time. Program in (a) captures hardware anomalies. In (b), read error is marked by horizontal bar. Vertical cursor in (c) marks point where same read error also triggered analyzer timing section. Here, state section detects error and timing section supplies data to isolate its cause

prototype while the analyzer monitors all bus activity. Once the prototype warms up, the analyzer triggers, indicating a RAM failure. Fig 2(b) shows the resulting display of RAM read cycles leading to the trigger.

Next, the data acquired by the asynchronous timing section should be checked. Fig 2(c) shows the display produced by the timing section, which was triggered at the same time as the state section. The display uses a timing diagram format and shows the read/write operation of the RAM. The channels represent the following signals:

- Ch 0 - $\overline{CE}$ (chip enable)
- Ch 1 - $\overline{WE}$ (chip write enable)
- Ch 2 - ALE (CPU address latch enable)
- Ch 3 - $\overline{RD}$ (CPU read)
- Ch 4 - AD0
- Ch 5 - AD1 } low order
- Ch 6 - AD2 } data lines
- Ch 7 - AD3

Channel 2 (ALE) defines the start of each 8085 cycle, and channel 3 ($\overline{RD}$) determines when the 8085 is reading data. Channel 0 ($\overline{CE}$) determines when the RAM chip is being accessed; channel 1 ($\overline{WE}$) indicates whether it is being read or written. Investigating the area around the cursor, it is evident that the 8085 reads binary 1 (channels 4 to 7) instead of the anticipated binary 101 from the RAM in question.

In this example, the RAM latches the address off the bus with the falling edge of the chip enable ($\overline{CE}$), allowing the output buffers to drive the data bus for the subsequent read cycle. By examining the timing relationship between ALE and $\overline{CE}$ and associating it with the erroneous read in the four data lines on the bottom of the display, a violation of the chip manufacturer's specification for address setup and hold is discovered.

Using the logic analyzer's combination of state and timing sections saves a great deal of time when tracking down an intermittent system fault, such as the one just described. Normally, this procedure would be a 2-step process. First, there would be a software search using synchronous data sampling to find the approximate fault location. Once it was found, the observed state parameters would be used to build a trigger for asynchronous sampling to trace the problem back to its hardware source. Here the process is reduced to a single step since the main (state) acquisition section can locate a software anomaly and then trigger both itself and the timing section. With data being acquired from two sections, the user can look at both the hardware and software sides of system bus events occurring during a single time window.

Solving an Interrupt Problem

Next in the process is the debugging of the system's interrupt mechanism. In this particular system, the interrupt mechanism consists of a realtime clock interrupting the processor every 30th of a second, causing the processor to begin execution at location 002C. A small amount of test code must be written to help determine whether the clock is operating properly:

```
        ORG     0
        MVI     A, 0E
        SIN
        EI
HERE    JMP     HERE

        ORG     2C
        EI
        RET
```

This code, written in 8085 assembly language, establishes a brief interrupt routine that executes in response to the realtime clock interrupt. The first four lines initialize the conditions for the interrupt; the fifth line sets up a repetitive cycle that continues until an interrupt occurs. The last three lines make up the interrupt handler, which should execute each time the processor receives the realtime clock signal.

This test code will run long enough to establish the accuracy of the clock. During this period, the logic analyzer can be programmed to perform two separate tasks while monitoring program execution: establish and measure the realtime period, and count the number of interrupts processed during this period. The time period selected is 65.5 s, which corresponds to 65,534 ms, the maximum value for one of the counters. If the realtime clock is operating properly, there should be about 1966 interrupts during this period.

Fig 3(a) shows the program used to accomplish the timekeeping and counting functions. In TEST 1, CTR1 is initialized and set to run in milliseconds. TEST 2 establishes a trigger at the end of the time period and uses CTR2 to count the number of interrupts based on the appearance of the interrupt vector (002C) on the system address bus.

The test code is run and the analyzer captures the results shown in Fig 3(b). Pertinent is the information in the reverse video field at the top of the display. Here we see that the test code ran for the anticipated time period (CTR1 = 65,534 ms), and that a correct number of interrupts occurred during this period (CTR2 = 01965 EVT). If the CTR2 value had been less, the clock would have been running slow. If the value had been more, the clock would have been running fast or there would have been glitches on the line. The analyzer's timing option can be used to trigger on glitches on the interrupt line with the sampling rate set slightly faster than the interrupt.

If it is found that there is a problem with the interrupts, the analyzer can determine the amount of time that elapses from the point at which the interrupt is requested until the interrupt service routine begins (this should be a few microseconds. Or, the analyzer can determine the time between interrupt requests (33 ms) and the length of time spent executing the interrupt service routine. If this takes longer than 33 ms, interrupts will be missed.

System Software Integration

The basic hardware kernel is now debugged, and software modules are to be added in small increments, starting with the main software kernel, until the system is complete. In most cases, each section of code is de-

```
 TEST 1
1ELSE DO
1
1┌──────────
1│COUNTER # 1 2-MS
1│   0-RUN
1│GOTO 2
1└──────────
 END TEST 1
 TEST 2
2IF
2 COUNTER # 1 = 65534 2-MS
2THEN DO
2 TRIGGER 0-MAIN
2    2-ZERO DELAY
2    0-SYSTEM UNDER TEST CONT.
2    0-STANDARD CLOCK QUAL.
2OR IF
2 WORD RECOGNIZER # 1
2 DATA=XX
2 ADDRESS=002C
2 IO/M=X  INR0=X  FETCH=1  R/W=X
2 INACK=X  HOLD=X  EXT TRIG IN=X
2 TIMING WR=X
2THEN DO
2 COUNTER # 2 0-EVENTS
2    0-INCREMENT
 END TEST 2
```

(a)

```
CTR1=65534MS    TRIG LOC =255
CTR2=01965 EVT  TRIG IN TEST 2
LOC    ADDR  OPERATION INR0-IO/M
239    0006   00 READ      00
240    0004  JMP  0004H     00
241    0005   04 READ      00
242    0006   00 READ      00
243    0004  JMP  0004H     00
244    0005   04 READ      00
245    0006   00 READ      00
246    0004  JMP  0004H     00
247    0005   04 READ      00
248    0006   00 READ      00
249    0004  JMP  0004H     00
250    0005   04 READ      00
251    0006   00 READ      00
252    0004  JMP  0004H     00
253    0005   04 READ      00
254    0006   00 READ      00
255T---0004---JMP  ****H-----00
```

(b)

Fig 3 Interrupt system verifier. In (a), first test routine establishes a timer (CTR1), and second test routine counts interrupts (CTR2) during established time period. Result in (b) verifies that expected number of interrupts was serviced in established time period. Lower value for CTR2 might show that interrupts were missed. Higher value might indicate glitches on interrupt line

bugged independently: inputs to the code are simulated using software test stubs; outputs are verified for accuracy using the logic analyzer. Modules, once debugged independently, are integrated and debugged together. Once again, accuracy is verified using the logic analyzer. This step is repeated until all modules are integrated into the system.

When bringing up the software, there are several problems that normally occur. Occasionally, when new code is added, the processor begins executing outside of the address space occupied by the code. Data may be executed as instructions (causing the processor to perform random operations), or subroutines may be called incorrectly. Causes of these problems can be detected by defining the address range in which the processor should be executing and triggering when the processor fetches an opcode from outside the defined range.

Fig 4(a) shows a simple program used to detect code that is executing outside the prototype system's normal address space. The word recognizer is set to trigger on any address between 8000 and FFFF, which would represent a violation of the code's normal address range. (Here the address bus value is entered using a binary radix format.) Fig 4(b) shows the results and reveals the point at which the code began to execute erroneously—address 8126. The *** indicates an illegal opcode.

Another cause for software failure can be a subroutine that is called out of order, even though it may be validly called in the program in response to a different input. In this prototype system, there is a subroutine starting at the address 2870 that is occasionally called at the wrong time in the program. In order to be called correctly, this subroutine must be summoned by an instruction located at 7500. A call from any other location is incorrect.

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX
1 ADDRESS=1XXXXXXXXXXXXXXX
1 IO/M=X  INR0=X  FETCH=1  R/W=X
1 INACK=X  HOLD=X  EXT TRIG IN=X
1 TIMING WR=X
1THEN DO
1 TRIGGER 0-MAIN
1    2-AFTER DATA
1    0-SYSTEM UNDER TEST CONT.
1    0-STANDARD CLOCK QUAL.
 END TEST 1
```

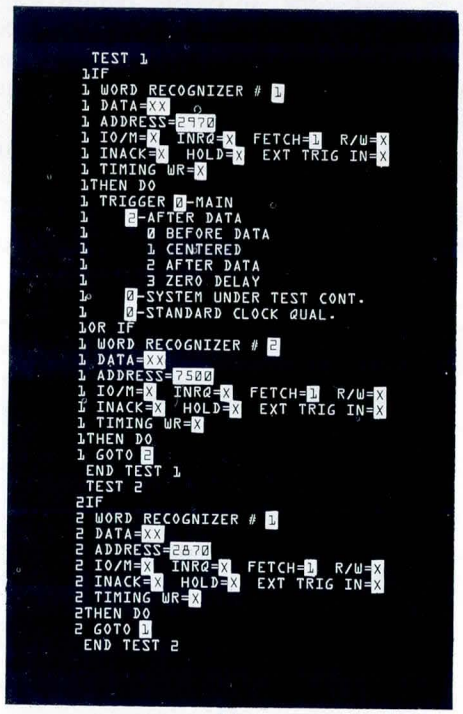
(a)

```
CTR1=00000 EVT  TRIG LOC = 239
CTR2=00000 EVT  TRIG IN TEST 1
LOC    ADDR  OPERATION INR0-IO/M
229    2006  LXI  H,3126H  00
230    2007   26 READ      00
231    2008   31 READ      00
232    2009  STA  8200H     00
233    200A   00 READ      00
234    200B   82 READ      00
235    8200   00 WRITE     00
236    200C  MVI  H,81H     00
237    200D   81 READ      00
238    200E  PCHL           00
239T---8126---***  {CB}-----00
240    8127  NOP            00
241    8128  DAD  SP        00
242    8129  NOP            00
243    812A  DAD  SP        00
244    812B  NOP            00
245    812C  DAD  SP        00
246    812D  NOP            00
247    812E  DAD  SP        00
```

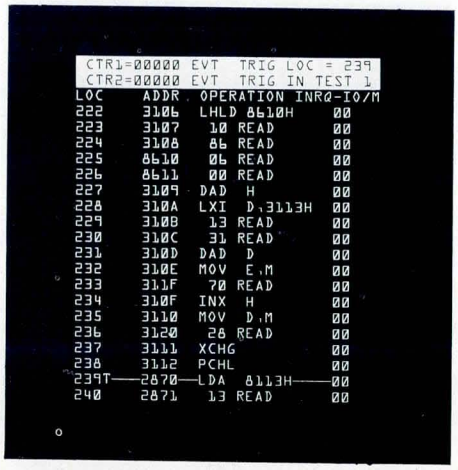
(b)

Fig 4 Address space monitor. Analyzer program in (a) triggers on any attempt to execute instructions above address 8000, capturing wild program branches into data storage portion of memory. In (b), bar shows where program branched to 8216. Asterisks indicate illegal operation code where data word was fetched as instruction

In Fig 5(a) the program locates the faulty subroutine call, using two tests to create a loop that searches for address 2870 and triggers on this event when it is not preceded by address 7500. Fig 5(b) shows the resulting data display, with the trigger on address 2870. The code preceding the trigger is a case statement with an incorrect case variable, 0006, combined with another value to form a pointer into a branch table. The resulting pointer is wrong and causes the program to go astray by jumping to the wrong subroutine.



(a)



(b)

Fig 5 Test of subroutine calling sequences. Analyzer program in (a) triggers when subroutine is called incorrectly. Here, subroutine at address 2870 must be called from address 7500. In (b), invalid call from address 3100 triggers analyzer. Display shows cause of error—incorrect case variable used to form branch table offset

A more complex problem would be a subroutine returning to an invalid address. This could be caused by an erroneous value on the stack and can be detected by triggering on writes to the stack between the call to the subroutine and subsequent return. In this system, there is a subroutine that begins at address 1532 and ends at 1602. Addresses 8770 and 8771 are the stack locations where the subroutine return address is located. The object is to determine whether or not these stack locations are being corrupted during the execution of the subroutine.

In Fig 6(a), the program used to solve the problem, TEST 1 recognizes the start of the subroutine and branches to TEST 2, where the trigger is activated if either of the stack locations is modified. If not, TEST 2 contains an alternative branch that recognizes the end of the subroutine and branches back to TEST 1, which watches for the next occurrence of this particular subroutine. Fig 6(b) shows the data acquired by the program, which was triggered on a write to one of the stack locations during execution of the subroutine. The preceding code shows that the erroneous write was caused by a pointer, 8228, indicating that the stack location, 8771 was the destination for a data byte, 21.

If the subroutine calls other subroutines, it may be necessary to qualify on writes to the stack and on the location doing the writing to see if there is anything out of the ordinary. This problem can be caused by an indexed write out of range (writing over the stack rather than to the appropriate memory location), too many parameters pushed on the stack by the calling routine, or a bad memory location, and can be detected by the logic analyzer.

The analyzer can also be used for performance analysis. Word recognizers manipulate the counters to determine the percentage of time out of the total time to perform a task that the processor is spending to execute different sections of code. Finding the slower sections of code and refining the percentages allows inefficient or time critical sections of code to be optimized to make the total system faster. This speed is important to systems in which the software must respond to the hardware within a minimum amount of time.

Integrating Peripheral Devices

As the main operating system is brought up, driver routines—software modules used to directly control the hardware—can be added to perform such tasks as the manipulation of the internal registers of a peripheral interface chip. As adequately testing the driver routines may require complex inputs or handshaking, it is usually easier to add the drivers at this point and debug them rather than debug them independently.

Peripheral hardware is now integrated into the system. In this system, the RS-232 port is tested along with its interaction with the rest of the system. It presents an integration challenge because it is parallel synchronous on the processor side of the interface [the universal asynchronous receiver transmitter (UART)] and serial asynchronous on the other side. The RS-232 system and UART are further complicated because they

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX
1 ADDRESS=1532
1 IO/M=X  INRQ=X  FETCH=1  R/W=X
1 INACK=X  HOLD=X  EXT TRIG IN=X
1 TIMING WR=X
1THEN DO
1 GOTO E
 END TEST 1
 TEST 2
2IF
2 WORD RECOGNIZER # 2
2 DATA=XX
2 ADDRESS=1602
2 IO/M=X  INRQ=X  FETCH=1  R/W=X
2 INACK=X  HOLD=X  EXT TRIG IN=X
2 TIMING WR=X
2THEN DO
2 GOTO 1
2OR IF
2┌──────
2│WORD RECOGNIZER # 3
2│DATA=XX
2│ADDRESS=8770
2│IO/M=X  INRQ=X  FETCH=X  R/W=0
2│INACK=X  HOLD=X  EXT TRIG IN=X
2│TIMING WR=X
2│OR
2│WORD RECOGNIZER # 4
2│DATA=XX
2│ADDRESS=8771
2│IO/M=X  INRQ=X  FETCH=X  R/W=0
2│INACK=X  HOLD=X  EXT TRIG IN=X
2│TIMING WR=X
2└──────
2THEN DO
2 TRIGGER 0-MAIN
2    2-AFTER DATA
2    0-SYSTEM UNDER TEST CONT.
2    0-STANDARD CLOCK QUAL.
 END TEST 2
```

(a)

```
 CTR1=00000 EVT  TRIG LOC = 239
 CTR2=00000 EVT  TRIG IN TEST 2
LOC    ADDR  OPERATION INRQ-IO/M
232    15F9  LHLD 8228H     00
233    15FA   28 READ       00
234    15FB   82 READ       00
235    8228   71 READ       00
236    8229   87 READ       00
237    15FC  MVI  M,21H     00
238    15FD   21 READ       00
239T---8771---21 WRITE------00
240    15FE  STA  8007H     00
241    15FF   07 READ       00
242    1600   80 READ       00
243    8007   00 WRITE      00
244    1601  EI             00
245    1602  RET            00
246    8770   27 READ       00
247    8771   21 READ       00
248    2127  NOP            00
249    2128  DAD  SP        00
250    2129  NOP            00
```

(b)

Fig 6 Subroutine return conventions. Incorrect stack handling causes failure to return from subroutines. In (a), when subroutine is invoked, TEST 1 branches to TEST 2, which triggers if stack is modified before subroutine return. Display (b) flags occurrence of error and shows that incorrect pointer variable caused it

require handshaking, with some timing constraints, to work properly. The timing option of the logic analyzer is either connected to the serial side of the UART to observe the handshaking and serial I/O or used synchronously on the parallel or processor side to look at the processor interaction in more detail.

With the driver software installed, the logic analyzer is ready to synchronously and asynchronously check the program's effect on system operation. At this point, any number of symptoms and possible causes could become evident.

For example, the system could exhibit erratic communication across the RS-232 port with some characters being received as sent, others not. One possible cause is that the processor is not able to service incoming data as fast as the UART is supplying them. If the processor is busy servicing one character when a new one comes in, the new one may be missed altogether. In testing for this possibility, it is known that the RS-232 serial data speed is 9600 baud. Since the system uses a 10-bit serial character format, the data rate is 960 char/s, giving 1042 μs/char as the maximum amount of service time the processor can spend on one character before it must be ready for the next.

Also, the UART sends an asynchronous interrupt to the processor each time a new character is ready. The processor is able to ignore this interrupt, either through a generalized mask that blocks all interrupts or through a mask specific to this particular line (RESET 6.5). Regardless of these masks, the processor must service the interrupt within the allotted 1042 μs or the next incoming character will overrun the first. Once the interrupt is acknowledged, the software is vectored to the address 0300, the start of the UART service routine.

The object of the test is to search for the asynchronous interrupt and to trigger the first time the processor fails to implement the service routine within the allotted time after it occurs. Accordingly, the state section probes are connected to the system's address and data buses, and channel 7 of the timing section is hooked to the interrupt line. Fig 7(a) is the program used to construct the test. TEST 1 sets channel 7 of the timing word recognizer to look for the interrupt signal. When the interrupt is recognized, CTR1 begins to count the allotted processing time for a single character (1042 μs). At this point, TEST 2 becomes active and provides two alternatives: (1), if the interrupt service routine (0300) begins execution time before CTR1 reaches 1042 μs, the program will loop back and start over; (2) if the counter exceeds the allotted time, the main (state) section will trigger, capturing only data stored prior to the trigger (zero delay).

A qualify block is included at the end of the program and allows only the storage of instruction fetches. By eliminating all operands, it extends the stored data time window considerably while still providing enough information to monitor the code. Fig 7(b) is the data captured by the program. Note that the interrupt request (INRQ) remains high throughout the code, indicating that the interrupt is not being acknowledged. Scrolling back through the stored data reveals that the program error sets the interrupt mask during a subroutine without restoring it prior to returning to the main program.

```
 TEST 1
1IF
1 WORD RECOGNIZER # 1
1 DATA=XX
1 ADDRESS=XXXX
1 IO/M=X  INRQ=X  FETCH=X  R/W=X
1 INACK=X  HOLD=X  EXT TRIG IN=X
1 TIMING WR=1
1     THRESHOLD V. = 0-PLUS 1-40
1    1-ASYNC
1     SAMPLE PERIOD 1 * 1-100NS
1     WORD RECOGNIZER=XXXXXXXX
1     EXT TRIG IN=X
1     GLITCH RECOGNIZER=XXXXXXXX
1     FILTER=000 NS
1THEN DO
1┌──────
1│COUNTER # 1 1-µS
1│   2-RESET AND RUN
1│GOTO 2
1└──────
 END TEST 1
 TEST 2
2IF
2 WORD RECOGNIZER # 2
2 DATA=XX
2 ADDRESS=0300
2 IO/M=X  INRQ=X  FETCH=1  R/W=X
2 INACK=X  HOLD=X  EXT TRIG IN=X
2 TIMING WR=X
2THEN DO
2 GOTO 1
2 COUNTER # 1 = 01042 1-µS
2THEN DO
2 TRIGGER 0-MAIN
2    3-ZERO DELAY
2    0-SYSTEM UNDER TEST CONT.
2    0-STANDARD CLOCK QUAL.
 END TEST 2
 QUALIFY
QSTORE ON
Q WORD RECOGNIZER # 3
Q DATA=XX
Q ADDRESS=XXXX
Q IO/M=X  INRQ=X  FETCH=1  R/W=X
Q INACK=X  HOLD=X  EXT TRIG IN=X
Q TIMING WR=X
 END QUALIFY
```

(a)

```
CTR1=01042 µS   TRIG LOC = 255
CTR2=00000 EVT  TRIG IN TEST 2
LOC    ADDR  OPERATION INRQ-IO/M
238    640F  INX  H        10
239    6410  INX  H        10
240    6411  INX  H        10
241    6412  ADD  M         10
242    6413  STA  ****H     10
243    6416  ANI  **H       10
244    6418  MOV  B,A       10
245    6419  MVI  A,**H     10
246    641B  SUB  B         10
247    641C  STA  ****H     10
248    641F  LDA  ****H     10
249    6422  RRC            10
250    6423  RRC            10
251    6424  RRC            10
252    6425  ANI  **H       10
253    6427  LXI  H,****H   10
254    642A  MOV  E,M       10
255T---642B--INR  E---------10
```

(b)

Fig 7 Debugging an asynchronous serial interface. Test program (a) triggers when processor fails to service interrupt from asynchronous serial interface within allotted time period. Then, data captured in display (b) reveal that program handled interrupt mask incorrectly, causing error in processing subsequent interrupt

Advantages of Combined Logic and State Analysis

Combining state and timing acquisition into one instrument enables the timing section to monitor the hardware and also to interact with the state section, which simultaneously monitors software activity. A logic analyzer of this complexity allows realtime hardware and software verification with minimal time devoted to writing software test code and developing extra hardware to test the system. Designers need to make fewer measurements than when they are using conventional logic analyzer techniques because the sophisticated data qualification and triggering allow specifying in greater detail the exact data needed to solve the problem, thus minimizing the number of passes to be made over the data.

Historically, logic analyzers have been considered hardware debugging tools only, with emphasis placed on the timing section. Now, combining state and timing sections with interactive triggering and including a powerful user language to manipulate the instrument's hardware resources make the logic analyzer an effective tool throughout the integration process.

About the Authors:

Paul Dittman has spent his time at Tektronix, Inc, writing assemblers for the 8002A microprocessor lab in logic development products engineering and co-designing the user interface and firmware for the 7D02 logic analyzer. He has a BS in electrical engineering/computer science from the University of California at Berkeley.

Senior electronic design engineer in logic analyzer engineering, Dennis Glasby has helped design 7D02, 7D01, WR501, and LA501 logic analyzer products, as well as being involved in the 434 and 465 oscilloscope projects. He holds a degree from California Polytechnic State University.

Chris Benenati, a software engineer, works on logic analyzers at Tektronix, Inc. He received an AB and an ScM in computer science from Brown University.

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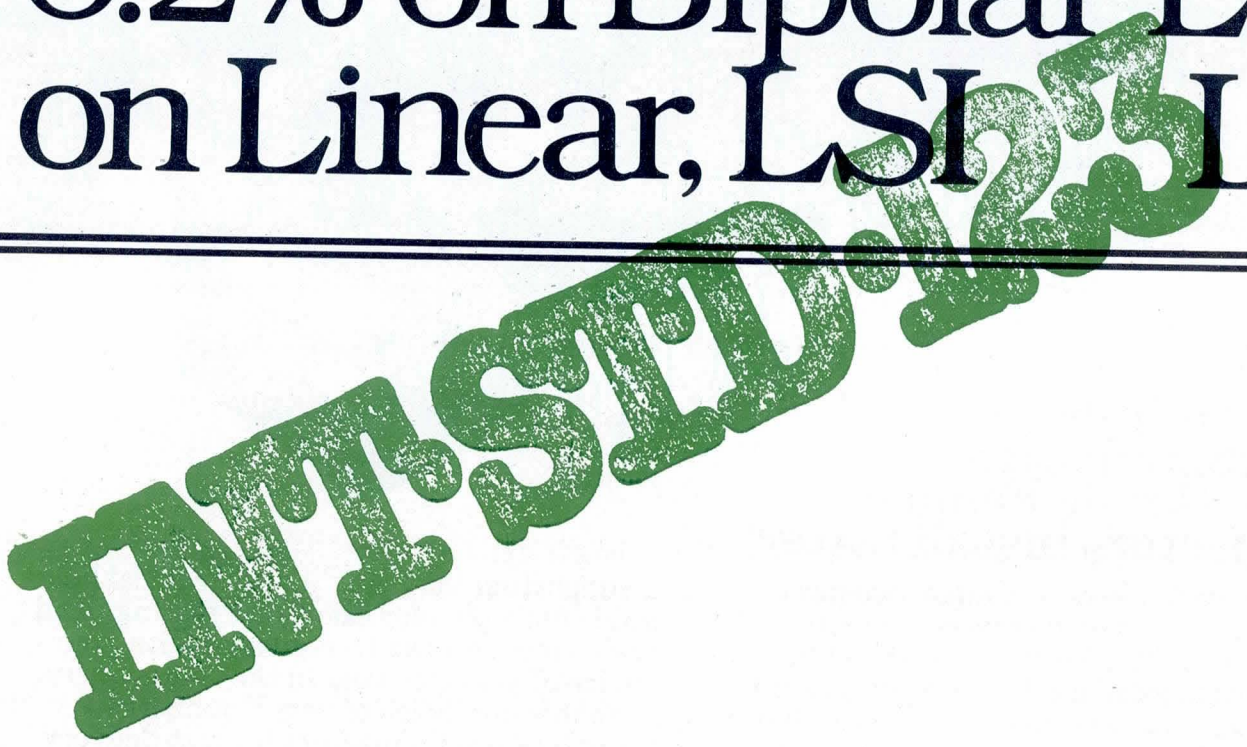

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Memory Structure Speeds Generation of Pseudonoise Sequences

Fast, efficient algorithm can benefit communication systems through an innovative memory organization to simulate multiple binary shift registers that operate in parallel and generate a sequence of pseudorandom numbers

P. Schöbi

Institute for Communications Technology
Swiss Federal Institute of Technology, CH-8092 Zürich, Switzerland

Communication links frequently rely on binary pseudonoise sequences, deterministic strings of binary digits that repeat only after a relatively long period and have statistical properties similar to those of true random numbers. The autocorrelation properties of pseudonoise sequences are important in broadband communications systems, in coding schemes or stream cipher systems, and when producing test signals for unknown channels. Their cross correlation properties are important for identification, synchronization, and control of remote devices such as distributed data terminals. The use of microprocessors in data terminals and other equipment that might rely on pseudonoise sequences has established the need for algorithms that can generate these sequences, in software, quickly and efficiently.

Although used extensively for pseudorandom number and pseudonoise sequence generation in large computers, and by far the most successful approach, the linear congruential algorithm is not well suited for use on small computers because it relies on multiplication of large integers. Instead, in conventional systems, linear feedback shift registers are used to produce binary pseudonoise sequences. The term *linear*, here, means that only exclusive OR connections appear in the feedback logic (Fig 1).

Straightforward simulation of a linear feedback shift register poses a problem. The shift register is a finite

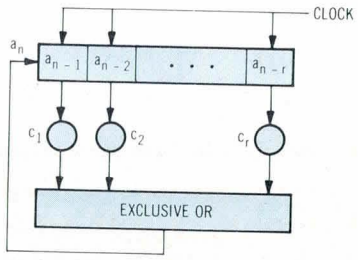

Fig 1 Binary shift register. In this general configuration, some register stages are exclusive ORed and fed back. Operation is linear because only exclusive OR connections are required

(continued on page 136)

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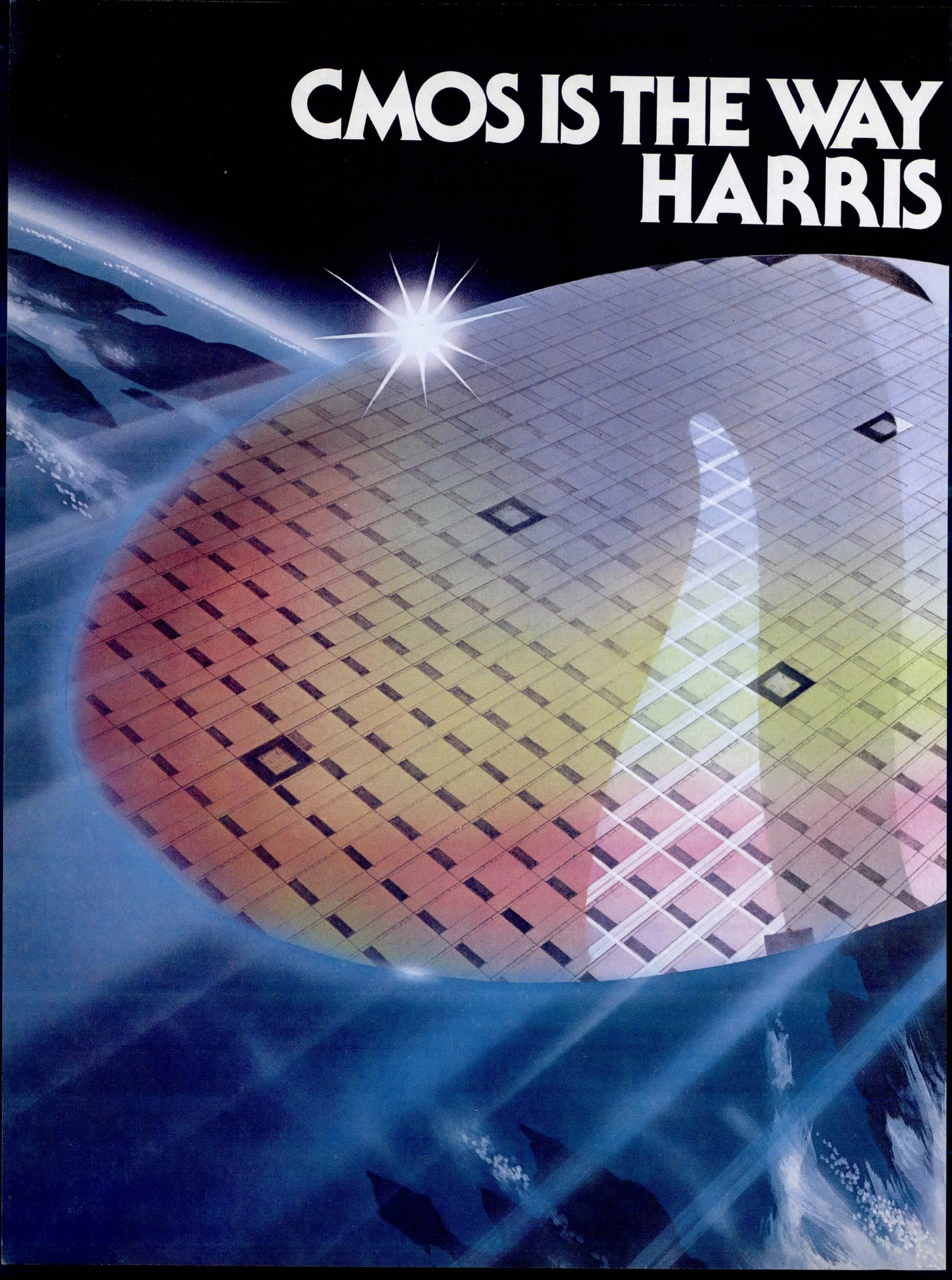

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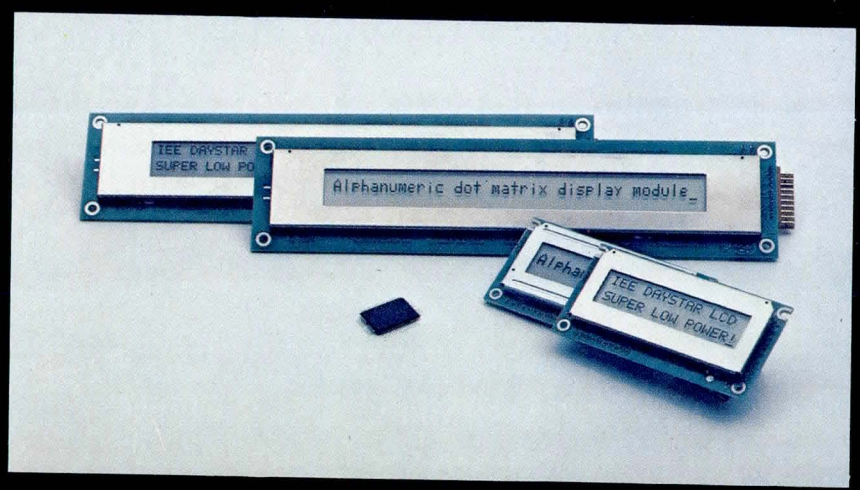

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automaton and therefore produces a periodic sequence whose finite period depends strongly on the length of the register. In many applications where statistical properties are important, very long registers are required. On the other hand, as soon as the length of a straightforward shift register exceeds one or two processor words, only very low bit rates can be attained. However, throughput improves if a more sophisticated memory organization is used to implement linear shift registers in a small, word oriented processor.

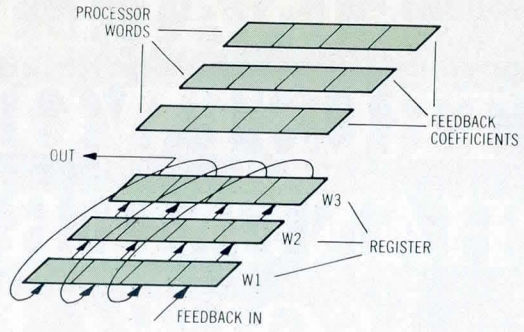

Fig 2 Serpentine memory organization. Performance improves when very long shift registers are stored in memory as shown. Arrows indicate shift direction. Second region of memory contains feedback coefficients

Theoretical Background

In a mathematical description of linear shift registers, based on the structure of Fig 1, the c_i feedback coefficients can have two possible values: 1, if a_{n-1} is connected to the exclusive OR gate and fed back, otherwise 0. Because the exclusive OR connection performs a modulo 2 addition,

$$a_n = \sum_{i=1}^{r} c_i a_{n-i} \qquad (1)$$

and the resulting sequence, $\{a_n\}$, can be represented as a polynomial in X, with each power of X marking the time at which its associated coefficient occurs. Then, the shift register output at time n is the coefficient of X_n and, for the general polynomial

$$G(X) = g_0 + g_1X + \ldots + g_kX^k + \ldots + g_nX^n$$

where the coefficients take on only the values 0 and 1, the vector of coefficients $\mathbf{g} = (g_0, g_1, \ldots, g_n)$ supplies the binary digit g_k, generated at time k for any particular value of k between 0 and n.

The sequence produced by the generator in Fig 1 can be represented as

$$G(X) = \frac{Z(X)}{1 + \sum_{i=1}^{r} c_i X^i} \qquad (2)$$

Here, Z(X) depends on the initial value loaded into the register. The denominator in Eq (2) is defined as the recursion polynomial for the sequence. If it is primitive, then the period of G(X) is $2^r - 1$, the maximum period, and the sequence is a maximum length binary sequence, called an m-sequence. If the recursion polynomial is irreducible, then the period of G(X) is a factor of $2^r - 1$. In any other case, the period of G(X) depends on Z(X) and, therefore, on the initial value loaded into the register.

Shift Register Simulation

Sequences can be produced on the basis of Eq (1) by simulating the hardware methods just discussed. A typical program might store the content of the shift register in successive memory words. When this is done, it is advantageous to assign a second memory word—containing the associated feedback coefficients—to each register storage location. When a certain register cell is connected to the exclusive OR adder, the corresponding feedback bit in the feedback word is set to 1; otherwise, the feedback word bit contains 0.

To calculate the feedback input to the shift register, feedback coefficients must be ANDed with the shift register content, and the number of binary 1s in this result must be counted. The feedback input will be 0, for an even number of 1s, otherwise 1. Programs based on this approach can be very time-consuming for two reasons. It is awkward, at best, to shift a bit pattern through several words of memory. Also, the feedback input is difficult to calculate from Eq (1). Fig 2 shows a more sophisticated, serpentine memory organization that addresses these problems and offers several advantages when used with long shift registers.

The arrows in Fig 2 mark the shift direction in the simulated shift register. Using this approach, feedback coefficients can be handled as suggested earlier and results can be calculated in much the same way. The advantage, with the serpentine structure, lies in the easy implementation of shift operations. As shown in Fig 2, a cyclic exchange of register words (W1 to W2, W2 to W3, W3 to W1) and a shift of the first register one position to the left achieve a shift of the entire simulated register value. The cyclic exchange is easily obtained through use of a cyclic counter in a relative addressing mode.

Division Method

Another useful means of generating shift register sequences is by evaluating Eq (2), performing the division in the sense of a binary long division. As can be seen from the example worked out in Fig 3, the division method is useful if the shift register length does not exceed one less than the processor word size, or one less than twice the word size on a processor that implements double-word instructions. The example shows that each bit of output requires one shift right of the denominator and one exclusive OR operation. Faster program execution results if, instead of shifting the denominator to the right, it is left stationary and the

(continued on page 138)

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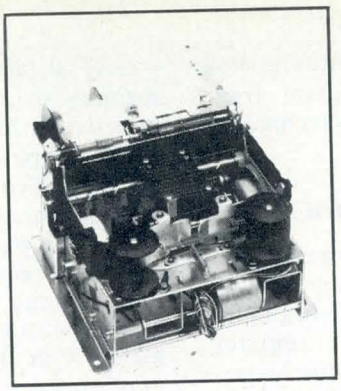

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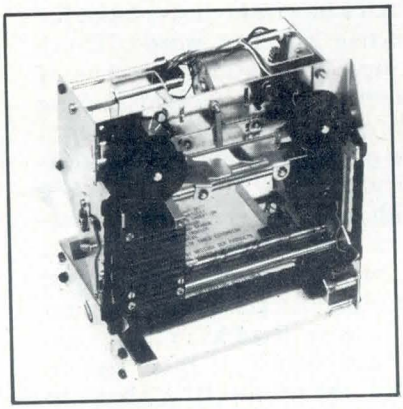

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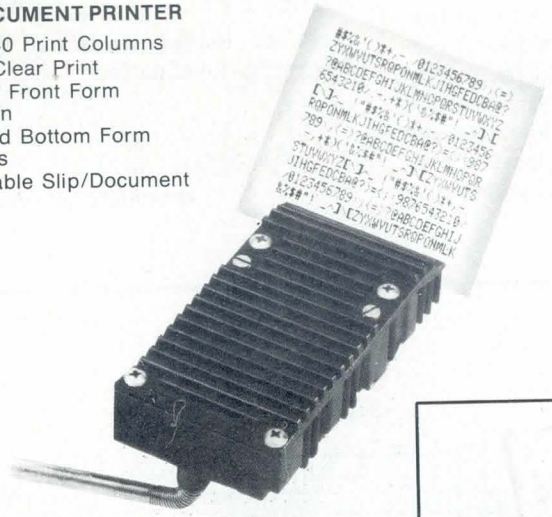

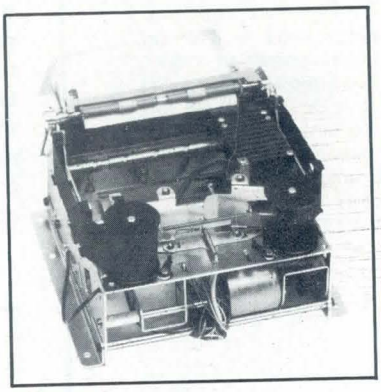

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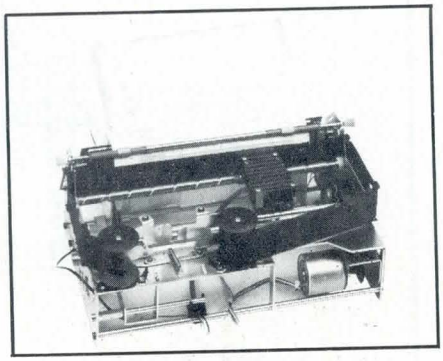

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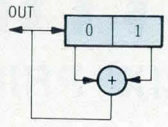


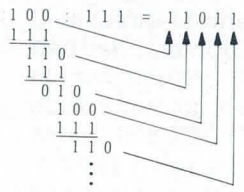
(a)

USING EQ (2)

$$G(X) = \frac{1}{1 + X + X^2}$$

(b)

AND A LONG DIVISION LEADS TO



(c)

```
LOOP:   JP      ZERO    ; if sign-flag zero
        XRA     B       ; if sign-flag one
ZERO:   ADA     A       ; shift left A
        CALL    OUT     ; output
        JMP     LOOP    ; next bit
```

(d)

Fig 3 Division method. Two-stage shift register (a) has initial condition "01" and recursion polynomial $1 + X + X^2$. Eq (2), in (b), leads to binary long division (c) implemented by compact 8080 microprocessor routine (d)

numerator is shifted left. The 8080 assembly language program fragment of Fig 3(d) uses this technique.

New Parallel Structure

A parallel memory organization allows especially fast generation of shift register sequences. Working in parallel, several shift register generators produce multiple sequences that can be used as output following parallel to serial conversion. Similar techniques have been used in hardware implementations, and the approach is particularly well suited to a microcomputer sequence generator in software. Basically, if $\{a_k\}$ is an m-sequence with the recursion polynomial f(X), then the sequence $\{a_{2^L k}\}$ has the same recursion polynomial, f(X). This means that the elements of $\{a_k\}$ taken in steps of every 2^Lth element constitute the same sequence, $\{a_k\}$. The concept can be applied to the structure of Fig 4. Taking 2^L parallel generators, each with the same feedback logic, and providing initial conditions so that the first generator produces intermediate sequence $\{a_{2^L k}\}$, the second produces intermediate sequence $\{a_{2^L k+1}\}$, and so on; a parallel to serial conversion of the output word produces the desired output sequence.

Several factors make the parallel memory structure a good basis for effective software implementation. Most computers use a word length of 2^L, which makes the required memory organization convenient. All of the parallel generators have identical recursion—the same as that of the desired output sequence—and identical feedback logic. With the memory organization shown in Fig 5, this permits easy calculation of feedback values through a bitwise exclusive OR of the respective memory words. Every shift operation produces 2^L bits of the desired sequence, and shifting can be performed by incrementing a cyclic pointer in a relative addressing mode.

With parallel generator initialization, it is important to note that a shift register length of r stages, using 2^L parallel generators, requires $2^L r$ bits to be fixed as initial conditions, and only r of these can be selected independently. Thus, to produce the sequence $\{a_0, a_1, \ldots\}$, the first $2^L r$ bits $\{a_0, a_1, \ldots, a_{2^L r - 1}\}$ must be loaded as initial values following the equation

$$W_i = \{a_{2^L(i-1)}, a_{2^L(i-1)+1}, \cdots, a_{2^L(i-1)+2^L-1}\}$$

(continued on page 142)

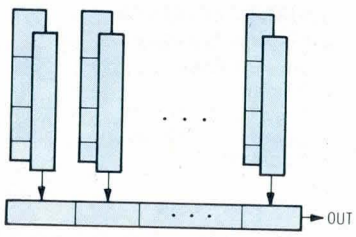


Fig 4 Parallel structure. Operating independently, identical generators each produce one bit of desired output sequence. Then, parallel to serial conversion produces final result. Parallel structure allows especially convenient implementation in software

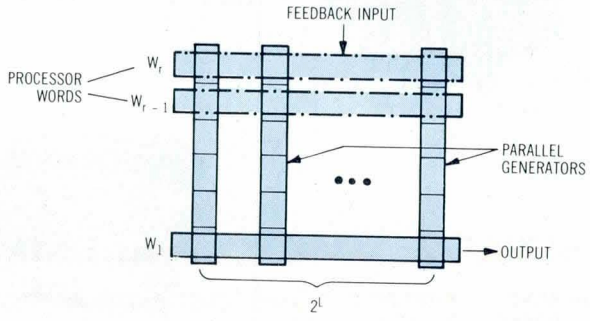


Fig 5 Parallel structure memory organization. Using L-bit word, 2^L shift registers can be simulated in parallel. Since all shift registers have identical recursion (ie, feedback mechanism), exclusive OR of respective words yields feedback value. Shifts also are easy to perform, and each shift produces 2^L bits of output

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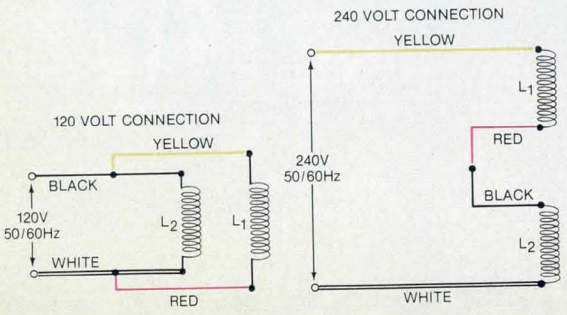

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This means that the first set of 2^L bits goes in W1, the second set in W2, and so on. These initial conditions can be calculated using a conventional shift register simulation.

Comparison of Methods

Various methods for generating pseudonoise sequences can be compared by counting the number of processor cycles per bit of the output sequence, for each method, assuming an 8080 microprocessor with word length of $2^3 = 8$ bits (Fig 6). The problem of obtaining the sequence as functional output is not considered here, nor is the problem of applying this output in a particular implementation. However, with a parallel structure in which every step delivers 2^L bits in one register, both of these tasks should be easy to accomplish.

The stepwise nature of the curves for the direct simulation [Fig 6(a)] and the serpentine structure [Fig 6(c)] arise from the increased overhead when a new computer word must be added to represent the shift register. With the parallel structure, the computing time generally depends on the number of feedback connections in the simulated shift register, and not on the length of the register. For most shift register lengths, there exist primitive polynomials that need only two feedback connections and result in very efficient programs. In general, the number of feedback connections for registers of length r is on the order of one-half r, and a distribution similar to the binomial distribution with p = 0.5 can be observed.

Overhead for the parallel structure with r/2 feedback coefficients appears in Fig 6(e). It is important to realize that increasing the processor word length leads to faster generators. This is especially true with the parallel structure, whose throughput increases in proportion to the processor word size, because the number of bits that can be produced with the same effort is directly proportional to the number of parallel generators.

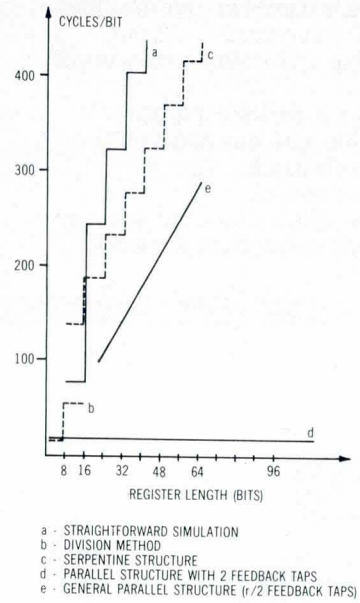

Fig 6 Relative performance. Chart shows average number of processor cycles required to generate each bit of output using (a) straightforward shift register simulation, (b) long division, (c) serpentine memory organization, (d) parallel memory organization with two feedback taps, and (e) generalized parallel organization with r/2 feedback taps

Summary

Communication systems and other applications often require pseudorandom numbers or pseudonoise sequences, which are usually generated in binary linear feedback shift registers. Carefully structured memory organization permits fast and effective simulation of binary shift registers in a small, word oriented computer. The possibility of programming 2^L identical generators in parallel leads to an especially promising structure that produces 2^L bits of the desired output sequence in each major step. Although the output sequence fails several tests for randomness, it can still be used as a random number sequence if statistical demands are not too stringent. The proposed techniques achieve fast generation of pseudonoise sequences in a wide range of small computers and, especially, in the control processors of remote data terminals.

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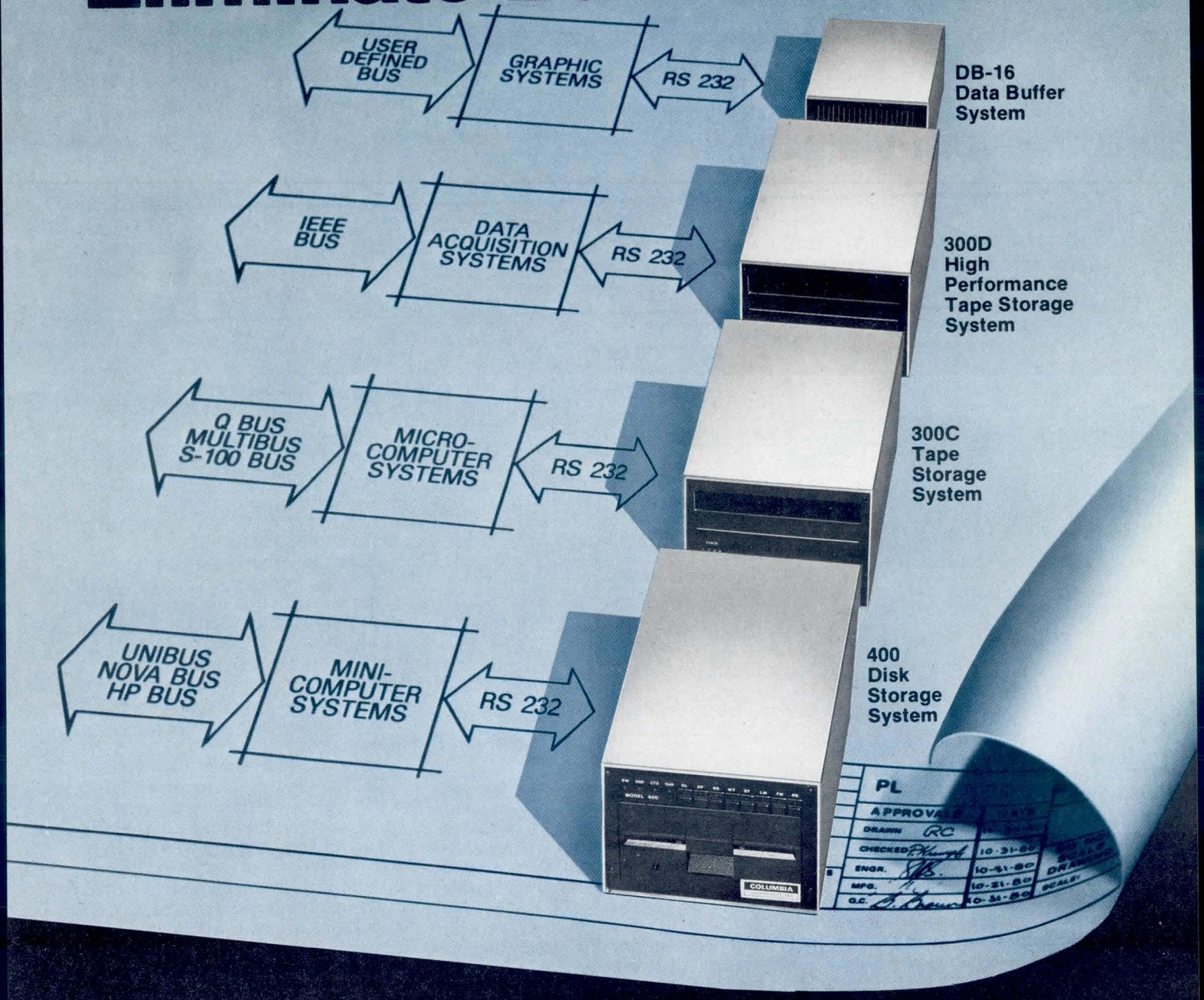

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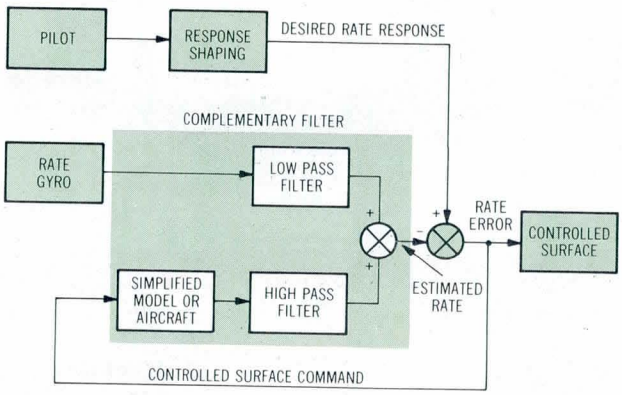
Complementary filtering and a simple system model combine to increase gain and bandwidth



Complementary filtering and a simple electronic model greatly increase the amount of useful gain achievable in a feedback control system subject to environmental vibration. This technique, devised for a sensor-actuator control loop on a CH-47 helicopter, has increased useful gain from 2 to 4 and increased system bandwidth from less than 0.5 Hz to over 1 Hz.

Useful gain between sensor signal and actuator in a vibrating system is limited by the vibrational noise, which is amplified along with the sensor signal. Some improvement is possible by putting the sensor signal through a low pass filter to remove the relatively high frequency components (sharp vibrational accelerations). However, the time lag introduced by the filter limits the achievable gain through its effect on the control system limit cycle.

In a feedback control loop, there is a certain amount of hysteresis (or slop) between system response and actuator signal. This hysteresis lag leads to oscillations, called the limit cycle effect, if the gain is increased beyond a certain point. The additional time lag produced by simple filtering further lowers the tolerable gain.

Effect of this hysteresis can be compensated for by attempting to predict the response of the controlled portion of the feedback loop and incorporating this prediction into the actuator signal. An implementation of this approach is shown in the block diagram. The sensor (rate gyro) is fed through a conventional low pass filter to remove vibrational noise. At the same time, a simplified model predicts the controlled surface response to an infinitesimal actuator signal. This prediction signal is put through a high pass filter that removes the long term errors in the calculated response and leaves a good estimate of the high frequency components of the system motion.

The time constants (0.2 in the illustrated application) of the two filters are matched so that the sum of their outputs is a complete angular rate feedback signal, with noise and lag removed.

Effect of filter time constant on the noise boundary for the complementary filter is the same as for a conventional filter, but the effect on the limit cycle boundary is changed profoundly because no lag is added. Therefore, by increasing the filter time constant, gains can be made much higher than with a low pass filter alone.

In tests with the CH-47, results were impressive. Gain and bandwidth improvements were found to be relatively insensitive to the accuracy of the system model. Even a zero order model showed measurable improvement, and all first order models tried resulted in reduced system noise with significant increases in gain and bandwidth without encountering a limit cycle problem.

Note

This work was done by John F. Garren, Jr, and Frank R. Niessen, of Langley Research Center.

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Fault Tolerant Computer System

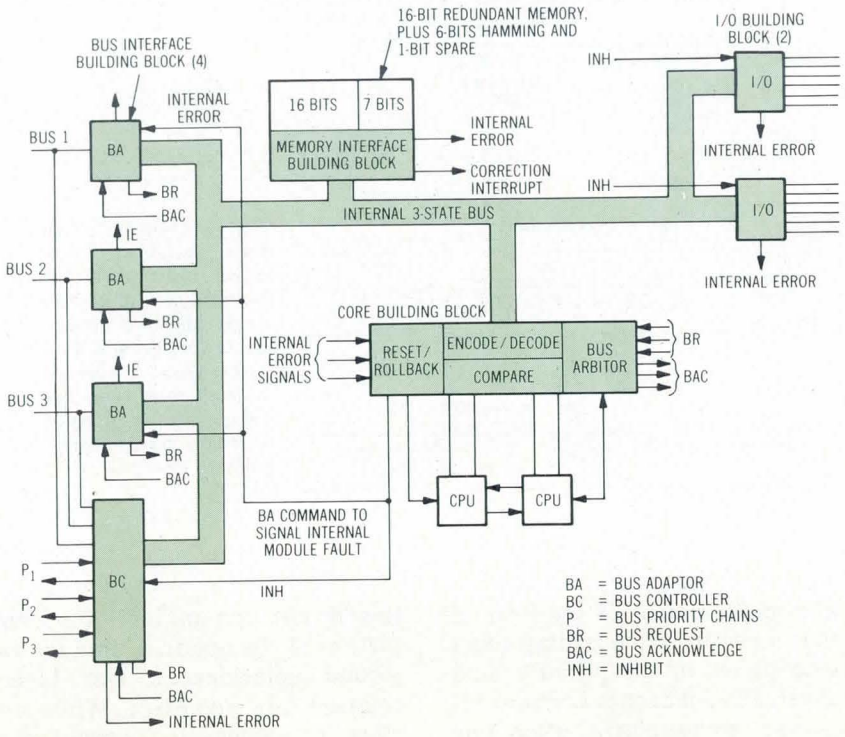
Self-checking building blocks can increase reliability

More reliable computers could be assembled by using proposed VLSI building block circuits with built-in error detection. Four such circuits would be connected with standard microprocessors and memory devices to form a self-checking computer module. Each building block detects its own malfunctions, and the complete module also corrects single-bit errors found in memory (usually the most fault susceptible part of a computer). Noncorrectable faults are handled by switching in replacement computer modules, shutting down operation, or by taking other corrective steps.

The four fault tolerant building blocks, designated memory interface, programmable bus interface, input/output (I/O) interface, and core, are interconnected as shown in the figure. A 3-state internal bus is shared by the building blocks. Each block signals faults in its circuitry to the core. The core also checks the bus signals for proper coding.

Upon detecting a fault, the core disables the bus control and I/O functions, isolating the computer from its environment. The core can then either halt further processing, initiate rollback and restart, or initiate a memory reload and restart. If the fault repeats, an external module could take over processing.

The fault detecting and correcting memory interface building block interfaces the computer memory to the internal bus. The block feeds Hamming corrections to damaged memory data, automatically replaces a faulty bit with a spare, generates parity coding and decoding, and detects its own internal faults.



The bus interface building block transfers information between computer modules or between a computer module and I/O devices over an external bus. This block can be microprogrammed as a bus adapter or bus controller. Faults are detected through parity coding and through internal duplication, with morphic comparison for most of the logic circuitry.

Since I/O hardware has different voltage ranges, currents, timing parameters, and word formats, the I/O building block would offer a standard set of functions for interfacing the most common configurations. The user could supply additional functions for special or nonstandard applications.

The *core building block* detects central processing unit faults, collects fault indications from itself and other building blocks, and disables its host computer module upon detection of a permanent fault.

Preliminary cost studies indicate that as the level of large scale integration is increased in the building block circuits, memory becomes the dominant cost in the network. However, as the level of integration is increased, the cost of producing the self-checking computer approaches that of conventional computers.

Note

This work was done by Algirdas A. Avizienis, David A. Rennels, and Milos Ercegovac of Caltech and UCLA for NASA's Jet Propulsion Laboratory.

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Multichannel Coincidence Circuit

Circuit records coincidences between pulses in two or more channels

The digital circuit shown in the block diagram in Fig 1 looks for coincidences between pulses in a primary channel and those in one or more secondary channels. When two consecutive coincidence events are found, the circuit records the elapsed time (the interval time) between the leading edges of the pulses in the primary channel.

Having already been built for two channels of data pulses, the coincidence timer will soon have a 3-channel version. It has been tested with both simulated and actual data sources. Originally used in a laser velocimeter to determine the time between velocity measurements, the circuit can also be used to measure time intervals in other instruments that receive data at irregular rates from two or more sources.

The timer considers a pulse of the primary channel to be coincident with one of the secondary channel pulses if both occur within a predetermined timespan or aperture (see Fig 2); the coincident pulses do not necessarily have to overlap as long as their leading edges are less than 1 aperture time apart.

As seen in the Fig 1, the circuit is divided into three major functions. The *interval time measurement subcircuit* contains binary counters, temporary data storage, and data output devices to generate a digital number related to the time between coincident pulses. The *measurement control subcircuit* controls the operation of the counters, storage, and output devices. The *system control and timing sequence generator* oversees routine timing and control.

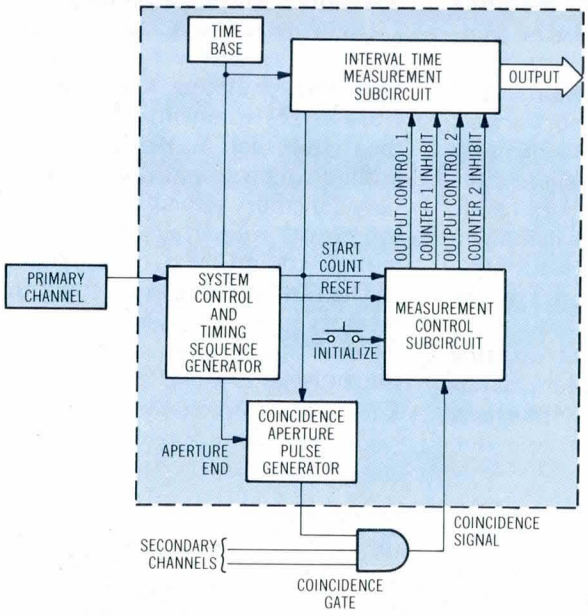

Fig 1 The coincidence circuit. Binary counters and latches are in interval time measurement subcircuit, timing pulses originate in measurement control subcircuit, and routine timing is generated in timing sequence generator

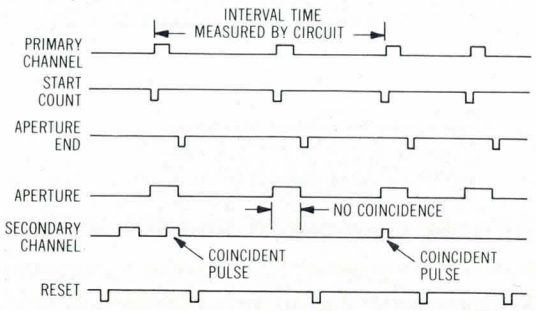

Fig 2 Pulses from two channels. Here, coincidence, when both pulses fall within same aperture period, occurs in first and third apertures. Interval time is thus time between leading edges of first and third pulses in primary channel

The measurement of the interval time is made from the leading edges of the pulses in the primary data channel. Since it cannot be known if the time measurement after one coincidence is valid until a second coincidence event is recorded (and this is not certain until the completion of the aperture time for the second coincidence), two binary counters are required. While the counter making the current measurement continues its count until after the second coincidence

aperture has ended, the second binary counter has already begun to measure the next interval. If a coincidence event is recorded, the leading edge value of the interval time is stored, and the first counter is reset to zero to await a new input pulse. Meanwhile, the second counter is already measuring the next interval. If a coincidence does not occur, the first counter continues its measurement, and the second counter is reset.

A fixed series of pulses, consisting of start-count, aperture-end, and reset signals, is supplied to the coincidence interval measurement subcircuit from the measurement control subcircuit. The start-count pulse, generated immediately after receipt of a pulse from the primary channel, initiates the measurement. A pulse from one or more of the secondary channels during the aperture pulse time generates a coincidence signal. The measurement control subcircuit continuously reads the count value on the active counter; when the coincidence signal is received, the count value that existed at the leading edge of the primary channel pulse is transferred to the output bus.

Note

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Independent Synchronizer for Digital Decoders

Circuit maintains synchronization at low signal to noise ratios

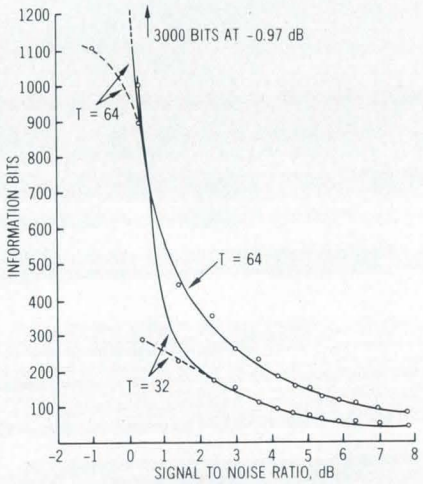
A digital logic circuit synchronizes the branches of a convolutional code decoder, but operates independently of the decoder. The synchronizing circuit can be used with any convolutional decoder, regardless of the decoding algorithm. Nevertheless, the circuit is simple, consisting of a 15-stage shift register, three up/down counters, and a few logic gates.

In an experimental version of the synchronizer built for a Viterbi decoder using the Odenwalder 7 code, the sign bit from the input to each branch of the decoder is applied to a 15-bit shift register, and the modulo-2 sum is formed of the register 1st, 3d, 12th, 14th, and 15th stages. A second modulo-2 sum is formed of the contents of the 8th, 10th, and 11th stages, and a third modulo-2 sum is formed of the 5th and 6th stages.

Parity checks are used as an indicator of correct or incorrect node synchronization. If all three parity checks agree, an up/down counter is incremented. If the first two checks agree but the third disagrees, the same up/down counter is decremented. In any other situation, the counter is neither incremented nor decremented.

The process is repeated when the next bit is read into the shift register, but with a second up/down counter, and is repeated once more with the third input bit and a third up/down counter. The sequence starts again with the fourth input bit.

Associated with the properly framed code sequence, the up/down counter is more likely than the other two counters to be augmented and less likely to be decremented when the polarity is correct. Correct node synchronization is thus determined by observing which of the counters



first reaches predetermined positive and negative threshold values. Since a negative threshold crossing indicates an inverted decoder input, node synchronization and sign ambiguities are resolved simultaneously.

In tests the synchronizer maintained synchronization at signal to noise ratios as low as −3 dB. (See Fig.) In contrast, a conventional branch synchronizer (one based on comparisons of unanimity and nonunanimity counters) was limited to signal to noise ratios above 1.4 dB.

Note

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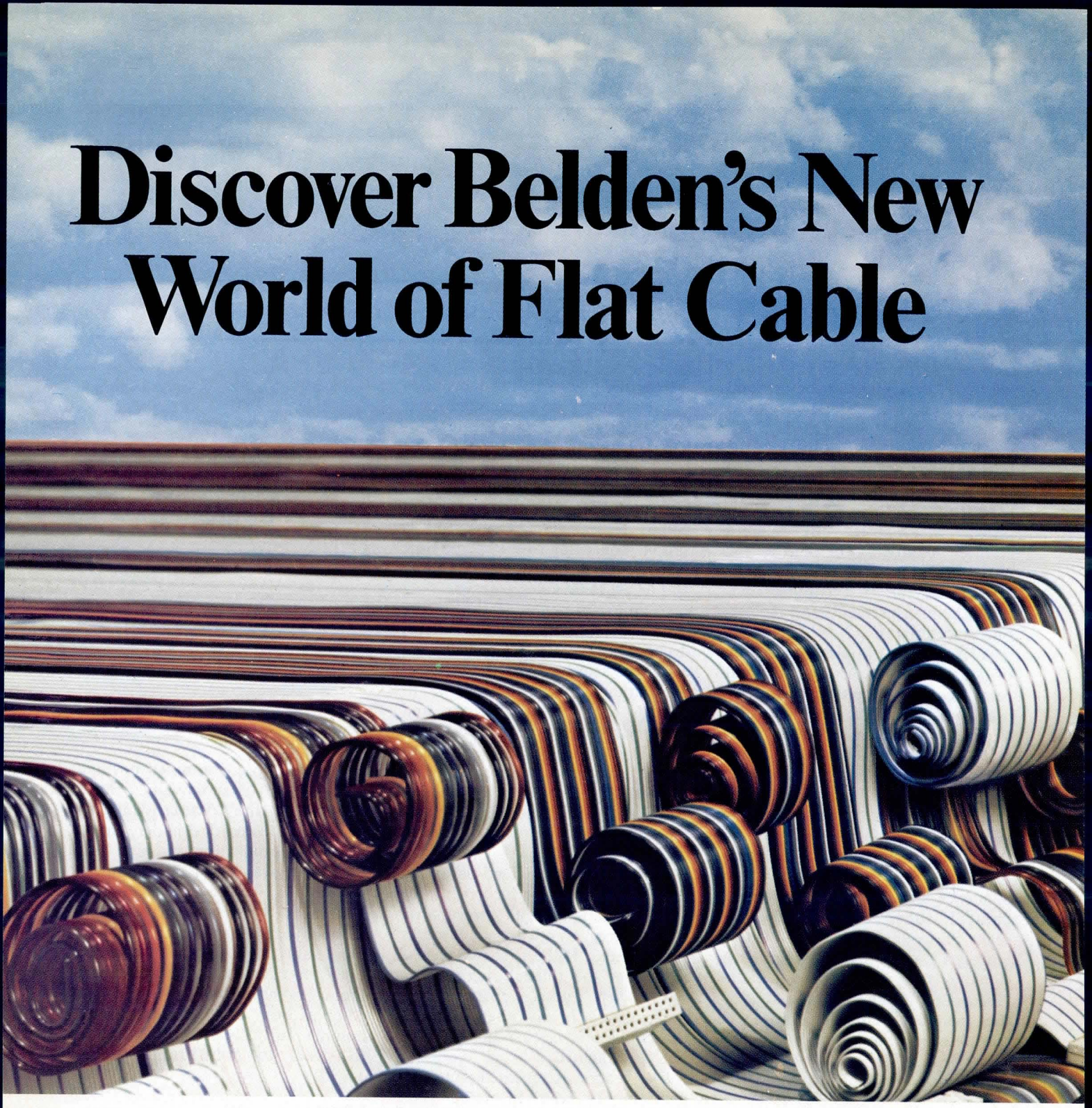

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Interfacing Fundamentals: The 8255 Semaphores

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Since most of the newer microcomputer boards and single-chip microcomputers contain some type of programmable parallel interface port, it is increasingly likely, when interfacing two microcomputers, that this will be done via such a port. One of the more popular programmable parallel interface chips is the Intel 8255, which contains 24 input/output lines and exhibits three different modes of operation: (a) mode 0, unconditional input or output; (b) mode 1, conditional input or output; and (c) mode 2, conditional bidirectional input/output. Depending upon how the 8255 is programmed, various combinations of modes 0, 1, and 2 ports can be selected.[1] This column describes the characteristics of the three semaphores present within the chip.

Results presented here were obtained experimentally with two 8080A based microcomputers interfaced to each other via port A of an 8255 chip operated in the mode 2 (port A) and mode 1 (port B) configurations. (The details of the interface circuit and programs will be given in the next column.) Rather than execute the programs at 2 MHz, each machine cycle on each computer was executed single step using a hardware single-step circuit.[2] The logic states of the $\overline{RD}$, $\overline{WR}$, $\overline{ACK}_A$, $\overline{STB}_A$, $\overline{OBF}_A$, and IBF_A signals were determined with a logic probe.

The three 8255 semaphores acted identically. Their truth table [Fig 1(a)] is compared [Fig 1(b)] to the truth table for a 7474 D-type positive edge triggered flipflop with preset and clear [Fig 1(c)]. There is one difference between the two tables [Figs 1(a) and 1(b)]: Q is logic 1 for the semaphore and is Q_o for the 7474 flipflop when PRESET is at logic 1 and CLOCK is at logic 0. This difference in behavior is unexpected and appears to be unnecessary.* A semaphore that behaves as a 7474 flipflop should be acceptable.

Shown in Fig 2 is a comparison of the timing diagrams for (a) the 8255 semaphores and (b) the 7474 flipflop. The asynchronous PRESET input causes output Q to go to a logic 1 state for both flipflops. Any additional negative PRESET pulses that occur while Q is at logic 1 have no effect. The difference in behavior occurs with the synchronous CLOCK input. For the semaphore, the positive edge of the CLOCK input always causes a 1 to 0 transition in Q, whereas for the 7474, the 1 to 0 transition occurs only if Q is initially at a logic 1.

*Perhaps a reader can suggest why the difference exists. Please communicate any suggestions to the author.

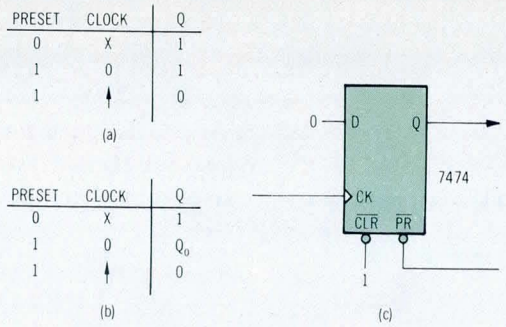

Fig 1 Truth table comparison. Truth table for 8255 semaphore (a), and truth table for 7474 D-type edge triggered flipflop (b) displayed in (c), in which CLEAR = 1 and D = 0, are shown. Symbol ↑ represents a transition from 0 to 1 required at the CK input; X means that either logic state is acceptable; and Q_o is level of Q before indicated input conditions were established

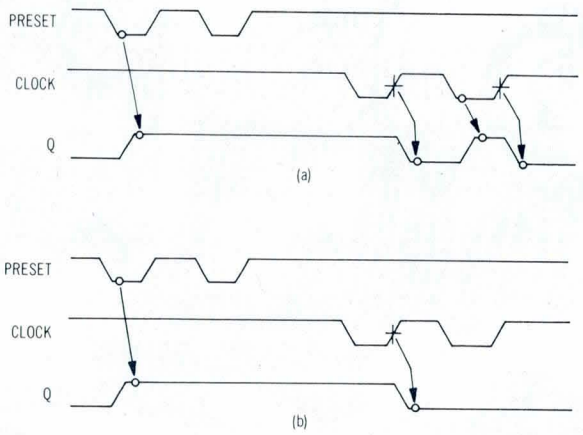

Fig 2 Timing diagram comparison. Timing diagram shown in (a) is that of 8255 semaphore; a negative clock pulse, when Q is initially logic 0, causes a positive clock pulse output. Timing diagram shown in (b) is that of 7474 flipflop

When operated in the mode 2 configuration, port A on the 8255 chip presents an excellent example of bidirectional conditional input/output (I/O). The port itself is a bidirectional buffer that has both input and output semaphores associated with it.[3] The two semaphores and the semaphore timing diagrams for I/O operations are summarized in Figs 3 and 4. Fig 3(a) shows the output semaphore for the bidirectional port A. A negative $\overline{WR}$ pulse at pin 36 on the 8255 clears $\overline{OBF}_A$ and outputs data from the 8080A to port A. An acknowledge signal, $\overline{ACK}_A$, from the I/O device sets $\overline{OBF}_A$ [Fig 3(b)]. The input semaphore is shown in Fig 4(a). A negative $\overline{RD}$ pulse at pin 5 clears IBF_A and permits the 8080A to input data from port A. A strobe signal, $\overline{STB}_A$, from the I/O device sets IBF_A and causes port A to latch a new data byte [Fig 4(b)].

fiber optic modem for local data distribution

multiplexes control signals along with the data

Fiber optic modems are ideally suited for many local data distribution applications since they offer several inherent advantages over conventional hard-wired systems. These include immunity from rf and magnetic signals, increased bandwidth, and a significant improvement in the security of the data link.

Versitron's FOM-5 fiber optic modem (one of a family of fiber optic modems) not only provides the basic advantage of fiber optics, but also offers several unique system operating features that makes it ideal for local data distribution applications.

Multiplexes Control Signals — Three separate control signals in each direction are multiplexed with the data over the fiber optic link. This provides a fully interactive handshaking sequence with the FOM-5 functioning as a truly transparent device at both ends of the link.

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Intrusion Alarm — The receive circuitry continuously monitors the receive data for the presence of the multiplexer sync signal generated by the remote unit. Loss of this signal will cause an audible alarm condition and block further data transmission at both local and the remote modems. After verifying that the link is still secure, the system may be reset from either the local or remote unit.

Plug-In Compatibility — The FOM-5 has DSU/V35 or RS-232/MIL-188 interfaces. Precut and terminated fiber optic cables are also available from Versitron.

Versitron, Inc. installed its first fiber optic link utilizing a multiplexed data technique in the early 1960's. Since that time we have sold over 19,000 fiber optic links covering a wide variety of requirements for military and commercial applications.

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CIRCLE 72 ON INQUIRY CARD

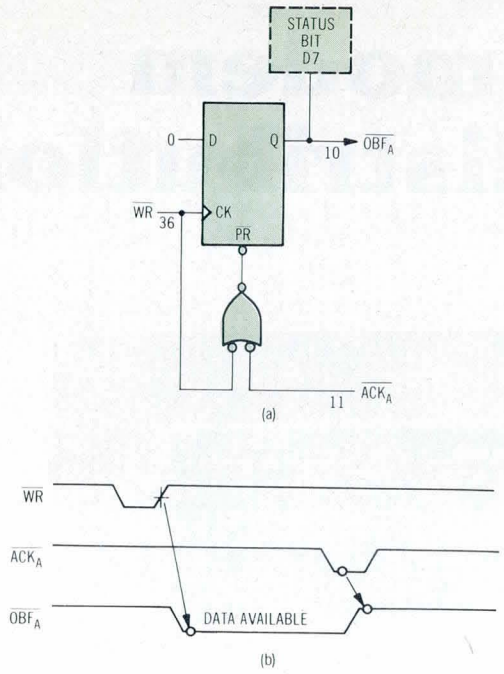

Fig 3 8255 port A output semaphore (a) and timing diagrams (b). Semaphore nature of flipflop can be clearly seen: Q output is monitored as status bit by master computer and as external pin by slave. Pin numbers for $\overline{WR}$, $\overline{OBF_A}$, and $\overline{ACK_A}$, are shown

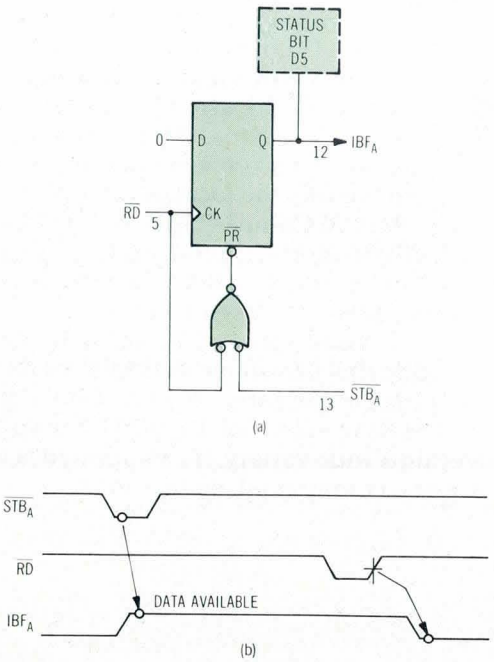

Fig 4 8255 port A input semaphore (a) and timing diagrams (b). I/O semaphores are identical in operating characteristics. Pin numbers for $\overline{RD}$, IBF_A, and $\overline{STB_A}$ are shown

The OR gate symbols at the PRESET input of the semaphores in Figs 3(a) and 4(a) have been added to account for the difference in behavior between the semaphores and the 7474 flipflop, as discussed previously. Negative logic is used for the OR gate: a logic 0 at either of the two OR gate inputs produces a logic 0 output that presets the semaphore. Thus, if $\overline{WR}$ or $\overline{ACK_A}$ is 0, then $\overline{OBF_A}$ is set. If $\overline{RD}$ or $\overline{STB_A}$ is 0, then IBF_A is set. With this OR gate representation, the behavior of these two semaphores is consistent with the truth table in Fig 1 and the timing diagrams in Fig 2. In practice, would negative $\overline{RD}$ or $\overline{WR}$ pulses ever cause IBF_A or $\overline{OBF_A}$ to be set during the input or output machine cycles, respectively, of the 8080A microcomputer that is interfaced to the 8255? This situation is unlikely because there would never be an attempt to read data from an empty input buffer (IBF_A at logic 0) or to output data to a full output buffer ($\overline{OBF_A}$ at logic 0).

Port B on the 8255 chip can be operated as a conditional input or output port with semaphore, but not as a bidirectional conditional I/O port. Bit D1 in the control word determines the I/O characteristics of this port, with logic 1 selecting input and logic 0 selecting output. The port B semaphore has the same truth table, timing characteristics, and configuration as shown for the port A semaphores in Figs 1 to 4. The difference is that the clock input (CK) to the semaphore is more complex than simply CK = $\overline{RD}$ or CK = $\overline{WR}$, which is the case for the port A semaphores. For the port B semaphore, the CK input exhibits the following logic, CK = $\overline{CD1} \cdot \overline{WR} + \overline{CD1} \cdot \overline{RD} + CD1 \cdot \overline{RD}$, where CD1 represents the logic 1 state of the D1 control bit, $\overline{CD1}$ represents the logic 0 state, and · and + represent the AND and OR logic operations, respectively. A negative $\overline{WR}$ clock pulse produces a negative clock pulse only if control bit D1 is logic 0. A negative $\overline{RD}$ clock pulse produces a negative clock pulse no matter whether control bit D1 is logic 0 or logic 1. Consequently, the logic for CK can be simplified to CK = $\overline{CD1} \cdot \overline{WR} + \overline{RD}$, an expression that can be verified experimentally.

REFERENCES

1. *Intel Peripheral Design Handbook*, Intel Corp, Santa Clara, Calif, 1979, pp 1-52 to 1-72 and 2-114 to 2-144 (includes specification sheets and application notes)
2. P. R. Rony, *Introductory Experiments in Digital Electronics and 8080A Microcomputer Programming and Interfacing, Book 2,* Howard W. Sams and Co, Inc, Indianapolis, Ind, 1978, p 55
3. P. R. Rony, "Interfacing Fundamentals: A Comparison of Block Diagrams for I/O Techniques," *Computer Design*, Feb 1980, pp 175-177

silent partner.

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Now Lear Siegler can fill the bill. Because our 310 Ballistic™ Printer is one silent partner that knows when to HUSH up.

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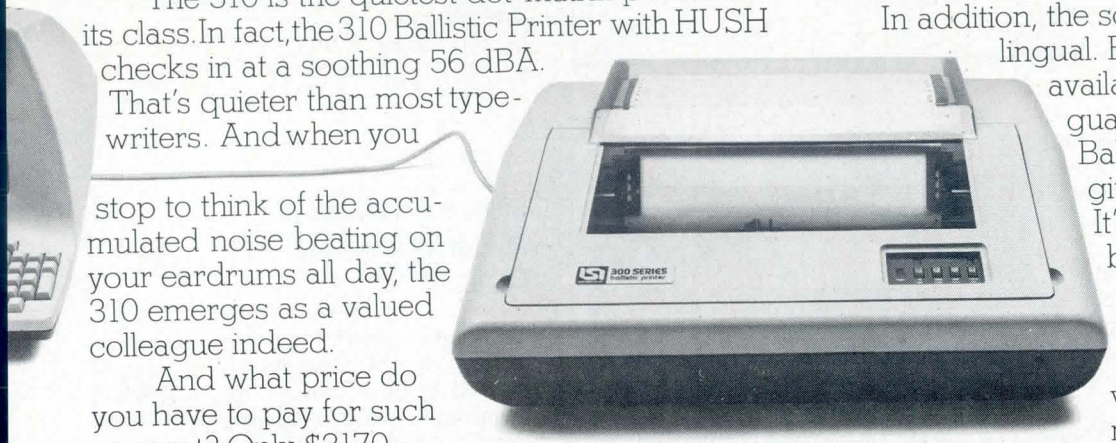

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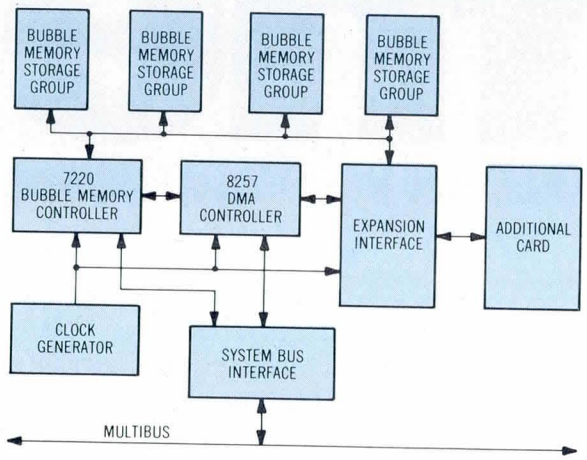
CIRCLE 73 ON INQUIRY CARD

512k-Byte Bubble Memory Board Incorporates Support Chips, Multibus Interface



Bubble memory board. From Intel Corp, the iSBC 254 is a complete inboard peripheral with 512k bytes of nonvolatile bubble memory and all support chips provided on one board

High density magnetic bubble memory board iSBC 254 combines up to 512k bytes of storage capacity with an interface for Multibus systems to serve as a realistic replacement for tape and disc systems. By providing all support chips onboard, Intel Corp, 1302 N Mathilda Ave, Sunnyvale, CA 94086, has freed designers to concentrate on higher level system objectives instead of on problems of interfacing.

The board contains the IM7220 bubble memory controller (BMC) that operates in DMA, interrupt, and polled data transfer modes, and features built-in power fail protection and automatic error correction. Other support chips on the board include a formatter/sense amplifier, three packages for coil driving, and a current pulse generator.

Capacities of 128k, 256k, or 512k bytes are obtained using one, two, or four IM 7110 1M-bit bubble memories. Transfer rates vary with capacity, with a 128k-byte version operating at a maximum of 12.5k bytes/s. Rates of 25k and 50k bytes/s can be achieved with 256k- and 512k-byte units by accessing the bubbles in parallel. Average access time is 48 ns.

The board runs under either the iRMX/80 or the iRMX/86 operating system. Under iRMX/80, the bubble manager (BMGR) software task keeps track of free or available space on the magnetic bubble memory. The bubble I/O (BUBIO) task can run with or without the bubble manager and controls all the board operations. Under iRMX/86, the board is supported as an integral part of the I/O system software.

Three modes of operation are employed for data transfer: direct memory access, polled, and data request. In the DMA mode, the board uses the 8257 DMA controller in conjunction with the BMC to perform DMA read, DMA write, and DMA verify operations. DMA read and write operations are used for high speed data transfers involving bus accessible memory; DMA verify operations are typically used to maintain control of the system bus while verification tasks are being performed. In the polled mode, the CPU periodically checks the status register of the BMC. In the data request (DRQ) mode, when the BMC's FIFO is half empty during a write operation, or half full during a read operation, the DRQ pin becomes active and an interrupt signals that data can be written or read.

Two status monitoring modes, interrupt and polled, are also provided. In interrupt mode, a change in the status register such as a completed operation, failed operation, or timing or parity error, will cause an interrupt to occur. In the polled mode, as in the data transfer polled mode, the CPU periodically checks the status register for a completed operation, failed operation, or timing or parity error.

Measuring 12 x 6.75 x 0.62″ (30 x 17.15 x 1.57 cm), the board requires two normally spaced card slots for adequate mechanical clearance, and has an operating temperature range of 0 to 55 °C. All address, data, and control signals are TTL and Multibus compatible. The board is compatible with 16-bit addressing for 8-bit processors, and with 20-bit addressing for 16-bit processors.

Circle 461 on Inquiry Card

System Offers up to 16M-Byte Storage Capacity

QT System + provides standard 2M-byte storage, as well as the availability of up to 16M bytes of storage, and includes mainframe, two 8″ (20-cm) disc drives, double-sided, double-density 5.25″ (13.33-cm) and 8″ (20-cm) floppy disc controller, power supply, fan, and Televideo 920C terminal. The 4-MHz Z80 CPU system is a product of QT Computer Systems, Inc, 15620 S Inglewood Ave, Lawndale, CA 90260. Features include 48k dynamic memory expandable to 64k; 2k monitor program on 2716 EPROM; RAM, ROM, and P/ROM in any combination up to 8k; two RS-232-C serial I/O ports; two parallel I/O ports; hard disc compatibility; realtime clock; CP/M 2.2 operating system; and power-on/reset jump to monitor program. The system will soon be available with MP/M to allow multiuser, multitasking operations.

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CIRCLE 74 ON INQUIRY CARD

Ideals tell you to design for performance. STC's product plan

Balancing your I/O performance objectives against your company's cost objectives can be a vexing challenge. STC is ready to help you resolve the dilemma with the most comprehensive offering of tape subsystem products and capabilities ever offered to the OEM.

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The 1900 Tape Family provides a choice of 9 basic subsystem configurations. So you can pick the precise combination of speeds, densities and features to complement your processor and your customers' applications.

The chart on the right will help you start sizing up the appropriate model.

In demanding processing environments GCR (6250 bpi) is the obvious choice. For example, a GCR tape drive can handle a 100 Mbyte disk dump/restore with a single reel in as little as 4 minutes. (Compared to 4 reels and 20 minutes for PE.) On long sequential files, a 125 ips GCR drive will actually outperform most disk drives. Best of all, GCR performance comes with a significant bonus in read/write reliability.

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If your company markets a line of systems to meet a variety of customer requirements, the STC 1900 can simplify your engineering and cut your costs.

The 1935 Formatter/Control Unit will handle up to four 1950 and 1920 Series Drives, intermixed in any combination of speeds and densities. That means a single hardware interface and a single set of operating system drivers and utilities can accommodate all the configurations in your marketing mix.

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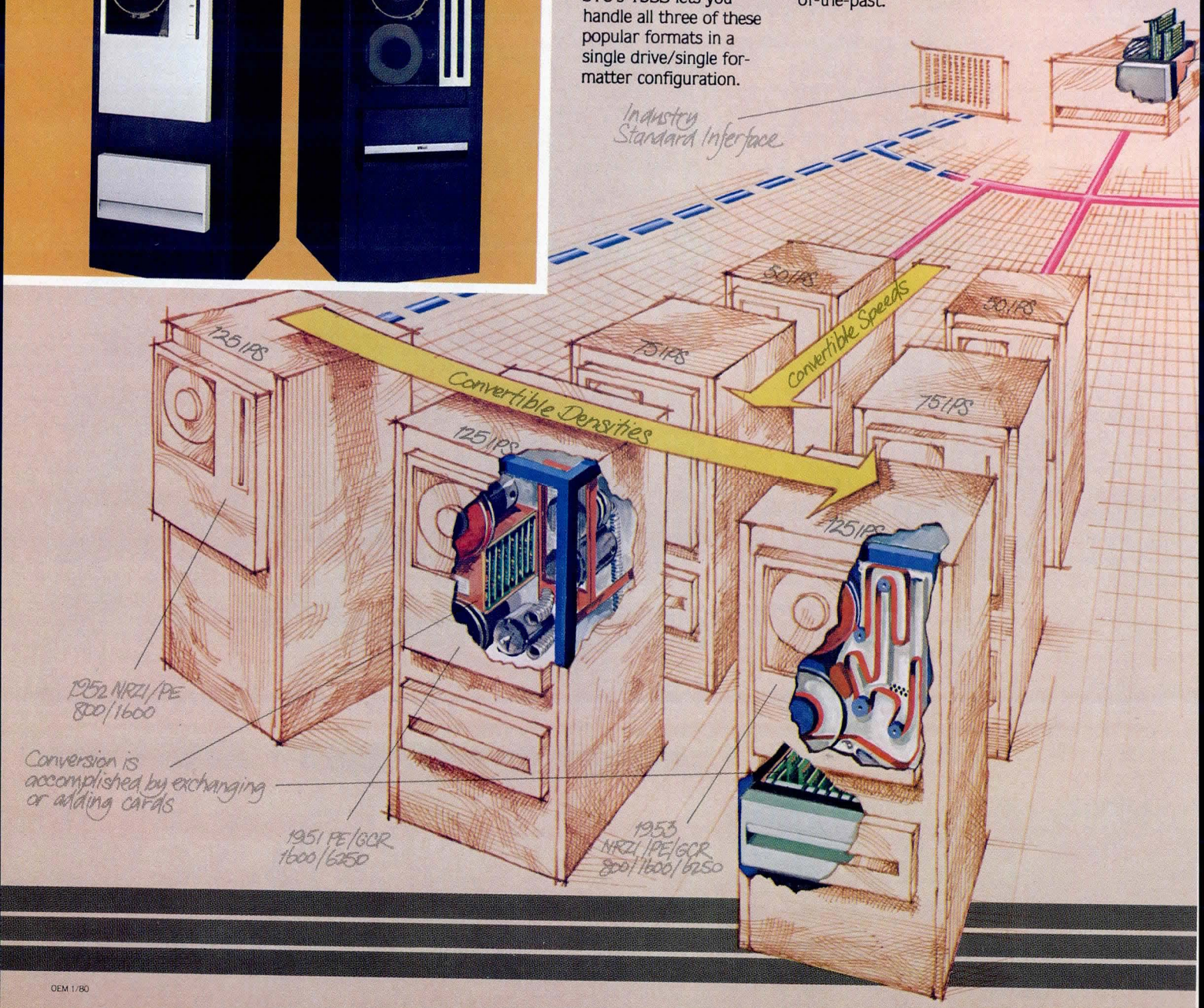

Practicality says design to cost. gives you both.

And for the ultimate in flexibility, 1900 subsystems provide a convenient growth path. With a few simple card changes, your field engineers can convert speeds and densities, on-site, in a matter of minutes.

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To assure fast, effective field service, STC provides you with the most comprehensive diagnostics in the industry. The 1900 Diagnostic Software features more than 180 routines including functional, reliability and artificial stress testing. Field experience has shown the package will deliver 95% fault detection and 70% isolation to one of three cards.

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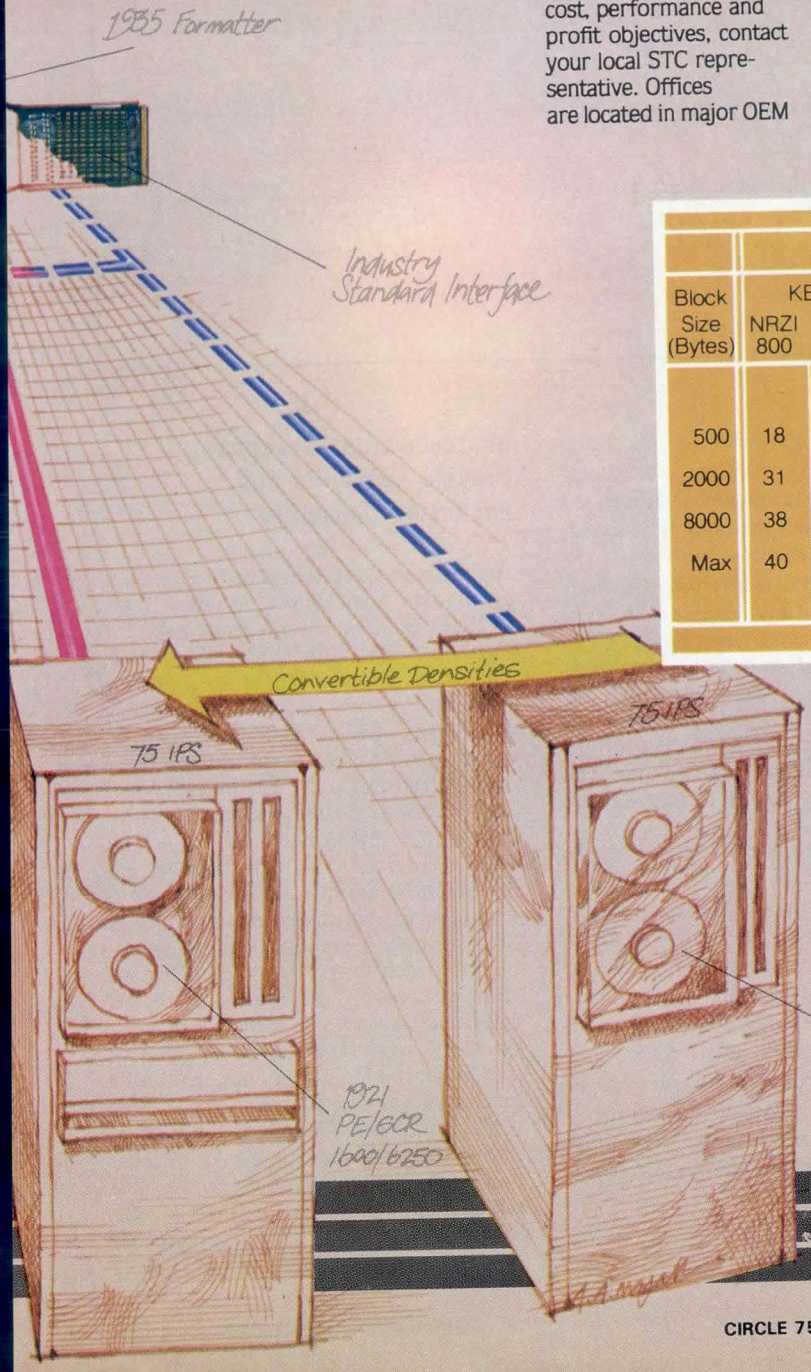
Or write Storage Technology Corp., P.O. Box 6, 2270 S. 88th Street, Louisville, CO 80027. Phone (303) 673-5151.

Block Size (Bytes)	50 ips KBytes/Sec NRZI 800	PE 1600	GCR 6250	75 ips KBytes/Sec NRZI 800	PE 1600	GCR 6250	125 ips KBytes/Sec NRZI 800	PE 1600	GCR 6250
500	18	27	62	28	42	94	47	70	156
2000	31	52	156	46	78	235	77	130	390
8000	38	71	249	57	107	379	96	178	624
Max	40	80	312	60	120	470	100	200	780



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CIRCLE 75 ON INQUIRY CARD

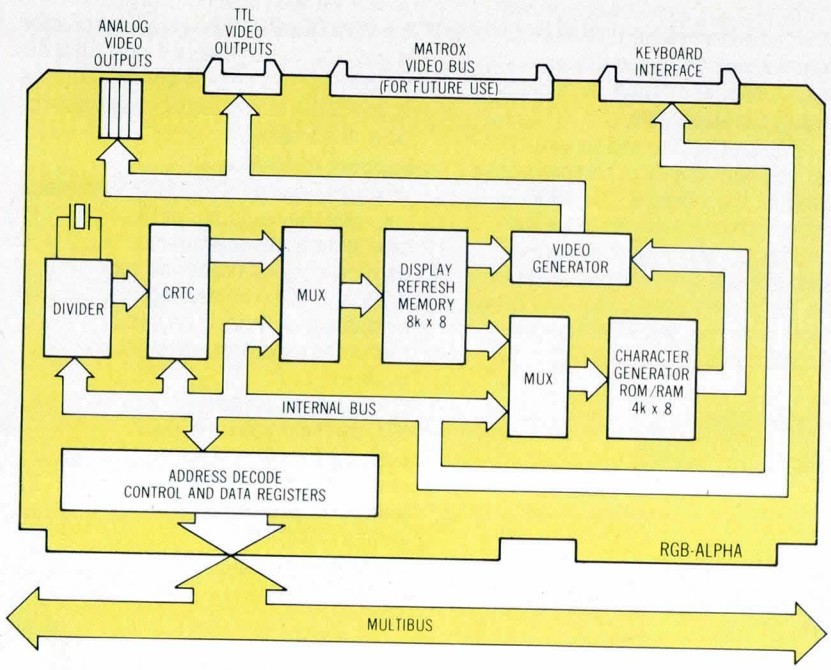
Color Video Display Controller Card Is Multibus Compatible

RGB-ALPHA, a color video display controller card, provides a complete color display generator and interfaces for a high speed lightpen and an 8-bit parallel keyboard on a single Multibus, LSI-11, or PDP-11 compatible card. Display and character formats in any combination of lines per page and characters per line, up to a maximum of 400 char/line, may be set by programmed I/O commands. In the character graphics mode, maximum resolution is 640 x 480 pixels interlaced, and 1024 x 240 pixels noninterlaced.

Features include 8 display colors, up to 4000 characters, 256 user defined characters, blinking and inverse video, addressable cursor, transparent memory, MC6845/HD46505SP CRTC, ROM/RAM character generator, and 50- or 60-Hz operation. The controller card is available from Matrox Electronic Systems Ltd, 5800 Andover Ave, TMR, Quebec H4T 14H, Canada

The character font contains 128 5- x 7-dot upper/lowercase alphanumeric characters and graphics symbols; by adding a second ROM, 128 additional symbols can be defined. Both character generator ROMs can be replaced by pin compatible byte-wide RAMs, permitting the processor to change fonts at any time by rewriting the character generator RAM. Each character can be specified to be one of eight foreground colors on one of eight background colors. Characters can be either single- or double-height, with character foreground and/or background normal or blinking at 2 Hz. Characters can also be underlined or stored in display memory but not displayed.

Each character position on the CRT corresponds to a location in the onboard 8k-byte display memory that occupies 1k, 2k, 4k, or 8k bytes of system address space depending on the display size. The system processor can read or write the display memory at full speed using all memory reference instructions. All accesses to the memory are transparent, and the processor can read or write the refresh memory at any time.



Color video display controller card. Offered by Matrox Electronic Systems, single Multibus, LSI-11, or PDP-11 compatible card integrates color display generator and interfaces for 8-bit parallel keyboard and high speed lightpen

To display a character, its ASCII and attribute codes are written into the appropriate memory display location. As the display refresh memory is scanned, the contents of each location select the appropriate bit pattern from the character generator and enables the appropriate character attributes. The display is scrolled up or down by changing the contents of the display start address register. When used as a console, the controller provides a 5- to 10-fold speed improvement in writing the display over a terminal receiving data at 9600 baud.

The controller, which plugs directly into the Multibus, works with any monochrome or color RGB video monitor at 50 or 60 Hz, and with both 8- and 16-bit microprocessors. It can be slaved to a color graphic display controller card to provide combined color alphanumerics and high resolution graphics. User-display interaction is possible using a high speed lightpen; however, a lightpen can be used only with monitors having short persistence phosphors.

Circle 463 on Inquiry Card

Microcomputer Systems Provide Flexibility and Expansion Capability

A Z80A based CPU serves as the basis for a line of S-100 based systems from California Computer Systems, 250 Caribbean Dr, Sunnyvale, CA 94086. This CPU provides realtime hardware vectored interrupt and interrupt nesting capabilities. Its DMA structure permits multiprocessing with interleaved data transfer rates of up to 2M bytes/s.

In addition, the CPU includes two programmable realtime clocks, two 8-bit parallel interface channels, and two independently baud rate programmable RS-232 serial I/O channels capable of asynchronous operation to 19.2 baud, one of which may also be used in synchronous mode. Available in either cabinet mountable or tabletop models, systems have a keylock power control switch and a power failure indicator located on the front panel.

Model 2210 provides 64k bytes of RAM, one serial I/O channel, a 12-slot chassis, power supply, controller, and CP/M operating system. Model 200 includes 32k byte of static RAM, hardware vectored

(continued on page 162)

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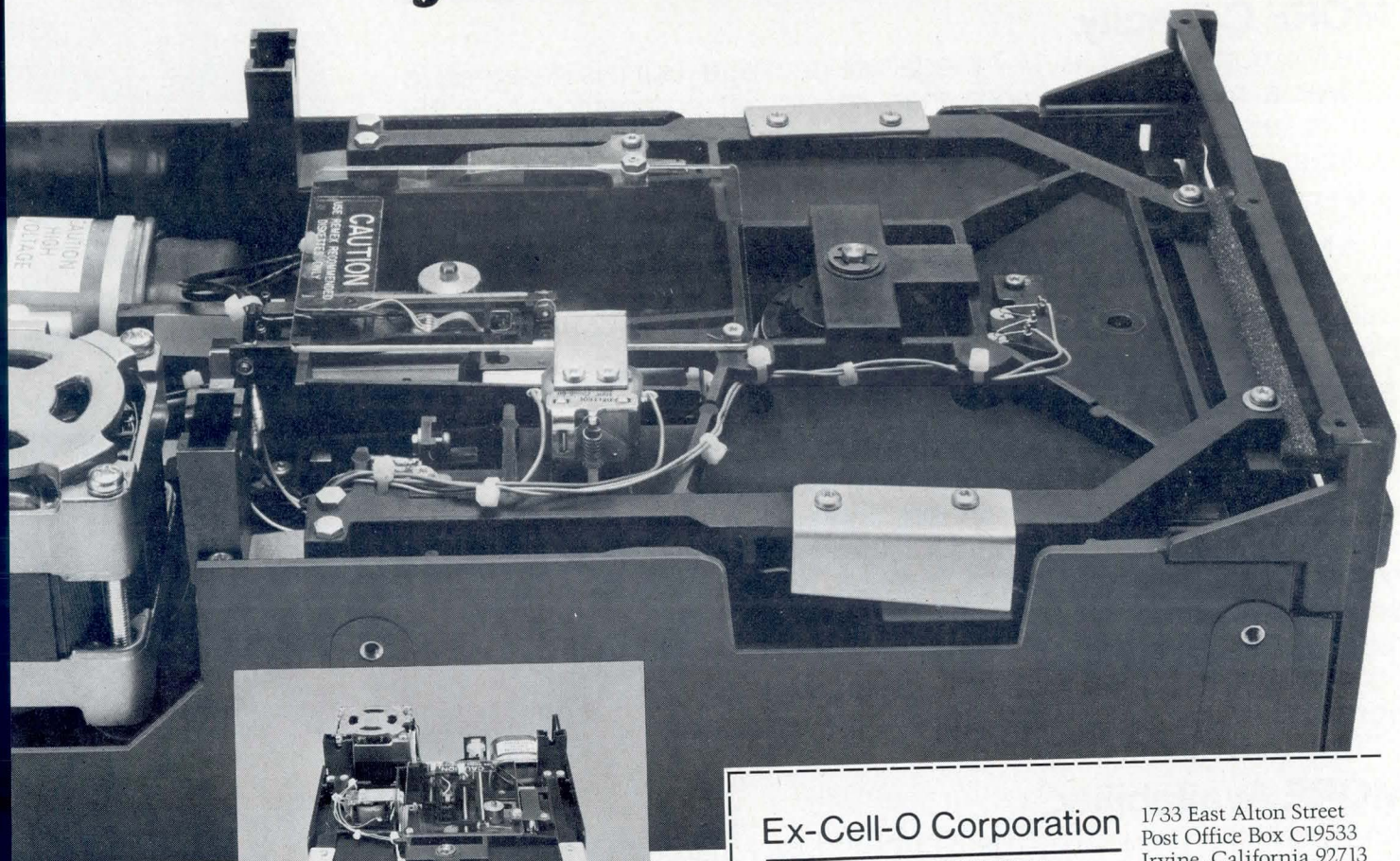
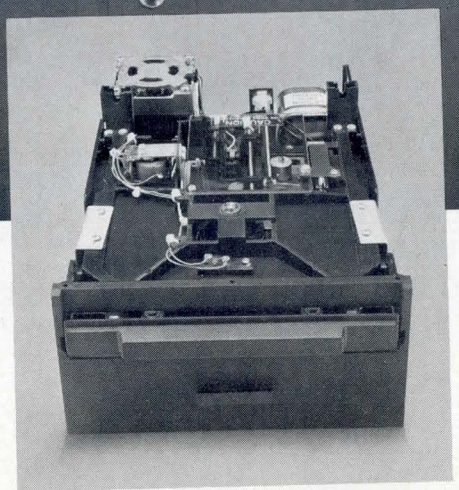


Remex RFD4000 Dual Head Flexible Disk Drive



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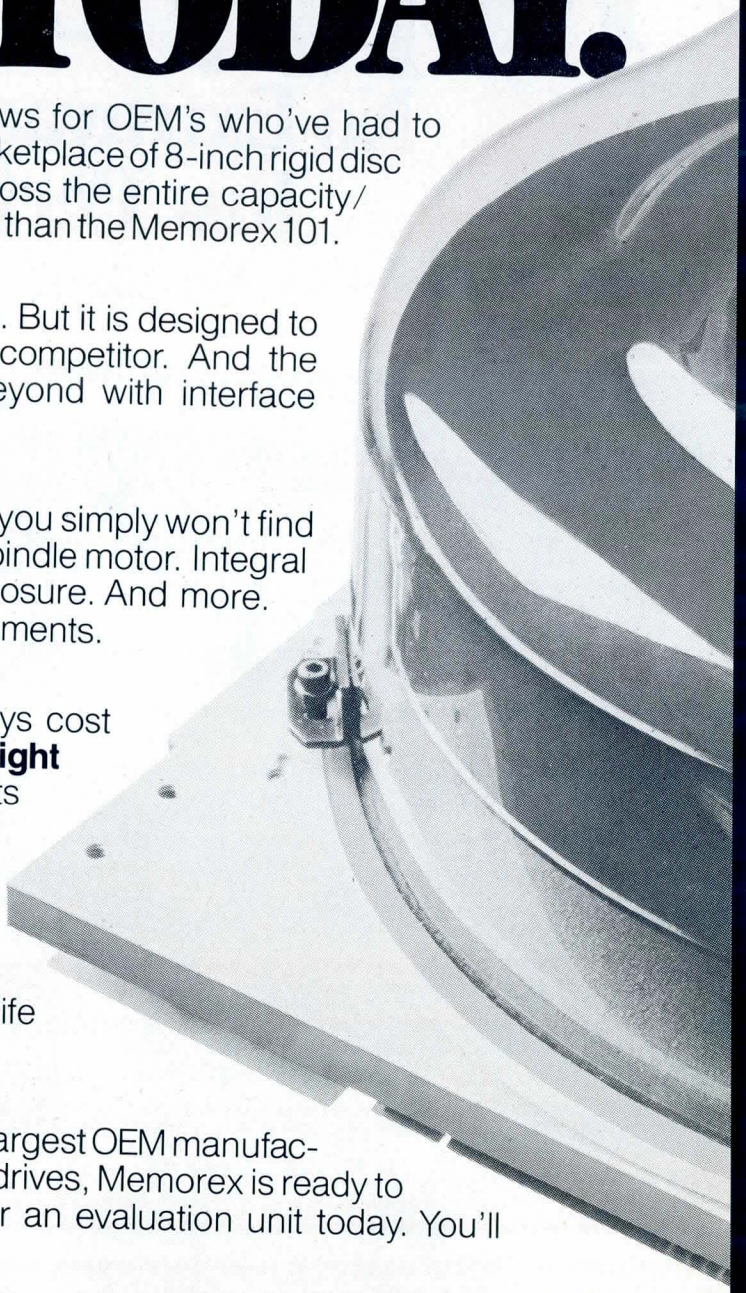
For a number of reasons, the Memorex 101 says cost efficiency like others cannot. Start with **more weight savings.** The 101 is a full five pounds lighter than its nearest competitor. And thanks to its all-DC power requirements, the 101 delivers **more energy savings** as well. Add to this the high-reliability design of the 101 and what you wind up with is a drive that is, bottom line, **more economical**—in the short run and over the whole life cycle of the product.



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CIRCLE 77 ON INQUIRY CARD

interrupt, power fail detect, DMA channel, two realtime clocks, two serial I/O channels, a Centronics parallel channel, 19-slot chassis, and power supply; model 300 is the same as the 200, except that it provides 64k of dynamic RAM, and a 2.4M-byte dual-floppy disc system. The model 400 is also the same as the 200, except that 64k of dynamic RAM and a 10M-byte Winchester disc subsystem are supplied.

A realtime, multitasking software operating system, OASIS features reentrant and relocatable program capabilities and uses an ISAM file structure. Task to task communications, file protection, timekeeping, spooling, overlay, and device independent I/O can be accomplished through software. The operating system is supported with debug, editing, relocatable linkage, and file sort utilities. CP/M and MP/M will also be available for use with the system. Available languages include a relocatable assembler, BASIC interpreter and BASIC compiler, and FORTRAN, COBOL, and Pascal compilers.

Full expansion of any unit is allowed by the modular design of the system family. Optional modules include 16k-, 32k-, and 64k-byte memory modules; a high speed arithmetic unit; serial and parallel I/O modules; floppy disc subsystems, floppy disc subsystem expansion, and floppy disc expansion drives; and Winchester disc subsystems and Winchester disc subsystem expansion.

Circle 464 on Inquiry Card

Single-Board Development System Offers Choice of CPU

ZX-85 single-board development systems feature the architecture and software of the Intel MDS Series II development system. Each development system includes 8085A-2 CPU with 10-MHz clock, boot/monitor in EPROM, 64k x 8 bytes of MM5290 dynamic RAM controlled by an 8202A DRC, two RS-232 channels with 8251A USARTs, two 8259A interrupt controllers, 5-MHz internal CPU operation, and 8219 Multibus arbiter, and is MDS IPB and Multibus compatible. The 8085A-2 CPU can be replaced by an 8088 CPU, and the monitor exchanged for one compatible with the CP/M-86 operating system.

The microcomputer boards are products of Zendex Corp, 6680 Sierra Lane, Dublin, CA 94566, and support various standard disc operating systems. Changeover from one CPU to the other is accomplished through the use of four row sockets provided for the CPU chips. Other devices that must be removed, installed, or changed to complete the switchover have sockets installed.

Designed for use in a standard SBC system, the processors are configured on 6.75 x 12.00″ (17.14 x 30.48-cm) circuit cards. The processor can also be run in the IPB slot of a Series II MDS chassis for an overall speed improvement. Compatible software includes Intel ISIS-II and CP/M for MDS-230 from Digital Research. Interfaces for Multibus, serial I/O, interrupt, and memory expansion are provided. Power requirements are 5 V ±5% at 2.25 A, 12 V ±5% at 0.09 A, and −12 V ±5% at 0.01 A.

Circle 465 on Inquiry Card

Module Allows User Programming of Microcomputer

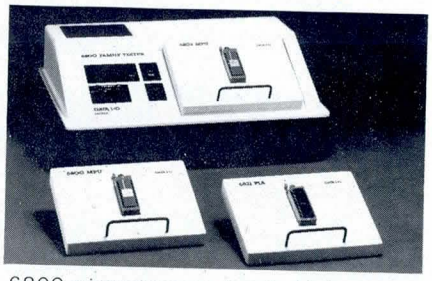
A programming module, available from Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, for use with the semi-custom MC6801 microcomputer, contains an M68701 MCU, 2k bytes of RAM, an RS-232 interface for the system terminal, and a 2k-byte ROM. The module enables users to program their microcomputers rather than have the procedure performed at the factory.

ROM contents provide the intelligence for programming the MC68701, as well as the monitor routines for loading and verifying programs that will reside in the EPROM. The only external hardware required is a power supply for the programming potential and module power.

The MCU is an offshoot of the MC6801, with one difference; while the MC6801 has onchip ROM, the MC68701 has onchip programmable EPROM that allows easy firmware corrections and provides convenient means for MC6801 software development. Both microcomputer units have the M6800 instruction set, serial communications interface, 16-bit timer, and RAM, and are pin for pin compatible.

Circle 466 on Inquiry Card

Device Tester Available For 6800 μProcessor Family



6800 microprocessor family device tester. Data I/O Corp model 1500A tests 6800, 68A00, 68B00, 6802, and 6808 microprocessors, 6810 RAMs, 6821 PIAs, and 6850 CIAs using software located on individual test adapters

Incoming inspection of 6800 family microprocessor and support devices is provided by the model 1500A device tester from Data I/O Corp, Box 308, Issaquah, WA 98027. The unit can test 6800, 68A00, 68B00, 6802, and 6808 microprocessors, 6810 RAMS, 6821 PIAS, and 6850 CIAS. With software located on individual test adapters, a series of functional tests specified to each device type is performed to determine whether dc parameters remain within the manufacturer's specified ranges. Performance is verified as the device is run at its upper, nominal, and lower V_{CC} ratings, with its outputs resistively loaded; ac performance is also verified, since the component is run at its rated speed.

In normal mode, the tester sorts out faulty devices in a batch, running a series of tests on each one in less than half a second. The continuous mode allows the tester to run its sequence repeatedly on a device suspected of intermittent or temperature related failures. A green light indicates a good device, and a diagnostic message points out a device failure. The tester requires neither additional software nor training to operate.

Circle 467 on Inquiry Card

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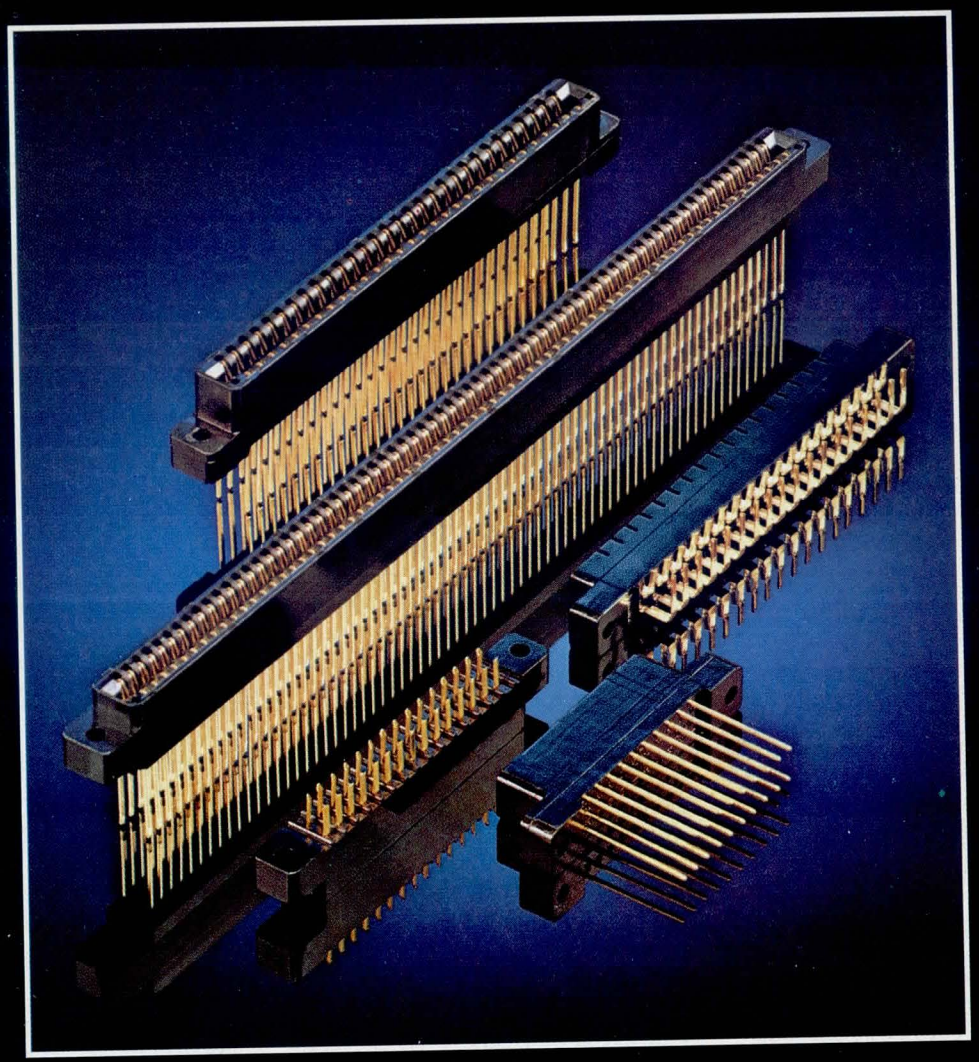

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CIRCLE 78 ON INQUIRY CARD

Personal Computer Serves Both Business and Technical Applications

HP-83 personal computer. Hewlett-Packard's typewriter sized unit features integrated keyboard and CRT, plus graphics capabilities

Identical to the company's HP-85 except that it does not include an integrated tape cartridge drive and integrated thermal printer, the HP-83 personal computer has been introduced by Hewlett-Packard Co, 1501 Page Mill Road, Palo Alto, CA 94304. The HP-83 is a powerful typewriter-sized unit with an integrated high resolution CRT and keyboard, enhanced BASIC language, and powerful graphics capabilities.

Two HP models of flexible disc drives, providing mass storage of from 270k to approximately 5M bytes, can be connected to either of the Series 80 machines. Both computers support the company's VisiCalc PLUS software and can communicate with various printers and plotters.

New Series 80 peripherals include the HP 9111A graphics tablet, which enables users to digitize or draw graphics with a pen on the tablet and see those graphics transferred automatically onto the CRT and memory. Diagrams such as schematics, computer aided designs, and circuit layouts can be easily entered and changed with the tablet. A parallel printer interface will allow the computers to be used with inexpensive printers when print quality is not critical.

A variety of business software packages were also introduced for both the HP-83 and the -85. The Information Management Pac is a database management tool for accessing, modifying, searching, and sorting data. Database totaling and statistics are included, as are report and graphics generation. Creating, updating, and printing out customer or mailing lists, inventory records, catalogs, and other data bases are easily handled by these programs. The Graphics Presentation Pac lets the user make 4-color overhead projection transparencies or report copies of text, bar charts, pie charts, and line charts. Three different character sets, nine variable letter sizes, and six different line and hatching styles are available. Greek and European characters, slanted or upright charcters, three alternate highlighting styles, and up to 25 slices per pie chart are also featured. The Data Communications pac enables the computers to perform intelligent terminal functions such as asynchronous communication at 300 to 9600 baud over a direct line or through a modem.

New software development tools make it easier for software developers to generate and distribute programs for Series 80 machines. The System Monitor debugs assembled code, an Advanced Programming ROM adds powerful BASIC commands, and a plug-in drawer for EPROMs is also available.

Circle 468 on Inquiry Card

Microcomputer Meets Harsh Environment Requirements

A 4k-byte RAM, 8k-byte EPROM microcomputer, the MC-65 CMOS system provides two pulse counters, two optically isolated sense inputs, and two spst relay outputs. Available from Micronet Ltd, PO Box 7066N, Halifax, Nova Scotia B3K 5J4, Canada, the system is programmed in 1802 Assembler or a high level concurrent Pascal, will support five user available realtime processes, and allows direct or scheduled control of relay outputs. Standard software features include storing 21 days of 15-min pulse count totals and sense input changes of state, a realtime clock, memory zeroing, and built-in system diagnostics.

Weighing under 1.5 lb (0.7 kg), the 7 x 9″ (18 x 23-cm) board is NEMA 4 enclosure compatible. Its standard operating temperature of −25 to 55 °C makes the board suitable for harsh environments. Power required is 12 Vac at less than 500 mA while charging the battery, and less than 150 mA otherwise. An optional 2.5-Ah battery plugged into the onboard charger provides RAM holdup for 30 days.

Circle 469 on Inquiry Card

μComputers Are Based On Ada Software

A family of ME1600 microcomputers featuring the Ada Microengine™ microprocessor is available from Western Digital Corp, 3128 Red Hill Ave, Newport Beach, CA 92663. Features of Ada, functionally a superset of Pascal, extend Pascal in four major areas: error recovery on exception handling, separately compiled packages, multitask synchronization via rendezvous, and strongly enforced user defined data types. System architecture features a 16-bit data path, 24-bit addressing (32M bytes), Sentinel/24™ bus, and multiprocessor architecture.

System Sentinel fault tolerance architecture complements Ada's error recovery features by providing error detection and recovery at the hardware level, and the system's capabilities are implemented on four levels. Level 1 is the device level where self-test features built into the system's LSI components continually test for failure, marginal conditions, or performance degradation. At level 2, each module contains a dedicated controller that polls the Sentinel pins of the LSI devices, performs checksums, and monitors power supply levels and temperature.

At level 3, the module continuously monitors all level 2 modules on the Sentinel/24 bus for pending fault or performance degradation, and maintains audit trail of bus activity for use in fault isolation and recovery. The level 4 module adds remote access capability and dynamic polling of level 2 and 3 functions, and allows system verification, interactive diagnostic, and software distribution from remote sites.

Phase I products, including Pascal/Ada processor, 128k bytes of RAM, floppy disc controller, four serial and one parallel I/O controllers, general purpose interface, chassis/power supply, UCSD Level III.0 Pascal software system, and selected development configurations, are available in limited quantities for OEM and private label applications. Phase II products, including storage module hard disc controller, cryptographic security module, memory error correction module, System Sentinel level 3 module, TSI-Ada compiler from TeleSoftware, Inc, and a distributed multiprogramming operating system, are scheduled for May delivery. Phase III products will exploit proprietary X.25 packet switching and local network products.

Circle 470 on Inquiry Card

Introducing quality print at matrix speed. For only $1295.*

Until now, you could pay thousands for a slow, letter-quality character printer. Or hundreds for a dot matrix printer, giving up print quality for speed and price.

But that was before Paper Tiger™ 460 offered you a better choice.

The new Paper Tiger 460 is the first matrix printer with high-density dot matrix characters plus high speed. At a low price.

The secret? A unique nine-wire, staggered matrix head provides overlapping dots in both horizontal and vertical planes. The result is dense, high-quality characters you'll be proud to show off.

What's more, Paper Tiger 460 gives you a combination of features simply not available on any other printer, at any price. Like bi-directional, logic-seeking printing at speeds in excess of 150 cps. Microprocessor electronics, with field-installable character sets. Proportional spacing. Automatic text justification. DotPlot™ high resolution graphics option. RS232 and parallel interfaces. And more.

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Automatic proportional spacing,
processing systems, plus the cap
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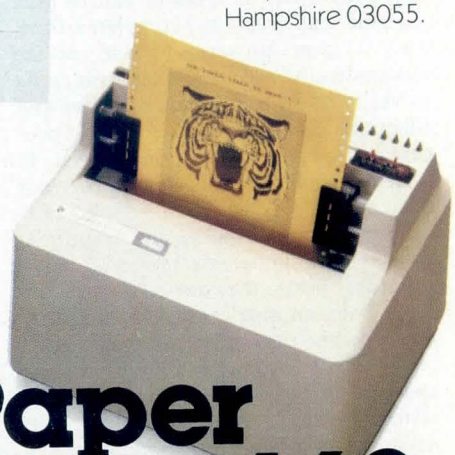
Paper Tiger 460 Print Sample

But its most important feature is high reliability. The Paper Tiger 460 is designed to be tough and dependable. It has rugged, stepper-motor head and paper drives. A new rugged ballistic-type print head.

And its simple, chassis-mounted cartridge ribbon lasts up to four times longer than cassette or spool ribbons.

All this means that Paper Tiger 460 is perfect for word processing, data processing, or electronic mail. It's also perfect for anyone who requires the flexibility of a matrix printer but wants superior quality printing. Without trading off speed or price.

Get your paws on the Paper Tiger 460, and join the tens of thousands of satisfied Integral Data Systems users. Call us toll-free: 800-258-1386. (In New Hampshire, Alaska, and Hawaii, call (603) 673-9100.) Or, write for complete specifications. Integral Data Systems Inc., Milford, New Hampshire 03055.



Paper Tiger 460

Integral Data Systems, Inc.

*Suggested single-unit, U.S. price. Generous OEM discounts available.

CIRCLE 79 ON INQUIRY CARD

Incircuit Emulator Simulates, Reads, and Programs EPROMs

An incircuit emulator for EPROMs, the Micro Memory Tracer is an intelligent ROM simulator for designing and debugging microprocessor hardware and software, and replaces up to four 2708 or two 2716 EPROMs, or one 2732 EPROM, in a microprocessor system. The product, available from Logical Services Inc, 2340A Walsh Ave, Santa Clara, CA 95051, can simulate EPROMs in a system under test, display and change program memory, trace program execution in real time using simulated ROM, display a simulated ROM access map on CRT, count accesses to specific locations during trace, guard against unintended memory access, and capture data during realtime trace. It can also accept serial data from a host computer or a development system, drive a line printer, and read and program EPROMs. Object programs are downloaded from a host development system or timeshared computer into high speed RAM within the tracer via an RS-232 port. When the system hardware and software finally operate correctly together using the simulated ROM, the built-in EPROM programmer can create the completed firmware. Upon power up, the device automatically executes diagnostic tests to verify its own internal memories and functions. Since it is independent of processor type, it can be employed in systems using various microprocessor devices.

In the terminal mode, and connected to a host computer via the serial RS-232 interface port, the device's CRT and 53-key alphanumeric ASCII keyboard interact with the host computer as a remote data terminal using the protocol specified for the host computer. As a terminal, the device can enter, edit, assemble, compile, read, store, or otherwise handle programs in accordance with the host computer's capabilities. When operated as a ROM simulator, the device is a standalone system using an internal high speed RAM connected to the 24-pin EPROM sockets in the system under test. Object programs can be displayed, changed, patched, and executed out of emulated ROM to avoid repetitive EPROM programming during debug.

System operating temperature is 16 to 32 °C, at humidity levels of 20 to 80%. Power required is 115 Vac, 60 Hz, 3 A. The device measures 17 x 5.5 x 17.5″ (43 x 13.9 x 44.4 cm), and weighs 45 lb (20 kg).

Circle 471 on Inquiry Card

Universal Peripheral Controller Chip Assumes Host Processor Tasks

Tasks such as arithmetic, translation, formatting of data, and control of I/O devices, traditionally performed by the host computer, are assumed by the Z8090 universal peripheral controller (Z-UPC). An intelligent device designed for distributed processing and multitasking applications, the controller has a powerful and extensive instruction set and an efficient internal addressing scheme to speed program execution and pack program code efficiently into the onchip ROM.

Based on the Z8 single-chip microcomputer, the controller features 2k bytes of internal program ROM, a 256-byte register file, three programmable 8-bit I/O ports, two counter timers, and six levels of internal prioritized interrupts, and supports a daisy chain interrupt structure. It is available in sample quantities from Zilog, 10340 Bubb Rd, Cupertino, CA 95014.

Three I/O port registers, 19 status and control registers, and 234 general purpose registers are contained in the Z-UPC's internal register file. I/O ports and register file can be accessed by both the Z-UPC program and its associated master CPU, facilitating byte and programming efficiency; the master CPU's access to the register file is controlled by the Z-UPC. Twenty-four of the controller's 40 pins can be dedicated to I/O functions; grouped logically into three 8-line ports, these can be programmed in various I/O combinations with or without handshake. Two programmable 8-bit hardware counter/timers relieve the controller's software of handling realtime counting and timing problems; each has a 6-bit prescaler, and is independent of program execution.

Four optional versions of the controller are available, as well as the standard configuration: Z8091, a 64-pin development version with interface for up to 4k bytes of ROM; Z8092, a 64-pin version with external interface for up to 4k bytes of RAM which can be downloaded from the master CPU; Z8093, a 40-pin protopack version with a socket for up to 2k bytes of ROM; and Z8094, a 40-pin protopack RAM version with a socket for up to 2k bytes of RAM which can be downloaded from the master CPU. These four prototyping devices cover a wide range of system peripheral device control needs, and are available in sample quantities of 10 to 99.

Circle 472 on Inquiry Card

Computer Systems Expand To Accommodate Multiple Users

Modular microcomputer systems from White Computer, 1876 Industrial Way, Redwood City, CA 94063, support single and multiple users with hard disc and tape backup option. The Winchester/floppy disc system includes a Z80A CPU, 64k bytes of dynamic RAM, a 35M-byte 8″ (20-cm) Winchester fixed disc, an 8″ (20-cm) single-sided, single/double-density floppy drive, and one parallel and two serial ports for terminals, printer, or communications. The dual floppy disc system includes a Z80A CPU, 64k bytes of dynamic RAM, dual 8″ (20-cm) single-sided, single/double-density floppy drives, and one parallel and two serial ports.

Both systems can be backed up by either a streaming cartridge tape with 17M-byte cartridges, or by removable hard discs, and are delivered with CP/M operating systems. Multiuser options employ a time-sliced MP/M system that executes CP/M applications and languages for up to eight users.

Each system can support a series of expansion options, including a cartridge disc system with 16M bytes of removable cartridge and 16M, 60M, or 80M bytes of fixed disc storage, field upgradable. Double-sided drives with 1M-byte floppy disc storage per drive, 8″ (20-cm) Winchester fixed discs for 7M, 21M, or 35M bytes of storage, and 14″ (35-cm) Winchester fixed discs for 33M or 40M bytes of storage are also available as options. Each disc system can support up to four drives per controller.

Circle 473 on Inquiry Card

TOTAL CDC COMPATIBILITY AND GREAT DELIVERY, TOO!

The only thing worse than not having enough disk storage, is not being able to get enough disk storage.

Fortunately, the Ampex DM-9300AQ solves both problems. With 300 megabytes of reliable disk pack storage and off-the-shelf delivery.

But the advantages of the DM-9300AQ don't stop with delivery. It's completely compatible with CDC's 300 megabyte drive. So disk packs can be interchanged, written on, or read by either drive. Of course, the industry standard SMD interface, and power sequencing of both units are also compatible.

DM-9300AQ disk pack swapping is as easy as using them. Its large front opening has been designed with the convenience of a top loader, and human engineered for minimal lifting. So even a 20-pound pack is easy to insert and remove. It's such a good idea, we're surprised somebody didn't think of it sooner.

But then, the DM-9300AQ is full of good ideas. Like highly reliable on-track servoing, and a single port daisy-chain interface with ribbon cable that can be converted—in the field—to an internal dual port.

And the same goes for maintenance. Service requires only front, rear, or top access. Side access is eliminated, so you can arrange the units side by side. What's more, the logic chassis in the rear of the unit swings out to provide easy access to all test points and connections. And extensive use of LEDs simplifies trouble-shooting.

The DM-9300AQ has a lot to offer. But what's even better, is that it's all offered right now. With delivery that's ready when you are.

The DM-9300AQ. Just one of a complete line of Ampex plug compatible disk drive memories for nearly any CPU.

For more information, contact Gary Owen at Ampex Memory Products, 200 North Nash Street, El Segundo, California 90245. If you're really in a hurry call him at 213/640-0150. Or contact your local sales office.

Either way, we won't keep you waiting.

AMPEX

MAKES THE DIFFERENCE.

CIRCLE 80 ON INQUIRY CARD

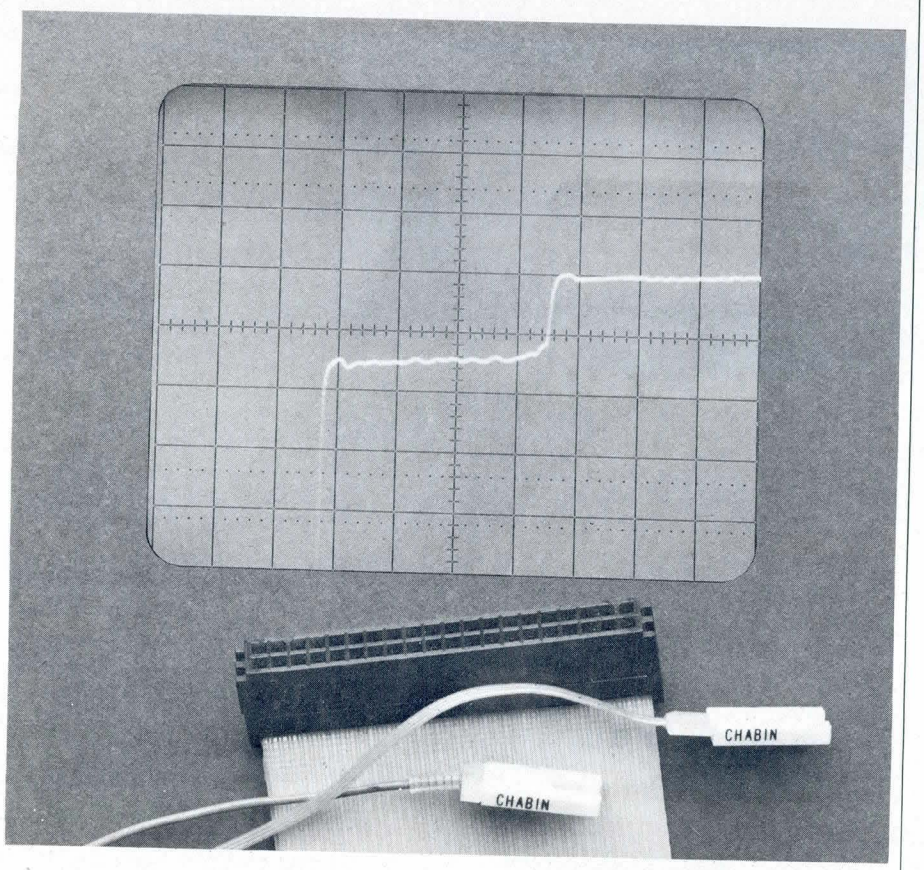
Color Graphics Capability Available for Small Business Computers

A memory expansion set and a color graphics board are now offered by Heath Co, Benton Harbor, MI 49022, for the H-8 and All-In-One computers. The WH-88-16 64k wired memory expansion set increases memory capacity of the All-In-One computer to 64k bytes of RAM when using the company's standard CP/M operating system; RAM capacity is 56k bytes when the set is added to the same computer using the company's disc operating system and 48k of RAM. The HA-8-8 extended configuration option increases the H-8's memory capacity to 64k bytes of RAM when used with the company's CP/M operating system, and also includes a replacement front panel ROM.

The HA-8-3 color graphics board uses the Texas Instruments TI-9918 color video display generator. An AY-3-8910 programmable sound generator is also included. Eight ADC channels can handle up to four X-Y joystick consoles, each of which has four bits of parallel I/O for switches or LEDs. A socket is also provided for the AMD-9511 arithmetic processor chip. The board connects to the video input of most video monitors as well as other video accessories using NTSC composite color video.

Demonstration software for the color graphics board is provided on a 5.25″ (13.33-cm) floppy disc. Additional software for the board will be offered through SOFTSTUFF, the company's software line.

Circle 474 on Inquiry Card



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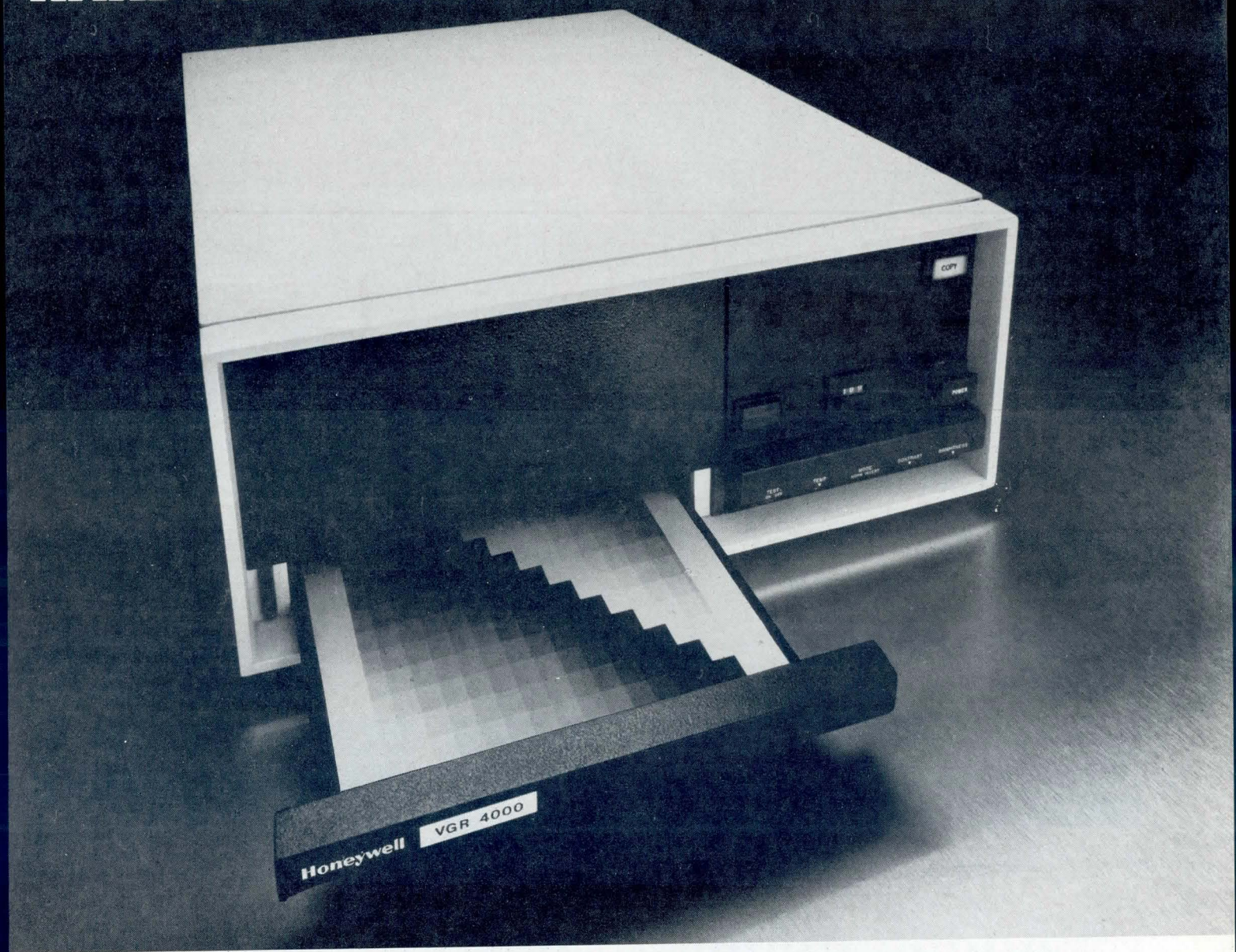
μProcessor Enhancement Modules Increase System Throughput

8080A incircuit emulation is performed by the Series II microprocessor enhancement modules using a code compatible Intel 8085A-2 processor. As a result of the reduced memory access time requirements of the 8085A-2 processor, a throughput increase of from 1.5 to 2.5 times is claimed to be possible. Installation of the modules involves only the replacement of the 8080A processor with a software compatible 8085A-2 processor, and status latch with DIP connectors. Flat 6 or 12″ (15 or 30-cm) cables allow the module to perform in tight spaces, and various mounting configurations are available. The modules are available from Paragon Systems Inc, PO Box 2050, Corvallis, OR 97330.

Three models are offered: Series II-8228 for 8080A with 8228 systems, Series II-8212 for 8080A with 8212 systems, and Series II-273 for 8080A with 74LS273 systems. The modules measure 4.5 x 3.5 x 0.5″ (11.4 x 8.9 x 1.3 cm). Power dissipation is 2.0 W max, and clock frequency is 5 MHz.

Circle 475 on Inquiry Card

THE LATEST ADVANCE IN VIDEO GRAPHIC HARD COPY RECORDING FROM HONEYWELL



VGR 4000, Honeywell's new and advanced video graphic recorder, provides fast, crisp, 8½ x 11" hard copies on dry silver paper from most CRT's and other video sources.

White-on-black or black-on-white images are as simple as flipping a switch. With options, images can be produced having up to 16 shades of grey or even more.

An innovative processing technique eliminates the need for large heated platens. This allows the recorder to run cool, consuming very little energy.

The VGR 4000 is the only recorder on the market available with a self-contained test-pattern generator providing a choice of formats for proper copy verification.

Rugged, yet cleanly designed for easy operation, the compact VGR 4000 can be used on a desk top or rack-mounted, taking up only 7" of front panel space.

Honeywell's VGR 4000 is the latest advance in video-input hard-copy reproduction systems, built by the people with the most fiber-optic CRT recorder experience in the field.

To get the whole story on the VGR 4000 and how it can meet your needs, call Durke Johnson at 303/773-4700. Or write Honeywell Test Instruments Division, Box 5227, Denver, Colorado 80217.

WE'LL SHOW YOU A BETTER WAY.

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HON-6-631

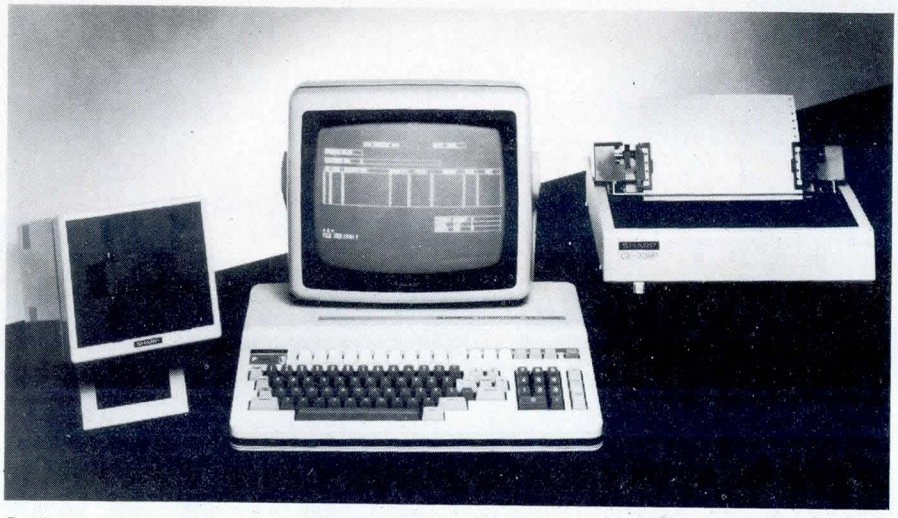
CIRCLE 82 ON INQUIRY CARD

Desktop Business Computer Offers Expansion Capability

A Z-80 CPU, high resolution CRT, floppy disc drive, and an impact printer are included in the YX-3200 business computer from Sharp Electronics Corp, 10 Keystone Pl, Paramus, NJ 07652. The desktop system features a 32k-byte ROM/64k-byte RAM that is expandable to 72k-byte ROM/128k-byte RAM, automatic program generator, and extended BASIC language.

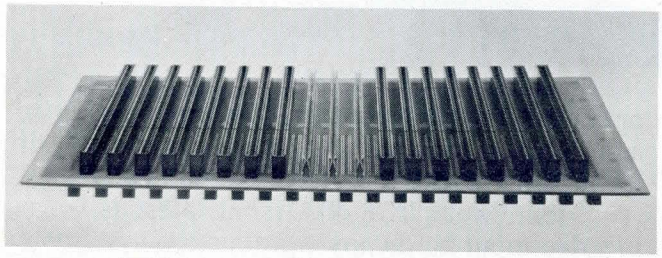
Up to eight 5.25″ (13.33-cm) dual-sided, double-density floppy disc drives can be accommodated. The CRT offers upper- and lowercase green characters on an 80-col, 24-line screen; the character size can be increased to a 40-col, 15-line display for group viewing or graphics purposes. The bidirectional, dot matrix printer offers 80-char/s printing speed and 80-col, 132-line capability.

Circle 476 on Inquiry Card



Desktop business computer. Sharp Electronics Corp's YX3200 includes CRT, floppy disc drive, and impact printer

Backplanes



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CIRCLE 83 ON INQUIRY CARD

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Now that SAE's EMI filters are recognized around the world, isn't it time *you* recognized them?

All SAE filters are suitable for use in equipment that has been designated by the FCC as a *computing device* and are designed to help meet the new conducted emission requirements.

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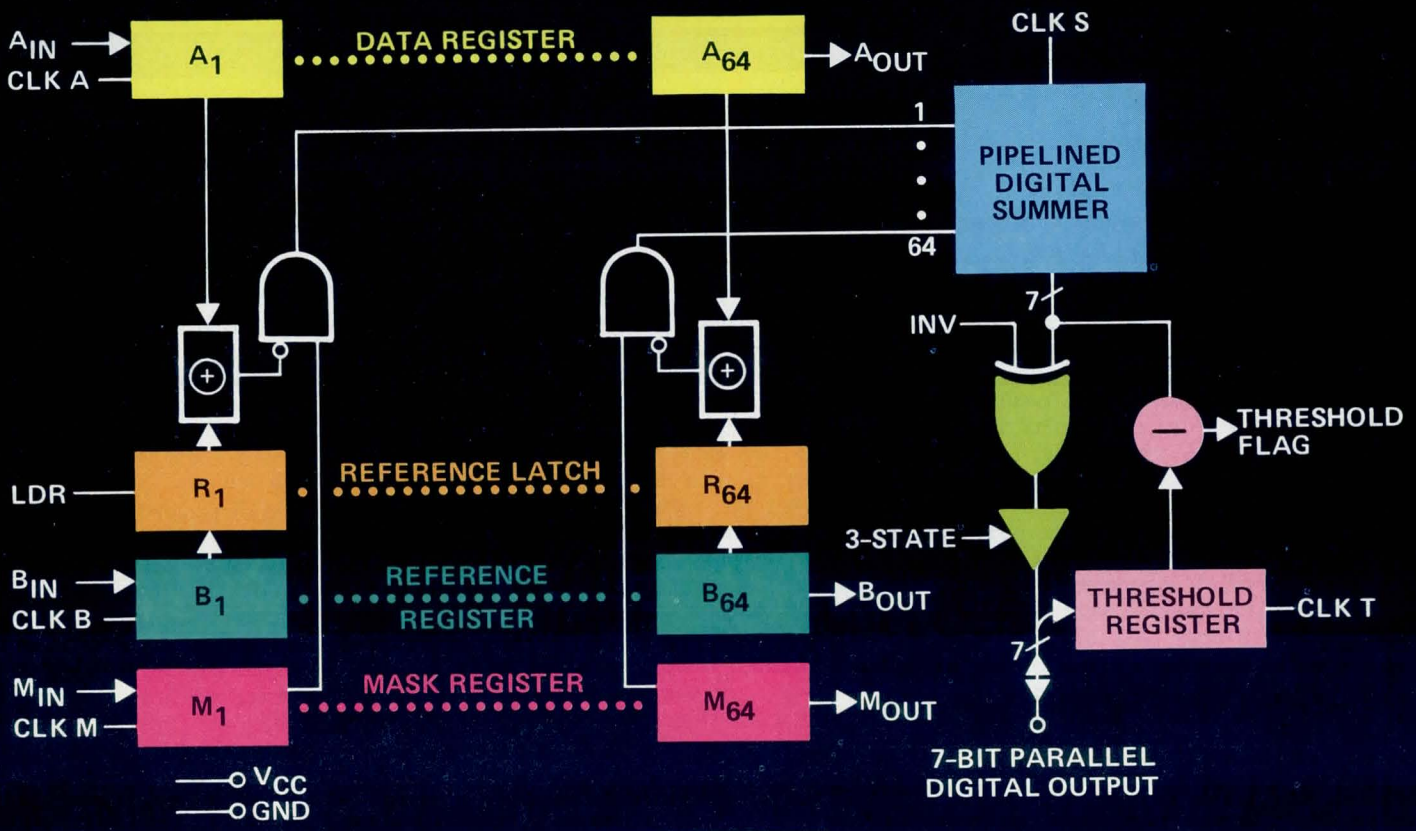

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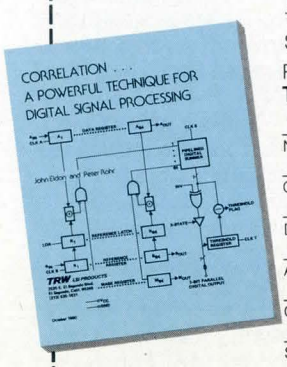

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BRIEFS

Debugging Program Is Both Software Emulator and Realtime Debugging Monitor—RAID software debugging tool for 8080/8085 microcomputers, available from Lifeboat Assocs, 1651 3rd Ave, New York, NY 10028, uses CP/M operating system, is written in 8080 assembly language, and requires only 13k bytes of space and no overlays. Features include multiple breakpoints, symbolic input of arguments, symbolic display and alteration of registers, and a built in assembler and disassembler. Eight input and display formats, memory search, and direct disc access via track and sector are also provided.
Circle 477 on Inquiry Card

Memory Modules Expand Personal Computer Capability—RAMCRAM's 16 memory chips alllow a total of 32k bytes of RAM to be added to the Atari 400 and 800 personal computers; the plug-in modules both upgrade system capabilities and provide for future expansion. The Atari 400 system can be expanded to 32k bytes of RAM, and the Atari 800 to 48k bytes of RAM using these memory modules from Axlon, Inc, 170 N Wolf Rd, Sunnyvale, CA 94086.
Circle 478 on Inquiry Card

Pascal Versions Offered for a Variety of Microprocessors—Micro Concurrent Pascal (MCP), a Pascal based high level language offered by Enertec, Inc, 19 Jenkins Ave, Lansdale, PA 19446, for realtime programming of 8086, Z80, 8080/8085, and 1802 microprocessors, supports the full addressing range of the processor in use. μCP programs compile into pseudo code (P-code) that can either be interpreted or used to generate pure code for microprocessors.
Circle 479 on Inquiry Card

Compiler System Offered for North Star BASIC—A full compiler system for North Star BASIC, Comstar is available from Allen Ashley, 395 Sierra Madre Villa, Pasadena, CA 91107, for double- or quad-density systems only. The compiler translates a North Star type 2 (program) file into an assembly language program, and then into a fully operational machine language program that runs faster than its BASIC equivalent. The system uses approx 12k bytes of memory with additional space required for data storage, and is available for DOS located at either 100H or 2000H.
Circle 480 on Inquiry Card

Microprocessor System Power Supply Meets Requirements of Single- and Dual-Floppies—Floppy disc drives plug into the output connectors of the model FD503 8-A power supply from CEI Corp, PO Box 501, Grenier Industrial Park, Londonderry, NH 03053. Power supply outputs are 5 Vdc at 8 A, 12 Vdc at 2.5 A, −5 Vdc at 1 A, −12 Vdc at 0.5 A, and 24 Vdc at 1.5 A continuous/4 A surge; positive outputs are regulated to 0.1% and negative outputs to 1%. Power input is 115/230 Vac, 50/60 Hz. Circle 481 on Inquiry Card

High Speed Memory Allows Maximum Processor Throughput—A dynamic memory system, CI-6800-2 is available in 16k, 32k, 48k, or 64k configurations from Chrislin Industries, Inc, Computer Products Div, 31352 Via Colinas Suite 102, Westlake Village, CA 91361, and allows maximum processor throughput with the use of onboard hidden refresh control logic. For use with Motorola's EXORcisor I and II, and Rockwell 65, the system features onboard memory select, onboard even parity with jumper selectable output, clock rates in excess of 1.5 MHz, 225-ns data access time, and 400-ns cycle time. Circle 482 on Inquiry Card

C Compiler Supports All C Language Facilities—For use with the 68000 microprocessor under Motorola's VERSAdos operating system, a C compiler that supports all facilities of the complete C language is available from Whitesmiths Ltd, PO Box 1132, Ansonia Station, New York, NY 10023. C programs can be intermixed with assembler code or other languages with the use of suitable interface protocols, and the portable C library provides approximately 80 functions for machine independent string manipulation, formatted data I/O, and controlled storage allocation. Circle 483 on Inquiry Card

Disc Drive Increases Small Business Computer's Storage Capacity—The "Octo-density" 5.25" (13.33-cm) flexible disc drive for 6809 series Chieftain small business computers provides 1.5M bytes of formatted storage capacity in its standard dual-drive configuration. A product of Smoke Signal Broadcasting, 31336 Via Colinas, Westlake Village, CA 91362, the drive incorporates a double-track, double-bit, double-sided design, features a recording density of 5877 bits/in (2314/cm) with 80 tracks/side, and has track to track time of 3 ms.
Circle 484 on Inquiry Card

Universal EROM Programmer Available for Sprint 68 System—The ROMMR programmer is available from Wintek Corp, 1801 South St, Lafayette, IN 47904, as an option to the Sprint 68 microcomputer/development system. It can erase test, program, and verify 2708, -58, -16, -32, and -64; 2516, -32, -64; and 68764 series EROMs.
Circle 485 on Inquiry Card

Z-80 CPU Board Available for S-100 Based Systems—CB2 Z80 CPU board operates at 2 or 4 MHz by DIP switch selection and includes sockets for two 2716 or 2732 EPROMs or HM6116 2k-byte RAMs. Available from SSM Microcomputer Products, 2190 Paragon Dr, San Jose, CA 95131, the board features firmware vector jumps and an output port to control eight extended address lines, permitting use of more than 64k bytes of additional memory within the board. Separate run/stop and single/step switches permit system evaluation without the need for a front panel.
Circle 486 on Inquiry Card

Cross Assembler Transforms Computers into Development Systems—Cross assemblers generate Intel 8080/8085 programs and combine with a Millenium MicroSystem emulator to transform various computers into development systems for the 8080/8085 family. Available from Millenium Systems, Inc, 19050 Pruneridge Ave, Cupertino, CA 95014, the assemblers also combine with the company's FASTPROBE software, generating diagnostic programs for production test and field service. Programs include MACRO assembler, linking loader, formatter/downloader, and analyzer or designer; FORTRAN source code is provided on floppy disc or magnetic tape.
Circle 487 on Inquiry Card

APL Available for Apple Computer Systems—APL/V80 for Apple computers requires CP/M, Microsoft's Z80 Soft Card, and a 24 x 80 video card, and includes 11 APL arithmetic functions, 11 Boolean and relational functions, 11 selectional and structural functions, and 9 general functions. A product of Vanguard Systems Corp, 6901 Blanco, San Antonio, TX 78216, the language contains system variables and functions such as canonical representation, function fix, and share offer and retract. An auxiliary processor for interfacing I/O ports and one for indexed file systems are provided.
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SOFTWARE

Control and Monitoring Software Provides Computer Control of Controllers

PM550 network software is a control and monitoring package that interfaces one or more TI PM550 programmable controllers to a TI model 990 computer, under the DX10 operating system. It allows 2-way access to each controller, either through a computer terminal or from the user's program. Communication between computer and controller is transparent to controller operation.

This package, available from Computer Technology Corp, Park 50 Technecenter, 2002 Ford Circle, Milford, OH 45150, allows users to define and implement applications without concern for details of host to controller communications. The user can also initiate internal self-diagnostic routines and create batch programs for automatic cycling of the diagnostics.

In production, the package eliminates manual reprogramming after a shutdown by allowing programs to be copied and distributed to other controllers or systems. In systems using multiple controllers, the software gives the computer both monitoring and control functions; the computer can automatically make programmed changes in any or all controllers, as required. If a controller fails in operation, it can be replaced as a unit, and the program installed in the replacement unit instantly. Where complex processes make status monitoring difficult, computer interfacing permits all variables to be tested continuously for display, recording, or realtime analysis.

Through a high level interactive command language, controller memory contents can be viewed, and new values for variables or constants can be written. Parts or all of the memory can be uploaded into a computer file, and then downloaded to the same or other controllers. High and low level routines are written as Pascal procedures, but are accessible from any language; these routines can read and write to specific memory locations or to controller image registers, test status and error tables, and examine PID loop values. At a lower level, routines that interface directly to the device service routine are included, written in assembly code for maximum efficiency. All the routines link with standard TI Pascal libraries.

Hardware/software requirements include a computer interface module. Connection to the computer is by RS-232-C interface operating at up to 4800 baud. The computer requires a TTY/EIA terminal interface module for each controller connected, and the operator interface is written for a video data terminal.

Circle 489 on Inquiry Card

RESEARCH REPORT

CHINESE AND RUSSIAN COMMUNICATIONS MARKETS

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- Reviews the opportunities and constraints in relation to marketing in China and Russia, along with a discussion of possible future export control considerations.
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COBOL Package Uses 8086 Power to Triple Execution Speed

COBOL-86, available for OEM licensing from Microsoft, 10800 NE Eighth, Suite 819, Bellevue, WA 98004, provides full use of the extended power and speed of the 8086 microprocessor. The compiler executes three times as fast as the 8080 version, and uses the processor's expanded register set, extra addressing modes, and powerful arithmetic instructions to implement high performance algorithms for computation, program control, and character operations.

The COBOL-80 compiler was mechanically translated, and the runtime system rewritten into smaller and faster 8086 code to form COBOL-86. The package uses the Intel medium model of computation to fully utilize the microprocessor's expanded memory space. It generates reentrant object code, allowing multiple users to share either object programs or the runtime system, or both; the runtime system is also reentrant. CHAINing, full screen ACCEPT/DISPLAY, program and data structuring tools, and an advanced verb set—STRING, UNSTRING, COMPUTE, SEARCH, and PERFORM (VARYING/UNTIL)—are provided.

Circle 456 on Inquiry Card

Software Warranty Extended to Provide Replacement and Backup

Replacement and backup coverage have been added to the existing 90-day limited warranty policy offered by Personal Software Inc, 1330 Bordeaux Dr, Sunnyvale, CA 94086. This coverage for the Productivity Software Series is designed to alleviate user concern about being without software for a sustained period of time.

During the 90 days of the limited warranty, and to the original purchaser only, the magnetic disc on which the VisiCalc, Desktop/Plan, and CCA Data Management System programs are recorded will be replaced free of charge by a company dealer or by mail, if the diskette is defective in quality or workmanship. After the 90-day warranty, and up to 1 year from purchase, a defective diskette will be replaced for $20.00. Prepayment and the original disc must accompany requests for replacement.

For a $30.00 fee, one backup diskette per customer will be provided for those programs protected from copying. Both Apple II and Atari 800 VisiCalc programs are currently included. For either replacement or backup diskettes, the dealer must first receive the program warranty card or other proof of purchase from the owner. The complete warranty, replacement, and backup statement is available with each productivity product packaged after Jan 1, 1981.

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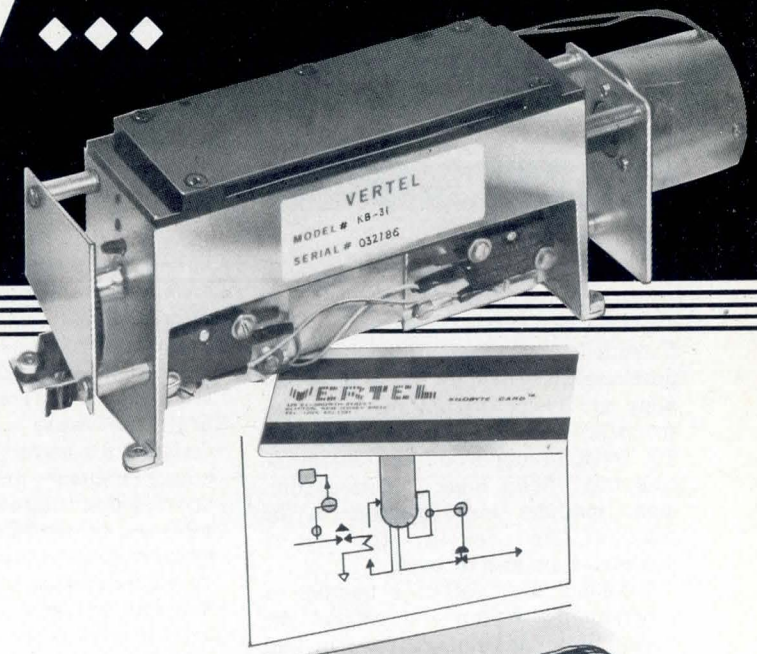

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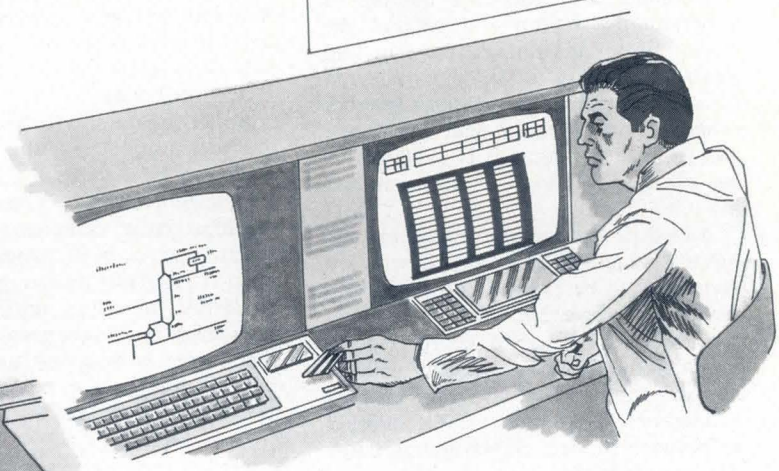

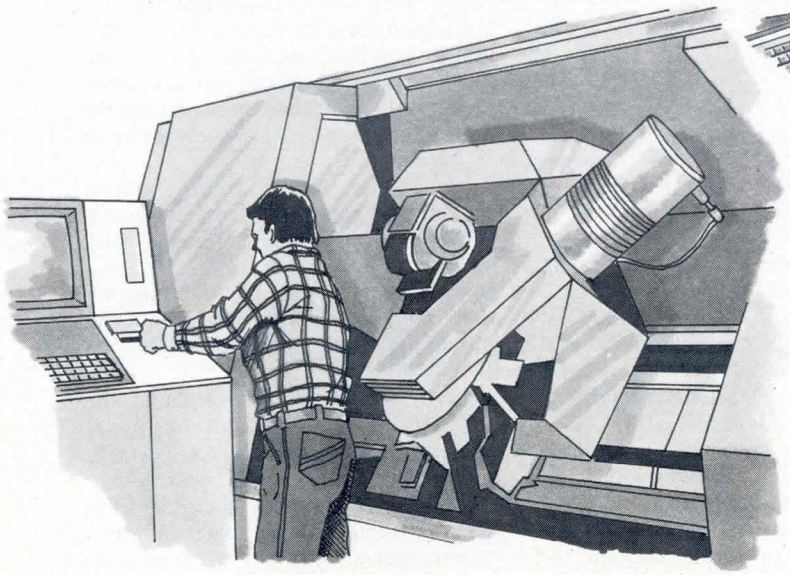

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SOFTWARE

TI-99-4 Support Includes Extended BASIC and Pascal

Extended BASIC, UCSD Pascal, and a development system for Pascal programming are being offered by Texas Instruments Inc, PO Box 53, Lubbock, TX 79408, in support of the TI-99/4 home computer. Solid State Software command modules and reductions in the price of the computer and the rf modulator are also offered.

Extended BASIC offers a number of programming features to expand the flexibility, programming efficiency, and general capability of the computer, and to help software authors write a broader range of home enrichment programs. The enhanced language is available to users in a Solid State Software command module.

Added programming displays include ACCEPT AT and DISPLAY AT, allowing information to be entered and read from any part of the screen. The SPRITE statement allows up to 28 objects to be moved around the screen, each with its own direction and speed. Objects can be accelerated, decelerated, and magnified or reduced in size. Subprograms allow the programmer to write true subroutine programs that can have arguments passed to them and can also have their own local variables. An error handling feature allows the programmer to choose the action taken if an error occurs. When Extended BASIC is selected from the menu screen, the computer will automatically load and run a turnkey program from disc. A memory expansion unit adds 32k bytes of RAM to the 16k bytes resident in the computer console.

UCSD Pascal Version IV.0 and a development system for Pascal programming are also offered. The highly structured, efficient programming language is faster, more logical, and more flexible than BASIC, and offers added features in the area of memory management and scheduling services, as well as options for the applications program developer. The language features portable programs—through the use of a P-code compiler, programs developed for the TI-99/4 can be run on other computers, and programs for other computers can be run on the TI-99/4. The P-code system includes an assembler and linker, and offers the ability to run other languages as they become available.

Included in the development system are a modified TI-99/4 console, a Solid State Software command module designed for assembly language debugging, language programs, two disc drives, a disc controller, Pascal compiler software, a modified RS-232 interface peripheral, and a prototype P-code software development peripheral. The UCSD P-system has been combined with 32k bytes of RAM in the prototype unit that will allow software authors to develop Pascal programs.

Solid State Software command modules available for the TI-99/4 use an assembly level Graphics Programming Language (GPL) developed to provide machine code compaction, execution speed, and ease of program development. GPL offers greater capability and flexibility for color, music, sound effects, high resolution graphics, and synthetic speech than the BASIC designed into the computer.

Circle 458 on Inquiry Card

Enhanced PASCAL/M and Option Packages Available For 8086/88 Based Computers

An enhanced version of PASCAL/M and option packages that include a symbolic debugger, 16-digit BCD real type accuracy, and capability to run on 8086/88 based microcomputers are being offered by Sorcim Corp, 1333 Lawrence Expy, Suite 418, Santa Clara, CA 95051. Expanded to accommodate up to 40 dynamically loadable program blocks, or SEGMENTS, PASCAL/M is a complete implementation of Wirth Pascal that meets the ISO draft standard, and is designed to run on Z-80, 8080/85, or 8086/88 based microcomputers using CP/M, CP/M86, or CDOS operating systems. A special version supports execution on CP/M 2.2 using the COMPUPRO 85-88 CPU board.

Runtime debugging of PASCAL/M programs is supported by the PASCAL/M symbolic debugger option. Reference to program defined procedure and variable names can be accomplished without dealing with internal representation. The symbolic debugger allows setting of breakpoints, single stepping of statements, trapping on stores, examining and changing of variables, and tracing of program execution. The 16-digit BCD real type accuracy option is designed for business and scientific applications where 16-digit precision is essential.

Circle 459 on Inquiry Card

CIS COBOL Simplifies Software Integration For OEM Users

Release 4.3, an enhanced OEM version of CIS COBOL, available from Micro Focus, Inc, 1601 Civic Center Dr, Santa Clara, CA 95050, simplifies integration into a new environment and increases program compilation and execution. The ANSI 74 COBOL compiler and runtime system assures OEMs of greater upward compatibility to multiuser operating system environments and of transportability to future equipment.

On certain system configurations, compilation speed is almost doubled, execution speed is also improved compared with earlier release levels. These improvements principally result from revised mechanisms for BCD arithmetic, and an optimized indexed sequential access method.

CIS COBOL, which also includes the ANSI-defined batched debug facility, is available for use on 8080-, 8085-, 8086-, and Z80 based microcomputers, for DEC LSI-11 based computers, and for TI-990 based equipment. It also runs on Apple II computers with CP/M operating systems and in conjunction with the Z80 Softcard, which makes the Z80 instruction set available in addition to the Apple's 6502 microprocessor. An optional screen formatter/program generator that reduces the time needed to develop screen-processing applications is also available.

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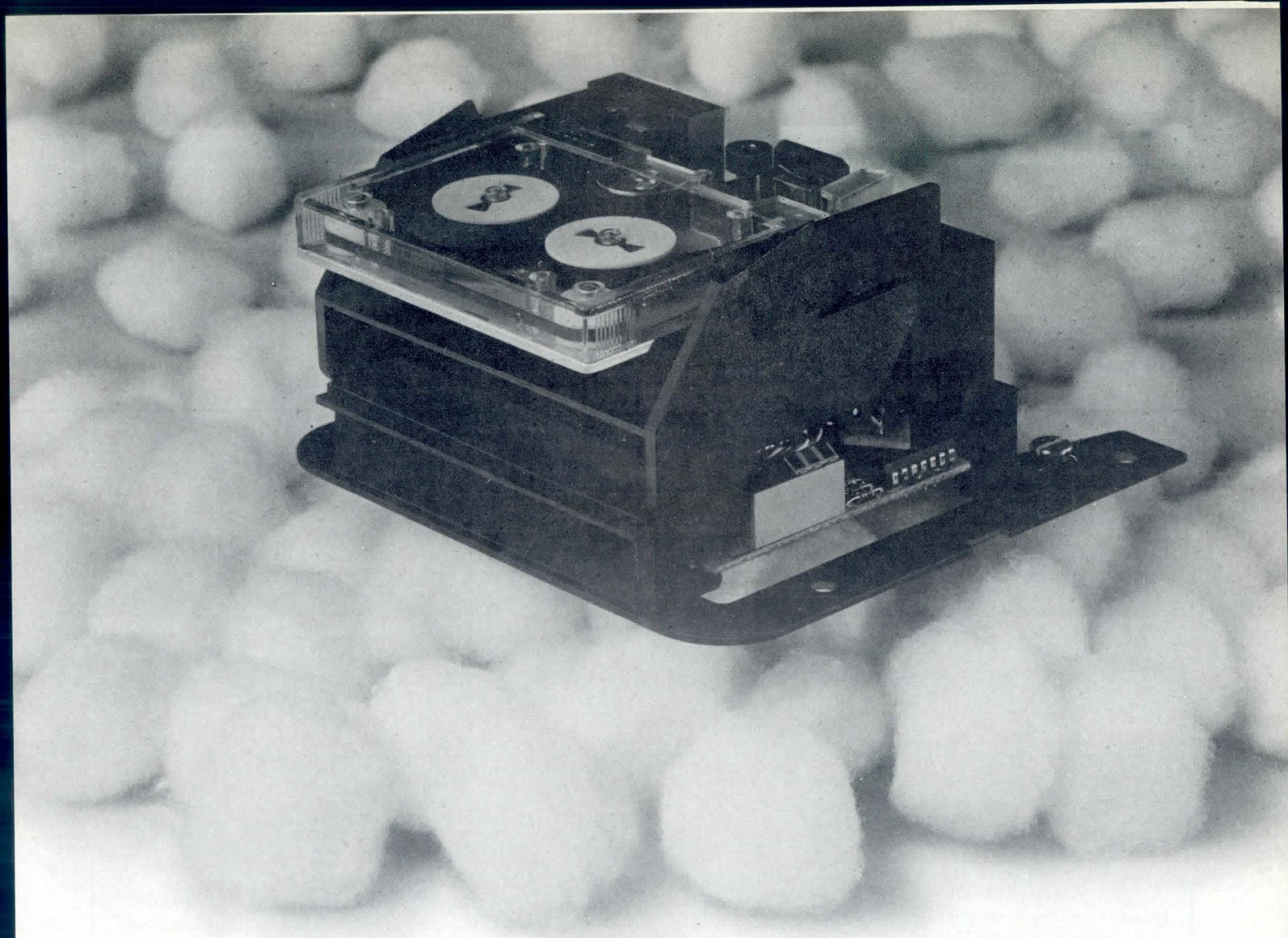

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Circle 88 For Detailed Specifications

Floating Point Microprocessor Implemented as Optional Co-Processor

Richard Lowenthal

Convergent Technologies
2500 Augustine Dr, Santa Clara, CA 95051

Since the advent of microprocessors, designers have yearned for a way to significantly improve the arithmetic power of a system, simply by adding another processor chip. Such an improvement in computational capability can be attained by using the Intel 8087 floating point numeric processor as a co-processor (*Computer Design*, Feb 1981, pp 176-178). Co-processing involves an architectural design in which two execution units use a common instruction stream. Each processor looks at the instructions being fetched to determine whether the instruction is to be executed by it or the other processor.

An 8087 is available as an option on Convergent Technologies's family of information processors. The technique of co-processing is used to operate the processors in tandem. The 8087 and 8086 operate like a single processor, but have an extended instruction and register set and the ability to execute instructions simultaneously.

To program the two processors, the object code contains operation codes (opcodes) that are recognized by one processor and ignored by the other. Thus, the object code translator, assembler, or compiler will generate code for the co-processor system just as it would for a single processor.

In systems with multiple processors operating concurrently, the programs running in the different processors occasionally must run synchronously. When a program running in one processor needs a result from a program running in another processor, the processor that needs the result must wait for the other to produce it. Another requirement of co-processing is the extension to exception handling software. Since the processing hardware is split into two units, the resulting implementation of exception, as will be explained, is somewhat different from that of a single processor. A block diagram of a co-processing system, indicating the various control and data signals, is shown in Fig 1.

Co-Processor Programming

Object code for the 8086/8087 is biased toward the 8086, since the 8086 controls the fetching of instructions. 8087 opcodes are called ESCAPE instructions in the 8086 instruction repertoire, indicating that another execution unit is escaped to and the 8086 does not operate on these instructions. ESCAPE instructions (or 8087 opcodes) contain two operands. The first operand of six bits determines the operation to be performed by the 8087, and the second is a source field that indicates a register or memory location. If the source field of the ESCAPE instruction refers to memory, the 8086 reads the indicated memory

(continued on page 180)

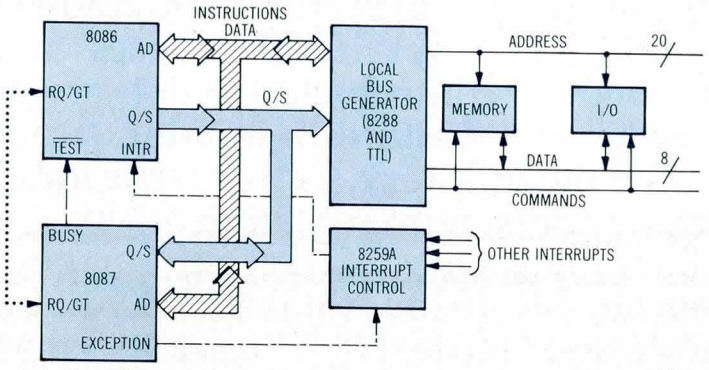

Fig 1 Co-processing system. 8086 and 8087 are operated in tandem. Dependent processes in co-processors are synchronized by signal. Exception signals communicate occurrence of exceptional events, usually errors, to 8086. Arbitration signal controls contention for shared buses. Command/status lines determine current use of instruction/data bus, indicate to 8087 when instructions are on bus, and trigger I/O and memory cycles

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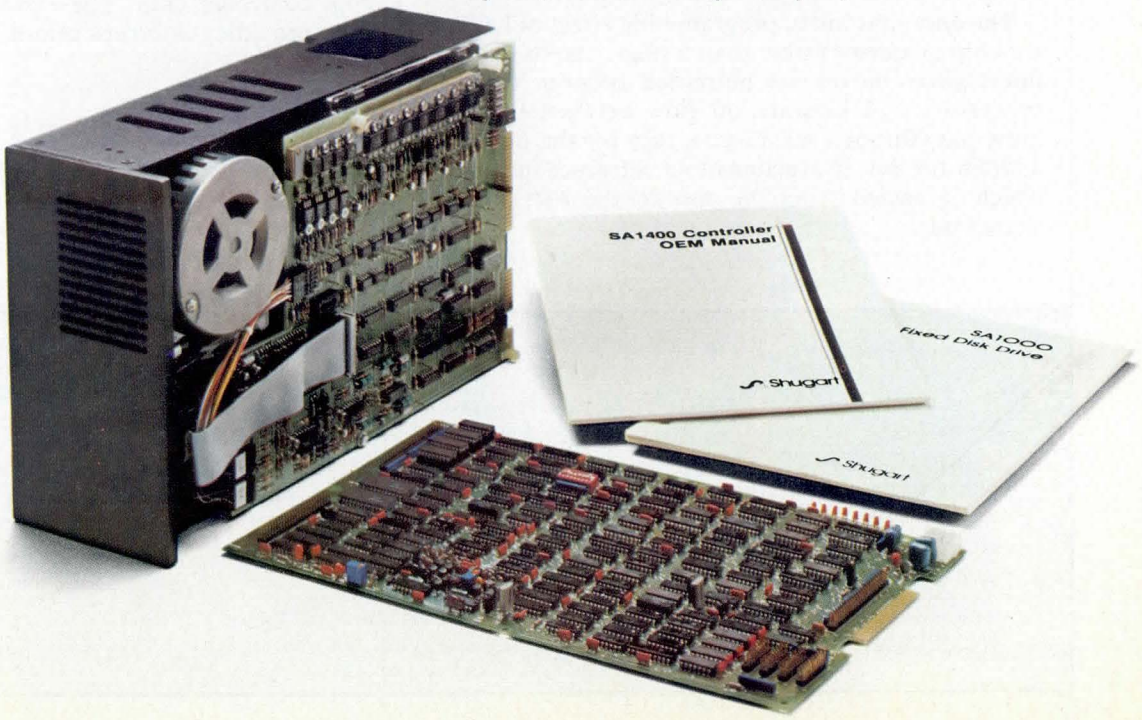

location on behalf of its co-processor and ignores the data. This saves the 8087 from needing an address calculation circuit. While the 8086 drives the operand address on the shared bus, the 8087 simultaneously reads and stores the address. The 8087 can then use the address to write into the memory location, or increment it to get multiword operands.

Once the 2- or 4-byte (depending on the type of source operand) ESCAPE instruction has been fetched, the 8086 continues to fetch and execute instructions in parallel with the 8087's execution of the ESCAPE. The 8087 will at times use the shared processor bus to read and write operands from and to memory without affecting 8086 operation, except in preventing simultaneous bus use. (See "Sample 8086/8087 Instruction Code.")

The 8086 program executes a WAIT instruction when it requires some data from the 8087 to continue, or when another instruction is about to be fetched for the 8087. The WAIT instruction causes the 8086 to stop until the 8087 is idle. If an exception condition occurs during an 8087 operation, the 8087 communicates the event to the CPU (8086) via an interrupt. 8086 software then handles the condition appropriately.

A future release of the company's assembler will "understand" mnemonics, and generate code for the 8087 opcodes (or ESCAPE instructions). Syntactically, the code is similar to 8086 opcodes with names such as FADD for floating point add. The assembler will have a WAIT instruction to implement the synchronizing scheme. It will automatically insert a WAIT instruction before every 8087 instruction (unless explicitly overridden) to ensure that the new ESCAPE instruction will not arrive while the 8087 is running. Also, a future release of the company's FORTRAN compiler will generate object code directly for the 8087.

The only substantial programming effect of having a 2-chip processor rather than a single-chip is that no interregister moves are permitted between the co-processors. All information flow between the two must pass through memory, except for the operand address for 8087 instructions that reference memory, which is passed from the 8086 to the 8087 on the shared bus.

Hardware Implementation

When the 8086 (and 8087) reset pins are pulsed, the 8086 is given control of the shared processor bus, queue status, and bus status lines. After reset, the 8086 immediately begins to fetch and execute instructions. If the 8086 encounters an ESCAPE, it treats it as a no-op, unless it specifies a memory source operand; then it will read the operand. The 8087 simultaneously monitors the instruction queue status lines of the 8086 to determine when instructions are being fetched. When the 8087 sees an ESCAPE instruction on the bus during a fetch cycle, it begins to execute that instruction.

Any time the 8087 needs to use the processor bus to access memory, it pulses the REQUEST/GRANT line to the 8086. As soon as the 8086 recognizes the bus request and has given up the bus, it answers the 8087 by issuing a GRANT pulse on the bidirectional REQUEST/GRANT line. When the 8087 is finished with the bus, it tells the 8086 by issuing a third pulse on the line, called the RELEASE pulse, to return control to the 8086.

The 8087 asserts its BUSY output whenever it is executing an instruction. In this system, BUSY is connected to the TEST input of the 8086. The 8086 instruction WAIT causes the 8086 to stop until the TEST line goes active (TEST is active low, while BUSY is active high). Thus, if WAIT is executed in the 8086 while the 8087 is executing, the 8086 will stop. If the 8087 is not executing (ie, not working on an ESCAPE instruction), the WAIT instruction becomes a no-op.

When an exception condition (such as arithmetic overflow) occurs within the 8087, the interrupt output is asserted. In this system, the interrupt line is connected to the level 4 interrupt input of an 8259A interrupt controller chip. The 8259A then interrupts the 8086, providing interrupt priority, masking, and vectoring.

System Interface

As LSI density has gone up, the interconnect between chips has become a bottleneck. The largest standard

(continued on page 182)

Sample 8086/8087 Instruction Code*

Instruction	Hexadecimal Object Code	Processed By	Effect
FADD ST (2), ST	DCC2	8087	Add stack items within 8087
FST <MEMORY LOCATION>	D996XXXX	8087	Store real value into memory
ADD AX, BX	03C3	8086	Add two registers within 8086
MOV <MEMORY LOCATION>, AX	A3XXXX	8086	Store word into memory
WAIT	9B	8086	Wait for 8087 to become idle

Mnemonics© Intel Corp 1980
XXXX stands for a 16-bit segment offset address
<MEMORY LOCATION> is the name of a data item in program

32 TO 64
Channels...with a Battery

Dolch Logic Instruments' third generation logic analyzer, the LAM 3250, lets you meet your troubleshooting needs now, and expand for the future. The LAM 3250 records up to 32 channels of information at sampling rates to 50 MHz, and with optional Channel Expansion Probes, its capability can be extended to 64 channels. And there's more.

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Since it incorporates dual 16-channel X 1000-bit recording blocks, the LAM 3250 can accept up to two independent external clocks for sampling data, letting you independently monitor both address and data on a multiplexed bus.

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- Sampling rates to 50 MHz
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- Powerful word search feature
- Window triggering
- Real-time trigger tracing
- Non-volatile menu memory
- GPIB and RS-232 interfaces standard
- Personality probes and disassemblers for many popular uP's and bus systems (optional)

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Circle 12 for Demonstration Circle 90 for More Information

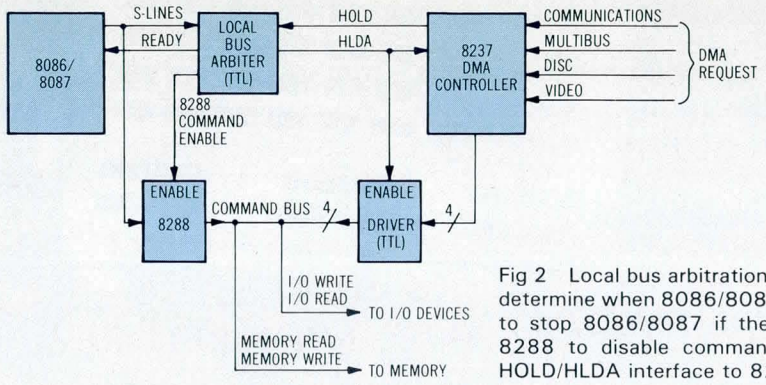


Fig 2 Local bus arbitration. Local bus arbiter uses status lines to determine when 8086/8087 are not using local bus, uses READY to stop 8086/8087 if they need local bus during DMA, uses 8288 to disable commands from 8086/8087, and presents HOLD/HLDA interface to 8237

chip pin count has grown from 14 pins to 40, and some chips use as many as 64 pins. This high pin count uses up printed circuit board space and has caused manufacturing difficulty for integrated circuit and board manufacturers. To help solve the interconnect problem, Intel multiplexes the use of some 8086 and 8087 pins; ie, it uses them for a variety of operations. Multiplexing pins facilitates the interconnection of LSI chips. Also developed have been I/O and small memory chips that connect to multiplexed buses. Almost all chips and circuits, however, require signals that have a single function.

In this system, a nonmultiplexed, local bus and applications bus (Multibus) are required. The multiplexed 8086/8087 bus, therefore, must be converted to the nonmultiplexed buses. To create the local bus (from which the Multibus interface generates the applications bus), the local bus generator contains a demultiplexing latch that is controlled so that it latches address information from the multiplexed bus at the beginning of each bus cycle. The local bus interface also provides electrical buffering during the data portion of each cycle to connect the local and multiplexed buses during that time.

The 8086 and 8087 save pins by encoding bus command information on a set of status lines (S-lines). The S-lines are decoded in the local bus generator to form individual command lines such as I/O read (IOR) and memory write (MEMW) for the peripherals and memory. This logic is completely shared by the 8086 and 8087. Although the two LSI chips communicate with each other over the multiplexed bus and the encoded status line, they share the same local bus interface logic, including the LSI 8288 bus controller chip. The addition of the 8087 to an 8086-only system requires no additional logic to the local bus interface. Contention for use of the local bus interface is handled by the REQUEST/GRANT technique already described.

The READY signal, common to the 8086 and 8087, is used to signal when an I/O or memory cycle is completed. This signal is connected directly to both chips. The chip that has been "granted" the bus and is asserting the common S-lines looks at READY to end a bus cycle.

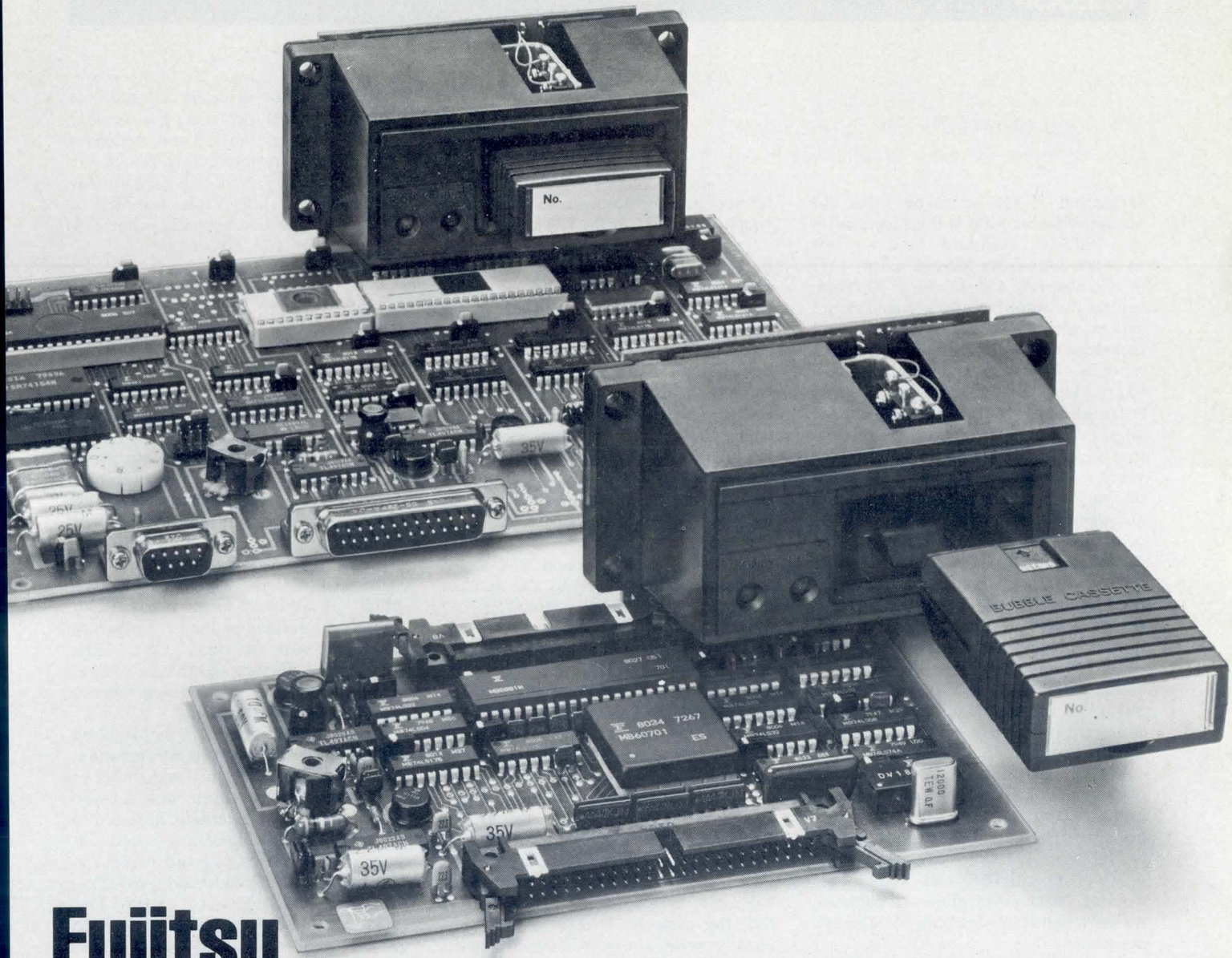
Arbitration with Other Local Bus Masters

When used with a co-processor such as the 8087, the 8086 has no direct memory access (DMA) handshake signals. In the "minimum mode," which prohibits co-processing, the 8086 has DMA HOLD and HOLD ACKNOWLEDGE signals. The computer uses the READY signal for local bus arbitration. (See Fig 2.) Each bus master, except the 8086/8087, requests the DMA controller for the local bus. In turn, the 8237 DMA controller chip requests access to the bus from the arbiter. The arbiter uses the 8086/8087 S-lines to determine when the processors are not using the bus, eg, during internal cycles or between cycles. When the arbiter grants hold acknowledge (HLDA), it disables the 8288 processor command decoder and drops the READY signal to the processors. This local bus arbiter needs no special logic to handle the 8087, as the S-lines and READY are connected in parallel to both processors, and have the same effect in both.

Exception conditions of the 8087 are handled by asserting an interrupt output. This signal is compatible with the 8086's interrupt LSI chip, the 8259A. Although it can be connected to any 8259A input directly, in this system it is ORed into and shares an interrupt level with other components of the system.

Summary

Optional hardware in a system usually requires a number of compromises necessitated by maintaining two sets of software and by providing for hardware. The co-processor concept, as designed by Intel and implemented by Convergent Technologies, has avoided most software and hardware compromises. The co-processor option does require an assembler with a few extra instruction types and registers, but these extra instruction types are flagged so that they will not be used in 8086-only systems. Also, co-processing requires compilers to generate code including the new 8087 instructions. For hardware, the only price paid for the co-processor option is a few extra holes in the CPU board, for the 8087, and an OR gate input for the interrupt line.



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CIRCLE 91 ON INQUIRY CARD

16k Compatible 16-Pin 64k Dynamic RAM Uses Dynamic Circuitry to Minimize Power Dissipation

Organized 65,536 words by 1 bit, the MK4164 dynamic RAM is the successor to the industry standard MK4116. This dynamic RAM from Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006, utilizes the manufacturer's Scaled Poly 5 process technology and advanced circuit techniques to provide wide operating margins, internally and to the system user. Use of dynamic circuitry throughout, including 512 sense amplifiers, ensures that power dissipation is minimized without sacrifice of speed or operating margins. By maintaining 128 cells for each sense amplifier and switching to polysilicon bit lines, the company improved the ratio of cell capacitance to bit line capacitance to 12 to 1. Refresh characteristics maximize production yield while maintaining compatibility between dynamic RAM generations. Access times and cycle times include 120 and 265 ns for the MK4164-12, 150 and 325 ns for the -15, and 200 and 395 ns for the -20. Maximum power consumption is 300 mW active and 22 mW standby.

Multiplexed address inputs permit packaging in a standard 16-pin DIP with only 15 pins required for basic functionality. The design is compatible with the JEDEC standards for 64k x 1 dynamic RAMs. Compatibility with the MK4516 dynamic RAM (16k) allows a common board design to service both 16k and 64k designs.

Output of the RAM can be held valid indefinitely by holding $\overline{CAS}$ active low. A refresh cycle can be performed while holding data valid from a previous cycle. The 16 address bits required to decode 1 of the 65,536 cell locations within the MK4164 are multiplexed onto the 8 address inputs and latched into the onchip address latches by externally applying two negative going TTL-level clocks. Row address strobe ($\overline{RAS}$), the first clock, latches the 8 row addresses into the chip. High to low transition of column address strobe ($\overline{CAS}$), the second clock, subsequently latches the 8 column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events that are controlled by internal clocks with different delays. The two clock chains are linked together logically so that the address multiplexing operation is done outside of the critical timing path for read data access. These later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain.

"Gated $\overline{CAS}$" allows the $\overline{CAS}$ clock to be externally activated as soon as the row address hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from row address to column address information. $\overline{CAS}$ may be activated at any time after t_{RAH} and will have no effect on the worst case data access time (t_{RAC}) up to the point at which the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end points result from the internal gating of $\overline{CAS}$. However, access time is determined by the access time from $\overline{CAS}$ ($t_{\overline{CAS}}$) rather than from $\overline{RAS}$ ($t_{\overline{RAS}}$), and $\overline{RAS}$ access time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

Data to be written into a selected cell are latched into an onchip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The last negative transition made, $\overline{WRITE}$ or $\overline{CAS}$, is the strobe for the data in (D_{IN}) register and permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought active low prior to the point at which $\overline{CAS}$ is brought active low, the D_{IN} is strobed by $\overline{CAS}$, the input data are set up, and hold times are referenced to $\overline{CAS}$. If the input data are not available at $\overline{CAS}$ time (late write), or if it is desired that the cycle be read/write or read/modify/write, the $\overline{WRITE}$ signal should be delayed until after $\overline{CAS}$ has made its negative transition. The normal condition of the data output (D_{out}) of the device is the high impedance (open circuit) state; any time $\overline{CAS}$ is high (inactive), the D_{OUT} pin will float. Once the output data port is active, it will remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state. $\overline{CAS}$ can be left active low indefinitely, to permit either $\overline{RAS}$-only or $\overline{RFSH}$ refresh cycles to occur without invalidating D_{OUT}.

The page mode feature of the RAM allows for successive memory operations at multiple column locations within the same row address. The page mode boundary of the RAM is limited to the 256 column locations determined by all combinations of the 8 column address bits. Operations within the page boundary need not be sequentially addressed, and any combination of read, write, and read/modify/write cycles is permitted within the page mode operation.

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2-ms interval. Although any normal memory cycle will perform the required refreshing, this function is easily accomplished by using either $\overline{RAS}$-only or $\overline{RFSH}$ type refreshing.

Circle 441 on Inquiry Card

Improved Performance And Reliability Claimed for 12-Bit ADC

A recently announced 12-bit successive approximation analog to digital converter (ADC) is designed to replace the ADC581, ADC85/84, and ADC-HX12B/HZ12B. Claimed to offer superior performance, the ADC85, from Hybrid Systems Corp, Bedford Research Pk, Bedford, MA 91730, is designed with a monolithic 12-bit DAC, instead of the multiple chips used in conventional ADCs. The monolithic structure and the use of laser trimmed thin film resistors contribute to the device's high reliability.

Conversion speeds of 10 μs for 12-bit operation, and 8 μs for 10-bit operation, allow use of the ADC85 in a wide range of applications. Short cycle and internal clock rate may be externally adjusted to provide faster conversion speeds at lower resolutions. Gain and offset can be externally trimmed to zero, providing full-scale accuracy of $\pm 0.012\%$, $\pm \frac{1}{2}$ LSB. Data are obtainable in both parallel and serial form with the corresponding clock and status signals. Digital input and output signals are DTL/TTL compatible.

Equipped with an internal clock and a reference and input buffer amplifier, the device can be used with an external clock for synchronization. External clocking is accomplished via a negative going pulse, 100 to 200 ns wide.

Total power consumed by the ADC is 1.2 W maximum, allowing the device to operate reliably at high temperatures. Input scaling resistors provide for the selection of input ranges of ± 2.5, ± 5, or 0 to 10 V.

Specified over the -55 to 125 °C temperature range, it has a low linearity drift specification of only ± 2 ppm/°C, maximum. All "B" versions of the ADC85 series are fully screened and tested to MIL-STD-883, Class B requirements. The device is packaged in a 32-pin hermetically sealed metal case.

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CIRCLE 92 ON INQUIRY CARD

DMC Provides Control For 16k- or 64k-Dynamic RAMs

The Am2964B dynamic memory controller (DMC) bipolar LSI device provides address multiplexing, refresh address generation, and row address strobe/column address strobe ($\overline{RAS}/\overline{CAS}$) control for memory systems built with 16k- or 64k-dynamic RAMs. It replaces, at higher speed and lower power, high speed Schottky MSI packages now being used. Am2964B is the latest addition to the Am2960 family of dynamic memory support products from Advanced Micro Devices Inc, 901 Thompson Pl, Sunnyvale, CA 94086. Eighteen input latches hold up to 18 bits of address, 8 bits for row address, 8 bits for column address, and 2 higher order address bits for decoding to determine which one of four memory banks is selected. A 3-input, 8-bit MUX selects from one of the two 8-bit address latches or from an internal 8-bit refresh counter, and presents the RAM address at the DMC's output. (See the diagram.)

During a memory cycle, the multiplexer select input (MSEL) selects the row or column address. The $\overline{RAS}$ input ($\overline{RAS/I}$) determines $\overline{RAS}$ timing for the $\overline{RAS}$ output by initiating the decoding of the $\overline{RAS}$ select inputs ($RSEL_i$). A $\overline{CAS}$ buffer is also included onchip to guarantee minimum skew. All critical path timing, address, $\overline{RAS}$, and $\overline{CAS}$ to output, are typically 14 ns. This time is comparable to that achieved by higher power Schottky SSI parts.

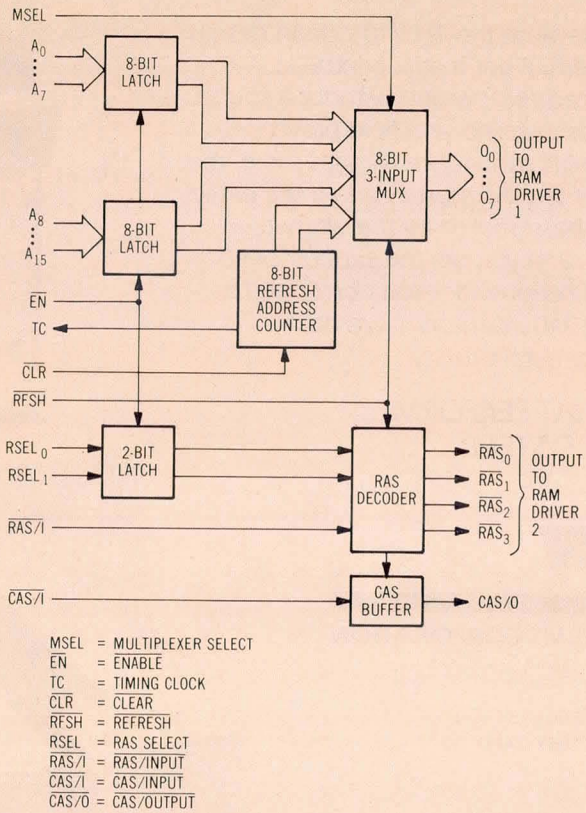
The active low refresh control input refresh ($\overline{RFSH}$) forces the contents of the device refresh counter onto the output of the multiplexer, causes all four $\overline{RAS}$ outputs to go low upon application of $\overline{RAS/I}$, and inhibits the $\overline{CAS}$ output ($\overline{CAS/O}$). The refresh counter automatically advances on the low to high transition of $\overline{RFSH}$ and can be cleared at any time by applying an active low signal to the clear ($\overline{CLR}$) input. The refresh counter also produces a terminal count output ($\overline{TC}$) every 256 counts. For 16k RAMs, when A_{15} is pulled up to 12 V through a 1-kΩ resistor, $\overline{TC}$ will go low every 128 counts. A_{15} acts as an address input for 64k RAMs when addressed with a normal TTL-level input.

Refresh control is external for maximum flexibility. Users can select burst, periodic, or transparent refresh modes. Similarly, $\overline{RAS}$/MSEL/$\overline{CAS}$ timing is external to allow use of any speed 16k or 64k RAM in any system speed environment.

In addition to the address control functions, the DMC includes a special $\overline{RAS}$ decoder and $\overline{CAS}$ buffer. Placing these functions on the same chip is beneficial. Skew in t_{PD} is virtually eliminated, at 25 °C, over the temperature range, and with power supply variations. In maximum performance applications, access time can be improved by as much as 20 ns.

The special $\overline{RAS}$ decoder is a simple 2- to 4-line decoder during normal memory operation. But, during refresh ($\overline{RFSH}$ = low), the refresh counter outputs the RAM refresh address before all $\overline{RAS}$ outputs go low. The decoder function permits $\overline{RAS}$ decoding to select one of four banks of memory with common address and $\overline{CAS}$ busing.

Circle 443 on Inquiry Card



Dynamic memory controller. From Advanced Micro Devices Inc, eighteen input latches hold direct memory address in two 8-bit bytes plus 2 bits for memory expansion by RAS decoding. Three input, high speed MUX selects address output from 1 of 2 8-bit address latches or from 8-bit refresh counter

Operational Amplifiers Combine Bipolar and FET Characteristics

Two low cost, precision BI-FET operational amplifiers have been announced by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. Invented by the company, the BI-FET process combines bipolar and field effect transistors on the same chip, offering the low input bias and offset characteristics of FETs and the high performance of bipolar transistors. The LF411 and the LF412 are the first of a new company series of plastic packaged devices that offer low input offset voltage and guaranteed offset drift. These amplifiers are intended for use in high speed integrators, fast digital to

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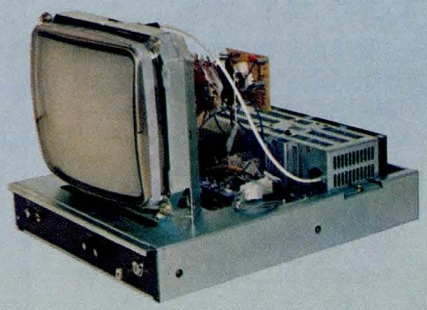

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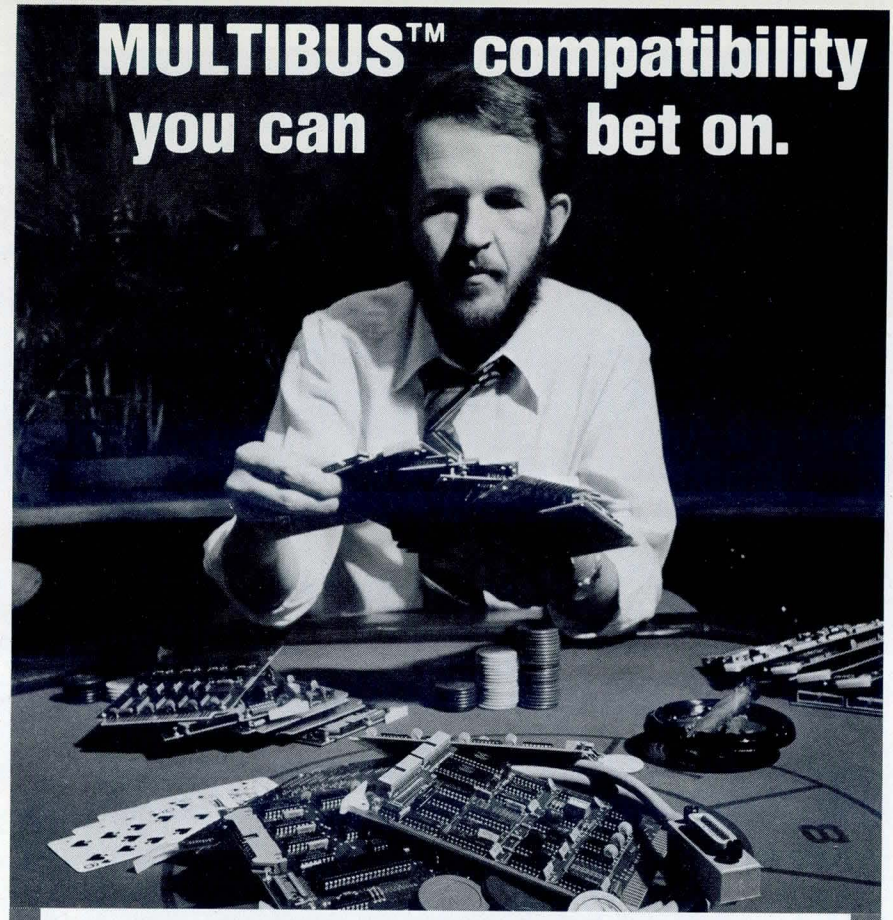
CIRCLE 93 ON INQUIRY CARD



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Both devices require a low supply current, yet maintain large gain bandwidth and fast slew rate. In addition, matched, high voltage JFET input devices provide low input bias and offset currents. The LF411 is pin compatible with the LM741. The LF412 is a dual op amp and is pin compatible with the LM1458.

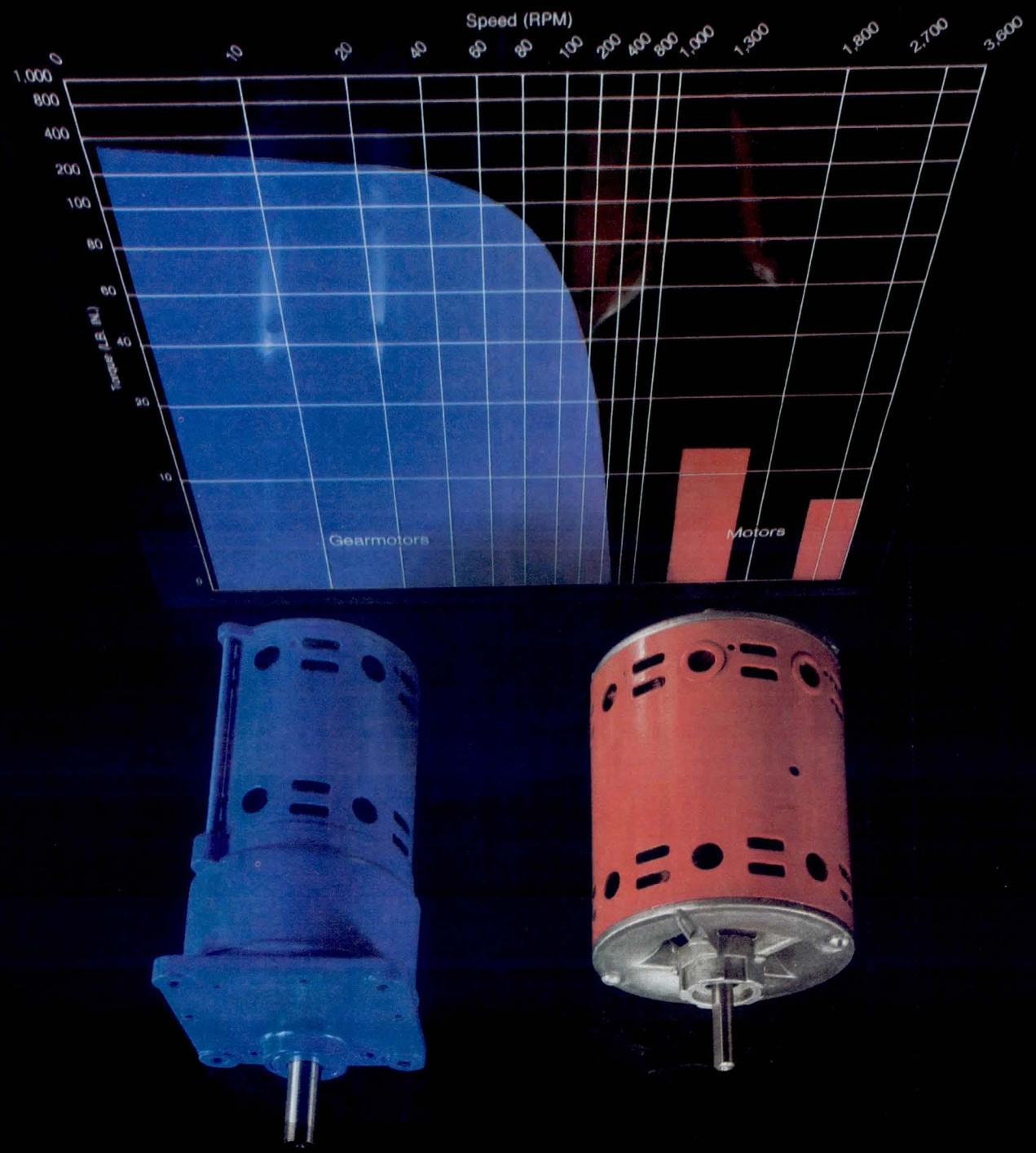
LF411A has an internally trimmed offset voltage of 0.5 mV (max), and the LF412A has an internally trimmed offset voltage of 1 mV (max). Both have input offset voltage drifts of 10 μV/°C (max), wide gain bandwidths of 3 MHz (min), and high slew rates of 10 V/μs (min). The devices are available in 8-pin molded dual-inline plastic and 8-lead TO-5 metal can packages for use in the commercial temperature range of 0 to 70 °C, and the military temperature range of −55 to 125 °C.

Asynchronous Communications Element Combines UART and Baud Rate Functions

The WD8250 asynchronous communications element (ACE), from Western Digital Corp, 3128 Red Hill Ave, Newport Beach, CA 92663, combines UART and baud rate generator functions in a single 40-pin ceramic or plastic package. Claimed to be the first programmable LSI device to successfully combine these features over a usable temperature range, the ACE performs serial to parallel conversion on data characters received from a peripheral device and parallel to serial conversion on characters received for the CPU.

The 5-V serial I/O interface device is programmed by the system software through a 3-state, 8-bit bidirectional data bus. Equipped with an independent receiver clock input, fully programmable serial interface characteristics, false start bit detector, line break generation and detection, and fully prioritized interrupt system controls, the ACE can be interfaced with microprocessors, including the Z80, 8080A, and 6800. Providing improved reliability and reduced board space, the ACE is available with a 0 to 70 °C operating range and is multiple-sourced.

Circle 444 on Inquiry Card



Drive at the right speed

If your speed-torque need falls within the blue or red areas of the chart, Robbins & Myers can get you the gearmotors or speed reducers, motors, and controls to give you the exact output that's right for your application. No compromise. Request Catalog D-1120 for full details on: **Gearmotors.** Comprehensive line of face and foot mounted spur gearmotors rated to 1/6 HP. **Speed reducers.** Three basic spur gearheads with 226 standard ratios from 3.5:1 to 2544:1, with output torques from 16 to 176 in. lb. **A.C. Subfractional HP motors.** Specially sized for OEM needs up to 1/2 HP with millions of standard design variations in diameters from 3 1/8″ to 4 11/16″. **Variable speed control.** SCR controls for DC gearmotors give constant torque performance from near zero to rated rpm. Get expert help! Electric Motor Division, Robbins & Myers, Inc., 1949 Lagonda Ave., Springfield, OH 45501. Tel. 513-327-3329.

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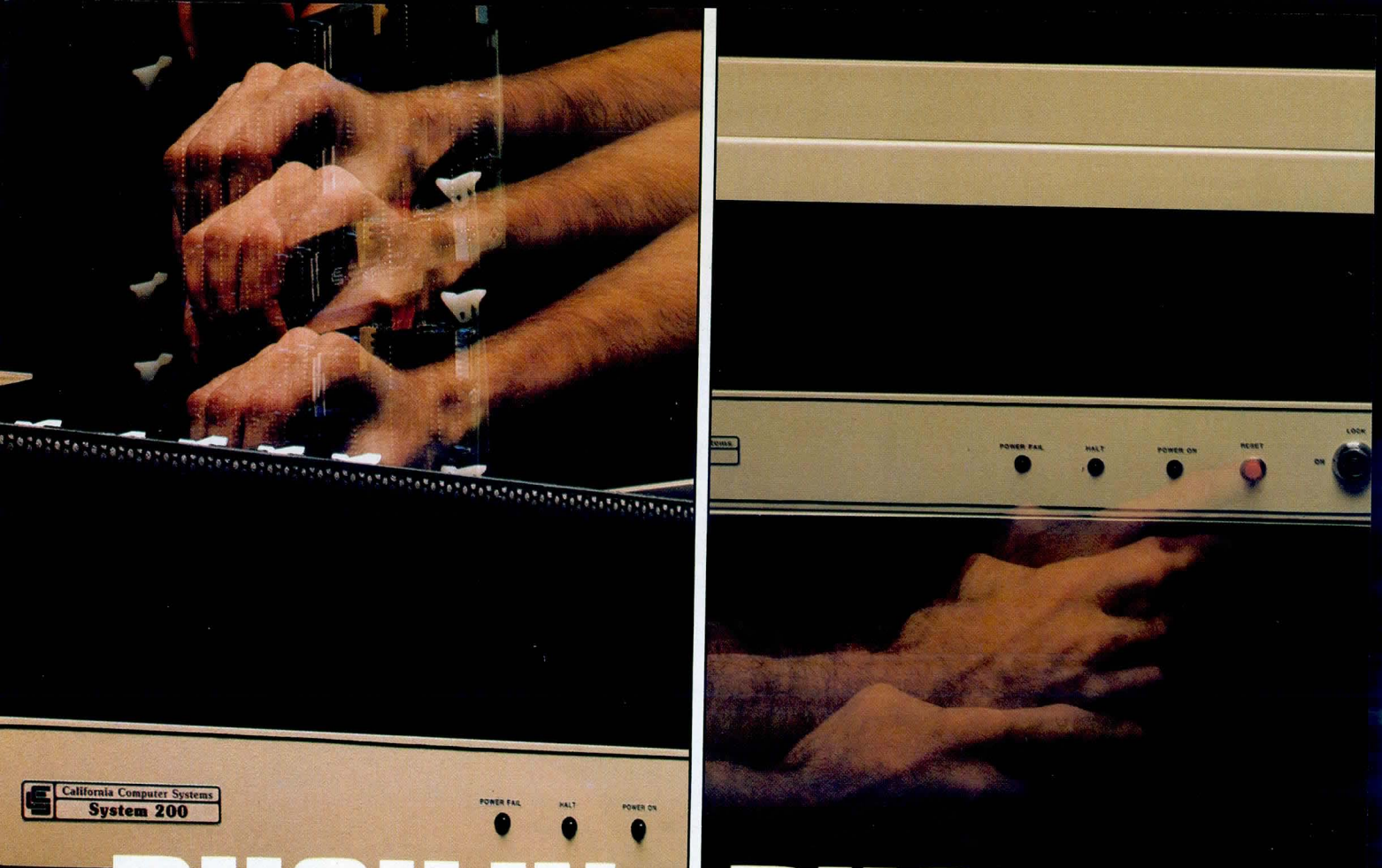
CIRCLE 95 ON INQUIRY CARD



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Here's the CCS line of board-level computers for system builders on the move. **Push in** the CCS board. And **push on** with your application. CCS board-level systems go together easily, come up quickly, and run reliably, with a proven return rate of less than 1%.

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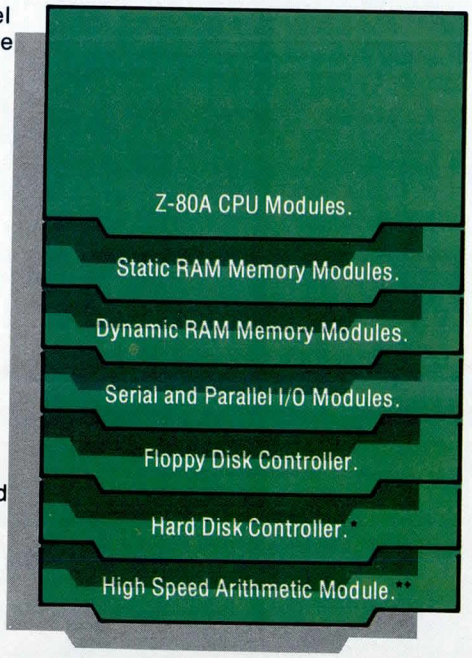

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CIRCLE 96 ON INQUIRY CARD

VLSI Static RAM Combines 50-ns Access With Low Power Consumption

A high speed/low power 16k static RAM with maximum address access and cycle times of 50 ns and 660-mW power dissipation has been introduced by INMOS Corp, PO Box 16000, Colorado Springs, CO 80935. Designated IMS1400, the RAM is manufactured with minimum channel lengths of 2.7 μm, gate oxide thickness of 500 Å, and one layer of polysilicon.

Innovative circuit design techniques allow devices to be produced at a reasonable cost without heavy dependence on device scaling and process complexity. Conservative transistor channel lengths avoid the threshold variation, punch-through, and subthreshold current problems common to very short channel transistors. The device is fabricated by an advanced local oxidation, single-polysilicon N-channel process. Direct wafer stepping is used for all critical photolithography operations. Threshold adjustment, resistor value control, and doping of source/drain junctions are accomplished through ion implantation. Plasma etching is used extensively throughout, especially where dimensional control is critical.

Simplified circuit design allows the device to achieve typical address time of 35 ns while dissipating 375 mW (typ) of active power. Unlike conventional static RAMs, the active power of the device is reduced significantly at high temperatures. This reduction in active power consumed results from the elimination of zero threshold transistors from the circuit design.

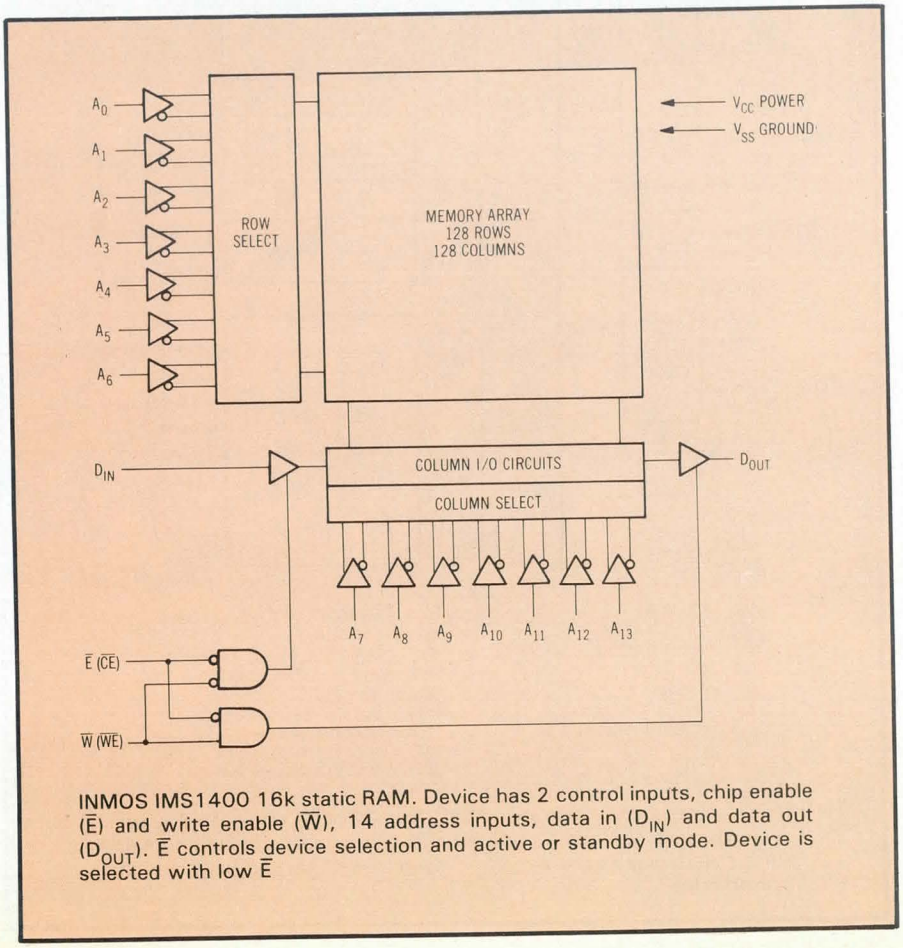
Housed in a standard 20-pin, 300-mil (8-mm) package, the RAM requires a single, 5-V power supply, and uses an onchip bias generator to supply a negative voltage to the substrate. All inputs and the output have direct TTL compatibility. The memory has equal address access and cycle times. A chip enable ($\overline{E}$) pin is provided which, when taken high, automatically puts the chip in a low power standby mode. The access time from chip enable is 55 ns. Further performance improvements are planned for the device. A 40-ns maximum address time version should soon be available.

When V_{CC} is first applied, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode, regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2 ms, the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the 14 address inputs are decoded to select 1 memory cell out of 16,384. Read and write operations on the memory cell are controlled by the $\overline{W}$ input. With $\overline{E}$ high, the device is deselected and the output is disabled.

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the RAM. Impedance in the decoupling path—from the power pin through the decoupling capacitor—to the ground pin must be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Circle 445 on Inquiry Card



INMOS IMS1400 16k static RAM. Device has 2 control inputs, chip enable ($\overline{E}$) and write enable ($\overline{W}$), 14 address inputs, data in (D_{IN}) and data out (D_{OUT}). $\overline{E}$ controls device selection and active or standby mode. Device is selected with low $\overline{E}$

Programmable Disc Controller Chip Interfaces with 8- or 16-bit Microprocessors

Suitable for word processing equipment, the recently released TMS9909 floppy disc controller (FDC) chip, from Texas Instruments Inc, PO Box 25012, Dallas, TX 75265, can control floppy drives while interfacing with any popular 8- or 16-bit microprocessors, and can read from and write onto partial sectors, unlike other FDC chips. The chip can also read from or write onto single- or multiple-sectors of both hard- and soft sectored discs, and simultaneously control two different types of discs, 5.25″ (13.3-cm) mini and standard 8″ (20-cm) drives.

Onchip flux density compensation maintains spacing between flux transitions when writing data onto a disc's inner tracks. Cyclic redundancy checking generation and verification are used to

detect errors. Programmable data transfer rates of 125-, 250-, and 500k bytes/s are accomplished with one frequency determining crystal.

The FDC is compatible with principal floppy data recording formats such as IBM single-density, for recording at 128 bytes/sector (as used in the 3740); IBM double-density, for recording at 356 bytes/sector (as used in System 34); and TI maximum density for recording at 288 bytes/sector (as used in the 990/9900 series of minis and 16-bit peripherals). Capable of supporting up to four double-sided, standard or mini drives, the FDC also supports popular floppy frequency modulation data encoding schemes such as FM for single-density recording, modified FM (MFM) for double-density and modified, and modified, modified FM (M²FM) for very high densities.

To aid in reducing overall systems chip counts, the TMS9909 offers onchip clock generation logic with one 6-MHz external crystal, regardless of the programmed data rate. For the most efficient and flexible interface possible, the FDC also has a memory mapped microprocessor interface that supports an external DMA interface. As a result, the FDC allows a designer to build one interface for all floppy disc formats.

With a direct memory access controller chip, file management programming or logic, and with either an analog or digital data separator (of the user's choosing), the FDC forms an autonomous microsystem. In effect, this combination extends a microprocessor's instruction set to include what are in essence macro level commands. These macros can control virtually any set of floppy disc drives that might be appropriate for a high end microprocessor based system.

Circle 446 on Inquiry Card

Fully Programmable Small System CRT Controller Includes Dual-Row Buffers

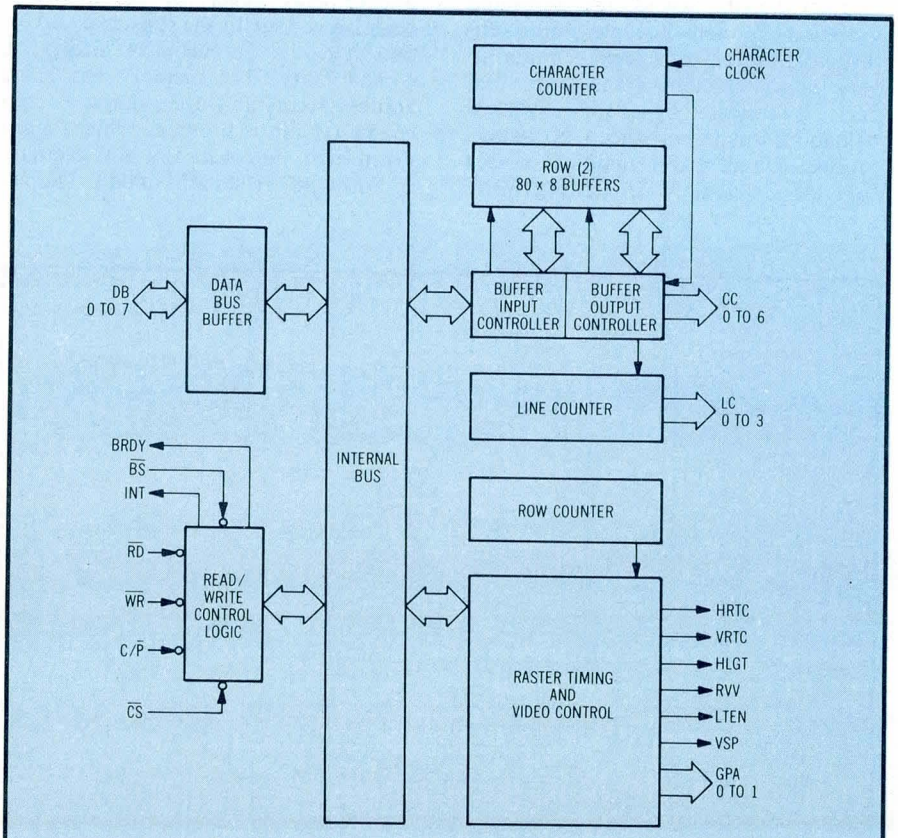
Intended for low cost, small system applications, the 8276 CRT controller, from Intel Corp, 2625 Walsh Ave, Santa Clara, CA 95051, has many of the features found in more sophisticated controllers including dual-row buffers, onchip attribute generation, and fully programmable screen and character formats. The device reduces the number of integrated circuits usually required for a CRT display subsystem from more than 100 to less than 20. When implemented with the company's 8051 single-chip microcontroller, the parts count can be reduced to about 10 chips.

Unlike many other CRT controllers, the device does not require the dedication of high performance memory to screen refresh. Instead, the buffer architecture allows existing system memory to hold all screen refresh data.

Display characters are retrieved from system memory and displayed on a row by row basis. The onchip dual buffer allows the next row of characters to be filling one buffer while the other is being used to display the previous row. This scheme provides rapid shifting of data from memory to the screen, and frees the system bus for screen editing, keyboard scanning, serial data handling, and other local terminal functions to be handled by the CPU.

The number of characters per row (up to 80) and the number of rows per frame (up to 64) are programmable. In addition, the number of lines per character row, the underline position, top and bottom line blanking, and cursor location and format are also user programmable. This capability permits users to design a large variety of screen and character formats.

Circle 447 on Inquiry Card



Small system CRT controller chip. Intel 8276 is designed for CRT systems, such as "dumb" terminals. Dual-row buffer architecture ensures that data are transferred from system memory to display circuitry at high rates

Valedictorian of the Smart Editing Class of Terminals.

Compare the new VISUAL 400 with the other smart terminals. Then compare it to your own specification. And if that doesn't do it, we have "Room for RAM" for custom modifications in large quantities.

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FEATURE COMPARISON CHART

FEATURE	Visual 400	Lear Seigler ADM-42	Perkin Elmer 1251	ADDS Regent 60	Hazeltine Executive 80, Model 30	Beehive DM30
ANSI X3.64 Specified	STD	**NO**	**NO**	**NO**	STD	**NO**
Set-up Modes Eliminate External Switches	STD	**NO**	STD	**NO**	**NO**	**NO**
Typomatic Solid State Keyboard	STD	**NO**	**NO**	**NO**	STD	**NO**
Detached Keyboard	STD	STD	**OPT**	**NO**	STD	STD
CRT Saver	STD	**NO**	**NO**	**NO**	**NO**	**NO**
Block or Underline Cursor	STD	**NO**	STD	STD	STD	**NO**
80 and 132 Columns	STD	**NO**	**NO**	**NO**	**OPT**	**NO**
Double Size Characters	STD	**NO**	**NO**	**NO**	**OPT**	**NO**
Smooth Scrolling	STD	**NO**	**NO**	**NO**	**OPT**	**NO**
Horizontal Split Screen	STD	**NO**	**NO**	**NO**	STD	**NO**
Video Attributes Require No Display Space	STD	**NO**	**NO**	**NO**	STD	STD
8 Area Qualifications	STD	**NO**	**NO**	**NO**	**NO**	**NO**
8 Resident Nat'l Char. Sets Including Line Drawing	STD	**NO**	**NO**	**NO**	**NO**	**NO**
Programmable Non-volatile Function Keys	STD	**OPT**	STD	**NO**	**NO**	**NO**
Display of ALL Control Codes	STD	STD	STD	STD	**NO**	STD
Insert Delete Line with Push Up or Down	STD	**NO**	**NO**	**NO**	**NO**	**NO**
Insert Delete Character with Push Right or Left	STD	**NO**	**NO**	**NO**	**NO**	**NO**
Select Editing Extent to Field, Area, Line, Page	STD	**NO**	**NO**	**NO**	**NO**	**NO**
20 mA Current Loop	STD	STD	**OPT**	**OPT**	**OPT**	STD
Programmable Message Framing (non-volatile)	STD	**NO**	STD	**NO**	**NO**	**NO**
Programmable Answerback	STD	**NO**	STD	**NO**	**NO**	**NO**
Baud Rates to 19200 BPS	STD	**NO**	**NO**	**NO**	STD	STD
Independent Xmit/Receive Rates	STD	**NO**	**NO**	**NO**	**NO**	**NO**
Printer Port Independent of Communication Interface	**OPT**	**OPT**	STD	STD	**OPT**	STD
Paging	**OPT**	STD	**NO**	**NO**	STD	STD

VISUAL 400

VISUAL See for yourself

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CIRCLE 97 ON INQUIRY CARD

5½-Digit Resolution ±0.2-ppm/°C Drift Attained by Monolithic ADC

A recently announced monolithic CMOS integrating analog to digital converter (ADC) offers 4½ or 5½ digits of resolution. Available from Analog Devices Semiconductor, 804 Woburn St, Wilmington, MA 01887, the ADC features relative accuracy of ±1 count maximum in 20,000 for 4½-digit operation, and ±10 counts maximum in 200,000 counts for 5½-digit operation.

Device capabilities include a low scale factor drift of ±0.2 ppm/°C, low power dissipation of 50 mW maximum, automatic calibration capability, and multiplexed BCD outputs for displays. A serial count output is provided for use with rate multipliers for linearization, with BCD or binary counters for data reformatting, or with microprocessors for data manipulation. Applications for the device include high resolution, high stability digital voltmeters and weighting scales, process monitoring, remote serial transmission, and data acquisition.

Operation at either 4½- or 5½-digit resolution is pin selectable. Conversion times are 610 and 1760 ms maximum for 4½- and 5½-digit operation, respectively. The ADC requires a single positive reference voltage and operates with a 5-V supply. It can free-run, continuously converting and updating displays, or operate under computer or microprocessor direction.

Circle 448 on Inquiry Card

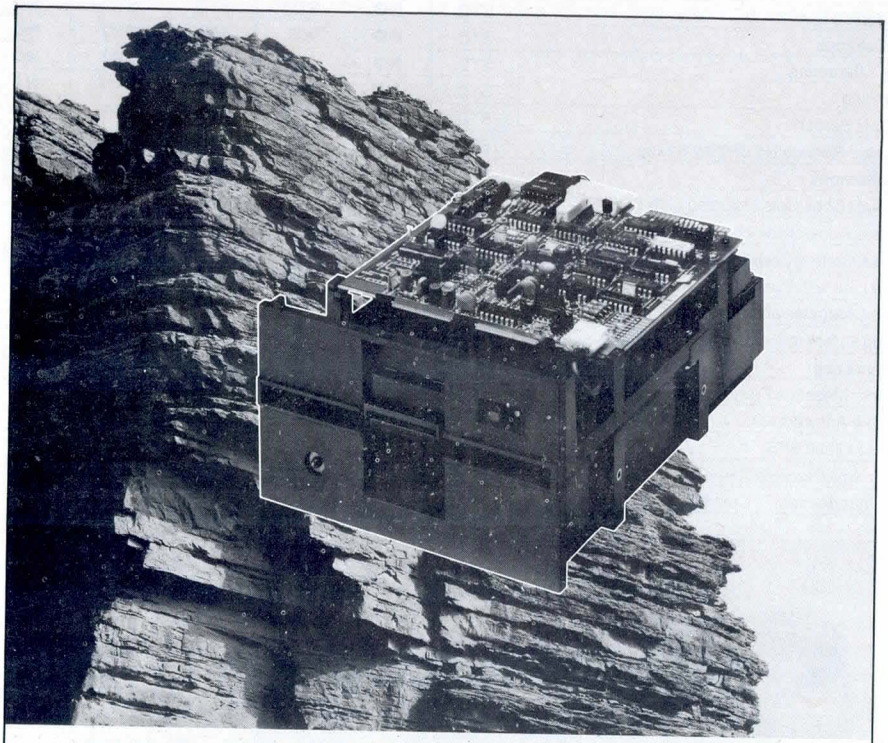
Video Speed DACs Designed for Low Cost Signal Processing

Designed for use in low cost digital signal processing systems, a recently announced monolithic DAC is fabricated with ECL technology and features complementary current outputs and highly stable, onchip voltage references. Peripheral parts are reduced to one current setting resistor and two power supply decoupling capacitors. Designated SP9768, the 8-bit DAC performs at video speed of 5 ns.

With all input bits TRUE, the DAC from Plessey Semiconductors, 1641 Kaiser Ave, Irvine, CA 92714, is capable of driving 20 mA into a 50-Ω load. Desired full-scale current is established by the external resistor selection. Differential nonlinearity is specified at better than 0.2%, and voltage reference stability is better than 30 ppm/°C.

In order to balance its internal currents, provide linear operation over the −55 to 125 °C temperature range, and automatically cancel output glitches, the device operates with a multiple-current source technique, devised by the company. In the balance of currents design, two arrays of four bits each contribute to the analog output signal. Each array's most significant bit is represented by

(continued on page 196)



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Unique DC Spindle Drives feature our continuously-running brushless DC motor whose typical life expectancy is over 10,000 hours. Rock-stable, no electrical noise will interfere with the integrity of your data.

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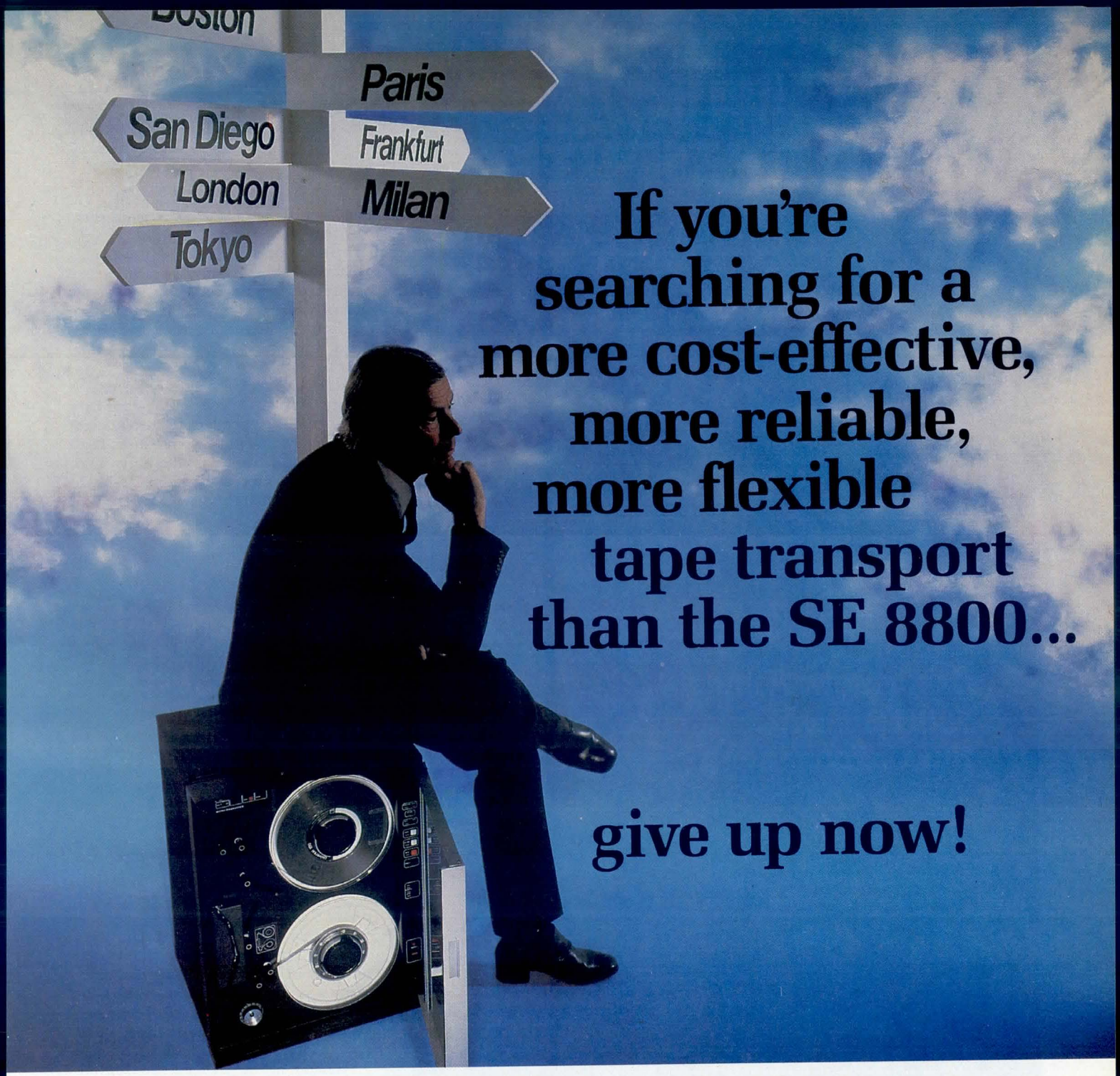
(213) 726-8417



If you're searching for a more cost-effective, more reliable, more flexible tape transport than the SE 8800...

give up now!

You'll have to go a long way to find a buffer arm tape transport to come near the SE 8800 for performance, dependability and user convenience – even further to find a transport with a lower cost of ownership.

SE 8800 is a microprocessor - controlled intelligent tape transport system of totally modular construction with powerful interactive diagnostics. In fact you can install, commission and service the SE 8800 without the use of external equipment.

Interfaces for most mini-computers are available and an integral formatter provides Dual, PE or NRZ options – all at the lowest system costs in the industry.

A flexible reliable unit for OEM's, an easy-to-operate, economical transport for the end user, SE 8800 is the formatted high performance tape transport of the 80's. Follow the sign to SE and find out more about SE 8800 and our unbeatable customer support.

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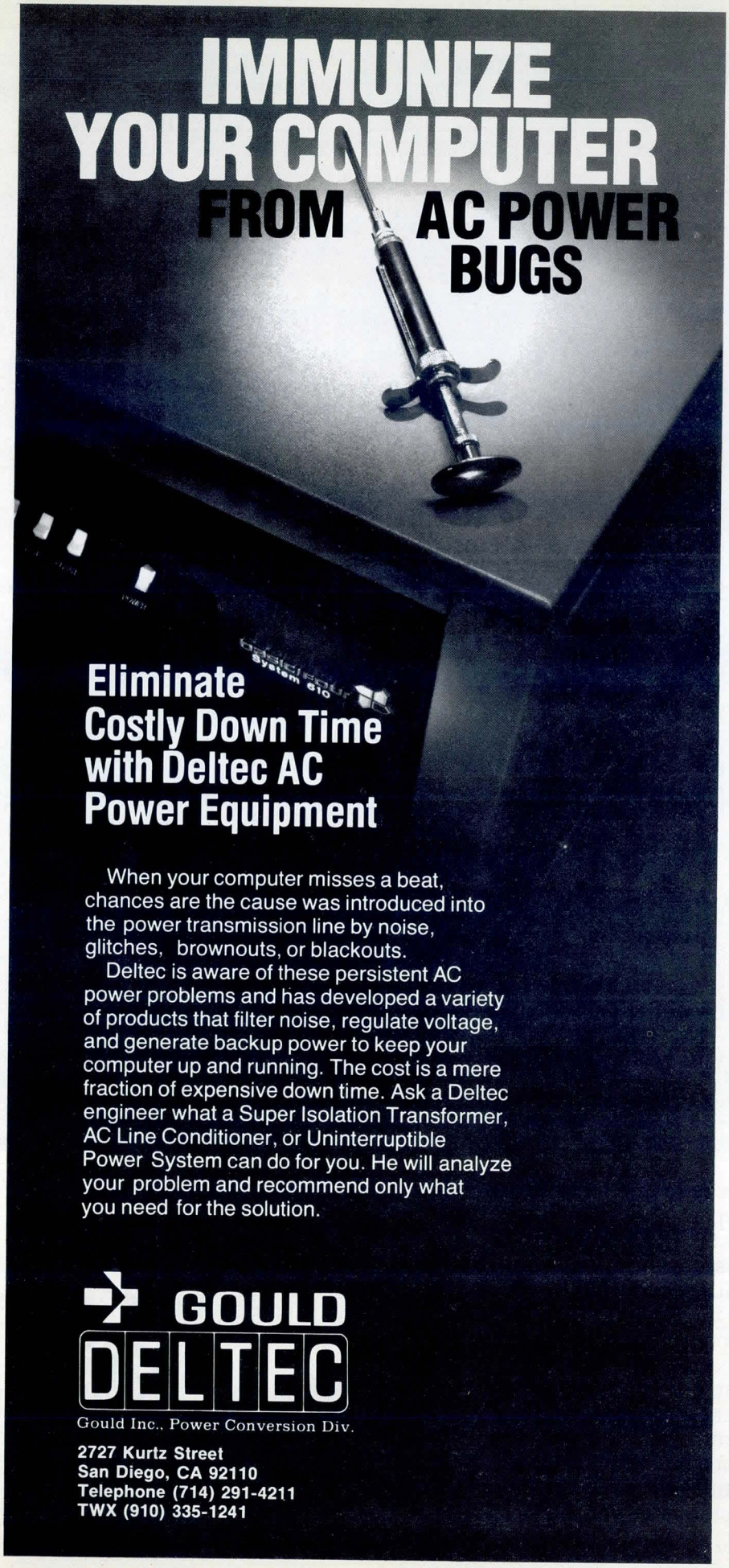

IC LOOP

four currents of equal magnitude. The next most significant bit is represented by two such currents, the next by one, and the fourth by one-half. Transistors that control these output currents are all switched simultaneously, and each switch carries an equal current density. Individual currents from both 4-bit arrays combine to drive the 256-level analog output signal.

Each unit of balanced current is temperature and process stabilized by a resistive divider chain composed of eight 250-Ω equal and matched resistors; three in series and five in parallel to ground. The series parallel combination results in a 16 to 1 current division that combines random process variations so that they cancel each other.

Circle 449 on Inquiry Card

Clock/Display Drivers Designed for Battery Backup Applications

Two COS/MOS clock/display drivers, designed for battery backup applications in microprocessor based systems, can be read by the microprocessor and be displayed using a standard BCD to 7-segment LED decoder driver. M755 is a 24-hour clock and M756 is a 12-hour clock. The circuits also provide a 1-Hz flashing colon output and include a day of the week count section. It is possible to display the content of the data registers instead of the clock section output. The drivers interface with a microprocessor I/O port through a 4-bit bidirectional bus and two strobe signals, which are used to address, load, and read the internal registers and counters.

Assembled in 24-lead dual-inline plastic or ceramic fit seal packages, the drivers, from SGS-Ates Semiconductor Corp, 240 Bear Hill Rd, Waltham, MA 02154, contain the clock logic and a TTL-compatible microprocessor interface. The only external chip normally required is a display segment decoder/driver. Digit multiplexing is performed onchip.

Both devices operate on supply voltages as low as 2 V, with a display-off power consumption of only 75 μW. An input pin is used to switch off the outputs to reduce consumption, and disable the inputs to avoid corruption of the internal registers resulting from spurious data transfers during power-down.

Circle 450 on Inquiry Card

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MIPROC-16AP Associate Processor

The MIPROC-16AP offers super fast preprocessing, postprocessing and I/O handling power for your DEC® PDP-11® computer.

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CIRCLE 101 ON INQUIRY CARD

BRIEFS

450-V NPN Transistor Devices Designed For Electrostatic Printers—With a high 450-V rating and low 500-nA leakage current characteristics, the DN-1006 transistor chip family from Dionics, Inc, 65 Rushmore St, Westbury, NY 11590, is designed for use in hybrid circuits where swings of 400 V or more are required. Claimed to offer the highest available voltages for such devices and utilizing new construction techniques, the transistor chip is extremely rugged and features uniform turn on and fast switching speeds.

The device is suitable for discharge stylii drivers (found in high voltage, high speed electrostatic printers) and in ink jet printer applications. Other applications include inductive load drivers; deflection amplifiers, level shifters, and display drivers. Circuitry of this kind is found in CRT terminal displays, gas discharge displays, ignition systems, and electroluminescent displays. Three devices are offered: the DN-1006 transistor chip, the DTN-1006 in a TO-92 package, and the DQN-1006 in a 14-pin DIP package.

Circle 451 on Inquiry Card

CMOS Manchester Encoder/Decoder Integrated Circuit—A CMOS digital Manchester encoder/decoder has been announced by Harris Semiconductor, PO Box 883, Melbourne, FL 32901. Labeled HD6409, the device is a high speed, low power encoder/decoder with guaranteed performance of one 1M bits/s over the industrial temperature range of −40 to 85 °C. This IC consumes only 12 mA worst case (5 mA typical) of current from a single 5-V (±10%) power supply.

The encoder/decoder allows high speed serial data communication while eliminating dc and low frequency components, and provides clock recovery from the received signal. It also has a high degree of noise immunity and tolerates jitter in the received signal.

Circle 452 on Inquiry Card

ADC Pair Utilizes Quantized Feedback—A 2-chip, 4½-digit analog to digital converter (ADC) set, designated LD122/LD121, offers 1-μV resolution. The pair is suitable for low level signals, such as those from strain gauges, thermocouples, and Hall-effect devices.

Using quantized feedback instead of the more conventional dual slope eliminates the need for an expensive, high quality integrating capacitor. Quantized feedback also simplifies voltage ranging and ensures insensitivity to long-term clock drift. With auto-zero, auto-polarity, and compatibility for differential inputs, the converter, from Siliconix, Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054, provides TTL-compatible multiplexer BCD output for direct BCD to LCD conversion or interfacing to TTL hardware for additional processing.

Circle 453 on Inquiry Card

4096 x 8 ROM Interfaces with All N-Channel Microprocessors—A 4096-word by 8-bit mask programmable ROM with a maximum access time of 350 ns (2332-3) or 450 ns (2332-4), designed for use in bus oriented applications with 8-bit N-channel microprocessors, has been announced by GTE Microcircuits Div, 2000 W 14th St, Tempe, AZ 85281. Dual chip select inputs provide convenient memory expansion allowing up to four 2332 32k ROMs to be OR-tied without external coding.

3-state output buffers allow simple parallel busing for memory expansion. The ROM is TTL-compatible and requires a single 5-V power supply, but does not require external clocks or refresh circuitry. Packaging is standard 24-pin plastic or cerdip.

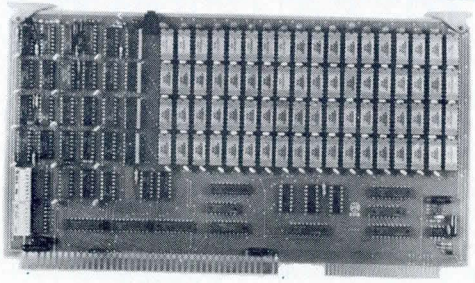
Circle 454 on Inquiry Card

Two Monolithic Dielectrically Isolated CMOS Dual/Quad Analog Switches Introduced—Two analog switches have been introduced by Micro Power Systems, Inc, 3100 Alfred St, Santa Clara, CA 95050: the 100-Ω model MP200DI monolithic dielectrically isolated CMOS dual spst analog switch, and the 125-Ω model MP201DI monolithic dielectrically isolated CMOS quad spst analog switch. These devices are direct replacements for Analog Devices's ADG200/201, Siliconix's DG200/201, and Harris Semiconductors's HI200/201.

Monolithic dielectrically isolated CMOS processing provides advantages of overvoltage protection, total latch free operation, lower power dissipation, 30 mW maximum, and fast switching times. Both switches exhibit low on resistance over the temperature range.

Circle 455 on Inquiry Card

CHRISLIN YEARS AHEAD IN MEMORY DESIGN



WE'VE DONE IT AGAIN — State of the Art Multibus® Memory Design. First to offer up to 512K on one board, and CHRISLIN again brings pricing sanity to the memory market. Why pay over **$2000** for our competitor's 64K x 8 memory board when we will give you the CI-8086 128K x 9 memory for just **$1500** or better yet, the CI-8086 512K x 9 memory module for **$4700.**

Up to 512K bytes in a single option slot. Available in 64K, 96K, 128K, 256K, or 512K configurations. On board parity generator checker, for both 8 bit or 16 bit systems. Off shelf deliveries.

CI-6800-2 — 16KB to 64KB. Plugs directly into Motorola's EXORcisor I or II. Hidden refresh up to 1.5 Mhz. Cycle stealing at 2 Mhz. Addressable in 4K increments with respect to VXA or VUA. On board parity. **64K x 9 $750.00.**

CI-1103 — 16KB to 256KB on a single dual height board. Plus directly into LSI 11/2, H11 or LSI 11/23. Addressable in 2K word increments up to 256KB. **8K x 16 $390.00. 32K x 16 $750.00. 128K x 18 $2880.00.**

CI-S100 — 16KB to 64KB. Transparent hidden refresh. No wait states at 4 Mhz. Compatible with Alpha Micro and all Major 8080, 8085 and Z80 Based S100 Systems. Expandible to 512K bytes thru Bank Selections. **64K x 8 $750.00.**

CI-8080 — 16KB to 64KB on a single board. Plugs directly into MDS 800 and SBC 80/10. Addressable in 4K increments up to 64K. **16KB $390.00. 64KB $750.00.**

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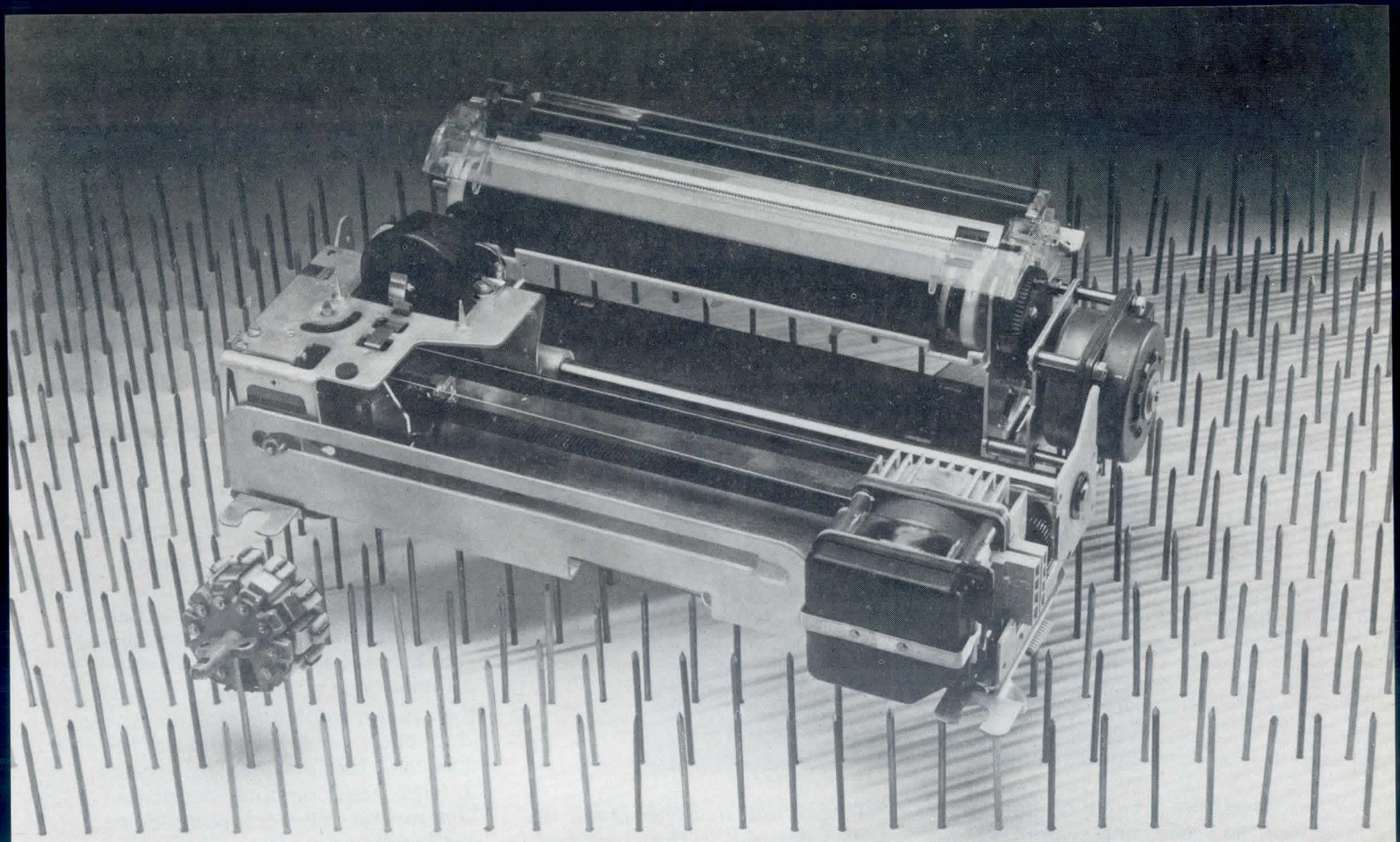
CIRCLE 102 ON INQUIRY CARD



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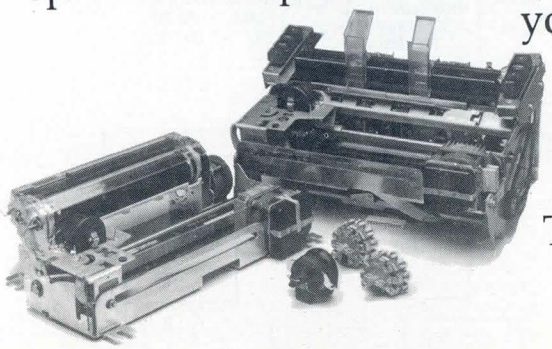
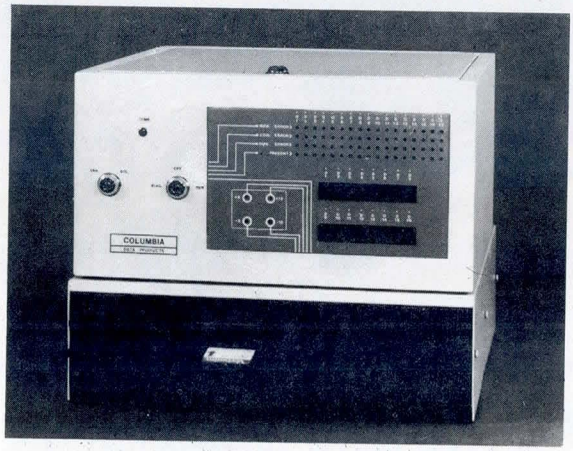


Burroughs OEM Marketing, Burroughs Place, Detroit, MI 48232. (313) 972-8031. In Europe, Langwood House, High Street, Rickmansworth, Hertfordshire, England. Telephone Rickmansworth (09237) 70545.

Burroughs

Circle 103 For Further Information
Circle 104 For Detailed Specifications

Distributed Computing System Provides User Terminals With Dedicated Intelligence



Architecture of the DC 1000 distributed processing system is configured to maximize performance in multiuser environments and to accommodate a wide variety of I/O devices. The system employs a central microcomputer to serve the sole function of resource management for shared peripherals, including communication access to a higher level host. Each of the 1 to 16 user stations has its own dedicated ''satellite'' microcomputer with up to 64k bytes of RAM (see diagram).

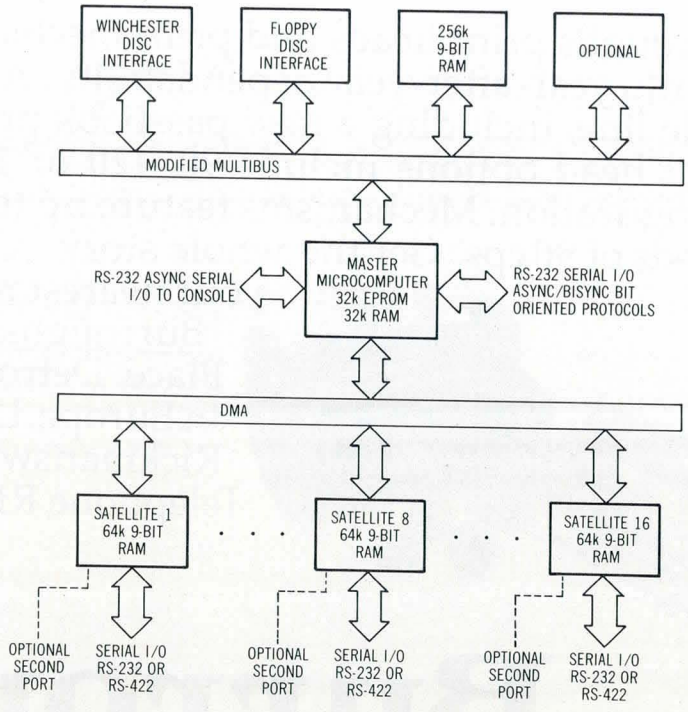
Internal Organization

Contained in a single 17 x 9 x 17" (43 x 22 x 43-cm) enclosure, the system comprises up to 17 4-MHz Z80A based microcomputers linked in a star configuration. One microcomputer is the master and the others act as the dedicated satellites. The master, with up to 64k bytes of memory with parity, services requests for shared resources from each satellite and coordinates communications between them. Typical configurations of the central microcomputer require only 32k bytes of RAM and 32k bytes of EPROM, but it may access up to 256k bytes of RAM with bank switching.

The central microcomputer occupies one slot in the company's version of the Multibus. Slot two is usually reserved for a floppy or hard disc controller, and slots three to five are available for other shared peripherals. Proprietary memory expansion boards as well as floppy and Winchester disc controllers are available for the Multibus, and most available Multibus compatible peripherals can also be used.

The master microcomputer has an RS-232 link for an operator console at the central computer site. Another RS-232/-422 port allows the system to communicate asynchronously or bisynchronously for SDLC/HDLC formats enabling access to large host computer networks. The master microcomputer does not initiate tasks but responds to each satellite user request on an interrupt basis, and provides 200k-byte/s data transfer.

Each satellite microcomputer is an independent fully capable system, with up to 64k RAM, dedicated to its user. A simple



remote terminal communicates with its satellite at 1200, 2400, 4800, or 9600 baud over a dial-up or dedicated telephone link to one or two RS-232 ports on the satellite, and has access to up to 64k bytes of 9-bit dedicated RAM.

System Implementation

Individual users may execute programs without interference from other users under the CP/M* operating system, that also enables access to a broad range of other software. The system can also support MP/M* and CP/NET.* Each user station can develop new programs using the shared resources for mass storage and printout.

Internal diagnostics are activated at power-on, either remotely via the host CPU interface or by the local operator through front-panel switching. Status of both master and satellite microcomputers is displayed by LED indicators. Power requirement is 108 W at 110 to 120 Vac 60 Hz.

Applications

The system provides the designer with an economical alternative to conventional distributed processing systems, especially in office automation applications. System transparency gives the user terminal the appearance of direct interactive communications with a large host without the delays normally associated with time-sharing.

Price and Delivery

Single-unit price for a basic configuration of central microcomputer and four 16k-byte satellites is $6995. Deliveries begin in June 1981. Columbia Data Products, Inc, 8990 Route 108, Columbia, MD 21045.

For additional information circle 199 on Inquiry Card.

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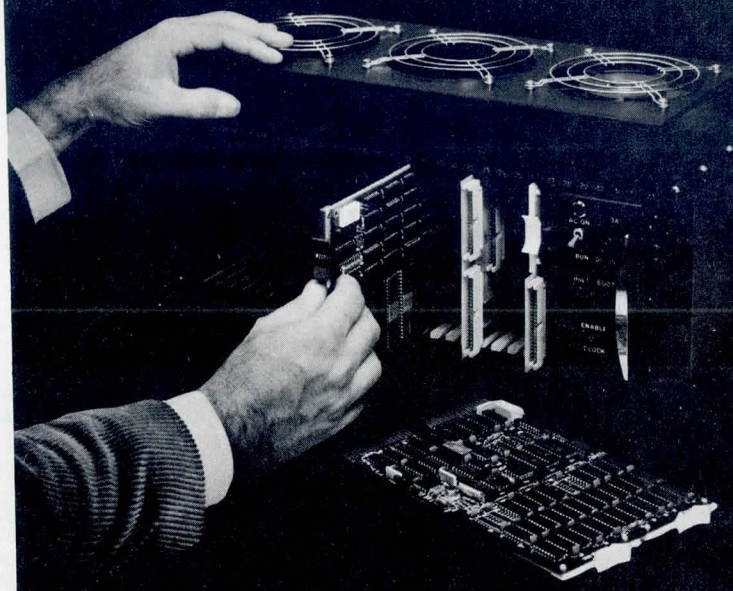

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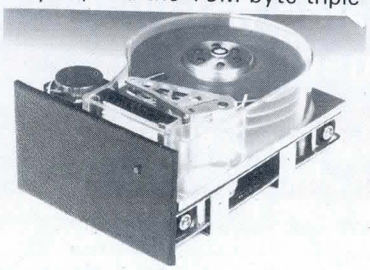
CIRCLE 105 ON INQUIRY CARD

5.25" Winchester Drives Offer Capacity and Interface Options

A 5.25" (13.33-cm) Winchester disc drive family, SA600 series comes in 3 versions: the single-platter SA602 with 3.33M-bytes (unformatted) storage capacity, the double-platter SA604 with 6.66M bytes, and the 10M-byte triple-platter SA606. Designed to complement Mini-floppy™ drives in desktop business systems, the unit's form factor is exactly the same. Identical physical dimensions and mounting holes allow easy use of both types in the same system; identical power requirements permit the use of a single power supply for both. Average access time of the units is 75 ms (160 max); transfer rate is 4.34M bits/s, track to track access time 18 ms (including settling); and track density 256/in (100/cm). One interface design is pinout-compatible with the standard Minifloppy, permitting the two types to interface using the same control lines; the other design is pinout-compatible with existing 5.25" Winchesters already being supplied.



The housing is surrounded by a heavy duty wire form frame that is fitted with true shock mounts. An integral brake/lock mechanism automatically secures both rotary actuator and spindle when the drive is powered off, preventing damage to both media and heads. The otherwise unused area of the disc surface, inside the data bands, is designated a shipping zone to which the heads can be accessed before the drive is powered off. **Shugart Associates,** 475 Oakmead Pkwy, Sunnyvale, CA 94086.

Circle 200 on Inquiry Card

Multifunction Logic Analyzers Link For 64-Channel Operation

The PI-616, a high performance 16-channel logic analysis tool, is suited to hardware development, debug, and maintenance applications. When combined with the 48-channel, software oriented PI-648, a powerful hardware/software test and integration system is attained. Collecting data in a 16-channel x 1000-word data memory at rates up to 50 MHz, the -616 provides keyboard commands that allow users to configure the data memory for 8-channel operation at 100 MHz or split the memory for 8 channels of data collection plus 8 channels of glitch storage. Glitches as narrow as 5 ns can then be collected and highlighted on the CRT. The instrument can also be configured with a waveform recording option that adds high speed digital oscilloscope functions. In this configuration, an analog signal is sampled at rates up to 50 MHz, stored in a 1000-word memory, and then software smoothed for display. A cursor provides instantaneous voltage and time data as it is moved along the waveform.

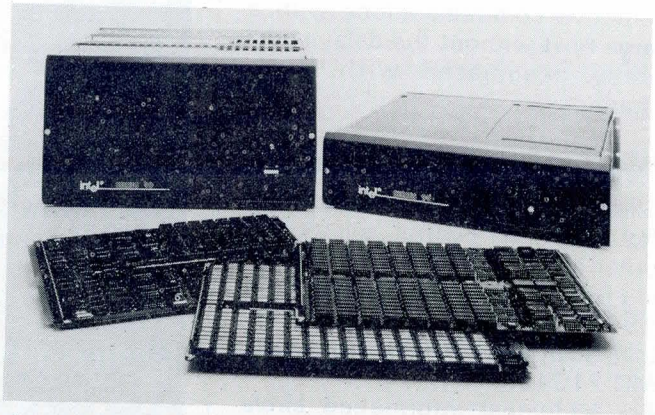
For analysis of software and hardware interactions, the -648 collects 48 channels of synchronous data in its 250-word memory at rates corresponding to 15M system operations/s. Features include 3 separate clocks for demultiplexing, two 54-bit clock qualifiers, 16 levels of nested triggering, and data search and comparison functions. Furthermore, the unit is fully compatible with probe accessories for serial (RS-232) analysis and disassembly of 8- and 16-bit microprocessor program flow. **Paratronics, Inc,** 2140 Bering Dr, San Jose, CA 95131.

Circle 201 on Inquiry Card

High Density Memory Modules Use 16k x 1 Static RAMs

Capacities up to 128k words x 22 bits in unidirectional and 64k words x 44 bits in bidirectional mode are attainable on CM-92 memory modules through use of high speed 2167 static RAM chips. The 16k x 1 RAMs achieve 4 times the memory density of presently available static RAMs with no increase in power consumption or loss of performance. The higher density reduces costs of large capacity systems by minimizing the number of memory modules, chassis, and power supplies where memory capacity exceeds that of a single chassis. In addition, the unit allows users to move up to higher density devices without changing system interface.

In addition to the greatly increased memory density and low power consumption, the two configurations maintain performance levels of earlier static RAM modules with 100- and 140-ns cycle times and 70- and 95-ns access times. The combination of high density and static operation adapt



the unit to use in mainframe and minicomputer applications such as array processing. **Intel Corp,** 1302 N Mathilda Ave, Sunnyvale, CA 94086.

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15V	3.4A	SD15-3.4
24V	2.1A	SD24-2.1
28V	1.8A	SD28-1.8
SIZE: 2"H X 4.88"W X 6.25"L		

$170
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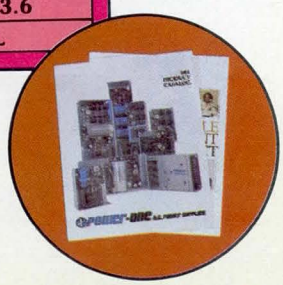
VOLTS	AMPS	MODEL
5V	20A	SF5-20
12V	8.4A	SF12-8.4
15V	6.7A	SF15-6.7
24V	4.2A	SF24-4.2
28V	3.6A	SF28-3.6
SIZE: 2"H X 4.88"W X 10"L		



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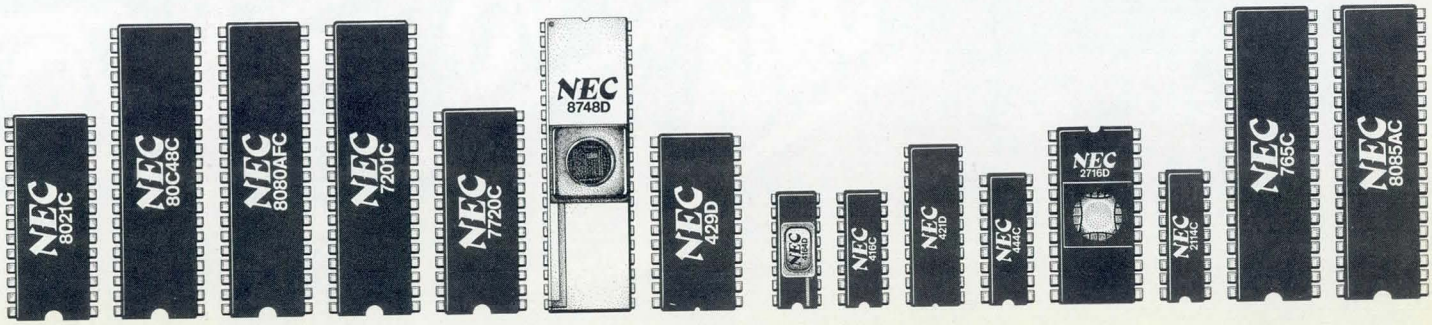

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When you need a powerful processing system that talks to your world... you need a COMMANDER COMPUTER. Four standard RS-232C ports handle serial data to 19,200 baud, allowing you to add low speed peripherals or even communicate with remote devices over a phone line. But if you need higher speed or more flexibility, use COMMANDER's parallel I/O under program control. And, if that's not efficient enough, select the optional DMA port to process parallel data on a cycle-steal basis direct to memory. COMMANDER's optional IEEE/488 controller gives you direct interface to the world of instrumentation and a host of compatible devices readily available. The optional Real Time Interface module gives you individual bit I/O to input status lines and digital sensor signals ...or to output alarms and commands. And you can use up to four independent programmable real time clocks for precise time interval control without wasted processor time. Inquiries for custom features are welcome.

BUT THAT'S NOT ALL...Select the COMMANDER configuration to fit your system need. The models 500 and 900 have an integral CRT and keyboard while the models MX and FX (not pictured) can be married to a simple terminal for operator interface. Add the optional arithmetic unit for high speed fixed point or floating point processing. And, if your application requires graphics, optional memory is added to provide 512x256 video graphics capability.

All COMMANDER models will execute higher level programs in BASIC, FORTRAN or COBOL or machine level programs in MACRO-80 Assembler. Operating programs are executed under CP/M™ FDOS, the new MP/M™ operating system or UCSD Pascal.™

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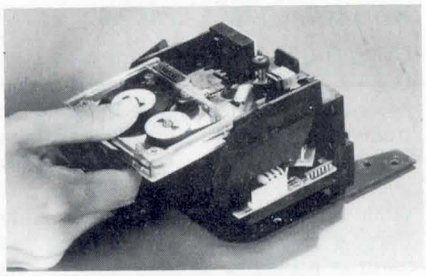
™UCSD Pascal is trademark of University of California

MEMORIES

MINICARTRIDGE DRIVE



An economical transport for DC100A type data cartridges, the compact TM 110 Minicartridge Drive serves as an OEM building block for minicomputer and microprocessor systems where size, cost, low power consumption, and reliability are considerations. In conjunction with a minicartridge type 3M DC100A, the unit has capacity of 1.34M bits (unformatted) or 120k bytes (formatted). It has an 8000-bit/s transfer rate. The transport accepts phase encoding, 800-bit/in (314/cm) density, formatted per ECMA 41, with 256 data bytes/block. All components and subassemblies, including head, motor, detectors, and printed circuit board, are mounted on a precision molded, high strength plastic frame. Guides in the frame position cartridge during insertion. Final phase of insertion travel is executed by a spring loaded toggle action that forces tape against the head and belt drive roller against the motor capstan at proper operating pressures. The recording head mounts precisely to the frame and is alignment free. The unit can be mounted horizontally or vertically. Power required is 5 and −12 V; power consumption is 4.5 W average. **Burroughs Corp,** Burroughs Pl, Detroit, MI 48232.

Circle 203 on Inquiry Card

256k-BYTE SEMICONDUCTOR ADD-IN FOR PDP-11/44

DR-144S is a single-board 256k-byte add-in for DEC's PDP-11/44 minicomputer. Completely compatible with MS11-M memory module, it functions as a 128k x 16-bit system, although internally configured as 64k x 39. The 39-bit word consists of two 16-bit words plus 7 ECC bits. Although 16k dynamic RAMs are used, the design allows use of 64k RAMs when they become economically viable. With 64k RAMs the board would provide 1M bytes on a single hex board. The system occupies one hex slot in the computer chassis and operates with its 22 extended Unibus (EUB) address lines. The EUB allows addressing capability to 4M bytes. Memory starting location may be set in 64k-word increments up to 1920k words. Read and write cycle times are 500 and 1000 ns max. Read access time is 525 ns max; and refresh cycle time is 500 ns. The unit requires 5, 12, and −12 V. LED indicators on the board indicate presence of 5 V and error status. Operation is guaranteed from 0 to 55 °C. **Dataram Corp,** Princeton Rd, Cranbury, NJ 08512.

Circle 204 on Inquiry Card

DEC COMPATIBLE OEM SEMICONDUCTOR MEMORIES

Add-in/add-on memories include 94134P for PDP-11/34 and -11/44, 94178 for VAX-11/780, and 94170 for PDP-11/70. Configured with storage capacities ranging from 32k to 256k 18-bit words, the 94134P operates with either standard or modified Unibus system. It features extended 22-bit addressing and onboard parity check circuitry, and serves as replacement for DEC MS11-L series memory. 94178 is available in a 32k x 72-bit configuration with read/write, and refresh operating modes. In addition to basic 250-ns access and 400-ns cycle times, this array features 400-ns refresh and 800-ns write cycle times. Refresh operation, externally controlled by the VAX memory controller, allows refresh cycle to be performed on the assembly's memories according to timing and control constraints of the memory control logic. The 94170 add-on memory is available with capacity from 512k to 4M bytes in 512k-byte increments. The system features 460-ns access time and 600-ns read and 800-ns write cycle times. It uses error correction circuitry that provides single bit error correction and double bit error detection. **Control Data Corp,** PO Box 0, Minneapolis, MN 55440.

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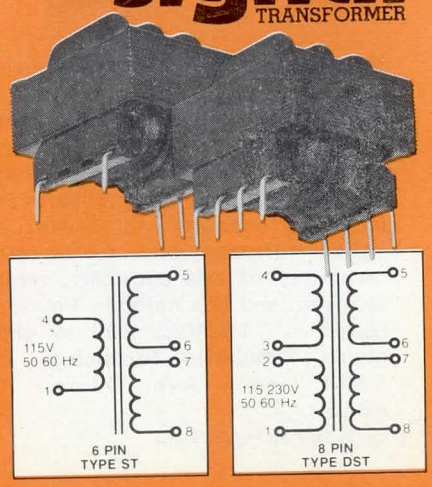


CIRCLE 163 ON INQUIRY CARD

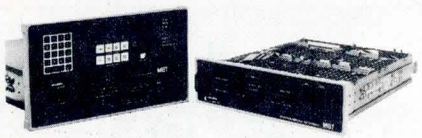
SUBASSEMBLIES AND CIRCUIT COMPONENTS

TOUCH SENSITIVE CRT ADD-ON KITS

Add-on kits use a capacitance sensitive faceplate which is mounted in front of the CRT monitor of the existing terminal. When the faceplate is touched by the human finger, detected changes in capacitance are identified and interpreted. In contrast with earlier techniques, the method uses no mechanical contacts, active electromagnetic, or acoustic elements. A continuous recalibration feature compensates for temperature, humidity, or other environmental fluctuations or changes, resulting in error free accuracy in virtually any operating environment. Std kits are provided in 32 touch position configurations for 12″ and 15″ (30- and 38-cm) CRT monitors. Std electronic outputs are provided for either parallel or serial interfaces. The Z80 based electronics interface to the faceplate occupies less than 25 in² (161 cm²) of PC area and requires less than 500 mA at 5 V (± 12 V at 200 mA for RS-232). **Interaction Systems, Inc,** 24 Munroe St, Newtonville, MA 02160.

Circle 206 on Inquiry Card

MICROPROGRAMMABLE MULTIPLEX BUS INTERFACE



Multiplex Bus Terminal (MBT) provides general purpose interface between MIL-STD-1553 data bus systems and a minicomputer, supporting hardware development and test system integration. Microprogramming provides flexibility to support F-16, 1553A, and 1553B formats and to simulate responses of bus controller, remote terminal, and bus monitor. Power required is 110 Vac, 300 W single phase. **Simulation Technology, Inc,** 4124 Linden Ave, Dayton, OH 45432.

Circle 207 on Inquiry Card

RS-232 TO CURRENT LOOP ADAPTER

Allowing use of an RS-232 terminal instead of a current loop teletype with KIM microcomputers, the ADA400 adapter both converts an RS-232 signal to a 20-mA current loop signal and a 20-mA signal to RS-232. With this adapter, a computer's teletype port can be used to drive an RS-232 terminal, or the reverse, without modification of the port. In addition, the device can be paralleled to drive a Teletype or RS-232 printer while using regular terminals. **Connecticut microComputer, Inc,** 34 Del Mar Dr, Brookfield, CT 06804.

Circle 208 on Inquiry Card

OPTICAL BADGE READER

Said to be the first of its type to have an integral optically generated strobe pulse for each column whether or not the badge is punched, punched badge reader DSR-100 reads standard 12-row 20-col badges or 12-row 22-col credit cards. It uses GaAs LED sources and phototransistor sensors, measures 6 x 1.5 x 5.5″ (15 x 3.8 x 14 cm) and weighs 12 oz (336 g). Open collector sensor outputs can be directly interfaced with low impedance TTL or high impedance CMOS logic. All external connections are via two 20-way ribbon cable connectors. **Programming Devices Div, Sealectro Corp,** Mamaroneck, NY 10543.

Circle 209 on Inquiry Card

OEM CONTROL MODULES

Providing step times as fast as 5 ms for sequencing operations, 800 HS is engineered for use in original design or retrofit of automation and machine control applications requiring higher speed operations than those typically available from CAM programmers, stepping switches, and drum timers. Series consists of a control module capable of driving 8 output devices (expandable to 40), an array of output modules for driving ac and dc devices, a time module for synchronizing system operation to time of day, and a power module. **Control Technology Corp,** 82 Turnpike Rd, Westboro, MA 01581.

Circle 210 on Inquiry Card

4-CHANNEL R/W HEAD WITH EQUAL TRACK SPACING

Using 0.020″ (0.508 mm) tracks on 0.040″ (1.016 mm) centers, 4-channel head provides equal spacing of tracks for cassette and minicartridge applications. This format reduces leakage inductance and crosstalk, while improving sensitivity. In addition, a 0.005″ (0.127-mm) guard band is provided at tape edges. The full metal face and hyperbolic contour ensure good tape contact with or without pressure pads. Gap lengths range from 0.000050 to 0.000500″ (1.27 to 12.7 mm). **Forglo Corp,** 3rd & Reagan Sts, Sunbury, PA 17801.

Circle 211 on Inquiry Card

VOICE SYNTHESIS MODULE

The VSM2032 module incorporates a single-chip speech synthesizer with a timeshared 2-stage filter section (SP-0250), a PIC1650A microcomputer, and a std 32k ROM (RO-3-9333). The 3 MOS/LSI devices are fabricated with n-channel ion implant technology. The module forms a complete speech system capable of storing 30 s of speech. It can combine 32 words and syllables to form over 1G phrases. Audio output is 200 mW. The unit has an operating temperature of 0 to 70 °C, and measures 3.25″ x 5.0″ (8.2 x 12.7 cm). **General Instrument Corp, Microelectronics Div,** 600 W John St, Hicksville, NY 11802.

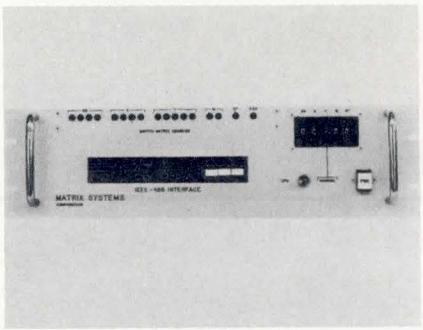
Circle 212 on Inquiry Card

SPEECH SYNTHESIZER

Series III speech module consists of speech synthesizer, vocabulary data memory, onboard speech filter, and audio amplifier, and accommodates std and custom vocabularies up to 256 total utterances. Memory is any combination of one or two 16k, 32k, or 64k ROMs or P/ROMs providing up to 128k bits; approx 100 s of speech can be stored in ROM, allowing words and phrases to be retrieved on command. TTL-compatible I/O and 5-V single supply simplify interfacing to microcomputer bus or I/O port. **Telesensory Systems,** 3408 Hillview Ave, Palo Alto, CA 94304.

Circle 213 on Inquiry Card

IEEE-488 INTERFACE CHASSIS



Model 6595-M interface acts as a listener on the IEEE-488 bus and converts the 8-bit parallel bus signal to a 16-bit TTL positive signal compatible with the relay matrix. Front panel LED display shows status of the 16-bit output from the unit. Available in CPU control configuration or with an alternate manual control feature, the chassis measures 5.25 x 19 x 15" (13.33 x 48 x 38 cm). **Matrix Systems Corp,** 5177 N Douglas Fir Rd, Calabasas, CA 91302.

Circle 214 on Inquiry Card

LSI-11 TO PRINTER ASYNCHRONOUS SERIAL INTERFACE

Offering complete DEC DLV-11F compatibility, MLSI-DLV-11F interface provides buffer ready/printer busy monitor circuit in the EIA mode. Features include four levels of priority interrupts; serial EIA-RS-232C/CCITT V.24 interface; 20-mA current loop interface; programmable, switch-selectable baud rates of 50 to 19.2k; and switch-selectable word character format, address, and interrupt vectors. **MDB Systems, Inc,** 1995 N Batavia St, Orange, CA 92665.

Circle 215 on Inquiry Card

SMALL, CODED ROTARY SWITCHES

For applications such as avionics, navigation, and telecommunications, series 56000 switches are fully sealed and contamination resistant, and measure 0.688" (1.747 cm) in diameter. Std features include 8 dial positions, knob actuation, and pin terminals for PCB mating. Various dial positions, pull to turn isolation stops, and solder lug pin terminals are options. Shock resistance is greater than 100 Gs; rated current is 28 Vdc at 128 mA resistive; and op temp is −65 to 100 °C. **The Digitran Co,** 855 S Arroyo Pkwy, Pasadena, CA 91105.

Circle 216 on Inquiry Card

CAPACITANCE KEYBOARD

A replacement keyboard for Keytronics L1660, MPNK-72 is a low profile, solderless contact key switch keyboard featuring microprocessor controlled P/ROMs that allow custom programming. The device offers single 5-Vdc supply, automatic repeat, an electronic shift lock with LED target, and patented N-Key rollover. With rugged construction and rigid chassis mounting, it utilizes the replaceable silent "snap in" switch that offers greater than 100M keystroke MCBF. **Amkey, Inc,** 220 Ballardvale St, Wilmington, MA 01887.

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The Ambassador III Portable Terminal... puts you in two places at the same time!

Whether you're transmitting data or retrieving it, the Portable Ambassador III Terminal with its built-in 300 baud telephone coupler gives you immediate access to all kinds of important data.

At a realistic price, the Ambassador III is the perfect companion for remote bureaus, insurance executives, salesmen, bankers, educators, accountants, stock brokers, or any profession where you're away from a central office and quick versatile, reliable communications are vital.

Consider these features: full 7" screen displays 24 lines of 80 characters per line. Weighs less than 20 pounds. Measures 18" x 15" x 8". Utilizes virtually any power source. Can be used anywhere in the world using ASCII standard protocol, conversational or time sharing. The Ambassador III's commands are also a subset of the DEC VT 103. **Telcon also manufactures the Ambassador IV with an 80 column printer.** For additional information contact the distributor's office nearest you.

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CIRCLE 109 ON INQUIRY CARD

ONE GREAT SHOW DESERVES ANOTHER

Since the COMDEX show was first established two years ago, and particularly after the recent overwhelming success of COMDEX '80, many vendors and ISOs alike have been telling us that this unique conference and exposition once a year just isn't enough.

Hello there, COMDEX/SPRING!

The big push is on to computerize America, boost productivity in every office and shop across the land. That's why Independent Sales Organizations (ISOs) are springing up like dandelions after the rain. Vendors are accelerating their schedule of new product introductions, and their intense search for independent sales representation.

Thus, COMDEX/SPRING, in New York City, June 23-25, 1981. If you're a computer industry marketer, whether vendor or ISO, you've now got TWO opportunities each year to get together with the people who really count. You've got COMDEX/SPRING in New York in June, and you've got COMDEX '81 in Las Vegas in November. That's a one-two marketing punch guaranteed to get the job done!

Who exhibits at the COMDEX shows?

Leading vendors of small computer and word processing systems, peripherals, software and media-supplies-services have been flocking to COMDEX since its inception in 1979. Write or call us immediately for detailed information on COMDEX/SPRING and, among other things, we'll send you a list of more than 360 such companies which exhibited at COMDEX '80.

ISO, as defined in our dictionary.

ISO (ai-ess-oh) Independent Sales Organization. Acronym coined by The Interface Group in summer 1979 as convenient umbrella for all independent third-party sellers of small systems and related products and services. Such as: *Dealers, distributors, systems houses, commercial OEMs, computer retailers, manufacturers' reps, turnkey vendors, office machines/products dealers, software houses, etc.* The acronym has gained widespread acceptance, following its introduction by COMDEX.

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For further information, write to COMDEX/SPRING '81,
160 Speen Street, Framingham, MA 01701.
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Another Conference and Exposition from THE INTERFACE GROUP
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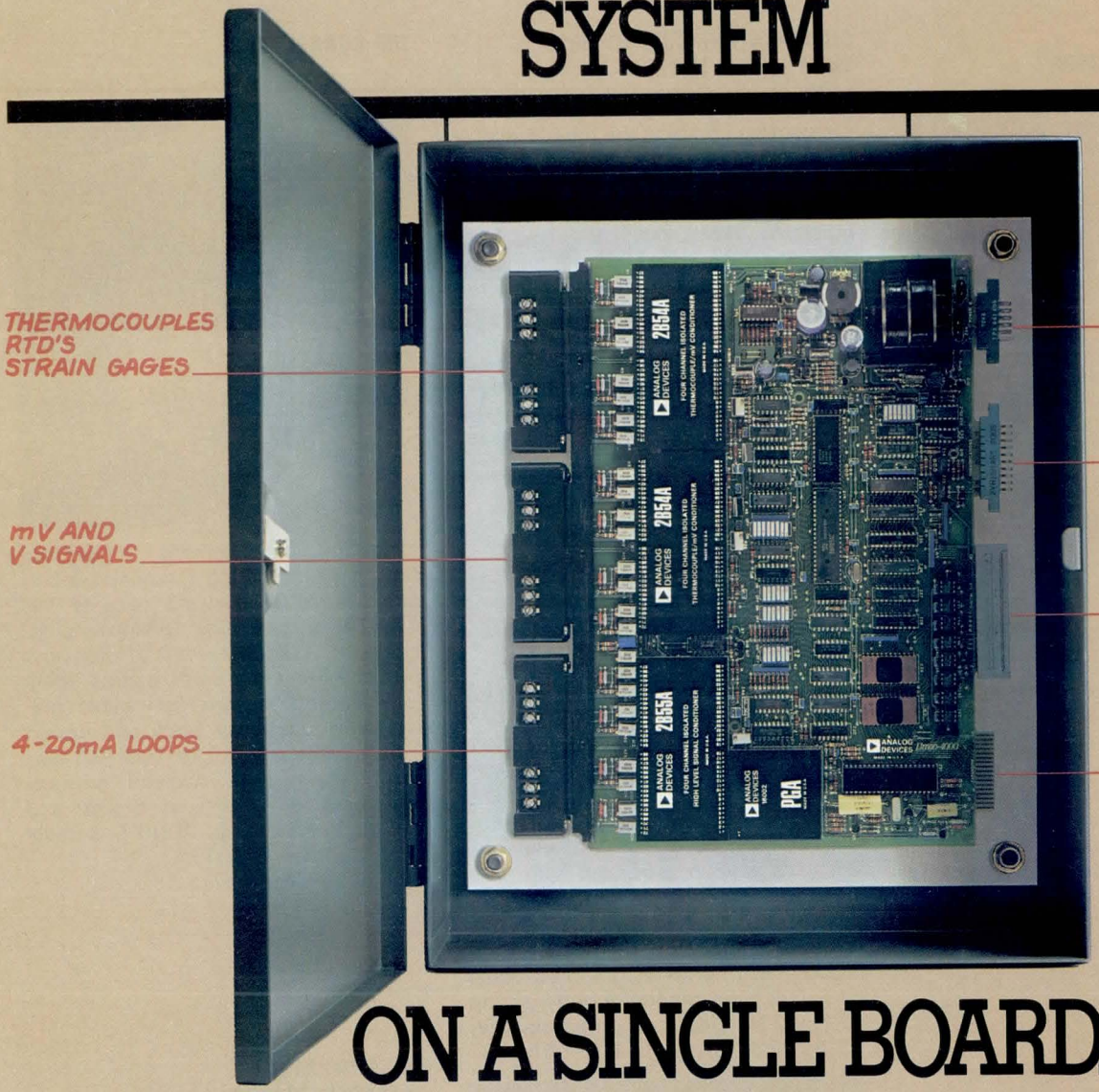
CIRCLE 110 ON INQUIRY CARD

THE FIRST COMPLETE SENSOR-BASED MEASUREMENT AND CONTROL SYSTEM



ON A SINGLE BOARD.

At last, there's a single board solution for both local and remote industrial measurement and control. It's μMAC-4000—the low-cost per channel, easy-to-implement system that can be used anywhere a cluster of sensors and analog signals must be conditioned and digitized.

μMAC-4000 is a fully integrated, pre-calibrated, intelligent system, complete with sensor signal conditioning, multiplexing, A/D conversion, digital I/O and serial communications to any host computer. Its on-board microcomputer unburdens the host CPU by performing sensor linearization, scaling and conversion to engineering units, and limit checking.

μMAC-4000 was designed to accurately process low level transducer signals in the harshest environments. Its accuracy is assured by high quality signal conditioning, featuring input protection, ±1000V channel to channel and input to output isolation, high noise rejection, RFI/EMI immunity and low drift amplification. And with μMAC-4000, you can readily mix and match signal conditioning modules as you require.

For the full story, write Analog Devices, Box 280, Norwood, MA 02062, or call (617) 329-4700.

ANALOG DEVICES

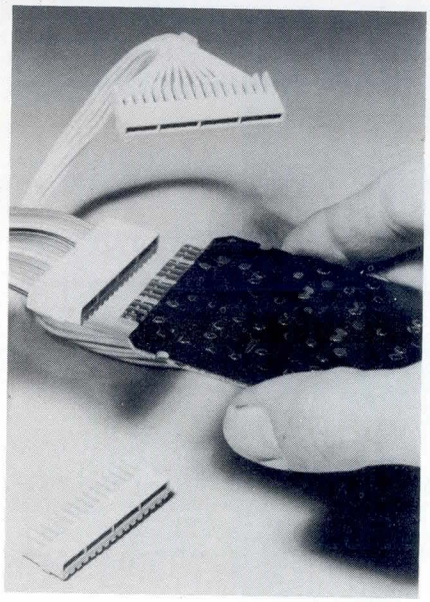
WAY OUT IN FRONT.

Analog Devices, Inc., Box 280, Norwood, MA 02062; East Coast: (617) 329-4700; Midwest: (312) 894-3300; West Coast: (714) 842-1717; Texas: (713) 664-6704; Belgium: 031/37 48 03; Denmark: (02) 84 58 00; England: 01/941 0466; France: 01/687 3411; Germany: 089/53 03 19; Japan: 03/263 6826; Netherlands: 01620-51080; Switzerland: 022/31 57 60; Sweden: 08/282 740; and representatives around the world.

CIRCLE 111 ON INQUIRY CARD

PACKAGING AND INTERCONNECTION

SINGLE-READOUT CARD EDGE CONNECTOR



1500 series 0.100" (0.254-cm) center mass terminated insulation displacement connectors offer std Jaguar series features and are available in 4 through 15 positions. Connectors terminate with flat ribbon cable or discrete wires, 24 through 30 AWG. Housings are molded of glass reinforced nylon and contacts are copper alloy, tin plated. **Methode Electronics, Inc,** 1700 Hicks Rd, Rolling Meadows, IL 60008.

Circle 218 on Inquiry Card

FIBER OPTIC FACE PLATES

Engineered for silicon photodiode arrays, linear or matrix arrays, and charge-coupled devices, fiber optic face plates are precision ground and polished, then installed in intimate optical contact with the silicon photodiode array to prevent loss of resolution. To ensure device life, face plates are hermetically sealed. The units typically incorporate 6-μm diameter fibers with a numerical aperture of 1; other values can be specified. **HSS, Inc,** 2 Alfred Cir, Bedford, MA 01730.

Circle 219 on Inquiry Card

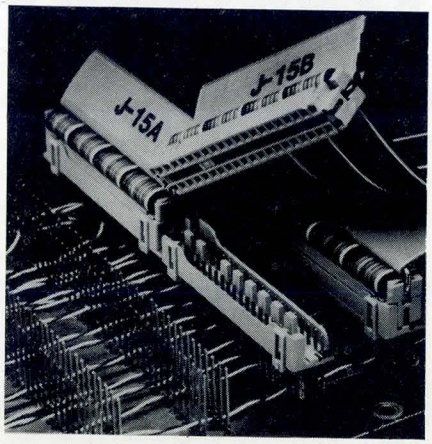
SUBMINIATURE CONNECTORS WITH EMI/RFI FILTERS

GH series rack and panel subminiature connectors combine the functions of a D subminiature type connector with low, mid, standard, or high frequency feedthrough filters to minimize emi/rfi problems. Produced in 9-, 15-, 25-, 37-, and 50-pin configurations, they meet MIL-C-24308 intermateability requirements. Incorporating rugged soldered grounds, environmentally sealed devices can be supplied with 3 types of contacts in any mix: filter, power, or ground. **General Connector Corp,** 80 Bridge St, Newton, MA 01258.

Circle 220 on Inquiry Card

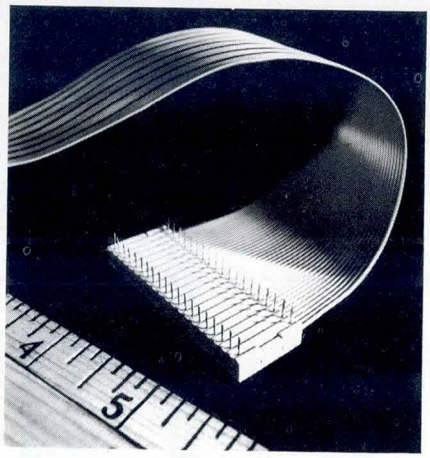
MASS TERMINATION BACKPLANE SOCKETS

Available in 20, 26, 34, 40, and 50 positions, 0.100 x 0.200" (0.254 x 0.508-cm) Scotchflex backplane socket/header system interfaces with 0.025-in² (0.161-cm²) backplane wrap pins and mates with Scotchflex flat cables in 26 or 30 AWG solid, and 28 AWG solid or stranded wire versions. Uniform engagement eliminates need to cut pins and allows for two layers of wrap below the header. Keying devices fit onto header, interfacing with 2 slots on connector body, acting as lock. **3M Electronic Products Div,** PO Box 33600, St Paul, MN 55133.



Circle 221 on Inquiry Card

DIP CONNECTORS



Insulation displacement connectors for mass terminating 50-mil flat ribbon cable are offered in std sizes of 14, 16, 24, and 40 pins. Design is pluggable to IC sockets and affords low profile installation on PC boards; snap lock detents ensure firm cable grip between connector body and cover. Temp range is −55 to 105 °C; current rating is 1 A; and contact resistance is 10 mΩ at 6 Vdc and 0.3 A. **Belden Corp,** 2000 S Batavia Ave, Geneva, IL 60134.

Circle 222 on Inquiry Card

DEC COMPATIBLE EXTENDER BOARDS

DE2ET (dual), 4ET (quad), and 6ET (hex) are compatible with DEC products, including the VAX. Cards use gold-plated, double-looped test points on every connection between the card under test and the backplane. Each test point is clearly identified with connector contact number and is arranged in a staggered fashion so that probes can be attached without danger of short circuit. Heavy ground strips down the side of the card are used for putting ground clips of test cables on. **Hybricon Corp,** 410 Great Rd, Littleton, MA 01460.

Circle 223 on Inquiry Card

THE SMART SET

Members of this exclusive circle of PRIAM Winchester disc drives have several uncommon things in common. With database capacities from 10.8 to 158 megabytes, they all have the same interface. And they all connect quickly and easily to the typical microprocessor I/O bus through PRIAM's SMART Interface.

A simple adapter, added to the SMART Interface, is all you need to provide your system with the remarkable reliability of Winchester disc drives. And PRIAM's DISKOS drives have the broadest available capacity range, with the lowest cost-per-megabtye, for microprocessor-based systems.

How Smart Is SMART?

With its own sophisticated preprogrammed microprocessor, PRIAM's optional SMART Interface gives you these disc subsystem functions:

Controls any combination of one to four PRIAM Winchester disc drives.

Serializes and deserializes data and formats disc with selectable sector sizes of 128, 256, 512 or 1024 bytes.

Full sector buffering permits data transfers at any rate up to 2 megabytes per second, with programmed I/O or DMA.

Automatic alternate sector assignment makes disc defects transparent to the host processor.

Overlapped-command and implied-operations capability improves system throughput in multiple-drive systems.

The single 8″ x 14″ SMART Interface printed circuit board mounts on the PRIAM disc drive and draws power from the drive; or it can be mounted separately to maintain the basic drive size envelope.

Meet The Elite! PRIAM's High-Capacity, Cost-Effective 14-Inch Disc Drives

PRIAM's high-technology 14-inch Winchester disc drives are available with capacities of 34 and 68 megabytes, with a 158-megabyte version on the way. And they all fit in the same 7″ x 17″ x 20″ package, including optional power supply. Fully servoed linear-voice-coil head positioning provides fast, precise and reliable data retrieval. Average positioning time is only 45 milliseconds, and track-to-track is a fast 8 milliseconds for high throughput.

Use of a brushless DC spindle motor assures mechanical simplicity, positive disc speed control, and operation of PRIAM drives with power sources anywhere in the world without change. No relays, no mechanical brakes, no brushes, belts, or pulleys. Pure, reliable electronic control. Elegantly simple!

The Talk of the Town: PRIAM Eight-Inch Disc Drives

When you want to debut a Winchester disc drive where you now have an 8-inch floppy disc, PRIAM's DISKOS 2050 and 3450 fit right in. And they give race-horse performance to your system by expanding your database to 21 or 35 megabytes, with head-positioning times of only 45 milliseconds average and 8 milliseconds track-to-track.

From the same technical family tree as their bigger brothers, PRIAM 8-inch drives use linear-voice-coil positioning and brushless DC motors. In the next generation, they will permit database expansion to 70 megabytes, in the same small, interface-compatible package.

If a simpler, even lower-cost drive will serve your purpose, the DISKOS 1070 gives you 10.8 megabytes of capacity, with stepper-motor positioning for seek times of 73 milliseconds average and 23 milliseconds track-to-track. Not as fast as other PRIAM family members, but still just as SMART when used with PRIAM's SMART Interface.

Other Interface Options!

Is SMART too smart? PRIAM also offers a lower-cost serial-bit NRZ data interface for the OEM who wishes to design the complete controller or to purchase one. This interface, similar to the evolving ANSI standard, has an 8-bit bidirectional microprocessor interface for all spindle motor and head positioning controls.

And if you have an existing storage module controller, PRIAM offers an SMD interface to extend the life of your controller and software and put Winchester disc drive benefits into your system quickly and easily.

For complete information about the SMART Interface and the members of the SMART SET of PRIAM Winchester disc drives, RSVP by telephone or mail to:

Visit us at NCC. Booth #4704 & #4705, Concourse Level, McCormick Place.

PRIAM

3096 Orchard Drive San Jose, CA 95134
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CIRCLE 112 ON INQUIRY CARD

With Raytheon new Beam-Penetration Color CRT's. Designed specifically for computer color-graphic system applications, Raytheon Beam-Penetration Color CRT's offer better color resolution and better overall system performance than conventional color tubes and other beam penetration CRT's.

Available in 15″ to 25″ diagonal rectangular and 10″ to 23″ dia. round sizes, Raytheon Beam-Penetration Color CRT's feature the unique Raytheon patented split-anode design. And this means faster switching, constant focus voltage and good spot size for all colors.

Such tubes are just one example of Raytheon's wide choice of versatile, performance-proven CRT's that are available in a variety of electron-gun types and phosphors and in all shapes and sizes 3″ to 25″.

Color it right. Color it with Raytheon Beam-Penetration Color CRT's. For complete information, contact the Marketing Manager, Raytheon Company, Industrial Components Operation, 465 Centre St., Quincy, MA 02169. (617) 479-5300.

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CIRCLE 113 ON INQUIRY CARD

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CITE is a new show for the reseller industry — dealers, distributors, OEM's, system integrators, consultants, value adders, turnkey vendors, and software and service organizations.

CITE-CON, the accompanying conference and seminar series, features topics important to the reseller's business future — managing leading edge technology in a rapidly expanding marketplace!

It's the one place to meet with the vendors that provide big business opportunities for you. Meet them when they are prepared to talk the language of the reseller in a marketplace that's private to your trade.

The CITE schedule and format allows attendance at conference sessions without missing any exhibit hours, and the show closes on a Friday, leaving open the possibility of a wonderful weekend at Atlantic City's world-famous beach in summer.

Decide now to gather with the industry in June at Atlantic City's Convention Hall! Register now for CITE-CON, the reseller conference that will show you new ways to profit in the 1980's.

CITE's CONFERENCE DIRECTIONS

CITE's profit-minded conference will deliver a powerful package of up-to-the-minute management and technical information to the busy OEM and systems integrator! But attendees will have plenty of time to explore the exhibits and make new friends because the program manager, CW/Conference Management Group, has come up with a timetable that gets the most from the precious time you will invest in CITE!

You will start the program on Tuesday, June 23, the day before the show opens, with a full day of "In-Depth" seminars on key business and product trends, presented by leading vendors, system integrators, and technical and management consultants. Evenings are reserved to explore new business contacts in the new Atlantic City!

Get an early start on Wednesday and Thursday with "Early Bird Rap Sessions" at 7:30 a.m., with coffee to open your eyes to new solutions to your business problems! More conference sessions follow, just a few steps from the exhibit floor, until 11:00 a.m. when the exposition opens. All of mid-day is reserved to explore the show, until "Wrap-Up Sessions" begin at 4:00 p.m. when the show closes, focusing on some of the product and market issues you have seen in "three dimensions" at the show booths. Friday morning sessions bring down the curtain on an integrated show and conference experience!

CITE 81

CITE is sponsored by The Microcomputer Industry Trade Association (MITA)
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Want to speak at CITE? Call CW/Conference Management Group at **(800) 225-4698!** Want to exhibit at CITE? Call CITE Expo Sales headquarters **(201) 569-8542.** Want to attend? Register now or get on our lists for latest program information! Send in the coupon below!

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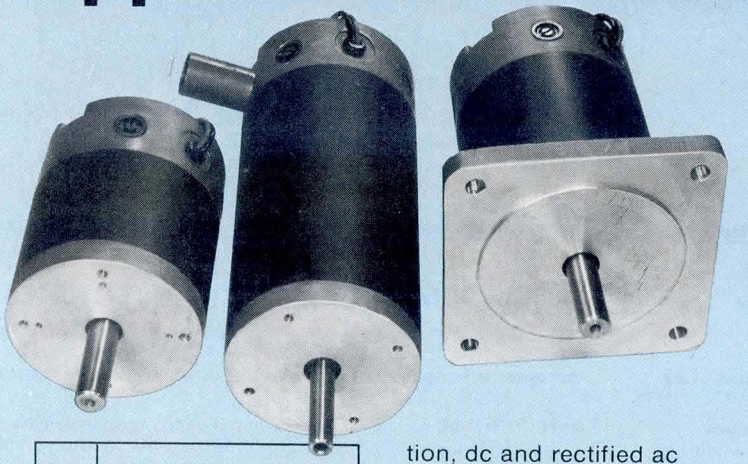
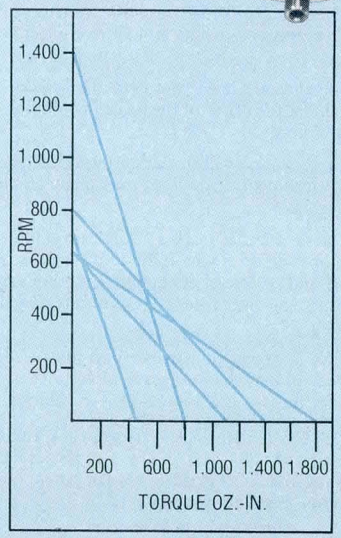
Lamb® pm motors are designed for high performance applications





High torque in small frame size saves space and weight.

These 4" diameter pm motors are for high-performance, variable-speed applications, particularly those requiring a repeatable, straight line speed/torque curve. Features include ball bearings, ceramic magnets, Class F insulation, dc and rectified ac excitation, rapid two-lead reversibility, stable commutation for long brush life and high current capability.

The motors are available in standard 5", 6", 7", 8" and 9" lengths and can meet requirements for continuous rated torque to 540 oz.-in. and peak torque to 2400 oz.-in. with speeds to 2000 rpm. Component recognized by U.L. Inc., the motors are widely used in data processing peripherals, reproduction equipment, machine tools and similar applications.

The design of the motor, coupled with Lamb Electric's manufacturing capabilities, make these motors a very economical power package for mid- and high-range production requirements.

For additional details, contact AMETEK, Lamb Electric Division, 627 Lake Street, Kent, Ohio 44240. Telephone (216) 673-3451.

AMETEK
LAMB ELECTRIC DIVISION

DATA COMMUNICATIONS

212A MODEM REPLACEMENT

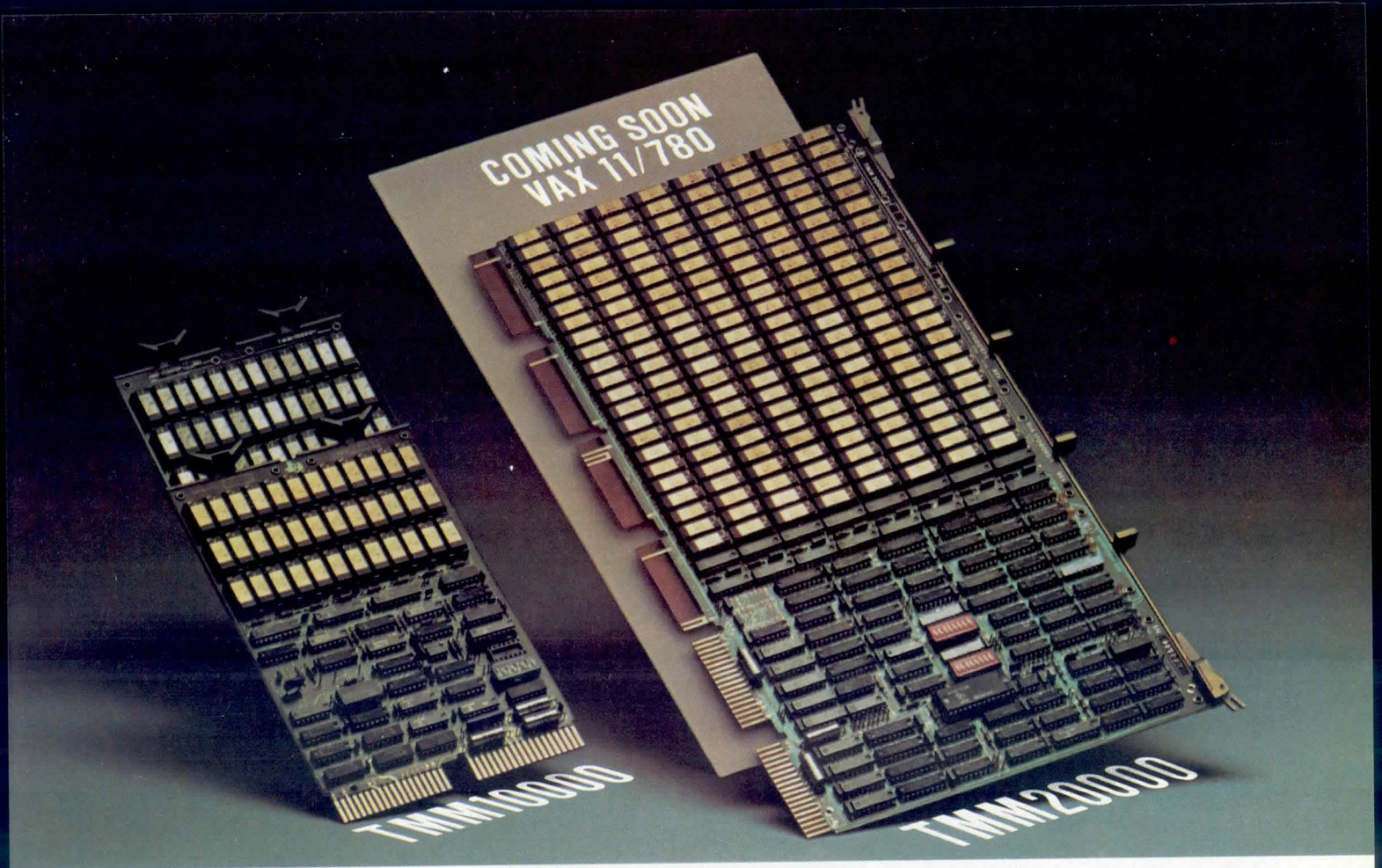
TC2121 optimizes full-duplex transmissions at either 300 or 1200 baud over switched networks. Compatible with Bell 212A modems and 103/113 series, the microprocessor controlled unit provides auto-answer and manual originate/answer. Other features include full-duplex operation over dial-up network, four local and remote test features, visual diagnostic indicators, asynchronous or synchronous operation, −50-dB sensitivity, and high accuracy and stability over wide variations in temperature, data rate, line voltage, and received signal amplitude. The unit uses Bell 103 series communications protocols to allow rapid changeover to 1200 baud without operating system changes. Low speed transmission can be asynchronous or synchronous. Eight status indicators are provided and all std Bell compatible options are available. Model TC2121-2 features built-in voice/data switch, eliminating need for special telephone handsets or auxiliary equipment; -3 includes built-in dial pad and autodialer that is auto redial and field programmable, and requires no telephone handset. **Tek-Com, Inc,** 2142 Paragon Dr, San Jose, CA 95131.

Circle 224 on Inquiry Card

LIMITED DISTANCE MODEM WITH RS-449/422 INTERFACE

Operating in 4-wire, full-duplex, and point to point, internally or externally timed, over unloaded twisted pairs or coaxial cables, the 2300M medium speed modems provide data rates between 64k and 460.8k bits/s. For transmission at higher speeds, the 2300H operates from 460.8k to 6.3M bits/s. Both units utilize bipolar digital transmission techniques, compatible with the Bell 551A channel service unit, and achieve error rates better than 10^{-9}. **Avanti Communications Corp,** Aquidneck Industrial Pk, Newport, RI 02840.

Circle 225 on Inquiry Card



New 96K word module. LSI-11/23 compatible. TI's growing memory systems family.

Quality. Reliability. Compatibility. And a new addition to our TMM10000 Series as the TI memory systems family keeps growing.

TMM10000 Series

- 64K words or new 96K words
- Optional parity
- Standard "dual" DEC board
- Low power

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- Error correction transparent to operating system
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85214A

CIRCLE 70 ON INQUIRY CARD

TEST AND MEASUREMENT

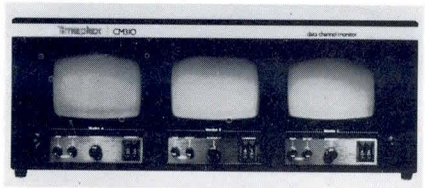
PORTABLE I/O CHANNEL TESTER

A diagnostic tool that pinpoints I/O channel problems in IBM system/370s and plug compatible mainframes, model 9 acts as a peripheral controller and interfaces with companion software in the mainframe under test. It exercises CPU I/O channels and identifies specific problems saving time and cutting system diagnostic costs. Useful for both system debug and channel burn-in testing, it speeds checkout and repair time for both OEM system integrators and mainframe builders. The unit operates as an intelligent microprogram controlled analyzer that recognizes addresses, interprets commands, receives and transmits data, monitors data transaction protocol including timing, and can force errors that should be detected by the mainframe's channel hardware. Errors are analyzed with help of 16-word FIFO buffer. An array of LED indicators and buffered test points allow operators to determine problems. Combinations of 6 LEDs display type of channel operation, and 8 more display nature of problem. Data bytes in and out of the mainframe are displayed on 18 LEDs; another 8-LED array displays bus historical data, and 4 more display 1 of 16 data file addresses. **Data-Ware Development, Inc,** 4204 Sorrento Valley Blvd, San Diego, CA 92121.

Circle 226 on Inquiry Card

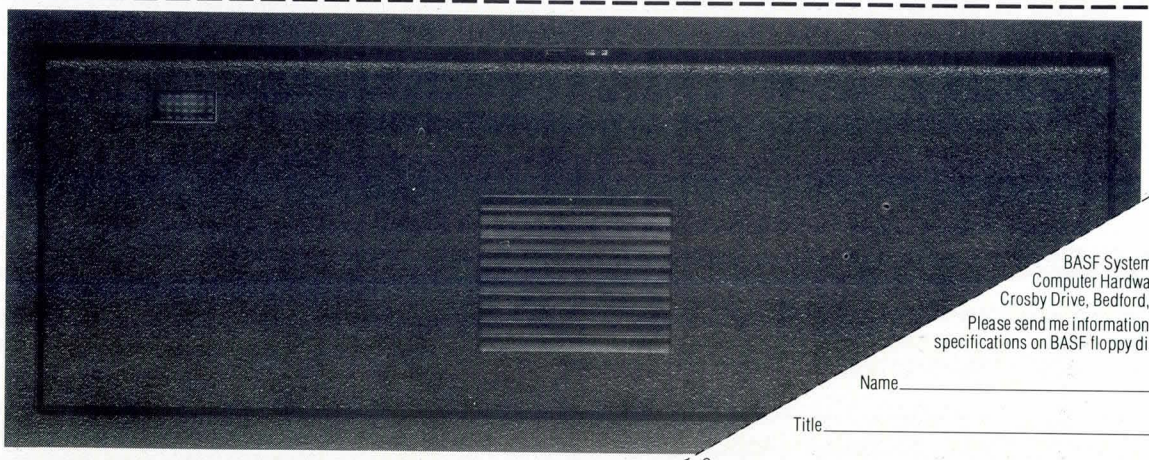
3-CHANNEL DATA MONITORING SYSTEM

CM310 simultaneously monitors all data transmitted on up to 3 asynchronous data communications channels and displays the output on its 3 CRT screens. Operating and display modes include both full- and half-duplex realtime monitoring and display as well as a range of arrested display and scrolling modes that allow close inspection of all data. In most modes, the system can be set to display changes in EIA functions and to flag and highlight data stream troubles such as parity errors or the absence of echoback data. It can interface with any data network equipment that meets EIA RS-232-C output standards, including DCE, DTE, or any combination of the two. The system does not interfere with operation of channels being monitored nor alter characteristics of the data stream. Once installed and tested, it requires no internal programming. It displays all 128 ASCII characters, including nonprinting characters, monitors speeds from 50 to 19,200 bits/s, and offers an internal 2000-byte buffer. **Timeplex, Inc,** One Communications Plaza, Rochelle Park, NJ 07662.



Circle 227 on Inquiry Card

Only BASF can run a floppy drive ad this small.



ACTUAL SIZE

The BASF 5.25" floppy disk drive is only 2.1" high, just ⅔ industry-standard height. You can put three of ours where only two of theirs fit, yet BASF drives pack all the performance and features of conventional-sized units. Expand your design options and shrink your space requirements. Write or call today (in the East, 617-271-4168; in the West, 714-752-6126) and get the big story.

CD-3

BASF Systems Corp.
Computer Hardware Sales
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Please send me information and specifications on BASF floppy disk drives.

Name_____

Title_____

Company_____

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BASF

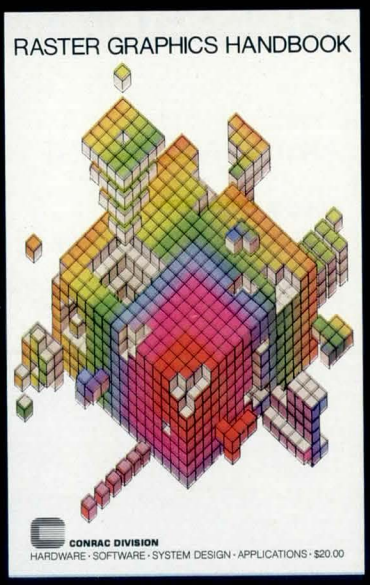
DO YOUR HOMEWORK FOR THE NEXT DECADE.

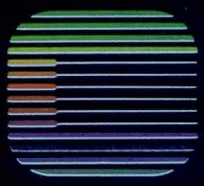
Presenting the Raster Graphics Handbook written and published by the Conrac Corporation. Only a company with experience in all video display applications, and only a company with the most extensive and competitive line of monitors could write this exciting book.

In it is everything you need to know about raster graphics. Whether you design computer systems for management decision-making, process control, cartography, image enhancement, trend analysis, or medical diagnostics, raster graphics will be the dominant information display medium of the '80's. The range of options and alternatives are limitless.

Decision-making images. To find out if you qualify for this book, simply circle the bingo number.

Catch up on your reading.





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DECISION-MAKING IMAGES

CIRCLE 165 ON INQUIRY CARD

TEST AND MEASUREMENT

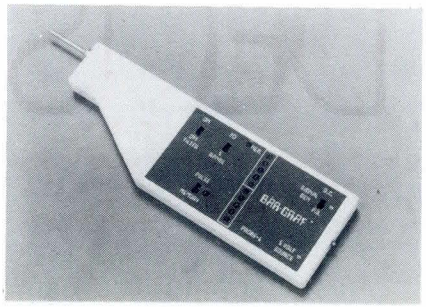
POWER LINE FAULT DURATION MONITOR

Monitoring power lines continuously for disturbances on 1- or 3-phase maine supply, FDM-3 Power Guard provides detection, process, analysis, and classification functions. Unit detects such line faults as voltage errors, transients, and frequency errors, even if left unattended for extended periods. It will also monitor a dc source simultaneously. The microprocessor based system, produces an alphanumeric printout of any power disturbance while storing all information in memory. **Consultronics Inc,** 26 Just Rd, Fairfield, NJ 07006.
Circle 228 on Inquiry Card

PORTABLE, PROGRAMMABLE SIGNAL ANALYZER

ALN 4040 captures ultrasonic and other signals at software selectable sampling rates up to 20 MHz. In nondestructive evaluation of materials, the high speed data and signal analyzer is used in conjunction with an ultrasonic transducer and pulser/receiver or an eddy current signal source. The programmable device analyzes NDE waveforms at the same time signal acquisition is occurring. Signal analysis programs which can filter and interpret NDE waveforms are supplied as preprogrammed memory modules that plug into the printed circuit cards. **Adaptronics, Inc,** 1750 Old Meadow Rd, McLean, VA 22102.
Circle 229 on Inquiry Card

LOGIC TEST PROBE



Bar-Graf combines functions of digital multimeter, signal generator, and oscilloscope in handheld test instrument; it features a 10-segment display with no settling time, internal dc-dc converter, and reverse and overvoltage protection. Pulse amplitudes as short as 300 ns can be detected and ac and dc voltages are displayed with 5% accuracy. Active rectifier measures positive and negative with equal precision and indicates when measuring negative. Alternating voltages are displayed as peak values with illuminated polarity and pulse. **Amcorp Inc,** 15031 Parkway Loop, Tustin, CA 92680.
Circle 230 on Inquiry Card

The new Spectra-Strip 817 is the IDC D-subminiature connector for those of you who've become disenchanted with D-Sub's.

With our D-Sub, you can mass terminate your flat cables without separating each and every strand. Without stocking up on weird-pitched cable. Without a mechanical kluge tacked onto the back of the connector to go from .054-pitch pins to .050-pitch cable.

It terminates our Twist 'N' Flat,® 3C™ Color Coded and that great old standby Spectra-Zip™ with no fuss, no hassle.

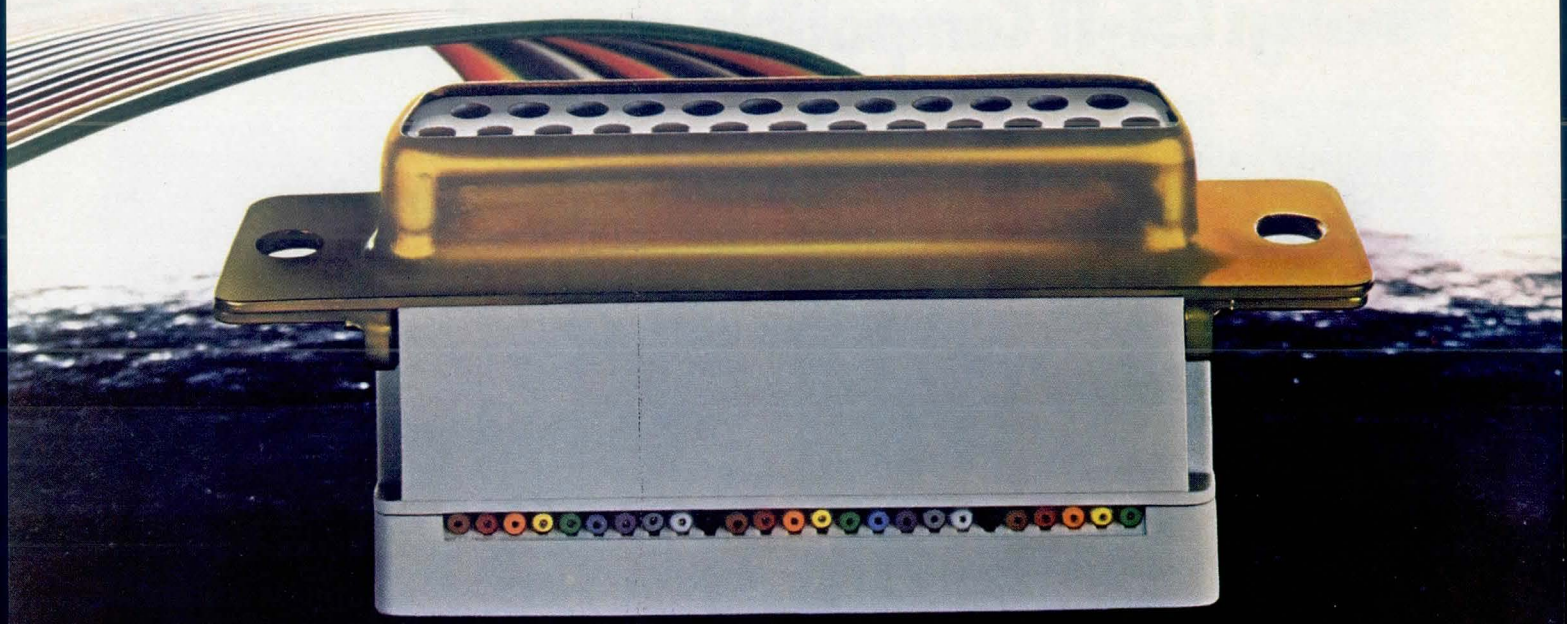
And only the 817 comes with a metal shell so that it's *fully* intermateable and intermountable with any of the other real D-sub's.

If that sounds like the way to build a D-Sub, call your nearest Spectra-Strip distributor. He can also tell you about what we've got for you in our other IDC connectors, flat cable and assemblies.

They're simply superb.

SPECTRA·STRIP

When you're down to the wire.



D-Suberior.

Allied Chemical

Spectra-Strip: 7100 Lampson Avenue, Garden Grove, CA 92642. (714) 892-3361
720 Sherman Avenue, Hamden, CT 06514. (203) 281-3200

In Europe: Spectra-Strip, Ltd.
Romsey, Hampshire, England (0794) 517575

CIRCLE 137 ON INQUIRY CARD

Add in Reliability. Then Relax.

Our LSI-11* compatible memory systems come with built-in ECC (Error Checking and Correction) circuitry. So you don't have to worry about expensive service calls, or strained relations with customers. Our 2,500 ECC systems in the field have a proven MTBF *in excess of 15 years.*

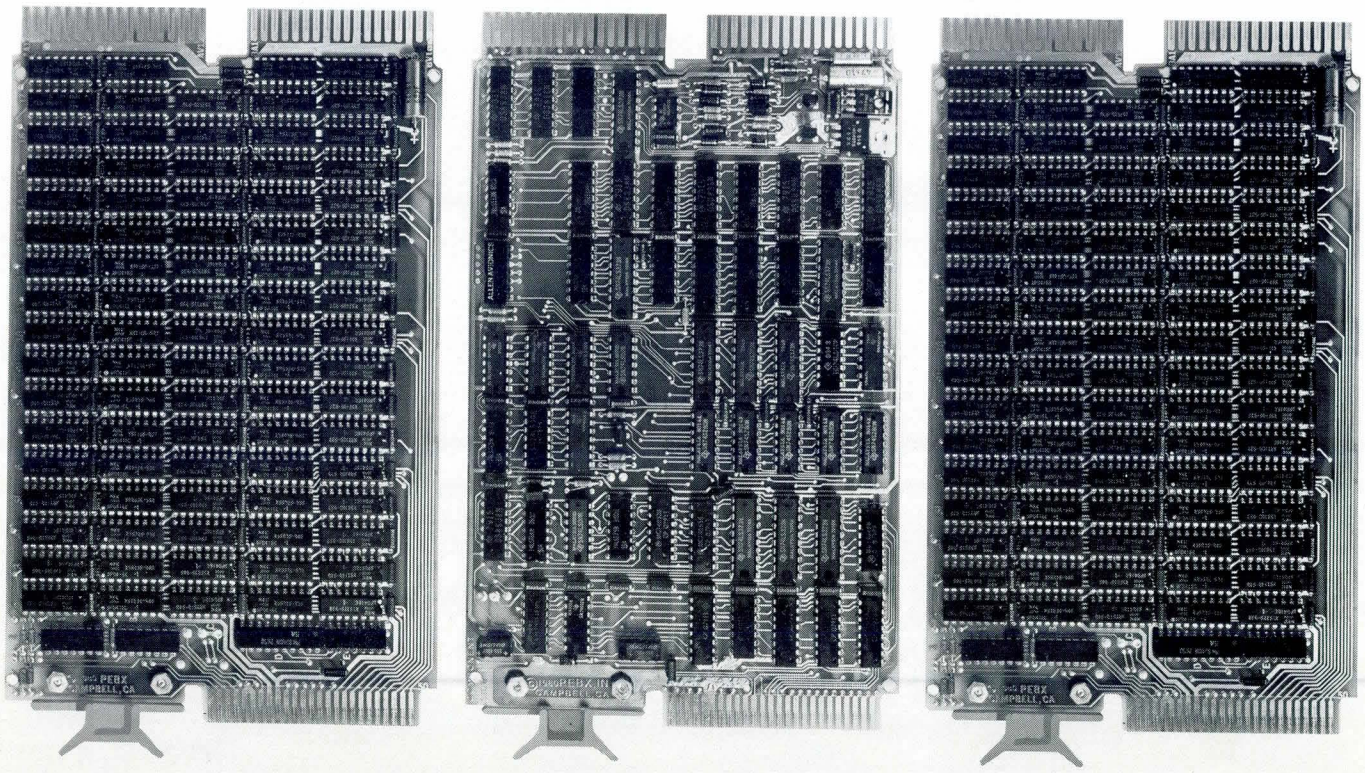
PEBX is the first to protect your LSI-11 system from failing RAMs and those random alpha particle crashes. We've also made protection from power outages as easy as hooking up a battery.

We'll give you from 32 to 256K bytes of error-correcting memory that takes care of all single-bit errors. Plus a display that points to any erring RAM, allowing *preventive* maintenance rather than finger-pointing after a system crash.

So if you're an OEM and you don't want to worry about costly service calls, find out about our add-in reliability and relax. *Contact PEBX toll-free today at (800) 538-3112, (in California (408) 866-7838), for full information on how you can get the best LSI-11 compatible memories available today.*

PEBX
501 Vandell Way
Campbell, CA 95008
(408) 866-7838

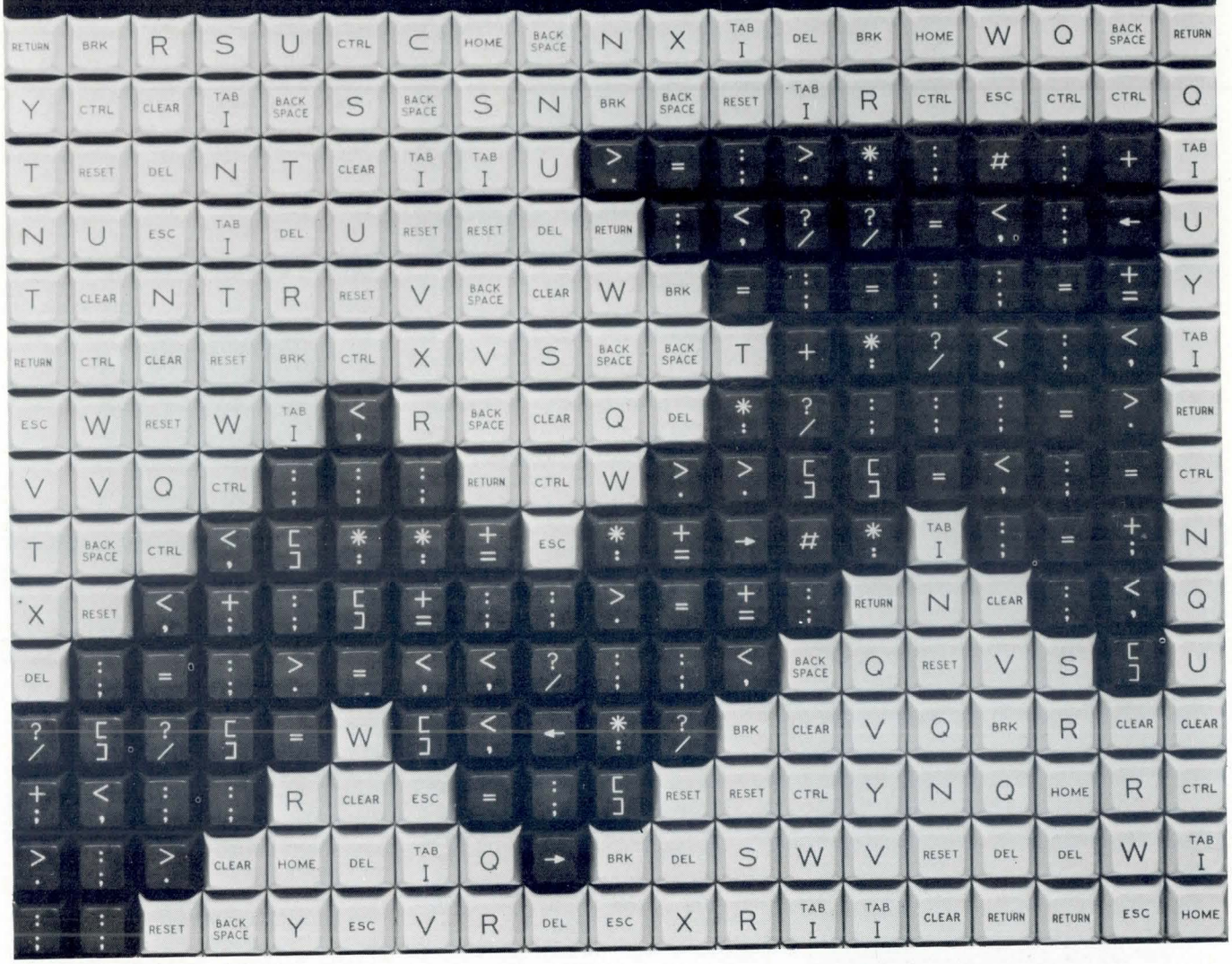
Finally: LSI-11 Compatible memories with ECC.



*LSI-11 is a registered trademark of Digital Equipment Corporation.

CIRCLE 169 ON INQUIRY CARD

KEYS TO PRODUCTIVITY



If you plan, make, use, or buy computer systems or services, you can't afford to miss the upcoming **National Computer Conference,** McCormick Place, Chicago, May 4-7.

The theme of this year's conference is "Keys to Productivity", how to use computers and computer services to help increase output and control costs.

Come see the latest in new equipment and money-saving techniques at over 300 exhibits. Take your pick of over 100 technical sessions and 21 Professional Development Seminars. Enjoy the Personal Computing Festival, now a part of the main conference.

Save time. Save money. Pre-register now for the most dynamic NCC ever. You can:

- Avoid long registration lines
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For Conference Information, call or write **National Computer Conference c/o AFIPS, P.O. Box 9658, 1815 N. Lynn Street, Arlington, VA 22209, (703) 558-3610.**

For discount air fares, airline reservations, hotel and show information, or to pre-register, call toll-free (800) 556-6882.

NCC '81

CIRCLE 161 ON INQUIRY CARD

The O.E.M. Micro-Disc

It looks like all the others because, for a great many applications, it needs very little modification. In fact, many of our O.E.M customers are quite impressed with how quickly and economically we can customize these data recorders to meet their exact requirements.

However, many others find the standard, off-the-shelf Micro-Discs are perfect for their needs, with no modification at all. It's not so surprising when you consider all these standard features:

- Microprocessor control
- String and global search
- Automatic file directory and freespace count
- Dual RS-232 ports
- Variable file lengths
- Powerful text editor
- Rack mount or desktop
- Disc repack feature
- 110 to 9600 Baud, switch selectable
- 200 KBytes per diskette

Read-after-write error checking option

If you need super secure data integrity, our optional Read-after-write error checking feature will double-check every entry to ensure that data recorded is identical to data entered.

The O.E.M. Micro-Disc— It's worth a closer look

Dependable, versatile Micro-Discs. You'll be surprised how easily they fit into your designs. For complete details, write or call today:

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Rochester, NY 14623
(716) 334-9640

PRODUCTS

DATA TERMINALS

DATA GENERAL COMPATIBLE CRT TERMINAL

Sprinter replaces Dasher CRT models 6052 (D1), 6503 (D2), D100, and D200. It features a function key that converts the top row of keys to function keys that duplicate all 4 modes of the D200 and CRT's 15 function keys, full upper/lowercase keyboard, separate numeric keypad with cursor controls, and a half-intensity screen attribute. Print screen, green screen, and custom keyboard features are available as options. **Computer Enhancement Corp,** 3189-E Airway Ave, Costa Mesa, CA 92626.
Circle 231 on Inquiry Card

HANDHELD INPUT TERMINAL

MICROFIN records, stores, and verifies information before transmitting it by telephone to a computer for processing. The system allows application programs to be loaded into terminals by phone line, using a secure communications protocol, thereby eliminating logistical problems involved in returning terminals to the manufacturer each time an application program is altered. The standard, full-alphanumeric keyboard combined with advanced software is suitable for most applications. **Microfin Systems Ltd,** Winslade House, Egham Hill, Egham, Surrey TW20 OAZ, England.

Circle 232 on Inquiry Card

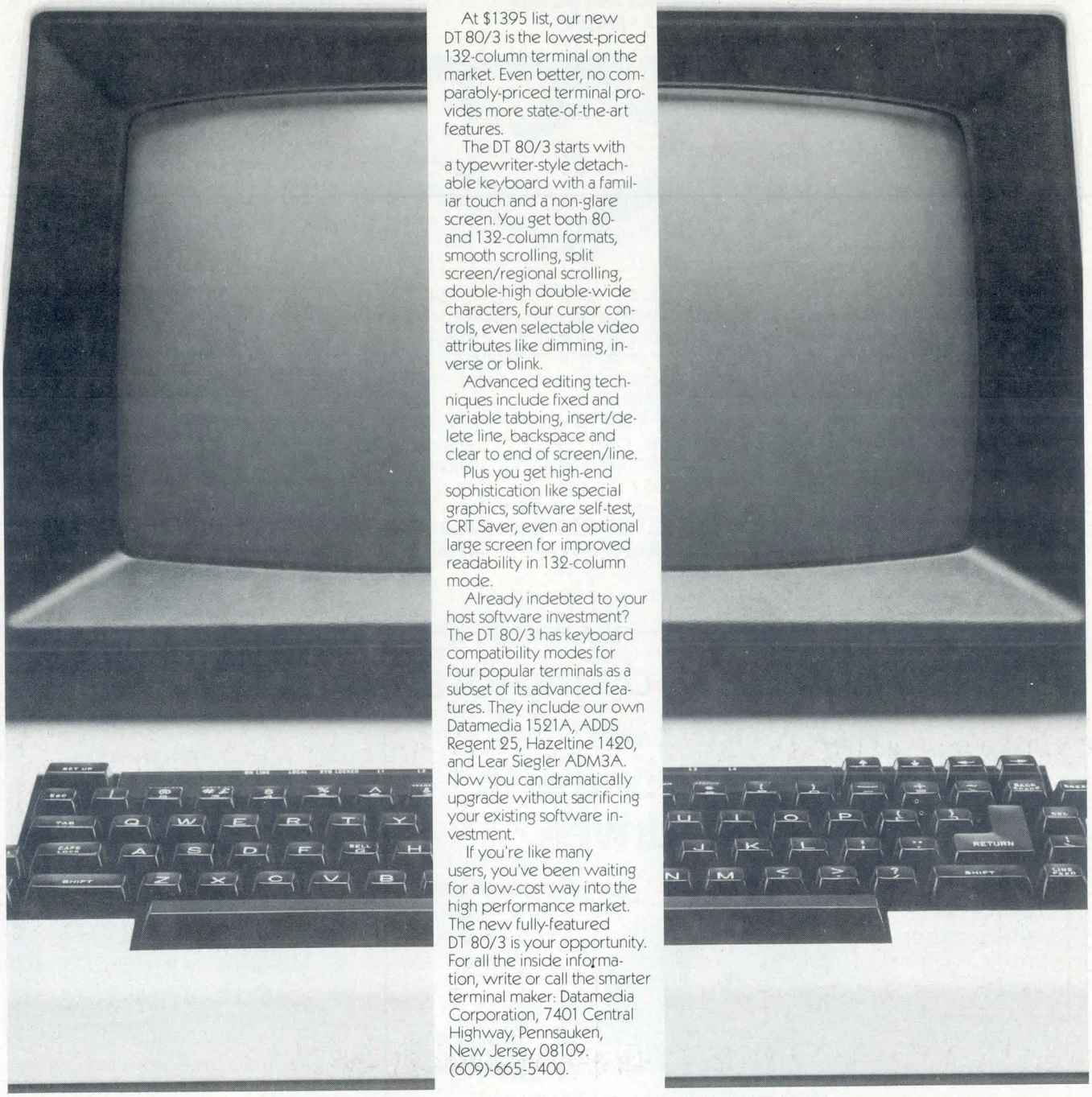
132-COLUMN MONITOR

VR-800L15 displays an 800 x 1200 noninterlaced raster using a 15" (38-cm) CRT and generates a 132-char x 66-line page of upper and lowercase alphanumerics. 65-MHz video bandwidth and 50-kHz scan rate produce clearly defined 8-mil pixels, and the entire screen is refreshed at 60 frames/s for a flicker-free image. Std phosphor is P-104; others are available. **Moniterm Corp,** 250 N Central Ave, Wayzata, MN 55391.
Circle 233 on Inquiry Card

EDITING DISPLAY TERMINAL

Offering a 15" (38-cm) nonglare screen, large characters, 80- or 132-col format, 4 pages of memory, split screen, soft keys, high speed communications, and English language prompts, 132/15 is a smart editing terminal. Screen labeled soft keys make more than 100 functions—some user programmable—accessible to the operator. English (or other language) prompts lead the operator through setup and operation modes. Features such as bidirectional, smooth or jump scroll, horizontal scroll, split screen, communications speeds to 19,200 baud, 4 pages of display memory, and fully displayed status line, adapt the unit for most applications. CRT screen displays total of 24 data lines at 80 or 132 char each; lines 26 and 27 serve as status indicators and soft key legends. Characters are formed by a 7 x 11 pattern in an 8 x 14 dot matrix. Graphics characters are provided in addition to ASCII character set. Horizontal scrolling prevents loss of columns 81 to 132 when changing from 132 char to 80. Visual attributes include underline, blink, reverse video, bold, double height, and double width. Transmission may be by character, line, partial page, or whole page. **Tab Products Co, Electronic Office Products,** 1451 California Ave, Palo Alto, CA 94304. Circle 234 on Inquiry Card

We've just opened up the 132-column terminal market.



At $1395 list, our new DT 80/3 is the lowest-priced 132-column terminal on the market. Even better, no comparably-priced terminal provides more state-of-the-art features.

The DT 80/3 starts with a typewriter-style detachable keyboard with a familiar touch and a non-glare screen. You get both 80- and 132-column formats, smooth scrolling, split screen/regional scrolling, double-high double-wide characters, four cursor controls, even selectable video attributes like dimming, inverse or blink.

Advanced editing techniques include fixed and variable tabbing, insert/delete line, backspace and clear to end of screen/line.

Plus you get high-end sophistication like special graphics, software self-test, CRT Saver, even an optional large screen for improved readability in 132-column mode.

Already indebted to your host software investment? The DT 80/3 has keyboard compatibility modes for four popular terminals as a subset of its advanced features. They include our own Datamedia 1521A, ADDS Regent 25, Hazeltine 1420, and Lear Siegler ADM3A. Now you can dramatically upgrade without sacrificing your existing software investment.

If you're like many users, you've been waiting for a low-cost way into the high performance market. The new fully-featured DT 80/3 is your opportunity. For all the inside information, write or call the smarter terminal maker: Datamedia Corporation, 7401 Central Highway, Pennsauken, New Jersey 08109. (609)-665-5400.

Tell me more about the software-saving

DT80/3

- ☐ Please send product information.
- ☐ Please have your representative call to arrange a demonstration.

Name _____

Title/Dept. _____

Company _____

Street _____

City _____ State _____

Zip _____ Telephone _____

I plan to buy _____ terminals this year.

DATAMEDIA

From the smarter terminal maker.

CIRCLE 167 ON INQUIRY CARD

PRINTERS/PLOTTERS

CRT EMULATORS WITH PRINTER OPTIONS

In addition to complete emulation of Dataspeed model 40s, terminals can be upgraded to various communications applications and customized protocols with only a change in firmware. Capabilities include entering, displaying, modifying, printing, and sending and receiving messages in a dial-up or private line communication system. Models 40/1 and 40/2 are essentially dial-up CRTs with printer option and speed up to 1200 bits/s. The 40/3 is a multipoint private line terminal operating within 8A1 store and forward communications systems. **RCA Service Co,** Cherry Hill, NJ 08358.

Circle 235 on Inquiry Card

COMPACT DOT MATRIX IMPACT PRINTER

E_Z PRINT 21, designed for small screen CRTs, records an exact audit trail of all terminal data and prints it in a 21-col format at a max throughput rate of 42.5 char/s on a std adding machine paper tape. Printer has a buffer that allows input rate of 120 char/s and pathces into std RJ11C modular or RS-232-C interface outlet. Lightweight, desktop printer weighs 7.0 lb (3.1 kg) and measures 10.25 x 7.5 x 3.5" (26.03 x 19.0 x 8.9 cm). **Mepcom International,** 15181 Business Ave, Dallas, TX 75234.

Circle 236 on Inquiry Card

SERIAL MATRIX PRINTER

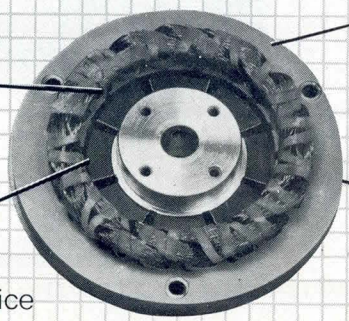
Computer printer offers up to 150-char/s print speed, and up to 136-col output at a competitive price. Designed to provide user convenience, model 500 has few external controls, and can be operated with a minimum of training. Paper loading is simple, and up to 6 copies (original plus 5 carbons) can be produced on either continuous roll or fanfold paper. Paper feeds from either front or bottom and exits at the top rear, reducing forward noise transmission. The adjustable formfeed tractor can handle paper widths from 1.5 to 15" (3.8 to 40 cm). A 9-wire ballisticc printhead forms a 9 x 9 dot matrix capable of producing a range of characters under software control. Standard ASCII 96-char set is stored in printer memory. An alternate set can also be stored there and selected on a line by line basis. Printing format can be selected for 10, 13.6, or 16.5 char/in (3.9, 5.3, or 6.5/cm) and either 6 or 8 lines/in (2.3 or 3.1/cm). Up to 136 char can be printed on a line at 10/in. Double-wide and double density printing is also possible. **Infoscribe, Inc,** 2730 S Harbor Blvd, Santa Ana, CA 92704.

Circle 237 on Inquiry Card

Clifton brushless dc motors work hard for more precise control in Winchester drives.

Special 15-slot configuration for low cogging

8 Ceramic magnets for dependable service



Compact size Easier packaging; better air flow

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Plus, you get:
• Better speed control • Fewer moving parts for better reliability • No arcing—no brush dust • Optional control electronics package • Performance customized to meet your needs

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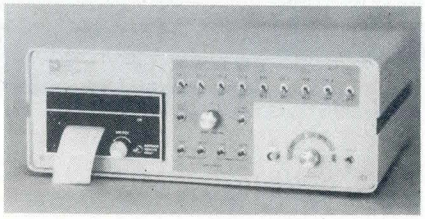
...We make it happen with motors

CP1055A

DATA TEST SET PRINTER



Designed to operate with the WECo 1ARDT (Radio Digital Terminal) and 914B data test sets equipped with the company's model 25 full-duplex long word converter kit or model 15 full-duplex adapter kit, the 2910 printer incorporates a quiet, thermal print head. It can be used online to obtain a record of failures of critical signals in the various data interfaces under test or offline for a record of data errors, block errors, and failure of EIA interface signals. **International Data Sciences, Inc,** 7 Wellington Rd, Lincoln, RI 02865.

Circle 238 on Inquiry Card

A Brilliant New Graphics Terminal from Genisco

Raster brilliance, contrast and erasability. Z-8001 intelligence plus programmability. All in a desk top, high resolution (1024 x 792), monochrome, graphics terminal ticketed at a low $10,000.*

Genisco's G-1000 is the low cost graphics terminal you've been holding your purchase order for. It is the first direct raster replacement for the Tektronix 4014-1** terminal—plug to plug and software compatible. But, at the same time, the on-board Z-8001 microprocessor plus 16K words each of RAM and PROM let you develop your own programs at your pace while your system is up and running on existing software (like PLOT-10).

Because the G-1000 is a bit map raster scan device it can do things a storage tube can't approach—like provide easy viewing in normal room light, and allow erasure of any portion of the screen without altering or redrawing the rest of the display. Genisco has equipped the G-1000 with all the quality features—60Hz noninterlaced refresh for flicker free viewing, a large 19 inch display, a detachable keyboard with cursor joystick. And, an optional alphanumeric overlay eliminates the need to use a second terminal. The unit supports a selection of I/O equipment including graph tablet and hard copy devices. With all that and the Z-8001 intelligence, the list of future capabilities is virtually open-ended.

Take a look at Genisco's new G-1000—the 4014-1 replacement and a whole lot more.

Call or write for more information to Genisco Computers Corporation, 3545 Cadillac Avenue, Costa Mesa, California 92626. (714) 556-4916.

*Price varies according to quantity.
**Trademark of Tektronix
Graphics software from ISSCO Graphics.

Genisco

THE COMPETITION IS GREEN WITH ENVY

CIRCLE 117 ON INQUIRY CARD

COMPARE PRINTER TERMINALS AND BE CONVINCED

After you compare* features and performance... then look at price. With the Digi-Data Model 2516 KSR printer terminal, you get more value at 16 to 30% lower cost.**

For that Receive Only application, our 2511 RO provides similar advantages. And once your Series 2510 is installed, you have the reliability of fewer components with no cooling fan required... and the serviceability of a single board controller.

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(301) 498-0200

...First In Value

*Specifications and pricing obtained from vendor literature for comparably equipped units.

**Substantial OEM quantity discounts available.

Printing Terminal VALUE COMPARISON

	DIGI-DATA 2516	TI 820	Tally T1612	HP 2635B
SPEED [Characters/sec]	150-200	150	160	180
SIZE Width	21.9"	26.0"	25.5"	25.2"
SIZE Depth	18.5"	21.0"	27.0"	23.0"
SIZE Height	8.5"	8.2"	8.5"	8.5"
WEIGHT [lbs]	39	40	69	56
Maximum BAUDRATE	19200	9600	9600	9600
EXTENDED BUFFER CAPABILITY	Yes	No	Yes	No
PRICE	$2150.	$2545.	$2605.	$3950.

DIGI-DATA CORPORATION
...First in Value!

CIRCLE 118 ON INQUIRY CARD

The new data comm tester that obsoletes all others.

ARC's INTERVIEW® 4500 Interactive Test System.

Now a total solution to problems encountered in data communications networks. ARC's new INTERVIEW 4500 Interactive Test System. Featuring a new concept in portable test equipment design that simplifies diagnostics of data comm problems and reduces the most complex testing to a few simple operations.

Three units in one. The 4500 is an emulator, programmable monitor and high speed bulk recorder. Fully emulates CPU, terminal and node. And simplifies network performance measurements.

Special capabilities to emulate packet protocols and SNA. Seven codes are standard.

The first graphic display that guides the operator in entering timing relationships between data and interface leads.

Self documented tapes allow user to build library of diagnostic tests. Unit records data and all test parameters, providing a record of system problems with the test that found the problem.

Selective recording of specific terminal, controller and logical channel eliminates time spent reviewing unrelated data. Reliable 72 Kbps recording is provided by a one megabit high speed bulk memory (optional).

Easy to understand code converted keyboard and self-teaching menus dramatically reduce training time.

Easiest to use interactive tester. Unique triggers automatically locate problems by simultaneously looking for up to 16 test conditions. Significantly reducing time required locating problems in the network. Developing a test is no more complicated than responding to a few simple prompts.

If you need interactive capability, your best choice is the 4500. Or you can have monitor capability now with the 3500, and convert it later to a fully interactive unit.

Call us or our representative today.

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Teleproducts Division
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Memory
- Extensive Family
  - EPROM/RAM
  - CMOS/Battery Backup
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  - Bank Switched

Digital I/O
- Low Cost I/O
  - Isolated/Non-Isolated
  - Up to 96 Channels/Module
- Intelligent I/O
  - Automatic Input Scan
  - Stepper Motor Control
  - Event Count
  - High Level/TTL
  - Isolated/Non-Isolated
  - Up to 64 Channels/Module

Analog I/O
- 12/14 Bit Resolution
- Differential/Single-Ended
- Unipolar/Bipolar
- 250V CMV
- Intelligent
  - Programmable Sampling Rate
  - Transducer Compensation
  - Linearization
- ISA – S50.1

Communications
- Low Cost
  - Serial to 9600 Baud
  - 4 Channels/Module
  - RS-232 / 20 mA
- Intelligent
  - Serial to 800K Baud
  - Pre-Programmed/User-Programmable
  - Async/Byte Sync/Bit Sync
  - IBM Bisync (3270, 2780, 3780)
  - IEEE 488-78 (GPIB)
  - 4 Channels/Module
  - DMA
- Level Converters
  - RS-232/RS-422/RS-423/20 mA
  - Fiber Optics Family
  - Coax/Fiber Optics Tap

Accessories
- Power Supplies
- Card Cages
- Cables
- XYCOAT - Module Sealant
- XYLUBE - Corrosion Preventative

Minicomputer Power in a Microcomputer

From the hardhat computer people, the new 1868+A, the fastest Z8000 module on the market — faster than most minicomputers, and tougher than the harshest industrial environment.

Based on the Z8001, the segmented version of the powerful new Zilog Z8000, the 1868+A is a 16-bit master/slave microcomputer module with enough speed and flexibility to outperform most minicomputers.

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I/O: Two-channel serial I/O (Zilog SIO) communications up to 800 kilobaud. Additional memory-mapped I/O installed in backplane.

Use the 1868+A as a stand-alone microcomputer or as a master or slave in a multiprocessor array in any industrial environment. As part of Xycom's 180+ line of modular components, the 1868+A is hardhat tough, built to work wherever it's needed.

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Like all of Xycom's full line of modular products, the 1868+A is fully supported by our Industrial Software System, featuring:
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■ Industrial Basic ■ Assemblers

We make the Industrial Grade

Xycom recently introduced the term "Industrial Grade" to the computer industry, because unprecedented ruggedness and reliability are what Xycom products are all about. We began, over a decade ago, producing computers designed to work on the line, in the plant, and in other demanding industrial environments. Since then, the state-of-the-art has progressed dramatically, mostly as a result of Xycom's research, development, and years of experience in the heat, cold, dust, vibration, and corrosive atmosphere of more than 20,000 installations worldwide.

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The Hardhat Computer People

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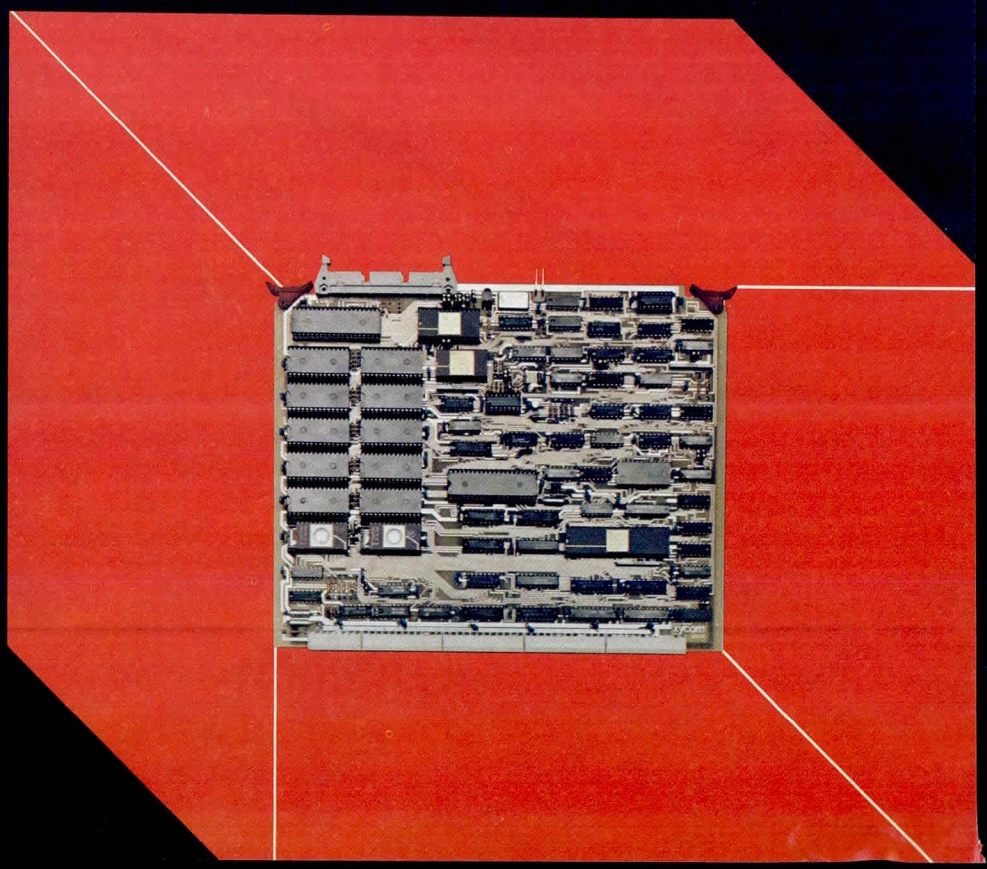


CIRCLE 120 ON INQUIRY CARD

POWER SOURCES AND REGULATORS

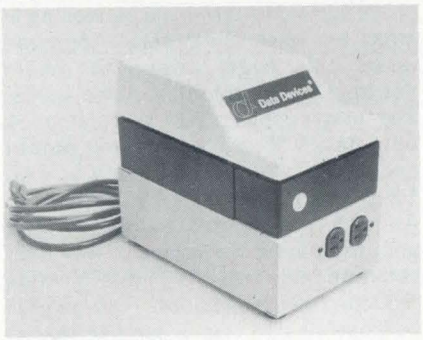
5-CHANNEL MULTIPLE-OUTPUT SWITCHER

PM2679 provides 5 completely isolated outputs, with max power rating of 850 W. Input range is 92 to 138 or 184 to 250 Vac, and unit will regulate through line DIPs to 80 or 160 Vrms. Switcher provides regulated outputs of 2 to 60 Vdc; output power will hold for a min of 30 ms after input power failure. Unit measures 5 x 8 x 15" (12.7 x 20.3 x 38.1 cm), weighs 27 lb (12.3 kg), and features overload, short circuit, and reverse voltage protection, remote sense, and automatic overtemp and overvoltage shutdown. **Pioneer Magnetics, Inc,** 1745 Berkeley St, Santa Monica, CA 90404.

Circle 239 on Inquiry Card

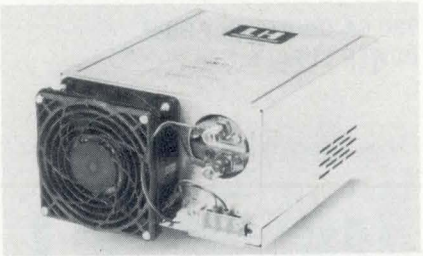
PORTABLE POWER CONDITIONERS

Datapower eliminates need for dedicated power line for computers and reduces equipment failures related to power fluctuations. Input voltages as low as 25% below normal are regulated immediately to within ±7% of nominal. The conditioners, available in seven 50- and 60-Hz models, are UL listed and unconditionally guaranteed. **Data Devices International, Inc,** 20235 Bahama St, Chatsworth, CA 91311.



Circle 240 on Inquiry Card

SINGLE-OUTPUT SWITCHERS



To protect against brownouts, both Super-MITE SM71 series 750-W and SM11 series 1-kW switchers accept ac inputs from 85 to 130 Vac, and from 166 to 260 Vac, at 47 to 63 Hz. Std features include power fail detection signal, remote sense, remote on/off circuit, plus monitored parallel operation and capability. Emi filter that meets FCC-A and VDE-0871 specifications is optional. Units measure 5 x 8 x 11" (13 x 20 x 28 cm), and weigh 15.8 lb (7.1 kg). **LH Research, Inc,** 14402 Franklin Ave, Tustin, CA 92680.

Circle 241 on Inquiry Card

EYECOM II the IMAGE PROCESSING PERIPHERAL

Add this image processing peripheral to your present PDP-11* or LSI-11* to measure variations in image brightness, separate image features, enhance edges and contrast, measure areas of interest, do real time image integration, and real time image differencing.

A basic software package is provided to apply the EyeCom System to your particular problem.

FEATURES:

- **Real Time Digitizing, 640x480x8-bits**
- **Add, Subtract and Convolution of images at video frame rates**
- **Joystick Cursor, 640x480 Resolution**
- **Graphic & Alphanumeric Overlay**
- **Color & Gray Scale Mapping Tables**
- **Terminal or Rack Mount Configuration**

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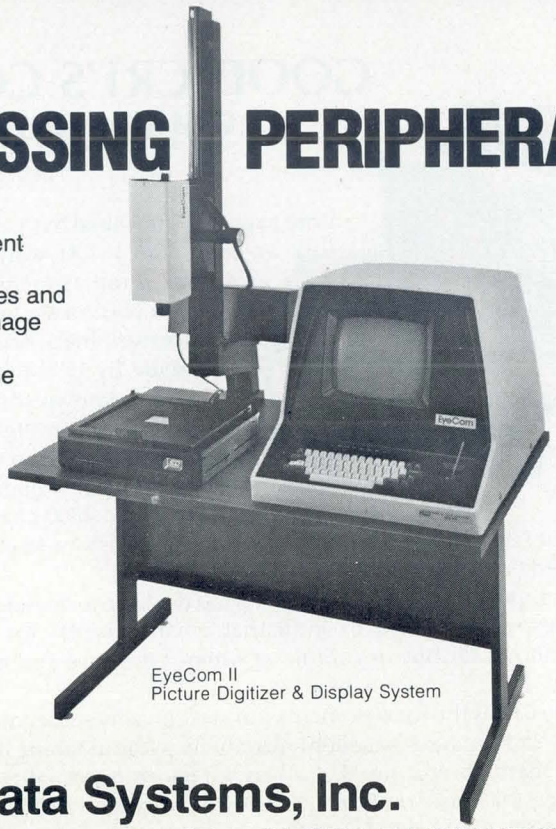

EyeCom II
Picture Digitizer & Display System

Spatial Data Systems, Inc.

P.O. Box 978, 508 So. Fairview Ave., Goleta, CA 93117 • Tel: (805) 967-2383

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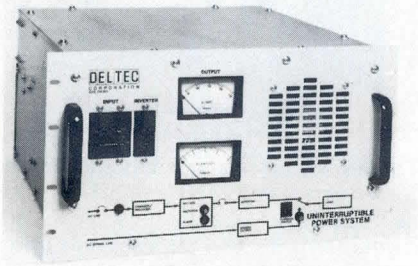
The Image Processing Company

CIRCLE 121 ON INQUIRY CARD

POWER SOURCES AND REGULATORS

700-VA UNINTERRUPTIBLE POWER SUPPLY



Sized to provide standby power for small business computers, PABX, process control, and other microprocessor based equipment, model DSU72 UPS can be supplied with battery power from 5 min to over 4 hours. Front panel indicates operating status, ac voltage, and current levels; contact closures provide full status information to remote monitoring locations. Filtering option allows system to operate in critical rfi/emi environments, and static transfer switch option operates bypass in 1 ms and resets when overload condition decreases. **Gould-Deltec,** 2727 Kurtz St, San Diego, CA 92110.

Circle 242 on Inquiry Card

200-W SWITCHER FOR SMALL BUSINESS SYSTEMS

An open frame design having VDE approvals for use in Europe, the 200-W model XL200-3501 can be used in word processors and terminals as well as in small business computers. Approved under VDE 0730 safety, it meets VDE 0871 (N-12) electrical noise specs. The unit supplies 200-W total on 4 outputs—5-V ±1% primary output and auxiliary outputs of −5 V at 9%, 12 V at 9%, and −12 V at 9%. About 5 times lighter, 5 times smaller, and dissipating 50% less power than conventional units, its high efficiency reduces heat dissipation. The general purpose design has 2 jumper selectable input voltage ranges: 95 to 130 Vac and 190 to 265 Vac at frequencies from 47 to 440 Hz. Output regulation is specified as total, including effects of line power fluctuations and effects of primary output regulation on auxiliary output levels. The 5-V primary output delivers 5 to 25 A at total regulation within ±1% and combined noise and ripple within ±2%. Auxiliary outputs each provide 0.5 to 4 A with combined noise and ripple of ±2%. Minimum output voltage holdup time is 16 ms at max load and nom input voltage. **Boschert, Inc,** 384 Santa Trinita Ave, Sunnyvale, CA 94086.

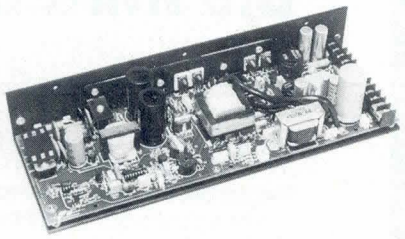
Circle 243 on Inquiry Card

UNINTERRUPTIBLE POWER SYSTEMS

Uninterruptible power system (UPS) rated at 12.5 to 60 kW are available in both 50- and 60-Hz models. Expandable onsite to double their original power rating, units allow users to meet future demands for higher power without removing their current UPS. Expansion kits contain slave inverter and rectifier cabinets controlled by existing UPS units. **LorTec Power Systems, Inc,** 5214 Mills Industrial Pkwy, North Ridgeville, OH 44035.

Circle 244 on Inquiry Card

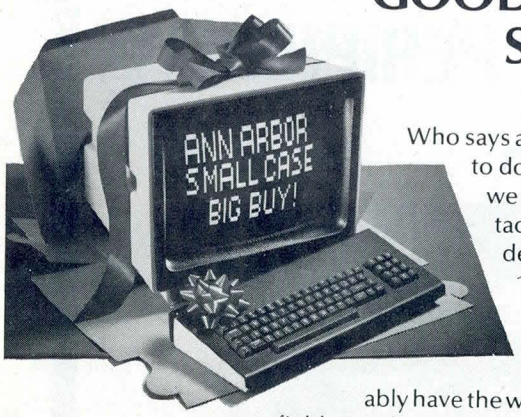
150-W OPEN FRAME SWITCHERS



Triple- and quad-output capability, with post-regulated auxiliary outputs in Boschert compatible outline configuration, is provided by NT150 and NQ150 switchers. Features include built-in line filtering, soft start circuitry, 115/230-Vac input capability, LSI control circuitry, and built-in remote sense and overvoltage protection. Ripple and noise is 1% of nominal. Units provide recovery to within 1% of nominal output voltage within 500 μs for a 25% load step. Op temp is 0 to 50 °C, and size is 13.6 x 4.8 x 2.5" (34.5 x 12.1 x 6.3 cm). **National Power Technology,** 2111 Howell Ave, Anaheim, CA 92806.

Circle 245 on Inquiry Card

GOOD CRT'S COME IN SMALL PACKAGES



Who says a CRT terminal has to be big and bulky to do a good job? At Ann Arbor Terminals, we offer a full 15-inch screen *and* detached keyboard as standard on all our desktop terminals. And the case is only 14" wide by 15" high by 13.6" deep. We're known throughout the industry for our high quality and reliability. On top of this, we probably have the widest range of available options in the field. Display formats from 256 to 4800 characters. Foreign language character sets. Special command sets. Custom keyboards. Editing, protected fields and block transmit.

And if your application doesn't lend itself to a desktop terminal, we offer display controllers (especially good in industrial environments) for use with free-standing monitors. Or buy our terminal without the case and mount it in your own console.

So when the CRT is the focal point of your system, why settle for a large case and small screen? You can have excellent readability without taking up a lot of room. And get the features you need. Call us for more information at Ann Arbor Terminals, Inc., 6175 Jackson Road, Ann Arbor, Michigan 48103.
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ANN ARBOR TERMINALS, INC

CIRCLE 122 ON INQUIRY CARD

DEC 11* USERS....

COMPACT, DUAL PURPOSE, 1/2-INCH TAPE DRIVE AND ONE CPU QUAD SLOT TAPE COUPLER... NEW STANDARD FOR IBM/ANSI/DEC COMPATIBLE TAPE SUBSYSTEMS.

HUMAN ENGINEERED . . . SMALL SIZE . . . LOW COST

If you're considering a TM-11, TS-11, TS-03, TJE-16 or TJU-45 magnetic tape subsystem from DEC, then you're probably aware of all of the advantages offered by industry standard 1/2-inch magnetic tape . . . universally interchangeable media and DEC/IBM/ANSI compatible format. Plus its multiplicity of applications . . . data acquisition, file management, computer output microfilm, archival storage and disc backup, etc.

This subsystem gives you all this capability in about 1/3 the rack space required for classic 10-1/2-inch reel machines, without cumbersome manual threading of tape around heads, compliance arms, etc., to load the drive.

And since it's a dual function drive, you get (1) a tape subsystem that's completely DEC RT-11 and RSX-11 and RSTS software compatible in the conventional mode . . . without any modifications (2) a tape subsystem that will run in a high speed "gap on the fly" mode while writing or reading industry standard compatible magnetic tape. This mode permits high speed data acquisition using standard software or Winchester backup using a DILOG supplied or customer written software routine.

Here are a few features making this drive and intelligent coupler an exceptional addition or subsystem replacement for your PDP-11 or LSI-11.

CIPHER F880 DUAL PURPOSE 1/2-INCH TAPE DRIVE—25 ips conventional or 100 ips streaming mode operation • fits the same space as TS-03 (8.75″) • automatically loads 7, 8-1/2 and 10-1/2-inch reels, simplifying and speeding operator loading and operation • 46 M Bytes unformatted storage • 1600 bpi PE compatibility • built-in microdiagnostics.

DILOG uP MAGNETIC TAPE COUPLER • requires single quad slot in either PDP-11 or LSI-11 • emulates TM-11 • handles up to 8 drives in conventional or streaming modes • selectable IBM or DEC byte packing • requires only 3.5 amps from CPU • automatic self-test/data protect and status indicators • FIFO buffer for DMA latency.

Compared to conventional, bulky, hard-to-load tape subsystems, you can achieve up to 60% cost savings. Plus they're field proven and available now.

For data send coupon below. Or for instant info, phone direct (714) 534-6911.

*DEC, LSI-11, PDP-11, TM-11, RT-11/RSX-11/RSTS Trademarks of Digital Equipment Corp.

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☐ Please send data on Dual Purpose Tape Subsystem
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Company_____ Dept./Div._____
Address_____
City_____ State_____ Zip_____

CIRCLE 133 ON INQUIRY CARD

POWER SOURCES AND REGULATORS

TRIPLE-OUTPUT POWER SUPPLIES

Two triple-output supplies have total output of approx 9.5 W. They provide outputs of 5 Vdc at 1000 mA with ±12 Vdc at 150 mA, and 5 Vdc at 1000 mA with ±15 Vdc at 150 mA. Overload protection is provided on the 5-V outputs. Packaging is in cases measuring 3.5 x 2.5 x 1.62" (8.9 x 6.4 x 4.1 cm) for PC card mount, or 4.0 x 2.7 x 2.0" (10.2 x 6.9 x 5.1 cm) for chassis mounting. **Power Products, Div of Computer Products, Inc**, 1400 NW 70th St, Fort Lauderdale, FL 33309.

Circle 246 on Inquiry Card

200-W SWITCHING POWER SUPPLY

Triple-output model 20E5/±12 delivers 5 V at 30 A and ±12 or ±15 V at 1 A, and has ac input ranges of 100 to 132 and 200 to 260 Vac. Line and load regulations for 5-V output are 0.2% and 0.3%, respectively; auxiliary outputs line and load regulation are 0.7% and 1%. Ripple and noise for all outputs are limited to 30 mV. Features include overload and reverse polarity protection, overvoltage protection for main inverter, logic inhibit, soft start, remote sensing, and remote sense protection. **Nortel**, 31149 Via Colinas, Bldg 608, Westlake Village, CA 91361.

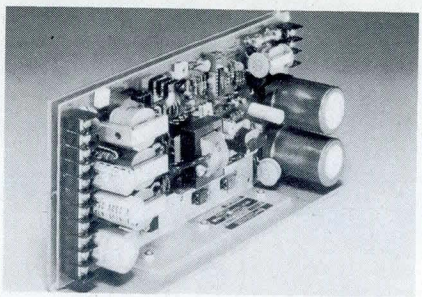
Circle 247 on Inquiry Card

1-kW POWER SUPPLY

SRX 5-200 is a 5-V, 200-A offline switching power supply power density of 2.47 W/in³ (0.15 W/cm³). Efficiency is typically 75% at full load. Housed in an industry standard 5 x 8 x 11" (13 x 20 x 27-cm) case size, the supply incorporates advanced switching technology, conservative design, and modular packaging. Std features include LED indicators, digital interfacing, std overvoltage protection, and external crowbar drive. **Sorensen Co**, 676 Island Pond Rd, Manchester, NH 03103.

Circle 248 on Inquiry Card

150-W OPEN FRAME SWITCHER



MOS series supplies, available in four 150-W models, meet FCC specs for rfi. MOS-150-0512 delivers 5 V at 15 A, −5 V at 1 A, 12 V at 4 A, and −12 V at 3 A. 2412 will deliver 5 V at 15 A, −5 V at 5 A, 12 V at 1.5 A, −12 V at 1.0 A, and 24 V at 3 A with the ability to deliver 6 A peaks. Both are also available in an A version, which will provide 20 A from the 5-V output. Significant features include current limit on all outputs designed to protect user's load as well as the power supply; 115 Vac or 230 Vac is available by changing a jumper. **Todd Products Corp**, 50 Emjay Blvd, Brentwood, NY 11717.

Circle 249 on Inquiry Card

Attn: ECLIPSE/NOVA* users!

Before you graduate to 'Streamer Tape' for disk backup, check out our Model 130 Coupler.

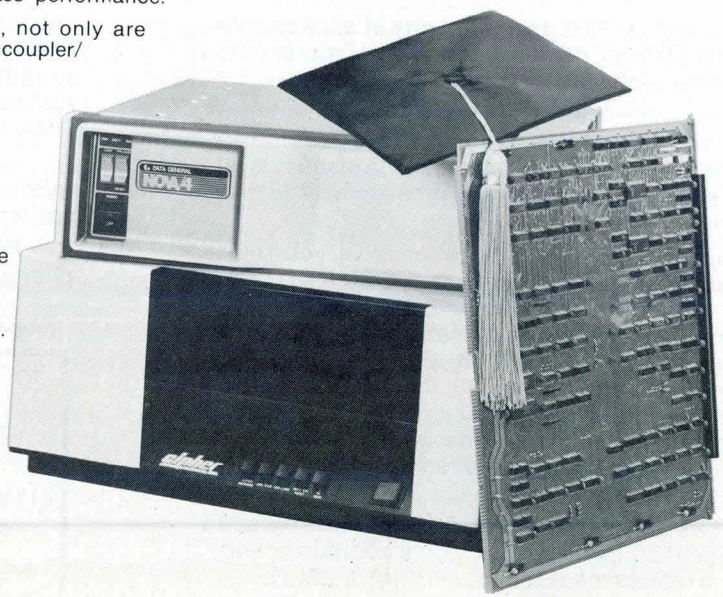
In conjunction with an independent, high-quality streamer unit, Custom Systems' Model 130 Coupler provides economical, 'top-of-the-class' performance.

When compared to DG's streaming tape subsystem, not only are the data rates superior (up to 160 KBS), but the price of the coupler/streamer combination is about $2000 less!

Model 130 Coupler features include:

- True 100 ips streaming!
- Full emulation of Data General 6026 Magnetic Tape Subsystem.
- Microprocessor design to maximize streamer performance.
- Software utilities for optimized disk image or selective load/dump backup.
- Actual backup of 20 Mb disk in under 3 minutes.
- Alternative operation in conventional start/stop mode.
- Compatibility with industry standard NRZI/PE formatted tape drives.
- Two-year warranty.
- $1490 complete with manuals and cables.

Contact us today for a detailed data sheet.



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DUP-11* compatibility—plus! Now it's yours for Q-Bus as well as Unibus with the MLSI-DUPV-11 and MDB DUP-11 synchronous, single line communications interfaces.

In addition to providing functional equivalency and software compatibility with DEC, the quad size MDB DUP-11 and MLSI-DUPV-11 interfaces will accommodate BI-Sync and DDCMP in byte-control and SDLC, ADCCP and HDLC bit-oriented protocols, with programmable character lengths of one to eight bits for BOP and five to eight for BCP. This is performance flexibility never possible before. In addition, the MDB DUP boards feature complete error control including CRC-CCITT preset to O's or 1's, CRC-16 preset to O's or VRC odd or even. For Q-Bus users this hardware error checking saves a lot of computer time and memory over the software checking of other systems.

But that's not all MDB can do. If you need line printer controllers for your DEC, Data General, IBM Series/1, Perkin-Elmer or Hewlett-Packard computer, we've got them for more than 100 computer/printer combinations. We don't just make plain PROM modules—we have modules that let you program EPROM on the board and we have interprocessor links which will maintain high speeds over distances to 3,000 feet. MDB's new multiplexors let you mix up to eight lines of EIA and/or current loop, and our foundation modules require only one card slot.

All MDB interface products are warranteed for one year, most can be delivered in 30 days or less and all are available under GSA Contract #GS-00C-02423.

Now, what can we do for you?

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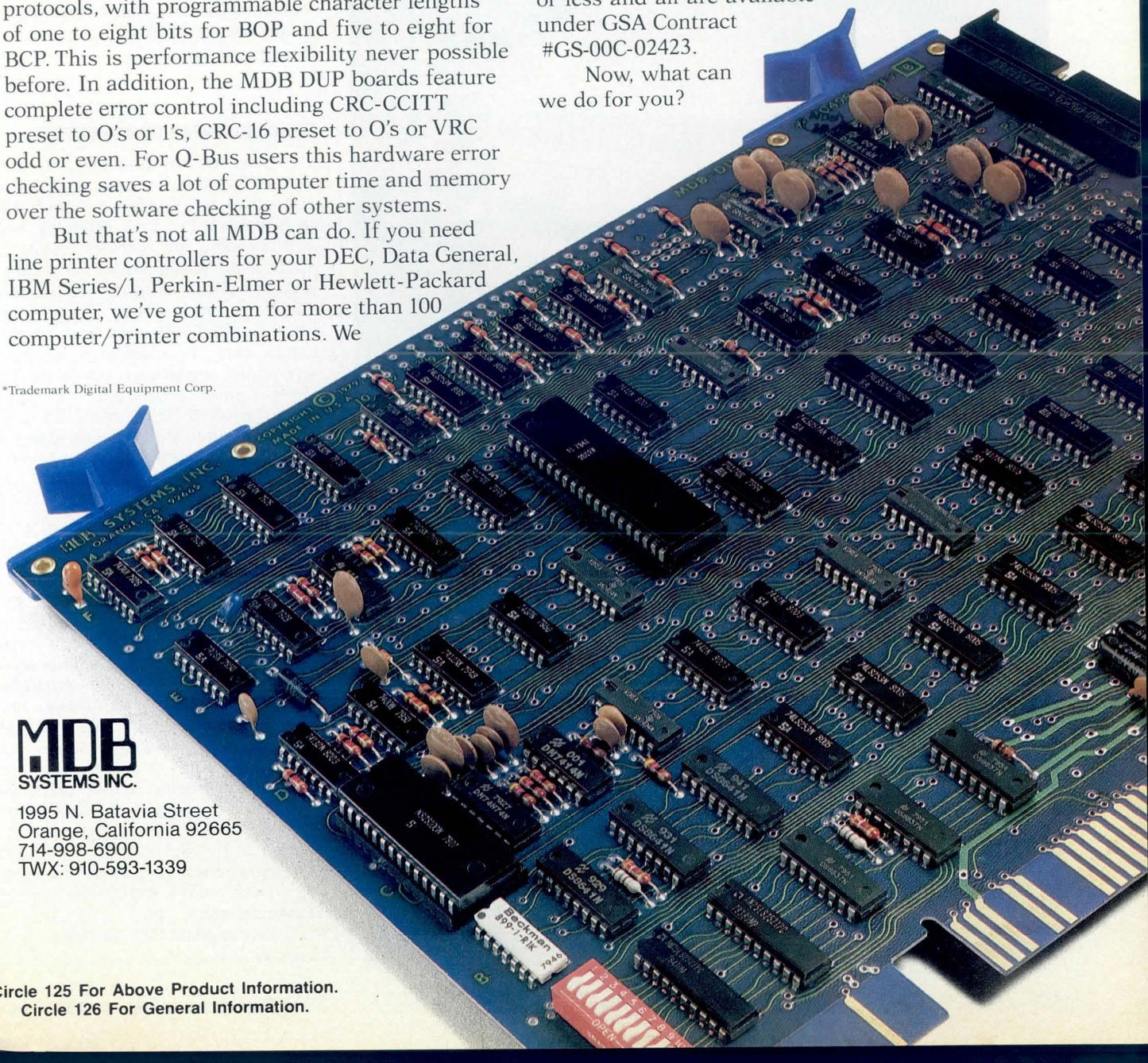

MDB SYSTEMS INC.

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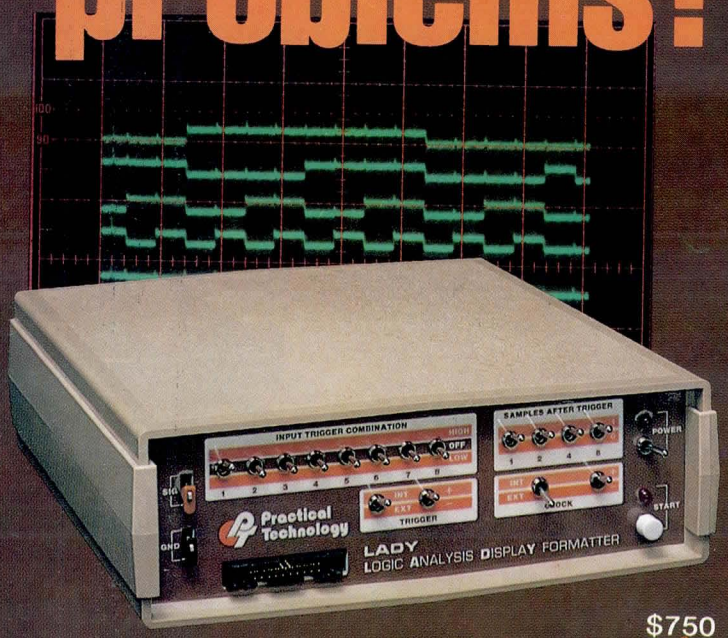
Orange, California 92665
714-998-6900
TWX: 910-593-1339

Circle 125 For Above Product Information.
Circle 126 For General Information.

trouble-shooting problems?



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PRODUCTS

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PC BOARD RIGHT ANGLE LED INDICATORS

Series 5322 incorporates an LED at right angles to the base mounting pins of the assembly. These pins are simply pressed into holes in the PC board to provide precise LED location and height. The indicator incorporates high intensity light output LEDs in red, green or yellow. High dome lens permits max light output over a 90° viewing angle. Typ forward voltages are approx 2 V at 20 mA. Luminous intensity at this current is typ 4 to 5 mcd. **Industrial Devices, Inc,** 7 Hudson Ave, Edgewater, NJ 07020.

Circle 250 on Inquiry Card

SYNCHRO-LINEAR DC CONVERTER

Designed for PCB mounting, series of converter modules has accuracy of ±6 min of arc. The 2.6 x 3.1 x 0.82" (6.6 x 7.9 x 2.1-cm) modules convert synchro or resolver inputs of 11.8 or 90 V 400 Hz, or 90 V 60 Hz into ±10 Vdc outputs representing 180° of input angle. The devices have isolated reference and synchro inputs and are insensitive to input amplitude variations. Outputs are short circuit protected. Op temp ranges are 0 to 70 °C and −55 to 85 °C. **Computer Conversions Corp**, 6 Dunton Ct, E Northport, NY 11731.

Circle 251 on Inquiry Card

SINGLE-MODULE 2-SPEED S-D CONVERTER

Single module accepts 2 synchro or resolver inputs from a 2-speed system and combines them into a digital word of high resolution and high accuracy. Design maintains accuracy and nonambiguous output even though gear errors or backlash reach 5°. A self-test feature, 2-speed ratio formats, and velocity output units are available. Features include 16-bit resolution; ±20-arc seconds accuracy; 9:1, 18:1, 32:1, 36:1, and 64:1 gear ratios; and 1440°/s tracking rate for 400-Hz units. **Transmagnetics, Inc,** 210 Adams Blvd, Farmingdale, NY 11735.

Circle 252 on Inquiry Card

VISACOM/23 GRAPHIC/IMAGE SYSTEM. SUPER CAPABILITIES, SUPER FAST, SUPER PRICE.

DeAnza's VISACOM/23 now offers you features and capabilities previously only found in large-scale systems. Features like proven and superior image and graphic display software, advanced computing capabilities and proven operating systems software.

All at a very reasonable price.

The VISACOM/23 and the DeAnza Library of Image Processing Software (LIPS) allows you to perform work you only thought possible on the large, expensive systems.

Graphic and display efforts like convolutions, rotations, classification, amplifications, addition, subtraction, image and graphic zoom and scroll as well as much more.

And, the VISACOM/23 incorporates the powerful LSI-11/23 computer so you perform graphic and image processing more easily and much faster.

It allows you to do more work in less time.

VISACOM/23 has a full 512K byte memory for dedicated computer operation or image display as well as 128K bytes of dedicated memory outside of the image memory, four independent graphic overlay channels, alphanumeric character generators, color and monochrome transformation units and cursor overlays.

If your graphic and imaging application calls for a system that provides quality, flexibility and added capabilities all in an economical package, find out more about the VISACOM/23 today.

Call or write:

DeAnza Systems Incorporated

CORPORATE HEADQUARTERS: 118 Charcot Avenue, San Jose, CA 95131, (408) 263-7155, TWX: (910) 338-7656
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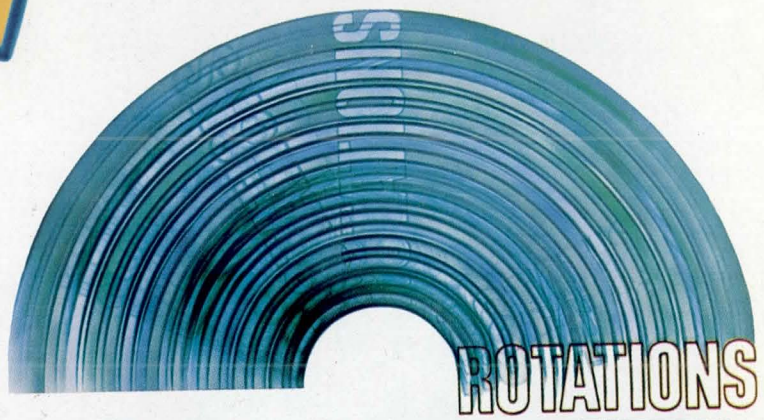

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CIRCLE 129 ON INQUIRY CARD

SUBASSEMBLIES AND CIRCUIT COMPONENTS

INTELLIGENT LIQUID CRYSTAL DISPLAYS

Four versions comprise PCIM 180 series of LCDs: 3½- and 4-digit multiplexed BCD models 180 and 181, and 3½- and 4-digit serial input 182 and 183 that require only clock, data in, and load inputs. Devices use single 5-Vdc supply (3 to 15 V), draw 20 mA, and have 0.5" (1.2-cm) high numerals. They may be cascaded, are CMOS or TTL compatible, and generate all LCD waveforms internally. Op temp is 0 to 50 °C. **Printed Circuits International, Inc**, 1145 Sonora Ct, Sunnyvale, CA 94086.

Circle 253 on Inquiry Card

12-BIT SUCCESSIVE APPROXIMATION ADC

ADC-1202 provides 2-μs conversion time and pin-selectable input voltage range of 0 to 10 V unipolar or ±5 V bipolar. Output coding is straight binary, offset binary, or 2's complement. Gain offset and differential nonlinearity tempcos are specified at ±30, ±15, and ±3 ppm/°C, respectively. Power supply requirements are 15 Vdc ±3% at 80 mA, −15 Vdc ±3% at 20 mA, and 5 Vdc ±5% at 150 mA. **Intech Inc**, 282 Brokaw Rd, Santa Clara, CA 95050.

Circle 254 on Inquiry Card

16-BIT DIGITAL TO SYNCHRO/RESOLVER CONVERTER

With accuracy of ±1 arc-min and scale factor variation of ±0.05%, converter is packaged in a std 36-pin DIP. Reference voltages of 115, 26, or 1.3 V are selected by pin programming, without external resistors. Reference impedance is 200 kΩ. Inputs are double-buffered, and converter is TTL and std or high level CMOS compatible. Parallel binary input can be either a 16-bit word or two 8-bit bytes, providing microprocessor compatibility at both 8- and 16-bit levels. **Natel Engineering Co, Inc**, 8954 Mason Ave, Canoga Park, CA 91306.

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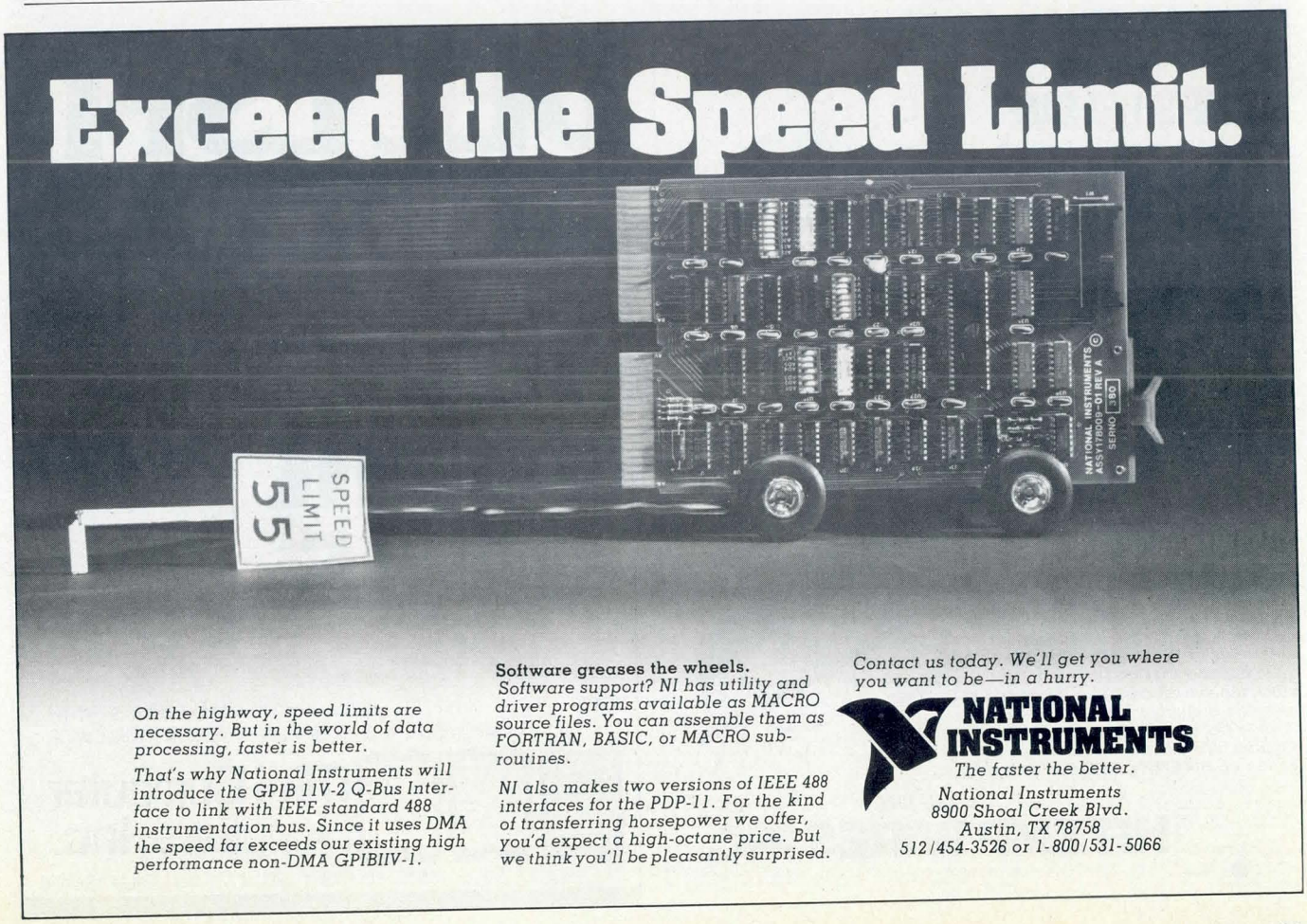
8-BIT A-D CONVERTER

Linearity of 0.0087% is achieved through use of a statistical linearization technique in the ADC-881 8-bit A-D converter. Conversion time is 1.5 μs max, 1.3 μs typ. Device has ±5 V analog input range, offset binary coding, output overrange logic signal, and ±30 ppm/°C max tempco. Unaveraged rms output noise is 0.2% of full scale. Black enameled steel case measures 5 x 3 x 0.375" (12.7 x 7.6 x 0.95 cm) and weighs 6.5 oz (184 g). Device draws 6.6 W at ±15 Vdc and 5 Vdc. Op temp range is 0 to 70 °C. **Datel Intersil**, 11 Cabot Blvd, Mansfield, MA 02048.

Circle 256 on Inquiry Card



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CIRCLE 130 ON INQUIRY CARD

SUBASSEMBLIES AND CIRCUIT COMPONENTS

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High efficiency red in three intensities, and three intensity levels each for std red, yellow, and green, are colors of LED lamps that replace RL-10, GL-11, and YL-12 types. In a T-1¾ package size, they emit a rectangular wedge of light measuring 0.1 x 0.2" (0.2 x 0.5 cm), and can be stacked 10/in (4/cm) in line or 5/in (2/cm) end to end. Luminous intensity with 20-mA current is 0.6 to 3.2 mcd. Max power dissipation at 25 °C is 200 mW. **Litronix, Inc**, 19000 Homestead Rd, Cupertino, CA 95014.

Circle 257 on Inquiry Card

HIGH SPEED THERMAL PRINTHEAD

Onboard BiMOS memory and drive circuitry provide easy interface to microprocessor control and permit printing rates of up to 1600-char lines/min of 5 x 7 text by the SM20100 20-col thermal printhead. Device comes with integral heat sink, thermistor preheater, and connector terminated cable. Heads are stackable for column expansion and are available in preganged arrays of 40, 60, and 80 cols or more. Compact design results from fixed head technology and constant speed paper drive. **Gulton Industries, Inc, Hybrid Microcircuit Dept**, 212 Durham Ave, Metuchen, NJ 08840.

Circle 258 on Inquiry Card

DATA DRIVER MODULES

Model 10910 is programmable over −10 to 10 V range for 10-V pk-pk output signal, and features 2-ns rise and fall time with output swing of 5 V, 12-ns max switching time for enable or disable modes, data repetition rates over 50 MHz, and pulse widths as narrow as 5 ns at 5 V pk-pk. Data are transmitted through coaxial cable, parallel or 50-Ω source terminated. Module includes output inhibit mode, allowing Tri-State® configuration, and accepts std ECL output as input. **Versatile Integrated Modules**, 1283-A Mountain View Alviso Rd, Sunnyvale, CA 94086.

Circle 259 on Inquiry Card

HARD COPY INTERFACE FOR TEKTRONIX COLOR TERMINAL

HC 4027 interface generates full color, plain paper hard copy for the Tektronics 4027 color terminal on the COLORPLOT model C-100. Interface accepts raster format RGB video data from terminal and converts this 3-dot video pixel to a 4-dot copy pixel. Multiple, full color hard copies can be automatically generated by either operator or computer initiated commands. **Trilog, Inc,** 17391 Murphy Ave, Irvine, CA 92714.

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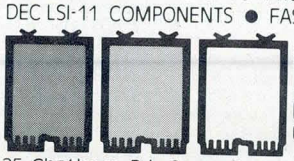

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The new 1421 by Hazeltine:

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CIRCLE 123 ON INQUIRY CARD

COMPUTERS AND COMPUTER SYSTEMS

PROCESS CONTROL COMPUTER SYSTEMS

Mod 3100 systems offer combinations of standalone, multiple, and remote modes of operations. Featuring fully integrated hardware and software, wide capacity range, common software and hardware, distributed intelligence, and evolutionary systems compatibility, the systems can be configured to operate in combination with the company's MOD 3 system for max process management and control. MOD 3103 is a compact low end system (64k words) with primary memory expansions (up to 256k words) making small unit processes and remote or critical operations comprising a few loops economically possible. The 3106 is a high end system (64k words) with memory expansions to 512k words for complex or critical process management and control requirements. Both systems use 16-bit semiconductor main memory with ECC logic that automatically corrects single-bit errors, reducing system downtime and enhancing system availability. POL (Process Oriented Language) software, a realtime high level process control language, features online editing capability that allows addition or deletion of operating procedures without interrupting control of the process. **Taylor Instrument Co**, 95 Ames St, Rochester, NY 14601.

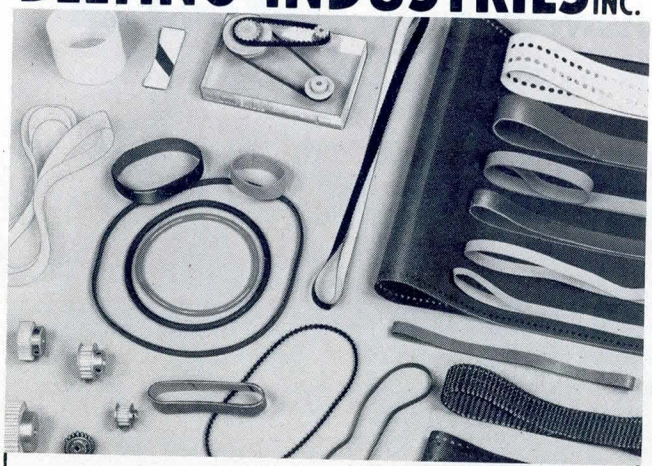
Circle 261 on Inquiry Card

MINICOMPUTER SYSTEMS

V77-500 and -700, 16-bit microprogrammable minicomputers designed for easy field upgrading, offer features and functions of mainframes. Suitable for nodes in a distributed data processing network, both models are fully compatible with the company's range of DDP software, including transaction processing systems and software based on distributed communications architecture. In a DDP environment with a remote IBM host, either system can provide the necessary interface between IBM 3270 terminals and the IBM host. As general purpose minicomputers, the systems feature high speed CPUs, memory mapping and control, error detection and correction, hardware multiply and divide, and direct memory access. Both offer optional writable control store of 2k 48-bit words. Up to 2048k bytes of MOS ECC memory can be installed in the -700; up to 1024k bytes in the -500. Memory cycle time is 600 ns. An optional floating point processor on the -700 accelerates FORTRAN program execution. VORTEX II is the standard operating system. Programming languages include FORTRAN IV, COBOL, RPG II, and micro and macro assemblers. **Sperry Univac,** PO Box 500, Blue Bell, PA 19424.

Circle 262 on Inquiry Card

BELTING INDUSTRIES CO. INC.



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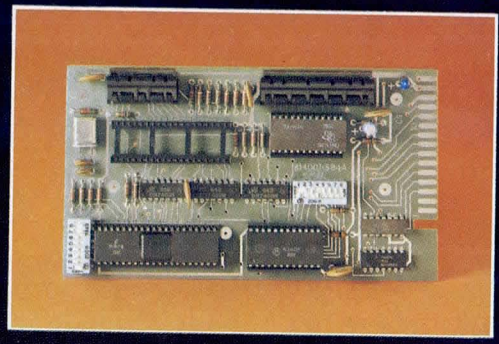

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Circle 139 For Further Information. **Circle 140 For a Salesman to Call.**

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CIRCLE 164 ON INQUIRY CARD

LITERATURE

CAD/CAM Tools

Information file consisting of brochure, history, and file folder introduces AD2000 series. **Manufacturing and Consulting Services, Inc,** Santa Ana, Calif.

Circle 300 on Inquiry Card

Data Converters

Using tables to present technical data and specs, color catalog features hybrid and discrete data conversion products. **ILC Data Device Corp,** Bohemia, NY.

Circle 301 on Inquiry Card

TTL Compatible Fiber Optic Transmitter

Data sheet describing OTX5000 series lists fields of application, features, and specs, and includes block diagram, performance curves, and dimensional drawing. **Optical Information Systems,** Elmsford, NY.

Circle 302 on Inquiry Card

Signature Analysis

Application Note 222-3 presents economic model for determining cost and feasibility of signature analysis for testing and servicing microprocessor based products. **Hewlett-Packard Co,** Palo Alto, Calif.

Circle 303 on Inquiry Card

Computers and Peripherals

Naked Mini family is covered in 20-p color brochure that includes photos and specs and highlights Naked 4 series. **Computer Automation, Inc,** Irvine, Calif.

Circle 304 on Inquiry Card

I/O Subsystems

Booklet provides overview of devices for use with DPM family of industrial computerized management systems, detailing specs and summarizing configurations. **Digital Equipment Corp,** Maynard, Mass.

Circle 339 on Inquiry Card

Capacitors

Line drawings, dimensions, ratings, tolerances, and temperature characteristic curves present complete array of multilayer capacitors and electronic ceramics in multicolor catalog. **RMC-Radio Materials Corp,** Chicago, Ill.

Circle 305 on Inquiry Card

Stabilized Power Supplies

Tables, photos and specs describe linear (series pass), ferroresonant (CVT), and switching (offline) stabilizers. **Kepco, Inc,** Flushing, NY.

Circle 306 on Inquiry Card

Operating Systems

Diskette based MDOS/80 and disc based HDOS/80 features are itemized in two separate brochures. **Ontel Corp,** Woodbury, NY.

Circle 307 on Inquiry Card

Dot Matrix Printers

Brochure discusses advantages of hammer bank over font printing mechanisms, and provides functional and general specs by models. **Printronix, Inc,** Irvine, Calif.

Circle 308 on Inquiry Card

Programmable Modular Test Instruments

Included in 4-p catalog are features and functions of 50-MHz clock generator, 30-MHz word generator, and MOS/CCD drivers. **Pulse Instruments Co,** San Pedro, Calif.

Circle 309 on Inquiry Card

Panels and Systems

Tables and photos in panel selection guide describe wirewrapping packaging panels and systems, and include compatability information. **Augat Inc, Interconnection Systems Div,** Attleboro, Mass.

Circle 310 on Inquiry Card

Power Supplies

Modules with outputs from 1 to 200 V and up to 60 A are detailed in catalog that includes selection guide. **Acopian Corp,** Easton, Pa.

Circle 311 on Inquiry Card

Digital to Synchro/Resolver Converter

Microprocessor compatible, 16-bit hybrid unit is described in data sheet that provides features, applications, specs, and notes on designing with HD SR 2006. **Natel Engineering Co, Inc,** Canoga Park, Calif.

Circle 312 on Inquiry Card

Display Systems Operation and Applications

System overview, interfaces, and demonstration program sequences for SM-810-001/002 are illustrated with block diagrams and schematics in application note. **Beckman Instruments, Inc,** Scottsdale, Ariz.

Circle 313 on Inquiry Card

Power Sources

Catalog uses tables and photos to detail specs for both voltage and current programmable models. **Kikusui International Corp,** Carson, Calif.

Circle 314 on Inquiry Card

Magnetic Shields

Combination catalog and technical reference guide uses illustrations, photos, formulas, and graphs to detail magnetic shields and shielding materials. **MuShield Co,** Malden, Mass.

Circle 315 on Inquiry Card

Switching Power Supplies

Catalog details MOS open frame switchers and single-output switchers up to 1200 W, and features tutorial article on VARI-DRIVE. **Todd Products Corp,** Brentwood, NY.

Circle 316 on Inquiry Card

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CIRCLE 141 ON INQUIRY CARD

LITERATURE

Datacomm Diagnostic System

Brochure on DATA MONITOR 200 discusses design concept and includes photo of front panel with callouts and functional summaries of all controls. **Digitech Industries, Inc,** Ridgefield, Conn.

Circle 317 on Inquiry Card

Integrated Communications

Brochure addresses networking requirements of datacomm users and contains schematics illustrating applications for TRANSPORT, COMMAND, and EXCHANGE products. **Codex Corp,** Mansfield, Mass.

Circle 318 on Inquiry Card

Logic Analyzer Instruments

One brochure covers PI-532 and its application in lab, factory, and field; another explains state, timing, and waveform facilities of PI-540. **Paratronics Inc,** San Jose, Calif.

Circle 319 on Inquiry Card

CAD/CAM Functions

CADAM system's hardware and software components, applications, and database access are detailed in full-color brochure. **Lockheed-California Co,** Burbank, Calif.

Circle 320 on Inquiry Card

Local Data Distribution

Catalog presents overview of modem and line driver families, ancillary products, and interface converters, together with summary of their specs. **Avanti Communications Corp,** Newport, RI.

Circle 334 on Inquiry Card

Microcomputers

Catalog introduces TRS-80 model III, color and pocket computers, and VIDEOTEX systems, as well as printers, software, and accessories. **Tandy Corp/Radio Shack,** Fort Worth, Tex.

Circle 335 on Inquiry Card

Microcomputer Accessories and Interfaces

Short form catalog provides descriptions and photos of ac remote controls, data acquisition modules, and printer adapters. **Connecticut microComputer, Inc,** Brookfield, Conn.

Circle 336 on Inquiry Card

High Voltage dc Power Supplies

Technical specs, model selection table, photos, and dimensional drawings are supplied by data sheet on MG series. **Glassman High Voltage, Inc,** Whitehouse Station, NJ.

Circle 337 on Inquiry Card

CRT Terminal

Flyer shows keyboard layout and outlines command and control set and basic specs of Ambassador. **Ann Arbor Terminals, Inc,** Ann Arbor, Mich.

Circle 338 on Inquiry Card

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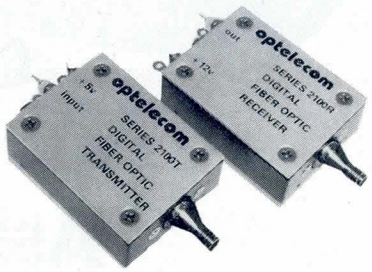

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	LA120 DECwriter III RO	2,095	200	112	75
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	VT132 CRT DECscope	1,995	190	106	72
TEXAS INSTRUMENTS	TI745 Portable Terminal	1,595	153	85	58
	TI765 Bubble Memory Terminal	2,595	249	138	93
	TI783 Portable KSR, 120 CPS	1,745	167	93	63
	TI785 Portable KSR, 120 CPS	2,395	230	128	86
	TI787 Portable KSR, 120 CPS	2,845	273	152	102
	TI810 RO Printer	1,895	182	102	69
	TI820 KSR Printer	2,195	211	117	80
CENTRONICS	730 Desk Top Printer	715	69	39	26
	737 W/P Desk Top Printer	895	86	48	32
	704 RS232-C Printer	1,795	172	96	65
	6081 High Speed Band Printer	5,495	527	293	198
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	DT80/1L 15" Screen CRT	2,295	220	122	83
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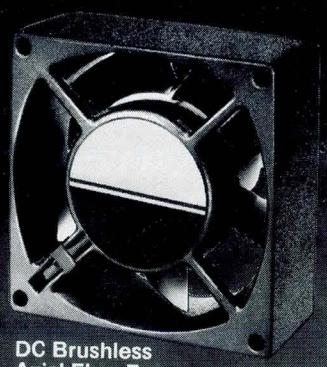

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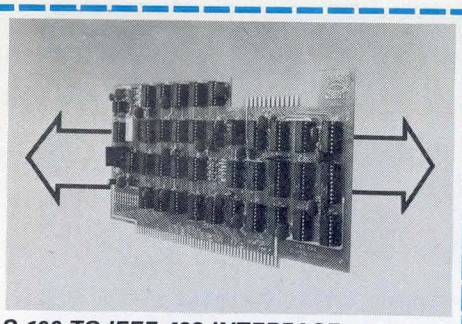

S-100 TO IEEE-488 INTERFACE

THE P&T-488 INTERFACE BOARD lets your S-100 computer be a talker, listener, or controller on the IEEE-488 instrumentation bus. Software packages allowing high level language access to the 488 bus are available for CP/M, CDOS, North Star DOS/BASIC, as well as for direct assembly language programming. Price of the P&T-488, assembled and tested with one of the software packages, is $450.

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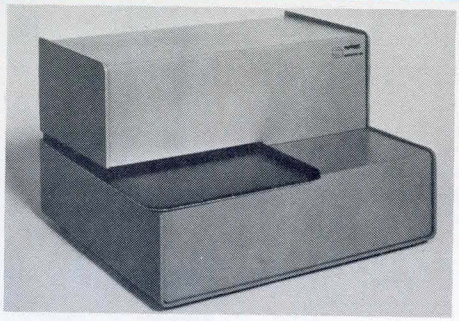

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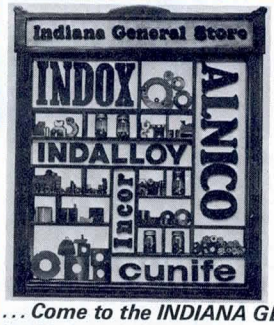

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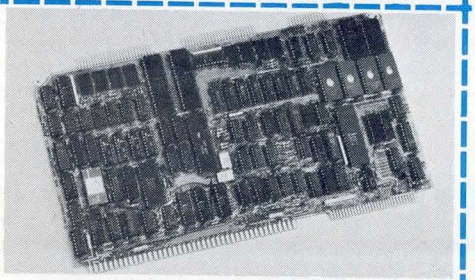
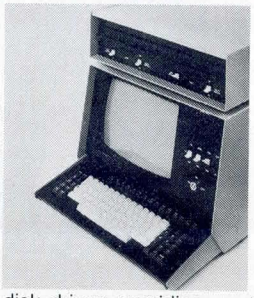


THE MC 85 SINGLE BOARD COMPUTER

features a 5MH$_z$ 8085 CPU, 4K bytes of RAM, four sockets for 16K bytes of EPROM, 48 programmable I/O lines with sockets for interchangeable line drivers and terminators, a programmable RS232C communications interface, a programmable eight-level vectored priority interrupt controller, and three programmable interval timers. In addition, a programmable CRT display controller with 2K of display RAM, keyboard input port, belltone driver, and 8-level parallel bus arbitration have been included.

COMARK CORP., 257 Crescent St., Waltham, MA 02154. (617) 894-7000. **CIRCLE 556**



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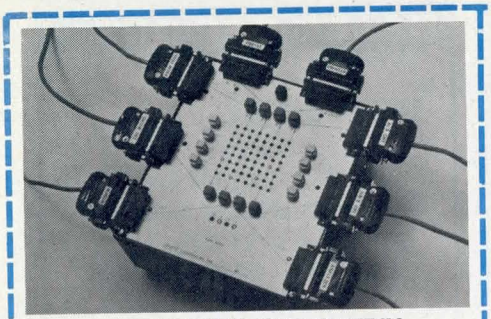

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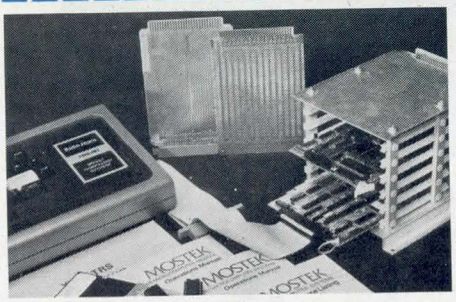

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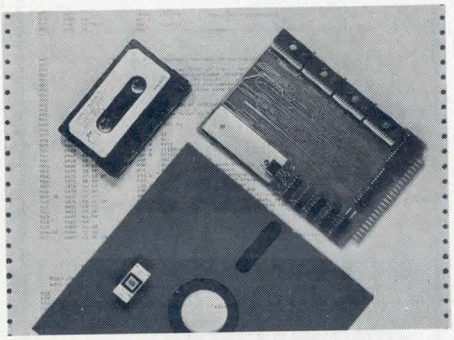

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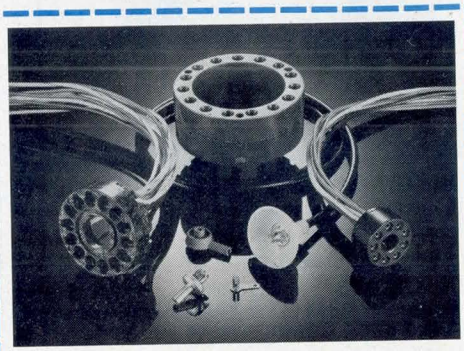

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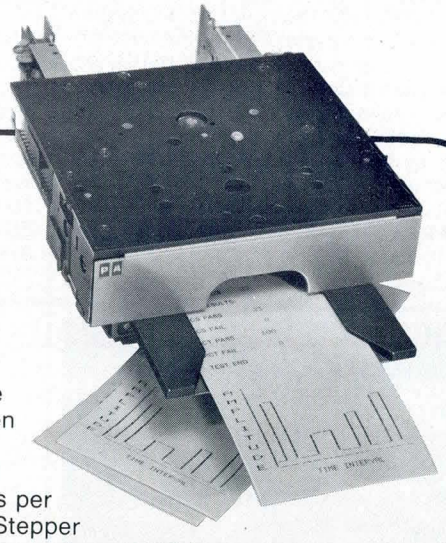
CIRCLE 148 ON INQUIRY CARD

Our Alphanumeric Ticket Printer



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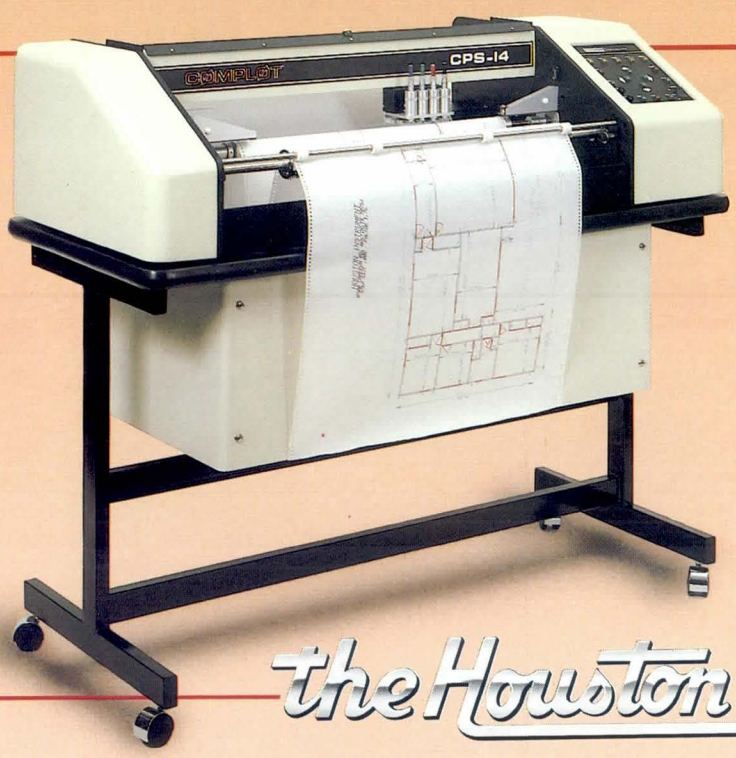

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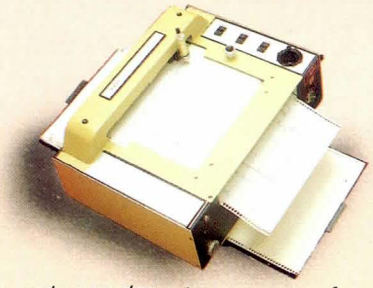
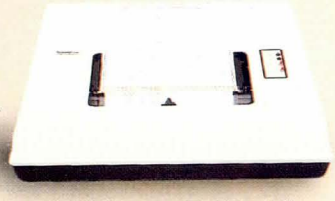
CØMPLØT® pen plotters are available in fourteen different models with X-Y plotter sizes of 8½ x 11" (DIN A4) or 11 x 17" (DIN A3) and drum plotter sizes of 11" (28 cm) to 42" (107 cm). Pen speeds range from 240 to 4,000 steps/sec. Prices begin at a low $1,085.*



CØMPLØT electrostatic plotters and plotter/printers are available with models for printing (up to 2,400 lines per minute), plotting (up to 2" per second), or simultaneous plotting and printing.

CØMPLØT electrostatic CRT copiers provide fast, quality hardcopies from Hewlett Packard Series 2640 terminals or Tektronix® 4010 family terminals for just a few cents per copy. Prices for the Houston Instrument electrostatic products range from $3,950 to $6,550.*



Our Model 6000 TISPP (Thermal/Intelligent/Strip/Plotter/Printer) allows superior quality graphics output from either an analog or digital source and provides the continuity and clarity of a continuous trace with alphanumeric annotations under intelligent control. It's the versatile graphic output device for the new generation of microprocessor controlled instrumentation. Available in one or two pen versions. Prices start at $1,795.*

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Circle 149 for Information on Pen Plotters.

Circle 150 for Information on Electrostatic Products.

Ask Ramtek.

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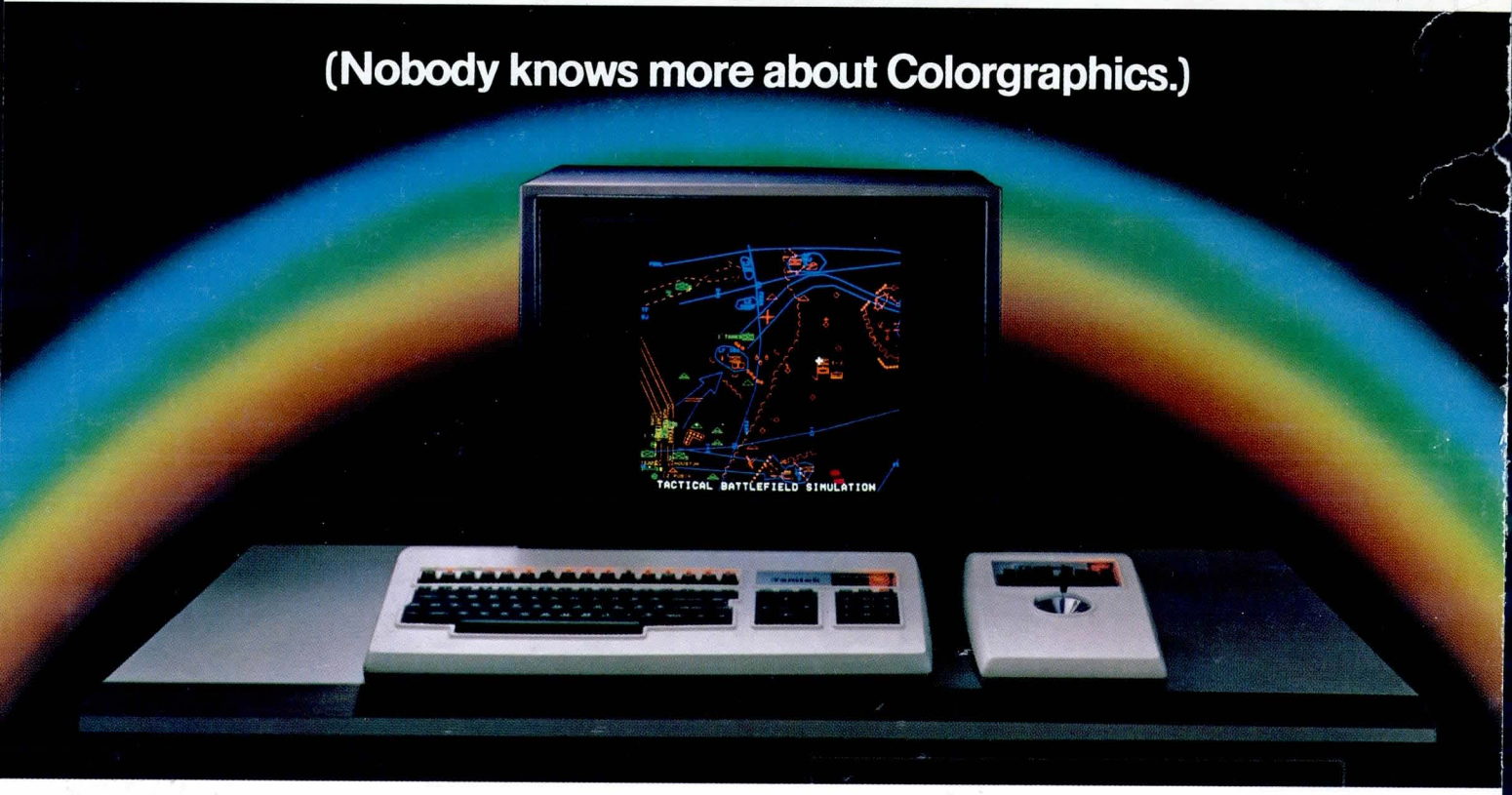

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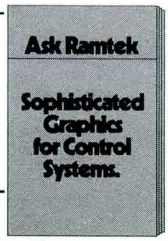

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