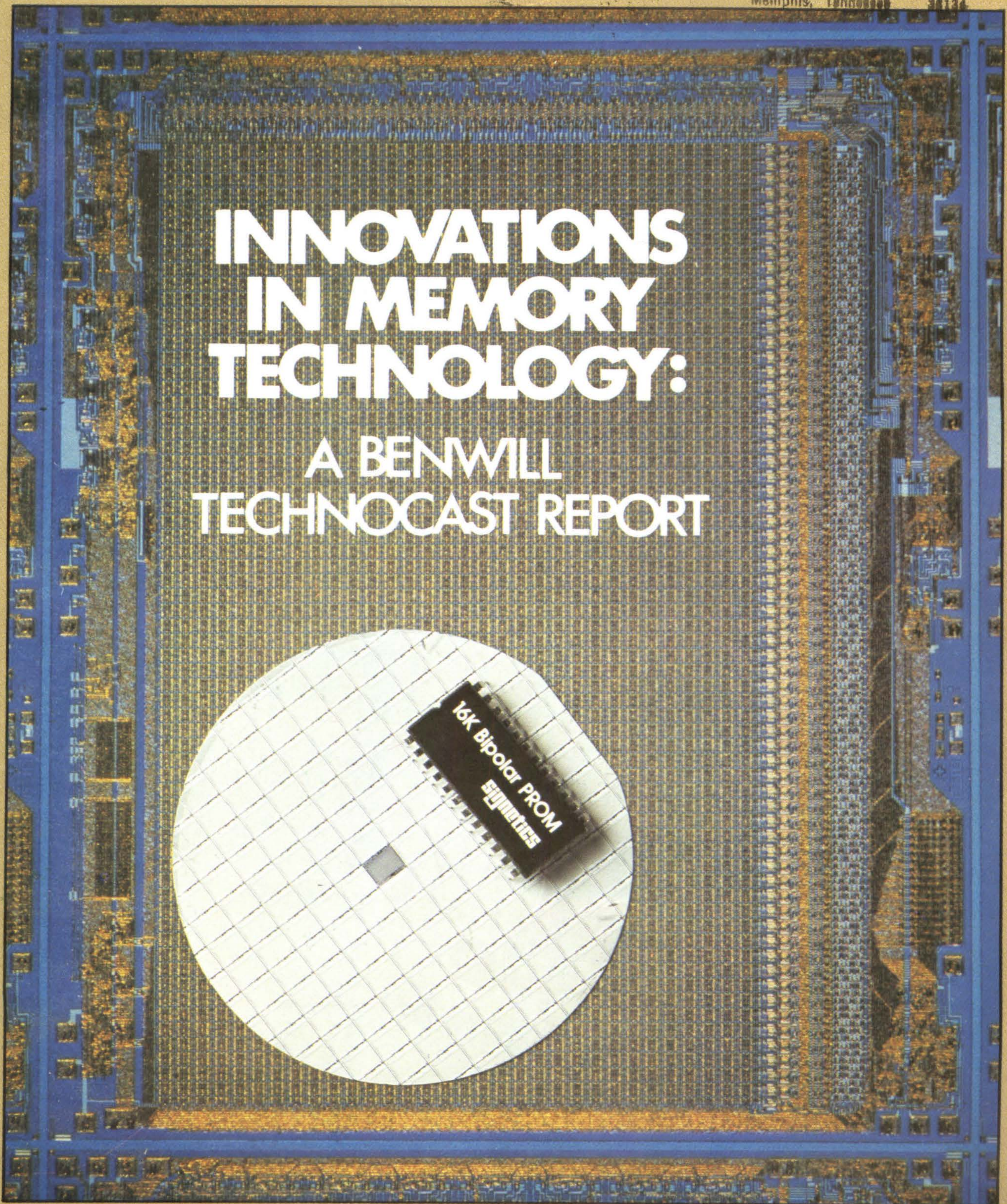
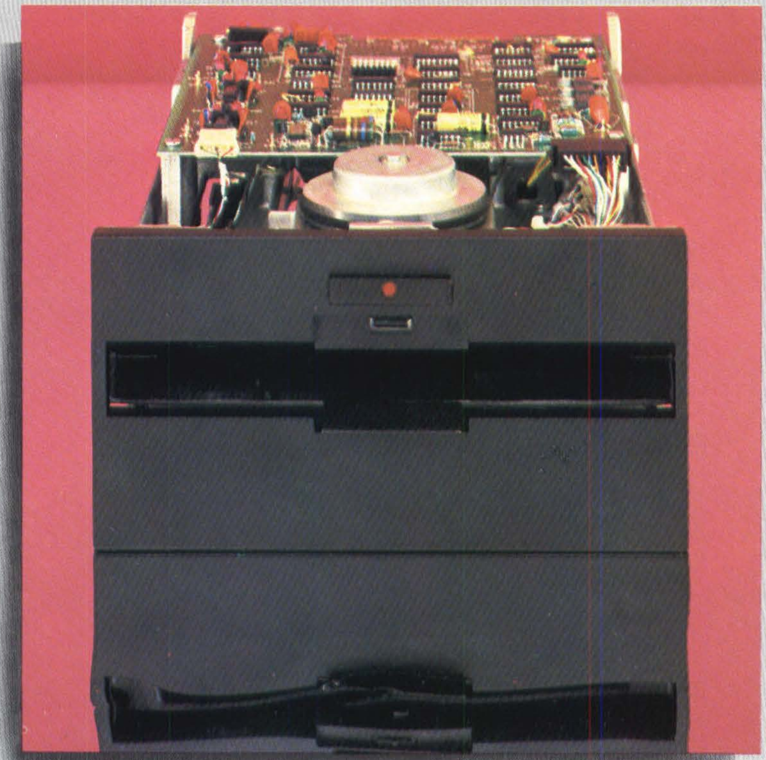
August, 1977

digital design

the magazine of digital systems





Go with the winner-GSI-FDD 200.

Double-sided, double-track density, flexible disk drive

The winner in high quality, delivery and price. GSI's FDD 200 disk drive accommodates up to 25.6M bits using MFM or M^2FM encoding techniques. Downward compatible with GSI's FDD 110 and available in the same package design, it is available for upgrading with minor system modifications. It is fully IBM compatible and will read and write IBM 3740 formatted diskettes. You also can daisy chain up to 4 drives.

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Go with the thousands of happy GSI winners. What have you got to lose?

ter peripherals-second to none.

CIRCLE 1

GSI THE WINNER

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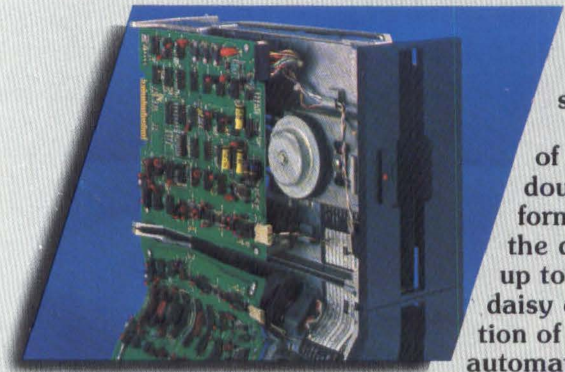
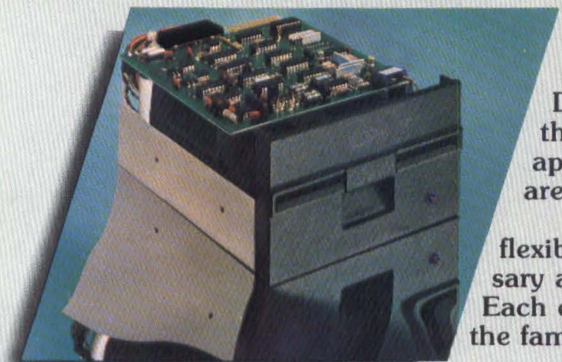


Flexible Disk Drive *GSI-FDD 110*

A compact, random access, flexible disk drive for single or double density data storage.

It will accommodate up to 6.4M bits of data on one side of standard media using MFM or M²FM encoding techniques for double density applications. Single density storage in variable formats provides up to 3.2M bits of data. Fully IBM compatible the disk drive will read and write IBM 3740 formatted diskettes up to 1.9M bits. The high performance unit offers up to 4 drive daisy chain operation, parallel ready lines plus unit select, separation of clock and data and Track "00" photo sensing. It also has automatic diskette ejection and a fail safe interlock.



Flexible Mini-Disk Drive GSI-MDD 050

The GSI family of highly reliable small Mini-Disk Drives: MDD 050, 100K bytes; MDD 051, 200K bytes and the MDD 052, 465K bytes are designed to fit into many applications where conventional disk drives (GSI-FDD 110) are physically inappropriate and space is at a premium.

Low in cost, the MDD 050 Mini-Disk Drive utilizes a small flexible disk permanently housed in an envelope with the necessary apertures for drive spindle, head and sector hole access. Each envelope is 5¼" by 5¼" but otherwise is conceptually like the familiar IBM diskette.

Horizontal Autoloader *GSI-H155*

The Horizontal Autoloader automatically loads and unloads open or closed flap diskettes to and from a GSI-FDD 110 Flexible Disk Drive. Diskettes are loaded sequentially from the hopper. After processing in the diskette drive, the diskettes are electronically selected and stacked horizontally in either of its two bins. The bins are removable and suitable for general handling of diskettes.

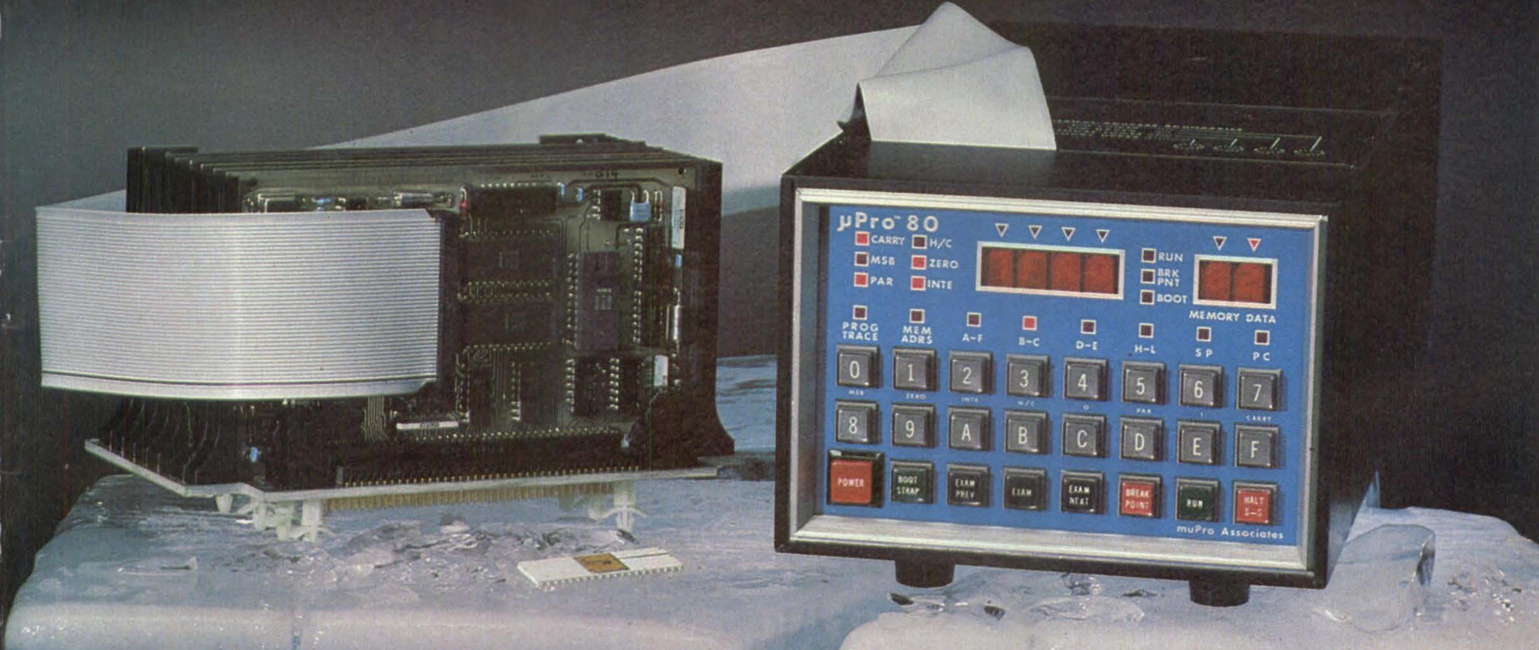
Flexible Disk Drive Sub-Systems GSI-FDD 2100

Packaged horizontally into a 19" Retma rack mount chassis, the GSI-FDD 2100 series sub-systems provide single and dual drive capability. Included in the sub-system is the necessary power to drive two flexible disk drives and a customer supplied formatter. Input AC power is supplied from the host computer controller via a relay system included in the GSI-FDD 2100.

GSI-World leadership in compu

The 8080 "Ice Breaker"

Portable for Development - Production Test - Field Service



BREAKTHROUGH QUESTIONS	muPro-80E	INTEL® MDS + ICE*
Portable for development, test, and field service?	YES, 4.6" x 6.6" x 15" 18 lbs.	NO, 8.5" x 19" x 17" 65 lbs. Plus terminal
Real time execution from emulator or users system memory?	YES, phase locked to user clock; rate up to 2.86 mHz	NO, emulator resident programs execute slower than real time
Totally transparent control/display functions?	YES	NO, imposes memory, I/O and interrupt restrictions
Memory available to user in 16K emulator system?	ALL 16K	LESS THAN 4K (12K+ used by ICE-80 driver)
High-level relocatable language supported by 16K paper tape or 32K disk system?	YES, BSAL-80	NO, PL/M® requires 64K disk system
Assembly language efficiency with high level language?	YES, BSAL-80	NO, PL/M® burdened with typical compiler inefficiences
Multi-user/Multi-task disk operating system?	YES, plus concurrent batch capability	NO, single user/single task

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Consider Your Field Service and Production Requirements.

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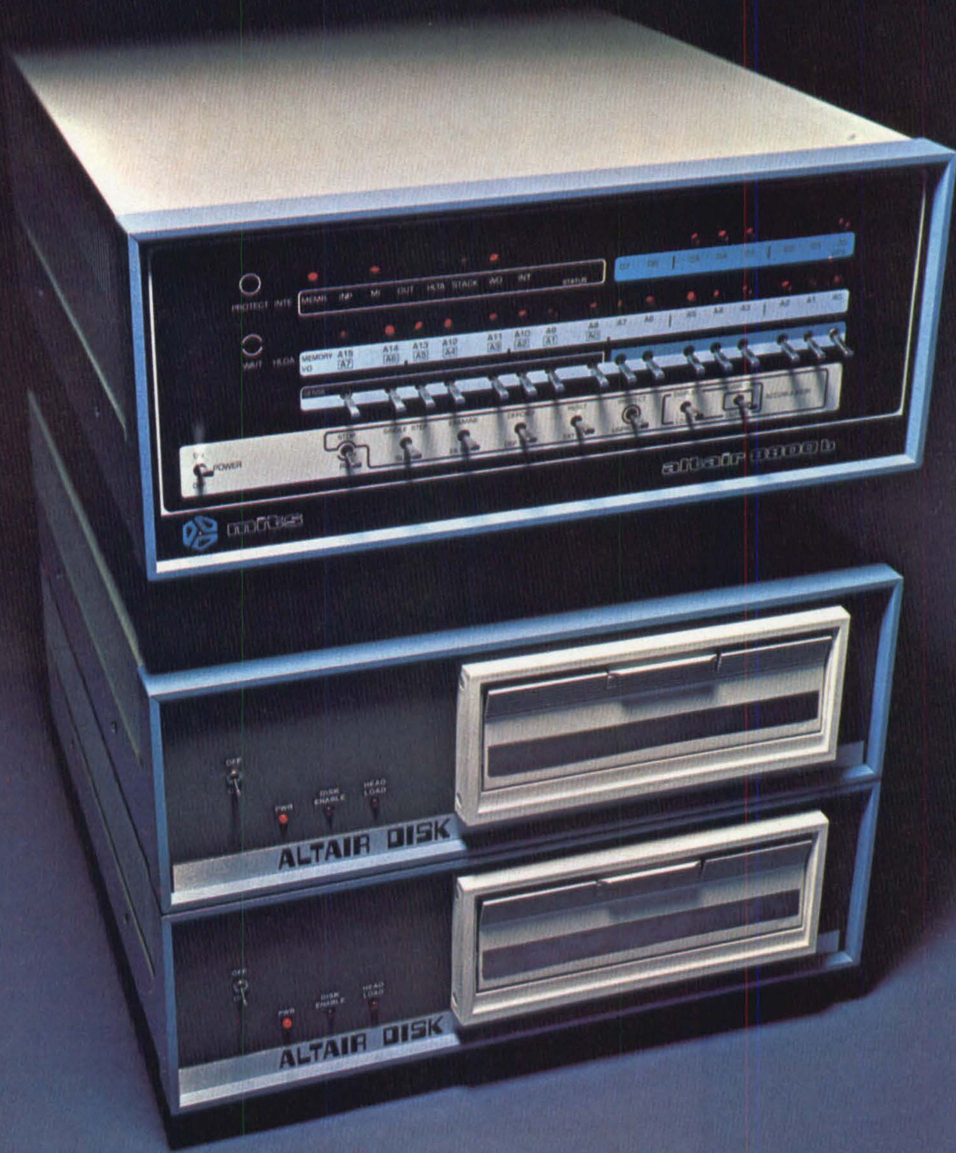
muPro Inc. ▪ 424 Oakmead Pkwy ▪ Sunnyvale, CA 94086 ▪ (408) 737-0500

Circle for Demonstration - Circle 100 for Literature



altair™ floppy disk system

Disk capabilities can transform an ordinary microcomputer system into one of infinite magnitude. By introducing one Altair Floppy Disk System (88-DCDD), your 8800 series system acquires a mass storage capacity of 310,000 bytes per diskette.

The 88-DCDD includes a disk drive, controller, power supply, interconnect cable and case. Featuring a Pertec FD-400, the disk drive unit has direct drive dc motor operation which is insensitive to disrupting line frequency variations.

Up to 16 disk drives may be interfaced with the Altair Disk Controller. Consisting of two PC cards that plug into the Altair 8800 bus, the Disk Controller regulates all mechanical operations and disk status.

Two software systems are available for the Altair Floppy Disk. Altair Disk BASIC offers the many features of Altair Extended BASIC plus increased program and data file load/save facilities. Our new DOS provides comprehensive tools for assembly language program development and disk file maintenance.

See the Altair Floppy Disk System along with the complete Altair product line at your local Altair Computer Center, or contact the factory for further information.

mits

2450 Alamo SE Albuquerque, N.M. 87106

CIRCLE 5

digital design

Volume 7 Number 9 August, 1977

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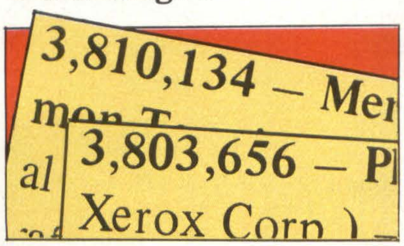
Computer Memory Technologies



Development of new memory technologies is changing the face of computer design. Part I of our Benwill Technocast memory report covers the state-of-the-art and patent activity for magnetic core, charge coupled devices and other types of memories.

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Fiberoptics Design for Digital Systems

Technological advances have opened up new applications for fiberoptics. Richard A. Cerny and Dr. Marshall C. Hudson discuss the use of fiberoptic technology in the specification and design of digital communication systems.

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Multiplexing Planar Gas Discharge Displays

Multiplexed drive of gas discharge displays becomes more effective as the number of digits increases; Robert Kuntz, Dave Sien and Wayne Wong show you how to multiplex these displays in your system.

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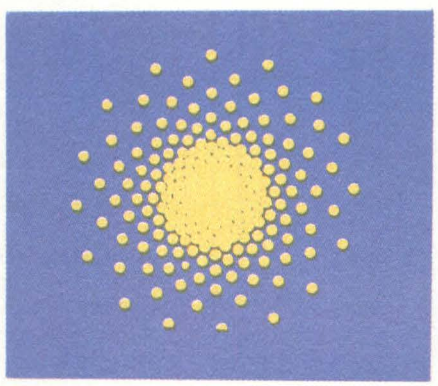
Stacked Microprocessors: A Better Way To Go



Races between memory speeds and processor speeds are forcing new architectures to develop. In this book excerpt, Charles Sippl discusses multiprocessing with microcomputers.

This Month's Cover

This month's cover, spotlighting our Benwill Technocast memory technology report, shows a Signetics 16K bipolar ROM in three forms: wafer, die and finished package.

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Adjustable concrete-mix scale-encoder handles special codes.
Altering keyboard's interconnection scheme trims calculator design.
Small double-sided double density disk.

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Future Microprocessor Software: Another View— Mike Hordeski looks at μP software development.

Published monthly by Benwill Publishing Corp., 167 Corey Rd., Brookline, MA 02146. Controlled Circulation postage paid at Long Prairie, MN.

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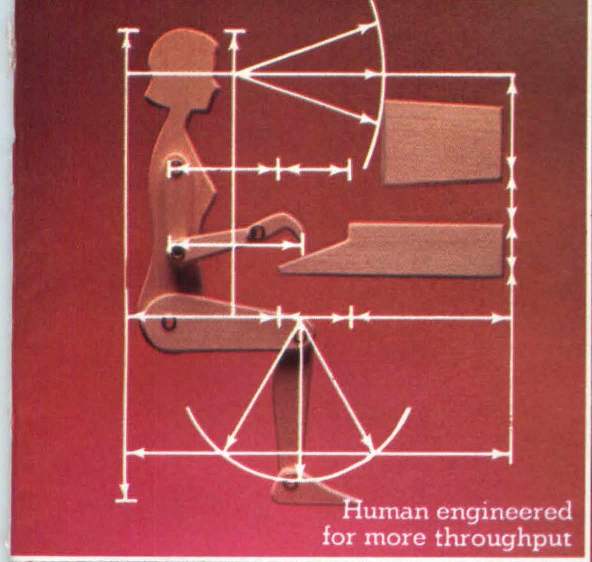
Published monthly by Benwill Publishing Corporation, Harold G. Buchbinder, Chairman of the Board; George Palken, President; Esther Shershow, Treasurer, Executive, Editorial and Subscription Offices, 167 Corey Rd., Brookline, MA 02146. Telephone: (617) 232-5470.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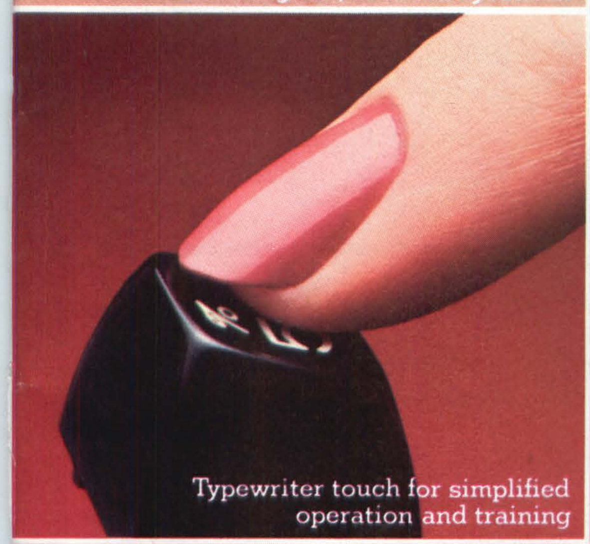
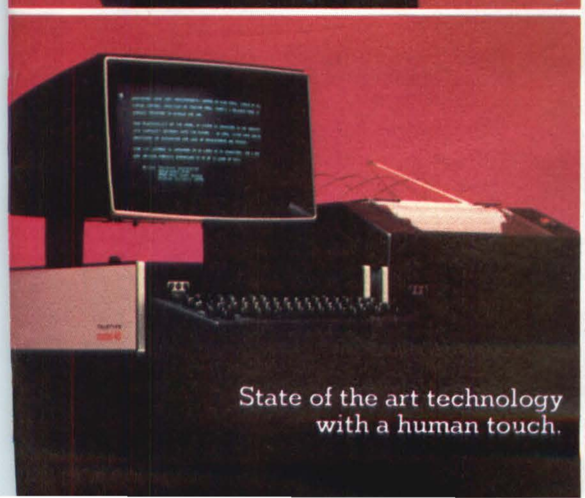
for more throughput


Reduced glare, reduced eyestrain


Typewriter touch for simplified
operation and training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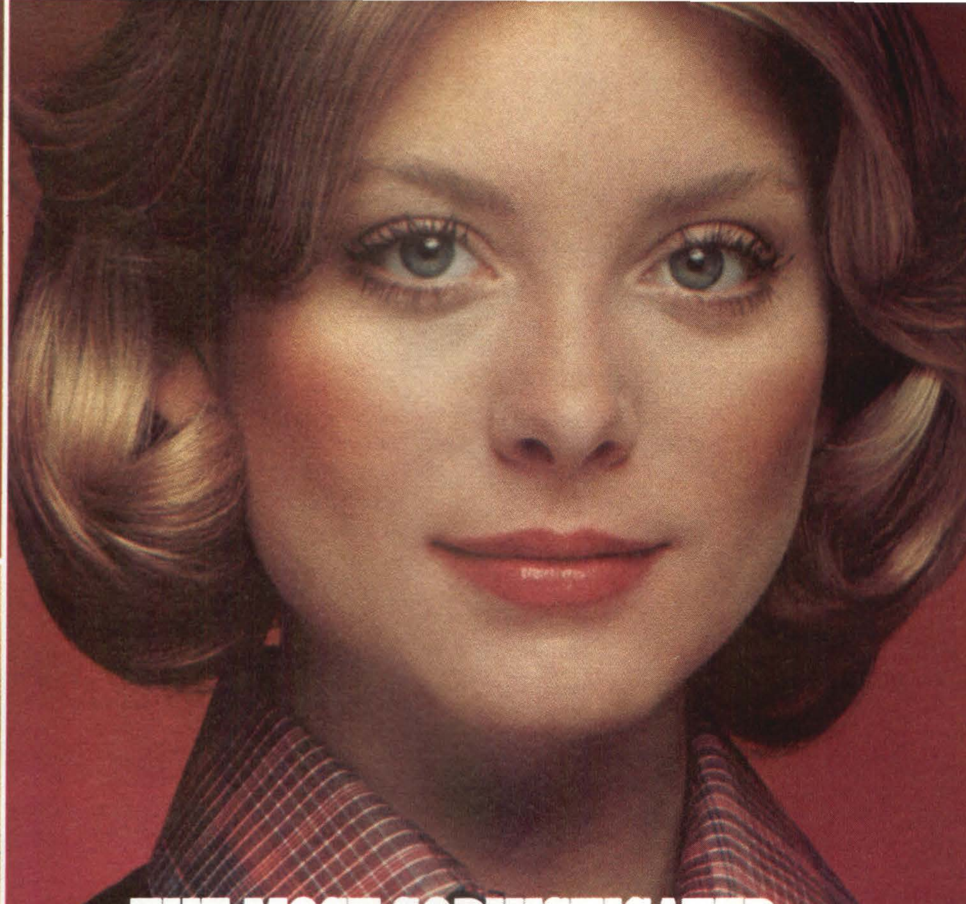
with a human touch.



THE MOST SOPHISTICATED, COMPLICATED COMPONENT OF ANY DATA TERMINAL SYSTEM IS THE PERSON BEHIND THE CONSOLE.

When we designed the Teletype® model 40 product line, we paid as much attention to human engineering as we did to electronic engineering. Simply because we don't think one makes much sense without the other.

After all, throughput is as much a function of operator performance as it is of advanced CMOS technology.

That's why we positioned the tube so it's a comfortable 19" to 21" from the operator. The tube isn't in a fixed position, either, but tilts through 20° to adjust for lighting conditions and individual viewing preferences.

To eliminate eyestrain, a specially darkened and etched glass is used on the screen to diffuse surface reflections and increase contrast by 100%. Even the large 7 x 9 display font is designed for legibility, with a flicker-free refresh rate of 60 times/second. Plus generous spacing between characters and lines increases readability even more.

Keyboard controls aren't just grouped by function so they look right, we made them "feel" right, too. Not only do they fit the fingers, they also duplicate the touch and feel of office typewriters.

As you can see, we think the best way to impress you with our model 40 product line is to make sure your operator is impressed. For more information, write: Teletype, 5555 Touhy Ave., Skokie, IL 60076. Or call: 312/982-2000.

TELETYPE

1200 baud acoustic couplers are available

• Dear Editor: Yes is the answer to the question that Mr. Scott Kellogg of the University of Hawaii asked in the May issue of Digital Design about the availability of a 1200 baud acoustic coupler. Omnitec Data Corporation has had the 1200A intelligent acoustic coupler (capable of doing line control) on the market for three years now and has recently introduced the 1200B. Since Mr. Kellogg had a baud rate selectable terminal, he might also be interested to know about Omnitec's 103/202 switchable coupler which allows 110-300-600 and 1200 baud operation in one unit. This is also an intelligent coupler which can be field programmed for 'smart' or 'dumb' terminals and the full variety of timing delays available in 202S operation.

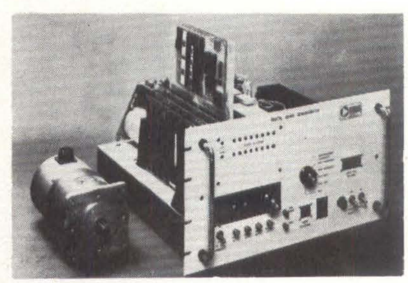
FRAN WILLES
National Sales Manager
Omnitec Data Corporation
Phoenix, AZ

What is wrong with 3 letter mnemonics?

• Dear Editor: Either I fail to understand what the modestly proposed no-language proposal is about (Viewpoint, May 1977), or Mr. Amatneek fails with some 'hands-on' experience with either programming or logic design. Isn't the 'something explicit, easy to remember and universal' no-language which computer people are supposed to have just what is well-known as a truth table or machine-code ('language')? What is wrong with 3 letter mnemonics? After all, assembly code is the next best thing to a truth table.

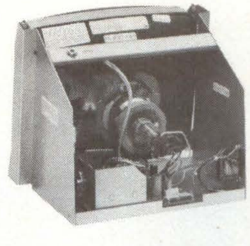
GERO TIMMERMANN
Kitt Peak National Observatory
Tuscon, AZ

So who makes it?



In our story on the programmable servo-control (**Digital Design**, June, 1977, p. 19), we inadvertently omitted the name of the manufacturer, Torque Systems, P.O. Box 588, 225 Crescent St., Waltham, Massachusetts 02154. We apologize for this omission.

Reliability:



Our data displays are outstanding solid-state designs with critically matched magnetics to optimize the performance levels and dependability demanded by your customers. We use the most advanced engineering and production techniques to assure consistency of performance. No data display is built with more deliberate attention to quality and reliability.

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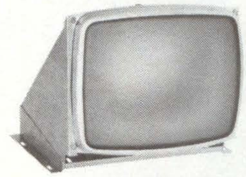

We have been in the display electronics business long enough to know about rush orders. If you need it yesterday — we'll try to get it to you yesterday.

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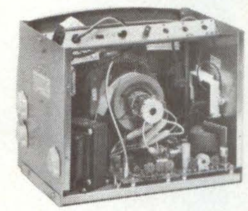
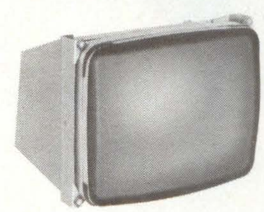


We've built thousands of displays for many of the major manufacturers in the country. Perhaps we already have a unit that would meet your requirements. With slight modifications. It would be less costly than starting from scratch. If you need a new, special package — we'll produce it for you, in the configuration you want, at minimal expense.

Cooperation:



If you're developing a new data terminal, we will be glad to cooperate with your terminal design engineers in reviewing your exact specifications and developing the most economical display possible. And quickly! Whatever you need, we have the experience and talent to design it. And improve it.

But don't take our word. See for yourself by contacting us today.

You'll come up with your own reasons for using Setchell Carlson CRT display modules.

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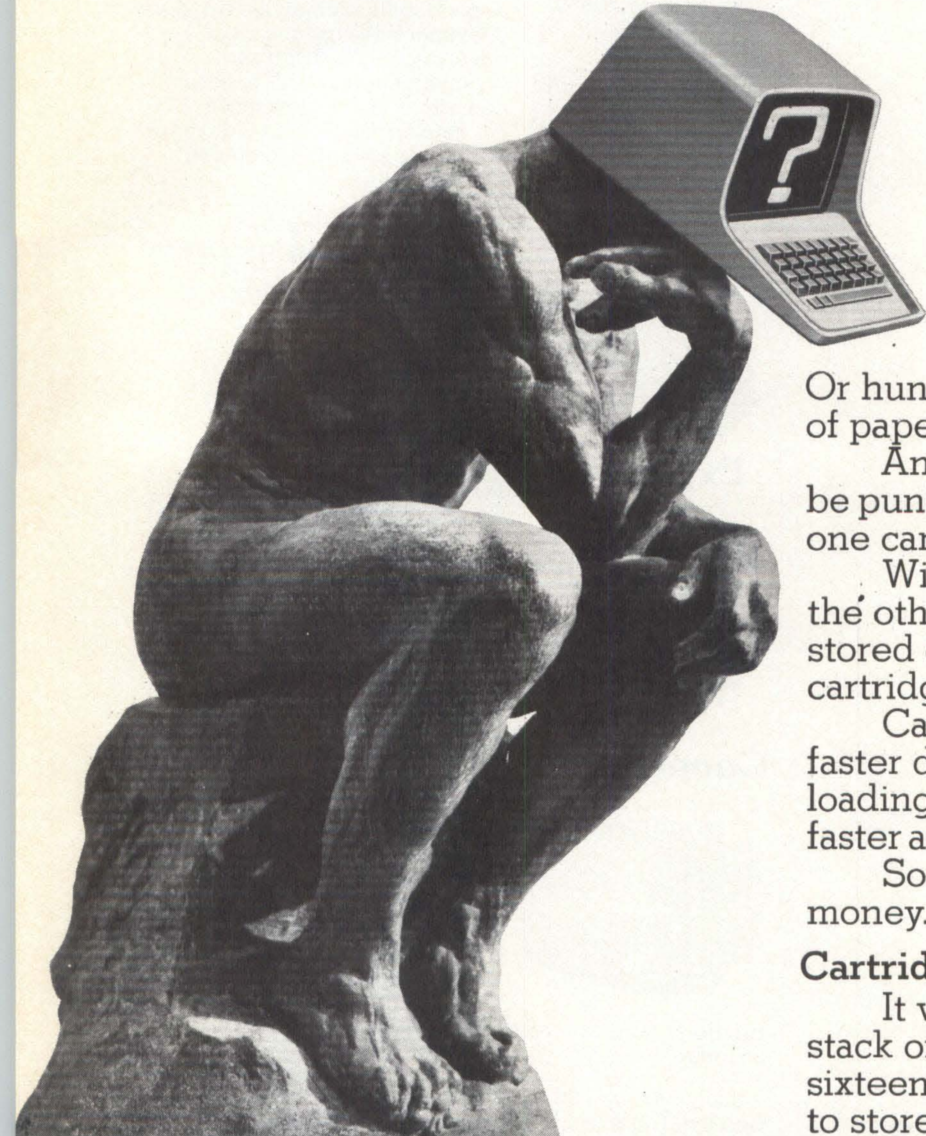
If you make top-quality data terminals, here are four reasons to use Setchell Carlson CRT display modules in your system.

CIRCLE 12

Is your computer smart enough



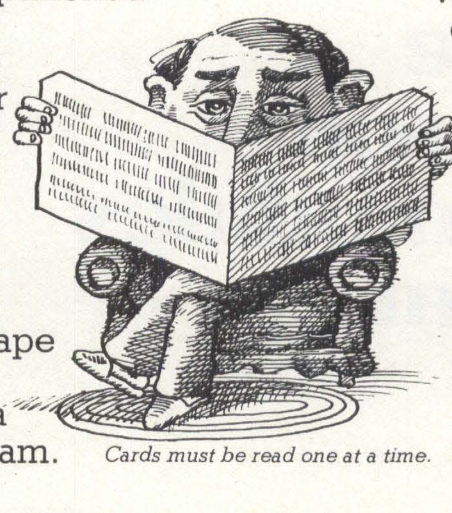
A 3M peripheral drive which uses 3M data cartridges is better than any drive which uses punched cards or paper tape.

And, if you'd take the time to ask it, your computer would probably tell you so.

It's simple logic.

Cartridges are faster than cards.

Cards and paper tape are slow. It takes hundreds of cards for a single computer program.



Cards must be read one at a time.

Or hundreds of feet of paper tape.

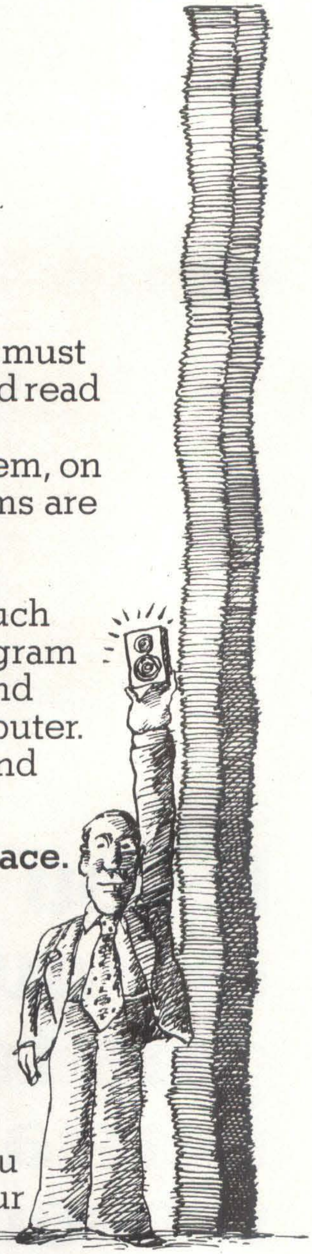
And each program must be punched, verified and read one card at a time.

With our drive system, on the other hand, programs are stored on a single tape cartridge.

Cartridges offer much faster data storage, program loading, data transfer and faster access to the computer.

So you save time and money.

One DC-300A cartridge equals almost 16 feet of cards.



Cartridges take less space.

It would take a stack of cards almost sixteen feet high to store all the information you can store on a single 3M DC-300A data cartridge.

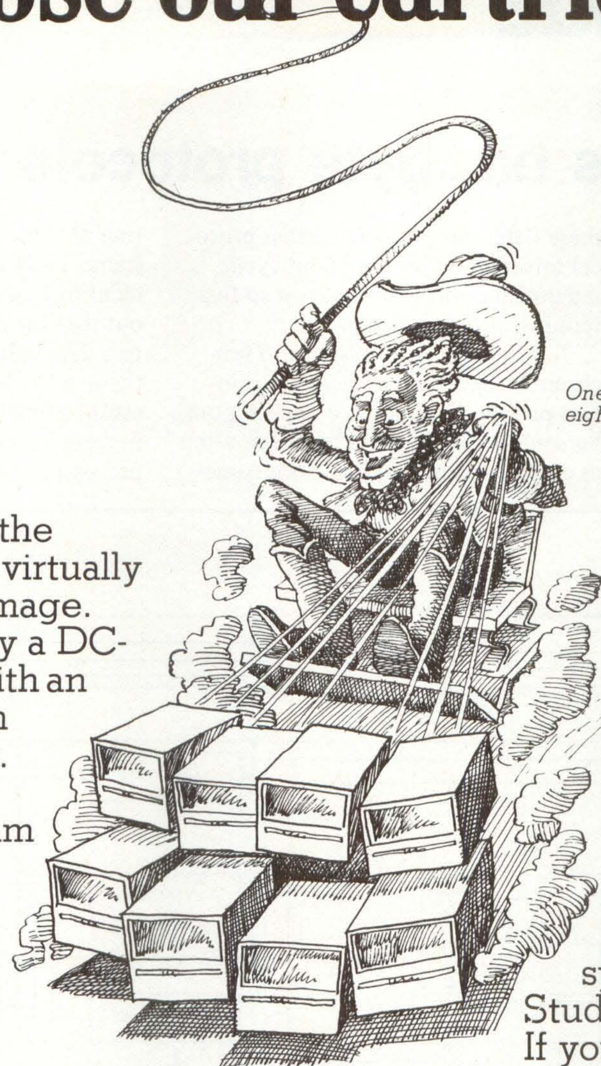
With cartridges, you can store all of your programs in a fraction of the space you'd need for cards or paper tape.

Your filing system is simplified and overhead is greatly reduced.

Cartridges won't fold, spindle or mutilate.

Unlike paper cards, you need never touch the media. It's well

to choose our cartridge drive?



One formatter can control eight drives at once.

protected inside the cartridges, so it's virtually impossible to damage.

You can carry a DC-100A cartridge with an entire program in your shirt pocket.

Even if you drop it, the program will survive unscathed.

Remember that the next time you drop a stack of cards.

Don't take our word for it. Ask your computer.

If you'll send us the coupon, we'll send you the specifications for all three of our drive systems.

Ask your computer to compare them with any other type of drive system.

We'll bet your computer will prefer ours.

Maybe it'll choose our famous DCD-3 drive. It's people-proof, jam-proof and wear-resistant.

Or maybe your computer will decide upon our DCS-3000 series, an ANSI-formatted system that allows one formatter to control up to eight drives.

The DCS-3000 is extremely easy to integrate into your system. Only one cable to the user's logic is required.

But if you require compact size, your computer will probably choose our unique DCD-1. It offers many of the features of our bigger systems, yet it will fit inside a five-inch cube.

The cartridge alone measures just 2.4 x 3.2 x .5 inches.

See for yourself.

Send us the coupon. There's much more we can tell you about our drive systems.

Study the information carefully.

If your computer isn't smart enough to choose our drive systems, we'll bet you will be.

Send me more information.

Name ______ Title ______

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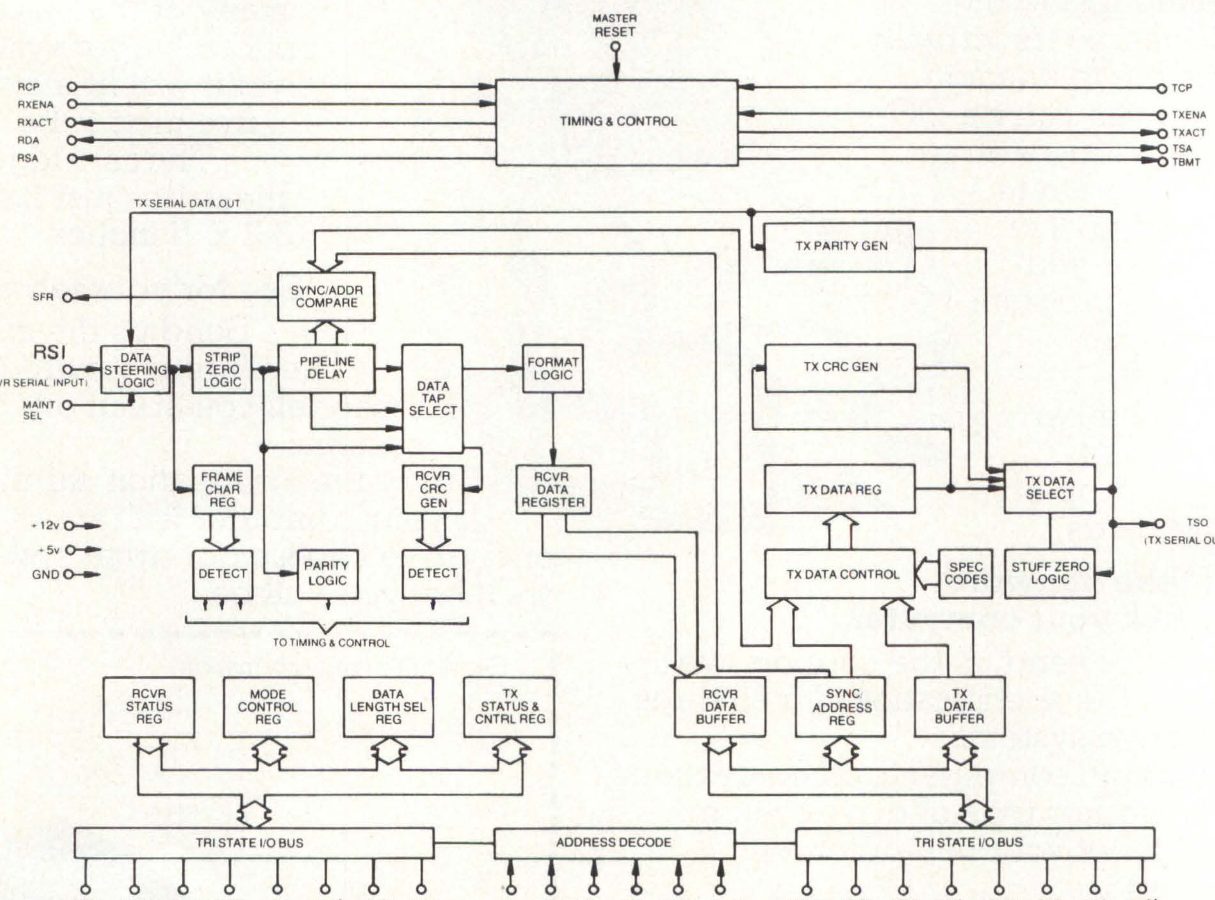
technology trends

LSI device allows bit, byte protocols

Because of the growth of distributed network computing, data communication requires protocols of increasing sophistication. These protocols supervise the signalling, switching and processing activities associated with distributed networks. Two general types of protocols-bit-oriented and byte-oriented-handle these activities.



This block diagram shows the internal structure of SMC's COM 5025 multi-protocol device.

In byte-oriented protocols, such as BiSync, each data byte carries its own overhead. In addition to data, every byte contains a start bit, a parity bit and a stop bit.

Bit-oriented protocols such as SDLC efficiently transmit large blocks of data. A standard format uses the first eight bits as a start flag, followed by address and control fields. The data follows these fields without any further protocol information until a 16-bit cyclic redundancy check arrives. A stop flag terminates the transmission.

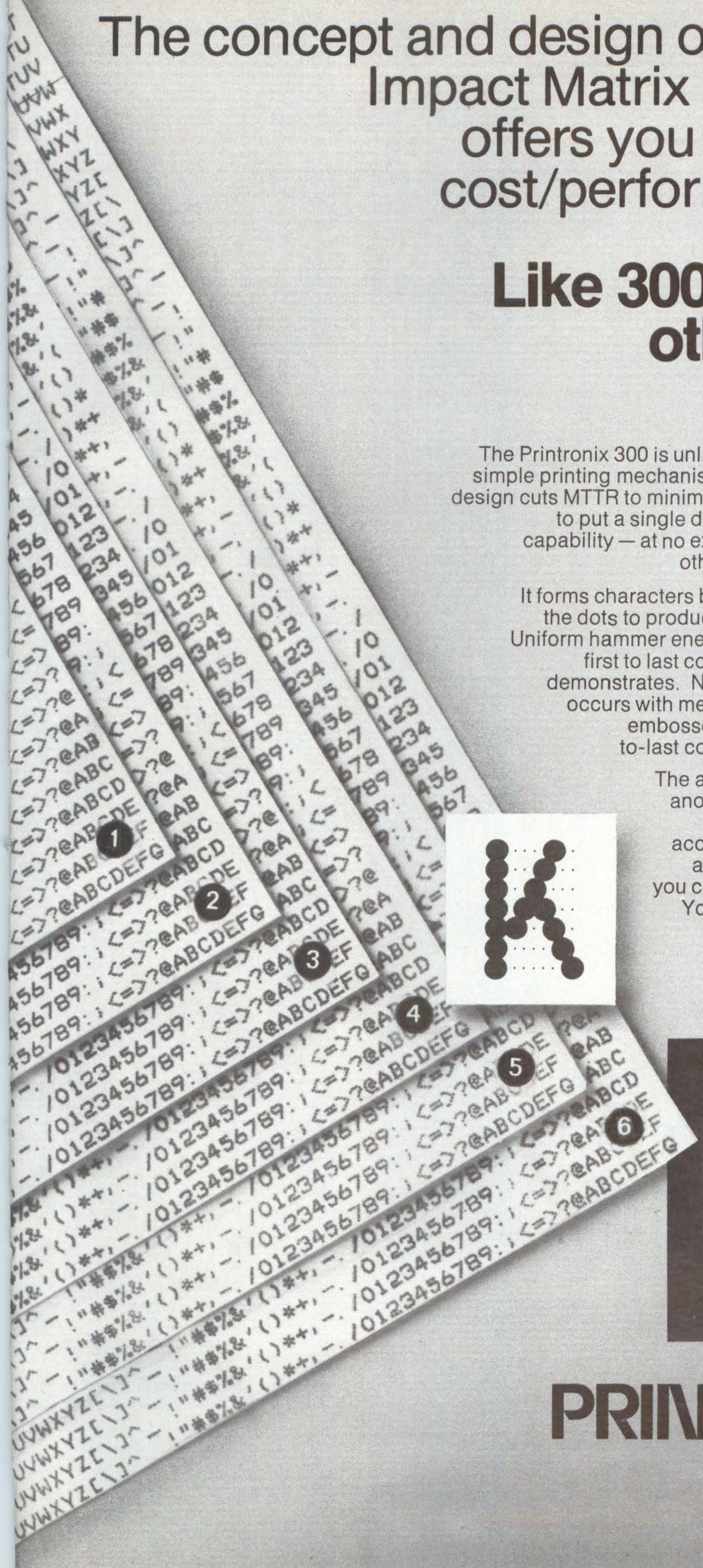
Interfacing digital systems to synchronous data communication channels previously required complex, cumbersome logic. Protocol handlers, often as complex as microprocessors, sometimes used as many as 330 chips.

Developed by Standard Microsystems Corp. of Hauppauge, NY, a multi-protocol controller, the COM 5025, operates at speeds to 2 Mbaud. This single-chip device handles most available protocols, including SDLC and BiSync.

The device controller handles all higher level decisions and interpretation of some fields within the message frame. Peter Zimbelmann, Vice President of Engineering for SMC, points out that the chip hooks up a processor to a data link, and performs many of the overhead functions that the processor normally handles, freeing the processor to do calculation or data processing. In this way, he says, "the processor doesn't have to worry about 'handshaking' requirements involved in sending or receiving messages."

For byte-oriented protocols, the chip provides automatic detection and generation of sync characters, error checking, variable length data capacity, variable sync characters, deletion of leading sync characters after synchronization and an idle mode to transmit

The concept and design of the Printronix 300 Impact Matrix Line Printer/Plotter offers you several remarkable cost/performance advantages.



Like 300 lpm print quality others can't match.

The Printronix 300 is unlike any other impact matrix printer. Its elegantly simple printing mechanism gives it a greater MTBF than others. Modular design cuts MTTR to minimize downtime. And the basic concept enables it to put a single dot anywhere on the paper, providing full plotting capability — at no extra cost — plus print quality unattainable by any other line printer. All-in-all, it's rather remarkable.

It forms characters by printing one dot row at a time. And it overlaps the dots to produce a solid appearing character, as shown below. Uniform hammer energy dot-by-dot produces clear, crisp dots on the first to last copy of a six-part form, as the actual form pictured demonstrates. No ghosting, smearing or misregistration as often occurs with mechanical font drum/chain/belt printers. And no embossed periods or faint "W"'s, either. Just clear, first-to-last copies. After all, printing ought to be easy to read.

The ability to form characters one dot at a time yields another advantage. Simply by plugging in different ROM sets, optional character styles can be accommodated. Various foreign language sets are already available, such as Katakana and Farsi, or you can easily program your own. Send for literature. You'll learn why it prints so well, why it's your best buy, and why we've felt comfortable offering a one-year warranty from the beginning.

Printronix Inc., 17421 Derian Ave., Irvine, California 92714. (714) 549-8272.

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It's your best buy!

Adtech Power Supplies cost about the same as the others.

But they're guaranteed for 6 years, while 1 to 2 years is typical.

Here's why.

3 Day Delivery . . . 6 Year Guarantee!

Single Output Microcomputer Power Supplies.

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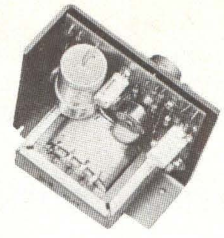

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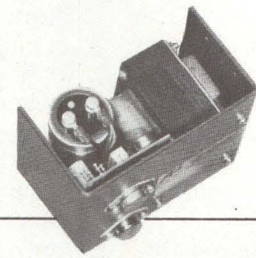
APS 6-2.5	6	2.5	±0.05%	±0.1%	3mV	OV1-63	5-9	33.15	6.90
APS 12-1.6*	12	1.6	±0.05%	±0.1%	3mV	OV1-122	10-24	32.20	6.70
APS 15-1.5*	15	1.5	±0.05%	±0.1%	3mV	OV1-152	25-49	30.70	6.40
APS 20-1	20	1.0	±0.05%	±0.1%	5mV	OV1-201	50-99	29.20	6.05
APS 24-1*	24	1.0	±0.05%	±0.1%	5mV	OV1-241	100-249	27.00	5.70
APS 28-0.8*	28	0.8	±0.05%	±0.1%	5mV	OV1-281	250-499	25.20	5.25

30 TO 60 WATT "GREEN HORNET" SERIES. †U.L. Recognized (File No. E58512)

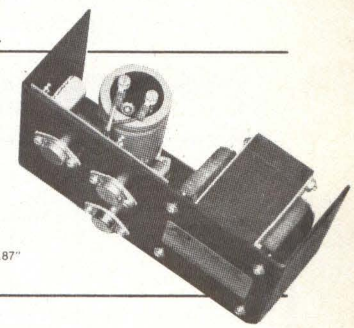


DIMENSIONS: 5.62"x3.40"x4.87"

MODEL NUMBER	RATING		REGULATION		OVP MODEL SUFFIX	POWER SUPPLY PRICES			OVP PRICES
	Vdc	Amps	Line	Load		QTY	APS 48-1	ALL OTHERS	
APS 5-6†	5	6.0	±0.05%	±0.1%	OV2-56	1-4	68.00	55.00	15.00
APS 6-5	6	5.0	±0.05%	±0.1%	OV2-65	5-9	66.70	53.65	14.85
APS 12-4†	12	4.0	±0.05%	±0.1%	OV2-124	10-24	64.75	52.10	14.40
APS 15-3†	15	3.0	±0.05%	±0.1%	OV2-153	25-49	61.75	49.65	13.75
APS 20-2.4*	20	2.4	±0.05%	±0.1%	OV2-203	50-99	58.75	47.25	13.05
APS 24-2.2*†	24	2.2	±0.05%	±0.1%	OV2-245	100-249	55.15	44.35	12.25
APS 28-2*†	28	2.0	±0.05%	±0.1%	OV2-284	250-499	50.75	42.00	11.30
APS 48-1*	48	1.0	±0.05%	±0.1%	OV2-481	500-999	49.60	40.00	11.05

* RIPPLE: (PK/PK) 5mV. All others 3mV.

50 TO 120 WATT "BLACK BEAUTY" SERIES. *U.L. Recognized (File No. E58512)

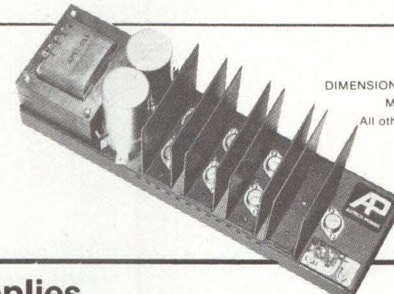


DIMENSIONS: 9"x3.65"x4.87"
APS 5-18 DIMENSIONS: 14"x3.65"x4.87"

MODEL NUMBER	RATING		OVP MODEL SUFFIX	POWER SUPPLY PRICES					OVP PRICES
	Vdc	Amps		QTY.	APS 5-9	APS 5-12	APS 5-18	ALL OTHERS	
APS 5-9	5	9	OV2-510	1-4	71.00	85.00	108.00	75.20	15.00
APS 5-10*	5	10	OV2-510	5-9	68.75	82.95	104.50	73.40	14.85
APS 5-12	5	12	OV2-512	10-24	66.74	80.55	101.45	71.30	14.40
APS 5-18	5	18	OV2-518	25-49	63.90	76.80	96.70	67.95	13.75
APS 12-7*	12	7	OV2-127	50-99	61.05	73.00	91.95	64.60	13.05
APS 15-6*	15	6	OV2-156	100-249	57.30	68.55	86.35	60.65	12.25
APS 24-5*	24	5	OV2-245	250-499	52.75	65.00	79.45	55.80	11.30
APS 28-4*	28	4	OV2-284	500-999	51.60	57.90	77.70	54.60	11.05

REGULATION: LINE +0.05% Load +0.1%. RIPPLE (PK/PK): 3mV on 5, 12, 15V models. 5mV on 24, 28V.

125 TO 250 WATT "BLUE MAX" SERIES.



DIMENSIONS: 16.72"x4.87"x6.60"
Max. APS 5-30 only.
All others 16.72"x4.87"x5.75"

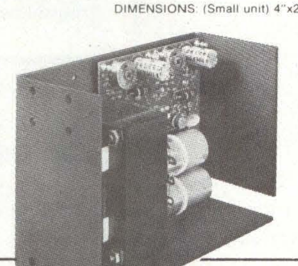
MODEL NUMBER	RATING		REGULATION		OVP MODEL SUFFIX	POWER SUPPLY PRICES			OVP PRICES
	Vdc	Amps	Line	Load		QTY	APS 5-30	ALL OTHERS	
APS 5-25	5	25	±0.05%	±0.0.1%	OV3-525	1-4	163.00	158.00	25.00
APS 5-30	5	30	±0.05%	±0.0.1%	OV3-530	5-9	159.25	154.40	24.50
APS 6-22	6	22	±0.05%	±0.0.1%	OV3-622	10-24	154.65	149.95	24.25
APS 12-17	12	17	±0.05%	±0.0.1%	OV3-1217	25-49	147.45	142.95	23.15
APS 15-15	15	15	±0.05%	±0.0.1%	OV3-1515	50-99	140.20	135.90	22.00
APS 20-11	20	11	±0.05%	±0.0.1%	OV3-2011	100-249	131.65	127.60	20.65
APS 24-10	24	10	±0.05%	±0.0.1%	OV3-2410	250-499	121.10	117.40	19.00
APS 28-9	28	9	±0.05%	±0.0.1%	OV3-289	500-999	118.50	114.85	18.60

RIPPLE (PK/PK): 3mV on 5.6.12.15V models. 5mV on 20.24.28V models.

New Multiple Output Microprocessor Power Supplies.

DUAL OUTPUT MICROPROCESSOR SERIES U.L. Recognized (File No. E58512)

DIMENSIONS: (Small unit) 4"x2.75"x4.87" (Large Unit) 7"x3.40"x4.87"

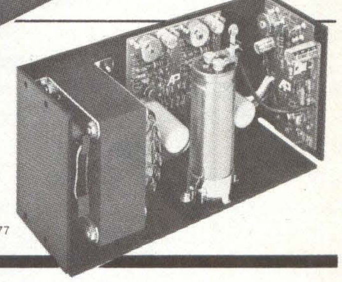


REQUEST BULLETIN DAPS - 976

MODEL NUMBER	RATING		QUANTITY PRICES						
	Vdc	Amps	1-4	5-9	10-24	25-49	50-99	100-249	250-499
DAPS 5.8	±5	0.8	43.00	41.95	40.70	39.80	38.00	36.80	33.00
DAPS 9-12.5	±9-12	0.5	43.00	41.95	40.70	39.80	38.00	35.80	33.00
DAPS 12-.75	±12	0.75	43.00	41.95	40.70	39.80	38.00	35.80	33.00
DAPS 15-.60	±15	0.06	43.00	41.95	40.70	39.80	38.00	35.80	33.00
DAPS 5112.5	+5 -12	1.0 0.5	43.00	41.95	40.70	39.80	38.00	35.80	33.00
DAPS 12-1.5	±12	1.5	59.00	57.60	55.90	53.30	50.65	47.60	43.80
DAPS 15-1.3	±15	1.3	59.00	57.60	55.90	53.30	50.65	47.60	43.80
DAPS 53121.5	+5 -12	3.0 1.5	59.00	57.60	55.90	53.30	50.65	47.60	43.80

REGULATION: +0.05% Line, +0.1% Load. RIPPLE (PK/PK) 3mV.

TRIPLE OUTPUT "TAPS" MICROPROCESSOR/GENERAL PURPOSE SERIES



DIMENSIONS:
8.62"x3.65"x4.87" to
15"x4.5"x4.87"

REQUEST BULLETIN TAPS - 377

MODEL NUMBER	RATING		QUANTITY PRICES						
	Vdc	Amps	1-4	5-9	10-24	25-49	50-99	100-249	250-499
TAPS 1	5V ±9-12*	4.0 0.5	94.15	91.85	89.20	85.05	80.85	75.90	71.00
TAPS 2	5V ±9-12*	6.0 1.0	107.00	104.60	101.60	96.85	92.10	89.00	87.50
TAPS 3	5V ±9-12*	9.0 1.5	137.00	134.00	129.80	127.80	125.00	123.75	113.85
TAPS 4	5V ±9-12*	12.0 3.0	163.00	159.00	154.45	151.50	149.00	148.00	147.00

* Also available with +12-15V output. Specify if desired. REGULATION: +0.1% Line, +0.1% Load. RIPPLE (PK/PK): 5mV

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CIRCLE 10

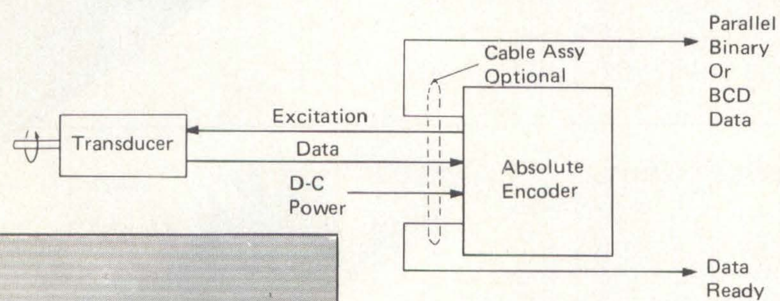
sync characters to mark the line.

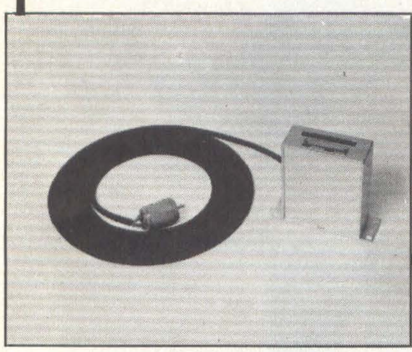
For bit-oriented protocols, the device performs bit stuffing, automatic frame character detection and generation and residue handling. Options for bit protocols include variable length data, error checking, primary or secondary station address mode and idle mode to transmit flag characters or mark the line. Zimbelmann explains that the ability of this device to handle different protocols "allows you to glue a processor into almost any system in use or being designed for future use." For further information write Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, NY 11787 or call (516) 273-3100.

Adjustable concrete-mix scale-encoder handles special codes

An adjustable scale encoder allows Erie Strayor Company of Erie. Pa. to standardize on a single electronic device to interface with minicomputers in the their complete range of batch plants. The shaft encoder converts ingredient weights to digital signals, and handles different weight ranges using chip plug-in modules.

Developed for this application by Astrosystems, Inc., Lake Success, N.Y., the encoders also handle unconventional codes to accommodate a 343° full-scale turn instead of 360°, or other special scale factors.





The diagram shows that this encoder (left), used for interfacing minis in automated batch plants, contains both transducer and electronics.

Erie Strayor makes automated batch plants in capacities from 1,000 to 60,000 lbs. "We would have needed 15 different encoders, one each for our 15 different plant capacities," says Jerry Reilly, Erie Strayor design engineer.

"Now," Reilly explains, "we have a single encoder with 15 different chips or plug-in modules, and 15 different scale charts for mounting on the encoders. Whatever size batch plant is ordered, we use exactly the same encoder, selecting the chip that's compatible with that size plant and the right dial chart. This has simplified our design tremendously, and also keeps parts and replacement inventory to a minimum." Erie Strayor concrete-mix plants are available in fixed and portable models. They are computer-controlled to batch the ingredients and feed them to either a fixed or portable station.

The concrete ingredients are stored in hoppers. They include sand, stones of several sizes, various types of cements, water, ice and admixtures. A minicomputer controls hopper flow. On demand, ingredients are weighed by conventional scales with mechanically connected encoder transducers. The encoder converts scale values to digital signals; these signals are then transmitted to the minicomputer. The computer checks weights against preset values and issues feed commands if the values are correct.

The scales rotate approximately 343° instead of 360° for every 1000 lbs., requiring an unconventional code count capacity in the encoders.

Allowing both span and offset adjustability, and using plug-in modules, the encoder can be scaled in 1,000 count increments up to 8,000 counts. This is achieved by modifying the full scale count by means of integral factors through the use of wired program plugs. As a result, the same electronics can be used in systems that vary in full scale values.

Because the scales in the Erie Strayor batch plants rotate only 343°, conventional codes such as 1000, 1024 and 2000 counts per revolution are not used. Instead, the encoder provides such counts as 1050 per rev, with an added ±5 counts field adjustable.

A conversion scheme that depends upon the synchronous frequency ratio of two signal sources gives the code count. The ratio is varied over a wide range, permitting full scale encoder counts not found in standard units.

The basic encoder consists of a magnetic transducer and an electronics package. The rotating shaft of the magnetic transducer is the only moving part of the encoder.

The transducer is not affected by temperature, shock, vibration or atmospherics. It is insensitive to noise pickup on the lines. These features allow it to be incorporated in machinery in manufacturing or processing environments without fear of damage or loss of operating characteristics. The electronics package contains circuitry to convert the transducer's shaft position to digital data for use by the minicomputer.

There are two printed circuit boards in the electronics package: a generator board and a receiver board. The generator board provides two-phase excitation signals to the transducer. A high frequency clock enables the receiver board to digitize the angle position information in the transducer signal.

The electronics package provides a data-ready pulse when data is updated and ready for use by external equipment. The pulse synchronizes operation of external equipment.

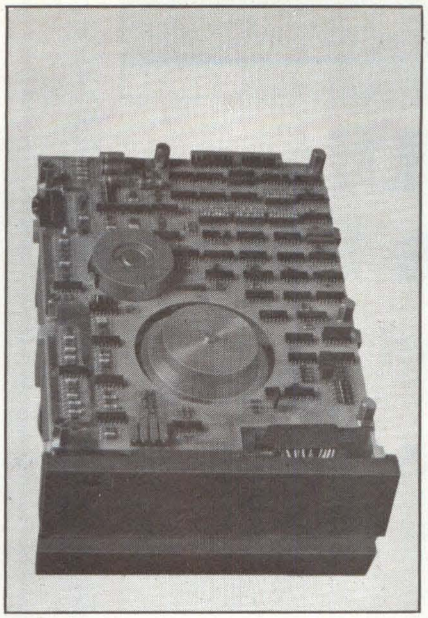
The encoder provides + 5 VDC output, suitable for interfacing with standard printers, numerical displays and computers. To assure maximum noise immunity and to eliminate "zeroing," outputs are absolute rather than incremental. If power is lost, the correct output is immediately present upon restoration of power. Sudden accelerations cannot cause loss of correct output by exceeding the "counting" speed of the unit. "We had some adjusting to do ourselves with this new encoder," says Reilly, "but once we got the bugs out, we realized that we had successfully achieved an encoding method that simplifies design and inventory, while linking up directly with our minicomputer control system."

Small double-sided double density disk

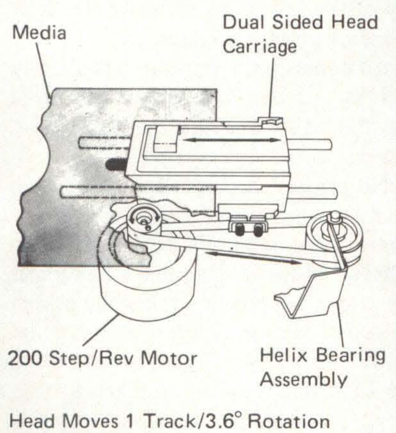
MFE unveiled its Mayflower (700-750) line of IBM compatible flexible disc drives at NCC in June with what they said is the smallest (8.70" x 4.35" x 12"), double sided, double density floppy disk. It uses a proprietary "Heli-Band" TM head positioning system which translates 3.6^0 (2 steps) of rotary stepper motion to one full track of head travel, at track-to-track travel times of 3 ms.

Mayflower is available with either a center mounted brushless DC spindle drive motor or a corner mounted AC motor. MFE offers a wide range of options meeting most OEM needs. Other basic features include: Data Transfer rates of 250K bits/second/side; a packing density of 3400/6800bpi; 77 tracks per side at 48 tracks/inch and easy, positive media loading. Standard options include: Activity lights; DIP switch drive select for daisy chaining; write fault reset, radial ready; radial index sector; separated data and separated clock; sector outputs; and a wide range of head select options.

For complete technical data and prices contact Mr. Jim Bartley at (603) 893-1921 or MFE Corporation, Keewaydin Drive, Salem NH 03079.



AC spindle drive, housed in a small frame, uses floppy disks.



The head carriage mechanism utilizes dual ceramic read-write heads and ceramic head load pads. This eliminates trouble-prone felt pressure pads and extends head life to more than 4×10^7 wear revolutions.

Altering keyboard's interconnection scheme trims calculator design

In recent years, the interconnections between calculator keyboards and their mother-boards have become nearly as expensive as the keyboards themselves, claims Hank Boulanger, an engineering manager at Texas Instruments' Control Products Div. in Attleboro, MA. To reverse this inflationary trend, Boulanger and his colleagues in the division's Data Controls Dept. have designed an alternative keyboard in which the contacts beneath each key consist simply of a series of parallel wires. At the same time, the engineers have modified their calculator manufacturing process to produce keyboard switches in strips rather than as individually assembled units.

Boulanger credits the revised production technique and the simplified interconnection scheme with cutting keyboard costs for high-volume users roughly in half. In 100,000-piece volumes, TI's modified keyboards cost four cents each; in higher quantities, even less.

Though originally designed for calculators like the TI 1200, 1250 and comparable models, the keyboards also suit other consumer products like credit-card verifiers, telephone data handling equipment and electronic games.

TI offers the keyboards in 20, 24 and 28 position standard versions with 0.5 x 0.562 key spacing. The company also provides a 40-position standard version with 0.5 x 0.4 key spacing. A

20-position board measures 2.4" x 2.95"; a 24-position board, 2.4" x 3.512".

Simplified contacts. To minimize the cost of each version, Boulanger and his associates have based their keyboard design on what they term "X-Y matrix" technology. In this design, strips of switches arranged in rows form the X direction of the keyboard's matrix, while wires measuring 0.07" in diameter form the Y direction. One wire lies beneath each switch and runs at right angles to the rows of switch strips.

Another set of wires, running parallel to the contact wires, lies between the switch columns and are electrically connected to the disk strips. Both these and the contact wires emerge at the top of the keyboard to form a leadframe or umbilical. Thus, the TI keyboard comes with an umbilical already built in – a feature that lets users insert the lead wires into the motherboard.

No printed circuits. Boulanger also credits the keyboard's relatively low cost to his company's manufacturing process. In the TI calculator keyboard, the integral leadframe takes the place of a costly printed circuit board. Thus, unlike most other keyboards of its type, the TI device requires no plating.

To manufacture the device, the company continuously feeds wires from one end of its processing equipment and disk strips from the other end. As the contact wires advance through the processing equipment, they pull the keyboards with them. When the boards reach the end of the processing machine, they are cut into equal lengths like taffy. The machine then welds the switch strips in place and attaches the calculator cover.

TI makes the switch strips at a separate station, feeds them in continuous reels and cuts them as they are assembled on the keyboard, Boulanger adds. Every switch in a strip functions independently and the carrying frame serves as an electrical circuit element. Each switch in a given row, therefore, is electrically common.

In the final production step, the company simultaneously flow-solders the keyboard and the MOS chips to the motherboard. With most other keyboards, calculator manufacturers usually must flow-solder a connector to the motherboard before attaching the keyboard. The TI process, however, has eliminated this intermediate step and thus the associated production expense, Boulanger claims.

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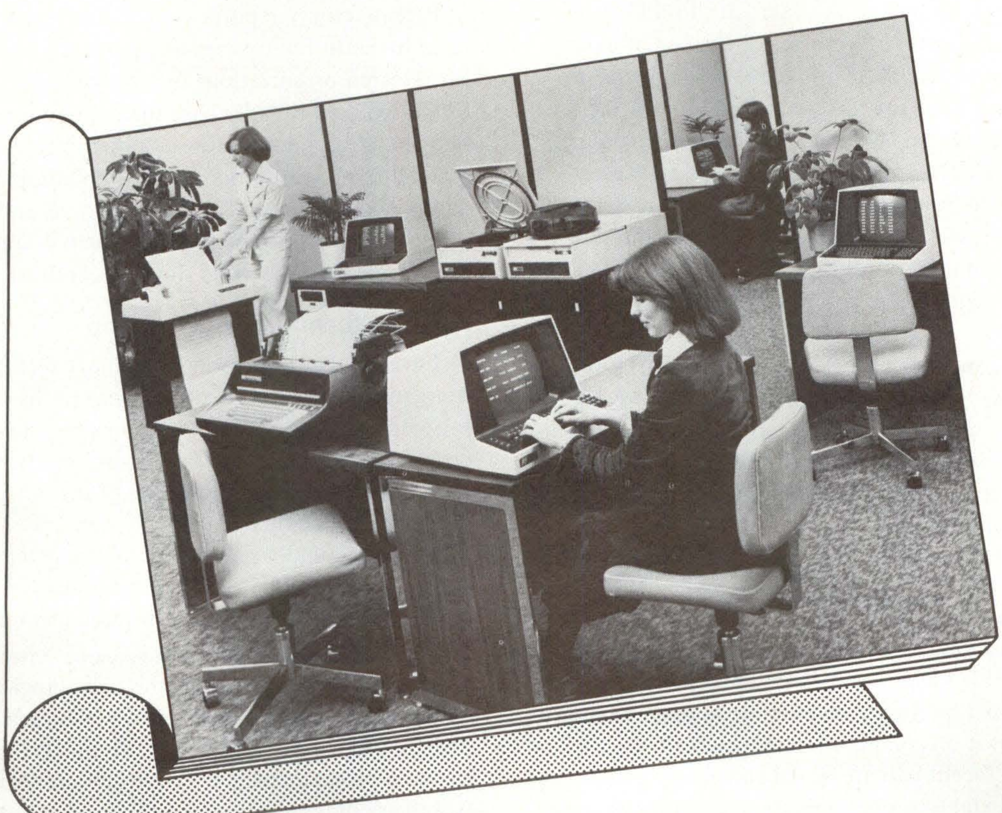
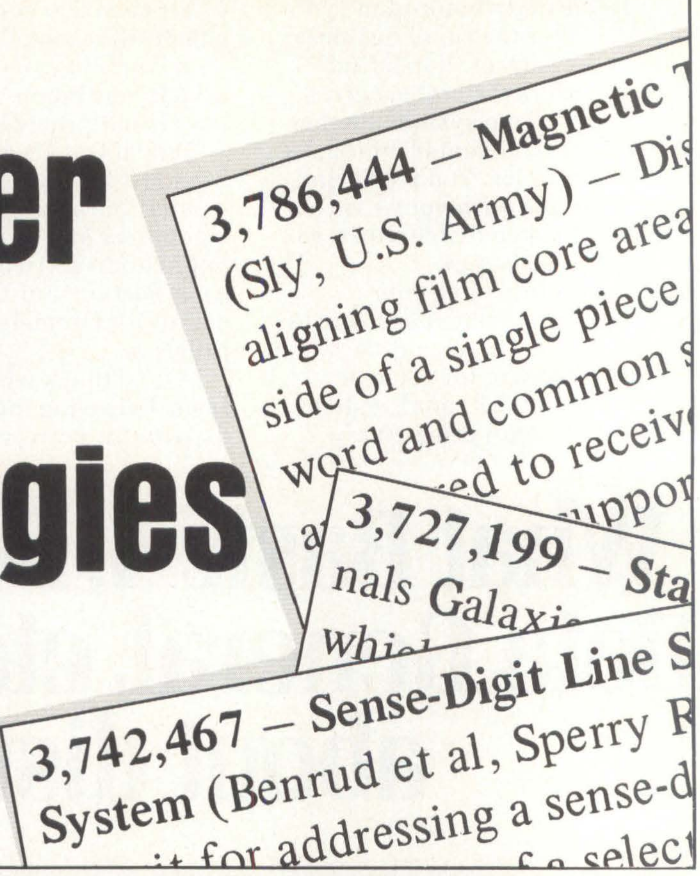


CIRCLE 17

BENWILL TECHNOCAST REPORT

PART I: Computer Memory Technologies

A State-of-the-Art and Patent Activity Analysis



The innovation analysis, state-of-the-art trends and patent activity we present here provide useful information to more corporate individuals than the design engineers who dream up the innovations and the systems designers who incorporate them into improved products. It should help design managers who worry about the directions of a particular segment of an overall technology, the financial managers who plan the expenditure of R&D funds, the researchers and developers who decide on what and where to spend those funds, the marketing and sales managers who have to sell the resulting product in competitive marketplaces and the users who need assurance that the products and components they specify for their OEM system won't be obsolete before the equipment leaves the production floor.

In essence, the manner of presentation is one from which you can obtain with ease the kind of information you need – regardless of your corporate function or interest – about any of the technologies we present in this and future issues. In that sense it represents a different kind of reporting function that we hope you'll find useful: US and foreign patent activity, brief summations of the innovations, corporate ownership, notes on activity and growth and decline of interest in different segments of a technology.

We started this kind of coverage last May with a report on Magnetic Bubble Memories (omitted here) and presented a short form report on floppy disc and drive patent activity in July. This report on computer memories defines each type, reports on recent patents issued and charts patent applications and grants as one measure of technology trends and thrusts. Memories covered are charge coupled devices, semiconductor, magnetic core, magneto-optical, optical, holographic, superconductive, ferroelectric, cathode ray tube, plated wire, planar film and domain tip propagation.

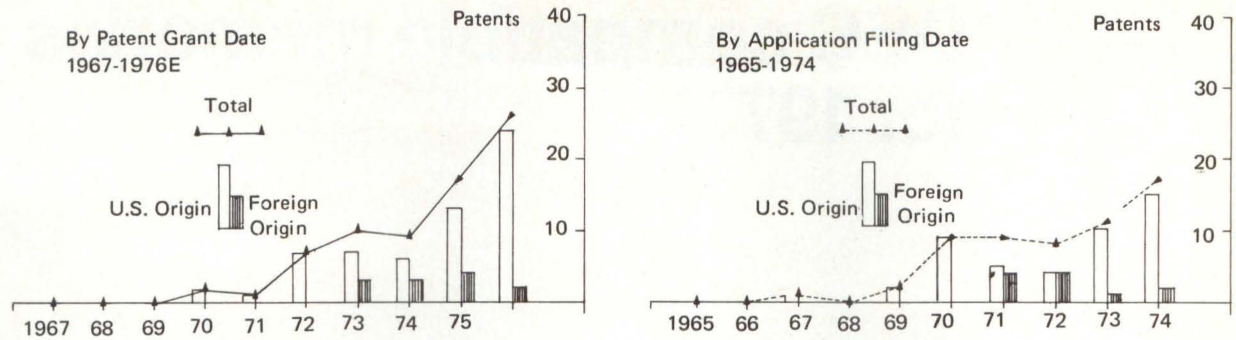
Patent activity reports such as we present here cannot replace in-depth forecast reports normally provided by market research organizations that provide more extensive information on a broader base than patent activity information alone can provide. These in-depth forecasts, however, generally cost many thousands of dollars and are affordable only by governments, large corporations and research organizations. Reports of this type may help you determine the extent to which you need more in-depth data.

memory technology ownership

Firms obtaining patents in memory technologies vary from among the largest corporations in the world to very small companies with one or two patents in the field. Approximately 450 different corporations obtained at least one patent since 1969, but most of the patenting is done by relatively few companies. For example, the top 25 companies (6%) account for 30.0% of all the patenting in this area. The top nine firms (2%) alone account for 22.0%, over one fifth of all the patenting in static memory systems.

This report concerns the ownership pattern of these nine largest firms in some of the technological areas considered in this report. The results are expressed as the percent share of all patents within the technology; the data is analyzed on broad levels – magnetic and nonmagnetic areas – as well as component and subcomponent levels.

Figure 1 Country Distribution of Charge Coupled Device Memory Patents



	By Patent Grant Date 1967	68	69	70	71	72	73	74	75	76E	Total 67-76E	By Patent Application Filing Date 1965	66	67	68	69	70	71	72	73	Total 65-73
Total Patents				2	1	7	10	9	17	26	72			1		2	9	9	8	11	40
United Kingdom				2	1	7	7	6	13	24	60			1		2	9	5	4	10	31
Total Foreign							3	3	4	2	12							4	4	1	9
United Kingdom									1	2	3								1	1	2
Japan							1	1	1		3							1	1		2
France							1	1			2							1	1		2
Netherlands									2		2							1			1
Germany								1			1								1		1
Italy							1				1							1			1

The most dominant firm in these areas in terms of total number of patents obtained was the International Business Machine Corp., followed by Bell Telephone Laboratories Incorporated, Sperry Rand Corp., RCA Corp., General Electric Corp., U.S. Phillips Corp., Siemens Aktiengesellschaft, Burroughs Corp. and Honeywell Inc.

These firms do not all have similar interests. Note the differences in the patents in specific areas. While IBM owns most of the nonmagnetic memory patents, Bell Telephone Laboratories owns most of the magnetic area patents. BTL is most dominant in the magnetic film area and particularly in magnetic bubble type memories, owning 48% of all these patents. IBM leads in all other areas shown in Table A except charge coupled device memories, in which the General Electric Corp. is the leading patent holder.

charge coupled device memories (CCD)

The basic charge coupled device, a species of an analog shift register, is a semiconductor device in which an applied electrical field induces potential minima for signal charge packets at storage sites at or near the surface of the semiconductor material. Varying the applied electric field shifts the potential minima to adjacent storage sites, transferring the signal charge in a controlled manner within the semiconductor substrate from storage site to adjacent storage site in serial fashion. Appropriate manipulation of the imposed electrical field recirculates, stores or delays the signal charges in their movement through the substrate. Thus, electrical signal charges, representing information, can be generated (read in), translated (moved or shifted) and retrieved (read out).

Patent applications to charge coupled device memories first began to appear in 1967. Since then this technology has experienced rapid growth, especially in the three year period, 1974-76 (estimated), during which 71.4% of the patents in the technology were issued. Fig 1 illustrates this growth by patent grant date and the application filing date of these patents.

In terms of numbers of patents granted, the U.S. is the clear leader in CCD memories. Over the period 1974-76 (estimated), only 18% of all U.S. patents in the area have been granted to foreign residents. This amount is about half the technology foreign share average of 35.4% for the same period for all kinds of memories patented. Table 1 shows, by patent grant date and application filing date of these patents, the country distribution of the patents granted for CCD memories.

Technology Concepts

The original Boyle and Smith concept (patent no. 1 in Table 1) appeared in The Bell System Technical Journal in April 1970, pp 587-93. Fig 2 illustrates a portion of it diagrammatically. It is composed of a semiconductor substrate of n-type silicon that carries a thin insulating film of silicon oxide on which nine metal electrodes are placed in succession. In these devices the electric field is generally supplied by clock potentials of different time sequences applied to electrodes. Two-phase CCD devices have electrodes in groups of two with alternate electrodes connected to the same phase clock line. Three- and four-phase devices have three and four electrode groups with alternate electrode groups connected to the same phase clock line. In each case the electrode group constitutes one storage element or one bit of information. Fig 2 explains the operation of a three-phase group configuration.

The charge introduced at the input to the CCD is generated by forward biasing of a p-n junction located in front of the string of electrodes. Charge input can also be produced by surface avalanching or by radiation-induced pair creation. Detection at the output of the CCD is obtained by current detection with a reverse biased p-n junction or Schottky barrier diode. For shift register operation in a

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16K words in a single quad slot (2 option slots)

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2. Burst refresh mode. (DEC method)

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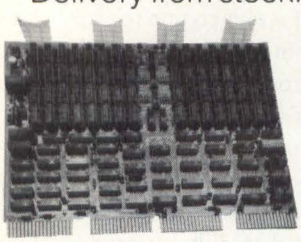

MSC 4501
January

CIRCLE 60

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Requires 75% less power than equivalent core memories (8K words requires only 0.6A at +5 volts DC).

Nonvolatile, 8K words fits in a single OMNIBUS® slot.

Totally PDP-8 A, E, F or M hardware and software compatible.

One year warranty on parts and labor.

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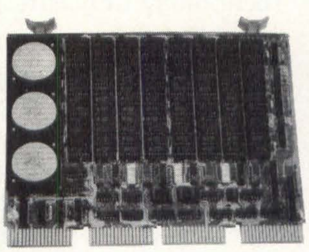


MSC 3201
February

CIRCLE 61

PDP-11/04/34 Memory

Up to 64K words, with or without parity, in a hex wide "SPC" slot.

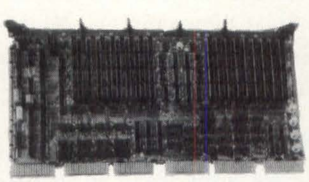
Totally PDP-11/04/34 hardware and software compatible.

Expandable in 4K increments to 16K words, and in 16K increments to 64K words.

One year warranty on parts and labor.

$1495* (16K words) single quantity. OEM discounts available.

Delivery from stock.



MSC 3501
March

CIRCLE 62

PDP-11 Extended Memory Unit

Up to 2.8 megabytes, with parity, in a 10½" high rackmount chassis (includes power supply and forced air cooling).

Expandable in 512K byte increments to 4 megabytes.

Faster than RF-11/RS-11— 2.1μsec. access time, 1 μsec. transfer rate, selectable.

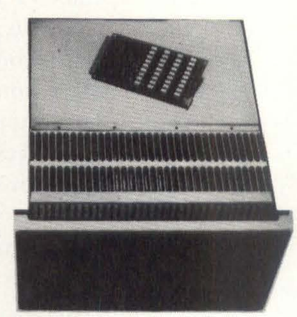
More reliable than disk or comparable core memory.

Nonvolatile with available battery backup.

PDP-11/04 through 70 hardware and software compatible.

One year warranty on parts and labor.

Delivery 45 days ARO.



MSC 3601
April

CIRCLE 63

PDP-11/70 Memory

Up to 2.0 megabytes, with error correction and detection, in a 10½" high rackmount chassis (includes power supply and forced air cooling).

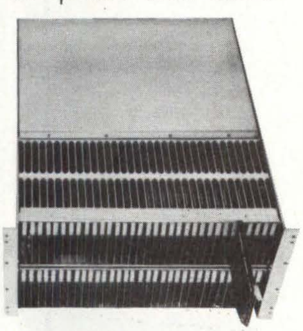
Expandable in 64 kilobyte increments to 3,932,160 bytes. (Max. PDP-11/70 capacity.)

High speed performance utilizes PDP-11/70 memory bus at maximum data rate.

Nonvolatile with available battery backup.

PDP-11/70 hardware and software compatible.

One year warranty on parts and labor.



MSC 3602
May

CIRCLE 64

LSI-11 Dual Height Memory

Up to 32K words in a single option slot.

Available in 4K, 8K, 16K, 24K, 28K, and 32K word configurations.

Available with either on-board, distributed refresh or external refresh.

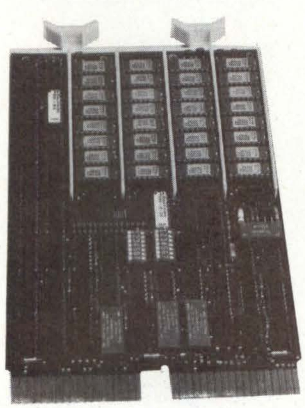
Addressable in 1K word increments.

Provision for battery backup.

Totally LSI-11 hardware and software compatible.

One year warranty on parts and labor.

Delivery from stock.



MSC 4601
June

CIRCLE 65

PDP-11 Add-on Memory

Up to 128K with parity in a 5¼" rackmount chassis (includes power supply and forced air cooling).

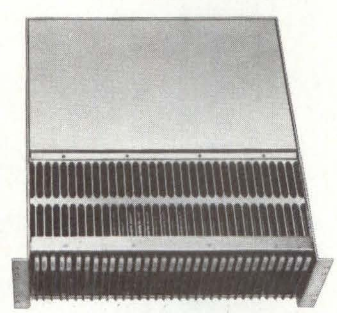
Totally PDP-11/04 through 55 hardware and software compatible.

Optional dual port operation with two CPU's, one at a time or simultaneously.

One year warranty on parts and labor.

$4810*(64K words) single quantity. OEM discounts available.

Delivery from stock.



MSC 3302
July

CIRCLE 66

On being first

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typical memory the output is recirculated to the input.

Thrust of Technology

One important criterion by which computer memories are judged for commercial effectiveness is access time. The access or latency time is defined as the time required to access any bit of information in a memory matrix. Since CCD is a serial memory device, access to a given bit of information usually requires a relatively long latency time. However, the access time depends heavily on chip organization and can be varied over rather wide limits. For this reason, a major impetus in patent activity is geared towards chip organization.

A typical chip organization (patents 2 and 3 of Table 1) is a serial-parallel-serial (SPS) configuration. The information is written into a series register and then transferred simultaneously or multiplexed onto parallel paths from which the information is selectively loaded into charge storage elements. The information is then selectively read out of the storage elements, transferred into parallel paths and then transferred into a series output register. Variations of the basic SPS configuration have been investigated, for example, a dual SPS memory (patent 5) where means are provided to inject time samples of input signal alternately to two shift registers and to multiplex the outputs therefrom.

To achieve higher densities for CCD memories, circuit topology becomes an important consideration. High bit densities are available by alternately storing input and output bits at even and odd numbered storage electrodes of the input and output register so that each storage electrode may serve a separate channel of the parallel storage section (patent 5). To permit high channel packing density in the storage matrix of an SPS memory, the output register has as few as M/N stages where M is the number of channels in the matrix and N the number of phases employed (patent 6).

Certain tradeoffs are required for efficient chip organization. For instance, longer shift registers result in longer access times but require less on chip decoding and sense regeneration circuitry. On the other hand shorter shift registers reduce access times but require more support circuitry. To promote this efficiency, a CCD stack memory having a last-in-first-out memory organization was developed (patent 7). Another memory architecture which lends itself to efficient chip organization is a circulating memory in which the memory stream of data that is circulating can be modified at will (patent 8). Another improvement to CCD memories is to use two phase clock signals (patents 9 & 10). This makes it easier to fabricate the shift register and allows for greater density. The two phase clock capability is achieved in part through the use of overlapping gate electrodes and non-uniform insulator thickness (patent 11).

A major problem in CCD memories is keeping the charges shifted and stored at proper charge levels. Signal charges tend to deteriorate as they pass through a register, and a logic 1 can become a logic 0. To prevent errors, a novel serpentine structure has been developed in which the registers of two adjacent arrays are interleaved to provide a refresh-cell width of four times the width of a single-shift register (patent 12). Another method to compensate for distortion is to provide a series of equal background pulses that are constantly circulated through the shift register at the clock rate of the register (patent 13).

Charge also has a tendency to be produced within the substrate material thereby causing erroneous signals at the register output. This problem was overcome by a recirculating memory in which integrated circuit transistors are appropriately located for draining off excess electrical charges (patent 14). Furthermore, sensing of the register output can occur physically near the power supply so that the signal becomes

Table 1 Important CCD Patents

Patent No.	Inventor	Assignee	Country
1. 3,858,232	Boyle & Smith	Bell Telephone Labs.	U.S.A.
2. 3,763,480	Wiemer	RCA Corp.	U.S.A.
3. 3,914,748	Barton & Check, Jr.	Texas Instruments Inc.	U.S.A.
4. 3,953,837	Check, Jr.	Texas Instruments Inc.	U.S.A.
5. 3,913,077	Erb	Hughes Aircraft Co.	U.S.A.
6. 3,967,254	Kosonocky & Saver	RCA Corp.	U.S.A.
7. 3,942,163	Goyal	Burroughs Corp.	U.S.A.
8. 3,889,245	Gosney, Jr.	Texas Instruments Inc.	U.S.A.
9. 3,819-959	Chang & Sumilas	IBM Corp.	U.S.A.
10.3,829,884	Borel et al	Commisariat a l'Energie Atomique	France
11.3,651,349	Kahng & Nicollian	Bell Telephone Labs.	U.S.A.
12.3,965,462	Belt	U.S. Air Force	U.S.A.
13.3,660,697	Berglund & Boll	Bell Telephone Labs.	U.S.A.
14.3,967,136	Krambeck	Bell Telephone Labs.	U.S.A.
15.3,891;977	Amelio et al	Fairchild Camera and Instrument Corp.	U.S.A.
16.3,946-368	Chou	Intel Corp.	U.S.A.
17.3,949,381	Dennard & Spampinato	IBM Corp.	U.S.A.
18.3,654,499	Smith	Bell Telephone Labs.	U.S.A.
19.3,755,793	Ho et al	IBM Corp.	U.S.A.
20.3,750,114	Valassis	GTE Automatic Electric Labs., Inc.	U.S.A.
21.3,864,550	Cragon	Texas Instruments Inc.	U.S.A.
22.3,952,290	Williams	U.S. Navy	U.S.A.
23.3,944,990	Chou	Intel Corp.	U.S.A.

Figure 2 Surface Conductor Configurations

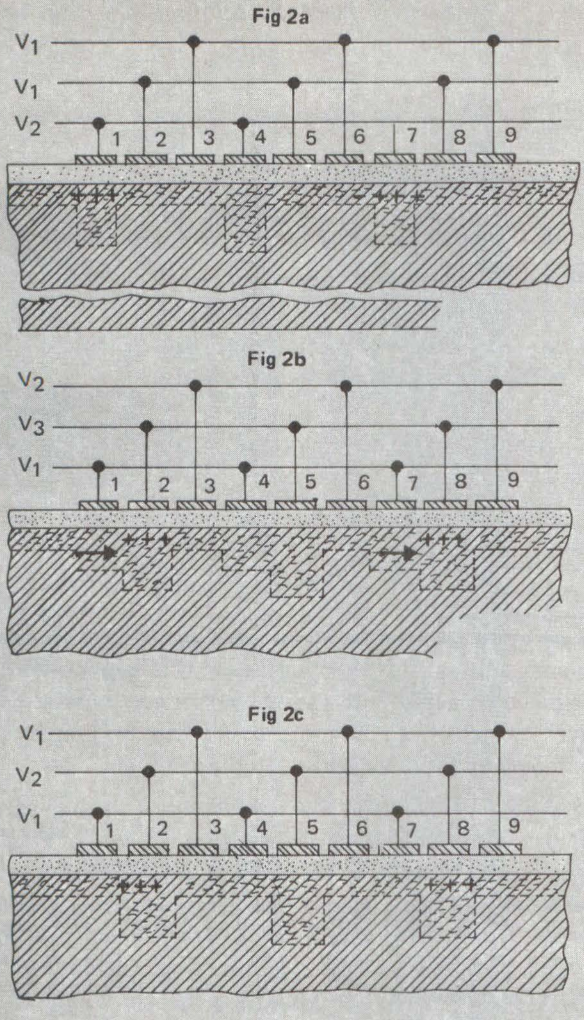


Fig 2 Electrodes shown constitute a three-phase group configuration with surface conductors interconnecting all the electrodes of one group. The clocks, which are not illustrated, serve to modify the phase of the three potentials V_1, V_2, V_3 applied to the conductors. In the case of Fig 2a depletion regions are shown beneath electrodes 1, 4 and 7 with charges present beneath electrodes 1 and 7 and no charge present beneath electrode 4. In the latter region, the semiconductor material is in a state of deep depletion; edges of the regions are indicated by the dashed lines. The logical level 1 can be assigned to the absence of charge beneath the electrode. Clocks serve to apply a potential V_1, V_2 and V_3, measured with respect to the substrate, and designated, respectively: quiescent or bias level; storage and transfer level. During storage of information beneath electrodes having the order 3a + 1, (a being a positive integer or zero) as in Fig 2a, potential values V_2, V_1 and V_3 are applied to the conductors. To initiate transfer beneath the electrodes, these potentials are brought to V_2, V_3 and V_1, increasing the absolute potential of these electrodes. The charges move from the electrodes having a voltage V_2 to electrodes having a voltage V_3 as shown in Fig 2b. Finally, the voltages are brought to respective levels V_1, V_2 and V_1, as shown in Fig 2c, which correspond to the same distribution as in Fig 2a except they are displaced by one electrode.

distorted due to interference from the power supply. To solve this problem, a plurality of charge comparison circuits were included in a CCD memory which are insensitive to voltage variation in the power supply (patent 15).

To mass produce CCD memories, one problem that must be solved is the reliable detection of memory output, both for reading information from memory and for refreshing it. Typically, the charge output of any particular CCD device will vary from one device to another due to fabrication variations, high temperature or low operating frequencies. To achieve reliability, compensation must be provided for the above problems through the use of self regulating signals which adjust the threshold of the detection circuitry so that the latter correctly senses the output of a storage CCD memory (patents 16 and 17).

CCD devices have also been devised as "read-only" memories (patent 18). In these, the charge capacity of selected sites is permanently or semipermanently fixed during manufacture. If charge is accumulated in these sites to the equilibrium amount and shifted to an output site, the signal will reflect the programmed capacity of the sites. A latent image memory which is selectively operable as either a read-write memory or a read-only memory has been developed (patent 19).

Charge coupled imaging devices have also been investigated in which CCD shift registers are coupled to light sensitive regions to store an image. For instance, one device has a light emitting diode array disposed adjacent to a CCD semiconductor device. The CCD semiconductor device is operated in a shift register mode to write binary line status information into a random access memory (patent 20). Other applications are a CCD reader capable of reading and buffer storing the data from a punched card (patent 21), and a read-only optical memory system where a multiple element photo responsive CCD is positioned to receive light energy transmitted from a mask having many discrete increments of recorded information (patent 22).

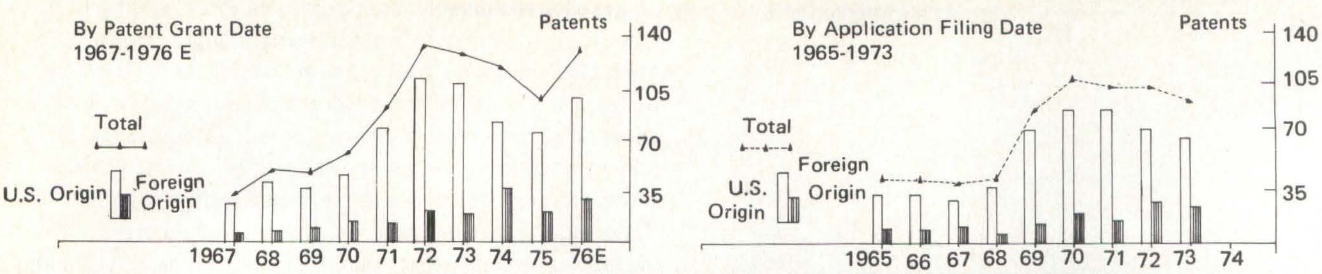
Trends in CCD Technology

Computer memory systems are organized in hierarchies in which small, fast and expensive memories are backed up by increasingly larger, slower and less expensive memories to maximize system cost effectiveness. CCD memories can find application in both central processor unit and inline bulk memories; however, it has been projected that CCD memories will be used to replace magnetic drum and disk memories where their non-volatile characteristics are not requisite. To date, 16K bit memory chips have been fabricated (patent 23), and 64K bit chips are in the development stage. CCD memories seem well on their way to firmly entrenching themselves in the present and future memory technology.

semiconductor memories

Semiconductor memories use active transistor circuits as memory cells. They are classed into two major groups: unipolar metal oxide semiconductor (MOS) and bipolar MOS. MOS random access read-write memories can be either static flip-flops or dynamic charge storage circuits. The static flip-flops typically use six transistors per bit and store information as one of two stable states. Dynamic circuits generally consist of three FET (Field Effect Transistor) cells which use the presence or absence of charge on a capacitor to store information. MOS devices are classified according to different fabrication techniques, i.e., P-channel (PMOS), N-channel (NMOS) and complementary (CMOS). Two variations of MOS fabrication technology, metal-nitride-oxide-silicon

Figure 3 Country Distribution of Semiconductor Memory Patents



	By patent grant date 1967	68	69	70	71	72	73	74	75	76E	Total 67-76E
Total Patents	32	48	46	59	88	129	123	115	94	126	860
United States	26	40	36	45	75	108	104	79	73	96	682
Total Foreign	6	8	10	14	13	21	19	36	21	30	178
Japan		3	2	6	2	8	5	10	11	16	63
Germany	1	2	1	1	4	4	7	11	4	4	39
United Kingdom	3		3	4	1	3	1	4	3	2	24
France		1	2	2	1	1	2	3	1	6	19
Netherlands		1		1		4	2	1	2	2	13
Canada	1				4			5			10
Switzerland					1		1	1			3
Sweden	1		1			1					3
USSR								1			1

	By patent application filing date 1965	66	67	68	69	70	71	72	73	Total 65-73
Total Patents	42	41	39	42	86	106	101	101	92	650
United States	32	32	28	36	73	86	86	74	68	515
Total Foreign	10	9	11	6	13	20	15	27	24	135
Japan	2	2	6	1	2	8	5	4	15	45
Germany	1	1	1	2	4	4	4	12	3	32
United Kingdom	2	3	1	3		3	1	3	4	20
France		3	1		2		2	3		11
Netherlands			1		1	4	2	1		9
Canada	1				3	1		1	2	8
Switzerland			1					2		3
Sweden	2				1					3
USSR								6		6

(MNOS) and silicon-on-sapphire (SOS), are also being used in semiconductor memories. The main difference between unipolar and bipolar technologies is the number and sequence of diffusion operations during manufacture. Bipolar processes are identified by the type of logic circuit used; either TTL (Transistor Transistor Logic) or ECL (Emitter Coupled Logic). Charge Coupled Devices (CCD) comprise a subsection of semiconductor memories.

Semiconductor Patent Activity

Fig 3 presents semiconductor memory patent activity by application filing and patent grant dates and details the country distributions of the same data. Major activity occurred over the 1972-76 (estimated) period; foreign patents represented 26.0% of all patents granted over the 10 year base. Of all the patents in Figure 3, 94.6% are corporate owned and 2.4% government owned.

Recent emphasis has been on methods and circuitry for efficient reading of semiconductor memories to achieve faster access times. Other activity involves reducing the number of transistors per bit. Patents issued since February 1976 include:

3,967,252 – Sense Amp For Random Access Memory (Donnelly, Mostek Corp.) – Discloses a MOSFET random access memory having a sensitive sense amplifier. The sense amplifier utilizes a field effect transistor connected in the common gate mode to produce a large output swing as a result of a relatively low voltage swing which is produced by reading data stored in a memory cell.

3,965,460 – MOS Speed-Up Circuit (Barbara, Motorola, Inc.) – Discloses a circuit used to speed up the sensing of a bit-sense line of a MOSRAM. The circuit includes a cross-coupled latch subcircuit having an output suitable for coupling to an output circuit for the RAM.

3,959,781 – Semiconductor Random Access Memory (Mehta et al, Intel Corp.) – Discloses a MOSRAM system which employs a dynamic storage in which each cell comprises a single active element. A plurality of sense amplifiers are disposed in a column substantially bisecting each row of memory cells. A single input/output bus is employed for communications with all the cells. Two dummy cells are employed on each row line on opposite sides of the sense amplifier.

3,953,838 – FIFO Buffer Register Memory Utilizing A One-Shot Data Transfer System (Gilberg et al, Burroughs Corp.) – Discloses a system in which memory data words flow in parallel from an input register through a plurality of registers towards an output register, under automatic control of a one-shot data transfer system. A one-shot device and a status flip-flop are associated with each individual register to asynchronously transfer a data word register-by-register.

3,949,385 – D.C. Stable Semiconductor Memory Cell (Sonoda, IBM Corp.) – Discloses a field effect transistor memory array in which each cell comprises four FET's. The first two FET's are cross coupled while the third and fourth FET form loads for the cross coupled pair. D.C. stability is achieved by conditioning the load FET devices into partial conduction during the stand-by state of the memory cell.

3,949,382 – MOSFET Circuit For Reading The State of The Charge (Yasui, Hitachi, Ltd.) – Discloses an insulated gate field effect transistor memory device which has at least two parasitic capacitors and which delivers at its outputs the state of charge accumulated in at least one of the capacitors. The parasitic capacitors are provided with inverter circuits for discharge purposes.

3,940,747 – High Density, High Speed Random Access Read-Write Memory (Kuo et al, Texas Instruments, Inc.) – Discloses a MOSRAM which uses one transistor per storage cell. The cells are in a matrix of rows and columns, and a sense and refresh amplifier is located in the center of each column. The amplifier is precharged to a predetermined voltage level, which can be varied based upon supply and threshold voltages, for accurate data sensing.

magnetic core memories

Magnetic core memories contain toroidal core elements

Another first for ISS

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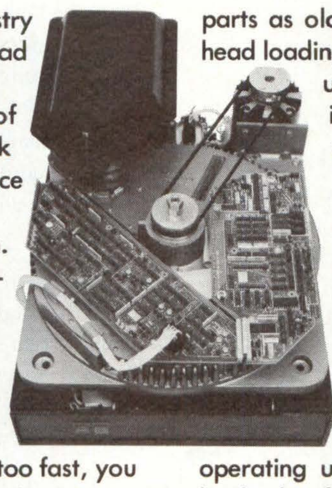

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All this performance and all this reliability go into a compact package that occupies just 14.5 inches of rack space.

But when all is said and done, the most significant statement we can make about the 550 is this: the price-performance ratio is twice as good as that of fixed head drives using older technology.

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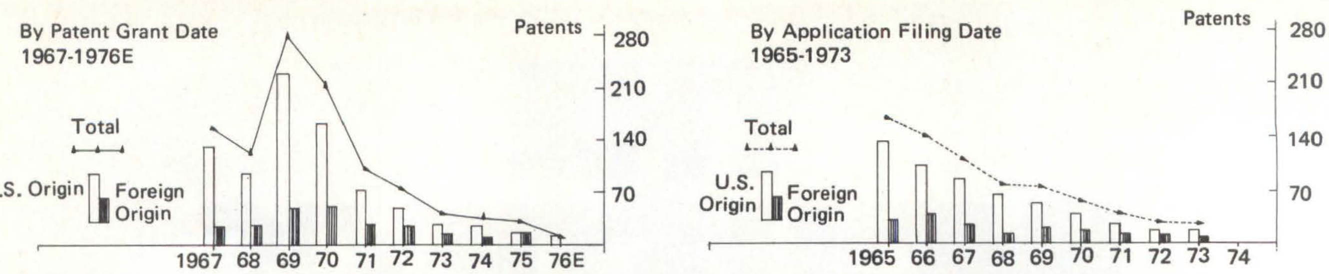
CIRCLE 19

Figure 4 Distribution of Magnetic Core Memory Patents



	By Patent Grant Date										Total
	1967	68	69	70	71	72	73	74	75	76E	67-76E
Total Patents	154	121	273	210	101	74	42	36	32	10	1053
United States	129	94	224	159	73	49	28	25	16	10	807
Total Foreign	25	27	49	51	28	25	14	11	16		246
United Kingdom	6	7	16	16	1		1	3			50
Germany	12	7	16	12	7	9	4	2	3		72
Japan	2	4	3	9	8	13	2	3	5		49
France		3	8	6	1		1		1		20
Netherlands		1	2	4	2	3	1	2			15
Sweden	1	2	2	1			1				7
Switzerland	3	1	1	1	2			1			9
Canada				1	2		1		3		8
USSR				1	2				3		6
All Other (6)		2	1	3			3		1		10

	By Patent Application Filing Date									Total
	1965	66	67	68	69	70	71	72	73	65-73
Total Patents	165	142	111	78	75	57	40	29	27	724
United States	134	103	85	64	53	39	27	18	18	541
Total Foreign	31	39	26	14	22	18	13	11	9	183
United Kingdom	9	7	7	1	2			2	2	30
Germany	13	16	7	5	3	6	4	3	1	58
Japan	1	6	2	6	7	9	4	2	2	39
France	4	3	5	1	1		1		1	16
Netherlands	3	1	1		3	2	1	2		13
Sweden	1		1				1			3
Switzerland		2	1		2				1	6
Canada			1		2			1		4
USSR		1	1		1			1	2	6
All Other (6)		3		1	1	1	2			8

which are switchable between two stable states of magnetic remanence. In a typical arrangement, known as 3 wire 3D, the cores are arrayed in matrices, known as mats, having core elements arranged in rows and columns. These cores are provided with drive lines for storage of information and sensing lines for reading information.

Recent Activity

Recent patent activity has been directed to reading out the information stored by the magnetic core memory, with ancillary emphasis on noise cancellation during the reading process. Activity also has focused on geometric arrangements of the core and drive lines. Patents issued since January 1973 include:

3,924,250 – Magnetic Core Matrix and Winding Pattern for Mass Core Memory (Ngo, Litton Systems, Inc.) – Discloses a mass core memory having magnetic core matrices in which the x-axis word wires and y-axis digit wires are paired and interwoven with periodic double cross-over regions so that a continuous sense wire can be easily threaded through selected memory core at the word and digit wire intersections. These winding patterns eliminate cross coupling and cancel delta noise.

3,924,248 – Non-Destructive Read Out Magnetic Core Memory Apparatus Having Linear Hysteresis Loop Nose Cancelling Core (Kobayashi et al, Fuji Electrochemical Co., Ltd.) – Discloses a device for supplying a cancelling voltage of a binary 1 or 0 to the sense lines to retain the memory state of the core before the magnetic flux change.

3,922,653 – Ring Core Memory Arrangement (Lighthall et al, GTE Automatic Electric (Canada) Ltd.) – Discloses a word ring core memory arrangement having word wires threaded around some cores of a module for bit 1 and around others for bit 0. A current ramp pulse, from a selected memory driver through a word wire to a selected memory switch, produces an output in sense windings on the cores with bit 1. The current ramp is produced by two generators, one on the driver side and one on the switch side.

3,905,926 – Large, High Speed Two Dimensional Core Memory (Sell, Ampex Corp.) – Discloses a large planar core memory utilizing highly stable, high density cores which are connected in a two dimensional configuration having a read-write cycle below 400 nsec, for 18 mil OD cores, and as low as 150 nsec, for 13 mil OD cores. The arrangement eliminates the need for temperature compensating circuitry.

3,878,543 – Sensing Circuit For Use in Core Memory (Yoshida, Hitachi, Ltd.) – Discloses a core memory sensing circuit capable of producing a read-out output higher than a predetermined level independently of the distance between the core and the sense amplifier. The sense lines passing through magnetic cores have near-ends connected with an amplifier and with first termination resistors and far-ends connected with second termination resistors.

3,864,672 – Matrix Store Wiring Pattern (Ingelaere, U.S. Philips Corp.) – Discloses a memory having magnetic elements arranged in columns and rows, forming two fields. Each of two sense-inhibit wires couples one half of the columns and the wires cross each other between the two adjacent fields in the column direction. All elements of a field are oriented along a single diagonal; adjacent fields in rows are oriented in two different diagonals; and adjacent fields in columns are oriented in a single diagonal.

3,825,907 – Planar Core Memory Stack (Sell et al, Ampex Corp.) – Discloses a planar, pluggable core memory stack having variable word and bit length. The stack includes a single printed circuit board having symmetrical plug connectors and printed circuits permitting either a first size memory on one side or different size memory on the other.

3,824,569 – Matrix Store Incorporating Noise-Balancing (Schuur, U.S. Phillips Corp.) – Discloses a three-wire matrix storage system in which signal amplifiers are connected to the center of two sense wires. Noise caused by the x-selection current is balanced by a similar, opposed noise on a

OEM, if you are using Dot Matrix Printers, see this...

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2 3 4 5 6 7 8

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second x-selection current, so that both sense wires pick up the same noise. Y-selection currents are balanced in a similar manner.

3,711,839 – High Density Core Memory Matrix (Sell et al, Ampex Corp.) – Discloses a memory arrangement where the cores are closely spaced together along the longitudinal axes, facilitated by orienting the cores at the maximum acute angle with respect to the longitudinal axis consistent with proper passage of latitudinal drive lines.

cathode ray tube memories

Cathode ray tube memories use photosensitive surfaces as a target upon which an electron beam reads and writes information. These surfaces are incorporated into a cathode ray tube (CRT), and circuitry for addressing the photosensitive surface is used to control the CRT's electron beam.

Recent Activity

Recent patent activity has been geared towards methods and apparatus for addressing the photo-sensitive storage plate in the CRT. Patents issued since November 1973 include:

3,889,244 – Graphic Data Display System With Multiple Display Inhibit Delay Times (Sinobad, Compagnie Industrielle des Telecommunications Cit-Alcatel) – Discloses a graphic data display system for effecting controlled traces on the screen of a cathode ray tube. The data display is inhibited by different delay times in response to the detection of changes in selected portions of binary data signals which indicate a change in the required trace. Trace changes are detected through use of a memory which stores binary signals, and comparators which compare input and output signals.

3,889,239 – Selective Storage Systems (Gillissen, Societe Honeywell Bull Societe Anonyme) – Discloses a random access memory system having a data storage loop, formed by a pair of data storage assemblies. Each assembly contains a memory for optical line-at-a-time reading by a television camera. Each camera is positioned in front of a display panel of an associated memory for reading the information stored in that memory and is simultaneously electrically linked to another memory for writing at least one information line into that memory. It is asserted that a storage time of several days is possible without the use of a power supply.

3,882,471 – Apparatus And Method Of Operating A High-Density Memory (Walker et al, Westinghouse Electric Corp.) – Discloses a high density cathode ray tube memory having a high density storage target. The target comprises a plurality of storage elements disposed in lines and columns. In order to provide a high density of storage elements each column and line is provided with a positioning tab with which the electron beam may be accurately positioned to read, write and erase information upon the storage target.

3,879,714 – Method of Recording Information with a Picture Storage Tube and Reading Without Erasing The Information (Veith et al, Siemens Aktiengesellschaft) – Discloses a method of writing, recording or erasing information on the signal plate of photodiodes by exposing one side to an electron beam containing data to be recorded. Each of the steps of writing, reading, and erasing is characterized by changing the value of a potential applied to the signal plate so that reading is accomplished without erasure.

3,798,633 – Data Storage and Display System (Hofstein, Princeton Electronic Products, Inc.) – Discloses a system utilizing a storage tube, the target of which includes separate storage areas for character configurations and character digital data. Characters are written in common form in the storage area and are read and transferred to a visual display. Characters are written in digital form on an offscreen area and are read and transferred to information storage.

3,789,372 – Self Tracking Beam Accessible Memory and Addressing Method Therefor (Lejon) – Discloses a method of addressing the access beam of a two dimensional information storage memory array. The array is adapted to store binary coded information in the form of addressable words for which the bits are aligned in one dimension.

3,778,786 – Data Storage, Image Tube Type (Fletcher et al, National Aeronautics and Space Administration) – Discloses a memory storage system employing a conventional vidicon tube. The tube is first conditioned to accept electrical input data and is then scanned by a first electron beam to write information data onto a photosensitive target. A second electron beam scans the surface to read the information. Conventional television camera scan, sync and power supply circuitry are used for conditioning and scanning.

3,774,168 – Memory With Self-Clocking Beam Access (Koo et al, National Cash Register Co.) – Discloses a beam accessed MOS semiconductor memory into which binary information can be written and stored and from which that information can be read and erased. The counting of electrical pulses created by the electron beam impacting on metal indexing strips is used, in a self-clocking mode, to control the position of the electron beam.

optical memories

Optical memories include all memory systems in which light waves (e.g., laser beams) are used to read or write information from photosensitive films, semiconductors or ferroelectric materials. Holographic memory systems comprise a subsection of optical memories and are separately reported on.

Patent Activity

Recent patent activity has been geared toward reading of information by optical systems into a semiconductor memory element. Activity is also directed to manipulating laser beams for more efficient reading or writing of information. Patents issued since September 1975 include:

3,962,688 – Optical Mass Data Memory (Westerberg) – Discloses a high density storage system which includes a laser beam used to read and write information in a rotating memory disc in response to acousto-optical modulation of this beam. This modulation provides fine adjustment of the beam in a radial direction while coarse direction adjustments are done mechanically.

3,958,229 – Optical Memory Systems Utilizing Organ Arrays of Optical Fibers (Duguay, Bell Telephone Laboratories, Inc.) – Discloses an optical memory system comprising an organ array of optical fibers. Each fiber has a uniformly different length in respect to its lengthwise consecutive adjacent fiber. The fibers are arranged in a bundle so that one

set of ends of the fibers are terminated in an input plane and the opposite set of ends are terminated in an output plane. A translating memory tape or rotating disc is juxtaposed with the output plane of the organ array to readout information on the tape or disc, or, in conjunction with a modulator, to write information onto the tape or disc.

3,950,738 – Semi-Conductor Non-Volatile Optical Memory Device (Hayashi et al, Agency of Industrial Science & Technology) – Discloses an optical memory having a light-permeable charge retention floating gate on an insulating layer. The insulating layer is situated on a first semiconductor surface. Photo-generated carriers in the surface of the semiconductor are injected over the semiconductor-insulator potential barrier by applying reverse bias between a first semiconductor region and a second region forming a rectifying junction with the first semiconductor region.

3,946,367 – Three Dimensional Electro-Optical Retrieval System (Wohlmut et al, Videonics of Hawaii, Inc.) – Discloses a system for sensing information located in tracks in various layers or depths of a multilayer recording medium. An electro-optical system tracks the desired information located in the recording medium in lateral and normal (or depth) directions, thereby controlling the positioning and focusing of the sensing system on the desired information. The third dimension is tracked by moving the desired information track past the electro-optical sensor to compensate for relative movement between the system and the track.

3,935,566 – Multiple-Channel Information Translation System And Method (Snopko, Zenith Radio Corp.) – Discloses a multiple-channel information translation system including a Bragg light-sound interaction cell interposed in the path of a spatially coherent input light beam. A number of electrical carriers are generated and amplitude modulated by information bearing input signals to drive the Bragg cell. The cell diffracts the input beam into a number of primary output light beams, respectively amplitude modulated in relation with the input signals.

3,925,767 – Radiation Set Thermally Reset Read-Only Memory (Witteles et al, The Singer Co.) – Discloses storing an arbitrary pattern of "ones" and "zeroes" into a standard MOSFET wafer containing individual transistors by selectively irradiating individual MOS transistors to a sufficient level to shift the threshold voltage by a predetermined amount. The irradiated transistors store zeros since they would not turn on when pulsed while all non-irradiated transistors in the wafer would store ones.

3,906,462 – Optical Storage Device Using Piezoelectric Read-Out (Feinleib et al, Itek Corp.) – Discloses a system which optically retrieves an information pattern by utilization of the dimensional changes of a piezoelectric material in response to an impressed electric field.

In the September Issue of *Digital Design*, part II of this **Benwill Technocast Report** will cover patent activity for other types of semiconductor memory technologies.

NATIONAL REALLY GETS THE LED OUT.

National Semiconductor, in case you didn't know it, is in the LED business. In a big way.

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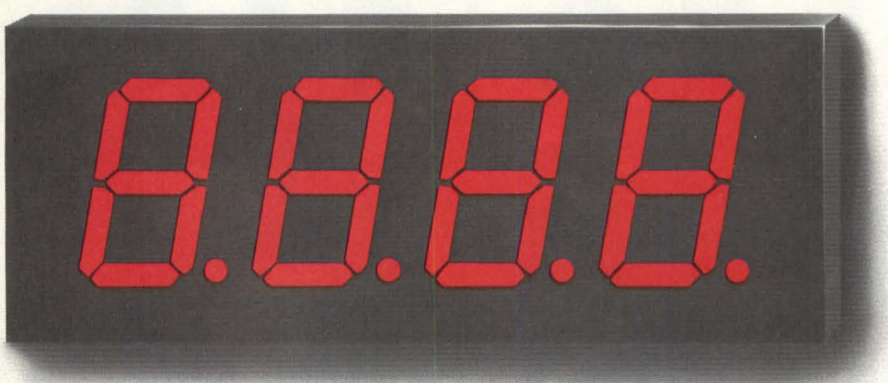
GOOD NUMBERS

All displays are multi-digit packages (0.3, 0.5, 0.7 inch high), pre-matched for brightness.



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Our units are available common cathode or common anode, multiplexed or direct drive.

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From "The Lamps of Tiffany" by Dr. Egon Neustadt, Fairfield Press, N.Y.

In fact, if we can't come up with the lamp you're looking for, maybe you should get a Tiffany.

National Semiconductor

FIBEROPTICS FOR DIGITAL SYSTEMS

by Richard A. Cerny and Dr. Marshall C. Hudson

Fiberoptic technology has its roots in 19th Century England with the discovery by physicist John Tyndall that light was guided along an arc by a stream of water. Simple unclad glass fibers were first used for image transmission in the 1930's The technology flourished in the 1960's and created a stable market for image transmission, light distribution and sensing applications. The emergence of the communications era in the seventies brought about a host of new applications for conventional fiberoptic assemblies. Today, fiberoptic communications is the most rapidly growing area of this technology.

design benefits

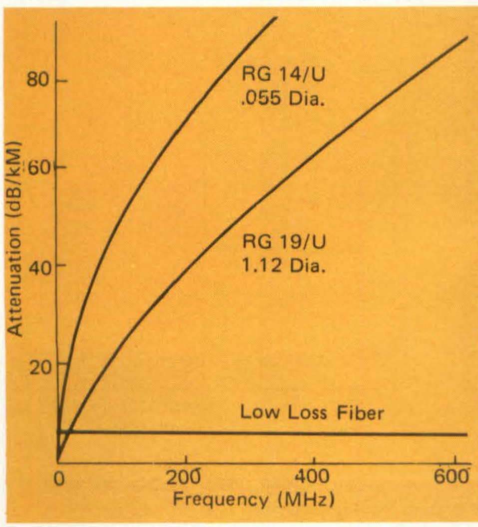
Some of the advantages of fiberoptic transmission are inherent to all fiberoptic systems because of the dielectric nature of the light conductors. Isolation, noise immunity, safety and security are among these advantages. Manufacturers can optimize other features such as information carrying capacity, repeater spacing, reliability and cost. For example, transmitting data through totally dielectric cables permits transmission directly across very high voltage potentials without the need for isolation transformers. Similarly, fiber optic cables eliminate ground loops inherent with coaxial cables. Because they are dielectric, fiberoptic cables do not attract lightning. Nor do they act as antennae; they pick up no inductive surges from nearby lightning flashes or corona discharges.

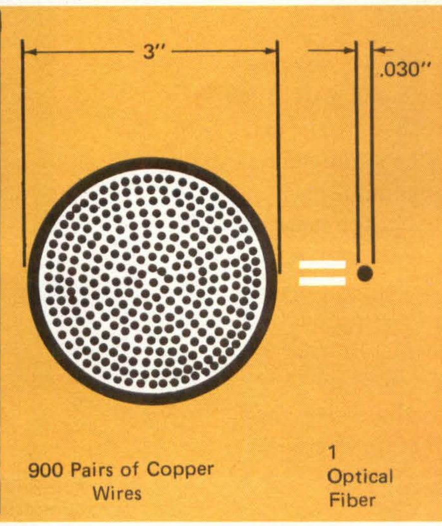
Electromagnetic interference (EMI) caused by lightning or inductive fields, radio frequency interference (RFI) caused by radio stations or radar and electromagnetic pulses (EMP) caused by nuclear events are no cause for concern to fiberoptic system designers. EMI/RFI/EMP noise will not cause measurable transmission error or damage to terminal equipment. Government standards concerning electromagnetic emission from data transmission cable and CATV lines are becoming increasingly stringent. Arguments as to whether these standards need be so strict may be purely academic because fiberoptics offer an immediate solution to the problem of cleaning up the electromagnetic environment. Fiberoptic cables, properly coated, do not radiate their signals or pick up external electromagnetic signals. They are essentially free from cross talk regardless of data rate, cable length or number of channels per cable.

Since signals do not radiate from fiberoptic cables, they are resistant to intrusion. A simple well designed cable would have to be broken into to allow an intruder access to the signal. Information cannot be compromised by using conventional external "listening" devices. The impact on national security is obvious. On industrial security the impact is more subtle.

Fiberoptic systems do not spark or short circuit. They cannot cause explosions in hazardous environments nor cause shocks to personnel, a safety feature in military data processing systems used where explosives are present. The Navy A-7 ALOFT fiberoptic program demonstrated both safety and cost savings by running fiberoptic cable through the liquid oxygen and weapon storage area where electrical cables were prohibited.

Fiberoptic cables have a larger information transfer capac-





Comparing coax and fiberoptic cables. Fig 1 (left): Attenuation vs length for several grades of coaxial cable and low loss fiberoptic cable.

Fig 2 (right): For the same information carrying capacity, the small diameter fiberoptic cable replaces up to 80 times its size in copper pairs.

ity than copper wire cables. Most fiberoptic systems are limited in bandwidth by the amount of energy per pulse arriving at the detector. However, laser diodes and externally modulated lasers have been successfully coupled to fiberoptics with information rates exceeding 1000 Mbit/sec. Material dispersion and modal dispersion of the optical fiber limit the bandwidth for a particular source.

Low cost fiberoptic cables can run from 5 to 10 kilometers before repeaters are necessary, transmitting data rates in excess of 100 megabits per second. Long repeater spacing results in improved system reliability, decreased initial system costs and decreased maintenance costs. Weight savings of up to 80:1 for fiberoptic cable versus conventional coax are possible. These savings are reflected in shipping and storage costs and are particularly meaningful for volume users. Historically, dramatic savings have been accomplished in aircraft, mobile field installations, surface ships and submarines. More recently, space savings have been demonstrated in interoffice telephone trunking applications. Weight savings have been especially significant where the electro-optics were designed in, rather than converted by adaptive equipment; where electromagnetic noise problems are severe; and where the lengths and sizes of wire cable replaced were large.

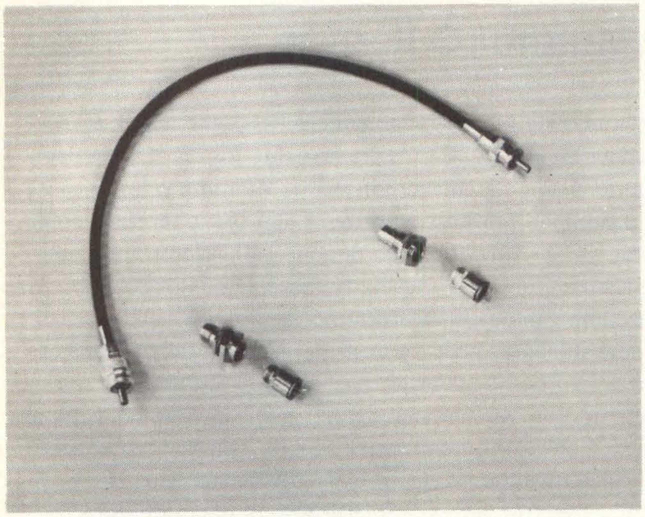


Fig 3 Electro-optic link for OEM use saves shielding and system hardware costs.

economic considerations

Before examining specific cost areas, note that we are comparing two different types of cables – copper and glass. The great multiplexing capacity of fiberoptics cables means that only a fraction of the number of lines may be required, resulting in decreased costs for both cables and interface connectors. Fiberoptic cables today cost about the same as premium grade coaxial cable. Indications are that coaxial cable prices will continue to rise along with copper prices. However fiberoptic cable prices will go down as production volume goes up – much like the experience/cost curve for semiconductor products. When fiber cables are in full production, they will cost only pennies per foot – less than 1/10 of their present cost. But even now, before fiberoptic cables are in full production, it may make economic sense to consider them for your application.

Ground fault systems and other devices which are designed into or added onto equipment to protect against grounding or voltage problems associated with electronic cable may be designed out or eliminated when fiber cable is used.

The low losses of fiberoptic cables allow the use of fewer repeaters and attendant structures on long length cable runs. In the computer field, fiberoptics can eliminate expensive hardware and software used for error checking and correction in those systems where errors normally tend to occur due to noise pick-up.

A major problem in interfacing computer peripherals to the CPU – or the terminal to the modem – is electromagnetic noise. This interference is the cause of errors and wasted time in retransmission. To limit this problem the data rate or cable length is often reduced. Fiberoptics, on the other hand, are immune to the induced noise that plagues metal cables regardless of data rate or length. Unlike coaxial cables, fiberoptic cables transmit clean digital data with no attenuation increase as bandwidth goes up.

Transmission errors caused by ground loops are likewise eliminated. In large buildings there is usually no such thing as a truly common ground. In fierce electrical storms tremendous voltage differentials occur that can damage expensive equipment. The electrical isolation quality of fiberoptics avoids this conductive tie between pieces of equipment.

Many types of fiberoptic cables available today will be able to be automatically upgraded over the years, as the technology advances. For instance, a good quality, graded-index low loss cable that uses an LED device today may be capable of transmitting 10 times as much data by using a high quality injection laser diode next year. Further source/modulator advances will no doubt bring still another order of magnitude improvement. And, throughout these improvements, the original cable need never be replaced.

The small size and low weight of fiberoptic cables naturally helps to keep manpower costs of installation down. But other installation costs are also affected. For example, the U.S. Army has shown that they can use a 1¼ ton trailer to

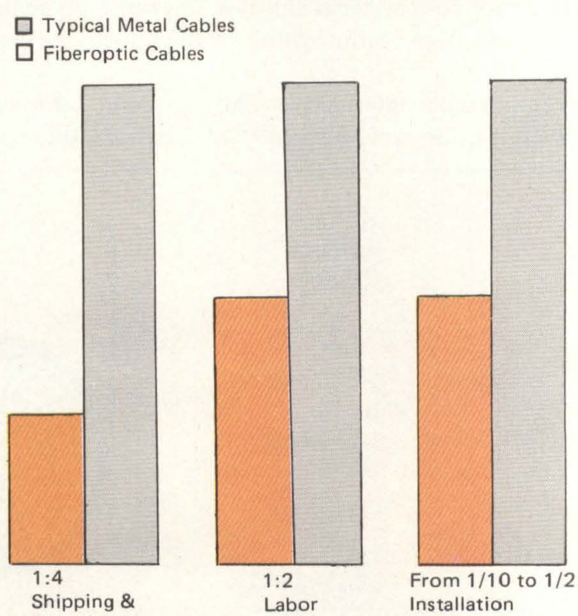


Fig 4 Comparison of some 'hidden costs' associated with communication system implementation.

Digital introduces DECstation. A big computer system that's small enough for anyone.

Digital put an amazing LSI version of the PDP-8 inside a DECscope, added some ingenious interconnecting devices and created something new. The DECstation. A complete computer system big enough to do all kinds of work and small, simple and inexpensive enough to do it for almost anyone.

DECstation. A complete computer system in disguise. It looks like a terminal, but look again. The DECstation has a powerful general purpose computer, a video terminal, a dual diskette drive, and its own special operating system. What's more, you can hook up two different printers and a second dual diskette drive. Then put the whole thing in a mini-desk, and when you're done you'll have the smallest big computer you've ever seen.

The Video Data Processor. It's the big reason the DECstation's so small. The VT78 Video Data Processor is a computer wrapped in a terminal. Inside the familiar DECscope you'll find an LSI version of the PDP-8 with 16K words (32K characters) of MOS memory and built-in interfaces. Two serial asynchronous ports feature speeds from 50 baud to 19.2 kilobaud. A disk port interfaces with up to 4 diskette drives. A parallel I/O port for printers and custom interfacing provides data transfer rates up to 180 kilobits/sec. All standard.

You can go from carton to computer in less than an hour. If you can push a button, you can run a DECstation. Because one button is all it takes to start things up. The bootstrap and self-test routines are built in.

Put it together, plug it in, and immediately you can begin to run anything from the PDP-8 software library. Which means you start with one of the most comprehensive sets of software tools available in a small system. Including two proven operating systems: OS/78 for stand alone applications and RTS/8 for real-time. OS/78, an extension of OS/8, supports a number of languages, including FORTRAN IV and BASIC. So all you have to do is load the operating system and start programming your application.

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transport fiberoptic cable that replaces three 2½ ton truck-loads of CX-4566 conventional electrical cable. Where installation space is limited, a fiber cable can be combined with, or laid adjacent to, a power cable, because line currents won't disturb a fiberoptic signal. It is conceivable that with the use of small fiber cables, computer room raised floors may become a thing of the past.

Electrical codes often require that electrical cables be confined in conduits. There are no codes (and no need for codes) for intrinsically safe fiberoptic cables. Therefore the

Fig 5 Digital transmission over the fiberoptic communication links eliminates modems for local distributin of data.

cost of laying conduits – typically $4/foot – is saved. Cable routing through hazardous areas makes it possible to save on line length as well. This is an important consideration for all safety related applications.

Since the technological development of fiberoptic communications was prompted by the telephone companies, it follows that they promise to be the major users of fiberoptics. Western Electric's field test in Atlanta demonstrated a large cross sectional cable for use in interoffice trunk lines in metropolitan ducts where expensive real estate is now overcrowded by wire cables.

Cable TV contractors are also working on prototype installations to determine the ways to take advantage of fiberoptics in their systems. As with telephone applications CATV systems will exploit the fiberoptic cables' large information carrying capacity and long repeater spacings. It is likely that as with telephone technology, the CATV community will also convert to digital transmission, which is more compatible with laser and LED source characteristics than is analog transmission.

Fiberoptic telecommunication systems also will solve other problems, i.e. cross talk, ringing and echos. Transmission of real time data in high noise environments avoids interference and induced errors of high frequency data. Lightning damage to cables and connected equipment can be eliminated where fiberoptic cables replace metallic conductors.

Refineries and chemical plants often have explosive atmospheres where sparks from shorted electrical cables could be catastrophic. Fiberoptic cables are now being designed into process control instrumentation systems to take advantage of their safety features. Fiber cables, used as control lines from a central process controller to remote processors or equipment, are essentially free from electromagnetic noise or "spikes", caused by motors, relays or power cables. This holds true whether the fibers run a few feet or a few thousand feet.

the design system

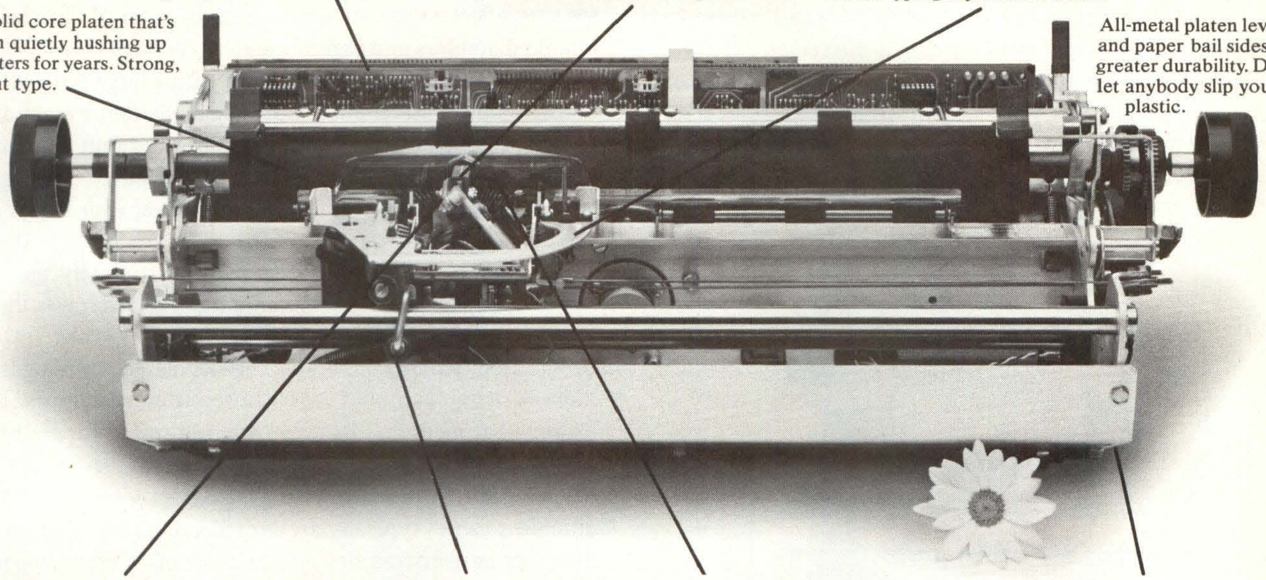
A fiber is a transparent material system that conducts or "guides" light. This guiding phenomenon is a result of a dissimilar set of material refractive indices. That is, an optically dense core material (high refractive index n_1) is usually surrounded by a less optically dense cladding material (lower refractive index n_2). The magnitude of the resulting optical density difference between the core and cladding determines the maximum angle at which guiding occurs (*numerical aperture*). Only rays which are less than or equal to the maximum angle are "accepted" and guided along the fiber, while all other rays escape from the side of the fiber and are "radiated."

A very simple fiber structure would consist of a simple strand of glass ($n_1 = 1.5$) surrounded by air ($n_2 = 1.0$). Such a simple optical fiber would perform very well were it not for the optical degradation that would occur from dirt and smudges on the glass-air interface. That is why nearly all fibers use a multi layer system of glasses, plastics or a combination of glass and plastic. The more reliable material systems are glass core with glass or plastic cladding, because there are no aging problems with glass as there are with plastics.

The most promising of these is the graded-index fiber which most efficiently transmits high volumes of data over long distances. Low loss fibers are necessary for lengths of over ½ kilometer. Since these fibers are relatively expensive on a fiber-meter basis, typically only one fiber per channel is used. Light sources and connectors for single fiber channels are not yet low cost. When they are, low loss fiber cables will also be cost effective for short lengths as well as

Property	Edge Emitter LED	Burrus LED	Injection Laser Diode
Bandwidth	F	G	E
Source Fiber Coupling Efficiency	G	G	E
Total Power Into Fiber	G	G	E
Narrow Line Width	F	F	E
Low Cost Volume Manufacturability	E	F	G
Lifetime	E	E	G

F = Fair G = Good E = Excellent



Planned unobsolescence.

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Qume just believes continuity of product is everything. Savings in design, spares provisioning, training. So all Qume products are part of a continuing family. Not a designer-gone-berserk whim factory.

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And it's a sound philosophy we're committed to. Whether it's the industry's first true microprocessor-controlled character printer, our Sprint Micro 3. Or Qume's new WideTrack™ — 26 inches of bi-directional printing power.

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long. That will cut inventory costs by avoiding the need for several grades of cable.

A typical fiberoptic data transmission system converts electrical pulses to light pulses that are then conducted by an optical fiber (sometimes called a "lightpipe") and received by a detector which reconverts the light into electrical data. This simple trio of components comprises a *link*. A link can be considered as a "black-box" from which the output data is a replica of the input data.

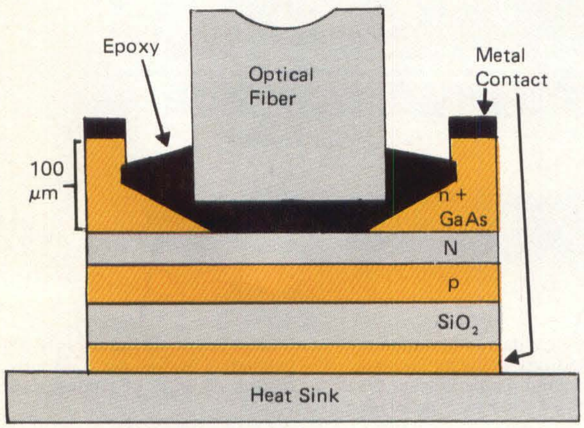


Fig 7 Typical 'Pigtail' configuration of fiber to Burrus LED.

the light source

A good light source for fibers is *small, bright, fast, monochromatic and reliable.* A *small* light source is efficient. *High radiance* assures that plenty of light gets coupled into the fiber. *Fast modulation* is necessary for the transmission of high bandwidth data. A *narrow spectral line width* helps keep the dispersion in the fiber low. And, of course, a source must have a *lifetime* of thousands of hours.

Laser diodes and LEDs are now being developed with factory assembled fiber pigtails attached to avoid the need for field alignment of fiber to devices smaller than a grain of salt. Only a simple fiber-fiber splice will be required. The light emitting diode, a dependable solid state device, is capable of transmitting moderate optical power at modulation rates in the tens of megahertz. The two most common types of LEDs for communications are the edge emitter which resembles a diode laser, and the surface emitter. The most promising surface emitter is known as the "Burrus" design.

Recent developments have increased average lifetimes of commercial room temperature CW diode lasers to several months. Laboratory versions are achieving predicted lifetimes of over ten years. The advantages of diode lasers stand out in the long line digital telecommunication applications if you must maximize power and bandwidth. Modulation rates in the *hundreds* of megahertz are currently being demonstrated in prototype laser systems.

fiber types

Fibers are generally classified in two ways – by refractive index profile (step or graded index) or by attenuation (dB loss per kilometer). Since the graded-index fiber is typically a low-loss type, all the rest being step-index, we shall look at the fibers by attenuation range.

High Loss (greater than 100 dB/km) For lengths less than 30 meters, high loss fiber cables are the most practical. They are very efficient at coupling in light because of their large bundle diameters and high numerical aperture (NA). (A large acceptance angle is associated with a large NA). Attenuation per unit length is not very important over short lengths, as it is in telecommunications, but input coupling is. So in a short length, say 20 meters, an inexpensive light emitting diode can transmit far more power over a high loss cable than a low loss cable.

Medium Loss (20 – 100 dB/km) Unfortunately the numerical aperture of the medium loss cable is lower than the high loss cable; hence, the input coupling is also lower. In sufficient lengths, however, this decreased coupling is more than compensated for by lower attenuation loss. The lengths that medium loss fibers are best suited for are between 30 and 500 meters. Fortunately, however, as the NA decreases, the information carrying capacity increases. Medium loss cables typically are provided in bundles of small fibers, or as oversized single-fiber channels. Certain types of pure fused silica medium loss fibers are also preferred for use in high nuclear radiation environments because of their resistance to damage.

Low Loss (Less than 20 dB/km) There are three commercial types of low loss fibers, all based on refractive index profiles as discussed earlier: step-index, graded index and single-mode fibers.

connectors

Whether connecting cable-to-cable or cable-to-device there are two basic connector types; single-fiber and bundle type.

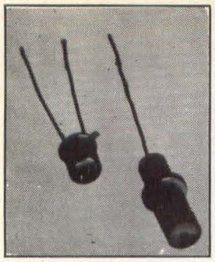
Bundle In splicing or terminating bundles, moderately careful alignment is required – normally, modified versions of standard RF connectors are adequate (BNC, TNC, SMA, etc.). The fibers are held together as a unit with epoxy. Then they are ground and polished to a smooth optical end finish.

Single Fiber. Because of the very small active core area in single fibers, and the very small emitting area of single-fiber sources, alignment is critical. For efficient coupling of single fibers, the end separation, axial and lateral alignment tolerances must be on the order of a few microns. These connectors are now in the first stages of development. Epoxies are normally not used in these connectors. Rather than grinding and polishing the fiber ends, they employ a technique of scoring and breaking the fiber to a flawless perpendicular end finish.

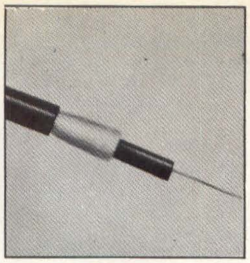
the receivers

To transduce the light to electricity we use a photodetector and some associated electronics. The choices of a photodetector device include a PIN photodiode, an avalanche photodiode (API), a phototransistor or a photomultiplier. Because of their efficiency and ease of use at red and near IR wavelengths, silicon PIN and avalanche photodiodes are used most often.

PIN Photodiode For relatively fast speeds and adequate sensitivity in the 0.75 µm to 0.95 µm wavelength region, the silicon PIN photodiode is commonly used. The PIN photodiode has quantum efficiencies of over 50% and can

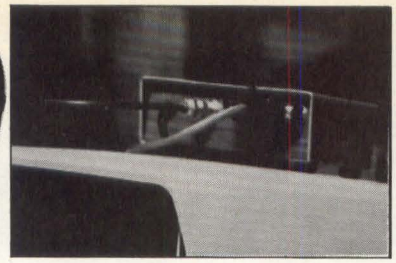


Source and Detector

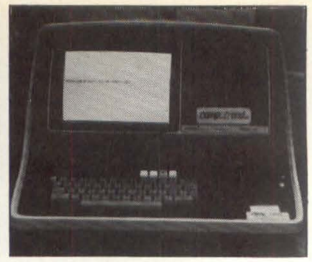


Fiber Cables

Data Link



Modem Eliminator



Terminal

operate at low reverse bias voltages. For high speed operation, they must be biased by voltages of up to 50v. Rise times of less than 1 ns are commercially available.

Avalanche Photo Diode (APD) The internal amplification of avalanche photodiodes results from avalanche multiplication of carriers taking place in the junction region. The high reverse biasing necessary means that voltages on the order of 100v–300v must be available. The temperature sensitive nature of these diodes suggests that the installation environment should be carefully examined. The advantage of using APD's appears in higher signal-to-noise ratios, especially at high bit rates. Gain-bandwidth products of 100 GHz have been documented.

how to specify

When selecting fiberoptic cable consider the following parameters:

Length The most important consideration in choosing fiberoptic cable is the length of the system. Length can limit the transmission of both power and bandwidth, and the proper choice of cable can optimize this transmission.

Data Rate In short length cables, data rate limitations seldom occur. But in long length cables data rate can be a problem, since cable bandwidth decreases linearly with length up to some equilibrium length – typically ½ km. Beyond that length the bandwidth appears to decrease as the square root of the length. So by determining where either low NA or graded-index cables are required, one can optimize the system data transmission capability.

Source Wavelength Attenuation of most fibers tends to be at a minimum in certain wavelength regions, especially near .82 μm and 1.06 μm. In some fibers, the attenuation at .9 μm, where reliable GaAs sources exist, is high due to "water" (OH-ion) absorption bands near this wavelength. Other types of fibers tend to display even lower attenuation at .9 μm than at .82 μm.

Number of Channels Each signal channel should have its own fiber on which to transmit, since two-way transmission

CIRCLE 29

on a single fiber requires additional coupling losses on input and output. Therefore, whether the number of channels are provided all in one cable, or in several cables on a modular basis, is up to the discretion of the user, and his cost, space and weight requirements.

Fig 13 Direct transmission of data over fiberoptic data links incorporates new system design elements.

Cost There may be several fiberoptic cables which would be suitable for a given system. However, for additional cost, a greater upgradability may be built into the system. As an example, if a very high bandwidth graded-index cable were used rather than a moderate bandwidth, low numerical aperture, step-index cable, it could be upgraded in band-

A DECADE OF FIBEROPTIC COMMUNICATIONS

1966 – ITT/STL - Dr. Charles Kao and George A. Hockham theorize that optical communications via fiberoptics could revolutionize the telecommunication industry because of increased bandwidth potential in a noise free medium. The barrier is seen as fiber attenuation of less than 20 dB/km, compared to the current 1000 + dB/km fibers.

1968 – Bell Laboratories begins a program to develop fibers that are adequate for telecommunications ($<$ 20 dB/km).

1970 – Corning Glass Works breaks the 20 dB/km barrier, using a vapor phase oxidized silica glass.

1974 – Valtec Corporation breaks the 20 dB/km barrier, using low cost, commerical grade silica.

1975 – ITT develops the first fiberoptic cable capable of withstanding 400 lb. tensile loads

1976 – US Navy Naval Electronics Laboratory Center successfully proves the systems feasibility of fiberoptics in an avionics application on an A-7 Corsair. IBM develops the hardware using Valtec cables.

1976 – Valtec breaks the 5dB/km mark in high-bandwidth fiberoptic cables.

1976 – AT&T field tests multichannel fiberoptic cable and finds results positive.

1977 – Valtec delivers first commercial cable with less than 2 dB/km attenuation and first commercial, single mode optical cable.

DEFINITIONS OF TERMINOLOGY

Attenuation: The optical power loss per unit length: the sum of components of absorption and scattering.

Bend Loss: A form of increased attenuation caused by allowing high-order modes to radiate from the side of the fiber. The two common types of bend losses are: (a) those occuring when the fiber is curved around a restrictive radius of curvature and (b) *microbends* caused by small distortions of the fiber imposed by externally induced perturbations, such as poor cabling techniques.

Cladding: The low refractive index material which surrounds the core of the fiber and protects against surface contaminant scattering. In all-glass fibers the cladding is glass. In plastic-clad silica fibers, the plastic cladding also may serve as the coating.

Conservation of Radiance: A fundamental conservation law which relates the amount of power coupled into a fiberoptic to the source radiance rather than the total source power. The conservation law negates the effectiveness of lenses or tapered waveguides to improve source-to-fiber coupling in most cases.

Core: The light conducting portion of the fiber, defined by the high refractive index region. The core is normally in the center of the fiber, bounded by the cladding material.

Dispersion: The cause of bandwidth limitation in a fiber. Because dispersion causes a broadening of input pulses along the length of the fiber, this mechanism is usually referred to as pulse-spreading. The two major types of dispersion are *mode* and *material.*

Graded-Index: Fiber type wherein the core refractive index decreases almost parabolically radially outward toward the cladding. This type of fiber combines high-bandwidth capacity with moderately high coupling efficiency.

Infrared: The electromagnetic wavelength region between approximately 0.75 μm and 1000 μm. For fiberoptic transmission the near infrared region between 0.75 μm and 1.3 μm is the most relevant because glass, light sources and detector techniques are most nearly matched in this wavelength region.

Injection Laser Diode: A semiconductor device in which lasing takes place within the P-N junction. Light is emitted from the diode edge.

Lambertian Emitter: An optical source which has a radiance distribution that is uniform in all directions of observation.

Light Emitting Diode: A semiconductor device which emits incoherent light formed at the P-N junction either from the junction stripe edge or its surface.

Material Dispersion: Light impulse broadening due to differential delay of various wavelengths of light in a waveguide material. This group delay is aggravated by broad linewidth light sources.

Modal Dispersion: That component of pulse spreading caused by differential optical path lengths in a multimode fiber.

Modes: Allowed solutions to a mathematical expression describing the propagation of light through a fiber. Compare Ray.

Multimode Fiber: A fiber that supports propagation of more than one mode of a given wavelength.

Multiplexing: Combination of information signals from several channels into one single optical channel channel for transmission.

Numerical Aperture: Measure of light acceptance of a fiber; the sine of the half angle of light acceptance, defined by:

$$NA = \sqrt{n_1^2 - n_2^2}$$

where n_1 and n_2 are the refractive indices of the core and cladding respectively.

Packing Fraction: The fractional proportion of active core area to cross-sectional area in a bundle of fibers.

Pulse-Spreading: The increase in pulse width in a given length of fiber due to the cumulative effect of material dispersion and modal dispersion.

Radiance: Radiant power per unit source area per unit solid angle, expressed in watts / m^2 / steradian.

Ray: A geometric representation of a light path through an optical device: a line normal to the wave front indicating the direction of radiant energy flow. Compare: mode.

Refractive Index: The ratio of light velocity in a vacuum to its velocity in the medium of interest.

Single mode fiber: A fiber in which the "V value" is less than approximately 2.4 where $V=(\pi dNA)/\lambda$,d is the core diameter and λ is the propagating wavelength.

Step-Index Fiber: A fiber in which the core is of a uniform refractive index.

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width as modulation rates and quality of the optical sources increase.

Strength. Fiberoptic cables can be made to meet desired tensile or crush strength. A heavy duty cable should be capable of several hundred pounds tensile strength, enough to pull through long lengths of conduit. Medium duty cables can pull through intrabuilding cable trays. Light duty cables are useful for laboratory use or system wiring.

Strength-to-weight ratios of fiberoptic cables can be much greater than most metal cables, making them much easier to install. Crush tolerance of many fiberoptic cables is also greater than that of conventional metal cables.

Richard A. Cerny *and* **Dr. Marshall C. Hudson** *are with Valtec Corporation, West Boylston, Massachusetts 01583.*

Multiplexing Planar Gas Discharge Displays

by Robert Kuntz, Dave Sien and Wayne Wong

Gas Discharge Displays operate in two basic modes – dc and multiplex. In the dc mode, all digits are on (lighted) at one time. Each digit, as a consequence, requires its own drive, for example, to each digit. Another method would be to obtain drive for all digits from a single device such as an MOS LSI chip or some circuit designed for the decoding and driving task.

In multiplexed operation, on the other hand, digits in the display field are not on at one time but, rather, are individually switched on in some sequence at a high repetition rate. Two or more digits thus time-share a single cathode driving device. If the display field consists of a large number of digits, a matrix of two or more cathode drive circuits may be used with a corresponding reduction in anode drive circuitry.

The most common method of multiplexing connects all

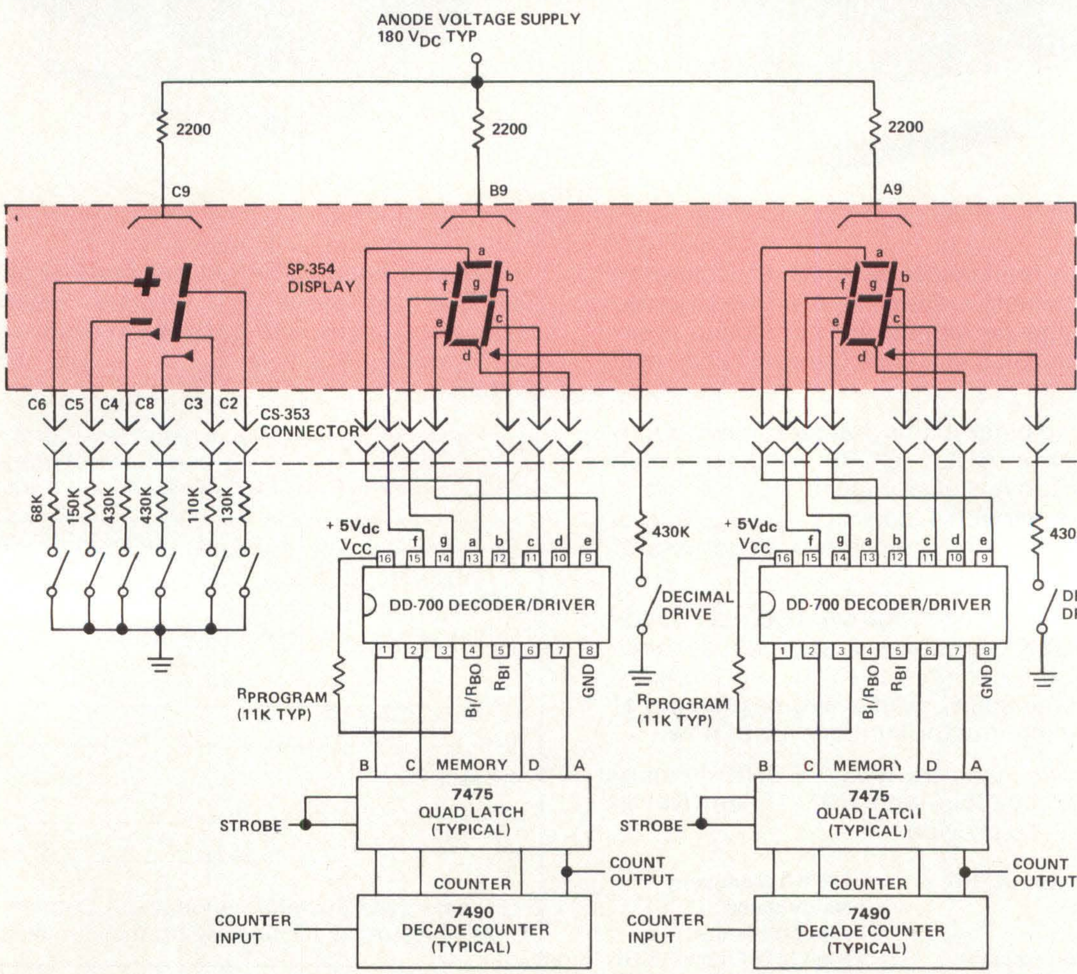
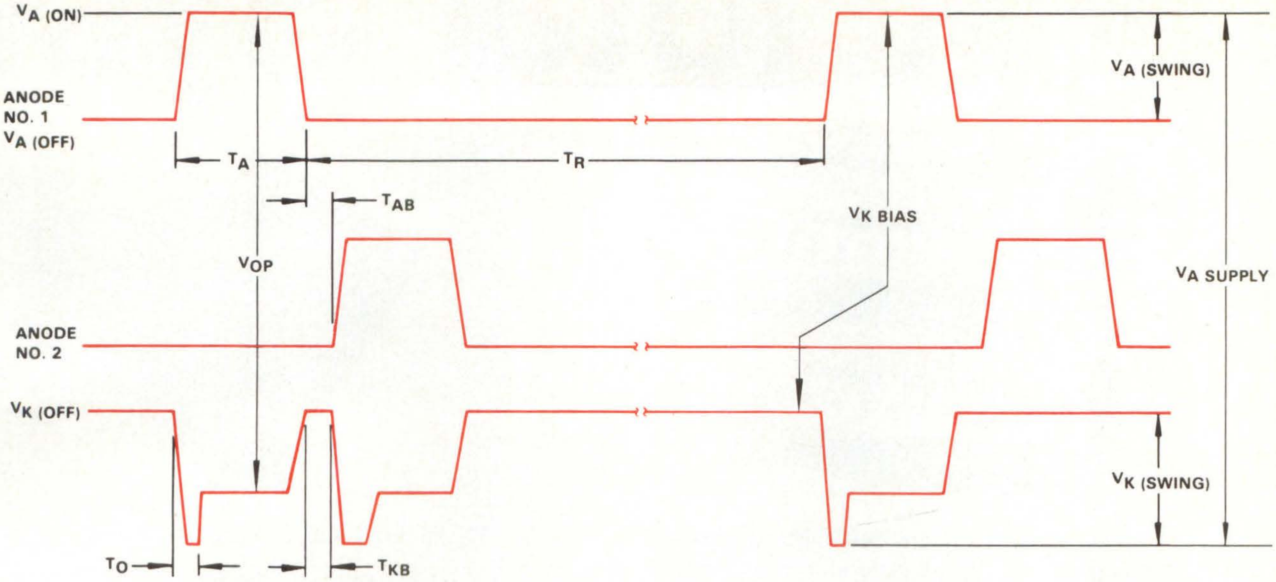


Fig 1 Conventional dc operation of a typical display; one decoder/driver drives each digit.



GENERAL CONSIDERATIONS:
V_K BIAS, MAX VOLTAGE SP300 = 125V, SP400 = 130V
V_A (SWING), TYP 40 VOLTS
V_K (SWING) MIN SP300 = 40 VOLTS, SP400 = 50V
KEEP-ALIVES SHOULD BE EMPLOYED IN MULTIPLEX OPERATION

V_A SUPPLY = DISPLAY SUPPLY VOLTAGE
V_A (ON) = ANODE ON VOLTAGE
V_A (OFF) = ANODE OFF VOLTAGE

V_K (OFF) = CATHODE OFF VOLTAGE
V_{OP} = TUBE OPERATING VOLTAGE
T_O = TUBE TURN-ON DELAY
T_A = ANODE ON TIME
T_R = ANODE OFF TIME
T_{AB} = ANODE BLANKING TIME
T_{KB} = CATHODE BLANKING TIME
V_K (BIAS) = CATHODE BIAS VOLTAGE
V_K (SWING) = CATHODE VOLTAGE SWING
V_A (SWING) = ANODE VOLTAGE SWING

Fig 2 Sequential scan multiplex waveforms.

like cathode segments in parallel to one cathode driver and scans the display anodes in one of two ways: *sequential scan* – each anode is successively switched on for a brief period; or *interlaced scan* – anodes are scanned as long as no two adjacent digits are successively energized.

factors in the choice of dc or multiplexed drive

When weighing dc against multiplexed operation of gas discharge displays, several virtues appear on the dc side of the scale. One is the fact that its simplicity (no anode switching is necessary) avoids the dynamics of multiplex timing. Another is economy. Conventional dc drive, using decoder/drivers or MOS (custom or standard), can be less expensive for four or fewer digits. The multiplex decision is not totally digit-dependent. There are occasions when component costs for memory, time-base, data-select, anode drivers and the like will make it economically feasible to multiplex five digits or more. A third important factor is readability under high ambient light conditions, which requires a higher-than-usual cathode current for greatest display brightness. Further, because of duty cycle, the multiplex mode always requires a higher pulsed cathode current than dc operation does to achieve an equivalent brightness. Since use of extremely high cathode currents can reduce the life expectancy of a multiplexed display, dc operation is generally used in high ambient light environments.

In a typical installation for dc operation, the current limiting resistors in each display's anode circuit are recommended for voltage and current surge protection of the decoder/drivers. Drive for the decimal points, as well as the plus and minus symbols, and the two numeral one segments is provided by switching to ground through individual current limiting resistors. With decoding circuitry, the display could also be driven by means of switching transistors or electromechanical switches using the proper current limiting resistors recommended by the manufacturer for their displays.

The decision to use multiplexed operation for a display is generally based on economic tradeoffs. Some major considerations: • the requirements of any MOS/LSI circuits used; • the number of digits, since multiplexed operation becomes more cost effective as number of digits increases; • multiplexing circuitry cost versus cost of decoder/drivers or cathode drivers; • system power requirements (multiplexing generally reduces power drain).

technical multiplex circuit considerations

Multiplex waveforms and terminology – The timing required for multiplexed operation of gas discharge displays is important but not critical. The digit on-time, for example, can be as short as 80 μs or as long as 2 ms. Field scan repetition rates are limited only by the visually perceptible flicker (about 100 Hz) at the low end and the digit turn-on delay time at the high end. Fig 2 shows the typical waveforms of a multiplex circuit and defines terms used to describe operation of the circuit.

Flicker – Human visual perception plays a role in determining multiplex circuit timing. Since each digit is addressed individually, operation must be fast enough so that the display appears to be steady and flicker-free. Although a rate from 50 to 60 Hz is generally thought adequate to provide flicker-free perception, a strobing effect caused by relative motion between eye and display can result in apparent

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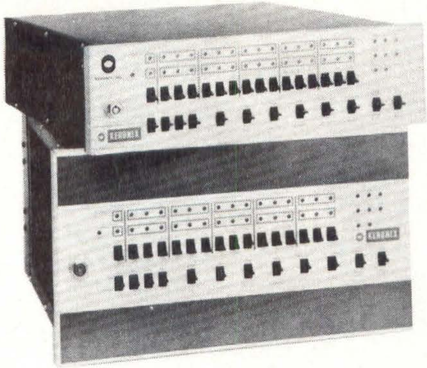

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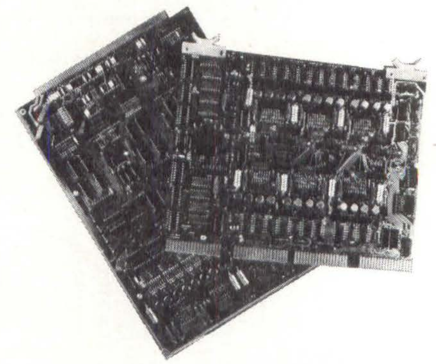

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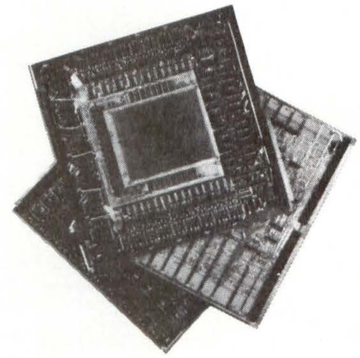

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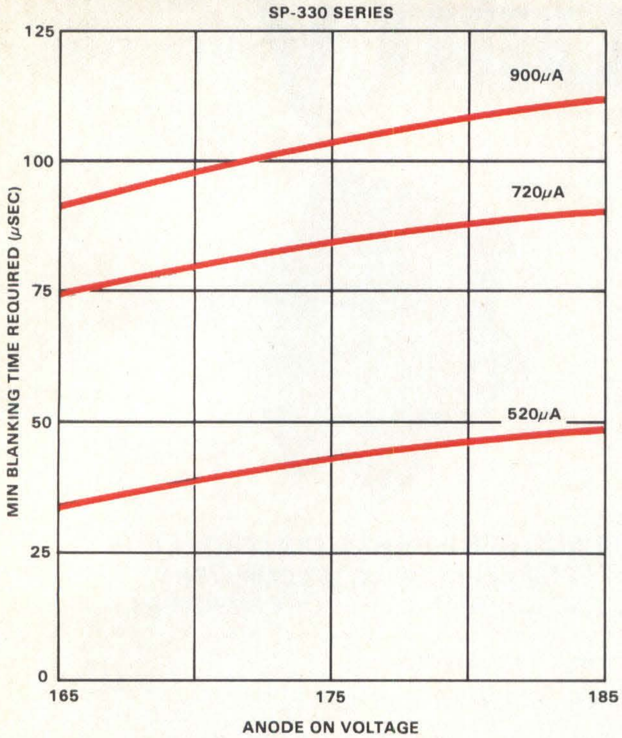

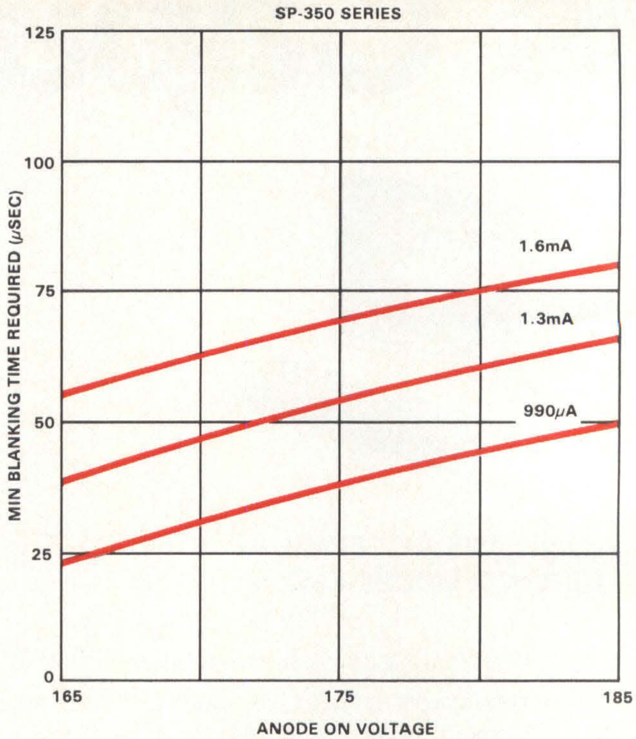

NOTE:

THE FOLLOWING TEST CONDITIONS WERE USED:

1. FIGURE "808" DISPLAYED USING SP-333, SP-353 STROBED LEFT TO RIGHT.
2. 20 μSEC ANODE BLANKING AS WELL AS INDICATED CATHODE BLANKING.
3. CATHODE BIAS — 120 VOLTS.
4. ANODE BIAS — 120 VOLTS DC.
5. ANODE PULSE — 200μSEC "ON," 1.4mSEC "OFF".

Fig 3 Minimum sequential scan blanking requirements for two different raised cathode displays.

flicker at these frequencies. For this reason, we recommend a minimum multiplex scan rate of 100 Hz.

As will be explained later, a properly operating keep-alive circuit provides a continuous source of ionization, assuring effective operation at low multiplex scan rates. If, however, a condition exists in which the keep-alive is not used and the refresh period is greater than 3 milliseconds, reionization delay of the display becomes a random function of the decaying ionization from the most recently ionized segments. Without a steady source of ions, a given digit may not turn on before the next digit is addressed. The result is a random flicker because of delay uncertainty. To sum up, you can avoid flicker by properly operating the keep-alive cathode, by providing an 80 μsec minimum digit pulse-length and by using a multiplex scan frequency greater than 100 Hz.

Streamers – Where sufficient potential difference exists between the anodes of adjacent digits, the anode with the lower potential will act as a cathode for the pair and spurious ionization may cause a harmless blue glow called a streamer to appear between the two digits. A similar condition can exist between two cathodes.

In dc operation, because the digits are on continuously, a 14-volt differential is sufficient to cause a streamer. For this reason, the maximum voltage difference between anodes or cathodes cited in a display's specs must be observed.

In multiplexed operation, on the other hand, because digit on time is relatively short and a single digit is on at one time, a voltage difference up to 90 volts between adjacent anodes is permissible. A voltage swing greater than 90 is unnecessary and is not recommended for two reasons: first, because the cathode is typically biased at some potential above the reference and, second, more costly anode switches with a higher breakdown voltage rating would be required.

Blanking – Streamers may also occur when the anode of one digit position serves as the anode for the adjacent digit position. This condition can occur in multi-digit, multiplexed displays when insufficient blanking time (time for de-ionization) is allowed between adjacent digit strobes. In a left-to-right scan, the residual ionization will most affect segments "b" and "c" of the digit being deenerigized. Conversely, in a right-to-left scan, the affected segments are "e" and "f".

To prevent streamers caused by residual ionization: • the removal of turn-on voltage from, and the application of turn-on voltage to, adjacent digits must be adequately separated in time by electrode blanking or, • successively energized digits must be physically separated by use of the technique of interlaced scan. Blanking creates a "dead time" between the on times of adjacent digits so that ionization from a deenergized digit can sufficiently decay before the next digit is energized. Interlaced scan, on the other hand, increases the distance between successively energized digit positions and eliminates the need for blanking.

Blanking may be applied to the anodes, cathodes or both (for best results, both), using either the leading or trailing edge of the addressing waveform. Cathode blanking has been found to be the more effective and may eliminate the need for anode blanking. However, because of the possibility of overlapping waveforms occurring with some digit drivers, it's good general practice to use both cathode and anode blanking.

Fig 3 shows the minimum blanking requirements for raised cathode, planar gas discharge displays in sequential scan circuits as a function of supply voltage and segment current. Because of construction differences, displays using the new screened image technology need no blanking to prevent streamers.

Waveforms of the applied voltage, anode current and light output generated during scan of one digit of a blanked display are shown in Fig 4. The amount of blanking required to de-ionize a digit will depend on the display voltage, peak segment current and type of display used.

Still another multiplexing technique also needs no blanking. As will be explained later, under split cathode multiplexing, multiple digit scanning, such as might be used in simultaneously addressing both digits in a dual package, requires no blanking because successively energized digit pairs are separated by display envelopes. Streamers, in this case, are a physical impossibility.

Power Consumption – A multiplex circuit consumes less power than a comparable dc-driven circuit because only one digit at a time is on. Furthermore, the logic power consumed will be less in the case of anode scan multiplexing since only one set of cathode switches is necessary. For each numeral, the peak power is equal to the peak segment current, times the number of "on" segments, times the power supply voltage. Average digit power is a digit's time-averaged power; i.e., the digit's peak power times its duty cycle. If interdigit blanking is used, the average power consumed by several multiplexed digits is simply the sum of the average power of each digit and may be expressed as follows:

$$(1) \quad P_a = \sum_{i=1}^{x} P_i \, [T_A/(T_A + T_R)]$$

where, P_a = average power consumed per multiplexed display
P_i = peak power consumed by the ι-th digit (a function of the number selected)
x = the number of digits
T_A = digit "on" time
T_R = digit "off" time, including blanking.

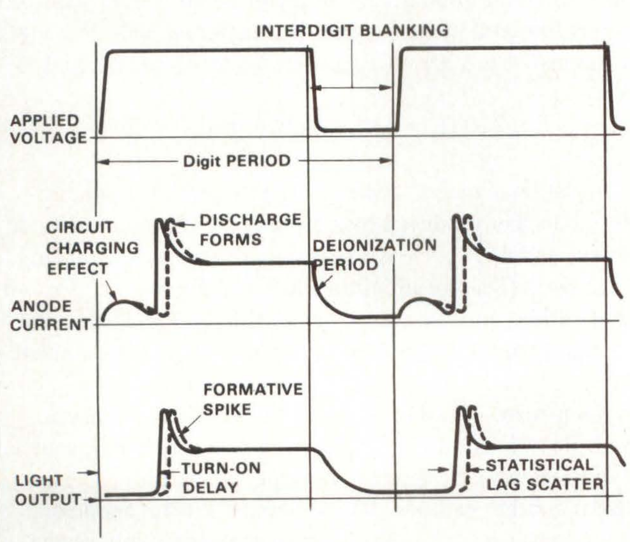

Fig 4 Typical waveforms driving blanked scan.

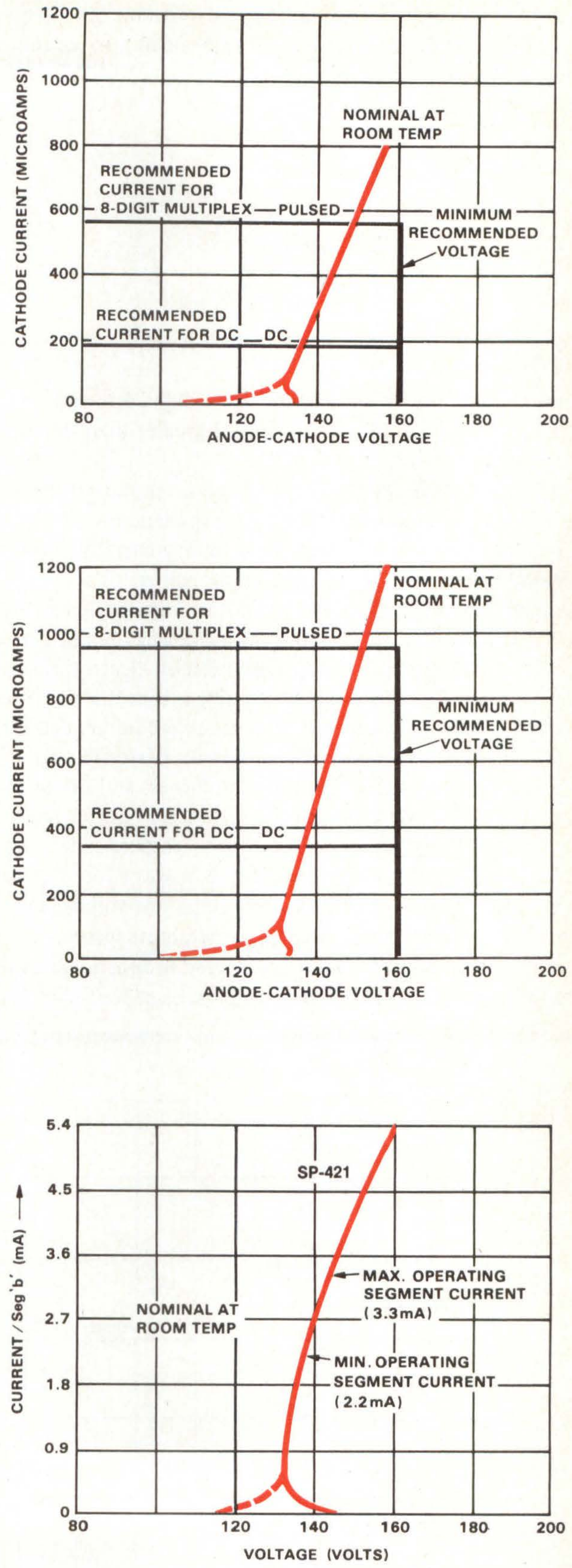

Fig 5 Typical plots of direct current operating characteristics for 3 different displays. Note typical manufacturer application recommendations.

P_i is the peak power consumed by one digit; $T_A/(T_A+T_R)$ is the duty cycle for that digit. It can be shown that, in general, P_{DC} will be greater than P_a by first assuming a worst case where the peak powers of all digits are at a maximum equal to n times the dc power, and that $n < (T_A+T_R)/T_A$. Then, rewriting equation (1):

$$P_a = \sum_{i=1}^{x} n\, P_{DC}[T_A+T_R]$$

(2) $P_a = xn\, P_{DC}[T_A/(T_A+T_R)]$

or,

(3) $P_a < xP_{DC}$

Since xP_{DC} is the power required by x digits driven in the dc mode, the dc power requirement is greater than the multiplexed requirement.

Fig 5 shows the voltage/current characteristics of three typical displays and manufacturer recommendations for each. To operate a display at a high multiplexing current, it is important to select a high enough supply voltage to support the required segment current but not so high that excessive power is wasted in the current limiting devices. Values of current limiting resistors for displays driven by electromechanical or transistor switches may be derived from the VI curves. However, constant current IC drivers are recommended for constant brightness and consistent circuit performance.

Brightness and Life – Both the brightness and life of a display are a function of cathode current and duty cycle. Fig 6 shows the relationship between brightness and current as a linear function. Brightness is also a function of power, since power is equal to the product of voltage and current, and may therefore be expressed in its terms.

If the average brightness is considered proportional to the average power, P_a, and the peak brightness produced at peak power, P_i, is considered to be equal to some factor, n, times the dc brightness, then equation (1) can be rewritten:

(4) $B_a = (nB_{DC})\, T_A/(T_A+T_R)$

where, B_a = brightness produced by average power
B_{DC} = brightness produced at typical dc power
n = number x DC (brightness) current

Since equation 3 is true for multiplexed circuits, therefore, $B_a < B_{DC}$. In general, then, brightness in a multiplexed display circuit is less than that in a dc circuit.

Fig 6 Relationship of brightness to segment current for 2 typical raised cathode displays.

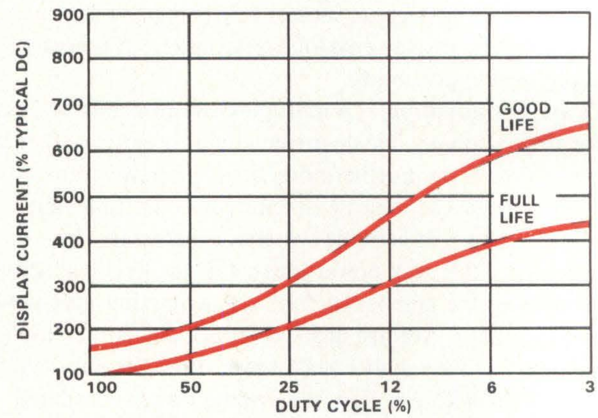

Fig 7 Maximum operating current limitations plot for a specific display to permit calculation of brightness and life.

Display lifetime, unlike brightness, is approximately a non-linear, inverse function of cathode current. An empirically derived relationship in Fig 7 shows the dependency of display life on current and duty cycle.

The constraint of lifetime will limit maximum brightness in a given system. For example, if a system requires a life of 5 years and the duty cycle is 25%, the maximum average brightness can be found using Fig 7 and equation (4). From Fig 7, since the good life curve is equivalent to five years of display life, at 25% duty cycle the maximum allowable segment current is 300% of typical dc value. There, n equals 3, and,

$$B_a = \frac{3 \times 210\ \text{fL}}{4} = 157.5 \text{ foot lamberts.}$$

In the final analysis, whether the brightness of a multiplexed display produced by a given combination of cathode current and duty cycle is adequate or not requires human judgement. (See the circuit in Fig 9.) Adjusting the programming current and the duty cycle to the proposed values for a design permits this multiplex simulator circuit to simulate the brightness of the design.

Keep Alive – The function of the keep-alive element, available in most displays, is to provide a continuous source of ionization in the display envelope. Electrically, a keep-alive is another cathode. Its use permits shorter anode on times, longer refresh periods, lower ionization voltage and lessened need for power supply filtering as well as faster initial ionization. In general, keep-alive use expands the per-

formance range of a display in many circuit applications.

Only one keep-alive cathode per display (there may be more) need be energized with a continuous current of approximately 25 microamperes. To be effective, a keep-alive must conduct even though its anode is off. Fig 8 shows several methods by which the voltage is developed for continuous keep-alive operation.

A minimum of 160 volts is required to insure continuous keep-alive current flow. For a typical anode off voltage of 140 volts, the keep-alive should be returned to a potential at least 20 volts more negative than ground. As an alternative, the anode may be bypassed with a resistor as shown in Fig 8 (e). Another method for conventional multiplex operation, Fig 8 (b), uses a power supply providing -200 volts for the keep-alive. This large negative potential improves initial turn-on time and insures keep-alive conduction regardless of anode off voltage. Because keep-alive current is small, the filter capacitor can be small. Fig 8 (d) shows how to obtain the required negative voltage using a DC-to-DC converter with single output.

A means of calculating the keep-alive resistor value is provided in Fig 8 (c). For example, the total available keep-alive voltage is 160 if the anode off voltage is 140 and the keep-alive cathode is returned to -20 volts. Since the anode-to-cathode voltage drop for a keep-alive is about 135, the remaining 25 volts must be dropped across the resistor. A 1-megohm resistor would be required to limit keep-alive current to 25 microamperes. Should more than one keep-alive for applications using several displays be used, a resistor is required with each.

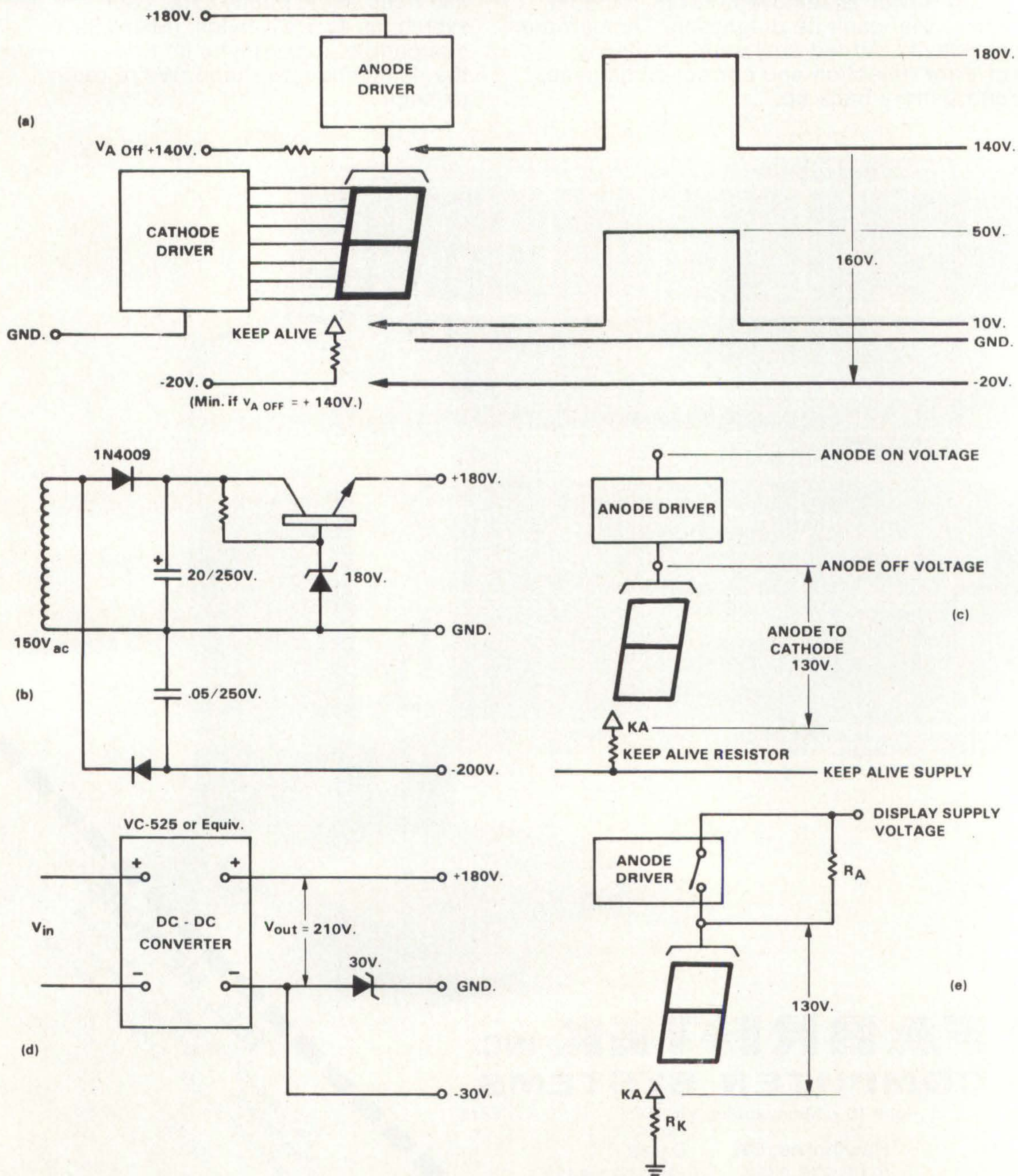

Fig 8 Several methods for keep-alive operation.

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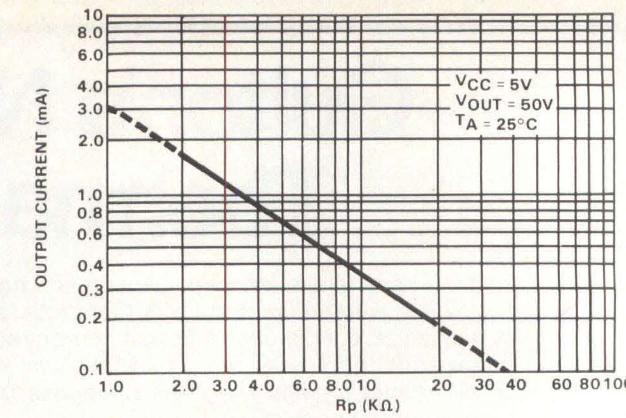


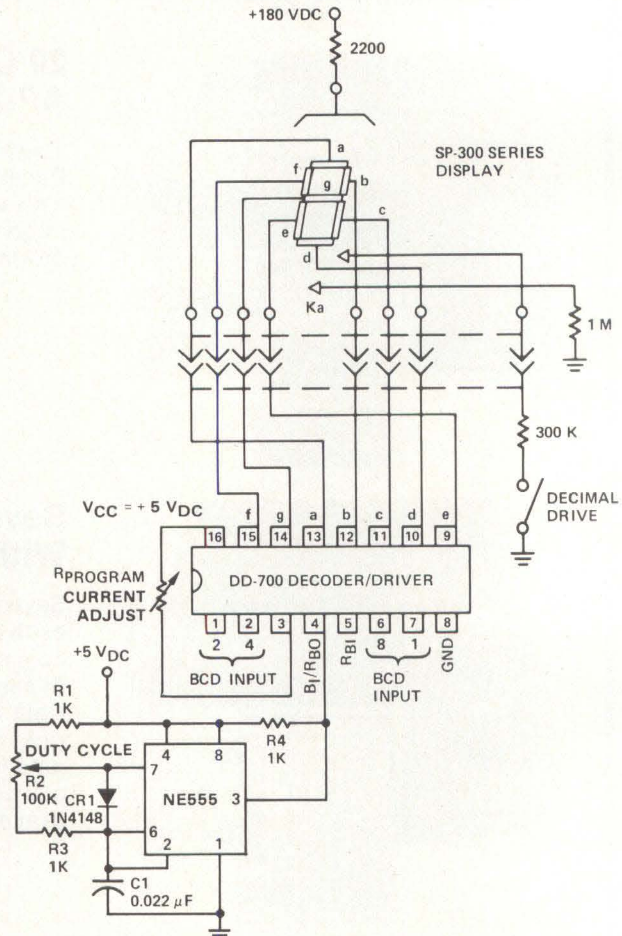


Fig 9 Suggested circuit for display brightness test.

Fig 10 is a typical multiplex circuit with discrete anode and integrated circuit cathode drivers. Its timing could be provided from a CMOS or TTL circuit or from an integral part of an MOS LSI clock, calculator or microprocessor chip. Fig 10 (a) is a discrete anode drive for active high input. When conducting, the NPN level shifter acts as constant current sink for the PNP anode switch, thus avoiding a need for a series resistor between NPN collector and PNP base. Fig 10 (c) is basically the same as 10 (a) but with an active low input. The 220 kilohm resistor connected between the display anode and the V_A (off) bias point allows use of a lower voltage PNP switch and insures that the anode is pulled to "off" by preventing any leakage across the PNP switch.

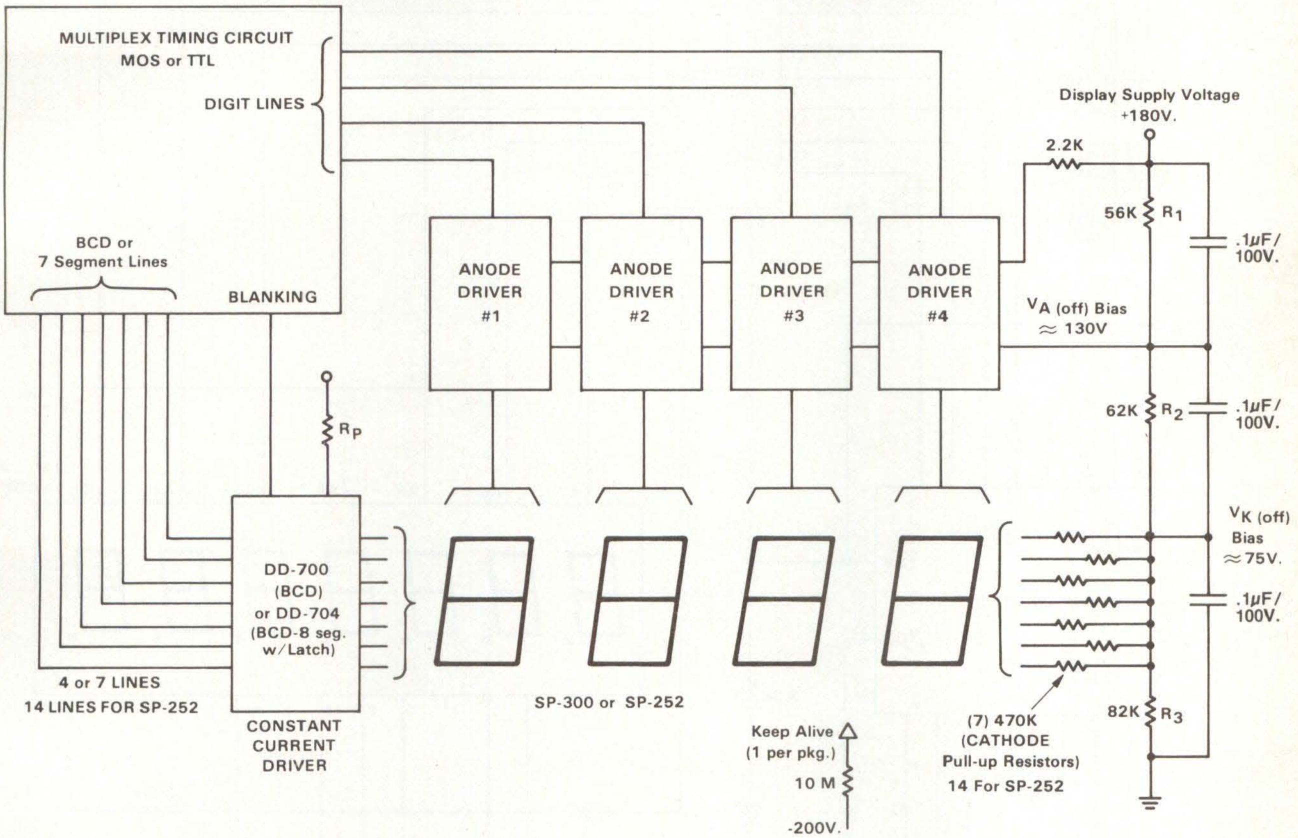
A discrete constant current cathode driver is shown in

Fig 10 (b). Use of a constant current driver insures constant brightness of the display with changing power supply voltage. The 470-kilohm pullup resistors help turn the display off quickly, allowing faster timing to be used. These resistors also protect the NPN transistor from over-voltage and prevent non-selected segments from glowing.

multiplex circuits using high voltage IC drive

The Beckman multiplex circuit shown in Fig 11 incorporates integrated circuit high voltage drivers. The Motorola anode drivers have an internal active pulldown and internal biasing zeners and can provide a 50-volt swing. A single current limiting resistor is used to provide about 0.5 mA for the zeners and switches. Where multiplex circuit lines are active high, the MC3490P is used; where the digit lines are active low, the MC3494P may be used.

The Dionics DI 300 cathode driver is both a level shifter and a constant current segment driver. It will level shift up to 200 volts below the logic levels and then drive the cathodes with a 100-volt, constant-current drive. To use this part in an application with fast timing and minimal blanking, cath-



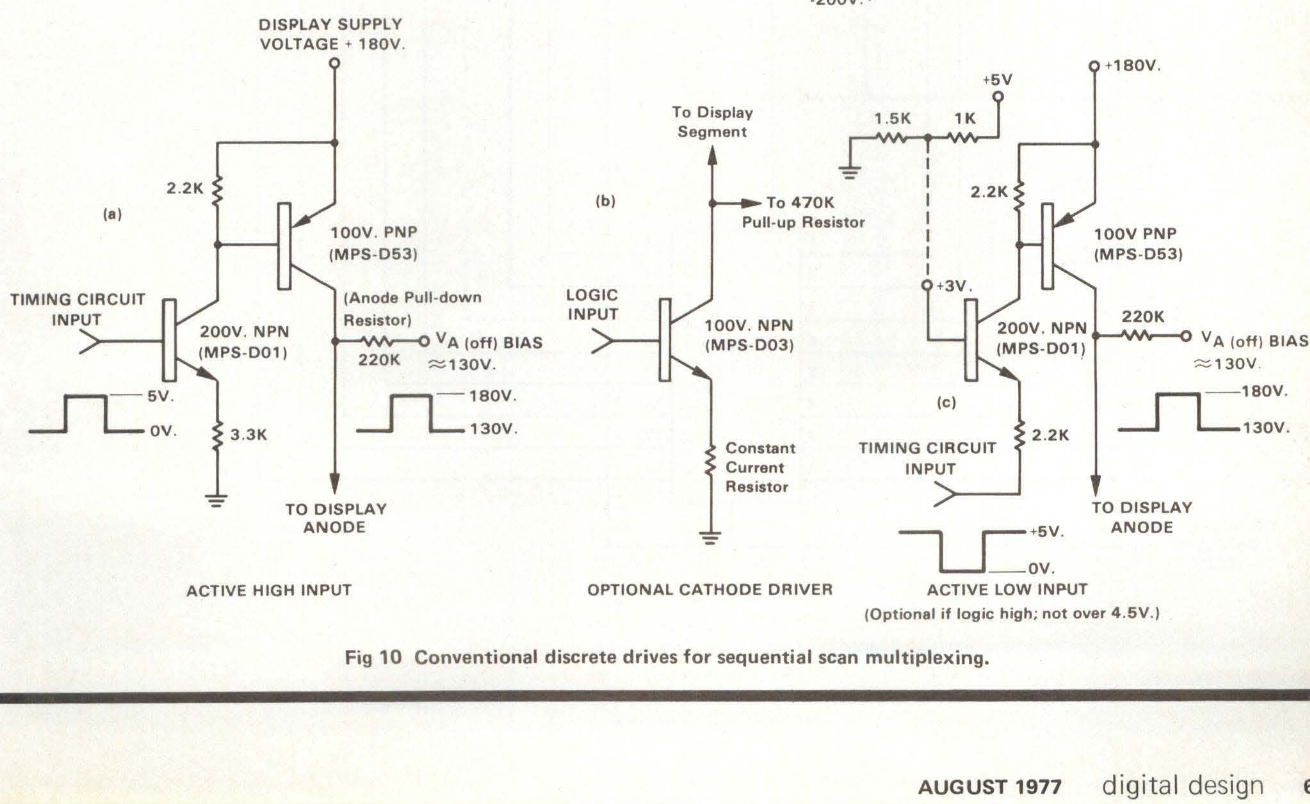


Fig 10 Conventional discrete drives for sequential scan multiplexing.

ode pullup resistors are necessary both to insure that the cathodes are turned off and to protect the driver. Since the DI 300 is rated for 200 volts, the total display supply voltage should be limited to a maximum of 200.

The circuit configurations shown in Fig 12 may be used with an MOS chip which has a 40 to 50 volt swing. Its digit selecting outputs must be active high, with enough current capability to handle seven times the chosen segment current. Segment selecting outputs should be active low (pull high, to V_{SS}, in the non-selected state) and have a current capability of twice the chosen segment current.

Display digits are turned on by pulling their anodes high (to V_{SS}); the 220-kilohm pulldown resistors turn the digits off by preventing any leakage across the MOS output. The display cathodes are biased at -110 volts by the 1N914 diode. When a segment output of the MOS chip is pulled high, the segment is turned off. When the segment output is open, the current limiting resistor [47 kilohms in Fig 12 (a)] pulls one

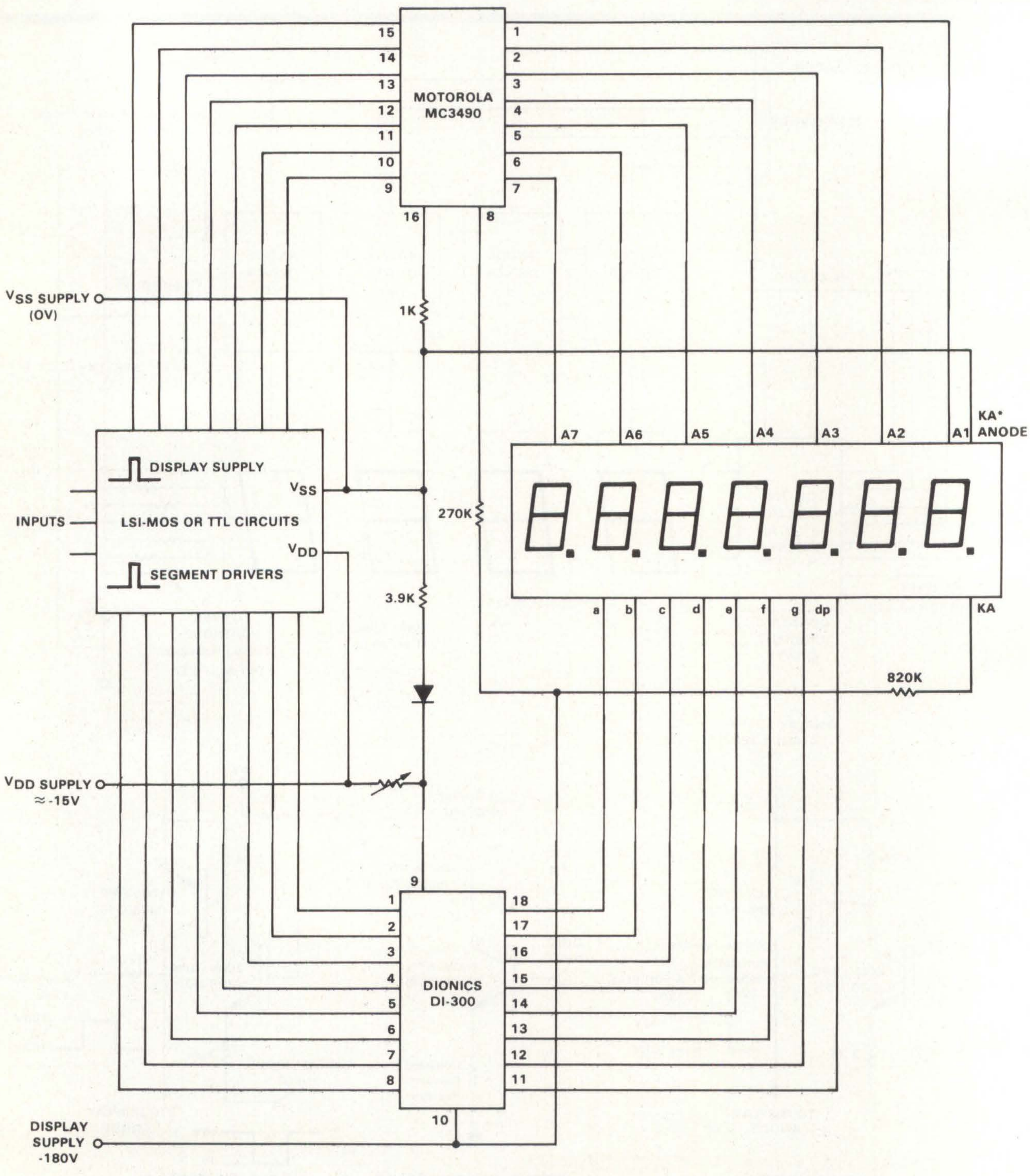


Fig 11 High voltage IC drive for multiplexing.

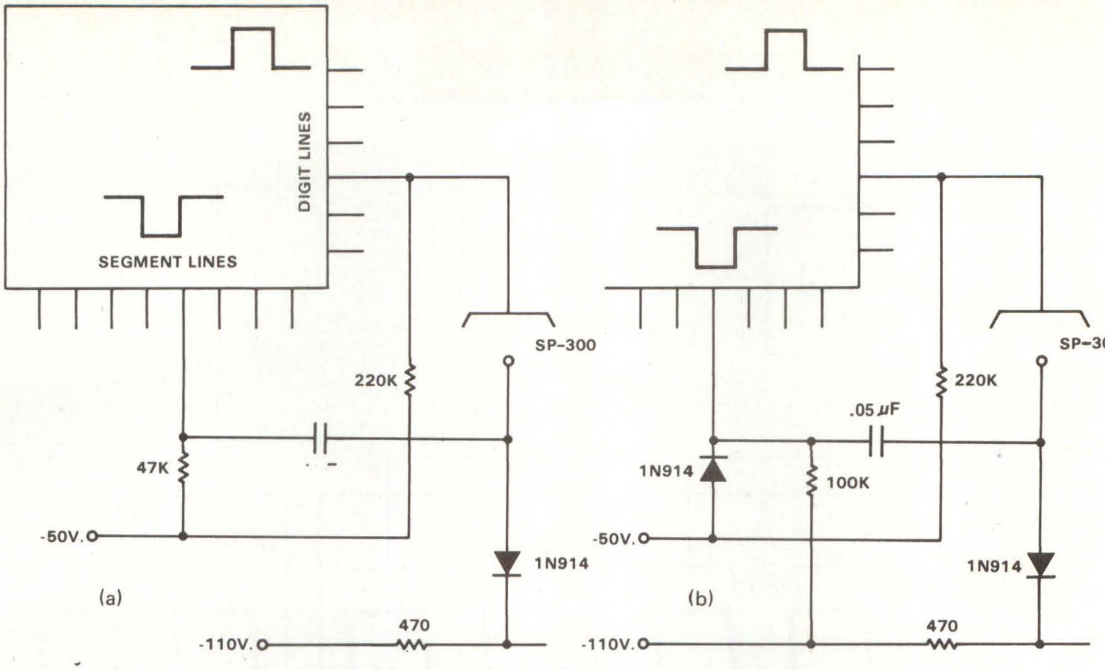


Fig 12 AC coupled high voltage MOS drive for multiplexing.

end of the capacitor to -50 volts. The capacitor couples this 50-volt change in the negative direction to the cathode, the diode allowing it to be added to the -110 volt bias. The resulting -160 volts is sufficient to ionize the digit.

Fig 12 (b) is essentially the same circuit but with a resistor to -110 volts and an additional diode used to protect the segment driver. The same cathode current will be obtained with a smaller capacitor. Protection against power supply transients is provided for the cathode biasing diodes by a single 470-ohm resistor. *(Continued next page.)*

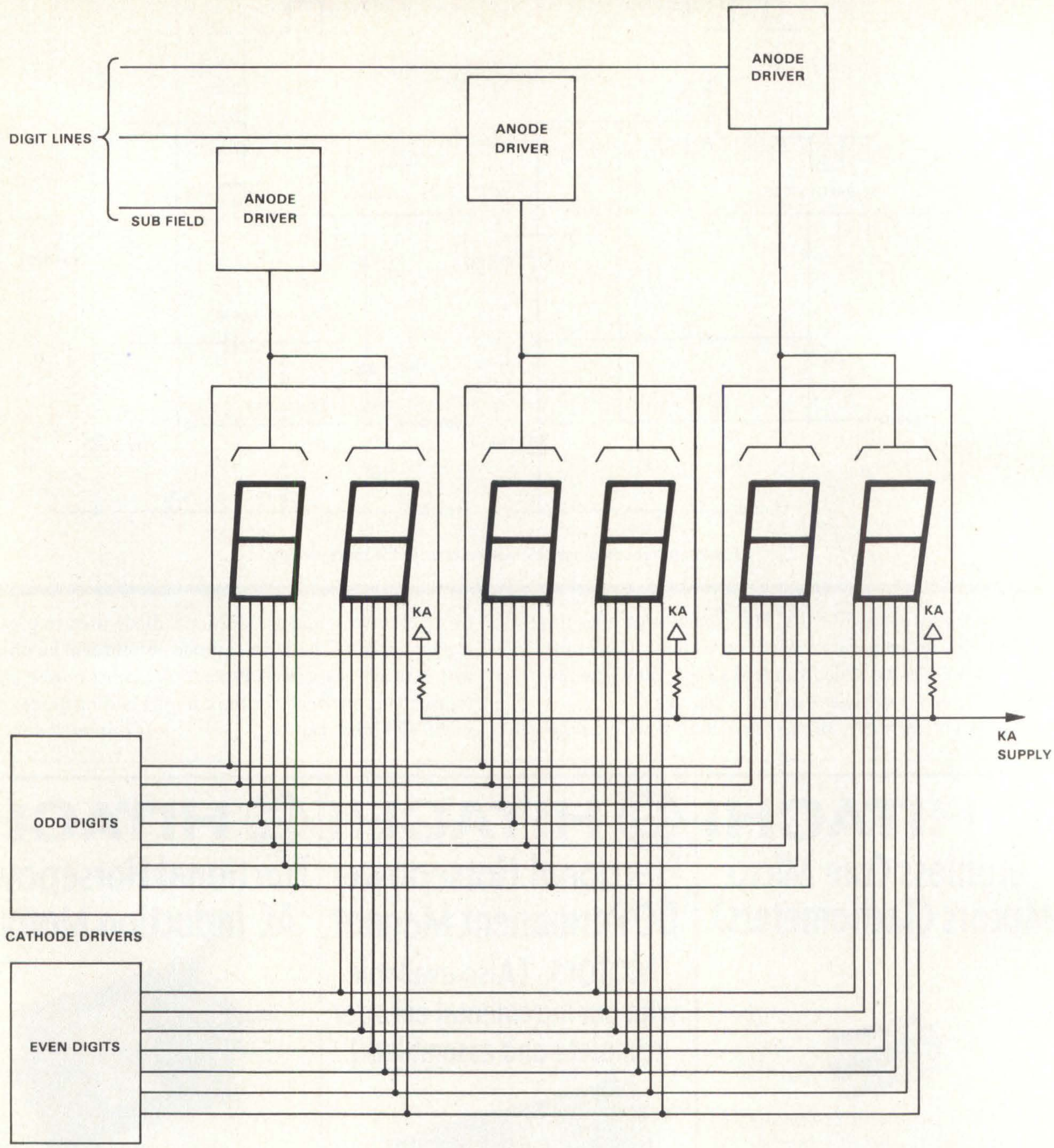


Fig 13 Split cathode operation for multiplexing.

multiplex circuits using split cathode operation

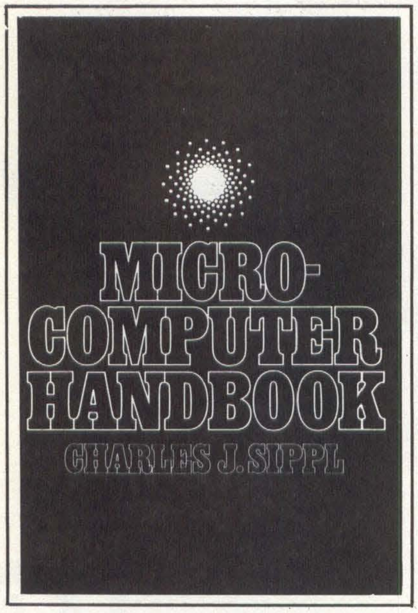
The duty cycle may be so low, when sequential scan multiplexing a very long display field, that brightness may be inadequate. Fig 13 shows how the overall duty cycle may be doubled or tripled by splitting a field into two or more subfields and addressing them simultaneously. Also, by using two-digit displays in a dual decoder scheme or three-digit displays in a triple decoder scheme, the requirement for interdigit blanking is eliminated since all digits in a given package are being addressed at the same time. This split cathode scheme also reduces the number of anode drivers required since one driver can control two or three digits.

multiplex circuits using interlaced scan

Adjacent digits are never scanned in sequence with interlace scanning. For example, a scan of digits 1-3-5-7 would be followed by one of digits 2-4-6-8. Interlace scanning eliminates interdigit blanking, thus eliminating streamer problems. A larger number of multiplexed digit positions is impossible because no interdigit blanking time is required.

Robert Kuntz *is product Manager,* **Dave Sien** *is Applications Specialist, and* **Wayne Wong** *is Field Support Engineer in the Information Displays operations at Beckman Instruments in Scottsdale, Arizona.*

Stacked Microprocessors A Better Way To Go?



The following discussion of stacked microprocessors is an excerpt from the Microcomputer Handbook by Charles J. Sippl. Published earlier this year by Petrocelli/Charter, the book covers the basics of microcomputing; it includes hardware fundamentals, programming, development and testing and a variety of applications. You can order the 480 page Microcomputer Handbook for $19.95 direct from Mason Charter Publishers, 641 Lexington Ave., NY 10022.

Exciting, low-cost, and extremely fast throughput advantages have led to coordinated groups of microcomputers that already outperform many of today's standard computers. The difference between a multiprocessing system of, say, 16 microcomputers and 16 standard computers working independently is that the multimicroprocessors share memory; that is, some of the primary memory can be addressed by two or more machines. A more common technique in today's standard computing world is multiprogramming. Multiprogramming means that more than one program can reside in main memory at a time and the central processor can switch among them. This means that the CPU does not have to remain idle while waiting for a job's input/output to be completed. Whenever a job must wait for an I/O operation (it sometimes takes a long time to read some data from a file into main memory), the operating system looks over the set of other jobs in main memory and chooses one whose I/O operation has been completed. If there is more than one CPU, many problems are solved and the user has—multiprocessing. If a job starts running on one processor and is stopped while waiting for I/O, it may be restarted later on another processor. Generally, multiprocessing systems come in two types: master/slave or symmetrical. In a master/slave system, one processor (not necessarily similar to the others) controls the rest. From the user's point of view, the maxicomputer, the Control Data Corp.'s (CDC) 6600 is an example of such a machine.

With LSI, speed limits are imposed only by the speed of light. Electric current moves only one foot per nanosecond.

In England, several of the units have been combined to share the work load. In addition to the truly modular systems in which processing capability is added in units rather than by system replacement, the use of multiple processors of the same design has added greatly to system reliability. Low-cost processors easily operate in tandem and choose jobs in priorities. Several "spares" are added, and, in the event of one unit's failure, to ensure system integrity, the next "spare" takes over. This is not the case for many

[5] *Electronics*, November 28, 1974.

Engineers

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CIRCLE 38

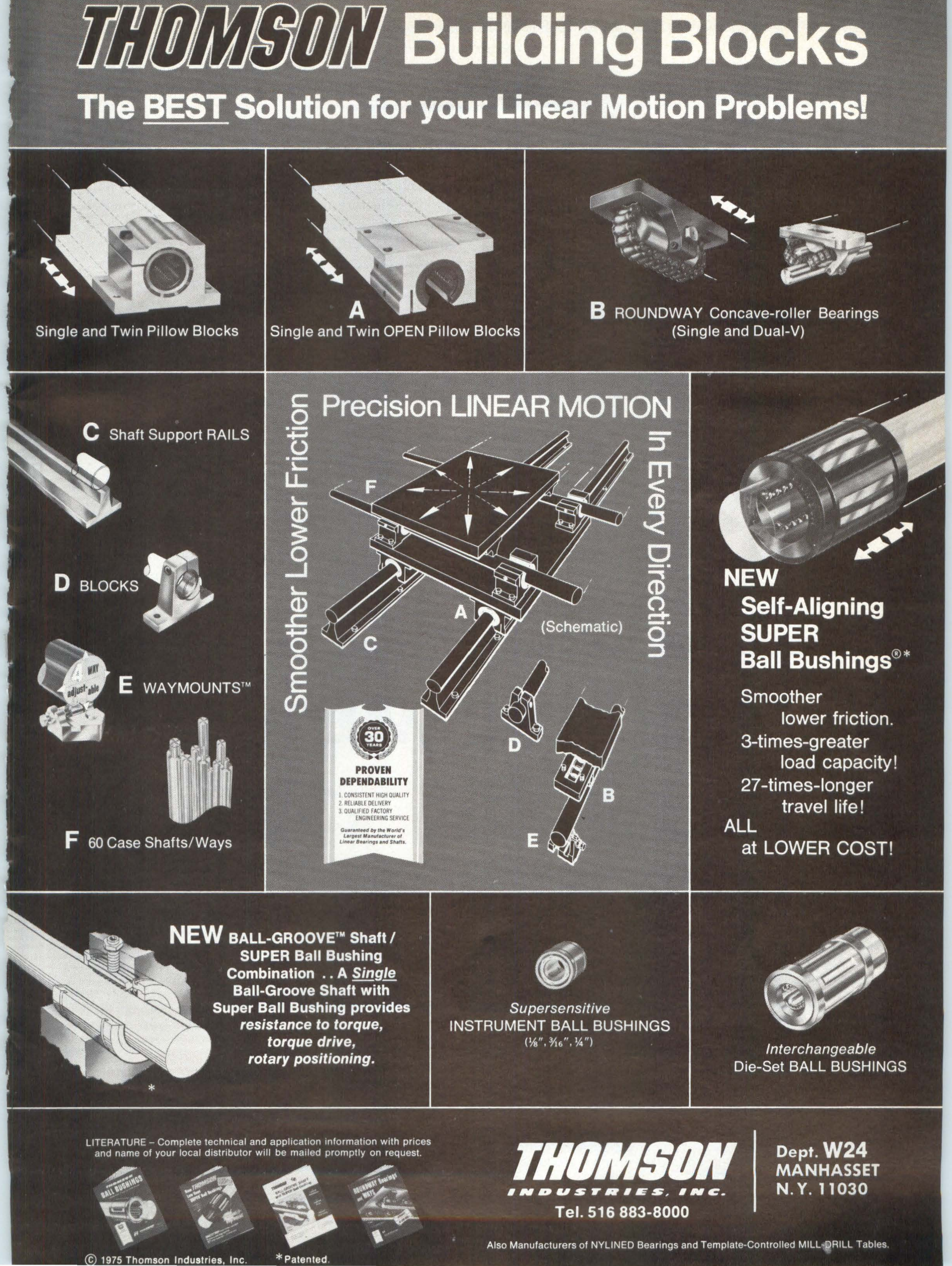
large computers that use multiprocessor designs. Several units in the micro systems are always identical. They might as well be built of many of the same units because they are so cheap. Systems may use one microprocessor for a storage manager; another, for communications; and still others, for compilation, execution, and job scheduling. They provide performance equivalent to current million-dollar systems for only a few thousand dollars. Although the speed of individual microprocessors may be limited, several units now easily run out of phase with each other to provide smooth, fast, and powerful processing. Races between memory speeds and processor speeds are forcing new architectures to evolve utilization of the latest technological states of the art, as they have in the past.

Economies of scale have been obliterated. Function alone no longer defines the types of computers that are purchased. Ranges of systems from pocket-calculator types through centralized giants do share technology but not design. Micros have new functions, new power, new component speeds, and great new system capabilities. Wide ranges of user firms have been seeking new ways to use new microcomputers—to control very fast processes like graphic displays, plotters, radar, and so on.

Advantages of Stacked Microprocessor Systems

Most considerations for the use of "stacked micros" are much the same as for multiminicomputers with the exception of three characteristics: shared memory, low cost, and microprogramming capability. Many microcomputers have limited execution rates; that is, the system throughput is limited by the processor rather than memory. This means that several micros can share the same memory without seriously degrading individual execution rates. Their low cost (compared to costs of memory and peripheral devices) allows the use of many microprocessors in one system. This more than offsets the lower throughput of a single processor and reduces the importance of utilizing each processor to maximum capability. Microprogramming further allows the use of special instructions that aid in satisfying control requirements. The advantages of implementing systems with many micros solve several system control problems and offer approaches to solving many others. Many of these advantages may be realized with multiprocessor systems. In general, it may be said that

1. Throughput often increases almost directly with the number of processors although system cost increases by only a small amount.
2. Shared system resources offer an economic advantage by eliminating devices that would need to be duplicated in separate stand-alone systems.
3. Shared resources provide direct access to data that might otherwise require transmission from one system to another.
4. With many processors, the cost of a standby is small.
5. A spare processor that can be switched into the system to replace a failed processor may be provided.
6. Functionally equivalent processors are treated as unassigned system resources to be allocated as required to process incoming tasks (symmetrical multiprocessors can be used in general-purpose environments where processing requirements are constantly changing).
7. Any currently idle processor may be used for the next task to be executed, eliminating the need to wait for the availability of a dedicated processor specialized to that task.
8. Failure of an individual processor causes only slight degradation in system capabilities rather than complete failure of an assigned system function (symmetrical systems require that every processor have full capabilities).
9. Systems are able to assign any task to any processor and set up interprocessor communication when required without the complications of software of single large systems processors.



Systems may use one microprocessor for a storage manager, another, for communications; and still others, for compilation, execution and job scheduling.

10. Individual processors can have fixed specialized processing functions; that is, the asymmetric class is typically used in dedicated applications where type, frequency of occurrence, and relative importance of tasks are known in advance; processors may be specialized to carry out one particular type of task. For example, one processor may perform all I/O operations; another may provide floating point arithmetic capability; a third may provide file maintenance; and so on.
11. Specialization may occur via the software programs executed, as well as the microprogram (which implements the processor's instruction set) and hardware architectural features (for example, number of registers, interrupt capabilities, and stack processing).
12. Each specialized processor is kept busy a sufficient amount of time to justify its cost. When low-cost microprocessors are used, utilization does not have to be exceedingly high to justify addition of a new processor.
13. Simplication of programming is developed because each task can be treated as an independent module, with no provisions required for execution of other tasks by a given microprocessor.
14. Switching matrices can connect any processor to any memory (or peripheral) in the system. This allows many processors to utilize simultaneously many different memory modules, reducing memory reference interference between processors.
15. All processors, memories, and peripheral devices can be multiplexed over one data bus (or a limited number). This is a very low-cost approach, and cost increases negligibly with the number of processors. The infrequent memory reference characteristics of stacked micros makes this organization attractive.
16. The asymmetric processor with multiplexed bus appears to offer the best cost advantage for stacked micro implementations and is of simpler organization than the others.

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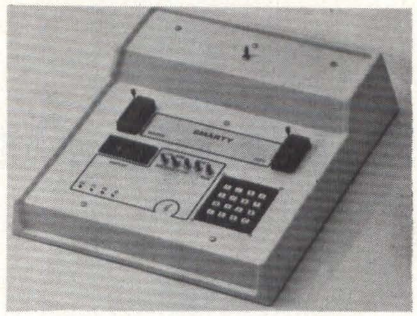
A solid state charge-coupled device, the semiconductor CCDISC memory has an ultra-fast average access time of 250 μs. Applications include communications, airborne systems and severe shock and vibration environments. CCDISC memories can serve in fast buffer, paging, scratch pad, program-swapping, time-sharing and distributed network applications. The memory unit has a capacity of up to 1024K bytes in 128K byte increment plug-in circuit memory boards. Capacities of up to 4 megabytes can be achieved by daisy chaining. A standby power system, available as an option, provides up to 30 minutes of power for a megabyte of memory. Controllers for

most computers, including Data General and DEC minis, are available. Price in OEM quantities is $3195 each. Alpha Data Inc., 20750 Marilla St., Chatsworth, CA 91311. (213) 882-6500. **Circle 126**

SYSTEM PROGRAMS AND EMULATES PROMS

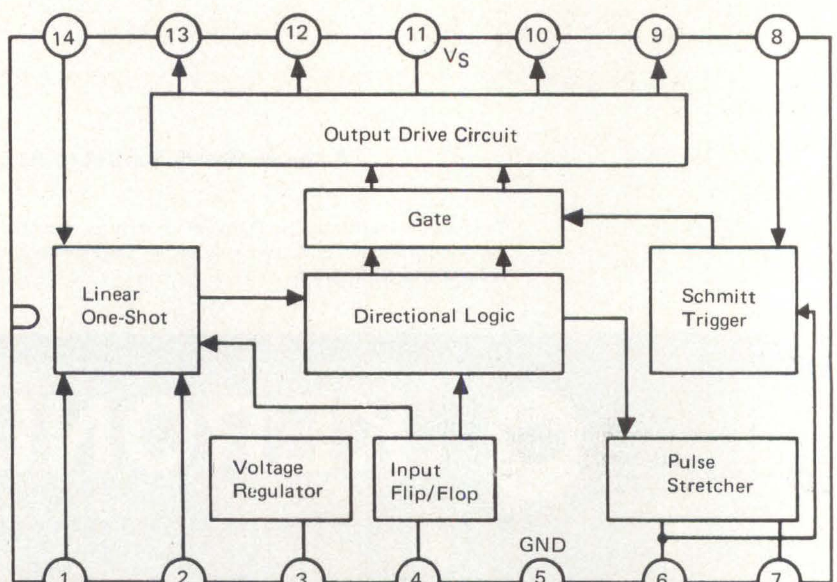
An MPU based programmer/emulator with slave expandability, the Smarty contains an RCA 8 bit CMOS microprocessor, 1Kx8 Data RAM, 128 byte scratch pad, parallel and serial data interface, 2704/2708 programmer and hexadecimal keyboard, display and indicators. PROM data is loaded into the Data RAM by TTY using the built in RS 232 or 20 ms current loop interface, by high speed paper tape reader, by the optional Cassette Data Storage Unit, by



built in keyboard or by reading an existing PROM or ROM through the Master socket. System software includes fault tolerant input/output subroutines for BPNF, Hexadecimal, packed Binary, ASCII/HEX or user defined format. The software provides multiformat input and the parallel and serial I/O buffers permit interfacing with any kind of peripheral. The user's system accesses the Data RAM just like it was a PROM or ROM. Output can be packed Binary, BPNF, HEX, Octal, HEX/ASCII or user definable format. Cost: $1495. Sunrise Electronics, 228 N. El Molino Ave., Pasadena, CA 91101. (213) 963-8775. **Circle 165**

SERVO AMPLIFIER IC INCLUDES MOTOR DRIVE

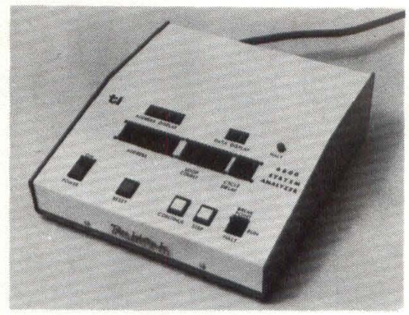
The NE544 servo amplifier IC integrates all basic servo amplifier functions including motor drive. Designed for remote control applications in digital proportional systems, it can be used in other closed loop position control applications. The NE544 combines a servo amplifier with a pulse width demodulator containing integral motor drive transistors. It includes an internal voltage regulator, low standby power drain (typically less than 6 mA), 500 mA load capability, high linearity with 0,5% maximum error and a maximum supply voltage of 6 V. The NE544 is available in three basic packages (14-pin N, 16-pin N, and 16-pin miniature WJ). Philips, P.O. Box 523 Eindhoven, The Netherlands.



product news

ANALYZER DEBUGS 6800 SYSTEMS

Designed to assist the microprocessor system designer, Telcons 6800 analyzer incorporates individual hexadecimal address and data displays, thumbwheel selectable address, loop count and cycle delay for use in break point and



halt modes. Single step operation debugs software by manually stepping through the program; breakpoint operation executes the program until reading the selected address, at which time the program enters single step. Price: $995.00. Telcon Industries Inc., 5701 N.W. 31st Ave., Ft. Lauderdale, FL 33309. (305) 971-2250. **Circle 128**

SWITCHING SUPPLY OUTPUTS 200 WATTS

Designed specifically for computer and computer peripheral applications the DA200 series of switching regulated power modules operates from user selectable inputs of 115 Vac± 10% single phase or three phase Wye, or 230 Vac± 10% single phase or three phase Delta. Three units are available with outputs of 5 Vdc, ± 12 Vdc and ±15 Vdc with total power of 200 watts. Full power is available at ambient temperatures of 35°C with 50% derating at 71° C. Line and load regulation is less than 0.5%; peak-to-peak ripple is less than 100 mV. Each unit includes overvoltage protection, short circuit protection, overtemperature shut-down and remote error sensing. Abbot Transistor Laboratories Inc., 5200 W. Jefferson Blvd., Los Angeles, CA 90016. (213) 936-8185. **Circle 145**

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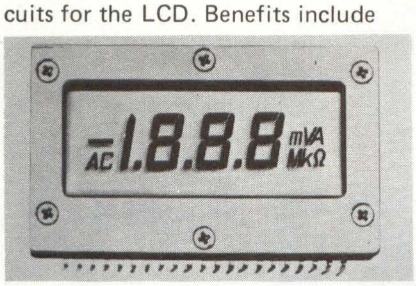
The 2020 Teledisk ASCII terminal uses 5-1/4" mini-disks for low-cost storage and random access retrieval of data. Storing and transmitting the equivalent of 37 CRT screens of data (71,680 characters) or 13-1/2 pages of 8-1/2" x 11" printed material, Teledisk has two RS-232 interfaces for attachment to any

asynchronous ASCII terminal and modem. The 2020 operates in read, write, find, insert, erase and address modes with operator prompting, and is 103/113/202 modem-compatible. Typical applications: time sharing, communications, data storage, cassette or paper tape replacement, extended memory buffer and mini-micro/computer loading. Price is $1750. Research Inc., P.O. Box 24064, Minneapolis, MN 55424. (612) 941-3300. **Circle 127**

LOW COST DISPLAY WITH A-D CONVERTER

A low cost 3½ digit liquid crystal display with an integral one-chip C-MOS LSI A-D converter employs the field effect method. The A-D converter, a linear C-MOS and a digital C-MOS, includes oscillation and driving circuits for the LCD. Benefits include



small size, light weight and several hundreds of hours of continuous usage when battery driven. Symbols of AC or – are displayed before the four numerals; units of m, V, A, M, K and Ω are displayed after the numerals. EPSON products are manufactured by Shinshu Seiki Co., Ltd, Japan. Epson America, Inc., 23844 Hawthorne Blvd., Torrance, CA 90505. (213) 378-2220. **Circle 166**

PRINTER OUTPUTS 2000 LINES/MIN

A microprocessor controlled line printer runs at 2000 line/min., single-spaced, using a 48 character set with a fully buffered print line of 132 characters. The controller communicates with the host system, decodes all commands, controls the printer hardware and reports various errors and status. An optional in-depth fault locating and hardware timing diagnostic panel plugs into the controller, providing off-line maintenance independent of the host system. The DOC 2000 handles up to six-part forms. Vertical line spacing is at 6 or 8 lines per inch. The printer also includes a powered forms stacker and an acoustically

insulated cover, interchangeable character arrays and a universal character set buffer allowing any character set to be used. The DOC 2000 line printer is OEM priced at $36,000.00 for single orders and $28,000.00 for quantity orders. Documation Inc., P.O. Box 1240, Melbourne, FL 32901. (305) 724-1111. **Circle 136**

MULTIPLEXER BOARD INTERFACES DG COMPUTERS

The AMS-4000 four port multiplexer PC board accomodates up to four RS-232 devices (CRT's, printers, etc.) for interface with Nova, Eclipse or most Data General emulators. The multiplexer board is 15" x 15" with a selectable real time clock of 10 or 100 Hz, and each port has its own address and a selectable baud rate from 110 to 9600 baud. In small quantities the price is $600 each for the four port version and $500 for the two port version (AMS-2000). Applied Management Systems P.O. Box 4795, Whittier, CA 90605. (213) 696-2002. **Circle 151**

MOVING HEAD DISK SYSTEM SERVES LSI-11

The Phoenix 145 moving head disk system consists of a Phoenix C45L disk controller and power supply contained in a 5-1/4" chassis, an LSI-11 CPU, 28K semiconductor

memory, power sequencing/terminator and a DLV-11 serial interface enclosed in a 30" pedestal cabinet. The system can stand alone or accommodate other standard LSI-11 and 11/03 peripherals. The moving head disk drive has a 10 megabyte capacity which can be expanded to 40 megabytes and supports up to 14 Q bus I/O devices, a line printer and a 28K-word LSI-11 processor in the nine-slot backplane. The system operates with the DEC RT-11 operating system. Xylogics Inc., 42 Third Ave., Burlington, MA 01803. (617) 272-8140. **Circle 129**

CONVERTERS SERVE VIDEO APPLICATIONS

Two new video devices, the ADC 820, an 8 bit 20 MHz Analog to Digital Converter and the DAC 850, an 8 bit 50 MHz Digital to Analog Converter, are optimized for video applications. The ADC 820 resides on a single board, 6" X 8" X 1", and dissipates less than 7 W. Power requirements are ±12 V, +5 V, -5.2 V. It has an on-board low pass anti-aliasing filter at the input to the quantizer. Differential phase and gain are less than ½^{0} and 1% RMS. The DAC 850 D to A Converter is also 6" X 8" X 1", with the same voltage requirements. Dissipation is less than 5 W. It comes with 3 times or 4 times subcarrier output filters, or with no filter. Differential phase and gain are less than ¼^{0} and ¾% RMS. Prices: The ADC 820 costs $1650, the DAC 850 costs $525. Tektronix Inc., P.O. Box 500 Beaverton, OR 97077. (503) 644-0161. **Circle 132**

CRTs FIT GRAPHICS TERMINALS

A line of high deflection sensitivity post deflection magnification CRT's, both electrostatic and electromagnetic deflection types, range in size from 8" rectangular to 23" in diameter. The electrostatic types fit high frequency applications such as spectrum analyzers, medical waveform analyzers and high data rate computer displays. The electromagnetic deflection types are used for graphic displays, air traffic control, radar and other applications where a reduction in deflection power is most desirable. Thomas Electronics, Inc., 100 Riverview Dr., Wayne, NJ 07470. (201) 696-5200. **Circle 141**

product news

GRAPHICS TERMINAL INCLUDES HARDWARE ZOOM

The microprocessor-based *Cluster 1000* computer graphics terminal employs a digital TV display, refreshed out of local RAM at 60 Hz. The 416 x 312 pixel image is treated as a movable camera, viewing a 1024^2 bit picture data base, so that most interactions with the image are local and immediate. The terminal allows local implementation of such interactive functions as panning, zooming (1 to 8X), multiple split screens, write through and background grids. Cost: $14,990 for a complete terminal. NuGraphics, 3012A Scott Blvd., Santa Clara, CA 95050. (408) 249-8480.
Circle 159

μP CONTROLS MATRIX TERMINAL

The 1660 terminal has a 1200 baud transmission rate, 200 cps print speed, a 100% duty cycle ballistic matrix head with extra wide head to paper gap, microprocessor control to provide incremental and bidirectional printing, unique horizontal and vertical tabbing, multiple selectable fonts, control code functions and versatile forms handling. The printer employs a 7 x 9 dot matrix and provides upper and lower case print. Diablo Systems Inc., 24500 Industrial Blvd., Hayward, CA 94545. (415) 786-5000. **Circle 147**

DISK SYSTEMS COMPATIBLE WITH DEC/DG

Available with top loading disk cartridge plus fixed disk, the Data General-compatible 10 megabyte Model 3860 cartridge disk subsystem uses IBM 5540-like removable cartridges. The Model 3860 disks have 200 tpi track density, 2200 bpi data density, 2400 rpm and a disk access speed of 38 ms. The DEC PDP 11-compatible model 3850 disk subsystem incorporates a removable front or top loading disk cartridge plus fixed disk and may use four dual platter disk drives for up to 20 megabytes of storage. Model 3850 disks have 100 or 200 tpi track density, 2200 bpi data density, 1500 or 2400 rpm and disk access speed of 38 ms. Data 100 Corp., 6110 Blue Circle Dr., Minneapolis, MN 55435. (612) 941-6500. **Circle 148**

DPMs SPORT LED OR BECKMAN DISPLAYS

The Electro-Numerics 4000 series digital panel meters include 2000, 4000 and 20,000 count models. They offer high brightness LED and Beckman displays and operate at ±15% of nominal 115/230VAC, 47 to 400 Hz. Options include ratio input, floating differential input, parallel-latched BCD and special scaling. Electro-Numerics, Inc., 1811 Reynolds St., Irvine, CA 92714. (714) 549-8821. **Circle 138** digital design

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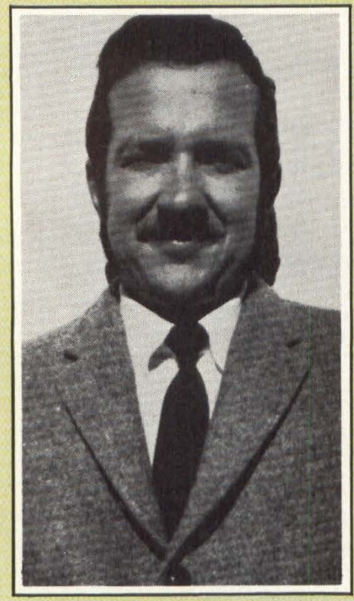

Future Microprocessor Software: Another View

Karl V. Amatneek's proposal (Viewpoint, May and June 1977) to use Boolean arithmetic operations as the basis for microprocessor software poses a number of interesting questions.

Do microprocessor manufacturers care enough about the market served by the logic designer? In the past, major marketing of microprocessors has stressed the low chip cost for large volume OEM users. Software costs in these applications can be a low percentage of the total dollar figure and manufacturers have been eager to provide programming and assembly support to land these large volume contracts.

Small users have to contend with the programming task on their own, sometimes spending excessive amounts of time and money in relation to the total project budget. A keyboard assembler/programmer such as Mr. Amatneek suggests could make these smaller microprocessor applications profitable, but how to put such standards into hardware and who will do so are other questions.

The experience of the IEEE and its interface standard has been sobering. While only the future will tell the ultimate impact of this standard, many manufacturers either ignore it completely (because it does not fit their product) or use parts of it under an in-house code name. It appears that a standard for microprocessor programming would meet a similar fate.

The cost of developing a keyboard assembler/programmer is large and without incentives for most chip manufacturers. The incentives do exist for some of the smaller firms specializing in microprocessor system support but there is no assurance that a sound market will coexist without the cooperation of the chip manufacturers.

Another problem that surfaces relates to the reduced power of the chip that occurs by limiting instructions to arithmetic operations. The power of microprocessors allows them to replace many times their equivalent in hardwired logic. This is compromised if branching and interrupt operations are not allowed. Some will argue that if these operations are permitted, then why not others which solve particular application problems?

Modern programming is largely based on the original concepts devised by von Neumann 30 years ago. Only recently have efforts been made to try to discard this method of operating on one word at a time and to think of a computer as a processing unit and a memory.

Drastically changing the contents of a memory such that it solves a problem in a better way generates greater computer power. But I doubt that arithmetic methods alone can achieve this kind of progress. Unfortunately, many microprocessor operations lack a mathematical foundation and it is just that that makes them difficult for the logic designer to use.

Mike Hordeski *is the president of Siltran Digital, Silverado, CA, and a member of the ISA Standards Review Board. We will be pleased to provide space for opposing views.*

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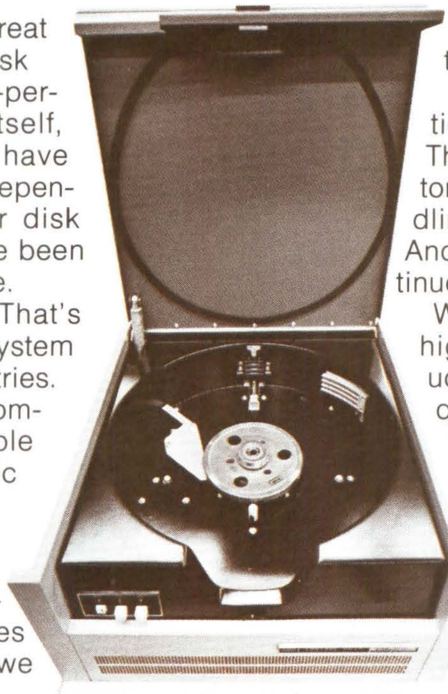

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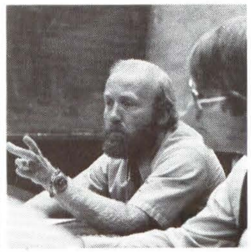

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