A MORGAN-GRAMPIAN PUBLICATION

Digital Design

COMPUTERS/SYSTEMS • PERIPHERALS • COMPONENTS • 11/15/83

VOL. 13
NO. 11

Designer's Guide To Disk Drives

• Solids Modeling • The Q-Bus • LANs

• Telecommunications • Plotters

Model 6455 Cartridge Tape System

Loaded with Features — Loaded with Benefits.

Kennedy products have always provided innovative new features. And these features have always provided added benefits and convenience for the user. For instance, our Model 6455 offers these features and benefits:

Feature: Start/Stop Operation

Benefit: Drive can emulate a ½" tape drive by providing the ability to perform selective file back-ups, file-restructuring, journaling and software updates.

The drive is effectively a ½" Tape Drive in a smaller package.

Feature: Hard Read Error Spec. of 1 in 10^{11} bits.

Benefit: Best data reliability of any tape cartridge drive. Gives the user confidence in the integrity of the back-up medium.

Feature: On-board Diagnostics

Benefit: Drive can be tested off-line with no test equipment required. Use of S.A. also lowers the MTTR.

Feature: Cartridge Jam Protection

Benefit: Protects the cartridge from damage if cartridge jams. This is accomplished by sensing a current surge and then disabling the motor, thus insuring that the cartridge will not be damaged.

Feature: High Density Recording

Benefit: Storage capacity of 23 MB on a single cartridge.

Feature: Optional industry standard ½" tape interface.

Benefit: Operates with existing tape couplers and software. The drive operates as though it were a ½" tape drive without having to modify existing hardware or software.

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The array processor plugs directly into your Multibus. Without fuss. And takes up only a single slot.

To the host, it looks like 64K of extra memory. With memory mapping, it's easy to access.

The processor has both fixed point and full floating point capabilities. Data flows to and from the board either through dual port memory or through the auxiliary high speed I/O port. Cycle stealing and simultaneous access of data can also be accomplished.

It can be ordered with standard algorithms in PROM. Or as a programmable version with RAM in program memory.

And behind this new array processor is a staff of engineers and programmers that offer, as needed, comprehensive hardware and software support.

The APB-3024 is fast enough for real-time analysis, versatile enough to handle almost any algorithm and simple enough to talk with easily.

Which is why the processor is in demand for military applications such as radar processing, simulation and C3 analysis.

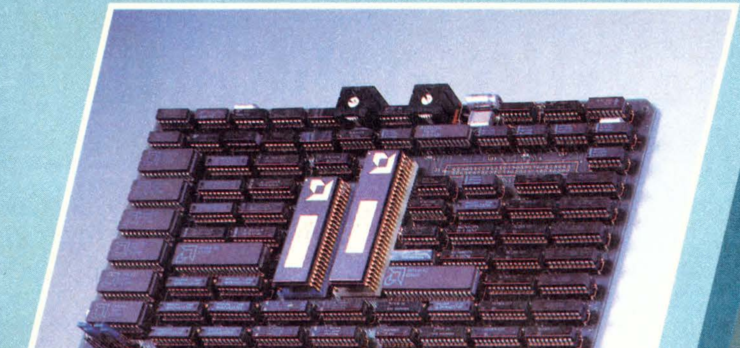
For commercial uses such as image processing, financial analysis, computer aided design and geophysical analysis.

And for such industrial tasks as vibration analysis and power transient monitoring and well logging.

Yet the price is only $4250. (Quantity discounts available.)

If numbers have you in a crunch, call us. We'll show you how to make short work of long problems.

Specifications:
Program memory 2K X 48 bit word **Data memory** expandable 8K X 24 bit word **Data word** 24 bits long, 8-bit exponent, 16-bit mantissa **Maximum Power Required** 25 watts **Standard Routines** fast fourier transform, power spectral density, inverse FFT, auto correlation and FIR digital filter



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Trademark: Multibus, Intel

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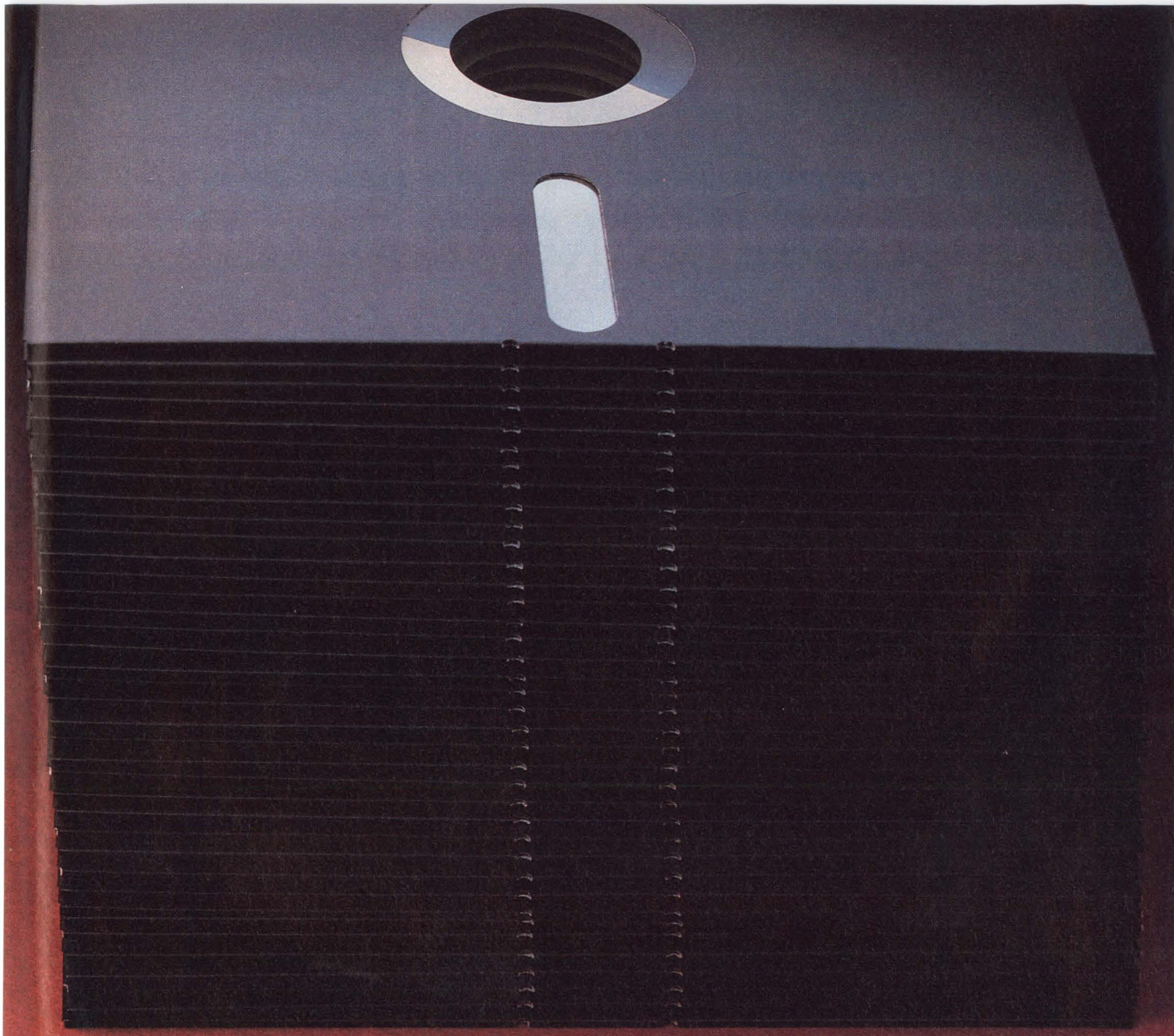
The design solution: Winchester

Save your customers time, space, and money with ¼" data cartridges.
When 3M invented the ¼" data cartridge, they designed it to be fast, dependable, small in size, and big in capacity—up to 67 megabytes today, with more in store for the future. No wonder more and more systems designers are finding it the perfect choice for backing up Winchester drives. 45 megabytes of data can be transferred from disk to tape in under nine minutes—with no time lost for media changes. One cartridge does it all! It would take a stack of 38 eight-inch floppies* to hold the same amount of data. The cartridge is small enough to fit in a coat pocket—and rugged enough to be transported that way, too.

New rules of standardization.
Industry standards are now being formulated which will improve interchangeability of ¼" recorded data cartridges across most major manufacturers' ¼" drive systems.



back-up that eliminates stack-up.

This means concerns about compatibility are diminishing.

The logical choice.

The ¼" data cartridge is the logical choice for designers specifying back-up systems for Winchester drives. It's small, reliable, easy to handle and transport, and has a very low cost per megabyte.

These high capacity cartridges are useful for archival storage and program loading, too. So don't wait, give your customers the future. Put this innovative technology to work in the next computer system you design. Data cartridge drives are available from over 30 manufacturers throughout the world.

For more information:

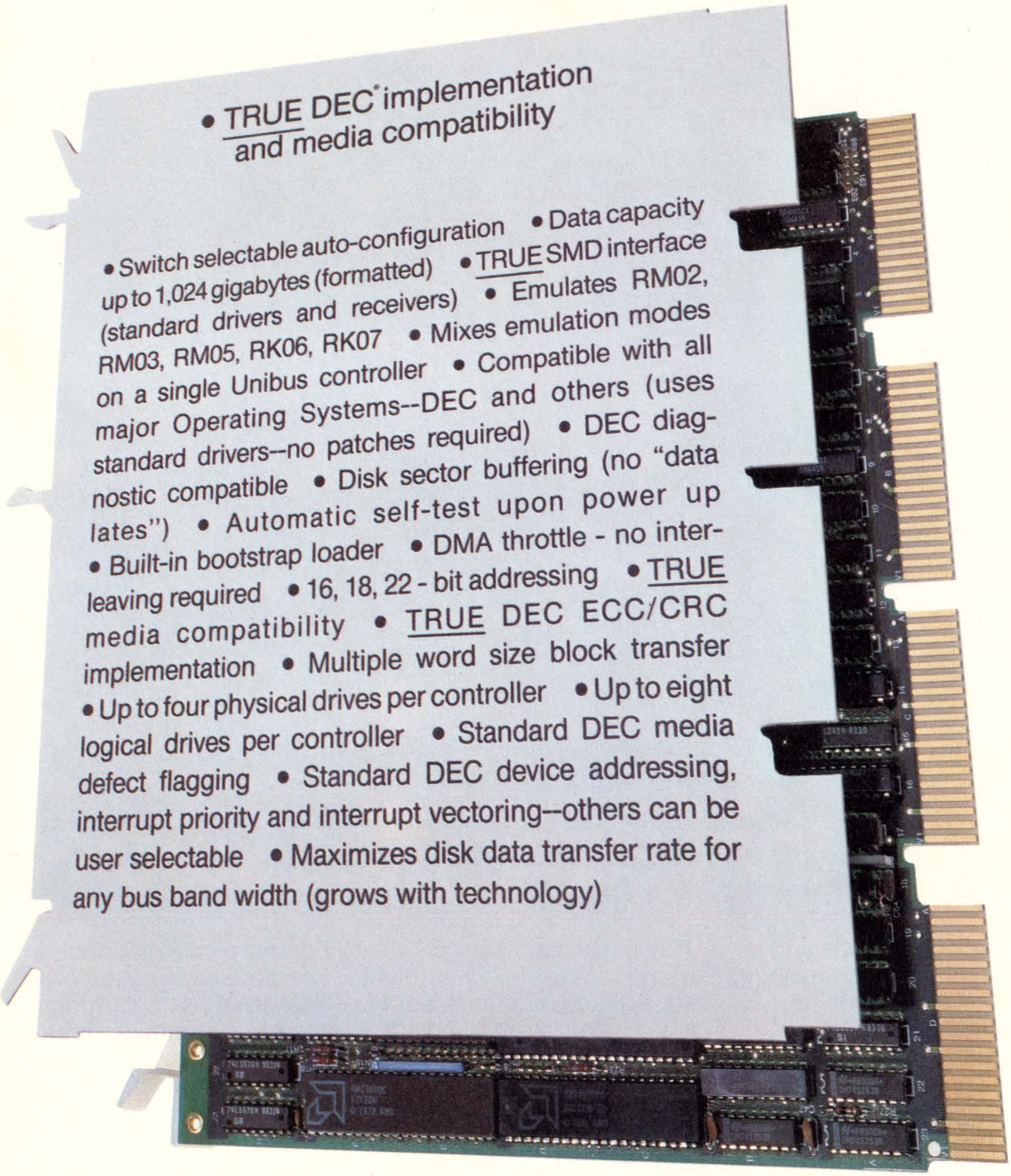
For more information on how 3M ¼" data cartridges can save your customers time, space, and money, write to Chris Binner, National Sales Manager—OEM Market, Data Recording Products Division, Building 223-5N, 3M Center, St. Paul, MN 55144.

*Double sided/double density 1024 format 8" diskettes.

3M hears you...

3M

20 major capabilities together for the first time on a single SMD controller!



Sometime a picture isn't as good as 10,000 words.

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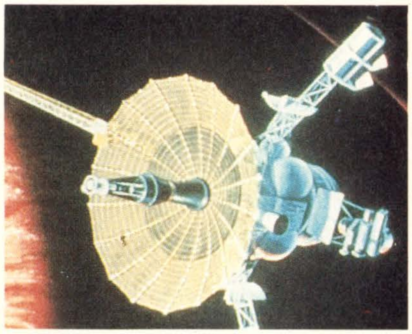
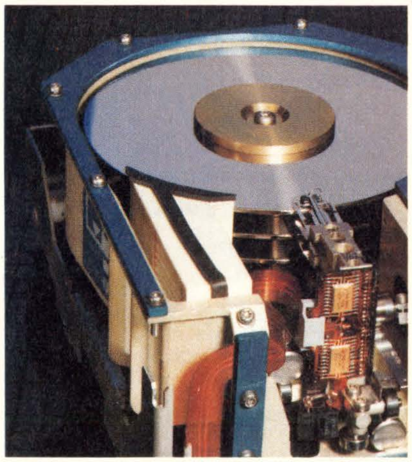
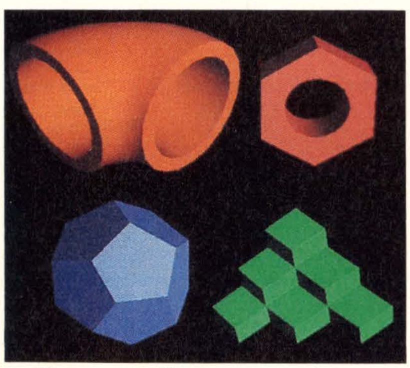


p. 30 *(Photo courtesy Harris)*



p. 39 *(Photo courtesy Evotek)*



p. 88 *(Photo courtesy Cubicomp)*

Cover

The PRIAM Winchester Disk Drive. PRIAM's family of Winchester products includes 14-inch (34, 68, and 158 Mbytes), 8-inch (35, 70, 85 and 105 Mbytes) and 5.25-inch (35, 71, 86 and 111 Mbytes) drives, as well as SMART-Series intelligent controllers. See page 39.

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COMPUTERS/SYSTEMS

PERIPHERALS

COMPONENTS

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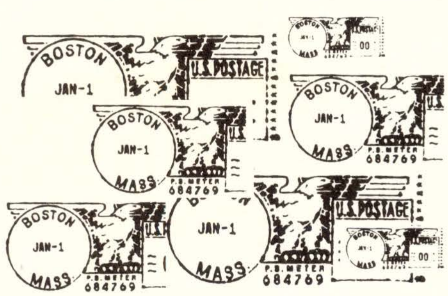

Please use the enclosed qualification form to notify us of your address change. A change of address requires that you fill out the entire form. Please allow 6 – 8 weeks for your change to take effect.

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Lundy's T5484 Color Raster Graphics Terminals have the highest color resolution available. Think of that resolution as a Super Hue—a 4097th color—that mixes with all other 4096 colors to make each as sharp as you've ever seen.

Our 5480 Series of color raster terminals and workstations aren't the only ones with 4096 colors. But the colors have never looked so good. Because resolution has never been higher.

New standards.

The 1536 × 1024 pixels set a new standard for displayable resolution. Raster staircasing is significantly reduced without the complexity of anti-aliasing.

But new standards don't stop with highest resolution. Areas are filled virtually instantaneously so the 5480 Series also sets a new standard for polygon fill.

Vector generation sets a new standard, too. The time lapse between the moment you draw until the picture is generated is as much as 50 percent faster than many others.

Enemy of obsolescence.

You shouldn't be forced to ditch programs in place when you buy a new terminal. For that reason, standard with all 5000 Series models is a Tektronix

Lundy's 5484 color raster design workstation.

4010 or 4014 Emulator with mixed-mode software switch for enhancing existing programs with color-native protocol.

Currently, our terminals can be driven by many of the leading software products. And the list is growing rapidly. Because Lundy is committed to an aggressive third-party software development program to provide the most comprehensive application packages.

Lundy will help you see more in graphics.

When you look at our 5480 Series, take a close look at Lundy, too. We're a company that's as good as its products.

A company that balances high tech with solid business sense.

A company as proud of its service (one of the largest service organizations in the industry—39 locations nationwide) as its engineering expertise.

A company you can count on to help you see more in graphics—and get more out of graphics—both now and in the long term.

For more information, write Lundy, Glen Head, New York 11545, or call: (516) 671-9000.

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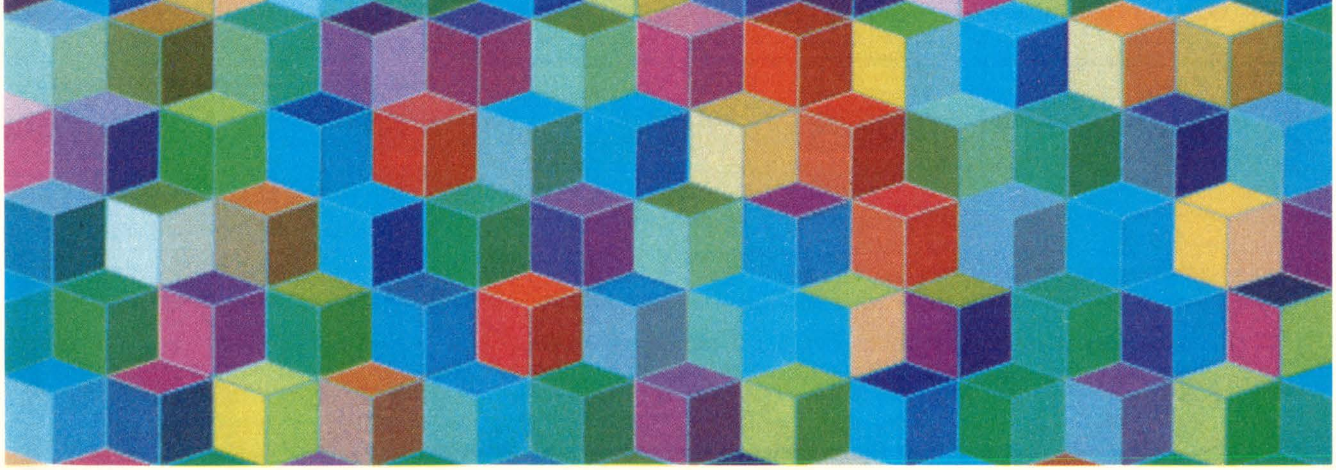
The Lundy 5688 displays 256 high resolution colors at a time. User downloadable character fonts; programmable character sizes.



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LEADERS IN PACKAGING TECHNOLOGY

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Tell us your thoughts

Digital Design is your forum — your inputs help keep the magazine interesting and vital to the design community. So let us know how we're doing and how we can serve you better in the future. We want to know what you like or dislike about *Digital Design*, the subjects you'd like to see us address, how you feel about the problems you face every day as design professionals.

If you have thoughts your peers should know about, put them in a letter in *Digital Design*. Have your say in *your* magazine! Send letters and comments to: Editor, *Digital Design*, 1050 Commonwealth Ave., Boston, MA 02215.

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Put powerful instrument control at your fingertips.

IEEE-488

The new Fluke 1722A Instrument Controller combines the computational ability and interfacing flexibility you need with the rugged packaging and easy-to-use human interface your factory demands. All at a new, low price. Now you can integrate your next factory test, process control or OEM system faster and put your people to work sooner.

The power of the 1722A is a 16-bit single-board computer with 136K bytes of main memory. Its 12 MHz speed puts it in the same class as many minicomputers. Four programming languages are available to simplify programming,including Interpreted and Compiled BASIC, FORTRAN and Assembly. Each includes special adaptations for controlling IEEE-488-compatible programmable instrumentation. And if you already own a 1720A Instrument Controller, you can run existing software on the 1722A—without modification.

The modular mainframe easily mounts in a standard 19 inch rack and allows you to configure the interfaces and memory to your exact needs. The IEEE-488 (1980) and RS-232-C interfaces can be expanded with an optional IEEE-488 and RS-232-C interface card, parallel interface card or dual serial interface card. Onboard memory is expandable to 2.6M bytes with RAM cards or 1.4M bytes with bubble memory.

The 1722A's touch-sensitive display dramatically simplifies system operation. Once programmed, your system can be operated entirely from the CRT. The 1722A displays only the pertinent options, allowing you to structure the user's response to a system. This helps reduce mistakes and increase throughput.

The 1722A is priced at $7450 (U.S. list), including BASIC Interpreter, documentation and a limited one-year factory warranty. So get in touch with your local Fluke Sales Engineer or Representative. Or call us toll free at **800-426-0361** for more information.

Use the new graphics capability of our 16-line, 80-character touch-sensitive display to create more effective operator prompts.

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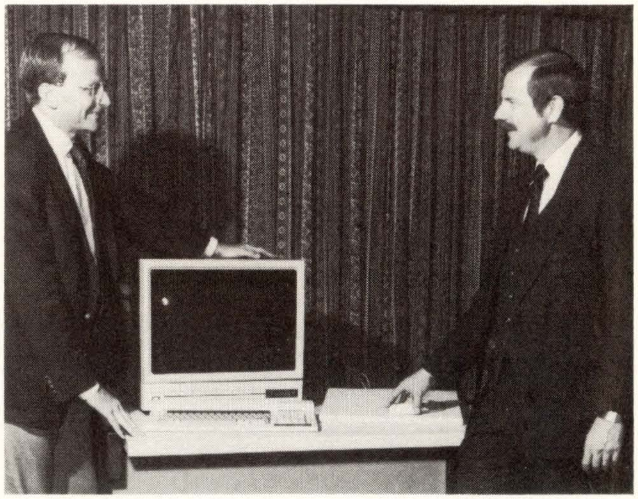
EDITOR'S COMMENT

During recent months there has been tremendous movement within the world of computer and electronics manufacturers. The recent collapse of Osborne Computers in Santa Clara has brought home many predictions about the imminent shakeout of the personal computer industry. The recurrent losses of several computer firms may indicate that other closings are soon to follow. At the same time, history repeats itself as larger manufacturers of computers such as IBM and Hewlett-Packard work to consolidate their market position and begin the war for percentage points of their competitors' sales. The rapid rise of IBM to leadership in the personal computer industry has made the PC important to the long term health of the company, rather than just being another successful product. With all of the wisdom of hindsight we can see that IBM's major reorganization in 1980 has had profound effects upon its ability to compete. The likely secondary benefits to IBM from the PC should be considered in light of new products offered for the computer by others. IBM has shown the willingness to use outside sources for expertise or technology that it may not have the time to develop internally. By design or by chance the impact of the PC provides the company with access to the means to move ahead of the growth curve in the remarkably volatile market of small computers.

Digital Equipment Corporation recently held "DEC-TOWN" at the Hynes Auditorium in Boston, this apparently the result of the recent reorganization of the company and indicative that it recognizes the need for more responsive marketing plans in changing times.

Events such as this may show that while the larger computer firms have relatively slow moving organizations, what was once perceived as a hindrance to competition in new technology does have its advantages. In light of Pioneer Osborne, we might conclude that the advantage is not always to the first entry. The economic success of a small manufacturer of computers may be dependent upon narrowly focussed technical expertise, where a firm the size of IBM is in the opposite position. Events within the marketplace also have less affect upon managers at larger corporations, DEC notwithstanding. Rather, these companies are able to benefit in times of adversity, refining their approach in response to events.

One of the most evident trends in response to both market changes and rate of change is apparent in the growing number of cooperative developments of technology. Chairmen and Presidents are willing to relinquish the "not invented here" approach and openly admit that technology is so complex that no one company can hope to accomplish everything. Control Data Corporation is a pioneer in the organization of technology consortia, indeed it was the effort of Chairman Norris that lead to the foundation of the Micro Electronics & Computing Consortium. CDC has had several successful experiences in the area over the last years. Sharing development costs for new technology reduces both capital outlay and the dependence of par-



Jerry Borrell and William N. Stout, President, Lundy.

ticipants on third parties which a system integrator may have little control. IBM's flexibility has allowed it to take part in these movements as well, perhaps best represented by its acquisition of significant shares of stock from ROLM and Intel Corporations. NCR which integrates several products in its sytems has similarly acquired a portion of its suppliers' stock, notably Convergent Technologies.

New areas of technology continue to be developed and announced, but once set into production success brings immediate emulation.

One area currently with a robust profile is that of the computer workstation. As one developer terms the growing attitude "JAWS" amongst system users, "just another workstation". The number of graphic related workstations for PC design, IC Design, general engineering applications, graphics arts, and office applications is proliferating—and is the subject of an article in the December *Digital Design*. While we might be tempted to draw further parallels from the small computer marketplace for the currently ebullient workstation market, the Editors of *Digital Design* have had ample opportunity to observe the uses to which these systems are being put. The basis for success of many workstation products is tied to the expanding market for system components as represented by the areas of bus technologies *Digital Design* has covered throughout the year; S-100, VME, Versabus, Multibus, Q-Bus, Unibus and others. The success of the secondary suppliers is limited only by their ability to react to new semiconductor products, and therefore to rapidity of design—the very market towards which the workstations are directed.

In summary, I see a healthy development continuing, despite possible Wall Street perceptions of what might become a "general shakeout" of the computer industry.

Jerry Borrell
Editor-in-Chief

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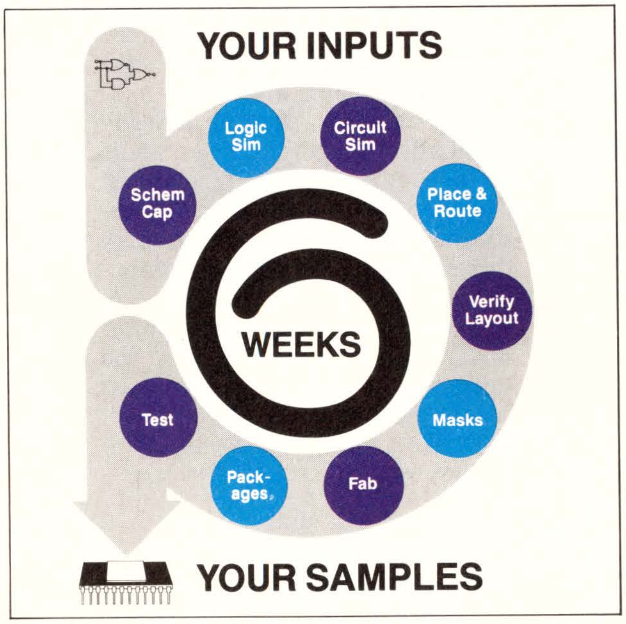

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Weeks 1 and 2—We computer-capture your schematic and create a net list. Next, we run complete logic and circuit simulations. Any problems are noted, discussed with you, and fixed. Then, we start developing the test program.

Week 3—Using computer assistance, we place and route your circuit. All functions are implemented with standard precharacterized macrocells.

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NEWS UPDATE

Level II COBOL for UNIX Market

Cadmus Computer Systems (Lowell, MA), and Micro Focus Inc., (Palo Alto, CA) have completed a joint development effort to place mainframe COBOL capabilities on high-performance, 68000-based supermicrocomputers and workstations. The LEVEL II COBAL compiler and Micro Focus VISUAL PROGRAMMING tools are the first application software packages ported to Cadmus 68000-UNIX based 9000 Series of high-performance systems and workstations. The software is the first outside-developed software to be ported to the UNIX-based Cadmus 9000 and the port connects Micro Focus software to the Cadmus Q-bus, which enhances existing compatibility with Digital Equipment Corp.'s VAX and PDP-11 minicomputers.

FAA Awards Design Contracts

As part of a program to replace the air traffic control computers used in the air route control centers, the Federal Aviation Administration has awarded two design contracts valued at $76 million to IBM and Sperry Corp. The nearly two-year long competition phase will end when the FAA selects one of the two systems to replace the IBM 9020 computer which is currently used by the FAA. The FAA placed the IBM contract at $40.5 million and Sperry's at $35.6 million.

Smart Card

Intelmatique, the international marketing arm of the French telecommunications administration, announced that the French Ministry of Post and Telecommunications will issue one and a half million Multi-Service Smart Cards in 1984. The smart card, which is plastic and the size and shape of a credit card, has one or more embedded microcircuit chips which are programmable and intelligent, with memory storage capabilities. The card will be used in a variety of consumer service applications. The present smart card point-of-sale trials in the cities of Blois, Caen, and Lyon are being conducted by the Post Office, French banks, and the telecommunications authority of the Common Economic Interest Group (GIE).

Marketing Peripherals

The Peripherals Marketing Association was recently formed to address the marketing concerns of manufacturers of computer peripheral equipment. The newly formed PMA is designed to be an effective tool in responding to common marketing interests, such as industry standards, sales channels, trade shows and government regulations. Membership includes over 20 companies who manufacture disk drives, tape drives, printers, terminals, controllers and/or other peripheral devices. For more information on membership and the upcoming meetings, please contact: Joseph Sheppard, President, Xico, Inc., 120 Ocean Way, Santa Monica, CA 90403, (213) 459-1044.

Systems Link Via Remote Line Printer

Digital Associates Corporation announced the availability of an interface for a wide variety of computer systems with the Xerox 2700 laser printer. Using its Remote Line Printer System (RLPS), Digital Associates has engineered a solution to the problem of placing a 12-page-per-minute Xerox 2700 laser printer in a location remote from a user's host computer. By providing both remote and local plug compatibility for the 2700 with many systems, including those manufactured by Digital Equipment Corporation, Data General, Hewlett-Packard, Prime, Tandem and IBM, more users will be allowed to take advantage of the 2700's unique print capabilities in an increasing range of environments, chiefly in the office environment.

Orcatech Contracts With Market Vision

Orcatech Inc., a manufacturer of computer graphics workstations announced the signing of an estimated $10 million (CDN) agreement with Market Vision of New York, N.Y. for the supply of graphic computers to be used in commodity futures information system. The terminals will form the base for a sophisticated commodity futures information system used by brokers and traders to display time variations and statistical analysis of trading occurring on various U.S. commodity exchanges.

Graphics Merger

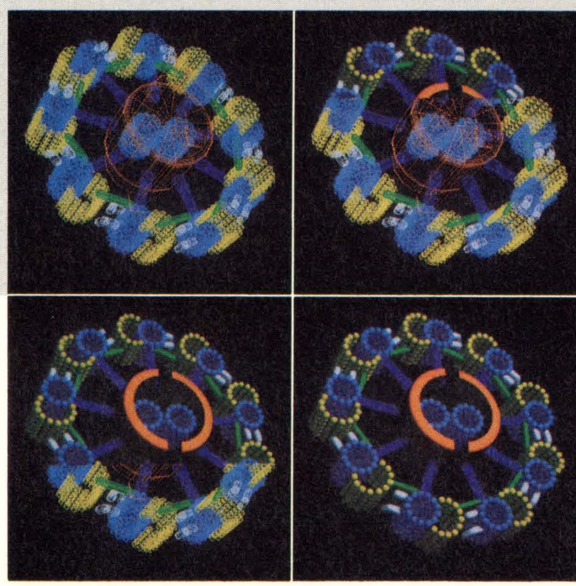
Mentor Graphics Corp. and California Automated Design Inc. (CADI) announced that they have agreed to merge, under which terms, Mentor Graphics and CADI will form a joint company which will be called Mentor-CADI in the United States. Mentor-CADI will offer turnkey, CAE and CAD systems on both engineering workstations and host computers. The move is expected to strengthen Mentor's and CADI's position as developers of computer-aided engineering (CAE) workstations, and CAD systems, respectively.

p-Systems Licences

SofTech Microsystems recently signed over $1 million in new licenses with five major microcomputer manufacturers, including Epson, NCR, Olivetti, Wang and Zenith. The contracts award the manufacturers the right to distribute the p-System, a microcomputer operating system. The interactive p-System will be an important systems software component for each of these manufacturers: Epson America, Inc. licensed the p-System for their QX-10 personal computer; NCR Corp. will offer the p-System as well as compilers for UCSD Pascal, FORTRAN-77 and BASIC; Olivetti plans to market the p-System, as well as UCSD Pascal and FORTRAN-77, on their new M20 business microcomputer in both the domestic and the European markets; Wang will offer the p-System on its 8086-based Professional Computer; and Zenith will also distribute the p-System for its 8086/8088-based Z100 with hard disk support.

Image manipulations in seconds, not hours.

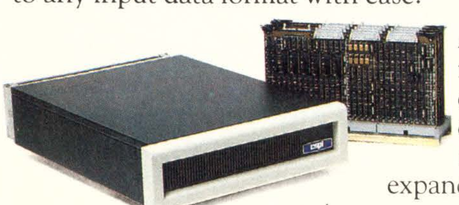
With Mini-MAP™... The Array Processor For The Graphics OEM



Courtesy of Al Barr, Raster Technologies, Inc.

For tough image processing problems like pixel rotation, picture regeneration, or hidden line removal from wire frame models, Mini-MAP gets results in seconds, not hours. Attach a Mini-MAP, model MM-111, to a PDP-11 UNIBUS and you have an interactive number cruncher that is ideal for image processing, CAD/CAM, solid modeling, simulation, and animation.

Shared memory simplifies programming and provides the unprecedented throughput necessary for truly interactive image processing of complex algorithms. 32-bit floating point arithmetic, along with 7 MFLOPS of number crunching power, adapts to any input data format with ease.



A scientific subroutine library of FORTRAN callable routines including an expanding selection of image processing algorithms is available for Mini-MAP. For optimum performance, high-level FORTRAN control languages are provided for both the host and Mini-MAP.

Memory is expandable up to 16 MBytes. Configurations include a four-board set with DEC-type backplane or fully packaged systems.

System integrators are finding Mini-MAP is the most cost-effective number crunching solution for image manipulation. Write for information or call toll-free 1 800 325-3110 for applications assistance.

- 32-bit floating point precision
- Shared memory UNIBUS interface
- 150 FORTRAN callable arithmetic routines
- Up to 16 MBytes of memory
- 1024 x 1024 2-D real FFT in 8.8 seconds
- 1280 x 1024 4-color image rotation (Raster Scan Storage Format) in 27.5 seconds.

CSPI

THE ARRAY PROCESSORS

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Write 49 on Reader Inquiry Card

by Anne A. Armstrong

Selling computers and data processing equipment to the federal government will be faster and less complicated this fall thanks to a new ruling from the General Services Administration which raises the amount agencies can spend without prior GSA approval. Previous regulations were designed for large centralized equipment systems; procedures were complex and ill-suited for dealing with the surge of agency requests for smaller end-user systems.

Under the new system the threshold for blanket GSA delegation of procurement authority has been raised significantly across the board (**Figure 1**). Another change is the way the cost of different systems is measured—under \$25,000, a decision can be based on the lowest offered price rather than on the life-cycle cost.

Item	Old Spending Threshold	New Spending Threshold
ADP equipment		
purchase, competitive	\$500,000	2,500,000
annual rental, competitive	150,000	1,000,000
purchase, sole source	50,000	250,000
annual rental, sole source	18,000	100,000
Software		
competitive	\$100,000	1,000,000
sole source	50,000	100,000
Maintenance		
competitive	\$200,000	1,000,000
sole source	50,000	100,000
Commercial ADP services		
competitive	\$300,000	2,000,000
sole source	50,000	200,000

Figure 1: GSA Procurement Spending

For observers who follow GSA, the most dramatic change in the new regulation is the shift from precontract to postcontract review. "Agencies will be held responsible for their purchases, but they do not need prior approval to spend money," said Robert Dornan, program director of International Data Corporation's procurement information management service. "It represents a change in management philosophy to give agencies more autonomy."

Within GSA, officials acknowledge that the change was prompted not only by philosophy, but also by GSA's diminishing staff. "We decided our limited resources could be better spent on the larger contracts," said one GSA executive.

To check up on the use of this higher blanket authority, GSA plans to send special teams around to the agencies to conduct reviews similar to those of Inspector Generals' offices or the General Accounting Office. Agencies that do not use their new power well will find their purchasing authority reduced.

Telecommunications Tangle

It's a sign of the times that press kits handed out to reporters at the Federal Computer Conference by AT&T contained business cards with the name American Bell scratched out and AT&T Information Systems scribbled in. The loss of the Bell name for its unregulated subsidiary was the latest modification made by Judge Harold H. Greene to the divestiture agreement under which AT&T will spin off its local companies and set up an independent subsidiary to market information systems.

The divestiture and the issues it raises are driving most telecommunications activity in Washington currently. The loss of the Bell name was only one skirmish. Although AT&T chairman Charles Brown said his company was sorry to lose the name and bell logo, he said they had decided not to fight the decision because "we do not want to continue with the uncertainty that has dogged us over the last decade."

For everyone else in the world of telecommunications, the big issue is access charges—how much should inter-city carriers be charged for hooking up to the local phone system and should business users carry the burden for residential users. The Federal Communications Commission has stepped into the middle of this battle. Judge Greene blasted the commission verbally and Congress responded with no less than 15 bills aimed at guaranteeing universal phone service and reducing the financial burden on individuals.

What concerns most businesses more than the FCC ruling is the threat of some new legislation that will completely change the rules. Most telecommunications providers and users would rather live with the current situation than deal with the uncertainty of Congress making some sweeping change at the last minute.

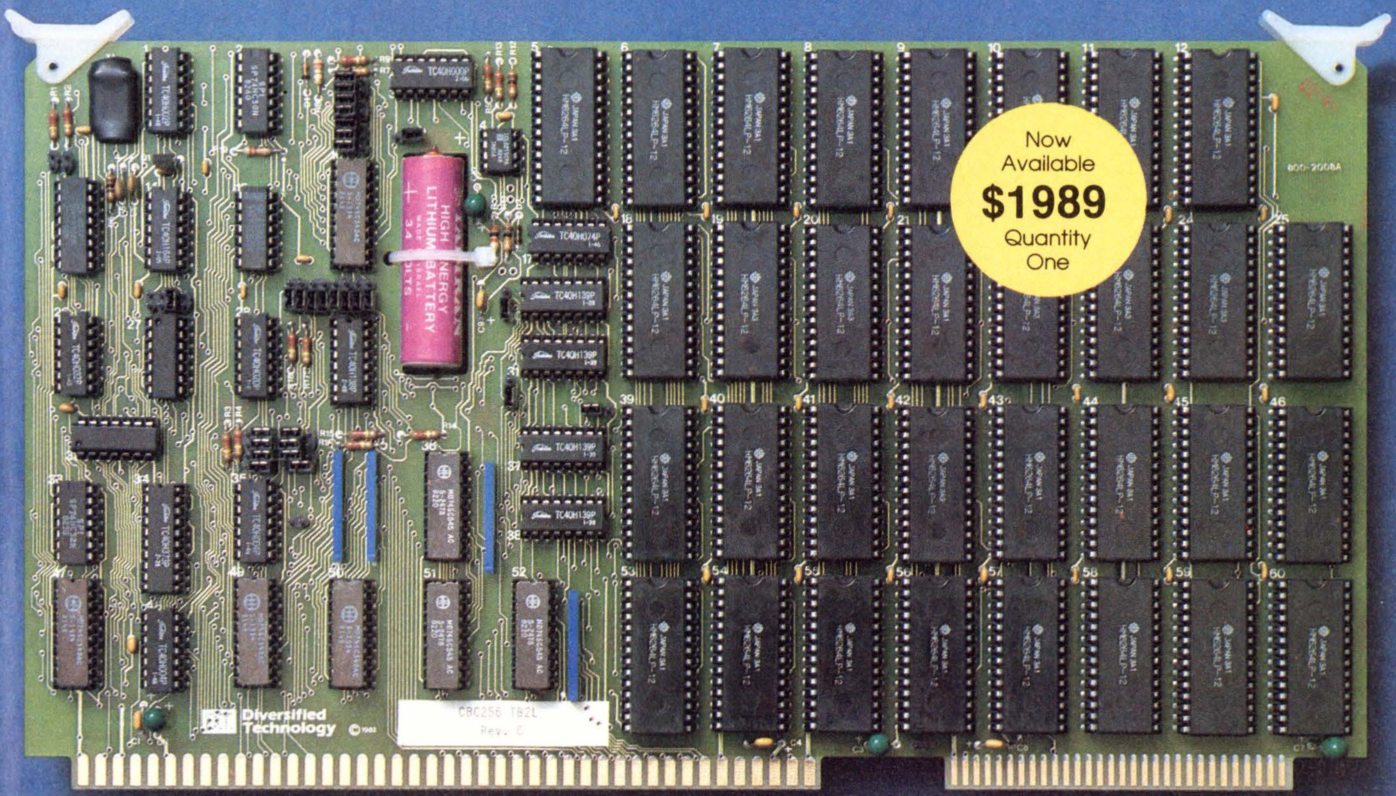
Lobbying to table any new legislation is intense. The American Council for Competitive Telecommunications (ACCT) has urged Congress to "slow down the steam roller and get the facts before acting." ACCT charges that the new bills would hobble the telecommunications industry, penalize efficient companies, reward inefficient companies, raise all telecommunications costs, and give too much power to state regulators.

The Computer and Business Equipment Manufacturers Association (CBEMA) has also entered the fray with a new analysis report of the entire issue, "Perspective on Universal Service Legislation." CBEMA opposes the idea of subsidies to large groups of individuals contained in most of the new bills. "They (the new bills) could stifle competition and technological advances in telecommunications," says Vico Henriques, CBEMA president.

Meanwhile, on Capitol Hill, an early fall markup was expected by the Senate Commerce Committee on bills guaranteeing universal service and low costs, including Sen. Robert Packwood's bill S. 1160, and H.R. 3621, introduced by Reps. John Dingell and Timothy Wirth. How far the bills get after that will depend on the pressure applied to Congress by the various interest groups. If the members do not sense a large constituent reaction to higher phone costs, they are likely to let the legislation flounder. The pressure applied by an almost united business community demanding a halt to the rule-changing will be hard to resist.

256K CMOS RAM

Better Performance than Bubble - at a Comparable Price



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Operating Currents	3.0A, 1.4A (max.)	100mA (max.)
Cycle Time	48 milliseconds avg.	500 nanoseconds typ.
Card Slots Required	2	1
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New Directions for Engineering Workstations Indicated in Announcements From Calma, Lundy, and Megatek

Figure 1: The Sticks Package on the new Apollo.

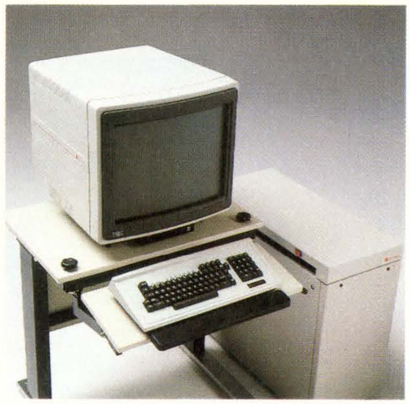

Figure 2: Megatek's 8086-based terminal.

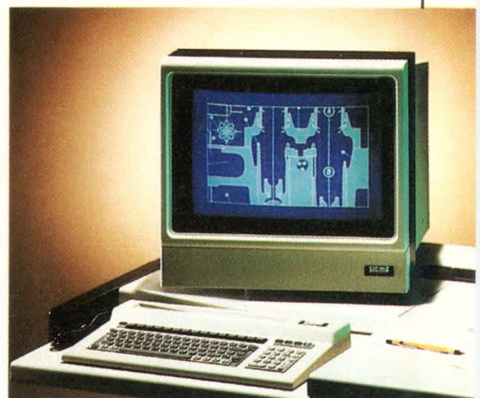

Figure 3: Sigma's workstation.

Calma has joined companies such as Auto-Trol, ICM, and Computervision in basing their CAD products on a second party processor, which in this case is the color workstation from Apollo.

The company will support Sticks software, its Design, Drafting, and Manufacturing package (DDM), for symbolic IC design, and the CHIPS software for IC design on the system. In addition the companies other product lines for applications such as Architectural Engineering and Dimension III Construction will be available on the system.

The shift may represent a trend of designing hardware among developers of software for CAD systems. The announcement is significant because Calma, as one of the largest firms in CAD, will influence the work of smaller systems integrators. One cause of the shift is the increasing sophistication of graphics components available from smaller manufacturers, and the increasing cost of developing graphics software for specific applications.

Calma has also introduced third party software, the rights to which were purchased fom the Communications Satellite Corporation. The package called TEGAS, designed to run on a larger configuration of the company's offerings in minicomputer environments, indicates that even software is being sought by the larger vendors in their efforts to retain market share. (**Figure 1** shows the Sticks Package on the new Apollo workstation.)

The new 6100 workstation series from Lundy is indicative of two trends among graphics systems manufacturers: ergonomic design considerations and the implementation of graphics standard operating software for systems. Lundy is said to be the first to provide full GKS functionality on a monochrome and color graphics terminal. Others such as Spectragraphics and Megatek have implemented partial functions for GKS on their terminals, but Sigma, the licenser of the workstation's design has had special access to GKS expertise through Ray Spiers, one of the formulating committee members for GKS. (**Figure 3** shows the Sigma workstation.) The company notes that graphics standards are going to be required if users and purchasers of systems are going to be able to maintain their software equity while acquiring new systems as they become available.

One shortage of the GKS is that it does not address some of the issues raised by the new work in solid modeling including color shaded surfaces. William Stout, the company's President, expects that these issues will be addressed when software has matured to the point where there are large groups of users. The high resolution (1536 and 1024) terminal provides for both Tektronix 4014 and DEC VT-100 emulation. The work station incorporates other features such as display manipulation and work surface manipulation that are embodied in new ergonomic standards.

The final trend in this triumvirate of releases is from Megatek (San Diego, CA) which has just announced the lowest price of its high performance terminal line (**Figure 2**). Based upon an 8086 16-bit processor, the terminal is hardware and software compatible with the company's other products while allowing the user a much lower cost alternative for access to the company's strength in functions such as 2D rotations, translations, and scaling. The processor retains the 32-bit Megatek graphics engine of the more powerful systems, incorporating the display list and making real time dynamics possible. The product is said to be the precurser of an entirely new product line that will offer similar functions in 3D, and likewise, offer lower cost than is possible to date. *—Borrell*

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In The Government Marketplace

Several new products geared for the government market were recently introduced at the Federal Computer Conference in Washington, D.C. Capitalizing on the interest in DOD's new standard language, Gould Electronics has demonstrated its ADA Learning Environment, a system of hardware and software packages which teach a programmer how to use ADA.

Since DOD requires ADA as the programming language on all future projects, Gould believes a large potential market is available to train the people who will use the new systems.

The Gould ADA Learning Environment is available in three basic packages, each with a different CONCEPT/32 computer. Also included in each package is the Gould UTX operating system, ICSC-ADA Translator, on-site training, installation and all necessary documentation. A rental program is also available.

The model 1815-3 ALE Package is an entry level offering which includes a Gould CONCEPT 32/27 computer with 2 Mbytes of main memory and eight alphanumeric CRT terminals. The purchase price is $129,000. The top of the line package sells for $366,000. Gould is offering just the ADA Translator Software for $30,000 to customers who already have the basic hardware.

Hewlett-Packard added two new laser printers to its product line. The HP Series 1200 Models 2687A and 2688A are desktop printers with 300 dots-per-inch resolution and a 12-page per minute output. The text only model sells for $12,800 and the graphics model goes for just under $30,000. HP stresses that the graphics model can print forms and the data which goes on them at the same time, eliminating the need for most preprinted forms.

Teleram Communications Corporation, whose products are used by several government agencies, has introduced a portable disk drive to expand the memory of its 9-pound notebook computer. The T-3620 is a 5¼″ dual-density, double-sided, portable floppy disk drive. It has a formatted capacity of 320 KB and is used to load and unload programs and data from the computer's built-in bubble memory.

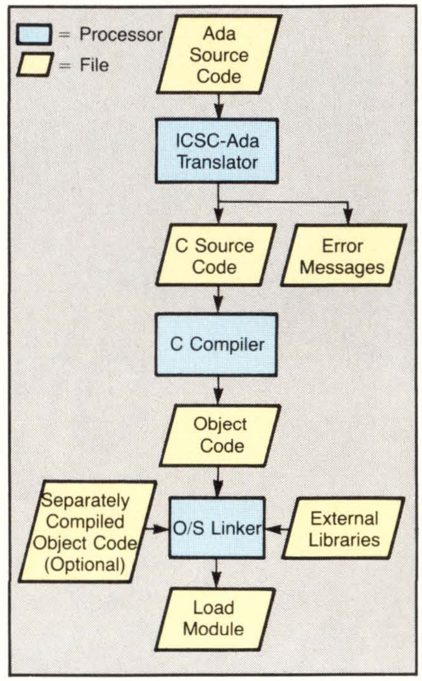

Figure 1: ICSC-ADA enables users of Gould CONCEPT/32 computers to learn ADA and develop ADA programs to satisfy emerging requirements of military and scientific computer applications.

—*Armstrong*

The Changing Custom Chip Factory

Full-custom chip designs are manufactured in exactly the same way as is any standard product, and therefore is causing little change in factory methods or tools. It is the semi-custom chip, however, which promises to change the way factories are run.

In both the gate array and the standard cell approach to semi-custom chip manufacturing, the individual devices and circuit cells are predesigned; and with gate arrays they are also prefabricated. According to VLSI Research, Inc. (San Jose, CA) the standard cell approach is expected to become the manufacturing method adapted by most merchant firms, while the gate array approach is expected to find greatest application among captive manufacturers. This is because standard cell methods are more suitable to factories in which all activities are performed in one central location, while gate array methods are more suitable for decentralized operations. Consequently, the captive gate array factory is expected to act as the forerunner of future custom chip factories.

A future factory designed for producing gate arrays can be expected to depart radically from one designed for producing standard chips. VLSI Research cites the difference as the gate array factory is underutilized and consequently, equipment intensive. Another difference is that it is optimized for quick turnaround from design through the finished product, thus tieing circuit design to final test. A third difference is that it is application specific, and more closely related to system manufacturing than to semiconductor manufacturing.

As the gate array factory evolves, wafer processing will split into two segments. One segment, to become known as pre-metalization processing, will develop into the foundry. It will chunk out standard wafers with predefined cells whose designs seldom, if ever, change. The other segment, known as post-metalization processing, will be the circuit patterning processes which determine the characteristics of each final product. These activities include metal deposition, metal etch, CAD, automatic testing and assembly.


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Roam, Zoom, World Window Functions Offer Design Flexibility

A nationwide emphasis on high productivity in both R&D and manufacturing supports expectations of a 60% market growth for lower cost CAD/CAM systems. Smaller companies, when exposed to the productivity gains of CAD/CAM, are expected to seek fully integrated automation of their design and manufacturing process.

Telesis Corp. (Chelmsford, MA), a manufacturer of turnkey systems for electronic CAD/CAM applications, is designing systems for companies that were previously unable to take advantage of full CAD/CAM capability, because of price or training time limitations. A Telesis system starts at under $70,000, substantially reducing the investment required for full function CAD/CAM. Traditionally lengthy and complex operator training time is reduced through the Telesis proprietary "Function Screen(TM)" which replaced the usual array of input/output devices, computer languages, and codes with simple English commands. A graphics processor and placement and routing capability were recently added to the low-end system.

The Telesis Graphics Processor utilizes three microprocessors and dual-ported memory architecture, offering advanced functions such as *Roam, Zoom, World Window,* and user-definable color priority. The processor integrates with current first generation Telesis systems.

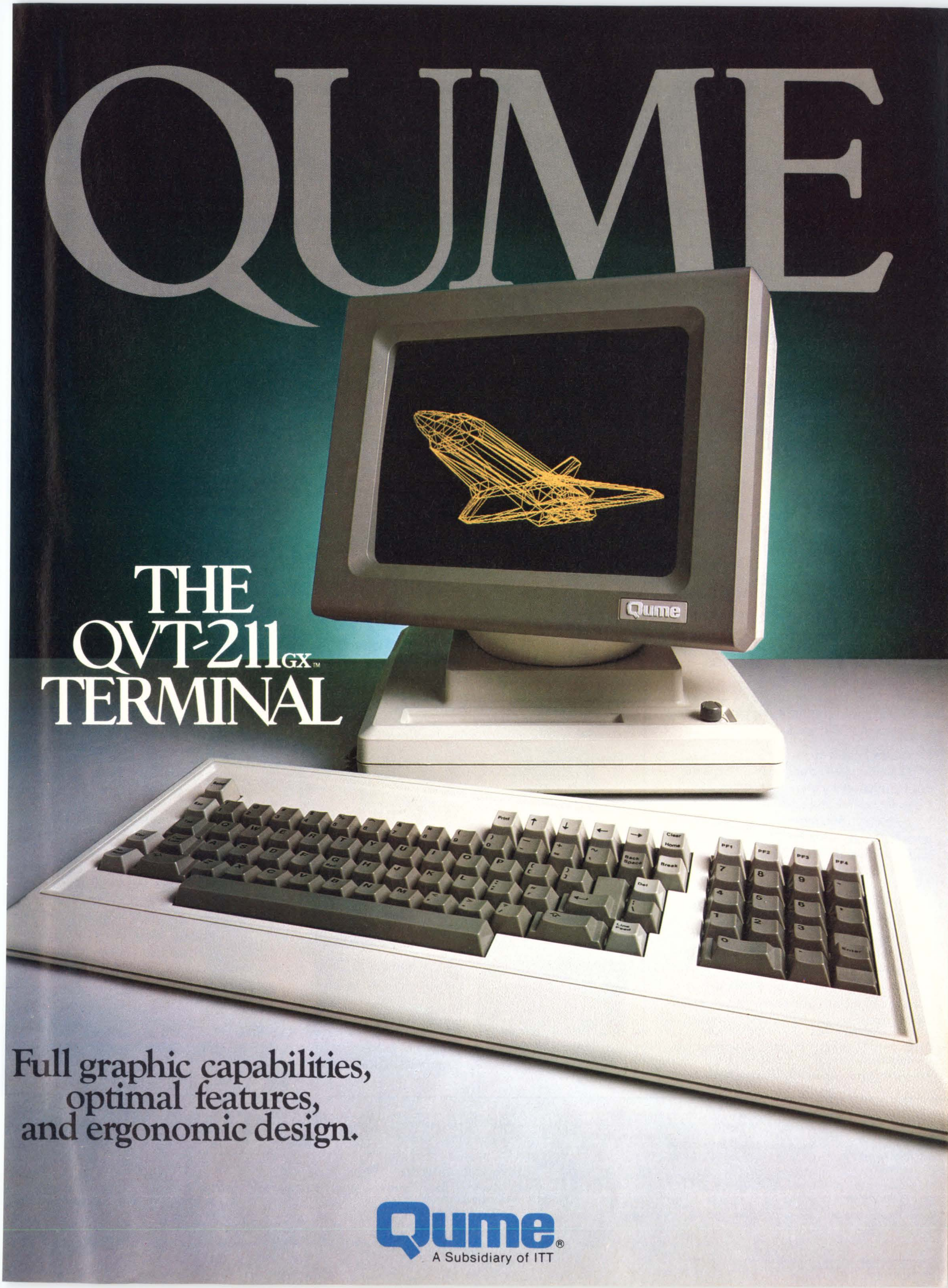
The Graphics Processor has the ability to store a picture with a resolution of up to 2,000 × 1,000 pixels. The system can display a printed circuit board with a defined "tight" grid of 15 mil and 30" on one side without having to repaint the picture. Through the use of the Roam controls, the designer can roam over the entire picture.

Roam. The Roam feature is controlled through the Telesis proprietary, patent-pending, "Function Screen," which replaces the conventional array of input/output devices, computer languages and menu codes with a single, user-friendly device. The Function Screen utilizes a method whereby simple English commands and messages interactively pace the operator through the design steps. The Graphics Processor provides two operator-optimized methods of allowing the user to scan through the stored picture, and adds new dimensions to the capability of the Function Screen. In the "joystick" mode, the Function Screen takes on the characteristics of a velocity joystick, where displacement from the initial point increases the velocity of picture movement, enabling the user to rapidly roam from one end of the picture to the other by simply moving the light pen across the Function Screen.

In the "natural" Roam mode, the designer works in a normal manner on that portion of the picture currently appearing on the display screen. When the user moves the cursor to the outer limits of the displayed portion, the system automatically detects these limits and, after a short pause, begins to move the picture in the appropriate direction.

Zoom. The Zoom control enables the designer to increase the size of the existing picture in steps of 1, 2, or 4X magnification. This gives the designer the ability to focus in on a particular section of the board design for detailed editing. All system editing commands are fully operational in the Zoom mode. Since the Telesis database ensures that all features and functions are re-entrant, when changes are made to the design in the Zoom mode, all other parts of the design are automatically and accurately updated.

Figure 1: The Telesis Function Screen.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The QVT 211 GX features a 14-inch green display as standard (amber optional). The completely independent graphics memory can be displayed simultaneously with the alphanumeric memory.

The QVT 211 GX is compatible with the Tektronix™ 4010* and 4014* command sets, which makes it ideal as a preview terminal for CAD/CAM and Tektronix PLOT - 10 applications. Also, in its native graphics mode, microprocessor-based vector generation greatly simplifies programming. Specify the endpoints and the QVT 211 GX creates the line! Arcs, circles, boxes, and fill can be quickly generated with single commands. These powerful features bring a full spectrum of business graphics within the reach of micro and mini-computer users. Image size and location, as well as additional features — such as variable display windows, relocatable origin and area fill — are easily programmed by the user.

In the Qume tradition, the QVT 211 GX delivers a powerful array of graphics capabilities, at a cost well within reach.

Graphics Features

• Full, interactive vector graphics • Separate display memory for graphics • Switchable video • Absolute and relative addressing • Variable gain and relocatable origin • Draws lines, boxes, and arcs (including circles) • Area fill • Selectable power-up option • Graphics memory dump to host • Cross hair cursor • **Native Command Mode** • Large addressable area (65Kx65K) • Addressable screen area 2500x2000 • Vector generated line, box, arc and circle • Area fill • Relocatable origin • Variable gain • **Tektronix Emulation Mode** • 4010 and 4014 software compatibility — PLOT - 10 • Addressable plot area 4096x4096 • Vector variation (dot, dash, and lines) • Incremental plot • Write through plot • Resolution 644x288.

*Tektronixs 4010 and 4014 are registered trademarks of Tektronixs Inc.

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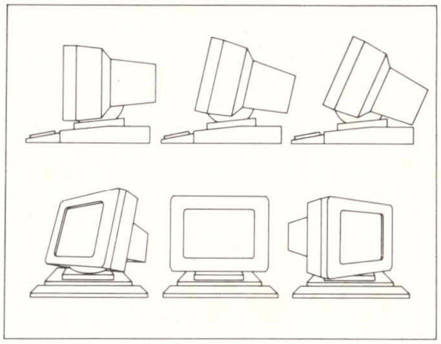


Alphanumeric Features

Display Format
24 lines x 80 characters
25th status/set-up line

Character Formation
7 x 9 matrix in a 9 x 12 cell

Displayed Character Set
96 ASCII characters, 15 line-drawing symbols, and 32 control character symbols

Editing
Cursor: up, down, left, right, and home. Character/line insert and delete, erase to end of line/field/page, tab, back tab, field tab, field back tab.

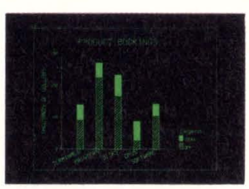
Communications Interface
EIA RS232-C with optional 20 mA current loop

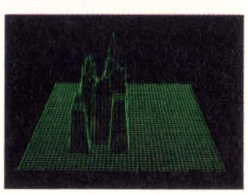
Communication Protocols
DTR and/or X-ON/X-OFF

Communication Modes
Full or half duplex, block/line, block/page; 7 or 8 data bits

Baud Rates
16 selections from 50 to 19.2K

Auxiliary Port
Bidirectional EIA RS232-C, partial/full screen copy, transparent print.





Screen
Tilt/swivel 14-inch diagonal standard non-glare green (optional non-glare amber)

Character Attributes
Blink, blank, normal video, reverse video, underline, half intensity

Keyboard
Detached, adjustable-tilt, low-profile (home row 30mm from work surface), alphanumeric keys, 14-key numeric pad, 12 function keys (8 user programmable), defeatable autorepeat and key click. Print, setup, and no-scroll keys.

Fields
Protected and unprotected fields

Parity
Odd, even, mark, space

Screen-saver
Screen shut off after 15 minutes of inactivity with no data loss

Emulations
Hazeltine 1500, Lear Siegler ADM-3A/5, Televideo 910

Set-Up Mode
Menu style, preserved in non-volatile memory

Power Requirements
95-125 VAC
200-264 VAC
50/60 Hz, 40 W

Dimensions
Keyboard 1.5″(H) X 18″(W) X 8″(D)
Display 14″(H) X 13″(W) X 12″(D)

Weight
Display 20 lbs, keyboard 3 lbs

Options
Amber phosphor screen
Foreign character sets
20 mA current loop (passive or active)

Character Sets
USASCII and APL

Software

A library of PLOT - 10 compatible subroutines which speeds the development of graphics applications programs is available from Tektronix Corporation. The library is available under RT-11, RSK-11M, and VMS. The subroutines are written in FORTRAN, but any higher level language which supports a FORTRAN-style call can be linked to the package. Business graphics package for personal computers is available from Digital Research.*

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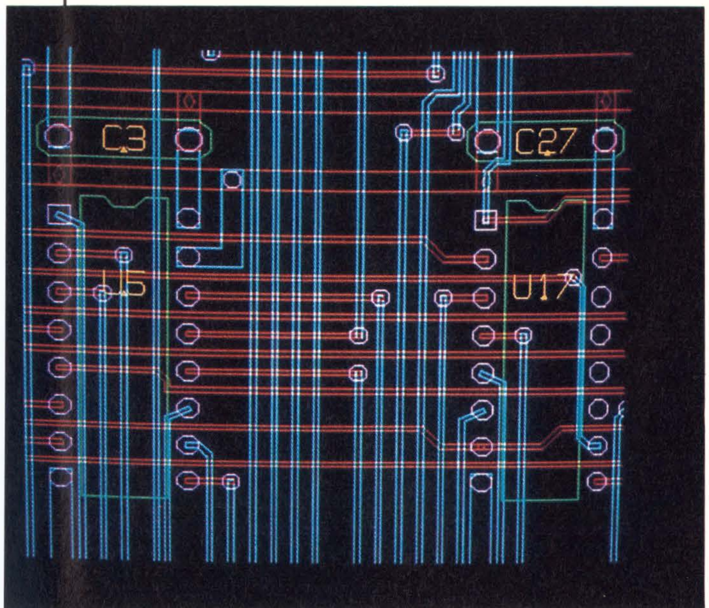


Figure 2: A Zoom closeup of a completed routing scheme.

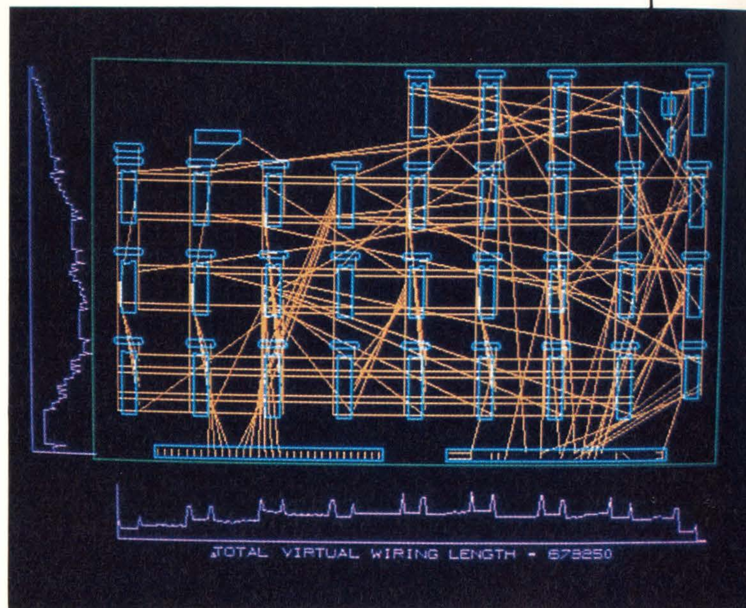


Figure 3: Ratnested Placement.

World Window. With the Graphics Processor, the designer has the freedom to switch from a view of the entire schematic or board design being developed (the world) to that portion which is stored in the picture space (the window). The system performs this switch in less than 0.5 sec., and maintains synchronization between both representations. The designer has complete control over the relationship of the window to the world, and can increase or decrease the window area at will. When in the world mode, the system dynamically highlights the window portion for visual verification of its relationship to the entire design.

A unique feature of the Graphics Processor is its ability to allow the designer to assign a color to a designated class of functions, such as a particular layer. The system then commits the color to that layer (or other function) independently of its overlap with other colors or layers, for superior visualization. The designer may establish which color is on "top" in order to view the representation from one direction or another.

The graphics processor is implemented using a pipeline architecture, incorporating the following microprocessors: the 8 MHz Motorola 68000, the Intel 8085, and the NEC 7220 graphics processor. By utilizing dual-ported memory architecture and an optimized cross-compiler, graphics software originally written for the first generation Telesis graphics processor can be downloaded to the 68000 microprocessor and executed at speeds of up to five times faster than before. The data stored in pages on the Winchester disk can then act on this data and pass the results to the 7220 processor. The architectural structure of the graphics processor currently provides 512 Kbyte of dedicated memory, and it is expected that this will be significantly expanded in the future.

Routing And Placement Software

With interactive re-entrant routing, a designer can interrupt automatic routing at any point, manually delete, add or change any connections which appear on the screen, using standard editing commands and then re-start the process in the same or another algorithm of his choice. The system utilizes three customized routing algorithms, and provides a high degree of user-defined control. Capabilities include routing an entire board, routing a window or a net, and addition of single layers to a previously routed board.

The placement process automatically selects locations for components and places the required components on the board drawing. The placement routing is optimized to fully exploit the features of the router and thereby maximize the number of successful automatic connections on the board, while minimizing the number of unwanted vias (feed-thru holes). The placement process employs a concurrent algorithm which simultaneously considers a set of components, as opposed to most other placement systems which can only consider one component at a time. Subsequent to automatic or manual positioning of a component, the designer may "lock-in" any placed component to its assigned location. Once locked, a component is not subject to modification by placement routines, thus providing the user with a convenient and effective means of controlling the location of position-sensitive critical components. If design considerations dictate, the designer may "unlock" any component previously designated as "locked." **Write 231**

Performance-Oriented Architecture Strengthens Graphics Capabilities

Figure 1: The MASSCOMP workstation with Floating Point/Array Processor.

In today's workstation market, participants range from mainframe vendors to micro computer suppliers. For OEMs to decide on what and how to buy technology, they must clearly identify their unique contribution in respect to the industry's driving forces. These forces could be characterized as computational performance, communications capability, graphics requirements, and applications software.

Because graphics requirements are both applications and technology driven, no one vendor can yet support varied requirements in resolution, speed, refresh rate and special enhancements. The system architecture should permit the addition (or subtraction) of graphics processors or monitors depending on OEM needs. The computational power of workstations rides the fastest moving part of the technology curve, therefore performance oriented architecture is required. The architecture must encompass and accomodate μP independence, CPUs with cache, Floating Point processors, array processors and high performance peripherals.

MASSCOMP (Littleton, MA) recently introduced a 32-bit virtual memory workstation with an integrated floating point and array processor. By combining enhanced processing power with a performance-oriented architecture, MASSCOMP has strengthened the workstation's computation and graphics capability for real-time numerical analysis in CAD, CAE, and other scientific and engineering applications.

The MASSCOMP Workstation 500 supports two 19″ raster displays—either 1024 × 800 resolution monochrome, or an 832 × 600 resolution color unit, each with a dedicated graphics processor. Workstation 500 executes a multiuser/multitasking, virtual memory UNIX operating system, featuring RTU, MASSCOMP's software enhancements for real-time operation. The system design features a 8 MB/sec memory interconnect bus, closely coupling dual 32-bit 10 MHz VLSI processors (MC68010 and MC68000) with a 4 Kbyte cache; a 1024-element translation buffer; and a 1024-entry I/O map, with up to 6 Mbytes virtual address space.

Within this system CPU, an integrated, independent floating point processor, or combined floating/array processor can be added. The independent floating point processor performs a single-precision (32-bit) add or multiply in 1.6 microseconds. The floating point processor also provides double-precision (64-bit) IEEE standard arithmetic. The FP-501 Floating Point Processor (FPP) is closely coupled to the central 32-bit CPU through the high-speed 500-Series Bus. The FP-501 is a pipelined design implemented using high-speed Advanced Schottky logic. In order to provide the maximum level of system performance, the FP-501 is closely coupled to the central VLSI 32-bit processor via the 8 Mbyte/sec 500 Series Bus.

The Floating Point Processor is supported by the C and FORTRAN 77 compilers, and is also supported under the Pascal-2 package which includes a symbolic debugger. The performance of a program which has extensive floating point computation can be expected to increase by an order of magnitude. All computation is carried out to full accuracy specified by the IEEE floating point standards.

The AP-501 Array Processor (APP) was designed to enable 500-Series systems to provide single and double precision, floating point, vector computation. The AP-501 features a pipelined design implemented using high-speed NMOS VLSI logic. Both the Adder and Multiplier are independently pipelined with a staging-time of 200 nsec. The pipeline design allows the initiation of a new arithmetic operation without waiting for the previous one to complete. Maximum arithmetic processing capability is achieved through parallel operation of the Adder and Multiplier. Parallel operation is crucial because many algorithms are expressed predominately by a series of multiply and add operations.

Most array processing functions involve a series of basic operations (add, multiply, etc.) on a given set of data. To reduce the amount of host memory access during a sequence of such operations, the AP contains 16K 32-bit elements of local memory. Therefore, system memory is accessed only during the initial data load, and to retrieve the final results. No program loads are required with the AP-501.

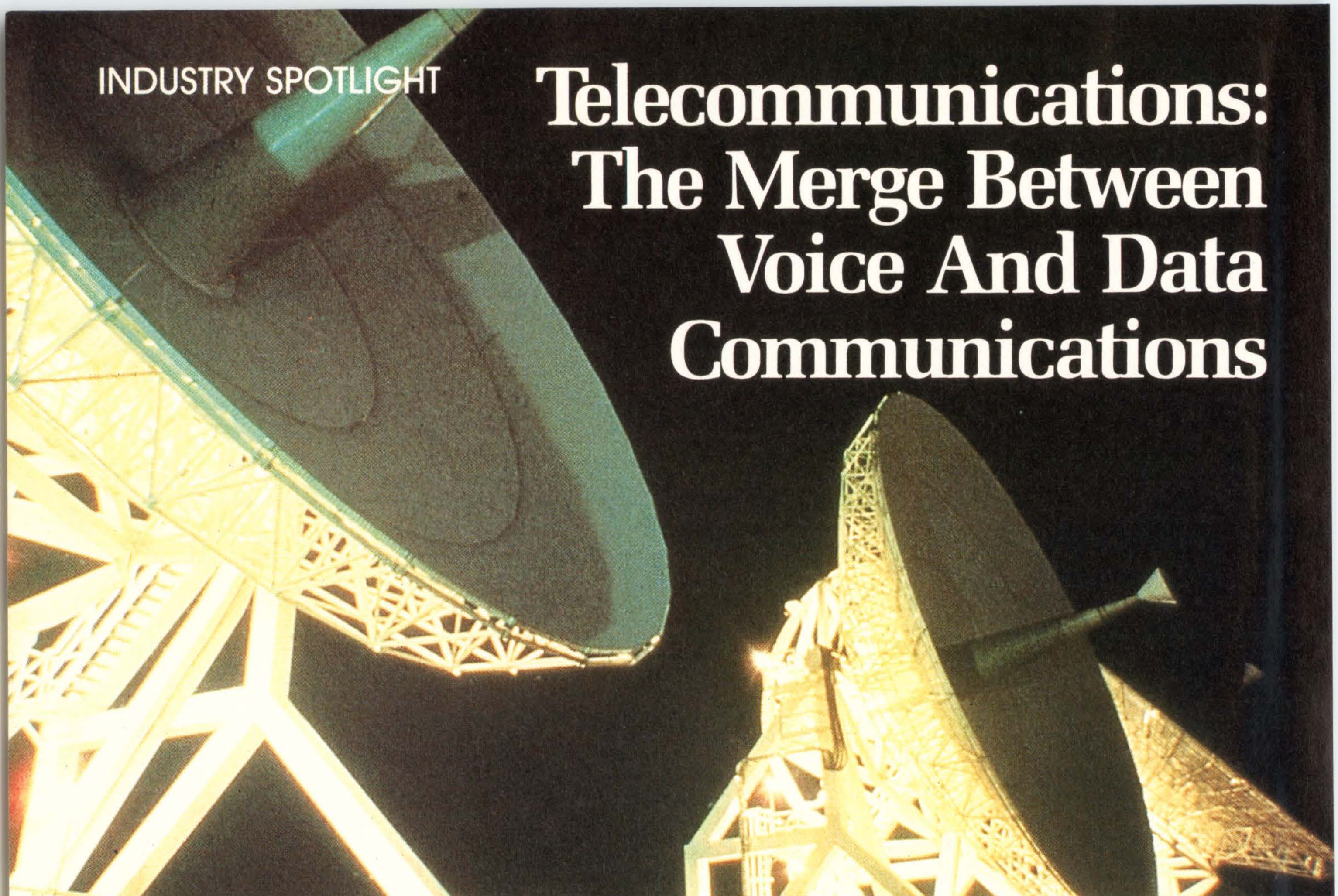
The AP-501 operates in conjunction with the FP-501 Floating Point Processor (which is a prerequisite). The FPP is used as the double precision math engine for the AP. The single precision square-root and divide instructions also utilize the FPP to perform the necessary computation. The AP-501 is contained on a single board which communicates with the FP-501 via an "over-the-top" connection.

Each MASSCOMP Independent Graphics Processor (IGP) contains an 8 MHz MC68000 with its own 128 Kbyte program store. "Because the IGP independently processes its graphic images, it frees the CPU to run applications programs. Thus, the design avoids the overall performance degradation common in systems which use a single processor to both generate graphics and execute applications code," stresses Allan Wallack, MASSCOMP's V.P. Marketing.

To support rapid (dynamic) image transformations and multiplanar displays, each IGP can have up to 1.2 Mbytes of raster memory in dual frame buffers up to 10 planes deep. A MASSCOMP IGP drives a 19" monochrome display with a single memory plane, or a 19" color display with either 6 or 10 memory planes. The IGP display's 60 Hz non-interlaced refresh rate eliminates screen image flicker that causes operator fatigue. Both color and monochrome displays feature a 117-key, low-profile keyboard, plus an optional mouse or data tablet and puck. **Write 232**

INDUSTRY SPOTLIGHT

Telecommunications: The Merge Between Voice And Data Communications



The merger between voice and data communications assures the future of the PABX in the automated office scenario.

Jose Reines started the operations of American Telecom, Inc. in 1976. He is President and CEO, and a member of the Board of Directors. Mr. Reines started his professional career at IBM's T. J. Watson Research Center and, prior to starting ATI, was Director of Development Operations for ITT's Central Office and PABX switching in North America. He is a senior member of IEEE and several engineering honor societies.

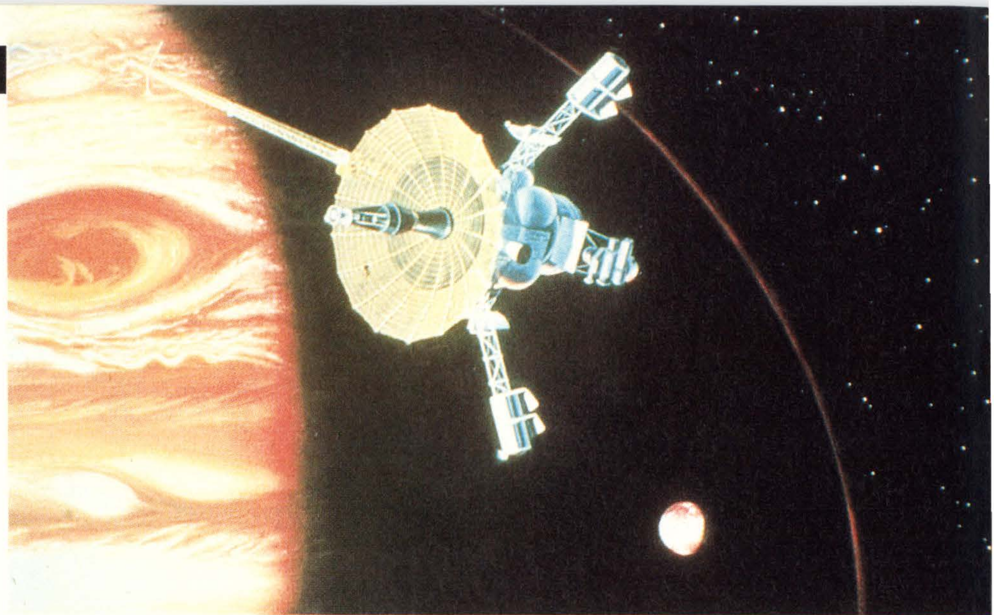
by Jose Reines

When considering the spectrum of the telecommunications industry today, the most significant observation is its present identification as a new and emerging industry of the 80's. In fact, telecommunications is not a "new" industry at all. Leading edge developments in the industry date back more than fifty years ago, with Bell Laboratories' research and developments on semiconductors and the invention of the transistor, paving the way for the computer industry. A popular misconception is that telecommunications is a recent spin-off of the computer industry, when almost the reverse is true.

From its beginning, the telecommunications industry operated under rigid governmental regulatory practices. This caused a lack of entrepreneurial opportunities and investment interest on the part of the business community and, as a result, the industry was slow moving in independent technological research and development. Unlike telecommunications, the computer industry has never operated under regulatory policies, and because of this, has always attracted tremendous interest from major investors and entrepreneurs.

The U.S. government began to deregulate telecommunications in the early 70's. In the short amount of time in which telecommunications has operated under the principles of free enterprise, the industry has surfaced as highly competitive and assumed a primary position in office automation.

When presenting an overview of telecommunications, it is crucial to bear in mind its history, as well as events currently in motion, prior to naming key players and significant technological achievements. A combination of factors including current legislation, past industry policies and present market conditions are critically impacting the direction of research and development. Further, these factors distinguish the position of one manufacturer from another.



Two looks at telecommunications satellites. Photos courtesy Harris Corporation.

Office Automation

Until recently, the idea of the computer maintaining the dominant role in the automated office was another popular assumption, possibly generated by their sheer visibility. However, many manufacturers and consultants are beginning to see an eventual merger of two disciplines: the data processing manager and communications manager.

In the broader sense, the merger between voice and data communications is already complete. Most computers can utilize telephone lines for the transfer of data, and most major PABX (private branch exchange) systems now utilize resident data switching capabilities, for the transmission of data communication. Voice-data switching is a significant technological accomplishment by PABX manufacturers since the ability to transfe data via the PABX allows for a faster and less expensive alternative for data communication. Assuring the future of the PABX in the automated office scenario, voice-data capabilities also presents itself as a gateway for information from a variety of sources, including personal computers, word processing terminals and public information networks.

In addition, the microprocessor, first popularized by the computer industry, is permitting the PABX manufacturer to offer feature-rich systems with the same cost-effective, user-friendly designs that characterized the microcomputer. Manufacturers are capable of addressing the needs of every market: small, medium and large businesses, as well as highly specialized markets such as healthcare and lodging communications systems, with unique requirements due to the nature of their respective business environments. The image of the PABX is undergoing a transformation from that of a large box in the out-of-the-way equipment room routing the usual voice-only calls, to a facet of an automated system that can provide the end-user and management with highly flexible means of cost-displacement and detailed call-accounting information, which serves to justify the expense of automated equipment on a return on investment basis.

The electronic terminal or custom telephone, is the telecommunications industry's response to a shift toward more flexible and interactive terminals in the office place. Microprocessor-controlled electronic terminals often combine traditional voice communication with LCD information displays, multi-line capabilities and single-button access to advanced features.

When supported by a major PABX system, these display terminals may also transfer data, as well as replace traditional handwritten messages on pads with electronic message systems. More sophisticated terminals represent the telecommunications industry's jump on related office automation concepts, such as electronic mail and environmental control/surveillance systems, priming the PABX for the seat of "Office Controller."

Key telephone systems complete the basic product line of most manufacturers. These systems are designed to provide small businesses, requiring under 100 lines of service with the sophistication of a larger, more advanced communications system.

Reselling Telephone Services

As a result of a Federal Communications Commission (FCC) ruling, which took effect December 18, 1980, American Telephone & Telegraph's monopoly on telephone service was overturned, and allowed the reselling of interstate telephone service. The reselling, however, of telephone service began much earlier with companies now very familiar to the general public: Microwave Communications, Inc. (MCI) and Sprint. Entrepreneurs envisioned the alternatives to AT&T by utilizing their own technologies and the ability to interconnect with AT&T. Their idea was to carve a high-growth niche out of the market: reduced long-distance rates.

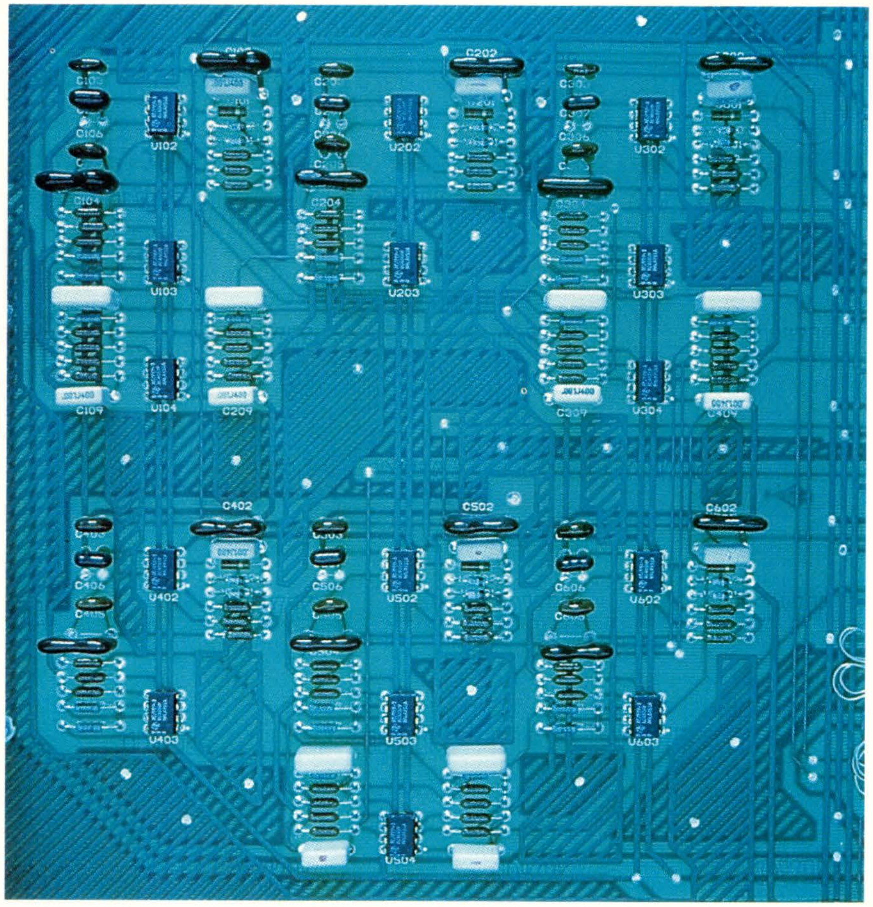
In 1974, MCI filed an antitrust suit against AT&T. The suit alleged that AT&T had illegally impeded MCI's entry into the long distance private line market. MCI sought damages of nearly $900 million. In a trial ending June 1980, the jury found in favor of MCI on 10 of 15 specific complaints and MCI was awarded an unprecedented $1.8 billion judgment—the largest in U.S. history.

The Breakup of AT&T

No other industry event has drawn as much attention as the court-ordered divestiture of American Telephone & Telegraph Co., and for good reason. Not only is it the largest corporate breakup in U.S. history, but the company has provided approximately 75% of the nation's customers for nearly a century with "one-stop" shopping for telephone equipment and services.

The significance of the breakup is multi-faceted. Most importantly, it has divided AT&T into telephone companies that provide telephone services and telecommunications equipment. The "new" AT&T has faced its toughest competition the longest period of time—long distance service and telecommunications equipment markets. According to a recent report from market researchers at the Eastern Management Group, nearly 80% of the $3.1 billion spent this year on PABXs, will go to AT&T competitors. Approximately $3 billion or 8% of the total long distance market will be spent this year on long-distance phone calls made outside the Bell system through such companies as MCI Communications, ITT Longer Distance and GTE Sprint.

American Bell (renamed AT&T Information Systems) enters the equipment market at a time when competition is fierce. Companies such as Northern Telecom and Rolm have long-established positions in the PABX market backed by solid reputations for reliable equipment. Both companies tout the widest range of equipment product lines, promoted by honing teams of sales and marketing professionals already expertly aware of the market.



A circuit board from a PABX.

There are juxtapositional sides on the subject of American Bell, with many analysts predicting the company will have to play a game of "catch-up"; that the traditional marketing strategy of "we're the only logical choice" when the company was primarily in the telephone service market, is no longer a viable plan. The fact is, consumers have never had a greater selection of manufacturers and suppliers to choose from.

The recent introduction of System 85(TM), an advanced digital PABX, was a clear move on the part of Bell to alert customers and competition that the company has no intention of forfeiting its share of the market. System 85 was criticized for being too expensive for the features it offered; customer reaction was modest. American Bell, with the assistance of Western Electric, was quick to respond

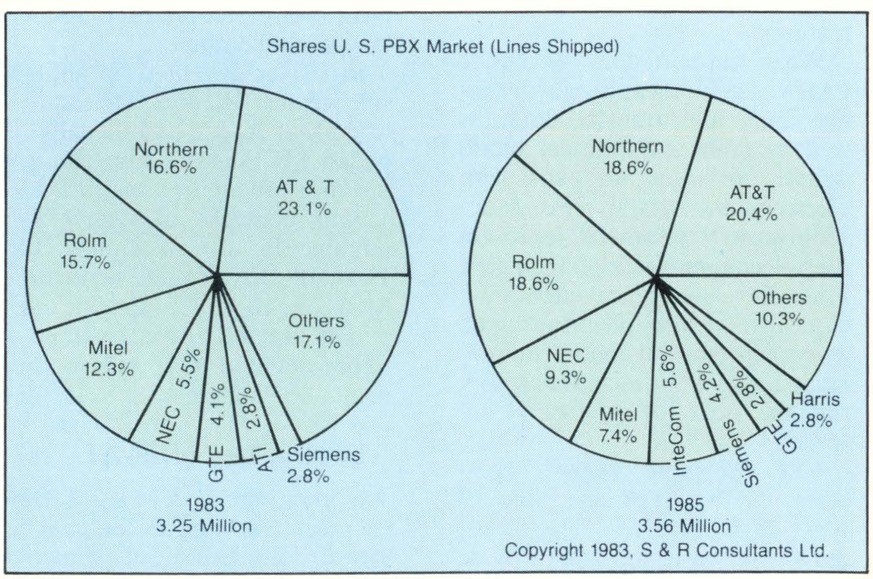
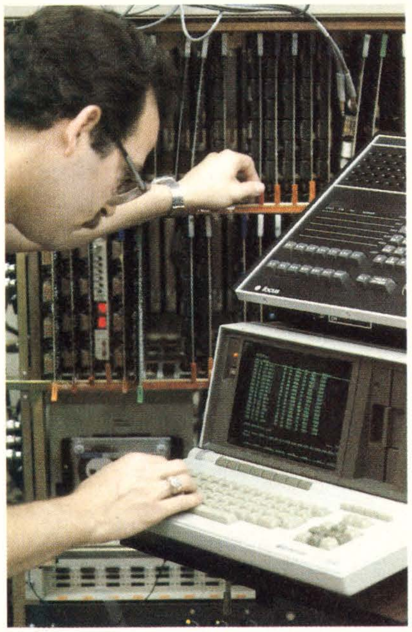


Figure 1: Shares of U.S. PBX Market (Lines Shipped).



Technicians performing system testing on main attendant consoles after pro gramming.

with improvements which the company claims have helped to boost sales and raise Western Electric's 1984 production forecasts.

In other camps, smaller firms such as American Telecom, Mitel, Siemens and Ericsson are betting that enormous size can also be a hindrance, since it is assumed that larger firms are also slow-moving in response to the market and customer needs.

The debate invariably leads to the entire inustry's primary concern: has the long awaited shakeout already come, or is it just beginning? Obviously, there is no definite answer to the question at this point in time. But much of the answer lies in the course of action taken by the Regional Bell Operating Companies (RBOCs), which officially go into operation January 1, 1984.

As a result of the AT&T breakup, the RBOCs will be forced to act as separate companies responsible for individual profitability. In view of their immediate lack of sales and marketing forces, how will they set about to capture a share of the market? Will consumers passively remain with their regional telephone company? Since the court-ordered breakup precludes the RBOCs from making their own product, will the RBOCs look to other manufacturers as their suppliers, and if so, will they continue the policy, or will it be dropped in favor of acquiring their own manufacturing subsidiaries?

As these decisions are made by the RBOCs, the immediate future of the industry will appear less complicated. And at least one of those decisions has already been made, since the RBOCs are actively lining up suppliers. American Telecom recently signed an agreement with PacTel Communications Systems worth $15 million to the company for its office communications equipment aimed at small and medium-sized businesses. (PacTel is the equipment subsidiary of Pacific Telesis, the result of the union between Pacific Telephone and Nevada Bell). For businesses requiring 10,000 to 25,000 lines of capacity PacTel has announced it will sell equipment manufactured by Northern Telecom, Ltd.

The Market

Interest in telecommunications market opportunities, though competitive, is nearly as bullish as the oil industry experienced a decade ago. As a result of continuing deregulation, the breakup of AT&T and growing integration of voice and data communications, the industry is attracting interest from sales and service, suppliers, manufacturers and service carriers.

Central office-based Centrex systems, once the only alternative for large businesses requiring 10,000 to 20,000 lines of communications service, have been losing ground to manufacturers such as Northern Telecom and Harris. For years, telephone companies marketed Centrex service and reliability without the maintenance worries; however, steadily rising Centrex costs and the interest in integrating voice-data communications has caused the corporate buyer to look again at privately owned large business exchanges.

As little as two years ago, the large system market was considered the most volatile. Marking the industry's incredible pace, that opportunity is described by most analysts as "closed" to newcomers. Companies such as Northern Telecom, American Bell and Rolm have introduced very large systems to pull the lion's share away from Centrex.

Marketing savvy and system reliability are key factors in manufacturer's sales. Consumers in the under 1,000 line range are typically purchasing their first major communications system. Primary concerns to management are easy maintenance, system expansion and equipment that provides a return on investment. For example, American Telecom's FOCUS$92/ digital PABX is widely recognized for its reliability and its modular concept for system expansion. Ericsson, Siemens and Mitel have also gained significant influence in this area of the market.

Key telephone systems addressing the needs of the small business environment under 100 lines is not a new market. Yet, advanced technology is being introduced to this market which permits manufacturers to offer the small business market, premature in its need for a PABX, with a microprocessor-controlled key system that offers some of the sophistication of larger systems, automatic route selection (ARS), station message detail recording (SMDR), visual displays and hands-free dialing.

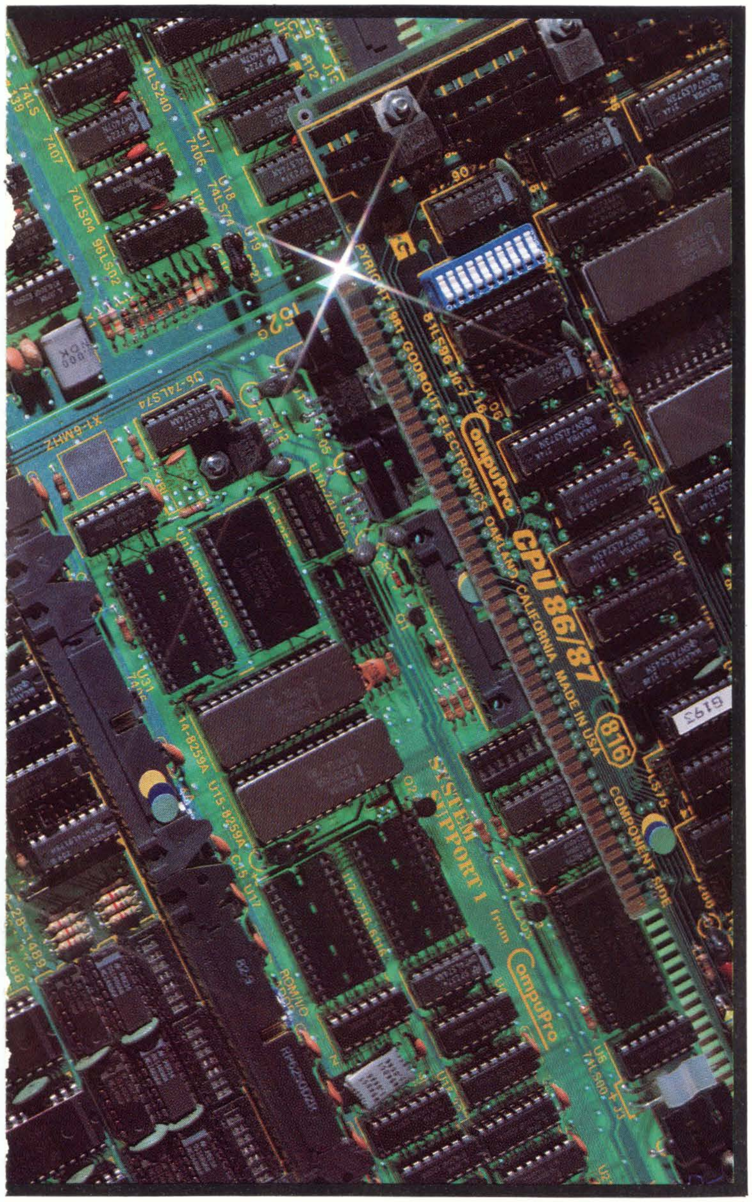
Optimism Is Guarded

Since the early 70's, the PABX market has enjoyed robust sales, however, 1982-1986 annual PABX line sales will reflect the industry's period of transition and analysts are guarded in their predictions.

A key factor in the high sales figures in the early 70's was the "replacement factor". The replacement factor helped to conceal the fact that the true PABX market is much smaller than it was ten years ago. From 217,000 installed systems in 1971, the market tightened to 145,600 "pure" PABXs displacing old switches in 1981.

In actuality, the drop in PABX installations is being compensated by non-PABX devices, such as key telephone systems. This point underscores how important it is for manufacturers to understand the PABX market; to analyze generic product types, since the market is greatly determined by the life expectancies and eventual replacements of these older installations.

According to Eastern Management Group, a Boston-based research firm that tracks the telecommunications industry, as the inventory of older-generation PABXs about to be replaced is exhausted and dwindling numbers of replaceable Centrex systems remain, several markets are beginning to narrow—most significantly, the 100-400 line market or mid-size business system. The research firm predicts a drop by 29% in annual line shipments in this market from year-end 1982 to year-end 1985. Key systems, being a glamor market, is expected to reach a $1.5 billion market by the mid-1990's, with the over-1,000 line market reaching $2.1 billion. While other markets begin to level off by the late 80's, the third gen-



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eration PABX market will surge. Projections for the 1983 PABX market are in the area of $3 billion in sales.

In lines shipped, both AT&T and Northern Telecom have shipped nearly 50% of all PABX lines in 1983, which will total in the area of 3.25 million. Rolm is expected to increase its share of line shipments substantially by 1985, competing on equal turf with Northern Telecom for the more than 3.5 million line market. (**Figure 1**).

Bottom-line indications point to a saturated market and the prognosis for the industry, though healthy in general, is that some casualties will be unavoidable.

Worker assembling minute pieces of PABX (private branch exchange) circuit boards. Circuit boards, the mainstay of the system, can be programmed to handle thousands of calls each hour.

Mergers And Joint Efforts

Indications also suggest that the staying power of telecommunications manufacturers will weigh heavily on the ability to raise necessary capital to conduct new research and development projects. In the last few years, Lexar's acquisition by United Technologies, InteCom's search for financing from sources other than Exxon, and Rolm's sale of 15% of its shares or $228 million to IBM, strongly suggest the expense PABX manufacturers face in order to move away from traditional voice-only systems.

A number of firms already subsidiaries of computer conglomerates, such as American Telecom (majority owned by Fujitsu-Japan with $4.0 billion in sales), may face fewer roadblocks in getting new products to the market. And the trend will undoubtedly continue for joint efforts, such as the one recently announced by Ericsson and Honeywell to develop a research and development firm aimed at supplying Ericsson with data switching capabilities for its newly-introduced MD 10™ digital PABX.

But capital alone will not guarantee success, as recently witnessed by a pull-out by Datapoint and Rockwell International (Wescom) from the PABX market. Many joint efforts result in dragging schedules for promised voice-data capabilities and other product enhancements. Ultimately, it is the combination of operating capital, a quality product and the often overlooked ability to stage a sound marketing plan, supported by a competent sales force that lead to success.

Looking Ahead

Despite areas of confusing and ongoing regulation changes, most insiders agree that with some casualties certain, the industry's period of transition remains a healthy sign. The eminent threat of an industry shake-out is regarded as a positive indication that free enterprise will encourage competition, as well as research and development of new technologies. The most promising technologies already being tested include electronic or teleconferencing, cellular mobile radio, fiber optics and videotex.

Teleconferencing is being carefully scrutinized as an alternative to executive travel. As travel expenses have continued to escalate, the costs of video teleconferencing have comparably lowered. Particularly of interest to large multi-site establishments, teleconferencing is a growing portion of the industry. While competition continues to heat up between camera, projectors and coder/decoder manufacturers, improvements in electronic component technology are paving the way for more versatile applications. According to Quantum Science Corporation, a New York-based research group, by the end of 1982, an estimated 30 full-motion compressed-video teleconferencing rooms were in operation. The number is expected to triple in 1983 and reach 300 by 1985.

Of all the new technologies, cellular mobile radio is causing the greatest stir. Its attraction is convenience that leads to increased productivity, and it is seen as the step before a watch-size portable telephone. With cellular mobile radio, the business executive and general consumer are assured of two-way voice communication almost anywhere in the nation without distortion, fading or typical problems associated with mobile communications of the past. According to Kuhn Loeb Research Industry, potential markets include public safety and health workers, utility firms, press and business executives, handicapped drivers, as well as the general public. Future annual sales figures have been projected at $7 billion by 1987. □

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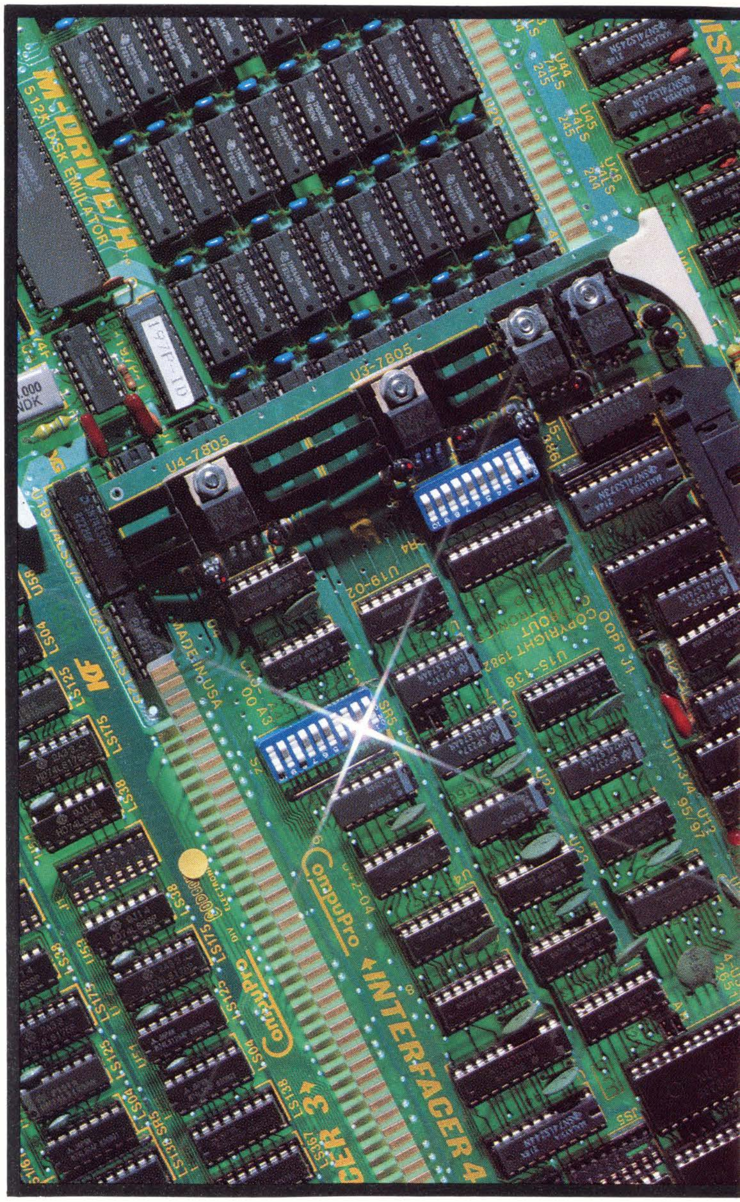

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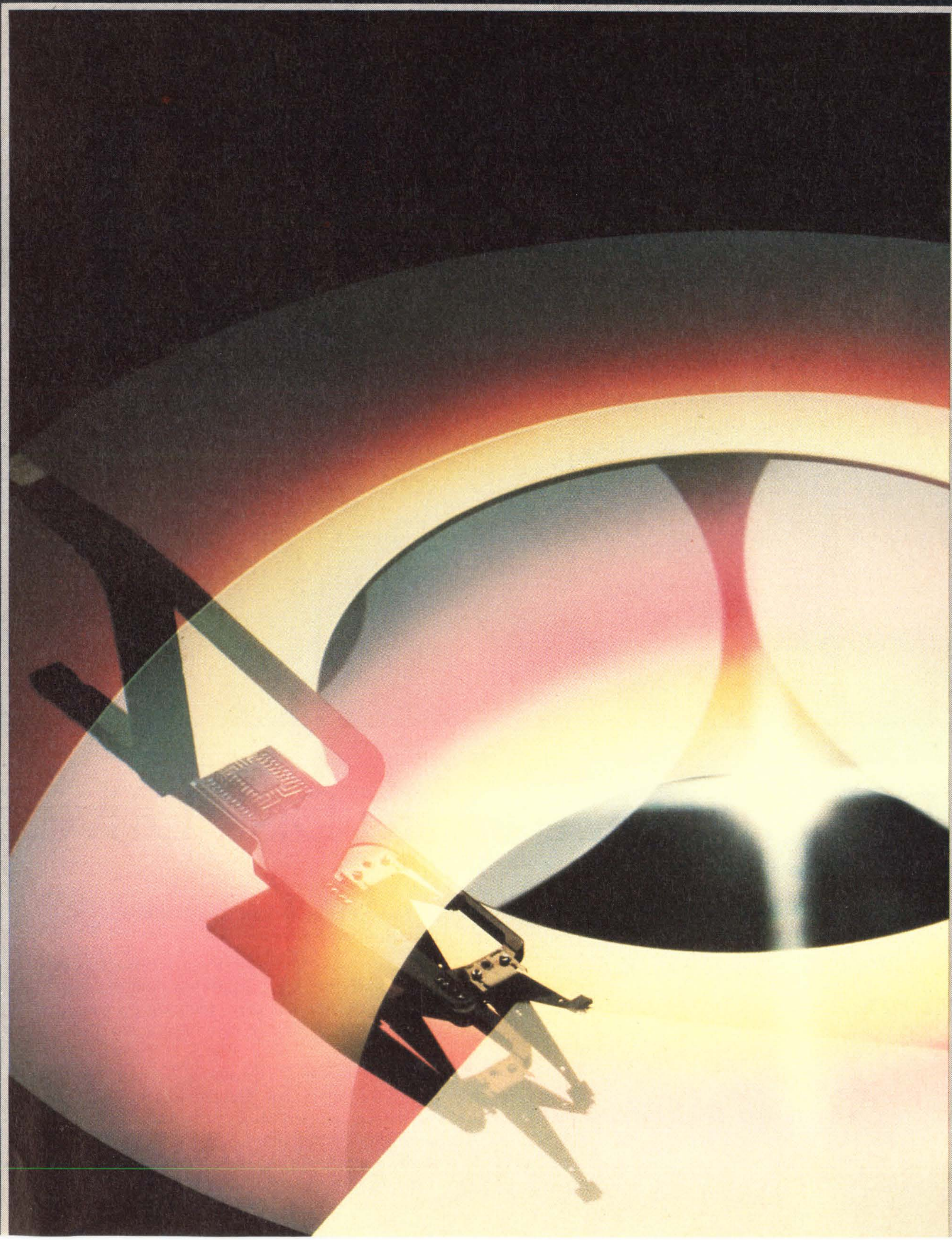


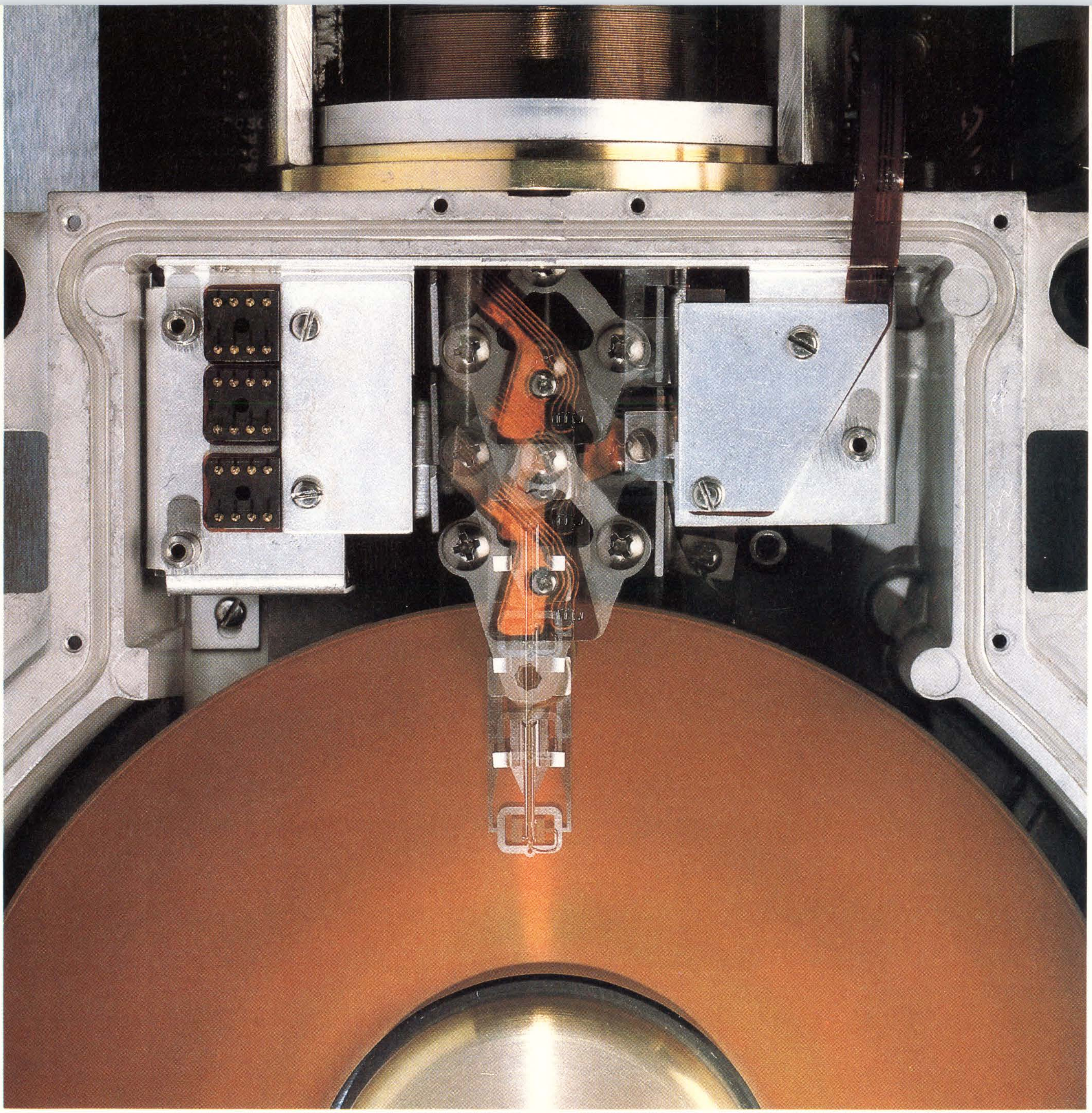


Photo courtesy Priam

Designer's Guide To Disk Drives

Winchester disk drive technology is one of the fastest changing, fastest growing segments of the computer industry.

by Doug Eidsmore and Bob Hirshon, Contributing Editors

Nothing sparks design innovation like a complex challenge paired with an insatiable demand. This explains why Winchester disk drive technology is one of the fastest changing, fastest growing segments of the computer industry.

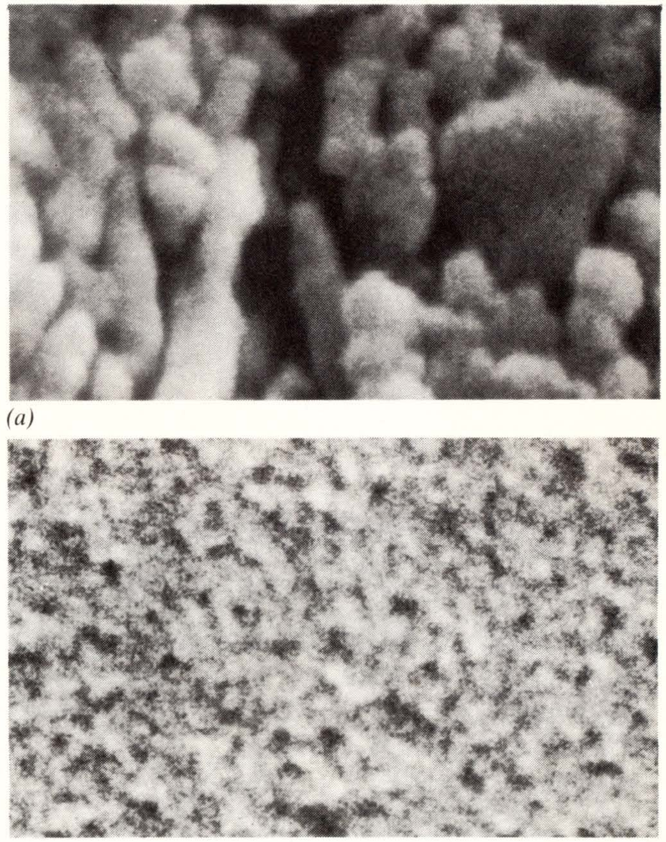
Winchester design provides a challenge not only in the area of electrical engineering, but also in mechanical design, electro-optics, magnetic materials, coating deposition, aerodynamics, ferrofluidic seals, surgically-sterile manufacturing and a diverse assortment of other disciplines. Each of these areas poses specific challenges for industry specialists and provides numerous footholds for innovation.

Significant innovation can mean significant rewards, thanks to the current demand for memory. The bottom line is an estimated \$15 billion to \$20 billion annual market for Winchester disk drives by 1986.

The activity resulting from this design potential and high demand has had both positive and negative consequences. On the positive side, improvements in small Winchester price/performance have been exponential, making possible vastly increased local mass memory, especially in small systems and work stations. In fact, the availability of low-cost, high-capacity Winchesters has been a key force in making powerful, local processing possible in such memory-intensive applications as solids modeling and image processing.

On the other hand, frenetic activity has made standardization difficult and has also led to such a profusion of technology that it's difficult to distinguish the viable new ideas from those that sound good, but won't make it out of the lab. Countless early announcements of unproven technologies, generally by companies seeking venture financing, haven't helped the situation.

Sound Winchester evaluation under these conditions means keeping abreast of drive technology, being aware of interface options, and understanding the relationships between applications and drive selection. Regarding technology, functional areas currently exhibiting particularly great activity include disk media, R/W heads, and head positioning systems.



(a)

(b)

Figure 1: Although ferrite and thin-film disks look equally smooth to the naked eye, these 40,000X electromicrographs reveal that thin-film media (b) is smoother and more uniform than particulate iron oxide media (a). (Photos Courtesy Memorex).

Drive Technology: Media

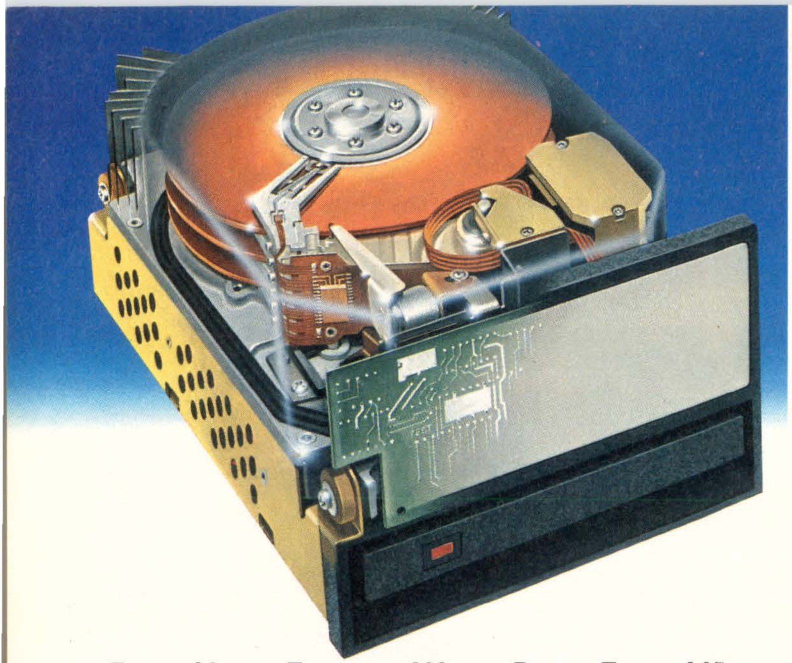
Magnetic recording on today's Winchester disk drives is similar to magnetic recording first employed in tape recorders 40 years ago. Particulate gamma iron oxide (γFe_2O_3) is still the medium of choice to act as the recording surface. The gamma (γ) refers to the phase of the iron oxide: γFe_2O_3 indicates the low-temperature, metastable phase, while αFe_2O_3, or alpha iron oxide, refers to a high-temperature, stable phase. Because of the structure of αFe_2O_3, its magnetic moments tend to cancel each other out, resulting in little net magnetization.

The needle-shaped particles of gamma iron oxide act like miniature bar magnets, each with a north and south pole. Consequently, when arranged in a line, they may lie one of two ways: either north-pole-first or south-pole-first. By selectively altering the direction of these magnets, the write head records information. By detecting the resultant changes in polarity as it moves along this string of magnetized particles, a read head deciphers the information. A north-to-south change in polarity may indicate a digital "1", in which case a south-to-north change would indicate a "0".

A single line of these magnetized regions is called a *track*; in disk drives, tracks occupy concentric rings around the disk surface. In drives recording on multiple disk surface, the term *cylinder* refers to a given track on all of the disk surfaces. In other words, if you construct an imaginary cylinder at the radius of, say, track 24 on disk surface 1, extending downward through the stack of platters, the tracks through which the cylinder passes together comprise cylinder 24. Disk surfaces divide radially into *sectors*, resembling slices of a pie.

The density of information that may be recorded along a track is measured in flux changes per inch (fcpi) or bits per inch (bpi). In actual operation, the two may or may not be equivalent, depending on the encoding method used to record data, but for media comparisons the terms are often used interchangeably. Radial density is measured in tracks per inch (tpi). Areal density, measured in bits per square inch (bits/in^2), is the product of these two values.

Getting more bits into a square inch of area requires smaller particles of iron oxide deposited in a thinner layer. Conventional particulate ferric media consists of iron oxide mixed with non-magnetic binders and fillers, and may be deposited as thin as 300 μinches (.75μ). This allows a bit density of about 15,000 bpi and a track density of about 1000 tpi, for an areal density of 15 Mbits/in^2. Theoretically, this density could be doubled, but at higher densities there are so few magnetic particles per bit cell that signal resolution and am-



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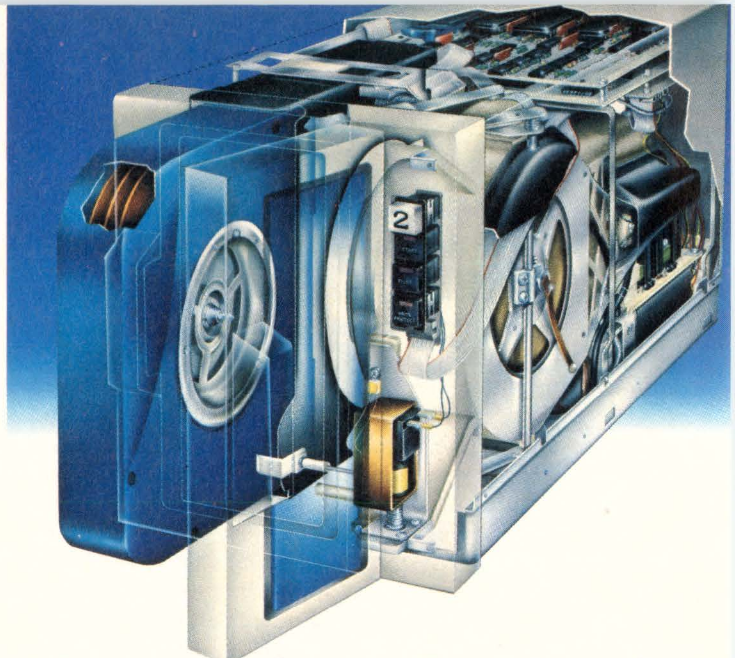

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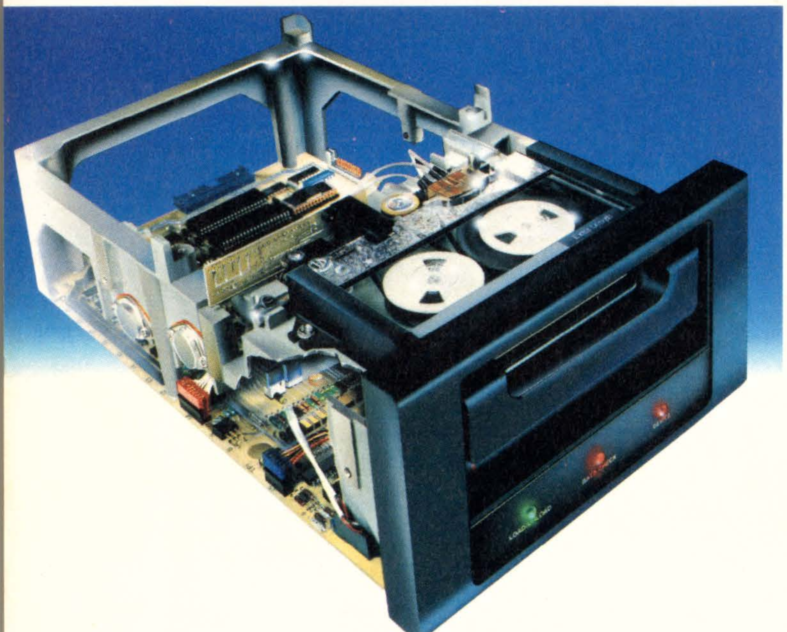

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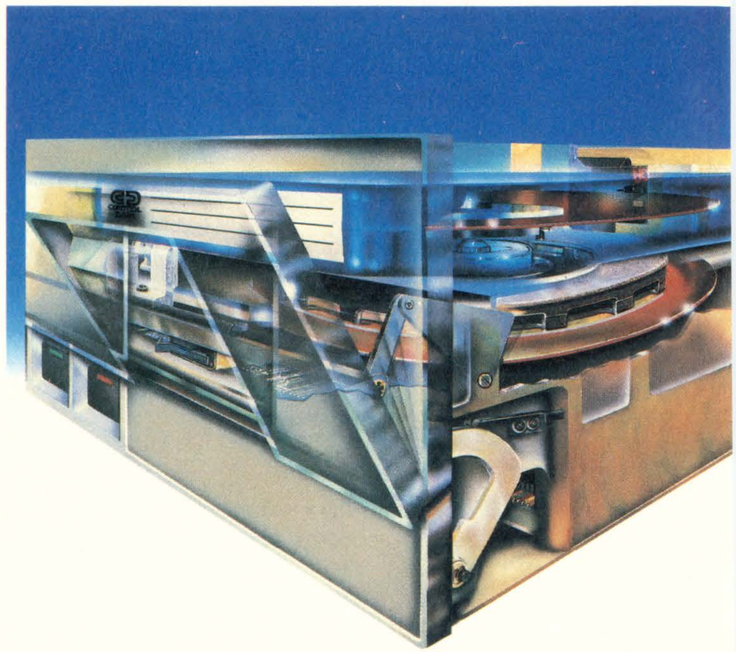

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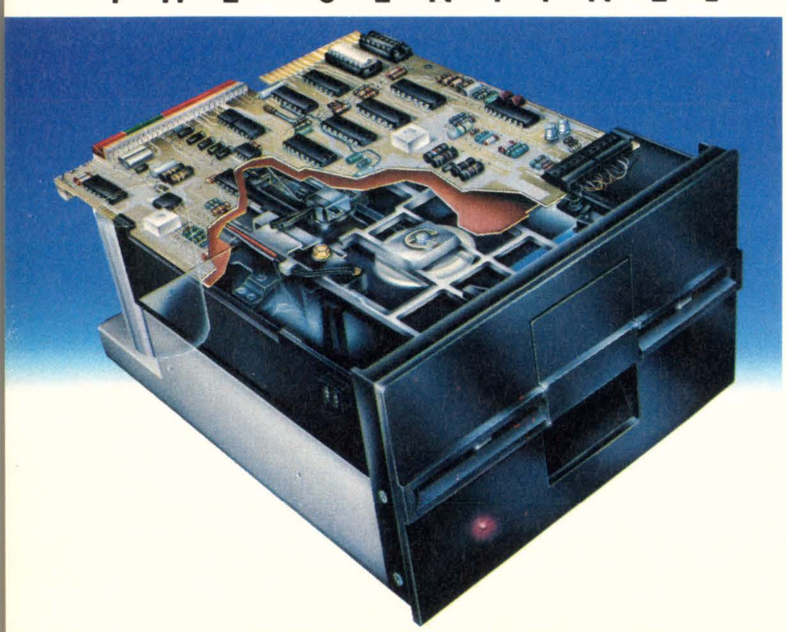

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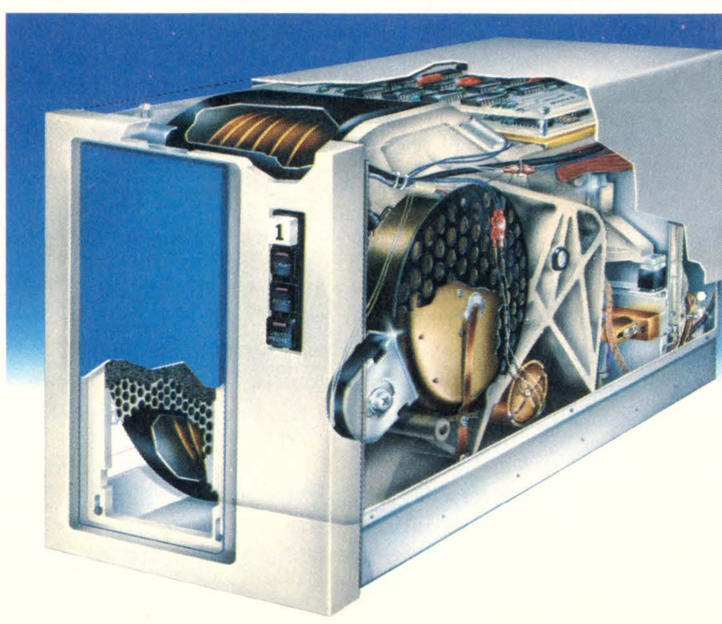

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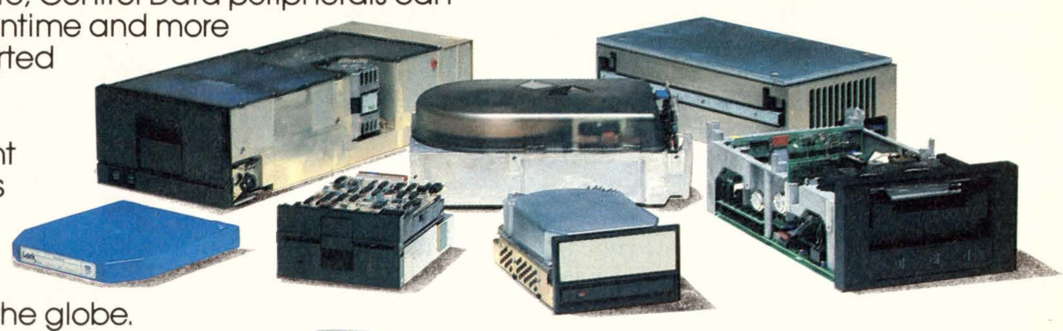

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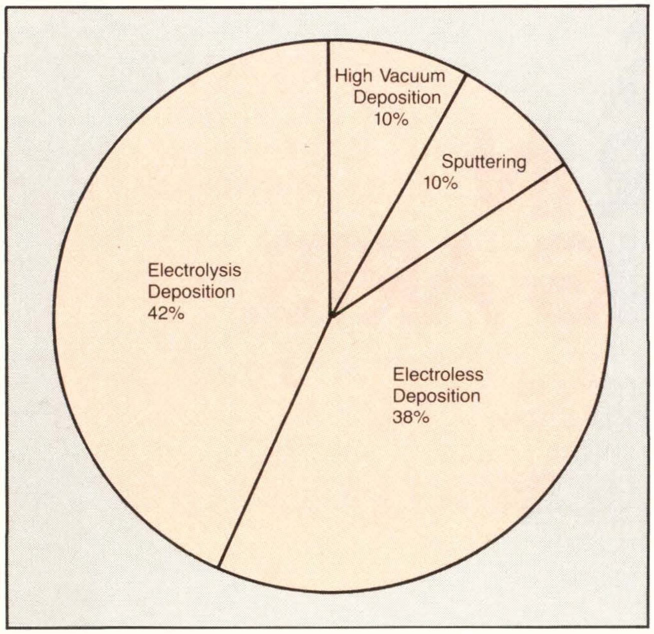

Figure 2: According to a survey conducted by Memorex, 29 companies manufacture thin-film media, using four processes.

plitude are extremely low. In addition, quality control of the media becomes extremely critical since small discontinuities translate to large error rates. Also, current R/W head positioning technology is limited to about 1000 tpi. Still, even 15 Mbits/in^2 is dense enough to pack 15 Mbytes on a 5.25″ disk surface.

Thin-Film Media

Higher densities than that may be obtained by using *thin-film*, or *plated*, media (**Figure 1**). Both of these terms refer to a disk coated with a continuous layer of extremely fine, uniform, non-ferric magnetic particles, usually a combination of nickel, cobalt, phosphorous, chrome and/or the alloys of these metals. The film may be as thin as 1 μinch (.075μ). However, thin film isn't necessarily thin: it may be deposited 300 μinches thick for use in older, head-per-track disk drives.

Nor is plated media always plated. "Plating" generally refers to chemical or electroplating processes, but thin-film media may also be made by high vacuum deposition and *sputtering* (**Figure 2**). Sputtering is a deposition technique involving bombardment of the magnetic material with positive ions in the presence of the surface to be coated.

Track density isn't much higher for plated media than for particulate media, but bit density, resolution, amplitude, data integrity, and durability all are markedly improved. Because thin film doesn't require fillers and binders, there's more magnetic material in a smaller area, increasing resolution and amplitude at high bit densities. Thinner media provides a narrower, more concentrated signal with less head fringing (**Figure 3**). And thin film media is more durable and abrasion resistant than is standard iron oxide media, although thin-film media manufacturers have had to cope with long term corrosion problems.

A study published in May by Memorex surveyed 26 disk drive manufacturers concerning their attitudes about thin-film media and found that availability, and not corrosion problems, was the chief reason many of them weren't using plated media. Most felt that individual media companies were solving corrosion problems, but they weren't so sure about their ability to meet growing demands for the media. Memorex's conclusion? "The need for plated media is here today, but the industry supplying this product, in the volumes that will be demanded, won't be viable for at least 18 to 24 months."

This estimate may be several months on the pessimistic side, in light of recent developments. First of all, Winchester disk manufacturers, tired of waiting for high-volume shipments from media manufacturers, have begun to produce their own plated media. This will cut back somewhat on demand.

In addition, Ampex has stepped up production of its San Jose manufacturing facility, opened earlier this year. The plant now produces 15,000 units of Alar-brand plated media per week, ramping up for an eventual output of 38,000 per week by 1986. Also, Ampex has licensed Computer and Communications Technology Corp. (Santa Barbara, CA) to produce Alar media. A number of other companies have also recently announced plans to manufacture various types of plated media in high volume.

Of course, "high volume" is a relative term. To smaller Winchester drive manufacturers building high capacity, high performance drives, it means several hundred units per week. To a company like Seagate Technology, high volume means several thousand units per week. The "high volume" requirements of the former will undoubtedly be met well before those of the latter.

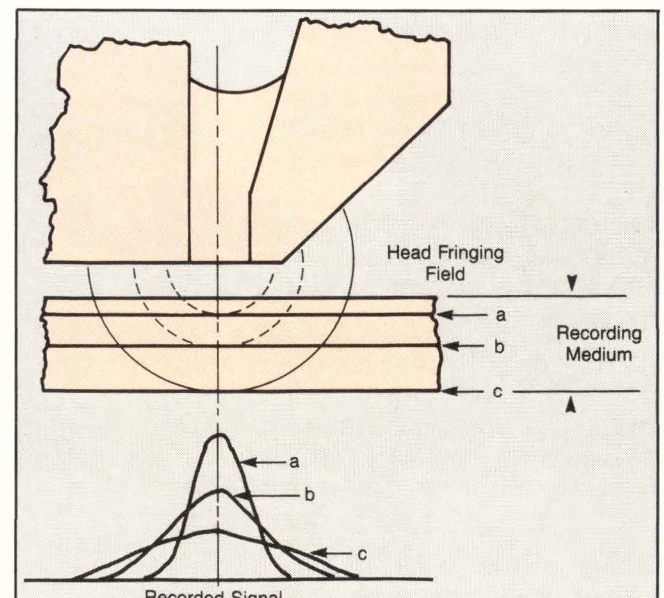

Figure 3: Thin-film (a): less head fringing and a higher-amplitude recorded signal than thicker media (b, c). (Courtesy Evotek).

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Perpendicular Recording

Even with thin-film media, maximum bit densities are approximately 30 Mbits/in^2. This maximum density is set by two factors. First of all, to prevent the north and south poles of each magnet from demagnetizing each other, the magnets must be considerably longer than they are wide. So as more magnetized regions are squeezed into less space longitudinally, and they are made shorter in length, their width must be decreased proportionately. As a result, the mass of each magnet drops dramatically as bit density increases. Eventually, there is so little magnetic material per bit that the output signal is too weak to be detected above random noise.

Secondly, with magnetized regions adjacent to each other linearly, there are south poles adjacent to south poles and north poles adjacent to north poles. The repulsion of these like charges causes demagnetization and physical deformities that become more exaggerated at higher bit densities.

Perpendicular recording is one solution to these problems. Rather than arranging the magnetic regions lying linearly along the track, perpendicular recording (also known as vertical recording) arranges them standing down into the track (**Figure 4**). Since the magnetic regions are much narrower than they are long, for the reasons mentioned above, this vertical configuration immediately increases linear bit density; width of the

New Servo Techniques Provide High Performance And Reliability At Low Cost

As 5¼″ Winchester disk drive capacities and performance reach levels exceeding those of past 14″ Winchesters, manufacturers are placing increasing emphasis on the design of reliable, low-cost high-performance head-positioning mechanisms. The open-loop servo systems common in first generation and low-end (500tpi) 5¼″ Winchesters are not up to the task of accurately positioning read/write heads in the new high-track density drives, which feature densities of about 1000tpi. At the same time, virtually all current dedicated surface closed-loop servo systems, particularly the di-bit/tri-bit servos, are relatively expensive and require defect-free media surfaces.

Disk drive reliability and cost is of primary concern to system integrators. Pressure is bearing on 5¼″ Winchester manufacturers to provide higher performance at lower cost, while maintaining high reliability. Closed-loop servo systems using a dedicated disk surface for track following allow not only higher performance over stepper motor actuators, but also higher data reliability. The rule of thumb for maximum head-to-data track offset while maintaining data reliability is 10% of track pitch. Therefore, a high performance 1000tpi machine must maintain 100 μ inches or less off-track, including all servo tolerances and non-servoable factors. Environmental temperature variations cause a shift in head to disk position that can be corrected by a closed-loop servo system. In stepper actuator systems, there is no closed-loop feedback for a shift in head-to-disk position. Such open-loop stepper actuator drives are limited to 400 to 500tpi, especially if data reliability is required over a wide temperature range.

The dual-frequency design from Vertex uses a fully dedicated surface of one of the disks for track servo information. A read head picks up the

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track servo information from the dedicated surface and through electronic manipulation a position error or off-track signal is developed that is used for feedback to the actuator motor to correct any off-track error that occurs as the disk rotates under the servo read head. Because the servo read head is fixed to the data read/write heads by a rigid actuator arm, any movement of the servo head is translated to all other read/write heads of the disk.

The off-track error signal is also used during a seek operation. As the actuator is moving across the disk during a seek, the error signal produces track crossing pulses that may be counted in order to determine track location.

The difference between a dual-frequency servo system and the more common di-bit or tri-bit servo systems is in track servo information recorded on the dedicated servo surface and how this servo information is manipulated to develop an off-track error signal. Once the off-track error signal is developed, the dual-frequency and di-bit or tri-bit servos are virtually the same.

The dedicated servo surface in a dual-frequency system has alternating tracks recorded with two frequencies, f1 and f2. A third frequency, f3, is recorded on several inside and outside tracks as a guardband frequency to indicate the extent of useable area of the disk. A fourth frequency, f4, is recorded on track 0 to indicate the home position of the actuator (See Figure). The f1 and f2 used in the Vertex design are 700kHz and 1020kHz respectively. The choice of the f1 and f2 frequencies is limited for the low frequency by track fringing and harmonic distortion characteristics and the high frequency by data frequencies. The R/W heads are "on-track" when the servo head is located midway between an f1 and f2 frequency band, so that the relative amplitude of the f1 component and f2 component signal is equal as read by the servo head. Any "off-track," where the servo head is more in the f1 band than the f2 band, will produce a higher signal amplitude of f1. If the servo head is positioned more in the f2 band than the f1 band, then a higher signal amplitude of f2 is produced.

The servo head continuously samples f1 and f2 frequencies. The servo electronics separates the f1 and f2 component, sums and averages the signals and positions the head at the point where this averaged signal is zero—exactly between the two f1, f2 frequency bands.

This servo technique offers a stable and accurate feedback control system with an "error" signal that tells how much and in which direction the R/W head is "off-track." Off-track accuracy is maintained at ±100 μinches.

The dual-frequency servo offers both cost and reliability benefits over the classical di-bit/tri-bit servo designs. The most significant benefit is the dual-frequency method's relative insensitivity to defects in the servo disk surface. Di-bit/tri-bit methods require error-free servo surfaces. Because the dual-frequency servo continuously samples f1 and f2 amplitudes, media defects are averaged out and not sensed by the servo. The result is a significant improvement in manufacturing yield of servo surfaces of at least two to one over di-bit/tri-bit methods. A corresponding improvement in field reliability is also enjoyed since servo surface defects that occur in the field do not affect servo performance, whereas with a di-bit/tri-bit type servo, a servo surface defect may cause a failure of the servo and require disk drive maintenance to repair.

The dual-frequency servo system does not provide a write clock or an index mark from the servo information as with the di-bit/tri-bit technique. However, 5¼" Winchester formats do not use servo-generated index or clock information, making both superfluous. The 5¼" Winchesters are designed with tight tolerance spindle speed control, while the data format allows for large index tolerance so that an index may be generated externally or within the spindle motor.

Manufacturing servo writing equipment required to precisely record the servo tracks is less complex for dual-frequency servo systems. Precise servo track position accuracy is important to any servo method. However, the di-bit/tri-bit methods require exact bit and phase close, an index mark, and precise phasing of the di-bits or tri-bits from track to track. This requires complex servo writing equipment that cost roughly $250,000, compared to dual-frequency servo writers costing around $50,000.

The servo read head azimuth alignment is critical in di-bit/tri-bit servo methods to insure precise phase relationship of bit sync information. Because the dual-frequency method uses a relative amplitude difference of f1 and f2 frequencies, servo head azimuth alignment is not critical, thus reducing production costs and service requirements.

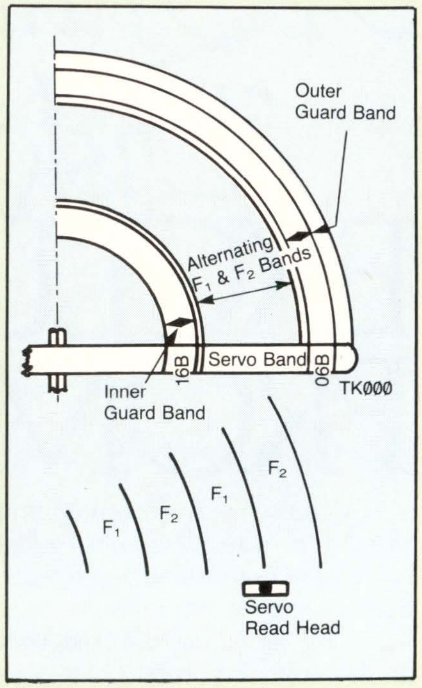

Figure 1: Servo disk surface.

An additional advantage of the dual-frequency servo system is the ease of separating write data noise out of the servo read channel. The f1 and f2 frequencies are recorded well below data frequency, so write data noise that may be injected into the servo read channel via a read/write head to servo head cross talk can easily be filtered out.

The dual-frequency servo system is a key reason Vertex Winchester drives have achieved performance of 30 msec average access and 72MB capacity while maintaining low cost. This cost-effective servo technology can easily provide much higher performance levels as well, and may become the dominant servo technology in low-cost, high-performance 5¼" Winchesters.

John Fravel
Electrical Engineering Manager
Vertex Peripherals
San Jose, CA
Write 356

magnet, rather than length, now determines bit density. The vertical dimension of the magnet can remain long, as the width decreases, effectively increasing the length-to-width ratio of each magnet, thus improving its magnetic qualities. Also, eliminating adjacent areas of like polarity allows packing the magnets closer together without demagnetization and deformation.

Although ultra-thin media is not a necessity with vertical recording, the media must be made of a crystalline substance, such as chromium cobalt, that will magnetize along a perpendicular axis. As a result, lack of media is a more serious problem for vertical recording even than for thin film recording. According to a second Memorex survey, this one of 29 media suppliers, only three manufacturers surveyed plan on producing media to support vertical recording in the near future. Three more said they will eventually support it, and three other manufacturers said their media would support vertical or longitudinal recording.

The Japanese seem to be at the forefront of vertical recording, not only for use in computer-related products, but also for use in audio and visual recording equipment for the entertainment industry. There are, however, major R&D efforts going on at many large rigid disk drive companies in the US. Lack of announcements concerning vertical recording from these companies doesn't necessarily indicate a lack of activity so much as a demand for secrecy. And at least one US-based firm, Applied Information Memories (Milpitas, CA), has outpaced even the Japanese, and plans to have a vertical-recording Winchester on the market by next year.

The promise of perpendicular magnetic recording is considerable. By eliminating demagnetizing problems associated with longitudinal recording, bit densities on the order of 100,000 bpi are predicted. Theoretically, areal densities of $100{,}000 \times 100{,}000$, or 10^{10} bits per square inch would be recordable, if R/W heads could be positioned to fine enough tolerances. And one Japanese company has projected even higher possible densities, on the order of 440,000 bits per inch. If attainable, bit densities of these magnitudes would allow single-surface 5.25″ disk capacities measurable in gigabytes. Of course, these densities aren't attainable with current or even projected technologies. But if perpendicular recording fulfills even a small part of that promise, constraints other than media should become the limiting factors in magnetic recording capacity.

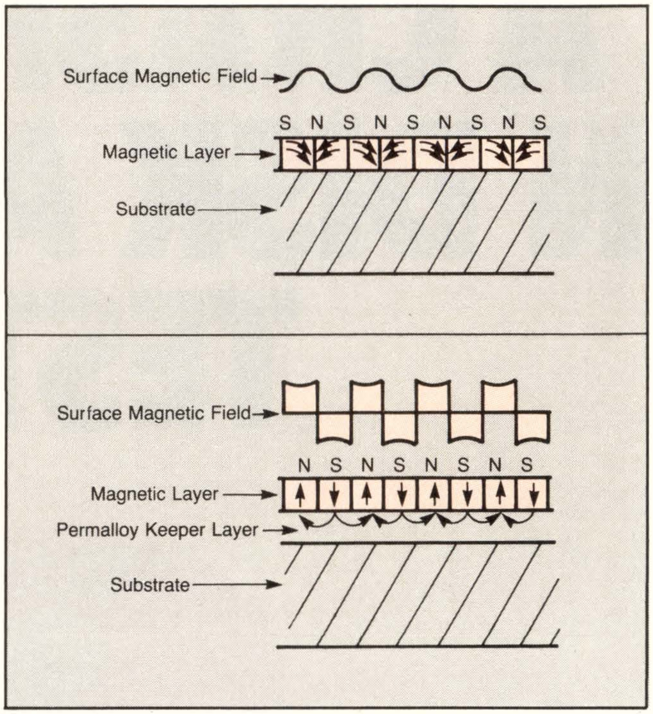

Figure 4: Vertical recording (b) reduces demagnetizing effects caused by adjacent poles of like charge, and produces a sharper surface magnetic field than conventional horizontal recording (a). (Courtesy Vertimag).

R/W Heads

Headlines of two years ago read "Thin Film Heads Invade Micro-Winchesters". Rather than an invasion, however, thin film heads are engaged in more of an inexorable migration into Winchester disk drives. Eventually, they will all but replace conventional heads. But today, two years since the "invasion", non-thin film heads are still the dominant R/W head technology in Winchesters.

Conventional head technology hasn't stagnated in anticipation of thin film heads. A number of improvements have been made over traditional monolithic nickel-zinc-ferrite heads used in larger disk drives to create heads more suitable to mini- and micro-Winchesters (**Figure 5**). For example, use of manganese-zinc rather than nickel-zinc boosts the heads' signal output, and provides a frequency response better suited to small Winchesters. Composite heads isolate the MnZn or NiZn core, and allow a shorter flux path. The result is increased signal output and decreased parasitic inductance.

The combination of a low mass slider (the slider is the block on which the transducer is mounted) and a thin, rigid load beam is known as the Whitney suspension/slider, and was developed as part of IBM's 3370/3380 second-generation Winchester disk drive project.

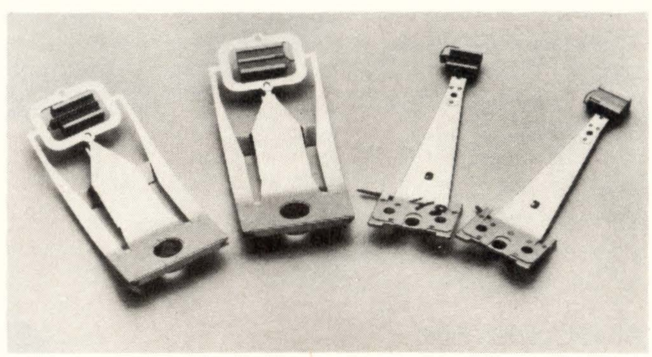

Figure 5: The heads shown from Applied Magnetics are, from left: Standard, full-size monolithic ferrite slider on the Winchester suspension; full-size composite slider on Winchester suspension; mini-monolithic ferrite slider on Whitney suspension; and a mini-composite slider on the Whitney suspension.

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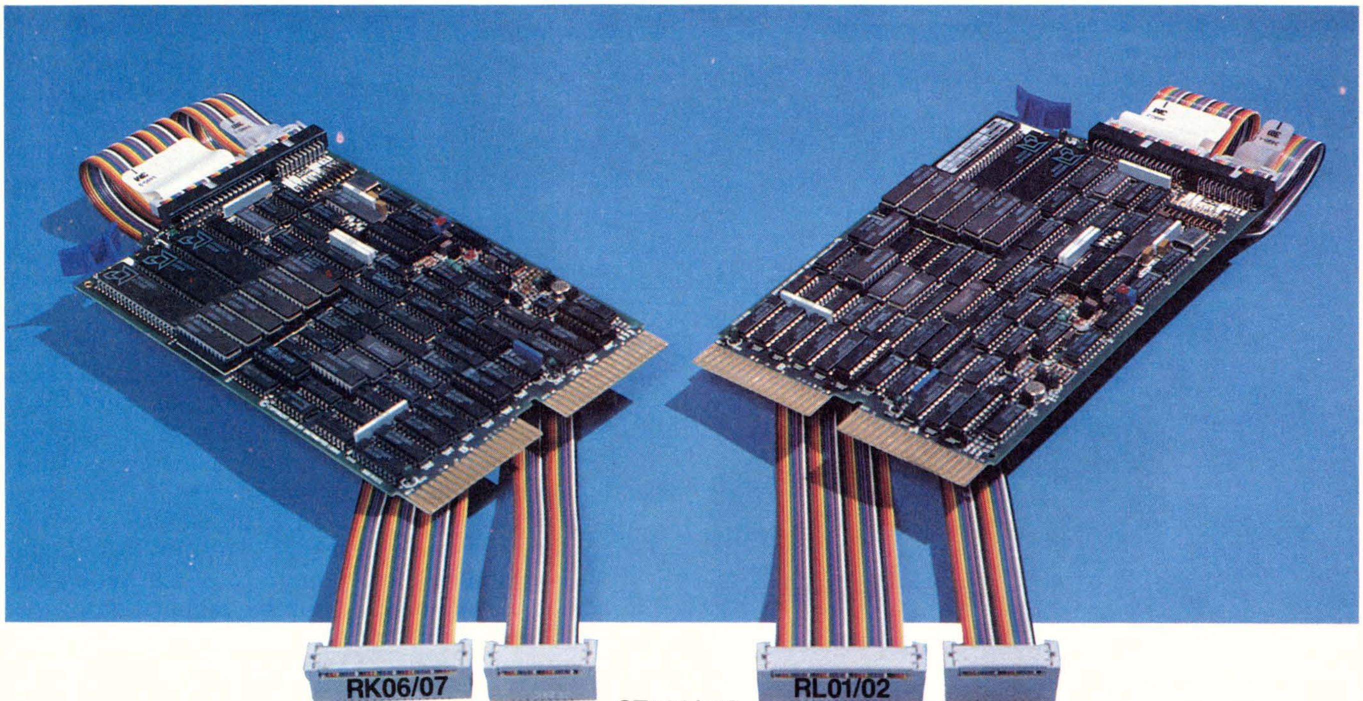

ST506/412

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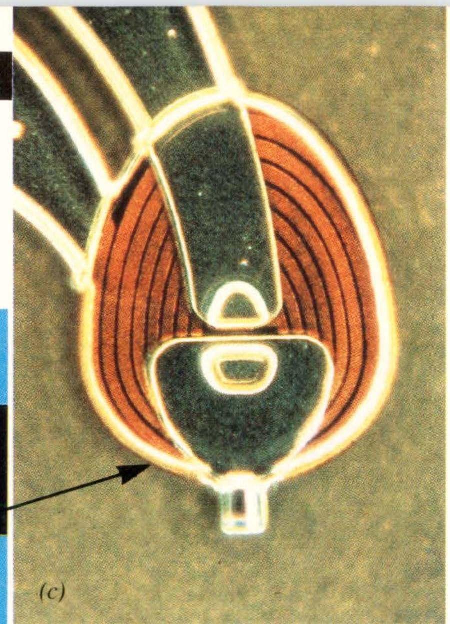
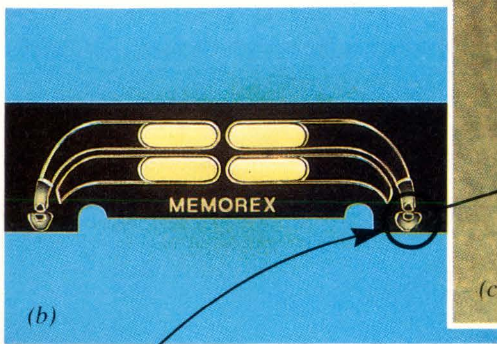
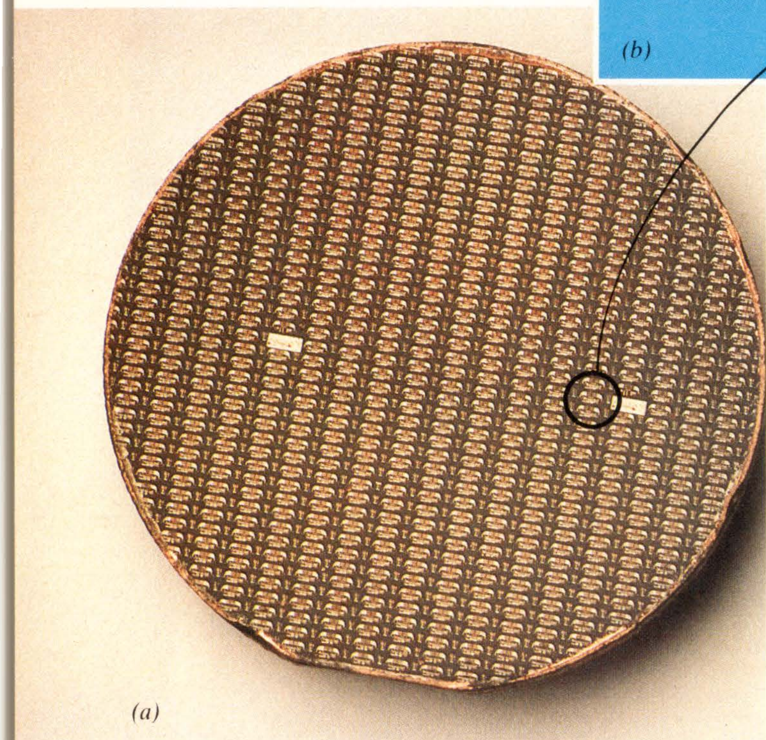


Figure 6: A photo/mask/etch deposition-type process can produce several hundred R/W heads from a single 3½" silicon wafer (shown actual size). The heads are produced in pairs (b) for redundancy purposes, and have extremely fine gaps between the copper "wires" (c) which, in conventional ferrite head manufacturing, would be hand-wound copper wire.



(b)



(a)

Whitney technology allows lower head flying height, improved head stability, higher tracking accuracy, and higher signal-to-noise ratio. The result is higher potential areal density and fewer errors.

In addition, the low mass sliders, narrow suspension and decreased flying height have other benefits: Maxtor (San Jose, CA) found that they could save enough space with Whitney sliders and suspensions to squeeze eight platters into their 5.25" Winchester drive.

Thanks to these and other improvements, conventional-style heads now allow 10 Mbits/in^2 in the field, and 20 Mbits/in^2 in the lab.

Thin Film Heads

Beyond the 20 Mbits/in^2 level, thin film heads become necessary. Thin film heads have little in common with thin film media, except that both are manufactured using the sort of deposition techniques used to make semiconductors (**Figure 6**). With media, these fabrication techniques allow a thinner, more consistent coating. With heads, thin film fabrication allows a narrower gap between the magnetic pole tips on the transducer. It also allows a greater number of narrower copper transducer windings. As a result, thin film heads are expected to provide 32 Mbits/in^2 by next year.

Perhaps more important than the increased bit densities thin film heads allow is the potential for decreased head manufacturing costs. As head manufacturers refine and perfect thin film head production, they should be able to produce a much more consistent product at higher yields, and benefit from the elimination of mechanical and manual manufacturing techniques used for conventional heads (**Figure 7**).

Positioning Systems

No matter how many tracks per inch heads can write and media can retain, it's of little consequence unless the heads can be positioned precisely enough to distinguish them. To accomplish this task, all movable head disk drives have, in addition to the spindle motor, a second motor, or actuator. This motor moves an arm assembly, to which are fixed the R/W heads. Positioning accuracy and speed are functions of the motor's ability to quickly and precisely move the arm assembly, and the arm assembly's ability to translate that motion smoothly to the R/W heads. In addition, some drives employ a servo positioning system. In these drives reference data on the disk surface provide the R/W heads with location information.

In most cases, either a stepper motor or a voice coil moves the head assembly. Each has its advantages. Stepper motors are inexpensive, extremely reliable, and allow the drive to be easily mounted in any orientation without loss of performance. Voice coils are more accurate and faster, but are also considerably more expensive. Also, some voice coil positioning systems require that the drive be mounted flat.

The arm assembly can be either linear, meaning it moves back and forth, or rotary, meaning it pivots on a shaft. Linear positioning is the more direct technique, minimizing dynamic instability. However, linear systems usually require more space in the drive package, and most must be mounted flat. Rotary positioners consume less space, and can be balanced to allow mounting in any orientation.

R/W head positioning systems may be *closed-loop*

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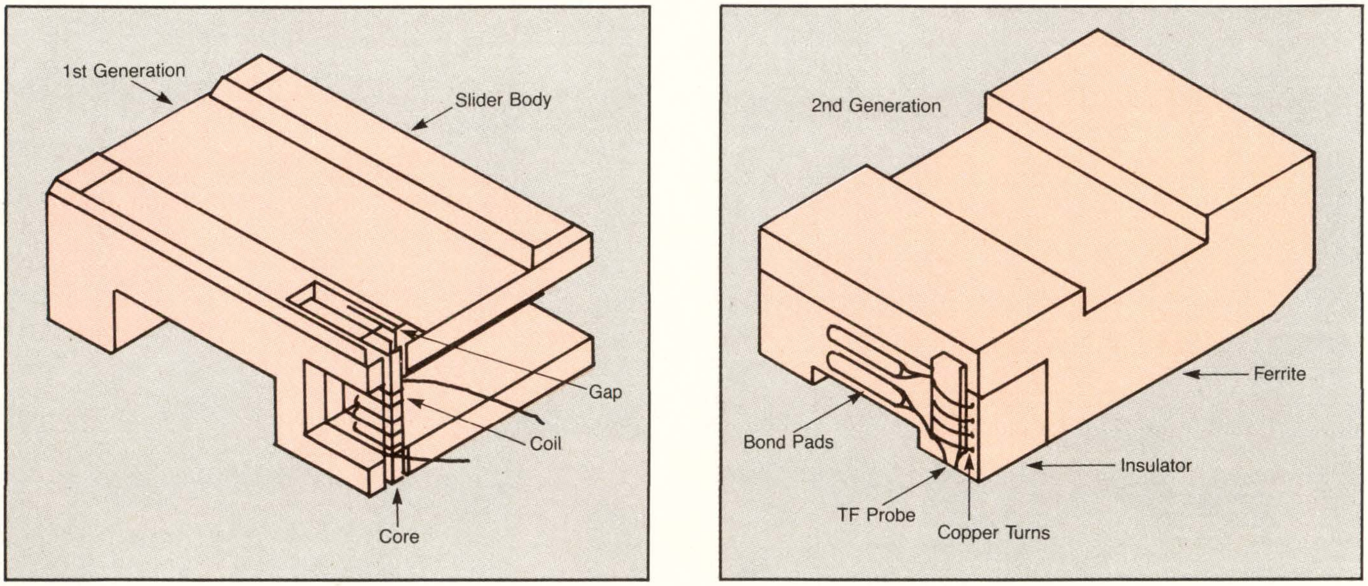

Figure 7: The vertical-recording R/W head at left is a narrow-gap composite head manufactured using conventional techniques. The "probe-style" head at right can be made using thin-film processes. (Courtesy Applied Magnetics).

or *open-loop*. Closed-loop systems sense their location from reference data stored on the disk surface and feed this information back to the actuator for more precise head positioning. Open-loop systems operate blindly, relying on the mechanical accuracy of the actuator mechanism to locate the proper track.

Open-loop systems, obviously, are much simpler and less expensive than closed-loop systems. But because the R/W heads of open-loop systems are not position-sensing, they rely directly on the accuracy of the actuator—they have no way of determining if they are off track. At low track densities, this is not a problem, but as track density increases, open-loop systems become unsuitable. Also, open-loop systems can't compensate for environmental factors, such as vibration and thermal expansion. Consequently, they are limited to lower capacity, lower track density disk drives.

Closed-loop, or *servo*, positioning systems have servo heads that read reference information that was permanently written onto the disk surface during manufacture. This positioning information is then fed back to the actuator that controls head movement, thereby keeping the heads on track, despite mechanical off-tracking, vibration or thermal stress.

Closed-loop systems may be either *dedicated* servo systems or *embedded* servo systems. Dedicated systems reserve one disk surface solely for reference data, and one head solely to read it. The servo head positions itself according to the reference data on the disk surface. As it does so, it also positions the R/W heads serving the other disk surfaces, since they are physically attached to the servo head. The biggest problem with this technique is that it devotes an entire disk surface to reference data, lowering overall drive capacity. Also, because of the physical distance between the servo head and the R/W heads, mechanical off-tracking may occur, creating the very problem the closed-loop system was intended to overcome.

Embedded servo systems have reference data right in the data storage tracks, and the R/W heads double as servo heads. Some disk capacity is lost due to the space taken up by the reference data, but it is less than that lost in dedicated servo systems. And since R/W heads and servo heads are one in the same, off-tracking is kept in control, even under varying environmental conditions.

Positioning systems determine not only how many tracks can be read and written, but also how fast data can be accessed. *Seek time* indicates how long it takes the positioning system to put a R/W head on a particular track. Of course, this varies, depending on whether you're looking for track 9 or track 109, so *average seek time*, which is the average required for all possible seeks, is more meaningful.

To look for a particular block of information, more than the proper track is required; the correct sector is also necessary. *Latency time* is the amount of time it takes for a given sector to rotate into alignment with the R/W head once seek is complete. This is determined not by the positioning system, but by the disk spindle speed. *Average latency* is usually calculated as one-half of a disk rotation.

Access time is the total time required for the R/W head to locate a particular piece of data and begin data transfer, and is the sum of the seek time and the latency time. *Average access time*, one of the most commonly used performance specs for Winchester disk drives, is the sum of average seek time and average latency.

Device Level Interfaces

To the OEM or system integrator, the characteristics of a drive may be of less importance than the interface that the drive is designed to. The 5¼″ Winchester market has flourished adhering to the *de facto* ST506/412

standard. But the low transfer rate and lack of flexibility of the interface restricts the performance of high-end 5¼" drives. As a result, there are now three proposed standards that threaten the dominance of the ST506/412 interface. All three promise higher performance, higher capacity memory sub-systems than could be obtained by adhering to the established interface. For example, 10 Mbit/s, very high capacity drives can create the illusion that each user in a LAN has his own processor and CAD stations will be able to pull data off a drive rather than from inordinately large RAM memory.

The new interface contenders are, in the order of their introduction, the Enhanced Small Disk Interface (ESDI), an ANSI approved standard and a high performance Seagate inspired interface, the ST412HP (**Figure 12**). All three open up the 5Mbit/s ST506 transfer rate to at least 10Mbit/s. The ESDI and ANSI interfaces also move the data separator from the controller onto the drive, and data is transferred in a Non-Return to Zero (NRZ) format. This arrangement means each drive will require its own separator, a costly duplication in multiple drive systems, but it offers increased flexibility.

The ESDI specification defines two implementation modes, Serial and Step. The Step mode is used with stepper motor positioners and the Serial with linear and voice coil motors. The Serial mode uses NRZ data transfer along with serial commands and serial configuration and status reporting across the command cable. The Step mode also uses NRZ data transfer; however, the STEP and DIRECTION lines are used to cause actuator motion, meaning configuration and sta-

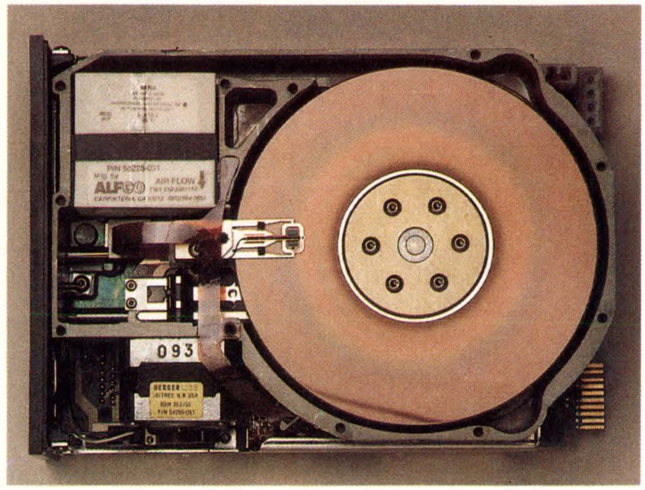

Figure 8: The positioning system on Seagate's 12.76-Mbyte ST412 uses a split-band actuator and a stepper motor for an average access time of 85 msecs.

Analyzing Disk Drive Specifications

With a few basic terms under your belt, you can avoid the pitfall of comparing apples to oranges when shopping for rigid disk drives. As with most product selection and evaluation projects, choosing a rigid disk drive for a specific application involves collection and analysis of data on the various alternatives available from manufacturers. Since no universal standard regulates the presentation of information in disk drive data sheets and advertisements, the potential buyer must become familiar with how manufacturers handle key specification areas to make product comparisons. This necessitates focusing on those areas where manufacturers use different approaches to present basic statistical information, identifying the way popular industry terms are used, and looking for important information which may be omitted.

Most manufacturers specify the total storage capacity in a given drive in its *unformatted* state. Formatted capacity, the actual usable storage space, may be different among drives of the same unformatted capacity. For example, some high performance drives have sophisticated spindle speed control circuits, and less format overhead is required for speed tolerance. These drives can support 33 sectors per track (256 bytes each), in addition to the more common 32 sectors format, therefore yielding a higher formatted capacity even though the unformated capacity of the drives is the same.

While very few vendors misrepresent their specifications intentionally, a lot of confusion surrounds the definition of Access Time. Part of this confusion stems from the fact that the list of 5¼" Winchester drive manufacturers includes companies from both floppy and rigid disk backgrounds.

Simply stated, *Access Time* is the delay between requesting data and getting it. At the drive level, there are two components to Access Time: Seek Time (positioning the read/write heads on the desired track) and Rotational Latency (rotating the disks until the desired track is found). Access Time and Seek Time are not synonymous.

The actual Seek Time of a drive is observed at the "Seek Complete" interface signal, which is false for the duration of the seek. By definition, Seek Time includes the head settling delay, although some vendors mistakenly quote this separately.

An important factor to consider in comparing Seek Time specifications is the way "Step" pulses are handled. Most drives now support "buffered mode" seeking, where a burst of step pulses are transmitted to the drive at high speed. By contrast, early drives could accept pulses only as fast as their stepper motor positioners could move. The step pulse rate becomes important because most drives don't begin positioning until the entire burst of "step" pulses has been received. If, for example, step pulses are sent at 100 μs intervals, a 200 track seek requires 20 ms to buffer the pulses before the positioner begins to move. Since the step pulse rate is set by the controller, not the drive, those Seek Time specifications that do not take this into account are not represented properly.

The more technically advanced drives address this situation by initiating movement immediately with the

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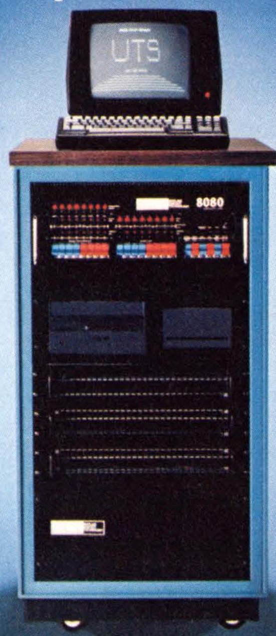

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The definition of Average Seek Time is another source of confusion. Most data sheets fail to define the meaning of "Average", but the most widely accepted technique is to measure the time of a ⅓ length seek. (The average distance between any two cylinders is ⅓ the number of cylinders.) Some specifications use an averaging method such as dividing the total time required to do all possible length seeks by the number of seeks performed. For a fair comparison, find out which technique is used in quoting the Average Seek Time.

Average Seek Time specifications are also subject to distortion by the drive's capacity and configuration. Obviously, a high capacity drive with more cylinders and/or surfaces provides access to more data within the limits of a ⅓ seek than does a low capacity drive. A more realistic comparison might result if the Seek Time is measured over the same number of cylinders or over the same amount of data. In some cases, the operating system software may dictate a seek length typical of normal system operation. Comparison on this basis yields "real world" results.

The *form factor* of 5¼" rigid disk drives has been adopted from the 5¼" flexible disk drives developed by Shugart Corporation, and is widely accepted as the industry standard. This permits OEM's to buy drives from multiple sources without changing mounting requirements. Some drives, however, exceed the standard 8" length and require additional depth in the system enclosure.

The *shock isolation* figures stated under the Physical Statistics section of a data sheet must also be carefully examined. If, for example, the drive you are considering requires additional shock isolation material it may exceed the standard form factor envelope. Your best bet may be a drive with shock isolation built into the industry-standard form factor.

Drive *mounting statistics* are often omitted in the physical statistics section of many data sheets. Information should be provided indicating the various positions in which the drive can be mounted and still operate properly. Some drives restrict mounting orientation to one or two of the three possible mounting axes. In addition, the mounting statistics should be carefully scrutinized by users installing systems in unstable environments, such as moving vehicles.

Another service rarely provided in the physical statistics section of the typical 5¼" rigid disk drive data sheet is a description of the *bezel and indicators*. Specifically, system integrators need to know if the exterior appearance of the drive unit will be compatible with most systems on the market. For the most part, a data sheet should indicate if the unit's bezel compliments the black, textured design, which has become the de facto industry standard. If the unit deviates from this standard, a complete color and style description should be provided. The location of the "selected" LED indicator, for example, varies considerably among vendors.

Acoustic noise statistics, another important issue frequently overlooked, should state the dBA level one meter away from the unit. If this statistic is missing, and the system will be installed in an office environment, you may be looking at a unit too noisy for the application you have in mind.

To be sure you are getting accurate *MTBF* statistics look for those 5¼" rigid disk data sheets that show separate HDA (Head Disk Assembly or "clean" area) and overall unit MTBF figures. Circuit board problems can often be fixed in the field by exchanging a spare board, but HDA failures require the drive to be returned to the vendor (with data still on it) for clean room repair. Buyers should also be aware of the fact that if the electronics have been isolated from the clean area, or HDA, a very high HDA MTBF figure will undoubtedly be presented along with a lower figure for the typical repair time.

When stating *media defects* in the reliability section of a data sheet, most manufacturers mention that the tracks on cylinder 0 (system tracks) are error-free. However, for complete media defect information you should look for an indication as to how defects outside this area are accounted for. For example, is a hardcopy defect map provided? How many defects are allowed in total? This information frequently is not included on a data sheet and must be requested.

Solid purchasing decisions can be made if the buyer understands how manufacturers present information. If you know the right questions to ask and are able to convert statistics to a common denominator, you can significantly improve the chances of finding the right product to fit your needs.

Bob Mortenson,
Applications Engineering Manager,
Micropolis, Chatsworth, CA
Write 357

tus reporting are unavailable over the interface. It is up to the disk drive manufacturer which mode to implement. Both may be implemented and a selection method established if the manufacturer so desires.

The specification has been revised since its release last spring. The latest version, dubbed Revision B, includes changes to the command structure. The number of basic commands has been decreased. But more flexibility and capability has been provided through command modifier bits.

One thing that hasn't changed from the original specification is the 10 Mbit/s transfer rate. At one time there was movement in the ESDI camp to establish a higher transfer rate. The two other proposed 10 Mbit/s interfaces may provide the needed impetus to up the transfer rate to 15 or 20 Mbit/s. Such a move would set high performance ESDI drives, such as Maxtor's, apart from the others. But such a move would have been easier to make earlier in the development of the specifications. Now, disk and controller electronic designs may have to be modified.

The ANSI standard is being sponsored by Priam and

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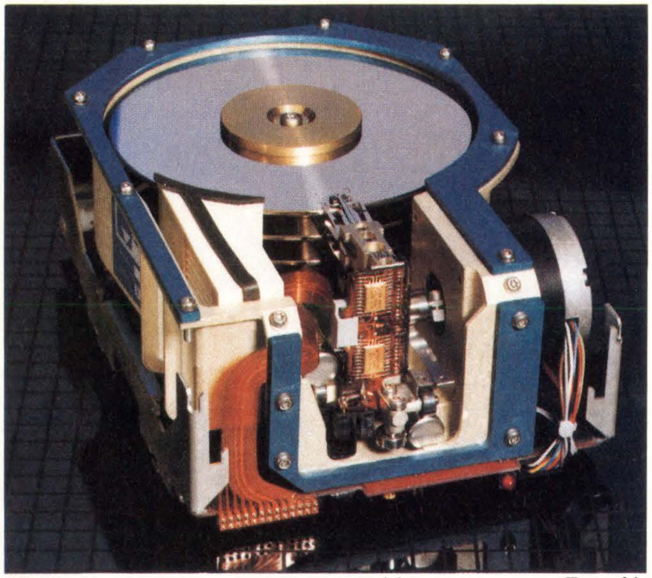

Figure 9: Using a stepper motor and linear actuator, Evotek's 5000 series drive provides an average access time of 49 msecs.

Xebec (Sunnyvale, CA). This standard was originally developed for 8″ Winchesters, but the promoters feel it can be, and is worth, adapting to 5¼″ drives. The main benefit the ANSI spec provides, they say, is that it is already defined and proven. For example, some of the 8″ control electronics being produced by semiconductor companies are ANSI compatible. The interface supports addressability of up to 8 devices in a daisy chain configuration. Radial attention and selection is supported throughout the daisy chain bus.

Critics of the ANSI interface point out that the standard by itself does not guarantee plug compatibility. To obtain device interchangeability, an operational specification must be defined. Neither the operating specification, the power requirements, nor the format used to write or read are defined.

The only manufacturers claiming to develop ANSI compatible products are Priam and Xebec. They have also announced the intention to establish an independent non-profit corporation, DISC Labs, Inc., to test and confirm that drives and controllers meet the standard.

The proposed standard has stirred up little interest among drive and controller companies. In fact, Priam's commitment seems less than wholehearted, as the company is also supporting the new ST412HP. The "HP" (for high performance) was developed by Seagate and along with Priam is supported by drive manufacturers Tandon and Atasi and by the controller companies Adaptec and Western Digital.

Designed to minimize the engineering required to upgrade systems based on lower speed ST506/412-compatible Winchesters, the ST412HP resembles the established ST506/412 interface. With the exception of one pin-out designation (RECOVERY MODE), the ST412HP interface is physically the same as the lower capacity ST506/412 standard. The addition of the RECOVERY MODE signal gives the controller the ability to microposition the head carriage during read operations. This provides the controller with an added data recovery technique on drives having higher track densities. Electrically, the ST506/412 and the new ST412HP interface are the same with the exception of the higher speed drivers and receivers needed to handle increased transfer rates. The old interface drivers and receivers were limited to a rate of about 7.5 Mbit/s. The new differential receivers/drivers will support transfer rates up to 15 Mbit/sec.

Like ESDI, ST412HP-compatible controllers will operate in the step mode, and can convert to the serial mode for drives with closed-loop servo positioning systems and linear or rotary voice coil actuators. But, ST412HP retains the modified frequency modulation (MFM) encoding scheme characteristic of ST506/412 interfaces. This interface will also support run-length limited (RLL) encoding schemes, permitting even higher drive capacities.

If adopted by a sizeable part of the industry, this new interface will create a booming demand for controllers. Other companies can be expected to enter the fray. One of the first companies to bet on such a demand is Seagate. They have added low cost controllers based on the Small Computer Systems Interface to their product line. The first "ST9000" devices will support SCSI at the systems level, and the 5 Mbit/s ST506/412 transfer rate specification at the drive level. Future Seagate controllers will incorporate the SCSI standard with the ST412HP drive-level interface.

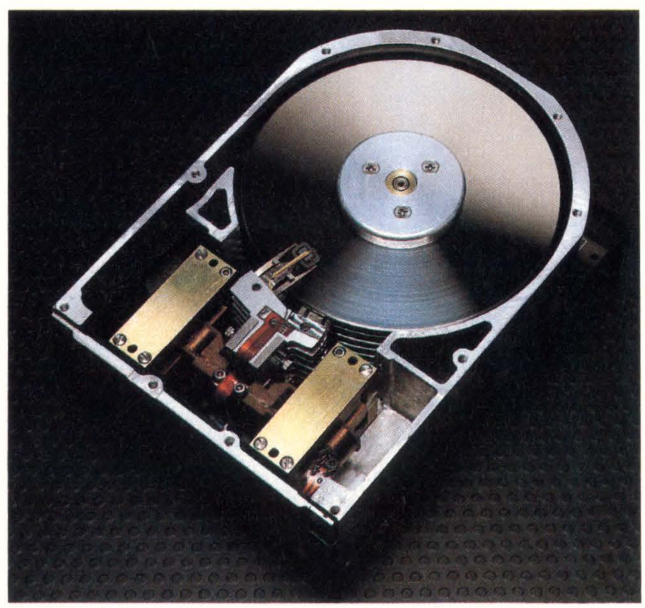

Figure 10: Priam's 500 series features a linear voice coil actuator delivering an average access time of 32 msecs.

Adaptec is supporting the standard with their ACS-1000 chip set. The set includes the AIC-100 Winchester controller chip; the AIC-250 encoder/decoder chip; and the AIC-300 buffer controller chip. They claim to be the first controller manufacturer to design and deliv-

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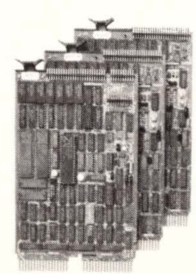

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er chips capable of a 10 Mbit/s transfer rate and are the only company currently shipping such products. These chips can be used to build ST412HP interface controller boards. Adaptec will offer an ST412HP board-level product when the drives become available. The company will continue to support other small drive level interfaces including ST506, SMD and ESDI.

Western Digital Corporation, another controller manufacturer, announced it is developing ICs and controller boards to support the proposed interface. Western Digital plans to offer board controllers that support the ST412HP interface in conjunction with the industry standard SCSI/SASI, Multibus and VME host interfaces, as well as selected custom bus interfaces for its key customers.

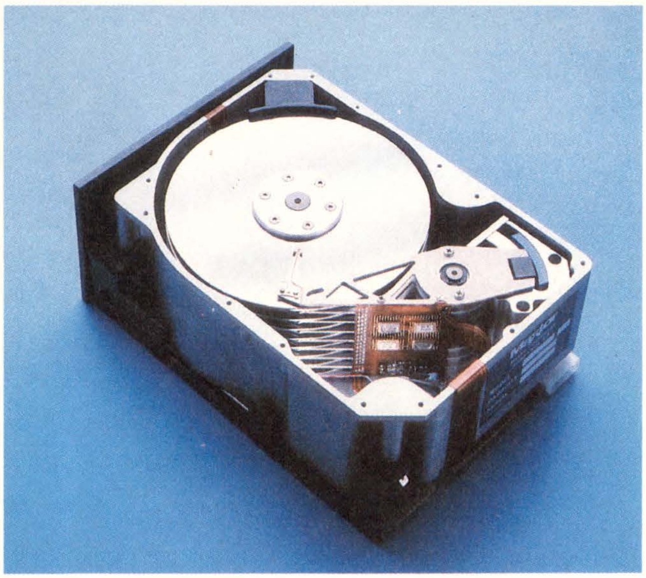


Figure 11: With a rotary voice coil positioning system, Maxtor's XT-4000 provides an average access time of 30 msecs.

Drive Selection

With such a myriad of drive and controller technologies available and now interface options, how does an OEM or system integrator evaluate and select a drive? Unfortunately there aren't any clear decision trees available. But a rough cut, in terms of drive capacity and performance, can be made by looking at some gross host system characteristics.

Some factors that influence capacity include: number of users, number of tasks, the operating system, the applications and the desired performance. A single user system can usually be supported by a 20-Mbyte or less, stepper motor, open-loop, 5 Mbit/s drive. These drives are often referred to as low-end drives. Some single user systems, such as engineering work stations, will require much higher capacities and higher performance than can be obtained by low-end drives, as will most multiuser systems.

The amount of memory each user needs in a multiuser system is a function of the systems and applications software used. Multiuser operating systems use memory to varying degrees. UNIX is a notorious memory consumer as are data base and spreadsheet applications packages. A central file server in a multiuser system may require more than 30 Mbytes. Because users are accessing a shared data base, disk contention can be a problem that will severely restrict system performance. Fast disk access is therefore required. Fast access and high capacity almost demand a high performance closed-loop servo system and linear or rotary voice coil motors. In the past these two types of drives represented the two ends of the 5¼" drive spectrum. With the high performance interfaces becoming available, the range of drive possibilities is being stretched.

To drive manufacturers, integrators always seem to want more capacity than they logically need. But many integrators have learned that memory feeds on itself; as you use more you demand more. Choosing a higher capacity than is apparently needed is one way to allow for unforeseen memory demands. Another method of dealing with unforeseen memory demands down the road is to structure the memory subsystem so that drives can be added as needed.

Once the capacity, performance and interface parameters have been defined, products can be evaluated. This evaluation should include cost, reliability and availability. In terms of cost, low-end drives are usually evaluated in terms of cost per drive and high-end drives in terms of cost per megabyte. These days drive manufacturers are in general very quality conscious. But many integrators subject drive samples to a battery of tests. Rough handling is a big enemy of hard disk drives. Shock and vibration testing by prospective

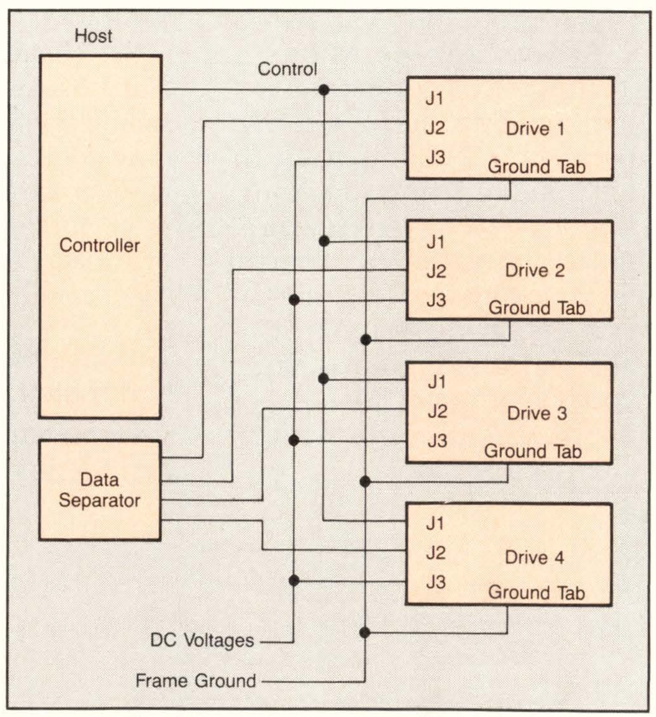


Figure 12: This diagram depicts a typical four-drive ST412HP system. Note that unlike the ESDI, the data separator is not on the drive.

customers is not uncommon. The type of positioner used is a major factor in determining a drive's ability to withstand shock. Balanced rotary positoners absorb shock at the fulcrum. Linear positioners usually must be kept flat and if jarred move easily across the disk surface. Standard rotary positioners will also sweep data out of a disk area.

Availability of the drive and its components must be determined. Integrators should make sure that the drive can be manufactured in the required volume. Multiple platter, half height, sub-micros and exotic technology drives should be especially scrutinized. If thin film heads, plated media or new interface controllers or other specialized electronics are used, a check on their sources is called for. High-end performance or capacity doesn't demand that risks be taken. Fujitsu America is offering an 80 Mbyte 5¼″ with standard heads and six standard platters.

Finally, a look at alternative solutions other than a 5¼″ or other Winchester can be worthwhile. For example, a 3.3 Mbyte 5¼″ floppy disk may be a better answer for some single user systems. Or, at the other extreme, consideration may be given to an 8″ Winchester as a high-end solution.

Winchester Outlook

With Winchester technology evolving so rapidly, one would think that competition from other technologies would be of little concern. However, Winchesters are not the only technology benefitting from the current demand for memory. Flexible disks—some expected to use vertical recording—challenge Winchesters at the low end, while optical memory could make a show of it at the high end. The biggest market is in the middle, however, and there Winchesters seem secure.

Predictions about the future of Winchester disk drives are notoriously inaccurate—even compared to the computer industry in general. Even three years is too long a period to allow meaningful forecasts. In 1978, a year before IBM delivered the first 8″ Winchester, how many predicted that in three years, 61,000 5.25″ Winchesters would be sold? And in 1980, the year Seagate delivered the first 6 Mbyte 5.25″ drives, who predicted that 380 Mbyte 5.25″ drives would be announced in 1983? Plainly, any predictions for 1986 should be taken with a rather large grain of salt.

But although specific predictions of technological developments are impossible, one broad prediction of the Winchester industry is easy. Given Winchester technology's superior potential for improvement, and given the diverse areas of engineering throughout which this potential is scattered, it's certain that Winchester technology will not only keep up with demand, but will actually drive demand in the coming years. □

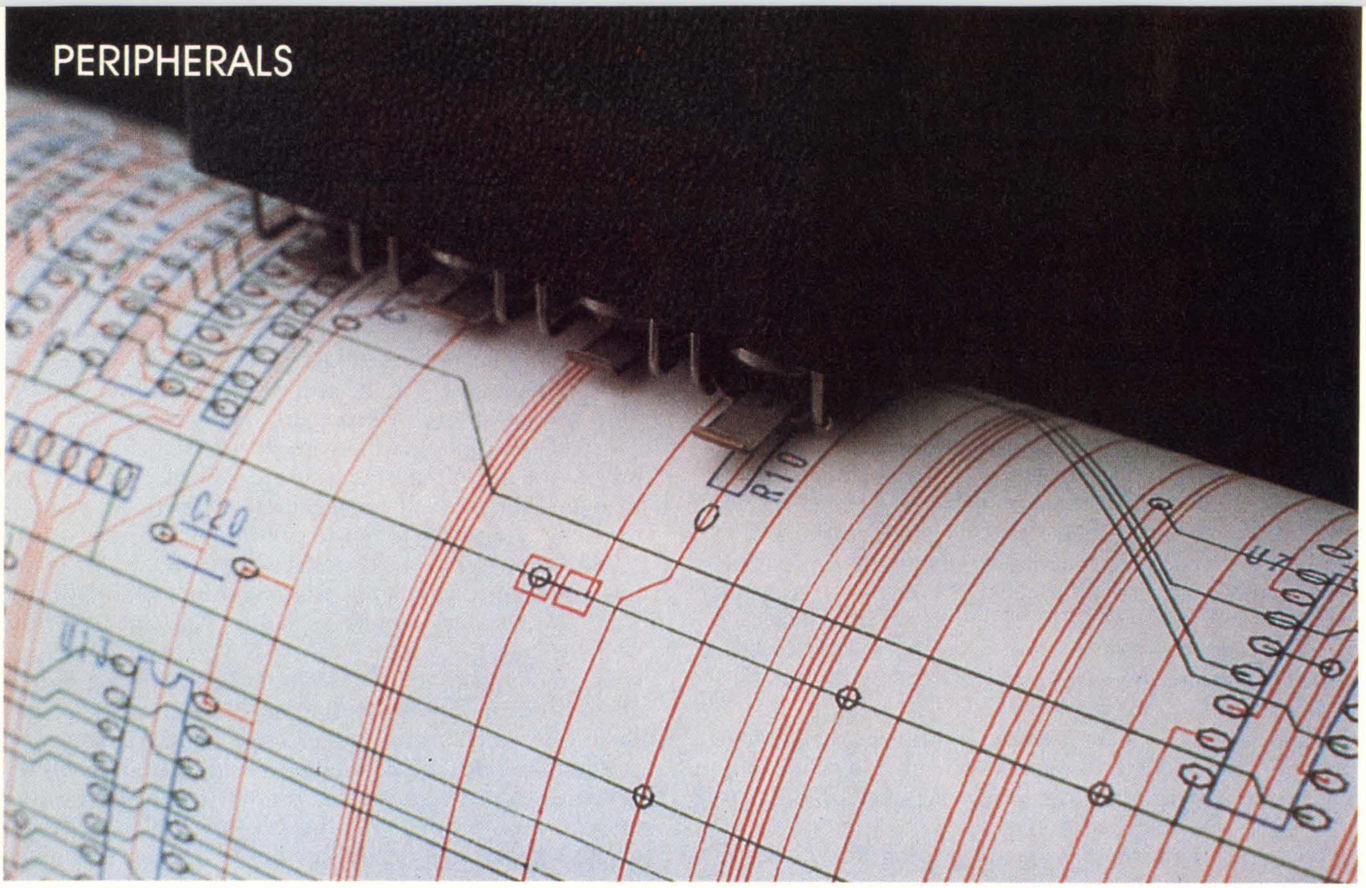


Photo courtesy CalComp

Looking At Plotters

Recent advances in plotter technology have been at a pace rivaling that of computer technology itself.

by Ram Appalaraju

Numerical output from the computer and the need to make that output easily read and understood has been a longstanding problem in the industry. From that need has emerged the graphic output device, i.e. the plotter. Recent advances in this technology have been at a pace rivaling that of computer technology itself.

One variety of hard copy output device primarily used in CAD applications is the digital plotter. Plotters may be classified into pen plotters and electrostatic plotters. The pen plotters may be further divided into drum and flat-bed types.

In the drum type, the pen moves on one axis only and the bi-directional movement on the other axis is achieved by the movement of the drum. In the flat-bed type, the paper is held down by electrostatic or vacuum suction, and pen moves on both axes. The flat-bed type pen plotters suffer from limited paper size, and although the drum type pen plotters have no length restriction on one axis, they offer less resolution than flat-bed plotters.

Electrostatic plotters, on the other hand, use a row of styli instead of a pen, which create lines on statically charged paper, and are preferred in applications which require a large volume of graphic output.

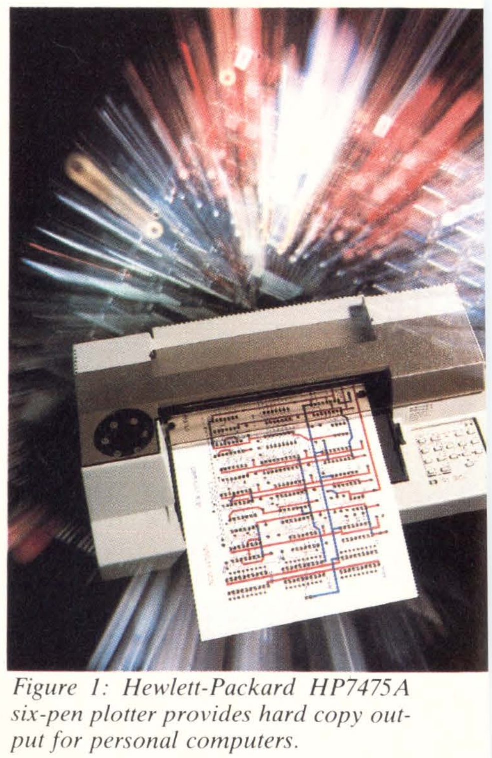


Figure 1: Hewlett-Packard HP7475A six-pen plotter provides hard copy output for personal computers.

The fact that they provide output in raster format, as opposed to the vector format of the pen plotter, makes them faster.

Often, the sophistication of a plotter is determined by its resolution, but in practical terms, the res-

olution is usually considered in terms of its application. Resolution is specified as the reciprocal of the number of addressable points per unit length in each axis. Accordingly, a specification of 0.002″ means that there are 500 addressable points (lines) per inch on each X and Y axis. Sometimes, resolution is classified as both addressable resolution and mechanical resolution. The first is what the user can expect from the plotting equipment and the second is what the equipment actually gives. Further, the term resolution depends on the ability of the electronics in the system to interpolate the data.

For a given application, the disadvantages associated with higher resolution plotters should also be considered. The higher the resolution, the higher the cost. The output string (i.e. the number of bits to define each point to be plotted) in high resolution equipment is high, resulting in the consumption of a large amount of memory.

Many plotters that are available today have been designed with "intelligence". By incorporating a microprocessor in the plotting unit, some of the software burden is taken from the host computer. The microprocessor also executes certain other functions such as changing colors (changing pens), implementing character sets, and arcs and vectors.

The microcomputer in the WX 46XX series from Watanabe Instruments Corp. (Tokyo, Japan) includes a Z80A microprocessor, three 4 Kbyte EPROMs, and two 2114 RAMs. Two 8255's and three LS 368's are mounted as I/O ports. One of the I/O ports is used as an I/O data line from/to the interface board. The other ports are used for the I/O processing such as motor drives, keyboard, etc.

The software in the microprocessor unit controls the pen speed through a WAIT circuit logic. The other functions of the microprocessor unit include establishing handshaking protocol between the interface and I/O ports, D/A conversion circuitry for motor drive, and control paperfeed mechanism, etc. The plotters from Watanabe have different types of interfaces like RS-232-C and GP-IB to make them compatible with various hosts.

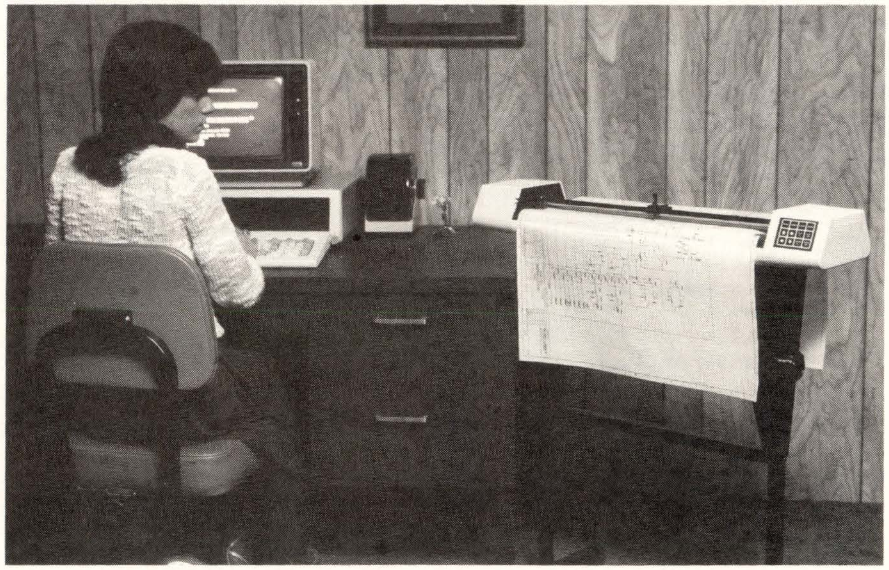


Figure 2: The Houston Instruments DMP-41 drum type pen plotters can accommodate large size papers.

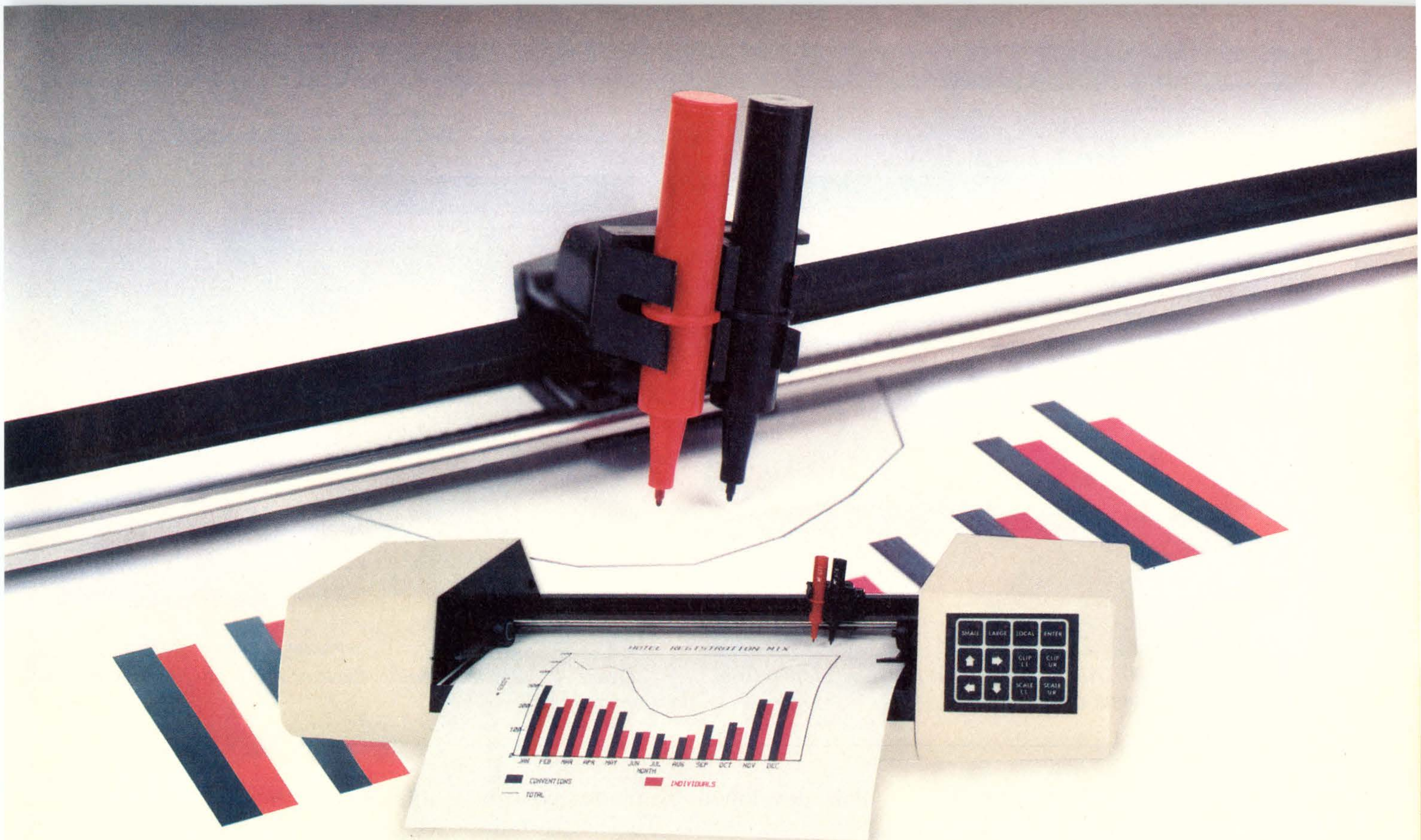
Other similar intelligent plotters are Houston Instruments DMP series; Strobe; Hewlett-Packard 7470, 7475; Benson 1332, 1333; Numonics 5400; and IBM. The XY/750 from IBM is the company's first intelligent graphic output device. The plotter is provided with RS232 and IEEE488 to make it globally compatible. The features of this microprocessor controller plotter include up and down scaling without change of program, offline and online, offscale data handling, and automatic linear interpolation with absolute and relative coordinates.

Houston Instrument, a division of Bausch and Lomb, has various models of dumb plotters on the market. The DMP-29 is the company's largest flat-bed model. The DMP-41 and DMP-42 differ only in the size of paper used. The features of the plotters include a user addressable resolution of 0.001″, 0.005″ or 0.1″. The addressable resolution allows GRAPH mode addressing of the plotter on a matrix of 4096X by 4096Y points. This increases the address resolution by a factor of four over the standard 1024X × 1024Y. This resolution requires two additional bits be added to each axis address, bringing the total to 12 bits; therefore an "extra" byte must be inserted in the vector addressing string.

The CalComp plotters from California Computers (Anaheim, CA) have designed a hybrid type of plotter known as a belt-bed. Their model 945/965 provides graphic output up to an acceleration of 4g and diagonal pen positioning speeds up to 42″/sec. The plotter incorporates a drum that drives a moveable belt which holds precut drafting media. The pen cartridge rides on a stationary beam. All the inking takes place over the drum portion of the plotter. The model 945/965 has eight vector plot movements. The other standard features of the plotter include a message display, selectable electronic limits, plot parameter inputs, re-settable plot-time meters, and plot size counters.

Hewlett-Packard's HP 7475 is the company's latest 6 pen plotter. The plotter can be specified by two interfaces, HPIB (HP's enhanced version of the IEEE-488 bus) or RS-232-C.

Of late, some manufacturers have been involved in more than one type of plotter technology. Benson, for example, has made drum, flat-bed and electrostatic types. The latest in the drum type series are the 1332/33 members. These plotters incorporate DC servomo-



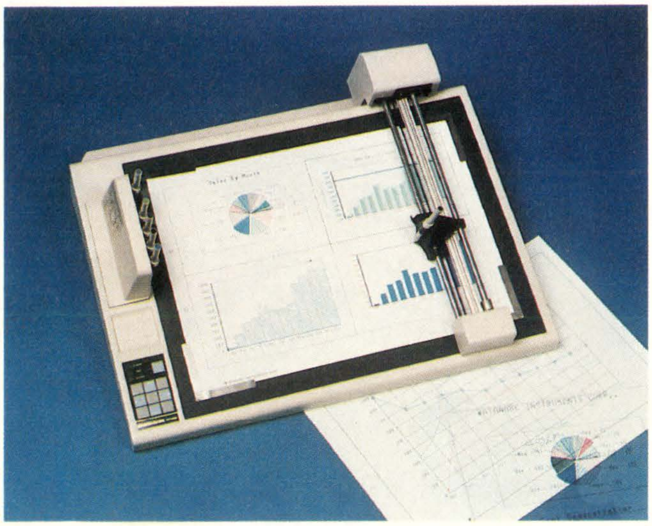


Figure 3: MP-1000: An intelligent flat-bed pen plotter from Watanabe Instruments Corporation.

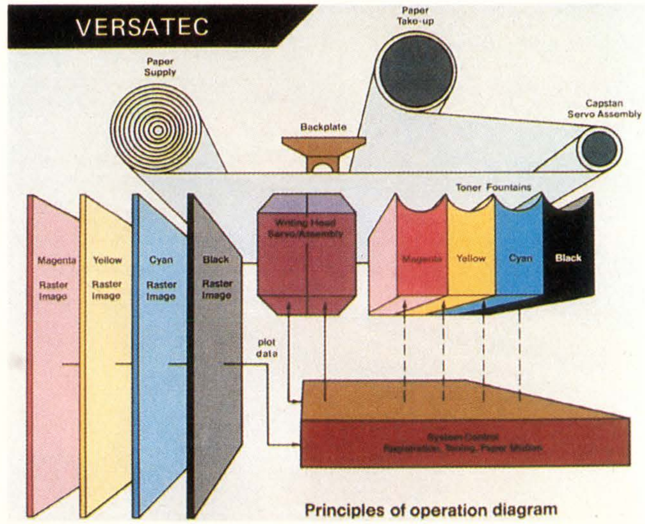


Figure 4: Versatec's color electrostatic plotter—principle of operation.

tors for high speed plotting. One prominent feature is the hardware character generation.

Benson's 9300/9400 electrostatic plotters produce graphic images on paper or film by applying a toner consisting of carbon particles in suspension to a charged electrostatic pattern created on the paper. The charged dots are created by applying a high voltage charge to a row of conducting metal styli. Furthermore, the technology uses quadrascan technique. This technique allows overlapping the charged areas from each stylus by arranging the styli in an offset pattern. Four styli are arranged such that, by delaying input data, the styli will overlap charged areas and produce a solid print line.

The paper or film of the 9300/9400 plotter is pulled past the writing styli in high-speed incremental steps by the drive roller. The appropriate bits in the plotter input turn on the styli in the first row of the writing head. The remaining bits are delayed in the shift registers. The process continues through rows of styli and allows stylus overlap of 50% as required by the plot. The drive roller is incremented by a step motor driven in microstep mode. The charged pattern is produced by a short pulse of 600–800 V applied between segmented backplate and styli. The thousands of styli are driven by multiplexed signals developed by plotter control electronic circuits. The electrostatic pattern intensity is sufficiently strong that it will last for hours if necessary. A suspension of very fine carbon particles in a dielectric fluid is applied to the paper surface. The carbon particles are attracted to the charged areas and remain on the surface of the paper. The paper is passed over a drying roller, which removes the toner liquid by capillary action.

The whole process appears to be quite complex. The 9300/9400 series houses Intel's 8085 which performs the plotter control functions. In order to improve the resolution of electrostatic plotters, recent models are provided with a suprascan device. Of these, Benson's provides a resolution of 400 dots per inch.

The first electrostatic plotter on the market was from Versatec. To obtain color, the plotter repeatedly backs up the paper and runs it under the print head and toner, once for each primary pigment. The primary pigments are black, cyan, magenta, and yellow. Over 400 colors are possible by interspersing dots of these primary colors.

Versatec's V-80 plotter plots complex 11″ × 8½″ drawings in 8.5 seconds with a resolution of 200 dots per inch. The system can hold up to a gallon of toner and the toner concentrate can be added by a microprocessor controlled push button that prevents inadvertent overconcentrating. A unique feature of the V-80 is the plotter's ability to handle papers with a width of 72″.

At present, technology is more advanced in pen plotters than electrostatic. The microcomputer boom is popularizing low-cost plotters that are becoming compact and portable. However, for applications which require large drawings or fast plotting, electrostatic plotters are the automatic choice. The difficulty associated with design of plotters today is to accommodate papers of large dimensions, a problem which becomes more prominent if the paper is to move back and forth.

Many manufacturers have started R&D efforts into ink jet technology. However, the technology's exorbitant price has kept it from becoming very popular.

The intelligence of plotters is on the increase. A considerable number of functions are being implemented by the plotters without the help of the host CPU. Furthermore, the user interaction is being lessened. The rapidity with which prices are falling has made the plotter an indispensable item in a CAD workstation. Large arrays of numeric output which are a result of scientific simulations make a lot more sense when they are plotted graphically. Although hardcopy devices have proved successful, their full potential is yet to be realized. □

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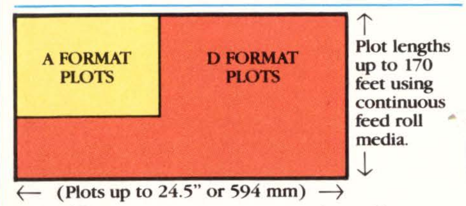

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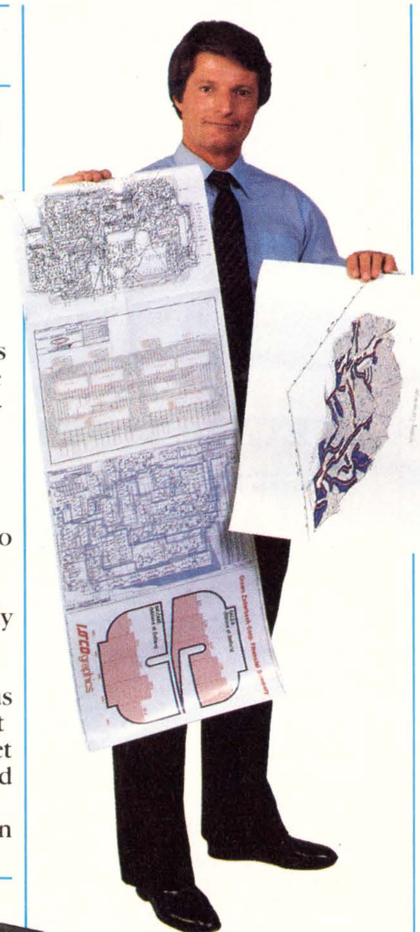

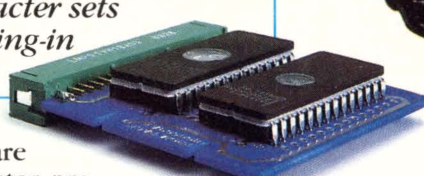

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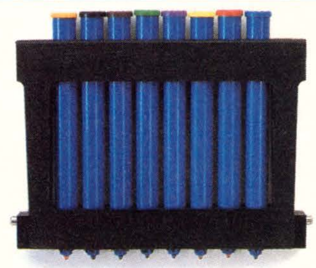

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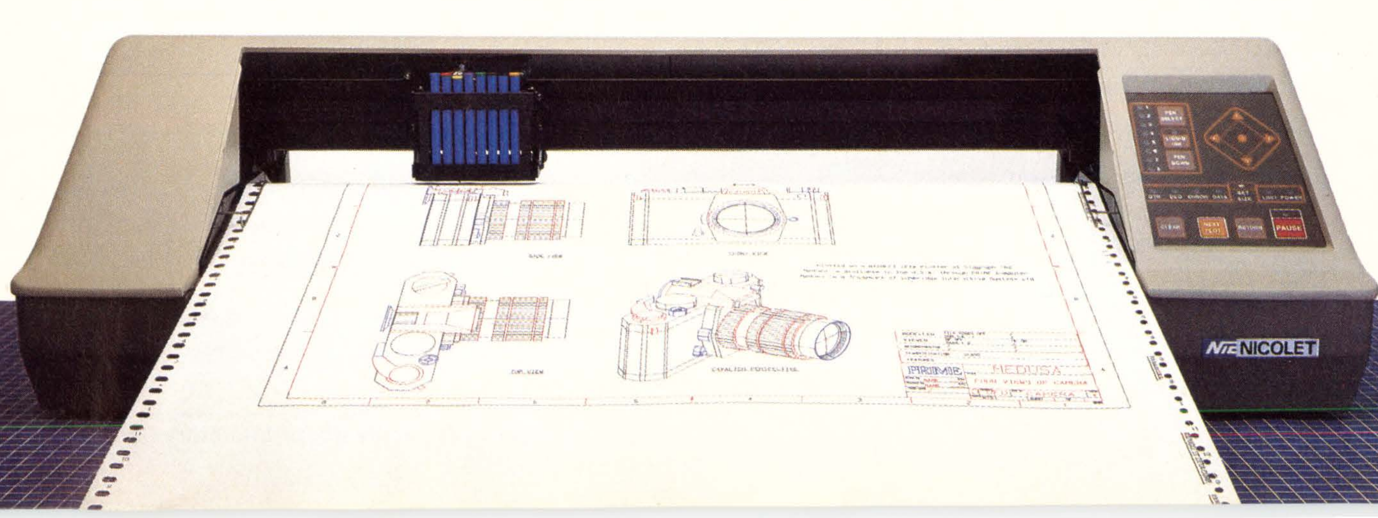

℞ FOR HEALTH

By Lawrence Lee, MD

Dr. Lee is a leading Southern California Internist, specializing in cardiology. He is a co-founder and board chairman of LH Research, Inc. This column is presented as a public service for better understanding of topical medical problems and possible solutions.

HERPES!

Some Facts You Should Know.

This is the first in a series of columns by Dr. Lee on medical subjects of current interest, although perhaps not fully understood, by the public. If you have a question, please write Dr. Lee at LH Research, Tustin, CA 92680.

Did you know, for instance, that there are actually **four** types of Herpes virus that infect humans. They include Herpes Simplex (Types I and II), Varicella Zoster (chickenpox/shingles), Cytomegalo virus, and Epstein-Barr virus (infectious mononucleosis).

What is a virus?

A virus is a group of minute, infectious agents **not** seen in a light microscope, and only visible in an electron microscope. A virus is characterized by not having its own metabolism, and only being able to propagate (multiply) in the cells of a living host. Thus, a virus cannot propagate in food, water or any other "non-living" host.

Herpes used to mean **any** inflammatory skin disease characterized by a cluster of small vescicles (blisters less than 1 cm. in diameter). The most commonly known type of this disease is Herpes Simplex, which comes in two types. Type I (HSV-1) infects mucous membranes of the mouth, the skin around the lips and mouth, the eyes, and other skin areas of the body above the waist.

Herpes Simplex Type II (HSV-2) usually infects the genitalia, rectal area and other skin areas below the waist. This is the widely publicized type of Herpes currently receiving national media attention.

In future columns, I will discuss the details of this and other types of Herpes virus, the methods of avoidance and potential cures.

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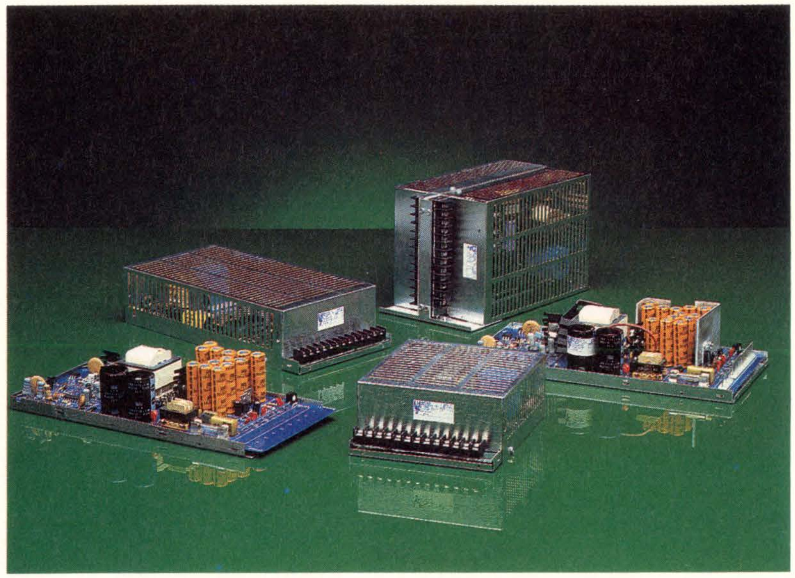

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Interfacing The Z-Bus Peripherals

The Z-Bus peripherals can interface easily to most multiplexed address/data bus structures, while the Z8500 peripherals interface to most non-multiplexed address/data bus structures.

by John D. Kennedy

It has always been customary for designers of microprocessor-based products to look to their CPU suppliers to provide them with the necessary peripheral support components. This is because peripherals have traditionally been designed as members of particular component families and have been bound to parent CPUs. Zilog, Inc. has an array of third-generation peripherals which can free designers from this restriction: the Z8000 peripherals (or Z-Bus peripherals) can interface easily to most multiplexed address/data bus structures, while the Z8500 peripherals (or Universal peripherals) interface to most non-multiplexed address/data bus structures.

The following is a discussion of the Z-Bus and other multiplexed bus structures, along with techniques for interfacing the Z-Bus peripherals. A detailed example is given using Intel's 8086/8088 CPU. Software sequences are also included to provide examples of how to initialize the Z-Bus peripherals for some simple applications.

At the heart of the Z-Bus is a set of multiplexed address/data lines and the signals that control these lines. Multiplexing data and addresses onto the same lines makes more efficient use of pins and facilitates expansion of the number of data and address bits. Multiplexing also allows straightforward addressing of a peripheral's internal registers, which greatly simplifies I/O programming.

The Z-Bus uses a daisy-chained priority mechanism to resolve interrupt and resource requests, thus allowing distributed control of the bus and eliminating the need for separate priority controllers. In an interrupt daisy-chain, for example, the peripherals are connected together via their Interrupt Enable Input (IEI) and Interrupt Enable Output (IEO) pins. The interrupt sources within a device are similarly chained together, with the overall effect being a daisy-chain connecting all the interrupt sources. The daisy chain allows higher priority interrupt sources to preempt lower priority sources and, in the case of simultaneous interrupt requests, determines which request will be acknowledged.

The Zilog microprocessors that can act as master of the Z-Bus include: Z8000, Z800 (16-bit bus ver-

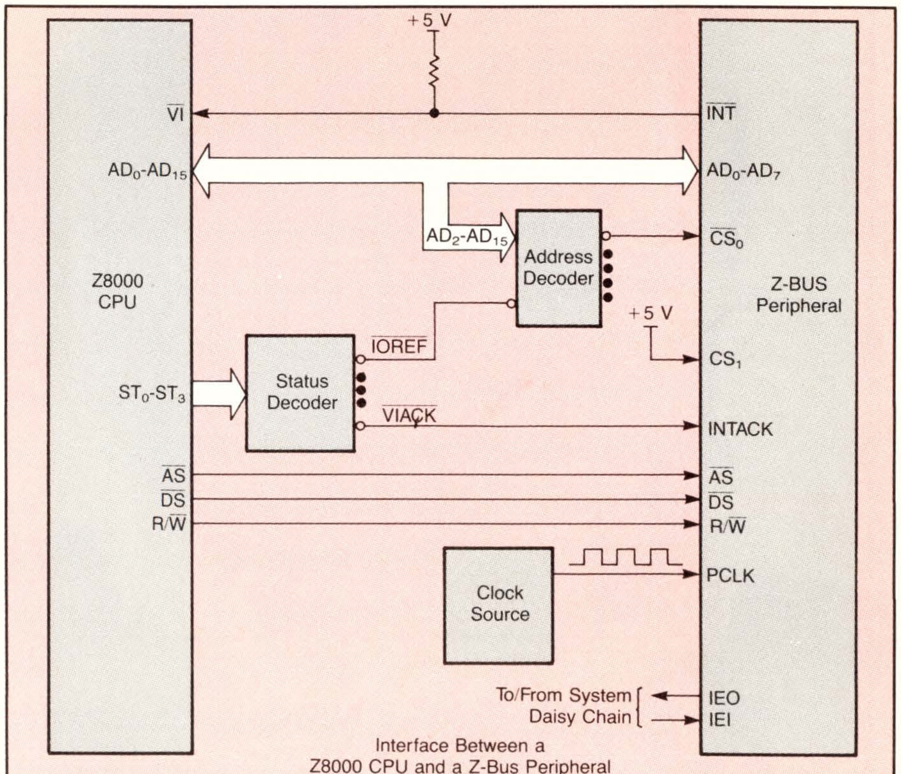
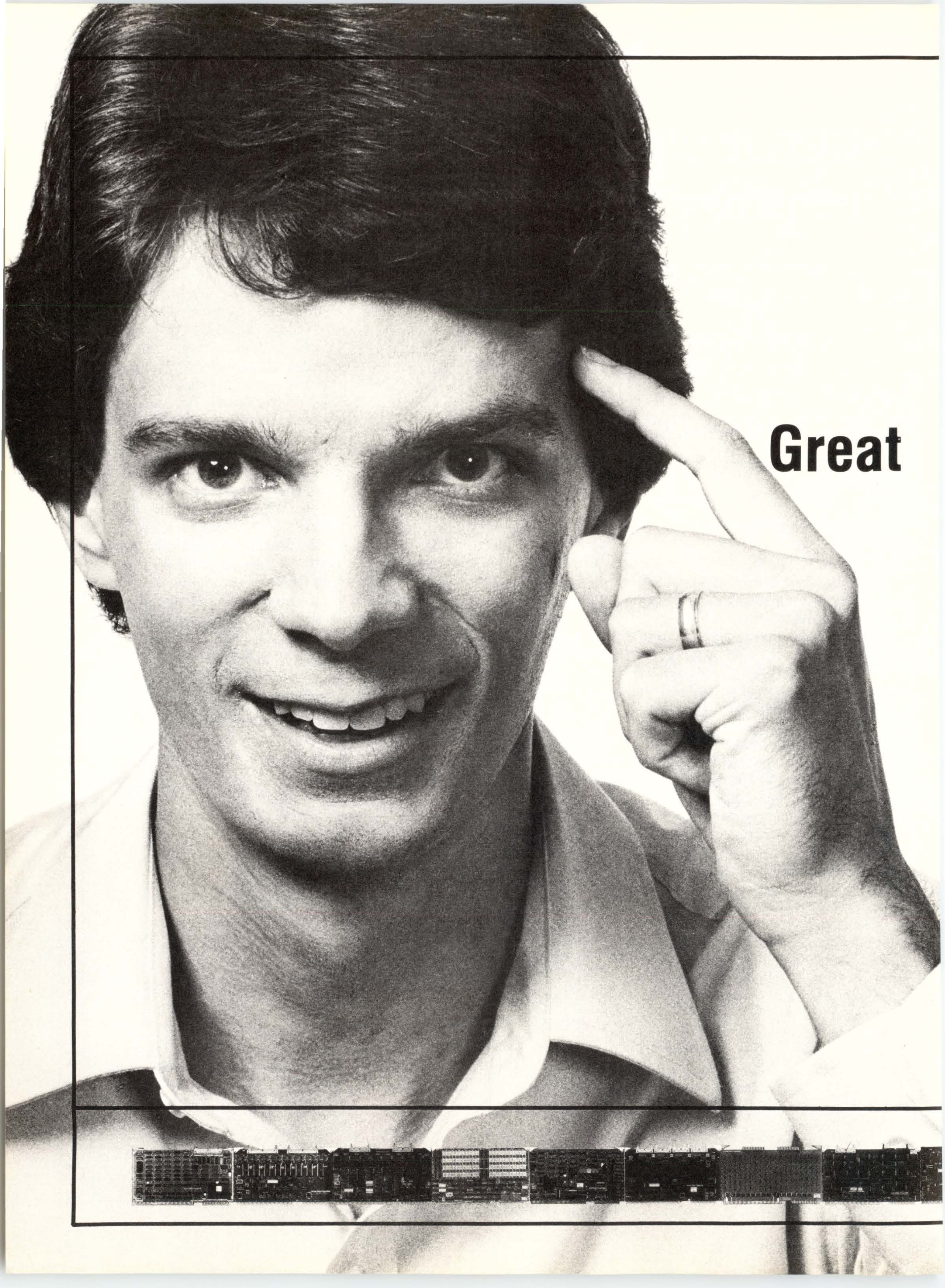


Figure 1: Interface between a Z8000 CPU and a Z-Bus peripheral.

John Kennedy is an Applications Engineer with Zilog Corp., 1315 Dell Ave., Campbell, CA 95008.


Great

sion), and Z8. The Z-Bus peripherals include:

- •Z8016 DTC Direct Memory Access Transfer Controller
- •Z8030 Z-SCC Serial Communications controller
- •Z8031 Z-ASCC Asynchronous Serial Communications Contoller
- •Z8036 Z-CIO Counter/Timer and Parallel I/O Unit
- •Z8038 Z-FIO FIFO Input/Output Interface Unit
- •Z8060 FIFO Buffer Unit and Z-FIO Expander
- •Z8070 APU Arithmetic Processing Unit
- •Z8090 Z-UPC Universal Peripheral Controller

Figure 1 shows an interface between a Z8000 CPU and a Z-Bus peripheral, while **Table 1** gives descriptions of each signal involved in the interface.

Interfacing Non-Zilog CPUs

Among the non-Zilog CPUs that can easily interface to the Z-Bus peripherals are: 8085, 8086, 8088, and NS 16032. The Z-Bus peripherals lend themselves conveniently to designs based on these processors because of the multiplexed address/data bus architecture and the fact that they allow the CPU direct access to all of their data and control registers. Futhermore, the Z-Bus peripherals are asynchronous in the sense that they do not need to be synchronized with the CPU clock; all timing information is provided by the control signals. Of course, the designer must provide the interface logic but, as will be shown, the amount of external hardware is minimal. **Table 2** associates the Z8000 control signals with the analogous control signals of the non-Zilog CPUs.

In the simplest case (where the CPU must merely read from and write to the peripheral), the only bus cycles that need to be considered are the I/O Read and I/O Write bus cycles. The peripherals need an Address Strobe ($\overline{AS}$) to tell them when the address and the state of $\overline{CS_0}$ are valid, a Data Strobe ($\overline{DS}$) to tell them when the bus contains valid data (write) or when to drive data on to the bus (read), and a Read/Write (R/$\overline{W}$) signal to tell them whether the present transaction is a read or write.

All of the processors in **Table 2** generate a signal that is analogous to the Z-Bus $\overline{AS}$. The NS 16032 generates the $\overline{ADS}$ signal, which has the same polarity as AS, while the 8085, 8086, and 8088 generate the ALE (Address Latch Enable) signal which must be inverted if it is to drive $\overline{AS}$. Similarly, all of the processors generate signals from which the Z-Bus $\overline{DS}$ can be derived. If DS is not directly available then it can easily be generated using external logic. For example, **Figure 2** (in the hardware example) shows how the $\overline{RD}$ (Read) and $\overline{WR}$ (Write) signals of the 8085, 8086, and 8088 can be used to control $\overline{DS}$. The Z-Bus R/$\overline{W}$ signal can be driven by DDIN of the NS 16032 or by an inversion of DT/$\overline{R}$ of the 8086/8088. Since the 8085 does not generate a DT/$\overline{R}$ signal, it requires an external flip-flop which is set when ALE goes high and reset when $\overline{WR}$ goes low.

In the case of a system with a daisy-chain controlled interrupt scheme, the designer must consider the Interrupt Acknowledge bus cycle. The Z-Bus peripherals interpret the present bus cycle as an Interrupt Acknowledge cycle whenever the $\overline{INTACK}$ input is latched low with the rising edge of AS. During the Interrupt Acknowledge cycle, the daisy-chain determines which interrupt source is being acknowledged in the following way: Any interrupt source that has an interrupt pending and is not masked from the chain will hold its IEO low. Similarly, sources that are currently under service (i.e. have their IUS bit set) will also hold their IEO low. All other interrupt sources make IEO follow IEI. The result is that only the highest priority, unmasked source will have a high IEI input; only this interrupt source will be acknowledged. The hardware example that follows shows how the Z-Bus interrupt ac-

$\overline{INT}$	Interrupt Request (output, open-drain, active Low). This signal is pulled low when the peripheral requests an interrupt. In **Figure 1** it is connected to the VI (Vectored Interrupt) input of the Z8000.
$AD_0 - AD_{15}$	Z-Bus Address/Data lines (bidirectional/3-state). These multiplexed Address/Data lines are used for transfers between the CPU and the peripheral.
$\overline{CS_0}$ and CS_1	Chip Select 0 (input, active Low) and Chip Select 1 (input, active High). CS is latched with the rising edge of AS while CS is unlatched. In **Figure 1**, CS is tied high and CS is generated with the address decode logic.
$\overline{INTACK}$	Interrupt Acknowledge (input, active Low). This signal indicates to the peripheral that an Interrupt Acknowledge cycle is in progress. In **Figure 1**, INTACK is driven by the VIACK (Vectored Interrupt Acknowledge) output of the status decoder.
$\overline{AS}$	Address Strobe (input, active Low). The Z-Bus peripherals sample addresses, INTACK, and CS while AS is low.
$\overline{DS}$	Data Strobe (input, active Low). Data strobe provides timing for the transfer of data into or out of the Z-Bus peripherals.
R/$\overline{W}$	Read/Write (input). R/W indicates that the CPU is performing a read (High) or a write (Low) operation.
PCLK	Peripheral Clock (input, TTL-compatible). The maximum frequency is 4 or 6 MHz depending on the grade of the component, and it can be asynchronous to the system clock.

Table 1: The Z-Bus signals. A hardware reset of a Z-Bus peripheral is performed by drawing AS and DS low simultaneously.

Z8000 CONTROL SIGNALS	ANALOGOUS CONTROL SIGNALS OF NON-ZILOG CPUs 8085/8086/8088	NS 16032
$\overline{AS}$	ALE (Address Latch Enable)	$\overline{ADS}$ (Address Strobe)
$\overline{DS}$	$\overline{RD}$, $\overline{WR}$ (Read, Write Strobes)	$\overline{DS}$/ $\overline{FLT}$ (Data Strobe/Float)
R/$\overline{W}$	DT/$\overline{R}$ (Data Transmit/Receive)[1]	DDIN (Data Direction In)
$\overline{V1}$	INTR (Interrupt)	$\overline{INT}$ (Interrupt)
$\overline{IOREF}$[2] (I/O Reference)	IO/$\overline{M}$ (Input-Output/Memory)[3]	—
$\overline{VIACK}$[2]	$\overline{INTA}$ (Interrupt Acknowledge)	IAM (Interrupt Acknowledge, Master) [2]

Note:
1. DT/$\overline{R}$ is not available on the 8085.
2. Must be decoded from CPU status.
3. M/$\overline{IO}$ on 8086.

Table 2: Z8000 Control Signals and Analogous Control Signals of non-Zilog CPUs.

knowledge protocol can be made compatible with the 8086/8088.

A Hardware Example

The Z-Bus peripherals are easily integrated into, and can satisfy many of the peripheral support requirements of a typical 8086/8088-based system. **Figure 2** shows the interface logic that links the 8086/8088 to Zilog's Serial Communications Controller (Z8030 Z-SCC), Counter/Timer—Parallel I/O Unit (Z8036 Z-CIO), and FIFO I/O Controller (Z8038 Z-FIO). The 8086/8088 is assumed to be running at 5 MHz in the Minimum Mode.

Bus Timing. Each bus cycle begins with an ALE pulse, which is inverted to become $\overline{AS}$. The trailing edge of this strobe latches the address, as well as the states of $\overline{CS_O}$ and $\overline{INTACK}$ within the peripheral. $\overline{DS}$ is then used to gate data to (write) or from (read) the selected register, provided that an active $\overline{CS_O}$ has been latched. The important timing parameters to consider are the Data Strobe Width and the Write Data Setup Time to $\overline{DS}$.

The Z-Bus peripherals have a minimum requirement for the width of Data Strobe: 390 ns for the 4 MHz peripherals, and 250 ns for the 6 MHz peripherals. On read cycles, $\overline{DS}$ has the same width as $\overline{RD}$ which is at least 325 + 200N_W ns, where N_W is the number of wait states in the bus cycle. On write cycles, the D flip-flop shortens this minimum width to 210 + 299N_W ns. It is clear that one wait state (T_W) in the bus cycle ensures a sufficiently wide Data Strobe for both types of bus cycles.

The Z-Bus specifications also require that the CPU put valid data on the bus prior to the falling edge of $\overline{DS}$ on write cycles. The minimum setup time is 30 ns for the 4 MHz devices, and 20 ns for the 6 MHz devices. The D flip-flop guarantees this setup time by delaying the falling edge of $\overline{WR}$ until the next falling edge of SYS CLK (**Figures 3 and 4** are the Read and Write cycle timing diagrams).

Wait State Generation. Since 8086/8088-based systems typically use an 8284 Clock Chip, which synchronizes the CPU's READY input to the system clock, the task of designing a wait state generator reduces to designing a circuit that controls RDY1 of the 8284 (RDY2 is assumed to be grounded).

For the processor to enter a wait state after T_3, the RDY1 input must be low during the falling edge of SYS CLK at the end of T. Then, for the processor to enter T_4 after the wait state, RDY1 must be high during the next falling edge of SYS CLK. To make sure that these levels are valid within the required set-

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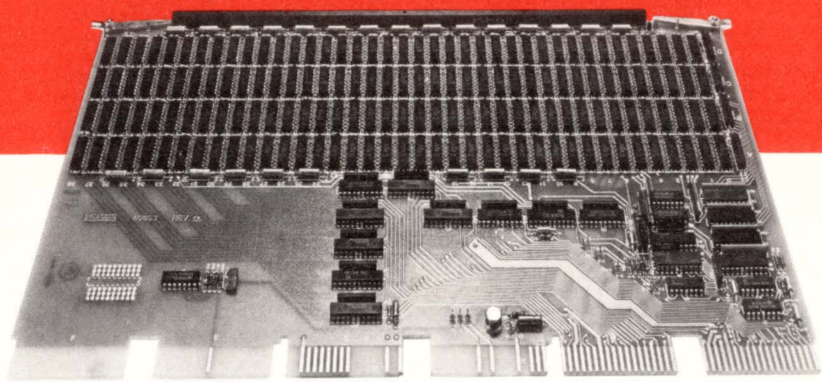

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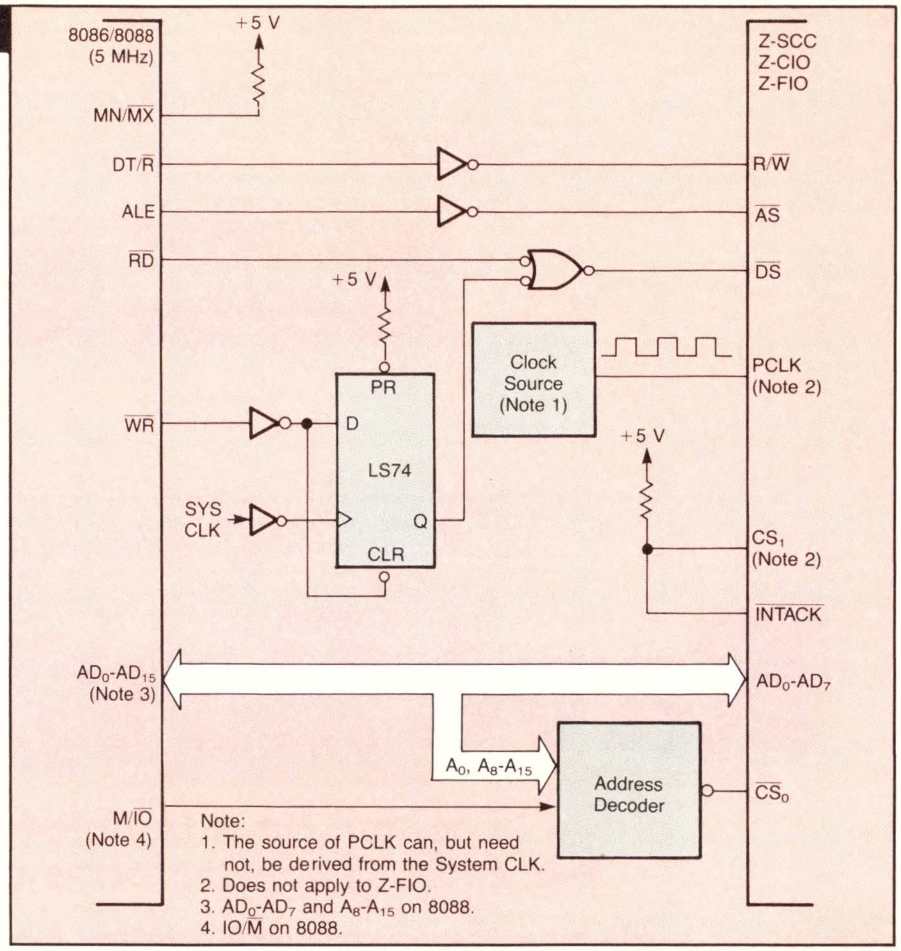

Figure 2: Interface Logic.

up time, the single wait state generator should toggle RDY1 using the clock edges that precede the sampling edges. The circuit in **Figure 5** performs this function and generates a single wait state whenever one of the $\overline{CS_O}$ inputs is active.

Though read/write operations require only one wait state, Interrupt Acknowledge transactions require multiple wait states to allow for daisy-chain settling, which is explained in the next section. In the preceding discussion of the single wait state generator, we established that RDY1 must be high at the end of T_3 for the processor to enter T_4 after the wait state. In general, the 8086/8088 will continue to insert wait states until RDY1 is driven high, and the number of wait states is equal to the number of clock cycles that RDY1 is held low after the rising clock edge in T_2.

A convenient way to implement a multiple wait state generator is to use a serial shift register such as an 74LS164. **Figure 6** shows a wait state generator that requests one wait state on Read/Write cycles, and up to seven wait states on Interrupt Acknowledge cycles. When $\overline{RD}$, $\overline{WR}$, or $\overline{INTA}$ goes active, the 74LS164 is taken out of the clear state and logic "ones" are allowed to shift sequentially from Q_A to Q_H. On Read/Write cycles, RDY1 is held low until the leading "one" appears at Q_B, and on Interrupt Acknowledge cycles, RDY1 is held low until the leading "one" appears at Q_H. The next section shows how $\overline{INTACK}$ can be generated and discusses the complete interrupt interface.

Interrupts. In **Figure 1** the $\overline{INTACK}$ input to the Z-Bus peripheral is tied high. This does not mean that the peripheral can't interrupt the CPU; it just means that it won't respond to the CPU's interrupt acknowledge. The designer can, however, implement a circuit that will drive $\overline{INTACK}$, and allow the 8086/8088 to properly acknowledge the interrupts of the Z-Bus peripherals.

Recall that a Z-Bus interrupt daisy-chain resolves interrupt priority

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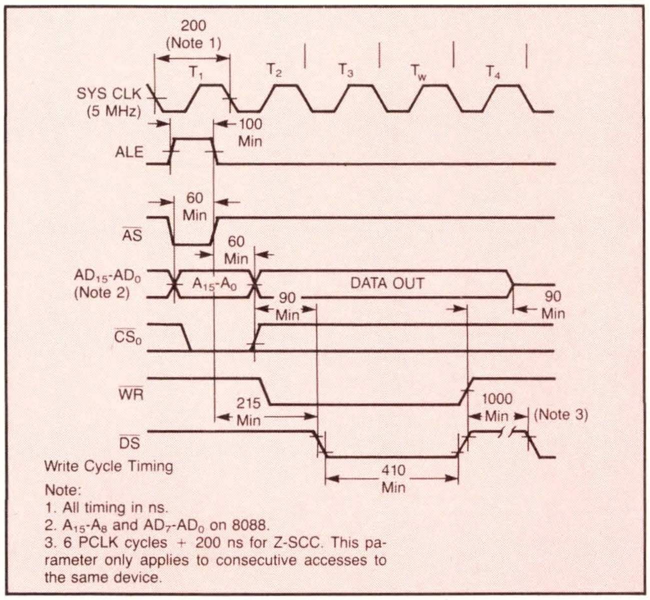

Figure 3: Read and Write cycle timing.

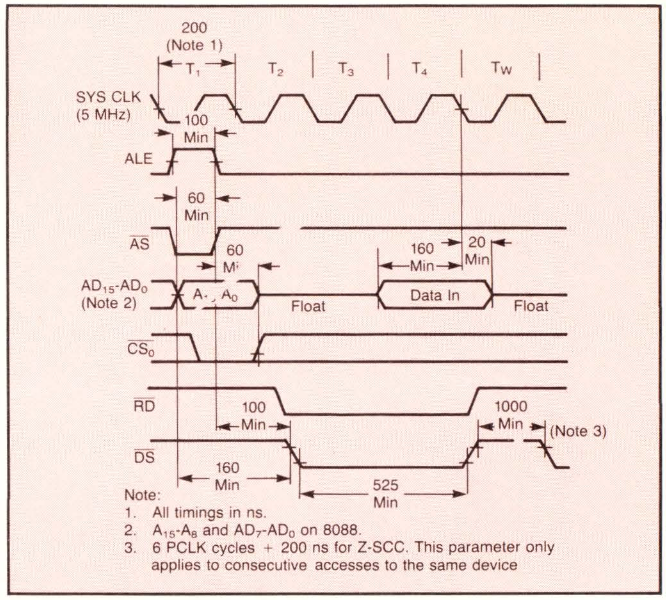

Figure 4: Read and Write cycle timing.

by way of a signal that propagates from high priority interrupt sources to low priority sources during $\overline{\mathrm{INTACK}}$ cycles. To make sure that this daisy-chain signal has settled by the time $\overline{\mathrm{DS}}$ gates the vector onto the bus, the Z-Bus peripherals require a sufficient delay between the rising edge of $\overline{\mathrm{AS}}$ and the falling edge of $\overline{\mathrm{DS}}$ during $\overline{\mathrm{INTACK}}$ cycles. For a particular daisy-chain, the delay is T_{high} for the highest priority device, plus T_{low} for the lowest priority device, plus T_{mid} for each device in between.

The 8086/8088 Interrupt Acknowledge (INTA) sequence consists of two identical INTA bus cycles with two clock cycles in-between. In both cycles, $\overline{\mathrm{RD}}$ and $\overline{\mathrm{WR}}$ remain inactive while an $\overline{\mathrm{INTA}}$ strobe is issued with the same timing of a $\overline{\mathrm{WR}}$ strobe. The 8086/8088 requires an interrupt vector to appear on AD_0—AD_7 at least 30 ns before the beginning of T_4 in the second INTA cycle. This protocol is normally used to read vectors from an 8259 Interrupt Controller but it can easily be adapted to the Z-Bus Interrupt Acknowledge protocol.

The first function of the Interrupt Acknowledge circuit is to generate the Z-Bus $\overline{\mathrm{INTACK}}$ signal from $\overline{\mathrm{INTA}}$ of the 8086/8088. Since $\overline{\mathrm{INTA}}$ goes active after ALE has terminated, the peripherals do not latch an active $\overline{\mathrm{INTACK}}$ during the first INTA cycle. However, if the rising edge of $\overline{\mathrm{INTA}}$ is used to toggle $\overline{\mathrm{INTACK}}$, then an active $\overline{\mathrm{INTACK}}$ is latched with the rising edge of $\overline{\mathrm{AS}}$ in the second INTA cycle. Thus a rising-edge triggered toggle flip-flop can be used to gen-

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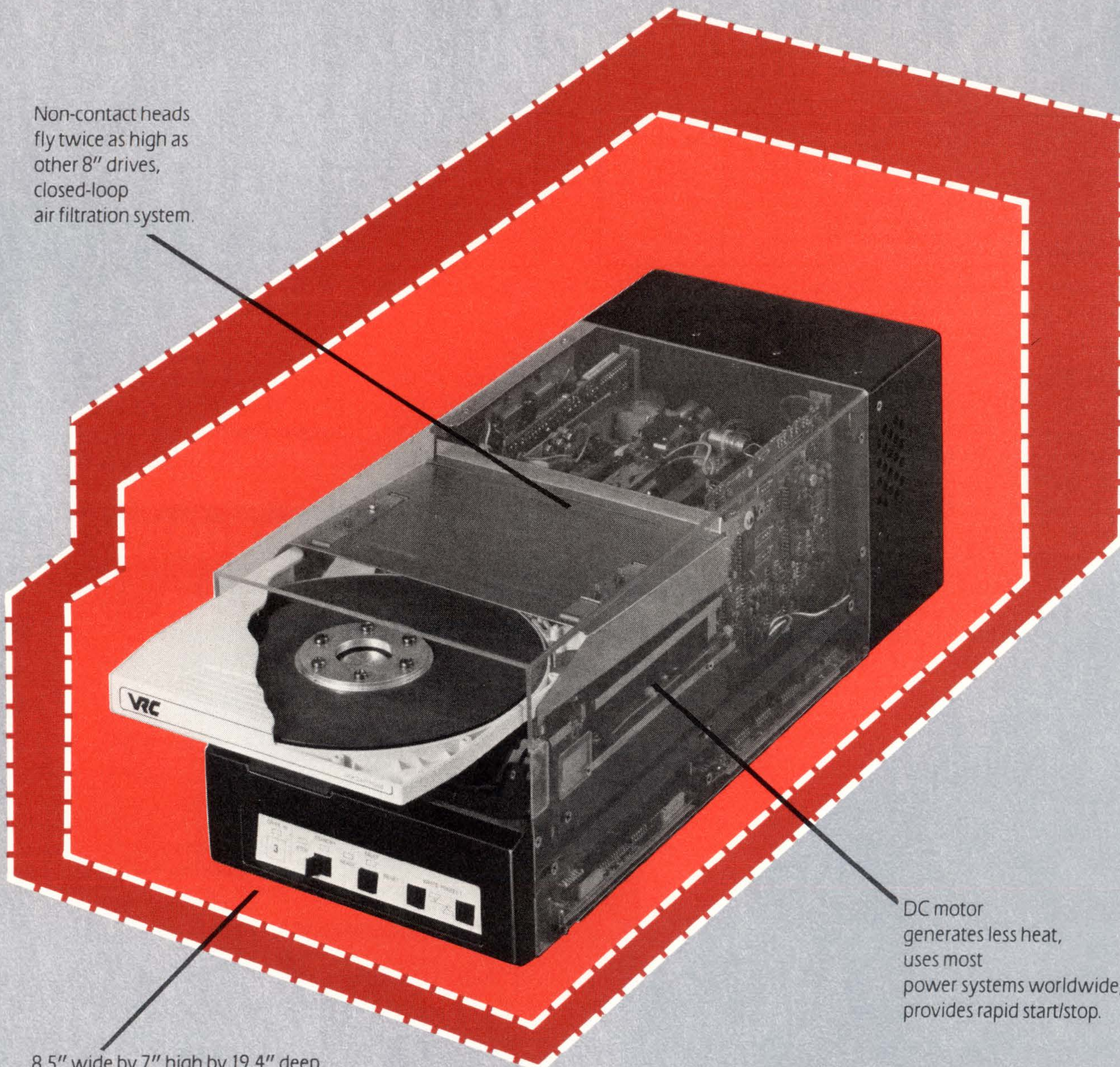

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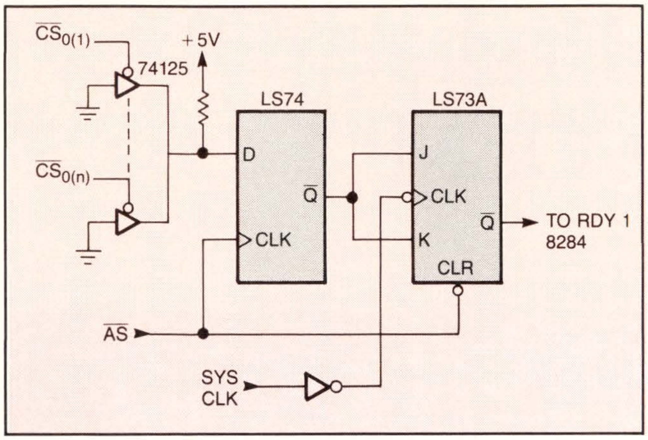
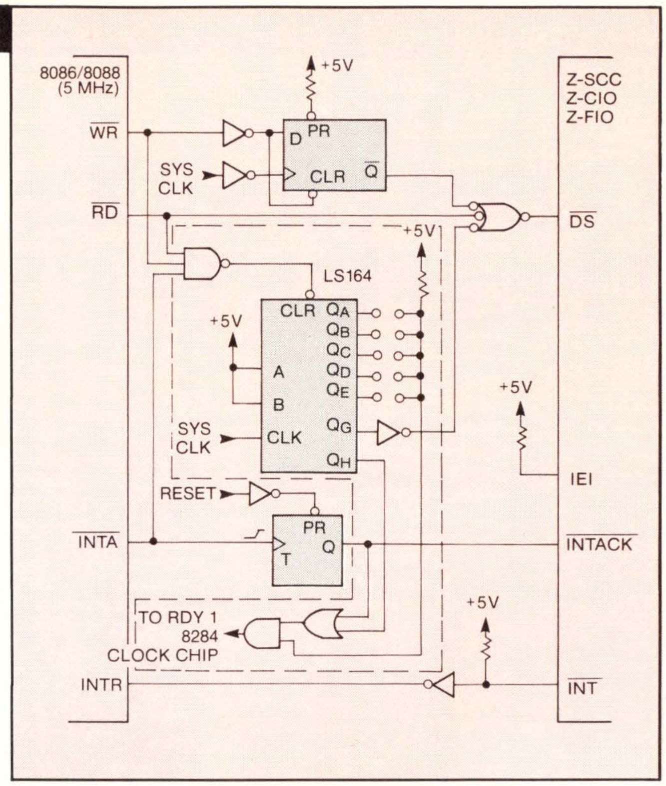


▲*Figure 5: Single wait state generator.*



▶*Figure 6: Interrupt acknowledge circuit (dotted line shows wait state generator).*

erate $\overline{\text{INTACK}}$ (see **Figure 6**).

The next function of the Interrupt Acknowledge circuit can be broken down into three operations: first, it must cause the CPU to enter a series of wait states after T_3 in the second $\overline{\text{INTA}}$ cycle; then it must activate $\overline{\text{DS}}$ after a sufficient daisy-chain settling time; lastly, it must bring the CPU out of the wait state condition when the vector is available on the bus.

The multiple wait state generator can be used to perform each of these operations. While $\overline{\text{INTACK}}$ is high it operates normally; the number of wait states it requests is determined by the positioning of the jumper on the Q outputs. When $\overline{\text{INTACK}}$ goes low, it operates as follows: the next activation of $\overline{\text{INTA}}$ brings the shift register out of the clear state, and logic "ones" shift into Q until they fill the entire register. When the leading "one" appears at Q_6, $\overline{\text{DS}}$ is driven low; when it appears at Q_H, the CPU is taken out of the wait state condition.

This arrangement takes advantage of the full length of the shift register and provides a daisy-chain settling time of more than 1300 ns, which allows the implementation of a chain with as many as seven Z-Bus devices.

Hardware reset. The designer may want to incorporate a hardware reset in the interface design. This can be accomplished with two NOR gates. The NOR gates allow a system RESET signal to pull $\overline{\text{AS}}$ and $\overline{\text{DS}}$ low simultaneously, and hence put the peripheral in a reset state. A hardware reset is not necessary, however, because all of the peripherals are equipped with software reset commands.

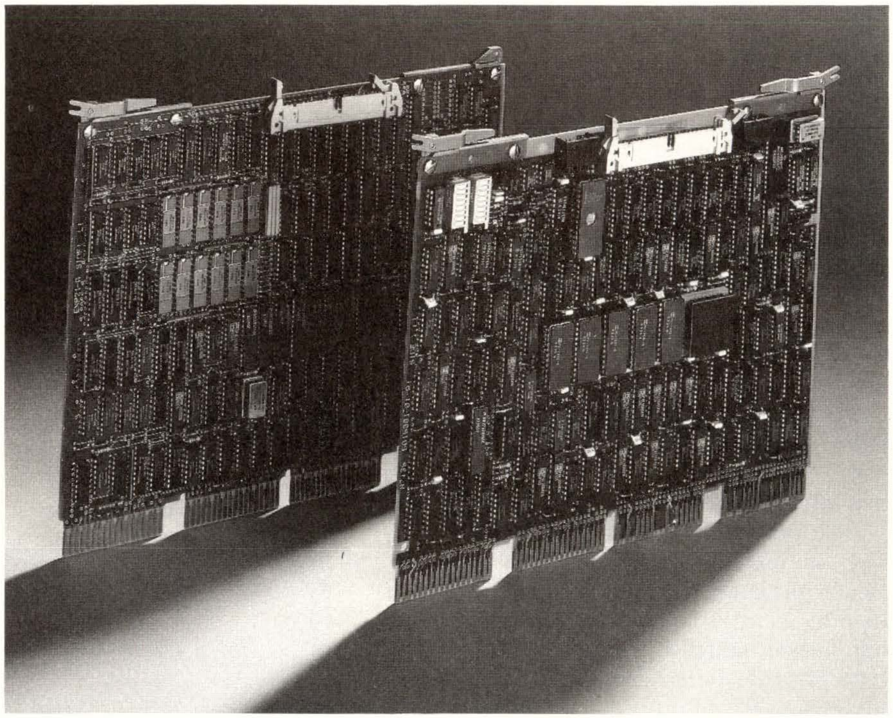
Designers need not be limited to peripherals offered by their CPU suppliers. Zilog's Z-Bus peripherals are designed with the flexibility to interface to most multiplexed address/data bus structures. □

Q-Bus Line Offers Design Flexibility For The OEM

by Dave Wilson, Technical Editor

Two conflicting forces, increased system design times and shortened product life cycles have placed new competitive pressures on OEMs. One way to remove some of the pressure is to move to a higher level of integration of the basic hardward and to a higher level of software. The tremendous market for single-board computers highlights this trend. Competitive pressure will continue to be the driving force behind new introductions in the OEM microcomputer market (**Figure 1**).

Competitive pressure will continue to be the driving force behind new introductions in the OEM microcomputer market.



These two boards constitute the CPU of Digital Equipment Corp.'s MicroVAX-1.

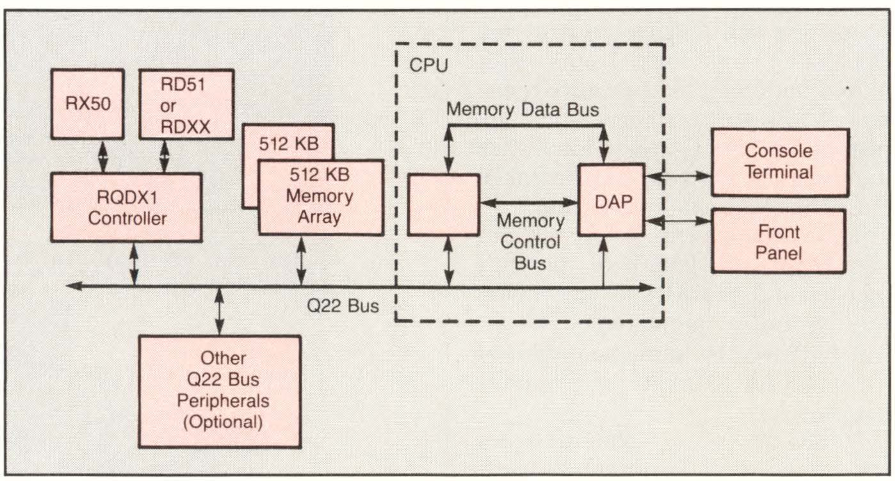
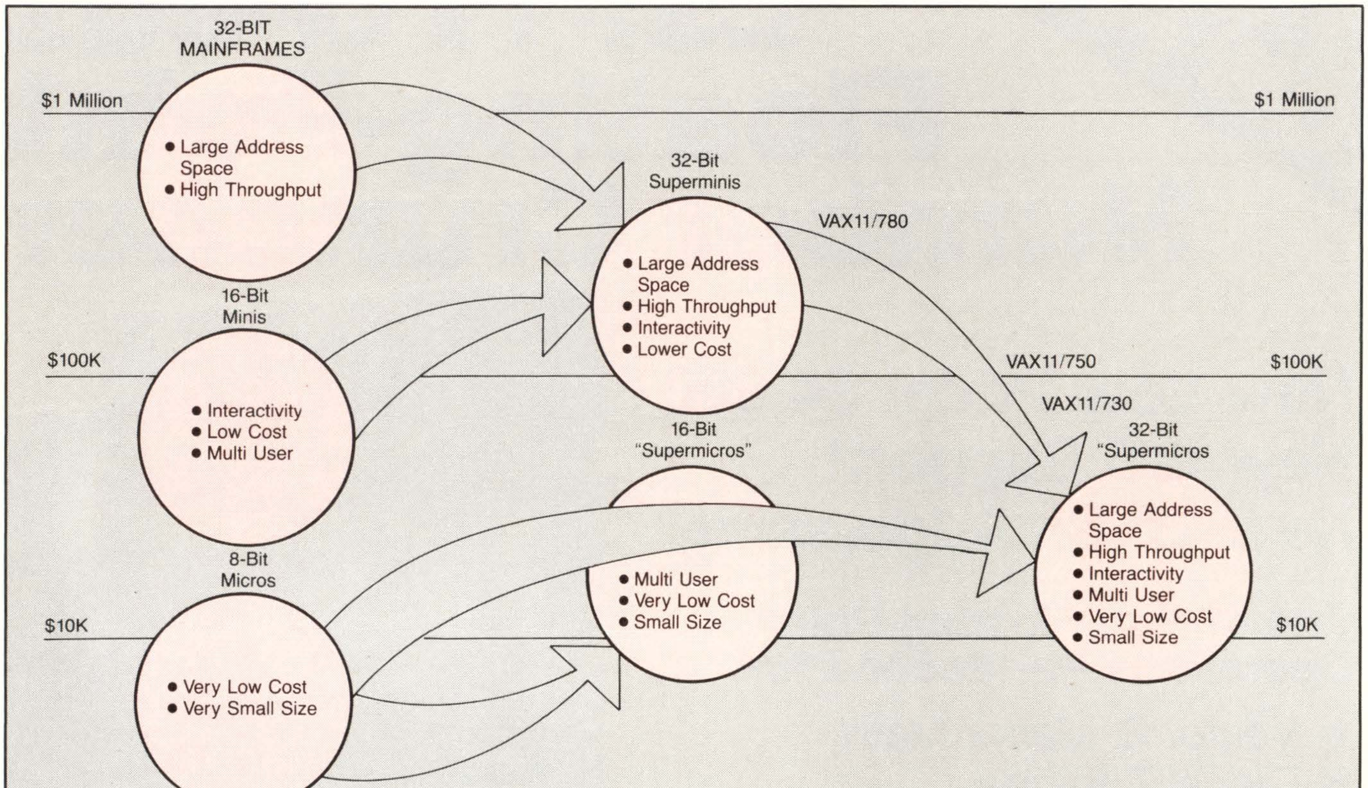


Figure 2: Schematic drawing of the Micro-VAX1 which illustrates its two-board Q-bus configuration. (Figure courtesy Digital Equipment Corp.)

This new OEM microcomputer systems market has seen product introductions from two classes of manufacturer: the conventional IC house and the third party. Intel's new 286/310 and 286/380 are examples of offerings from one IC house's systems division which are built around Intel's µP (in this case the 80286 and 80287 numeric coprocessor); the NCR Tower, on the other hand, represents one third-party design based around the NS16000 from National Semiconductor. The inexpensive computing power of these new microcomputers, coupled with their operating system support (in many cases UNIX or some version of it), is challenging the position of the large mini-mainframe manufacturer, such as Digital Equipment Corporation. Indeed, many manufacturers of such systems, compare their sys-



(Figure courtesy Charles River Data)

This chart depicts the development of the 32-bit supermicro, one of the new introductions in the OEM microcomputer market.

tems to Digital's VAX line.

Charles River Data, for example, currently claims that it's Universe 68/05 (under $10,000, and supported by UNOS, a UNIX Rev 7 compatible operating system) compares favorably with the VAX 11/750. Momentum Computer Systems compares its 32/E supermicro with the VAX 11/780 claiming that "you get 80% of the VAX's performance for 10% of the price". A System III UNIX operating system is available for the machine.

Recognizing this as clear competition, DEC has recently released a new series of VAX machines that includes the Micro-VAX 1, a two-board Q-bus configuration in a micro-PDP 11 look-alike box that will sell for less than $10,000. The major components of the Micro-Vax 1 include the KD32-AA CPU, RQDX1 controller, RX50 floppy drives, RD51 or RDXX fixed disk, Q22 memory with block mode capability, console terminal and front control panel (see **Figure 2**).

Micro-VAX 1 implements the MicroVAX architecture which is a strict subset of the VAX architecture. It features a 4 Gbyte virtual address space, 32-bit word size, full memory management (virtual to physical address translator and page protector mechanism) and emulation support for the full VAX instruction set (except PDP-11 compatibility mode). "The reason for putting the micro-VAX 1 on the Q-bus is that it's the lowest cost bus we've got today," says Ian Evans, Product Development Manager at DEC's (Hudson, MA) plant. "Further, it provides a means for the user to maintain his hardware investment."

The system busses which interconnect the modules in the micro-VAX 1 are the memory data bus, the memory control bus and the extended LSI-11 Q-bus. The memory data bus and the memory control bus connect the two CPU modules (DAP and MCT). The 32-bit bidirectional data bus is implemented

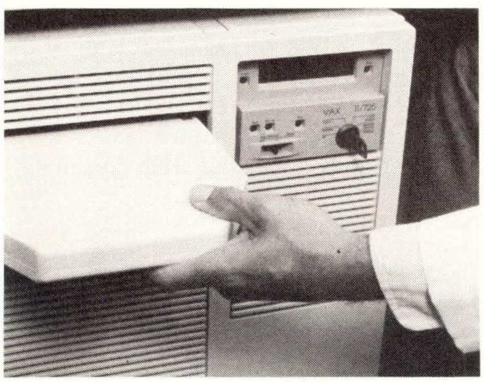
	CHIP OEM	BOARD OEM	SYSTEM OEM
DESIGN/PRODUCTION TIME	18–24 MONTHS	12–18 MONTHS	6–9 MONTHS
UNIT VOLUME	>10,000/YEAR	300–10,000/YEAR	20–500/YEAR
HARDWARE DESIGN EXPERTISE REQUIRED (TYP)	VERY HIGH	HIGH	LOW
APPLICATION SOFTWARE VALUE—ADDED (TYP)	LOW—MEDIUM	MEDIUM	HIGH
UNIT PRODUCT COST	LOW	MEDIUM	MEDIUM-HIGH

Courtesy of Intel

Figure 1: Changing OEM requirements are pushing manufacturers toward standard chip, board, and system requirements and causing them to buy higher levels of integration.

using an over the top 50-pin cable. The 8-bit memory control bus is implemented using the CD interconnect on the backplane. The remaining lines on the CD interconnect are used for dock distribution, status and miscellaneous control logic. Slots 1 & 2 on the backplane are for the two CPU modules which must be placed in Q22/CD slots.

The data path module (M7135) contains the data path, instruction decode, microsequencer and miscellaneous logic needed to implement the microVAX instruction set. The memory controller module (M7136) is the interface between the main data path, the micromachine, the Q22 I/O and the memory subsystem. An on-board data and instruction cache, consists of a 2K by 32-bit wide data store and a 2K by 16-bit wide tag store. It is the main element of a mechanism that transparently translates 16-bit data from the Q22 bus into the 32-bit data that the macromachine needs.



The 11/725 uses Digital Equipment's own 26 Mbyte fixed/26 Mbyte removable technology.

Along with their hardware announcement, DEC has introduced three software products that complement the VAX line. MicroVMS (the version of VMS that will run on the microVAX) will allow any native mode non-privileged VAX program to run on the microVAX. VAXElan is specifically tailored for the development of dedicated real-time systems for VAX machines, and VAX Ultrix will be DEC's UNIX-like operating system.

Although the microVAX may be the most significant product from DEC for a number of years, two other new VAX models should not be overlooked. The 11/725 is an open office environment VAX that uses DEC's own 26 Mbyte fixed/26 Mbyte removeable technology. The 11/730 comes as a set of modular building blocks that the user may configure a system from. The latter emphasizes DEC's commitment to offer price competitive products in an extremely active third party market.

Customers will find changing to newer architectures offered by the Motorola 68000 processor family (32-bit internal architecture) or the Intel 8086 family (16-bit architecture) far less attractive.

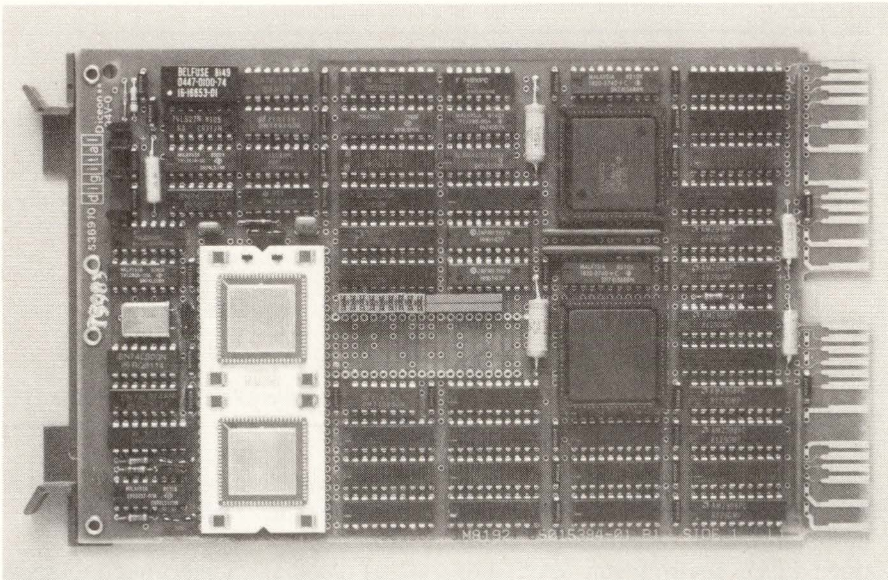
—Andrew Davis, Data Translation (Marlboro, MA)

Does this mean DEC has neglected to support its board OEM business? Not at all. DEC has recently strengthened its support of the Q-bus product line by the introduction of several new boards aimed at both computation and I/O intensive applications.

Although there has been no change in the architecture of the Q-bus itself, the new offerings will give the designer the flexibility to upgrade his existing Q-bus designs, without sacrificing the investment he has made in software development. One of the products, the LSI-11/73 is DEC's first implementation of the J-11 microprocessor. Offered as a dual-height module, the 11/73 includes integral floating point instructions, 8 Kbytes of on-board cache memory, and 4 Mbytes of memory addressing. LSI-11/23 users who require increased performance can insert the 11/73 board in the 11/23 slot and run their current application software with only minor configuration changes. These changes may include the replacement of a multifunction module used for bootstrapping. For example, many designers have integrated the 11/23 with the MXV11A multifunction module that together provide the basic essentials for a computer.

If those 11/23 users need the power of the 11/73, it will be necessary to replace the MXV11A with DEC's latest revision, the MXV11B, since the A version will not support the 11/73 board. Relative to the LSI 11/23, DEC is claiming a four times increase in performance for this product. "This is a critically important product for DEC" says Gene Banman, Director of Marketing at Data Systems Design in San Jose, CA. "The LSI-11/73 will help DEC preserve their existing base of customers in two ways. First, the 11/73 provides a fully compatible upgrade path for customers who have previously been constrained by the performance limitations of Q-bus systems, such as the LSI 11/23. Second, it provides a low cost solution for customers who have been using the Unibus-based PDP 11/34 and PDP-11/44 systems. Without the LSI-11/73 alternative, many customers may have defected to other supermicro solutions based on the 68000 or Intel 286 chips," he concludes.

The LSI 11/73 should create significant new business opportunities for Digital. Recent enhancements to the Q-bus such as block mode DMA transfers, 22-bit addressing and now the 11/73 announcement, make the Q-bus competitive with alternative bus solutions, such as Intel's Multibus. Although DEC is touting the new product as a solution to computation-intensive applications, such as CAD/CAM and graphics, (areas that require a high performance processor with float-



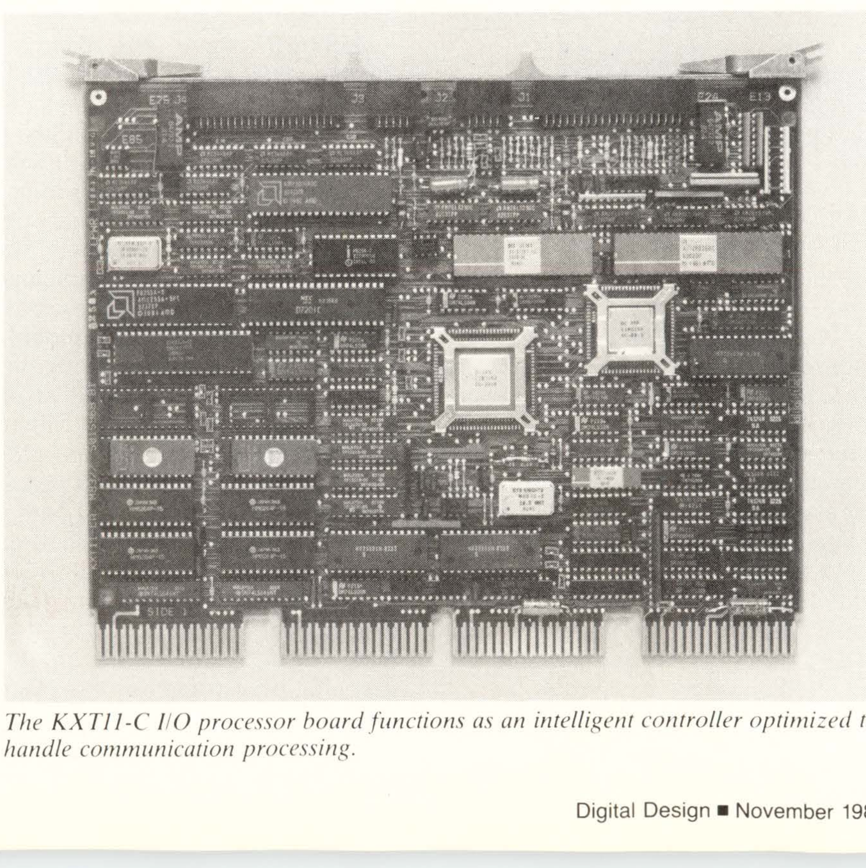
The 11/73 will be offered as a dual height module and includes integral floating point instructions.

ing point capability), Roger Aouizerat, President of Ranyan Computer Enhancement Systems, has some doubts. "The primary problem with the Q-bus engines is their program space," he says. "This, even more than computer power, is very important to CAD/CAM, image processing and data acquisition applications. It's a problem that remains unsolved with the J-11, partricularly in comparison with 68000-based Q-bus boards available on the market already that address both compute power and address space problems."

The second new DEC introduction, and the most important of the new announcements is the KXT11-C I/O processor board. The board functions as an intelligent controller optimized to handle communication processing from a wide variety of I/O devices. Since it has a dedicated μP, the bus arbiter CPU is free to perform other functions required by the application. "I/OP's are DEC's shot at what might be called multiple computing," says Robert Maiorana, Product Marketing Manager at Digital's Hudson Facility.

It is possible to add as many as 14 KXT 11-C boards in the same Q-bus configuration, each dedicated to a specific task within the application. Each KXT11-C has its own 16-bit microprocessor, RAM and ROM memory, asynchronous and synchronous communication interface and two-channel DMA controller. For systems designers the combination of the KXT11-C with the LSI 11/73 or 11/23 provides an architecture of multiple dedicated processors previously unavailable on DEC's Q-bus products. But "this kind of a solution is already being offered by many of the DEC compatible vendors to alleviate I/O bottlenecks when using DEC's architecture," adds Bill Wollan, National Sales Manager for MDB Systems (Orange CA). As with any DEC introduction, the KXT 11-C has led many to attempt to predict DEC future plans. Richard Hickstead, President of Micro Technology feels that the 11-C may simply be a lead-in to a product which will add an I/O Q-bus in parallel with the normal Q-bus and dual-ported memory, a rumor that has been around the industry for several months. Only time will tell.

The third DEC introduction, the Falcon-Plus, replaces the Falcon SBC-11/21 as DEC's low-cost PDP-11 SBC for ROM-based dedicated applications. It offers a T-11 CPU, RAM memory with sockets to support additional RAM or ROM memories, a real-time clock, and a Q-bus interface to provide bus expansion should the application ever require it. "A whole lot of customers thought the (original) Falcon was a great machine for dedicated ROM-based applications," says Philip Pomeroy of DEC's Technical Volume Group. ". . . but they expressed the need for a low-cost PDP-11 that they could use for more general purpose applications



The KXT11-C I/O processor board functions as an intelligent controller optimized to handle communication processing.

for which they would need an operating system."

Falcon-Plus, with its 16KB of RAM, and optional additional 32KB not only accommodates the RT-11 single-user real-time operating system running on-board, but also improves the performance of programs written in MicroPower/Pascal. MicroPower/Pascal was announced in 1981 with the Falcon SBC-11/21. It is a software tool kit that is actually an operating system and a high-level real-time programming language. Micro Power/Pascal allows realtime programmers to select only those software resources they need to build efficient run time kernals.

Development of MicroPower/Pascal programs is performed on a separate host system. Code is written, compiled and linked on the host system, then down-line loaded over a serial line into the MicroPower target CPU for execution. Debugging also takes place from the host system. In the past, Micropower/Pascal development was only possible on RT-11 systems. Many customers who had RSX-11M RSX 11M-Plus, and VAX/VMX systems had to purchase single-user RT-11 systems to develop MicroPower programs. They also wanted to have more than one programmer developing code for the same application on a development system.

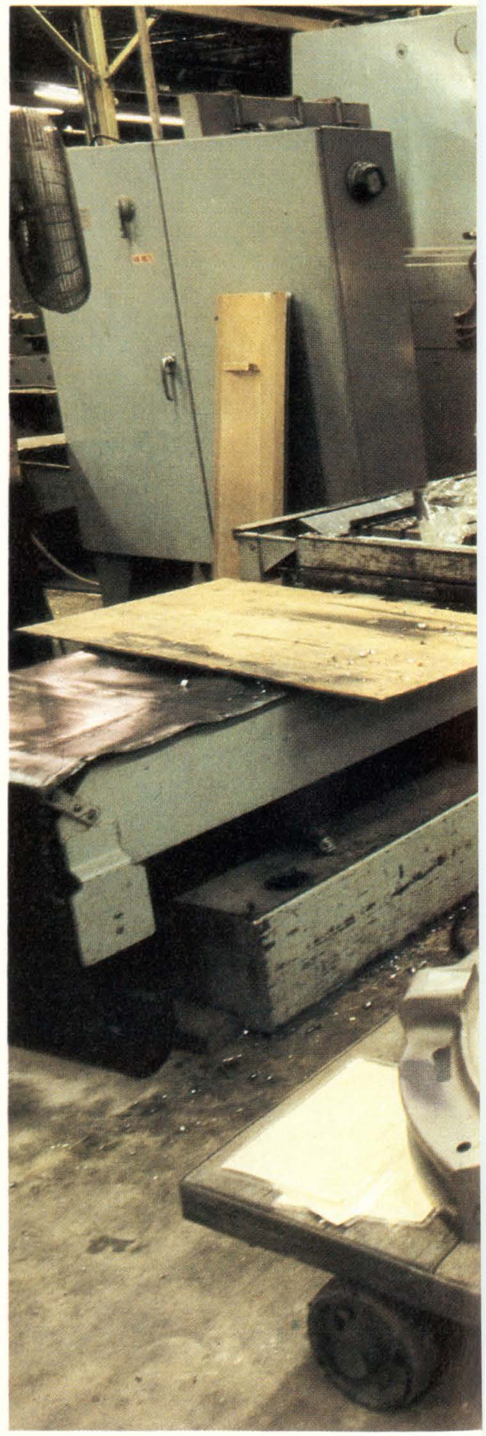
With the annoncement of MicroPower/Pascal-VMS and MicroPower/Pascal-RSX, multi-user MicroPower development is possible on 32-bit and 16-bit DEC Systems. Each is a layered software product that allows multiple programmers to develop MicroPower applications concurrently on the same VAX/VMS, RSX-11M or RSX-11M-Plus system. Programmers can divide the application into tasks, share common files, code and compile separate MicroPower modules, and then link them together into a single customized runtime kernal using special MicroPower utilities.

Finally, DEC has bowed to competitive pressure in offering a one year, return-to-factory warranty on the three new Q-bus products, the 11/73, 11-C, and Falcon Plus, a standard in the DEC compatible industry for years. All of these products indicate DEC's renewed interest in the low-end OEM world, and the new introductions will go a long way in retaining the large market DEC has already captured.

With DEC recently making available the J-11 chip set to designers, it will be interesting to observe the third parties that take advantage of the large base of DEC software, while introducing products based around the J-11 onto the Multibus or the VME bus. Many companies interviewed during the preparation of this article indicated that a few such designs are currently under development and should be available early next year. □

Solids Modeling Becomes The Driving Force Behind Automation

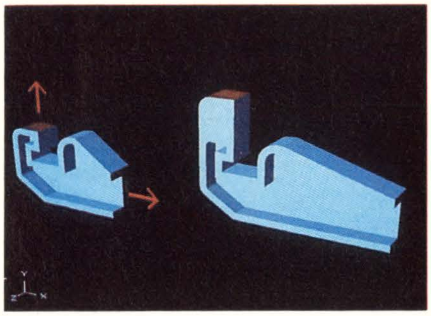
Solid modeling systems have been available for over a decade but recent developments in semiconductor memory and processing capabilities have brought SM to the forefront of active development and promotion.

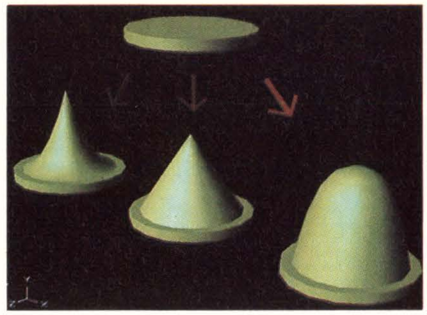


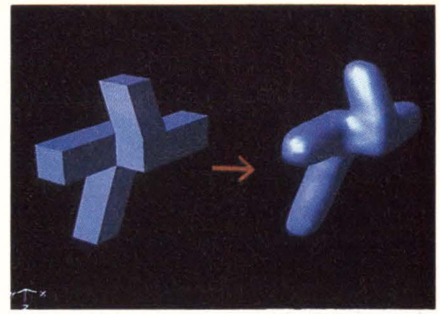
by Jerry Borrell, Editor-in-Chief

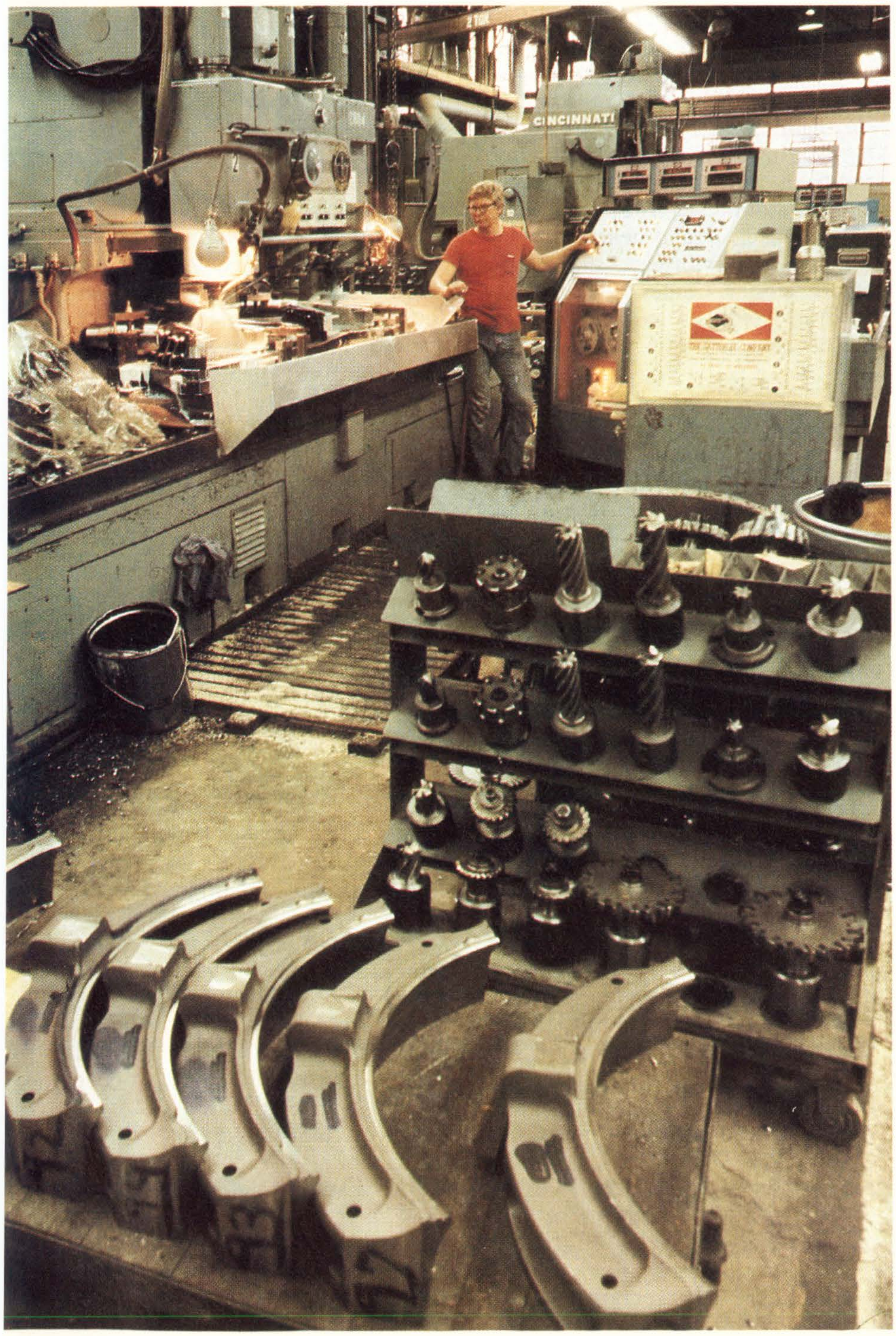
The annual Autofac show, held in Detroit and sponsored by the Society of Manufacturing Engineers, has become one of the premier events at which robotics, computer graphics, and manufacturing processes are brought together to demonstrate the progress in new technology. This year, a key focus of the event will be the integration of computer aided design, computer aided engineering, and computer aided manufacturing by system builders, integrators, and software developers. This integration centers upon what is known as "Solid Modeling" (SM), and is occurring because the data stored by the computer to geometrically describe the shape of a solid model is useful in all three of the disciplines mentioned above.

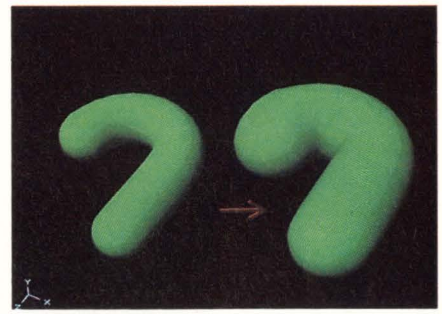
One of the most contentious issues for potential users of SM is the need to understand what the term means, and how to obtain access to the technology. One of the difficulties in doing this is that SM is a term often applied to hardware, software, and integrated systems. For instance, a CAD system may be said to have SM capability if it allows the user to define (for any given model) points within, adjacent to, or outside of a plane of the object. Others take a much more demanding view and state that a system may be said to have SM capability if it allows for design, drafting, or analytic functions related to solid objects. There are several manufacturers of graphics processors that are particularly suited for SM applications who claim to have SM systems, whether or not they are able to provide software capability to the user. Similarly software developers claim to have solid modelers, and their relationship to the display device and the central processor are secondary. Finally, there has been confusion about what sort of software capabilities may be used to define a SModeler. In this area there are several issues. One relates to the manner in which the system or software organizes its data for storage, often as either a faceted (approximate) or a precise model. Another issue is whether or not the displays are wire frame drawings or color rendered (smooth shaded). The last and most current misconception is that

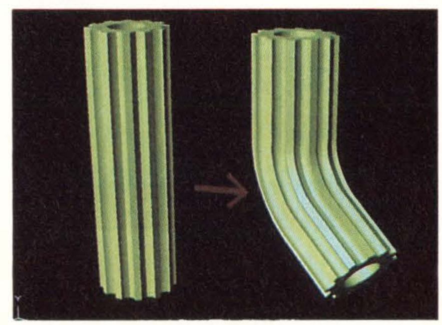


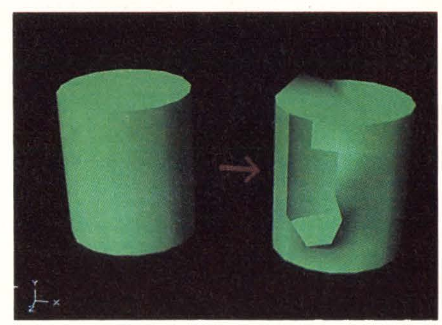












Above: Editing functions performed by SDRC's IDEAS modeling package 2D equivalent functions such as stretching and warping as well as functions unique to SM: blending, thickening, and bending. Other tasks unique to SM include surface operations such as tweaks for deformation.

The use of SM as a point of integration for industry in computer aided design, computer aided engineering, and computer aided analysis is occurring at firms such as Control Data (left) where all of these disciplines are being united.

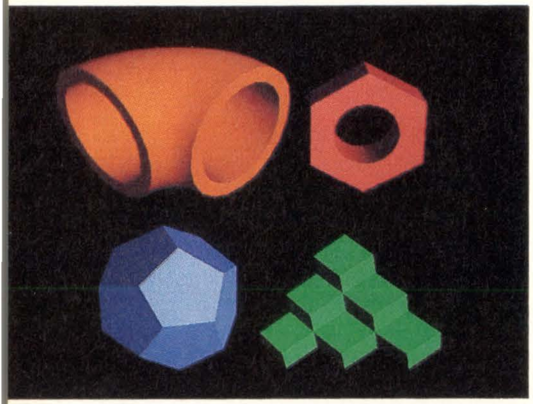


Figure 1: Geometric Primitives available on the CT-S modeler developed for use with the IBM PC by Cubicomp of Berkeley.

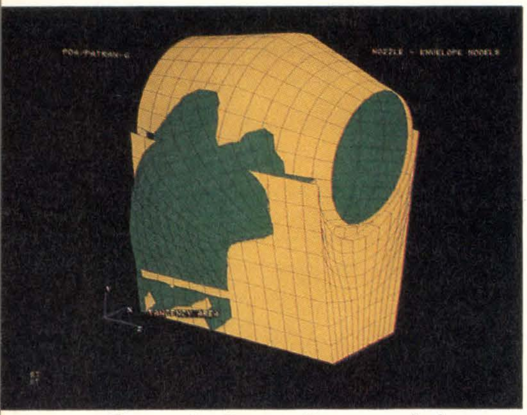


Figure 2: Patran-G, one of the most widely available finite element modelers, demonstrates the use of SM for interferences in this shot where the internal construction of the combustion chamber in green overlaps with its housing in yellow.

a system may have to allow for operator interaction with geometric primitives to qualify as a solid modeler. Unfortunately, many of these issues will not be readily answered because the announcements of products for this fall will offer systems that provide for operations within many of these functions. At least one company, Phoenix Data Systems and its designer Donald Meagher, raise questions about the viability of the mathematical approach that most system providers have taken, and advocate their unique solution for more sophisticated models—initially medical displays.

In this article we examine how SM systems have developed, how the functions for CAD/CAM/CAE are being integrated in SM, discuss the new products from graphics display processor manufacturers which are oriented to faster rendering of shaded images, examine how systems are being provided by marketing groups, and consider the designer interaction tools offered with SM systems.

Development Of Solid Modeling Systems

Many of us forget that solid modeling systems have been available for over a decade, primarily because recent developments in semiconductor, memory, and processing capabilities have brought SM to the forefront of active development and promotion. Early research and development at and near the University of Cambridge, the Cambridge Design Center, and at firms such as Compeda and CIS led to the development of SM software in the late '60's based upon storage tube display systems. A great deal of work also went towards providing an interface for the numerical control of manufacturing devices and several machining and milling control packages were developed. The geographical isolation from US CAD firms, and their lack of color rendering provided a superficial barrier to the implementation of these systems in the US. Even in cases where there was an effort to supply them, the marketing efforts have been less than successful. Over the last few years, many young mathematicians and designers have left British firms and institutions with experience in solid modeling, subsequently joining firms such as Computervision and McAuto providing for an effective transfer of technology. Several firms have been acquired, for example, the recent purchase of CIS by Computervision, Shape Data Ltd. by Evans and Sutherland, and Compeda by Prime Computers. Other US systems have roots of development in France, including the CATIA package IBM acquired from Dassault, and Euclid developed by Matra of France and marketed in the US by Matra Datavision.

During the same period of time in the US the emphasis of development was towards applications packages for 2D drafting and design; with Computervision, Applicon, Intergraph (formerly M&S) and Auto-trol being prominent examples. One firm, the Mathematical Applications Group Inc. of New York (MAGI) was performing extensive work for the military to investigate armor piercing capabilities of projectiles which led them to develop a software program which came to be known as Synthavision. This software, long ignored by the leading CAD firms, became a bastion of available expertise and licensing for several US CAD firms, who in the late 70's were seeking to develop their own SM capabilities. Synthavision applied a ray tracing technique to determine impact characteristics of projectiles that was also suitable for rendering color surfaces. In addition, they popularized the use of a stored group of geometric primitives which allowed their systems to be used to create solid object models rapidly. Control Data, Applicon, and others either made use of or studied their software to help them enter the field more quickly.

Another effort to develop SM tools came from a group of manufacturers including General Motors that funded a research program for SM at the University of Rochester, called the Production Automation Project under the direction of Herb Voelckler. The project developed two important programs, PAD-L and PAD-L II which have been widely licensed and remain excellent educational tools. Two companies, GM and McDonnell Douglas have used this research as a basis for their development of SM systems called GM Solid and UNISOLIDS respectively. Another product developed as a result of research is the TIPS modeler, from Hokkaido University. This package is sold as an educational tool as well, by the CAM-I of Austin, Texas.

Several currently available packages have been developed by individuals either from the companies above or from research environments where solid geometry was a basic consideration. The Anvil

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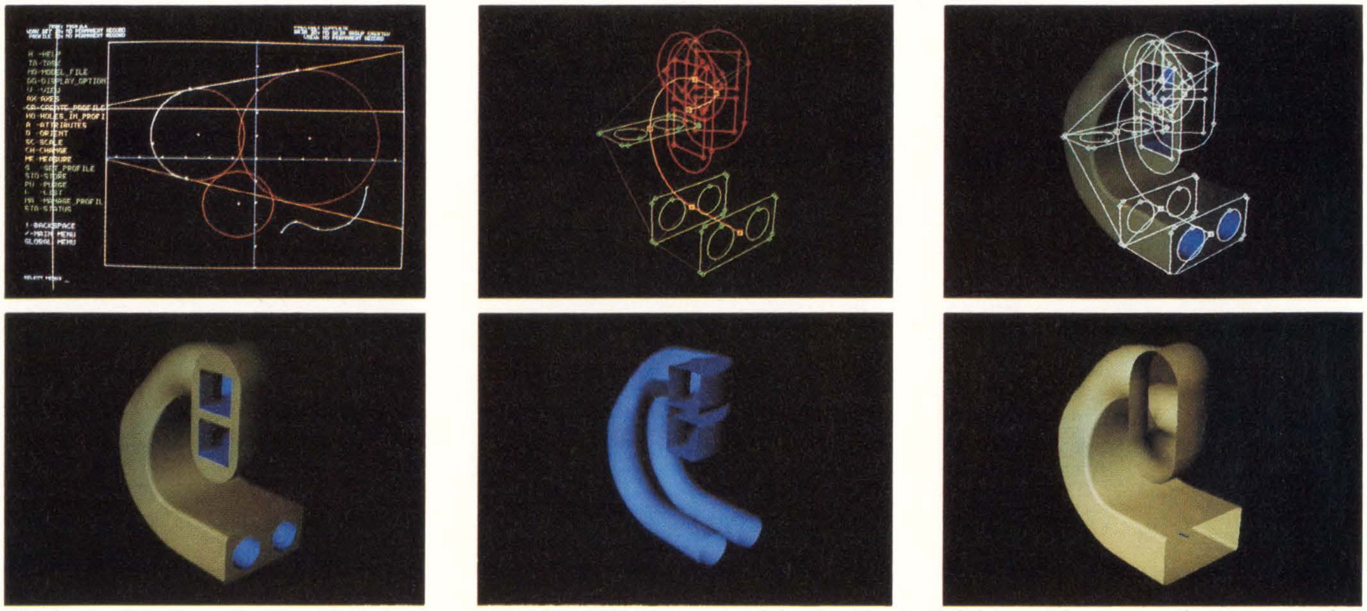

Figure 3: Creation of a manifold design on SDRC's IDEAS supported by Lexidata's Solidview. The system demonstrates the problem of parametric input in terms of time required, and the technique's flexibility in the creation of complex designs. Another advantage of SM in general is shown by the ability to define internal views once geometry is input.

packages, for instance, were developed by Pat Hanratty who had experience with 2D CAD manufacturers. The ICM modeler from Larry Barinka resulted from earlier work developing modeling systems for CAD in the nuclear power plant design arena. SDRC of Milford, Ohio developed a SM capability as a result of work with the analysis of vibration study for the automotive industry.

It is difficult, perhaps needless, to consider the origins further because today the bodies of code used to build these software packages have been redefined or rewritten to such an extent that they bear only marginal resemblance to their sources. The marketplace has become so active that most SM system providers are developing a second generation of SM technology. Large companies that originally took inefficient approaches have purchased the rights to or licenses for SM capability. In addition, there is ongoing research in commercially available packages at centers such as Purdue Universities' Graphics Lab, and in corporations such as IBM and Grumman, where there are proprietary SM systems in use.

Graphics Processors

Two factors are driving development of graphics processors for SM—the demands for color and interactivity. When these two combine they tax the ability of system providers to compete effectively with 2D and 3D CAD systems. As one might expect, the complexity of solid geometry makes rendering in color difficult. Two approaches are taken by manufacturers today: allowing the design process to be performed in "faceted" or approximate representations of the SM (which speeds the process greatly),

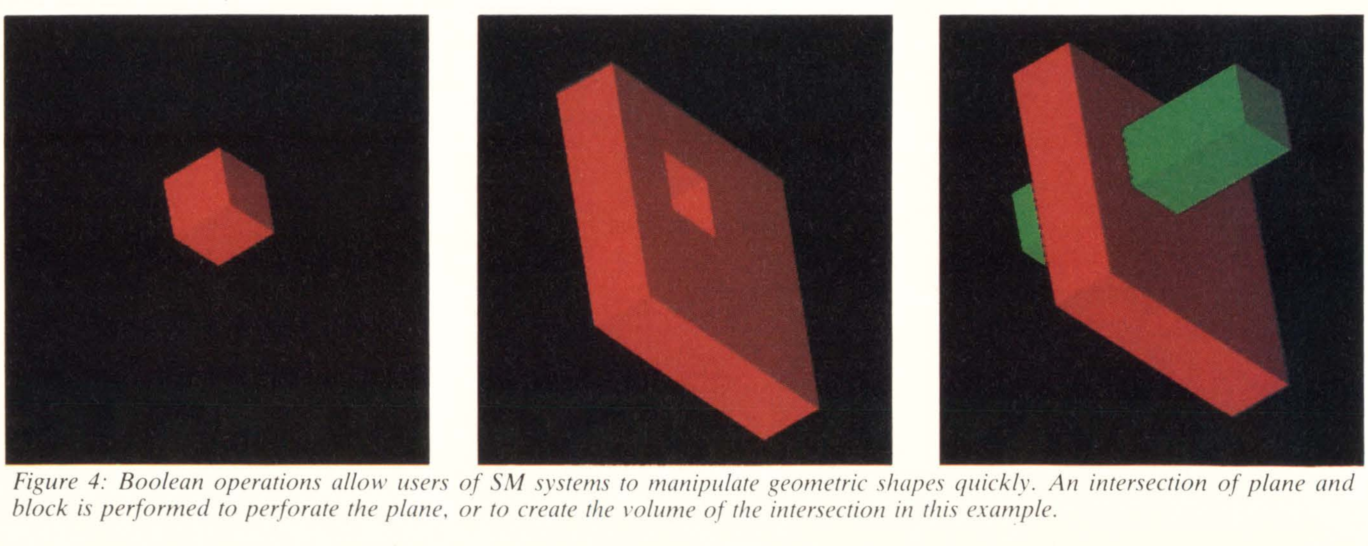

Figure 4: Boolean operations allow users of SM systems to manipulate geometric shapes quickly. An intersection of plane and block is performed to perforate the plane, or to create the volume of the intersection in this example.

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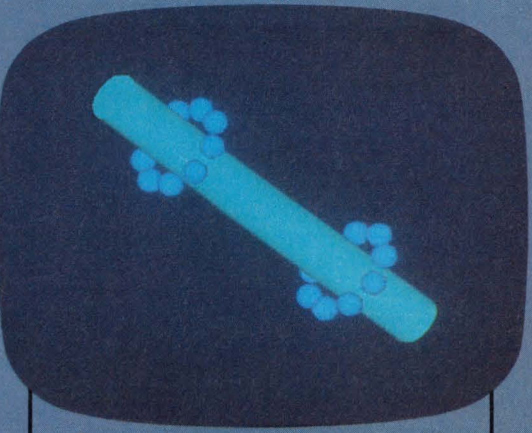

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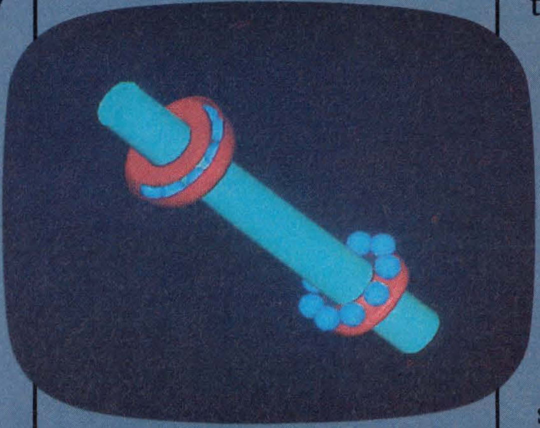

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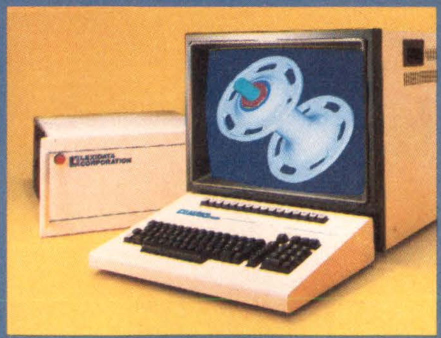

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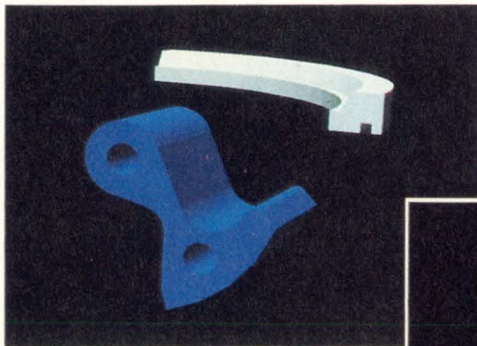
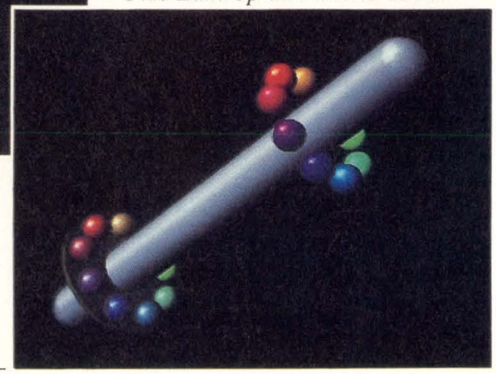
™ SOLIDVIEW is a trademark of Lexidata Corporation and assigning a device to the specific functions of rendering the model's surfaces. Only a year ago, the universe of SM systems could be divided into those who stored data as precise or faceted files. At present, many systems maintain both types of data files for some portion of the design process. In merely inputting or editing a geometry there is little need to dedicate processor time to producing a display that has the same quality required for product promotion or advertising.

The demand for color is addressed by devices such as Lexidata's Solidview, Raster Technology's 125S, Weitek's Tiling Engine, and custom processors such as those developed by Megatek, Intergraph, Applicon and others. While these devices still do not support dynamic manipulation of SM with the facility available on 2D and 2½D systems, their rendering ability is now very close to being "interactive". This demand has brought six announcements on the Lexidata Solidview: ICM of Virginia, Prime Computer, MCS's OMNISOLID, Matra Datavision's Euclid, SDRC's IDEAS, and Patran-G from PDA. The first three of these represent new product lines based upon the processor. The Solidview is a separate product which at this point is added to systems as a post processor. ICM has implemented an Apollo 300 workstation for the faceted modeling and the Solidview for color rendering in what is the fastest capability for rendering color SM in a precise form available at present.



▲ *Figure 5: Techniques of software editing include operations of revolution shown in white and extrusion in blue. Both types of operations allow 2D planar outlines to be translated across space to quickly generate solid parts.*

▼ *Figure 6: Image generated on Raster Technologies' new 125S of a ball bearing/axel chassis created by Olin Lathrop and David Kirk.*



The Weitek Tiling Engine represents a similar approach, but is being sought by several manufacturers as an OEM product, to be manufactured to the integrators system and bus specification to allow a color capability. For instance, Ramtek, Auto-trol, and Sun are said to be seeking agreements to add the engine as an integral portion of their display; an advantage because the engine could then be made to accept data for rendering in the form used by the system, rather than having to convert to the format of the processor itself.

Why cannot the well established high performance processor developers such as Evans and Sutherland, Megatek, Ramtek, Genisco, and Adage immediately support SM rendering? The answer lies in the need to provide the additional memory for the Z axis, so called "ZBuffer" memory. The Z buffer is used to process the shape date for the models, and render the surfaces either from polygons or primitives and perform functions such as lighting and clipping. Devices such as those from Lexidata, Weitek, Raster Technologies, Parallax, and GTI are ideally suited for the Z buffer sorting. This capability would have to be combined with the fast refresh rates for drawing vectors to provide a SM system with color shading that is not only interactive, but which would support dynamic operations such as translations and rotations.

Phoenix of Albany combines existing graphics processors, high capability minicomputers, and its custom processor to provide rendering capabilities of the most complex solids being rendered, medical displays of brain scans. Both Ramtek and Intergraph indicate the use of gate arrays in their new products, at up to a 5000 gate level which may show that the third generation of SM display processors has yet another alternative for implementation. These solutions are aimed in the near term at providing rendering and not dynamics and rendering. One indication about this sort of capability is shown by Weitek who indicates that their next generation product will combine their tiling engine and floating point processor in silicon.

Promising directions in technology come from those firms working with 16 bit microprocessors and new display processors such as Cubicomp of Berkeley, Vectrix of Greensboro, Catronix of Atlanta, and Graftek of Colorado. Cubicomp's processor is designed specifically for the IBM PC, Vectrix is initially configured for the Apple, Catronix has been written for the Terak, and Graftek is now being implemented on the new N-GEN system from Convergent Technologies. The common problem for all of these systems' developers is that the majority of software developed for SM has been on the mini and super minicomputers. The effort by these four manufacturers then has had to be both developing their own less costly display processors, and to write SM software suitable for 16 bit processors. Catronix has demonstrated a Romulus in the first effort of a small system to provide access to one of the established packages. While many of the systems have generated a great deal of excitement, as shown by the capabilities of Cubicomp in the illustration, it may be necessary for 32 bit microprocessors to be available for systems integration before it is practical to mount much larger packages. Joint efforts by Hewlett-Packard and Gerber, and Hewlett-Packard and Metheus show the trend towards this area.

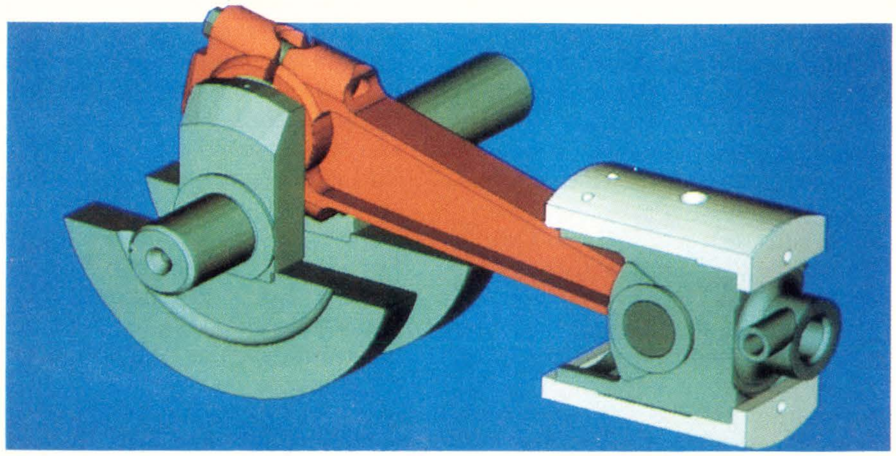


Figure 7: Applicons' Solid Modeling II is a second generation SM system and incorporates one of the most advanced DBMS, pre, and post processor interface packages for interactive design, and development of displays for engineering analysis and design, under the BRAVO product line.

Design Interaction Design Input

One of the greatest potentials for enhanced efficiency through SM use is found in the design function. While the bulk of software design techniques for SM are those of 2D and 2½D CAD, several manufacturers have developed techniques that offer more benefits. These may be divided into two categories: those for the input of geometry and those used in editing functions. The input techniques may be further subdivided into those systems using constructive solid geometry (often geometric primitives) for the creation of designs or those who use design parameters and more traditional lines, points, and 2D primitives (circles, etc.). The latter distinction has, however, become blurred, because of systems such as Solids Modeling II from Applicon which maintain a database of primitives, but which nevertheless require some parameter input to call up the primitives.

There are advantages in both approaches. While the input of a design's geometry may be much slower with parametric techniques (see series of slides) there may be advantages in that if a 2D drawing is required for drafting purposes, the geometry is already available and may not require extensive computing. In addition, no CSG SM system can maintain a library of primitives large enough to always avoid having to create new primitives. In the case of developing models for related applications such as finite element analysis the designer will have to use parametric input to define complex surfaces. The delay in this application, 2D drafting, and CSG SM is that in order to display lines, the user must extract edge and vertices information from the display files. A final advantage in the wire frame or parametric approach is that many of these systems have been developed from 2D CAD systems and already have the capability of drafting, annotation, and plotter interface: Medusa, Romulus, Euclid, Omnisolid, Solid Modeling II, PADL, ICEM, and others. Both approaches have suffered in applications requiring fast rendering, as noted above.

Design Editing

Just as SM is useful to the designer by providing more information about an object, the same characteristics can prove to be detrimental or beneficial in editing functions. One of the primary benefits is seen in the rapid ability to provide sectional views. Sections become even more easily defined when the system has Boolean capability shown in the slides from Phoenix. Boolean functions provide the designer with the capability of intersecting, unioning, or subtracting models from one another. Boolean operation may also be considered an input function, but is most efficient for sections.

The broadest range of SM editing techniques is demonstrated in the series of slides from SDRC. Many of the editing functions are the SM equivalent of 2D functions. Stretching, for instance, is the 3D equivalent of scaling or rubberbanding. Sweeping functions have been used in 2D and allow design modification through rotating the outline or profile of an object about a horizontal or vertical axis. Similarly, skinning or warping functions are equivalent to 2D interpolations of shape between two endpoints. An especially complex example is shown in the creation of a manifold example from SDRC in which several midpoint and two endpoint planes were parametrically defined and joined.

There are unique functions to SM. Bending and blending, for example, perform what the name describes (shown in illustrations) but in 3D. There is also a series of complex surface editing functions best exemplified in SDRC in which a surface may be deformed, or "tweaked." These functions are vital if the system is to have ready application in CAE for the definition of surfaces is at the heart of most analysis. These functions vary from system to system, and may prove a vital point of evaluation for the purchaser. Parametric based surface operators such as tweaks may allow for easy manipulation, and have secondary benefits in readily providing surfaces and edges upon which to define meshes. CSG surface or planar primitives lack this but are defined with a fraction of the effort.

Both parametric and CSG input based systems have the ability to store primitives of convenience, that is those objects that may be frequently modeled can be stored and retrieved when needed. Unique primitives created by the operator may be the most effective applications of this design function.

The last consideration of design interaction is that of the physical interface; keyboards, joysticks, trackballs, and voice. Until recently one of the inhibitions to the use of SM was the lack of a physical device interface. In working with MAGI, for instance, where rendering time was significant, a single edit would entail a lengthy wait before the operation could be inspected. This type of interface is addressed with faster rendering devices. Related to the slowness of interaction was the lack of a tablet interface which has become a standard design tool for drafting systems in CAD.

Another insufficiency relates to the development of interactive techniques for CAD from 2D systems where cursor controllers such as joysticks and trackballs were sufficient. In manipulating solids, these tools had limitations in both input of geometry and for editing. This has been addressed by the development of the 3D cursor from Lexidata and the 3D trackball.

Several of the systems have retained a keyboard means of interaction, in part due to a research-limited origin, and in part to the European systems being related to systems that had strong use of text and annotation for traditional CAD application.

More than any other aspect of SM, design interaction becomes an area where systems slowly emulate one another bringing a commonality of functions. This is not true of applications functions where any manufacturer develops expertise and software in areas were subject expertise is represented. Intergraph has been the first to successfully sell voice interaction devices into the market, perhaps resolving the issues above.

Interface To CAD And Analysis

One of the most problematic issues for the developers and users of SM systems is the integration of analysis and manufacturing capabilities. Conceptually the advantages are obvious—in describing the geometry for an object's shape the designer also deals with the information that may be used in subjecting a model to analysis or in transfer to numerically controlled machine tools. In practice, the requirements of processor time and capacity, and the need to transfer information from one set of data files to another becomes onerous. Beyond this is the need to unite all of these operations in a single set of operating commands and system menus, representing enormous tasks—best addressed, to date, by Applicon, Control Data, and MCS. System developers must consider this in light of the relatively recent addition of graphics capabilities to what has traditionally been the statistical and tabular evaluation of designs by engineers. However, as analytic functions become available in graphics displays, the effort to integrate design and analytic functions has increased. The link to manufacturing functions is relatively primitive in graphics terms, but applications such as interference investigation indicate trends in the area.

Design and Analysis

Two of the most commonly used techniques for engineering design and analysis are the generation of meshes and the use of analytic programs based upon the structural information provided by the mesh. While several of the larger manufacturers such as Control Data, Applicon, Intergraph, and MCS have sufficient expertise to write their own mesh generators, the majority of firms rely upon well established companies with finite element modeling packages used for mesh generation, most often GE's subsidiary SDRCS' Supertab or PDA Engineering's Patron-G. The second step is to subject these models to an analytic program where the best

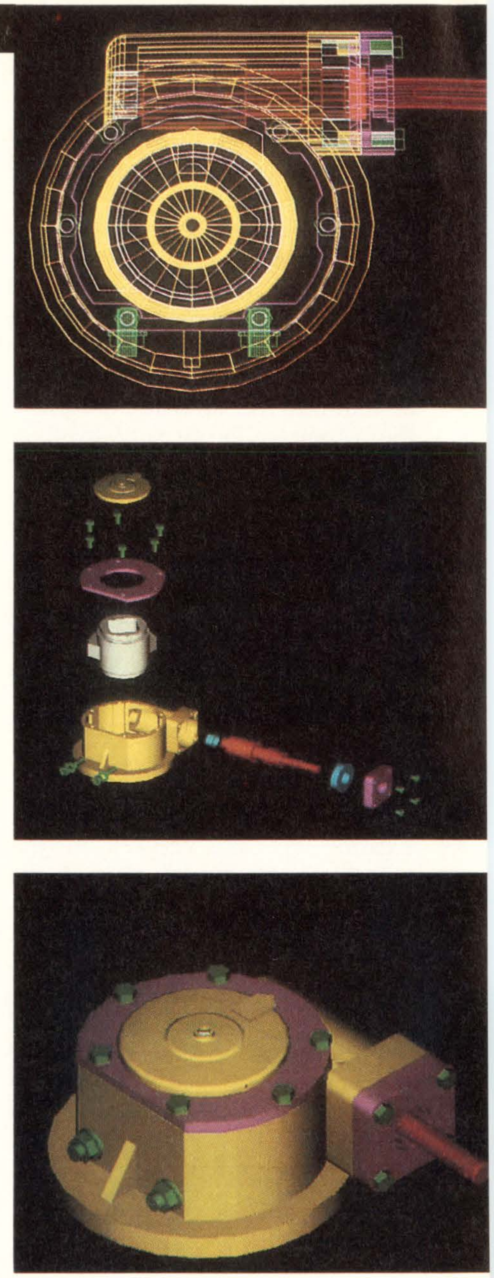


Figure 8: ICM has implemented a faceted modeling technique on the Apollo 300 workstation for interface with Solidview to provide one of the fastest renderings of a precise model SM system commercially available. A worm screw housing is seen displayed in color wire frame, rendered as exploded and united.

known independently written packages are MSC NASTRAN Mac Neil Swindler, Swanson's Ansys, and STRUDL. The companies mentioned above as having written their own mesh generators have also been able to develop analytic packages. SDRC and CDC, for example, have particularly broad offerings for analysis.

While the data used for these purposes and for SM is basic to the information needed in post processing work such as the creation of tapes to drive numerical control devices, extensive work is required to develop the interface between the programs. The best known include tool path generators such as Compact II or APT for milling use.

It is practical for companies such as Control Data to maintain an expertise related to all of these fields in house, but for the majority of firms, the effort at comprehensive availability of several types of these functions must be directed towards providing interfaces that will provide for common computer system operation. Even where device interfaces are provided for a broad group of software applications, the size of any given area may overwhelm the capability of a single system to provide interactive use of the programs. SDRC's mesh generation alone requires over a quarter of a million lines of code. Given the large amounts of data operated upon by the programs, the limitations become evident. Storage alone becomes a significant problem, as does the speed at which this quantity of data can be transferred. In the face of such issues, the problems of adding an interactive display capability based upon use of these sophisticated programs remains to be solved.

Summary

The race towards the automation of industry has many centers of focus and is known under acronyms such as: computer integrated manufacturing, or factory of the future. All of these areas are dependent upon the ability of the computer to manipulate information, and upon the ability of devices like robots to manipulate processes in manufacture.

Computer manufacturers seek to either maximize the number of independent software developers providing SM packages that will operate on their computers, seek to add SM hardware capability to their systems through OEM purchase of products from graphics processor companies, or hope to provide totally integrated capabilities for SM including training, support, consulting, and maintenance. The graphics processor manufacturers seek to insure the software houses write the interface needed so that their packages can prevent the loss of sales to other producers. Software developers similarly seek the widest base of device interfaces to allow customers easier access to their products. Finally, the designer must consider that there is a new generation of technology soon to be available that may resolve several of these issues at one time—potentially slowing processes of acquisition or evaluation. Thus advances in technology are at once providing new promise for the automation of industry and at the same time requiring that the user or designer be a more sophisticated evaluator not only of the systems and their applications but of the trends of technology at large. □

Solids Modeling Manufacturers

For more information on the following solids modeling manufacturers write in the appropriate number on the *Digital Design* Reader Inquiry Card.

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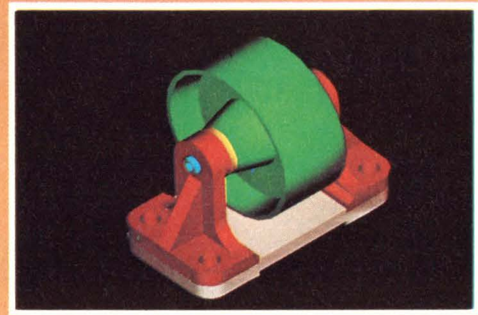

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  - Graphical Sketching Mode
- **Geometrical Modelling Attributes**
  - 2-D Drawing
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  - Isometric, Perspective, Cutaway Views
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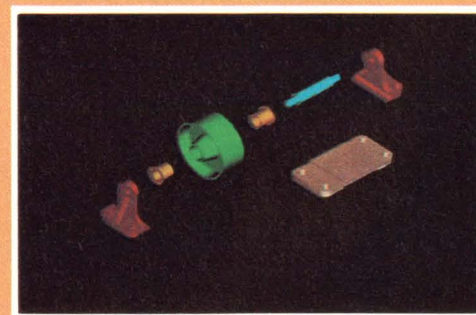
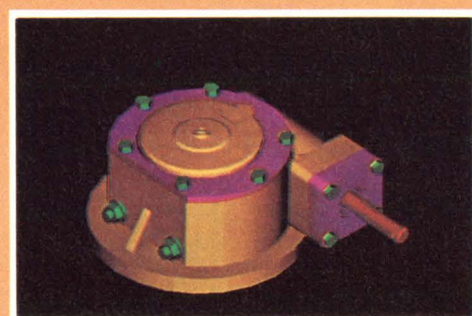
  - Input Error Processing
  - "Exact" Procedure Files
  - "Approximate" Model Files



ICM: Interactive Computer Modelling, Inc. (ICM) is a professional consulting corporation specializing in the finest in computer assisted engineering (CAE) software products and services.



MODELLING PHILOSOPHY: The ICM Geometrical Modelling System™ employs a hybrid implementation of the constructive solid geometry and boundary representation approaches that combines the advantages and minimizes the disadvantages of "exact" and "approximate" geometric models.

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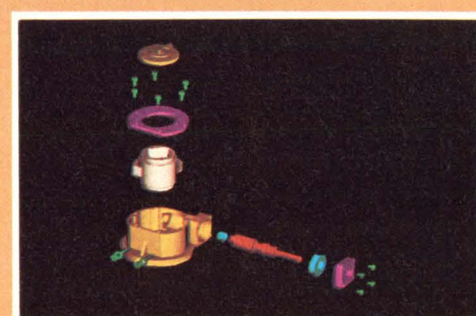

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REMEMBER: "If a picture is worth a thousand words, then an ICM geometrical model is worth (at least) a million words!"

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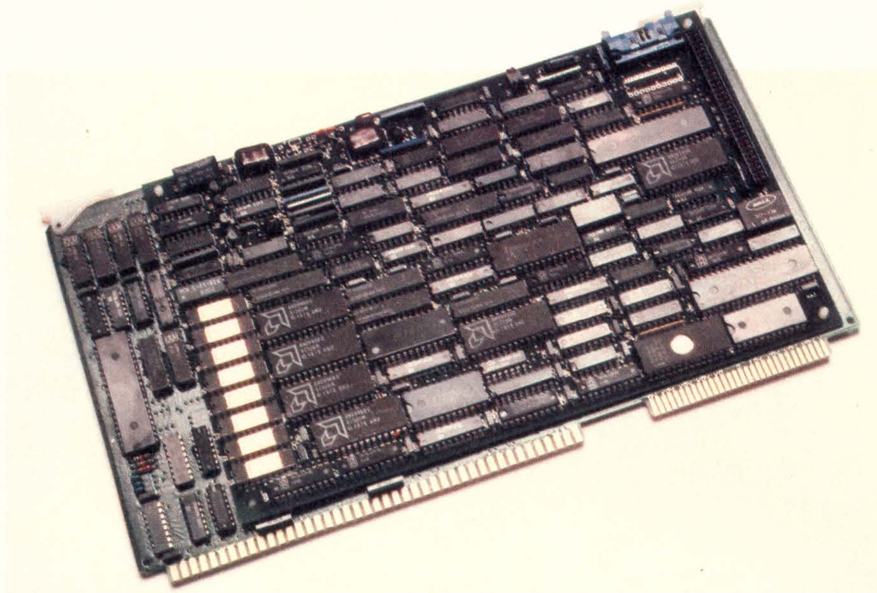
LAN—A Solution To Efficient Computer Interaction

by Ram Appalaraju



Ethernet Controller for Multibus based processors—Interlan NI 3010.

Applications in which computers separated by a short distance (a few kilometers) are interacting between themselves and not with a distant device are said to be involved in local area computing. The networks in such applications, known as Local Area Networks (LANs), are an offspring from distributed data processing environments. A LAN may be defined as a network that covers an area within a radius of a few kilometers, a total data rate exceeding 1 Mbps, and single organization ownership.

Since the late 1970s, many companies have entered the LAN market. Today, various types of networks have become standardized, helping the users, and manufacturers of supporting devices. The IEEE 802 standard on LANs is widely accepted, however, the IEEE 802 defines only with the physical and data link layers of the 7-layer open system interconnection model developed by the International Standards Organization. The seven layers and their functions are represented in **Figure 1**. Terms such as interfaces and protocols may be defined based on the 7-layer model. An interface can exist only between a module in one layer with the layer below it. Protocols are relationships between equivalent modules in different workstations (also known as nodes). The formats and the rules for exchange of messages are defined by the protocols.

According to the IEEE 802 standard, LANs may be classified into Carrier Sense Multiple Access with Collision Detect (CSMA/CD) and Tokenpass. The CSMA/CD is further classified into baseband, (<10Mb/sec) and broadband (>10Mb/sec) networks. Token pass networks are divided into bus and ring. Further classification is based on the media of communication, which, to a large extent, determines bandwidth and range. A detailed performance comparison of different media is made in **Table 1**.

The physical and data link layers of the 7-layer model has been implemented in hardware in recent products. The hardware implementation is either VLSI Cs or Field Programmable Logic Arrays (FPLAs). Apart from the media of communication, factors such as topology and speed of transmission must be considered in the design of the hardware. The nature in which

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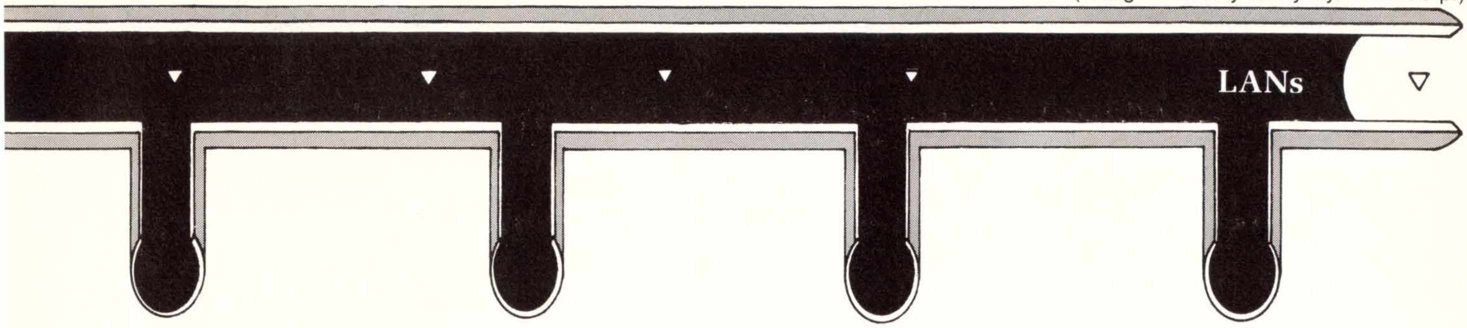
(Design Courtesy Daisy Systems Corp.)



A LAN may be defined as a network that covers an area within a radius of a few kilometers, a total data rate exceeding 1 Mbps, and single organization ownership.

the different nodes are connected through links constitute the topology. Though rings and busses are growing in popularity, stars and meshes are also in existence.

The CSMA/CD networks are based on a contention technique, basic fundamentals of which include: no errors except collision, constant length packets, delay very small compared to transmission time and absence of capture effect.

The nodes in the network have the ability to determine the traffic in the channel. In CSMA/CD networks, each node transmits only if the node senses that the channel is free (i.e. no traffic). It is, of course, possible for two different nodes to detect that there is no traffic on the channel at the same instant. In such a case, if both nodes attempt to transmit at the same time, a collision occurs. The hardware at each node determines the varied energy level on the channel and thus detects the collision. After waiting an arbitrary length of time, each node will try again to access the channel and initiate transmission. The waiting period (though arbitrary) is unique to each node. This facility prevents subsequent collisions between the same nodes. All workstations are informed of a collision by hardware means.

The Ethernet Approach

Ethernet, a baseband LAN, is a popular CSMA/CD network. The development and testing of the Ethernet approach to LANs was a joint research project of Xerox, DEC and Intel. DECs implementation of Ethernet uses coaxial cable in a bus topology. The network can link up to 1024 nodes in a range of 2.8 kms. with a maximum transmission speed of 10 Mb/sec. The characteristics of the data link layer include a variable packet length allocation from 64 to 1518 bytes.

DEC has integrated Ethernet into the Digital Network Architec-

<table>
<tr><th>Layer No.</th><th>ISO Seven Layers</th><th>Functions</th><th>DNA Layers</th><th colspan="3">Function</th></tr>
<tr><td>7</td><td>Application (user)</td><td>Support user and applications tasks. Overall network management.</td><td>User Network Management</td><td colspan="3" rowspan="2">File Transfer
Remote Source Access
Down Line System Load
Remote Command File Submission
Virtual terminals</td></tr>
<tr><td>6</td><td>Presentation</td><td>The encoded data is translated and connected to display on terminals, screens and printers. Under user control.</td><td>Network Application</td></tr>
<tr><td>5</td><td>Session</td><td>Bridges gap between transportation layer and logical functions under operating systems. Controls system dependent aspects of communications.</td><td>Session Control</td><td colspan="3" rowspan="2">Task to Task</td></tr>
<tr><td>4</td><td>Transport</td><td>Once the path is established, the layer allows exchange of data reliably and sequentially.</td><td>End Communications</td></tr>
<tr><td>3</td><td>Network</td><td>Addresses messages, sets up paths between communicating nodes.</td><td>Routing</td><td colspan="3">Adaptive Routing</td></tr>
<tr><td>2</td><td>Data Link</td><td>Establishes an error free communications path between nodes over channel, frames messages, checks the data.</td><td>Data Link</td><td>Point to Point Multipoint</td><td>X2.5</td><td>Ethernet</td></tr>
<tr><td>1</td><td>Physical</td><td>Electrical and mechanical aspects of interfacing to medium.</td><td>Physical Link</td><td colspan="3"></td></tr>
</table>

Figure 1: 7-layer ISO model as implemented by DEC.

MEDIUM	RANGE	BANDWIDTH	(20MHz) LOSS	EMI/RFI IMMUNITY	SECURITY	COST	COMMENTS
(Shielded) Twisted Pair	<1200m <100	<100kHz <10MHz	High	Very Good	Fair	Low	Inexpensive Limited Range
Twinax	<1km	<200MHz	50–100dB/km	Very Good	Fair	High	'Controlled Impedence' can be 802 compatible
Multiconductor Flat Cable	<100m	<10MHz	High	Poor	Fair	High	Shielding available Can be byte parallel
Coaxial Cable	<2km	<400MHz	6.5dB/km 60dB/km	Fair	Fair	Very High Low	Can be 802 compatible
Fiber-Optics	2–10km	>500MHz-km	1–8dB/km	Excellent	Very Good	$1–10/m	Costs lowering rapidly
Telephone Line (PABX, PBX)	—	<60kHz	High	Poor	Poor	Low	Low Cost Installed Base
Infrared (radiation)	300m	<20MHz	High	Good	Fair	Currently High Potentially Low	(Free Space) line of sight; reduced range in fog; (moisture dependent)
Microwave (radiation)	<50km (horizon)	>100MHz	$1/r^2$	Poor	Fair	High	(Free Space) line of sight; subject to scattering; link loss depends on antenna size

Table 1: LAN media comparison. Courtesy Proteon Associates.

ture (DNA) in its DECnet products. The layers of DNA which satisfy the ISO model for Open System Interconnection are shown in **Figure 1**. The data from the higher layers of DNA pass through the data link layer to be formatted into packets and transmitted through the medium. The packet formation of data encapsulation is done at the data link layer so that data may be transmitted over Ethernet. Typically the packet format of Ethernet comprises five fields. The specifications and functions of each layer is depicted in **Figure 2**.

The transmission is initiated by the higher layers at the node. The data link layer forms a packet by arranging different fields in a proper order. The physical layer senses the traffic in the channel and signals the data link layer when the channel is clear. The physical layer serially accepts the formatted packet from the data link layer and starts transmission by sending the preamble to synchronize all receiving stations. The physical layer then transmits the bits of the packet into Manchester-phase-encoded form. During transmission, the physical layer of the sender monitors the channel. Any change in the energy level, due to collision, will be detected by the physical layer and a collision detect signal will be generated.

As soon as a node starts to transmit, all stations accept the preamble and synchronize their clocks.

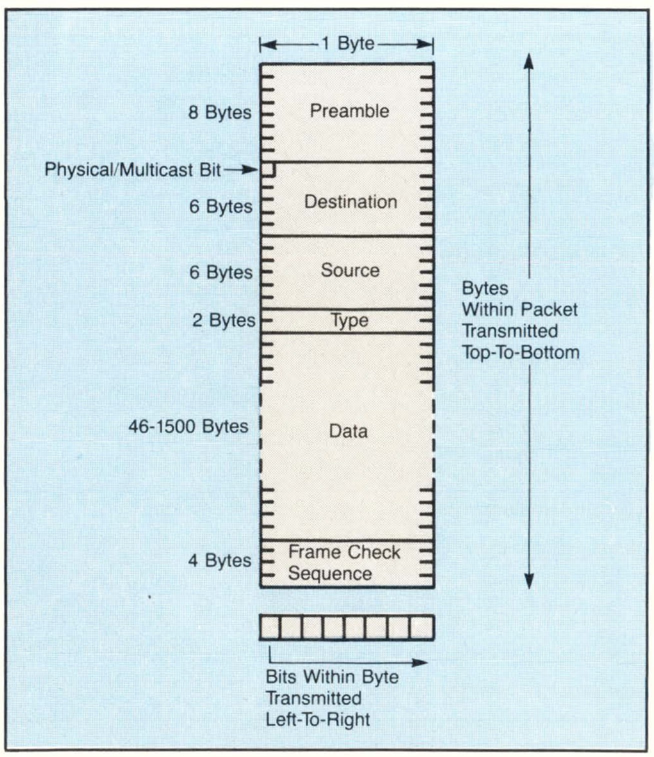


Figure 2: Ethernet Packet Format, courtesy DEC.

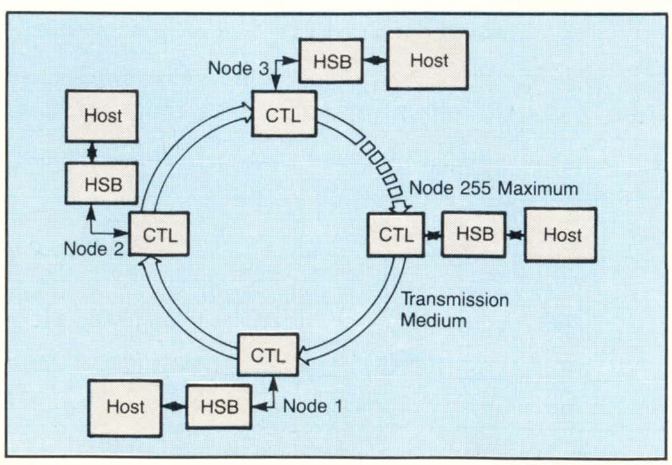


Figure 3: PRONET Ring Architecture.

The physical layer at the receiving stations then pass on the information to the data link layer where the destination address of the received packet is checked. If the packet is intended for that station the information is passed to higher layers, otherwise the bit stream to the data link layer is halted.

Interlan manufactures single board Ethernet Communications controllers to interface the host processor and the tranceiver unit. The four controllers from Interlan are available for Intel's Multibus, Digital's Q-bus, Unibus, and Data General Systems. 100 Work stations separated up to 2-5 km can interact at a maximum rate of 10 Mbps.

The Ethernet communications controller board and the transceiver unit together perform the functions of the first two layers of the ISO model. Even under 70% loading conditions the waiting time for any node to transmit is just 10 msecs.

The NT10 Ethernet tranceiver unit which connects an Ethernet controller to coaxial cable contains optional collision-detection test capability. The unit provides protection for the circuit board and shielding against electromagnetic interference. The tranceiver houses the transmitter, receiver, collision detector, and power converter.

The collision detect essentially performs as an error amplifier. When the average signal voltage exceeds the reference voltage (due to collision), a collision presence signal is sent to the host station. The host immediately orders the controller to reinitiate the attempt to transmit. Considering the speed of transmission in most cases the problem due to reinitiation is trivial. Usually the time lost due to collision is in the order of milliseconds or even microseconds.

The Token Pass Network

The other classification determined by the IEEE 802 specification is the token pass network. The token approach, which is already popular in Europe is gaining interest in the US because of its ability to outperform CSMA/CD networks under some conditions. Some of the token pass network manufacturers include PRONET from Proteon Associates (Waltham, MA), Prime net from Prime Computer, Inc. (Natick, MA), Xodiac from Data General (Westboro, MA), and IBM (Research Triangle Park, NC). The topology of the token pass networks may be either a bus or a ring.

The organization of the transmission media in a token pass scheme is fundamentally different from CSMA/CD networks. The consecutive stations are connected through point-to-point cables (**Figure 3**). Unlike CSMA/CD, the network and the interfaces used in token pass networks are active. The token, a special bit pattern, keeps circulating around the ring in a particular direction when there is no traffic in the channel. The right to use the channel by each node is in a predetermined order. A node attains exclusive access to the network only on capturing the token.

VLSI Ethernets

VLSIC technology has resulted in the production of an IC for both the data link and physical layers of ISO's open systems model. In early 1980, the specifications of the IEEE 802 standard, according to Mostek, was not firm enough to base a VLSI C chip design on. Moreover, it was not possible to build a controller that would operate at the high data rate of Ethernet (10 Mbits/sec). Hence, Mostek offered a solution in the form of a high performance N-channel MOS VLSI C for the protocol controller.

Ethernet, as incorporated by Mostek, has two components: the Local Area Network Protocol Controller (LANPC) with on-chip DMA and the bipolar Serial Interface Adapter (SIA). The functions of SIA includes encoding and decoding of the Manchester data stream and interfacing to the Ethernet cable connector. The LANPC, on the other hand, monitors the data link layer which includes serial to parallel connection and address recognition. The LANPC also houses the 48 byte FIFO.

Intel's solution to Ethernet also has two VLSI circuits, one for the data link layer and other for a part of the physical link control. The Local Communications Controller (LCC) (82586) which handles the data link layer, is user-configurable to a 8 or 16 bit data bus. This provision allows the LCC to be directly interfaced to 8 or 16 bit processors from Intel. The 82586 consists of two units: The Command Unit and the Receive Unit. The function of the Command Unit is to execute the host CPU commands and the tasks of the Receive Unit include buffer management, address recognition and cyclic redundancy checking. The interaction between the CPU and 82586 takes place through a

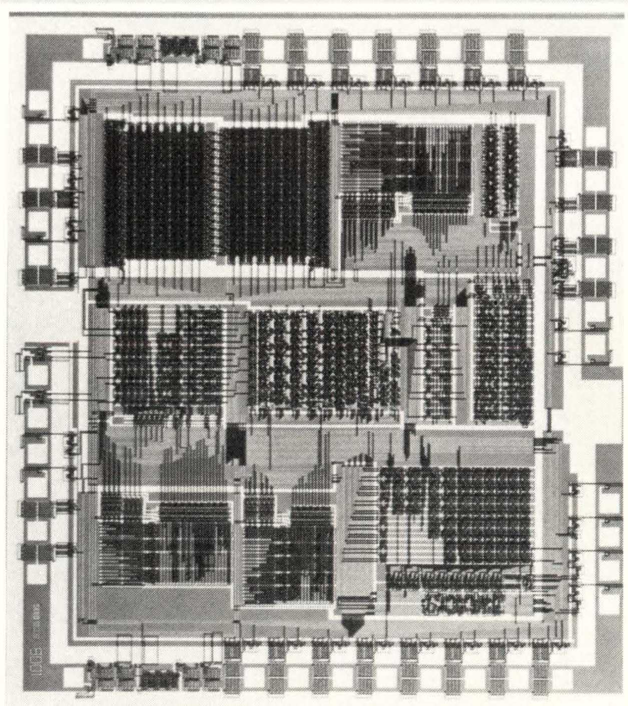
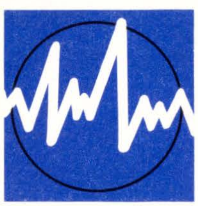


Figure 1: 8001— Ethernet Data Link Controller performs functions of data link layers of ISO model. Courtesy Seeq Technology, Inc.

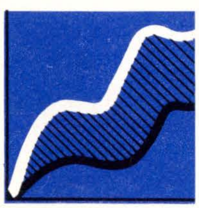
Make sure your disk drive bearing has these six critical characteristics.

Today two great challenges face the designer of computer systems: performance and reliability. The right disk drive bearing plays a critical part in seeing that both of these challenges are fully met. Here are its characteristics:



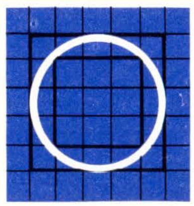
1. Low Vibration Level

High-density magnetic disk spindles require high dynamic accuracy. Hoover-NSK makes bearings specifically for that level of accuracy. We can provide the spindle designer with the dynamic characteristics of a bearing, so that resonance with a particular spindle frequency can be avoided.



2. Long Life

Durability testing has shown that nothing outperforms Hoover-NSK's combination of vacuum-degassed high-carbon chromium steel and Super Finish surface honing. Add a special filtered lubricant, and you have a bearing capable of outlasting its application.



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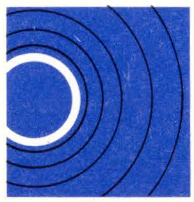
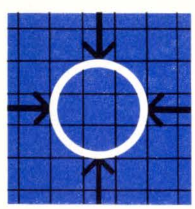
The more perfect its raceway roundness, the more perfectly a bearing will run. Hoover-NSK establishes its prototype characteristics using equipment that detects runout deviations as small as 1 microinch. This equipment enables us to set manufacturing parameters that maintain or exceed ABEC 7 standards, even in large production runs.



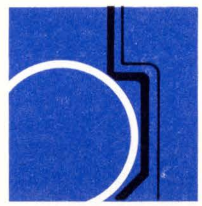
4. Low Noise Level

Bearing noise can have a substantial effect on performance. Hoover-NSK employs an anechoic chamber to establish noise levels for its prototypes and to test production samples. The result is a disk drive bearing capable of performing to levels as low as 30 db.



5. Minimum Torque

Starting torque generated by most bearings can eventually ruin a DC brushless motor. Hoover-NSK has minimized this problem in two ways: first, through manufacturing techniques that produce a virtually frictionless bearing; and, second, through the use of an exclusive patented V Labyrinth Seal. This seal retains the lubricant without actually contacting the bearing inner ring.



6. High Lubricant Integrity

In some cases ordinary bearing-seal designs can permit the volatile compounds of a lubricant to evaporate. Hoover-NSK has developed a special contact seal for these applications. When paired with a V Labyrinth Seal, this combination provides excellent lubricant integrity and maintains low torque characteristics.

Send for your copy of the Hoover-NSK Design Reference Guide for Disk Drive Bearings. It contains all the information you'll need for proper design and specification, including data not normally easy to find.

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shared memory structure called the System Control Block (SCB). The Command and Receive units are controlled and monitored by the host CPU through the system control block. The System Control Block contains pointers to two other memory structures, the Command Block List (CBL) and Receive Frame Area (RFA). The CBL and RFA hold lists of commands to be executed by LCC and hold all received frames respectively. The SCB also has status registers and counters.

The host CPU loads the shared memory with the data to be transmitted. The other memory blocks inform the LCC where the actual data buffer locations are located. When the CPU is to receive data it makes room in the shared memory. As data packets are received, the 82586 checks for both errors in the information field, and exact numbers of bytes received. It also checks if the received packet meets the protocol requirements. The pipelined architecture of the 82586 allows the above functions to be performed simultaneously and supports task completion more quickly.

The other features of the 82586 include 4 on-chip DMA channels for efficient transfer of data, serial transmission from 100K bps to 10M bps and an independent 8 MHz system clock input.

The other chip which performs most of the function of the physical layer is the Ethernet Serial Interface (ESI) (82501). The 82501 is directly pin compatible with 82586. Like the SIA of Mostek the ESI also performs noise filtering and Manchester decoding. When in receive mode, the ESI provides signals to the LCC indicating the presence of data to be received. When in transient mode, the ESI informs the LCC of collisions, if any.

When the node is transmitting, the ESI (after receiving data from LCC) performs retrieving, Manchester encoding on the data stream, and passes the information to the communications channel.

The 82501 also performs functions like diagnostic loopbacks for fault detection and isolation and prevents continuous transmission in case of any channel error.

Seeq Technology offers two types of Ethernet Data Link controllers (EDLC) to perform Data Link Functions. The 8001 and 8003 EDLCs perform medium access control, data capsulation, data decapsulation and error detection functions. The physical layer functions, carrier sense, collision signal detection and data encoding and decoding are performed by the 8002 Manchester Code Converter.

The 8001 and 8003 EDLCs are both single 40-pin NMOS VLSI devices with a capacity to transmit up to a speed of 10 MHz. These devices are provided with a universal system interface which will interface with most μPs, and μCs. The difference between the 8001 and 8003 is basically in the application. The 8001 has direct provisions to be interfaced to FIFO where as 8003 is suitable for DMA interface.

The 8002 MCC comes in a 20 pin DIP and is manufactured in CMOS technology. The chip has both analog (phase-locked loops, preamplifiers, etc.) and digital circuits, making CMOS a more appropriate technology for its implementation. The 8002 performs Manchester encoding by exclusive-ORing the clock and data prior to transmission, and decoding by deriving the clock from the data with a PLL and exclusive-ORing, this time with the incoming signal, thus recovering the original data.

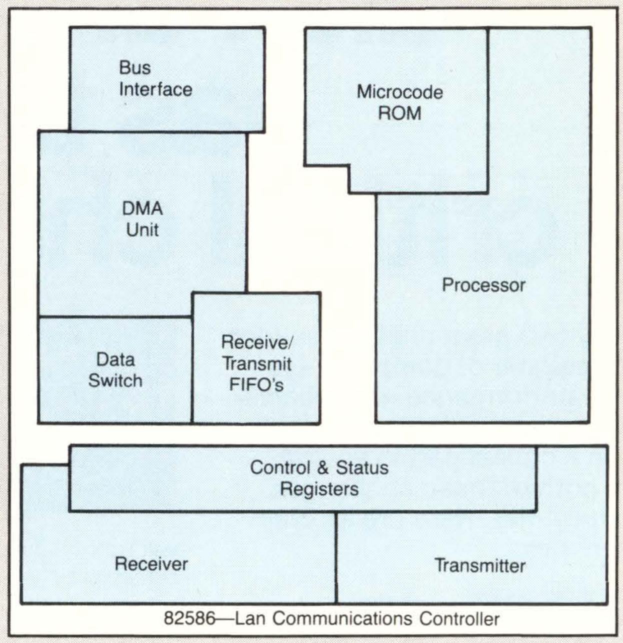


Figure 2: 82586—VLSI Local Area Network Communications Controller from Intel.

The data link layer of the ISO model is implemented by Fujitsu with advanced CMOS technology. The MB8795A is the Ethernet data link controller configured in two sections—transmitter and receiver—each with its own client layer parallel interface port. The collision is detected by the "Time Domain Reflectometer" function of the device. The MB8795A uses a 14-bit counter which counts the number of bits transmitted in each packet. The counter is cleared at the beginning of each transmission and counts bits from that time until the carrier drops or a collision happens. The purpose of the function is to provide a rough measure of the distance of the unit on the network to some cable fault, either an open or short on the coax.

Fujitsu implements the physcial layer functions through MB502A Encoder/Decoder—a low power bipolar Schottky device. Apart from Manchester encoding/decoding functions, the device interfaces to the baseboard coax cable transceiver and handles the signal distortions.

The application oriented layers of the ISO model handle functions like error control, buffer management, etc. which means that it is entirely up to the user to make the interface work. However, when it comes to hardware, VLSI technology supporting LANs has resulted in a global compatibility with various CPU's available in the market today.

To initiate transmission, a node first receives the token and transforms it into a connector. The connector also forms the beginning of message (BOM). The BOM is followed by destination address, source address, the data and end of message. The entire sequence comprises the data format. Finally, the sending station places the token back on the ring.

When a node is transmitting, the other nodes in the ring are responsible for identifying the message. If the message is addressed to it, the node receives the information. If not, the node repeats the message and passes it on to the other nodes.

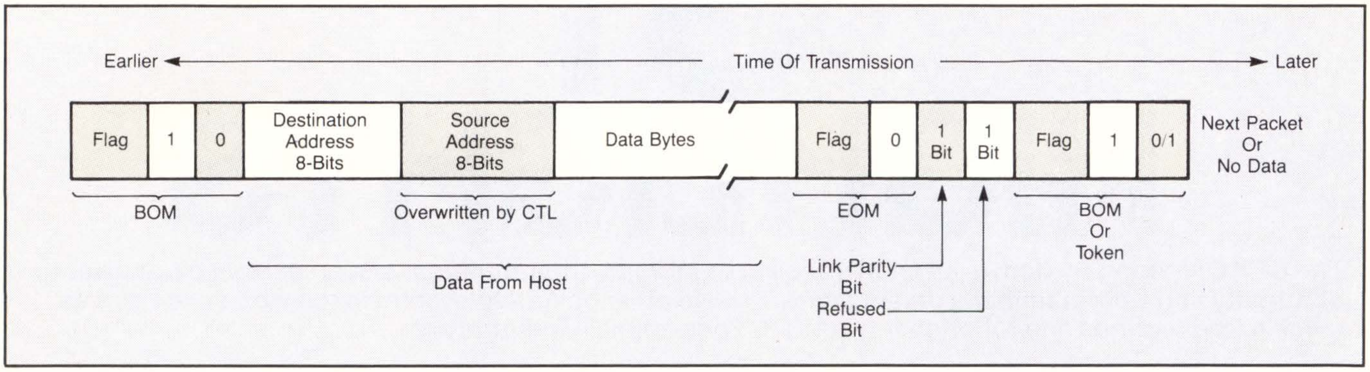


Figure 4: Data Encapsulation Format of Ringnet works, courtesy Proteon Associates.

The ring interface operates in two modes: listen and transmit. In the listen mode, the interface checks if the receiving bits form a token. Once the token is tranformed into BOM, the ring interface switches to transmit mode. Since the change over from listen mode to transmit mode happens in 1-bit time, the ring interface is usually supported by a buffer to store a few packets of information.

Ring Networks

Unlike CSMA/CD networks, ring networks are free of collision. The ring network architecture from Proteon Associates known as PRONET, has the capacity to support 255 work stations per ring. Even under full traffic conditions data is sent at a rate of 9.94 Mbits/sec. The transfer rate is limited by the host bus bandwidth. Furthermore, PRONET is compatible with different media on the same network. Three different PRONET models are available for three popular busses: Digital's Unibus, Q-bus and Intel's Multibus.

Each mode in the PRONET architecture consists of a ring control board (CTL) and host specific board (HSB). The tasks of CTL includes network control and signed modulation/demodulation. The HSB module houses a full duplex direct memory access (DMA) interface to the host bus. The HSB is designed to minimize the software burden on the host. Two complete DMA controllers on board allow full duplex operation. Both DMA transfers from host to transmitter packet buffer, and receiver packet buffer to host, are simultaneous.

The data encapsulation is done at the data link layer. The data format is shown in **Figure 4**. As much as 2044 bytes of data (1022 words) can be encapsulated. The link parity and refused bits perform maintenance/acknowledgement functions. The control characters of PRONET, viz. source address, destination address, BOM, EOM, and token are uniquely defined. If a character in the data stream happens to be similar to any of the control characters, bit stuffing is performed. The de-stuffing of the extra bit is automatically done at the receiving station.

The error recovery scheme of PRONET uses three hardware timers. The token timer sends "ring not OK" status signal to HSB. The flag timer along with "ring not OK" reports an absence of a control character on the ring. The third timer known as a "message lost timer" informs the host if a message is not returned to the sender. This only happens if there is a cut in the ring. If the token is lost due to any such discrepency the ring is reinitialized. The reinitialization is done by any of the hosts by placing a token on the ring. If two hosts attempt to reinitialize at the same time, a collision occurs and the stations try again after an arbitrary length of time.

The low error possibility is attributed to the one-to-one connection between the nodes, and each connection is a terminated, properly connected, matched network. This means that optical fibers are best suited as the medium of communication. Since the connections are one-to-one, the medium of two subsequent links can be of different materials.

Ring networks have a distinct advantage over CSMA/CD networks in collision free performance. On the other hand, the CSMA/CD approach allows faster transmission. If, for example, station A is transmitting to station B, the message has to travel from A to B to all other nodes in the ring and finally to A. This makes the ring networks slower. Furthermore, the right to access the transmission medium is random and quicker in the case of CSMA/CD networks since the node need not wait for a token as in ring networks. The advent of Ethernet chips has made them compact but expensive. The FPLA (Field Programmable Logic Array) technique, implemented by Proteon Associates, provides reliable ring networks at a lesser cost. The dual redundant ring networks from Proteon Associates perform in spite of breaks in the ring, since subsequent nodes can form a ring, a feature made possible by two way links between subsequent nodes in the ring.

In the event of a collision in the channel, the transmitting nodes of CSMA/CD networks that do not know about the collision will continue to send messages. This deficiency in CSMA/CD networks is overcome in token pass networks. The characteristics of the token network are that only that node that has the token can utilize the network. During this time, the other nodes can only listen to the network. Since

Globally Compatible LAN Architecture To Perform In A MultiVendor Environment

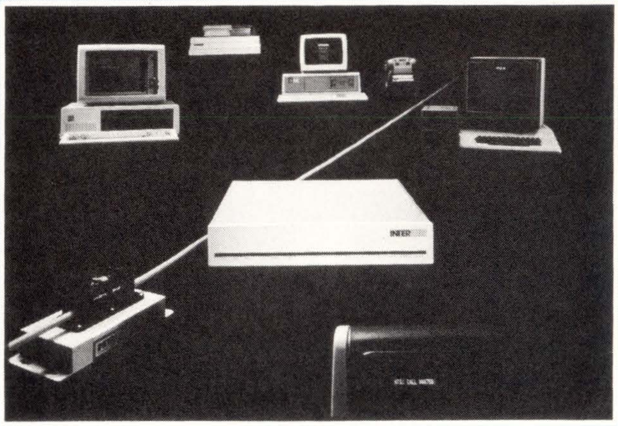
Most LAN devices available today cater to the requirements of a particular manufacturer. In order to make the LAN globally compatible Interlan (Westford, MA) released a networking architecture to function in a multivendor environment known as NET/PLUS. The network is designed to meet the Ethernet IEEE 802.3 CSMA/CD industry standard.

A variety of computer systems such as DEC's VAX and PDP family, Data General's Computers, and Intel's Multibus Systems, are supported by the NET/PLUS communication controllers. The performance of NET/PLUS is achieved through a Network Terminal Server (NTS 1D) and Multi-Vendor personal computer Networking Software.

The NTS 10 is an interface between any EIA RS232-C asynchronous serial I/O device onto the Ethernet LAN. The hardware of the NST 10 consists of Intel's iAPX 186 (80186) and Intel's local communications controller (82586). The device, however, establishes only visual circuit connections allowing easy electronic switching. The terminal server is fabricated in four or eight port units to suit different applications.

The other functions of the NTS 10 terminal server include two types of virtual connections: switched virtual circuits and permanent virtual circuits. Typically the types differ only in the method by which connections are established and terminated.

When in swtiched virtual circuit mode a workstation can create a logical connection to another device on the network by issuing a call command to the NTS 10. Once connected, either of the nodes has the capability to disconnect. But the node that caused the connection has the added privilege that the NTS 10 supports multiple open connections per port. By issuing "Switch" and "Resume" commands, a terminal user can switch between the different connections that were previously established. The permanent virtual circuit connection, on the other hand, is established and terminated by a network manager. An example of this connection is the establishment of a permanent connection between a printer and a computer port.



NTS 10 offers a LAN solution to global compatibility.

SYSTEMS SUPPORTED BY NET/PLUS

Personal Computers	Microcomputer Development Systems	Mini-Computer
Apple II (DOS)	Intel Series I and II	Digital VAX
Apple II (CP/M)	Motorola Exercises	" RSTS/E
Digital DECmate II		" RSX-11M(+)
Digital Rainbow 100		" RT-11
Digital P350		
Digital VT/180		
IBM PC (MSDOS)		
IBM PC (CP/M-86)		
Televideo 802		
TRS-80 Model II		
Xerox 820		

An interesting feature of the NET/PLUS is the ability to support a variety of computer systems which include personal computers, microprocessor development systems and mainframe systems (**Figure 1**). The Multi-Vendor Personal Computer Networking Software is made possible by incorporating body-TRM and poly-XFR packages of Polygon Associates, Inc.

The poly-TRM package converts a PC into a terminal that can make connections on the network and log on host computers or other devices. The package facilitates transfer of ASCII files between a PC and a host. The poly-XFR package provides transfer of binary data files and ASCII text files to and from another system running in poly-XFR software. This is accomplished by dividing the file into "packets". Each packet is sent with a sequence number and a CRC error checking value. The flexibility is due to software device drivers in the NET/PLUS that allows applications programs running under a variety of operating systems to interface with the appropriate Interlan Communications controller.

the token networks are synchronous, each workstation can access the channel within a predetermined period of time.

Nodes in the ring networks are usually connected to the channel through electromagnetic relays. If the node experiences any malfunctioning (e.g. a software problem at host, power failures, or broken cable between host and ring) the relay is immediately de-energized. This makes the token or the data stream by-pass the defective node. In networks involving a number of nodes, token pass networks are likely to consume more power than CSMA/CD networks. The synchronous nature of the token pass scheme makes it prone to error. IBM uses concentrators in their ring network architecture to regenerate lost tokens. In the event of a failure in the node, the concentrators set up a by-pass around the defective node.

One other advantage of token pass networks is that unlike CSMA/CD LANs, the token approach is not a function of the length of the communicating channel and the transmission rate (whereas the CSMA/CD networks can detect collision only within a certain distance).

However, considering the fact that a number of interface products are available for Ethernet LANs, it appears the inherent defect (collisions) is considered trivial by the manufacturers. Ethernet chip manufacturers include Intel, Mostek, Seeq Technology, Inc., 3Com, Ungermann-Bass, Fujitsu, Advanced Micro Devices, Digital Equipment Corporation, etc., whereas there are only a few chip manufacturers for ring networks. The rapidity with which the cost of ICs is declining may further popularize Ethernet.

Conclusion

So far, hardware supports the lower two layers of the open system interconnection model of ISO, and the software protocols that are available have made the entire process of networking very efficient. The rapidity and volume of data that is to be processed in applications such as robotics and computer graphics necessitates the services of different processing elements to yield high performance. The VLSI and FPLA techniques have reduced the entire interface between workstation and medium of communication to just a couple of boards. Parallel advancements in the media include fiber optics and infrared channels, removing bandwidth limitations. Furthermore, satellite communication techniques can reliably link two computers from geographically distant locations.

There has been a significant breakthrough in the software too. Networking software that caters to the upper layers of the ISO model, is available from many different vendors. This means there will most likely be reductions in the cost associated with each workstation. What remains to be seen is the outcome of an efficient media for transmission. Though the coaxial cables are quite popular now, they lag far behind fiber optics in the matter of immunity to EMI and RFI. A technological breakthrough in terms of cost is expected soon in this area. Therefore, whatever has been achieved until now in local area networks is just the beginning. □

Ada For Large-Scale Software Systems

by Michael R. Gardner, Ph.D.

In sponsoring the design of Ada, the US Department of Defense was concerned that the new language be suitable for use in embedded military computer systems. However, Ada's designers included many features which make the language useful for large-scale software systems, regardless of the area of applications.

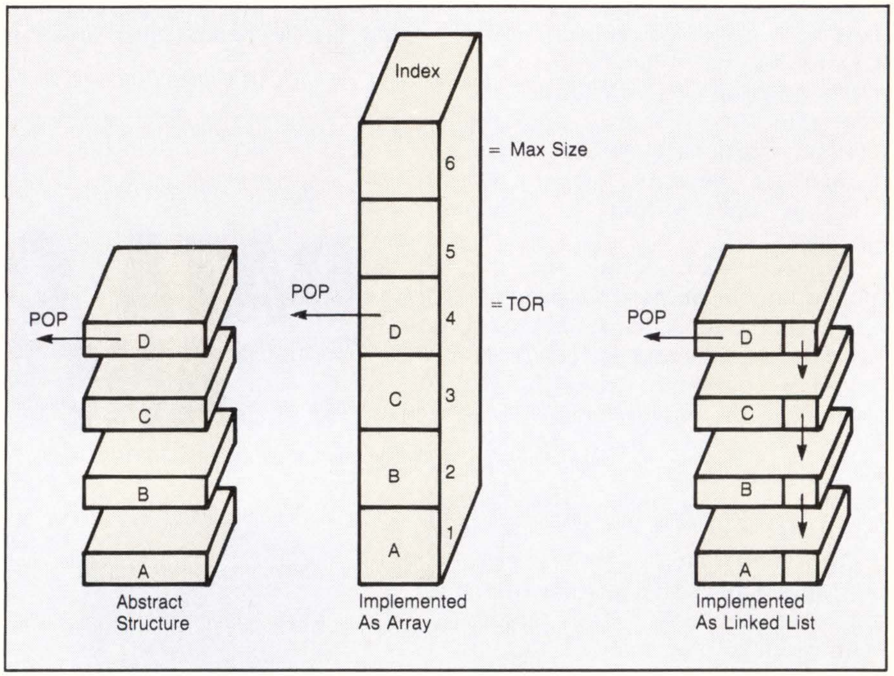


Figure 1: Three conceptions of a stack.

Consistency

The package is Ada's single most useful feature for projects involving thousands of lines of code and several programmers. A package contains a set of declarations and subprograms designed to solve a group of related problems. It can be used by several programs, each of which needs to solve some or all of these problems.

The contribution of Ada's package concept to software design is the way abstraction and information hiding are built into the language.

For a single project, such as a payroll system, one can place declarations and subprograms needed by more than one program in a package; in this case, all the declarations of the record-types for all the payroll-related files. The Ada compiler checks everyone's program for consistency with the shared declarations of identifiers and subprograms.

Well-designed packages also promote uniformity of interface with the user. For example, every program using Intellimac utility packages will enforce the same syntactical requirements for the user's entry. For example, a date or dollar amount entry will write the same error messages for the same errors, and will write them on the same place and display-mode on the screen. This uniformity across programs makes it easier to learn to use a system.

Productivity

The use of packages also promotes programmer productivity, since a given version of a package needs to be compiled only once. Separate compilation has been available for some time with older languages such as Fortran. The novel contribution of the Ada package concept to software design is not this, but the ways in which the software-engineering principles of "abstraction" and "information hiding" are built into the language.

Abstraction is the separation of the functionality of a program unit from the details of its implementation. This serves two main functions: first, it reduces the amount of complexity and detail one copes with while working on a problem; second, it makes it possible to change the way a given capability is implemented without affecting the code using the capability.

Abstraction is especially important in a large-scale project, where it is helpful for one programmer to be able to use the work of another without understanding all of its details. In stacks, one should not have to think about links or array indices when using Push or Pop; nor should one's uses of these operations depend upon their implementation.

Abstraction is realized in Ada by

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means of the distinction between a package's abstract "specification part" and its "body." A specification part contains the declarations and subprograms accessible by code outside the package. To use another programmer's package, it should be sufficient to read the brief specification part. The rest, the package body, should only contain details of how the specification part is implemented. Since the package specification part is at a higher level of abstraction than the body, it provides capabilities which could be implemented in a variety of ways, the details of which need not concern the user of the capabilities.

If a change is made to the package body but not to the specification part, the programs using the package can use the new package object code without themselves being revised or even recompiled. Consequently, one programmer can enhance the speed or accuracy of his implementation of a process described in the specification part, without affecting either the source or object code of his co-workers who use the package.

It is often desirable to enforce abstraction by "information hiding": rendering implementation details located at lower levels inaccessible at higher levels of abstraction. Ada packages provide two main ways of achieving this sort of hiding. One is that the user of a package cannot access those of its variables or call those of its subprograms which do not appear in the specification part. This means that if he does happen to use any of the same identifiers, he will not unwittingly interfere with what occurs in the body.

The second mechanism for information hiding is the Ada facility for "private" and "limited private" types. A type is a set of possible values of a variable and a set of operations on those values. If a type declared in a package specification part is defined as private, a user of the package cannot make direct use of the structure of objects of those types. The only allowable operations upon the objects, except equality and assignment, are those declared as subroutines in the specification part. Even predefined equality and assignment are ruled out for limited private types. If a programmer has used a private or limited private type, he can then change the way in which he has implemented a given abstract structure—e.g., a stack of dynamic string—without affecting the source code of programs that are using the package.

There are two main advantages of private or limited private types. One, is that maintainability is enhanced through greater independence of separate code modules.

Strong typing provides two ways to catch errors: the wrong type will be caught at compile-time, and an out-of-range value will be caught at run-time.

The other is that with limited private stacks, no programmer can violate the designer's intentions by performing some other operation on the package. By contrast, in nearly any other language, nothing in the compiler or runtime support could prevent such access.

Ada promotes the productivity of a team of programmers working on a large-scale project by enhancing their ability to coordinate efforts. It does this by minimizing the extent to which they need to understand the details of each other's work, maximizing the extent to which their code modules are independent of each other, and minimizing the number of ways in which one programmer's work can interfere with another's.

Supplements to Ada

Packages also enable supplementing the language by adding features not required by the language specifications. For example, Ada proper does not contain dynamic strings, complex numbers, or sets, but these can be added by writing appropriate packages.

One important omission is the dynamic string. But this problem has been overcome by using a dynamic-string package.

In a sense, it is possible to "supplement" any language by creating a library of subprograms. But Ada, unlike Fortran, Cobol, PL/I, and Pascal,

- enables grouping of subprograms—for example, for the purpose of defining a new type of object and operations thereon;
- provides better control over visibility of identifiers in the library than languages which lack local variables or have nothing like a package specification part;
- allows limits on operations on an object as defense against errors.

Strong Typing

Types or sets of possible values of a variable and sets of operations on those values are important for Ada, which is strongly typed. In Ada, every variable must be declared by specifying its type, and the possible types are not limited to such standard ones as characters, strings, integers, floating-point and fixed-point numbers, but may be defined by the programmer for special purposes. Conversions between types (e.g., from integers to strings or to fixed-point numbers) are never implicit in assignment statements or subprogram calls as in PL/I, but require explicit calls to conversion functions.

When a variable is first introduced, the programmer must declare what values it can take and what operations can be performed on it. This declaration provides two ways to catch errors: a statement using one type where another is required will be caught at compile-time, and an assignment of a value which is out of range for the type will be caught at run-time. The Ada compiler helps insure that usage of a given variable or type is consistent throughout all parts of the project which use it. Moreover,

(continued on p. 123)

Product Index

To help you find the products you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a write number for additional information on that product. Bold type indicates advertised products.

(continued from p. 116)

the declarations themselves enhance the clarity of the code and thereby facilitate maintenance by programmers.

Strong typing can be negative for certain kinds of projects, such as coding a general-purpose screen-editor or report-writer. While such programs are fairly easy to write in a weakly typed language such as Basic, the fact that Ada programs must specify in advance the types they use makes such jobs more difficult.

Strong typing may also appear to be a drawback when performing essentially the same operations upon objects of different types. Each subprogram has a fixed list of parameters, each of which has a fixed type. Hence, the same subprogram-call "Put (Item)" cannot work if Item can be either a string or an integer. This problem can be overcome by "overloading"—that is, using the same identifier "Put" to refer to different subprograms which do essentially the same thing to objects of different types. The compiler can then use the type of the actual parameter to determine which subprogram is meant.

In full Ada, but not the current version of TeleSoft-Ada, one can also get around strong typing by using generic program units. If one package, for example, can be obtained from another by global replacement of a type-name and perhaps other entities such as numbers, the two packages can be consolidated into a single generic one which takes the type and other entities as parameters. Thus one could have a single package concerning stacks of characters or integers or strings, where the maximum stack-size is a variable as well.

Enumeration Types And Exceptions

In addition to types and packages, one other feature which enhances one programmer's ability to use another's source code is the enumeration type, a sequence of identifiers (or characters) which comprise the set of possible values of a variable of that type. This feature enables one to name things explicitly rather than just referring to them by number. An enumeration type can be used to index arrays and also to control loops.

Though the fields are not mere numbers, they still have a numerical order. Thus, there can be operators (called "attributes") which deliver such objects as the first or last field, or the predecessor or successor of a given field. "Fields 'first" always refers to the first field, even if the definition of the type Fields changes. Hence, the use of attributes makes program revision easier. Enumeration types and attribtues allow increased clarity and maintainability of programs, as well.

One final advantage of Ada is its exception-handling. Dissatisfaction with the handling of exceptional situations by existing languages was one reason the DoD chose not to adopt one of them. An "exception" is a condition necessitating suspension of normal program execution. When such a condition arises ("is raised"), one usually wants the error to be reported, and often wants the program to do something reasonable to get the error corrected, or at least to continue to handle subsequent cases without halting.

Enumeration types and attributes allow clarity, maintainability and ease of revision of programs.

In a program which edits, prints, or otherwise processes a series of records in a file, one can have a subprogram to process a single record. If an exception is raised during that subprogram, an exception-handler at the end of it can report what error occurred and then pass control back to the main program, which then processes the next record by calling the subprogram.

Ada exceptions can be simulated in older languages by writing "if . . . then" statements referring to possible errors and using error-codes passed as parameters by subprograms. But Ada exception-handlers are clearer, since they're separated form the normal code, and efficient since they're executed only when exceptions actually are raised.

A defect of the language specification is the lack of any simple way to report what exception has arisen. For every possible exception, an exception-handler must be written to report that the particular exception has arisen. It would be preferable to have a functon of exceptions which returns their names, so that a single exception-handler could report any exception.

Using Ada

Some critics of Ada have claimed that the language is excessively complex and difficult to learn to use in writing reliable programs.

But starting with a knowledge of such languages as Basic, Pascal, and PL/I, our programmers were able to study books on Ada and become reasonably competent in using the language in about three weeks. Moreover, they can use a subset of the language correctly without knowing the entire language. Ada's designers attempted, with considerable success, to create a language which is relatively easy to understand and remember because its constructs correspond to intuitive expectations.

While some of Ada's most distinctive features (such as tasks) suit it for military or other embedded systems, other features are excellent for a much wider class of software projects. In particular, the facilities for packages, strong typing, enumeration types and exceptions are extremely helpful in the efficient production of reliable, fault-tolerant, readable, and maintainable code for large-scale systems in any area of application. □

Acknowledgement

An earlier version of this paper appears in the Proceedings of the Sixteenth Asilomar Conference on Circuits, Systems and Computers, Copyright IEEE, 1983.

Single Board Solution To Distributed Measurement And Control

Combining the signal conditioning hardware of industrial control systems and the programming ease of personal computers, the μMAC-5000 offers a single-board solution to distributed measurement and control. The board incorporates a 16-bit microcomputer based on the Intel 8088, and expandable analog/digital I/O design, and a BASIC programming language compatible with MICROSOFT™ BASIC. To permit OEM manufacturers, system houses and end-users to customize the system for particular applications, the μMAC BASIC programming language borrows some of the structured concepts of PASCAL and ADA. Structured programming improves software development time by allowing users to add custom keywords to the language.

System Hardware

Board-level data acquisition systems have been typically assembled from a collection of bus-compatible boards. The practice of combining a microcomputer, analog and digital I/O board, memory board and communications card into a system, however, has a number of hardware limitations. Bus-compatible input/output boards, for the most part, are designed to handle high-level analog inputs, have a fixed analog-to-digital conversion speed and resolution, and are unprotected against power supply interruptions. To overcome these limitations requires external hardware.

The μMAC-5000 from Analog Devices (Norwood, MA), combines a flexible signal conditioning and data conversion design

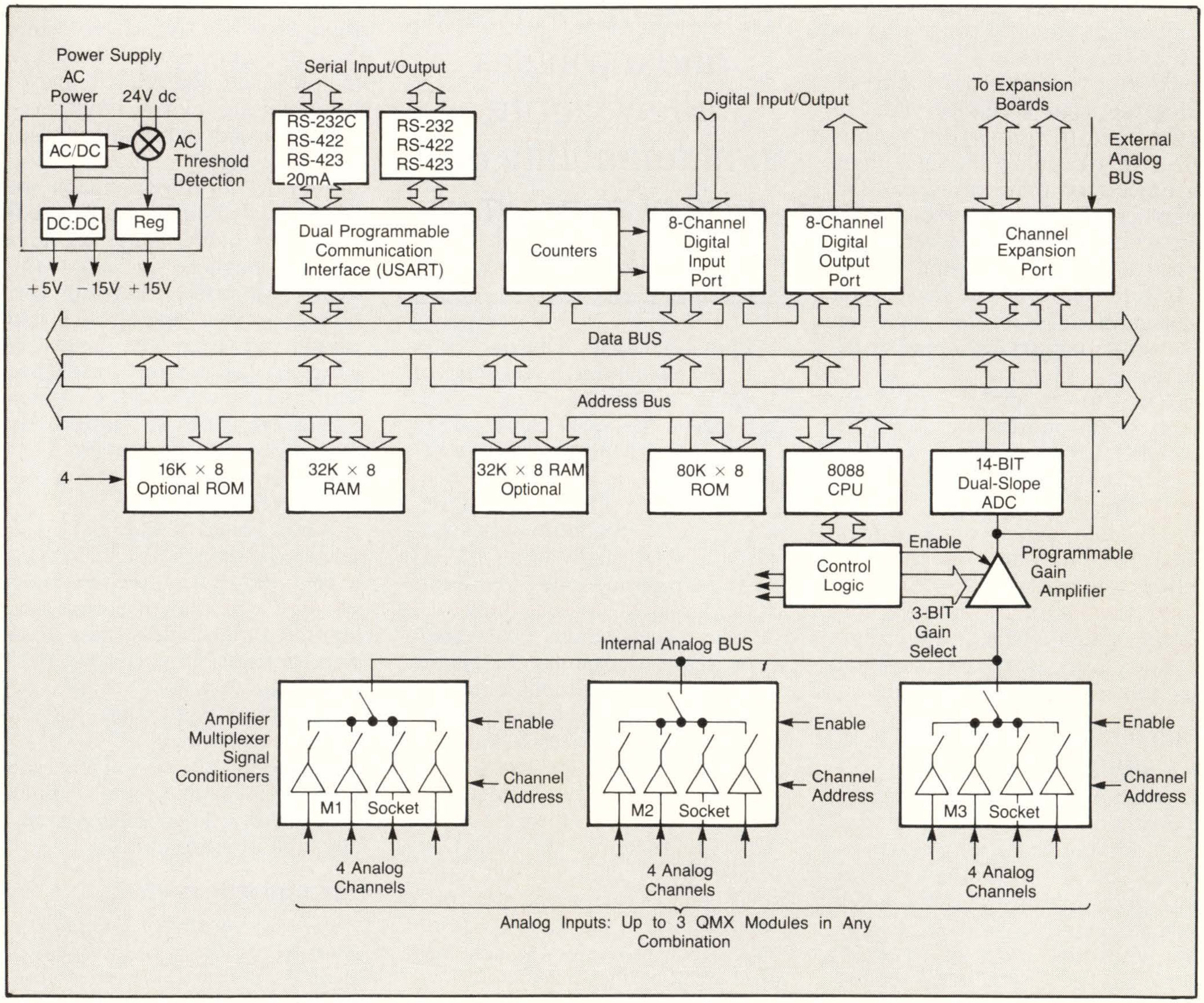

Figure 1: μMAC-5000 block diagram.

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with on-board protection against electrical faults. A master board contains the analog/digital I/O hardware, data conversion circuitry, power supply, communication and expansion ports. Mounted directly to this board is a 16-bit microcomputer, up to 64 Kbytes of battery-backup RAM and 96 Kbytes of ROM. The 12 analog input channels have three, four-channel signal conditioning modules which can be interchanged according to the sensor requirements of the application. The user attaches the sensor to the screw terminal connections, and the hardware automatically provides up to +1000V isolation, filtering, amplification, excitation for RTD inputs and cold-junction compensation for thermocouples. The system also automatically linearizes and converts the information to engineering units through built-in firmware routines. Digital inputs and outputs (of which two channels support pulse or frequency inputs) and an expansion port are available to increase the number of I/O channels.

Since conversion speed and resolution requirements can vary from channel to channel, the μMAC-5000 uses a software programmable analog-to-digital converter. An integrating converter provides to 14-bits of resolution. Higher conversion rates can be obtained with a minimum of 11 bits of resolution. Communication rates are also flexible. Selectable baud rates for a remote and local serial communication channels ease interfacing the μMAC-5000 to a variety of host computers. The two serial communications ports support RS-232C, RS-422, RS-423 and 20mA (remote port) at baud rates from 110 to 19.2K. The on-board power supply operates from either AC or battery-backup +24V dc. The system automatically switches to dc upon an ac power interruption.

Software Design

Although a number of single-board microcomputers support high-level languages such as BASIC or FORTRAN, none are directly oriented toward measurement and control applications. The μMAC-5000 supports a high-level language called μMAC BASIC. The language is an extension of Microsoft™ BASIC. To the standard library of BASIC commands it adds analog and digital I/O commands, program interrupts and a number of time-keeping commands. In addition, the programming language permits users to develop and add custom keywords to the language. The software extensions in μMAC BASIC simplifies acquiring data, processing it and sending out control signals. Rather than having to resort to low-level programming commands for data acquisition and control the programmer uses commands such as AIN, AOT, DIN and DOT for analog and digital inputs and outputs. An example of this is: **10 PRESSURE = AIN(12)**

This assigns the value (in engineering units) of analog input channel number 12 to the variable PRESSURE. μMAC BASIC also allows variable names up to 256 characters to improve program documentation. Two other major enhancements to μMAC BASIC are software interrupts and the ability to call assembly routines through a CALL statement. Two clock-based interrupts, two communications interrupts and two event-based interrupts alter the execution of the main program to branch to interrupt procedures. The software interrupts give a degree of real-time operation to the system and minimize system response times. To further improve execution speed the BASIC program can access user-written assembly language routines.

Program Development

A programmer can use a dumb terminal or any computer to develop programs. The μMAC-5000 has an on-board incremental compiler that will compile a line of code as it is entered from the terminal. The system also has a work station operating system software package, half of which resides on-board and half in a host computer. Software packages for the APPLE IIe, IBM PC and MAC 150 are available. User developed work-station operating systems for other computers take less than 100 lines of user developed code. The workstation permits the programmer to develop a program on a host computer using all of its facilities including the CRT, disk drives and printer and downloading the program into the μMAC-5000. A user can therefore write a program using a word processing package, download the program and then debug it on the μMAC-5000.

—John Sylvan, Analog Devices, Inc., Norwood, MA **Write 233**

Facit, Inc.

Dear Sir:

Facit, Inc. was listed in two locations in the September, 1983 issue of *Digital Design*. However, both listings were incorrect. In the article, "Keeping Pace With Printers," (page 88) we were listed as Facit, Inc., Greenwich, CT. We have not been in Greenwich, CT since January 1983. We are now located in Nashua, NH.

We were also listed in the article, "Tape Drives Vie For Disk Back-up Market," on page 106. Facit does not manufacture tape drives. Thank you for your cooperation.

George Bausewein
Director of Advertising
Facit, Inc.
235 Main Dunstable Rd.
Nashua, NH 03061

Stratus Computer, Inc.

Dear Sir:

Stratus Computer, Inc. was pleased to be included in the article, "Fault Tolerant Architectures" (*Digital Design*, August, 1983). However, we were somewhat disappointed at the comparative lack of detail accorded to the proprietary hardware architecture of the Stratus/32 Continuous Processing™ System.

The architecture of the Stratus/32 includes comparative circuitry and duplicate components which permit the system to continue processing despite the loss of one or more functional components. Each major printed circuit (PC) board includes two identical sets of logic circuitry. Each set performs the same operations on identical data and the results are compared. A duplicate PC board performs the same operations as its partner. If the sets of logic circuitry on either board do not produce identical results, the failed board immediately shuts itself off while operation of the sytem continues uninterrupted with the partner board. Other major components, such as disk drives and power supplies, are also duplicated to operate in parallel with a partner.

The Stratus hardware approach enables the company's systems software developers and its customers' programmers to develop software without the need to take account of the special software techniques inherent in software approaches to fault tolerance. This feature improves the productivity and efficiency of such programmers and makes it easier to convert previously developed applications to run in a fault tolerant mode. This architecture also eliminates the software overhead that can consume processing capacity of a system using a software approach.

The Stratus/32 has other important features in addition to fault tolerance. It is modular in design, permitting system expansion without the replacement of existing hardware or software and without interrupting operations. An entry level system consists of a single processing module with 4 million bytes of memory and 60 million bytes of disk capacity and is priced at approximately $140,000. A processing module can be expanded to contain up to 16 million bytes of memory, 16 disk drives with a total capacity of 4.5 billion bytes and 64 communications ports. A system can be expanded to include up to 32 processing modules using StrataLINK™, a high-speed interface, and multiple systems can be connected in a network using standard telecommunications facilities with StrataNET™ software. Processing modules can also be connected to IBM or other manufacturers' computers through industry standard communications protocols.

In summary, the Stratus hardware approach to fault tolerance provides several advantages over other approaches that readers of *Digital Design* will appreciate.

William E. Foster
President
Stratus Computer, Inc.
17–19 Strathmore Rd.
Natick, MA 01760

Terminal Design With The 8052

A basic challenge in designing terminals is how to handle arbitration of the CRT peripheral controller and the microprocessor accessing video memory. With some systems, such as the 8275 or 8276 CRT controllers, the CRT controller interrupts the processor when it needs one row of characters. This happens every 60 ns. Consequently, the design usually includes a DMA controller to feed one row of characters to the controller quickly so the microprocessor can resume its control program. Another approach is used in 6845-type systems where the CRT controller gets video characters itself from memory as needed. In this approach the microprocessor shares memory read cycles with the CRT controller. As a result, logic is necessary to arbitrate accessing video memory from the processor or CRT controller. Some processors have an on board signal for this, but this requires faster memory speeds than the row buffer approach.

The 8052 provides a highly integrated solution to the multiple peripheral needs which was not possible with earlier less powerful single chip processors. The terminal serial requirements can readily be handled by the serial port. This supports asynchronous communication at a variable rate, as determined by an internal dedicated 16-bit timer driven from the internal clock. Variable rates from 110 to 38K baud are obtainable by loading values under software control. The port causes an on-chip interrupt when a byte is received or transmitted. Received characters are double buffered. This way fast interrupt responses are not required in avoiding overwriting received characters.

The on-board interrupt controller provides five interrupts. Each one can be enabled and prioritized (two level) under software control. One interrupt source is the serial port, as mentioned earlier; two others are internal timers. One of these controls DMA. The other timer interrupt can be used as a slow timer, e.g. 50 ns. Each interrupt causes the keyboard to be scanned for changes in keys depressed.

There are two external interrupt sources which are inputs to the 8052. One will be used to initiate a DMA request for the CRT controller. The other interrupt is also from the CRT controller, but is used to indicate an end of vertical scanning which causes resetting the row pointers for DMS.

The 8052 memory includes 8K of ROM, which should be more than adequate for most "dumb" terminals. Also, 256 bytes of RAM provides many features, including a variable length stack for saving data by PUSH and POP instructions for subroutines. Also there are four banks of eight registers in RAM. By one or two simple bit set instructions, the working bank of registers is changed.

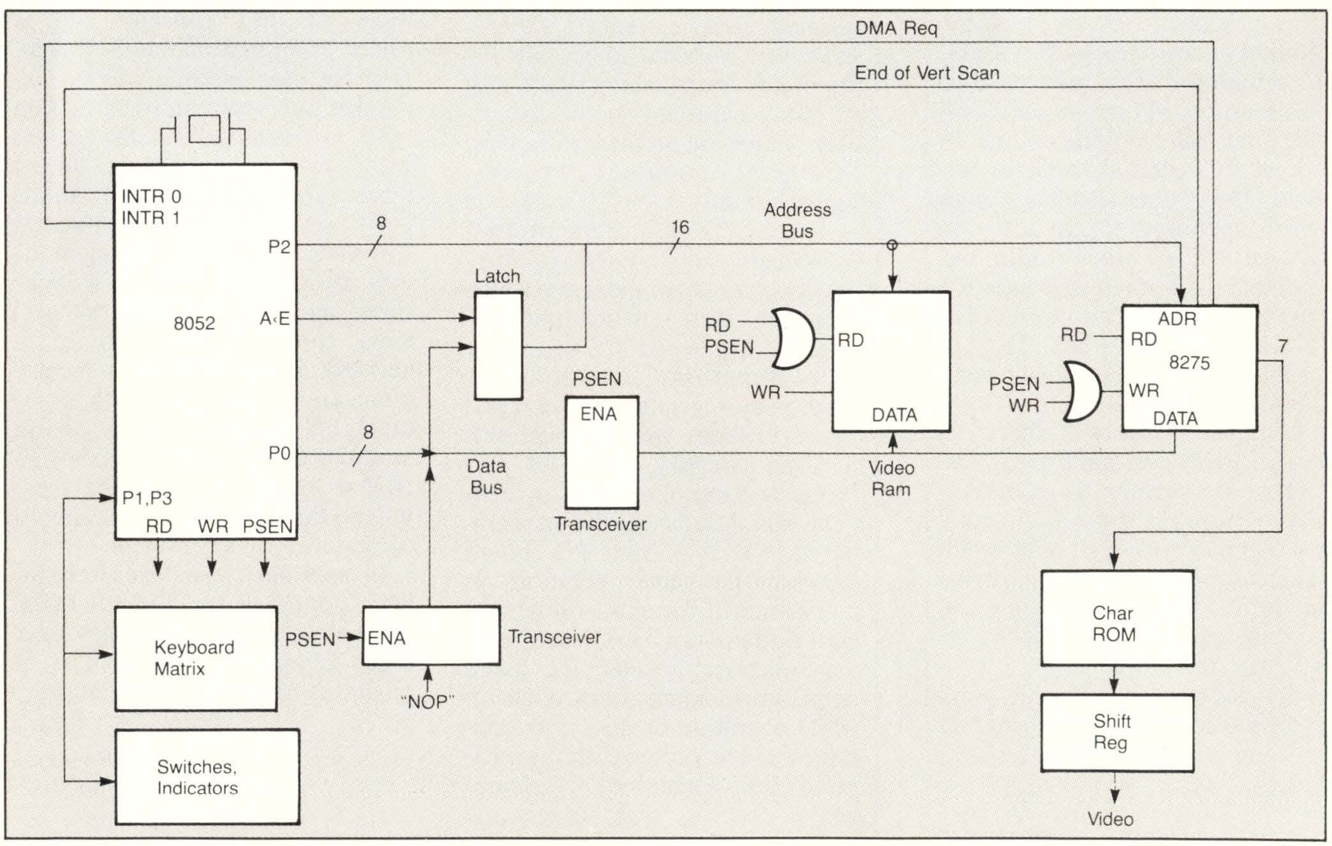


Figure 1: 8052/8275 block diagram. (Positive true logic signals shown for conceptual illustration).

This is useful for quick context switches to interrupts or subroutine calls. For a terminal this may be necessary for quick servicing of DMA requests, where pointers must be re-adjusted to reference a new row. **Figure 1** contains a block diagram of the terminal. General I/O pins are used for scanning the keyboard matrix, reading terminal configuration switches such as baud rate and outputting to LED's or audible alarms for terminal status.

DMA is accomplished with minimal SSI "glue". The overall operation is as follows: On power up, blanks are first written to the video RAM by the 8052. After that, characters are written to the 8052 as they arrive at the serial port or read from the keyboard.

The CRT controller, an 8275 (or lower cost 8276) is "fed" 80 characters by DMA. These characters go to an internal 8275 buffer for generating dot signals for all the horizontal scan lines in that row. The 8275 has two internal row buffers so one buffer can be used to generate video out while the next row is being filled.

The DMA operation is simple. Whenever the 8275 requires a row of characters, it interrupts the 8052. Internal memory has an initialized 16 bit pointer to the proper row to be refreshed. The program counter then jumps to that location. When this happens, the 8052 senses the memory address is beyond the internal 8K and automatically activates the PSEN signal. Normally PSEN (Program Storage Enable) would be a read signal for program memory. But rather than enabling an external ROM, PSEN enables a transceiver to the 8052 data bus which jams a dummy "NOP" instruction. Also the 8052 data bus is blocked to the video RAM and 8275 so the dummy "NOP" is not seen by them.

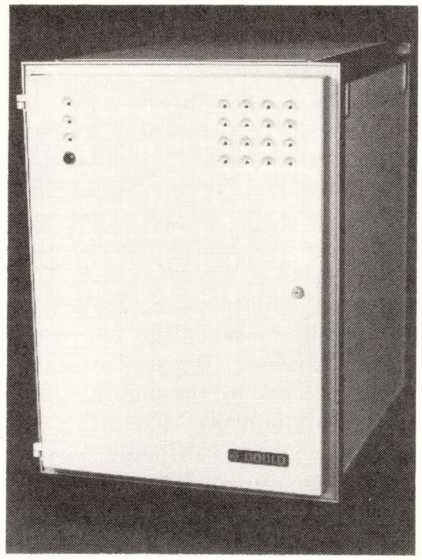
At the same time, PSEN is allowed to strobe the video RAM read input and 8275 write input. The net result is that the processor continues to increment its address while reading "NOPS" and the video RAM outputs data to the 8275 for the character row. The speed of DMA by this technique is 2 MHz for a 12 MHz 8052 clock. Slightly slower clocks will be necessary to meet 8275 timing. By now you may be asking, "how does it all stop?" Remember the 8052 has timers on the board which can cause interrupts. Also the timer "ticks" are directly related to memory cycles. As a consequence, an exact number of external "NOP" or DMA cycles can be set up. (Note that actually two DMA cycles occur per instruction cycle since the 8052 has a prefetch queue for faster throughput.)

—*Steve Mihalik, Intel Corp., Phoenix, AZ.*

Write 234

CACHE DISK ACCELERATOR

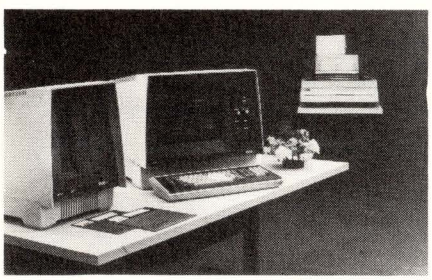
1 mSec Access Time



The Cache Disk Accelerator from Gould Inc., Computer Systems Division, is designed for their Concept 32 line of super minicomputers. The subsystem supports eight disk drives which can be any combination of 40, 80, 160, 300 and 600 Mbyte storage modules. The accelerator is useful in applications which require extensive disk I/O because it provides 1–16 Mbytes of cache memory on a microprocessor based controller. Specifically, a write operation is completed as soon as the CPU transfers data from main to cache memory (in the controller) rather than when it is written on the physical disk. During read operations, the cache memory stores programs and data files. The accelerators' moving head disk has an average access time of 2msec and the system has specific applications in transactional systems, large data base applications, CAD and image teleprocessing. Price is $77,000. **Gould**, Ft. Lauderdale, FL **Write 154**

DATA PROCESING SYSTEM

256 Kbytes Memory



The Model 21/10 is a single station data processing system that features 256 Kbytes of memory, SDLC communications, and an 80 cps printer. The system has 5 to 15 Mbytes of fixed disk storage and double-density diskettes with 1 Mbyte capacity. The 21/10 also supports 40, 45 and 120 cps printers. Price is $6,000. to $20,000. **Mowhawk Data Sciences**, Parisippany, NJ **Write 138**

RASTERIZING COMPUTER

Connects Tektronix Printer To Graphics

The UI—100T computer connects the Tektronix 4691 ink jet printer with any color graphics capable host computer. No color terminal is required for printing the image. The UI-100T accepts graphic commands from the host computer over an RS-232 serial ASCII line and converts the commands into a raster format which is transmitted to the 4691. Resolution is 140 × 150 dots/in. The UI-100T includes software-selectable resident fonts (six included in the standard configuration). Price is $9,950. **Lasergraphics**, Irvine, CA **Write 140**

DEVELOPMENT SYSTEM

616 Kbytes Storage

The KDS-908 development station features dual 5¼″ floppy disk drives with 616 Kbytes of storage which are integrated into the terminal. It contains a Z80 CPU, 256 Kbytes of RAM, two RS-232 ports, a Centronics-compatible printer port and four expansion slots. The KDS-908 runs CP/M, version 2.2 and can be used as a single-user system, a station on a KDS-901 CP/NET development system network, or as a terminal on the KDS-968 UNIX system. Price is $6,500. **Kontron Electronics,** Culver City, CA **Write 131**

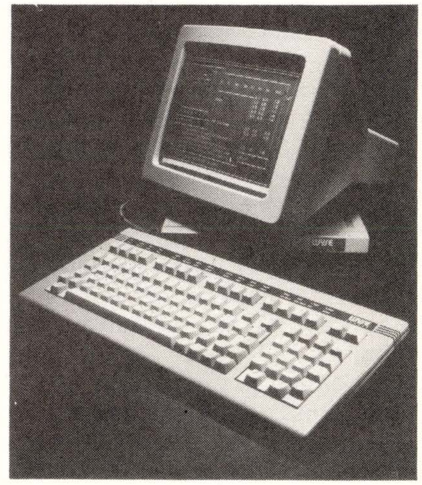
TERMINAL CONVERTER

64 Kbytes NMOS

The TC3278 universal terminal converter is a self-contained microprocessor-based system that turns an IBM 3278 or 3178 terminal or IBM plug-compatible terminal into a stand-alone workstation with personal computing capabilities. It allows terminal users to maintain their existing connection to the IBM host computer, and by emulating asynchonous terminals like the VT 100, provides access to other host computers within the organization. The TC3278 has a Z80A microporcessor with 64 Kbytes of RAM and 16K of ROM. It features two RS232-C compatible ports and two coaxial interfaces. There is a serial printer interface on the main processor board. **Avatar,** Westboro, MA **Write 148**

DISPLAY TERMINAL

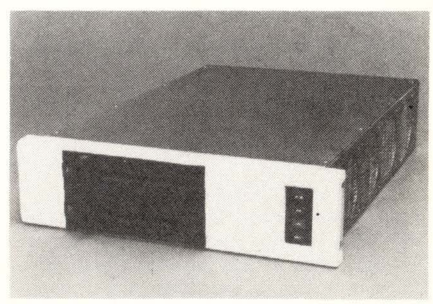
132 Column Capability



The WY-50 and WY-75 are smart editing alpha-numeric terminals which feature 14″ screens with selectable 80 or 132 column widths. The terminals include nonvolatile memory which enables terminal parameters such as cursor type, transmission speed and operating mode, to be entered from the detached keyboard. Prices are $695. (WY-50) and $795. (WY-75). **Wyse Technology,** San Jose, CA **Write 134**

WORK STATION

Dual Flopy Subsystem



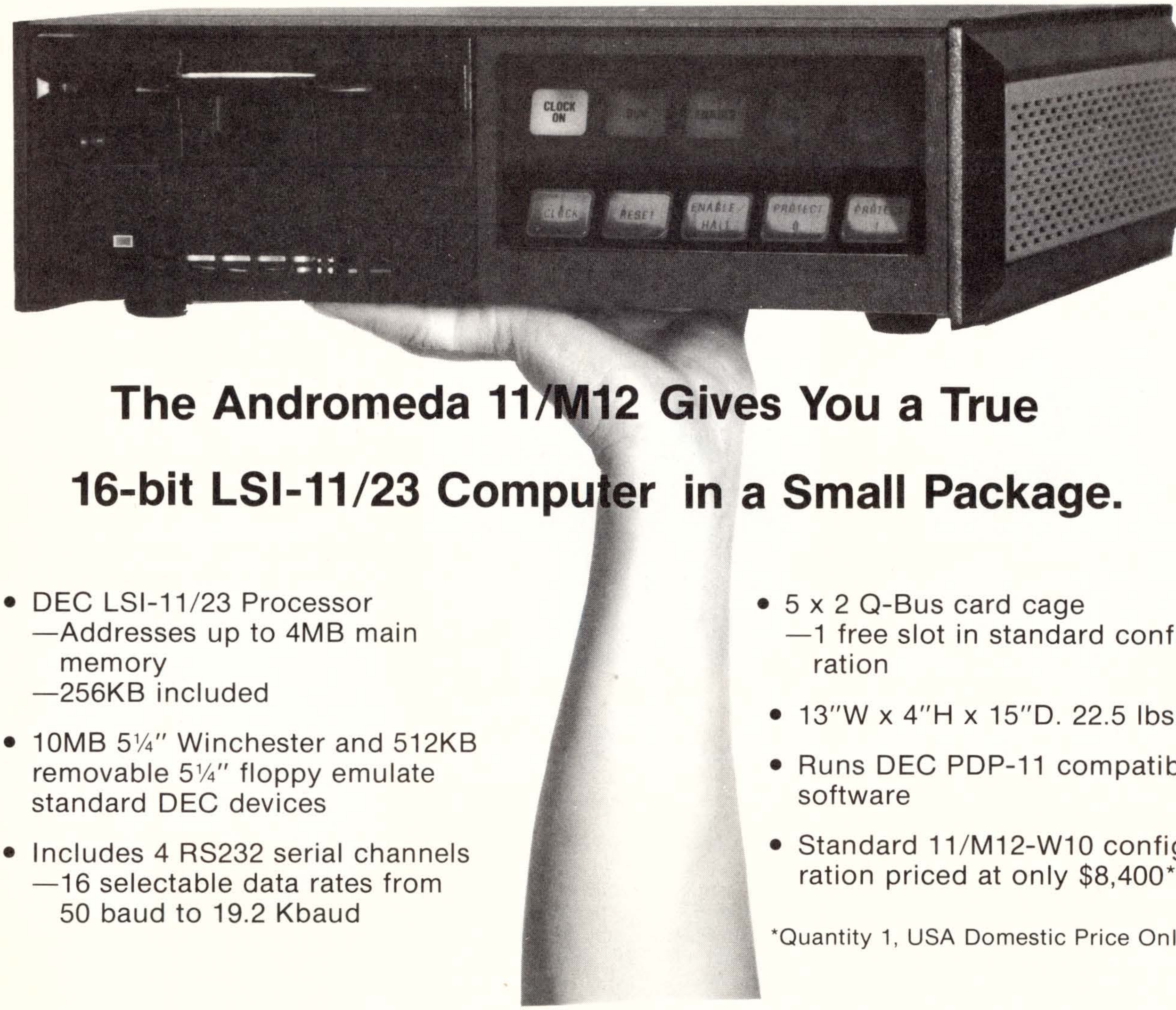
The Micro-11 Computer System, features an 11/23 Plus operating system, a 10.4 Mbyte Winchester disk drive and a dual floppy subsystem. The floppy diskette is RXV21 software and RXS02 media compatible allowing transfers to and from DEC systems. The system accommodates MDB interface modules such as multiplexors, line printer controllers, disk and tape controllers, DMA and interprocessor-link modules. The unit includes a removable front panel, a BPA84-T backplane/card guide assembly, with 22-bit addressing and revolvable bus terminator. Price is $9,200. **MDB**, Orange, CA **Write 152**

VMEBUS OPERATING SYSTEM

For 16-, 32-, And 64-bit Operations

The VMEFORTH/32 is real-time operating system which uses 68000 and 68010 proce-

A HANDFUL INSTEAD OF A ROOMFUL



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  - —256KB included
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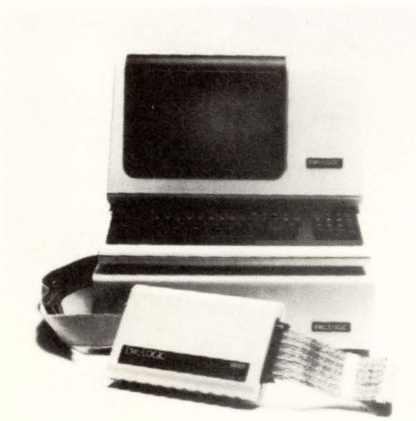
Write 59 on Reader Inquiry Card

sors in its VMEbus structure. 16-, 32- and 64-bit mathematical operations can be performed on the 32-bit language system. The VME-FORTH/32 addresses 16 Mbytes of memory, has control of the 68000 from the resident system, contains a disk storage of 2,000 Gbytes and has 230 Kbytes of user program space in 256K partition. It is compatible with 68000, 68010 and 68008 processor configurations to 4 Gbytes of memory. **Astraea Computer,** Sunnyvale, CA **Write 135**

DEVELOPMENT SYSTEM
Supports 60 Workstations

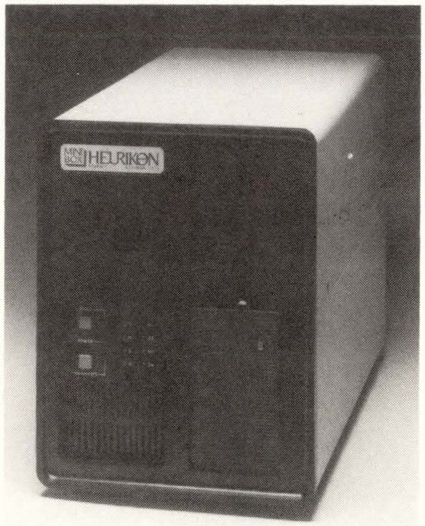


The EMUNET-2, is a microprocessor development system designed for use with DEC's VMS operating system. Emunet-2 supports 60 hardware/software workstations at distances of 5,000 ft. and has a 1 Mbaud data transfer rate. Each software-only workstation is linked to the VAX by a RS232 line. The links can accommodate 15 hardware/software workstations. A typical EMUNET-2 system consists of six satellite hardware/software workstations and six software-only stations, (not including VAX). Price is $110,000. **Emulogic,** Norwood, MA **Write 141**

GRAPHICS TERMINAL
512 × 920 Resolution

The GO-140 is an integrated alphanumeric/graphics terminal which emulates the DEC VT100 and Tektronix 4010 series of terminals. Its alphanumeric features include 24 lines of 80 or 132 characters, selectable status line, and bidirectional scrolling. The GO-140 has 512 by 390 pixel resolution and can store four alphanumeric pages. It has 31 MHz bandwidth monitor, detached keyboard communicates via an RS-232 interface. Price is $1995. **GraphOn,** Santa Clara, CA **Write 147**

WORKSTATION
Based On MC6800



The Minibox is a multiuser UNIX workstation based on the MC68000. It has a C compiler, six Multibus slots, single and dual floppy disk drives and 31.2 to 140 Mbytes of Winchester storage (expandable to 420 Mbytes). The Minibox is built around the Heruikon HK68 microcomputer and provides CPU, floppy disk drive controller, Winchester and tape interfaces, 4 to 8 serial ports and 650K bytes of RAM in two of the four or six Multibus card slots. It has two forward and rear disk drive bays which house the Winchester disk drives. **Heurikon Corp.,** Madison, WI **Write 132**

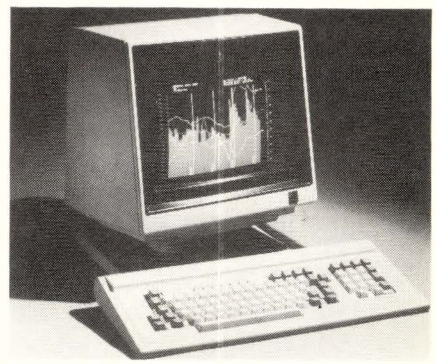
IBM-COMPATIBLE COMPUTER
With Built-In LAN

The PCterminal is an intelligent terminal which functions in an IBM network called PCnet. The terminal includes a monitor, keyboard, 8088 microprocessor, serial and parallel interfaces, four expansion slots for peripheral cards, 256K of RAM memory, built-in networking capabilities and a connection for an 5¼" floppy disk drive. It runs under IBM-DOS and SCS-DOS and has a 1Mbit/sec transmission rate. 16 PC terminals can be connected to an IBM PC or IBM XT. Price is $1,295. **Santa Clara Systems, San Jose, CA** **Write 153**

DEVELOPMENT SYSTEM
For 16-Bit System Designers

The SYS16 multi-user development system is based on the NS16032 16-bit microprocessor, allowing access to an assembler, C and PASCAL compilers, and real-time ISE tools. The SYS16 includes both processor and disk tape modules that provide hard-disk memory and streamer tape backup. One terminal is provided and an additional 8 may be added. Each user can address 16 Mbytes of memory. The CPU board contains timing, and interrupt control units as well as diagnostic firmware and a parallel printer port. **National Semiconductor,** Santa Clara, CA **Write 146**

GRAPHICS TERMINAL
With Dual Video Generator



The ID-200 series of graphics terminals have 1280 × 480 pixel resolution, and display writing rates of 1.25 million pixels/sec. The model ID200 has a dual video generator that permits images to be split and displayed on separate monitors. It features NTSC color signal output which allows graphics to be recorded on TV recorders. The ID-200 has 128 fonts, a palette of 16 colors, and independent color plane control. Support for interactive and hard copy devices is provided in the terminal. **ID Systems,** Hilliard, OH **Write 129**

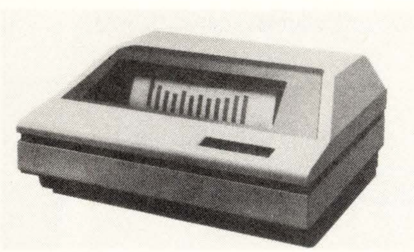
OPERATING SYSTEM
Support 256 Processors

The S1 operating system, with its modular design, can be configured as a workstation or as a multiuser/multitasking system. It can be tailored for other specific purposes, like development, as well. It is capable of networking and can support 256 processors simultaneously. The S1 can read and write files to and from CP/M, MP/M 11, MS-DOS, UNIX, XENIX and others. It also features printer, plotter, and terminal support. **Multisolutions Inc.** **Write 137**

CAE WORKSTATION
Uses HP-9000 32-Bit Processor

Avera Corp.'s EDS-2100 is the only computer-Aided Engineering Design Workstation based on the Hewlett-Packard 9000 32-bit processor. The system and its software was developed for custom, semicustom, integrated circuit, hybrid and PC board design. Avera's product is significant because as IC's become denser they will require more power. In its desktop configuration the EDS-2100 provides ¾ to 2¼ MIPS of power, which is comparable to that of the VAX II-750/780. The 19" terminal has a resolution of 1024 × 1280 pixels, autoconvergence, and a 60Hz non-interlaced refresh rate. It can be integrated with the Avera 1000 series and used as a stand-alone workstation or as a supplementary design station. Portions of larger designs can be uploaded to the EDS-2100 for analysis and assembly. Price will be around $1200,000 and deliveries start January 1. **Avera Corp.** Scotts Valley, CA **Write 150**

PRINTER/PLOTTER
6 or 8 LPI Selection



The Printronix 4260 is designed for high resolution engineering and scientific graphics as well as bar codes. It features a Centronics compatible parallel interface and software commands for forms control. It has a print speed of 130 lpm and a plot speed of 136 lpm. The 4160 has an ASCII 96 character set and built-in diagnostics. Options include a field installed PROM set and OCRA character set. **Printronix**, Irvine, CA **Write 151**

DISK SUBSYSTEM
31.2 Mbyte Storage Capacity

The Sabre is a 5¼" Winchester disk subsystem which is software transparent and operates under DEC LSI-11 systems. The disk is formatted as three RL02 units that provide 31.2 Mbytes of storage. An additional 10.4 Mbytes are in backup. The UC01/LX host adapter embeds in the QBus backplane of the LSI-11 CP,U. The UC01 is a bipolar, microprocessor-based, quad-wide circuit board that emulates two DEC RLV11/RLV12 controllers, using two register sets, allowing four drives per controller. The controller and supporting DEC software provide 22-bit addressing capacity on the LSI-11/23+ computer. Price is $9595. **Emulex,** Costa Mesa, CA **Write 167**

MICRO-FLOPPY DISK DRIVE
80 Tracks/Side

The TC 1000 Drivette has a storage capacity of one Mbyte on a 3¼" format. It is plug and data compatible with double-sided and density 96 tpi, 5¼" drive. It has a media format of 80 tracks/side and users can download 5¼" software packages to the unit's diskettes with no modification. Components of the TC 1000 Drivette include a direct drive spindle motor, a lead screw head-actuator mechanism that records at 140 tpi, and R/W and motion-control electronics boards. Price is $295. **Tabor,** Westford, MA **Write 157**

ELCTROSTATIC PLOTTER
Emulates HASP And 3780

The Versatec electrostatic remote plotting system emulates HASP and 3780 workstations, and supports binary synchronous communications protocols under DEC VAX/VMS, RSX-11M/M-Plus or RT-11 operating sytems. It includes a remote plotting controller, random element processor, and electrostatic plotting software. The random element processor handles plot data ordering and rasterization and the disk-based processors support remote color plotting. Price is $6,500. **Versatec,** Santa Clara, CA **Write 160**

STORAGE SYSTEM
With Cluster Caching

This disk controller from U.S. Design is designed for its CSS-800 line of Winchester storage systems. It contains 64 Kbytes of cache memory and includes features such as look-ahead buffering, cluster caching and adaptive control. The system is configured with 60 Mbytes of disk, ¼" cartridge backup, Q-bus interface 32 Kbyte caching controller. Price is $9,995. **U.S. Design,** Lanham, MD **Write 165**

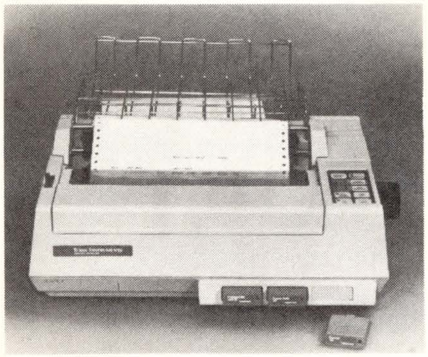
JOURNAL PRINTER
For Electronic Measurement Systems

The President Printer is a 40 column dot matrix impact journal printer. It is packaged for an industrial environment and for use with Durant's electronic count and measurement systems. The printer is interfaced to the count control or toalizer by a connecting cable. The printer provides a record of production totals, test results, and manufacturing data. **Eaton Corp.**, Watertown, WI **Write 159**

NETWORK SERVER
Connects Instruments And Peripherals

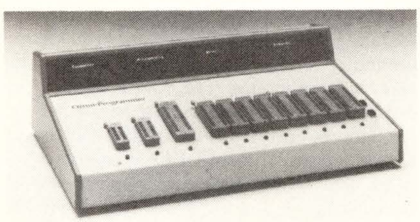
The network interface server connects microcomputers, peripherals, controllers and instruments through an RS 232, RS 422, parallel or IEEE 488 port. It contains the network interface, host I/O interface and timing and control logic based on an internal CPU. The unit contains its own enclosure, power supply and control firmware in ROM. Connection to the network is made via a transceiver active tap or a daisy chain configuration through Type F connectors. **Destek,** Sunnyvale, CA **Write 172**

DUAL MODE PRINTER
150 CPS Draft Mode



The OMNI 800 Model 8545, is a dual mode dot matrix printer for word and data processing applications. It has a 150 cps draft mode and is compatible with industry-standard escape codes, featuring Epson, Qume and Diablo data streams. Three fonts can be plugged in simultaneously, permitting the user to switch print styles without stopping. Each font module provides draft and letter-quality character sets. It has two matrix formats, 9×9 and 32×18. Price $935.–$995. **Texas Instruments**, Dallas, TX **Write 176**

PROM PROGRAMMER
With Self-Test Diagnostics

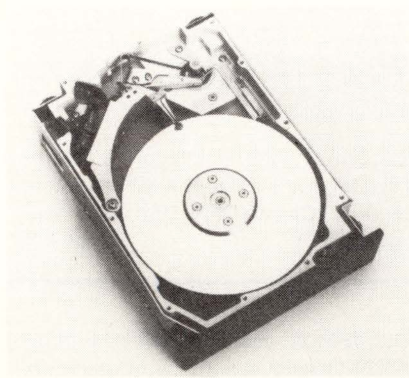


The Model GP-1140 provides gang programming capabilities for NMOS devices including EPROMs, EEPROMs, and MPUs. Nine devices may be programmed. Features include diskette storage of chip masters and command files, self-test diagnostics, and chip error detection. The GP-1140 has a clamp lever for group insertion and removal and adaptors for auxilliary devices. Price is $6995. **Varix**, Dallas, TX **Write 175**

BACK-UP SYSTEM
With Interface Adaptors

The disk back-up system from ADIC has interface adapters for most systems and buses including SASI, QIC-02, S-100, Multibus and GPIB. The system utilizes a 16 track ¼″ data cartridge. Each track has 4096 addressagble blocks with 1024 bytes of data. The sytem features a 600 ft cartridge, error correction routine, and on board microprocessor control. **Adic**, Kirland, WA **Write 163**

WINCHESTER DISK DRIVES
10.48 to 31.46 Storage Capacity

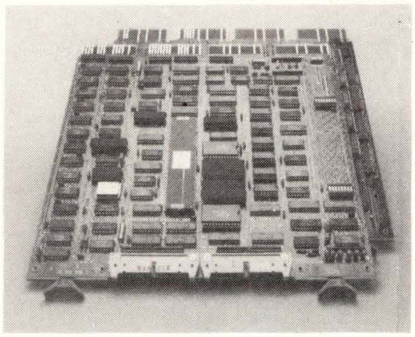


Models TL213, TL226, and TL240 are half-height Winchester disk drives which offer 10.48 to 31.46 Mbytes of formatted storage. Features include plated media, automatic spindle brake and actuator lock, dedicated head landing/shipping zone, four-point shock mounting, single PCB, and internal diagnostics. The three drives use standard ST506/412 interfaces. Access times are 95ms-average, 20ms-track to track, and 230ms max. Standard transfer rate is 5.0 Mbits/sec. Prices are: Model TL213—$650, Model TL226—$850 and Model TL240—$1055. **Tulin**, San Jose, CA **Write 171**

MULTIPLEXER
5 Mbit/sec Transfer Rate

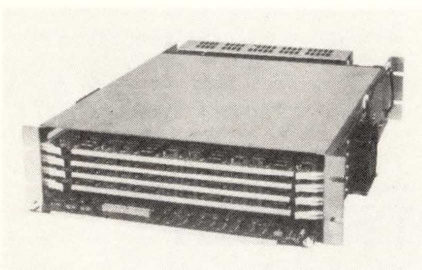
When combined with a hard disk subsystem, this multiplexer enables users to share a hard disk with four computers without the need for additional hard disk drives. The Multiplexer is a parallel transfer device with transfer speeds of 5 Mbit/sec and is compatible with most 5½″ fixed and removable hard drives. **B.T. Enterprises**, Bohemia, NY **Write 173**

PROCESSOR BOARD
32-Bit



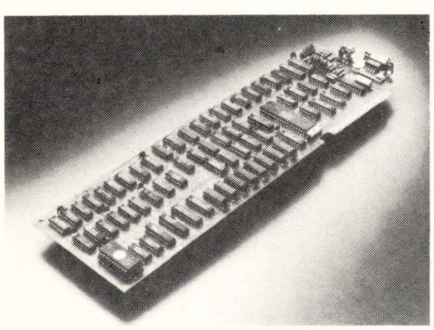
The 32-bit UniVax processor from Cambridge Digital is a 68000-based board for the DEC PDP-11 product line. The UniVax replaces the PDP-11 both in terms of power and speed because of its 32-bit processor. The operating system, 68000 processor and memory is available at board level or as part of an integrated system. Cambridge Digital will offer their Multi-User Systems 58 and 94 with the Univax processor. The UniVax provides 16 Mbytes of logical address within the Q-bus' 4 Mbyte address pace and dual bus architecture with dual port memory. Throughput is around 1 MPS. Price is $8,000. **Cambridge Digital**, Cambridge, MA **Write 208**

VOICE PROCESSING SUBSYSTEM
For Remote Data Entry Systems



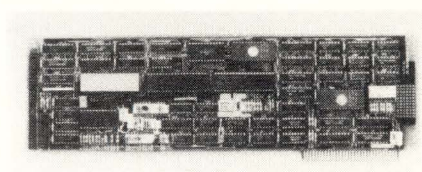
The VoiceStör Model 30 voice storage subsystem is designed for integration with systems to provide voice response and voice storage retrieval. Applications include remote data entry teleprocessing, and message broadcast systems. Model 30 supports thirty-two simultaneous voice channels allowing access on an asynchronous basis. The system interface is a RS-232C control channel, and system commands include record and playback on the specified channel along with supervisory and maintenance functions. **VoiceTek**, Newton, MA **Write 187**

COLOR GRAPHICS BOARD
320 × 200 Resolution



The Color/Graphics Monitor Adapter Board provides color display and graphics capabilities output for the Eagle PC, Eagle 1600 Series, IBM PC and most IBM PC compatible microcomputer systems. It has a resolution of 320 × 200 pixels and 16 foreground and eight background colors in the color mode. 640 × 200 pixels may be displayed in the monochrome mode. The adapter has two operational modes, A/N and APA. **Eagle Computer**, Los Gatos, CA **Write 188**

DISK CONTROLLER
Supports St 506 Drives

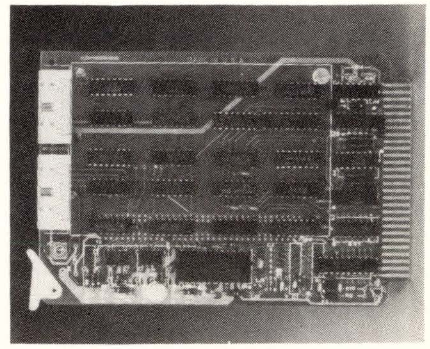


The P Series is an IBM PC I/O bus compatible ST506 Winchester disk controller. It has an on board microprocessor and is compatible with PC-DOS 2.0. Other features include, a single card interface, multiple sector R/W operations, 8 bit error correction, and an on board socket for 8 Kbyte boot EPROM. The P Series supports drives with 16 heads. **Adaptive Data,** Pomona, CA **Write 205**

MICROCOMPUTER SYSTEM
Contain 64K RAM

The MCPU-900 is a microcomputer system located on a STD bus card. It features a 4MHz Z-80A processor, 64K RAM, a 28 pin ROM/EPROM socket for accepting a 2K, 4K, 8K, or 16K device, and I/O and peripheral control devices. The controller handles four 5" or 8" disk drives in either single or double density. Its parallel printer interface functions as either the hard copy output or as a strobed 8-bit output. Price is $795. **Miller Technology,** Los Gatos, CA **Write 193**

STD BUS A/D BOARD
32-Channel

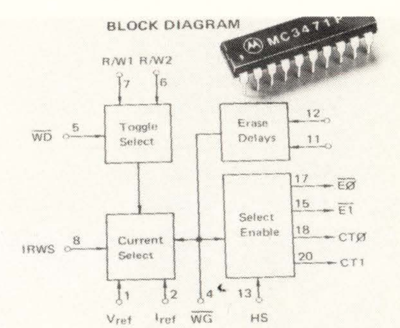


The DT2712 is a STD Bus compatible A/D system that operates with any STD Bus 8 or 16-bit microcomputer. The DT2712 provides 10-bits of resolution on 32 single-ended analog input channels. Input signals are scanned at a throughput rate of 3300 samples/sec. and the board is jumper selectable for I/O mapped or memory-mapped addressing, and supports software polled or vectored interrupt schemes. Price in quantities of 100 is $195. **Data Translation**, Marlboro, MA **Write 202**

CONTROLLER BOARD
10 Mbyte Transfer Rate

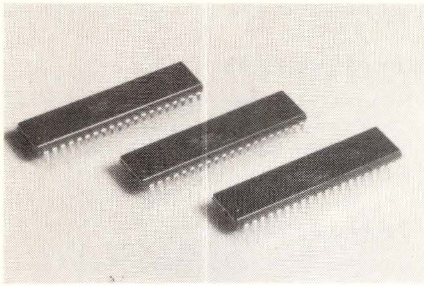
The WD2000 boards, a VLSI and controller, feature 10 Mbyte/sec transfer rates, run limited codes (2, 7 type), buffered step rates and recovery modes. The boards include on-board diagnostics and on-board 10 Mbyte/sec data separators. The WD2011 VLSI controller features on-chip ECC re-entry algorithm and DMA interface. **Western Digital**, Irvine, CA **Write 186**

FLOPPY DISK CONTROLLER
RC Or Logic Compatible



The MC3471P is a monolithic integrated Write Controller/Head Driver designed to interface the data and control signals and the heads for Tunnel or Straddle-erase floppy disk systems. Features include write current switching, track compensation, and on-chip erase delays. Price in quantities of 100-999 is $4.25. **Motorola**, Phoenix, AZ **Write 194**

INTERFACE ADAPTER
With 8-Bit Data Ports

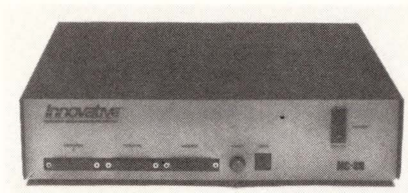


The HD6321 is a CMOS version of the NMOS parallel I/O peripheral interface adapter. Characteristics include two sets of 8-bit parallel data ports, four interrupt inputs, and handshake control. It is packaged in a 40-pin DIP and has a 10 mA current consumption during operation, and 500 A during standby. **Hitachi,** San Jose, CA **Write 198**

DISPLAY CONTROLLER
Graphics Applications

VG150 is a display controller for graphics composition applications. The unit is a single board with IEEE 796 compatibility. The VG-150 displays 1400H x 1100V pixels non-interlaced (60 Hz field rate) and is software programmable. Features include a bipolar 16 bit controller, transparent memory, graphics primitives and proprietary microcode. **Datacube,** Peabody, MA **Write 201**

COMMUNICATIONS PROCESSOR
Emulates IBM 3274-51C Controller



The MC-80/600-1 communications processor emulates the IBM 3274-51C communications controller which runs configurations support level A. The device converts a DEC VT-100 compatible terminal into either a IBM 3277-1, 3278-1 and 3278-2 terminal using a BSC protocol. The MC-80/600-1 performs mapping and any data displayed on the terminal will be the same as an IBM 3277/3278 display station, with virtual screen sizes of 480, 960, and 1920 characters. All screen formatting capabilities are supported. Price is $1,495. **Innovative Electronics,** Miami, FL **Write 207**

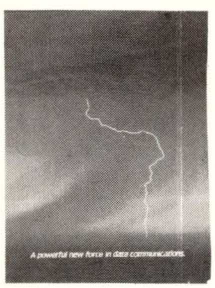
16-BIT MICROPROCESSOR
MC8000L12-Compatible

The HD68000-12 is a 12.5 MHz 16-bit microprocessor which is pin- and software-compatible with Motorola's MC68000L12. It has a minimum instruction execution cycle time of .32 μsecs and operates from a supply of 5V consuming 1.75W at maximum. Operation temperature ranges from 0.C–70°C. Prices in lots of 1,000 are HD68000-12 (dual in-line package) $18,000., HD68000Y12 (pin-grid array package) $20,000., HD68000Z12 (leadless chip-carrier package) $21,000. **Hitachi,** Tokyo, Japan **Write 203**

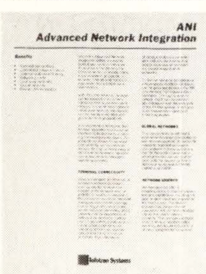
DATA CABLES
With 25 Connected Conductors

The 232/25 and 232/RIB series of cable connectors are available in standard and flat ribbon configurations. Both contain 25 connected conductors and come in polarity configurations: male-to-male, male-to-female, and female-to-female. Standard and custom lengths are available. **Electro Standards,** Providence, RI **Write 190**

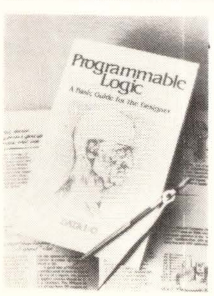
New Literature



Local Data Switches Brochure. Develcon Electronics' full-color brochure describes the Develnet modular, intelligent local data switches, or nodes, which can be expanded to a user's networking needs. Each node supports 248 data lines with a throughput of 3 million characters/sec. Many standard features such as password-protected access, prioritized queuing, universal line access and operator defined configurations are detailed.
Develnet **Write 261**

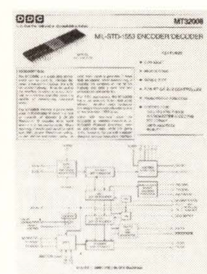


Networking Brochure. The four-page illustrated bulletin from Infotron Systems describes Advanced Network Integration (ANI), an approach to data communications that permits interconnection of nodes, transmission speeds, protocols, interfaces, and formats. The bulletin covers connectivity, global and local area networks, and network growth.
Infotron **Write 263**

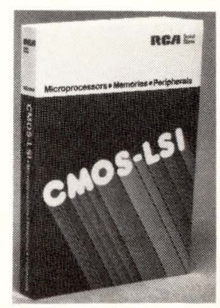


Programmable Logic Guide. Data I/O's 32-page guidebook explains programmable logic and its advantages over fixed-function LSI/MSI logic and custom logic. The book details a design problem, showing how design equations are generated and translated into fuse tables and how a PAL or IFL device is programmed and functionally tested.
Data I/O **Write 264**

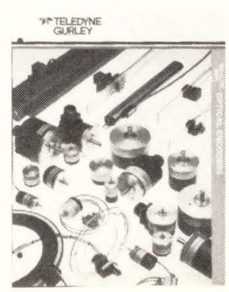
Encoder/Decoder Bulletin. This eight page product data bulletin from ILC Data Device Corp. describes their MT32008 MIL-STD-1553 Encoder/Decoder. The MT32008 is a single chip device which acts as an interface between a serial data bus transceiver and a subsystem 16 bit parallel data highway. It is designed for operation as either a remote terminal or bus controller. The product bulletin contains a general description.
DDC **Write 265**



CMOS-LSI Databook. The 588-page Databook, SSD-260A, provides technical information on RCA's line of CMOS-LSI products. Included are the 1800-series CMOS microprocessors, CMOS memories, CMOS peripherals, and RCA alternate-source types to the 6805 CMOS series of microprocessor products.
RCA **Write 267**



Optical Encoder Brochure. This six-page color brochure describes Teledyne Gurley's modular and linear encoders, highlighting the red, white and blue lines of rotary encoders. Photographs and charts detail size, tolerances, and accuracy. Also discussed are the electronics of the encoders and the availability of disks.
TRL **Write 268**



Calendar

November 28–December 1

NATA 14th Annual Convention and Exhibition Showcase. Sheraton Washington, Washington, D.C. Contact: North American Telecommunications Assoc., Box 75196, Washington, D.C. 20013. (202) 547-4450.

November 28–December 2

COMDEX Fall '82. Las Vegas, NV. Contact: The Interface Group, 300 First Ave., Needham, MA 02194. (617) 449-6600.

December 1–3

SEMICON/Japan '83. Mountain View, CA. Contact: SEMI, 625 Ellis St., Mountain View, CA 94043. (415) 964-5111.

December 5–6

Computer Conference. San Diego State University, San Diego, CA. Contact: Professor Nenad Marovac, Dept. of Mathematical Sciences, San Diego State University, San Diego, CA 92182. (619) 265-4345.

December 5–6

The Southwestern Conference on CAD/CAM. San Diego, CA. Contact: Nenad Marovac, Dept. of Mathematical Sciences, San Diego State University, San Diego, CA 92182. (619) 265-4345.

December 5–7

International Workshop on Data Management in Distributed Real Time Telecommunication Systems. West Palm Beach, FL. Contact: Subir Purkayastha, American Bell Inc., Crawfords Corner Rd., Holmdel, NJ 07733. (201) 834-4774.

December 5–8

National Database & 4th Generation Language Symposium. Boston, MA. Contact: Radisson-Ferncroft, 50 Ferncroft Rd., Danvers, MA 01923. (617) 777-2500.

December 7–9

Workshop For EDP Professionals. Ritz-Carlton, Boston, MA. Contact: The American Institute for Professional Education, 100 Kings Rd., Madison, NJ 07940. (201) 377-7400.

December 7–9

SNA Seminar. Washington Hilton, Washington, D.C. Contact: The American Institute for Professional Education, 100 Kings Rd., Madison, NJ 07940. (201) 377-7400.

December 7–9

Software Maintainance Workshop. Monterey, CA. Contact: H. Schneidwind, Computer Science Dept., Naval Postgraduate School, Monterey, CA 93940. (408) 646-2719.

December 13

Computer Networking Symposium. Silver Spring, MD. Contact: Computer Networking, Box 639, Silver Spring, MD 20901. (301) 589-8142.

December 13–15

Fifth Israel Conference And Exhibition on CAD/CAM. Tel Aviv, Israel. Contact: The Israel Society for CAD/CAM, Box 3473, Tel Aviv 61033.

December 13–16

Designing With 16-Bit Micros. Los Angeles, CA. Contact: Ruth Dordick, Integrated Computer Systems, 6395 Arizona Pl., Los Angeles, CA 90045. (213) 450-2060.

December 19–21

22nd IEEE Conference On Advanced Automation. Taipei, Taiwan. Contact: J. T. Tou, Center For Information Research, University of Florida, Gainesville, FL 32611. (904) 392-0920.

January 9–12

ATE West Conference. Anaheim, CA. Contact: Morgan-Grampian Expositions Group, 2 Park Ave., New York, NY 10016. (212) 340-9780.

Advertiser Index

Introducing the Whizzard® 3355. Now you can break the speed limit without paying the price.

Whizzard 3355. Meet the Whizzard 3355, the newest computer graphics system from Megatek. Up to 400 thousand vectors per second. The fastest high speed performance of any system in its price range, thanks to our Graphics Engine.™ Upward compatibility with every Whizzard. And a high resolution color raster display with 2D real-time dynamic transformations.

Now you can have the speed you want, and pay a lot less for it in the bargain.

The Whizzard 3355 is a full-function computer graphics system that cost-effectively supports your graphics applications. Especially in the areas of mechanical or electronic CAD, simulation, or command and control. And its RS232C interface, with its own 16-bit processor and up to 500 Kbyte dedicated local RAM, offloads the host computer and allows serial communications.

The Whizzard 3355's standard features include a 19″ 1024^2 60 Hz non-interlaced monitor, 16 simultaneously displayable colors out of a possible 4096, complex 2D graphics transformations (rotate, translate, continuous scale, and clip), and proprietary local processor with serial interface. You also get VT-100™ emulation, an ergonomic keyboard, and a host of available options. Then there's graphics software. Megatek's WAND,™ TEMPLATE® and a wide variety of third party application packages, too.

The Whizzard 3355. High speed performance, and true cost-effectiveness.

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Write 2 on Reader Inquiry Card