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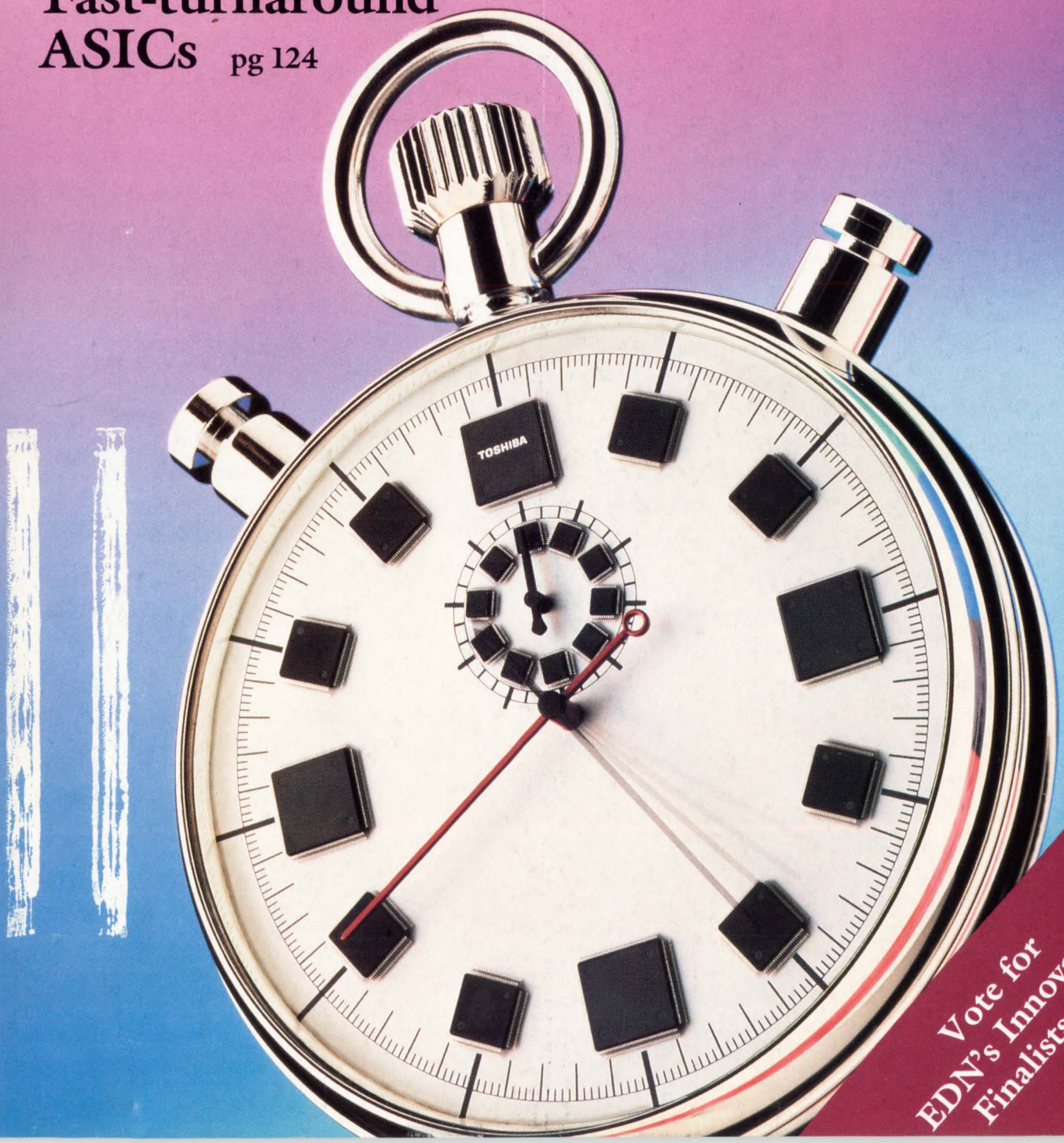
SEPTEMBER 3, 1990

EDN®

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

ASIC SPECIAL ISSUE

Special Report: Fast-turnaround ASICs pg 124



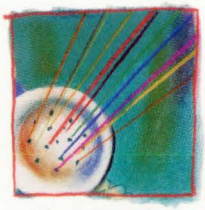
Vote for EDN's Innovation Finalists pg 49

PC Collection

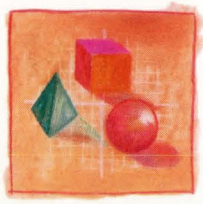
Peripheral Collection

Data Communications Collection

Industrial Collection



Telecommunications Collection



Graphics Collection

high-density versions.

Some of the most contemporary ASIC art is in data communications design. Where increasingly complex network requirements are creating new challenges for designers.

Which is precisely why we created the *Data Communications Collection*.™ All you need to improve the art of network reliability and performance. Now and in the future.

The collection integrates SuperMacros, supporting industry-standards such as Ethernet,™ with compiled cells to let you reduce components and board size.

For ASIC art with industrial strength, take the *Industrial Collection*™ to work with you. It offers everything you need to make your industrial application a memorable one. Whether you're designing controllers, instrumentation, process control or robotic systems.

At the heart of the collection is Fujitsu's family of DSP core controllers, which support fixed and floating-point operations and a variety of finite word lengths.

So you get controllers and vision systems that are inexpensive, fast and easily programmable.

Now that the industry is implementing the ISDN standard, what you need most is an ASIC that supports it. Which brings us to the *Telecommunications Collection*.™

The collection meets telecom design needs. Offering standardized building blocks such as DSP cores and other functions to implement standard protocols and enhanced features.

If you're a graphics designer, you know that 3-D graphics have turned into 3-D art. And the best way to create it is with the *Graphics Collection*.™

The Graphics Collection integrates functions onto a single device which are unavailable as standard products. Cutting your design time and honing your competitive edge.

In addition to getting SuperMacros for most of the 2900 family, the collection also provides you with RAM and ROM compilers and specialized graphics algorithms.

All in all, there's no better way to begin your next ASIC design than with a visit to the ASIC Gallery.

Stop by and tour the collections. Call 1-800-642-7616. We'll be happy to show you around.

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CIRCLE NO. 128

Welcome to the ASIC Gallery.™

Six priceless collections let you create your own design masterpiece.

A is for art. And also for ASIC. We put them together to bring you the ASIC Gallery. Six masterful collections of applications-oriented products and services let you create your own design masterpiece.

Works of art, like applications, are unique. So is the ASIC Gallery. We've made silicon itself application-specific. So that instead of a blank canvas, you get specific collections of priceless "objets d' art" that make it easier to compose your own design masterpiece.

Each collection contains building blocks that let you design more compact, higher performance systems in far less time.

All in a CMOS environment using Fujitsu's high-speed .8μ channeled and channelless gate-array technologies as your foundation. Just choose the collection that's right for you.

The *PC Collection*™ lets you paint a PC portrait you'll be proud of. Using SuperMacros™ and compiled cells for 8086/8088/80186 and 80286-based PCs and laptops.

The PC Collection's SuperMacros cover the entire 8200 macro family. And integrate greater functionality onto a single device. So you can increase speed and reliability while you lower board space, power consumption and cost.

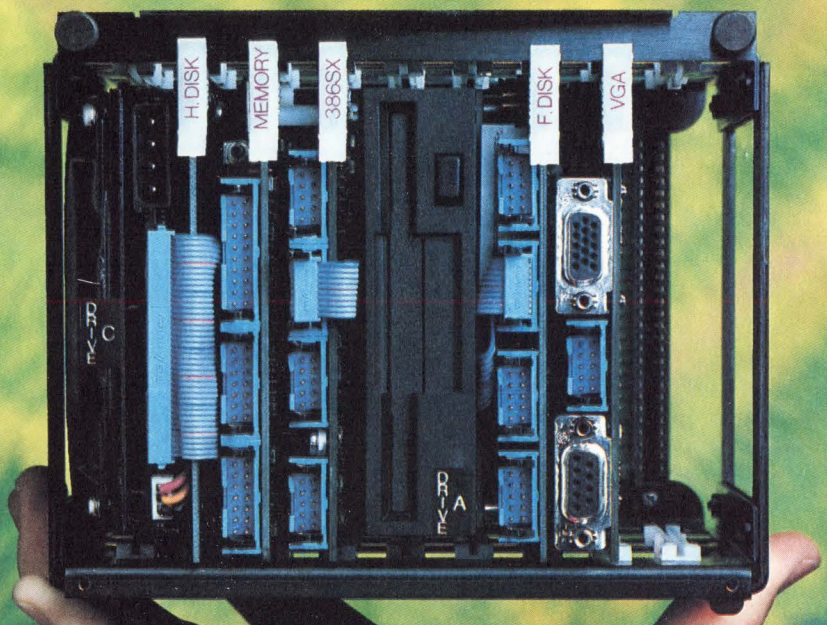
If your taste in ASIC art runs to peripherals, check out the *Peripheral Collection*.™ Its high level of integration incorporates greater functionality in a smaller footprint.

Plus you get support of industry standards like SCSI. As well as 8200 SuperMacros and RAM compilers in both high-speed and

You're invited to an exhibit of modern ASIC masterpieces.

THE CAT

A NEW CompactAT 386SX INDUSTRIAL COMPUTER



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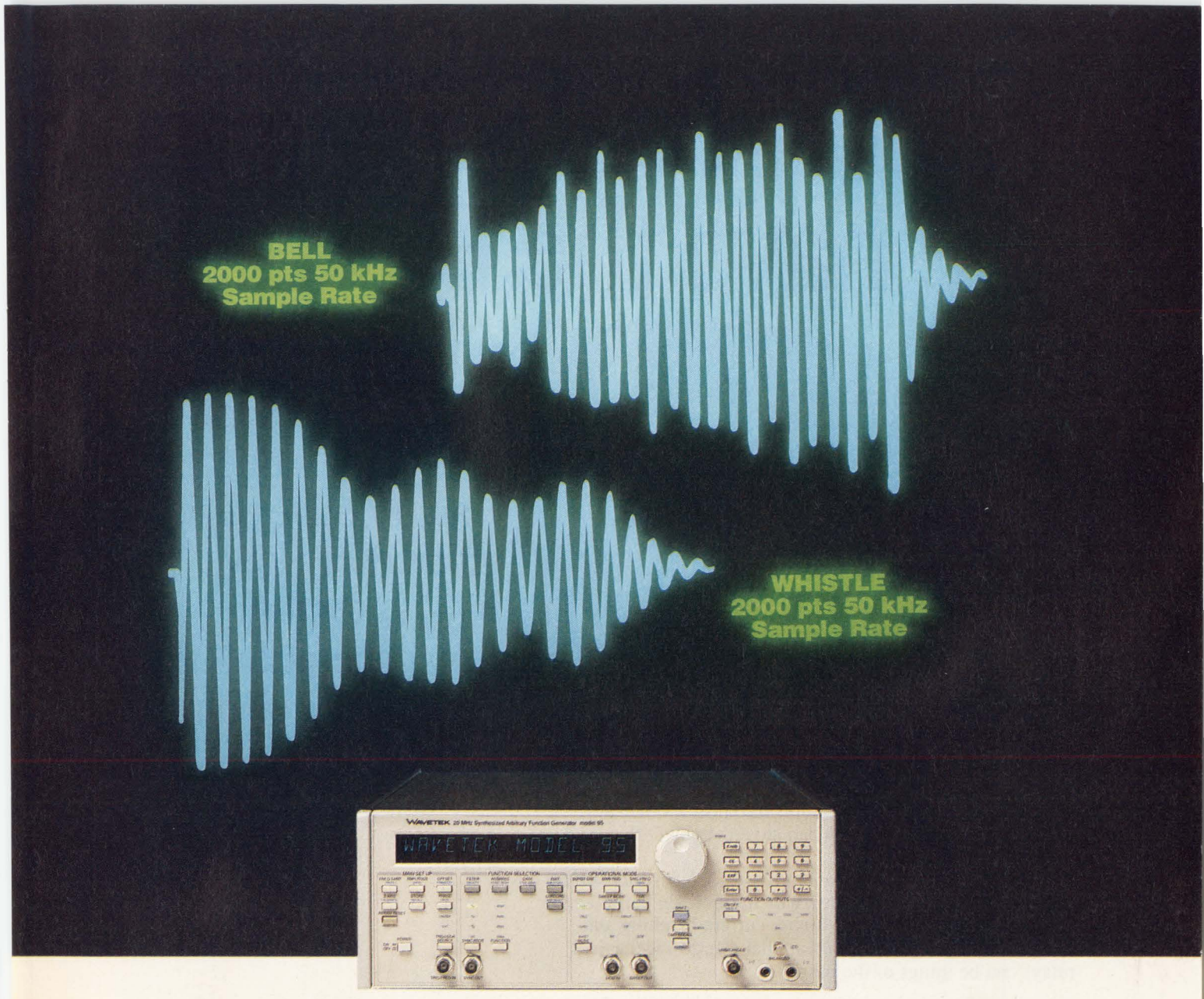

Our new function generator has all the bells and whistles.

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For information about all the other bells and whistles you'll find on the Model 95, call Wavetek San Diego, Toll Free at **1-800-874-4835** today.

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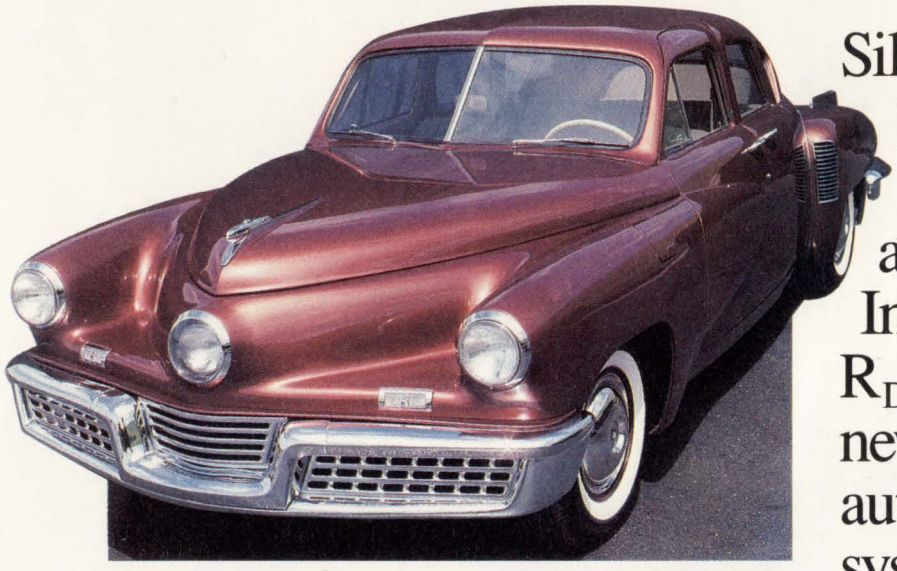


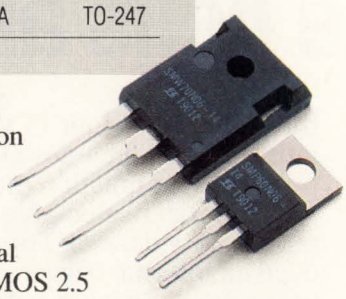
Photo courtesy Behring Auto Museum

Siliconix' power MOSFETs for leading-edge automotive designs. Incredibly low $R_{DS(ON)}$ for the new generation of automotive electrical systems.

Preston Tucker built features into his cars that were far ahead of his time. Now you can have the power that Tucker missed.

Siliconix' new 14-milliohm $R_{DS(ON)}$ power MOSFETs dramatically reduce system size by minimizing part count or shrinking heat sinks. Their higher current handling and cooler running capabilities mean that electro-mechanical relays can be things of the past.

Device	On-Resistance	Voltage	Current	Package
SMP60N06-14	14 mΩ	60 V	60 A	TO-220
SMW70N06-14	14 mΩ	60 V	70 A	TO-247



These MOSFETs are more than tough enough to handle the voltage spikes common in cars. And they have lower gate charge so you can design with smaller drive circuits and fewer components.

Design cooler cars and shrink electrical system size! Ask for a free gift and the SiMOS 2.5 Design Kit. Call our toll-free hotline now! **1-800-554-5565, ext. 953.**

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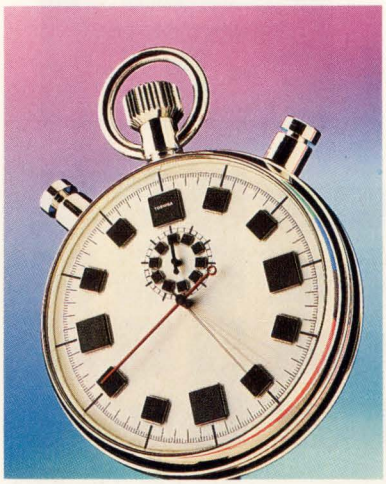
EDN Magazine Edition

Volume 35, Number 18 September 3, 1990

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *In the special report in this ASIC Special Issue, learn how vendors' shrinking fabrication cycles can affect your ASIC design. Turn to pg 124. (Photo courtesy Toshiba America Electronic Components Inc; photography by Paul Kleiter Graphic Design)*

ASIC SPECIAL ISSUE

SPECIAL REPORT

INNOVATION™ Driving Electronic Technology Into The Next Century

DESIGN FEATURES

Continued on page 7

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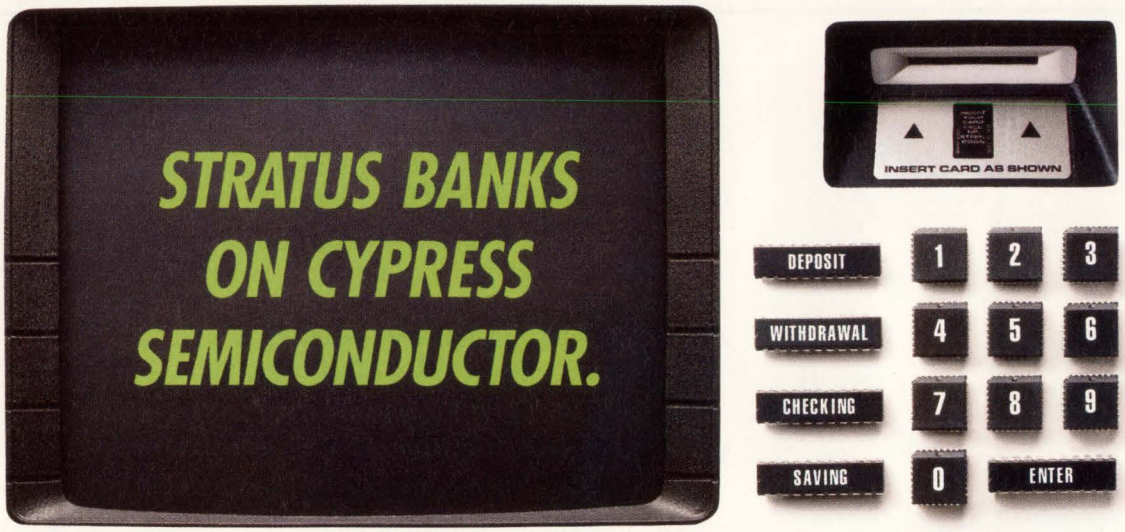

Customers don't tolerate ATMs that are down, which is why many ATM networks rely on fault-tolerant computers. Stratus Computer's systems deliver the utmost reliability in a wide range of critical, on line applications. Since their success is based on quality, Stratus demands the highest quality from its vendors. In their words, they look for the "best in the business." Their vendor relationships are so strong that often Stratus can eliminate incoming component inspection. We are proud to have earned a Vendor Excellence Award from this excellent manufacturer.

Thanks, Stratus.

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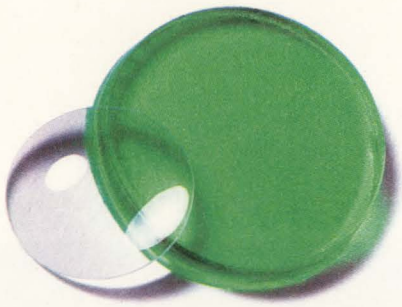

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Mike Evans, National Semiconductor's Director of Strategic Applications, Integrated Systems Group, talks about applying high-performance VLSI solutions to communications problems.

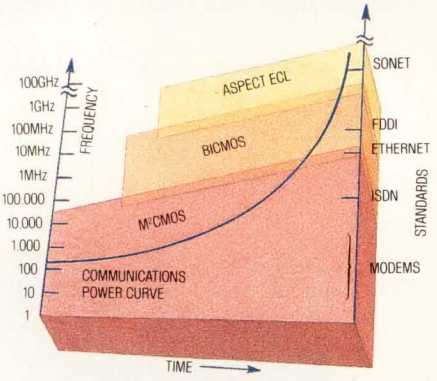
Achieving single-chip integration for IEEE 802.3 local area networks.

"We're already a generation ahead in Ethernet chip design. We're the LAN market leader and the de facto standard in the industry. And now we've set a new standard in analog and digital integration with SONIC, for 'Systems-Oriented Network Interface Controller.' It combines a controller, an encoder/decoder, and a phase-locked loop onto a single chip that delivers a data rate of 10Mbits per second.

"It's the first device that implements all 802.3 network management functions. And the first capable of embedding the Ethernet control functions in 32-bit computer systems. High performance, low power, small footprint."

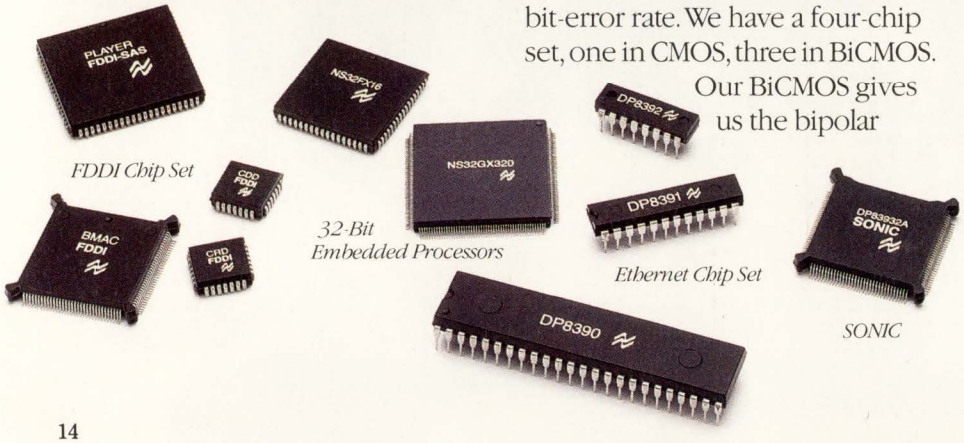
Setting the pace for tomorrow's fiber-optic solutions with FDDI.

"This is a quantum leap from Ethernet. Fiber Distributed Data Interface. It's the backbone of next-generation LANs. And it delivers at an incredible 100Mbits per second, and with an incredibly low bit-error rate. We have a four-chip set, one in CMOS, three in BiCMOS. Our BiCMOS gives us the bipolar speed necessary for these data rates, with the CMOS density for high-speed logic functions. And we're already adding a fifth chip — a high-performance system interface. This is the frontier — and we're right on the edge of it."



Creating the world's first analog programmable CODEC/filter.

"Here's another example of how we're building on our leadership position. Our COMBO I, combined coder/decoder and filter, is already on nearly half of the non-captive analog linecards in the world. But the telecom market needs higher performance and more flexibility, so we've given



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Putting the pride of National to work for you.

"You know, communications affects the whole world. But the first step in communicating is overcoming our natural reluctance to do it. If I wanted to talk to communications experts, I'd call National. That's where it starts."

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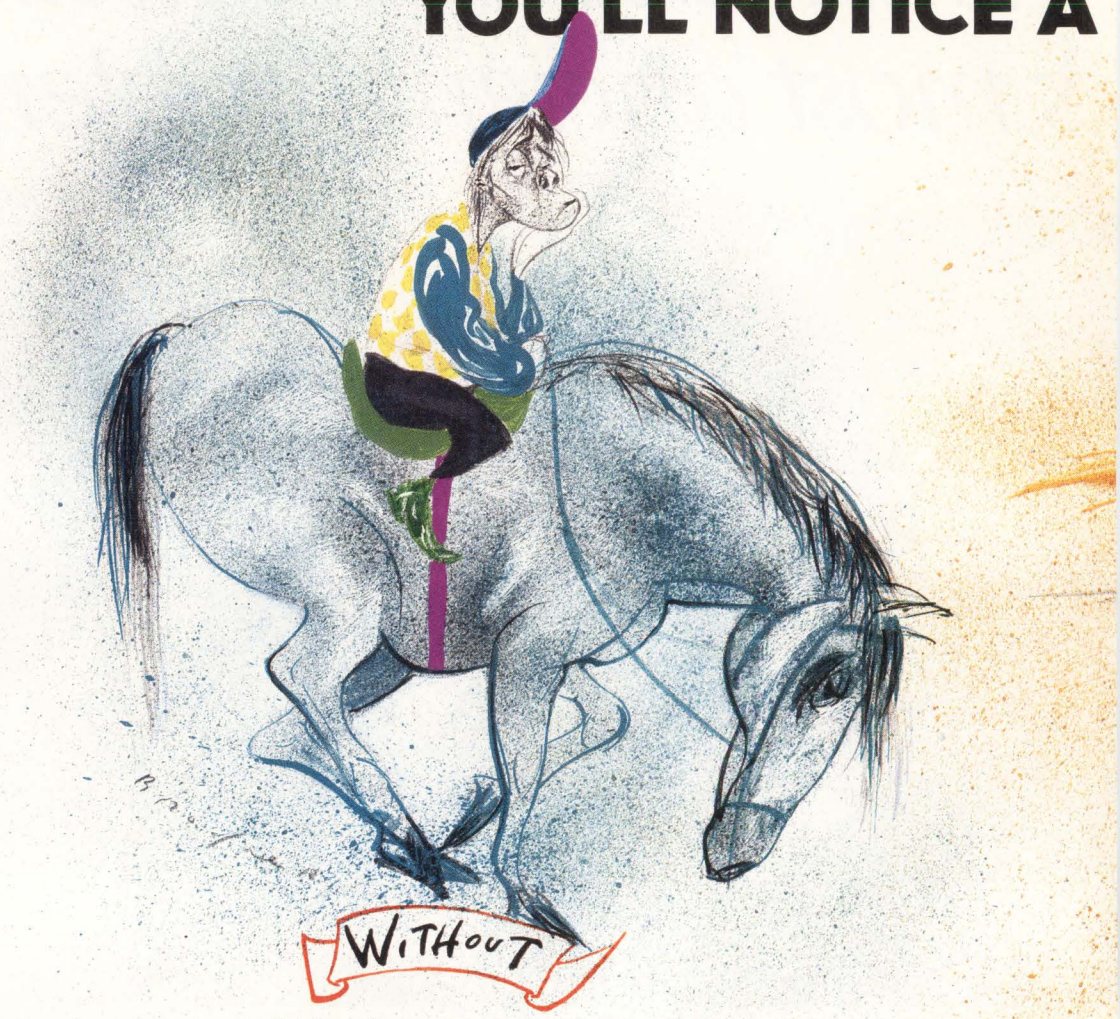
SAMSUNG NOW

68040 SYSTEMS EQUIPPED WITHOUT YOU'LL NOTICE A



Systems utilizing the new Samsung 84C31 take off. They run like Triple Crown-winning thoroughbreds. They blaze, scorch, and leave others in their dust.

In a word, they are fast.

And they make even speedy 68040 systems that *don't* use the 84C31, look like they're not in motion.

The 84C31 was designed with the close cooperation of Motorola. It is the *only* DRAM controller designed specifically for Motorola's powerful 68040 and 68030 microprocessors.

SAMSUNG'S DRAM CONTROLLER FOR THE 68040 AND 68030

Part Number	*RAMs Supported*	*Package*
KS84C31-33CL	256K, 1Mb	68-pin PLCC
KS84C32-33CL	256K, 1Mb, 4Mb	84-pin PLCC

Samples and production available now.

Like the extremely successful earlier-generation Samsung System Accelerators™, the part is highly integrated and inherently fast. And as the cutting edge in memory control, it can help you simply and economically enhance even 68040 performance.

The 84C31 supports both the burst and non-burst modes of the 68040. It also provides a direct interface

WITH OUR DRAM CONTROLLER: CERTAIN IMPROVEMENT.

to the microprocessor. Which saves you dollars, board real estate, and design time, since it means you don't need additional glue logic.

68030 PERFORMANCE SUMMARY

Access Clocks	*DRAM Speed*	*Frequency (Mhz)*
4-2-2-2	70 ns	20
5-2-2-2	120 ns	20
5-2-2-2	80 ns	25
6-2-2-2	120 ns	25
6-2-2-2	80 ns	33
7-2-2-2	100 ns	33

68040 PERFORMANCE SUMMARY

Access Clocks	*DRAM Speed*	*Frequency (Mhz)*
3-2-2-2	80 ns	25
5-2-2-2	100 ns	25
6-2-2-2	120 ns	25
5-2-2-2	80 ns	33
6-2-2-2	100 ns	33

Ease of design is another advantage. As a glance at our System Design Guides will show, it's an unusually simple chip to design in.

All in all, we believe the 84C31 is the best memory controller solution available today.

For details on using it to make *your* designs take off, contact DRAM Controller Marketing, Samsung Semiconductor, 3725 No. First St., San Jose, CA 95134. Or call 1-800-669-5400, or 408-954-7229.

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CIRCLE NO. 82

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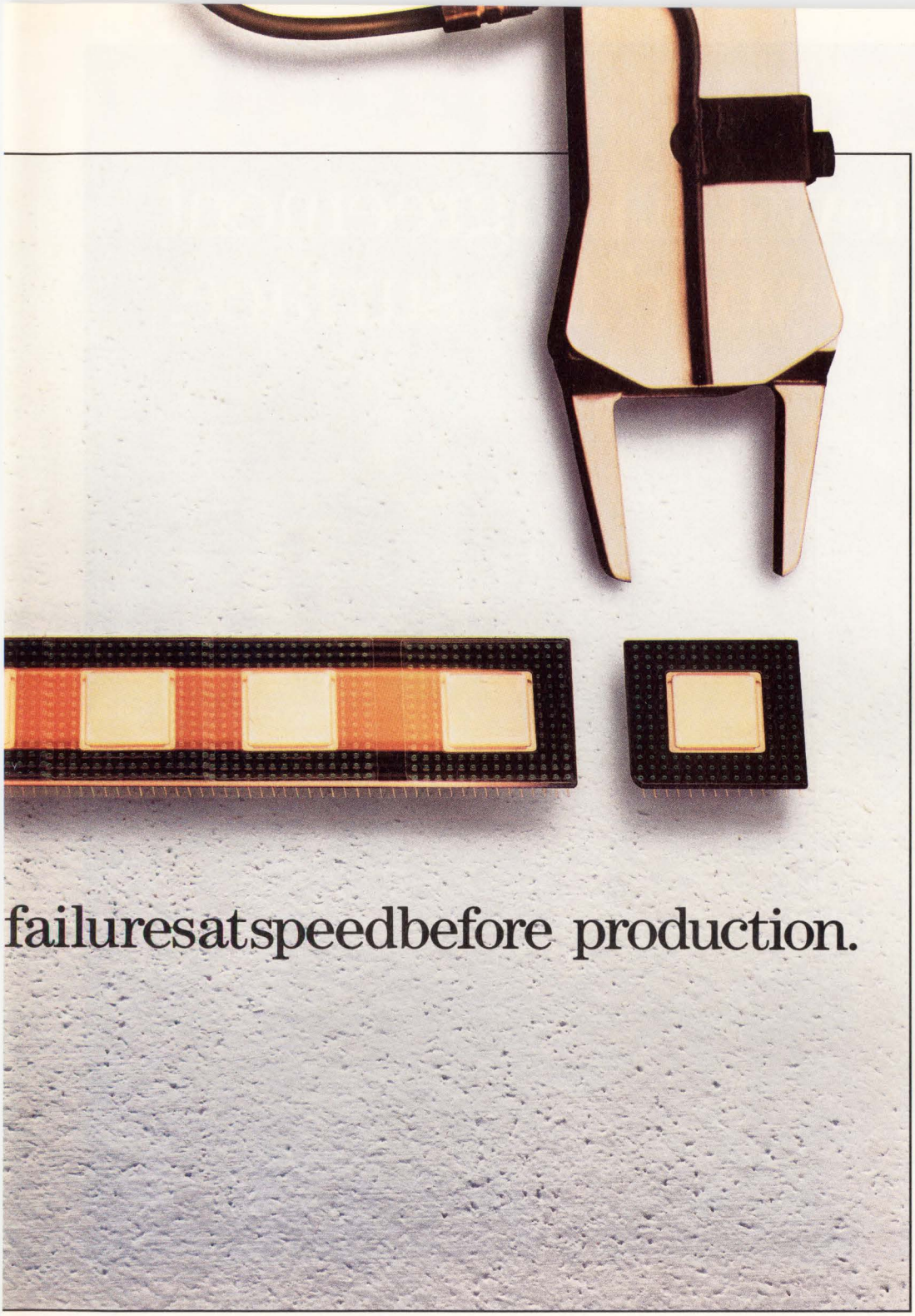
a 400 MHz vector rate on all channels and up to 512 pin capacity. Finally, you can verify and characterize complex prototype ASICs to their limits. Which means you'll send fast ICs to production with the confidence that they won't return for time-consuming and expensive redesign.

You can even go a step further. Its high-throughput software lets you efficiently test small



batch production runs, too.

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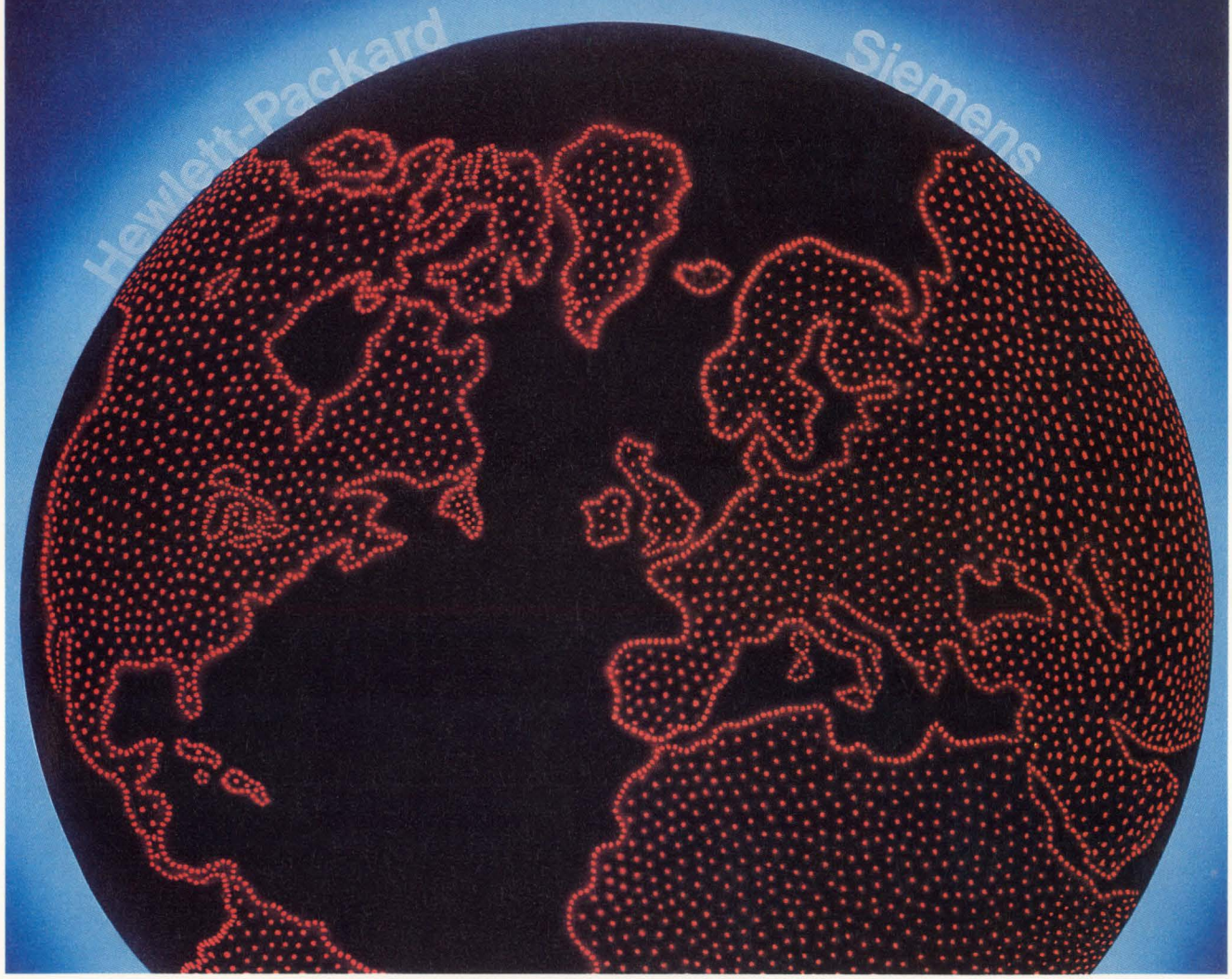

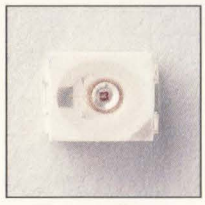

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NEWS BREAKS

EDITED BY SUSAN BUREAU

$199 DOS-BASED STD BUS COMPUTER SUITS INDUSTRIAL TASKS

The MCM-SBC41 single-board computer from WinSystems (Arlington, TX, (817) 274-7553) gives you IBM PC compatibility in a form factor small enough for many embedded applications. You can plug as much as 1M byte of memory into the board's three 32-pin memory sockets. The computer also has three RS-232C channels and a Centronics-compatible parallel port. A watchdog timer, power-failure reset circuit, and low-power sleep mode enable the computer to operate unattended. You can use the board's STD Bus interface for I/O; the computer can also operate independent of the bus. Dissipating less than 3W, the computer, which has a 16-bit NEC V40 CPU, costs $199 (500); $295 for single units.—J D Mosley

VXIBUS SLOT-0 MANAGER CAN CONTROL NON-VXI INSTRUMENTS

The multitalented VX4520 slot-0 resource manager from Colorado Data Systems Inc (Englewood, CO, (303) 762-1640) provides the services required of a VXIbus slot-0 device plus several features that let you reduce the number of slots your system needs. As a C-size, slot-0 device, the $3000 module supplies a 10-MHz clock and a Modid (Module Identification) function that identifies the slot locations of other VXIbus modules. As a VMEbus system controller (VXI incorporates the VMEbus specs), the module provides bus arbitration, interrupt control, and a system-failure monitor. As a VXIbus resource manager, the module performs system-configuration duties such as device identification, address mapping, and memory allocation. An integral IEEE-488 port lets the module configure and map non-VXI instruments as if they were on the VXIbus.—Steven H Leibson

T/H AMPLIFIER BREAKS SPEED AND ACCURACY RECORDS

The AL1210 track-and-hold amplifier from Acculin Inc (Natick, MA, (508) 650-1012) features 8-bit accuracy at a sampling rate of 100M samples/sec and 12-bit accuracy at 50M samples/sec. The amp acquires a 2V step input to within 0.1% and 0.01% in a maximum of 9 and 14 nsec, respectively. The total harmonic distortion produced by sampling a 20-MHz, 2V p-p input at 50M samples/sec is −70 dBc max over the full operating temperature range. The device's supporting specifications are commensurate with its speed and accuracy: It offers a 300-MHz small-signal bandwidth, a 5-μV/°C offset temperature coefficient including pedestal, 1-psec rms aperture jitter, and 50-μV rms total noise. The device's maximum power dissipation is 400 mW. Available in both commercial and industrial grades, the $95 (100) amplifier comes in a 16-pin SOIC. Surface-mount packaging minimizes the pin inductance, which is the limiting factor in the amplifier's settling time.—Anne Watson Swager

SERIAL COMMUNICATIONS CONTROLLER UNBURDENS CPU

The Z16C31 serial controller from Zilog (Campbell, CA, (408) 370-8000) can give your system's CPU a break from handling data communications. The controller provides a full-duplex communications channel with dual baud-rate generators, a clock-recovery phase-locked loop, and an ISDN (Integrated Services Digital Network) time-slot assigner for multiplexed transmissions. The device features two 32-bit DMA channels, each with its own 32-byte FIFO. The DMA channels support several buffer-management schemes and transfer data stored in noncontiguous blocks of

memory without CPU intervention. You can limit the bus-mastership time of the channels to prevent them from hogging your system's bus.

The controller can handle a variety of serial communications protocols, including asynchronous, byte-oriented synchronous, and HDLC (high-level-data link control). You can independently program the transmit and receive protocols as well as their baud rates. You can also program the device to provide sync stripping, preamble transmission, and automatic CRC (cyclic redundancy check) handling. The device will directly connect to the 680x0 and 80x86 processor families and supports both 8-bit and 16-bit bus widths. It costs $34 (1000) and comes in a 68-pin plastic leaded chip carrier.—Richard A Quinnell

OP AMPS SETTLE TO 14-BIT ACCURACY IN <32 NSEC

Two op amps from Comlinear Corp (Fort Collins, CO, (303) 226-0500) provide fast, accurate settling for data-acquisition systems. Over their full operating-temperature range, CLC402 and CLC502 settle to within 0.0025% (for a 2V step), without undershoot or overshoot, in less than 32 nsec (25 nsec typ), ensuring 14-bit accuracy. The amps' settling performance is independent of gain for gains ranging from ±1 to ±8. The $7.65 (1000) CLC402 is pin compatible with and faster than the company's existing CLC400 op amp. The $8.35 (1000) CLC502 offers the same performance as the CLC402 but adds a clamped output for protecting the sensitive and expensive conversion circuitry the op amp may be driving. The clamped amp recovers from overloads within 10 nsec and features a 3-dB bandwidth of 150 MHz for a gain of 2. The 3-dB spec for the CLC402 is 175 MHz. The company offers both products in 8-pin DIPs and 8-lead SOICs.—Steven H Leibson

50-MHz ASIC VERIFIERS COST $300 PER PIN

The ETS 200 family of benchtop ASIC verification testers from Hilevel Technology (Irvine, CA, (714) 727-2100) offers configurations of as many as 512 pins for approximately $300 per pin on a 128-channel system. The testers handle 50-MHz clock rates and 25-MHz data rates and have ±2-nsec pin-to-pin skew. Unlike the manufacturer's ETS 100 family, which is limited to functional-test applications, the ETS 200 testers have 16 timing generators with 500-psec resolution for timing characterization. The devices support split-cycle I/O operation on all pins for testing multiplexed bidirectional buses. Each pin's memory depth is 16k test vectors; memory depth of 64k test vectors is available as an option.—Doug Conner

INTERFACES ADD ISDN CAPABILITIES TO PROTOCOL ANALYZER

Four interface modules from Hewlett-Packard Co (Palo Alto, CA, (800) 752-0900) add basic- and primary-rate ISDN (Integrated Services Digital Network) capabilities to the company's HP 4952A wide-area-network protocol analyzer. The four modules are the HP 18281A ISDN basic-rate monitor and simulation interface; the HP 18282A ISDN primary-rate interface for 1.544M-bps systems; the HP 18283A ISDN primary-rate interface for 3-pin, 2.048M-bps systems; and the HP 18284A ISDN primary-rate interface for 2.048M-bps systems that employ 75Ω BNC connectors. The primary-rate interface modules cost $2500 each, and the monitor/simulation interface module costs $2000. Using the interfaces, the $8540 protocol analyzer with optional memory expansion can handle all coding schemes employed by the ISDN central-office switches now available from the major global-telecommunications companies.
—Steven H Leibson

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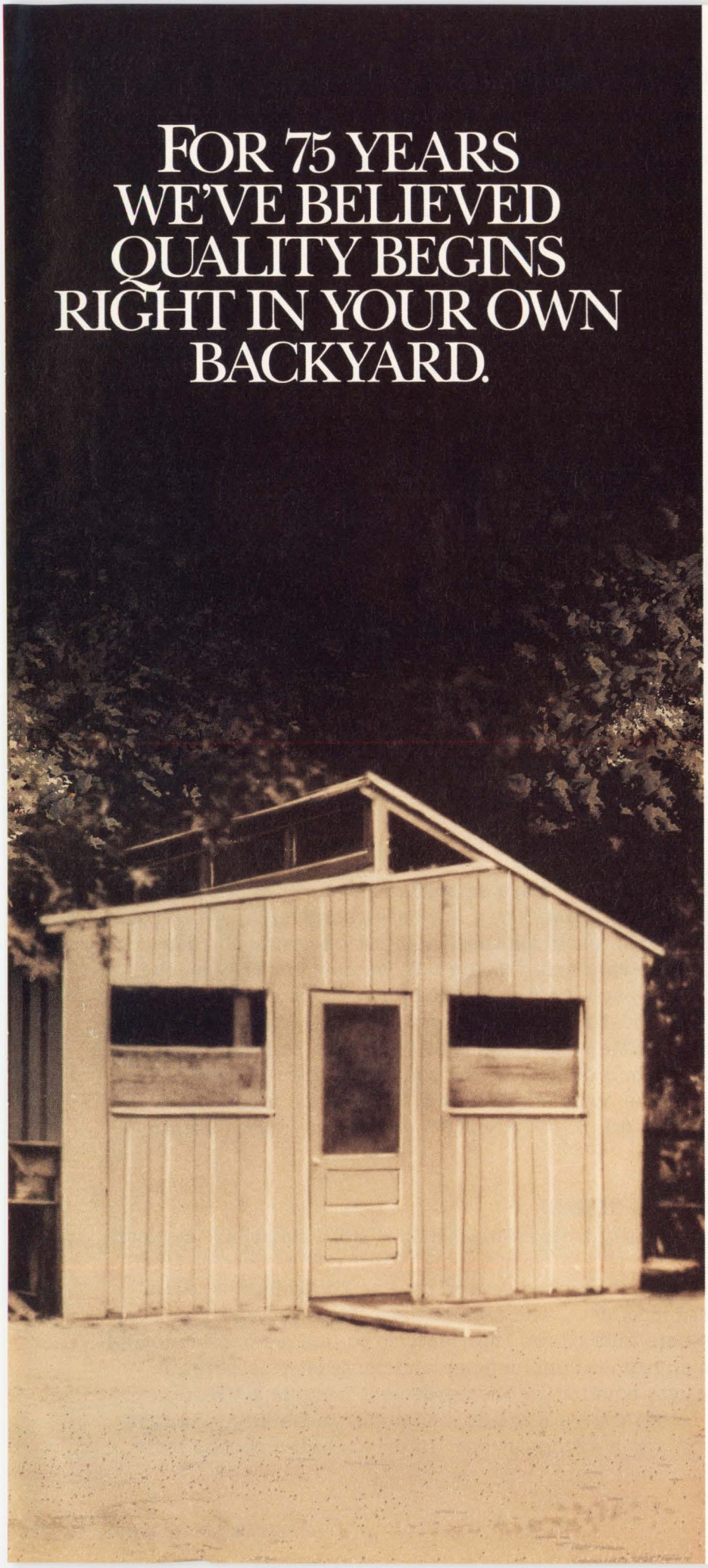

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NEWS BREAKS

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Hewlett-Packard Co (Palo Alto, CA, (800) 752-0900) is renting all the development tools and instruments in its catalog to those who have value-added business contracts with the company. By HP's definition, value-added business partners include software suppliers, systems integrators, resellers, distributors, and consultants. For 2% of the products' list price per month, such companies can rent products approved in their demonstration/development contracts, including workstations, minicomputers, terminals, software, networking products, instruments, and medical equipment. The initial rental agreement lasts for six months after which companies can renew the agreement month by month, purchase the product (65% of the rental fee will be credited to the purchase price), or return the product.—Steven H Leibson

CONTROL CHIP KICK-STARTS COMPUTER SYSTEMS

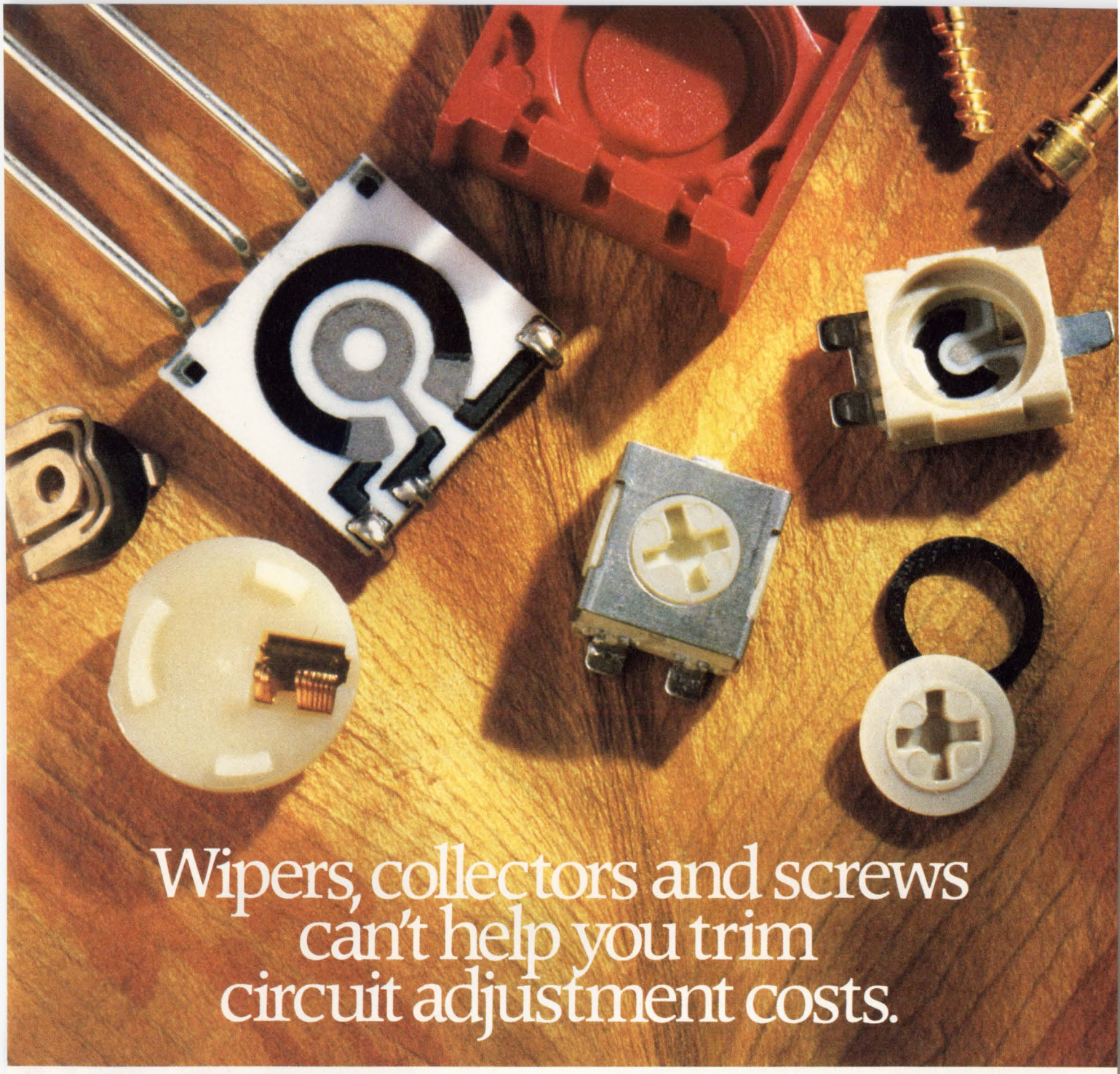
Designing a DS1239 MicroManager chip into your desktop or laptop computer eradicates the need for a power switch. This chip from Dallas Semiconductor (Dallas, TX, (214) 450-0400) lets end users turn their computers on and off with a single keystroke; for automatic booting, you can design the chip to sense an external signal from a telephone or a time clock. The chip can also monitor a second key or signal in case the end user wants to manually reset the CPU without terminating power to the computer. If power fluctuations or software problems cause the CPU to lose control of your computer, a watchdog timer resets the CPU. The chip draws less than 100 nA from its internal lithium battery. This power energizes an optoisolator, which in turn empowers a triac that lets power flow to the computer. The $3.50 (1000) chip also isolates end users from the ac power control, making it easier for you to obtain UL approval for your computer design.—J D Mosley

DOS OPERATES FROM ROM OR DISK

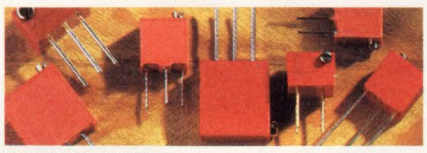
Industrial and non-PC applications that require embedded PCs need operating systems in addition to cloned hardware. ROM-DOS, a low-cost operating system from Datalight (Bothell, WA, (206) 486-8086), provides these applications with the capabilities of Microsoft's DOS 3.2. An independent testing lab, Veritest Inc (Inglewood, CA, (213) 670-5848), has certified the system's compatibility with major DOS application programs. Running both COM and EXE files, the system requires approximately 34k bytes of ROM and consumes as little as 14k bytes of RAM. You can load the operating system to your system from a disk drive, or you can place the system in a ROM. A developer's kit with linkable object modules costs $495; a source code license costs $10,000. You also pay a $6 (5000) royalty fee for each copy you ship. —Steven H Leibson

VHDL'S IMPORTANCE ACKNOWLEDGED

Recognizing the importance of tightly integrating VHDL (VHSIC Hardware Description Language) products with their existing design tools, Valid Logic Systems (San Jose, CA, (408) 432-9400) has agreed to buy the source code to Intermetrics' (Cambridge, MA, (617) 661-1840) VHDL products. The accord gives Valid the right to market future Intermetrics products and allows Intermetrics to license back existing and future products for current customers and defense and contract-related business. Current Intermetrics' products covered by the agreement include a VHDL analyzer/compiler, a full VHDL interactive simulator, and a design-library manager. An upcoming product release will add a graphical user interface and a source-level debugger.—Michael C Markowitz



Wipers, collectors and screws can't help you trim circuit adjustment costs.



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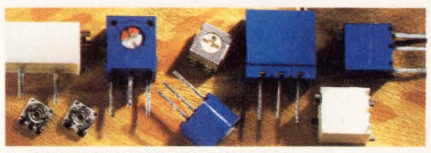

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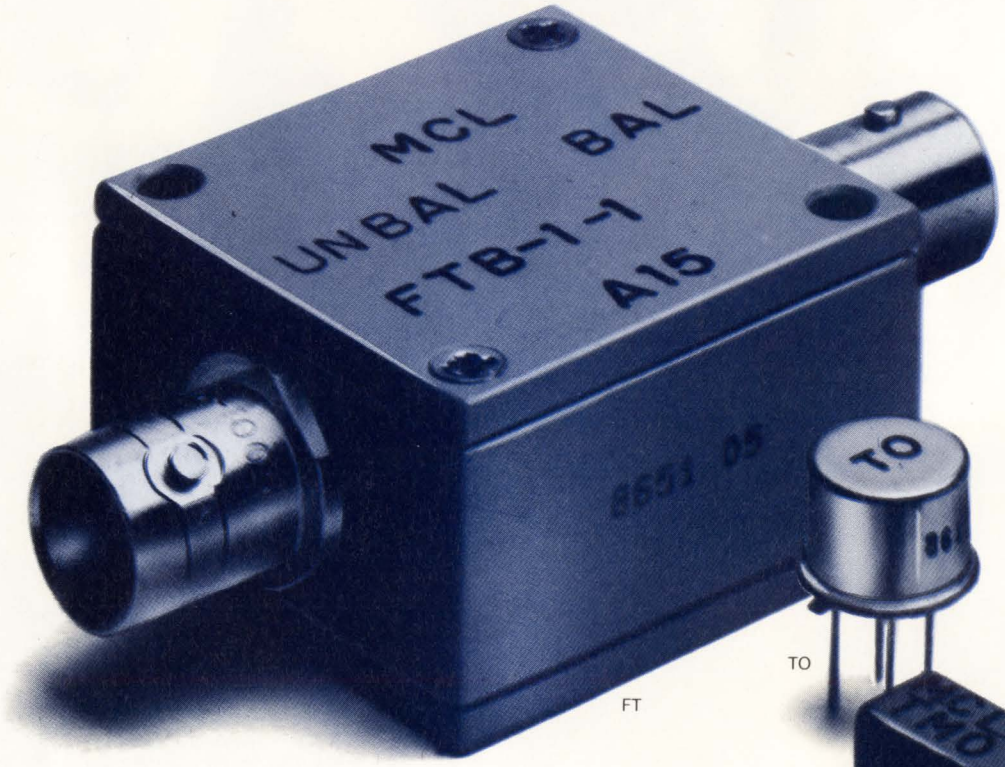
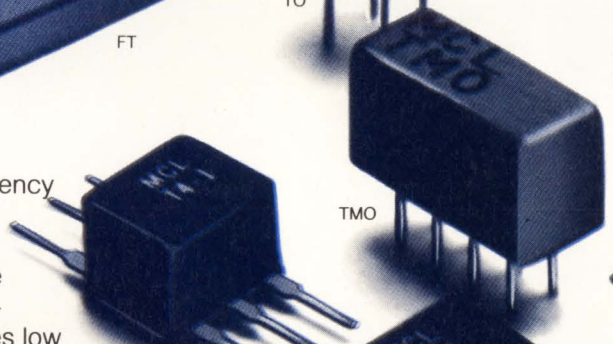
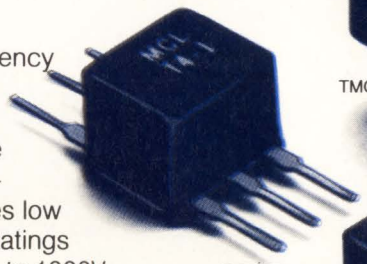


FT

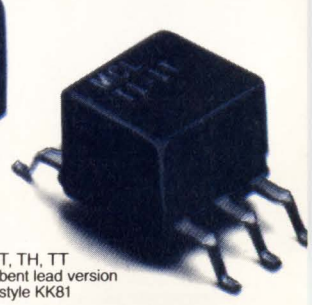
TO



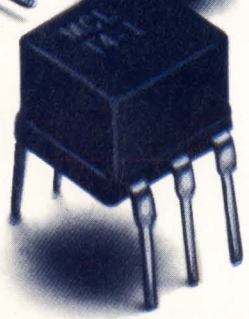
TMO



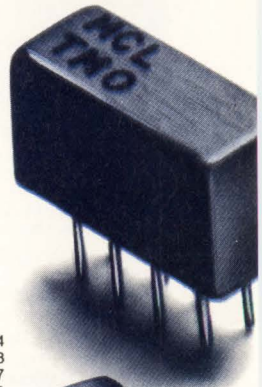
T, TH, TT



T, TH, TT
bent lead version
style KK81



T, TH, TT
bent lead version
style X 65



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case styles
T, TH, case W 38, X 65 bent lead version, KK81 bent lead version
TMO, case A 11, † case B 13 FT, FTB, case H 16
NEW TC SURFACE MOUNT MODELS from 1MHz to 1500 MHz

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MCL NO.	NSN	MCL NO.	NSN
FTB1-1-75	5950-01-132-8034	TMO2-1	5950-01-183-6414
FTB1-6	5950-01-225-8773	TMO2.5-6	5950-01-215-4038
T1-1	5950-10-128-3745	TMO2.5-6T	5950-01-215-8697
T1-1T	5950-01-153-0668	TMO3-1T	5950-01-168-7512
T2-1	5950-01-106-1218	TMO4-1	5950-01-067-1012
T3-1T	5950-01-153-0298	TMO4-2	5950-01-091-3553
T4-1	5950-01-024-7626	TMO4-6	5950-01-132-8102
T9-1	5950-01-105-8153	TMO5-1T	5950-01-183-0779
T16-1	5950-01-094-7439	TMO9-1	5950-01-141-0174
TMO1-1	5950-01-178-2612	TMO16-1	5950-01-138-4593

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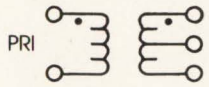
case style number see opposite page		MODEL NO.	Ω RATIO	FREQUENCY MHz	INSERTION LOSS 3dB MHz	INSERTION LOSS 2dB MHz	INSERTION LOSS 1dB MHz	PRICE $ Qty (1-9)
A* 	T	T1-1T	1	.05-200	.05-200	.08-150	.2-80	4.45
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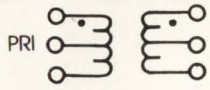
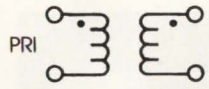
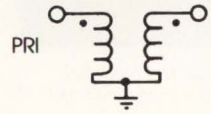
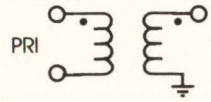
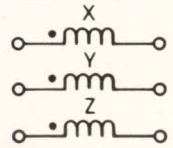
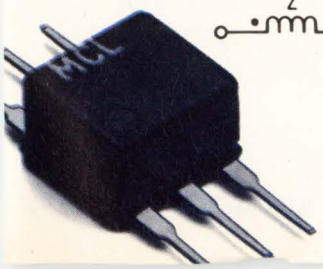
		T2-1T	2	.07-200	.07-200	.1-100	.5-50	4.95
		T2.5-6T	2.5	.01-100	.01-100	.02-50	.50-20	4.95
		T3-1T	3	.05-250	.05-200	.1-200	.5-70	4.95
		T4-1	4	.2-350	.2-350	.35-300	2-100	3.25
		T4-6T	4	.02-250	.02-250	.05-150	0.1-100	4.45
		T5-1T	5	.3-300	.3-300	.6-200	.5-100	4.95
		T8-1T	8	.03-140	.03-140	.10-90	1-60	7.95
		T13-1T	13	.3-120	.3-120	.7-80	5-20	4.95
		T16-6T	16	.03-75	.03-75	.06-30	.1-20	5.65
	TH	T4-1H	4	10-350	10-350	15-300	25-200	5.95
	TMO	TMO1-1T	1	05-200	.05-200	.08-150	.2-80	7.95
		TMO2-1T	2	.07-200	.07-200	.1-100	.5-50	8.45
		†TMO2.5-6T	2.5	.01-100	.01-100	.02-50	.05-20	8.45
		†TMO3-1T	3	.05-250	.05-250	.1-200	.5-70	7.95
		TMO4-1	4	.2-350	.2-350	.35-300	2-100	6.25
		TMO5-1T	5	.3-300	.3-300	.6-200	5-100	8.45
		TMO13-1T	13	.3-120	.3-120	.7-80	5-20	8.45
B* 	TT	TT1-6	1	.004-500	.004-500	.02-200	.1-50	6.95
		TT1.5-1	1.5	.075-500	.075-500	.2-100	1-50	5.95
		TT2.5-6	2.5	.01-50	.01-50	.025-25	.05-10	6.45
		TT4-1	3	.05-200	.2-50	.2-50	1-30	5.95
		TT4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	6.95
		TT25-1	25	.02-30	.02-30	.05-20	.1-10	9.95
	TTMO	TTMO25-1	25	.02-30	.02-30	.05-20	.1-10	11.95
		TTMO1-1	1	.005-100	.005-100	.01-75	.05-40	11.45
		TTMO4-1A	4	0.1-300	0.1-300	0.2-250	0.3-180	13.95
C 	T	T1-1	1	.15-400	.15-400	.35-200	2-50	3.25
		T1.18-3	1.18	0.01-250	0.01-250	0.02-200	0.03-50	5.65
		T1-6	1	.01-150	.01-150	.02-100	.05-50	5.65
		T1.5-1	1.5	.1-300	.1-300	.2-150	.5-80	4.45
		T1.5-6	1.5	.02-100	.02-100	.05-50	0.1-25	5.65
		T2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	4.45
		T4-6	4	.02-200	.02-200	.05-150	.1-100	4.45
		T9-1	9	.15-200	.15-200	.3-150	2-40	3.95
		T16-1	16	.3-120	.3-120	.7-80	5-20	4.45
		T36-1	36	.03-20	.03-20	.05-10	.1-5	6.95
	TO	TO-75	1	10-500	—	10-500	40-250	6.95
	TH	T1-1H	1	8-300	8-300	10-200	25-100	5.95
		T9-1H	9	2-90	2-90	3-75	6-50	6.45
		T16-H	16	7-85	7-85	10-65	15-40	6.45
	TMO	TMO1-02	1	1-800	1-800	2-500	—	9.45
		TMO1-1	1	.15-400	.15-400	.35-200	2-50	6.25
		TMO1.5-1	1.5	.1-300	.1-300	.2-150	.5-8	8.45
		†TMO2.5-6	2.5	.01-100	.01-100	.02-50	.05-20	7.95
		†TMO4-6	4	.02-200	.02-200	.05-150	.1-100	7.95
		TMO6-1	6	.3-200	.3-200	.5-150	5-50	7.95
		TMO9-1	9	.15-200	.15-200	.3-150	2-40	7.95
		TMO16-1	16	.3-120	.3-120	.7-80	5-20	7.95
D 	T	T2-1	2	.050-600	.050-600	.1-400	.5-200	3.95
		T3-1	3	.5-800	.5-800	2-400	—	4.45
		T4-2	4	.2-600	.2-600	.5-500	2-250	3.95
		T8-1	8	.15-250	.15-250	.25-200	2-100	3.95
		T14-1	14	.2-150	.2-150	.5-100	2-50	4.95
	TMO	TMO2-1	2	.050-600	.050-600	.1-400	.5-200	7.95
		TMO3-1	3	.5-800	.5-800	2-400	—	8.45
		TMO4-2	4	.2-600	.2-600	.5-500	2-250	7.95
		TMO8-1	8	.15-250	.15-250	.25-200	2-100	7.95
		TMO14-1	14	.2-150	.2-150	.5-100	2-50	8.45
	FT	FT1.22-1	1.22	.005-100	.005-100	.01-50	.05-25	35.95
		FT1.5-1	1.5	.1-400	.1-400	5-200	1-100	35.95
E 	FTB	FTB-1	1	.2-500	.2-500	.5-300	1-100	36.95
		FTB1-6	1	.01-125	.01-125	.05-50	.1-25	36.95
		■FTB-1-75	1	.5-500	.5-500	5-300	10-100	36.95
F 	T	T-622	1	0.1-200	0.1-200	0.5-100	5-80	3.25
		T626	1	0.01-10	0.01-10	0.2-5	.04-2	3.95



■ Denotes 75 ohm models

* FOR A AND B CONFIGURATIONS

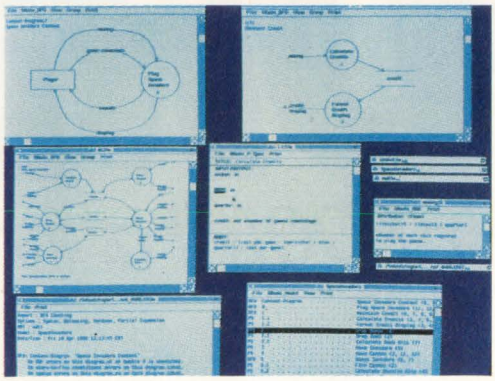
Maximum Amplitude Unbalance
0.1 dB over 1 dB frequency range
0.5 dB over entire frequency range

Maximum Phase Unbalance
1.0° over 1 dB frequency range
5.0° over entire frequency range

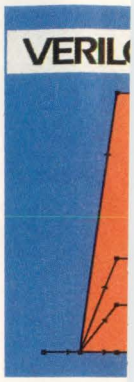
C72-2 REV. B

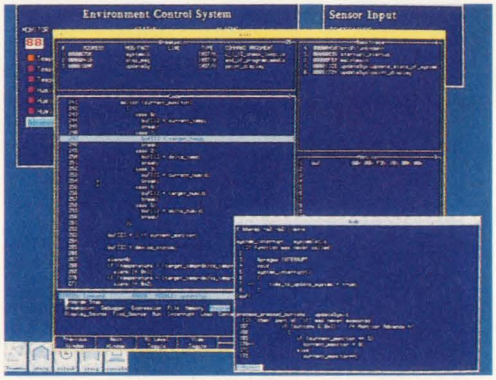
CIRCLE NO. 88

HP SoftBench: A software development environment with an integrated set of program development and integration platform tools.



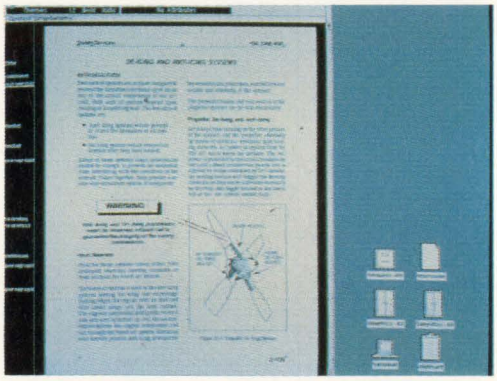
Cadre Teamwork: A family of tools that implement system analysis and software design methodologies.



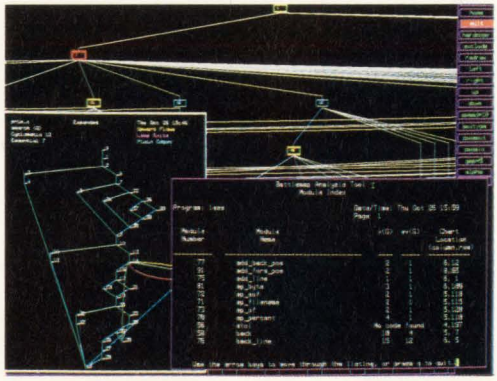


HP AxDB Debugger: Displays microprocessor code, stack backtrace, and variables. Test coverage window shows statements not executed during test.

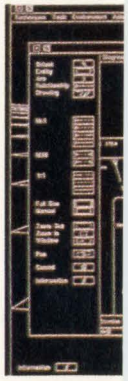
Best CA

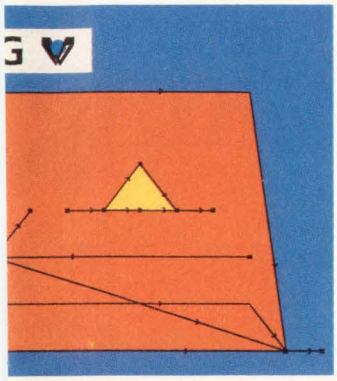


Interleaf Technical Publishing Software: A documentation software and management system that features integrated text and graphics.

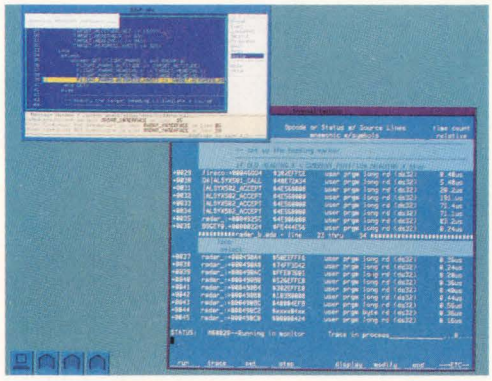


McCabe Test Tools: An automated software testing and reverse engineering application.

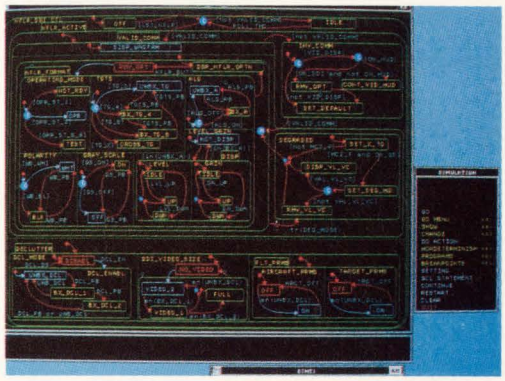




Verilog LOGISCOPE: Automated testing of source code analysis for reverse engineering.

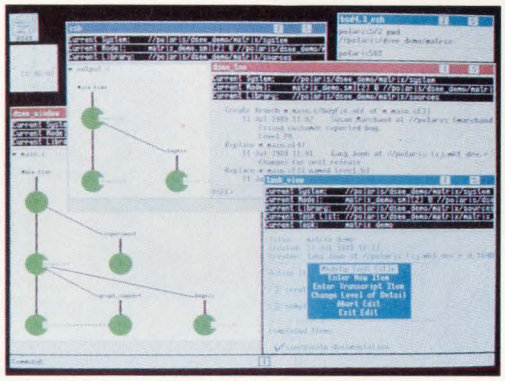


Ada: A development environment that allows real-time symbolic debugging, available from multiple vendors.

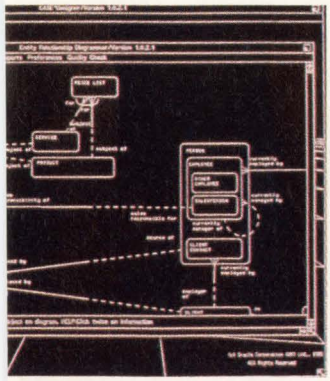


i-Logix Statemate: Allows dynamic analysis of complex systems long before design and implementation.

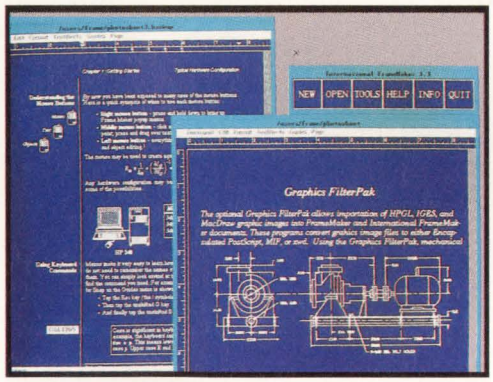
SE scenario.



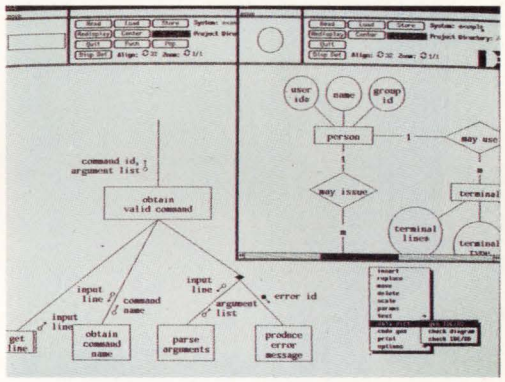
Apollo DSEE: Offers unequaled software development support for complex, team-oriented projects.



ORACLE: An application for structured, computer-assisted development of systems solutions.



Frame FrameMaker®: Easy-to-use text, graphics, and layout tools for documentation.



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Your software release dates are continually postponed. Defects are discovered late in your development process. And your team can't find contemporary solutions to existing problems.

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With the HP CASEdge program and our software suppliers, we offer a broad selection of development tools for the software engineering industry. And a strong commitment to helping your team find, evaluate, and implement the right software engineering tools and best practices for the task at hand.

HP CASEdge solutions speed the automation of specification, design, implementation, debugging, and maintenance. And decrease development costs while getting your products to market faster.

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CIRCLE NO. 89

you've put so much it perfect.

OF ICs, YOU GET OUT OF IT WHAT YOU PUT INTO IT.

COMPUTING		COMMUNICATIONS		CONTROL	
APPLICATION	**PRODUCT**	**APPLICATION**	**PRODUCT**	**APPLICATION**	**PRODUCT**
Workstations	● Advanced BiCMOS Logic ● High Speed ASICs ● Futurebus Chip Set ● High Speed PAL®-type Devices ● High Performance MCUs ● SRAMs	Cellular Communications	● Cellular Chip Set ● Frequency Synthesizers	Automotive Control Systems	● 8-bit 80C51-based MCUs ● OTP EPROMs ● Linear/Digital/Mixed Mode ASICs
Personal Computers	● High Density ASICs/PLDs ● DRAM Controllers ● OTP EPROMs ● FLASH Memory	Mobile Telephony	● Paging ICs ● Frequency Synthesizers	Consumer Appliances and Entertainment	● A/D MCUs ● LCD Displays ● Audio Circuitry ● Dolby Noise Reduction ● Frequency Synthesizers
Desk Top Video	● A/D Converters ● Digital Color Decoders	FAX/Modems/ Features Phones	● 8-bit 80C51-based MCUs ● E^2PROM ● LCD Drivers ● Dialers ● Speech Circuits ● RF Chip Set	Industrial Control & Robotics	● Advanced BiCMOS Logic ● UV/OTP EPROM MCUs ● Real-Time Bus Communications Controller
Peripheral Products	● 8-bit 80C51-based MCUs ● Zero Power PLDs ● Programmable Sequencers ● 3-State ECL Transceivers	DataComm LANs	● Ethernet Chip Set ● 100-Mbit Fiber ● High Speed PLDs ● Advanced BiCMOS Logic	Portable Instrumentation	● Low Voltage/Power MCUs ● Advanced CMOS Logic ● LCD Drivers
		Multi-Protocol	● Dual Universal Serial Controller ● UARTs and DUARTs		

As illustrated above, we're listening to customer needs and developing products in three focused areas: computing, communications and control.

This includes products based on our advanced BiCMOS technology, QUBiC. Developed from our strength in bipolar technology and fully integrated with our sub-micron CMOS technology, QUBiC gives you nearly twice the speed of previous-generation bipolar ICs. With CMOS power savings. We're incorporating QUBiC into all our product families, creating a new class of high-performance devices.

Philips Components-Signetics is committed to the military market, with over 80% of our ICs meeting MIL-SPEC certification. This commitment is evident in our Class S domestic assembly plant and DESC-certified wafer fabs.

To learn how Philips Components-Signetics helps you make the perfect design, call today for more information: 800-227-1817, ext. 711D.

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For example, design engineers can independently clock, reset and preset each of ten output logic macrocells. These individually programmable clocks enable asynchronous designs, taking your system performance to even higher levels.

If your design is ready for the big time, call **1-800-FASTGAL**, and ask for dept. 203. We'll send you free samples and a data-book describing our entire line of high speed E²CMOS GAL devices. Fast.

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Circle 75 for Literature **Circle 76 for Employment Information**

SIGNALS & NOISE

"Peripheral processor" mode allows mating

In John Gallant's article, "Floating-Point Chips Boost Microprocessor Performance" (EDN, June 7, 1990, pg 63), he notes that the Motorola 68881/68882 and Texas Instruments' TMS34082 do not mate with general-purpose microprocessors. Actually, both have a "peripheral processor" mode that does allow use of any μP that has the appropriate interface circuitry to address the chips. The 68881/82 can size the data bus to either 32, 16, or 8 bits, depending on the needs of the main processor. And you can program the TMS34082 in its own assembly language, allowing development of custom math routines. The 34082 can address 64k bytes each of program and data long words (32k bits) for custom programming.

Tony Lewis
Seven-L Engineering
Raleigh, NC

Cheers for article; jeers for Unix

The article by Charles H Small on Unix (EDN, June 7, 1990, pg 88) was well timed and much needed. Engineers hate to work on things without schematics, and Unix is the worst "black box" I've seen. Thanks for the peek under the hood.

Noor S Khalsa, Senior Engineer
EG&G Inc
Los Alamos, NM

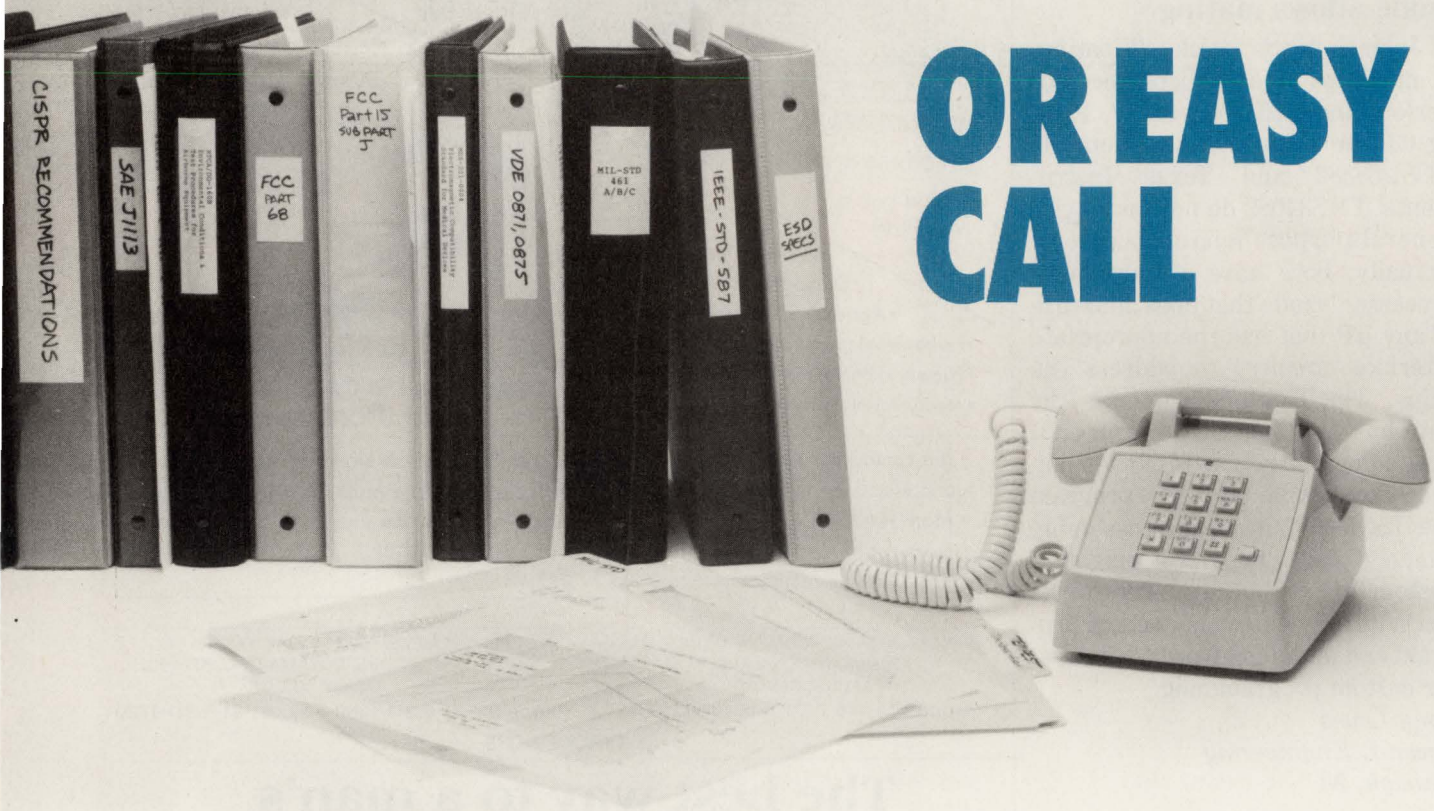
Correction

Because of erroneous information, some of the specifications for the call-back modem from B&B Electronics Manufacturing Co was incorrectly published (EDN, June 7, 1990, pgs 164-165). The product coverage should say that the modem operates at 300, 600, 1200, 2400, 4800, 9600, and 19,200 baud with automatic baud-rate selection, and it costs $149.95. EDN

FOR EMI SHIELDING COMPLIANCE:

HARD WORK...

OR EASY CALL



Faced with designing or testing a product which must comply with one of the many commercial or military EMI specifications? You have two choices:

You can dig through the mountain of published material...and still not be much further ahead.

Or, you can make one easy phone call to Chomerics. Because whatever standards you're dealing with, our people know them inside and out. No other supplier delivers the combination of knowledge, products, and services to make your EMI problems disappear.

Design Help

Call us early on in the design phase of your product and take advantage of our no-charge EMI design review. We'll help you get it right the first time.

Applications Assistance

With your design criteria in mind, we'll look across the full range of EMI shielding possibilities, and provide detailed drawings and prototypes on short notice.

EMI Testing

Our depth of experience becomes very important when it's time to test your system. The fact that we operate comprehensive military and commercial testing facilities, with on-site design, applications support, and materials manufacturing, is a real advantage to our customers.

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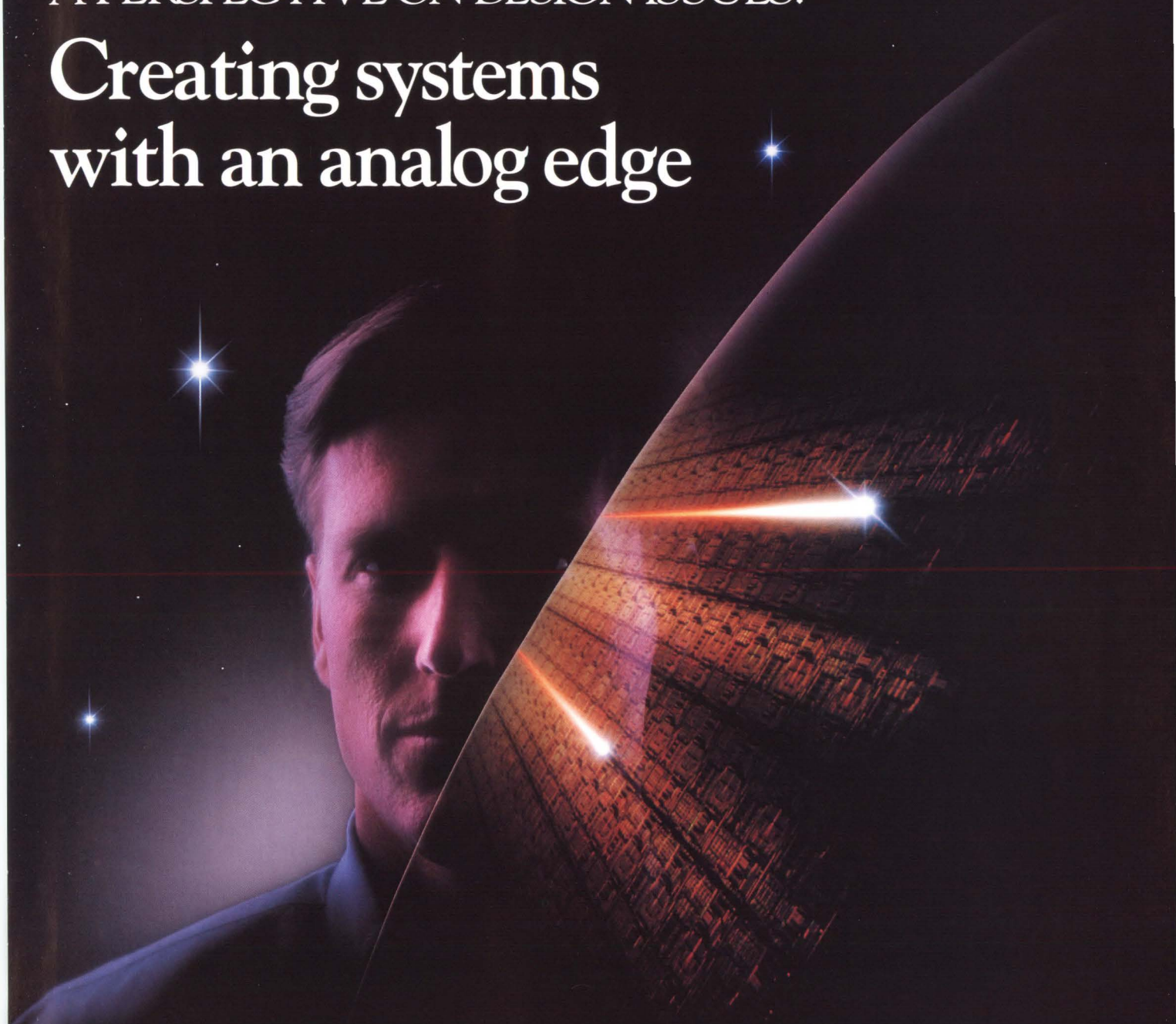
TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

Creating systems with an analog edge



IN THE ERA OF

MegaChip TECHNOLOGIES

Advanced Linear can help you raise system performance levels.

A leadership family of analog circuits from Texas Instruments is helping designers meet difficult design challenges.

The evidence is strong. Throughout the design community, systems using the new breed of Advanced Linear functions from Texas Instruments are achieving the keener performance edges that can spell marketplace success.

TI's new analog devices are enabling design engineers to link digital brains to analog worlds more effectively and efficiently than ever before. Some offer new standards of accuracy or speed while others are highly integrated devices combining analog and digital functions on a single chip. The result is superior system performance and design flexibility.

These Advanced Linear functions are the result of leadership process technologies that we at TI firmly believe are the key to the advanced analog devices your future applications will demand.

Intelligent power for automobiles

Designers in the automotive industry face a tough challenge: Handle high reverse voltages and achieve rapid load turnoff while providing fault protection, detection, and reporting and efficient load management. To provide the needed intelligent power devices, we developed one of our newest process technologies, Multi-EPI Bipolar. It is unique because it can combine rugged power transistors with intelligent control functions.

The resulting circuits are now providing reliable, cost-efficient control of solenoids and valves in such automotive applications as antiskid braking systems, electronic transmission controls, and active suspension systems.

Other industry segments are also benefiting from TI's Advanced Linear process technologies. Here are a few of the winning designs to which we have helped add an analog edge:

Toledo Scale

Challenge: Improve the accuracy of point-of-purchase scales by eliminating drift over time and temperature.
Solution: The TI TLC2654 Chopper op amp. Our Advanced LinCMOS™ process makes possible chopping frequencies as high as 10 kHz, reducing noise to the lowest in the industry.

Pulsecom

Challenge: Develop a linecard capable of driving low-impedance loads with greater precision.
Solution: Our TLE206X family of JFET-input, low-power, precision operational amplifiers. These devices offer outstanding output drive capability, low power consumption, excellent dc precision, and wide bandwidth. Fabricated in our Excalibur process, they remain stable over time and temperature.

Leitch Video

Challenge: Design a compact, cost-efficient direct broadcast satellite TV descrambler for consumer use.
Solution: TI's TLC5602 8-bit Video DAC. Our LinEPIC™ process combines one-micron CMOS with precision analog to satisfy the demands of the application for video speeds and low-power operation.

U.S. Robotics

Challenge: Build a modem for high-speed data transmission between computers; allow flexible operation and minimize data errors.
Solution: Our TLC32040 Analog Interface Circuit (AIC). A product of our Advanced LinCMOS process, the AIC combines programmable filtering, equalization, and 14-bit A/D and D/A converters with such digital functions as control circuitry, program registers, and a DSP interface.

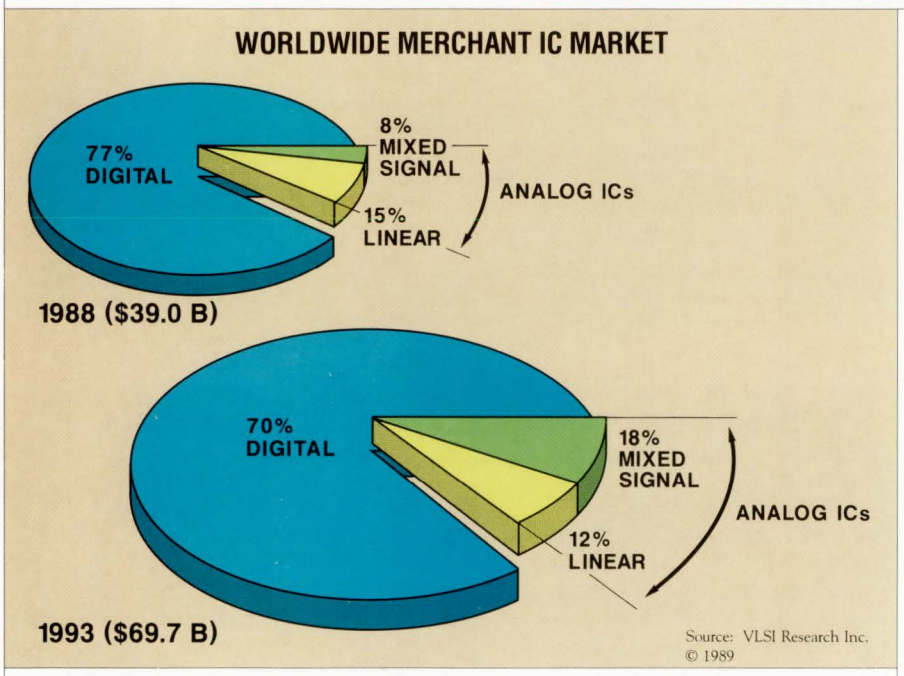
Xerox

Challenge: Cut component count and cost of copier systems while boosting reliability.
Solution: Our TPIC2406, a top-performance peripheral driver in a standard DIP package that is capable of driving heavy loads. It is fabricated using our Power BIDFET™ process which permits greater circuit density and incorporates CMOS technology for low total power dissipation.

Mr. Coffee

Challenge: Design an intelligent coffee maker that brews faster, maintains optimum temperature, shuts off automatically, and has a built-in cleaning cycle.
Solution: Our LinASIC™/LinBiCMOS™ capability permits us to combine both analog and digital library cells with custom analog cells. This results in cost-efficient integration of temperature monitoring, timing, and high-current outputs on a single control chip.

All of these examples point to one conclusion: TI's Advanced Linear functions are adding an analog edge to many system designs. They are contributing significantly to the enhanced system performance that marks a market winner.



Helping you implement your designs in a changing world.

An increasing share of the total analog market is being captured by mixed-signal devices. As they gain more widespread acceptance, they are driving the expansion of the overall analog market (*see above*).

Changes such as this are the order of the day in the IC marketplace. Texas Instruments continues to provide not only the high-performance circuits you need but also the depth of experience, support, and service fundamental to successful completion of your designs.

Experience: Building on three decades in ICs

We at TI can successfully meet your requirements for mixed-signal devices because we have acquired the necessary knowledge from 30 years of experience in developing both analog and digital functions. We have also drawn upon our digital ASIC strengths in developing our LinASIC capabilities.

Support: Speeding our chips to you

The faster we move new products through our design cycles, the faster you can get through yours. We employ a wide variety of design-automation tools and sophisticated software to speed our development process.

Service: Providing a surety of supply

However advanced our circuits may be, they are of little value if they are inaccessible to you. TI operates on the principle of global coverage, local service. We manufacture semiconductors in 13 countries and operate support centers in 22. We have product and applications specialists, designers, and technicians around the world. They are linked by one of the world's largest privately owned communications networks so that we can bring you our best — circuits and support — from wherever they may be to wherever you are.

Keeping our communications open

The relationship between you as customer and us as vendor is vital: You are our chief source for firsthand information that can help guide us in developing the circuits you will need for your future designs. We at TI welcome your comments and your suggestions.

TI's Leadership Analog Processing Technologies

LinBiCMOS — Combines Advanced LinCMOS, digital ASIC CMOS, and up to 30-V bipolar technologies to allow the integration of digital and analog standard cells and handcrafted analog components on a monolithic chip.

LinEPIC — One-micron CMOS double-level metal, double-level polysilicon technology, which adds highly integrated, high-speed analog devices to the high-performance digital EPIC process.

Advanced LinCMOS — An N-well, silicon-gate, double-level polysilicon process featuring improved resistor and capacitor structures and having three-micron minimum feature sizes.

Power BIDFET — Merges standard linear bipolar, CMOS, and DMOS processes and allows integration of digital control circuitry and high-power outputs on one chip. Primarily used for circuits handling more than 100 V at currents up to 10 A.

Multi-EPI Bipolar — A very cost-effective technology that utilizes multiple epitaxial layers instead of multiple diffusion steps to reduce mask steps by more than 40%. Used to produce intelligent power devices that can handle loads as high as 20 A and voltages in excess of 100 V.

Excalibur — A true, single-level poly, single-level metal, junction-isolated, complementary bipolar process developed for high-speed, high-precision analog circuits providing the most stable op amp performance available today.

If you would like a more detailed explanation of our Advanced Linear process technologies, please call **1-800-336-5236, ext. 3423**. Ask for a copy of our *Advanced Linear Circuits* brochure.

TEXAS INSTRUMENTS

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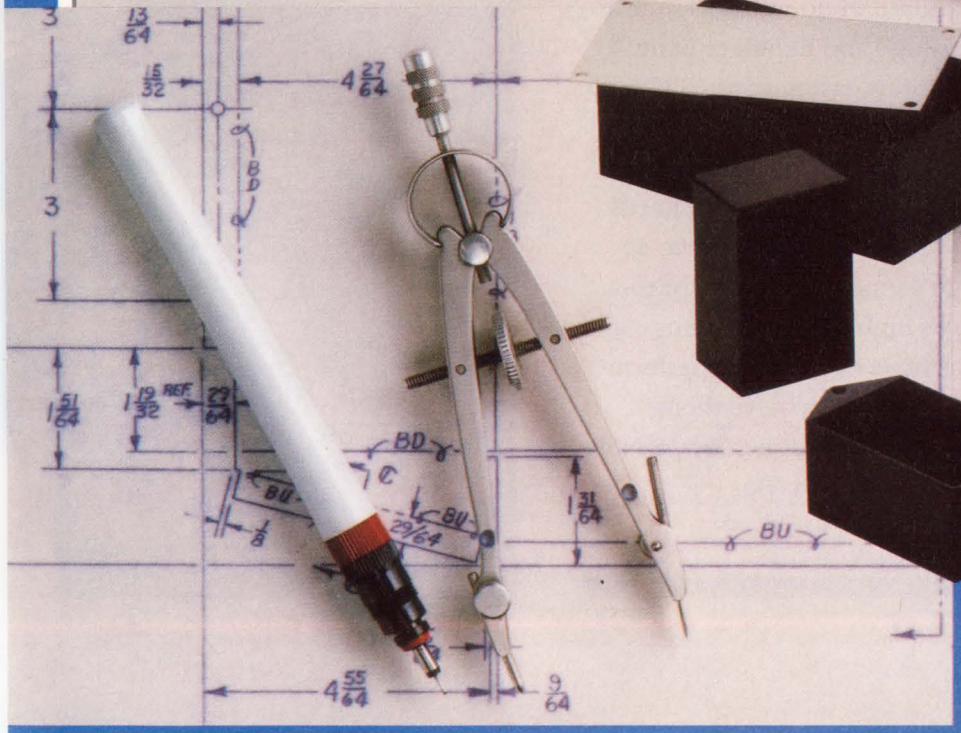

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CIRCLE NO. 92

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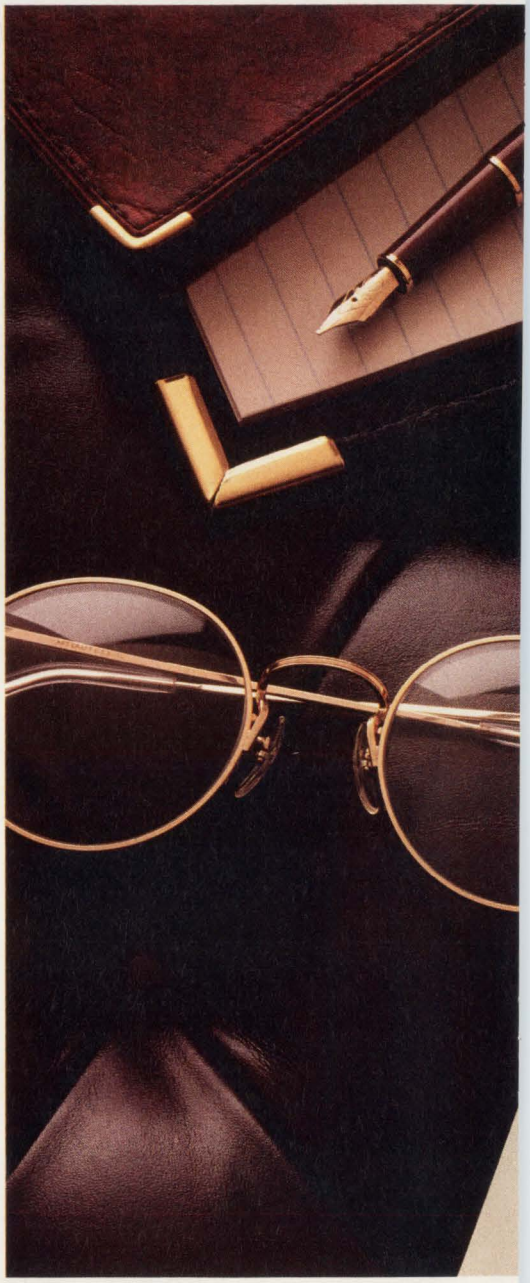

Transforming technology into customer solutions

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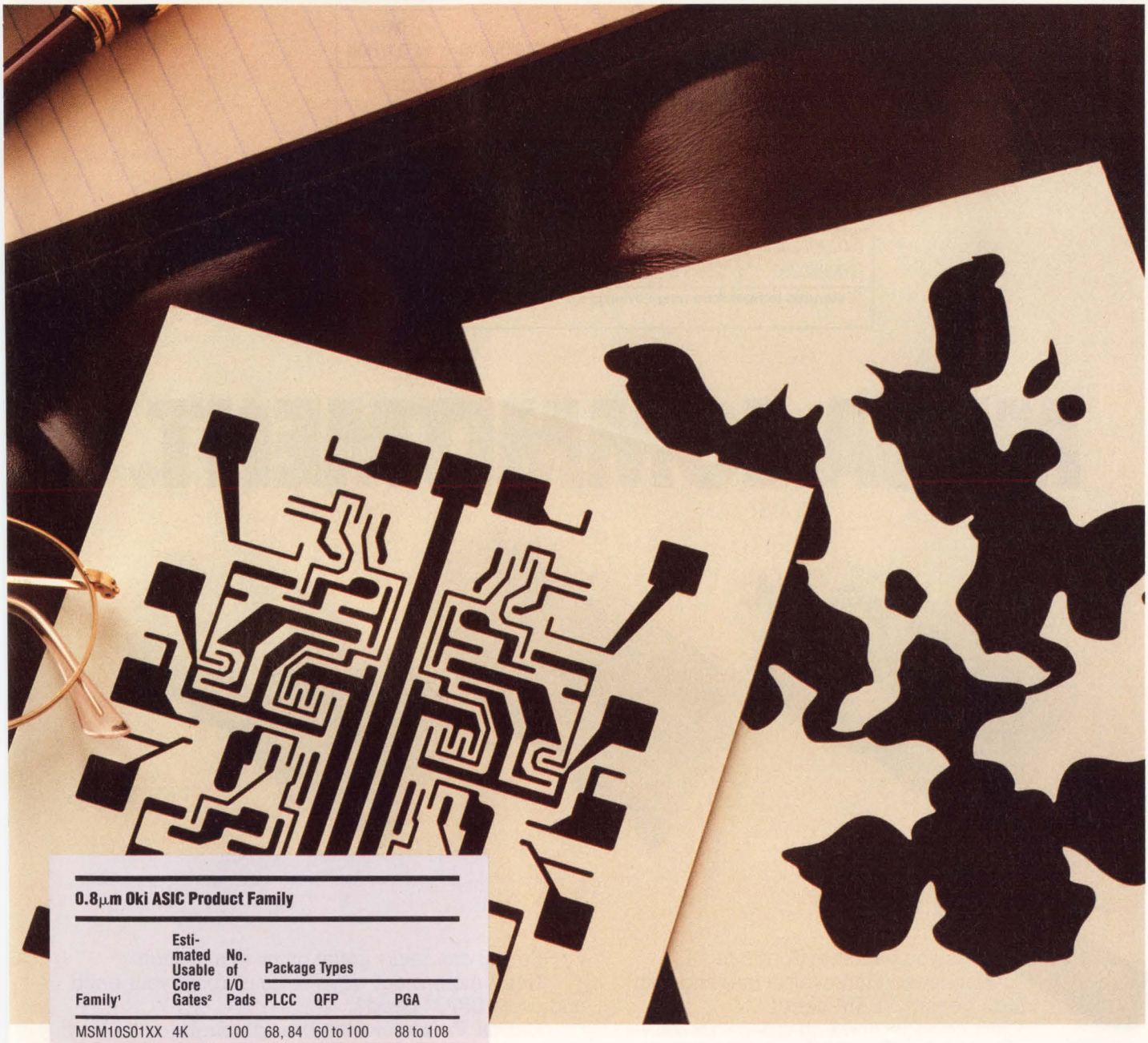

0.8μm Oki ASIC Product Family

Family[1]	Estimated Usable Core Gates[2]	No. of I/O Pads	Package Types		
			PLCC	QFP	PGA
MSM10S01XX	4K	100	68, 84	60 to 100	88 to 108
MSM10S03XX	12K	160	68, 84	80 to 144	88 to 132
MSM10S05XX	22K	208		120 to 208	108 to 208
MSM10S09XX	36K	272		144 to 272*	108 to 256
MSM10S11XX	47K	304		144 to 304*	132 to 301
MSM10S18XX	72K	384		144 to 304*	208 to 340
MSM10S23XX	92K	424		144 to 304*	240 to 340

[1]Other products are under development
[2]Up to 100% utilization increase with 3-layer metal, memory, and other regular blocks
*JEDEC metric packages

OKI Semiconductor

785 North Mary Avenue
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Telephone 1-800-654-6994

Verilog is a registered trademark of Cadence Design Systems, Inc.
Explorer Rene is a trademark of Mentor Graphics Corporation.

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SONY HIGH-DENSITY SRAMS				
MODEL	CONFIG.	SPEED (ns)	PACKAGING	DATA RETENTION
CXK581000P*	128K x 8	100/120	DIP 600 mil	L, LL
CXK581000M*	128K x 8	100/120	SOP 525 mil	L, LL
CXK581100TM*	128K x 8	100/120	TSOP	L, LL
CXK581100YM*	128K x 8	100/120	TSOP (reverse)	L, LL
CXK581001P	128K x 8	70/85	DIP 600 mil	L
CXK581001M	128K x 8	70/85	SOP 525 mil	L
CXK581020SP	128K x 8	35/45/55	SDIP 400 mil	
CXK581020J	128K x 8	35/45/55	SOJ 400 mil	

*Extended temperature range available.

L = Low power.
LL = Low, low power.

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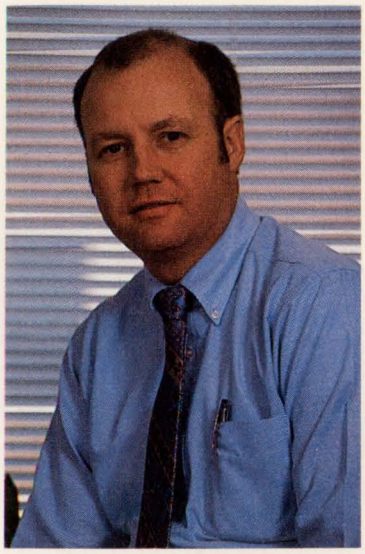
SONY®

Show a little humility



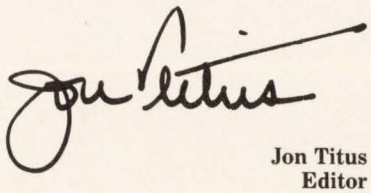
During the early '50s and '60s, Long Island, NY saw tremendous growth. Companies such as Grumman, Republic, and Hazeltine were growing rapidly and employees needed places to live. The potato and cabbage fields on the north shore of Long Island sprouted developments of tract housing. My father, a real-estate attorney, told us that many of the newcomers lacked humility. He saw beautiful new homes that displayed an elegant lamp, table, and curtains in the front window, but otherwise the houses were almost bare of furniture. The owners were too proud to start with a smaller investment and work their way up at a reasonable pace. Their homes were hollow displays of pride and cockiness—often to be lost in bankruptcy court.

Somewhat the same problem pervades today's computer-aided-design and -engineering industry. A look at the lavish displays, hospitality suites, and other accoutrements on display at the 1990 Design Automation Conference (DAC) would have convinced you that there is a problem. I have seen much the same behavior in the computer industry, and it is disappointing to see the CAE and CAD companies repeat the process. Perhaps it is something that all new industries must go through.

Still, it is hard to reconcile the CAE and CAD companies' trappings of power and wealth with reality. Few of the companies involved in the industry are making such fabulous profits to warrant large expenditures on demonstration suites, limousines to and from meetings, and large, expensive booths. Customers I spoke with wondered how the companies could afford such expenses when they weren't yet shipping the products they promised many months ago. The customers also wondered why the money spent at DAC wasn't being spent on developing the promised products instead of on making a splash at a relatively small show.

In all industries there must be a balance between spending money on product development and spending it on product publicity. However, if the display at DAC represents the industry's apportionment of resources, many CAE companies must be making measurements on unbalanced scales. If more stockholders attended DAC, the situation might change. After all, stockholders want a return on their investment, not constant spending on glamour and hype as product-shipment schedules continue to slip. If the electronic CAE and CAD industry hopes to reach maturity, it must start by showing some humility.

Jesse H Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2),
1977, 1976, 1975
American Society of
Business Press Editors Award
1988, 1983, 1981



Jon Titus
Editor

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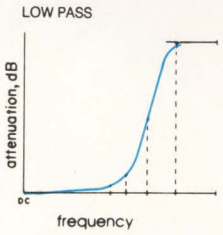

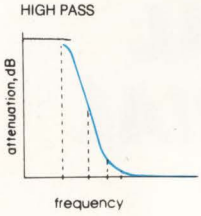

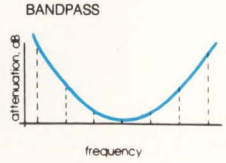

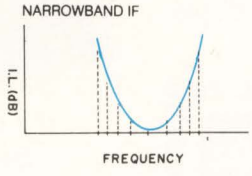

low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	(loss>40dB) Max.	Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	(loss>40dB) Min.	VSWR pass-band typ.	VSWR stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	Max. F4	(loss > 20 dB) Min. F5	Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95

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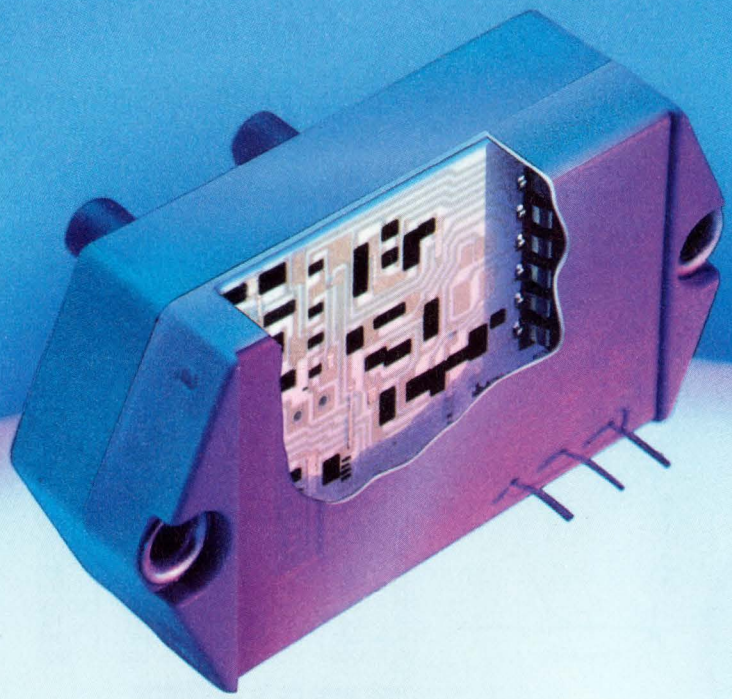

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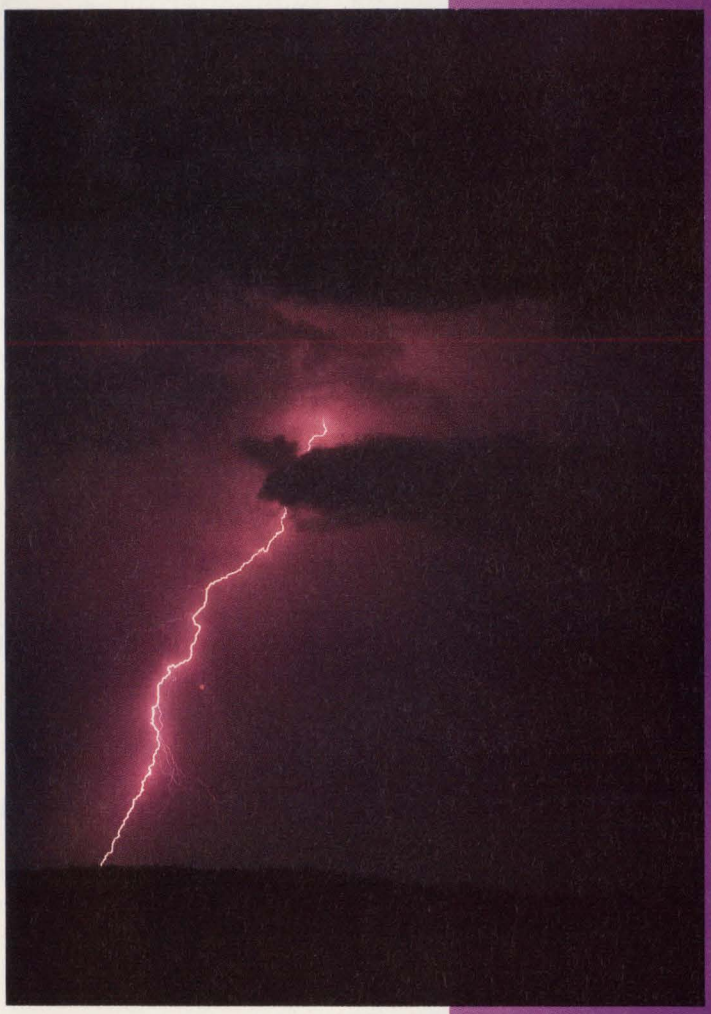
Vote for Innovation

INNOVATION

We're very pleased with the lineup of finalists that EDN's editors chose in our Innovations of the Year and Innovator of the Year competition. Now it's up to you to vote. On the following pages you'll find brief descriptions of the products and the people that our editors chose as finalists. Carefully consider these finalists, and make your vote on the postage-paid ballot that appears at the end of this article. You can have one vote in each product category and one vote for one of the three innovators. In the power-supply category, our judges found only one product innovative enough to qualify; we present it here with the finalists to give it the recognition it deserves.



After the votes are counted, EDN will announce the winners and honor them at an awards banquet during Wescon/90 in Anaheim, CA, this November. We'll also print a special section in our January issues that will include descriptions of the winning products and people.

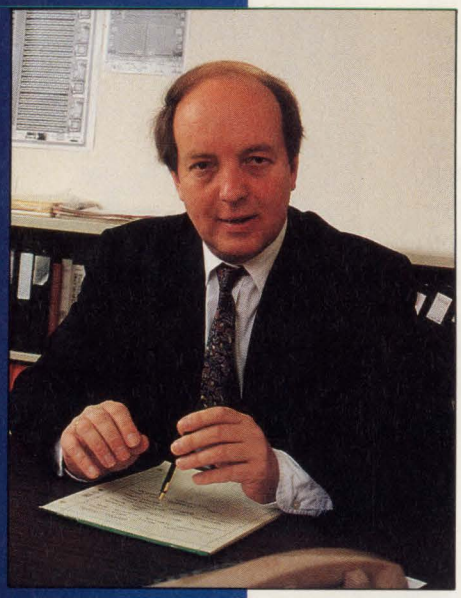
We appreciate the enormous amount of time and effort that it took to nominate the innovative people and products for these awards. Trying to single out the finalists from your nominations was a formidable task. But from the caliber of people and products you nominated, it's clear that there's no lack of creative and talented people and innovative products in the electronics industry.

If you or your company didn't participate in this year's innovation-awards program, we encourage you to take part next year. It's not too early to start thinking about products and people you could nominate. We will be pleased to mail you 1991 nomination packets as soon as they are ready in early 1991. Just Circle No. 801 on the Information Retrieval Service (bingo) card in this issue, and we'll add you to our award mailing list.

INNOVATION

INNOVATORS

Dr Klas Eklund



Power Integrations Inc
Mountain View, CA
(415) 960-3572

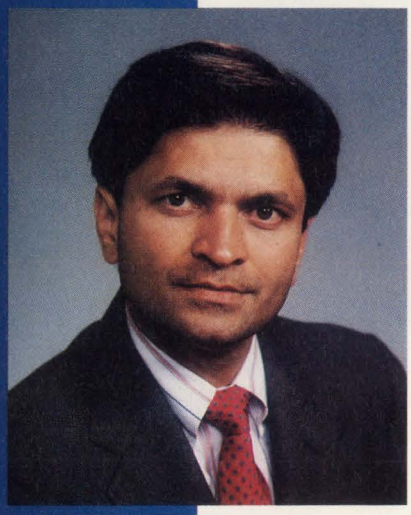
Dr Klas Eklund has developed an unusual technique to implement a power MOSFET using a standard CMOS-logic semiconductor-manufacturing process. This new technology allows designers to add power MOSFETs to the same chip with other analog and digital functions without any penalty in die size. Therefore, the power-circuit technology further enhances the miniaturization and cost benefits achieved by mixed-signal (analog/digital) semicustom-IC technology.

Last spring the company Eklund founded, Power Integrations, introduced the first significant product that uses his patented technology—the PWR SMP-3. This IC includes a fully integrated preregulator, bandgap reference, error amplifier, digital PWM circuit, a variety of protection circuits, and a 400V power MOSFET on a single die. The PWR SMP-3 features breakdown voltages of 400V or higher. Standard 5V CMOS logic signals can turn the power MOSFET on and off, and low internal capacitance yields fast switching speeds.

Most other "smart-power-IC" companies have attempted to add logic and analog circuits to ICs that use the power-MOSFET semiconductor process. Eklund's idea of implementing circuits in standard CMOS results in savings in die size and makes the technology available to designers familiar with standard CMOS.

To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballet.

Tushar Gheewala



Crosscheck Technology Inc
San Jose, CA
(408) 432-9200

While working for IBM and Sperry Corp during the 1980s, Tushar Gheewala experienced the explosion in VLSI technology firsthand. Semiconductor test technologies, however, didn't keep pace with the dramatic increases in ASIC gate densities. "I was frustrated as a designer," he says, "because we had the ability to manufacture very aggressive devices, but we couldn't test them." When Sperry merged with Unisys Corp, Gheewala left and founded Crosscheck Technology Inc to develop and market the advanced IC test technology he envisioned.

Gheewala's method begins by embedding test points at the outputs of an ASIC's internal gates. This placement gives an IC tester 100% access to a device's critical nodes. It provides total observability and substantially reduces the burden of generating test vectors. Semiconductor vendors can then use software to generate test vectors. Because ASIC vendors can install the required test structures automatically, design engineers are free to focus on the device's functional capabilities exclusively and leave testability considerations to others. Best of all, Gheewala's testing technique exacts no speed penalty.

To vote for this entrant as the Innovator of the Year, mark the appropriate box on the ballot.

INNOVATION

INNOVATORS

Analog Fastrack Design Team

The Harris Semiconductor Analog Fastrack design team developed a CAE software tool set used in all phases of ASIC design—schematic capture, circuit simulation, layout, design-rule checking, and layout parasitic extraction. The project involved 16 major contributors from four disciplines. Two of these people are researchers—college professors who consulted with the rest of the team. Their pioneering work provided the seeds of the product concept. Two team members are managers at Harris; four specialize in analog-IC design; and eight are specialists in CAE development. Two of the CAE development specialists are Harris alumni who now work for Cadence, the company under whose CAD framework the tool set runs.

The analog-IC designers on the team specified the simulation methodology. Their spec offered direction to two groups of people at Harris: CAE developers and process/device engineers. The characterization methodology and the links to the circuit simulator are key contributions of these members.

The CAE developers performed many tasks, including integration of the tool set with the framework. One of the major tasks was development of a statistical and geometry-dependent modeling technology. Another was development of a tool for automatically synthesizing the hierarchical macromodels used by the simulator. This tool, which behaviorally models common functions such as op amps, allows rapid "what-if" analyses. An IC designer can change a parameter and rerun the simulation or can ask the simulator to sweep parameters over a range of values.

The Analog Fastrack design team: T. Coston; N. English; A. Sangiovanni-Vincentelli; A. Strojwas; C. Garcia; P. Landy; R. Webb; R. Cooper; M. Chian; K. Eshbaugh; S. Majors; G. Porter; S. Rader; R. Singleton; P. Hernandez; J. Spoto.

To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

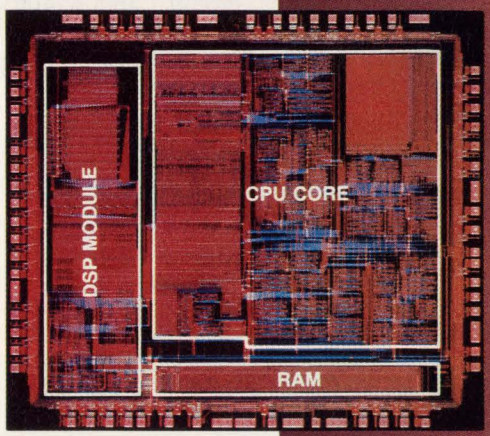
Harris Semiconductor
Melbourne, FL
(407) 724-3739

INTEGRATED CIRCUITS AND SEMICONDUCTORS

NS32FX16 μP

The NS32FX16 μP—a member of the manufacturer's 32-bit Series 32000 processor family—incorporates a digital-signal-processing (DSP) module that performs math operations on vectors of complex numbers. The device integrates both DSP functions and graphics-information-processing operations in a single μP chip. This combination of functions suits the chip for use in modems, facsimile machines, laser printers, graphics terminals, and telephones.

Because software controls all of the device's operations, a manufacturer can adopt one architecture and adapt it to many office-automation and telecommunications tasks. Designers can also use the chip to implement software equivalents of tone-generator and filter circuits into telecommunications equipment. The DSP section shares memory with the core μP functions, so it can quickly exchange filter coefficients and other information with the main processor. Besides handling DSP tasks, the chip also supplies 18 graphics instructions that let it address frame buffers and move blocks of data. Individual program steps can also compress, expand, and magnify image data. Available now, the NS32FX16V in a plastic chip carrier costs $33.78 (100).



To vote for this entry as the Integrated Circuit and Semiconductor Innovative Product of the Year, mark the appropriate box on the ballot.

National
Semiconductor Corp
Santa Clara, CA
(408) 721-5000

INNOVATION

INTEGRATED CIRCUITS AND SEMICONDUCTORS

TMS320C50 DSP μP

The TMS320C50 digital-signal-processing (DSP) μP has a 4-line Joint Test Action Group (JTAG) serial interface that lets you test internal chip operations. The JTAG interface gives you access to all of the device's internal bits and registers, thus you can use the chip to emulate itself. The JTAG port lets you control single-step, trace, and breakpoint operations through a dedicated on-chip register without intruding upon or altering the chip's internal operations. You can set breakpoints in both hardware and software. The manufacturer supports development tools that operate through the chip's JTAG port. These tools include a high-level-language debugger and an IBM PC-compatible add-in board that incorporates the JTAG control circuitry.

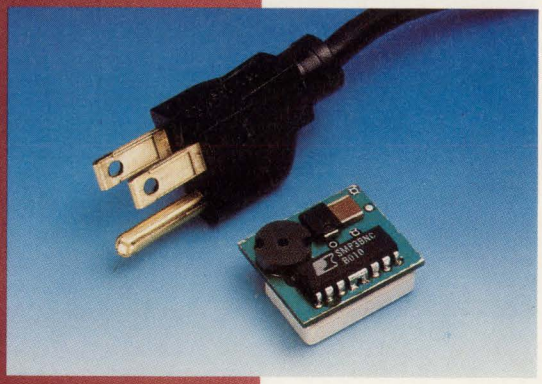
The DSP chip contains a fixed-point CPU that executes instructions as fast as 35 nsec. To allow for fast context switches, the chip's architecture includes a backup storage register for each of 11 internal registers. An internal stack lets the CPU hold eight levels of subroutines. The device also supplies a parallel logic unit that lets software set, clear, test, or toggle multiple bits in registers or memory locations. On-chip memory includes 9k words of program RAM, 1k word of data RAM, and a 2k-word boot-up ROM. The chip comes in a quad flatpack and is available from stock. In OEM quantities, the TMS320C50 costs $75 to $150.

To vote for this entry as the Integrated Circuit and Semiconductor Innovative Product of the Year, mark the appropriate box on the ballot.

Texas Instruments Inc
Dallas, TX
(800) 232-3200

PWR SMP-3 Switching-Power-Supply IC

The PWR SMP-3 switching-power-supply IC combines an off-line preregulator, a 1-MHz PWM control circuit, and a 400V power MOSFET switch in a single monolithic device. The novel combination of these analog, digital, and power functions lets you build a small 3W power supply with only a handful of accompanying passive components. Because the IC's switching speed is much higher than that of other supplies, the accompanying electronics can be small in size. The device has built-in overvoltage, undervoltage, thermal-shutdown, and current-limiting protection. The preregulator connects directly to the rectified 110V ac line and supplies initial power to the chip. The PWM circuit determines the duty cycle that the device should apply to its 400V power MOSFET switch to maintain a consistent output voltage.

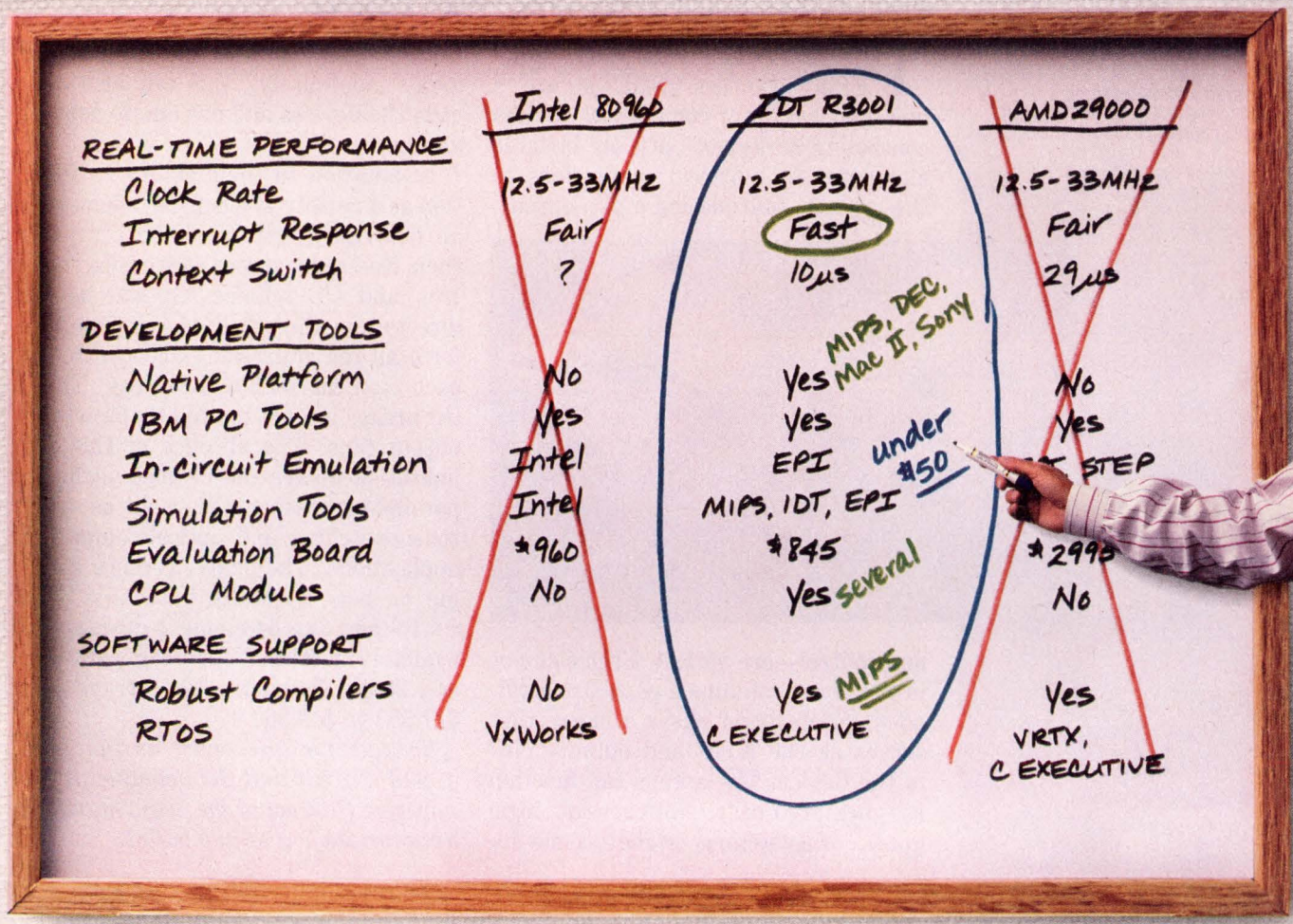


You can use the device to produce power supplies in a variety of circuit topologies, but it especially suits flyback power-supply topologies. The device's small size and small accompanying parts count make it suitable for bias or housekeeping supplies for larger power supplies, consumer products, and medical instruments. The piece price of the 16-pin plastic DIP varies from $3 to $6, depending on volume.

To vote for this entry as the Integrated Circuit and Semiconductor Innovative Product of the Year, mark the appropriate box on the ballot.

Power Integrations Inc
Mountain View, CA
(415) 960-3572

Embedded RISC

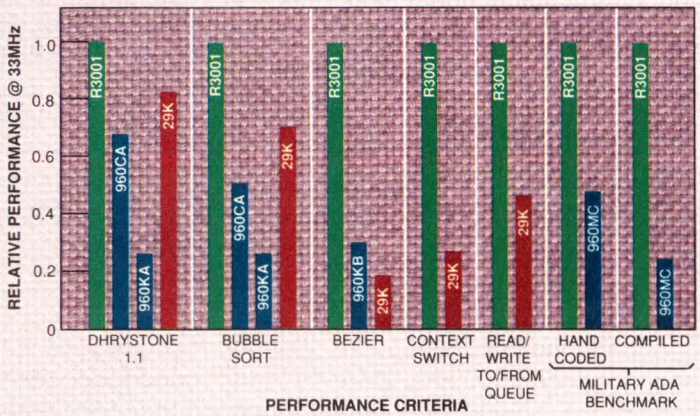


Get the Facts

When evaluating RISC processors for embedded applications, you need real benchmark data from independent sources. The *R3001 Performance Comparison Report* is a collection of the original third-party data used in the graph below.

Benchmark Your Code

Of course, we know that published data can't give you all the information. You'd prefer to perform benchmarks for your specific application, and our six technology centers are equipped to do just that—bring us your code and we'll run your benchmarks!



Sources: *Electronic Engineering* Magazine, *High-Performance Systems* Magazine, *Microprocessor Forum* Conference Fall 1989, *Independent Assessment Benchmark Report* Atlantic Research Corporation

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IDT offers a full array of complementary high-performance system building blocks for all your applications. Contact us today and get the facts: an R3001 Data Pak and R3001 Performance Comparison Report.

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When cost-effective performance counts

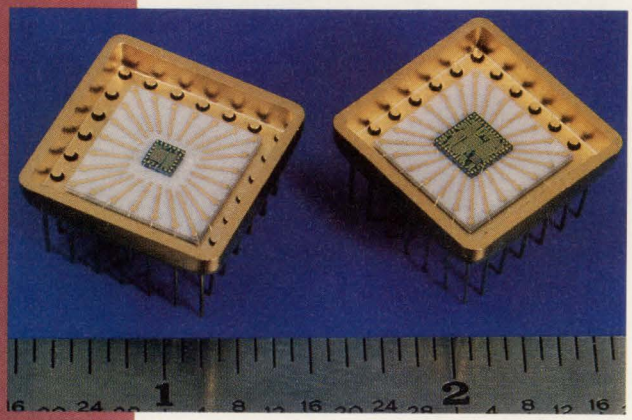
Integrated Device Technology

INNOVATION

INTEGRATED CIRCUITS AND SEMICONDUCTORS

4000-Series Self-Electro-optic-Effect Devices

The 4000-Series Self-Electro-optic-Effect Devices (SEEDs) are a new generation of commercial devices containing arrays of optically bistable elements. All physical connections to the arrays—information input, output, and control—are optical. Each element in the array contains a pair of photodiodes. Each diode has a window that serves as the input and output "pin" of the device. The arrays can function as memory cells, differential logic gates, or switching latches; a low-intensity beam can hold the state of the array indefinitely. You can also cascade the devices and use one to control another.



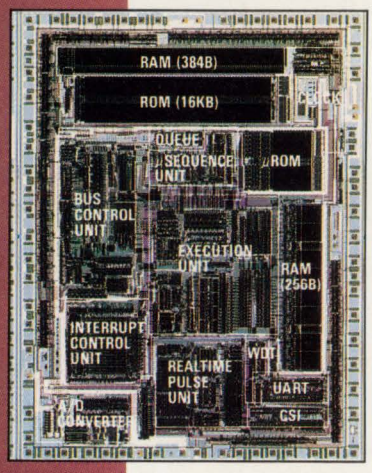
In addition to their ability to function as a variety of electronic elements, an innovative feature of the arrays is their free-space optics addressing, control, and I/O scheme. Optical beams directed on the top of the arrays perform all the addressing and control of each element within the array. Thus, the arrays are not limited by input and output pins. The absence of this I/O limitation makes the devices useful in parallel-processing, as well as photonic-switching and optical-computing applications. The arrays require a single dc bias, typically 5 to 15V. The 8×16- and 32×64-element devices are available in 24-pin open-can packages and 28-pin flatpacks. The arrays cost $17,550 to $19,950.

To vote for this entry as the Integrated Circuit and Semiconductor Innovative Product of the Year, mark the appropriate box on the ballot.

AT&T Bell Laboratories
Breinigsville, PA
(215) 391-2510

K Series Microcomputers

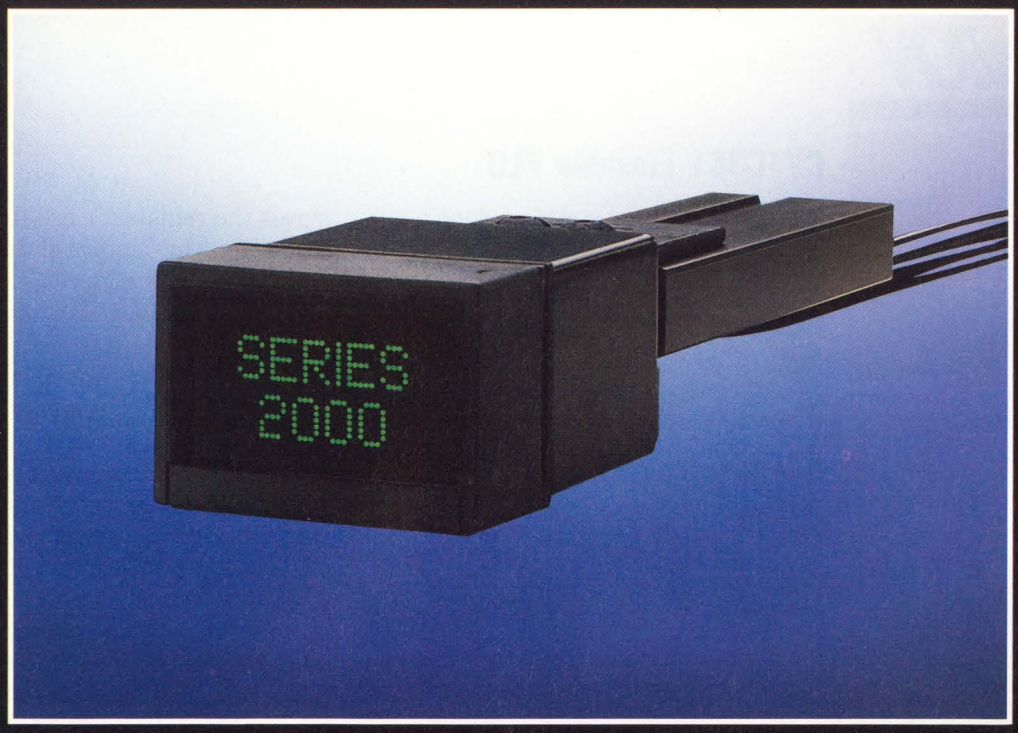
The interrupt-control unit of the K Series of 8- and 16-bit microcomputers has a dedicated hardware section called the peripheral management unit (PMU). While off-loading interrupt servicing from the CPU, the PMU can manipulate data that would otherwise be the responsibility of the CPU. These data manipulations can be control oriented or computational. The PMU performs the manipulations via registers that are mapped to each of the peripherals. The PMU can also handle housekeeping functions, such as incrementing pointers.



Because the manipulations do not depend on the CPU, the PMU sidesteps much of the overhead of vectored interrupt processing. During vectored interrupt processing, the CPU must Stop, Push its present status onto the stack, Branch to an interrupt service routine, perform the routine, Pop the previous status from the stack, and continue processing. If you use the PMU, you only need to specify the total number of data transfers, which peripherals are involved in the transfer, and the mode of transfer. K Series microcomputers cost $5 to $10.

To vote for this entry as the Integrated Circuit and Semiconductor Innovative Product of the Year, mark the appropriate box on the ballot.

NEC Electronics Inc
Mountain View, CA
(415) 965-6048



The program in a switch.

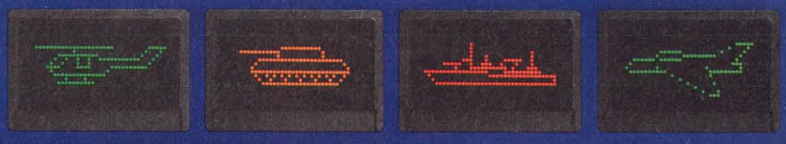
Introducing Vivisun Series 2000, the programmable display pushbutton system that interfaces the operator with the host computer. The user friendly LED dot-matrix displays can display any graphics or alpha-numerics and are available in green, red or amber. They can efficiently guide the operator through any complex sequence, such as a checklist, with no errors and no wasted time.

They also simplify operator training as well as control panel design. Four Vivisun Series 2000 switches can replace 50 or more dedicated switches and the wiring that goes with them. In short, Vivisun Series 2000 gives you more control over everything including your costs.

Contact us today.

AEROSPACE OPTICS INC.
3201 Sandy Lane, Fort Worth, Texas 76112
(817) 451-1141 · Telex 75-8461 · Fax (817) 654-3405

SERIES
VIVISUN 2000™



Programmable display switches. Making the complex simple.

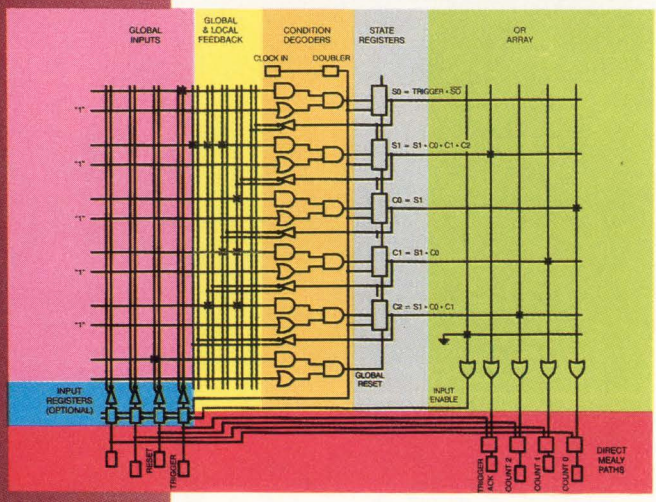
CIRCLE NO. 99

INNOVATION

INTEGRATED CIRCUITS AND SEMICONDUCTORS

CY7C361 Erasable PLD

Optimized for state-machine applications at clock rates as fast as 125 MHz, the CY7C361 CMOS erasable PLD features an architecture in



which the state registers are between the input condition array and the output translation array. This placement moves the registers close to the inputs, minimizes the length of the feedback path, and thus reduces the feedback delay from the register output relative to the clock-to-output delay. The PLD also features an output skew of only 3 nsec and an input-register metastability MTBF of 10 years.

The device interconnects its 32 state-machine macrocells in a shift-register arrangement that can use token-passing logic to directly exchange information between registers. This arrangement lets the device represent multiple concurrent states. You can configure the device's input macrocells for 0, 1, or 2 registers. Available now, the CY7C361 costs $27.10 (100).

To vote for this entry as the Integrated Circuit and Semiconductor Innovative Product of the Year, mark the appropriate box on the ballot.

Cypress Semiconductor
San Jose, CA
(408) 943-2653

TEST AND MEASUREMENT

Codetap 386 Run-Time Debugging Tool

The Codetap 386 is a run-time debugging tool for software engineers who are developing embedded

386 applications. The instrument combines some of the functions of a ROM-based software debugger and an in-circuit emulator. Unlike a ROM-based software debugger, the instrument allows the program under test to run in real time and does not usurp any target-system memory. Its cost, however, is less than one-quarter of that of a full-fledged in-circuit emulator. The tool lacks the complex breakpoints and trace memory of an in-circuit emulator.

Codetap comes with a linker and a source-level software debugger. Its probe, containing a modified 386 μP and registers, replaces the 386 in your target system. The tool's control software, running on an IBM PC, has access to both your target system's hardware and the structure of your program. Consequently, the tool can set simple breakpoints and give you source-level access to structures, arrays, and variables—including dynamic variables. The Codetap 386 starts at $5000.

To vote for this entry as Test and Measurement Product of the Year, mark the appropriate box on the ballot.

Applied Microsystems
Redmond, WA
(206) 882-9702

The FS700 LORAN-C frequency standard

10 MHz cesium stability

$4950

Cesium long term stability at a fraction of the cost

Better long-term stability than rubidium

Not dependent on ionosphere position changes, unlike WWV

Complete northern hemisphere coverage, unlike GPS.

The FS700 LORAN-C frequency standard provides the optimum, cost-effective solution for frequency management and calibration applications. Four 10 MHz outputs from built-in distribution amplifiers provide cesium standard long-term stability of 10^{-12}, with short-term stability of 10^{-10} (10^{-11} optional). Reception is guaranteed in North America, Europe and Asia.

Since the FS700 receives the ground wave from the LORAN transmitter, reception is unaffected by atmospheric changes, with no possibility of missing cycles, a common occurrence with WWV due to discontinuous changes in the position of the ionosphere layer. Cesium and rubidium standards, in addition to being expensive initially, require periodic refurbishment, another costly item.

The FS700 system includes a remote active 8-foot whip antenna, capable of driving up to 1000 feet of cable. The receiver contains six adjustable notch filters and a frequency output which may be set from 0.01 Hz to 10 MHz in a 1-2-5 sequence. A Phase detector is used to measure the phase shift between this output and another front panel input, allowing quick calibration of other timebases. An analog output with a range of ±360 degrees, provides a voltage proportional to this phase difference for driving strip chart recorders, thus permitting continuous monitoring of long-term frequency stability or phase locking of other sources.

FS700: The optimum frequency management system

SRS

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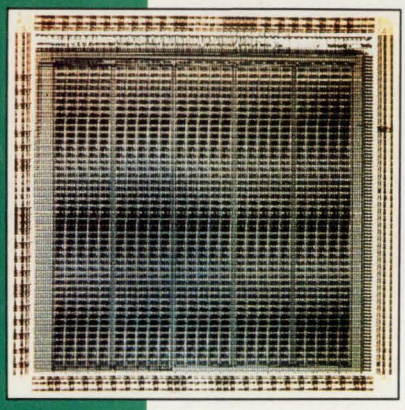
INNOVATION

TEST AND MEASUREMENT

Crosscheck Test Technology

Crosscheck renders ASICs and other VLSI devices testable by embedding a test structure into the devices' silicon substrate. The technique adds test points to the IC and allows you to access the test points over a serial bus. ASIC designers do not have to concern themselves with designing in the test structure; device fabricators can add it automatically. The product also includes control and diagnostic software.



The resulting silicon structure compares to a conventional bed-of-nails test fixture for pc boards. With one test point per gate, an IC becomes inherently testable because of its 100% observability. The test points are actually small FETs. The embedded test points measure logic levels at every gate and collect the data in an internal serial register. You can either compress those data into a signature for go/no-go testing or read them out directly to see precisely the output of any gate at any time.

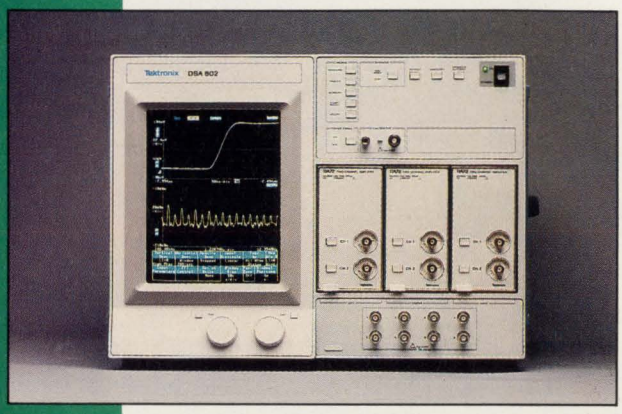
Prices for Crosscheck devices will be set by ASIC vendors; users are expected to pay a 25 to 40% premium for an ASIC that includes Crosscheck.

To vote for this entry as Test and Measurement Innovative Product of the Year, mark the appropriate box on the ballot.

Crosscheck Technology Inc
San Jose, CA
(408) 432-9200

DSA 602 Digitizing Signal Analyzer

The DSA 602 digitizing signal analyzer has two functions. It captures and displays high-speed signals at real-time sample rates as high as 2 gigasamples per second with 8-bit resolution, and it uses its dedicated digital-signal processor to analyze the acquired data in real time. It combines features of spectrum analyzers, network analyzers, logic analyzers, and digital storage oscilloscopes. The instrument's front end has four custom hybrids for acquisition. Each hybrid contains a track-and-hold circuit and an 8-bit, 500-megasamples-per-second flash A/D converter.



A proprietary digital-signal processor analyzes the captured data and formats them for screen display. Consequently, you can simultaneously view both the time-domain and frequency-domain waveforms—with each waveform appearing live. The instrument also features Boolean-event triggering and conventional analog triggering. The DSA 602 costs $35,000.

To vote for this entry as Test and Measurement Innovative Product of the Year, mark the appropriate box on the ballot.

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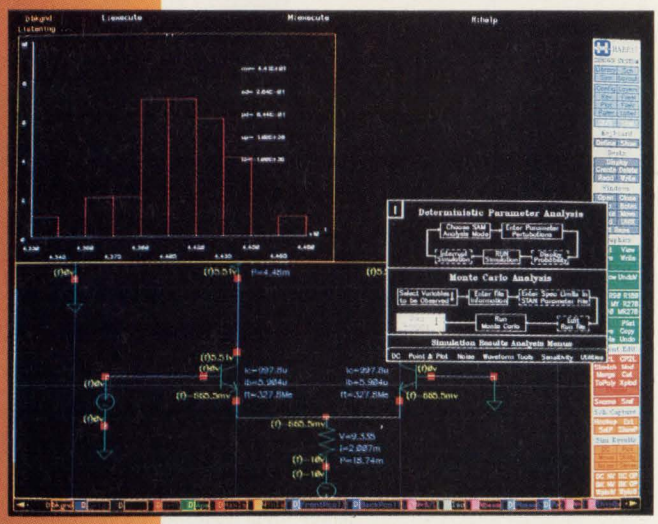
INNOVATION

CAE/CAD

Analog Fastrack Design System

The Analog Fastrack design system contains CAE tools that cover the spectrum of IC design. Tools within the system perform schematic capture; circuit simulation; layout; design, electrical, and consistency checking; layout parasitic extraction; and packaging.



Within the Analog Fastrack, a statistical and analysis modeling (SAM) tool uses a correlated model parameter database. The database uses a knowledge of how process variations simultaneously affect several device parameters to prevent the simulation from choosing more worst-case values than can occur in a real process at one time.

The ASIC vendor provides means, variances, and correlation coefficients for the model parameters. Next, a correlated Gaussian-random-number generator allows the software to calculate model parameters for successive passes through a Monte Carlo simulation loop. The SAM converts the device model parameters to a Gaussian-distribution format for internal processing. In the Monte Carlo simulation, Gaussian distribution assures that the simulated process parameters are distributed about their mean values in the same way the parameters of a real process would be. The statistical distribution of the circuit responses provides a more realistic metric of the manufacturing yield than you can expect from the circuit. The Analog Fastrack software costs $140,000.

To vote for this entry as the CAE/CAD Innovative Product of the Year, mark the appropriate box on the ballot.

Harris Semiconductor
Melbourne, FL
(407)724-3739

TMS34010 Simuboard

To reach simulation nirvana—complete system-level simulation—you need to model every element of your system. Subsystem-level simulation remains stalled for lack of enough accurate device-level simulation models. The TMS34010 Simuboard is a software model of a PC add-in graphics board that can also serve as an on-line application note.

The Simuboard includes schematics, parts models, a design database, stimuli, support software, a compiler, and tutorials. The model allows users to interactively learn about the board's devices, CAE tools, and modeling in general.

Using workstation-based CAE tools (currently only those from Mentor Graphics), you can design, verify, and tweak a circuit using existing software models. Other features of the Simuboard include the creation of JEDEC PAL files, image files to initialize memories, processor-control-language programs that support the models, and test stimuli that support your simulation examples. The 34010-based board-model package costs $1490.

To vote for this entry as the CAE/CAD Innovative Product of the Year, mark the appropriate box on the ballot.

Texas Instruments Inc
Dallas, TX
(214) 997-2796

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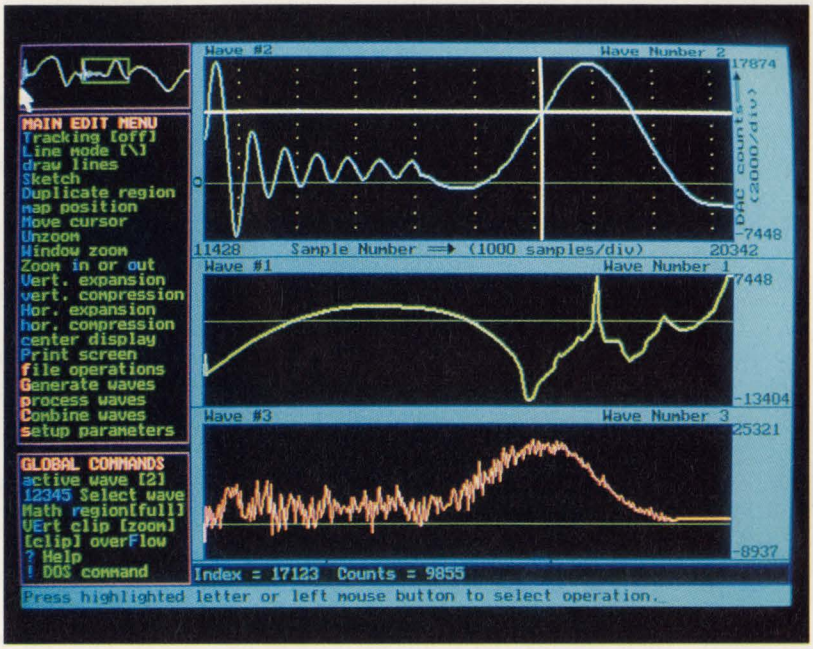
Introducing the R4 Arbitrary Waveform Generation/Editing software, at only $995.



With R4, any waveform you can imagine can be created, edited and displayed on the PC, and then instantly downloaded to your ARB. You can sketch with a mouse, enter any equation, or capture real world waveforms. Five, 32k waveforms, with up to 20 bits of resolution, can be displayed at once. You can create and edit complex, sophisticated waveforms with no programming, no data entry, and no frustrating front panel buttons.

With R4 you can create any waveform you can imagine.

Let's say you've just started with R4.

In 10-15 minutes you'll be creating waveforms. It's that easy. Everything is intuitive and obvious.

You might begin by sketching a waveform (everything is mouse driven and instantaneous). Or use one of the line drawing modes. Or enter any equation into the equation editor for an instant waveform. Or capture real world waveforms from a DSO.

Then you might want to edit. Maybe add, subtract, multiply, divide or convolve your created waveforms (up to five, 32K long waveforms on the screen at once). Maybe zoom into the waveform, down to the individual data point (to 20 bits of resolution), and manipulate: duplicate sections, invert, limit (clip), smooth with a moving average, compress or expand in either dimension. That's a small start on what is possible with R4.

So far you've invested maybe 15 minutes. And you're downloading complex, sophisticated waveforms.

Try and do that with any other software.

Now, let's add up what you did not have to do. No programming. No front panel pushbuttons or silly rubberbanding that never really gives you what you want. No long data entry or impossible ASCII file edits. Most importantly, you did not have to invest long, frustrating, irritating and nonproductive hours.

Instead, R4 is as straightforward as a video game. As quickly as a waveform comes to mind, you can create it on the screen.

And we guarantee support for your ARB.

We make you this promise: when you purchase R4, you are guaranteed a driver.

For many users, the R4 driver library will include your ARB across GPIB. But if it doesn't, we will deliver a driver for your ARB within 20 working days of receipt of your order.

Call for an R4 demo disk today: (206) 547-8311

Isn't it time you discovered the reason to own an ARB?

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RAPID SYSTEMS

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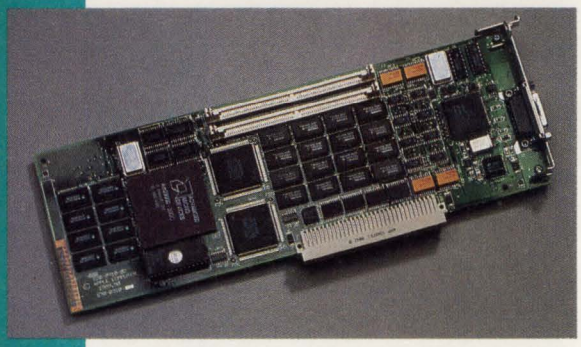
INNOVATION

COMPUTERS AND PERIPHERALS

Macintosh Display Card 824 GC

The Macintosh Display Card 824 GC graphics coprocessor and display card occupies one Nubus expansion slot in a Macintosh II computer. The card uses a 30-MHz Am29000 RISC μP to run an optimized version of the company's Quickdraw software. The RISC CPU and the host's 600X0 μP work together to accelerate Quickdraw programs from 5 to 30 times normal speed, depending on the application. The host CPU dispatches a Quickdraw call over the Nubus to the card and resumes other activities while the Am29000 processes the command. In most instances, the RISC CPU finishes a task before receiving another call from the host. In rare instances when the host issues a call while the card is busy, the card issues a wait signal to the host.



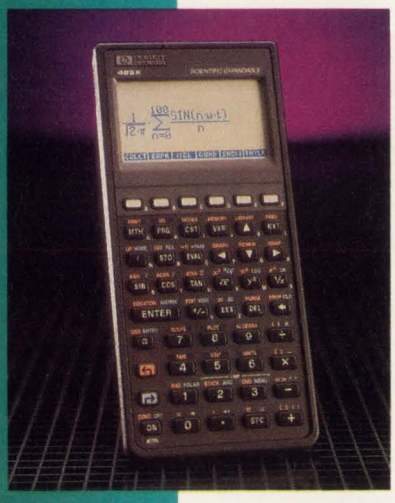
The card can drive all of the company's monitors and has auto configuration circuitry to determine which monitor is present. Representative monitors include 256-level gray-scale models and 24-bit color models, such as the Applecolor high-resolution RGB monitor, which can simultaneously display 16.7-million colors. The card also has an RS-170-compatible output signal for driving interlaced-video devices, such as VCRs and televisions. The interlaced-video output uses Apple Convolution software to evaluate adjacent lines and pixels and then adjust the image on the screen to provide smooth continuous images. The card costs $1990.

To vote for this entry as the Computer and Peripheral Innovative Product of the Year, mark the appropriate box on the ballot.

Apple Computer Inc
Cupertino, CA
(408) 996-1010

HP 48SX Scientific Calculator

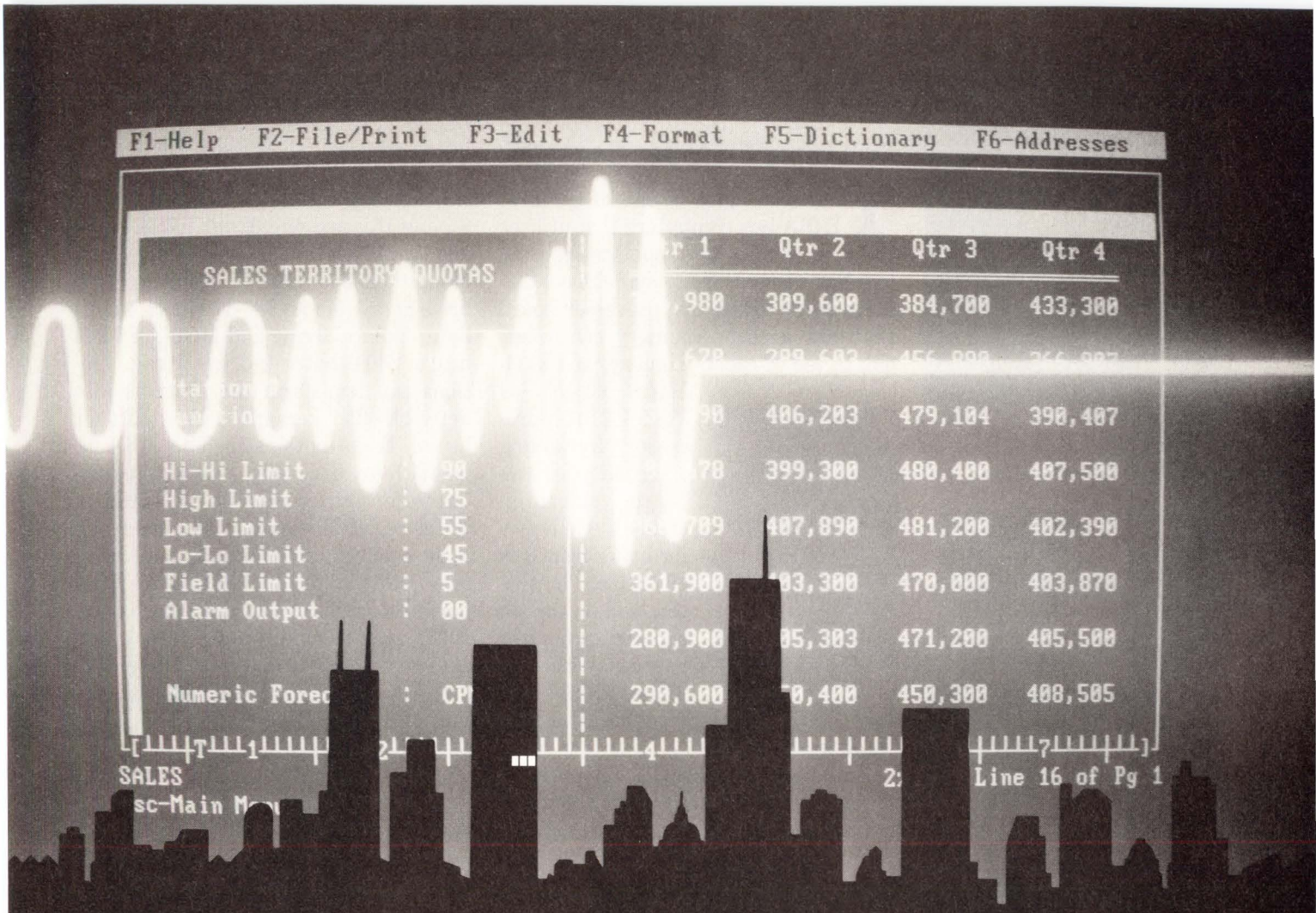
The HP 48SX scientific calculator has functions not found on any other scientific calculator. You access the calculator's 2100 functions with menus and soft keys. You draw and edit your equations in standard mathematical form on the 8-line × 26-character graphics LCD. You can enter equations in algebraic or reverse-Polish notation. Once you are satisfied with the equation, press the enter button to translate the equation into the calculator's format and push it onto the stack. You can attach units to any variable, and the calculator will perform conversions and flag illegal operations. The calculator can automatically simplify, differentiate, and integrate many functions. It can also graph functions in many formats.



The calculator has a conventional 1-piece case and two slots for ROM and RAM expansion cards. You can couple the calculator to an IBM or Apple Macintosh personal computer using a serial RS-232C adapter to transform the calculator into a math package. Bidirectional infrared ports let two calculators separated by a few inches communicate with each other. The $350 unit uses three AAA batteries. The serial adapter costs $99.95, the math-pack ROM card costs $99.95, the 32k-byte battery-backed RAM card costs $79.95, 128k-byte RAM card costs $250, and the infrared coupled printer costs $135.

To vote for this entry as the Computer and Peripheral Innovative Product of the Year, mark the appropriate box on the ballot.

Hewlett-Packard
Corvalis, OR
Phone local office



SOLA SIDEKICK.™

IT'LL KICK YOUR POWER PROBLEMS ASIDE.

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That's why there's Sola Sidekick,™ the economical UPS that'll make light of even the most serious blackout. The Sola Sidekick features an advanced microprocessor-based design that keeps your sensitive electronic equipment fully functional through all types of power line surges and sags. That means no loss of valuable data, and no damage to your system's components.

What's more, if a power failure continues for an unusually long period of time, this exceptionally versatile unit even has the wherewithal to alert you to shut down your electronic equipment.

UL listed and CSA Certified, the Sola Sidekick is not only easy to use, but is also easy to look at. It compliments any office decor, yet takes up very little space.

Sola Sidekick is only one of a full-line of power protection products made by Sola. And every product is designed with this single purpose in mind: If your equipment depends on power, you can depend on Sola. Try the Sola Sidekick. You'll discover that you have absolutely nothing to lose... especially your important data.

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CIRCLE NO. 105

INNOVATION

COMPUTERS AND PERIPHERALS

Systempro EISA Bus Computer

The Systempro is one of the first EISA bus computers that utilizes the bus's ability to support more than one bus master. Each model has a 33-MHz 80386 EISA bus processor board that has a cache memory controller, 64k bytes of cache memory, and a 33-MHz 80387 or Weitek 3167 coprocessor. By adding a second processor board, you can increase system performance from 8 to 16 MIPS. The system will be able to support processor boards with 33-MHz 80486 μPs that deliver 20 MIPS when they become available.

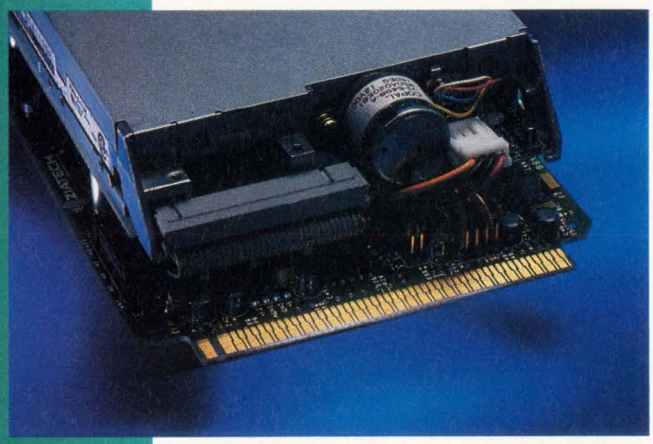
Standard models have 4M bytes of 32-bit system memory, which you can expand to 256M bytes; a 5¼-in. 1.2M-byte floppy-disk drive; a 32-bit intelligent drive-array controller; eight full-size expansion slots, which include six 8-, one 16-, and one 32-bit EISA slots; and two 32-bit processor/memory slots. Model 386-840 has a 840M-byte, 4-drive array; Model 386-420 has a 420M-byte, 2-drive array; and Model 386-240 has a 240M-byte, 2-drive array. Options can transform the systems into network file servers and multiuser hosts. These options include a 3½-in. 1.44M-byte disk drive, tape-cartridge drives for cartridges with capacities of 150M to 525M bytes, a 240-baud modem, color graphics boards and monitors, and 120M- to 650M-byte fixed hard-disk drives. The systems have a 300W power supply and keylock and password security features. Model 386-240 costs $15,999; Model 386-420 costs $19,999; and Model 386-840 costs $25,999.

To vote for this entry as the Computer and Peripheral Innovative Product of the Year, mark the appropriate box on the ballot.

Compaq Computer Corp
Houston, TX
(713) 370-0670

STD 32 Bus Specification

The STD 32 Bus specification is the electrical, mechanical, and functional description for 32-bit data transactions over the STD Bus. It is a superset of the STD-80 Series specification and maintains that spec's physical form factor and pinouts. The additional pins required for 32-bit data transactions are on 0.065-in. centers between existing STD-80 pins, and the number of card-edge pads increases from 56 to 114 pins. The STD 32 Bus spec lets existing 8-bit products work alongside 16- and 32-bit products in either an 8-bit backplane or the STD 32 backplane.

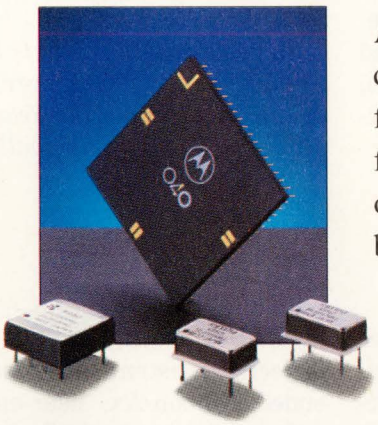


The specification adds several features to the STD Bus including 32-bit addressing, 16- or 32-bit data transfers, multimaster capability with bus arbitration, backplane DMA, slot-specific interrupts, an 8-MHz backplane clock, and software-configurable peripheral boards. These added features give STD Bus users a growth path without endangering their investment in peripheral boards, such as I/O and memory cards. Because the STD 32 Bus spec is similar to EISA, designers can use ISA or EISA chip sets to make STD 32 products compatible with IBM PCs.

To vote for this entry as the Computer and Peripheral Innovative Product of the Year, mark the appropriate box on the ballot.

Ziatech Corp
San Luis Obispo, CA
(805) 541-0488

Our 680's TICK makes Motorola's 040 TOCK.



AVX/Kyocera's 680 clock oscillator is specifically designed to meet all of Motorola's strict timing requirements for their MC68040: the tight symmetry (47.5%/52.5%) for delivering 20MIPs at 25MHz, the dual outputs* of 50MHz and 25MHz to eliminate external adjustments, buffers and dividers. These plus controlled skew to ± 7.0 nsec between clocks and the ability to tolerate supply voltage variations up to ± 10% keeps Motorola's 040 right on time.

Uncompromising precision, that's what makes AVX/Kyocera clock oscillators "tick."

To talk about our 680, contact AVX/Kyocera today by calling (803) 448-9411, fax us at (803) 448-1943, or write to AVX/Kyocera, 17th Avenue South, P.O. 867, Myrtle Beach, SC 29577.

* Also available in single 50MHz frequency, K680S.

☐ Please send me more information on what makes the 680 tick.

NAME _____

TITLE _____

COMPANY _____

ADDRESS _____

CITY _____ STATE ____ ZIP _____

TELEPHONE _____

Send to: AVX/Kyocera, Literature Department, P.O. 867, Myrtle Beach, SC 29577.

EDN090390

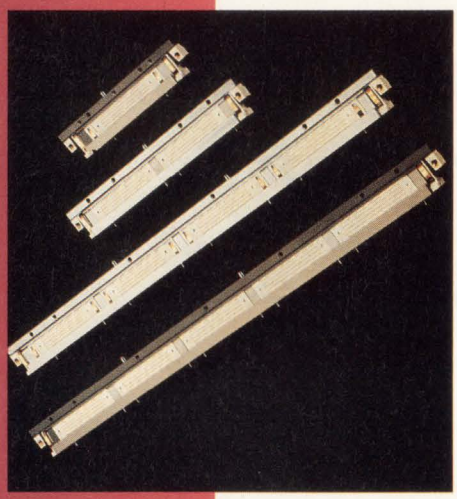
AVX KYOCERA

CIRCLE NO. 106

INNOVATION

COMPONENTS, HARDWARE, AND INTERCONNECTS

EII Connectors



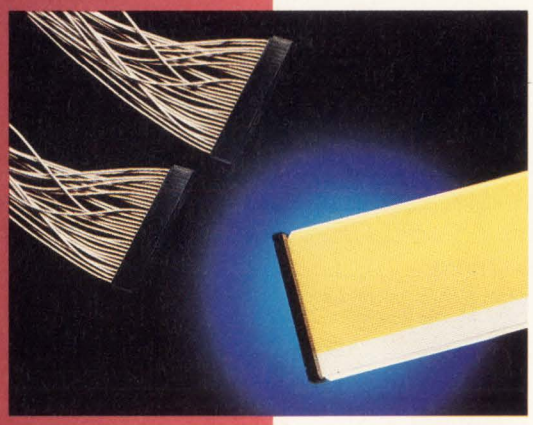
EII connectors feature a high-density array of controlled impedance signal lines and power lines in a modular assembly that can handle signals with rise times as fast as 35 psec. The connectors route signals from a mother board to a daughter board through a flexible circuit, which has a 50Ω characteristic impedance. The flexible circuit also includes a ground plane, which reduces crosstalk to −40 dB for 500-mV, 100-MHz signals with a 900 psec rise time. For each signal line, propagation delay, attenuation, and signal skew are 30 psec (±10%), <−0.025 dB, and <10 psec, respectively.

EII connectors are made up of 2-in.-long, 160-position modules, which you can stack to create larger connectors. Standard connectors can accommodate as many as six modules for a total of 960 signal lines. Standard connectors also accommodate power and ground modules, each of which can handle 10A at 5V. A protective locking and aligning cover on the daughter board properly positions the two boards' main connectors. The card-mating process wipes the daughter board contacts across spring-loaded contacts in the mother board connector to ensure low-resistance interconnects. Contacts are available with either gold or tin-lead plating. EII connectors are guaranteed for a minimum of 100 mate/unmate cycles. They cost $0.30 to $0.40/signal (1000).

To vote for this entry as the Innovative Component, Hardware, and Interconnect Product of the Year, mark the appropriate box on the ballot.

Augat Inc, Interconnection Products Group
Attleboro, MA
(508) 222-2202

Ribbon-Ax Cable



Ribbon-Ax ribbon cable eliminates the high costs involved in terminating coaxial cables without sacrificing signal fidelity. Ribbon-Ax can replace as many as 60 conventional coaxial cables, will transmit both analog and digital signals with minimal crosstalk, and is readily terminated using standard 0.050-in. pitch insulation displacement connectors. Ribbon-Ax is available with impedances of 50, 75, or 95Ω. The 50Ω cable has a capacitance of 24.3 pF/ft, a 70% propagation velocity, a time delay of 1.45 nsec/ft, and a 2.03 effective dielectric constant. In 10 feet of single-ended Ribbon-Ax, near-end and far-end crosstalk is typically less than 1% for signals with 5-nsec rise times and can be as low as 2% for rise times of 1.5 nsec.

Ribbon-Ax cable has an integrated outer copper shield and selectable ground/drain wires. The integrated shield, which can be connected to one or more of the ground wires, protects the signals from outside interference, controls impedance, and provides increased line-to-line isolation. Ribbon-Ax is available with as many as 64 #30 or #28 AWG conductors. The cable costs $0.30 to $0.80 per conductor foot.

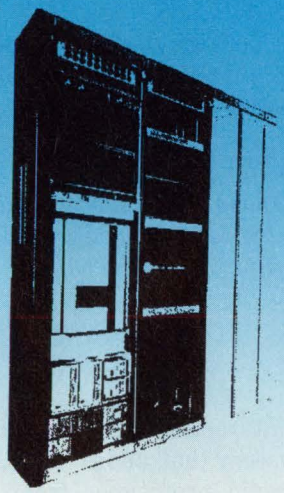
To vote for this entry as the Innovative Component, Hardware, and Interconnect Product of the Year, mark the appropriate box on the ballot.

W L Gore & Associates
Phoenix, AZ
(602) 431-0077

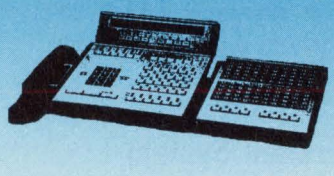
TELECOM DC/DC CONVERTERS

VICOR PROVIDES THE POWER FOR TELECOM APPLICATIONS

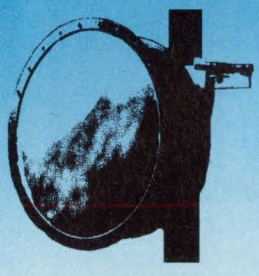
Central Office



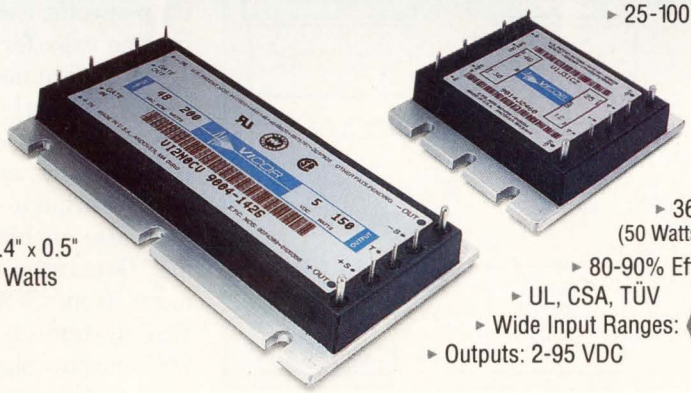
Customer Premises Equipment



Remote Cell Site



VI-J00
- 2.28" x 2.4" x 0.5"
- 25-100 Watts



VI-200
- 4.6" x 2.4" x 0.5"
- 50-200 Watts

Family features
- 36 Watts/in³ (50 Watts/in³–SlimMod™ option)
- 80-90% Efficiency
- UL, CSA, TÜV
- Wide Input Ranges: 36 to 76 VDC, 21 to 56 VDC, 18 to 36 VDC
- Outputs: 2-95 VDC

From remote sites in Alaska and desert sites in Egypt to central offices in Oklahoma, agency approved Vicor converters have consistently demonstrated the ability to meet rigorous demands (Bellcore or British telecom) at competitive prices.

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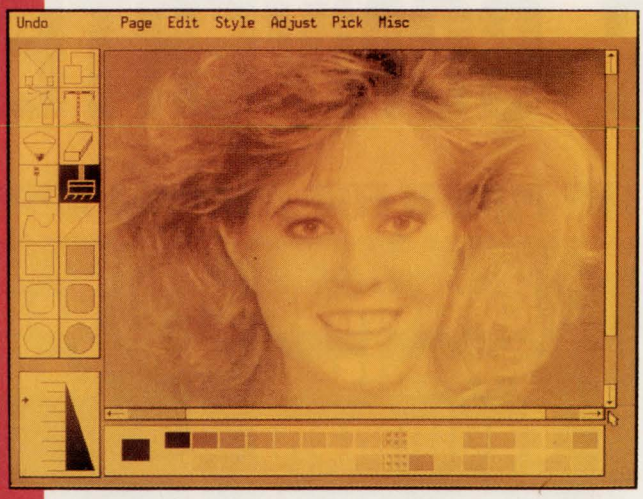
INNOVATION

COMPONENTS, HARDWARE, AND INTERCONNECTS

EL1C-C000 VGA Display



Because the EL1C-C000 direct-current, electroluminescent VGA display is less than 2 in. thick, it provides an attractive alternative to CRTs. Proprietary drive electronics furnish a fast 170-Hz refresh rate and a high 25-fL brightness without any heat buildup.

The display has a true 16-level gray scale and a 1:1 aspect ratio, which complies with DIN character contrast specifications. The amber display has a 160° viewing angle and shows no diminution of light output during the first 20,000 hours of use. Power requirements are 12V nominal at 1A typ. The display's active area measures 8.64×6.48 in. (640 columns by 480 rows). The overall panel measurements are 11.48×8.44×1.662 in. The EL1C-C000 weighs 34 oz and operates over a 0 to 50°C range at altitudes up to 45,000 ft above sea level.

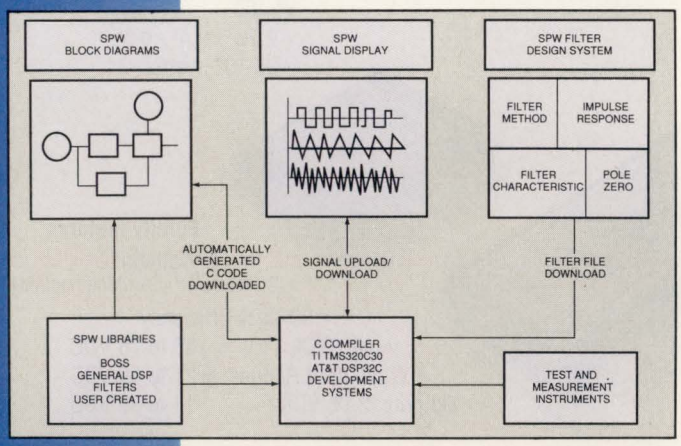
To vote for this entry as the Innovative Component, Hardware, and Interconnect Product of the Year, mark the appropriate box on the ballot.

Cherry Corp
Waukegan, IL
(708) 360-3413

SOFTWARE

Code Generation System

By generating C code for DSP applications from signal-flow block diagrams, the Code Generation System (CGS) frees designers from the intricate details of software development and allows them to concentrate on objectives in digital signal processing. As an option on the manufacturer's Signal Processing Worksystem (SPW), CGS produces generic C code for supercomputer and mainframe CPUs or optimized C for specific DSP chips.



Together, SPW and CGS form a graphical, interactive DSP code-development system that allows designers to create rapid prototypes from system designs. The generic C code produced by CGS can be compiled and run on any processor that has an ANSI C compiler. Chip-specific code contains special subroutine calls for AT&T's DSP32C and Texas Instruments' TMS320C30 processors. Libraries for these chips contain optimized code for implementing FFTs, filters, and other DSP tasks.

In addition to code generation, SPW/CGS also enables DSP prototype testing. Generated code and input signals move from SPW/CGS to the target DSP system via an Ethernet link, and DSP-output signals return to SPW/CGS for analysis. The SPW/CGS development system is available for Sun-3, Sun-4 (SPARC), DECstation, and Hewlett-Packard/Apollo workstations. SPW costs $25,000; the CGS option is $10,000 per DSP target.

To vote for this entry as the Software Innovative Product of the Year, mark the appropriate box on the ballot.

Comdisco Systems Inc
Foster City, CA
(415) 574-5800

Spread Spectrum At Your Finger Tips.

HIGHEST PERFORMANCE VITERBI DECODER
At 20 Mbps with 4-bit soft decision the STEL-2020 is the highest performance K=6 and K=7 Viterbi decoder in the industry.

HIGHEST FLEXIBILITY PN CODER
At 30 Mcps and up to 32 taps per coder the STEL-1032 Triple PN Coder has the flexibility to generate a wide variety of codes for many spread spectrum applications.

HIGHEST PERFORMANCE DIGITAL FILTER
The STEL-3310 64-Tap Complex Matched Filter provides the highest performance in a single package for signal despreading applications.

GPS CODER
The STEL-1023 generates the C/A (Clear/Acquisition) coding and timing for GPS receivers in a single chip.

LOWEST PRICE VITERBI DECODER
At less than $100 (qty. 1000) the STEL-5269 K=7 Viterbi decoder has the most attractive price in the industry, with industry standard polynomials and a 256 Kbps data rate.

HIGHEST SPEED ACCUMULATOR
With a 70 Msamples/sec. accumulation rate the STEL-2410 is the industry's highest speed signal accumulator for spread spectrum applications.

HIGHEST PERFORMANCE BIT SYNCHRONIZER/ DEMODULATOR
The STEL-2110A is a digital bit synchronizer and PSK demodulator, providing high performance in spread spectrum BPSK and QPSK applications.

FASTEST BURST DATA ACQUISITION
The STEL-2210 Block Phase Estimator allows burst signals to be acquired rapidly and demodulated coherently when used in conjunction with the STEL-2110A.

HIGHEST PERFORMANCE QUADRATURE NCO
The STEL-1177 Quadrature NCO has a 60 MHz clock frequency and incorporates linear PM and FM capabilities as well as providing quadrature 12-bit outputs for –75 dBc purity.

SIGNAL QUALITY ESTIMATOR
The STEL-2330 Signal Quality Estimator provides front-end processing to allow the E_b/N_o of signals to be calculated at up to 15 Msamples/sec.

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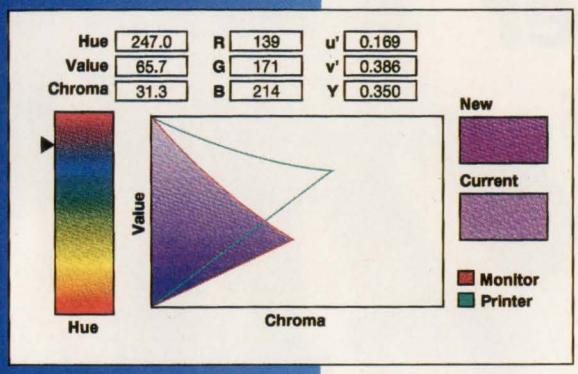
INNOVATION

SOFTWARE

Tekcolor CMS

The Tekcolor Color Management System (CMS) consists of software and development tools that provide precise matching between many different graphics devices, such as color monitors and color printers. The system's color space or specification is essentially device independent. The system's device-characterization mechanisms allow you to accurately represent and duplicate the color gamuts of a variety of peripheral devices. Furthermore, its calibration mechanisms let you measure and mathematically describe the color characteristics of a specific device. And the system's human interface prompts the user for the information needed by its transformation algorithms to match, as closely as possible, the way in which different devices represent the colors of a given image.



Previous methods of color specification were based on existing device signals and did not take into account the perceptual nonlinearities of human vision and the specific characteristics of different devices. The innovative Tekcolor CMS, because it does account for these factors and is essentially device independent, lets you link computer color-graphics systems to such diverse applications as film, fabric design, and paint and dye with a precision that has hitherto not been possible. A Tekcolor general license is free; an implementation manual costs $250.

To vote for this entry as the Software Innovative Product of the Year, mark the appropriate box on the ballot.

Tektronix Inc
Beaverton, OR
(503) 627-7656

OS-9000

The OS-9000 is a modular, real-time, multitasking operating system and software-development environment. Written in C, the system runs on Motorola and Intel CISC (complex-instruction-set computer) and RISC (reduced-instruction-set-computer) μPs. The system includes a ROMable real-time kernel, a hierarchical file manager, a utility function, and a variety of I/O and networking options. It also offers a suite of development tools, including a Unix-like "shell" user interface, editors, compilers, a graphical user interface (GUI), and source-level and system-state debuggers. You can do your development work on the target system or use C cross-development tools, which run on Unix and MS-DOS computers.

The system serves as both a real-time execution environment and as a development environment. As an execution environment, OS-9000 provides a variety of services to application programs including multitasking, interrupt handling, task synchronization, memory management and protection, as well as I/O and networking. You can put all of the system's modules in ROM. And, because the system is modular and scalable, you can build up configurations ranging from a stand-alone kernel to a full-blown development system. A single operating system for an IBM PC costs $995; Motorola μP systems cost $2500. Development tools are extra.

To vote for this entry as the Software Innovative Product of the Year, mark the appropriate box on the ballot.

Microware Systems Corp
Des Moines, IA
(515) 224-1929

Text continued on next page

How To React When Your Customers Send You Mixed Signals.

Big trouble. A customer sends you a mixed signal ASIC design. You simulate it as best you can with your in-house tools. And then cross your fingers. Because guess what happens when your customer plugs it into his system?

That's right. Zippo.

Who's to blame? Who cares? The important thing is you've lost a potentially profitable working relationship.

Here's a way out: Saber, the industry's most popular mixed signal simulator. You provide your customers with accurate Saber behavioral libraries that cover all your ASIC cells' functionality. They can then use Saber to simulate not only the ASIC, but also the entire digital/analog system that surrounds it (even the non-electrical parts).

When they're satisfied, they send you models of the entire system design along with the completed ASIC design. Now you can run a Saber device-level simulation that interacts with the customer's system as a whole.

The result? Fewer failures. Lower customer costs. Increased customer confidence. No more mixed signals – except those on silicon.

For more information on how Saber can help with your mixed signal designs, phone (503) 626-9700, ext. 39, or FAX (503) 643-3361.

Saber environments include: Cadence, Calay, Computervision/Prime, Daisy/Cadnetix, HP, Mentor Graphics, NCR, Racal-Redac/HHB, Schlumberger, Siemens, Teradyne, Valid/ADT and Viewlogic.

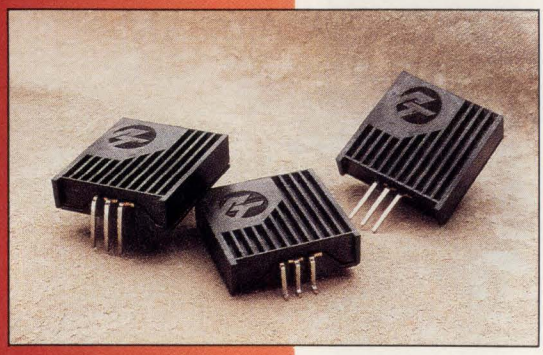
Analogy

INNOVATION

POWER SUPPLIES

78SR/79SR Switching Regulators

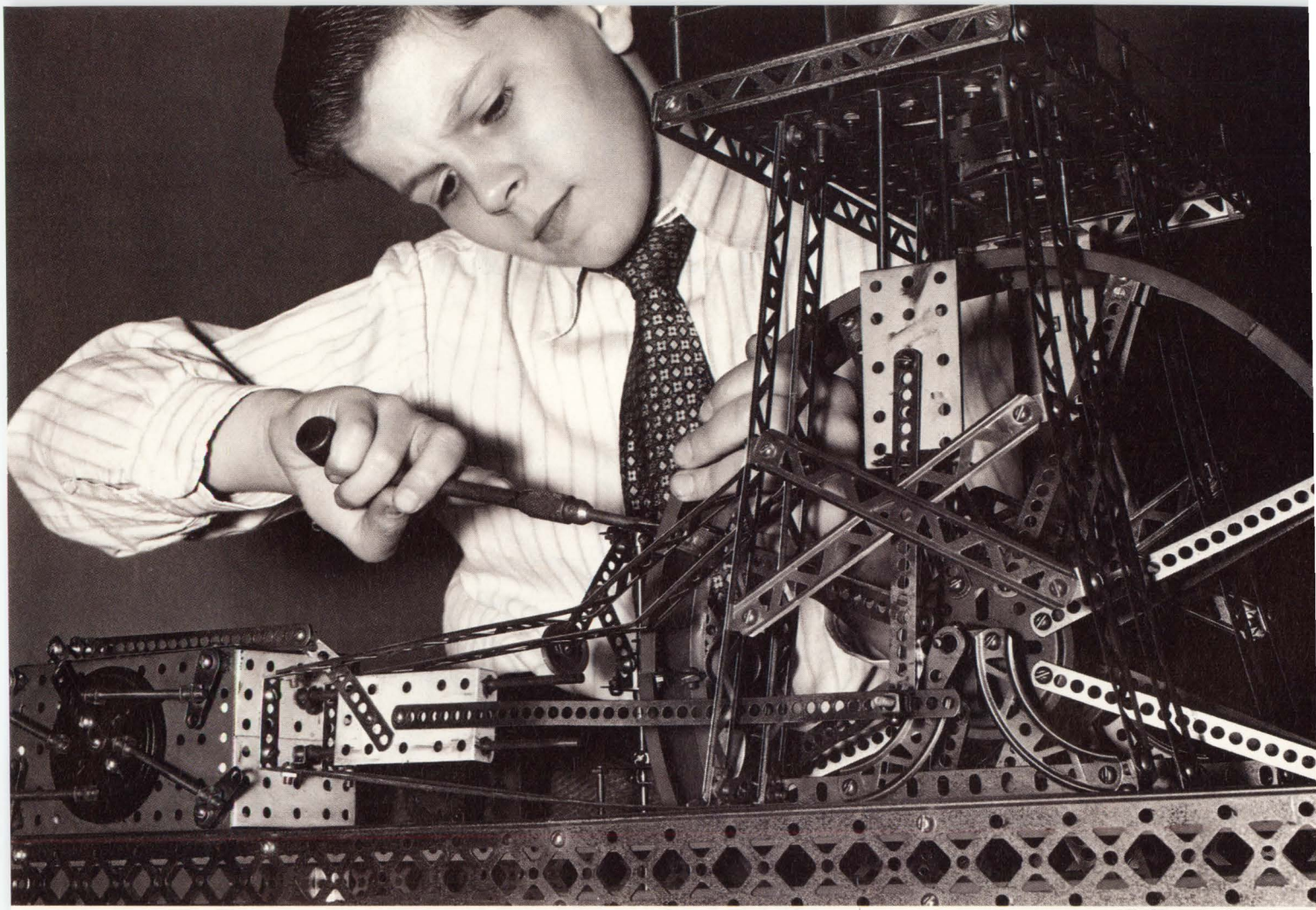
A startup company, Power Trends, is offering the 78SR and 79SR families of 3-terminal, positive and negative 1.5A switching regulators that can directly replace linear 3-terminal regulators. Switching frequency is 1 MHz and efficiency exceeds 87% under most operating conditions. As a result, power dissipation is significantly lower than that of linear devices, allowing the units to operate without a heat sink in many applications. The units produce their full rated current without a heat sink when the ambient air temperature is 65°C.



Innovations in the products lie in several areas: High-frequency switching-regulator technology, surface mounting, and planar magnetics produce 3-terminal regulators in packages the same size as those of linear devices. Laser trimming sets the units' output voltages with extreme accuracy. High-speed automated assembly yields economical devices despite complexity that is greater than ICs'. Notwithstanding that complexity, the vendor boasts of MTBFs greater than 100 years.

The vendor supplies the units trimmed for outputs of 5, 6, 8, 9, 12, 15, 18, and 24V in packages optimized for vertical or horizontal through-hole mounting or for surface mounting. The regulators require, at most, two external components—an optional capacitor from input to ground and another from output to ground. The regulators cost $12 (1000).

Power Trends Inc
Batavia, IL
(708) 406-0900



The Bettman Archive Inc.

Even the most ambitious project is limited by its parts.

Most kids use the pieces of their building toys just like they came out of the box. So they're limited by the characteristics of those pieces.

The same is true of today's suppliers of "custom" interconnect systems. Assembling systems from components that are readily available, they call these products custom when they're really only customized.

At Precision Interconnect we're often not satisfied with the components or assembly procedures readily available. So we design, test and implement our own.

First we ask every question imaginable about the application of the product. Then we apply our knowledge of manufacturing, materials, cable and connector designs, and termination processes to solve the problem.

So the complete interconnect systems we deliver will be high performance and application specific, meeting every requirement of your particular interconnect problem.

We know the whole is greater than the sum of the parts. And more functional if you challenge those parts.

P.I. miniaturized this cable of 68/40 AWG, 50 ohm coaxes to a .192" O.D. to fit into the end of an endoscope tube. The O.D. of one RG-59 is .242".

CIRCLE NO. 37

PRECISION INTERCONNECT

16640 S.W. 72nd Avenue
Portland, OR 97224
(503) 620-9400

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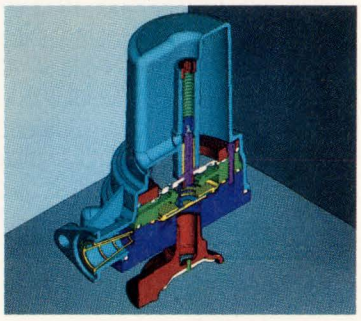
The IBM RISC System/ Designing on any other workstation

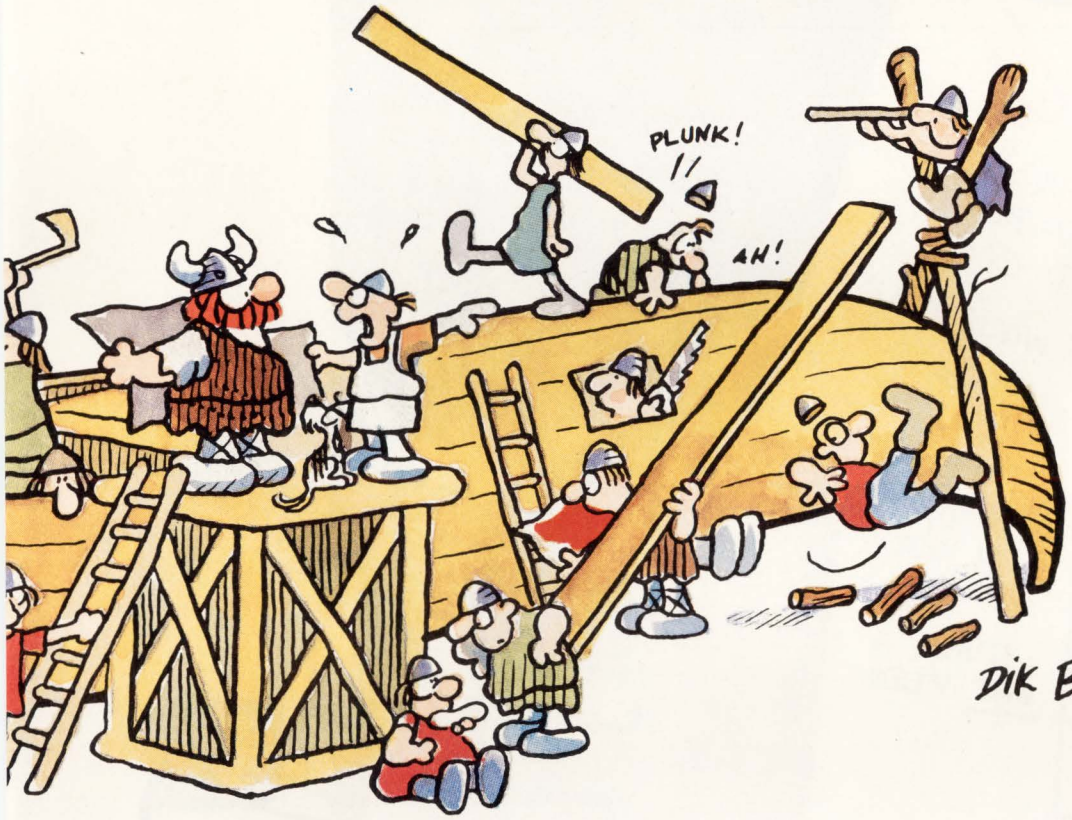
Whatever you're creating, you'll sail into a whole new age with any of the four POWERstations in the RISC System/6000 family. Because POWER (Performance Optimization With Enhanced RISC) processing can give you performance you've probably only dreamed about:



up to four instructions per machine cycle, 42 MIPS and 13 MFLOPS. Suddenly, complex designs don't take eons anymore.

The four RISC System/6000 POWERstations feature a range of graphics processors from grayscale to Supergraphics to satisfy any graphics demand. Great news for Power Seekers working on animation, scientific visualization, medical imaging and engineering solutions like CADAM,™ CAEDS™ and CATIA.™ And for electrical design automation, there's IBM's all new CBDS™ and an arsenal of over 60 EDA appli-

6000™ family.
will seem downright primitive.

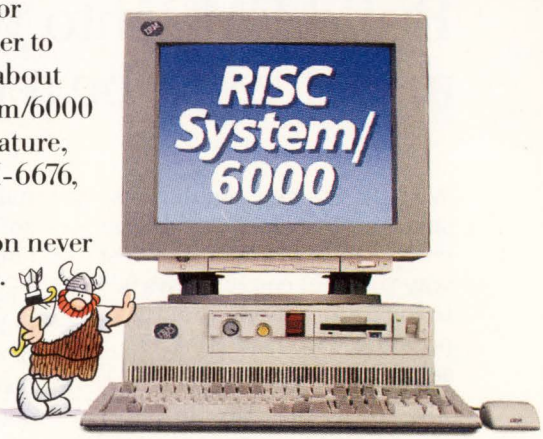


cations from more than a dozen vendors.

With every POWERstation, you can get an almost unimaginable palette of 16 million colors, which gives you 3D images so realistic, they fairly leap off the screen, with super sharp resolution of 1,280x1,024 pixels. And when it's time to call in the heavy artillery, the POWERstation 730 draws nearly one million 3D vectors per second. Like all POWERstations, it can come complete with its own graphics processor, freeing the POWER processor to rapidly create and analyze your designs. All at prices that won't sink anybody's budget.

So if you're tired of paddling upstream with yesterday's performance, call your IBM marketing representative or Business Partner to find out more about the RISC System/6000 family. For literature, call 1 800 IBM-6676, ext. 991.

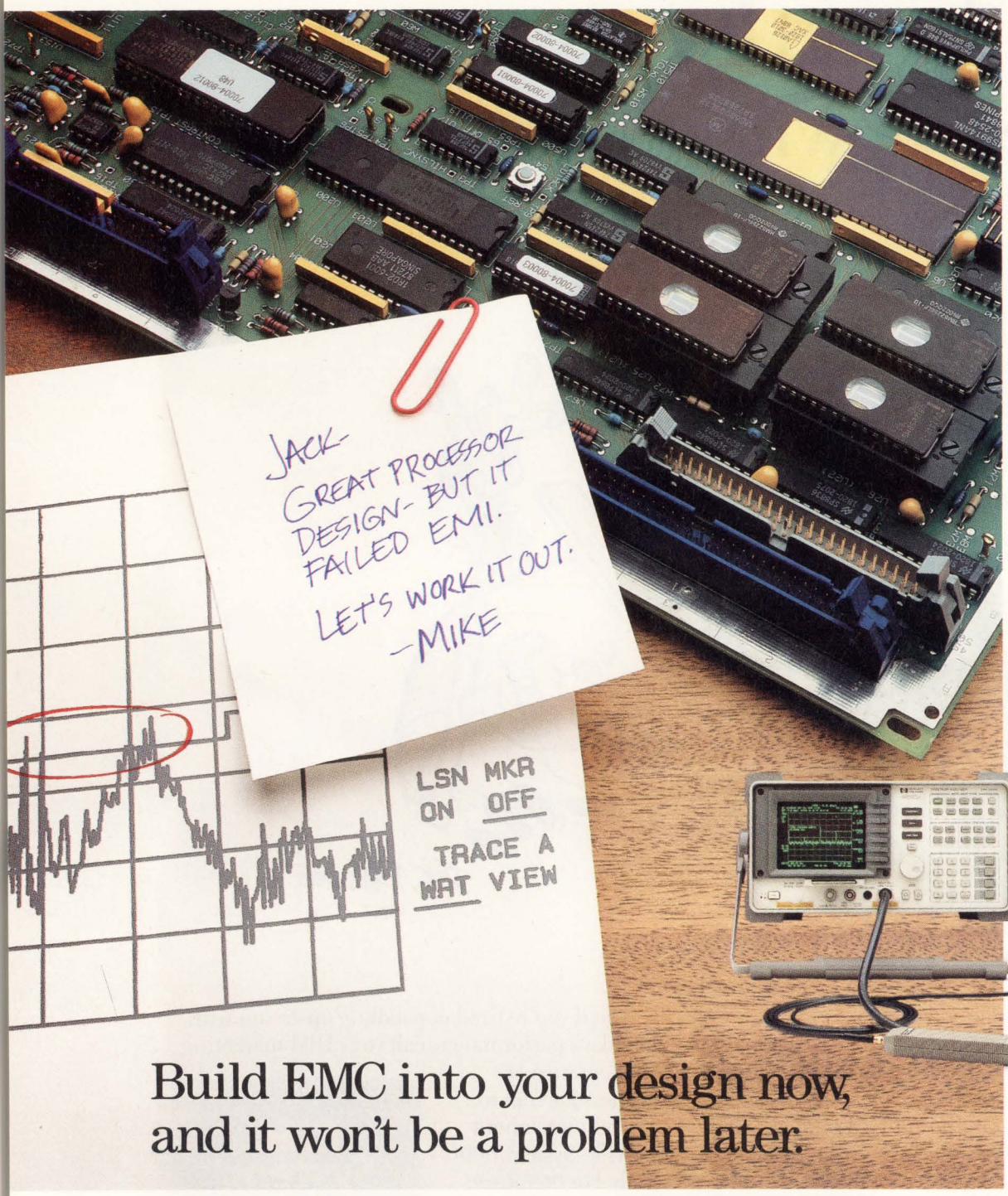
Civilization never looked so good.



For the Power Seeker.

IBM®

CIRCLE NO. 38



Build EMC into your design now, and it won't be a problem later.

With all the new regulations surrounding electromagnetic compatibility (EMC), the best way to avoid costly delays is to locate problems as early as possible. Two new HP EMC solutions make that easy.

The HP 84100A Design Development Solution helps you correct problem areas at the design stage. It pinpoints hot spots on breadboards and prototypes using a spectrum analyzer with software memory cards that simplify troubleshooting.

The HP 84110A Pre-Production Solution gives you added confidence that your designs will pass compliance. It has all the analysis capability, software and accessories you need to uncover conducted and radiated emission problems before final EMI testing.

So, find out how to build EMC into your designs. For information about HP's full line of EMC solutions and design training programs, call **1-800-752-0900.*** Ask for **Ext. 1350,** and we'll send you our EMC Measurement Solutions fact kit.

There is a better way.

HEWLETT PACKARD

See us at EMC Expo, Booth #212

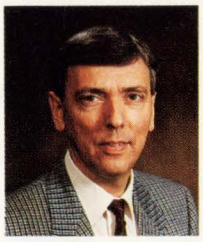
*In Canada, call 1-800-387-3867, Dept. 502

CIRCLE NO. 42

Please See our Design Seminar Listings on Page 192.

ANALOG SPICE SIMULATION MODELS

Spice models enjoy multiple sources



Several routes exist for obtaining simulation models, but availability and price vary remarkably.

Brian Kerridge,
European Editor

Interest in analog simulation is snowballing. Texas Instruments responded to more than 23,000 requests in the US for its op amp macromodel manual and disk during the first six months after publication. Forty percent of Comlinear Corp's customers now demand Spice models. Precision Monolithics fielded literally thousands of demands for its models. It calls the interest the Spice model craze.

And so the quest for simulation models continues.

Component vendors mostly ignore your requirement for models, hoping that the need for models will fade away. Notable exceptions are a handful of op-amp suppliers, who have an expanding range of models and data to support their preferred types.

Dedicated and independent model vendors do exist, but there are surprisingly few of them. They operate largely as modeling consultants, tailoring their service to specific requirements. Depending upon your demands, one transistor model can cost you from $75 to $2500.

Vendors of simulation packages have the strongest motivation to source models. They want to promote and support their software. Simulation packages generally start you off with a library of models for popular components. Additional software helps you to expand on that library. This software translates component data into Spice models. Depending upon the simulation package you choose, the component data you input comes from component data sheets or from measurements of samples of the device.

Pros and cons exist with either method. Going the hardware-measurement route involves deciding upon a top-end software package, which may cost in the region of $25,000. The software includes drivers for controlling component parametric test and measurement equipment, which adds an additional $50,000 to your bill. Dedicated modeling vendors themselves use this route, but apart from them, only component designers can generally justify the expense. **Fig 1** shows a summary of routes for obtaining models.

Component vendors are in the best position to supply accurate data for simulation-model parameters. It is almost certain that they use simulation techniques in their production processes. Nonetheless, only a trickle of Spice models is officially available from this source.

In exchange for a nondisclosure agreement, key-account purchasers can probably negotiate access to a component vendor's in-house Spice models. This route will provide job-satisfaction for aggressive buying managers, but it is likely to leave you with a Spice model and nothing else. The component ven-

Analog Spice simulation models

dor's motivation and capability to support your work with an in-house model is likely to be nonexistent.

Motorola makes a token effort at support. It publishes 12 Spice models for RF small-signal transistors. For other models, the company steers you toward one of the few independent model vendors, like Silvaco. Motorola's Norm Dye, an applications engineer, doubts the validity of using Spice models in simulations above 100 MHz. The Spice model by itself is not reliable at RF unless something is done to characterize package parasitics. The Spice Gummel-Poon transistor model mirrors the component die only. If you extract Gummel-Poon parameters at RF on a packaged component, then the parameters assume invalid values to accommodate unmodeled lead inductance and capacitance.

Avantek helps you skirt this problem. It publishes models for both packaged and unpackaged components. The company devotes one chapter of its data book to device modeling. The book includes net lists for bipolar transistors, GaAs FETs, and MMICs (monolithic microwave ICs). In each case, the book shows subcircuit schematics of the model with the package parasitics. A representative selection of companies that supply models appears in **Table 1**.

Op-amp vendors provide a refreshing exception to the no-support rule. They offer a good range of models for new and preferred types, free of charge. In all cases, the vendors offer macromodels, which have a simplified model structure but retain essential simulation characteristics. Op-amp macromodels emanate from an early standard model configuration, called the Boyle model.

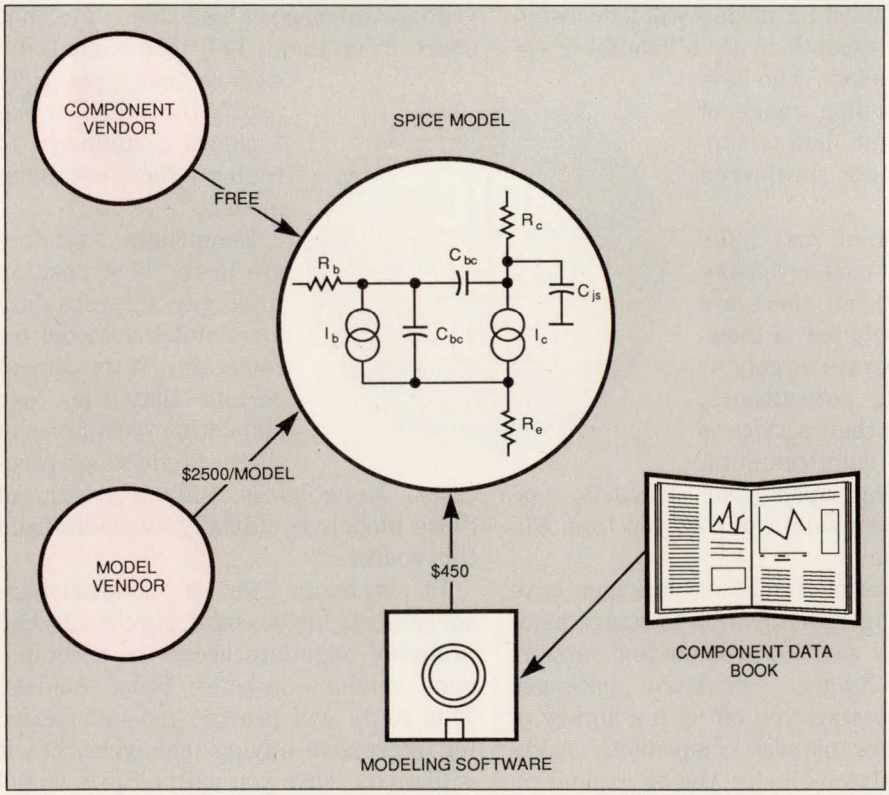


***Fig 1—Various paths can lead you** to a Spice model.*

Boyle models disregard certain aspects of an op amp's performance, leaving vendors to express as much enthusiasm for their particular enhancements to the model as for the op amps themselves. Modeling enthusiasts dwell endlessly on these developments, and several articles cover the subject (**Ref 1**). Whatever the level of enhancement, vendors' support data fairly and clearly states the deficiencies.

Precision Monolithics Inc's op-amp macromodels depart furthest from the familiar Boyle standard. Its most recent development, manifest in the PMI OP-177, adds noise-generator elements to input stages for modeling broadband, thermal, and 1/f noise (**Fig 2**). PMI's op-amp macromodels in general boast superior frequency-response simulations to Boyle models because of the unlimited poles and zeros that the macromodels can accommodate. Boyle models limit poles to two and ignore zeros entirely.

Joe Buxton, an applications engineer with PMI, says that the motivation to produce Spice models was user driven. Models for later products simply weren't available in simulator libraries, and users were looking for more accurate models. Enhancing the Boyle model extends simulation time, but PMI believes that the time penalty is not a problem. Buxton maintains that the majority of users model only sub-sections of their overall circuits at one time. He defends the complexity of the company's model by quoting simulation times for a 4-op-amp bandpass filter. A 12-MHz, 286-based PC takes <1 minute for a dc simulation and <5 minutes for an ac simulation. On a 25-MHz, 386-based version, simulation speeds increase by a factor of eight.

Both Texas Instruments and Burr-Brown offer more-or-less Boyle models. They developed their re-

Analog Spice simulation models

spective models using modeling software from MicroSim, ensuring model compatibility with MicroSim's PSpice simulator. However, their models are incompatible with Berkeley Spice 2G.6 simulators. Texas Instruments acknowledges this shortcoming, and plans to publish errata information this month.

Manually editing a net list to obtain compatibility is not difficult, but it somewhat negates the advantage of receiving data on a floppy disk. Intusoft recognizes this problem, and for $20 sells a floppy disk, which contains a library of models from all component vendors converted to classic Spice format.

Comlinear publishes net lists for eight of its principal current-feedback op amps in its product data book. Michael Steffes, the company's applications engineering manager, says that the company's reason for supplying the models came in direct response to customer demands. Of the 40% of Comlinear's customers who now request Spice models, he suspects that barely 10% eventually perform simulation. It seems that most customers expect models to help them predict likely production spreads in their designs. When they discover that this level of information is not available, the models are set aside.

This scenario airs a general grievance about all semiconductor models which may result from exaggeration of the benefits of Monte Carlo analysis by simulation vendors. The capability to perform tolerancing truly exists within Spice-based simulators, but you cannot exercise this feature fully, as the tolerancing data for semiconductor model parameters is not readily available. It is true that a good design is insensitive to a semiconductor's characteristic spreads, but without semiconductor-model parameter tolerances, you cannot use simulation to prove it.

Start-up library is available

Most simulation packages contain a library of models of popular components, but these libraries cover only a small proportion of available devices. Paul Tuinenga, a software engineer with MicroSim, explains the difficulty. First, there exist almost 500,000 semiconductor types. Second, regular library updates can't hope to include all new component releases. The PSpice simulator currently includes a model library of around 3000 of the more frequently used devices.

Charles Hymowitz, chief applications engineer at Intusoft, stresses the importance of quality rather than quantity of models in a library. He directs users to beware the un-

Table 1—Representative component vendors with Spice models[1]

Manufacturer	Component types	Format	Spice compatibility	Comments
Avantek	Bipolar transistor MMIC, GaAsFET	Data book net list	Spice	8 bipolar transistor models, 9 GaAsFET models. Package subcircuits shown with values.
Burr-Brown	Op amp	Floppy disk	PSpice[2]	2 models, OPA620 and 621. App note AN-167.
Comlinear	Op amp	Data book net list	Spice	7 models, CLC205, 206, 220, CLC231, 400, 405, 501. App note OA-09 includes net lists & schematics. Performance curves for CLC400.
Harris Semiconductor	Op amp	Floppy disk	Spice	7 models, HA2539, 2540, 5102, HA5104, 5112, 5114, 5190. App note per model with performance curves.
Linear Technology	Op amp	Floppy disk	Spice	40 models. Disk includes demo version of MicroSim's PSpice to allow you to generate performance curves. App note 41 answers 20 typical novice's questions.
Motorola	RF transistor	Printout	Spice	12 models. Includes MRF522, 544, MRF571, 901, 911, 941, 951, 2N2440, 2N6338, 2N6617, 2N6618, 2N6679.
Precision Monolithics	Op amp	Floppy disk	Spice	54 models. Includes AMP-01 & AMP-02 instrumentation amp models. OP-77 and OP-177 includes noise modeling.
Texas Instruments	Op amp	Floppy disk	PSpice[2]	106 models listed in macromodel data book. Support hotline number (214) 997-3389.

Notes: 1. All models in this table are free of charge.
2. PSpice simulator is a MicroSim product.

Analog Spice simulation models

supported model. You should insist that a data sheet or some type of explanation and application note accompany the model. He says that some libraries are beefed up by a simple restatement of Spice default-model parameter values, or by just listing a series of equivalent type numbers for the same model. He says that models should come with a listing of all the effects that the model simulates, and, just as important, those that it omits.

Intusoft offers a free modeling service to users of its IsSpice simulator. As well as developing its own models, the company gathers, vets, and redistributes models from component vendors. The company publishes texts and a free bimonthly newsletter on modeling (**Ref 2**).

Although all simulation packages allow you to modify models by text-editing the net list of a similar component, the problem lies in knowing what new model parameters to insert for the new type number. Component data sheets offer a primary source of information, but figures quoted do not relate to Spice model parameters.

PC-based simulators from Intusoft and MicroSim include software for direct translation of values commonly found in component manufacturer's data sheets to Spice model parameters.

MicroSim's Parts ($450) is the modeling option for the PSpice simulation package. It establishes model parameters for diodes, bipolar transistors, JFETs, power MOSFETs, and op amps. Graphical feedback, based upon the derived parameters, indicates the validity of characterization. The program outputs model statements for transistors, and, in the case of op amps, subcircuit net lists.

Intusoft's Spicemod modeling program costs $200; it operates independently of a simulator. It produces diode and transistor model files that are strictly Spice compatible (**Fig 3**). It behaves as a modeling spreadsheet, updating model parameters each time you enter a new value from the data sheet. The more data you enter on a device, the more accurate becomes the model. And if some data values are missing, the program makes estimates for you.

If you decide that the models you need are not accurate enough, or just not available elsewhere, your

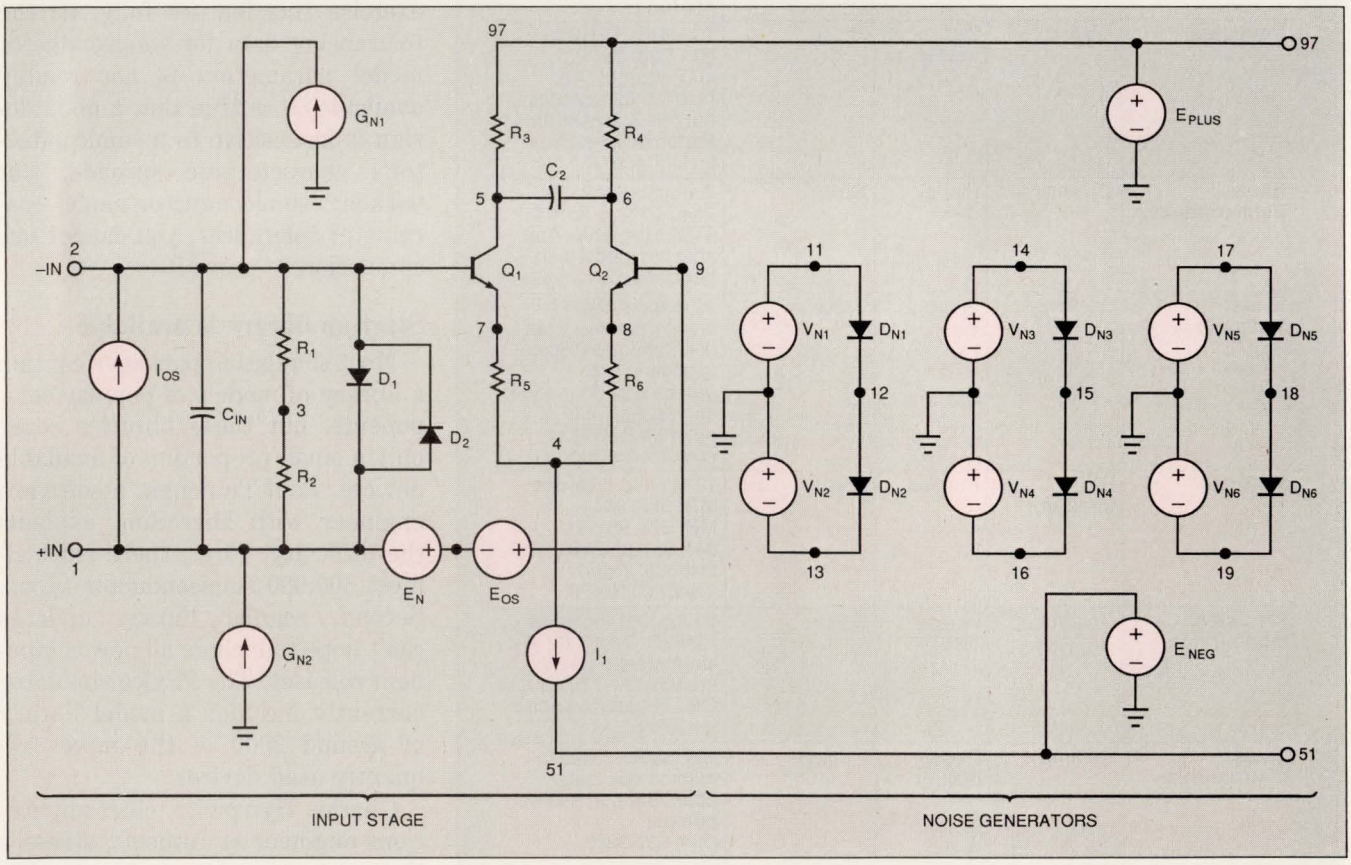


Fig 2—PMI's macromodel for op amp OP-177 *includes noise generators G_{N1}, G_{N2}, and E_N in the input stages to create broadband, thermal, and 1/f noise.*

Analog Spice simulation models

final recourse is to use a modeling vendor. These vendors derive model parameters from measurements of a hardware sample, and the service covers mainly bipolar junction transistors.

Their in-house equipment includes a range of instrumentation, which, under software control, collects data from the sample to be modeled. This data produces sets of characteristic performance curves and provides model-parameter estimates. A simulator then operates on a model of the device, iteratively optimizing the model parameters while using the characteristic curves as a target.

Silvaco offers access to a library of around 2500 transistor types, which have been modeled by this method. If the model you need is there, it costs you $350. If not, then the company will perform a custom model characterization of your component for an additional charge, requiring typically six samples. The system accepts packaged or unpackaged components, although if the measurements involve probing a wafer, the cost escalates to around $4000.

MEL, a Philips company, offers an equally adaptable modeling service at its Device Modeling and Characterization Center (DMCC). Although the company concentrates on parameter determination for bipolar junction transistor models, it also develops and provides models of active and passive components for use in a variety of circuit simulators and applications.

DMCC has extensive modeling capability, comprising temperature characterization and the determination of packaging parasitics. It will give you a set of parameters for one device for £1500. For £15,000, you'll receive parameters for 10 devices and membership in the DMCC user group. Members have access to DMCC's library, which currently contains Spice models for 29 diodes, 120 bipolar junction transistors, and nine FETs.

Analog and RF Models offers a special service for accurate RF models of bipolar transistors, JFETs, MOSFETs, and MMICs. The company uses only data sheets for source information. Bill Sands, the company's president, explains two advantages of this technique. First, it holds down the price of one model to $75. Second, data-sheet information represents the average of many components over several years, whereas measurements of samples may depart from typical data. The company's in-house software gives precedence to ac and transient characteristics of a model, to 5 GHz. Sands maintains that normally just enough data is available to produce an accurate model. At a minimum, this requires I_C, V_{CE}, $f_{\tau MAX}$, and a set of s or Y parameters. If s or Y parameters exist for three different frequencies, then the program can model package parasitics.

Hymowitz at Intusoft summarizes the merits of modeling from data-sheet and hardware information. With hardware modeling you can never be sure if the sample is a maximum, minimum, or typical part. Nonetheless, for diodes, transistors (excluding RF types), and

```
SPICEMOD 1.1 ========== Bipolar Junction Transistor (Q) ============ 07-13-1990
                    .MODEL Name (MPSA06) = MPSA06        (Estimated Data)
       Type (GeNPN, GePNP, SiNPN, SiPNP) = SiNPN         (Entered Data)
     Max. Collector-Emitter Voltage, VCEO =    80.000 V.  <VAF>
          Max. Emitter-Base Voltage, VEBO =     4.000 V.  <VAR>
   Max. Continuous Collector Current, IC =     0.500 A.  (Scales all Values)
                 Peak Current Gain,  hFE =   220.238      <BF>
        High Current 50% HFE Point,  IH =     0.300 A.  <IKF>
         Low Current 50% HFE Point,  IL =     0.300 mA. <ISE>
  Collector Saturation Voltage, VCE(SAT) =     0.140 V.  <RE> (RC, RB)
                               at IC =     0.500 A.  (near max. current)
      Base-Emitter On Voltage, VBE(ON) =     0.653 V.  <IS> (ISE)
                (at IB = IC/10) at IC =     0.020 A.  (at IC(max) / 25)
      Max. Gain-Bandwidth Product,  fT =   219.203 MHz.<TF>
         Storage Time at I(fTmax),  TS =     0.325 us. <TR>
               Output Capacitance, COB =     8.000 pF. <CJC>
                               at VCB =     5.000 V.
                Input Capacitance, CIB =    40.277 pF. <CJE>
                               at VEB =     1.000 V.  (Reverse Bias)
========================== SPICE MODEL PARAMETERS: ============================
.MODEL MPSA06   NPN (IS= 5.08E-14 NF=1.0 BF= 286  VAF= 161
+ IKF= 3.0E-01 ISE= 1.77E-11 NE=2.0 BR= 4  NR=1.0 VAR= 16
+ XTB=1.5 RE= 1.0E-01 RB= 4.1E-01 RC= 4.1E-02
+ CJE= 5.3E-11 CJC= 1.6E-11 TF= 7.3E-10 TR= 1.4E-07)
      << SELECT WITH ARROWS, ENTER NEW DATA - F1 HELP - 'Esc' WHEN DONE >>
```

Fig 3—Intusoft's Spicemod modeling software *operates like a spreadsheet. Spice model parameters update as you enter a range of values from a component data sheet. The more points you enter, the more accurate the model becomes.*

JFETs, hardware modeling produces accurate data. This hardware modeling can be a great help when data-sheet information is incomplete or nonexistent. Data sheets often omit plots for capacitance vs reverse voltage, IV curves, H_{FE}, and V_{BE} vs I_C. You cannot determine Spice model parameters without this data. Although data sheets do not provide enough information to create a complete model, enough data is usually available for a dc model, and enough for a good shot at an ac model. For MOSFETs, unless level 1 models suffice, modeling from hardware measurements is almost a must, as data sheet information is quite insufficient.

Models for power MOSFETs and power, RF, and Darlington transistors require a subcircuit representation. Data-sheet information is usually adequate, but optimization must be done with Spice, as there is no way to input the variable subcircuit topology.

Op-amp data sheets contain more than enough information to produce models.

The saying, "you get what you pay for," is never more true than when trading simulation models. The skill is to decide what modeling source and attendant expenditure meets your simulation objectives.

If you use simulation to check a design's basic functionality or just to throw around ideas, then loosely defined models suffice. For component design and manufacture, demand a highly accurate simulation result with the best models from modeling specialists.

Between these application extremes lie a lot of middle ground. Clearly, no one model, even for the same component, is ideal for the range of applications possible. Your skill and knowledge as an analog engineer, far from being diminished by the use of simulation, must expand until you know as much about your simulation models as you do about the components being modeled. EDN

References

1. Alexander, Mark and Derek Bowers, "New Spice-compatible op-amp model boosts ac simulation accuracy," *EDN*, February 15, 1990, pg 143; and "Op-amp macromodel proves superior in high-frequency regions," *EDN*, March 1, 1990, pg 155.

2. Meares/Hymowitz, "Simulating with SPICE", and "SPICE Applications Handbook Vol 1," and *Intusoft Newsletter*, Intusoft.

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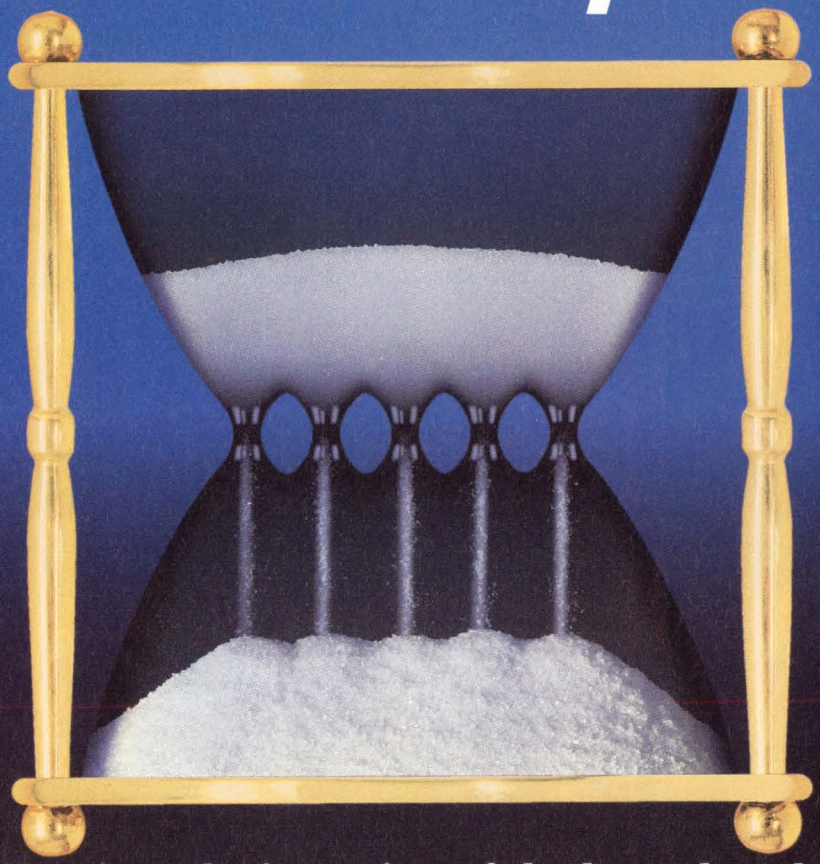

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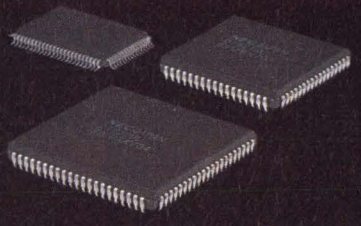

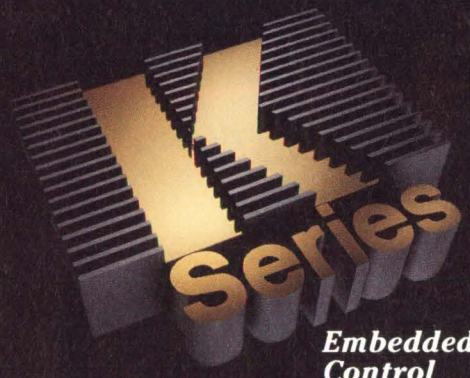

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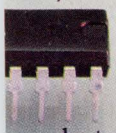

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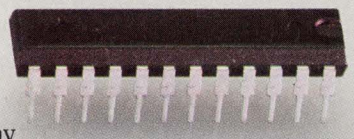

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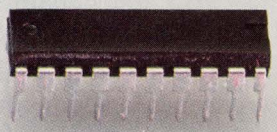

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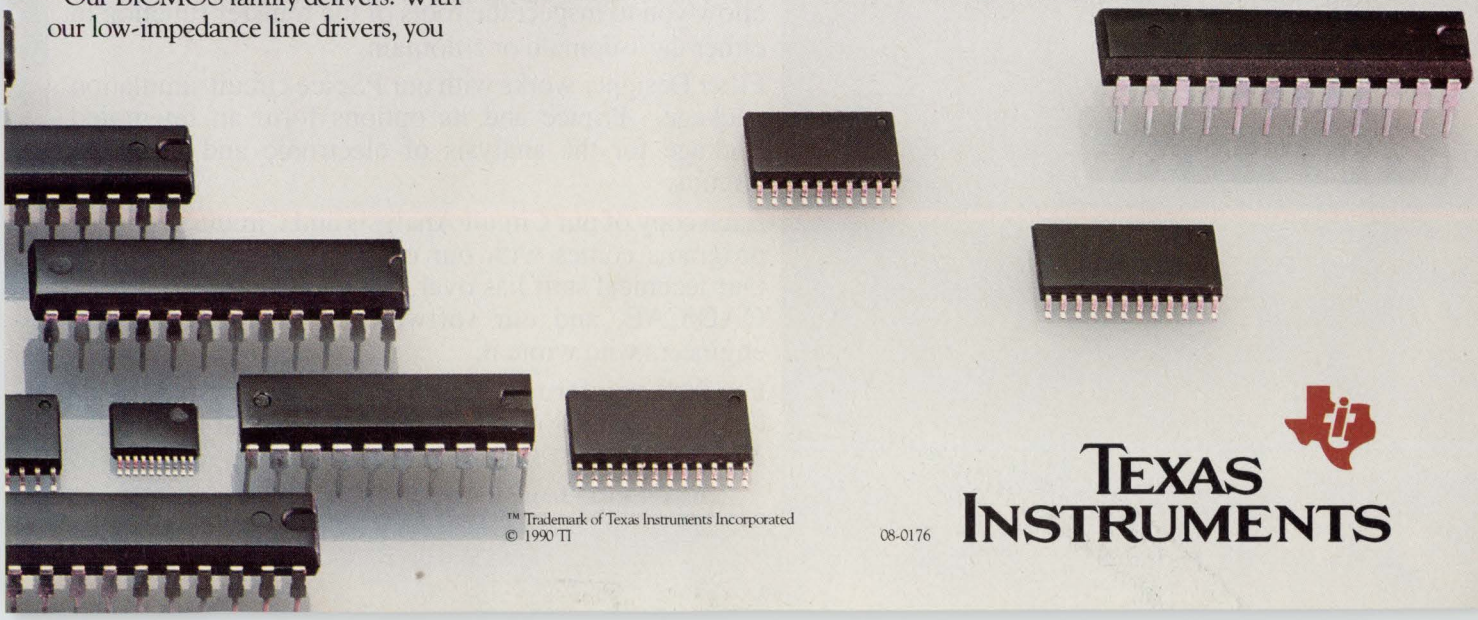

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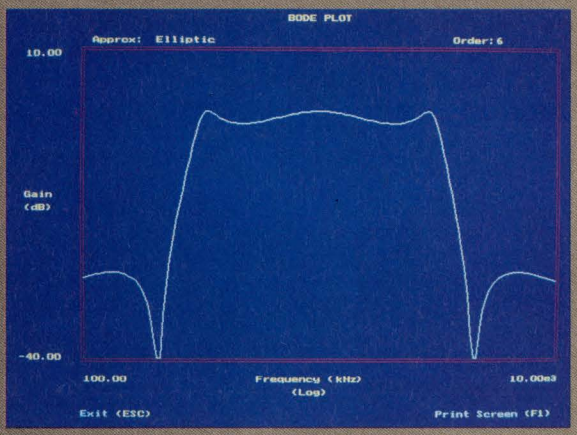

Advanced Filter Designer Bode Plot

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CIRCLE NO. 39

CRYSTAL OSCILLATORS

Signal sources handle tough timing jobs

As system speeds continue to increase, extremely precise clock sources, such as crystal oscillators, become more critical.

Tom Ormond,
Senior Editor

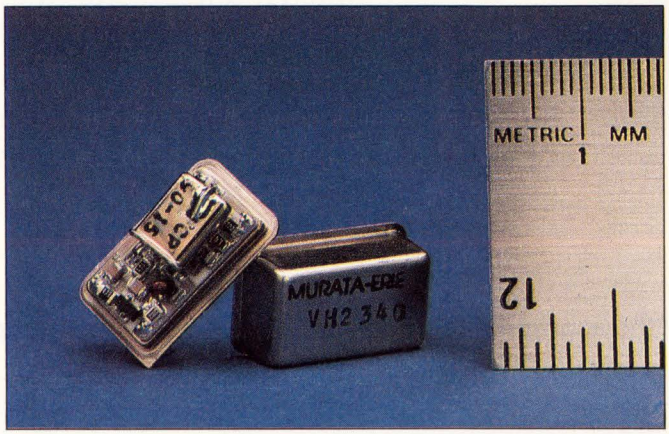
System operating speeds in the hundreds of megahertz range are far from uncommon. At such speeds, precise and stable clock frequencies are an absolute must. In a 100-MHz oscillator, a 0.1% stability figure translates into a frequency error of 100 kHz. This figure might seem trivial, but such a deviation could considerably degrade the performance of a high-speed electronic system. The only way to obtain the stability figures necessary in today's design arena is to employ a crystal oscillator as the clock source.

When you go shopping for a crystal oscillator, you'll find you have a varied product menu to choose from. Your options include uncompensated oscillators, temperature-compensated oscillators (TCOs), digitally compensated oscillators (DCOs), voltage-controlled oscillators (VCOs), and ovenized oscillators (OCOs). The choice of oscillator type depends on the stability requirements of your application. You might also have to make some tradeoffs concerning power consumption and oscillator size, but these considerations are normally secondary to stability.

Simple crystal oscillators are fixed-frequency devices that have no temperature compensation. Designers mainly use these devices as clocks in digital systems where stability requirements are not too severe. The devices' typical frequency stability specs are ±100 to ±1000 ppm. Manufacturers of uncompensated crystal oscillators often use hybrid assembly techniques to produce devices with small volumes. The cost of these devices varies depending on a number of factors, but uncompensated crystal oscillators are typically the least expensive crystal oscillators available.

KDS America, NEL Frequency Controls, and Pletronics all offer uncompensated crystal oscillators. As the data in **Table 1** illustrate, these crystal oscillators have a wide range of output frequencies—156 kHz to 200 MHz. The units feature TTL- and CMOS-compatible outputs and are fairly inexpensive and quite small. However, they do have a limited operating-temperature range.

Voltage-controlled crystal oscillators (VCOs) offer a little more capability



Featuring outputs of 15 to 60 MHz, *VH2340 oscillators from Murata Erie have a ±100-ppm deviation capability, a stability of ±25 ppm max, and a 0 to 70°C operating range. With a mounted height of 0.32 in., the units are suitable for high-density applications.*

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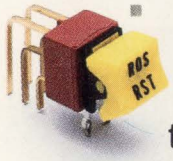

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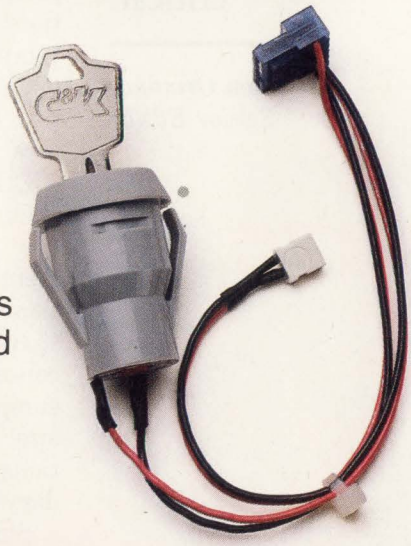

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Crystal oscillators

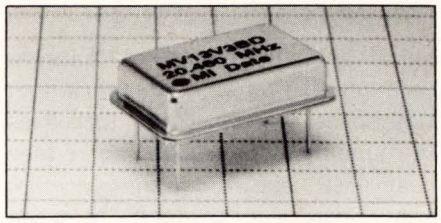
than do simple crystal oscillators. The VCO has an input terminal that lets you apply a control voltage and pull the oscillator output frequency in either direction. These devices are available from AT&T, Conner-Winfield, MF Electronics, M-tron, Murata Erie, and Vectron.

This VCO tuning capability is advantageous in a number of applications. You can use the devices to clean up a noisy incoming signal or multiply a frequency by a precise integer or fraction of an integer without introducing any error. These devices are quite useful for detecting the frequency modulation of an incoming signal. A VCO also lets you custom tailor a phased-locked loop.

The frequency-deviation capability of typical VCOs (**Table 1**) ranges from ±50 to ±200 ppm. Control inputs operate with standard logic-level signals, and output-frequency figures span the 3.5- to 200-MHz range. However, VCOs have a somewhat limited operating-temperature range. When your application involves wide operating temperatures and high stability, you should go with a compensated oscillator.

Handling tougher environments

In an ovenized crystal oscillator (OCO), a temperature-controlled module houses the crystal and the associated electronics. This module maintains the crystal at a stabilized temperature that is higher than the ambient temperature at which the oscillator is likely to operate. No other type of oscillator can match the stability characteristics of an OCO. Over the range of −55 to +85°C, OCOs can attain typical stability figures of ±1 to ±100 ppb (parts per billion). Over narrower temperature ranges, stability figures are even better.



Offering a selection of pull ranges *to satisfy a variety of phase-locked-loop applications, M-tron's MV Series voltage-controlled oscillators are general-purpose, HCMOS-compatible units with center frequency outputs of 3.5 to 25 MHz.*

You have to pay a price for this stability performance. OCOs draw a lot of power, require a lot of pc-board space, take time to warm up, and are expensive. Two factors affect power consumption: the amount of oven insulation the device has and the temperature differ-

Table 1—Representative crystal oscillators

Manufacturer	Model	Type	Frequency (MHz)	Stability (ppm)	Deviation (ppm)	Control voltage (V)	Output	Operating range (°C)	Size (in.)	Price
AT&T	157	VCO	50 to 200	NS	±50	0 to −5.5	10K ECL	0 to 70	0.97×0.795×0.28	$50 (1000)
Bliley	N60B	OCO	5 to 15	0.005	NA	NA	Sine wave	0 to 50	2.25×2.25×1.0	$225 (100)
Connor-Winfield	HV54-160	VCO	51.840	±20	±80	0 to 4.8	MOS square wave	0 to 70	0.798×0.497×0.26	$87.95 (10)
Hybrids International	1406	TCO	1 to 40	±10	NA	NA	TTL/HCMOS square wave	0 to 70	0.82×0.52×0.2	$15 to $25 (1000)
K&L Oscillatek	M84	TCO	0.001 to 32	±2 to ±15	NA	NA	TTL, ECL, CMOS, sine wave	0 to 50 to −30 to +85	0.8×0.5×0.375	$50 (100)
KDS America	DOC 49/492	CO	0.156 to 20	±50 to ±100	NA	NA	MOS, TTL	−10 to +70	11×5×4.5 mm	$2.50 (1000)
MF Electronics	M2000	VCO	8 to 32.768	±50	±175	0 to 10	TTL	0 to 70	0.795×0.495×0.2	$15 to $20 (OEM qty)
M-tron Industries	MV	VCO	3.5 to 25	±100	±200	0 to 5	HCMOS, TTL	0 to 70 −40 to +85	0.815×0.526×0.265	$10 (1000)
Murata Erie NA	VH2340	VCO	15 to 60	±25	±100	0 to −5	ECL	0 to 70	0.815×0.515×0.32	$70 (1000)
NEL Frequency Controls Inc	HF-5700	CO	0.78 to 200	±0.01%	NA	NA	TTL, ECL	0 to 70	1.08×0.515×0.23	$20 (1000)
Piezo Technology	X01190C	OCO	9 to 25	0.005	NA	NA	Sine wave	−35 to +95	2×1.6×0.9	From $1500
Pletronics Inc	DF1100	CO	4 to 60	±25 to ±100	NA	NA	Dual TTL, CMOS	0 to 70	0.8×0.5×0.2	$4.37 (1000)
Vectron Laboratories Inc	CO454V	VCO	8 to 200	±10 to ±50	±30 to ±100	5, ±5	100K ECL	0 to 50 −55 to +85	0.98×0.8×0.2	From $100

Notes: CO=crystal oscillator, VCO=voltage-controlled crystal oscillator, TCO=temperature-compensated crystal oscillator, OCO=ovenized crystal oscillator, DCO=digitally compensated crystal oscillator, NA=not applicable, NS=not specified.

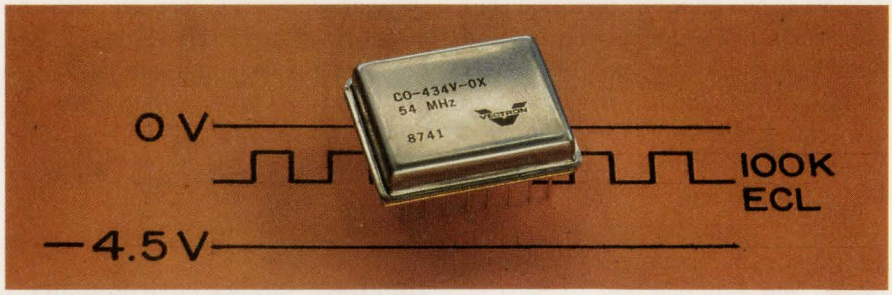
Crystal oscillators

ential between the oven temperature and the ambient temperature. When the manufacturer increases the amount of insulation to reduce heat loss, the oscillator package gets larger—a tradeoff between power consumption and size.

Warm-up time is the time the OCO requires to reach the operating temperature required to stabilize its output frequency. To a large extent, warm-up time depends on the amount of power available and the thermal mass of the oven. Warm-up time can be as long as 10 minutes.

Using a single supply to power an OCO is possible, but using one supply for the oscillator and a second supply for the oven is wiser. To power the oscillator, you'll need a supply that has the same regulation and noise characteristics as the supply you're using to power the system logic. You don't need a well-regulated supply to power the oven. Typical supply requirements can be as high as 20W at turn on; after the oven stabilizes, the supply's power drain can be as low as 2W.

Although they can't match the stability performance of OCOs, temperature-compensated crystal oscillators (TCOs) do have some advantages over OCOs. Their warm-up time is significantly shorter (in the microsecond range), their power consumption is in milliwatts, and they are smaller and less expensive.



Significantly reduced in size through hybridization, *Vectron's CO-454V crystal oscillators are 100K ECL compatible and provide outputs of 8 to 200 MHz. Housed in a 0.8×0.98×0.2-in. double DIP, the oscillators operate over the −55 to +85°C range.*

Getting the right answers

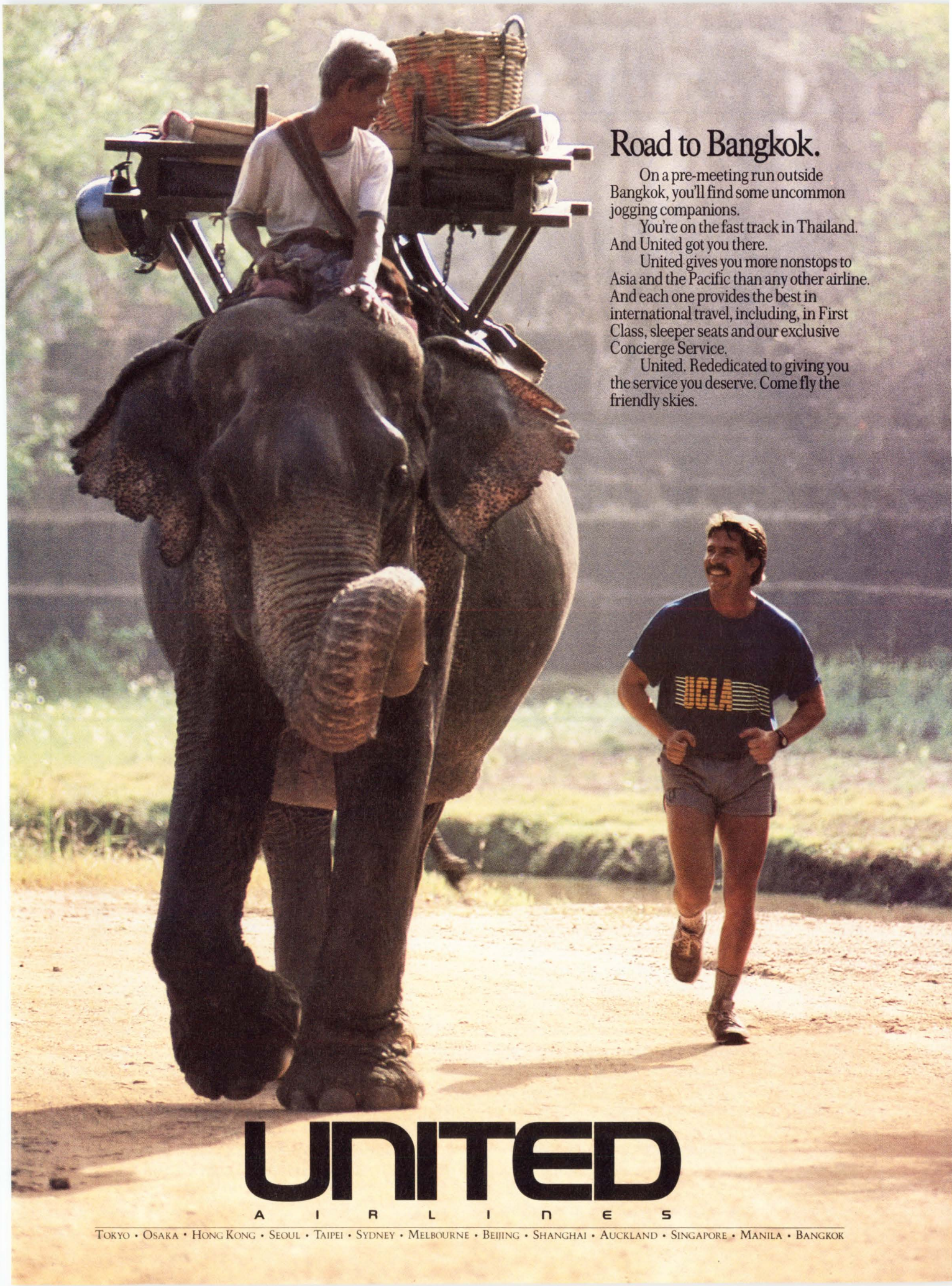
The frequency-deviation vs control-voltage specifications for voltage-controlled crystal oscillators (VCOs) are simple and explicit. Unfortunately, most users devise their own schemes to confirm the validity of these specifications. These schemes are often difficult to implement and are prone to operator error.

A software program can take the uncertainty out of confirming whether oscillators meet published specifications. MF Electronics has a VCO test program that runs on an IBM PC/XT or compatible computer. The complete test system requires two add-in boards and an IEEE-488-controlled frequency counter. The two add-in boards are an IEEE-488 bus card and an analog-output card that generates the control voltage levels. Both are commercially available. With this system, users can perform a deviation vs control-voltage test in about three seconds.

Typically, the deviation specification for a VCO will list the nominal center frequency and the low and high control-voltage levels (VL and V^H, respectively) that define the boundaries of the center frequency. To check the VCO, the test system applies four control-voltage levels (<VL, V^L, V^H, and $>V^H$), compares the resulting frequency against the oscillator specification, and makes a pass/fail determination. You can use this test system in production, as well as for smaller runs in the quality assurance and incoming inspection departments.

The program comes with several of the most common control-voltage conditions preset. It also includes options that let users establish their own voltage bands. The oscillator test starts when the test operator inputs a frequency input. The tester steps through the voltage levels, reads the oscillator frequency, and makes an expected/actual comparison. The system displays the applied control voltage and the resulting output frequency during the test. If an oscillator fails one of the tests, the screen displays a failure indication. The operator has the option to retest or step through the voltage levels one by one under his or her own control. The system also lets the operator print out voltage-frequency characteristics.

For interested readers, MF Electronics will provide the test program on a 5¼-in. disk along with a user manual for no charge. For more information, contact Marty Finkelstein at (914) 576-6570.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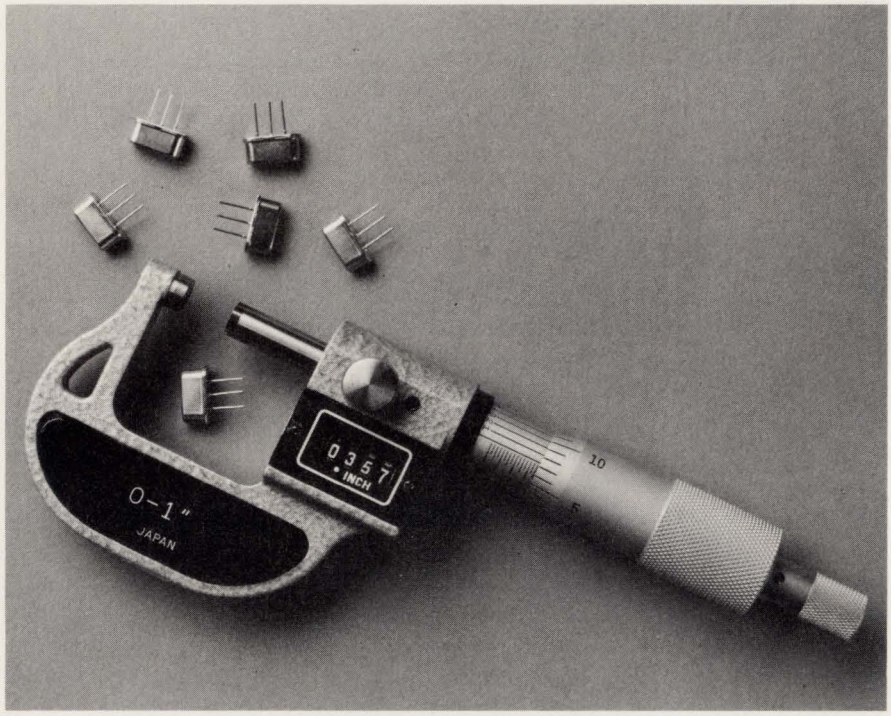
TECHNOLOGY UPDATE

Crystal oscillators



Small size and low power consumption *are key features of KDS America's DOC-49/492 oscillators. Offering outputs of 0.156 to 20 MHz, the units measure 11×5×4.5 mm and consume less than 25 mW.*

Analog TCOs use a temperature-sensitive, custom-tailored compensation network to tune the oscillator just enough to offset the uncompensated frequency change with temperature. The result is that the net oscillator stability is much better than that of simple crystal oscillators and VCOs. Standard compensation techniques can achieve stabilities of ±2 ppm over the −30 to +85°C range. As with OCOs, stability figures for TCOs are even better over narrower temperature ranges. Unlike OCOs, you can power a TCO with a single supply without running into problems.

These TCOs employ analog schemes to develop temperature compensation. However, you can also find TCOs that use digital techniques to provide temperature compensation. These digitally compensated crystal oscillators (DCOs) have excellent stability figures but

Put the source where it's needed

As pc boards and bus interfaces run at increasingly higher clock frequencies, handling high-frequency clocks becomes more difficult. The problems associated with routing high frequencies across a densely populated pc board include noise, harmonics, signal loss, and routing crosstalk. The ICD2031 family of satellite oscillators from IC Designs lets designers avoid these problems by placing a high-frequency clock source next to each device that requires it, much as designers now use bypass capacitors.

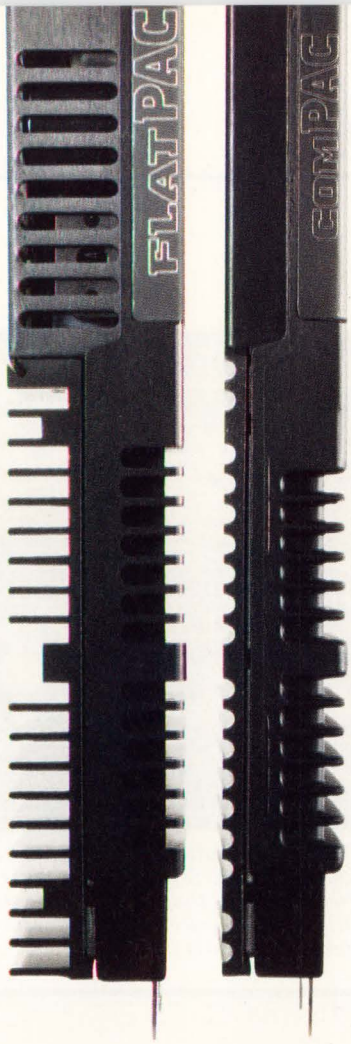
The Sbus low-frequency reference clock typically routes a 1-MHz signal to each satellite oscillator. Each ICD2031 synthesizes a synchronous high-speed clock signal from this Sbus input. The high-frequency signal thus occurs only at the point of use. This scheme keeps high-frequency traces to a minimum, which reduces the radiation of spurious high-energy harmonics.

You can use the Sbus to route the low-frequency reference throughout the system, including through the primary board and any peripheral boards. Whatever the situation, all satellite clocks are synchronized to the reference. The Sbus clock should be low enough in frequency to minimize routing problems. It does not necessarily have be set at 1 MHz, but IC Designs recommends this frequency as a good compromise value.

The ICD2031 uses a phased-locked-loop topology. The external input frequency from the Sbus reference goes into a divide-by-N block. The resulting signal becomes the reference frequency for the phase-locked loop.

The phase-locked-loop phase matches the reference signal and the synthesized signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to go faster or slower. The variable frequency eventually locks onto the reference frequency and provides a stable high-frequency output oscillation.

The parts are available in 12 versions with frequency values of 10 to 80 MHz. Prices start at $2 (100) for a 10-MHz device.



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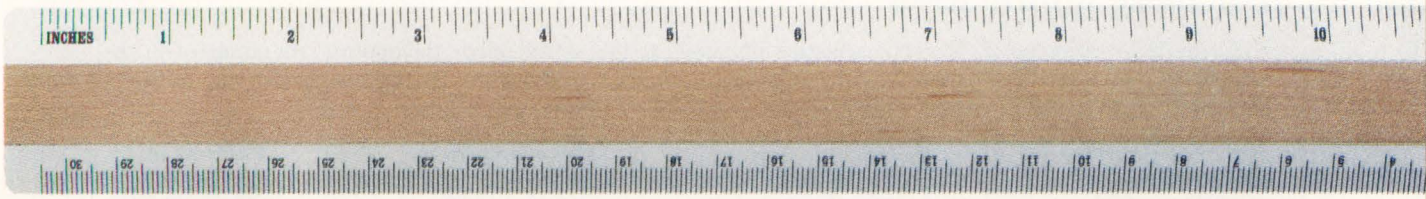

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Crystal oscillators

are somewhat larger in size than are TCOs. High-stability DCOs are more expensive than similar TCOs.

Digital compensation techniques fall into two general categories—direct and indirect. In the direct approach, a varactor diode located in a feedback loop electronically tunes the oscillator's frequency. Internal circuitry generates a compensating voltage. This voltage tracks the characteristic frequency-versus-temperature drift of the crystal and pulls the oscillator output back to nominal frequency over the specified operating range.

In the indirect approach, the oscillator runs at its natural frequency, regardless of the temperature. Digital circuitry develops the compensating output by subtracting as many oscillator pulses as is necessary to stabilize the output frequency as the temperature changes. The indirect approach can also lock a PLL to the crystal frequency and develop stabilization by digitally varying the division rate in the PLL feedback loop.

The indirect approach results in better long-term stability performance, but such design schemes are complex. Direct digital compensation schemes are less complex and, therefore, more reliable. In addition, direct approaches are compatible with oscillator circuits that have been employed in TCOs over the years.

For these reasons, Murata Erie

Featuring 3-state outputs *over the 0.5- to 40-MHz range, SQ Series oscillators from Pletronics are housed in 4-pin miniature DIPs. The devices are available with output stabilities of 0.005 to 0.1%.*

For more information . . .

For more information on the crystal oscillators discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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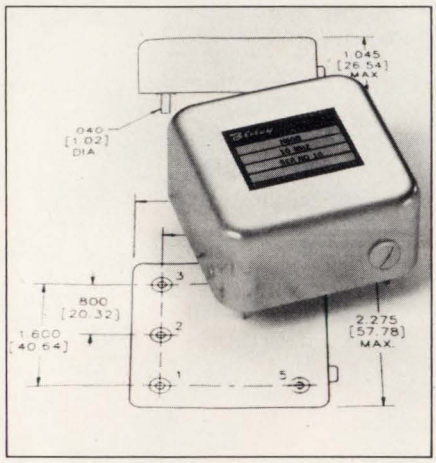
UPDATE

Crystal oscillators



When high output stability is the prime parameter, *ovenized crystal oscillators provide the necessary performance. Type N60B units from Bliley are available with outputs of 5 to 15 MHz and feature stabilities of* $\pm 5 \times 10^{-9}$ *ppm over the 0 to 50°C operating range.*

uses the direct approach in its Series DC 2210 and 2200 families of DCOs. DC 2210 devices offer outputs of 10 to 25 MHz. Frequency stabilities vary with the operating-temperature range. Model 2210 has a stability figure of ±1 ppm over the −40 to +85°C range. Model 2213 has a ±0.2 ppm stability figure over the 0 to 50°C range. Housed in a 0.79×0.79×0.45-in. package, these oscillators cost $60 to $70 (1000).

Units in the DC 2200 series ($200 (1000)) have outputs ranging from 0.1 to 22 MHz. Housed in a 2×2×0.5-in. package, these DCOs have some impressive output characteristics. Model 2201, for example, maintains the oscillator output frequency within ±0.2 ppm over the −40 to +85°C range. For less demanding applications, Model 2203 stabilizes the output frequency to within ±0.05 ppm over the 0 to 50°C operating range. EDN

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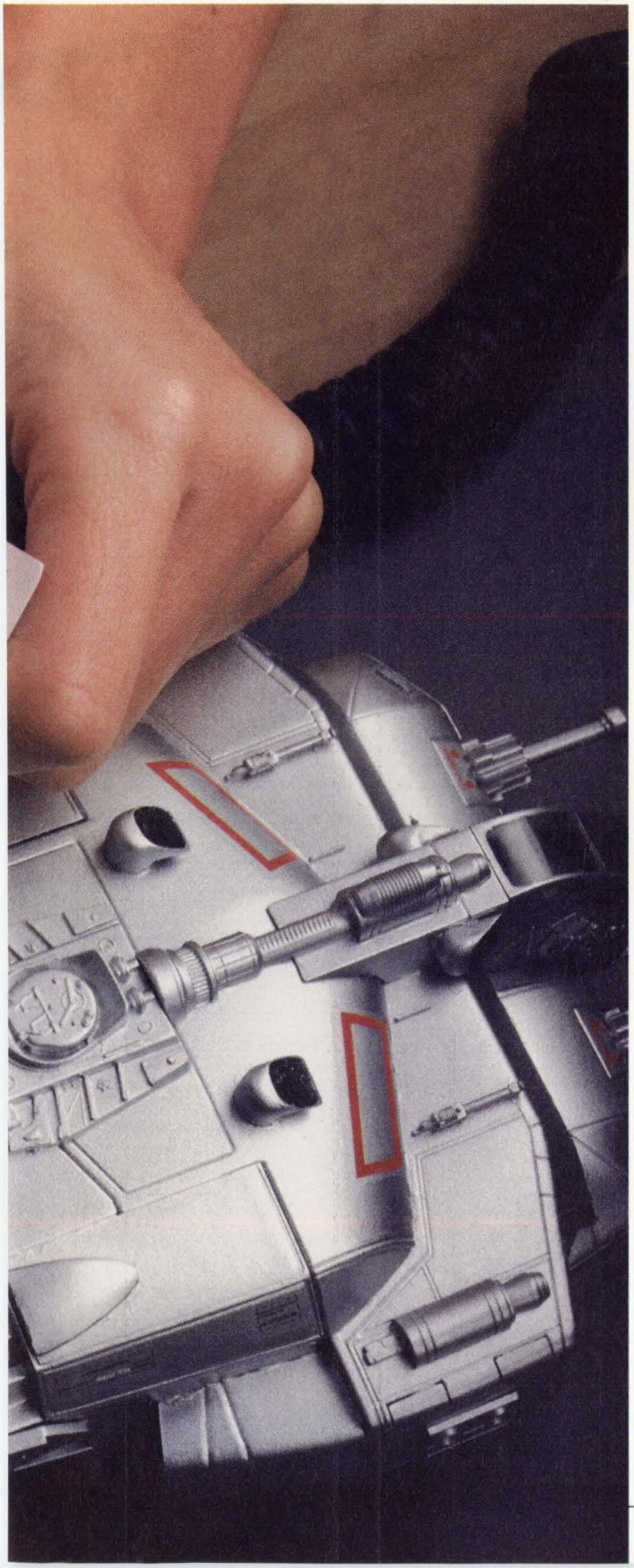

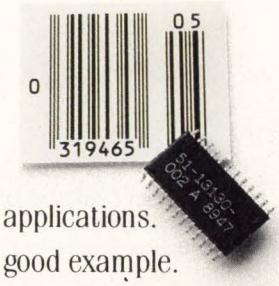

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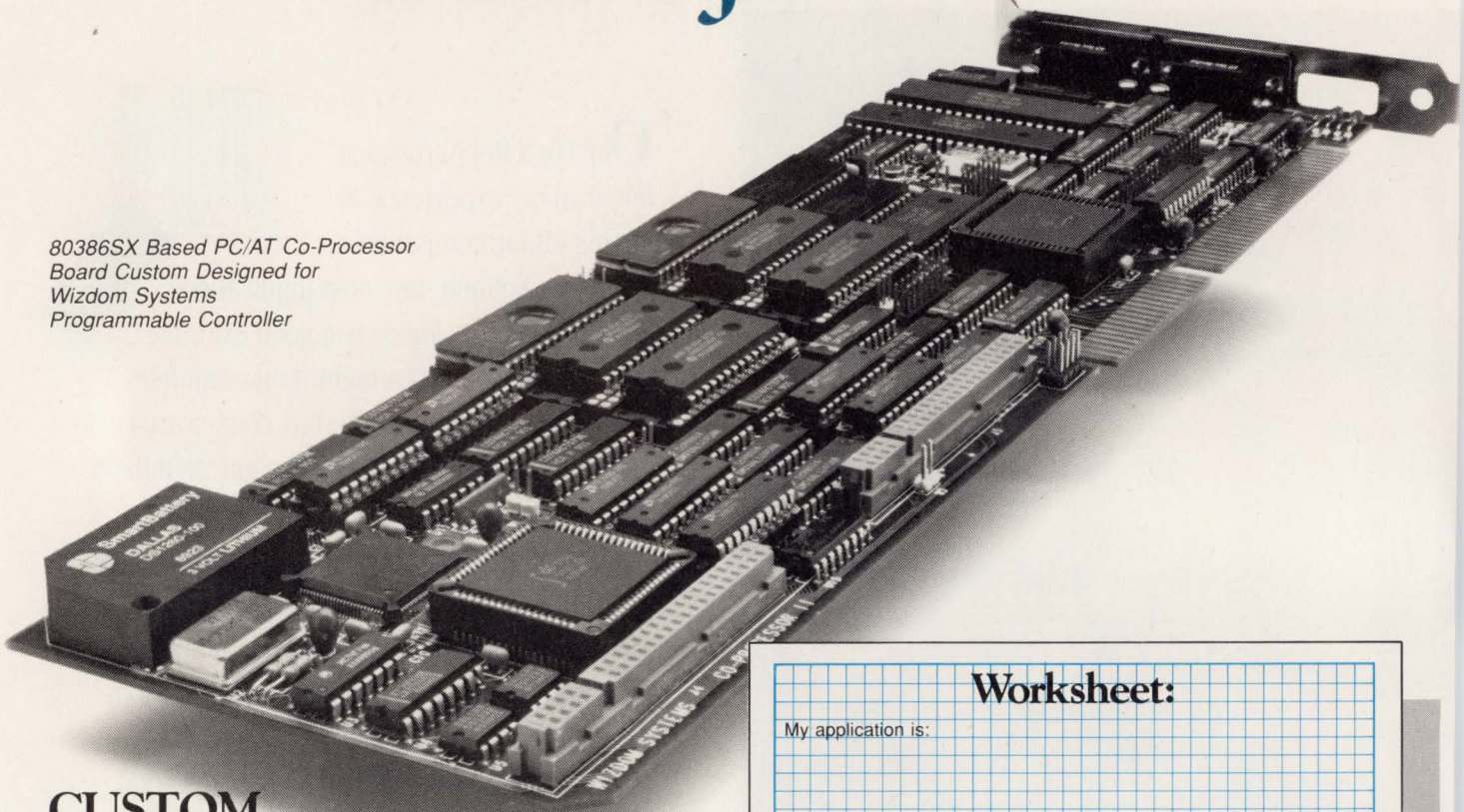

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CIRCLE NO. 49

HIGH-SPEED OP AMPs

Current feedback revs up op amps

An unbalanced input structure gives current-feedback op amps an edge in bandwidth, slew rates, and settling times.

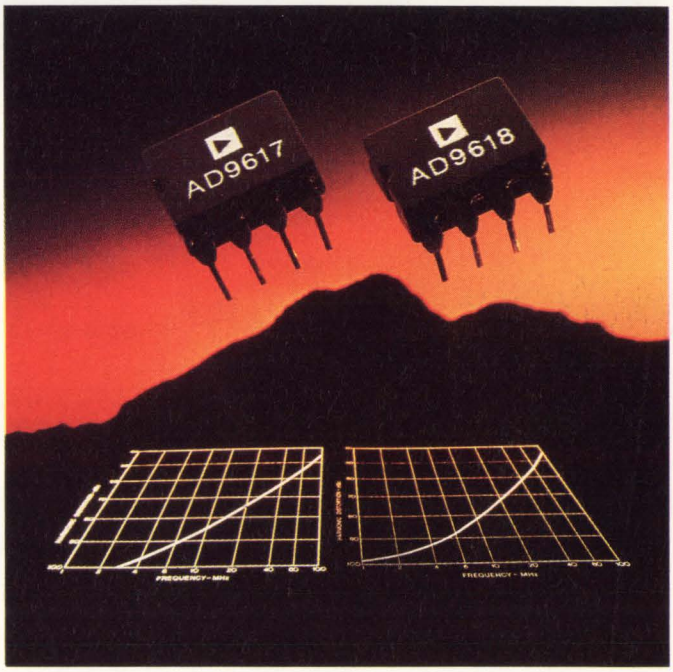
Bill Travis,
Contributing Editor

If your application—for example, video or radar processing—calls for the highest possible bandwidth or extremely speedy pulse response, chances are you'll design in one of the latest generation of current-feedback operational amplifiers. Compared with most classical voltage-feedback types, today's current-feedback op amps offer considerably faster speed parameters.

To use these amplifiers, though, you'll have to adjust your thinking about input-biasing schemes. Their unbalanced-input-impedance structure (low-Z inverting input, high-Z noninverting input) eliminates input offset current as a dc consideration in your designs. **Fig 1** gives two simplified representations of what the input structure looks like to driving sources.

In **Fig 1a,** the inverting input has a low-impedance common-base configuration, and the noninverting input has the high-impedance common-emitter architecture found in classical voltage-feedback amplifiers. The gain of a current-feedback op amp is a function of its transresistance: R_T in **Fib 1b.** This parameter is the ratio of the incremental output voltage and the incremental inverting-input current.

An analogue exists between voltage-and current-feedback amplifiers. Negative feedback in a voltage-feedback device tends to reduce the difference between the two input-terminal voltages to zero. The error, or departure from a perfect 0V difference, is a function of the open-loop voltage gain. In a current-feedback op amp, the negative feedback tends to reduce I_{IN} in **Fig 1b** to zero, and the error is a function of the amplifier's transresistance. C_T in **Fig 1b** is the transcapacitance of the current-feedback op amp. The time constant of the R_TC_T combination represents the open-loop amplifier's dominant pole.



Characterized for settling to 12-bit resolution, *the AD9617 and AD9618 current-feedback op amps from Analog Devices offer an array of distortion and differential-gain and -phase specs for communications and video applications.*

High-speed op amps

Table 1—Representative current-feedback op amps

Manufacturer	Model	Small-signal bandwidth (MHz)	Slew rate (V/μsec)	Settling time (nsec)	Package
Analog Devices	AD844	60 typ at $A_V=-1$ 33 typ at $A_V=-10$	1200 min 2000 typ	100 typ to 0.1%	8-pin DIP
	AD9617	145 min at $A_V=+3$	1100 min 1400 typ	15 max to 0.1% 23 max to 0.02%	8-pin DIP
	AD9618	130 min at $A_V=+10$	1400 min	15 max to 0.1% 23 max to 0.02%	8-pin DIP
Apex Microtechnology	WA01	80 typ at $A_V=-5$	5000 typ	20 typ to 0.1%	TO-3
Burr-Brown	OPA603	45 min at $A_V=+2$	1000 typ	50 typ to 0.1%	8-pin DIP
Comlinear	CLC207	140 min at $A_V=+20$	2000 min	27 max to 0.1% 30 max to 0.05%	TO-8
	CLC232	200 min at $A_V=+2$	2500 min	17 max to 0.1%	TO-8
	CLC402	130 min at $A_V=+2$	500 min	15 max to 0.1% 25 max to 0.01% 32 max to 0.0025%	8-pin DIP
	CLC404	150 min at $A_V=+6$	2000 min	15 max to 0.2%	8-pin DIP
	CLC410	150 min at $A_V=+2$	430 min	13 max to 0.1% 15 max to 0.05%	8-pin DIP
	CLC502	100 min at $A_V=+2$	500 min	15 max to 0.1% 25 max to 0.01%	8-pin DIP
	CLC505	115 min at $A_V=+6$	1200 min	16 max to 0.05%	8-pin DIP
	CLC520	170 min at $A_V=+10$	2200 typ	12 typ to 0.1%	14-pin DIP
Elantec	EL2030	110 typ at $A_V=+2$	1200 min 2000 typ	40 typ to 0.25%	8-pin DIP 14-pin DIP 20-pin Small-outline 20-pad LCC
	EL2070	150 min at $A_V=+2$	430 min	13 max to 0.1% 15 max to 0.05%	8-pin DIP 8-pin Small-outline
	EL2090	75 min at $A_V=+2$	600 typ	200 typ to 0.05% (internal S/H)	14-pin DIP 20-pin Small-outline
	EL2130	75 typ at $A_V=+2$	625 typ	No spec	8-pin DIP 20-pin Small-outline 20-pad LCC
Harris Semiconductor	HA-5004	100 typ at $A_V=+1$	1200 typ	50 typ to 0.1%	14-pin DIP 20-pad LCC
MS Kennedy	MSK450 (dual)	65 typ at $A_V=-1$	2000 typ	50 typ to 1% 100 typ to 0.1%	16-pin DIP 28-pin Small-outline
National Semiconductor	LH4117	100 min at $A_V=+20$	2500 typ	9 typ to 0.2%	24-pin DIP
	LH4118	200 min at $A_V=+2$	2400 min	2.5 typ (rise time)	TO-8
Precision Monolithics	OP-160	90 typ at $A_V=+1$	1000 min	75 typ to 0.1% 125 typ to 0.01%	8-pin DIP 20-pad LCC
	OP-260 (dual)	90 typ at $A_V=+1$	1000 typ	250 typ to 0.1%	8-pin DIP TO-99 16-pin Small-outline 20-pad LCC

Price (100)	Comments
$4.50	Specs include distortion and differential gain and phase at video frequencies.
$8.75	Optimized for gains from ±1 to ±40. THD characterized over frequency.
$8.75	Optimized for gains from ±5/−1 to ±100. THD characterized over frequency.
$109.35	Pin-compatible with industry-standard 3554. Supplies 400-mA output current.
$4.95	Supplies ±10V to terminated 75Ω cables.
$56	Optimized for gains from +7/−1 to ±50. Low-distortion member of CLC20X Family.
$56	Optimized for gains from ±1 to ±5. Low-distortion version of CLC231.
$14.15	Characterized for 14-bit settling. Pin-compatible with industry-standard CLC400.
$10.99	Characterized for differential gain and phase for video applications.
$9.15	Optimized for gains from ±1 to ±8. Provides disable feature for video switching.
$15.45	Pin-compatible with industry-standard CLC400. Provides user-settable output clamping.
$9.98	Supply current is user programmable.
$11.60	Provides voltage-programmable gain control.
$3.35	Characterized for differential gain and phase for HDTV video applications.
$7.70	Characterized for HDTV video specs. Provides 200-nsec disable and enable.
$6.75	Contains S/H amplifier to correct dc errors and eliminate hum in video systems.
$4.35	Lower-voltage version of EL2030. Characterized for HDTV video applications.
$5.22	Characterized for differential gain and phase for video applications.
$33	Offers precision dc input characteristics.
$107	Has high-impedance FET at inverting input.
$21.30	Provides ±100-mA output to 50Ω cable.
$4.50	Characterized for differential gain and phase for video applications.
$7.95	Consumes only 4.5 mA per amplifier.

In practice, what really dominates the amplifier's frequency response is the time constant $R_{FB}C_T$, where R_{FB} is the feedback resistor from the output to the inverting input. As with a voltage-feedback amplifier, the ratio of R_{FB} and the resistance from the driving source to the inverting terminal determines the closed-loop gain. What's different is that, in a current-feedback device, this ratio has a much smaller effect on the closed-loop bandwidth. In a voltage-feedback unit, for example, the closed-loop bandwidth is inversely proportional to this ratio; in a current-feedback device, changing the ratio from 1:1 to 10:1 doesn't even halve the bandwidth.

Table 1 lists the salient speed parameters of the latest generation of current-feedback op amps. The slew rates of these devices, for example, are many times higher than those obtainable from most voltage-feedback amplifiers. The common-base input structure of the current-feedback units is largely to blame for this disparity; in effect, the incremental input current is the charging (slew) current for the first stage, as opposed to the collector bias current in a voltage-feedback device.

A number of devices in the **table** attain a slew rate of 2000V/μsec; Analog Devices' AD844 is one that achieves that rate. The amplifier, like most of the units discussed here, lists differential gain and phase in its spec sheet. These parameters, important in video applications, are an indication of the variation in gain and phase of a device's transfer function (at a given video frequency) over a span of input voltages.

The AD844 also gives total harmonic distortion (THD = 0.005% typ) at 100 kHz. Other units in **Table 1** that specify THD are Harris Semiconductor's HA-5004, MS

High-speed op amps

Kennedy's MSK450, and Precision Monolithics' OP-160. Distortion figures for the remainder of the devices are more specific—the data sheets specify second- and third-harmonic distortion in dBc units.

Several op amps from Comlinear, the industry's pioneer in the development of current-feedback amplifiers, meet the ≥2000V/μsec slew-rate criterion. Models CLC207 and CLC232, for example, are improved versions of the company's earlier CLC200-Series devices. The CLC232's ±10V, ±100-mA output capability allows the unit to drive a double-terminated 50Ω line directly.

Other fast-slewing (≥2000V/μsec) op amps that offer hefty output drive are Burr-Brown's OPA603 (±150 mA), National Semiconductor's LH4117 (±200 mA) and LH4118 (±100 mA), and Apex Microtechnology's WA01. The WA01, packaged in a TO-3 metal can, is the fastest slewing (5000V/μsec) and highest power device (±400 mA) of the units in **Table 1.**

Fast slewing is, of course, desirable in any application that requires quick level-to-level changes. One such application is output amplification (or current-to-voltage conversion) for a D/A converter. When high precision is required, however, speedy slewing alone is not enough. The amplifier's output must settle to within a prescribed error band in an acceptable interval.

Most of the units in **Table 1** specify settling time to an error band of ±0.1% or greater. You can't use these devices, with any confidence, in D/A-conversion applications entailing a resolution of 12 bits or greater. One LSB (least significant bit) at 12 bits is about 0.024% of the full-scale output.

To design an amplifier that settles in a predictable manner to within ±0.02% is not an easy task. You have to consider not only pulse-related incremental parameters such as overshoot and ringing, but also the thermal characteristics of the amplifier. Heat from the output stage, coupled back to the input stages, can cause dc drifts that result in a "thermal tail" at the output. Careful and clever isothermal design is critical when creating precise-settling amplifiers.

Two units from Analog Devices specify settling to within a ±0.02% error band. The AD9617 and AD9618 settle in 23 nsec max. Their unequivocal second- and third-harmonic distortion specs, as well as their differential-gain and -phase specs, qualify them for a broad range of data-conversion and video-processing applications.

Two recent units specify settling to within ±0.01%—approximately ½ LSB at 12 bits. Precision Monolithics' OP-160 settles to this level in 125 nsec typ. Another unit suitable for 12-bit processing is Comlinear's CLC502, which specs 25-nsec max settling time to ±0.01%. A bonus with the CLC502 is a clamping feature, which allows you to clamp the output swing to predetermined levels.

Only one current-feedback op amp has features that qualify it for signal processing at a resolution greater than 12 bits. The CLC402 guarantees 32-nsec max settling time to within a ±0.0025% error band. This performance qualifies the device for use in 14-bit data-conversion systems. Specs for second- and third-harmonic distortion, as well as differential gain and phase, round out the CLC402's suitability for high-speed signal-processing systems.

Several of the devices covered in **Table 1** furnish incremental improvements over earlier models; others offer novel new features. The Elantec Model EL2030's 2000V/μsec typical slew rate is quadruple that of the earlier EL2020. In addition, the EL2030's data sheet adds the valuable video parameters differential gain and phase. A lower voltage version of the ±15V EL2030, Model EL2130, operates from ±5V supplies with about a 50% compromise in speed.

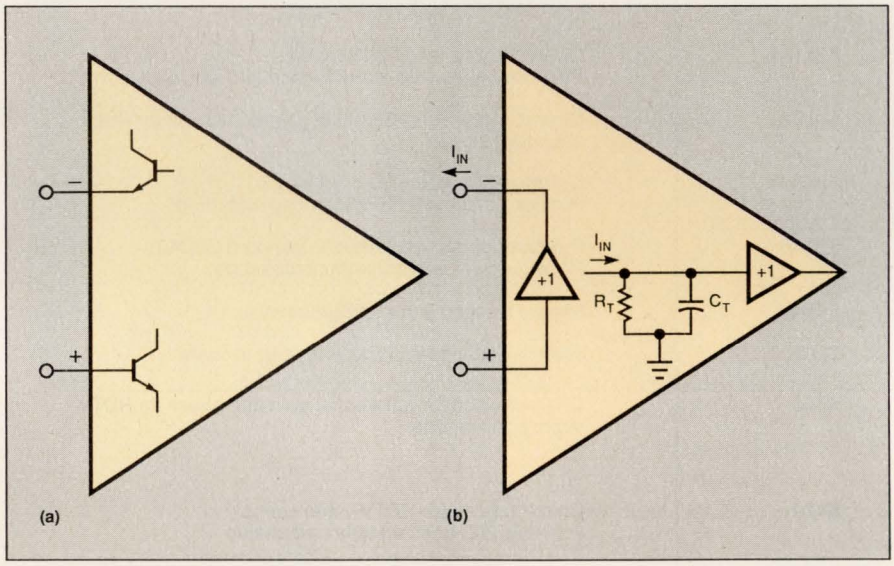
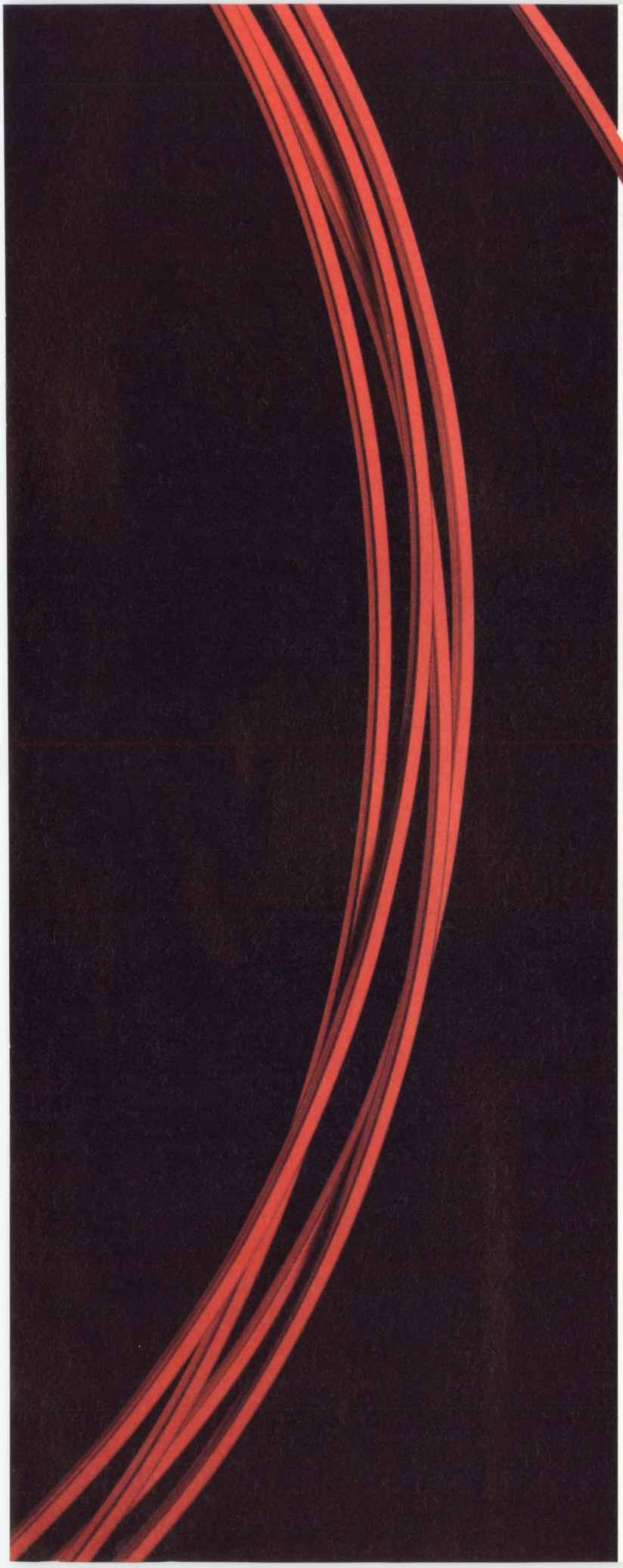
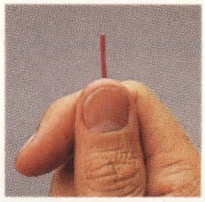


Fig 1—Unbalanced inputs characterize current-feedback op amps. *The noninverting input* ***(a)*** *has a high-impedance, common-emitter configuration; the inverting input has a low-impedance, common-base structure. The equivalent circuit in* ***b*** *shows the transresistance R_T and the transcapacitance C_T that determine the amplifier's transfer function.*





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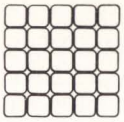

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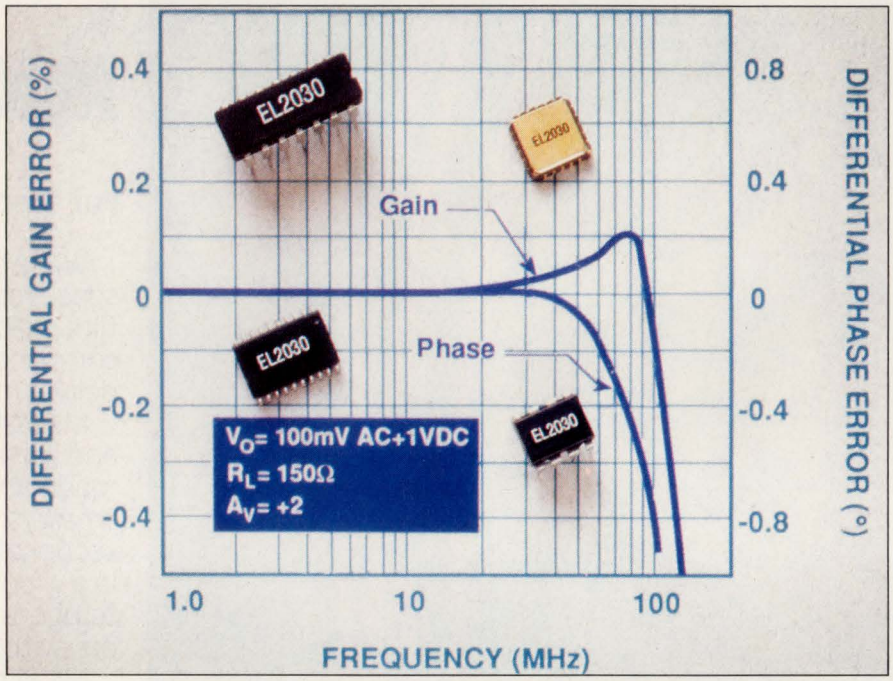
TECHNOLOGY UPDATE

High-speed op amps

You might consider that it's original to offer dual current-feedback op amps. MS Kennedy's MSK450 and Precision Monolithics' OP-260 both offer two independent op amps in 16- and 8-pin DIPs, respectively. A notable feature of the MSK450 is its low offset voltage—50μV typ. This unit and Analog Devices' AD844 (also 50 μV typ) are the only ones to offer sub-100-μV input offset-voltage specs; the others spec offsets from about 0.5 mV to several tens of millivolts.

The Model OP-260 dual device offers laudable high-speed performance in light of its low operating current. Drawing only 4.5-mA supply current per amplifier section, the device slews at 1000V/μsec typ. An obvious advantage of using dual op amps such as the MSK450 and the OP-260 is the inherent match in ac characteristics between the two sections.



Low differential-gain and -phase errors *characterize Elantec's EL2030. These figures are 0.05% and 0.02°, respectively, at 30-MHz HDTV frequencies and 0.01% and 0.01° for lower NTSC and PAL frequencies.*

Three of Comlinear's recent current-feedback amplifiers incorporate some bells and whistles. The CLC410 has a disable pin that allows you to turn the amplifier on and off in 100 and 200 nsec, respectively. This feature makes the device suitable for such applications as video switching and distribution.

Model CLC505 allows you to program its supply current over a 10:1 range by use of a single external resistor. As always, speed performance is a function of supply current. For example, the device slews at 800V/μsec at 1-mA supply current and 1700V/μsec at 9 mA. Voltage-controlled gain is the claim to fame

For more information . . .

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UPDATE

High-speed op amps

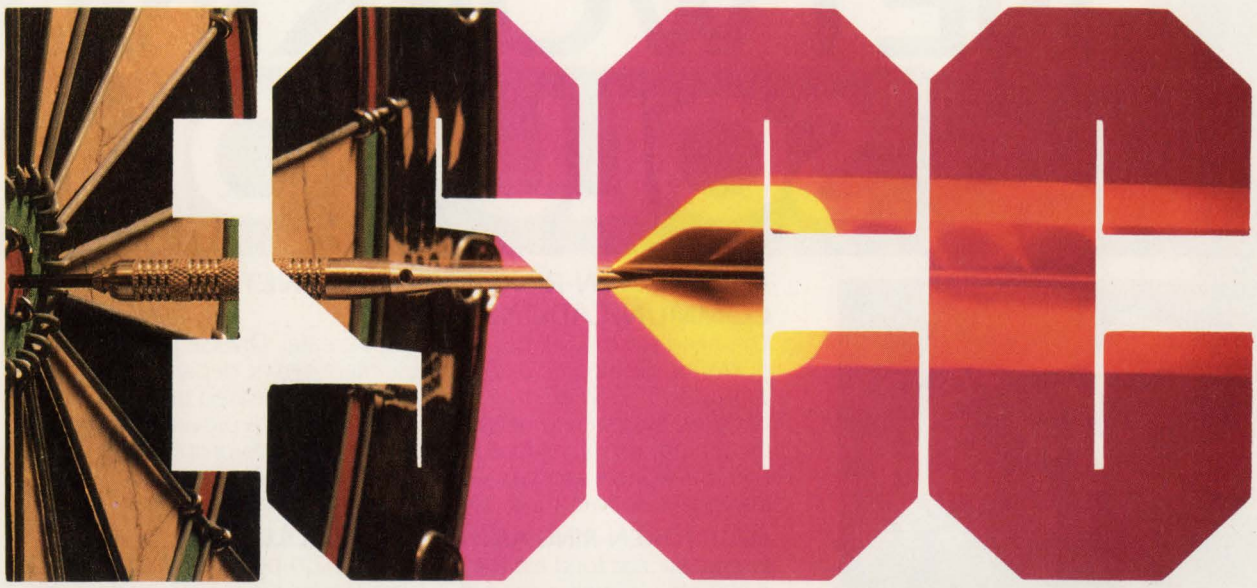
of Comlinear's CLC520. A voltage applied to its gain-control input varies the gain over a >40-dB range. Thanks to the gain control's 100-MHz bandwidth, you can use the amplifier in wideband AGC applications.

Like Comlinear's CLC410, Elantec's pin- and spec-compatible EL2070 has a disable/enable feature. Intended for video applications, the Model EL2090 contains a S/H amplifier for dc restoration. You can use the S/H section to null the dc offset of a video system. Once per video line (during the back-porch interval), the S/H amplifier compares the output level of the amplifier against a dc-clamp reference at the S/H input. The S/H amplifier stores the correction voltage needed to offset the back porch to the clamp level.

The amplifiers discussed here use both monolithic and multichip-hybrid construction. The monolithic devices owe their existence to the development of high-speed complementary-bipolar processes, which make it possible to produce fully vertical pnp transistors whose speed is almost comparable to that of npn devices. As this semiconductor process evolves, you can expect many more, and much faster, current-feedback amplifiers to appear in the years to come. As an example, Linear Technology Corp is joining the current-feedback fray with its LT1223, which is slated for sampling this month. Though its specs were too tentative at the time of writing to allow including the device in **Table 1,** it's projected to slew at approximately 1000V/μsec and settle to within ±0.1% in about 75 nsec. EDN

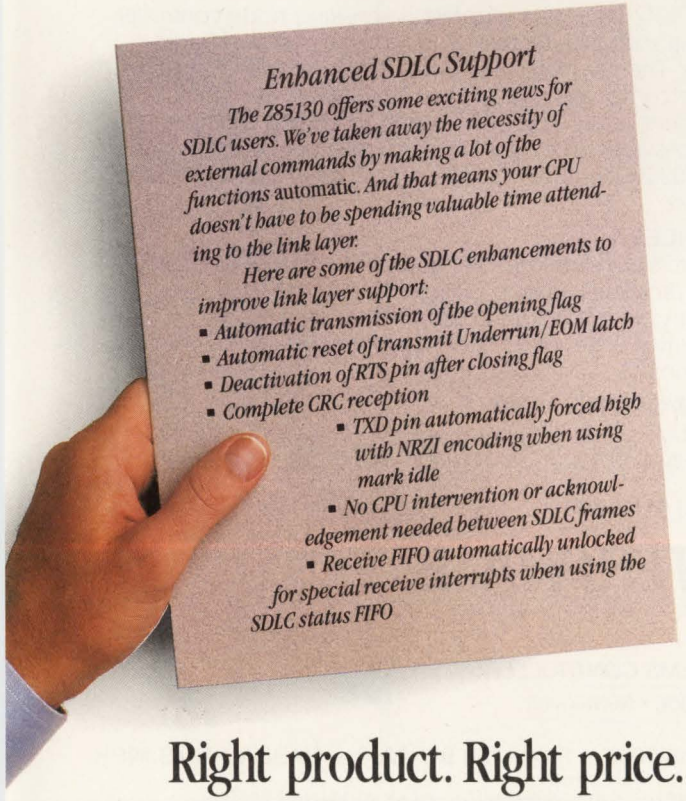
Article Interest Quotient
(Circle One)
High 500 Medium 501 Low 502

Z I L O G



The *ENHANCED SCC.* Smoother operation. Super CPU performance. Same socket.

Introducing Zilog's Z85130,™ the enhanced serial communication controller (ESCC) that significantly reduces your CPU overhead, gives you new deep FIFOs, and offers plenty of SDLC support for your 16 and 20 MHz applications. *And* it's pin and function compatible to the Zilog CMOS and NMOS SCCs you may already be using.



Deep FIFOs improve CPU performance.

The ESCC gives you a 4-byte deep transmit FIFO, an 8-byte deep receive FIFO, with programmable FIFO interrupt and a DMA request level. Since you're manipulating the data in byte strings, you don't have to attend to it as often. This, combined with other features that simplify the CPU interface, means a lot better utilization of CPU horsepower.

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The low-power CMOS ESCC is designed for 16 and 20 MHz CPUs. It also gives you improved databus timing, 2 Mb/S with DPLL and faster interrupt response. DMA timing is the same for transmit and receive. And you can now read WR3, 4, 5 and 10.

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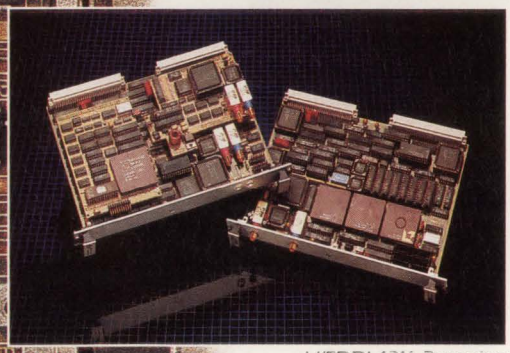
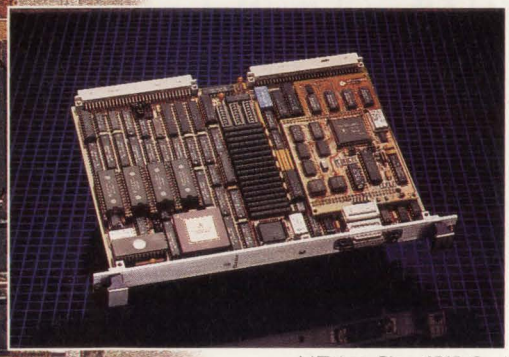
CIRCLE NO. 52

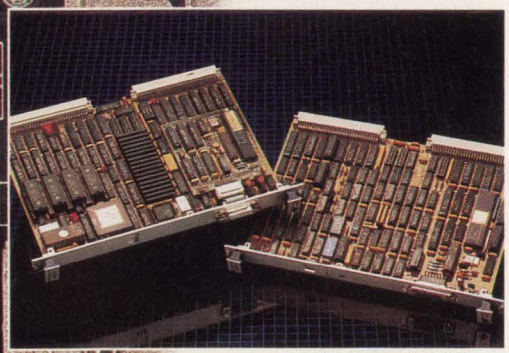
NETWORKING SOLUTIONS



V/FDDI 4211 Peregrine
V/FDDI 3211 Falcon



V/Token-Ring 4212 Owl



V/Ethernet 4207 Eagle
V/Ethernet 3207 Hawk

FDDI, TOKEN-RING AND ETHERNET COMMUNICATIONS

The need to network has never been greater. Diverse processing platforms, distributed architectures, client-server, departmental and workgroup environments all contribute to increased demands on the network. System and network designers need a proven source of technology solutions for the wide range of networking and communication application problems they face. Interphase delivers those solutions.

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Interphase has long led the industry in high-performance VMEbus peripheral controllers, and that same leadership is now evident in networking node controllers. Interphase has FDDI, Token-Ring and Ethernet solutions for virtually any VMEbus system application challenge.

PROVEN FDDI SPEED AND INTELLIGENCE

Interphase's FDDI 100 Mb/s offerings are a logical choice for the industry. The V/FDDI 3211 Falcon received *UnixWorld* magazine's Product of the Year designation and was the industry's first 6U VMEbus FDDI solution. Interphase's newest FDDI product is the V/FDDI 4211 Peregrine, a RISC-based high-performance node controller capable of link level operation or on-board protocol processing. The Peregrine provides single or dual attach configurations, with SMT (Station Management Software) running on-board, all in one 6U VME slot.

TOKEN-RING RESULTS

The V/Token-Ring 4212 Owl is an ultrafast Token-Ring node controller based on the partitioned architecture of Interphase's proven Eagle class of controllers. The Owl facilitates connectivity of UNIX® systems, workstations, supercomputers or any other VMEbus system into an IBM® environment using IEEE 802.5 Token-Ring. This multiple processor design provides an elegant queued interface to the system supporting IEEE 802.2 LLC, and a flexible 4 or 16 Mbit interface to the Token-Ring network.

ETHERNET CHOICES

Interphase also offers two Ethernet design options. The V/Ethernet 4207 Eagle 32-bit protocol platform is the high-performance standard for the industry, and offers on-board TCP/IP support. The V/Ethernet 3207 Hawk is designed specifically for cost-sensitive VMEbus applications.

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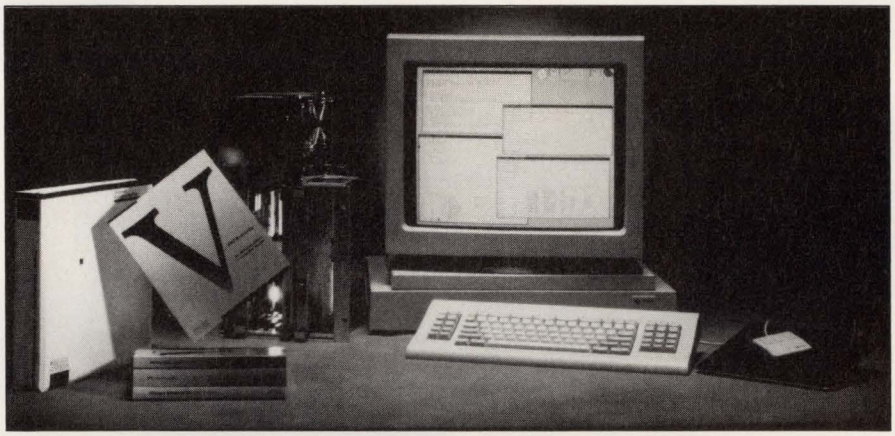
CIRCLE NO. 53

Real-time operating system links Unix with transparent support for standard networks

Real-time system software from Ready Systems Corp, called VRTXvelocity 2.3, gives users access to the broad range of powerful software-development tools for Unix. Support for network standards such as TCP/IP (transmission control protocol/internet protocol) and NFS (network file system) transparently interfaces VRTX-based target hardware to Unix-based Sun workstations. The network capabilities simplify the development of 680X0-based targets and are suitable for use in distributed real-time systems.



Network management services included in this real-time system software allow you to control real-time targets with standard Unix commands from Sun workstations. *VRTXvelocity 2.3 integrates the Unix and target file systems using NFS and can interface with other network standards such as TCP/IP and BSD Sockets.*

The real-time multitasking kernel, VRTX32, forms the basis of the software product. VRTX32 includes features such as pre-emptive priority-based task scheduling, interprocess communications, synchronization facilities, and semaphores. The target-based kernel guarantees a maximum interrupt latency of 10 μsecs—one wait state on a 25-MHz 68020 μP. The kernel also implements all system services such as queues, mailboxes, and global event flags at the kernel level rather than depending solely on semaphores for task synchronization.

The real-time operating system, VRTX/OS, adds features such as a file-management system and serial I/O to the VRTX32 kernel. Real-time targets, such as a data-acquisition system, increasingly demand a fast full-featured file system. This operating system also includes a portable re-entrant C runtime library, loosely coupled multiprocessor support, and support for standard networks.

The software's network-management services transparently integrate VRTX/OS with a Unix host. Release 2.3 includes support for Sun workstations, and the company plans to offer packages for other Unix systems. In addition, Ready plans to offer versions for X-Windows in the future, making Ready able to port the software easily among Unix systems.

The network management services include TCP/IP—an industry-standard full-duplex network communications protocol. The software also supports the BSD Sockets programming interface, and the user can specify stream sockets or datagram sockets. A set of library routines support RPC (remote procedure calls) and XDR (external data representation). Finally, the system incorporates Sun NFS and the Telnet virtual terminal facility.

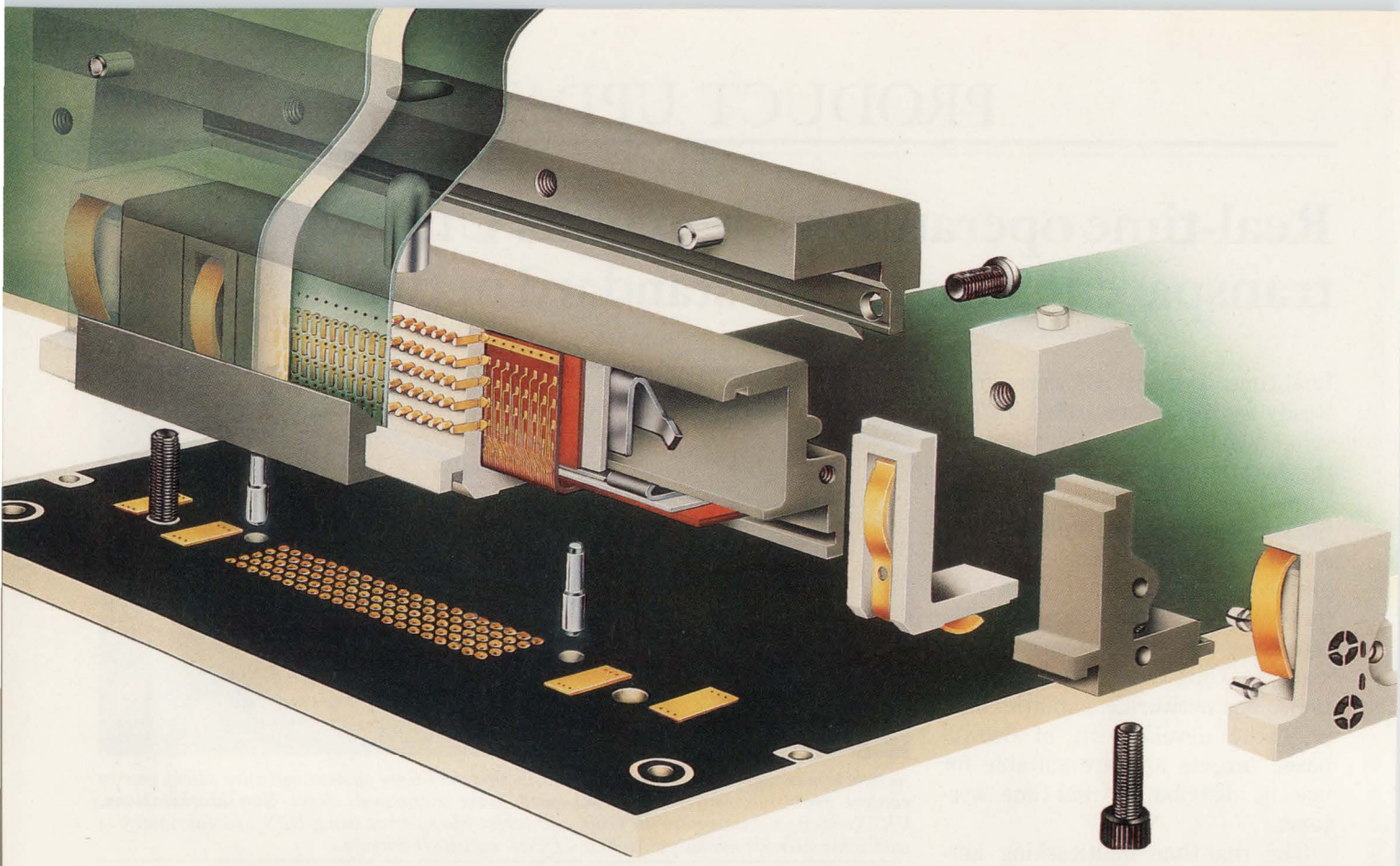
Users can work with the Sun host and the VRTX/OS target via the SUN display, keyboard, and mouse. For example, one window on the screen might include a Sun-based text editor for modifying source code. A second window might host a target-based debug session that the workstation views via the Telnet network terminal-emulation facility. This feature allows designers to swap seamlessly between software development, compile, test, and debug.

The user can view the file system of the Sun host and the target, and both appear as part of the standard NFS. The target software includes a command interpreter that allows you to control the target with standard Unix commands. Code compiled on the Unix system moves over the network to the target at a rate much faster than serial communications would allow.

The software system runs with a number of popular 680X0 boards from Force, Heurikon, and Motorola. The vendor supports the boards in board-support packages that include full documentation for using VRTXvelocity with a particular target. The package costs $17,500, and the company offers discounts for multiple or site licenses.—***Maury Wright***

Ready Systems Corp, Box 60217, Sunnyvale, CA 94086. Phone (800) 228-1249; in CA, (408) 736-2600. FAX (408) 736-3400.

Circle No. 730



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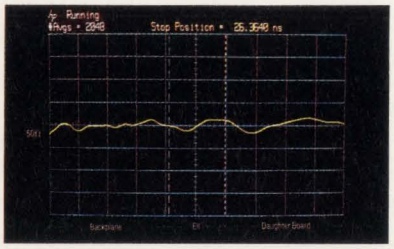

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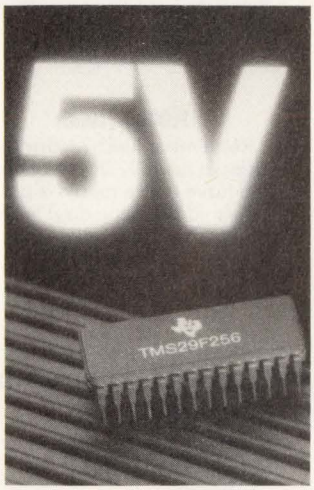
READERS' CHOICE

Of all the new products covered in EDN's **May 24, 1990,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, use EDN's Express Request service, or refer to the indicated pages in our **May 24, 1990,** issue.



5V Flash EEPROM ▲

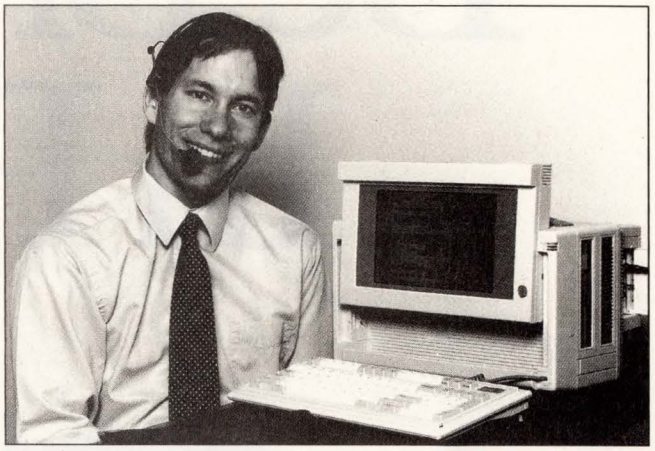
The TMS29F256 flash EEPROM combines the electrical alterability of byte-erasable EEPROMs with the density and low cost of EPROMs. This 256K-bit device uses a single 5V power supply for program, erasure, and read options. Pinout is compatible with standard 256k-bit devices (pg 198).
Texas Instruments.
Circle No. 802

CAE Menu System

The Intelligent Menu System software package lets you control all of the OrCAD CAE tools from within a system of pop-up menus. The system can automatically generate long DOS command strings and lets you edit or repeat the strings with a mouse. The system is hardware independent and uses no RAM working space. It also adds new facilities such as a file viewer, an editor, a directory manager, and a stuff-filer maker, which automates the assignment of package modules to schematic symbols (pg 229).
Velotec.
Circle No. 803

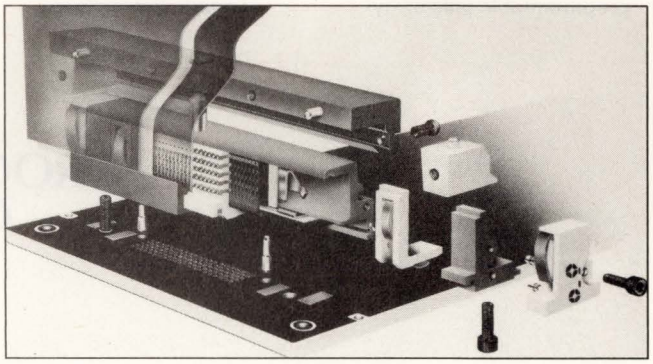
PC Diagnostic Software

QAPlus, a diagnostic software package, tests all of the subsystems usually found on IBM PC-compatible computers and PS/2 series machines. The menu-driven package provides both pass/fail information and more detailed data, including performance levels. It can log test results to a hard-copy output device or to a disk file (pg 236).
DiagSoft Inc.
Circle No. 804



Voice-Recognition System ▲

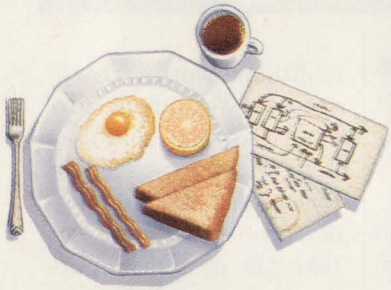
Creating text at 30 to 40 wpm, the DragonDictate system recognizes words that are less than 5 sec in duration and separated from the next word by a 0.25-sec pause. The software contains 25,000 commonly used words and lets you define editing commands and 5000 additional words. Using acoustic word models to identify sounds and statistical language models to establish the likelihood of a word in a given context, the system can update information on your speech pattern (pg 105).
Dragon Systems Inc.
Circle No. 805



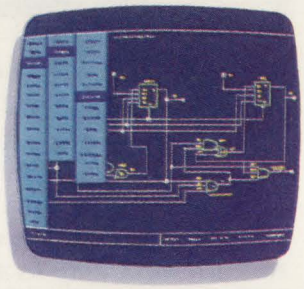
Impedance-Matched ▲ Connector

Supplying a high-density array of controlled-impedance signal lines and power lines in a modular assembly, this electronically invisible interconnect connector handles signals with rise times as fast as 35psec. The surface-mount connector supplies as many as 80 signal lines/in. of connector length. The device's flexible circuit has a characteristic impedance of 50Ω (±10%) and supplies a ground plane that reduces crosstalk to −40 dB for 500-mV, 100-MHz signals with a 900-psec rise time (pg 106).
Augat Inc.
Circle No. 806

Be Brilliant At In Productio

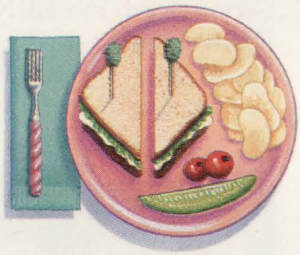


7:05 am: Breakfast
Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am: Design
You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.

11:00 am: Place & Route
You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm: Lunch
Remember lunch? Normal people actually *stop working* and have a nice meal—right in the middle of the day! With Actel's logic solution, this could become a habit.

ACTEL FIELD PROGRAMMABLE GATE ARRAYS

They're a feast for your imagination.

Actel's ACT™ 1 arrays bring you a completely new approach to logic integration. Not just another brand of EPLD, PAL®, or LCA™ chips. But true, high density, desktop configurable, channeled gate arrays.

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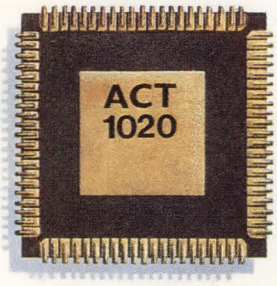
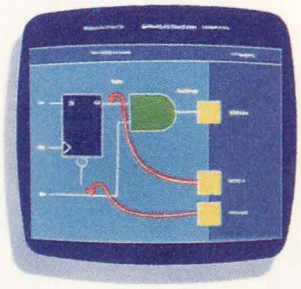
And do it in hours instead of weeks. Even between meals.

How? With features like 85% gate utilization. Guaranteed. Plus 100% automatic

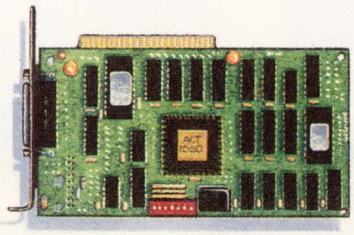
Breakfast And n By Dinner.



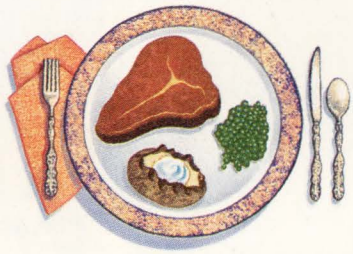
1:15 pm: Program
You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a *very* quick coffee break while your design becomes a reality.



1:25 pm: Test
You do a complete, real-time performance check, with built-in test circuits that provide 100% observability of all on-chip functions. *Without* generating any test vectors.



4:00 pm: Production
Your pride and joy is designed, created, tested, and off to the boys in Production. And you're finished *way* ahead of schedule! Better think of something to do until 5:00.



6:00 pm: Dinner
Remember dinner? Normal people actually *go home* and eat with their families. On your way, start thinking about how Actel's logic solution can help you be brilliant tomorrow.

placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most tedious part of the job by hand. And design verification is quick and easy, with on-chip Actionprobes™ that work with your logic analyzer to provide 100% observability of internal logic signals. Guaranteed.

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CIRCLE NO. 56

Fast-turnaround ASICs

A disadvantage of mask-programmed ASICs is the lag between finishing the design and getting back the prototypes. Vendors are streamlining fabrication to get your ASICs in your hand before your prototyping schedule clock strikes twelve.

Michael C Markowitz, Associate Editor

As an ASIC designer, you're stuck. Marketing people give you increasingly complex specifications to design and implement in less time. Often, these specs are either cast in Jello or incomplete. And with the perception of the importance of trade-show product demonstrations and introductions, you've often got an immutable deadline. Worse, if your first cut at an ASIC has an error, then you must find the mistake and repeat the fabrication cycle. Don't tell your marketing folks—they'll likely try to steal the time for product definition—but help is on the way. ASIC vendors are trying to give you more design time by shrinking their fabrication cycles.

ASICs come in many shapes and sizes. Obviously, your implementation choice depends on cost, but cost depends on several other factors: design density; complexity; performance; volume. PLDs and FPGAs, in all their various forms, are most suitable for lower-density and lower-volume applications. Their programmability allows you to convert your schematic to working silicon in a matter of minutes and to make design changes in hours.

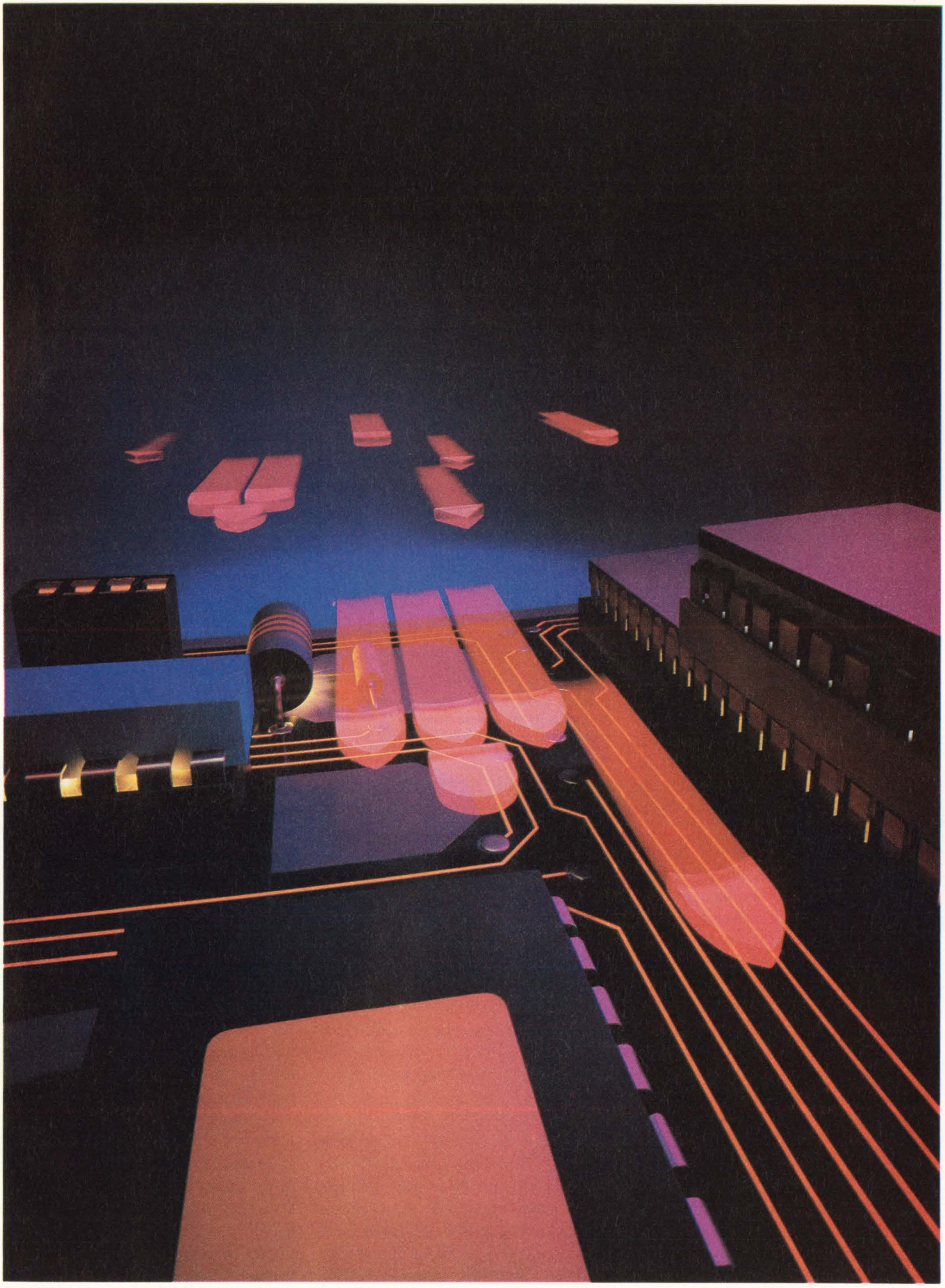
But if your design is dense and you expect high-volume production, you'll likely choose a masked-programmed ASIC. Array-based masked-programmed ASICs offer a balance between density and performance for high-volume designs. Their preprocessing to the interconnect stage reduces fabrication time once you sign off on the design. All-level ASICs, such as cell-based and full-custom devices, trade higher densities and lower production costs for slower turnaround and higher prototyping costs.

Array-based ASIC vendors have cut their fabrication cycles by more than half. Five years ago, eight- to 12-week cycles were the norm. Unfortunately, it is misleading to consider these times as leadtimes to good prototypes. Too often you'll need to revise your first pass and repeat the fabrication cycle.

Because of the shrinking product life cycles and the potential for having to iterate the design, ASIC vendors' efforts to reduce turnaround time are crucial. Today, most vendors quote a three- to five- week fabrication cycle for an array-based ASIC. But if the vendor really likes you (or more accurately, your business), or you're willing to pay an NRE premium of 50 to 100%, you may be able to shrink the turnaround to as little as seven days. Direct-write, on-site fabrication processes can cut the turnaround time to eight hours.

Buy a fabrication clean room

Although direct-write ASICs can give you silicon quickly, owning the capability isn't cheap. Lasarray sells a transportable, 750-ft^2 3-mod-



Thanks to streamlined fabrication processes, ASIC prototypes are now arriving at their design destinations sooner. (Photo courtesy NCR)

Incomplete or capricious specifications stretch design cycles—although they don't usually affect your deadlines.

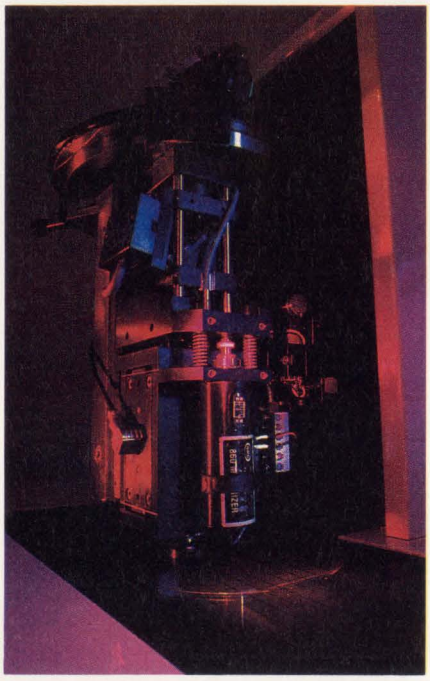
ule ASIC facility for $4,200,000. This module provides all the equipment and tools you need to design and fabricate prototype and short-run production ASICs. If you've already got processing equipment and a clean room, Lasarray will sell you the Direct-Write Laser Pattern Generator (DWL-I) for $750,000.

However, if you think getting $4,200,000 from the corporate bean counters is unlikely, or if the corporate parking lot is a bit crowded for a 750-ft^2 module, Lasarray will provide an ASIC fabrication service. Typical NRE charges are between $12,000 and $15,000 for net-listed designs containing as many as 10,000 gate equivalents.

The direct-write system also permits a sort of silicon breadboarding. The DWL-I writes as many as 16 different patterns to a single wafer. As a result, you can build 16 different variations of the same design. Alternatively, groups designing multiple ASICs can prototype them concurrently.

Chip Express also uses a direct-write laser to program prototype arrays. Typically, vendors put all the transistors on base wafers without connecting any of the transistors. The vendors then put these preprocessed base wafers in stock. When you place an order, the ASIC vendor connects the transistors to customize the bases with your application. Chip Express stocks fully processed wafers that it customizes using a double-metal disconnect approach. The advantage to this approach over other direct-write methods, according to Adi Gamon, the company's vice president, is that there is no performance degradation, and the real-estate penalty is typically less than 10%.

The vendor has software that can output data in three formats. The cut-list output directs the laser to cut the appropriate metal lines to implement your logic. To keep costs down on lower-utilization, small-volume production runs, the software can keep the necessary interconnects on one layer and produce data to generate one photolithographic mask. Finally, for high-utilization, high-volume production runs, the software can produce the data for double-metal interconnect on four masks in GDS II format or CIF (Cal-Tech Intermediate Format).



A direct-write laser pattern generator customizes a wafer with as many as 16 different ASIC patterns. (Photo courtesy Lasarray)

Robots do the dirty work

Another laser-based alternative is the QT-GA from Lasa Industries. This $3,000,000 21-ft^2 system contains five chambers to process bonded, pin-grid-array-packaged uncommitted CMOS- or bipolar-array die. The QT-GA interprets GDS II-format layout data. The system commands a robot, inside the module, to move the arrays between processing chambers. Within these chambers, the QT-GA deposits a dielectric between two layers of directly written metal interconnect, etches vias, and seals the package.

One warning about the direct-write approaches: when quoting turnaround time, vendors generally don't include the time it takes to generate test programs. These times may not be inconsequential. In addition, direct-write approaches often don't include packaging times, though the QT-GA system's turnaround does include package-sealing time.

An example of the approximate times through the various stages of a fast-turnaround masked-programmed-ASIC line could highlight the steps. According to Rob Walker, vice president of technical marketing at LSI Logic, mask making takes one day, metallizing the gate array takes two days, wafer sorting and final testing each take about a day, and packaging takes about two days. LSI allows a day or two for miscellaneous holdups. Direct-write ASICs eliminate only mask making from this schedule.

Of course, small direct-write fabrication lines dedicated to prototyping only one ASIC don't have queues at every fabrication stage. As a result, process steps that might take days in a merchant fabrication facility take only hours in your direct-write ASIC facility.

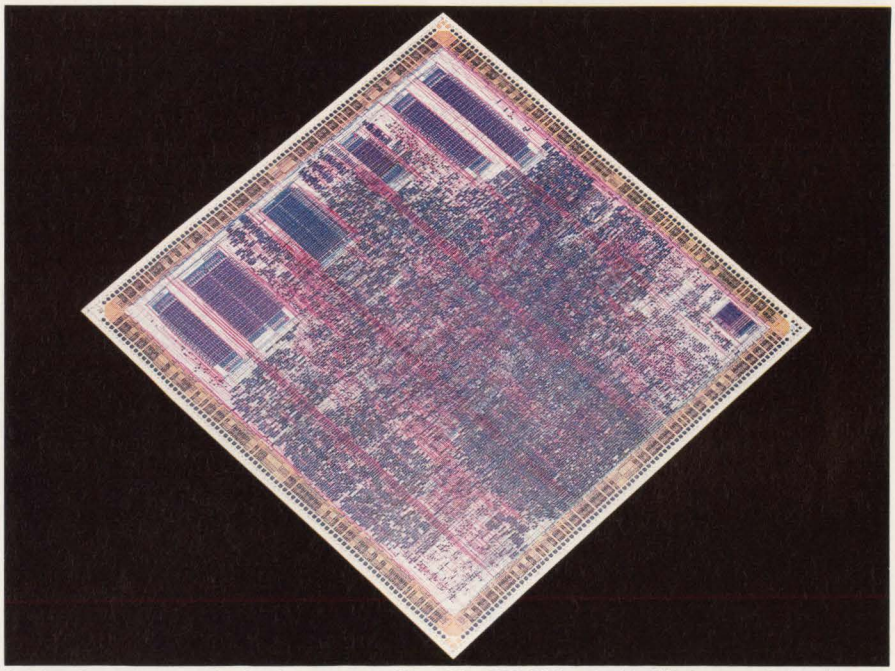
Evaluating ASIC prototypes and moving them into production is just as important as fast prototyping. More than one ASIC vendor relates that they've rushed ASICs through their fabrication line—at great expense to the customer—and found weeks later that the customer hadn't yet evaluated the ASICs. On the other hand, if after evaluating

your ASIC you're ready to move into production, you don't want to find any bottlenecks. The direct-write approaches claim to use wafers from other standard-processing ASIC vendors to facilitate shifting the design to production. Make sure you find out whose wafers they use and then talk to the ASIC vendor about moving into production after prototype acceptance.

Direct-write approaches aren't limited to array-based ASICs. US2 builds all-level direct-write ASICs. Unlike most other all-level ASIC vendors, US2 has no minimum order and, like Lasarray, can mix designs on a wafer. After evaluating your prototypes, if you need high-volume production quantities, US2 has agreements with other semiconductor vendors to transfer your design into production.

When you are fighting the clock to finish a design, the biggest problem is remembering that the design is more than just a collection of appropriately wired gates. Resist the temptation to let up after you've turned your net list over to the ASIC vendor. You still have to ensure that a test program is ready to evaluate the ASICs when they leave the fabrication plant.

An approach developed by Crosscheck Technology (San Jose, CA (408) 432-9200) overlays your design on a matrix of testability transistors. This approach is currently licensed to LSI Logic, Harris Semiconductor, Fujitsu Microelectronics, and an internal IC group within Raytheon Corp (Andover, MA (508) 860-3412). The test matrix demands that IC vendors create new bases for their ASICs. Although none of the vendors currently offer devices with the Crosscheck test matrix, LSI Logic has proven the validity of the approach with working silicon and presented a paper on the results at this year's Custom Integrated Circuit Conference in Boston. Michael Carroll, Crosscheck's vice president of marketing, expects to see commercial devices available early next year.



Getting fast turnaround of a large array, like this 150,000-gate Toshiba array, takes longer than smaller arrays because mask making and testing take longer.

Software smooths development

When the pressure is on, VLSI Technology can shave a week off their normal three-week gate-array turnaround time. The bottleneck has been test-program development. Its Test Assistant is a CAE tool whose purpose is to improve an ASIC's testability. The software inserts isolation multiplexers and control circuitry to allow you to test functional blocks independent of peripheral logic. After software processing, your design contains all the necessary control signals. The software even updates your schematics.

After adding the isolation logic to all the functional blocks in your design, the software creates a coherent set of test vectors to verify the logic. In addition to improving testability using isolation logic, the Test Assistant can add built-in self test (BIST) circuitry, generate the control patterns to initialize the logic, run the test, and evaluate the results. As a result of this test software, your circuit becomes easier to observe and to control, and is therefore easier to test.

If performance constraints demand that you control where the software inserts isolation or BIST logic, you can intervene while the software works. You can determine which pins the software multiplexes with test signals, which isolation circuits it uses, and how it connects BIST blocks.

Another ASIC vendor stressing the testability of your design is Integrated Logic Systems Inc (ILSI). Integrated Testability is its combination of a scan-testable array ar-

Making sure the test program is waiting for your ASICs at the end of their fabrication cycle is crucial for quick delivery of your prototypes.

Table 1—Representative fast-turnaround ASIC vendors

Company name	Fast turn-around (days)	Normal turn-around (days)	PC-or workstation-based libraries	Available technologies	Usable gates	Delay through 2-input NAND with 2 mm metal (psec)	Typical NRE (from net list)	Typical piece-part price (5000 qty)
AMCC	14–21	21–28	Workstation	Bipolar arrays BiCMOS arrays	1300–18,000 800–28,000	100–210 310–430	$10–$25 per gate $5–$15 per gate	$0.03–$0.05 per gate $0.0075–$0.04 per 1000 gates
Chip Express	1	5	Workstation	CMOS arrays	<20,000	Base-dependent	$10,000–$25,000	Must be contracted with silicon vendor
Fujitsu	7–14	30	Both	CMOS arrays ECL arrays	2880–60,000	470 350	$15,000–$150,000 $15,000–$150,000	$1.90–$2300 $1.90–$2300
Gould/AMI	21	38	Both	CMOS arrays	1286–150,000	320–500	$13,000–$120,000	$3.30–$145
Harris Semiconductor	14	21	Both (a)	CMOS arrays	960–32,854	<500	$13,000–$30,000	$0.12–$0.17 per 1000 gates
ILSI	21	56	PC	CMOS arrays	800–21,400	780	$5000–$25,000	$3–$30
IMI	7	10	Both	CMOS arrays	800–12,000	2000	$10,000–$25,000	$2.25–$29.03
Lasa Industries	8–12 hrs	Not applicable	(b)	CMOS and Bipolar arrays	(b)	(b)	(b)	
Lasarray Corp	8 hrs	2	PC	CMOS arrays	<10,000	700	$12,000–$15,000	$20
LSI Logic	8	21	Workstation	CMOS arrays	1000–50,000	570	$60,000–$80,000 (c)	$22
Mitsubishi	14	21	Both	CMOS arrays	224–35,000	370	$15,000–$75,000	$0.15–$0.18 per 1000 gates
Motorola	21	21	Workstation	CMOS arrays ECL arrays	2100–73,400 750–60,000	810 120–350	$20,000–$70,000 $14,000–$70,000	$1.80–$250 $10–$1600
National Semiconductor	14	21	Both	CMOS arrays	360–125,000	500–650	Starts at $40,000	$20–$400
NCR Microelectronics	7	28	Workstation	CMOS arrays	4800–74,800	530	$20,000	$7.00 (d)
NEC	14	21	Both	CMOS arrays BiCMOS arrays ECL arrays	300–133,056 575–23,200 540–33,250	430–1780 240–1180 200–270	$9000–$171,000 $10,000–$42,000 $12,000–$49,000	$1.90–$700 $7.50–$275 $160–$810
Oki Semiconductor	10	24	Both	CMOS arrays	300–140,000	270–1300	$35,000 (e)	$9.50 (e)
Plessey Semiconductor	28	60	PC	Mixed-signal CMOS	<10,000	60 nsec	$15,000–$40,000	$16.50
Siemens	13	25	Both	CMOS arrays	2000–70,000	400	Starts at $20,000	$4–$150
SMOS	14	21	Both	CMOS arrays	10,000–50,000	350–800	$15,000	$10
Toshiba	7	14–21	Both	CMOS arrays	5000–120,000	400	Starts at $15,000	Starts at $3
US2	21	28	Both	All-Layer CMOS	Layout-software dependent	500	$10,000–$200,000	Starts at $5
VLSI Technology	14	21	Workstation	CMOS arrays	960–69,000	340	$33,000–$139,000	$13–$345

Notes: (a) Harris supports schematic capture on both PCs and workstations and schematic capture on workstations.

(b) Lasa Industries does not build ASICs. It does sell the equipment that allows you to fabricate ASICs. The bases that you build the ASICs on determine the ASIC's density, speed, and cost.

(c) LSI Logic's NRE charge is for a 15,000-gate design and includes "hot-lot" premium.

(d) NCR's piece-part price is for a 5000-gate design in a 52-pin PLCC.

(e) Oki Semiconductor's prices are for an 8000-gate, sea-of-gates array fabricated on its 1.0 μm process.

(f) Toshiba achieves 7-day turnaround from its Sunnyvale, CA facility.

chitecture and automatic test-pattern-generation software. In addition to its larger testable arrays, the company offers the MPGA family to replace PLDs, EPLDs, and FPGA circuits that contain as many as 3000 gates.

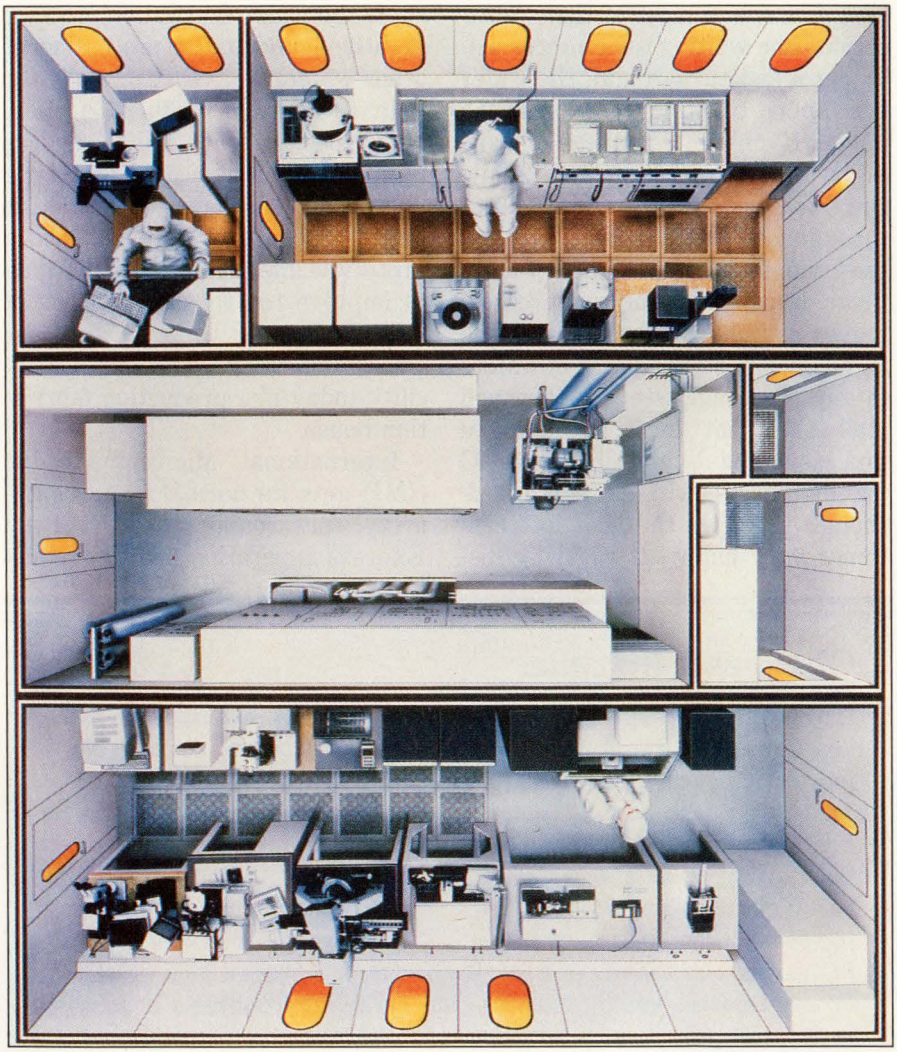
These smaller arrays accept PLD, EPLD, and FPGA circuit files. If your design is strictly synchronous, the vendor guarantees that the MPGA circuit will function as a drop-in replacement for the PLDs.

Software looks at critical paths

Harris also recognizes that testing your ASICs is the biggest hurdle to quickly delivering your prototypes. Like other leading-edge ASIC vendors, it has developed software that automatically converts your simulation patterns into test patterns. However, in addition to the functional and parametric tests that the software creates, Harris' test software evaluates critical paths during full-speed tests.

Just identifying the critical paths though, isn't enough. NCR has found that labeling these paths and then blindly letting the place and route software make tradeoffs often leads to poor overall circuit performance. The ASIC vendor should work with you to ensure that while the layout permits your critical paths to meet their design goals, noncritical paths don't become critical.

NCR also has software that bridges the ubiquitous wall between design and test. This software works with the simulator and allows you to input the kind of IC tester you'll use to evaluate your ASICs. With this information, the software creates tester-specific test patterns. By defining an operation, like a Write, as a particular set of inputs, you can program the software to drive the simulator with a user-defined high-level language. And, like many testers, the software offers a Learn mode. In this mode, you drive the simulator with a set of input conditions and the software learns the appropriate outputs. Beware, though. If your design contains an error, learning the outputs rather than programming them based on expected behavior will mask the error.



Direct-write systems need a fabrication facility. Lasarray's 750 ft² facility is shipped to your site in three modules.

The Test Assistant, Integrated Testability, and other test-logic and pattern-generation CAE tools reduce the bottlenecks that many vendors identify as slowing ASIC prototyping. Speeding the silicon through fabrication won't help you if there is no way to test and evaluate the devices when they come out.

Normally, an IC fabrication line resembles a motor-vehicle bureau's collection of queues. Every batch of wafers gets on a queue at every step of the fabrication process. In

Shortcuts that you take to finish a design—for example, not checking an input condition or ignoring testability—will inevitably come back to haunt you.

fact, ICs spend most of their fabrication time waiting to be processed. To get a fast turnaround, the wafer batch must bump to the front of the queue. Even jumping ahead of waiting wafers, the batch stalls while the wafers currently cycling through the process finish—unless the vendor is pushing wafers through using pre-emptive processing or call-ahead scheduling. If he is, he doesn't start a batch of wafers in any processing steps if they will stall the "hot lot." Pre-emptive processing is something few IC manufacturers will admit to. Although it makes the "hot lot" customer very happy, it radically disrupts the wafer-fabrication process, greatly delaying the processing of other wafers.

In recognition of these queues, NEC posits that ASIC vendors must employ a dedicated prototype line in addition to its full production line. The company employs such a prototype line at its facility in Japan to improve the turnaround time of its prototypes. Unfortunately for US customers, its Roseville, CA facility today is a production fabrication house.

International Microcircuits Inc (IMI) gets its normal 10-day gate-array turnaround using its Pony Express fabrication line. By reducing queues and walking wafers through the fabrication line, it can cut the fabrication time to seven days. Looking into the future, IMI claims that it sees ways to further reduce queues so that in the fall it can offer seven-day turnaround times as normal. Further plans are in place to cut the turnaround to four days by next summer. The company has a three-year goal of eliminating queues entirely and taking only 48 hours to process gate arrays.

In recognition of project turnaround being more than just prototype delivery, IMI offers specific suggestions to speed designs

Changes take time

If you have to revise your ASIC, do you have to wait for the entire fabrication-cycle time? Not necessarily.

There isn't much you can do to facilitate processing of array-based circuits. Should you need to revise these ASICs, count on fast-turnaround times of a week or two that the vendors in this report can provide as a best case.

Cell-based or all-level designs may offer an alternative to the complete fabrication cycle. Some vendors, Harris and VLSI Technology among them, will hold a few wafers of a wafer lot before metallization. Using these pre-metallized wafers, you can correct minor cell-based interconnect errors in array-based fabrication times. One hint: if you can, add a few spare inverters, NANDs, NORs, and flip-flops throughout your cell-based layout in case you need extra gates for corrections. Make sure you tie the spare gate's inputs to either power or ground so that they don't float.

Another alternative available to correct design errors is Micrion Corp's DMOD, a laser-based system that can cut interconnect, drill through dielectric, deposit vias, and rewire your ASIC.

The DMOD uses a beam of ions, focused to as little as 0.1 μm and accelerated to an energy of 25,000 eV. This beam makes cuts as small as 0.2 microns with a resolution to 0.25 microns. The system removes material by sputtering. To add connections, the ion beam decomposes a metal-carrying gas, such as tungsten carbonyl, at the surface of the circuit. Milling and deposition rates are about

$$\frac{2\times10^{4}\text{microns}^{3}}{\text{pA sec}}.$$

The DMOD uses a 68000-based Multibus architecture to control beam placement on the IC. By detecting secondary electrons or ions as the beam scans over the target, the system generates an image of the milling and deposition. The system handles packaged chips, unpackaged die, and whole wafers as large as 8 in. The machine starts at $695,000.

Machines with similar capabilities are available from Seiko Instruments USA and FEI Company. Seiko's machine, which starts at $600,000, features a dual optical lens and aperture control external to the vacuum so you needn't open the vacuum to adjust the aperture.

FEI Company makes the ion-focusing columns that Micron uses in its machines. FEI's focused-ion-beam machine starts at $250,000, can mill and deposit material on either 6-in. wafers or packaged die, and claims an ion source life of 500 hours.

Manufacturers of fast-turnaround ASICs

For more information on fast-turnaround ASICs such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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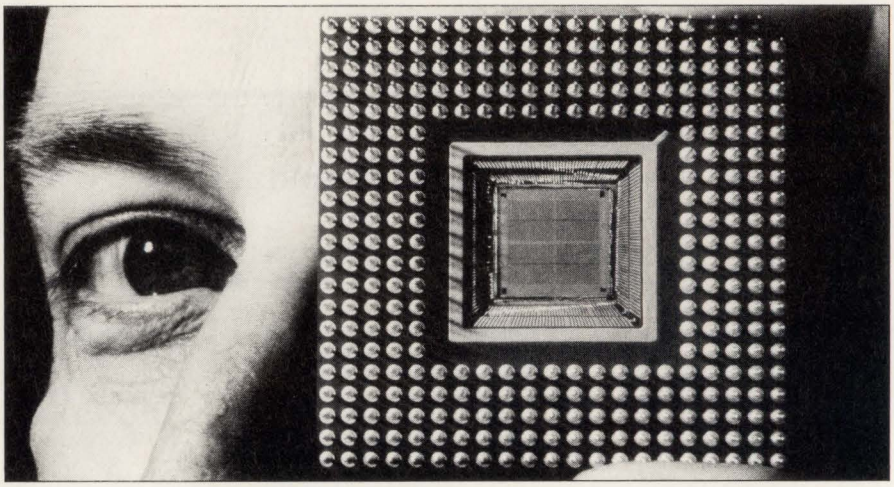

Quickturn processing of an ASIC isn't difficult. However, writing a test program to verify high-pin-count devices can slow prototype delivery. (Photo courtesy Siemens Components Inc)

through to production. Gary Smith, director of sales and marketing, warns that when the clock is ticking and people are breathing down your neck, there is a temptation to take short cuts to get the design out faster. Unfortunately, Smith claims that short cuts inevitably slow down the program in the end. IMI's engineering group works closely with customers to ensure that designs are right the first time. Most companies make similar claims, but IMI puts its money where its mouth is—it guarantees that your design will work in your system or it'll fix it for free.

Getting your ASIC through the design phase is another way to speed up the receipt of prototypes. Fujitsu and Mitsubishi, among others, offer RAM compilers that simplify the design of memory on an array-based ASIC. Fujitsu also offers collections of macro cells and compiled cells geared toward data-communications, graphics, personal-computer, and peripheral applications. Many components in Mitsubishi's low-power ASIC library offer four drive-strength options to optimize circuit performance and power requirements.

Plessey sees emulation as the key to ensuring a fast, first-time-right ASIC. The company couples its mixed-signal ULA series of arrays with its $15,000 PDM PC-based emulation system. With the PDM, you can build and system-test your mixed-signal ASIC, correct the design if necessary, and retest in the system before committing to silicon. Though emulation isn't foolproof—parasitics and other second-order effects differ between the emulator and actual design—Plessey hopes to provide working prototypes that don't need revisions.

If you need fast turnaround times, make sure that everyone in your company knows that you're pressing the vendor for time. Grease and prime each cog in your company machine so that people can prepare the appropriate paperwork and documentation. After begging and pleading with an ASIC vendor to speed your design through fabrication and give you prototypes in a week, nothing can be more embarrassing than to have the vendor wait three weeks for the purchase order. EDN

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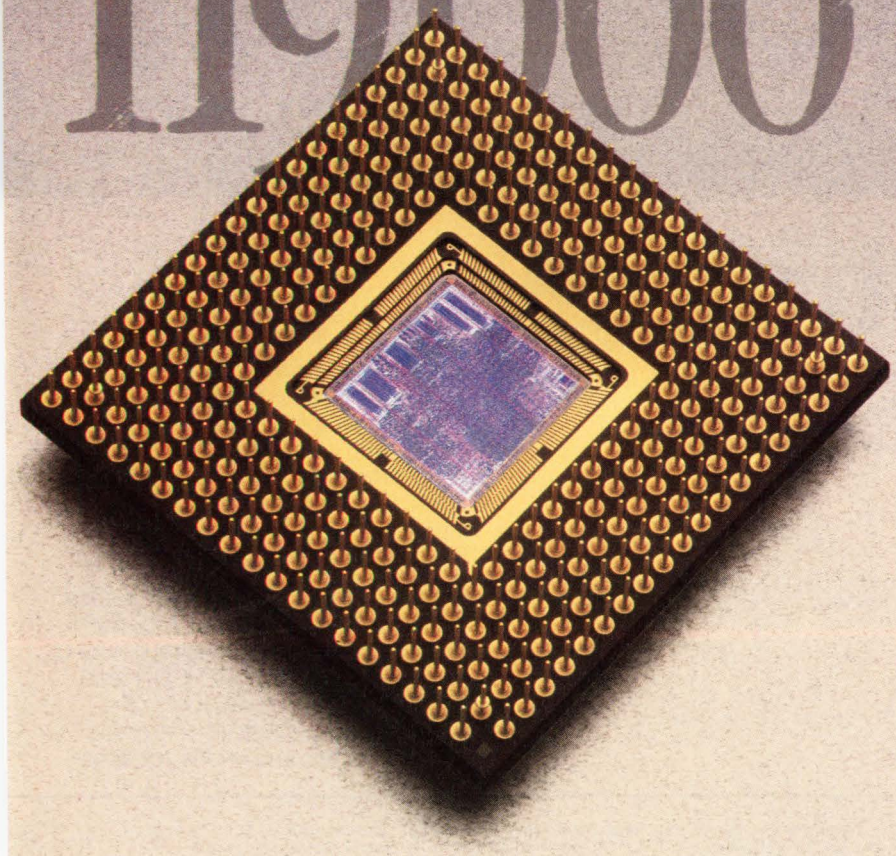

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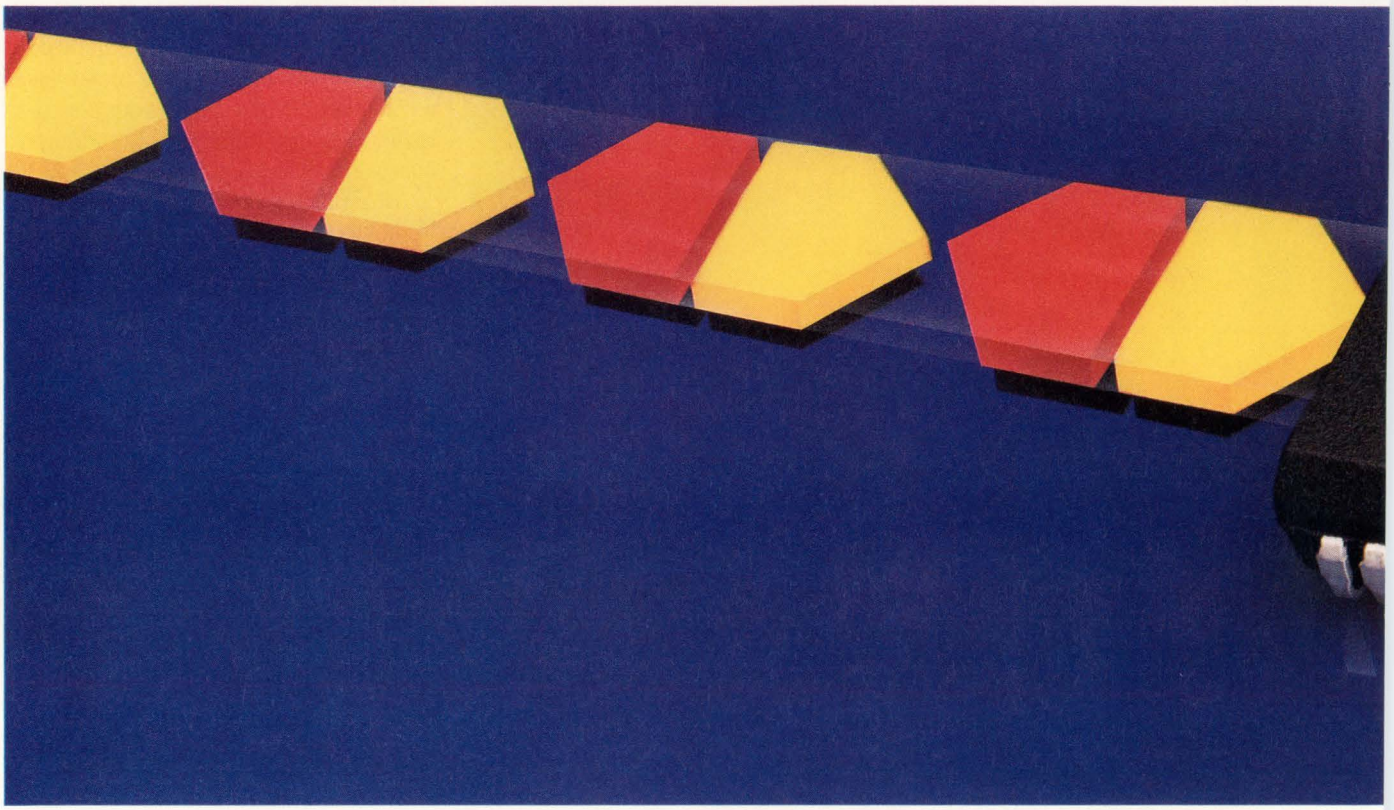

Sound Strategy.

Siemens announces a single-chip echo cancellation U-interface device for ISDNetworks of all sizes. From switching to transmission, a clearly superior solution. Berlin to Iselin.

Siemens has won another sound victory in communications technology by developing the industry's first single-chip solution in CMOS for echo cancellation circuit functions in ISDN. It's a clear example of the innovative thinking which has made Siemens a leader in ISDN technology.

From its single-chip design to its ease of integration, the Siemens PEB 2091 ISDN Echo Cancellation Circuit (IEC-Q) represents a milestone in ISDN realization. This device can double the traffic-handling capability in existing telephone lines, and is ideal for appli-

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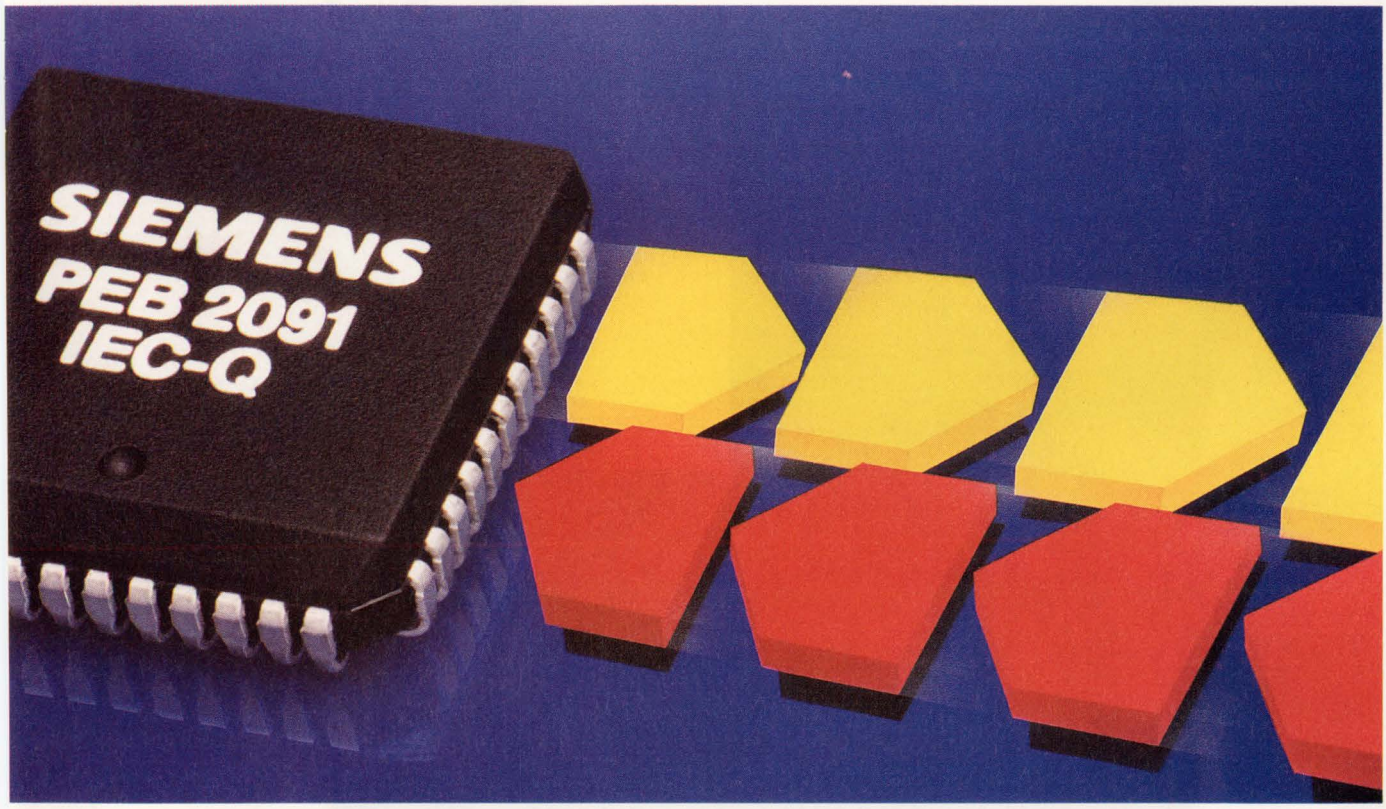

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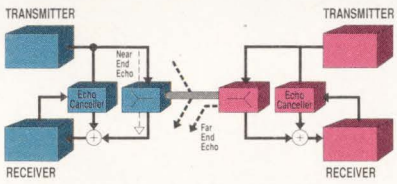

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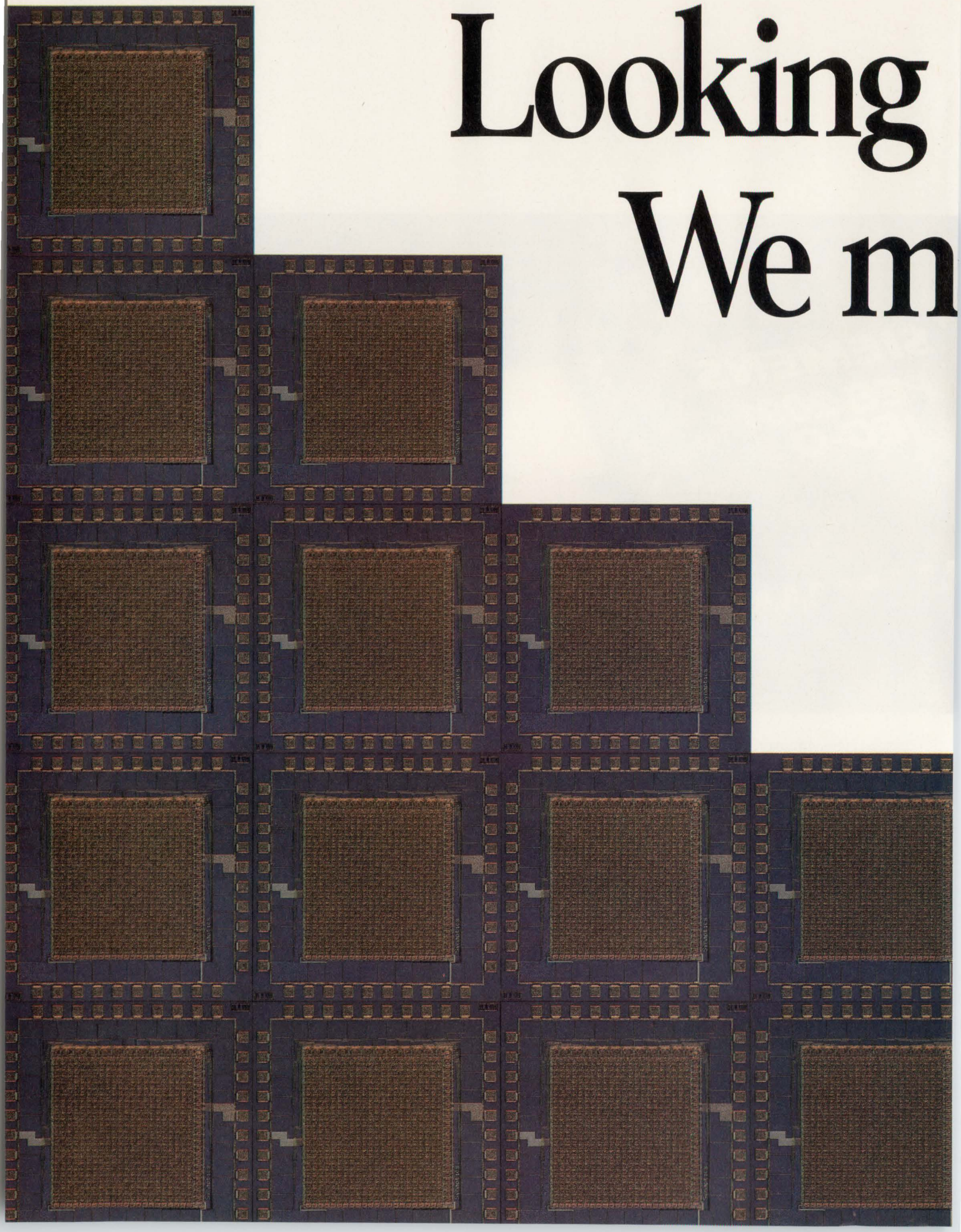

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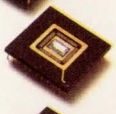

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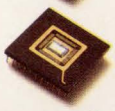

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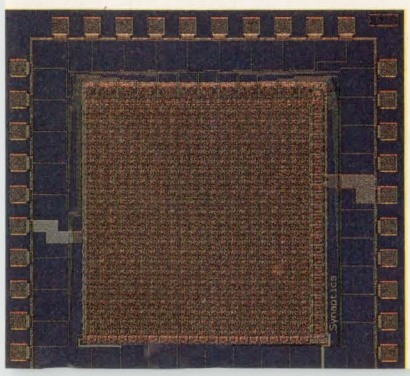

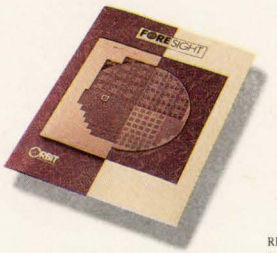

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Minimizing the effect of metastability in BiCMOS circuit design

In a digital circuit with two or more inputs, simultaneous changes in the signals at the inputs can produce an indeterminate or metastable state at the output. An unavoidable aspect of digital circuits in an analog world, metastability can impact a system's reliability. Intelligent circuit design requires a strategy to minimize this impact.

K Nootbaar, R W Spehn, and E Tyler, *Applied Microcircuits Corp*

Digital logic systems must be capable of interacting with the outside world to have practical applications. That world, on a human scale at least, is continuous and asynchronous—characteristics that are in direct contrast to the discrete quantization in value and time that digital systems require. Although this synchronization problem has been discussed in papers on computer-design theory since the early 1950s, the limitations of early technologies and the modest requirements for real-time input and output of data allowed most digital design engineers to safely ignore the problem (**Ref 1**).

The synchronization problem reappeared when the source of the input data was no longer a human at a keyboard or a low-bandwidth physical process, but rather another computer or fast digital system. Current applications, such as high-speed telecommunications and digital signal processing, force the designer to consider synchronization at almost every design stage.

The fundamental purpose of synchronization is to ensure that all portions of a clocked digital system uniformly agree on the binary value of any signal to which that portion is expected to asynchronously respond. One or more latches or flip-flops, which define the next state of the digital machine, synchronize that asynchronous decision. The logic designer is able to ensure that this condition is met in the sheltered environment of the synchronous system because all logical signals change at defined times relative to the clocking signal of any internal latch. The signals become stable again well before the next clock transition. However, the system functions as expected only if the designer considers the guaranteed propagation delays of the logic elements and respects the setup-and-hold restrictions of the latch or flip-flop.

The problem in the real world is that not all of the flip-flops in the system can satisfy their setup-and-hold restrictions. Some initial flip-flop must respond to an asynchronous event. This external event may have bandwidths that are orders of magnitude greater than those that were previously handled by simple analog filtering and oversampling.

A flip-flop or latch, which is designed to have two stable logic states, has two or more controlling inputs that let you predictably place the device in either state. For most configurations, changing the logic state of each input one at a time (a key consideration) results in the device assuming a known state after a finite and predictable

The fundamental purpose of synchronization is to ensure that all portions of a clocked digital system uniformly agree on the binary value of any asynchronous signal.

number of such input changes. The manufacturer usually defines this one-at-a-time restriction in terms of set/reset release times or data setup-and-hold times. These times are usually stated as guaranteed minimums. They are based on simulations and/or measurements of the specific device's behavior with respect to a well-behaved device. This procedure is true whether the flip-flop is a stand-alone device or a macro cell in an ASIC vendor's library.

According to most logic manufacturers, the result of violating the minimum setup-and-hold times of a flip-flop ranges from increased propagation delay to failure of the device to reliably retain the intended data state. What is not usually stated is that the flip-flop can become effectively "stuck" between states. More specifically, for some narrow range of multiple control-signal transition times, the output state can become anomalous (neither a logic 1 or a logic 0) prior to settling to some final state. Moreover, the duration of this anomalous state can become arbitrarily long.

The internal feedback loop of the master latch in a master-slave flip-flop comprises two inverting gain elements and a controllable feedback switch (**Ref 3**). This minimal structure is common to all logic technologies. The inverters have finite gain; the passive feedback paths have finite parasitics. These real-world limitations mean that in addition to the two intended stable states, the device can have a metastable state, which is often caused by conflicting, simultaneous commands at the inputs.

Compounding the problem is a real probability that the flip-flop will stay in the metastable state for a long time. Theoretically, the flip-flop can stay there forever (practically speaking, until the next clock cycle). This "middle-level" anomalous state at the feedback node of the flip-flop's master latch is also affected by succes-

Flip-flop timing definitions

Setup Time: The time allowed for the data signal to remain stable prior to the active edge of the clock signal.
Minimum Setup Time: The manufacturer's specified stabilization requirement of the flip-flop. Setup time less than this may cause unreliable or unspecified behavior of the flip-flop.
Hold Time: The time allowed for the data to remain stable after the active edge of the clock signal.
Minimum Hold Time: The manufacturer's specified minimum hold requirement. Like **Minimum Setup Time**, this term defines the boundary of reliable operation of the flip-flop.
Reset/Set Release Time: The manufacturer's specified minimum time after the de-assertion of an asynchronous reset or set for reliable clocking of the flip-flop.

For SSI flip-flops and latches, these times are specified at the package pins. For ASIC devices, the specifications apply to the inputs of the internal flip-flop macro. ASIC vendors provide guidelines for calculating the limits at the package pins as a function of the specified times, together with the propagation delays and skews of the other macros in the clock and data paths.

The figure is from D E White, "Logic Design for Array-Based Circuits," Chapter 5, Academic Press (Fall 1990).

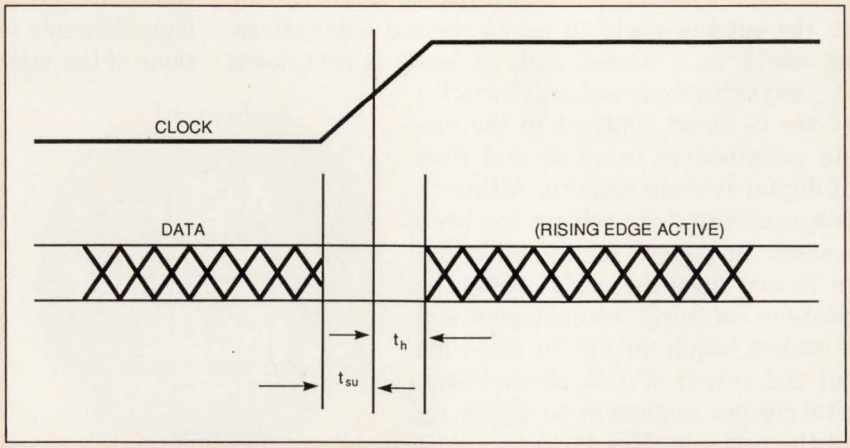

Fig A—Setup-and-hold times can be either positive or negative. *Here, the positive setup time (t_{su}) occurs before the midpoint of the active clock edge; the positive hold time (t_h) occurs after the midpoint of the clock edge. Negative setup time (not shown) occurs after the midpoint of the active clock edge, and negative hold time (also not shown) occurs before the midpoint of the active clock edge.*

sive logic stages that this node drives. Unless driven differentially, these logic stages, starting with the slave latch, will make an independent thresholding decision on this middle-level value. This signal level is usually "illegal" with respect to the requirements of the logic elements. It is likely to change before the circuit achieves final, stable equilibrium. Thus, different portions of the circuit assume different logical values of the node. This confusion usually results in a circuit malfunction.

You can define the flip-flop's metastable behavior as a statistical process. However, it is not possible to define a single, upper bound to the duration of this state. The question is not whether the state will occur, but rather how often a metastable state of duration greater than a specified time will occur. The accepted method of describing this type of performance limitation is in terms of mean time between failures (MTBF).

The MTBF model for quantifying the metastable behavior of a MOS flip-flop was formulated and extended to a method for using that information to optimize the design of the surrounding circuit (**Refs 3, 4**). A combination of circuit simulation of anomalous state duration and correlation with observed state duration of actual devices were used to define the criteria for optimizing the performance of an ECL bipolar flip-flop as a synchronizer, resulting in a "metastable-hardened" device (**Ref 5**).

We confirmed that there was no strict correlation between propagation delay and metastable behavior for different flip-flops. For at least the bipolar case, this lack of correlation was the result of specific and differing design optimization strategies. We also quantified the MTBF behavior of the metastable-hardened flip-flop and demonstrated a good correlation of the more useful and repeatable resolution-time-constant (τ) to the previously observed relative differences in anomalous state duration of the same devices (**Ref 6**).

Synchronizer functions

A synchronizer's function is to recognize the logic state at the input at any given instant. The output of a well-behaved synchronizer is a clear correlation of the sampling clock or periodic window function with the aperiodic and asynchronous external event or decision. In the case of the ideal or infinite-bandwidth synchronizer, the time-domain decision is strictly binary; the event either occurred or did not occur. If the event time is smoothly slewed through the clock edge or window, the resulting decision moves discretely from one clock period to the next in a monotonic fashion. In this ideal case, the synchronizer cannot fail because, as a state machine, it will only make transitions between its allowed states at the clock-period boundaries.

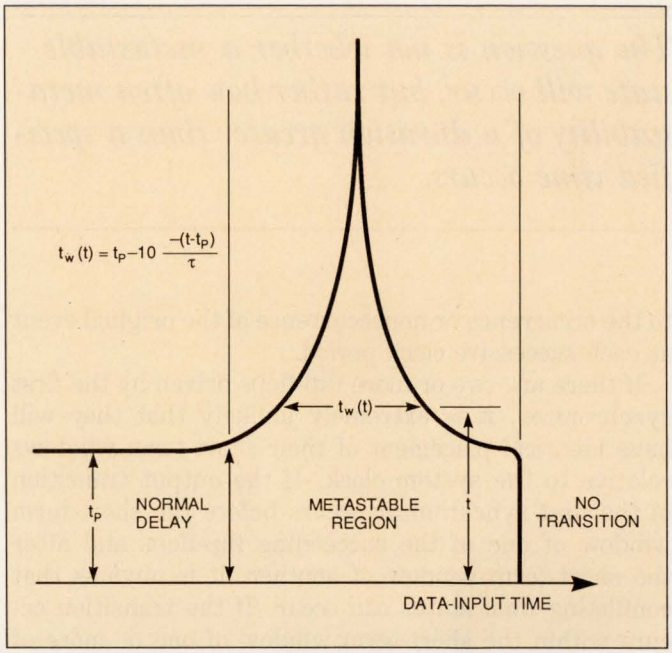

Fig 1—A timing graph *illustrates the relationship of output propagation delay with respect to data input time. The spike in the graph represents the region of possible metastable behavior.*

In actual applications, the synchronizer is implemented as one or more D flip-flops. These flip-flops have a nominal propagation delay when operated outside of the specified minimum setup-and-hold window, and the possibility of an increased or pathological propagation delay when operated within the window. The timing graph illustrates the relation of propagation delay to data-input transition time relative to the clock (**Fig 1**). The spike in the graph represents the region of possible metastable behavior. Depending on the amount of excess delay that succeeding logic stages can tolerate, the graph defines a short-term failure window. The position of this window can vary as a function of temperature, input-data state, clock pulse width, clock state at the time of data change, or operating frequency. This short-term window will usually fall within the larger specified setup-and-hold window of the flip-flop.

If the changing event or signal presented to the D input of the synchronizer falls within the smaller short-term window, there will be an increase in the clock-to-output propagation delay of the synchronizer. The final, stable state the output attains will be unpredictable. At some point, the lengthened propagation delay will violate the short-term window of one or more flip-flops whose inputs are Boolean functions of the synchronizer output. If only one flip-flop is driven by the synchronizer, it is, in effect, a second-stage synchronizer. If the lengthened propagation delay of the signal falls outside the short-term window of the second flip-flop, that second stage will make a clean decision as

The question is not whether a metastable state will occur, but rather how often metastability of a duration greater than a specified time occurs.

to the occurrence or nonoccurrence of the original event at each successive clock period.

If there are two or more flip-flops driven by the first synchronizer, it is extremely unlikely that they will have identical placement of their short-term windows relative to the system clock. If the output transition of the first synchronizer occurs before the short-term window of one of the succeeding flip-flops and after the short-term window of another, it is obvious that conflicting final states can occur. If the transition occurs within the short-term window of one or more of the flip-flops, it is also likely that they will make differing decisions as to the state of the synchronizer output and, within some subset of that window, the metastable condition will propagate further into the system. In either case, the logical integrity of the system will be compromised, synchronizer failure will occur, and a system crash will soon follow.

MTBF models in system design

A quantitative measure of synchronizer performance will buttress the preceding qualitative discussion. An MTBF model provides that quantitative tool; it lets you optimize system performance. This model is based on the concept of the "failure window"—$t_W(t)$ **(Ref 4)**. This window is the range of data-event transition times for which the flip-flop's propagation delay is greater than t. You can represent this relationship as

$$t_W(t) = t_P \cdot 10^{\frac{-(t-t_P)}{\tau}},$$

where t_P is the nominal clock-to-output propagation delay of the flip-flop and τ is the resolution time constant.

Although it is the base-10 form of the equation rather than the natural logarithmic base-e form, the equation is similar to that used in other research. Based on an analysis of the surrounding circuit, you can express the MTBF of the flip-flop in a specific application as

$$MTBF(t_F) = \frac{1}{2 \cdot f_C \cdot f_D \cdot t_W(t_F)},$$

where t_F is the pathological delay sufficient to violate the setup requirement of one or more of the succeeding flip-flops, f_C is the clock frequency of the synchronizer, and f_D is the data frequency or bandwidth of the synchronized event. The constant 2 indicates that there are two transitions in one cycle of the data waveform.

This form of the MTBF equation was used in previous work **(Ref 6)** with an adaptation of a published test-fixture design **(Ref 4)** as a 10K ECL version to characterize the resolution time constant of bipolar ASIC flip-flop macros. This combination further extended the MTBF equation to the specific case of the 2-stage pipeline synchronizer.

Characterizing BiCMOS metastability

The inclusion of bipolar internal buffers in BiCMOS ASIC arrays such as the AMCC Q14000 family provides the macro designer with an additional tool with which to address the reduction of the exponential time constant in the window and MTBF equations. Preliminary measurements indicate that design choices such as the placement of the set/reset gating as well as the use of a BiCMOS inverter to drive the transfer gate path has a significant impact on the metastability time constant. The ASIC user does not usually have the freedom or time to design custom flip-flops, but the user should inquire if the ASIC vendor has done such optimization and characterization.

In many applications the combination of event bandwidth and clock frequency may allow the single-stage synchronizer to provide adequate MTBF performance. In other situations system response-time limits (effective control-loop bandwidth, for example) may not allow multistage approaches. In either case, the system designer must evaluate the metastable hazard MTBF to ensure acceptable system reliability and, if required, provide a graceful recovery strategy to the next level of the system. In the case of the single-stage synchronizer, you can combine the failure-window equation and the MTBF expression as

$$MTBF(t_F) = \frac{1}{2 \cdot f_C \cdot f_D \cdot t_P \cdot 10^{\frac{-(t_F-t_P)}{\tau}}}.$$

Consider an application where you need to synchronize an effective 9600-baud data stream with a 50-MHz clock **(Fig 2)**. In this case, the $2 \cdot f_D$ term is replaced by the bit rate—9600. This function is well within the capabilities of 1.5-μm BiCMOS technology. Preliminary evaluation of representative AMCC BiCMOS flip-flops show that the worst-case time constant (τ) can range from 2.06 nsec for the FF04 to 1.22 nsec for the FF07. The clock-to-Q propagation delay of these two flip-flops is nearly identical; the difference in metastability characteristics is due to the more complex set/

reset function of the FF04 relative to the reset-only FF07.

You can make the first MTBF calculation assuming equal propagation delay and setup times of the succeeding logic stage. Using 3.75 nsec as the worst-case sum of propagation delay and setup time (t_P in the above equation) for both macro types, and noting the period of the clock is 20 nsec, the MTBF for the FF04 in the case above is 20 hours; the MTBF of the FF07 in the same application is 613 years. As an example of the relative sensitivity of the above equation to changes in parameters, repeat the calculation assuming that the t_P of the FF07 has been increased to 5.0 nsec because of additional factors such as wire length or fan-out. The MTBF of the FF07 version now falls to 58 years. It is apparent that the choice of the correct macro by the ASIC user (and its optimized design by the ASIC vendor) has a much stronger effect on MTBF improvement than user choices of interconnect, placement, and fan-out.

As the clock period becomes smaller, or the interstage gate delays and effective setup times increase, the $t_F - t_P$ term in the MTBF equation shrinks, degrading the MTBF value. Similarly, an increase in the f_D term by several orders of magnitude can have the same effect. If the bit rate in the preceding example is increased to 25M baud, the MTBF for the FF04 drops to 27.5 sec. By comparison, the FF07 version of the synchronizer has an MTBF of 86 days.

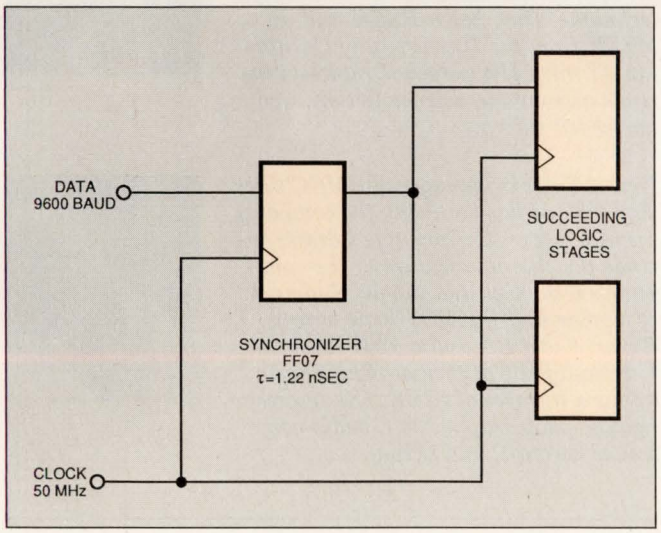

Fig 2—A single-stage synchronizer *can often provide adequate MTBF performance. In this 9600-baud application, the FF07 BiCMOS flip-flop with a worst-case time constant of 1.22 nsec can yield a theoretical MTBF of more than 600 years.*

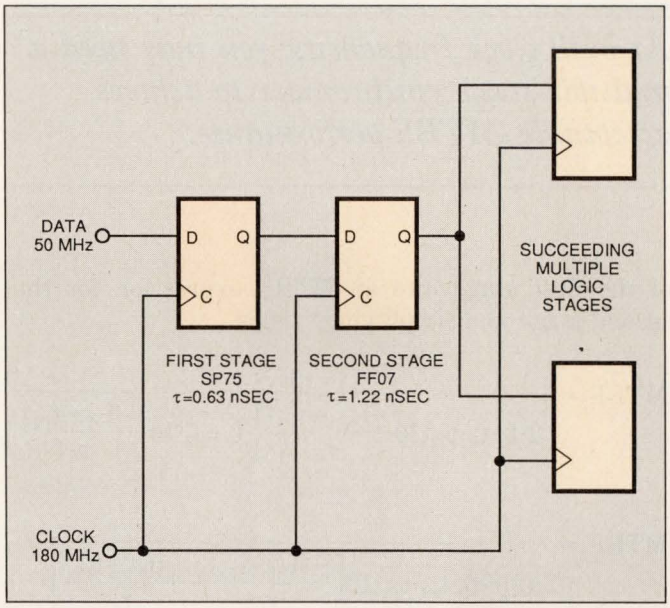

Fig 3—A 2-stage synchronizer *has the advantage of presenting the potentially metastable decision of the first stage to the second stage. In this example, the combination of high event bandwidth and clock frequency necessitate the use of a first stage having a time constant of only 0.63 nsec.*

The Q14000 BiCMOS array can also support all-bipolar structures in the I/O cells. Using this technique to construct a metastable-hardened bipolar flip-flop, the SP75, a worst-case time constant (τ) of 0.63 nsec was measured. If this I/O-based flip-flop were used as a synchronizer in the 25M baud example, the MTBF rises to 1.6×10^{14} years. Though the performance of this flip-flop in this application is impressive, the BiCMOS array has I/O bandwidth capabilities to 180 MHz. If the clock frequency of the previous example is doubled and the data frequency is raised to 50 MHz, the MTBF of the SP75 synchronizer falls to 23.5 hours.

Multistage synchronizers

The solution to this apparent roadblock to acceptable system reliability is a multiple-stage synchronizer. **Fig 3** shows a 2-stage version of such a synchronizer using the flip-flop macros discussed in the preceding example. The principal advantage of this shift-register-like structure is that the potentially metastable decision of the first stage is presented to only one flip-flop, the second stage. The possibility of multiple conflicting decisions is avoided until the next logic stage. The second-stage flip-flop still has the possibility of being forced to a metastable condition, but the frequency of transitions likely to fall in the short-term window is the reciprocal of the MTBF of the first stage for the t_F corresponding to the worst-case position of that short-term window.

Although experimental observation of devices indicates that the short-term window is about midway between the specified setup-and-hold times, conservative engineering would guide you to use the setup time as the worst-case position. Substituting the expression for the reciprocal of the MTBF (the failure frequency)

At high clock frequencies, you may need a multiple-stage synchronizer to achieve acceptable MTBF performance.

of the first stage into an MTBF expression for the second stage and simplifying, yields

$$MTBF_2 = \frac{1}{\left[2 \cdot f_C \cdot f_D \cdot t_{P1} \cdot 10^{\frac{-(t_{F1}-t_{P1})}{\tau_1}}\right] \cdot f_C \cdot t_{P2} \cdot 10^{\frac{-(t_{F2}-t_{P2})}{\tau_2}}},$$

$$MTBF_2 = \frac{1}{2 \cdot (f_C)^2 \cdot f_D \cdot t_{P1} \cdot t_{P2} \cdot 10^{\left[\frac{-(t_{F1}-t_{P1})}{\tau_1} + \frac{-(t_{F2}-t_{P2})}{\tau_2}\right]}}.$$

For the 2-stage synchronizer in this example, both t_{F1} and t_{F2} are 7.75 nsec. Worst-case t_{P1} is 0.95 nsec and worst-case t_{P2} is 2.25 nsec. The time constants for the two flip-flops are $\tau_1 = 0.63$ nsec (for SP75); $\tau_2 = 1.22$ nsec (for FF07). Inserting these values into the preceding expression gives a value for the MTBF of the 2-stage synchronizer as 5.98×10^9 seconds, or 189 years.

Note that adding second, third, or more stages to the synchronizer delays the decision in a pipeline fashion. This action narrows the effective short-term window at the input to the first stage. The definition of this effective window is the range of data-to-clock phase that will result in pathological delay at the output of the last stage. No amount of additional stages will make the short-term window reduce to zero width, but you can reduce the probability of synchronizer failure to "acceptable" levels if you can define such levels, and if the system response-time requirement allows the pipeline delay.

BiCMOS arrays allow a great expansion in the range of frequencies that VLSI ASICs can process. Just as a similar expansion in the capabilities of mainframe hardware and integration level required ECL designers to address the realities of metastability, progress in BiCMOS challenges the VLSI ASIC user. EDN

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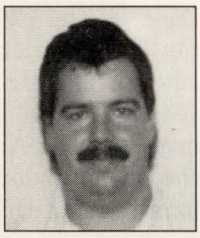
Authors' biographies



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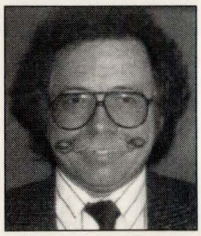

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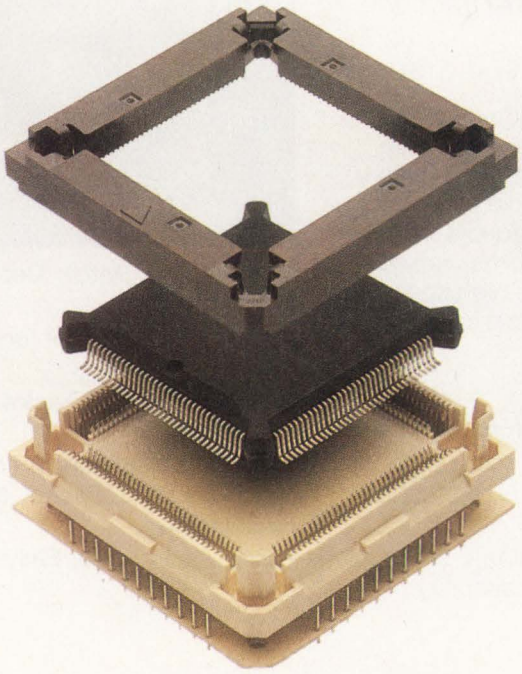

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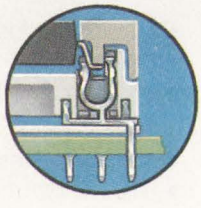

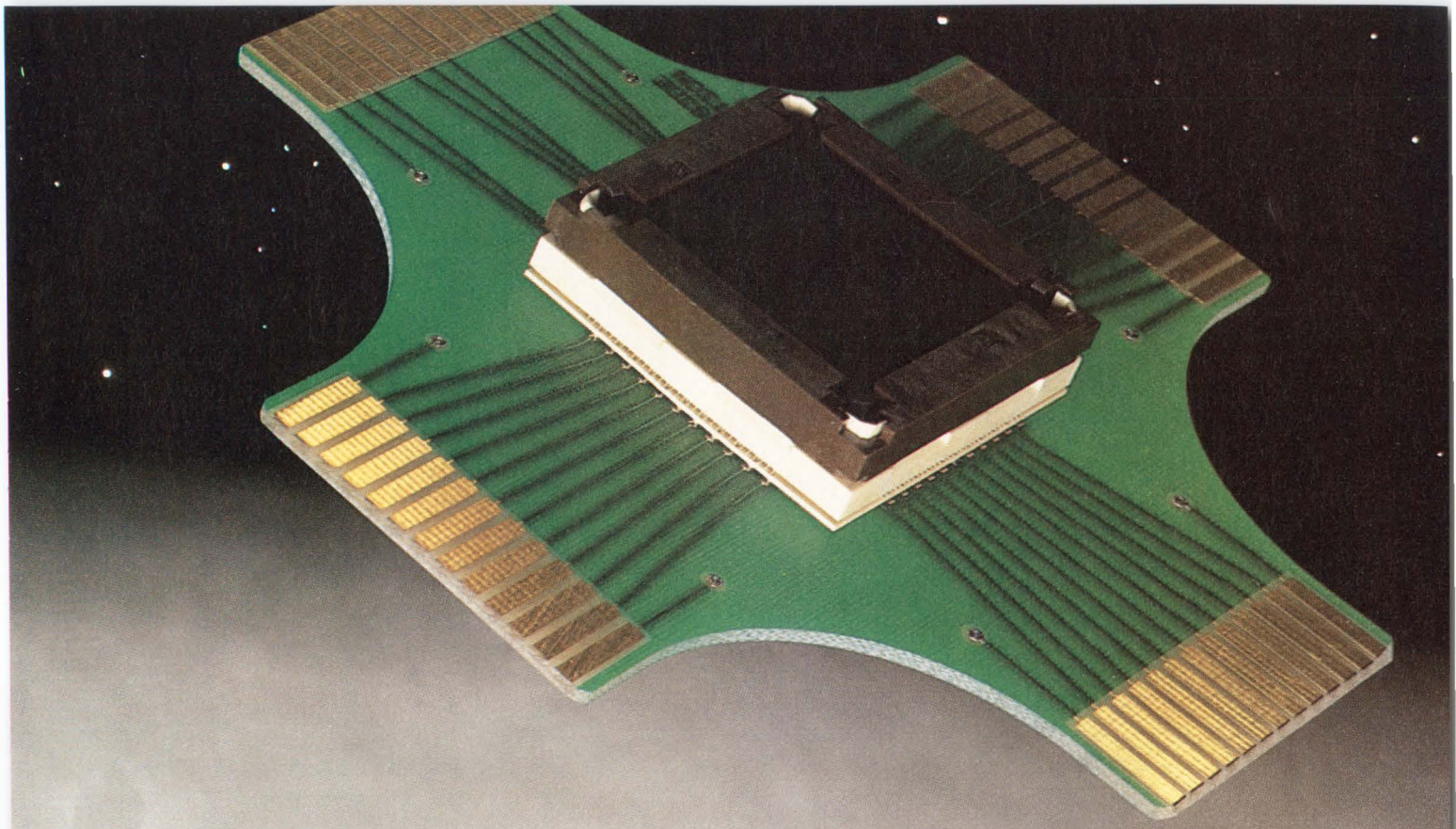

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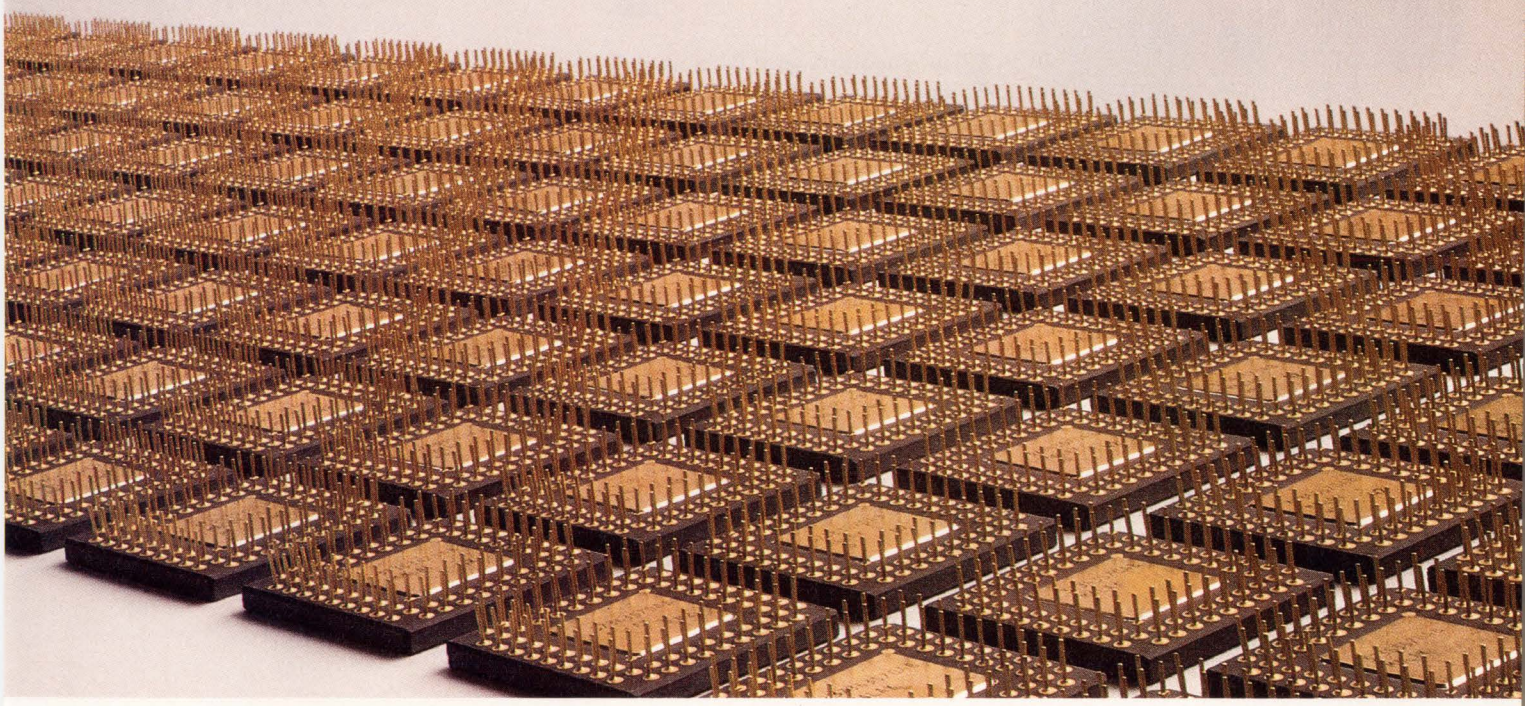

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EDN DESIGNERS' GUIDE TO

real-time Ada
Part 1

Ada's fundamental language structures build reliable systems

You can use the Ada programming language to build dependable real-time, embedded systems that work on a wide range of computing hardware. This article, the first in a 3-part series on Ada, illustrates the Ada features that support real-time programming and takes an in-depth look at multitasking.

Benjamin M. Brosgol, *Alsys Inc*

Ada's principal goals are program reliability, readability, efficiency, and portability. Many real-time application programs, such as those used in avionics, telecommunications, and manufacturing, need these features because of the large, complex, and long-lived pieces of software involved. Large programs beg for structure. Complex programs require modularity and well-defined interfaces between modules. Long-lived programs must be readable so that people unfamiliar with the programs can maintain them.

Ada achieves these goals through a structured-programming approach that permeates the language. For example, Ada is called a "strongly typed" language, which means that it prevents you from making implicit conversions between variables of different types. In addition, Ada will not allow you to call subprograms with arguments of the wrong type. The language rejects sloppy programming in favor of a more structured approach.

Match the type to the data

Ada lets you define many different data types so you can match a data type to the quantity that the variable represents. Scalar data types include numeric types for integer, floating-point, and fixed-point computation, and enumeration types for mnemonic names of constant integer values. Array types and record types let you define composite data structures. You can use access types to obtain pointers to dynamically allocated data. "Subtypes" let you constrain a data type's allowable values without affecting the available operations. For instance, the predefined type *INTEGER* has a subtype, *NATURAL*, that includes only the non-negative values.

Ada incorporates several features that aid in structured program control, such as conditional statements (*if—then—else* and *case*), iterative statements (*loop*, *while*, and *for*), and blocks (*begin* and *end*). Ada's procedures and functions, collectively referred to as "subpro-

Ada prevents you from making implicit conversions between variables of different types.

grams," work in much the same way as they do in other traditional algorithmic languages. However, Ada forces you to be very specific about the subprogram's calling parameters, which may be specified as *in* (read only), *in out* (readable and updatable), or *out* (write only). All of these descriptions are from the subprogram's viewpoint. Subprograms can be recursive, and you can nest them.

Multiple versions of a subprogram can have the same name, a facility known as "overloading." These like-named subprograms are differentiated by the types of the parameters and, in the case of functions, by the type of returned result. Overloading lets you use conventional mathematical notations—for example, "+"—for programmer-defined operations so you can create operations that work consistently over a range of data types. Ada also offers the ability to define parameterizable program units (referred to as generic units). For example, the predefined SEQUENTIAL_IO package is generic with respect to the element type. To obtain sequential input or output operations for a particular variable type, the program instantiates SEQUENTIAL_IO with the desired variable type. This generic facility is one of the keys to defining reusable, parameterizable components in Ada.

Packages provide modularity

The language's fundamental unit for program modularization is the "package," which lets you separate essential interface information from representational or algorithmic details. Implementation details within the package may change as program development un-

```
package SIMPLE_STATISTICS is
     type SAMPLE_TYPE is array (1..10) of FLOAT;
     function AVERAGE ( SAMPLE : SAMPLE_TYPE ) return FLOAT;
     procedure SORT ( SAMPLE : in out SAMPLE_TYPE ); -- Sort in descending order
end SIMPLE_STATISTICS;

--------------------------------------------------------------------------------

package body SIMPLE_STATISTICS is
     function AVERAGE ( SAMPLE : SAMPLE_TYPE ) return FLOAT is
          TOTAL : FLOAT := 0.0; -- Local variable, initialized to 0.0
     begin
          for I in SAMPLE'FIRST .. SAMPLE'LAST loop
               TOTAL := TOTAL + SAMPLE(I);
          end loop;
          return TOTAL / FLOAT(SAMPLE'LENGTH); -- TOTAL/10.0
     end AVERAGE;

     procedure SORT ( SAMPLE : in out SAMPLE_TYPE ) is
          TEMP : FLOAT;  -- Local variable
     begin -- Interchange sort
          for I in SAMPLE'FIRST .. SAMPLE'LAST-1 loop
               for J in I+1 .. SAMPLE'LAST loop
                    if SAMPLE(J) > SAMPLE(I) then -- swap them
                         TEMP := SAMPLE(I);
                         SAMPLE(I) := SAMPLE(J);
                         SAMPLE(J) := TEMP;
                    end if;
               end loop;
          end loop;
     end SORT;
end SIMPLE_STATISTICS;


with SIMPLE_STATISTICS; use SIMPLE_STATISTICS;
with SIMPLE_IO;
procedure MAIN is
     SOME_NUMBERS : SAMPLE_TYPE;
     MEAN         : FLOAT;
begin
     for I in SOME_NUMBERS'FIRST .. SOME_NUMBERS'LAST loop
          SIMPLE_IO.GET(SOME_NUMBERS(I));
     end loop;
     MEAN := AVERAGE ( SOME_NUMBERS );
     SIMPLE_IO.PUT(MEAN);
     SORT ( SAMPLE => SOME_NUMBERS );
     for I in SOME_NUMBERS'FIRST .. SOME_NUMBERS'LAST loop
          SIMPLE_IO.PUT(SOME_NUMBERS(I));
     end loop;
end MAIN;
```

***Fig 1—Ada programs consist of** specifications and program bodies. The specifications list a module's interface characteristics, and the bodies contain the code to implement the module algorithms. (Note: Text beginning with -- and continuing to the end of a line is a comment.)*

folds, so the separation of the package's interface information from the working code encourages the separation of program design from its implementation. The "package specification" contains the module's interface description; algorithmic details appear in the "package body."

Within a package, you can define a private variable type and subprograms that work on data having that type. In this way, you control exactly which properties of the privately defined type are accessible to other portions of the program outside the package. The package must explicitly export these public properties. Private variable types support data abstraction and information hiding and give Ada some of the characteristics of an object-oriented language. If you make a change in the representation of a private type (for example, by switching to a linked list instead of an array), this change is completely localized to the package; programs that use the package need not be modified. This language characteristic limits the effects of program changes to smaller, more manageable blocks of code.

Rules cross separate compilation boundaries

Ada permits separate compilation, which supports both top-down and bottom-up development. All language rules are enforced across separate compilation boundaries, requiring that interface information relevant to a compilation unit be preserved in a program library. Checking interfaces between separately compiled units saves time during system integration because mismatches between different parts of the program are caught incrementally as the program is built and not during final program integration.

Problems can also occur during a program's execution, so Ada provides exception-handling facilities for detecting and dealing with rare events, errors, and other unusual events that may occur during program execution. The language defines some exceptions, such as an index bounds violation; you may define others. A data-structure overflow is one example of a user-defined exception.

Fig 1 depicts an Ada program that comprises five compilation units: a specification and body for the package SIMPLE_STATISTICS, a main procedure (MAIN) that is called when the program starts, and the specification and body (which are not shown) of a package SIMPLE_IO. The specification of the package SIMPLE_STATISTICS declares a type SAMPLE_TYPE that serves as a template for 1-dimensional floating-point arrays. Each object of this type has 10 elements, indexed 1 to 10. The package specification also declares a function, AVERAGE, and a procedure, SORT.

Localize the effects of change

The package specification does not supply the algorithms for the AVERAGE and SORT subprograms; instead, the package body contains these details. The notation SAMPLE'FIRST denotes the index of formal parameter SAMPLE's lower bound (which has a value of 1). Similarly, SAMPLE'LAST denotes the index of the array's upper bound (10), and SAMPLE'LENGTH denotes the number of elements in the array (also 10). Although the literal values 1 and 10 could have been used, it is better to refer to these values symbolically through the "attributes" 'FIRST, 'LAST, and 'LENGTH. Using this method, you can localize the effects of a change in SAMPLE_TYPE's definition to one declaration.

The compiler requires the clause "with SIMPLE_STATISTICS;" to appear in MAIN so that the compiler can find the definition of SAMPLE_TYPE and the SORT and AVERAGE subprograms. The supplementary clause "use SIMPLE_STATISTICS;" in MAIN lets the program refer to names from the package SIMPLE_STATISTICS by their simple identifiers instead of using longer identifiers with prefixes that identify the package. MAIN also references the procedures GET and PUT defined in package SIMPLE_IO by the clause "with SIMPLE_IO;." The invocation of the SORT procedure

```
SORT ( SAMPLE => SOME_NUMBERS );
```

illustrates Ada's use of named parameters as opposed to a parameter passed by position—a feature many other programming languages don't offer. In this case, the array SOME_NUMBERS is passed as the array SAMPLE to the procedure SORT. Thus, you can use a formal parameter name as part of the syntax of a subprogram call, thereby improving the readability of the program.

Ada's general-purpose facilities encourage sound programming practice and are useful for any programming job, not just real-time applications. Real-time systems require two additional sets of capabilities: tasking features, which define parallel-processing units and their communicating and synchronizing methods; and

Isolating a package's interface information from the code that does the work encourages the separation of program design from its implementation.

low-level facilities, which deal with interrupt handling and machine-level representations. The remainder of this article discusses Ada's tasking features. **Part 2** discusses the language's interrupt-handling capabilities.

Concurrency in Ada

If a language provides a mechanism for defining parallel activities (tasks), you should investigate the following issues:

- How do I define a task?
- How do two tasks synchronize or communicate with each other?
- When does a task begin execution, and when does it terminate?
- How is mutually exclusive access to a shared resource obtained?
- How do I ensure that real-time processing constraints are met?
- How is execution controlled if there are not enough processors for running all eligible tasks (that is, what is the scheduling strategy)?

An Ada "task" is a program unit somewhat similar in form to a package. It consists of two parts: a "specification," which defines the task's interface to other program units, and a "body," which defines the task's algorithmic behavior and its interactions with other tasks. The interface defined by the task specification consists of a set of "entries"—names and parameters for sections of the task body's code that are used for synchronization or communication with other tasks. Each entry can be considered a service offered by this task to other tasks. Note that a task need not declare any entries in its specification. This situation might arise when the task offers no services to other tasks and is just a user of other tasks' services.

An entry is a generalization of a subprogram exported by a package. A package's subprogram exercises no control over the sequencing of calls from separate tasks. The same subprogram may have several simultaneous activations (and several copies of its local data) if called from several tasks; thus subprograms are re-entrant. However, this situation can lead to errors if the subprogram modifies nonlocal (shared) data. By limiting subprogram access through an entry, the task body determines the circumstances under which the entry's code body will be executed and the Ada tasking semantics ensure that this code is only executed on behalf of one task at a time. If several customers try to call the same entry at the same time, they will be queued and serviced one at a time.

An example of a task specification follows:

```
task SENSOR_DATA_MONITOR is
   entry SET ( ITEM : in SENSOR_DATA_TYPE );
   entry GET ( ITEM : out SENSOR_DATA_TYPE );
end SENSOR_DATA_MONITOR;
```

This task provides mutually exclusive access to an object of type SENSOR_DATA_TYPE. It assumes that other tasks may make asynchronous attempts to change the value of the object or read the object's value at any time. These other tasks use the SET entry call to assign a value to the data object and the GET entry call to retrieve the object's value.

Concurrent tasks interact through a mutual but

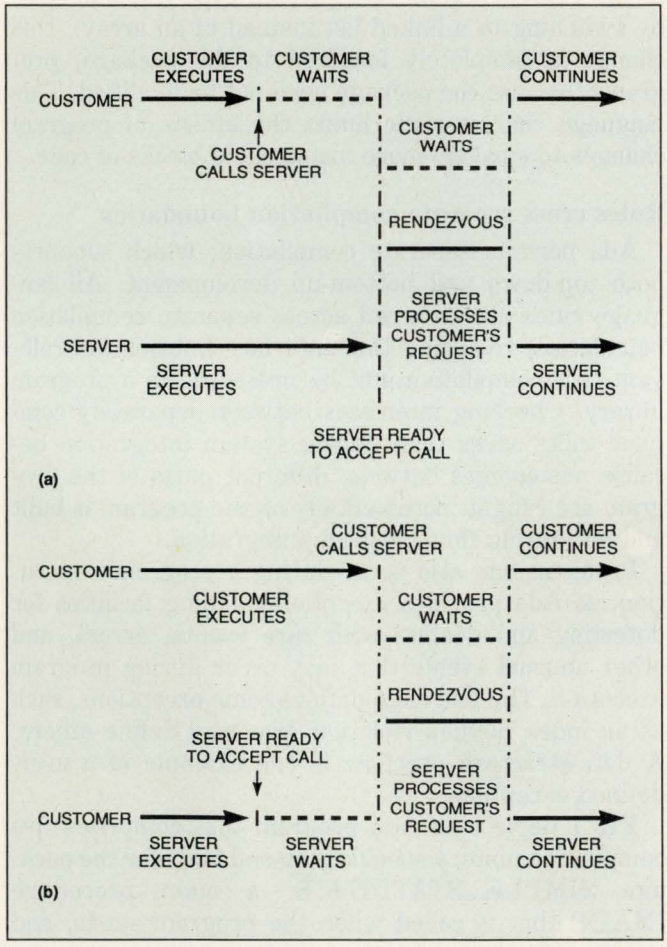

Fig 2—During a rendezvous, customer and server tasks achieve synchronization *by waiting for each other, if necessary. In* ***a****, the customer task waits for the server. In* ***b****, the server task waits for the customer.*

asymmetric arrangement known as a "rendezvous." The task body contains one or more "accept" statements for each entry declared in the specification for that task. Each accept statement corresponds to a point when the executing task can provide the service for the corresponding entry. An example of an accept statement from the body of SENSOR_DATA_MONITOR is

```
accept GET ( ITEM : out SENSOR_DATA_TYPE )
  ITEM := SENSOR_DATA;
end GET;
```

where SENSOR_DATA is the local data object that is being protected by the task.

Other tasks interact with an accepting ("server") task by issuing entry calls. For example, a task that assigns the current value of SENSOR_DATA to the variable SOME_DATA would contain the entry call:

```
SENSOR_DATA_MONITOR.GET ( SOME_DATA );
```

When the server task reaches an accept statement for an entry, and a calling ("customer") task is waiting for its call to be serviced, the server task executes the code associated with the accept statement while the customer task is still suspended. This event sequence is the rendezvous. Following execution of the server task's accept statement, both the customer and the server tasks can proceed again in parallel.

Serving the unknown task

The rendezvous is asymmetric because a customer task always specifies the name of the task when it calls an entry, but the server task's accept statement is anonymous—any customer will be served. This asymmetry makes it easier for you to define server tasks as reusable components because you don't need to make assumptions about the identities of the calling tasks.

The effect of a rendezvous depends on which of the two partners is the first to attempt communication. It's unlikely that the server task will reach an accept statement at precisely the moment when the customer task issues a corresponding call. If a customer task tries to call the entry of a server task, but the server isn't ready, **(Fig 2a)**, the customer task's execution suspends, freeing its processor for running other tasks. The customer task is placed in a queue associated with the entry that was called. The server task services this queue in FIFO order. On the other hand, if a server task reaches an accept statement for an entry call, but no callers are pending **(Fig 2b)**, the server task suspends. As soon as a customer task calls that entry, the server awakens and executes its accept statement.

```
1   task SENSOR_DATA_MONITOR is
2        entry SET ( ITEM : in SENSOR_DATA_TYPE );
3        entry GET ( ITEM : out SENSOR_DATA_TYPE );
4   end SENSOR_DATA_MONITOR;

5   task body SENSOR_DATA_MONITOR is
6        SENSOR_DATA : SENSOR_DATA_TYPE;
7   begin
8        accept SET ( ITEM : in SENSOR_DATA_TYPE ) do
9             SENSOR_DATA := ITEM ;
10       end SET;
11       loop
12            select
13                 accept SET ( ITEM : in SENSOR_DATA_TYPE ) do
14                      SENSOR_DATA := ITEM;
15                 end SET;
16            or
17                 accept GET ( ITEM : out SENSOR_DATA_TYPE ) do
18                      ITEM := SENSOR_DATA;
19                 end GET;
20            or
21                 terminate;
22            end select;
23       end loop;
24  end SENSOR_DATA_MONITOR;
```

Fig 3—You can use the accept statement *to create a task that offers more than one service to other tasks. (Note: Line numbers are for reference purposes only and are not part of the source program text.)*

Ada's tasks offer you considerable flexibility. For example, you can nest tasks. A task comes into existence as a separate parallel activity when the unit in which it is declared begins executing its statements. A task completes its execution when it reaches the *end* that terminates the task's statement sequence. Note that you can create a task that does not terminate. For example, a real-time system may require a task to execute an algorithm in an infinite loop. Further, programmers commonly use infinite loops for server

Named parameters help you improve your program's readability.

```
1    procedure TEST_MONITOR is
2         type SENSOR_DATA_TYPE is ...; -- Details not relevant
3         task SENSOR_DATA_MONITOR is ... end SENSOR_DATA_MONITOR;
4         task body SENSOR_DATA_MONITOR is ... end SENSOR_DATA_MONITOR;
5         task DEVICE_SIMULATOR;
6         task DEVICE_SIMULATOR is
7              DEVICE_DATA : SENSOR_DATA_TYPE;
8         begin
9              ... SENSOR_DATA_MONITOR.SET(DEVICE_DATA); ...
10             ... SENSOR_DATA_MONITOR.SET(DEVICE_DATA); ...
11        end DEVICE_SIMULATOR;
12        task DATA_COLLECTOR;
13        task DATA_COLLECTOR is
14             RAW_DATA : SENSOR_DATA_TYPE;
15        begin
16             ... SENSOR_DATA_MONITOR.GET(RAW_DATA); ...
17        end DEVICE_SIMULATOR;
18   begin
19        -- SENSOR_DATA_MONITOR, DEVICE_SIMULATOR, and DATA_COLLECTOR activated here
20        ...
21   end TEST_MONITOR;
```

***Fig 4—Ada's tasking constructs** let you create independent tasks that execute in parallel.*

tasks. Ada provides a mechanism to arrange an orderly shutdown of a task when no further interactions with it are possible so that tasks with infinite loops need not run forever.

Ensuring exclusive access

You can program mutual exclusion quite reliably in Ada. If your application requires mutually exclusive access to a data structure, you can declare the data local to the body of a protector (or "monitor") task. The monitor task allows access to the data only through accept statements. Thus all program access to that data is funneled through a single control thread. If several customer tasks try to access the data simultaneously, they will be queued and serviced in FIFO order. You control the degree of mutual exclusion when you write the monitor task. This approach is more secure than other exclusionary programming techniques such as semaphores, where mutual exclusion depends on all customer tasks observing the semaphore's protocol. Ada enforces mutual exclusion through the nature of the call-and-accept mechanism.

Ada also provides explicit timing control. A predefined fixed-point type named *DURATION* measures relative time, and a private type named *TIME* in the predefined package *CALENDAR* tracks absolute time. The *DELAY* statement suspends a task's execution for a specified *DURATION* value and thus allows you to program periodic activities. Other tasking statements let you program timed waits for entry calls and accept statements, so that server or customer tasks can proceed with execution if the rendezvous has not started within the specified period.

You can control task scheduling by assigning priorities to tasks. During execution, if a high-priority task becomes eligible to run—perhaps after the expiration of a delay—then the program's scheduler will pre-empt execution of a lower-priority task, if necessary, to run the high-priority task. During a rendezvous, if the server and customer tasks have different priorities, the accept statement executes at the higher of the two tasks' priorities.

If your application program requires a number of tasks that have the same algorithmic behavior, you

can use Ada's "task type" facility to obtain this effect. Because Ada treats tasks as data objects, you can assign a type to a task. A task type is a template for task objects and provides considerable expressive power especially when combined with "access types." An access type whose instances designate task objects allows the dynamic creation of tasks, linked lists of tasks, and other useful forms.

Putting the fundamentals together

Tasking programs frequently employ monitor tasks. **Fig 3** shows an example of a monitor task that encapsulates access to a sensor data structure. The handler for a hardware interrupt, as will be shown in more detail below, can call the SET entry to write a new value for the data. Alternatively, this entry can also be called by software tasks. A software task can call GET periodically to read the current value of the data.

Ada's tasking semantics and visibility rules provide mutually exclusive access to SENSOR_DATA through the accept statements for GET and SET in the body of SENSOR_DATA_MONITOR. If two customer tasks try to rendezvous with SENSOR_DATA_MONITOR simultaneously, then only one of them will get through, and the other will be queued.

SENSOR_DATA_MONITOR illustrates a very important Ada tasking construct, the "select" statement, which appears in lines 12 through 22 of **Fig 3**. You use this statement when you want to create a task that provides more than one kind of service—here GET and SET—and that can accept a call for any of the services offered. For each service offered, the task contains an accept statement within the select statement (lines 13 and 17). As illustrated in line 21, there may also be a special branch within the select statement to allow the task to shut down gracefully through self termination.

The task chooses which service to provide based on which service has pending customers. If no customers await service, the server task suspends until a call for one of its services is received. If exactly one service has customers in its queue, the first customer in the queue (the one waiting the longest) is served. If several of the queues contain customers, the task chooses one of the queues and serves the first customer in that queue. Ada's definition does not designate which of the non-empty queues the task should serve first although some implementations of the language may specify a scheduling discipline or allow you to exercise some control over the choice.

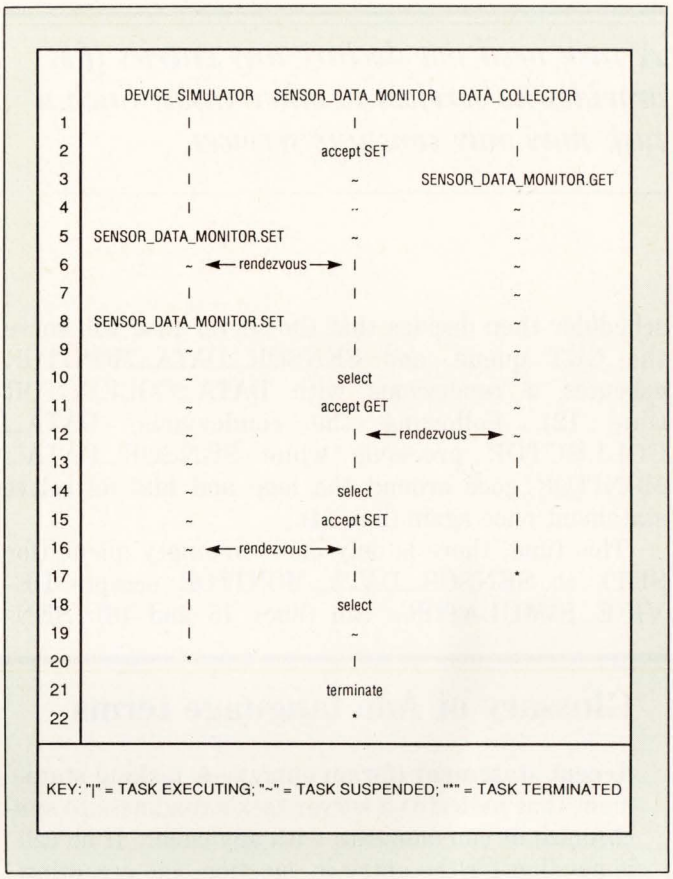

***Fig 5—Correct execution** of the server task is independent of the order in which entry calls occur.*

Tracing the execution of SENSOR_DATA_MONITOR illustrates the semantics of Ada tasking and the select statement. SENSOR_DATA_MONITOR activates when the unit in which it is declared reaches the beginning of its statements. For example, SENSOR_DATA_MONITOR might be declared in a procedure with the skeletal form shown in **Fig 4**. After this procedure reaches *begin*, its three "children" tasks SENSOR_DATA_MONITOR, DEVICE_SIMULATOR, and DATA_COLLECTOR activate and execute in parallel.

Suppose that the time ordering of the various tasking interactions is as shown in **Fig 5**. When SENSOR_DATA_MONITOR reaches its first accept statement for SET (line 2), no call is pending. Thus SENSOR_DATA_MONITOR suspends (line 3). Subsequently DATA_COLLECTOR calls SENSOR_DATA_MONITOR.GET (line 3) and suspends. Eventually DEVICE_SIMULATOR calls SENSOR_DATA_MONITOR.SET (line 5). This event awakens the server task, which executes the rendezvous and then proceeds in parallel with DEVICE_SIMULATOR.

DEVICE_SIMULATOR calls SET again on line 8 before SENSOR_DATA_MONITOR has reached its select statement. DEVICE_SIMULATOR therefore suspends. Eventually SENSOR_DATA_MONITOR reaches its select statement (line 10), with both the SET and GET queues non-empty. In this example, the

A task need not declare any entries if it provides no services to other tasks. Such a task may only consume services.

scheduler then decides that the server task will serve the GET queue, and SENSOR_DATA_MONITOR executes a rendezvous with DATA_COLLECTOR (line 12). Following the rendezvous, DATA_COLLECTOR proceeds while SENSOR_DATA_MONITOR goes around the loop and hits its select statement once again (line 14).

This time, there is only one non-empty queue (for SET), so SENSOR_DATA_MONITOR accepts DEVICE_SIMULATOR's call (lines 15 and 16). SENSOR_DATA_MONITOR will execute its select statement once more, on the next iteration of the loop, but because there are no pending calls to either entry, it suspends (line 19). The customer tasks eventually terminate normally (lines 17 and 20). Because no further communication with SENSOR_MONITOR_TASK is possible after these other two tasks terminate, SENSOR_MONITOR_TASK selects its terminate alternative (line 21), and the task terminates (line 22). Note that putting SENSOR_DATA_MONITOR's accept

Glossary of Ada language terms

Accept statement (for an entry)—A tasking statement that indicates a server task's readiness to synchronize or communicate with any caller. If no call is pending for the entry in question, the accepting task is suspended.
Access type—A data type whose values designate (or point to) dynamically created objects.
Block—A compound statement that can introduce local declarations.
Delay statement—A statement that suspends a task for a specified duration.
Entry—The interface to a task, used for synchronizing and communicating.
Entry call—A statement that indicates a task's readiness to synchronize or communicate with the server task that has declared the entry. If the server task is not ready to accept the call, the caller is suspended and placed in the queue corresponding to the called entry.
Entry family—A set of entries typically used to program prioritized selection of callers.
Exception handling—An Ada feature that allows the programmer to specify actions in response to runtime errors or other unusual events.
Exception propagation—The action a subprogram takes when it cannot handle an exception locally.
Generic—A template for a package or subprogram. It can accept parameters that select types, subprograms, or objects for inclusion in a particular package or subprogram the generic produces.
Interrupt entry—An entry corresponding to a hardware interrupt. The accept statement for this entry performs interrupt-handling functions.
Overloading—The ability to have the same name designate different declared program entities.
Package—An Ada feature for grouping related entities together. It comprises a separately compilable specification and body, and is the basic unit of program modularity in Ada.
Priority—A mechanism for indicating which of several tasks eligible for execution should be given to the processor.
Private type—A type whose representation is inaccessible outside the defining package and whose objects can only be manipulated by the package's operations. Private types support data abstraction and information hiding.
Program library—A database of information about compiled units that allows language-rule enforcement across separately compiled units.
Rendezvous—The Ada task-synchronizing and -communicating primitive. It is the server's execution of an accept statement on behalf of the longest-waiting task that has called the entry.
Representation clause—An Ada feature that lets end users specify type representation, machine addresses for declared program entities, and other low-level characteristics.
Select statement—A statement that lets a server task accept an entry call from one of several tasks.
Server task—A task that declares an entry.
Strong typing—A means of categorizing data objects based on the kinds of operations that can be performed on them.
Subprogram—A code module; either a procedure or a function.
Subtype—A constrained set of values from a type.
Task—The unit of parallelism in Ada.
Task type—A template for creating task objects.
Type—A template for creating data objects.

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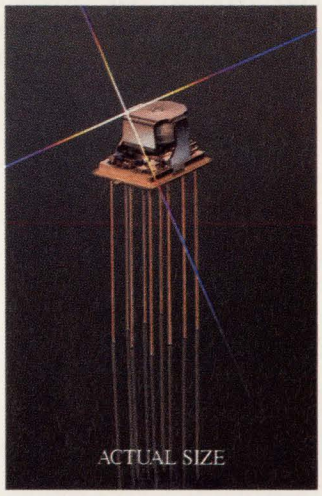

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CIRCLE NO. 66

Concurrent tasks interact through a mutual but asymmetric arrangement known as a "rendezvous."

statement for SET before the select loop ensures that the monitor data item is always assigned a value before it can be read. As illustrated in **Fig 5,** any customer that calls GET will suspend until the server task accepts at least one call to SET.

For simplicity, this specific example showed only two customer tasks that called different entries. For this scenario, the maximal length of either queue is one. In more general cases, the queue sizes can be greater than one. Moreover, SENSOR_DATA_MONITOR is written so that two tasks cannot obtain the protected variable's value through GET simultaneously. This condition is more restrictive than necessary. You can write the monitor task in a more general way to allow simultaneous read accesses while still preventing simultaneous writes or a simultaneous read and write. An example of such a read/write task appears in **Ref 1.**

Limiting services as needed

The monitor task illustrates the basic form of the select statement, in which a task can provide any of its services at any time. In some situations, you may need to restrict some services. For example, consider a task that encapsulates a bounded (also called a circular or ring) buffer with entries that allow other tasks to insert or remove buffer elements. A task cannot insert an element into the buffer if the buffer is full. Any task trying to perform this operation should suspend until there is room in the buffer. Similarly, a task cannot remove an element if the buffer is empty.

Placing special conditions called "guards" on the select statement achieves this effect. The program evaluates the guard expressions first. Any guards that test false are ignored and are said to be "closed." Only those branches with true ("open") guards, together with those branches that don't contain any guards, are considered as candidates for selection. After eliminating closed branches, selection occurs as for a simple select statement.

You can build a bounded buffer **(Fig 6)** using the guarded select statement shown in **Fig 7.** Initially the buffer contains no elements (COUNT is 0), and any

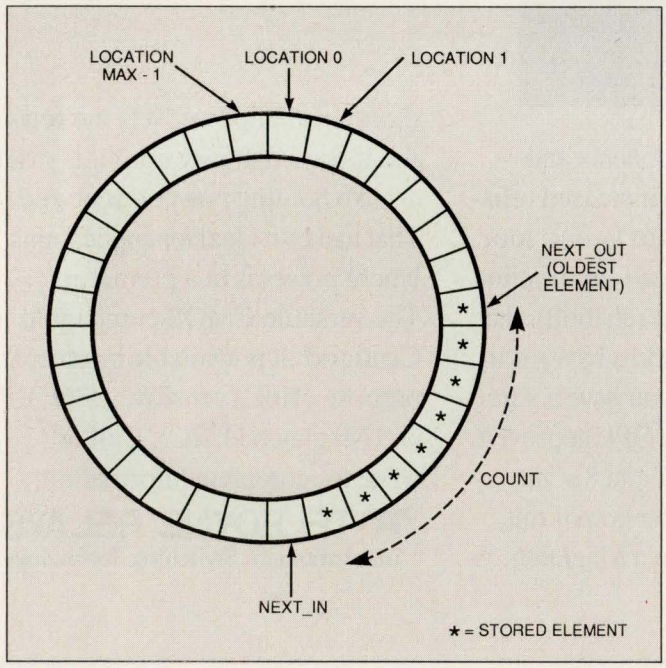

***Fig 6—A bounded buffer** starts out empty and can become full. The task that implements this buffer must not accept calls to remove elements when the buffer is empty (or the buffer will underflow) and must not accept calls to insert elements when the buffer is full (or the buffer will overflow).*

```
task BUFFER is
     entry INSERT (ITEM: in ELEMENT_TYPE);
     entry REMOVE (ITEM: out ELEMENT_TYPE);
end BUFFER;

task body BUFFER is
     RING : array (0..MAX-1) of ELEMENT_TYPE;
     NEXT_IN, NEXT_OUT: INTEGER range 0..MAX-1 := 0;
     COUNT : INTEGER range 0..MAX := 0;

begin
     loop
          select
               when COUNT > 0 =>
                    accept REMOVE (ITEM: out ELEMENT_TYPE) do
                         ITEM := RING(NEXT_OUT);
                    end REMOVE;
                    NEXT_OUT := (NEXT_OUT + 1) mod MAX;
                    COUNT := COUNT - 1;
          or
               when COUNT < MAX =>
                    accept INSERT (ITEM: ELEMENT_TYPE) do
                         RING(NEXT_IN) := ITEM;
                    end INSERT;
                    NEXT_IN := (NEXT_IN + 1) mod MAX;
                    COUNT := COUNT + 1;
          or
               terminate;
          end select;
     end loop;
end BUFFER;
```

***Fig 7—Guarded select statements** allow you to selectively activate and deactivate a task's services based on changing conditions.*

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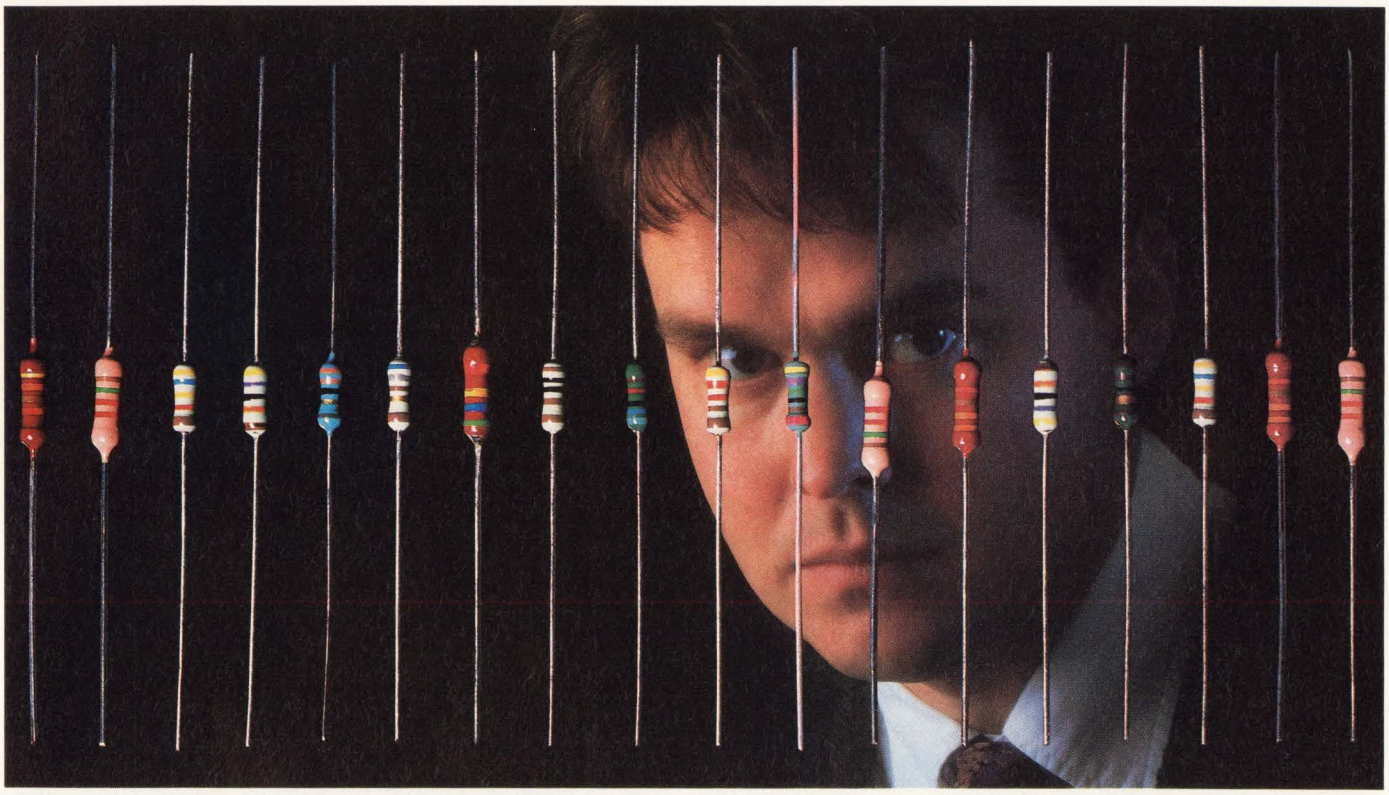

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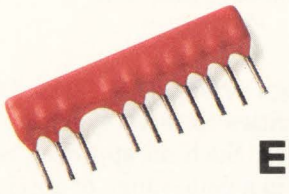

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Ada's tasking semantics and visibility rules provide mutually exclusive access to variables through accept statements.

task attempting to call REMOVE will be suspended and queued because only the INSERT branch of the select statement is open. After a task calls INSERT, BUFFER puts the element passed by the call into the RING array and increments COUNT. The next time through the loop, both branches of the select statement are open and calls to either INSERT or REMOVE can be accepted. If a stream of calls from producer tasks fills RING (COUNT = MAX), then the INSERT branch will close and subsequent producers will suspend when they call INSERT. If a consumer task eventually calls REMOVE so that RING is no longer full, both branches will again be open so that BUFFER can accept calls from producers or consumers.

The BUFFER task is useful for producer-consumer application programs. Note that both producers and consumers are customers of BUFFER. This is a common situation in Ada; you often create a task to provide resource encapsulation. Tasks that use this resource do so via entry calls. Thus the producer and consumer tasks can proceed asynchronously. The buffer eliminates the need for a producer to wait for an item to be consumed before producing the next one. If you programmed the producer and consumer tasks to communicate directly, the rendezvous semantics would induce unwanted synchronization.

The BUFFER algorithm illustrates yet another important point. The rendezvous code for each entry copies the item into or out of the RING array; it does not perform the additional housekeeping operations such as incrementing or decrementing COUNT. Your tasks should perform housekeeping operations after the rendezvous in the lines following the accept statement. Putting these operations outside the accept bodies increases the system's parallelism, because the customer task can continue as soon as the rendezvous completes. If the housekeeping code were in the accept statements, the program would still work, but the customer tasks would be unnecessarily suspended for the additional time required to execute this code.

Don't abuse priorities

Ada allows you to assign priorities to tasks, but you should not use task priorities to force synchronization to occur in a certain order. Such an approach reduces the language's flexibility in a wide range of applications and encourages an error-prone programming style. For example, the use of priorities to enforce a desired schedule could result in different (incorrect) behavior when you port your program from one processor to a multiprocessor environment.

The rules for task scheduling in Ada require a program to use task priorities in only one situation. If two tasks with different priorities are both eligible for execution and could sensibly be executed using the same CPU, then the task with the higher priority must execute while the task with the lower priority suspends (**Ref 2**). However, entry service occurs on a FIFO basis regardless of priority (a rule based on efficiency considerations). In addition, when a select statement has several open alternatives, implementations need not take priorities into account when deciding which one to accept. Instead, for example, they can take fairness criteria into account.

These characteristics of Ada's priority rules have attracted some criticism. For certain applications, a task's importance can change during the program's execution. Ada's priority rules don't match this mode-dependent change in a task's importance. To meet the real-time deadlines for such applications, the scheduling mechanism for entry service and for choosing among a select statement's alternatives must take into account the importance of these tasks. Implementation-specific facilities offered by various Ada systems address these issues.

If your application requires priority-based entry service, you can make use of an Ada feature known as "entry families," which creates multiple entry queues for customer tasks with different priorities (one queue for each priority level). Guards for low-priority queues can check the higher-priority queues before opening. If any of the higher-priority entry queues contain at least one customer, the guard on the lower-priority queue remains closed. The server task thus accepts calls from low-priority customer tasks only when there are no pending calls from higher-priority customers.

Ada language implementations can solve the problem of nondeterminism when there are several open alternatives in a select statement by providing directly or letting you dictate the use of task priorities. A similar method can resolve problems created by the static nature of Ada's predefined subtype *PRIORITY*. A language implementation can provide a more general concept than *PRIORITY* and thus allow dynamic manipulation of task priorities.

You can also obtain the effects of priority scheduling for entry service and select statements through a sim-

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ple programming style, without any support from the Ada implementation. Define the priority of each server task to be greater than the priority of any of its customers. This is equivalent to having nonpre-emptable servers. So long as such tasks do not block, there is no way that queues will form or that more than one entry can have a pending caller.

Ada's design intentionally leaves many of the task-scheduling decisions open rather than settling on a particular strategy, since such flexibility extends the language's range to a wide class of applications. Consequently, various Ada implementations can provide the capabilities required for real-time and many other kinds of programs. Thus, Ada allows you the flexibility to create real-time systems while avoiding the chaotic programming styles often employed to create such systems. EDN

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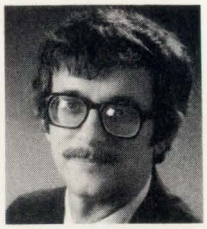
1. Barnes, John, "Programming in Ada (3rd edition)," Addison-Wesley Publishing Co, 1989, Sections 14.5 and 14.7.
2. "ANSI/MIL-STD-1815A Ada Reference Manual," Section 9.8, Paragraph 4.

Author's biography



Benjamin Brosgol is vice president and technical director at Alsys Inc (Burlington, MA). He is in charge of the company's Ada training and consulting, has helped develop Ada compilers and computer-based training products, and is the chairman of the Commercial Ada Users Working Group of the SIGAda professional society. Benjamin holds an MS and PhD in Applied Mathematics from Harvard University in Cambridge, MA, and is a member of both the IEEE and the Association for Computing Machinery.

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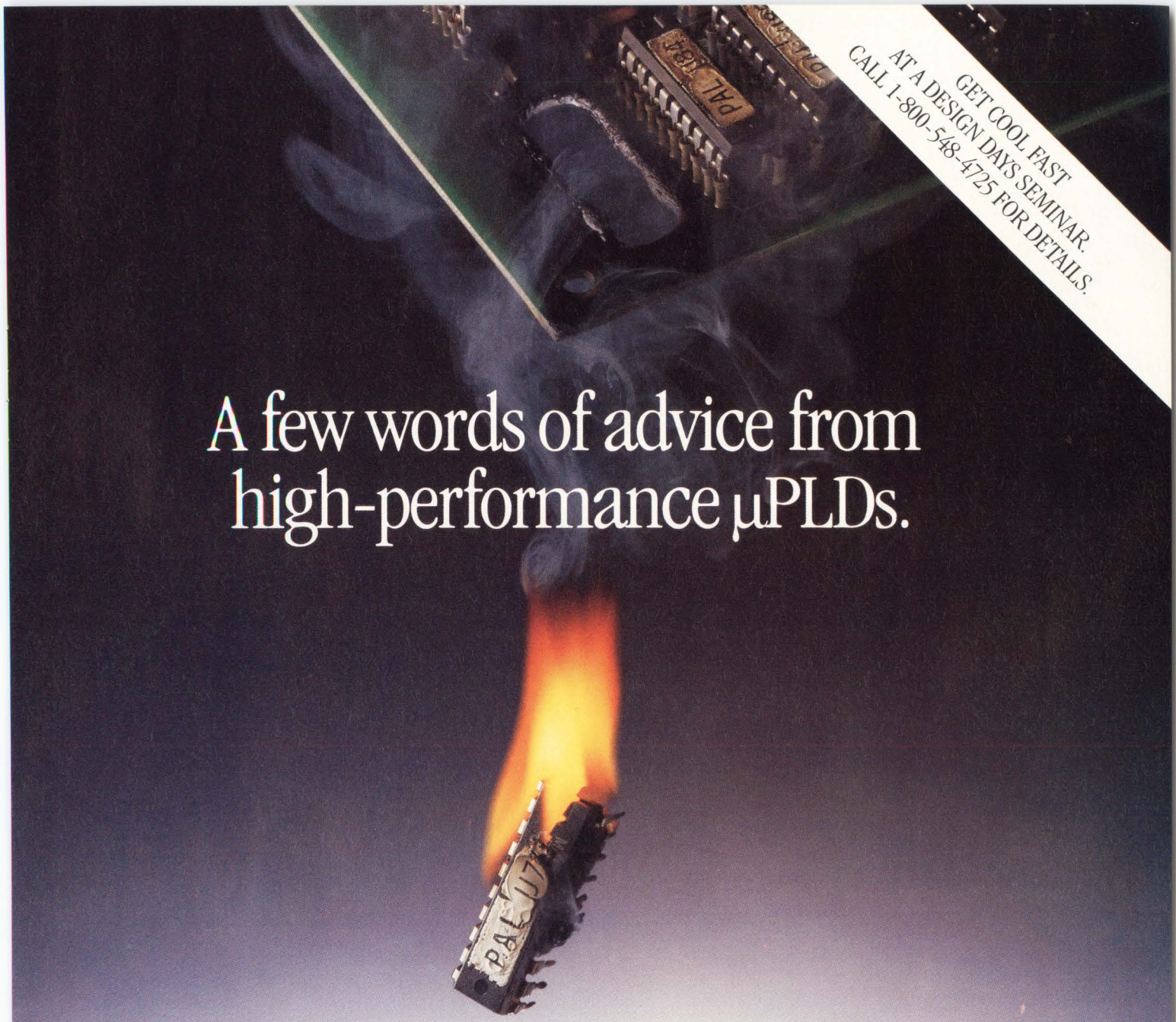

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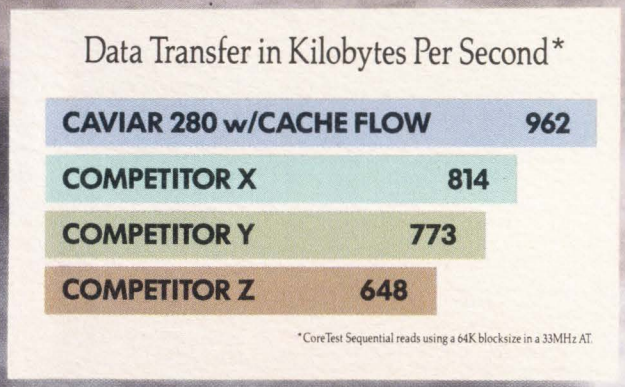

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CIRCLE NO. 72

EDITED BY CHARLES H SMALL

Rectifier converts wideband sine waves

Greg Schaffer
Maxim Integrated Products, Sunnyvale, CA

The circuit in **Fig 1** converts the amplitude of ac sine waves to an equivalent dc level over a 10-MHz bandwidth. The circuit's video op amps have transconductance output stages, which suit the circuit's active rectifier. **Table 1** shows the circuit's output voltage at different input levels and frequencies.

Op amp IC_{1A} is a scaling amplifier whose inputs offer no appreciable load to the signal source. Resistors R_1 and R_2 set this stage's closed-loop gain to a level that both compensates for small-signal losses arising from the amplifiers' low open-loop gains and boosts the signal voltage from an rms level to an average, equivalent dc level. R_3 and C_3 compensate this amplifier to achieve unity-gain stability.

In the second stage, IC_{1B} is an active full-wave rectifier with differential dc output. R_5, R_6, and D_1 rectify negative-output signals. R_9 and C_4 form a lowpass filter, as do R_{10} and C_5. The dc output is the sum of two equal and opposite signals. You could also use either signal alone and multiply it by two to get the proper dc level.

The circuit can handle only pure sine-wave inputs with amplitudes of 1.5V rms max. The circuit functions best with sine waves in the 0.1 to 1.0V rms range, but works well at amplitudes as small as 10 mV rms.

EDN

Table 1—Frequency response

V_{in} (V rms)	V_{OUT} (V dc) at frequency (MHz)								
	0.001	0.010	0.100	1.00	2.00	3.00	5.00	7.00	10.0
0.010	0.0096	0.0096	0.0094	0.0072	0.0045	—	—	—	—
0.030	0.0298	0.0298	0.0296	0.0279	0.0238	0.0205	0.0142	0.0076	—
0.100	0.1002	0.1002	0.999	0.968	0.931	0.894	0.828	0.752	0.616
0.300	0.3016	0.3015	0.3011	0.2959	0.2914	0.2876	0.2815	0.2728	0.2570
1.000	1.005	1.005	1.003	0.995	0.986	0.979	0.970	0.948	0.920
1.500	1.492	1.493	1.489	1.478	1.464	1.446	1.398	1.351	1.284

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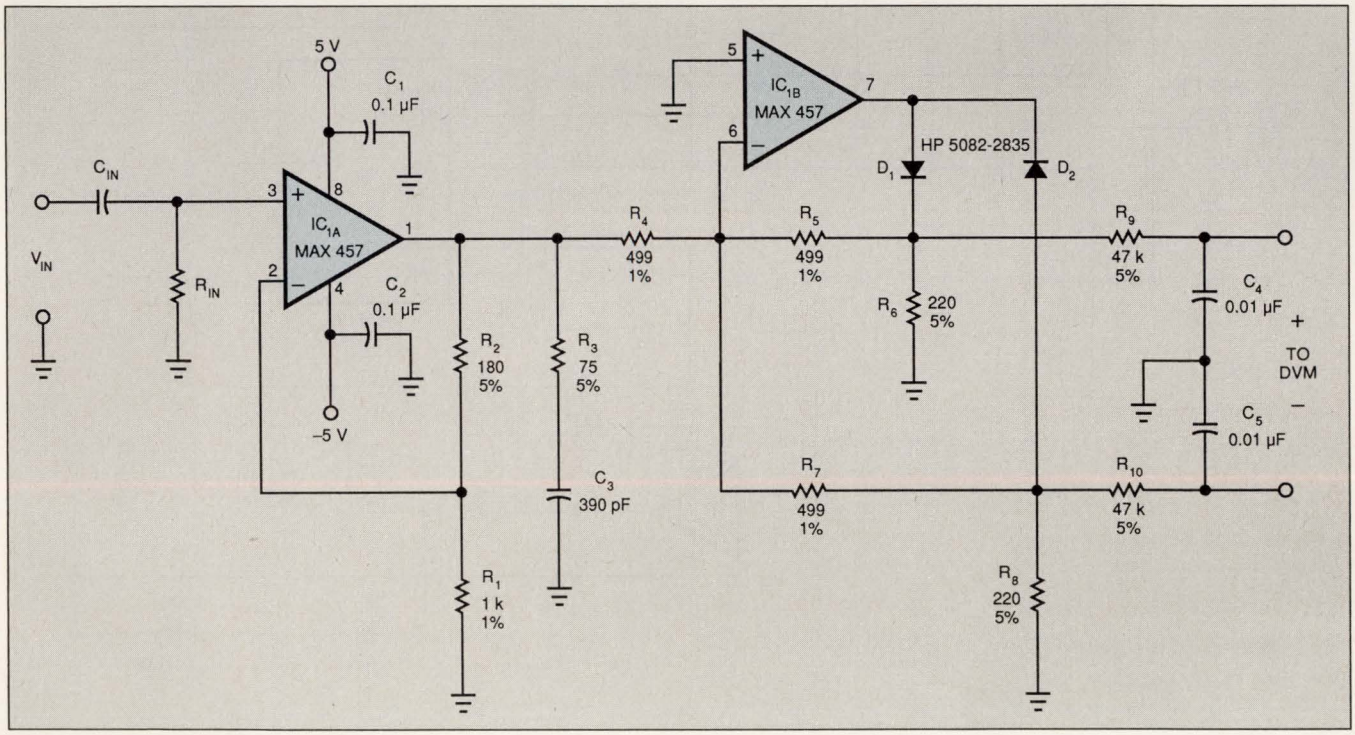

***Fig 1—This active-rectifier circuit converts** pure sine waves to equivalent dc levels with 1% accuracy at frequencies as great as 10 MHz.*

Dynamic mixer performs unusual function

Mark Anglin
Novar Electronics Corp, Barberton, OH

The dynamic mixer in **Fig 1** combines two audio inputs by adding the primary signal, Input A, to a gain-controlled signal, Input B. The unusual aspect of this circuit is that the average voltage level of Input A controls the gain of Input B.

IC_1 has the averaging function and many of the specialized gain blocks that the circuit requires. R_1 sets the level of the primary input, Input A, to be passed to the output. R_2 governs Input B's level to the modulator, while R_3 sets the level of the modulating signal. IC_1 can be either a NE571N or a NE570N. The average ac signal at pin 2 controls the amount of signal that shows up at IC_1's output, pin 3.

The primary signal gets to IC_2, a NE5534N low-noise op amp, via C_1 and R_7; the gain-modulated secondary signal arrives via pin 5 of IC_1. IC_2 sums the two signals.

Potentiometers R_4 and R_6 make dc-offset and distortion adjustments, respectively. IC_3, C_7, R_{14}, R_{15}, D_1, and D_2 form a filter for IC_1. Volume 1 of the 1987 Signetics Linear Data Manual describes this filter in detail. EDN

To Vote For This Design, Circle No. 747

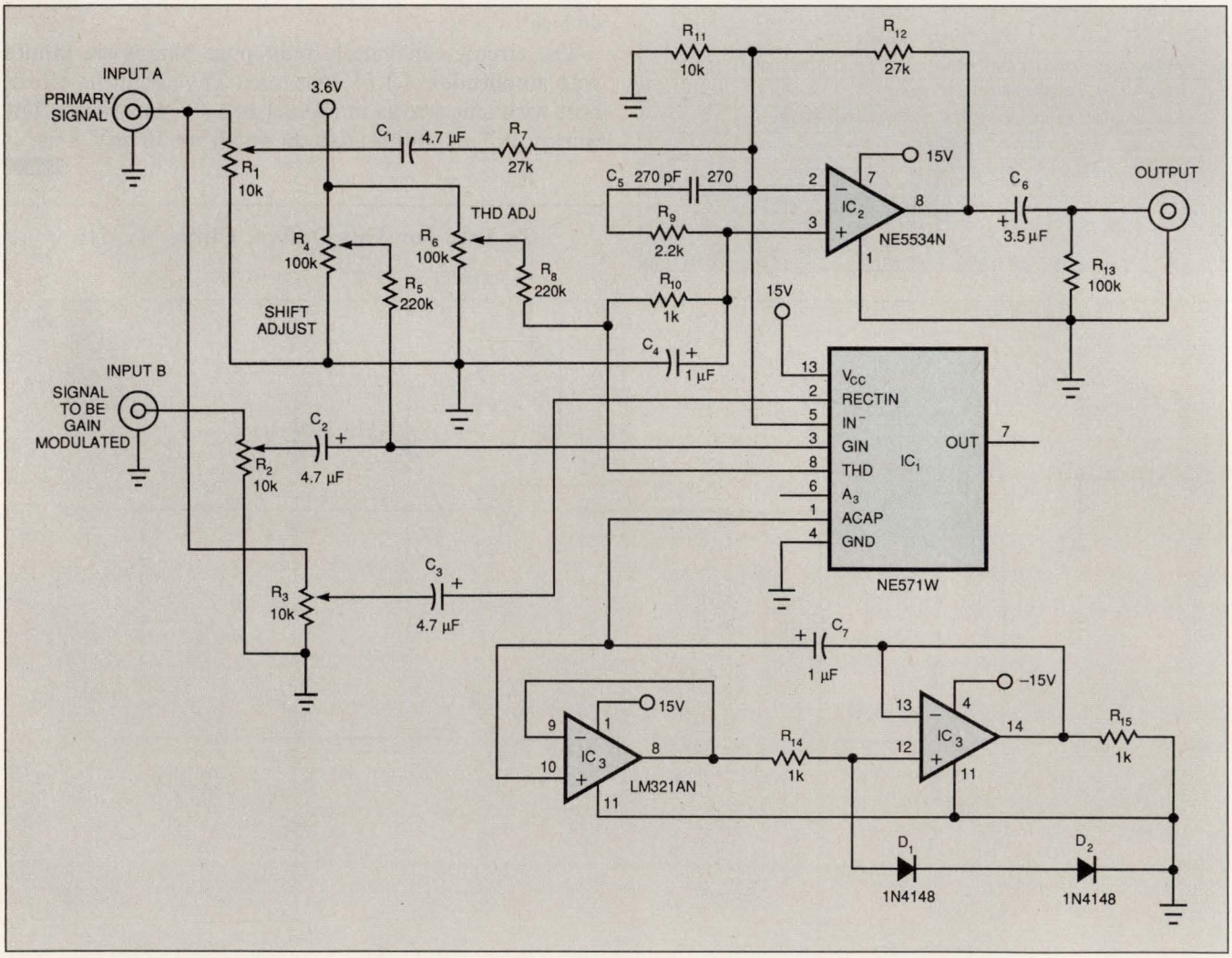

Fig 1—This circuit mixes a gain-modulated signal, *Input B, with the gain-modulating signal, Input A.*

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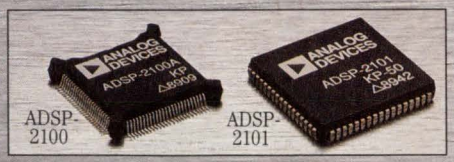

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ANALOG DEVICES

Programmable amp provides arbitrary gain

Tarlton Fleming
Maxim Integrated Products, Sunnyvale, CA

The programmable-gain instrumentation amplifier in **Fig 1** ensures that your A/D converters will always see signals in the upper half of their input-signal range. The channel-select signals to IC_1 also automatically set that channel's gain via IC_2.

Table 1 lists the gains for each channel. With this design, channel 1's gain is necessarily unity. But the other channels can have any reasonable gain value, not just the binary ratios in **Table 1**.

To determine resistor values, begin by choosing an arbitrary value for R_4, such as 5 kΩ. Using the binary values in **Table 1** as an example, for a gain of 8, the total resistance, R_T, would be 40 kΩ. If $R_3+R_4+R_5=10$ kΩ, then $R_3+R_5=5$ kΩ. Setting R_3 and R_5 equal, $R_3=R_5=2.5$ kΩ. Similarly, $R_2=R_6=5$ kΩ, and $R_1=R_7=10$ kΩ.

Note that this 1-to-4 resistor range suits a custom resistor network. Note also that IC_2's switch resistances ($r_{DS(ON)}$) contribute virtually no voltage error because they conduct no signal current. Leakage currents cancel to some degree; therefore, errors arising from leakage depend primarily on the differential leakage currents. For example, if S_{1A} has 1 nA of leakage current and S_{1B} has 0.9 nA, then only the 0.1-nA difference current flowing in the gain-setting resistors would cause errors.

Table 1—Resistor ratios

Channel	Switches Closed	Desired Gain	Formula
1	S_{1A}, S_{1B}	1=	R_T/R_T
2	S_{2A}, S_{2B}	2=	$R_T/(R_2+R_3+R_4+R_5+R_6)$
3	S_{3A}, S_{3B}	4=	$R_T/(R_3+R_4+R_5)$
4	S_{4A}, S_{4B}	8=	R_T/R_4

Note: R_T =total resistance.

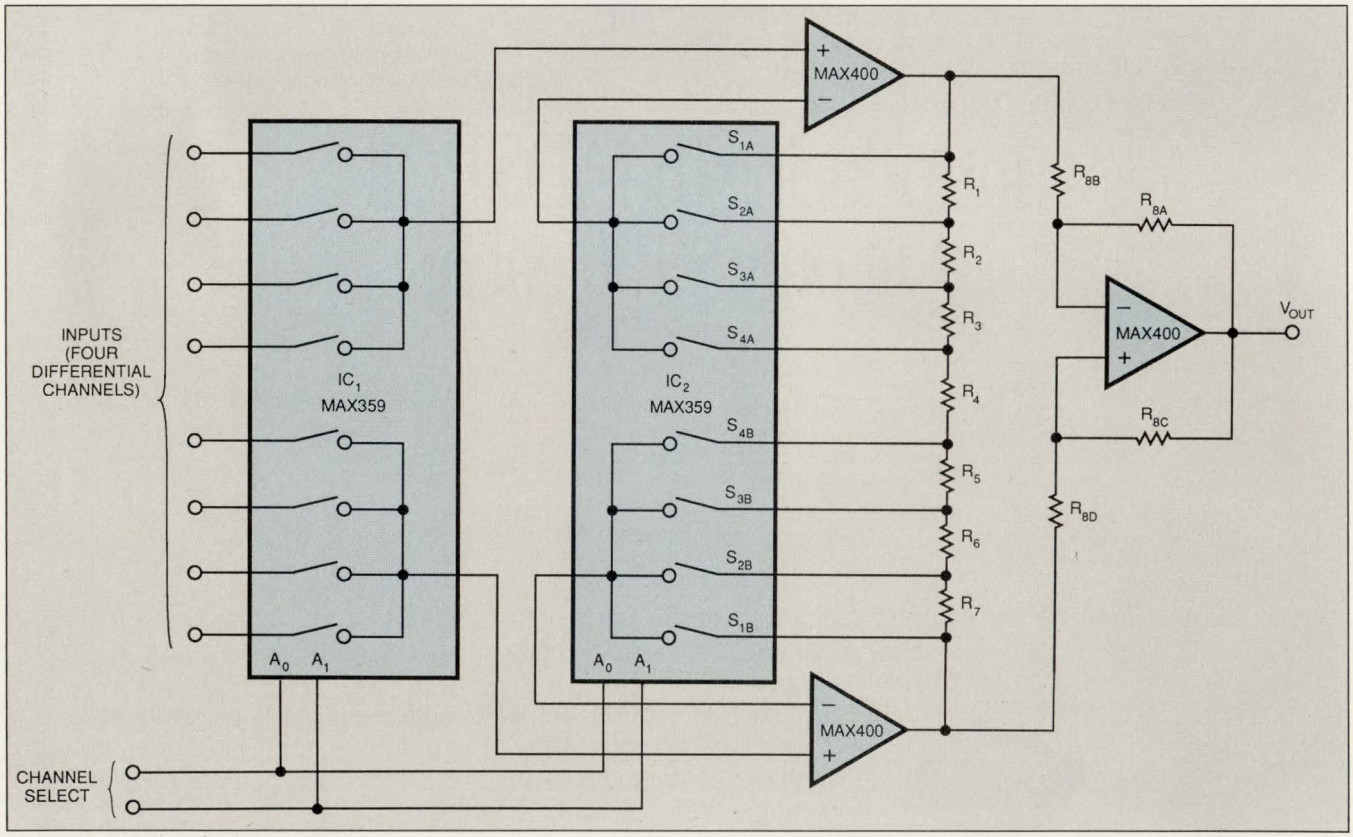
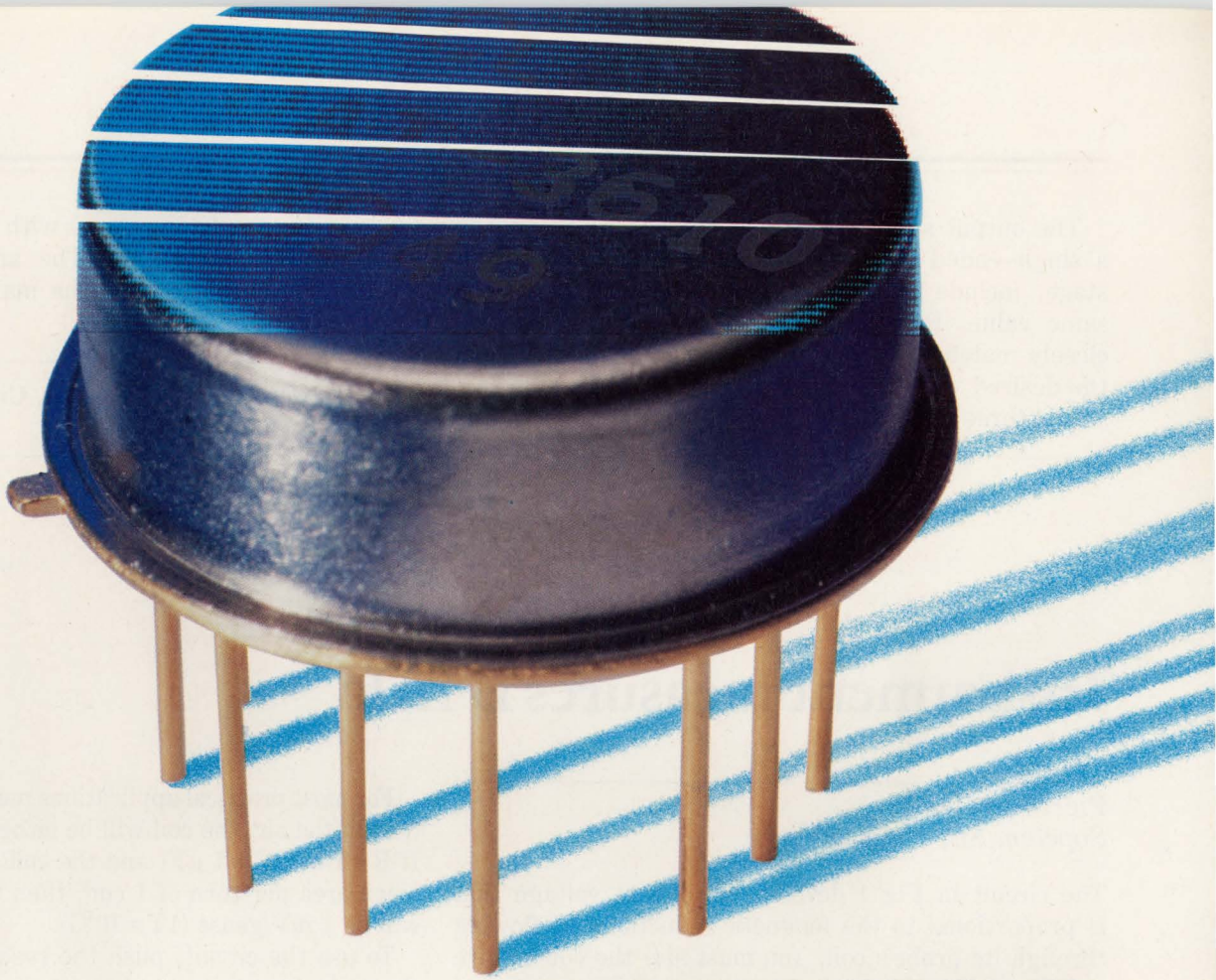


Fig 1—This instrumentation amplifier, *which comprises IC_2 and the three op amps, automatically sets one of four arbitrary gain levels for each input channel selected. Resistors R_1 through R_7 determine the gain of each channel.*



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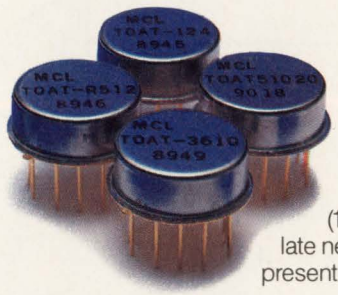
0.5	**0.12**	**1.0**	**0.2**	**3.0**	**0.3**	**5.0**	**0.3**
1.0	**0.2**	**2.0**	**0.2**	**6.0**	**0.3**	**10.0**	**0.3**
1.5	0.32	3.0	0.4	9.0	0.6	15.0	0.6
2.0	**0.2**	**4.0**	**0.3**	**10.0**	**0.3**	**20.0**	**0.4**
2.5	0.32	5.0	0.5	13.0	0.6	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	30.0	0.7
3.5	0.52	7.0	0.7	19.0	0.9	35.0	1.0

bold faced values are individual elements in the units



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CIRCLE NO. 110

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The output stage converts the differential signal to a single-ended output. For unity gain in the output stage, include four closely matched resistors of the same value, R_{8A} through R_{8D}. For other gains, use closely matched ratios R_{8A}/R_{8B} and R_{8C}/R_{8D} that equal the desired value.

The three op amps should combine precision (low I_B, I_{OS}, and V_{OS}, and high A_{VOL}) with as much speed as your application requires. The amplifiers' common-mode range should exceed the maximum signal level by at least two volts. EDN

To Vote For This Design, Circle No. 748

Instrument measures B field

Pierre Breteau
Sopelem SL, Paris, France

The circuit in **Fig 1** develops an output voltage that is proportional to the magnetic induction, **B,** flowing through its probe's coil. You must size the coil to give a full-scale, 10V output for your maximum expected magnetic-induction intensity.

For a given value of **B** (in tesla) and output voltage, V_{OUT},

$$B = (R \cdot C \cdot V_{OUT})/A,$$

where A is the effective area of your coil in m^2 (A = number of turns × average area of each turn), R is the resistance of the coil and the probe, and C is the value of the capacitor. Note that C should be a low-leakage polypropylene or Teflon device.

For most practical applications measuring a magnetic field in the air, the coil will be either tiny or very thin. If R = 1 kΩ, C = 1 μF, and the coil is 100 turns with a mean area per turn of 1 cm^2, then the circuit's output will be 1 mV/gauss (1T = 10^4G).

To use the circuit, push the reset button and place the probe in an area you know to be devoid of magnetic fields. Be sure to avoid magnets and iron. Then put the probe into the field to be measured and read the V_{OUT} with a voltmeter. Finally, calculate the **B** field's intensity using the equation.

When constructing the instrument, guard the op amp's inputs to avoid undesirable currents at the minus input. For full-scale outputs, use a ±15V supply for the op amp. EDN

To Vote For This Design, Circle No. 749

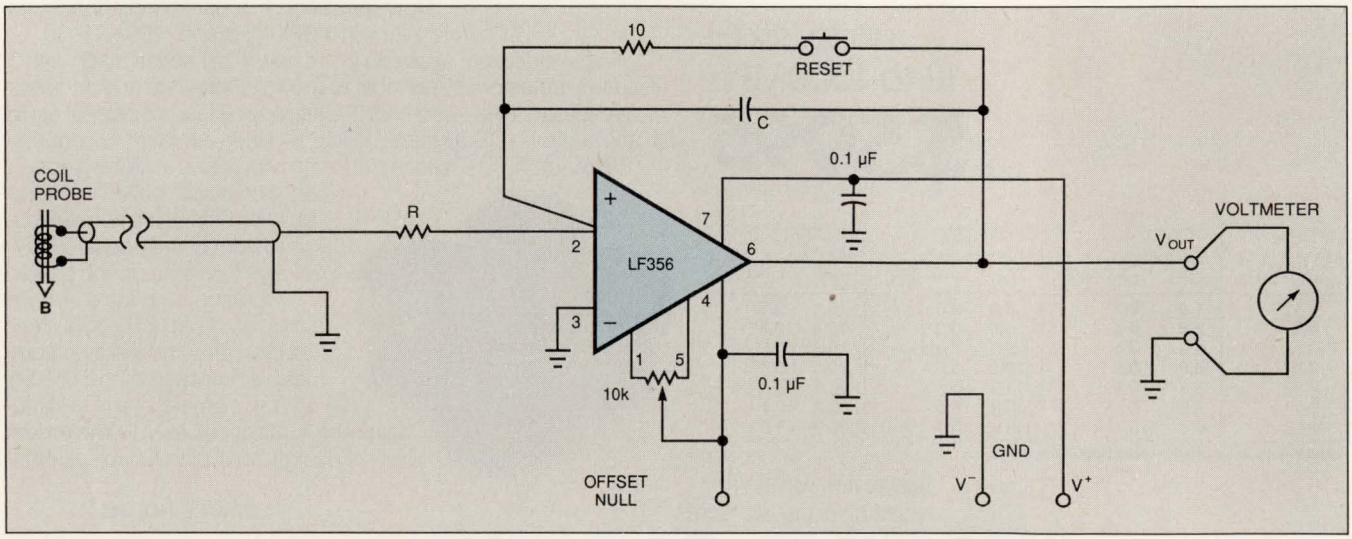

***Fig 1—This simple instrument measures** magnetic induction, **B**.*

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HP-28 program engenders elliptic filter

David Báez-López and Eduardo Olguin-Osorno
University of the Americas, Puebla, Mexico

Given the passband frequency (rad/sec), stopband frequency (rad/sec), passband ripple (dB), and order (number of poles), the program in **Listing 1** will determine the poles and zeros for an elliptic lowpass filter. The program runs on a Hewlett-Packard HP-28S calculator. EDN

To Vote For This Design, Circle No. 750

Listing 1—HP-28S elliptic lowpass-filter program

```
MAIN
« CLLCD RAD STD
"     Elliptic Filter"
1 DISP
"          Evaluation"
2 DISP
"       Low-Pass Case"
3 DISP 3 WAIT CLMF {
STO N WC WS AMX }
MENU HALT '√(WS/WC)'
EVAL 'A0' STO 'WC*A0
' EVAL 'KTE' STO 4
AS 'A4' STO '2^(N-1)
*A4^N' EVAL 'J4' STO
J4 'JX' STO 4 JS
'J0' STO '-10*LOG(
INV((INV(ALOG(-AMX/
10))-1)*J0^4+1))'
EVAL 'AMI' STO '√(
INV(ALOG(-AMX/10))-1
)' EVAL 'KA' STO
CLLCD
"The value of Amin is →
"
2 DISP AMI 3 DISP
HALT CLMF CLLCD
" Evaluating Zeros .."
2 DISP ZER CLLCD
" The zeros are → "
2 DISP 3 WAIT CEROS
ARRY→ DROP CLMF HALT
CLLCD
" Evaluating Poles .."
2 DISP POLOS CLLCD
"    The poles are → "
2 DISP 2 WAIT CLMF
CLEAR 6 FIX POLS
ARRY→ DROP HALT CLMF
CLLCD
"        END OF PROGRAM"
4 DISP CLMF CLR
CLEAR
»
```

```
ZER
« STD 'EP(N/2)' EVAL
'SI' STO
  IF SI 0 >
  THEN 'N-2' EVAL
'NN' STO
  ELSE 'N-1' EVAL
'NN' STO
  END NN 0
  FOR K 'A4/COS(K*π/
(2*N))' EVAL →NUM
'XY' STO 3 0
    FOR J J AS 'AZ'
STO 'INV(2*AZ)*(XY+
INV(XY))' EVAL 'XY'
STO -1
    STEP XY Σ+ -2
  STEP 'ΣDAT*KTE'
EVAL 'CEROS' STO {
ΣDAT } PURGE
»


POLOS
« CLEAR 'CEIL(N/2)'
EVAL 'L' STO 'L-1'
EVAL 'L1' STO 'INV(
J0*KA)' EVAL 'SX0'
STO 4 1
  FOR K K JS 'JX'
STO 'JX*SX0+√((JX*
SX0)^2+1)' EVAL
'SX0' STO -1
  STEP '(J4/SX0+√((
J4/SX0)^2+1))^INV(N)
' EVAL 'E50' STO
  IF SI 0 <
  THEN 'π/2' →NUM
'C' STO
  ELSE 0 'C' STO
  END 0 L1
  FOR E '(C+E*π)/N'
EVAL →NUM 'DB' STO
E50 DB R→C P→R 'EX'
STO 4 0
    FOR K K AS 'AZ'
STO 'INV(2*AZ)*(EX-
INV(EX))' EVAL 'EX'
STO -1
    STEP EX
  NEXT L →ARRY 'POL'
STO 'POL*KTE' EVAL
'POLS' STO
»
```

```
AS
« → N 'IFTE(N≠0,A0,
AS(N-1)^2+√(AS(N-1)^
4-1))'
»

JS
« → N 'IFTE(N≠0,J4,√
(.5*(JS(N-1)+INV(JS(
N-1)))))'
»

CLR
« { POLS POL EX DB
L1 C E50 SX0 L CEROS
AZ XY NN SI KA AMI
J0 JX J4 A4 KTE A0
AMX WS WC N } PURGE
»
```

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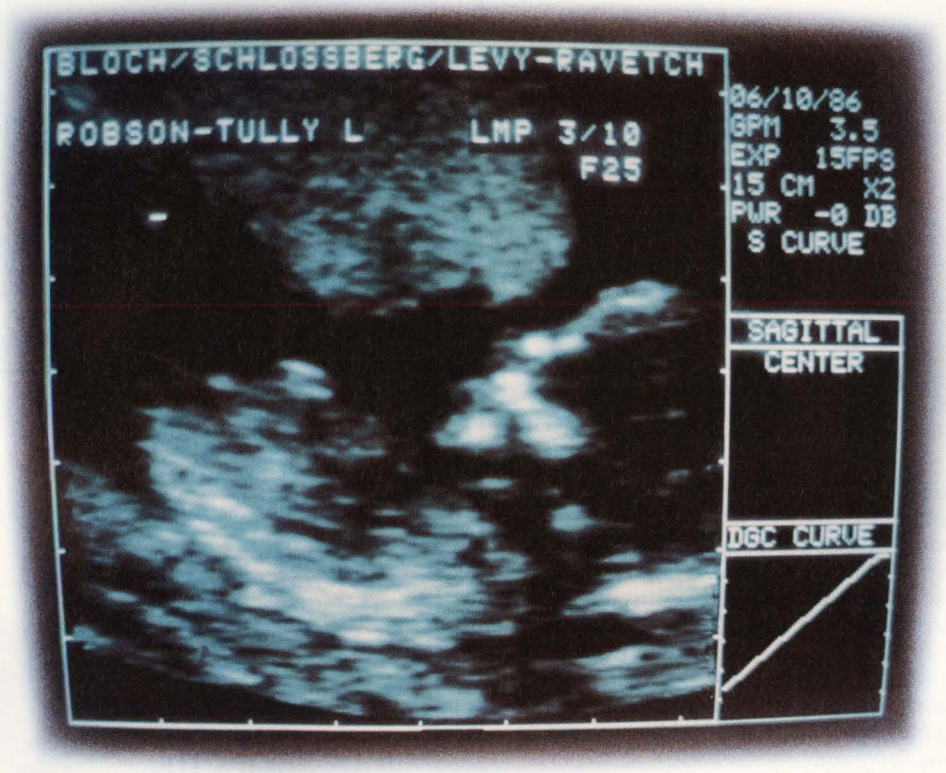

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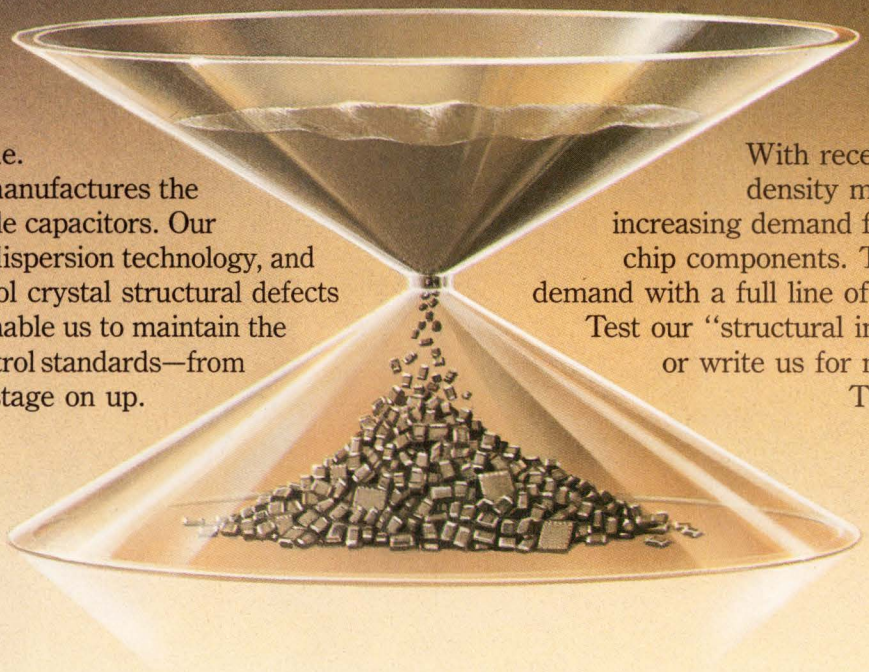

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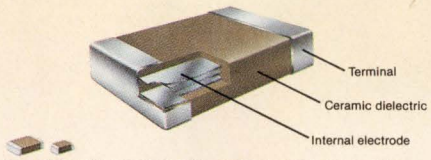

C1608 (CC0603) C: 0.5 ~ 220,000pF
C2012 (CC0805) C: 0.5pF ~ 1μF
C3216 (CC1206) C: 0.5pF ~ 2.2μF
C3225 (CC1210) C: 750pF ~ 3.3μF
C4532 (CC1812) C: 2,400pF ~ 1μF
C5650 (CC2220) C: 5,100pF ~ 1.5μF

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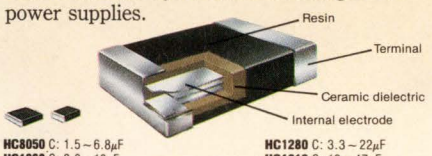

HC8050 C: 1.5 ~ 6.8μF
HC1063 C: 2.2 ~ 10μF
TC: +20, −30% (−25 ~ +85°C)
HC1280 C: 3.3 ~ 22μF
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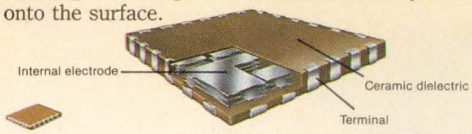

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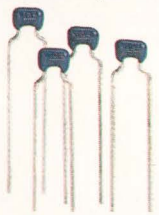
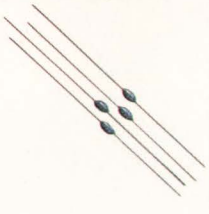


Multilayer Ceramic Dipped Axial Lead Capacitors



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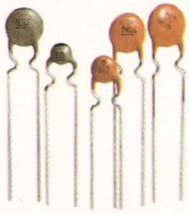

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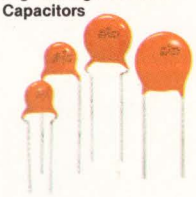

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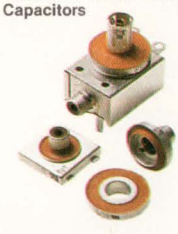

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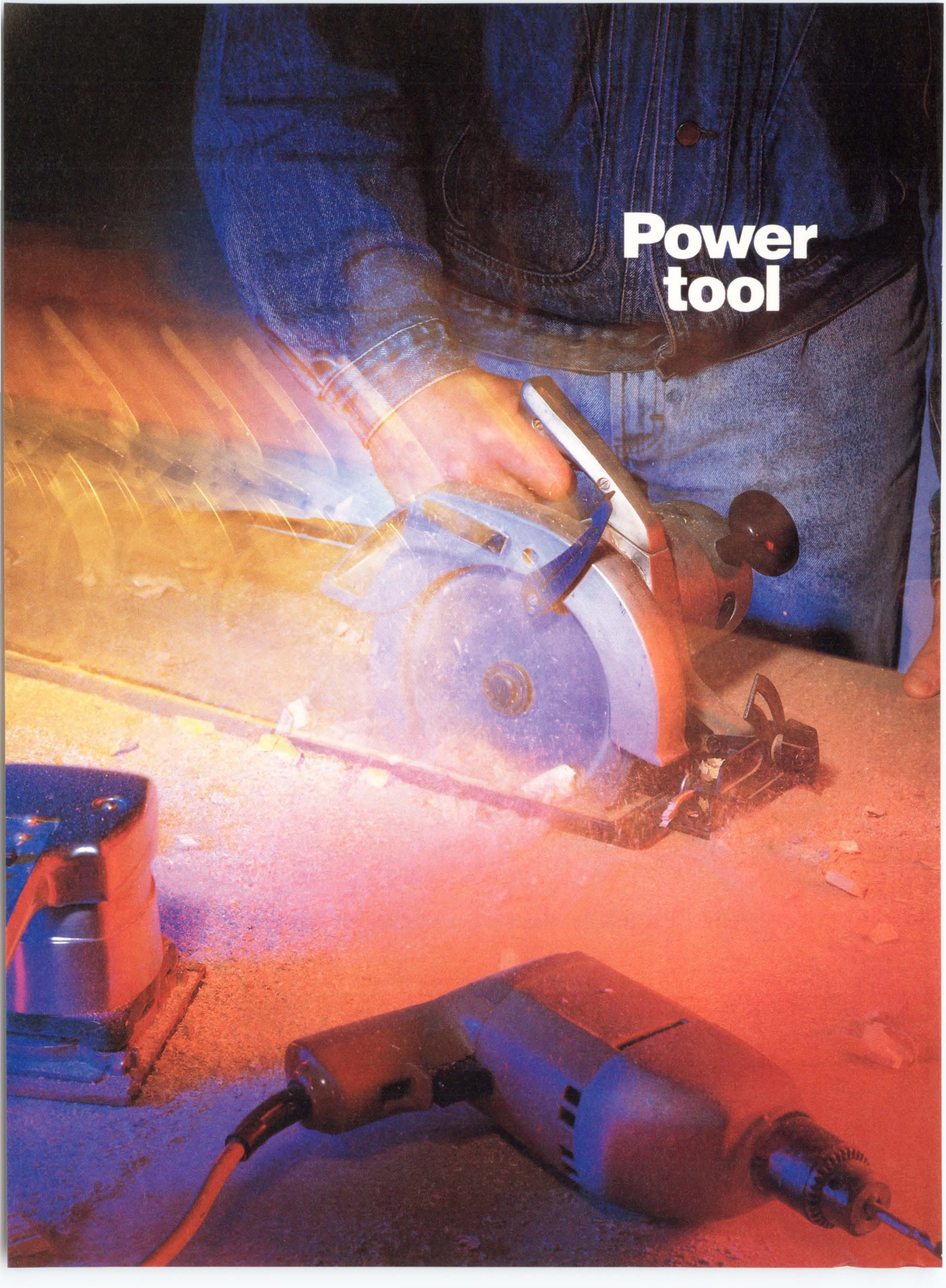
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Power tools

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Choose your tools carefully for the work at hand. Choose a single unit ATE power supply and drive it with an SN digital analog interface to translate GPIB commands to useful voltage and current or choose a multiple-unit TMA-MAT system and drive up to 27 independent voltages and currents from a single GPIB address with full status monitoring and read back of actual values.

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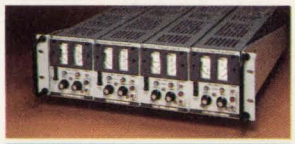

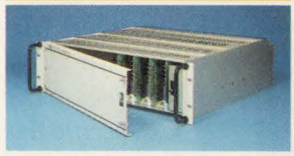

dc, unipolar power

- ☐ Listen only, GPIB
- ☐ 12 bit control, 0-6V to 0-325V, unipolar dc
- ☐ Power: 50W, 100W, 250W, 500W, 1000W
- ☐ Control one, four or eight units, analog drive

SN/ATE

dc, bipolar power

- ☐ Listen only, GPIB
- ☐ 12 bit control ± 20V to ± 200V bipolar dc
- ☐ 100W, 200W, 400W
- ☐ Single unit, self-contained

BIT/BOP

dc, unipolar power

- ☐ Listen, talk-verify, GPIB
- ☐ 12 bit control, 0-6V to 0-325V unipolar dc
- ☐ Power: 50W, 100W, 250W, 500W, 1000W
- ☐ Control one to sixteen units, analog drive

TLD/ATE

dc (selectable polarity) power

- ☐ Talk-listen, GPIB, full read back of both voltage and current
- ☐ 12 bit control, 0-6V to 0-150V Unipolar dc with polarity selection
- ☐ Power: 360W, 720W, 1080W
- ☐ 1-27 unit control, digital (bit-bus) drive

TMA/MAT

ac power

- ☐ Talk-listen, GPIB
- ☐ 12 bit control, 0-125V ac 47-2000Hz ac power
- ☐ 1KVA to 18KVA
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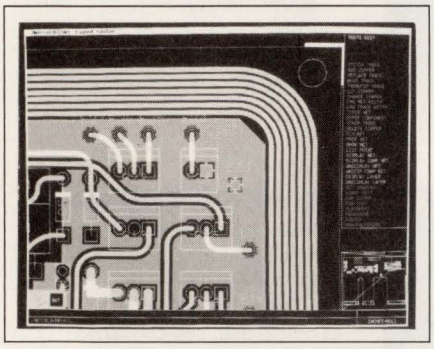


Enhanced Layout System For Sun And Apollo

- *Lets you create curved traces and copper areas*
- *Provides an IGES 3.0 interface for integration with other systems*

Release 4.2 of Omnicards is a greatly enhanced version of the vendor's pc-board layout and autorouter package that runs on Sun-3, Sun-4, SPARCstation, and Apollo workstations. New features that help analog designers include the ability to use curved traces to reduce analog effects on high-speed ECL circuits, and fully automatic copper-area creation with auto-clearing and auto-fill. An enhanced, 32-bit layout database lets you specify English or metric working units or multiple units of measure. The database also gives you precision layouts with sub-micron resolution for technologies that use lines finer than 0.004 in. An improved autorouter reduces the number of vias used by 5 to 15%. An optional, bidirectional IGES 3.0 interface program lets you offload graphics data to mechanical-design and thermal-analysis programs. In addition, bidirectional net-list interfaces let you exchange data with Teradyne/EDA and Data I/O (FutureNet) schematic-capture systems. Omnicards interactive design software costs $12,000.

Task Technologies Inc, 6 N Main St, Suite 235, Fairport, NY 14450. Phone (716) 377-1060. FAX (716) 377-6611. **Circle No. 384**

Enhanced Modeling Program

- *Lets you optimize parameters for specific devices*
- *Includes new features to model bipolar quasi-saturation effects*

Release 3.1 of the Suxes 20 device-modeling and -optimization program automatically provides initial parameter values for the bipolar model; these values are based on linear extrapolation from measured data. You can use sequential parameter optimization to organize one region at a time, or global parameter-optimization for all regions of device operation. In addition, a new bipolar model allows the modeling of quasi-saturation effects. A new grouping function lets you dynamically select a group of targets, data files, and sorting and weighting strategies for application to a particular parameter optimization. Suxes 20 version 3.1 comes bundled with EXModeler for macro modeling and the PLUS option for driving test equipment. $35,000.

Electrical Engineering Software Inc, 4675 Stevens Creek Blvd, Suite 200, Santa Clara, CA 95051. Phone (408) 296-8151. FAX (408) 296-7563. **Circle No. 385**

Multichip-Module Design Tool

- *Lets you use any of current manufacturing technologies*
- *Includes sophisticated floor-planning tools*

Allegro-MCM is a package that facilitates the design of multichip modules. It includes schematic-capture and logic-simulation facilities, high-speed layout capability, and in-process analyses. The system lets you use any of the current technologies for manufacturing multichip modules. Allegro-MCM adheres to specific design rules for each process, and allows you to switch from one process to another so that you can base your decisions on the tradeoffs between the cost, size, and performance of each technology. When you've completed your design, the program provides an output format that's appropriate to the manufacturing process—Gerber format for pc-board-like processes or GDSII format for IC-like processes. The package includes floor-planning tools to help you produce a modular design; component-clustering and -placement rules partition the design to produce a compact, efficient, and routable layout. In-process analysis tools give instant readings of propagation delays and other parameters. You can also use the vendor's Signal Noise Analysis tool to identify nets with excessive reflections, crosstalk, thermal drift, and ohmic loss. From $50,000.

Valid Logic Systems, 2820 Orchard Pkwy, San Jose, CA 95134. Phone (408) 432-9400. FAX (408) 432-9430. **Circle No. 386**

Stimulus Generator

- *Facilitates stimulus generation and control for circuit design*
- *Adds pattern data to timing specifications for test programs*

The WaveMaker interactive graphics tool can create pattern and timing data for generating stimulus during circuit design; can add timing data to pattern data for μP development; and can combine pattern and timing data for interactive test-program development. The program uses four interactive graphics editors that operate on a common object-oriented database. The program can accept data from multiple sources such as simulation runs, existing circuits and test programs, files that you create, or data generated by hardware modelers. WaveMaker can then generate input data

CAE & SOFTWARE

for logic and fault simulators, logic analyzers, component testers, in-circuit board testers, and functional board testers. The program runs on Sun and Apollo computers. From $10,000/copy (5).

TSSI, 8205 SW Creekside Pl, Beaverton, OR 97005. Phone (503) 643-9281. **Circle No. 387**

Enhanced Analog Simulator

- *Provides a real-time waveform viewer*
- *Includes new libraries of thyristors and Harris op amps*

PSpice version 4.04 is a greatly enhanced version of the vendor's analog simulator. Among the new features are a real-time waveform viewer, for the OS/2 version, that lets you view output waveforms while a simulation is running; a library file of more than 400 SCR and Triac thyristors; a library file of seven Harris op amps; virtual-memory capability for the DOS/16M version; and an optimizer for parts that give more accurate model parameters. In addition, the expression-handling routines for ac analysis can now perform complex arithmetic. $950 to $29,900 depending on your host computer and the options you select.

MicroSim Corp, 20 Fairbanks, Irvine, CA 92718. Phone (800) 245-3022; in CA, (714) 770-3022. FAX (714) 455-0554. **Circle No. 388**

ASIC Design System

- *Modifies designs to guarantee testability*
- *Automatically generates test patterns*

Version 2.0 of the SilcSyn ASIC Design System is enhanced to provide multilevel synthesis and optimization, automatic test synthesis and test generation, and integrated simulation for rapid design verification from ASIC design through the board and system levels. New fea-

tures let you enter behavioral descriptions for architectural synthesis and optimization before logic synthesis; let you enter net lists and register-transfer-level descriptions for logic synthesis; and have the system automatically modify your design to guarantee testability, as well as automatically generate test patterns. In addition, you can now use either VHDL or the enhanced SilcSyn Design Description Language for behavioral and structural descriptions. Also, the EDIF interface allows you to import structural net lists from other systems. $30,000 to $50,000, depending on the host-computer configuration.

Racal-Redac Corp, 238 Littleton Rd, Westford, MA 01886. Phone (508) 692-4900. **Circle No. 389**

Mixed-Level Simulator

- *Simulates multiple coupled transmission lines*
- *Performs mixed-level, mixed-mode simulation*

ContecSPICE provides mixed-level, mixed-mode simulation that lets you simulate some parts of your design at the behavioral level and other parts at the transistor level. The program uses special algorithms that can handle large numbers of coupled transmission lines 125 times (or more) faster than other methods; these algorithms are also very economical in their memory usage. A model-parameter generator program comes with a library of 2500 devices; it also lets you generate model parameters directly from information that you input from a data sheet with the aid of a digitizing tablet. The interactive user interface lets you define new model topology, as well as equations, at any level from a transistor to a large functional macro. Simulator and model-parameter generator for IBM PCs and compatibles, $1998; for Sun workstations, $5419.

Contec Microelectronics Inc, CAE Div, 2010 N First St, Suite 530, San Jose, CA 95131. Phone (408) 436-0340. **Circle No. 390**

OCR Software For PCs

- *Runs under Windows 3.0 on 80286/386-based machines*
- *Throughput as high as 700 words per minute*

WordScan and WordScan Plus are optical-character-recognition software packages that run on 80286/386-based IBM PCs, PS/2s, and compatibles that have at least 2M bytes of main memory. Both programs provide omnifont recognition of hard copy and can recognize dot-matrix fonts in draft mode (including fax output). They have a preview mode for checking the quality of the scanned image before beginning the recognition process; an editor for proofing recognition; and the ability to defer the processing of documents. WordScan Plus also has a pop-up image verifier that puts on the screen an enlarged original bit-map image of questionable characters and words so that you can proof them without referring to the original document. A clipping feature lets you view scanned images and place a line around only those areas of the page that you want to retain. The multijob feature lets you process multiple documents in one step and create a separate file for each document. The style-sheet feature lets you reformat the input document to your preferred style, overriding the original format. WordScan, $595; WordScan Plus, $995.

Calera Recognition Systems Inc, 2500 Augustine Dr, Santa Clara, CA 95054. Phone (408) 986-8006. FAX (408) 986-1440.

Circle No. 391

NEW PRODUCTS

COMPONENTS & POWER SUPPLIES

Board Headers/Receptacles

- *Available in polarized and nonpolarized versions*
- *Compatible with surface-mount processes*

The nonpolarized versions of Series A025 and A026 right-angle receptacles mate to standard unshrouded headers in either single- or dual-row designs. Polarized versions mate with straight headers and are available in dual-row styles. All accommodate perpendicular, horizontal, and parallel interconnection schemes. Right-angle receptacles, in sizes with 4 to 130 contacts, feature a staggered mating depth, high-temperature plastic housings that are compatible with surface-mount processes, a built-in pin stop to prevent shorting of connector rows, and a longer back row of solder tails to ease insertion into pc boards. A026 right-angle polarized receptacles and the mating A038-Series shrouded headers are available in 8- to 130-pin versions, and feature molded-in polarization slots and pins for error-free and blind mating capability. Gold and tin-lead platings are standard. $0.04 per mated position. Delivery, stock to five weeks ARO.

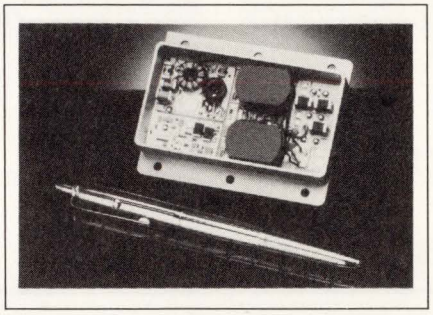
Augat Inc, Interconnection Products Div, 33 Perry Ave, Attleboro, MA 02703. Phone (508) 222-2202. **Circle No. 351**

IC Sockets

- *Feature an open-frame design*
- *Have dual wipe contacts*

The high-compression, dual-wipe design of the spring contacts in GASF-Series IC sockets ensures a gas-tight connection. They have an open-frame insulator design that facilitates board cleaning, improves pc-board cooling, and eases inspection. The sockets feature phosphor bronze stamped and formed contacts. The standoffs, which are built into the side of each socket, keep the pins from sealing off the plated-through holes in the pc board and thereby eliminate gas-entrapment problems. A closed-bottom design prevents solder wicking and flux entrapment. The sockets have a large target area to ease the IC entry process. They are available in widths of 0.300 and 0.600 in. and are end-to-end and side-by-side stackable. 20-pin version, $0.12 (5000).

Garry Electronics, 9 Queen Anne Ct, Langhorne, PA 19047. Phone (215) 949-2300. FAX (215) 943-8742. **Circle No. 352**



Military DC/DC Converters

- *Feature 0.05% regulation*
- *Develop 60W output power*

PWR82400-Series devices are full MIL-processed 60W dc/dc converters with a characterized output from −55 to +125°C. Built in a MIL-STD-1772 certified facility, the converters include element evaluation, 883B design and construction guidelines with full environmental screening, burn-in testing, and full-temperature testing as standard processing. The converters accept inputs of 16 to 40V and supply three outputs: ±15V at 1.33A and 5V at 4A for 82400 versions; ±12V at 1.7A and 5V at 4A for 82402 models. Input-to-output isolation equals 500V dc, and main-output line regulation equals 0.05%. Separate output returns let you power sensitive analog circuitry while maintaining digital signal isolation. Pulse-by-pulse current-limiting circuitry, which monitors output load, protects the converters from short circuits. From $898. Delivery, stock to 90 days ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. FAX (516) 567-7358. **Circle No. 353**

Solid-State Relays

- *Have a FET output*
- *Will switch 1.75A*

The C46F/C47F-Series commercial solid-state relay line includes dc switching versions with output current ratings as high as 1.75A and bipolar versions that will switch 1A ac or dc loads. Output voltage ratings for both types span a 50 to 360V range. Relay design features an optically coupled, photovoltaic generator, which drives output FETs that feature low on-resistance and fast response time. Internal construction utilizes thick-film hybrid microcircuit technology with a patented lead frame design. From $6.10 (OEM qty). Delivery, stock to six weeks ARO.

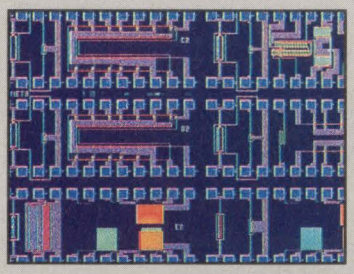
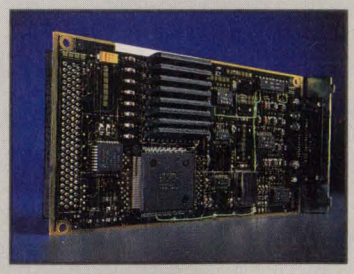
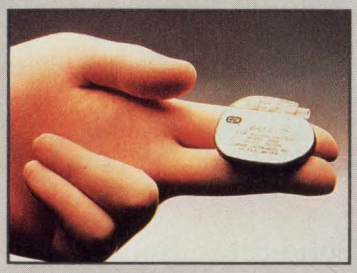
Teledyne Solid State, 12525 Daphne Ave, Hawthorne, CA 90250. Phone (213) 777-0077. FAX (213) 779-9161. **Circle No. 354**

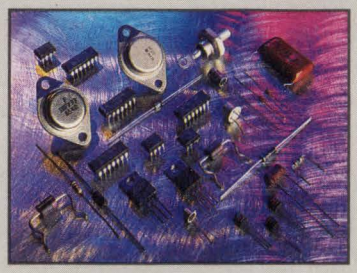
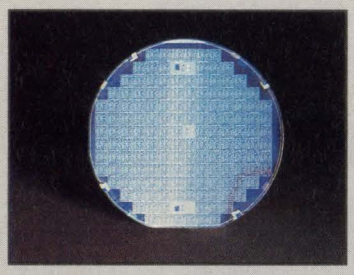
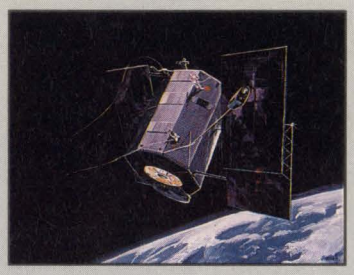
D Subminiature Connectors

- *Have gold plating*
- *Feature a sealed back*

These right-angle D-subminiature connectors all have a tin-plated metal shell for shielding purposes. The units are available in four families. The first features 0.318-in. footprint sockets and plugs in 9-, 15-, 25-, and 37-position versions; the second family features 0.590-in. footprint sockets and plugs in identical position options. These units

Text continued on pg 191

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LINEAR TECHNOLOGY

DESIGN NOTES

Number 39 in a series from Linear Technology Corporation *September, 1990*

Low Power CMOS RS485 Transceiver

Robert Reay

Introduction

The EIA RS485 data transmission standard has become popular because it allows for balanced data transmission in a party line configuration. Users are able to configure inexpensive local area networks and multi-drop communication links using twisted pair wire and the protocol of their choice.

Previous RS485 transceivers have been designed using bipolar technology because the common mode range of the device must extend beyond the supplies and be immune to ESD damage and latchup. Unfortunately, the bipolar devices draw a large amount of supply current and are unacceptable for low power applications. The LTC485 is the first CMOS RS485 transceiver featuring ultra low power consumption (I_{CC} = 500μA max.) without sacrificing ESD and latchup immunity.

Proprietary Output Stage

The LTC485 driver output stage of Figure 1 features a common mode range that extends beyond the supplies while virtually eliminating latchup and providing excellent ESD protection. Two Schottky diodes SD3 and SD4 are added to a conventional CMOS inverter output stage. The Schottky diodes are fabricated by a proprietary modification to a standard N-well CMOS process. When the output stage is operating normally, the Schottky diodes are forward biased and have a small voltage drop across them. When the output is in the high impedance state and is driven above V_{CC} or below ground by another driver on the party line, the parasitic diode D1 or D2 will forward bias, but SD3 or SD4 will reverse bias and prevent current from flowing into the N-well or substrate. Thus, the high impedance state is maintained even with the output voltage beyond the supplies. With no current flow into the N-well or substrate, latchup is virtually eliminated.

Propagation Delay

Using the test circuit of Figure 4 with only one foot of twisted pair wire, Figures 2 and 3 show the typical propagation delays.

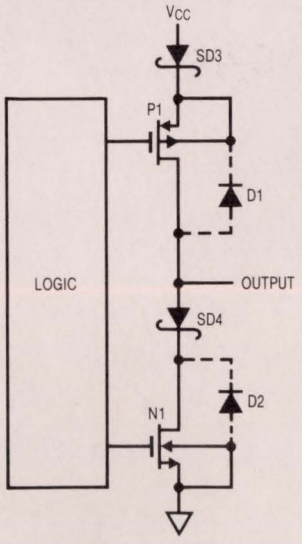

Figure 1. LTC485 Output Stage

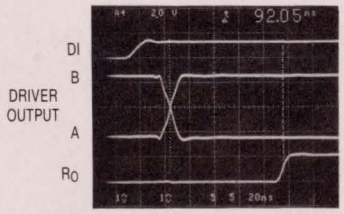

Figure 2. LTC485 System Waveforms

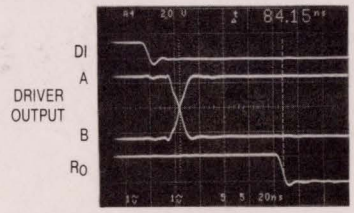

Figure 3. LTC485 System Waveforms

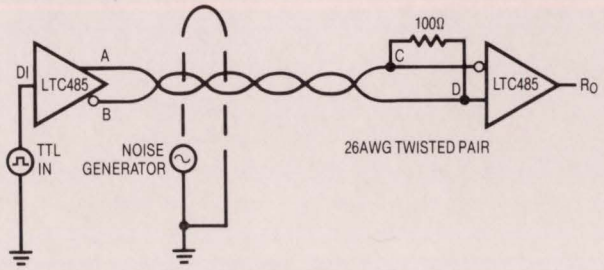

Figure 4. LTC485 System Test Circuit

LTC485 Line Length vs Data Rate

The maximum line length allowable for the RS422/RS485 standard is 4000 feet. Using the test circuit of Figure 4 with 4000 feet of twisted pair wire, Figure 5 and 6 show that with ≈20Vp-p common mode noise injected on the line, the LTC485 is able to reconstruct the data stream at the end of the wire.

Figures 7 and 8 show that the LTC485 is able to comfortably drive 4000 feet of wire at 110kHz.

When specifying line length vs maximum data rate the curve in Figure 9 should be used:

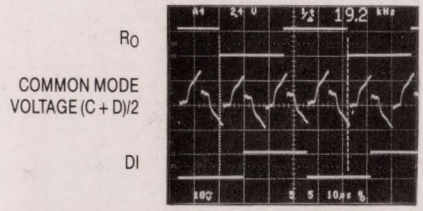

Figure 5. System Common Mode Voltage @19.2kHz

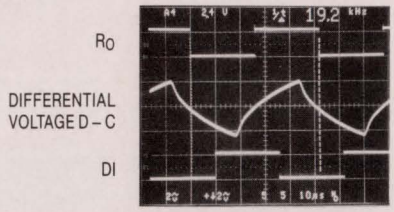

Figure 6. System Differential Voltage @19.2kHz

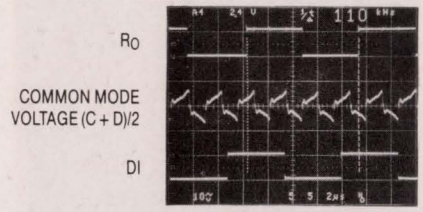

Figure 7. System Common Mode Voltage @110kHz

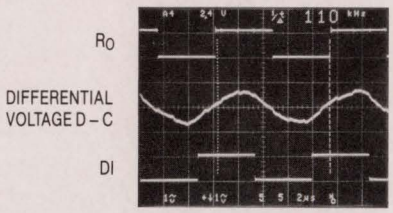

Figure 8. System Differential Voltage @110kHz

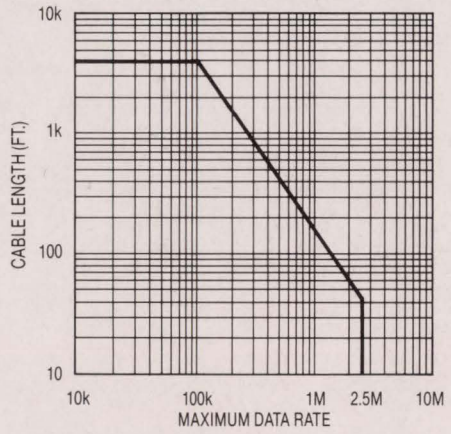

Figure 9. Cable Length vs Maximum Data Rate

For literature of our Low Power Transceivers call **(800) 637-5545.** For applications help, call (408) 432-1900, Ext. 456.

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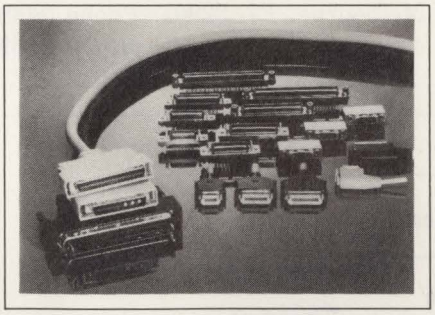
FAX: (408) 434-0507 • TELEX: 499-3977

IM/GP 990 185K

are available with either 10 or 30 μin. of gold plating. The third family features high-density sockets that have 15 positions in a 9-position-size shell. The final family includes stacked designs with two 9-, 15-, or 25-position or 9-over-25-position socket/socket, plug/plug, or plug/socket models. All the devices have sealed backs to protect against solder and flux entrapment. Friction dimples on the male connector's metal face provide ground continuity with the mating connector for effective EMI shielding. Tin-plated solder tails are standard. $1.80 (5000) for a 25-position female connector with 10 μin. of gold plating.

3M Electronic Products Div, Box 2963, Austin, TX 78769. Phone (800) 225-5373. **Circle No. 355**



Connectors

- *Feature high contact density*
- *Offer ESD protection*

DX and 3100-Series connectors feature 0.05-in. contact spacings. The DX line offers as many as 132 positions and features positive locking, terminal protection, and die-cast zinc alloy backshell and receptacle shell to reduce EMI problems. The devices carry 0.5A at 125V ac. Insulation and withstanding voltage figures are 250 MΩ and 300V rms, respectively. Insulators are made of PBT resin, and pin and socket contacts are copper alloy with selective gold plating. Series 3100 I/O connectors are available in 6-, 8-, 12-, 14-, and 16-position versions. They will handle 0.5A at 125V ac. They feature a 94V-0-rated molded shell that provides complete ESD protection. Connector lifetime equals 500 cycles. DX Series, $28 per mated pair for a 132-position version; 3100 Series, $11.75 per mated pair for a 12-position model.

Hirose Electric Inc, 2685-C Park Center Dr, Simi Valley, CA 93065. Phone (805) 522-7958. FAX (805) 522-3217. **Circle No. 356**

Surface-Mount JFETs

- *Can dissipate 1W*
- *Switch off in 6 nsec*

Series PMBFJ108 and PZFJ108 JFETs are housed in surface-mountable SOT23 and SOT223 packages, respectively. The SOT-223 package can dissipate 1W when mounted on a normal pc board and

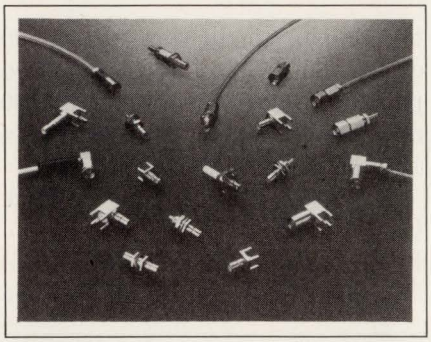
as much as 2W when mounted on ceramic substrates. The devices have an 8Ω max on-resistance and on and off switching times of 4 and 6 nsec, respectively. Standard TO-92 versions are also available, and these units are plug-in replacements for existing types. $1.25.

Philips Components, Box 218, 5600 MD Eindhoven, Netherlands. Phone (40) 724324. FAX (40) 724825. **Circle No. 357**

Coaxial Connectors

- *Handle hostile environments*
- *Available in pc-board-mount versions*

Units in the SMB and SMC lines of RF coaxial connectors feature brass bodies and beryllium-copper center contacts to accommodate the most harsh environments. In right-angle versions, the bodies of the connectors are brazed to ensure a



reliable junction, and the center contacts are laser welded to eliminate problems of reflow during wave soldering operations. The lines include crimp-and-clamp versions for flexible cable applications, panel-mount receptacles, and printed-circuit-board mount styles. $2.37 to $5.52 (OEM qty) for pc-board SMC male connectors.

M/A-COM Omni Spectra Inc, 140 Fourth Ave, Waltham, MA 02254. Phone (617) 890-4750. FAX (617) 890-2381. **Circle No. 358**

Surge Suppressors

- *Handle harsh automotive environments*
- *Rated for 2000A*

V2ML-Series surge suppressors are designed for automotive electronics applications. They are fabricated to absorb externally or internally generated energy surges that might otherwise damage or destroy a system's electronic components. The units are rated for peak currents as high as 2000A, and they have a jump-start overvoltage capability of 24.5V for 5 minutes. Voltage ratings range to 16V. The surface-mount suppressors are available in 1206, 1210, 2220, and 2820 packages. Operating range spans −55 to +125°C. $0.46 (1000) for V24ML1210 units. Delivery, stock to 12 weeks ARO.

Harris Semiconductor, Box 883, Melbourne, FL 32901. Phone (800) 442-7747. **Circle No. 359**

NEW PRODUCTS

COMPUTERS & PERIPHERALS

PC Modems

- *Uses a 2400-bps chip set to transmit at 9600 bps*
- *Have 2400-, 1200-, and 300-bps fallback modes*

The 9624 and the 9624e are modems for PC compatibles that operate internally or externally to the computer, respectively. The modems employ the company's extended-baud-rate (EBR) technology which enables a 2400-bps chip set to provide 9600-bps full-duplex communications. In addition, the modems have 2400-, 1200-, and 300-bps fallback modes. The modems also employ MNP5 error-checking and -correction protocols. Using an EBR modem at both ends of a communication link, the unit can achieve four times the transmission speed of a 2400-bps modem without bursts that are common with MNP5 or V.42 bis protocols. Both modems automatically select the highest speed after checking to confirm that an EBR modem is at the answering end. The units include a speaker and comply with the Hayes AT command set. 9624, $299; 9624e, $399.

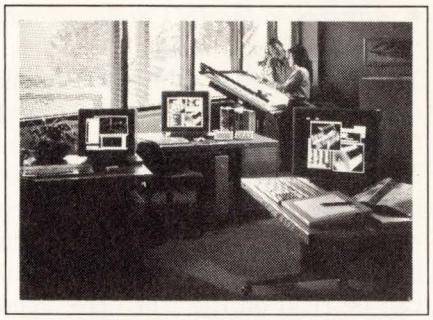
Sharp Digital Information Products, 16841 Armstrong Ave, Irvine, CA 92714. Phone (714) 261-6224. FAX (714) 261-9321.

Circle No. 360

Workstation Series

- *Based on the 68040 and 50-MHz 68030 μPs*
- *Delivers 12- to 26-MIPS performance figures*

The 9000 Series 400 product line provides the first workstations resulting from the HP and Apollo merger. The series 400 runs both the Domain/OS and HP-UX operating systems, which comply with AT&T's Unix system. The model 400dl is the entry-level desktop model that uses a 50-MHz 68030



μP. You can upgrade the 12-MIPS system to a 20-MIPS system by installing a 25-MHz 68040 μP. The models 425t and 400t use a 25-MHz 68040 and a 50-MHz 68030, respectively. The desktop systems deliver as much as 20 MIPS and 3.5M flops. All of the above models use the 9000 VRX graphics monitors with 1280 × 1024 pixels. Monitor options are 19-in. monochrome and 16- or 19-in. color. The Models 433s and 400t are deskside models and use a 33-MHz 68040 and a 50-MHz 68030, respectively. The 433s delivers 26 MIPS and 4.5M flops and uses the EISA bus. 400dl, $4999; 425t and 400t, $9000; 433s and 400s, from $12,990.

Hewlett Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900.

Circle No. 361

Serial-Port Expansion Board

- *Provides system with 16 ports for multiuser terminals*
- *Uses two 12-MHz 80C186 μPs as communications processors*

The ACL 16 provides a 16-bit ISA bus system with 16 serial expansion ports. The single expansion board uses two 12-MHz 80C186 μPs to control the communications tasks. The board contains a 16k-byte dual-port RAM to handle data transfers to and from the host; each μP has its own 64k-byte scratch-pad RAM. The board has three handshake options for the serial ports—full, partial, and no handshake lines. The

partial and no handshake lines have RJ-12 connectors. The full handshake lines use DB25 connectors. You can install as many as four boards in an 80386 PC-compatible system to provide 64 serial ports. The four boards can share the same dual-port memory, thus conserving address space. $1495 to $1595, depending on handshake option.

StarGate Technologies Inc, 29300 Aurora Rd, Solon, OH 44139. Phone (800) 782-7428; in OH, (216) 349-1860. FAX (216) 349-2056.

Circle No. 362

5¼-In. Optical-Disk Drive

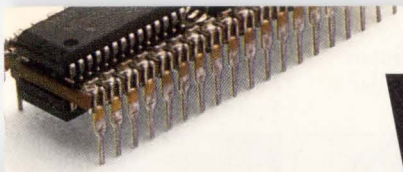
- *Uses rewriteable or WORM-type media*
- *Adheres to the ISO standard for sampled servo media*

The LaserDrive 520 optical-disk drive can use both write-once and magneto-optic (rewriteable) media. The 5¼-in. disk drive lets the user select the media option in hardware or in software. All media written on the company's LaserDrive 510 can be read on the new drive. The drive uses media that conforms to the ISO DP10089 standard for sampled servo media. Conformance gives the drive a capacity of 654M bytes/cartridge. Other features include a 53-msec average seek time; a 490k-byte data-transfer rate, a stand-alone cabinet, and multiple media sources. $2395; compatible rewriteable media, $200; compatible write-once media, $113.

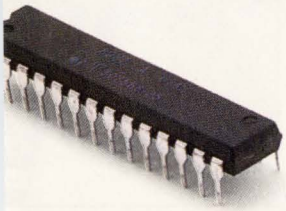
Laser Magnetic Storage International Co, 4425 ArrowsWest Dr, Colorado Springs, CO 80907. Phone (719) 593-7900. FAX (719) 599-8713.

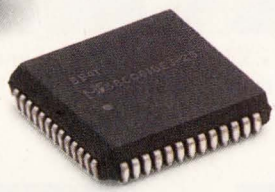
Circle No. 363

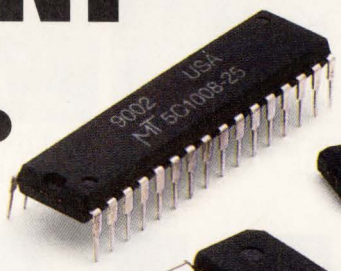
Text continued on pg 198

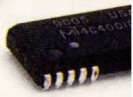


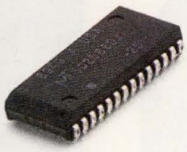
WE APPROACH THE MEMORY BUSINESS FROM ONE POINT OF VIEW...

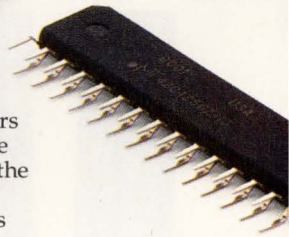












YOURS.

At Micron Technology, we offer a full line of leading-edge RAM components in speeds and packages for virtually any application.

But the memory business is more than just parts — it's people.

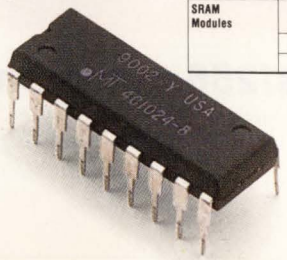
That's why we offer a total commitment to service and support, and a team of engineers and technical support personnel that are the most experienced memory professionals in the industry.

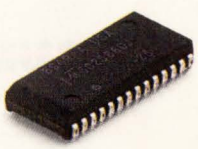
Because in the memory business there's only one point of view that counts. Yours.

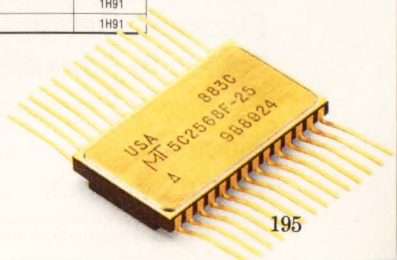
Component Product Family	Memory Size (Total)	Org. (Bits)	Speed (ns)	Package DIP	ZIP	SOJ	PLCC	TSOP	PQFP	Special Features	Availability	Military Qualified
SRAMs	1MEG	x1,x4,x8	25-45	X		X				x4 option: OE	Now	2H90
	256K	x1,x4,x8	20-45	X	X	X				x4 option: OE	Now	X
	64K	x1,x4,x8	12-45	X		X				x4 options: Separate I/O, OE	Now	X
	16K	x1,x4,x8	12-45	X		X				x4 options: Separate I/O, OE	Now	X
Cache Data SRAMs	288K	x9	14-34				X			486 Compatible, Self-timed write, Fast toe 7ns, 486 Burst and extended burst support	Samp: 1H91, Prod: 2H91	
	144K	x18	20-35				X		X	386/486 Compatible, Fast toe 8ns, Auto write completion, Parity bits	Now	
	128K	x16	20-35				X		X	386 Compatible, Fast toe 8ns	Now	
Synchronous SRAMs	288K	x18	15-25				X			Registered address, chip enables and write control; Data latch, Fast toe 6ns, Byte write capability	Samp: 2H90, Prod: 1H91	Samp: 1H91
	256K	x16	15-25				X					
SRAMs with Address Latch	288K	x18	15-35				X			Address, data and chip enable latches; Byte write capability, Fast toe 6ns, 3.0 Volt output buffer option	Samp: 2H90, Prod: 1H91	Samp: 1H91
	256K	x16	15-35				X					
	16K	x8	100	X		X				Intel 8051 and 8096 compatible	Now	X
	16K	x8	15-35	X		X				Compatible with high end micro controllers	Now	X
FIFOs	18K	2Kx9	15-35	X			X			Family options: 300 mil DIP package, Programmable flags	Samp: 1H91	2H91
	9K	1Kx9	15-35	X			X				Samp: 1H91	2H91
	4.5K	512x9	15-35	X			X				Samp: 1H91	2H91
DRAMs	4MEG	x1,x4,x8,x16	60-100	X	X	X		X		x4,x8 options: Write per bit x16 options: 2 WE/1CAS; 1WE/2CAS and 1WE/1CAS with write per bit	x1,x4 Samp: Now, Prod: 1H91; x8,x16 Samp: 1H91	Samp: 1H91
	1MEG	x1,x4,x16	70-120	X	X	X		X		x16 options: Byte write or write per bit	Now	X
	256K	x1,x4	100-120	X	X	X	X				Now	X
	64K	x1	100-150	X			X				Now	X
Quad CAS DRAMs	4MEG	x4	60-100			X				Separate CAS control for each DQ input/ output, Enhanced write per bit capabilities	Samp: 1991	
	1MEG	x4	70-100			X					Now	
Pseudo Static DRAM	1MEG	x8	80-120	X		X		X		Unmultiplexed addresses, Simple refresh control	Samp: 2H90, Prod: 1H91	
Dual Port DRAMs (VRAMs)	1MEG	x4,x8	80-120		X	X				CMOS, Fully static SAM, Serial input, Split read transfer	Now	Samp: 1H91
	256K	x4	100-120	X	X					CMOS, Fully static SAM, Serial input	Now	X
Triple Port DRAMs	1MEG	x4,x8	80-120			X	X			CMOS, Two fully static SAMs, Transfer mask, Split transfers, Functional superset of 1MEG VRAM	Samp: Now, Prod: 2H90	

Module Product Family*	Word Size (Words)	Org. (Bits)	Speed (ns)	Package DIP	ZIP	SIP	SIMM			Special Features	Availability	Military Qualified
DRAM Modules	2MEG,1MEG, 512K,256K	x36	70-120		X		X			Industry standard pin-out	256K, 512K: Now; 1MEG, 2MEG Samp: 2H90	
	4MEG,1MEG, 256K	x9	70-120			X	X			Industry standard pin-out	256K, 1MEG: Now; 4MEG Samp: 2H90	
	4MEG,1MEG, 256K	x8	70-120			X	X			Industry standard pin-out	256K, 1MEG: Now; 4MEG Samp: 2H90	
SRAM Modules	256K, 128K, 64K, 16K	x32	15-45		X					Industry standard pin-out with OE	16K, 64K: Now; 128K,256K: 2H90	1H91
	64K,32K	x16	30-45	X						Industry standard pin-out with OE	Now	1H91
	128K	x8	30-45	X						Compatible with 1MEG monolithic	Now	1H91

* Custom module and board-level product manufacturing services available.







MICRON TECHNOLOGY, INC.

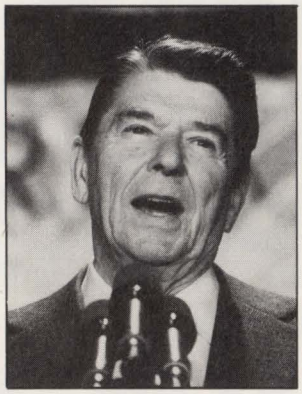
2805 E. Columbia Rd., Boise, ID 83706 (208) 368-3900

CIRCLE NO. 116

In 1979, Margaret Thatcher is voted in as Prime Minister of Great Britain...

and EDN is voted #1 in readership.

In 1980, Ronald Reagan is elected President of the United States...



and EDN presides as #1 in readership.

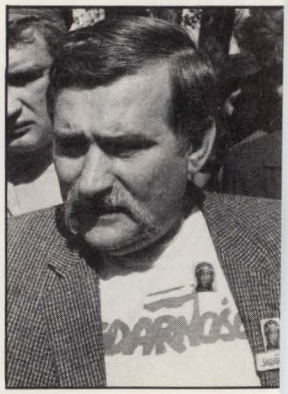
In 1981, Sandra Day O'Connor is the 1st woman on the Supreme Court...

and EDN is first in readership.

In 1982, Yuri Andropov is elected as the leader of the USSR...

and EDN leads as #1 in readership.

In 1983 Lech Walesa of Poland wins the Nobel Peace Prize...



and EDN wins the #1 prize in readership.

WORLD I

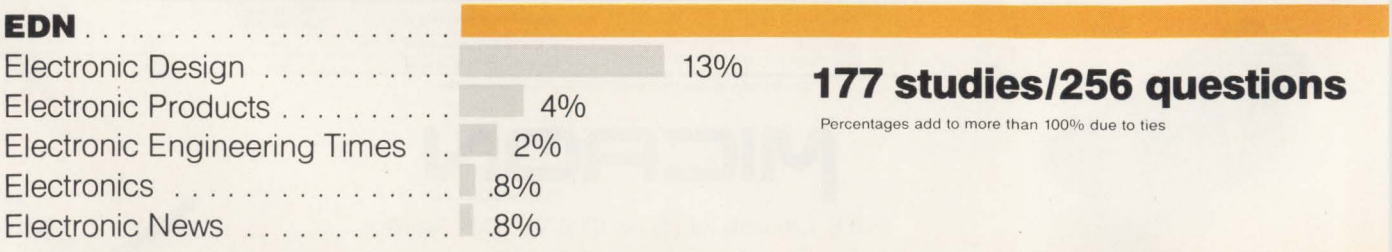
All Around The World, They Come; And They Go. There Has Been Only One Leader Since 1978... EDN.

Winning one study doesn't make history. But winning 84% of 177 independent readership studies since 1978 makes EDN a first class world leader. That's more wins than the rest of the electronics publications combined.

Announcing 7 new EDN independent

	EDN	Electronics
Zenith Electronics	#1	5
Sprague Semiconductor	#1	5
SGS Thomson Semiconductor	#1	5
3M	#1	5
Apex Technology	#1	5
Sipex Corporation	#1	4
Kyocera Northwest, Inc.	#1	NOT INCL.

CUMULATIVE WINS—
% of Readership/Reader Preference Wins* 1978–1989 (to date)

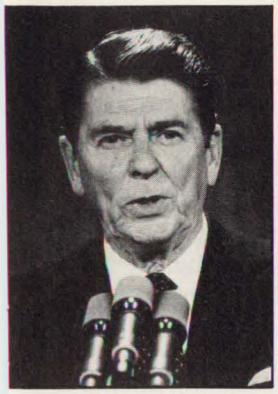


177 studies/256 questions

Percentages add to more than 100% due to ties

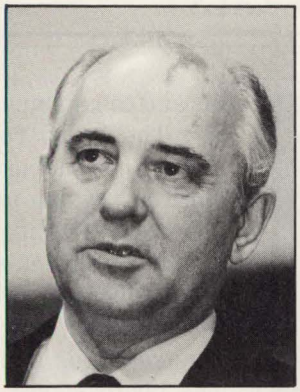
*Independent studies are conducted across customer/prospects lists or TIDS lists, not across a magazine's or newspaper's own list, which results in obvious bias. **Results based on the question

In 1984, Ronald Reagan is re-elected #1 in a landslide...



and EDN is re-elected #1 in a readership landslide.

In 1985, Mikhail Gorbachev is elected as the leader of the USSR...



and EDN is elected the leader in readership.

In 1986, Corazon Aquino is chosen as the President of the Philippines...

and EDN is chosen as #1 in readership.

In 1987, Margaret Thatcher wins a third term as Prime Minister...

and EDN wins another year as the leader in readership.

In 1988, George Bush is elected to highest office in the United States...

and EDN holds the #1 spot in readership.

LEADERS

But In The World Of Covering Electronics Technology, And EDN's Leadership In Readership Reign Continues.

*readership/reader preference study wins:**

Electronic Design	Electronic Products	EE Times	Electronic News
2	4	3	NOT INCL.
2	4	3	NOT INCL.
4	3	2	NOT INCL.
2	4	3	6
2	3	4	NOT INCL.
2	NOT INCL.	3	NOT INCL.
3	2	4	5

84%

If you would like to see the complete record of EDN's readership wins, contact your local sales representative. EDN will send you a six-foot long brochure that proves history repeats itself.

And only a leader dares to offer $1000 to anyone who can disprove its claim to readership. No other electronic engineering magazine or newspaper in the US or throughout the world has won more independent readership/reader preference studies than EDN.

EDN Magazine Edition
News Edition

A Partnership in Power & Prestige Worldwide

*Which of these publications do you read regularly (3 out of 4 issues)?" in each study.

Ultrasonic Measurement Unit

- *Provides 0.001-in. resolution from 2 to 9.999 in.*
- *Housed in NEMA 4× enclosure with internal power supply*

The LD1000 ultrasonic device provides high-resolution distance measurements. The unit provides linear measurements in the range of 2 to 9.999 in. with an effective resolution of 0.001 in. Its internal resolution is 0.0006 in./bit. The analog and digital outputs transmit in serial ASCII format. The analog outputs use a 12-bit D/A converter, and the operator can scale the analog voltage output range. A resident communications protocol provides interactive communications over an RS-232C or RS-422 link. You can observe the measurement data on a 4-digit LED display that's also used to trigger relay closures for high- and low-range measurements. The unit is housed in a NEMA 4× enclosure with an internal 120V ac, 60-Hz power supply. From $1499.

Contaq Technologies Corp, 15 Main St, Bristol, VT 05443. Phone (802) 453-3332. FAX (802) 453-4250.

Circle No. 364

X-Station Terminal

- *Dedicates 68020 μP as an X-Server controller*
- *TI34010 handles frame-buffer management*

The X-station display is a series of X-station terminals. The series consists of two gray-scale and three color terminals. Three color display terminals offer 14-, 17-, and 19-in. monitors and a choice of 16 or 256 colors. They dedicate an MC68020 μP as an X-server controller and a TI34010 chip handles the graphics tasks such as frame-buffer management and drawing operations. All models can run local X Window managers and terminal emulators to reduce host overhead and network traffic. Two different window managers are available—one based

on MIT's twm and the other based on OSF's Motif window manager. The terminals communicate over Ethernet networks using TCP/IP and over an RS-232C link using a serial protocol. $3000 to $6000.

NCR World Headquarters, 1700 S Patterson Blvd, Dayton, OH 45479. Phone (800) 225-5627.

Circle No. 365

Image-Capture Board

- *Grabs video-camera images in 1 sec*
- *Displays images on VGA screens with 64 levels of gray scale*

The VIP 640 image-capture board for PC compatibles drives IBM VGA-compatible monitors and delivers 640×480 pixel resolution. The board is compatible with most graphics application packages such as desktop publishing and paint programs. A grab function captures an image from an NTSC or PAL-compatible video camera in less than 1 sec. The board displays 64 gray levels and can manipulate 256 gray levels. The board runs with X Windows and supports editing using word-processing programs. You can silhouette an image using standard geometric shapes or freehand drawing. Advanced cut and paste features include cropping, sizing, scaling, rotation, and mirror images. The board comes with Astral Picture Publisher Video Software, which integrates with application packages such as PageMaker, Ventura Publisher, and Publisher's Paintbrush. $249.

Ventek Corp, 31336 Via Colinas, Suite 102, Westlake Village, CA 91362. Phone (818) 991-3868. FAX (818) 991-4097. **Circle No. 366**

Voice/Data/Fax Multiplexer

- *Accesses T1, ISDN, SDM, and CCITT X.50/X.58 networks*
- *Data channel operates at 64k bps for LAN-to-LAN connections*

The SDM-T multiplexer provides voice, data, or fax communications. The unit integrates a variety of communications channels for transmission over 48k- to 128k-bps digital networks. It can also access public network services such as fractional T1, ISDN Basic rate, AT&T's SDM, and CCITT's X.50/X.58 protocols. A high-speed data channel operating at 64k bps permits LAN-to-LAN communications. Five medium-speed data channels operate as fast as 19.2k bps for asynchronous or synchronous communications. You can install as many as six voice-channel cards, which have echo cancelers and digitize voice signals from 8k to 16k bps. A dynamic bandwidth-allocation feature allows the link to always operate at maximum capacity. You can install as many as four Group-3 fax relay channels. Each fax channel operates with a voice channel to provide voice in the fax relay mode. An asynchronous command port lets you configure the network and provides diagnostics. Basic unit,

COMPUTERS & PERIPHERALS

$2400; unit with two voice channels and six data channels, $6000. Delivery, 60 days ARO.

Advanced Compression Technology Inc, 31368 Via Colinas, Suite 104, Westlake Village, CA 91362. Phone (818) 889-3618. FAX (818) 889-2041. **Circle No. 367**

386SX Laptop PC

- *Has 120M- or 60M-byte disk drives and runs at 20 MHz*
- *Weighs 14 lbs and measures 4 × 13½ × 8½ in.*

The SLT 386s/20 laptop computer uses a 20-MHz 80386SX μP. The unit weighs 14 lbs, measures 4 × 13½ × 8½ in., and has a NiCd battery pack that provides more than 3 hours of operation. Standard features include a 4k-byte, 4-way set-associative cache memory; 2M bytes of RAM expandable to 14M bytes; a 3½-in., 1.44M-byte disk drive; an enhanced keyboard with an external numeric keypad interface; a VGA backlit display; parallel and serial interfaces; interface for an external VGA monitor; and the company's expanded memory manager. Options include a 20-MHz 387SX coprocessor; a 1M-, 2M-, or 4M-byte memory board; a 60M- or 80M/120M-byte tape drive; a 2400 baud internal modem; and a carrying case. Model 120 with 120M-byte hard-disk drive, $7499; Model 60 with 60M-byte hard-disk drive, $6799.

Compaq Computer Corp, Box 692000, Houston, TX 77269. Phone (713) 370-0670. **Circle No. 368**

Does it meet Six Sigma

Can it do true mixed-mode testing?

What tools have been developed?

Before the A500 started testing Motorola's mixed-

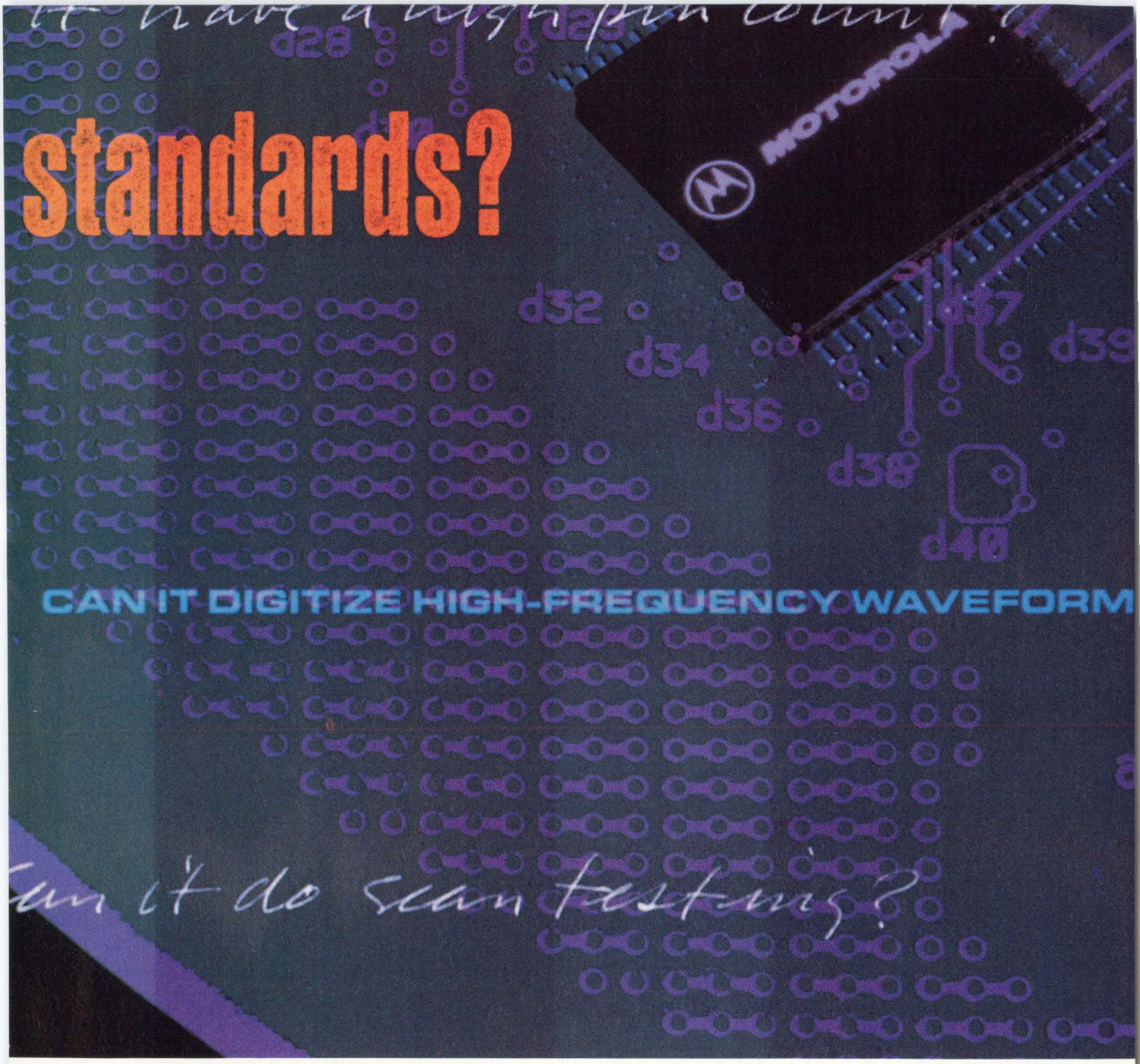
"Motorola has adopted a Six Sigma initiative which focuses attention on approaching zero-defect performance in everything we do, including our test systems. Our purchase of the Teradyne A500 test system supports our Six Sigma initiative and our competitive leadership challenge."

Director of Marketing

Motorola knows you can't have a Six Sigma process unless you can test to Six Sigma standards. That's why Motorola's MOS Digital-Analog Integrated Circuits Division chose the Teradyne A500 Analog VLSI Test System. Because, in addition to proving the A500 could handle the complex technical requirements of Motorola's advanced ISDN interfaces, we also demonstrated that we could perform to Motorola's stringent quality levels.

"Can it do scan testing? Digitize high-frequency waveforms? Do true mixed-mode testing? Does it have a flexible architecture? Can you give us the support for a Six Sigma process? Applications expertise? Complete documentation? The right tools? In each case, Teradyne answered yes."

Manager, Advanced Test Technology



signal technology, Teradyne had to pass a few tests.

With the A500, Motorola had the ability to digitize waveforms at 20 MHz, plus the high pin count necessary to guarantee that their ISDN U-Interface worked the way it was supposed to.

Best of all, the A500's full tester simulation and powerful IMAGE™ software provided the design flexibility and rapid debugging Motorola needed to deliver defect-free parts on time.

"The A500 gave us the resources we needed, in one place, to be able to have a functioning test program very quickly – at least two to three times faster than any other test system. This type of support is just what we need to get our complex circuits, such as the U-Interface transceiver, to the marketplace ahead of the competition."

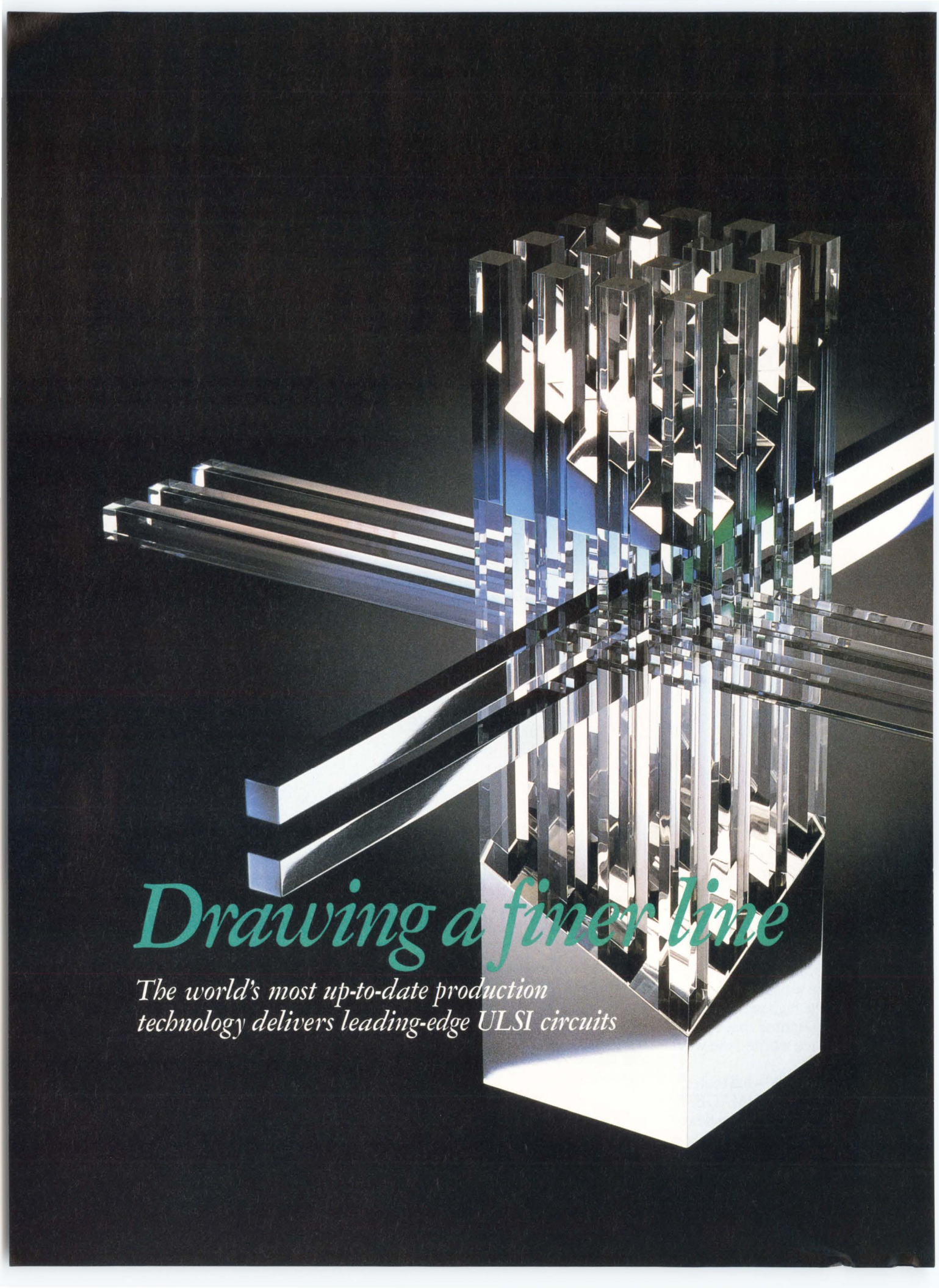
Operations Manager

To Motorola, delivering Six Sigma quality is not just a promise. It's a way of doing business. And it's a test that must be passed by suppliers as well.

To see how our A500 family of test systems can help you deliver quality, call Beth Sulak at (617) 482-2700, ext. 2746.

Or call your nearest Teradyne sales office, or write: Teradyne, Inc., 321 Harrison Ave., Boston, MA 02118.

TERADYNE



Drawing a finer line

The world's most up-to-date production technology delivers leading-edge ULSI circuits

OKI SYSTEM TECHNOLOGIES.

Sub-micron production in full swing, bringing the new age of 4M DRAMs

Oki's Miyagi Plant, benefitting from the latest advances in the company's system technology, has already reached mass production and shipment of 1M-bit memories and has recently begun quantity production of 4M DRAMs. At the Miyagi Plant, broad utilization of ultra-fine process technology and state-of-the-art automation combine to assure the high quality of these products. Oki is already well underway with technological innovation enabling production of 16M-bit memories.

High-level automation with ultra-fine process production

Oki's 0.8μ process technology used in its second-generation 1M- and 4M-bit memories has been integrated into one of the world's most advanced production lines for reliable mass production of over 20,000 6-inch wafers per month.

In 1988 Oki led the world with the first facility dedicated for production of sub-micron devices. Today that lead is being extended with the latest advances in automated manufacturing, such as sophisticated wafer tracking systems for improved quality and production control monitoring.

From the transportation system, driven by linear motors, to individual production equipment in each process machine group, all are computer controlled. To assure products of extremely stable quality, automation and every detail of the production environment are maintained at the world's highest levels.

High performance and packaging flexibility support customers in a wide range of applications

Oki's Advanced System Technologies are dedicated to total customer satisfaction. A comprehensive service system provides flexibility, quality, cost savings and quick turn-around times.

Oki's Miyagi Plant, featuring world-standard process technology and automation.

Oki Electric Industry Co., Ltd.
Electronic Devices Group
Overseas Marketing Group
7-5-25 Nishishinjuku, Shinjuku-ku,
Tokyo 160, Japan
■ Tel: 3-5386-8100 ■ Fax: 3-5386-8110
■ Telex: J27662 OKIDENED

Oki Electric Europe GmbH
Hellersbergstraβe. 2, D-4040 Neuss
West Germany
■ Tel: 2101-15960 ■ Fax: 2101-103539
■ Telex: 8517427 OKI D

Oki Semiconductor Group
785 North Mary Avenue, Sunnyvale,
CA 94086, U.S.A.
■ Tel: 408-720-1900 ■ Fax: 408-720-1918
■ Telex: 910-338-0508 OKI SUVL

Oki Electronics (Hong Kong) Ltd.
Suite 1801-4, Tower 1
China, Hong Kong City, 33 Canton Road.,
T.S.T. KLN, Hong Kong
■ Tel: 3-7362336 ■ Fax: 3-7362395
■ Telex: 45999 OKI HK HX

OKI

Oki Electric Industry Co., Ltd.
Tokyo, Japan

CIRCLE NO. 121

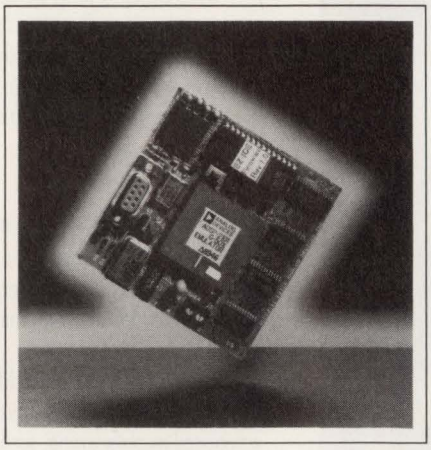
NEW PRODUCTS

TEST & MEASUREMENT INSTRUMENTS

ICE For ADSP-2101

- *Operates at chip's full 12.5-MHz speed*
- *Requires only 5V power and target's serial port*

The EZ-ICE is a stand-alone in-circuit emulator for the vendor's ADSP-2101. The 3.5-in.-square board requires only 5V and an ASCII terminal or a computer running terminal-emulation software. When you plug the emulator into the target system, you can execute programs either from target or emulation memory or a combination of the two. The DSP operates at its full 12.5-MHz clock speed with no performance or signal-timing degradation (except for three bus-control lines). An internal microcontroller controls the emulator's operation and allows single-step program execution with multiple breakpoints as well as bidirectional transfers of memory images. Firmware in the emulator generates the menus displayed on the host terminal. $2101.



Analog Devices Inc, Box 9106, Norwood, MA 02062. Phone (617) 461-3881. **Circle No. 369**

Word Generator

- *Reads and outputs 40-channel signals to 40 MHz*
- *Connects to IBM PC's parallel port*

The W4040 Word Generator operates to 40 MHz with an internal or an external clock. It operates in single-step, burst, and continuous modes and produces outputs on 40 channels or reads data from 40 channels. Whether reading or writing, it uses the same I/O lines and stores patterns 2048 words deep. Four channels control 3-stating of 32 of the channels in groups of eight. Four other channels operate as trigger or auxiliary signals. You connect the unit to the parallel printer port of an IBM PC or compatible machine. Pattern-editing software accompanies the unit. The

software displays patterns in several forms, including graphical. It also lets you store patterns on disk and retrieve them. $2200.

Testelektronik, Postfach 2101, D-7030 Böblingen, West Germany. Phone (7031) 277916. FAX (7031) 289222. **Circle No. 370**

Test Board For IBM PC/AT

- *Makes full-speed dynamic tests of all PC-bus signals*
- *Has 72-channel logic analyzer that stores 2k samples/channel*

V-ATE is a tester for IBM PC/ATs and compatible computers. The heart of the system is a μP-based card that plugs into the 16-bit ISA Bus. The card contains a 72-channel logic analyzer for the bus. The analyzer stores 2048 samples. The card also contains diagnostic displays, a keyboard-interface port, and circuits that monitor the ±5V and ±12V buses of the computer under test. Memory on the board lets you download custom tests. A feature of the accompanying menu-driven software is an expert system whose learning capabilities assist in fault diagnosis. Among the tester's functions is verification of the design of new peripherals, chip sets, and system units. The vendor claims that the tester can reveal marginal conditions in such products more quickly and reliably than can other debugging techniques. From $2500.

Vista Microsystems Inc, 6 Whipple St, North Attleboro, MA 02760. Phone (508) 695-8459.

Circle No. 371

2-GHz Optical-To-Electrical Converters

- *Plug-in and stand-alone forms*
- *Include averaging power meter*

The OCP 5002 and 5502 are optical-to-electrical converters with an integrated averaging power meter. The 5002 is a module that plugs into the vendor's TM 5000 series mainframes; the 5502 is a stand-alone in-

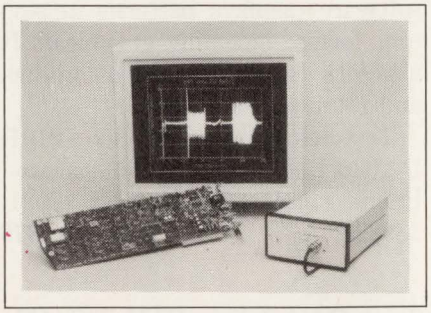
strument. The units' bandwidth is dc to 2 GHz. Wavelength is 1100 to 1650 nm. The units have aberrations of less than 15% p-p (5% to 10% typ). Noise floor is below 1 μW. The vendor offers IBM PC-based software that enables the units to make rapid comprehensive measurements on communications waveforms. OCP 5002, $8950; OCP 5502, $9950.

Tektronix Inc, Box 19638, Portland, OR 97219. Phone (800) 426-2200. **Circle No. 372**

PC-Based-Modulation And Time-Interval Analyzer

- *Covers dc to 1.3 GHz*
- *Resolves 1-ppm deviation when sampling at 1 kHz*

The GT2210S time-interval and modulation analyzer is usable from dc to 1.3 GHz. It provides such data as plots of frequency vs time and



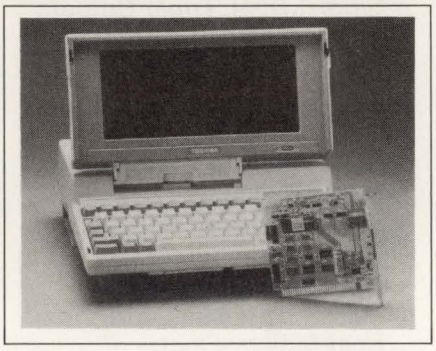
frequency deviation vs time. The hardware consists of an IBM PC-based frequency counter card and an external prescaler that operates from 50 MHz to 1.3 GHz. The unit has a resolution of 10 digits with a 1-sec measurement interval; at a measurement rate of 1 kHz, resolution is less than 1 ppm. You can vary the sample interval from below 1 msec to nearly an hour. The software generates a virtual front panel and includes a graphing facility that produces printouts on the computer's CRT as well as on plotters and most graphics-capable printers. You can save acquired data in ASCII or graphical formats. $2395.

Guide Technology Inc, 18 Fallenleaf Lane, Los Altos, CA 94024. Phone (800) 288-4843; in CA, (415) 961-9259. **Circle No. 373**

Half-Size Data-Acquisition Board For PCs

- *Works in laptop PCs*
- *Generates −12V on board*

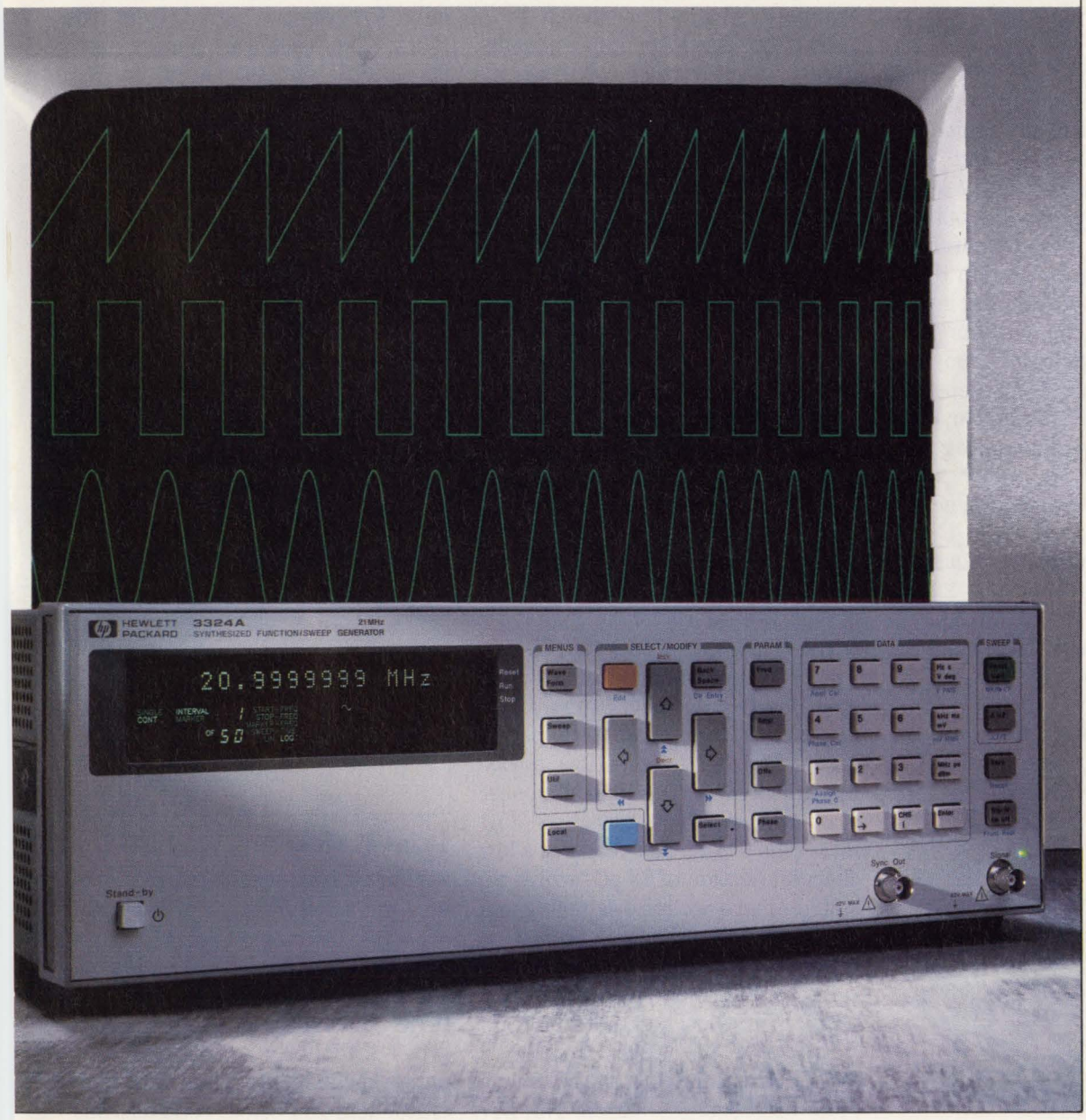
The DT2814 is a half-size data-acquisition card for the IBM PC bus. The board does not use −12V power from the bus—it generates what it needs from the 12V supply using an onboard charge pump. This feature and its small size suit the board for use in laptop PCs—



both those that have internal I/O expansion capability and those whose expansion capability is based on a clip-on chassis. Thus, you can use the board as the heart of portable, battery-operated data-acquisition systems. The board, which owes its compactness to surface-mount assembly, has 16 single-ended channels and makes 40,000 12-bit A/D conversions/sec. A programmable clock triggers conversions. Jumper-programmable input ranges are 0 to 5V, ±5V, and ±2.5V. The vendor's DT/Gallery menu-driven software accompanies the board. $345.

Data Translation Inc, 100 Locke Dr, Marlboro, MA 01752. Phone (508) 481-3700. FAX (508) 481-8620. TLX 951646. **Circle No. 374**

Synthesizer performance... priced to generate some waves.



The HP 3324A Synthesized Function/Sweep Generator.

The attractive price of this generator is bound to generate some waves. It's much less than you'd expect to pay for a function generator that has 5 ppm frequency accuracy, 9-digit frequency resolution and multi-interval sweep capabilities too.

Put it to work in testing filters and amplifiers where you need synthesizer accuracy, stability and signal purity. Tap its high linearity and multi-interval sweep features for A/D converter testing and for simulating rotating signals. Simplify the creation of phase-related signals for PLL or navigation-system testing with the new automatic phase-calibration options.

And there's more. Such as the high-stability frequency-reference option, and a high-voltage output option for making really big waves. Call **1-800-752-0900** today. Ask for **Ext. 1598** or mail the reply card and we'll send a brochure and application information.

There is a better way.

HEWLETT PACKARD

NEW PRODUCTS

INTEGRATED CIRCUITS

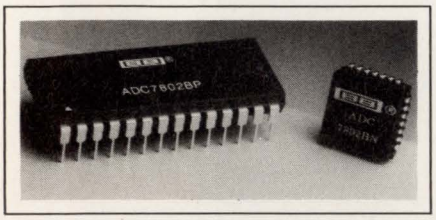
Quad Comparators

- *Propagation delay is 8 nsec*
- *Operate from single or dual supplies*

The MAX900 and MAX901 quad comparators reportedly consume 7× less power than do equivalent combinations of single and dual comparators. Using a 5-mV overdrive, the devices consume only 18 mW/comparator. The comparators, which feature a propagation delay of 8 nsec, contain differential inputs and TTL-compatible outputs with internal active pullups. You can power the devices from separate analog and digital supplies or from a single 5V supply. The analog supply can be from 5 to 10V or ±5V. For applications requiring synchronous operation, the MAX900 provides a latch-enable function. The comparators come in 20-pin (MAX900) and 16-pin (MAX901) plastic DIPs, ceramic DIPs, and SO packages. MAX900, $7.01; MAX901, $5.98 (1000).

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No. 375



4-Channel, 12-Bit ADC

- *Operates at low power*
- *Features autocalibration*

The ADC7802 4-channel, 12-bit A/D converter is optimized for accurate multiplexing of dc signals. The ADC is self-calibrating and needs no offset or gain adjustments. Operating from a single 5V supply and dissipating only 10 mW, the device accepts unipolar inputs from 0 to 5V. Total conversion time is 17 μsec, and conversion results are available in two bytes with "no missing codes" guaranteed. Channel separation is typically 92 dB and channel-to-channel mismatch is ¼ LSB max. The IC contains a monolithic capacitor-array with an on-chip S/H device, a 4-channel multiplexer, autocalibration circuitry, and an 8-bit μP interface port. A special register permits full control over the converter through the μP bus, eliminating the need for hard-wired control lines. The ADC7802 is available in a 28-pin DIP or a 28-lead plastic leaded chip carrier. $19.95 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. FAX (602) 889-1510. TWX 910-889-1510. **Circle No. 376**

Quad TTL-Compatible Analog Switch

- *Has 45-nsec switching time*
- *On-resistance is 35Ω*

The DG601 quad spst analog switch operates from a single supply of 5 or 12V or from a dual supply of ±5V. The TTL-compatible device features a switching time of 45 nsec max and an on-resistance of 35Ω max. The switch also features a low charge injection of 13 pC, which results in more accurate sampling and cleaner switching. ESD protection is enhanced by the device's ±4000V rating on all pins. In a 16-pin DIP, $3.26; in a SO package, $3.41 (1000).

Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000. **Circle No. 377**

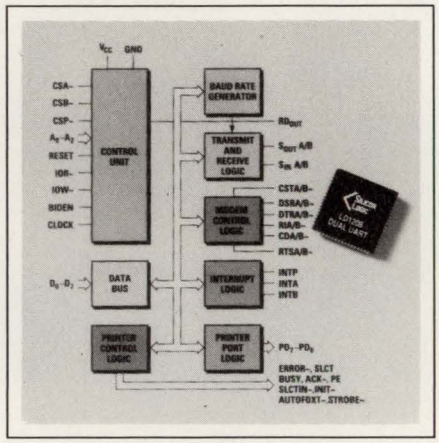
Stepper-Motor Driver

- *Includes control circuitry*
- *Drives 4-phase motors*

Available in a 24-pin DIP, this hybrid IC contains a gate array, four power MOSFETs, and four protection diodes. Because all nine components are contained in a single package, the module occupies half the total area normally required by discrete components. The module's universal controller can drive multiple 4-phase stepper motors with only the digital signal from the CPU. The user can choose from three different excitation modes. The module is available with voltage and current ratings of either 60V at 2.4 or 4.2A or 120V at 1.3, 2.0, or 2.5A. 120V/2.5A module, $4.70 (100,000 annually). Delivery, 12 weeks ARO.

Fujitsu Component of America Inc, 3330 Scott Blvd, Santa Clara, CA 95054. Phone (408) 562-1000.

Circle No. 378



Dual UART

- *Has on-chip printer port*
- *Handles 50-Hz to 56-kHz clock rates*

The LD1208 dual universal asynchronous receiver/transmitter features a bidirectional Centronics-type parallel printer port. An internal programmable baud-rate generator lets you select receive/transmit clock rates from 50 Hz to 56 kHz. The device is pin- and function-compatible with the VLI16C-452 device, but supports higher speeds as well as PS/2 applications. The LD1208 performs parallel-to-serial and serial-to-parallel conversion on the data characters received from a CPU or modem. On-chip status registers provide error conditions, and type and status of the transfer operation. The UART has complete modem control capability;

users can software-tailor its interrupt system to their own requirements. LD1208 in a 68-pin plastic leaded chip carrier, $6 (1000).

Silicon Logic, 550 E Brokaw Rd, San Jose, CA 95161. Phone (408) 441-1615. FAX (408) 954-0727.

Circle No. 379

Dual MOSFET Drivers

- *Operate at high speed*
- *Include undervoltage lockout*

The MC34151 series of dual MOSFET drivers features two independent channels with 1.5A totem-pole outputs. The low on-state resistance of the bipolar drivers allows significantly higher output currents at lower supply voltages than drivers using CMOS technology. With a 1000-pF load, the output rise and fall times are 15 nsec. Standby current is only 6 mA. The devices also feature an undervoltage-lockout function, which puts the outputs in a defined low state when in an undervoltage condition. The lockout function also has hysteresis to prevent erratic operation at low supply voltages. The MC34151 series is available in 8-pin DIP and SO packages for either the commercial or industrial temperature range. From $0.65 (10,000).

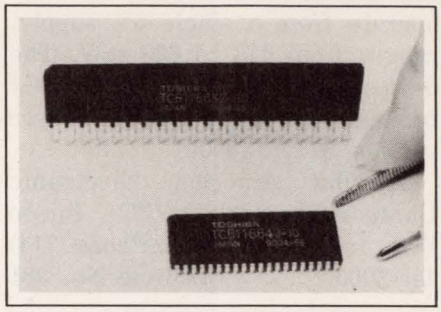
Motorola Semiconductor, EL340, 2100 E Elliot Rd, Tempe, AZ 85284. Phone (602) 897-3873.

Circle No. 380

1M-Bit Dynamic RAMs

- *Feature 16-bit word widths*
- *Have 80- or 100-nsec access times*

Organized as 64k×16 bits, byte-write TC511664 and write-per-bit TC511665 dynamic RAMs are the



industry's first 1M-bit devices with 16-bit word width. In the byte-write mode, an upper or lower byte is written by controlling the appropriate write-enable pins. The write-per-bit mode is a JEDEC standard operating mode, which allows users to inhibit the write operation for any of the 16 bits during each write cycle. The devices are available in 80- and 100-nsec versions. Low-power (L) versions, which need only 400 μA in a battery-backup application, are also available. Power

consumption for the devices, which operate from a single 5V supply, ranges from 413 to 633 mW. The devices are available in 40-pin SOJ packages and 40-pin ZIPs. 100-nsec version, $11.70 (5000).

Toshiba America Electronic Components Inc, 9775 Toledo Way, Irvine, CA 92718. Phone (714) 455-2000. **Circle No. 381**

Micropower Regulator And Comparator

- *Supply current is 40 μA*
- *Dropout voltage is 0.6V*

The LT1120 combines, on a single monolithic chip, a micropower positive voltage regulator and a free-collector comparator. Designed for battery-powered applications, the device includes a pin that permits shutdown of the device under logic control. With a supply current of only 40 μA, the LT1120 can provide more than 125 mA of output current at a dropout voltage of only 0.6V. The input voltage range is from 4.5 to 36V. The on-chip comparator is useful for system or battery monitoring. The device also includes a 2.5V reference that can source or sink 2 mA. Available in an 8-pin plastic miniature DIP or an 8-lead TO-5 metal can. From $2.40 (100).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 432-1900. FAX (408) 432-0507. **Circle No. 382**

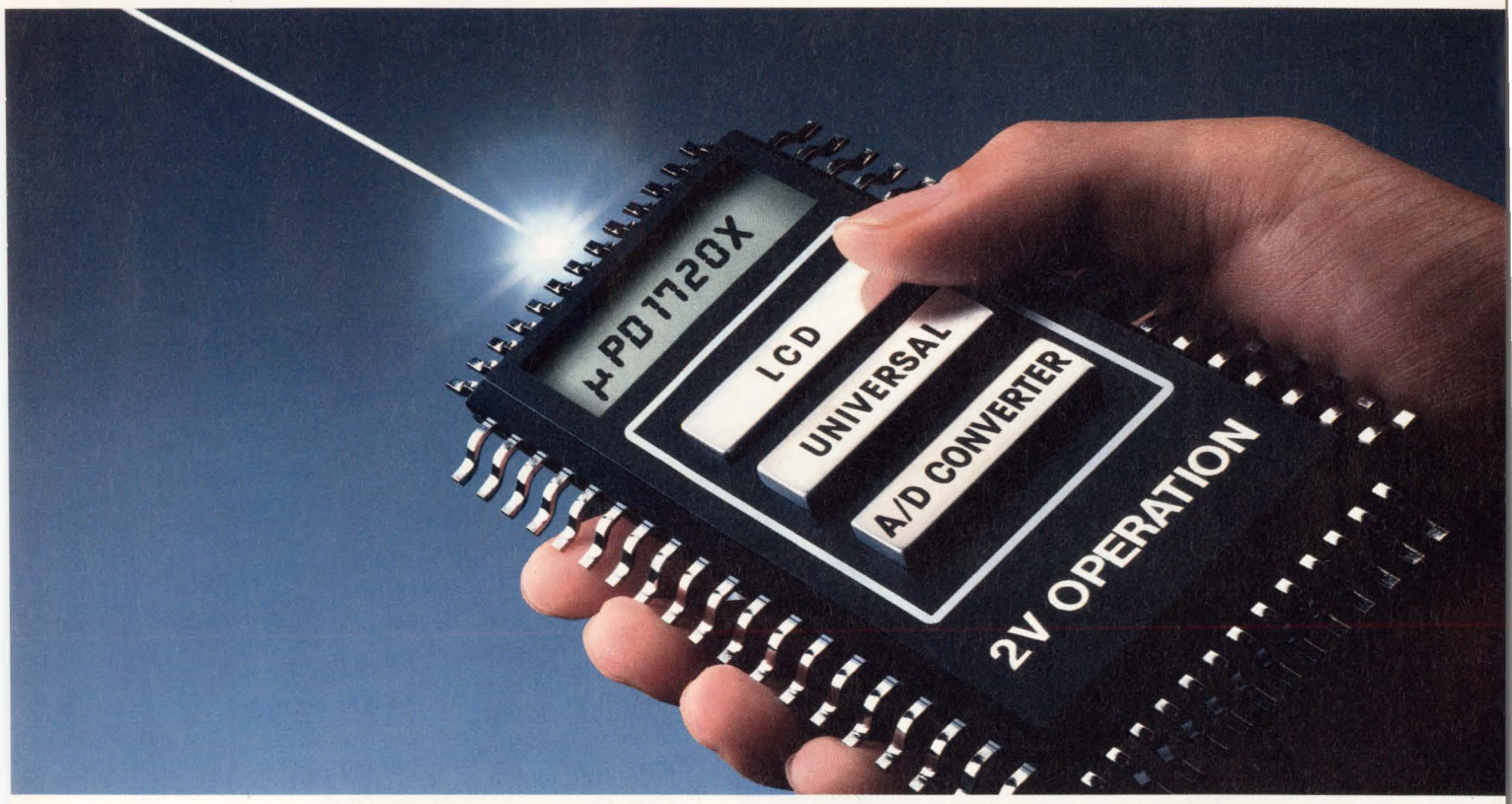
12-Bit High-Speed DAC

- *Update rate is 50M samples/sec*
- *Settling time is 12 nsec*

With a guaranteed update rate of 50M samples/sec, a settling time of 12 nsec to 0.1%, and a spurious-free dynamic range of 70 dB, the TDC1112 12-bit DAC is well suited for high-performance signal reconstruction. On-chip input data registers eliminate the data skew between bits, which causes glitching in nonregistered parallel input DACs. You can bypass these registers to reduce throughput delay. The DAC also uses 63 equal current sources to represent the most significant bits, a feature that eliminates the glitches associated with the switching of the much larger current sources used in conventional R-2R and binary-weighted current source DACs. Other features include ECL-compatible inputs and an output drive capability of 40 mA, which enables each of the two complementary outputs to drive 50Ω doubly terminated loads to 1V p-p. The TDC1112 is available in 24-pin DIPs and 28-lead chip carriers. From $31 (1000).

TRW LSI Products, Box 2472, La Jolla, CA 92038. Phone (619) 457-1000. **Circle No. 383**

Put the home electronics universe under your thumb



With NEC's high-end remote controller ICs.

One of the most powerful attractions your product can offer is a remote control unit that gives users a genuine sense of control. You get that kind of high-end performance across the full spectrum of remote control applications with NEC's 4-bit single-chip microcontrollers.

If you're designing air conditioners, for example, check out our μPD17201A. With an A/D converter and LCD driver on-chip, it lets you add a sophisticated remote control attraction—LCD displays of temperature, wind volume and more.

The 17202A also with on-chip LCD driver—is optimized for convenient control of home entertainment products. The LCD display gives users visual confirmation of VCR or audio programming commands.

For consumers who own one remote for the TV, another for the VCR, still others for the audio and air conditioner, we've developed a universal solution. The 17203A and 17204 let you design a remote that reads the code of any other controller, memorizes it with on-chip SRAM (16K/8K), and thus provides universal remote control from a single unit.

All devices in our μPD1720X series feature 4μs cycle time (4MHz), 2-to-6 volt operation, and two standby modes: STOP and HALT.

OTP versions will be available soon for the entire series. And NEC supports your design with a full set of development tools.

If you're ready to take control of a larger share of the home electronics market, call NEC today.

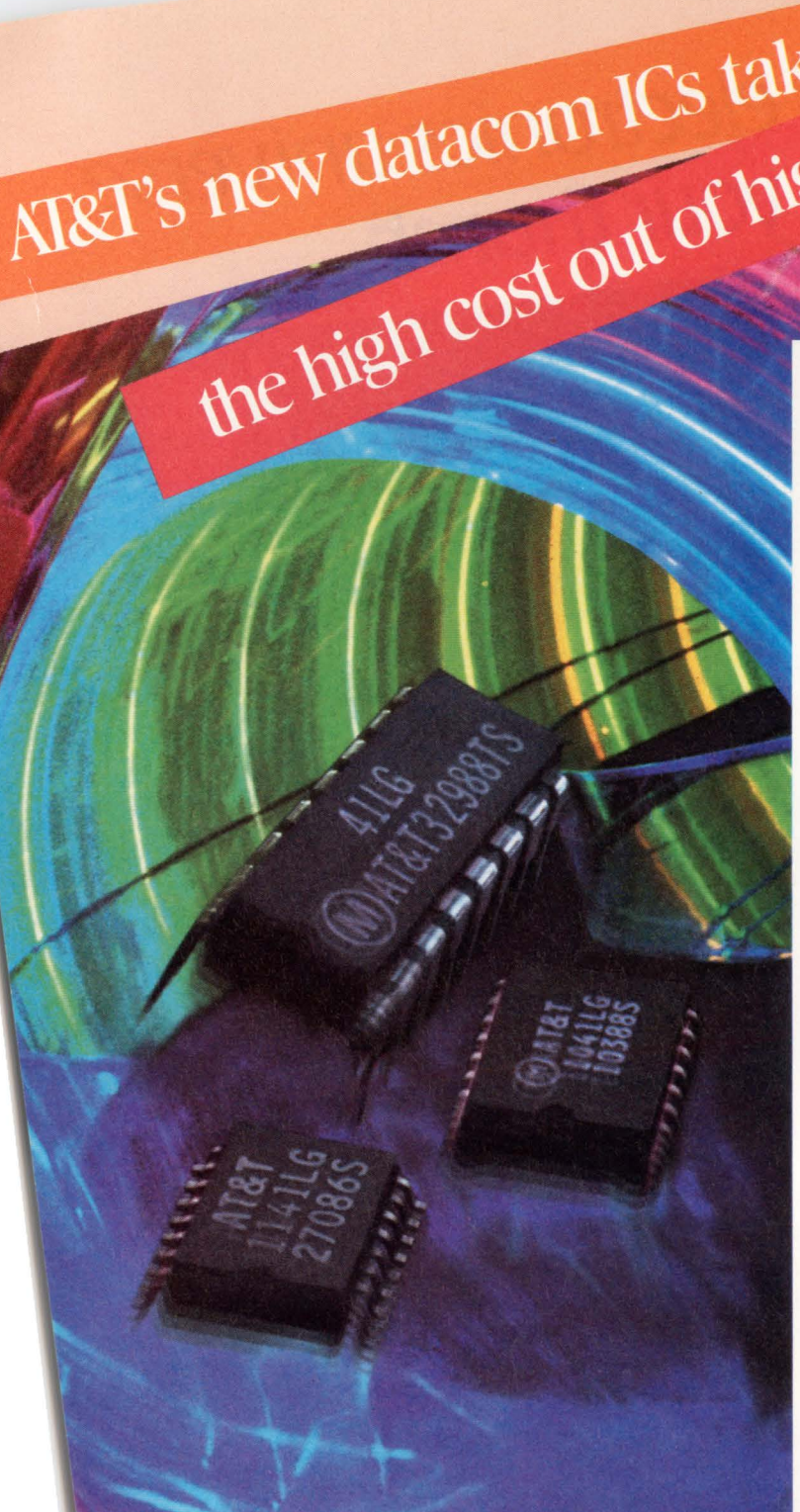
For fast answers, call us at:

USA Tel:1-800-632-3531. TWX:910-379-6985. W. Germany Tel:0211-650302. Telex:8589960. The Netherlands Tel:040-445-845. Telex:51923. Sweden Tel:08-753-6020. Telex:13839. France Tel:1-3946-9617. Telex:699499. Italy Tel:02-6709108. Telex:315355. UK Tel:0908-691133. Telex:826791. Hong Kong Tel:755-9008. Telex:54561. Taiwan Tel:02-719-2377. Telex:22372. Korea Tel:02-551-0450. Fax:02-551-0451. Singapore Tel:4819881. Telex:39726. Australia Tel:03-267-6355. Telex:38343.

NEC

CIRCLE NO. 123

AT&T's new datacom ICs take the high cost out of high speed.



AT&T's new 41 Series of differential quad line drivers/receivers and dual transceivers reach 400 Mb/s with substantially reduced EMI.

Our new datacom ICs do more than offer one of the industry's highest data rates and shortest propagation delays.

Their unique design can take you to 400 Mb/s on common twisted pair—at low EMI levels. This makes them an affordable alternative to fiber, when fiber's other benefits aren't needed.

In system use, they decrease EMI levels up to 30 db compared with standard 26LS TTL ICs. This sharply reduces cabinet design costs. And they meet ESDI standards, making them ideal for disk drive applications.

41 Series devices are pin-for-pin compatible with 26LS ICs—so they're easy to use. They help reduce board complexity and cost via on-chip termination and line-impedance-matching resistors. And they come in space-efficient, surface-mount SOJ and SOIC packages as well as standard DIPs.

Not exactly what you need? Create your own custom version quickly and easily by using our standard cell library.

Call **1 800 372-2447** for our databook on 41 Series components, in stock today at Hamilton/Avnet and Schweber.

The components of success.

AT&T
The right choice.

CIRCLE NO. 124

LITERATURE

Test Instruments Categorized

This short-form catalog of waveform-measurement and -generation products is aimed at research and test and measurement fields. Product areas covered include portable and benchtop digital oscilloscopes, modular digitizing systems, and fast-signal-generation products. The publication features high-performance measuring instruments. Specifications, although abbreviated, allow you to evaluate the suitability of the instruments to your needs.

LeCroy, 700 Chestnut Ridge Rd, Chestnut Ridge, NY 10977.

Circle No. 392

Catalog Presents VMEbus Board-Level Items

This 4-color, 8-pg catalog lists a range of board-level, software, and development-system products. Processor boards described include 68030- and 68020-based multiprocessor boards, as well as 68010-based single-board computers and 68000-based general-purpose processors. The publication details memory boards for commercial, ruggedized, and MIL-spec applications as well as a selection of SCSI and disk-controller boards. The catalog describes a variety of development software for systems integrators such as Unix, VRTX32, OS-9, VXWorks, and Ada.

Radstone Technology Corp, 20 Craig Rd, Montvale, NJ 07645.

Circle No. 393

Computer Software For Control Systems

Control Systems and Robotics comprises a collection of computer program abstracts from NASA. Included in the publication are 11 computer programs that address various aspects of control-systems design. The programs that are described include FSD (Flexible Spacecraft Dynamics), IAC (Integrated Analysis Capability), and ALPS (A Linear Program Solver).

Cosmic, University of Georgia, 382 E Broad St, Athens, GA 30602.

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Handbook Of Memory-Management Circuits

The *Dynamic Memory Design Data Book/Handbook* is a guide to memory-management circuits, including specifications and examples of how to design dynamic memory systems using high-speed CMOS logic and interface products. The 500-pg book presents application notes for dynamic-RAM interface designs for the company's 80C286, 80386, 68020, and 29K 32-bit RISC (reduced-instruction-set computer) μP. Two other notes describe memory board designs that support error detection and correction for the IBM PC/AT and PS/2. Article reprints discuss the Am29C668 4M-bit configurable dynamic memory controller/driver, error detection and correction system implementations, and memory subsystem reliability issues. The memory design manual also includes data sheets for the entire line of memory-management products.

Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088.

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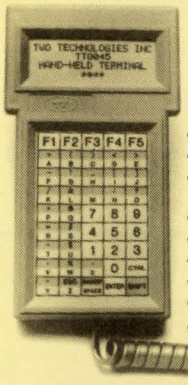

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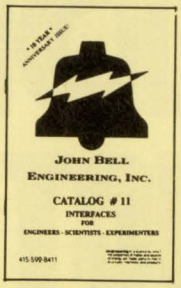

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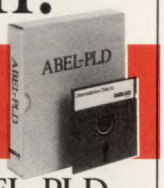

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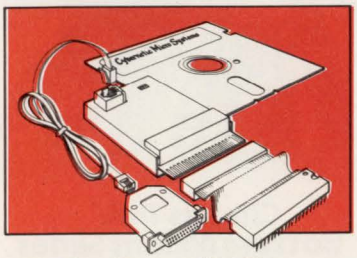

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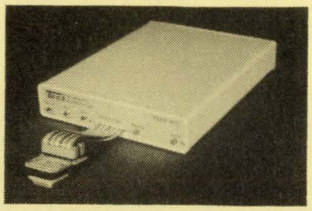

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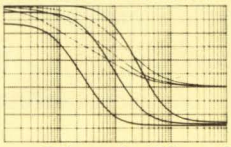

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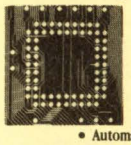

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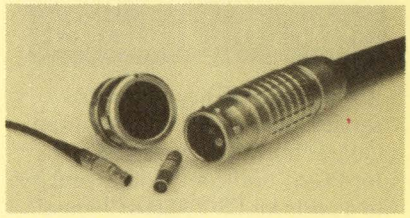

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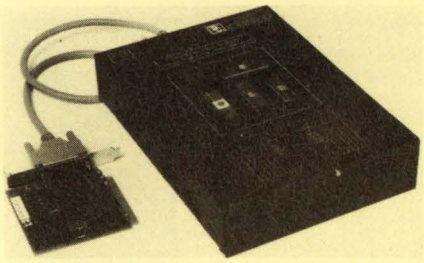

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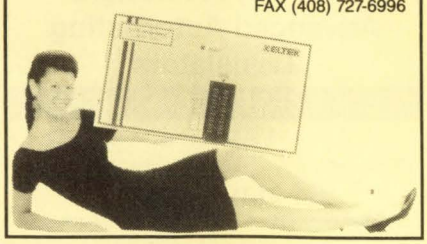

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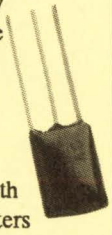

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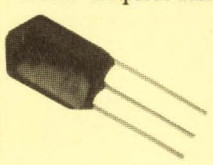

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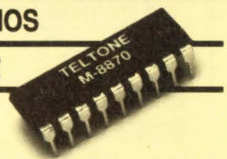

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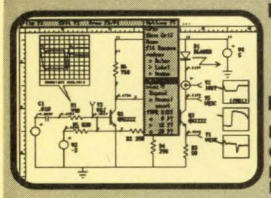

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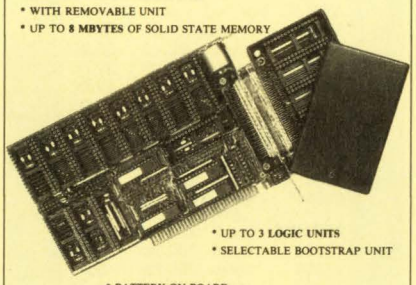

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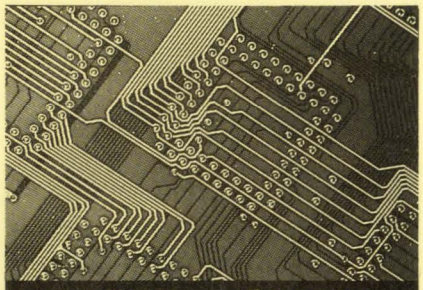

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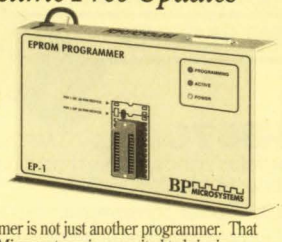

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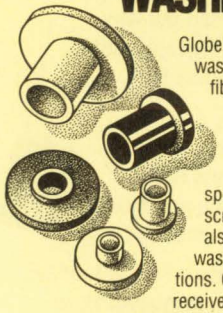

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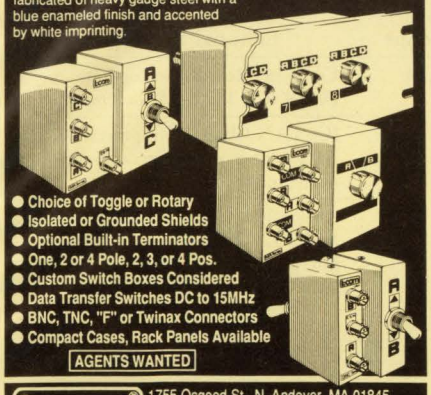

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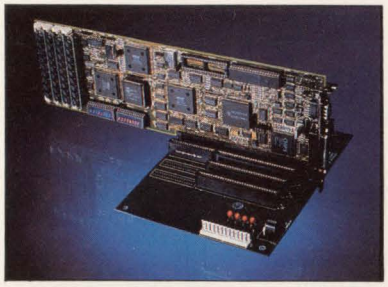

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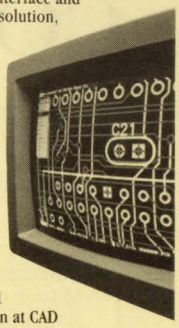

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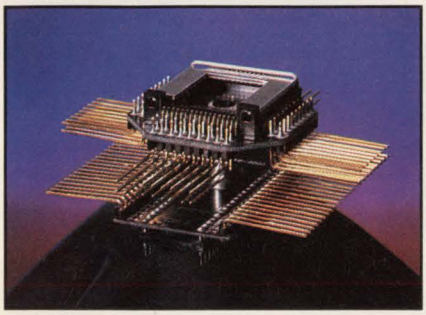

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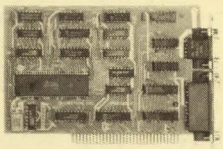

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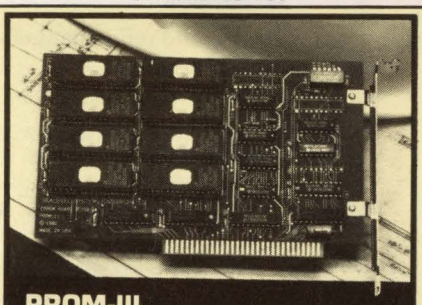

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1990 Recruitment Editorial Calendar

Issue	Issue Date	Ad Deadline	Editorial Emphasis
Magazine Edition	Oct. 1	Sept. 10	Computer Boards, Analog ICs, Digital ICs, Test & Measurement
News Edition	Oct. 4	Sept. 14	ICs/LAN Chips/Microprocessors, AI/Expert Systems, Special Supplement: Instruments
Magazine Edition	Oct. 11	Sept. 20	Analog ICs, Computer-Aided Engineering, DSP IC Directory, Displays, International Technology Update
News Edition	Oct. 18	Sept. 28	CAE/Hardware, Datacom, Regional Profile: Idaho, Colorado, Utah
Magazine Edition	Oct. 25	Oct. 4	Test & Measurement Special Issue—Digital Instruments, Computers & Peripherals, ICs & Semiconductors, System Software
Magazine Edition	Nov. 8	Oct. 18	Signal Processing, Computer-Aided Engineering, Computers & Peripherals, Software, Wescon Show Issue
News Edition	Nov. 15	Oct. 26	Displays, Defense, Special Supplement: Interconnect
Magazine Edition	Nov. 22	Nov. 1	17th Annual Microprocessor Directory, ICs & Semiconductors, Test & Measurement, Workstations
News Edition	Nov. 29	Nov. 8	ICs/Communication Controllers/ Microprocessors, DSP, Regional Profile: Illinois, Minnesota & Michigan
Magazine Edition	Dec. 6	Nov. 15	Product Showcase—Volume I: Software, ICs & Semiconductors, Packaging & Interconnect, Power Sources
News Edition	Dec. 13	Nov. 21	Power Supplies, Computers, Special Supplement: Salary Survey, Regional Profile: Florida
Magazine Edition	Dec. 20	Nov. 29	Product Showcase—Volume II: Test & Measurement, CAE Systems, Computers & Peripherals, Components

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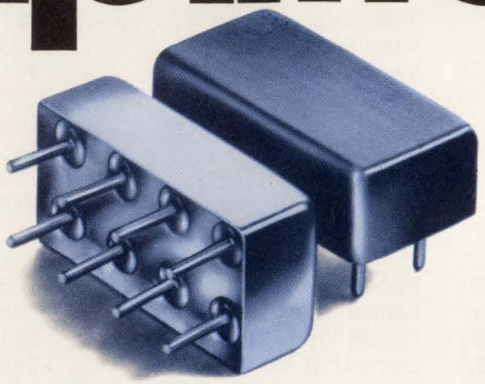

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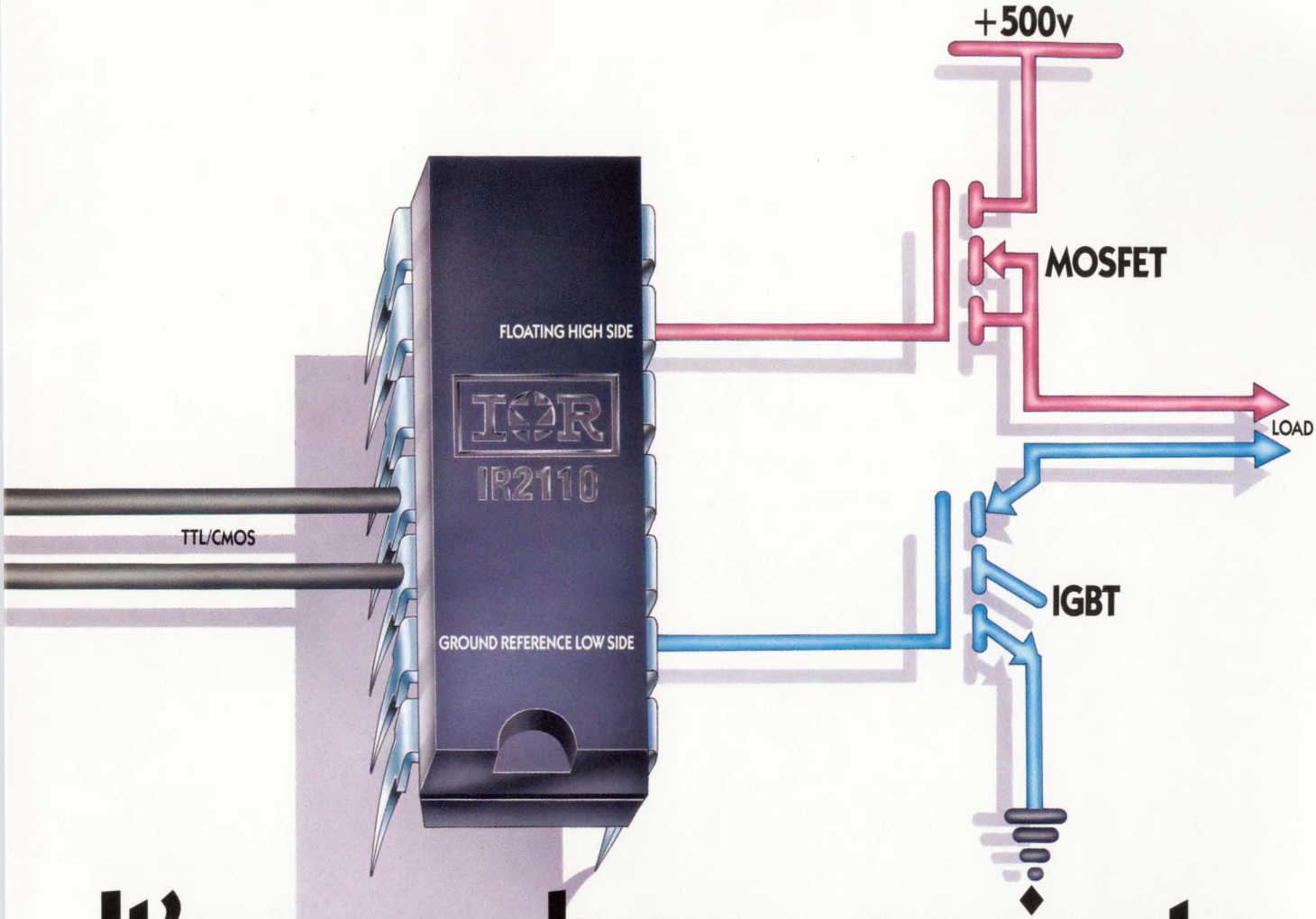
CIRCLE NO. 126

C118 REV. E



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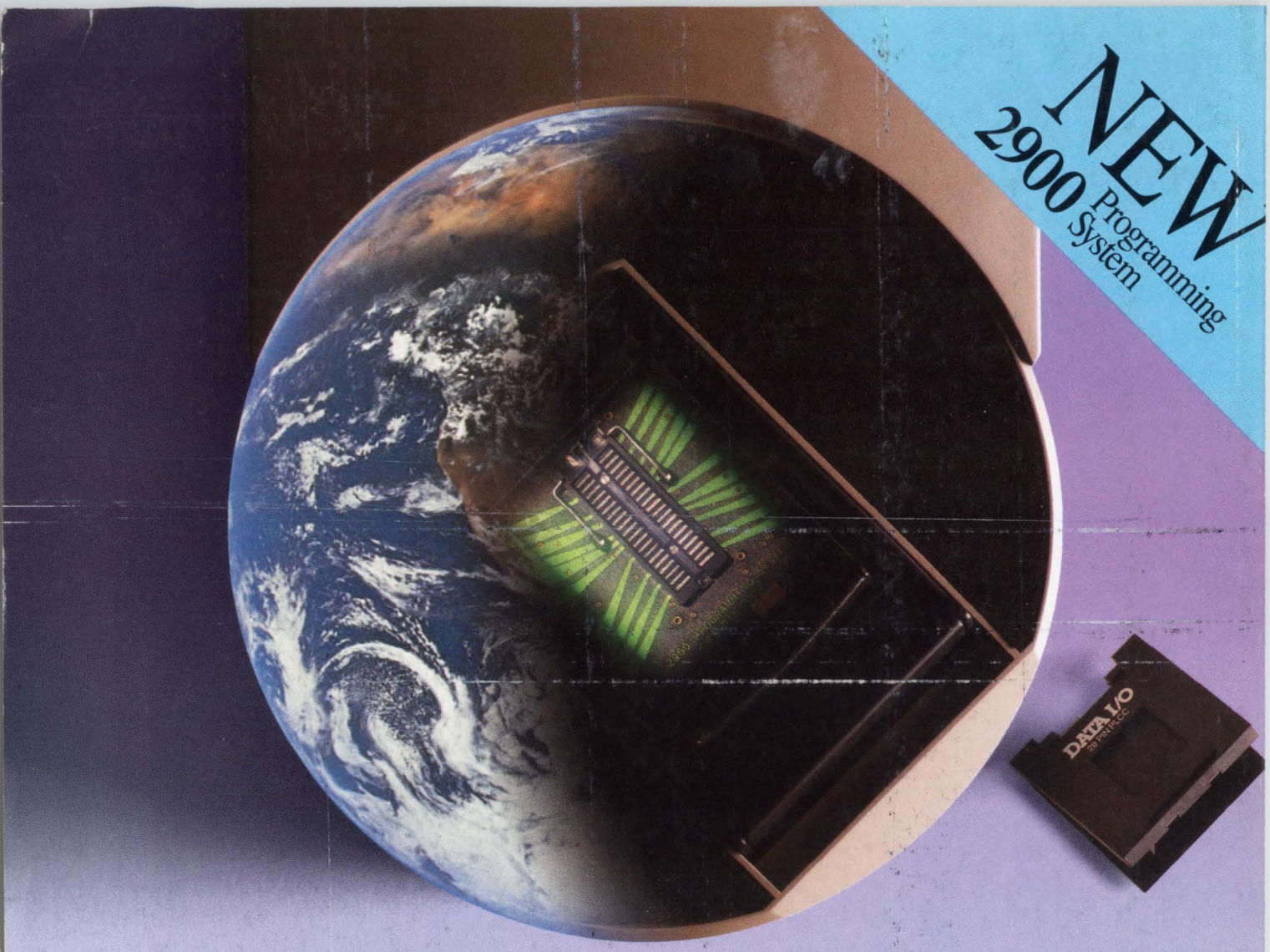

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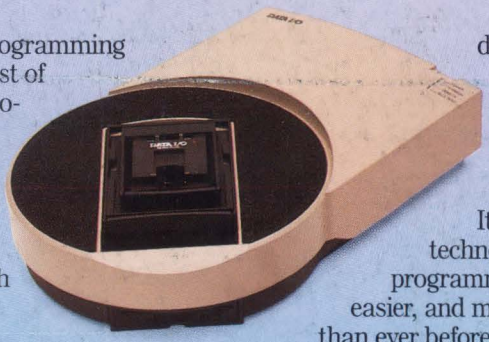

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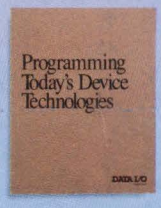

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