

EDN[®]

Combined logic analyzers and DSOs pg 77

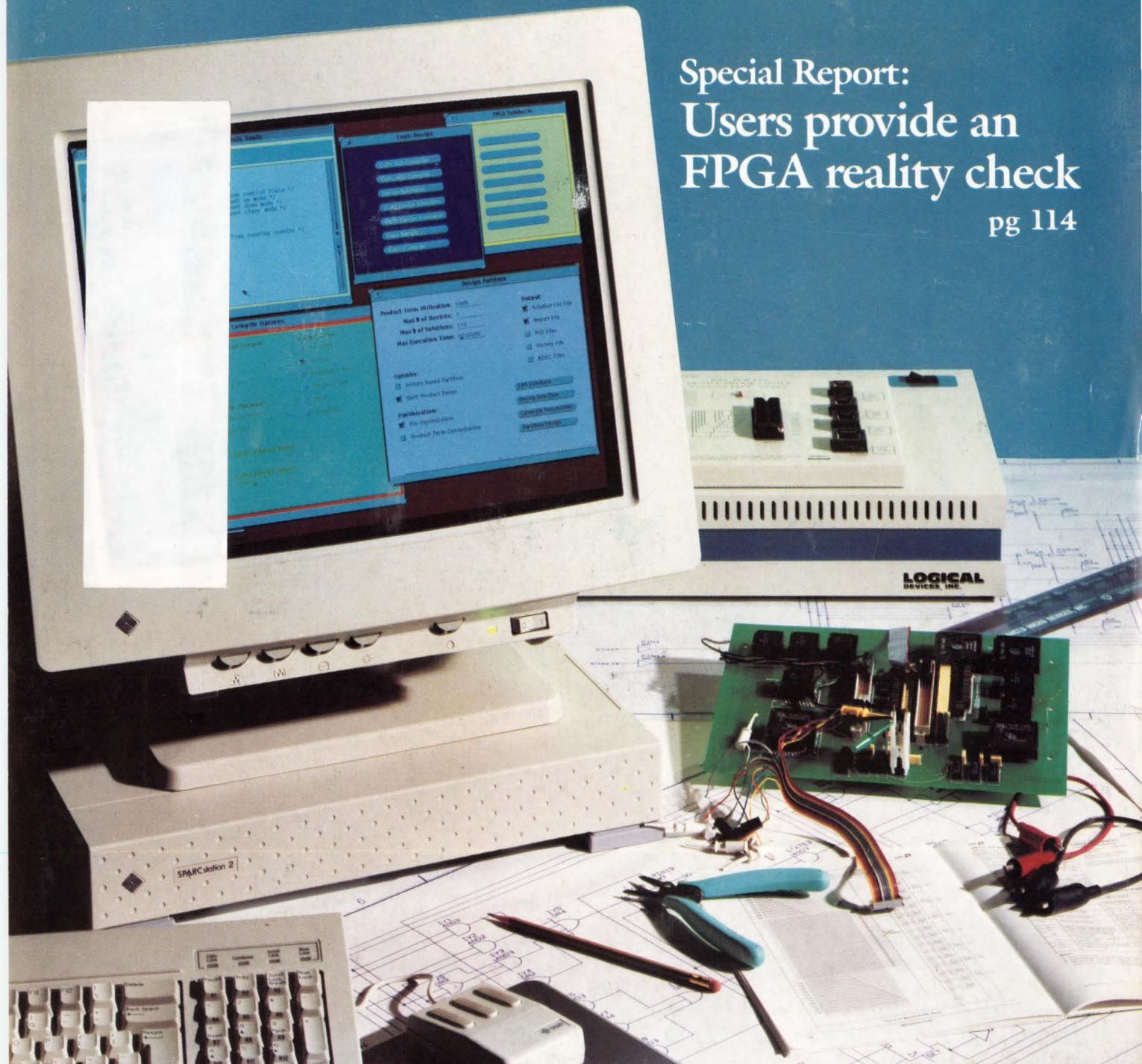
Slot-0 controllers pg 93

Know your options when designing filters pg 129

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ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Special Report:
Users provide an
FPGA reality check
pg 114



Vote for EDN's Innovation Finalists pg 49

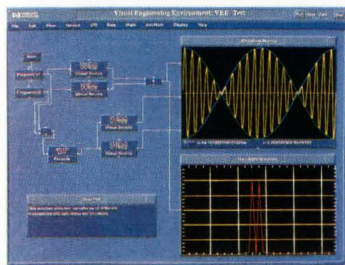
Finally, engineering software that clears the way to problem solving without programming.

```

void service(eid)
int eid;
{ int stat, byte;
/*serial poll
byte=hpib_spoll(eid)
if ( (byte<0) || ! (b
    printf("SRQ Problem\n");
    return; }
stat=my_read(eid, DVM_
if (stat>0) {
    buffy[stat] = '\0';
    printf("Data from instrument\n");
else printf("I/O read error\n");
return; }

main() {
int busid, stat, MTA, MLA;
char command[MAXCHARS];

busid=open("/dev/hpib7", O_RDWR); /* open raw HP-IB
MTA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 64;
MLA=hpib_bus_status(busid, CURRENT_BUS_ADDRESS) + 32;
stat = BUTTON_BIT ;
sprintf(command, "KM%02o", stat); /* 2 octal digits */
    
```



With HP VEE, you simply link the icons.

Computers are great for problem solving, if only programming didn't get in the way and slow you down. And now, it doesn't

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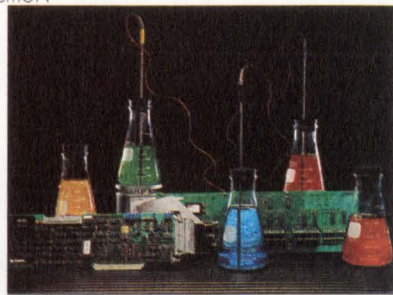
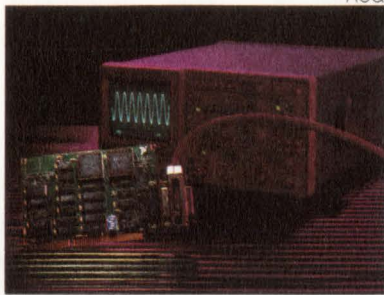
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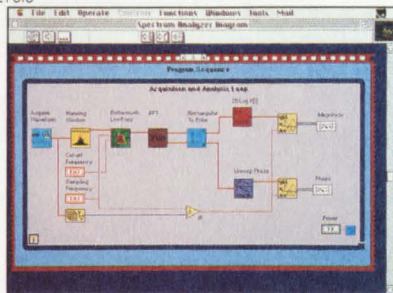
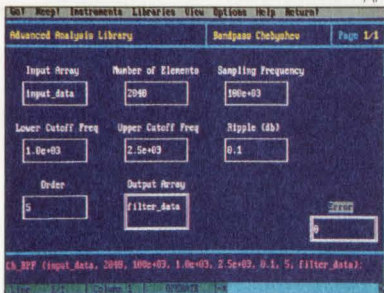
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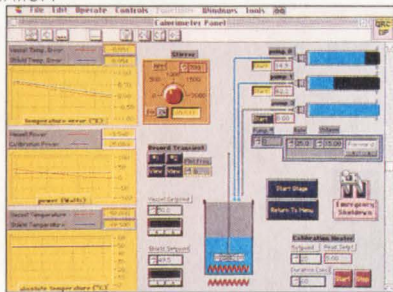
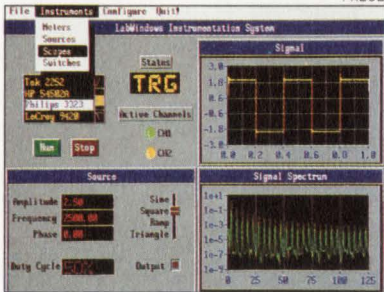


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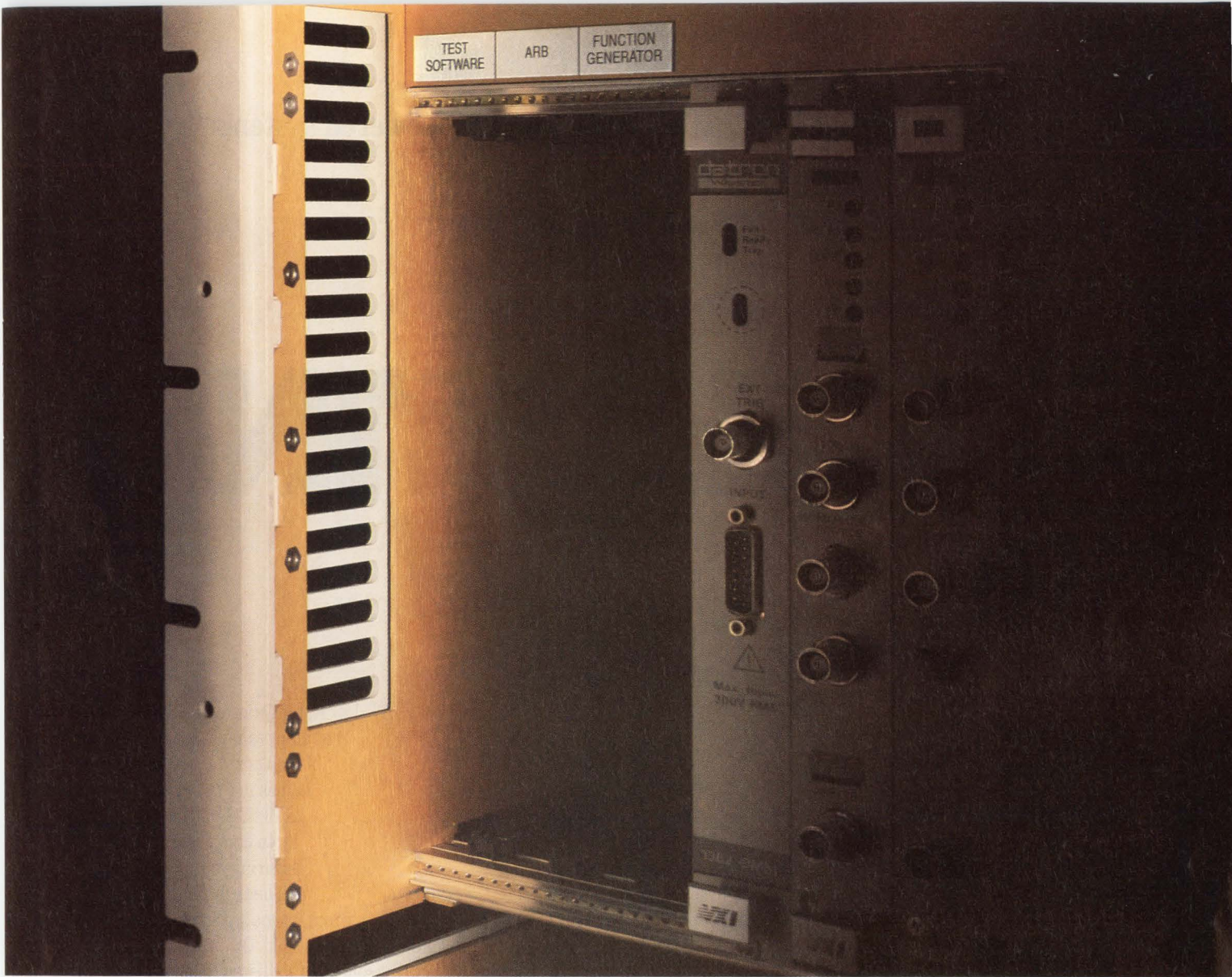
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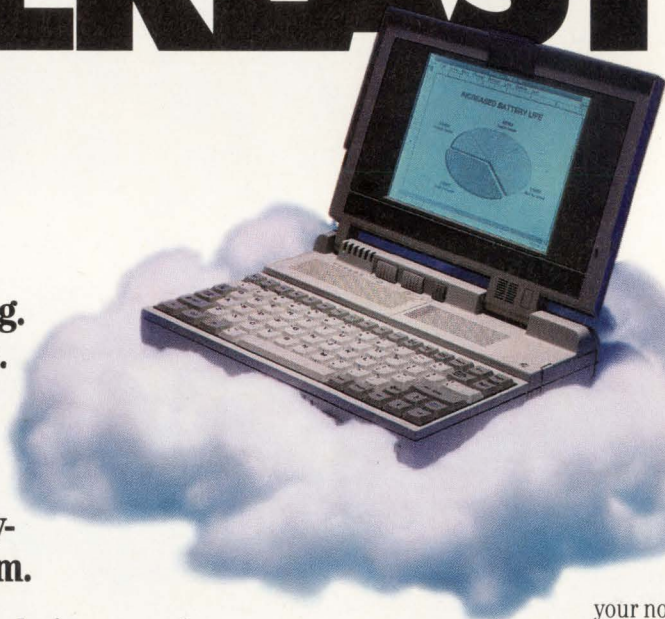
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These SO-8 IC devices can be driven directly by 5-V logic.

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This SO-8 IC device is ideal for higher current loads.

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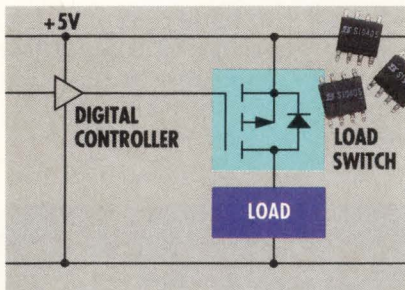
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On the cover: Field-programmable gate arrays (FPGAs) and the methods engineers use to adapt these devices to digital designs continue to evolve. EDN surveyed 40 engineers to examine their problems, preferences, and various design practices when working with this new technology. See our Special Report on pg 114. (Photo courtesy Logical Devices)

SPECIAL REPORT

FPGA design methods

114

Digital-design engineers are beginning to employ a diverse and rapidly evolving class of large programmable devices, called field-programmable gate arrays. As varied as the architectures of these devices are, engineers' design methods are even more diverse. However, the design method you do choose can profoundly affect which devices you can use.

—Charles H Small, Senior Editor

INNOVATION
Driving Electronic
Technology Into The
Next Century

DESIGN FEATURES

Know your options and requirements when designing filters

129

You can configure lowpass, highpass, bandpass, and notch filters in several ways. Knowing the performance characteristics of different filter configurations will help you specify the best filter for your application. —William Chambers, Acquisition & Control Electronics

Determine PLD metastability to derive ample MTBFs

147

As system speeds increase and more systems use asynchronous input sources, metastability becomes increasingly important. Because you can't eliminate metastability, you have to determine an appropriate MTBF for metastability-induced failures and use design techniques that limit the extent of these failures.

—Sean Dingman, Cypress Semiconductor

TECHNOLOGY UPDATES

Vote for Innovations and Innovator

49

Your votes will determine the winners in EDN's Innovations and Innovator of the Year competition. Use the bound-in ballot to make your choices.

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Continued on page 7

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Discover the new breed of timer/counter: the PM 6680.

Until now timer/counters have plodded along as workhorses of test and measurement. Now Fluke is the first out of the gate with a whole new breed of timer/counter: the Philips PM 6680. A powerfully fast, powerfully versatile instrument with capabilities usually associated with analyzers costing up to five times more. Yet the PM 6680 runs under \$2100—less than half the cost of comparable timer/counters. And for that low price you get more than twice the capabilities.

Compare the stats:

	PM 6680	HP 5334B	HP 5335
Frequency Range, A	225 MHz	100 MHz	200 MHz
Frequency Range, C (optional)	2.7 GHz	1.3 GHz	1.3 GHz
Single Shot Res.	500 ps	2 ns	2ns
Max. Reading Rate	2000/s	150/s	125/s
Base Price	\$2,075*	\$2,305	\$5,000

* GPIB interface optional (\$550)

Besides setting a faster pace, the PM 6680 adds new time and frequency analysis tools. Built-in mathematics and statistics functions give you stand-alone processing power that makes it easy to obtain measurements such as drift and rate of drift.

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And a host of new measuring capabilities give you the versatility to address your toughest measurement problems.



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Combined logic analyzers and DSOs: 77 Combined instruments find logic problems

When logic errors in your circuit turn out to be signal integrity problems, you need to team up a logic analyzer with an oscilloscope. A single instrument that combines the two is often more efficient than separate units.—*Doug Conner, Regional Editor*



Slot-0 controllers meet VXI-system needs 93

At the core of every VXI system lies its controller. Choosing a controller, then, would seem to be the first step in setting up your system, but it isn't.—*Richard A Quinnell, Regional Editor*

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News Flash

SPORTS

The 90 Nanosecond Workout
An Exhaustive Look At High Tech
Training Equipment

PAGE 2B

SCIENCE AND TECHNOLOGY

Virtual Reality
Close But No Cigar

PAGE 8H

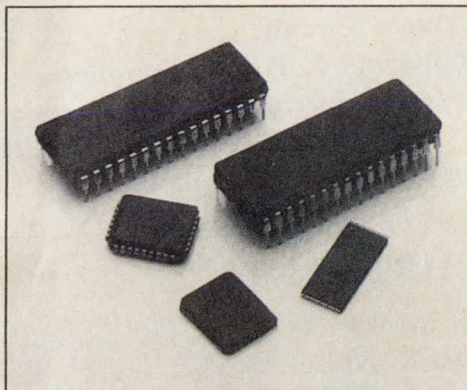
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FANTASTIC FL

AMD Ships 2 PLCC Flash



How Fast Is A Flash? A Direct Comparison

Density	AMD	Fastest Competitor
256K	90ns	120ns
512K	90ns	120ns
1 Mbit	90ns	120ns
2 Mbit	90ns	150ns

SUNNYVALE — The computer industry takes a giant leap forward in performance with the help of the new Flash memory family from Advanced Micro Devices, Inc.

Flash memory is a high-density, reprogrammable, non-volatile technology that has a bright future in computation, laser printers, network and telecommunications hardware. Many military systems use Flash technology in radar and navigational applications.

Flash memory also has the potential to eliminate mechanical hard disks and the need for cumbersome batteries. These are two of the biggest and heaviest obstacles in laptop and notebook computer applications.

Today, Flash memory is the most cost effective replacement technology for UV EPROMs and EEPROMs in applications that require in-system programming. Flash memories can literally be reprogrammed in a flash —

hence the name.

Standard, But With A Little More Flash

AMD's Flash memory family effectively etches in silicon the de-facto standard for this burgeoning technology that is compatible with Intel's initial Flash architecture.

Because AMD Flash memories are pin-for-pin compatible with the now standard architecture, AMD is positioned as an alternate source for design engineers and purchasing agents alike.

"Alternate source may be an inadequate term," said Jerry Sanders, chairman and CEO of Advanced Micro Devices. "Given our speed and feature set, our customers think of us as a superior resource."

Indeed, AMD's Flash memory family offers designers significant performance advantages (see chart), with speeds almost twice as fast as the nearest competitor.

**Engineer Spontaneously
Combusts At Meeting**

**Vice Pro
At Lee**

From AMD.

FOOD

Chips And Salsa

A Business Person's Guide To Silicon Valley Restaurants

PAGE 7F

ette

MORNING EDITION

ASHIES!

Megabit, 90ns, Memories

The AMD Flash family offers designers and purchasers many packaging options. Particularly popular is AMD's advanced 2 Megabit, PLCC part. Other packaging options include PDIP, CDIP and LCC in 256K, 512K, 1 Mbit and 2 Mbit capacities. TSOP packages will be available in the second half of this year. (LCC not currently available in 2 Mbit.)

AMD's 2 Mbit Flash memories come complete with embedded program and erase algorithms on board. These automatic algorithms speed up the design process and considerably shorten time to market. Previously, engineers were required to develop tedious and time-consuming algorithms to implement in-system reprogrammability. AMD's automatic algorithms also allow several Flash memories to be written or erased at once, without tying-up the CPU. The system is now free to perform other tasks while these operations are in

progress. AMD plans to include embedded algorithms in a future release of its 1 Mbit part.

The Ultra-Violet Blues

Flash technology is particularly suited to applications requiring reprogramming in place, because these devices can be reprogrammed in seconds, and within the system.

To update the code on a UV EPROM, the part must first be removed from the system. Once removed, erasure can take up to a full 20 minutes. After reprogramming, the part is then plugged back into the system. The process can result in damage to other components, costly service calls, and headaches.

Flash memories, on the other hand, can be bulk erased in about one to two seconds, without system disassembly. Reprogramming can then be accomplished via floppy disk, over phone lines, or even ISDN
(continued)

Stop the presses!

Advanced Micro Devices makes big news again—this time with an enhanced family of Flash memory devices.

That's good news for veteran and new Flash users alike.

Because our Flash devices are pin-for-pin compatible with Intel's existing Flash memory architecture, they establish the *de facto* industry standard.

Our standards, however, are a bit higher.

And so are yours.

That's why our Flash Memory family offers densities, speeds and packaging options that improve performance and save board space. For instance, our advanced 2 Mbit PLCC part with a scant 90 nanosecond delay.

You can also choose from Flash devices in 256K, 512K and 1 Mbit densities. As well as packaging options that fit your design best, including CDIP, PDIP, LCC, TSOP, and PLCC.

And you'll find implementation faster and easier than ever, because we've included automatic programming algorithms on all our 2 Mbit devices, and soon on our 1 Mbit parts, too. So you'll spend less time writing code, and take less time getting products to market.

To keep up to date with all the latest and greatest in Flash memory, call AMD today at **1-800-222-9323**. And start making some headlines of your own.



Advanced Micro Devices

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CIRCLE NO. 6

9

ident To Speak
Spelling Bee

How Orbit's Fores Out of IC Deve



Right Takes the Bite Development Costs.

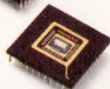
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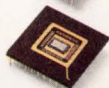
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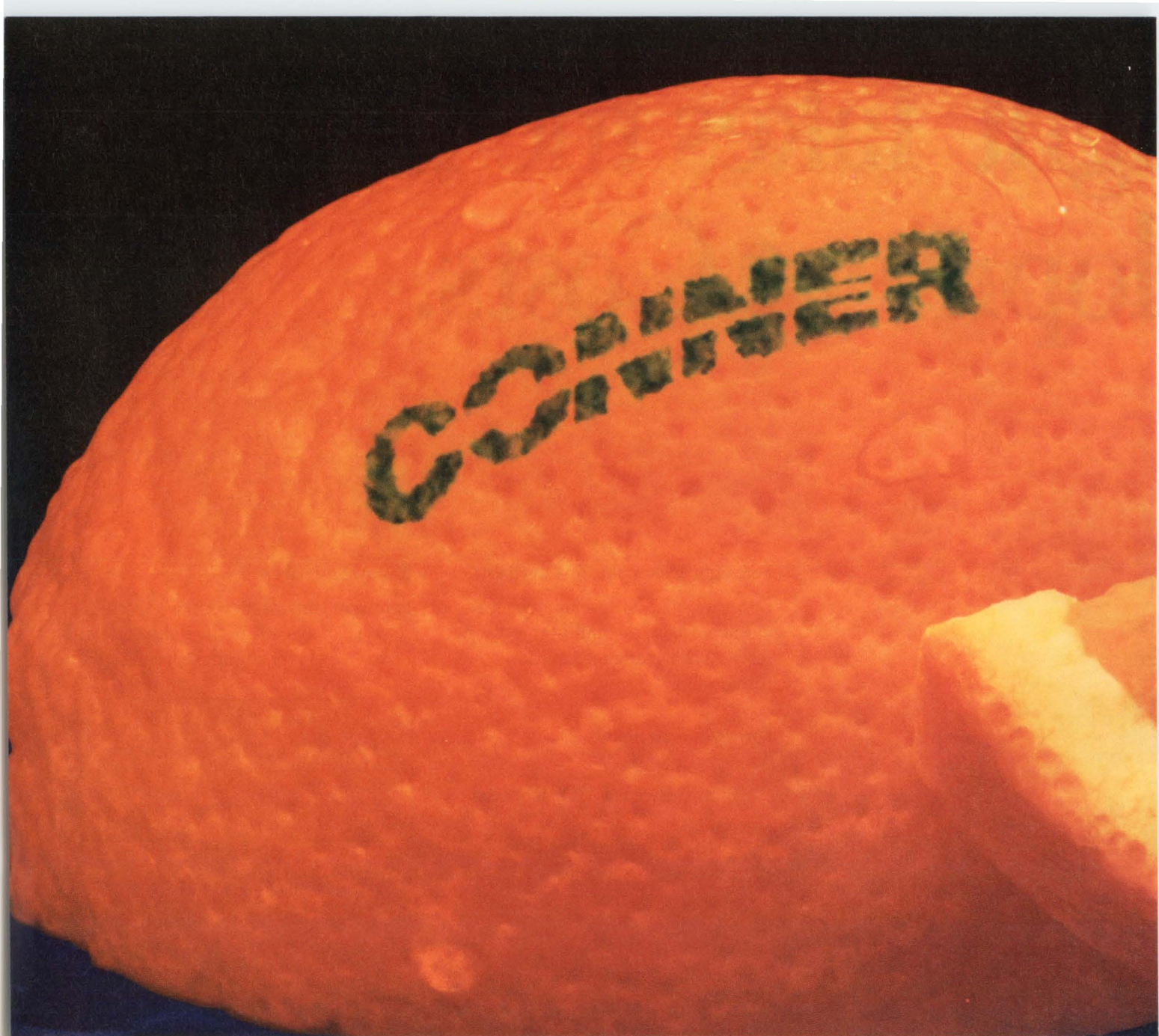


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What others promise, we guarantee.





ANY WAY YOU SLICE IT, GENERATION COVERS EVERY

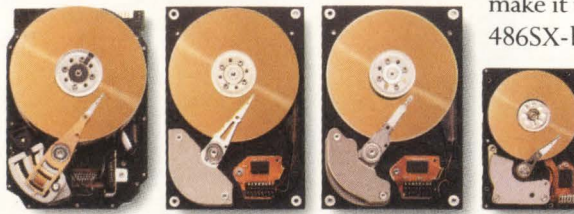
The squeeze is on. Today the PC market is rapidly concentrating into three segments: Notebooks, Desktops and Workstations. And once again, Conner has anticipated these changes.

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Then there's our new Jaguar Series for the desktop market—3.5-inch drives offering 85 and 170 Mbytes. A 17 msec. average seek time and a light weight, patented 1-inch



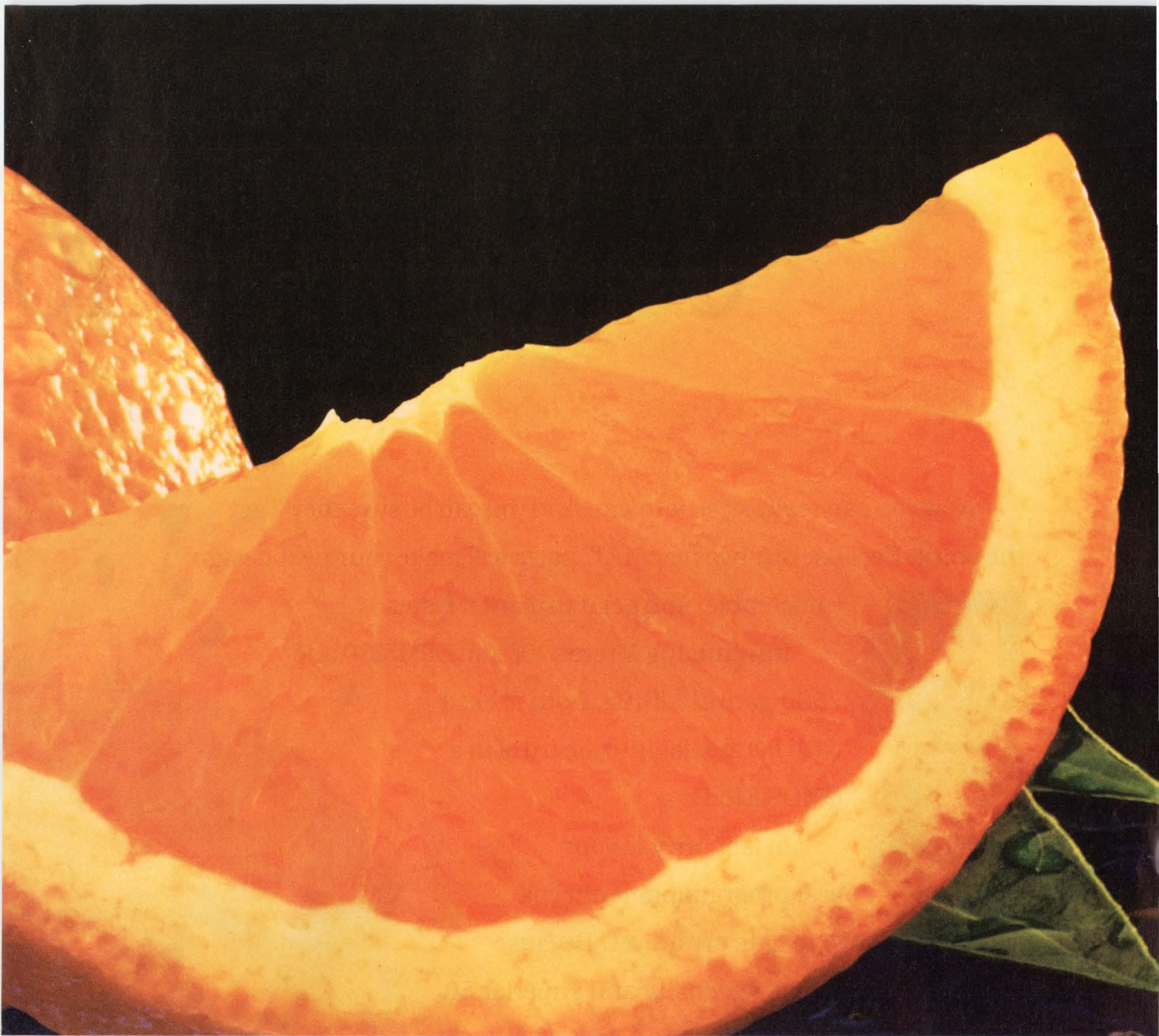
Summit 540 MB

Cougar 210 MB

Jaguar 85/170 MB

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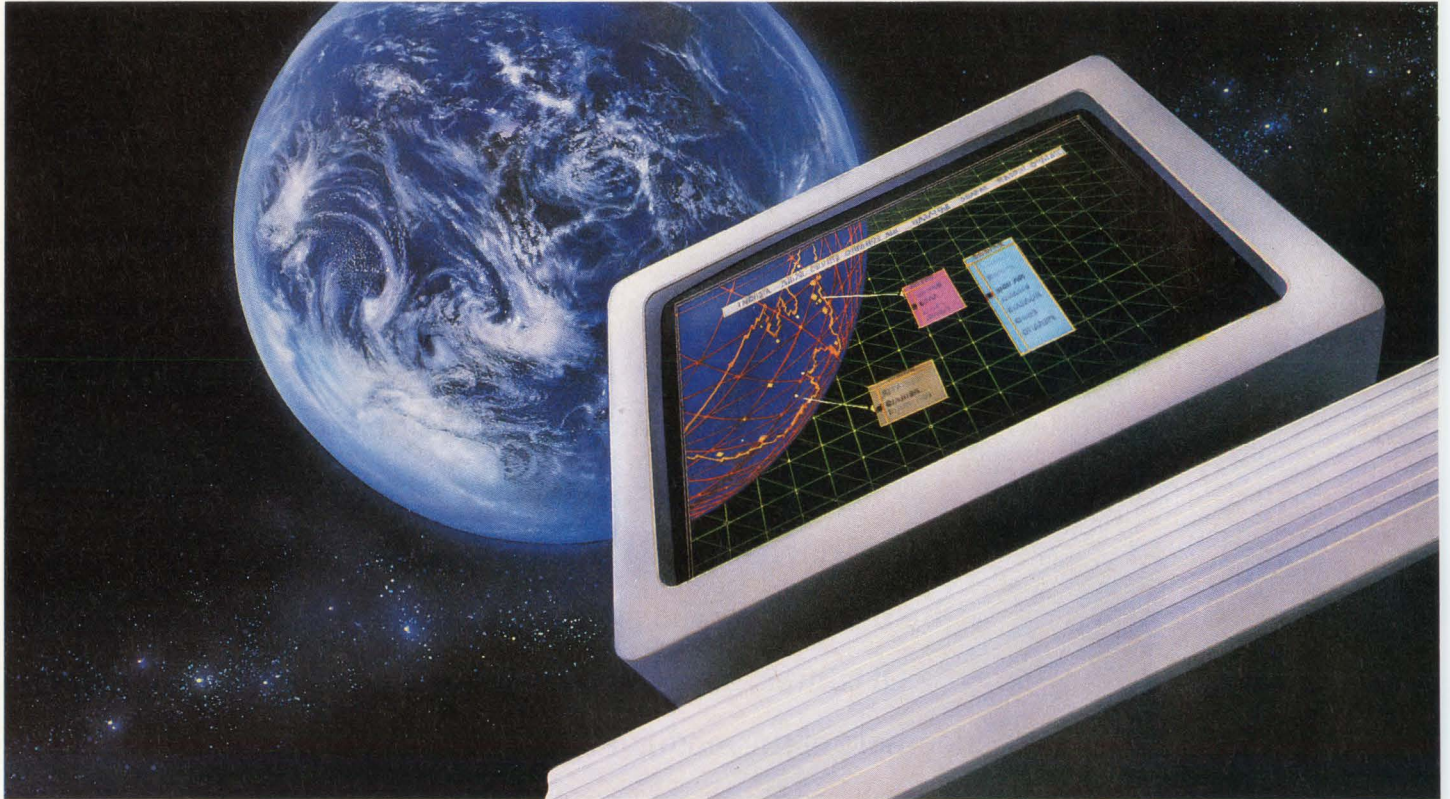
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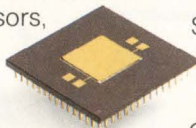
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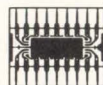
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NEWS BREAKS

EDITED BY SUSAN ROSE

DC/DC CONVERTERS DELIVER 3W ON FOUR BIPOLAR OUTPUTS

The HPR2xxx series of dc/dc converters provides as many as four isolated, bipolar outputs delivering 750 mW per channel (3W of total delivered power). The units in the series provide 750V isolation between channels. Various members of the family accept 5, 12, 15, and 24V and produce outputs of ± 5.2 , ± 12 , or ± 15 V. Both the inputs and the outputs of the device are filtered. The converters are packaged as single inline modules measuring $0.35 \times 2.22 \times 0.41$ in. and cost \$16.89 (1000). Burr-Brown Corp, Tucson, AZ, (602) 746-1111, FAX (602) 889-1510.—Steven H Leibson

PC PLUG-IN CARD PREFERS BASIC PROGRAMMING

The DPA1 from Signalysys Ltd is a DSP tool set comprising an IBM PC or compatible plug-in card and support software. The tool set offers a straightforward route to data acquisition and DSP, in real-time or off-line, by running programs in QuickBasic 4.5. The plug-in card provides two channels of differential input with a voltage range of ± 1.75 V and input impedance of 100 k Ω . Each channel uses an independent sigma-delta ADC, which you can program to sample as high as 400 kHz at 12 bits or 100 kHz at 16 bits. Sample skew between channels is <15 nsec. The card uses a 20-MHz T400 transputer (30-MHz T800 version is optional). The software tools include a Basic compiler from Fifth Axiom Ltd. Also in the software package are sample Basic programs for continuous, transient, and averaging signal analysis, which output a graphical display. To overcome speed limits of the PC bus in real-time applications, the card accommodates 1M byte (expandable to 4M bytes) of RAM for sample storage. A library of DSP routines includes digital filters and FFTs and a self-test program. The tool set (1M byte) costs £1750. Signalysys Ltd, Buckland, Aylesbury HP22 5HU, UK, (296) 631306, FAX (296) 631815.

—Brian Kerridge

DUAL COMPARATOR HAS SUB-NSEC PROPAGATION DELAY

The SPT9689 dual voltage comparator has a propagation delay of 850 psec max (650 psec typ) with the application of a 20-mV input-signal overdrive. The propagation delay varies less than 100 psec with input overdrives ranging from 5 to 50 mV. The device has a 3-dB bandwidth of 900 MHz and an open-loop gain of 66 dB. It requires 5V and -5.2V for operation and consumes less than 385 mW. Each of the comparators in the package has a separate ground pin to minimize crosstalk. The comparators' 30-mA outputs can drive 50 Ω loads. The \$11.70 (1000) device comes in a 20-contact leadless chip carrier, or a 16-lead ceramic DIP. Signal Processing Technologies, Colorado Springs, CO, (719) 540-3900, FAX (719) 540-3970.

—Steven H Leibson

WINDOWS 3.0 GAINS REAL-TIME DATA-ACQUISITION

Labdriver for Windows is a \$295 dynamic link library for the Microsoft Windows 3.0 graphical user interface. The library lets you perform real-time, multifunction data acquisition using the manufacturer's line of plug-in data-acquisition boards. This software provides double-buffering techniques and resource management to optimize data input and prevent multiple-board contention over DMA channels, interrupt levels, and bus channels. National Instruments Corp, Austin, TX, (800) 433-3488, (512) 794-0100, FAX (512) 794-8411.—JD Mosley

NEWS BREAKS

CAD DISPLAY CONTROLLER SMOOTHES JAGGED EDGES

Nth Engine/124 from Nth Graphics can perform antialiasing for 1024×768-pixel and 800×600-pixel images. The \$995 device appears to double the displayable resolution of your 2-D and 3-D wire-frame drawings. The antialiasing eliminates the jagged edges that appear when submegapixel monitors attempt to display diagonal lines. The board can display 16.8 million simultaneous colors on 640×480-pixel monitors, for photorealistic 24-bit color. The device's enhanced display-list processing drivers produce instant zooms and pans on AutoCAD drawings. The board comes with Hydra View/AC, a 3-D visualization program that works within AutoCAD Release 11, and uses the board's rendering capabilities. You also get a 16-bit Windows 3.0 driver and true-color drivers for Autoshade 2.0 and Autodesk 3D-Studio. Nth Graphics, Austin, TX, (800) 624-7552, (512) 832-1944, FAX (512) 832-5954.—J D Mosley

200-mW REGULATOR ICS HAVE CONTROL PIN

The SPT114 series of voltage regulators from Signal Processing Technologies are packaged in 0.130×0.134×0.049-in. SOT-23L surface-mount packages and can dissipate 200 mW. The devices feature a control pin that lets you switch the regulators on and off. While off, the ICs draw 500 µA. Devices are available with output voltages in 0.5V increments between 2 and 5.5V. The company also offers 3.25, 6, and 8V versions. The ICs cost \$0.83 (500). Signal Processing Technologies, Colorado Springs, CO, (719) 540-3900, FAX (719) 540-3970.—Steven H Leibson

ETHERNET INTERFACE IC HANDLES AUI AND TWISTED PAIR

The LXT901 Ethernet interface transceiver from Level One Communications handles both attachment-unit-interface (AUI) and 10Base-T (twisted-pair) media. The IC connects directly to any of several LAN controllers, including those from AMD, FMI, Intel, and National Semiconductor. All of the necessary signal filters are built into the IC; you need only an external isolation transformer to connect to the AUI drop cable or shielded or unshielded twisted pair. The IC can automatically select the active port and will detect and correct polarity errors. The IC comes in a 44-lead PLCC and costs \$19.32 (1000). Level One Communications, Folsom, CA, (916) 985-3670, FAX (916) 985-3512.—Richard A Quinnell

AGREEMENT PROVIDES PATHS FROM FPGA TO MILITARY ASIC

Users of Actel field-programmable gate arrays (FPGAs) who wish to convert their designs into military ASICs can now take one of two simple paths to achieve that transformation. Through its recently-announced SystemASIC program and an agreement with Actel, United Technologies Microelectronic Center offers bidirectional conversions between its mask-programmed gate arrays and Actel's FPGAs. One option lets you design an ASIC using the company's cell libraries and then convert your design into an FPGA for prototype testing. When your design is solid, the company will build the mask-programmed part using its radiation-hardened, military-standard, or level-S (space-qualified) gate arrays. Alternatively, you can create your design using FPGA tools, test the prototype FPGAs, and the company will convert your net lists and behavioral descriptions into mask-programmed parts. NRE charges for the ASICs start at \$35,000, which gets you 10 prototype parts in eight weeks. Actel, Sunnyvale, CA, (408) 739-1010, FAX (408) 739-1540. United Technologies Microelectronics Center, Colorado Springs, CO, (719) 594-8000, FAX (719) 594-8187.—Steven H Leibson

New Schematic Capture Front End for PSpice

MicroSim Corporation now offers a versatile schematic capture front end, called Schematics, to our popular Circuit Analysis programs, PSpice and Probe. Schematics provides a unified system for designing and editing schematics, running analyses using PSpice, and viewing the results using Probe, all without leaving the Schematics environment. Any mix of analog and digital components can be used when defining a schematic for simulation.

Schematics provides a menu-driven interface for specifying analysis parameters and running simulations directly from the schematic display. If device simulation parameters need adjustment after running a simulation, they can be easily modified and the simulation rerun. Netlists for PSpice are generated automatically and can be examined on the screen.

Schematics was designed and written as a native Windows 3.0 application for the PC and is also available as an OpenWindows application for the Sun-4 and SPARCstation. Both packages include the Schematics library with symbols for all parts contained in the PSpice libraries—over 3,500 analog and 1,500 digital components. An integrated symbol editor with full editing capability allows new symbols to be created and new part attributes to be defined while working on a schematic.

Schematics is sold as part of the Genesis package and comes with MicroSim Corporation's extensive customer/product support. Our expert engineering team is always on hand to answer your technical product questions.

For further information on Schematics, or any other MicroSim Corporation product, call toll free at (800) 245-3022 or FAX at (714) 455-0554.

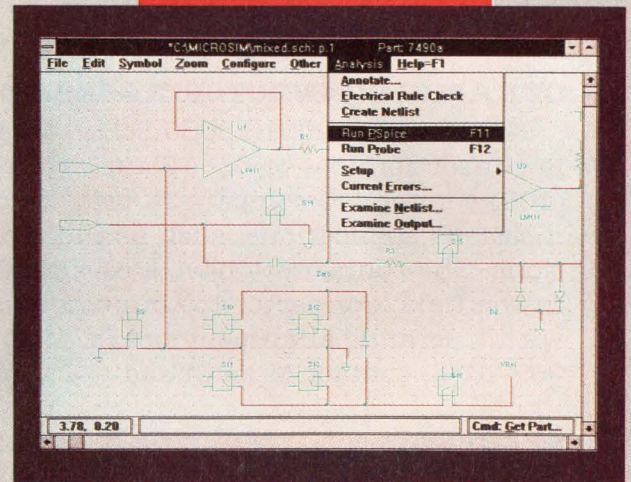


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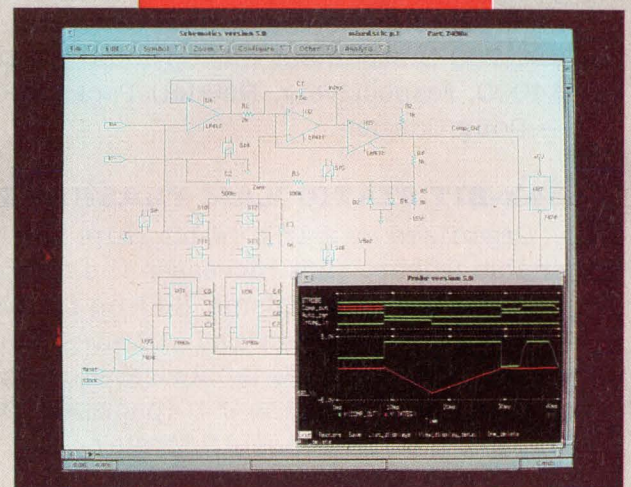
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Schematics as a Windows 3.0 application



Schematics with Probe

NEWS BREAKS

PREDICT EFFECTS OF GROUND BOUNCE ON SYSTEM TIMING

Quad Design's Crosstalk Tool Kit release 4.2 predicts the effects of ground bounce on system timing. The software models simultaneous switching interactions with power and ground inductances for each chip on a pc-board. The tool kit provides signal quality analysis across multiple pc-boards and systems with backplanes. The software also automatically generates behavioral simulation models for nonlinear circuit drivers and receivers from Spice models. The software will be available the third quarter of 1991. The package starts at \$27,000; current users with maintenance contracts receive free upgrades. Quad Design, Camarillo, CA, (805) 988-8250.

—Doug Conner

CERAMIC CONNECTOR EASES TERMINATION

The MX Plus 86010-6000 Series ceramic connectors from Molex offers a maximum low-insertion loss of 0.7 dB and are compatible with AT&T's ST connectors. The \$4.78 (100) connectors compare in price to metal connectors. The devices suit data communications applications, such as those found in LANs and instrumentation installations. The connectors have a ceramic ferrule for easy connection and termination in the field. Connector to connector mating combines a molded polymeric housing with a ceramic alignment sleeve. Molex, Des Plaines, IL, (708) 803-3600, FAX (708) 969-1352, contact Mike Quaas.—J D Mosley

SPECTRUM AND NETWORK ANALYZER IN ONE INSTRUMENT

The HP 3589A from Hewlett-Packard lets you measure frequency, distortion, phase, group delay, return loss, and impedance on signals from 10 Hz to 150 MHz. A time-gated, spectrum-analysis feature lets you restrict your signal measurements to a desired portion of a signal for burst-type or time-varying signals. Using the time-gated feature, you can make noise level, signal-to-noise, and distortion measurements of signals that would otherwise be difficult or impossible to measure. The \$21,750 instrument has optional 50 and 75 Ω S-parameter test sets for \$3650 and \$4000, respectively. Hewlett-Packard Co, Cupertino, CA, (800) 752-0900.

—Doug Conner

64k-BIT STATIC RAM FLASHES 10-NSEC ACCESS TIME

Organized as a 16k \times 4-bit chip, the MCM6290CJ10 from Motorola has an output-enable feature that increases the chip's flexibility by making it easier to eliminate bus-contention problems. Selling for \$30 (1000), this static RAM is TTL-compatible with a 3-state output and operates from a single 5V power source. Requiring 120 mA of power, the IC is fabricated from 0.8- μ m CMOS and comes in 300-mil plastic DIP and small-outline J-10 packages. Motorola MOS Memory Products Div, Austin, TX, (512) 928-7726.—JD Mosley

MEMORY CARDS PROVIDE SIMPLE UPGRADES FOR PORTABLES

Texas Instruments' one-time programmable memory cards range in price from \$73 for 64k-byte cards to \$160 for 512k-byte cards. These credit-card-size dynamic RAMs (DRAMs) let you customize applications for portable instruments and computers by storing programs or expanding on-board memory. The cards have 200-nsec access-times and consume less power than conventional disk-drives. An 80-nsec, 1M-byte DRAM card costs \$340 in sample quantities. The cards use a JEDEC-format, 60-pin, two-piece connector and orientation guide. Texas Instruments, Dallas, TX, (800) 336-5236 ext 700, (214) 995-6111 ext 700.—JD Mosley



PROFILES IN PARTNERING

Motorola® and Dale®

PRODUCTS: Metal film resistors manufactured to MIL-R-39017 (RLR) and MIL-R-55182 (RNC).

OBJECTIVE: Integrate Dale RNC and RLR resistors into Motorola Government Electronic Group's (GEG) Approved Manufacturer's Part Program.

UNITS INVOLVED: Motorola GEG and Dale Film Resistor Division.

Dale and Motorola have a long history of working together in a conventional vendor/customer mode. One of the major product lines supplied by Dale has been metal film resistors.

During the second quarter 1990, GEG and Dale's Metal Film Division began a Supplier Continuous Improvement Plan. This plan initially targets specific Military and Established Reliability metal film resistors (RLR/RNC) for integration into Motorola GEG's Approved Manufacturer's Parts Program (AMPP).

Following this, the plan is keyed to integrating all Dale Film Resistor products into AMPP — which is a "no-inspect" dock-to-stock program. The agreement was an outgrowth of intensive Total Quality Management pro-

grams at both companies and was driven by Motorola's well-known Six Sigma commitment and Dale's Commitment to Continuous Quality Improvement.

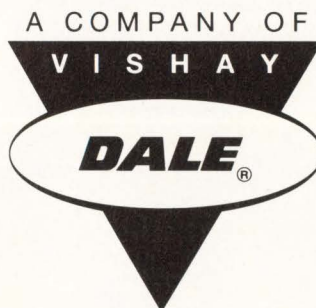
The Supplier Continuous Improvement program is administered by Passive Commodity personnel from Motorola's GEG Supply Management Organization in conjunction with a Dale team which includes top management and extends throughout the work force. Its framework was established beginning with a thorough evaluation of Dale's overall quality management system and its metal film resistor manufacturing process control and SPC plans.

As a part of this plan, RNC and RLR resistors were received by Motorola GEG at a 99.70% acceptance rate in 1990 and a

99.82% acceptance rate in early 1991. In both cases, Dale's Metal Film Division exceeded the continuous improvement plan acceptance rate goals. To facilitate this, the two companies established a system of open communication which: (1) permits quick identification of areas where corrective action is needed; (2) establishes a reporting system to identify action taken to isolate the root cause and prevent reoccurrence; and (3) uses regular Quality/Business Reviews as a means to track progress toward the goal of Zero Defects on all material delivered to Motorola.

In conjunction with the plan, Dale is actively expanding its own partnering program for certifying the suppliers of raw material to all of its divisions and is preparing to be a competitor for the Malcolm Baldrige Quality Award.

If you would like more information about how Dale's Commitment to Total Quality Management (TQM) Improvement can be applied to your project goals, please contact Joe Matejka, Vice President Quality Assurance, Dale Electronics, Inc., 1122 23rd Street, Columbus, Nebraska 68601-3647. Phone 402-563-6511. Fax 402-563-6418.



FILTERS



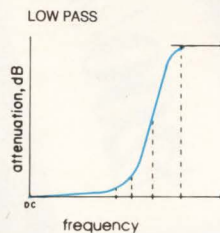
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- 5-section, 30dB/octave rolloff • VSWR less than 1.7 (typ) • meets MIL-STD-202 tests
- rugged hermetically-sealed pin models • BNC, Type N; SMA available
- surface-mount • over 100 off-the-shelf models • immediate delivery

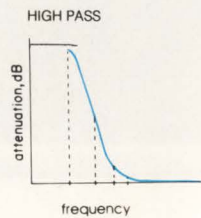
low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB)		STOP BAND, MHz (loss >20dB) (loss >40dB)			VSWR		PRICE \$ Qty. (1-9)
	Min.	Nom.	Max.	Max.	Min.	pass-band typ.	stop-band typ.	
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45



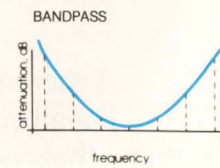
high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB)		fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss >20dB) (loss >40dB)		VSWR		PRICE \$ Qty. (1-9)
	Min.	Min.		Min.	Min.	pass-band typ.	stop-band typ.	
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95



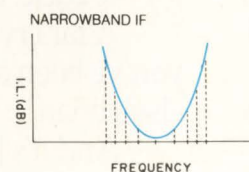
bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB)		STOP BAND, MHz (loss > 10 dB) (loss > 20 dB)				VSWR 1.3:1 typ. total band MHz	PRICE \$ Qty. (1-9)
		Max. F1	Min. F2	Min. F3	Max. F4	Min. F5	Max. F6		
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB		STOP BAND, MHz I.L. > 35dB		PASS-BAND VSWR Max.	PRICE \$ Qty. (1-9)
			F5	F6	F7	F8-F9		
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
PBP-60	60.0	55.0-67.0	44	79	4.6	190-1000	1.7	18.95
PBP-70	70.0	63.0-77.0	51	94	6	193-1000	1.7	18.95



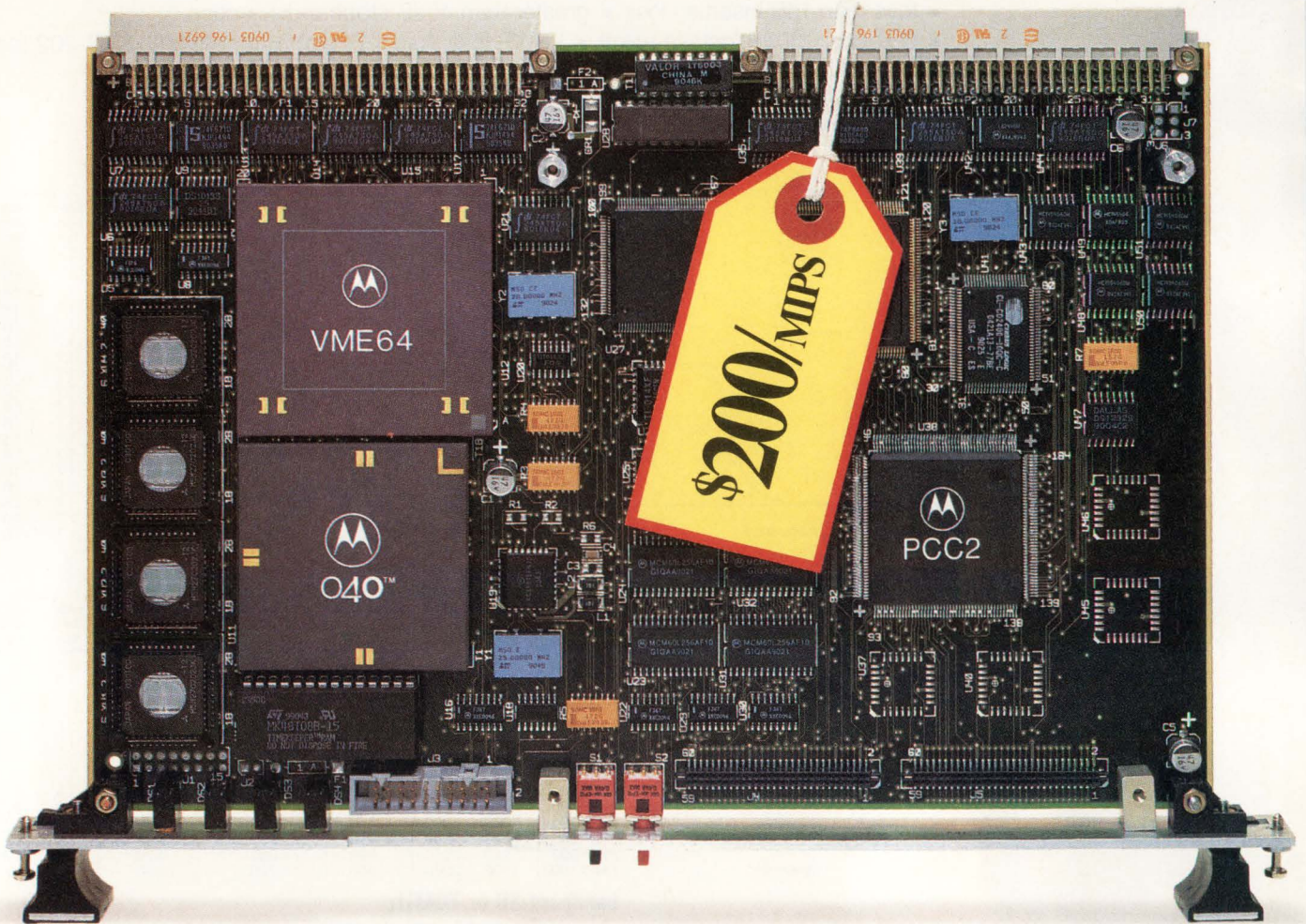
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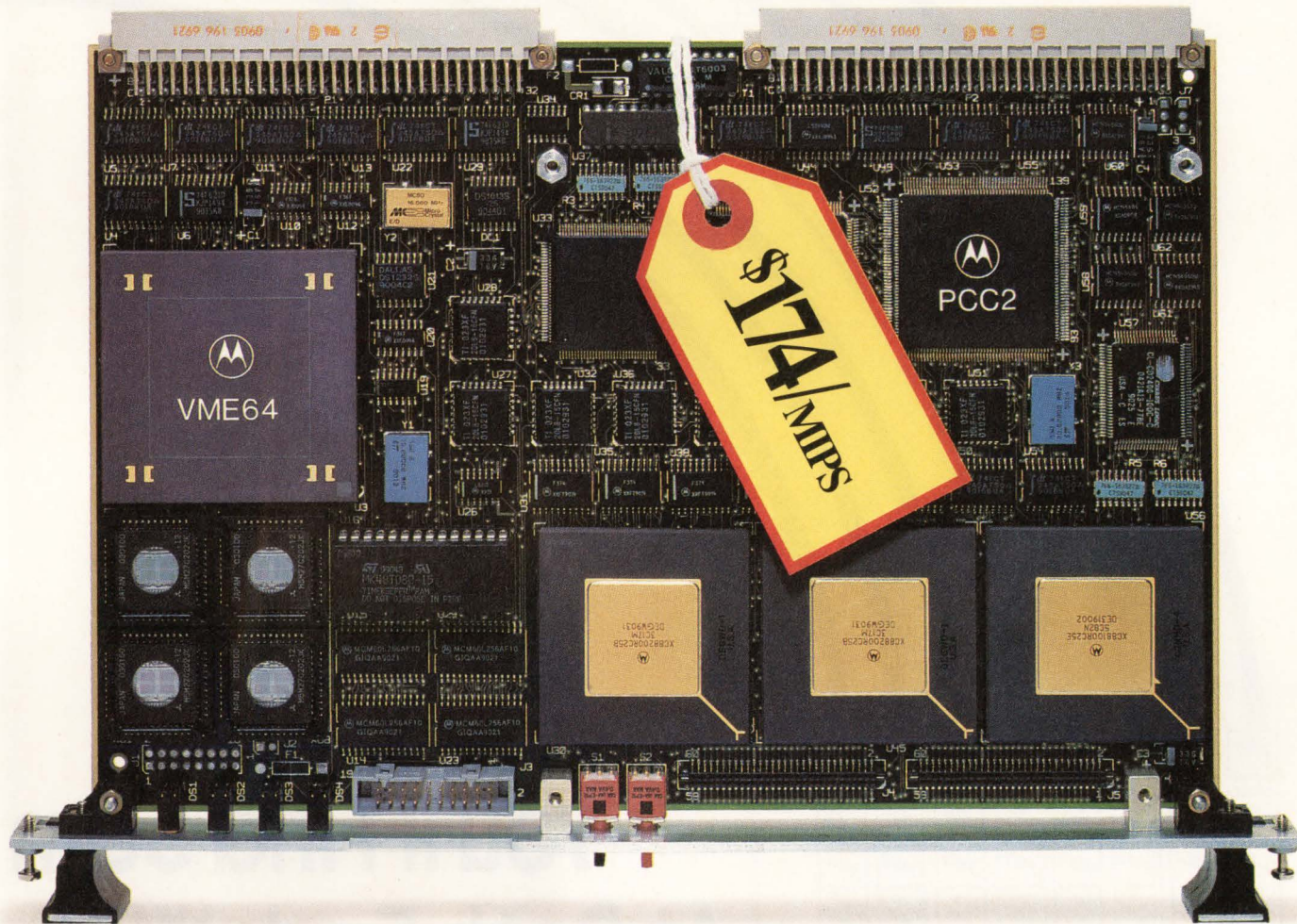
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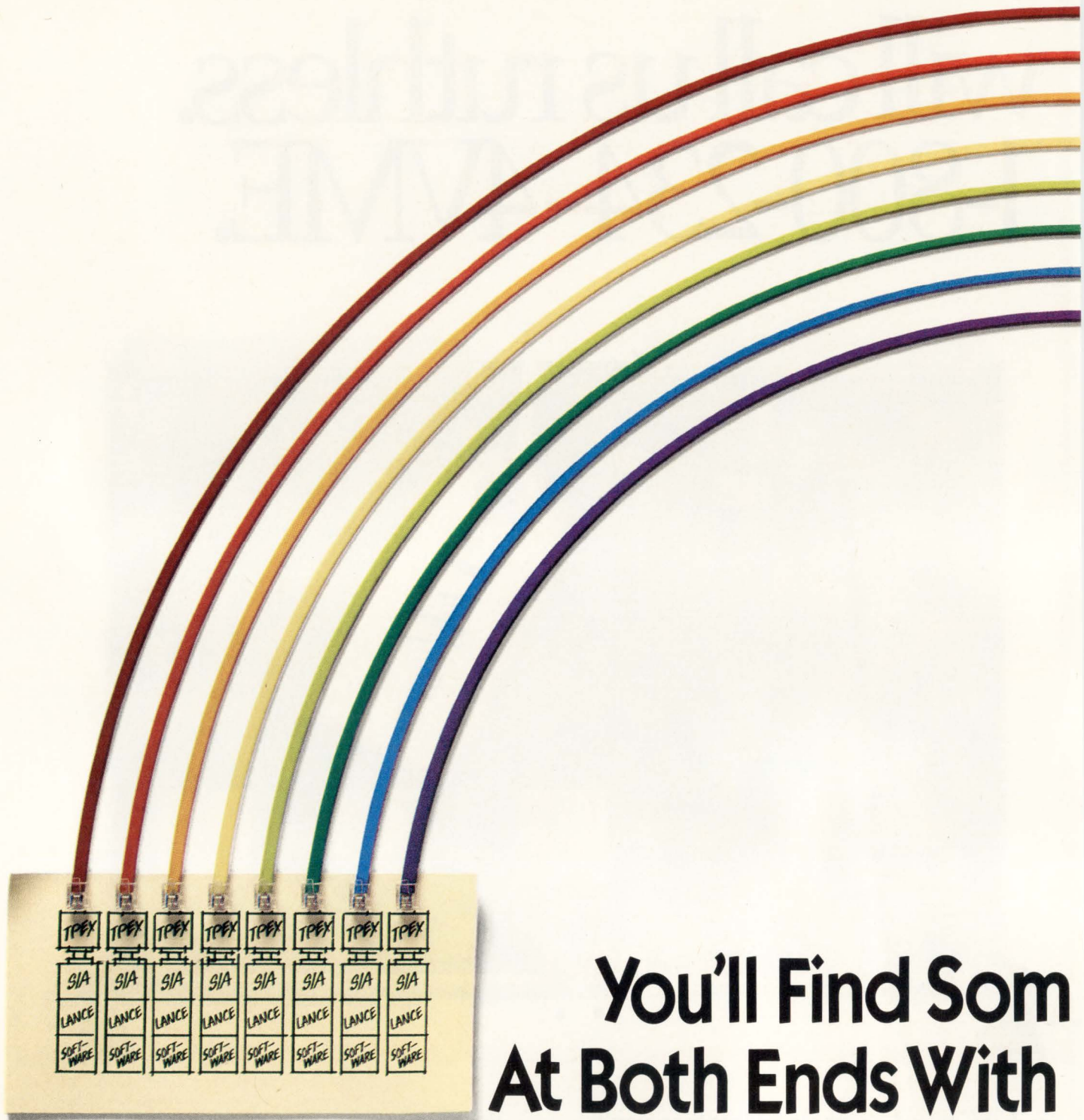
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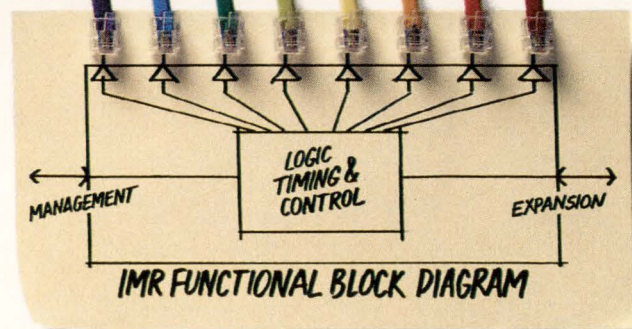
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SIGNALS & NOISE

Alerting readers to possible adverse effects

In the December 1990 issue of *Stereophile*, an article on contact cleaners and enhancers agrees with the positive comments about Cramolin in the article, "Fluids vanquish intermittent contacts" (EDN, March 14, 1991, pg 59). However, the "Stereophile" article also warns of possible adverse effects of Stabilant 22 over time, when used with dissimilar metals.

The EDN article mentions the porosity of plated gold and how it lets contaminants pass through the base metal. The "Stereophile" article describes contamination chemically generated by Stabilant 22 (Tweek) between thinly plated gold connectors.

To avoid problems with Stabilant 22, the minimum required plating thickness should be known as well as the performance expected under environmental conditions more severe than the shop-floor aging reported by the D W Electrochemicals Ltd tests.

W C Wright
Fullerton, CA

(Ed Note: The referenced article points out that Stabilant 22A may allow a chemical reaction to occur between contacts made of dissimilar metals and that the reaction products can degrade a connection's conductivity.)

Missing information

EDN missed some features of Quad Design Technology's Transmission Line Checker (TLC) and Crosstalk Toolkit (XTK) when summarizing transmission-line analysis products in Table 1 of the article, "CAE tools help cure transmission-line woes" (EDN, March 1, 1991, pg 47). Both tools handle analysis as well as post-placement screening. They calculate trace and settling delays, and detect overshoot, undershoot, and

multiple threshold crossings. The XTK tool also handles lossy line modeling. EDN regrets the error and any confusion that resulted.

Missing from manufacturers' box

In the article on spectrum analyzers (EDN, May 9, 1991, pg 100), the following company's name and address were omitted:

Advantest Corp
300 Knightsbridge Pkwy
Lincolnshire, IL 60069
(708) 634-2552
FAX (708) 634-2610.

Correct address and phone number

In the article "Analog Spice simulation models: Accurate models mirror extremes of operation" (EDN, May 9, 1991, pg 61), the correct address and phone for Intusoft is:

Box 710
San Pedro, CA 90731
(213) 833-0710
FAX (213) 833-9658.

IT'S EASY TO HAVE YOUR SAY

EDN's Signals & Noise column provides a forum for readers to express their opinions on issues raised in the magazine's articles or on any topic that affects the engineering industry. You can use one of several easy ways to reach us. First, there's always the mail. Send your letters to Signals & Noise Editor, EDN Magazine, 275 Washington St, Newton, MA 02158. Or, send us a message via MCI mail at EDNBOS. Finally, EDN's bulletin-board system is ready for use—and it's free (except for the phone call). You can reach us at (617) 558-4241 and leave a letter in the EDITORS Special Interest Group. You'll need a 2400-bps (or less) modem and a communications program that is set for eight data bits, no parity, and one stop bit, or 1200/2400, 8,N,1 in shorthand.

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Kit provides serial interface to IBM PC for quick prototyping. Board also supports displays up to 240 x 128 pixels.

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* The CY325 LCD Windows Controller provides parallel or serial high-level control of Instrument-size LCDs. Up to 256 built-in windows support window-relative text, bargraphs, waveforms, and plots. Text and graphics are maintained in separate planes, facilitating special effects. Complete User Manual included.

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Kit also includes:

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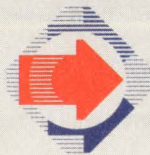
Oki High-Performance ICs

Part Number	Description
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MSM514221A	262,263-word x 4-bit, 1-Mb serial memory with self-refresh control circuit
MSM10S0000	0.8 μ m SOGs, true 82xx, UARTs, memories, standard 24ma drive, 300ps, >500MHz logic
MSM6388	Solid-state recorder/IM serial register I/F
MSM67620	16-bit MCU with 16KB ROM, 512B RAM, 56 I/Os, 3 x 16-bit timers, 2 x 8-bit timers



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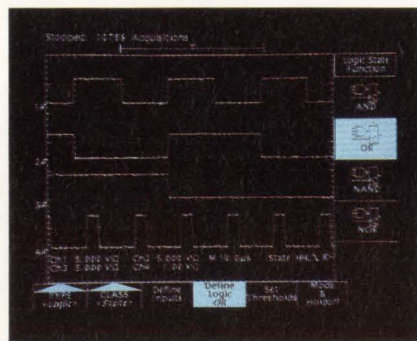
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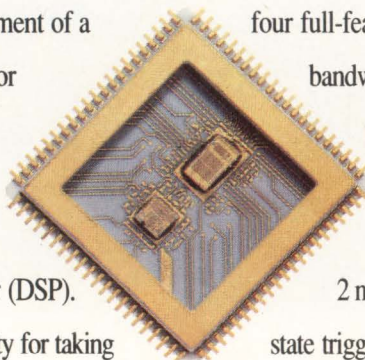
four full-featured channels. 500 MHz bandwidth. Up to 1 GS/s sam-

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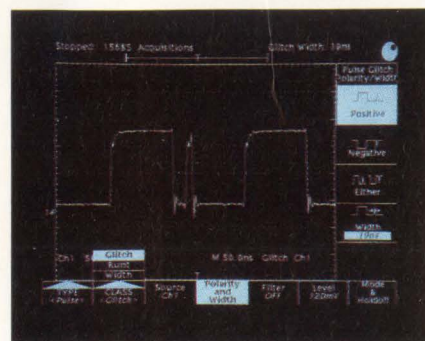
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2 ns glitch, runt, pattern and

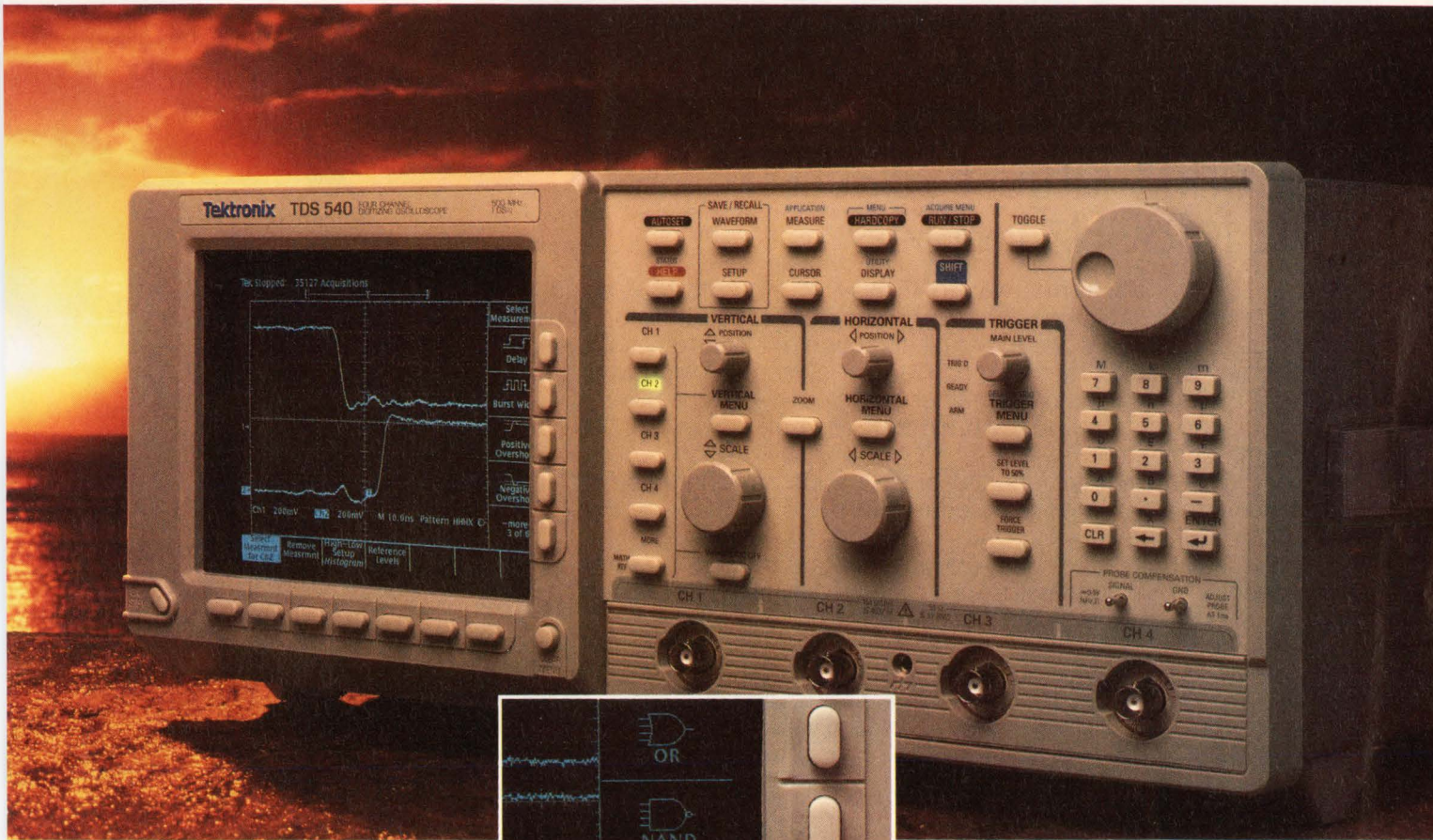
state triggers. With acquisition sensitivity and fast overdrive recovery bringing greater waveform detail within your grasp.



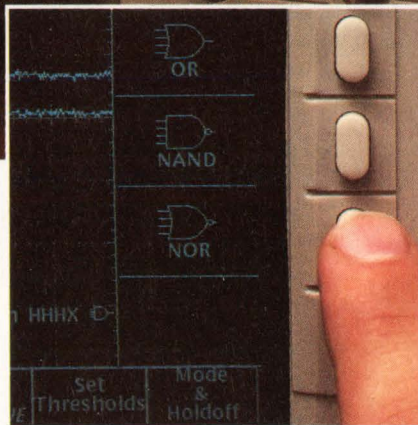
And if you think oscilloscopes aren't as easy to use and comprehend as they



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could be, you owe yourself a demo of the TDS. Its simplified front panel, VGA-quality display resolution, on-line help text, innovative icons that instantly differentiate menu functions — all add up to a scope that makes the user's manual more a formality than a necessity.



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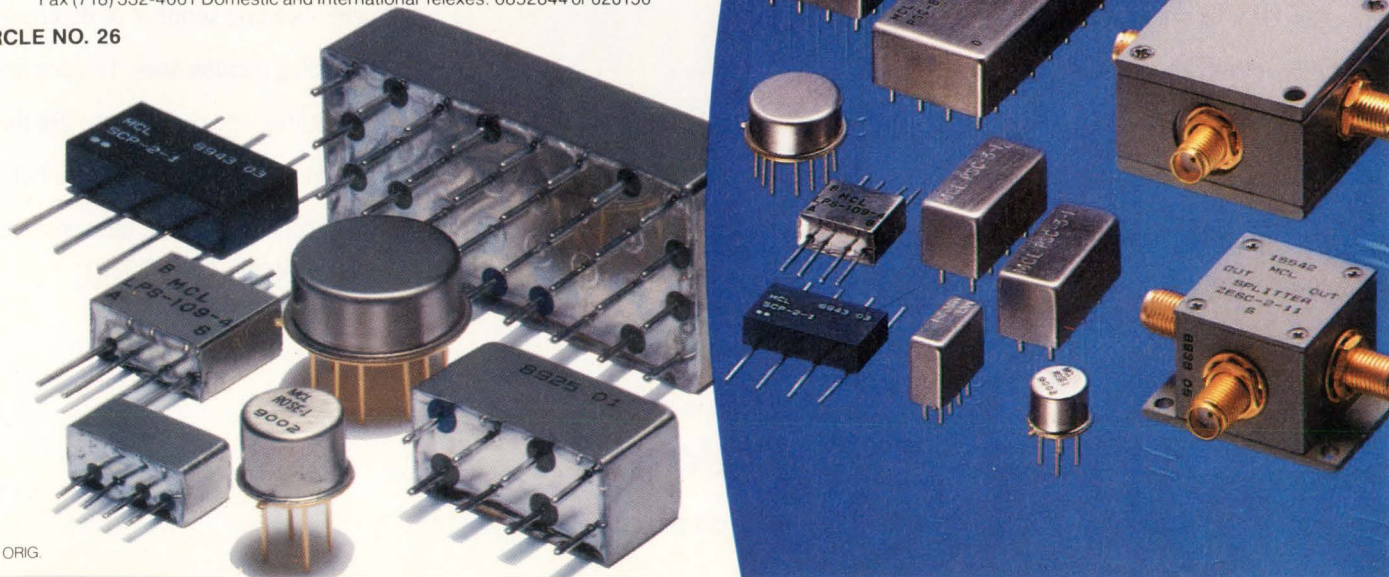
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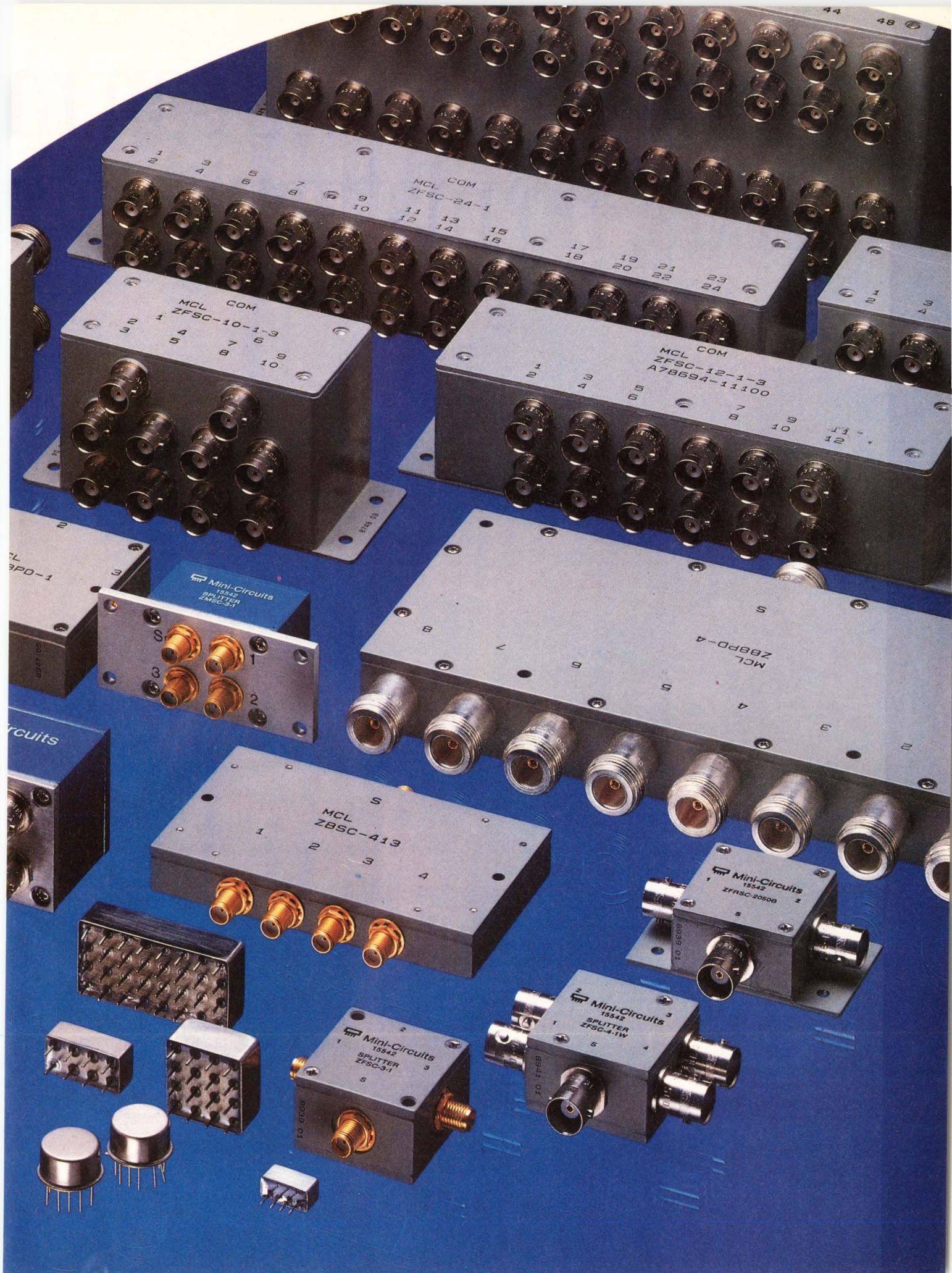
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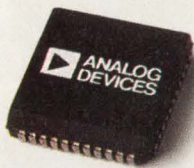
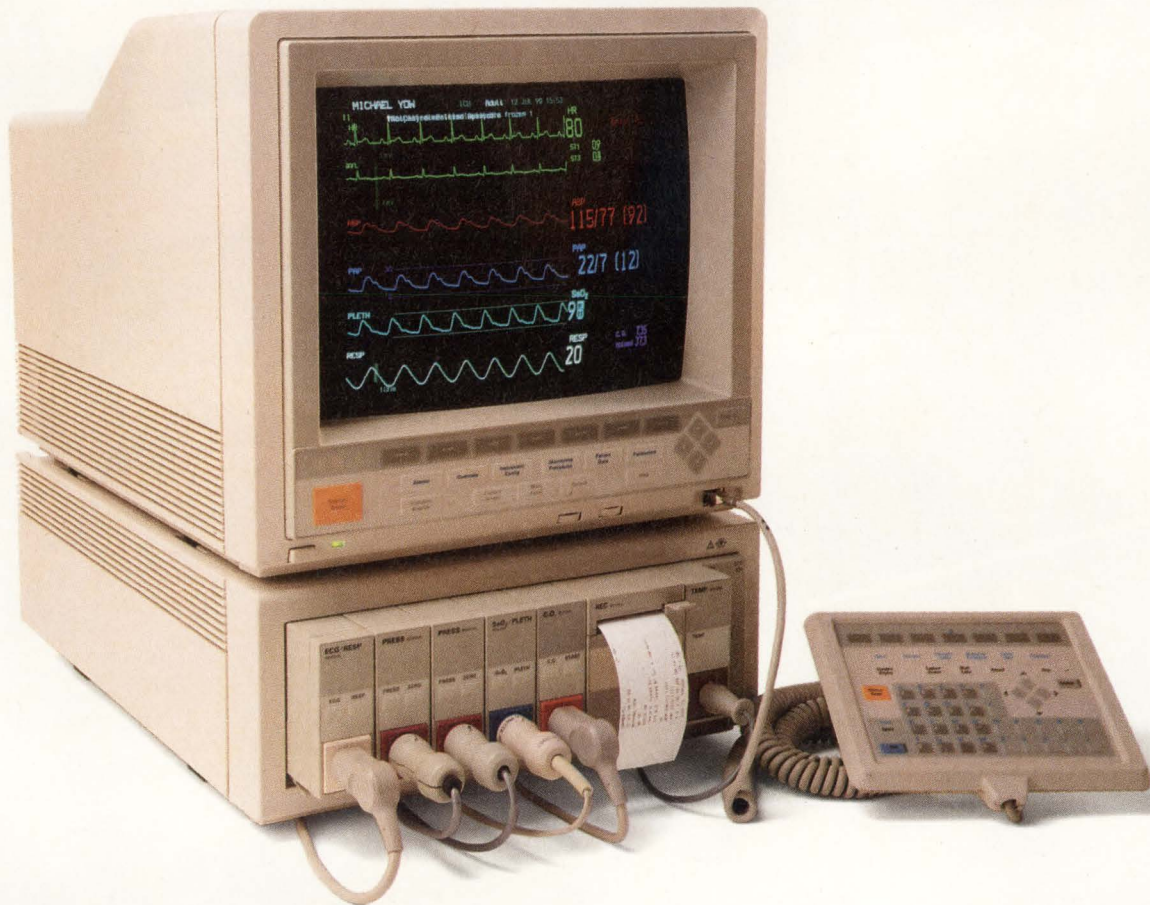
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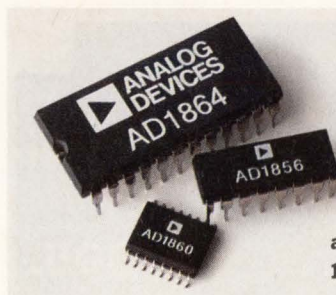
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EDITORIAL

Time to vote for innovation



The time has come to vote in EDN's Annual Innovation and Innovator competition. You'll find a complete list of the finalists and a ballot in this issue on page 49. The finalists whom our editors have chosen represent the most innovative products and people among the applications submitted to us for judging. In most cases, the finalists stand out from the other entries for specific reasons. Our selections might seem biased unless you understand the criteria we apply. To us, a product is innovative when:

- It offers significantly higher levels of performance in ways not previously available.
- It solves a continuing problem much more effectively than its predecessor—if any.
- It exhibits a marked degree of "cleverness," which differentiates it from earlier products.
- It embodies new technology that advances the state of the art or uses older technology in a unique and innovative way.

Such products might not have an immediate, widespread, or obvious use. Some innovative products take time to catch on and fire the imagination of designers.

Our editors also look for innovative people and design teams. They seek people who did innovative work and people who work in innovative ways. Perhaps a group of workers broke through management barriers to increase their efficiency and creativity. In the same vein, an engineer could have made a significant breakthrough in designing a product or part of a product.

Now that you know what we look for, take a few minutes to review the finalists and vote for your choices. We'll announce the winners at Wescon '91 in San Francisco. You'll also hear about the winners in EDN's magazine and news editions.

As you review the finalists, you may be disappointed that none of your company's products or people are among the finalists. Even though a great deal of work goes into each application, we can select only a few finalists in each category. On the other hand, your company may have never entered this year's competition. If you want to be sure to receive a nomination packet for the 1992 Innovation and Innovator awards, drop me a note and I'll make sure we send you one. If someone else in your company should get the information, let me know and I'll make sure we send it to them, too. The awards program is international, and we seek and receive entries from companies worldwide.

For information on the 1992 awards program, circle number 802 on the Information Retrieval Service form in this issue or send your request via mail to EDN Innovation Awards, EDN Magazine, 275 Washington Street, Newton, MA 02158 USA. You can reach me via fax at (617) 558-4470.



Jesse H. Neal
Editorial Achievement Awards
1990 Certificate, Best Editorial
1990 Certificate, Best Series
1987, 1981 (2), 1978 (2),
1977, 1976, 1975

American Society of
Business Press Editors Award
1988, 1983, 1981

A handwritten signature in black ink that reads "Jon Titus".

Jon Titus
Editor

Send us your comments via FAX at (617) 558-4470, or on the EDN Bulletin Board System at (617) 558-4241 300/1200/2400, 8, N, 1.

HOW ENGINEERING SEES OUR NEW 32-BIT INTEGRATED PROCESSOR.



Actually, a bullet doesn't do it justice. But you get the picture. Motorola's new 68330 integrated microprocessor is fast.

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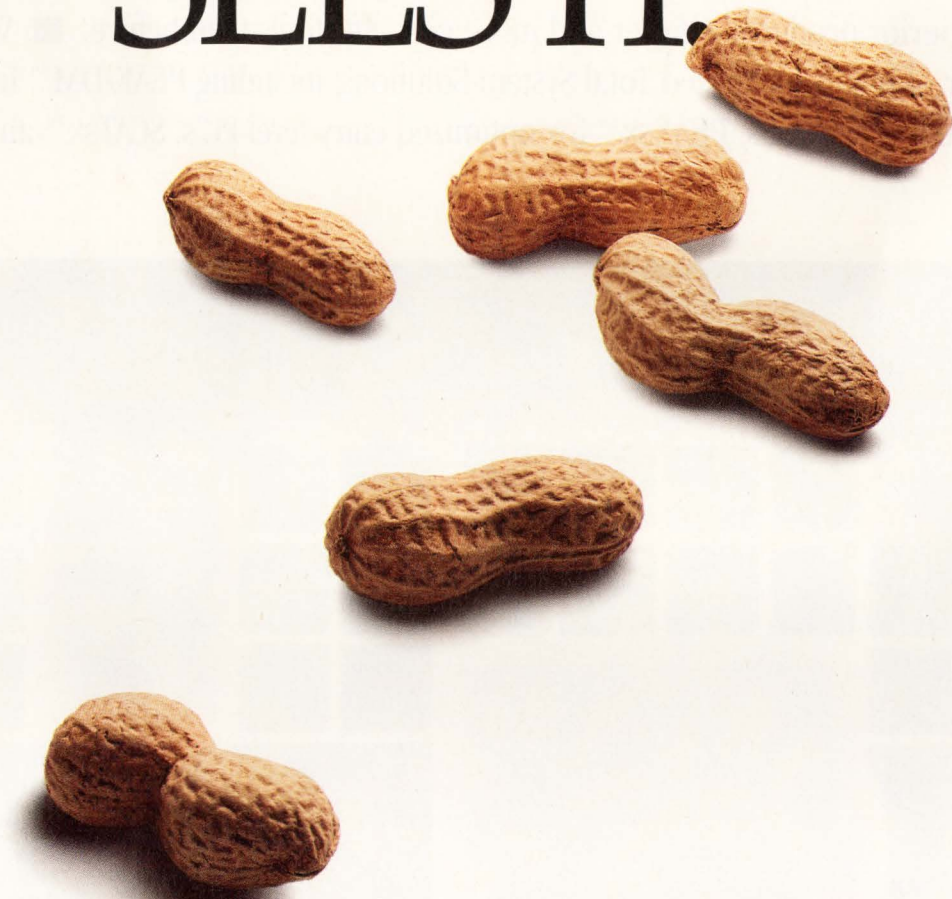
What's more, the 68330's Systems Integration Module comes already loaded with system glue logic. Saving you the trouble of designing in functions like clock

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68000 CPUs Architectural Integration	000	020	030	040
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Motorola's 68000 families let you choose the performance and integration that's right for your application.

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HOW PURCHASING SEES IT.



generation, chip selects and interrupt control.

And, since the '330 is fully binary software compatible with all members of the 68000 and 68300 families, it provides a seamless migration path, reams of reusable code, popular operating systems and familiar development tools.

All of which can save you a lot of trouble, while lowering overall system costs and raising your accountants' morale.

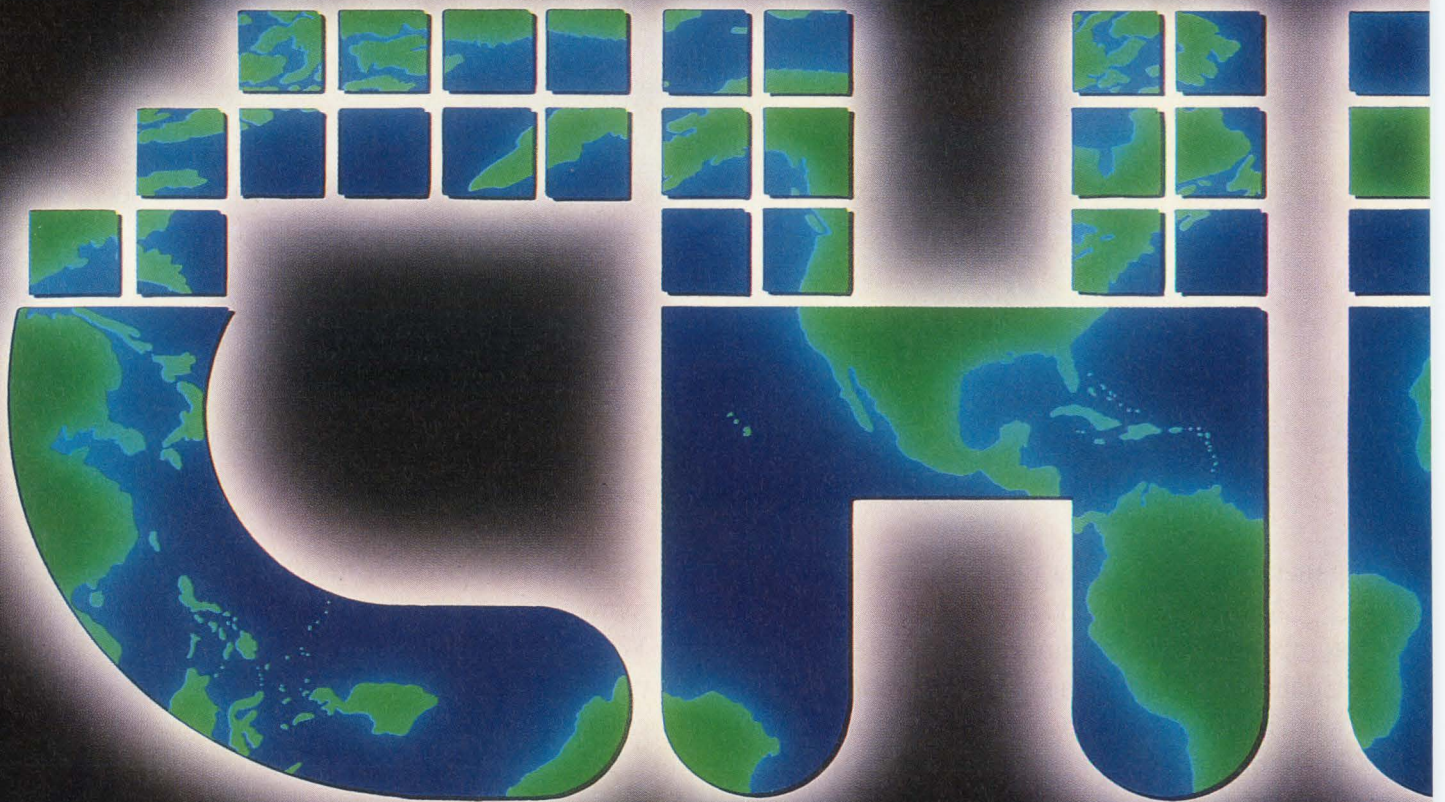
So if you're looking for 32-bit performance at a 16-bit system price, call 1-800-845-MOTO. Ask for a free 68330 product sample* and discover a high-caliber value.



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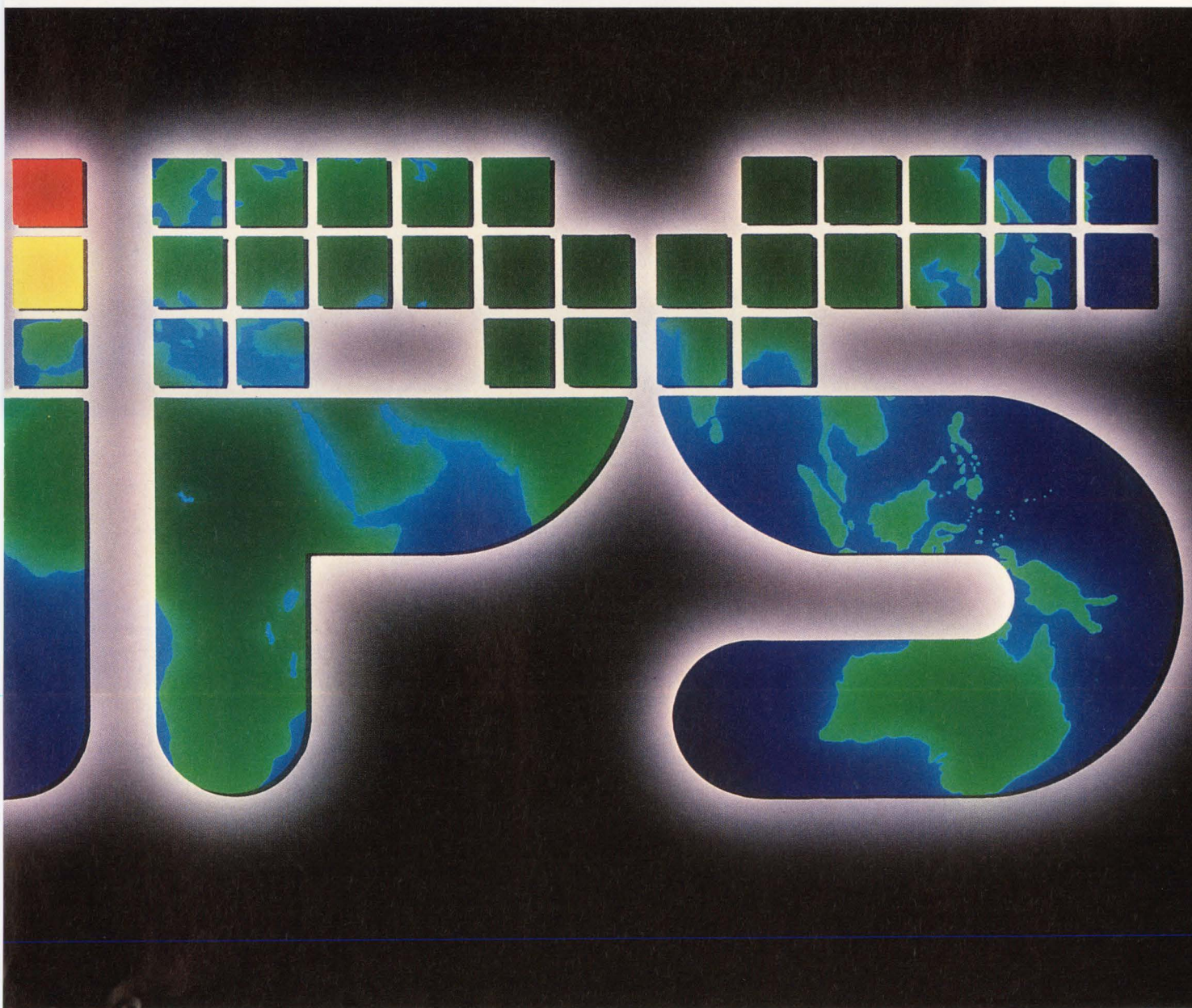
power conscious notebooks. We also have a complete line of CHIPSets for both flat-panel and CRT applications requiring VGA resolution and beyond. Plus PC Video™ for Multimedia, and PUMA™ for graphics acceleration. And we've got Data Communications and Mass Storage solutions too! ■ Call us at 1-800-323-4477 x2355 or fax us at 408-434-0412 for the sales office nearest you and get started on your next design today.

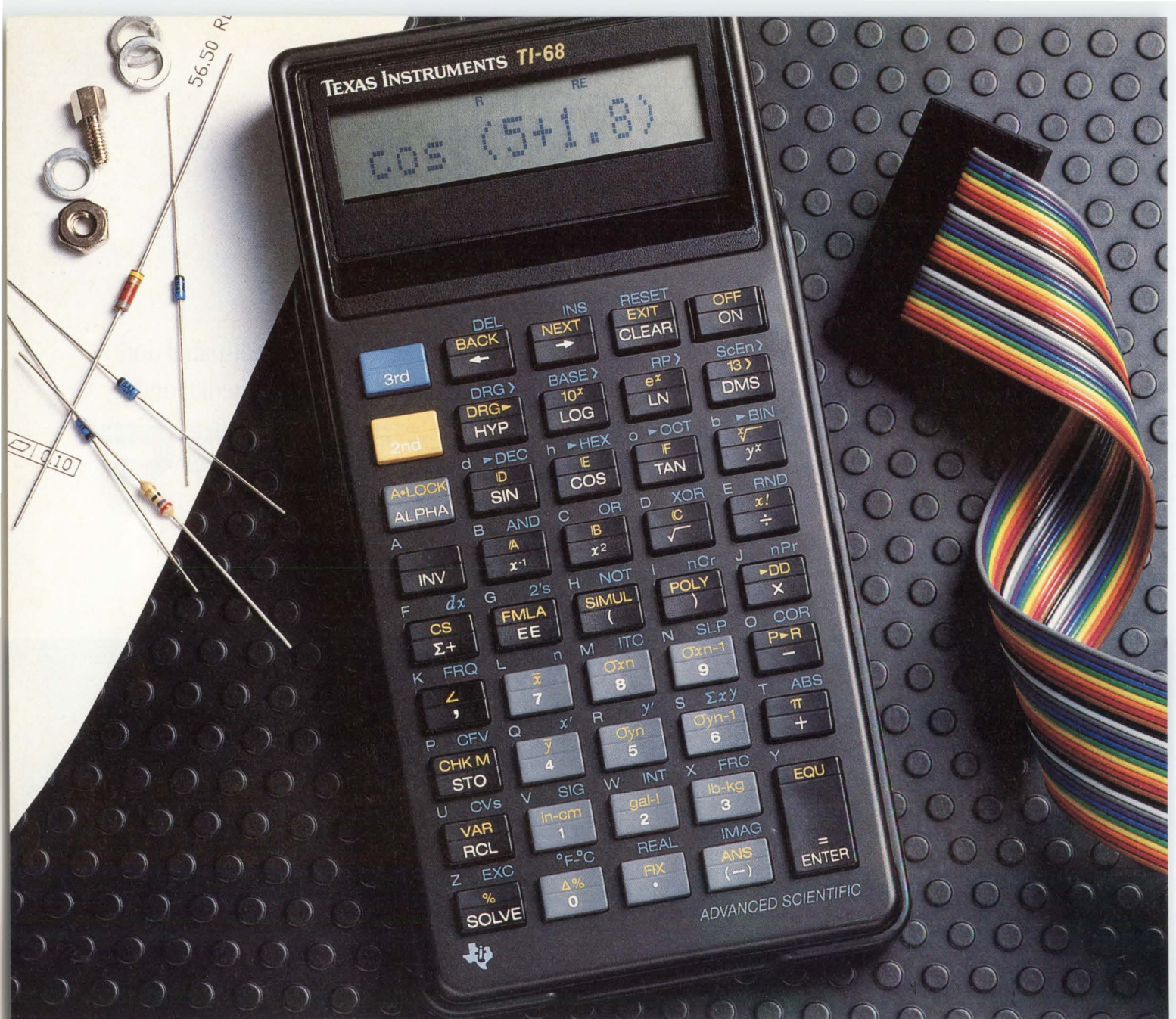


Chips and Technologies, Inc.

CIRCLE NO. 29

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There's a new standard for functionality, ease-of-use and price. The TI-68.

We set some tough goals for ourselves in designing the TI-68. It had to have the powerful functions that technical professionals need. It had to be easy to use. And it had to provide all of this at a substantially lower price than the competition.

We met all of our goals and then some. The TI-68 has 254 useful functions. It solves up to five simultaneous equations with real or complex coefficients. A prompting system guides you through all entries and results. You can handle the complex numbers exactly the way you want, without entering a special mode. The TI-68 evaluates 40 complex number functions and lets you choose polar or

rectangular forms for entries and results.

It also lets you easily check your equations with a 12-character alphanumeric display that can scroll through up to 80 characters for long equations. And, the last equation replay feature lets you edit or check the last computation without having to go back and reenter it.

In addition, when you need to solve quadratic, cubic or quartic equations, the TI-68's polynomial root finder will calculate the real and complex roots — automatically.

Working with number bases and conversions are also no problem. Perform arithmetic functions in decimal, hexadecimal, octal or

binary. And it does Boolean logic operations, too.

The TI-68 provides up to 440 program steps for as many as 12 user-generated formulas. It even stores up to 36 values in memories with user-defined alphanumeric names.

The TI-68 has what you've been looking for — the right functionality at the right price. See and try it at a nearby retailer, or call 1-806-747-1882 for additional information and to request free product literature.

TEXAS 
INSTRUMENTS

Vote for Innovation

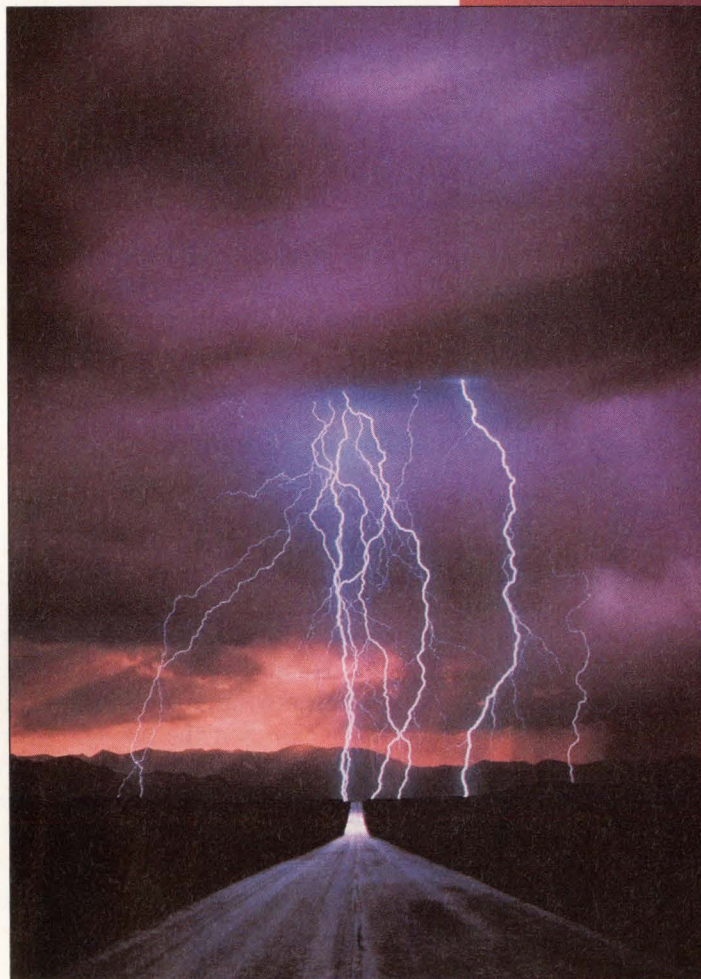


We're very pleased with the lineup of finalists that EDN's editors chose in our Innovations of the Year and Innovator of the Year competition. Now it's up to you to vote. On the following pages you'll find brief descriptions of the products and the people that our editors chose as finalists. Carefully consider these finalists, and make your vote on the postage-paid ballot that appears at the end of this article. You have one vote in each product category and one vote for one of the three innovators. In the software and power-sources categories, our judges found only one product in each category innovative enough to qualify; we present them here with the finalists to give them the recognition they deserve.

After the votes are counted, EDN will announce the winners and honor them at an awards banquet during Wescon/91 in San Francisco, CA, this November. We'll also print a special section in our January issues that will include descriptions of the winning products and people.

We appreciate the enormous amount of time and effort involved in nominating the innovative people and products for these awards. Trying to single out the finalists from your nominations was a formidable task. But from the caliber of people and products you nominated, it's clear that there's no lack of creative and talented people and innovative products in the electronics industry.

If you or your company didn't participate in this year's innovation-awards program, we encourage you to take part next year. It's not too early to start thinking about products and people you could nominate. We will be pleased to mail you 1992 nomination packets as soon as they are ready in early 1992. Just Circle No. 801 on the Information Retrieval Service (bingo) card in this issue, and we'll add you to our award mailing list.



INNOVATORS

Paul Gulick and Arlie Conner

Defying the conventional additive-color approach to creating color displays, Paul Gulick and Arlie Conner labored on a subtractive approach to creating a color LCD projection panel



In Focus Systems Inc
Tualatin, OR
(503) 692-4968

built from three stacked monochrome panels. They exploited the birefringence effect, once perceived as one of the LCD's drawbacks, to create this

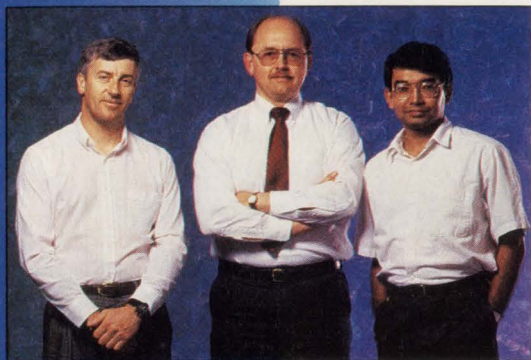
breakthrough technology. The resulting triple supertwisted nematic (TSTN) LCD furnishes color pixels that emit smooth, continuous colors, brighter images, and higher quality images than other color LCD modules.

Conventional color LCD techniques mimic the additive color triads used in CRTs, using additive-color filters over individual pixels, which reduce transmittance. The TSTN Color LCD module avoids the use of additive filters (red, green, and blue), thereby letting more light pass through. Instead of additive-color filters, the TSTN display employs polarizers and LCD panels tuned to three subtractive colors (yellow, cyan, and magenta) which produce the multicolor, single-element pixel and permit the brighter display.

To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

Richard T Simko, Trevor Blyth, and Sakhawat Kahn

Richard Simko, a key player in the development of the digital EEPROM cell, knew that EEPROMs were inherently analog devices, even though they were initially used for digital purposes. He also realized that many tough engineering problems



Information Storage
Devices Inc
San Jose, CA
(408) 428-1400

blocked the use of EEPROM cells for analog storage. In 1987, he finally decided to overcome those problems. Simko hired Trevor Blyth and Sakhawat Kahn to help him tackle the challenge. The work started in Simko's living room. Three years later, the team realized its goals by building a practical device.

The resulting ISD10xx family of analog storage devices can store 12 to 20 sec of audio or other analog signals at an effective rate of 64k bits/sec. The devices incorporate a stable, on-chip,

20V reference generator that permits careful metering of stored charge. Metering overcomes storage nonuniformity caused by trapped charge. Using this feature, the device can reliably record one of 230 discrete voltage levels in each EEPROM cell. The devices overcome the long writing time required by EEPROM cells by accumulating samples and writing to several cells at once. This feature permits the IC to operate in real time. With all of these unique features, the design team was understandably anxious to try out the first devices; so anxious in fact, that they couldn't wait for the die to be packaged. They stored their voices and played them back while the wafer was still in the prober.

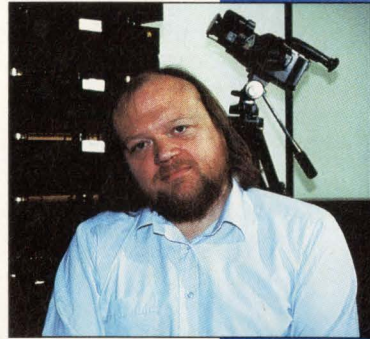
To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

Derek Bowers

Since he became a design engineer in 1982, Derek Bowers has developed more than 37 analog products. The design of the Precision Monolithics AMP-01 precision instrumentation amplifier, one of his first, eliminated the need for trimmed input resistors and became one of the company's most successful products. Over the ensuing years, he has developed a range of analog ICs, including amplifiers, voltage references, analog switches, cable drivers, and A/D and D/A converters.

Subsequent designs include matched transistor pairs, comparators, operational amplifiers, and another instrumentation amplifier. In 1985, Bowers achieved the input-offset, drift, and input bias performance of a single precision op-amp IC in a quad, low-

power op-amp design: the OP-400. He developed a temperature-insensitive CMOS voltage reference in 1987 and collaborated with a process development team to create the company's high-speed bipolar and BiCMOS processes. Analog Devices bought Precision Monolithics in 1990 and gave Bowers the position of Division Fellow in recognition of his achievements.



To vote for this entrant as Innovator of the Year, mark the appropriate box on the ballot.

INNOVATORS

Analog Devices
Norwood, MA
(617) 461-3557

ISD10xx Analog Storage ICs

The ISD10xx family of 28-pin non-volatile CMOS ICs record, store, and reproduce from 12 to 20 seconds of analog information. In addition to speech and music, these ICs can store test waveforms, store correlation data, sample analog signals, and hold filter coefficients. For certain applications, these chips can replace ADC, memory, and DAC functions. Each chip processes and stores analog samples in a 128k-cell EEPROM array and can reconstruct and amplify linear outputs in real time. Two key features are reproduction quality and nonvolatility. For example, the ISD1016 features an S/N ratio of 40 dB and has a 3-dB bandwidth of 3.4 kHz, slightly above telephone-grade specifications. Because the EEPROM array consists of non-volatile memory cells that use a proprietary CMOS EEPROM technology to store charges, the chip requires no backup supply to maintain its analog information. Each device operates from a 5V power supply and requires few external passive components—resistors and capacitors that control filtering and automatic gain control.

The key to the ICs' storage feature

is the physics of nonvolatile floating-gate CMOS EEPROM cells, which are inherently capable of storing "gray scale" voltages that lie between hard-programmed digital states. Each gate acts as a capacitor with an extremely long decay time. These cell features are well known, but these ICs incorporate novel analog transceivers, supporting analog and digital circuits, and high-voltage and -frequency references to control storage and retrieval functions. Typical applications include voice-output products: phone-answering equipment, portable telephones, pagers, emergency equipment, and alarms. The ISD1012, 1016, and 1018 can store 12, 16, and 20 seconds of information, respectively. The devices cost \$15, \$18, and \$20 (1000), respectively.

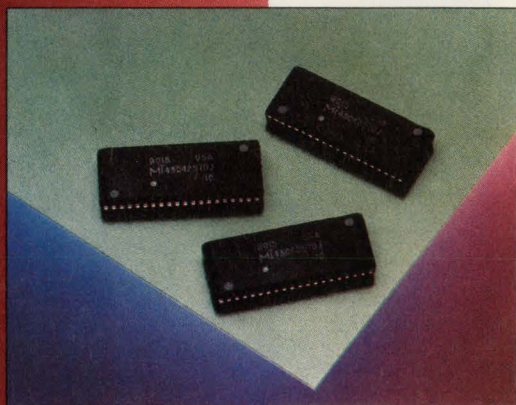
To vote for this entry as the Integrated Circuit and Semiconductor Innovative Product of the Year, mark the appropriate box on the ballot.



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San Jose, CA
(408) 428-1400

INTEGRATED CIRCUITS AND SEMICONDUCTORS



Micron Technology Inc
Boise, ID
(208) 368-3900

Multiport Dynamic RAM

The serial bit-processing needed to refresh CRTs will soon push the limits of Video RAM (VRAM) technology in imaging and graphics applications. The 1M-bit Multiport MT43C4257 dynamic RAM (DRAM) meets this need by increasing I/O bandwidth as well as memory density. The part can eliminate the need to bank VRAMs in many applications.

The device uses an asynchronous triple-port architecture. Sequential data is read or written simultaneously from the

part's 512 × 512 × 4-bit memory array through two static access memory (SAM) ports, while a processor or controller interfaces to the device's bidirectional-DRAM port.

Access times are 80 nsec (random)

and 25 nsec (serial). Special memory functions include masked write, persistent masked write, split read/write transfers, block write, and bit-masked transfers. To support bit-masked transfers, the triple-port DRAM contains an internal 2048-bit-page static bit-mask register (BMR). The BMR lets you isolate any combination of 2048 bits that must transfer between either of the two SAMs and the device's DRAM array.

Active power consumption is 450 mW. Parts in the series include the 256k × 4-bit MT43C4257/8 and the 128k × 8-bit MT43C8128/9. The devices come in a 40-pin, standard-outline J-lead package or a 52-pin plastic leaded chip carrier, respectively. Depending on quantity and speed rating, the ports cost from \$18.50 to \$35.

To vote for this entry as the Integrated Circuit and Semiconductor Innovative Product of the Year, mark the appropriate box on the ballot.

bq2001 Energy Management Unit

The bq2001 Energy Management Unit (EMU) is a peripheral IC that provides battery system management. The device determines a battery's capacity as well as battery-charge consumption. A fast-charge control facility assures that NiCd, NiMH, lead acid, or lithium rechargeable batteries can quickly recharge. You can configure the device to work with 4.8 to 12V (nominal) batteries. A 3-pin serial data inter-



Benchmark
Microelectronics Inc
Carrollton, TX
(214) 407-9845

face provides access to common μ P-bus structures. This interface remains active only when V_{CC} is valid.

The IC executes adaptive battery-

conditioning routines to maintain a higher battery capacity for more cycles than common charge/discharge schemes can provide. An internal regulator provides a backup output for a real-time clock or other low-current ICs. When you remove the main system battery, a lithium cell sustains the EMU and any external circuits the EMU powers. The part can also work directly off a charging supply. This \$10 (1000) CMOS part operates from a 5V-system supply and comes as a 24-pin SOIC or a 300-mil DIP.

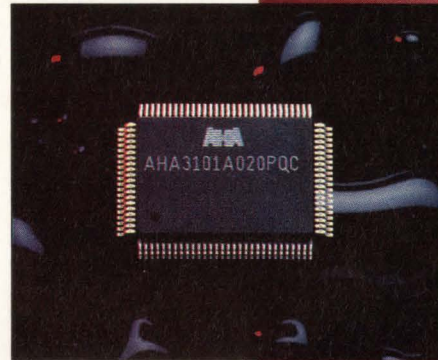
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Data Compression Coprocessor

The AHA3101 is a lossless data-compression IC that uses the Lempel Ziv Data Compression algorithm. The algorithm steps through a file's bytes and creates a dictionary of recurring strings of bytes. When the algorithm finds subsequent occurrences of the strings, it replaces them with their dictionary entry. At each byte, the algorithm compares the input stream to the dictionary entries, and if it finds a match, it outputs a pointer to the dictionary in the form of a code-word. In addition, by constantly monitoring the compression ratio as it proceeds through the file, the algorithm can restart using a new dictionary if the ratio decreases. The dictionary contains as many as 4k 128-byte entries. Because the dictionary is embedded in the coded data, you needn't ex-

plicitly transmit and store the dictionary. The dictionary is rebuilt as the data is decompressed.

The data-compression IC combines hardwired compression and decompression algorithms for high throughput. The chip also features on-chip DMA control, μ P control for the algorithm, and interfaces to static RAM. The circuit costs \$35 (1000).



To vote for this entry as the Integrated Circuit and Semiconductor Innovative Product of the Year, mark the appropriate box on the ballot.

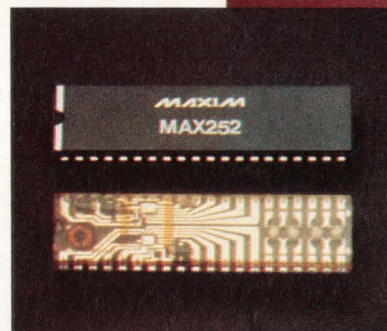
Dual RS-232C Transceiver

By passing RS-232C data, and the power required, across a galvanic isolation barrier, the MAX252 eliminates two vexing problems. These problems relate to the voltage difference that often exists between dissimilar environments and to the possible creation of large ground currents when a common ground connection is made. This hybrid transmitter/receiver provides the necessary isolation using two monolithic ICs, a toroid transformer having a 0.2-in. core diameter, four GaAs photo emitters, four silicon photo detectors, and tantalum and ceramic capacitors. The transmitter/receiver uses a custom lead frame and special insulation and winding techniques to minimize transformer size.

The device converts two TTL inputs on the primary, or equipment, side of the isolation barrier to the currents necessary to drive the self-contained optocouplers. A power oscillator drives a small transformer that delivers ± 10 V to the secondary side of the isolation barrier. Circuitry on the secondary side converts the optocoupler outputs to RS-232C-compatible levels. Re-

ceiver circuitry accepts two RS-232C inputs that are sent (through two additional optocouplers) to the primary side, where these signals are converted to TTL output levels. No external components are needed.

The two versions of the device are UL-approved. The MAX252A withstands 1500V; the MAX252B withstands 600V rms. Both devices can operate at 9600 bps while meeting EIA232D and CCITT V.28 specifications. Other features include an output-enable mode and a shutdown mode, which reduces power consumption to 50 μ W when the RS-232C port is not in use. Each device comes in a 40-pin DIP. Prices start at \$50 and \$29.50 (1000), respectively.



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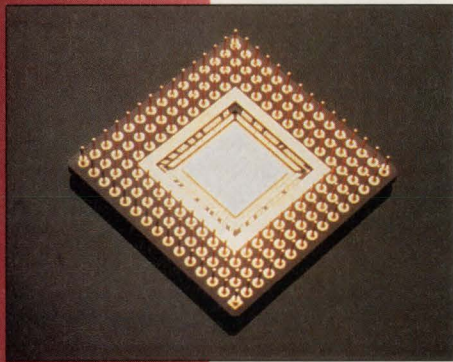
INTEGRATED CIRCUITS AND SEMICONDUCTORS

Advanced Hardware Architectures Inc
Moscow, ID
(208) 883-8000

Hewlett-Packard Company
Integrated Circuits
Business Div
Corvallis, OR
Phone local office

Maxim Integrated Products
Sunnyvale, CA
(408) 737-7600

INTEGRATED CIRCUITS AND SEMICONDUCTORS



C-Cube Microsystems Inc
San Jose, CA
(408) 944-6300

CL550 Image Compression IC

The CL550 image compression processor speeds overall system performance, reduces storage requirements, and minimizes transmission times in systems that manage high-quality full-color images. Thus, the IC makes it possible to implement digital-imaging technology in computers, communications, and consumer applications. The device implements the proposed JPEG (Joint Photographic Experts Group) standard for image compression, shrinking the 25M-byte data files of high-resolution, true-color im-

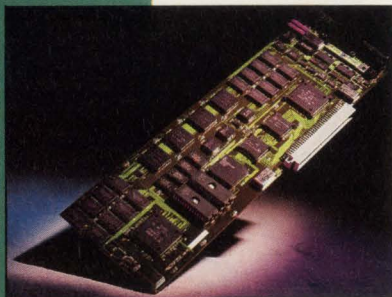
ages down to 1M byte. Because of its extensive pipelining, the IC can perform compression tasks faster than alternative approaches, such as general-purpose DSPs. The device has more than 300 stages of pipeline, letting it perform more than 300 processing steps concurrently. The device can compress/decompress 24-bit

color images in less than one second.

The device's specific compression scheme relates to the JPEG algorithms. Using a combination of discrete-cosine-transform and Huffman-coding methods, the device operates on pixels in 8×8-pixel blocks. On-chip quantizer and Huffman tables store the compression coefficients, which you can access through a host-bus interface. Also, because the JPEG algorithms are symmetrical, the device can compress or decompress images with equal facility. Thus, you can use just one device to both record and play back images. The device can handle grayscale or color images in the RGB (red, green, blue), CMYK (cyan, magenta, yellow, black), or YUV (luminance/chrominance) color-space representations. Two versions of the device are available with operational frequencies of 10 MHz (\$95) and 30 MHz (\$155 (OEM quantities)). Each version comes in a 144-pin pin-grid array; the 30-MHz version consumes a maximum of 2.5W.

To vote for this entry as the Integrated Circuit and Semiconductor Innovative Product of the Year, mark the appropriate box on the ballot.

TEST AND MEASUREMENT



Spectral Innovations
Santa Clara, CA
(408) 727-1314

MacDSP II Signal Processor

The two linked AT&T DSP32C μ Ps and dual 200-kHz, 16-bit ADC/DAC channels on the \$7995 MacDSP II signal-processing card let

you perform high-speed, concurrent signal processing on Apple Macintosh II computers. Each DSP μ P executes programs from its own 1M-byte SRAM (static RAM); the DSP chips communicate through an 8k-byte, dual-ported SRAM. An onboard 68000 μ P with 2M bytes of DRAM (dynamic RAM) coordinates communications between the DSP chips and the host PC. The DSP

chips use DMA to move data between the 68000's memory and the chips' own memory at speeds as fast as 50M bytes/sec.

The onboard 68000 runs Apple's A/ROSE (Apple real-time operating-system executive) to control the DSP chips. An onboard timer drives the executive's scheduler. A/ROSE employs round-robin scheduling with 32 priority levels and achieves a 110- μ sec context switching time with 20 μ sec of latency. The company offers C, Pascal, Fortran, and Basic programming language libraries for the board.

To vote for this entry the as Test and Measurement Innovative Product of the Year, mark the appropriate box on the ballot.

TDS 540 4-Channel DSO

The \$13,900 TDS 540 digital-storage oscilloscope (DSO) has a 10- μ V resolution for lower-frequency signals. The 500-MHz scope enhances resolution by sampling at high rates and creating a short-term average in real time. Only the average goes into waveform memory, so averaging exacts no penalty in memory depth. At maximum sensitivity, you can clearly see 10- μ V signals. However, you'll obtain this resolution only if the scope is capturing no more than 1M samples/sec in its waveform memory. Each of the product's four 8-bit ADCs converts at a maximum speed of 250M samples/sec. Hence, with one channel active, the 4-channel unit can take 1G samples/sec.

The instrument's triggering is much like that of logic analyzers; thus, complex conditions can trigger a sweep. The scope performs waveform math, makes 22 preprogrammed measurements, and produces hard copy on graphics-capable printers. The instrument has no mechanical adjustments. Battery-backed CMOS RAM stores all trim values. A high-resolution DAC

converts the stored calibration values and sends the analog trim voltages to the appropriate nodes.



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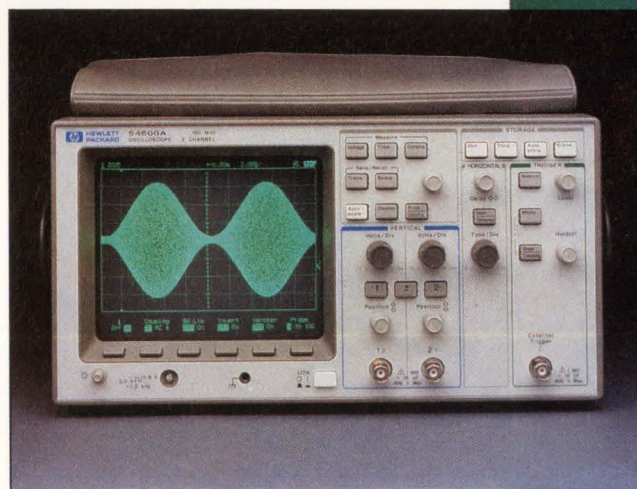
TEST AND MEASUREMENT

Tektronix Inc
Portland, OR
(800) 426-2200

HP54600A 100-MHz DSO

The \$2395 2-channel HP54600A and \$2895 4-channel HP54601A digital-storage oscilloscopes (DSOs) couple analog-style controls—separate knobs for such functions as gain, position, and sweep speed—with real-time performance. No perceptible lag occurs when you observe the output of a circuit under test and manually adjust the parameters of that circuit. With the exception of a few expensive scopes that incorporate high-speed DSP μ Ps, nearly all DSOs exhibit a noticeable lag in display updates.

The scopes have an analog bandwidth of 100 MHz. You can use the entire bandwidth when viewing repetitive waveforms. The scopes have a resolution of 8 bits and a maximum vertical sensitivity of 2 mV/div.



To vote for this entry as the Test and Measurement Innovative Product of the Year, mark the appropriate box on the ballot.

Hewlett-Packard Co
Colorado Springs, CO
(800) 752-0900

TEST AND MEASUREMENT

PM 3580/3585 Logic Analyzers

The PM 3580 and 3585 logic analyzers can perform simultaneous state and timing analysis through a single set of probes. This ability saves you the setup time required to double-



John Fluke Mfg Co Inc
Everett, WA
(206) 347-6100

probe a node. Moreover, not having to put two probes on an IC lead eliminates the capacitance of the second probe set. The instruments' state-

analysis speed is 50 MHz—fast enough for most μ Ps. The products perform assembly-language disassembly for a variety of processors through optional add-on modules and software.

The PM 3585 performs timing analysis at 200 MHz and has 2k bits of memory per channel. The PM 3580's timing-analysis speed is 100 MHz, and it has 1k bit of memory per channel. Both analyzers incorporate transitional timing—they record the time between events instead of taking periodic samples. This feature significantly extends the instruments' memory depth in most applications. You can equip either model with 32, 64, or 96 channels. The 32-channel PM 3580/30 costs \$4250; the top-of-the-line 96-channel PM 3585/90 costs \$10,950.

To vote for this entry as the Test and Measurement Innovative Product of the Year, mark the appropriate box on the ballot.

Asset Scan-Based Test System

Asset (advanced support system for emulation and test) employs the IEEE 1149.1 scan-based test standard by combining a plug-in card and



scan registers. Scan testing gives you the control and observability you need to test a circuit board without resorting to bed-of-nails testers or complex probing with logic-analysis tools.

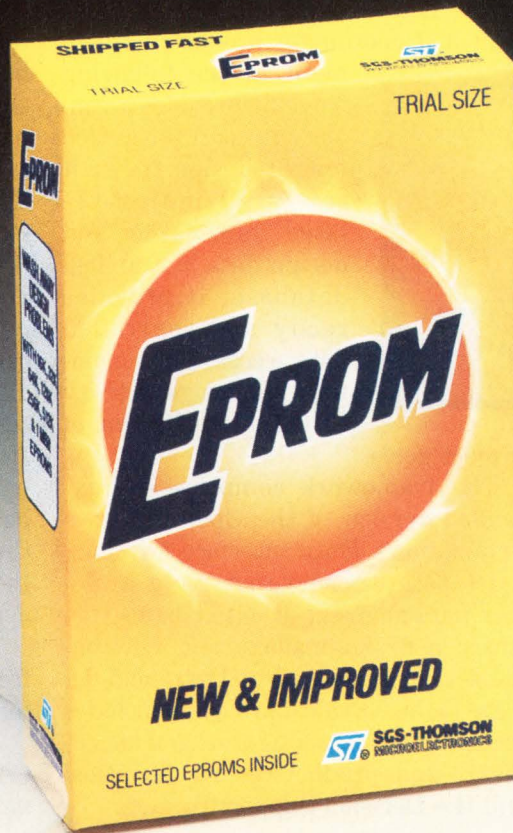
The complete \$25,000 test and development system includes a scan controller on a plug-in card, a C++ compiler, a configuration file library of routines for existing ICs that support IEEE 1149.1, an interactive program debugger, and a model builder that lets you describe your design for the test system. The package also includes two demonstration modules to help you learn about scan testing. You can outfit additional development stations, minus the demonstration modules, for \$22,500; additional test systems without the development software cost \$7500.

To vote for this entry as the Test and Measurement Innovative Product of the Year, mark the appropriate box on the ballot.

software to create a PC-based test system. The software lets you interactively debug or test a hardware design that incorporates ICs using on-chip

Texas Instruments Inc
Dallas, TX
(214) 997-2796

How to wash away memory problems.



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and 2 Meg devices, plus every density in between, right off the shelf. We won't soft-soap you with delivery excuses either. Backed by a list of distributors that reads like Who's Who, SGS-THOMSON ships on time.

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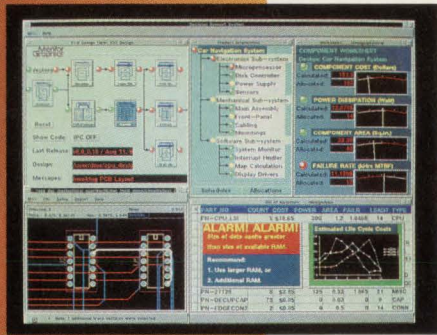
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CAE/CAD



Mentor Graphics Corp
Wilsonville, OR
(503) 685-7000

Falcon Framework For Concurrent Design

The Falcon Framework for Concurrent Design is the foundation of Mentor Graphics Corp's next-generation software suite, System 8.0. Falcon helps engineering organizations plan and coordinate product development in the following ways: it provides a consistent user interface for all design tools; it stores all project-related information and design data in a unified database; it provides ready and controlled data access; and it monitors all design activity to ensure fulfillment of

project goals.

The framework comprises an extended version of the Open Software Foundation's Motif interface for Unix; a database manager that stores all design data in object-oriented data structures; a design-management environment that represents software and designs as hierarchical icons and includes version-control, configuration-management, and product-release facilities; and the Decision Support System.

The Decision Support System enables a design team to simulate a product's behavior based solely on specification parameters entered into its spreadsheet. You enter the equations that describe the desired model, and, based on the parameters, the spreadsheet calculates such factors as cost, power dissipation, and reliability. It can even perform preliminary thermal analyses. The software automatically extracts the data needed for the calculations from the framework's database and from other, linked databases—a purchasing department's list of sanctioned components, for example.

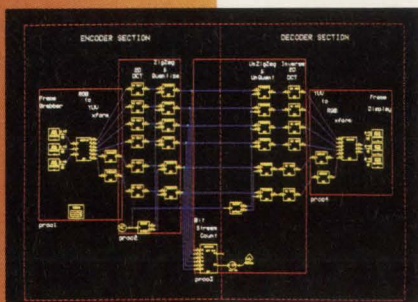
Resulting design models become a sort of living specification: ongoing design information and predetermined parameters are treated as a working body of knowledge. If at any point in the cycle the parameters are violated, the system sends out an alarm to the appropriate project-team members.

The Falcon Framework is shipped free of charge as part of Mentor's System 8.0.

To vote for this entry as the CAE/CAD Innovative Product of the Year, mark the appropriate box on the ballot.

Multiprox Graphical Multiprocessor Platform

An option for the Signal Processing Worksystem (SPW), Multiprox enables you to graphically partition your DSP algorithms to run on multiple processors. To begin your design, you use the SPW to draw a signal-flow diagram, incorporating icons that represent FFTs, filters, modulators, channels, and other functions. After the work-system performs simulation and debugging, you can parti-

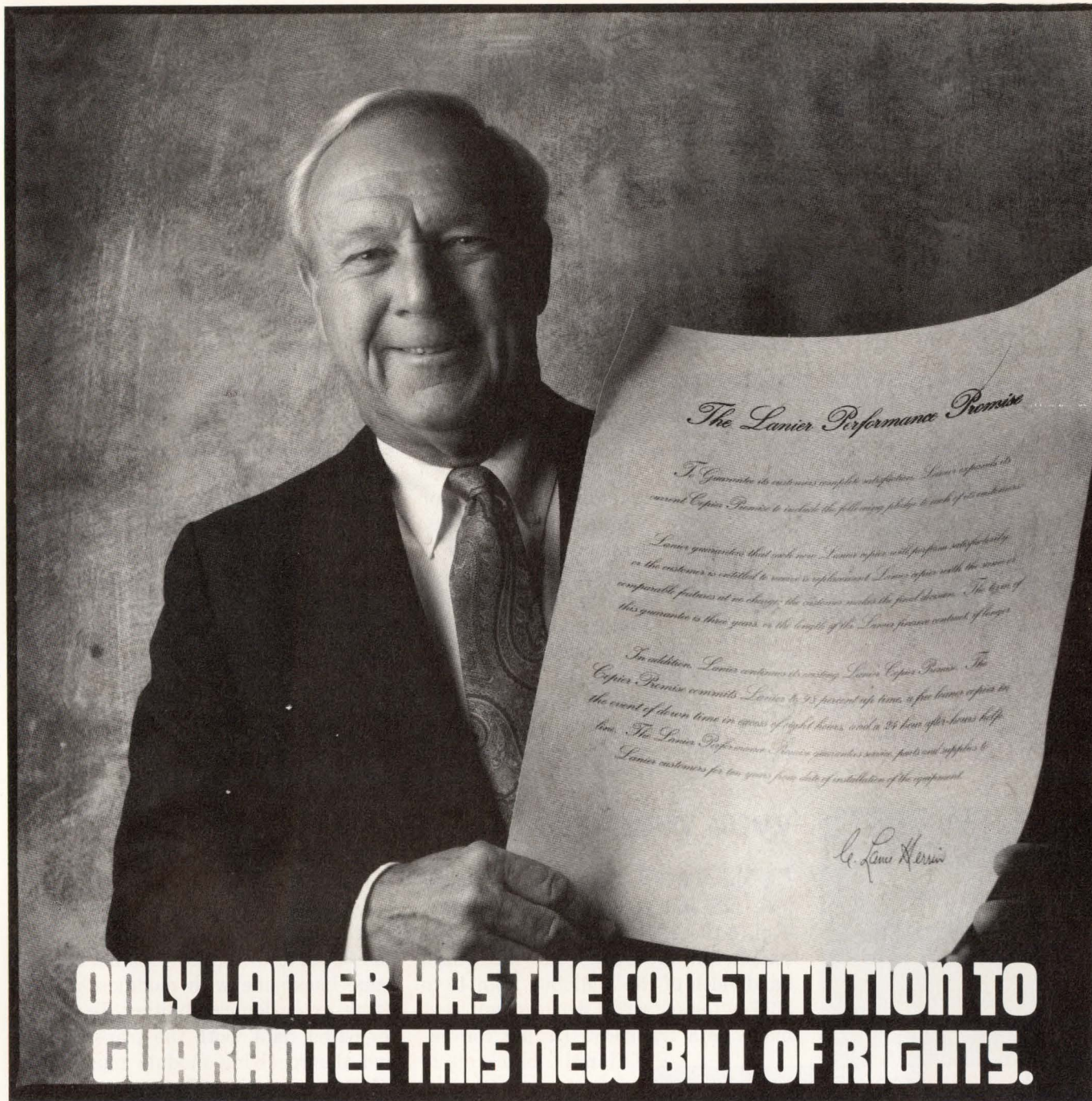


tion the design by drawing rectangles around circuit functions. Another optional software package, the Code Generation System (CGS), converts the

signal-flow block diagrams into executable C code for single-processor execution. Multiprox ensures that your partitions are honored; the CGS converts each partition into standalone code for each processor. The software compiles each code module and inserts all of the code necessary for interprocessor communication before downloading the programs onto your target hardware. To aid in balancing workload, the software also reports on your utilization of each processor; you can redraw the partition to distribute processor resources more equitably. The Multiprox option for the SPW costs \$10,000.

To vote for this entry as the CAE/CAD Innovative Product of the Year, mark the appropriate box on the ballot.

Comdisco Systems Inc
Foster City, CA
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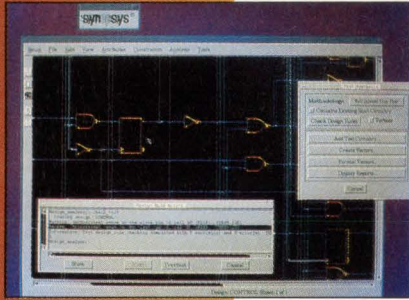
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CMN891

CAE/CAD

Test Compiler

Test Compiler works as a synthesizer to optimize circuit designs' speed, area, and testability. Logic synthesis translates electronic circuit descriptions into multilevel logic representations that you can implement in silicon. Initial design input can take the form of netlists, schematics, equations, state-machine descriptions, truth tables, and VHSIC (very high speed integrated circuit) or Verilog hardware-description-language (HDL) programs. Synthesizers perform both translation and optimization.



Synopsys Inc
Mountain View, CA
(415) 965-8637

The compiler automatically removes redundant logic, inserts test-scan elements, and connects these scan elements in a chain. The compiler supports application-specific integrated-

circuit (ASIC) test methodologies such as level-sensitive scan design and multiplexed scan-path design. Trials show that the compiler reduces area and speed penalties incurred by other compilers that employ typical automatic scan-element insertion techniques. Test Compiler helps you produce test vectors for projects that use the Synopsys Design Compiler and HDL Compiler.

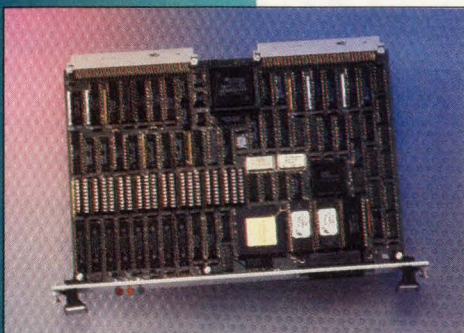
The tool runs under UNIX using an X.11 Window System graphical user interface (GUI). Hardware platforms supported are HP/Apollo, DECstation, Sun/3, and Sun/4. Test Compiler requires a minimum of 16M bytes of physical memory; it is priced from \$25,000.

To vote for this entry as the CAE/CAD Innovative Product of the Year, mark the appropriate box on the ballot.

COMPUTERS AND PERIPHERALS

VME64 VMEbus Extension

The VME64 is a conceptually simple and straightforward extension to the VMEbus specification. The extension increases the maximum bandwidth of the VMEbus from 40 to 80M bytes/sec when performing block-mode data transfers. During conventional block-mode transfers, defined as D32BLT, the VMEbus transmits a 32-bit address and a 32-bit data word during the first transfer cycle. Subsequent cycles only transmit 32-bit data words over the data bus, while the address bus remains



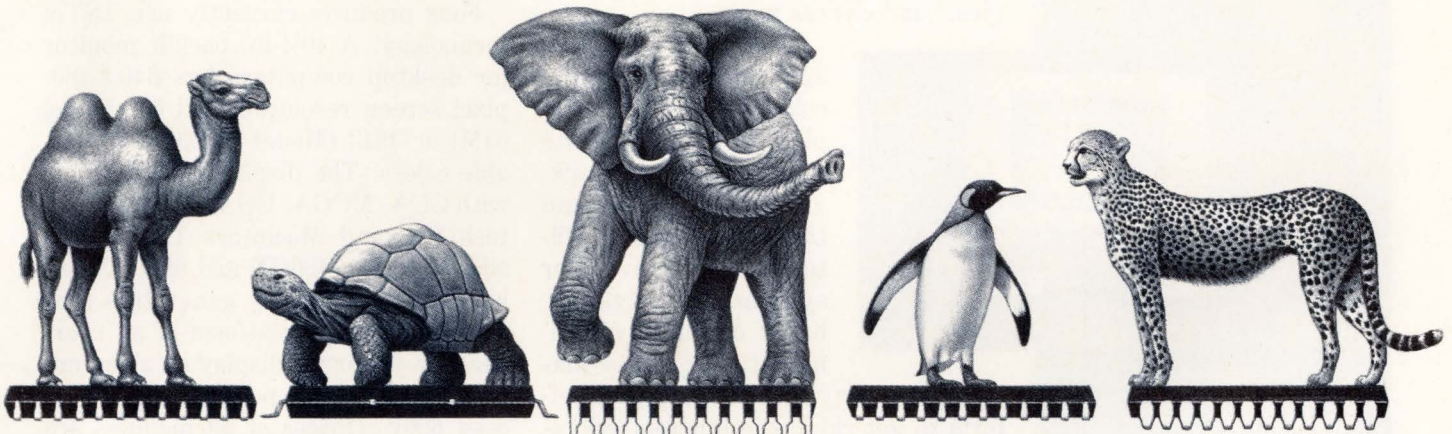
Performance
Technologies Inc
E Rochester, NY
(716) 586-6727

dormant. The extension takes advantage of this situation by multiplexing a second 32-bit data word onto the address bus during its idle time. Therefore, the extension can transfer 64 bits of data after the first cycle in block mode, effectively doubling the VMEbus bandwidth.

The extension is compatible with existing VME modules. Therefore, boards supporting conventional 8-, 16-, and 32-bit transfers can coexist on the same backplane with modules having 64-bit extension capabilities. To transfer 64-bit data, both the transmitting and the receiving module must have VME64 capability. The company estimates that the 64-bit capability of the extension increases the cost of a 32-bit VME module by 25 to 30%. The company has teamed with DY-4 Systems in Ottawa, CA to produce bus-interface silicon that includes a VME64 operating mode. In addition, the extension is now part of the proposed Revision D to VMEbus specification IEEE P1014 currently before IEEE members for certification.

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-- CXX581000M	100/120	SOP 525mil	L/LL	B/X	Now	
-- CXX581100TM	100/120	TSOP (normal)	L/LL	B/X	Now	
-- CXX581100YM	100/120	TSOP (reverse)	L/LL	B/X	Now	
-- CXX581001P	70/85	DIP 600mil	L/LL		Now	
-- CXX581001M	70/85	SOP 525mil	L/LL		Now	
-- CXX581020SP	35/45/55	SDIP 400mil			Now	
-- CXX581020J	35/45/55	SOJ 400mil			Now	
128Kx9 -- CXX77910J	17/20	SOJ 400mil		Sync ASM	3/Q '91	
256Kx4 -- CXX541000J	25/30/35	SOJ 400mil			3/Q '91	

L = Low LL = Low,Low B = 3 Volt X = Extended Temperature

SONY

Sony Corporation of America, Component Products Company, 10833 Valley View St., Cypress, CA 90630

Sony Canada, 411 Gordon Baker Rd., Willowdale, Ontario M2H 256

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COMPUTERS AND PERIPHERALS



In Focus Systems Inc
Tualatin, OR
(503) 692-4968

Color LCD Technology

Triple supertwisted nematic technology (TSTN) yields an economical true-color LCD display. The display uses a subtractive system, bypassing additive-systems' color filters and yielding a brighter screen, fewer "jaggies," and clearer images.

The widely accepted approach to obtaining color from an LCD display is to concentrate first on a good black-and-white image, and then to apply color filters in an additive color system. This system, based on supertwisted-nematic or active-matrix technology, has entailed great efforts to get rid of the inherent coloration of the displayed image. The TSTN technology takes the opposite approach of stacking magenta, cyan, and yellow color cells on top of one another to exploit the inherent coloration of the image in a subtractive color process,

like that used in photography. This process yields higher transmission and better contrast than the additive process and, despite early doubts about its viability, is manufacturable at an economic price.

Four products currently use TSTN technology. A 10½-in. backlit monitor for desktop computers has 640 × 480-pixel screen resolution and 64 (Model 64M) or 4913 (Model 5000M) addressable colors. The display is compatible with CGA, MCGA, EGA, VGA, Macintosh SE, and Macintosh II graphics adapters. The 480CX and 5000CX are heat-resistant display generators that you place on the platform of an overhead projector for display on a screen, provided the lamp power does not exceed 600W. Prices of all modules are \$1500 (OEM qty).

To vote for this entry as the Computer and Peripheral Innovative Product of the Year, mark the appropriate box on the ballot.

EXB-8500 Tape Subsystem

The Exabyte EXB-8500 8-mm cartridge-tape subsystem is a backup device capable of storing 5G bytes of digital data (without compression) on a cartridge at a continuous data-transfer rate of 500k bytes/sec.



Exabyte Corp
Boulder, CO
(303) 447-7359

An integrated 1M-byte speed-matching buffer allows peak transfer rates of 4M bytes/sec and searches at rates as high as 37.5M bytes/sec. The drive uses helical-scan technology to achieve its high data density; the tape is guided around a head-drum assembly that carries two read heads, two write heads, and a servo head. The tape's linear velocity is less than 0.5 ips, whereas the drum rotates at 1831 rpm; this combination produces an effective tape velocity of 150 ips but retains gentle tape handling.

The subsystem records two tracks simultaneously, each 3 in. long, at angles of -10 and +20° from the edge of the tape, resulting in a track density of more than 1600 tracks per inch and an area density of 75M bits/in.². Metal-particle media do not saturate until the density reaches 120 to 150M bits/in.²; thus, the vendor expects to increase total capacity to approximately 67G bytes per tape over the next few years.

The drive includes a read-after-write function that guarantees that data, once written, can be read. The error detection and correction features restrict hard errors to one in 10⁻¹³ bits. The drive uses a standard SCSI controller/formatter that can have either a single-ended or a differential interface. The drive costs \$2400 (1000).

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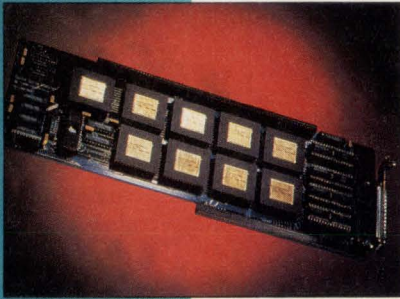
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COMPUTERS AND PERIPHERALS

CHS2 × 4 Custom Computer

The CHS2 × 4 Custom Computer is a 16-bit ISA-bus board that provides an alternative to performing computations on an IBM PC. The custom computer uses a hardware-logic array that you can program to produce configurations of Boolean logic functions.



Algotronix Ltd
Edinburgh, Scotland
(031) 668-1550

The board contains a 2 × 4 array of the company's CAL1024 ICs, as much as 2M bytes of static RAM, and control circuitry that manages the host-data transfer and loads a configuration EPROM on power-up.

Each chip is a "sea-of-gates" field programmable gate array (FPGA) comprising a 32 × 32 array of configurable logic cells. You can program a cell to implement any combinational function of two Boolean variables. The board lets you interconnect cells via dedicated data paths, or you can map algorithms directly into the hardware. The 2 × 4 array of chips provides 8192

cells, which is expandable to a 4 × 4 array of 16,384 cells. You can program the board to implement custom computing structures, such as systolic arrays and computational cells for finite element analysis. Because the board's array is programmable, you can dynamically configure the structure. In addition, you can quickly program the board to emulate an ASIC design to solve wire demand problems.

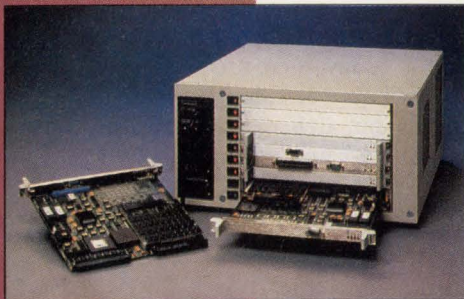
A suite of software tools lets you input a design via an OrCAD (Hillsboro, OR) schematic package, a symbolic editor, or logic equations. An assembler generates binary data for the board, which is controlled by an application program running on the host. All programs are written in C, so a library of C routines can be called by an applications program. Depending on configuration, the board and software costs from \$5,000 to \$10,000.

To vote for this entry as the Computer and Peripheral Innovative Product of the Year, mark the appropriate box on the ballot.

COMPONENTS, HARDWARE, AND INTERCONNECTS

Live Insertion Backplane

The Multibus Manufacturers Group Technical Committee has developed a product specification for a live-insertion backplane for Multibus II Open Bus Systems. The specification implements an intelligent slot controller that permits removing and inserting boards while the system is operating.



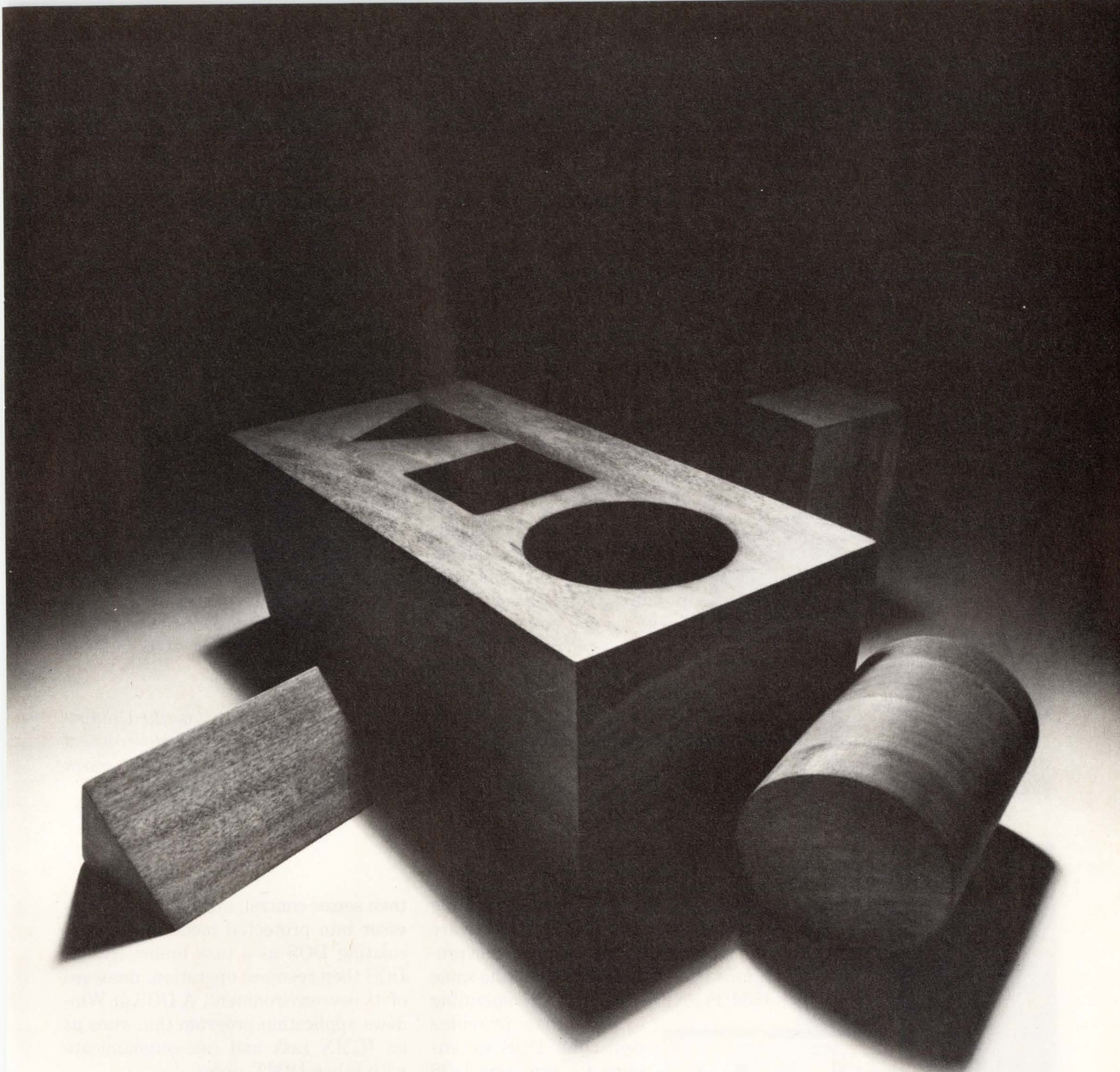
Multibus
Manufacturers Group
MMG Technical Committee
Aloha, OR
(503) 696-7155

When you insert a board into an active system, an isolated ground pin on the backplane (pin A1) becomes grounded, sending a detection signal to the controller. The controller recognizes an insertion or removal within a few msec and begins arbitration by asserting the bus request signal (BREQ).

After asserting the BREQ line, the controller monitors the system-control lines. It waits for at least two cycles to pass with no bus traffic before releasing the BREQ line. The controller supplies power to the new board using a power FET as a voltage controller. The controller also assigns a valid card slot and arbitration identification number via independent reset (RST) and reset-not-completed (RSTNC) lines for each slot on the backplane.

The open-bus technology is available to anyone, and there are no patents pending. The design is 100% compatible with existing Multibus II boards and typically costs \$2000 to implement.

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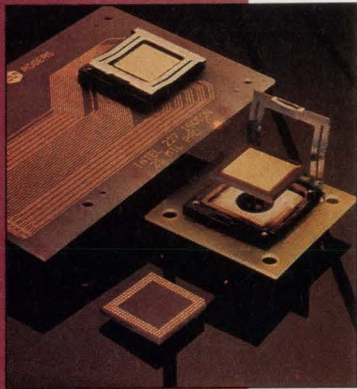
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COMPONENTS, HARDWARE, AND INTERCONNECTS



Rogers Corp
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Tempe, AZ
(602) 967-0624

Interconnection System

The Isocon connector is a pressure-mated device that interconnects arrays of contact pads. The unit consists of flat, S-shaped beryllium copper conductors (nickel- and gold-plated) suspended in a high-stress-retention microcellular silicone. Applying downward force causes the conductors to rotate, providing a wiping action at each contact point. The microcellular silicone maintains the contact force and provides a gas-tight seal.

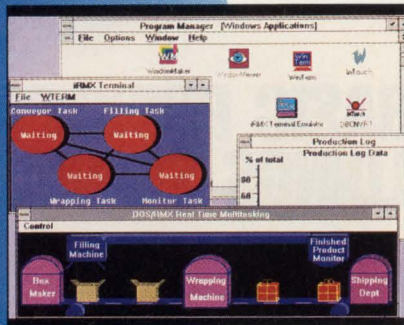
Isocon connectors provide a solderless demateable interconnect for electronic components, such as IC chip packages and pc boards. The connector can provide contact configurations and spacings down to 50-mil pitch in grid—as many as 400 contacts per in.² of board surface. The connector can accommodate large variations in compression levels, so its performance is not adversely affected by

diverse package and board tolerances. Because it has a lifetime in excess of 10,000 mate/unmate cycles, this connector is compatible with test and burn-in applications.

Isocon connectors consist of the conductor-populated silicone material permanently attached to a socket that aligns the IC of a multichip module package with the pc-board contact pads. The socket also controls compression in the silicone material. In most cases, the system is custom designed for each application. However, there is very little tooling cost associated with the Isocon array. Hardware costs depend on customer requirements and final contact-array complexity. Including socket hardware, the product is priced at \$0.05 to \$0.15 per contact.

To vote for this entry as the Component, Hardware, and Interconnect Innovative Product of the Year, mark the appropriate box on the ballot.

SOFTWARE



Intel Corp
Hillsboro, OR
(503) 696-2441

IRMX For Windows


The IRMX for Windows operating system lets real-time software and DOS and Windows application programs run simultaneously on the same IBM PC/AT processor. The operating system also provides real-time DOS extensions for real-time DOS or Windows program development.

Standard, unaltered DOS runs as a task under the operating system; Windows 3.0, also unaltered, runs as a DOS application. The operating system's real-time control comes from the multitasking kernel of IRMX, a real-time operating system that was previously limited to Multibus boards and systems.

Initially, DOS loads IRMX as an application program. This "application"

then seizes control, switching the processor into protected mode and encapsulating DOS as a task under IRMX. DOS then resumes operation, unaware of its new environment. A DOS or Windows application program thus runs as an IRMX task and can communicate with other IRMX tasks.

The combined DOS and IRMX operating system has multiple layers. The nucleus is a 32-bit, real-time kernel that has 255 task-priority levels, preemptive scheduling, prioritized interrupt management, timer management, semaphores, mailboxes, and other means of intertask synchronization and communication. Other layers include an I/O system layer and a human-interface layer. The operating system, with libraries and documentation, costs \$1995. Run-time disks are \$150 each.



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Genesis High-Power-Density Battery

POWER SOURCES



Gates Energy Products Inc
Gainesville, FL
(904) 462-4110

In designing the Genesis battery, Gates Energy Products has accomplished an objective that has eluded lead-acid-battery designers for decades: reducing by approximately 40% the size and weight of a battery that delivers high power (720W) for approximately 15 min. Indeed, when called upon to deliver 1800W, the battery operates for 5 min vs as little as 30 sec for more conventional batteries of the same size.

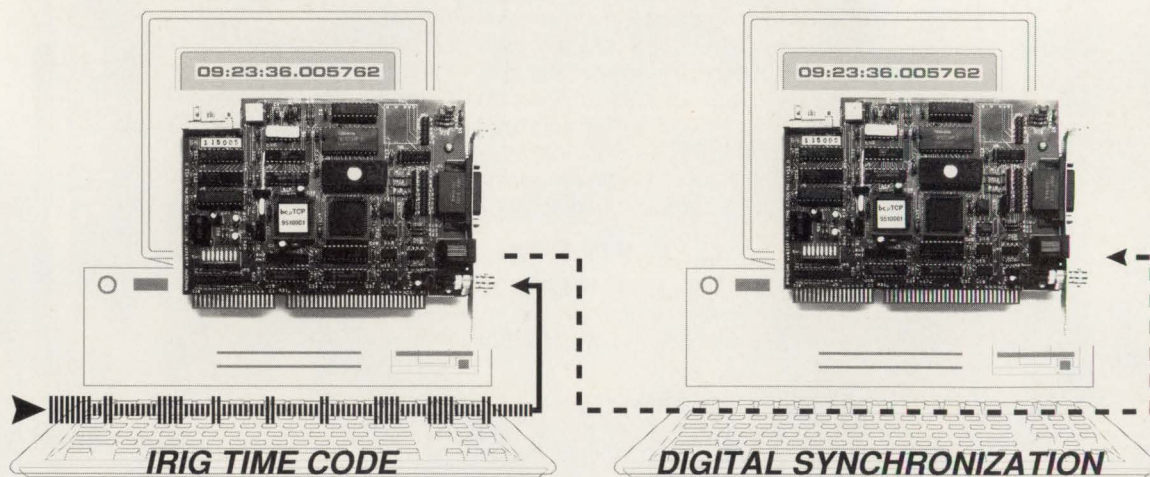
Certain immutable rules constrain the design of lead-acid batteries. Obtaining higher current requires increasing the area of the battery plates. But increasing the plate area while holding the battery's size constant requires making the plates thinner. Previous attempts to make thinner plates resulted in re-

duced physical strength and shortened battery life. But the manufacturer's improvements in processes and materials have overcome those problems.

Having created a battery specifically for low- and medium-power uninterrupted power supplies, the manufacturer has tailored the battery's characteristics to that application—a feat not possible in a battery intended for a range of uses. For example, the hardened terminals eliminate the need to periodically tighten cable clamps. The batteries are sealed and require no maintenance; under normal operating conditions, their electrolyte system eliminates venting of hydrogen into the atmosphere. Their flame-retardant cases conform to UL standard 94V-0 and have built-in carrying handles. The batteries cost \$94.50.

SYNCHRONIZE PC COMPUTERS

bc 630AT Real Time Clock modules install in your PC computer replacing the conventional PC Real Time Clock. The bc 630AT can be synchronized to an external IRIG time code source and/or multiple PC's can be synchronized together using digital synchronization signals.



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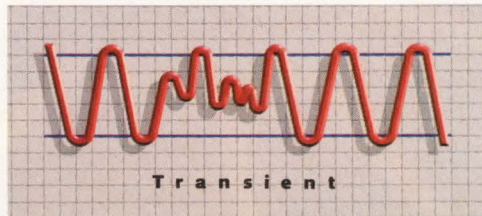
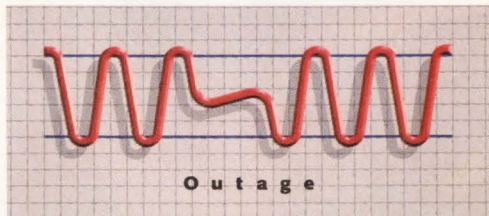
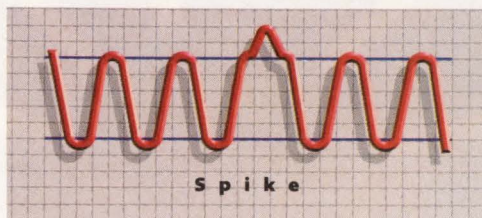
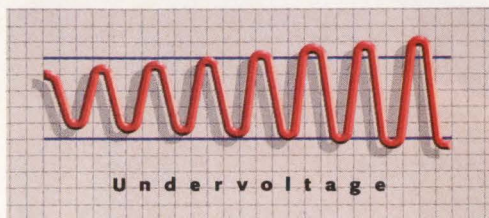
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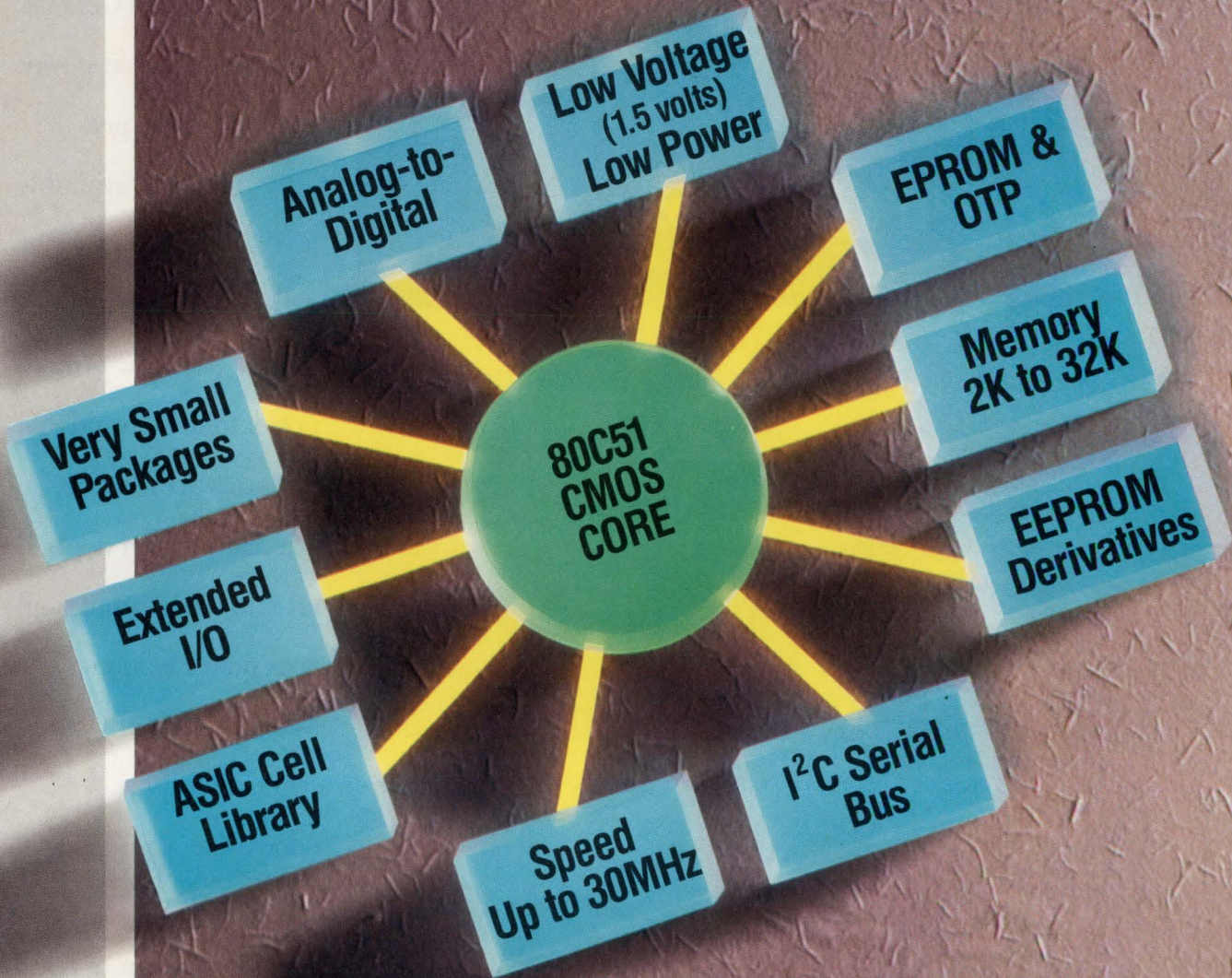
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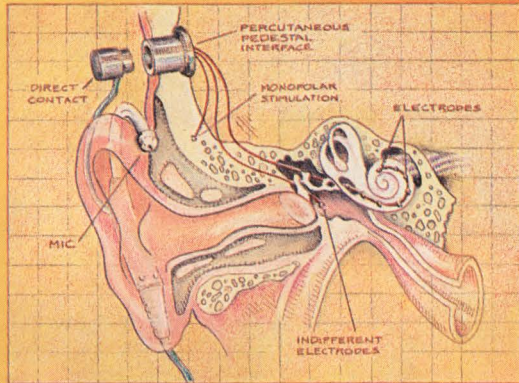


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TECHNOLOGY UPDATE

COMBINED LOGIC ANALYZERS AND DSOs

Combined instruments find logic problems

When logic errors in your circuit turn out to be signal integrity problems, you need to team up a logic analyzer with an oscilloscope. A single instrument that combines the two is often more efficient than separate units.

*Doug Conner,
Regional Editor*

Many engineers have had their oscilloscope working side by side with their logic analyzer for years. However, just because instruments are used together isn't good justification for combining them. The best reason for combining a logic analyzer with an oscilloscope is because a single instrument does a better job and does it easier. Combined instruments are effective because as digital designs continue to increase in clock rate, signal integrity becomes more of a problem. Logic that is correct at low speeds runs into trouble when short timing margins will no longer cover up jitter, ringing, and other signal integrity problems. It's not good enough to connect digital circuits correctly, you have to ensure signals are stable when the system timing requires them to be valid. To find signal integrity problems, a logic analyzer isn't sufficient—you need to add an oscilloscope.

With combined logic analyzers and DSOs (digital storage oscilloscopes), you can save bench space and operate both instruments through one keyboard and display. (Although when using separate instruments you can choose any type of oscilloscope, manufacturers of combined instruments use DSOs for their single-shot capture.) More important, you can view the results of both instruments on one display. Not only will the single display save you from having to look continually back

and forth between two instruments with different displays and, undoubtedly, different time scales, but the combined instrument can correlate the data times so that data is easier to interpret.

When you are tracking down the cause of a problem that shows up in the logic, a logic analyzer has the sophisticated triggering features to help you catch the problem and the digital events leading up to the problem. Logic analyzers provide trigger qualifiers for address, data, time, count, and other ways to help you trigger on the correct event.

Connecting the two separate instruments adds a delay that the instruments

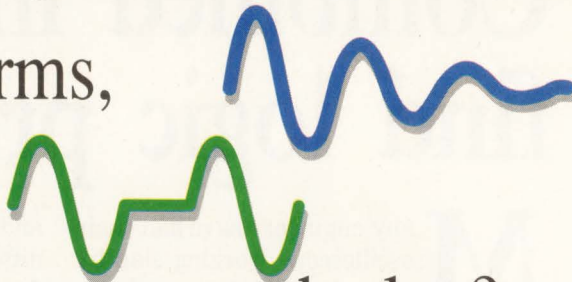


Color displays, available on many combined logic analyzers and DSOs for benchtop use, help communicate information quickly and clearly. Color displays aren't usually available on portables. The Tektronix Prism 3002 is available in several versions, including a portable.

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Combined logic analyzers and DSOs

won't compensate for. If you are triggering an oscilloscope off a logic analyzer, there will be some delay associated with the trigger out from the logic analyzer and the cable between the logic analyzer and the scope. The total delay should be relatively small, but will probably require you to devote one of your scope channels to a known signal in order to time-correlate the oscilloscope display with that of the logic analyzer.

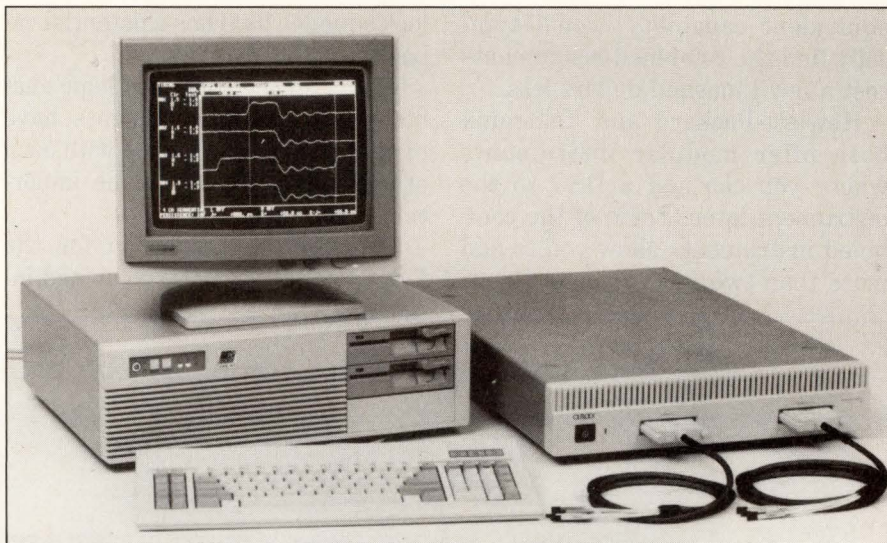
See the data time-correlated

Combined instruments offer a time-correlated display between the logic display and the DSO display. The most common method for providing a time-correlated display is to use a time-aligned display where logic-analyzer and DSO waveforms all appear on the same time scale.

Time stamping is another method instruments use for time correlating events. The instrument attaches a reference time with each event captured by the logic analyzer. Time stamping lets you compare a state listing on a logic analyzer with the DSO or logic-analyzer timing display. Stepping through the state display causes timing cursors to show the time position on the logic-analyzer timing and DSO displays. The combined instruments make it easy to view the time correlations accurately for evaluating cause-and-effect relationships.

Instruments that combine a logic analyzer and a DSO aren't just useful for examining logic signals. The DSO means that you can examine analog signals for problems too. You can look for analog signals causing digital problems and vice versa. If the wrong analog signal is going into an A/D converter, you can't hope to get the correct digital signals out.

Whether you use a combined in-



Sixteen channels of logic or analog signals can be displayed on a PC using the Outlook's 1620 system. You can expand this unit to 32 channels. You can expand the 1600 standalone version to 160 channels.

strument or a separate logic analyzer and oscilloscope, the oscilloscope should let you capture single-shot events. The reason you need an oscilloscope with single-shot capture is that a logic analyzer is a single-shot instrument. When a logic analyzer observes the trigger conditions, it records the data occurring before the trigger, after the trigger, or both. An oscilloscope should complement the single-shot capability of the logic analyzer. DSOs are the only types of oscilloscopes that offer single-shot capture and effectively record data of more than a few nanoseconds before the trigger.

The single-shot capability is important when you are tracking down an intermittent problem. With the single-shot capability, you only need one trigger event to capture all the data for both the logic analyzer and the DSO. Waiting for multiple triggers on a problem that only happens once an hour wastes time. Capturing the data with a single-shot DSO also avoids potential problems, such as jitter from your trigger source.

Using a single-shot DSO also

means you won't continually have to modify the code running on the system you're testing just so you can get a signal bright enough to view on an analog oscilloscope. Capturing the event directly saves time and avoids adding to the problem new variables which are caused by modifying code on the system you're testing.

Combined logic analyzers, such as HP's 16500 system, have DSO channels with sample rates of 1000M samples/sec for capturing single-shot signals having bandwidths as high as 250 MHz.

DSOs on some of the combination instruments offer bandwidths of 350 MHz, which are useful on repetitive signals. Accumulating data for a waveform over the course of a minute on a repetitive DSO using an infinite persistence display is a viable solution when trigger conditions are frequent.

Combined logic analyzers and DSOs have another attractive feature: They often cost less than the equivalent separate instruments. If you compare the cost of purchasing a DSO and a logic analyzer with

TECHNOLOGY UPDATE

Combined logic analyzers and DSOs

equivalent capability, you'll typically find the combined instruments cost a few thousand dollars less.

Hewlett-Packard and Tektronix both offer modular instruments where you can add a DSO to the instrument later. Some of the combined instruments allow you to add more than two DSO channels. Out-

look's model 1600 has a potential capacity of 160 channels.

Although the combined logic analyzer and DSO instruments have many features in common with each other, there are also some important differences.

The voltage resolution for the DSO portions of these combined in-

struments ranges from 8 bits to 4 bits (Outlook's 1600 series in single-shot mode). Although it is fairly coarse, contrasted with what a logic analyzer can offer, 4-bit—16 discrete voltage levels—resolution is a major improvement. The 1600 series is different from the other combined instruments in **Table 1** be-

Table 1—Representative combined logic analyzers and DSOs

Manufacturer	Model	Logic Analyzer			DSO				Price	Comments
		Synchronous (channels at clock (MHz))	Asynchronous (channels at clock (MHz))	Memory (words)	Bandwidth (MHz)	Maximum single-shot sample-rate (channels at M samples/sec)	Resolution (bits)	Memory (words)		
Hewlett-Packard	1652B	80 at 35	80 at 100	1k	100	2 at 400	6	2k	\$11,300	
	1653B	32 at 25	32 at 100	1k	100	2 at 400	6	2k	\$7400	
	16500 Series:	N/A	N/A	N/A	N/A	N/A	N/A	N/A	\$7700	5-slot mainframe, no modules.
	16510B	80 at 35	80 at 100	1k	N/A	N/A	N/A	N/A	\$6000	
	16515A	N/A	16 at 1000	8k	N/A	N/A	N/A	N/A	\$8300	
	16530A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	\$1600	Timebase supports four 16531As or 16532As.
	16531A	N/A	N/A	N/A	100	2 at 400	6	2k	\$4400	Requires 16530A.
	16532A	N/A	N/A	N/A	250	2 at 1000	8	8k	\$9000	Requires 16530A.
Orion	Omnilab 9350	96 at 34	96 at 34, 32 at 102, 16 at 204	16k (64k optional)	100	2 at 204	8	16k (384k optional)	\$14,550	Requires PC for control and display.
	Omnilab II	96 at 34	96 at 34, 32 at 102, 16 at 204	16k (64k optional)	100	2 at 204	8	16k (384k optional)	\$21,340	Standalone unit.
Outlook	1600	N/A	16 at 200	4k	350	16 at 100 (4 at 400, 2 at 800)	4, 6	1k	\$21,700	Expands to 160 channels with 1610s.
	1610	N/A	16 at 200	4k	350	16 at 100 (4 at 400, 2 at 800)	4, 6	1k	\$15,450	Expansion module (up to nine with 1600).
	1620	N/A	16 at 200	4k	350	16 at 100 (4 at 400, 2 at 800)	4, 6	1k	\$16,450	Requires PC for control and display.
Tektronix	1230	16 at 25	16 at 25, 8 at 50, 4 at 100	2k	N/A	N/A	N/A	N/A	\$2995	Logic analyzer with three expansion slots.
	1230EI	16 at 25	16 at 25, 8 at 50, 4 at 100	2k	N/A	N/A	N/A	N/A	\$1200	Logic analyzer expansion module.
	1230DSM	N/A	N/A	N/A	100	2 at 100	8	2k	\$2995	Digital scope module.
	Prism 3002CD	96 at 16 and 9 at 90	9 at 200	8k, 2k	350	2 at 200, 1 at 400	8	16k, 32k	\$14,950	Mainframe with 30MPX and 30DSM.
	30MPX	96 at 16 and 9 at 90	9 at 200	8k, 2k	N/A	N/A	N/A	N/A	\$6000	
	30HSM	N/A	20 at 400 to 4 at 2000	24k to 120k	N/A	N/A	N/A	N/A	\$6000	Dual threshold, 20 channels at 200 MHz.
	30DSM	N/A	N/A	N/A	350	2 at 200, 1 at 400	8	16k, 32k	\$6000	

Note: N/A = Not applicable.

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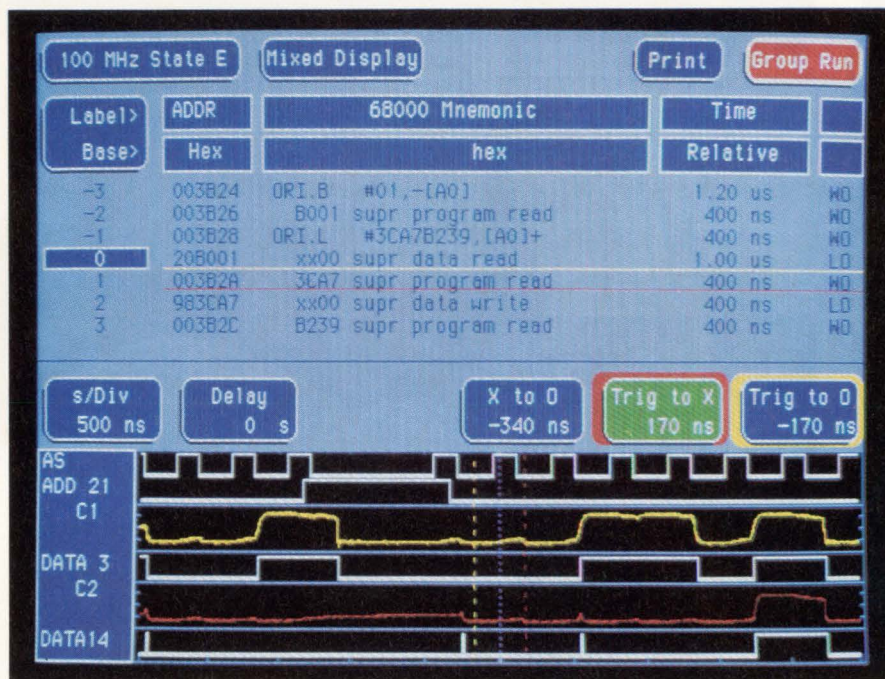
cause it provides either a DSO or logic-timing display of every channel. You get one or the other, but not both simultaneously.

When you look for high-speed, single-shot, digitizing rates, you need to be careful. On some systems, resource sharing causes channel reductions that may be significant.

For example, Orion's Omnilab products have two digitizing channels that each subtract eight logic-analyzer channels from the total of 96 when you are using them. The DSO channels nominally operate at 34M samples/sec. For higher single-shot sampling rates, you can select a 3x or 6x interleave. Using the 6x interleave gives you a sampling rate of 204M samples/sec and consumes 48 logic-analyzer channels per DSO channel—that's all 96 channels in the system if you are using both DSO channels. An advantage of interleaving is that the memory behind each channel is multiplied by the interleave factor, making it possible to obtain 384k data points in a DSO record with the maximum optional memory. By using repetitive sampling, you can operate the two DSO channels at their 100-MHz bandwidth and still have 80 logic-analyzer channels.

Another example of interleaving is the nominal 100M-samples/sec operating speed for Outlook's 1600 series products. By adding an optional probe to interleave eight channels into one, you can obtain an 800M-sample/sec digitizing rate for single-shot events.

On modular instruments you have a limited number of module slots, which may also cause limitations. For example, Tek's 1230 logic analyzer has a total capacity of four 16-channel logic-analyzer modules. You can trade out one logic-analyzer module for a DSO module,



Time-correlated displays of state, logic, and analog signals from an HP16500 combined instrument help you keep track of what's happening. You can control the instrument using a keyboard, a mouse, or the touch-sensitive screen.

which reduces the maximum channel count to 48.

Some modular instruments, such as HP's 16500, Outlook's 1600, and Tek's Prism, offer expansion units for additional modules when you run out of slots.

One drawback to combined instruments, when compared with standalone oscilloscopes for scope-only use, is that they lack dedicated scope controls. You always have to go through menus to setup scope operations. When using a combined instrument, the limitation is relatively insignificant. You'll probably spend far more time setting controls for the logic analyzer portion of the instrument than for the DSO. If you expect to be using the DSO portion of the instrument often by itself, you may find using the menu structure less efficient than using a separate oscilloscope with dedicated knobs and switches.

When evaluating the logic ana-

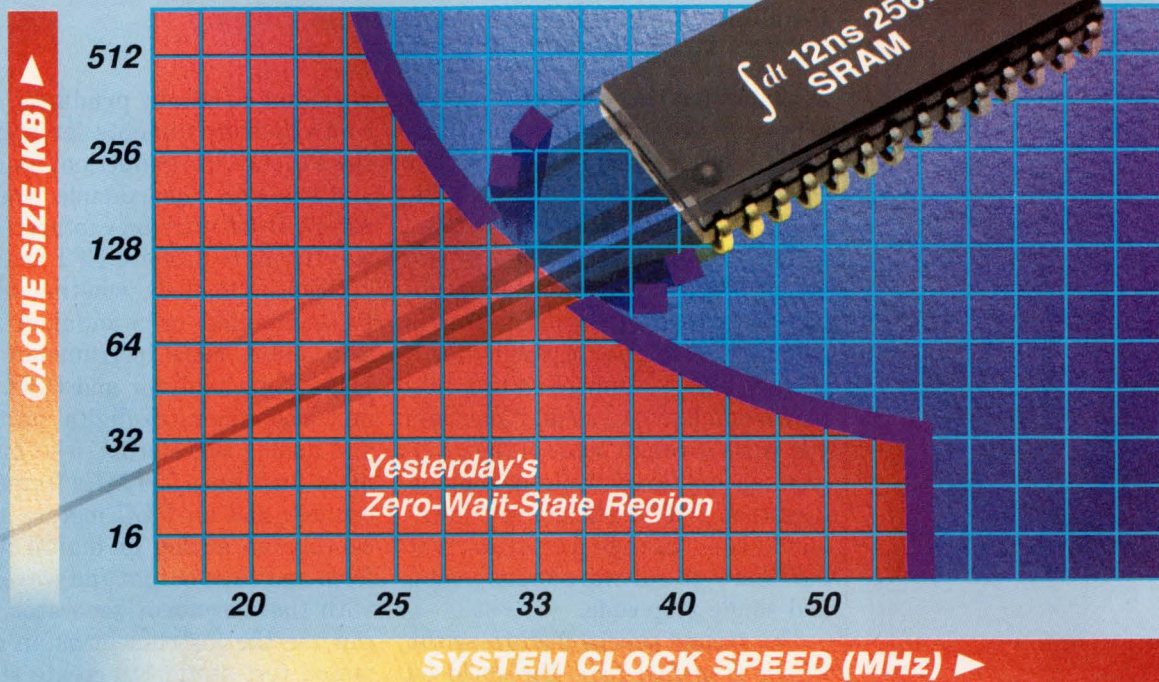
lyzer portion of a combined instrument you'll find interleaving or multiplexing again becomes an issue.

Interleaving is common on many logic analyzers to trade channel width for faster clock speeds. The products from Tektronix and Orion both use interleaving or multiplexing on their logic analyzers to boost clock rates. HP is conspicuous by its lack of interleaving of any kind in its combined instruments.

If you're using a μ P to develop a product, logic-analyzer support for the μ P can save time by making the hardware connections and decoding instructions, rather than having to look at the state listings of machine code.

Outlook's 1600 series doesn't offer state displays; the instruments are strictly timing analyzers. Instruments from the other manufacturers, however, offer support for μ Ps. You'll want to consult the manufacturer to see if support is

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available for the particular processors you are using—or anticipate using. You can also find support for specific buses, such as VME, VXI, SCSI, and IEEE-488.

Tek's Prism instrument has two useful features not commonly available on logic analyzers. The first is a limited emulation capability. Although it's no comparison to a full-blown emulation system, it can help you work through many of the problems encountered while debugging a system. The Prism lets you download code, change registers, set hardware or software breakpoints, and single step code.

The second special feature on the Prism is a dual logic threshold on the 30HSM modules. The dual threshold captures and displays when signals are between logic states. This feature is useful for identifying problems such as slow rise time, slow fall time, and bus contention. The 30HSM module also lets you digitize two channels at 400M samples/sec with 11 levels (3.5 bits) of resolution.

Additional features found on some of the combined instruments make them useful for special applications. Orion and Outlook both offer standalone and PC-controlled

versions of their products. PC-controlled instruments let you use the PC for data reduction, storage, and analysis. For example, you can use DSP software on captured DSO waveforms to perform FFT analysis.

Orion's Omnilab, whether in the PC-controlled or standalone version, offers more instruments than just a logic analyzer and DSO. The unit also generates digital patterns and analog waveforms. The instrument features a 550-MHz frequency counter and an RLC meter; it can capture an analog or digital waveform and then output the waveform with the waveform generator. You can use the instrument as an automated test station to create stimulus and measure response. You can program the instruments to perform tests with loops, conditional branches, and operator prompts.

HP's 16500 system also has an optional pattern-generation module that lets you capture digital signals and then create and output digital signals that duplicate the captured pattern.

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For more information on the combined logic analyzer and DSOs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

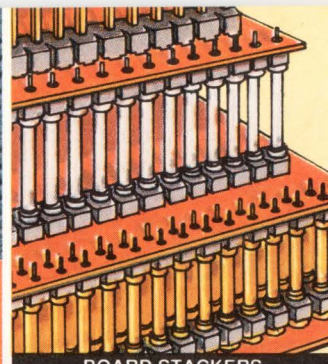
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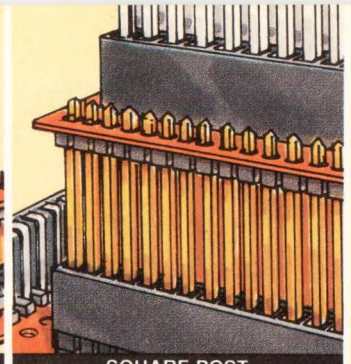
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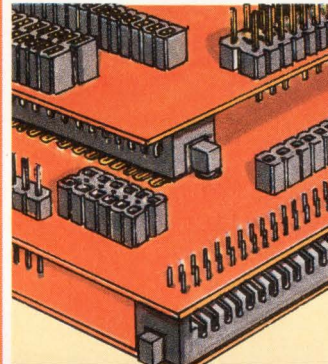
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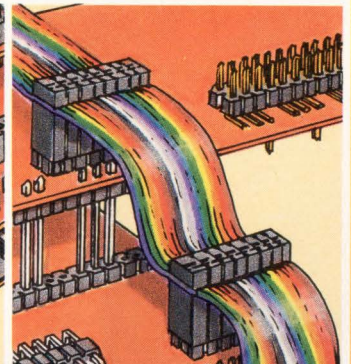
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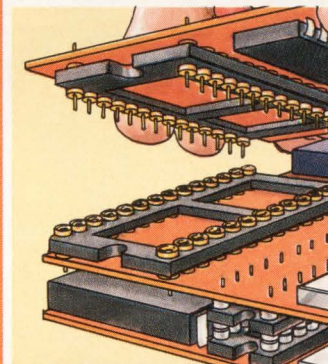
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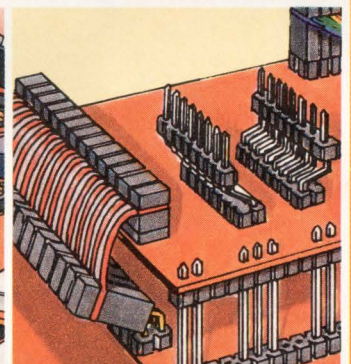
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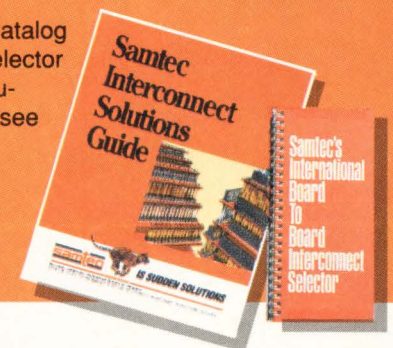
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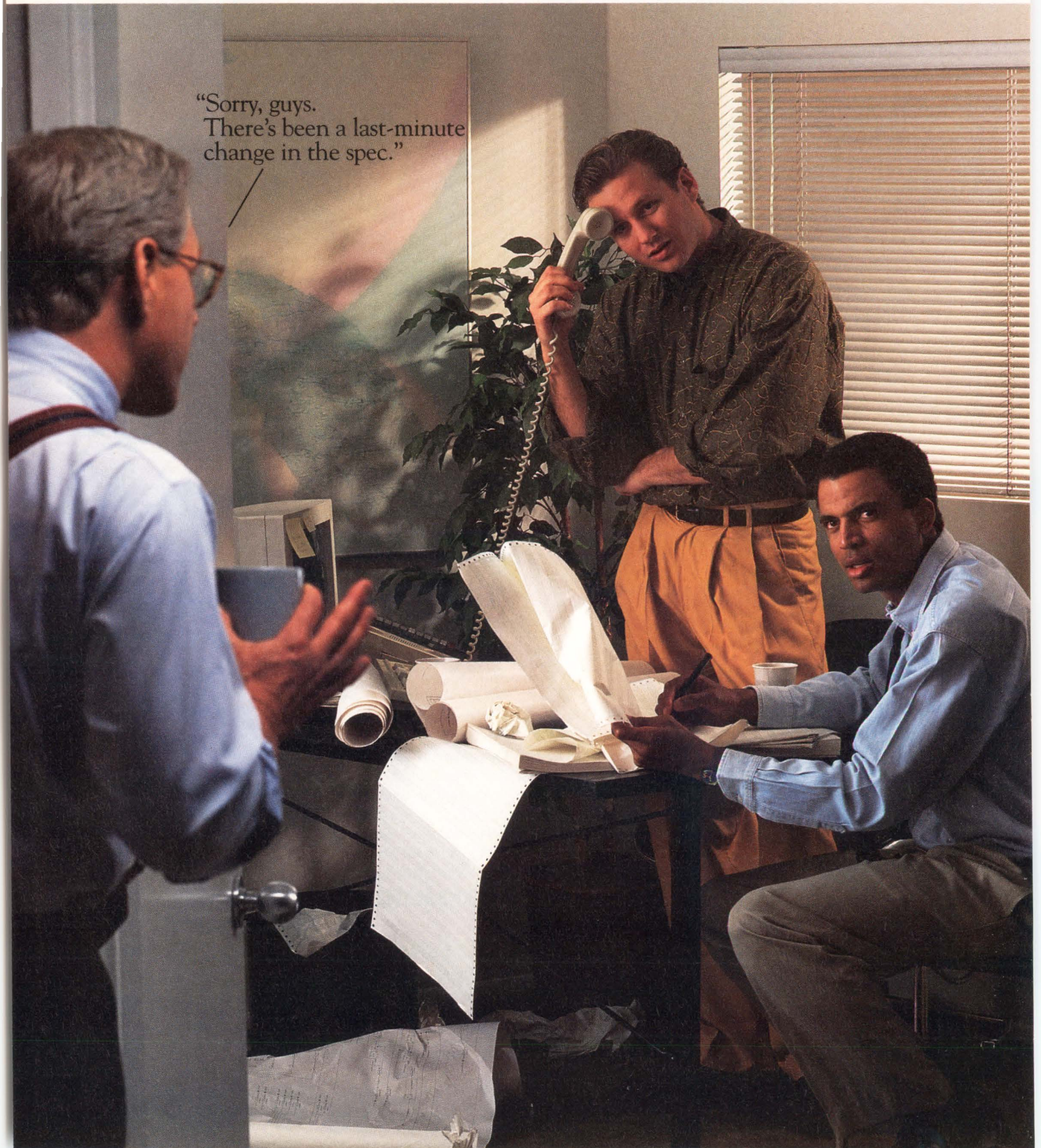
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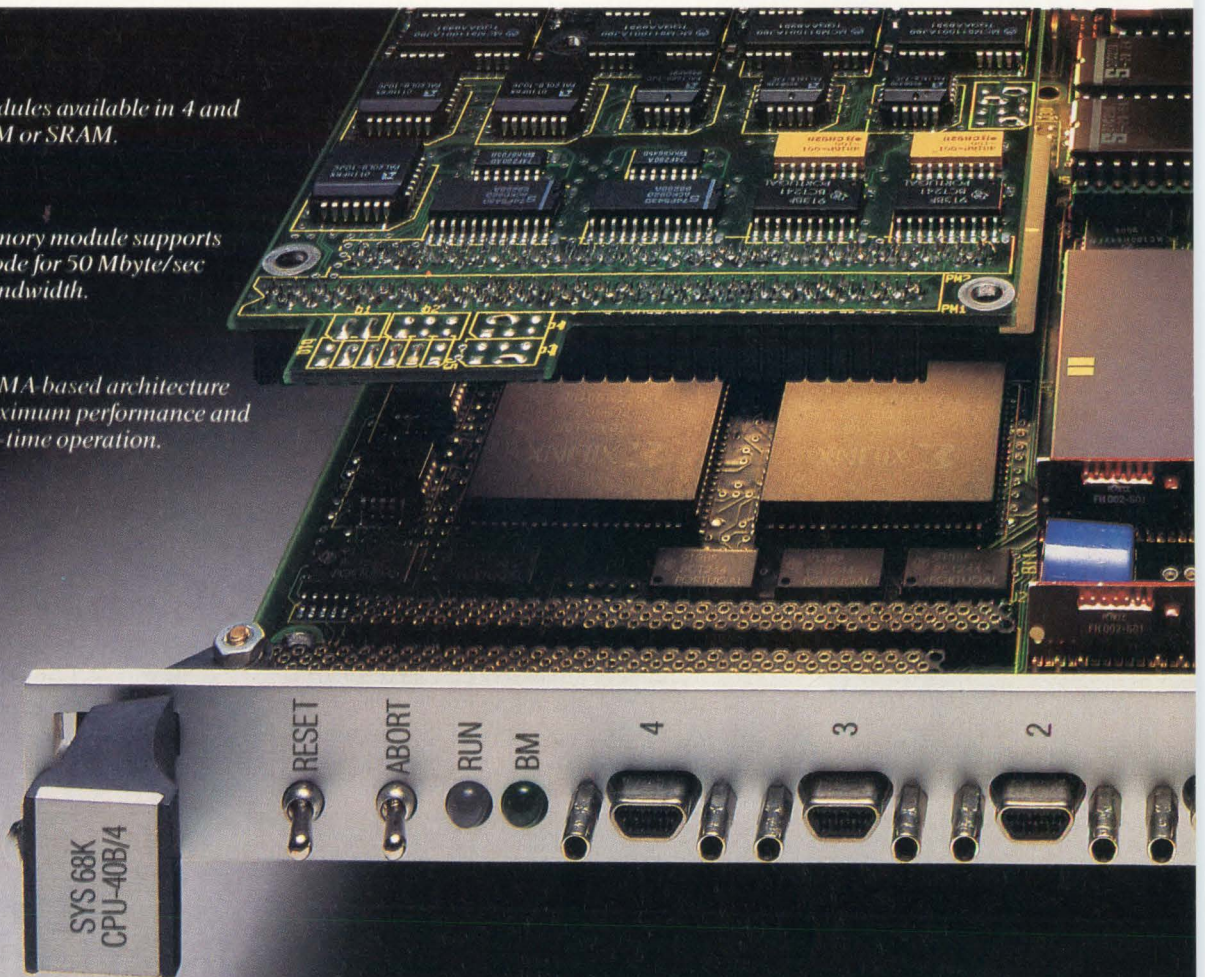
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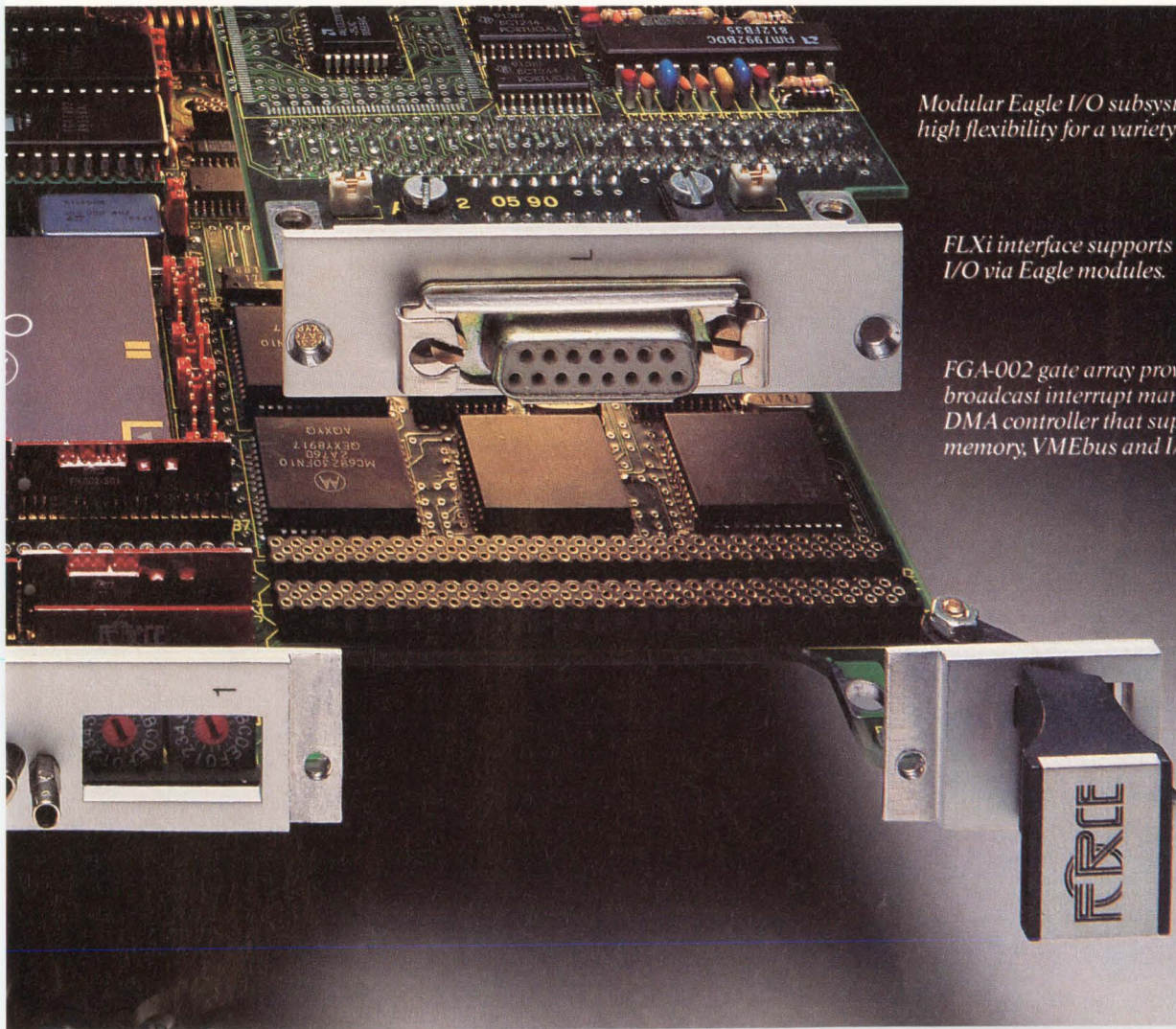
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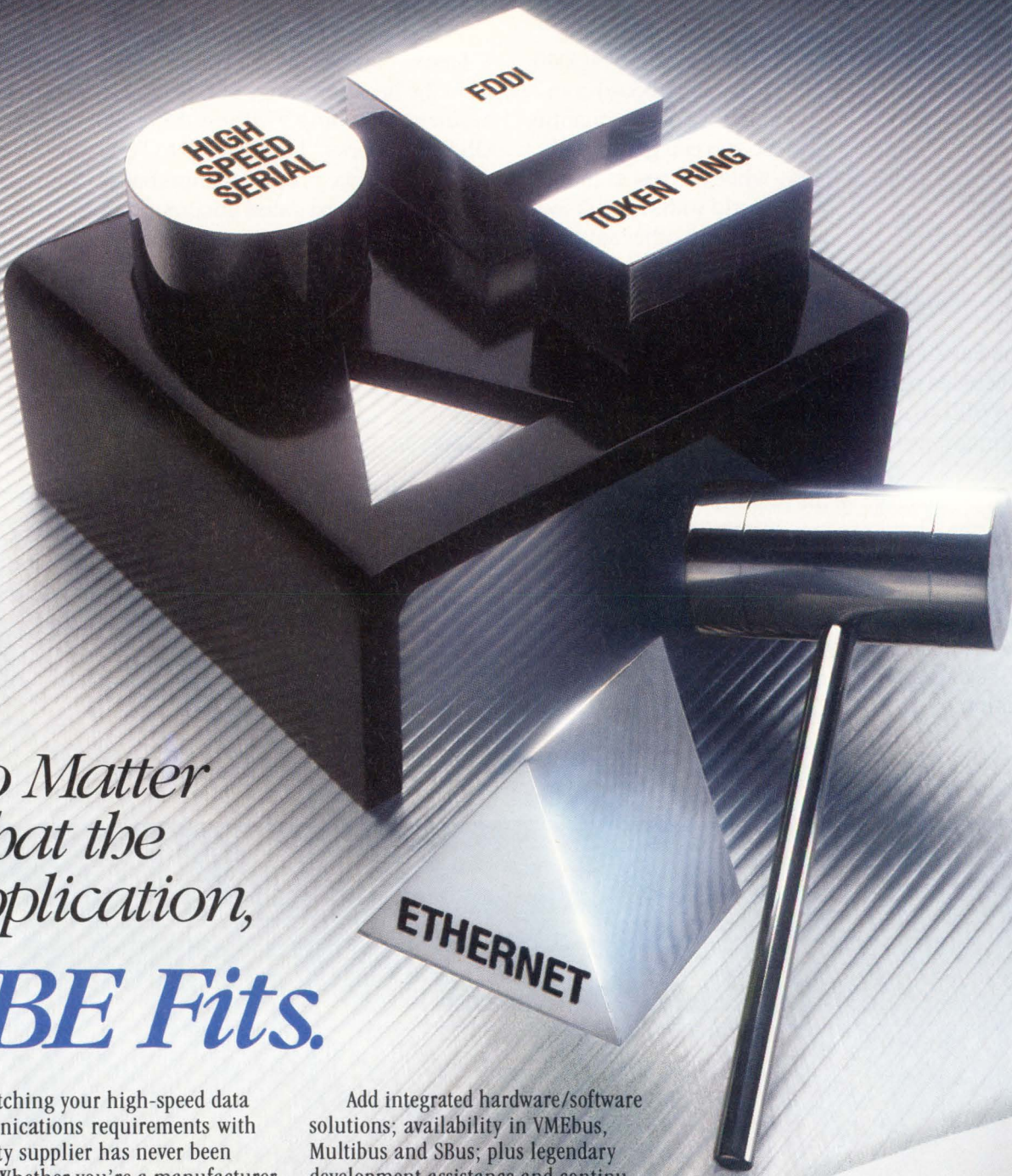
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Slot-0 controllers meet VXI-system needs

At the core of every VXI system lies its controller. Choosing a controller, then, would seem to be the first step in setting up your system, but it isn't.

*Richard A Quinnell,
Regional Editor*

Choosing a controller for your VXI (VME extensions for instrumentation) system requires that you first determine the instrument types, a programming methodology, and your data-throughput goals. Failing to consider these factors may lead you to purchase a high-cost controller that doesn't work any better in your system than a low-cost one.

Four system-level factors impact your controller selection: physical constraints, architectural compatibility, programming methodology, and system performance goals (measured in tests/sec). Cost circumscribes the range of controller choices or can serve as a tie breaker.

Physical constraints are the easiest to resolve. VXI controllers come in two flavors, external and embedded. Both types use plug-in cards to offer VXI slot-0 functions and VMEbus system control (see box, "VXI-controller basics"), but each type has different physical requirements.

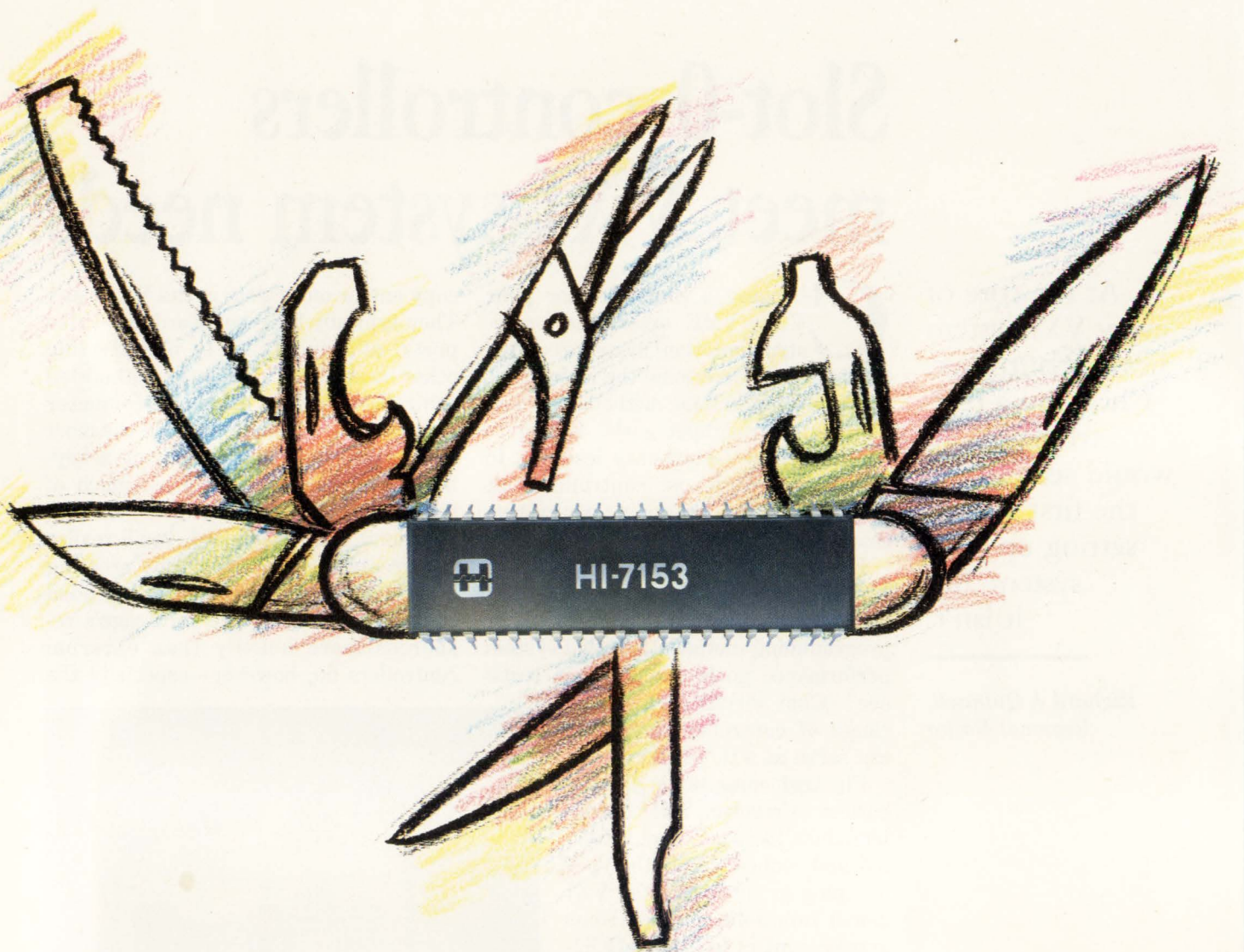
External controllers use a host computer connected via cable to a controller card in a single VXI card slot. This configuration lets you use the host computer as an operator's console and locate it as much as 20 meters from the instrument. An external controller also makes the fewest demands on the VXI cage's power, cooling, and available-slot capacities.

Embedded controllers are stand-alone computers that oc-

cupy one or more slots in the VXI cage. They typically have keyboard and video ports, allowing them to operate like other computers. Because embedded controllers let you move the computer inside the card cage, they yield the most compact system, although using a keyboard and monitor adds back much of the bulk. If your system can run without the monitor and keyboard, you'll realize the greatest space savings by creating a self-contained instrument. Embedded controllers consume the card cage's resources more heavily than external controllers do, however—especially the



Self-contained portable VXI instruments, such as the VXI-B1 from RadiSys (\$9995), require an embedded controller.



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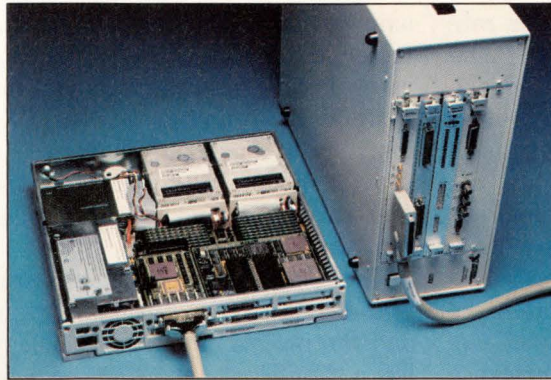
TECHNOLOGY UPDATE

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cage's card slots. Most embedded controllers occupy two or more card slots, although Logical Design Group, National Instruments, and Racal-Dana now offer single-slot embedded controllers.

Architecture limits choice

Architectural considerations are also easy to resolve. As Table 1 shows, external controllers let you use virtually any computer architecture to operate your VXI instrument. The range of embedded architectures is limited, as Table 2 shows. Most embedded controllers use the IBM PC architecture; some have custom architectures. Two notable exceptions are the VAX-based VXI-5300 from Logical Design Group and the National Instruments VXIpc-030, which is built around an Apple Macintosh SE/30



External controllers offer the greatest range of choices for the controlling computer's architecture. The VXI-SB2020 (\$3700) from National Instruments, for example, connects your VXI system to a Sun SPARCstation. Other external controllers work with GPIB, IBM PC/AT, IBM PS/2, and VMEbus host computers.

mother board. A requirement for architectural compatibility, then, may force you to use an external controller.

System performance and programming methodology, the remaining two factors, are much more difficult to resolve because they are closely interrelated. Simply looking at bus bandwidths and concluding

that one controller will outperform another is tempting. An external controller using a GPIB link, for example, is limited to a 1M-byte/sec transfer rate between the VXIbus and the host. Using the MXIbus (multisystem extension bus), a VXIbus extender that National Instruments and Hewlett-Packard support, you can obtain a faster

VXI-controller basics

A VXI controller runs the test application program. The controller communicates with other modules in the system in one of two ways: by directly addressing module registers or through a word-serial protocol. Direct addressing means that the controller uses the VMEbus, on which the VXIbus is based, to access an instrument module's registers as though they were part of the controller's address space.

The word-serial protocol defines a polling handshake method through which one word at a time transfers between a commander and its servant. The commander checks a status register on the servant unit it's communicating with to determine if there is data to read or a place to write data. It reads or writes a single word each time the status register indicates that the way is clear. The servant sets and clears the status registers as appropriate to indicate its willingness to transfer another word.

Although referred to as VXI slot-0 controller cards, VXI controllers do not have to occupy slot 0, nor must VXI slot-0 cards necessarily be controllers. At minimum, a VXI slot-0 card provides two system resources: a 10-MHz ECL system clock (CLK10) and module-identification (MODID) lines.

The MODID lines let the Resource Manager, a software element the VXIbus specification requires, determine what modules are in the system, assign address space, create commander/servant control hierarchies, and manage self-test diagnostics.

Only CLK10 and the MODID lines must physically reside at slot 0. The controller and the Resource Manager can occupy any slot. The controller may also be an external host computer linked to the VXIbus through an interface card. The interface card can also reside in any slot. In practice, however, the 13-slot limit on VXI cages encourages most vendors to combine the slot-0 card functions with the controller card or the controller-interface card. The Resource Manager typically runs on the controller or on the interface card.

The combined slot-0 controller typically handles several additional tasks. It can serve as the control point for the VXIbus's eight trigger lines, handling synchronous, asynchronous, and start/stop trigger protocols. It also can handle the optional Star bus, which provides high-speed communication between modules.

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rate. The theoretical transfer rate of a MXIbus host controller is 20M bytes/sec, although practical considerations such as cable delays limit that rate to about 6M bytes/sec. The embedded controller has the greatest potential speed, theoretically able to operate at the VXIbus's full speed of 40M bytes/sec.

The differing transfer rates are misleading, however. Several factors affect the overall performance of your VXI system, and the controller's data bandwidth is least

among them. The most important factor, naturally, is the actual data rates involved. The speed of the system you're testing and the VXI instrument's measurement speed provide obvious performance limits. You may find that any controller can handle your needs.

The second most important factor is the VXI system's message rate, and the programming methodology has a significant impact on the message rate. VXI instruments communicate in one of two ways: by pass-

ing messages using the VXI word-serial protocol or by directly addressing registers in the VMEbus address space. The two communication methods offer you a tradeoff between the message rate and programming ease.

The word-serial protocol used in message-based communication is quite similar to the GPIB protocol. The similarity is great enough that VXI controllers can transparently convert commands and data between the two forms. The transpar-

Table 1—External VXI controller-interface cards

Company	Model number	Size	Host computer	Link to host	Resource Manager Location	Front-panel connections					Base price	Comments
						GPIB	RS-232C	Trigger	Clock	Other		
Hewlett-Packard Co	HP E1300A	B	Any GPIB controller	GPIB	Onboard	1	1	In		RS-422	\$2320	7-slot mainframe with built-in controller; convertible to stand-alone controller. Battery-backed RAM.
	HP E1301A	B	Any GPIB controller	GPIB	Onboard	1	1	In		RS-422	\$2900	7-slot mainframe with built-in controller; convertible to stand-alone controller. Battery-backed RAM, external floppy-disk option.
	HP E1404A	C	Any VMEbus controller	VMEbus	Host			In/out			\$860	For register-based instrument.
	HP E1405B	C	Any	GPIB or RS-232C	Onboard	1	1	In/out	In/out		\$2820	
National Instruments	VXI-SB2020	C	SPARCstation	MXIbus	Host			In/out	In/out	MXIbus, interrupt	\$3700	Includes host add-in card, VXI card, and cable.
	VXI-MC6000	C	IBM RS/6000	MXIbus	Host			In/out	In/out	MXIbus, interrupt	\$4200	Includes host add-in card, VXI card, and cable.
	VXI-AT2000	C	IBM PC/AT	MXIbus	Host			In/out	In/out	MXIbus, interrupt	\$3800	Includes host add-in card, VXI card, and cable.
	VXI-MC2000	C	IBM PS/2	MXIbus	Host			In/out	In/out	MXIbus, interrupt	\$4200	Includes host add-in card, VXI card, and cable.
	GPIB-VXI	C	Any GPIB controller	GPIB	Onboard	1	1	In/out	In/out	I ² C serial port	\$3000	
NH Research	81120	C	Any GPIB controller	GPIB	Onboard	2				Quiet bus, 34-pin utility	\$4400	
Racal-Dana Instruments Inc	1260-00B	C	Any	GPIB or RS-232C	Onboard	1	1	In/out	In		\$3500	Can execute runtime programs without host interaction.
Tektronix/Colorado Data Systems	73A-151B	C	Any GPIB controller	GPIB	Onboard	1					\$1800	
	73A-155	C	Any GPIB controller	GPIB	Onboard	1		In/out	In		\$2800	
	VX4520	C	Any GPIB controller	GPIB	Onboard	1			In		\$2000	
	VX4521	C	Any GPIB controller	GPIB	Onboard	1		In/out	In		\$3000	
	VX5520	D	Any GPIB controller	GPIB	Onboard	1	2				\$4250	

Note: All units provide slot-0 resources and VMEbus control.



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VXI slot-0 controller cards

ent conversion lets you program your VXI instrument as though it were another GPIB instrument. This approach, in turn, lets you leverage your GPIB programming experience and use GPIB software-development tools.

Message-based communication affords another advantage: It lets you use the standard commands for programmable instrumentation (SCPI). A consortium of nine instrument makers defined these commands to enable you to create

vendor-independent instrument-control programs. The SCPI command set has a limited scope and may not handle all your needs; however, using SCPI can reduce the effect of instrument changes on software.

Communication adds overhead

Message-based communication carries with it a tremendous software overhead. For starters, the messages are all in ASCII and require instruments to interpret the

incoming message in order to execute the commands. The instruments also have to encode their binary data into ASCII before transmitting it to the controller. Similarly, the controllers must decode the data before processing. Software also handles the word-serial protocol's handshaking by polling status registers between word transfers. All this software activity slows down communications.

Hewlett-Packard reported some test results that demonstrate the

Table 2—Embedded VXI controllers

Company	Model number	Size	Width (slots)	Architecture	CPU	Clock rate (MHz)	RAM (bytes)	1.4M-byte floppy disk	Hard disk (megabytes) included/ (optional)
Hewlett-Packard Co	HP E1300A/01A OPT 020	B	N/A	HP Series 300	68000	8	256k to 2M	Optional	(20)
	HP E1405B OPT 020	C	1	HP Series 300	68000	16	512k to 1M		
	HP E1480A	C	4	HP Series 360	68030	25	4M to 16M		
Logical Design Group Inc	VXI-5300	C	1	DEC Vax	rtVAX300	20	4M to 16M		
National Instruments	VXIpc-386/1	C	1	IBM PC	80386	20	1M to 8M		20 (40)
	VXIpc-386/2	C	2	IBM PC	80386	20	1M to 8M	X	20 (40, 105)
	VXIpc-030	C	2	Macintosh SE/30	68030	16	4M to 8M	X	(40, 80, 210)
	VXIcpu-030	C	1	Custom	68030	25	2M to 16M		(20, 40)
Racal-Dana Instruments Inc	1265	C	2	IBM PC	80386	16	2M to 8M	X	40
	1260-00B	C	1	Custom	68070	N/A	512k to 4M		
Radisys Corp	EPC-2	C	2	IBM PC	80386	16	2M to 16M	X	40 (100, 200)
	EPC-2e	C	2	IBM PC	80386	16	2M to 16M	X	40 (100, 200)
	VXI-B1	B	2	IBM PC	80386SX	16	2M to 4M		(40, 100)
	VXI-B2	B	3	IBM PC	80386	25	2M to 4M		(40, 100)
Tektronix/Colorado Data Systems	VX4542	C	3	IBM PC	80286	16	2M to 4M	X	20 (40)
	VX4544	C	3	IBM PC	80386	20	4M	X	40 (119)
	VX5530	D	2	IBM PC	80386	16	2M to 8M	X	40
	VX5535	D	2	IBM PC	80386	20	2M to 8M	X	40

Notes:

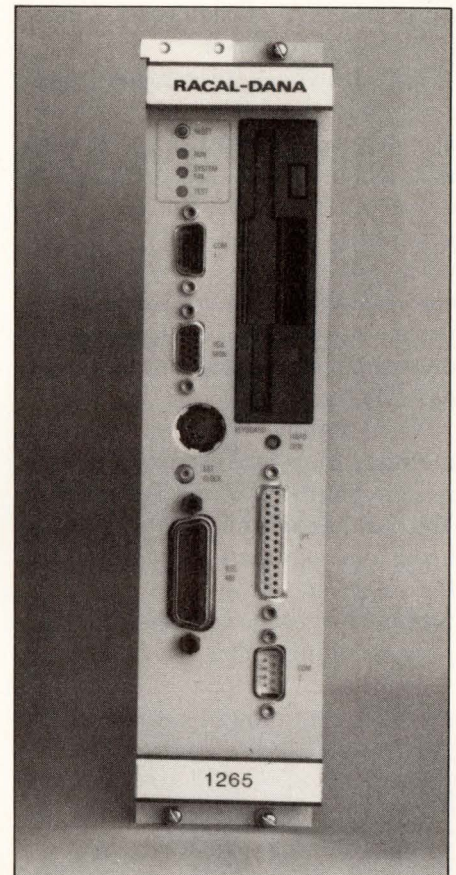
1. All units provide slot-0 resources, VMEbus control, and Resource Manager.
2. Units with GPIB interface can control other GPIB instruments.
3. Units with IBM PC architecture include keyboard, printer port, and VGA graphics interfaces.
4. Units with Macintosh architecture include mouse, keyboard, and video ports.
5. N/A=Not available.

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impact of command-interpretation overhead on a VXI system's speed (Ref 1). A Hewlett-Packard customer tested two digital multimeter units, one with a repetitive measurement rate of 300 readings/sec and one with a rate of 1000 readings/sec. When the customer used the instruments to make a series of measurements, changing settings between measurements, the speeds dropped to 50 and 4 readings/sec, respectively. The dramatic drop in the second instrument's speed is at-

tributable solely to its command-interpretation overhead.

Using SCPI relieves the command-overhead burden somewhat. SCPI commands are hierarchically structured, thus allowing a manufacturer to create a fast interpreter. Hewlett-Packard compared two of its counters that have similar hardware by using the devices to measure a test signal's frequency, period, and rise time. One instrument used a proprietary command set; the other used SCPI. The SCPI



The PC on a card is typical of most embedded controllers. The Racal-Dana 1265 (\$8680) includes the standard keyboard, printer, serial, and VGA video ports found on a PC, as well as a floppy-disk drive.

device operated 10 times faster.

Tektronix/Colorado Data Systems has attacked the handshaking-overhead burden with what it calls "smart registers." These registers are specialized hardware that implement the VXI word-serial protocol as a state-machine instead of in software. Both the sender and receiver must have smart registers for you to notice any speed improvement, however.

Register-based communication bypasses all of the overhead bottlenecks by letting the controller access command and data registers directly. The result is much faster operation. The HP E1326 DMM, for example, sets up and makes a single

Front-panel connections					Base price	Comments
GPIB	RS-232C	External clock	Trigger I/O	Other		
X	1		In only	RS-422	\$3320	Battery-backed RAM.
X	1	X	X		\$3830	Battery-backed RAM; external floppy-disk option.
X	1	X	X	Ethernet	\$10,500	External floppy-disk option; RGB video output.
X	2			Ethernet, SCSI	\$10,000	Real-time calendar/clock; battery-backed RAM.
X	2	X	X	Floppy disk	\$9000	
X	2	X	X	Floppy disk	\$9000	
X	2	X	X	Floppy disk, SCSI	\$14,800	
X	2	X	X	Ethernet, SCSI	\$5995	Runs VXWorks real-time operating system.
X	2	X			\$8680	
X	1	X	X		\$3000	
X	2	X			\$5995	
X	2	X		Ethernet	\$7345	
	2		X		\$9995	
	2		X		\$12,285	
X	2	X	X		\$4500	Includes keyboard and PC/AT expansion slot.
X	2	X	X		\$5500	Includes keyboard and PC/AT expansion slot.
X	1	X	X		\$18,000	Includes keyboard, mouse, and VGA monitor.
X	1	X	X		\$24,000	Includes keyboard, mouse, and VGA monitor.

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reading in 264 μ sec when using register-based communication. The same transaction requires 6.7 msec if it's message-based.

The drawback to register-based communication is that you must create unique programming for each instrument, which adds to software development time. Further, programming a complex instrument with numerous control parameters can become tedious and error-prone. A good set of software drivers from the instrument maker can ease the task.

Your choice of programming method, therefore, strongly determines your system throughput. You can mix methods, of course, by using message-based programming for most of the system and fine-tuning the rest with register-based programming. The programming

method you choose, though, will tell you your controller needs.

If you decide on a message-based system, an embedded controller offers no performance advantage. In the absence of physical constraints, an external controller will work just as well and probably cost less. An external controller may even prove to be faster. According to Ron Wolfe, strategic marketing manager for National Instruments, the difficulty of shoe-horning a computer into a VXI module virtually guarantees that embedded controllers won't keep pace with the performance improvements occurring in desktop computers. The computer's performance affects the duration of communications overhead.

If you're using register-based programming, embedded controllers have an advantage over GPIB-

based external controllers. An embedded controller addresses instrument registers as part of its own address space. When using an external GPIB controller, you can only PEEK and POKE into registers. These primitive operators may not be fast enough if your application requires register-based speeds.

MXIbus external controllers represent a hybrid solution. The MXIbus extends the VXIbus outside the cage, which lets an external controller directly address registers as if the controller were physically in the VXI cage. Currently, only National Instruments has MXIbus-based controllers.

The controller-performance issue is a moving target, however. SCPI and Tektronix/Colorado Data Systems' smart registers represent efforts to bring register-based speeds

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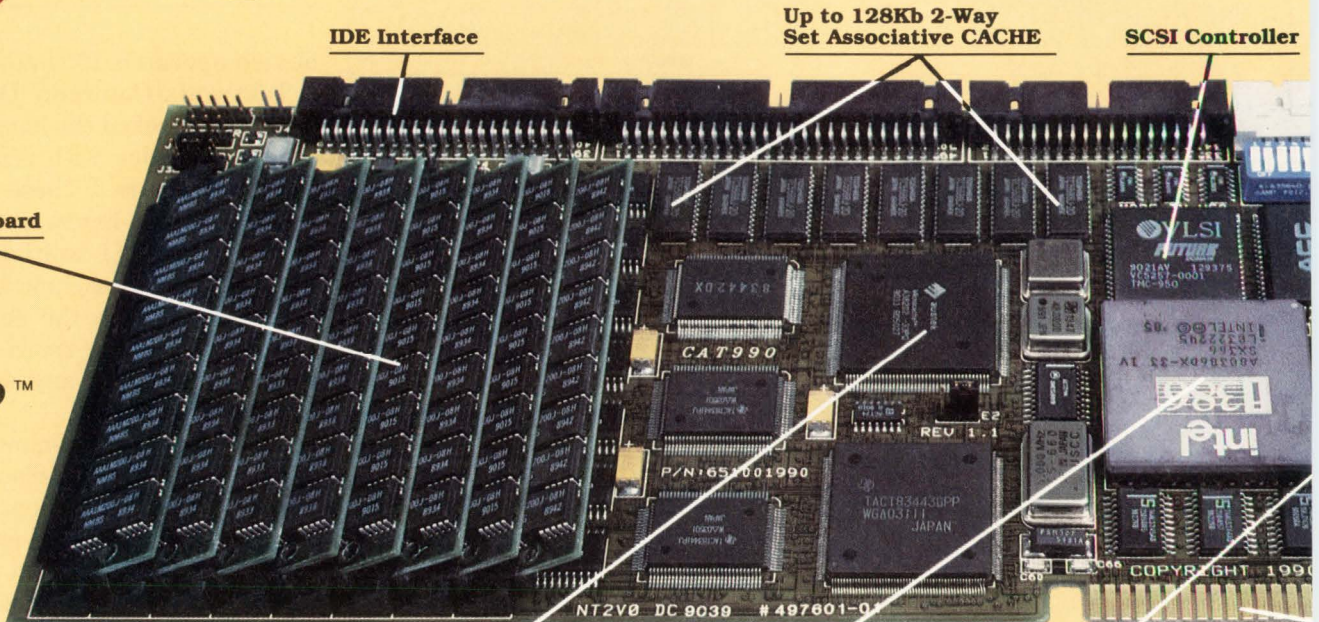


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to message-based systems. Hewlett-Packard has firmware, which is built into its controllers, that interprets message-based commands for its register-based instruments, thus simplifying programming. Such improvements will continue to occur as more instrument makers identify and remove obstacles to VXI-system users. **EDN**

Reference

1. DesJardin, Larry, "VXI versus GPIB: Is VXI actually faster?" *VXI Journal*, November 1990, pg 11.

Article Interest Quotient
(Circle One)

High 515 Medium 516 Low 517

For more information . . .

For more information on the VXI controllers discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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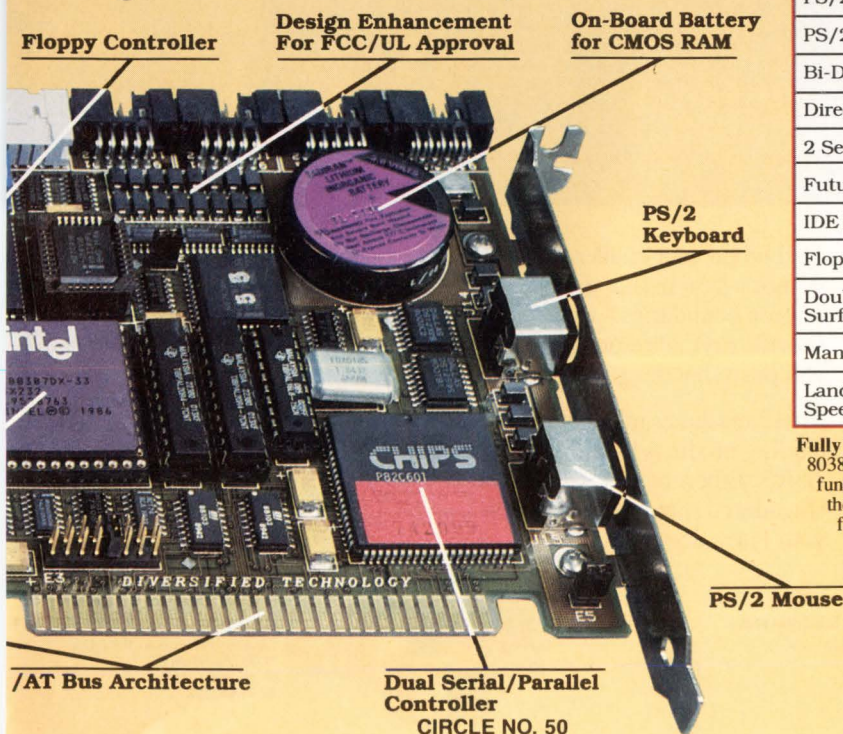
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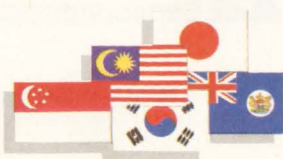


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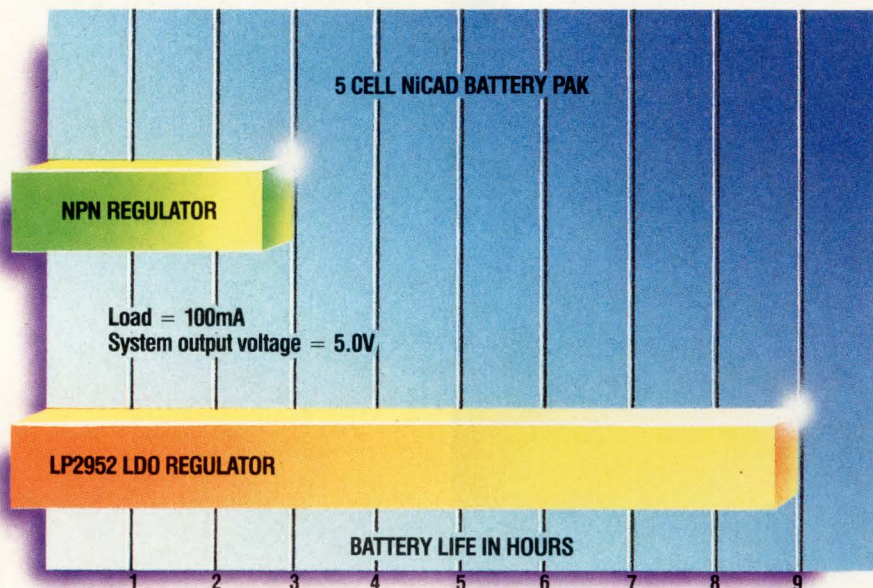
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Io	50mA	100mA	100mA	250mA	250mA	250mA	1Amp	1Amp
Vo	5V	5V	1.23V to 29V	1.23V to 29V	1.23V to 29V	5V	5V, 8V, 9V, 10V, 12V, 15V	5V to 20V
Package	Z, M	Z	J, N, M, H	N, M	N, M	T	T	T

H = Metal Can
J = Ceramic DIP
M = Surface Mount
N = Plastic DIP
T = TO-220
Z = TO-92

*(with Additional Comparator)

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μP core and proprietary command set allow SCSI-2 ICs to automate bus sequences

An on-chip μP core allows the MB86600 family of SCSI-2 ICs to perform sequences of commands without interrupting the host CPU. The ICs support the "wide" and "fast" data transfers defined by the latest version of the ANSI SCSI specification, X3.131-1990. You can use the ICs to implement a SCSI host design that complies with the CAM (Common Access Method) or the LADDR (Layered Architecture Device Driver) de facto standards.

The SCSI-2 ICs support target and initiator applications. A proprietary command set features 22 initiator-specific commands, and 22 commands used by targets. Each of the MB86600 commands cause the ICs to perform one or more SCSI-2 commands. The ICs automatically handle the requisite bus phases and sequences.

Fig 1 depicts the architecture of the ICs. The chips have separate data paths for control signals and data transfers. Using no glue logic, host CPUs, either the Intel 80x86

or the Motorola 68000 family, interface to the SCSI-2 ICs via the microprocessor-unit interface. An input signal to the SCSI-2 ICs directs them to automatically handle differences in control signals and byte ordering.

A 32-byte FIFO buffer paces data transfers between the SCSI bus and the DMA interface. The buffer permits a transfer offset value as high as 32 bytes during synchronous data transfers. Therefore, the ICs can transfer 32 bytes of data between each SCSI-2 REQ/ACK (request/acknowledge) signal handshake. The ICs also include a 40-bit byte-transfer counter. The counter allows the ICs to automatically transfer blocks of data as large as 64k bytes.

The ICs also have 32-byte send-and-receive buffers that handle command, message, and status information. Therefore, you can program the host to load a sequence of SCSI-2 operations without waiting for specific bus phases to com-

plete. Finally, you can load the 512-byte program memory with the proprietary commands supported by the MB86600 family of ICs.

The MB86601 and MB86602 ICs support 10M-byte/sec "fast" synchronous data transfers. The former provides signal transceivers on chip for single-ended SCSI-2 applications, and the latter contains control circuitry for external differential or single-ended transceivers.

The ICs come in a 100-pin plastic quad flatpack and cost \$19.95 (1000). You can buy samples now; production quantities will be available in the third quarter of 1991. The MB86603 and MB86604 will support 16-bit "wide" SCSI-2 data transfers and will be available in the fourth quarter.—*Maury Wright*

Fujitsu Microelectronics Inc, 3545 N First St, San Jose, CA 95134. Phone (408) 922-9000. FAX (408) 432-9044.

Circle No. 730

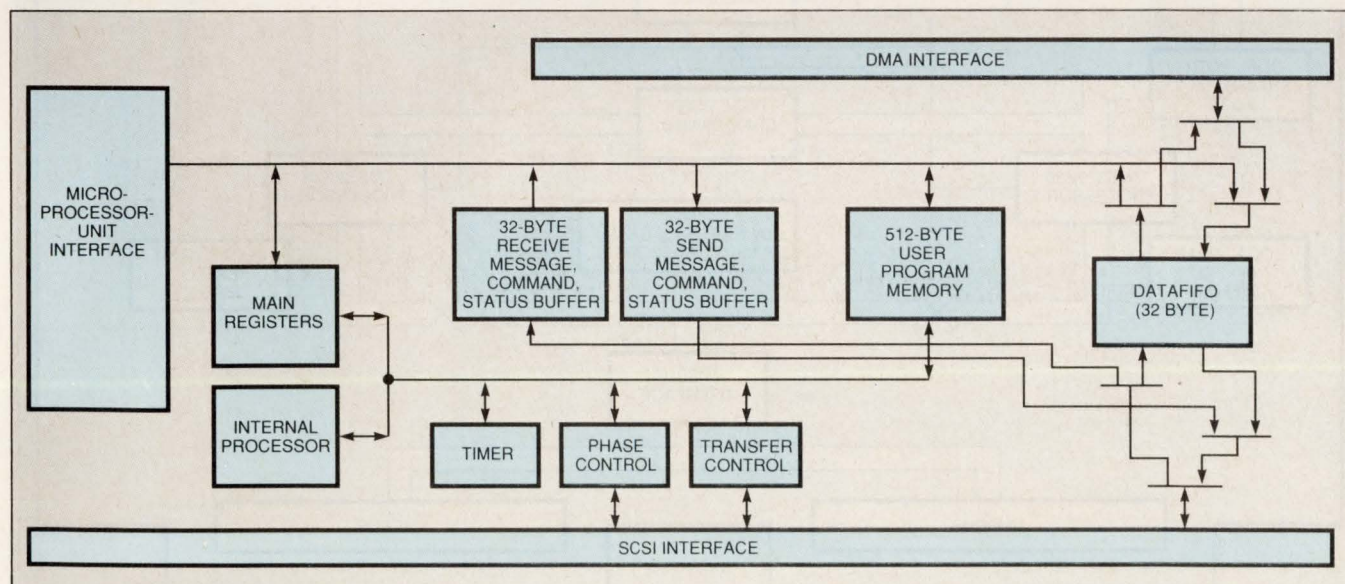


Fig 1—The 512-byte program memory and 32-byte send-and-receive buffers allow MB86600 ICs to perform sequences of SCSI-2 commands without interrupting the host CPU.

VMEbus card couples two TMS320C30s for general-purpose DSP applications

The DPV30 is a 6U VMEbus DSP board that employs two TMS320C30 processors running at 33 MHz. The essential parts appear in the block diagram of Fig 1. The twin processors operate independently, in parallel, or by pipeline multiprocessing. System architecture tightly couples the processors with dual-port static RAM (SRAM), which occupies the same address location of each processor. The dual-port SRAM's capacity is $2k \times 32$ -bit words and enables data transfers between processors with zero overhead. One processor shares an additional $2k \times 32$ -bit-word dual-port SRAM with a slave parallel I/O port, and the other processor links directly to a master parallel I/O port.

You can achieve multiprocessing capability by daisy-chaining master-to-slave I/Os on any number of DPV30 boards and can attain similar tight coupling between all processors.

This board functions as an application-development platform in Sun SPARCstations or for embedded DSP with a real-time VMEbus host processor. You can develop applications in MS-DOS or Unix using IBM PC or compatible computers, or Sun SPARCstations, respectively.

Each TMS320C30 processor has a separate, local $64k \times 32$ -bit-word, zero-wait-state SRAM to optimize program execution speed. You can expand this SRAM to $256k \times 32$ -bit words using plug-in SIP packages.

Both processors share additional RAM, which—with the local SRAM—is also directly accessible from the VMEbus backplane. This feature enables data-array transfers between processors—or the VMEbus—without affecting local processing. Depending upon your application, optional models have this additional RAM fitted with $128k \times 32$ -bit-word one-wait-state SRAM or $1M \times 32$ -bit-word dynamic RAM (DRAM), expandable to $512k \times 32$ -bit words or $4M \times 32$ -bit words, respectively.

Other optional models include a factory-fitted daughter board accommodating a dual-channel ADC and dual-channel DAC. One option provides 16-bit delta-sigma ADCs

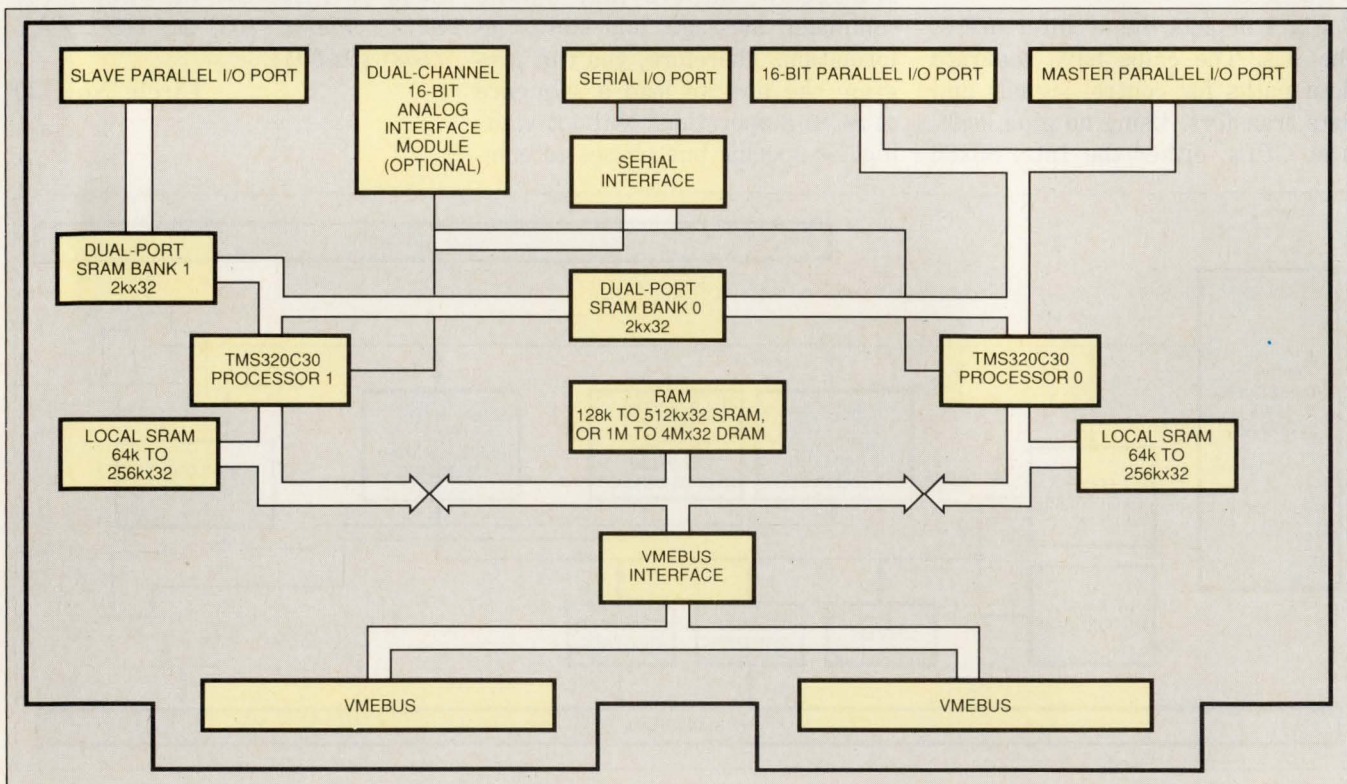
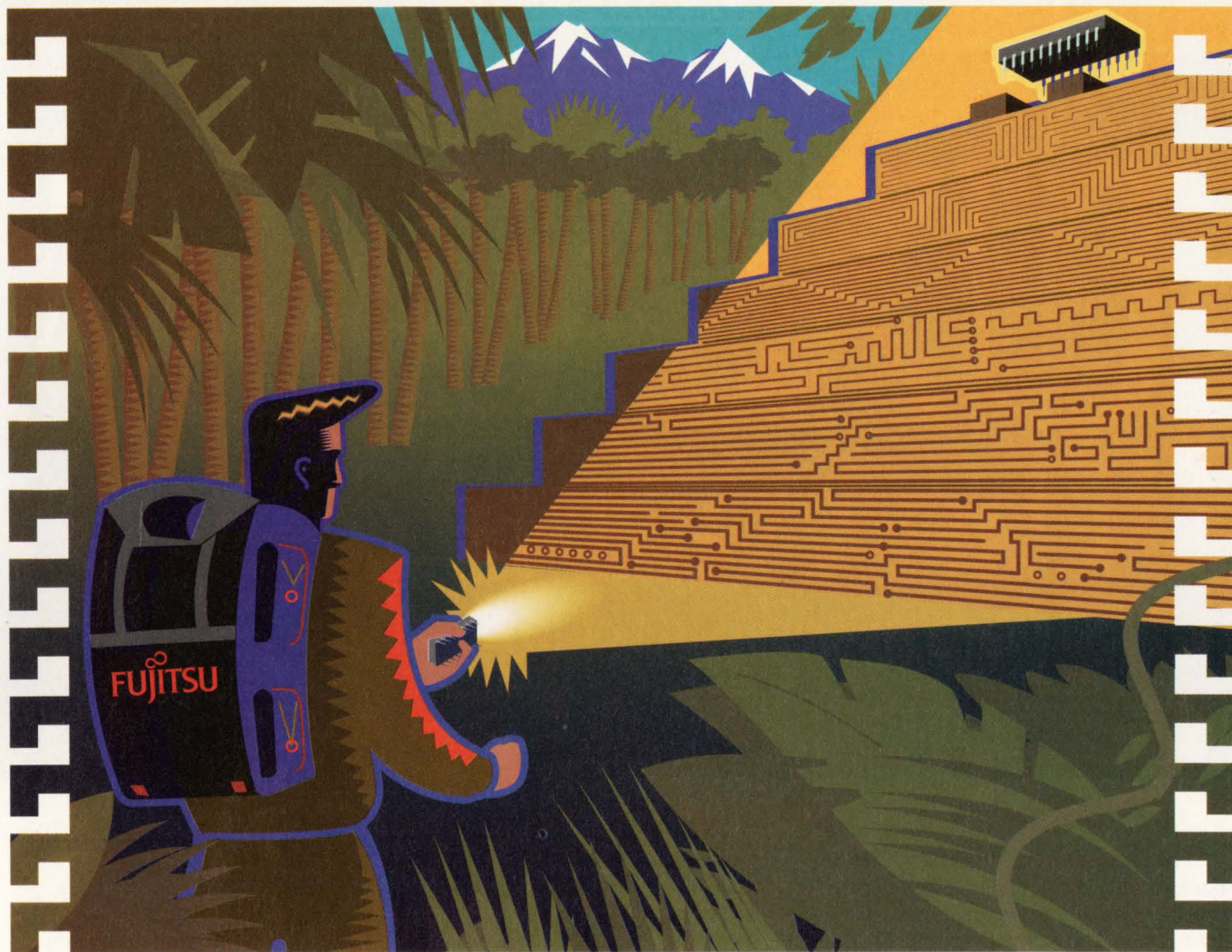


Fig 1—You can achieve multiprocessing capability using any number of DPV30s by daisy-chaining master to slave I/Os.



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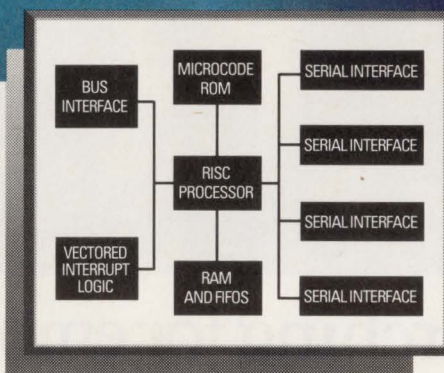
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UPDATE

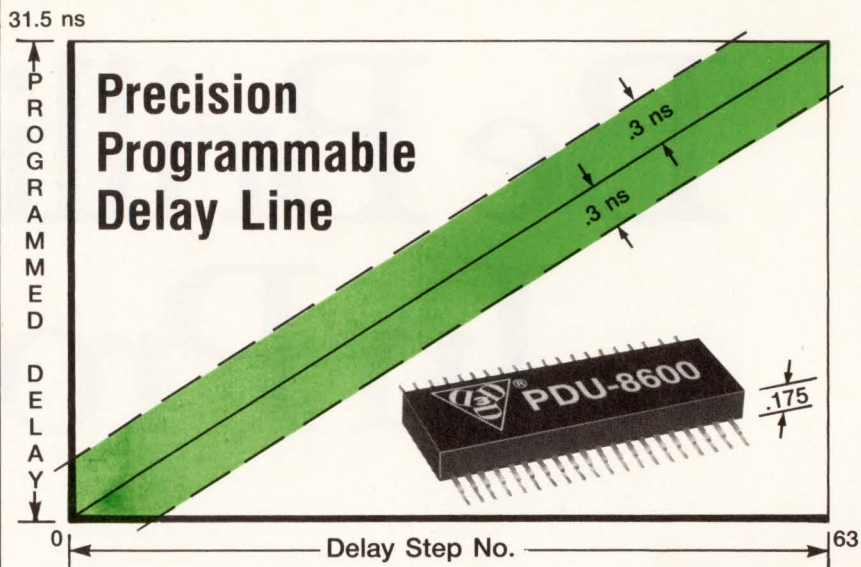
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Circle No. 731



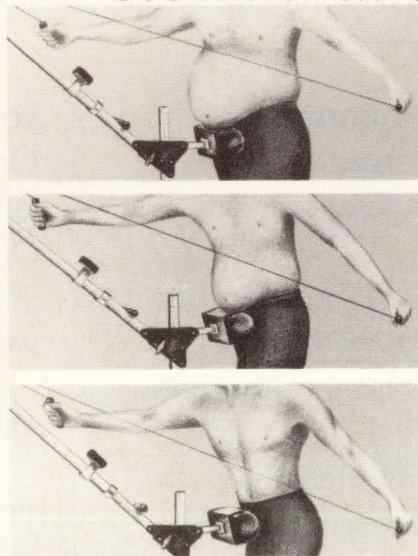
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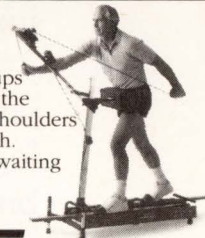
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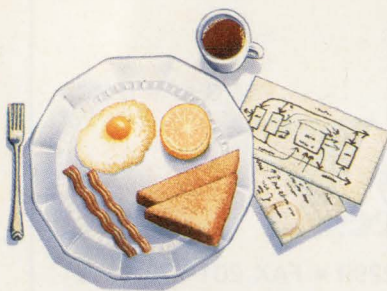
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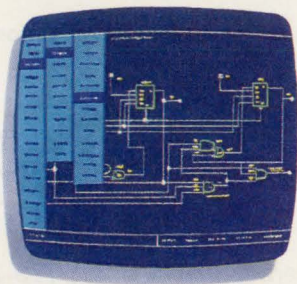
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Be Brilliant At In Productio



7:05 am: Breakfast

Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



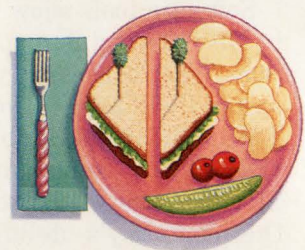
8:50 am: Design

You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.



11:00 am: Place & Route

You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm: Lunch

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They're a feast for your imagination.

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They're the core of the Action Logic System, Actel's comprehensive design and production solution for creating

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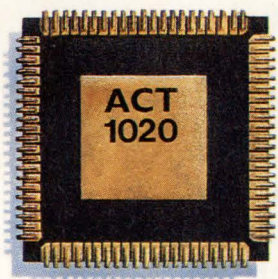
And do it in hours instead of weeks. Even between meals.

How? With features like 85% gate utilization. Guaranteed. Plus

100% automatic placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most

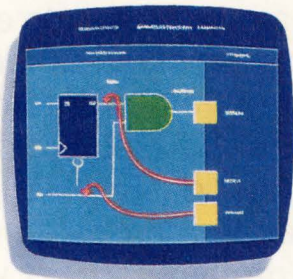
Actel FPGA Product Family		1010A	1020A
Equivalent Gate Array		1200	2000
Gates	PLD/LCA	3000	6000
User I/O		57	69
System Clock (MHz)		20-40	20-40
Availability		NOW	NOW
Technology (micron)		1.2	1.2

Breakfast And n By Dinner.



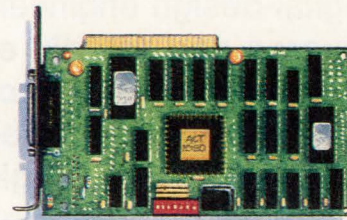
1:15 pm: Program

You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a very quick coffee break while your design becomes a reality.



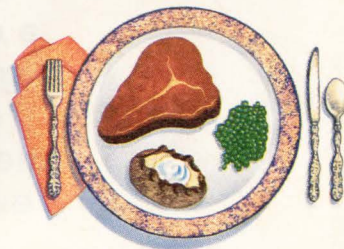
1:25 pm: Test

You do a complete, real-time performance check, with built-in test circuits that provide 100% observability of all on-chip functions. *Without* generating any test vectors.



4:00 pm: Production

Your pride and joy is designed, created, tested, and off to the boys in Production. And you're finished way ahead of schedule! Better think of something to do until 5:00.



6:00 pm: Dinner

Remember dinner? Normal people actually go home and eat with their families. On your way, start thinking about how Actel's logic solution can help you be brilliant tomorrow.

tedious part of the job by hand.

Design verification is quick and easy with our Actionprobe™ diagnostic tools, for 100% observability of internal logic signals. Guaranteed. So you don't have to give up testability for convenience.

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FPGA

DESIGN METHODS

Digital-design engineers are beginning to employ a diverse and rapidly evolving class of large programmable devices, called field-programmable gate arrays. As varied as the architectures of these devices are, engineers' design methods are even more diverse. However, the design method you do choose can profoundly affect which devices you can use.

Charles H Small, Senior Editor

The siren song of field-programmable gate arrays (FPGAs) promises quick and effortless design cycles powered by magic software. In the world to be, an engineer need only whisper hints about his desired design to the magic software. Then, the jinni in the workstation will take care of all the niggling details that once were done manually: minimizing the logic, selecting the best devices, partitioning the design over multiple devices, routing the design, simulating it, and generating test vectors. In this vision of the future, FPGAs are only a brief pause in purgatory before the design achieves apotheosis as a gate array.

FPGAs fit perfectly into that peculiarly American vision of reality: a reality having an inconsequential past, a fleeting present, and a wonderful world to be. Americans see themselves as pioneers constructing a shining future out of a crude, rough present. What's behind you doesn't matter.

To take the pulse of the body of current practice, EDN spoke with 40 American digital-design engineers about their experiences designing with FPGAs. This group does not constitute a statistically valid sample, but it is big enough for a reality check.

Reality turns out to be twofold: first, no single FPGA methodology exists and, second, real life is much more

prosaic, mundane, and tedious than are the promises of what is to come.

The overwhelming majority of engineers interviewed work on personal computers, not workstations. The methodology of the only designer claiming to be doing concurrent design—yet another wave upon a sea of change—consists of sprinkling 22V10s around his design in strategic places in an effort to minimize pc-board reworking.

Few are doing trash compaction—that is, recasting existing PAL-device designs into FPGAs. In fact, one designer of fault-tolerant computers notes that such integration creates the potential for a single-point failure—lowering reliability. Designers do not use FPGAs just for prototyping what will eventually be gate-array designs. Their circuits are new designs that will ship with the FPGAs installed.

Certain gate-array foundries report that 30% of their business consists of rolling over FPGA designs to gate arrays. Despite these reports, upgrading FPGA designs to gate arrays is only a faint thought in the back of the minds of the engineers interviewed. In fact, one designer eagerly awaits even bigger FPGAs than those currently available so that he can get his designs out of gate arrays and into FPGAs. Most wish only for



plastic-packaged, 1-time-programmable versions of their FPGAs. And low-cost, mask-programmed PAL devices are a fond memory.

Some users bitterly resent being locked into what they see as high-priced software from FPGA vendors, preferring more universal, third-party software. These designers ask pointedly if FPGA vendors are in the chip business or in the software business. Others feel secure getting their software and FPGAs from the same source in a timely, thoroughly supported fashion. Some prefer to stick with offerings from a single FPGA vendor; others strive to check out each new device no matter which company offers it, and are willing to pay for whatever software each new device requires.

Exploring the avenues of FPGA design methods requires consideration of your overall approach to design, as well as the software tools you use. (Photo courtesy Data I/O)

Their opinions on current FPGA pricing ranged from a noncommittal "acceptable" to "outrageous," "out of control," "out of hand," "unquestionably out of reach," and "we really need some second sources and competition here."

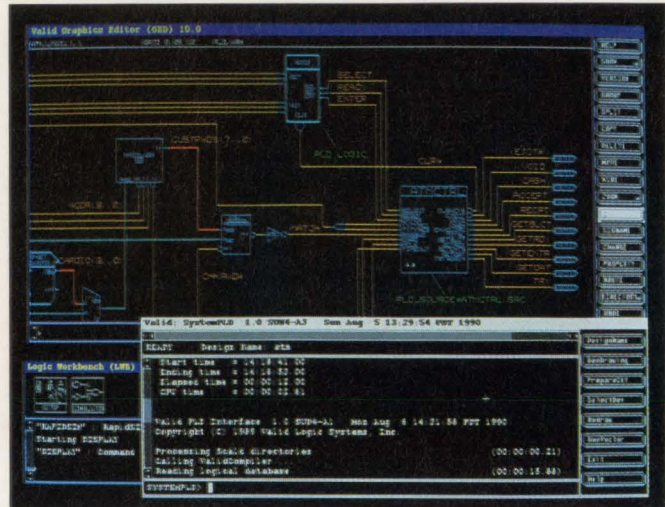
Opinions on the importance of FPGA semiconductor technology are mixed and show no clear preference. FPGAs come in a bewildering variety of programming technologies: fuse, antifuse, UV-erasable, electrically erasable (EE), and RAM cells. Most users profess to

Some users bitterly resent being locked into what they see as high-priced software from FPGA vendors. They prefer more universal, third-party software.

be unconcerned with programming technology, evaluating devices only by how large they are and how fast they can run.

A few need FPGAs that can be reprogrammed in circuit, a requirement that precludes all but RAM- and EE-based FPGAs. Some applications, such as video interfaces or communications equipment, demand field-reprogrammable hardware. One user cites the need to rework surface-mount-technology pc boards as a reason to prefer in-circuit-programmable FPGAs to ones that have to be removed from the board to reprogram them. On the other hand, two users avoid reprogrammable devices altogether, quoting government regulations that prohibit devices that can change their programming after leaving the factory.

Each engineer interviewed has his own unique way of working with these new, very large, programmable devices. Overall, their methods break down into two broad categories: extensions of familiar PAL-device methods and methods that resemble gate-array techniques or, strangely enough, designing with antiques such as small-scale-integration and discrete logic (Fig 1). But sticking with PAL-device methods doesn't guarantee that you can work with your brain coasting in neutral. Even designers that chose to stick with



You can mix FPGAs with other devices by using SystemPGA when doing circuit design on a workstation running Valid software.

familiar PAL-device methods still had to rethink the way they do logic design.

These engineers' experiences were at odds with management's fixation on shortening time to market. One engineering VP expressed this fixation succinctly in

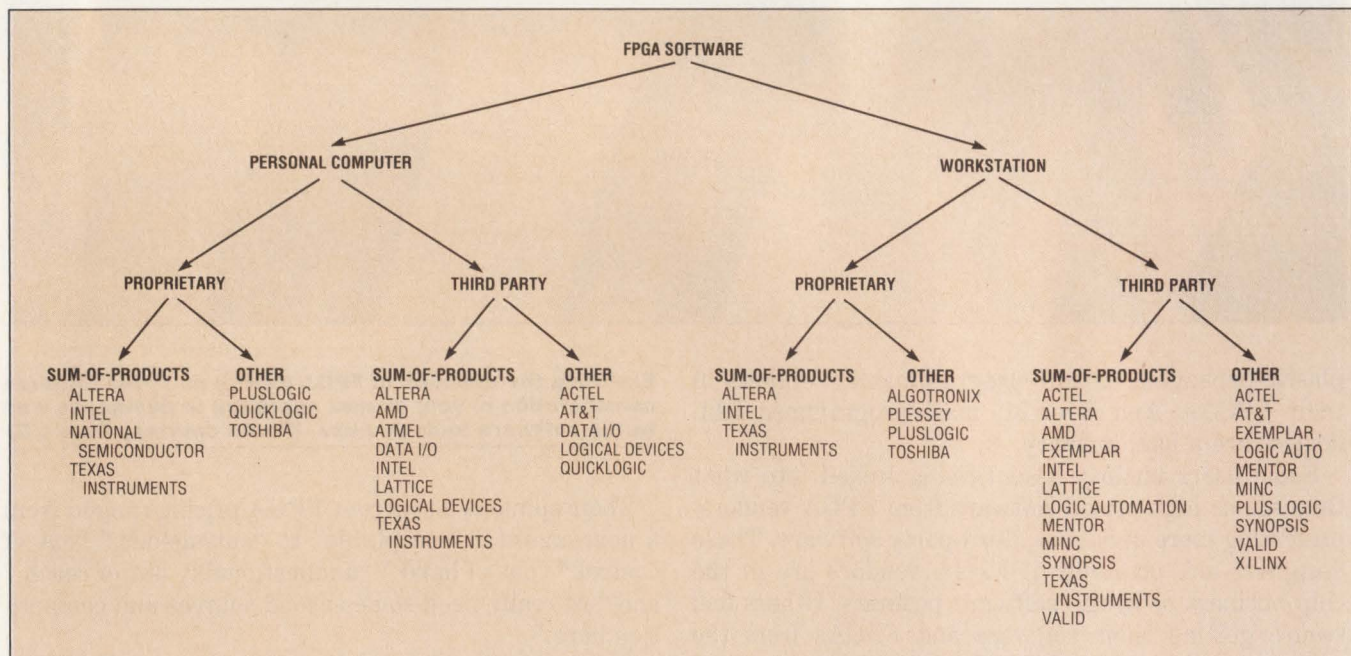


Fig 1—This chart provides a starting point for matching your preferred FPGA-design method to possible devices. There are eight software categories based on the computer the software runs on, the source, and whether it applies to sum-of-products FPGAs or other types of FPGAs. The third-party categories mix device vendors and software vendors. Not every third-party software vendor supports every device listed in the same column; coverage is more spotty than this simple chart indicates.

practical terms when he said, "I'll spend money on anything that will save time. I won't buy anything that takes time. I don't want my engineers taking more than an afternoon learning how to use any FPGA."

All the engineers interviewed said that they could not work from published specs for FPGAs. Instead they had to experiment with the devices for a considerable time before they achieved enough expertise to produce optimal designs. Further, they found that they preferred to do many design tasks, such as selecting devices and partitioning designs over multiple devices, manually, even if they had software for performing these tasks automatically.

Managers fixated on time to market would do well to review the history of technology. Henry Ford and his associates invented the production line between 1913 and 1914 by optimizing every operation for minimal execution time. Until then, work was mostly task-oriented, not time-oriented. The key factors in such minimal-time optimization were to eliminate any need for skill on the part of the worker and to reduce the number of operations each worker performed to the absolute minimum. But as soon as these budding industrial engineers had their production lines optimized, they had to deal with a 350% yearly turnover in workers. Even the most desperately poor, unskilled worker could not stand the unrelentingly monotonous work for long.

Engineers become engineers because they like to understand how things work and because they like to solve problems. Few engineers become engineers because they simply like to run programs. Engineers' experiences with Xilinx FPGAs illustrate that they are really, at heart, task-oriented artisans, not time-oriented automatons.

When they first appeared, the Xilinx FPGAs were a radical departure from any existing programmable-logic devices. Until then, PAL devices and most other PLDs realized the canonical sum-of-products form of logic equations. In the course of transforming the sum-of-products ideal into a reality, PAL devices ended up with definite, hard limitations that channeled designs into certain courses. The logic elements in PAL devices have high, but hard-limited, fan-in specs. PAL devices also have relatively few outputs or registers for the amount of logic they contain. Lastly, the sum-of-products form leads to consistent, predictable timing because PAL devices have essentially only two layers of logic. And at least one end of each internal connection comes already hardwired.

Xilinx FPGAs are completely different. The logic

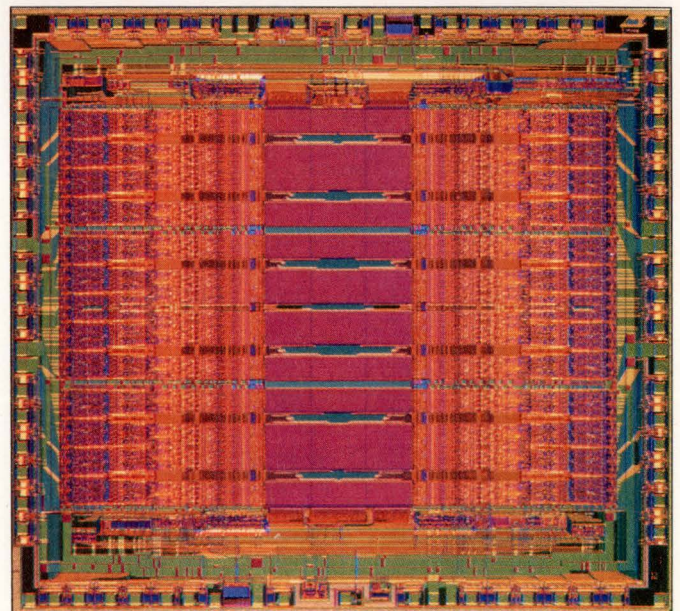
elements in these FPGAs have very limited fan-in compared to the logic elements in a PAL device. The FPGAs have an I/O driver for every pin. Most importantly, their timing isn't designed in. Rather, the speed at which a design in a Xilinx FPGA runs depends heavily on how intelligently the designer lays out his design. In a Xilinx FPGA, both ends of each internal connection are uncommitted until you program the connections.

Four years ago, when EDN first began talking to Xilinx FPGA users, the frustration level was very high. Despite having a large array of blazingly fast internal logic elements at their disposal, engineers struggled to achieve designs that would run as fast as 12 MHz. Engineers also vociferously complained about the Xilinx autorouter, saying that they had to spend weeks, or even months, endlessly rerouting complex designs by hand with a manual routing editor.

What a difference time makes. Experienced designers now claim to regularly crank out designs having multiple Xilinx FPGAs that run at 70, or even 100, MHz. Further, they avow they never do any hand routing.

Old ways reappear

The story behind this dramatic change is not one of revolutionary breakthroughs. Rather it is the usual dreary tale of hard work, thorough experimentation, and attention to details that leads to gradual, incre-



This 50-MHz, UV-erasable FPGA, the ATV5000 from Amtel, has 128 flip-flops and 52 latches.

FPGA design methods

mental improvements. In short, engineering as usual. One older Xilinx-FPGA designer said that he regularly bests younger designers because he recycled the skills he had developed during the era of discrete logic and small-scale integration.

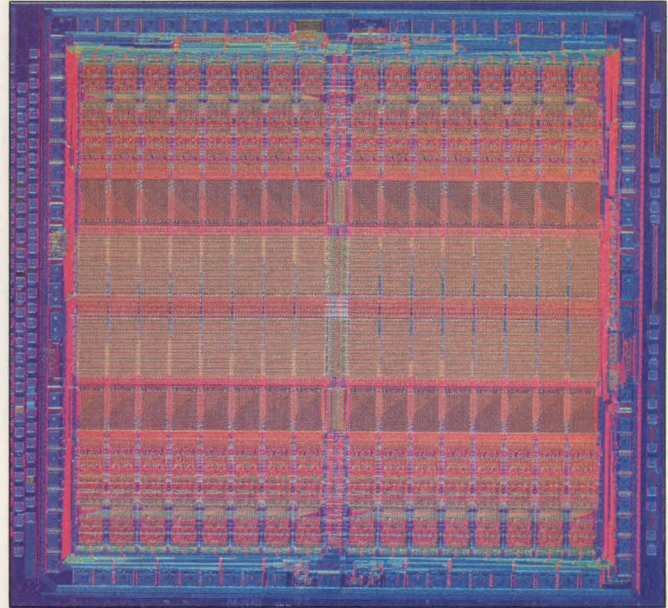
Attempts to roll over PAL-device techniques to Xilinx FPGAs meet with disaster. For example, one designer compiled a set of Boolean equations for a PAL-device state machine over a Xilinx FPGA. The state machine was a dismal failure. When the designer reoriented his thinking to align with the characteristics of the FPGA, a new, equivalent "hot-bit" state machine that suited the FPGA's architecture proved much more successful.

The methods that these experienced Xilinx designers have evolved differ significantly from the methods of PAL-device designers. Their FPGA methods begin with a suite of known-good design elements that have proven to compile into fast structures on a Xilinx FPGA. For example, a PAL-device designer can take advantage of a PAL-device's high fan-in and two-layer logic to implement big, high-speed counters. A Xilinx FPGA designer might employ a recirculating shift register to do the same job as a counter. Because a shift register is more serpentine (that is, low fan-in and a single layer of logic), it is a much better fit in a Xilinx FPGA than a counter is.

The next stage in their methodology involves draw-



Gate-array-like FPGAs such as the XC3090 from Xilinx typically have excellent I/O resources. This plastic-packaged, surface-device, 160-pin FPGA costs \$176.



The electrically erasable FPGA family from Lattice includes four in-circuit-programmable versions. The pLSI family's equivalent-gate counts range from 2000 to 8000.

ing a schematic of the design with some popular schematic-capture programs running on a personal computer. These designers use their intimate knowledge of the Xilinx autorouter to constrain the schematic so that the autorouter will produce the layout that they want.

A key difference between the Xilinx autorouter and the fitters for FPGAs that have a sum-of-products architecture is that the Xilinx autorouter is not deterministic. Every time you run a given schematic through a sum-of-products FPGA's fitter, it will produce the same layout. Not so for the Xilinx autorouter. It is not a deterministic router. So some experienced users run multiple autoroutings in parallel.

One lucky Xilinx designer, who works for a large computer company in the Northeast, has a network of superminicomputers at his disposal. He frequently has several routings of the same design under way at once as background tasks on the networked computers. Another designer who works in a shop that uses IBM PCs exclusively, simply stays late. After his co-workers go home, he launches as many as 14 routings of the same design on the 14 IBM PCs in his shop. So instead of a jinni in a workstation, this designer has shoemaker's elves in the form IBM PCs.

These designers use the manual-routing editor only for viewing the results of their various autoroutings. Based on a scan of the results, they go back to their

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And Who's Leading It?

ZYCAD

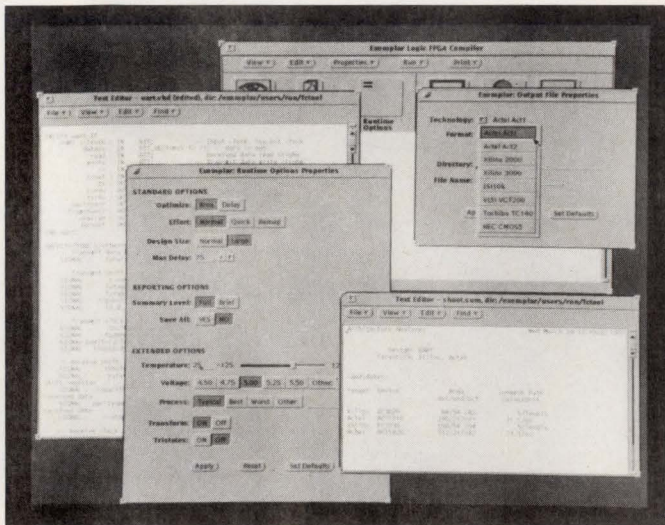
FPGA design methods

schematics and revise the constraints, resubmitting the revised schematic to the autorouter. Note that less advanced Xilinx designers emphatically state that they absolutely must hand-route a few critical paths with the manual-routing editor before turning the autorouter loose.

PAL-device techniques persist

Not all FPGAs have an architecture as unstructured and uncommitted as Xilinx's. The heart of FPGAs, such as those from Altera, AMD, Atmel, and Lattice, is still the canonical sum-of-products architecture. These FPGAs are not only bigger than their PAL-device forebears, they are also more complex. They sport a variety of ingenious schemes to ameliorate the rigidity of PAL devices. For example, they have structures that allow designers to share product terms among I/O cells or add extra product terms to an I/O cell. Designers can program these devices' output cells to function as many different kinds of flip flops and logic gates. In addition, uncommitted, buried registers let designers implement finite-state machines without sacrificing I/O registers.

Still, like PAL-devices, much of these devices' internal connections are fixed. Consequently, the fitter, or device compiler, has an easier job simply because it has fewer decisions to make. Thus each design iteration compiles much faster for these devices than do Xilinx autoroutings. Note that devising a fitter for a sum-of-products FPGA is not a trivial task. The logic minimiz-



You can compare the different implementations' speed and power consumption when you use Exemplar's Release 1.0 third-party FPGA software to compile your design over a variety of FPGAs.



Commonly, new FPGAs get their first software support from the device maker, such as the Opal software for National Semiconductor's MAPL FPGAs.

ers for PAL devices use public-domain algorithms. No such algorithms exist for sum-of-products FPGAs.

Despite the availability of integrated, high-powered software, designers are largely sticking with PAL-device design-entry methods and software that runs on personal computers (one respondent uses Logical Devices's CUPL on a MAC; all other personal-computer users interviewed employ IBM PCs). Most use either schematic capture or Boolean equations to specify their designs. A few use truth tables or finite-state-machine formats, with only one designer expressing a preference for multiple, linked state machines. Exotic hardware-description languages such as VHDL (VHSIC Hardware Description Language) have not lured experienced PAL-device designers away from their familiar tools.

The flexibility of the sum-of-products FPGAs definitely pays off. Those using Boolean equations find that they have to spend less time torturing their equations to make them fit than they did back when they were designing with PAL devices. Further, some find that after they became familiar with their FPGAs they can use clever tricks to put to work internal logic that would have gone unused in a less-flexible PAL device.

Designers also express a preference for selecting their own chips and partitioning their designs over multiple chips manually.

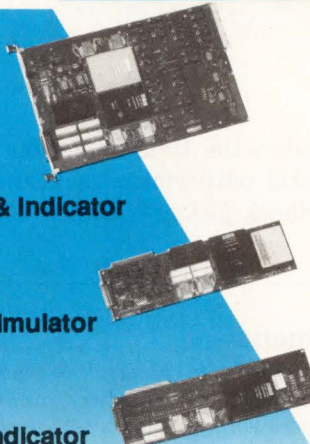
Few simulate their designs either at the chip level or the board level, preferring to go straight to prototypes. Those that do simulate, tend to use the simple

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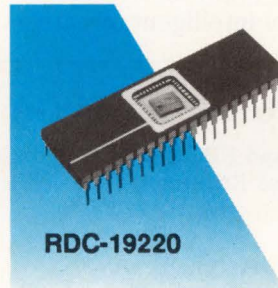
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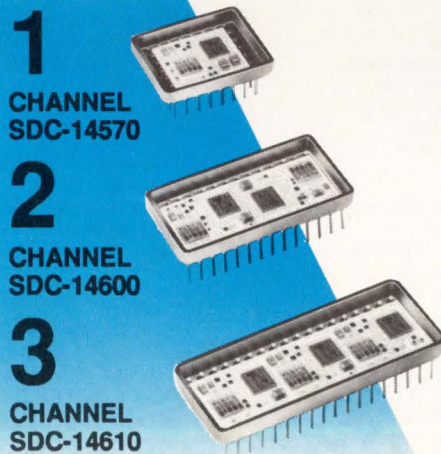
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FPGA design methods

simulators that come with their schematic-capture packages or simulators that run on personal computers, rather than simulators from the FPGA vendors or simulators that run on workstations.

The "foreseeable future" is an oxymoron. No one can predict the future, near or far. Assuming that the practices of the pioneers of a new technology will be the same as the practices of those who follow on when the new technology becomes widespread is also dangerous. But FPGAs just make too much sense for too many good reasons to be ignored. Thus, a taste of how some engineers work with FPGAs can provide some useful insight. Perhaps the most important lesson to be learned, is that once again, the intelligent, creative

engineer who takes the time to master his tools and materials will still outperform the handbook jockey, even if the handbook jockey is armed with magic software.

EDN

Acknowledgment

EDN and the author wish to thank all of the engineers who cooperated with our survey by speaking frankly and for sharing their experiences with the engineering community.

Article Interest Quotient (Circle One)
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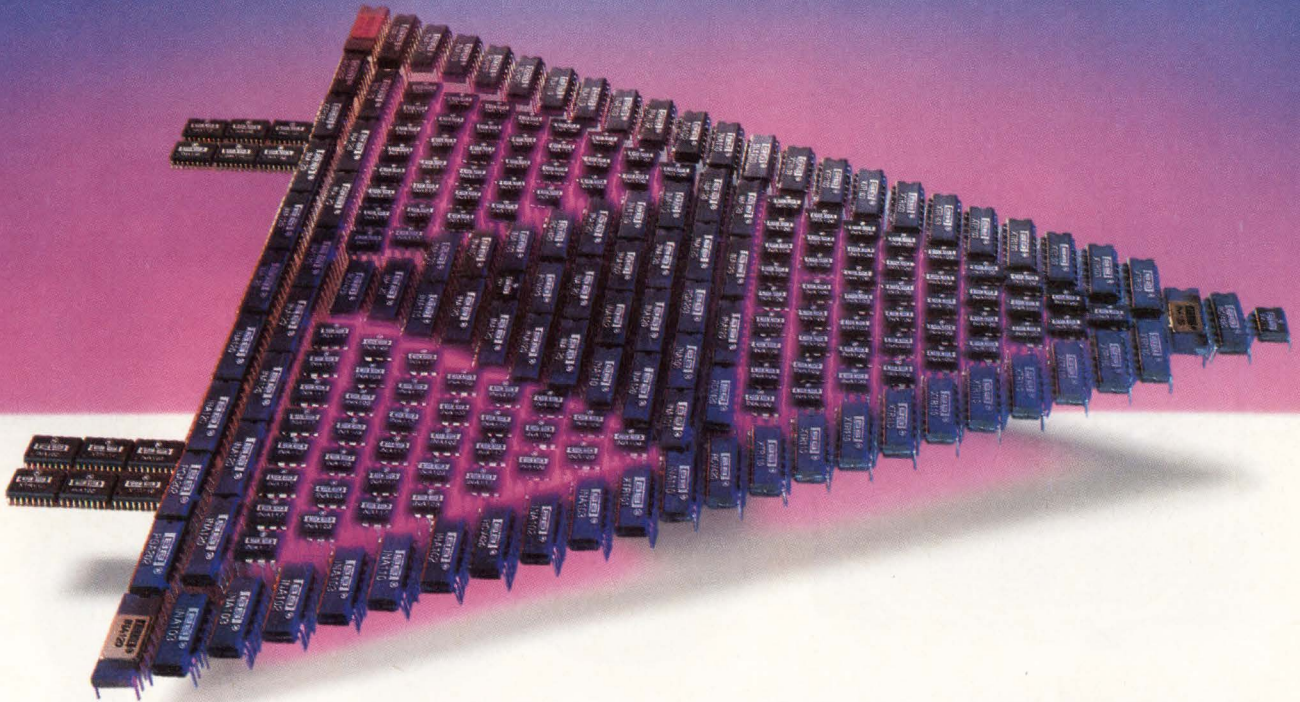
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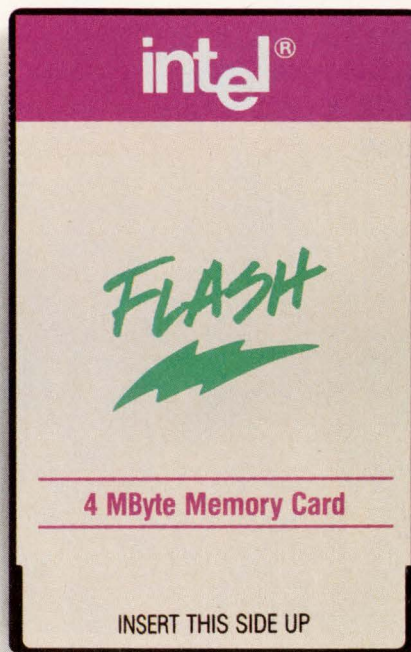
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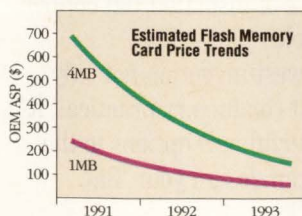
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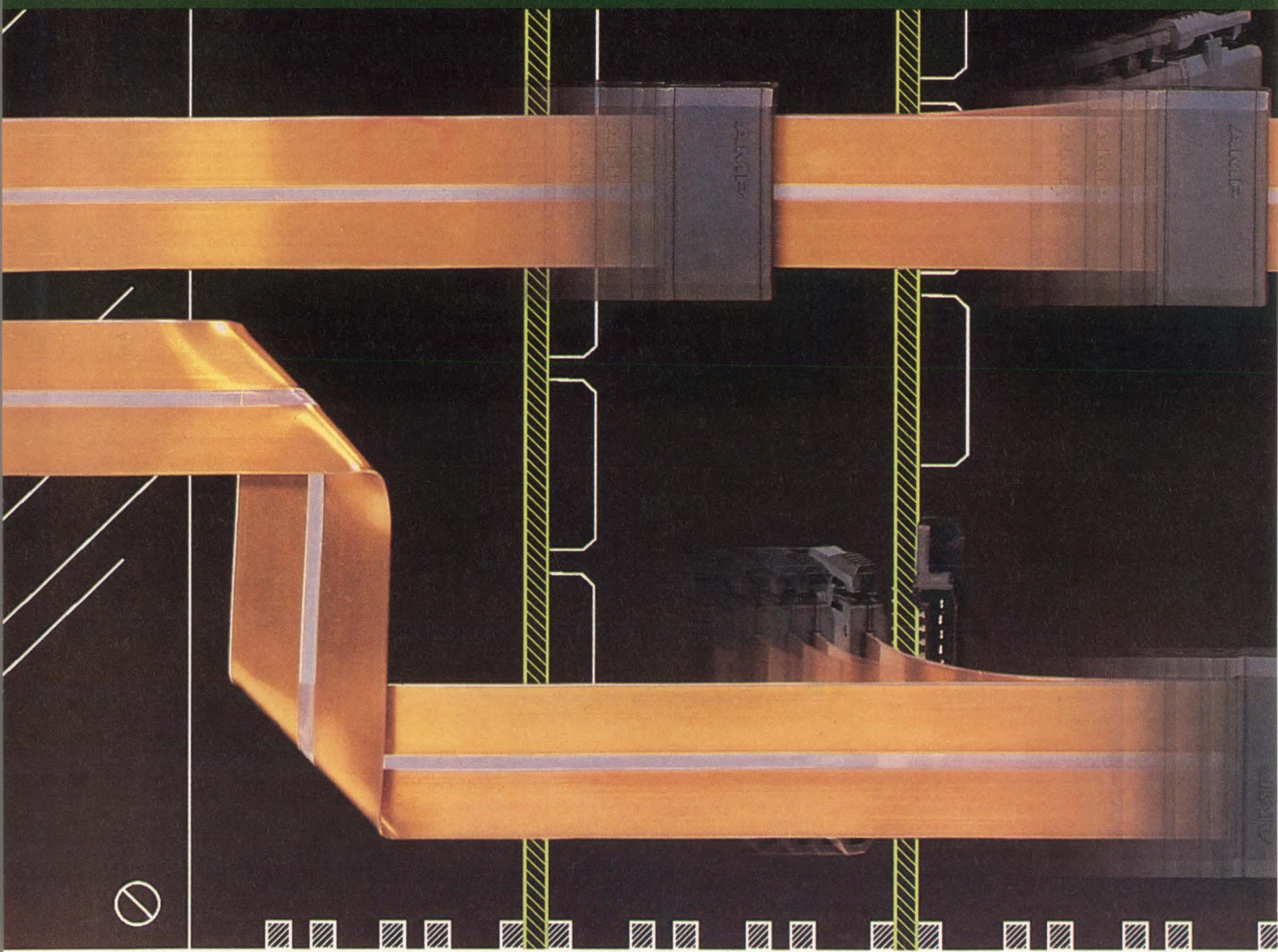
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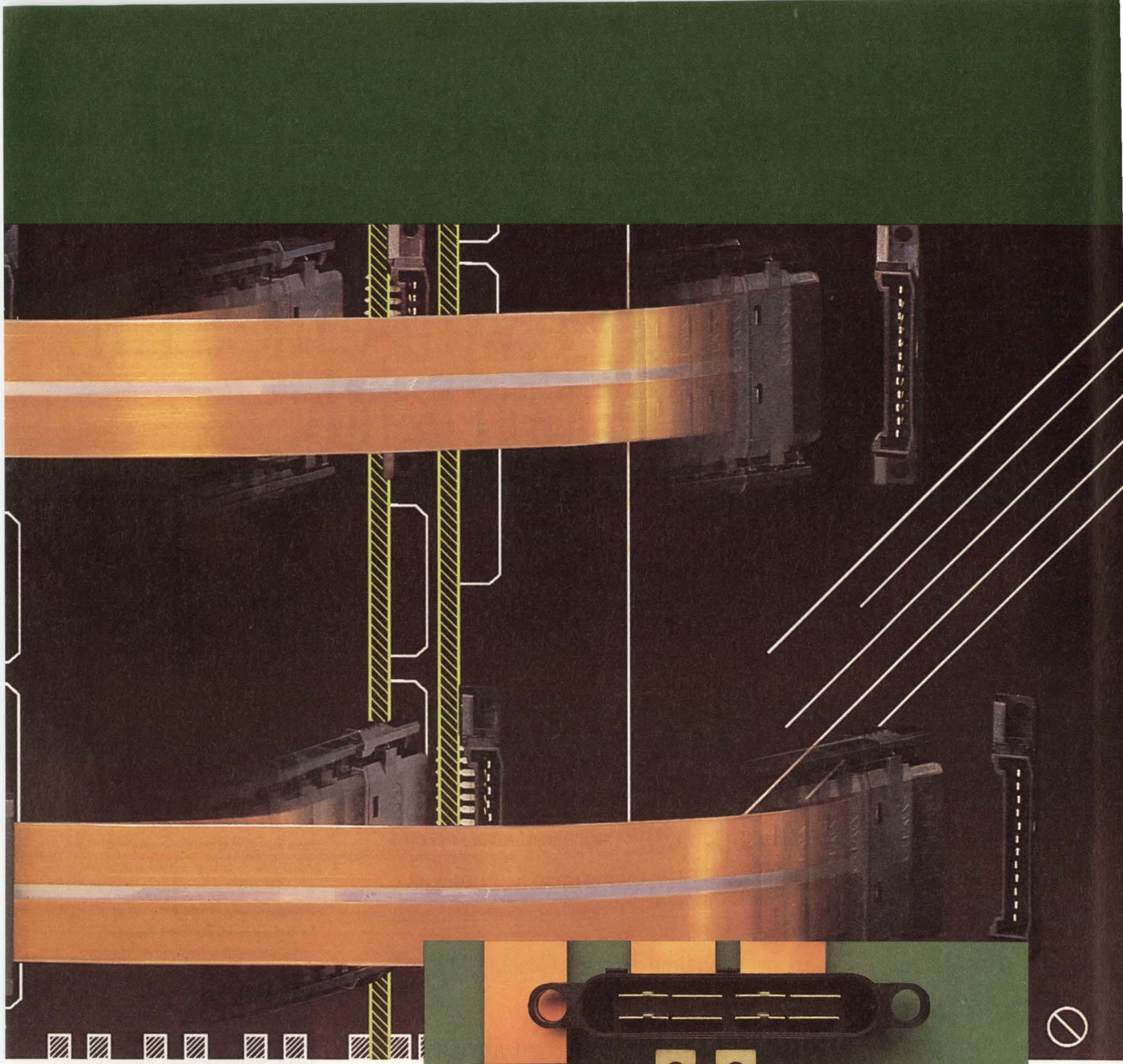


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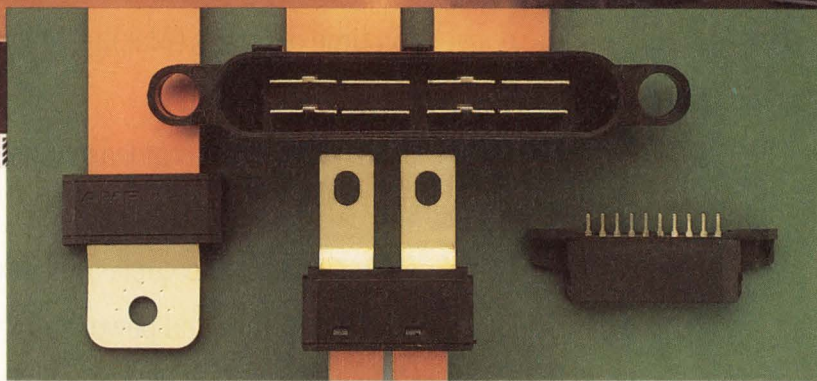
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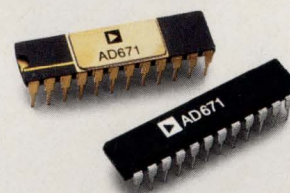
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 **ANALOG
DEVICES**

Know your options and requirements when designing filters

Designing a filter can be an overwhelming task. You can configure lowpass, highpass, bandpass, and notch filters in several ways, each of which has unique characteristics. Knowing the performance characteristics of different filter configurations will help you specify the best filter for your application.

William Chambers,
Acquisition & Control Electronics

Filters range from small but omnipresent parasitic impedances to computer systems running signal-processing programs. Lowpass, highpass, bandpass, and notch filters can be configured as Bessel, Butterworth, Chebyshev, and elliptic types. Choosing a configuration is only the first step. You must also decide between active and passive filters, between discrete-time vs continuous-time sampling, the number of filter stages you'll need, and how to achieve the accuracy you need. This article focuses on designing filters that work at frequencies ranging to 10 MHz.

Filters are found in many applications. Perhaps the most common application is using a bandpass filter to improve signal quality (see **box**, "Sorting out terminology," for a glossary of filter terms). You'll greatly improve the signal-to-noise ratio (S/N ratio) by using a filter to reject extraneous frequencies. The cleaner signal will almost always give better results. In ex-

treme cases, noise can have a high enough amplitude to saturate system circuitry or waste an unacceptable amount of power. When the lost power radiates, it can cause electromagnetic-interference problems.

Because noise of any frequency can enter a system, the system's bandwidth should be as small as practical. The power of random noise is proportional to the bandwidth of the system input signals. Reducing the bandwidth 100 times reduces the noise power 100 times and the noise voltage 10 times. Radio-frequency energy is a notorious source of noise that may be well above the highest frequency of interest.

Tailoring a signal's frequency components is also a job for a filter. The human ear can hear frequencies of approximately 20 Hz to 20 kHz. But with noisy signals, it's usually best to attenuate the high-frequency response. Recording methods such as Dolby emphasize a signal's high frequencies before recording so the signal can override hiss. At playback, a lowpass filter (often a tape player with an inferior frequency response) reduces high frequencies. The record-and-playback process yields a high S/N ratio while retaining a flat frequency response.

Feedback systems include a wide variety of filters to help improve, or compensate, system dynamics. Electronic systems have unavoidable high-frequency poles. These poles cause phase shift, which results in peaking or oscillation. Filters must reduce the loop gain before too much phase shift occurs. Even a simple op amp is a lowpass filter. General-purpose op amps have a single, dominant pole, which causes a long, slow roll-off beginning at less than 10 Hz.

Practical filters have limitations on their frequency responses.

Filters are also a key element of sampled data systems. Filters prevent aliasing by keeping system inputs below the Nyquist limit. The sampled output changes at the sampling rate in steps whose edges contain spurious high-frequency information. Filters can remove these edges; the reconstructed sine wave is smooth and includes only a fundamental frequency component.

To capture full information about an input, you must meet the Nyquist criterion, which states that your system must sample an input at a rate at least twice the input's bandwidth. Often the input's minimum frequency is very low, so its bandwidth is the same as its maximum frequency. Two samples per cycle, however, are enough only in theory. Filter limitations will make your system's usable bandwidth several times lower. Systems that produce a coarse visual display may require 10 sample points per cycle. Even if the 10 samples contain no noise, they can miss individual waveform peaks by as much as 0.314 rad, or $(1 - \cos 0.314) \cdot 100\% = 4.89\%$ of the peak value.

If an A/D converter runs at 200,000 samples/sec, then the converter's input must see no significant components above 100 kHz. The designer's choice of acceptable levels for these high-frequency signal components and the components' degradation of the desired signal

can have a large impact on system cost. If your budget is tight and the system's S/N ratio is relatively poor, you might have to use a filter with poles one decade away from the 100-kHz point, at 10 kHz (see **box**, "Mind your poles and zeros"). The filter will add phase and amplitude errors to any signals that approach 10 kHz. To avoid these errors, you need a faster A/D converter or a sharper filter response.

Consider using a simple Butterworth lowpass filter in this example. Suppose you can afford to cut the 10-kHz corner frequency by 3 dB. A 1-pole filter can then cut interference at 100 kHz by 20 dB, or 90%. A similar second-order filter can cut 100-kHz interference by 40 dB, or 99%.

The phase error also depends on a filter's number of singularities. The single pole shifts corner frequencies by $\pi/4$; two poles will cause a $\pi/2$ shift. The two filters have errors at $1/10$ the corner frequency of $\arctan(1/10) = 0.1$ rad (5.71°) and 0.142 rad (8.14°), respectively. Raising the poles' Q to sharpen the corner frequency makes the phase shift even worse.

When you're designing a filter circuit, you'll usually know what type of filter you need—lowpass, highpass, bandpass, or notch filter. To begin a design, you will need to decide on required accuracy, response sharpness, and filter configuration. These

Sorting out terminology

The following glossary defines some of the terminology you'll find in filter literature:

Aliasing—the generation of false frequency components caused by sampling an input below its Nyquist rate.

Allpass filter—a device that changes the phase of signals rather than their amplitude.

Bandpass filter—a device that passes only a certain range of frequencies. These filters are usually formed from lowpass and highpass filters if the resulting passband is at least as wide as the center frequency.

Bandstop filter—also called a notch filter, this device blocks a specific band of frequencies.

Continuous time—describes a normal analog signal—no sampling is involved.

Cutoff frequency—the frequency at the end of the passband.

Digital—describes a discrete-time system that can have only discrete values.

Discrete time—having values that are valid only at certain moments; sampled.

Highpass filter—a device that passes only high frequencies.

Lowpass filter—a device that passes only low frequencies.

Nyquist rate—a sampling rate equal to twice the bandwidth of an input. This rate may be seen as one sample per peak and one

per valley. Conversely, this rate limits the input to half the sample rate.

Order—the number of poles a circuit uses.

Passband—the band of frequencies that a filter must pass with little change. The user decides what tolerances to allow.

Q—the ratio of a filter's half-power bandwidth to peak frequency.

Skirt—the sharp change in filter output magnitude in the transition band.

Stopband—the band of frequencies that the filter should not pass.

Transition band—the frequencies between the passband and stopband.

factors will determine how you develop the filter.

In the previous ADC example, filter constraints reduced the usable bandwidth to less than 10% of the allowable input bandwidth. Practical filters have limitations on their frequency responses; they have passbands, transition bands, and stopbands (**Fig 1**). To change from a signal-passing to a signal-stopping mode, every filter requires a band of frequencies in which to make the transition. You need to make complex trade-offs among cost, the bands' frequency accuracy, passband fidelity, stopband depth, and phase accuracy.

Specify the passband and stopband to be as accurate as you need. No gains can exceed the system's reference point, which will usually be 0 dB. Extending the passband to the half-power point—a drop of -3 dB, or -29.3%—is traditional. However, you may decide to keep your transfer function's passband accurate to -0.10 dB, or -1.15%. Frequencies beyond this limit are considered cutoff. The term "cutoff" refers to all signals that the filter reduces more than the passband allows, not only to signals in the stopband. Your stopband requirement might be a 99% reduction in the transfer function (-40 dB). The transition band con-

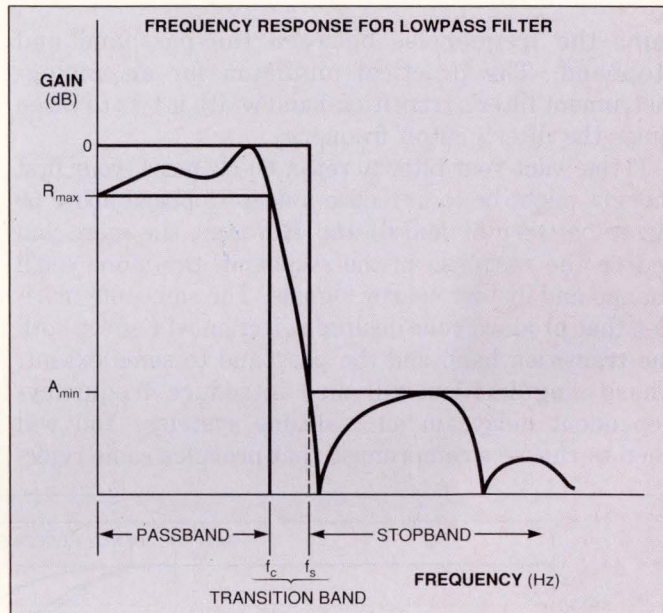


Fig 1—Infinite attenuation beyond the cutoff frequency, f_c , is the norm in an ideal filter. However, errors due to the passband ripple, R_{MAX} , and stopband attenuation, A_{MIN} , make attaining such performance in real-world filter designs impossible.

Mind your poles and zeros

A filter's order reflects the number of poles the filter includes. All filters require at least one pole; usually, the number of poles equals the number of circuit reactances. In continuous-time systems, certain values of the complex variable s define the location of singularities in the transfer function. Depict these poles and zeros on the complex number plane; put the input frequencies on the imaginary axis. You can then plot the transfer-function magnitude as a function of frequency on log-log coordinates.

Poles and zeros complement each other: Poles can increase a nearby signal component without limit; zeros can reduce the same signal component to zero. Unless canceled, each singularity introduces a slope of 1 in the transfer

function. This slope is negative for poles and positive for zeros, and starts at the frequency of the singularity. This slope value is the asymptote used in Bode plots and is not accurate near the frequencies of singularities. At high frequencies, each zero and pole also introduce a phase lead and phase delay, both of which are $\pi/2$. This delay is frequency dependent and distorts signals.

Single poles and zeros always occur on the real axis in the s plane. Each pole causes a 3-dB reduction from the Bode-plot levels at the pole's frequency. Pole pairs that are within $\pi/4$ rad of the real axis have a transfer function with no peaks. As the poles approach the imaginary axis, they produce peaks in the transfer function.

Q is a common measure of poles' lack of damping. A Q of 0.5 indicates critical damping—poles that are coincident on the real axis. Critical damping allows no ringing but gives a very slow roll-off. A Q of 0.707 makes the frequency response out to the corner frequency as flat as possible without peaking. High Q s create frequency-response peaks, which are useful in multistage filters and narrow bandpass filters. The Q of poles rises sharply as the poles approach the imaginary axis, where they would form an oscillator (that is, the poles would have infinite Q). The steep slope of Q makes the response of high- Q circuits very sensitive to component values and subject to drift.

Place damped, passive filter stages at the input. If all remaining stages receive the same input levels, place the stages in order of ascending Q.

tains the frequencies between the passband and stopband. The practical minimum for an analog-instrument filter's transition-band width is two to three times the filter's cutoff frequency.

If you want your filter to reject 60-Hz noise, your first thought might be to introduce a deep stopband above 59 Hz or between 59 and 61 Hz. However, the more you reduce the response in the stopband, the more you'll change and distort nearby signals. The same singularities that produce your desired rejection will affect both the transition band and the passband to some extent. These singularities will also introduce frequency-dependent delays in all real-time systems. You will need to choose a compromise that provides some rejection

at 60 Hz without unduly distorting your signal.

Several mathematical functions define filters that have reasonable performance tradeoffs. Each function's frequency response has a distinctive shape. Each filter type can have any order. Higher-order filters emphasize the characteristics of each function—both the desirable features and the problematic ones. The higher orders also incur the longest signal delays. The filters with the sharpest roll-off, Chebyshev and elliptic filters, have the longest delays. The filters achieve sharpness by allowing ripple in the passband (or both the passband and stopband). Chebyshev and elliptic filters are also the most complex and most sensitive to component variation (Figs 2 and 3). The following filter

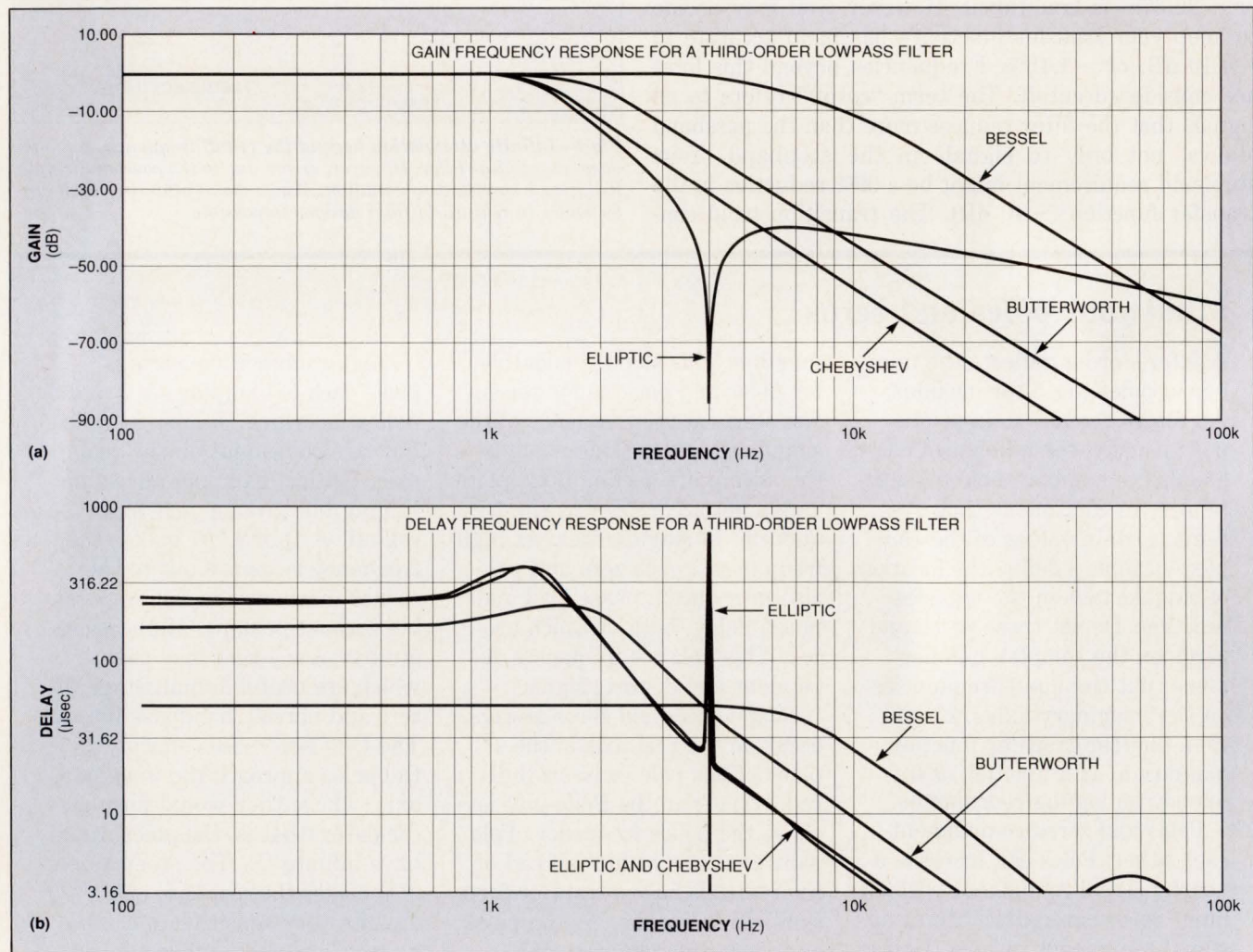


Fig 2—Variation in roll-off slope is a key difference in the gain response of the various filter configurations (a). The transfer functions are for analog, third-order lowpass filters that are accurate to approximately 1% (0.1 dB) in the passband. Delay curves illustrate that real-world filters are far from ideal—delay would be constant in the ideal case (b).

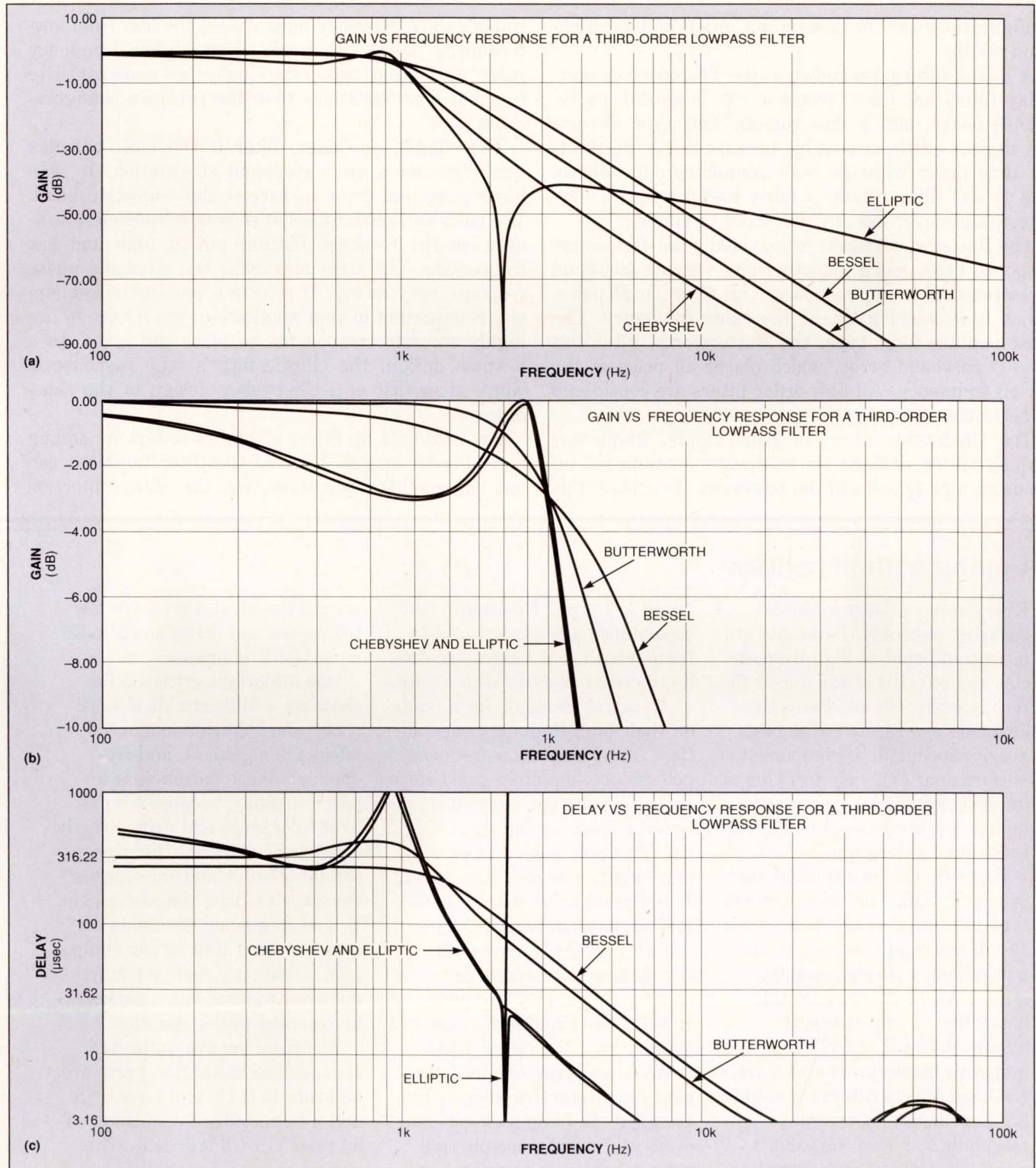


Fig 3—By relaxing the passband accuracy to 3 dB, you dramatically increase the roll-off slope of the filter gain curves (a). However, this increase in roll-off slope comes at the expense of an increase in passband error (b) and a degradation in delay variation (c).

The passive RC filter cannot provide power gain, and the filter has complex-value input and output impedances.

configurations are in descending order of transition-band width:

A Bessel filter (also known as the Thompson or best-delay filter) has linear phase in the passband, no response peaks, and a slow roll-off. This type distorts the signal as little as possible because it has the shortest time delay with the least frequency dependence. The Bessel filter retains a fairly useful frequency response and never has any overshoot or ringing.

The Butterworth filter, or maximally flat-frequency-response type, has a monotonically varying passband and a reasonable step response. This filter has all poles, which have varying Q s, at the same frequency. The most popular filter type, the Butterworth, often has a 3-dB passband error, which places all poles at the cut-off frequency. All first-order filters are considered to be Butterworth filters.

The Chebyshev filter, or equal-ripple, frequency-response filter, achieves the sharpest monotonic roll-off by using high- Q poles in the passband. To achieve this

roll-off, the Chebyshev must cancel the loss from low-frequency poles with peaks from higher frequency poles. This design makes the Chebyshev more sensitive to component variations than the previous configurations.

The elliptic, or Cauer, filter is the most complex filter type for a given stopband attenuation. It combines poles and zeros to narrow the transition band. The poles and zeros cancel at remote frequencies, however, so the response flattens out at high and low frequencies. The zeros also make the stopband phase response very messy. If rejecting particular frequencies is important in your application, you'll have to use highly accurate components to place the zeros. In a lowpass design, the elliptic filter's step response is worse than that of a Chebyshev design of the same order.

You can build up filters of higher orders by adding second-order stages. Each of the filter functions can use one amplifier per stage, but the elliptic function

Coping with parasitics

Every component introduces parasitic elements. Parasitics are most significant at high frequencies and effectively add messy filters to every circuit. Parasitic elements are rarely (or at best, poorly) specified, so component performance can vary from lot to lot. This situation makes canceling out parasitics or allowing for them during design quite difficult.

Parasitic values are often surprisingly high. The most common type of printed-circuit board uses 10-mil traces of 1-oz copper and a 0.0625-in. epoxy/glass substrate. An 11-in. trace on this board has an impedance of $0.50\Omega + 0.46 \mu\text{H}$. At 175 kHz, the inductive reactance is also 0.5Ω . Leakage effects can cause shunting impedances of several megohms to a long adjacent trace. The trace's capacitance to a plane on the other side of the

board is 1.9 pF. Resistance and capacitance are proportional to trace length, but inductance does not increase linearly with length.

All active elements have limits on their high-frequency capabilities. An op amp's low-frequency pole reduces amplifier gain before parasitic poles can excessively affect the phase of the output signal. This pole is also an example of a loosely specified parameter. A $100\times$ amplifier using a general-purpose op amp will have -3-dB and $-\pi/4$ errors where the op amp's open-loop gain falls to 100—roughly at a frequency of 10 kHz. The amplifier's phase will already be -0.1 rad at 1 kHz.

When analyzing circuits, you usually assume that components are ideal. To build a circuit, however, you have to use physical components with complex behaviors. High-quality parts do ap-

proach the ideal; they have low tolerances and drifts and almost no parasitic elements.

One important criterion for choosing a filter circuit is sensitivity—how do component values affect filter gain, Q , and frequency? These parameters impact reliability because component tolerances and drift directly affect performance. The higher the filter order and the sharper the filter's skirts, the worse gain, Q , and frequency problems become. Even a shift in one component value may change the frequency response into a series of unexpected peaks and dips.

Resistors behave quite well. Inexpensive metal-film parts are accurate to 0.1% and have drift and a temperature coefficient of 50 ppm/ $^{\circ}\text{C}$ with low drift. This part is cheaper than most capacitors. Much better parts are also

should have more. Odd-order configurations also require one first-order stage. Every stage will be different, if only in its Q. You can find the necessary pole and zero locations for a desired response in filter-design tables. Each order has only one Bessel shape and one Butterworth shape. There are many more Chebyshev frequency-response shapes, and the elliptic design tables are very complex. Each combination of order, shape, and passband and stopband errors requires a separate table entry. You may have to interpolate to achieve a particular parameter value.

Filters that have sharp skirts always require high-Q stages. These filters are troublesome because they require small, slow inputs and tight component tolerances. Step changes at the input can cause ringing, saturation, and distortion. Using several amplifiers per stage can reduce component-tolerance problems.

You can prevent ringing by filtering the input before it reaches high-Q stages. Place any damped, passive stages at the input. If all remaining stages receive the

same input levels, place the stages in order of ascending Q. However, if you have an active stage with a Q less than but close to 0.707, it should be the first active stage. A filter stage that has a Q of 0.707 will be the most effective one with no peaking and almost no ringing. This sequence of stage orders is the best way to avoid saturation.

Passive networks offer simple solutions

An RC network using either discrete or distributed components is by far the least expensive filter available (see **box**, "Coping with parasitics"). An RC network introduces no overshoot and the least noise possible and will work at any frequency. The input to the network need only stay within the resistor and capacitor power-dissipation and breakdown-voltage limits. The simplicity of the RC network makes its behavior much more predictable for variations in frequency, temperature, or time than that of other filters.

The passive RC filter cannot provide power gain,

available. The values of commonly stocked metal-film resistors range from 10 Ω to 1 M Ω , with a value every 2 or 3%. You can adjust potentiometers over a wider range, and these parts allow easy circuit trimming and tuning. Carbon-film resistors are acceptable only for less critical applications because they introduce more noise and have higher tolerances than other resistor types. The temperature coefficients of carbon-film resistors often reach 500 ppm/ $^{\circ}$ C.

Spend extra money on accurate resistors if these parts will let you relax capacitor requirements. An inexpensive resistor is superior to any capacitor you would want to buy. Capacitors have many problem characteristics, some of which vary with temperature and frequency. Initial tolerances of 10% and more are normal. Dielec-

tric absorption, leakage, equivalent series resistance, and inductance all are potential capacitor problems.

Electrolytic and high-K ceramic capacitors are space efficient but experience serious drift and voltage-coefficient problems. Electrolytics have problems with aging, polarity, and internal heating at high currents. Solid tantalum capacitors have better leakage, drift, and temperature characteristics than aluminum electrolytics.

Accurate filters require NP0 (low-K or COG) ceramic or film capacitors. Still, pay close attention to capacitor specifications. Check the actual impedance at all input frequencies. NP0 ceramic parts function well at 100 Hz to beyond 1 MHz, and they also have the lowest temperature coefficient. At 100 kHz, NP0 and

good film capacitors may have a 1% error. At low frequencies, lower dielectric absorption makes plastic film a better choice. Teflon is the best plastic film, but it makes large and costly capacitors. Polystyrene is nearly as good as Teflon for temperatures as high as 70 $^{\circ}$ C.

Inductors have fallen out of favor for low-frequency filter designs in which a capacitor-amplifier combination can replace the part. Inductors can pick up hum and noise and are lossy and often heavy. Magnetic cores make inductance a function of temperature, frequency, and dc current. Inductors the size of a resistor have high series resistance and low current capacity. Beyond their current-capacity limit, inductors may begin to saturate and allow destructive current flows.

Active filters can provide both voltage and current gain, and their low output impedance eliminates stage interaction.

and the filter has complex-value input and output impedances. These impedances interact unless the driving impedance is very low and the load impedance is very high. You can cascade several RC stages, but the computations for predicting the filter's behavior are complex unless each stage has a much higher impedance than the previous one. All the poles will have very low Qs as a result of resistor power losses. An RC network cannot provide a sharp filter response, and the network will have disproportionate delay errors. An LC network can provide high-Q poles but introduces all the problems associated with inductors.

Active networks feature high Q

Active filters can provide high-Q poles without the use of inductors. Excluding the power requirements, a second-order active filter can be as simple as a surface-mount transistor and four passive parts. In addition, active filters can provide both voltage and current gain, and their low output impedance eliminates stage interaction.

You can meet low-Q, low-gain needs with an active filter that has one amplifier per second-order stage. For higher-Q applications, this circuit becomes much too sensitive to component changes. Circuits that use more than one op amp per stage have much better

sensitivity performance. Multi-amplifier stages are useful for elliptic filters, and they make high-Q circuits practical.

However, amplifiers add problems. The devices require power supplies, and the amplifier output cannot swing outside the supply rails. Amplifiers may give inverted results for input excursions approaching the rails and sustain damage for wider excursions. Amplifiers add noise, especially at low frequencies; at high frequencies, they cause distortion and couple in noise from the supplies. As op-amp manufacturers introduce general-purpose parts with smaller errors, input offsets and bias levels will no longer be major problems.

The advantages of active filters over inductors diminish with frequency—smaller inductances become more useful at high frequencies. To keep errors to a minimum, active filters need an excess gain. The loop transmission (open-loop gain of the amplifier and feedback network) should be at least 50 at critical frequencies, especially at poles and zeros. This loop-transmission requirement means that the amplifier's open-loop gain should be at least 50 times the gain of a noninverting circuit or 100 times the gain of an inverting circuit. Many circuits feature unity voltage gain, which lets you employ buffer stages. These circuits work well at

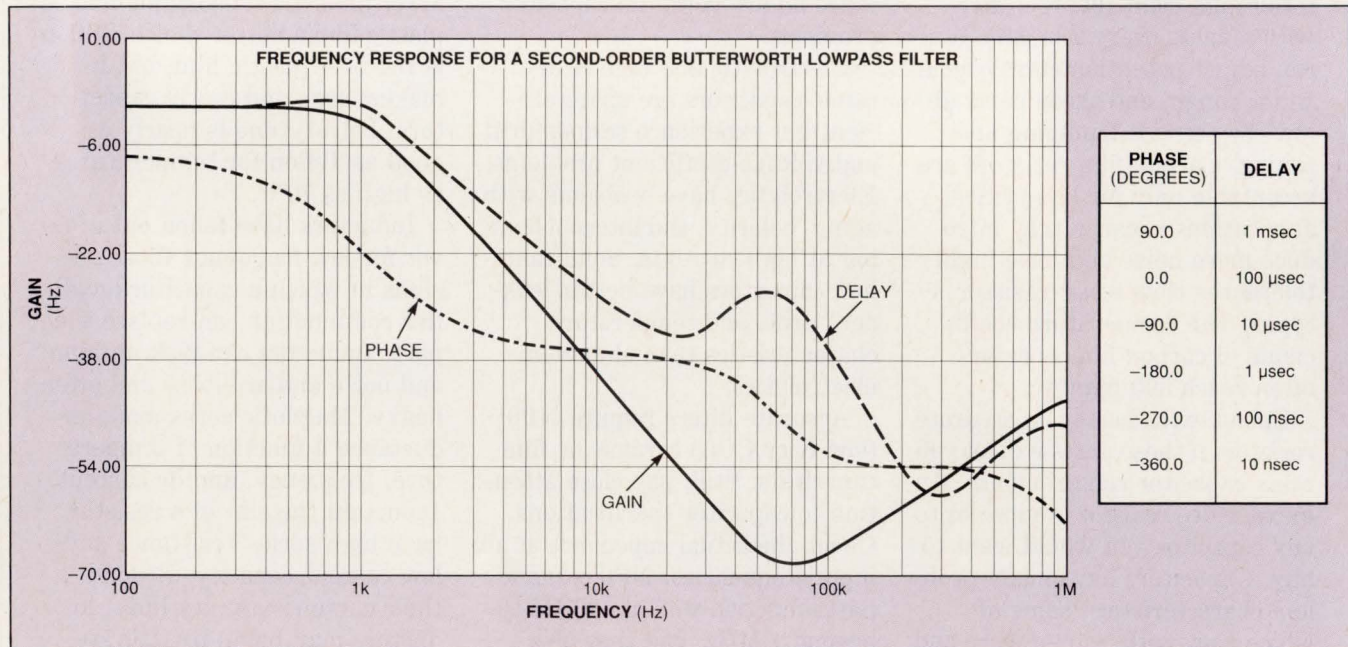


Fig 4—Op-amp problems are quite evident when you extend the frequency range of this lowpass second-order Butterworth filter to 1 MHz. Note that the phase should never fall below -180° . The stopband gain does remain below -40 dB and would be lower for a filter of any other order.

frequencies as high as 1/50 of the buffer's corner frequency.

If only the filter's response magnitude is important, 20-dB loop transmissions may be sufficient. At low gains, the filter response will deviate noticeably from the mathematical prediction. Also, as gain decreases, the power-supply and common-mode rejection ratios decrease and distortion increases. Response in a stopband may remain acceptably low if you use only a 20-dB loop transmission (Figs 4 and 5). Be sure to measure your filter's behavior at the highest frequencies the circuit may encounter. Fast transients will often pass through passive components to the output before the op amp has a chance to respond.

A multiple-feedback bandpass circuit requires a large gain. Even with a moderate Q of 5, the circuit's peak gain is 50. This high gain suggests the need for an op amp that has a gain of at least 500 to 2500 at the filter's peak frequency. An open-loop gain of 600 actually lowers the peak frequency by 1% and raises Q the same amount.

In this bandpass circuit, always try to use capacitors and resistors with a much lower impedance than the amplifier's equivalent input components. If you use high-value resistors, check how high the op amp's current noise is. Also, be sure that the resistances don't combine with the op amp's input capacitance to form

poles in the frequency range of interest. The passive components' values only need to be high enough to prevent loading down the op amp's output. Dedicated, continuous-time active-filter ICs are available that include very accurate capacitors. These ICs are moderately expensive but are useful in low-frequency, high- Q circuits.

Discrete-time systems use only samples of the input, and the rate at which they can obtain accurate samples severely limits their speed in real-time systems. The switched-capacitor filter is one example of a discrete-time system. Another example is digital signal processing, wherein digital computations produce a filter response. Both filter types produce accurate and stable frequency responses (largely determined by clock frequency), and both will tune over a wide frequency range under clock control.

In discrete-time systems, the clock must have a stable frequency and low jitter. A crystal clock may be necessary to maintain accuracy. The sampling clock rate must exceed the input bandwidth, and the filter must remove any aliased frequency components. Meeting these conditions is relatively easy for high-order filters and filters whose system clock rate is many times the cut-off frequency.

Although you should use the z transform to represent sampled systems, you can often model sampled

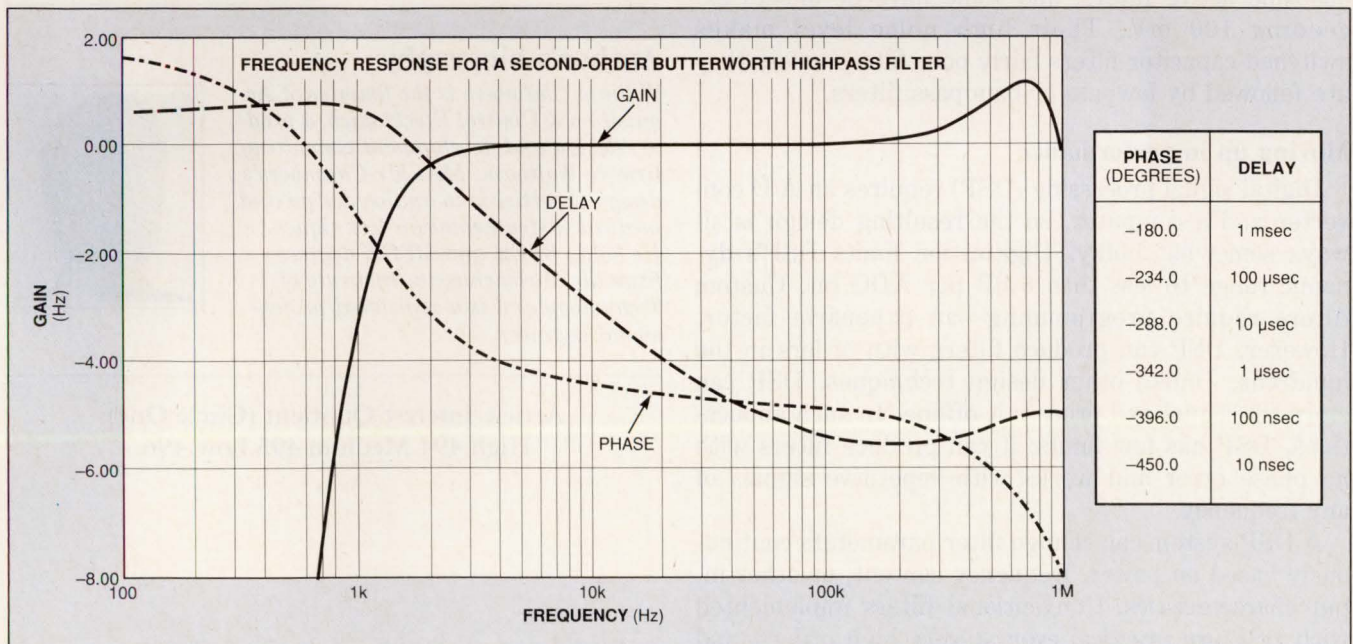


Fig 5—You'll also run into op-amp problems in highpass filters. The gain exceeds 1 at 7 kHz but remains within 0.1 dB of ideal at frequencies as high as 170 kHz. The phase should remain between -180 and -360° .

Digital signal processing has few limits; it can produce filters with no phase error and works with repetitive signals of any frequency.

systems as continuous-time systems. This modeling is a good approximation as long as the system's sampling rate is high compared with the input bandwidth. However, the continuous-system approximation will begin to break down for high input frequencies.

Switched-capacitor filters can use extremely small capacitors because the filters sample the input. They also typically operate at clock rates 50 or 100 times the corner frequency. Switched-capacitor filter ICs include several complete integrators on the die. These integrators form the basis of stable, high-Q filter circuits. The integrators can replace second-order stages that would require three op amps. The internal capacitors on the ICs also eliminate the worst component-tolerance and drift problems. Most chips are at least fourth-order (four integrators), and eighth-order chips are not uncommon.

General-purpose switched-capacitor ICs let you complete a filter design with precision resistors that determine filter characteristics. Some filter ICs are programmable—either digitally or by pin strapping. Other ICs are preconfigured and are available in 8-pin DIPs. Switched-capacitor filters introduce sampling and clock-feedthrough problems. They are noisier and introduce more harmonic signal distortion than continuous-time active filters, and some have dc offsets exceeding 100 mV. Their high noise level makes switched-capacitor filters fairly poor filters unless they are followed by lowpass or bandpass filters.

Moving up in performance

Digital signal processing (DSP) requires an A/D converter and a computer, so the resulting design is always somewhat bulky. Digitization limits DSP's dynamic range to less than 6 dB per ADC bit. Custom filters require programming—an expensive factor. However, DSP can produce filters with orders in the hundreds. Unlike other design techniques, DSP can store the signal and process it offline. In such applications, DSP has few limits; it can produce filters with no phase error and works with repetitive signals of any frequency.

A DSP system can change filter parameters continuously based on power, frequency content, or other input characteristics. Conventional filters implemented with DSP are practical even at very high orders, and linear-phase filters are common. Since the input signal need no longer be a function of time, DSP cut-off fre-

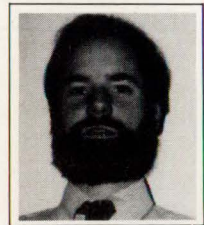
quencies can be as low as zero. DSP can run any filter both forwards and backwards in time, thus canceling the filter's normal phase errors. DSP can also handle signals that exist in several dimensions.

The front end of a DSP system must digitize an analog input. This operation introduces both sampling-rate problems and digitizing errors. Computations add even more error, especially if they use recursive algorithms. If the input is periodic and output delay is permissible, sampling successive cycles of the input can yield equivalent sampling rates in the gigahertz range. However, to process an audio input, you'll need a real-time system that has a wide dynamic range.

A 100-kHz A/D converter can sample signals as high as 35 kHz. This process requires two analog filters with steep skirts—one to prevent input aliasing and one to smooth the output. These filters will introduce severe phase distortion that the digital filter cannot fully correct. An easy fix for this problem is to specify a lower-frequency cutoff—the lower frequency will relax the filter requirements. Alternatively, the DSP system can interpolate extra data points. This choice requires more DSP time and a faster DAC, but also relaxes filter requirements. In addition, D/A converters are faster and cheaper than A/D converters. **EDN**

Author's biography

William Chambers is the founder of Acquisition & Control Electronics, a product design and development consulting firm in Waltham, MA. Mr Chambers's design expertise is in analog design and medical instrumentation techniques. He holds BSEE and MSEE degrees from the Massachusetts Institute of Technology and is a registered professional engineer.



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Telecommunications and Networks Group
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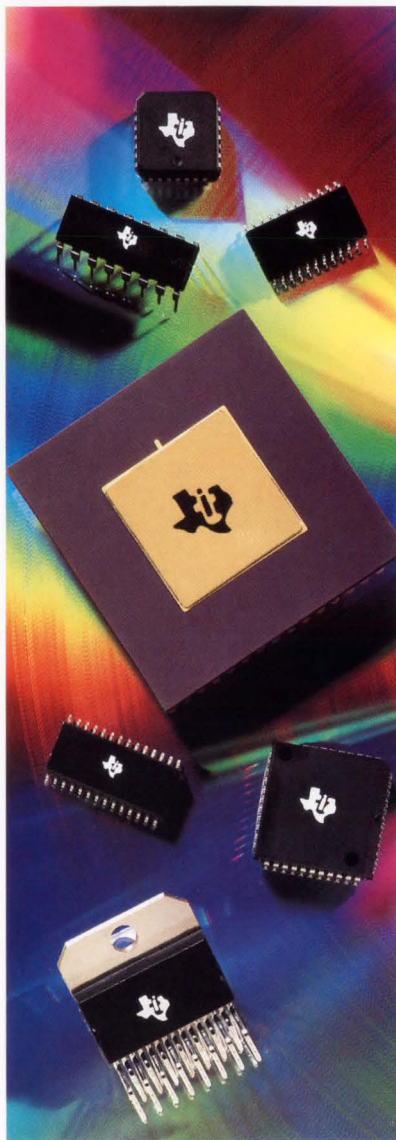
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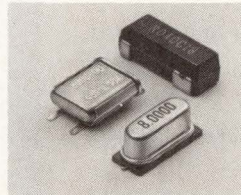
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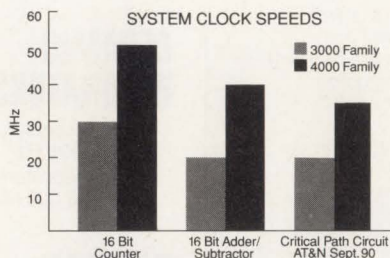
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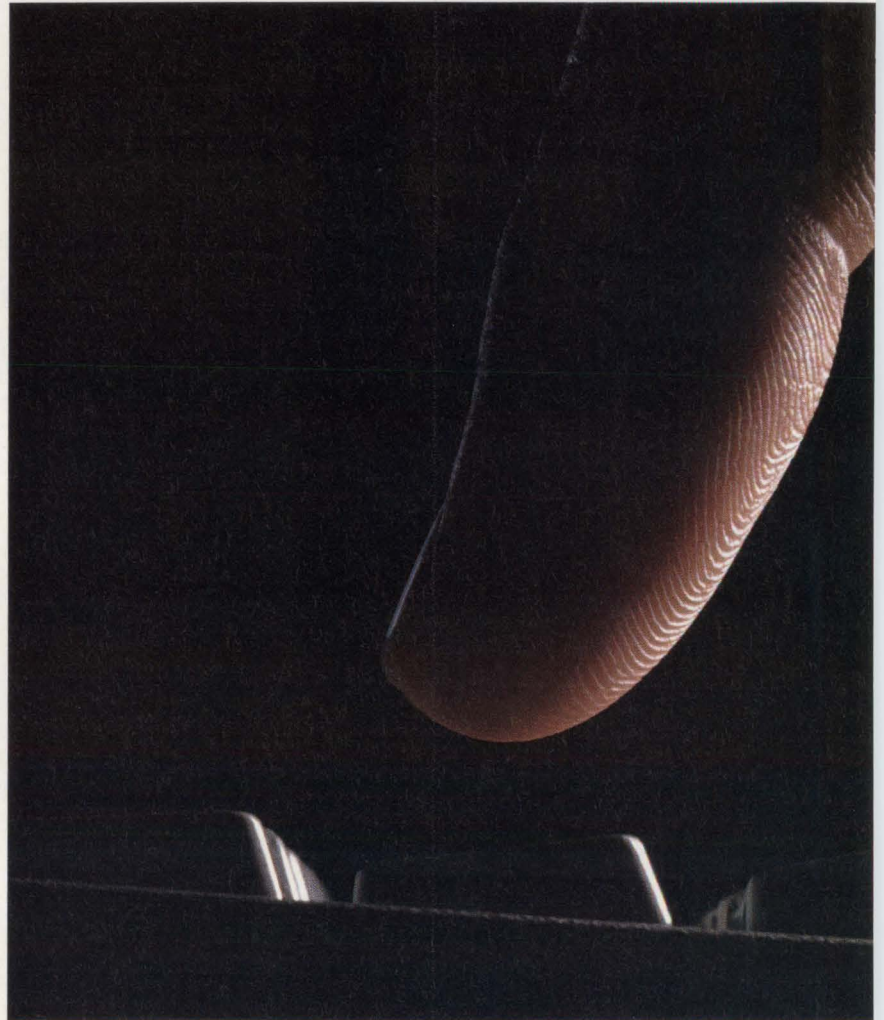


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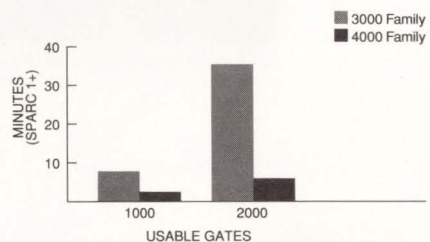


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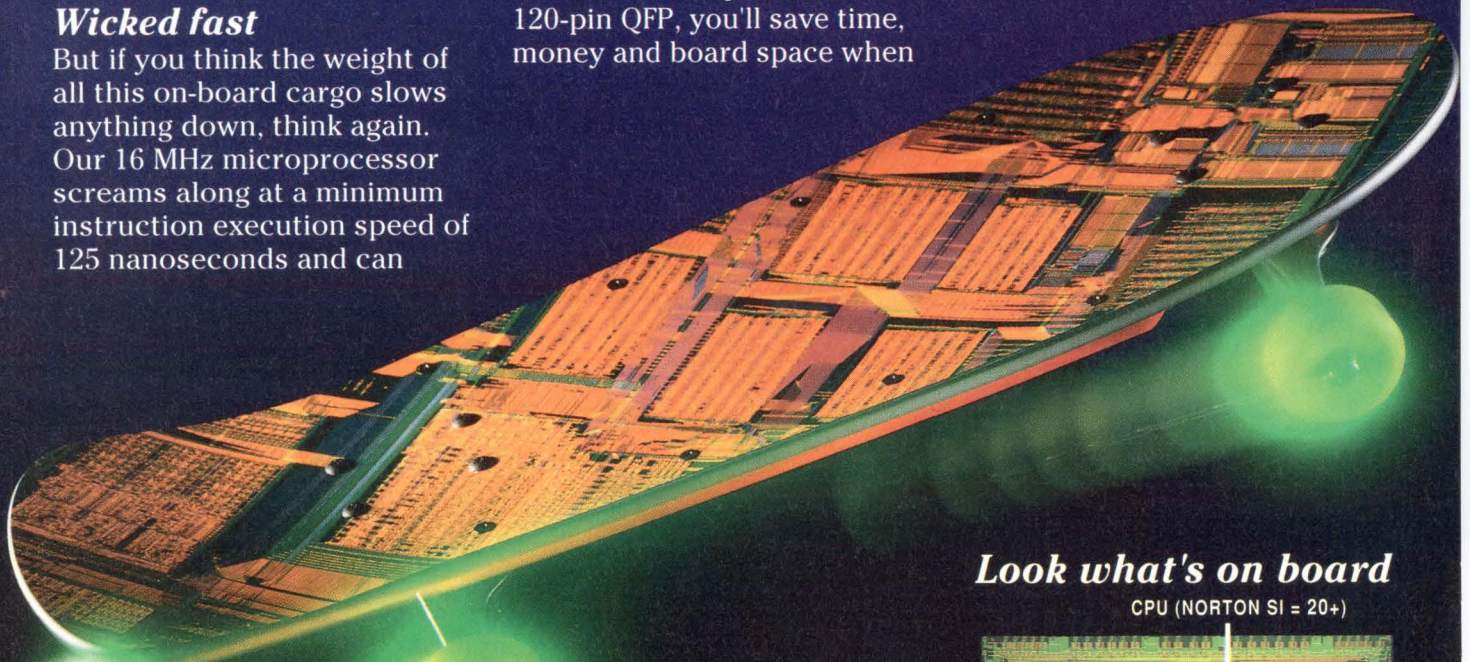
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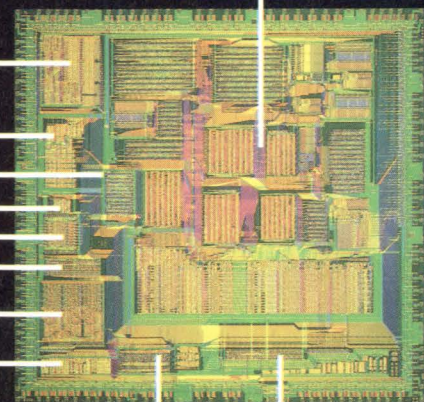
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Determine PLD metastability to derive ample MTBFs

As system speeds increase and more systems use asynchronous input sources, metastability becomes increasingly important. Because you can't eliminate metastability, you have to determine an appropriate MTBF for metastability-induced failures and use design techniques that limit the extent of these failures.

Sean Dingman, Cypress Semiconductor

Determining the metastability characteristics of logic devices, particularly PLDs, is an ongoing challenge. Because there is no standard metastability test method, manufacturers do not provide metastability specs on data sheets. You can use the procedures that follow, however, to measure the metastability characteristics of actual PLDs and calculate the additional resolution time you must factor into your designs' time budgets to achieve acceptable metastability MTBFs. Beyond using equations and implementing procedures, you can also build and equip a metastability test fixture.

Characterizing metastability

Many authors have reported experimenting on circuits to predict the likelihood of metastability for devices. Their testing theories and apparatus fall into three classifications:

1. *Intermediate voltage sensors:* Two voltage-compara-

tors are used to determine if the output voltage of a register lies between two given voltages (Fig 1a).

2. *Output proximity sensor:* The sensor determines whether the Q and Q# outputs have voltages that are about the same (indicating that the device was metastable) (Fig 1b).

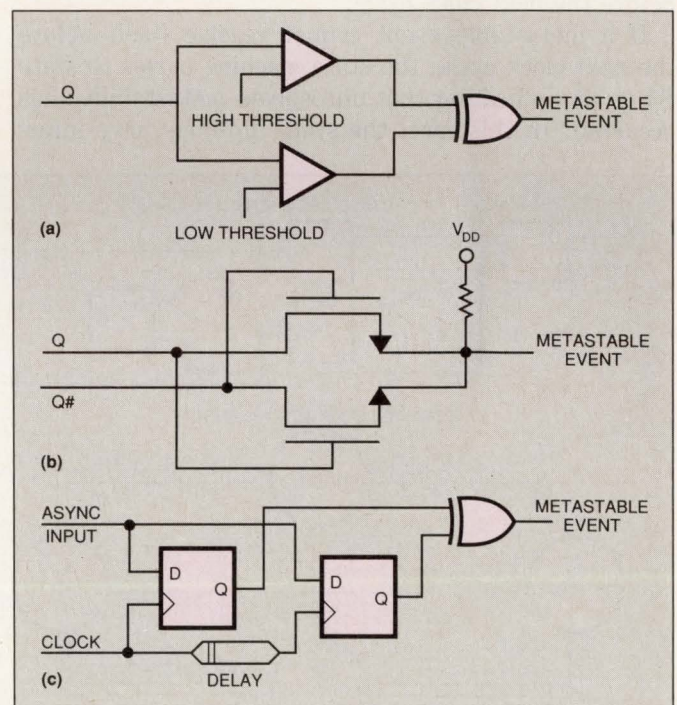


Fig 1—Of the three methods commonly proposed for metastability testing, you cannot use the intermediate voltage sensor (a) or the output proximity sensor (b) with PLDs because of the internal circuitry that comes between their input registers and their outputs. However, you can create a late-transition sensor (c) within the PLD itself.

Because there isn't a standard metastability test method for PLDs, vendors do not provide this information on data sheets.

3. *Late-transition sensor:* If the sensor is separated from the metastable signal by one or more gates, as in a PLD, the metastable signal itself may not be detected; the test circuitry must infer the occurrence of metastability by some other means. Using a late-transition sensor, the sample input is detected at a time t_1 , and then at a later time t_2 . If these two signals disagree, the device under test was metastable at time t_1 (Fig 1c).

Test circuit for PLDs

The only practical test for PLDs uses late-transition detection. Fig 2a shows a metastability test circuit that you can implement within sample PLDs. This circuit allows a PLD to, effectively, test itself.

A state diagram, Fig 2b, shows how the circuit works. During normal operation, the states of the two flip-flops transition between S1 and S2, depending on the state of the synchronizer, and the exclusive-OR of these outputs produces a logical-high output from the device. The high indicates either that metastability has not occurred or, if it did occur, that it was resolved before the next clock cycle.

If a metastable event cannot resolve itself before the next clock cycle, the state machine moves to state S3 or S4, indicating that unresolved metastability has occurred. In this case, the state flip-flops have inter-

preted the signal from the synchronization register differently, and the exclusive-OR of this signal produces a logical low at the output of the device.

Although this test setup catches all failures, it does not record metastable events that resolve themselves before the next clock cycle. The fact that a given flip-flop went metastable is meaningless by itself. What you need to know is how often metastability creates an error in the system. Metastability only causes an error when it is not resolved by the time the signal is needed by the user.

The test circuit also includes the ability to check the maximum operating frequency of the device under test (Fig 2c). At each clock edge, the output of the first register toggles. When the device reaches its maximum operating frequency, the PLD array cannot resolve the changing signal fast enough to produce a valid output. At this speed, one register may resolve the signal correctly and one may not, or both may produce invalid signal resolutions. In any case, when the exclusive-OR of the state (T1/T2) of the two maximum-frequency testing registers results in anything other than a logical high, the maximum operating frequency of the part has been exceeded.

The setup for testing metastability consists of the equipment in Fig 2d. You will need a fixture (see box, "Physical characteristics of the test board"); a stop-

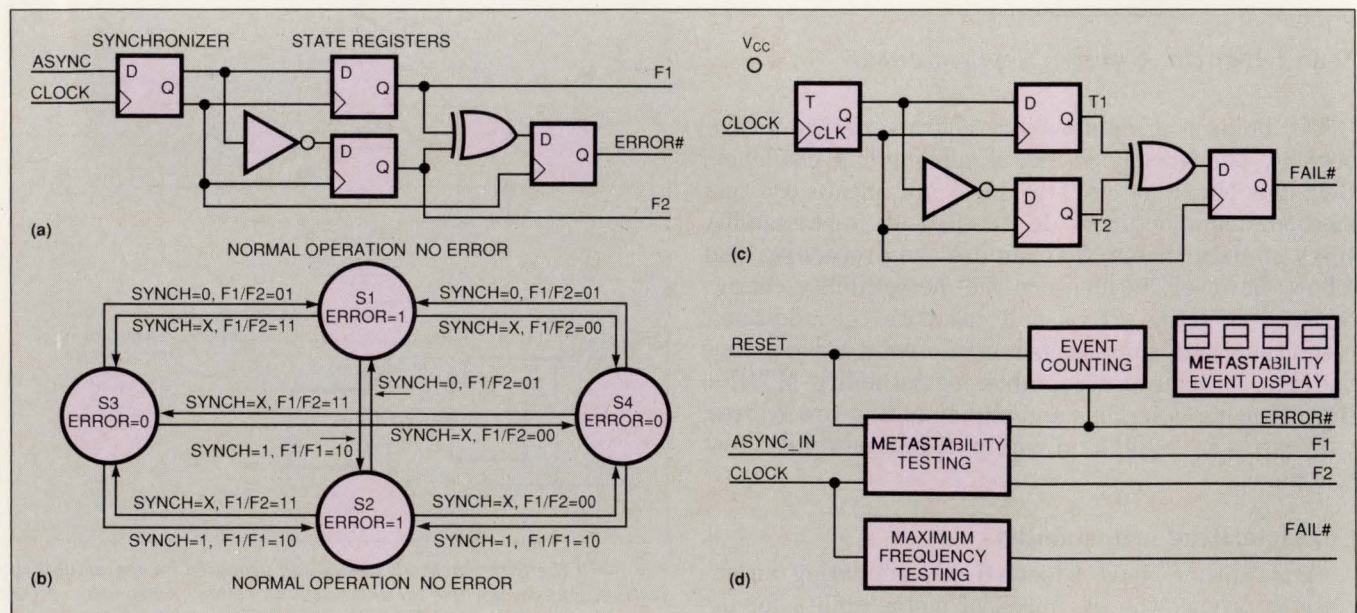


Fig 2—These diagrams illustrate the basic elements of a test fixture. Circuit (a) shows the implementation of a late-transition metastability detector within a PLD, whereas (b) shows its state diagram. Also shown is a maximum-operating-frequency test circuit (c) and a block diagram (d) of the entire fixture.

Physical characteristics of the test board

Cypress uses a 4-layer pc board with two signal planes, a ground plane, and a power plane to perform the metastability measurements. A complete schematic of the test board is shown in **Fig A**. The device under test (DUT) is decoupled with a 0.01- μ F and a 100-pF capacitor. The test circuit is designed to fit all industry-standard and Cypress proprietary PLDs. The socket lets you use pins 1, 2, and 4 of the DUT as clock pins. Pin 3 is the asynchronous input to the device. The ERROR# condition is located on pin 26 (of a 28-pin device) and the FAIL# condition is on pin 20. Two additional outputs, F1 and

F2, are used to monitor the state of the metastability test-circuit flip-flops.

All inputs and outputs connect with BNC connectors located around the board. The clock line, which is terminated with a 50 Ω resistor to match the coaxial input impedance, is buffered with a 74AS04 inverter and isolated from other signals by a ground trace. The input line is also terminated with a 50 Ω resistor and buffered with a 74AS04. Four PLDs drive a 4-digit LED display that counts metastability occurrences.

The ERROR# signal transitions low following a metastable

event, and automatically transitions high again at the next system clock. This low-to-high pulse provides a clock signal to the input of the first of the display-driver PLDs, which in turn increments the display of metastable events. When a digit reaches 9, a cascade signal to the next higher digit is generated at the next occurrence of metastability. You can obtain a JEDEC map of the programming of these 16R8-25 PLDs from the Cypress Applications Bulletin Board ((408) 943-2954). You'll need to use 20- or 25-nsec PLDs to count reliably at high clock rates such as those used in the previous examples.

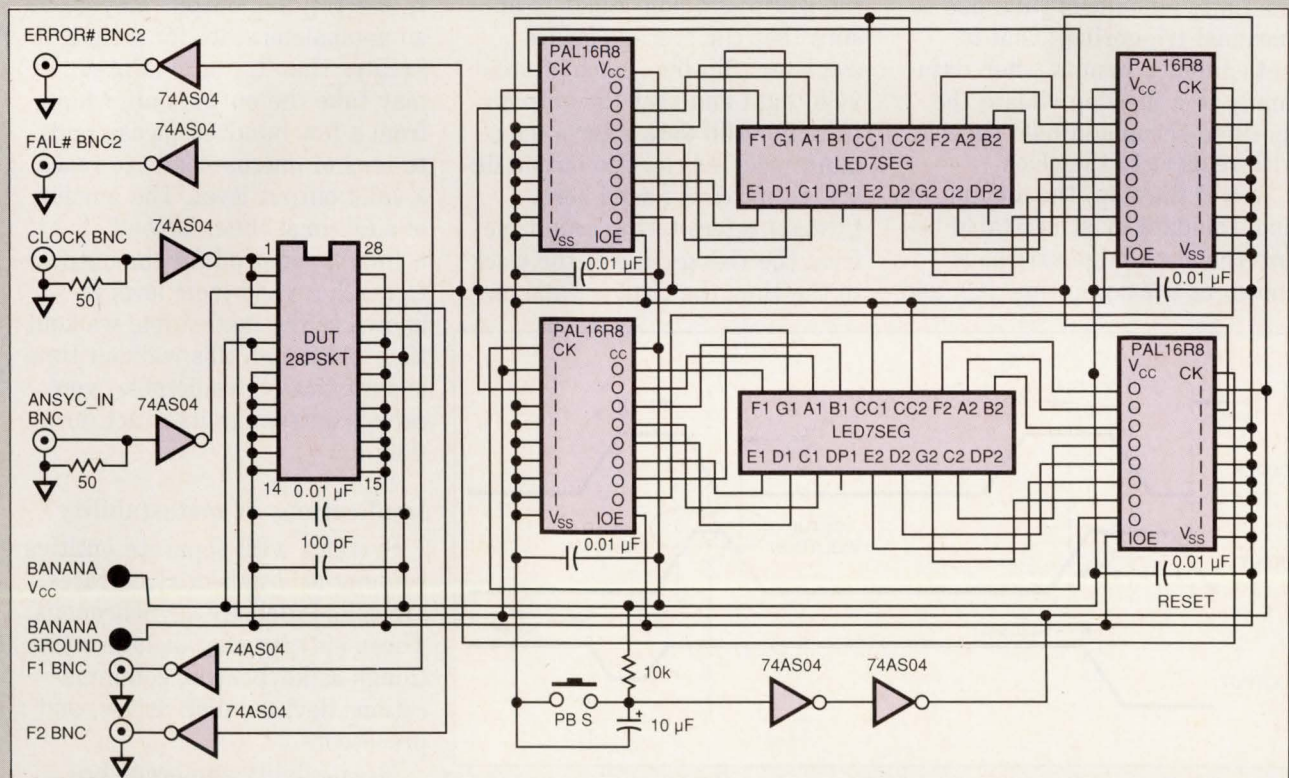


Fig A—This test-fixtue circuit is constructed on a 4-layer board with separate ground and power planes for high-speed performance. JEDEC maps for programming the 16R8-25 display-driver PLDs are available from the Cypress Applications Bulletin Board.

In addition to being able to provide good metastability characteristics, PLDs offer greater versatility than flip-flops or latches.

watch; some programmed PLDs to test; pulse generators to simulate the clock signal, f_c , and the asynchronous data signal, f_d ; a frequency counter; an oscilloscope; and a logic analyzer. The results discussed in this article were obtained using two independent pulse generators (Hewlett-Packard 8082As), a Tektronix DAS9200 logic analyzer, and a Tek 2465 CTS digital oscilloscope with an internal frequency counter.

When the metastable event rate is low, you can use the stopwatch and the readouts on the test fixture to determine MTBF. When the event rate is high, connect the FAIL# output of the fixture to the logic analyzer and measure the event rate.

The purpose of the test is to determine two constant,

device-specific parameters, W and t_{sw} , that will enable you to calculate t_r , the resolution time you must use in your designs to limit metastability MTBF to an acceptable value. The W parameter represents a bounded time interval of the clock edge within which a simultaneous transition of the clock and data will cause a metastable event. The t_{sw} parameter represents the settling time of a metastable flip-flop. In a graphical presentation such as that in Fig 3, t_{sw} is 1/slope of the line that plots t_r vs $\ln(\text{MTBF})$. Start the test on samples of a particular PLD by creating the equations used to program the devices. Listing 1 shows the equations for 22V10s.

After programming the devices, test each part for

Metastability basics

Metastability is a phenomenon in which the outputs of a flip-flop are undefined or oscillate between high and low states for an indefinite amount of time due to marginal triggering. That is, metastability results when data inputs to a flip-flop violate the specified setup and hold times with respect to the clock.

In a D flip-flop, the amount of time the data must be stable before the clock edge arrives is known as the setup time (t_s), and

the amount of time this data must remain stable after the clock edge occurs is known as the hold time (t_h). The data must satisfy both the setup and hold times to ensure that the storage device (register, flip-flop, latch) stores valid data and that the outputs present valid data after a maximum specified clock-to-output delay, $t_{co}(\text{max})$. As used here, $t_{co}(\text{max})$ refers to the total time from the rising edge of the clock to the time the data is valid on

the outputs. In most cases, $t_{co}(\text{max})$ is equal to the maximum t_{co} specified in data sheets.

If the data violates either t_s or t_h , the flip-flop output may go to an anomalous state for a time greater than $t_{co}(\text{max})$ (Fig A). It may take the outputs anywhere from a few hundred picoseconds to tens of microseconds to reach a valid output level. The amount of additional time, beyond $t_{co}(\text{max})$, required for the outputs to reach a valid logic level is known as the metastable walkout time. Although this walkout time is statistically predictable, you cannot determine its exact duration.

Implications of metastability

Systems with separate entities running at different clock rates are called globally asynchronous. These entities may include such things as keyboards, communications devices, disk drives, and processors.

Metastability can occur between two concurrently operating digital systems that lack a

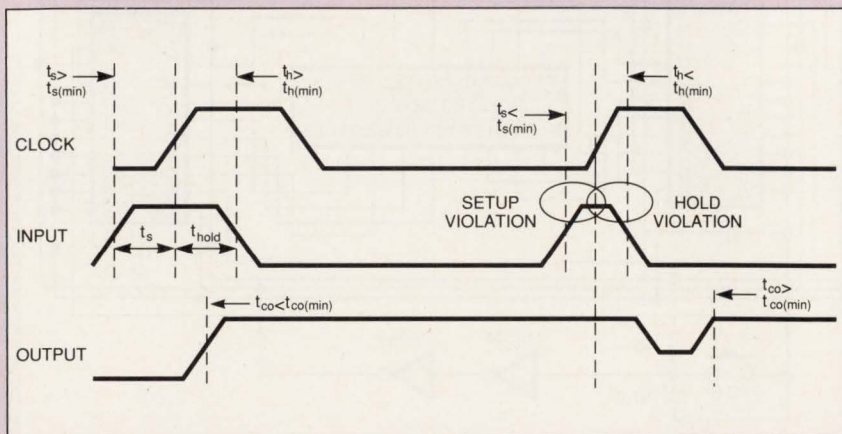


Fig A—This diagram shows the triggering modes in a simple flip-flop. If the setup and hold times are violated, the output will be metastable for a time that is not predictable. In any system that is not globally synchronous, such violations are inevitable.

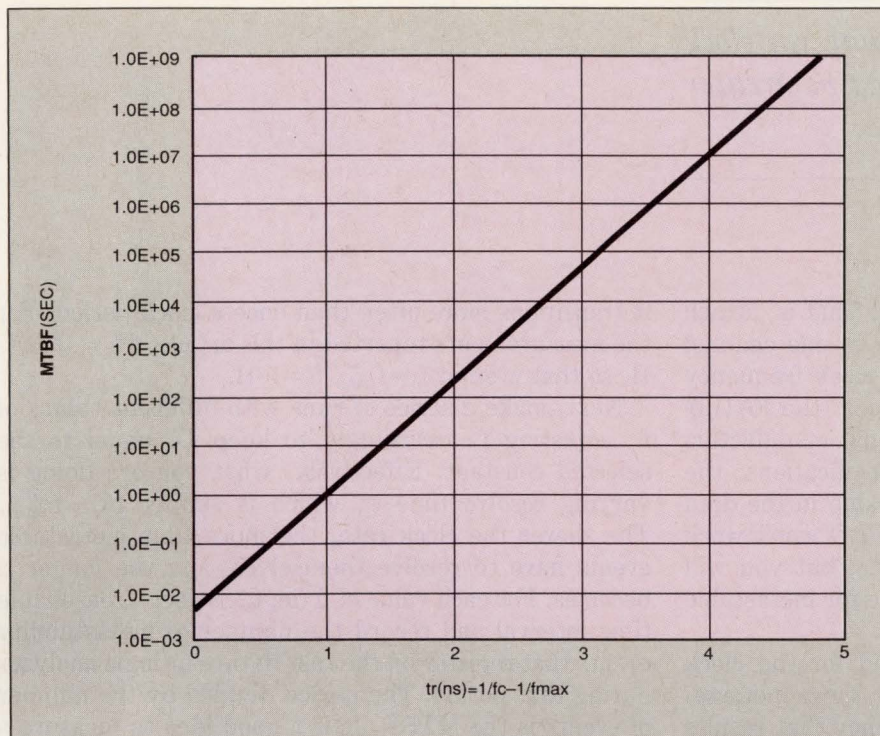


Fig 3—Using this semilog plot, you can quickly determine the resolve time (t_r) needed in your system to achieve a given MTBF.

common time reference. For example, in a multiprocessing system it is possible that a request for data from one system may occur at nearly the exact moment that this signal is sampled by another part of the system. In this case the request, if it does not obey the setup and hold times of the requested system, may be undefined.

When globally asynchronous systems communicate with each other, their signals must be synchronized. Arbitration must occur when two or more requests for a shared resource are received from asynchronous systems. An arbiter decides which of two events are serviced first. A synchronizer, a type of arbiter with a clock as one of the arbitrated signals, must make its decision within a fixed amount of time. A device may synchronize an input signal from an external, asynchronous device in cases such as a keyboard input, an external interrupt, or a communications request.

You can use two methods to

produce locally synchronous systems from globally asynchronous systems. The first involves producing self-timed systems. In a self-timed system, the entity that performs a task also emits a signal that indicates completion of the task. This handshaking signal allows another component to use the results when they are ready instead of having to wait for the worst-case delay.

The advantage of the self-timed method of synchronization is that machines are able to run at their average speed instead of at their worst-case speed. The disadvantage is that a self-timed system must have extra circuitry to compute its own completion signals and check for the completion of tasks it may have assigned to external entities.

Petri Nets, data-flow machines, and self-timed modules all use the self-timed method of communication among locally synchronous systems. Self-timed structures, however, do not completely eliminate metastability because some may include arbi-

ters that can become metastable.

The second, and more common, method of producing locally synchronous systems from globally asynchronous systems is to use a simple synchronizer. Because most globally asynchronous systems use synchronizers, you must limit the extent of the metastability events that may arise from these systems.

The easiest—and the most widely used—solution for limiting the extent of such events is to give the synchronizing circuit enough time to both synchronize the signal and to resolve any possible metastable event before other parts of the system sample the synchronizer's output. This solution requires knowledge of the metastable characteristics of the device performing the synchronization and an analysis like the discussion of the examples in the main text.

To properly sample the data signal, the clock frequency for a test fixture must be greater than twice the data frequency.

its maximum operating frequency, f_{max} . That is, attach the FAIL# output of the test fixture to one channel of the oscilloscope and watch for the clock frequency at which the device starts to malfunction (the FAIL# scope trace becomes unstable). Note that manufacturers are conservative in assigning specifications; the value of f_{max} will be higher than the value in the data book. At clock rates beyond f_{max} , the PLD won't work reliably. At f_{max} , the PLD will operate, but you will not be able to allow any additional time for metastable events to resolve themselves.

Now that you have an upper bound for the clock frequency, you need a lower bound for these metastability measurements. The clock frequency that results in one metastable event per minute is appropriate. Reduce the clock frequency from f_{max} until the average time between metastable events is one minute and call this clock frequency f_{1min} .

Between f_{max} and f_{1min} , you must select a frequency constant, f_{cd} . The selection criterion is that the clock frequency must always be greater than twice the average data frequency. This relationship is necessary because you cannot effectively sample the data signal if

it transitions more often than once a clock period. For the measurements reported in this article, $f_{cd} = (f_{1min})^2 / \Pi$, so that even at $f_c = f_{1min}$, $f_d = f_c / \Pi$.

Next, make a series of runs with different values of f_c , adjusting f_d accordingly to keep f_{cd} equal to the selected constant. Effectively, what you are doing is varying resolve time t_r , which is simply $1/f_c - 1/f_{max}$. The slower the clock rate, the more time metastable events have to resolve themselves, and the longer t_r becomes. For each value of f_c (ie, t_r), select a reasonable time interval and record the number of metastability events that register on the test fixture or logic analyzer during that period. The period divided by the number of events is the MTBF. It is a good idea to measure a batch of identical PLDs and average the results in order to account for process variations.

To describe an idealized graph of the metastability characteristics of the device under test, you can use the expression $\ln(\text{MTBF}) = (t_r/t_{sw}) - \ln(f_{cd}W)$. In the real world, there will be some scattering of the experimental data points, but you can fit a straight line (on semilogarithmic coordinates) by using a linear regression analysis. The graph in Fig 3 was created using Lotus 1-2-3, which incorporates linear regression analysis among other statistical functions.

Forcing the Y intercept ($f_{cd}W$) of the graph of $\ln(\text{MTBF})$ vs t_r to a constant value, allows you to use the equation $t_{sw} = (t_{r1} - t_{r2}) / (\ln(\text{MTBF1}) - \ln(\text{MTBF2}))$ to calculate the slope of the line. This is the actual value of t_{sw} for the PLDs. With f_{cd} held constant, W is the intercept with the MTBF axis, divided by f_{cd} .

Table 1 lists the results of the metastability tests on Cypress PLDs. It should be possible for users to duplicate these results and extend them to PLDs made by other manufacturers. Cypress recommends that others adopt this procedure as an effective standard for metastability testing. The table lists the devices, along with the maximum data-book operating frequency, $f_{max} = 1/(t_{co} + t_s)$, where t_{co} is the clock-to-feedback delay and t_s is the setup time of the output register. The experimental results also include the metastability equation constants, W and t_{sw} , and the metastability resolve time, t_r , required for a 10-year metastability MTBF.

You are not limited to a 10-year MTBF. You can use this data directly to determine the maximum metastability resolve-time (t_r) that you must use in a system to yield the degree of reliability you desire. For example, to determine the operating parameters of the Cypress PALC22V10-20 when used as a synchro-

Listing 1—Equations for testing 22V10-PLD metastability

```

C22V10;
{
  Cypress Semiconductor
  Revision: 06/28/90

  These are the equations to perform
  metastability testing on the PALC22V10
}

CONFIGURE;

CLOCK,          {CLOCK input on pin 1}
ASYNC_IN(node = 3), {Asynchronous input signal}
RESET(node = 5),   {RESET signal}
TSYNC(node = 15), {Synchronization for Fmax}
T1(node = 17),    {State node for Fmax}
T2(node = 18),    {State node for Fmax}
FAIL(node = 16),  {Fmax indication}
SYNC(node = 19),  {Synchronization for Meta test}
F1,              {State node for Meta test}
F2,              {State node for Meta test}
ERROR,          {Metastable Event indication}

EQUATIONS;

/ASYNC = <sum> ASYNC_IN;          {Synchronize Asynchronous input}

/F1 = <oe>
      <sum> SYNC;                {Have two registers hold the}
                                  {true and inverted sense of}
                                  {the synchronization register}

/F2 = <oe>
      <sum> /SYNC;

/ERROR = <oe>
          <sum> /RESET * F1 * /F2 {ERROR# goes low when the XOR}
          + /RESET * /F1 * F2    {of F1 and F2 is false, ERROR#}
          + RESET * ERROR;      {also toggles on RESET}

/TSYNC = <sum> TSYNC;            {Fmax reg toggles on every clock}

/T1 = <sum> TSYNC;              {Have two registers hold the}
                                  {true and inverted sense of}
                                  {Fmax reg}

/T2 = <sum> /TSYNC;

/FAIL = <oe>
          <sum> T1 * /T2          {FAIL# goes low when the XOR}
          + /T1 * T2;           {of T1 and T2 is false, indicating}
                                  {Fmax has been exceeded}

```

TABLE 1—Metastability characteristics of some Cypress PLDs

Device	f _{max} (MHz)	W (fsec)	t _{sw} (nsec)	t _r (nsec) (10-year MTBF)
PALC16R8-25	28.5	9.503	0.515	14.68
PALC20G10-20	41.6	3.73	0.173	4.91
PALC20RA10-15	33.3	2.86	0.216	5.87
PALC22V10C-10	90.9	0.00808	0.547	13.0
PALC22V10B-15	50.0	55.76	0.261	8.19
PALC22V10-20	41.6	0.125	0.190	4.73
CY7C330-66	66.6	1.02	0.290	8.12
CY7C331-20	31.2	298.0	0.184	5.91
CY7C332-15	47.6	1.55	0.337	9.35
CY7C344-20	41.6	966.0	0.223	7.55

nizer, first decide on your desired MTBF. Suppose you pick a 10-year (315 × 10⁶ sec) MTBF, meaning that, on the average, you can accept a synchronization failure once every 10 years.

From **Table 1**, t_{sw} = 0.190 × 10⁻⁹, and W is 0.125 × 10⁻¹². Assume that the clock, f_c, is operating at f_{max} (41.6 MHz in the Cypress Data Book). Also, to ensure effective data sampling by the synchronizer, assume that the average asynchronous data frequency is, at most, half of the clock frequency.

Recall that frequency f_d, as defined here, represents the rate at which the data changes state. During any given asynchronous data period, the asynchronous data changes state twice: once from a logic-low state to a logic-high state and again from a logic-high state to a logic-low state. Because any state change may cause a metastable event, f_d must be set to twice the average asynchronous data frequency when determining the worst-case MTBF.

From this information, you can calculate the minimum time (t_r) you must allow in your circuit timing budget for metastability resolution beyond the minimum operating period of the device. Use the following calculations. From

$$MTBF = \frac{e^{t_r/t_{sw}}}{f_c f_d W}$$

it is clear that

$$t_r = t_{sw} (\ln(MTBF) + \ln(f_c f_d W))$$

$$t_r(\text{sec}) = (0.190 \times 10^{-9}) [\ln(315 \times 10^6) + \ln(41.6 \times 10^6 \times 41.6 \times 10^6 \times 0.125 \times 10^{12})]$$

$$t_r = 4.73 \text{ nsec}$$

Because of the uncertainty in real-system trace delays and clock-generator skew, you would probably use 5 nsec instead of 4.73 nsec for t_r. Then, working backwards, the maximum operating frequency of the synchronizer, f_c, in this system would become

$$f_c = 1/(t_s + t_{cf} + t_r) = 1/(10 \text{ nsec} + 12 \text{ nsec} + 5 \text{ nsec}) = 37.0 \text{ MHz}$$

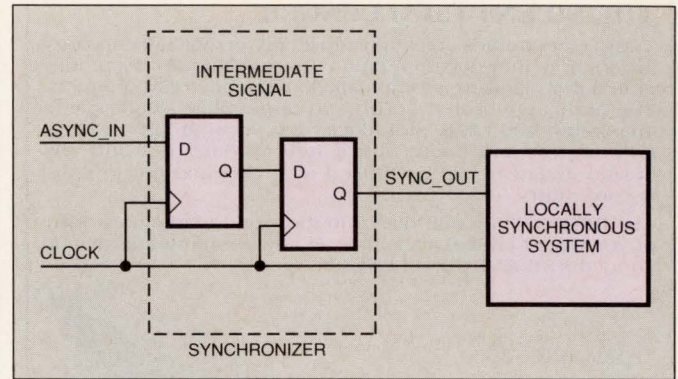


Fig 4—Two-stage synchronization improves metastability performance by an order of magnitude. If you also use the second stage for some Boolean operations that are required by the application, you may not have to pay a latency penalty for adding the second stage.

Using these new values for t_r and f_c, and substituting them in the previous relationship for MTBF, the effective MTBF becomes 1.57 × 10⁹ sec = 49.7 years.

For another example, consider using a Cypress CY7C330-50 as a synchronizer in a system that has output registers clocked at a frequency, f_c, of 35.7 MHz and in which the data has an average frequency of 10 MHz. You can calculate the MTBF for this example by first determining the metastable resolution time, t_r, allowed for synchronization. You can calculate t_r with the following equation.

$$t_r = 1/f_c - 1/f_{max} = 1/35.7 \text{ MHz} - 1/50.0 \text{ MHz} = 8 \text{ nsec}$$

With this result, you can calculate the MTBF as before. In this case, MTBF = 1.31 × 10⁹ sec = 41.6 years.

In this example, the **Table 1** values for W and t_{sw}, which were measured on a 66-MHz part, were used with a 50-MHz device. The experimentally determined constants are valid for all speed grades of a particular device. To achieve these results, the typical 10-MHz test data frequency was doubled to 20 MHz.

The next example shows how you would use a Cypress PALC22V10C-10 as a synchronizer. For a 10-year MTBF, assuming f_c and f_d are at their maximum (from the Cypress Data Book), the required t_r is

$$t_r(\text{sec}) = (0.547 \times 10^{-9}) [\ln(315 \times 10^6) + \ln(90.9 \times 10^6 \times 90.9 \times 10^6 \times 8.08 \times 10^{-15})] = 13.0 \text{ nsec}$$

Using this result, the maximum operating frequency of the synchronizer would be reduced from 90.9 MHz to

$$f_c = 1/[(1/f_{max}) + t_r] = 1/[(1/90.9 \text{ MHz}) + 13.0 \text{ nsec}] = 41.6 \text{ MHz}$$

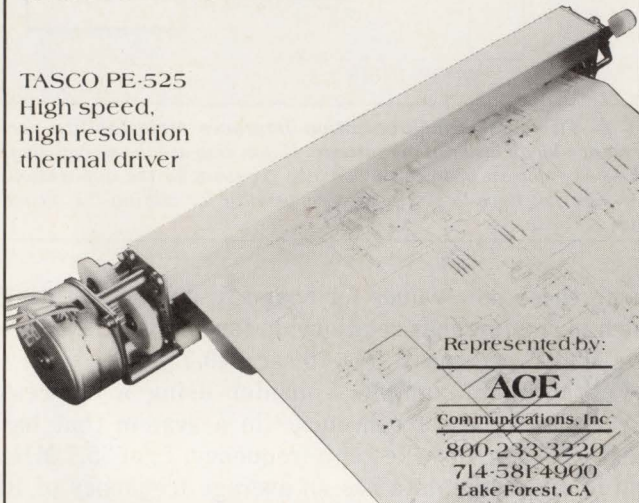
You can improve MTBF by using a second register in series with the first register to perform 2-stage synchronization, as shown in **Fig 4**. In this arrangement, the output of the first synchronization register is fed to the input of the second synchronization register. Even though you use a second register stage, you often

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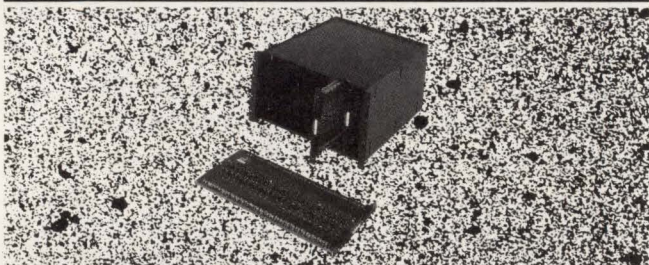
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don't incur additional latency because you can feed the second stage with some Boolean combination of input and output signals that you would need to input anyway. The metastability characteristics listed in Table 1 apply to asynchronous inputs that are used for combinations of existing inputs and outputs, as well as asynchronous inputs to PLD registers that are used directly.

The reason for using a 2-stage synchronizer in a PLD is that the probability of a synchronizer's being metastable after the second stage of synchronization is the square of the probability that a synchronizer is metastable after the first stage of synchronization. The MTBF equation becomes

$$MTBF = \left[\frac{e^{t_r/t_{sw}}}{f_c f_d W} \right]^2$$

From this result, the equation for t_r becomes

$$t_r = [t_{sw} \ln(MTBF) + 2 \ln(f_c f_d W)] / 2$$

Using this result for a 2-stage synchronizer in a Cypress PALC22V10C, the t_r for a 10-year MTBF is reduced from 13.0 nsec to

$$t_r(\text{sec}) = (0.5)(0.547 \times 10^{-9}) [\ln(315 \times 10^6) + \ln(90.9 \times 10^6 \times 90.9 \times 8.08 \times 10^{-15})] = 7.65 \text{ nsec},$$

and the maximum f_c is increased from 41.6 MHz to

$$f_c = 1 / [(1/f_{\text{max}}) + t_r] = 1 / [(1/90.9 \text{ MHz}) + 7.65 \text{ nsec}] = 53.6 \text{ MHz}.$$

This example shows that if the cycle of latency caused by the additional synchronization stage is acceptable, you can dramatically increase the maximum operating frequency of the synchronizer. **EDN**

Author's biography

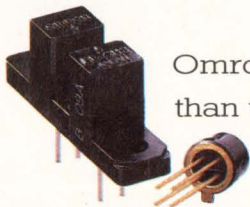
Sean Dingman is an applications engineer and has been with Cypress Semiconductor for two years. His duties include finding applications for existing products and defining the requirements for new products. Sean has a BS in computer engineering from the University of Michigan.

Article Interest Quotient (Circle One)

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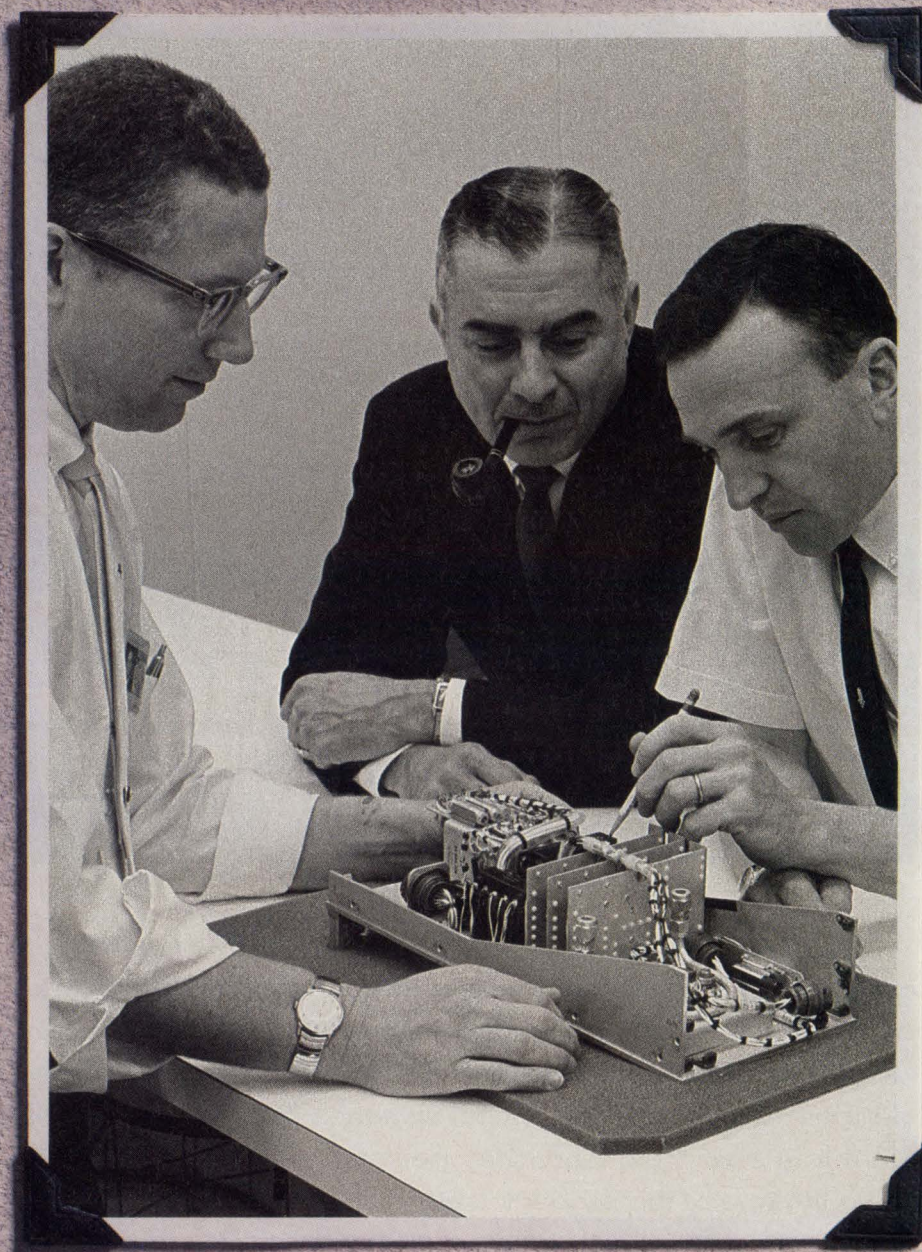
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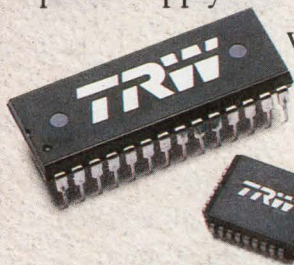
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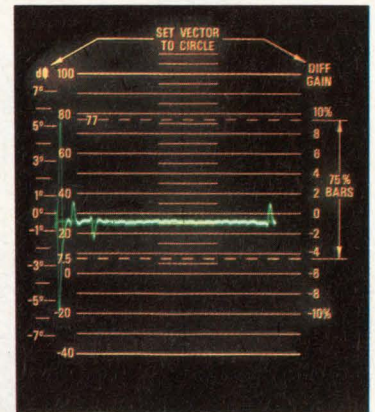
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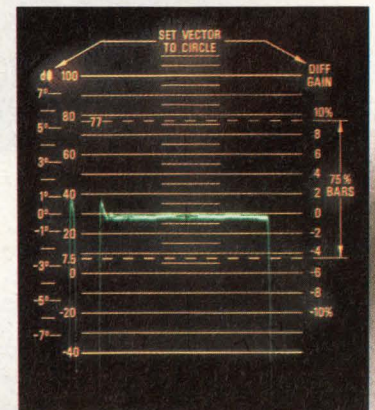
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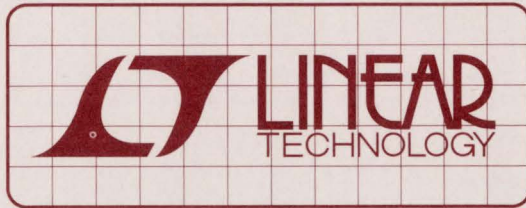
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DESIGN NOTES

No Design Switching Regulator 5V, 5A Buck (Step Down) Regulator – Design Note 48

Ron Vinsant

Introduction

This simple, no design regulator, is a step down DC to DC converter designed to convert an 8V to 40V input to a regulated 5V output. The 5V output is capable of sourcing up to 5A of output current.

This converter is based on the Linear Technology LT1074 switching regulator IC. This device needs only a few external parts to make up a complete regulator including thermal protection and current limit. This design uses off-the-shelf parts for low cost and easy availability of components. Specifications for the circuit are in Table 1.

Circuit Description

Figure 1 shows the schematic of the circuit. For the purpose of this explanation assume that the output is at a constant +5V DC and that the input voltage is greater than +8V DC.

At intervals of $\approx 10\mu\text{s}$ (100kHz) the control portion of the LT1074 turns on the switch transistor between the V_{IN} and V_{SW} pins impressing a voltage across the inductor, L1. This causes current to build up in the inductor while also supplying current to the load and capacitor C1.

The control circuit determines when to turn off the switch during the $10\mu\text{s}$ interval to keep the output voltage at +5V DC. When the switch transistor turns off, the magnetic field in the inductor collapses and the polarity of the voltage across the inductor changes to try and maintain the current in the inductor. This current in the inductor is now directed (due to the change in voltage polarity across the inductor) by the diode, D1, to the load. The current will flow from the inductor until the switch turns on again, (continuous operation) or until the inductor runs out of energy (discontinuous operation).

Referring back to Figure 1, the divider circuit of R1 and R2 is used to set the output voltage of the supply against an internal voltage reference of 2.21V DC.

R3 and C2 make up the frequency compensation network used to stabilize the feedback loop.

Conclusion

This Design Note demonstrates a fully characterized step down converter circuit that is both simple and low cost. This design can be taken and reliably used in a production environment without the need for any custom components. A P.C. board layout and FAB drawing are available from Linear Technology.

Table 1. Performance Summary (Operating Temperature Range 0°C to 50°C)

Input Voltage Range		+ 8.0V to + 40.0V DC	
Output	Output Voltage ($\pm 0.15\text{V DC}$)	+ 5.00V DC	
	Max Output Current $V_{IN} = 8.0\text{V to } 40.0\text{V}$	5.0A DC	
	Typical Output Ripple at $I_{OUT} = 4.0\text{A DC}$ @ Switching Frequency	With Optional Filter (L2 & C4) Without Optional Filter (L2 & C4)	5mVp-p 50mVp-p
	Load Regulation $V_{IN} = 8\text{V}$	At $I_{OUT} = 0.5\text{A DC to } I_{OUT} = 5.0\text{A DC}$	0.5%
	Line Regulation $I_{OUT} = 5\text{A}$	At $V_{IN} = + 8.0\text{V DC to } V_{IN} = + 40.0\text{V DC}$	0.5%

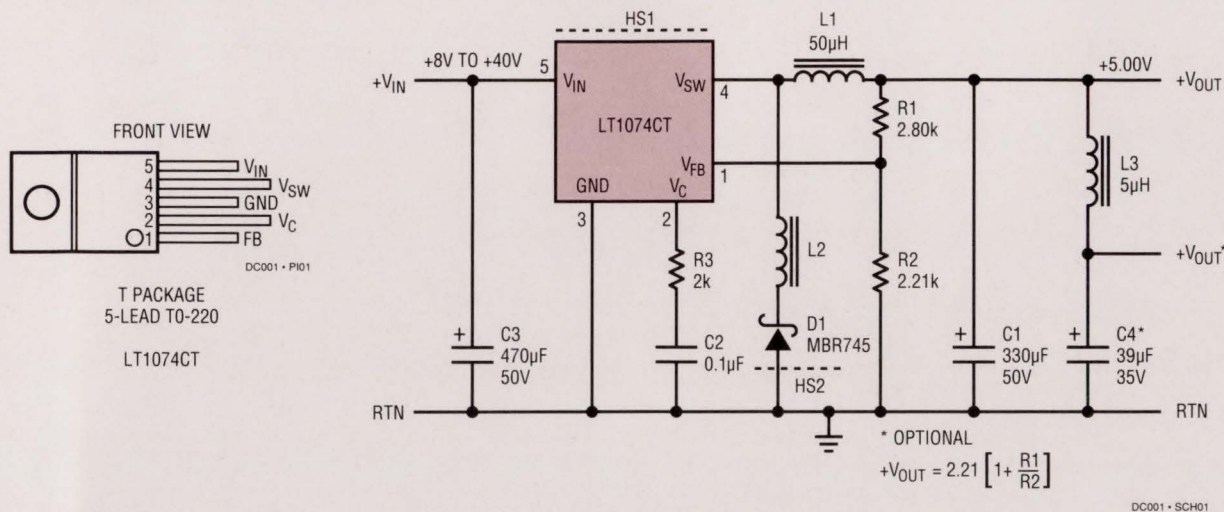


Figure 1. Package and Schematic Diagrams

Table 2. Parts List

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR
PCB	1	001A	PCB FAB, Buck Switching Regulator	LTC
D1	1	MBR745	Diode, Schottky, 7A, 45V	Motorola
HS2	1	6038B-TT	Heatsink	Thermalloy
L2	1	2664000101	Shield Bead	Fair-Rite
VR1	1	LT1074CT	Switching Regulator, 100kHz	LTC
HS1	1	7020B-MT	Heatsink	Thermalloy
C1	1	SXE50VB331M12X20LL	Cap, Alum Elect, 330µF, 50V	United Chemicon
C2	1	CKO6BX104K	Cap, Ceramic, 0.1µF, 50V	AVX
C3	1	UPL1H471MRH	Cap, Alum Elect, 470µF, 50V	Nichicon
C4	1	UPL1V390MAH	Cap, Alum Elect, 39µF, 35V	Nichicon
L1	1	CTX50-5-MP	Inductor, 50µH, 5A	Coiltronics
L3	1	CTX5-5-FR	Inductor, 5µH, 5A	Coiltronics
R1	1	MF 1/8W 2.80kΩ	RES, MF, 1/8W, 1%, 2.80kΩ	
R2	1	MF 1/8W 2.21kΩ	RES, MF, 1/8W, 1%, 2.21kΩ	
R3	1	CF 1/4W 2kΩ	RES, CF, 1/4W, 5%, 2kΩ	

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DESIGN IDEAS

EDITED BY CHARLES H SMALL

Utility modifies Zipfiles

Gábor László Kiss
Budapest, Hungary

Zipzap is a utility for modifying, cutting, and pasting Zipfiles (compressed archives in Zipfile format, as defined by Phil Katz). Zipzap lists contents of Zipfiles, copies or moves files from source Zipfiles to destination Zipfiles, removes files from Zipfiles, and encrypts/decrypts files in Zipfiles (registered copies only). You do not have to un-Zip files and Zip them up again if

you want to split a large Zipfile into small pieces. Just use Zipzap. Zipzap is fast, because it handles files without expansion (or decryption). You can obtain the executable program and documentation from the EDN BBS's DI Special Interest Group (617-558-4241,300/1200/2400,8,N,1—from main menu, enter (s)ig, <s/di_sig>, rk992). EDN BBS /DI_SIG #992 **EDN**

To Vote For This Design, Circle No. 746

Detector spots sneaky smokers

Miss J Vandana
SEMP, Kalpakkam, TN, India

The circuit in Fig 1 detects smokers who surreptitiously light up in nonsmoking areas before they can take a single puff. The Hamamatsu UVTRON R2868 flame sensor detects a cigarette lighter's ultraviolet emanations from as far away as 16 feet, producing a train of pulses across capacitor C_1 . The LM2907N-8 compares these pulses to a preset reference level, flashing the LED as soon as a flame appears.

The UV detector is a form of Geiger-Mueller tube. The sensor is "sun blind," that is, it will operate properly in the presence of sunlight. It will pick up both petroleum fuel and gas flames, which are rich in ultraviolet light. However, be prepared for false alarms from other sources of ultraviolet light such as electrical arcs and reflections from shiny surfaces.

EDN BBS /DI_SIG #991 **EDN**

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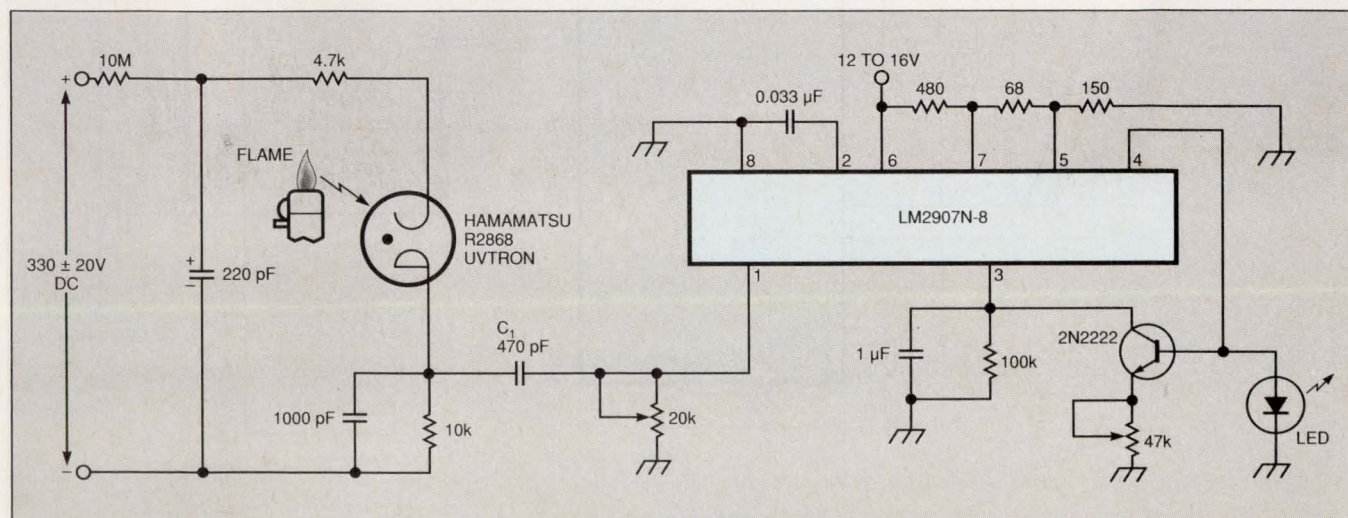


Fig 1—The ultraviolet flame detector in this alarm circuit can spot potential smokers as soon as they fire up their lighters, before they have a chance to take a single puff.

DESIGN IDEAS

FEEDBACK AND AMPLIFICATION

High-side alternatives suggested

Did you notice that in the same January 21, 1991 issue that you printed DI #927, Chuck Thurber's and Ily King's 2-chip "High-side switches control 5V supply," on pg 154, Micrel Semiconductor's advertisement on pg 1 shows a 1-chip solution?

Alternative solutions abound. My high-side-switch circuit in Fig 1 draws less than 5 μA whether it is on or off, and it also uses one chip instead of two. My other circuit (Fig 2) provides output short-circuit protection. Its On current is 275 μA and its Off current is 105 μA . A 5-m Ω shunt resistor and the 5-mV reference voltage applied to pin 12 set the output-current trip level.

Mitchell Lee, Applications Engineer
Linear Technology
1630 McCarthy Blvd
Milpitas, CA 93035

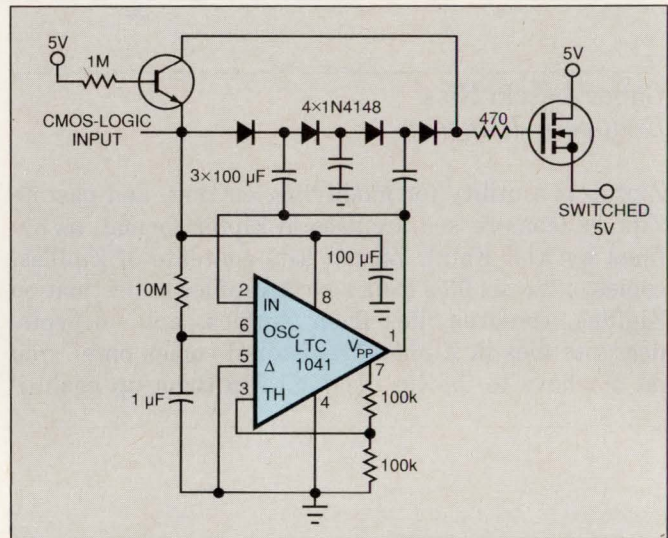


Fig 1—The high-side switch draws less than 5 μA .

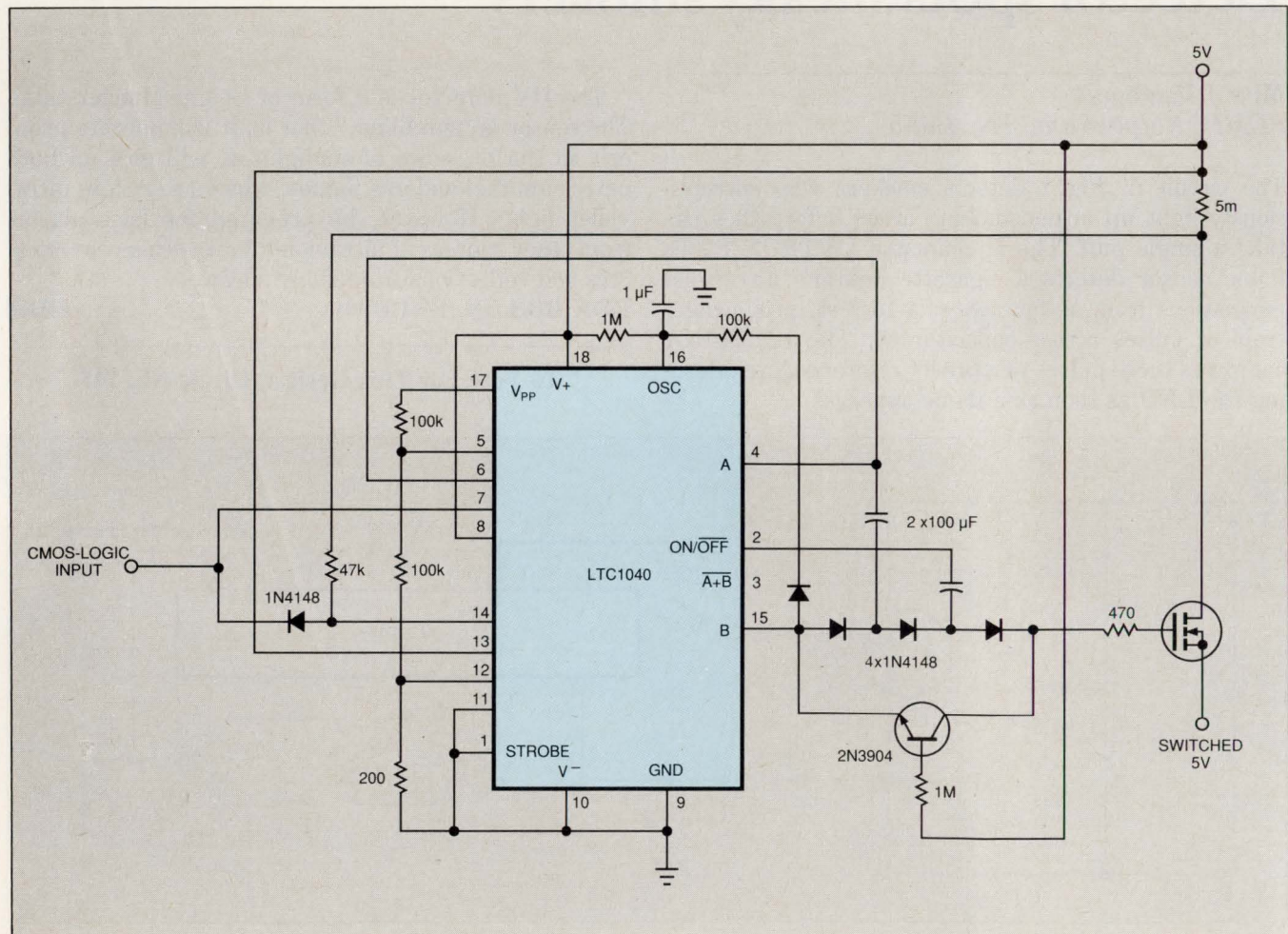
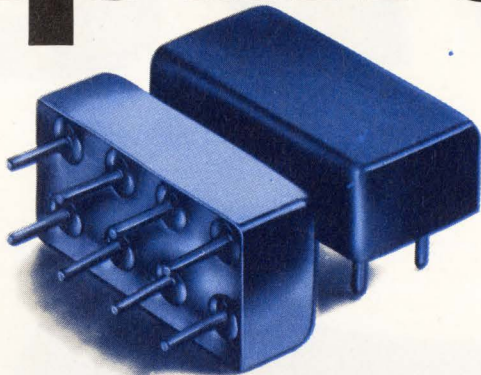


Fig 2—An alternative high-side switch provides short-circuit protection.

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Internally the MAN amplifiers consist of two stages, including coupling capacitors.

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- wide bandwidth • low noise • high gain
- high output power • high isolation

MODEL	FREQ. RANGE (MHz)	GAIN dB		MAX PWR [†] dBm	NF dB (typ)	ISOL. dB (typ)	DC PWR V/ma	PRICE \$ ea. (10-24)
	f_L to f_U	min	flat ^{††}					
MAN-1	0.5-500	28	1.0	+8	4.5	40	12/60	13.95
MAN-2	0.5-1000	18	1.5	+7	6.0	34	12/85	15.95
MAN-1LN	0.5-500	28	1.0	+8	2.8	39	12/60	15.95
◊MAN-1HLN	10-500	10	0.8	+15	3.7	14	12/70	15.95
MAN-1AD	5-500	16	.05	+6	7.2	41	12/85	24.95
MAN-2AD	2-1000	9	0.4	-2	6.5	28	15/22	22.50
MAN-11AD	2-2000	8	0.5	-3.5	6.5	22	15/22	29.95

††Midband $10f_L$ to $f_{U/2}$, ± 0.5 dB † 1dB Gain Compression ◊Case Height 0.3 in. Max input power (no damage) +15dBm; VSWR in/out 1.8:1 max.

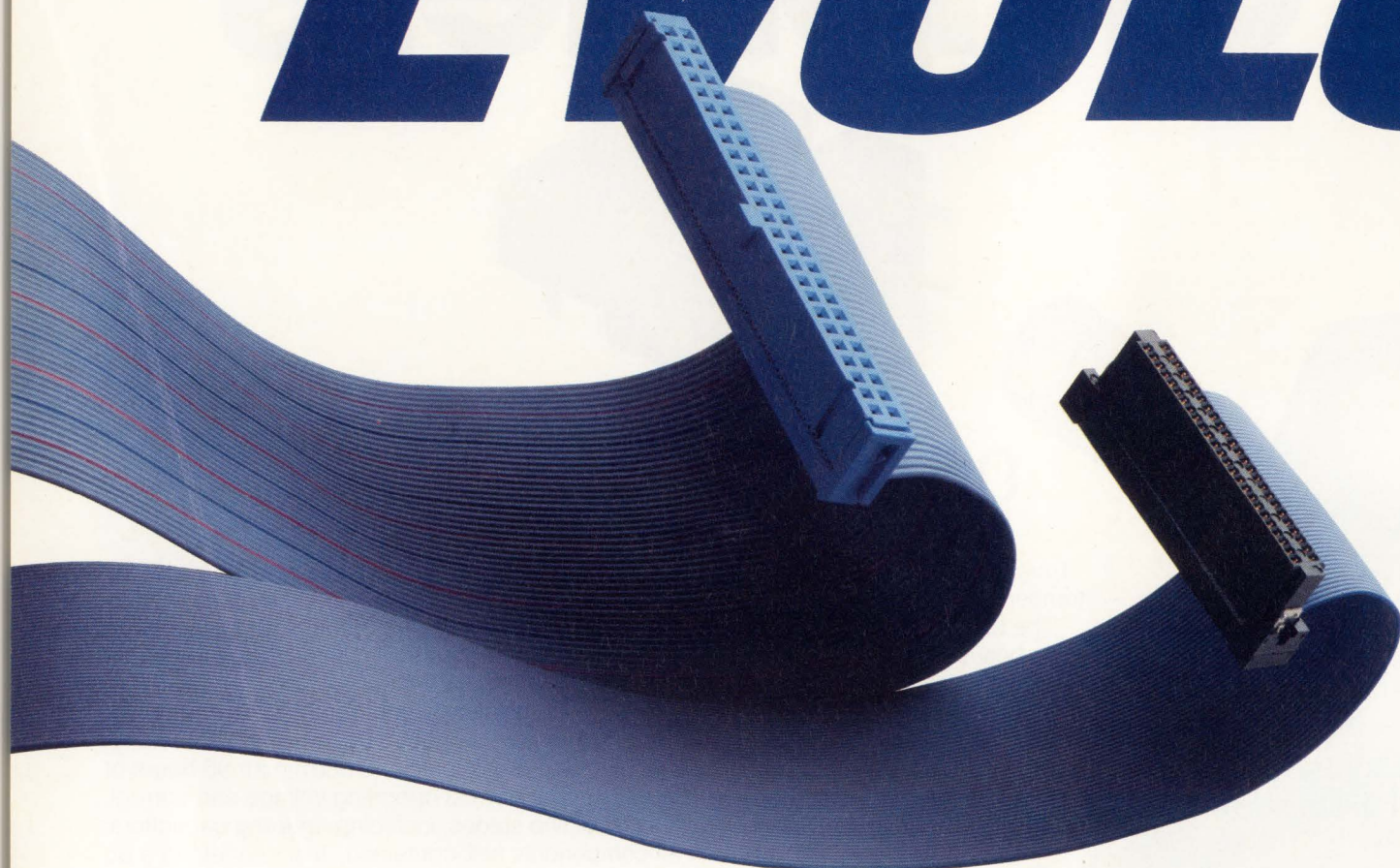
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EVOLVING



The next generation of IDC Interconnection:

Same performance,
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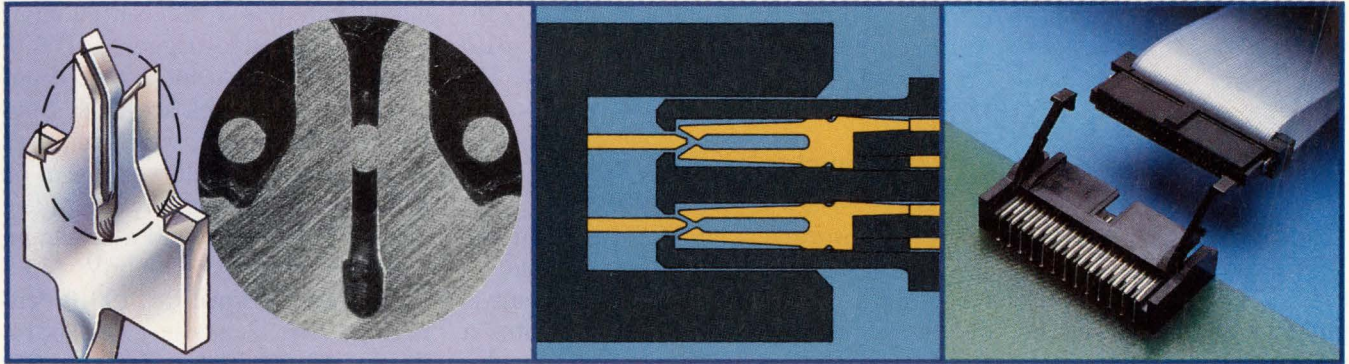
System 311 is the next generation of reliable high performance IDC mass termination systems from Thomas & Betts, a pioneer in the development of IDC.

A natural evolution, the new System 311 combines the finest capabilities of our proven Ansley® IDC System, downsized and precision engineered to terminate .025 pitch cable.

Performance-oriented features make System 311 the new standard in IDC fine pitch systems – a beryllium copper contact with a dual mating beam that provides greater than 100 grams normal force (150

KPSI Hertz Stress), a unique "coined-slot" IDC contact joint, one piece housing design,

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Contact-to-Conductor Relationship –
Thomas & Betts' "coined-slot" contacts are designed to position the terminated conductors within a specified region for maximum conductivity and reliability.

Precision Lead-In Design –
assures that repeated connect/disconnect functions are consistently smooth and without pin damage.

Our Own Vertical Eject Design –
saves board real estate and ensures positive locking and easy disengagement of header from mating socket without stress to cable, contacts, or solder joints.

and high performance materials are combined to ensure excellent system integrity and maximum reliability.

System 311 incorporates these customer-requested features into a compact interconnect system with board space savings of up to 50%.

From cable to connectors to application tooling, System 311 is designed to meet or exceed the most stringent customer requirements for fine pitch IDC mass termination.

For complete information or help with a specific application, call or fax: Thomas & Betts Corporation, Electronics Division, 200 Executive Center Drive, Greenville, S.C., Phone: 803-676-2900, Fax: 803-676-2991.

For the new System 311 Catalog call 800-344-4744.

Thomas & Betts

• **EUROPE – England:** Marlow, 44-6284-6055; **France:** Rungis Cedex, 33-1-4687-2385; **Germany:** Egelsbach, 49-6103-4040; **Italy:** Milano, 39-2-6120451; **Luxembourg:** Foetz, 35-255-0002; **Spain:** Barcelona, 34-3-3002252; **Sweden:** Upplands Vasby, 46-760-88110

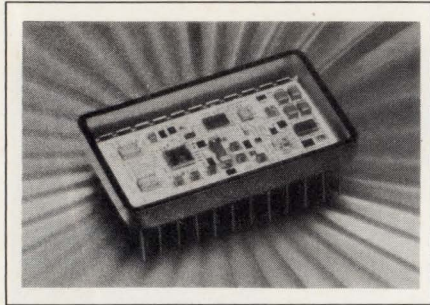
EDN August 5, 1991

NEW PRODUCTS

INTEGRATED CIRCUITS

12-Bit D/A Converter

- 15-MHz update rate
 - 200-nsec full-scale settling time
- Available in a 24-pin hermetic package, the DAC-02320 is a 12-bit D/A converter that features a 15-MHz update rate for small-step changes and a 200-nsec full-scale settling



time. The hybrid circuit includes input latches, a precision dc voltage reference, and a deglitched T/H

output. The device is available in linearity grades of 12 bits (0.012%) and 13 bits (0.006%), and is pin programmable for three output voltage ranges. The device, which uses external potentiometers to trim the offset and gain errors to zero, operates over the -55 to $+125^{\circ}\text{C}$ temperature range. From \$185 (100).

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. FAX (516) 567-5209. **Circle No. 351**

Decision Circuit For Fiber-Optic Systems

- Suitable for SONET applications
- ECL-compatible input/output

The HDMP-2006 decision circuit is a data regenerator that creates a stream of digital data from samples

of the incoming analog signal on a fiber-optic line. It resets the timing to an external reference supplied by the user. Typical applications include Synchronous Optical Network (SONET) 622M-bps repeaters and data-communications and computer links operating at speeds as fast as 1.5G bps. Housed in an 8-pin surface-mount package, the decision circuit contains a differential-input amplifier; an edge-triggered, D flip-flop; and a 50Ω output driver. Input and output voltages are ECL compatible. The device, which requires a minimum threshold voltage of 55 mV, provides a minimum phase margin of 700 psec and a minimum amplitude margin of 100 mV. \$55.

Hewlett-Packard Co, 19310 Pruneridge Ave, Cupertino, CA 95014. Phone (800) 752-0900. **Circle No. 352**

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Available Emulators

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68008	68HC11 Family
68010	including F1&D3
68020	8051 Family
68030	DS5000
68302	8096/80196 Family
68331	8085
68332	64180/Z180
68340	Z80
6809/6809E	

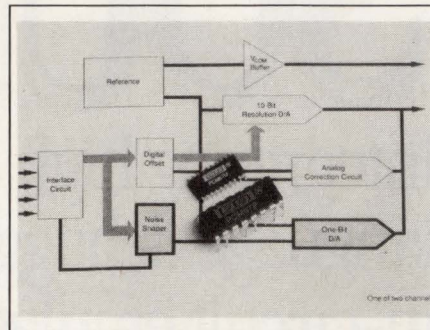


CIRCLE NO. 78

Dual 18-Bit Audio DAC

- *Dynamic range is 108 dB*
 - *Capable of 8× oversampling*
- Targeted for portable and automotive digital-audio applications, the PCM67 dual 18-bit D/A converter operates from a single 5V supply. The device combines a conventional 10-bit DAC using a thin-film R-2R

ladder, a digital offset with analog correction, and a 1-bit DAC to provide high resolution and low zero-crossing distortion. Key specifications include a maximum THD + N of -92 dB at 0 dB FS, an idle-channel S/N ratio of 110 dB, and a dynamic range of 108 dB. The device can sample at a 352.8-kHz rate,



which allows 8× oversampling of the audio spectrum on each channel. Each channel provides an analog output of 1.2 mA typ. The PCM67 is available a 16-pin DIP and a 20-pin SOIC. \$19.50 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (800) 548-6132; in AZ, (602) 746-1111. FAX (602) 889-1510. **Circle No. 353**

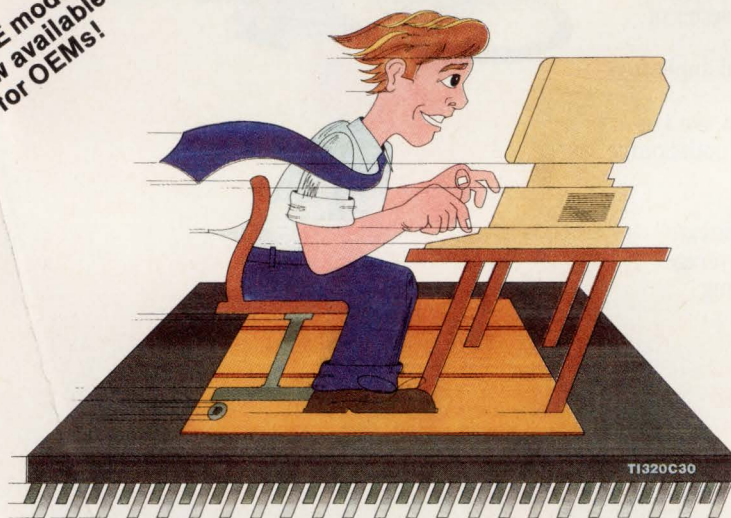
Single-Chip Controller

- *Integrates three separate functions*
- *Supports Intel and Weitek coprocessors*

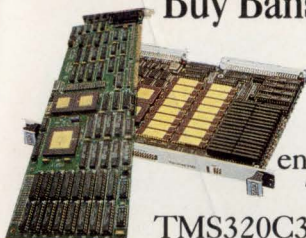
The ACC-2046 chip integrates a memory controller, cache controller, and peripheral controllers in a single chip. The 208-pin plastic quad flatpack device supports 486 and 386DX-based AT systems. The controller supports 512k bytes of direct-mapped cache memory, shadow RAM for video and system BIOS, and a single ROM. The chip interfaces with 8- or 16-bit BIOS ROMs in 128k- or 64k-byte EPROM spaces. The controller handles one to four memory banks of 32-bit dynamic RAM (DRAM) using 256k-, 1M- or 4M-byte DRAMs on a system board that allows as much as 64M bytes of onboard memory. The controller also supports the Intel 80387 and the Weitek 4167/3167 math coprocessors. 25-MHz version, \$100; 33-MHz version, \$125; 40-MHz version, \$140 (1000).

ACC Microelectronics, 3295 Scott Blvd, #400, Santa Clara, CA 95054. Phone (408) 980-0622. FAX (408) 980-0626. **Circle No. 354**

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For detailed specifications and prices, contact Atlanta Signal Processors, Inc., 770 Spring St., Atlanta, GA 30308. Telephone 404/892-7265. Fax 404/892-2512.



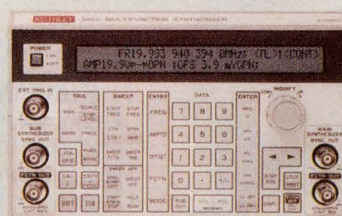
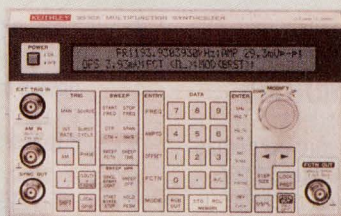
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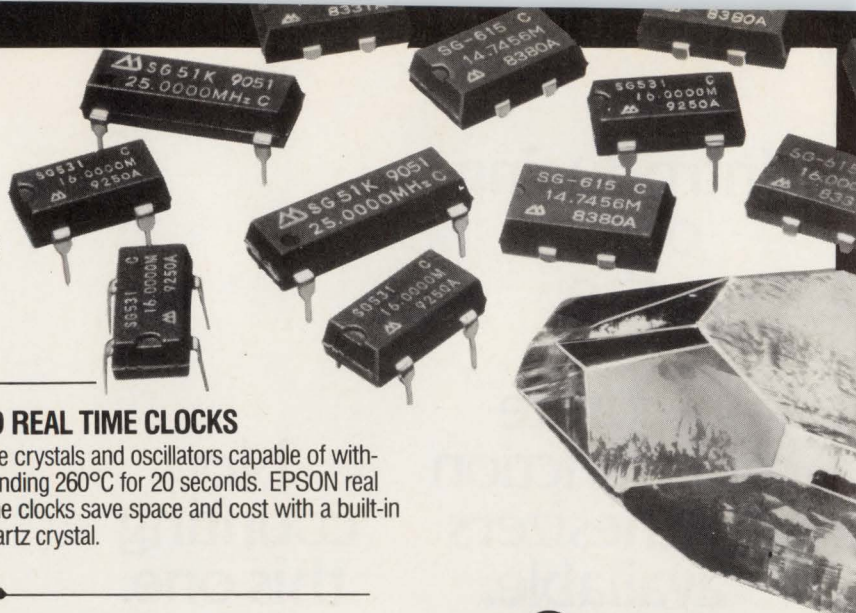
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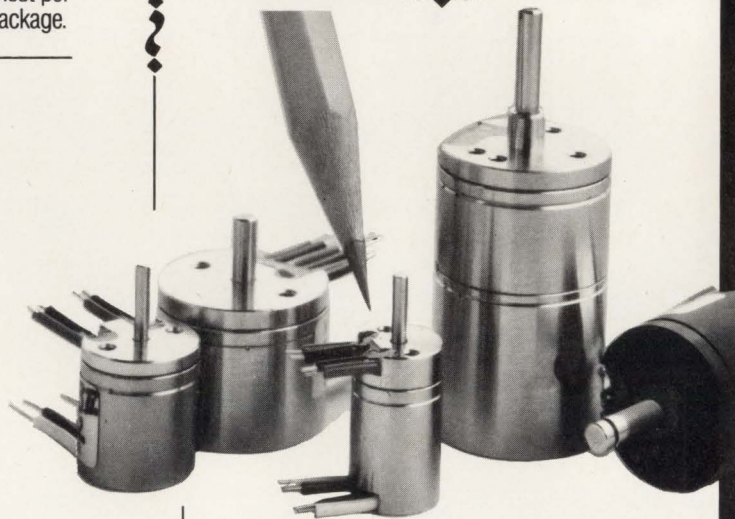


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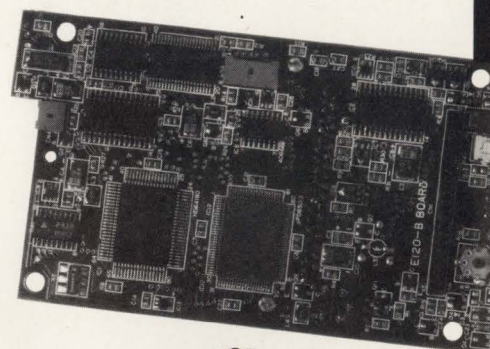
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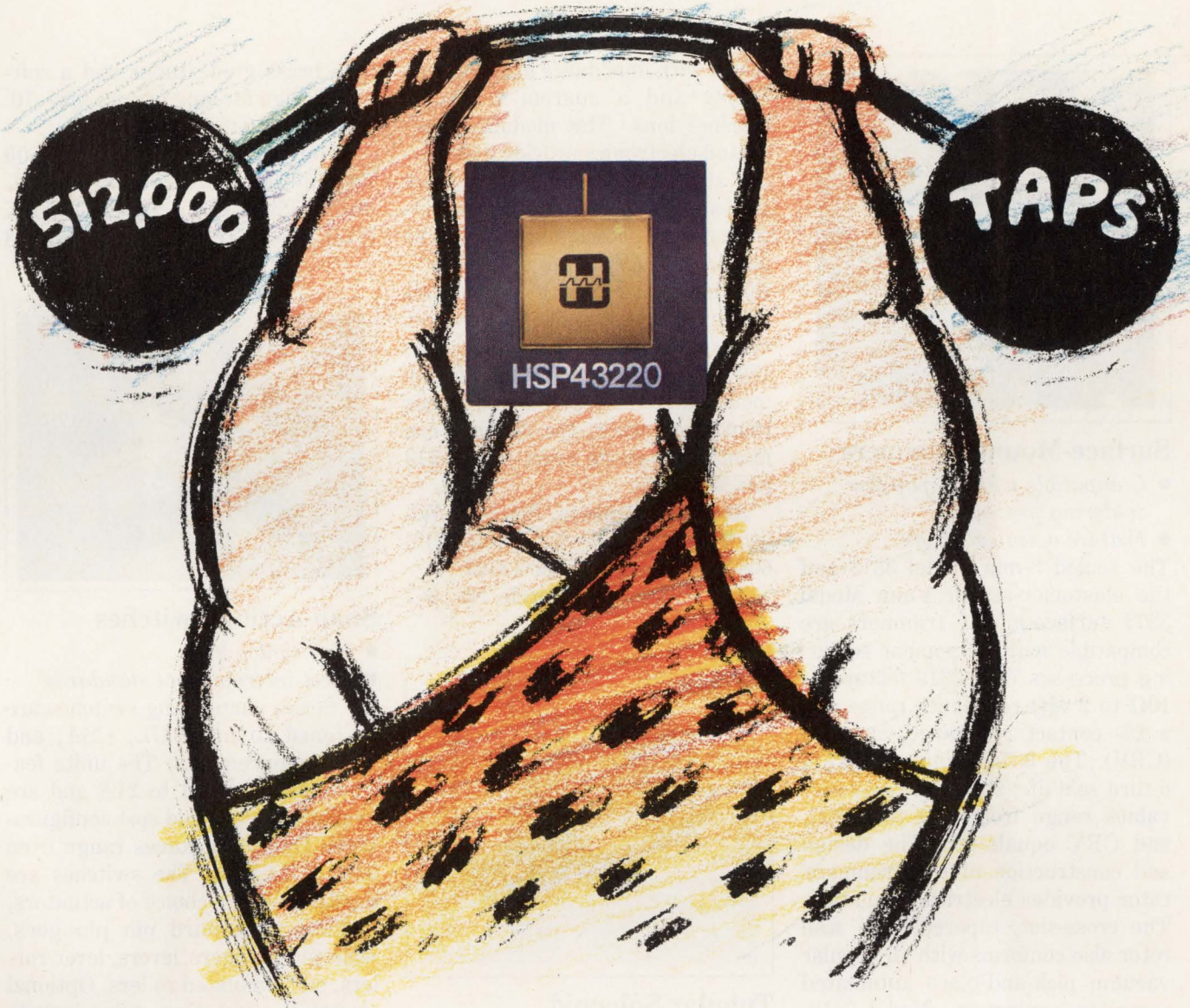
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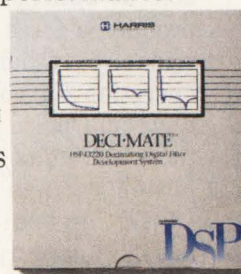
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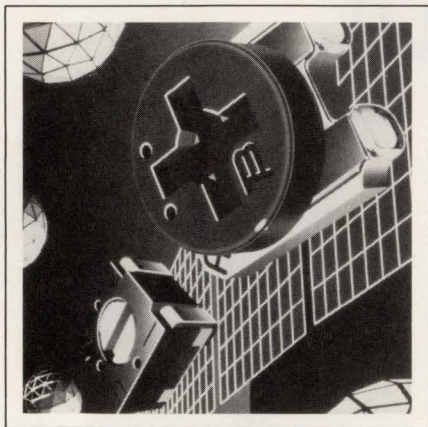
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Surface-Mount Trimmers

- Compatible with all popular soldering processes
- Feature a sealed design

The sealed 3-mm Model 3313 and the elastomer-sealed 4-mm Model 3374 surface-mount trimmers are compatible with all popular soldering processes. The 3313 features a 10 Ω to 2 M Ω resistance range and a 2% contact resistance variation (CRV). The 3374 trimmers have a 5-turn seal life; standard resistance values range from 10 Ω to 2 M Ω , and CRV equals 3%. The design and construction of the trimmers' rotor provides electrical insulation. The cross-slot, tapered, side wall rotor also conforms with all popular vacuum pick-and-place automated assembly equipment. Model 3313, from \$0.87; Model 3374, from \$0.60 (1000). Delivery, eight weeks ARO.

Bourns Inc., 1200 Columbia Ave, Riverside, CA 92507. Phone (714) 781-5071. TLX 676423.

Circle No. 366

Infrared Detector

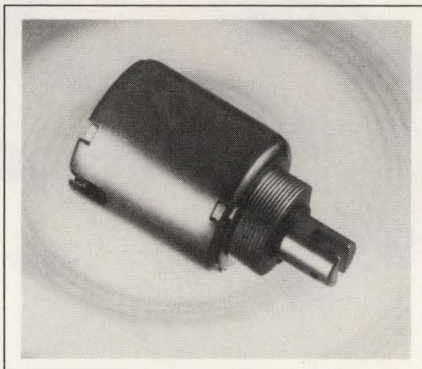
- Has a 180° sense field
- Includes digital electronics

The PIRM 180-200 infrared detector module has a 180° field of view. Developed for human-occupancy sensing applications, the module includes a curved, patterned, 6-element pyroelectric polymer film de-

detector with impedance matching circuitry and a custom 2-curtain Fresnel lens. The module's integrated electronics provide a 0V output at rest and a 5V output when activated. The custom lens and patterned pyroelectric film combine to provide 34 horizontal and 30 vertical (downward-looking) beams; this pattern allows the device to detect even small movements within its 180° field of view. When centrally mounted at the top of a wall rather than in a corner, the detector can monitor an entire room. \$10 to \$13 (OEM).

Atochem Sensors, Box 799, Valley Forge, PA 19482. Phone (215) 666-3500. FAX (215) 666-3509.

Circle No. 367



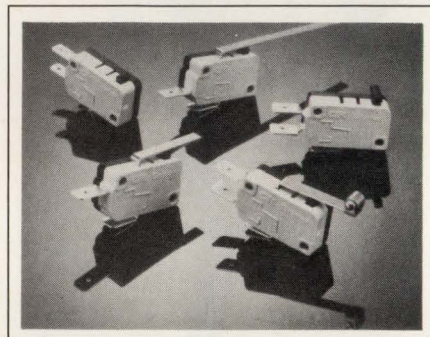
Tubular Solenoid

- Produces 16-lb force
- Various operating modes available

L-15 Series tubular solenoids have a 1.5-in. diameter and come in 1 $\frac{5}{8}$ - and 2 $\frac{3}{8}$ -in. lengths. Standard operating voltages are 6, 12, 24, and 110V dc; other voltages are available as options. The solenoids will produce a force of 16 lb min. Versions are available for push or pull operation for continuous, intermittent, and pulse duty cycle applications. All units are UL recognized. Power ratings range from 9 to 100W, and dielectric strength equals 1500V rms. The units fea-

ture brass guide tubes and a soft-stop design for long service life—10⁷ cycles. \$13 (OEM).

Liberty Controls Inc., 500 Brookforest Ave, Shorewood, IL 60435. Phone (815) 725-2241. FAX (815) 725-6571. Circle No. 368



Snap-Acting Switches

- Will switch 21A
- Meet international standards

TF Series snap-acting switches are designed to meet UL, CSA, and VDE requirements. The units feature ratings of 0.1 to 21A and are available in spdt and spst configurations. Operating forces range from 0.53 to 14.1 oz. The switches are available with a choice of actuators, including standard pin plungers, wide pin plungers, levers, lever rollers, and simulated rollers. Optional electrical connection styles include solder terminals, standard quick-connect, offset quick-connect, screw terminal, and pc-board terminal. From \$1. Delivery, eight weeks ARO.

Unimax, Box 152, Wallingford, CT 06492. Phone (800) 624-4308; in CT, (203) 269-8701. FAX (203) 265-5398.

Circle No. 369

Reed Relays

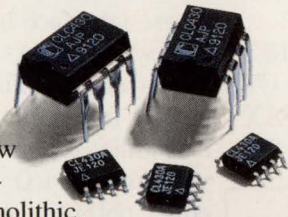
- Require only 33mW to operate
- Switch 10W loads

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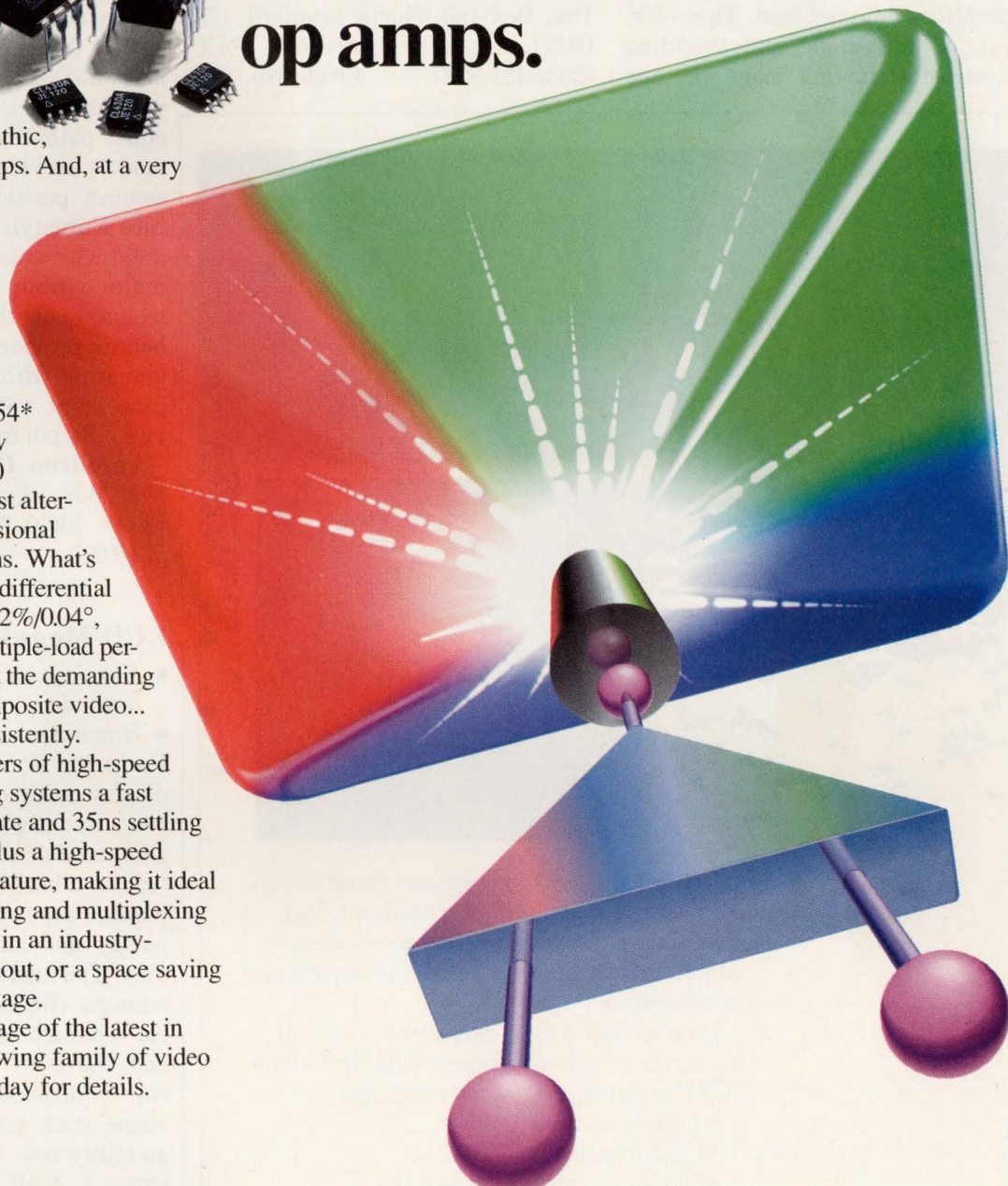
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reed contacts. The contacts will switch loads as high as 10W at 0.5A in 0.65 msec. The relays are designed to meet the environmental requirements of MIL-R-83516A. The relays' lifetime measures 10^7 operations at rated load. They offer optional coil diode and shielding (electrostatic and/or magnetic) and

are available in versions that have 5, 12, or 24V input ratings. From \$3.70 to \$8.90 for 1 Form-A and 2 Form-C versions, respectively (1000). Delivery, 10 to 12 weeks ARO.

Prime Technology Inc, EI&S Div, Box 185, North Branford, CT 06471. Phone (203) 481-5721. FAX (203) 481-8937. **Circle No. 370**

Interface Boards

- Have a 64-position capacity
- Provide a ribbon-cable to discrete-wire interface

These interface boards simplify circuit wiring tasks in industrial control systems. The boards are designed for mounting on DIN rails, a chassis, or on panels. They provide direct I/O connections with equal potential on both sides. Ten models provide from 10 to 64 interconnect positions. The boards feature Eurostyle terminal strips with a 45° wire-entry configuration. The male ribbon cable connectors mounted on the other side of the boards provide reliable mating and unmating with IDC (insulation displacement connector) socket devices. 34-pin model, \$30.

Vernitron Corp, Beau Products Div, Box 10, Laconia, NH 03247. Phone (603) 524-5101. FAX (603) 524-1627. **Circle No. 371**

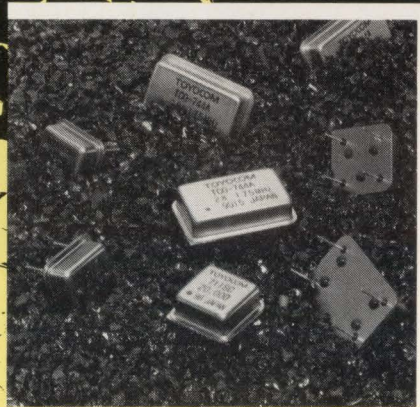
LCD Module

- Employs super twisted nematic technology
- Has a 240×64-dot display

Featuring a negative transmissive display with cold-cathode fluorescent backlighting, the EG-2405 LCD module displays white characters on a blue background. It incorporates super twisted nematic technology and has a 240×64-dot display. The module will display alphanumeric characters as well as special characters, graphs, patterns, and charts. It features sequential row multiplexing, which allows a single data string to be input for an entire row. The module also features a 4-bit, chip-enable data-transmission system that allows data to be input directly to a specific driver rather than being shifted in. The module features a 10:1 contrast ratio and a 0.53×0.53-mm dot pitch. \$105.

Epson America Inc, Box 2842, Torrance, CA 90505. Phone (213) 787-6300. **Circle No. 372**

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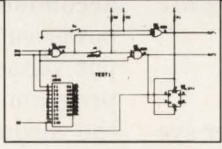
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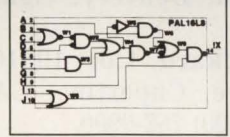
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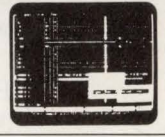
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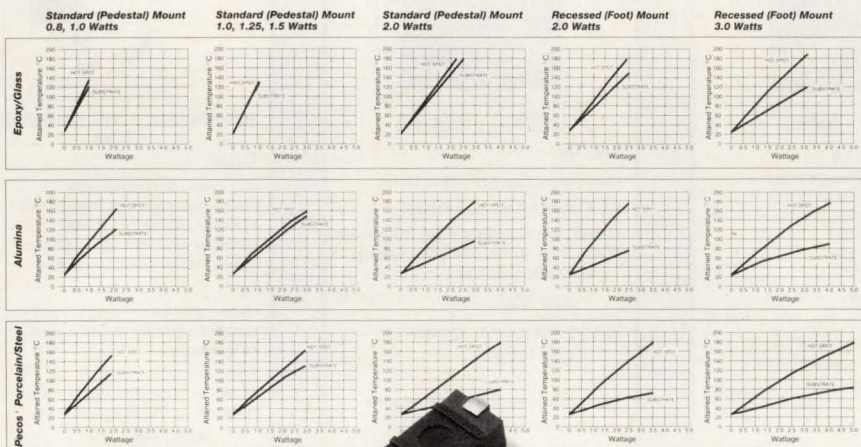
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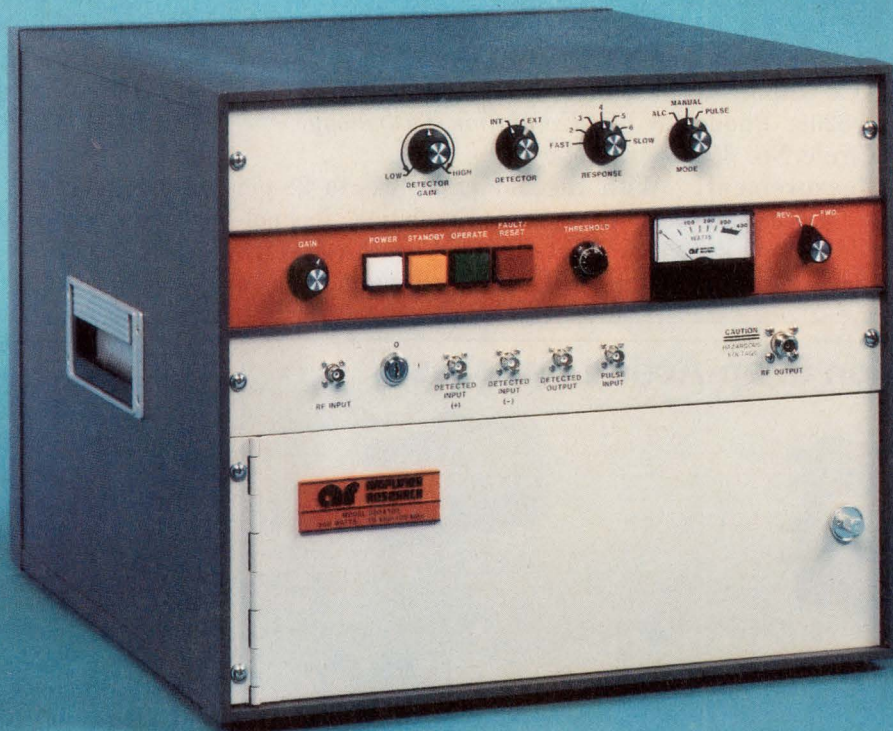
Timer/Counter

- Stores 2000 readings/sec at full resolution
- Resolves single-shot intervals to 500 psec

The PM 6680 timer/counter resolves single-shot intervals as brief as 500 psec. In direct mode, it can measure frequencies as high as 225 MHz. A prescaler extends the frequency range to 2.7 GHz. The unit can make a 9-digit-resolution frequency reading in 1 sec and can store 2000 readings/sec in its internal memory (5000/sec with reduced resolution). These abilities make the counter a possible alternative to time-interval analyzers in some applications. Among the unit's unusual features are its ability to accumulate the difference in counts between its A and B inputs; its inclusion of terminals that you can connect to a scope to view the input-amplifier outputs (useful for setting probe compensation); and its auto-trigger ONCE mode, which shuts off the time-consuming autotrigger

text continued on pg 180

CIRCLE NO. 87



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John Fluke Mfg Co Inc, Box 9090, Everett, WA 98206. Phone (206) 347-6100. **Circle No. 356**

Philips Test & Measurement, Bldg TQIII-4, 5600 MD, Eindhoven, the Netherlands. Phone local office. **Circle No. 357**

EEPROM And PLD Programmers

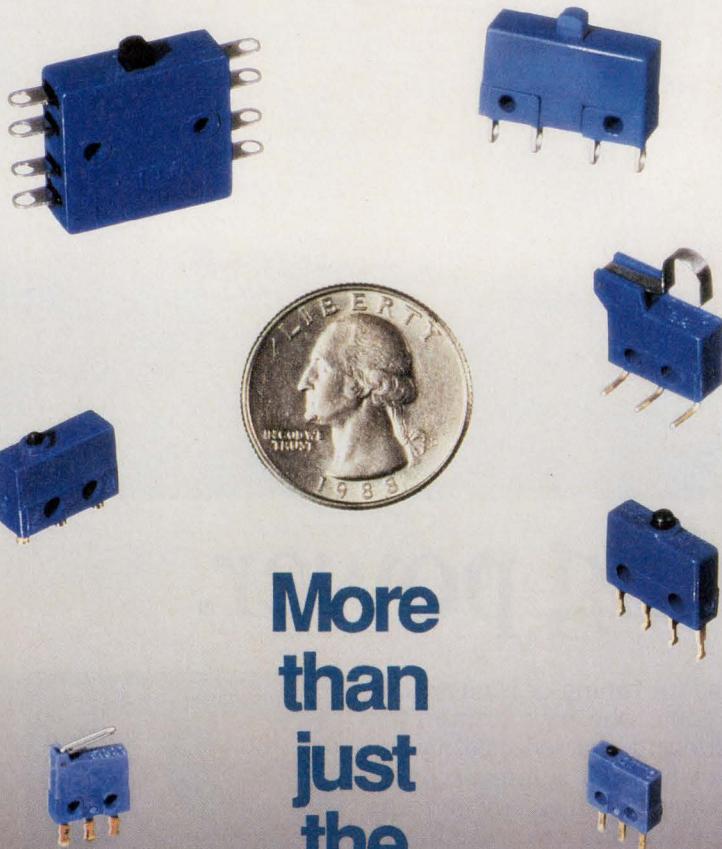
- Program AMD Mach130
- Use Emulation Technology adapter

With the aid of an 84- to 28-pin adapter from Emulation Technology (Santa Clara, CA), the CP-1128 and PLD-1128 programmers can

program the AMD Mach130 high-density PLD. The PLD—which has 64 I/O pins and uses CMOS EEPROM technology—is packaged in an 84-lead, plastic leaded chip carrier. Current owners of the programmers can download the software they need to support the PLD by calling the programmer vendor's bulletin-board system. The only cost for the software update is that of the phone call. CP-1128, \$1295; PLD-1128, \$995; socket adapter (Emulation Technology AS84-28-01P-6YAM), \$275.

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Circle No. 803

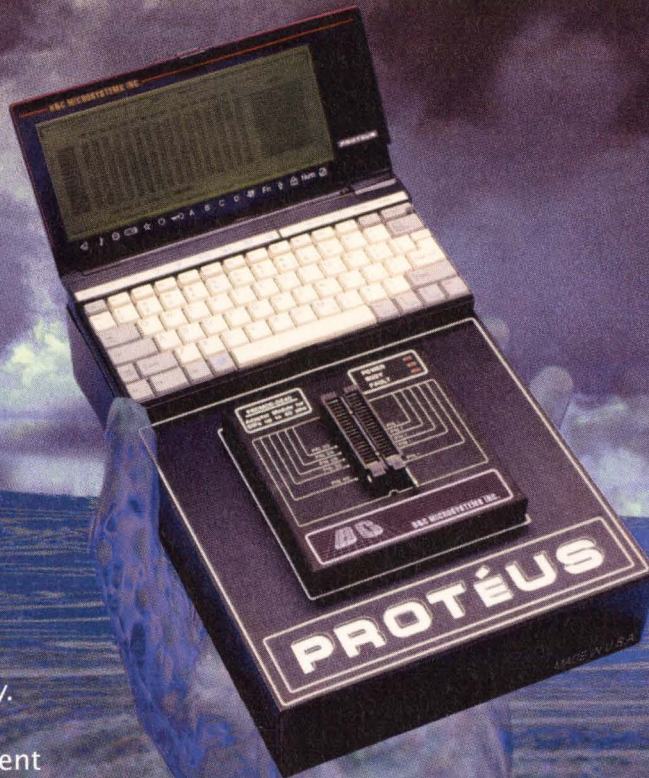
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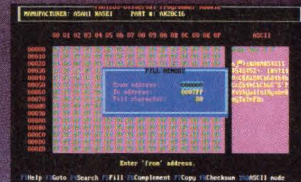
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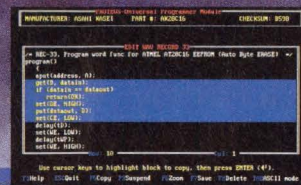
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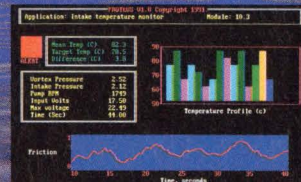
PROGRAMMER



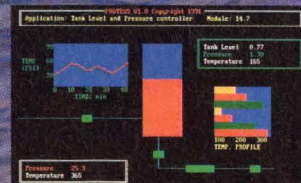
ALGORITHM DEVELOPMENT



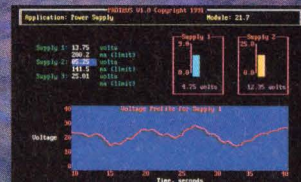
DATA LOGGER



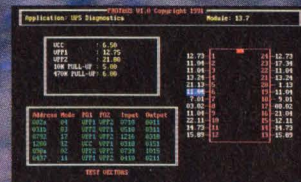
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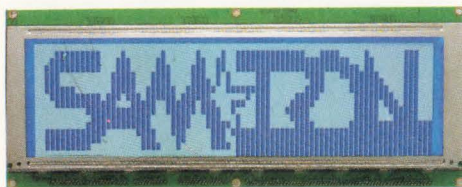
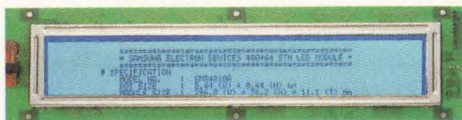
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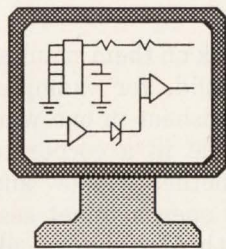
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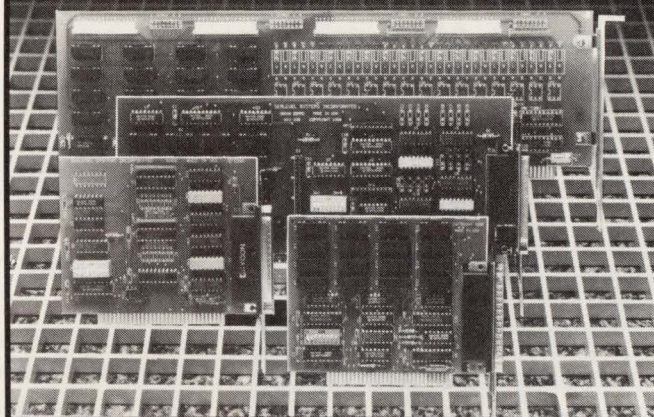
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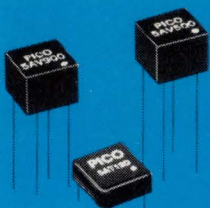
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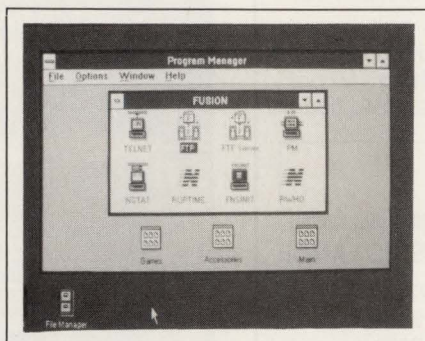
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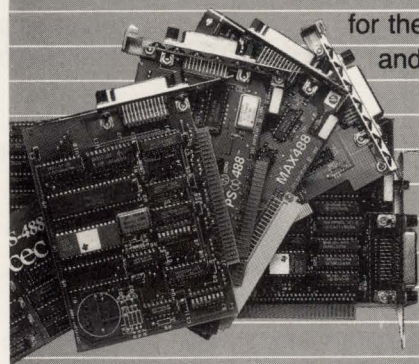
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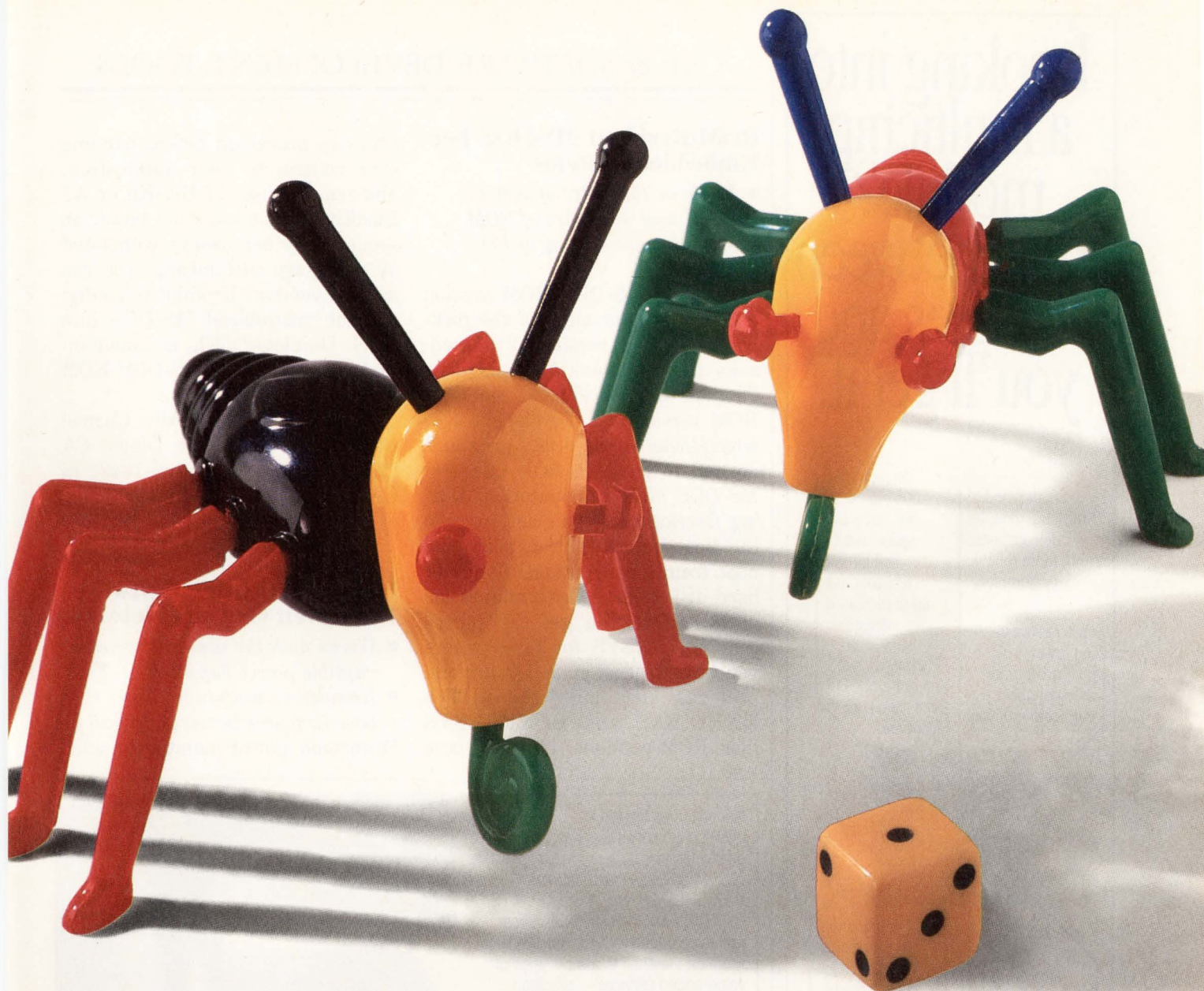
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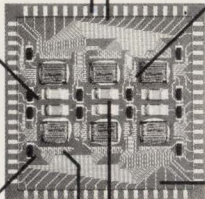
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3.5-Inch Disk Drive Comparison Criteria	Maxtor Cheyenne 7130A	Conner Model 30104
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Seek time	15ms	19ms
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ware works with the vendor's line of UPSs and Novell or Unix network operating systems. Whenever power problems occur, the software broadcasts warning messages to all users on the network. When the UPS battery becomes severely depleted, the software broadcasts a second warning to allow users to save work before shutdown. If the battery becomes totally depleted, the software automatically saves any open-network files and safely shuts down the system. The software also keeps a historical log of power failures to assist in determining trends or causes. Novell version, \$99; Unix/Xenix version, \$149.

Upsonic, 1392 Industrial Dr, Tustin, CA 92680. Phone (800) 877-6642; in CA, (714) 258-0808. FAX (714) 258-0811. **Circle No. 364**

Mixed-Signal Simulator For Sun Workstations

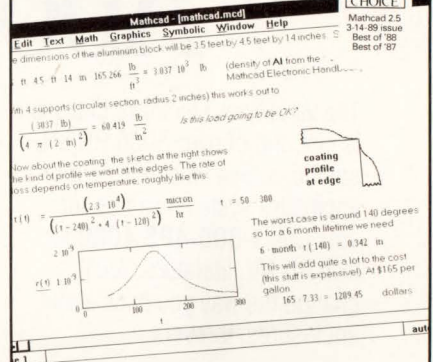
- Includes a full-featured Spice implementation
- Simulates mixed logic and analog designs

The Mixed Signal Simulator (MSS) is one of four packages that make up the vendor's CAE tool set called Contec CAE (CCA). MSS can simulate mixed-signal ASIC, pc-board, and multichip-module designs; you achieve speed by building suitable behavioral models for the digital and analog components. The package includes a functional ContecSpice simulator; the vendor has enhanced version 1.1 of this simulator to include faster, more accurate algorithms and to fix known Spice3C1 bugs. MSS provides support for uncoupled, lossless lines and comes with analog behavioral models for both analog and digital devices as well as libraries of discrete devices that include both analog and digital ICs. MSS currently runs on Sun workstations. \$20,000.

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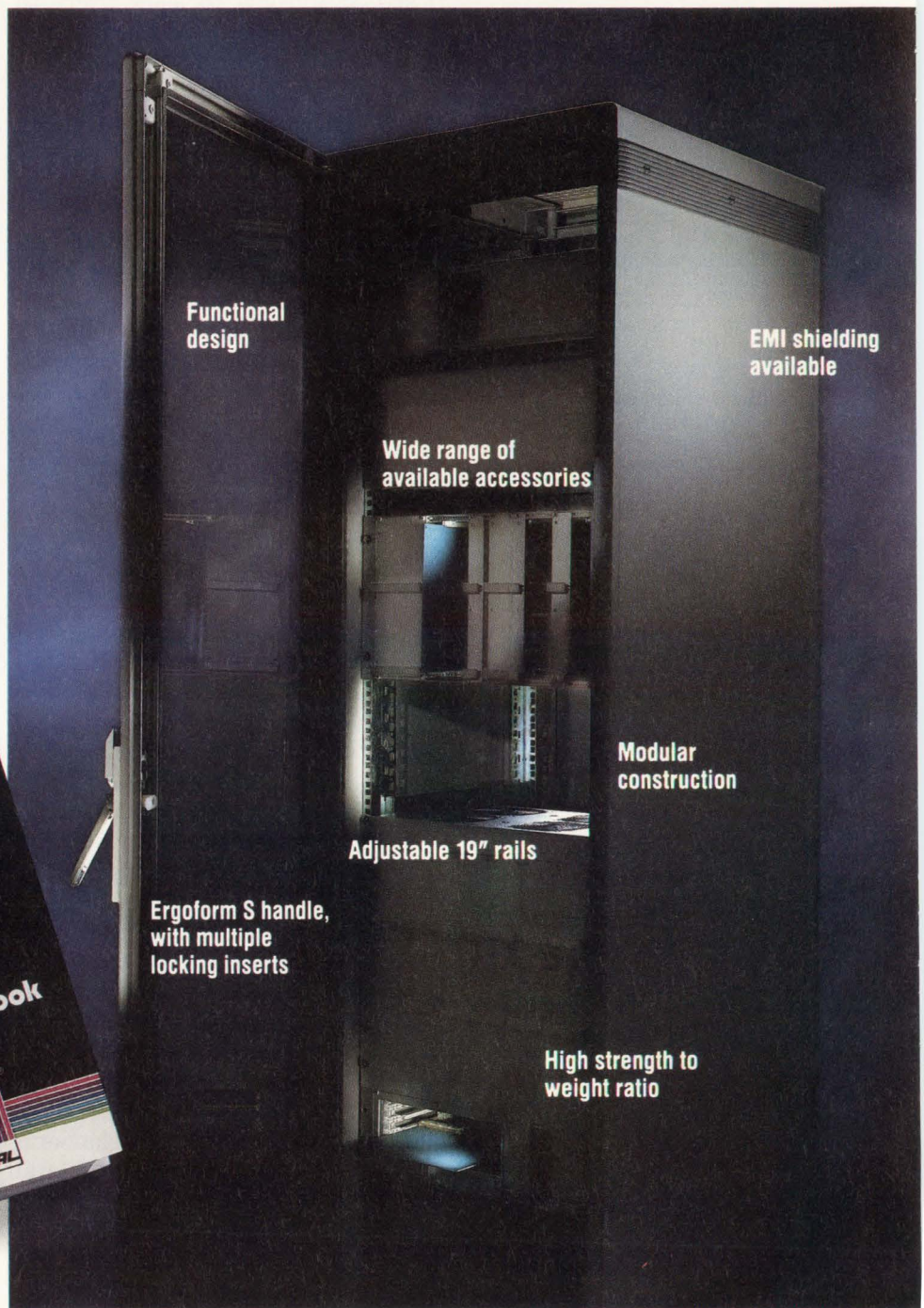
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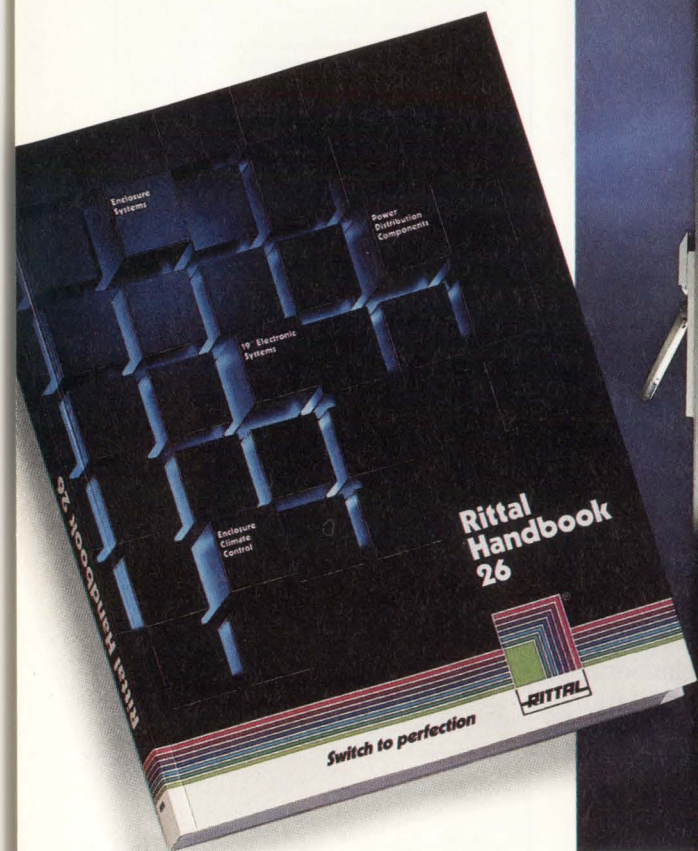
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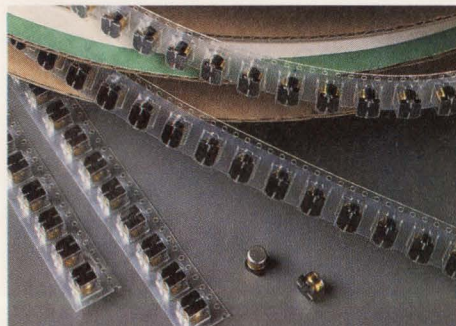
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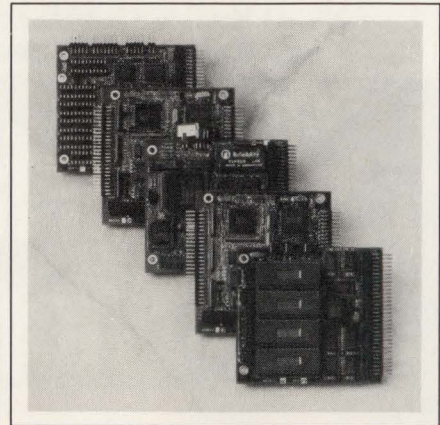
COMPUTERS & PERIPHERALS

Embedded Control Modules

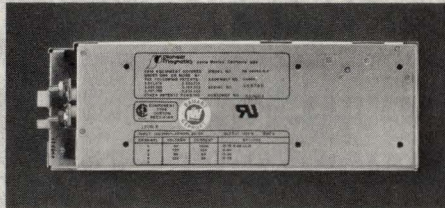
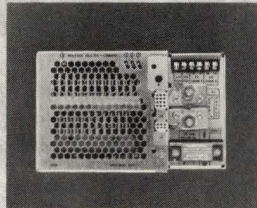
- Have IBM PC-compatible CPU and five expansion blocks
- Use 16-MHz Am286LX CMOS μ P

The Coremodule family has added an IBM PC-compatible CPU mod-

ule and five peripheral expansion modules. All the modules measure 3.6x3.8 in. and plug together to provide building blocks for embedded control applications. The CPU module, the Coremodule/286, uses a 16-MHz AMD Am286LC CMOS



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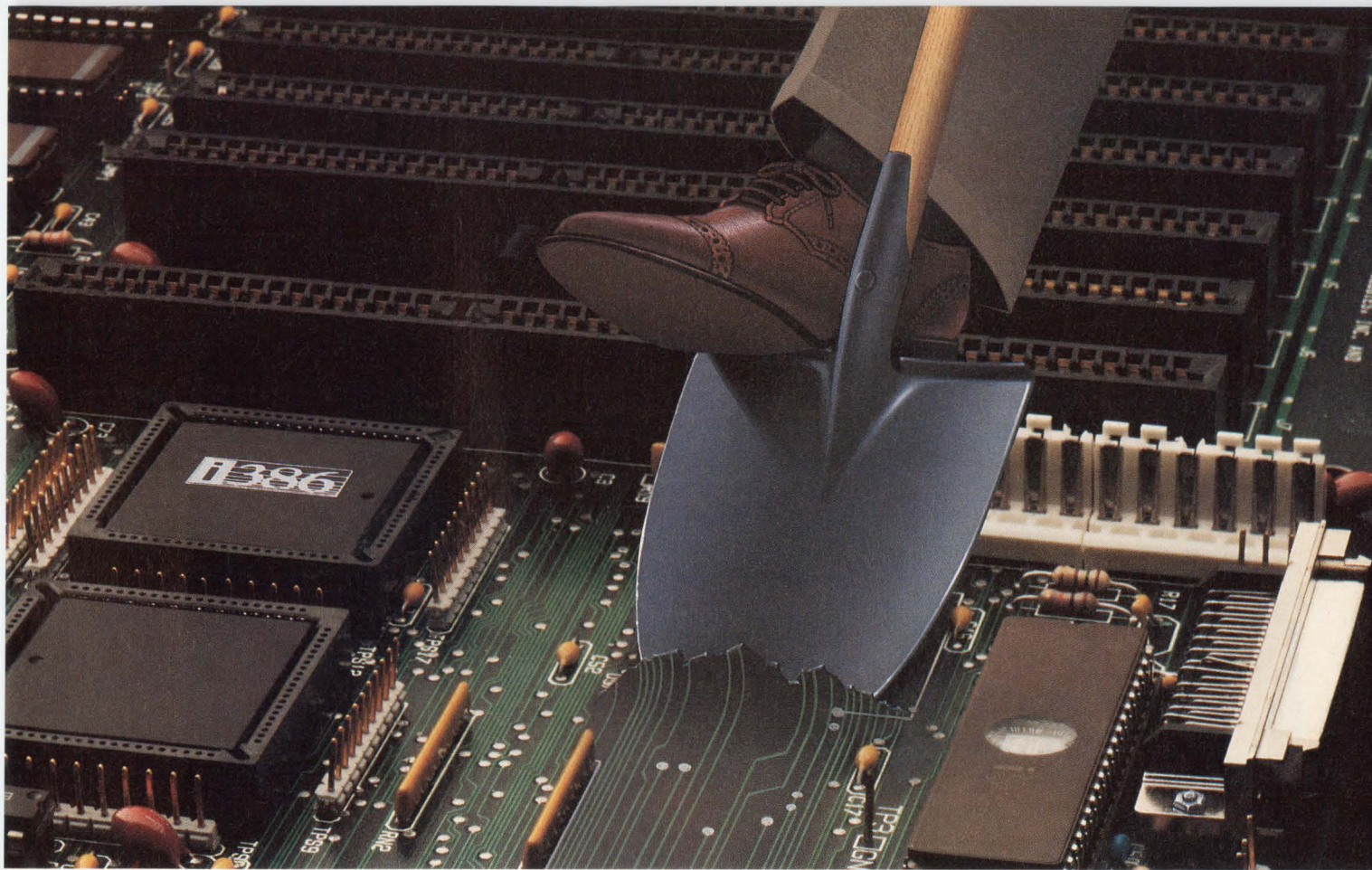
μ P and has all the functions of an IBM PC/AT mother board. Fully configured, the CPU module has DMA and interrupt controllers, timers, and sockets for as much as 4M bytes of RAM. The module also has an Award ROM BIOS, a bidirectional printer port, an RS-232C port, and a keyboard interface. The peripheral expansion modules consist of a super VGA graphics display, an Ethernet controller, a solid-state disk unit, an ISA bus to SCSI adapter, and an IDE interface. CPU module, \$180; expansion modules, \$65 to \$149 (1000).

Ampro Computers Inc, 990 Almanor Ave, Sunnyvale, CA 94086. Phone (408) 522-2100. FAX (408) 720-1305. **Circle No. 359**

Embedded Multiprocessor

- Features four i860 CPUs on 9U VMEbus board
- Uses 480M-byte/sec crossbar switch between nodes

The MC860VS device is an embedded multiprocessor board for the VMEbus. The 9U board has as many as four compute nodes, each consisting of a 40-MHz i860 CPU, as much as 16M bytes of distributed memory, and a data switch that connects the CPU or distributed memory to a central crossbar switch. The 480M byte/sec crossbar switch has six ports: Four of the crossbar ports connect to the



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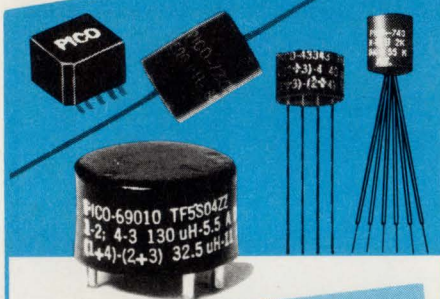


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board's respective compute nodes; one port connects to a 64-bit, 160M-byte/sec bus that communicates with the VMEbus; and one port connects a 160M-byte/sec Inter-board Bus that provides communications between multiple MC860VS boards. You can install as many as eight boards in a VMEbus system, which couples as many as 32 i860 compute nodes together. Running on the company's MC/OS release 2, the maximum processing power is 2.5G flops. Board with four i860 CPUs and 8M to 16M bytes of RAM, \$24,300 to \$38,300 (OEM qty).

Mercury Computer Systems Inc., 600 Suffolk St, Lowell, MA 01854. Phone (508) 458-3100. FAX (508) 458-9580. **Circle No. 360**

Transputer Board

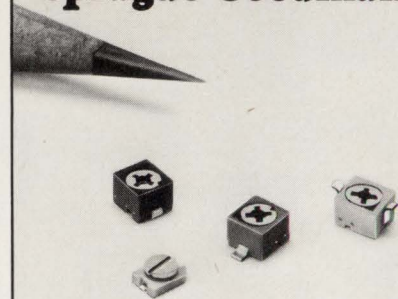
- Contains a T222 Transputer
- Has a prototype section, which interfaces to the Transputer

The TPM-EXP Transputer board for developing custom hardware has a Transputer node and a prototype section. The Transputer node has a T222 Transputer, which provides 10 MIPS, and a communications link that has a 9M-byte/sec bandwidth. The node also has a real-time clock and 64k bytes of static RAM. A lithium battery backs up the time and memory in industrial applications. A watchdog timer on the node monitors the Transputer's status. The prototype board operates on the Helios distributed operating system, Express tool kit, and Multitool Transputer development-system software. The board also operates with several cross-compilers running under MS-DOS, Apple O/S, and Sun Unix. \$1280.

Parsytec Inc., Bldg 9, Unit 60/61, 245 W Roosevelt Rd, West Chicago, IL 60185. Phone (708) 293-9500. FAX (708) 293-9525.

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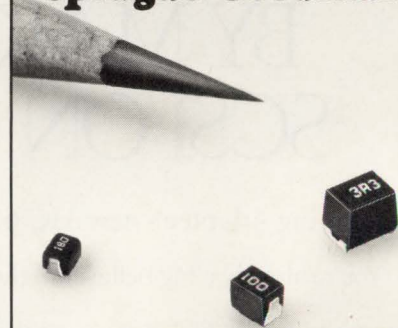
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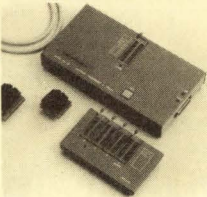
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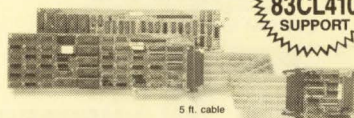
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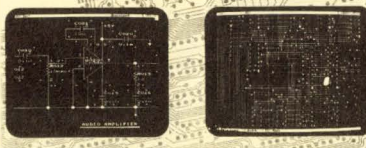


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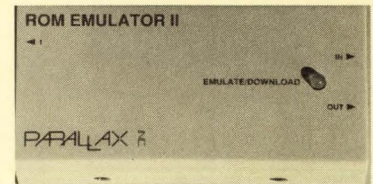
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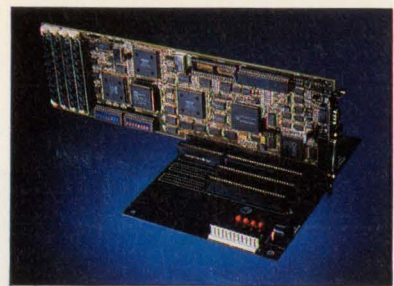
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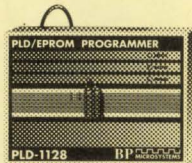
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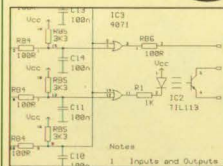
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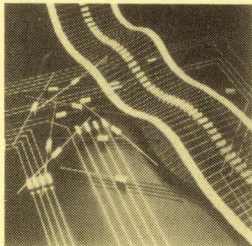
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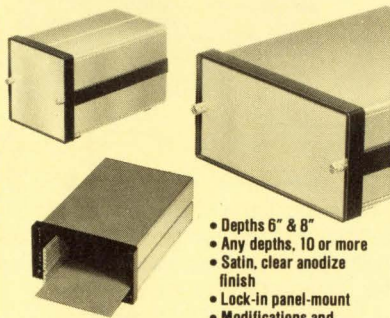
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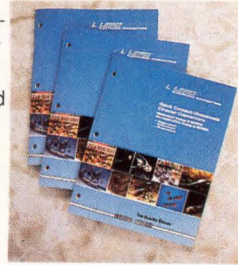
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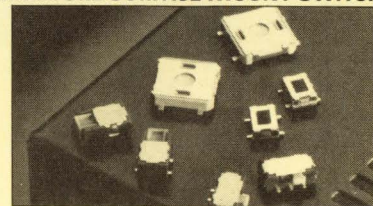


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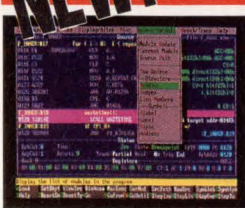
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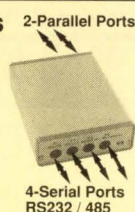
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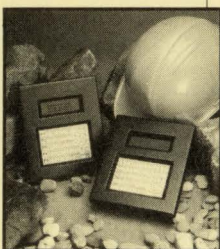
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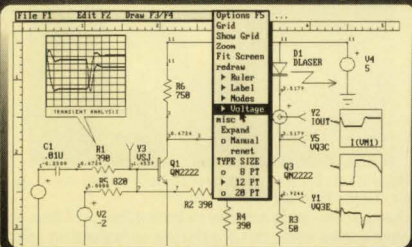


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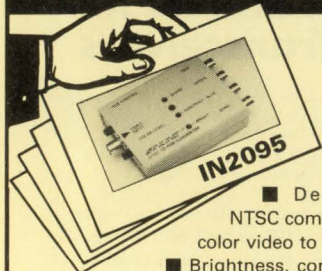
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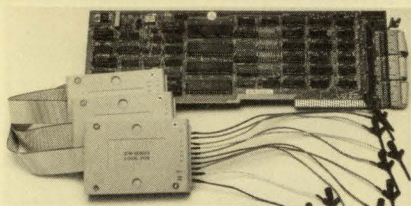
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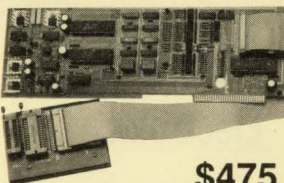
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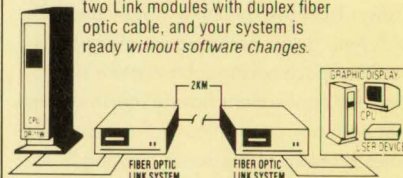
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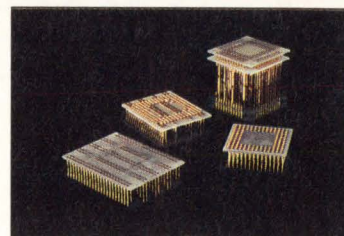
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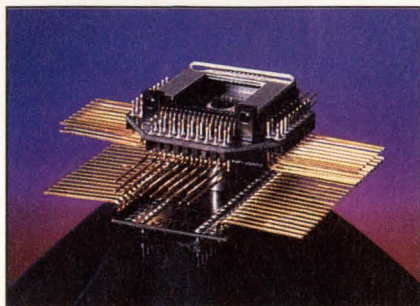
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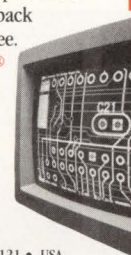
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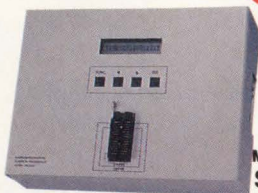
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Magazine Edition	Sept. 16	Aug. 21	DSP/Microprocessors, ICs & Semiconductors, CAE/ASICs, Environmental Engineering • Software
News Edition	Sept. 19	Aug. 29	RISC/ICs, Computers**, Regional Profile: Florida**
Magazine Edition	Oct. 1	Sept. 5	Computers & Peripherals/Networks, DSP Chip Directory • ICs & Semiconductors/Memory Technology, Instrumentation
News Edition	Oct. 3	Sept. 13	ICs & Semiconductors, Multimedia**
Magazine Edition	Oct. 10	Sept. 19	Test & Measurement Special Issue, Oscilloscopes, VXI Board Directory • CAE/ASICs, Sensors & Transducers •
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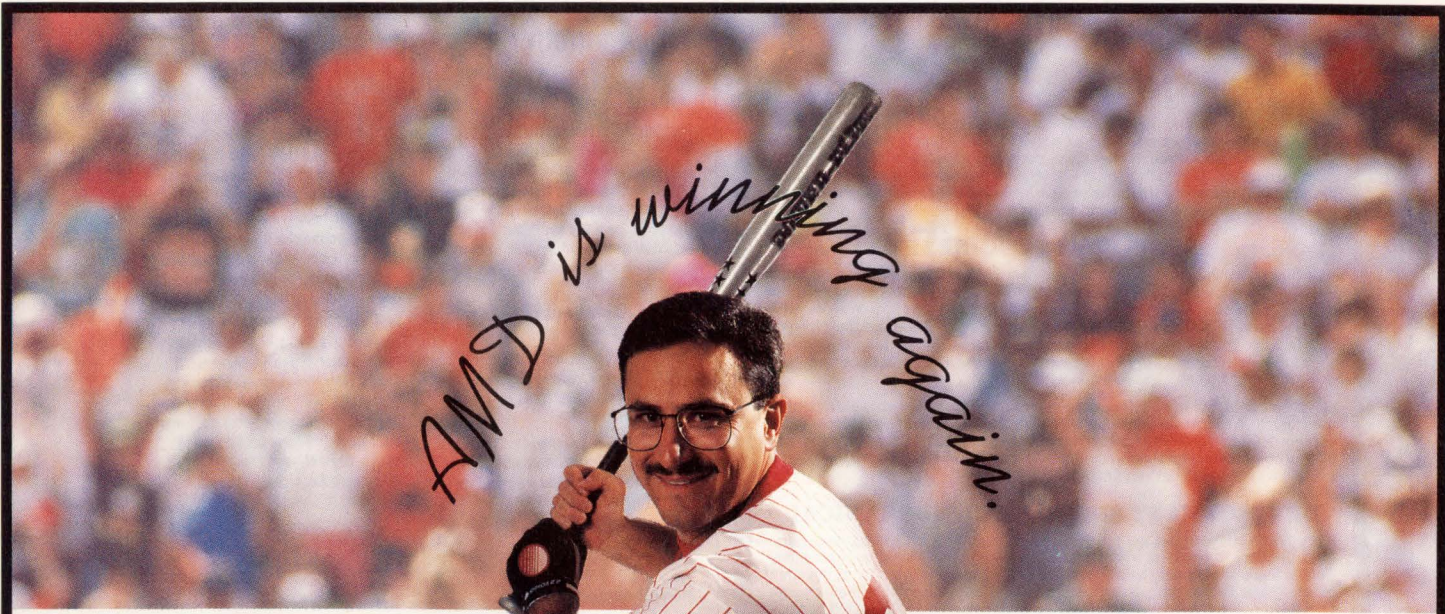
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Requirements include: BSME with a minimum of 5 years mechanical design experience in new product development area; proven project management experience; experience with CAD systems (Autocad, Automatrix, or Aries preferred); basic understanding of statistics, electronics, and optics (light emitting diodes, photodetectors). Medical device background preferred.

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We are looking for an experienced Design Assurance Engineer to support Oximetry product lines. This person will be involved with product development from design conceptions through product release. Acting as the customer quality advocate, the Design Assurance Engineer will be a key member of the project leadership teams responsible for setting customer quality standards and continuing to improve performance against those standards. He/she will act as the liaison with Quality Assurance to ensure regulatory compliance, and instill a quality focus in the development teams.

Requirements include: BSEE or BSME with a minimum of 8 years related design experience including significant expertise in electrical/mechanical design. Some clinical background is preferred.

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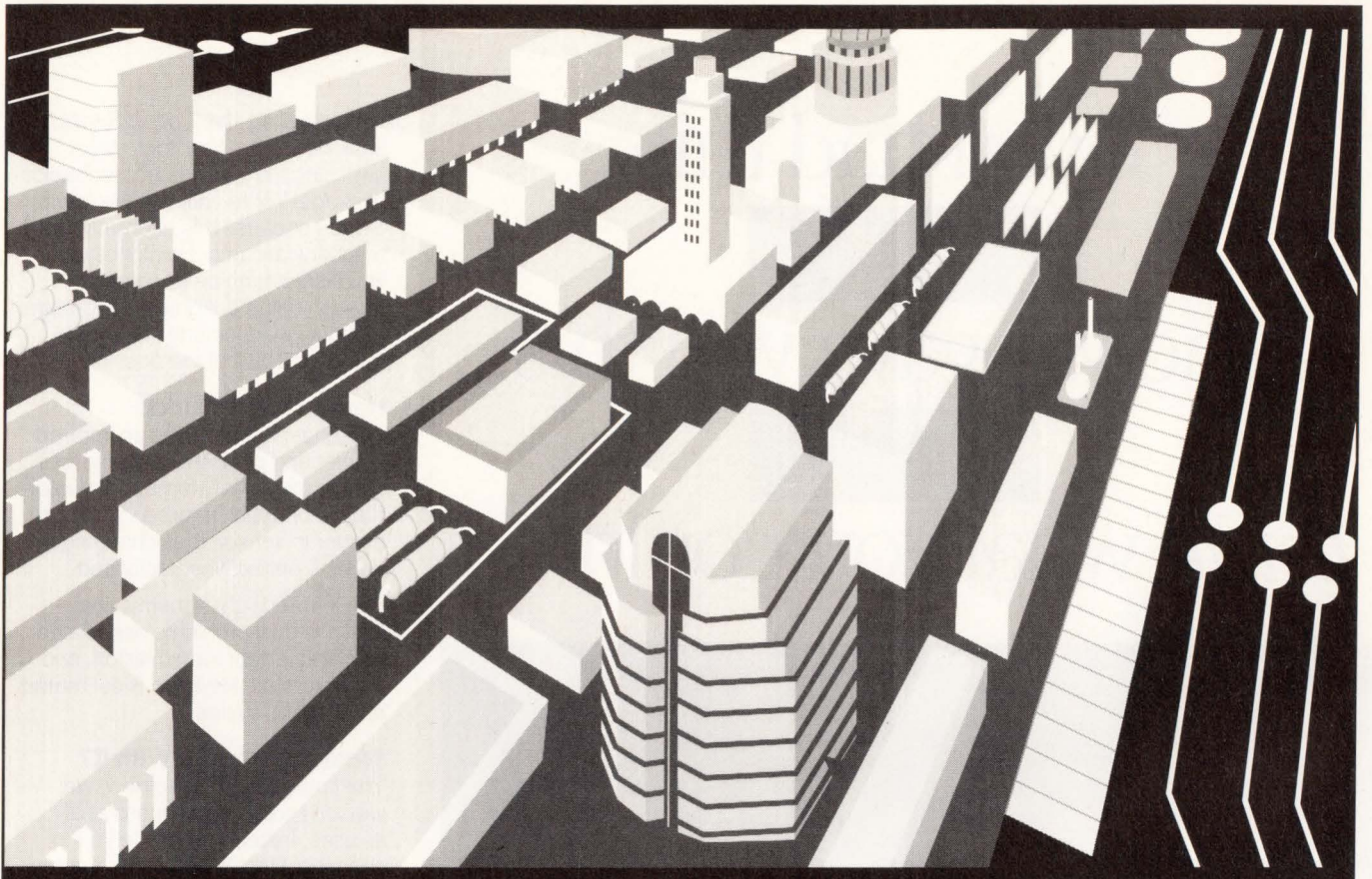
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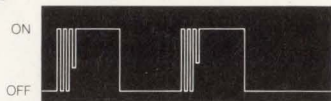
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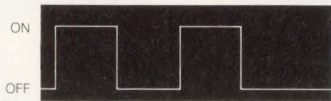


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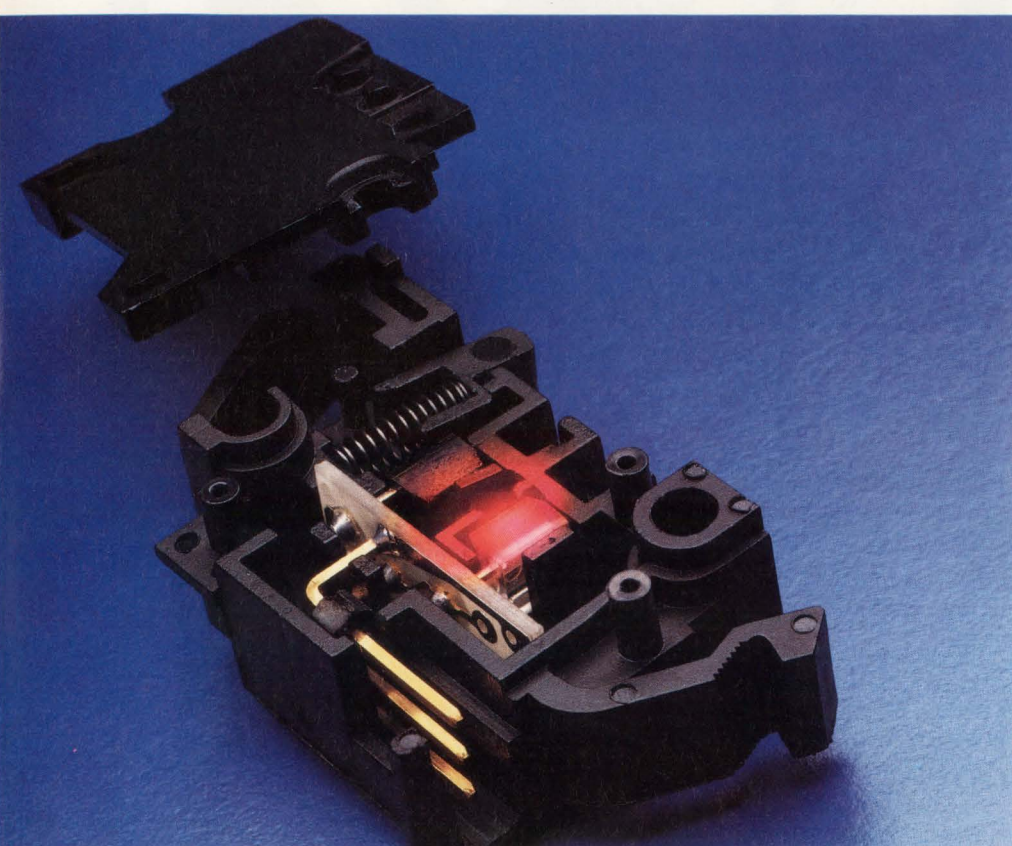
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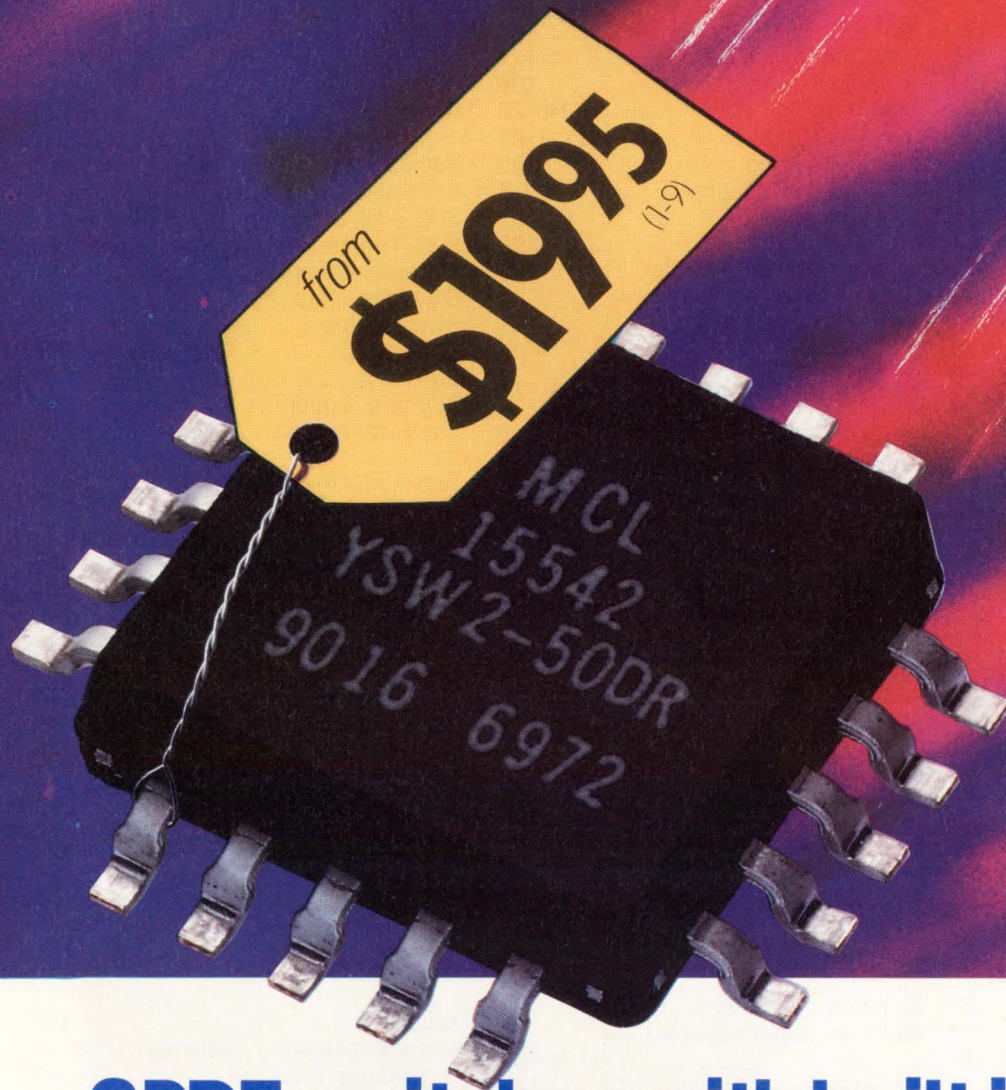


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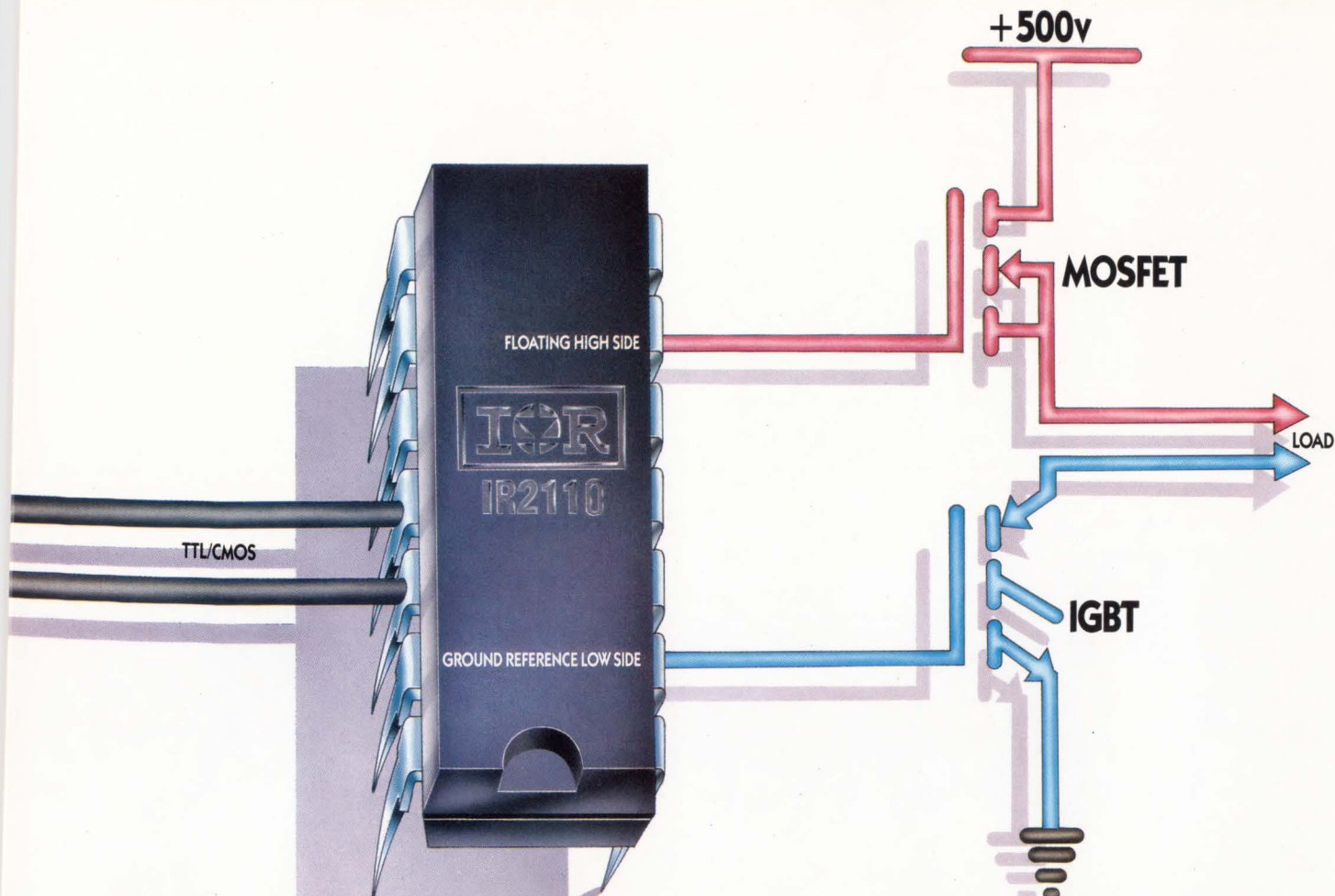
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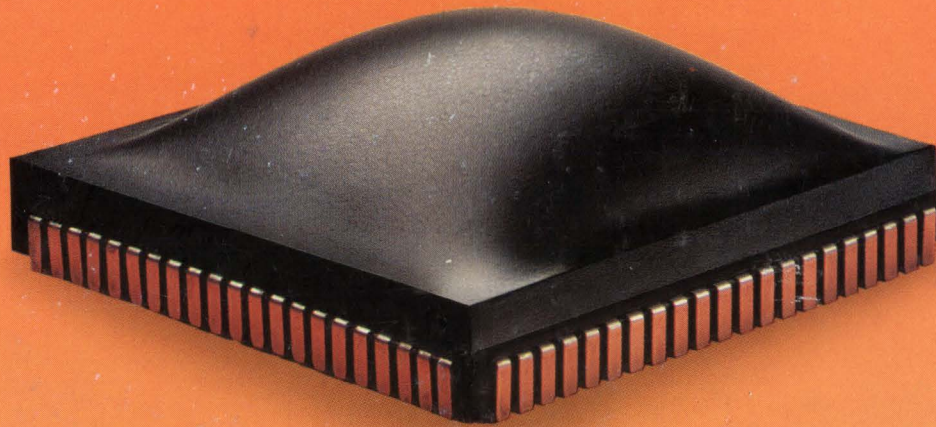
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