March 31, 1994

EDN®

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

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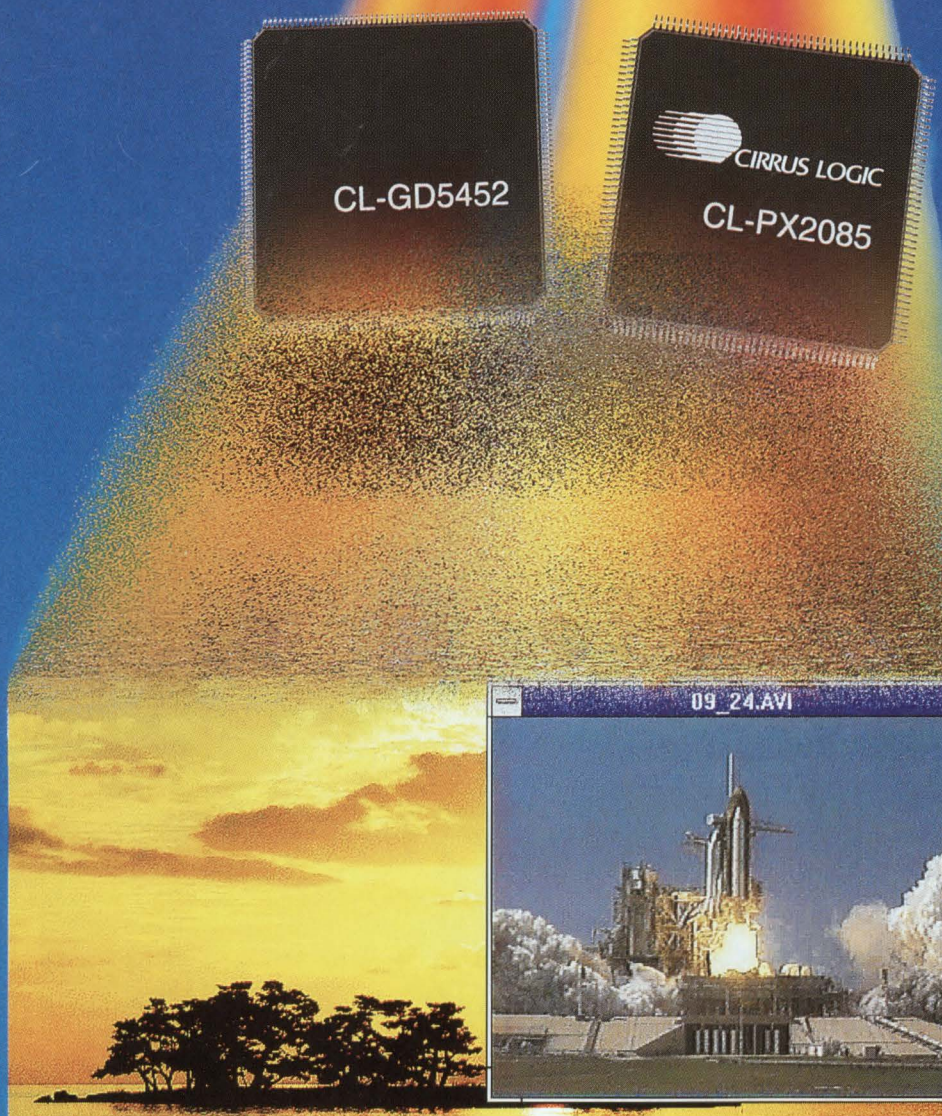

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The first multiprocessor setup with RISC and DSP on one chip pg 67

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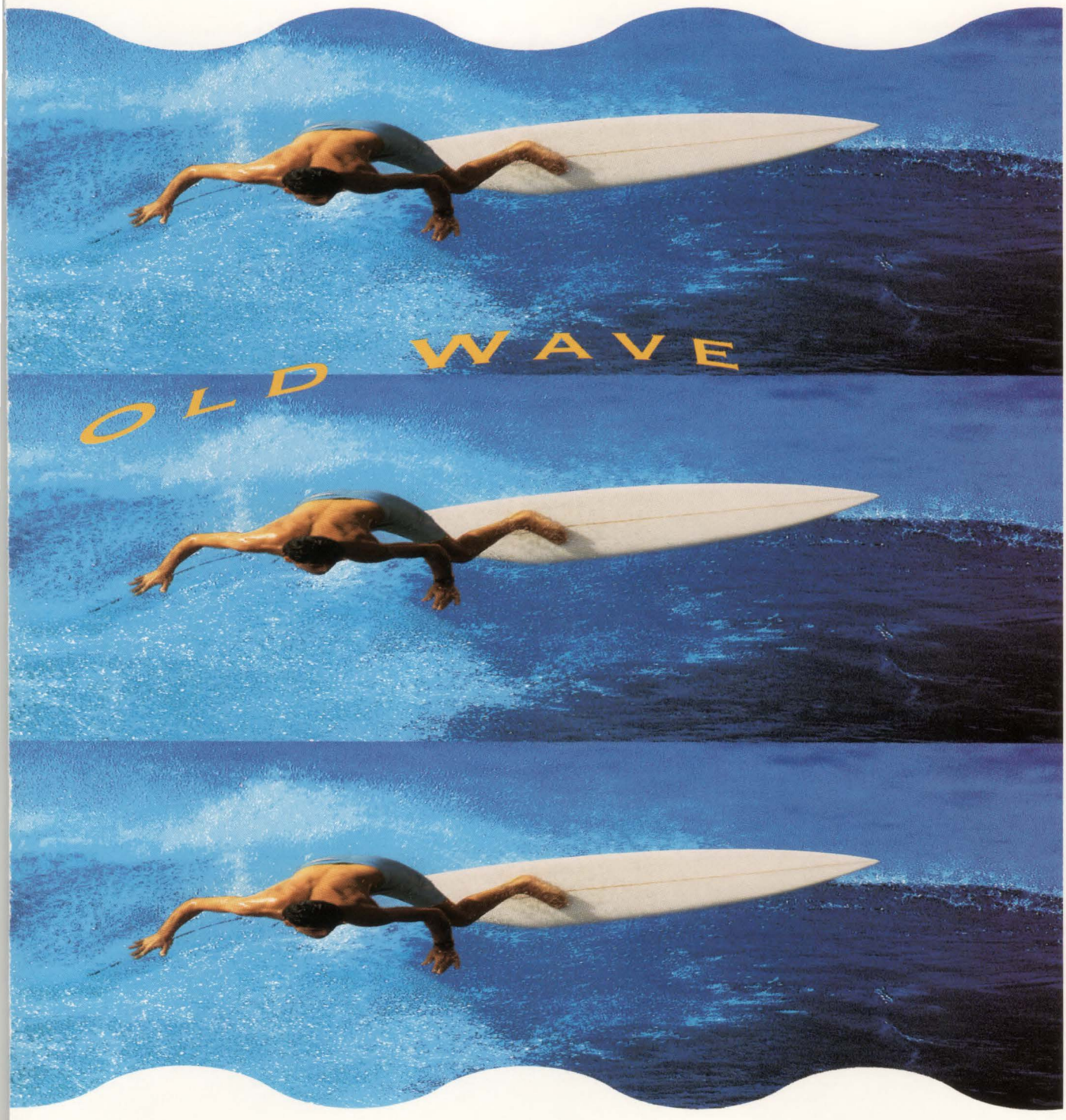

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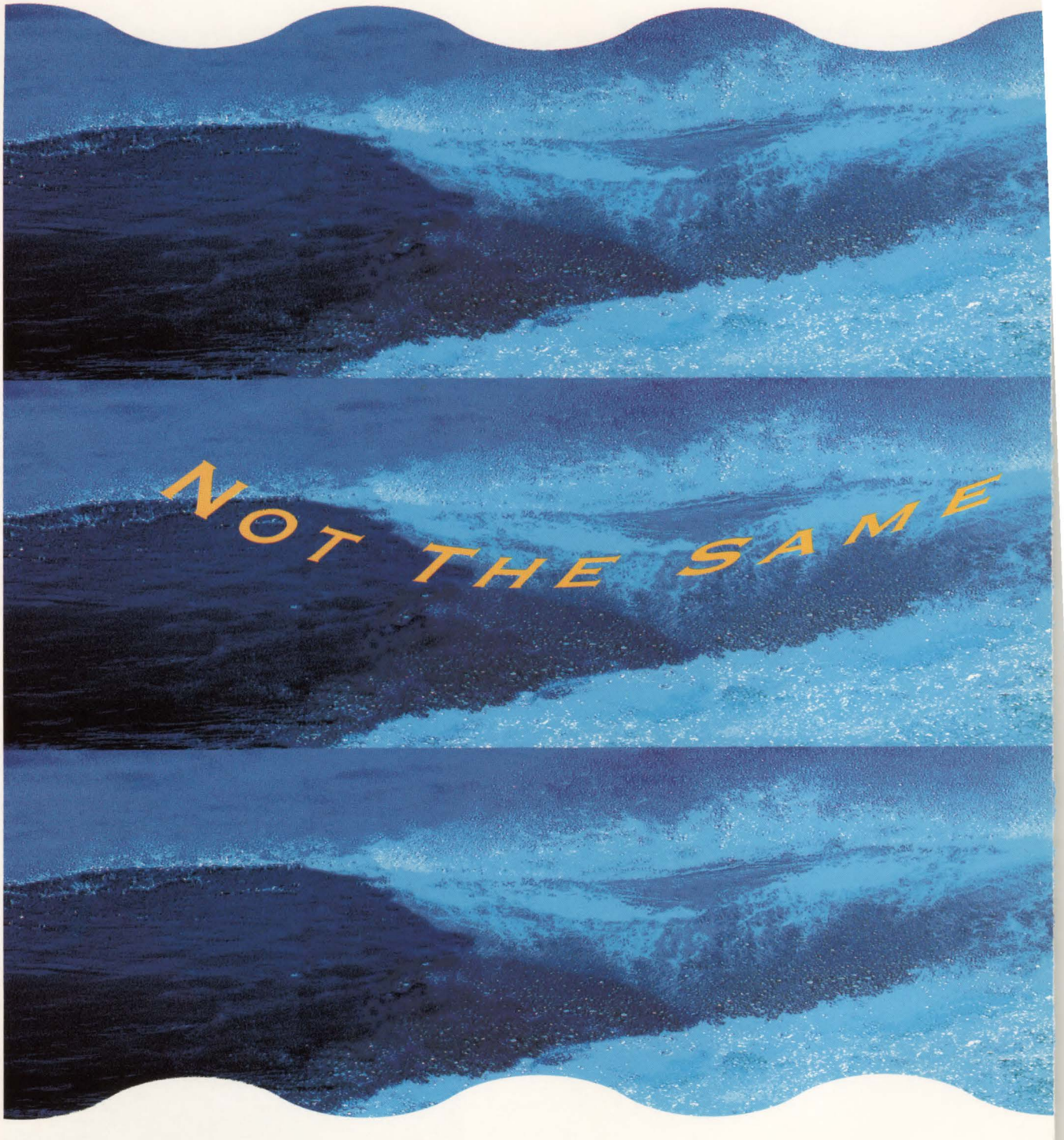

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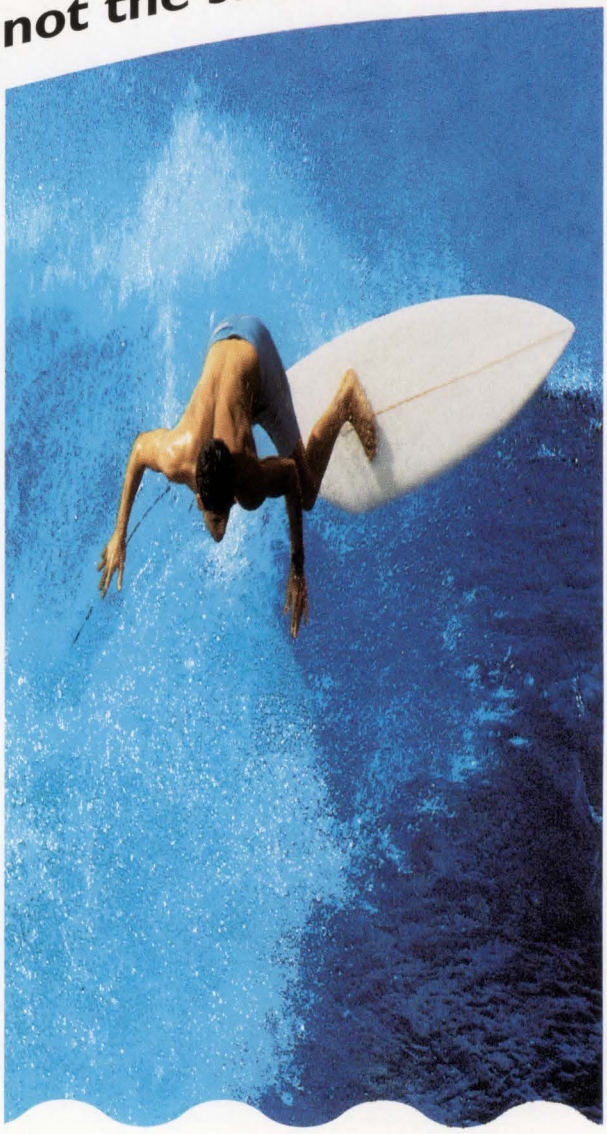

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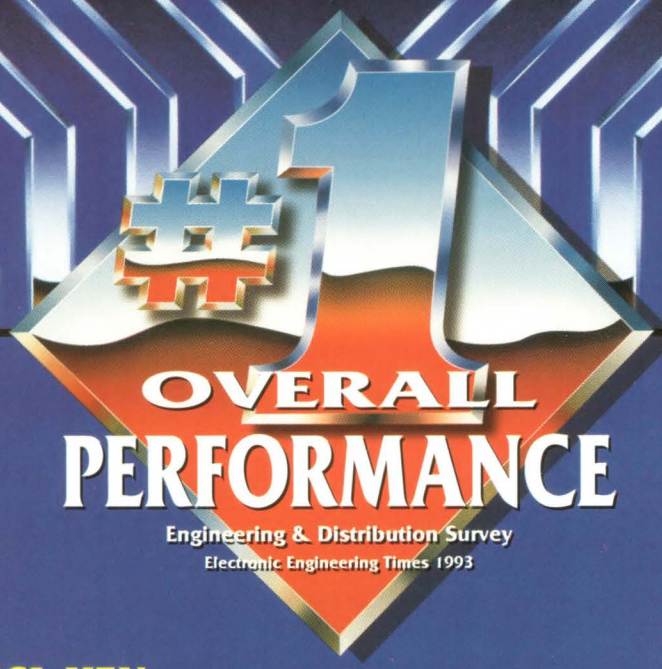

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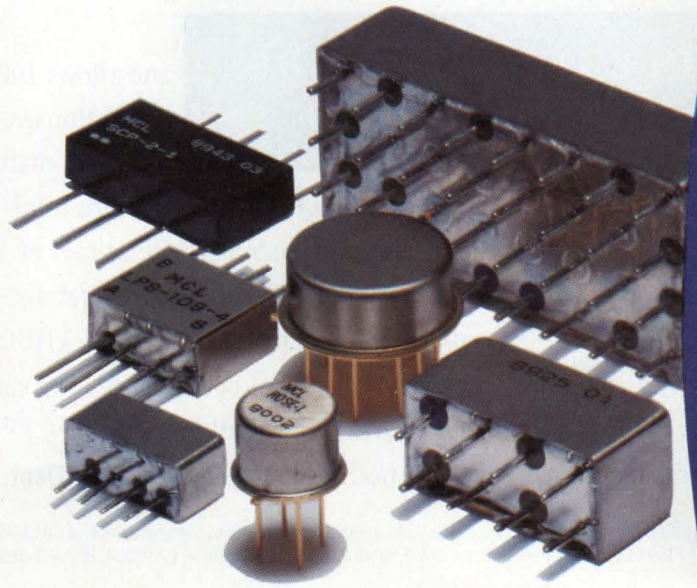

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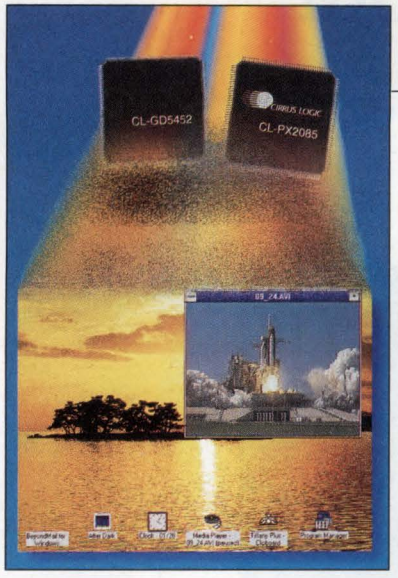

On the cover: New video ICs produce images on a PC that have the resolution and motion quality of television video. See Gary Legg's Special Report, beginning on **pg 38.** (Photo courtesy Cirrus Logic Inc)

SPECIAL REPORT

New chips give PCs TV-quality video 38

If you think video on a desktop computer has to mean small images and jerky motion, think again. The latest video chips can fill a PC's entire screen, or any part of it, with smooth, realistic motion. —*Gary Legg, Senior Technical Editor*

DESIGN FEATURE

The right μP simplifies using induction motors to propel electric cars 48

Induction motors are inexpensive and reliable. Controlled by an appropriate μP, a PWM inverter powered by a single battery can generate waveforms that appear to such motors as the 3-phase, variable-voltage, variable-frequency sine waves they need for speed control.—*Jeff Baum and Ken Berringer, Motorola Inc*

DESIGN IDEAS

PLDs implement delay lines 57
DAC and μP implement hardware window generator 58
LC oscillator has 1% THD 58
Low-cost converter drives fluorescent tubes 59

TECHNOLOGY UPDATES

Peripherals race to catch up with today's CPUs 21

The performance marathon among CPUs, memories, and peripherals is heating up, severely straining parallel interconnecting pathways. To relieve the tension, many system designers are considering high-speed serial interconnecting links.—*John Gallant, Technical Editor*

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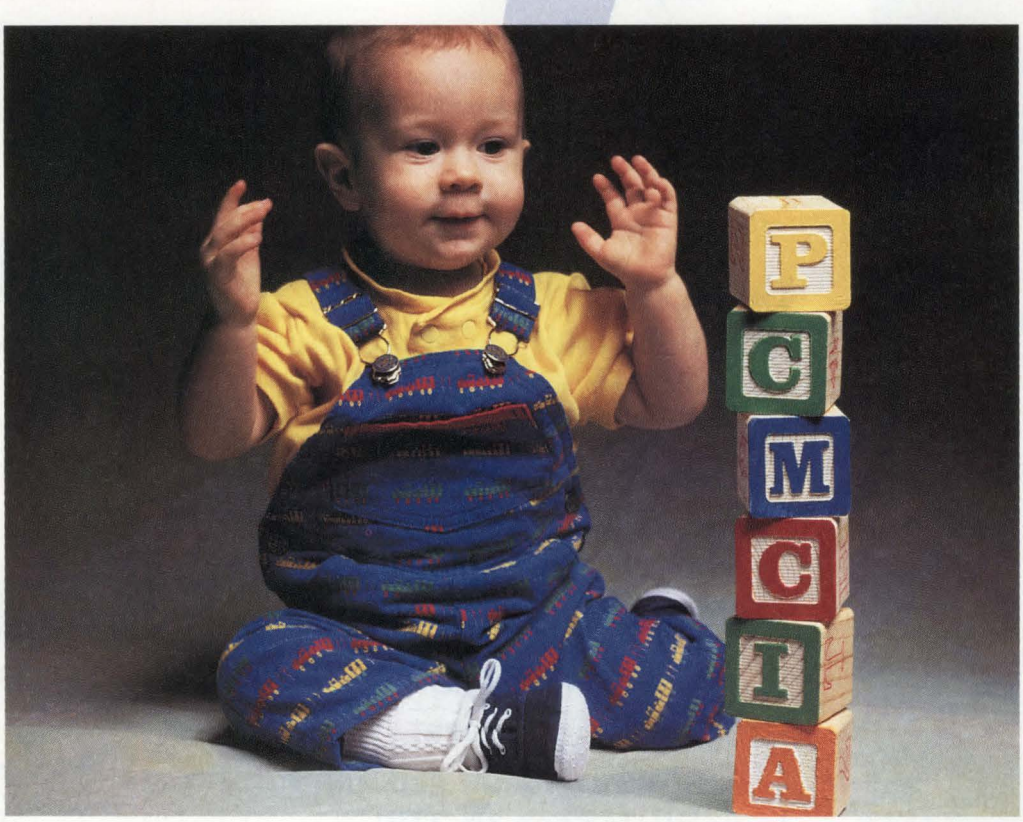

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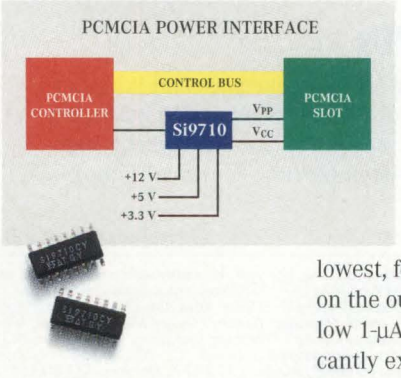

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March 31, 1994

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TECHNOLOGY UPDATES

Blending gate arrays with dedicated circuits sweetens ASIC development 29

Special-function gate arrays are a cross between the gate-array and the standard-cell approach to a semicustom ASIC design. They inherit advantages from each parent.—*Richard A Quinnell, Technical Editor*

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The C-Quad phone 19

How can products take advantage of converging computer, communications, and consumer technologies? More on the C-Quad market from *EDN*.—*Steven H Leibson, Editor-in-Chief*

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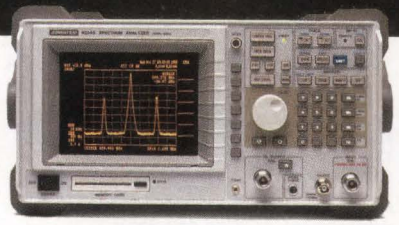

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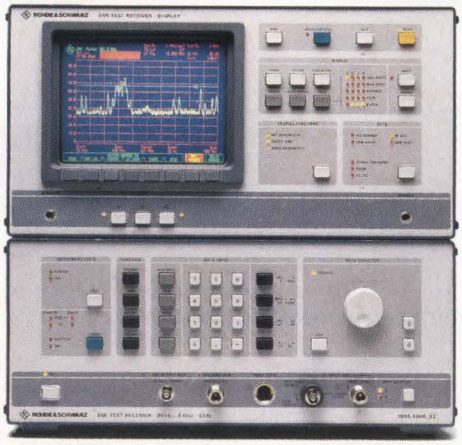

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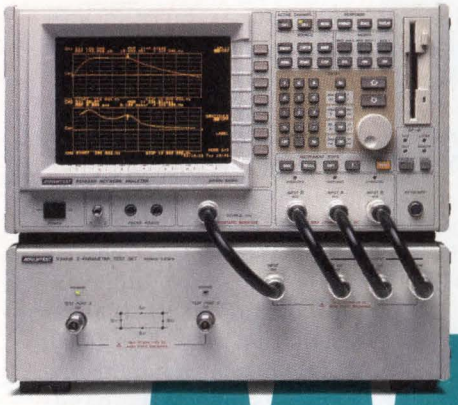

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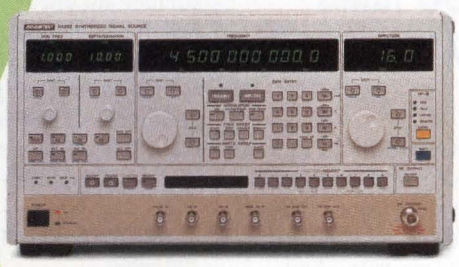

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CIRCLE NO. 33

EDITED BY FRAN GRANVILLE

IBM's portable PowerPC workstation rivals the power of a desktop

The first PowerPC-based notebook workstation, IBM's RISC System/6000 N40, provides performance of 41.7 SPECint92, 51 SPECfp92, and 2.58 Xmarks. The N40 is not only more powerful than any other notebook computer, but also than many desktop workstations. The 6.9-lb N40 runs AIX, IBM's version of Unix, on a 50-MHz PowerPC processor.

IBM's RISC System/6000 N40 is the first PowerPC-based notebook workstation.

The N40's 9.5-in. TFT active-matrix screen displays 256 colors. You can view a 1280×1024-pixel image in piecemeal fashion with pan and zoom features or all at once on an external monitor. (Initial information from IBM does not specify how many pixels the portable's own screen can display simultaneously.) A Trackpoint II pointing device in the center of the keyboard eliminates the need for a mouse.

Main memory for the N40 ranges from 16 to 64 Mbytes, and a 340-Mbyte removable disk drive is standard. The computer has ports for Ethernet, a SCSI-2 floppy-disk drive, a mouse, a keyboard, and Appletalk printers. Personal Computer Memory Card International Association (PCMCIA) slots allow future connection to token-ring networks, ISDN, and wireless adapters. An external battery pack provides four hours of operation; IBM has not yet disclosed the operating time with the N40's internal battery. The N40 sells for $11,995.—by Gary Legg

IBM Corp, White Plains, NY. (Call local IBM office for more information.) **Circle No. 452**

AnyLAN silicon springs to market

AT&T Microelectronics, in conjunction with Hewlett-Packard Co, has developed a chip set that implements the 100VG AnyLAN standard for 100-Mbps local-area networks (LANs). The standard, recently adopted by the IEEE as IEEE-802.12, uses four pairs of unshielded twisted-pair wire to carry data and handles token-ring or Ethernet data packets. It uses a demand-priority protocol to ensure timely handling of information, such as real-time video.

The chip set, designated the Regatta 100, includes a transceiver, a media-access controller (MAC), an EISA/ISA system interface, and a repeater. The MAC device provides both the 100VG AnyLAN and a 10-Mbps Ethernet MAC layer, allowing boards implemented with the chip set to connect with either LAN structure. The repeater handles the demand-priority protocol and allows creation of a managed hub as large as 90 ports. The chip set is due out in May and costs $75 for a node-adapter set and $285 for a 6-port hub set.

—by Richard A Quinnell

AT&T Microelectronics, Allentown, PA, (800) 372-2447. **Circle No. 453**

4-channel DSO takes 5G samples/sec in real time

A DSO that acquires signals in real time at 5G samples/sec is more than fast enough to raise eyebrows. Nevertheless, 5G samples/sec isn't the industry's fastest acquisition rate. And a 1-GHz bandwidth in such a scope, though very high, is also not the highest in a real-time DSO. But combine those specs in a unit that has four channels, a color display, a memory depth of 15k samples/channel, and a selling price of $29,495 ($34,690 with four 1-GHz active probes), and you have a groundbreaking product—the Tektronix TDS 684A. The scope also offers slew-rate- and setup-and-hold triggers that, according to Tektronix, are not available in any other DSO.

Both Hewlett-Packard and LeCroy Corp make real-time-sampling DSOs that offer comparable sampling rates on two channels. HP's 54720D comes with two 4G-sample/sec plug-ins, offers a 1.1-GHz bandwidth, and has a memory depth of 64k samples/channel, but the unit costs roughly $60,000. (An 8G-sample/sec, 2-GHz-bandwidth plug-in is also available, but with that plug-in, the scope has only one channel.) LeCroy's 9360 (approximately $15,000) takes 5G samples/sec on two channels but stores only 500 samples/channel at its highest acquisition rate. The 9360, which has a monochrome display, provides 600-MHz bandwidth.

The P6245 1-GHz active FET probes that Tektronix is offering with the TDS 684A also break new ground. They are small enough that you can squeeze all four onto a square cluster of posts on 0.1-in. centers. That spacing is close (the probes are much smaller than other active probes of comparable bandwidth), but the pins of surface-mount ICs are even closer. For probing such fine-pitch parts, Tektronix now offers flexible fan-shaped Capton adapters that you solder to the ICs under test. The adapters, which cost from $20 to $45, provide posts that easily accommodate the probes.

—by Dan Strassberg

Tektronix Inc, Beaverton, OR, (800) 426-2200. **Circle No. 454**

LeCroy Corp, Chestnut Ridge, NY, (800)-453-2769. **Circle No. 455**

Hewlett-Packard Co, San Jose, CA, (800) 452-4844. **Circle No. 456**

Premiere workstation-based math package gets an upgrade

For nearly a quarter of a century, developers have been refining and improving Macsyma, the symbolic-numeric mathematical software that took its name from the Massachusetts Institute of Technology's project MAC (for multiple-access computing; the name predates the Apple Macintosh by more than 10 years). Because of its long history with a discerning community of scientists and engineers, Macsyma has acquired a reputation for robustness.

For years, Macsyma ran only on minicomputers and then on workstations. Several years ago, the current publisher, Macsyma Inc, put a major effort into developing a version for PCs. Users of Unix workstations can now obtain the benefits of that work; the publisher has updated Macsyma for Unix (and related operating systems) with features first made available on the PC version. In addition to an extensive on-line help system and a new 2-volume manual, release 418 contains improvements in such areas as integration, trigonometric simplification, linear algebra, solution of ordinary and partial differential equations, simplification of Bessel functions, computing with inequalities, and numerical analysis. The publisher has also reduced prices and has adopted a "square-root" policy for multiple-user licenses. A single-user license for a SPARC 10 workstation costs $999 ($699 for academic institutions). A 25-user floating license costs five times as much.

—by Dan Strassberg

Macsyma Inc, Arlington, MA, (800) 622-7962. **Circle No. 457**

Logic-analysis systems wear workstation's clothing

Just because a product *looks* like a workstation doesn't mean that it is one. Tektronix's new TLA 510 and TLA 520 systems look like workstations, complete with 14-in., high-resolution color displays. Appearances can be deceiving, however; the TLA 510 and TLA 520 are logic analyzers. The TLA 510 ($18,000) offers 100 channels; the TLA 520 ($33,000) offers 200. Both systems perform state analysis to 100 MHz and timing analysis to 400 MHz. They offer 16-state, 100-MHz real-time triggering with two 32-bit counter/timers. More than 100 processor-specific development tools are available, including ones for the Pentium and Intel's forthcoming P54C. In the base configurations, both systems provide a memory depth of 8k frames. As shipped, all of the systems include the hardware to expand the memory depth to 512k frames, but you have to pay to enable it. Expansion costs per 100 channels are 32k frames, $4000; 128k frames, $8000; and 512k frames, $12,000. A 50-MHz pattern-generation option costs $7920; a software-performance-analysis option costs $1500.—by Dan Strassberg

No, it's not a workstation, it's a logic analyzer. Tektronix's 100-channel TLA 510 ($18,000) and 200-channel TLA 520 ($33,000) perform state analysis to 100 MHz and timing analysis to 400 MHz.

Tektronix Inc, Beaverton, OR, (800) 426-2200. **Circle No. 458**

Popular PC buses pairing off

The popularity of the Peripheral Component Interconnect (PCI) and Personal Computer Memory Card International Association (PCMCIA) buses for PCs has triggered the development of bus bridges. At least two companies—Cirrus Logic and Intel—have created PCI-to-PCMCIA controller ICs, and others are extending the two expansion buses to other popular structures.

The Cirrus CL-PD6729 ($24 (1000)) controls two fully independent PCMCIA sockets that can run at 3.3 or 5V operating voltages. The Intel 82092AA ($19 (10,000)) can control as many as four PCMCIA sockets, two using internal buffers and two using external buffers. The sockets are logically independent, but pairs must run at the same supply voltage. The device also provides a local-bus IDE interface for as many as four drives.

Other companies are expanding the PCI and PCMCIA buses in other directions. For example, Sun's SPARC Technology Business subsidiary is creating the STP4020QFP PCMCIA-to-SBus bridge. The device handles two PCMCIA cards of any type and allows use of these peripherals in SPARC-compatible workstations. On the PCI side, IBM France and the CETIA subsidiary of Thompson-CSF have begun development of a PCI-to-VME bridge. The companies plan to ship the device in early 1995.

—by Richard A Quinnell

CETIA, Toulon, France, (33) 94.08.80.00. Cambridge, MA, (617) 621-7062. **Circle No. 459**

Cirrus Logic, Fremont, CA, (510) 623-8300. **Circle No. 460**

Intel Corp, Folsom, CA, (800) 548-4725. **Circle No. 461**

SPARC Technology Business, Mountain View, CA, (415) 960-1300. **Circle No. 462**

Aris bundles three multimedia packages for less than $30

Aris Entertainment has announced WinTutor 3.1, a multimedia tutorial CD-ROM for Windows 3.1. Aris is initially selling the product in a $29.95 bundle that includes the company's MPC Wizard 2.0 and WorldView. Separately, MPC Wizard and WorldView sell for $14.95 and $39.95, respectively. The company plans to continue to offer the three products as a bundle until Microsoft Corp announces the next version of Windows (4.0), according to Diane Heppting, Aris cofounder.

WinTutor 3.1 provides 10 interac-

SHORTS

Duracell batteries to power Compaq portable computers. A new line of standard-size Duracell batteries will power Compaq Computer Corp's family of Contura Aero subnotebook computers. The DR19 battery will come with Compaq's 486SX-based monochrome model; Duracell will offer the DR31 as a longer-lasting option. The DR19 and DR31 NiCd batteries provide four and six hours of battery life, respectively; they cost $99 and $169, respectively. Duracell International Inc, Bethel, CT, (203) 796-4654. **Circle No. 468**

Mathletes get a piece of the Π. The winners of next month's Mathcounts state championships will go on to the national finals in Washington, DC, in May. There, they'll vie for $31,000 in scholarships, trips to Space Camp in Huntsville, AL, a PC, and calculators. Mathcounts is a joint effort of business and education to promote and reward excellence in junior-high mathematics. Sponsors include the National Society of Professional Engineers, the CNA Insurance Companies, the Cray Research Foundation, the General Motors Foundation, the Intel Foundation, Texas Instruments Inc, the National Council of Teachers of Mathematics, and the National Aeronautics and Space Administration. Mathcounts, Alexandria, VA, (703) 684-2828. **Circle No. 469**

Fax from your flight. Avtech and GTE Airfone (Oak Brook, IL, (708) 572-1800) have developed an airborne facsimile service, which will become available on some major airlines in March. The system couples GTE's GenStar digital-telecommunications system with Avtech's AvFax airborne fax terminal. It provides users with voice, document-fax, and data-fax capabilities via the AvFax or their own laptop PCs or portable fax machines. Avtech Corp, Seattle, WA, (206) 634-2540. **Circle No. 470**

tive, progressively more advanced lessons that let users master the basics of using Windows. Each lesson finishes with a quiz and a practice session. One of the other two titles in the bundle, MPC Wizard 2.0, combines 100 Mbytes of Windows 3.1 video and sound drivers with a collection of multimedia clips. The other title, WorldView, offers 100 color photographs of outer space (from the NASA), new-age music, and 25 runtime videos. Aris products are available through retail outlets, including CompUSA, Egghead Software, Fry, and Software Etc.

—by Fran Granville

Aris Multimedia Entertainment Inc, Marina Del Rey, CA, (310) 798-7875. **Circle No. 463**

Tutorials and technical sessions at SunWorld

IDG World Expo's Sun User Group miniconference will occur jointly with SunWorld '94 Conference and Exposition, scheduled for June 13 to 18 at the Moscone Center in San Francisco. The Sun User Group miniconference offers approximately 30 technical sessions, including "An Overview of Perl Programming," "Spring Operating System Technical Overview," and "The Adaptive Communications Environment." In addition, six day-long classes cover topics such as Perl, responding to security incidents, and internetworking with Transfer Control Protocol/Internet Protocol (TCP/IP) and Unix.

—by Jim Leonard

Sun User Group, IDG World Expo, Framingham, MA, (508) 879-6700. **Circle No. 464**

Free software prevents network break-ins

In response to a rash of recent break-ins on the Internet information network, Cygnus Support has released Cygnus Network Security (CNS) software, a stable, tested version of Kerberos network security software. (Software engineers at the Massachusetts Institute of Technology, Cambridge, MA, developed Kerberos.)

CNS works by preventing passwords from traveling over the Internet in clear text. Kerberos uses data-encryption-standard (DES) encryption to validate a user's password at a local machine rather than send it via network to a remote machine, thus blocking intruder access.

Cygnus is offering CNS for free; CNS binaries are available for Unix systems such as SPARC, DECstation, HP 700, and Sun-3. The software is not currently available for PCs or Macintosh systems.—by Jim Leonard

Cygnus Support, Mountain View, CA, (415) 903-1401. **Circle No. 465**

Access the Internet via Windows

WinNET Mail and News version 2.0 from Computer Witchcraft Inc lets users access the Internet information service from a PC running Microsoft Windows version 3.1. The only other equipment required is a 300-bps to 14.4-kbps, Hayes-compatible modem. The product lets users omit having to use terminal emulators, Unix command prompts, character-oriented menus, or obscure commands. The service provides instant account registration and automated news subscriptions. WinNET rates are $8/hour with a monthly minimum fee of $9.95.

—by Fran Granville

Computer Witchcraft Inc, Louisville, KY, (502) 589-6800. **Circle No. 466**

Fingerless gloves offer wrist relief

Proper hand positioning on a keyboard is essential for avoiding Carpal Tunnel Syndrome. To ensure proper positioning, MouseMitt International offers a fingerless glove called the Keyboarder. It holds and supports your wrist as you type, and it provides padding to protect the carpal bones when your wrist is resting on the work surface. The gloves come in a variety of sizes and colors and cost $19.95/pair.

—Richard A Quinnell

MouseMitt International, Scotts Valley, CA, (408) 335-9599. **Circle No. 467**

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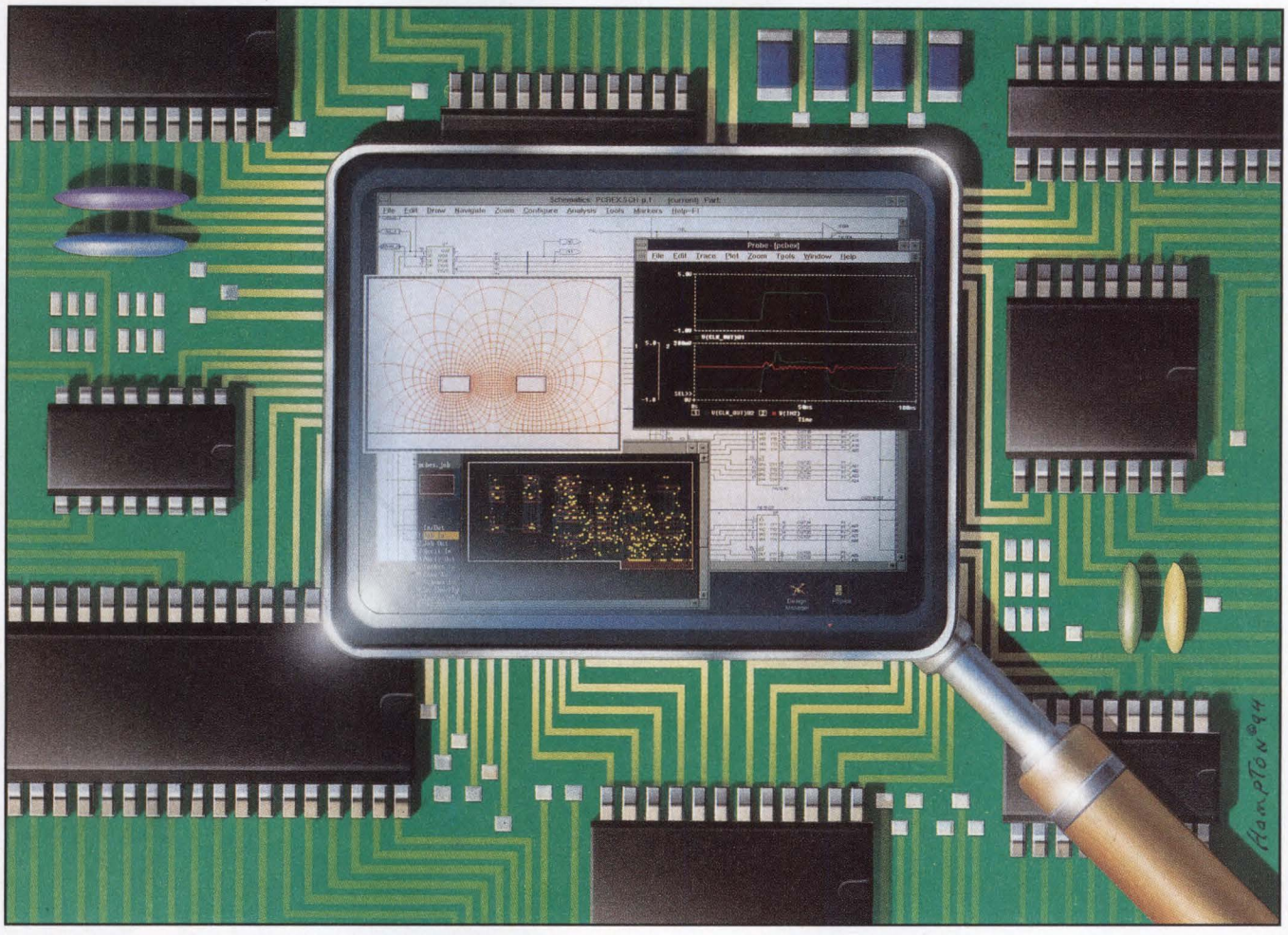

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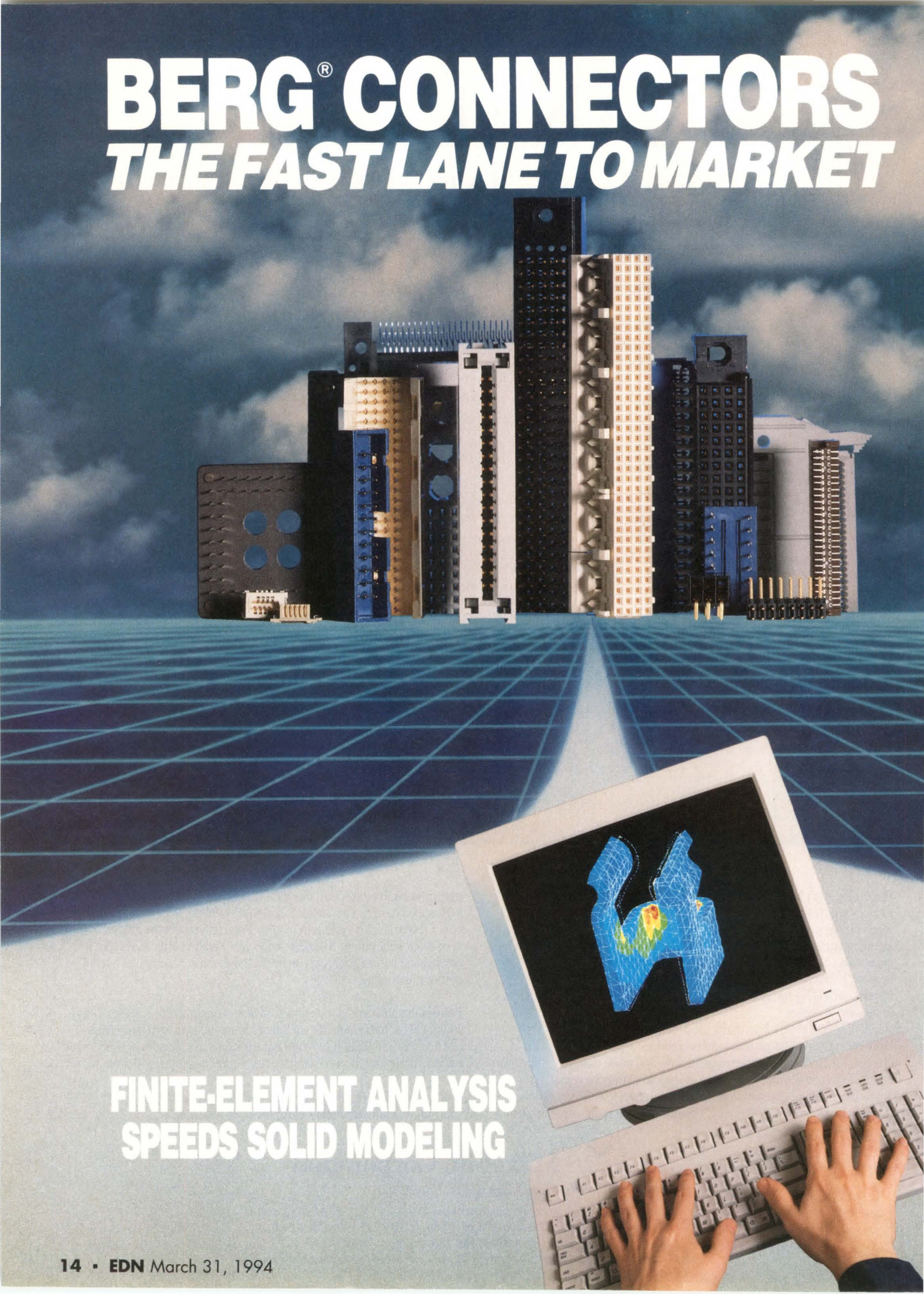

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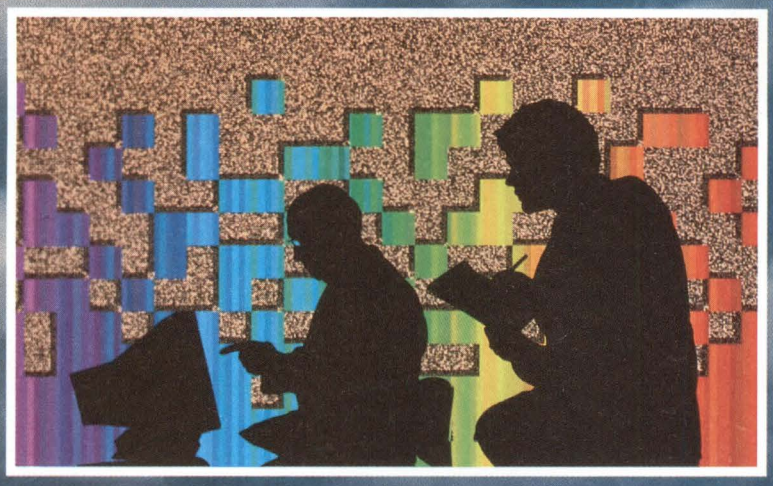

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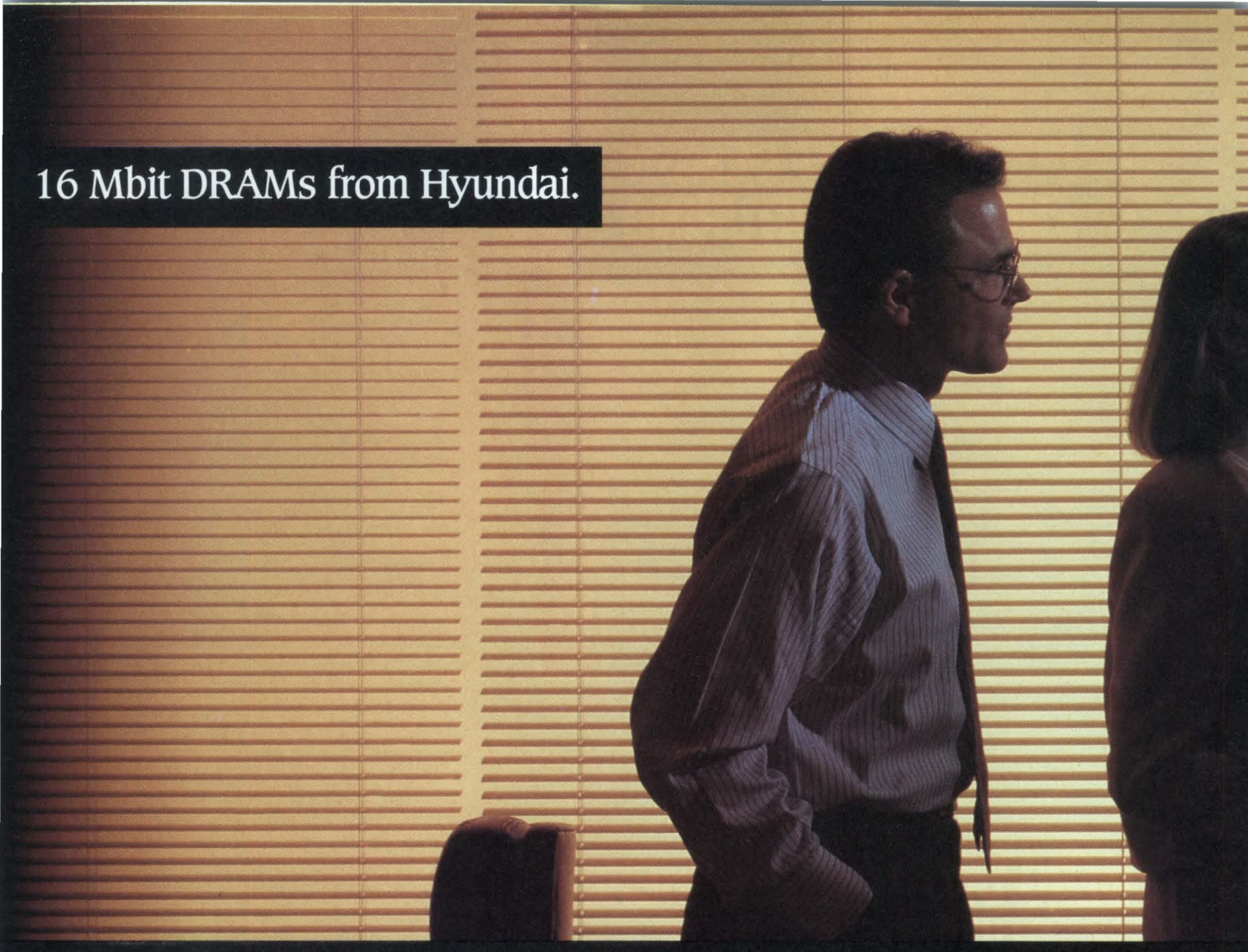
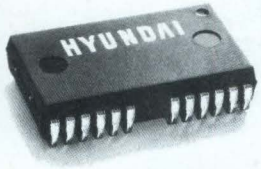
CIRCLE NO. 34

16 Mbit DRAMs from Hyundai.



Team Dy



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Now, virtually all of the make or break purchases for DRAMs and other major ICs in companies with over $10M in sales* are the result of a cross-functional team dynamic. And remember, no company has a bigger commitment to team dynamics than Hyundai.

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Our new 16 Mbit dynamic RAMs are one more example of our dedication to the needs of the new team dynamic. We're committed to your success and the success of your cross-functional buying team through Hyundai's commitment to quality, reliability, manufacturing capability and value added pricing.

Your Hyundai DRAM Source Guide

Size	Part Number	Speed ns	Refresh Cycles/ms	Production
16M x 1	HY5116100	60/70/80	4096/64	now
	HY5117100		2048/32	
4M x 4	HY5116400	60/70/80	4096/64	now
	HY5116410		4096/64, WPB	
	HY5117400		2048/32	
	HY5117410		2048/32, WPB	
2M x 8	HY5116800	70/80	4096/64	Q4 '94
	HY5116810		4096/64, WPB	
	HY5117800		2048/32	
	HY5117810		2048/32, WPB	
1M x 16	HY5116160	70/80	2$\overline{\text{CAS}}$, 4096/64	Q4'94
	HY5116260		2$\overline{\text{CAS}}$, 4096/64, WPB	
	HY5118160		2$\overline{\text{CAS}}$, 1024/16	
	HY5118260		2$\overline{\text{CAS}}$, 1024/16, WPB	

All available in standard and low power versions.
Packages include SOJ, TSOP II, reverse TSOP II.

namics.

New 16 Mbit DRAMs, designed with team dynamics in mind.

Evaluation samples of Hyundai DRAMs organized 16M x 1, 4M x 4 are available now. Coming soon are DRAMs organized 1M x 16 and 2M x 8. And many will operate off of a 3 volt source too.

Hyundai's new DRAMs feature speeds of 60, 70, or 80 ns. Immediately available, the HY5116100 and HY5117100 are organized 16M x 1 and provide 4096 refresh cycles per 64 ms and 2048 refresh cycles per 32 ms, respectively. New 4M x 4 parts include the HY5116400, with 4096 refresh cycles per 64 ms, the HY5116410 with write-per-bit capability, and the HY5117400 and write-per-bit capable HY5117410 offering 2048 refresh cycles per 32 ms.

All parts are available in standard and low power versions, dissipating 495 mW operating at 60 ns, 440 mW at 70 ns, and 385 mW at 80 ns. Other features include operation from a single 5V ±10% power supply, TTL compatible inputs and outputs, fast page mode operating, multi-bit test capability, read-modify-write capability, and CAS-before-RAS, RAS-only, as well as hidden refresh. Packages include standard 24/28 pin plastic, TSOP II, and reverse TSOP II. TSOP will be available soon.

These new parts are products of Hyundai's 0.55 micron CMOS process, at one of the most advanced electronics manufacturing plants in the world. So if purchase of 16 Mbit DRAMs is on your agenda, and you don't want to get caught short the way some did on 4 Mbit, start the team dynamics now.

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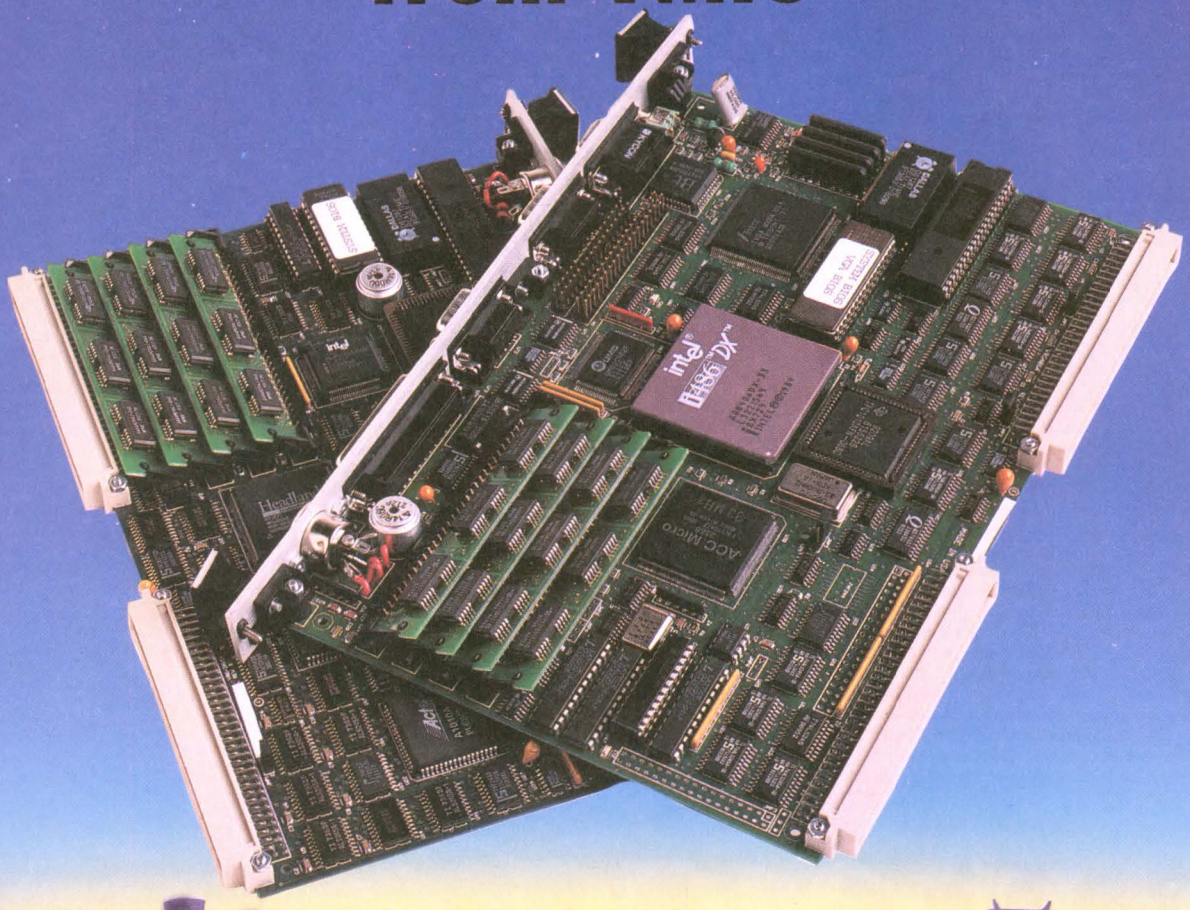

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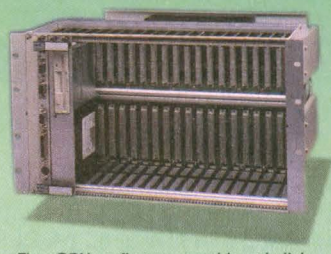

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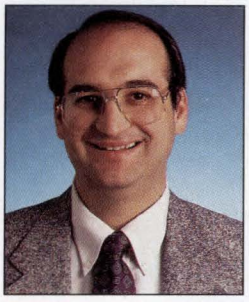
The C-Quad phone



How many times have you heard someone say: "Hold on; I'll try to transfer you, but if I lose you...?" The reason for this problem with business phones is simple: Most telephone sets connected to PBX systems still employ the traditional 12-button Touch-Tone keypad AT&T introduced in the early 1960s. I can think of no other electronic market in which we settle for 30-year-old user interfaces. Most business phones available today do not take advantage of the tremendous technological innovation that has occurred over the past two decades. However, it's relatively easy for me to quickly conjure an advanced technology phone for this editorial, to illustrate how such a product might look in the C-Quad market. (For more information about the C-Quad market—named for the convergence of the computer, communications, and consumer markets—please see my editorial in the previous issue of *EDN*.)

First and foremost, let's fix the phone's user interface. The biggest advance we can make is to give the phone a display and a better input device. A small alphanumeric LCD with a touch-sensitive overlay would provide a tremendous boost to the operation of a phone. It could display the extension or phone number of incoming calls (using caller ID); it could display user prompts at any stage of a call so that you don't need to remember how to transfer a call, how to set up a conference call, or how to pick up a call within your calling zone; and it could provide a menuing system for more complex operations.

These more complex operations are the bane of any individual or company. For example, phone-number formats vary from country to country, and it's often more difficult than necessary to make international calls. A phone with a display can easily give you calling directions for any location on the planet and tell you the time of day at that location to boot. Equally important, a phone with an alphanumeric LCD can display a list of your frequently called phone numbers for easier dialing.

This advanced phone should be connected to a far smarter PBX or central-office switch. The entire telephone directory of the United States is now available on a half-dozen CD-ROMs. The business directory fits onto just one CD-ROM. A phone with a display can provide you with a window into those directories.

In fact, this sort of telephone system has been available for years in France. It's called the Minitel, and it has become very successful, not just as a communications device but as a money-making information source and as a replacement for paper telephone directories. Minitel employs a CRT instead of an LCD and has a full keyboard instead of a touchscreen. Functionally, however, it provides the same capabilities as the advanced phone I propose. Minitel is but one excellent example of the C-Quad market's enormous potential. Time and again, the worldwide market has established that it is willing to pay well for education, communications, and entertainment. Successful C-Quad products such as Minitel will directly target these needs and wants.

Jesse H. Neal
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SSOP 20-pin	PY	0.650	56.0	7.2	5.3	1.9
SOIC 20-pin	SO	1.270	133.1	12.8	7.5	2.5
TSSOP 48-pin	PA	0.500	102.1	12.6	6.2	1.1
SSOP 48-pin	PV	0.635	164.4	15.9	7.5	2.6

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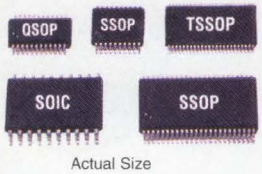

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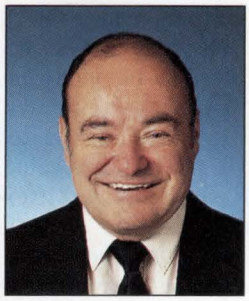
Peripherals race to catch up with today's CPUs

JOHN GALLANT, Technical Editor



The performance marathon among CPUs, memories, and peripherals is heating up, severely straining parallel interconnecting pathways. To relieve the tension, many system designers are considering high-speed serial interconnecting links.

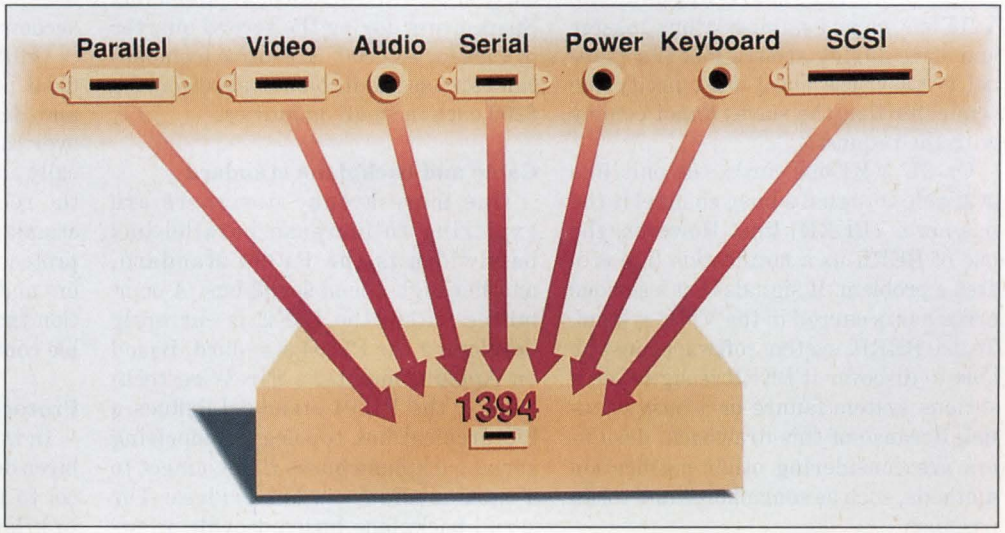
In the early 1980s, slow CPUs were the limiting factor to system processing; peripherals and memory interfaces were faster. But since the mid-1980s, all that has flip-flopped: Now, the bottleneck for transferring data has shifted from CPUs to I/O devices. Today, CPUs typically run at 50 MHz and faster—speeds that strain or exceed the capacity of communication pathways to memory and I/O devices. As a result, system designers trying to match CPU speeds are looking toward high-speed serial buses to extend computer memory and I/O bandwidths.

To extend the bandwidth of parallel buses, designers must increase clock rates and widen data paths. However, these solutions entail high power consumption, increased real estate, high cost, increased crosstalk, and decreased noise immunity due to skew factors and the large-ground-bounce effects of many lines switching at once. A high-speed serial bus transmits data over a single path, which eliminates many of these potential problems, providing that the electrical connection can handle the fast data rates.

One way designers are increasing memory and I/O bandwidth is by using the AutoBahn—the VMEbus's answer to high-speed serial communications. PEP Modular Computers created the AutoBahn for 3U VMEbus cards. The AutoBahn uses two little-used lines on the P1 connector, B21 and B22, defined as a serial clock and a serial data line for low-speed communications. AutoBahn develops a differential 50Ω transmission line on these two lines to transfer data initially at 200 Mbytes/sec (1.6 Gbps) using positive-ECL-compatible (PECL) transceivers. In the future, transfer rates will reach 400 Mbytes/sec (3.2 Gbps).

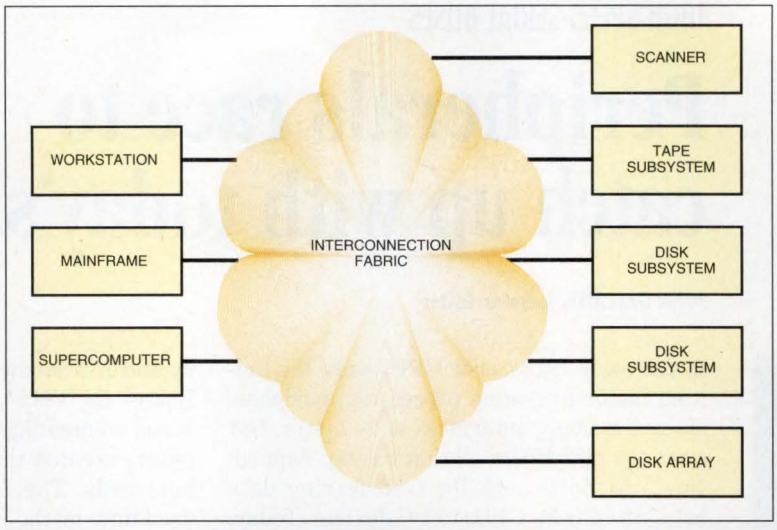
AutoBahn is part of the VMEbus extension, which also adds VME64 and source-synchronized block-transfer (SSBLT) capability to an IEEE-1014-compatible VMEbus. In February 1993, several companies, including Motorola Semiconductor, formed the AutoBahn Consortium to develop an ECL gate array, called the Spanceiver (serial-parallel transceiver) to transfer data over AutoBahn. The Spanceiver employs Motorola's Mosaic V ECL-in-Picoseconds-Lite technology.

The Spanceiver has a 16- or a 32-bit TTL parallel interface, which the chip serializes



IEEE defines P1394 as a global I/O standard to interconnect asynchronous devices and to support a guaranteed bandwidth for real-time applications, such as audio and video.

for transmission at PECL levels. The same single-chip Spanceiver, on other boards in the same backplane converts the serial data back into 16- or 32-bit parallel data for the receiving board. The chip inserts a synchronization bit, which guarantees a transition at the start of each transmitted byte. An on-chip phase-locked loop, which employs an off-chip crystal reference, detects the synchronization bit to maintain timing accuracies.



The Fibre Channel defines an intelligent interconnection scheme, called a fabric, to connect devices. A port only has to manage a simple point-to-point connection between itself and the fabric.

VMEbus performs arbitration

The AutoBahn employs the VMEbus arbitration and data-transfer buses to control the flow over the serial data link. The VMEbus's address bus transfers source and destination address information to a potential receiving node. The AutoBahn then transfers data over the serial bus to the node in blocks, which must start on a 32-byte boundary.

A simplex connection, which transfers 1-way data point-to-point, is the easiest transfer method and lets systems transfer large blocks of graphics data. A duplex configuration containing multiple parties on the bus is more complicated. In this configuration, the VMEbus must establish a bus master and slave during arbitration. If a channel is busy, the slave must notify the requester that the slave cannot comply with the request.

On 3U VMEbus cards, the only line available to signal a busy channel is the bus-error (BERR) line. However, the use of BERR as a notification line creates a problem: It signals that a serious error has occurred in the VME system. To use BERR, system software must be able to discover if BERR is signaling a serious system failure or a busy channel. Because of this drawback, designers are considering other notification methods, such as semaphores and token passing.

Although PEP developed AutoBahn to give 3U VMEbus boards a midlife spark, 6U VMEbus implementations provide a wider range of possibilities. A 6U implementation can use the RETRY line on the P2 connector to notify a busy signal instead of the BERR line. The RETRY line requires less software work. In addition, designers can construct multiple AutoBahn serial buses on the undefined pins of rows A and C of the P2 connector to create multichannel architectures.

Until August 1994, AutoBahn Spanceivers will be available through the AutoBahn Consortium. Thereafter, all Spanceiver sales will be through Motorola Semiconductor. Membership in the AutoBahn Consortium gives you early access to five first-run production Spanceivers during the second quarter of 1994 for $30,000. Executive members can purchase additional Spanceivers for $250 each in small quantities.

Cable and backplane standard

One more avenue designers are exploring to increase parallel-bus bandwidth is the P1394 standard, another high-speed serial bus. A committee within the IEEE is currently developing the P1394 standard. Based on Apple Computer's FireWire technology, the P1394 standard defines a hierarchical bus topology comprising serial backplane buses that connect to a cable medium via bus bridges. The serial backplane buses provide a low-cost alternative for parallel backplane buses, and the cable medium interconnects modules on different backplanes.

The cable medium allows 16 physical connections, each as long as 4.5m. Using the cable medium in node-branching and daisy-chaining topologies enables the connection of workstations, hard-disk drives, printers, cameras, CD-ROMs, and scanners. An inexpensive multiconductor cable employs six shielded, twisted-pair wires. The cable dedicates two differential lines for data and two as a strobe line. The other two lines are 8 to 40V-dc power lines having 1.5A capacity for driving the physical layer of each node. This method lets you insert live cables onto the bus without damaging the network.

P1394 transmits data at 98.304, 196.608, and 393.216 Mbps over the cable medium. All higher speeds must be backward-compatible with lower speeds. Backplanes, which can have as many as 63 nodes, have data rates that depend on the logic circuitry employed. A TTL serial backplane bus transfers data at 24.576 Mbps, and a backplane-transceiver-logic (BTL) or ECL serial backplane transfers data at 49.152 Mbps. The bus bridge that connects a backplane to the cable medium must accommodate the rate differences.

Unlike AutoBahn, the P1394 standard provides arbitration and source and destination information directly over the serial bus. The bus automatically assigns node addresses, removing the requirement for ID switches. The standard also defines a transmission protocol comprising three stacked layers and a serial bus-management function that employs IEEE-1212-compatible control and status registers.

Protocols describe transfers

In the P1394, a software-transaction layer defines a request-response protocol to perform the bus transaction. A link layer provides a confirmation of reception to the transaction layer and provides addressing data checking and

data framing. The physical layer translates the logical symbols used by the link layer into electrical signals on the serial bus media.

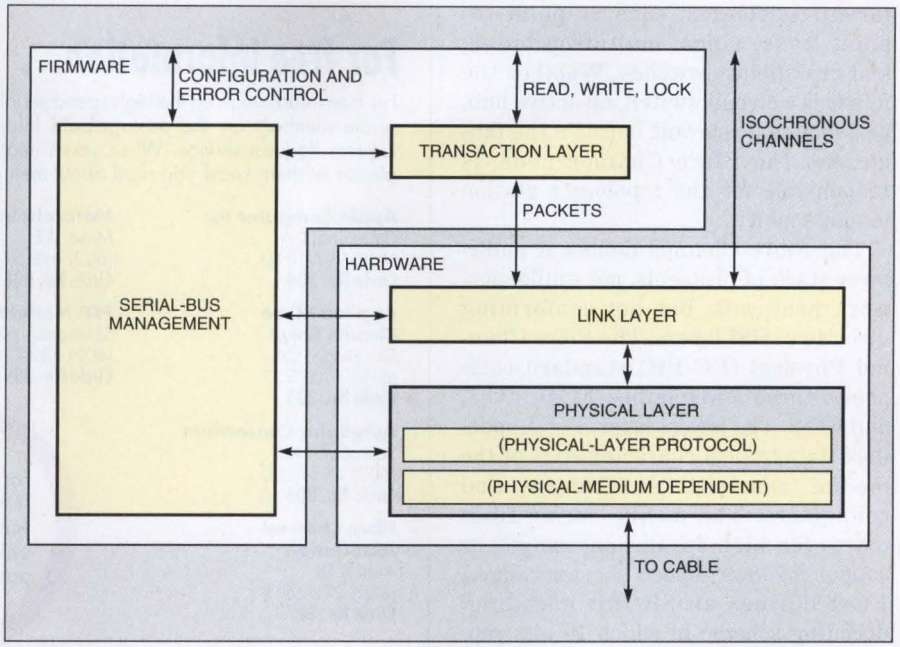
The transmission protocol adds header information to data packets on the serial bus. The protocol allows for direct transactions, lock subcommands, and split transactions on the bus. The bus can transmit data asynchronously or isochronously. Isochronous-data transmission occurs at regular intervals to guarantee a fixed latency for real-time applications, such as multimedia. Texas Instruments has a licensing agreement with Apple Computer to develop a 2-chip set for the link and physical layers of the P1394 standard. That chip set should be available in the second quarter of 1994.

Gaps separate each data packet on the serial bus, giving each node an opportunity to arbitrate for the bus. Isochronous access has highest priority, and a fair arbitration protocol prevents any node from monopolizing the entire asynchronous bandwidth of the bus. In addition, the protocol can give urgent access to nodes operating on a backplane serial bus. Draft copies of the P1394 standard are available from the IEEE Computer Society, 1730 Massachusetts Ave NW, Washington, DC 20036, or phone (202) 371-0101.

Moving up the performance curve is the Fibre Channel. The ANSI X3T9.3 committee chartered the Fibre Channel working group in 1988 to develop an interconnection standard for bidirectional point-to-point serial data communications between workstations, mass-storage subsystems, and peripherals. The requirements are ambitious. The Fibre Channel transfers data at 133 to 1062 Mbps on a single fiber over distances as long as 10 km. Because information can flow in both directions simultaneously, users can transmit on one fiber and separately receive data on another fiber.

The Fibre Channel's interconnection fabric operates similarly to that of a switched telephone exchange, where a user dials an address (node) and connects to another address (node) on the fabric. The fabric uses crosspoint switches to provide a choice of multiple paths between nodes. Fibre Channel allows 16 million nodes on a single fabric, whereas a SCSI parallel bus allows only 16 nodes that must be within feet of each other.

Transmission over the Fibre Channel is isolated from the control protocol, so that users can implement dif-



The IEEE-P1394 serial-bus standard describes a hardware and firmware communication protocol to provide data transfer over a hierarchical serial backplane and interconnecting-cable topology.

Looking ahead

All of the high-speed serial buses this article discusses are still under development. The current activity for AutoBahn is to establish a reliable physical layer on the VMEbus. However, Ray Alderman, CEO at PEP Modular Computers, outlines a wide range of possibilities for AutoBahn. One possibility is to add arbitration and source and destination headers directly over the serial bus using carrier-sense multiple-access/collision detection (CSMA/CD) coding. Alderman envisions that using multiple channels on rows A and C of the P2 connector will provide multidimensional computer architectures, similar to hypercubes on a VMEbus backplane using multiple AutoBahns as a media.

The P1394 standard is still in the proposal stage and, as such, is not yet an official IEEE standard. The committee has finished most of the work, however, and Jonathan Zar, business manager of the FireWire project at Apple, expects the proposal to go out for final bids in May. The goal for P1394 is to keep node costs less than $15/node. One specification that still needs definition is the bus bridge that interfaces a backplane serial bus to the cable medium, both of which operate at different data rates. In addition, the committee is developing a SCSI serial-bus protocol (SBP), which will define how the P1394 serial bus will transport SCSI functions.

The ANSI working group has finalized and put out for second public review all FC-PH layers of Fibre Channel. Early applications for Fibre Channel are for Redundant Array of Inexpensive Disks (RAID) disk drives and clusters of computers. Development continues on FC-4 to transport other protocols, including asynchronous-transfer mode (ATM), Fiber Data Distributed Interface (FDDI), High-Performance Parallel Interface (HIPPI), SCSI-3, Ethernet, Token Ring, and the Transfer Control Protocol/Internet Protocol (TCP/IP), over Fibre Channel.

HIGH-SPEED SERIAL BUSES

ferent topologies, such as point-to-point links, rings, multidrop buses, and crosspoint switches. Whether the fabric is a circuit switch, an active hub, or a loop is irrelevant because the fabric, not the Fibre Channel node, is responsible for the topology's station management.

The Fibre Channel defines a multilayer stack of protocols, not unlike network protocols, but not conforming directly to OSI layers. The Fibre Channel Physical (FC-PH) standard comprises three lower levels: FC-0, FC-1, and FC-2. The lowest layer, FC-0, specifies the physical characteristics of the media, transmitters, receivers, and connectors. The media can be fiber optics for high-speed long ranges or copper for lower-speed shorter ranges. FC-1 defines an 8B/10B encoding/decoding scheme in which 10 bits represent 8 bits of real data. IBM has a patent on the scheme, and the 25% overhead of using 10 bits of transmission to transfer 8 bits of data causes a maximum transfer rate of 100 Mbytes/sec (200 Mbytes for 2-way transmission) at 1062 Mbps.

FC-2 defines the Fibre Channel's transport mechanism. This layer manages rules for placing data, frame headers, cyclic-redundancy-check error detection, and frame delimiters into packets for Fibre Channel's packet-switched services. Because Fibre Channel is hardware-intensive, it relies on the frame header to trigger actions. At 1062 Mbps, the Fibre Channel cannot make decisions in microcode fast enough. Fibre Channel also puts no limit on the size of transfers between applications.

The ANSI working group is still developing two upper layers for Fibre Channel. The FC-3 layer will provide common services, such as striping to achieve higher bandwidths and multicasting to deliver a single transmission to multiple destinations. FC-4 will provide a seamless integration to other data-communication protocols, such as asynchrounous-transfer mode (ATM), Fiber Data Distributed Interface (FDDI), High-Performance Parallel Interface (HIPPI), SCSI-3, Ethernet, Token Ring, and the Transfer Control Protocol/Internet Protocol (TCP/IP), to communicate directly over Fibre Channel.

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Fibre Channel Association
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To accommodate a wide range of communications needs, Fibre Channel defines three classes of service. Unlike with FDDI or other ring-type LANs, each class can use as few as two nodes on the fabric. Class 1 is a circuit-switched, dedicated, physical channel. When a host and a peripheral use Class 1 to connect, they make their connection path unavailable to other hosts or peripherals. As a result, Class 1 has the nickname "selfish mode" and is an ideal method to use when the time to make a connection is short or data transmissions are long.

Class 2 is a connectionless, frame-switched link, which provides guaranteed packet delivery with an acknowledgement on receipt. If Class 2 cannot make the delivery due to congestion, it gives the sender a busy signal and immediately tries again. Similar to traditional packet-switched systems, Class 2 systems do not have a dedicated path between two devices, providing a wider-link bandwidth.

Class 2 service is ideal for data transfers to shared mass-storage systems that are some distance from several workstations. An optional Intermix mode reserves a dedicated Class 1 connection but also allows connectionless traffic to share the link if there is available bandwidth.

Class 3 is a connectionless service, similar to Class 2, that sends data to multiple devices attached to the fabric but does not confirm receipt. The transfer, or datagram, is most practical when the time to make a connection is short. Class 3 service is useful for real-time broadcasts, in which timeliness is key, and information not received has little value.

Distance is the greatest factor influencing connection time. It takes an electrical signal about 10 μsec to travel 3 km. To establish a logical connection for Class 2 service requires a signal to make a round trip of 20 μsec before transfer can begin, whereas Class 3 service can make the connection in 10 μsec.

For designers interested in developing Fibre Channel nodes, Applied Micro Circuits Corp offers a Fibre Channel chip set to perform high-speed serial data transmission over fiber-optic or coaxial cable. The interfaces conform to the ANSI X3T9.3 Fibre Channel specification. The S2039 and S2040 transmitter pairs cost from $78 to $225 (1000). EDN

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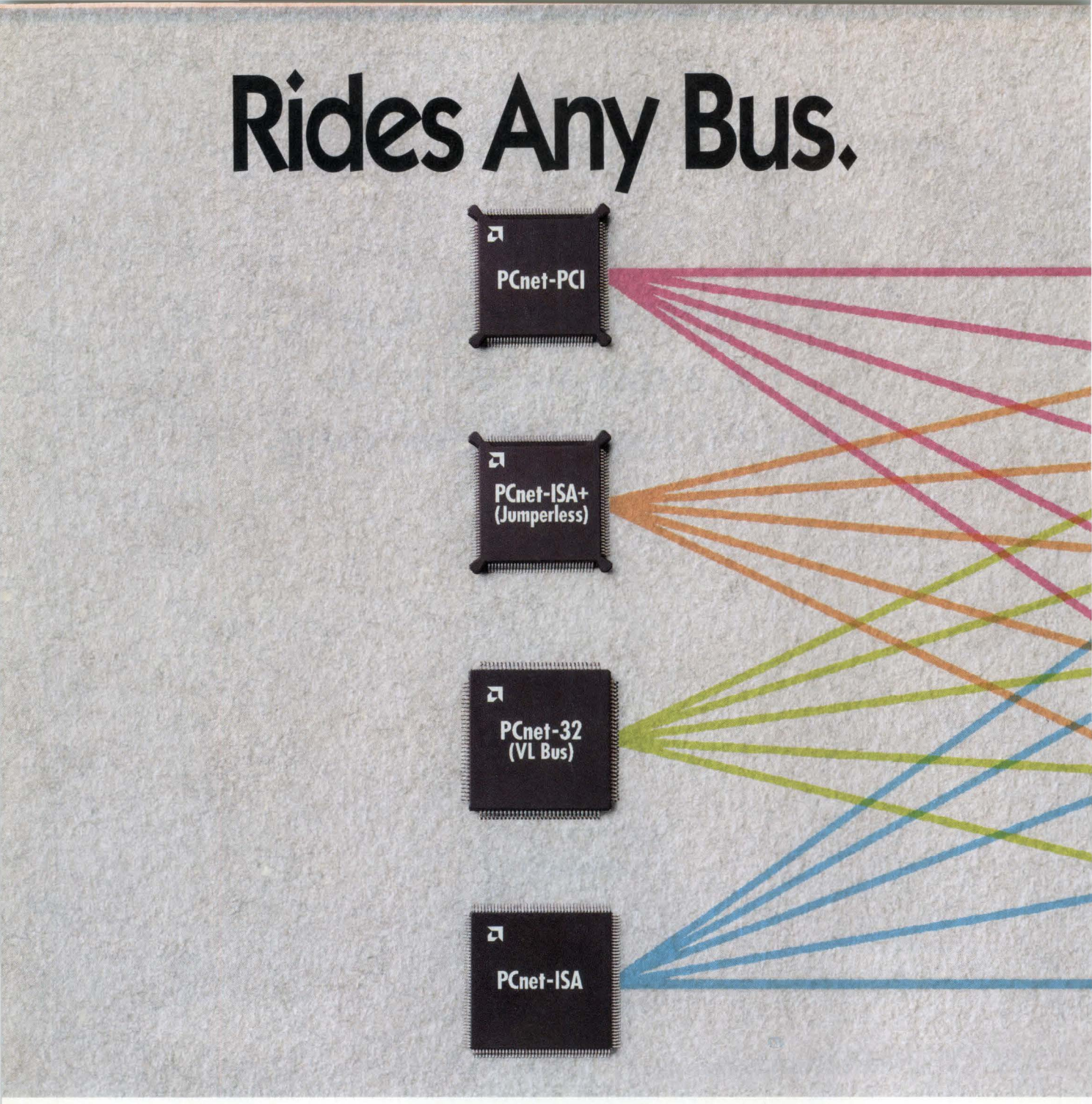

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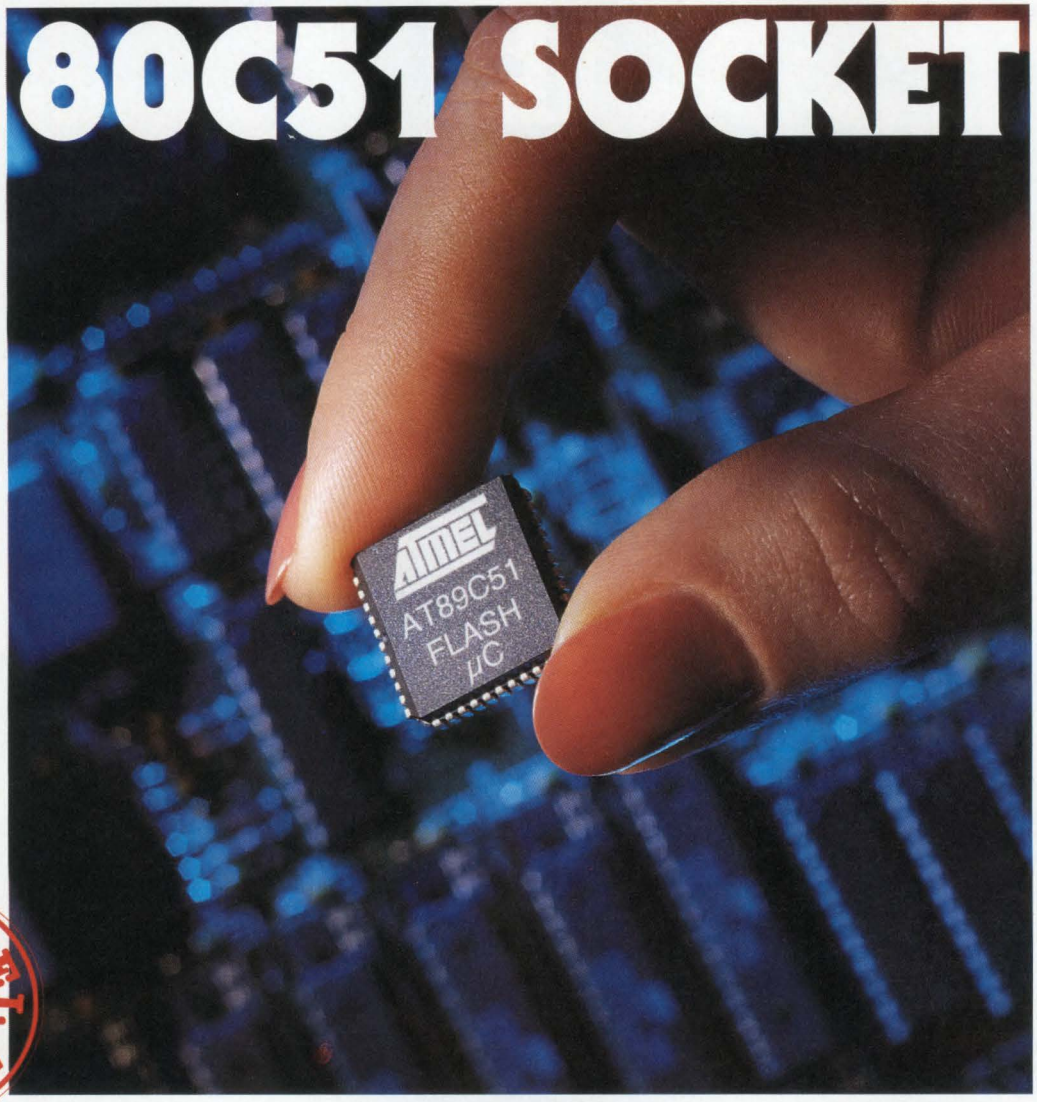

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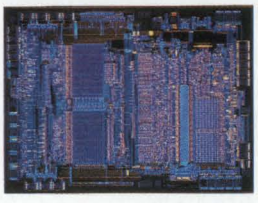

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Blending gate arrays with dedicated circuits sweetens ASIC development

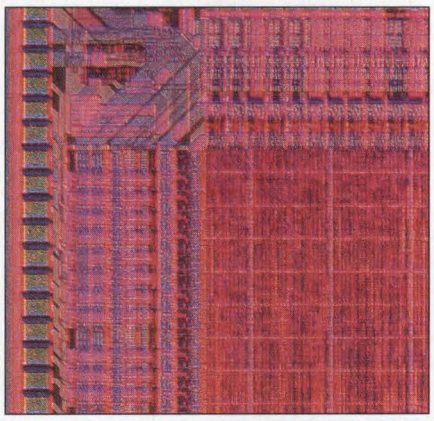
RICHARD A QUINNELL, Technical Editor

Special-function gate arrays are a cross between the gate-array and the standard-cell approach to a semicustom ASIC design. The gate arrays inherit advantages from each parent.

Approaching the design of a semicustom ASIC was once simple. You picked a gate array for low development cost and quick turnaround. For top performance and the greatest density, you took the standard-cell approach. The distinction between the two methods, however, has blurred, creating a third alternative: the special-function gate array (SFGA).

The SFGA, a hybrid approach to semi-custom ASIC design, combines a mass of undedicated gates with blocks of predesigned circuits (**Fig 1**), which are typically too large or too slow when implemented in gate logic. Memory is one such circuit that has been available since 1990 as a special-purpose block within a gate array. Implemented in raw gates, a block of memory may be three times the size of an equivalent predesigned block.

SFGAs are available in predesigned and customer-designed forms. A predesigned SFGA, like conventional gate arrays, is one that a manufacturer designs and fabricates through all process steps but the final interconnections. You pay for just the metal-mask-layer design. Then the manufacturer quickly fabricates your circuit from a stock master slice. Such devices suit a class of applications that have common need for the special function. These predefined circuits are typically blocks of memory or PLLs that configure into final form simply through the interconnecting wiring. Other functions are possible, however, where there is a broad enough base of applications that need the function.



You cannot create the special function in the corner of this Motorola array with gates alone. It is an analog PLL that operates at 125 MHz.

For example, Texas Instruments' TGB2000E series gate arrays include high-speed BiCMOS multiplexing and demultiplexing circuits in addition to CMOS sea-of-gates arrays. The devices are for telecommunications applications that, due to the data rates involved, need the speed of bipolar circuits as well as the lower power demands of CMOS. The BiCMOS circuits serve as specialized I/O ports that convert high-speed data to multiple lower-speed data streams that the CMOS array can handle. By working only with the metal layers, you implement your logic in the CMOS array and wire the multiplexers into the structures your data interface needs.

With customer-designed SFGAs, you customize a gate array by adding blocks from a hard macro library to the array matrix (see **Table 1**). The macro may be memory, a microprocessor, a serial port, or virtually any other function that can be created in the same process used in fabricating the sea of gates.

SFGAs offer several advantages over pure gate-array and standard-cell designs. The embedded function in SFGAs is smaller and faster than that of a gate-equivalent design. The size and speed improvements translate into lower unit cost due to smaller die size and better performance in the final design.

Also advantageous, SFGAs are able to include a function on their ICs that you cannot implement using gates alone. However, implementing this function still retains the

development-time benefits of the gate-array approach. The Motorola H4C+ series, for example, integrates an analog PLL with its base array. Using a standard gate array with a separate PLL increases part count. Having the two parts separated also reduces performance because of the additional signal delays the packaging causes.

The development time and cost required to use an SFGA depends on its type. Predesigned versions retain the development advantages of their gate-array parent. Customer-designed types require development of a complete mask set, just as standard-cell designs do. For designs needing quick turnaround, the predesigned types seem the best choice. Unfortunately, they are relatively scarce.

For users, the major problem with predesigned SFGAs is a mismatch between the special function on the base wafer and the users' needs. With predefined blocks of embedded memory, for example, you may have more memory on chip than necessary, so you pay for features that you don't need. Manufacturers do not want to offer a wide range of choices; if they guess what you require, they may guess wrong and have to pay for an inventory of master slices that go unused.

Because of potential mismatches, some manufacturers avoid the SFGA market until high-volume applications with clearly defined needs arise. To circumvent the mismatch, most SFGA manufacturers offer only the customer-designed devices. Unfortunately, these cost more to develop.

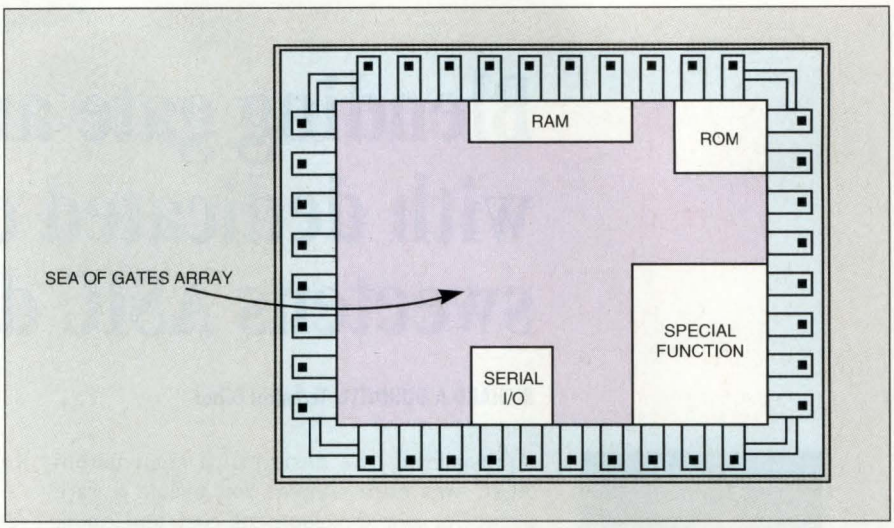


Fig 1—Special-function gate arrays float islands of dedicated circuits in the sea of gates. The dedicated circuits typically handle functions that are too large or too slow when implemented in gates.

Most ICs require at least 14 lithography masks during fabrication at a cost of $1000 to $3000 per mask. Gate-array users need only to develop the final three to four masks to complete a design. All the users of the base array share the costs of the remaining masks. With a customer-defined SFGA, a user pays for a full set of masks.

Customer-designed SFGAs also lose some of gate arrays' quick-turnaround benefits because you cannot draw from the vendor's stock of partially completed gate-array wafers. Instead, the manufacturer has to fabricate your silicon from scratch. You might infer, then, that a customer-designed SFGA is no better than a full standard-cell design. The customer-designed SFGA has development-time advantages, however, and represents a lower risk than the standard-cell approach.

The advantages of SFGAs are a result of their ability to catch most of a design's uncertainties, errors, and changes. Designers will have defined their circuit's basic structure and content several weeks before finishing the design and simulation. With that basic

Looking ahead

Customer-designed special-function gate arrays (SFGAs) offer some time and risk advantages over standard-cell designs. However, since customer-designed SFGAs cost much more to develop than pure-gate-array designs, the market for the customer-designed devices is limited. Manufacturers estimate that SFGAs account for about 10% of dollars shipped in the ASIC market.

Predesigned SFGAs, on the other hand, duplicate the development-cost advantages of pure arrays and seem a welcome alternative for designers. But few manufacturers are making predesigned units because of the risks involved in their manufacture. If the manufacturer makes the wrong choices, it could waste its entire development effort. Because the overall SFGA market is small, many ASIC manufacturers are taking a wait-and-see stance before they offer predesigned products. Even then, they will offer only those products that have high-volume applications. For the moment, such applications include clock generation for PCs, data recovery, telecommunications, and designs with embedded memory.

Customer-designed units, then, will dominate the SFGA offerings for now. The number of offerings will continue to grow, but not rapidly. Customer-designed SFGAs offer only a few advantages over conventional gate arrays, and improvements in conventional array technology and in CAE tools that create soft macro blocks will erode those advantages.

One direction SFGA technology could take that would accelerate its acceptance among designers is the embedding of special functions into field-programmable gate arrays instead of conventional gate arrays. Several manufacturers are pursuing this approach. Process incompatibility between the embedded function and the programmable logic, however, has so far made the approach too expensive. Don't look for it soon.

Table 1—Special-function gate arrays

Company	Part no.	Process	No. of gates	Functions available	Costs	
					NRE	Unit
AMCC Circle No. 329	Q24P008	1.0-µm BiCMOS	800	PLL	$40,000	$20 (plastic)
	Q20P010	1.0-µm Bipolar	800	PLL	$58,000	$80 (ceramic)
	Q20P025	1.0-µm Bipolar	2000	PLL	$64,000	$125 (ceramic)
	Q20M100	1.0-µm Bipolar	10,000	High-speed RAM	$88,000	$500 (ceramic)
AMI Circle No. 330	AMI8G	0.8-µm CMOS	2000 to 450,000	RAM, 80C51, FIFO, 6502, DMA, others	$65,000	$25
Fujitsu Circle No. 331	CE31	0.8-µm CMOS	3200 to 207,000	High-speed RAM, multiplier, PCI buffer	$20,000 to $100,000	Not provided
	CE51	0.5-µm CMOS	34,000 to 754,000	High-speed RAM, PLL	$65,000	Not provided
Motorola Circle No. 332	H4C	0.7-µm CMOS	18,000 to 318,000	SRAM to 256 kbits, JTAG logic in I/O	$110,000[1]	$29 (PQFP)
	H4C Plus	0.6-µm CMOS	28,000 to 178,000	Analog PLL, SRAM, JTAG JTAG logic in I/O, high-speed I/O (GTL, CMTL, PCI, PECL), mixed 3/5V power	$110,000[1]	$36 (PQFP)
NEC Electronics Circle No. 333	CMOS-8	0.6-µm CMOS	11,000 to 233,000	Digital PLL, GTL I/O, compiled RAM, 24-mA I/O, clock tree	Not provided	$6 to $50
	CMOS-8L	0.5-µm CMOS (3.3V)	11,000 to 627,000	As above with 5V-protected I/O	Not provided	$6 to $50
	CMOS-8LCX	0.5-µm CMOS (3.3V)	40,000 to 486,000	As above with CrossCheck testability	Not provided	$6 to $50
	ECL-8	ECL	23,000 and 67,000	BiCMOS RAM,	Not provided	$233 to $770
	BiCMOS-8	0.5-µm BiCMOS	250,000	Analog PLL, 8-nsec RAM, GTL I/O	Not provided	$440
Oki Semiconductor Circle No. 334	MSM92S	0.8-µm CMOS	5000 to 132,000 (usable gates)	Compiled memory, PLL, UART, 82Cxx, SCSI controller, PCI controller, PCMCIA controller, JTAG I/O	Not provided	$13 to $15
	MSM91S	0.8-µm CMOS	2800 to 62,000	As above	Not provided	$19 to $21
Texas Instruments Circle No. 335	TGB2000E	0.7-µm BiCMOS		1-GHz I/O, high-speed MUX/DEMUX		
Toshiba Circle No. 336	TC160E/ TC163E	0.8-µm CMOS[2]	210,000 (usable)	RAM, PLL, RAMBUS interface cell	Not provided	Not provided
	TC180E/ TC183E	0.5-µm CMOS[2]	339,000	As above	Not provided	Not provided
Vitesse Semiconductor Circle No. 337	FX	0.6µ GaAs	20,000-350,000	RAM, registers, PLL content-addressable memory, divider, floating-point, pulse-formatter, counter, timing generator, timing vernier	$60,000	$150-$250
VLSI Logic Circle No. 338	VGC750	0.5-µm CMOS	15,000 to 614,000	Compiled RAM, PLL, SCSI, PCI, GTL, JTAG I/O, Flex array[3]	Not provided	Not provided
	VGC650	0.6-µm CMOS	15,000 to 614,000	As above	Not provided	Not provided
	VGC450/3	0.8-µm CMOS	4000 to 232,000	Compiled RAM, GTL, PCI, PECL, JTAG I/O, Flex array[4]	Not provided	Not provided
	VGT350/3	1.0-µm CMOS	3000 to 133,000	Compiled RAM Flex array[5]	Not provided	Not provided

Notes: [1]Special I/O, JTAG, and PLL built in. An additional $45,000 NRE for fully-diffused functions such as memory.
[2]TC163 and TC183 offer mixed 3/5V operation.
[3]Flex array options include datapath compiler, PLL, delay-locked loop, and ROM compiler.
[4]Flex array options include Note [3] options plus multiplier compiler and multiplier/accumulator.
[5]Flex array options include RAM, ROM, and datapath compilers.

definition in hand, you can initiate production of the SFGA base wafer with an uncommitted array. The base wafer will be available for adding the final metal layers once the design is complete. This action can cut weeks off the development cycle of a standard-cell approach, which can't undergo fabrication until final simulation.

The SFGA approach not only speeds a design to prototype, but also involves less financial risk because designers can accommodate last-minute design changes in the logic array. Thus, a mistake or a last-minute specification change affects only the metal layers, not the entire mask set. Mistakes and changes also do not make obsolete any stock of unmetallized base wafers. Similarly, an SFGA allows you to make production design changes quickly and with minimal cost. You can even reuse an SFGA base wafer on similar projects to spread NRE over several designs.

SFGA limitations

The SFGA approach has drawbacks, however. For example, the resulting design is less dense than a full standard-cell approach. Further, a core-limited design causes the SFGA to have greater unit cost in production. If it is pad-limited, you should check to see if a pure gate-array design fits in the space circumscribed by the pads. If it will, the density benefits of embedding a special function are lost.

Also, SFGAs can take longer to place and route metal traces than do conventional gate arrays. Manufacturers estimate that this step takes 50 to 100% longer with SFGAs because it is difficult to place traces across the special-function area. Because the special function has fixed I/O points between the function and your circuit, the place and route may be awkward.

If you pursue the SFGA approach, you should discuss several issues with potential suppliers. For instance, find out how the vendor characterizes the combination of a function block and the gate array. Production of nearly any semiconductor involves slight process adjustments (tweaks) to improve yield or performance of the design. Thus, even when using the same base process, manufacturers may have fabricated gate arrays and functional block designs under different conditions before characterization, resulting in errors in simulation models. If available, sample silicon containing that core embedded in an array can eliminate that risk by providing a real-world check.

Another topic to investigate when evaluating potential suppliers is the level of design support they provide. Check if the vendor has tools specifically for the design of an SFGA. Also, make sure the vendor provides design support for the functional blocks you choose. Vendors sometimes license high-level blocks from other sources. Thus, they can fabricate and test designs using that block but may not be able to resolve problems when embedding the block into an array.

Design flexibility is another consideration. Some vendors have only a few functional blocks you can embed in an array. There may also be restrictions on the placement of blocks within an array or the size array available for modification. A limited selection of array sizes may not be a disadvantage, however. If you have predefined base arrays, the vendor can provide standardized test fixtures. Using a random-sized array means that you'll pay for your own custom test fixture.

Finally, consider the future. As process lithography improves, so does circuit performance. If you plan on taking advantage of those improvements, be sure that your vendor has plans to move its offerings, including both the array matrix and the special functions you embed, to the new lithography. EDN

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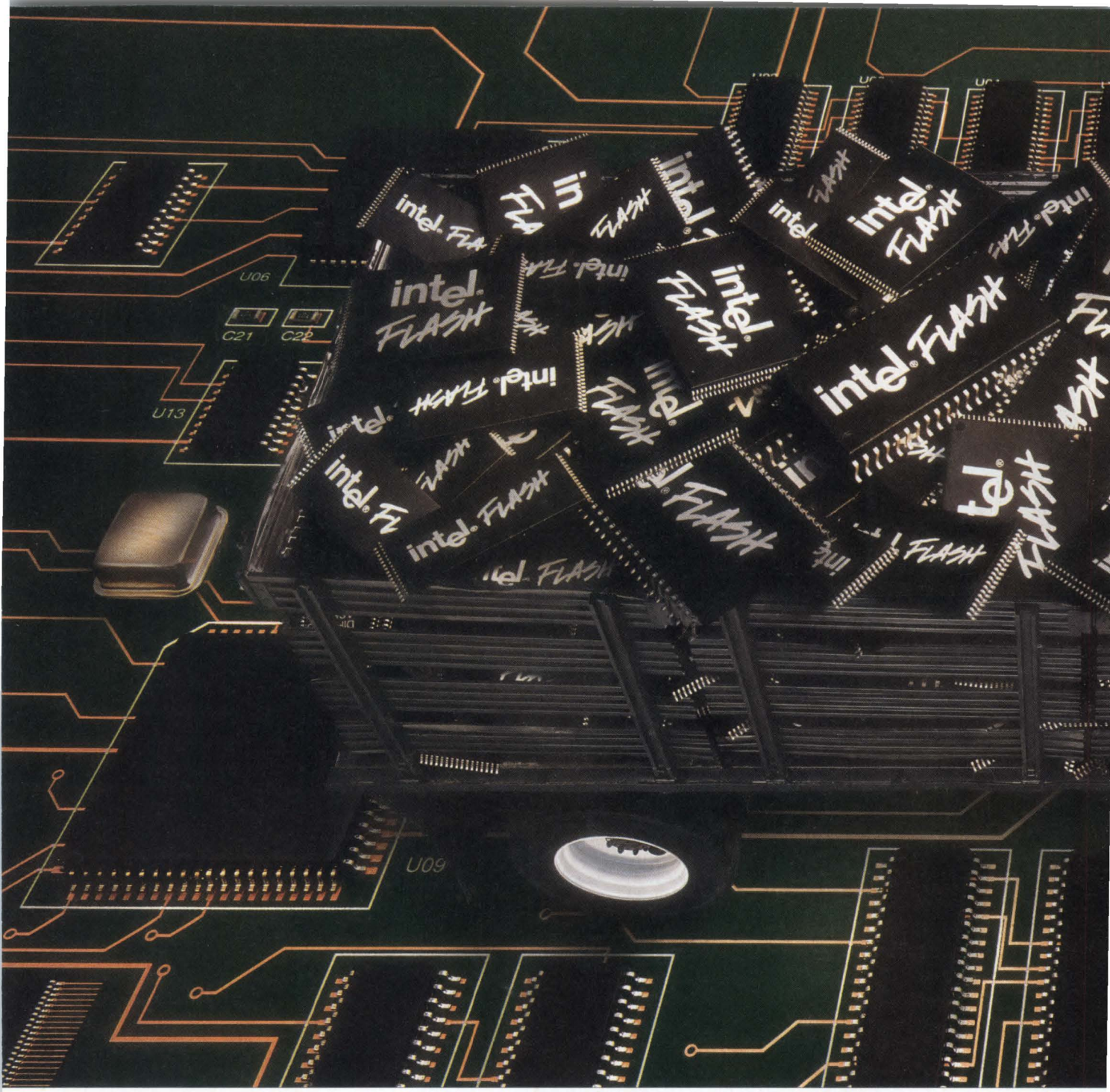

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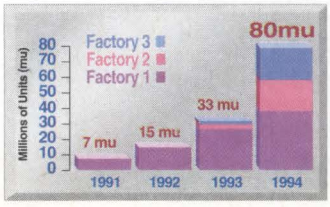

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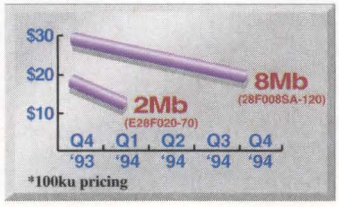

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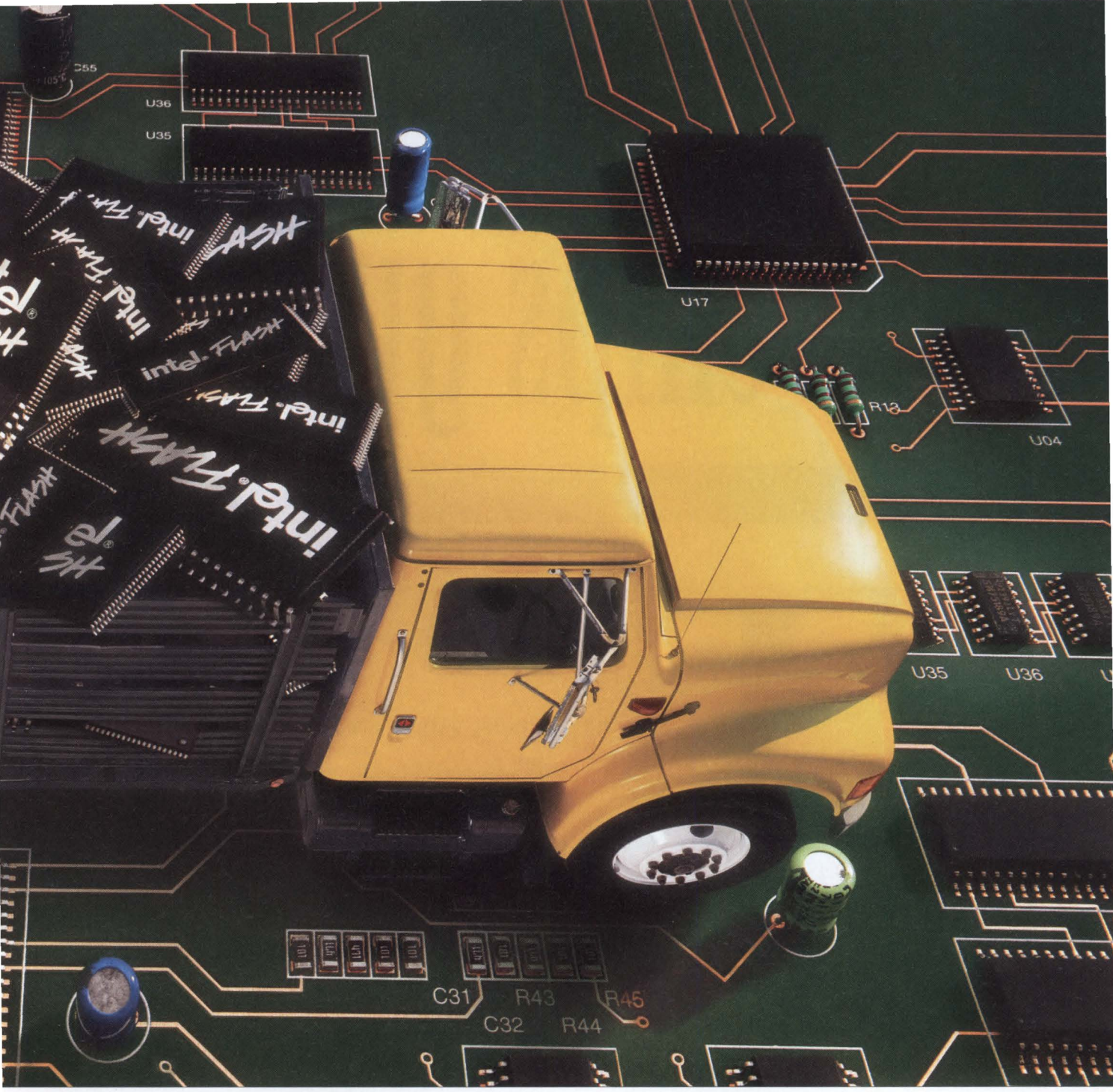

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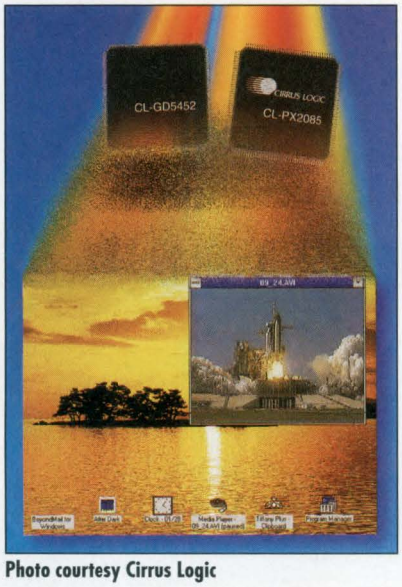

Photo courtesy Cirrus Logic

If you think video on a desktop computer has to mean small images and jerky motion, think again. The latest video chips can fill a PC's entire screen, or any part of it, with smooth, realistic motion.

If you've been unimpressed with PC-based video, it might be time for a second look. The video you've seen so far has probably filled only a fraction of a PC's screen while jerking along at maybe 15 frames/sec, producing an annoying strobelike effect. PC video is dramatically improving, though, thanks to some new video ICs. These chips produce images with the size, the resolution, and the motion quality of television video, the apparent standard of acceptable quality for most people (see **box**, "TV on a PC").

PC video's quality improvements reflect the innovative merger of video and graphics. For example, dual-port RAMDACs accept both graphics and digital video data and merge the two to make a "video-in-a-window" display. In addition, new video-processor ICs that work with the RAMDACs (or directly with graphics-accelerator chips) provide a computing boost that dramatically improves video's image and motion quality. Some RAMDACs even perform some video processing themselves.

Easy video upgrades

Dual-port RAMDACs make it especially easy to upgrade a graphics-subsystem design to include video. All you have to do is add a connector for the input of digital video data (for example, from an NTSC decoder or from image-decompression software or hardware) and replace a conventional RAMDAC with one of the dual-port versions. The dual-port RAMDACs include Video

TV-quality video

GARY LEGG, SENIOR TECHNICAL EDITOR

CacheDACs from Brooktree and MediaDACs from Pixel Semiconductor (a subsidiary of Cirrus Logic). With 135-MHz pixel-clock rates, they can generate 1024×768-pixel displays with 24-bit color at high refresh rates.

It takes video processing, though, to make PC video perform up to users' expectations. Without hardware assist, video on even a powerful Pentium-based computer is limited to small images, jerky motion, or both.

Although dual-port RAMDACs contain some video-processing hardware, separate video processors add more. For example, RAMDACs from Brooktree and Pixel can perform color-space conversion (video's YUV format to a graphics system's RGB), and the Brooktree Bt885 (**Fig 1**) can also perform some video-image resizing, or scaling. Video processors perform these tasks and others, and their scaling is more sophisticated. Companies with recently introduced video processors include ATI Technologies, AuraVision, IBM Microelectronics, Intel, Pixel, S3, Trident, Tseng Labs, VideoLogic, Weitek, and XTechnology (Xtec).

At the most basic level, designs with dual-port RAMDACs use an approach called DAC-attach, in contrast to the memory-attach approach (**Fig 2**). In a DAC-attach design, a dual-port RAMDAC multiplexes digital video and graphics data to a display device. Multiplexing occurs pixel by pixel, with either a video or a graphics pixel converted to analog, depending on previously specified overlay coordinates or color keying. (In color keying, video pixels replace a block of graphics pixels that the application has generated in a particular color and denoted as an overlay area.) In memory-attach implementations, video and graphics both connect to the same frame-buffer memory. The Shared Frame Buffer Interface (SFBI), a proprietary implementation by ATI Technologies and Intel, is perhaps the best known of these.

There is no shortage of variations on these schemes, however, with the main goal being a shared frame buffer without memory attachment. This scheme saves the cost of redundant memory but avoids some of the complications of memory attachment. It requires a graphics processor with a video port, several of which are now—or soon will be—available.

To avoid incompatibilities in PC-video products, the Video Electronics Standards Association (VESA) has created two specifications that address short- and long-term issues. The VESA Advanced Feature Connector (VAFC) helps add video capability to graphics subsystems by providing a standard interface between video and graphics (**Fig 3**). The VESA Media Channel, also called VM Channel (VMC), addresses latency requirements for real-time performance and allows the connection of multiple multimedia devices (**Fig 4**).

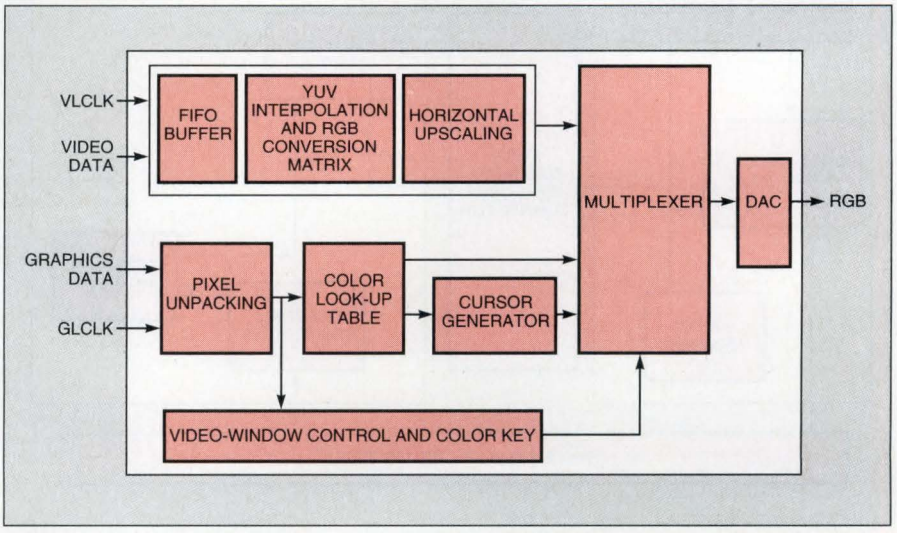

Fig 1—Dual-port RAMDACs accept both graphics and digital data and merge the two for display. As shown here in Brooktree's Bt885, they can also perform some video-processing functions.

VAFC-compatible products—for example, Pixel's CL-PX2085 MediaDAC (**Fig 5**)—are just now starting to become available; VMC has not yet been fully implemented.

The newly specified VAFC extends the old VGA Feature Connector. The 8-bit VGA implementation is suitable for 256 colors on 640×480-pixel displays, but it is inadequate for higher-resolution and "true-color" displays. VAFC provides a 16- or 32-bit data path with 75- or 150-Mbyte/sec data transfers, respectively.

Physically, VAFC comprises an 80-pin connector and some circuitry for clocks and sync signals. The circuitry is relatively uncomplicated and goes inside a chip—a RAMDAC or a video IC, for example—to create a VAFC-compatible interface. VAFC's main benefits are the ease and the low cost of making graphics designs "video enabled" and compatible with products from numerous companies.

VESA specifies both a "baseline" implementation of VAFC, primarily for compatibility with older graphics designs, and an "extended" implementation, for higher performance. An extended implementation of VAFC requires a dual-port RAMDAC that allows asynchronous input of video and graphics. These devices capture video input in a FIFO buffer, decoupling it from the graphics pixel clock. Pixel's CL-PX2085 MediaDAC (with VAFC) is FIFO-based, as are the CL-PX2080 MediaDAC and Brooktree's Bt885 Video CacheDAC (without VAFC).

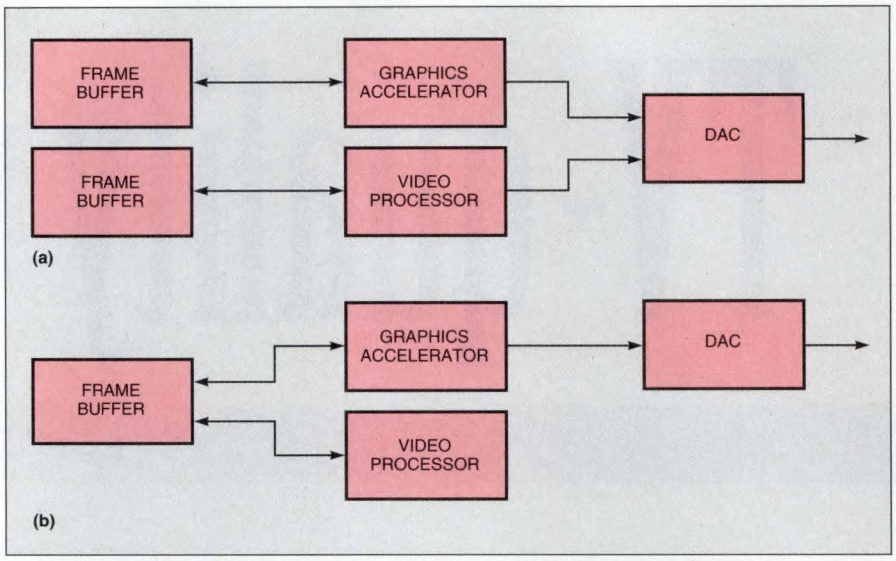

Fig 2—In a DAC-attach video implementation (a), the video and graphics subsystems have separate frame buffers. Video and graphics data merge for display in a special RAMDAC that has separate video and graphics ports. In a memory-attach implementation (b), the video and graphics subsystems connect to a shared frame buffer.

Video requirements simplified

Extended VAFC's asynchronous operation frees the input video from graphics' more stringent resolution requirements, permitting use of video data in any of its various lower-resolution native formats. The video frame buffer thus requires less memory, and the video-input channel requires lower bandwidth. In addition, the video data can enter the RAMDAC at any time, even during the graphics subsystem's blanking intervals.

When low-resolution video merges with higher-resolution graphics, however, the video image requires scaling to a larger size. Otherwise, you would be substituting video data for graphics data pixel by pixel, and the video image would fill only a small part of your display. For example, a 320×240-pixel small-image format (SIF) image, which is commonly used in PC video, would fill only about 10% of a 1024×768-pixel display. More generally, a video image must be scalable up or down to fill as much or as little of a display as a computer user desires.

The new video processors use pixel interpolation for scaling, thus yielding enlarged images that are smooth and natural-looking. In contrast, pixel replication—an earlier and simpler technique—simply duplicates certain pixels in the enlarging process, producing images with a blocky, mosaic-like appearance. Pixel interpolation can't add detail that an original image doesn't have, but modest magnification

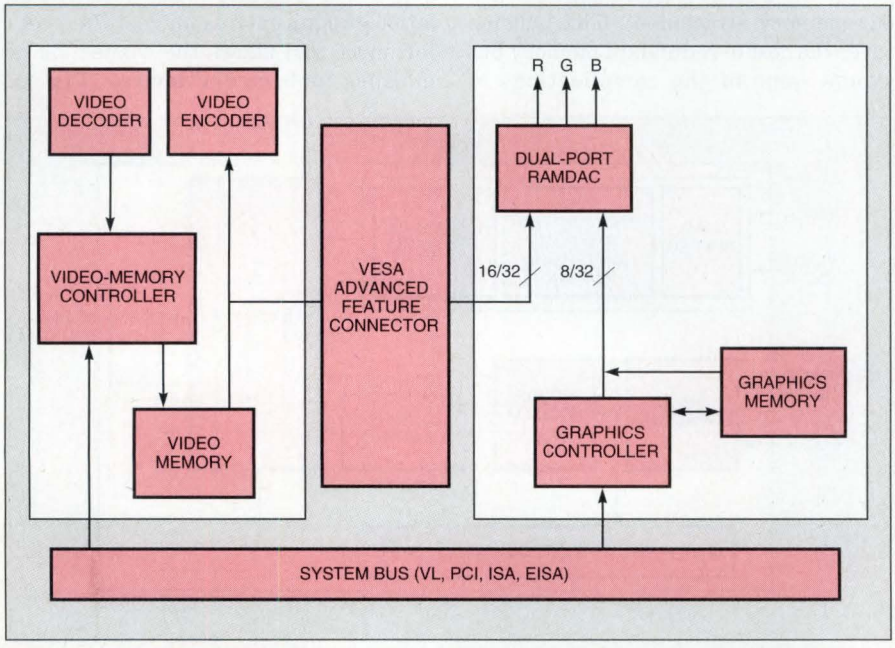

Fig 3—The VESA Advanced Feature Connector (VAFC) provides a standard interface between a video subsystem and a graphics subsystem's dual-port RAMDAC. The 16- or 32-bit VAFC has a much higher bandwidth than the old 8-bit VGA Feature Connector.

yields images that most people find acceptable. Video chips typically provide a maximum of four times greater expansion, although images start to look a little fuzzy after about two and one-half times.

Some limited scaling is possible without a video processor, as in Brooktree's Bt885 Video CacheDAC. The Bt885 performs horizontal upscaling and provides support for vertical upscaling by an external device.

Video processors can also scale down images, shrinking them into less space to fit multiple images on a screen. Pixel's CL-PX2070 video processor, for example, provides four video windows, but some processors allow multiple windows only by overlaying a large video image with a smaller one. Typically, a video processor can scale an image down to 1/128 of its original size.

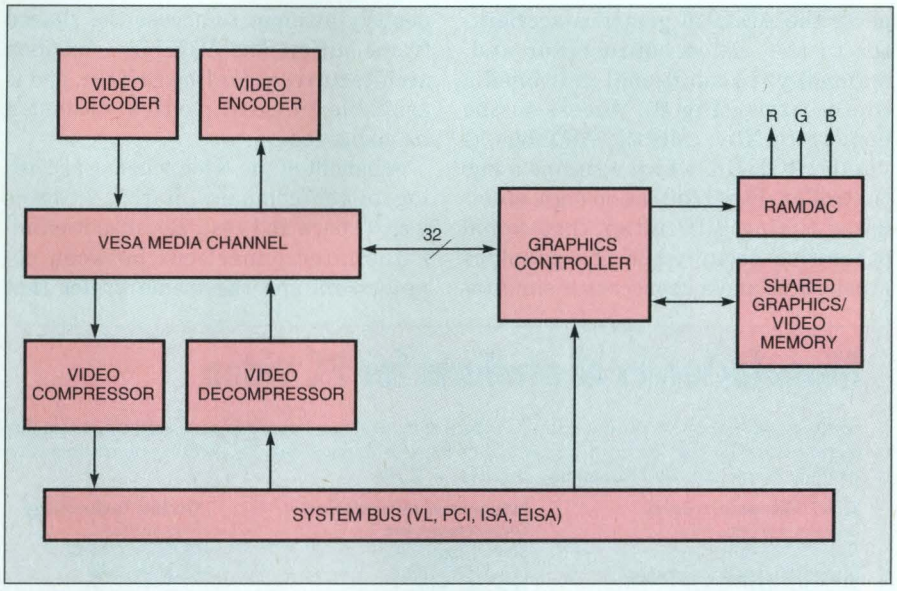

Fig 4—The VESA Media Channel, also called VM Channel, allows video and graphics subsystems to share a frame buffer. It also addresses latency requirements for real-time performance and allows the connection of multiple multimedia devices.

Versatile video processors

Other functions performed by video processors may include color-space conversion and dithering. In color-space conversion, video data (usually YUV) becomes graphics data (RGB). Dithering enables the display of image-quality color on systems not designed for imaging—for example, the display of 24-bit true color, with a palette of 16 million colors, on a system designed for 8-bit color, or a palette of 256 colors.

Increasingly, video processing occurs in coprocessor chips that connect directly to graphics chips. IBM Microelectronics' Video Integration Processor, for example, is implemented in special versions that attach to S3's Vision964 graphics accelerator and to Xtec's AGX016.

In Xtec's alternative shared-frame-buffer approach, a special bus con-

TV on a PC

Television picture quality isn't very good, but we're used to it. We usually watch TV from across a room, and standard TV resolution is fine at that distance. Watching a tabletop TV from 12 ft away is roughly equivalent to looking at a wallet-sized photograph at arm's length. If you replace the photograph with a digital image, you won't need many pixels to represent it.

But most video on PCs, until now, has not measured up even to TV quality. PC-video images have been less detailed—perhaps 320×240 or only 160×120 pixels—and we see them up close, where resolution takes on extra importance. You could get around resolution limitations by displaying a very small image—in fact, hardware limitations practically mandated a small image—but that's not satisfactory to most users, either.

What does seem to be satisfactory is plain old TV. In North America, a TV display uses 525 horizontal scan lines, of which 485 have picture content. Resolution within a scan line varies, but it is usually adequate to distinguish at least 300 vertical lines. Distinguishing 2300 lines requires 600 pixels. Thus, a 600×485-pixel display—or, conveniently, a VGA-format 640×480 display—provides acceptable resolution for PC video (**Ref 1**).

Because we see PC-video images up close, we accept smaller images than we would on a TV. For example, a 9-in. (diagonal) image on a PC, when seen from a typical distance of 2 to 3 ft, corresponds to a 27-in. TV viewed from 6 to 9 ft. You can make the image larger on a PC, but then you might perceive a lack of sharpness.

We're not accustomed to jerky motion on a TV, and we don't want it on a PC, either. Anything less than about 30 frames/sec produces a flickering effect. We also want realistic color, which, by most accounts, requires 24 bits/pixel for images in RGB format or 16 bits/pixel for YUV format. With fewer bits/pixel, an image loses subtle gradations in color and shading.

The latest video ICs, notably video processors and coprocessors, have the computing power to produce TV-quality images on a PC. They provide the necessary frame rates for realistic motion; they accommodate enough bits/pixel for realistic color. They do fudge a little in making images as large as we want, but the results are usually acceptable.

Video chips must enlarge small images to fill a display space, and they accomplish this task by interpolating between pixels in the input image to produce additional pixels for the output. Typically, they start with a digitized image of 320×240 pixels (sometimes 160×120) and scale it to 640×480 or larger. Images that result from 2-times scaling look fairly good; 4-times scaling produces rather soft images.

nects the AGX016 graphics accelerator to the vision coprocessor and, optionally, to additional multimedia coprocessors (**Fig 6**). Access to the bus, which Xtec calls the AGX bus, is via the AGX016, which contains a bus controller. Bus-arbitration logic eliminates timing difficulties that would otherwise occur when the graphics accelerator and a coprocessor simultaneously attempt to access the shared frame buffer. The AGX bus is an open architecture, according to Xtec, and is available to third parties without a licensing fee.

A benefit of the Xtec scheme, according to the company, is that it saves board space and cost. Because it eliminates interconnections between coprocessors and the frame buffer that must also exist between the graphics chip and the frame buffer, coprocessors can fit in 84-pin packages instead of more expensive 208-pin devices.

Save memory: Share a frame buffer

Another approach that saves cost links Oak Technology's OTI-107 graphics chip with Brooktree's Bt885 Video CacheDAC. The two chips work togeth-

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er with a single frame buffer that holds both graphics and video data in only 1 Mbyte of memory. Yet, the graphics and video data are separate; one type does not destructively overlay the other.

The key to this implementation is in the storing of video data in an unused part of the memory. The frame buffer for an 8-bit (256-color), 1024×768-pixel graphics subsystem requires only 75% of the 1 Mbyte of memory found on low-cost VGA boards. The remaining 25% holds two 16-bit, 320×240-pixel windows of video data stored in YUV format, and, because YUV doesn't replicate luminance information as RGB does, the displayed video images are equivalent to 24-bit RGB true color. The Bt885 converts the video to RGB as it goes to the display.

No matter how video and graphics data merge, a larger problem involves additional multimedia data, such as audio. Ultimately, then, different types of data need to move around in a system at very high rates. For these high-bandwidth transfers, a multimedia bus is necessary.

Two buses are competing to handle multimedia data—the VMC and a form of the Peripheral Component Interconnect (PCI) bus. The PCI implementation is a secondary bus, created atop a regular PCI bus with a PCI-to-PCI bridge chip. The purpose of both VMC and the secondary PCI bus is to handle only multimedia devices; they're distinct from the VESA-local (VL) and PCI-local buses that computers use to connect other types of peripheral devices.

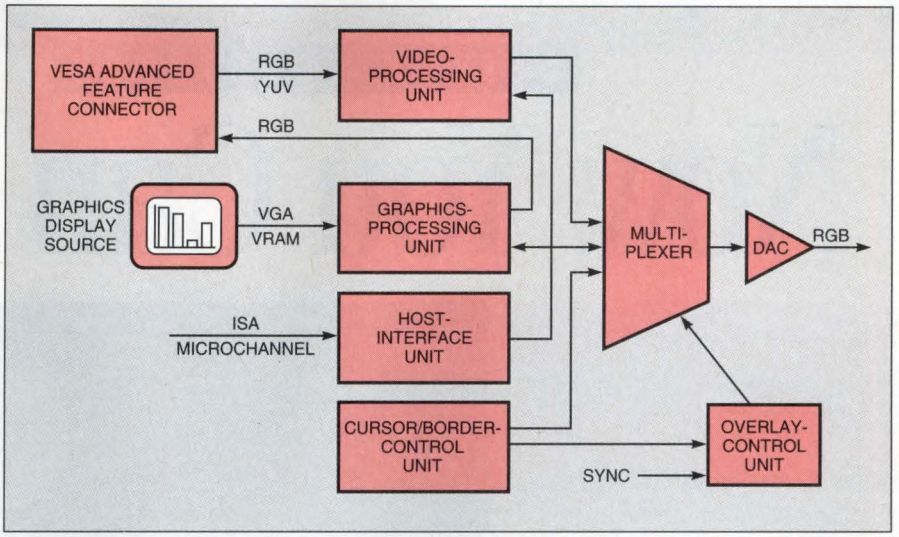

Fig 5—Chips that are compatible with the VESA Advanced Feature Connector (VAFC), such as this CL-PX2085 MediaDAC from Pixel Semiconductor, provide a standard link to other components.

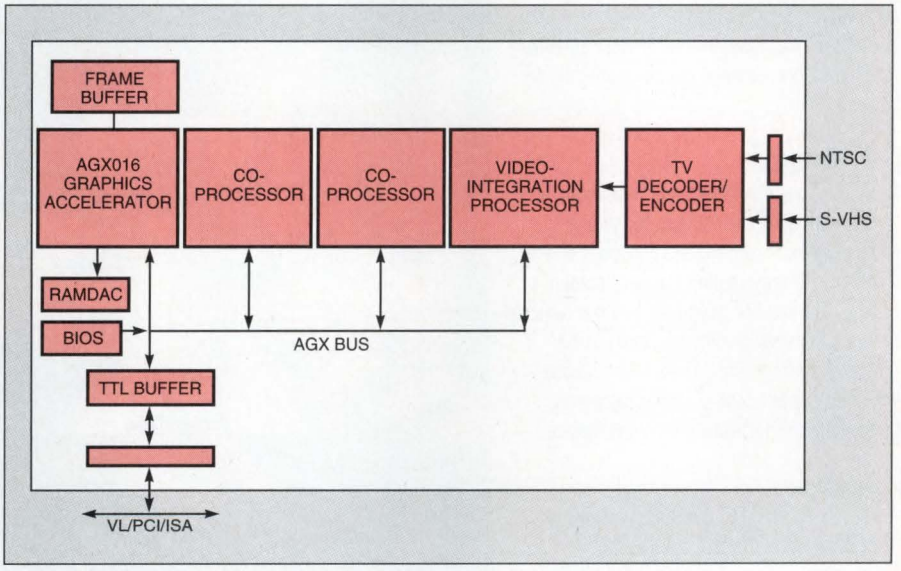

Fig 6—A special bus in Xtec's AGX016 graphics accelerator lets a video subsystem share the graphics frame buffer via the graphics chip. This approach avoids the replication of frame-buffer connections in a memory-attach implementation, thus allowing use of an 84-pin video processor instead of a more typical 208-pin device.

Multimedia bus needed

Although the VL bus and a primary PCI bus have the necessary bandwidth for multimedia data, they do not specifically address multimedia's stringent latency requirements. VMC is designed for multimedia problems, such as synchronizing video with audio. PCI is not, but its backers say that a dedicated, secondary PCI bus can handle multimedia just fine. In any case, neither VMC nor PCI is yet ready for multimedia, although many of the pieces are in place.

VMC is a better technical solution than PCI, say some PC-video marketers, but that doesn't necessarily guarantee its success. With the powerful backing of Intel, PCI's creator, a secondary PCI bus could yet prevail. EDN

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With the demand for integrated data, graphics, voice and video transmission capabilities, designing products for the subscriber side of wireless will require IC-level products with wide data bandwidths, low power, CODEC capabilities and extremely high on-chip integration. And because of user location and wireless infrastructure limitations, satellite uplink capabilities will be required.

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As the number of wireless users continues to grow, so also will the demand for seamless communications capabilities regardless of user location. This may require the development of multiple close-range microcells (<a few hundred meters) deployed around fast and flexible macrocell base stations. These base stations will need a great deal of computing power, bandwidth and software-driven intelligence.

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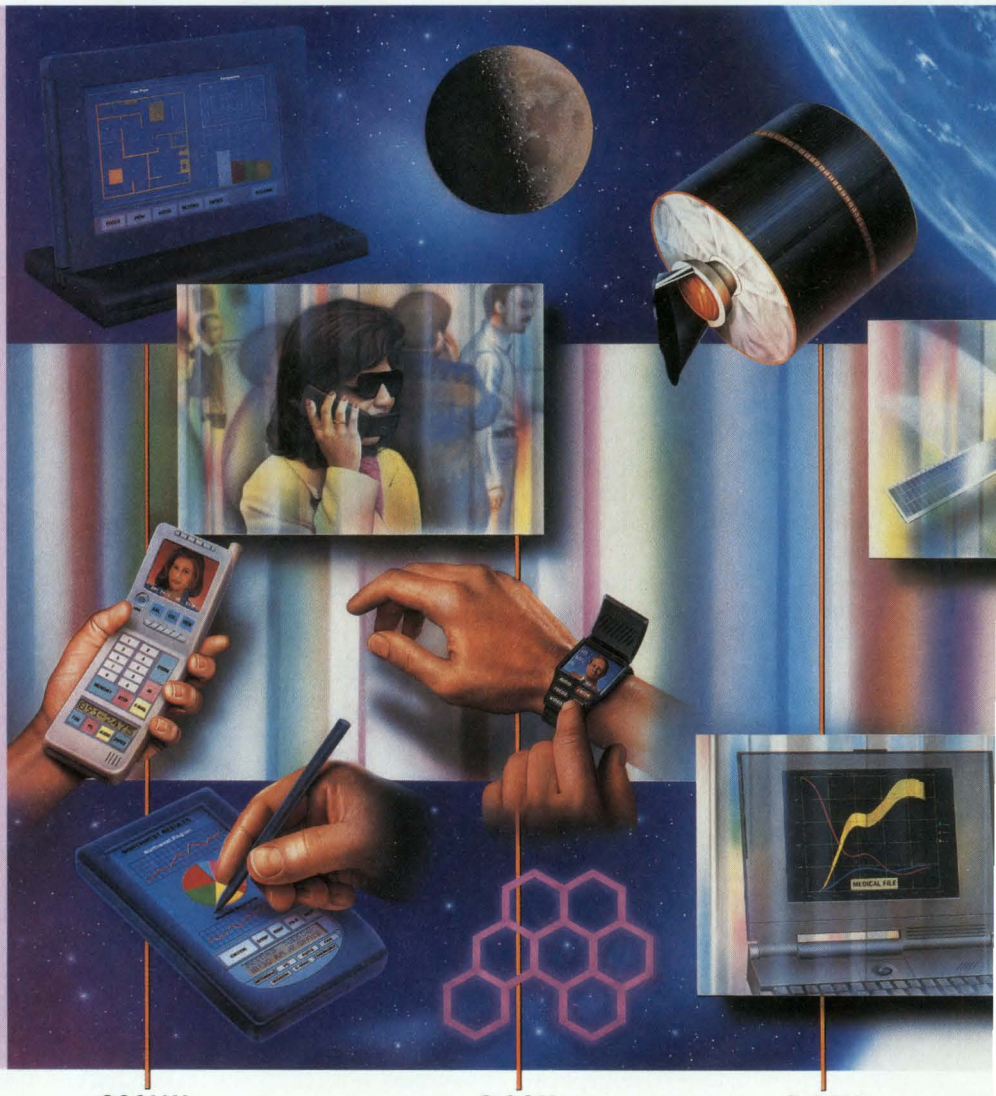

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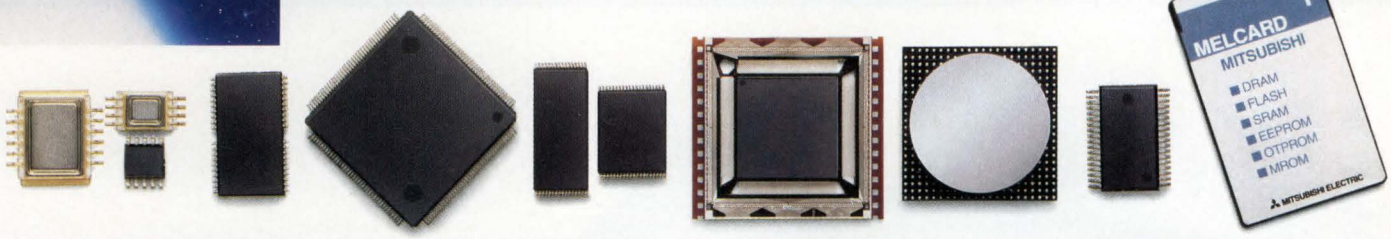

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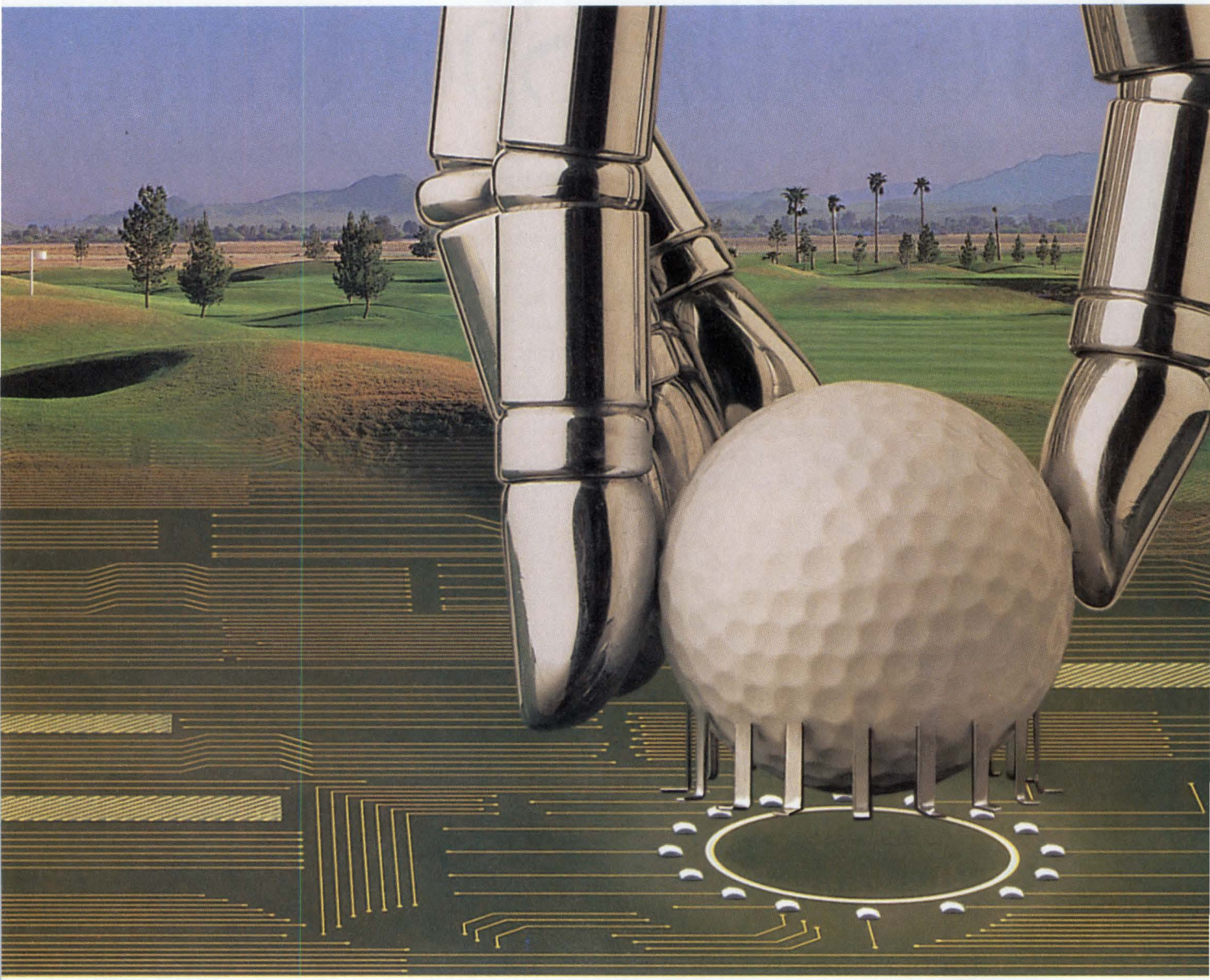

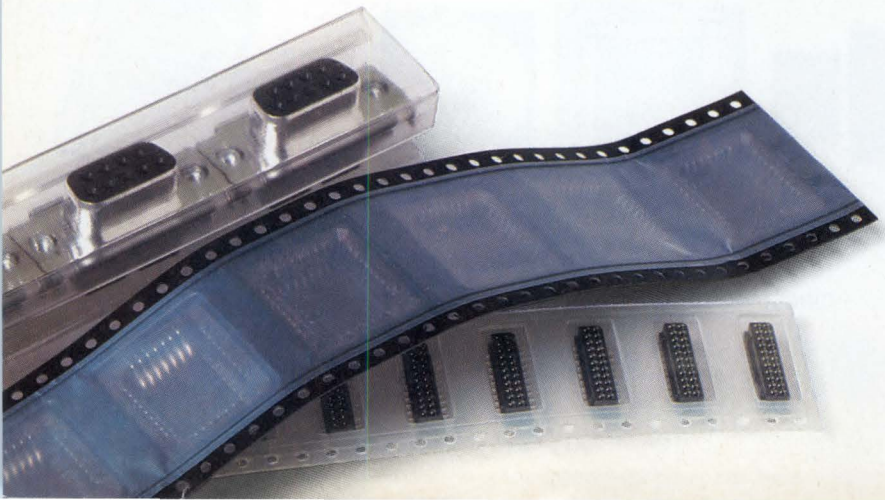

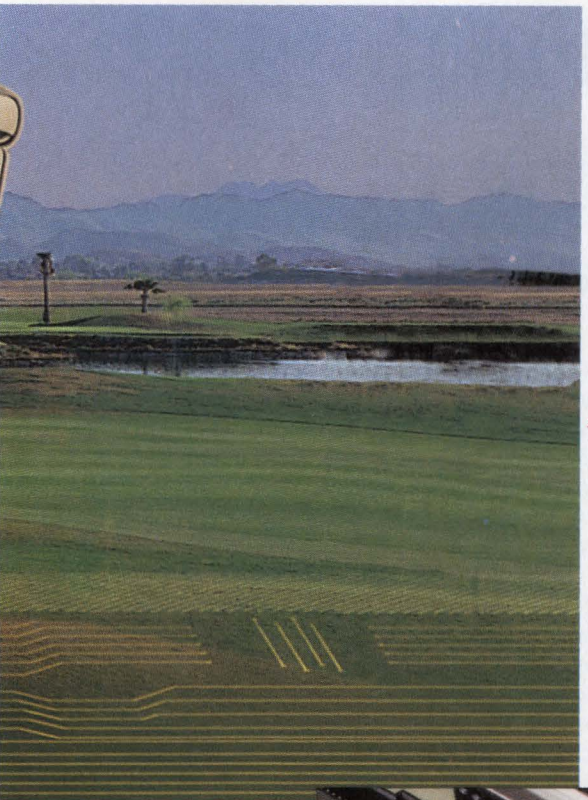

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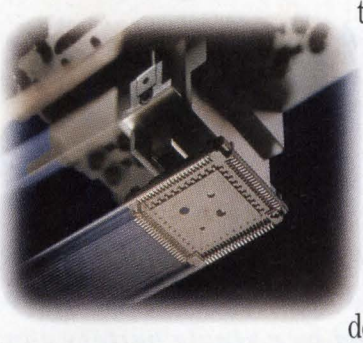

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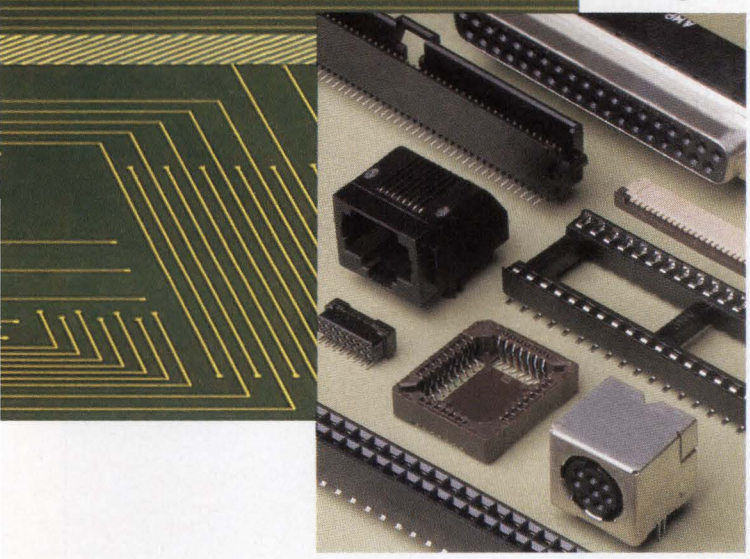

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CIRCLE NO. 49

The right μP simplifies using induction motors to propel electric cars

Jeff Baum and Ken Berringer, Motorola Inc

Induction motors are inexpensive and reliable. Controlled by an appropriate μP, a PWM inverter powered by a single battery can generate waveforms that appear to such motors as the 3-phase, variable-voltage, variable-frequency sine waves they need for speed control

In electric vehicles (EVs), ac induction motors can provide variable speed at low cost. The most common method for controlling induction motors uses a 3-phase ac voltage-source inverter with sine-wave PWM. Because the motor's speed and acceleration depend on amplitude as well as frequency, the inverter must produce sine waves of variable voltage and frequency. A single microcontroller can provide control functions while generating PWM waveforms in which the modulation is sinusoidal.

Motorola's MC68332 (332) is particularly well-suited to controlling induction motors. The 332 is built around the CPU 32, a 32-bit core whose instruction set is almost identical to the MC68020's. A new table-look-up-and-interpolation (TBL) instruction, performs linear interpolation between points in a look-up table. You can use TBL to generate very precise sine waves from a relatively small table.

The 332 also contains a time-processor unit (TPU), a dedicated microcoded processor that handles time-related tasks. One of its microcoded primitives, synchronous PWM (SPWM), generates three PWM waveforms for the induction motor. These waveforms have the same period, independently varying pulse widths, and well-controlled time relationships among phases.

The TPU limits the minimum and maximum pulse widths, the minimum offset between waveforms, the worst-case latency, and the update coherency. This article describes an algorithm for generating sine waves of variable voltage and frequency by lowpass filtering or integrating a rectangular "pulse" waveform produced by switching a fixed-voltage dc source on and off. The CPU handles all calculations and periodically updates the TPU output waveforms. This article also presents relationships among such algorithm parameters as PWM frequency and sine-wave voltage resolution.

BBS The software listings in this article are available on *EDN*'s computer bulletin-board system (BBS). Phone (617) 558-4241 with modem settings 300/1200/2400 8,N,1. Access the */freeware* SIG and specify the *(r)ead* option followed by a *(k)eyword* search for "MS706." You can also download the listings from a BBS run by the authors' employer, Motorola Inc. Access that BBS at (512) 891-3733. Modem settings are the same as for the *EDN* BBS.

EVs—a 100-year history

Early EVs used dc motors and SCR choppers to control motor speed. Both the motors and the control circuits limited EV performance. Brush arcing limits the speed range of brushed dc motors, requiring the use of a transmission with its associated losses. Many EVs have used series- or shunt-wound motors, which require complex excitation circuits to allow regenerative braking.

Brushless, permanent-magnet dc motors are used in many low-power applications. Electric vehicles might use large brushless dc motors, but such motors would likely be larger and heavier than induction motors of comparable horsepower. Also, the cost of the perma-

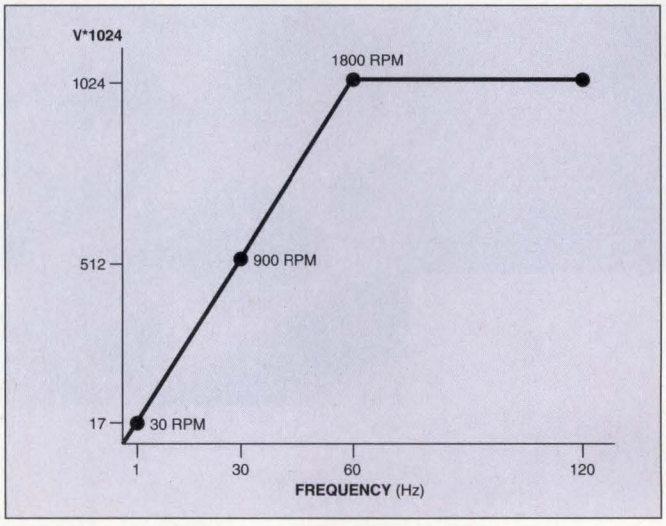

Fig 1—You control the speed of an ac motor by controlling the ac power frequency. At low frequencies, you must reduce the applied voltage. Once the voltage reaches the system limit, applying higher frequencies makes the motor turn even faster—provided that it can withstand the higher speeds. In this mode, represented by the horizontal portion of the curve, the motor can deliver the same power at all speeds.

nent magnets makes brushless dc motors more expensive.

A variety of applications have employed 3-phase ac induction motors for many years. They are readily available in a wide range of sizes from ¼ to more than 1000 hp. In the 1960s, the advent of large bipolar power transistors made it possible to build variable-speed systems using conventional induction motors. Complexity and cost limited these drives to industrial applications whose need for variable speed was acute. Also, the low switching speeds of the larger power semiconductors limited the drives' operating frequencies to the audible range. Although the audible noise of a large variable-speed drive might be acceptable in a noisy industrial environment, it is undesirable in a consumer vehicle.

Because of their low switching frequency and abrupt switching, SCR choppers produce large amounts of acoustic and electrical noise. Conventional bipolar devices run at higher frequencies (5 kHz) but still operate within the audible range. The recent development of high-speed insulated-gate bipolar transistors (IGBTs) allows large variable-speed drives to operate at 20 kHz. This is a substantial improvement over drives built from conventional bipolar devices.

The EV market is about to explode

EVs provide a potentially large consumer market for variable-speed induction-motor drives. The California legislature has mandated the production of EVs by 1998. Although the exact configurations of motor type, transaxle, and battery voltage are still subject to much debate, other requirements are quite clear. A practical EV will have an inverter or inverters capable of supplying 50 to 100 kW at high switching frequencies. The most promising approach is a high-speed ac induction motor and a 3-phase IGBT inverter.

Induction motors normally operate from three nearly sinusoidal voltages, 120° apart. Originally, these motors operated at constant frequencies and voltages (for example, 60 Hz and 230V ac). Induction motors are not synchronous machines; they run at less than synchronous speeds. The difference (in effect, the slip frequency) depends on the load and the applied voltage. Induction motors are relatively inexpensive to manufacture. The rotor, a copper squirrel cage within laminations, does not require expensive permanent magnets. Because 3-phase induction motors deliver constant, nonpulsating power and present a balanced inductive load to the power source, they are ideal for transmitting large amounts of power.

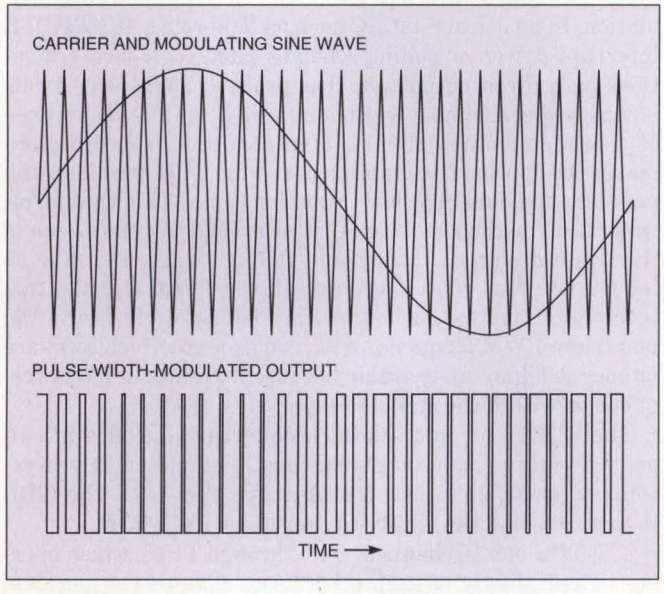

Fig 2—Conceptually, you can create sinusoidal PWM by connecting the ungrounded end of a ground-referenced load to one of two equal-magnitude, opposite-polarity supplies whenever a carrier's instantaneous voltage exceeds the modulating sine wave's instantaneous voltage.

To run an induction motor at variable speeds, you must vary the sine-wave frequency. To keep the motor's magnetic structures from saturating, which would reduce efficiency and could allow destructively large currents, you must also vary the applied voltage. Two common methods of controlling the motor speed are constant voltage-over-frequency control (constant V/F) and closed-loop, or vector, control.

Vector control has many advantages for EV applications: It uses a current-feedback loop that limits motor currents and protects the power devices. A closed-loop speed control can provide a controlled acceleration profile. In fact, you can program a closed-loop system to make an EV "feel" exactly like an internal-combustion vehicle, with all of its idiosyncrasies. Nevertheless, because of the complexity of vector control, the rest of this article deals only with simpler control methods. The principles of sine-wave generation also apply to vector control based on algorithms in which voltage and frequency are outputs.

The simplest form of ac-motor speed control is open-loop constant V/F. A conventional ac motor is usually rated at a specific voltage and frequency, such as 230V ac and 60 Hz. If you hold the voltage-to-frequency ratio constant, the motor produces a constant maximum torque. For example, if you operate a 230V 60-Hz ac motor at 115V ac and 30 Hz, it produces the same torque at about half the speed. Because it functions open loop without any speed feedback, this system allows slip. Usually the slip frequency is fairly low, allowing the use of open-loop control in many variable-speed applications. If the load torque is a well-defined function of speed, you can characterize the actual motor speed as a function of the applied voltage and frequency.

To improve the speed range, many constant-V/F controllers also operate in a constant-power region. Even when the output voltage reaches the system's maximum, the frequency can increase further. Because the voltage doesn't increase, the maximum torque decreases, and the maximum output power remains constant. Thus, a motor can produce half as much torque at twice the speed. **Fig 1** shows a plot of voltage and frequency for a constant-V/F controller with a constant-power region. This curve characterizes a motor rated at ¾ hp and 1800 rpm, at a nominal line voltage of 230V ac and 60 Hz. You must not operate conventional ac induction motors beyond their rated speed unless you are sure that they can sustain the higher speeds without damage to their rotors or bearings. Motors for high-speed operation are often smaller and less expensive than conventional motors. Therefore, EVs that use small high-speed motors can be smaller, lighter, and less expensive than vehicles that use conventional motors.

CONTROLLING AC-MOTOR SPEED

Today, the most common ac-motor inverter is a hard-switched, 3-phase PWM circuit. PWM drives apply a train of fixed-amplitude, high-voltage, high-frequency pulses to the motor and vary the duty cycle, or pulse-high time. The average voltage over each cycle is then the peak-to-peak voltage times the duty cycle. A variable-voltage, variable-frequency sine wave pulse-width modulates the duty of each phase. This simple principle allows a fixed-voltage power supply to generate variable-frequency, variable-amplitude, 3-phase sine waves.

The actual voltage applied to the motor is a constantly changing train of pulses. The motor currents are nearly sinusoidal, however, because the motor's inductance and back EMF limit the high-frequency ripple current. In effect, the motor inductance integrates the applied voltage minus the motor's back EMF. As a result, even though the applied voltage contains a large high-frequency component, the motor dissipates little high-frequency power.

$$V=L\cdot dI/dt,$$
$$I=(1/L)\int(V-EMF)dt.$$

Integrating over one PWM period produces the high-frequency ripple current. The motor resistance also has some effect on the motor current, especially at low speeds.

It is easiest to envision a system using a bipolar power supply and motor windings grounded at one end. In other words, you can visualize the supply as producing equal positive and negative voltages and the inverter as connecting the winding's ungrounded end to the positive supply, the negative supply, or neither. In fact, the battery voltage is unipolar, and the motor's 3-phase windings are usually "delta" connected. That is, each inverter drives one end of two windings. At any instant, a winding is connected in one of four ways: a) both ends at V_C, the supply voltage—no current flows; b) both ends at ground—no current; c) end A at V_C and end B grounded—current flows from A to B; or d) end B at V_C and end A grounded—current flows from B to A.

You can best understand the generation of sine-wave PWM waveforms by superimposing a sine-wave signal on a triangle or sawtooth carrier. When the carrier's amplitude is higher than the sine wave's instantaneous value, the output level is high, as **Fig 2** illustrates.

You can use analog methods to generate PWM waveforms by using a variable-frequency sine-wave oscillator, a fixed-frequency carrier-wave oscillator, an analog multiplier, and a comparator.

μP directly implements PWM

An EV motor-drive waveform generator should accurately control speed by providing a high-resolution approximation of 3-phase sine waves and by smoothly varying the sine-wave voltage and frequency. A more elegant approach than the preceding scheme eliminates the analog sine wave by performing all calculations in the discrete-time domain. This approach provides the most accurate control over the effective sine-wave amplitude and frequency. A single microprocessor generates all three PWM signals and provides control functions, communications, and a user interface. This article describes an ac drive system that uses Motorola's MC68332 microcontroller (μC).

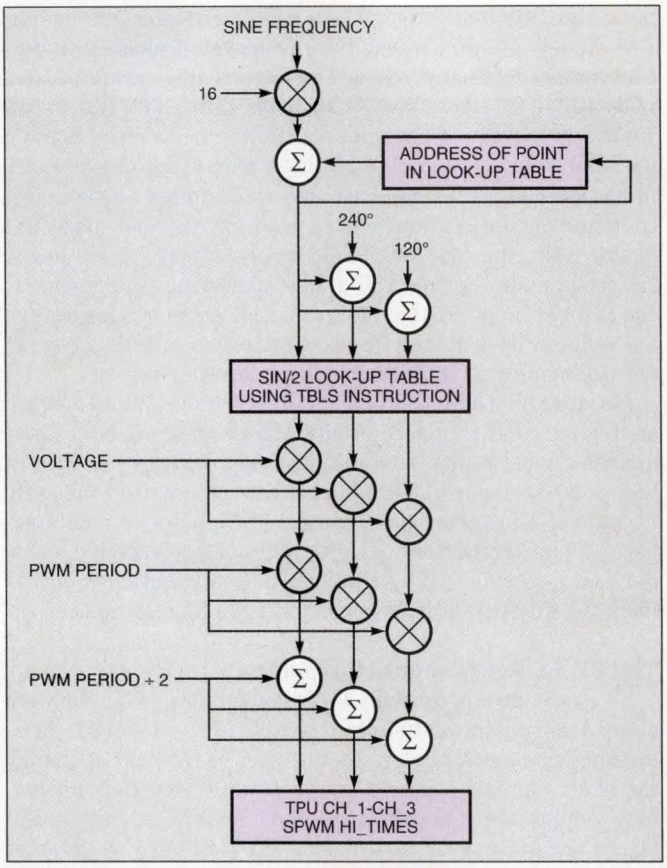

Fig 3—This diagram illustrates the algorithm the authors used to implement sinusoidal PWM in a system based on the 32-bit MC68332.

A μC can produce logic-level pulses; by varying the duty cycle of a square wave, a μC can implement pulse-width modulation. In a typical 8-bit μC such as Motorola's MC68HC11, interrupt-driven or polling schemes cause logic-level transitions on a given output pin that produce PWM waveforms having a specific pulse width and period. On the occurrence of a predetermined timer-match condition, the pin state makes the appropriate transition, and the CPU calculates the next low-high and high-low transition times. This waveform-generation method requires CPU overhead to create each of the desired signal's rising and falling edges. Because ac induction-motor control requires three PWM signals, this technique imposes a service time that severely limits the maximum PWM frequency a μC can produce. Such software latency is highly undesirable because it results in PWM frequencies within the audible range.

The 68332's modular 32-bit architecture includes intelligent on-chip peripheral subsystems. For motor-drive systems, this μC's critical features are the TPU, the TBL instruction, and the ability to operate at 16.78 MHz.

The TPU has 16 channels, TP0 through TP15, which operate independently of each other. Any channel can perform any of the TPU's time functions. The TPU also contains microcoded primitives for performing complex time-related functions, such as motor control and pulse-width modulation. Once the CPU writes the necessary parameters for a time-function algorithm to a TPU channel, the TPU runs

autonomously. It requires CPU intervention only to alter previously written parameters.

For the PWM example above, once you assign the desired high time, period, and reference addresses to a TPU channel's parameter block, the corresponding pin for that channel outputs the desired waveform. To perform PWM, you can have the TPU interrupt the CPU and have it calculate and write a new high time (that is, pulse width) to a particular parameter block. Most μCs require a CPU interrupt for each PWM-signal logic transition. In contrast, the TPU calculates all of the rising and falling transition times and affects the output pin accordingly without CPU intervention. It requires CPU overhead only to alter the current duty cycle (that is, to write new high times). Besides avoiding interrupt and polling latencies, the TPU offers greater speed because its primitives are implemented in microcode. In addition, the 68332's 16.78-MHz system clock provides 240-nsec timing resolution. This resolution is twice that of the HC11's general-purpose timer. A subsequent section discusses the effects of this timing resolution.

The TBL instruction works with signed (TBLS) or unsigned (TBLU) data. This instruction lets you use a data table of up to 257 points and get 65,536 values of the function represented by the data points. In other words, the instruction performs an 8-bit table look-up and an 8-bit interpolation between consecutive data entries.

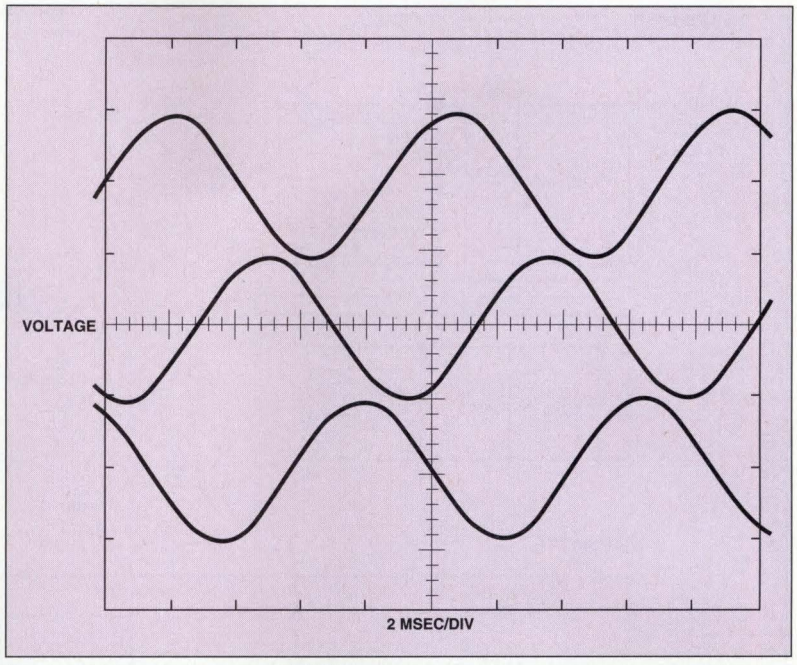

Fig 4—Although the actual PWM voltage waveforms scarcely resemble sine waves, the current that flows in the motor windings is nearly sinusoidal because the inductance and back EMF of the motor windings filter out the high-frequency components. If you simulate this effect by integrating or lowpass filtering the PWM signals, you obtain these near-perfect 3-phase sine waves.

TPU performs timing-related tasks

Five TPU channels implement this sine-wave-generation algorithm. A single channel producing a 50%-duty-cycle square wave with a period of 50 μsec (20 kHz) acts as a master timing channel. Each sample of the resultant sine waves has a finite duration before the next sample is produced. The master channel controls the sine-sample update rate and aligns the other TPU channels' signal timing. Another channel uses the input-transition counter (ITC) primitive. This channel counts the rising logic-level transitions at its input pin and, with the master timing channel, provides the means for updating the sine-wave samples at designated intervals.

Three TPU channels execute the SPWM primitive. This TPU protocol allows specified timing relationships among PWM channels. Among its benefits, synchronizing each PWM waveform to the master channel allows coherent updating of PWM parameters. Each TPU channel implements the overall sine-wave-generation motor-control algorithm.

Originally, we chose to have 21 samples represent a sine-wave cycle. Each sample of the sine function translates into a particular high time for the PWM waveforms. The following equations determine the pulse widths (high times) for each of the three PWM phases.

$$PWMA=((V\cdot\sin\Theta+1)/2)\cdot PER,$$
$$PWMB=((V\cdot\sin(\Theta+240°)+1)/2)\cdot PER,$$
$$PWMC=((V\cdot\sin(\Theta+120°)+1)/2)\cdot PER,$$

where: V is the voltage amplitude of the sine wave, Θ is the angle of the sine function, PER is the period of the PWM waveforms.

Expanding the expressions above shows that two terms are summed to provide the desired pulse widths. One term provides a constant 50% duty cycle (that is, PER/2); the other can vary at most from a –50 to a +50% duty cycle (restricted by voltage, V). The second term accounts for the desired phase relationship and provides amplitude modulation of the sine wave via voltage multiplication. This technique achieves duty cycles of 0 to 100%.

For a fixed number of 21 samples per sine-wave cycle,

$$\Theta=i(360°/21),$$

where i = 0,1,2,3,...20.

The μC stores the 21 values of the sine function as data in a look-up table (LUT). The rate of stepping through the LUT and of computing new pulse-width values determines the resulting sine-wave frequency. The algorithm sine-wave modulates the high times of the three PWM signals that drive the transistor bridges. The motor integrates the voltages to produce sine-wave currents.

We have modified this simple method to better drive the motor over the desired voltage and frequency range. The ability to vary the number of samples per sine cycle, to update all PWM parameters coherently, and to use a simple interface for speed control are some of the enhancements to the algorithm.

Because μCs operate in the digital domain, they must construct sine waves from discrete values. Thus, a μC produces a staircase approximation of a sinusoid. As a result, you must consider the effect of sample duration, or step size, on motor performance.

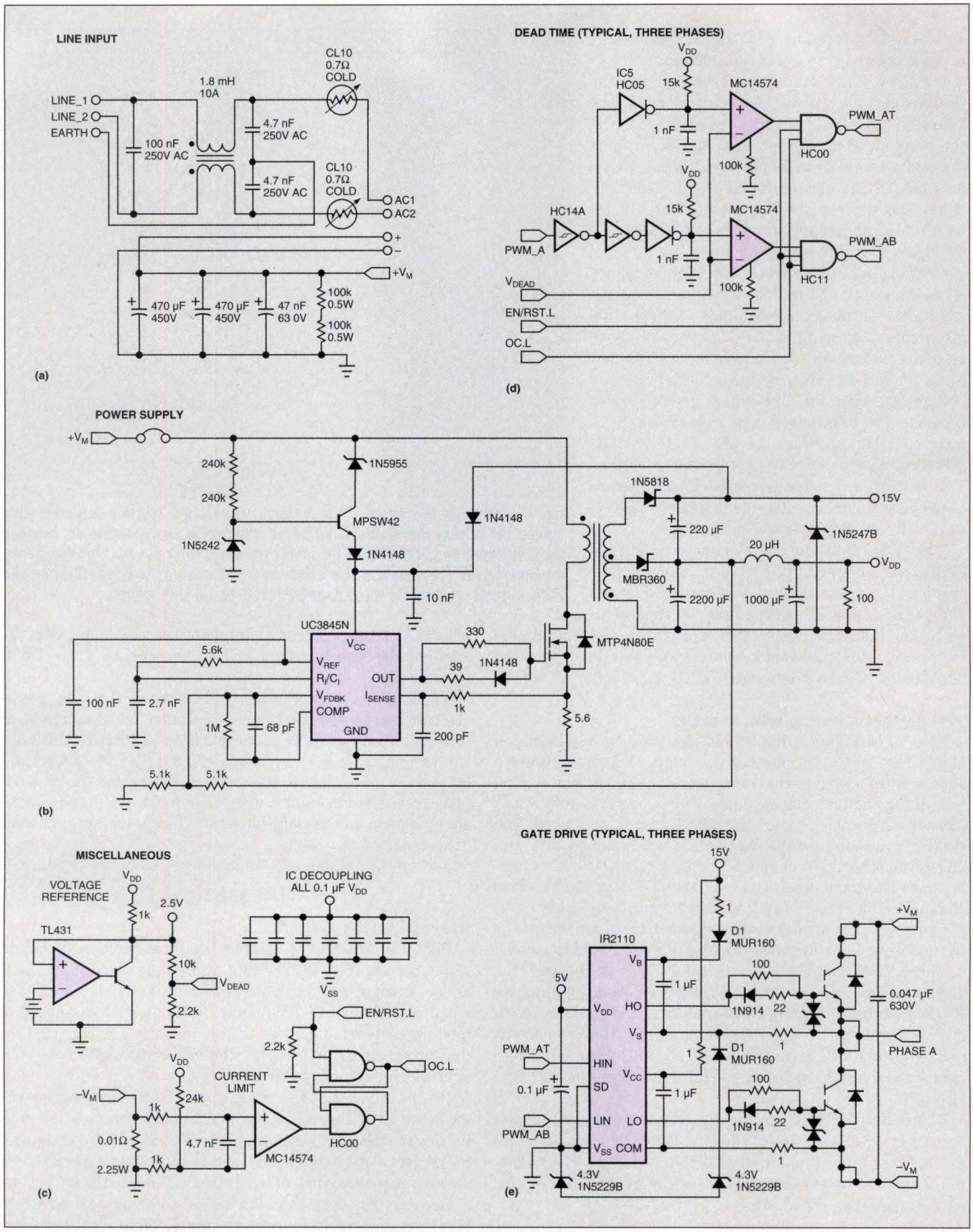

Fig 5—The motor drive has five major sections: the ac power-line interface (a), a power supply (b), miscellaneous circuits (c), a dead-time circuit for each phase (d), and a gate-drive circuit for each phase (e). This demonstration implementation is powered from the single-phase 60-Hz ac line. In a real EV, sections (a) and (b) would change somewhat to incorporate the large battery and the associated charger.

The simple algorithm uses a constant number of samples (21) per sine cycle and varies the duration of each step to create sine waves of different frequencies. To produce the lowest frequency, the μC had to produce 21 steps per cycle, each approximately 48 msec wide. Producing the highest frequency requires 400-μsec-wide steps. One rule of thumb requires that the step size be less than or equal to half of the motor's stator time constant. As estimated from the inductance of the motor, the stator time constant is 500 μsec. Therefore, the step size should not exceed 250 μsec. Even for the best-case example above (400 μsec for a sine frequency of 120 Hz), the 21-sample method does not result in efficient motor control.

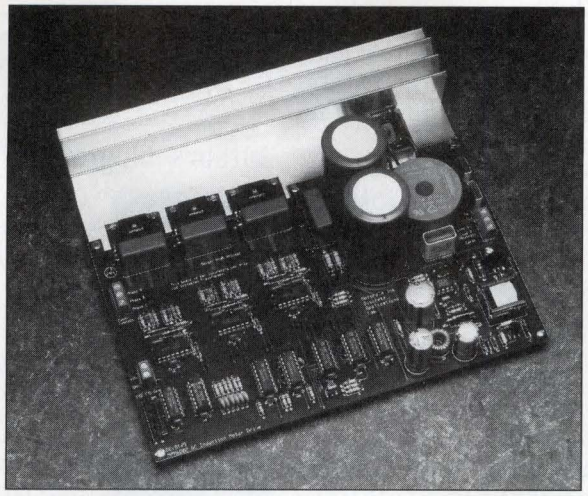

Fig 6—Much of the circuitry of the demonstration 3-phase, variable-voltage, variable-frequency PWM inverter fits on this medium-sized pc board.

To produce the frequencies of interest using a constant number of samples and an acceptable step size, you would need a data table of at least 4000 values. Not only does this approach demand an undesirable LUT length, it may not work for producing a frequency of 120 Hz, which would require 4000 2-μsec steps.

A more desirable approach to sine-wave frequency control is to use a constant step duration of 250 μsec or less and to vary the number of samples that represent the sine wave. You can implement a frequency-dependent number of sine samples by using a different-length LUT for each sine frequency. For frequencies at 1-Hz increments (over the range of 1 to 120 Hz), you would need 120 LUTs with lengths ranging from 33 to 4000 values. Obviously, this would waste memory and require tedious data entry. An alternative is to use a single LUT of reasonable length (257 values or less) with the 332's TBLS instruction.

The argument of the TBLS instruction is a word-size operand in which the upper byte is a pointer to an entry in the LUT and the lower byte determines how far to interpolate between pairs of entries. By clever manipulation of the TBLS operand, you can create virtual LUTs of varying size from a single fixed-length data table.

Now, let's make (sine) waves

The code developed for this task consists of a main program that initializes some parameters, branches to two subroutines that configure the TPU and queued-serial-module (QSM) subsystems of the 332, and loads the interrupt vectors for the ITC and serial-communications interface (SCI) interrupt-service routines (ISRs). This sine-wave-generation scheme is interrupt driven. As mentioned, the master timing channel outputs a 20-kHz square wave. This channel serves as the input to another TPU channel, initialized as an input-transition counter that generates a CPU interrupt after every fifth timing-channel rising edge.

Because the timing channel has a 50-μsec period, ITC interrupts occur at 250-μsec intervals (½ the stator time constant). Each time the interrupt is serviced, the CPU writes a new high time to the three SPWM outputs. By making the CPU-provided high times be values of a sine function, you can produce a sine-modulated PWM signal. Thus, the ITC ISR and the sine-function LUT are the heart of this algorithm. Producing three such PWM waveforms, each shifted by 120° relative to the others, produces 3-phase power.

On entering the ISR, the CPU writes the three phase-high times calculated during the previous ITC interrupt service to the appropriate TPU PWM channels. The ISR's calculations implement the equations in the initial-algorithm section above. The flow chart in **Fig 3** illustrates the duty-cycle computations that produce sine-modulated PWM waveforms. The entries in the LUT are 256 scaled values of the sine function. The numbers are scaled by 1024 so that all operations can use integer arithmetic. The actual table values have been halved to satisfy the pulse-width equations while avoiding an extra division operation in the ISR. You can download a complete source-code listing from either the *EDN* or Motorola bulletin-board system.

Fig 4 shows a set of 3-phase sine waves generated for a desired speed of 3600 rpm. These signals are indeed at full voltage and 120 Hz, as the speed characteristic of **Fig 1** predicts. You can observe high-quality sine-wave voltages through direct integration (that is, lowpass filtering) of the SPWM outputs. A simple user interface demonstrates speed control. A user varies the voltage and frequency of the sine waves by specifying "f" for faster or "s" for slower. The protocol displays the demonstration motor's correct speed (in revolutions per minute) on the screen. The sine-wave frequency changes occur smoothly, without abrupt voltage changes.

Hardware provides ac-motor control. First, a single phase was tested with the μC and an inductive load. A complete 3-phase inverter was then built for demonstration purposes (**Fig 5**). Most of it resides on one pc board (**Fig 6**). The single-phase 60-Hz ac line powers this version. In a real EV, the inverter would, of course, include a large battery and a charger.

Although the circuit accurately generates high-resolution 3-phase sine waves, it has several limitations. The TPU microcode service time imposes a constraint on the minimum and maximum pulse widths the SPWM primitive can produce. Approximately 1900 and 1300 nsec were the minimum high and low times, respectively. This limits the maximum duty cycle to approximately 94%. To prevent the possibility of inaccurate high times, which could occur as a result of TPU latency, each SPWM TPU channel is offset from the previous channel by 2.4 μsec.

The PWM frequency determines the voltage resolution of the sine waves. For a 20-kHz PWM frequency, the period is 50 μsec, or 210 counts of the TPU time base (240 nsec/count). Because the PWM duty cycle corresponds to sine-wave voltage amplitude, the voltage resolution is limited to 210 levels. Thus, the voltage resolution is approximately 0.5% of the full-

CONTROLLING AC-MOTOR SPEED

scale voltage. Higher resolution would provide better low-level sine waves at very low motor speeds. However, to take advantage of the higher resolution, the bandwidth of the entire inverter must be higher than 4 MHz.

You can use custom microcode to implement future improvements to the sine-wave algorithm. Using two adjacent channels per phase allows updating the rising edge before the occurrence of the falling edge and vice versa. This will permit minimum high and low times of 240 nsec (one timer count). You can also use microcode to center the pulses with respect to each other. This would allow further reduction of the high-frequency ripple current, an important consideration with low-inductance motors. You can implement coherent updating of all TPU variables in microcode, as well.

With the simple user interface and open-loop control you can quickly get a system up and running. A large motor for an EV requires a current loop to protect the power devices and the motor from destructive currents. To provide smooth response, you should use a position encoder and control loop. Vector control would optimize the flux vectors inside the motor, resulting in the highest possible efficiency. EDN

Acknowledgment

We would like to thank Dr Allan Plunkett, AC Drives Technology, for his contributions to the final algorithm. His inputs were essential for a thorough understanding of the details involved in sine-wave PWM generation. We wish to extend out gratitude to Peter Pinewski, Motorola Semiconductor Products Sector, for his assistance throughout the development of the MC68332 code.

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Jeff Baum holds a BSEE from the University of Illinois, Urbana, and an MSEE from the University of Arizona, Tucson. He is a systems engineer with Motorola's semiconductor product sector in Phoenix, AZ, where he has worked for more than five years. He has helped to develop solid-state power modules, embedded microcontrollers, and solid-state sensors. His hobbies include hiking and mountain biking.

Ken Berringer, who holds a BSEE from the University of Florida, Gainseville, has also worked for Motorola's semiconductor product sector in Phoenix for more than five years. His title is Senior System Engineer. Berringer's duties involve the design of motor-control circuits and intelligent power modules. His leisure activities include playing the guitar, running, and swimming.

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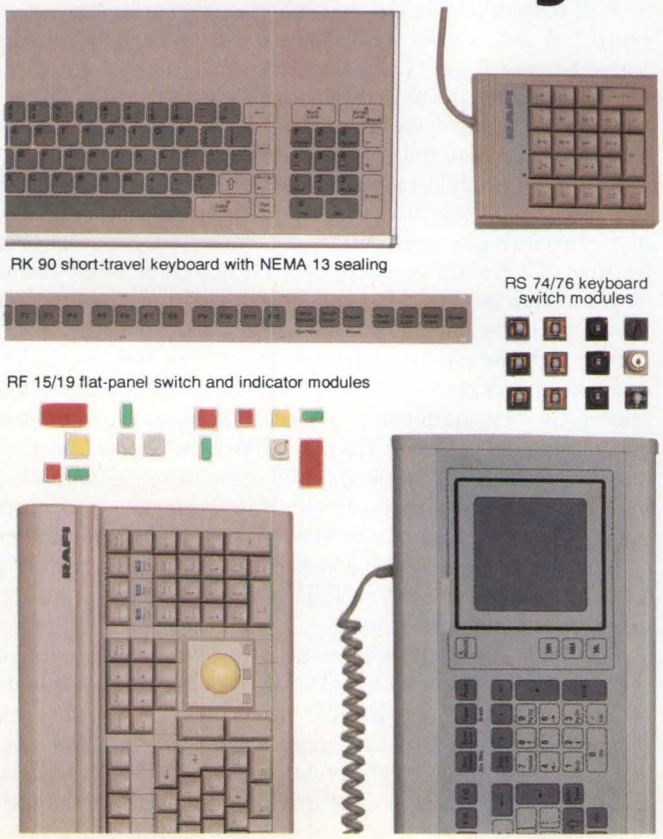

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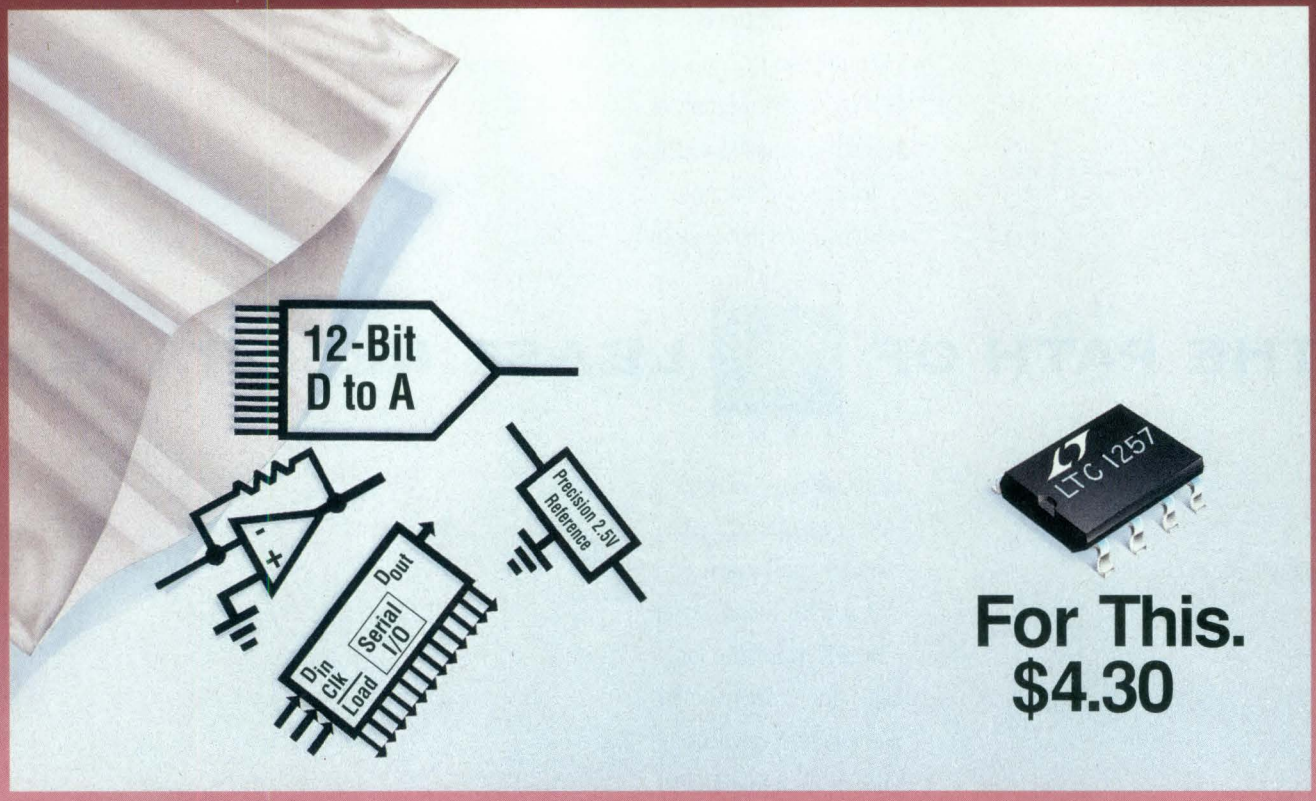

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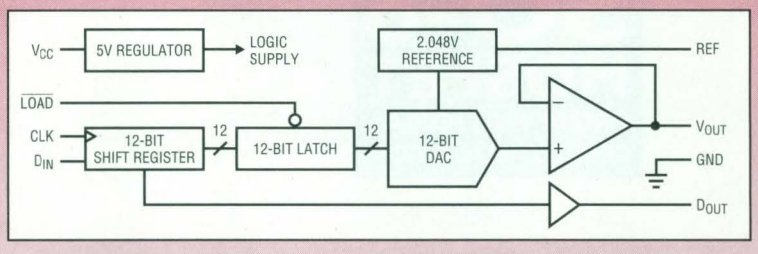

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CIRCLE NO. 66

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PLDs implement delay lines

Trevor J Preston, Astromed, Cambridge, England

PLDs such as the Altera MAX5000 family can easily generate asynchronous delays and pulses with an edge-to-edge timing resolution of 8 nsec. Newer families can go even faster. The development-system simulator allows you to quickly and accurately design and predict the timing of the required delay patterns. However, you must be careful when chaining logic together to generate longer delays because the logic synthesizer can sometimes synthesize out gates and produce delays much shorter than you expect. **Fig 1**'s schematic for an EPM5016 device illustrates the principles of generating a range of delays; **Fig 2** shows the simulator's output.

The delay equals the sum of the following: input-pad-and-buffer delay, the output-pad-and-buffer delay, and the logic-array delay. (Even when no logic is used, the signal must pass through the logic array.) For large MAX devices, there may also be a programmable-interconnect delay. Depending on the speed of the device, this minimum delay can range from 15 to 20 nsec. The shortest delay possible occurs when an input pin connects directly to an output pin, as in DELAY_0. DELAY_1 includes a single inverter in its path. Although DELAY_2 chains two inverters in the attempt to lengthen the delay time, the resultant signal in **Fig 2** has no additional delay. The logic synthesizer has cleverly synthesized out the redundant logic to produce a signal identical to DELAY_0 and DELAY_1, and the delay remains unchanged.

To produce additional delay, you have to force the synthesizer to use an additional logic block by including two macrocells (MCELLs), the result of which is signal DELAY_3. The Maxplus compiler never synthesizes a macrocell out of the circuit. Even so, the synthesizer is clever enough to synthesize out the two inverters in DELAY_4's path if it detects redundant logic embracing a macrocell. DELAY_5 shows the delay of three logic blocks plus the I/O delay, DELAY_6 shows the delay produced by a positive edge-triggered monostable, and DELAY_7 results from a positive and negative edge-triggered monostable. **EDN BBS /DI_SIG #1387** EDN

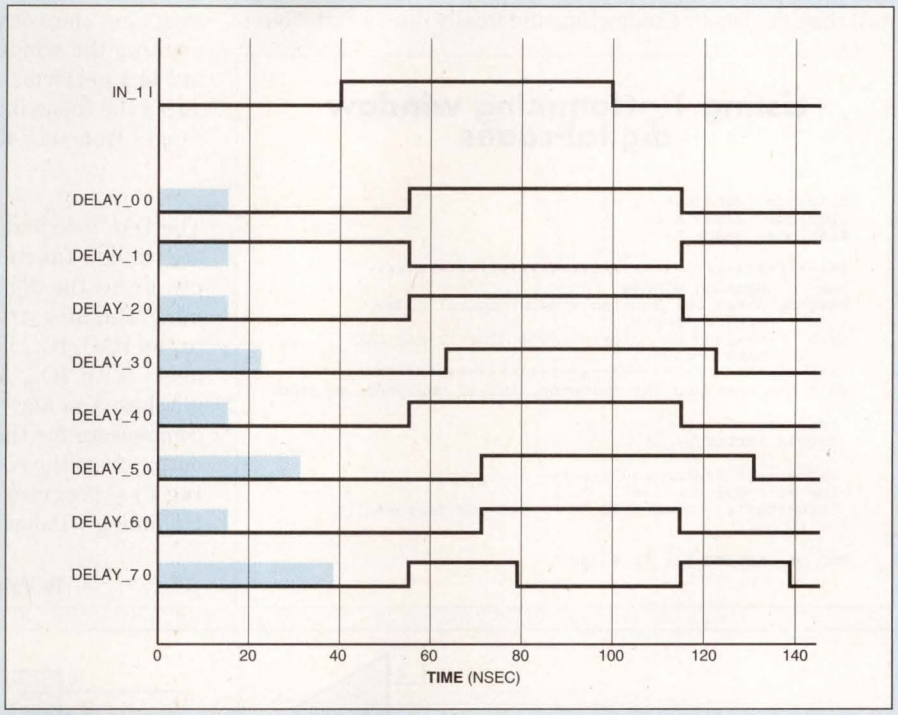

Fig 2—Chaining no (DELAY_0), one (DELAY_1), and two inverters (DELAY_2) together produces the same delay because the synthesizer automatically reduces redundant logic. Using macrocells instead of inverters produces longer delay times.

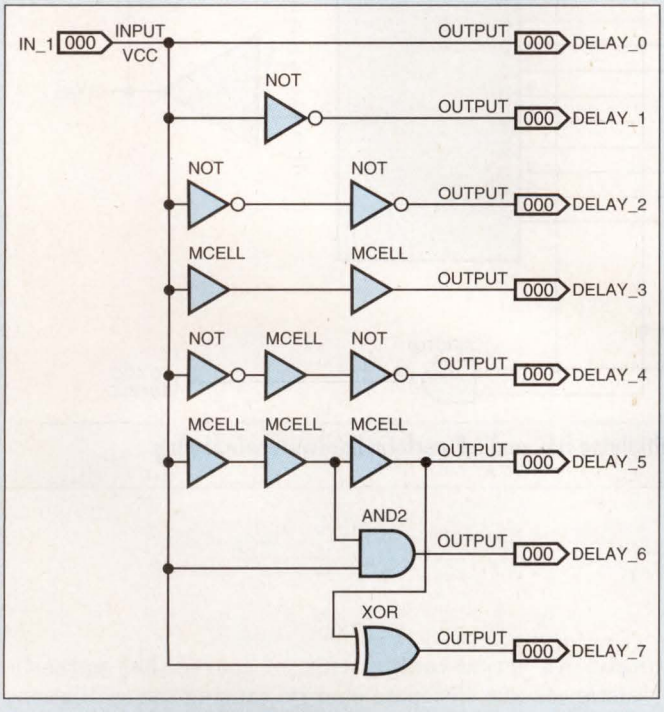

Fig 1—Chaining together PLD blocks produces varying delays, but you must take steps to outsmart the development-system simulator, which automatically removes redundant logic.

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DAC and μP implement hardware window generator

Sergey Velichko, Extended Systems, Boise, ID

A typical DSP system first converts an analog signal to digital, then performs windowing, and finally does a fast-Fourier transform. However, you can accelerate this process by swapping the converting and windowing steps and implementing the windowing in hardware. The multiplying DAC in **Fig 1** performs the windowing of an input signal and produces the following output signal, where the digital code N ranges from 0 to 4095:

$$V_{OUT}=-V_{IN}(N/4096.$$

The DAC7545 and 80C51 can easily implement an appropriate window function that ranges from 0 to 1. The 80C51 simply stores the digital codes for the window function (Hamming, Hanning, triangle, for example) and writes these codes to the DAC. IC_{1A} is simply a front-end buffer. The DAC connects with IC_{1B} for unipolar operation, and C_1 prevents glitches. You may want to add an inverter in the system to compensate for the fact that this circuit inverts V_{IN}. A low output from the NAND gate enables the system's ADC. **Listing 1**'s C program produces digital codes that implement the Hamming window. **EDN BBS /DI_SIG #1386** EDN

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Listing 1—Hamming window digital-codes

```
#include  <stdio.h>
#include  <stdlib.h>
#include  <math.h>

/*********************************************
ham     -Hamming window
hamming-array for Hamming window digital codes,
n       -window length
maxN    -maximum DAC digital code (for 12-bit DAC
         maxN = 4095).
*********************************************/
void ham(unsigned int *hamming, int n, unsigned int maxN)
{
 int   i;
 double factor;

 factor = 8.0*atan(1.0)/(n-1);
 for (i = 0;i < n;i++)
  hamming[i] = maxN * (0.54 - 0.46*cos(factor*i));
}

END OF LISTING for DI #1386
```

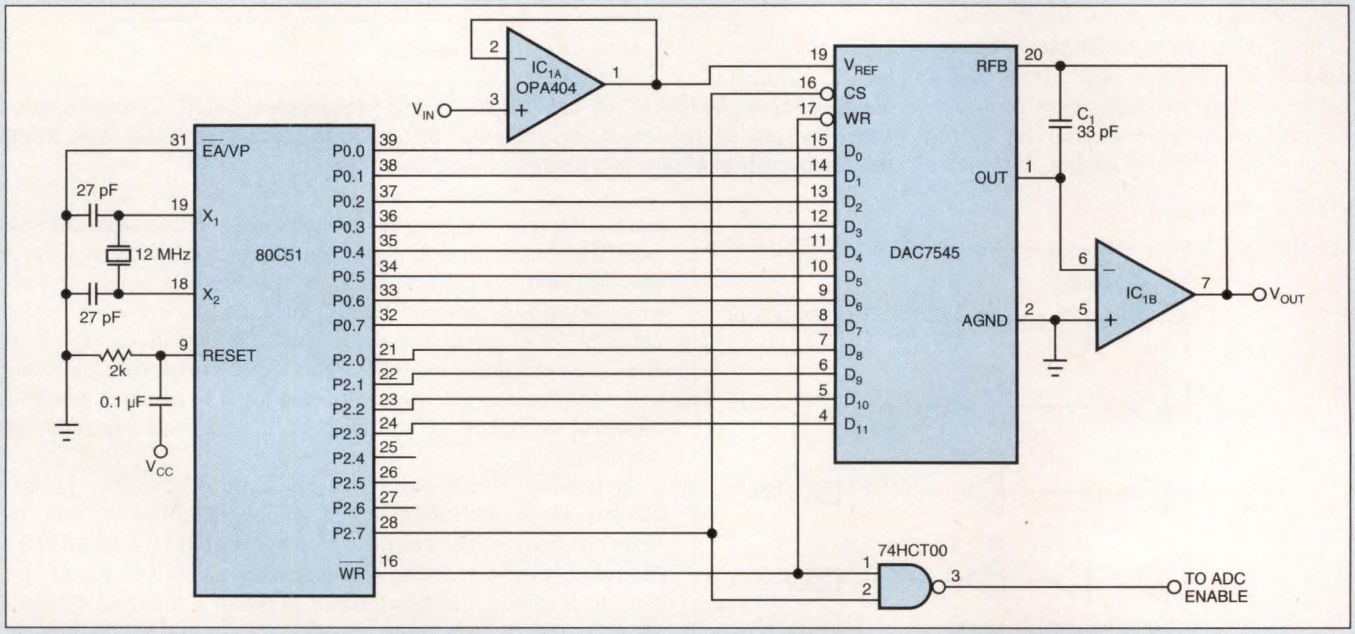

Fig 1—Instead of performing windowing in software, this circuit's multiplying DAC and μP perform hardware windowing.

LC oscillator has 1% THD

Gary Sellani, Maxim Integrated Products, Sunnyvale, CA

At the heart of many oscillators is a parallel-resonant LC tank circuit whose impedance is infinite at the resonant frequency of $1/2\pi\sqrt{LC}$ Hz. Infinite impedance implies an absence of parallel damping resistance, so once an ideal tank circuit starts oscillating, it should continue indefinitely. An actual tank circuit, of course, has parasitic resistances that dissipate energy, causing the oscillations to die out. You can counteract this effect by adding a "negative" resistance, which cancels the net parallel parasitic resistance. **Fig 1a**'s circuit uses a wideband transcon-

ductance amplifier to synthesize negative resistance easily.

This circuit connects the positive input of the amplifier, a MAX436, to its output and its negative input to ground. With this configuration, applying a positive voltage to the output causes current to flow *out of* the amplifier in proportion to the applied voltage. The circuit acts like a resistor whose current flows in the opposite direction; hence, the negative value. Note the equivalent circuit in **Fig 1b**.

The source impedance of the amplifier's current-source output, a minimum of 2.5 kΩ, is compatible with load resistances that range from 50 to 300Ω. The load resistance in this circuit, R_2, is 47Ω and should be much smaller than the tank-circuit parasitics, yet larger in absolute value than the amplifier's negative resistance. R_1 sets the negative resistance in terms of the amplifiers' transconductance, $g_m=8/R_1$, where factor 8 is inherent in the amplifier.

The negative resistance value is, therefore, equal to the value of $R_1/8$, which must be less than R_2. Choosing 47Ω for R_2 yields $R_1<8\times R_2=376\Omega$. A reasonable value for R_1, therefore, is 301Ω. As intended, the parallel combination of negative resistance, which is $-R_1/8$ or –37.6Ω, and a positive R_2 of 47Ω yields a negative resistance of –189Ω that shifts the oscillator's complex-conjugate pole pair to the right half plane.

By itself, the combination of tank circuit and regenerative element—the negative resistance—simply drives the output amplitude to saturation. To achieve steady oscillation, the circuit needs an amplitude limiter. R_3 serves that purpose and appears, in parallel with R_2, only when the amplitude is sufficient to turn on D_1 or D_2.

Then, excluding the diode resistance, the net parallel resistance is a positive value of 63Ω—two parallel 47Ω resistors in parallel with –37.6—that damps oscillation by shifting the pole pair to the left half plane. Thus, the circuit achieves amplitude stability by allowing the pole pair to toggle between positions slightly to either side of the jω axis.

The oscillator, whose tank circuit consists of a mica capacitor and an air-core inductor, has an output frequency of 9.3 MHz. You can trim the output frequency to any reasonable value, but above 10 MHz, the layout should include short connections and a ground plane. The output power spectrum for **Fig 1** indicates that the major source of THD is a third harmonic below –40 dB, which is less than 1%. After you apply power, the oscillator requires approximately 350 µsec to reach its final amplitude. **EDN BBS /DI_SIG #1392** EDN

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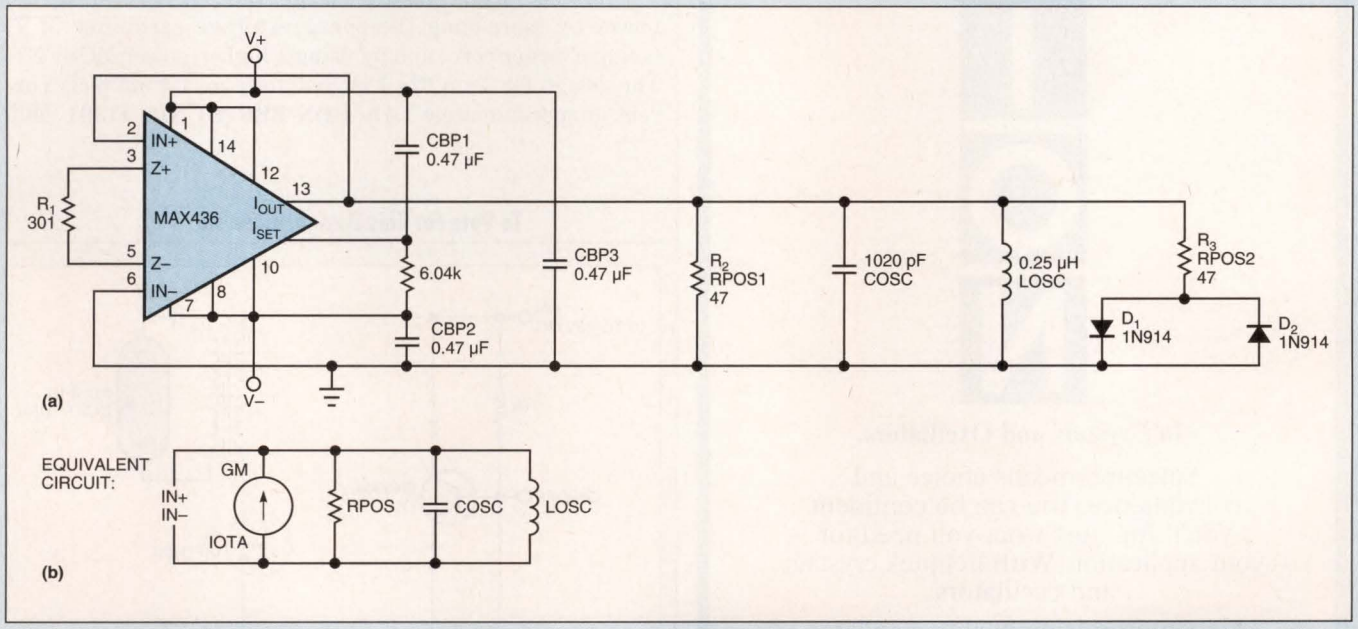

Fig 1—This parallel-resonant LC tank circuit uses a wideband transconductance amplifier to create a negative resistance to cancel the tank's parasitic resistances.

Low-cost converter drives fluorescent tubes

Steven C Hageman, Calex Manufacturing Co, Concord, CA

In the last few months, several designers have published circuits for cold-cathode fluorescent-tube (CCFT) power supplies, and a specialized power-supply IC is also now available. However, a significant number of CCFT applications don't require the complexity and expense of a dual-FET resonant approach. Applications such as electronic night-lights, backlights for industrial equipment, such as gas pumps or signs, simply can't justify the cost of building a resonant supply. The low-cost circuit in **Fig 1** produces a small, very reliable drive for many of the smaller CCFT tubes.

Initially, Q_1's emitter drives the gate of MOSFET Q_2 high, turning Q_2 on. Current then ramps up through T_1, which acts more like an inductor than a transformer. When the current through T_1 and Q_2 reaches approximately $0.62/R_SA$ (approximately 1A for this design), Q_3 turns on. The Q_3's collector pulls the Q_1's base and Q_4's gate toward ground and causes programmable unijunction (PUT) Q_4 to fire. When Q_4 fires, it acts like an SCR and quickly drives the gate of Q_2 to ground.

At this point, the energy stored in T_1's primary winding transfers to the secondary and causes the tube to ignite. Q_4 stays latched until T_1 releases all of its energy to the tube. The current in T_1 then reverses in a slightly resonant ring and flows back through Q_2's body diode, causing Q_2's gate to go slightly negative. Because of Q_2's stray capacitance, the anode of Q_4 then also goes negative, causing it to unlatch and release the gate of Q_2 for another cycle.

With the component values in **Fig 1**, the converter oscillates at a frequency of approximately 30 kHz. The circuit runs with inputs from 10 to 20V dc and draws 170 mA at 15V. The value of R_1 controls the brightness of the CCFT. Substituting a smaller value than 0.62Ω increases the energy in T_1 and causes the tube to glow more brightly. Additionally, pulling the ON/OFF pin to ground turns off the circuit.

This basic circuit can drive larger tubes if you scale up the power by increasing the energy-storage capability of T_1 (using a larger core) and by using a higher-power MOSFET. The design for T_1 in **Fig 1** is good for a maximum peak current of approximately 1.4A. **EDN BBS /DI_SIG #1391** EDN

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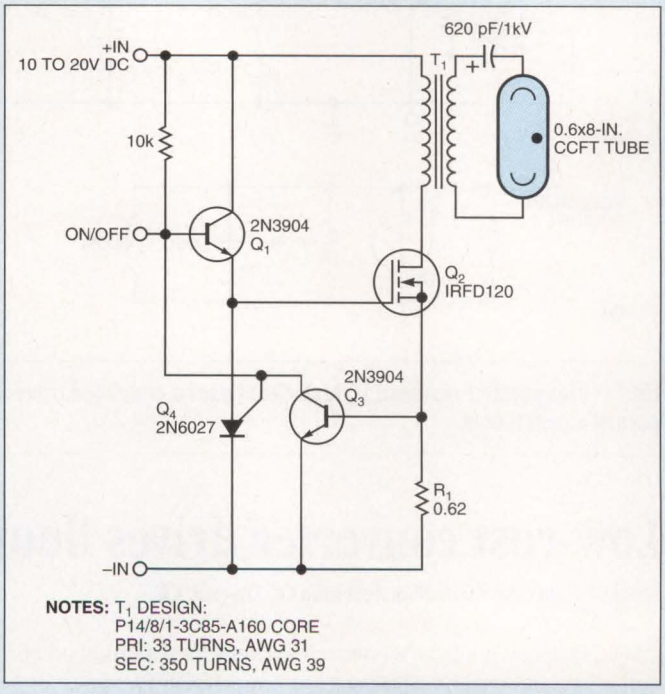

Fig 1—This low-cost cold-cathode fluorescent-tube power converter produces a small, very reliable drive for many of the smaller tubes.

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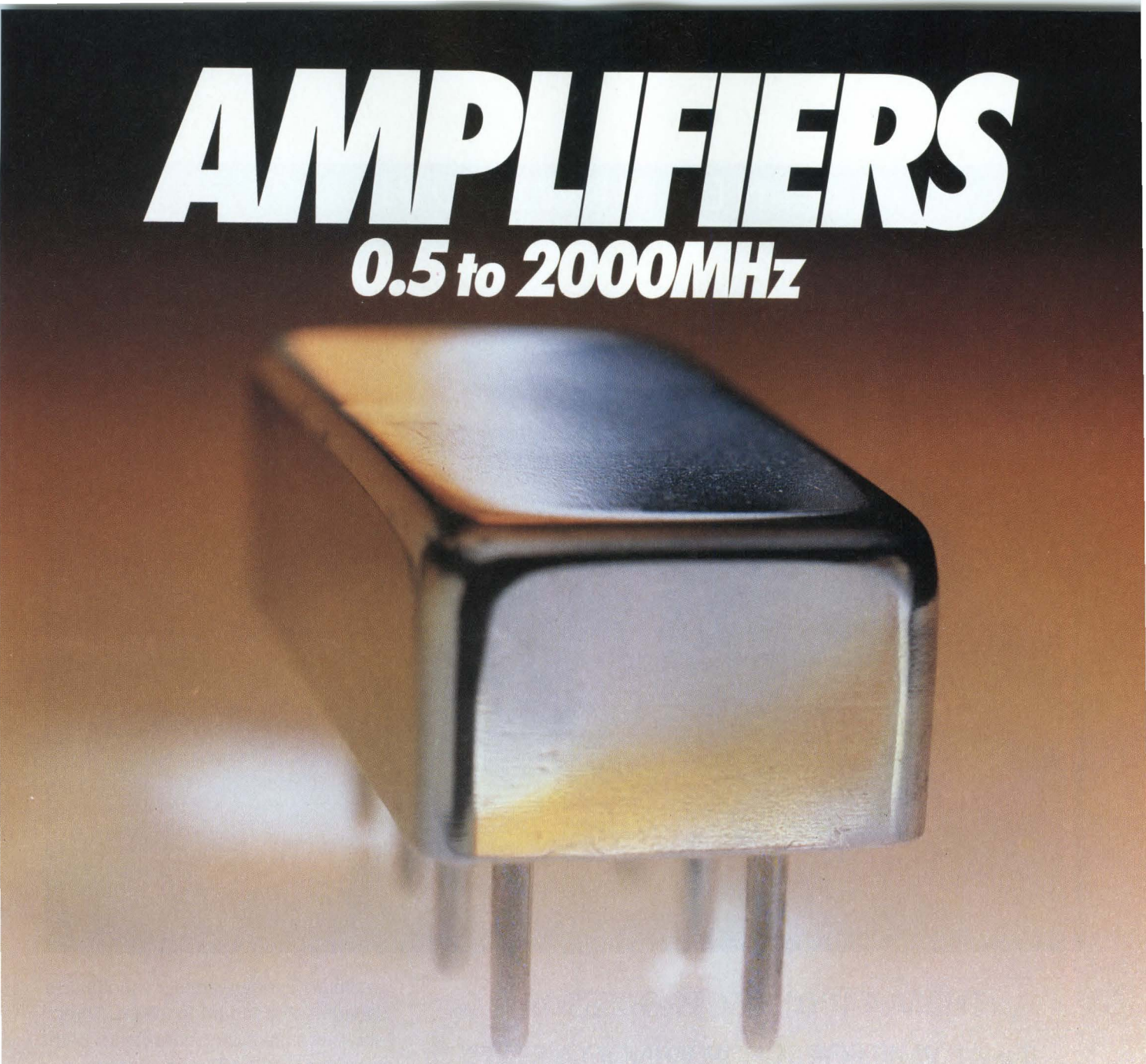

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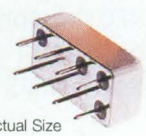
Model	Freq. Range f_L to f_U (MHz)	Gain min. (dB)	Gain flatness* (+/-dB)	Max. Output PWR** (dBm)	NF typ. (dB)	Isol. typ. (dB)	DC PWR (V/mA)	Price $ ea. (10-24)
MAN-1	0.5-500	28	1.4	8.0	4.5	41	12/60	13.95
MAN-2	0.5-1000	18	1.5	7.0	6.0	37	12/85	15.95
MAN-1LN	0.5-500	28	1.4	8.0	2.8	42	12/60	15.95
^MAN-1HLN	10-500	10	0.8	15.0	3.7	16	12/70	15.95
MAN-1AD	5-500	16	1.0	6.0	7.2	50	12/85	24.95
MAN-2AD	2-1000	9	0.7	-2.0	6.5	33	15/22	22.50
MAN-11AD	2-2000	8	1.5	-3.5	6.5	27	15/22	29.95

* Midband $10f_L$ to $f_U/2$, +/- 0.5 dB ** At 1dB compression point ^ Case height 0.3 inch

CIRCLE NO. 69



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For detailed specs on all Mini-Circuits products refer to • THOMAS REGISTER Vol. 23 • MICROWAVES PRODUCTS DIRECTORY • EEM • MINI-CIRCUITS' 740- pg. HANDBOOK.

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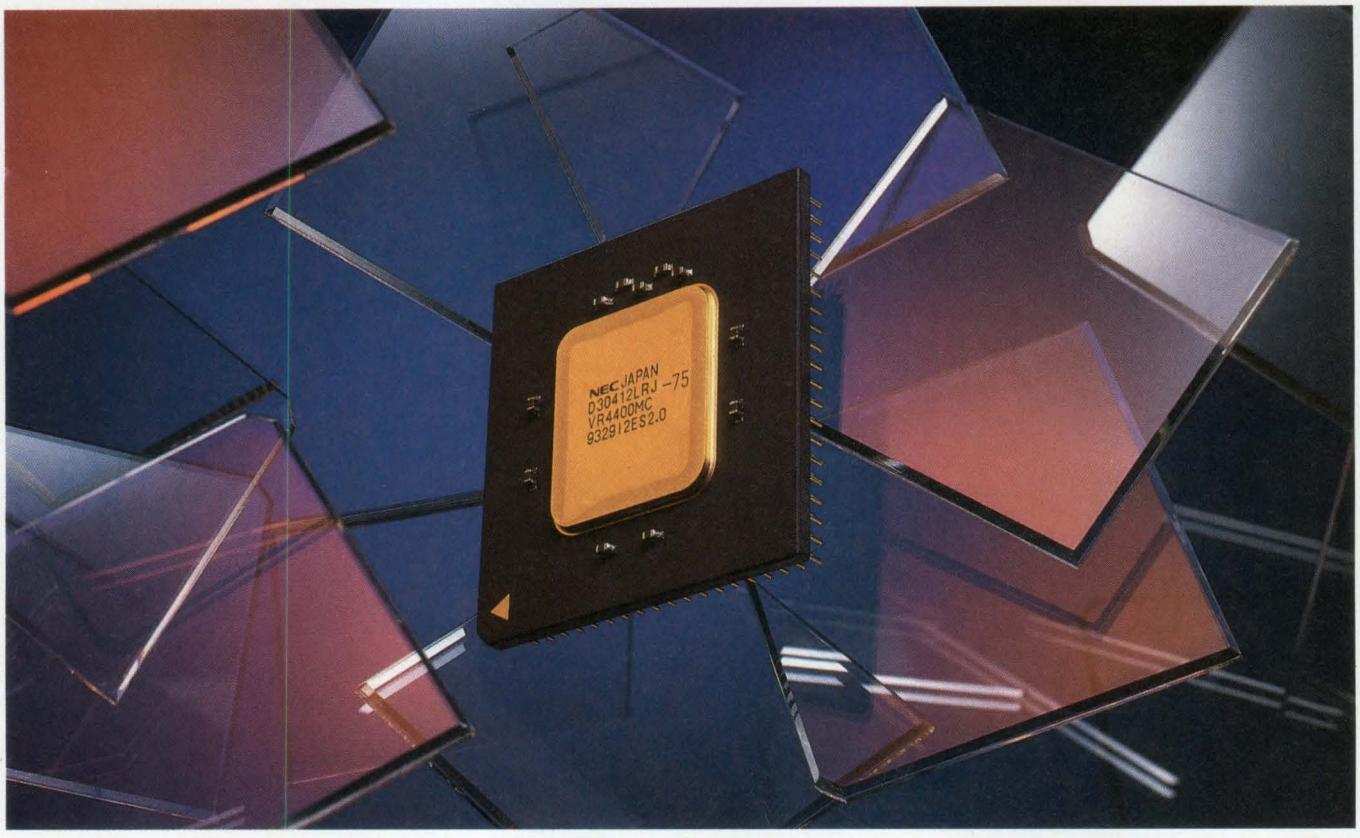


THE VR4400™ RISC PROCESSOR: IDEAL PLATFORM FOR WINDOWS NT.™

The Windows NT operating system has extraordinary potential. It offers the power, reliability and openness to launch a new era in business and high-end personal computing.

But this potential can only be realized if microprocessors provide the superior performance which Windows NT demands.

NEC's response to the challenge is the VR4400 – a 64-bit processor based on MIPS® RISC architecture. Running at 150MHz internally, it delivers 94 SPECint92 and 105 SPECfp92. Third-party benchmarks indicate that the VR4400 runs Windows NT nearly twice as fast as Pentium.™

The VR4400 comes in two versions. The standard VR4400PC features an on-chip floating point unit and separate 16K-byte instruction and data cache. The high-end VR4400MC supports a secondary cache of up to 4M bytes and a multiprocessing system, in addition to offering all standard functions. Three internal speeds are available for both versions – 100, 133 and 150MHz.

NEC's 64-bit RISC processor is already driving the world's most powerful workstation. While providing excellent price/performance, the VR4400 allows users to run existing DOS and Windows 3.1 applications software under the new NT operating system.

In addition to microprocessors, NEC also offers chip sets, advanced DRAMs and TFT color LCD screens to support the next generation of personal computing.

All trademarks are property of their respective holders.

Updates on the scope and depth of NEC technologies

Number 152

VR4200™ RUNS WINDOWS NT FOR NOTEBOOK PCs.

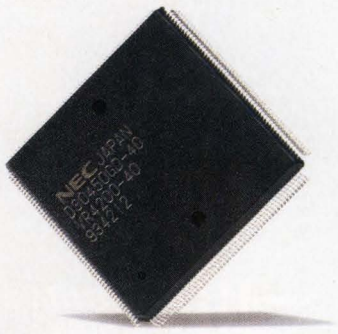
NEC has the industry's broadest line of 32- and 64-bit RISC microprocessors. Our latest offering is the 64-bit VR4200, which delivers VR4000 performance at 1/5th the cost.

With performance of 55 SPECint92 and 30 SPECfp92, the VR4200 is powerful enough to build desktop capabilities into notebook computers running Windows NT.

The 80MHz VR4200 also offers a cost-effective RISC solution for designers of low-end workstations, X-terminals and diverse embedded applications.

The VR4200 incorporates 16K-byte instruction cache and 8K-byte data cache. Implemented with a 0.6-micron CMOS process, it runs on 3.3V and consumes only 1.5W. The VR4200 is available in a low-cost 208-pin plastic QFP or 179-pin ceramic PGA.

The VR4200 was developed jointly with MIPS Technologies, Inc.

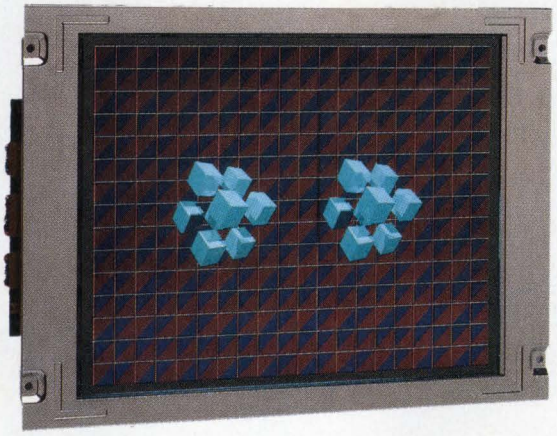


TFT ACTIVE-MATRIX COLOR LCDs.

Liquid crystal displays (LCDs) are becoming more brilliant, colorful and versatile. NEC believes the greatest advances will be made in thin-film-transistor (TFT), active-matrix color LCDs. We're committed to TFT LCDs because they give users clear advantages in display quality and performance.

For notebook PCs, we're mass-producing a 24cm (9.4-inch) display which offers an optimum balance between brightness, power consumption, size and weight. It displays 4,096 colors with 640 x 480 pixels, consumes 8W, measures 12.5mm deep and weighs 680g. 24cm displays were pioneered by NEC and have now become the de facto standard for notebook PCs.

For handheld terminals and measuring equipment, we offer a high-resolution 17cm (6.5-inch) display. It features 640 x 480 pixels arrayed at a 0.207mm pitch on a display area about half the size of 24cm model. The 17cm screen displays 4,096 colors, consumes 5W and weighs 360g. It has already been designed into high-end measuring equipment such as FFT analyzers.



16M SYNCHRONOUS DRAMs.

Microprocessor speeds are soaring while DRAM access speeds are not. To break the bottleneck, NEC is introducing a new species of ultra-fast DRAMs.

Operating at 100MHz external clock, our 16M Synchronous DRAMs eliminate CPU wait states. PC designers gain a quantum leap in system speed and workstation designers save by eliminating costly cache SRAMs.

The new DRAMs provide a minimum cycle time of 10ns (100MHz). The maximum data transfer rate for a x16 device is 200M bytes/sec with a 3.3V power supply. Our Synchronous DRAMs are designed with 3-stage pipeline architecture and fully meet JEDEC standards.

We offer a wide choice of 16M Synchronous DRAMs. Clock-speed versions are 66, 75, 83 and 100MHz. Bit organizations are x4, x8 and x16.

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CIRCLE NO. 70

Tools tame device with four DSPs and RISC μP

Many potential DSP applications require more power than has previously been available on a single chip. By stuffing 4 million transistors on a chunk of silicon, Texas Instruments has significantly increased the chip's computing power. The MVP (Multimedia Video Processor, or TMS320C80) includes four 32-bit DSPs along with a RISC μP that has a floating-point unit, a transfer controller, a video controller, and some common memory.

A set of DSP development tools helps you control the chip. The MVP tools include simulators, a debugger, a C compiler, an executive, a library of DSP and multiprocessing primitives, and an algebraic assembler.

The debugger allows you to debug the multiprocessor chip in a high-level language and runs in a Windows-based environment. A debug manager controls multiple debuggers to coordinate the multiple processors. On-chip emulation, which is accessed through a JTAG port, takes 9% of the MVP's silicon.

A device simulator provides a view of the five on-chip processors; you can independently view and manipulate each processor. A system-level simulator lets you verify system performance and compatibility with system devices.

The MVP device executive serves as a task scheduler. It works in conjunction with the on-chip transfer controller and manages communication between the processors.

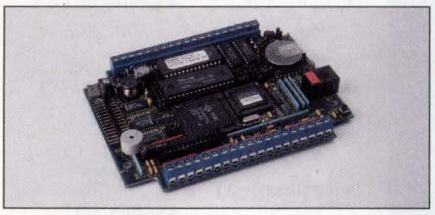
Separate C compilers for the RISC μP and the DSPs work with a common linker to create a single executable. The algebraic assembler accepts algebraic equations and creates assembly code. An expanding DSP-primitive software library comes with the $30,000 tool kit.

Texas Instruments, Denver, CO. (800) 477-8924, ext. 4500. **Circle No. 396**

For more information on the chip itself, see pg 67.

Small SBC, small price

The Z-180-based Little Star single-board computer (SBC) costs $195; measures 4×5 in.; and includes 16 protected digital inputs, 14 digital outputs, up to 512 kbytes of EPROM and SRAM, and two serial ports. A PC-based integrated development system for programming the board in C costs $195. For $295 you can buy the Little Star inside an enclosure with a built-in 2×20-character LCD and a 12-key keypad. A switching power supply accepts 9 to 36V dc and can provide up to 750 mA at 5V dc for external use.



Z-World Engineering, Davis, CA. (916) 757-3737. **Circle No. 397**

EPROM emulator handles serial communication

The Em4 EPROM emulator lets you communicate with your target μP via the EPROM socket. It interfaces to a PC via a parallel printer port. The interface to the target is entirely through EPROM reads. The target μP reads locations in the EPROM space. The emulator decodes these reads and sends the appropriate data to the PC.

Using the two serial links, you can examine the internal registers of the target μP when used with a debugger. You download programs under development to the SRAM in the emulator via the parallel port. An external BNC input allows other test equipment to cause a breakpoint.. The Em4 emulates 24-, 28-, 32-, 40-, and 42-pin EPROMs in 8- and 16-bit modes with up to 16 Mbits of memory. £695 for 1-Mbit version; £1495 for 16-Mbit version.

Crash Barrier Ltd, Wellingborough, Northants, UK. (0)933-224366. **Circle No. 398**

Integrated tool kit includes real-time kernel

Precise Solution is a Windows-based integrated development environment for Motorola 680X0/3XX μPs. It includes a C compiler, a real-time executive, an RTOS-aware debugger, a simulator, and communications and ICE support for $10,000.

You can use the debugger (PassKey/MQX) via a serial or an Ethernet link between the host and the target or via background-debug mode. When using the background-debug-mode option on 683XX μPs, you don't consume any of the target resources. The PassKey/TASK debugger works with ICEs from Embedded Support Tools Inc (Canton, MA).

Intermetrics Microsystems Software Inc, Cambridge, MA. (800) 356-3594. **Circle No. 399**

VxWorks RTOS gets networking products

WindNet adds to VxWorks' existing networking capability, which includes TCP/IP, sockets, SLIP, UDP, telnet, rlogin, ftp, tftp, rsh, bootp, proxy arp, RPC, and NFS. The new WindNet SNMP (Simple-Network-Management Protocol) is based on technology from SNMP Research (SNMP is a network-management standard). WindNet is based on STREAMS, a standard framework for networking protocols. WindNet operates with any STREAMS-compliant protocol. For specific networking needs, a variety of protocol sets will be available. From $3000.

Wind River Systems Inc, Alameda, CA. (510)748-4100. **Circle No. 400**

Ada moves to fixed-point military DSP

Ada is available for fixed-point DSP applications; it works with the Texas Instruments SMJ320C50A, a military version of the C5X fixed-point DSP family.

Tartan also has Ada compilers for the C3X and C40, which allows you to use the same development package for fixed- and floating-point DSPs. You have to learn only one set of tools. Ada runtimes can be small, ranging from 500 bytes to 24 kbytes. $28,000.

Tartan, Monroeville, PA. (412) 856-3600. **Circle No. 401**

—David Shear

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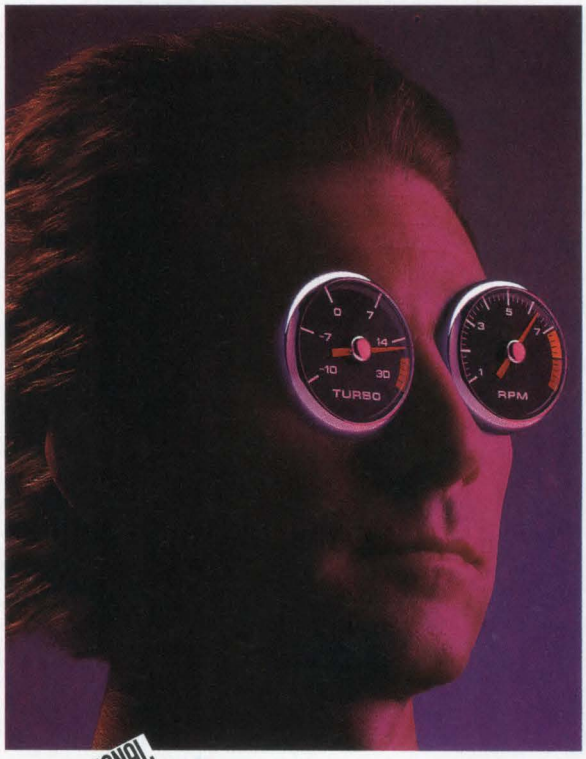

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HARRIS SEMICONDUCTOR

CIRCLE NO. 71

Motorola 68332 μP targets 600-dpi, 8-pg/minute printers

Only a few years ago, engineers prided themselves on their skills in designing 68000s into a wide range of applications. Memory-bus design of 68000s was considered an art. Those days are gone. These days, most designers want to minimize hand design by getting as complete a chip solution as possible. Fewer chips mean lower cost. Motorola's 68332 is a designer's dream; it minimizes design effort and delivers a low-end (8-pg/minute), moderate-resolution (600-dpi) printer. A custom variation of the 68000 powers the popular HP 4L LaserJet printer.

The 68332 integrates two processors on a chip—a 16/32-bit 68EC000 control CPU and a specialized RISC graphics processor (RGP). The 68000 serves as the printer controller, interfaces to the external world, and sets up the display list for RGP processing. A system-integration module minimizes 68332 design-in time. It provides a programmable interface for PROM, ROM, and I/O, and it supplies eight chip selects for decoding and a DTACK* strobe.

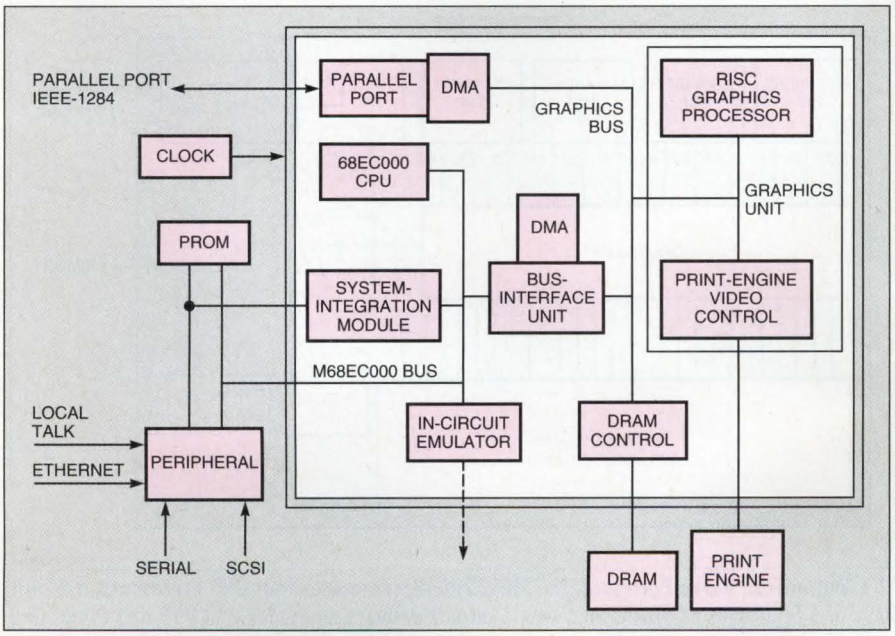
An on-chip DMA controller enables an external peripheral to move bursts of font data or to display lists to DRAM, bypassing the 68000's control CPU. The 68000's CPU executes from PROM on the 68EC000 bus. The RGP executes from DRAM and has its own controller. The RGP has a high processing throughput: Most RGP instructions involve multiple data accesses enabling data throughput to approach memory bandwidth.

The 68332 has two halves: a 68000 that handles system control and sets up display-list processing and an on-chip graphics unit that provides print processing. The graphics unit includes the RGP, the Print-engine Video Controller (PVC), and a DRAM controller. The RGP interprets the display list and produces a page image, which the PVC then passes to the print engine. The graphics unit handles display lists or banded display lists to build a page image. Banded printing significantly reduces hardware costs by breaking a page image into horizontal bands. With banding, the memory must store only part of a page at any time, reducing image memory by one-fourth to 1/20. Motorola engineers worked with Peerless Systems Corp to tailor the 68332 for banded printing and to run Peerless printing software.—**Ray Weiss**

Motorola Microprocessor and Memory Technologies Group, Austin, TX. (214) 891-2154. **Circle No. 346**

Motorola 68332 16/32-bit μP for printers

- 16-, 20-MHz clock
- 68EC000 (32-bit registers, 16-bit ALU, data path) acts as system controller
- Graphics unit: RISC engine interprets display list, builds bit map
- Print-engine Video Controller ships bit map to print engine
- Supports print banding, multiple print-description languages: HP PCL, PostScript, MS-Windows Printing system
- DRAM controller for display memory
- DMA controller passes data to DRAM
- ROM, PROM, I/O controller
- 8-bit parallel port (to 2 Mbytes/sec)
- 160-pin PQFP
- $17.95 (10,000), May production



A highly integrated chip, the Motorola 68332 combines a 68-kbyte CPU and a PROM/EPROM controller with a graphics engine to generate printer images.

TI multiprocessor chip peaks at 2 billion operations/sec

DSP processing will never be the same. TI's new Multimedia Video Processor (MVP) delivers breakthrough peak performance topping 2 billion operations/sec. How? TI has integrated four DSP CPUs and a 32-bit RISC CPU with a fast crossbar memory (50 kbytes) and memory and video controllers—all on a single chip.

Multiprocessing is the order of the day with the MVP. Each of the five processors—four parallel DSPs and a 32-bit RISC with its own FPU (floating-point unit)—execute independently and concurrently. A unique high-speed crossbar connects the CPUs with 25 2-kbyte blocks of dedicated SRAM. Any processor can access any SRAM block, although five blocks are dedicated to each CPU.

The chip supports high processor throughput. Each CPU has its own internal instruction cache: 2 kbytes for the DSPs and 4 kbytes for the RISC CPU. The RISC CPU also has 4 kbytes of data cache. The DSP processors get their data from their dedicated SRAM blocks through the crossbar. An access takes a cycle. The CPUs can achieve apparent single-cycle execution by executing out of their own instruction

caches and accessing crossbar memory.

The DSP CPUs follow in the DSP architecture tradition: They each have three zero-overhead loop controllers for X,Y MAC computations. They also have two 32-bit paths to the crossbar memory for concurrent X,Y variable/constant access. Interestingly, the DSP CPUs use a 64-bit-wide instruction word with three major subfields for specifying the operation and the X,Y addressing. They have a 32-bit ALU and a 16×16-bit or two 8×8-bit multipliers. Additionally, the DSP CPUs support bit-field and pixel processing and word packing.

The 32-bit RISC CPU has some special features. It has an integrated 64-bit FPU, which shares a common 31×32-bit register file with integer processing. The registers are scoreboarded to minimize register contention. The CPU has a basic 32-bit instruction word. A long immediate instruction does a second access to the instruction cache or memory for an immediate value. Unlike in standard RISC architectures, the instruction word is not a single fixed-field format. Additionally, memory accesses are not confined to an optimized fixed-word access; a transfer controller interfaces to external memory and has a dynamically resizable bus.

The FPU includes a single-precision floating-point multiplier and a double-precision floating-point adder. It also supports vector processing with built-in vector operations and four accumulators to hold interim vector results. Both the CPU main integer path and the FPU units are pipelined. The CPU has a 3-stage pipeline. A single-precision floating-point multiply typically completes in three cycles; a double-precision floating-point add, four cycles. FPU operations start out of the main integer pipeline.

The MVP goes beyond standard DSP/μPs: It has more than just CPUs and memory. The MVP has its own on-chip I/O and memory controller—the Transfer Controller (TC). The TC provides an adaptive memory interface with automatic byte alignment, as well as both linear and X,Y (frame-buffer) addressing. It supports DRAM, VRAM (video RAM), and SRAM. The MVP also has a video controller to minimize design for video applications. This controller supports two video frames (all video signals). It also has a special serial register transfer controller for transferring VRAM frame memories through the TC.—**Ray Weiss**

TI Multimedia Video Processor chip—TMS320C80

16-, 50-MHz clock
2 billion operations/sec
4 million transistors, 0.5-μm CMOS
- 3-input, 8-, 16-, 32-bit ALU
- 16316- or 838-bit multiply
- 64-bit instruction word
- 2-kbyte instruction cache
- Three zero-overhead loop controllers
- Bit-change detect in word
- Pixel and bit-filed operations
- Two address units (local, global).
- Two 32-bit crossbar data interfaces
- One 64-bit instruction crossbar interface

32-bit RISC CPU
- 4-kbyte instruction cache
- 4-kbyte data cache
- 64-bit FPU
- 31 32-bit register file
- Scoreboarded for IU and FPU
- Supports vector processing
- 64-bit data, 32-bit instruction
- Memory interface (to crossbar)

Crossbar memory
- Direct access for all CPUs, TC
- 25 2-kbyte RAM blocks
- Five 2-kbyte blocks per CPU
- Any CPU can address any memory block
- Up to 15 parallel accesses/clock cycle
- Up to three accesses/cycle for DSP CPUs
- Round-robin priority settles access contention

JTAG test and emulation unit
- JTAG test port
- Links all CPUs
- Background mode control of CPUs
- Integrated debugging: one breakpoint stops all CPUs
- Acts as I/O controller
- 400-Mbyte/sec peak off-chip transfer rate

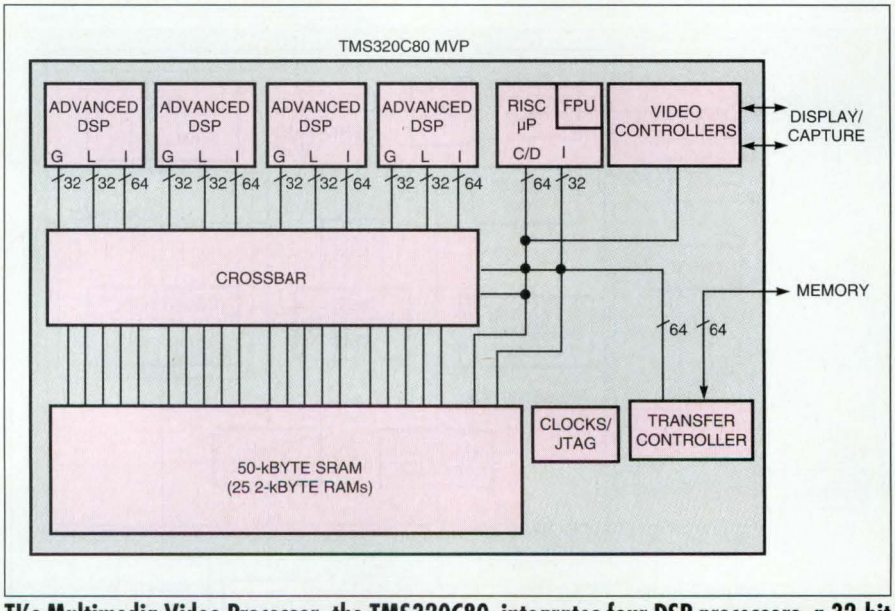
Transfer controller
- Links CPUs, crossbar to external memory
- DRAM/SRAM/VRAM interfaces
- Linear X,Y addressing
- 64-bit, dynamic bus sizing
- 400-Mbyte/sec max transfer rate

Video controller
- Two Frame Timers with its own clock, generates horizontal, vertical
- Frame timers for capture or display
- VRAM control
- Automatic byte alignment

Big or little Endian operation
3V (5V I/O), 305-pin CPGA
$300 to $400 (10,000) sampling

Texas Instruments Inc, Semiconductor Group, Houston, TX. (800) 477-8924, ext 4500. **Circle No. 347**

For more information on develop ment tools, see pg 65.



TI's Multimedia Video Processor, the TMS320C80, integrates four DSP processors, a 32-bit RISC and 50 kbytes of SRAM on a single chip. It delivers a new level in DSP and computing performance that can tackle computation-intensive applications in real-time compression/decompression for video, image, and audio processing. It can tackle problems that now require arrays of DSPs and μPs.

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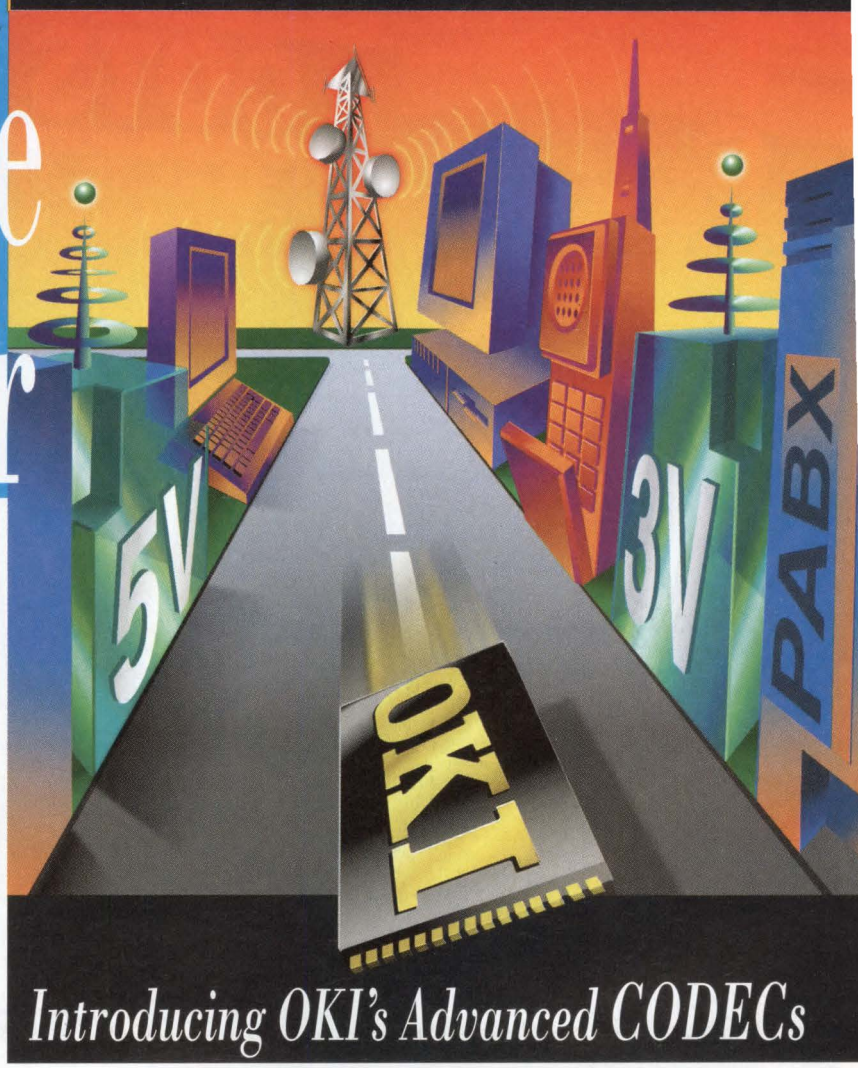
MSM7560	5 Volt	ADPCM	SOP
MSM7570/90	5 Volt	ADPCM	TSOP
MSM7570L/90L	3 Volt	ADPCM	TSOP



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VICOR

CIRCLE NO. 73

INTEGRATED CIRCUITS

High-voltage ICs displace magnetic components for electronic ballasts

Electronic-ballast circuits have remained one of the last domains of discrete, transformer-based designs that suffer from a number of liabilities: These circuits can't self-start, they have slow switching times, and they use labor-intensive components such as toroidal current transformers. These circuits are also expensive to manufacture in large quantity and aren't amenable to dimming.

These limitations coupled with the need for more efficient lighting systems (the cost of power conservation is much less than that of building new power plants) and the availability of power MOSFET switches, which have inherent efficiency advantages, have created a push for efficient, low-cost, and small driver ICs.

International Rectifier's IR2155 self-oscillating power MOSFET/insulated-gate bipolar-transistor (IGBT) gate driver is the first in a family of power ICs tailored to electronic ballasts for fluorescent lighting, partly because of its small size (8-pin DIP) and low cost ($1.96 (100) and $0.98 (50,000)). And, it is the most recent addition to the company's general family of MOS gate drivers. These power ICs can drive low- and high-side MOSFETs or IGBTs from logic-level, ground-referenced inputs. The IR2155 also suits high-frequency switch-mode power supplies and motor drives.

The IC integrates a number of noteworthy features: an integrated high-side driver that replaces the discrete transformer drive circuits, an on-chip self-starting oscillator that eliminates additional control circuitry, and an on-chip shunt regulator that generates 15V from the high-voltage bus via a low-wattage dropping resistor. Because of the on-chip regulator, the IC can operate without a bias supply directly off the rectified line voltage. The company produces the IC using a process that can integrate high-voltage structures with CMOS circuits.

The chip produces clean drive waveforms that minimize power MOSFET switching losses. These reduced losses allow designers using the IC to either downsize the power MOSFET or dispense with the heat sink. The internal oscillator is similar to the 555 timer, and the frequency is equal to $1/(1.4\times R_t\times C_t)$.

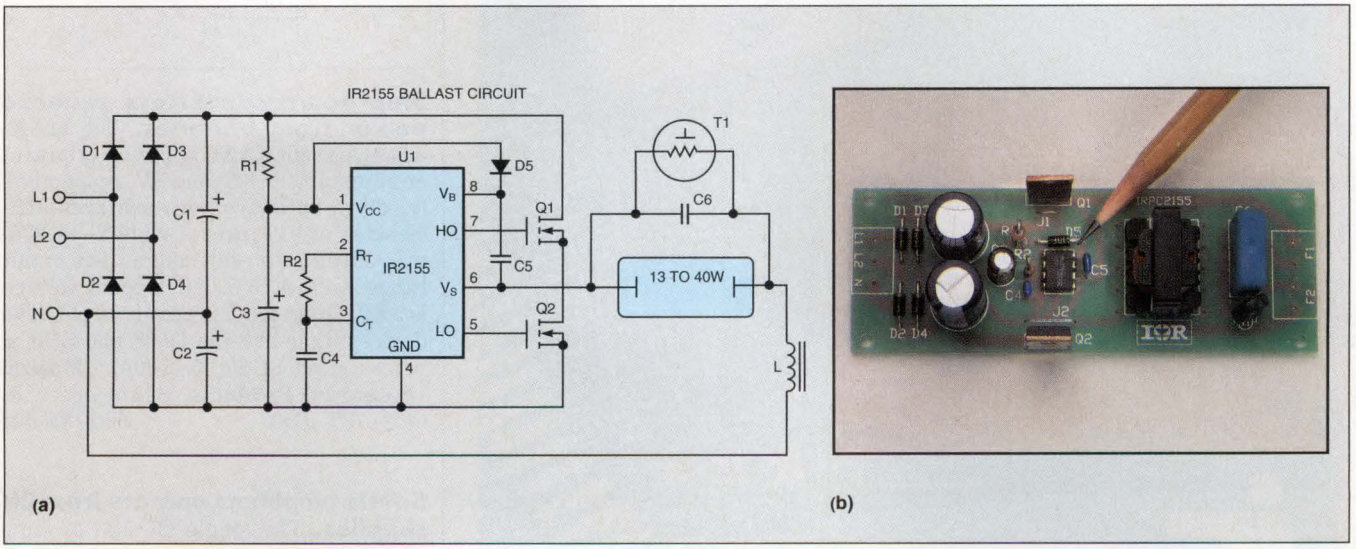
The output drivers feature a high-pulse-current buffer stage and an internal dead time of 1200 nsec for minimum driver cross-conduction. This dead time is compatible with dv/dt-snubbed circuits to operating frequencies of 100 kHz. Rated for 600V, the IR2155 is appropriate for all off-line 120/240/277V-ac ballasts, even those that include electronic power-factor correction.

Other notable features are respective output rise and fall times into a 1000-pF load of 80 and 40 nsec. The chip has a ±50 V/nsec dv/dt immunity, a 120-μA typical start-up supply current, a typical quiescent current of 500 μA, a maximum V_{CC} start-up current of 250 μA, and undervoltage lockout.

A companion driver, the IR2111 ($1.58 (1000)), is identical to the IR2155 except that it doesn't include the internal oscillator and regulator. You can use this IC with the IR2155 to implement a full-bridge 160W fluorescent ballast and other H-bridge circuits for larger power supplies. The IR2111 also comes in an 8-pin DIP, and SOIC versions will be available by the middle of the year.

At that time, the company also will release devices similar to these ICs but with ballast wattage ratings below 40W and with 100-mA output-source and sink currents.—**Anne Watson Swager**

International Rectifier, El Segundo, CA. (800) 245-5549. **Circle No. 403**



The 8-pin IR2155 MOS gate driver and surrounding circuitry that together implement an electronic ballast (a) take approximately 1.5×4.25 in. of board space (b). The circuit drives a 13 to 40W fluorescent lamp from a 115 to 230V-ac input. (Ask for Design Tips #DT94-3 for details of board, schematic, and parts list.)

INTEGRATED CIRCUITS

BiCMOS PWM controller runs on low power. The UCC3570 BiCMOS PWM controller features an 85-μA start-up current, a 1-mA run current for off-line operation, and the ability to drive a 1A MOSFET gate at frequencies up to 500 kHz. The device implements voltage feed-forward and responds to wide line-voltage variations without noise sensitivity. $2.10 (1000). **Unitrode Integrated Circuits Corp**, Merrimack, NH. (603) 424-2410.
Circle No. 405

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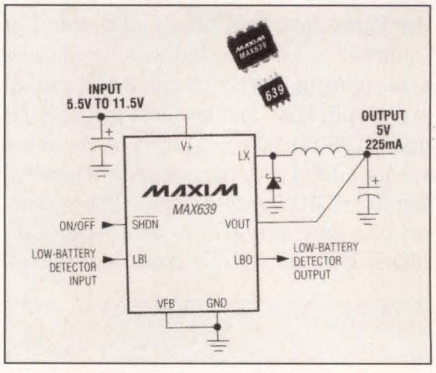
Inverting switching regulators are 85% efficient. The MAX774 delivers –5V at up to 1A with inputs from 3 to 16.5V. The MAX775 delivers –12V at up to 0.5A with inputs from 3 to 9V. The MAX776 delivers –15V at up to 0.4A with inputs from 3 to 6V. The devices' efficiency stems from a low quiescent current, which is a maximum of 100 μA and from a current-limited pulse-frequency-modulated control scheme. This scheme provides the benefits of PWM converters without high supply currents. The devices come in 8-pin DIPs and SOICs; prices start at $2.20 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600.
Circle No. 406

12-bit ADC samples at 800 kHz. The ADS7810 ADC contains a clock, an S/H amplifier, a 2.5V reference, a parallel μP interface, and 3-state output drivers. The manufacturer guarantees the sampling rate over the extended industrial temperature range of –40 to +85°C. S/N ratio plus distortion is a minimum of 70 dB, maximum integral nonlinearity is ±0.5 LSB, maximum differential nonlinearity is ±0.9 LSB, and maximum power dissipation is 250 mW. The device comes in a 28-pin DIP, SOIC, or die form; prices start at $29.45 (100). **Burr-Brown Corp**, Tucson, AZ. (602) 746-1111.
Circle No. 407



Step-down converters squeeze power from batteries. The MAX639/MAX640/MAX653 family of preset or adjustable 5, 3.3, and 3V, respectively, dc-to-dc converters achieves efficiencies of 94% over a wide 2- to 225-mA output-current range. The input range is 4 to 11.5V, and dropout voltage is 0.5V. Quiescent current is 10 μA. The devices come in 8-pin DIPS and SOICs; prices start at $2.95 (1000). **Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600.
Circle No. 408

5-MHz amplifiers operate from 3V supplies. The single OP-183 op amp and its dual counterpart, the OP-283, feature complete characterization data for operation from 3, 5, and ±15V supplies. The manufacturer guarantees 3V operating parameters, such as maxi-

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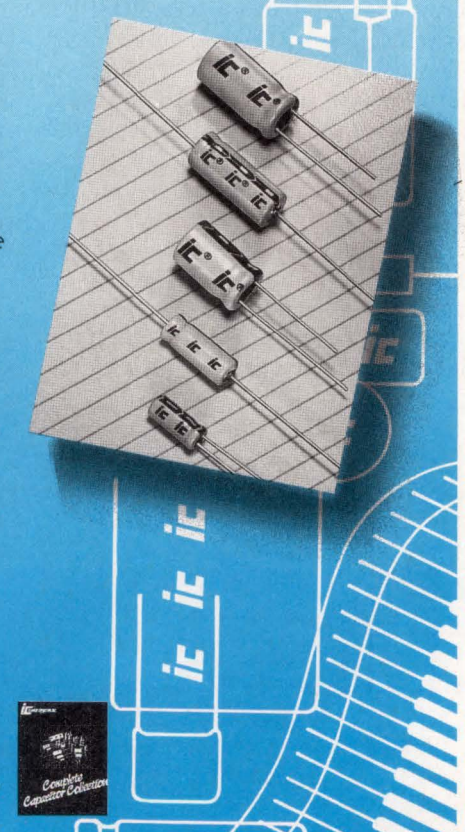

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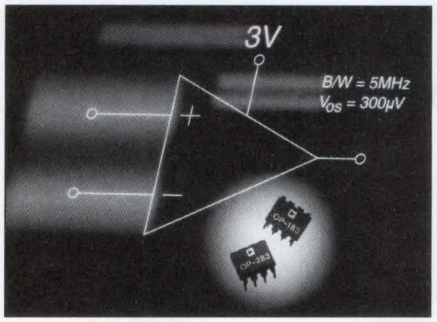
CIRCLE NO. 2

INTEGRATED CIRCUITS



mum input offset voltage of 1 mV, maximum offset current of ±50 nA, and maximum input bias current of 600 nA. Using a 3V supply, the op amps handle 1.5V input swings and provide 260-V/mV large-signal voltage gain with 104 dB of common-mode rejection. Supply current is 1.5 mA/amplifier, and voltage noise density is 10 nV/√Hz. Full-power bandwidth is 50 kHz, and 0.01% settling time is 1.5 µsec. The devices come in 8-pin DIPs and SOICs, and prices begin at $1.58 and $2.39, respectively. **Analog Devices**, Wilmington, MA. (617) 937-1428. **Circle No. 409**

Video multiplexers switch at 150 MHz. The LT1203 and LT1205 fast-switching multiplexers have low crosstalk of over 90 dB from dc to 10 MHz. The 1203 ($2.73 (1000) for DIPs and $2.96 for SOICs) is a 2-input, 1-output device in an 8-pin package; the 1205 ($5.06) is a dual version with four inputs, and two outputs in a 16-pin SOIC. Both parts have a minimum input impedance of 1 MΩ while driving a 1-kΩ load, eliminating the need for input-buffer amplifiers. A disable function puts the devices in a high-impedance state, which allows you to short the outputs together and run the ICs in parallel. Video characteristics include gain flatness of 0.1 dB to 30 MHz and differential gain and phase of 0.02% and 0.02°, respectively. The supply range is ±5 to ±15V. **Linear Technology Corp**, Milpitas, CA. (408) 432-1900. **Circle No. 410**

6-bit ADC can sample at 100 MHz. The MN5909 CMOS flash ADC samples twice as fast as the company's MN5906 at a guaranteed minimum of 85 MHz. When operating from a 5V supply, the ADC typically dissipates 200 mW. S/N ratio plus distortion is 30 dB min, and spurious-free dynamic range is 35 dB while sampling at 85 MHz and converting 10-MHz input signals. Maximum integral and differential nonlinearity errors are ±1 and ±3.4 LSB, respectively. The manufacturer guarantees no missing codes. In 20-pin DIPs and SOICs, the converter costs $19.25 (1000). **Micro Networks**, Worcester, MA. (508) 852-5400. **Circle No. 411**

Dual differential amplifier has 5-GHz power gain bandwidth. The HFA3102 long-tailed pair-transistor array contains two npn differential amplifiers with tail transistors. The array suits single-balanced mixers and AGC circuits for RF or first-IF amplifiers, multipliers, and local oscillators. The $2.66 (1000) IC in a 14-pin SOIC is pin-compatible with NEC's UPA102G but has a higher transistor-cutoff frequency of 10 GHz. Current gain is 70 and matches transistor-to-transistor within ±10%. The noise figure for each transistor is 3.5 dB. Collector cutoff current is 10 nA, and collector leakage current is <0.01 nA. **Harris Semiconductor**, Melbourne, FL. (800) 442-7747, ext 7154. **Circle No. 412**

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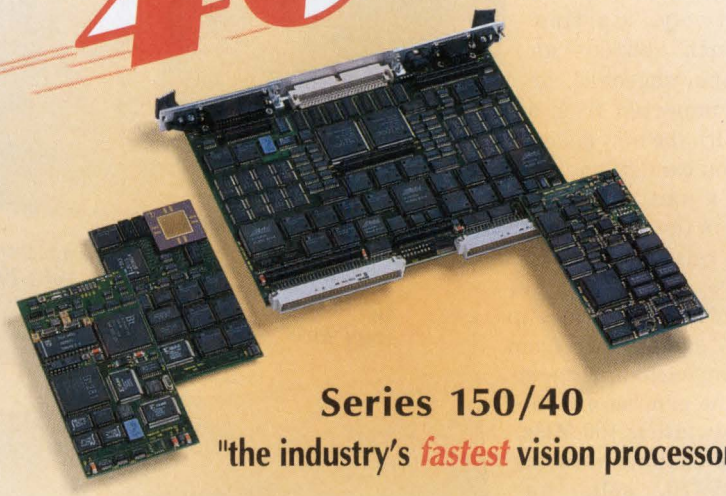

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CIRCLE NO. 3

ARBs bring a new level of interactivity to waveform definition

Defining the custom waveforms output by DAC-based arbitrary-waveform generators (ARBs) has always been tedious and time-consuming. Generators from such vendors as Analogic (Peabody, MA), Fluke Corp (Everett, WA), Pragmatic Instruments (San Diego, CA), and Wavetek (San Diego, CA) began to address the problem several years ago. Numerous software packages, including a new one—Tektronix's WaveWriter—also help you perform the task.

But none of these products goes quite as far as new generators from LeCroy and Tektronix. These ARBs, which include large CRTs that make them look just like DSOs, let you define waveforms interactively, starting from such sources as equations, sketches, or signals imported from a DSO. With the new generators, you can try out signals on a unit under test and tweak the signals until the unit reveals its secrets.

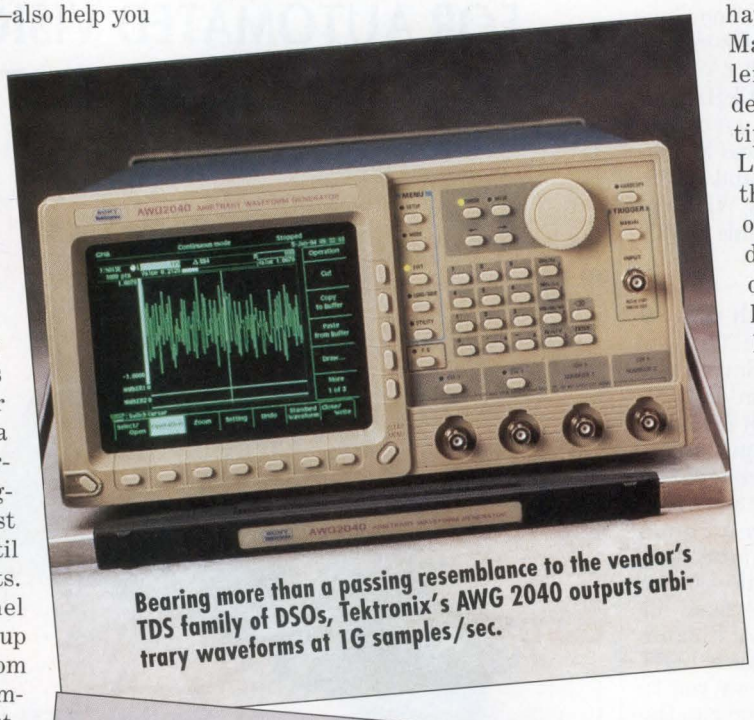
LeCroy's 2-channel LW420 ($18,950) outputs up to 400M samples/sec from 256k-sample/channel memories. The generator's output bandwidth is 100 MHz. A single-channel version, the LW410, sells for $13,945. Both units give you the option of 1M-sample/channel waveform memories. Tek's AWG 2040 ($19,995) outputs 1G sample/sec on one channel from a 4M-sample memory. The company's 4-channel AWG 2005 ($9995) outputs 20M samples/sec from memories that hold 64k samples/channel.

Although earlier generators had waveform-definition capabilities, engineers have customarily used PCs to perform this task off-line. If you use an IEEE-488 or an RS-232C interface, you can link a PC running a waveform-definition package to an ARB that has only minimal definition capabilities. You can then try out and tweak your waveforms much as if you were using one of the new generators. Tek and LeCroy insist, however, that many users find it too cumbersome to use both a PC and a generator for waveform definition. According to the instrument companies, these users want the definition capabilities in the generator, and the vendors believe that their new products provide the functions necessary to take the pain out of the definition process.

Waveform definition has been plagued by several problems you're unlikely to think of until you have to define a waveform. Many generators require the length of the data set that defines a waveform to be a multiple of eight samples. The LeCroy units allow ensembles that have any integral number of samples up to the memory depth. Modifying a waveform often results in changing the length of the sample set. To keep the repetition rate of the output waveform constant, you must tweak the clock rate to compensate. With the LeCroy and Tek generators, you needn't think about such details.

Both vendors' generators provide extensive waveform-editing capabilities. As with a word processor, you can edit in either insert or overstrike modes. In overstrike mode, your changes replace portions of the original waveform; the insert mode adds points between points that you choose. LeCroy also touts an undo feature that keeps you from losing your work if things go awry during your editing session.

One specification of the



Bearing more than a passing resemblance to the vendor's TDS family of DSOs, Tektronix's AWG 2040 outputs arbitrary waveforms at 1G samples/sec.

Looking exactly like the vendor's Scopestation 140 DSO, LeCroy Corp's LW420 and 410 output arbitrary waveforms at 400M samples/sec. Like the Scopestation, the generators include PC motherboards.

LeCroy generators and Tek's higher speed unit at first seems impossible: Both vendors claim 100-psec edge-placement resolution. Yet, all of these generators have a minimum clock period much longer than 100 psec—2500 psec for the LeCroy units; 1000 psec for the AWG 2040. The secret lies in the fact that the generators produce an analog output. If you realize that an edge is actually a ramp defined by several points, you discover that you can position an edge with greater precision than you might have thought possible.

Both vendors' generators incorporate a lot of high technology. The LeCroy units include a 33-MHz 80486DX PC mother-board with 16 Mbytes of RAM and a 130-Mbyte hard drive (a 240-Mbyte hard drive is optional). The LeCroy generators store data initially in a 4-byte/point floating-point format. DSP algorithms that run on the CPU chip's numeric coprocessor reduce the data to the 8-bit form that drives the output DAC. These algorithms perform a host of functions. For example, they filter the data to limit the signal bandwidth or slew rate, and they allow you to define waveforms in the frequency domain by specifying amplitude and phase relationships among the component frequencies.

It seems likely that in the future these vendors will produce less expensive generators that incorporate the new units' advanced output features but lack their waveform-definition capabilities. EEs in test development and design need generators that include the definition features. Organizations such as production-testing facilities need the definition capabilities much less; test departments are in the business of using waveforms, not of defining them. The LeCroy and Tek products let design and test-development engineers define waveforms and then transfer them to lower cost generators through floppy-disk drives or network connections.—**Dan Strassberg**

LeCroy Corp, Chestnut Ridge, NY, (800) 453-2769. **Circle No. 301**

Tektronix Inc, Beaverton, OR, (800) 426-2200. **Circle No. 302**

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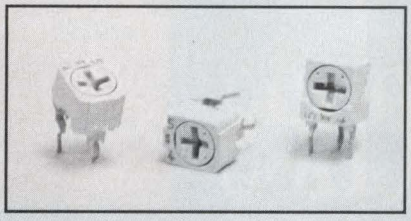

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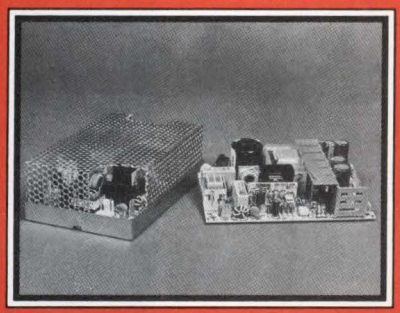

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CIRCLE NO. 9

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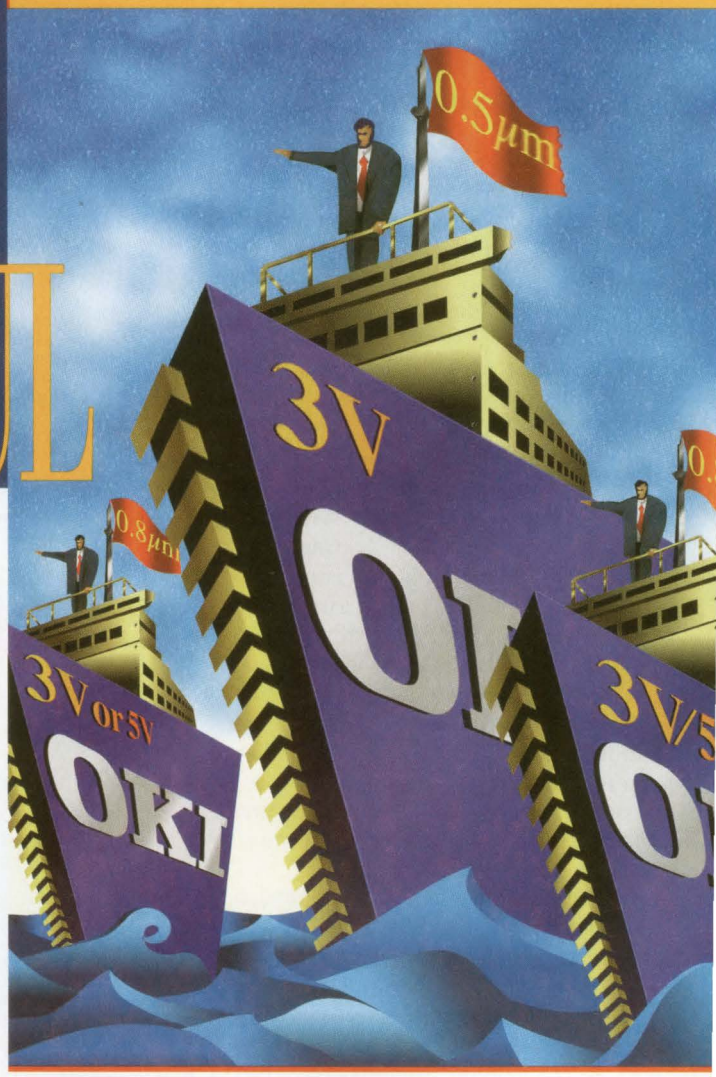
MSM92S	Supply voltage High-density macrocells	2.7 ~ 5.5 V ROMs, single- and dual-port RAMS



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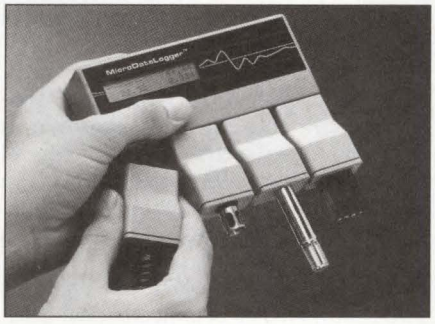
Circle No. 423

Data-acquisition units connect to PC parallel ports. As many as 15 5.5×1.75×7.5-in., 2-lb DataShuttles connect to one parallel port of a PC. Each of the units includes eight analog inputs with a choice of 12- or 16-bit resolution, eight digital I/O channels, and a counter/timer. GUI software is included. When you use the units to measure temperature, you can expect reading errors as low as 0.005 °C. From $995. **Strawberry Tree Inc,** Sunnyvale, CA. (408) 736-8800. **Circle No. 424**

Antivirus system includes software and hardware. The PC Defender ($119.95) comprises three elements: Scan and Clean software, a boot-monitor card that fits in an 8-bit ISA-bus slot, and an illegal-activity monitor, which loads as a DOS device driver but also works under Windows V3.1. You can use the Scan and Clean software to immunize files against future virus infestations. **American Megatrends Inc,** Norcross, GA. (404) 263-8181.
Circle No. 425

Windows data-acquisition-board drivers support 32-bit applications. DriverLinx V2.0 is a series of multiuser, multitasking drivers that run under Windows 3.x and work with boards from six vendors. The software is compatible with both the Win 32s API (a subset of the Windows NT API) and Watcom's proprietary Windows extensions. $395; upgrade for current users, $49. **Scientific Software Tools Inc,** Paoli, PA. (215) 889-1354.
Circle No. 426

VXIbus systems test SDH and SONET network elements. The VX4610 module and the SX4610 system permit comprehensive production testing. The $40,000 module is compatible with software for the vendor's recently announced CTS 710 and 750 SONET and SDH test sets. The $55,000 system includes a 13-slot VXI mainframe. Options add 52-, 155-, and 622-Mbps optical signal interfacing and DS-1/DS-3 and E1 tributary testing. **Tektronix Inc,** Beaverton, OR. (800) 426-2200.
Circle No. 427



Tiny 4-channel data logger accepts plug-in signal conditioners. The self-configuring, battery-powered MicroDataLogger accepts signal conditioners for temperature, humidity, pressure, light level, ac and dc current, power, luminance, occupancy, and rotational velocity, among other parameters. The logger stores 16,000 12-bit readings per channel. An internal real-time clock time-stamps the data. <$1000. **Architectural Energy Corp,** Boulder, CO. (303) 444-4149.
Circle No. 428

RF power meter measures to 26.5 GHz. The Rohde & Schwarz NRVS measuring heads are fully characterized at the factory and never need adjustment. Within each head is an EPROM containing the calibration data, including frequency response and temperature sensitivity. Both diode and thermal sensors are available. $2330; delivery, six weeks ARO. **Tektronix Inc,** Beaverton, OR. (800) 426-2200.
Circle No. 429

New μP speeds 5G-sample/sec, 2-channel portable DSO's command processing. The 9360 now includes a 33-MHz 68030 μP. The new processor speeds up most operations on the 600-MHz-bandwidth real-time scope by a factor of 2 to 3. There is no increase in the $12,490 price. **LeCroy Corp,** Chestnut Ridge, NY. (914) 425-2000. **Circle No. 430**

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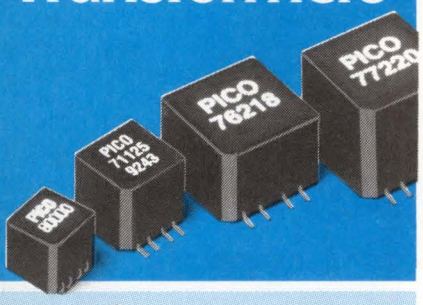

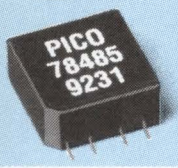

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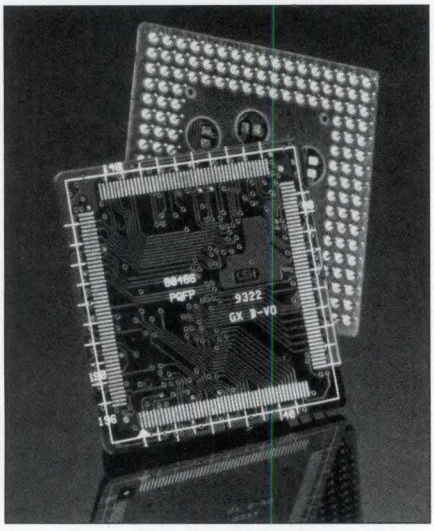
CIRCLE NO. 17

COMPONENTS

Broadband mixer covers 200- to 3000-MHz range. The RMS-30 broadband mixer covers 200 to 3000 MHz. The surface-mount device's all-ceramic housing measures 0.25×0.31×0.275 in. The units can pass MIL-M-28837. $6.95 (50). **Mini-Circuits,** Brooklyn, NY. (417) 335-5935. **Circle No. 440**

Power MOSFETs suit low-voltage applications. A line of low-voltage, low-power ($R_{DS(ON)}$) MOSFETs come in hermetic, isolated TO-254, TO-258, and TO-257 metal packages. The maker screens all units to MIL-S-19500, TX, TXV, and "S" levels. $34.50 to $43.05 (100). **Omnirel Co,** Leominster, MA. (508) 534-5776. **Circle No. 441**



Adapter converts quad-flatpack ICs to pin-grid-array devices. An adapter for 196-lead plastic quad flatpacks (PQFPs) 486 CPUs converts them into 169-lead PGA (pin-grid-array) devices. The adapter has an FR-4 glass-epoxy base and measures 1.6 mm square and 1 mm thick. The combination of the PQFP 486 CPU and adapter is less expensive than a PGA 486 CPU. $10 (1000). **TelTec Inc,** Minneapolis, MN. (612) 854-9177. **Circle No. 442**

Compact electrolytic capacitors have high capacitance. The SI series of electrolytic capacitors measures 22 mm in diameter×20 mm long. The snap-in devices are available in values from 47 μF to 33 mF (±20%) and voltage tolerances from 16 to 450V dc. Their operating range is –40 to +85°C, and load life is 2000 hours (±12 hours) at their maximum rated voltage. $1.59 to $10 (10,000). **NTE Electronics,** Bloomfield, NJ. (201) 748-5089. **Circle No. 443**

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Capacitor networks come in 4- to 14-pin configurations. The 900 Series of capacitor networks suit bypassing, filtering, coupling, and terminating applications for ICs. The capacitors can be bused or isolated. Delivery is eight weeks ARO for nine stock configurations. Isolated, $0.86; bused, $1.43 (500). **Bourns Inc,** Logan, UT. (801) 750-7200. **Circle No. 444**

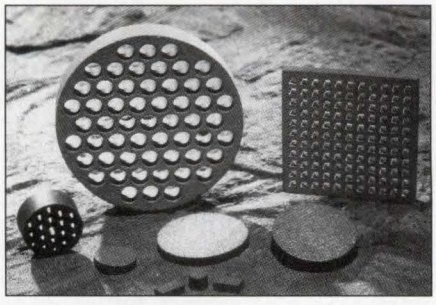
Nonexplosive separation nut provides safe release of hardware in critical applications. The Model 9421-2 nonexplosive separation nut, a space-grade 0.25-in. fastener, permits separating hardware in 20 msec with very low shock and no debris, contaminants, or pollution. Each nut contains two redundant electromechanical actuators. You can reset the nut using no special safety or handling restrictions. The nut carries the 5000-lb mating load of ¼-28UNF bolts. Operating temperatures range from –238 to +250°F. $2495 (25); delivery is two weeks ARO. **G&H Technology,** Camarillo, CA. (805) 484-0543. **Circle No. 445**

Tiny switch combines pushbutton with slide action for small, portable devices. The model MMPS101 switch measure 0.276 in. wide×0.472 in. long×0.079 in. high. The surface-mount switch's single button works as both a single-pole momentary pushbutton switch and a 1-pole, 3-position (maintained) slide switch. The switch body has seven 0.04-in. terminals and two pc-board projecting bosses. The switch's contact rating for both the pushbutton and slide contacts is 200 mA at 4V dc from –10 to +60°C. The switch body is high-temperature PPS and has molded-in, gold-plated copper-alloy contacts, a rigid stainless-steel frame, and a 6/6 nylon actuator. $2.59 (1000). **MORS/ASC,** Wakefield, MA. (617) 246-1007. **Circle No. 446**

IR thermocouple requires no power. The model IRt/c IR sensor has a 10:1 field of view. The device can measure the temperature of a 1-in. spot from a distance of 10 in. Its temperature ranges from –50 to >+3000°F. The device is intrinsically safe and exceeds all applicable NEMA standards. $199 (single sample). **Exergen Corp,** Newton, MA. (617) 527-6660. **Circle No. 447**

Passive network tightens up PCMCIA fax-modem cards. The IPEC series of thin-film network integrates 16 passive components in a monolithic chip. The components assist Personal Computer Memory Card International Association (PCMCIA) fax-modem cards in meeting international EMI/RFI specs. The series comprises three standard resistor/capacitor values. $2.30 to $3 (10,000); delivery, six to eight weeks ARO. **California Micro Devices Corp,** Milpitas, CA. (408) 263-3214. **Circle No. 448**

RF coaxial connectors feature quick-change design fo wattmeters. A line of quick-change RF 7/16 is compatible with a wide variety of multilevel wattmeters and is available in male and female configurations. Suitable for high-power testing and monitoring, the connectors meet DIN 47223 and IEC 169.4 requirements. The connectors feature 50Ω impedance, low VSWR up to 7 GHz, and a voltage rating of 2.7 kV. Male, $135; female, $65. **Tru-Connector Corp,** Peabody, MA. (508) 532-0775. **Circle No. 449**



PTC thermistors make dandy self-regulating heaters. Positive-temperature-coefficient (PTC) thermistors combine a heater and thermostat in one ceramic material. Because of their high temperature coefficient of resistance, these devices respond to temperature changes by automatically adjusting their power dissipation, maintaining a nearly constant body temperature over a wide ambient-temperature range. Configurations include chips and disks with no leads as well as special configurations with patterned holes. An application note is available. Standard devices cost $0.20 to $1 in large quantities. **Keystone Carbon Co,** St Marys, PA. (814) 781-4444. **Circle No. 450**

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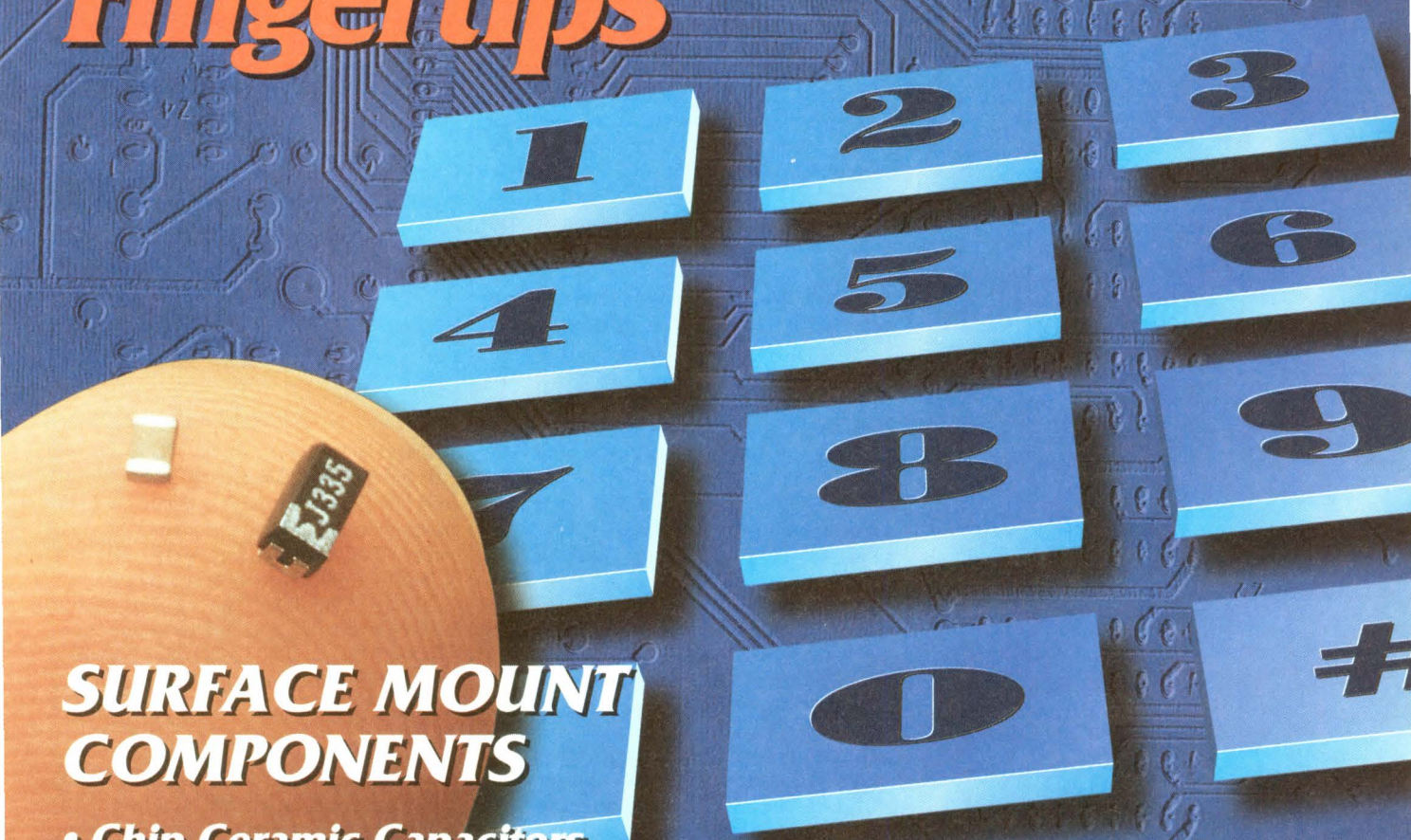

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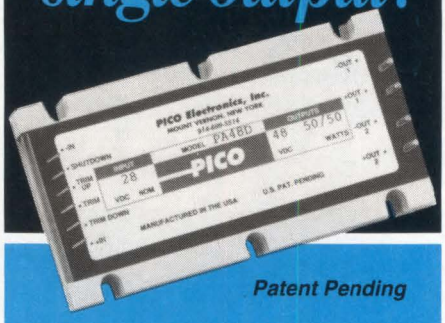

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EDN-New Products

POWER SOURCES

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Nickel metal-hydride cell is available in "prismatic" form. The model HHF80T nickel metal-hydride (NiMH) cell comes in rectangular, or "prismatic," form, permitting more densely packed batteries than possible with

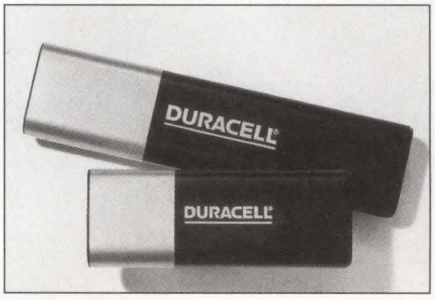
cylindrical cells. The cells measure 17 mm long×6.1 mm wide×67 mm high. The cells have a nominal output voltage of 1.2V and a nominal capacity of 760 mAhr. $8 (500 to 1000). **Panasonic Industrial Co,** Secaucus, NJ. (800) 848-3979. **Circle No. 432**

SIP bridge rectifiers streamline assembly and save space. Three pc-board-mounted, 3-ϕ, full-wave-bridge rectifiers suit inverters, servo motors, and HVAC applications. The devices' ratings are 20A at 800V ($10.15), 30A at 800V ($11.05), and 30A at 1600V ($13.50). Delivery is 16 to 18 weeks ARO. **Toshiba America Electronic Components Inc,** Irvine, CA. (714) 455-2000. **Circle No. 433**

Supply takes 50% less space than conventional models. The model SPA-125, a fully enclosed off-line 125W switcher supplies 56V dc. The device lets you parallel multiple units to achieve *n*+1 redundancy in the front end of a distributed-power system. The unit has Class B EMI filtering, thermal protection, remote on/off, and a power-fail signal. The unit also recharges a 48V backup battery. **MicroEnergy Inc,** Longwood, FL. $178 (100). (407) 831-2000. **Circle No. 434**

Integrated switching-regulator family conserves pc-board space. A family of integrated switching regulators includes three models that are pin-compatible with linear regulators. The PT5100 offers 3.3, 5, and 12V outputs. The dual 1A PT5600/7500 is a dual-output version of the company's standard 1A models. The PT6100 exhibits 90% efficiency, comes in a 12-pin SIP, and has adjustable outputs. PT5100, $11.90; PT5600, $19.90; PT6100, $14.90 (100). **Power Trends,** Batavia, IL. (708) 406-0900. **Circle No. 435**

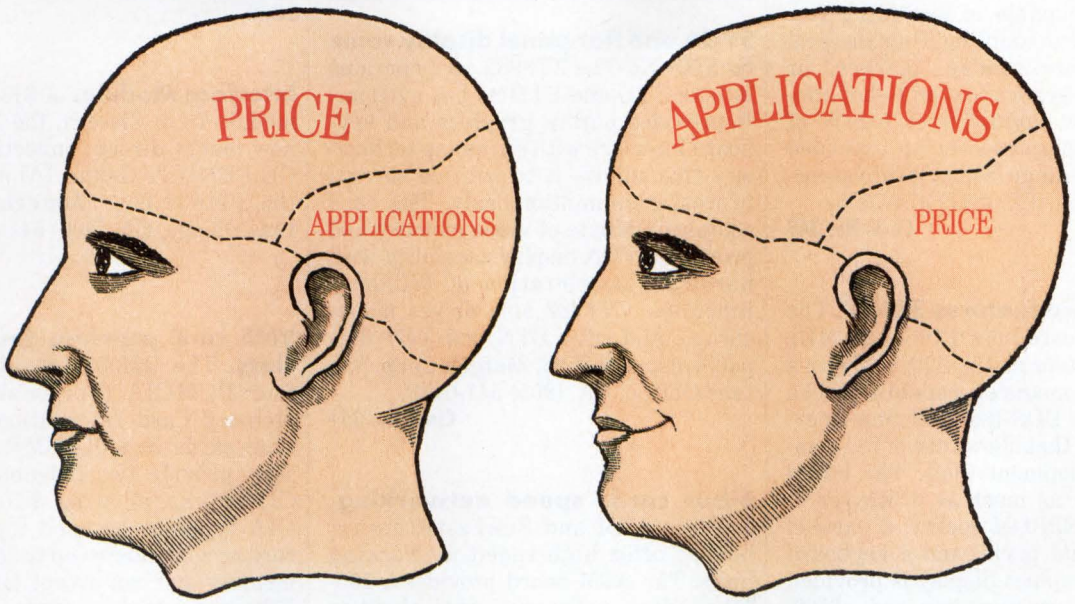
Bulk supplies fit three to a rack. The model LT1700 universal-input converter provides 400W at 56V dc. The unit comes in a 4×5×7-in. package. It features transient suppression, filtering, control, and shock and vibration immunity. You can parallel three units in one 5.25-in. rack. The supply operates at up to 71°C without forced air or heat sinks. The unit has a negative temperature coefficient for safe battery charging. Holdup time (when powering the company's dc/dc converters) is 75 to 300+ msec. $1036 (one); delivery, six weeks ARO. **Melcher Inc,** Chelmsford, MA. (508) 256-1812. **Circle No. 436**



NiMH batteries hold 40% more juice than NiCd batteries. The DR19 and DR31 nickel metal-hydride (NiMH) batteries last 40% longer than comparably sized NiCd batteries. The DR19 is a 10.8V, 1500-mAhr battery in a 9×4/5A package. The DR31 is a 10.8V, 2400-mAhr battery in a 9×4/3 A package. DR19, $99; DR31, $169. (retail). **Duracell International Inc,** Bethel, CT. (203) 796-3281. **Circle No. 437**

Inverters power CCFT backlighting of dual-scan color LCDs. The L360B series of cold-cathode fluorescent-tube (CCFT) inverters work with the Sharp LM64C08P and the Hitachi LMG972/XUFC dual-scan color LCDs. The inverters measure 120×20×13 mm. The inverters accept inputs from 10.8 to 13.2V dc. Output is 1600V-ac rms for the Sharp LCD and 1300V-ac rms for the Hitachi LCD. Typical output current is 4.8-mA rms. Both inverters offer brightness control. The manufacturer's factory is ISO9001 approved. $20 (OEM quantities). **Xentek Inc,** San Marcos, CA. (619) 471-4001. **Circle No. 438**

A radical shift in thinking about high power diode lasers.



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CIRCLE NO. 76

BOARDS & BUSES

Module brings 16-bit timers to PC/104. The PMC-CTC module provides six 16-bit counter/timers in a PC/104 module. The timers are independent, each with its own buffered clock running as fast as 10 MHz. The timers are capable of providing frequency or event counting, time interval measurements, pulse marker or square-wave generation, or 1-shot simulation. The module uses 5 mW of power and operates over an extended temperature range. $125. **WinSystems Inc,** Arlington, TX. (817) 274-7555.
Circle No. 349

STEbus board features 386SX. The SCIM386T board puts a 16- or 25-MHz 386SX processor on the STEbus with a mezzanine expansion capability. The board runs a DOS-like real-time operating system that allows use of PC-compatible development tools. The board has sites for as much as 4 Mbytes of DRAM, an EPROM socket, a parallel and two serial ports, and a keyboard interface. Graphics display is provided through the mezzanine bus card. <£500. **Arcom Control Systems Ltd,** Cambridge, UK. (0)258-840999. **Circle No. 350**

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SVGA and flat-panel display come to STD-32. The ZT8982 card operates in both STD and STD-32 bus systems. It provides both a graphics and keyboard interface with switching technology that allows it to service several processors simultaneously. The card contains 1 Mbyte of video memory and provides SVGA display capability with hardware acceleration of Windows functions. ZT8982 also drives monochrome and color STN and TFT flat-panel displays. $595. **Ziatech Corp,** San Luis Obispo, CA. (805) 541-0488.
Circle No. 351

S-bus cards speed networking. The SunATM and SunFastEthernet boards offer high-speed networking links. The ATM board provides a 155-Mbps data rate over optical fiber ($1295) or UTP wire ($995). It provides AAL5 service of ATM over a SONET physical interface. The Ethernet board ($795) provides a media-independent interface and can handle 10- or 100-Mbps CSMA/CD protocol Ethernet traffic. **Sun Microsystems Computer Corp,** Mountain View, CA. (415) 960-1300. **Circle No. 352**

Interface Module. A $1350 interface module from Ziatech, the ZT 88CT93, now allows direct connection between GE FENUC's Genius I/O products and the STD-32 bus. **Ziatech Corp,** San Luis Obispo, CA. (805) 541-0488.
Circle No.353

VME card provides four PCMCIA slots. The RM230 provides slots for four PCMCIA (Personal Computer Memory Card International Association) cards in a 6U VME board. The slots provide two independent PCMCIA blocks, allowing differing PCMCIA types to be used together. The card accommodates up to 256 Mbytes of memory and can accept fax/modem or Ethernet interface cards. From $580. **Ramix Inc,** Chatsworth, CA. (818) 349-6772. **Circle No. 354**

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CIRCLE NO. 26

EDN-NEW PRODUCTS

COMPUTERS & PERIPHERALS

SPARCstation 10 system includes graphics accelerator board. The Marixx ds Graphics Station, a fully configured, desk-side SPARCstation 10-compatible system, comes with graphics for Solaris 1.1 or 2.3 preloaded on the hard drive. The system includes a Viking 50-MHz SuperSPARC μP with a 1-Mbyte external cache, a TGX200 graphics accelerator board (1920× 1080-pixel resolution), and a 2-Mbyte video RAM. It also includes 64 Mbytes of RAM, a 2-Gbyte internal hard drive, an internal CD-ROM, a 19-in. color monitor, a floppy drive, a keyboard, and an optical mouse. $28,115. **Aries Research**, Fremont, CA. (510) 659-1544.
Circle No. 340

Removable-media subsystem stores 256 Mbytes. The SyQuest-based HammerDisk PE 250 cartridge subsystem, a SCSI-2 removable-media drive, stores 256 Mbytes. The drive is compatible with 105-Mbyte data cartridges used with the manufacturer's other subsystems. Other features include a 13.5-msec average seek time, a 2.4-Mbyte/sec sustained transfer rate, a 4-Mbyte/sec burst transfer rate, a 3600-rpm rotational speed, and a 100,000-hour MTBF rate. $899. **FWB**, San Francisco, CA. (415) 474-8055.
Circle No. 341

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Software allows easy upgrades to PA-RISC. Two software packages, HP Basic/UX for the HP 9000 Series 700 platform and HP Basic Plus, lets users upgrade to the PA-RISC computer technology without sacrificing their familiar programming environment. HP Basic/UX for Series 700, Model E2046A, costs $1600; HP Basic Plus for Series 300 and 700, Model E2165A, costs $350. **Hewlett-Packard**, Palo Alto, CA. (800) 452-4844, ext 8044.
Circle No. 342

Graphics cards offer increased speeds over Sun GX cards. The TGX100 and TGX120 graphics accelerators extend the company's Turbo GX series and increase speed to two to three times the performance of standard Sun GX cards. The two cards have respective resolutions and refresh rates up to 1152×900 pixels at 76 Hz and 1280×1024 pixels at 76 Hz. Both are single-slot, 8-bit color, single-buffered cards and are compatible with all SPARCstations. The TGX100, with 1 Mbyte of RAM, costs $1595; the TGX120, with 2 Mbytes, costs $2200. **Integrix Inc**, Newbury Park, CA. (805) 375-1055.
Circle No. 343

CD-ROM travels with portable PCs. The Reno Personal CD-ROM Player, a double-speed, external CD-ROM drive for computers or audio CDs operates with NiCd batteries or an ac power source. As a CD-ROM player, the drive connects to a PC via a SCSI connection. The package includes the player and a docking connector. Features include data-transfer rates up to 306 kbps, access speeds of <180 msec, and a 64-kbyte buffer memory. $399 to $549. **Media Vision**, Fremont, CA. (510) 770-8600.
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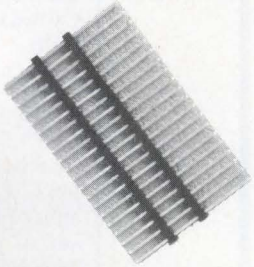

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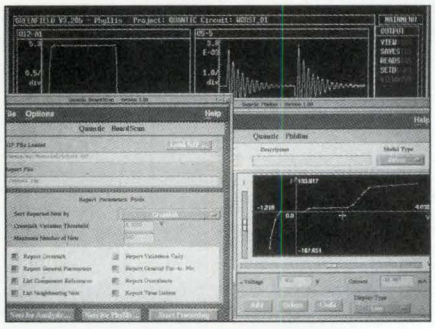
CIRCLE NO. 28

ELECTRONIC DESIGN AUTOMATION



Signal-integrity-analysis tools suits board-level designs. BoardSpecialist includes the BoardScan and PCB Greenfield signal-integrity tools. BoardScan, a pc-board screener, identifies critical nets violating specified design limits. PCB Greenfield is a transmission-line-verification tool for signal integrity, crosstalk, and time delays. BoardSpecialist Plus adds a third tool, Phidias, to the package. Phidias is a software tool for creating behavioral models used by BoardScan and PCB Greenfield from component-data-book information. BoardSpecialist costs $31,500, and BoardSpecialist Plus costs $37,000. **Quantic Laboratories Inc**, Winnipeg, Manitoba, Canada. (204) 942-4000. **Circle No. 414**

Generator automates library development. The Paradigm library tool set automates the development of the vendor's Paradigm XP and XP libraries from standard ASIC formats. The tool set includes three software packages: the VeriFE Verilog-to-Zycad format translator, the Libertee library compiler, and the Certifi library verifier. VeriFE costs $15,000, and Libertee comes bundled with Certifi for $15,000. **Zycad Corp**, Fremont, CA. (510) 623-4400. **Circle No. 415**

Math package is available on the Macintosh. Matlab Version 4 is now available for the Apple Macintosh. The software combines extensive computational features with 3-D object-oriented visualization capabilities. Prices start at $1695. **The MathWorks**, Natick, MA. (508) 653-1415. **Circle No. 417**

Low-cost automatic place-and-route IC-layout tool provides faster and denser layouts. According to the manufacturer, L-Edit/SPR Version 4.0 provides layout-optimization routines that offer an order of magnitude improvement in layout time and up to 25% higher layout densities than the previous version. The software also accommodates designs with twice as many elements as the old software. L-Edit/SPR Version 4.0 starts at $995 for PCs, $1495 for Macintosh systems, and $2995 for Unix workstations. **Tanner Research**, Pasadena, CA. (818) 792-3000. **Circle No. 416**

Viewer simplifies graphical debugging of Verilog designs. The RTL-Spreadsheet viewer displays block diagrams of designs, including dynamic data values, as you run a simulation. The program comes with the company's Magellan software. Prices start at $1995. **System Science Inc**, Palo Alto, CA. (415) 812-1800. **Circle No. 418**

REVISIONS

ProCAD Advanced for Windows version 2.0 performs schematic capture and pc-board layout. Prices start at $320. **Interactive CAD Systems**, (408) 970-0852. **Circle No. 419**

Release 1.2 of MultiProx, Comdisco's multiprocessor code-development system, generates C code that runs 30% faster than the earlier version. Multiprox 1.2 costs $15,000. **Comdisco Systems**, (415) 574-5800. **Circle No. 420**

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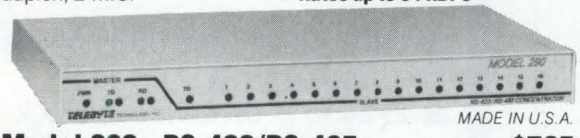

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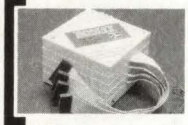

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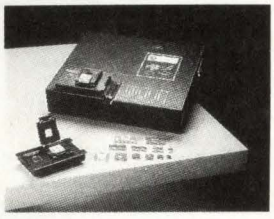

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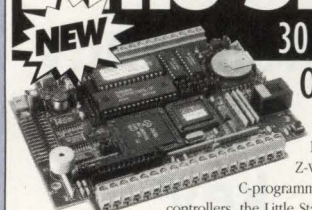

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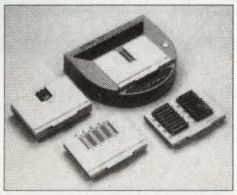

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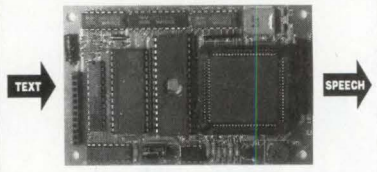

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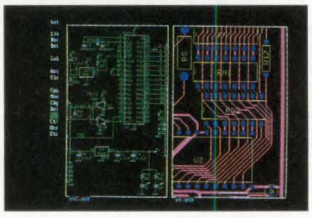

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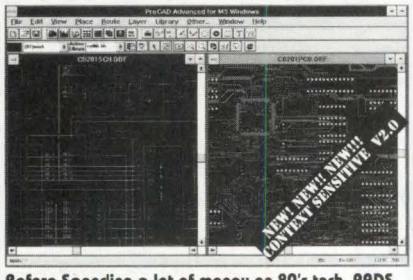

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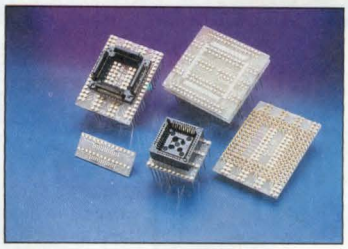

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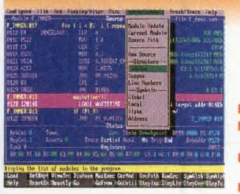

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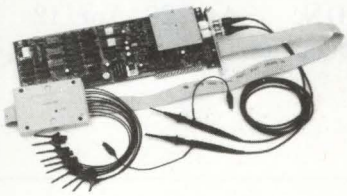

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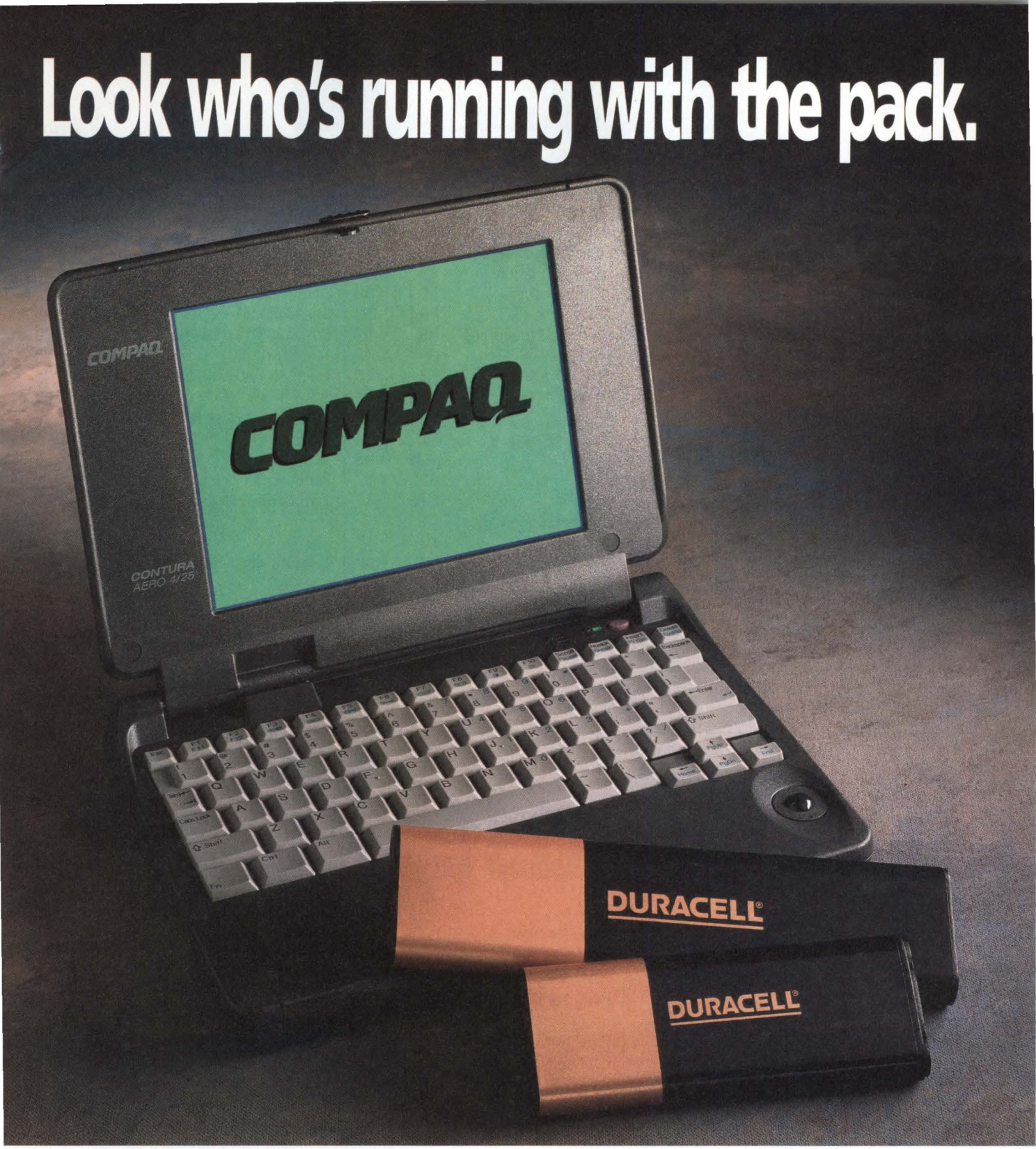

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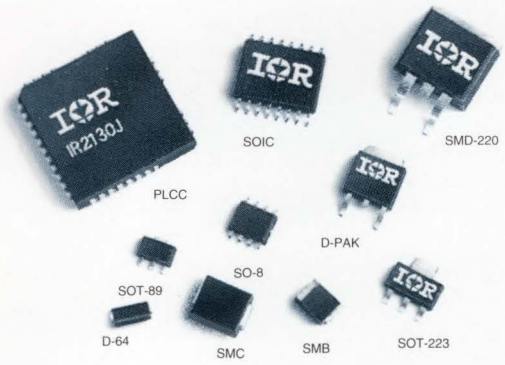

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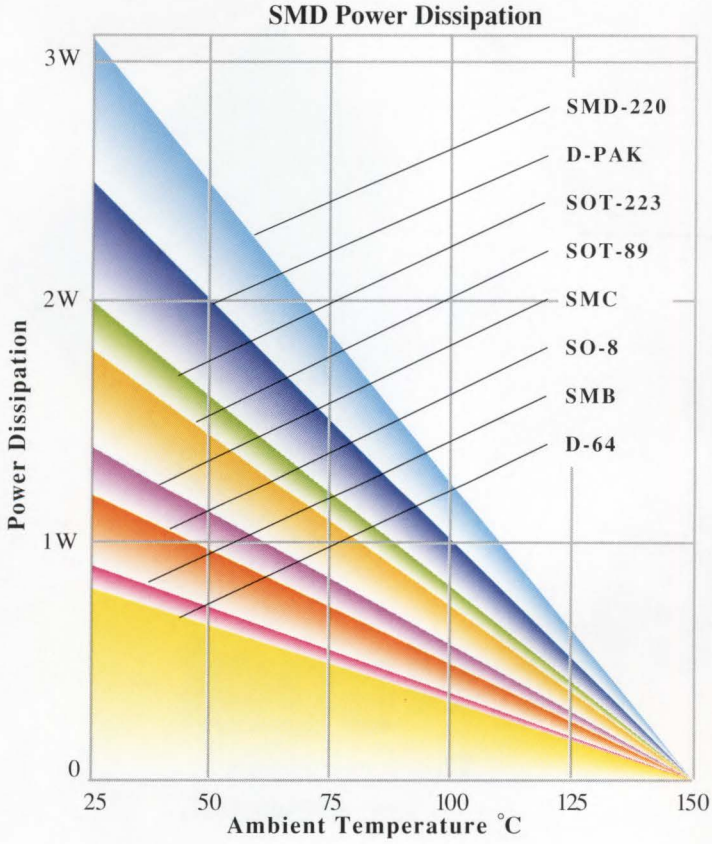

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Mechanical Dimensions

Size	L	W	H	ML (mtg)*	MW (mtg)*	WGT
200VA	3.750" 95.3 mm	4.203" 106.6 mm	3.720" 94.5 mm	3.250" 82.6 mm	2.800" 71.1 mm	6.22 lbs 2.82 kg
250VA	4.125" 104.8 mm	3.898" 99.0 mm	4.000" 101.6 mm	3.625" 92.1 mm	2.601" 66.1 mm	6.76 lbs 3.07 kg
300VA	4.125" 104.8 mm	4.223" 107.3 mm	4.000" 101.6 mm	3.625" 92.1 mm	2.915" 74.0 mm	7.80 lbs 3.54 kg
400VA	4.125" 104.8 mm	4.805" 122.0 mm	4.000" 101.6 mm	3.625" 92.1 mm	3.505" 89.0 mm	9.82 lbs 4.46 kg
650VA	5.250" 133.3 mm	4.430" 112.5 mm	4.800" 121.9 mm	4.500" 114.3 mm	3.415" 86.7 mm	14.83 lbs 6.73 kg
900VA	5.250" 133.3 mm	5.197" 132.0 mm	4.800" 121.9 mm	4.500" 114.3 mm	4.205" 106.8 mm	19.84 lbs 9.01 kg

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Mechanical Dimensions

Size	L	W	H	ML (mtg)*	MW (mtg)*	WGT
2000VA	7.500" 190.5 mm	5.600" 142.2 mm	6.560" 166.6 mm	5.750" 146.1 mm	4.350" 110.5 mm	41.3 lbs 18.71 kg
2750VA	7.500" 190.5 mm	6.230" 158.2 mm	6.560" 166.6 mm	5.750" 146.1 mm	4.980" 126.5 mm	48.0 lbs 21.77 kg
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