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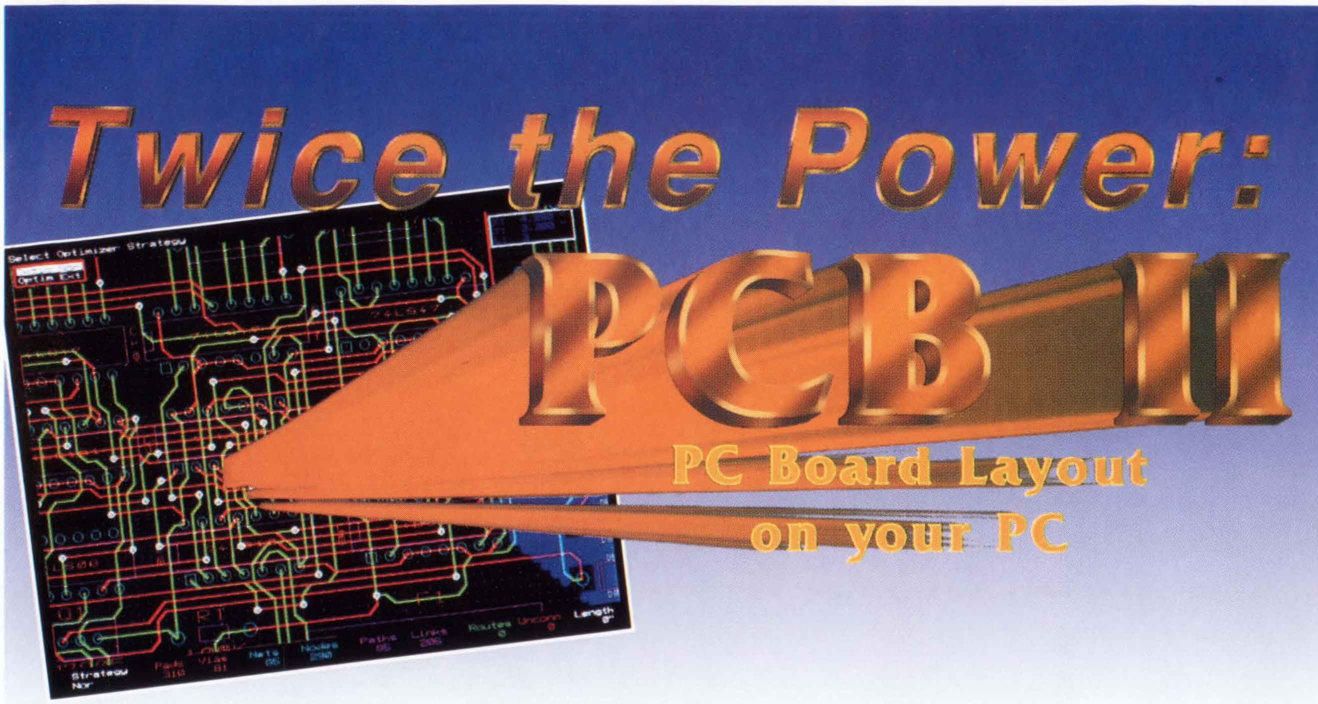
QUICKLOOK PAGE 97



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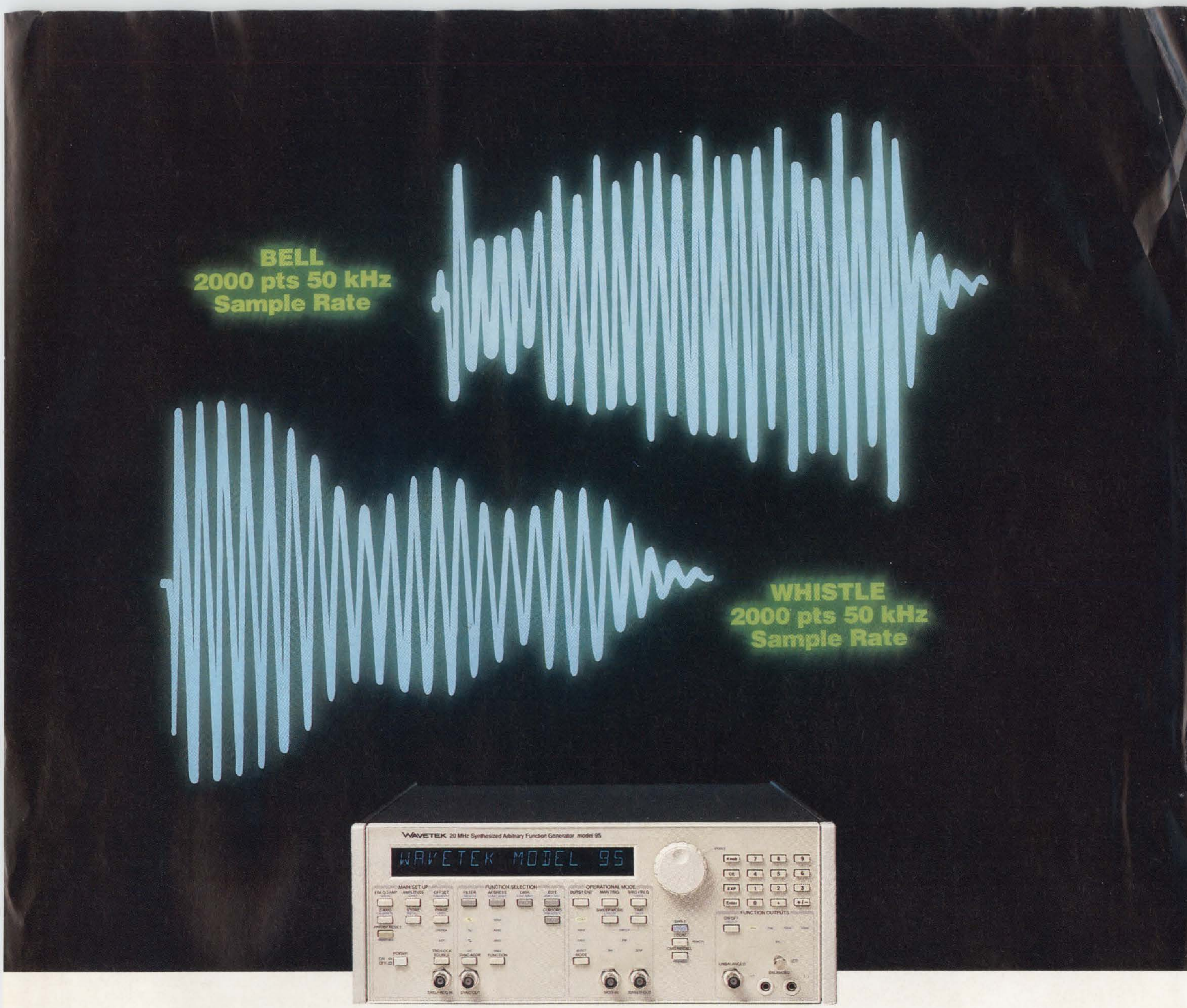

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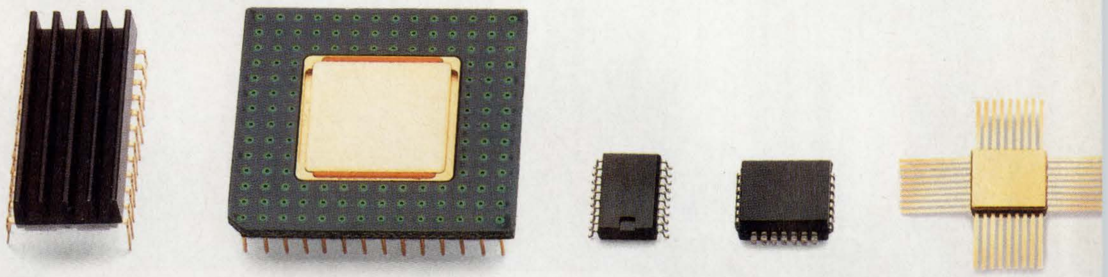

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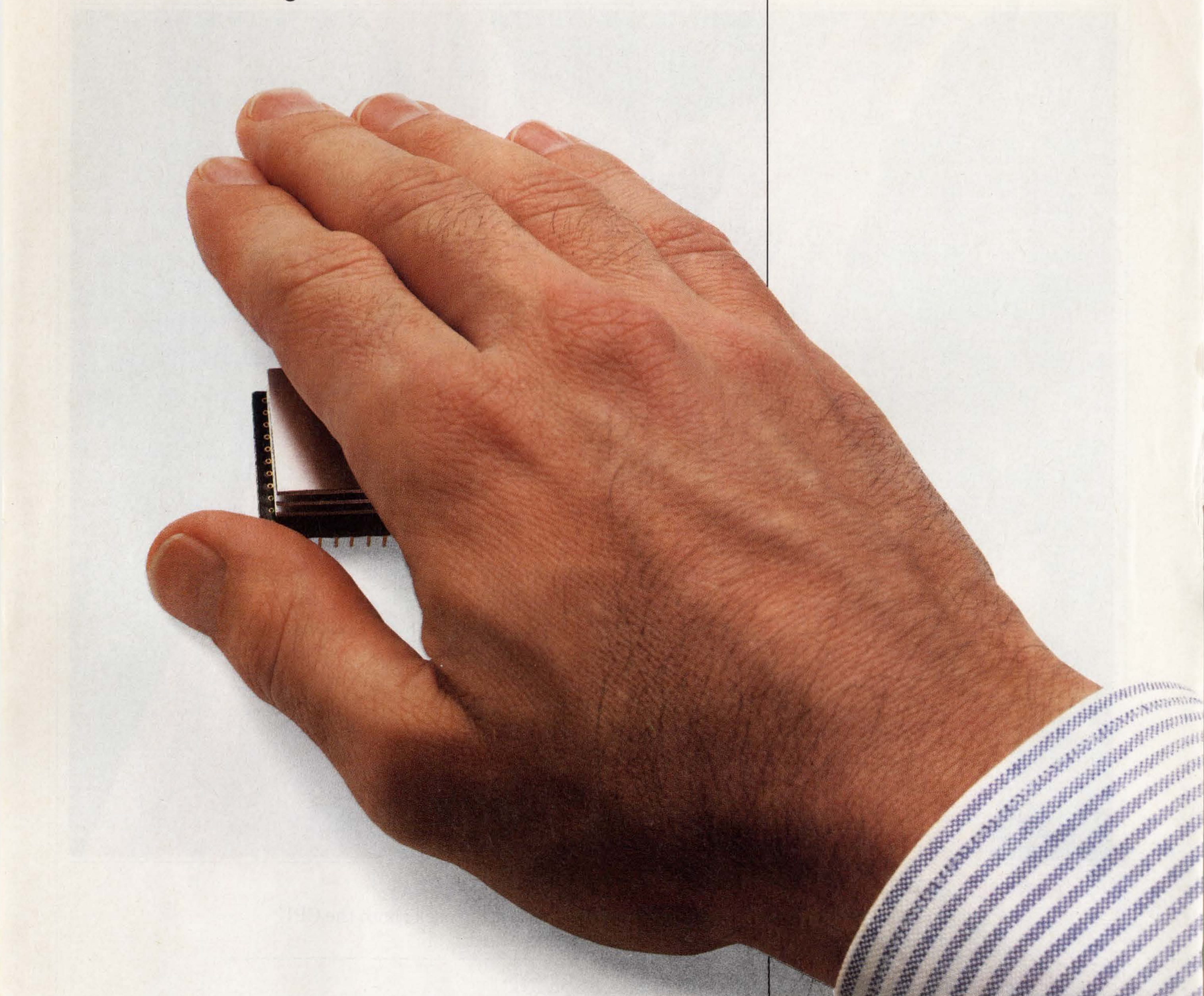

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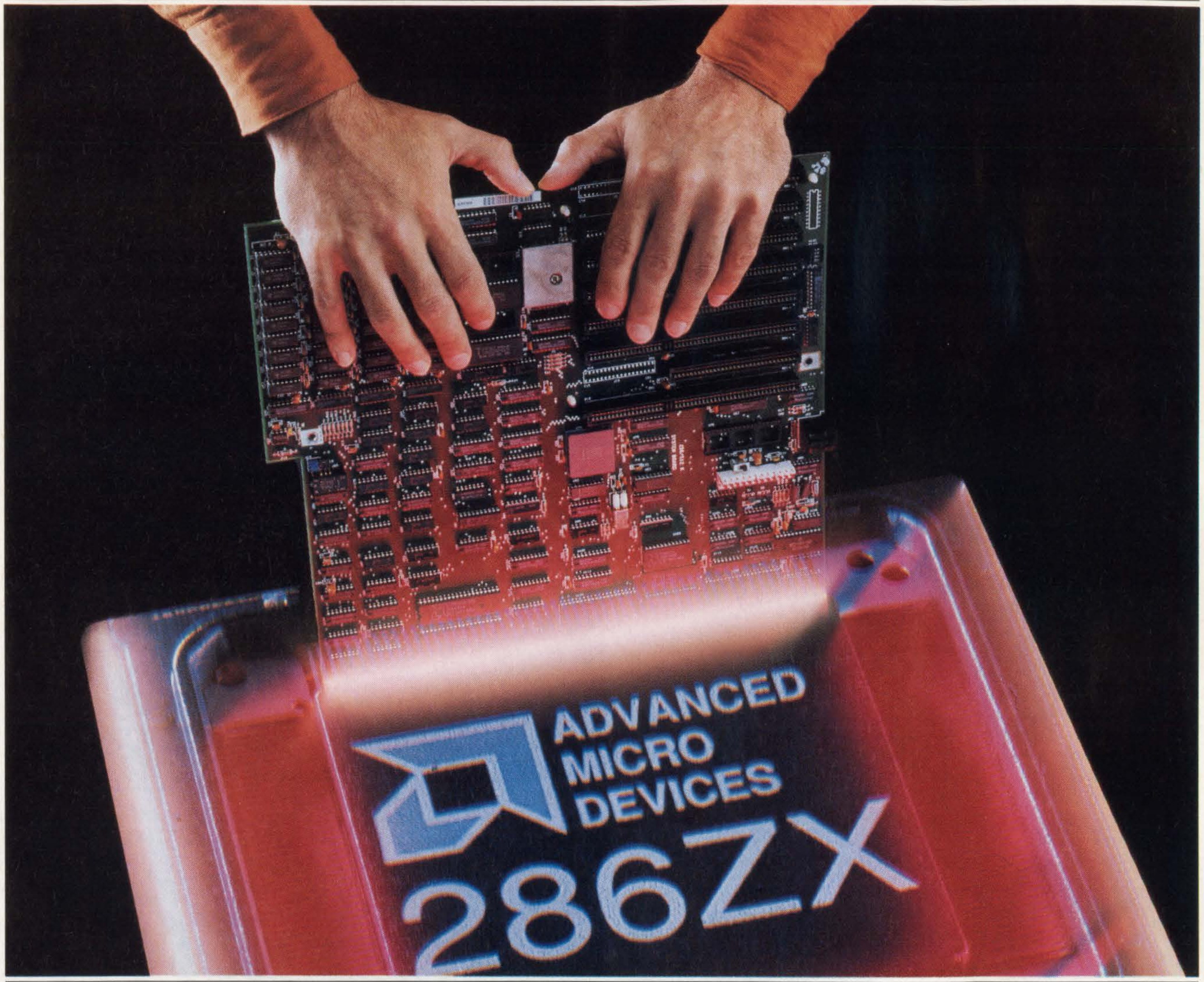

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- Special Report: Selecting design tools for PLD-based systems
- Career Special: Results and analysis of Electronic Design's annual salary survey
- Avoiding system pitfalls in PLD-based systems
- Understanding EISA bus-cycle translations
- Designing embedded controllers with new 386-based modules
- Pease Porridge: What's all this noise stuff, anyhow? (Part II)
- A new image-processing chip set offers expanded options
- A preview of the Buscon East show

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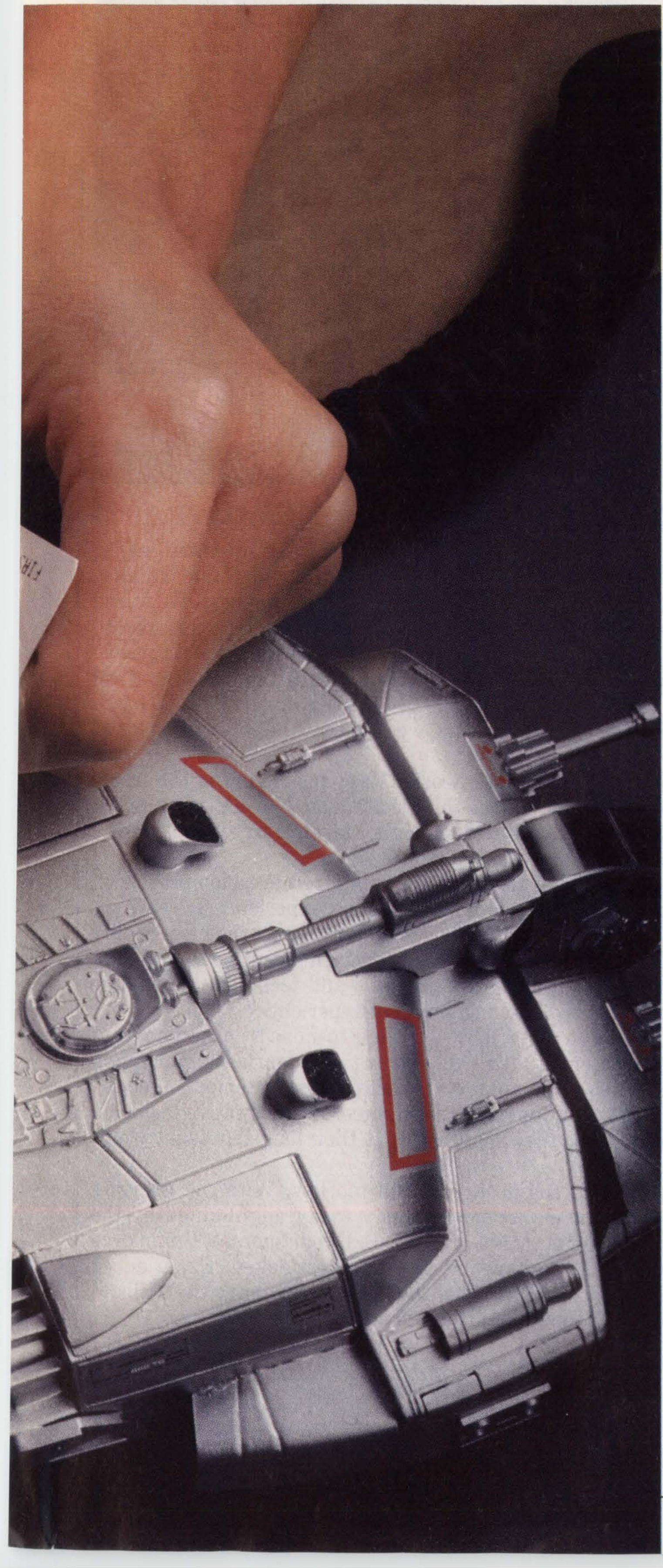

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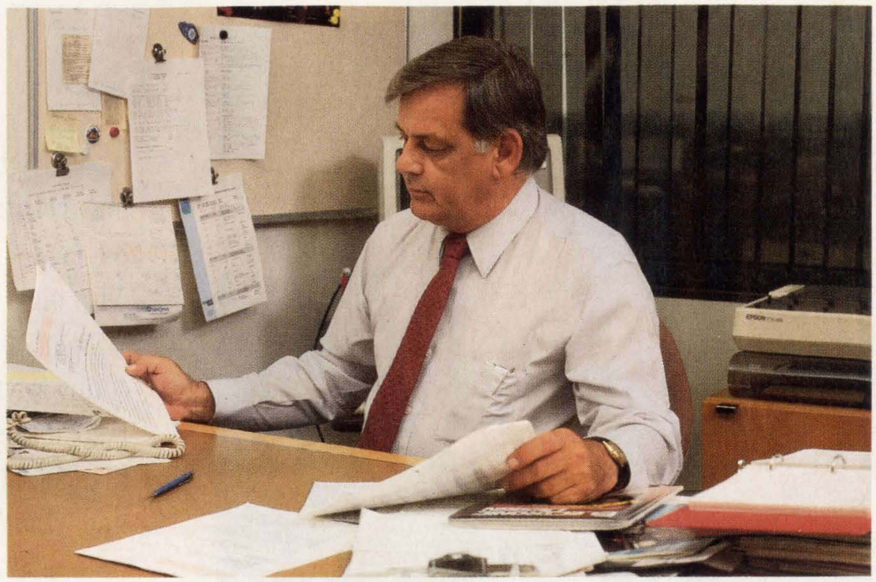
Where quality starts with fundamentals

EDITORIAL



LET'S RAISE THE CEILING

In our October 11 issue, we will publish the results of our annual reader survey on EE salaries. Don't miss it, we're sure that you'll find it makes for interesting reading. Some findings sparked our interest: We found that the average salary among the 350 or so readers who responded to our survey is $51,646, and the average reader has about 14 years of engineering experience. What's intriguing, however, is that many responses confirm the generally held belief that engineers face a definite salary ceiling. Averaging the numbers cited by the respondents, we find that the ceiling resides at about $59,500.

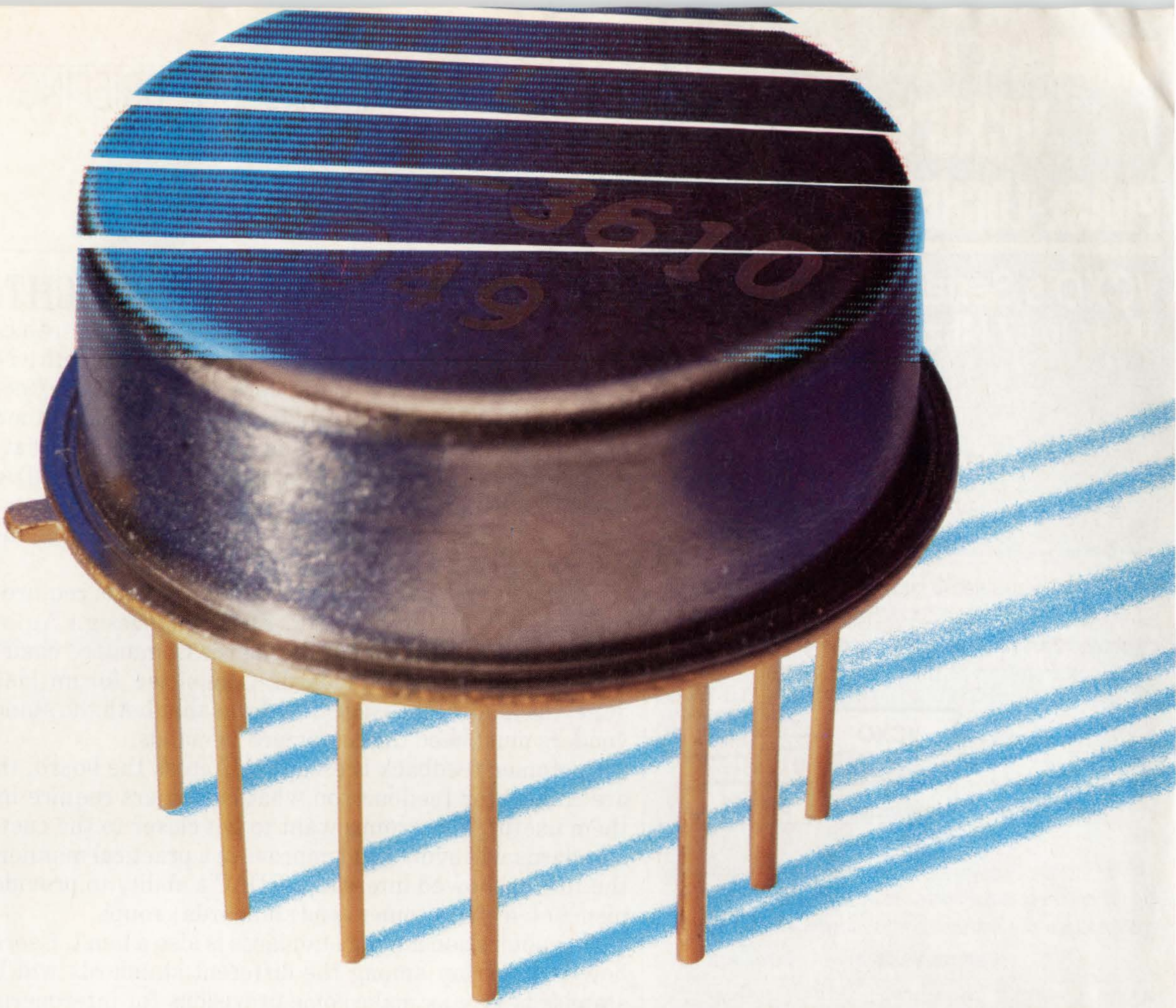
$59,500 isn't a bad salary in today's world. Many people in the U.S. raise families on salaries topping out at one-third that much. Nevertheless, many other professionals have earnings at much higher levels. First-year lawyers, for example, can easily command that salary level.

These numbers clearly illustrate the heavy salary compression present in today's engineering world: Engineers with 14 years experience are earning about $51,600, while engineers with many more years of experience earn only about $8000 more. But does that salary carry enough incentive to motivate engineers to continue honing their design skills and technical knowledge while they put in their years of gaining practical experience?

One way to break through that $59,500 barrier is to move from engineering into marketing or management. It's true that both the marketing and management functions in today's complex electronics industry demand a technical background. But why continue to force engineers with creative technical talent into such roles just so they might improve their long-term salary outlook?

Salaries for experienced engineers are still too low. With the growing emphasis on quality in the electronics industry today, highlighted by the growing respect for, and importance of, the U.S. Department of Commerce Malcolm Baldrige Awards, perhaps one angle is overlooked: Experienced engineers, more than any other group within a company, have the skills to achieve total quality. And they should be paid accordingly.

Stephen E. Scrupski
Editor-in-Chief



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1.5	0.32	3.0	0.4	9.0	0.6	15.0	0.6
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2.5	0.32	5.0	0.5	13.0	0.6	25.0	0.7
3.0	0.4	6.0	0.5	16.0	0.6	30.0	0.7
3.5	0.52	7.0	0.7	19.0	0.9	35.0	1.0

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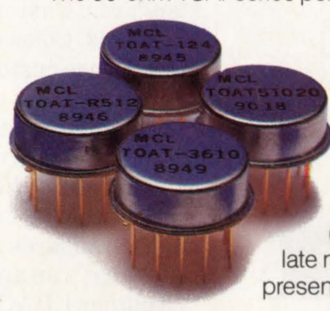

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THE CUSTOMER IS ALWAYS RIGHT

LISA MALINIAK
CAE EDITOR

There's no doubt that customers want electronic-design-automation tool standards. Competitiveness is making users more dependent on effective design tools. And for tools to work together effectively, there must be standards. In addition, creating and adopting these standards must be quicker. EDA tools are changing rapidly, as are hardware platforms. Therefore, the standards must keep pace with the advances in EDA technology.

"Nothing speaks louder than the customer's requirements," states Mitch Weaver, Electronic Design Automation Companies (EDAC) Standards Committee chairman. At the EDAC Standards Committee forum last June, the loudest message heard was that both the standards bodies and the vendors must heed the customers' demands.

Customer feedback is essential: Across the board, the standards groups are calling for feedback on what customers require in standards to make them useful. The groups want to get closer to the customer to ensure that standards will evolve and improve in a practical manner. Moreover, those at the forum showed interest in EDAC's ability to provide a feedback mechanism between customers and standards groups.

Harmonization among standards is also a must. Users are concerned over how the overlap among the different standards will be reconciled. While standards groups make some provisions for interoperability between standards, no one entity exists that's responsible for overall harmonization. Again, those at the forum showed an interest in seeing EDAC play a role in facilitating overall harmonization.

The EDAC forum consisted of standards bodies, vendors, and users. Among the standards represented were the CAD Framework Initiative (CFI), Electronic Design Interchange Format (EDIF), VHSIC hardware description language (VHDL), and Initial Graphics Exchange Specification (IGES) and Product Data Exchange Specification (PDES).

EDAC plans to act on its findings from the 1990 forum. It foresees creating a document that would represent customer requirements. The document would state, for each standards organization, what's needed to speed the adoption of its standard. This document would be written from the customers' perspective, not from EDAC's view.

EDAC must know how it can improve the rate of adopting standards. First, a better method of educating users on the importance of each different standard is required. All members agree that standards are important, but many don't know the difference between the standards.

Significant progress has been made within the last year, especially with EDIF and VHDL. It resulted from the failures in the marketplace in terms of standards. Customers have complained about their failings due to a lack of standards. Consequently, the standard creation-adoption process has accelerated since customers got involved.

A key element that's missing among standards organizations is communication with the customers. None of the standards bodies have an access to customers. The role of a trade association, such as EDAC, isn't only to educate, but also to influence. EDAC feels it can influence the standards associations by voicing customer requirements. It can also affect the user base as to where standards are and aren't appropriate. Lastly, it can influence vendors as to what's an appropriate model of business.

Another EDAC Standards Committee forum will be held in 1991. A couple of hours, however, isn't enough time to cover every problem concerning design-automation tool standards. Therefore, next year's forum will probably focus on specific topics.

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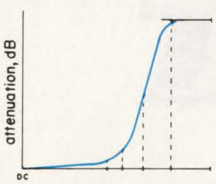
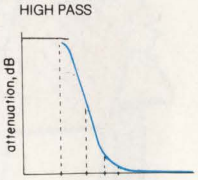
LOW PASS



low pass dc to 1200MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Max.	(loss>40dB) Max.	Min.	VSWR pass-band typ.	stop-band typ.	PRICE $ Qty. (1-9)
PLP-10.7	DC-11	14	19	24	200	1.7	18	11.45
PLP-21.4	DC-22	24.5	32	41	200	1.7	18	11.45
PLP-30	DC-32	35	47	61	200	1.7	18	11.45
PLP-50	DC-48	55	70	90	200	1.7	18	11.45
PLP-70	DC-60	67	90	117	300	1.7	18	11.45
PLP-100	DC-98	108	146	189	400	1.7	18	11.45
PLP-150	DC-140	155	210	300	600	1.7	18	11.45
PLP-200	DC-190	210	290	390	800	1.7	18	11.45
PLP-250	DC-225	250	320	400	1200	1.7	18	11.45
PLP-300	DC-270	297	410	550	1200	1.7	18	11.45
PLP-450	DC-400	440	580	750	1800	1.7	18	11.45
PLP-550	DC-520	570	750	920	2000	1.7	18	11.45
PLP-600	DC-580	640	840	1120	2000	1.7	18	11.45
PLP-750	DC-700	770	1000	1300	2000	1.7	18	11.45
PLP-800	DC-720	800	1080	1400	2000	1.7	18	11.45
PLP-850	DC-780	850	1100	1400	2000	1.7	18	11.45
PLP-1000	DC-900	990	1340	1750	2000	1.7	18	11.45
PLP-1200	DC-1000	1200	1620	2100	2500	1.7	18	11.45

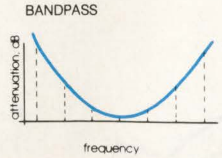
HIGH PASS



high pass dc to 2500MHz

MODEL NO.	PASSBAND, MHz (loss <1dB) Min.	Min.	fco, MHz (loss 3db) Nom.	STOP BAND, MHz (loss>20dB) Min.	(loss>40dB) Min.	VSWR pass-band typ.	stop-band typ.	PRICE $ Qty. (1-9)
PHP-50	41	200	37	26	20	1.5	17	14.95
PHP-100	90	400	82	55	40	1.5	17	14.95
PHP-150	133	600	120	95	70	1.8	17	14.95
PHP-175	160	800	140	105	70	1.5	17	14.95
PHP-200	185	800	164	116	90	1.6	17	14.95
PHP-250	225	1200	205	150	100	1.3	17	14.95
PHP-300	290	1200	245	190	145	1.7	17	14.95
PHP-400	395	1600	360	290	210	1.7	17	14.95
PHP-500	500	1600	454	365	280	1.9	17	14.95
PHP-600	600	1600	545	440	350	2.0	17	14.95
PHP-700	700	1800	640	520	400	1.6	17	14.95
PHP-800	780	2000	710	570	445	2.1	17	14.95
PHP-900	910	2100	820	660	520	1.8	17	14.95
PHP-1000	1000	2200	900	720	550	1.9	17	14.95

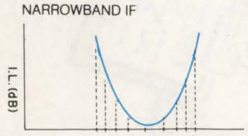
BANDPASS



bandpass 20 to 70MHz

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz (loss <1dB) Max. F1	Min. F2	STOP BAND, MHz (loss > 10 dB) Min. F3	Max. F4	(loss > 20 dB) Min. F5	Max. F6	VSWR 1.3:1 typ. total band MHz	PRICE $ Qty. (1-9)
PIF-21.4	21.4	18	25	4.9	85	1.3	150	DC-220	14.95
PIF-30	30	25	35	7	120	1.9	210	DC-330	14.95
PIF-40	42	35	49	10	168	2.6	300	DC-400	14.95
PIF-50	50	41	58	11.5	200	3.1	350	DC-440	14.95
PIF-60	60	50	70	14	240	3.8	400	DC-500	14.95
PIF-70	70	58	82	16	280	4.4	490	DC-550	14.95

NARROWBAND IF



narrowband IF

MODEL NO.	CENTER FREQ. MHz F0	PASS BAND, MHz I.L. 1.5dB max. F1-F2	STOP BAND, MHz I.L. > 20dB F5	F6	STOP BAND, MHz I.L. > 35dB F7	F8-F9	PASS-BAND VSWR Max.	PRICE $ Qty. (1-9)
PBP-10.7	10.7	9.5-11.5	7.5	15	0.6	50-1000	1.7	18.95
PBP-21.4	21.4	19.2-23.6	15.5	29	3.0	80-1000	1.7	18.95
PBP-30	30.0	27.0-33.0	22	40	3.2	99-1000	1.7	18.95
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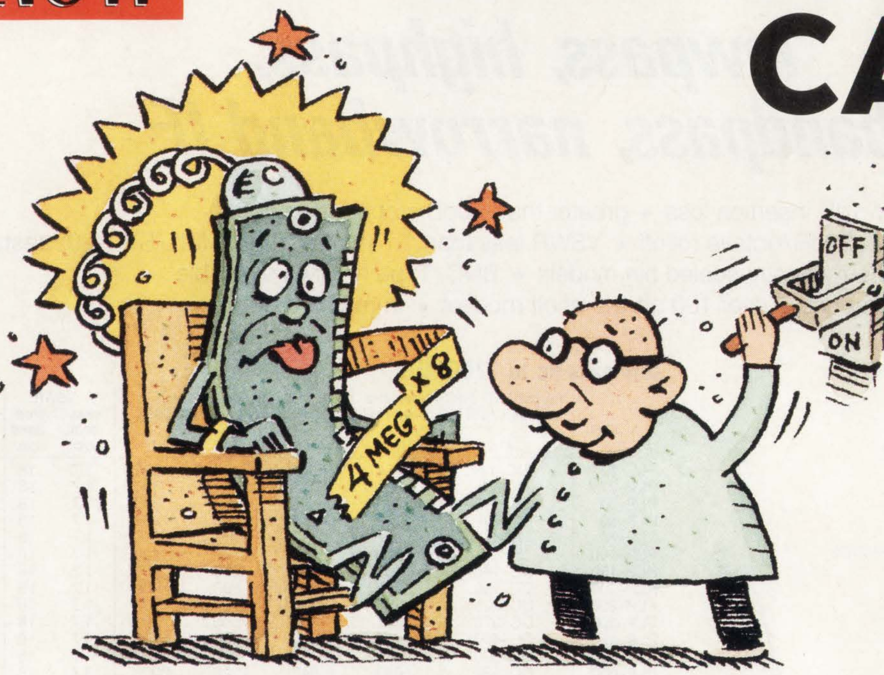

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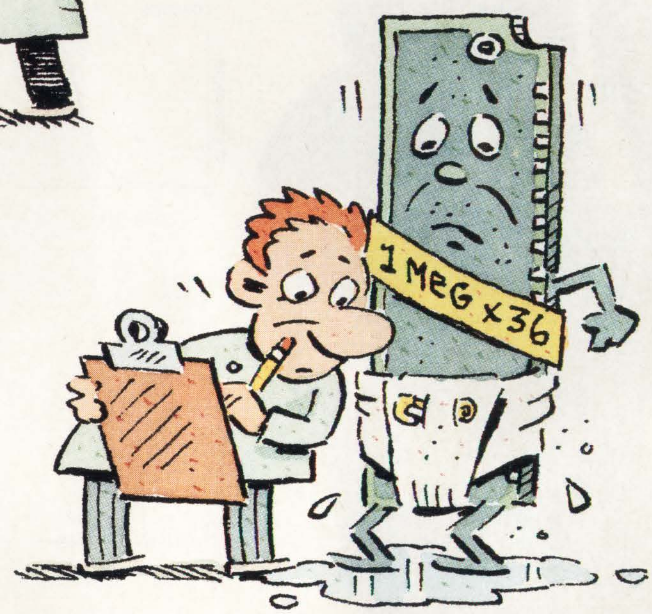
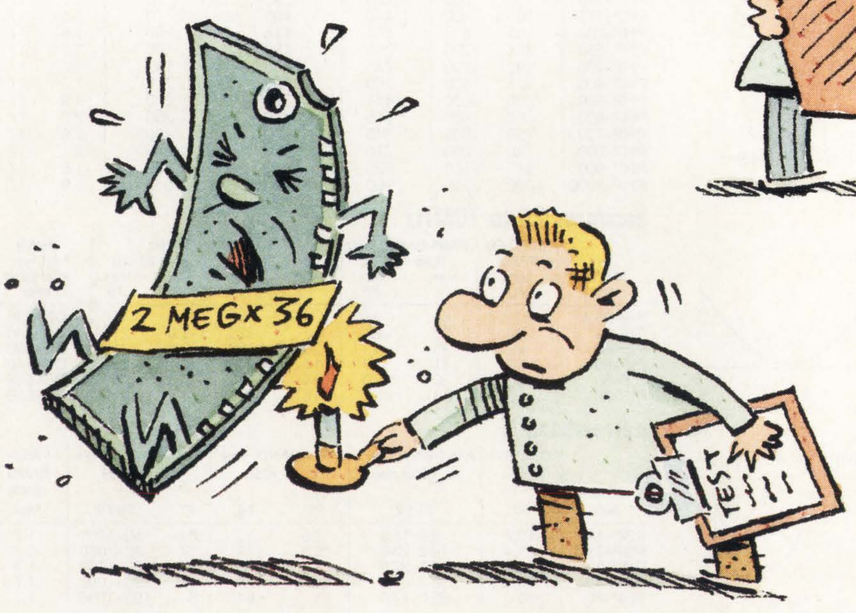


FLAMMABILITY

On flammability, our module people take great pains to assure that our products meet standards. As a result, we guarantee that every Samsung memory module meets or exceeds the 94V-O Underwriters Laboratory flame classification.



LEAKAGE

Even in the era of the 4-meg DRAM, there's still such a thing as a module with leaky pins. Many manufacturers just don't inspect for leakage. You guessed it, our team does comprehensive tests. All pins on all modules are 100% tested to the data sheet leakage specification.

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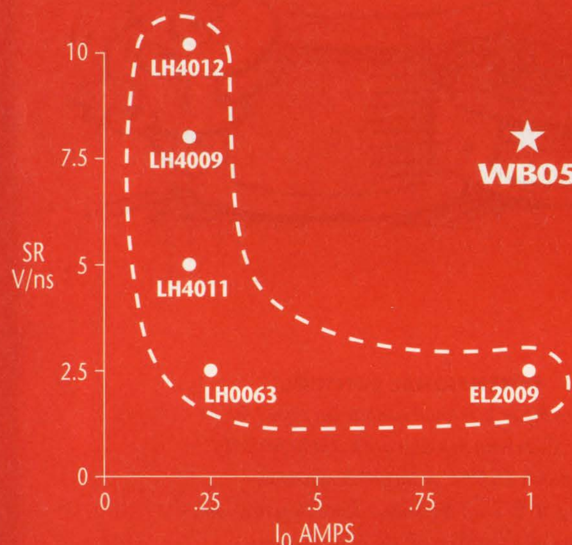

WA01

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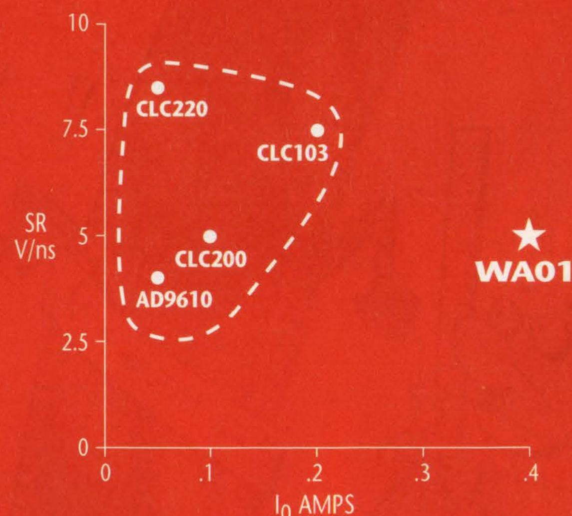

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CIRCLE 165

InP HEMT Sets Record, Operates At 260 GHz

The fastest high-electron mobility transistor (HEMT) to date, with an operating frequency of 260 GHz at room temperature, has been crafted in indium-phosphide. The device, created with electron-beam lithography and Varian's molecular-beam epitaxy system, hails from Varian Associates Inc. research laboratories, Palo Alto, Calif. The InP HEMTs have gate widths of less than 0.1 μm, which are formed in lattice-matched indium-aluminum arsenide and indium-gallium-arsenide epitaxial layers on a semi-insulating InP substrate. The actual transistor structure is based on a low-conductance drain that the company conceptually described in research papers at this past year's IEEE Indium Phosphide and Related Materials Conference and at the 48th Device Research Conference. Because the transistor is based on InP, a popular material for laser diodes, photo detectors, and many other opto-electronic applications, the merger of optical elements and HEMT circuitry will most likely follow. *DB*

Conductive Epoxies Seen As Solder Substitute

Isotropic conductive epoxies hold promise as a fluxless, low-temperature interconnection material for chip attachment. The epoxies hurdle many of the limitations of tin-lead solder for surface-mounted assemblies. These include package cracking from high-temperature reflow, potential contamination from fluxes, environmental difficulties with CFCs, solder bridging, and fatigue failures. In a paper presented at this year's Society for Advancement of Materials and Process Engineering Conference, Art Burkhart of Dexter Electronic Materials, Industry, Calif., suggests that isotropic conductive epoxies can greatly simplify process technology by eliminating up to 50% of the steps in chip attachment. *DM*

CAE, Database Companies Form Partnership

Digital Equipment Corp., Maynard, Mass., and Objectivity Inc., Menlo Park, Calif., have established a joint development and marketing partnership for Objectivity/DB, an object-oriented database-management system. As part of the agreement, Digital will sublicense and distribute Objectivity/DB to end users. According to Digital, the object-oriented database is a complementary solution to VAX Rdb/VMS, the company's relational-database product. Digital chose the Objectivity database because of the product's broad platform coverage and its open architecture. Both companies have committed to working together within standards organizations to advance evolving standards for object-oriented systems. Digital is a member of the Object Management Group (OMG), an international group of software and hardware companies focused on developing standards and guidelines for using an object-oriented database. *LM*

Silicon-On-Insulator Process Builds Diodes

Silicon-on-insulator (SOI) processes, which offer minimum-size ICs with galvanic-isolation and radiation-hardness properties, have been long on talk and short on practical applications. Now, however, Silicon General, Garden Grove, Calif., uses an SOI process to create a pair of arrays holding 7 and 8 silicon diodes. Each diode (anode and cathode) is completely isolated from its companions with silicon-dioxide rated at 400 V. The oxide is part of the original wafer, sandwiched between the silicon substrate and a layer of monocrystalline silicon in which the diodes are diffused. Each diode in the 7-diode SG6100 and the 8-diode SG6101 is rated at 75 V and 100 mA. Earlier versions of these devices were built using air-bridge techniques to obtain the isolation. Forward and reverse recovery times run 15 and 5 ns maximum, respectively. The arrays, rated for military temperatures, come in 14- and 16-pin ceramic DIPs and flat packs. High-volume pricing starts at $20.25 for each array. For additional information, call (714) 898-8121. *FG*

High-Power Lasers Make Efficient X-Ray Source

Using high-efficiency, diode-pumped solid-state lasers as a source of X-rays for a deep submicron lithography system promises to improve lithography-system performance and throughput. The work is part of a joint development between Hampshire Instruments Inc., Rochester, N.Y. and McDonnell Douglas, St. Louis, Mo. It will focus on adapting McDonnell Douglas' high-power lasers developed for military applications to Hampshire Instrument's commercial X-ray lithography system. The diode-pumped laser increases efficiency and power by about 250% over a standard neodymium solid-state laser pumped by arrays of flash lamps. Higher laser power translates into a stronger X-ray source, and thus a shorter exposure time per wafer and a higher overall wafer throughput. Though the agreement runs for five years, Hampshire expects to have prototypes ready sooner. *DB*

SYNTHESIS ACQUISITION FILLS OUT ASIC TOOLSET

With the procurement of logic-synthesis technology, the completion of GenRad Inc.'s ASIC toolset has been realized. The Concord, Mass.-based company bought the technology from Aptor S.A., Grenoble, France. GenRad will mesh the logic-synthesis tool with its System HILO simulation tools for a top-down design environment. Plans for the synthesis software, which will be announced later this year, include support for both the GenRad hardware description language (GHDL) and the VHSIC hardware description language (VHDL). *LM*

WINDOW COMPARATOR RESPONDS IN JUST 5 NS

Designers at Burr-Brown Corp., Tucson, Ariz., have succeeded in building a comparator IC—which takes a common-mode voltage (CMV) of ±12 V running off ±5-V rails—that responds in just 5 ns with 100 mV of overdrive. It was done by adding attenuators to the signal input and the two reference inputs of a typical high-speed window comparator. By limiting the supply voltage, the designers were able to build the comparator on a high-speed complementary linear process that could handle 12 V maximum between the rails. The input attenuator is RC-tuned (like an oscilloscope probe) to handle fast-rising waveforms, but the reference inputs are not. A buffer amplifier connects each attenuator to the comparators' inputs. Though designed for test-equipment pin-electronics, the IC can fill the bill on a wide range of threshold-detector, window-comparator applications previously limited by CMV restrictions. Each comparator provides complementary ECL outputs. In addition, latch-enable inputs permit sampling-type operation. In 16-pin DIPs and SOICs, pricing starts at $23.20 each in 100s. For additional information, call John Conlan, 1-(800) 548-6132. *FG*

HIGH-POWER SWITCHES, NEURAL NETS ADVANCE

A pair of developments from Sandia National Laboratories, Albuquerque, N.M., promise to improve machine vision and accelerate the speed of optical power switches. Both developments could eventually simplify some tough industrial and military control tasks. To enhance machine vision, one research group developed a neural network that can detect target objects placed at different angles or positions when mixed in among other objects. The network can process a camera image within seconds—an impossibility with previous neural networks. Most earlier systems typically focused on analyzing and identifying target features, such as a line or box, and thus could only handle rotations in two dimensions. The improved software and hardware enable the neural network to be both shift- and perspective-invariant so that the object's physical position and rotation make no difference during the recognition process. To teach the system, researchers use multiple training sets that contain the desired target viewed from different perspectives. When the system gives a wrong answer, the correct answer is supplied by the "teacher." The neural network can then compare the right and wrong answers in a process called back propagation to adjust itself in favor of the correct answer. The recognition software on the neural network requires about four seconds to identify the image. Similar software on a Sun 3 required about four hours.

In experiments to switch large amounts of electrical power under the control of an optical signal, another group of Sandia researchers developed a gallium arsenide photoconductive switch. The device, activated by light from an 850-W laser-diode array, could switch 8.5 MW. The switch also held off 55 kV until it was activated and delivered 470 A to a 38-Ω load. The optical pulse used to turn on the switch was just 21-ns wide. However, the fast switch required just 3.5 ns for the current pulse to reach its maximum value. The switch itself is built from a 1-in. disk of undoped GaAs. In the dark, the material is an insulator; but when exposed to intense light from the 850-W laser array, the disk rapidly becomes a conductor. Such a fast-acting switch could be a key element in such applications as ultra-wideband impulse radar, optically activated firesets for triggering explosives, pulsed power systems to supply energy to compact high-power accelerators, or as a fast-rise-time switch in electromagnetic-pulse testing. For details on the neural net, contact Mary Moya (505) 844-7031; for the optical switch, call Fred Zutavern (505) 845-9128. *DB*

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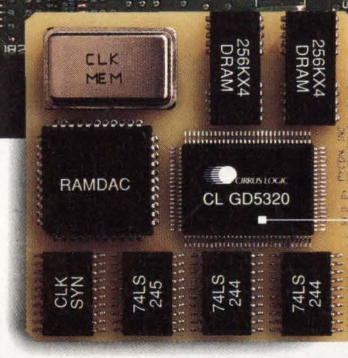

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90-GHz AlInAs/GaInAs Bipolar Transistors Build DC To 33-GHz Amp With 8.6-dB Gain

The world's widest-bandwidth dc amplifier with a 3-dB bandwidth of 33 GHz and a gain of 8.6 dB has been developed by Hughes Aircraft Co.'s Research Laboratories, Malibu, Calif. The circuit was described by Hughes' Joe Jensen at the recent Bipolar Circuits and Technology Meeting (BCTM) in Minneapolis (Sept. 17-18). The "true IC" is built with heterojunction bipolar transistors (HBTs) that feature an f_t (unity-gain or cutoff frequency) of 90 GHz and an f_{MAX} (maximum frequency of oscillation) of 70 GHz. The AlInAs/GaINAs (aluminum indium arsenide/gallium indium arsenide) transistors were grown on a semi-insulating GaP (gallium phosphide) substrate, using a molecular-beam-epitaxial (MBE) process.

The final circuit's development by Jensen and his associates at Hughes, as well as Mark Rodwell of the University of Calif. at Santa Barbara, shows that basic analog-circuit design still applies at millimeter wavelengths. The team started with a simple one-transistor common-emitter circuit employing both collector-to-base and emitter-circuit negative feedback with resistors R_f and R_e, respectively *(see the figure, part a)*. (Similar feedback was used throughout the amplifier's design.) It achieved a gain of 9.3 dB and a bandwidth of 14.4 GHz.

With a Darlington circuit, the bandwidth can go to 26 GHz at 10-dB gain *(see the figure, part b)*. The Darlington circuit supplies a low-impedance drive for the capacitive load that's represented by the base of the output transistor Q_2. In both the common-emitter and Darlington circuits, the Miller-multiplied collector-base capacitance represents the major factor limiting bandwidth.

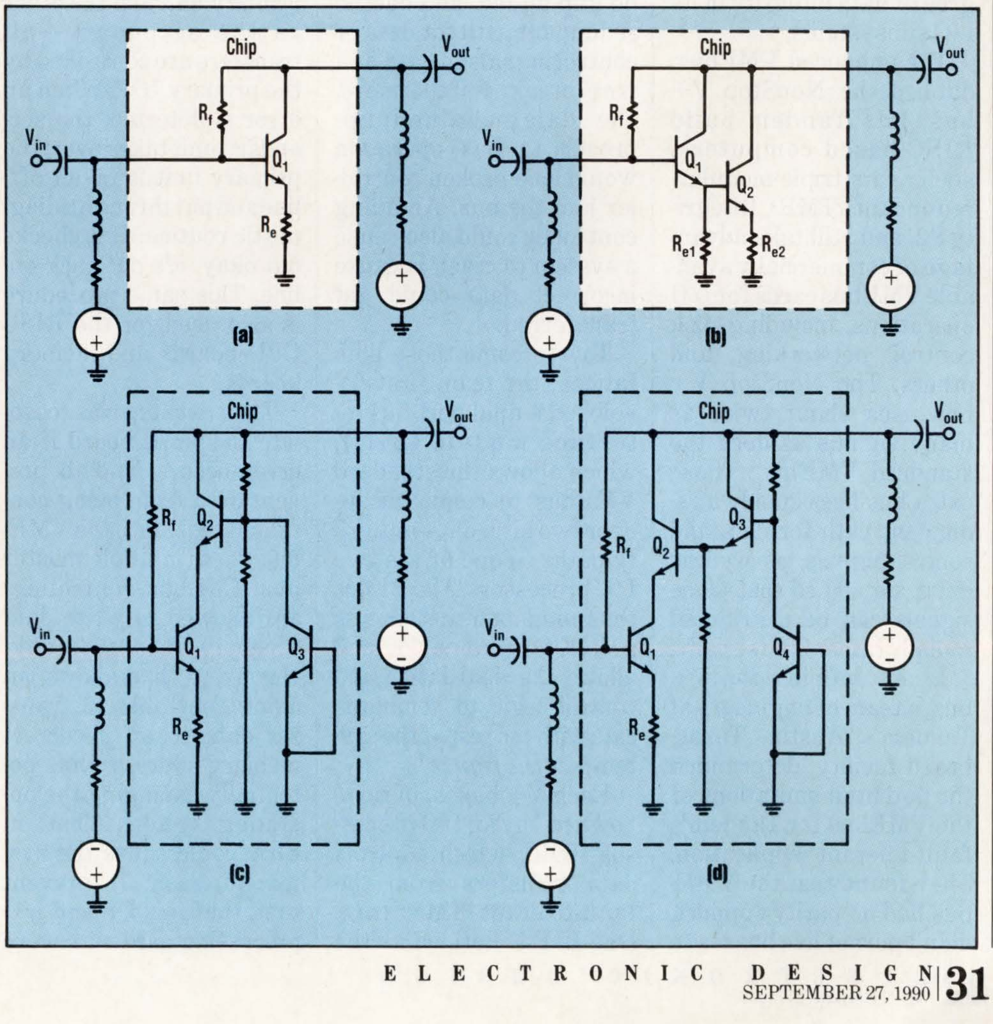
Moving to a cascode circuit reduces Miller multiplication and raises simulated bandwidth to 32 GHz *(see the figure, part c)*. This assumes the base of the upper transistor of the cascode (Q_2) can be at (bypassed to) ac ground. Because the process didn't provide the needed capacitors, the collector-base capacitance of an array of large transistors (represented by Q_3) was employed. However, its 0.35-pF capacitance was insufficient, and the resulting bandwidth was a mere 18.4 GHz.

The final circuit achieves the 33-GHz bandwidth with active biasing *(see the figure, part d)*. The bias-source buffer Q_3 reduces the source impedance that drives the base of Q_2, and the 0.35 pF supplied by Q_4 does the bypassing job. The amplifier output is biased at 4 V, the transistors in the cascode operate at 16 mA, and output power is about 5 dBm at the 1-dB gain-compression point (the point at which the output power ceases to increase linearly with input power).

The amplifier offers potential savings in cost, size, and weight over present techniques that use matched-impedance circuits with GaAs FETs whose transmission lines can occupy over 90% of the die. While such amplifiers achieve smaller bandwidths for a given transistor f_{MAX}, they take less die area and offer well-controlled performance that's set by internal feedback elements.

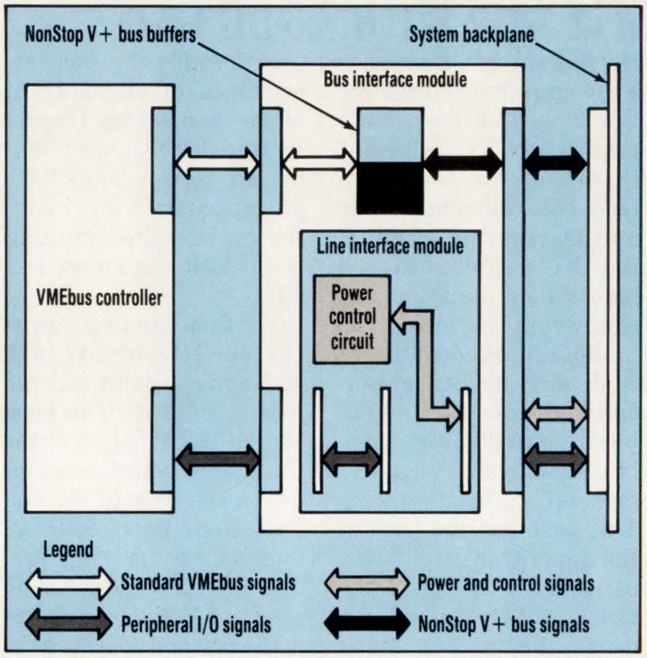
For more information, call Joe Jensen at (213) 317-5250.

FRANK GOODENOUGH



REDUNDANT BUSES, PARITY, RADIAL CONTROL BOOST RELIABILITY

Although such industrial system buses as VMEbus and Multibus offer reliable and sufficiently high performance for most applications, they're limited for applications that require non-stop operation should a board or part of the bus fail. There's no commercially available bus that can hold up under catastrophic system failures. That's why Tandem Computers Inc., Cupertino, Calif., developed an enhanced version of the VMEbus for its Integrity S2, a non-stop, fault-tolerant system. Integrity S2 enhances the VMEbus with redundancy and extra signals to add a high degree of data integrity in its I/O subsystems.



The enhanced VMEbus, dubbed the NonStop V+ bus, lets Tandem build RISC-based computers, such as its triple-modular-redundant (TMR) Integrity S2, and still take advantage of commercially available VMEbus cards for I/O operations, including disk control, networking, and others. The NonStop V+ bus uses about twice as many signals as does the standard VMEbus. Those extra bus lines supply a redundant path for data and control signals, as well as extra signals so that some signals can be distributed radially rather than serially.

When defining the V+ bus, a team of engineers at Tandem's Austin, Texas-based facility, determined the potential limitations of the VMEbus for Tandem's fault-tolerant application. They found that the VMEbus had no parity support, didn't permit live boards to be unplugged, and had no redundant path for data or control signals in case of a wire break. Furthermore, the daisy-chained approach to bus operation would let a broken controller jam the bus. An ailing controller could also cause a system to crash because incorrect data could get transferred.

To overcome those limitations, the team first developed a dual-port bus interface module (BIM), which allows the standard VMEbus to communicate over two high-data-integrity paths to one of the two I/O processors. The BIM is thus an adapter that accepts a VME card on one side, and allows the dual buses and control logic to communicate with the rest of the system *(see the figure)*.

Each V+ bus is, in turn, "owned" by an I/O processor (IOP), which controls data transfers from the fault-tolerant TMR core. One IOP is defined as the primary unit and the other as the secondary—all transfers are controlled by the primary IOP. When an error is detected, the secondary unit takes over; the primary unit is taken off-line and put through a diagnostic routine. If it checks out okay, it's put back on-line. This same procedure is also used for the RISC CPU boards and memory boards.

The next step was to isolate the VME board if an error occurs, and to prevent data from being contaminated. Since the VMEbus is a multiple-master bus, VMEbus controllers are allowed to write data directly into memory. However, that allows an ailing controller to transfer data to an in-correct memory address, thus potentially damaging the operating system. That, in turn, could cause the system to crash. To prevent that, the Unix OS and I/O processing hardware were enhanced to limit memory access of the VMEbus controllers to preauthorized areas.

Furthermore, to avoid the possible problem with daisy-chained Bus Request/Grant operations, the V+ bus uses a radial request scheme employing multiple request lines. The same approach was taken for the Interrupt line. Each BIM has its own "private" Request/Grant, Interrupt, and Reset lines.

Including a private reset line for each controller was a critical factor because the Integrity S2 must run without stopping. Consequently, it can't have one reset line controlling all boards—each board in the system must be controllable individually. Parity lines were also added to all data and address buses and to a number of control lines, especially those that control bus timing.

To allow hot removal of the boards, designers made the ground pins on the BIM substantially longer than the power pins. Upon insertion, ground contact will always be made before power reaches the card. And during card removal, power will be removed before the ground connection breaks. An inhibit circuit in the power-supply sense circuits on the BIM detects the board removal or insertion, and can quickly remove power from the card circuits on the supply. Furthermore, power to each of the VME cards is controllable on a slot-by-slot basis from both IOPs (both IOPs must agree to shut power to a card).

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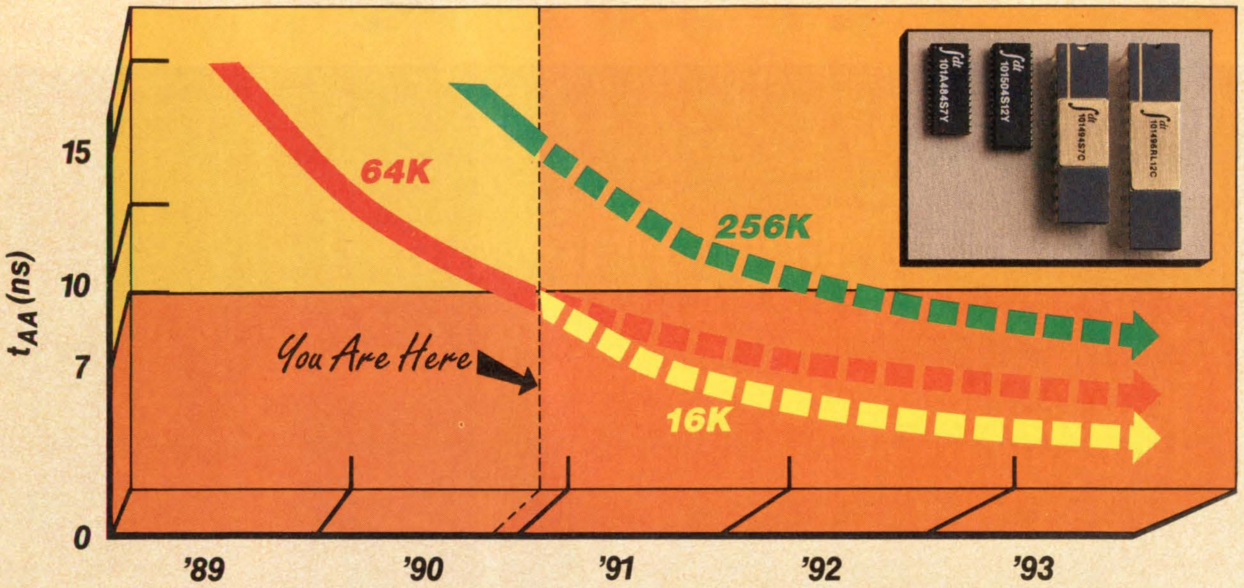

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IDT100490	64K (64K × 1) 100K ECL	8	320
IDT101490	64K (64K × 1) 101K ECL	8	420
IDT10494	64K (16K × 4) 10K ECL	7	700
IDT100494	64K (16K × 4) 100K ECL	7	500
IDT101494	64K (16K × 4) 101K ECL	7	700
IDT10496RL	64K (16K × 4) 10K STRAM	12	1000
IDT100496RL	64K (16K × 4) 100K STRAM	12	800
IDT101496RL	64K (16K × 4) 101K STRAM	12	1000
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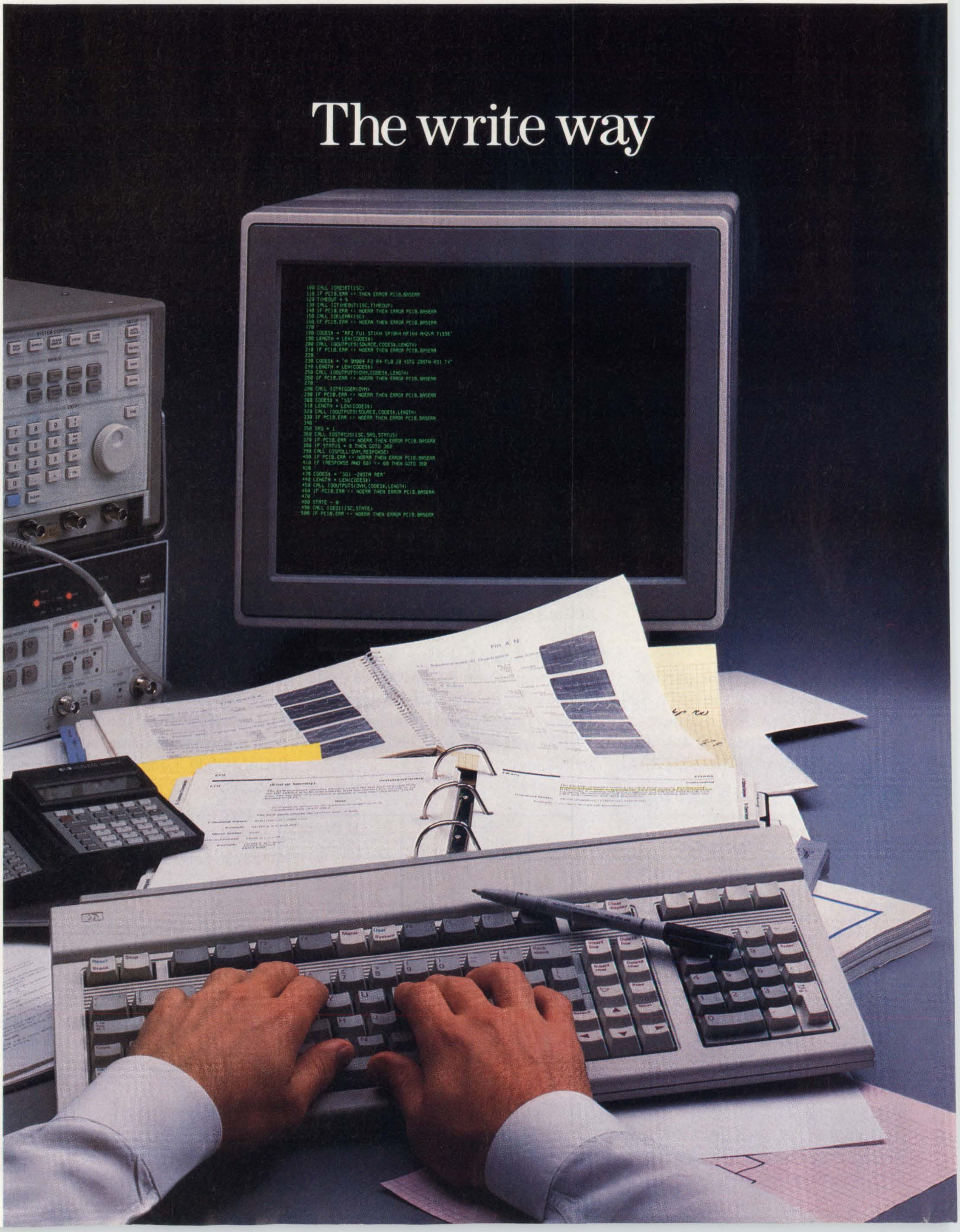

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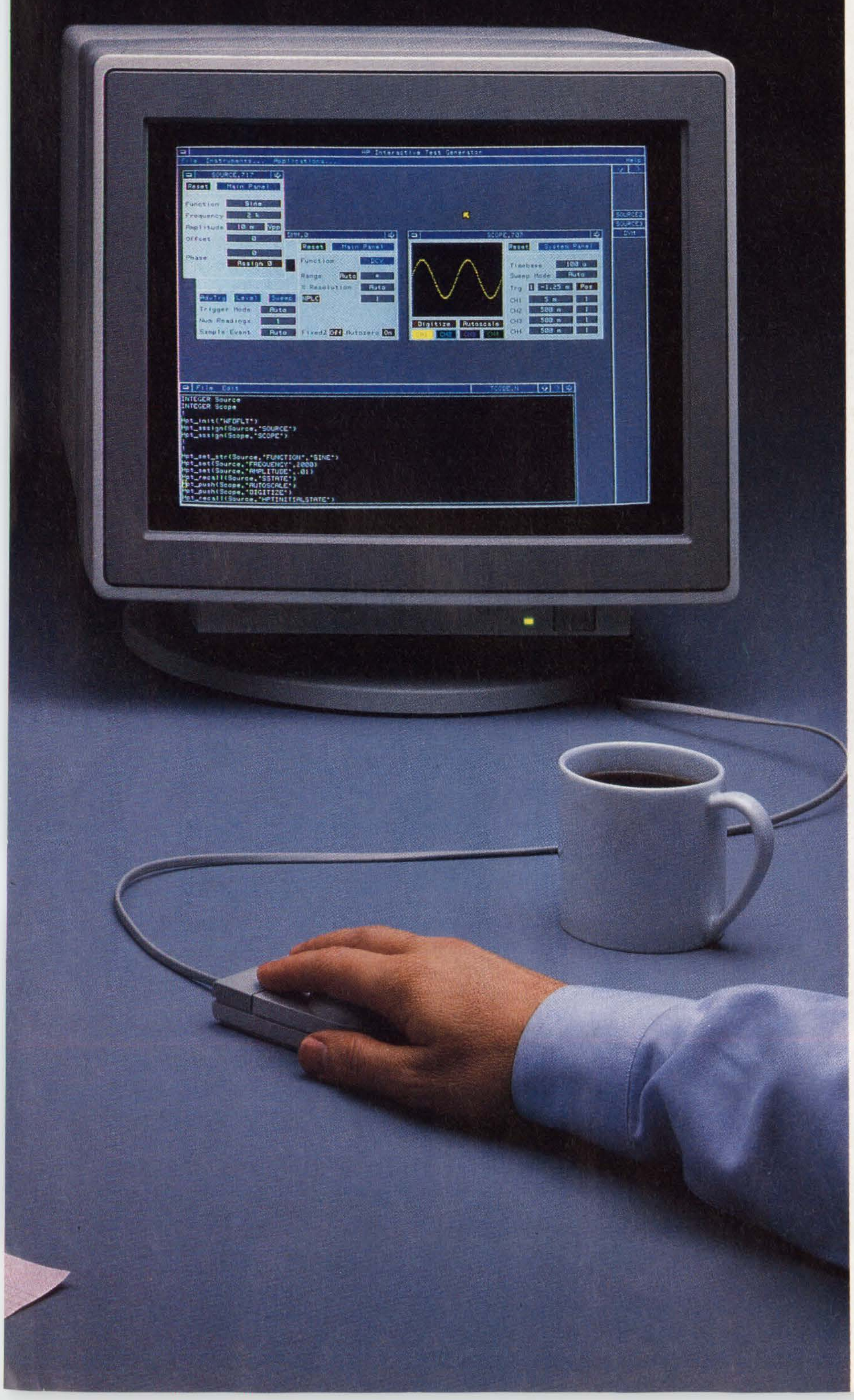

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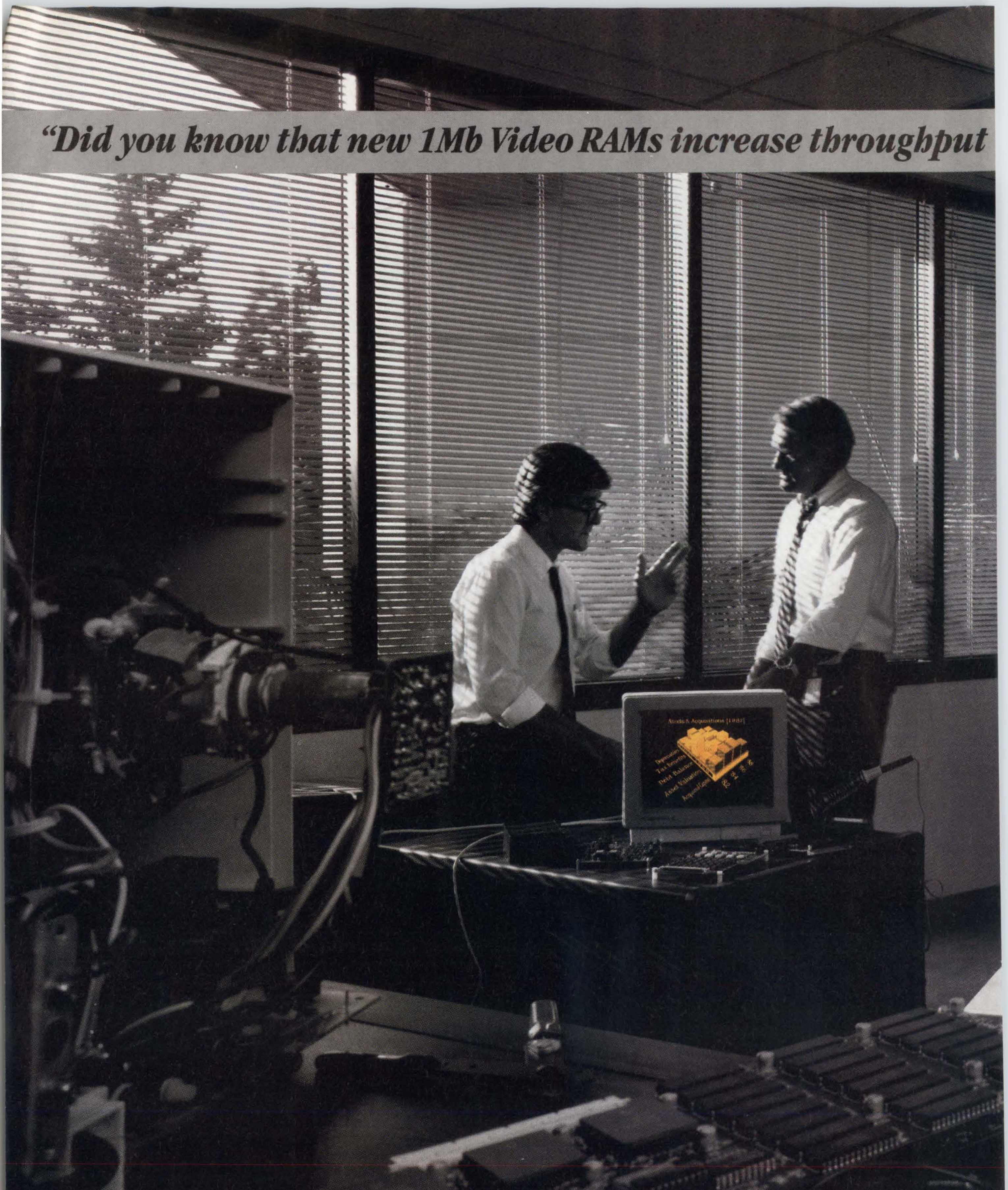

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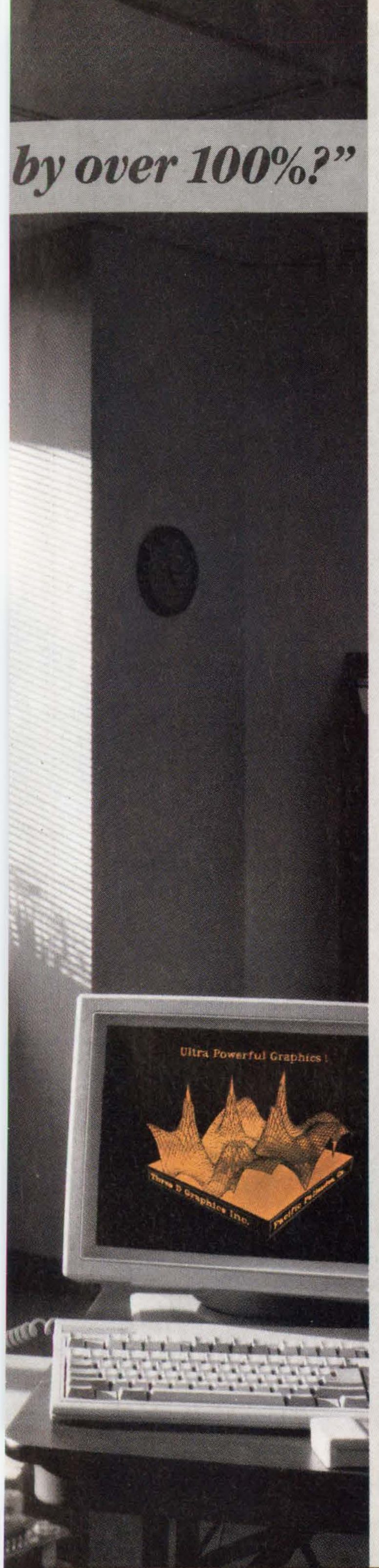

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TC524258A	X		X	X	X	X	X	X
TC528126A		X	X				X	
TC528128A		X	X	X	X	X	X	

A multi-port feature combining RAM and SAM gives you easy and fast access to data. Bit Masking is achieved through the Write Per Bit feature.

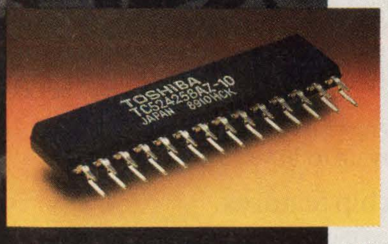
With this feature, selected planes of data can be modified using just a Write cycle instead of a Read-Modify-Write cycle.

Use the Block Write feature to write four times faster and simplify high speed window clear/fill. Use the Flash Write feature to accomplish high speed clear of selected planes without using the SAM register.

To speed things along even more, RAM read/write cycle times have been improved through fast page mode. A split SAM register provides the best method to simplify SAM to RAM and RAM to SAM transfer timing in the system.

TC524256A/8A & TC528126A/8A	–10	–12
RAS ACCESS TIME (MAX)	100NS	120NS
COLUMN ADDRESS ACCESS TIME (MAX)	30NS	35NS
FAST PAGE MODE CYCLE TIME (MIN)	60NS	70NS
SERIAL ACCESS TIME (MAX)	25NS	35NS
SERIAL CYCLE TIME (MIN)	30NS	40NS

Want more good news? Toshiba's service is every bit as good as their new Video RAM. With the people and the design specification information you need to get the job done. Call for your complete data sheet today. (1-800-888-0848 ext. 517).



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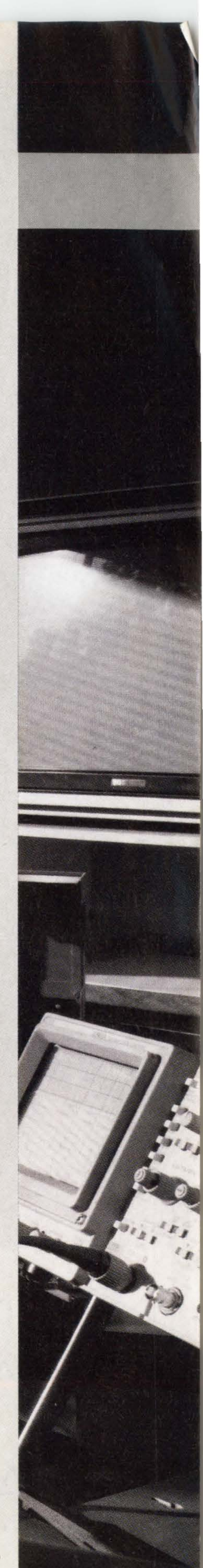

MST-88-009

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CIRCLE 119

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†Typical

Detect (BLD) circuits signal a low battery to your display. Software selectable twin clocks let you optimize your power consumption. A wide range of on-chip ROM and RAM, I/O ports and on-chip LCD drivers. As well as many other high performance peripherals. Plus, S-MOS offers powerful, easy-to-use PC-based development tools and add-on hardware that help you develop applications quickly.

S-MOS 4-Bit Microcomputers

Part Number	Memory (bits)		LCD Drivers		Features
	ROM	RAM	Common	Segment	
SMC6214	4096 x 12	208 x 4	3 or 4	32	*AC, **BLD, Timer Twin Clock
SMC6215		488 x 4		50	
***SMC6232	2048 x12	144 x 4	3 or 4	38	AC, Counter, BLD
***SMC6235	4096 x 12	574 x 4	3 or 4	48	Sound Generator Counter, BLD, AC
SMC6246	6144 x 12	640 x 4	8 or 16	40	Sound Generator Twin Clock, BLD
SMC6266	6144 x 12	1024 x 4	N/A	N/A	2 Channel AC Counter, Twin Clock
***SMC6281	1024 x 12	96 x 4	3 or 4	26	Melody Generator BLD, AC

*Analog Comparator (AC) **Battery Level Detect (BLD) *** Microcomputers running as low as 0.9V

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CIRCLE 193

APPROACHING THE LIMIT OF INTEGRATION FOR A PC, ONE CHIP PACKS BOTH THE CPU AND THE LOGIC NEEDED TO BUILD A COMPLETE MOTHERBOARD.

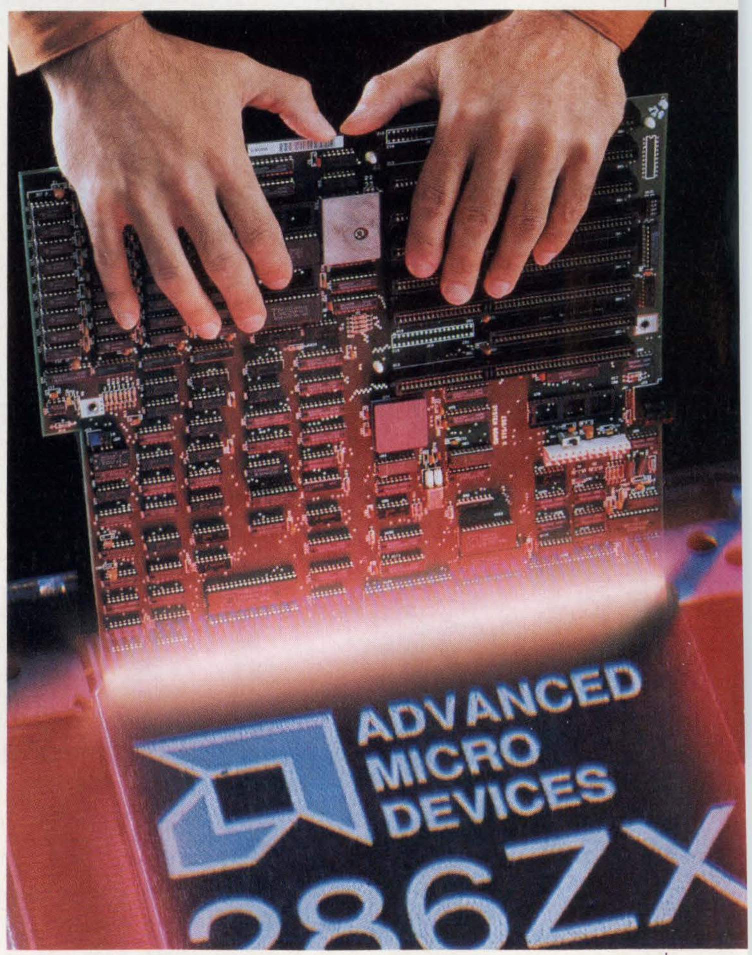
THE ONE-CHIP PC MAKES BUILDING SYSTEMS A SNAP

DAVE BURSKY

Ever since the IBM PC was introduced, designers have searched for ways to cost-reduce and shrink the size of the PC. Chip sets have reduced motherboard complexity, but without access to microprocessor designs, chipset manufacturers reached their limit. They've compressed the chip sets down to a single support IC with all the essential motherboard logic. However, Advanced Micro Devices, one of a few companies owning access to the 80286 design, has now integrated the CPU chip with all the base motherboard logic functions for PC/AT class 80286-based computers

The new processor, the AM286ZX, is targeted for motherboards in low-cost desktop systems. Its 286LX cousin, with on-chip power management logic, targets low-power, battery-operated applications, such as laptop and notebook computers, portable instruments, and so on. Both will be available in 12- and 16-MHz versions.

Besides the CPU core, the 286ZX has dynamic-memory control logic, peripheral-control and bus-clocking control circuits, and LIM EMS 4.0 memory-management logic to extend the available memory. It also has two DMA controllers, three counter-timers, two interrupt controllers, and a real-time clock *(Fig. 1)*. All of these functions are housed in a 28-by-28-mm 216-lead quad-sided flat package designed around the TapePak format defined by National Semiconductor. A plastic ring around the perimeter of the fine-pitch leads secures and protects the leads.



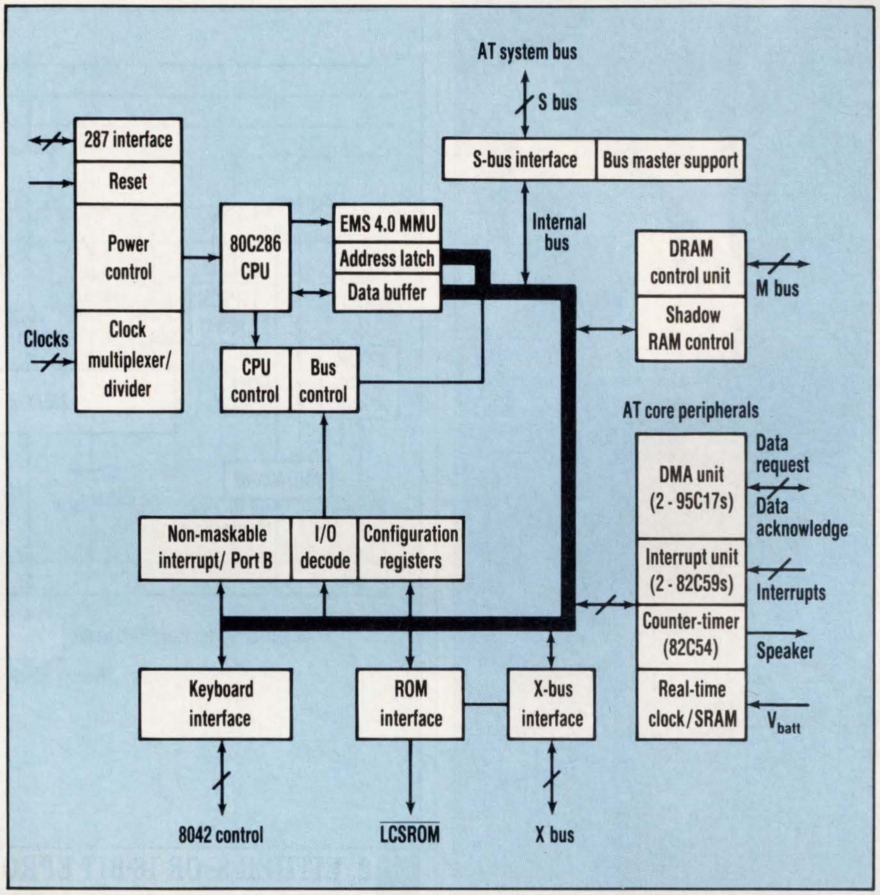
The ZX or LX replaces about 175 ICs originally used to build the first AT motherboard. To implement the full PC/AT equivalent system, dynamic-RAM (DRAM) and BIOS memories along with a keyboard controller are required, and optionally, a floating-point coprocessor can be used *(Fig. 2)*. The chip can directly drive two banks of DRAMs for a total of 16 Mbytes (using 4-Mbit chips), or 4 Mbytes (with 1-Mbit chips) and two AT-bus slots. Thus bus buffers are no longer required if only limited expansion is needed. Buffers can be added if more memory or more expansion slots are desired.

The chip can also serve in embedded PC applications, furnishing PC compatibility to an instrument, appliance, machine tool, or any other intelligent piece of hardware. For power-critical embedded applications, the LX's power management allows the chip to shut down the CPU, put the processor into a standby mode, and perform staggered or slow refresh of the DRAM array.

The CPU core is a complete 80C286 processor, functionally identical to the 80C286 that AMD sells as a standalone CPU. The on-chip DMA controllers are compatible with the 9517A/8327A controllers and support all seven PC/AT DMA channels. Similarly, the interrupt-control logic is compatible with the standard 8259A and has connections for the timer, keyboard, math coprocessor, real-time clock, and other PC/AT interrupts. The three-channel counter-timer is the same as the 8254 and provides the same configuration functions as in the AT—system heartbeat, speaker tone, and DRAM refresh request.

The real-time clock subsection has 114 bytes of low-power CMOS static RAM—64 bytes more than the AT standard 146818 real-time clock chip, for extra storage of extended-configuration data. The clock section in the LX version also includes a low-power oscillator that eliminates some external circuitry. The real-time clock includes complete time-of-day with alarm, a 100-year calendar, and the ability to generate programmable periodic interrupts.

The 286 core's fully static CMOS design allows the system to stop operation by reducing the clock to 0 Hz (dc), cutting power consumption to near zero. Or the application program can slow down the system's clock to conserve power when little activity is occurring, and speed up the processor for maximum throughput. The CPU retains data even with the clock stopped, and continues from where it left off when the clock signal returns.



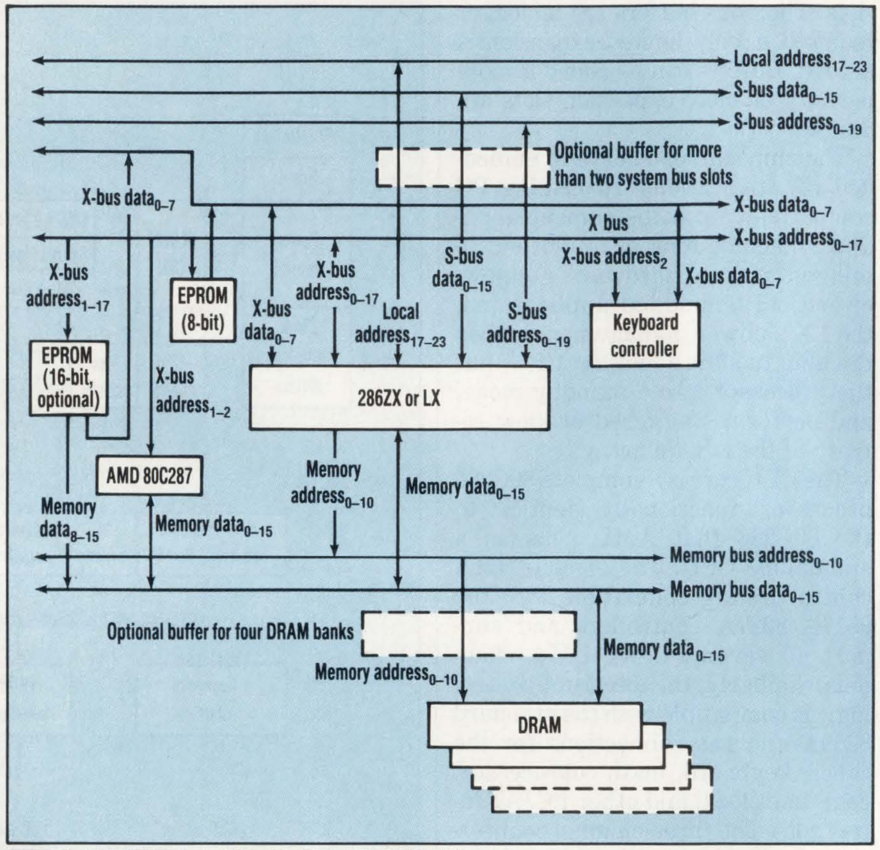
1. IF IT WASN'T A SINGLE-CHIP PC, designers would swear the 286ZX or LX was a basic PC/AT compatible motherboard. On one chip, AMD packed the CPU, EMS 4.0 control circuits, dual DMA controllers, three counter-timers, a pair of interrupt controllers, a real-time clock, DRAM refresh circuits, and an enhanced bus controller.

The CPU stop-clock mode causes a gate to stop the incoming clock from reaching the CPU logic until an interrupt arrives, thus saving system power. At the same time, the rest of the system is kept active so that the keyboard, display, and other sections can still respond. The system-standby mode stops all system clocks not essential for DRAM refresh. This mode could be used with slow-refreshing DRAMs that retain data with minimal power, and is handy if a system user had to temporarily stop work and then return to it later and not want to reload the computer's memory with the application program or data. This capability is often referred to as a "bookmark."

The chip includes an enhanced bus controller and clock-generation block with the features of the 82284 and 82288. An on-chip controller permits non-paged support, page-mode, or combined page/interleave operation with 2- or 4-way interleaving.

Furthermore, the EMS control block includes two sets of 64 address translation registers (main and alternate). This makes it possible for high-performance execution of such programs as Microsoft's Windows or Deskview. By supplying two sets of registers, the CPU enables the EMS software to switch rapidly between the two translated regions, improving the system's ability to handle multitasking applications.

With the internal system-timing circuits of the 286ZX or LX, designers can program various timing options for the CPU clock, the AT-bus clock, keyboard clock, and the math coprocessor clock. Internal configuration registers on the CPU chip hold



2. EITHER 8- OR 16-BIT EPROMS can be used with the highly integrated 286ZX/LX which stores the contents in shadow RAM for high-speed execution. All that's needed to complete the basic AT motherboard are a keyboard controller, the DRAM, and the optional math coprocessor. For large systems, optional bus buffers must be added.

the set-up information.

In addition to delivering the functionality of the 82284 and 288, the bus controller's dual state-machine design gives users a high-speed CPU synchronous state machine for DRAM control and internal register accesses. The other state machine handles system-bus control and operates either synchronously or asynchronously with respect to the CPU. Furthermore, the controller offers AT-compatible high-byte routing and word-to-byte transaction conversion for bus transfers to 8-bit peripherals. That bus subsection also controls all of the address and data routing and buffer control for all possible data transfers—CPU, DRAM refresh, and bus mastering.

A complete mini PC/AT motherboard with four card slots can be built with the chip on a card in just a 46-in.^{2} area.

In addition, by using the shadow-RAM feature that's part of the ZX memory control circuits, one low-cost 8-bit EPROM can be used to hold the BIOS. Phoenix Technologies Inc., Norwood, Mass., has developed BIOS and EMS drivers, and Hewlett-Packard Co., Palo Alto, Calif., is developing an in-circuit emulator.□

PRICE AND AVAILABILTY

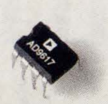
Samples of the 286ZX or LX will be available in the late fourth quarter in either 12- or 16-MHz speed grades; production quantities will be ready in the second quarter of 1991. Prices for the TapePak version in 1000-unit quantities are $69.00 and $85.50, respectfully, for the two ZX speed grades. The LX versions go for $76.50 and $89.00.

Advanced Micro Devices Inc., 5204 E. Ben White Blvd., MS-522, Austin, TX 78741; Rajesh Tanna, (512) 462-4700. CIRCLE 511

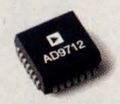
HOW VALUABLE?	CIRCLE
HIGHLY	529
MODERATELY	530
SLIGHTLY	531

Faster.

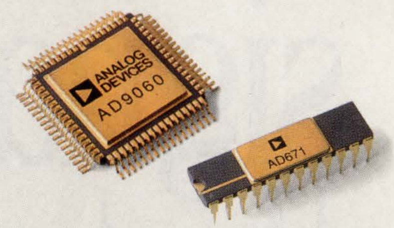
ADSP-2101 – Talk about fast – this DSP microcomputer executes a 1024-point FFT in only 2.26 ms. That's faster than other DSPs that operate at almost twice the clock rate. And since our entire ADSP-2100 family is code compatible, your code will run fast on all of our DSPs.



AD9617 – The fastest slewing and settling op amp around slews at 1400 V/μs and settles to 0.02% in just 14 ns. And with a closed loop bandwidth of 200 MHz and harmonic distortion at 20 MHz of −59 dBc (max), it makes driving A/D converters easier than ever.



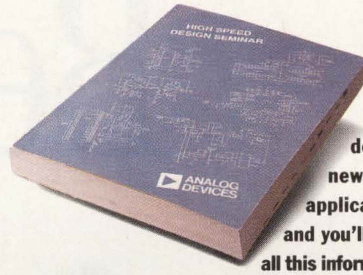
AD9712 – The only 12-bit, 100 MHz D/A converter on the market. Ideal for high-speed video and direct digital synthesis, its low glitch and low harmonics combine to deliver a spectrally pure output waveform.



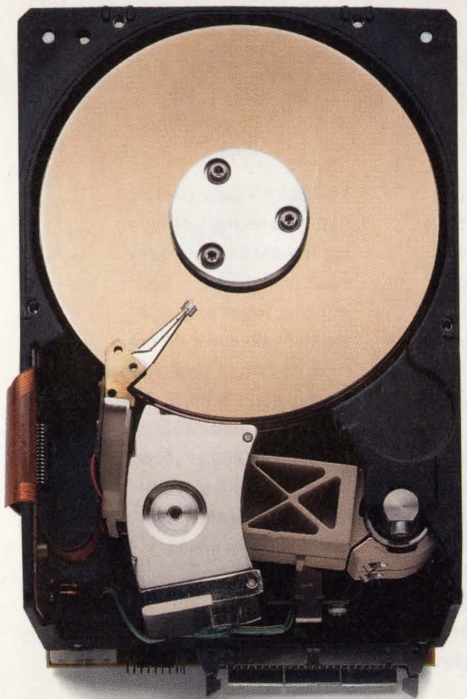
AD9060 & AD671 – The fastest 10-bit and 12-bit monolithic A/D converters, respectively. The AD9060 guarantees encode rates up to 75 MSPS for unparalleled dynamic performance. The AD671 is twice as fast as any other 12-bit monolithic, converting in under 0.5 μs, thanks to our high-speed mixed-signal ABCMOS process.

Our Spectrum CAD Tool is 100 times faster than traditional SPICE programs, so it makes quick work of mixed-signal ASIC design cycle time.

Perfect on-time delivery – it's our goal and at 97% we're getting close, thanks to our continuous improvement process based on Total Quality Management. Over 150 TQM teams make the customer and quality improvement the focus of our entire organization. A focus that gets translated into not just catchy slogans, but real action.



Tap into 25 years of experience at our high-speed and mixed-signal design seminars. You'll learn new techniques that'll get your applications to work more quickly, and you'll get design manuals that put all this information right at your fingertips.



In the disk drive market, you've got to be fast – in both performance and time-to-market. That's why seven of the top 10 disk manufacturers rely on Analog Devices for mixed-signal components.

Our high-speed D/A converters will have eavesdroppers hopping mad. In direct digital synthesis applications, they allow communications receivers to hop frequencies 100 times faster than traditional analog techniques.

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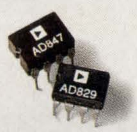
ANALOG DEVICES

CIRCLE 187

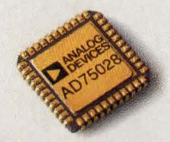
Better.



AD820/AD840 Series – If you're looking for the best in high-speed op amps, here they are – a whole family of components with the right combination of features to deliver high speed, precision, low noise, low input bias currents, low offset voltage and low drift performance. Our Complementary Bipolar process delivers gain-bandwidth products in excess of 750 MHz and slew rates in excess of 2000 V/μs.

ADV7141 – Our new Continuous Edge Graphics RAM-DAC gives users of standard low-end color monitors better graphics on their PCs. Graphics that are virtually the same as those produced on expensive engineering and scientific workstations. It does this by eliminating jagged edges, providing photo-realistic colors and shading, and displaying text comparable to a 300-dpi laser printer.

ADSP-2111 – Better integration on the best architecture in the industry. Adds an 8/16-bit host port to the two serial ports, timer, hardware companding and memory already on the ADSP-2101. And like all our DSPs, it's got fast, flexible arithmetic, wide dynamic range and a single cycle fetch of two operands (on- or off-chip). Plus it's code-compatible with the rest of our DSP family, so what's written today will be useful tomorrow.

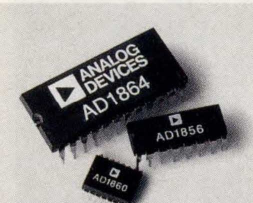


AD75028 – This custom ASIC passes the test for a top automatic test equipment manufacturer. Serving the function of 21 separate 12- and 8-bit D/A converters and providing on-chip static RAM, it also has seven channels of level setting (other monolithics only have four), and can automatically remove gain and offset errors.

Cheaper.

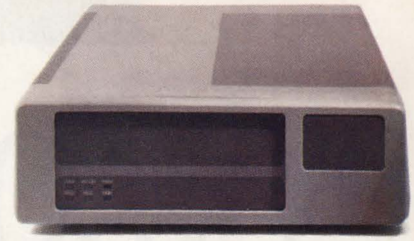
ADSP-2105 – High performance DSP at an incredibly low price. So low, in fact, you can now consider DSP in a host of new applications. And since it's pin-compatible with the ADSP-2101, and code-compatible with all of our other DSP processors, upgrading is easy and inexpensive.

AD712 – If you're working in professional audio and compact disc applications, you'll like the sound of this – an IC that combines two high-performance op amps in one compact package. You get low offset voltage and low input bias currents coupled with superb transient response, ambience, clarity and dynamic range.



SOUNDPORT DACs – We've made these DACs cost-efficient by making them complete with output amplifier, reference and digital logic interface. Perfect for high-fidelity digital audio and multimedia applications, these mixed-signal ICs achieve SNRs as high as 108 dB and THDs as low as 0.0025%.

AD22001 – One way to make a car less expensive is to make it with less parts. This component replaces a whole board of discrete analog and digital circuitry. It continuously monitors up to five automotive bulbs or indicators, along with the associated in-line fuse, and provides a digital status output.



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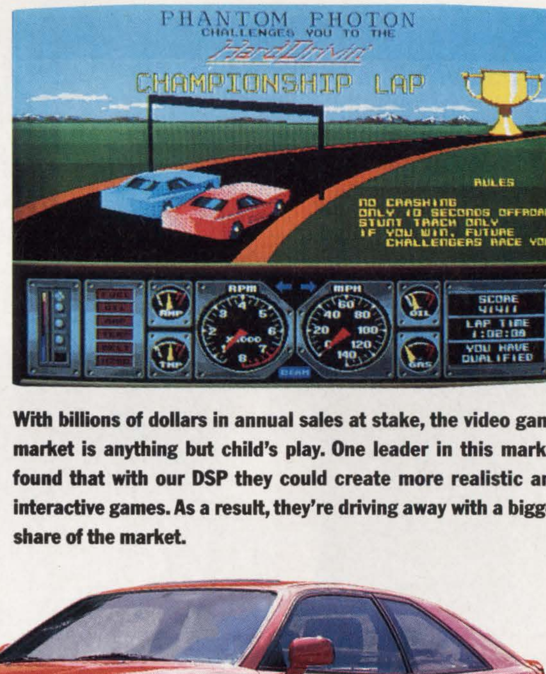
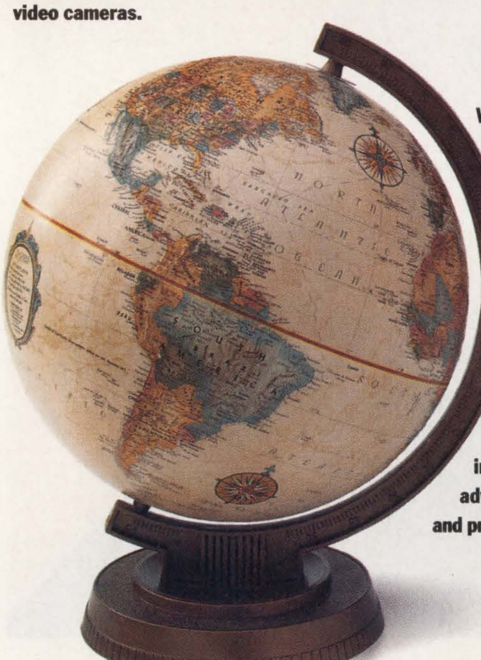
More gadgets for less money, and make it work better—that's the only way to survive in consumer electronics, the most competitive market there is. That's why three of the top five Japanese electronics firms rely on us to meet their mixed-signal needs in applications ranging from CD players to video cameras.



With billions of dollars in annual sales at stake, the video game market is anything but child's play. One leader in this market found that with our DSP they could create more realistic and interactive games. As a result, they're driving away with a bigger share of the market.



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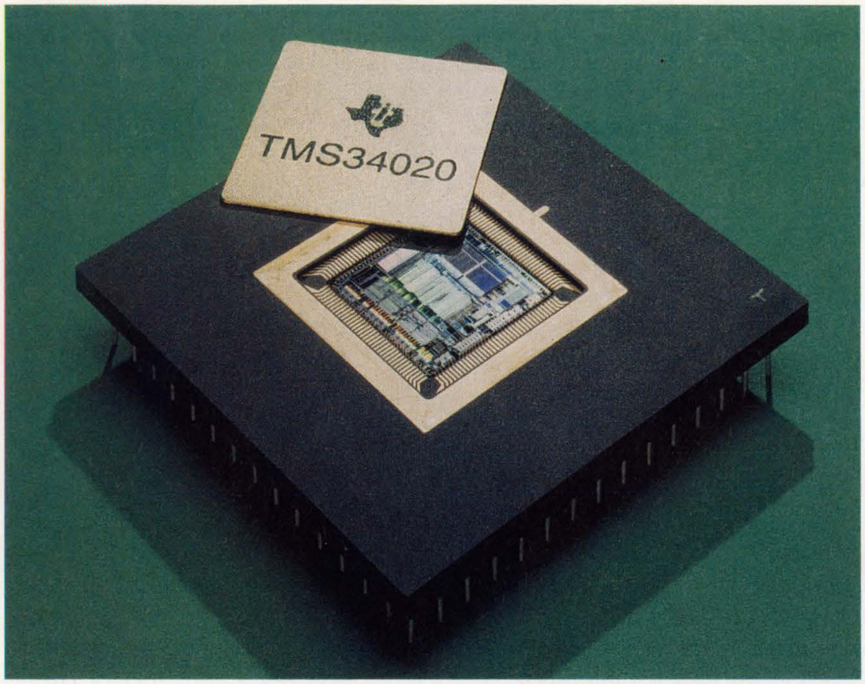


DAVE BURSKY

NEW CHIPS DELIVER HIGHER RESOLUTION AND MORE COLORS.

COLORFUL GRAPHICS FOR THE DESKTOP

Without question, the onslaught of windowed operating systems, graphical user interfaces, and multimedia applications is causing a performance bottleneck in many video subsystems. Previous PC video standards, such as IBM's VGA and EGA controllers and their predecessors, lack the resolution and color variety required by advanced applications. These requirements as well as faster drawing speeds are demanded by both users and application developers.

Apple's Macintosh computers, whose basic 8-bit graphics subsystems can be upgraded to 24 bits for true-color capability, are indicative of this trend. Furthermore, accelerators for the company's QuickDraw graphics interface—developed by Apple as well as by add-in card vendors—allow larger screens, more colors, and improved screen drawing speeds.

For graphics acceleration in any system, off-the-shelf floating-point digital signal processors or integer reduced-instruction-set computer (RISC) processors can either supplement or replace the controller. Such circuits can be used to accelerate the operations associated with repositioning an image (bit-block transfers or bitBLTs), or calculate shading or reflections. Such circuits will be discussed in a future report.

The myriad of choices offered to designers to create graphics subsystems delivers a kaleidoscope of resolutions, colors, and performance levels *(see "Manufacturers of graphics chips," p. 63)*. Dedicated commercial chips sparkle where standards exist, giving designers many alternatives from which to build controllers. When performance or speed levels can't be met by off-the-shelf chips, advanced programmable processors can either replace or supplement the video controllers. And where no hardware standards exist, semicustom or full-custom chips can be defined to do the job.

GETTING PERSONAL

The 640-by-480-pixel resolution and 16 colors offered by the IBM VGA standard has become the defacto minimum standard for most PCs. Almost all of the dozen or so VGA chip manufacturers, though, offer chips that duplicate the full set of features included in IBM's controller and provide enhanced operating modes that offer more colors and more than twice the resolution—peaking at 1024-by-768 pixels and 256 colors.

IBM's 8514/A graphics adapter, defined before the super-VGA capabilities were added to VGA chips, initially offered more than double the number of VGA pixels with up to 1024-by-768-pixel resolution and 256 simultaneous colors. Although such resolution matches the extreme high-end of the super VGA, the 8514/A chips perform their operations faster. That's because many of the time-critical graphics operations are integrated into the circuits on the chip instead of executed as firmware, as they are in the VGA cards.

The so-called "super-VGA" operating modes, however, aren't standardized and each VGA chip maker offers their own selected superset of video features. This confusion creates much duplicated software effort because each video card or chip maker must develop custom software drivers for each application program. Without the drivers, the application software couldn't take advantage of the enhanced video capabilities unless the application developer created the driver for a specific video chip or card. *(see "Extending the standards," p. 62).*

CHIP SUPPLIERS

About a half-dozen chip suppliers account for more than 80% of the non-IBM super-VGA controllers. Perhaps another six account for the remaining 20% or so of the add-in business. Chips and Technologies, Cirrus Logic, Headland Technology, Trident Microsystems, Tseng Labs, and Western Digital are the top six suppliers. Those fighting for the remaining 20% include Intel, NCR, Oak Technology, S-MOS Systems, United Microelectronics, Yamaha Systems, Zymos, and others.

Although all of the chips offered by the suppliers meet the basic VGA requirements, each slightly differs from the other when it comes to superset features. A few also include the ability to drive monochrome or color liquid-crystal, plasma, or electroluminescent display panels. In addition, several companies have more than one version of a VGA controller to cater to designers who want to offer systems at various price and performance levels.

For example, Chips and Technologies offers three VGA controllers: the 82C450, the C451 and the just-released C452A, an upgrade to the earlier C452. Another chip, to be released the last quarter of this year, is being developed.

The C450 is a low-cost controller chip. It offers a simple solution in a compact 100-lead plastic quad flat pack (PQFP) for designers that want to include super-VGA graphics on the motherboard. It supports 1024-by-768 16-color interlaced displays with just four dynamic RAMs (DRAMs) and a RAMDAC color palette. The C451 is the simplest chip, with extensions that include 800-by-600 pixels with 16 colors and a 132-column text mode. Released early this year, the C452 added the ability to drive noninterlaced monitors with 1024-by-768-pixel resolution and 16 colors. The controller uses the fast-page-mode DRAMs to operate at a 65-MHz clock frequency.

The C452A supports 16-bit-wide DRAMs and drives both interlaced and noninterlaced monitors. Housed in a 144-lead PQFP, it has a 32-bit-wide interface to the video memory to accelerate data transfers.

The chip includes support for both analog and digital monitors, and has a dual-bus architecture to tie into industry-standard-architecture (ISA), extended-ISA (EISA), or Micro Channel Adapter (MCA) buses. A controller aimed at high-end super-VGA performance is now being developed. It will include some graphics-support functions for windows or cursor acceleration.

Tseng Labs, which offers a trio of chips to suit various display needs, has two versions of its ET3000 and one version of the just-released ET4000. The ET3000A operates with up to a 65-MHz dot clock and includes support for nearly all super-VGA modes up to 1024-by-768 pixels with 16 colors, and 800-by-600 pixels with 256 colors, on interlaced monitors.

Unique features of the 100-lead PQFP chip include hardware zooming to view and alter individual pixels and the ability to simultaneously display up to eight character fonts. The chip also has a split-screen capability that permits up to three simultaneous windows with mixed graphics and text in each, and a two-color 1600-by-1280-pixel high-resolution mode with an externally supplied 180-MHz ECL clock. The 3000B offers a subset of features in a low-cost 84-lead plastic leaded chip carrier (PLCC). It only extends the VGA capability to 800-by-600 pixels with 16 colors and can only display two fonts concurrently.

For higher performance, the Tseng ET4000 adds support for video RAMs and provides 1024-by-768-pixel displays with 256 colors, or 800-by-600-pixel displays with 65,000 simultaneous colors. The 160-lead controller can drive either interlaced or noninterlaced monitors and can improve display speed up to 17-fold over the 3000A when video RAMs are used.

Some of that speed improvement is due to a small cache on the bus interface front end, and multiple first-in/first-out buffers on the CRT interface back end. By using the cache and FIFO registers, data transfers on either end are independent of true data-transfer speed. As with the ET3000, the new chip operates at 65 MHz, has the two-color high-resolution mode, and performs both vertical and horizontal panning and scrolling in both text and graphics modes.

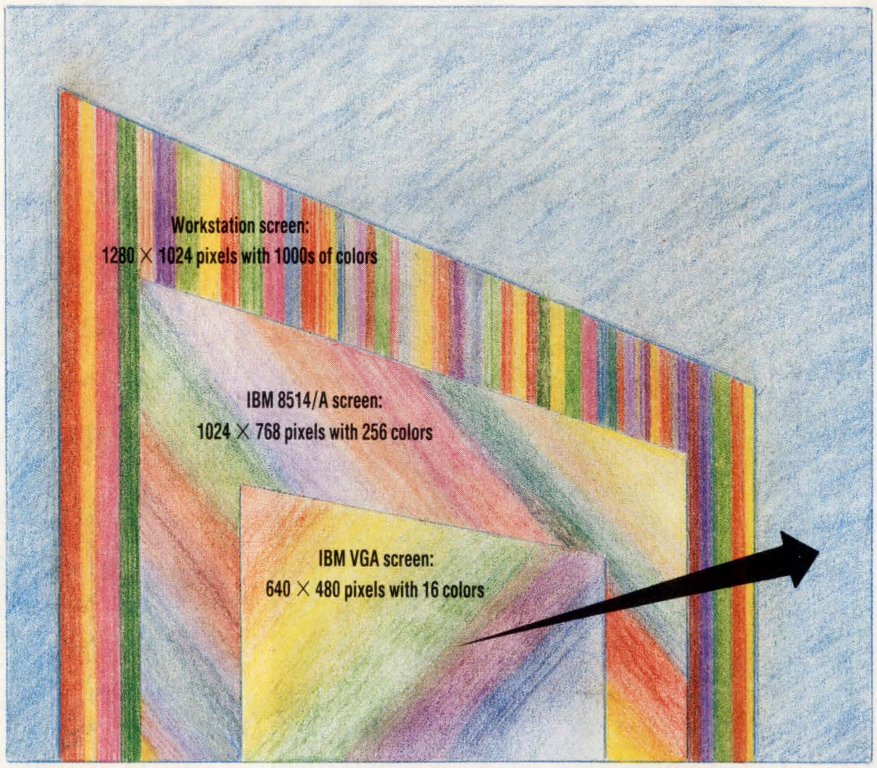
Headland has three super-VGA chips to choose from—the HT205, which supports only 800-by-600-pixel extensions with either video or standard DRAMs, and the newer HT208 and 209. The HT208 sup0orts only DRAMs but can display 1024-by-768 pixels with 16 colors on either interlaced or noninterlaced monitors.

An upgraded version, the HT209, will soon be released—it will display 256 colors on a 1024-by-768-, 800-by-600-, or 640-by-480-pixel image. It supports 65-MHz noninterlaced monitors as well as video or DRAMs (including 128k-by-8 devices), and includes hardware cursor support to improve display response time in window environments. The controller also packs an IBM 3270-compatible text mode and handles bit-mapped fonts with dithered fills for smooth character outlines. Compared to a 16-bit AT-bus super-VGA card, the HT209 can run about 15% faster with DRAMs and about 50% faster when equipped with video RAMs. The chip also has a 1-Mbyte remappable linear address space. This enables software drivers to reside in upper memory without the page boundaries encountered in video memory.

Two of a trio of controllers from Western Digital's Imaging division that have similar capabilities—the WD90C00 and 90C10—aim at desktop systems. The third, the 90C20, is targeted for portable systems. The 90C10 is a superset of the 90C00 and was released about 18 months ago. The 90C00, which delivers 16 colors for displays of 800-by-600 and 1024-by-768 pixels, and 256 colors for 640-by-400 and 640-by-480 pixels, operates with a 45-MHz dot clock. FIFO buffers on the video output allow the 100-lead chip to buffer video data to ease some of the DRAM timing requirements. Special text modes make it possible to display 132 columns with 25, 43, or 50 rows.

The more-integrated C10 operates with a 64-MHz maximum dot clock, and ties directly into two 256k-by-4 DRAMs and an 18-bit color palette. Two other extensions to the C10 are available. The C11 controls up to four DRAMs and displays up to 256 colors in the 800-by-600-pixel mode with either interlaced or noninterlaced monitors. Also available is the C12, which integrates the RAMDAC into the controller chip, greatly minimizing board space.

The 90C20 supports all functions of the 90C00 when in the CRT mode, and delivers 640-by-480-pixel resolution with 8-, 16-, or 32-shade gray-scale mapping. Consequently, the controller can drive either monochrome or color LCD or plasma panels. To keep system requirements low, the 132-lead PQFP-housed chip includes the 18-bit-wide color palette and the triple DACs to drive the CRT display. On-chip intelligent power-management logic reduces standby power for the display subsystem. Only four chips are needed to form an entire video subsystem—the 90C20 controller, two 64k-by-16 DRAMs, and the 90C61 clock IC.



ALTHOUGH THE STANDARD VGA SCREEN offers what seems to be sufficient display area and resolution for most users, it's dwarfed when compared to the typical workstation screen. A typical megapixel workstation screen provides four times as many pixels and thousands of simultaneously displayable colors. In between the workstation and IBM VGA display lies IBM's 8514/A standard, which with 256 displayable colors and 1024-by-768-pixel resolution supplies more than twice the number of pixels over the VGA screen. That's slightly over half the pixels that a workstation's screen might deliver.

Flat-Panels Are Hot

Several contenders are competing with the 90C20 to get a share of the high-growth laptop market. One challenger is the V6388 versatile panel-display controller from Yamaha Integrated Systems. The 128-lead V6388 can control LCD, plasma, and EL panels with resolutions ranging from 320-by-200 to 640-by-480 pixels. Up to 16 colors or gray scales can be displayed at maximum resolution. A built-in RAMDAC holds the color mapping data and supplies analog or digital outputs for CRTs. External DRAMs or static RAMs can hold the video data.

Yamaha is also developing an advanced VGA-compatible controller two-chip set—the 128-lead AVCC advanced video CRT controller and the 80-lead AVPC advanced video panel controller. The chips support extended 800-by-600-pixel resolution with 16 colors on either flat panels or CRTs, and up to 1024-by-768 pixels with 16 colors only on CRTs. They can use 16-, 8-, or 4-bit-wide DRAMs, and static or pseudo-static RAMs for the video memory. They provide up to 64 gray scales with monochrome displays, and up to 4096 colors with a color LCD panel.

Cirrus Logic's CL-610/620 and Chips and Technologies' 82C455 are designed for flat-panel control. The Cirrus chips don't have direct support for 16-bit-wide DRAMs and the internal RAMDAC, but can support 256-color modes and map those modes to 32 shades of gray. The CL-610/620 also include power-management logic and a hardware-assisted cursor. They can scale both text and graphics to fit flat-panel resolution.

Cirrus' CL-DG6340 supplements the 610/620 to improve the image quality of color LCD panels. The chip can take a standard 8-color LCD panel and make it appear as if it had 256 simultaneous colors (ELECTRONIC DESIGN, *July 28, p. 43)*.

For non-flat-panel applications, Cirrus also offers the CL-510A/520A

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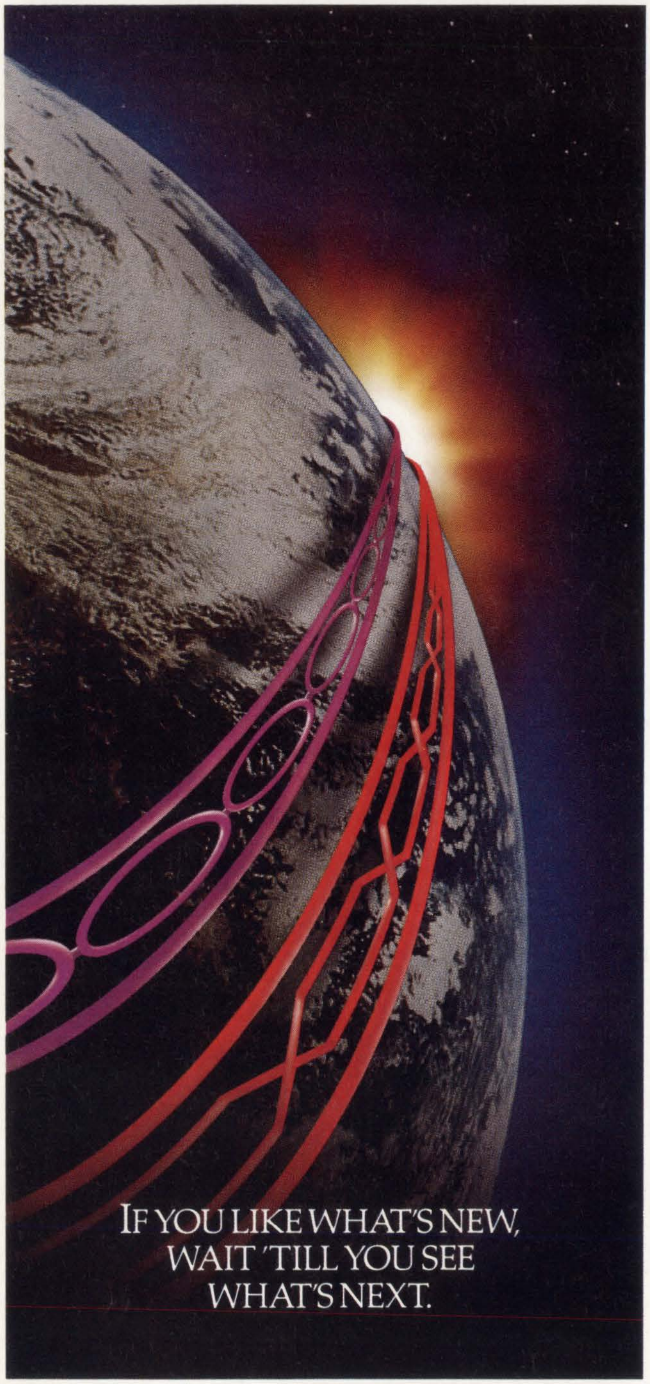

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chip set, which delivers 800-by-600-pixel resolution with 256 colors. Similar to the 610/620, the chips include a hardware-assisted cursor and a 32-bit-wide video memory interface.

Another recent addition, the CL-GD5320, integrates the functions of the 510 and 520 into one chip and includes some of the glue logic. The 100-lead IC permits a full VGA subsystem with a 800-by-600-pixel, 16-color display that's compatible with the Video Electronics Standards Association (VESA) standard to be constructed with a minimum of seven ICs. The chip—like Tseng Labs' ET4000—employs multiple internal FIFO buffers and a small CPU-to-memory read-write cache to make the DRAM and video-subsystem timing requirements independent of each other.

CRT AND LCD CHIPS

Three chips that control both CRTs and LCD panels form the Dragon chip set developed by S-MOS Systems. The SPC8000 controller handles the VGA operations, the SPC8010 or 8011 controls the LCD interface, and the SEA6461 RAMDAC ties the SPC8000 into a CRT subsystem. The LCD controller can convert color-palette information into 16 or 64 gray scales. For color LCD panels, S-MOS replaces the RAMDAC with another version, the SEA6462, and the LCD controller with an additional unit, the SPC8030. The 8030 can display up to 64 colors with resolutions reaching 800-by-600 pixels.

Trident's TVGA 8900A super-VGA controller, which slims down the designer's choice to one chip, has been available for about a year. With an interlaced or noninterlaced monitor, it can display up to 256 colors with resolutions of up to 1024-by-768 pixels. Similar to the Tseng Labs ET4000 and the Cirrus CL-GD5320, the TVGA 8900A includes a front-end cache to buffer data transfers for flicker-free display control. The chip can also drive plasma displays with resolutions reaching 640-by-480 pixels and 16 gray scales.

To handle complex character sets, such as Chinese or Japanese, Trident is developing the TBC8900. The chip can handle character font cells up to 24-by-24 pixels in the graphics mode, and 16-by-16 pixels in the text mode.

One little-seen supplier for VGA products, NCR, just unveiled a high-performance controller, the 77C22. The company claims it can deliver up to 10 times the drawing speed of standard VGA controllers. The chip incorporates a smart host interface with a deep 32-word by 16-bit FIFO buffer and other logic that improves system throughput. Also available is an enhanced version dubbed the 77C22E, which offers short-cycle data-transfer rates of 75 ns—faster than AT-buses can handle.

The 160-lead chip also has clock-generator support, a bit-mapped cursor and hardware control, and expanded DRAM control to handle the 64k-by-16 memories. Dot-clock rates of up to 65 MHz are possible with the 77C22. Font widths of 4 or 7 to 16 pixels can be displayed on screens with resolutions of 1024-by-768 or 800-by-600 pixels and 16 colors or 640-by-480 with 256 colors. Up to 4 Mbytes of frame-buffer RAM can be addressed, allowing the chip to handle multitasking video, extended-display modes, and animation.

Delivering 800-by-600 displays with 16 or 256 colors and 1024-by-768 images with 16 colors (interlaced), the Poach 52 VGA controller from Zymos boils a super-VGA subsystem down to just five chips plus memory. The controller includes a FIFO buffer to lessen bus-transfer-rate dependence. As a result, 100-ns DRAMs can be used—even with all of the enhanced modes. Using 4- or 16-bit-wide DRAMs, the controller enables a minimal-space VGA subsystem to be included on a system motherboard or occupy a small portion of an add-in card.

Also offering similar operating modes is the OTI-067, a super-VGA controller from Oak Technology. The 144-lead chip displays up to 256 colors in 800-by-600-pixel images, 16-colors in 1024-by-768-pixel screens, and offers a unique portrait mode with 4 colors and a 768-by-1024-pixel format. Both interlaced and noninterlaced monitors can be driven with a 65-MHz dot clock.

For simpler super-VGA systems, the company also offers the OTI-037. This chip has an 800-by-600-pixel 16-color extension and is in a 100-lead PQFP. Competing with the OTI-037 is the UM587 controller from United Microelectronics. The chip supports the 800-by-600-pixel 16-color extension as well as 132-column text modes. It also supplies basic VGA functionality in a 100-lead PQFP.

THE NEXT LEVEL

Beyond the VGA, IBM's 8514/A graphics standard has become the goal for many PC chip and board manufacturers. Although its resolution is the same as that of the highest end of VGA—1024-by-768 pixels—the controller's performance and intelligence is much higher. The higher performance comes from the controller implementing some operations in hardware rather than software. The operations integrated in silicon include bitBLT, line drawing, color mixing, polygon filling, pattern filling, and scissoring (post clipping).

The complex circuitry of the controller chip, though, makes developing functionally compatible silicon rather difficult. This challenge is further exacerbated because IBM released only its adapter interface (AI) definition, rather than a hardware register specification. By releasing only the AI, IBM hoped that all software developers would create their programs using the calls rather than relying on specific hardware features. If that was done, then the underlying hardware could be updated with no change to the software.

The 8514/A specification doesn't define a separate text mode in hardware. Rather, text is supported in the graphics mode, thus enabling characters to be any size. However, the AI does define three standard text modes for the 1024-by-768-pixel resolution option: mode 0 with 85 characters on 38 lines with a 12-by-20-pixel character cell; mode 2 with 128 characters on 54 lines and an 8-by-14 character cell; and mode 3 with 146 characters by 51 lines and a 7-by-15 character cell. With a 640-by-480-pixel screen, the AI also supports an 80-character-by-34-line screen (8-by-

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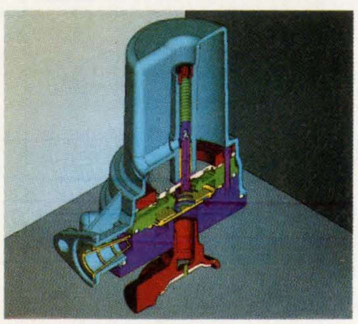

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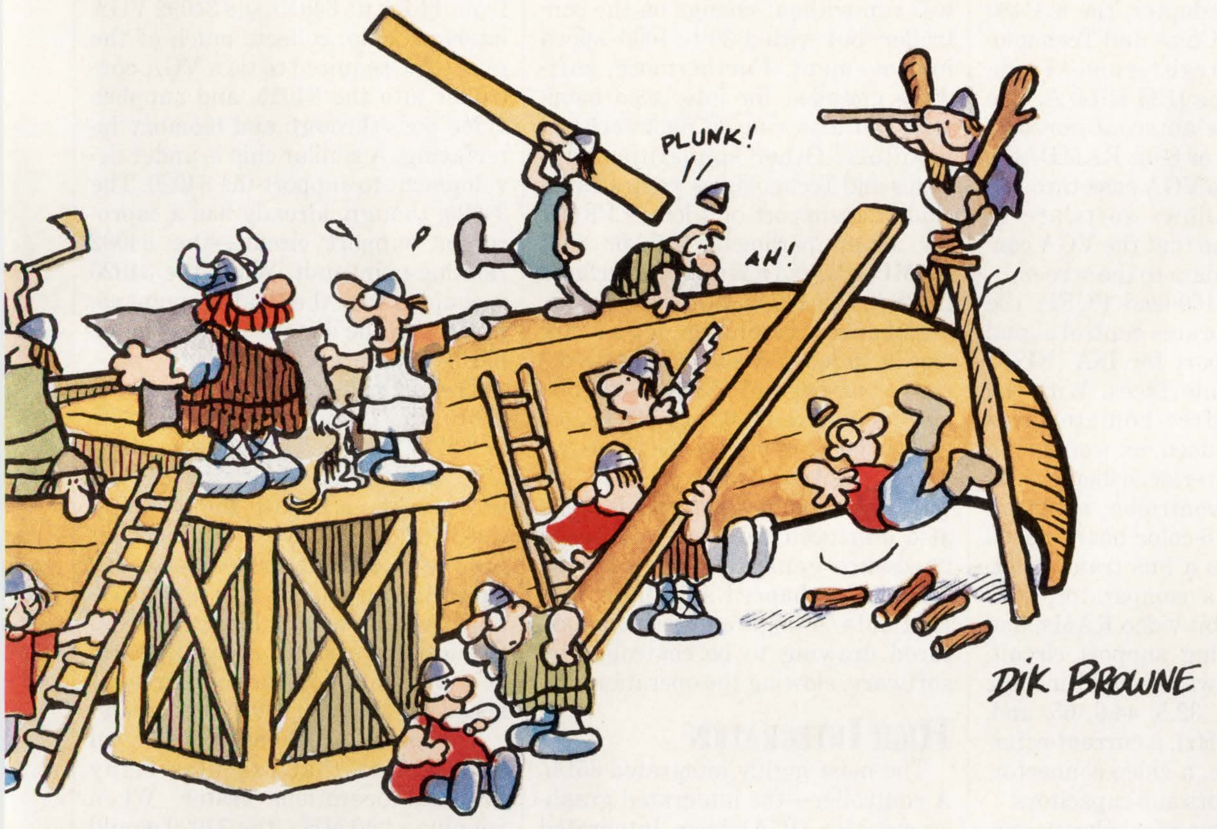

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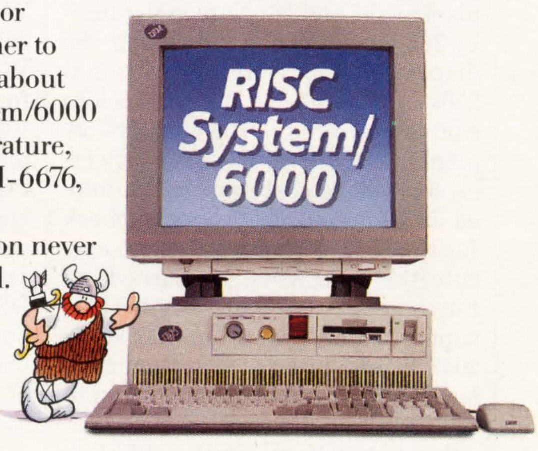

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14-pixel character cell).

Up to now, only three companies have released dedicated chips or chip sets to implement the 8514/A standard—Chips and Technologies, Western Digital's Imaging Products division, and Integrated Information Technology. Boiling down the number of chips to just nine to build a complete basic adapter, the 82C480 controller from Chips and Technologies offers both register and AI compatibility with the IBM 8514/A. The controller can be autoconfigured to tie into either 6- or 8-bit RAMDACs. Also included is a VGA pass-through mode, which allows software to switch the chip so that the VGA controller can send data to the screen.

Housed in a 160-lead PQFP, the chip also incorporates control-signal and timing support for ISA, EISA, and MCA bus interfaces. With the circuit, flicker-free noninterlaced displays can be used, as well as the IBM standard interlaced displays. In addition to the controller, all that's required for a 16-color board based on the 82C480 is a bus transceiver, the RAMDAC, a comparator, four 256-kword-by-4-bit video RAMs, and the 82B484 timing support circuit. Additional hardware would include crystals (25.175, 32.5, 44.9, 65, and, optionally, 80 MHz), a current reference and a diode, a video connector, and a few resistors and capacitors.

With 512 kbytes of display memory, the chip provides 16 or 256 displayable colors in the 640-by-480-pixel mode, and 16 colors in the 1024-by-768-pixel mode. By doubling the display memory (four additional 256k-by-4 video RAMs), 256 colors can be delivered in the 1024-by-768-pixel mode. An EPROM for power-on self-test code storage can be added as an option. The chip can check for the ROM automatically and execute the code when it's turned on. Furthermore, the controller can also support resolutions of up to 2540-by-2048 pixels, interlaced or noninterlaced, with video data rates of up to 300 MHz.

Implementing similar 8514/A functionality on a pair of chips, Western Digital's personal-workstation graphics-array (PWGA1) chip set divides the control task into a pixel address manager and pixel data manager, both housed in 132-lead fine-pitch PQFPs. Independent video and data clocks enable designers to optimize system timing.

As with the Chips and Technologies 8514/A controller, all software written for the IBM 8514/A adapter will run without change on the controller, but with a 30 to 100% speed improvement. Furthermore, software intended for interlaced monitors will also run on noninterlaced monitors. Other similarities with Chips and Technologies' controller include the support of a local EPROM for set-up parameters, 6- or 8-bit RAMDACs, and integrated interfaces for ISA, EISA, and MCA buses.

Enhanced resolution modes are also included in Western Digital's design—one page of 1280-by-1024 pixels, two pages of 1024-by-768 pixels, or two pages of 640-by-480 pixels, all with 256 colors, can be displayed by the chip. Graphics commands were also enhanced to allow high-speed hardware generation of textured lines and enhanced solid lines. The IBM 8514/A chip requires such textured drawing to be controlled by software, slowing the operation.

High Integration

The most highly integrated 8514/A controller—the integrated graphics adapter (IGA) from Integrated Information Technology—combines both the 8514/A controller and the VGA controller on one chip. As a result, the company eliminates the VGA display card typically required for VGA-pass-through when both VGA and 8514/A software must display data. Housed in a 144-lead PQFP, the controller supports interlaced or noninterlaced displays, runs with dot-clock rates of up to 65 MHz, and can be used with standard DRAM to implement a single frame buffer for the video memory. Displays with 256 colors and resolutions of 640-by-480, 800-by-600, and 1024-by-768 pixels can be created.

Alternatively, the 8514/A standard can be implemented with a general-purpose off-the-shelf graphics processor, such as the TMS34010 or 34020 from Texas Instruments. More than a dozen board-level manufacturers have done just that: By employing either of the two processors, they implemented either AT, EISA, or MCA-compatible graphics cards as well as cards for such systems as VME or Multibus backplanes.

A recently released support chip from TI for its 34010, the 34092 VGA interface chip, collects much of the glue logic required to tie a VGA controller into the 34010, and supplies video pass-through and memory interfacing. A similar chip is under development to support the 34020. The 34020, though, already has a coprocessor support circuit—the 34082 floating-point unit. When the 34020 is coupled with the floating-point coprocessor, the duo makes a formidable 3D graphics engine.

The highest-speed version of the 34010 runs at up to 60 MHz, with 40- and 50-MHz speed grades also available. Although a 16-bit external bus provides the I/O path for the data, the 34010 internally contains a 32-bit processor core optimized for video control. The chip can support displays with up to 16 million colors and resolutions reaching 4k-by-4k pixels. It's possible to draw images at speeds of about 50,000 2D vectors/s.

The newer 34020 has an improved architecture that executes many graphics operations faster. When running at 40 MHz, the 34020 would be equivalent to an 80-MHz 34010, which at 40 MHz give the 34020 a throughput of about 10 MIPS and a drawing speed of about 200,000 vectors/s. Some operations were accelerated by as much as 50-fold over those in the 34010. To get the speed, TI included a full 32-bit wide external bus structure, a 512-byte instruction cache, enhanced instructions, direct support of special features included in the latest megabit video RAMs, and a coprocessor interface for a floating-point accelerator.

The companion floating-point processor delivers 32 MFLOPS of single-precision calculations when running at 32 MHz and 40 MFLOPS at 40 MHz. TI is now sampling only the 32-MHz version. Multiple floating-point units can be included in a graphics

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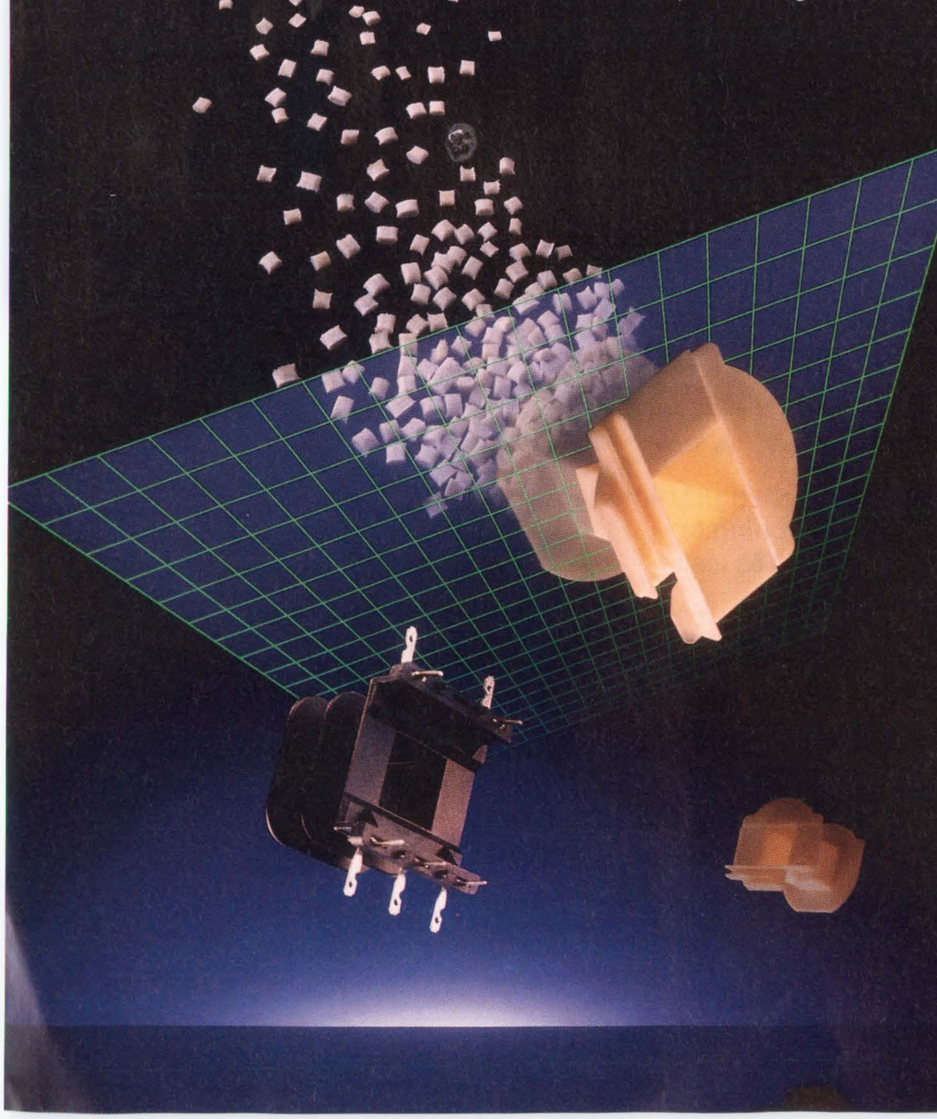

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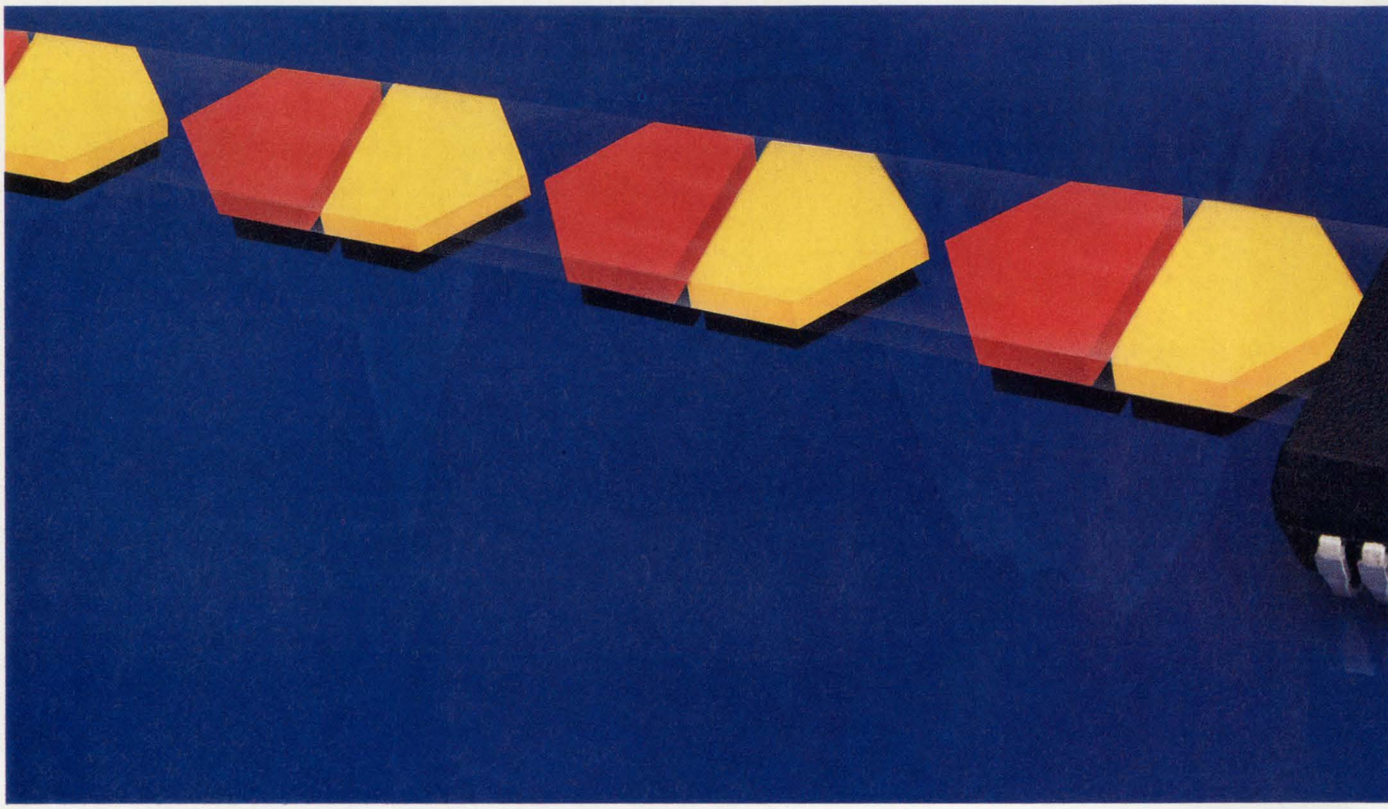

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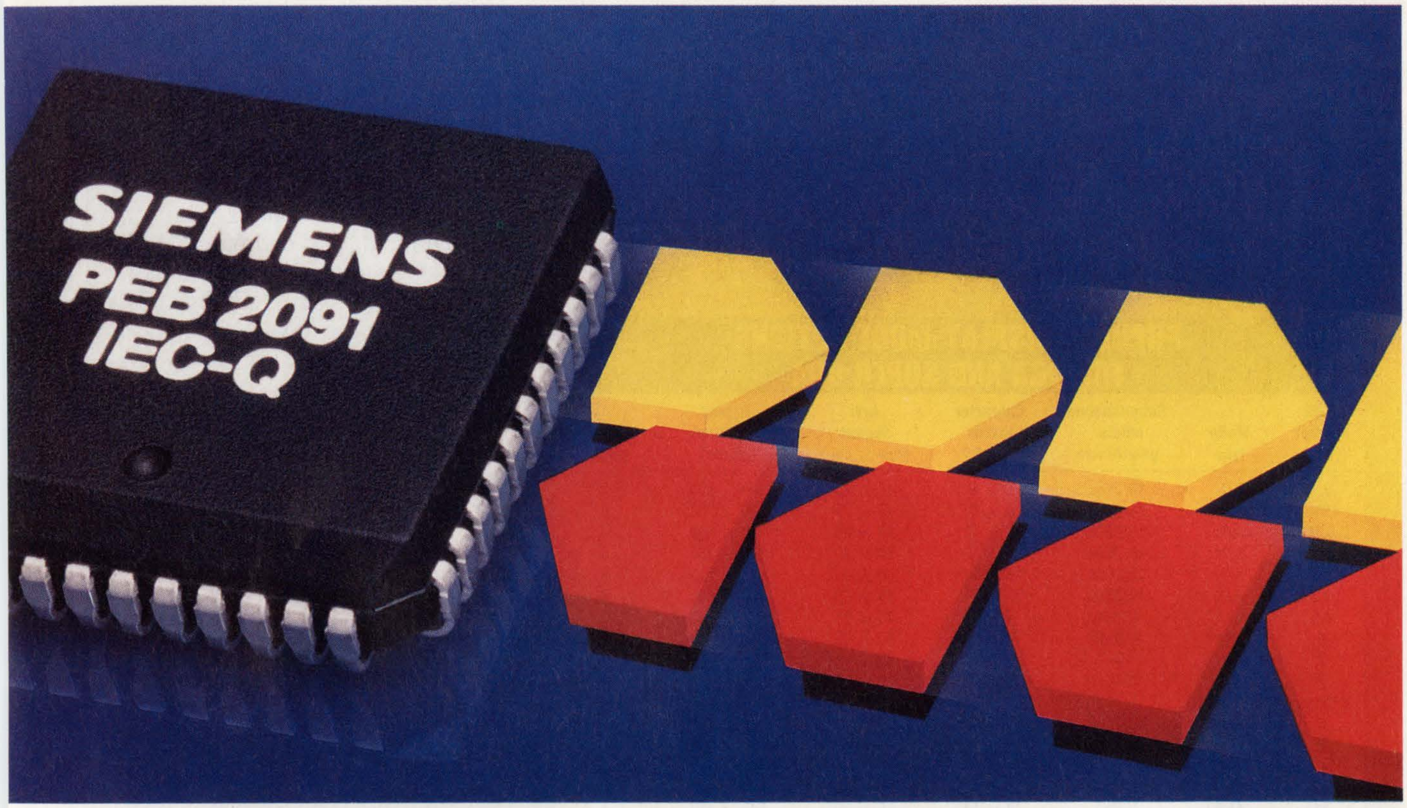

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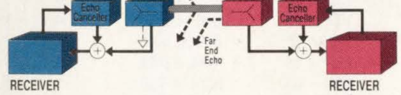

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CIRCLE 173

EXTENDING THE STANDARDS

In the world of IBM-compatible PCs, visual output is usually defined by an alphabet soup of progressive standards. These standards started with the monochrome display adapter and its 320-by-200-pixel resolution, and have improved gradually since then. Today's latest offering, the video graphics adapter (VGA), includes almost all previous PC display standards plus numerous enhanced modes by offering over a dozen programmable display resolution and color options *(see the table)*.

The basic VGA display options, defined by the mode settings, include previous color-graphics-adapter (CGA), and enhanced-graphics-adapter (EGA) modes for backwards compatibility. The best of the pre-VGA standard modes is the EGA standard with its 640-by-400-pixel and 16-color resolution. Many companies also extended the EGA standard to achieve VGA-level resolution, but the popularity of "Super EGA" was short-lived due to the rapid acceptance of VGA.

POPULAR DISPLAY-MODE OPTIONS FOR VGA AND SUPER VGA

Mode number (hex)	Mode type	Simultaneous colors/ palette size	Character matrix (pixels)	A/N format (row × col.)	Display resolution (pixels)	Maximum pages
0,1	A/N	16/256k	8 × 8	40 × 25	300 × 200	8
0,1[1]	A/N	16/256k	8 × 14	40 × 25	320 × 350	8
0,1[2]	A/N	16/256k	9 × 16	40 × 25	360 × 400	8
2,3[2]	A/N	16/256k	8 × 8	80 × 25	640 × 200	8
2,3	A/N	16/256k	8 × 14	80 × 25	640 × 350	8
2,3	A/N	16/256k	8 × 16	80 × 25	720 × 400	8
4,5	APA	4/256k	8 × 8	40 × 25	320 × 200	1
6	APA	2/256k	8 × 8	80 × 25	640 × 200	1
7	A/N	—	9 × 14	80 × 25	720 × 350	8
7[2]	A/N	—	9 × 16	80 × 25	720 × 400	8
8 through C RESERVED						
D	A/N	16/256k	8 × 8	40 × 25	320 × 200	8
E	APA	16/256k	8 × 8	80 × 25	640 × 200	4
F	APA	—	8 × 14	80 × 25	640 × 350	2
10	APA	16/256k	8 × 14	80 × 25	640 × 350	2
11	APA	2/256k	8 × 16	80 × 30	640 × 480	1
12	APA	16/256k	8 × 16	80 × 30	640 × 480	1
13	APA	256/256k	8 × 8	40 × 250	320 × 280	1
54[3]	A/N	16/256k	7 × 9	132 × 43	924 × 387	2
54[4]	A/N	16/256k	8 × 9	132 × 43	1056 × 387	2
55[3]	A/N	16/256k	7 × 16	132 × 25	924 × 400	4
55[4]	A/N	16/256k	8 × 16	132 × 25	1056 × 400	4
56[3]	A/N	4/mono	7 × 9	132 × 43	924 × 387	2
56[4]	A/N	4/mono	8 × 9	132 × 43	1056 × 387	2
57[3]	A/N	4/mono	7 × 16	132 × 25	924 × 400	4
57[4]	A/N	4/mono	8 × 16	132 × 25	1056 × 400	4
58[4]	APA	16/256k	8 × 8	100 × 75	800 × 600	1
59[4]	APA	2/mono	8 × 8	100 × 75	800 × 600	1
5A	APA	2/256k	8 × 16	128 × 48	1024 × 768	1
5B	APA	4/256k	8 × 16	128 × 48	1024 × 768	1
5C	APA	256/256k	8 × 8	100 × 75	800 × 600	1
5D	APA	16/256k	8 × 16	128 × 48	1024 × 768	1
5E	APA	256/256k	8 × 16	80 × 25	640 × 400	1
5F	APA	256/256k	8 × 16	80 × 30	640 × 480	1

Notes: A/N = Alphanumeric APA = all points addressable

1 EGA enhanced text modes (350 scan lines)

2 Enhanced text modes (400 scan lines)

3 Fixed-frequency monitor setting. The character font must be loaded by the software application or driver.

4 Mulitfrequency monitor setting. The monitor setting is DIP-switch selectable and can be determined by reading PR register 3CFH.

General comments: Chart includes all backwards-compatible EGA, CGA, Hercules modes.
Mode 5F can only be set if 512 kbytes of video memory exist.
3[2] is the power-on default mode for a color monitor.
7[2] is the power-on default mode for a monochrome monitor.
Cursor is not displayed in the all-points-addressable modes.

However, never content to accept just the VGA standard, many manufacturers extended the standard to add 800-by-600- and 1024-by-768-pixel resolution modes, and expanded the color options from 16 to 256. However, each chip or board maker selected or implemented the superset of features with their own twists that often makes their version incompatible with a similar resolution unit from another company. Most recently, several novel modes, such as a two-color 1280-by-1024, or a four-color 768-by-1024-pixel portrait mode have appeared (not listed in the table).

In turn, each video card manufacturer must provide a library of video driver software so users can take advantage of the extended-display modes. Such a large software undertaking results in a poor use of technical resources. It would be much more efficient if the application software developer could include a "universal" driver, which would check to see if a mode was available.

To get some degree of standardization, many chip, card, and monitor suppliers created an organization that will try to set up extended-mode standards for graphic adapters, monitor scan rates, signal timing relationships, and other aspects of video subsystems. The Video Electronics Standards Association (VESA) has over 50 members. It obtained agreement for an 800-by-600-pixel, 16-color standard (VS900602) that defines a common software interface to the VGA BIOS.

The committee is working on standards that define a common range of ROM addresses and register names for 8514/A-compatible boards in an AT bus (VS890802-1 and VP900308-1).

To contact VESA, call Jan Shepard, executive director, (408) 971-7525; 1330 South Bascom Ave., Suite D, San Jose, CA 95128.

TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

Creating systems with an analog edge

IN THE ERA OF

MegaChip

TECHNOLOGIES

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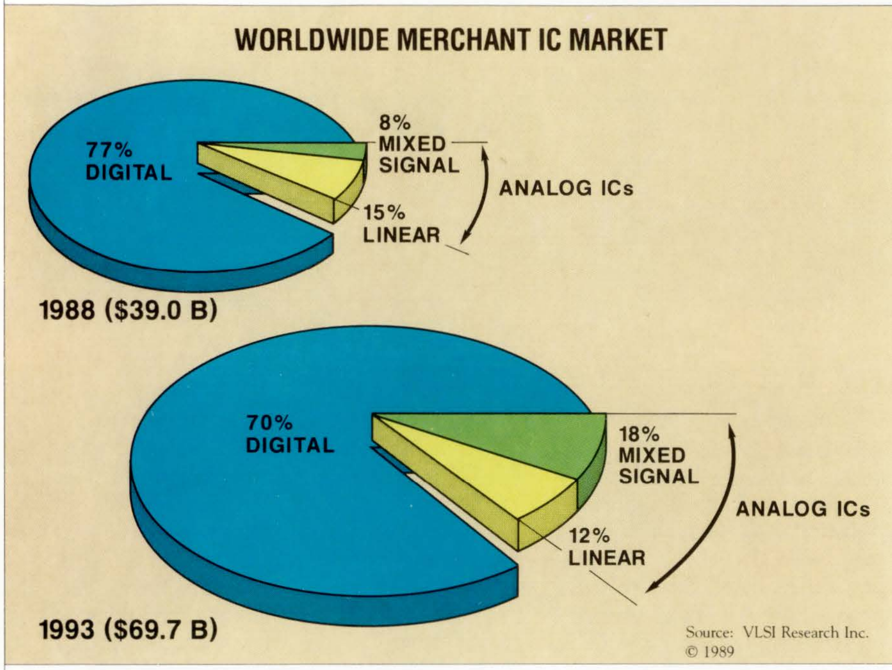

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TEXAS INSTRUMENTS

accelerator to improve the drawing speed.

Close to two dozen cards offered by nearly as many manufacturers employ either TI's 34010 or 020. One example consists of the Info IGX and SGX from Nissei Sangyo America. The IGX card is based on the 34010. It provides a 1280-by-1024-pixel display and emulates 8514/A, VGA, and CGA controllers. Higher-performance SGX cards use the 10 MIPS 34020 and deliver either 1280-by-1024- or 1600-by-1280-pixel displays with VGA and 8514/A emulation modes. All three cards can display 256 colors simultaneously from a palette of 16.7 million.

Some of the other PC card suppliers using the TI chip include Artist Graphics, Compaq Computer, Dell Computer, Matrox Electronic Systems, NEC Technologies, Number Nine Computer, Renaissance GRX (now owned by Zymos), and Vermont Microsystems. One alternative to the TI chips is the HD63484, a graphics processor offered by Hitachi America. Only Artist Graphics offers an 8514/A-compatible card with that chip.

In addition to PC add-in graphics cards, the 340X0 chips are widely used in other graphics applications: on VME cards for industrial systems, in X-window terminals as a graphics controller, laser printers, and other non-PC systems. One other controller, the Hitachi HD63484 can also be found in industrial systems. Although it hasn't become widely accepted, the controller does offer dedicated graphics operations considerably faster than software-controlled drawing operations.

Similarly, Apple has established a minimum performance level in the Macintosh world. This is done through its color and monochrome graphics adapters and its first accelerator—a RISC-based card employing the Am29000 from Advanced Micro Devices that speeds up the QuickDraw operations.

Also applying RISC to a Macintosh graphics card, Radius used the 6-MIPS Acorn processor manufactured by VLSI Technology to create its QuickColor graphics engine. The Nubus graphics card delivers about six times the performance of the Macintosh QuickDraw processor.

Combining both a 24-bit color video display capability and full-motion video, a board from RasterOPs gets its power from custom logic. The card can be used in multimedia applications, and brightness, contrast, or sound can be controlled from the keyboard. With a companion board—the Video Expander—Macintosh graphics can be sent to a video recorder.

Relying on custom circuits, two accelerator cards developed by SuperMac Technology also offer close to a six-fold performance increase. The custom chips implement many of the QuickDraw commands in hardware, significantly reducing the time for each operation to execute. The ColorCard/24 delivers 640-by-480-pixel resolution to drive the 12- or 13-in. Apple monitors, while the other product, the Spectrum/24, delivers 1024-by-768-pixel resolution for 19-in. monitors.□

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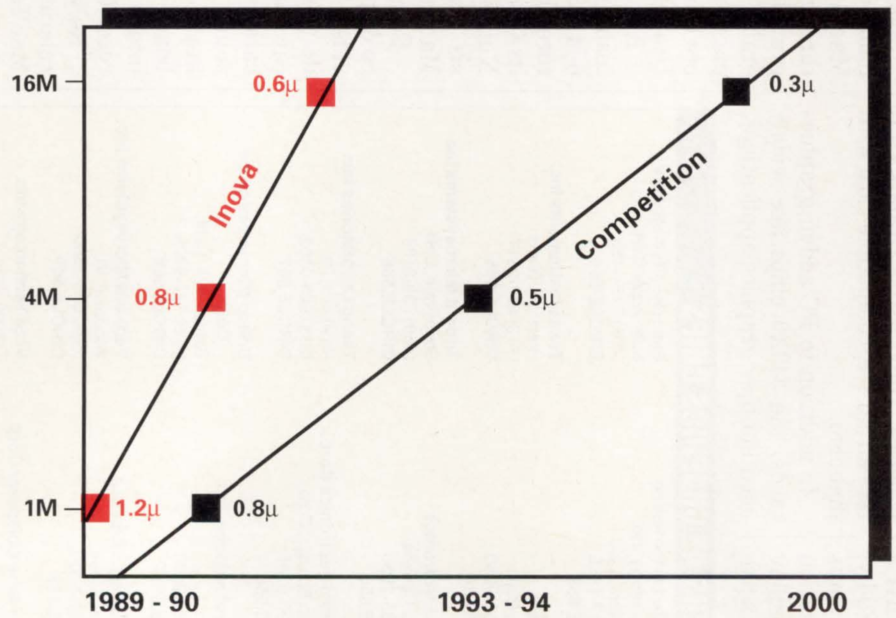

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CIRCLE 216

BECAUSE AN i486 EASILY OUTPACES THE MAIN MEMORY BUS, AN EXTERNAL CACHE STEPS IN TO BOOST SYSTEM THROUGHPUT.

DESIGN A SECONDARY CACHE FOR INTEL'S i486 PROCESSOR

Intel's i486 microprocessor, with its internal cache, can solve computational problems at blinding speeds. Thanks to the number of transistors on the i486 chip, functions once performed off the 386 CPU can be incorporated on chip for faster operation. The i486 CPU not only contains the cache memory and floating-point math unit, but many of the CPU's instructions have been streamlined with increased parallelism.

The i486 CPU's internal 8-kbyte, four-way set associative cache would seem to eliminate using an external cache. Current 386 benchmarks reportedly can run up to three or four times faster on the i486. Some of this can be attributed to these benchmarks, which are small enough to be completely contained within the i486's internal cache. However, real-world programs are often quite large or may operate on huge data sets. In that case, they would not fit within the i486's cache at all.

Without an external or secondary cache, the true speed of the i486 CPU can't be realized. This is because bus transactions are still limited by the speed of the system backplane and the economical dynamic memory used for program storage. In other words, any time the CPU pins can wiggle at a much faster rate than the signals on the main memory bus, a cache can step in to boost the system's throughput.

Backplane response time is limited by many factors: the time to refresh dynamic RAMs (DRAMs), buffers (with their associated propagation delays) within the bus timing's critical paths to route DMA or multiprocessing data paths, and the meeting of protocols for bus arbitration at the expense of timing delays. Even the time to travel along the backplane must be considered. To absorb the difference in speed between the CPU's irregular high-speed, data-transaction needs and the backplane's slower response, a cache is needed to buffer the data in either direction and to match CPU timing to backplane timing, much as a FIFO buffer would. Most current i486 system designs incorporate a simple external secondary cache.

Without a secondary cache and write buffer, all write cycles would require wait states, as would all of the read cycles that produced internal cache "misses." Intel suggests that, even with the internal cache of the i486, about 10% of all CPU read cycles must go external to the chip's 8-kbyte cache. This doesn't sound like a large number until designers consider 200-ns DRAM access time—through all of the bus buffers and refresh circuitry. A 200-ns access time

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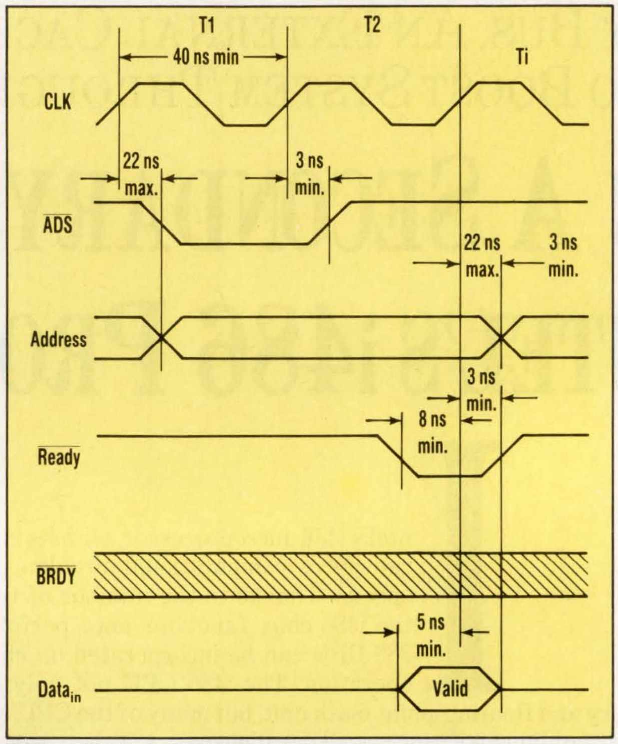
Santa Clara, CA 95052-8015; (408) 727-6116.

is equivalent to one normal cycle, plus four 40-ns wait states (on a 25-MHz CPU). As a result, if 10% of all I/O cycles incur four wait states, the system operates at an average of 0.4 wait states. Needless to say, this sort of system will never win a benchmark war.

Even if economy were ignored and a static-RAM-only system were designed, the signal buffering needs would still require that CPU wait states be inserted at any clock rate. Here's why: A static RAM (SRAM) would need to have an access time of at least 53 ns to support the slowest 25-MHz i486 I/O transaction (a derivation of this figure will be shown later). At first flush, this requirement doesn't seem too tough for an SRAM-based system. However, most systems use buffers on both the address and data buses to keep VLSI devices, such as the CPU, from driving large capacitive loads. Assuming that only one buffer is used between the SRAMs and the CPU on the address bus and one buffer is used on the data bus, a 10-ns buffer would cost the design 20 ns. Now the static RAMs would need to have a 33-ns access time to support 25 MHz.



1. FOR A 25-MHz i486 with a basic bus and single-read cycle, the addresses become valid during the first cycle. The address isn't guaranteed to become valid until 22 ns after the beginning of the first cycle. To support a zero-wait read, data must be valid at least 5 ns before the clock's rising edge at the end of the second cycle.

Unfortunately, most fast SRAMs are too small to handle much of the software written for Intel's processors. If system cost is no object, a 25-ns 64k-by-4-bit RAM is readily available, but this size device holds little code. This means that chip-select decoding must be used to expand the RAM's depth. Another problem is that chip-select access time on these devices is equivalent to their address access time. As a result, if a 25-ns SRAM was used in a system requiring a 33-ns SRAM access, only 8 ns would be left to decode addresses. Even discounting such real-world problems as skew and capacitive loading, an 8-ns decoding time is difficult to achieve.

All of this timing is based on the slowest cycle of the slowest speed grade i486—a 25-MHz CPU doing single reads. The i486 can also execute burst reads, where four reads are performed in five cycles, and clock speeds are specified up to 33 MHz. Imagine what this would do to the timing of the example SRAM-only system.

A secondary cache placed between the CPU and the system bus can enhance throughput immensely in any i486-based system. With a cache memory, a small number of SRAMs can be attached directly to the CPU's Address and Data pins without requiring intervening buffers. If cache depth and policies are chosen judiciously, the cache can be accessed instead of main memory for most CPU data I/O cycles, enabling the CPU to run at near-zero average wait states.

Another cache-design concern is minimizing board space. As a general rule, less-dense SRAMs are considerably faster than their denser counterparts. This implies that all speed requirements could be met by using many less-dense SRAMs. Some designers have committed half of a PC-style motherboard to the cache alone. Because most system designers would not want the cache to force them to remove other important functions from their boards, designing caches in minimal board space should be considered.

i486 Bus Timing

The i486 I/O bus is a drastic departure from the buses of its predecessors. Unlike the 386, 286, and earlier Intel CPUs that use asynchronous buses, the i486 uses a synchronous bus. This means that the output signals are levels instead of pulses. And these levels must be strobed into peripheral circuitry on the rising edge of the system clock. Consequently, the timing diagrams have been clarified by omitting the write/not-read (W/$\overline{R}$) output. The W/$\overline{R}$ signal follows the most-significant address bit timing. This simplifies the timing of critical-path signals, such as write pulses, and reduces ill effects of bounce and noise on level transitions. Unfortunately, peripheral devices (for example, standard SRAMs) require asynchronous input signals. It's challenging to derive these signals from the i486's synchronous interface.

In the basic-bus, single-read cycle for the 25-MHz i486—the slowest zero-wait cycle on Intel's slowest i486—the addresses become valid during the first cycle, while the data is sampled into the CPU at the end of the second cycle *(Fig. 1)*. The address isn't guaranteed to become valid until 22 ns after the first cycle starts. To support a zero-wait read, data must be valid at least 5 ns before the clock rising edge at the end of the second cycle. Any requirement for wait

SECONDARY CACHE FOR THE i486

states is indicated by the system taking the $\overline{\text{Ready}}$ input invalid (high) at least 8 ns before the clock rising edge of the second and subsequent cycles. Because the clock cycle time of the 25-MHz processor is 40 ns, the total time from a valid address to valid data is 53 ns ($2 \times 40 - 22 - 5 = 53$).

Another difference between the i486 and previous Intel CPUs is the use of a burst-mode transfer to refill cache lines. The i486 has a cache line size of 16 bytes, or 4 long words. The entire line must be replaced whenever a cache miss occurs. A burst sequence fetches four long words residing at adjacent memory locations into the i486's internal cache. Typical zero-wait, burst-read cycles are five clock cycles long *(Fig. 2)*.

As in the single read just described, the first cycle outputs the address to the system. During the second and following cycles (assuming no wait-states are used), data is input to the CPU, and the $\overline{\text{BRDY}}$ input is asserted to inform the CPU that the data transaction was finished accurately. The same sequence is followed for cycles three through five, except that the CPU changes its output address within the same cycle that the data is required.

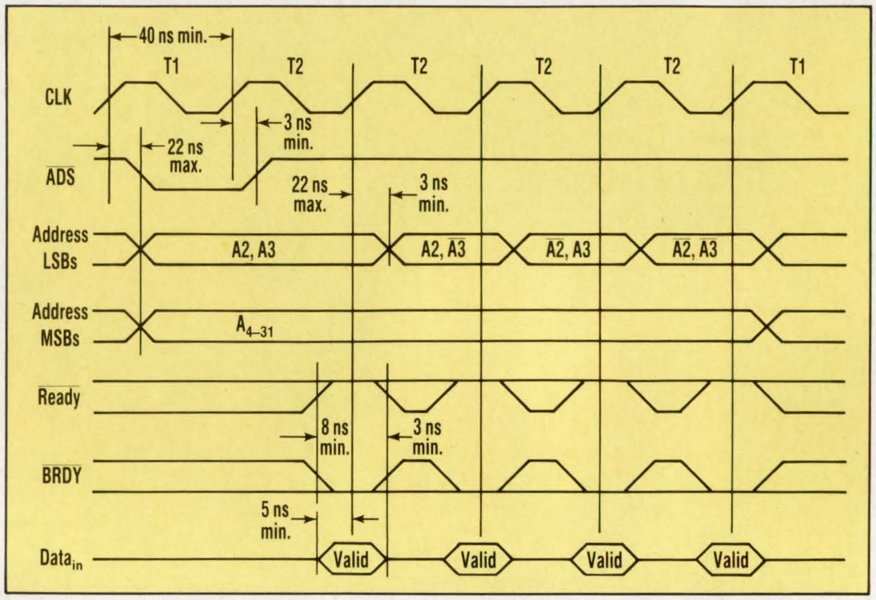
The timing on burst-read cycles and no-burst write cycles is somewhat tricky. On a 25-MHz i486, address outputs are guaranteed to be valid no sooner than 22 ns after the rising edge of the system clock. For data to be captured correctly, it must be presented to the CPU at least 5 ns before the clock rising edge. With the CPU's 40-ns minimum cycle time, this means that the cache memory would need to be designed to output burst data to the CPU in $40 - 22 - 5 = 13$ ns. At 33 MHz, this number drops to 9 ns, even without considering derating. Obviously, this speed requirement will keep designers from implementing a cache of an effective size by using standard SRAMs that are connected between the i486's address and data buses.

Fortunately, two things work in the cache designer's favor. First, all burst addresses share the same upper address bits. Only the lower two bits change during the burst transfer. Second, the initial cycle, during which the i486 outputs its first address, isn't the same cycle where data is first requested. This means that the 13 ns calculated can be added to an entire cycle time to get an initial access time of 53 ns in a zero-wait cache design. The initial access requirement matches what was mentioned previously for one read cycle.

Most designers take three routes when designing fast memories to support the i486. All three count on the extra time afforded by the first cycle to ease RAM timing requirements. The first method is to design the cache with a wide bus, which delivers all 16 bytes of the line simultaneously within the 53-ns window. Then, a simple multiplexer selects which long word will be routed to the CPU every cycle. Although this approach is simple and uses inexpensive, slower (35- to 45-ns) SRAMs, a typical version requires about 30 devices to implement. In fact, some designs consume half of a typical PC motherboard.

The second method requires no cache but adds wait states to the first cycle of a burst. As with the preceding example, the design uses a 16-byte word width and multiplexes the data to the CPU once it arrives. The difference is that this wide word is used as a main-memory bus, and the main memory's DRAMs are the weak link in the timing chain. As a result, the system should use very fast DRAMs to reduce the initial wait-states. A dedicated bus must be employed to support the wide word required by this approach. This makes such a design incompatible with most existing system bus architectures.

At this point, system designers experienced in working with nibble-mode DRAMs may wonder why these devices' sequential-addressing capabilities can't be harnessed to burst 32-bit data into the CPU once the burst cycle begins. One of the unique aspects of the i486 CPU is its peculiar bursting sequence. The sequence follows nibble-mode DRAMs only when the starting address is an even number. However, on odd-numbered addresses, the i486 counts down or even down, then up and down again. This means that nibble-mode DRAMs would not work in a



2. FIVE CLOCK CYCLES make up typical zero-wait, burst-read cycles. In the first cycle, the address is output to the system, and during the second and following cycles (assuming no wait-states are used), data is input to the CPU. The $\overline{\text{BRDY}}$ input is asserted to inform the CPU that the data transaction was finished accurately. The same sequence is followed for cycles three through five, except that the CPU changes its output address within the same cycle that the data is required.

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general enough manner to be usable in i486 burst cycles.

The third and most popular method of designing fast memories for the i486 is to build a cache with burst-count logic and a limited number of very fast SRAMs. This results in an effective cache size at a reasonable cost within a reasonable board space. Several existing designs employ fast 16k-by-4-bit static RAMs and implement a fast burst-address sequencer externally from the CPU in a very fast PLA. Such a design can be made to work because the i486 microprocessor has a predictable, if unusual, bursting sequence.

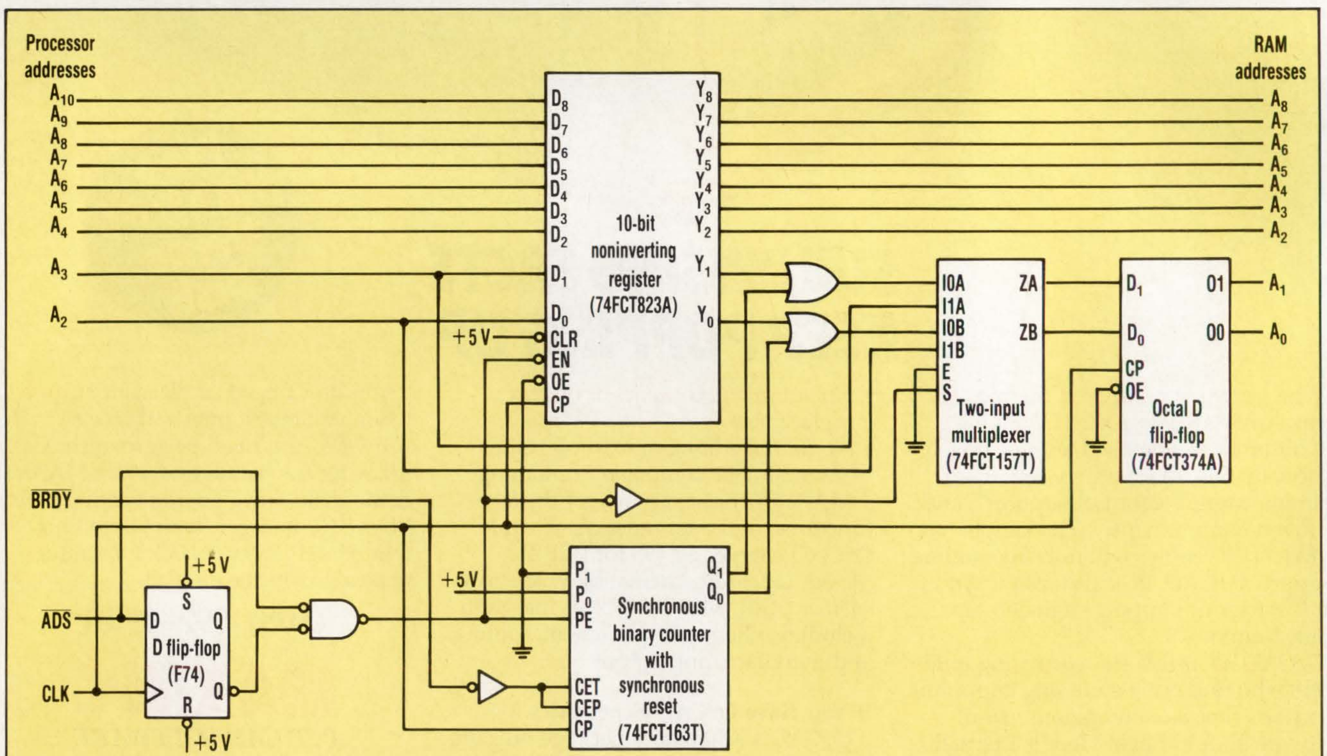
An i486-style counter can be implemented in discrete logic *(Fig. 3)*. The design is pipelined, where addresses are computed during the cycle before they're used. All of the cache addresses are latched into a 74FCT823A 10-bit noninverting register by the system clock during the cycle in which $\overline{ADS}$ first becomes active. The conditioned $\overline{ADS}$ signal also resets the 74FCT163T synchronous binary counter. In addition, the signal tells the 74FCT157T two-input multiplexer when to route addresses directly from the processor to the 74FCT374A octal-D flip flop, and when to take them from the burst address counter. The 74FCT163T counter outputs are exclusive-ORed with the original addresses to mimic the i486 burst sequence. The modified versions of the addresses are latched into the 74FCT374A latch on subsequent clock cycles.

If the PLA implementing this discrete logic can change addresses within 7.5 ns of a clock input and knowing that the CPU requires data 5 ns before the clock's next rising edge, a 25-MHz CPU could be supported with RAMs as slow as 40 – 7.5 – 5 = 27.5 ns, and a 33-MHz CPU would require 17.5-ns RAMs. In the future, as faster CPUs become available, this design becomes less attractive. Assuming that a 50-MHz CPU is used with a 5-ns PLA, it would still need SRAMs that boast an address access of only 10 ns, less derating. This clearly will push or even exceed the state of the art within the next year or two.

One simple alternative is to use a high-speed SRAM, into which an i486-style counter is absorbed. A counter can be implemented at the cost of only about 1 ns to the RAM's address access time by avoiding the need to translate internal logic signals to valid TTL levels and back again and by removing the requirement of driving highly capacitive DIP pins and interconnections. The IDT71589 32k-by-9-bit cache RAM is an example of such an SRAM. It supports a clock-to-data access time of as little as 15 ns.

WRITE-CYCLE TIMING

Another possible problem area on the i486 concerns write-cycle timing. About 50% of the I/O cycles of a typical i486 program are write cycles, because most of the device's read cycles will be absorbed by the internal cache. This means that cache designers need to focus as much attention



3. An i486-STYLE COUNTER can be built in discrete logic. The design is pipelined, where addresses are computed during the cycle before they're used. All of the cache addresses are latched into a 74FCT823A 10-bit noninverting register by the system clock during the cycle in which $\overline{ADS}$ first becomes active. The conditioned $\overline{ADS}$ signal also resets the 764FCT163T synchronous binary counter and tells the 74FCT157T multiplexer when to route addresses directly from the processor to the 74FCT374A, and when to take them from the exclusive ORs.

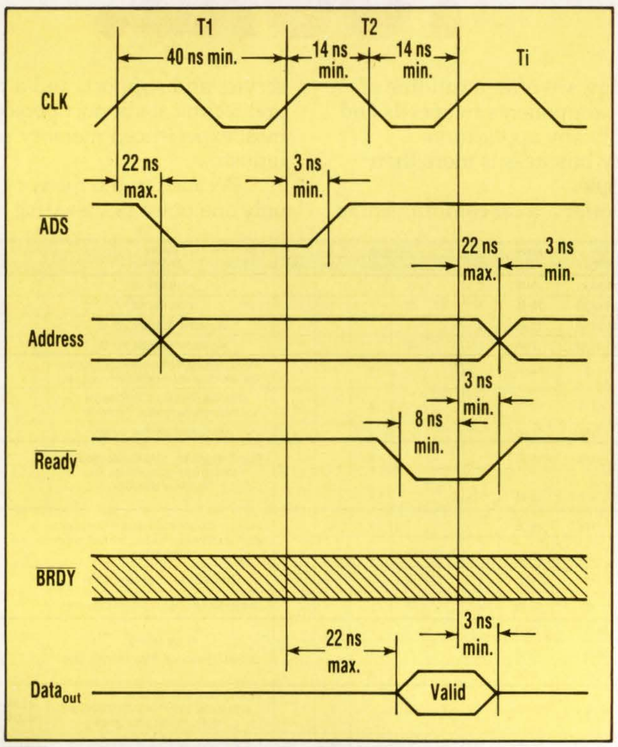
on the cache's write-cycle performance as on the read-cycle performance to maximize the cache's benefits. However, designing an i486 cache for zero-wait write cycles isn't as simple as it sounds.

The i486's zero-wait write cycle is similar to the zero-wait read, except that data is output from, rather than input to, the CPU. The W/$\overline{R}$ signal, which follows the timing of the address outputs, is held high for the entire write cycle *(Fig. 4)*.

For the cache-data RAM to support zero-wait write cycles, it must perform a write cycle within the tight constraints of the i486's timing. Here's an example based upon the 25-MHz i486 CPU: Because a 1x clock is used, most system designs would try to generate a write pulse from the system clock. The only question is whether to use the clock-high or the clock-low time to generate the write pulse.

Assuming that the clock-high time is used, the tag's output would be combined in a PLA or other fast logic element to produce a write pulse, which would be active for the first 20 ns or so of the second clock cycle. Unfortunately, the data isn't guaranteed to be stable out of the CPU until 22 ns after the rising edge of that clock cycle. This means that the data would not even be valid during the RAM's write pulse, unless the design supported a clock duty cycle other than 50%. Even if the minimum clock-low time of 14 ns were used (at the minimum clock period of 40 ns), there would be only 4 ns of overlap between the longer clock-high time and the data from the CPU. It's true that logic delays would cause the generated write pulse to overlap the data by more than 4 ns. But the minimum data setup time required by even a 12-ns RAM is 8 ns. Nonetheless, it would be difficult to absolutely guarantee that logic delays would consistently generate 4 ns of additional delay.

Thus ruling out the use of the clock-high time, the clock-low time should be explored. Now the address and data hold times become a problem. The i486 specification for this parameter is a minimum of 3 ns. If the write pulse is generated by gating the clock with any logic, the write pulse should stay valid after the i486's address and data stop being valid. Most fast SRAMs have a 0-ns data-and-address hold time. This figure would need to be a negative number to support a write pulse generated from a gated version of the clock-low cycle.



4. THE ZERO-WAIT WRITE CYCLE for the i486 resembles the CPU's zero-wait read. Data, however, is output from, rather than input to, the CPU. Furthermore, the W/$\overline{R}$ signal, which follows the timing of the address outputs, is held high for the entire write cycle.

From this example, it's clear that a synchronous RAM is needed in the design of zero-wait caches for the i486's synchronous bus. Few synchronous RAMs with TTL-compatible outputs are currently available. Most are offered only with ECL-compatible inputs and outputs. Of those with TTL I/O, certain timing and interface anomalies make most parts inappropriate for i486 designs. Only the IDT71589 chip has its pinout and timing matched to the i486—therefore it's the easiest to design into this kind of system.

Cache Specifications

Let's assume that the cache design will be implemented at a reasonable price and will consume little board space. Target operation requires all secondary cache "hits" to consume few, and preferably no, wait states. Naturally, every effort will be made to maintain the fastest allowable clock speeds by reducing capacitive loading wherever possible.

One rule of thumb in cache design is that an effective secondary cache must be about an order of magnitude larger than the primary cache. For the i486, the processor's internal 8-kbyte cache should be augmented with a secondary cache of about 80 kbytes. Two choices exist in this realm—64-kbyte and 128-kbyte caches. Using the previous example, a 64-kbyte cache could be designed with eight fast 16k-by-4 bits (nine, if parity were supported) plus a fast PLA (for the burst counter). Synchronous devices must be used to allow zero-wait write cycles. Should a synchronous 16k-by-4 be employed, this size cache could be built using about the same number of parts. It would be simpler and would consume less board space to design a 128-kbyte cache with the IDT71589 32k-by-9-bit device. This is because only four of these devices would be necessary even in a system with parity support, and synchronous writes would be offered.

It's generally accepted that an n-way set-associative cache offers a higher hit rate than a direct-mapped cache of the same size. However, there are three key reasons to avoid implementing an n-way cache.

The first reason is cost. An n-way

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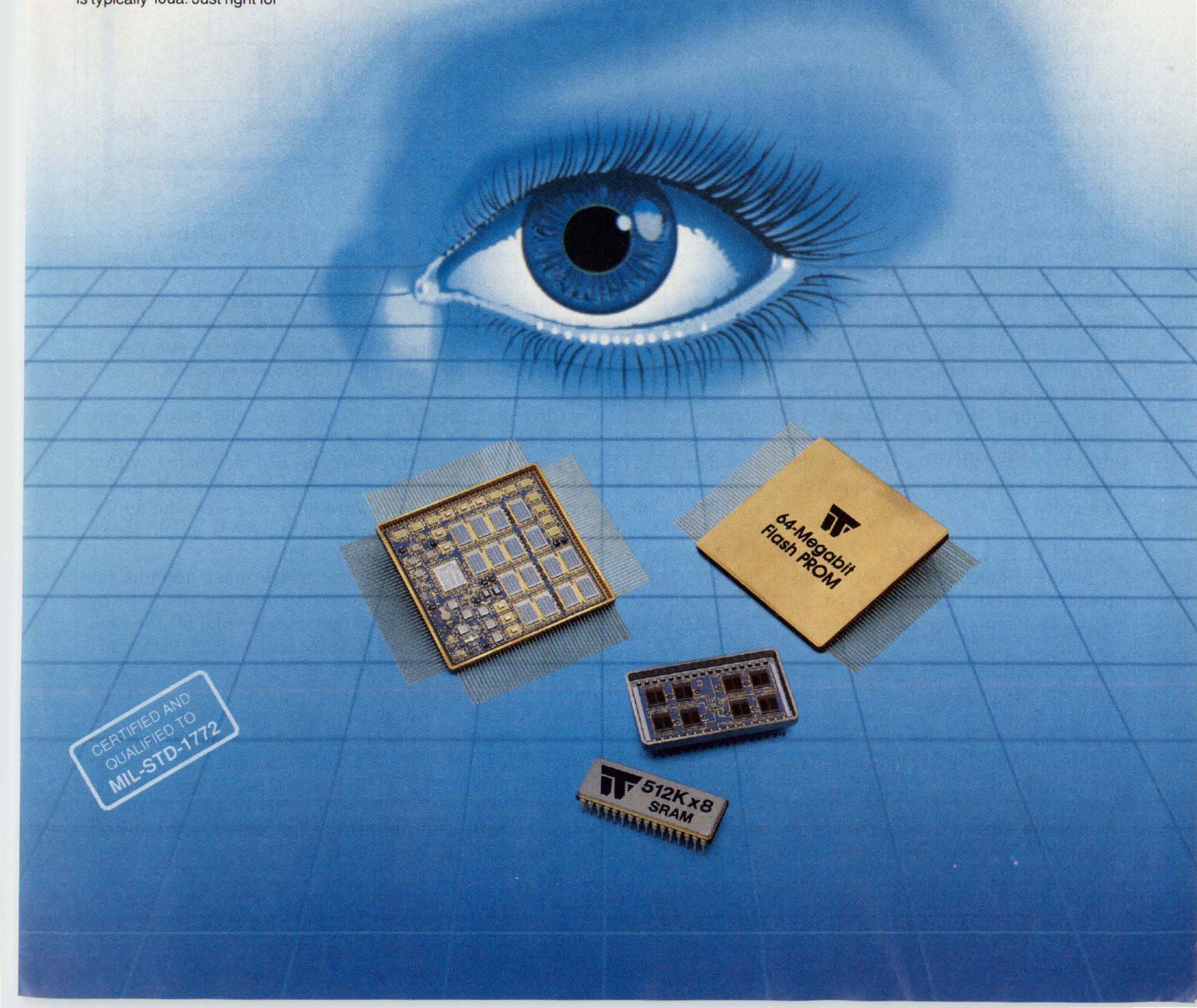
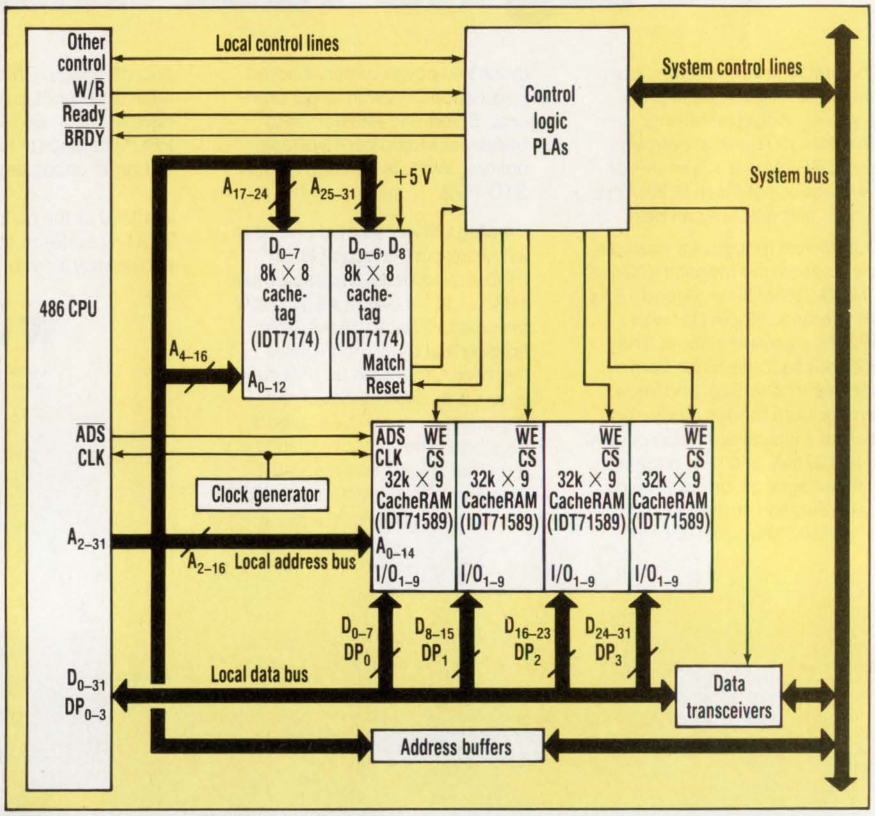


cache must start every cache cycle with the cache-data RAMs' outputs disabled. Only after the tags decide which RAM contains the appropriate data can the outputs be enabled for one of the data RAMs. The address-to-data critical path of the cache runs from the tag, through logic, and through the data RAMs' Output Enable pins. This requires a fast cache-tag RAM, which is usually costly. In a direct-mapped cache, the data RAMs' outputs are enabled onto the data bus as a default and are disabled only after a cache miss. The critical path in this system runs from the cache-tag RAM, through logic, and allows the cache-tag to be around 10 ns slower. Subsequently, it's much less expensive than in the n-way design.

The second reason is board space. A typical n-way cache design requires n cache-tag RAMs and n sets of data RAM, which typically doubles cache chip count for two-way and quadruples it for four-way. The cost in board space is obvious. The third reason is address loading. All cache-tag RAMs and cache-data RAMs must be either tied directly to the CPU's lower order address output pins or specified about 10 ns faster and tied to the bus through a buffer. Because of this, designers must either use even faster tags or find a way around the derating delays caused by overloading the CPU's address bus. For all three reasons, the example cache is a direct-mapped design *(Fig. 5)*.

SELECTING LINE SIZE

Line-size selection is another important consideration in cache design. To keep the cache design as simple as possible, the secondary cache in this example uses the same size line as the i486 *(Fig. 5, again)*. With this choice, a copy-back implementation can use the fact that the Cache RAM's internal counter wraps around and counts again after completing its count sequence. Clever designers use this feature to offload a "dirty" cache line to a write buffer while priming the system bus for a read cycle. When the bus finally responds, data can be written immediately to both the CPU and the cache during the following four cycles. The IDT71589 can move from a burst-read to a burst-write mode simply by changing the state of the Write Enable input. Even in simpler write-though caches, the internal counter simplifies line refills by using a cache line of the same length for both primary and secondary caches.



5. CPU ADDRESS OUTPUTS A_{2-16} **are tied to Cache RAM address inputs** A_{0-14}**, because the CPU's address outputs** A_0 **and** A_1 **are used only for byte and word manipulation during 8- and 16-bit accesses. Since this cache supports 32-bit transfers,** A_0 **and** A_1 **aren't needed. The cache-tag RAM observes only address bits** A_{4-31} **because each tag is responsible for a four-doubleword (16-byte) cache line. The most significant bit of the cache-tag data input is tied high as a "valid" bit. After the tag is reset at power-on or during a cache flush, this input is compared with a 0 in the corresponding RAM bit to cause a cache miss.**

Line size directly influences the cache-tag depth chosen for the cache. The cache-tag RAM must be deep enough to contain one location for every line in the cache-data RAM. Some systems minimize the number of tag-RAM bits by having tag address bits only for every fourth or eighth line and a separate valid bit for each line. With the cache-tag RAMs currently on the market, it's simpler and actually costs less in address loading and chip count to use one tag location for every line. For the example *(Fig. 5, again)*, with a 32k-deep cache-data RAM and a four-word-long line size, the appropriate cache-tag RAM would be 8k locations deep.

The tag width must account for any remaining address bits used by the system, plus a valid bit for each line. It's rare for a system to support the entire 4-Gbyte address range offered to i486-system users, so many designs discard some of the address bits. In this sort of design, there's no need for the cache-tag to examine bits that won't be referenced anywhere else in the system. Of the 30 address outputs used when addressing long words in a system, the lower two define the long word within the line and won't be used as inputs to the cache-tag RAM. The 8-k-deep

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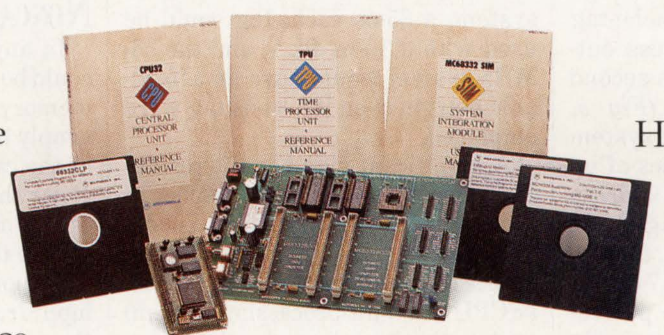

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cache-tag described in the preceding paragraph uses the next 13 address bits on its address input pins. One readily available cache-tag that matches this depth requirement is the IDT7174, an 8k-by-8 resettable tag RAM, which currently runs as fast as 30 ns.

If one of the IDT7174's data pins is used as a valid bit, with the seven remaining bits tied to the next more-significant address outputs, a 16-Mbyte main memory address range can be supported with one cache-tag chip. Eight more i486 address outputs could be supported by a second IDT7174, as in this design *(Fig. 5, again)*. This would allow the system to support main memory sizes of up to the CPU's full 4-Gbyte address range. Although other tag-RAM configurations are available, they're all less dense than the IDT7174. Subsequently, they present the processor's address bus with a drastically higher load to support the same number of tag bits. This usually means that the cache-tag RAM's address inputs would need to be buffered, at a cost of 5 to 10 ns. Designers using future i486 speed grades would be forced to use much faster cache-tag RAMs at a much higher cost. The IDT7174 offers the lowest board-space consumption and capacitive loading of any cache-tag RAM currently available.

SNOOPING THE BUS

Speed requirements of a cache-tag RAM in a direct-mapped cache are easy to calculate if self-timed cache-data RAMs are used. The equation is straightforward. First, a zero-wait cache must tell the i486 in two cycles that its data is available. During the first cycle, the CPU outputs the address, and in the second cycle, the cache must respond. From these two clock cycles, the clock to address delay must be subtracted, as well as the $\overline{\text{BRDY}}$ setup to clock time. Finally, the PLA's propagation delay is subtracted to show the required access time of the cache-tag to be used.

Fortunately, on the IDT71589 CacheRAM, the Write-Enable input sports timing identical to the timing of the i486's $\overline{\text{BRDY}}$ and $\overline{\text{Ready}}$ input pins. Therefore, no additional restrictions need to be put on the cache-tag's timing to accelerate write hit cycles, as would be required with the use of asynchronous RAMs. Assuming that designers use 7-ns PLAs downstream of a cache-tag to drive the $\overline{\text{BRDY}}$, $\overline{\text{Ready}}$, and Write Enable pins of the i486 and IDT71589, respectively, cache-tag requirements will be $(40 \times 2) - 22 - 6 - 7.5 = 44.5$ ns at 25 MHz. At 33 MHz, it's $(30 \times 2) - 16 - 5 - 7.5 = 31.5$ ns. In the 25-MHz system, a 35-ns cache-tag could be used with a 10-ns PLA, and the 33-MHz system would have an affordable margin even if a 30-ns tag were employed.

A significant side benefit results from using an external cache to "snoop" on the system bus. Snooping ensures that there aren't any writes from a DMA device (or another CPU in a multiprocessing system) on data that's replicated in the cache. On a snoop-hit, cache data should be either invalidated or updated. The i486 serves this need by either allowing the external system to flush the on-chip cache or to stop the CPU and drive addresses into the CPU to invalidate a single line in the on-chip cache.

Naturally, a cache flush bogs down the CPU from the time it's invoked until the cache can again be refilled from external memory. But if the CPU was stopped for a line invalidate every time a DMA device performed a main memory write, the CPU could be stopped often enough to seriously degrade system performance. The secondary cache's tag RAM can be set up to screen invalidate cycles to the CPU by using the principle of inclusion. This allows the CPU to be stopped for invalidation only at those addresses when it's probable that the address being written actually exists within the i486's internal cache.

The principle of inclusion requires that the external cache attempt to invalidate a corresponding line in the i486's internal cache every time a line is invalidated in the secondary cache. By performing this simple trick, the external cache-tag always contains a superset of the addresses in the internal cache-tag. Now, if the external cache-tag is used during idle cycles to monitor the write-cycle traffic on the system bus, it flags only those writes that could require a primary cache invalidation. Those bus writes cause an invalidation on the secondary cache, and a subsequent attempted invalidation on the primary cache. Coherence will be maintained with minimal impact on the CPU's performance.

NONCACHEABLE ADDRESSES

In any cache design, I/O devices could be mapped into the CPU's main memory space. This can be dealt with simply by blocking the match output of the cache-tag with an address decoder that recognizes the addresses of the memory-mapped I/O devices before the cache has an opportunity to respond. This can be handled by an input from an I/O address decoder to the logic between the tag and the CPU's $\overline{\text{Ready}}$ and $\overline{\text{BRDY}}$ inputs.

Although the final cache design consumes only four SRAMs, two cache tags, and various PLAs and random logic, it is a full, 128-kbyte, direct-mapped, zero-wait design. Either a write-through or a copy-back cache can be implemented with this basic design: The only difference is the sophistication of the PLA-based cache-controller state machine and the addition of an 8k-by-1 "dirty-bit" RAM (not shown) to express the status of each line in the cache. The low chip count keeps capacitive loading to a minimum and derating is avoided. Both the tag and the data RAMs come in narrow J-lead, SOIC packages, so board space for the entire cache is only a few square inches.□

Jim Handy, strategic marketing manager for Integrated Device Technology, received a bachelor's degree in electrical engineering from Georgia Institute of Technology and an MBA from the University of Phoenix.

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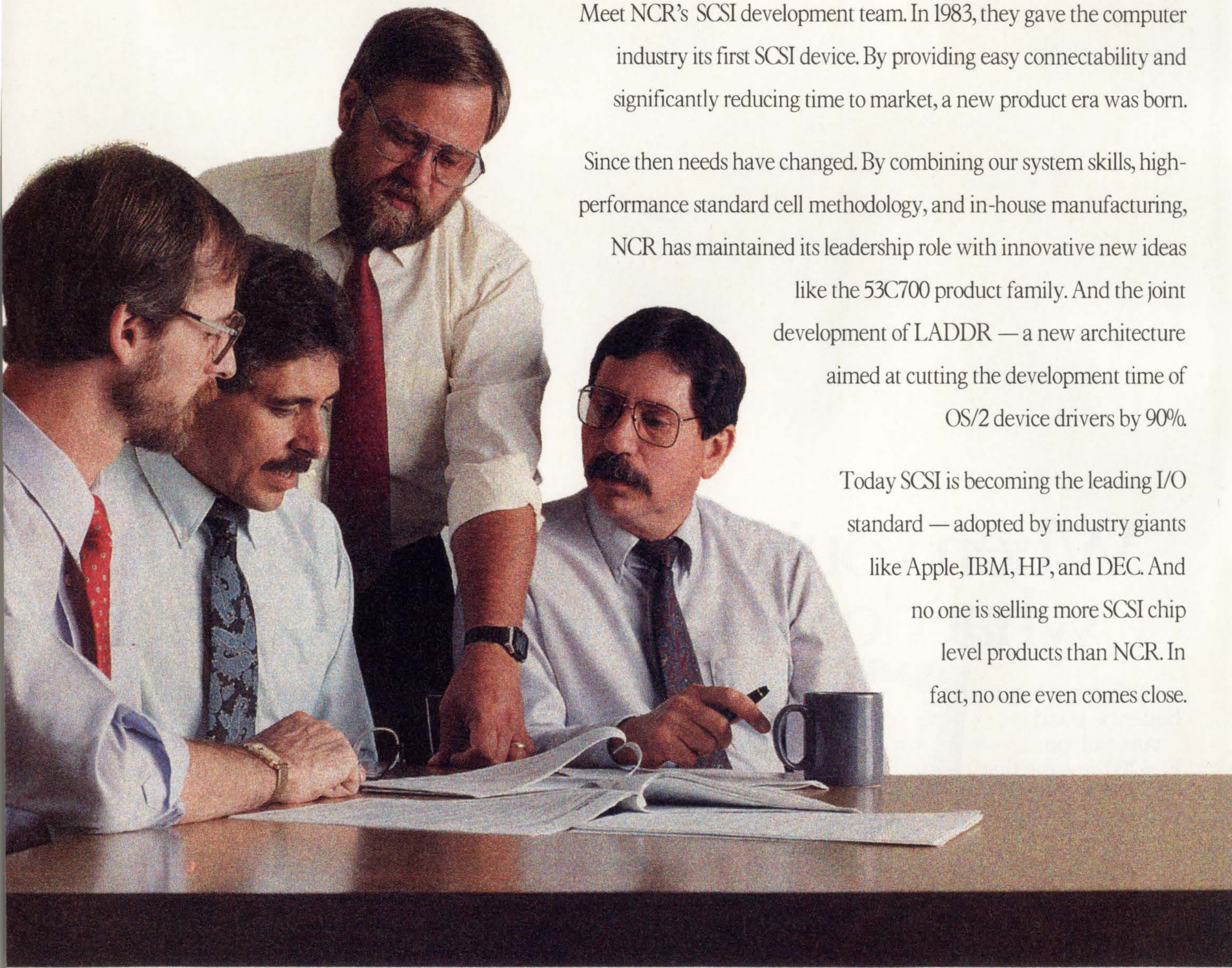

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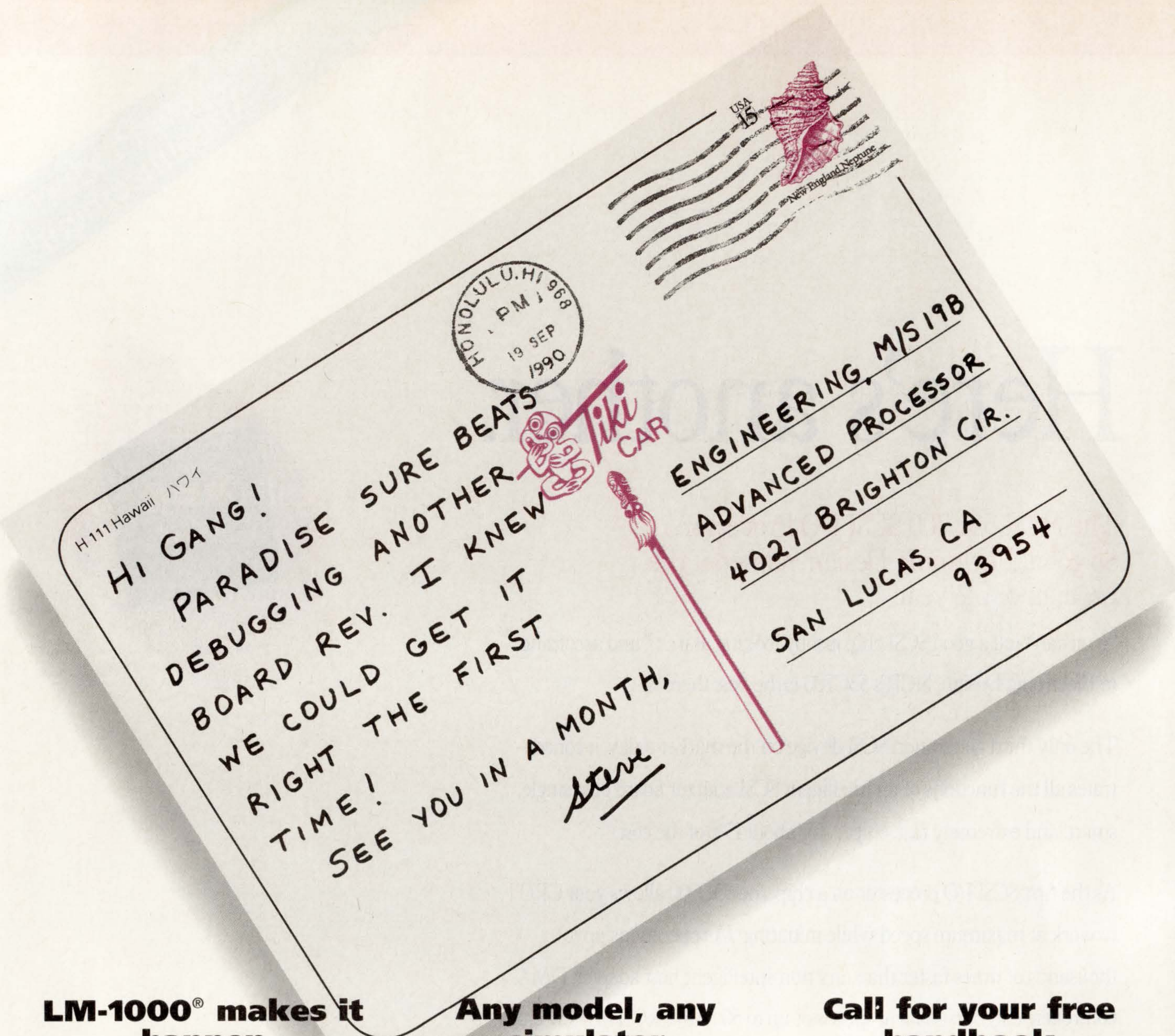

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CIRCLE 211

Simulation Sorts Out System Schemes By Surveying Trade-offs

A Hardware Modeler Helps To Accurately Predict The Performance Of A Microprocessor-Based Board.

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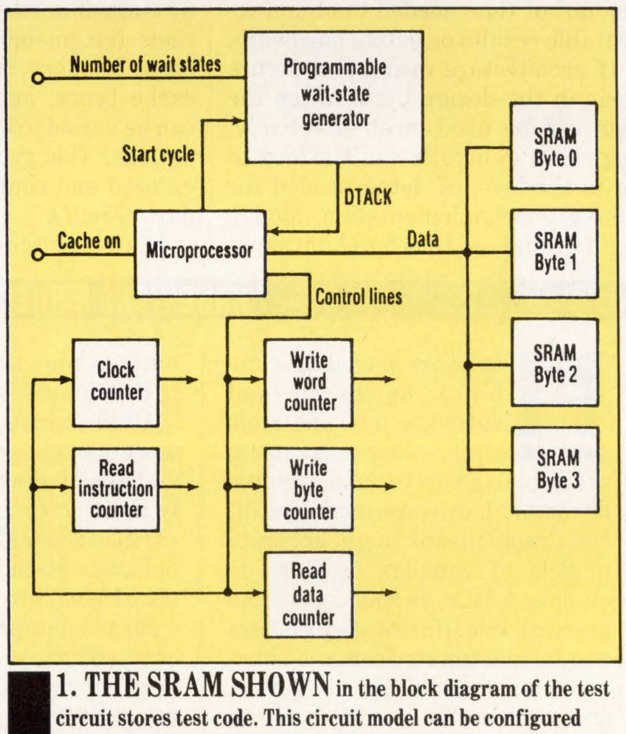
(216) 449-6700.

In a microprocessor-based system design, engineers strive to reach the best balance between performance, cost, design time, reliability, and board space. However, the data needed to accurately predict a microprocessor's performance in a design is usually unavailable. For design optimization, engineers need a way to calculate the trade-offs between various microprocessors and memory structures over a wide range of parameters.

Formerly, breadboarding the prospective designs was considered the only real alternative. However, breadboarding is difficult, expensive, and time-consuming. These cost and time factors can limit experimentation to only one or two design ideas.

Simulation, which has been used successfully for post-design verification, also holds promise for pre-design evaluation. Ideally, engineers would prefer to run actual code or a suitable benchmark on a wide variety of system models—many more variations than would be practical to evaluate on a breadboard. However, simulation wasn't used for this application because of the prohibitive amount of time required to execute code on a simulated system. But if engineers choose and refine appropriate test code, and focus on exploring specific design questions rather than attempt a full-system implementation, simulation can yield valuable data. It can also cost-effectively quantify architectural trade-offs for many design ideas.

A design team at Allen-Bradley Co. used simulation to evaluate the Motorola 68020 and 68030 microprocessor



1. THE SRAM SHOWN in the block diagram of the test circuit stores test code. This circuit model can be configured during simulation to represent different designs.

EVALUATING DESIGN TRADE-OFFS WITH SIMULATION

architectures for a specific application. This pre-design evaluation was performed in a matter of days, and produced critical information for making design trade-offs.

The Allen-Bradley design project involved a 68020-based board. The team wanted to evaluate whether upgrading from a 68020 to a 68030 would improve the price/performance ratio. The areas of interest were microprocessor speed and memory-architecture efficiency. The Dhrystone 2.1 benchmark was one of the tests chosen to evaluate relative system performance.

The key to getting accurate results from simulation is the timing resolution. The simulator is accurate to a fraction of a microprocessor clock cycle, whereas an actual system requires averaging results to compensate for the system clock's inaccuracies (50 to 60 ms). In this case, simulation results matched the test code results produced on the actual system to within 1%. Each configuration's simulation runs in about 20 min. because of intelligent design of the test circuit, test-code compaction, and using the inherent accuracy of simulation to limit run times. Twenty minutes is about the same amount of time needed to obtain repeatable results on actual hardware.

If architecture evaluation occurs early in the design cycle, when the data can be used most effectively, engineers generally can't afford to go to the level of detail needed for full-system implementation. Modeling time and run times prohibit simulating full systems. The most convenient option is to create a test circuit simplified to evaluate the design problems that are of most interest to engineers.

TABLE 1. ONE-PASS TEST SEQUENCE

68020 Internal caches on, cold start, 1 pass

Wait states	0	1	2	4	8	16
Clock cycles/Dhrystone	4888	5665	6512	8143	11759	19470
Read cycles	698	686	726	726	726	726
Instruction reads	376	364	404	404	404	404
Data reads	322	322	322	322	322	322
Longword writes	138	138	138	138	138	138
Byte or word writes	102	102	102	102	102	102

In the Allen-Bradley case, a test-circuit model was designed to evaluate the relationship between the microprocessor and the memory scheme. This circuit model has only a few schematic pages, and uses library models created by the company's engineers. It was designed for maximum flexibility, giving the engineers a way to vary architectures through the simulator without changing the circuit model itself. When simulating this circuit, the engineers could vary parameters quickly without being constrained by current device and process limitations (i.e. memory speed, memory size). Memory speeds, cache sizes, cache types, and processor speeds can be varied to explore many design options. This type of design can be entered and simulated in just a few days *(Fig. 1)*.

The test circuit contains a microprocessor, 1-Mbyte of static RAM (SRAM) to store the test code, a series of counters, and a programmable wait-state generator. The microprocessor is a hardware model, which incorporates the actual device into simulation. The rest of the circuit elements are simulation library models created by the engineers with schematic editing tools from Valid Logic Systems, San Jose, Calif.

The simulation ran on a Sun 3/60 workstation configured with 8 Mbytes of local memory, connected via Ethernet to the LM-1000 hardware modeling system from Logic Modeling Systems Inc., Milpitas, Calif. Allen-Bradley engineers employed Valid Logic's ValidSim 3.15 simulator, and entered schematics through the ValidGED design editor. Designing the test-circuit model, creating library parts, modifying test code, and entering the schematics took about six engineer-days.

No model-development time was needed because the microprocessor hardware models were obtained from Logic Modeling. The hardware

HARDWARE MODELS ENSURE ACCURACY

Hardware modeling combines hardware and software into one modeling solution. By using the actual device to model its own behavior, hardware modelers offer a rapid means to get accurate models of complex devices, including ASICs, as soon as devices are available. Hardware modelers can format inputs from the simulator, evaluate device behavior, and return the resulting device outputs plus timing information, to the simulator.

Unlike software models, hardware models are fully functional and exhibit device behavior exactly as it occurs, including nonlinearities and undocumented device behavior. Because hardware models of complex standard devices, such as microprocessors, can execute software, they're a logical choice for running benchmarks or for performing hardware-software integration.

A hardware model library of over 600 VLSI components is available from Logic Modeling Systems Inc., Milpitas, Calif., for the LM-1000 universal hardware modeler. The LM-1000 (which was used in this example) operates with a wide range of standard logic simulators. Therefore, engineers can share hardware models among the various simulators used by a design group.

EVALUATING DESIGN TRADE-OFFS WITH SIMULATION

models executed the test code accurately *(see "Hardware models ensure accuracy," p. 86)*.

Rather than create a different design for each variation in architecture, engineers use a generalized circuit model that can be configured dynamically. With no wait states imposed, the test circuit represents the fastest memory scheme under consideration. The programmable wait-state generator model enables engineers to alter memory architectures by adding the wait states that are typical of each architecture. This is done by changing input-signal values only. Then the simulation script file, which controls the simulation, can alter the design automatically, without recompiling the circuit. This allows engineers to model variations in memory speed, cache size, and bus width. By varying these architectures, the performance of each microprocessor for various memory designs can be viewed.

The microprocessor in the test circuit activates the programmable wait-state generator when it begins a bus operation. This generator produces wait states requested by the engineer in the simulation script, and then sends an acknowledge signal to the microprocessor. In the Allen-Bradley project, the acknowledge is sent through the DTACK pin. The microprocessor then continues its operation, accessing the test code stored in the SRAMs. The counters monitor the control lines from the microprocessor and record the number of clock cycles and memory cycles.

Designs are configured dynamically with a specially designed 24-bit multiplexed shift register in the programmable wait-state generator block. This can supply a different number of wait states for read, longword write, and non-longword write operations.

Within the simulation script (a list of commands to the simulator), engineers specify the desired combination of wait states to the programmable-wait-state generator, and indicate whether a particular test should be done with the microprocessor's internal cache on or off. The combination of wait states produces the appropriate speed for each memory scheme. In this example, as many as 26 designs, each with different wait-state combinations, are simulated in one session.

Dynamically configured wait states can also be used when evaluating different types of memory—SRAM, dynamic RAM (DRAM), and ECC DRAM (error-correcting memory)—for a given microprocessor design. SRAM is used as the base case. Then it's made to resemble dynamic memory by changing the acknowledge delays and including a timer to disable access to memory during the refresh cycles required by DRAM. This variation's simple implementation shows how a programmable-wait-state test circuit can be used in various evaluation procedures.

Fine-Grain Tools

Performance statistics depend heavily on the system in which the microprocessor resides. The statistics are rarely given for anything but the most optimal design case. The average number of clock cycles per memory fetch is seldom reported even though it's one of the most important parameters that an engineer considers when designing a memory interface to a microprocessor.

Measurement tools for the microprocessor test circuit were modeled to count clock cycles; read instructions; and non-byte-write, byte-write, and read data operations. The counters are started and stopped with the simulation script file. Counter data characterizes the rate and type of fetches per cycle. The resulting data, in turn, is used to compute internal cache hit rates and the memory bandwidth. The cache hit rate tells engineers how often external memory access is required. The memory bandwidth is the amount of information traveling across the memory bus per second. Both of these quantities aid engineers in creating the best memory design for an application.

When selecting test code, its size and complexity should be scrutinized. Ideally, actual system code should be used in the system comparison to give engineers an accurate measurement of system performance for that specific application. However, large, complex applications require too much simulation time. Therefore, running system code, such as an operating system, may be impractical.

Standard benchmarks can be used to measure system performance. The Dhrystone benchmark is a synthetic benchmark. It was chosen as one of the benchmarks used to compare 68020 and 68030 performance because this benchmark can be simplified for simulation, and is well known to most engineers.

Preparing test code calls for reducing the code to the minimum length possible without lowering the accuracy of the results. For the Dhrystone benchmark, minutes of CPU time are typically required to achieve an accurate result on a typical workstation. On the system under consideration, 3 million passes of the Dhrystone code were needed to achieve a repeatable result. Allen-Bradley engineers used two main strategies to reduce run times: eliminating unnecessary code and limiting test-code iterations.

The test code was compacted by eliminating non-critical code. To trim code and preserve the accuracy of the test results, only code residing outside the actual testing section was eliminated.

The setup phase of the Dhrystone benchmark was reduced by removing the C language function calls—scanf and printf—that required large C libraries and a large amount of memory. Hard-coding the number of tests to be run also reduced the setup phase. While this changed how the hard-coded value was stored in memory, the overall execution time was hardly affected because this value was accessed only once per iteration. The extensive pre- and post-test reporting and printing operations usually performed during this benchmark were purged in favor of extracting the desired information from the simulator's results. The compacted benchmark is roughly 80% smaller than the original code.

The key to running test code on a simulator is to utilize the simulator's

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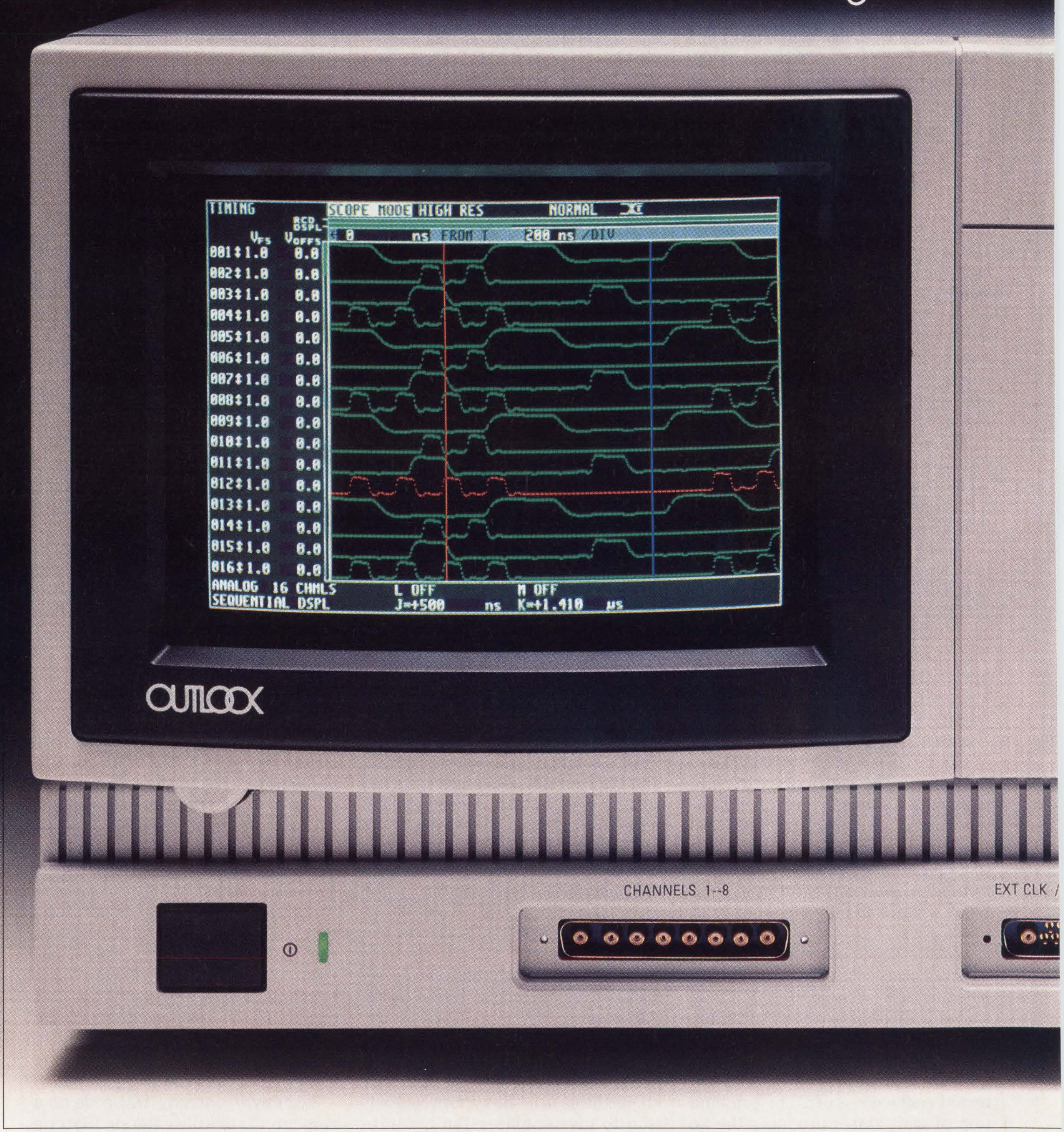


EVALUATING DESIGN TRADE-OFFS WITH SIMULATION

inherent accuracy to minimize the simulation time required to perform the system evaluation. Long run times are essential because of the limited timing accuracy of actual systems. Counters within actual systems rely on the system clock, which is typically restricted in accuracy to 1/60th of a second. Engineers must run iterative benchmarks repetitively until the uncertainty due to the system clock is negligible. In this example, the test code may typically have to run on an actual system thousands of times before a reasonable degree of accuracy is reached.

A simulator can determine time down to a fraction of a clock cycle, therefore it's not limited by the accuracy of a system clock. If exact start and stop times are known, only one iteration is needed to obtain accurate test-code execution times.

In the Allen-Bradley example, the number of passes of the Dhrystone benchmark test were reduced from the thousands ordinarily required on an actual system to only three passes run on the simulator. As a result, the benchmark simulated in less than 1 ms of actual CPU time. The simulator could run in a time comparable to the time required to achieve repeatable results (3 million iterations) on an actual system.

The benchmark's execution can be divided into five main phases: start, set up, test, reporting, and end. These phases are common to many types of benchmarks. If the exact start and stop times of each phase were known, only one pass would be needed to determine performance. However, these times can't be determined precisely. The problem was avoided in the Allen-Bradley example by eliminating the uncertainty in timing of the start, setup, reporting, and end phases.

The first step was to perform one pass through the benchmark *(Table 1)*. This was a "cold pass" because the cache was empty and some of the test's time was invested in loading the cache. The time to complete all phases, from start to end, is the single-pass time interval.

The second step was to run two passes of the performance test sequence *(Table 2)*. After running the identical start and setup sequences, a cold pass of the test phase was run. A second iteration of the test, a "warm pass," was then run. At this point, the caches were loaded from the previous cold-pass run, so the warm pass showed the system's performance in a steady-state condition. After the warm pass, the reporting and end phases were performed, just as in the single-pass benchmark.

The ultimate goal is to land the warm-pass time in order to calculate the Dhrystone rating. The warm-pass time is obtained by subtracting the single-pass time from the two-pass time *(Table 3)*. All timing uncertainty due to the start, setup, reporting, and end phases is eliminated. The cold-pass time is also eliminated because this test code is usually run through thousands of iterations, making the cold-pass time of the first iteration insignificant. In the end, the warm-pass time remains. As a result, only two iterations of the start, setup, reporting, and end phases, and only three full iterations of the test sequence were needed. The resulting benchmark test code ran in about 12,000 clock cycles.

To ensure that this compaction didn't reduce the accuracy of the results, the same benchmark was run for 3 million passes on existing system hardware. The simulated results were within 1% of the measured results on system hardware. The time required was also comparable: 15 to 20 min. of running actual hardware versus 20 min. of simulation run on a Sun-3/60. Achieving this degree of accuracy with a reasonable execution time made architectural evaluation practical.

The procedure to run the test code on a simulated design requires converting the code into a simulator-dependent format, then loading it into the memory models. Conversion tools were created to simplify and speed the process of modifying the executable code and loading it in the simulated system.

The first step in performing the simulation was to create the simulator script. This script loaded code into memory, supplied the desired number of wait states to the programmable-wait-state generator, started and stopped the counters, started and stopped the code's execution in simulation, recorded results and elapsed time, and restarted the procedure using a different number of wait states. After the C source code for the test code was compiled

TABLE 3. WARM-PASS RESULTS

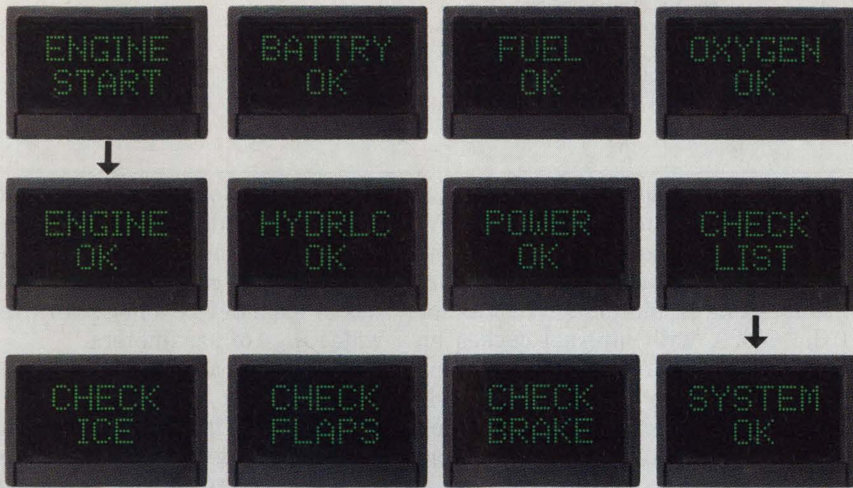
68020 Internal caches on, warm pass (cold 2 pass – cold 1 pass)

Wait states	0	1	2	4	8	16
Clock cycles/Dhrystone	3765	4406	5108	6451	9307	15370
Read cycles	572	560	600	600	600	600
Instruction reads	330	318	358	358	358	358
Data reads	242	242	242	242	242	242
Longword writes	119	119	119	119	119	119
Byte or word writes	40	40	40	40	40	40

TABLE 2. TWO-PASS TEST SEQUENCE

68020 Internal caches on, cold start, 2 passes

Wait states	0	1	2	4	8	16
Clock cycles/Dhrystone	8653	10071	11620	14594	21066	34840
Read cycles	1270	1246	1326	1326	1326	1326
Instruction reads	706	682	762	762	762	762
Data reads	564	564	564	564	564	564
Longword writes	257	257	257	257	257	257
Byte or word writes	142	142	142	142	142	142



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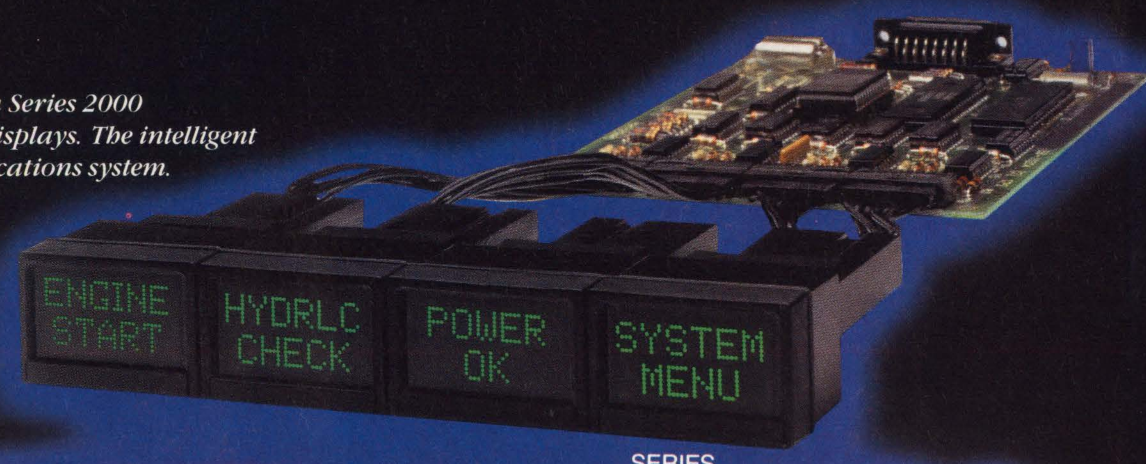

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EVALUATING DESIGN TRADE-OFFS WITH SIMULATION

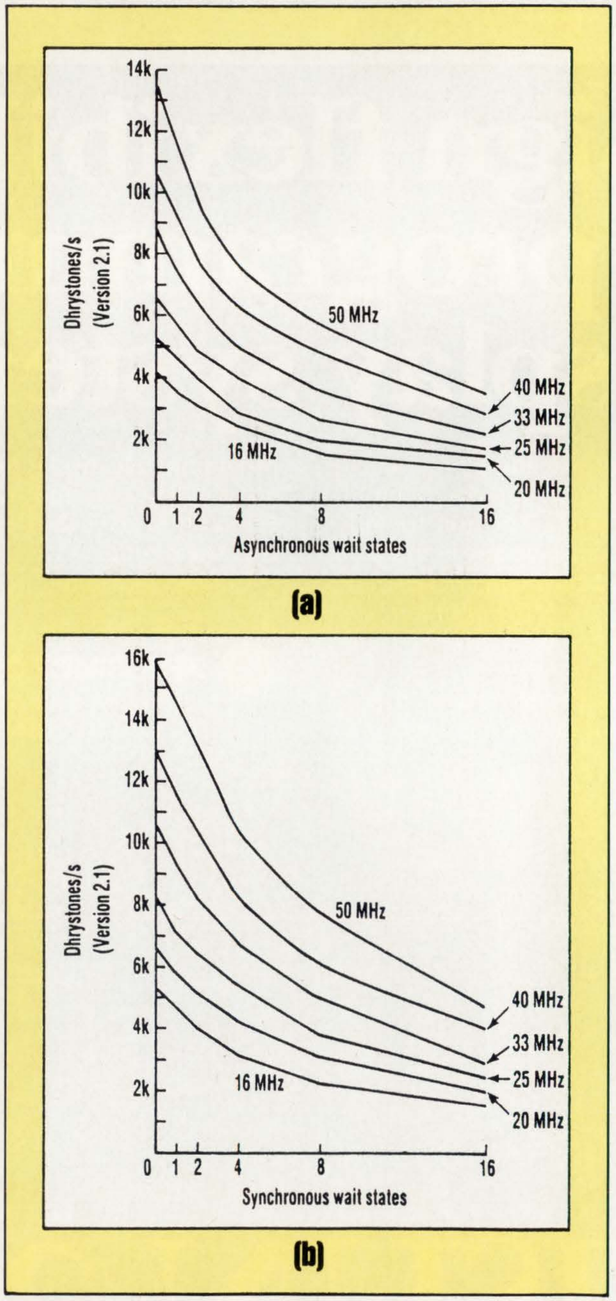
and linked, the executable file was converted to a downloadable Motorola S-records format. This file was then divided into four parts, transformed into a hexadecimal format file and loaded through a simulator routine into the four SRAM memory models.

The Dhrystone program was compiled and tested on the workstation before downloading to the simulation system. With translation utilities, changes were made in the source code and simulation began with the new executable code inside of 5 min. Each evaluation required about 20 min. to perform. For the 68020, engineers could evaluate 0 to 16 wait states in 6 hours and 18 min. For a 68030, the same evaluations required 5 hours and 35 min. As a result, simulation for architectural evaluation required less than one day per processor. The results enabled engineers to select the appropriate architecture for the design.

Revealing Results

Ideally, comparisons between the internal architectures of the 68020 and 68030 should be made at all available clock rates and desired wait states. Tests were run on the 68020 with 0 to 16 asynchronous wait states for memory access, and on the 68030 with 0 to 16 asynchronous and synchronous wait states. These tests confirmed that the 68030's asynchronous wait states are one wait state longer than the synchronous wait states. All of these tests were performed with the microprocessor's internal cache enabled and, in different runs, disabled to determine the cache hit rate. Tests were also performed with compiler register-optimization enabled and disabled.

Using hardware models of the microprocessors yielded highly accurate results *(Table 3, again)*. The simulation results revealed subtle variations in device behavior. For example, warm-start Dhrystone 2.1 simulation results for the 68020, with internal caches on and with registers, show an unexpected increase in instruction reads with two wait states. This variation in device behavior stemmed from prefetching operands while the 68020 executed a forward branch instruction. By using hardware models, engineers could learn the subtleties of each device's behavior over a wide range of parameters.



2. PERFORMANCE-COMPARISON GRAPHS show the number of Dhrystones/s calculated for the 68020 (a) and for the 68030 (b). The horizontal axis represents the memory speed given as the number of wait states.

The warm-pass time holds the key to calculating the design's Dhrystone rating. One Dhrystone equals the time the design requires to execute one test pass. When the Dhrystone benchmark is run on an actual system, only the first pass is a "cold pass." If the first pass is also assumed to be a warm pass, the margin of error is only:

$$\frac{\text{Cold pass time - Warm pass time}}{\text{Number of Passes}}$$

Determining the number of Dhrystones the design can execute per second from the warm pass time is trivial.

This benchmark is run independently of clock speed, so the effects of clock speed on performance must be calculated to attain performance-comparison graphs *(Fig. 2)*. To calculate the expected Dhrystone rating for a design, divide the clock frequency by the number of clock cycles per Dhrystone, which is determined during the benchmark. Repeat the calculation for different wait states by dividing each clock frequency by the clock cycle total for the given number of wait states.

For example, consider a 68020 system with 0 wait states and register optimization enabled. During simulation, this processor and memory configuration required 3765 clock cycles per Dhrystone. To determine the Dhrystone rating for each speed of the 68020 processor, divide each speed by 3765:

50 MHz $\div$ 3765 cycles per Dhrystone
= 13280 Dhrystones/s

DESIGN APPLICATIONS

EVALUATING DESIGN TRADE-OFFS WITH SIMULATION

TABLE 4. CALCULATED CACHE HIT RATES

Dhrystone 2.1 registered (warm start behavior)		
68020	Internal cache read cycle hit rate: Internal instruction cache read cycle hit rate:	32% 45%
68030	Internal cache read cycle hit rate: Internal instruction cache read cycle hit rate: Internal data cache read cycle hit rate:	57% 46% 86%

40 MHz ÷ 3765 cycles per Dhrystone = 10,624 Dhrystones/s

33 MHz ÷ 3765 cycles per Dhrystone = 8765 Dhrystones/s

25 MHz ÷ 3765 cycles per Dhrystone = 6640 Dhrystones/s

20 MHz ÷ 3765 cycles per Dhrystone = 5312 Dhrystones/s

16 MHz ÷ 3765 cycles per Dhrystone = 4249 Dhrystones/s

Because the clock cycle measurement is independent of microprocessor speed, this method makes it possible for engineers to rate microprocessors that aren't yet available, as shown in the previous chart.

Internal cache-hit rates can be determined with the read cycle counts by using the following formula:

$$1 - \left(\frac{\text{Read cycles with cache on}}{\text{Read cycles with cache off}} \right)$$

Large cache-hit percentages for the relatively small 68030 internal cache might indicate that this benchmark produced optimistic results for this particular processor design. Moreover, the cache-hit rates would probably be considerably less in an actual system *(Table 4)*.

In the graph of the 68020 and the 68030's performance operating within the test system, the horizontal axis represents the memory speed given as the number of wait states *(Fig. 2, again)*. The wait states are asynchronous for the 68020 and synchronous for the 68030. The vertical axis represents performance, given in Dhrystones/s as calculated with the aforementioned formulas.

Graphing data in this manner enables engineers to quickly determine the architecture options available for a given performance specification, and to ascertain the effects of design changes on performance. For example, the graphs show that there are four practical options for a 68030-based system to perform at 8k Dhrystones/s. Four curves—25 MHz, 33 MHz, 40 MHz, and 50 MHz—cross the 8k Dhrystone mark. Knowing these options, engineers can determine the best solution based on the relative cost and availability of the memory and processor components, as well as the difficulty of implementation.

In the Allen-Bradley example, the 68030 was compared to a 68020. These test results show an unexpected similarity in performance for the two microprocessors. For the asynchronous memory interface under consideration, the 68030 executed the test code only about 10% faster than the 68020. This difference can probably be attributed to the data cache in the 68030. Note that the 68030's asynchronous wait states are one wait state longer than the synchronous wait states.

For this application, the engineers found that a faster version of the 68020 offered the best price/performance ratio. If a memory management unit (MMU) or a synchronous bus was used in the test system, however, the difference in performance between a 68030 and a 68020 would be more pronounced. These results underscore the importance of modeling a test system that's as close as possible to the actual hardware, with test code that's as close as possible to the actual system code.

In particular, engineers should be careful when using benchmarks to compare different microprocessors. If different compilers are used to compare two different microprocessor families, the benchmark results might reveal more information about the compiler's efficiency than about the performance of the microprocessors being rated. Benchmarks typically test one aspect of performance, such as processor-to-memory interface, interrupt latency, or disk I/O transfers. The best way to compare different microprocessor families is to simulate with the compiler and code chosen to run in the final system. If this isn't possible, engineers should try to pick several benchmarks that most closely approximate how the final system will be used.

By simulating a test circuit model, designers can evaluate new processors over a wide range of design parameters with a minimum of effort. A test circuit model using full-function hardware models can reduce modeling time and run the test code accurately during simulation. This test circuit can be configured dynamically to deliver a wide range of architectures and measure system performance. To make the simulation most efficient, engineers can take advantage of the simulator's accuracy to reduce run time.

By evaluating a range of designs early in the design process, designers choose wisely and accurately predict the result of the final product. With the large number of new and increasingly complex microprocessors introduced each year, evaluating system architecture efficiently during simulation will help system designers realize the full benefit of these advances.□

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A free evaluation package demonstrates Accel's Tango PLD software for designing programmable logic devices. Tango PLD combines in one program a design compiler, logic minimizer and simulation. The program's list price is $495. The evaluation package consists of a 60-page illustrated tutorial and an evaluation version of Tango-PLD. To order the package, designers may call (800) 433-7801.

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Selecting the Correct Development Tools serves as a checklist for engineers choosing development and debugging tools. *What to Look for in an In-Circuit Emulator* covers how the emulator will work with the target and looks at basic emulator features, software considerations, and support issues.

Statistical Performance Analysis gives real-life examples of how statistical performance analysis helps improve code performance. The article also has C source code for a PC program, which stands alone or works with an Applied Microsystems' ES 1800 emulator. *Comparison of Source-Level Debug Tools for Intel 16-bit Microprocessors* describes features of the Validate/Soft-Scope, Validate/Unison, and GeneProbe debuggers.

Emulation in a Multiprocessor Environment: An 8051-68302 LAN explains a simple 68302-8051 local-area network and discusses using emulation and other tools to debug the design. Copies of the notes are available by calling (800) 343-3659.

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
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Imagination is more important than information.
Albert Einstein

Several trends stand out as the '90s open—the move toward a global peacetime economy, the opening of the European Common Market, the emergence of an Eastern European market, and changing environmental patterns. These will alter the product and service mix of many businesses while stimulating new opportunity. Defense companies in the U. S. are struggling with some of the most dramatic market changes since the late '40s. Participation in Europe's economic unification will affect many companies' bottom lines. Countertrade (barter) seems to offer a way to do business with cash-poor Eastern Bloc countries. Add to these items the difficulties of meeting tougher environmental and safety requirements.

Information on these issues, along with data on other significant items of national, local, and corporate interest, profoundly affects developing new products. Believable, accessible, voluminous, and conflicting information is producing a decision crisis. Only creative management and imaginative use of time-perishable information keeps the definition phase of the new-product development process from extending to infinity.

Developing a quality business definition and product definitions that align with the business definition isn't a single-step process done by an individual in a vacuum. It is a complex horizontal and vertical team effort that can touch just about everyone involved in the new-product development process. Top management, middle management, and individuals with the talent and the time for doing front-end work from R&D, marketing, manufacturing, and support become actively involved in coming up with business and product definitions. The accuracy of these definitions and the performance of new-product development teams to convert the ideas they contain into product reality forms the foundation for business success. To make the definition process more visible and therefore measurable, I've developed a Definition Matrix model. The two-by-six matrix establishes a recommended path to generate a stable product definition. The two columns are labeled business and product. The six rows are titled vision, big picture, market information, alternative synthesis, alternative analysis, and output. Each of the 12 cells identifies the production of refined information that leads to quality business and product definitions based on facts and verified assumptions. The results that managers and product development people produce within each cell are measurable. For example, you can tell if your business vision (row 1, column 1) is of high quality if:

- Everyone, from line worker to executive, understands the vision statement.
- It is short, bold, and optimistic.
- It was made by the right person, a leader in a position of power.
- It stimulates creative thinking.
- It doesn't speak of products and services.
- It places constraints on market focus.
- It lies beyond next quarter's earnings or this month's production schedule. It looks well into the future.

Likewise, a product definition is complete (row 6, column 2) when:

- A prototype or simulation of the final product exists for manipulation, measurement, and inspection.
- The complexity of work to be done within each functional area is quantized.
- The expected productivity for each functional group is understood.
- Estimates of resource availability are known.
- Information on complexity, productivity, and resource availability is used to estimate project time to market.

Space doesn't permit me to describe fully each cell of the Definition Matrix. But I've given you the basic structure. Next I'll describe an organizational model to further develop product-definition skills.

TIPS ON WRITING . . .

In their memos, letters, and periodic progress reports, engineers typically write about how they solved a technical problem. But since the writer of the report solved the problem, he may have difficulty seeing the forest for the trees. This form of tunnel vision is perhaps the biggest pitfall in engineers' writing—getting bogged down in details and not putting the problem and its solution in perspective. Perhaps the writer assumes that "everyone knows all that already."

Another common problem is digression. A writer trails off into side discussions that may be interesting technologically but aren't directly related to the subject at hand.

Remember—even if you know your subject cold, it is what's on the paper that counts—that's all that anyone else has at hand to learn about your project. Accept that your report may not say what you think you've said.

One helpful technique is to ask a colleague to read your first draft and give you feedback. If you do this, you'll have to swallow your writer's pride. But note that professional writers submit their writing to an editor's scrutiny every day. Everyone can use a second pair of eyes on his writing.

If you write on a PC, use one of the many spelling- and grammar-checking programs, besides the desktop standbys, a dictionary and a thesaurus. If you'd like to explore writing and grammatical topics in some depth, take a look at William Zinsser's *On Writing Well*, just out in a third edition.

DID YOU KNOW?

. . . that one-third of engineers and scientists doing research and development work are employed by the U. S. Department of Defense or by companies with DOD defense contracts?
IEEE

. . . that hard disk drives came to be known as Winchesters after the familiar .30-.30 rifle: The first drive held 30 Mbytes on each of its two spindles.
IBM *Directions*, Summer 1990

. . . that only 6% of working engineers are women. And just 16.5% of undergraduates currently majoring in engineering are women—a percentage that hasn't budged much in the past five years. Other fields are a different story, however. Women make up 40% of the enrollment in law schools and 35% of the enrollment in medical schools.
The New York Times

1-MINUTE OPINIONS

Should the U.S. government directly support U.S. electronic manufacturers, who face increasing international competition?

No. The problem is much more fundamental. The governmental system is already overloaded. **Herbert Heller**, *Pittsburgh, Pa.*

Yes. Everybody else does. Stop arguing about it, and *do* it. **James D. Traill**, *Tokyo, Japan*

The U. S. government should supply more tax benefits toward R&D investments as a means of combating foreign competition. **Ken Smetana**, *San Diego, Calif.*

The government seems to support other industries that can't support themselves (i. e., farming, railroads, welfare career specialists, etc.). What difference would one more make? **Mark A. Long**, *Bluffton, Ohio*

No! Absolutely not! The last thing we need in this country is the government subsidizing another important industry, especially the one I'm in.

All such subsidies do is isolate the beneficiaries from the market, ensuring that they will have no rock-hard stimulus to efficiency and leadership. Eventually the moribund companies lose their subsidies, and then they die, leaving the country with no means of catching up with the (foreign) companies that have had the benefit of exposure to the real world and its harsh lessons. I'd much rather see a bunch of unsubsidized gazelles than a whole lot of subsidized dinosaurs, and I wouldn't work for the latter. **Kenneth H. Fleischer**, *Los Angeles, Calif.*

No. I am against all attempts at manipulating free enterprise and all attempts to corrupt the free market. If a company or country cannot produce goods that are a of sufficient quality at a reasonable price, then they should be allowed to go under. It is well and good to say "Why not? The Japanese have been doing it for years." But that only makes you as bad as them and doesn't even begin to address the problem.

It's also how things like wars get started. **Paul Harper**, *London, England*

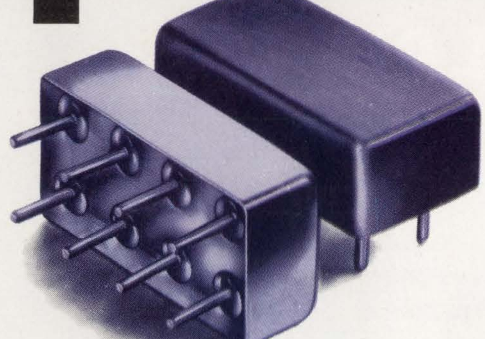
It is not a proper function of democratic governments in free-market economies to support underproductive industries. It is time for us to be done with corporate bailouts!

Government handouts and the restrictions accompanying them squelch necessity-motivated industriousness and creativity. The demoralizing and debilitating effects of government welfare for individuals are well known to political conservatives and liberals alike. The system, altruistic as it is, has produced multiplying generations of indolents and unemployables. Welfare recipients are soon entrapped by a bureaucratic, dehumanizing system. We can not afford to create a welfare system for corporations that will be equally counterproductive.

The parallel between individual welfare and government support of industry may seem obscure but it will become painfully clear to corporate recipients after the trap has been sprung. Whatever the government supports, it controls. Whatever the government controls, it corrupts. Government support and control aren't needed, but enlightened management is. Foreign competitors are beating us at our own game not because they are unfair but because we have tried to short-circuit the rules. The rules, originally made in America, are flexibility, individual initiative, productivity, and business decisions that promote long-term development vs. short-term greed. **Earl Pomeroy**, *Grand Rapids, Mich.*

What's your opinion on the design skills of today's EE graduates? How do their skills stack up against those of young engineers of the past? Or how important do you think analog design skills are for engineers? Send us your opinions on these questions to our Reader Opinions fax: (201) 393-0637. Or mail your responses to *Electronic Design*, Reader Opinions, 611 Route 46 W., Hasbrouck Heights, NJ 07604.

rugged plug-in amplifiers



0.5 to 1000MHz from $13.95 (10 to 24 qty)

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Internally the MAN amplifiers consist of two stages, including coupling capacitors. A designer's delight, with all components self-contained. Just connect to a dc supply voltage and you are ready to go.

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another Mini-Circuits' price/performance breakthrough.

MODEL	FREQ. RANGE (MHz) f_L to f_U	GAIN dB min	flatness††	MAX. OUT/PWR† dBm	NF dB (typ)	DC PWR 12V, mA	PRICE $ ea. (10-24)
MAN-1	0.5-500	28	1.0	8	4.5	60	13.95
MAN-2	0.5-1000	19	1.5	7	6.0	85	15.95
MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95
◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95
*MAN-1AD	5.500	16	0.5	6	7.2	85	24.95

††Midband $10f_L$ to $f_{U/2}$, ±0.5dB †IdB Gain Compression ◇Case Height 0.3 In.
Max input power (no damage) +15dBm; VSWR in/out 1.8:1 max.

*Active Directivity (difference between reverse and forward gain) 30 dB typ.

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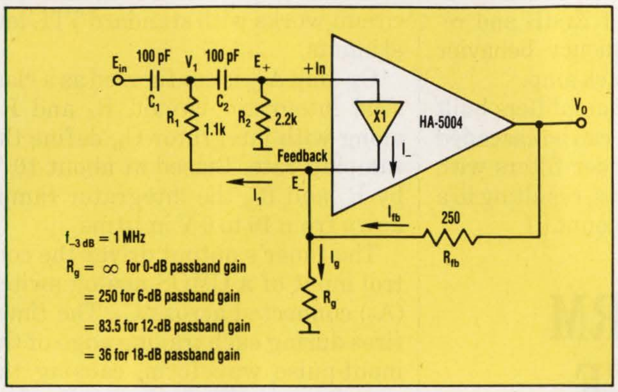
CIRCLE 169

C118 REV. E

CIRCLE 521

Vary Filter's Passband Gain

ALEKSANDER NIEMAND
Harris Semiconductor, P.O. Box 976,
Sollentuna, Sweden 19129; 46 8 623 5229.



1. BY USING the input buffer as the active element in the filter, the variable passband gain is set by the resistive feedback around the amplifier.

Standard op amps are widely used as building blocks in various active-filter configurations. One of the more popular is the Sallen-Key second-order high- or low-pass filter due to its straightforward design. However, while the filter simplifies second- or higher-order filter implementation, its passband gains can't be varied independently of other filter parameters. This limitation can be removed easily by using the new breed of current-feedback amplifiers as active elements in the filter design.

The main difference between a standard op amp and this type of amplifier lies in the input-stage topology. In the current-feedback amp, there's a high-impedance buffer between the noninverting and feedback inputs. Also, output voltage is a function of current in the buffer's output.

This current-feedback amp can be implemented in an active filter with a passband gain that's independently variable of other filter parameters. The filter itself is built using the input buffer as the active element while passband gain is set by resistive feedback around the amp *(Fig. 1)*.

The following equations can be derived from the circuit:

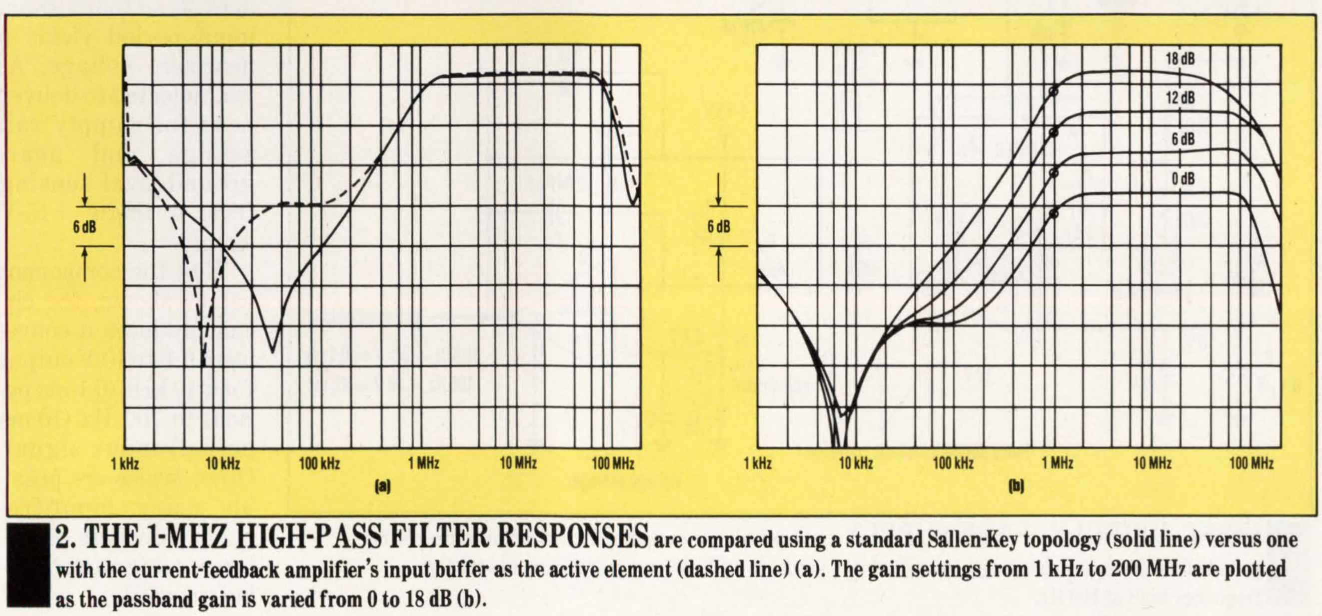
Output voltage: $V_O = A(s) \times I_-$
Input buffer: $E_- = E_+$
Current summing: $I_- + I_{fb} = I_g + I_1$
Kirchhoff: $I_{fb} = (V_O - E_-)/R_{fb}$
$I_g = E_-/R_g$
$I_1 = (E_- - V_1)/R_1$
$(E_{in} - V_1) \times sC_1 + I_1 = E_+/R_2$
$E_+ = V_1 \times sR_2C_2/(1 + sR_2C_2)$

Rearranging the equations and performing basic algebraic operations results in the following transfer function for the circuit:

$$V_O(s)/E_{in} = ([s^2R_1R_2C_1C_2]/[1+sR_1\{C_1 + C_2\} + s^2R_1R_2C_1C_2]) \times (1 + [R_{fb}/R_g] - [R_{fb}/sR_1R_2C_2]).$$

The first term is readily recognized as the second-order high-pass filter transfer function. The gain expression at the end of the equation contains a frequency-dependent term $[R_{fb}/(sR_1R_2C_2)]$ that produces a notch in the filter's stopband. With the proper dimensioning of components, this notch can occur at a sufficient low frequency so that its effect on the passband and the roll-off characteristics will be negligible. A prototype circuit was built using selected filter-component values to produce high-pass Butterworth characteristics that have a –3-dB frequency at 1 MHz.

A comparison was made between



2. THE 1-MHZ HIGH-PASS FILTER RESPONSES are compared using a standard Sallen-Key topology (solid line) versus one with the current-feedback amplifier's input buffer as the active element (dashed line) (a). The gain settings from 1 kHz to 200 MHz are plotted as the passband gain is varied from 0 to 18 dB (b).

filter response with standard topology and the proposed design. As evidenced by the frequency-response plots, a notch appears in the stopband for both topologies *(Fig. 2a)*. In a standard configuration, the notch results from leakages and input stray capacitances. If the capacitances were taken into account in the analysis, similar parasitic terms in the transfer function would have been produced.

Passband gain in the new design was then varied between 0 and 18 dB by adjusting the value of R_g between infinity and 36 Ω. Afterwards, frequency response was plotted for each gain setting between 1 kHz and 200 MHz. The plot shows that the cutoff frequency remains constant throughout the gain range, while roll-off is maintained at –20 dB/decade down to 100 kHz *(Fig. 2b)*. The upper bandwidth limit remains constant up to a gain of 12 dB and reflects the high-frequency behavior of the current feedback amp.

A number of filter amplifiers built with this technology can be cascaded to produce higher-order filters with higher passband gains, resulting in a reduced component count.□

CIRCLE 522

Convert Waveform Period To Voltage

DAVID JOHNSON
10198 W. Berry Dr., Littleton, CO 80127; (303) 973-8408.

On special occasions, a design may call for the monitoring of a signal's period rather than its frequency. This period-to-voltage circuit performs such a function. The circuit's 0.1- to 10-V output corresponds to an input period of 10 to 0.1 ms. The design is made of simple components, and requires just a single +15-V supply *(see the figure)*.

A CMOS 555 timer IC (A_1) is configured as a 5-μs one shot. Resistors R_1 and R_2 bias the timer's input at about 3 V above the triggering threshold. Because the timer fires only on the trailing edge of the input waveform, the signal doesn't need a symmetrical 50% duty cycle. However, it does require a fast fall time. The circuit works with standard TTL-level inputs.

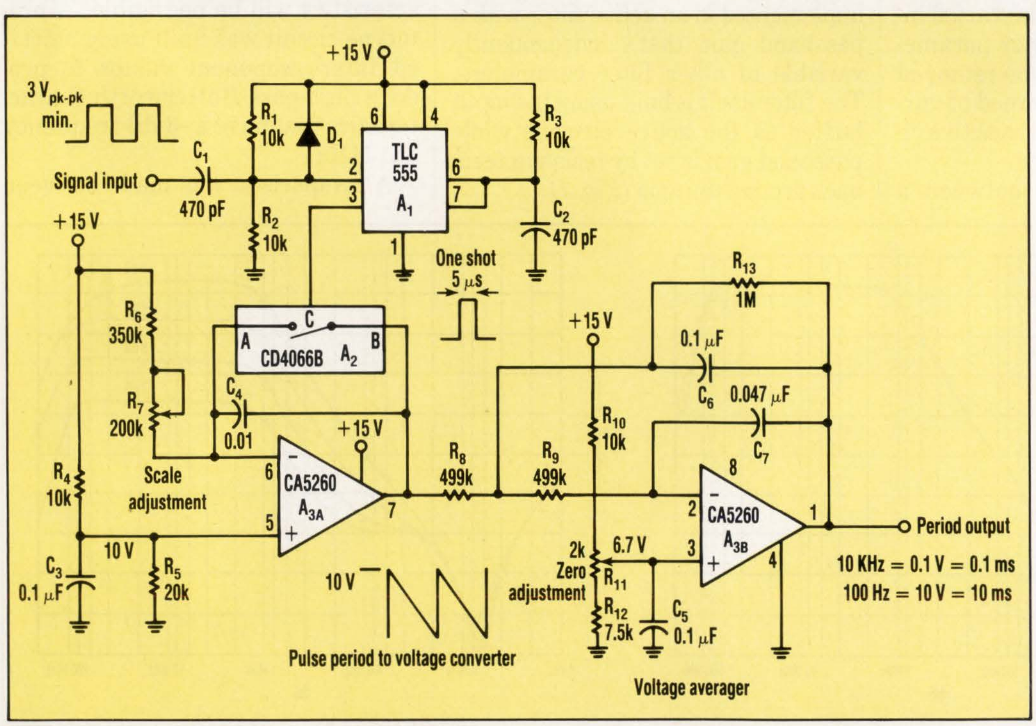
Op amp A_{3A} is configured as a classical integrator circuit. R_6 and R_7, along with integrator C_4, define the ramping rate. Biased at about 10 V by R_4 and R_5, the integrator ramps down from 10 to 0 V in 10 ms.

The timer's output drives the control input of a CMOS analog switch (A_2) connected across C_4. The timer fires during each trailing edge of the input-pulse waveform, causing the switch to reset the integrator back to 10 V.

The average of the sawtooth waveform voltage produced at the integrator's output is directly proportional to the time between the incoming pulses. R_7 adjusts the conversion scale and compensates for component tolerances.

The sawtooth waveform is averaged using an inverting low-pass filter (A_{3B}). The filter components are selected for a gain of 2 and a 5-Hz knee. R_{11} sets the zero reference voltage (6.67 V) so that a short input period yields a near-zero voltage. A_3 was selected to deliver near-full-supply rail swings and near-ground-level sensing from a single +15-V supply.

With the component values shown, the circuit produces a convenient 0.1- to 10-V output for a 10 kHz (0.1-ms period) to 100 Hz (10-ms period) input signal. Other scales are possible using input-frequency dividers or different integrator ramping times.□



USING A SINGLE +15-V SUPPLY and a few simple components, this circuit converts the period of a waveform to a voltage. Integrator A_{3A} produces a 10-ms ramp that determines the low-frequency limit of 100 Hz.

CIRCLE 523

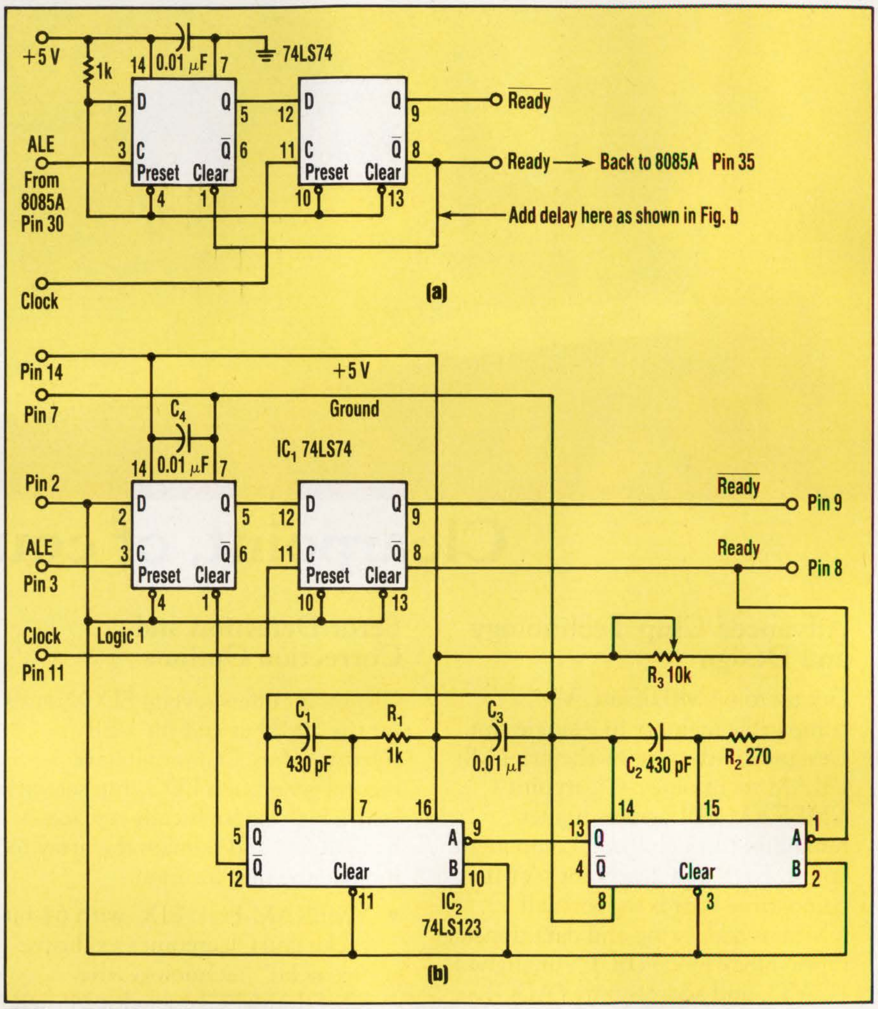
ADD VARIABLE WAIT STATES

JOHN DUNN
Bertan Associates Inc., 121 New South Rd., Hicksville, NY 11801; (516) 433-3110.

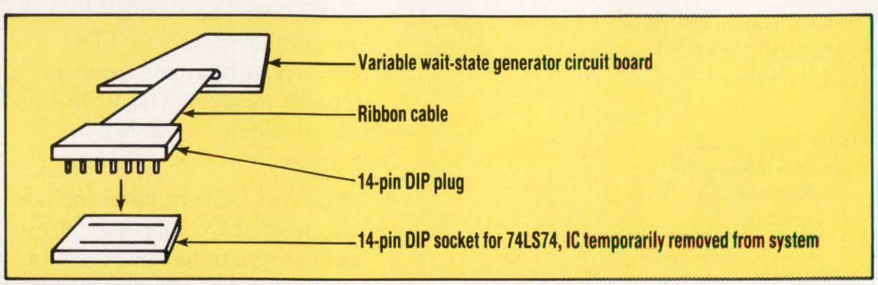
Any microprocessor system may require a fixed number of wait states. For the 8085A, the prescribed method of generating them uses a 74LS74 dual D flip-flop *(Fig. 1a)*. During system development, however, temporarily having more than one wait state per machine cycle could be useful. In such cases, a variable number of wait states can be generated by using the 74LS74 with a 74LS123 retriggerable monostable vibrator *(Fig. 1b)*.

The additional wait states are added by introducing a delay in the feedback path to the Clear input of the D flip-flop (74LS74). By making that delay adjustable with R_3, a variable number of wait states per machine cycle can be generated. Any portion of the target system that can't work quickly enough at normal speed may become operational when the system is slowed down by the additional wait states.

If the circuit's pinouts are followed for the basic wait-state generator, and if the flip-flop is put in a 14-pin socket, the circuit can be constructed with a ribbon cable ending in a 14-pin plug *(Fig. 2)*. To get the variable wait states, simply unplug the flip-flop and plug in the circuit board.□



1. THIS CIRCUIT ILLUSTRATES the prescribed method for generating wait states for an 8085A microprocessor (a). During system development, a circuit that generates a variable number of wait states per machine cycle is often useful (b).



2. THE VARIABLE WAIT-STATE GENERATOR is plugged into the socket normally occupied by the 74LS74 used to generate wait states. A ribbon cable and 14-pin DIP plug simplify the job.

IFD WINNERS

IFD Winners for May 10, 1990

Gary Multer, Sen Majumber, and Raj Pisupati, Digital Equipment Corp., 20 hampden St., Boston, MA 02119; (617) 569-0284. Their idea: *"Drive Stepper Motor, Cut Cost."*

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Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.

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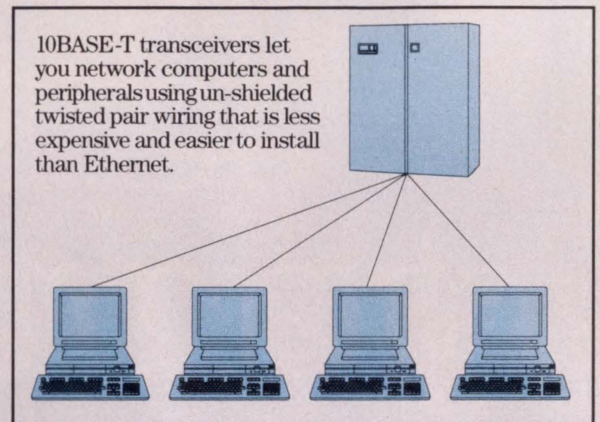
With our new ML4650 family of Single Chip 10BASE-T transceivers, you're covered all across the LAN. Because we have single chip twisted pair solutions for both ends, hub to node. Available now. In quantity. Giving you a fast, no hassle 10BASE-T solution.

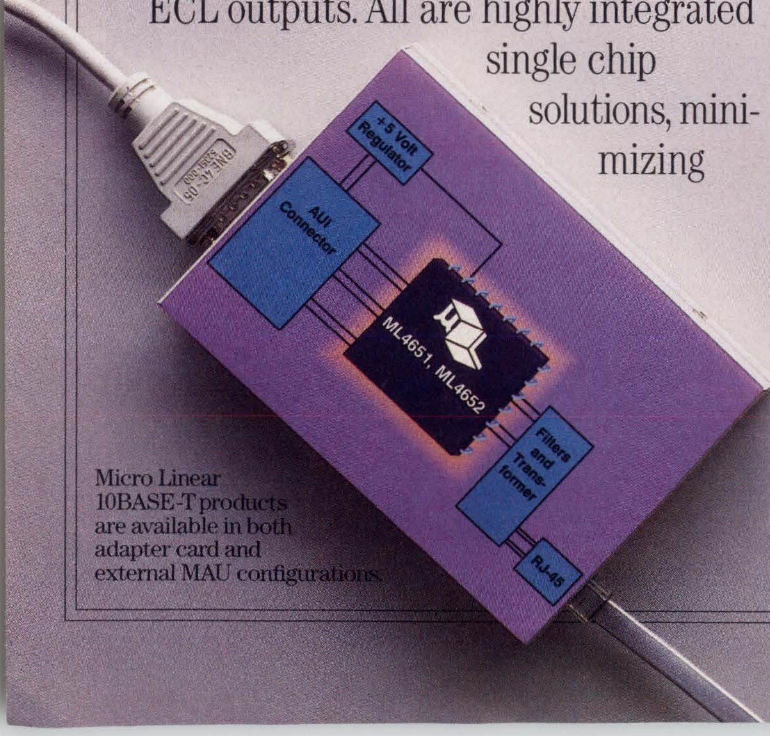
On the PC side, the ML4651 and ML4652 transceivers incorporate AUI interfaces designed for both Ethernet adapter cards and external MAUs. On the hub side, the ML4654 is tailor-made for a hub design with TTL or ECL outputs. All are highly integrated single chip solutions, minimizing the number of external components required. So your design-in process is much easier. And faster.



10BASE-T transceivers let you network computers and peripherals using un-shielded twisted pair wiring that is less expensive and easier to install than Ethernet.

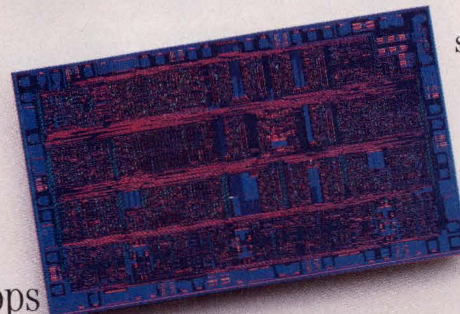
On-chip current driven transmitters are less sensitive to noise and power supply variations. So you get superior jitter performance and low noise outputs that help you easily pass FCC requirements. And the receiver includes an intelligent squelch that rejects cross-talk noise commonly found coupling from the phone wires into the LAN. There's no external crystal oscillator required either, and devices use 5 volts only power supplies.

Parts are available in 20- and



Micro Linear 10BASE-T products are available in both adapter card and external MAU configurations.

ist in 10BASE-T.


Semi-standard options of the standard 10BASE-T circuits are possible simply by modifying the metal mask on the FB3651 tile array.

24-pin skinny DIPs and 28-pin PLCCs. There's even an ML4621 Fiber Optic Inter-Repeater Link (FOIRL) receiver available to satisfy 10 Mbps fiber optic Ethernet requirements.

And, unlike much of the technology you've been hearing about, these are products of experience. We've been shipping twisted pair transceivers since 1987, as part of Synoptics' LattisNet network.

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We're one of the first to market for one simple reason. Our 10BASE-T family is based on our standard FB3651 bipolar tile array. So we were able to quickly modify our "standard" product to satisfy the rapidly-emerging IEEE 802 standards.

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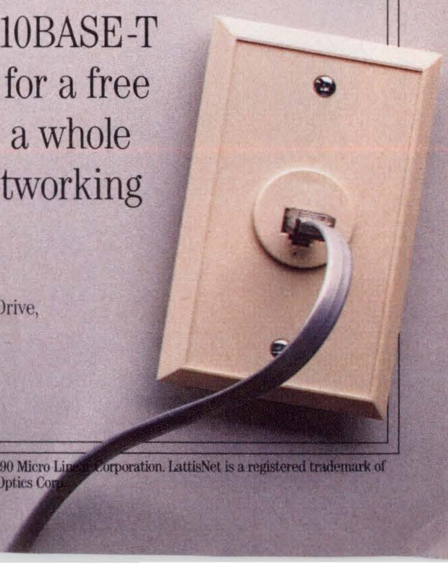
If you'd like to turn your 10BASE-T idea into a deliverable product, just call Charles Yager today at (408) 433-5200 and ask him for the complete story on our ML4650 family of single chip 10BASE-T transceivers. Or ask for a free sample. It could add a whole new twist to your networking scheme.



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CIRCLE 125

A SPECIAL EDITORIAL FEATURE

PIPS

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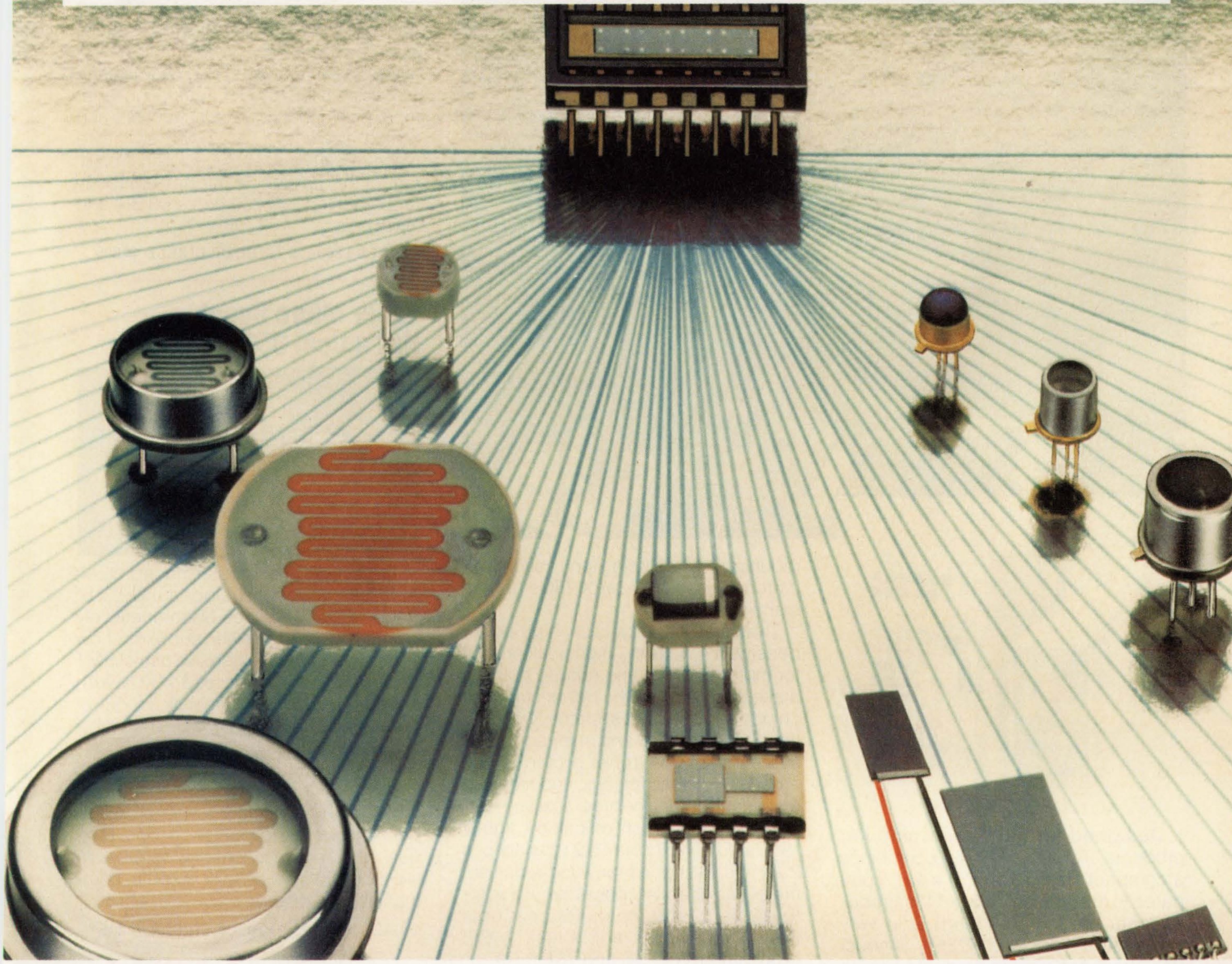

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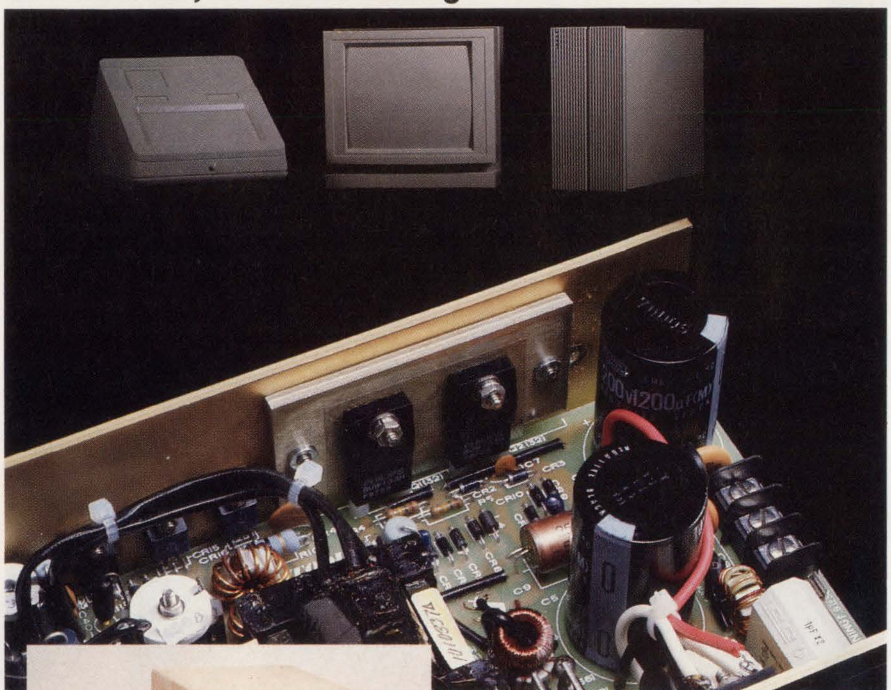

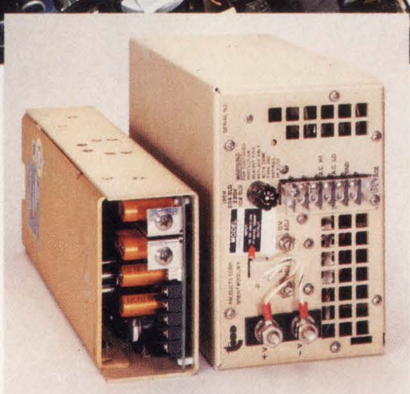

Designed for high-end computer products, TODD's MAX-750 combines a compact size, 13.5" x 5" x 2.6" compared to the typical 5" x 8" x 11" shoebox switcher (see photo insert), and very competitive pricing. OEM product designers can reduce product size with a MAX-750 or build in power supply redundancy, replacing one "shoebox" switcher with two MAX-750's in the same space.

The small package size, high power density of 4 watts/in., high peak current for motor starting, and cooling options, make the MAX-750 the power supply of choice for VMEbus systems, workstations, file servers and mini-computer systems. The switcher provides 120 amps of +5 volts for logic and memory, and features up to three auxiliary outputs providing high efficiency, tightly regulated 12 volts or −5.2 volts at up to 20 amps. Designed for world wide use, the series offers AC power fail, AC autoline select, and meets International Safety standards and Class A RFI requirements of FCC and VDE 0871.

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TODD's DC to DC converters provide up to 350 watts from 48 volts DC input. Designed as companion units to TODD's standard line of AC input power supplies, they are fit, form, and function compatible with the MAX-350, MTC-250, MTC-350, and certain single output SC series products.

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The series features up to 50 amps of +5 volts for logic and memory and fully regulated high efficiency mag-amp outputs to power up to four disc drives. Auxiliary outputs power common peripherals like ECL monitors, RS232 outputs, communications drivers, etc.

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More information on these and the full line of TODD Switching Power Supplies can be obtained in EEM File 4000, by circling the response card numbers, or by contacting:

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Use Power Bypassing and Busing for High-Performance Circuits

Taking A Sensible Approach To Decoupling Capacitors Can Mean Better Designs

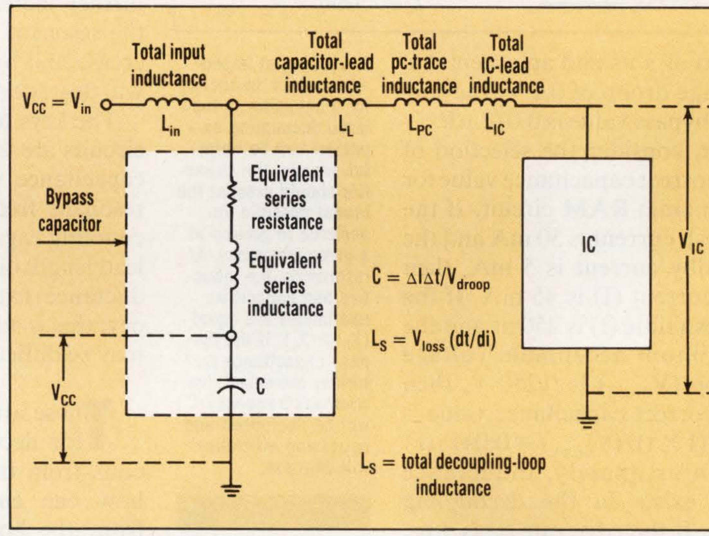
BY MICHAEL SCOTT HYSLOP

Rogers Corporation, Circuit Components Division, 2400 S. Roosevelt St., Tempe, AZ 85282; (602) 967-0624.

Advances in IC design and packaging are making bypassing more difficult than ever. Circuits containing high-performance ICs operate unpredictably unless the power-supply network is properly bypassed and distributed. Even a design that's thoroughly simulated and whose components are individually tested may fail to operate when the first board-level prototype is built. Signal rise times in the picosecond range can easily produce ground bounce and V_{CC} voltage-drop problems, particularly with large numbers of gates switching simultaneously. High-density packages, such as chip carriers with hundreds of closely spaced pins, worsen the problem.

These IC-driven advances create other problems, including noise generation within the pc-board environment, increased electromagnetic-interference (emi) and radio-frequency-interference (rfi) emission, and increased susceptibility to emi and rfi. As IC designs migrate from 5-V to low-voltage (3-V) operation, noise margins shrink, which makes bypassing even more critical. For most electronic systems, the primary sources of radiated emissions are the pc boards contained within that system. With their long trace runs carrying transient currents with sizable high-frequency spectral content, pc boards radiate emi efficiently.

A power-distribution system would not radiate at all if only dc currents flowed. But ICs draw large amounts of instantaneous current during logic switching.



1. In a typical IC-decoupling-circuit model, the decoupling capacitor (C) is a local energy source that supplies current to the chip during gate switching. The essence of good bypassing is to minimize the total decoupling-loop inductance by keeping the equivalent series inductance and resistance to a minimum.

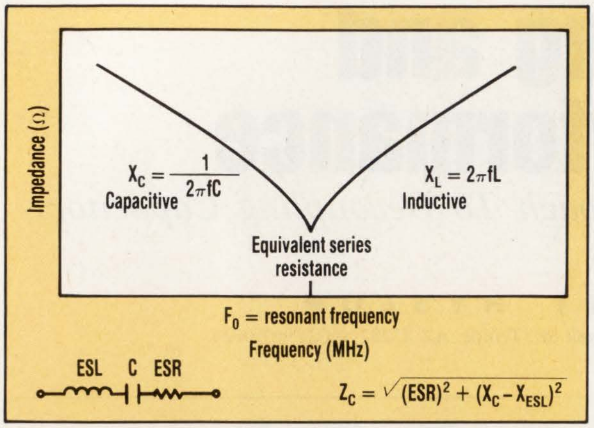
These current pulses rise and fall quickly, and therefore have significant spectral content between 30 MHz and 1 GHz. The faster the IC, the larger the portion of the spectrum falling within that band. But because system speed is critical, reducing emi by increasing rise and fall times isn't an answer.

This article suggests a number of power-bypassing and bussing options, some of which are novel and others that are often overlooked by system designers. Techniques to select the best bypassing and bussing options will also be presented.

Designers often attempt to decouple every IC in a system by liberally sprinkling bypass capacitors throughout the system. In doing so, little attention is paid to the correct capacitance values and their associated inductance. The capacitance values are chosen using empirical rules of thumb. It's better to optimize the capacitance value for the particular circuit with simple analytic techniques.

In any IC-decoupling circuit, the capacitor is essentially a local energy source that supplies current to the chip during gate switching. Without bypassing, the impedance of the pc traces causes a droop on the supply line. A typical IC-decoupling circuit can be easily modeled *(Fig. 1)*. Depending on the frequency, the typical unbypassed dynamic impedance of the V_{CC} line is about 50 to 100 Ω. That's high enough to produce a considerable V_{CC} droop unless a bypass capacitor is used.

Consider, for instance, the case of an octal buffer. Assume that each buffer output sees a 50-Ω dynamic load and that the output-voltage swing is 2.5 V. The current swing for the buffer is therefore 50 mA. If all eight buffers operate simultaneously, the maximum current swing is 400 mA. Assuming a switching



2. Looking at impedance versus frequency for a capacitor, a too-large decoupling capacitor can be harmful. Ideally, the capacitor should present the lowest possible impedance to ground at a given frequency. At resonance, the inductive and capacitive reactances are equal ($X_C = X_L$). If the bypass capacitance is further increased, the resonant frequency will be decreased and bypassing efficiency will degrade.

speed of 3 ns and an acceptable voltage droop of 0.1 V, the correct bypass value is 0.012 μF.

Or, consider the selection of the correct capacitance value for a dynamic-RAM circuit. If the refresh current is 50 mA and the standby current is 5 mA, then the current (I) is 45 mA. If the refresh time (t) is 250 ns and the maximum acceptable voltage droop (V_{droop}) is 0.250 V, then the correct capacitance value is $C = (I \times t)/(V_{droop}) = 0.045\ \mu F$.

Unfortunately, inductance also exists in the decoupling loop. If the edge rate (t) is 3 ns, the current change (I) is 45 mA, and the acceptable voltage loss (V_{loss}) is 0.250 V, then the maximum permissible decoupling-loop inductance is $LS = V_{loss} \times (t/I) = 17$ nH.

These capacitance values are the minimum that will keep voltage droop and loss within acceptable bounds. So why not choose a larger capacitance value "just to be safe?" The answer is related to the resonant frequency of the decoupling capacitor. Ideally, the decoupling capacitor should present the lowest possible impedance to ground at the frequency of concern. The decoupling capacitor is modeled as an equivalent series inductance (ESL) in series with an ideal capacitance (C) and an equivalent series resistance (ESR), which comprises both the dielectric losses and ohmic lead resistance. At resonance, the inductive and capacitive reactances are equal ($X_C = X_L$). If the bypass capacitance is further increased as suggested, the resonant frequency will decrease and bypassing efficiency will degrade *(Fig. 2)*.

The keys to decoupling noisy circuits are to select the correct capacitance value, to note the resonant frequency of the decoupling capacitor, and to keep lead length (and thereby lead inductance) to a minimum. In theory, this is well understood, but may be difficult to achieve.

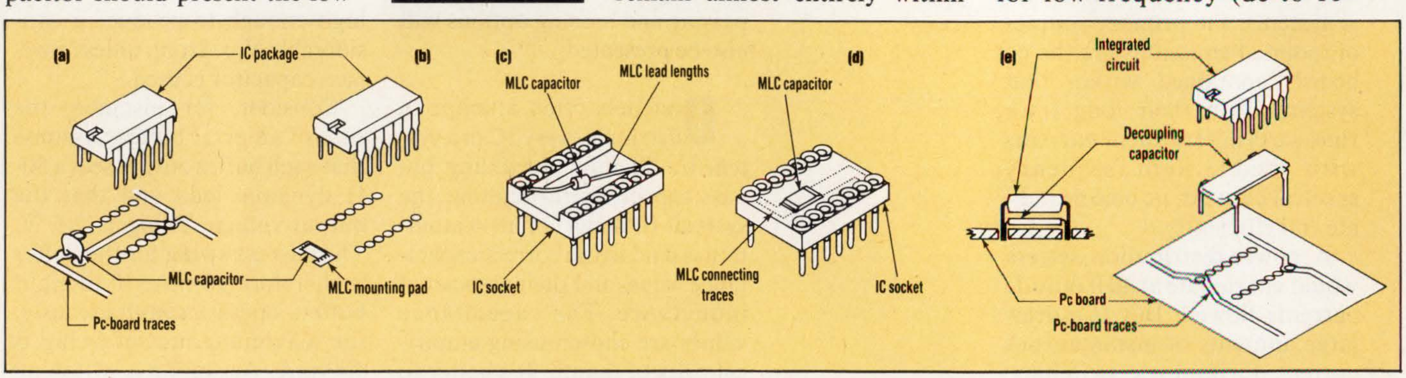
Those are some techniques for decoupling noisy circuits from the power bus. But how can emi that's radiated from the board traces be reduced? The best way is to contain the interfering high-frequency pulses in the smallest closed-loop area possible. That's because emi is a function of loop geometry and frequency. Such containment is accomplished by using a local decoupling capacitor for charge storage and short interconnects to the IC. As long as the impedance of the coupling loop is much lower than that of the rest of the power-distribution system, the high-frequency components of the circuit will remain almost entirely within this loop, minimizing emi. When the loop's impedance is no longer much lower than that of the rest of the system, some fraction of the high-frequency component will be carried on the larger loop formed by the power-distribution traces. This results in higher emission levels.

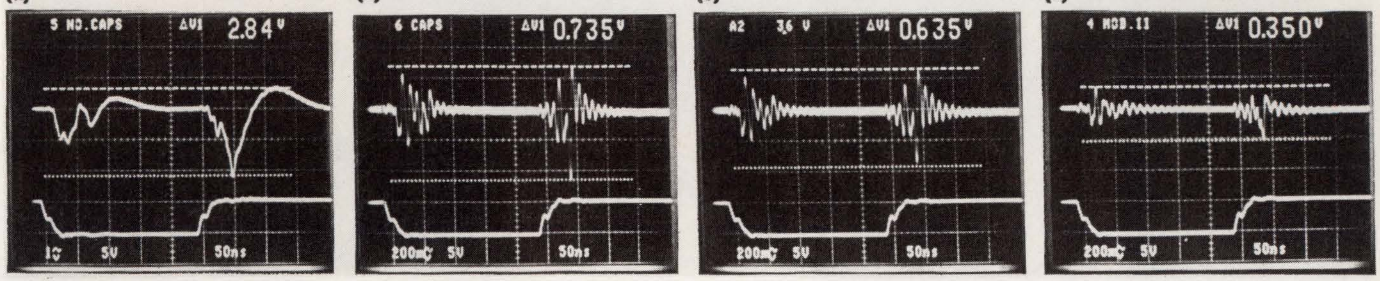
The key, then, is to minimize the impedance of the capacitor and the interconnects. Ideally, the capacitor should have no lead inductance, low loss and stable capacitance, and be as close to the IC as possible. Such a capacitor would have very low impedance and an excellent ability to deliver current in the desired band of rejection.

Unfortunately, real capacitors are often far from the ideal. Most decoupling capacitors are Z5U-grade barium-titanate-ceramic capacitors. Barium titanate is used because of its high dielectric constant, which allows small capacitors to have relatively large capacitance values. Depending upon the formulation and packaging, such ceramics perform extremely well—both in terms of losses and capacitance—at resonances that vary from less than 1 MHz to nearly 20 MHz. Above resonance, it becomes lossy and the capacitance begins to fall. This generally limits the effectiveness of a good Z5U capacitor to the 1-to-50-MHz frequency range.

Other dielectrics, such as strontium titanate, NPO, and some polymers, have better high-frequency performance but a lower dielectric constant. This can make them unsuitable for low-frequency (dc-to-10-

3. Shown are some DIP-decoupling options. Multilayer-chip (MLC) capacitors can be connected through pc-board traces (a) or through voltage and ground planes (b). Or, the IC sockets can be decoupled by placing MLC capacitors between the voltage and ground pins of the socket (c, d). Finally, decoupling can be accomplished by installing a parallel-plate capacitor under the IC package (e).





4. Various tests show the total noise resulting from various decoupling techniques for a memory array. The first scope photo shows the result with no decoupling in the memory array (a). The results of decoupling the array follow, with a 0.33-μF discrete multilayer-chip capacitor mounted at the end of every RAM (b), a 0.33-μF decoupled socket mounted under every RAM (c), and a 0.30-μF "under-the-DIP" flat decoupling capacitor (manufactured by Rogers Corp.) mounted under every RAM (d). The flat, under-chip capacitor held total noise the lowest.

MHz) decoupling. As a result, there is a trade-off of high-capacitance and low-frequency decoupling against low losses and stable capacitance for good high-frequency decoupling.

If the pc board works well with high levels of low-frequency noise that were only slightly attenuated by low-valued local decoupling capacitors, then low-valued capacitors may be used. Remember that low-valued bypasses reduce emissions more effectively than most high-valued decoupling capacitors. However, if this isn't the case, then a mix of the two types could be employed. It's best to have the resonant frequency of the decoupling loop at or near the troublesome frequency because the loop's impedance is lowest at that point.

The two types of capacitors should not be next to each other when being mixed. The high-dielectric-constant capacitor can dampen the resonance of the more frequency-stable, low-dielectric-constant capacitor. In cases where the emi problem is below 50 MHz, the best choice is a good, low-inductance Z5U (or equivalent) capacitor. This is because it combines excellent low-frequency decoupling with reductions in radiated emissions up to that frequency.

In theory, then, techniques to decouple noise from the power bus and minimize emi are known. But how is this achieved in practice? Bypass capacitors are often placed on the pc board as an afterthought. A typical capacitor placement has long asymmetrical capacitor leads and long pc-board traces *(Fig. 3a)*. But placement can be improved by using internal parallel power and ground planes, resulting in inherently lower bypass-loop inductance *(Fig. 3b)*. However, the relatively long pc-board traces to the IC's voltage and ground pins introduce inductive effects and limit the capacitor's effectiveness at high frequencies. Moreover, the capacitors take up board space, which often is tight.

Another possibility is to integrate the decoupling capacitor into the IC socket itself *(Figs. 3c and 3d)*. Although they're effective in some cases, such decoupling schemes add to the board's cost. In addition, this tactic can be ineffective at high frequencies because of inductive effects resulting from overly-long capacitor and socket pins and from the mounting configuration of the capacitor within the socket.

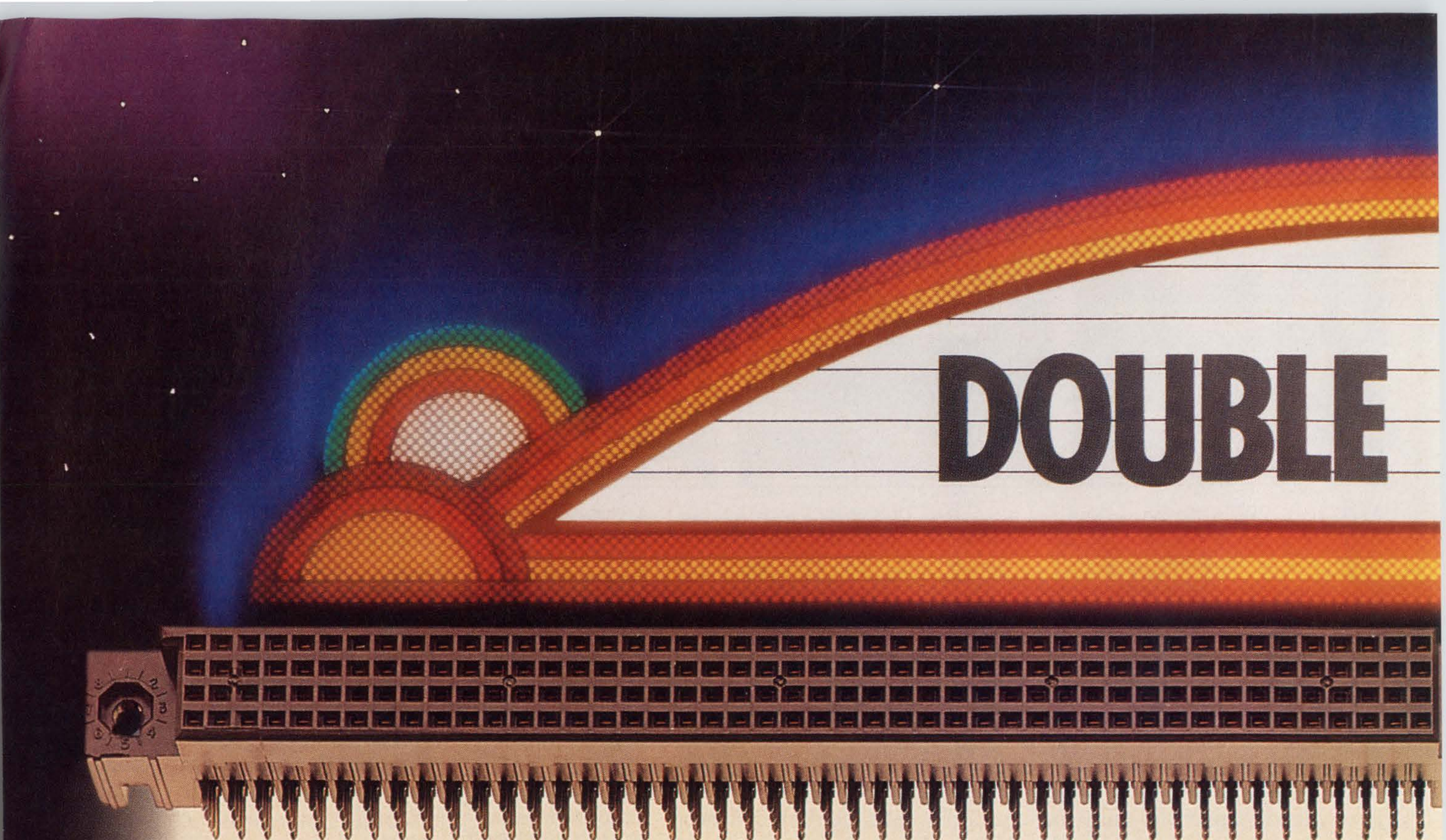
A more elegant and efficient solution involves a decoupling capacitor consisting of a single-layer ceramic dielectric sandwiched between two parallel-plate electrodes *(Fig. 3e)*. This decoupling capacitor offers two advantages over the others mentioned. First, it's positioned under the DIP, which increases board density. In addition, it has parallel-plate construction and shares pc-board holes with the IC, which yields the lowest possible inductance in the decoupling loop.

These "under-the-DIP" flat capacitors are available with values ranging from 450 to 3000 pF for decoupling in the 50-to-70-MHz range, and from 0.02 to 0.16 μF for the 1-to-30-MHz range. They use X7R, Z5V, and P3J dielectrics, and are available in standard 14-to-40-pin DIPs and in non-standard pinouts.

To verify the performance gains achieved by paying close attention to bypassing, characteristic impedance analysis was performed on alternative decoupling schemes. Under-the-DIP flat decoupling capacitors were analyzed for two dielectric materials (Z5V and X7R), and then compared to a conventional capacitor and to a decoupled socket of roughly equal capacitance. The test consisted of connecting each decoupling device to the test fixture in a manner that simulated actual use on a pc board. This included any circuit traces that might be used to connect the decoupling capacitor to the IC voltage and ground pins. The impedance analyzer's frequency was then swept from 1 to 500 MHz in logarithmic increments.

The net impedance of a decoupling capacitor and its associated leads is almost entirely inductive at frequencies above its resonant frequency. Typical values of inductance were calculated for each decoupling method at a frequency approximately one decade above resonance *(see the table)*. Note that the lowest value of inductance, 11.0 nH, is associated with the under-the-DIP capacitor. In addition, its resonant frequency is 50% higher (3 MHz compared with 2 MHz). This results from eliminating lead and pc-board traces.

To compare the three devices (an under-the-DIP flat capacitor, a socket with an integrated decoupling capacitor, and a ceramic monolithic capacitor) in an actual circuit, a memory ar-



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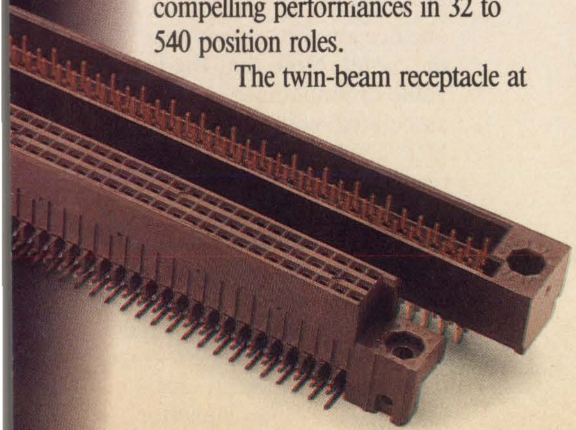
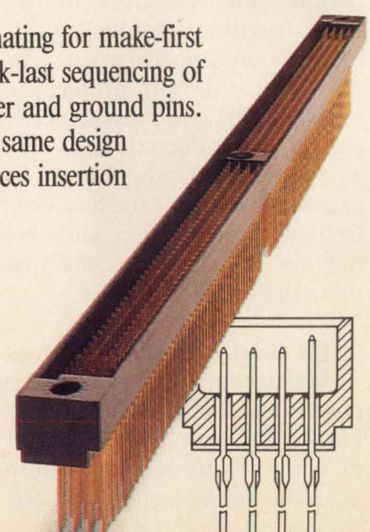




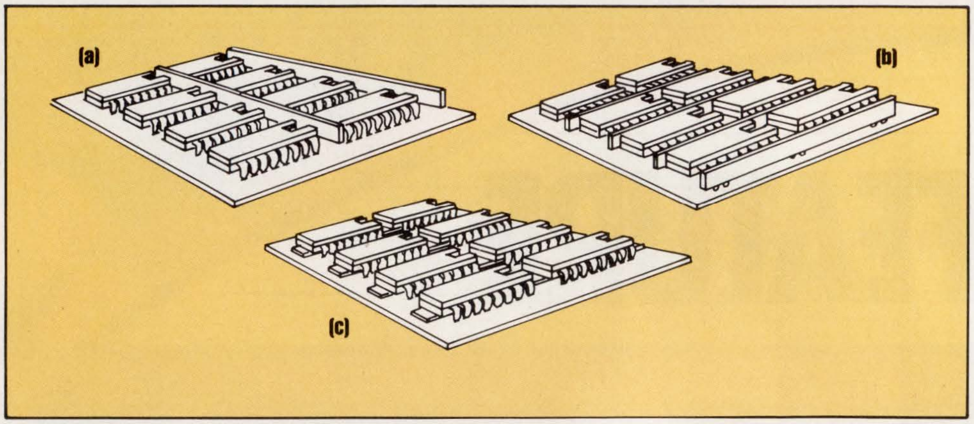
Two levels of sequenced mating allow "hot" connect/disconnect. Compliant pin option for solderless pcb insertion.

ray consisting of 32 Fujitsu MB81256-15 256-kbit dynamic RAMs (150-ns access time) was assembled on a Robinson Nugent VQC pc board. The DRAMs were connected to a counter, which provided row-address sequencing for refresh. Refresh waveforms following Fujitsu's recommendations were created by a waveform generator. All 32 DRAMs were refreshed simultaneously.

In the test, all like decoupling devices were attached on the board in their respective decoupling schemes. In addition, the ac-voltage noise was measured across V_{CC} and ground of the "noisiest" 256-kbit RAM for each set of decoupling devices. Measurements were also made without any decoupling capacitors in place. In all test cases, a 100-μF bulk decoupling capacitor was mounted at the test board's power-input pins.

The test results can be depicted graphically *(Fig. 4)*. In each display, the row-address-sequencing signal is shown as a reference (the bottom trace). The vertical and horizontal scales are found at the bottom of each figure. The decoupling method using the under-the-DIP flat capacitor resulted in the least amount of total noise, 350 mV, as compared to the total noise of 735 mV and 635 mV associated with the discrete multilayer-chip capacitors (MLCs) and decoupled sockets, respectively.

The memory-array example shows how bypassing minimizes the transmission of switching noise to a board's power bus. But how does bypassing affect the emi radiated by the board? A simple pc board was created to determine the effects of IC decoupling upon the radiated emissions of an electronic system. The board, which contained an Intel 8049 microcomputer IC, a clock circuit, and several driver transistors, executed a video-game program stored in ROM. Most radiated emissions from such a self-contained system can be attributed to the power-distribution system. A horizontally polarized antenna was positioned on-axis 90 cm above the board, operating in a shielded chamber.



5. Capacitive bus bars can be mounted vertically across IC rows (a), vertically between IC columns (b), or horizontally under IC columns (c).

Bypassing was improved incrementally. First, the board was run without any decoupling capacitors. Next, for bulk decoupling, a 22-μF tantalum capacitor was connected 13 cm from the 8049 chip. Reducing the decoupling loop by this small amount diminished emissions up to 10 dB. Bypassing was further improved by placing a 0.1-μF MLC Z5U capacitor as close to the 8049 IC as possible. This further reduced emissions below 50 MHz.

The next incremental bypassing gain was achieved by replacing the 0.1-μF capacitor with an under-the-DIP 0.03-μF flat capacitor. By eliminating the field associated with the traces and cutting lead inductance, emissions were further reduced by nearly 5 dB below 70 MHz and 2 dB above 70 MHz.

A key to building low-noise pc boards using high-speed logic, beyond optimizing local capacitive decoupling, is to minimize inductance. Two common methods are increasing the width of the supply traces and building additional planes into the board. The first method can't be used on pc boards with moderate-to-high package density. The second method—a multilayer pc board—is expensive compared with a two-sided board, though it does offer increased density. An alternative method combines multilayer performance with the cost advantages of two-sided pc boards, while providing excellent decoupling. That alternative is capacitive pc-board bus bars.

Such bus bars use wide, thick conductors with supply and return lines in close proximity. An example is Rogers Corp.'s Q/PAC bus bars. Their integral decoupling capacitors offer one of the lowest inductance power-distribution systems available.

To demonstrate the relative merits of combining decoupling with power distribution, hex inverters of the 74XX, 74LSXX, and 74SXX logic families were tested. The hex-inverter packages were connected with short jumpers to form a five-inverter ring oscillator. The ring oscillators were free-running and operated at the IC's maximum speed.

Five of the ring oscillators were soldered onto a board using one of three power-distribution and decoupling systems. One system was a two-layer board using 0.070-in.-wide supply traces with 0.1-μF capacitors at each IC for a total capacitance of 0.6 μF. A second was a multilayer board, including a ground plane, with a 0.030-in.-wide V_{CC} trace and a 0.1-μF capacitor at each IC. The third was a capacitive bus bar rated at 0.28 μF. All three were powered by a low-noise supply. The operating-noise level was measured at the end of the power-distribu-

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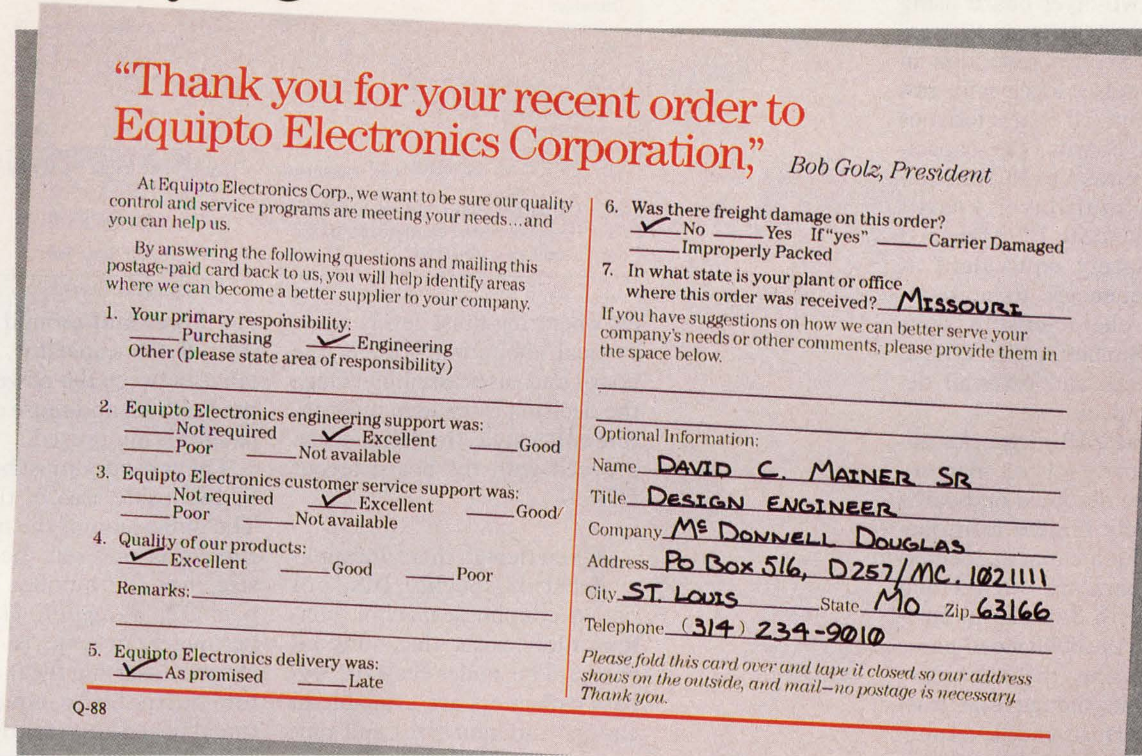

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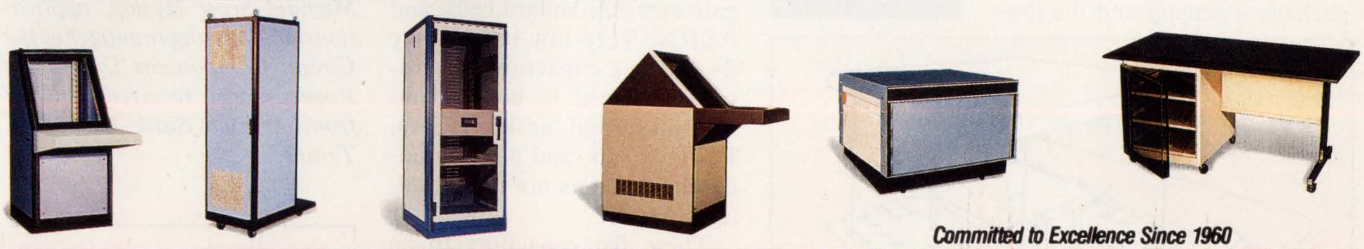

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tion system and displayed on a spectrum analyzer.

In all operating-noise-level tests, the capacitive bus bar was 25 to 35 dBm quieter than a standard two-layer board using equal or greater decoupling capacitance. Such a reduction in operating-noise level will improve the emi/rfi characteristics of most pc boards. The capacitive bus bar was 5 to 10 dBm quieter than multilayer boards from resonance to 150 MHz and approximately equivalent at higher frequencies. Its noise-attenuation characteristics were 10 to 20 dBm better than typical supply traces and external decoupling capacitors.

Now that ZIP memories enable extremely dense memory arrays to be designed on boards with severely limited form factors, very high capacitance-per-inch bus bars are offered that provide up to 3.0 μF/in. Incidentally, in the 8049 video-game example, using the capacitive pc-board bus bar gave at least the same performance level and, in most cases, an additional 1-to-3-dB emi-noise reduction. That's because it eliminated nearly all of the power and ground traces on the pc board.

Each circuit design has different requirements that can affect the way power-distribution and decoupling components are mounted. Factors such as board size, number and types of ICs, component-height requirements, and personal preferences play roles in determining which mounting style is best. Horizontal mounting allows maximum packaging density and the lowest operating-noise levels while vertical mounting stiffens the board and eases assembly. Once the decision is made to incorporate either style, the designer can proceed with the board layout *(Fig. 5)*.

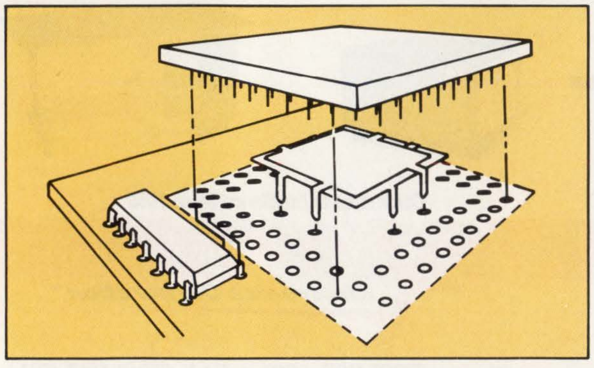
IMPEDANCE-ANALYSIS-DATA SUMMARY FOR VARIOUS DECOUPLING METHODS

Decoupling Method	Capacitance(2) (μF)	ESR (Ω)	f_0 (MHz)	f_1(3) (MHz)	$\|Z_1\|$ (4) (Ω)	L_{calc} (nH)
Decoupled Socket	0.333	.038	2.1	20.8	2.39	18.3
Discrete(1) MLC chip	0.330	.119	2.1	20.8	2.56	19.6
Under-the-DIP flat decoupling capacitor	0.300	.068	3.1	31.6	2.18	11.0

(1) This includes approximately 1.1 in (27).94 mm) of total pc-board traces. Trace width = 0.1 in (2.54 mm).
(2) Measured at 1.0 kHz, 1.0 V rms and 25°C
(3) Frequency used for inductance calculation
(4) Impedance magnitude at f_1

Even though there are application-specific ICs, not one decoupling-capacitor configuration exists that suits all needs. The under-the-DIP bypass capacitors are available in enough different sizes and pinouts to decouple virtually any DIP. These would include such devices as Zilog's Z80, Advanced Micro Devices' 2910, Texas Instruments' TMS32010, and center-pinout DIPs, as well as other MPUs and logic devices with non-standard corner power and ground pins.

One packaging innovation that makes bypassing a thorny problem is pin-grid-array (PGA) packages. These devices include 16- and 32-bit microprocessors, digital-signal processors, graphic-signal processors, gate arrays, standard cells, and ASICs. Very-low-inductance decoupling capacitors specifically designed to be through-hole-mounted under PGAs, PGA sockets, and plastic-leaded chip carriers are now available *(Fig. 6)*.



6. Flat decoupling capacitors for pin-grid arrays, such as Rogers Corp.'s Micro/Q 3000 decoupling capacitor, fit the inside area of the array. It's the dimension of the inside perimeter of pins that sets the size limit, not the number of PGA pins.

These flat capacitors to be used with pin-grid arrays consist of one capacitor with multiple leads. For example, an eight-pin have four pins that are common to each capacitor plate. By having power and ground on each side of the capacitor, the distance between the power pins of the PGA IC and those of the capacitor is minimized.

The capacitor must be sized to fit the inside area of the PGA. The dimension of the inside perimeter of pins sets the limit on size, not the number of PGA pins *(Fig. 6, again)*. This inside perimeter, or gap, is typically square. Inserting the flat capacitor into a pc board requires additional board holes for the appropriate gap size. As long as the gap is taken into consideration, one capacitor configuration can decouple various PGA packages with the same gap, regardless of pin locations.

With these new decoupling and power-distribution options, designers are more assured that their systems will operate as intended and without unexpected noise or stability problems. New systems will benefit from a more rational approach to decoupling.

Michael Scott Hyslop, applications-engineering manager at the Circuit Components Division of Rogers Corp., received a BSEE from Arizona State University, Tempe.

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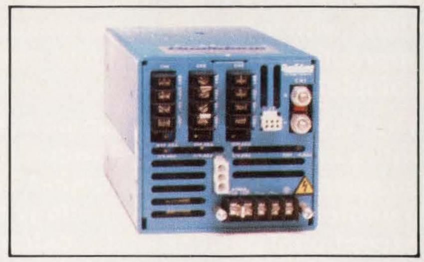

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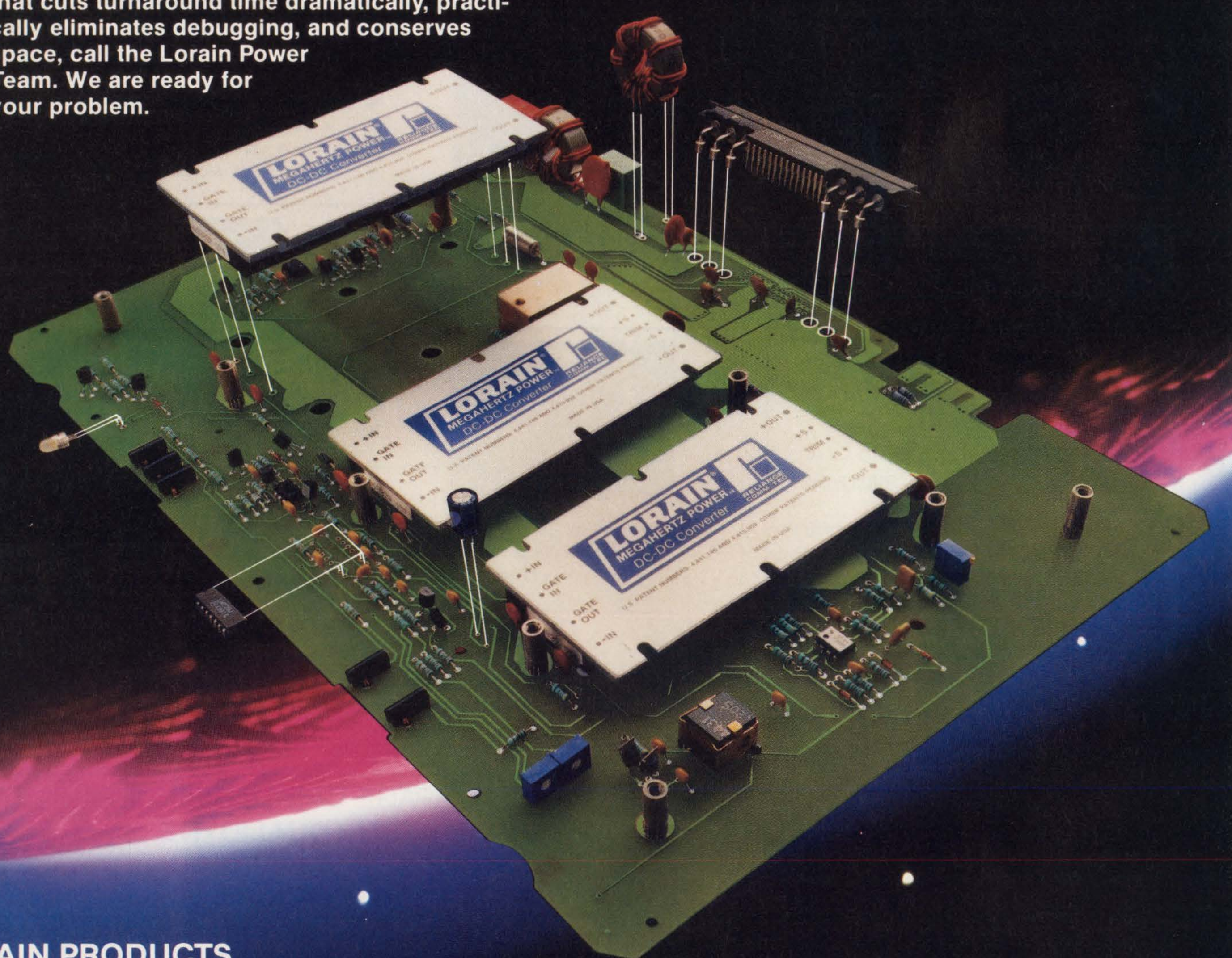
Custom Lorain® Megahertz Power™ Supplies

It seems that every custom power supply project starts with inflexible performance specifications, impractical space limitations, and unrealistic completion schedules.

That is why Lorain custom power supplies start with Lorain Megahertz Power Modules. These compact, field proven modules contain a patented megahertz technology that provides exceptional power density, extremely high operating efficiency, quiet operation, and agency compliance. There are over 170 master and booster modules to accurately meet your system requirements.

To these, we add custom circuitry to match your input and output specifications; design-in visuals, forced load sharing, and other peripheral components; even allow for future expansion capabilities with additional plug-in booster modules.

If you are looking for a custom power solution that cuts turnaround time dramatically, practically eliminates debugging, and conserves space, call the Lorain Power Team. We are ready for your problem.



LORAIN PRODUCTS
1122 F Street, Lorain, OH 44052-2293, (216) 288-1122

RELIANCE COMM/TEC, CANADA
St. Thomas, ONT., (519) 631-0780

RELIANCE COMM/TEC

CIRCLE 133

RESISTOR MANUFACTURERS

AVX Corp.
A Kyocera Group Co.
Box 867
Myrtle Beach, SC 29577
(803) 448-9411
(TF) (CH) (TR) (RN)
CIRCLE 300

Allen-Bradley Co.
Electronic Comp. Div.
1414 Allen-Bradley Dr.
El Paso, TX 79936-6415
(915) 592-4888
(CC)
CIRCLE 301

Allen-Bradley Co.
Div. of Rockwell Int'l. Corp.
1201 S. Second St.
Milwaukee, WI 53204
(414) 382-2000
(CC)
CIRCLE 302

Beckman Industrial Corp.
4141 Palm St.
Fullerton, CA 92635
(714) 447-2345
(TF) (TH) (ST) (MT) (CE)
CIRCLE 303

Bourns Inc.
1200 Columbia Ave.
Riverside, CA 92507
(714) 781-5071
(CE) (TF) (WW) (CH) (ST) (MT) (TR) (RN)
CIRCLE 304

Bradford Electronics Inc.
550 High St.
Bradford, PA 16701-9520
(814) 362-5635
(CF) (CE) (MN) (TF) (TH) (GL) (HR) (MO) (WW) (CH)
CIRCLE 305

Brel Int'l. Components
1621 University Pkwy.
Sarasota, FL 34243
(813) 355-9791
(CF) (CE) (MN) (TF) (HR) (MO) (WW) (CH) (CO) (ST) (MT)
CIRCLE 306

CTS Corp.
Frequency Control Div.
400 Reimann Ave.
Sandwich, IL 60548
(815) 786-8411
(CC) (CE) (TF) (TH) (WW) (CO) (ST) (MT) (TR) (RN)
CIRCLE 307

CTS Corp.
Resistor Network Div.
406 Parr Rd.
Berne, IN 46711
(219) 589-3111
(CE) (TF) (CF) (CO)
CIRCLE 308

Caddock Electronics Inc.
1717 Chicago Ave.
Riverside, CA 92507
(714) 788-1700
(MN) (TF) (HR) (MO) (RN)
CIRCLE 309

Capar
8243 Jericho Tpke.
Woodbury, NY 11797
(516) 367-7676
(CF) (MN) (MO) (CH)
CIRCLE 310

The Carborundum Co.
345 Third St.
Niagara Falls, NY 14302
(716) 278-3940
(CR)
CIRCLE 311

Cermetek Microelectronics Inc.
1308 Borregas Ave.
Sunnyvale, CA 94088-3565
(408) 752-5000
(CF) (TF) (TH)
CIRCLE 312

Clarostat Mfg. Co.
1 Washington St.
Dover, NH 03820
(603) 742-1120
(AU) (CC) (CE) (MN) (TF) (HR) (WW) (CO) (ST) (MT) (TR)
CIRCLE 313

D1 Products Inc.
95 E. Main St.
Huntington, NY 11743
(516) 673-6866
(CC) (CF) (MN) (MO) (WW) (ST) (MT)
CIRCLE 314

Dale Electronics Inc.
2064 12th Ave., Box 609
Columbus, NE 68601
(402) 564-3131
(CF) (CE) (MN) (TF) (TH) (GL) (HR) (MO) (WW) (CH) (CO) (ST) (MT) (TR) (RN)
CIRCLE 315

Dale Electronics Inc.
Tempe Div.
1155 W. 23rd. St.
Tempe, AZ 85282
(602) 967-7874
(CE) (ST) (MT)
CIRCLE 316

Electro-Films Inc.
111 Gilbane St.
Warwick, RI 02886
(401) 738-9150
(TH) (CH)
CIRCLE 317

Electronic Components Int'l.
121 Sheldon St.
El Segundo, CA 90245
(213) 322-7205
(CF) (CO)
CIRCLE 318

Electronic Precision Components
519 S. Fifth Ave.
Mt. Vernon, NY 10550
(914) 664-2333
(WW)
CIRCLE 319

Ericsson Components Inc.
Box 853904
Richardson, TX 75085-3904
(214) 480-8300
(TF)
CIRCLE 320

Hipotronics Inc.
P.O. Drawer A
Brewster, NY 10509
(914) 279-8091
(WW)
CIRCLE 321

Hycomp Inc.
165 Cedar Hill St.
Marlborough, MA 01752
(508) 485-6300
(TH) (CH)
CIRCLE 322

IRC Inc.
Greenway Rd., Box 1860
Boone, NC 28607
(800) 255-4472
(CE) (CO) (CC) (CF) (MN) (TF) (TH) (GL) (HR) (MO) (WW) (CH)
CIRCLE 323

International Mfg. Services
50 Schoolhouse Lane
Portsmouth, RI 02871-2418
(401) 683-9700
(TF)
CIRCLE 324

Iskra Electronics Inc.
222 Sherwood Ave.
Farmingdale, NY 11735
(800) 862-2101
(CF) (CE) (ST) (MT) (CF) (CE)
CIRCLE 325

KCK America Inc.
A Mitsubishi Co.
930 Remington Rd.
Schaumburg, IL 60173-4516
(312) 884-8688
(TF) (CH)
CIRCLE 326

KOA Speer Electronics Inc.
Box 547
Bradford, PA 16701
(814) 362-5536
(CF) (MN) (TF) (MO) (CH)
CIRCLE 327

Litton Systems Inc.
Potentiometer Div.
750 S. Fulton St.
Mount Vernon, NY 10550
(914) 664-7733
(CF) (CO) (ST) (MT)
CIRCLE 328

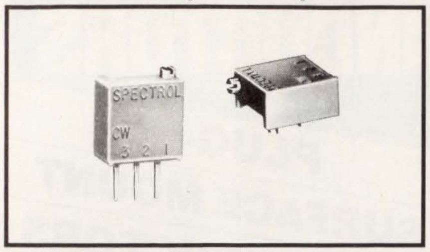
(continued on p. 126)

KEY

Resistors

(AU)	Audio
(CC)	Carbon composition
(CF)	Carbon film
(CE)	Cermet
(MN)	Metal/non-metal film
(TF)	Thick film
(TH)	Thin film
(GL)	Glass
(HR)	High resistance
(MO)	Metal oxide
(WW)	Wire-wound
(CH)	Chip
(CO)	Conductive plastic
(ST)	Single-turn pot
(MT)	Multi-turn pot
(TR)	Trimmers
(RN)	Resistor networks
(CR)	Ceramics

Multi-Turn Cermet Trimmer Measures Only 3/8" Square



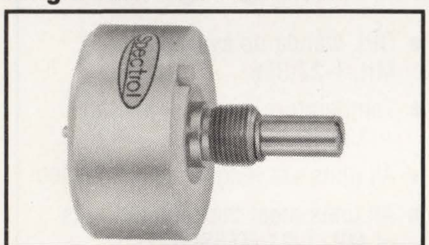
Spectrol's 3/8" square multi-turn cermet trimmer, the Model 64, offers five package/terminal styles to choose from. The unit is available in three side-adjust and two top-adjust versions, with pin configurations to suit any standard PCB application. This low cost space saver is available in resistance ranges from 10 ohms to 2 megohms with a ±10% resistance tolerance. It also features solder plated terminals, an integral multi-finger wiper contact, superior setability and stability, a TEMPCO of ±100 PPM/°C, a CRV of 3%, and is sealed for solvent and aqueous cleaning. Power rating 0.5 W at 85°C.

Spectrol®

Spectrol Electronics Corporation
P.O. Box 1220, La Puente, CA 91749
Phone: (818) 964-6565 Fax: (818) 810-1093

CIRCLE 222

Spectrol Offers Low Cost Single-Turn Precision Pots



Spectrol offers single-turn precision potentiometers for position sensing and panel control applications. These rugged, low cost 1-5/16 inch diameter pots offer a choice of resistive elements and are well suited for industrial usage where reliable service and long life are essential. The Model 132 features a low noise wirewound element. The Model 138 and Model 139 feature infinite resolution with conductive plastic and cermet resistive elements, respectively. Other specifications include a resistance range of 5Ω to 2MΩ, standard linearity of 0.5%, operating temperature of −55°C to +125°C and the choice of center taps, continuous rotation or mechanical stops.

Spectrol®

Spectrol Electronics Corporation
P.O. Box 1220, La Puente, CA 91749
Phone: (818) 964-6565 Fax: (818) 810-1093

CIRCLE 223

RESISTORS

▼ TINY CHIP RESISTOR NOW IN PRODUCTION

The industry's smallest surface-mountable chip resistor has an external package about the size of a pinhead. Measuring just 1 by 0.5 mm, Rohm's MCR 01 occupies 60% less board space than the company's earlier midget, its MCR 03. The new chip also weighs 75% less than its predecessor. Rated voltage for the MCR 01 is 0.032 W at 70°C with a maximum operating voltage of 25 W. The resistance range is from 5.6 Ω to 1.5 MΩ with tolerance of ±5%. The part operates from −55 to +125°C. The MCR 01 costs $35 per 1000 pieces. It's available in 5000-piece reels of 8-mm paper tape. Delivery is in 12 weeks from receipt of order.

Rohm Corp.
Electronics Division
8 Whatney
Irvine, CA 92718
(714) 855-2131.
▶ **CIRCLE 653**

▼ WIREWOUND RESISTORS FOR TRIMMING TASKS

Two types of microminiature wirewound resistors are available for temperature-compensating and trimming applications. Type 401 comes in three models that range in value from 500 Ω to 30 kΩ and handle a maximum voltage of 75 V dc. All are rated for 0.05 W at 70°C. Tolerances are from 0.05% to 20%. Type D-100 also comes in three models and range in value from 10 Ω to 25 kΩ. A flat surface on the device facilitates bonding for excellent response time. They're also rated for 0.05 W and come in tolerances from 1% to 20%. All feature wirewound epoxy construction, excellent repeatability, and rapid response time. Call for pricing and availability.

Micro-Ohm Corp.
1088 Hamilton Rd.
Duarte, CA 91010
(818) 357-5377
▶ **CIRCLE 495**

RESISTOR MANUFACTURERS

Mepcopal Co.
11468 Sorrento Valley Rd.
San Diego, CA 92121
(619) 453-0332
(CE) (WW) (ST) (MT)
CIRCLE 329

Micro Ohm Corp.
1088 Hamilton Rd.
Duarte, CA 91010
(818) 357-5377
(CF) (MN) (HR) (MO) (WW)
CIRCLE 330

Milwaukee Resistor Corp.
700 West Virginia St.
Milwaukee, WI 53204-0219
(414) 271-9900
(WW)
CIRCLE 331

Mini-Systems Inc.
Thick/Thin-Film Div.
20 David Rd.
North Attleboro, MA 02760
(508) 695-0203
(CE) (TF) (TH) (HR) (CH) (RN)
CIRCLE 332

Murata Erie
North America Inc.
2200 Lake Park Dr.
Smyrna, GA 30080
(404) 436-1300
(HR) (CH)
CIRCLE 333

NTE Electronics Inc.
44 Farrand St.
Bloomfield, NJ 07003
(201) 748-5089
(MN) (MO) (WW)
CIRCLE 334

Noble U.S.A. Inc.
5450 Meadowbrook Ind. Ct.
Rolling Meadows, IL 60008
(708) 364-6038
(CF) (CE) (GL) (HR) (MO) (WW) (ST) (TR)
CIRCLE 335

Nytronics Inc.
700 Orange St.
Darlington, SC 29532
(803) 393-5421
(WW)
CIRCLE 336

Ohmite Mfg. Co.
Div. of North American Philips
3601 Howard
Skokie, IL 60076
(312) 675-2600
(CC) (CF) (MN) (HR) (WW)
CIRCLE 337

Ohmtek Inc.
2160 Liberty Dr.
Niagara Falls, NY 14304
(716) 283-4025
(TF) (TH) (HR) (CH)
CIRCLE 338

PCA Electronics Inc.
16799 Schoenborn St.
Sepulveda, CA 91343
(818) 892-0761
(TH)
CIRCLE 339

Panasonic Industrial Co.
Electronic Comp. Div.
Two Panasonic Way
Secaucus, NJ 07094
(201) 348-5244
(AU) (CC) (CE) (CO) (ST) (MT) (TR)
CIRCLE 340

Philips Components
Discrete Products Div.
2001 W. Blue Heron Blvd.
Riviera Beach, FL 33404
(407) 881-3308
(CE) (TF) (TH) (ST) (TR) (RN)
CIRCLE 341

Piher International Corp.
903 Feehanville Dr.
Mount Prospect, IL 60056
(708) 390-6680
(CC) (CF) (CE) (MN) (MO) (WW) (CH) (ST) (MY) (TR) (RN)
CIRCLE 342

Preh Electronic Industries
470 E. Main St.
Lake Zurich, IL 60047-2578
(708) 438-4000
(CF) (CE) (TF) (TR)
CIRCLE 343

(continued on p. 129)

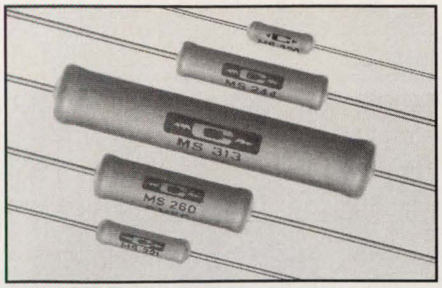
KEY

Resistors

(AU)	Audio
(CC)	Carbon composition
(CF)	Carbon film
(CE)	Cermet
(MN)	Metal/non-metal film
(TF)	Thick film
(TH)	Thin film
(GL)	Glass
(HR)	High resistance
(MO)	Metal oxide
(WW)	Wire-wound
(CH)	Chip
(CO)	Conductive plastic
(ST)	Single-turn pot
(MT)	Multi-turn pot
(TR)	Trimmers
(RN)	Resistor networks
(CR)	Ceramics

New

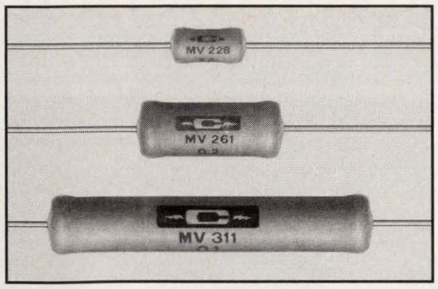
Type MS Precision Power Film Resistors



Power Rating up to 15 Watts
- **Non-Inductive Design** with power ratings from 2 Watts to 15 Watts
- Select from 17 Models
- Voltage ratings from 200 V to 6 KV
- Resistance Range 20 Ω to 30 Meg
- Tolerance of 1% (available to 0.1%)
- Max. Operating Temperature of 275°C

For Type MS data, circle number 90

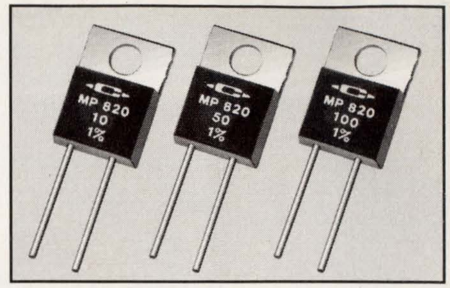
Type MV Low Resistance Power Film Resistors



Resistance Range of 0.1 Ω to 50 Ω
- **Non-Inductive Design** with power ratings from 1.5 Watts to 10 Watts
- Select from 5 Models
- Tolerance of 1%, 2%, 5% or 10%
- Max. Operating Temperature of 275°C

For Type MV data, circle number 91

Type MP Kool-Tab® Power Film Resistors



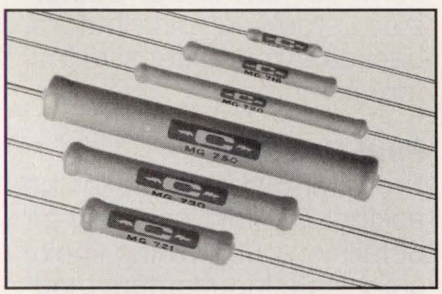
20 Watts in the TO-220 Package
- **Non-Inductive Design**
- Resistance Range 1 Ω to 10 K
- 20 Watts at 25°C Case Temperature
- Tolerance of 1%, 2%, 5% or 10%

For Type MP data, circle number 92

CADDOCK® Resistor Technology

High Performance Power Resistors and High Voltage Resistors with a 25 year record for solving problems across the board!

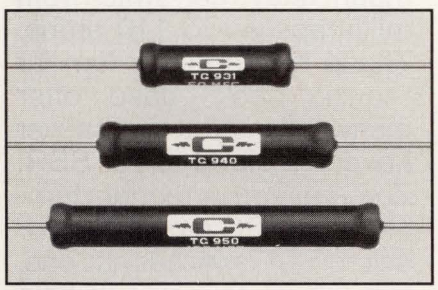
Type MG Precision High Voltage Resistors



Voltage Ratings from 600V to 48KV
- 80 ppm/°C, -15°C to 105°C, ref. 25°C
- Resistance Range up to 10,000 Meg
- Select from 23 Models
- Tolerance of 1% (available to 0.1%)
- Stability of 0.5% per 1,000 hours

For Type MG data, circle number 93

Type TG Low TC Precision High Voltage Resistors

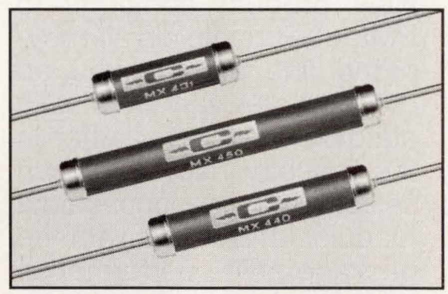


TC of 25 ppm/°C, -55°C to +125°C
- Resistance Range 1 Meg to 1,000 Meg
- 7 Models with Voltage Ratings from 4 KV to 48 KV
- Voltage Divider Match Sets with **Ratio TC to as tight as 10 ppm/°C**
- Tolerance of 1% (available to 0.1%)
- Stability of 0.25% per 1,000 hours

For Type TG data, circle number 94

New

Type MX Lab Grade High Voltage Resistors



New Cost Efficient Design
- 80 ppm/°C, 0°C to 70°C, ref. 25°C
- Resistance Range 1 Meg to 2,000 Meg
- 7 Models with Voltage Ratings from 7.5 KV to 48 KV
- Tolerance of 1%, 2%, 5% or 10% (available to 0.1%)
- Stability of 0.5% per 1,000 hours

For Type MX data, circle number 95

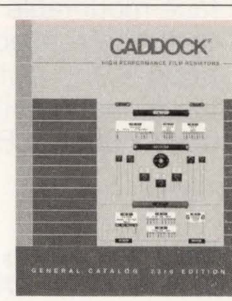
More high performance resistor products from

CADDOCK
ELECTRONICS, INCORPORATED

These products are manufactured with Caddock's exclusive Micronox® or Tetrinox® Resistance Film Technologies. For your copy of the Caddock General Catalog call or write:

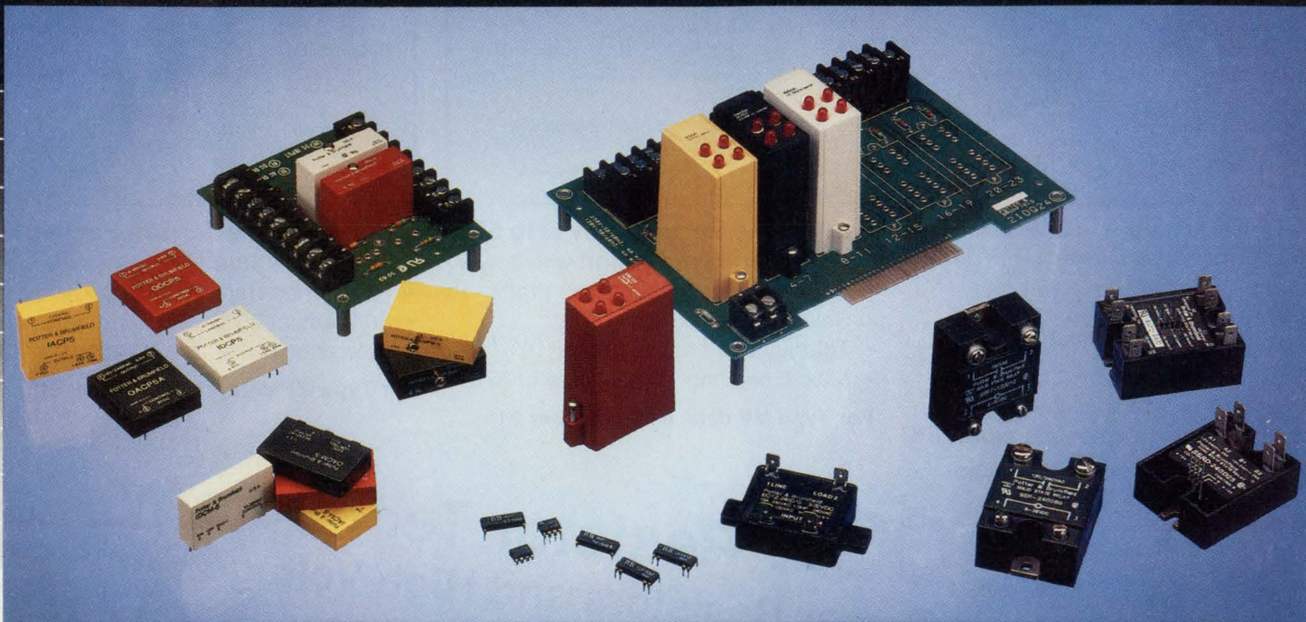
Applications Engineering
Caddock Electronics, Inc.
1717 Chicago Avenue
Riverside, California 92507
(714) 788-1700

The Caddock General Catalog includes specifications on over 200 models of high performance resistor products.



L121.119

Potter & Brumfield offers the solid state I/O module and relay options you need.



Expanded Offering
New product additions to Potter & Brumfield's already-broad line provide you an even greater variety of solid state products, unmatched in the industry. Now you can select solid state input/output modules and relays with the package style, performance and features just right for your application.

Input/Output Modules
Why force your design to fit around one or two standard configurations? P&B offers six different package styles for design flexibility. From plug-in quad modules to surface-mountable DIP units, our optically-isolated I/O modules provide the options and the traditional quality you expect from Potter & Brumfield.

Solid State Relays
Our new family of chassis mount relays can switch from milliamps up to 110 amps. These relays in our familiar "hockey-puck" case offer many options you might never have imagined in an SSR. Zero-voltage or random turn-on. AC or DC input. Triac or paired-SCR switches and one, two or even four outputs help open the door to your creative design. At the other end of the spectrum, DIP solid state relays put reliable P&B solid state switching of loads up to 1 amp right on your printed circuit board. And you have a choice of conventional or surface mount terminals.

Stock Availability
Most models are available from stock through our nationwide network of authorized stocking distributors, backed by our extensive factory inventory.

Find Out More
Free literature is yours for the asking. Contact us today for details on our growing line of solid state input/output modules and relays. Potter & Brumfield, A Siemens Company, 200 South Richland Creek Drive, Princeton, Indiana 47671-0001.

Call toll-free 1-800-255-2550 for the P&B authorized distributor, sales representative or regional sales office serving your area.

Potter & Brumfield **A Siemens Company**

8806

CIRCLE 189

RESISTOR MANUFACTURERS

RCD Components Inc.
520 E. Industrial Park Dr.
Manchester, NH 03103
(603) 669-0054
(CC) (CF) (CE) (MN) (TF) (TH) (GL) (HR) (MO) (WW) (CH)
CIRCLE 344

Robert G. Allen Co.
7267 Coldwater Canyon
North Hollywood, CA 91605
(818) 765-8300
(AU) (CC) (CF) (CE) (MN) (TF) (TH) (GL) (HR) (MO) (WW) (CH) (CO) (RN)
CIRCLE 345

Rohm Corp.
Rohm Electronics Div.
8 Whatney
Irvine, CA 92718
(714) 855-2131
(CF) (MN) (TF) (MO) (CH) (ST) (MT) (RN)
CIRCLE 346

Shokai Far East Ltd.
280 N. Central Ave.
Hartsdale, NY 10530
(914) 681-0700
(CC) (CF) (CE) (MN) (MO) (WW)
CIRCLE 347

Silicon Sensors Inc.
Old Hwy. 18 East
Dodgeville, WI 53533
(608) 935-2707
(CE)
CIRCLE 348

Solitron Devices Inc.
Semiconductor Div.
1177 Blue Heron Blvd., #1
Riviera Beach, FL 33404
(407) 848-4311
(CE) (MN) (TH) (CH) (TR) (RN)
CIRCLE 349

Spectrol Electronics Corp.
Box 1220
La Puente, CA 91749
(818) 964-6565
(ST) (MT)
CIRCLE 350

Sprague Electric Co.
Aluminum Capacitor Div.
Box 9102
Mansfield, MA 02048
(800) 777-7575
(TF)
CIRCLE 351

Stackpole Carbon Co.
Stackpole St.
St. Marys, PA 15857
(814) 781-1234
(HR)
CIRCLE 352

State of the Art Inc.
2470 Fox Hill Rd.
State College, PA 16803-1797
(814) 355-8004
(TF) (TH) (HR)
CIRCLE 353

TDK Corporation of America
1600 Feehanville Dr.
Mount Prospect, IL 60056
(708) 803-6100
(RN)
CIRCLE 354

Taiyo Yuden (USA), Inc.
714 W. Algonquin Rd.
Arlington Heights, IL 60005
(708) 364-6104
(RN)
CIRCLE 355

Ultronix Inc.
Box 1090
Grand Junction, CO 81502
(303) 242-0810
(WW) (CH) (CE) (ST) (MT)
CIRCLE 356

United Chemi-Con Inc.
9801 W. Higgins Rd.
Rosemont, IL 60018
(312) 696-2000
(TH)
CIRCLE 357

Vishay Resistive Systems Group
63 Lincoln Hwy.
Malvern, PA 19355
(215) 644-1300
(MN) (TF) (YH) (GL) (WW) (CH) (ST) (MT)
CIRCLE 358

Voltronics Corp.
Box 476
East Hanover, NJ 07936
(201) 887-1517
(CC) (CF) (TF) (HR) (CO) (ST)
CIRCLE 359

Zenith Electronics Corp.
1000 Milwaukee Ave.
Glenview, IL 60025
(312) 391-7733
(TF) (CH)
CIRCLE 360

KEY

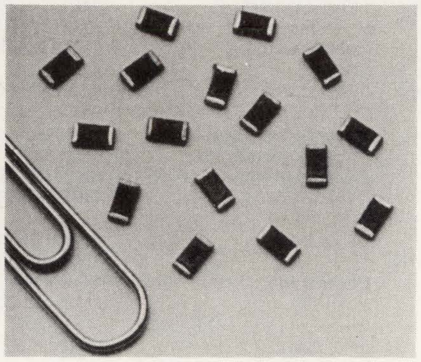
Resistors

(AU)	Audio
(CC)	Carbon composition
(CF)	Carbon film
(CE)	Cermet
(MN)	Metal/non-metal film
(TF)	Thick film
(TH)	Thin film
(GL)	Glass
(HR)	High resistance
(MO)	Metal oxide
(WW)	Wire-wound
(CH)	Chip
(CO)	Conductive plastic
(ST)	Single-turn pot
(MT)	Multi-turn pot
(TR)	Trimmers
(RN)	Resistor networks
(CR)	Ceramics

RESISTORS

▼ CHIP RESISTOR IS SURFACE MOUNTABLE

Rated for 100 mW at 70°C, the TNPW0805 international-standard-sized 0805 (2.0 mm by 1.25 mm) thin-film resistor chip comes in values from 10 Ω to 100 kΩ with ±0.5% tolerance. Tolerances of ±0.1% are also available with a short lead time. The standard thermal constant is ±25



ppm/°C for values of 100 Ω and higher and ±50 ppm/°C under 100 Ω. The TNPW0805 is a companion to the older TNPW1206, a 125-mW thin-film chip resistor that ranges between 49.9 Ω to 1 MΩ at 0.1% tolerance. Both feature solder-coated, nickel-barrier, wrap-around terminations that are compatible with surface-mounting assembly techniques such as vapor-phase and infrared soldering. The resistors come on tape and reel with 500 pieces per reel or in bulk. The typical cost for a 1-kΩ TNPW0805 with a ±0.5% tolerance and temperature coefficient of ±25 ppm/°C is $0.105 each in quantities of 10,000. Delivery is from stock in four weeks.

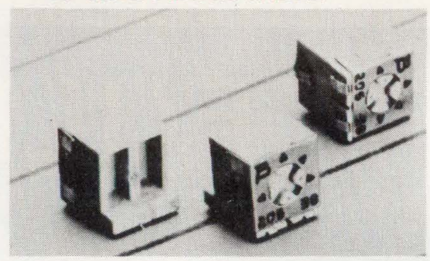
Dale Electronics Inc.
1122 23rd St.
Columbus, NE 68601-3647
(402) 644-4244
▶ **CIRCLE 493**

▼ TINY ST-4 TRIMMERS NOW MADE HERE

The ST-4 trimmer resistor, at 4.5 by 5 by 2.3 mm, is still the smallest and thinnest sealed single-turn unit available for surface mounting. Mepcopal now makes the trimmers in the U.S. The device withstands dip or reflow soldering temperatures up 260°C for 10 s, and manual-soldering temperatures up to 350°C for 3 s. The operating-temperature range is −55 to 125°C, the resistance range is 10 Ω to 2 MΩ, and the resolution is infinite. The trimmer can handle input voltages up to 200 V dc at 0.25 W and 70°C, derated to zero watts at 125°C. Rotational life is 100 cycles with a maximum shaft torque of 100 gcm. With a metal-alloy brush wiper and 1% maximum CRV, the ST-4 withstands thermal shock of −65 to 125°C, mechanical shock of 100 G, and vibration of 20 G at 10 to 200 Hz. Sealed with an O-ring, the trimmer passes the Flourinert leak test at 85°C and withstands high-temperature exposure of 125°C for 250 hrs. Reeled tape packaging provides 12-mm tape width, 8-mm part pitch, and 178-mm reel diameter for automatic placement. In 500-piece quantities, they cost $1.05 each. Prototypes are available immediately; production quantities take eight to 12 weeks.

Mepcopal Co.
11468 Sorrento Valley Rd.
San Diego, CA 92121
(619) 453-0332
▶ **CIRCLE 494**

▼ SEALED TRIMMER IS SIDE ADJUSTABLE

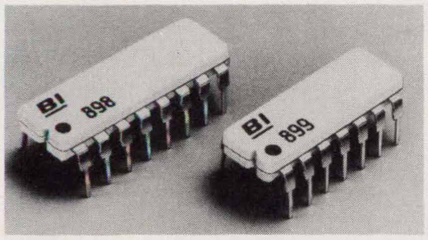


A side-adjustable, 4-mm sealed trimmer is surface-mounted on the edge of a circuit board for easy access from outside the housing of the end product. The 3314S is the latest addition to the 3314 family of trimmers, which includes top-adjusting and through-hole models. Applications include instrumentation and test and measurement systems, pagers, cellular phones, oscilloscopes, power supplies, video cameras, security alarms, factory automation, and process controls. Packaging specifications for 7-in. reels of 200 units, 13-in. reels of 100 units, and tubes of 100 units meet EIA standards. When packaged in tubes, the cost is $1.70 per trimmer.

Bourns Inc.
1200 Columbia Ave.
Riverside, CA 92507
(714) 781-5500
▶ **CIRCLE 636**

▼ LADDER NETWORKS HOLD VALUE OVER TEMPERATURE

Both 8- and 10-bit versions are available of thick-film ladder networks from Beckman Industrial. The models 898-8X and 899-10 networks are accurate to ±1/2 LSB (8 bits) and ±1 LSB (10 bits), respectively, and their

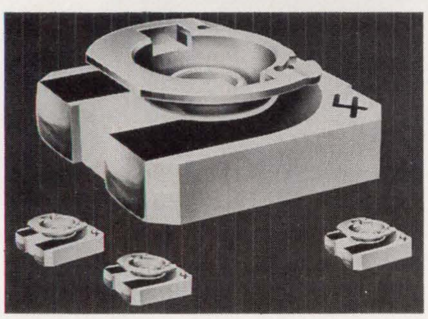


accuracies are maintained over the zero-to-70°C temperature range. Standard ladder impedances are 10kΩ/20kΩ, 25kΩ/50kΩ, 50kΩ/100kΩ, and 100kΩ/200kΩ. The 899 and 898 series are packaged in 14- and 16-pin ceramic DIPs, respectively. Call for pricing and availability.

Beckman Industrial Corp.
4141 Palm St.
Fullerton, CA 92635
(714) 447-2345
▶ **CIRCLE 646**

▼ 3-MM SMT TRIMMER FITS IN TIGHT SPACES

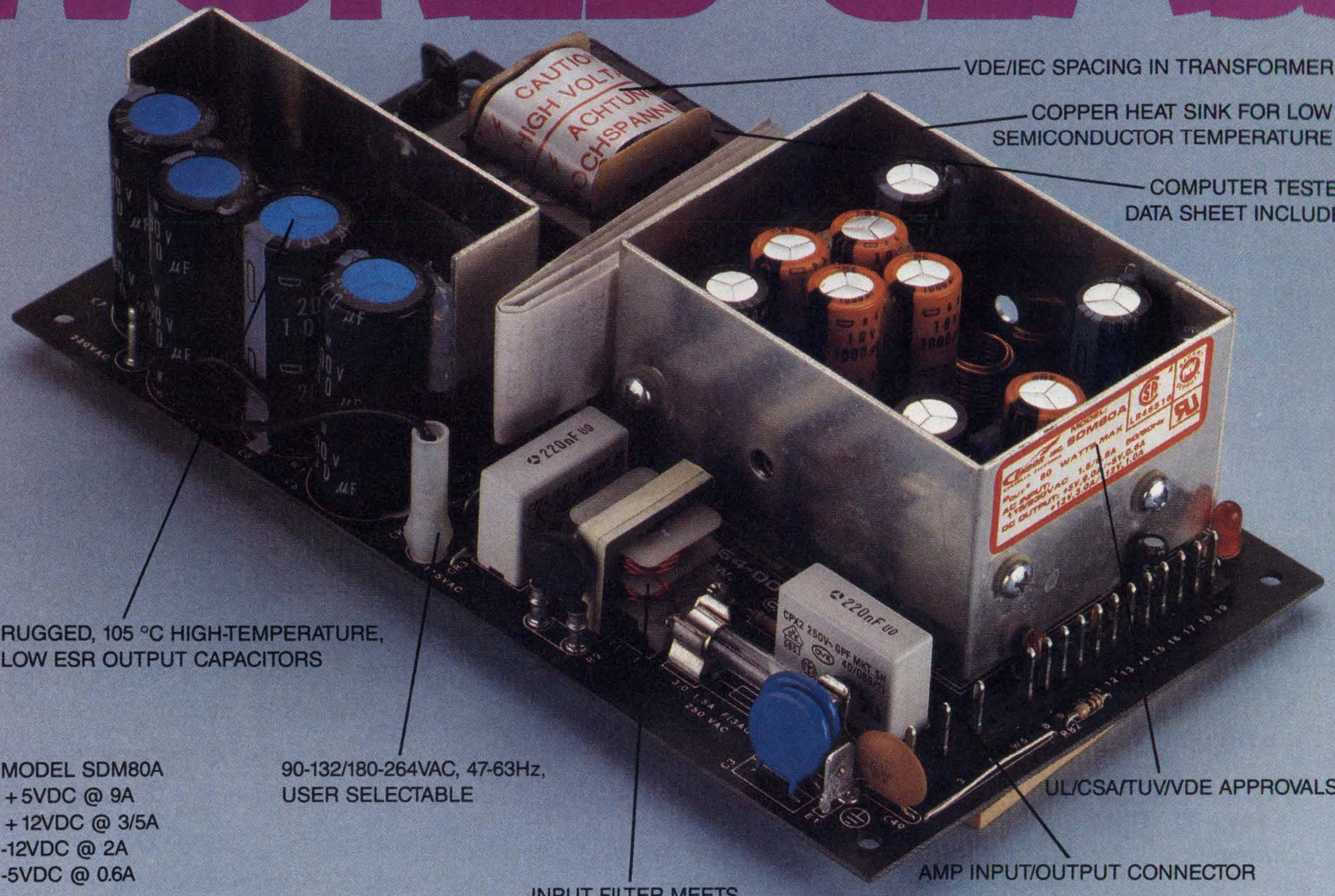
The model 3363 surface-mounted trimmer features what the company calls the industry's smallest 3-mm design. The device meets both EIA and EIAJ standards. Features include superior termination-pad ge-



ometry for improved solderability. The trimmer comes in an 8-mm embossed tape and carries values from 100 Ω to 1 MΩ with 5% maximum contact-resistance variation. In low volumes, the 3363 trimmer starts at $.395.

Bourns Inc.
1200 Columbia Ave.
Riverside, CA 92507
(714) 781-5500.
▶ **CIRCLE 647**

WORLD CLASS



Condor's SDS and SDM Series power supplies meet FCC/VDE Level B and have agency safety approvals!

Want a tough, versatile, well-designed power supply for your next application? Try a single (SDS) or multiple (SDM) output model from Condor!

Every Condor SDS or SDM power supply meets the toughest domestic and international safety requirements, and is UL, CSA and TUV/VDE certified. All units also meet FCC 20870 Level B and VDE 0871 Class B above 150KHz.

SDS/SDM Series features:

- 5 power levels — 45 to 200 watts
- 20 single and 29 multiple-output models (up to 5 outputs)
- Clean, low-cost, open-frame design
- Fully protected — adjustable current limit, built-in OVP and reverse voltage protection
- Full load burn-in and 2-year warranty
- LED "on" indicator
- Powerfail signal and logic inhibit on 140 and 200W levels
- High peak current disk drive outputs plus closely regulated 3-terminal-type outputs
- Extremely versatile output configurations for tough applications
- Very high value for your purchasing dollar
- Isolated outputs can be used for positive or negative sources or in series with other outputs
- Pass vibration and shock per MIL-STD 810D

Call us today and find out how a Condor SDS or SDM world-class power supply can meet your most demanding design requirements!

Send for our free catalog!

250 power supplies!
Switchers and linears!
Open frame and enclosed!
Custom capability!

CONDOR INC.
DC POWER SUPPLIES

2311 Statham Parkway, Oxnard, CA 93030
(805) 486-4565 • TWX: 910-333-0681
FAX: (805) 487-8911
CALL TOLL-FREE: 1-800-235-5929 (outside CA)

CIRCLE 87

CAPACITOR MANUFACTURERS

ASC
21541 Blythe St.
Canoga Park, CA 91304
(818) 710-8555
(FL) (FP) (FY) (FT) (FF) (CN)
CIRCLE 361

AVX Corp.
A Kyocera Group Co.
Box 867
Myrtle Beach, SC 29577
(803) 448-9411
(CM) (ED) (CG) (CP) (CN)
CIRCLE 362

Aerovox Inc.
740 Belleville Ave.
New Bedford, MA 02745
(508) 994-9661
(FY)
CIRCLE 363

American Precision Industries Delevan Div.
270 Quaker Rd.
East Aurora, NY 14052
(716) 652-3600
(CM) (CP)
CIRCLE 364

Arco Electronics Inc.
9822 Independence Ave.
Chatsworth, CA 91311
(818) 882-8707
(CM) (EA) (ED) (FP) (MI) (CP)
CIRCLE 365

Bourns Inc.
1200 Columbia Ave.
Riverside, CA 92507
(714) 781-5071
(CN)
CIRCLE 366

Brel Int'l. Components
1621 University Pkwy.
Sarasota, FL 34243
(813) 355-9791
(CD) (CM) (EA) (ED) (EW)
(FL) (FP) (FY) (FT) (CN) (CP)
CIRCLE 367

Capar
8243 Jericho Tpke.
Woodbury, NY 11797
(516) 367-7676
(CD) (CM) (EA) (ED) (FP)
(FY) (MI) (CP)
CIRCLE 368

Component Research Co. Inc.
1655 26th St.
Santa Monica, CA 90404
(213) 829-3615
(FL) (FP) (FY) (FT) (FF) (TE)
(CN)
CIRCLE 369

Cornell-Dubilier
Sangamo Comp. Div.
1605 E. Rodney French Blvd.
New Bedford, MA 02744
(508) 996-8561
(EA) (EW) (FL) (FP) (FY) (MI)
CIRCLE 370

D1 Products Inc.
95 E. Main St.
Huntington, NY 11743
(516) 673-6866
(AI) (CD) (CM) (EA) (FL) (FP)
(FY) (FT)
CIRCLE 371

Eldre Corp.
1500 Jefferson Rd.
Rochester, NY 14623
(716) 427-7280
(CD)
CIRCLE 372

Electro-Films Inc.
111 Gilbane St.
Warwick, RI 02886
(401) 738-9150
(CN)
CIRCLE 373

Electronic Components Int'l.
121 Sheldon St.
El Segundo, CA 90245
(213) 322-7205
(CD) (CM) (EA) (FP) (FY) (FT)
CIRCLE 374

GTE Corp.
Elec. Components and Materials
2401 Reach Rd.
Williamsport, PA 17701
(717) 326-6591
(CN) (CP)
CIRCLE 375

Globtek Inc.
7700 Marine Rd.
North Bergen, NJ 07047
(201) 861-0246
(EA) (FP) (FY)
CIRCLE 376

Hipotronics Inc.
P.O. Drawer A
Brewster, NY 10509
(914) 279-8091
(CN)
CIRCLE 377

Horizon Capacitor Corp.
2012 W. St. Paul Ave.
Chicago, IL 60647
(312) 252-2211
(FL) (FP) (FY) (FT) (FF) (TE)
(CN)
CIRCLE 378

ITT Components
1201 E. McFadden
Santa Ana, CA 92705
(714) 836-0351
(ED) (FL) (FP)
CIRCLE 379

ITW Paktron
1205 McConville Rd.
Lynchburg, VA 24502
(804) 239-6941
(FP) (FT) (CP) (CN)
CIRCLE 380

Illinois Capacitor Inc.
3757 W. Touhy Ave.
Lincolnwood, IL 60645
(708) 675-1760
(CD) (EA) (FL) (FP) (FY)
CIRCLE 381

Iskra Electronics Inc.
222 Sherwood Ave.
Farmingdale, NY 11735
(800) 862-2101
(FL) (FP) (FY) (FT)
CIRCLE 382

Johanson Dielectrics Inc.
Box 6456
Burbank, CA 91510
(818) 848-4465
(CD) (CM) (OP)
CIRCLE 383

Johanson Mfg. Corp.
400 Rockaway Valley Rd.
Boonton, NJ 07005
(201) 334-2676
(AI) (CD)
CIRCLE 384

KCK America Inc.
A Mitsubishi Co.
930 Remington Rd.
Schaumburg, IL 60173-4516
(312) 884-8688
(CD) (CM) (EA) (ED) (FL) (FP)
(FY) (FT) (CN) (OP)
CIRCLE 385

KEMET Electronics Corp.
Box 5928
Greenville, SC 29606
(803) 963-6621
(CM) (EA) (FL) (CP)
CIRCLE 386

KOA Speer Electronics Inc.
Box 547
Bradford, PA 16701
(814) 362-5536
(ED)
CIRCLE 387

Mallory Capacitor Co.
4760 Kentucky Ave.
Indianapolis, IN 46291
(317) 856-2430
(CD) (CM) (EA) (ED) (EW)
(PF) (FY) (FT) (CP)
CIRCLE 388

Marcon America Corp.
Toshiba Group
998 Forest Edge Dr.
Vernon Hills, IL 60061
(708) 913-9980
(CM) (EA) (ED) (EW) (FP)
(FY) (CP) (CN)
CIRCLE 389

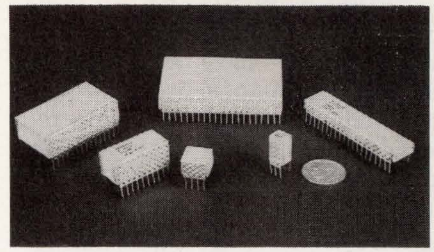
(continued on p. 134)

KEY

Capacitors

(AI)	Air
(CD)	Ceramic/disk
(CM)	Ceramic/multilayer
(EA)	Electrolytic/aluminum
(ED)	Electrolytic/tantalum dry slug
(EW)	Electrolytic/tantalum wet
(FL)	Film/polycarbonate
(FP)	Film/polyester
(FY)	Film/polypropylene
(FT)	Film/polystyrene
(FF)	Film/polysulfone
(CG)	Glass
(MI)	Mica
(TE)	Teflon
(VA)	Vacuum
(CP)	Chip
(CN)	Capacitor networks
(CR)	Ceramics

▼ MILITARY CAPACITORS FEATURE LOW ESR/ESL



Used for switchmode power supplies, the KMP multi-pack capacitors offer the low ESR and ESL values necessary for output filtering of high-speed switchers. They are approved to DESC drawings 87106 and 88011, are built with a full-height lead frame, and use M123-qualified dielectrics. Fabricated in a cleanroom multilayer-ceramic chip-fabrication facility, the capacitors employ solderless construction (cofired technology), undergo statistical process control, and the chips are parametrically screened and are burned in. Extra high-reliabilty processing and screening is available as is M123 screening.

Kemet Electronics Corp.
Box 5928
Greenville, SC 29606
(803) 963-6608
▶ CIRCLE 496

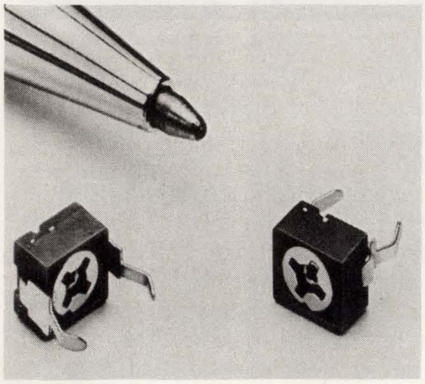
▼ METAL-FILM CAPACITORS SERVE POWER SYSTEMS

A line of metallized-polypropylene capacitors is qualified to MIL-C-84321/2, failure rate S for switchmode power supplies. The C15 series of hermetically sealed devlces covers the range of 0.056 μF to 20 μF with voltage ratings of 60, 120, and 240 V rms. Special values are also available on request. The ac ratings are specified for frequencies of 400 to 100 Hz within a temperature range of –55 to 105°C. All capacitors are burned in with rated currents at 85°C for 24 hrs. A typical specification for a 20-μF, 100-V dc capacitor is 60 V rms at 400 Hz, 15 A at 25°C. Maximum ESR at 100 kHz is a very low-loss 9 mΩ. Delivery of small quantities is from stock.

Component Research Co.
1655 26th St.
Santa Monica, CA 90404
(213) 829-3615
▶ CIRCLE 497

▼ TRIMMER CAPACITORS SPORT NEW STYLES

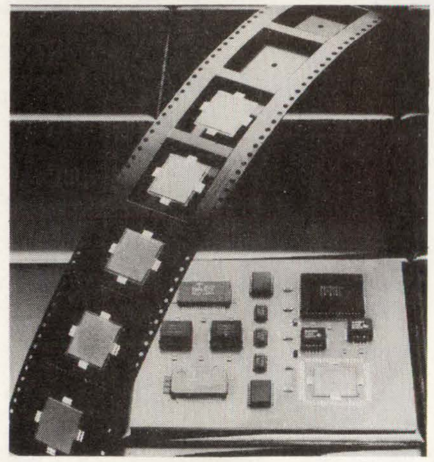
Two new configurations—top and bottom tuning—have been added to the GKG series of 4-by-4.5-mm ceramic trimmer capacitors. Both reverse-leaded types have snap-in spring leads on 5-mm (0.197-in.) mounting-hole centers. The bottom-



tuning models are designated GKGXXX72 when supplied with a membrane seal for the adjust cavity and GKGXXX22 when left unsealed. The top-tuned models are named GKGXXX74 when sealed and GKGXXX24 in unsealed versions. Their molded-plastic housings are color-coded to indicate each model's capacitance range. Seven capacitance ranges in each series go from 1.7 to 3 pF to 15 to 50 pF. All models operate from –25 to 85°C and have a voltage rating of 100 V dc. Top-tuning models are available in magazine packs for auto insertion.

Sprague-Goodman Electronics
134 Fulton Ave.
Garden City Park, NY 11040
(516) 746-1385
▶CIRCLE 498

▼ SURFACE-MOUNTED CAPS FIT UNDER PLCCs



With its very low profile of 0.027 in., Rogers' Micro/Q 3500SM decoupling capacitor fits underneath 68-pin, 84-pin, and larger plastic leaded chip carriers. The capacitors don't develop microscopic cracks during soldering as do multilayer ceramic chips, and have very low equivalent series inductance of 1.6 nH. Two dielectrics are available: the Z5V dielectric offers capacitances of 0.10 and 0.22 μF, while the X7R dielectric offers a value of 0.075 μF. The capacitors come on 32-mm-wide tape at a 28-mm pitch. Pricing is $.83 each in lots of 10,000. Delivery is in six to eight weeks after receipt of order. Samples are available now.

Rogers Corp.
Circuit Components Div.
2400 S. Roosevelt St.
Tempe, AZ 85282
(602) 967-0624
▶CIRCLE 499

CAPACITOR MANUFACTURERS

Mini-Systems Inc.
Thick/Thin-Film Div.
20 David Rd.
North Attleboro, MA 02760
(508) 695-0203
(CP)
CIRCLE 390

Murata Erie
North America Inc.
2200 Lake Park Dr.
Smyrna, GA 30080
(404) 436-1300
(AI) (CD) (CM) (VA) (CN) (OP)
CIRCLE 391

NEC Electronics Inc.
401 Ellis St., Box 7241
Mountain View, CA 94039
(415) 960-6000
(CM) (ED) (EW) (CP)
CIRCLE 392

NIC Component Corp.
6000 New Horizons Blvd.
North Amityville, NY 11701
(516) 226-7500
(CD) (CM) (EA) (ED)
CIRCLE 393

NTE Electronics Inc.
44 Farrand St.
Bloomfield, NJ 07003
(201) 748-5089
(CD) (EA) (ED)
CIRCLE 394

Nichicon (America) Corp.
927 E. State Pkwy.
Schaumburg, IL 60173
(312) 843-7500
(EA) (FP) (FY)
CIRCLE 395

Noble U.S.A. Inc.
5450 Meadowbrook Ind. Ct.
Rolling Meadows, IL 60008
(708) 364-6038
(FY) (FT)
CIRCLE 396

Nytronics Inc.
700 Orange St.
Darlington, SC 29532
(803) 393-5421
(FL) (FP) (FY) (FT)
CIRCLE 397

Philips Components
Discrete Products Div.
2001 W. Blue Heron Blvd.
Riviera Beach, FL 33404
(407) 881-3308
(CM) (CP)
CIRCLE 398

Piher International Corp.
903 Feehanville Dr.
Mount Prospect, IL 60056
(708) 390-6680
(CM)
CIRCLE 399

Robert G. Allen Co.
7267 Coldwater Canyon
North Hollywood, CA 91605
(818) 765-8300
(AI) (CD) (CM) (EA) (ED) (EW) (FL) (FP) (FY) (FT) (FF) (CG) (MI) (TE) (VA) (CP) (CN)
CIRCLE 400

Roederstein Electronics Inc.
Box 5588
Statesville, NC 28677
(704) 872-8101
CIRCLE 401

Rogers Corp.
Circuit Components Div.
2400 S. Roosevelt St.
Tempe, AZ 85282
(602) 967-0624
(CD) (CM)
CIRCLE 402

Seacor Inc.
Box 541, 123 Woodland Ave.
Westwood, NJ 07675
(201) 666-5600
(CM) (FL) (FP) (FY) (FT) (CN)
CIRCLE 403

Shokai Far East Ltd.
280 N. Central Ave.
Hartsdale, NY 10530
(914) 681-0700
(CD) (EA) (FL) (FP) (FY) (FT) (FF)
CIRCLE 404

Siemens Components Inc.
186 Wood Ave. South
Iselin, NJ 08830
(201) 906-4376
(FL) (FP) (FY) (CP)
CIRCLE 405

Spectrum Control Inc.
2185 W. Eighth St.
Erie, PA 16505
(814) 455-0966
(CD) (CM) (CP) (CN)
CIRCLE 406

Sprague Electric Co.
Aluminum Capacitor Div.
Box 9102
Mansfield, MA 02048
(800) 777-7575
(CD) (CM) (EA) (ED) (EW) (FL) (FP) (CN) (CP)
CIRCLE 407

Sprague-Goodman
Electronics
134 Fulton Ave.
Garden City Park, NY 11040
(516) 746-1385
(AI) (FL) (FY) (CG) (MI) (TE)
CIRCLE 408

TDK Corporation
of America
1600 Feehanville Dr.
Mount Prospect, IL 60056
(708) 803-6100
(CD) (CM) (CP) (CN)
CIRCLE 409

Taiyo Yuden (USA), Inc.
714 W. Algonquin Rd.
Arlington Heights, IL 60005
(708) 364-6104
(CD) (CM) (CP) (CN)
CIRCLE 410

Thomson Passive
Components Corp.
Box 4051, 6203 Variel Ave.
Woodland Hills, CA 91367
(818) 887-1010
(CD) (CM) (ED) (FP) (FY) (FT) (CN) (CP)
CIRCLE 411

United Chemi-Con Inc.
9801 W. Higgins Rd.
Rosemont, IL 60018
(312) 696-2000
(EA) (CP)
CIRCLE 412

Voltronics Corp.
Box 476
East Hanover, NJ 07936
(201) 887-1517
(AI) (CG) (TE)
CIRCLE 413

World Products Inc.
19654 8th St. East
Sonoma, CA 95476
(707) 996-5201
(FP)

For codes, see pg. 133

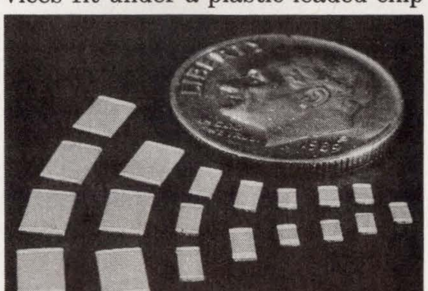
▼ SMT TRIMMER CAPS HANDLE OVER 5 GHZ

Surface-mounted trimmer capacitors come in three choices of dielectrics: sapphire, usable to over 5 GHz in 1.1-, 2.5-, 4.5-, and 8-pF values; air, usable to over 1.2 GHz in 10- and 14-pF values; and glass, usable to over 200 MHz in many values to 60 pF. All versions are sealed with O rings to meet stringent washing requirements. They have nonrotating pistons that provide linear tuning, long life, positive stops, and high Q. The capacitors are modified versions of a proven MIL-C-14409 design.

Voltronics Corp.
Box 476
East Hanover, NJ 07936
(201) 887-1517
▶ CIRCLE 637

▼ MULTILAYER CAPACITORS MOUNT LOW ON BOARDS

A line of multilayer ceramic capacitors was developed for applications that call for very thin, surface-mounted capacitors. With their maximum thickness of 0.020 in., the devices fit under a plastic leaded chip carrier. They also can be used on multichip modules. Four EIA sizes are available: 1206, 1210, and 1812. Values range from 0.01 to 0.3 μF. Typical pricing is $.15 each in OEM lots. Delivery is from stock to eight weeks.



Rogers Corp.
Circuit Components Div.
2400 S. Roosevelt St.
Tempe, AZ 85282
(602) 967-0624
▶ CIRCLE 638

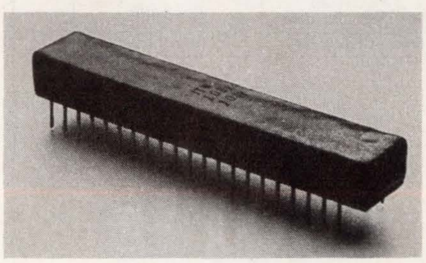
▼ METALLIZED CAPS SUIT PULSE CIRCUITS

Two non-inductive metallized-film capacitors feature high reliability and a self-healing nature. The radial types 2114 and 914 offer pulse properties, low losses, and low ESR. Type 2114 is a metallized polypropylene device that ranges from 0.01 to 2.2 μF with tolerances of ± 5, ± 10, and $\pm 20\%$. Standard voltages are 250,

400, and 630 V dc. The metallized polyester type 914 ranges in value from 0.01 to 6.8 μF and adds a $\pm 2\%$ version. In lots of 1000, the 2114 starts at $.08 each and the 914 at $.07 each. Delivery for both is from stock to eight weeks.

Tecate Industries Inc.
Box 711509
Santee, CA 92072
(619) 448-4811
▶ CIRCLE 648

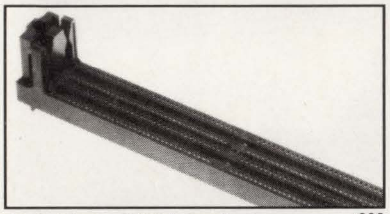
▼ HIGH-CURRENT CAPACITORS SUIT POWER CONVERTERS



Applications for ITW Paktron's type CS Capstick capacitors can be found in the input and output filter circuits of high-frequency switchmode power supplies and dc-dc converters. They're useful where conventional capacitors are too high in impedance because of dielectric losses or where they display high inductive reactance because of their size and shape. The high-current, high-capacitance devices are multilayer, metalized polyester-film types with multiple leads on a 0.1-in. grid. Their dissipation factor is stable in low-frequency applications. Standard capacitance values are available up to 25 μF at 50 V dc with 100- and 250-V dc ratings depending on value. In lots of 100, a 25-μF, 50-V dc capacitor goes for $.60. Delivery is in five to six weeks after receipt of order.

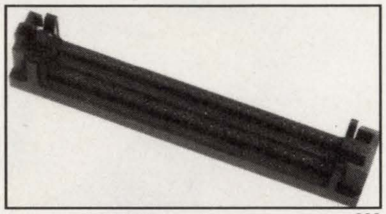
ITW Paktron
1205 McConville Rd.
Lynchburg, VA 24502
(804) 239-6941.
▶ CIRCLE 649

You need 'em. We got 'em. Let's talk sockets.



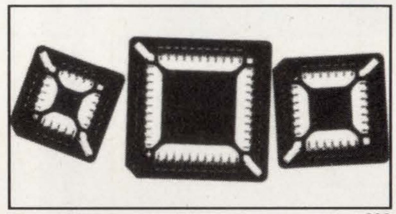
.050 Pitch SIMM Sockets 000

- Accepts SIMM modules with .010" thickness range
- IR compatible high temp insulator
- Audible "snap in" feature
- User friendly insertion/withdrawal



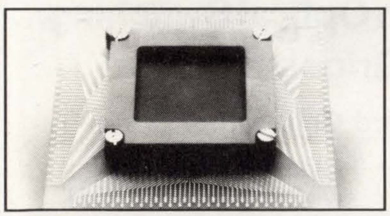
Rugged SIMM Sockets 000

- For larger, heavier SIMM's
- 100 cycle minimum durability
- Severe shock and vibration resistant
- Design eliminates latch breakage



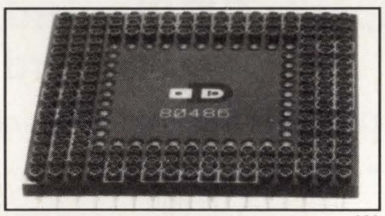
Low Profile SMT PLCC 000

- Easy visual inspection
- Footprint same as device
- Tape and reel packaging
- Shock and vibration resistant



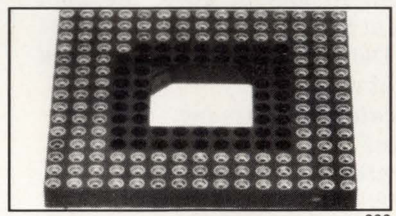
Solderless SMT .025" PQFP Socket 000

- Made for bumpered PQFP's
- Designed for high speed applications
- Footprint matches device
- Eliminates typical socket inductance



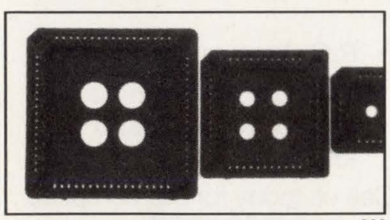
Customized PGA Sockets 000

- High density .050" interstitial
- For high speed microprocessors
- Reduced crosstalk
- Integral decoupling capacitor



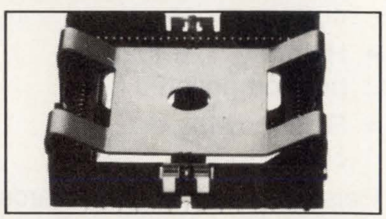
Ultra Low Force PGA Sockets 000

Contact Type	Insertion/Withdrawal Total (Based on 68 Pins)
Robinson Nugent Ultra-Low	**7.5/5.5 lb**
2-finger Tulip (Stamped & Formed)	10.3/6.7 lb
6-finger Staggered	14.8/8.7 lb



High Temp .050" PLCC Sockets 000

- Shock and vibration resistant
- 20 through 100 positions
- Closed bottom design
- Extraction tool common for all sizes



Motorola SLAM PAK .050" Socket 000

- Custom design DSP socket
- Shock and vibration resistant
- Anti-wicking bottom cover

The Call is on Us.

800-338-8152 000

Robinson Nugent

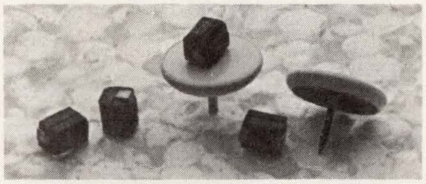
P.O. Box 1208 New Albany, IN 47150-1208
800/338-8152 • FAX 812/945-0804

6 Rue St. Georges, CH 2800 Delémont
(41) 66-22-9822 • FAX (41) 66-22-9813

CIRCLE 164

▼ MULTILAYER CHIP FORMS INDUCTOR

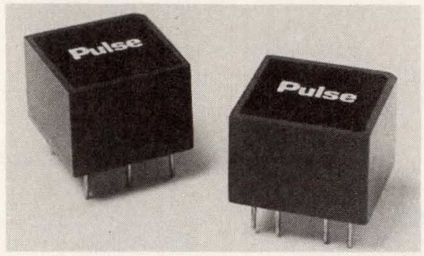
Unlike conventional coils, the LMCL multilayer chip inductor is built up of alternate layers of ferrite and conductor paste that form a perfectly closed magnetic circuit. They come in three of the smallest possible sizes for high-density applications and



cover a range of 0.047 to 220 μH. Highly heat resistant, the inductors withstand flow and reflow soldering and present no shelf-life problems over long years of storage. They are suitable for use in camcorders, disk drives, automobiles, and more.

Inductor Supply Inc.
1849 W. Sequoia Ave.
Orange, CA 92668
(800) 854-1881
▶ **CIRCLE 500**

▼ COMMON-MODE CHOKES WORK IN ISDN CIRCUITS

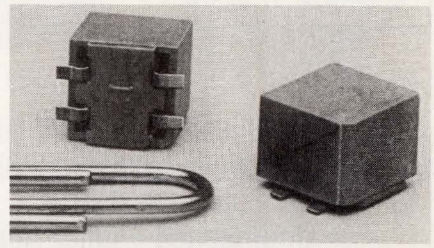


Specifically designed for ISDN four-wire S-interface circuits is a line of common-mode filter chokes. The chokes can be used in the transmit and receive lines and reduce common-mode noise. Two models are available with inductances of 1 and 6 mH and common-mode impedances up to 5 kΩ and 20 kΩ at 1 MHz. The packages are board-mountable and are a maximum of 0.4 in. tall.

Pulse Engineering Inc.
Telecom Group
Box 12235
San Diego, CA 92112
(619) 268-2400
▶ **CIRCLE 501**

▼ SMD INDUCTORS SPORT WIDE RANGE OF VALUES

Believed to be the first line of surface-mounted inductors to offer high Q and dc-resistance values, Dale's IS-22 inductors come in a wide range of standard inductance values. Models are available with values of 200, 1000, 10,000, and 25,000 μH. Minimum Q values range from 50 to 80 and dc-resistance values range from



0.2 to 8 Ω. Standard tolerance is ±40% over a temperature range of –20 to +105°C.

Dale Electronics Inc.
East Hwy. 50
Yankton, SD 57078
(605) 665-9301.
▶ **CIRCLE 502**

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4000 Bridge St.
Drexel Hill, PA 19026
(800) 331-8838
(PF)
CIRCLE 405

Allen Avionics Inc.
224 E. Second St.
Mineola, NY 11501
(516) 248-8080
(PL) (PF)
CIRCLE 406

American Precision Industries Delevan Div.
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East Aurora, NY 14052
(716) 652-3600
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(203) 242-0761
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(AF) (IF) (RF)
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Cary, IL 60013
(708) 639-2361
(IF) (RF) (SU) (PF)
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(AF) (IF) (RF) (SU)
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Milwaukee, WI 53219
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(PF)
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(402) 564-3131
(AF) (IF) (RF) (SU)
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Clifton, NJ 07013
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(PL)
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Datatronics Inc.
28151 Hwy. 74
Romoland, CA 92380
(714) 928-7700
(PL)
CIRCLE 415

ESC Electronics Corp.
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Palisades Park, NJ 07650
(800) 631-0853
(AF) (RF) (SU)
CIRCLE 416

Ecliptek Corp.
18430 Bandolier Circle
Fountain Valley, CA 92708
(714) 963-4009
(AF) (IF) (RF) (SU)
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Box 8121
San Luis Obispo, CA 93403
(805) 544-3800
(PD)
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FDK America Inc. Fuji Electrochemical Co.
17326 Edwards Rd., Ste. A130
Cerritos, CA 90701
(213) 404-1770
(RF)
CIRCLE 419

Ferroxcube Div. of Amperex Electronics
5083 Kings Hwy.
Saugerties, NY 12477
(914) 246-2811
(IF) (RF)
CIRCLE 420

Frequency Devices Inc.
25 Locust St.
Haverhill, MA 01830
(617) 374-0761
(PF)
CIRCLE 421

General Instruments Corp. Optoelectronics Div.
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Palo Alto, CA 94304
(415) 493-0400
(PF)
CIRCLE 422

Gowanda Electronics Corp.
1 Industrial Pl.
Gowanda, NY 14070
(716) 532-2234
(IF) (RF) (SU) (PO)
CIRCLE 423

ICS Manufacturing Inc.
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Anaheim, CA 92802
(800) 642-2645
(AF) (IF) (RF) (SU)
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Rahway, NJ 07065
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(PF)
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Mini-Circuits
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(718) 934-4500
(PF)
CIRCLE 428

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Smyrna, GA 30080
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(IF) (RF) (SU)
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700 Orange St.
Darlington, SC 29532
(803) 393-5421
(RF) (PL)
CIRCLE 430

Opt Industries Inc.
300 Red School Lane
Phillipsburg, NJ 08865
(201) 454-2600
(AF) (IF) (RF)
CIRCLE 431

(continued on p. 142)

KEY

Inductors, coils, and chokes
(AF) Audio frequency
(IF) Intermediate frequency
(RF) Radio frequency
(SU) Surface-mounted
(PL) Passive delay lines
(PF) Passive filters

MANUFACTURERS LISTING

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PCA Electronics Inc.
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Sepulveda, CA 91343
(818) 892-0761
(RF)
CIRCLE 432

Pacific Coil Co.
Div. of Inductor Supply Inc.
430 E. 19th St.
Bakersfield, CA 93305-5495
(800) 332-2645
(AF) (IF) (RF) (SU)
CIRCLE 433

Polara Engineering Inc.
4115 Artesia Ave.
Fullerton, CA 92633
(714) 521-0900
(AF) (IF) (RF) (SU)
CIRCLE 434

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3521 N. Chapel Hill Rd.
Mc Henry, IL 60050
(815) 385-2700
(AF) (RF)
CIRCLE 435

Pulse Engineering
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San Diego, CA 92112
(619) 268-2544
(IF)
CIRCLE 436

RCD Components Inc.
520 E. Industrial Park Dr.
Manchester, NH 03103
(603) 669-0054
(RF) (SU)
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East Deer Park, NY 11729
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Robert G. Allen Co.
7267 Coldwater Canyon
North Hollywood, CA 91605
(818) 765-8300
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4010 Transport
at San Antonio
Palo Alto, CA 94303
(415) 856-6900
(SU)
CIRCLE 440

Schaffner EMC Inc.
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Union, NJ 07083
(201) 851-0644
(PF)
CIRCLE 441

Shokai Far East Ltd.
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Hartsdale, NY 10530
(914) 681-0700
(IF) (RF)
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Sprague Electric Co.
Aluminum Capacitor Div.
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Mansfield, MA 02048
(800) 777-7575
(RF) (SU)
CIRCLE 443

Sprague-Goodman Electronics
134 Fulton Ave.
Garden City Park, NY 11040
(516) 746-1385
(RF) (SU)
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(814) 355-8004
(SU)
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Mount Prospect, IL 60056
(708) 803-6100
(SU) (PL) (PF)
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Arlington Heights, IL 60005
(708) 364-6104
(AF) (IF) (RF) (SU) (PF)
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Thermometrics Inc.
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Edison, NJ 08817
(201) 287-2870
(SU)
CIRCLE 448

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Mount Prospect, IL 60056
(312) 297-0070
(AF) (IF) (RF) (SU)
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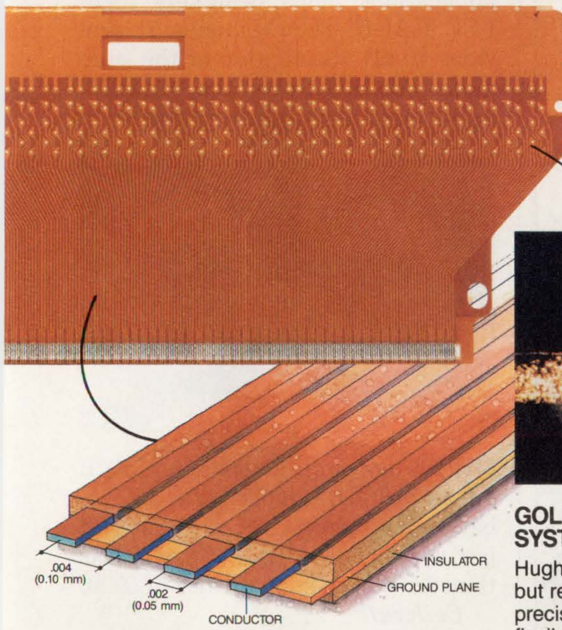
19654 8th St. East
Sonoma, CA 95476
(707) 996-5201
(RF)
CIRCLE 450

KEY

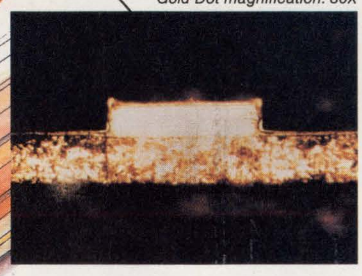
Inductors, coils, and chokes
(AF) Audio frequency
(IF) Intermediate frequency
(RF) Radio frequency
(SU) Surface-mounted
(PL) Passive delay lines
(PF) Passive filters

When It Comes To High-Speed, State-Of-The-Art Interconnection Technology, No One Can Touch Us.

HIGH SPEED FLEXIBLE CIRCUITS WITH GOLD·DOT INTERCONNECTIONS



Gold·Dot magnification: 80X



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Solving high density transmission problems is our business. Are high data clock rates and propagation delay limiting your system performance? Your solution lies in our ability to produce and test controlled impedance flexible circuits in line widths and spacing of .002.

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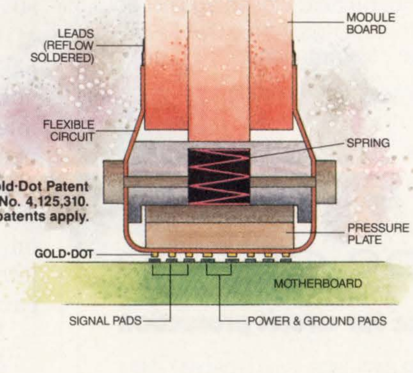
Hughes pioneered Gold·Dot.* Simple, but revolutionary, Gold·Dot is a precision gold bump, integral with a flexible circuit, that mates with a pad on a PC board or another flexible circuit. Offering unparalleled size, weight, and reliability advantages, Gold·Dot answers high performance electronics needs that exceed the limitations of the pin and socket connector.

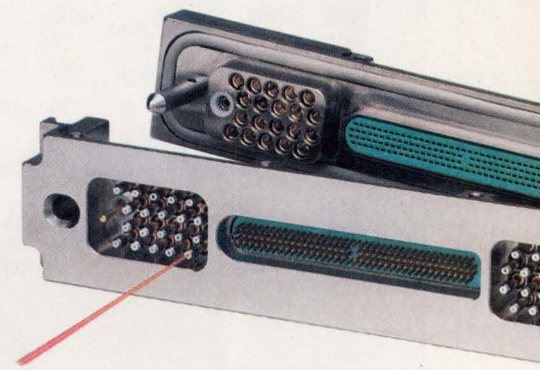
Gold·Dot, our solution for tomorrow's board-to-board, or multichip module-to-board interconnections, today!

TYPICAL APPLICATION

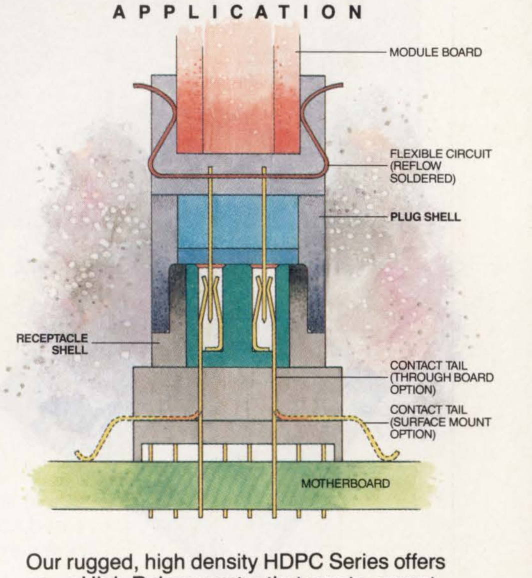


*Gold·Dot Patent No. 4,125,310. Other patents apply.

HIGH DENSITY PRINTED CIRCUIT CONNECTORS WITH DIGITAL, POWER AND FIBER OPTIC CONTACTS



APPLICATION



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Fiber Optics: Jack Maranto (714) 660-5759
In Europe: Hugh McInally (901144) 592-754311

Hughes Aircraft Company
Connecting Devices Division
17150 Von Karman Avenue
Irvine, California 92714

HUGHES
Subsidiary of GM Hughes Electronics

CIRCLE 124

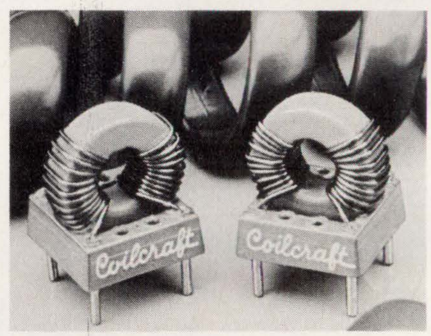
▼ ANALOG DELAY LINE IS PROGRAMMABLE

Housed in a 14-pin DIP, the DIP series of programmable analog delay lines (PADL) is of hybrid construction using both IC and discrete-component techniques. The MTBF of these units is over 1.6 million hours as calculated by MIL-HDBK-217 for a 50°C ground-fixed environment. The delay lines are digitally programmable by TTL signals from remote switch setting or by a computer in eight steps. Analog input signals are specified to be between –5 and 5 V at and input impedance is 100 Ω ±10 Ω. Supply voltage is nominally 5 V at less than 1 mA. Typical set-up time is 24 ns. The device is available in 10 models in maximum delays from 4.5 ns to 36 ns. The 36-ns PADL offers a maximum deviation of ±1 ns, a delay change per step of 5 ±0.5 ns, and 3-dB bandwidth of 10 MHz.

Engineered Components Co.
3580 Sacramento Dr., Box 8121
San Luis Obispo, CA 93403-8121
(805) 544-3800
▶ **CIRCLE 650**

▼ FILTER QUIETS TIP-AND-RING CIRCUITS

The TRF-4000 filter for tip-and-ring applications helps designers meet FCC Part 68 requirements. It provides 20-dB attenuation of the common-mode noise over the 30-to-250-MHz range, and attenuates 15 dB out to 300 MHz. Isolation is 1500 V between windings and dc resistance per winding is 65 mΩ. Cost is less than $2.00 each in quantities of 5000.



Coilcraft
1102 Silver Lake Rd.
Cary, IL 60013
(708) 639-6400
▶ **CIRCLE 651**

▼ THREE-PHASE EMI FILTER OPERATES TO 400 HZ

The FN 356 series of three-phase EMI filters is available in current ratings from 16 to 50 A at 45°C. The chassis-mounted filters provide over 80 dB of differential attenuation at 1 MHz. The 16-A model measures only 5.9 by 2.0 by 4.0 in. The operating-voltage rating is 250 V from phase line to neutral and 440 V between phase lines at a frequency of dc to 400 Hz. Solder-lug connections serve the 16-A size and UNC 8-32 studs are on the 25-, 36-, and 50-A models. In lots of 25, the 16-A unit costs $109.59 each; delivery is in four to ten weeks.

Schaffner EMC Inc.
825 Lehigh Ave.
Union, NJ 07083
(800) 367-5566
▶ **CIRCLE 652**

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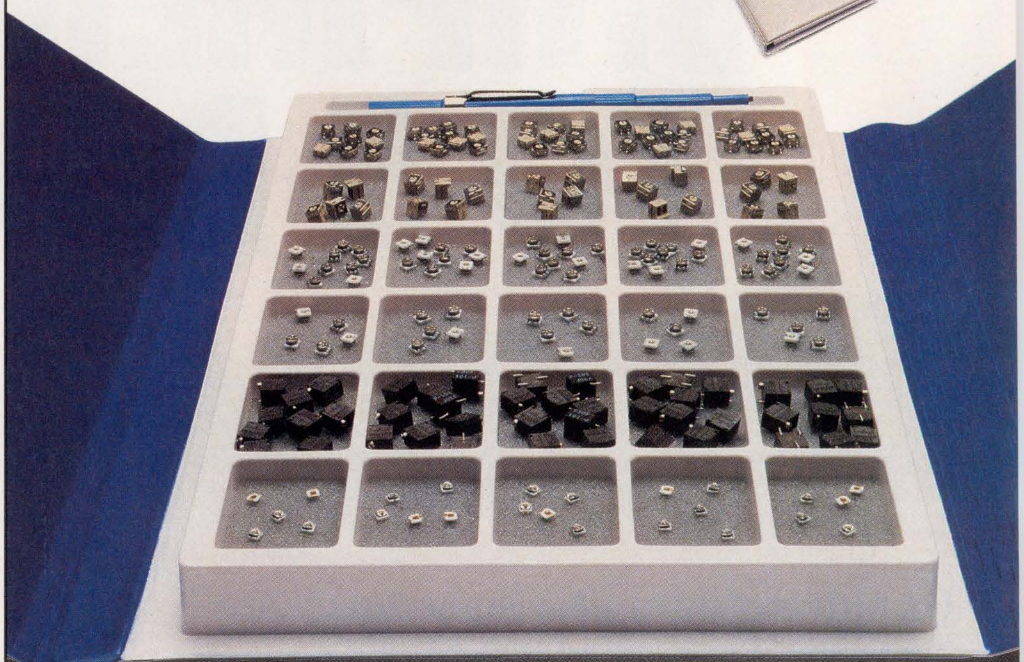

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Sarasota, FL 34243
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(MC) (QC) (CO)
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Sandwich, IL 60548
(815) 786-8411
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Connor-Winfield Corp.
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Aurora, IL 60505-1335
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(CO) (SO)
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(CO) (SO)
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(800) 348-0028
(CF) (TC) (VC)
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(CK)
CIRCLE 461

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Frequency Electronics Inc.
55 Charles Lindbergh Blvd.
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Elec. Components
and Materials
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Williamsport, PA 17701
(717) 326-6591
(QC)
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ITT Components
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Santa Ana, CA 92705
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(MC) (QC) (CO)
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KCK America Inc.
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Schaumburg, IL 60173-4516
(312) 884-8688
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Yankton, SD 57078
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(SC)
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(800) 331-1236
(CO) (VC) (SO)
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Valpey-Fisher
75 South St.
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(717) 486-3411
(QC) (SC) (CL) (CO)
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New York, NY 10010
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(MC) (QC) (CO)
CIRCLE 472

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Smyrna, GA 30080
(404) 436-1300
(CL) (CO)
CIRCLE 473

NDK America Inc.
20300 Stevens Creek Blvd.
Cupertino, CA 95014
(408) 255-0831
(MC) (QC) (SC) (CO) (TC) (VC)
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NEL Frequency Controls
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Burlington, WI 53105
(414) 763-3591
(MC) (QC) (SC) (CL) (CO) (TC) (VC) (CK) (SO)
CIRCLE 475

NTE Electronics Inc.
44 Farrand St.
Bloomfield, NJ 07003
(201) 748-5089
(MC) (QC)
CIRCLE 476

Piezo Crystal Co.
100 K St., Box 619
Carlisle, PA 17013
(717) 249-2151
(MC) (QC) (SC) (CO) (TC) (VC)
CIRCLE 477

Piezo Technology Inc.
Box 547859
Orlando, FL 32854
(407) 298-2000
(SC) (CL) (CO) (TC) (VC) (CK) (SO)
CIRCLE 478

Pletronics Inc.
9026 Roosevelt Way N.E.
Seattle, WA 98115
(206) 523-9395
(MC) (QC) (SC) (CO) (CK) (SO)
CIRCLE 479

Q-Tech Corp.
10150 W. Jefferson Blvd.
Culver City, CA 90232-3510
(213) 836-7900
(QC) (SC) (CO) (TC) (VC) (SO)
CIRCLE 480

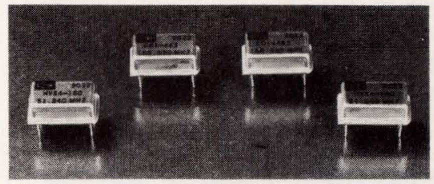
Saronix
4010 Transport
at San Antonio
Palo Alto, CA 94303
(415) 856-6900
(MC) (QC) (SC) (CO)
CIRCLE 481

(continued on p. 148)

For codes, see pg. 148

▼ CRYSTAL OSCILLATORS SERVE FIBER OPTICS

A family of four crystal oscillators for use with fiber-optic-transmission lines deliver ±20 ppm accuracy over operating temperature ranges of –40 to 85°C or zero to 70°C. The devices oscillate at 51.840 MHz (HV54/64) or 155.520 MHz (EO1-453/463), and are designed for Sonet STS1 and STS3,

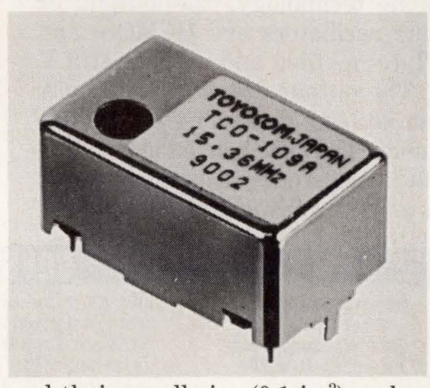


respectively. Prototypes are available in six to eight weeks and cost $87.95 (HV54/64) and $82.70 (EO1-456/463). Both prices are for lots of 10.

The Connor-Winfield Corp.
1865 Selmarten Rd.
Aurora, IL 60505
(708) 851-5040
▶ CIRCLE 502

▼ CRYSTAL OSCILLATORS BOAST HIGH STABILITY

A frequency stability of ±1 ppm from –30 to 80°C is featured in the TCXO digitally compensated crystal oscillators from Toyocom USA Inc. The oscillators require no warmup,

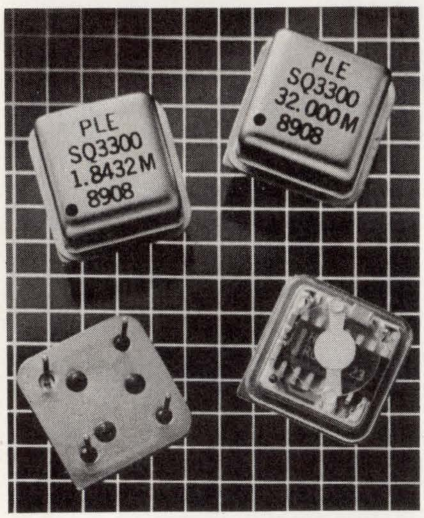


and their small size (0.1 in.^{3}) makes them well suited for fixed or portable applications. The oscillators are available with frequencies of 15.36, 16.8, or 12.8 MHz. Their output is 1 V pk-pk minimum. Pricing, depending on model, ranges from $105 to $117 for samples and from $30 to $35 each in lots of 5000.

Toyocom U.S.A. Inc.
617 E. Golf Rd., Suite 112
Arlington Heights, IL 60005
(800) 869-6266
▶ CIRCLE 503

▼ CLOCK OSCILLATOR REACHES TO 40 MHZ

With output frequencies available from 500 kHz to 40 MHz, Pletronics' three-state, SQ 3300 series clock oscillator includes an enable/disable control input. When in the enable condition, operation is normal. When in the disable condition, the output presents a high impedance and the clock oscillator is ready for connection to alternate circuits or to test signals. The operating temperature range is from zero to 70°C. Frequency stabilities from 0.005 to 0.1% are



available. Built with high-speed CMOS technology, the output of these oscillators are HCMOS- and TTL-compatible and operate at 5 V dc. The output draws 10 to 60 mA with no load, depending on the frequency. They are housed in hermetically sealed, four-pin metal mini-DIP containers. Pricing is $3.40 in quantities of 1000.

Pletronics Inc.
9026 Roosevelt Way N.E.
Seattle, WA 98115
(206) 525-2350
▶ **CIRCLE 504**

▼ TTL-COMPATIBLE CLOCKS IN 26 FREQUENCIES

An off-the-shelf line of TTL-compatible clock oscillators comes in 26 standard frequencies. CTS Corp.'s MXO55L line of oscillators offers frequencies ranging from 2.4576 to 70 MHz. All are capable of driving up to 10 standard TTL loads. With many applications in personal computers, facsimile machines, and telecommunications equipment, the MXO55L oscillators come in an all-metal, hermetically sealed 14-pin DIP. Stability for standard frequencies is ±100 ppm over an operating-temperature range of zero to 70°C. Call for pricing and availability.

CTS Corp.
Frequency Control Div.
400 Reimann Ave.
Sandwich, IL 60548
(815) 786-8411
▶ **CIRCLE 505**

▼ HIGH STABILITY ANCHORS OSCILLATOR

With high stability and low noise, the type CO-705SL2 crystal oscillator provides a noise floor of just –168 dBc/Hz. The oscillator warms up to within 10^{-8} of the output frequency in 4 minutes after turn on. Aging is 5×10^{-10} per day and 10^{-7} per year, and temperature stability is $\pm 10^{-9}$ from zero to 50°C and $\pm 5 \times 10^{-9}$ from –55 to

75°C. Standard output frequencies are 5 MHz and 10 MHz, and any frequency from 4 MHz to 12.5 MHz is available. The standard output is +7 dBm into a 50-Ω load. A +13-dBm or HCMOS/TTL output is optional. The frequency can be adjusted either mechanically or by means of an externally injected voltage. The unit is packaged in a 1.5-by-1.5-by-2-in. case. Delivery is in from 10 to 16 weeks, depending on the frequency requested.

Vectron Laboratories Inc.
166 Glover Ave.
Norwalk, CT 06850
(203) 853-4433
▶ **CIRCLE 506**

CRYSTAL AND OSCILLATOR MANUFACTURERS

Seiko Instruments U.S.A. Fiber Optic Comp. Div.
2990 W. Lomita Blvd.
Torrance, CA 90505
(213) 517-7841
(QC) (CO) (TC)
CIRCLE 482

Shokai Far East Ltd.
280 N. Central Ave.
Hartsdale, NY 10530
(914) 681-0700
(MC) (QC) (SC) (CL)
CIRCLE 483

Spectrum Technology Inc.
Box 948
Goleta, CA 93116
(805) 964-7791
(QC) (SC) (CO) (TC) (VC)
CIRCLE 484

Standard Crystal Corp.
9940 E. Baldwin Pl.
El Monte, CA 91731
(818) 443-2121
(MC) (QC) (SC) (CO) (VC) (CK)
CIRCLE 485

Statek Corp.
512 N. Main St.
Orange, CA 92668
(714) 639-7810
(QC) (SC) (CO) (CK) (SO)
CIRCLE 486

TDK Corporation of America
1600 Feehanville Dr.
Mount Prospect, IL 60056
(708) 803-6100
(VC)
CIRCLE 487

Taiyo Yuden (USA), Inc.
714 W. Algonquin Rd.
Arlington Heights, IL 60005
(708) 364-6104
(VC)
CIRCLE 488

Time & Frequency Ltd.
55 Charles Lindbergh Blvd.
Mitchell Field, NY 11553
(516) 794-4500
(MC) (QC) (CL) (CO) (TC) (VC)
CIRCLE 489

Toyocom U.S.A. Inc.
617 E. Gold Rd., Suite 112
Arlington Heights, IL 60005
(708) 593-8780
(MC) (QC) (SC) (CL) (CO) (TC) (VC) (CK) (SO)
CIRCLE 490

Valpey-Fisher Corp.
75 South St.
Hopkinton, MA 01748
(800) 982-5737
(MC) (QC) (SC) (CO) (TC) (VC) (SO)
CIRCLE 491

Vectron Laboratories Inc.
166 Glover Ave.
Norwalk, CT 06850
(203) 853-4433
(CO) (TC) (VC) (CK) (SO)
CIRCLE 492

KEY

Crystals and oscillators
(MC) Microprocessor crystals
(QC) Quartz crystals
(SC) Surface-mounted crystals
(CL) Crystal filters
(CO) Crystal oscillators
(TC) Temperature-controlled oscillators
(VC) Voltage-controlled oscillators
(CK) Clock oscillators
(SO) Surface-mounted oscillators

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155V
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BUS

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- High density designs to 24 watts/in.^{3}.
- Efficiencies to 80%+.

Mil-Std-1275A

- Extended MTBF to >500,000 hours.
- Low EMI/RFI options available.
- Meets applicable requirements of Mil-E-5400T, Mil-E-16400, Mil-E-4158E and Mil-Std-454J.
- Design and derating to NAVMAT P4855-1.

Mil-Std-704D

- Mil-I-45208A facilities and systems.
- Standard products for custom applications without NRE.
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ARNOLD MAGNETICS

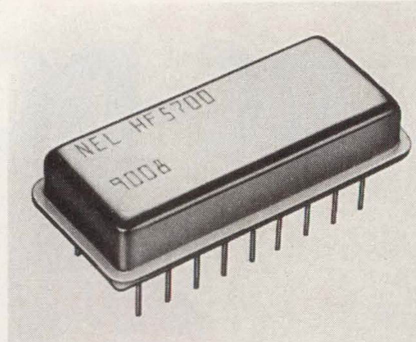
ARNOLD MAGNETICS CORPORATION

4000 Via Pescador, Camarillo, California 93012 • Phone: (805) 484-4221 • FAX: (805) 484-4113

CIRCLE 111

▼ PROGRAMMABLE CLOCK GENERATES UP TO 200 MHZ

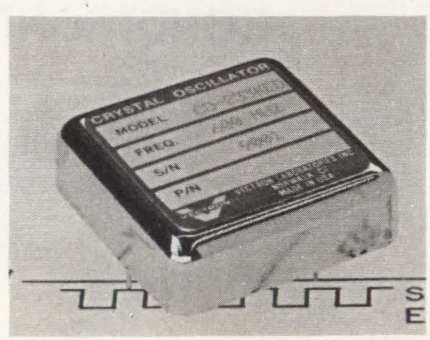
The HF-5700 series programmable clock can generate from 781.25 kHz to 200 MHz for applications where jitter and RFI considerations are critical. The unit incorporates the NSC DP8431 programmable-clock-generator IC with a proprietary ASIC TTL/CMOS clock oscillator, a quartz crystal, and a loop filter in one 18-pin DIP. The outputs from the device provide programmable pixel (PCLK) and system (SCLK, LCLK, and GCLK) clocks as required by the user. These are determined by digital control lines. Special attention is given to construction and layout to minimize jitter and radio-frequency interference. Peak-to-peak phase jitter is less than 1 ns under worst-case conditions. Applications include computer graphics, disk-drive constant-density recording, fiber optics, and local-area-network communications. Production quantities cost about $40 per unit; standard delivery runs from stock to 14 weeks.



NEL Frequency Controls Inc.
357 Beloit St.
Burlington, WI 53105
(414) 763-3591
▶ **CIRCLE 654**

▼ ECL CLOCK OSCILLATOR RUNS UP TO 700 MHZ

Complementary sub-nanosecond ECL-compatible outputs can be specified for any frequency from 150 to 700 MHz in the CO-233KEQ clock oscillator from Vectron Labs. The output is derived from either a 100K ECL or ECLiPS gate, depending on output frequency. The oscillator operates from –4.5 V dc, with –5.2 V dc operation optional. The device is factory-set to within ±0.001% of the specified frequency. A frequency adjustment for setting to within ±0.0001% is also available as an option. Delivery is from five to 10 weeks after receipt of order. Call company for pricing.

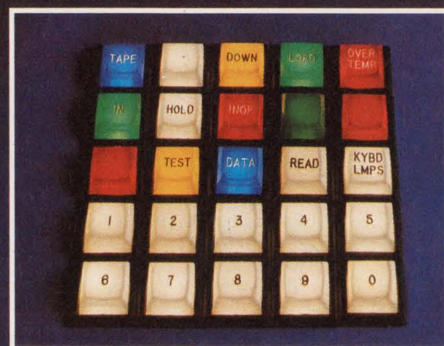


Vectron Laboratories Inc.
166 Glover Ave.
Norwalk, CT 06850
(203) 853-4433
▶ **CIRCLE 655**

Oak puts a leader's performance in lighted products.

As the primary physical link between your product and your customers, lighted pushbutton switches and indicators are components too important to receive anything less than your full attention. That's why it's just as important to look to the leadership of Oak Switch Systems Inc. for lighted products you can depend on.

Oak has been serving the industry with a full range of lighted products for almost 50 years. Whether your application requires military qualified products or the aesthetics of commercial components, we deliver the features, selections and quality that you demand. UL recognized components are also available.



Choose from a wide range of pushbutton switches and indicators to fit your specific requirements. Expect documented performance too. Our Marcoflex® 650 series, for example, provides wiping action, multiple point contact, true snap action, tactile feel, and high contact force—all in a standard 0.625 in. square panel opening. Add to that a demonstrated life of better than 1 million actuations, even in demanding low level switching applications.

Lighted pushbutton switches and indicators, however simple their function, still are critical components. So it makes sense to get them from a leader. Oak's 50 years of performance will make you glad you did.

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CIRCLE 109

OPTOELECTRONICS MANUFACTURERS

3M Fiber Optic Products
10 Industrial Way East
Eatontown, NJ 07724
(201) 544-9119
(FC) (ON) (EM)
CIRCLE 575

AC Interface Inc.
15560 Rockfield Blvd., #1E
Irvine, CA 92718
(714) 472-9524
(FC) (ON) (EM) (IE) (IS) (LL) (LI) (OS) (OI) (PH) (PD) (PT) (PR) (UV)
CIRCLE 576

AEG Corp.
3140 Rt. 22, Box 3800
Somerville, NJ 08876-1269
(201) 231-8300
(EM) (IE) (IS) (LL) (LI) (OS) (OI) (PD) (PT) (RR)
CIRCLE 577

AMP Inc.
Box 3608
Harrisburg, PA 17105-3608
(800) 522-6752
(FC) (ON) (EM) (OS)
CIRCLE 578

AND
W. J. Purdy Co.
770 Airport Blvd.
Burlingame, CA 94010
(415) 347-9916
(LL)
CIRCLE 579

AT&T Microelectronics
555 Union Blvd.
Allentown, PA 18103
(800) 372-2447
(OI) (PT)
CIRCLE 580

Amperex Electronic Co.
Optoelectronics
Business Group
George Washington Hwy.
Smithfield, RI 02917
(401) 232-0500
(LL) (LI) (OI) (PD) (PT) (PR)
CIRCLE 581

Clairex Electronics
560 S. Third Ave.
Mt. Vernon, NY 10550
(914) 664-6602
(IE) (IS) (LL) (LI) (OS) (OI) (PH) (PC) (PD) (PT) (PR) (UV)
CIRCLE 582

Cree Research Inc.
2810 Meridian Pkwy.
Durham, NC 27713
(919) 361-5709
(LL)
CIRCLE 583

D1 Products Inc.
95 E. Main St.
Huntington, NY 11743
(516) 673-6866
(LL) (LI) (OS) (OI)
CIRCLE 584

Data Display Products
445 S. Douglas St.
El Segundo, CA 90245-4630
(213) 640-0442
(LL)
CIRCLE 585

Dialight Corp.
1913 Atlantic Ave.
Manasquan, NJ 08736
(201) 223-9400
(LL)
CIRCLE 586

EG&G Reticon
345 Potrero Ave.
Sunnyvale, CA 94086
(408) 738-4266
(IS) (UV)
CIRCLE 587

EG&G Vactec
10900 Page Blvd.
St. Louis, MO 63132
(314) 423-4900
(IE) (IS) (LI) (OS) (OI) (PH) (PC) (PD) (PT) (PR) (UV)
CIRCLE 588

Epitaxx Inc.
3490 U.S. Route 1
Princeton, NJ 08540
(609) 452-1188
(EM) (IE) (IS) (LL)
CIRCLE 589

Fotec Inc.
529 Main St.
Boston, MA 02129
(617) 241-7810
(FC) (ON)
CIRCLE 590

Gilway Technical Lamp
800 W. Cummings Park
Woburn, MA 01801
(617) 935-4442
(EM) (LL) (LI)
CIRCLE 591

Hewlett-Packard Co.
Components Div.
370 W. Trimble Rd.
San Jose, CA 95131
(408) 435-7400
(FC) (ON) (EM) (LL) (OS) (OI) (PT) (PR)
CIRCLE 592

Hirose Electric (U.S.A.) Inc.
2685-C Park Center Dr.
Simi Valley, CA 93065
(805) 522-7958
(ON)
CIRCLE 593

Hitachi America Ltd.
Semiconductor & IC Div.
2000 Sierra Pt. Pkwy.
Brisbane, CA 94005
(415) 244-7286
(EM) (IE) (LL) (PT)
CIRCLE 594

Honeywell Optoelectronics
830 Arapaho Rd.
Richardson, TX 75081
(214) 470-4271
(EM) (IE) (IS) (LI) (OS) (OI) (PD) (PT) (PR)
CIRCLE 595

IDEA Inc.
1300 Pioneer St., Suite B
Brea, CA 92621
(213) 697-IDEA
(LL) (LI)
CIRCLE 596

Industrial Devices Inc.
260 Railroad Ave.
Hackensack, NJ 07601
(201) 489-8989
(LL)
CIRCLE 597

Industrial Electronic
Engineers
7740 Lemona Ave.
Van Nuys, CA 91405
(818) 787-0311
(LL)
CIRCLE 598

KCK America Inc.
A Mitsubishi Co.
930 Remington Rd.
Schaumburg, IL 60173-4516
(312) 884-8688
(LL)
CIRCLE 599

Ledtronics Inc.
4009 Pacific Coast Hwy.
Torrance, CA 90505
(213) 549-9995
(LL)
CIRCLE 600

Lemo USA
335 Tesconi Circle
Santa Rosa, CA 95401
(707) 578-8811
(ON)
CIRCLE 601

Marktech International Corp.
5 Hemlock St.
Latham, NY 12110
(518) 786-6591
(IE) (LL)
CIRCLE 602

Matec Corp.
Valpey-Fisher
75 South St.
Hopkinton, MA 01748
(508) 435-6831
(FC)
CIRCLE 603

Matec Fiberoptics
56 Hudson St.
Northboro, MA 01532
(508) 393-3753
(FC)
CIRCLE 604

(continued on p. 153)

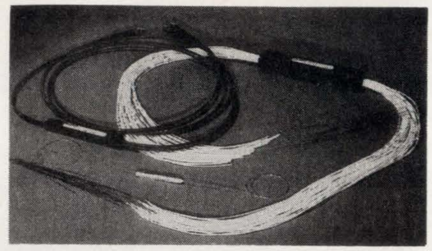
KEY

Optoelectronics

(FC)	Fiber-optic cables
(ON)	Fiber-optic connectors
(EM)	Fiber-optic emitters/ detectors
(IE)	Infrared emitters
(IS)	Infrared sensors
(LL)	LEDs, light-emitting
(LI)	LEDs, IR-emitting
(OS)	Optical switches
(OI)	Optocouplers/isolators
(PH)	Photocells
(PC)	Photoconductive cells
(PD)	Photodarlingtons
(PT)	Photodiodes and arrays
(PR)	Phototransistors
(UV)	UV sensors

▼ FIBER-OPTIC COUPLERS SPLIT OR JOIN PATHS

A family of single- and multi-mode couplers can combine or split light from fiber to fiber to create optical systems that transcend simple point-to-point interconnections. Standard input-output configurations for single-mode couplers are 1-by-2 and 2-by-2 arrangements. Units can be cascaded or combined to form single-mode tree or star couplers in configurations such as 1-by-8 or 8-by-8. Multi-mode couplers come in standard input-output configurations ranging from simple 1-by-2 arrangements to 32-by-32 star couplers. All



couplers are available in light-duty miniaturized, medium, or heavy-duty pigtailed packages. Delivery of single-mode units is in three weeks after receipt of order; multi-mode units are custom designed, which determines price and availability.

AMP Inc.
Box 3608
Harrisburg, PA 17105-3608
(717) 564-0100
▶CIRCLE 507

▼ BRIGHT BLUE LEDs COMPLETE SPECTRUM

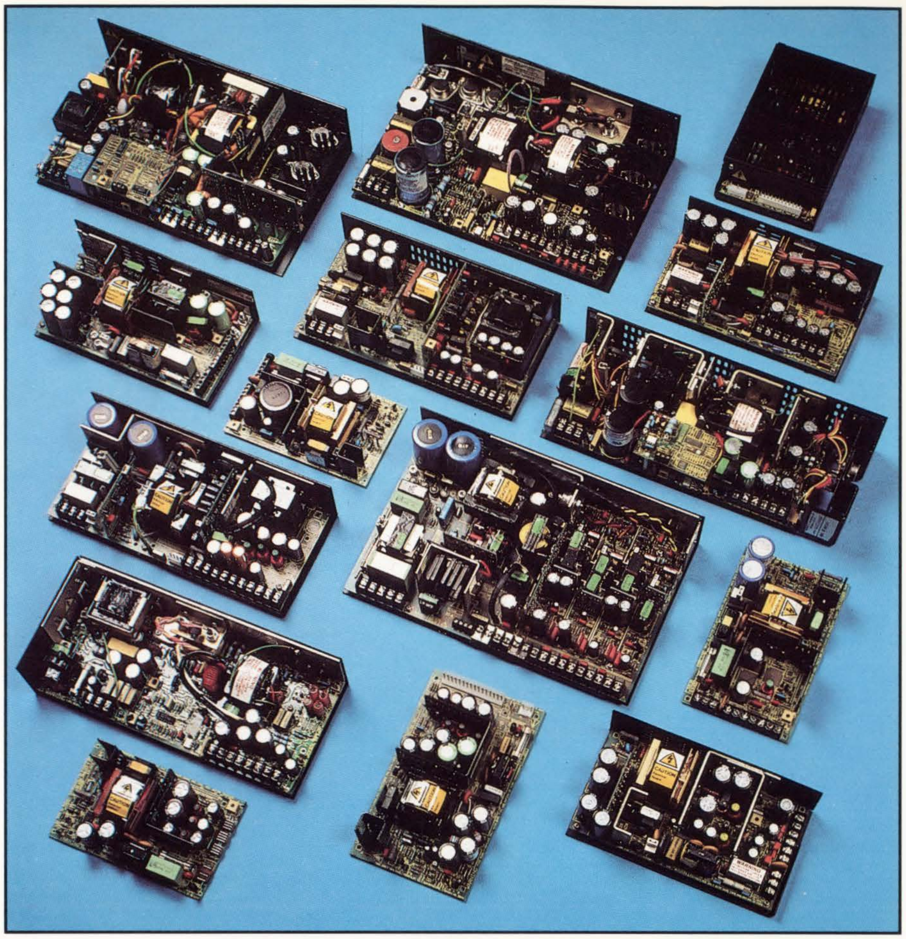
With the availability of bright blue LEDs from Cree Research, designers can now combine blue, red, and green LEDs in a single package to achieve any color light in the visible spectrum, including solid-state white. Fabricated in silicon carbide, the blue chips emit an intense color at a peak wavelength of 470 nm. They generate up to 35 mcd in a T-1-3/4 LED package. Typical optical power output is 8 mW at 20 mA. Pricing for the blue LEDs ranges from $.75 each for volume quantities of unpackaged die to $15 for sample quantities of packaged parts.

Cree Research Inc.
2810 Meridian Pkwy., Suite 176
Durham, N.C. 27713
(919) 361-5709
▶CIRCLE 508

NEW.
Open frame, "N" Range switch mode power supplies from Farnell Advance.

The Farnell "N" Range of open frame, 50 to 500-watt, switch mode power supplies offers electronic designers a wide choice of single and multiple output units, featuring technically superior designs and the highest standards of production quality. Refer to the listing of available standard models and contact Farnell Advance, 32111 Aurora Rd., Solon, OH 44139 for specifications.

PHONE: (216) 349-0755.
FAX: (216) 349-0142.



DVE ® FCC

FARNELL ADVANCE POWER

Output Power	Output 1	Output 2	Output 3	Output 4	Output 5	Package Options	Dimensions including covers	Model No.
50 watts multi output	+5V 6A	+12V 1A	+24V 1A	-5V 1A	-12V 1A	2,3	*a	N50R110
	+5V 6A	+15V 1A	+24V 1A	-5V 1A	-15V 1A	2,3	*a	N50R201
55 watts single output	5V 11A	—	—	—	—	1,3,4	b	NS055005
	12V 4.6A	—	—	—	—	1,3,4	b	NS055012
	15V 3.7A	—	—	—	—	1,3,4	b	NS055015
	24V 2.3A	—	—	—	—	1,3,4	b	NS055024
	30V 1.8A	—	—	—	—	1,3,4	b	NS055030
	48V 1.15A	—	—	—	—	1,3,4	b	NS055048
	56V 1A	—	—	—	—	1,3,4	b	NS055056
55 watts multi output	100V 0.55A	—	—	—	—	1,3,4	b	NS055100
	+5V 3.5A	+12V 3A(S)	-12V 1A(S)‡‡	—	—	1,3,4	b	NA055P300
	+5V 3.5A	+12V 3A(S)	+24V 1A(S)‡‡	—	—	1,3,4	b	NA055P301
	+5V 3.5A	+15V 3A(S)	-15V 1A(S)‡‡	—	—	1,3,4	b	NA055P302
	+5V 6A	+12V 3A(S)	F12V 2A(S)	F24V 1A(S)	—	1,3,4	c	NA055P400
	+5V 6A	+12V 3A(S)	F12V 2A(S)	F5V 1A(S)	—	1,3,4	c	NA055P401
	+5V 6A	+15V 3A(S)	F15V 2A(S)	F24V 1A(S)	—	1,3,4	c	NA055P403
	+5V 6A	+12V 3A(S)	F12V 1A	F12V 1A	—	1,3,4	c	NA055P413
75 watts single output	5V 15A	—	—	—	—	1,3,4	*d	NS075005
	12V 6.25A	—	—	—	—	1,3,4	*d	NS075012
	15V 5A	—	—	—	—	1,3,4	*d	NS075015
	24V 3.2A	—	—	—	—	1,3,4	*d	NS075024
	30V 2.5A	—	—	—	—	1,3,4	*d	NS075030
	48V 1.6A	—	—	—	—	1,3,4	*d	NS075048
75 watts multi output	56V 1.4A	—	—	—	—	1,3,4	*d	NS075056
	+5V 8A	+12V 3A(S)	F12V 2A(S)	—	—	1,3,4	e	NA075P300
	+5V 8A	+12V 3A(S)	F12V 2A(S)	F24V 1A	—	1,3,4	e	NA075P400
	+5V 8A	+12V 3A(S)	F12V 2A(S)	F5V 1A	—	1,3,4	e	NA075P401
	+5V 8A	+12V 3A(S)	+12V 2A(S)‡	-12V 0.5A‡	—	1,3,4	e	NA075P402
	+5V 8A	+15V 3A(S)	F15V 2A(S)	F24V 1A	—	1,3,4	e	NA075P403
	+5V 8A	+12V 3A(S)	-12V 1A‡	-5V 1A‡	—	1,3,4	e	NA075P414
90 watts multi output	+5V 10A	+12V 5A	-12V 2A	-5V 1A	+24V 1A	2,3	*f	N90R109
	+5V 10A	+15V 5A	-15V 2A	-5V 1A	+24V 1A	2,3	*f	N90R132

CIRCLE NO. 150

FARNELL ADVANCE OPEN-FRAME SWITCH MODE POWER SUPPLIES

Output Power	Output 1	Output 2	Output 3	Output 4	Output 5	Package Options	Dimensions including covers	Model No.
110 watts single output	5V 22A or 30A(FC)	—	—	—	—	2,3,4	*g	NS110005
	12V 9.2A or12.5A(FC)	—	—	—	—	2,3,4	*g	NS110012
	15V 7.5A or10A(FC)	—	—	—	—	2,3,4	*g	NS110015
	24V 4.6A or 6.25A(FC)	—	—	—	—	2,3,4	*g	NS110024
	30V 3.7A or 5A(FC)	—	—	—	—	2,3,4	*g	NS110030
	48V 2.3A or 3A(FC)	—	—	—	—	2,3,4	*g	NS110048
	56V 2A or 2.6A(FC)	—	—	—	—	2,3,4	*g	NS110056
110 watts multi output	+5V 12A	+12V 6A(S)	-12V 3A(S)‡‡	—	—	2,3,4	h	NA110P300
	+5V 12A	+15V 6A(S)	-15V 3A(S)‡‡	—	—	2,3,4	h	NA110P302
	+5V 10A	+12V 1.5A(S)‡‡	+12V 3.5A(S)	-12V 0.7A(S)‡‡	—	2,3,4	h	NQ110P400
	+5V 12A	+12V 5A(S)	-12V 2A(S)‡‡	—	+24V 2A(S)‡	2,3,4	*i	NA110P400
	+5V 12A	+12V 5A(S)	-12V 2A(S)‡‡	-5V 1A‡‡	—	2,3,4	*i	NA110P401
	+5V 12A	+12V 5A(S)	+12V 3A(S)‡‡	—	-12V 2A(S)‡	2,3,4	*i	NA110P402
	+5V 12A	+15V 5A(S)	-15V 2A(S)‡‡	—	+24V 2A(S)‡	2,3,4	*i	NA110P403
	+5V 12A	+12V 5A(S)	-12V 2A(S)‡‡	-5V 1A‡‡	+24V 2A(S)‡	2,3,4	*i	NA110P500
	+5V 12A	+12V 5A(S)	-12V 2A(S)‡‡	-5V 1A‡‡	+12V 2A(S)‡	2,3,4	*i	NA110P501
	+5V 12A	+15V 5A(S)	-15V 2A(S)‡‡	-5V 1A‡‡	+24V 2A(S)‡	2,3,4	*i	NA110P503
140 watts single output	5V 28A	—	—	—	—	2,3,4	*g	NS140005
	12V 12A	—	—	—	—	2,3,4	*g	NS140012
	15V 10A	—	—	—	—	2,3,4	*g	NS140015
	24V 6A	—	—	—	—	2,3,4	*g	NS140024
	30V 5A	—	—	—	—	2,3,4	*g	NS140030
	48V 3A	—	—	—	—	2,3,4	*g	NS140048
	56V 2.5A	—	—	—	—	2,3,4	*g	NS140056
140 watts multi output	+5V 17A	+12V 7A(Q)	F12V 3A(Q)	—	—	2,3,4	*j	NA140P300
	+5V 17A	+12V 5A(Q)	F12V 3A(Q)	F24V 3A(Q)	—	2,3,4	*j	NA140P400
	+5V 17A	+12V 5A(Q)	F12V 3A(Q)	—	F5V 1.5A	2,3,4	*j	NA140P401
	+5V 17A	+12V 5A(Q)	F12V 3A(Q)	F12V 1.5A	—	2,3,4	*j	NA140P402
	+5V 17A	+12V 5A(Q)	F12V 3A(Q)	F24V 3A(Q)	F5V 1A	2,3,4	*j	NA140P500
	+5V 17A	+12V 5A(Q)	F12V 3A(Q)	F12V 1.5A	F5V 1A	2,3,4	*j	NA140P501
	+5V 17A	+15V 5A(Q)	F15V 3A(Q)	F24V 3A(Q)	F5V 1A	2,3,4	*j	NA140P503
180 watts multi output and 48 volt D.C. input	+5V 20A	+12V 5A(S)	-12V 5A(S)	+24V 2A(S)	-5V 1A(S)	2,3,4	*k	ND180P500
	+5V 25A	+15V 1A	-15V 1A	—	—	2,3,4	*k	ND180P810
200 watts multi output	+5V 30A	+12V 7A(Q)	F12V 5A(Q)	—	—	2,3,4	*l	NA200P300
	+5V 30A	+12V 7A(Q)	F12V 5A(Q)	F24V 3A(Q)	—	2,3,4	*l	NA200P400
	+5V 30A	+12V 7A(Q)	F12V 5A(Q)	—	F5V 1A	2,3,4	*l	NA200P401
	+5V 30A	+12V 7A(Q)	F12V 5A(Q)	F12V 1.5A	—	2,3,4	*l	NA200P402
	+5V 30A	+12V 7A(Q)	F12V 5A(Q)	F24V 3A(Q)	F5V 1A	2,3,4	*l	NA200P500
	+5V 30A	+12V 7A(Q)	F12V 5A(Q)	F12V 5A(Q)	F5V 1A	2,3,4	*l	NA200P501
	+5V 30A	+12V 7A(Q)	F12V 5A(Q)	F12V 5A(Q)	F5V 5A(Q)	2,3,4	*l	NA200P502
	+5V 30A	+15V 7A(Q)	F15V 5A(Q)	F24V 3A(Q)	F5V 1A	2,3,4	*l	NA200P503
	F5V 30A	F12V 5A	F12V 5A	—	—	2,3,4	*l	NA200R300
	F5V 30A	F12V 5A	F24V 3A	—	—	2,3,4	*l	NA200R301
	F5V 30A	F15V 4.5A	F15V 4.5A	—	—	2,3,4	*l	NA200R303
	F5V 30A	F24V 3A	F24V 3A	—	—	2,3,4	*l	NA200R304
240 watts single output	5V 48A	—	—	—	—	2,3,4	*m	NS240005
	12V 20A	—	—	—	—	2,3,4	*m	NS240012
	15V 16A	—	—	—	—	2,3,4	*m	NS240015
	24V 10A	—	—	—	—	2,3,4	*m	NS240024
	30V 8A	—	—	—	—	2,3,4	*m	NS240030
	48V 5A	—	—	—	—	2,3,4	*m	NS240048
	56V 4.5A	—	—	—	—	2,3,4	*m	NS240056
300 watts multi output (FC)	+5V 40A	+12V 5A	-12V 5A	+24V 5A	-5V 1A	2,3,4	*n	N300R113U
	+5V 40A	+15V 5A	-15V 5A	+24V 5A	-5V 1A	2,3,4	*n	N300R135U
	F5V 40A	F12-24V 6A(8Apk)	F12-16V 6A(8Apk)	F12-16V 6A(8Apk)	F5-15V 4A(5Apk)	2,3,4	*o	NF300R500
	F5V 40A	F12-16V 6A(8Apk)	F48-56V 5A	F12-16V 6A(8Apk)	F5-15V 4A(5Apk)	2,3,4	*o	NF300R505
300 watts multi output and 48 volt D.C. input (FC)	+5V 40A	+12V 5A	-12V 5A	+24V 5A	-5V 1A	2,3,4	*n	ND300R801
	+5V 40A	+12V 5A	-12V 5A	-50V 5A	-5V 1A	2,3,4	*n	ND300R505
500 watts multi output (FC)	F5V 60A	F12-24V 6A(8Apk)	F12-16V 10A (12Apk)	F12-16V 6A(8Apk)	F5-15V 4A(5Apk)	2,3,4,5	*o+	NF500R500
	F5V 60A	F12-16V 6A(8Apk)	F48-56V 5A	F12-16V 6A(8Apk)	F5-15V 4A(5Apk)	2,3,4,5	*o+	NF500R505

CODES
(S) = Semi regulated (otherwise output is fully regulated) See specification sheets for further detail.
(Q) = Quasi regulated (otherwise output is fully regulated) See specification sheets for further detail.
F = Output is supplied floating
‡‡ = Can be supplied in opposite polarity to special order.
‡ = Floating or in opposite polarity to special order.
* = Localized areas may exceed these dimensions (eg terminal cover). Consult full outline drawings.
(FC)=Forced air Cooling at 1 meter/sec is required.
1 = PCB only.
2 = Mounted on L chassis.
3 = Fully cased (add suffix 'M' to end of model number).
4 = Customized enclosure to special order.
5 = Fully cased with integral fan.

DIMENSIONS (in inches)

	LENGTH	WIDTH	HEIGHT
a	7.19	4.32	2.00
b	6.50	4.15	2.13
c	7.19	4.41	2.13
d	7.19	4.41	2.41
e	7.98	4.72	2.41
f	10.53	4.63	2.36
g	8.30	4.53	2.36
h	7.99	4.43	2.36
i	8.28	4.53	2.36
j	9.74	5.00	2.36
k	10.91	4.93	2.83
l	10.49	4.79	2.76
m	9.76	5.91	2.61
n	12.02	7.59	2.95
o	11.81	7.48	2.56
o+ If Integral fan is required			4.06

Unless noted by "(FC)", power ratings are with convection cooling. Forced Cooling will increase output capacity by 25% on the average.

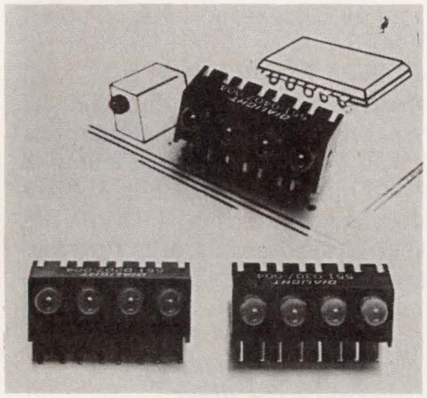
FARNELL ADVANCE POWER

Advance Power Supplies, Inc.
32111 Aurora Road
Solon, Ohio 44139
PHONE (216) 349-0755.
FAX: (216) 349-0142.

703-022

▼ FOUR-ELEMENT LED OPERATES ON 2 MA

A very efficient four-element LED for low-current 2-mA operation has been added to the Series 551 Quad-LED family of arrays for high-density circuit-board applications. In their compact T-1 3-mm-sized envelopes, they are suited for duty as logic-status indicators, binary-data displays, other types of circuit-board indicators, and even panel illumination.

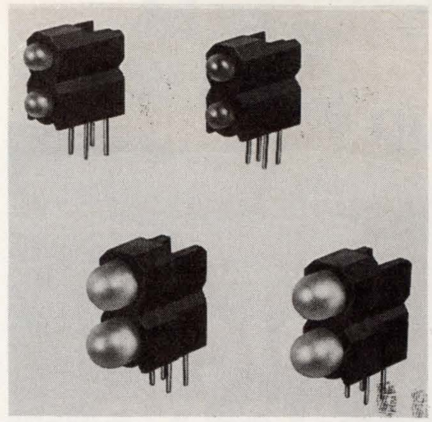


The operating temperature is from –55 to 100°C, and standoffs can provide right-angle viewing. The units, which come in a black housing for increased visibility, are available in standard or custom combinations of green, yellow, and red. Depending on the color combination, prices start at $1.25 each in lots of 1000. Deliveries are from stock to four weeks.

Dialight Corp.
1913 Atlantic Ave.
Manasquan, NJ 08736
(201) 223-9400
▶ **CIRCLE 509**

▼ DUAL-LED ASSEMBLY GOES PIGGYBACK

Two series of dual-LED piggybacked assemblies save board space. The units are available in T-1-3/4 (Series 5670H) and T-1 (Series 5680F) sizes in 2-to-12-V, 1-to-50-mA models. Built-in resistors are included. Two-color units in each of the two LEDs, allowing up to four-color indication,



are also available. Luminous intensities up to 1000 mcd and a high-contrast black-nylon housing make viewing easier. The LEDs are priced from $.38 each in bulk quantities. Free samples are available.

Industrial Devices Inc.
260 Railroad Ave.
Hackensack, NJ 07601
(201) 489-8989
▶ **CIRCLE 510**

OPTOELECTRONICS MANUFACTURERS

Meret Inc.
1815 24th St.
Santa Monica, CA 90404
(213) 828-7496
(FC) (ON) (EM) (IE) (IS) (LL) (OI) (PT)
CIRCLE 605

Micro Switch Div. of Honeywell
11 W. Spring St.
Freeport, IL 61032
(815) 235-6600
(EM) (IE) (LI) (OS) (OI) (PH) (PR)
CIRCLE 606

Mitsubishi Rayon America Inc.
520 Madison Ave.
New York, NY 10022
(212) 605-2392
(FC)
CIRCLE 607

Motorola Semiconductor Opto, Sensor, Comm Prods. Sector
5005 E. McDowell Rd.
Phoenix, AZ 85008
(602) 244-3955
(ON) (EM) (IE) (IS) (LI) (OS) (OI) (PD) (PR)
CIRCLE 608

NEC Electronics Inc.
401 Ellis St., Box 7241
Mountain View, CA 94039
(415) 960-6000
(ON) (LL) (OI) (PC) (PT) (PR)
CIRCLE 609

NSG America
28 Worlds Fair Dr.
Somerset, NJ 08873
(201) 469-9650
(FC) (ON) (EM) (IE) (OS) (OI)
CIRCLE 610

NTE Electronics Inc.
44 Farrand St.
Bloomfield, NJ 07003
(201) 748-5089
(IE) (IS) (LL) (LI) (OI) (PD) (PT) (PR)
CIRCLE 611

Optek Technology Inc.
1215 W. Crosby Rd.
Carrollton, TX 75006
(214) 323-2200
(EM) (IE) (IS) (LI) (OS) (OI) (PD) (PT) (PR)
CIRCLE 612

Opto Diode Corp.
750 Mitchell Rd.
Newbury Park, CA 91320
(805) 499-0335
(LI)
CIRCLE 613

Rohm Corp. Rohm Electronics Div.
8 Whatney
Irvine, CA 92718
(714) 855-2131
(IE) (IS) (LL) (LI)
CIRCLE 614

SI Tech
Box 609
Geneva, IL 60134
(312) 232-8640
(FC) (ON) (EM)
CIRCLE 615

Seiko Instruments U.S.A. Fiber Optic Comp. Div.
2990 W. Lomita Blvd.
Torrance, CA 90505
(213) 517-7841
(FC) (ON) (EM) (LL)
CIRCLE 616

Sharp Electronics Corp. Electronic Comp. Div.
Sharp Plaza, Box 650
Mahwah, NJ 07430
(201) 529-8757
(FC) (EM) (IE) (IS) (LL) (LT) (OS) (OI) (PH) (PC) (PD) (PT) (PR) (UV)
CIRCLE 617

Shelly Associates
14811 Myford Rd.
Tustin, CA 92680
(714) 669-9850
(LL)
CIRCLE 618

Shogyo International Corp.
287 Northern Blvd.
Great Neck, NY 11021-4799
(516) 466-0911
(LL) (LI)
CIRCLE 619

Shokai Far East Ltd.
280 N. Central Ave.
Hartsdale, NY 10530
(914) 681-0700
(IE) (IS) (LL) (LT)
CIRCLE 620

Siecor Electro-Optic Products
Box 13625
Research Triangle Park, NC 27709
(919) 481-5100
(FC) (ON)
CIRCLE 621

Siemens Components Inc. Optoelectronics Div.
19000 Homestead Rd.
Cupertino, CA 95014
(408) 257-7910
(LL) (OI)
CIRCLE 622

Silicon Detector Corp.
1240 Avenida Acaso
Camarillo, CA 93012
(805) 484-2884
(EM) (IE) (IS) (LL) (LI) (PH) (PC) (PT) (PR) (UV)
CIRCLE 623

Silicon Sensors Inc.
Old Hwy. 18 East
Dodgeville, WI 53533
(608) 935-2707
(IE) (IS) (LL) (LT) (OS) (OI) (PH) (PC) (PD) (PT) (PR) (UV)
CIRCLE 624

Sprague Electric Co. Aluminum Capacitor Div.
Box 9102
Mansfield, MA 02048
(800) 777-7575
(OS) (PT)
CIRCLE 625

TDK Corporation of America
1600 Feehanville Dr.
Mount Prospect, IL 60056
(708) 803-6100
CIRCLE 626

Texas Instruments Semiconductor Group
Box 809066
Dallas, TX 75380-9066
(214) 995-6611
(EM) (IE) (IS) (LL) (LT) (OS) (OI) (PH) (PC) (PT) (PR) (UV)
CIRCLE 627

Theta-J Corp.
107 Audubon Rd.
Wakefield, MA 01880
(617) 246-4000
(OS) (OI) (PD) (PT) (PR)
CIRCLE 628

Toshiba America Inc. Semiconductor Operation
9775 Toledo Way
Irvine, CA 92718
(714) 455-2000
(LL) (OS) (OI) (PD) (PT) (PR)
CIRCLE 629

KEY

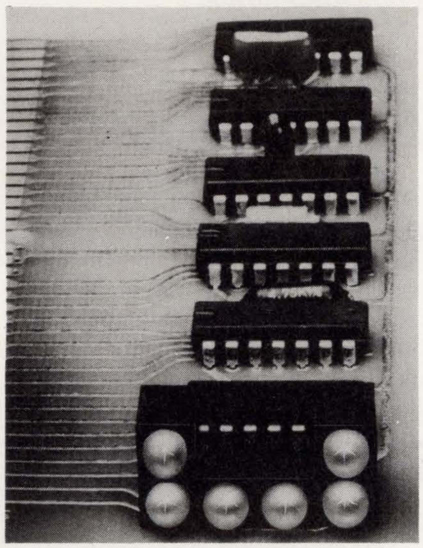
Optoelectronics

(FC)	Fiber-optic cables
(ON)	Fiber-optic connectors
(EM)	Fiber-optic emitters/detectors
(IE)	Infrared emitters
(IS)	Infrared sensors
(LL)	LEDs, light-emitting
(LI)	LEDs, IR-emitting
(OS)	Optical switches
(OI)	Optocouplers/isolators
(PH)	Photocells
(PC)	Photoconductive cells
(PD)	Photodarlingtons
(PT)	Photodiodes and arrays
(PR)	Phototransistors
(UV)	UV sensors

OPTOELECTRONICS

▼ LED DISPLAYS GET BRIGHTER

With their luminous-intensity ratings of 1000, 2000, or 3000 mcd, the 200K-R1K GaAlAs LEDs boast a luminous intensity that's 15 times brighter than standard water-clear units. That makes them well suited for outdoor applications. They come in a T-1-3/4 size snap-in or panel-mounting package as well as any 200-size package from the PCB line.

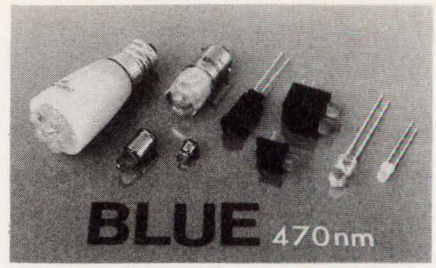


The panel-mount package can be manufactured in a tight-water version. The LEDs produce a red output with a peak wavelength of 660 nm. The 3000-mcd LED operates on a typical forward voltage of 1.8 V and offers a viewing angle of 35°. Prices begin at $.58 per unit in quantities of 1000. Delivery is in six weeks after receipt of order.

Data Display Products
445 S. Douglas St.
El Segundo, CA 90245-4630
(203) 640-0442
▶ **CIRCLE 666**

▼ BLUE LEDS LIGHT UP MEDICAL PANELS

Low-cost blue-light LEDs are now available in production quantities as discretes or in clusters housed in most industry-standard package styles. The 470-nm true-blue-peaked LEDs can replace incandescent filament lamps with blue filters and the older high-cost blue LEDs. The color blue is specified for critical status indicators in medical instruments and other control panels. The rugged LED lasts about 100,000 hrs compared with only about 4000 hrs for an



incandescent lamp. The LED chip operates on 20 mA and uses 170 mW, while a higher-powered 50-mA version uses 200 mW, with intensities of 5 and 10 mcd, respectively. Typical forward-voltage drop is between 3 and 3.7 V. Viewing angle is 12° with water-clear encapsulation, and 30° with translucent white. In quantities of 1000, the blue LEDs cost from $12 to $15 in standard packages. Clusters of seven run from $60 to $70. Delivery is four to six weeks for standard packages and eight to 12 weeks for clusters.

Ledtronics Inc.
4009 Pacific Coast Hwy.
Torrance, CA 90505
(213) 549-9995
▶ **CIRCLE 667**

▼ LED LASERS DELIVER VISIBLE LIGHT

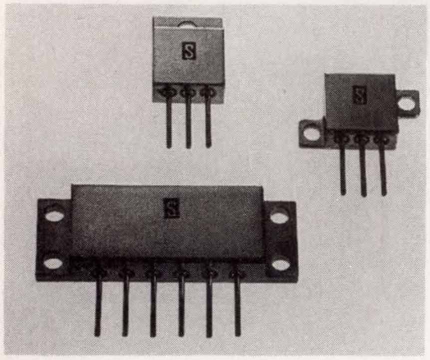
For applications such as bar-code readers, optical-alignment systems, and target markers, the CQL80/D emits 5 mW of a typical peak wavelength of 675 nm, a red light easily visible to the eye. Its life is anticipated at about 250,000 hrs under 3-mW continuous-wave operation at ambient temperature. Mounted in a 9-mm encapsulation, the device includes a monitor diode optically coupled to the rear facet of the laser to control the optical-output level. The low-power CQL90/D, a light-emitting collimating pen, has a power output of 1 mW at 675 nm. Encapsulated in a nonhermetic, circular stainless-steel enclosure, the pen is 11 mm in diameter with an accuracy between +0 and −11 μm. Unit pricing is $48 for the CQL80/D and $135 for the CQL90/D in lots of 5000. Delivery is up to eight to 12 weeks, respectively, depending on quantity.

Philips Components
Discrete Products Div.
2001 W. Blue Heron Blvd.
Riviera Beach, FL 33404
(407) 881-3308
▶ **CIRCLE 668**


Sipex
HS574A

▼ POWER MOSFETS ARE SEALED TIGHT

A line of MOSFET and Schottky power devices targeted for military and aerospace applications is now available in hermetically sealed TO-220 packages (TO-254, TO-258, etc.), as well as in multipin high-power flat packs. The devices feature one-piece copper construction instead of the



usual baseplate with a brazed-ring frame. Particularly important to high-reliability users are the packages' rugged ceramic feed-through seals, which eliminate the problem of cracking when glass seals are used. Pricing begins at $20 in 100-piece quantities with eight-to-10-week delivery.

Solitron Devices Inc.
1177 Blue Heron Blvd.
Riviera Beach, FL 33404
(800) 888-8763
▶ **CIRCLE 669**

▼ ISOLATED DIODE RECOVERS IN 200 NS

An isolated diode module from Marconi features an ultrafast reverse recovery time of 200 ns. The IMP110 module is intended for use with high-frequency devices such as IGBT and FET inverters and switching-power-supply freewheel and snubber diodes. Electrically isolated to 2500 V, the diode can handle over 100 A at 1200 V. The reverse-recovery charge is less than 20 μC at 40 A and a di/dt of 100 A/μs. The module measures 3.62-by-1.38-by-0.91 in. and has industry-standard mounting centers of 80 mm. Prices for the IMP110 start at $49 for one to nine pieces; delivery is six to eight weeks.

Marconi Circuit Technology
160 Smith St.
Farmingdale, NY 11735
(516) 293-8686 Ext. 432
▶ **CIRCLE 670**

▼ DIN CONNECTOR SIMPLIFIES ASSEMBLY

Designed to simplify assembly, a series of circular DIN connectors provides easy snap-in seating of the pin-and-wafer assembly into the low-profile one-piece metal shell, which gives it a streamlined appearance and EMI/RFI shielding. An available assembly tool guarantees a perfect hex-crimp strain-relief around the cable, thereby preventing molding compound from entering the connector. In addition to a standard male plug, the company offers a locking (30° twist) version in three-to-eight-pin configurations. Connector shells are of nickel-plated stamped steel. Pricing ranges from $0.70 to $1.50, and all versions are available from stock.

Preh Electronic Industries Inc.
470 E. Main St.
Lake Zurich, IL 60047-2578
(312) 438-4000
▶ **CIRCLE 671**

▼ MORE PINS ADDED TO LCD DISPLAYS

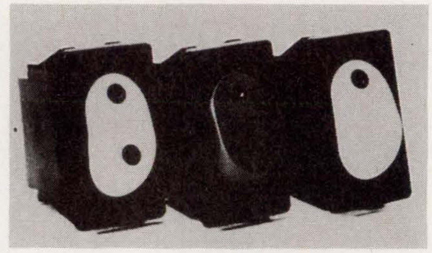
A technique that increases the number of pin terminals that can be affixed to a liquid-crystal display allows more information to be accessed by small LCDs. The pin pattern of terminals are on 0.075-in. centers. This feature complements the complex and dense information-display demands of many LCD applications and eliminates the need for alternate connector methods. The terminals can be supplied in all popu-

lar pin lengths from 0.120 through 0.350 in. long. Call for pricing and availability.

Standish Industries Inc.
Hamlin LCD Div.
W7514 Highway V
Lake Mills, WI 52551
(414) 648-1000
▶ **CIRCLE 672**

▼ EURO-STYLED SWITCHES FIT STANDARD OPENINGS

For designs with a European look, a family of oval-shaped rocker switches fits standard rectangular openings and can often be used without retooling. Applications include business machines, appliances, furni-



ture, marine panels, and many others. Available in one-light, two-light, and unlighted models, the Euro-Switch is UL-listed and CSA-approved for 3-A, 277-V ac; 6-A, 125-V ac; and 1/4-to-3/4-hp, 125-to-277-V ac ratings. The switch comes in both single- and double-pole styles and can be easily matched with a gasket for added moisture resistance.

McGill Manufacturing Inc.
1002 N. Campbell St.
Valparaiso, IN 46383
(219) 465-2200
▶ **CIRCLE 673**

▼ RELAY SWITCHES LOW SIGNAL LEVELS

Primarily for telecommunications applications, the NA relay has double-pole, double-throw bifurcated crossbar contacts rated at 1 A. The relay meets FCC Part 68, Bellcore, UL, and CSA specifications and has a minimum electrical life of 500,000 operations. The dielectric with open contacts can withstand 1000 V ac. Coil voltages range from 4.5 to 48 V dc, and the nominal power consumption is 140 mW. The ambient operating temperature ranges from –40°C to 85°C. Backfilled with nitrogen gas and permanently sealed, the maximum package dimensions of the relay are 0.55 in. long, 0.30 in. wide, and 0.37 in. high. Other applications include security systems, instruments, and portable devices. In quantities of 1000 pieces, pricing starts at $3.06 each. Lead time is 10 to 12 weeks.

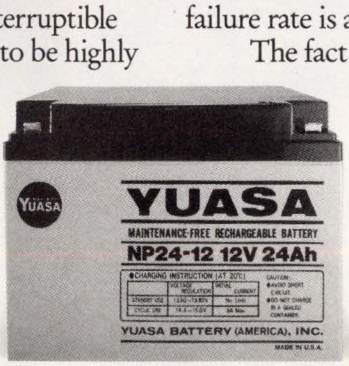
ITT Components
5 Jenner St.
Irvine, CA 92718
(714) 727-3001
▶ **CIRCLE 674**

Who interrupted the uninterruptible power system?

Did somebody push the wrong switch?

Was it faulty design?

Not at all. The uninterruptible power system turned out to be highly interruptible because a battery died. Scary, isn't it? You get a power system failure followed by a power backup system failure and—presto—you're plunged into darkness. Of course, while you'll recover, your computers won't. Their memories will be gone for good.



Well, it wouldn't have happened had that battery been a Yuasa. With Yuasa, sudden death is a virtual impossibility. Its failure rate is an almost non-existent .001.

The fact is that Yuasa is used by more UPS manufacturers than any other battery made today. No other sealed lead acid battery is more dependable or lasts longer.

Our point is simple. The next time you're designing an uninterruptible power system, make sure it stays uninterruptible.

Specify the battery that doesn't die on the job.

YUASA

The World Leader In Back-Up Energy.

Yuasa Battery (America), Inc. 9728 Alburtis Avenue Santa Fe Springs, CA 90670 (213) 949-4266 or (800) 423-4667
Eastern Regional Office 131 Industrial Ave. Hasbrouck Heights, N.J. 07604 (201) 641-5900 or (800) 962-1287

CIRCLE 158

▼ CHOOSE CARBON, CERMET OPEN-FRAME TRIMMERS

The 3300 family of single-turn open-frame trimmer resistors are low-cost components for circuit adjustments. Although carbon-resistance elements are usually the designer's first choice for economy, the cermet-resistance types should also be considered, according to the 12-page bulletin from Bourns. For industrial use, the cermet elements have better load stability, a superior temperature coefficient, improved moisture resistance, and higher power ratings than corresponding carbon units. Carbon units may give the lowest absolute cost, but cermet units can give the best performance per dollar. The bulletin will help designers compare performance factors and select the trimmer suited for the application.

Bourns Inc.
1200 Columbia Ave.
Riverside, CA 92507
(714) 781-5500
▶ CIRCLE 675

▼ CARBON-COMPOSITION RESISTORS FILL BILL

Hot-molded, carbon-composition fixed resistors are still vital components in modern electronic circuitry. A comprehensive 45-page guide provides in-depth data on Allen-Bradley's complete line from 1/8-to-4-W sizes. The first and second pages contain a selection guide to help make initial design decisions. Following are charts of detailed performance characteristics, temperature, derating, and other environmental specifications, packaging information, testing and reliabiltiy data. Six pages of power nomographs reflect years of experience and testing. The last page expands into a handy color chart explaining the MIL and EIA resistor color-band coding.

Allen-Bradley
Electronic Component Div.
1414 Allen-Bradley Dr.
El Paso, TX 79936-6415
(800) 592-4888
▶ CIRCLE 676

▼ FILM CAPACITORS BOAST HIGH RELIABILITY

Hermetically sealed high-reliability plastic-film capacitors that meet MIL-C-83421/39022-9/87217 military specifications are described in this 44-page booklet. The company's quality-control system, which is maintained in a complete military-approved environmental testing laboratory, is approved to MIL-Q-9858 and MIL-STD-790 standards. Also, its calibration laboratory complies with MIL-STD-45662 specifications. The catalog includes sections on the various available diectrics: metallized-polycarbonate, metallized-polypropylene, polyphenylene-sulfide, metallized-teflon, and polystyrene. Specifications listed include full case dimensions, ac ratings, and life-test data.

Component Research Co.
1655 26th St.
Santa Monica, CA 90404
(213) 829-3615
▶ CIRCLE 677

No. 5

Watt's Up™ from Semiconductor Circuits, Inc.

New DC/DC Converter Delivers 4.5 Watts in Half the Space at a Fraction of the Cost

The pioneering technology leader in encapsulated power converter modules, Semiconductor Circuits, Inc. introduces the QA series for space critical applications. For pin-for-pin replacement of 2" x 2" converters, the QA series offers 4.5 watts in a low profile case measuring just 1.0" x 2.0" x 0.4". And it offers all that performance at a significantly reduced price.

With the QA series, you also don't need to sacrifice a wide input range to have linear features such as low ripple and tight power regulation. The QA gives you both.

To achieve these price/performance breakthroughs, the QA series incorporates our extensive MOSFET and surface mount technology. These features also allow us to achieve higher power density and higher reliability.

With an input/output isolation of 500 Vdc, an operating temperature range of -25°C to +71°C, with no derating, efficiencies of 75% (typical), continuous short circuit protection and output voltage tracking providing protection for power sensitive devices requiring ± voltages. The QA series is ideal for many board-level power conversion applications. Including cellular and portable telecommunications, process control, ATE,CAD/CAM, and other space critical applications.

For more information on how to put the QA series to work for you, please contact your nearest Semiconductor Circuits, Inc. distributor or representative. Or contact us direct in New Hampshire, (603) 893-2330 or FAX: (603) 893-6280. And be sure to ask for the latest edition of our Quick Selection Guide to Power Converters.

Key Features	
Power	4.5 watts
Inputs	5.0 Vdc; 9.0 - 36.0 Vdc; 20.0 - 72.0 Vdc
Short Circuit Protection	Continuous with auto restart
Package Size	1.0" x 2.0" x 0.4"
Isolation	500 Vdc
Efficiency	75% (typical)

SEMICONDUCTOR CIRCUITS, INC.

SUBSIDIARY OF ASTEC AMERICA, INC.

CIRCLE 149

ASTEC

49 Range Road • Windham, New Hampshire 03087 • (603) 893-2330 FAX: (603) 893-6280

NEW LITERATURE

▼ QUARTZ CRYSTALS OPERATE AT 800 HZ

Very-low-frequency quartz crystals, from 800-Hz J-series types to high-frequency AT-cut units ranging to 300 MHz, as well as the DT-cut series operating from 80 to 500 kHz, are specified in this eight-page design guide. The guide includes dimensionally detailed illustrations of many standard crystal holders, design data, and typical oscillator circuits.

Standard Crystal Corp.
9940 E. Baldwin Pl.
El Monte, CA 91731
(818)443-2121
▶ **CIRCLE 678**

▼ SMALL INDUCTORS ARE SURFACE MOUNTED

In eight pages, ISI covers its line of surface-mountable inductors ranging in value from 0.047 to 1000 μH. Photos, dimensional outlines, graphs, and charts fully describe their characteristics and describe applications for the various inductor designs: multilayer chip, molded shielded, shielded-chip beads, and multilayered-chip beads. Impedance-versus-frequency graphs of the units' characteristics give users a better idea of how they will behave in a circuit than can single nominal values from charts.

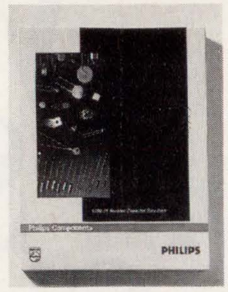
Inductor Supply Inc.
1849 W. Sequoia Ave.
Orange, CA 92668-1017
(714) 978-2277
▶ **CIRCLE 679**

▼ CUT LOSSES WITH FIBER-OPTIC LINKS

To accurately transmit a great amount of information over long distances, fiber-optic technology offers many advantages compared with copper-wire systems. The advantages include wide bandwidth, EMI immunity, low signal losses, small size, light weight, security, safety, and electrical isolation. The AMP Optimate catalog, a hefty 88-page volume, covers cable, connectors, splicing and repair kits, test equipment, couplers, optical switches, tools and other accessories. Seven pages summarize fiber-optic technology.

AMP Inc.
Harrisburg, PA 17105
(717) 564-0100
▶ **CIRCLE 680**

▼ RESISTOR, CAPACITOR DATA PRESENTED



A massive 700-page data book covers aluminum-electrolytic, ceramic, tantalum, film, and variable capacitors. In addition, the catalog provides full details on fixed, trimmer, and nonlinear resistors. Each section begins with a quick-reference index of all products. A complete competitor cross-reference section is featured.

Philips Components
Discrete Products Div.
2001 W. Blue Heron Blvd.
Riviera Beach, Fl 33404
(800) 447-3762
▶ **CIRCLE 681**

▼ QUARTZ OSCILLATORS WORK AT 0.0006 HZ

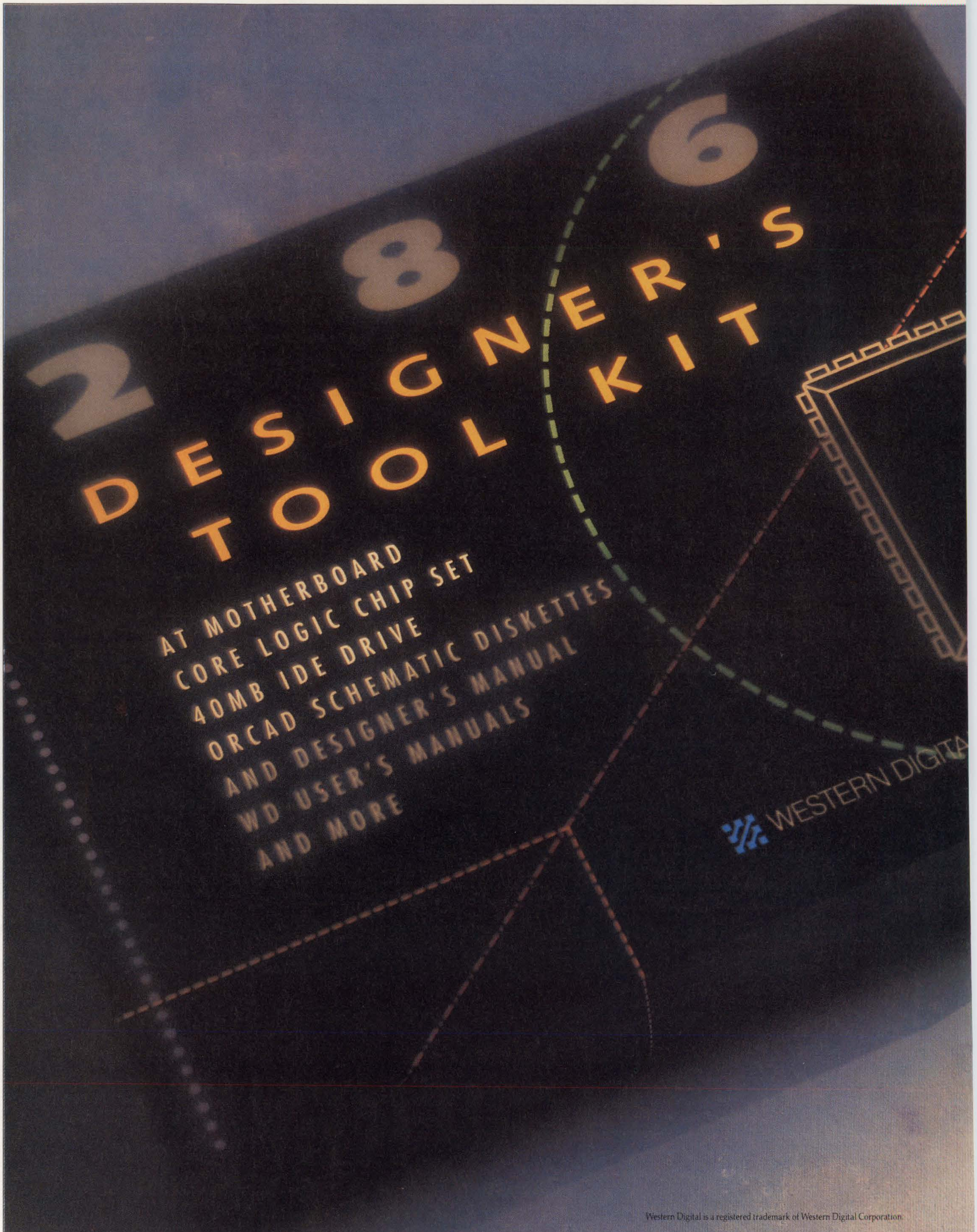
A four-page short-form catalog describes Statek's line of quartz crystals and quartz-crystal oscillators that operate from 0.0006 Hz to 2 MHz in DIP and TO-5 housings. For example, the CX series crystals consist of miniature quartz resonators hermetically sealed in rugged ceramic packages. They're available in two case sizes. An LXO series oscillator comes in a 4-pin metal case centered on a 14-pin DIP footprint.

Statek Corp.
512 N. Main
Orange, CA 92668
(714) 639-7810
▶ **CIRCLE 682**

▼ VARIED RESISTORS IN SHORT FORM

Resistors of many descriptions, from metal-film types to carbon-film devices to temperature-sensing resistors, can be found in a 28-page short-form catalog. The book includes taping and packing specifications as well as conversion tables and a handy color-code chart. Information is included on scores of resistors in 14 different types with full electrical and dimensional specifications.

Robert G. Allen Co. Inc.
7267 Coldwater Canyon
North Hollywood, CA 91605
(800) 423-3186
▶ **CIRCLE 683**


286
DESIGNER'S
TOOL KIT
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CORE LOGIC CHIP SET
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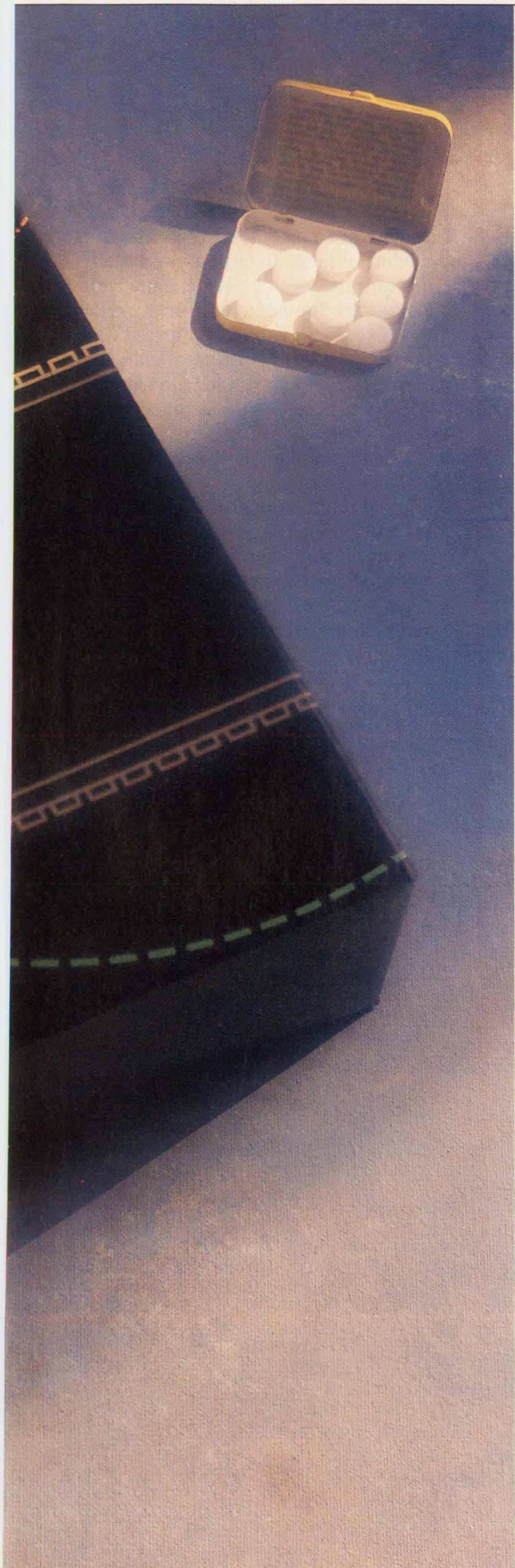
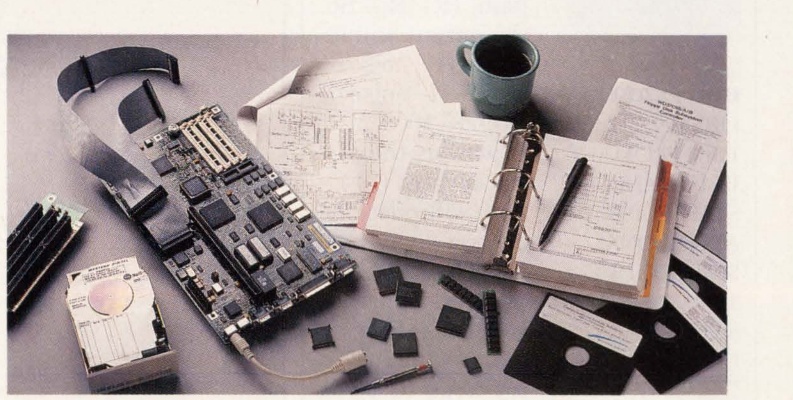
AND DESIGNER'S MANUAL
WD USER'S MANUALS
AND MORE
WESTERN DIGITAL

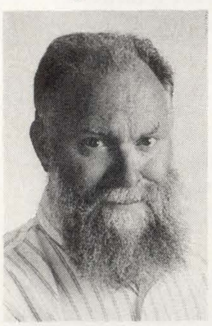




WHAT'S ALL THIS NOISE STUFF, ANYHOW? (PART I)

Recently I was invited to a meeting to see the results of a new high-performance, low-noise transistor project. I looked at the technical report. The new transistors were indeed quieter than the old ones. In fact, they were 2 to 4 *orders of magnitude* quieter than the conventional ones. I was suspicious. What was the test method? Oh, here is the test circuit *(see the figure)*.

Now, I asked, were the betas high or low? I was told they were pretty low, but they can be brought up later. I explained that when the betas get low, if they're not very well matched, the test circuit's output can peg—right up to the + or – rail. Then, of course, the apparent output noise gets rather small. (Ohhhhh!)



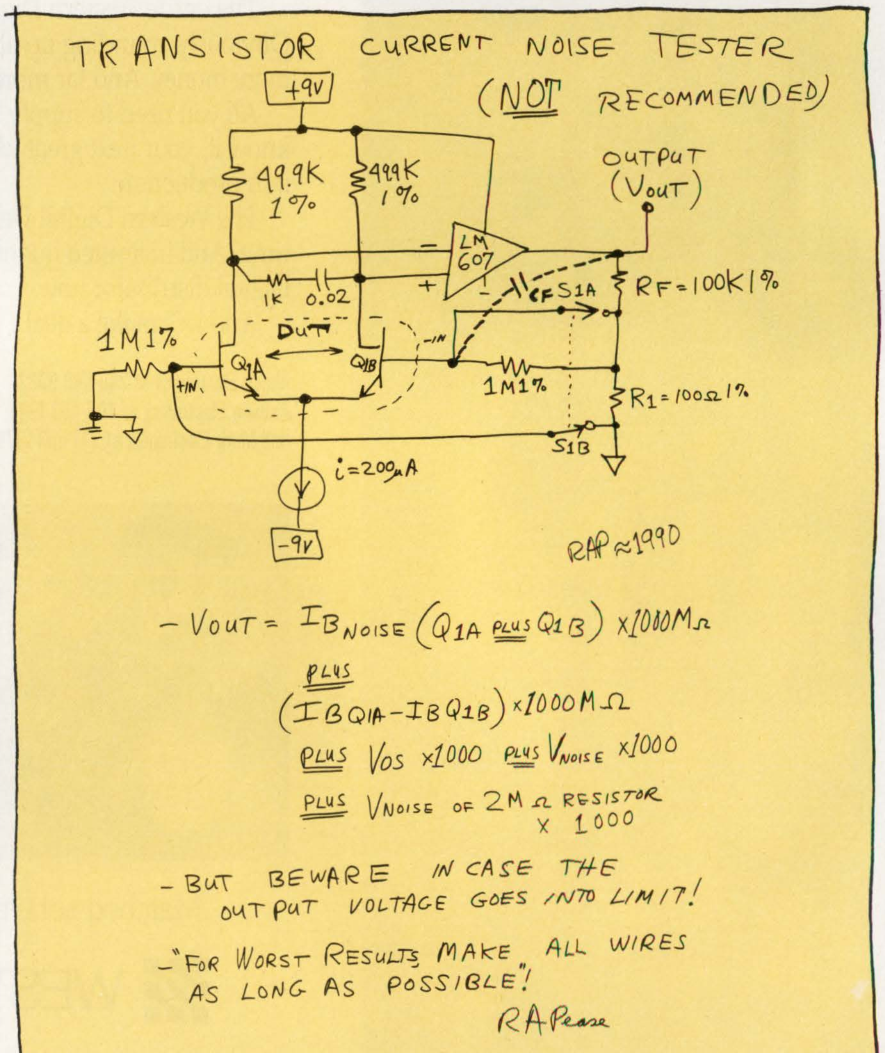
BOB PEASE
OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

When this circuit is running okay, the current noise is amplified by a big resistance: 1 MΩ × (N+1), where N is the closed loop gain, (R_F/R_1). So, the output will include: (I+ noise of Q_{1A}) + (I– noise of Q_{1B}) × 1000 MΩ. However, the offset current (I+) – (I–) will also be magnified by 1000 MΩ. So even 9 nA of offset current will cause the op amp's output to try to go to +9 V. If the power supply won't let the output get to a fair balance, the output will peg. Naturally the output becomes very quiet—the circuit has stopped amplifying the noise.

I also pointed out that ideally the circuit could measure the base-current noise of the transistor, or device under test (DUT). But the layout of the circuit is quite critical. Just 1 pF of capacitance (C_F) from the output to the base of Q_{1B} will cause a lag in the response: 1000 MΩ × 1 pF = 1 ms, so the noise will roll off above 160 Hz. You can make a layout with less than 0.1 pF, but you have to think about it and engineer it.

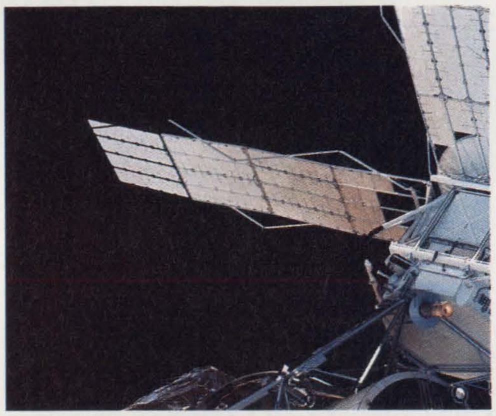
When we checked the test box, it was laid out very neatly: The output wire was bused alongside the summing-point (base of Q_{1B}) wire, and the bandwidth was indeed less than 100 Hz. In a future column, I will talk about what a picofarad looks like and the harm it can do to you. So, even if the output wasn't pegged and you looked for the noise at 1 or 10 kHz, this test circuit would give an answer that's considerably quieter than the *theoretical* minimum for the transistor. Now here's a good place for a sanity check.

It's not impossible to measure the noise of a transistor's base current, but you must have a suitable circuit. I wrote a paper back in 1968, and as I look at it today, the only things that changed are the names of the op amps. You can't buy any of those old discrete-transistor, potted-module op amps any more, but the testing



SPACE QUALIFIED, RAD-HARD CUSTOM CIRCUIT, 14 WEEK DESIGN.

WAS SECRET CRAZY OR WHAT?



Some stories can't be told.

We're going to try anyway and still respect confidentiality.

A major aerospace company wanted a RAD-HARD, space-qualified stepper-driver for positioning the solar array of a highly sensitive military satellite. They wanted fail-safe performance plus adherence to a set of intimidating specs.

And they wanted it fast. "We're in a bit of a hurry," they said.

That was enough for the incumbent. They stepped out of the picture.

Which is just when we stepped in.

You see, few companies in the U.S. can build custom circuits like Silicon General can—quickly, reliably and profitably. That's because in over 20 years of solving problems in silicon, our files are bulging with thousands of IC solutions. We've developed an encyclopedia of circuit design and manufacturing solutions that lead us around the problems and pitfalls that plague less experienced vendors.

We work in partnership with your engineering department through every stage of design and manufacturing and will often assign a full-time project manager to oversee your job, as we did with this customer.

In the case of the stepper-driver, our drop-in replacement not only met form, fit and function, our specs gave the customer a little more latitude to meet his own price/performance requirements.

And to cap it off, we even delivered ahead of schedule.

If you need a partner to design and manufacture power IC's, someone who can meet "impossible" specs and deadlines, remember, nothing is as crazy as it sounds.

Not when you call in the General.

To hear more, contact Silicon General, 11861 Western Avenue, Garden Grove, CA 92641. TWX: 910-596-1804. FAX: (714) 893-2570. Phone (714) 898-8121.

SILICON GENERAL

Solutions... that's the general idea.

CIRCLE 118

approaches are just as valid. Maybe I'll write an updated version. In this case, the problem was that a 1-MΩ resistor and a noise gain of 100 or 1000 (provided by R_F and R_1) wasn't a good idea. The stray capacitances and the noise of the 1-MΩ resistor are detrimental to accuracy. It's better to use a real 100-MΩ or 1000-MΩ resistor.

In fact, a 20-MΩ or 5-MΩ resistor is justified because it will still give plenty of signal-to-noise ratio, and a lot more bandwidth. More on how to do this in the next issue.

All for now. / Comments invited! / RAP / Robert A. Pease / Engineer

ADDRESS:
Mail Stop C2500A
National Semiconductor
P.O. Box 58090
Santa Clara, CA 95052-8090


1990-91 Resistor/Capacitor Data Book
PHILIPS

ULTRA-THIN PACKAGES HOUSE DRAMS, SRAMS

Adding the ultra-thin plastic small-outline package (SOP) to its list of packaging options, Hitachi America Ltd., Brisbane, Calif., gives designers another choice for 1- and 4-Mbit dynamic RAMs, and 1-Mbit static RAMs. The ultra-thin packages are just 0.047-in. (1.2-mm) thick—one-third the height of standard small-outline J-leaded packages. Their lead pitch is about 40% that of the SOJ—just 0.5 mm. The TSOP's small size means more chips on a circuit board, and the low profile means better cooling airflows. The 1-Mword-by-1-bit and 256-k-by-4 megabit DRAMs, the 4-M-by-1 and 1-M-by-4 4-Mbit chips, and the standard and low-power 128-k-by-8 SRAMs will all be included in the TSOP. The 1-Mbit DRAM TSOP is 6 by 16 mm, while the 4-Mbit DRAM and 1 Mbit SRAM TSOP are 8 by 20 mm. The TSOP option will also be offered for pseudostatic RAMs, EPROMs, EEPROMs, and mask ROMs. In 10,000-unit lots, the 1-Mbit DRAM (80 ns) in the TSOP sells for $9. The 4-Mbit DRAM sells for $48.75 and the 1-Mbit SRAM (100 ns) costs $25.50 in 5000-unit lots. Call Sally Withers for the 1-Mbit DRAM, Carrie Shulman for the 4-Mbit DRAM, and Victor Zilinskas for the 1-Mbit SRAM, (415) 244-7146, 7131, and 7183, respectively. *DB* **CIRCLE 631**

200-V-CMV DIFF-AMP NOW IN 8-PIN SOIC

A differential amplifier from Burr-Brown—the INA117—can now easily handle 200 V of common-mode voltage (CMV) in an 8-pin SOIC package. That's in addition to its original 8-pin TO-99 and miniDIP packages. The IC makes it possible to process millivolt signals riding on CMVs of more than ±15 V, with devices running off ±15-V rails. The precision IC op amp, which includes a thin-film resistor network, provides a fixed, differential-in to single-ended-out gain of unity while attenuating the CMV by a factor of ten. It's ideal for monitoring the current in the hot side of a high-voltage (up to 200 V) power supply. Gain accuracy at 25°C is 0.02% maximum and gain drift runs 10 ppm/°C. Full-power bandwidth is a minimum of 30 kHz. As a result, the device isn't limited to just dc levels. In quantities of 100, the amplifier costs $4.85 each. Call Bruce Trump at (602) 746-7347 or 1-(800) 548-6132, or their bulletin board at (602) 741-3978. *FG* **CIRCLE 632**

NONVOLATILE MEMORIES LEAVE THEIR MARK

With its latest nonvolatile-memory offerings, the nonvolatile division of Hitachi America Ltd., Brisbane, Calif., has covered almost every design need. The offerings include fast 4- and 1-Mbit EPROMs, a 1-Mbit flash EEPROM, a medium-speed 256-kbit full-function EEPROM, and a 4-Mbit masked ROM. Thanks to a fine-line 0.8-μm process, the EPROMs can access in as little as 100 ns. They're organized as a 256-kword-by-16-bit (HN27C4096) or as 128-k-by-8-bit (27C101A) memories. The megabit flash chip (HN29C101) is also organized as a 128-k-by-8-bit array and can endure more than 100 erase cycles. The chip's access time is 120 or 150 ns, and can be reprogrammed by applying a 12-V signal. The companion EEPROM, the HN58C256, is a basic EEPROM memory chip with an access time of 200 ns. The 4-Mbit ROM offers a 100-ns access time, and mounts in a multichip configuration to achieve 8- and 16-Mbit storage arrays in a 48-lead package. Chip prices start at $7 in volume for the ROM; $13 and $35, respectively, for the EEPROM and flash EPROM; $53 for the 4-Mbit UV EPROM; and $6 to $8 for the 1-Mbit UV EPROM. *DB* **CIRCLE 633**

STANDARD PALETTE DAC BECOMES STANDARD CELL

Joining the growing ranks of 8-bit triple-palette DAC suppliers for IBM PCs and clones, Sierra Semiconductor of San Jose, Calif., is offering the device both as a standard product and as a cell in their 1.5-μm mixed-signal CMOS library. Four speed versions of the product—the SC11478—are available between 35 and 80 MHz. Use of the VDAC78 cell (identical to the SC11478) in Sierra's library gives designers flexibility in creating proprietary solutions to CRT displays. The chip (and cell) also holds an anti-sparkle circuit that maintains prior output-color data on the three DAC outputs. At the same time, it transfers data between the lookup table RAMs and the RGB color registers. Housed in a 44-pin PLCC, the SC11478 costs between $3 and $5 each in 10,000-unit quantities, depending on speed. Call Zaheer Hassan, (408) 263-9300. *FG* **CIRCLE 634**

IC DIP OP AMPS MOVE INTO 8/14-PIN SOICS

Following the strong demand for ICs in surface-mounted packages, Harris Semiconductor, Melbourne, Fla., is producing 16 standard and proprietary amplifiers available in narrow-body SOICs. Heading the list are four high-speed op amps: the HA-5195, HA-2539, HA-2540 and HA-2544. It also includes the HA-5002 and HA-5033 video buffers and the HA-5141/42/43 low-power op amps. All nine devices are made on the Harris dielectrically isolated (DI) bipolar process. Low-noise op amps in these packages include the HA-5101/5111, the HA-5102/5112, and the HA-5104/5114. Also on the list is the general-purpose HA-4741. Call 1-(800)-427-7747. *FG* **CIRCLE 635**

TURN A FEW DOLLARS INTO A COOL 18 MILLION.

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18 MIPS.

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Applications are increasingly burdened with the overhead of friendliness. Even so, users expect everything to happen immediately, if not sooner.

As a result, applications with embedded microprocessors need more computing power than ever. Our CY7C611 SPARC RISC controller gives you the power to create, at a price that fits your application.

It performs. At 25 MHz, our CY7611 delivers 18 sustained MIPS.

It handles interrupts brilliantly. Asynchronous and synchronous traps let you jump to trap routines with 200 ns worst case response. 16 prioritized interrupt levels let you tailor your application. You get 136 32-bit registers that you can divide into register banks for fast context switching.

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It is extendable. You get a large address space, and support for multitasking and multiprocessing.

It is affordable. We're talking a few dollars per MIPS.

And it is SPARC. You can choose from a multitude of SPARC platforms to operate as native development platforms. You work with the world's most popular RISC architecture. You can expect faster evolutions, to keep your design current well after it is designed.

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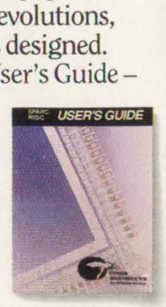

Free SPARC RISC User's Guide.
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PROGRAMMABLE FUNCTIONS LEAD TO COST-EFFECTIVE TRANSMISSION OF VIDEO AND PHOTO-QUALITY STILLS.

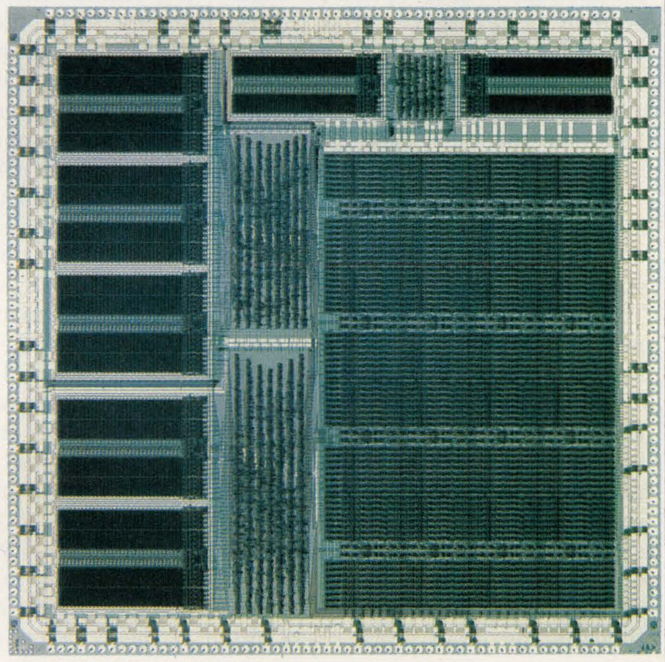
CHIP SET BROADENS OPTIONS FOR IMAGE COMPRESSION

MILT LEONARD

A surging trend in information handling is the merging of text, still images, and full-motion video pictures in computer terminals and workstations. Forcing this trend are rapid advances in data reduction and compression techniques, which reduce the amount of memory required to store data, as well as the bandwidth needed to transmit the data. And, with advances in VLSI, large arrays of digital signal processors are no longer required to handle the intense computations involved.

For example, LSI Logic has developed a new image-compression CMOS chip set which, when interconnected to form an image-processing pipeline, offers user-selectable image-compression ratios for both still and video images. Moreover, the chip set allows designers to take a building-block architectural approach—for maximum flexibility—in the face of a still-evolving standards environment.

The 40-MHz chip set consists of the L64760 interframe processor, L64730 discrete cosine transform (DCT) processor, L64740 DCT quantization processor, and the L64720 video motion-estimation processor *(Fig. 1)*. It also inlcudes the L64750 variable-length encoder, and L64715 error-correcting encoder-decoder. The chip set's programmable features not only afford a substantial amount of application flexibility, but also make it possible for designers to track the emerging standards. These include the CCITT (International Consultative Committee for Telegraphy and Telephony) H.261 standard for video conferencing (specifying VHS/VCR-type broadcast quality, which is about half that of broadcast television operating at 27 Mpixels/s), the JPEG (Joint Photographic Experts Group) standard for still-picture transmission, and the MPEG (Motion Pictures Experts Group) standard. The latter, which is a combination of JPEG and H.261,



1. A KEY PLAYER for compressing video images, the L64720 motion-estimation processor uses an array of 32 ALUs (right side) to detect relative motion between successive video frames. Static RAM (left and top) functions as input buffers to store the data block and search window, and to store computational results. Circuitry between the memory and ALU array provide control.

is expected to become an ISO (International Standards Organization) standard.

The functional partitioning scheme also supplies access to the bus architectures to allow further design differentiation. For example, although the image-compression algorithms are embedded in firmware, users can apply proprietary algorithms by connecting memory devices and additional logic to the buses. Using the building blocks, designers can construct an image-compression subsystem for low-volume production, with an option for higher-level integration in the future. Considering the downward cost trend of such I/O devices as video monitors, cameras, scanners, and facsimile machines, the chip set is more in stride with target system costs than, say, a $50,000 video-codec solution for data compression.

All chips are used to compress images of full-motion video *(Fig. 2a)*. The 64760 interframe processor's input signal is rasterized image data, coming from a scanner, video camera, or frame memory. Depending on the data source, users must insert logic between the 64760 and the signal source to implement the required signal conversion (for example, a video camera's analog signal would require analog-to-digital conversion).

For H.261 operation, the 64760 reformats the input image data into block form for subsequent processing by other chip-set members. Image data (luminance and chrominance) is formatted in 8-by-8 data blocks, with each block containing 8-by-8 pixels and each pixel defined by 8 bits. The 64760 sends this data in raster-scanned order to the L64720 motion-estimation processor, which generates a motion vector for each block. This is done by searching corresponding blocks in the current and previous frames for translational differences. As a result, once the initial frame is stored in memory, ensuing frames can be formed just by adding translational differences to the previous frame.

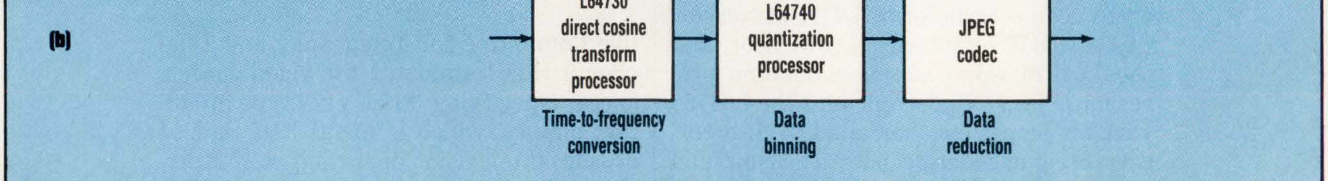
The L64730 DCT is a time-to-frequency converter that contributes to the image-compression process by changing the 64760's time-domain, motion-compensated output to the frequency domain. The DCT processor computes both the forward and inverse DCT over 8-by-8-bit data blocks, and can have up to 12-bit data precision at the input and output data terminals. Depending on a control pin's logic level, the device can also round off the output to 9 or 12 bits. In effect, this conversion changes the average value of a pixel block into a gray scale with a wide range of pixel values. Because the human eye is insensitive to minute changes in hue and brightness, many of these values can be stripped out without noticeable picture-quality degradation.

A "binning" operation on the DCT's output, performed by the L64740 quantization processor, sorts DCT coefficients according to value. Quantization step size, and thus compression ratio, is user-selectable. Although the result is an approximation of the image, the lost precision at the receiving end can't be seen.

The L64750 coder performs additional data reduction by encoding each quantized DCT coefficient in one cycle, using short code words for the predominant pixel block values and longer code words for lesser-used values. Combined with motion compensation, the overall result is a minimum number of bits needed to define a series of video frames.

Output data is packed into 24-bit words and multiplexed and coded according to the proposed CCITT H.261 standard. The compressed signal can now be transmitted to an I/O device, such as a video telephone or teleconferencing system.

For I/O devices lacking error-correction capability, the L64715 error-correcting encoder-decoder can follow the L64750. Containing both an encoder and decoder for full-duplex operation, the device processes blocks of 512 bits and corrects up to two errors per code word. This is acceptable for image-compression applications. The 64715 also performs



2. A VIDEO CODEC for broadcast-quality images requires all or part of LSI Logic's chip family (a). The optional L64715 error-correcting device isn't needed for communication with an I/O device having error-correcting capability. Still-image encoding is implemented with only the DCT processor and the quantization processor (b). JPEG encoding can be implemented with standard MSI devices. Signal paths are reversed to receive encoded still and motion pictures in the decoding mode. The L64760 and L64720 aren't required to decode video signals.

IMAGE-COMPRESSION CHIPSET

framing and synchronizing functions, and has a full-duplex operation at 20 Mbits/s.

Encoding still images according to the JPEG standard requires only two of the chips *(Fig. 2b)*. Unlike full-motion video, which requires real-time image reconstruction, JPEG applications use only the DCT and quantization processors and a JPEG encoder. At the present time, LSI Logic doesn't supply a JPEG encoder, but the company plans to do so in the near future. Meanwhile, this function can be provided by several medium-scale integration (MSI) parts. In both JPEG and H.261 designs, image data is decoded by having the processor chips perform the same functions in the reverse order.

The most complex member and a key element of the chip set is the L64720 motion-estimation processor *(Fig. 1 again)*. To detect relative motion between data blocks in two video frames, the chip performs intensive computations using a selectable data block (16-by-16 or 8-by-8) and search-window size (32-by-32 or 16-by-16). It can process a 352-by-288-pixel image at a 30-MHz frame rate with a 16-by-16 data-block size, and broadcast-quality images (600-by-480 pixel) at the same frame rate with an 8-by-8 data-block size. As with the DCT, multiple devices can be used to increase search-window size and performance. The main-memory access-time requirements for computing N^2 errors for an N-×-N data-block size ranges from 229 cycles for $N = 8$ at 40 MHz, to 2237 cycles for $N = 16$ at 30 MHz.□

PRICE AND AVAILABILTY

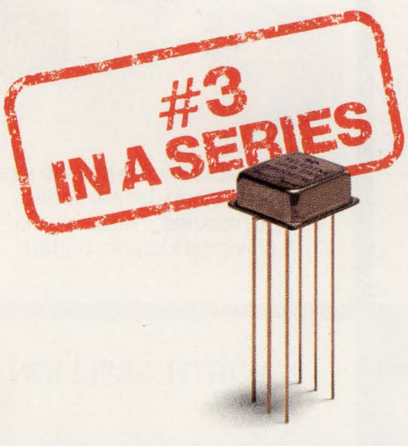
Available now in plastic packages, unit prices for 100-lot quantities are $93.50 for the L64715, $137.50 for the L64720 and L64730, and $151.25 for the L64740. The L64750 and L64760 will be available in November.

LSI Logic Corp., 1525 McCarthy Blvd., Milpitas, CA 95035; Simon Dolan, (408) 433-8000. CIRCLE 512

HOW VALUABLE?	CIRCLE
HIGHLY	518
MODERATELY	519
SLIGHTLY	520

S O L I D S T A T E R E L A Y

Our FB Series military solid-state relay features high speed and low off-state leakage.



ACTUAL SIZE

Here's what you get:

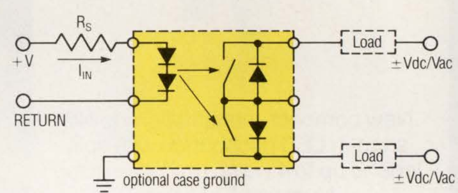
- Availability to pending DESC drawing 89116 with screening to "W" and "Y" levels of MIL-R-28750.
- High-voltage output
- Very-low leakage current (200 nA)
- DC or bi-directional power FET output (see wiring diagrams)
- Ideal for ATE applications
- Optical isolation
- Fast switching speed
- Adjustable turn-on times
- Low profile 6-pin mini-DIP
- Cost efficiency

Review the electrical characteristics below and call us for immediate application assistance.*

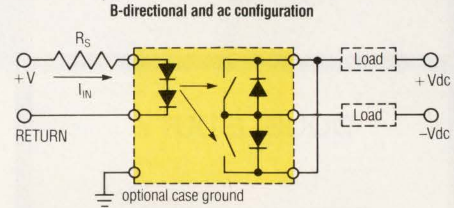
INPUT ELECTRICAL CHARACTERISTICS (–55° to +105° unless otherwise noted)			
	Min	**Max**	**Units**
Continuous Input Current (I_{IN})	10	50	mA_{DC}
Input Current (Guaranteed On)	10		mA_{DC}
Input Current (Guaranteed Off)		100	μA_{DC}
Input Voltage Drop at (I_{IN}) = 25mA		3.25	V_{DC}

OUTPUT ELECTRICAL CHARACTERISTICS (–55° to +105° unless otherwise noted)				
Part Number	**FB00CD**	**FB00FC**	**FB00KB**	**Units**
Bidirectional Load Current (I_{LOAD})	±1.0	±0.50	±0.25	A_{DC}/A_{PK}
DC Load Current (I_{LOAD})	2.0	1.0	0.5	A_{DC}
Bidirectional Load Voltage (V_{LOAD})	±80	±180	±350	V_{DC}/V_{PK}
DC Load Voltage (V_{LOAD})	80	180	350	V_{DC}
ON-Resistance (R_{ON}) at (I_{LOAD}) max.	0.72	1.8	12.9	Ohms
Turn-On Time (T_{ON})	800	800	500	μs
Turn-Off Time (T_{OFF})	300	600	500	μs

Notes: 1. A series resistor is required to limit continuous input current to 50mA (peak current can be higher).
2. Rated input current is 25mA for all tests.
3. Loads may be connected to any output terminal.
4. ON resistance shown is for the bidirectional configuration. The DC ON resistance is ¼ of these values.



B-directional and ac configuration



DC configuration

"CREATING THE STANDARD OF THE FUTURE"

TELEDYNE SOLID STATE
A Division of Teledyne Relays

***For immediate application assistance call 1-800-284-7007.**

Teledyne Solid State, 12525 Daphne Avenue, Hawthorne, California 90250.

CIRCLE 137

BEST OF THE '90s

NKK can show you exactly where the switch industry is headed because we're already there. We have over 917,000 different ways to improve your products' reliability and functionality — starting with the just-released break-through switch ideas on this page. Send for our free 400-page catalog.

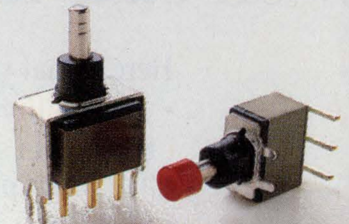
Contact
NKK Switches,
7850 E. Gelding Dr.,
Scottsdale, AZ 85260.
Phone (602) 991-0942.

nkk switches

WORLD'S SMALLEST

NKK introduces the surface mount G3T with patented STC contacts, gull-wing terminals. VPS or infrared reflow solderable.

EASY DOES IT



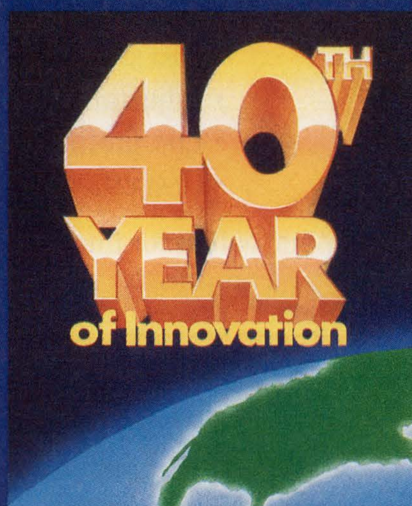
Washable M2B subminiature pushbuttons feature very-light-touch, snap-acting contacts. Straight, right angle, vertical PC terminals.

ULTRA-MINI

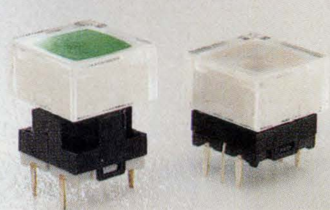
New ND switch is half the size of ordinary binary coded DIP rotaries. Washable and universal footprint pattern.

LEGENDARY

New compact, industrial-grade NB snap-in LED pushbutton with split legend up to 4 ways. Built-in resistor. Numerous options.



WORTH A MILLION



Million operations from unique LED illuminated JB keypad switch. Red, green or yellow LED options.

DOUBLE DUTY

Logic-level for PCB or power rating for snap-in panel mounting, from very low-profile UB pushbuttons with full-face LED illumination.

TURNING POINT

Washable Binary Coded DIP rotary DR-A switch can be PC or panel mounted. Crisp operation. Right angle or straight terminals.

100,000 CHOICES

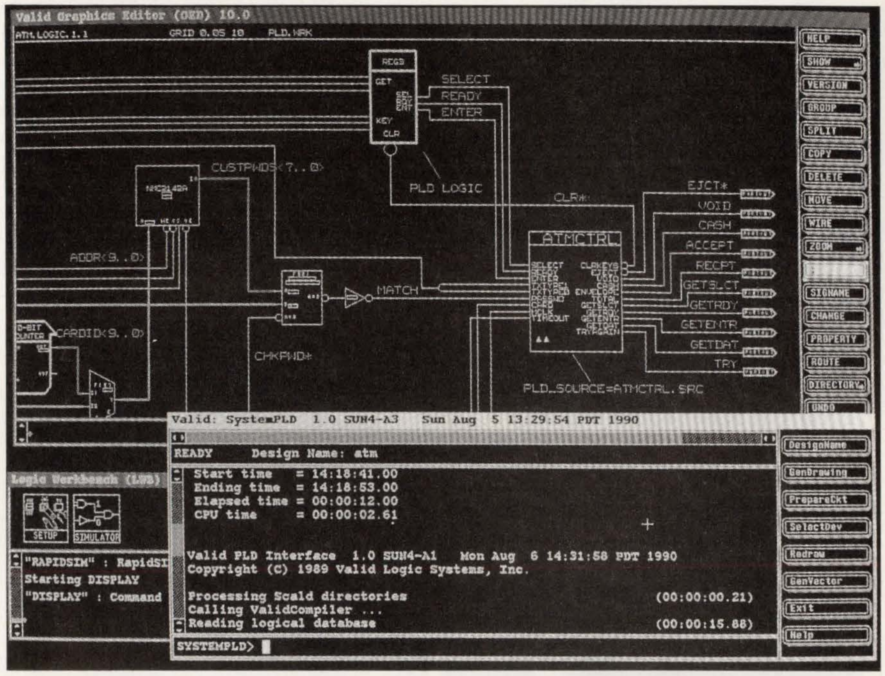
YB pushbutton yields literally 100,000+ part numbers with variations in mounting, illumination, circuitry and color.

CIRCLE 96

PLD AND FPGA TOOLS TAKE A SYSTEM-LEVEL APPROACH TO DESIGN

LISA MALINIAK

To make complex designs manageable, engineers need to take a system-level approach. Most programmable-logic design tools, however, don't facilitate system-level approaches. Two new design tools from Valid Logic Systems called SystemPLD and SystemPGA solve this problem. Using the Valid software, engineers can mix logic types throughout system schematics, perform system simulation before device selection, and automatically combine or retarget programmable logic without design-description changes. In addition, an automatic schematic redraw capability smooths the integration with physical design, packaging, and back-annotation.



The products are a result of the combined technologies of Minc Inc., Colorado Springs, Colo., and Valid Logic Systems Inc. Valid incorporated its Logic Workbench framework with Minc's synthesis capabilities.

With SystemPLD and SystemPGA, engineers choose the most efficient method for describing specific parts of their design. These methods include ValidGED schematics, hardware description languages (HDLs), waveform descriptions, state machines, truth tables, and Boolean equations. Unlike many of today's systems, these methods can be combined hierarchically in the same schematic without selecting a target device or technology.

The tools then synthesize functional simulation models. The system can be verified through simulation with Valid's RapidSim digital simulator. By simulating the programmable logic device (PLD) or field-programmable gate array (FPGA) within the target system early in the design cycle, problems can be detected and corrected with minimum impact on the design schedule. Earlier methods of design required that the engineer go back through the entire design process and re-simulate.

Designing with SystemPLD and SystemPGA is technology-independent. As a result, the design can be retargeted from one technology or vendor to another. In addition, users can migrate from PLDs to higher-density FPGAs transparently.

Device selection is simplified because users can specify such constraints as manufacturer, specific PLD type, speed, cost, power, and logic family. The engineer can include those constraints in the schematic to drive device selection and partitioning from the beginning of the design cycle. Users can also select devices manually. After part selection, the design is automatically fit into the device. For large designs that need more than one device, the tools automatically partition the design across multiple devices.

When the design is functionally correct, the logic is implemented with any of over 3000 devices in the Minc PLD and FPGA libraries. The libraries support nearly all PLD vendors and architectures, and have PGA support for Actel ACT, Altera MAX, AMD Mach, and Xilinx LCA families.

Full-timing models are synthesized once devices have been selected. Therefore, after device selection and fitting, the engineer can perform full-timing simulation. SystemPLD and SystemPGA automatically redraw the fully-annotated schematic containing the newly selected devices. After full-timing simulation, the target system with the actual devices is packaged for physical layout with Allegro, Valid's PCB layout system.

SystemPLD includes the tools for PLD logic synthesis and optimization design as well as the Minc library of devices. It is available now starting at $13,500. SystemPGA contains all the SystemPLD features, plus added capabilities and the Minc FPGA library. It is also available now, starting at $19,500. SystemPLD users can add SystemPGA functionality through an upgrade that costs $6000. Both products run on DEC, IBM, and Sun workstations.

Valid Logic Systems Inc., 2820 Orchard Pkwy., San Jose, CA 95134; (408) 432-9400. **CIRCLE 630**

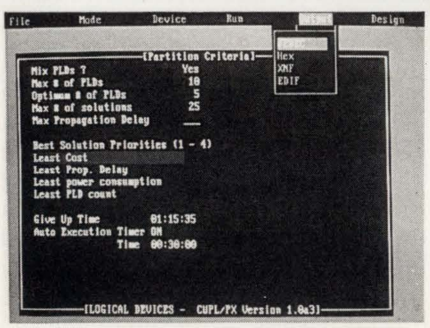
ANALOG DESIGN TOOLS INCREASE YIELDS

An analog design system called CLIO takes steps during the design phase to maximize yields in the manufacturing phase. The tools' capabilities include circuit optimization to match performance targets, yield analysis and design centering to increase manufacturing yield, schematic capture, design specification entry, circuit simulation and analysis, and results processing and presentation. Design centering involves choosing values to minimize the unwanted effects of component tolerances. CLIO is available now for $18,750 in a network configuration of four seats. It runs on HP/Apollo and Sun workstations.

Electrical Engineering Software Inc., 4675 Stevens Creek Blvd., Suite 200, Santa Clara, CA 95051; (408) 296-7563. **CIRCLE 691**

SOFTWARE SYNTHESIZES AND PARTITIONS LOGIC

PL Partition is a computer-aided-engineering tool that lets engineers synthesize and partition their programmable-logic designs into a convenient number of segments. Each segment can then be individually optimized for device cost, propagation delay, power consumption, and number and size of programmable logic devices (PLDs). The least-to-most or most-to-least feature lets engineers begin designing with the maximum or minimum number of PLDs. The split-product-terms feature gives flexibility during layout. If propagation delay is not critical for a particular signal, engineers can cross device boundaries during layout to allow for the use of smaller, less costly devices. In addition, engineers can designate the percentage of device capacity to be used to allow for future expansion and modification. Also, graphic representations of how the devices are to be connected offer engineers a preview of how the devices can be arranged on a pc board. PL Partition, which is shipping now, costs $995.



Logical Devices Inc., 1201 NW 65th Pl., Fort Lauderdale, FL 33309; (305) 974-0967 or (408) 970-0504. **CIRCLE 690**

RULES CHECKER KILLS REDUNDANT ERRORS

A hierarchical layout-rules checker called the LRC 2000 removes the redundant errors common in non-hierarchical systems. The errors are eliminated because each LRC 2000 run generates a hierarchical database that mimics the original layout database. In addition, the error-identification software works within the database hierarchy, allowing engineers to obtain immediate feedback on design errors simply by clicking on the error vectors. After each run, the software creates a log file listing the number and location of all errors. LRC 2000 runs on most 80386- and 80486-based computers, and on Apollo, Sony, and Sun workstations. It is shipping now for $20,000.

Integrated Silicon Systems Inc., P.O. Box 13665, Research Triangle Park, NC 27709; (919) 361-5814. **CIRCLE 692**

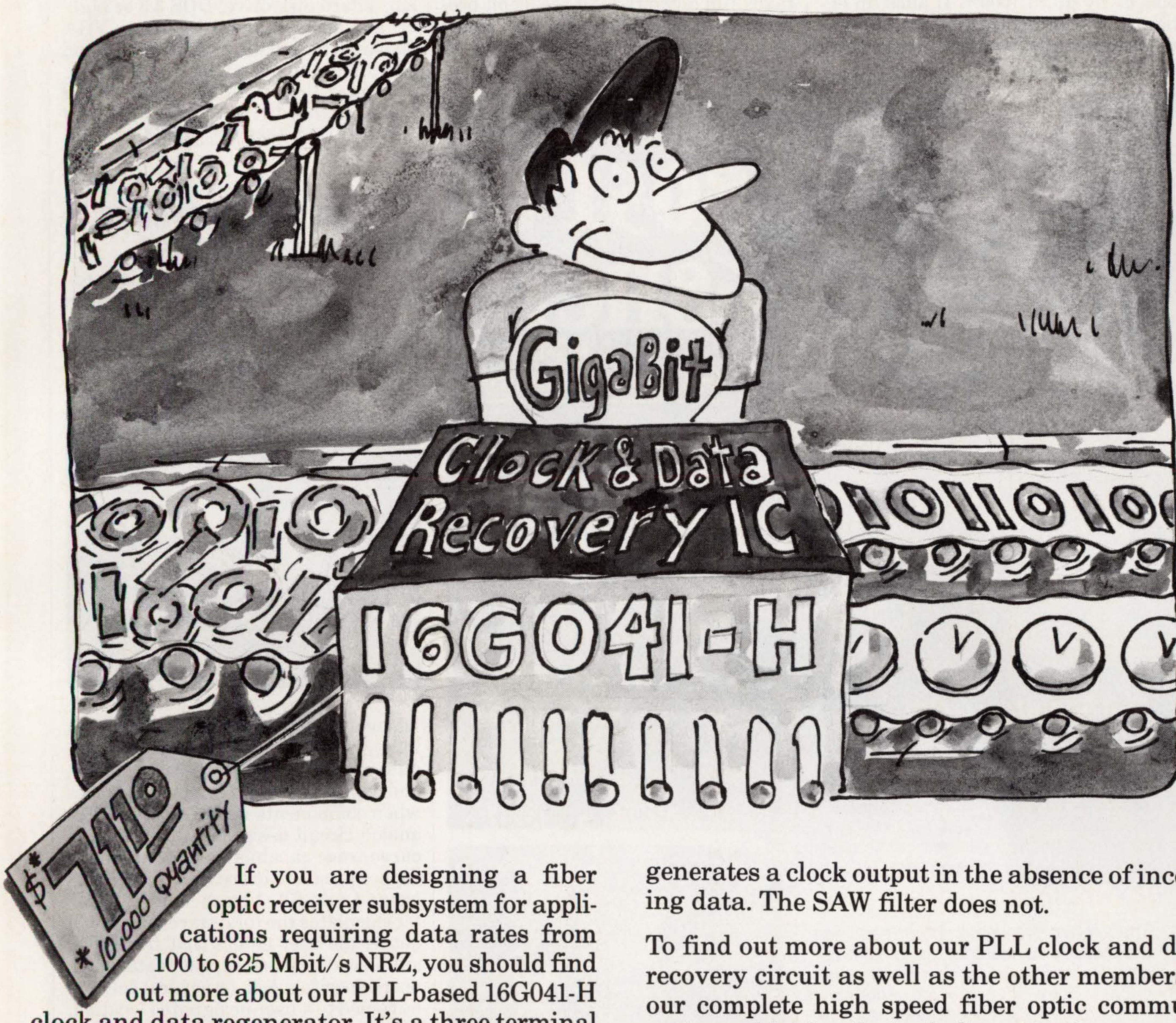
TIMING SOFTWARE SAVES SIGNAL INTEGRITY

SigDelay is a new signal-integrity tool from Valid Logic that analyzes high-speed pc-board signal transmissions for timing effects of logic transitions. With SigDelay, engineers can identify and correct high-speed timing problems before the prototype stage. It works with Valid's Signal Noise Analysis tool, which lets users analyze many different high-speed board characteristics. For signal-delay analysis, SigDelay uses the transmission-line simulation results provided by Signal Noise Analysis and applies heuristics to analyze the speed and smoothness of the signal. It then verifies length and delay constraints on the signal, and extracts the minimum and maximum pin-to-pin wire delay data for post-layout timing simulation. SigDelay will be available in January on DEC, IBM, and Sun workstations. Depending on configuration, it will cost between $12,500 and $50,000.

Valid Logic Systems Inc., 2820 Orchard Pkwy., San Jose, CA 95134; (408) 432-9400. **CIRCLE 693**

From OC-3 to OC-12...

Regenerate your SONET signals with our PLL clock and data recovery IC.



If you are designing a fiber optic receiver subsystem for applications requiring data rates from 100 to 625 Mbit/s NRZ, you should find out more about our PLL-based 16G041-H clock and data regenerator. It's a three terminal (data in, clock and data out) device in a compact 1.25 inch x 1.25 inch flatpack package.

The 16G041-H synchronizes an internal VCO directly to an incoming data stream and simultaneously retimes and regenerates the data, unlike SAW filter clock recovery circuits which first filter the clock signal from incoming data and then retime it. Moreover, the 16G041-H generates a clock output in the absence of incoming data. The SAW filter does not.

To find out more about our PLL clock and data recovery circuit as well as the other members of our complete high speed fiber optic communications chip family including 16x16 crosspoint switch, limiting amplifier, transimpedance amplifiers, laser diode driver, LED driver, MUX and DEMUX, call us today. United States and Canada: (805) 499-0610, FAX (805) 499-2751; Europe: GIGA, at +45 4343 1588, FAX +45 4343 5967.

GBL GigaBit Logic

CIRCLE 163 FOR MORE INFORMATION
CIRCLE 207 FOR REPRESENTATIVE CONTACT

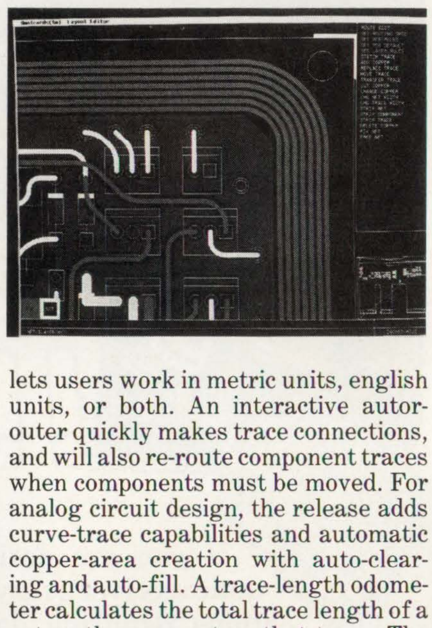
SIMPLIFY AND SPEED UP AUTOCAD 386

Soft Engine/386 is a display-list software driver that's used with AutoCAD 386. The software increases displays speeds by up to 1000%. It adds an enhanced user interface that makes AutoCAD zooms and pans easier to execute and avoids unnecessary regenerations. It also allows the user to choose between using this direct interface or using AutoCAD's own display commands. By running in the 80386 processor's protected mode, Soft Engine/386 takes full advantage of the 32-bit processor's power. AutoCAD's virtual-memory manager is effectively utilized by Soft Engine/386 so that extended memory is maximized. System requirements include AutoCAD 386, an 80386SX- or higher-based system with math coprocessor, a minimum of 2 Mbytes of RAM (4 Mbytes recommended), a hard disk drive, DOS 3.3 or higher, and an EGA, VGA, or super VGA display. The software sells for $295 and is available immediately.

Vibrant Graphics Ltd., 10622 Burnet Rd., Austin, TX 78758; (800) 937-1711 or (512) 832-1711. **CIRCLE 686**

AUTOROUTER PERFORMS SUBMICRON LAYOUTS

The newest release of the Omnicards design system from Task Technologies will layout analog and digital circuits to submicron resolution. Omnicards Release 4.2 incorporates many enhancements, including a 32-bit database that



lets users work in metric units, english units, or both. An interactive autorouter quickly makes trace connections, and will also re-route component traces when components must be moved. For analog circuit design, the release adds curve-trace capabilities and automatic copper-area creation with auto-clearing and auto-fill. A trace-length odometer calculates the total trace length of a net as the user enters that trace. The automatic step-and-repeat feature lets users specify a cell, or several cells, to be copied to a user-designated location. The copied cells maintain proper electrical connectivity data for back annotation. The complete Omnicards design system includes a schematic editor, a 3000-part library, interactive placement and routing, and outputs for manufacturing. Omnicards 4.2 runs on HP/Apollo and Sun workstations, and is shipping now. A complete system costs $24,000. The design software without the router costs $12,000.

Task Technologies Inc., 6 North Main St., Suite 235, Fairport, NY 14450; (716) 377-1060. **CIRCLE 687**

WAVEFORM GENERATOR BOASTS 16-BIT RESOLUTION

With its 16-bit resolution and 2-MHz sampling rate, the model 2201A arbitrary waveform generator is well-suited to high-precision, low-frequency test applications. The unit comes with interactive waveform creation and editing software that does'nt require an external PC.

Each of the three phase-coherent outputs has 64 kwords of battery-

backed static RAM for waveform memory. In addition, users can store setup and waveform data on a 32-kbyte battery-backed static RAM card that plugs into the front panel. When the outputs are used independently, phase between them can be programmed with a resolution of 0.0055 deg.

The 2201A includes a pseudo-random noise generator with a 150-kHz bandwidth. Its output can be used separately or displayed on channel one. Operating modes include continuous, triggered, gated, toggled, burst, hold, step, and return-to-start. The unit produces standard sine, square, triangle, and ramp waveforms. Typical sinewave total harmonic distortion at 1 kHz is –86 dB. IEEE-488.2 and RS-232-C interfaces are standard.

A 2-line by 40-character backlit LCD screen displays the setup parameters, which can be entered or changed The model 2201A costs $9985 and is available immediately.

***Pragmatic Instruments Inc., 7313 Carroll Rd.,** San Diego, CA 92121-2319; (619) 271-6770.* **CIRCLE 688**

■ *JOHN NOVELLINO*

PACKAGE GENERATES COMPLEX MODULATION

The HP 8791 Model 100 precision signal generator is a software package that provides an interactive work screen for the HP 8791 frequency-agile signal simulator. The package lets users create precise and complex signals with amplitude modulation (to 20 MHz), frequency modulation (to 20-MHz deviation), phase modulation (to 20-MHz rates), or with frequency-hop speeds of less than 250 ns. All modulations can be used simultaneously, along with other user-defined formats. The HP 8791 covers 10 MHz to 3 GHz with upconverters available to 40 GHz. The HP 8791 Model 100 costs $6000 and is available 4 to 6 weeks after receipt of an order.

Hewlett-Packard Co., (800) 752-0900. **CIRCLE 689**

BROOKTREE'S IMAGE TECHNOLOGIES

Capture iT

Change iT

Capture an image, manipulate it, transmit it, display it—and do it all with Brooktree's Image Technologies. They'll give your system a visual edge in competitive markets.

In fact, Image Technologies can be the key differentiator in today's look-a-like world. At Brooktree, we're dedicated to creating the highly integrated devices designers need to set their systems apart with exciting imaging and graphics capabilities.

IMAGE ACQUISITION

Image Acquisition starts with our Bt251 Gray-Scale or Bt253 Color Image Digitizer chips. They're the easy, economical way to add image capture to your system, with flexible architectures and standard MPU interfaces.

And they link up to our new Bt261 30 MHz Line Lock Controller. It will change the way you bring video images into your system. It's flexible and fully programmable.

Program it to strip horizontal and vertical sync information from any incoming video signal it encounters. Program its sync noise gating to cope with noisy signals and to enable locking to horizontal sync.

In fact, you won't find a more flexible solution to the timing control section of your design. Or a better way to assure your Image Acquisition system is programmed for success.

IMAGE MANIPULATION

Once you capture an image, change it.

That's easy with our Bt281 real-time Color Space Converter/Color Corrector chip. It's programmable and lets you convert from any color space to any other, including YIQ, YUV, RGB and Y, R-Y, B-Y, while capturing or displaying the image.

So now you can optimize the color space of your frame buffer for image processing independent of the video signal you're digitizing and the CRT's RGB needs. The Bt281 handles everything.

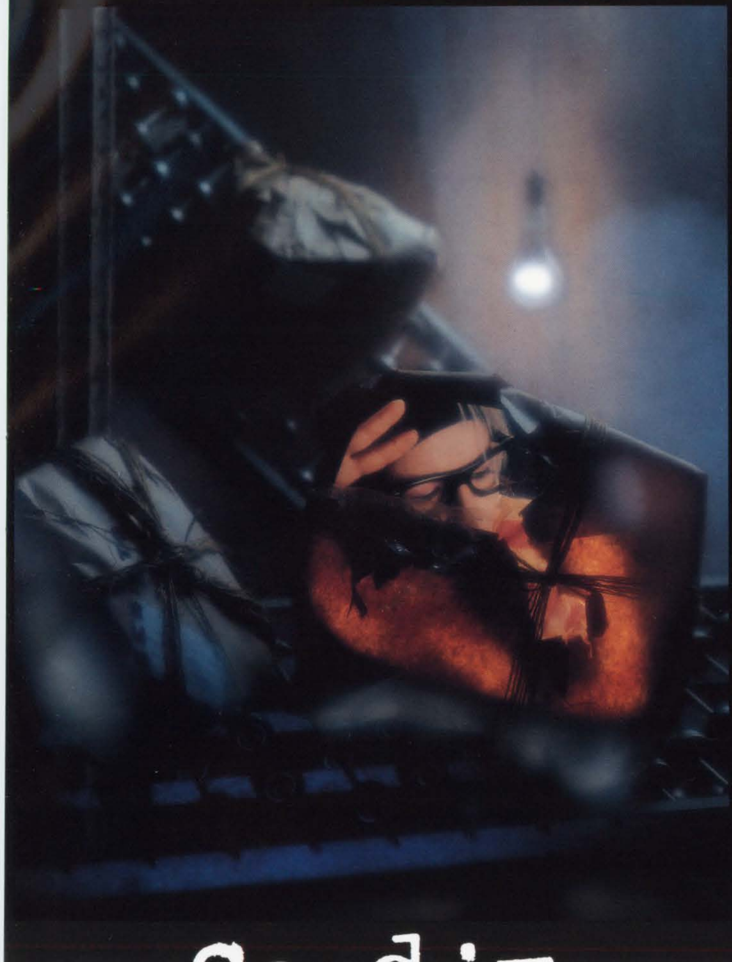
Since the Bt281 has programmable matrix coefficients and input look-up RAMs you can also use it for gamma correction, color correction or other image restoration techniques.

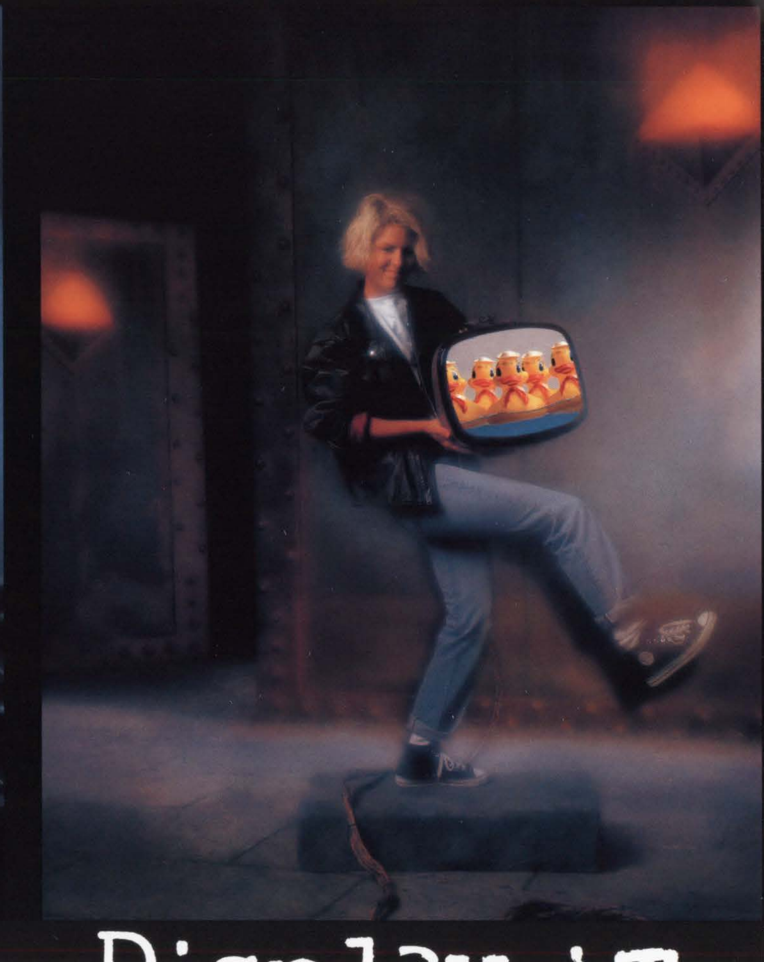
And if you think that's hot, you should see the Image Manipulation chips we'll be introducing this winter. Here's a hint: It will scale new heights.

IMAGE TRANSMISSION

How can you send your image from here to there? Digitally? In real time?

Enter two more pieces of Brooktree's Image Technologies story: The Bt291 and Bt294 VideoNet™ point-to-point Video Interfaces.





Send it Display it

Simply put, the Bt291 and Bt294 let you ship and receive live color digital video using an 8-bit interface.

Which means you can replace about a square foot of board real estate with two highly integrated devices. And take the rest of the week off.

The two devices have, respectively, input or output look-up table RAMs to simplify the interface to the frame buffer and to add or remove gamma correction and scale signal levels.

So if you're working with CCIR601, SMPTE RP125, EBU 3246-E or other digital video standards, we've done our parts. You take it from here.

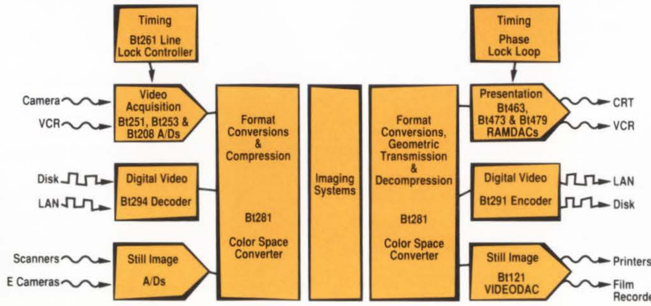


IMAGE PRESENTATION

When it comes to display technology, our true colors really shine. We invented RAMDACs. We understand the special needs of graphics systems designers. And we've never stopped innovating.

A perfect example is our Bt473, designed specifically for VGA true-color graphics. It has three 256x8 color look-up tables with 8-bit video D/A converters to support 24-bit true-color operation. And it can also support 8-bit pseudo-color, 8-bit true-color and 15-bit true-color operations. That makes it a perfect match for the Bt253 supporting the same formats.

Now our new TrueVu™ RAMDAC, the Bt463 is what's hot for designers of next-generation workstations eager to add windows capability, and delighted to do virtually everything with a single device. The Bt463 is the first monolithic true-color RAMDAC. That means it supports multiple display modes—both True Color and Pseudo Color—simultaneously. And with multiple windows, you get multiple colormaps, avoiding conflicts. Bt463 supports multiple plane depth, too, so a window can be 24, 16, 12 or 8 planes deep. And for a little frosting on the cake, it's flexible and easy to design in.

Dive into Image Technologies with Brooktree. We've got the growing family of highly integrated chips you need to handle graphics and imaging requirements in leading edge systems. Check these specs to see how easy we make it to capture, manipulate, transmit and display really neat visual stuff. Or call 1-800-VIDEO IC for complete product details.

Get With it

ACQUISITION

Bt208: 8-Bit Flash A/D Converter, 18 MSPS, External Zero and Clamp Control, On-Chip Voltage Reference, Overflow Output, No Video Amplifier Required, 28-Pin PLCC or 24-Pin DIP Package.

Bt251: 8-Bit Single Channel Image Digitizer, 18 MSPS, 4:1 Multiplexed Video Inputs, 256X8 Look-up Table RAM, MPU Adjustable Gain and Offset, Sync Detection, No Video Amplifier Required, 44-Pin PLCC Package.

Bt253: 8-Bit Triple Channel Image Digitizer, 18 MSPS, 2:1 Multiplexed Video Inputs, Output Format Logic, MPU Adjustable Gain and Offset, Sync Detection, No Video Amplifier Required, 84-Pin PLCC Package.

Bt261: HSYNC Line Lock Controller, 30 MHz Pixel Clock Generation, MPU Programmable Video Timing, Programmable Noise Gating, Generate HSYNC, Recovers VSYNC and FIELD, External VCO or High Speed Crystal Oscillator Clock Generation, 28-Pin PLCC Package.

MANIPULATION

Bt281: Color Space Converter, Three 256X8 Input Look-up Table, Programmable Matrix Coefficients, Optional Input Interpolation/Output Decimation, Standard MPU Interface, 36 MHz, 84-Pin Package.

TRANSMISSION

Bt291: RGB to CCIR 601/SMPTE RP125 Encoder, RGB Input Look-up Tables, RGB to YCrCb Conversion, Flexible Digital Filtering of YCrCb, 16-Bit YCrCb I/O Bus, Ancillary Input Port, Handles Video Timing Control, 100-Pin PLCC Package.

Bt294: YCrCb to CCIR 601/SMPTE RP125 Decoder, Handles Video Timing Recovery, Ancillary Output Port, Error Checking, 16-Bit YCrCb I/O Bus, YCrCb to RGB Output Look-up Tables, 100-Pin PLCC Package.

PRESENTATION

Bt463: TrueVu RAMDAC, 4:1, 2:1 MUX's, Switch on a Pixel Basis Between True Color and Pseudo Color of Multiple Plane Depths with Multiple Colormaps, Two 8 Plane Overlay Cursors, Variable Palette Size, Reconfigurable Pixel Port, Advanced Diagnostics including JTAG Port, 170, 135 and 110 MHz Operation, 169-Pin PGA.

Bt473: True-Color RAMDAC VGA Compatible, Compatible with Bt253 Output Formats—24-Bit, 15-Bit and 8-Bit True-Color, 6/8-Bit Pseudo-Color, Programmable Setup (0 or 7.5 IRE), Internal/External Voltage Reference, RS-343A/RS-170 Compatible Outputs, 80, 66, 50 and 35 MHz Operation, 68-Pin PLCC Package.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
1-800-VIDEO IC. FAX 1-619-452-7294

Brooktree®

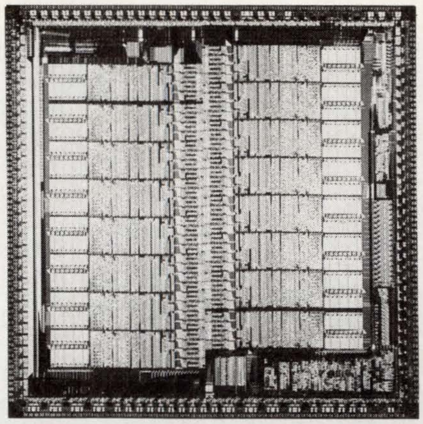
FIR FILTERS AND DIRECT DIGITAL SYNTHESIZERS TACKLE TOUGH APPLICATIONS

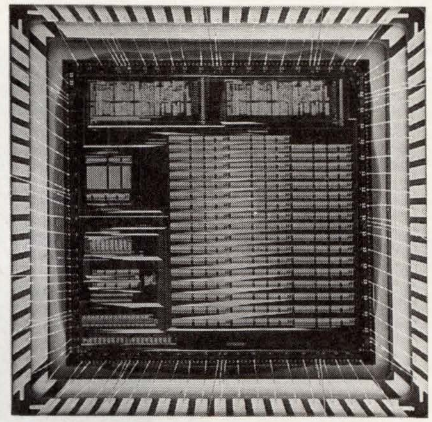
DAVE BURSKY

Aimed at demanding applications such as digital receivers for sonar, radar and electronic warfare, as well as secure communications systems, digital filter chips and an amplitude-and-phase-modulator chip operate at sampling rates of up to 20 MHz. The Plessey PDSP16256 is a programmable, variable-length finite-impulse-response filter that packs 16 16-by-12-bit multiplier-accumulators on a single chip. By multicycling the chip, from 16 to 128 stages of digital filtering can be created (with sample rates of 20 MHz, a 16-stage filter is possible at 2.5 MHz, 128 stages of filtering can be done). The other chip, the PDSP16350, is a direct digital synthesizer. It's the first chip to include an on-chip I/Q splitter to obtain the in-phase and quadrature components of an analog waveform.

The FIR filter chip accepts 16-bit data and coefficient values and accumulates results with 32-bit resolution. The chips, which come in 144-lead pin-grid array packages, can be cascaded to form filters of any length, limited only by the degradation caused by accumulator overflow. Intermediate 32-bit results are passed between devices without any intermediate scaling to minimize any deterioration of the precision. Two configuration modes are possible: the chip can be set up as one long filter or as two separate filters, with half the number of taps in each. Both organizations can have independent inputs and outputs. A decimate-by-2 mode is also available. It permits the chip to apparently double the number of filter stages at a given sample rate, but at an output rate that's one-half the input rate.

Filter coefficients can be stored in an off-chip byte-wide EPROM or down-loaded from a host system. If stored in the EPROM, an auto-boot loader in the filter chip can automatically transfer up to 128 coefficients from the EPROM to the filter chip's coefficient memory.





To support algorithm development, a behavioral model of the chip is available as part of the Signal Processing Worksystem from Comdisco Inc., Foster City, CA. Plessey offers a PC-AT hosted custom-filter-design-and-coefficient-optimization package at no charge to customers.

Providing the first integrated solution to obtain accurate, digitized, sine and cosine waveforms, the PDSP16350 produces both simultaneously with 16-bit-amplitude accuracy. The signals are synthesized with a 34-bit phase accumulator, with the most-significant bits (the upper 16-bits) providing the 16 bits of phase accuracy required for the sine and cosine lookup tables. Some typical applications for the chip include numerically controlled oscillators, quadrature signal generators, am/fm or pm modulators and constellation generators.

When driven with a 20-MHz clock, the circuit can synthesize waveforms that have 10-MHz maximum frequencies with 0.001-Hz resolution. If frequency modulation is required with no discontinuities, the phase-increment value can be changed linearly on every clock cycle. Furthermore, absolute phase jumps can be made to any phase value. Dual output multipliers on the chip allow the sine and cosine waveforms to be amplitude-modulated with a 16-bit value presented at the input port. That 16-bit value can also be used by the on-chip cordic processor to generate the in-phase and quadrature components from an incoming signal. An 84-lead PGA package houses the splitter.

Additionally, an AT-compatible card developed by ERA Technology contains both the PDSP 16256 and 16350 as well as either a 12-bit, 1-MHz ADC or an 8-bit 20-MHz DAC. Plessey expects to offer the board, but its price has not yet been set.

In addition to the two application-focused DSP chips, Plessey has also developed an upgraded version of its PDSP16116 complex multiplier. The new version, the 16116A, is still housed in a 144-lead PGA but runs at double the speed—20-MHz. The chip can multiply two complex 16-bit words every 50 ns and deliver the complete 32- + 32-bit result every cycle. On the chip are four 16-by-16-bit multipliers, two 32-bit adder-subtractors, and control logic.

All chips are fabricated in CMOS and consume about 1.5, 2, and 0.5 W, respectively, for the 16256, 16350, and 16116A. The price for either the 16256 or 16350 is the same—$395 in lots of 1000, and delivery of either is from stock. The industrial-temperature grade 16116A complex multiplier sells for $439.36 in 100-unit lots and is also available from stock.

Plessey Semiconductors Corp., 1500 Green Hills Rd., Scotts Valley, CA 95066; Steve Brightfield, (408) 438-2900. **CIRCLE 684**

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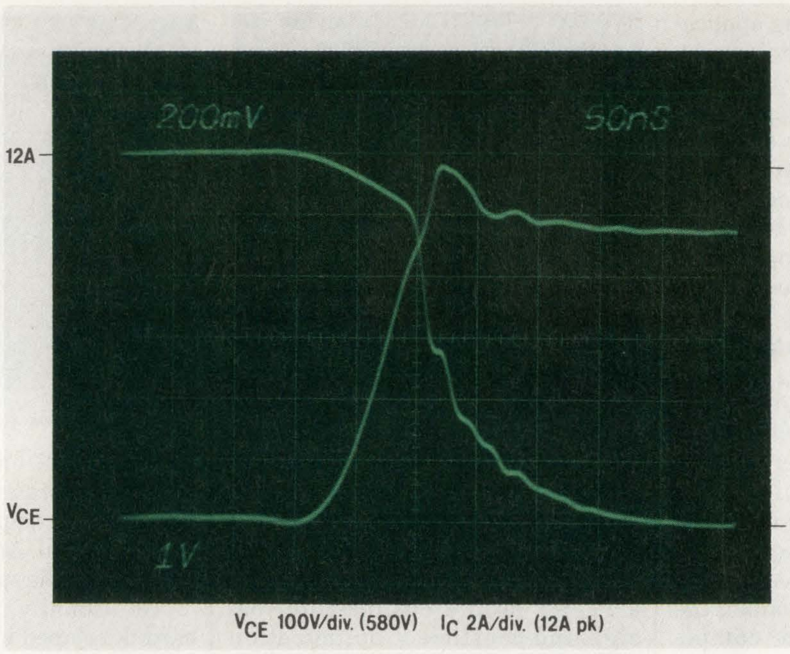
Can your IGBT do this?



Turn-off characteristics of a single-ended forward converter with 300Vdc input. International Rectifier's IRGBC30U switches 12A at 50 kHz. Easily. ***(Actual unretouched photo.)***

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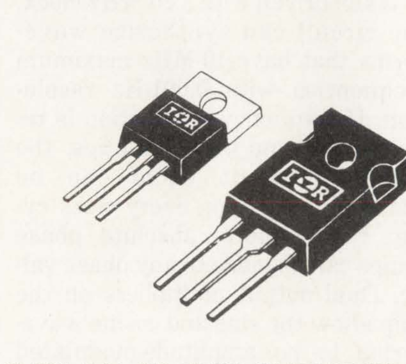

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Electronic Products Division

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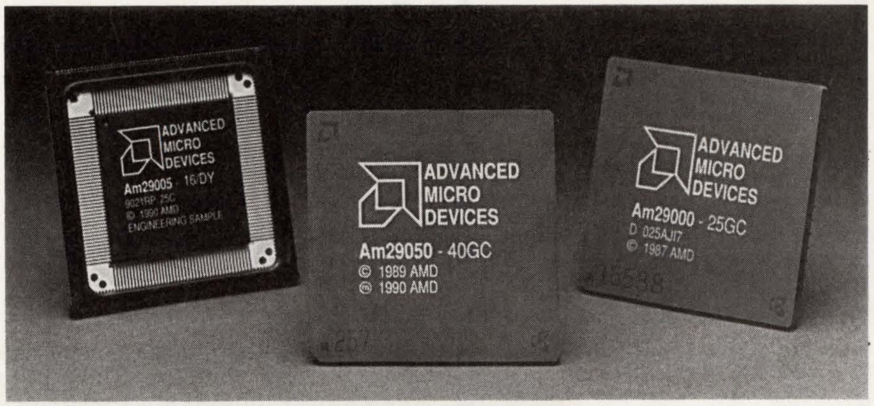
CIRCLE 215

ENHANCED RISC PROCESSOR PACKS FLOATING-POINT UNIT AND GRAPHICS COMMANDS DAVE BURSKY

With a high percentage of applications for its Am29000 RISC processor family in graphics-related subsystems, Advanced Micro Devices has developed an enhanced member of the family optimized for such compute-intensive requirements. Having a single-precision floating-point math unit on the same chip as the CPU allows the Am29050 to deliver three to four times the floating-point throughput of the previous 29000-family processors. And improvements in the integer unit boost the throughput of the integer portion of the processor by 20% over the standard 29000 RISC processor.

The 29050 delivers a sustained throughput of up to 32 MIPS and 36 MFLOPS (80 MFLOPS peak) when running at 40 MHz. In comparison, the original 29000 was rated at just 17 MIPS. Yet the 29050 still maintains pin- and code-compatibility with AMD's original 29000 processor family.

Basic improvements include a reduction of the average load latency and branch latency, and a simplification of the debug capabilities so that supervisor or user code can be debugged by hardware or software tools. Special hardware was added to permit the data load address to be issued early, thereby shortening about half of all load operations by one clock cycle. A larger branch target cache that can be configured as either a 64-entry by 4-word-deep or 128-entry by 2-word-deep array reduces the branching delay. Furthermore, to aid in imaging applications, the thrashing done by the memory-management unit on large libraries and data arrays has been reduced. Additionally, the integer multiplication time has been reduced. To reduce the thrashing, two new mapping registers augment the translation look-aside buffer to ease the processor's access to large data structures.



On-chip hardware on the 29050 speeds up 2- and 3-D window clipping and orthogonal rotations. The on-chip floating-point unit can execute single- or double-precision calculations with minimal latency. A single-precision computation requires 3 to 4 cycles. Operations can be transparently pipelined such that a new single-precision operation can be issued every cycle. The floating-point section fully supports the IEEE floating-point standard, including gradual underflow, rounding, and exception handling.

Floating-point operations possible by the new block include addition, subtraction, multiplication, division, comparisons, conversions, classifications, multiplication-accumulation, multiplication-summation, and square-root. Integer multiplications (32-bit) can also be done in the floating-point unit with a three-cycle latency before a 64-bit result is delivered.

Because the 29050 is pin-compatible with the 29000, almost all already-available development tools can be used for software and hardware development. These include the EB29K, a PC-AT add-in card containing the 25-MHz Am29000 and socket for the 29027 floating-point unit, Native C-compiler toolkit, HighC29K that runs on the EB29K to remove the 640-kbyte memory constraint of the PC, and assembly code monitor and debug software.

AMD has also created a developer's support organization called Fusion29K, which works with software and hardware developers to help define software standards, facilitate the development of high-quality tools and products, and disseminate information. Several standards already defined include a common object-file format for code portability across different development tools, a host interface for simple operating-system services, and a universal debugger interface to allow different debuggers to work with many target systems.

Supporting the 29050, JMI Software Consultants, Inc., Spring House, Penn., has enhanced and qualified its C Executive operating systems for the new processor. The software provides a real-time multitasking operating system for embedded control applications. Optional additions to the new version of the C Executive include CE-DOSFILE, a file system that replicates the DOS 8086 file structure on external media, and CE-View, a system debugger.

Samples of the Am29050 will be housed in 169-lead ceramic pin-grid-array packages. The 20-MHz version sells for $255 in 1000-unit quantities; the 40-MHz version for $410 in similar quantities. Intermediate 25- and 33-MHz grades will also be available. Samples will be available in the mid fourth quarter.

Advanced Micro Devices Inc., 5204 E. Ben White Blvd., Austin, TX 78741; Subodh Toprani, (512) 385-8542. **CIRCLE 685**

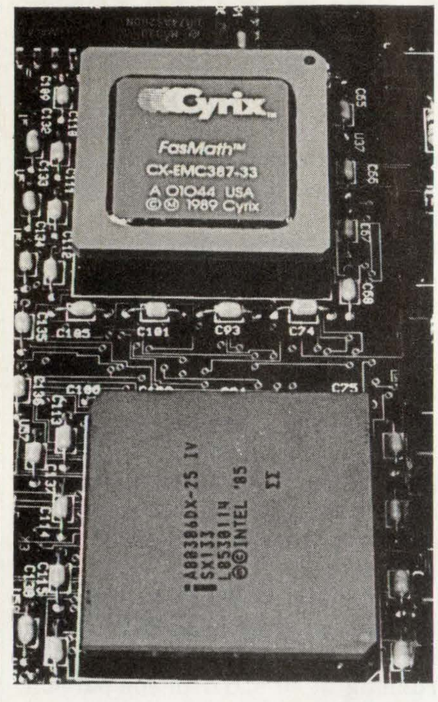
80387-COMPATIBLE COPROCESSOR PUMPS OUT FIVE TIMES THE PERFORMANCE

Delivering up to five times the application performance of the Intel 80387 coprocessor, the FasMath EMC87 math processor from Cyrix Corp., works with all 80386/387 programs without modification and guarantees fully-compatible numeric results. The chip fits in the standard 121-pin extended math coprocessor (EMC) socket found in most 386-based PCs.

Applications written to maximize the potential of the EMC87 are simplified using various programming and application tools serving the CAD market. These include Intusoft's Spice and Evolution Computing's FastCAD 3D.

The performance improvements result from implementing its floating-point primitive operations in hardware and by using proprietary algorithms for computing math functions. This lets the chip perform floating-point operations in fewer clock cycles than traditional coprocessors.

The processor implements a full extended double-precision IEEE-754-1985 architecture with parallel adder, multiplier, and exponent units. Also, the EMC87 automatically selects one of the two interface modes in response to the instruction being executed. The EMC87 either emulates 80387 style execution, or, for maximum speed, executes in EMC mode using its parallel command-data interface. The chip's 1.0-µm gate length, double-layer metal process permit clock rates of 20, 25, and 33 MHz. Electrostatic-discharge protection and latch-up-prevention circuits are built into the chip's 121-pin grid-array package.



Prices for 20-, 25-, and 33-MHz parts are $774, $865, and $994, respectively, and all are available now. The prices include a reference and installation manual and a utility disk containing test programs, demos, and utilities for the programmer to assist in tuning applications using the advanced parallel command-data interface.

Cyrix Corp., 1850 N. Greenville 184, Richardson, TX 75081; (214) 234-8387. **CIRCLE 695**

■ *RICHARD NASS*

CMOS PLDS RUN AT 80 MHZ, CONSUME LITTLE

Designed to balance the demands of two contradictory specifications—low power and high speed—the 85C224 and 85C060 programmable logic devices can operate at clock frequencies as high as 80- and 66-MHz, respectively. In addition, they consume only one quarter the power of their closest bipolar counterparts.

The 85C224 is a 24-pin PLD with t_{pd}'s of 10 ns, maximum. It has eight programmable macrocells and up to 22 inputs (14 dedicated and 8 programmable as inputs or outputs). When running at 25 MHz, the chip consumes 35 mA from its 5-V supply.

The 85C060 is a pin-compatible upgrade of Intel's previously available 24-pin 5C060, which was an alternate source to the EP600 from Altera Corp. The new chip has t_{pd}'s of 12 ns, maximum, 16 I/O macrocells, amd draws a supply current of 80 mA when running at 66 MHz.

Both the 85C224 and 85C060 PLDs are fabricated with a CMOS process and come in either reprogrammable windowed CerDIP or one-time programmable plastic packages. In quantities of 1000, the plastic-DIP versions of the 85C224 and 85C060 sell for $9.65 and $13.65, respectively.

Intel Corp., 3065 Bowers Ave., P.O. Box 58065, Santa Clara, CA 95052-8065; (408) 987-8080. **CIRCLE 696**

CIRCLE 82

IC SAMPLE-AND-HOLD AMPLIFIER GRABS SIGNALS AT 100 MHZ

As computers have upped their ability to perform real-time processing on faster signals, the demand for fast—yet accurate—ADCs to provide their digital data has likewise grown. And the ADCs in turn demand fast and accurate sampling amplifiers of reasonable cost, size and power. To meet that latter demand, Acculin has developed the AL1210 monolithic sampling amplifier. It grabs 2-V pk-pk waveforms, to within 1, 0.1 and 0.01% accuracy, in just 8, 9 and 14 ns maximum, respectively.

While completely specified for clasic data-acquisition-type applications (nonlinearity error over temperature is a maximum of 0.03%), dynamic performance, which is more important for many of today's applications such as driving flash ADCs, is also well specified. For example, sampling a 2-V pk-pk 43.75-MHz sine wave at 100 MHz results in total harmonic distortion (THD) of -61 dB (typical) and maximum THD over temperature of -55 dB (between 8 and 9 bits). Sampling an 18.75-MHz sine wave at 50 MHz provides a typical THD of -70 dB (about 11 bits). Similarly, mximum THD over temperature runs -64dB (about 10 bits).

The chip also lends itself well to undersampling applications (sampling frequencies greater than Nyquist, or more than half the sampling rate) as its 3-dB full-power bandwidth at the on-chip hold-capacitor is a minimum of 270 MHz (over temperature), and aperture jitter similarly is just 2 ps rms. The amplifier comes in a 16-pin narrow-body plastic SOIC and draws just 40 mA from ±5-V rails. In quantities of 100, the AL1210 goes for $95 each, a price that's significantly less than that for large, power-hungry hybrids.

Acculin Inc. *Suite 204, 214 N. Main St. Natick, MA 01760; Barry Hilton (508) 650-1012.* **CIRCLE 711**

■ *FRANK GOODENOUGH*

IC OP AMPS SETTLE TO 14-BIT SPEC IN 32 NS

The CLC402 and CLC502 current-feedback op amps from Comlinear are basically designed to drive flash ADCs. However, with their minimum full-power (5-V pk-pk output) 3-dB bandwidth of 50 MHz, and guaranteed settling times to 14-bits (0.0025%) for a 2-V step of 32 ns, they're useful with virtually any wideband precision analog signal. Bandwidth (3-dB) for a 0.5-V output is 120 MHz. Reccomended closed-loop gain ranges from ±1 to ±8. Due to their current-feedback design, the CLC402 and CLC502 IC op amps feature ac performance that's virtually identical—regardless of gain. All of these specifications are over temperature and while driving a load of 250 Ω. The CLC502 op amp is similar to the CLC402 op amp except that the user can externally set the value of internal positive and negative clamp voltages that limit the output voltage when driving a flash ADC. Most such ADCs have well-defined safe, maximum and minimum, input voltages. The CLC402 AND CLC502 op amps are available in 8-pin DIPs and SOICs. In hundreds, prices start at $9.56 for the 402, and $10.45 for its cohort.

Comlinear Corp. 4800 Wheaton Dr. Fort Collins CO., Wayne Lownowski (303) 226-0500. **CIRCLE 712**

SYNTHESISE 1 HZ TO 500-MHZ WAVEFORMS

A direct digital-to-analog waveform synthesiser from Plessey Semiconductors, the SP2002, generates square, triangle and sine waves, both in-phase and quadrature, from 1 Hz to over 400 MHz, with 1-Hz resolution. The device's square-wave outputs are from logic gates, and sine and triangle outputs from a pair of 8-bit digital-to-analog converters. The inputs are 32-bit parallel digital words to set the frequency, and a clock which can be as great as 1.6 GHz. The high clock rate permits switching between frequencies in just 10 ns, about 1000 times faster than the phase-locked loops commonly used. Applications range from commercial, multi-function radio (VHF, FM, AM, SSB and OPSK) as well as cellular-radio and satellite data links to military commmunications, radar and countermeasures systems.

The quadruple outputs are ideal for carrier recovery loops in MPSK modems while the fine frequency resolution and fast switching lend it to frequency-hopping (spread-spectrum) systems. The SP2002 comes in a 68-pin grid array and goes for a mere $1,400 each in hundreds.

Plessey Semiconductors Corp., 1500 Green Hills Rd., Scotts Vally, CA; Ashi Majid (408) 438-2900. **CIRCLE 713**

PRECISION DUAL OP AMP RUNS OFF BATTERIES

Needing just 500 μA per amplifier, a dual precision op amp from Burr-Brown aims at portable/remote industrial and medical applications which must run off batteries or other limited power sources. However, with a minimum open-loop gain over temperature of 120 dB and a maximum offset voltage of 350 μV, under similar conditions, the OPA1013 gives up nothing in performance. Moreover, with its pnp input transistors, its common-mode voltage includes ground. The op amp is completely specified operating from ±15-V rails and a single 5-V supply. It can put 12 V across 2000 Ω and 3.3 V across 600 Ω (with a single 5-V supply). From 0.1 to 10 Hz, 1/f noise typically runs 0.55 μV pk-pk. While basically for dc applications, slew rate is a minimum of 0.2 V/μs. In its 8-pin DIP or TO-99 metal can, it goes for $2.30 each in 100s.

Burr-Brown Corp., P.O. Box, 11400, Tucson, AZ 85734; John Conlon (800) 548-6132. **CIRCLE 714**

ISOLATION AMP WORKS FROM -55° TO +125°C

The AD203SN is one of the first isolation amplifiers to be tested and specified over the full military temperature range of –55° to +125°C. It can tolerate up to 1500 V rms of common mode voltage. Full power bandwidth is 10 kHz, accommodating high-frequency signals from ac-excited bridge transducers. The amplifier has low 0.012% (0.025% maximum) nonlinearity. Maximum offset voltage is $\pm(5 + 25/G)$ mV (G = gain), and typical offset voltage drift is $\pm(6 + 100/G)$ μV/°C. Typical gain temperature coefficient averages 50 ppm/°C over the full temperature range. The AD203SN is housed in a plastic 2.23-by-0.83-by-0.6-in. DIP. It costs $58 in lots of 100 units and is delivered from stock.

Analog Devices Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062; (617) 461-4065. **CIRCLE 715**

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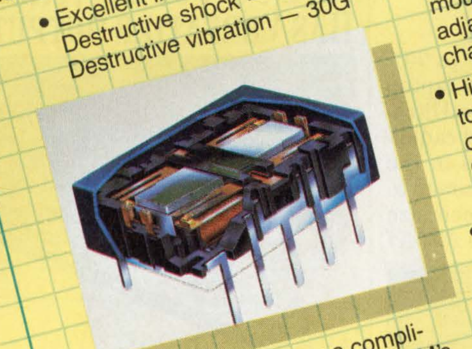

- Capable of high density board mounting without affecting the adjacent relays' operating characteristics.
- High speed performance is due to the low mass and small size of the moving components
  Operate Time: 2mSec
  Release Time: 1mSec
- Special hinge construction of the Armature block reduces friction. Consistent movement offers minimal variation in operating characteristics.

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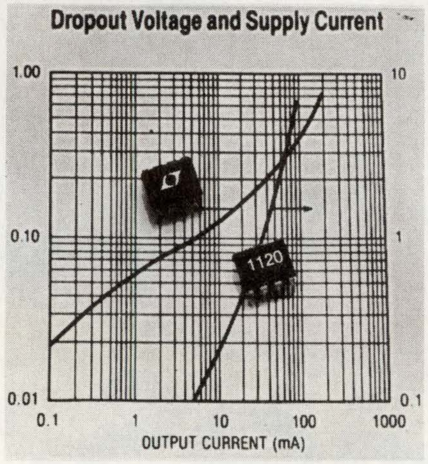
POWER LOW-DROP-OUT REGULATOR SOURCES 125 MA AT 4.5 TO 36 V

Not only can Linear Technology's LT1120 regulate up to 125 mA while operating with just 0.65 V across it (its drop-out voltage) but it also has a free-collector on the same chip that you can put feedback around and compensate, and so use as an op amp. The comparator's output handles 10 mA and the regulator's 2.5 V band-gap reference output can source and sink 2 mA. The latter feature lets it be used as a supply-splitter. One additional chip-input pin of the miniDIP lets a 5 V, logic-high turn off the regulator, for example to save battery power. Used to monitor the regulator's 4.5 to 36 V source, the comparator can turn the chip off if the input voltage gets too high or too low.



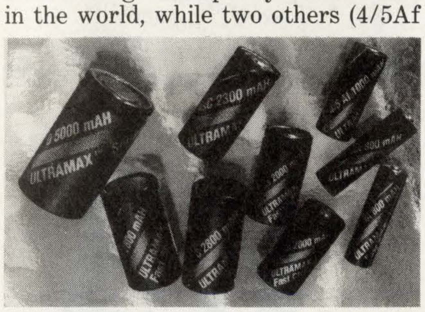
Drop-out voltage ranges from 0.65 V (maximum) while passing 125 mA to 50 mV while regulating 100 μA. Likewise, the current needed to run the IC ranges from 100 μA to 20 mA. Line and load regulation run maximums of 0.05%/V and 0.5% respectively over an input voltage range of 6 to 36 V and an output current of 100 μA to 125 mA. The LT1120 comes in 8-pin plastic DIPs and TO-5 cans. In quantities of 100, the former go for $2.40 each.

***Linear Technology Corp.**, 1630 McCarthy Blvd., Milpitas, CA 95035-7487; Bob Scott, (408) 432-1900.* CIRCLE 701

■ *FRANK GOODENOUGH*

BATTERIES FOR LAPTOPS BOAST HIGH CAPACITY

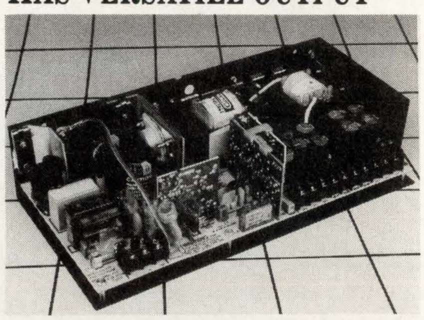
Run times of as much as 50% to 70% higher for cellular phones and laptop computers are promised by the Ultramax line of rechargeable nickel-cadmium batteries. Four of the cells in the line (AA, Cs, CsC, and C) are claimed to have the highest capacity for their size in the world, while two others (4/5Af



and D) match the highest capacities now offered. All cells, when used with proper charge-termination techniques, can accept three-to-five-hour and one-hour fast charging. Production quantities of all sizes will ship by the second quarter of 1991. Samples are available now. Call for pricing.

Gates Energy Products Inc., P.O. Box 861, Gainesville, FL 32602; (904) 462-3911. CIRCLE 702

FIVE-OUTPUT SWITCHER HAS VERSATILE OUTPUT



Measuring just 10.5-in. long, the SA200 switching-power-supply series offers users five outputs in a 200-W package. The supply lets users internally connect two outputs in either series or parallel to create new voltage or current levels. Other standard features include built-in filtering, international safety approvals, dual input-voltage selection, and overload protection. The five outputs are between +5 V and +24 V with the main output being 5 V at 20 A with 2% line and load regulation. The supply costs $207 in lots of 100. Delivery is from stock to eight weeks.

Astec America Inc., 401 Jones Rd., Oceanside, CA 92054-1216; (619) 439-4280. CIRCLE 703

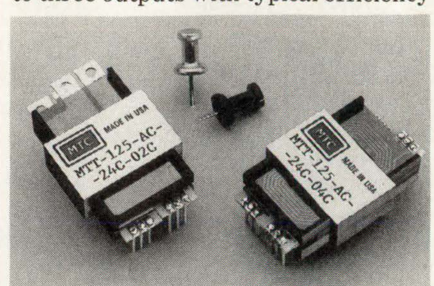
DESIGN YOUR OWN SWITCHED-CAP FILTER IC

A metal-mask programmable array allows designers to develop their own 12-pole, switched capacitor filter (SCF) ICs in a 16-pin DIP. The LMF120 lends itself to many applications, from mobile phones and anti-aliasing, to control systems and real-time audio analyzers. It can realize all common filter types: low, high, band and all-pass and notch, as well as all common responses including Butterworth, Chebyshev, Bessel and elliptic. The chip can hold the equivalent of three independent MF10 or MF100 filters in one package. Center or cutoff frequencies range from 0.1 Hz to 100 kHz, offset voltage is below 70 mV and they need 100 mW from ±5 V rails. An evaluation chip contains three 4th-order Chebyshev bandpass filters with center frequencies spaced 1/3 octave apart. Non-recoverable engineering (NRE) charges run $5000 per design, with a minimum order quantity of 5000 pieces.

National Semiconductor Corp. 2900 Semiconductor Dr., Santa Clara, CA 95052-8090; Andy Jenkins, (408) 721-2273. CIRCLE 704

PLANAR TRANSFORMER DRIVES OFF-LINE SOURCES

A high-frequency planar transformer is now available for off-line power supplies. The MTT-125-AC units are claimed to be the first of their kind to meet UL, VDE, CSA, and IEC safety standards. Standing just 0.5 in. tall, the transformer is designed for 100-kHz-to-1-MHz operation in pulse-width-modulated and resonant-topology converters. It can deliver 200 W from one to three outputs with typical efficiency



of 98% and low leakage inductance. Prototypes cost $100 each, and production lots cost $10 each in quantities of 1000. Delivery of small quantities is from stock.

Multisource Technology Corp., 393 Totten Pond Rd., Waltham, MA 02154; (617) 890-1787. CIRCLE 705

CIRCLE 131 →

QUAD HIGH-SIDE SWITCHES PASS 1 A—CONTINUOUSLY—AND 3 A PEAK

The jury is still out on whether the high-side solid-state switch will find a home outside the automobile. However the latest device in the genre has already attracted interest in applications as diverse as non-military avionics, and hotel electronic door-locks. It contains four switches, each rated at 28 V, a continuous current of 1 A, and peak currents of 3 A. The quad high-side switch comes from International Rectifier and National Semiconductor, the IR8400 and LMD18400, respectively.

Basically, these switches control dc power to small lamps, motors, solenoids and power supplies under the aegis of host processors, an activity that's becoming as common in appliances, toys, machine tools, copiers and computer peripherals as it is in cars. To meet automotive needs, these chips offer a number of features equally applicable to other applications. A circuit protects the switch from burn-out by sensing instantaneous switch voltage and current, calculating the power, and limiting the current if power exceeds 15 W. This action limits in-rush current in lamp loads raising lamp life. If the die temperature exceeds 170°C, all four switches turn off and a flag notifies the host.

A serial data port provides additional diagnostics to the host, including whether the load is open, shorted or okay. An early-warning feature tells the host when the die temperature exceeds 145°C, permitting the host to turn off some of the switches, in lieu of all four. Additionally, under- and over-voltage sensing are also provided. The switch survives 80-V transients. In its 20-pin DIP and in quantities of 100, the the IR8400 goes for $6.19 each; the LMD18400 for $6.50 each.

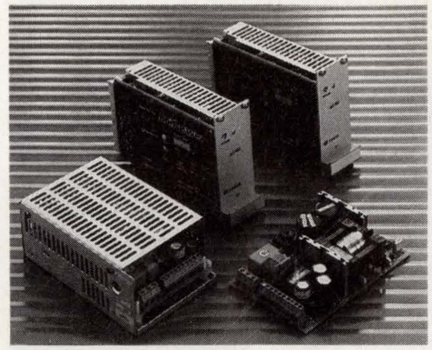
***International Rectifier Corp.**, 233 Kansas St., El Segundo CA 90245; Arnold Alderman (213) 607-8899.* CIRCLE 716

***National Semiconductor Corp.**, 2900 Semiconductor Dr. Santa Clara, CA 95052-8090; Al Kelsch (408) 721-6937.* CIRCLE 717

■ *FRANK GOODENOUGH*

SUPPLIES PERFORM CONSTANT-VOLT CHARGING

A series of 11 switching power supplies is intended for constant-voltage-charging applications in 24-V dc battery systems, such as for emergency equipment, or as a general source in 28-V systems. The PLB series comes in 19-in.



and open-frame mechanical versions. Output power is 100 W and hold-up time is 30 ms. Efficiency for the supplies is more than 87%. Two supplies can be connected in series to charge a 48-V battery system. Depending on mechanical model, pricing starts at $141 for lots of 100. Delivery is from stock.

Ericsson Components Inc., 403 International Pkwy., Suite 500, Richardson, TX 75081; (214) 669-9900. CIRCLE 720

100-V, 4-A, DMOSFET NOW HERE IN A TO-92

Now you can get 100-V power MOSFETs in a plastic TO-92 package with an on-resistance of just 0.35 Ω, while putting 10 V between the gate and source. Drain current is 4 A. From Supertex, the VN2210N3 is the first 100-V die with only 0.35 Ω on-resistance that's small enough to fit in a TO-92. The high cell density of the company's DMOS III process made possible this performance. Drive the MOSFET's gate with just 5 V—for example with a 5-V logic signal—and on-resistance is still a low 0.5 Ω. The transistor's 2.5-V gate threshold voltage, also a function of the process, insures this performance. A second device, the VN2206N3 is rated at 60 V. Applications for these transistors include driving small motors, solenoids, and lamps, as well as solid-state relays, high-voltage linear circuits such as op amps, and low-on-resistance signal (rather than power) switches. In quantities of 1000, the 100-V device goes for $0.88 each; its cohort for a penny less.

Supertex Inc., 1225 Bordeaux Dr., Sunnyvale CA; Dilip Kapur, (408)744-0100. CIRCLE 718

POWER SWITCHER NEEDS NO LOOP COMPENSATION

Now you can build a low-cost step-up, step-down or inverting, 15-W switching regulator without worrying about keeping a dominant-pole feedback loop stable. Motorola's MC34163 replaces typical PWM circuits with what's called the "fixed on-time, variable off-time, voltage-mode ripple topology". Operating in what might be called a bang-bang servo mode, somewhat analogous to a capacitor charge-pump, the chip's 3-A switch is continuously gated on by a 50-kHz clock and turned off by the feedback comparator which compares the output voltage to a stable reference. Regardles of the configureation, a typical circuit takes a small inductor (180 μH), a Schottky rectifier, a 300- to 3000-μF capacitor, and a handfull of additional resistors and capacitors. Efficiencies run 80 to 90% and line and load regulation from 0.01% to 0.1%. Features include cycle-by-cycle current limiting, thermal shutdown and a "low-output-voltage" flag. In quantities of 100, the MC34163 runs $1.59.

Motorola Semiconductor, Bipolar Analog IC Div. 7402 South Price Rd., Tempe, AZ; (602) 897-3615. CIRCLE 719

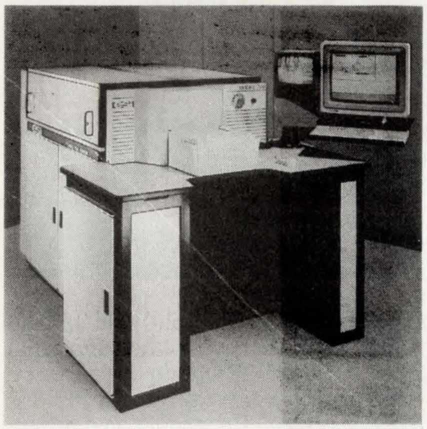
100-A, 50-V DMOSFET NOW IN A 5-PIN TO-218

By using a 5-pin, TO-218 package for a basic three-terminal power MOSFET, Harris has broken the barrier set by lead resistance and built the highest-current—100-A—lowest on-resistance—10 mΩ—power MOSFETs in a low-profile package. Two extra leads provide Kelvin connections directly to the die's drain and source bond pads. This permits internal sensing of FET voltages. Thus, FET current can be determined (and thus controlled) by measuring the voltage drop across the bond wire between die and lead (the voltage between the source lead and the source Kelvin lead). In addition, these are "logic-level" FETs that can be turned on hard with just 5 V. And they're rugged—they're rated for a single-pulse avalanche energy of 800 mJ. And like all DMOSFETs, the RFA100N05 FETs are fast, turning on and off in just 60 and 100 ns maximum, respectively. In quantities of 1000, they go for just $7.97 each.

Harris Semiconductor Corp., P.O. Box 883, Melbourne, FL 32901; 1-(800) 427-7747. CIRCLE 721

LASER TAPE-AUTOMATED BONDER QUICKLY, RELIABLY BONDS COMPLEX ICS

A faster, gentler, non-contact approach to tape-automated bonding (TAB) of complex ICs is now available in the model 7100 laser-TAB system from Electro Scientific Industries. The system bonds up to 65 leads per second and produces metal-



lurgical bonds with consistent high quality without subjecting the IC to extreme mechanical and thermal stress.

In operation, a technician aligns the die using a mouse and video monitor, positions the focused laser beam over the first lead, pulses the laser once, and moves on to the next lead. The operation is repeated until all leads are bonded. The ability to bond leads on a tight pitch especially suits the model 7100 bonder to modern ICs. With laser TAB, bond pitch is limited only by the laser-beam diameter. This is in contrast with the tool-size limitations of single-point bonders or the maximum-pressure limitations of gang bonders.

Because laser bonding is a non-contact methodology, the bond pressure is extremely low—about 2 grams/lead. In addition, die temperature is minimal at about 22°C.

Another advantage of laser TAB is the system's ability to change over from one die size to another in seconds by means of software control. In gang bonding, a thermode changeover can take up to an hour.

To meet the specific needs of laser TAB, the company developed its pseudo-pulsed Nd:YAG laser, which operates at a 1064-nm wavelength. The laser gives operators more precise control over laser energy, which means consistent repeatable bonding and flexibility for bonding different types of ICs.

Configurations of the model 7100 laser-TAB system start at $245,000. Call for system availability.

***Electro Scientific Industries Inc.**, 13900 N.W. Science Park Dr., Portland, OR 97229-5497; (503) 641-4141.* **CIRCLE 697**

■ *DAVID MALINIAK*

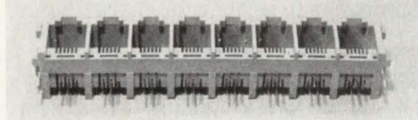
MULTILAYER PACKAGE STACKS 16 LAYERS

Cofired, multilayer ceramic modules are now available from CTS Corp. using DuPont Electronics' Green Tape technology. The substrate system combines the best features of thick-film and high-temperature cofired ceramic packaging technologies. Sixteen or more separate substrate layers can be stacked with screened conductive patterns on each layer. Also, cavities can be built so that discrete components can be recessed into the layers. The substrate material can be fired in one pass at a low 850°C. The process also makes possible higher print resolutions. Samples are available in four to six weeks after receiving customer specifications.

CTS Corp., Microelectronics Division, 1201 Cumberland Ave., West Lafayette, IN 47906; (317) 463-2565. **CIRCLE 698**

DATACOM GANG JACKS LINK EIGHT DEVICES

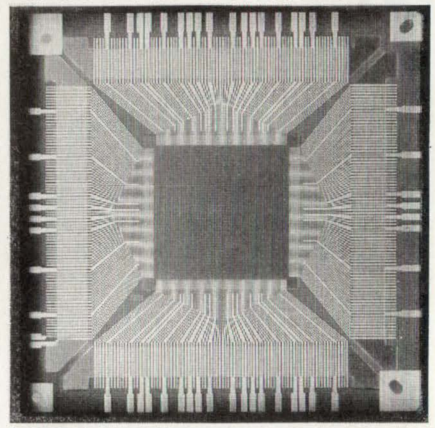
Dual-through octagon gang jacks are available in both right-angle and perpendicular versions. Triple, quadruple, and quintuple jacks are also offered.



Six position openings with up to six contacts in any combination can be specified. Metal locking brackets allow for quick, easy pc-board insertion. The contact material is phosphor-bronze with selective gold plating, and the current rating is 1.5 A. In lots of 1000, prices range from $0.85 for a dual jack to $4.52 for an octagon jack. Delivery is in six to eight weeks.

Kycon Cable & Connector Inc., 1772 Little Orchard St., San Jose, CA 95125; (408) 295-1110. **CIRCLE 699**

TWO-METAL TAB TAPE INCLUDES GROUND PLANE



The sub-300-ps rise times of today's ECL devices can be problematic, making even short tape-automated-bonding (TAB) leads look like impedance discontinuities. That adversely affects the devices' performance. But the advanced packaging requirements of high-lead-count, high-speed digital devices are taken into account by Rogers Corp.'s two-metal-layer TAB circuits. The second layer makes up a ground plane that delivers controlled impedance and reduced crosstalk right up to the die.

Rogers's advanced TAB circuits are based on a proprietary process that combines additive plating and dimensionally stable material systems. Circuits are manufactured in panel form, which makes for greater flexibility in part size and configuration.

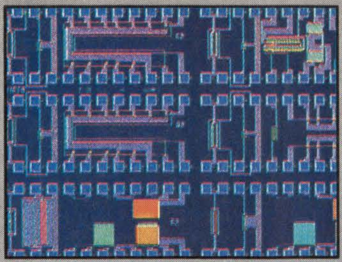
In the test area, it's becoming more critical that full or partial functional testing, as well as burn-in of the chip, be done in TAB form. This is especially true in multichip modules or tape-on-board applications. The double-metal-layer tape makes such testing possible at or close to speed.

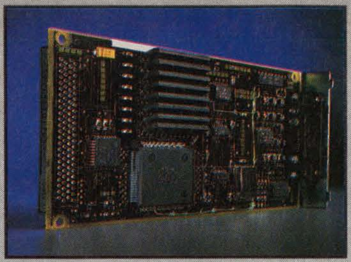
The additive process makes possible fine-line densities and high-lead-count circuits. Current production products have 360 or more leads with 0.002-in. lines and spaces. Prototype parts are in the 700-lead-plus range with lines and spaces measuring 0.0015 in.

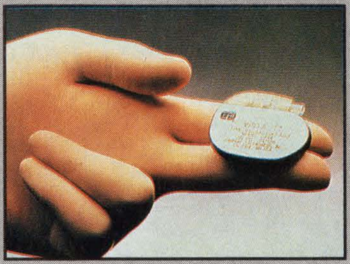
Price and availability depends on the complexity and size of the circuits.

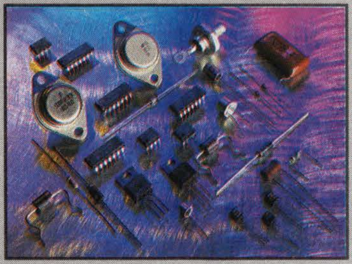
***Rogers Corp., Micro-Interconnections Div.**, 2001 W. Chandler Blvd., Chandler, AZ 85244; (602) 963-4584.* **CIRCLE 700**

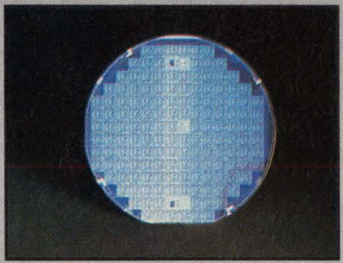
■ *DAVID MALINIAK*

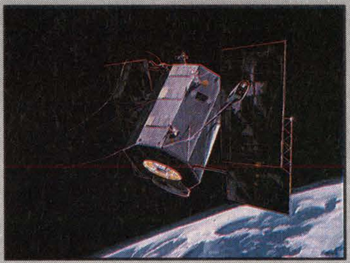












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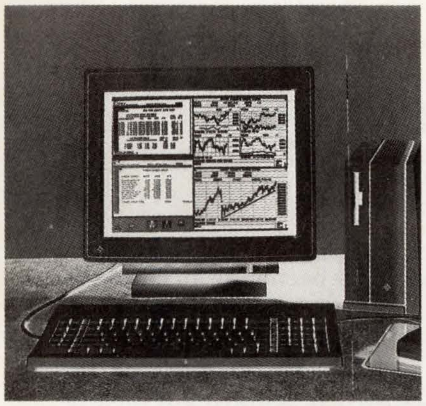
Pacemaker photo courtesy of Cardiac Pacemakers, Inc. Satellite photo courtesy of NASA. Use of PC board courtesy of Sun Microsystems, Inc.

CIRCLE 218

LOW-COST WORKSTATION PUSHES 15.8 MIPS

Coming in below $10,000, Sun Microsystems' SparcStation IPC is a compact color workstation that performs 15.8 MIPS. It comes with a 16-in. color monitor, 8 to 24 Mbytes of RAM, and two S-bus expansion slots. An Ethernet port enables the workstation to be



networked. The 9.5-by-10.25-by-4-in. package contains a 3.5-in. floppy drive and a 207-Mbyte hard drive. By incorporating Sun's Open Look graphical user interface, the IPC becomes as easy to use as a Macintosh. According to Sun, the IPC costs about half of what a PC with similar features would cost, and it runs faster, has more storage, and has a larger, higher-resolution monitor. In addition, more than 2100 software applications are now available for the Sparc architecture. These include Lotus 1-2-3, WordPerfect, FrameMaker, and Ventura Publisher. The SparcStation sells for $9995 ($8995 for the diskless version) and is available now.

Sun Microsystems Inc., 2550 Garcia Ave., Mountain View, CA 94043; (415) 960-1300. **CIRCLE 706**

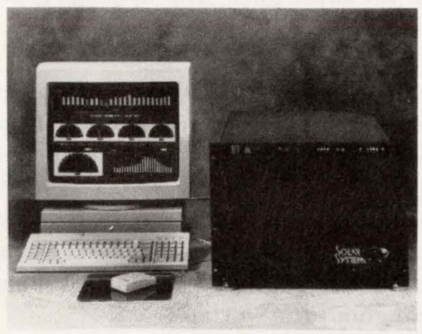
COLOR PC/AT MONITORS DISPLAY 3D IMAGES

Combining a color CRT with a proprietary liquid-crystal shutter, Tekronix Inc.'s three SGS (Stereoscopic Graphics Adapter) series monitors boast passive 3D viewing using simple, nontethered polarizing glasses. The three IBM PC/AT-compatible monitors, the 431, 630, and 635, come with an SGA card that offloads low-level graphics functions from the PC. The card supports all common 2D primitives such as move, line, polygon, and area fill. Applications that require 1280-by-1024-pixel, stereo 3D viewing include molecular modeling, mechanical CAD, cartography, photogrammetry, remote sensing, and medical imaging. Sizes of the 431, 630, and 635 (multimode) monitors are 16, 19, and 19 in., respectively. The 431 sells for $9800, the 630 for $13,300, and the 635 for $13,800. Quantity discounts are available. All the monitors come equipped with cables, polarizing glasses, SGA card, and a graphics subroutine library.

Tektronix Inc., P.O. Box 500, M/S 46-943, Beaverton, OR 97077; (503) 627-5000. **CIRCLE 707**

SUN PLATFORM LINKS TO RT VME FRONT END

The Solar System, from Matrix Corp., transparently links Sun Microsystems' Unix platforms with a real-time (RT) operating system, VxWorks, from Wind River Systems. While configured as an integrated VME target, the system is networked directly to a Sun SparcStation. By linking the system over an Ethernet network, development time is cut. Alternatively, the system can operate as a stand-alone VME



real-time target. Users can also choose from a variety of 68020/30/40 real-time VMEbus target processors with a wide range of available I/O modules. A key feature of the Solar System is that it separates the Unix environment from the real-time VMEbus subsystem. By maintaining the separate, yet linked, subsystems, neither system is compromised. Prices for a typical target system start at $7995, while prices for a development system start at $27,595.

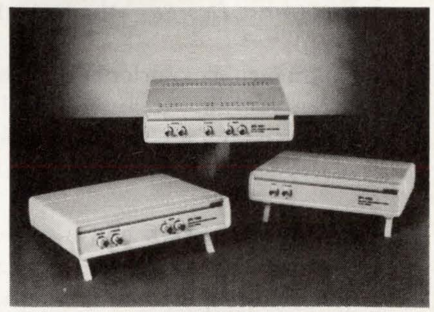
Matrix Corp., 1203 New Hope Rd., Raleigh, NC 27610; (919) 231-8000. **CIRCLE 708**

ADAPTER ADDS SERIAL AND PARALLEL I/O TO SCSI

The limited expansion capability of low-cost workstations no longer need be a limiting aspect of the system thanks to the SLAT-1. The SCSI local-area network adapter connects to the SCSI port that is typically available on all Unix workstations.It adds either one bidirectional parallel port, four serial ports and one parallel port, or up to eight serial and one parallel port to the workstation. Serial data rates of up to 150 kbits/s and full dial-in and dial-out modem capabilities, as well as hardware flow-control signals are available. The parallel port can operate at either 30 or 250 kbytes/s, depending on the adapter version. Prices for the 4-by-9-by-10-in. SLAT-1 adapter start at $575 for the parallel-only version plus a $100 site-license fee for the control software. The versions with 4 or 8 serial ports sell for $900 and $1595, respectively.

Uninet Peripherals Inc., 1209 Warner Ave., Santa Ana, CA 92705; (714) 546-1100, Paul Hammond. **CIRCLE 709**

UNITS GIVE DSP CARDS HIGH-SPEED ANALOG I/O



A family of analog I/O systems allows continuous real-time digital signal processing in PC environments. The systems are for use with Burr-Brown's DSPeed processing cards, which employ either the 16- or 25-MHz version of AT&T's WE DSP32 floating-point digital signal processor or the 50-MHz DSP32C. They enable the processor cards and the company's DSP development software, DSPlay XL, to obtain real-world signals with higher resolution than most other systems currently available. Used as development and interface systems, they can also speed the integration and testing of Burr-Brown's ultra-high-performance PCM78, ADC603, and ADC701 analog-to-digital converters.

The ZPD1001 offers 16-bit analog I/O and sampling rates to 150 kHz. The ZPD1002 features single or dual analog input with 12-bit, 10-MHz analog-to-digital conversion. Single analog input with 16-bit, 500-kHz resolution is achieved with the ZPD1003. Prices start at $1249, $2495, and $2295 for the ZPD1001, 1002, and 1003, respectively. All three systems are delivered from stock to four weeks.

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ 85734; (800) 548-6132. **CIRCLE 710**

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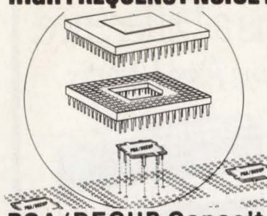

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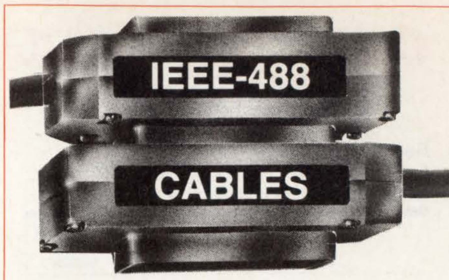

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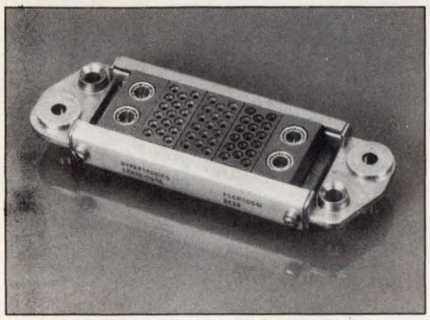

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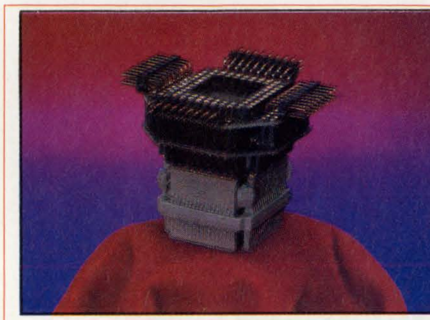

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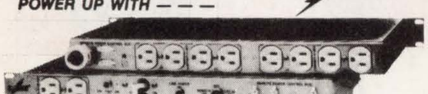

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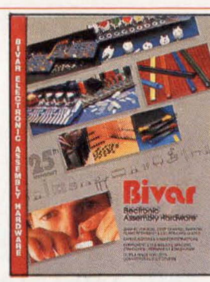

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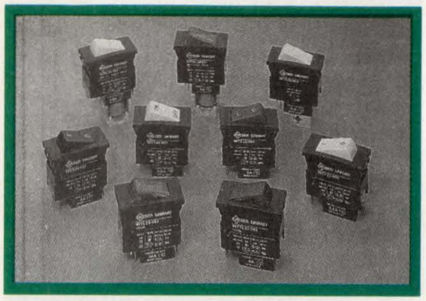

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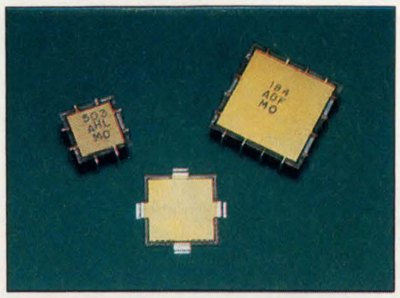

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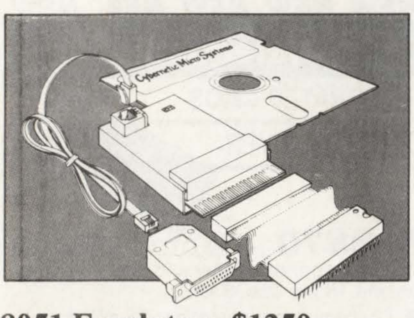

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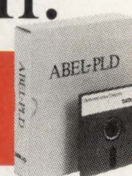

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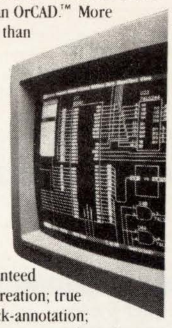

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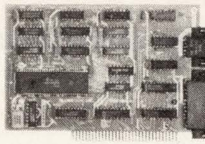

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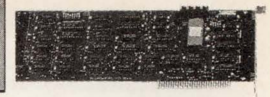

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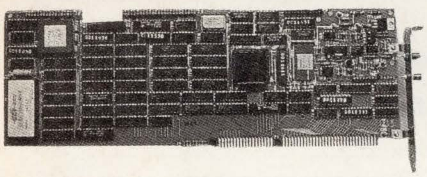

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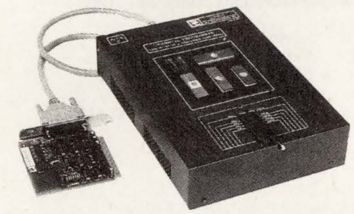

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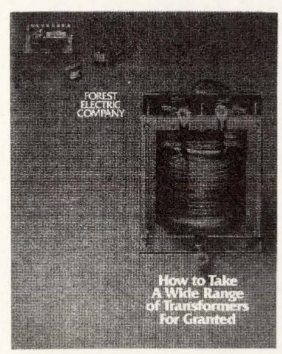

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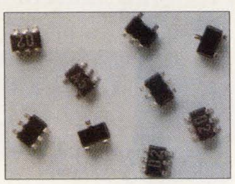

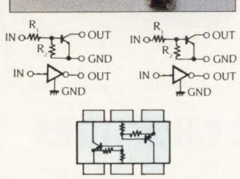

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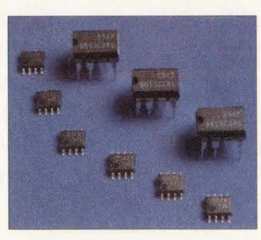

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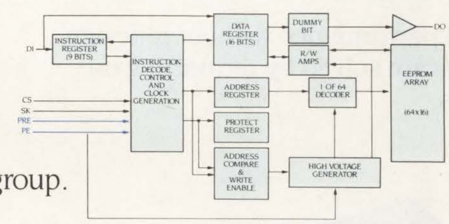

For more details, call Warren Schoals, the studious guy standing in the back. (Warren's also known as Mr. Whiteshirt when he's not out in his pick-up.)

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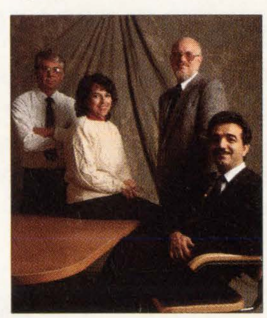

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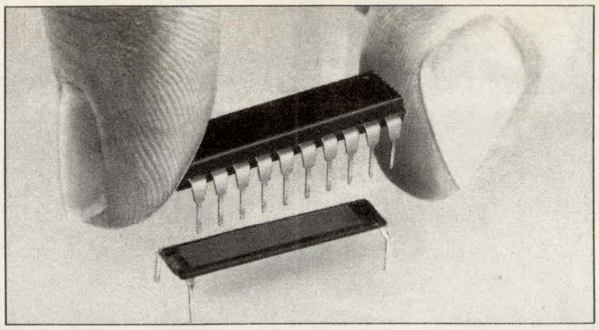

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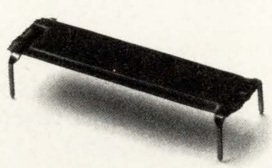

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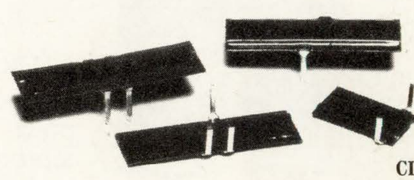

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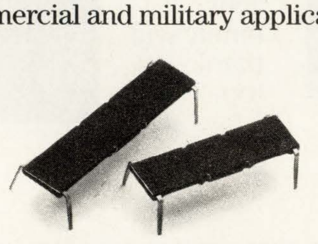
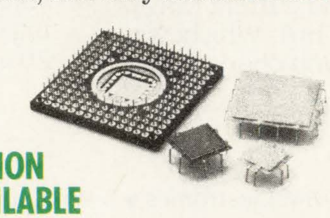


CIRCLE 107

MICRO/Q 3000 CAPACITORS

Reduces noise associated with the use of PGA and PLCC devices. Several part sizes are available to address a variety of package sizes, Micro/Q 3000 is designed to be used with all 16/32-bit MPUs, DSPs, GSPs, FPPs, gate arrays, standard cells, and fully custom ASICs.



SMT VERSION NOW AVAILABLE

CIRCLE 108